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Abstract— This paper presents an analysis and comparison of boundary conduction mode (BCM) and continuous conduction mode (CCM) in single phase power factor correction (PFC) applications. The comparison is based on double pulse tester (DPT) characterization results of state-of-the-art superjunction devices in the 600V range. The measured switching energy is used to evaluate the devices performance in a conventional PFC. This data is used together with a mathematical model for prediction of the conducted electromagnetic interference (EMI). This allows comparing the different devices in BCM and CCM operation modes and evaluating the performance as a function of the PFC power density and efficiency.

Keywords— Power factor correction (PFC), boundary (BCM), continuous conduction mode (CCM), conducted EMI, power density, efficiency, evaluation

I. Introduction

Power factor correction (PFC) circuits are widely used in industrial and household applications to fulfill the power factor and harmonic standards. This type of circuits are traditionally used in continuous conduction mode (CCM) configuration, however, nowadays the boundary conduction mode (BCM) solution has become a highly adopted solution because of its control scheme simplicity. The main disadvantage of converters operating in BCM is the increased inductor ripple that increases the differential mode input EMI filter requirement. Moreover, the current stress in all the components is increased, which negatively affects the converter conduction losses. On the other hand, the inductor size is reduced compared to CCM operation and the switch turn-on losses can be heavily reduced with zero current switching (ZCS) and valley switching to recover part of the energy stored in the switch output capacitance.

BCM operation has gained interest since the introduction of cascode 650 V Gallium Nitride (GaN) devices. These devices are formed by using a cascode connected low voltage silicon (Si) MOSFET with a normally on GaN switch. The interconnection of these devices makes cascode structures to present very low turn-off loss, which is almost independent of the current level [1]. This phenomenon happens because the output capacitance of the low voltage side MOSFET and the input capacitance of the GaN switch get charged in parallel by the load current at the turn-off event, minimizing the GaN

channel turn-off losses. Therefore, switches configured in cascode structure are very attractive for high frequency BCM operation, since the increased current level at the main switch turn-off event will have very little effect on the converter switching losses [2]. Moreover, GaN devices in cascode structure are very attractive for synchronous rectification applications due to the reduced reverse recovery compared to 600 V Si super junction structures. The reverse recovery energy corresponds to that of the low voltage MOSFET in the cascode configuration, and according to [2], this energy is a couple of orders of magnitude smaller than that of a vertical super junction Si device. The possibility of using synchronous rectification allows to further extend the operating power range of BCM converters, which makes this operation mode even more attractive.

In order to analyze the attainable advantages by using different semiconductor devices in PFC applications operating in CCM and BCM, it is necessary to evaluate the semiconductor loss and to compare the solutions in terms of converter power density. The semiconductor conduction loss can be calculated from the data provided in the manufacturer datasheets, but the switching loss needs to be evaluated and characterized. On the other hand, a mathematical model for prediction of the conducted EMI noise needs to be used to evaluate and compare the input filter requirement for different case studies. This paper presents a design oriented methodology for power factor corrector implementation based on double pulse tester (DPT) dynamic characterization to evaluate the switch-diode pair energy loss. Using this data and the manufacturer datasheets, the semiconductor switching and conduction loss can be calculated for half a line cycle. At the same time, the inductor size can be estimated based on the energy requirement $(1/2 \cdot I_{peak}^2 \cdot L)$. The input filter requirement can be evaluated based on the calculated quasi peak and peak noise from the calculated harmonics across half the line cycle.

II. Dynamic Characterization

The devices dynamic characterization is performed in a low inductive DPT. This circuit is the basic configuration used to evaluate the dynamic performance of different switches

technologies under clamped inductive load operation. The prototype has been designed to minimize the parasitic inductances and capacitances in the switching loop [3]. The main switch current is measured using a flat current shunt structure to minimize the parasitic inductance inserted in the loop and maximize the current measurement bandwidth.

The characterization procedure is the same followed in [4]. The CCM switching losses can be directly extracted from the double pulse tester measurements (Fig. 1). The BCM turn-off losses are obtained directly from the DPT measurements as well, but the turn-on losses are reduced compared to the measurements due to the valley switching operation. In order to obtain the MOSFET switching loss for BCM operation, the energy loss is measured under zero current switching conditions at the turn-on and turn-off events. Under zero current conditions the energy loss measurement at turn-on will correspond to the diode junction capacitance energy. In the same way, under zero current conditions at turn-off, the energy corresponds to the MOSFET output capacitance stored energy. Once these values are obtained, it is possible to estimate the MOSFET-diode pair performance under valley switching operation if the amount of energy loss at turn-on and energy recovered during the valley switching subinterval are calculated as a function of the converter input voltage (Fig.2).
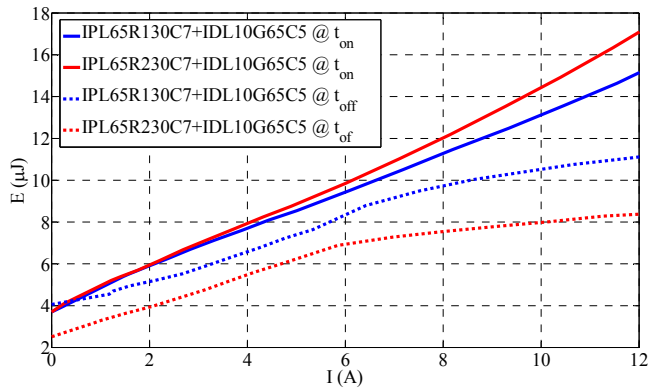

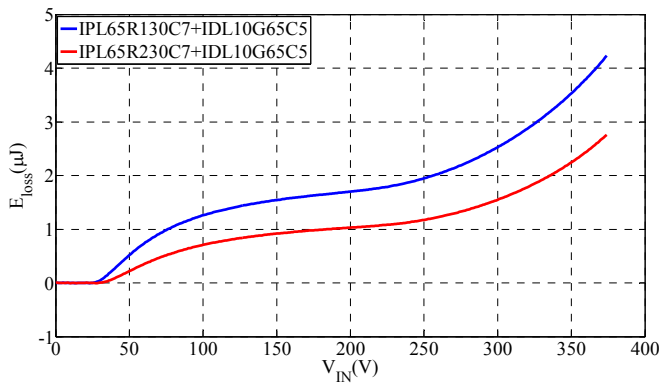Fig. 1. Measured turn-on and turn-off energy loss as a function of the current level

Fig. 2. Calculated remaining turn-on energy loss under BCM operation as a function of the converter input voltage

III. CONDUCTED EMI PREDICTION

Using a mathematical model for conducted EMI prediction enables to directly compare the EMI filter requirements for both CCM and BCM operation modes. This paper uses a mathematical model based on the work presented in [5], [6] to calculate the quasi peak conducted EMI noise under boundary and continuous conduction mode operation for a conventional single phase PFC, as shown in Fig 3. In CCM mode, the input current waveform can be defined according to the converter input voltage and the output power requirement. For the CCM operation mode deriving the inductor current is a straight forward calculation [7], but for the BCM mode, the switching frequency varies across the line cycle. This switching frequency can be calculated according to [6] as shown in (1).

$$f_{sw} = \frac{\left(V_{pk}/\sqrt{2}\right)^2 \left(V_{out} V_{pk} \sin \omega t\right)}{2 L P_{out} V_{out}} \quad (1)$$

However, the switching frequency is affected by the MOSFET and diode output capacitances, as shown in Fig. 4. As it can be observed, at low inductor current levels the charge of the MOSFET output capacitance creates a delay from the gate turn-off event until the inductor starts to discharge. Moreover, at the end of the inductor discharge, when the current level reaches zero and the output diode becomes reverse biased, the valley switching interval will create an extra delay and a negative current flow in the input inductor that affects the ideally calculated converter switching frequency [4], [8].
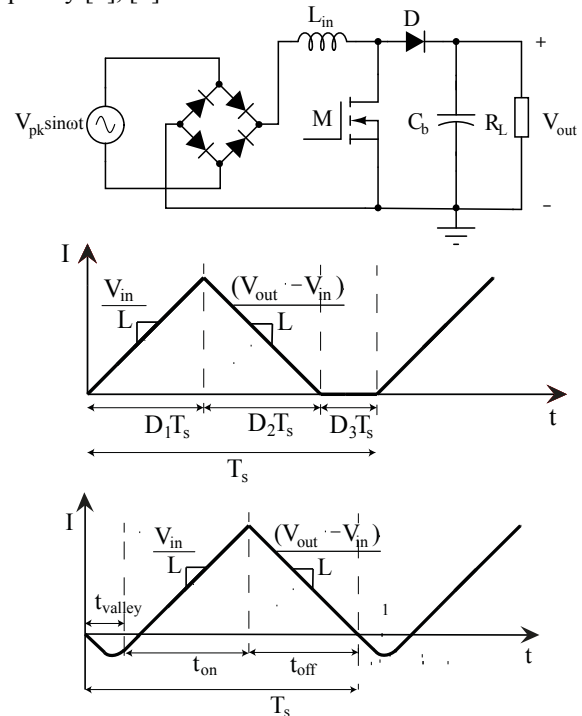

Fig. 3. Conventional PFC schematic and inductor current waveform used for definition of the CCM/DCM and BCM operating modes
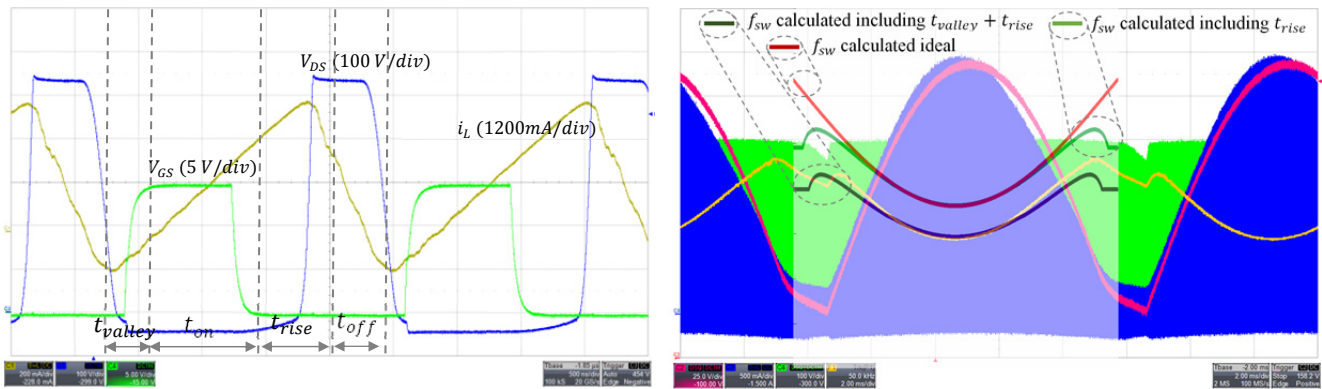
Fig. 4. Left, PFC BCM operating waveforms 500ns/div. Gate waveform (green 5V/div), drain waveform (blue 100V/div) and inductor current (yellow 200 mA/div). Right, MOSFET drain waveform (green 100 V/div), input voltage after the rectifier (red 25V/div), inductor current (blue 500 mA/div) and converter switching frequency variation across line cycle. Yellow measured, red ideally calculated and black taking switching node capacitance into consideration.

The switching frequency across the line cycle can be calculated taking into account the resonant periods between the input inductor and the switching node capacitance. In order to do so, the semiconductor parasitic capacitance can be extracted from the manufacturer datasheet, or measured using the setup shown in Fig. 5. Using a dc blocking capacitor it is possible to measure the variation of the capacitances as a function of an applied dc voltage. Fig. 6 shows the measured capacitance for a MOSFET-diode pair and the PCB switching node parasitic capacitance. The inductor current shape and converter switching frequency are calculated for half line cycle and the harmonics of the inductor current are calculated by approximating the inductor current shape to a pure triangular waveform to simplify the Fourier analysis. Fig. 7 shows a comparison of an average and quasi peak measurement performed over the inductor current of a single phase conventional PFC converter with the conditions shown in Table I.

TABLE I
SYSTEM SPECIFICATIONS AND COMPONENTS

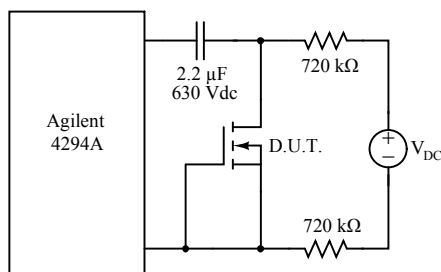|	
Input voltage	$V_{in} = 120\ V_{rms}$
Output voltage	$V_{out} = 389\ V$
Output power	$P_{out} = 100\ W$
Input inductor	$L = 220\ \mu H$
MOSFET	IPL65R230C7 650 V
Diode	IDL10G65C5

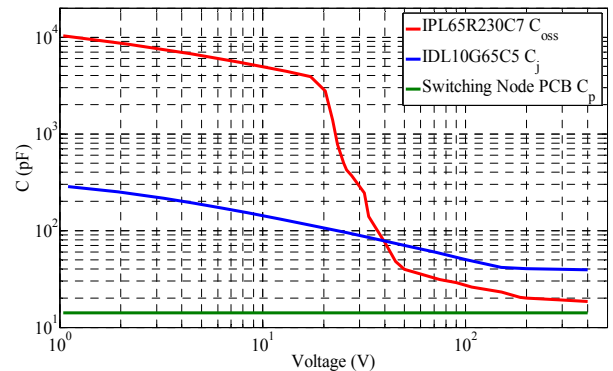Fig. 5 Semiconductor parasitic capacitance measurement setup

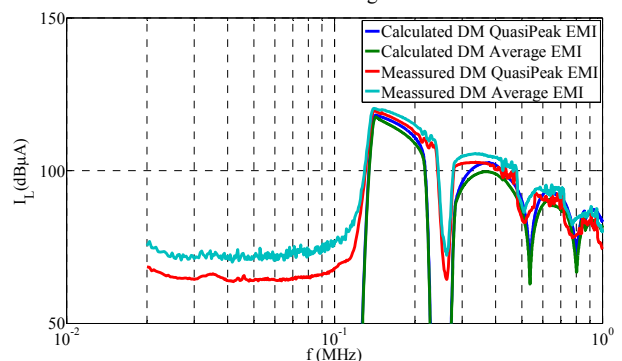Fig. 6. Measured capacitance of the components connected to the converter switching node

Fig. 7. Measured and calculated inductor current conducted EMI

Once the model for calculating the inductor current harmonics has been verified, the harmonics at the measurement point can be calculated by using the equivalent LISN network transfer function. With the calculated LISN network measurement point voltage is possible to calculate the necessary attenuation requirement for fulfilling the conducted standards. At the same time, thanks to the semiconductor characterization data, and the definition of the input inductor current shape across the line cycle, the semiconductor and switching loss can be estimated together with the input inductor energy storage requirement. In this way is possible to perform a comparison of the evaluated devices in BCM and CCM operating modes.

IV. EVALUATION

In this section, a case study for a single phase PFC using the superjunction IPL65R230C7 device with the IDL10G65C5 SiC diode is analyzed. The converter input voltage is $V_{in,rms} = 230\,V$ and the input power is $P_{in} = 200\,W$. The semiconductor pair is evaluated for both CCM and BCM operating modes for an input inductor value ranging from $L_{in} = 100 - 500\,\mu H$ and for a two stage pi filter at the input of the converter as shown in Fig. 8
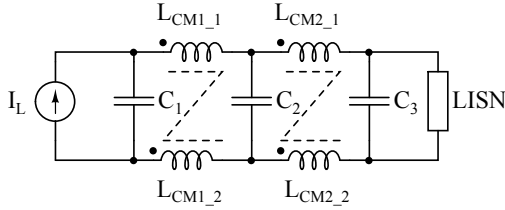

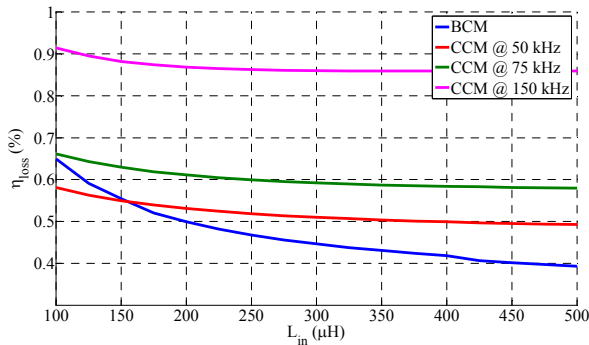Fig. 8 Two stage pi filter loaded with the LISN network

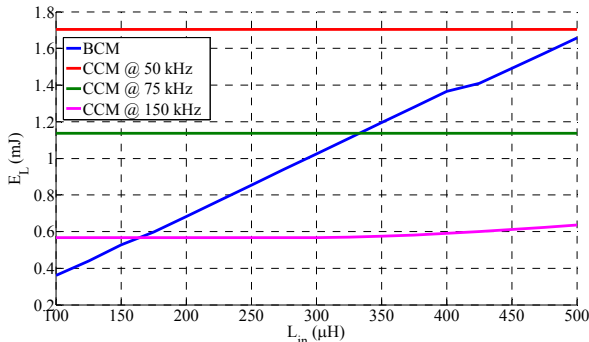Fig. 9 Semiconductor efficiency loss vs. input inductance value

Fig. 10 Input inductor energy strorage requirement vs. input inductance value
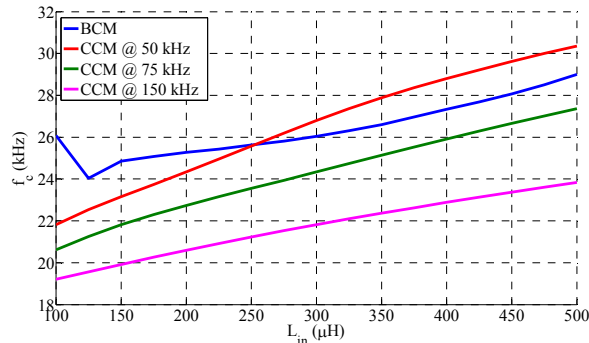

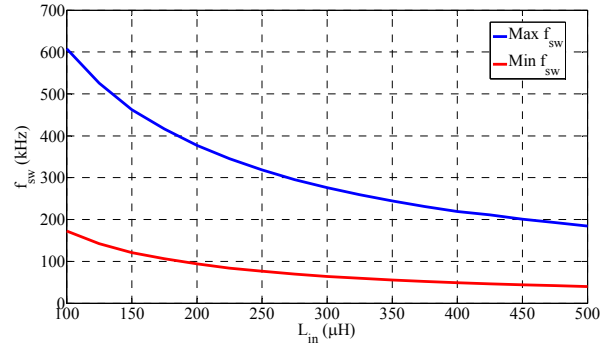Fig. 11 Input filter corner frequency vs. input inductance value

Fig. 12 BCM converter switching frequency vs. input inductance value

Fig. 9 shows the calculated semiconductor efficiency loss as a function of the selected input inductor values for BCM and three different CCM switching frequencies. In the BCM case, as the input inductor value is reduced, the converter switching frequency increases having a negative impact on the semiconductor switching losses. For the CCM cases, as the input inductor value is reduced for the same switching frequencies, the semiconductor loss is increased due to the increased current stress through the semiconductors. It is interesting to see that for this power level, when the input inductor is over 150 µH, the BCM presents the lowest semiconductor loss of all four solutions.

Fig. 10 shows the input inductor energy storage requirement. It can be observed, that for the BCM case at 150 µH, the energy storage requirement is very similar to the CCM at 150 kHz but with almost half the semiconductor loss, and almost three times smaller than the energy storage requirement compared to the CCM case at 50 kHz with similar semiconductor losses.

Fig. 11 presents the calculated corner frequency for the two stage pi filter selected for this analysis. It is interesting to see how only the CCM solution at 50 kHz is able to increase the input filter corner frequency respect to the BCM solution. Increasing the CCM operation frequency does not relax the input filter corner frequency requirement because the third and the second harmonic of the converter switching frequency get into the measurement range. In the BCM case, there exists an absolute minimum corner frequency when the input inductor value is equal to 125 µH. As can be seen in Fig. 12, when the input inductor is at this value, the minimum converter switching frequency reaches 150 kHz which corresponds to the initial frequency in the conducted EMI measurement range. It is important to observe that in BCM mode, the minimum operating frequency corresponds with the peak of the sinusoidal voltage waveform when the inductor current harmonics possess the highest value. As a conclusion, it can be said that the BCM operation is a good candidate for reducing input inductor size while maintaining a low semiconductor loss when compared to the conventional CCM operated converter under 50 kHz switching frequency. If both the input inductor and the input filter size need to be reduced respect to the conventional CCM implementation, MHz range BCM implementations need to be the adopted in order to push the converter minimum switching frequency at maximum power level far away from the beginning of the measurement range.

V. Conclusion

This paper presents a comparison of CCM and BCM modes in single phase PFC applications by evaluating the two operating modes in terms of power density and efficiency. The proposed method uses DPT dynamic characterization results together with the characterized devices' characteristic output capacitance in order to calculate the PFC switching losses through half line cycle both in CCM and BCM conduction modes. This makes it possible to analyze the converter performance for different inductance values and switching frequencies, which in combination with the analytical CCM and BCM conducted EMI models, enables a converter efficiency and power density comparison for different state of the art 600V range devices.

As previously shown in [5] and [4], BCM with valley switching operation, makes prediction of the converter switching frequency a complicated task. In order to obtain accurate results, the resonance periods at the valley interval and at the switch turn off event need to be taken into account. This can be done by obtaining the parasitic capacitances connected to the converter switching node.

The case study analyzed in this work shows that BCM operation mode helps reducing the converter semiconductor loss compared to the CCM implementations. This is due to the fact that, although the current stress through the semiconductors is increased respect to CCM implementations (producing an increased semiconductor conduction loss), the turn-on under ZCS and valley conditions, produce a bigger reduction on the semiconductor switching loss. Moreover, BCM makes it possible to achieve a great reduction in the input inductor energy storage requirement, when compared to conventional 50 and 75 kHz CCM implementations. However, concerning the input filter corner frequency requirement, a reduction in the size compared to a 50 kHz CCM implementation is only possible when the BCM implementation operates in MHz switching frequency range.

Observing Fig. 9 and 12, it can be seen that using these devices in MHz switching frequency range will produce a large penalty in the semiconductor efficiency loss. As it can be observed in Fig. 2, the non-linear capacitance characteristics in superjunction devices, makes this technology not the best option for high frequency BCM implementations. This non-linear capacitance with an abrupt increment at low voltage levels, produces an increment of the semiconductor capacitive switching losses under valley switching operation. On the other hand, GaN implementations in this voltage range help reducing capacitive switching losses under valley operation. Moreover, the cascode configuration with its intrinsic turn-off mechanism makes this technology a firm candidate in BCM MHz implementations pursuing high power density and efficiency.

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