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MOSFET Loss Evaluation for a Low-Power Stand-Alone Photovoltaic-LED System

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***Abstract*- This paper presents a performance evaluation and comparison of state-of-the-art low voltage Si MOSFETs for a stand-alone photovoltaic-LED Light to Light (LtL) system. The complete system is formed by two cascaded converters that will be optimized for a determined solar irradiation and LED illumination profiles. The comparison is performed based on dynamic characterization and evaluation of the devices energy loss at different current levels.**

Keywords— Renewable energy, photovoltaic, stand-alone, LED lighting, switching loss.

I. INTRODUCTION

Renewable energies have become an important part of energy production. Switched-mode power supplies (SMPS) play an important role in the integration of renewable energies due to the requirement of high efficiency conversion. One of the main advantages of renewable energies is the transformation of energy with zero carbon dioxide (CO2) emissions. Moreover, the ability of producing electricity off the grid allows to power up systems at remote locations, where cabling can be challenging and expensive. However, the main disadvantage is that the energy source is intermittent in nature since it strongly depends on the weather conditions. This is especially a drawback for solar energy in northern latitudes where the level of solar irradiation during winter is very low. Moreover, the solar resource in locations far away from the equator is characterized by large annual variations. The length of night and day are very different during the year, consequently, the major part of the solar radiation is received during summer, while there is very little radiation available during winter time as it can be observed in Fig. 1, which shows the annual solar irradiance pattern in a northern latitude [1].

Depending on the converter operating conditions, LED lighting strategy and the amount of available solar irradiance, the operating voltages, duty cycles and consequently current and voltage stresses in the system will vary. In such a system, it is important to investigate the performance of the different components under all the possible conditions. Therefore, it is possible to optimize the system to overcome the limitations due to the geographic location. On the one hand, in locations close to the equator where it is usual to have high irradiance levels all year long, conduction loss will dominate the performance of the system and switching loss will not be as significant. On the other hand, in northern latitudes –especially during winter time– it is important to overcome the low solar radiation by maximizing the system efficiency at low power levels. In this case switching losses will be the predominant source of loss. Switching loss can be difficult to calculate [2] since the result heavily depends on the circuit parasitic inductances and MOSFET input and output capacitances, C_{iss} and C_{oss}, which are highly nonlinear. Instead a measurement of the energy loss is significantly more accurate, since the device performance can be measured at the exact operating conditions. The aim of this paper is to perform a MOSFET loss evaluation for a low-power stand-alone photovoltaic LED system, which will be used in further work to optimize the system for a set of irradiance conditions and LED illumination patterns.

II. SYSTEM ANALYSIS AND SPECIFICATIONS

The investigation of the switching loss will be carried out on a low-power stand-alone photovoltaic LED system for street lightning applications. The system is composed by two parallel-connected monocrystalline panels at the input, a lithium-ion battery for energy storage and eight series-connected Cree XLamp XP-E LED at the output port. Fig. 2 shows the I-V and P-V characteristic curves of photovoltaic panel for different irradiation levels (G). As it can be observed, the output current of a photovoltaic panel varies strongly with changes of irradiation. Fig. 3 shows the LED lamp I-V curve extracted from the component datasheet. Table I presents the specifications of the photovoltaic LED system.

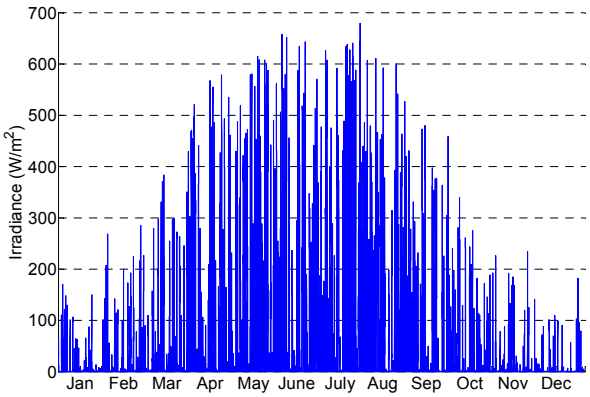

Fig. 1. Annual solar irradiance pattern in a northern latitude

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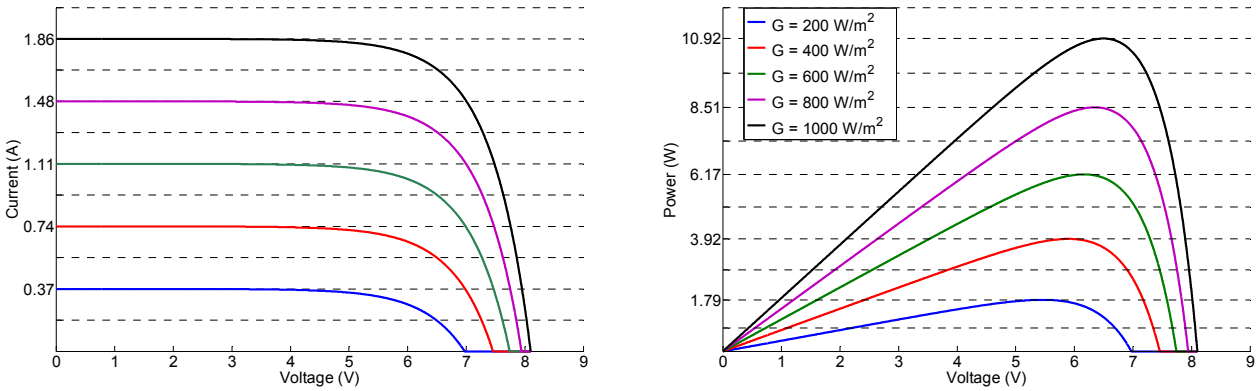


Fig. 2. Photovoltaic I-V (left) and P-V (right) curve characteristic for different irradiation levels (G).

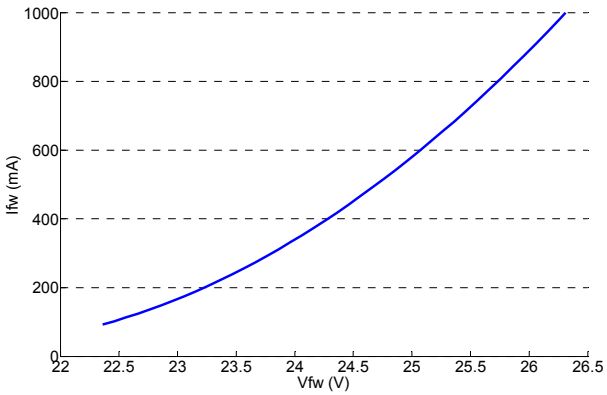


Fig. 3. LED lamp I-V curve (8 series-connected LED).

TABLE I
PV-LED SYSTEM SPECIFICATIONS

P_{PV-max}	10.92 W
V_{mp}	6.5 V
I_{mp}	1.68 A
V_{oc}	8.10 V
I_{sc}	1.86 A
V_{bat}	3.6 V
$Capacity_{bat}$	4.5 Ah
LED	8 x (2.6 − 3.3) V_{fw}

The configuration selected for the Light to Light (LtL) system is a cascaded combination of a buck converter from the photovoltaic panel to the battery and a tapped boost converter from the battery to the LED port, as shown in Fig. 4. An alternative solution to the cascaded configuration is the use of three-port converter topologies (TPC) [3], [4], [5]. Authors claim lower component number, higher efficiency and power density in TPC topologies than in combined separate converters [6], [7]. Nevertheless, many TPC topologies need extra switches and diodes in order to configure the power flow path and to provide controllability [8]. In some topologies, there are switches that are not referenced to ground and need to be active the whole period, which complicates the drive circuitry. In the low-power system under investigation, where the voltages of the photovoltaic panel –especially at low irradiance levels– and the battery are low it is important to avoid any voltage drop, and therefore the use of diodes in the power flow path. A comparison of TPC topologies for low-power stand-alone applications [9] based on component stress factor (CSF) analysis [10], showed that the combination of individual converters provides the best solution, even given the fact that the power from the photovoltaic panel is processed twice in some of the power flows. Therefore, in this application the cascaded structure is preferred because it features low number of components and easy implementation of synchronous rectification in both of the conversion stages. In order to drive the LED port, a high step-up ratio is required. The tapped boost converter is the selected topology because it achieves higher transformation ratio than the flyback topology and presents low number of components. The use of tapped inductors provides the necessary high step-up ratio, which makes it possible to avoid extreme duty cycles and high current stress in the components, reducing switching and conduction losses.

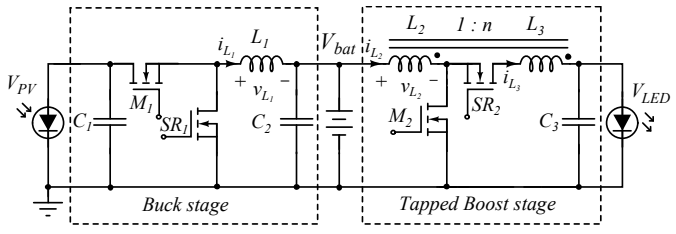


Fig. 4. Light to Light (LtL) system. Buck and tapped boost converters series-connected schematic.

The voltage at the battery port will vary as a function of the load current and battery state of charge (SOC). In order to maintain a stable voltage to perform the measurements, an electronic load configured in constant voltage (CV) mode can be used. However, due to the low voltage and power requirements of the application, a custom build electronic load is used in this work. The schematic circuit and the constructed prototype are shown in Fig. 5 and Fig. 6, respectively. The components used in the prototype are listed in Table II.

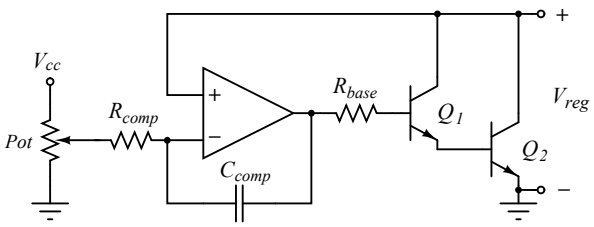


Fig. 5. Schematic circuit of the designed electronic load.

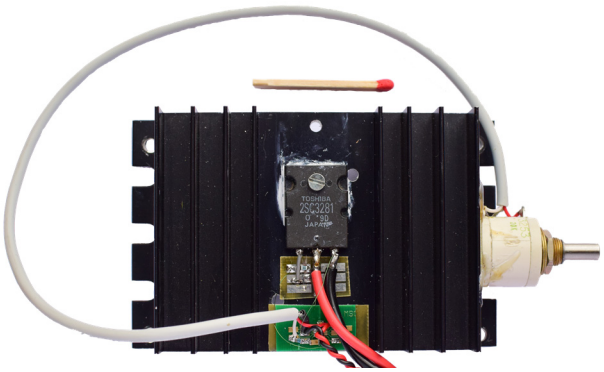


Fig 6. Prototype of the designed electronic load.

TABLE II
ELECTRONIC LOAD COMPONENTS

Q_1	MMBT2222L
Q_2	2SC3281
$op.amp$	MAX4470
R_{base}	470 Ω
R_{comp}	90.1 $k\Omega$
C_{comp}	100 nF
Pot	10 $k\Omega$

The design is based on bipolar junction transistors (BJT) in Darlington configuration in order to achieve high forward current gain. An operational amplifier controls the base current of the BJT pair according to the desired regulated voltage on the collector of the transistors. Therefore, this circuit is used as the load in the buck converter stage (PV panel to battery) in order to keep a regulated voltage during the measurements over the different current values. For the same reason, in the tapped boost converter stage, a power supply with kelvin connection is used at the input port. The kelvin connection is used to regulate the voltage at the converter terminals to achieve a constant voltage over the different current levels. Regarding the load of the tapped boost stage, the 8 series-connected LEDs are used at the output port.

III. SWITCHING LOSS EVALUATION

The switching loss of the LtL system will be evaluated in a buck converter (PV panel to battery) and a tapped boost converter (battery to LED lamp) stages. On the one hand, the switching losses on the buck stage will be measured at different inductor current levels. On the other hand, the switching losses on the tapped boost stage will be investigated for different leakage inductances and stray capacitances of the magnetic component. Both prototypes are implemented using a four layer printed circuit board (PCB) to minimize the areas of the high ac current paths. Moreover, a high bandwidth low intrusive current measurement method as presented in [11], [12], [13], [14] has been used. This current measurement method consists of a parallel combination of resistors with a pick-up wire, which is strategically placed in order to minimize the inductive coupling into the current measurement loop. Fig. 7 shows the implemented prototype with integrated flat current shunt resistors. The current measurement is performed in the main switch as well as in the synchronous rectifier device in both of the stages. The buck converter shunt resistance is composed of 8 parallel-connected 0603 resistors of 500 $m\Omega$ ($R_{shunt} = 62.5\ m\Omega$) for both current paths. The tapped boost converter shunt resistors are mounted in the same way, with a total resistance of 67.5 $m\Omega$ and 100 $m\Omega$ for the main switch and the synchronous rectifier, respectively. Since under low solar irradiation conditions the gate losses are also critical, the devices gate loss in both stages are also evaluated. The gate resistance of the main switch and the synchronous rectifier for both of the stages is $R_g = 10\ \Omega$. The MOSFETs gates are driven with a dual input synchronous driver MCP14700 from Microchip with an output voltage of 5 V. The prototype is designed to accommodate two Power-SO8 devices on each stage. The devices are selected with a low threshold value in order to be fully active at the selected driver voltage. Table III shows the characteristic parameters of the devices under test.

The magnetic components in both of the stages are placed at the bottom side of the board. The inductor value of the buck converter is $L = 33\ \mu H$ and is measured with an impedance analyzer Agilent 4294A. The stray capacitance is obtained from the resonance frequency of the impedance curve $C_p = 2\ pF$. The tapped boost stage switching losses are investigated for the coupled inductors structures shown in Fig. 8. The wire-wound structure core is an ETD29/16/10 and the planar magnetics is an ELP32/6/20, both in material N87 from EPCOS. The inductance value is $L = 18.7\ \mu H$ and $L = 18.56\ \mu H$ for the wire-wound and planar magnetics structure, respectively, with a transformation ratio of 1:5.

TABLE III
CHARACTERISTIC PARAMETERS OF THE DEVICES UNDER TEST

	V_{DS}	$R_{DS(on)}$ @ $V_{GS} = 4.5\ V$	Q_G @ $V_{GS} = 5\ V$	C_{OSS}
IRFH4213	25 V	1.9 $m\Omega$	30 nC @ $V_{DS} = 13\ V, I_D = 50\ A$	1250 pF @ $V_{DS} = 6.5\ V$
BSC050NE2LS	25 V	5 $m\Omega$	5.5 nC @ $V_{DS} = 12\ V, I_D = 30\ A$	450 pF @ $V_{DS} = 6.5\ V$
FDMS5362L	60 V	74 $m\Omega$	8.7 nC @ $V_{DS} = 36\ V, I_D = 17.6\ A$	68 pF @ $V_{DS} = 45\ V$
Si7120DN	60 V	28 $m\Omega$	16 nC @ $V_{DS} = 10\ V, I_D = 10\ A$	136 pF @ $V_{DS} = 45\ V$

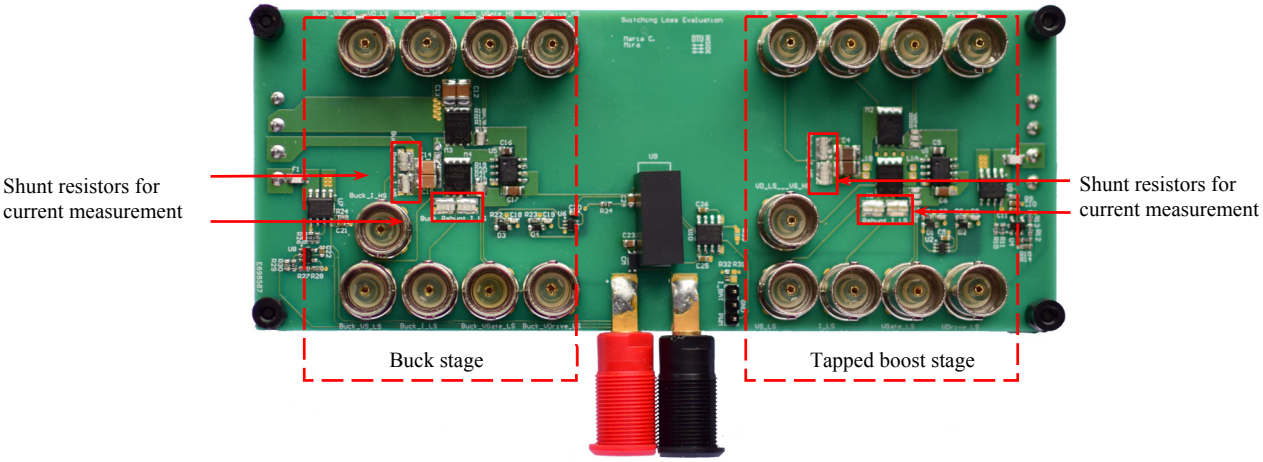


Fig. 7. Buck and tapped boost converter prototypes used to evaluate the switching loss.

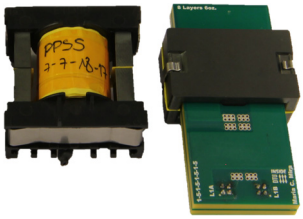
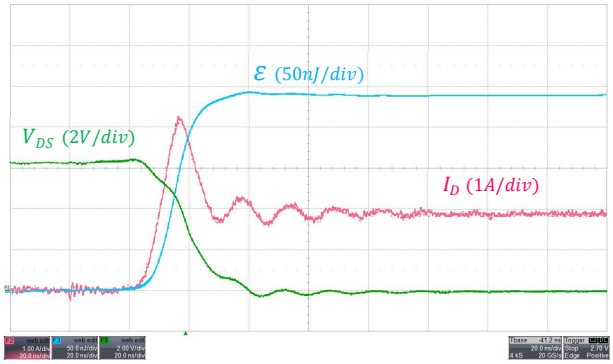


Fig 8. Coupled inductors structures of the tapped boost stage.

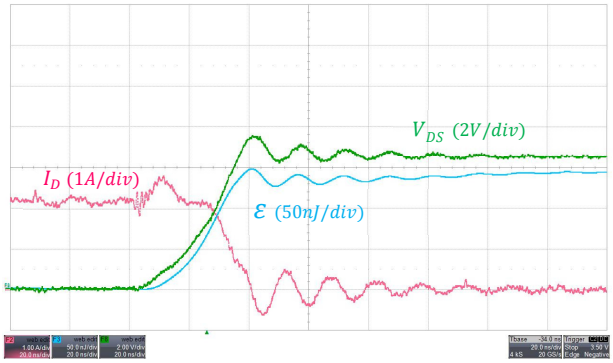
Different coupled inductor structures and interleaving techniques in a tapped boost converter for LED applications were analyzed in [15]. On the one hand, the ETD wire-wound magnetic structure without interleaving (PPSS) presents very low parasitic capacitance ($C_p = 0.73\ nF$) but very high leakage inductance ($L_{lk} = 199.20\ nH$). On the contrary, the planar magnetic structure with full interleaving technique presents very low leakage inductance ($L_{lk} = 18.40\ nH$) but very high stray capacitance $C_p = 4.95\ nF$.

The buck converter stage will be evaluated with the 25 V devices (IRFH4213 and BSC050) for both switches. The input voltage is considered constant ($V_{mp} = 6.5\ V$) since the output voltage of the photovoltaic panel presents small variations with irradiation changes. The tapped boost stage characterization will be performed with the 25V devices as the main switch and the 60 V devices (FDMS5362 and Si7210) as the synchronous rectifier.

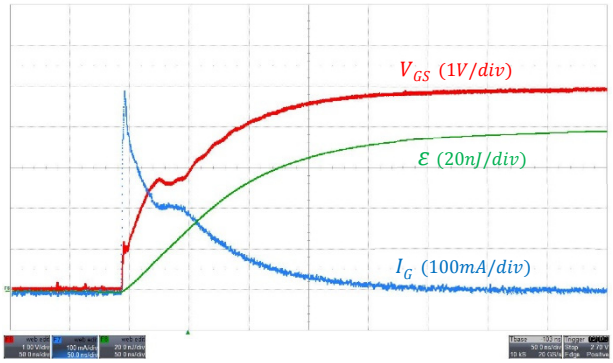
Fig. 9 show the measured switching waveforms of the buck stage with IRF4213 devices. Fig. 9 (a) shows the turn-on event drain-to-source voltage and drain current together with the energy loss. In the same way, Fig. 9 (b) shows the turn-off event of the main switch. Fig. 9 (c) presents the waveforms of the gate-to-source voltage of the synchronous rectifier switch together with the current through the gate resistors and the energy loss. The gate current is obtained from the differential voltage across the gate resistors. The energy measured is half of the total energy loss since the other half is dissipated in the resistive part of the drive circuitry. Fig. 10 presents the measured switching energy at the turn-on and turn-off events together with the energy loss of the main switch and synchronous rectifier gates for different current levels.



(a)



(b)



(c)

Fig. 9. Buck stage measured switching waveforms: turn-on and turn-off event, (a) and (b), respectively, on the main switch IRFH4213. Drain-to-source voltage (green), drain current (light red) and energy loss (light blue). Time scale 20 ns/div. Synchronous rectifier IRFH4213 gate activation (c). Gate-to-source voltage (red), current through the gate resistors (blue) and energy loss (green). Time scale 50 ns/div.

In the same way, the switching energy measurement is performed on the buck stage with BSC050NE2LS devices. Fig. 11 presents the measured switching energy at different current levels. It can be observed that for both of the characterized pair of devices, the gate energy loss is an important part of the total losses, and consequently it cannot be omitted for a low-power application. Fig. 12 shows a comparison of the semiconductor efficiency loss as a function of the available power in the photovoltaic panel for both of the evaluated devices. The switching loss is calculated based on the measured energy loss for a switching frequency of $f_{sw} = 100\,kHz$. The conduction loss is calculated from the semiconductor rms current value. For simplification, both

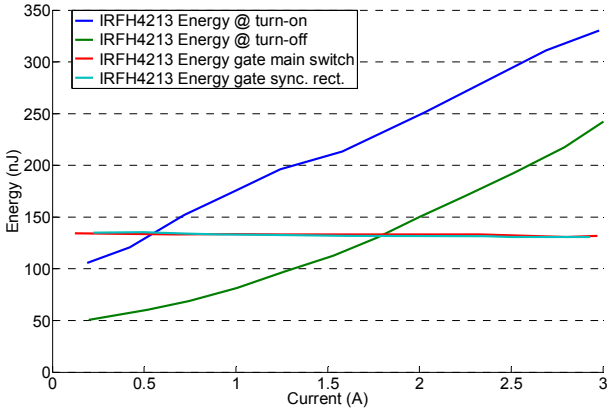


Fig. 10. Buck stage measured energy at different current levels with a pair of IRFH4213 devices.

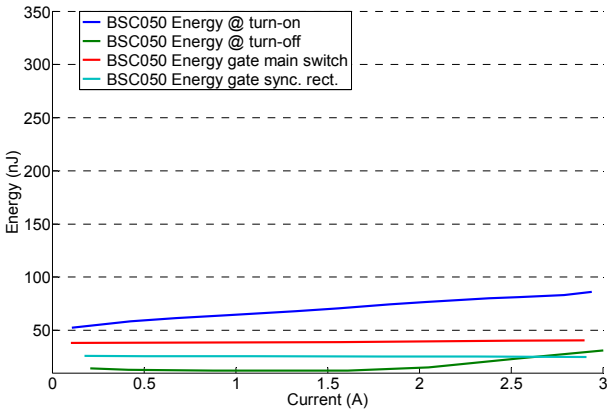


Fig. 11. Buck stage measured energy at different current levels with a pair of BSC050NE2LS devices.

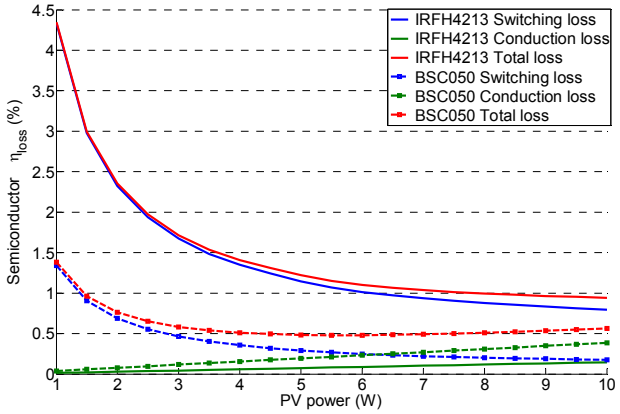


Fig. 12. Buck stage semiconductor efficiency loss for IRFH4213 (continuous line) and BSC050NE2LS (dotted line) devices.

calculations are perfomed assuming zero ripple in the inductor current. As it can be observed, the pair of BSC050NE2LS devices present the lowest semiconductor loss for the whole power range, due to a reduced switching loss. The evaluated IRFH4213 devices possess too large die size area for this application, since the switching losses are predominant over the conduction losses at all the power levels.

Fig. 13 and Fig. 14 show the energy at the turn-on event for a pair of BSC050NE2LS-Si7120 in the tapped boost stage with the wire-wound and the planar magnetics coupled inductor, respectively. As it can be observed in Fig. 13, due to the large leakage inductance of the wire-wound structure, the turn-on event happens under zero current switching (ZCS) conditions producing zero turn-on switching losses on the semiconductor devices. It is important to observe, that even there is no switching loss on the devices in this event, the charge of the coupled inductor parasitic capacitance is done in a resistive way and the same amount of energy stored in this capacitance will be dissipated in the circuit as resistive losses. Fig. 14 shows the same event with the planar magnetics structure. It can be observed that in this case there is much more energy involved in the charge of the magnetic component parasitic capacitance (5A/div compare to 1A/div in the wire-wound structure). Moreover, in this case there is some overlapping between the drain-to-source voltage and the current (the switch current is equal to 2A before the drain voltage drops down). This is due to the fact that the reduced leakage inductance does not delay the current enough to produce ZCS conditions at the MOSFET turn-on.

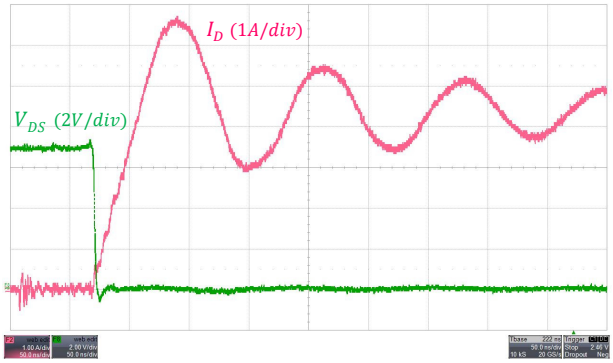


Fig. 13. Turn-on event on the tapped boost stage with ETD wire-wound coupled inductors and BSC050NE2LS-Si7120 devices. Drain-to-source voltage (green) and drain current (light red). Time scale 50 ns/div.

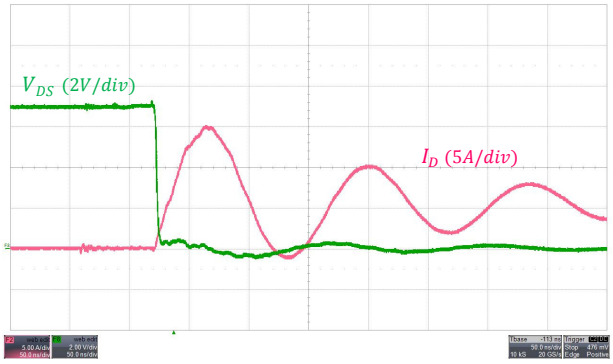


Fig. 14. Turn-on event on the tapped boost stage with planar magnetics coupled inductors and BSC050NE2LS-Si7120 devices. Drain-to-source voltage (green) and drain current (light red). Time scale 50 ns/div.

Fig. 15 shows the turn-on event with the planar magnetic structure and the IRFH4213-Si7120 combination. As it can be observed, the lower switching speed of these devices increases the amount of energy dissipated due to the charge of the parasitic capacitance in the inductors.

Fig. 16 and Fig. 17 presents the measured switching energy on the tapped boost stage with the planar magnetic structure and the wire-wound coupled inductors, respectively, for two combination of devices. Fig. 18 and Fig. 19 show the calculated semiconductor loss as a function of the converter output power or LED power for the planar magnetics and the wire-wound structure, respectively.

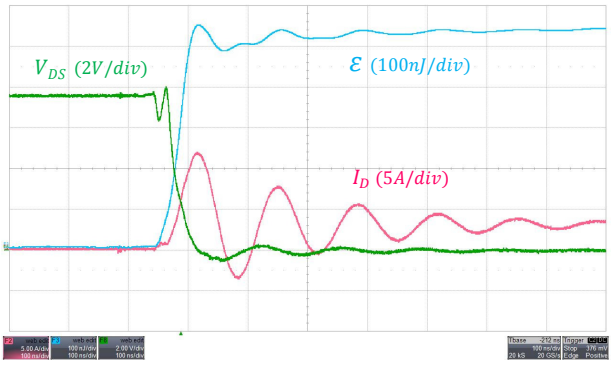


Fig. 15. Turn-on event on the tapped boost stage with planar magnetics and IRFH4213-Si7120 devices. Drain-to-source voltage (green) drain current (light red) and energy (light blue). Time scale 100 ns/div.

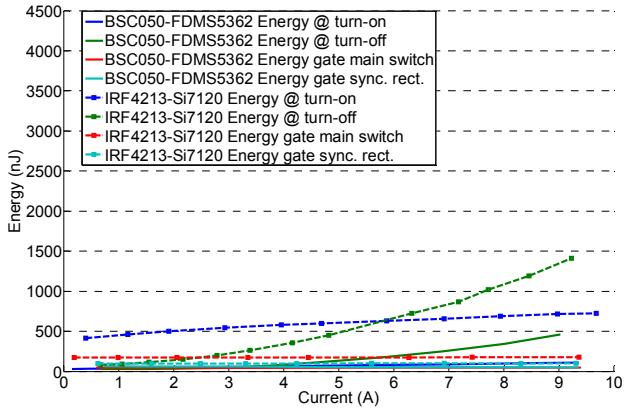


Fig 16. Measured energy at different current levels on the tapped boost stage with planar magnetic coupled inductors.

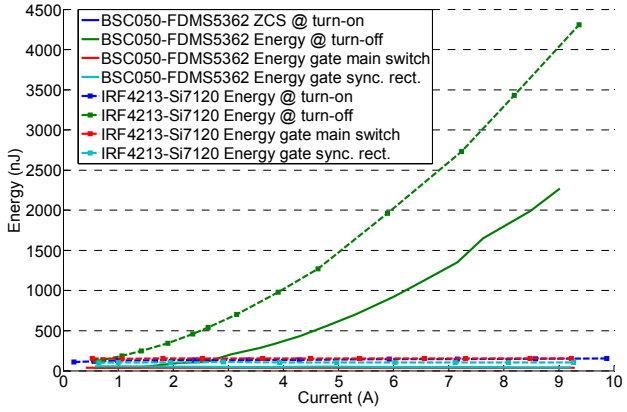


Fig. 17. Measured energy at different current levels on the tapped boost stage with wire-wound coupled inductors.

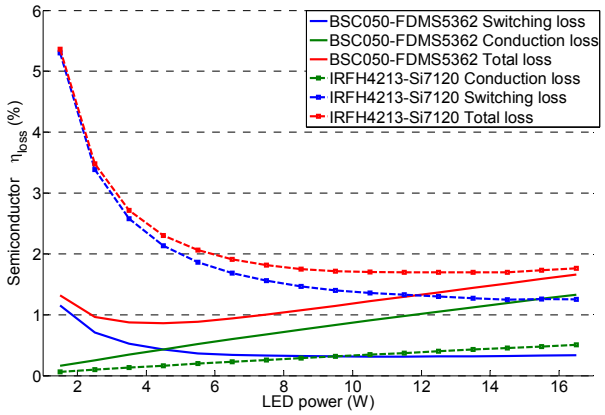


Fig. 18. Semiconductor efficiency loss of the tapped boost stage with planar magnetics coupled inductors.

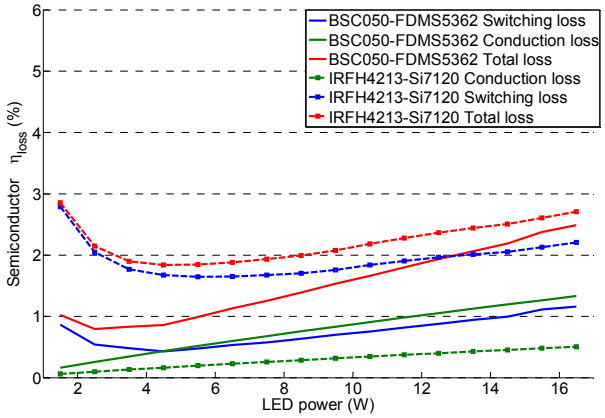


Fig. 19. Semiconductor efficiency loss of the tapped boost stage with wire-wound coupled inductors.

As it can be observed from Fig. 16 and Fig. 18, the high stray capacitance of the planar structure has a negative effect on the semiconductor switching loss at low power levels. This phenomenon is aggravated on the IRFH4213-Si7120 combination due to the reduced switching speed of the devices. However, in the BSC050-FDMS5362 pair, this parasitic capacitance energy will not dramatically affect the semiconductor turn-on loss, but will create energy loss on the circuit parasitic resistances during the charge process, moving the stress to other parts of the circuit. On the other hand, as it can be observed from Fig. 17 and Fig. 19, the increased leakage inductance of the wire-wound structure has a negative effect on the turn-off losses degrading in almost 1% the semiconductor loss at high power levels. Therefore, in this specific application the BSC050-FDMS5362 pair is preferred over the IRFH4213-Si7120 combination because it offers lower total semiconductor loss all the way up to 16 W of output power level, with a 2% improvement in the wire-wound case at 1 W output power level.

IV. Conclusion

This paper presents a MOSFET switching loss evaluation for a low-power stand-alone photovoltaic-LED (LtL) system. The evaluation is performed on a buck stage from the photovoltaic panel to the battery and a tapped boost stage from the battery to the LED output port. The switching energy of several

combination of devices, together with the gate loss energy of the main switch and the synchronous rectifier are measured. Based on the energy measurement, a semiconductor efficiency loss is calculated for both of the analyzed power stages.

In the buck stage the energy measurement shows that the gate energy loss is a significant part of the total losses, especially at low power levels. In the case of the IRFH4213 device, the gate loss of both switches at 1 W corresponds to 2.6% of the total power loss. Therefore, for a low-power application it is important to select a MOSFET with a small total gate charge. The calculated semiconductor efficiency loss of the buck stage presented in Fig. 12 shows an improvement of 3% on the total semiconductor loss at the lowest power level by using the devices with the lower gate charge (BSC050NE2LS). Moreover, this combination performs better over the whole power range of the converter because the reduction in conduction losses of the IRFH4213 is not visible at the evaluated power levels.

The tapped boost stage switching losses are investigated for two coupled inductor structures, with very different leakage inductances and parasitic capacitances. The effect of the high stray capacitance of the planar structure has a negative influence on the turn-on losses, especially at low power levels. However, not all the energy loss from the charge of this capacitance is visible at the MOSFET turn-on event. This is due to the fact that the parasitic inductances produce a delay in the current at turn-on, creating ZCS turn-on conditions depending on the switching speed of the device. This phenomenon can be observed by comparing Fig. 18 and Fig. 19. As it can be seen, the planar magnetics structure produces an increase of the semiconductor switching loss in the IRFH4213-Si7120 combination, but not in the BSC050-FDMS5362 pair. It is importance to notice that even if the parasitic capacitance has not a negative impact in the semiconductor switching loss (because of the ZCS conditions at turn-on), this parasitic capacitance will produce joule losses in different parts of the circuit. On the other hand, the high leakage inductance of the wire-wound magnetic component presents a significant impact on semiconductor turn-off losses. In the application under analysis the LED lighting strategy will operate most of the time at low power levels. In this case, the wire-wound structure with the BSC050-FDMS5362 pair is preferred over the planar structure and the IRFH4213-Si7120 combination, since it offers the best performance due to reduced magnetic and semiconductors parasitic capacitances.

The performed experimental work allows to create an accurate semiconductor loss breakdown, which can be used to perform an optimization for achieving minimum energy loss under a specific irradiance and LED illumination profiles. Therefore, this analysis allows for component selection and optimization of the PV-LED system for different geographic locations.

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REFERENCES

[1] "http://www.soda-is.com," Data Solar Radiation. [Online].

[2] Y. Ren, M. Xu, J. Zhou and F. Lee, "Analytical Loss Model of Power MOSFET," *IEEE Transactions on Power Electronics,* vol. 21, no. 2, pp. 310-319, 2006.

[3] Z. Zhou, H. Wu, X. Ma and Y. Xing, "A Non-Isolated Three-Port Converter for Stand-Alone Renewable Power System," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society* , 2012.

[4] H. Wu, Y. Xing, Y. Xia and K. Sun, "A Family of Non-Isolated Three-Port Converters for Stand-Alone Renewable Power System," in *IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society* , 2011.

[5] H. Wu, Y. Xing, R. Chen, J. Zhang, K. Sun and H. Ge, "A Three-Port Half-Bridge Converter with Synchronous Rectification for Renewable Energy Application," in *Energy Conversion Congress and Exposition (ECCE)*, 2011.

[6] N. Femia, M. Fortunato and M. Vitelli, "Light-to-Light: PV-Fed LED Lighting Systems," *IEEE Transactions on Power Electronics,* vol. 28, no. 8, pp. 4063-4073, 2013.

[7] J. Vieira and A. Mota, "Implementation of a Stand-Alone Photovoltaic Lighting System with MPPT Battery Charging and LED Current Control," in *IEEE International Conference on Control Applications (CCA)*, 2010.

[8] H. Wu, K. Sun, S. Ding and Y. Xing, "Topology Derivation of Nonisolated Three-Port DC–DC Converters From DIC and DOC," *IEEE Transactions on Power Electronics,* vol. 28, no. 7, pp. 3297-3307, 2013.

[9] M. Mira, A. Knott and M. Andersen, "A Three-Port Topology Comparison for a Low Power Stand-Alone Photovoltaic System," in *International Power Electronics Conference - IPEC-Hiroshima 2014 - ECCE-ASIA*, 2014.

[10] E. Wittenbreder, "Topology Selection by the Numbers," in *Technical Witts Inc.*, pp. 32-43, March 2006.

[11] J. Ferreira, W. Cronje and W. Relihan, "Integration of High Frequency Current Shunts in Power Electronic Circuits," in *23rd Annual IEEE Power Electronics Specialists Conference, 1992. PESC '92 Record.,* , 1992.

[12] J. Ferreira, W. Cronje and W. Relihan, "Integration of High Frequency Current Shunts in Power Electronic Circuits," *IEEE Transactions on Power Electronics,* vol. 10, no. 1, pp. 32-37, 1995.

[13] M. Danilovic, Z. Chen, R. Wang, F. Luo, D. Boroyevich and P. Mattavelli, "Evaluation of the Switching Characteristics of a Gallium-Nitride Transistor," in *2011 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2011.

[14] J. Hernandez, L. Petersen, M. Andersen and N. Petersen, "Ultrafast Switching Superjunction MOSFETs for Single Phase PFC Applications," in *Applied Power Electronics Conference and Exposition (APEC)*, 2014.

[15] M. Mira, A. Knott and M. Andersen, "Analysis and Comparison of Magnetic Structures in a Tapped Boost Converter for LED Applications," in *International Electronics and Application Conference and Exposition (PEAC)*, 2014.