High Efficiency Reversible Fuel Cell Power Converter

Pittini, Riccardo; Andersen, Michael A. E.; Zhang, Zhe

Publication date:
2014

Document Version
Publisher's PDF, also known as Version of record

Technical University of Denmark

Riccardo Pittini

High Efficiency Reversible Fuel Cell Power Converter

PhD Thesis, November 2014

DTU Electrical Engineering
Department of Electrical Engineering

Riccardo Pittini

High Efficiency Reversible Fuel Cell Power Converter

PhD Thesis, November 2014

High Efficiency Reversible Fuel Cell Power Converter,

This thesis was prepared by
Riccardo Pittini

Supervisors
Michael A.E. Andersen
Zhe Zhang

Release date:	30th November 2014
Category:	1 (public)
Edition:	Final
Comments:	This thesis is submitted in partial fulfillment of the requirements for obtaining the PhD degree at the Technical University of Denmark.
Rights:	©Riccardo Pittini, 2014

Department of Electrical Engineering
Electronics Group (ELE)
Technical University of Denmark
Oersteds Plads bygning 349
DK-2800 Kgs. Lyngby
Denmark

www.ele.elektro.dtu.dk
Tel: (+45) 45 25 25 25
Fax: (+45) 45 88 01 17

Preface and Acknowledgment

This thesis is submitted in partial fulfilment of the requirements for obtaining a PhD degree at Technical University of Denmark. The research has been carried out at the Electronics group in the Elektro Department from December 2011 to November 2014 under the supervision of prof. Michael A.E. Andersen and associate prof. Zhe Zhang.

The PhD project entitled "High Efficiency Reversible Fuel Cell Power Converter" is founded by the Danish Energy Technology Development and Demonstration Programme (EUDP), number 64011-0036 "Green Natural Gas", in cooperation with the industry partners.

- Haldor Topsøe A/S
- DONG Energy A/S
- DTU Energy Conversion
- Dansk Gasteknisk Center A/S
- EA Enegianalyse A/S.

Acknowledgements

During the PhD studies, I have become deeply indebted and grateful to all who has stood by me and helped me throughout this project.

I wish to thank everyone who somehow contributed to the formation of this thesis. My special thanks and deep appreciation goes to:

- My supervisors Michael A.E. Andersen and Zhe Zhang for giving me this opportunity, for their inspiration, encouragement and endless confidence in me throughout the entire project.
- All my colleagues at DTU Elektro for their help, support and constructive discussions. My special gratitude to Henriette and Bertil for making the DTU Electronics group one big family.

- The industry partners for their inputs to the project and many interesting discussions.
- Prof. Johann W. Kolar at ETH Zurich for accepting me as visiting PhD at PES Laboratory during spring 2014. My gratitude also to Partrico Cortes and Dominik Bortis for the inspiring discussions on optimization and design of AC/DC matrix based converters.
- My parents, Provino and Savina, and my sister Ottavia, with family, for their undoubtful support of my choices and their constant belief in me.
- A special thank you to all of who made the difference, shared good and special moments. To Juan and Maria, Gabriel and Adriana, Milovan, Miranda, Lina, Thomas. Thank you for friendship and everything that comes along, for occasional reboot moments, for shots at 2am on a Monday morning, for occasional conversations, for travels and shared experiences. Overall, thank you for making the PhD experience extraordinary.
- Coffee machine for keeping me awake during all those long working days.

A special gratitude to my partner, Maja, for her endless support, belief in me and for being the sunshine in my every day.

Kongens Lyngby, November 2014,

Riccardo Pittini

Abstract

The large scale integration of renewable energy sources requires suitable energy storage systems to balance energy production and demand in the electrical grid. Bidirectional fuel cells are an attractive technology for energy storage systems due to the high energy density of fuel. Compared to traditional unidirectional fuel cell, bidirectional fuel cells have increased operating voltage and current ranges. These characteristics increase the stresses on dc-dc and dc-ac converters in the electrical system, which require proper design and advanced optimization.

This work is part of the PhD project entitled "High Efficiency Reversible Fuel Cell Power Converter" and it presents the design of a high efficiency dc-dc converter developed and optimized for bidirectional fuel cell applications.

First, a brief overview of fuel cell and energy storage technologies is presented. Different system topologies as well as different dc-ac and dc-dc converter topologies are presented and analyzed. A new ac-dc topology for high efficiency data center applications is proposed and an efficiency characterization based on the fuel cell stack I-V characteristic curve is presented.

The second part discusses the main converter components. Wide bandgap power semiconductors are introduced due to their superior performance in comparison to traditional silicon power devices. The analysis presents a study based on switching loss measurements performed on Si IGBTs, SiC JFETs, SiC MOSFETs and their respective gate drivers. Magnetic components are a fundamental part in most power converters and have a significant impact on power converters performance and cost. After basic introduction on magnetic components, planar magnetics are evaluated for fuel cell (high current) applications as possible candidate for reducing the cost of magnetic components especially for large production volumes.

At last, the complete converter design is presented in detailed and characterized in efficiency terms. Both benefits, provided by SiC power devices and by a redesign of the converter layout increased the converter power density up to 2.2 kW/l, achieving efficiency above 98%.

A flyback derived topology designed for low power high voltage applications is also presented as a side task in connection to the PhD project.

Résumé

Den store integration af vedvarende energikilder kræver egnede energioplagringssystemer for at balancere energi-produktion og -efterspørgsel i elnettet. Tovejs brændselsceller er en attraktiv teknologi til energilagringssystemer på grund af den høje energitæthed af brændstof. Sammenlignet med traditionel envejs brændselscelle, har tovejs brændselsceller øget driftsspænding og strømområder. Dette kendetegn øger belastningen på dc-dc- og dc-ac-omformere i det elektriske system, som kræver et ordentlig design og avanceret optimering.

Dette arbejde er en del af ph.d.-projekt med titlen "High Efficiency Vendbar Fuel Cell Power Converter" og præsenterer udformningen af en højeffektiv dc-dc konverter udviklet og optimeret til tovejskommunikation brændselscelleapplikationer.

Først gives en kort oversigt over brændselscelle- og energilagringsteknologier. Forskellige systemtopologier samt forskellige dc-ac- og dc-dc-omformertopologier præsenteres og analyseres. Der foreslås en ny ac-dc topologi til højeffektive datacenterapplikationer og en effektivitetskarakterisering baseret på brændselscellestakkens I-V-kurvekarakteristik er præsenteret.

I anden del er de vigtigste omformerkomponenter diskuteret. Bredbåndgabs effekthalvledere introduceres på grund af deres overlegne ydeevne i forhold til traditionelle siliciumeffekthalvledere. Analysen viser en undersøgelse baseret på skiftetabsmålinger foretaget på Si IGBT'er, SIC JFET'er, SIC MOSFET'er og deres respektive gate drivere.

Magnetiske komponenter er en grundlæggende del i de fleste omformere og har en betydelig indvirkning på omformernes ydeevne og pris. Efter en grundlæggende introduktion til magnetiske komponenter, er planar magnetik evalueret til brændselscelleapplikationer (høj strøm) som mulig kandidat til at nedbringe udgifterne til magnetiske komponenter ved store produktionsmængder.

Til sidst bliver det komplette omformerdesign præsenteret i detaljer og karakteriseret i form af effektivitet. Fordelene ved SiC-effekthalvlederne og et redesign af omformerens layout øger omformerens effekttæthed op til 2.2 kW/l og bevirker en effektivitet over 98%.

En flyback afledet topologi designet til laveffekt højspændingsapplikationer præsenteres som en sideopgave i forbindelse med dette ph.d.-projekt.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Scope

The scope of this thesis is to present results achieved as part of the PhD project "High Efficiency Reversible Fuel Cell Power Converter" carried out by the author during the period from December 2011 till November 2014. The scientific results of the research have been published in form of peer reviewed conference and journal papers. The published papers form an integral part of this thesis and are included in Appendix.

The objective of this thesis is to supplement the already published information, and thereby present a more coherent and complete overview of the research work and results obtained in the project.

Furthermore, this thesis with its appendix condenses a large amount of advanced knowledge on design of high efficiency dc-dc converters. Work carried through this thesis is useful to power engineers who are about to design high efficiency dc-dc converters in the multi-kW power range for fuel cells and other applications.

1.2 Thesis Structure

The structure, organization and content of this PhD thesis are visualized in Figure 1.1 and 1.2. The flow chart guides the reader through the thesis contents starting from a general system view, moving towards more detailed view of wide bandgap devices and magnetics components. The last part presents an example of the complete converter design.

The main project contributions are highlighted through the different chapters and sub-chapters in Figure 1.1 and 1.2.

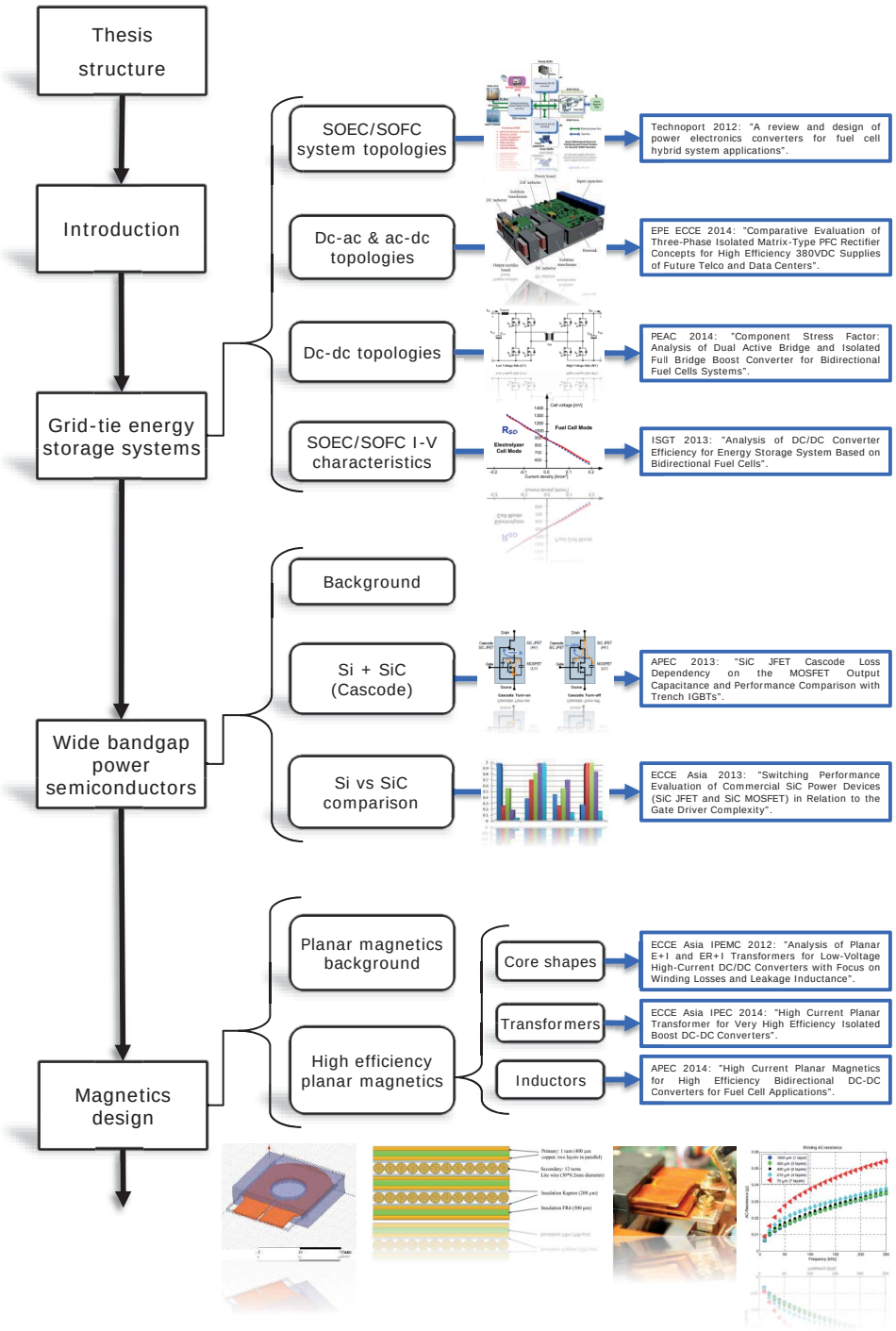


Figure 1.1: Thesis structure part 1/2.

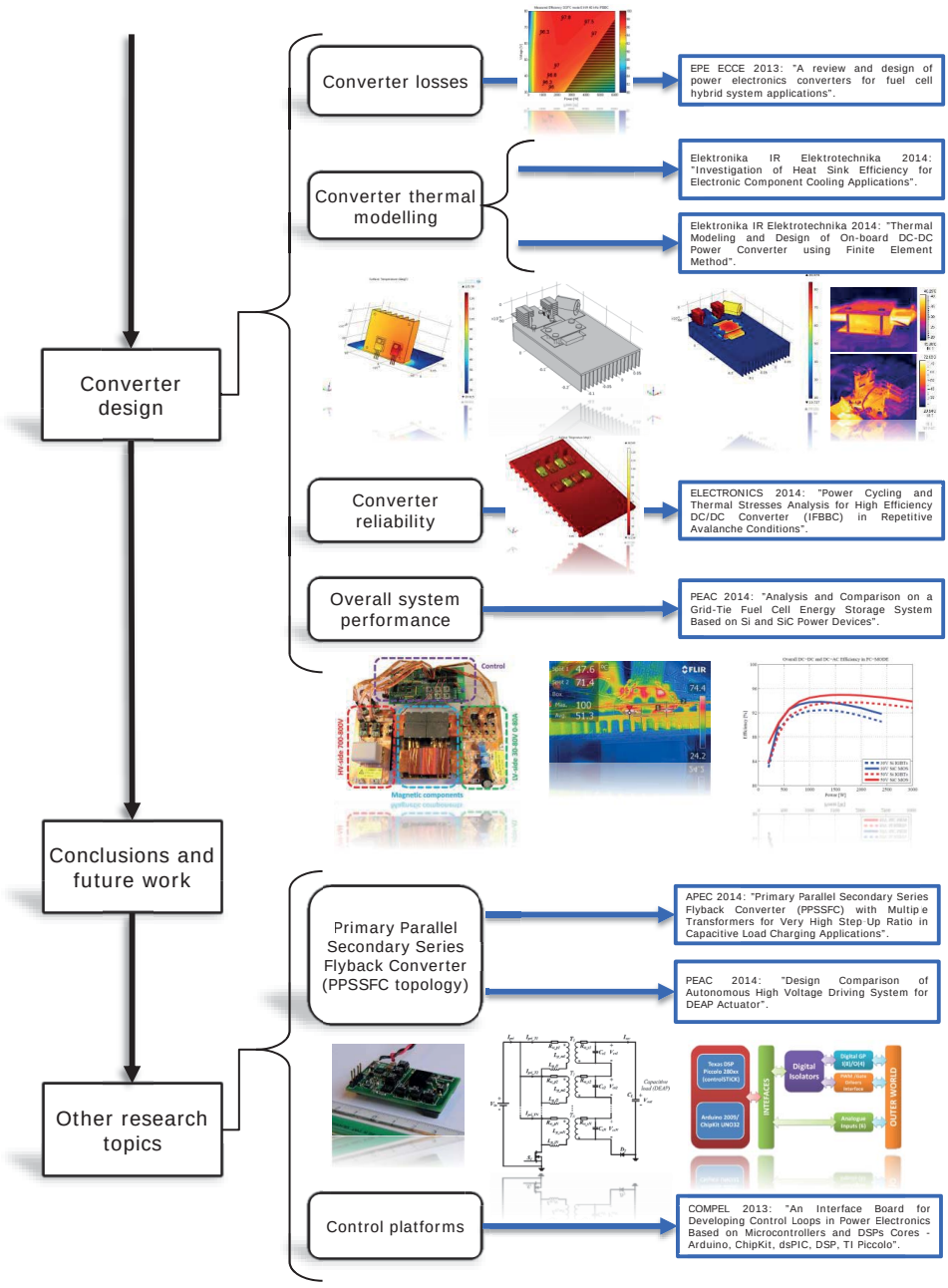


Figure 1.2: Thesis structure part 2/2.

1.3 Background and Motivation

The current electric grid is almost 100 years old. The grid infrastructure has been updated, but its topology remained unchanged for decades. Over the last two decades there has been a large scale diffusion of renewable energy sources due to the global awareness on the limited availability of natural resources. Renewable energy sources are mostly unpredictable and create high dynamics in the energy production. Traditional grid struggles to couple with high dynamics due to the limited information on the status of the grid as a system. Thus, the traditional grid is progressively moving towards a smart grid [1] where large use of information technology provides increased reliability, better dynamic load adjustment and efficiency, by balancing the energy production and demand, as shown in Figure 1.3.

Energy storage systems are fundamental components in smart grids [2]; they balance the energy production and demand, when there is an excess of power from the renewable energy sources or vice versa. For these systems, bidirectional fuel cells represent an attractive technology due to the high energy density of fuel. Bidirectional fuel cells typically operate at low voltages and high current levels, which furthermore challenge the design of high efficiency power converters [3]. In order to limit the converter losses, large amount of prime materials, such as copper and silicon, is required. This results in an increase of the converter cost and complexity. For these reasons, it is necessary to accurately model and design power converters by selecting suitable technologies that can potentially reduce the converter cost.

Nowadays, the latest developments in power semiconductor technology, resulted in commercially available dc-ac converters with efficiency up to 99% [4] and above [5, 6]. This highlights that absolute converter efficiency is not the main concern anymore; the new focus is the cost reduction in terms of lower amount of prime materials, less components and automated manufacturing.

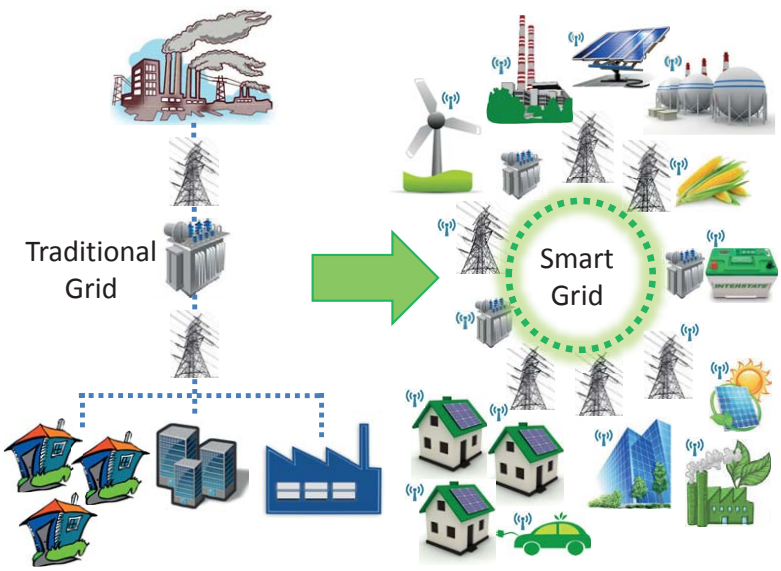


Figure 1.3: Electrical grid evolution from traditional grid to smart grid.

In traditional fuel cell applications dc-dc conversion efficiency up to 98% has already been proven [7]. This is not the case for bidirectional fuel cells, where the large operating ranges that the dc-dc converter is expected to operate impose significant design challenges in order to achieve such efficiency. The use of new power semiconductors and high current planar magnetics could provide the desired system efficiencies and at the same time reduce the cost of magnetic components. For all these reasons, bidirectional dc-dc efficiency is the major interest of this PhD thesis.

1.4 Project Objectives

The project was established to study the efficiency of electrical power conversion in bidirectional grid-tie fuel cell systems. The main goal was to establish a prototype of a high efficiency dc-dc that could cope with the increased requirements in operating voltage range typical of bidirectional fuel cells.

The major project objectives are:

- Demonstrate high efficiency bidirectional low voltage high current dc-dc conversion for bidirectional fuel cells. The aim is to achieve dc-dc conversion efficiency above 98% even when the converter is designed to operate in a wide voltage range.
- Investigate new power semiconductors; study their performance compared to traditional Si power devices and verify their potential in for bidirectional grid-tie fuel cell systems.
- Study high current magnetic components taking into account manufacturing issues. Planar magnetics can be a viable solution to reduce the manufacturing cost of the magnetic components, however it is particularly challenging to design high efficiency low-voltage high-current planar magnetics.

Chapter 2

Grid Tie Energy Storage Systems

This chapter presents a system overview of bidirectional energy storage systems and power converters.

2.1 Grid Tie Energy Storage Systems

Sustainability is the major driving force for large scale diffusion of renewable energies. The large scale adoption of renewable energy requires energy storage systems to balance the energy demand and energy production [2]. In fact, renewable energy sources are mostly unpredictable [8] and energy storage systems are required to guarantee a continuous energy supply even during periods with low energy production [2]. This is especially true with a large percentage of renewable energy over traditional energy sources (e.g. coal, gas, etc.).

The main energy storage technologies for grid applications [9] can be summarized in

- Pumped hydro
- Compressed air storage
- Batteries
- Power-to-gas: hydrogen and synthetic natural gas
- Flywheel
- Molten salt

From all these energy storage technologies, power-to-gas systems [10] represent an attractive solution, since energy can be stored as a high energy density fuel. Moreover, these systems can be used to produce natural gas or hydrogen [10], which can be further used for other applications, such as residential and urban mobility [11].

2.2 Bidirectional SOEC/SOFC Technology

Fuel cell (FC) technology is divided into two main categories: proton exchange membrane (PEM) [12] and solid oxide (SO) [13] fuel cell technology. PEM FCs operate at low temperatures (usually in the 80-90 °C range). Pilot and small commercial projects demonstrate the feasibility of the technology however, until now, the technology struggles to be successful on the market. The major drawbacks of this technology are related to the relatively high cost due to the use of rare materials (such as platinum) [14] and the sensitivity to fuel poisoning (especially to carbon monoxide) [15, 16]. Solid oxide fuel cells /electrolyzer cells (SOFC/-SOFC) are another type of FC technology which has the potential to significantly reduce the materials cost in the FC stacks. This type of FCs have been proven for bidirectional operation, often referred as regenerative fuel cells (RFCs), operate at high temperatures ~1000 °C and are sensitive to degradation [17], which introduces major challenges for the materials used in the construction of the stacks. Newly developed SOEC/SOFC cells operate at more manageable temperatures ($\leq$ 800 °C) which allows cheaper construction materials. SO-technology can operate not only with water, but also with a wider variety of fuels such as CO_2 [18, 19]. This makes SO-technology especially attractive for reducing the CO_2 emissions. Other major advantages of bidirectional SOEC/SOFC technology can be summarized in

- High efficiency at high operating temperatures
- Operates with multiple fuel compositions
- Water and CO_2 can be used to produce synthetic natural gas (SNG) [19]

2.2.1 System Topologies for Bidirectional SOEC/SOFC Fuel Cells

An overview of system topologies for grid tie energy storage with SOEC/SOFC stacks is presented in Figure 2.1. There is no unique suitable system topology [20], however costs and manufacturing challenges impose constrains to the system. Moreover, the maturity of the cells technology imposes physical constrains to cell stacks, such as maximum number of stackable cells, maximum current density, maximum cells voltage, operating temperature, etc.

A preliminary overview of dc-dc and dc-ac power conversion for fuel cell systems is performed in Appendix A. This type of fuel cell systems often includes auxiliary power sources (APS) such as supercapacitors [21] or batteries [22] to compensate the slow transient response of fuel cell systems [23]. In collaboration with a SOEC/-SOFC cell manufacturer and system operator it was determined that an APS is not required, since the typical transient response from the SOEC/SOFC cells is sufficient for the expected dynamics in the ac-grid. It was also determined that a 50-cells stack, with a cells active area of 10x10 cm, would represent a realistic design case. Based on the expertise in the SOEC/SOFC cells technology, the operating conditions for a 50-cells stack were defined as following

- SOEC mode: current up to 80 A
- SOFC mode: current up to 40 A

- Typical operating voltages are in the 50-80 V range for SOEC mode and in the 30-50 V range for SOFC mode
- Planned demonstrator system nominal power ~50 kW.

The listed specifications are used to preliminary define the power converters specifications. Pro and cons of each system topology in Figure 2.1 are summarized in Table 2.1. The topology in Figure 2.1a requires a too large cells stack which is not feasible due to limitations in the SOEC/SOFC cells technology. The topology in Figure 2.1b has centralized dc-dc and dc-ac converters. Since the same current flows through each cell stacks, the monitoring and control system has to compensate for variations in the cells characteristics. Moreover, a major drawback of Figure 2.1b is the required galvanic isolation between the stacks, which is particularly challenging for the fuel system. System topologies in Figure 2.1c and in Figure 2.1d are the most suitable for the state of the art cells. The major difference is related to the light load efficiency and system redundancy. An inverter failure in the system of Figure 2.1c would cause the shutdown of the entire system, while in Figure 2.1d it would cause the shutdown of only one sub-system branch. In terms of light load efficiency, the system in Figure 2.1d has better performance; in fact, it is possible to shutdown the light load operating branches and keep active only one part of the system.

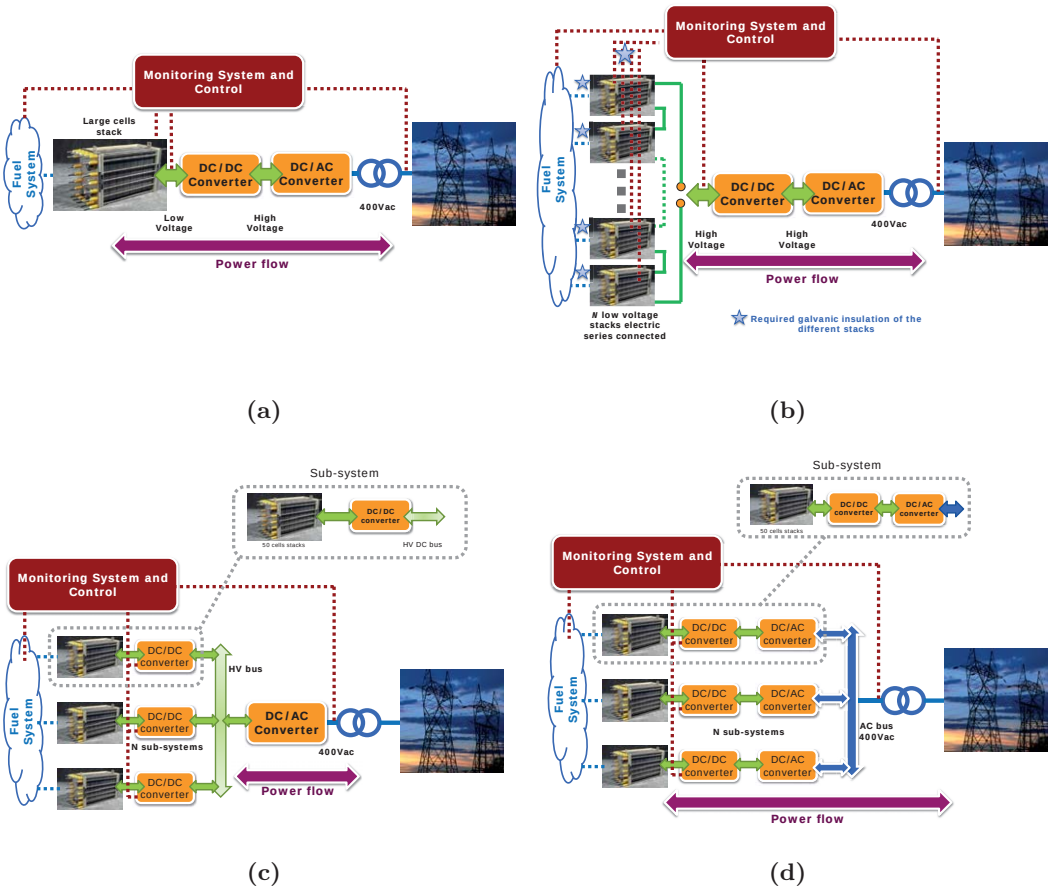


Figure 2.1: Investigated SOEC/SOFC system topologies.

Table 2.1: System topologies advantages and disadvantages

System topology	Advantages	Disadvantages
Figure 2.1a	Few components Two converters	Large stack Light load efficiency Non optimal cells I-V
Figure 2.1b	Small stacks Two converters	Electric insulation Light load efficiency Non optimal cells I-V
Figure 2.1c	Small stacks Optimal stack I-V Light load efficiency	Many dc-dc converters Increased complexity
Figure 2.1d	Small stacks Redundancy Light load efficiency	Many converters System complexity

The reference system is based on Figure 2.1c; it is designed for 10 sub-systems giving a total power rating of ~60 kW in SOEC mode and ~15 kW in SOFC mode.

2.2.2 Dc-ac and Ac-dc Converter Topologies

The ac-side of the system is defined based on the system power rating. Assuming a loss-less system the dc-ac converter in Figure 2.1c is rated to handle the entire power in SOEC mode of all 10 sub-systems. Therefore, the dc-ac converter has to be rated >60 kW; light overrating is desirable in order to have reactive power compensation [24] also at nominal system power.

Single phase systems are suitable for residential applications with typical power levels below 10 kW. Already above 5 kW there is a major trend to shift towards three phase systems due to their lower losses [25]. Multi-kW 400 V_{rms} three phase systems are widely used in industrial environments and are the most suitable systems at these power levels. Higher voltages are usually preferred with power ratings in the range of 500 kW-1 MW (e.g. converters in three phase systems rated at 690 V_{rms} for wind power applications [26]). Therefore, according to the design ratings for the SOEC/SOFC system, a 400 V_{rms} ac system represent the most suitable solution.

Dc-ac and ac-dc power conversion in multi-kW applications is typically performed with two or three level inverter topologies [27]. A typical example is represented by solar inverters, which exceptionally achieved low cost ($/W) and remarkable efficiencies above 98% [28] with traditional silicon power devices and up to 99% [4] with new wide bandgap devices. This latest developments highlight that efficiency is not a major concern any more. Reducing the power converters $/W cost while maintaining high efficiency is now the major focus. In order to achieve these goals, researchers are investigating new power semiconductor materials, which potentially can reduce both semiconductor power losses and converter cost.

Appendix B presents an evaluation of the efficiency improvement achieved in dc-dc and dc-ac converters with the introduction of new power semiconductors (silicon carbide). The analysis is performed on two laboratory converter prototypes. This

allows to quantify the overall efficiency for the SOEC/SOFC system with different power semiconductor technologies. It is observed that an overall electrical system efficiency improvement in the 1-3% range can be achieved. Moreover, it is possible to reduce the size of the converter cooling system and of the passive components, such as inductors and capacitors. This also allows a quick estimation of the economical benefit and payback time for the electrical system.

2.2.3 Integrated Ac-dc-dc Converter Topologies

During the research studies alternative high efficiency ac-dc topologies for data center applications [29] have been investigated. In these applications, the major concern is to increase the power distribution efficiency from the grid level down to the computational units. This can be achieved by increasing the efficiency of the single conversion units and by reducing the number of conversion stages in the system. Besides, compared to traditional ac systems the use of dc power distribution architectures [30] can reduce the number of power conversion stages and provide higher system efficiency [31].

A comparative evaluation of three phase isolated matrix-type PFC rectifiers is presented in Appendix C. The analysis compares different ac-dc PFC rectifier topologies designed for data center applications and presents a new topology, the Isolated Integrated Active Filter Matrix-type (I^2AFM) PFC rectifier, shown in Figure 2.2. The analysis considers two design cases of 7.5 kW converters. One design is based on the isolated matrix-type Y-rectifier topology (IMY-rectifier, [32]) and other on the I^2AFM topology. Both topologies provide significant major advantages, which can be summarized in

- Galvanic isolation
- Sinusoidal ac voltages and currents
- Unitary power factor
- Minimized dc-link capacitance.

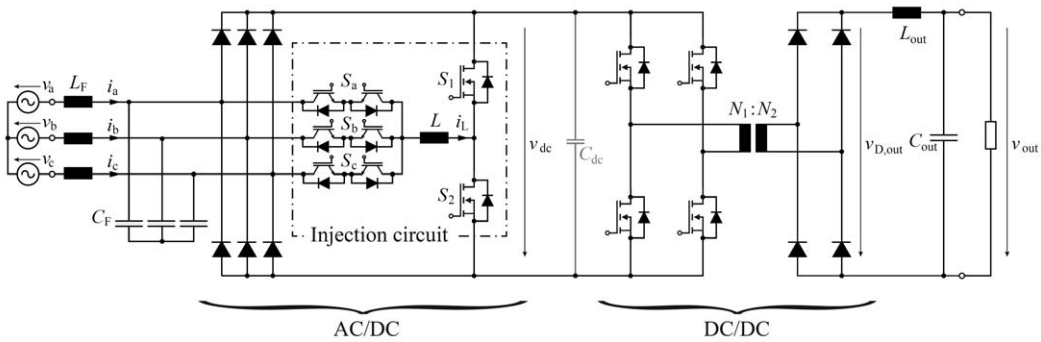


Figure 2.2: Proposed Isolated Integrated Active Filter Matrix-type (I^2AFM) PFC rectifier, Appendix C.

The design presented in Appendix C, is based on an interleaved dc-dc power stage, which can significantly improve the converter performance in mid-high load conditions.

The presented topology can also be adapted for bidirectional SOEC/SOFC systems. This solution can be applied to a system topology, as presented in Figure 2.1d, by replacing the inverter stage with a matrix-type PFC. Compared to the design case in Appendix C, it is necessary to redesign the transformers and replace the rectifiers diodes with suitable active switches (e.g. Si IGBTs and Si MOSFETs). In this scenario the I^2AFM topology could minimize the dc-link capacitance and provide very high system efficiency despite a higher number of power semiconductors and an increased complexity in the control system (minimized dc-link capacitance requires synchronization between the ac-dc and the dc-dc stages).

2.2.4 Dc-dc Converter Topologies

One of the major challenges of the electrical SOEC/SOFC system is the design of the dc-dc converter. The converter has to adapt the voltage and current levels of the SOEC/SOFC cells stack with the ones of the dc-ac converter. Based on the SOEC/SOFC cells stack characteristics, the preliminary specifications of the dc-dc converter are specified in Table 2.2. It is observed that the low voltage port (LV-side) of the dc-dc converter is expected to operate in the 30-80 V range with currents up to 80 A. In this case, the voltage variation at the port has a 2.67 factor, which significantly challenges the design of high efficiency dc-dc converters. Both dc-dc conversion efficiency and converter cost are important factors in the selection of the converter topology.

Resonant converters are well known for being capable of achieving high conversion efficiency due to their soft switching capabilities [33]. Resonant topologies are rather simple topologies however, they struggle to maintain high efficiency with large voltage variations at the converter ports [34]. This results in low conversion efficiencies outside their optimal operating conditions. After an analysis of the state of the art of dc-dc converter topologies, two main topologies are considered as the most suitable candidates for the dc-dc converter in the system in Figure 2.1c and 2.1d: the isolated full bridge boost converter (IFBBC) [35, 36] shown in Figure 2.3a and the dual active bridge (DAB) [37] shown in Figure 2.3b. These topologies were selected due to their proven efficiency performance [7, 38] and to the limited number of components (low complexity topologies).

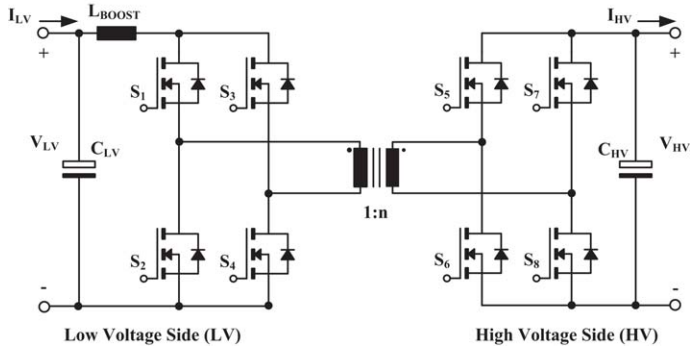
Table 2.2: SOEC/SOFC cells and converter specifications

Specification	SOEC	SOFC	Dc-dc converter
Voltage LV-side	50-80 V	30-50 V	30-80 V
Current LV-side	0-80 A	0-40 A	0-80 A
Power	0-6000 W	0-1500 W	0-6400 W
Power flow	$\Leftarrow$ from the grid	$\Rightarrow$ to the grid	$\Leftrightarrow$ bidirectional

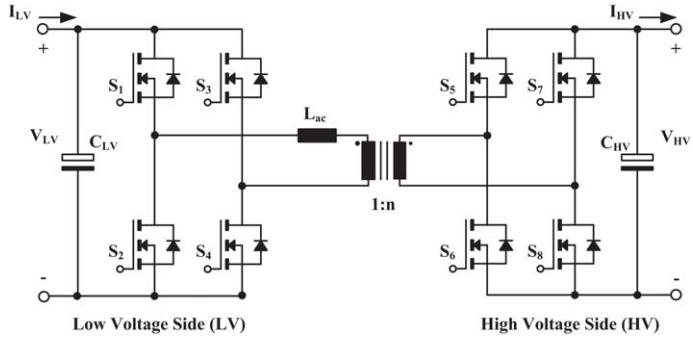
I order to select the most suitable topology for the application, a component stress factor (CSF) analysis is performed and presented in Appendix D. The analysis is performed according to [39] where the individual stresses are calculated based on the components current and voltage stresses. Results from the analysis highlight that the DAB topology is more suitable for narrow converter operating ranges. Far

from the optimal operating points and especially at light power loads, the DAB CSF values increase significantly, which result in challenging designs for high efficiency. On the other hand, the IFBBC topology has a more homogeneous distribution of CSF values highlighting that the topology could provide a more homogeneous efficiency distribution for the entire dc-dc converter operation range.

Based on this analysis and on previous experience accumulated, the IFBBC topology is selected for further analysis and design cases.



(a) IFBBC topology



(b) DAB topology

Figure 2.3: Analyzed dc-dc converter topologies.

2.3 SOEC/SOFC I-V Characteristics

SOEC/SOFC cell stacks have I-V characteristic that is dependent on the cells operating temperature, fuel composition and pressure. This leads that the I-V curve of a cell stack is not unique. It also requires that the dc-dc converter specifications are defined accordingly to the I-V stack characteristics, including a margin factor.

A complete model of the SOEC/SOFC stacks can become very complex [40, 41] and it has a minimum interest from electrical point of view. With the purpose of determining the simplified I-V stack characteristic, the SOEC/SOFC stacks are modeled as a voltage source or cells stack open circuit voltage (OCV) with a series impedance (Z_S), as shown in Figure 2.4. The dominant component in Z_S is the series resistance of the cell stack. In fact, cell geometry is typically rectangular (about 10 cm by 10 cm and 1~3 mm tick). The current flow is orthogonal to the cell plane, this leads that its stray inductance is negligible. The stray capacitive

component can also be neglected due to the series connection of the cells and due to the large thickness of the solid oxide between the cell electrodes. The cells' Joule losses (due to the series resistance R_S) are dependent on the operating conditions of the cells however, for modeling purposes R_S and OCV are supposed constant. From the equivalent circuit in Figure 2.4 it is observed that a change in the operating mode (from SOEC to SOFC and vice versa) is achieved by controlling the dc-voltage at the cells stack terminals with a suitable dc-dc converter.

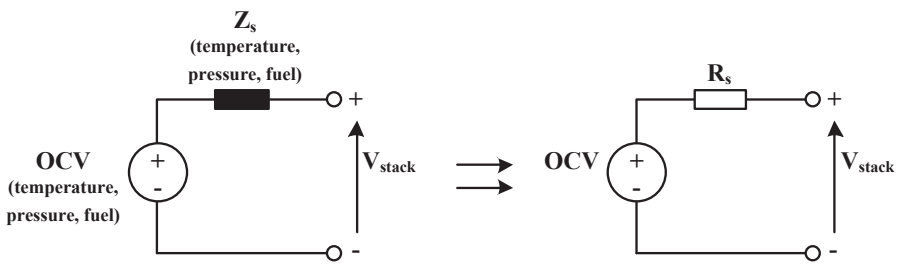


Figure 2.4: SOEC/SOFC equivalent electrical circuit model.

The dc-dc converter characteristics are determined by extrapolating and averaging the I-V curve of two SOEC/SOFC cell stack prototypes (10 and 20 cells). The two stack prototypes were tested at 60 A SOEC and at 20 A SOFC; their I-V characteristics is linearly scaled up to cover the entire stack operating range (up to 80 A in SOEC and up to 40 A in SOFC).

The extrapolated characteristics of the stacks at the maximum rated operating conditions (80 A for SOEC mode and 40 A for SOFC mode) are presented in Figure 2.5. In both operating modes, the converter specifications ensure a suitable margin over the stack characteristics.

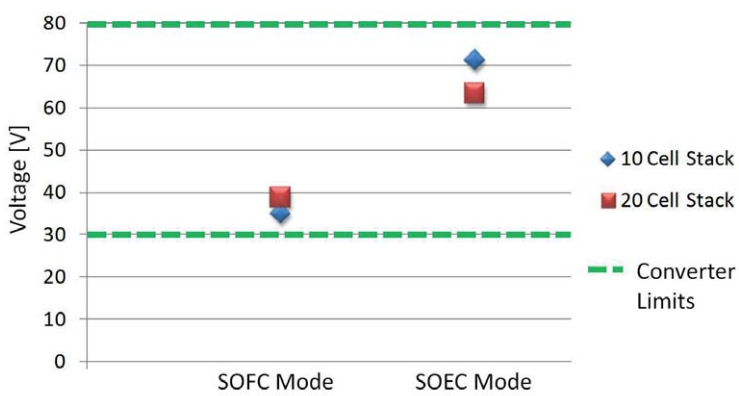
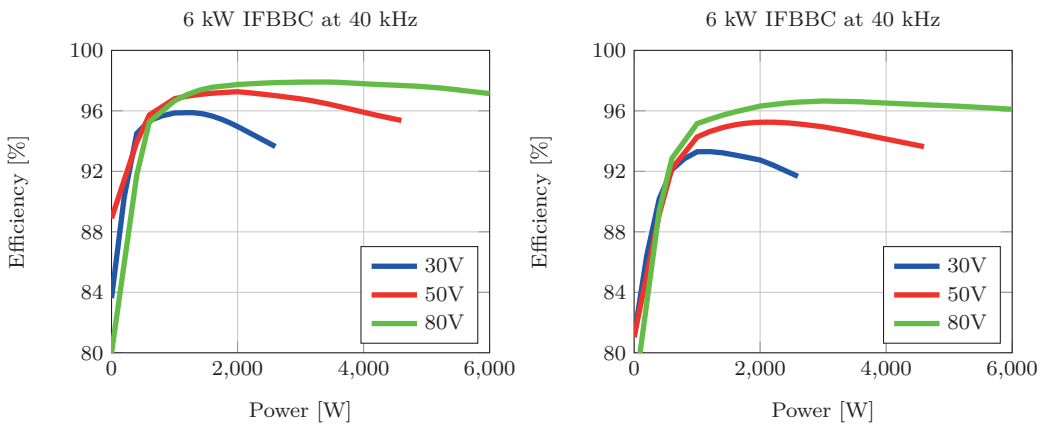


Figure 2.5: SOEC/SOFC prototype stacks I-V characteristics at 80 A in SOEC and at 40 A in SOFC (scaled characteristic).

The average I-V stack characteristics is used to determine the I-V operating points of the dc-dc converter low voltage side. Efficiency of dc-dc converters is typically characterized at different voltage levels [42], at different current levels and with

different power flow directions [43] (e.g. SOEC vs. SOFC), as shown in Figure 2.6a and 2.6b. The introduction of the I-V stack characteristics defines the dc-dc converter operating points. The resulting dc-dc efficiency is presented in Figure 2.7. It is observed that when the dc-dc converter is operated in the SOEC/SOFC system the maximum theoretical dc-dc converter is never achieved.

The dc-dc converter efficiency that takes into account the I-V characteristic of the SOEC/SOFC cell stacks is presented in Appendix E.



(a) Fuel cell mode (SOFC). **(b)** Electrolyzer cell mode (SOEC).

Figure 2.6: 6 kW dc-dc converter efficiency, conventional efficiency characterization.

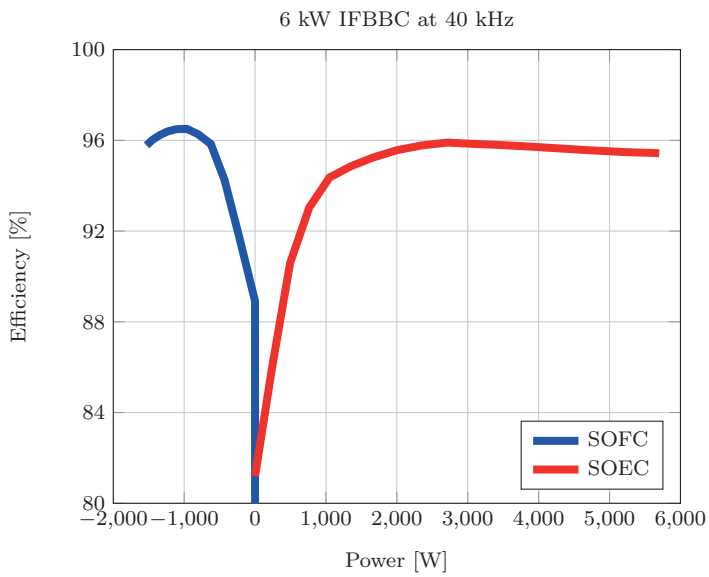


Figure 2.7: 6 kW dc-dc converter efficiency based on SOEC/SOFC I-V curve and Si IGBTs.

Chapter 3

Wide Bandgap Power Semiconductors

This chapter presents an overview of the state of the art wide bandgap power semiconductors and of the results achieved with these devices.

3.1 Evolution of Power Semiconductors

Power semiconductors were firstly introduced in 1952 with the introduction of the power diode and subsequently other devices such as semi-controlled rectifiers (SCRs) or thyristors [44] and other power devices such as BJTs, MOSFETs [45] and IGBTs [46].

Nowadays, power semiconductors are a key component in every switch mode power supply (SMPS). More efficient energy conversion has been the major focus over the last decade supported by the large scale integration of renewable energies. Silicon (Si) power semiconductors represent almost the entire power semiconductor market [47] however, new wide bandgap (WBG) power semiconductors materials are rapidly growing interest due to their pledge of outstanding performance [48]. The global interest in WBG power devices is driven by the potential advantages over traditional Si power semiconductors [49].

These advantages can be summarized in:

- Higher operating frequencies
- Higher efficiency
- Higher voltage ratings
- Higher operating temperatures
- Smaller passive components
- Smaller cooling system
- Lower amount of raw materials
- Lower cost due to smaller passive components and reduced requirements for the cooling system

Silicon carbide (SiC) and gallium nitride (GaN) are the two main WBG semiconductors candidates to replace Si in power applications. Their physical potential is huge in comparison to the Si limits, as shown in Figure 3.1 [50].

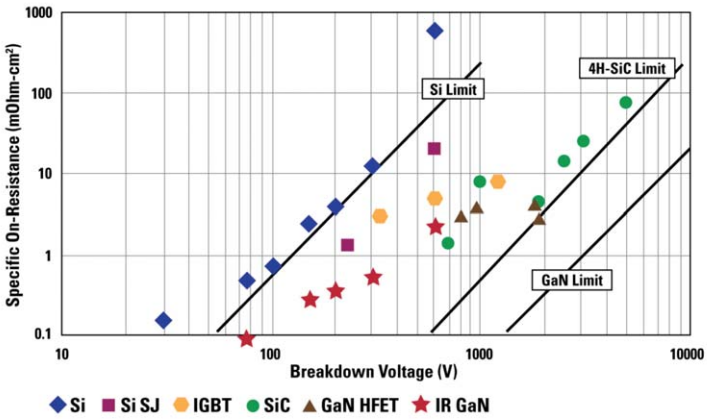


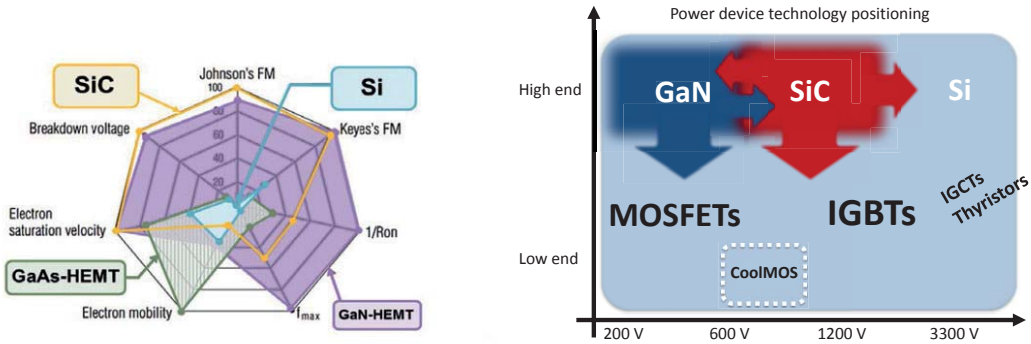
Figure 3.1: Si, SiC and GaN material physical limits for unipolar devices in comparison with the state of the art devices.

The materials physical characteristics are key components to determine the power semiconductor switching, conduction, blocking and thermal characteristics. A general overview of the main properties of Si, SiC and GaN is presented in Figure 3.2a [51]. Diamond is often used as reference as ideal semiconductor material however, material cost and processing represent the main challenges for this semiconductor.

Research in SiC started back in 1927, yet only recently SiC power devices reached the market. Although SiC has different crystalline structures, all commercial SiC power devices are based on 4H-SiC [52]. Material cost is down to ~10 $\$/cm^2$ [53] for 4 inches wafers [54] and more recently 6 inches wafers became available [55]. The wide bandgap energy and high electric field of SiC allows high temperature and high blocking voltage devices with lower on-state resistance $m\Omega \cdot cm^2$ compared to Si.

GaN technology has been widely used since 1990s for bright light-emitting diodes (LEDs) [56]. Only recently GaN became attractive for conventional power electronics [57] due to the lower cost of the substrate (GaN deposited on Si lowers the price down to <1 $\$/cm^2$ [53]). The major advantages of GaN are its high electric critical field and its high electron mobility compared to SiC [58]. However, the major challenges for GaN are related to the large thermal mismatch with the substrate when GaN is deposited on Si or sapphire and the lower thermal conductivity compared to SiC.

On overall, SiC and GaN have similar material properties and are in a tight competition. At present SiC technology seems more mature as there are already commercial products based on SiC power devices. However, GaN market growth rate over the last three years has been ~250%/yr while for SiC this was ~35%/yr [59]. There is no clear winner between the two technologies. A short term forecast indicates that GaN will replace Si for low voltage devices (<600 V) while SiC will mostly replace the market nowadays taken by the Si IGBTs (>600 V), as seen from Figure 3.2b [60].



(a) Material properties. **(b)** Device technology positioning.

Figure 3.2: Si, SiC and GaN power semiconductors materials and devices.

3.2 SiC Power Semiconductors

This section presents an overview of the most diffused power devices that have been developed in SiC.

3.2.1 SiC Schottky Diodes

SiC Schottky diodes [61] were the first commercial power devices in SiC. SiC diodes have comparable forward voltage drop as Si diodes, however they have extremely low reverse recovery charge Q_{rr} [62]. This results in higher converter efficiencies and reduced EMC/EMI issues caused by the high di/dt. SiC Schottky diodes are commercially available for voltages in the 600~1700 V range.

3.2.2 SiC JFETs

SiC junction field effect transistors (JFETs) are developed based on two structures: lateral channel layout (LCJFET) and vertical trench channel (VJFET) [63]. The SiC LCJFET are normally-on (SiCED-Infineon structure) [63] while SiC VJFET are available both as normally-on or normally-off (Semisouth Laboratories structure). The VJFET can provide very low $m\Omega \cdot cm^2$ [64] however, the device structure does not include a body diode. SiC JFETs are available with very limited availability (mostly engineering samples) from few companies such as Infineon and GeneSiC.

3.2.2.1 Normally-ON

Normally-on SiC JFETs [65] are available with on-state resistance of 45~85 $m\Omega$ rated at 1200 V 150 °C in TO-247. The pinch–off voltage of these devices is typically in the -6~$-26\,V$; in off-state their gate leakage current (100~800 µA) is usually negligible and a small positive voltage (2 V) is often used to furthermore reduce the channel on-state resistance. The gate driver is required to provide a high current pulse to further reduce the device switching losses [66].

3.2.2.2 Cascode Structure

The cascode structure was introduced [67] to overcome the normally-on behavior of SiC JFETs. The structure is normally-off and it is build on series connection of a normally-on SiC JFET with a Si MOSFET. The structure proved to be scalable also to high voltages [68] while maintaining control over its dV/dt [69].

3.2.2.3 Normally-OFF

Normally-off SiC JFETs [70] are available with on-state resistance of 65~100 $m\Omega$ rated at 1200 V 150 °C in TO-247 package. The devices have typically a low threshold voltage 1~2 V and their leakage gate current during on-state is not negligible (10~200 mA). When reversely biased the gate leakage current is negligible (as for normally-on JFETs). A pulsed gate driver [66] or an ac-coupled gate driver [71] is required to reduce the device switching losses and achieve the best performances from the devices.

3.2.3 SiC MOSFETs

SiC MOSFETs development started back in the 1980's [72], however only recently the devices became available. Current commercial devices are based on the UMOSFET structure [73]. Devices are available with voltage rating of 650~1700 V and on-state resistance down to 25 $m\Omega$ in TO-247 package [74]. SiC MOSFETs are normally-off with typical gate threshold voltages are in the 1.5~3.5 V range. On-state voltages up to 15~20 V are required to achieve low on-state resistance while off-state reverse biased voltages are limited to −5~−10 V.

3.2.4 SiC BJTs

SiC BJTs [75] are available with voltage ratings of 900~1700 V, currents up to 50 A and they are based on the NPN junction structure. Typical current gains are in the 40~80 β range, they provide the lowest $m\Omega \cdot cm^2$ and temperature dependence [76]. The devices require a continuous gate current; for very large devices and at high currents it can be up to 1.2 A. Nowadays, availability of SiC BJTs is very limited moreover, there are still concerns on long term reliability of the devices due to the risk of bipolar degradation [77].

3.3 SiC Device Comparison

Selecting the most suitable power devices for a specific applications is a non-trivial issue. This requires the analysis of the device performance, reliability, cost and availability. When considering SiC power semiconductors, there is a limited availability of devices that reached the market. During the first half of 2012, an analysis was performed on commercially available SiC power semiconductors. The investigation focused on power devices for multi-kW power converters with a device voltage rating of 1200 V and a current rating in the 15~40 A range. These device ratings are

determined by the converter specifications in Table 2.2 and by the system topologies presented in Figure 2.1. The investigation concluded that for the device voltage rating of 1200 V there is a limited number of SiC devices that are commercially available; these are limited to SiC MOSFETs, normally-on and normally-off SiC JFETs. In Si material, the considered power ratings are entirely covered by Si IGBTs. Other Si devices are not suitable, e.g. Si MOSFETs structures (including CoolMOS) are limited to voltages below 900 V and thyristor-type devices are more suitable for very high power applications in the kA-range. However, the major advantage of Si IGBTs is their wide availability from different manufacturers and different optimized structures.

A summary of the experiments and results achieved is presented both in Appendix F and Appendix G. The analysis and comparison of the power semiconductors is performed on the following devices:

- Si IGBTs (no.1 IGW15N120H3, no.2 IRG7PH30K10)
- Cascode structure (SJDP120R085+IPB017N06N3)
- SiC normally-on JFETs (SJDP120R085)
- SiC normally-off JFETs (SJEP120R100)
- SiC MOSFETs (CMF20120D)

Even though, Si IGBTs cannot be directly compared to SiC power devices, it is necessary to consider the state of the art of Si devices as technology reference. Moreover, the analysis and comparison presented in Appendix F and Appendix G can provide a quantitative analysis of the expected loss reduction that is achievable with SiC power semiconductors. In order to perform a proper comparison it is necessary that each power semiconductor is driven with a suitable gate driver, as presented in Appendix G.

Si IGBTs were selected among two manufacturers (Infineon and IR), focusing on devices which are optimized for fast switching (high frequency applications up to 100 kHz). These devices represent the latest generations of trench IGBTs.

The Cascode structure was analyzed in Appendix F. The structure is interesting since it can represent a bridge between Si and SiC technology. The major advantage of the structure is its normally-off behavior and the possibility of using a simple Si IGBT/MOSFET gate driver.

Normally-on SiC JFETs have the unwanted normally-on behavior, however they can be efficiently driven like a traditional Si MOSFET/IGBT with reversed driving voltages. This was considered a good compromise between device performance, gate driver complexity and cost. Normally-off JFETs represent a more interesting solution in multi-kW converters simply due to their normally-off behavior, which guarantees that a control power outage does not cause the destruction of the power converter. Normally-off SiC JFETs would significantly under-perform if driven with a simply gate driver. These devices require a high current at device turn-on, therefore a pulsed gate driver structure was used [66].

SiC MOSFETs represented the most recent evolution in Si power devices. The tested device, CMF20120D, is the first generation of commercially available devices.

Devices effectively perform with a simple gate driver with shifted voltage levels (e.g. from −4 V to 20 V).

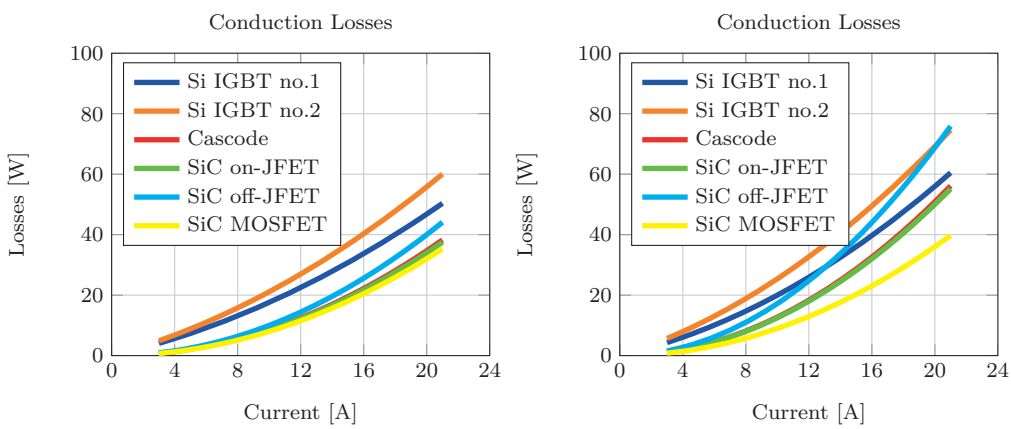
In hard switched converter topologies, the characterization of power semiconductors is mostly focused on:

- Conduction losses
- Switching losses

3.3.1 Conduction Losses

Conduction losses, or static characteristic, of the device can be easily characterized with a good accuracy based on datasheet values. Power semiconductors manufacturers often provide device temperature dependency and analytical equations that can be used to extract the I-V or I-P static forward characteristic. I-V curve tracers are also commonly use to characterize the conduction losses. A major advantage of I-V curve tracers is that they can characterized the device by using short pulses without affecting the device junction temperature.

The analysis of the conduction losses is based on calculations starting from datasheet values. This is presented in Figure 3.3a at 25 °C and in Figure 3.3b at 100 °C. It is observed that, especially at low current levels, all SiC devices provide a significant reduction of the condition losses. As the device current increases, the advantage of the SiC devices is reduced. In fact, the forward voltage drop of IGBTs dominate at low current levels. As the current increases, the gap between Si IGBTs and SiC devices is reduced due to the lower on-state resistance of the considered Si IGBTs. As the device junction temperature increases, device losses increase. In Si IGBTs the increase of on-state resistance is partially compensated by the reduction of the forward voltage drop resulting in limited increase of device losses. In SiC JFETs there is a large increase of on-state resistance for both normally-on and normally-off devices. In both devices, the increase in the channel resistance is in the 40%~50% range. The first generation of SiC MOSFETs have a more limited increase in on-



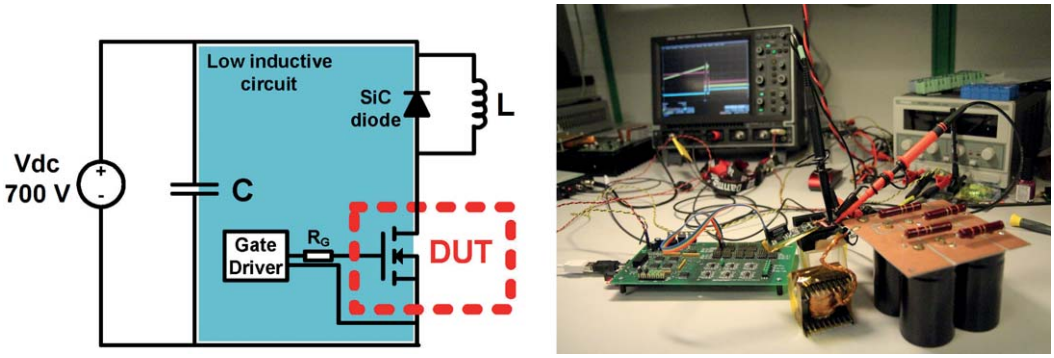
(a) Temperature 25 °C. **(b)** Temperature 100 °C.

Figure 3.3: Si and SiC conduction losses.

state resistance (~20%) compared to SiC JFETs. The second generation of SiC MOSFETs, introduced in early 2013 [78], has a lower increase of on-state resistance compared to the first generation due to the improved device structure.

3.3.2 Switching Losses

Power semiconductors switching losses are more difficult to characterize, since they strongly depend on the device parasitics, on the gate driver, on the circuit topology and circuit parasitics [79]. Circuit parameters are very challenging to model as they depends on components package and circuit layout. For these reasons, the most common approach is to perform switching loss measurements with an inductive clamped circuit [80] or double pulse tester (DPT). The circuit in Figure 3.4a applies two short pulses of variable width (typically in the 1~100 µs range). The pulses rise the inductor current to the desired level, then the power semiconductor switching losses are measured through a voltage and current probe on the device. With this methodology it is possible to characterize independently device turn-on and turn-off losses. Since test pulses are of short duration and represent a single event, the device's junction temperature increase due to the energy dissipated during the pulses can be neglected. This allows performing switching loss measurements at constant junction temperatures, where the junction temperature is set with an external controlled heat source. The waveforms acquired with the setup in Figure 3.4b are then post-processed to extract the device switching losses. The switching losses are computed by integrating the instantaneous power loss around its peak with a threshold of 3%, as presented in Appendix G.



(a) DPT circuit **(b)** DPT laboratory setup.

Figure 3.4: Double pulse tester (DPT).

It is fundamental that, for obtaining a trustworthy comparison of different devices, the test circuit layout and components remains the same. The power semiconductors part of the analysis have been characterized with a DPT. Measurements were performed at 700 V with currents up to 21 A. Linear scaling-interpolation of the energy loss measurements can be used to calculate converter switching losses for different voltages and currents levels [81].

The analysis aimed to investigate the efficiency improvement achievable with SiC power semiconductor due to the reduction of switching losses over traditional Si IGBTs. In order to consider the best trade-off, different devices were characterized

with different gate drivers, as presented in Appendix G. Si IGBTs and the Cascode configuration were driven with a single ended supply 0-15 V; on-JFET were driven with a negative single ended supply −15-0 V; off-JFET were driven with −15-3 V with a high current pulse at device turn-on and SiC MOSFETs were driven with −4-20 V. All Si and SiC power devices are in TO-247 package, expect for the low voltage Si MOSFET used in the Cascode configuration (TO-263-7 package). A comparison of the power semiconductor switching losses is presented in Figure 3.5a for the devices turn-on and in Figure 3.5b for the devices turn-off.

The Cascode structure has large turn-on losses compared to fully SiC switches. In this structure, the JFET's turn-on is delayed compared to the Si MOSFET's turn-on and the SiC JFET is switched-on without a high current pulse, this leads to high device turn-on losses. The lowest turn-on switching losses are achieved with normally-off SiC JFETs driven with an optimal gate driver or with SiC MOSFETs Figure 3.5a. IGBTs of the latest trench generation, optimized for fast switching (high switching frequencies >30 kHz), have smaller tail currents compared to soft IGBTs. IGBTs are still the devices with the largest turn-off losses due to their tail current Figure 3.5b. As expected, all SiC configurations achieve lower turn-off switching losses than then state of the art Si IGBTs. It is observed that the Cascode structure has extremely low turn-off losses, in fact the JFET's turn-off controlled by the low on-state resistance of the Si MOSFET ($m\Omega$ range). This acts as an extremely low gate resistance and achieving the lowest possible turn-off losses from the structure.

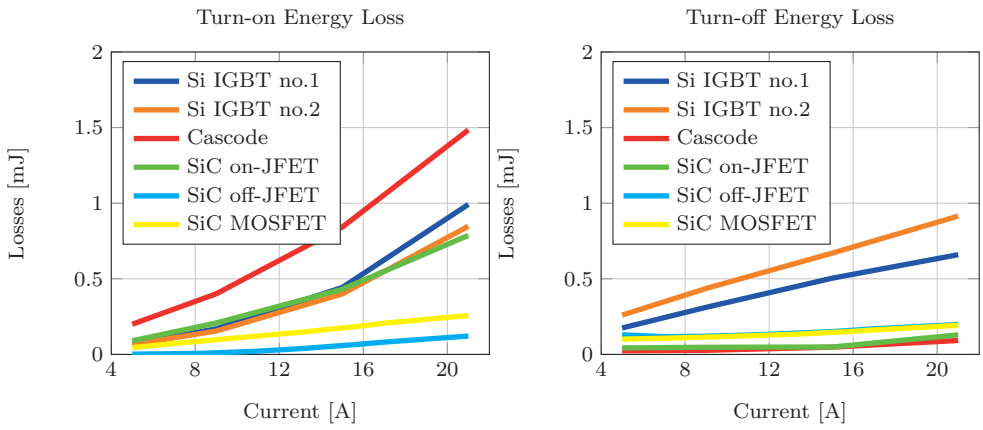
The overall device switching losses are presented in Figure 3.6. In general, IGBTs still represent the best trade-off between the power semiconductor performance and cost (without taking into account the other converter components). This is especially true when IGBTs are driven at their limit of the switching performance.

SiC devices can achieve remarkably low switching losses when suitable gate drivers are used. In the case of SiC JFETs, it is necessary to use a high current pulse at device turn-on through a pulsed gate driver or and RCD gate network [66, 82]. The major drawback of SiC JFETs is their high dependency of the on-state resistance on the junction temperature and, for normally-off JFETs, the current required to maintain the devices in low ohmic on-state. SiC MOSFETs achieve very low switching losses without the need of a high current pulse at device turn-on. Moreover, these devices have the lowest increase of on-state resistance as a function of the temperature.

A major concern, which has to be considered when choosing power semiconductors, is the device availability from different manufacturers. Currently, SiC JFETs, both normally-on and normally-off from Semisouth Laboratories, have been discontinued. Other companies (GeneSiC) started to commercialize SiC JFETs, however their availability is very limited and these devices are often more expensive than their SiC MOSFET competitors. Most of the large competitors in the power semiconductor market are focusing on SiC MOSFETs. SiC MOSFETs require a more simple gate driver structure compared to SiC JFETs, moreover SiC MOSFETs have a negligible gate leakage current. For all these reasons, SiC MOSFETs are the preferred choice for new converter designs.

An analysis and comparison of the switching performance of different Si and SiC

devices has been performed and are presented in Appendix F and in Appendix G.



(a) Turn-on. **(b)** Turn-off.

Figure 3.5: Si and SiC switching losses. Separate components.

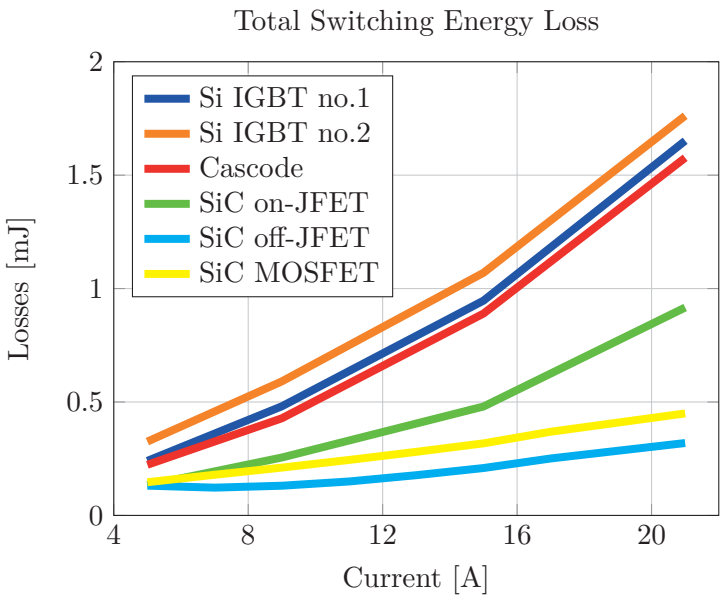


Figure 3.6: Si and SiC total switching losses.

Chapter 4

Magnetics Design

4.1 Planar Magnetics Overview

Magnetic components are fundamental part of switch mode power supplies and, for this reason, they are a major research interest [83]. For simple winding structures traditional wire wounded components are suitable for high volume production, however as the winding structure complexity increases, they require more production steps, which significantly increases the manufacturing cost.

Over the last years developments in commercial electronics and in its manufacturing techniques have led to large cost reductions in printed circuit boards (PCBs) technology. PCBs represent the elementary support unit for creating the interconnections between all electronic components. PCBs are also an attractive technology for windings of magnetic components [84, 85]. In these specific cases, it is possible to integrate the magnetic component together with the other circuit components in a manufacturing friendly layout [86].

The integration of PCB windings is often combined with low profile magnetic components, which have a better aspect ratio for this purpose. Low profile magnetics are often referred as planar magnetics [87] and can be used with PCB windings or other winding technologies such as foil windings and traditional winding techniques. Planar transformers are available up to 20 kW [88], where the use of foil windings can ensure also high power density. Planar magnetics technology has been widely discussed and researched for many applications [87, 89]. The technology has been particularly successful in low power (<1 kW) and high power density applications, where integration of magnetic components with power and control devices is the key factor [86]. Typical example of this success are bus converters, where integration allowed reaching power densities up to 167 W/cm^3 (VI Chip® BCM®, 2750 W/in^3 [90]).

4.1.1 Advantages and Disadvantages

Designing magnetic components for power converter based on planar magnetics can provide significant advantages over traditional magnetics designs. In order to take full benefit from this technology, it is necessary to consider both advantages and drawbacks [91].

The major advantages provided by planar technology can be summarized in:

- Good thermal performance allows to easily cool the transformer core
- High power density
- High fill factor with foil windings or flexible PCB
- Easy interleaving with PCB windings
- Suitable for low leakage structures
- High repeatability with PCB technology
- Cost reduction with low cost PCB windings, suitable for mass production
- High integration, magnetic components can be integrated on the same boards as the other power components.

The major drawbacks of planar technology are:

- Low filling factor with PCB windings
- Large stray capacitances with PCB/foil windings
- Challenging design of high current magnetics
- Difficult to achieve large number of turns
- High prototyping cost of multilayer and thick copper PCBs.

4.2 Losses in Magnetic Components

The design of highly efficient magnetic components requires accurate loss models for both core and winding losses. The most common approach is based on the minimization of the total magnetic component losses in Eq. 4.1 [92, 93]. This point is in proximity of the even distribution of the losses between the core and the windings. This type of optimization is mostly performed as a closed loop optimization [94] based on a fixed converter operating point. For power converters with large operating ranges, magnetics optimization becomes particularly challenging and it requires the use of weight factors to take into account different operating points.

$$P_{loss} = P_{core} + P_{windings} \tag{4.1}$$

The main methodologies to analytically evaluate the winding and core losses in magnetic components are briefly summarized in the following part.

4.2.1 Winding Losses

Winding losses can be classified in three main components: dc losses, ac losses and fringing flux losses [95]. Dc winding losses can easily be calculated based on the winding geometry and winding current. The analysis of ac winding losses is more complex. The most common method is represented by Dowell's approach [96], which is a 1D solution based on the assumption that current and voltages are sinusoidal, that the winding area is completely filled, that the windings are infinitely long with negligible curvature and that the leakage flux is parallel to the conductors surface. This method takes into account eddy current losses, skin and proximity effects, and it allows expressing the winding resistance as in Eq. 4.2 where the R_{ac}/R_{dc} ratio is calculated as in Eq. 4.3. $\xi = h/\delta$ where h is the layer height along the 1D section, δ is the skin depth and m (Eq. 4.4) is a coefficient that takes into account the magneto motive force (MMF) of each layer. Ac fringing losses are due to the fringing flux in proximity of gaps along the magnetic core. Dowell's 1D approach is not valid anymore and it is required to analyze the structure in a 2D solution, considering both x-y flux components of the 2D plane, as presented in [97] and [98]. In designs where the gap dimension is small compared to the core cross sectional area and where the windings are distant from the gap, it is possible to neglect the fringing flus loss component. Another possibility to minimize fringing flux losses is to design magnetic components based on magnetic materials which does not require a gap (e.g. distributed gap materials such as Kool Mu) [99].

$$R_{ac} = \sum_{layers} \left(\frac{R_{ac}}{R_{dc}}\right)_{layer} \cdot R_{dc,layer} \tag{4.2}$$

$$\left(\frac{R_{ac}}{R_{dc}}\right)_{layer} = \frac{\xi}{2}\left[\frac{\sinh(\xi)+\sin(\xi)}{\cosh(\xi)-\sin(\xi)} + (2m-1)^2\,\frac{\sinh(\xi)-\sin(\xi)}{\cosh(\xi)+\sin(\xi)}\right] \tag{4.3}$$

$$m = \frac{MMF(h)}{MMF(h) - MMF(0)} \tag{4.4}$$

4.2.2 Core Losses

Based on a loss separation [100, 101] approach core losses can be classified as hysteresis, eddy current losses and excess of eddy current losses [102] in the core material. In ferrite-based core materials, due to the high core resistivity, the eddy current and the excess of eddy current losses can be neglected, thus the core losses are simply hysteresis losses. The most common method to analyze hysteresis losses is based on the generalized Steinmetz equation [103] and its further developments. These approaches are summarized in:

- Generalized Steinmetz equation (GSE) [103]
- Improved generalized Steinmetz equation (IGSE) [104]
- Improved^2 generalized Steinmetz equation (I^{2}GSE) [105].

The most used approach is the GSE [103], based on empirical coefficients (K, α and β) provided by the core manufacturers, as in Eq. 4.5. The computations through the GSE are straight forward and only depend on the peak flux density B_{max} and the operating frequency f, however the equation is only valid for sinusoidal excitation. The IGSE [104] applies a piece wise linear model for calculating the hysteresis losses for any form of excitation, using the same empirical coefficients as the GSE. The I^2GSE [105] improves the IGSE model by taking into account that the core losses are not necessarily zero when zero voltage is applied (constant flux). However, this approach requires additional empirical parameters which are not provided by the manufacturers and require additional measurements.

$$P_{core/vol.} = K \cdot f^{\alpha} \cdot B_{max}^{\beta} \tag{4.5}$$

4.3 Stray Parameters

Winding structures strongly influence the stray parameters in magnetic components. In a transformer, heavy interleaving results in low leakage inductance, reduced winding ac resistance, but increased interwinding capacitance [106]. Therefore, it is necessary to consider the major stray parameters.

4.3.1 Leakage inductance

The leakage inductance is due to flux linkage in air which causes non ideal coupling between the transformer windings. In some topologies like the DAB, leakage inductance could be desirable, e.g. for integrating the ac inductance with the transformer [107, 108]. However, in other topologies, such as the IFBBC, the leakage inductance causes voltage spikes and oscillations, increasing the converter losses and increasing the current commutation time [7]. Leakage inductance can be calculated as in [109] or extracted from finite element analysis (FEA) simulations. It is commonly believed that planar structures are intrinsically low leakage. However, low leakage in this structures is achieved from the advantageous aspect ratio of the windings (winding thickness and width) and from heavy interleaving.

4.3.2 Stray Capacitance

Magnetic component windings act as electrode in a capacitor, electrostatic energy can be stored in insulation layer between the winding turns. There are mostly two types of stray capacitance in magnetic components: interwinding capacitance and winding stray capacitance. Interwinding capacitance, e.g. primary-secondary stray capacitance, is a major source of EMI issues (common mode) [110] and thus requiring large EMI filters or suppression techniques [111]. Interleaving structures have large interwinding capacitance due to the large number of interface layers (insulation layers) between primary and secondary windings. The winding stray capacitance is the winding self-capacitance, which causes oscillations and resonances in the circuit. Heavy interleaving typically reduces this capacitance due to the increased distance between turns of the same winding. In resonant topologies winding

self-capacitance can be used as a resonant element [112]. Planar transformers, due to the flat winding aspect ratio, have large stray capacitances which means that they are prone to produce oscillations in the circuit and to require large EMI filters.

4.4 Design of High Efficiency Planar Magnetics

In order to achieve high efficiency magnetic designs it is necessary to analyze different solutions in terms of core shapes, core materials, winding typologies and structures. One of the most common approaches for determining suitable transformer core dimensions is based on the core shape and material, operating frequency and applied waveforms. This approach often refers to the core area product and provides a rough indication of the power handling capability of a specific core [92]. Based on the dc-dc converter specifications in Table 2.2 and for the required target efficiency, it was determined that stacked planar E58, E64 and E99 [113] are the most suitable. Most of the studies are performed on the E64 core shape due to the good aspect ratio of the core winding window.

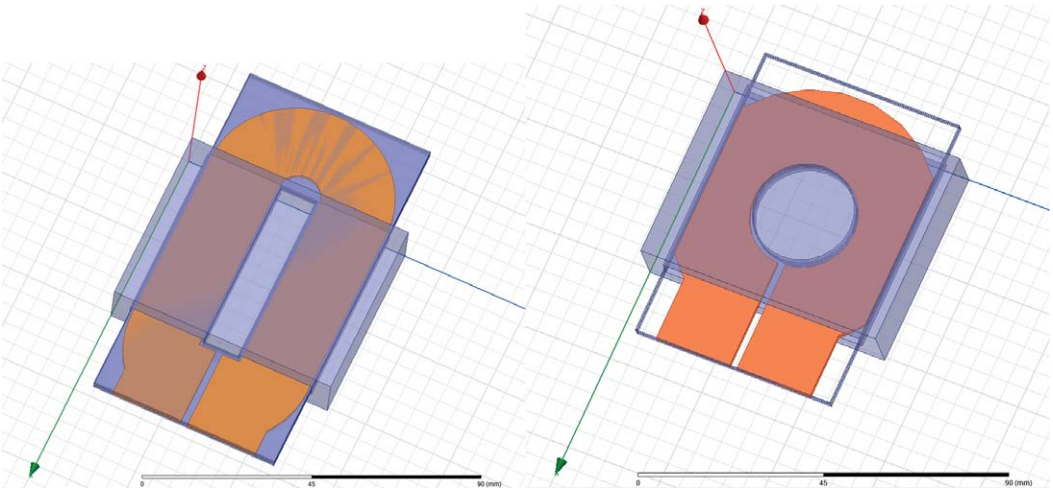
A key factor for achieving high transformer efficiency and high power density is represented by the winding area W_A fill factor K_W. Low fill factors will result in non optimized magnetic components due to the larger magnetic core required for the desired number of turns $N_{1,2}$. When designing high efficiency magnetic components it is essential to achieve high fill factors in order to reduce the winding losses, Eq. 4.6 [92]. This strategy has been applied to the design of both high frequency transformer and high frequency inductor for dc-dc converters.

$$P_{winding} \propto \frac{1}{K_w} \cdot f(\rho, MLT, N_{1,2}, I_{1,2}, W_A) \tag{4.6}$$

In Appendix H an analysis of two equivalent planar core shapes is performed. The analysis focuses on determining whether for high current applications the reduced core mean turn length (MTL) in the ER64 cores [114] can provide a significant advantage over the E64 cores. It is verified that the core with round cross sectional window (ER64) provides higher ac-resistance compared to the equivalent E64. This is due to the non-constant winding width of the ER64 core (limited winding width in proximity of the core center). The ER64 core would be more suitable in for transformer designs where the turn width does not occupy the entire winding area width (e.g. high number of turns and low current windings).

Using windings that occupy the entire winding area width in planar transformer cores can provide high fill factor, especially with multiple stacked layers. This type of windings becomes especially suitable for low voltage and high current applications, where the transformer windings have a low number of turns. However, in transformer structures which require both low voltage and high voltage windings (high turns ratio) large number of turns can be difficult to achieve.

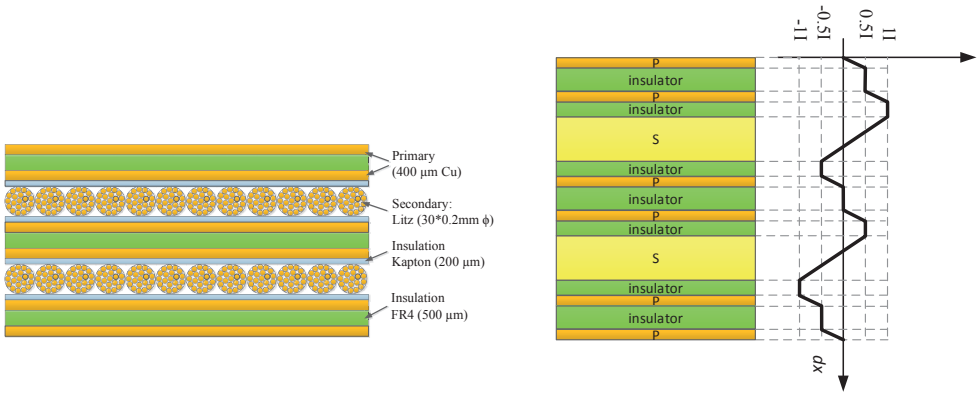
A hybrid transformer structure, combining thick copper foil and Litz wires, is presented in Appendix I. The hybrid structure, presented in Figure 4.2a, combines the high filling factor achieved with copper foils with the high number of turns of Litz wires. In Appendix I different transformer winding structures are analyzed. The



(a) Planar E64 **(b)** Planar ER64

Figure 4.1: Analyzed Planar E64 and ER64 core shapes in Ansoft Maxwell.

goal is to determine the trade-offs between PCB windings interleaved structures and thick copper foil windings. It is observed that extreme copper foil thickness is not advantageous due to the skin effect at high frequencies, which leads to a poor copper utilization and waste of expensive material. Thick copper PCBs (e.g. 6 oz copper thickness) can also provide high fill factor however, this requires a large number of PCB layers to completely fill the core winding area. It is also observed that with switching frequencies typical of multi-kW converters (e.g. up to 150 kHz), thick copper foils (400-1500 μm) and PCB windings provide the best performance especially with interleaved structures, as shown in Figure 4.2b, and with switching frequencies that are not critically high.



(a) Transformer structure **(b)** Transformer MMF

Figure 4.2: Hybrid transformer structure for high efficiency dc-dc converters.

The transformer presented in Appendix I is designed for an IFBBC for bidirectional SOEC/SOFC as specified in Table 2.2. Copper foil is ideal for the low voltage

high current winding, as shown in in Figure 4.3a, in fact, copper foil is mostly suitable for low number of turns (3 primary turns). The large number of secondary turns (24), required on the transformer high voltage, would significantly complicate the transformer winding structure. For this reason, copper foil is not suitable for the secondary winding. Other winding techniques, such as PCB windings or more traditional wire-winding techniques, are required. Proper selection of Litz wire could ensure high fill factor, high number of turns and good high frequency performance, therefore Litz wires became the candidate solution, as shown in Figure 4.3b.

The transformer primary (P) secondary (S) interleaved structure, PSPSP, has a significant impact over the transformer performance. The interleaved structure reduces the maximum transformer magneto motive force (MMF in Figure 4.2b), resulting in lower transformer leakage inductance and ac-resistance compared to non interleaved cases. Minimizing the transformer leakage inductance is of vital importance in the IFBBC topology in order to minimize the current loops commutation times, and therefore the losses in the converter.

(a) Transformer high current side (copper foil). **(b)** Transformer high voltage side (Litz wires).

Figure 4.3: High frequency high current transformer prototype.

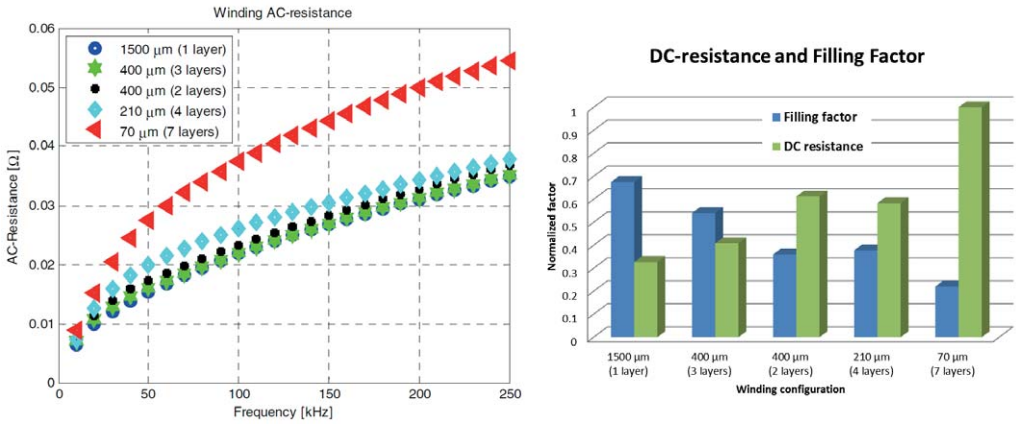
The design of high current planar inductors requires a similar analysis as performed for planar transformer. The winding structures analyzed in the transformer cases can be similarly applied to planar inductors, however in this case, the approach requires a different perspective; now it is necessary to minimize the conduction losses taking into account both their ac and dc components. Core losses can be analyzed as performed for transformers based on the three methods presented in [101, 100].

It is possible to perform a distinction between two major inductor structures: gapped and ungapped. In terms of winding losses, the major difference between gapped and ungapped inductors lies in how the winding losses are calculated. In gapped inductors the winding losses are calculated based on skin effect, proximity losses and fringing flux losses. In ungapped inductors, the fringing flux is considered negligible, this results in a reduction of the total winding losses. Advanced magnetic materials, such as distributed gap materials, have been developed in order to avoid fringing flux losses, an therefore provide constant permeability over the entire magnetic path. Distribute gap materials, are available with different satu-

ration flux under different names (such as Kool Mu and AmoFlux materials from Magnetics [113]). The major advantage given by powder based materials is that cores can be customized to a variety of shapes. Kool Mu cores are also available in planar shape, which makes these cores suitable for high current inductors with no fringing effects.

The study presented in Appendix J analyses five different winding structures for a high current planar inductor based on Kool Mu material. The design case is a boost inductor for an IFBBC for bidirectional SOEC/SOFC as specified in Table 2.2. The major goal of the study is to investigate how dc and ac resistances varies, depending on the copper thickness and on the number of PCB layers. These parameters directly affect the fill factor and the conduction losses.

Results from the analysis of the ac resistance of the five different cases are presented in Figure 4.4a. Here it is observed that in the analyzed frequency range the winding ac resistance is lower for in the thick copper cases; this results that having multiple thin copper layer in parallel is not beneficial in terms of ac resistance. The relation between the winding dc resistance and the fill factor in the different cases is presented in Figure 4.4b, where the dc resistance has been normalize to an unitary value (3.03 mΩ).



(a) Ac-resistance **(b)** Dc-resistance and fill factor

Figure 4.4: High current inductor analyzed cases.

The prototype of a custom planar inductor is also presented in Appendix J. The prototype is based on three planar E6030 core pairs in Kool Mu material. The E6030 core pairs were obtained as engineering samples from Magnetics and are manufactured from grinded from 6030 cores core blocks. The core stack is composed by two cores, with a relative permeability of 90 and one core, with a relative permeability of 26. This allows an intermediate permeability level reducing also the inductance drop at high dc bias currents.

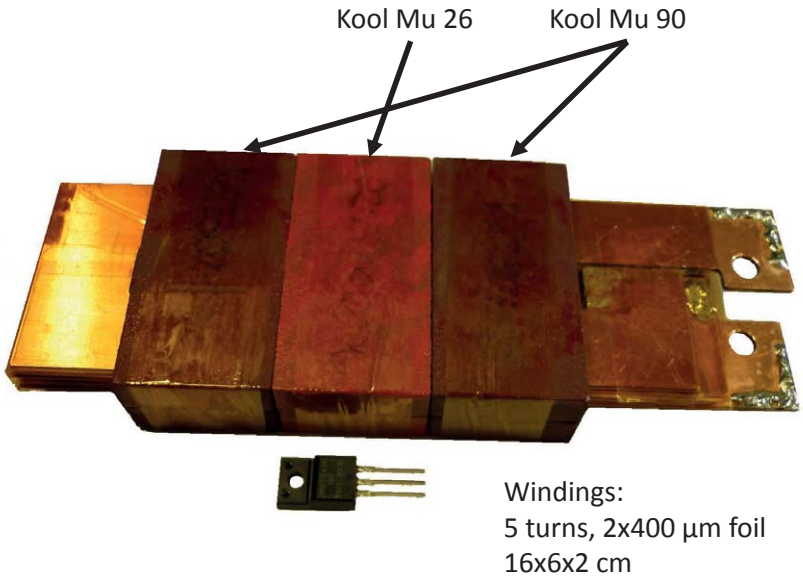


Figure 4.5: High current inductor prototype.

Chapter 5

Converter Design and Experimental Results

This chapter briefly summarizes the design approach utilized to design a high efficiency bidirectional dc-dc converter for fuel cells applications.

5.1 Converter Specifications and Topology

The SOEC/SOFC application does not have strict direct requirements for the converter topology; efficiency and converter cost are the main concerns for this application. Moreover, system galvanic isolation is desired and therefore an advantage for isolated converter topologies. The dc-dc converter is expected to operate with a variety of SOEC/SOFC cells. For this reason the converter is not tailored or optimized for a specific I-V curve.

The dc-dc converter specifications are defined in Table 5.1; the converter is often referred as a 6 kW converter, however, the maximum converter power is determined by the maximum converter current and voltage on its low voltage side.

Table 5.1: Converter specifications

Specifications	
Low voltage (LV) side	30-80 V
High voltage (HV) side	700-800 V
LV-side current	0-80 A
Power rating	1500-6400 W
Efficiency (peak)	≥98 %
Voltage ripple (LV)	<5%

The converter topology is selected based on an isolated full bridge boost converter (IFBBC) [35]. In order to achieve a high dc-dc conversion efficiency it is necessary to have an overview of all the loss components of the converter.

The main contribution to the converter losses can be summarized as:

- Power semiconductors losses: switching and conduction, LV and HV sides
- Magnetic components losses: core and winding
- Capacitive components losses
- Control and gate driver losses
- Cooling system.

Different approaches can be used to optimize a power converter. The most common approach considers the converter design constrains, available devices and resources [115]. This method evaluates all possible design combinations through recurring consecutive optimization loops. It also provides the absolute best design based on the desired design constrains however, it is very complicated to construct the complete optimization routine without incurring into large computational time and data handling issues [116].

A second approach is based on genetic algorithm where a constrained fitness function is used to evaluate the converter designs [117, 118]. This approach requires a databased of "genes", possible genes combinations and constrains for the genetic algorithm. The genetic algorithms do not evaluate all possible "genes" combinations, saving computation time. The convergence of the algorithm returns a local minimum of the fitness function, however the algorithm does not ensure that the local minimum is also the absolute minimum. For this reason, different instances of the genetic algorithm can return different minimums.

The approach utilized in this thesis is based on resource distribution of the losses, based on the converter specifications. Based on the design target efficiency, the resources are equally distributed and assigned to the main sources of converter losses, as in Figure 5.1. As second step, the main converter components are designed according to the resource allocation; a 20% margin factor is used in the resource allocation allowing better resource optimization based on available components.

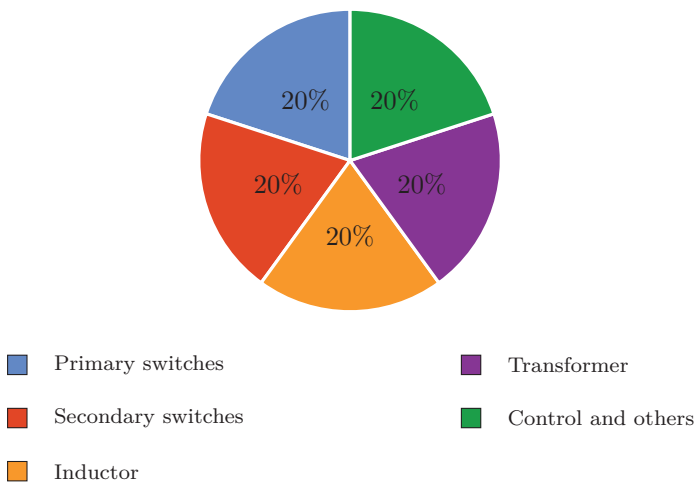


Figure 5.1: Arbitrary loss distribution

The design refinement is then performed, completing the optimization loop, as in Figure 5.2.

The design approach used for the converter design focuses on two key points:

- Optmize duty cycle operation range
- Maximize utilization factor of each converter component.

The converter duty cycle is dependent on the converter's voltages and transformer's turns ratio, as in Eq. 5.1. A conventional rule of thumb is to limit the variations in duty cycle in order to optimize the converter for a fixed operating point. Moreover, it is necessary to avoid extreme duty cycles. In this case, as the transformer's number of turns increase, the duty cycle operation range deceases, Eq. 5.2 and 5.3. However, reducing the transformer's turns require increased voltage ratings for the power semiconductors (low voltage side) and, as a consequence, the converter would operate at high average duty cycle. Since the candidate power semiconductors for the converter low voltage side are Si MOSFETs and their on-state resistance is $\propto V_{DS,max}^{2.5\sim2.7}$ [119], it is desirable to minimize the voltage ratings of these devices, and therefore choose high transformer turns ratio. High utilization of each converter component can provide high power density and low converter cost due to fewer materials. However, power density is often a trade-off with the efficiency requirements [120, 121]. For the magnetic components, this means utilize small magnetic cores with high fill factor. In a similar way for power semiconductors, it is required to select available devices with the lowest ratings that respect the resource constrains.

$$D = 1 - \frac{n}{2}\frac{V_{LV}}{V_{HV}} \tag{5.1}$$

$$D_{max} = 1 - \frac{n}{2}\frac{V_{LV,min}}{V_{HV,max}} \tag{5.2}$$

$$D_{min} = 1 - \frac{n}{2}\frac{V_{LV,max}}{V_{HV,min}} \tag{5.3}$$

The initial design approach used to evaluate the different source of losses in the converter is presented in Appendix K. The converter design and optimization is performed in order to prioritize the SOFC operating mode (with current up to 40 A). This mode is particularity trivial since the SOEC/SOFC stack can process about 1/4 of the power compared to SOEC mode. Additionally, SOFC mode is expected to operate during high electricity price, as presented in Appendix K. For these reasons, it is interesting to achieve the maximum conversion efficiency, around 40-50 A (maximum power from the cell stack in SOFC mode). Forehand calculations on the converter losses and on the size of the magnetic components determined that operating frequencies around 40 kHz would be suitable to achieve the desired performance.

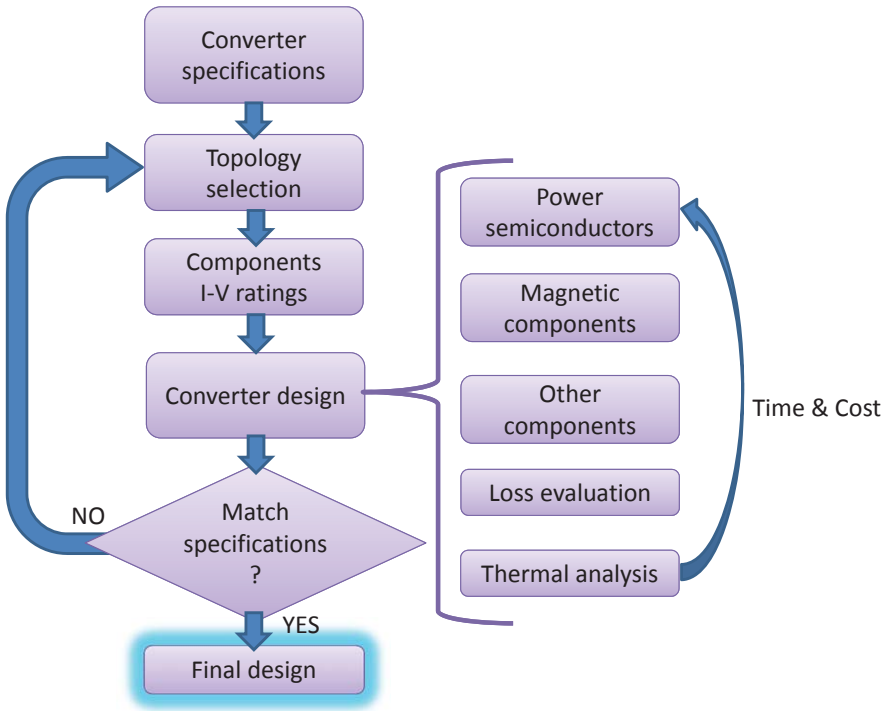


Figure 5.2: Converter design procedure

5.2 Magnetic Components

The design of magnetic components was performed based on planar E64 and E6030 cores. The methodology and different cases are briefly previously presented in section 4.4, in Appendix J and Appendix I. The converter magnetics are custom designed based on thick copper flat windings.

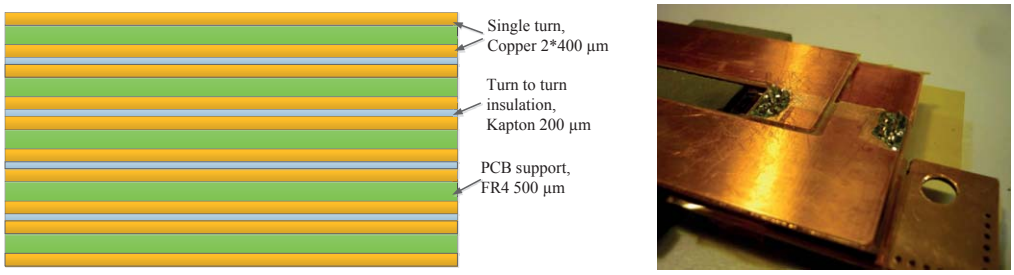
5.2.1 Boost Inductor

The boost inductor is operating at 80 kHz, twice the converter's switching frequency (40 kHz). In high power inductors a suitable ratio between the nominal inductor current (80 A) and the ripple current (peak to peak) is in the range from three to five times. This requires limiting the inductor ripple current to ~20 App and an inductance in the 10-20 μH range.

Candidate materials for the boost inductor are gapped ferrites and high flux materials. High flux distributed gap materials were preferred due to the absence of fringing flux and, therefore, simplifying the inductor structure. Moreover, distributed gap materials, such as Kool Mu, have an almost linear dc bias in the intended operating range (typically up to a 50-70 % reduction in permeability).

The final inductor prototype is based on three stacked cores. The combination of different Kool Mu permeabilities (90-26-90) allows achieving the desired inductance

levels while maintaining the inductance above 50%, also at full converter current. To maintain low dc and ac resistances thick copper PCB windings are used. The inductor requires five turns, where each turn occupies the entire winding area width (18 mm winding width and 20 mm winding area width). Each turn has two stacked 400 µm copper layers (top and bottom) on a PCB support, Figure 5.3a. The turn to turn insulation is ensured by Kapton layers and high current copper-filled vias interconnect subsequent turns, Figure 5.3b. The inductor's dimensions are comparable to two stacked planar E64 cores achieving a filling factor of ~36% and, together with its main characteristics, are presented in Table 5.2.



(a) Winding structure. **(b)** Turn to turn interconnections.

Figure 5.3: High current inductor prototype.

Table 5.2: Inductor prototype characteristics

Inductance	19.8μH
Inductance @80 A	>65 %
Dc-ac current ratio (rms)	6.5
Turns	5
Winding	PCB 2*400 µm
Turn-to-turn insulation	2*100 µm Kapton
Dc-resistance	1.47 mΩ
Ac-resistance (80 kHz)	22.3 mΩ
Rac/Rdc ratio	15.1
Core	E6030 planar
Core material/structure	Kool MU 90-26-90
Dimensions	160x60x20 mm

5.2.2 Transformer

The transformer in the IFBBC is operating at the converter switching frequency of 40 kHz. The large variations in converter duty cycle affect the transformer V-μs product and, therefore, its loss distribution.

E64 planar cores are easily available in Epcos N87, Magnetics R and P type materials. Magnetics R type material was selected due to its slightly lower losses compared to the other materials and also for its availability. The stacked transformer structure (two planar E64 pairs) allows to limit the number of transformer turns (large cross sectional area), which is especially critical for the primary winding (high current

winding). The primary winding (P) is interleaved with the secondary winding (S) in a PSPSP structure, Figure 4.2a. The interleaved structure reduces both winding ac resistance and leakage inductance [109]. Each of the three primary turns is realized with two parallel copper layers (400 µm). In order to achieve both high filling factor and high number of turns for the transformer secondary winding, thick Litz wires (30 strands of 0.2 mm diameter) are used for the two secondary winding sections (12 turns each). In the designed transformer prototype the achieved filling factor 32.4%.

Since the selected topology is operated without active clamp, the transformer leakage inductance will cause voltage overshoot and eventually avalanche losses on the primary power semiconductors. As consequence, the transformer design directly affects the switching losses on the converter low voltage side. Limiting the leakage inductance is necessary both to limit the power dissipation and to achieve the desired efficiency. The interleaved structure resulted in a leakage inductance of 78.2 nH, which represents 0.0286% of the transformer magnetizing inductance (273.9 μH). A summary of the main transformer characteristics is presented in Table 5.3.

Table 5.3: Transformer prototype characteristics

Turns ratio	8
Primary (LV-side)	3 turns
Secondary (HV-side)	24 turns
Core	2*E64 pairs
Core material	Magnetics R-type
Winding structure	PSPSP
Primary (P) winding	PCB 2*400 µm
Secondary (S) winding	30*200 µm Litz wire
Insulation P-S	2*100 µm Kapton
Operating frequency	40 kHz
Eq. primary magnetizing inductance	273.9 μH
Eq. primary resistance (40 kHz)	5.72 mΩ
Eq. primary leakage	78.2 nH
Dimensions	200x64x20 mm

A genetic transformer multi-objective optimization is setup in order to prove the potential of PCB windings, in order to achieve low transformer losses and low leakage. The optimization consider different PCB copper thicknesses (1-6 oz), insulation thicknesses, different winding structures (both interleaved and non-interleaved), core materials and core shapes. The output from the optimization is presented in Figure 5.4, where different transformer designs (blue dots) are presented as a Pareto front (red-dashed line) based on their total losses and on their leakage inductance. It is observed that the lowest leakage and power loss are achieved with stacked planar E64 cores (two stacked), with a large number of PCB layers (full-filling the winding area), with high copper thickness (6 oz) and with heavy interleaving (PSPSPSPS). This also results in high prototyping costs. It is important to observe that PCB windings with high interleaving can provide extremely low leakage inductance, well below 10 nH for a 6 kW 40 kHz transformer.

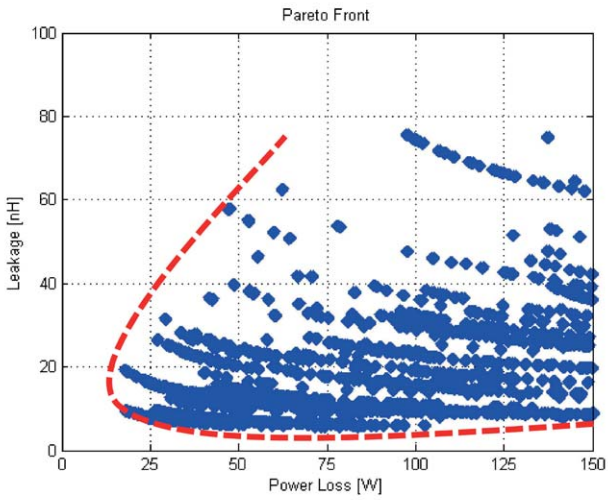


Figure 5.4: Example of a 6 kW 40 kHz PCB transformer multi-objective genetic optimization.

5.3 Power Semiconductors

Converter power semiconductors are selected based on the voltage-current ratings required by the topology, on power semiconductor availability, on package and power loss ratings.

5.3.1 Low Voltage Side

The full bridge on the converter low voltage side is required to handle the entire current from the SOEC/SOFC cells stack and to block the reflected voltage from the converter secondary side. This implies, that with a transformer turns ration of 8, the minimum blocking voltage for the primary side semiconductors has to be higher than 100 V. At this voltage range Si MOSFETs are the preferred devices in terms of static and dynamic performance, availability and cost. Other devices, such as GaN FET, might also be suitable at these voltage ratings. However, these devices became mostly available in 2013-2014 only and GaN FET mostly utilize LGA or PQFN packages which can provide low stray inductances but cannot handle high current and high power loss. For all these reasons GaN FET has not been considered.

The IFBBC topology is often used in combination with a voltage clamp. The voltage clamp limits the transient over voltage during the commutations of the primary side switches. In this case, it is required to have an operating margin between the maximum reflected voltage over the primary power semiconductors and the absolute maximum voltage rating of the primary power semiconductors. This margin is necessary to store and eventually ri-generate (active clamp) power over the clamping capacitor. For these reasons, to effectively utilize the clamping circuitry, 150-200 V rated Si MOSFET would be required.

Another approach relies on the ruggedness of modern Si MOSFETs. State of the art

Si MOSFETs can withstand repetitive avalanche conditions; in this case the phenomena is thermally limited as long as the maximum device and package absolute currents are limited. It is important that the absolute maximum device current is limited in order to avoid too high current densities in the chip-bond interface, which could cause interface and chip degradation. The maximum avalanche energy for Si MOSFETs is limited by the maximum junction temperature rise. The power MOSFETs can handle repetitive avalanche conditions as long as the avalanche losses are properly dissipated by the cooling system. In this way, it is possible to reduce the MOSFET's voltage ratings down to 120-150 V.

For Si MOSFETs the on-state resistance $m\Omega \cdot cm^2$ is proportional to the maximum drain to source voltage with an exponential coefficient between two and three (typically $\propto V_{DS,max}^{2.5\sim2.7}$ [119]). This implies that for limiting the converter conduction losses, it is desirable to utilize MOSFETs with lowest voltage ratings that are suitable for the selected topology. Assuming the package stray inductance of the low voltage side MOSFETs negligible, the current commutation loop inductance is determined by the transformer leakage and by the stray inductances of the interconnections and PCB, Eq. 5.4. At turn-off the power devices will be subject to an overvoltage due to the limited di/dt [7]. Assuming the turn-off event driven by the avalanche voltage of the MOSFETs ($V_{BR.MOS}$) and assuming the voltage constant during this interval, the current commutation time is calculated as in Eq. 5.5. This results that the contribution of the transformer leakage inductance on the MOSFET's switching losses ($P_{loss,stay}$) is expressed as in Eq. 5.6.

$$L_{tot,stray} = L_{leak,tr.} + L_{interconn.} + L_{pcb} \tag{5.4}$$

$$t_{off,di/dt} = L_{tot,stray} \cdot \frac{I_{DC,LV}}{V_{BR.MOS}} \tag{5.5}$$

$$P_{loss,stay} = f_{sw.} \cdot L_{tot,stray} \cdot I_{DC,LV}^2 \tag{5.6}$$

Under the assumption that the current ripply is negligible, the current in the primary side switches $I_{sw.LV,RMS}$ is calculated as in Eq. 5.7. This results that in the worst case operating conditions (maximum converter current and minimum duty cycle) each switch, on the primary side, would have to handle a current of 55 A.

$$I_{sw.LV,RMS} = I_{LV}\sqrt{\frac{3}{4} - \frac{D}{2}} \tag{5.7}$$

Both 120 V and 150 V Si MOSFETs are available with current ratings above 100 A in TO-220 and TO-247 packages. A 120 V MOSFET in TO-220 package has lower on-state resistance than a 150 V MOSFET in TO-247 package. Moreover, the TO-220 package has lower leakage inductance (about ~50%) compared to the TO-247 package. This leads that high power 120 V MOSFETs in TO-220 are preferable compared to higher voltage ratings. The same MOSFET chip is also available in other packages TO-263-7 (D2PAK-7); however, SMT packages cannot easily dissipate large amount of power (e.g. more than 5 W) without a significant increase of the junction temperature [122]. In fact, the device top side has too high junction to case thermal resistance and the bottom side tab requires thermal PCB vias [122] or PCB copper planes to transfer the heat away from the device. Double side

cooled packages (e.g DirectFET, Power-56-8, TSDSON-8, etc.) can minimize the package leakage inductance and they are also compatible with SMT technology which could potentially reduce the manufacturing cost. The major disadvantage of these packages is that they are not designed to dissipate a sustained amount of power and their low profile does not allow having other large SMD components on the same PCB side when a heatsink is mounted on the power device.

5.3.2 High Voltage Side

The full bridge on the converter high voltage side has to withstand the maximum dc-bus voltage (800 V) plus a margin factor. Assuming the ripple current in the boost inductor negligible and the switches are bidirectional, it is possible to express the device rms current $I_{sw.HV,RMS}$ as a function of the dc current on the converter low voltage side I_{LV}, of the duty cycle D and of the transformer turns ratio n, as shown in Eq. 5.8.

The power semiconductors on the converter high voltage side are required to handle a maximum current of ~10 A. Power devices rated at 1200 V and capable of handling currents above 15 A are chosen. With this specifications the main component candidates are Si IGBTs and SiC MOSFETs, as presented in section 3.3. IGBTs were selected, among the ones optimized for fast switching, in order to reduce the converter switching losses, when the power flow is form the high voltage side to the low voltage one.

$$I_{sw.HV,RMS} = I_{LV}\frac{\sqrt{1-D}}{n} \tag{5.8}$$

The first converter prototype, presented in Appendix K, is based on Si IGBTs. Even thought the selected IGBTs have low switching losses (IGW15N120H3 and IRG7PH30K10), there is a significant difference in converter efficiency depending on the power flow direction. This is also presented in the loss analysis in Appendix K. In SOFC mode, the converter high voltage power semiconductors are purely used for rectification while in SOEC mode these power semiconductors operate in hard switching conditions. Using IGBTs introduces large switching losses in SOEC mode, thus limiting the converter efficiency in this operating mode.

The use of SiC MOSFETs for the second converter prototype, presented in Appendix D, significantly improved the overall efficiency. The major efficiency improvement is due to the reduction of switching losses (SOEC mode); however, there is also a significant reduction of conduction losses (active rectification) which results in a peak efficiency above 98% in SOFC mode. Another major advantage is the overall loss reduction which allows to operate the devices at much lower junction temperature and eventually reduce the size of the converter colling system.

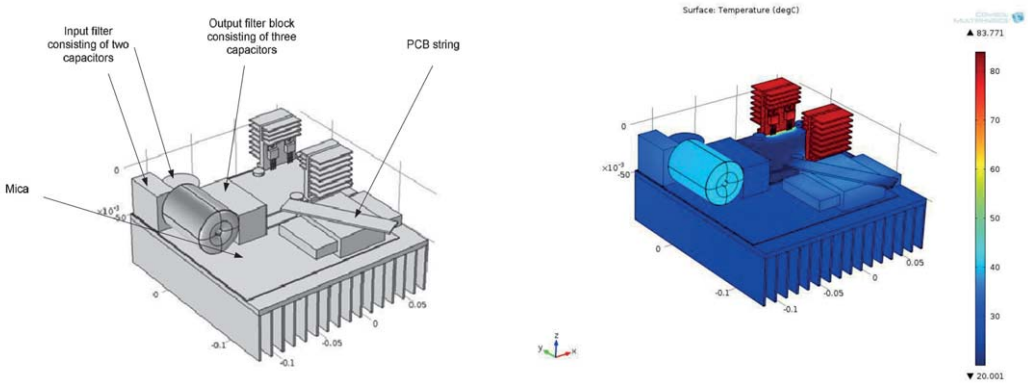
5.4 Thermal Analysis

Thermal analysis is a fundamental component in the design process of a power converter. Thermal investigations are initially performed on an IFBBC unidirectional

low power converter prototype, as presented in Appendix L and Appendix M. In a second step, the analysis considered the full power converter prototype. In this case the major concern is the short avalanche pulses (high power dissipation), which can cause power cycling stresses. Thus, a thermal analysis of the low voltage side power semiconductors is presented in Appendix N.

Appendix L contains an analysis on how the device temperature varies, when multiple devices are mounted on the same heatsink and its relation to the device distance. These cases are representative of power devices are mounted close to each other or when a unidirectional switch (e.g. IGBT) is combined with an external antiparallel diode. Moreover, the influence of the airflow (forced cooling) on the heatsink performance is presented.

Thermal analysis is performed on the individual converter components of the low power converter prototype, as presented in Appendix M. The layout of the converter's components affects strongly the temperature distribution in the converter. In order to increase the power density of the low power converter prototype, 3D FEM is used to design a boxed converter, shown in Figure 5.5a. Here, the converter components are rearranged to obtain a more compact design and their cooling capabilities are improved by introducing thermal interface materials between the converter components and the heatsink. Better thermal interface provides better cooling for the converter's components resulting in an overall reduction of the component's temperatures, shown in Figure 5.5b.



(a) 3D model. **(b)** Temperature distribution.

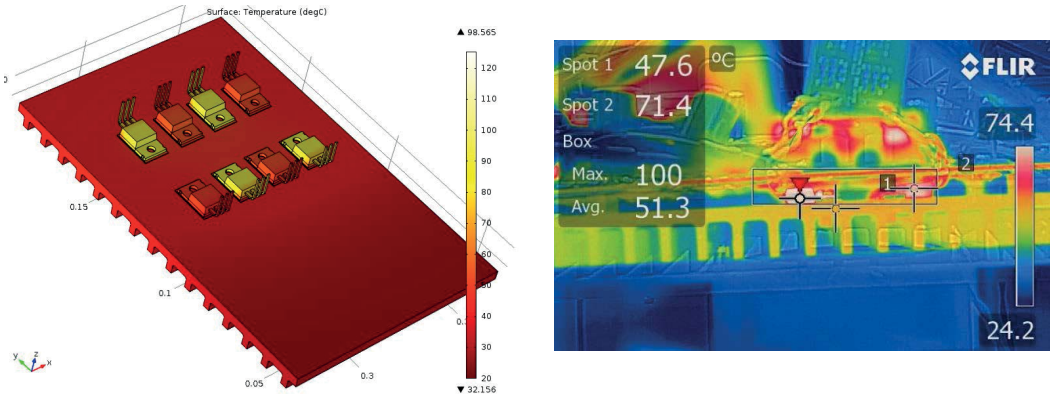
Figure 5.5: FEM analysis of a low power converter prototype in COMSOL.

Even thought modern MOSFETs are avalanche rated, it is necessary to verify that the maximum absolute device operating conditions are withstood (both maximum operating temperature and maximum device current) even for the worse converter operating conditions. This is presented in Appendix N.

Power cycling is a phenomena that slowly degrades the layers of the power semiconductor package, which would lead to a converter failure [123, 124]. Repetitive high power dissipation during avalanche pulses could cause the junction temperature to oscillate, thus degrading the package layers [125, 126]. It was verified that having low transformer leakage inductance limits the avalanche interval to ~60 ns at the nominal converter current. During this interval the power dissipation is not sufficient to instantaneously increase the junction temperature to critical levels, which

could cause power cycling stress.

The maximum operating temperature for the low voltage side power semiconductors was analyzed for both even and unequal distribution of the avalanche losses in these power semiconductors. FEM analysis highlights that in case of uneven distribution of avalanche losses, the MOSFET's case temperature can reach values ~100 °C (so the junction temperature), as seen from Figure 5.6a. This was also experimentally verified on the developed converter prototype, as shown in Figure 5.6b.



(a) 3D model. **(b)** Temperature distribution.

Figure 5.6: FEM analysis and temperature distribution on the low voltage side of the full power converter prototype (full load, 80 V 80 A).

5.5 Efficiency and Measuring System

Power conversion efficiency has been one of the major concerns related to the converter design. During the studies three converter prototypes were developed: a low power prototype (1 kW), a full power converter prototype based on Si IGBTs and one based on SiC MOSFETs.

The first converter prototype was developed to perform initial studies on the IF-BBC topology and on planar magnetics. The full power prototype, shown in Figure 5.7, was initially designed to prove the achievable performance with Si power semiconductors, as presented in Appendix K.

This converter proved to achieve efficiencies up to 97.8% in SOFC mode and up to 96.5% in SOEC mode. This prototype has been afterwards upgraded to operate with SiC MOSFETs.

The efficiency of the final converter prototype, based on SiC MOSFETs, is presented in Appendix D and Appendix B, as shown in Figure 5.8 for both SOEC and SOFC operating modes. Measurements were performed according to the converter specification in Table 5.1. Efficiency characterization was performed with a fixed dc-link voltage of 750 V and by varying the voltage on the converter primary side allowing currents up to 80 A. Measured efficiencies are linearly interpolated and plot in Figure 5.8. These values also take into account the control and cooling (fans) losses. For both converter operating modes the highest efficiency is achieved with

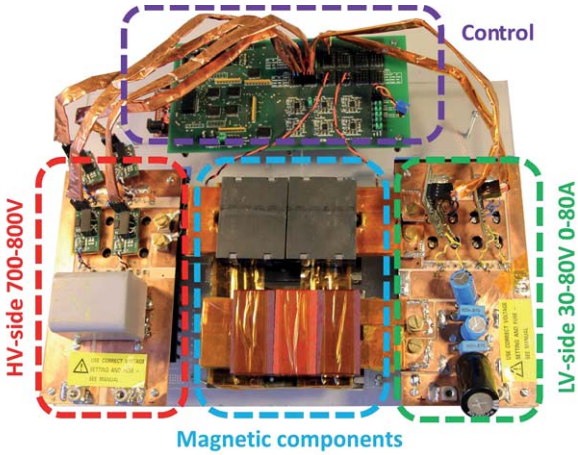


Figure 5.7: Full power converter prototype, operated first with Si IGBTs then upgraded to SiC MOSFETs.

the converter operating at 80 V at a power of ~3 kW. In SOFC mode the achieved efficiency is up to 98.2%, while in SOEC mode this is limited to 97.45%. The total converter power loss are briefly presented in Figure 5.9.

The converter efficiency that take into account the I-V curve of the SOEC/SOFC stack is presented in Figure 5.10. It is possible to observe that an efficiency improvement around 1% is achieved compared to the converter prototype based on Si IGBTs (as presented in Figure 2.7). This efficiency improvement come at a price of a higher cost for the high voltage power semiconductors (increased by ~80$).

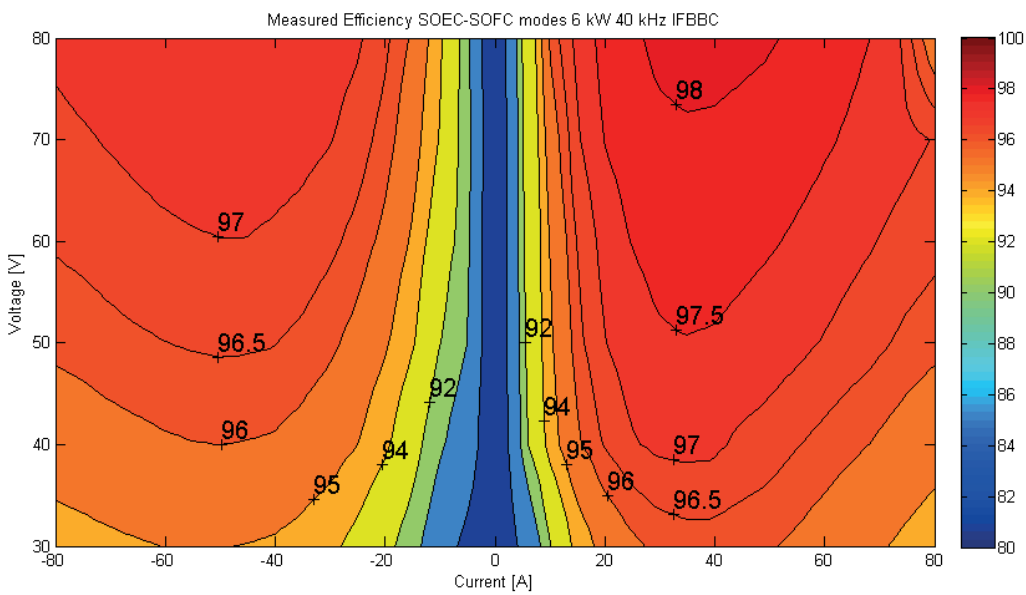


Figure 5.8: Efficiency of the developed converter prototype (IFBBC topology) based on SiC MOSFETs considering gate and control losses. SOEC operating mode (left side) and SOFC operating mode (right side).

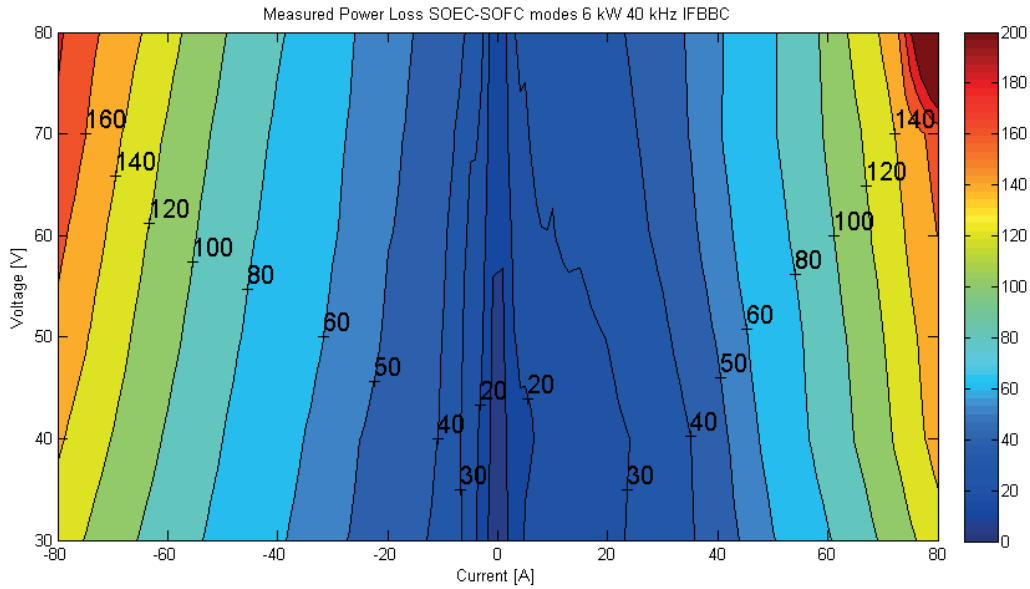


Figure 5.9: Power loss [W] of the developed converter prototype (IFBBC topology) based on SiC MOSFETs considering gate and control losses. SOEC operating mode (left side) and SOFC operating mode (right side).

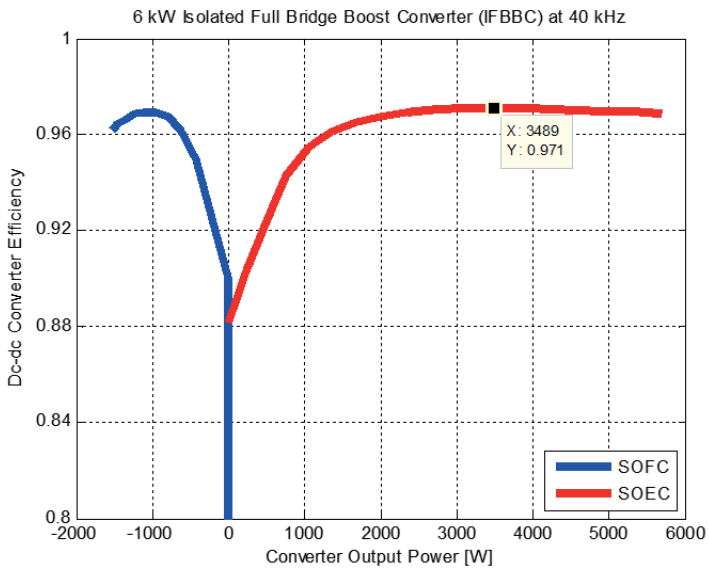


Figure 5.10: Efficiency of the developed converter prototype (SiC MOSFETs) tanking into account the I-V curve of the SOEC/SOFC stack.

5.5.1 Measuring System

Measuring power loss from very high efficiency converters is not trivial. Three methods are mostly used: traditional voltage-current measurement, calorimeter loss measurement [127, 128] or losses measurement through two bidirectional converters (closed loop) [129]. Measuring the power converter losses through a voltage-current

measurement is the most straight forward method. The major drawback of this method is the large error, which can be encountered if the setup is not properly analyzed and calibrated. A proven method that provides high accuracy is the loss measurement through a calorimeter [127, 128]. This method is especially suited for high efficiency converters (dc-dc, dc-ac, ac-dc), however it requires the design and calibration of a calorimeter (time and cost) and the converter size is constrained by the calorimeter chamber. Last method considers two bidirectional converters in a closed loop configuration [129]. In this case, only the power loss is fed to the system and the renaming power flow is regenerated in the converters as a closed loop system. Even though it is possible to measure the energy fed to the system with high accuracy, it is not directly possible to separate the losses between the two converters in the closed energy loop.

For the developed dc-dc converter prototype, the efficiency was characterized based on a voltage-current measurement calibrated setup as presented in Figure 5.11. Four high precision multimeters (Agilent 34410A) were used to measure converter voltages and currents. The instruments were connected and synchronized through a PC, as in Figure 5.11, and set up with long integration times to ensure sufficient high frequency noise filtering. The absolute error on the efficiency, due to the instruments accuracy, is <0.01 % (taking into account measurement range, temperature and last calibration). However, dc currents are measured through high power precision (0.1 %) current shunts. This leads that before system calibration in the worst case scenario, the absolute error on efficiency was ~0.2 %. After shunt calibration the maximum error on efficiency is less than 0.1 %, which is acceptable for efficiency characterization.

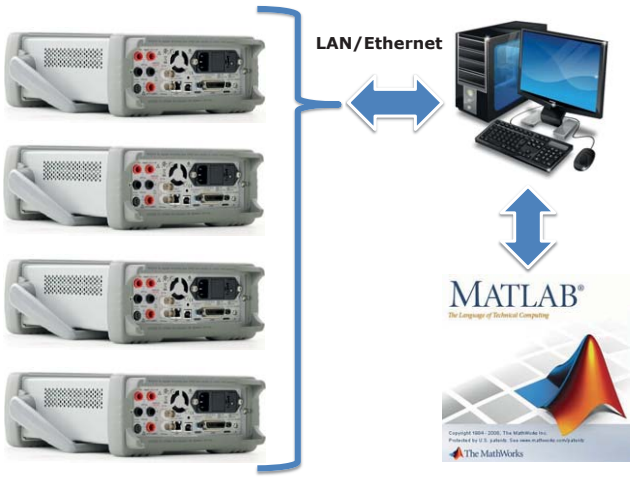


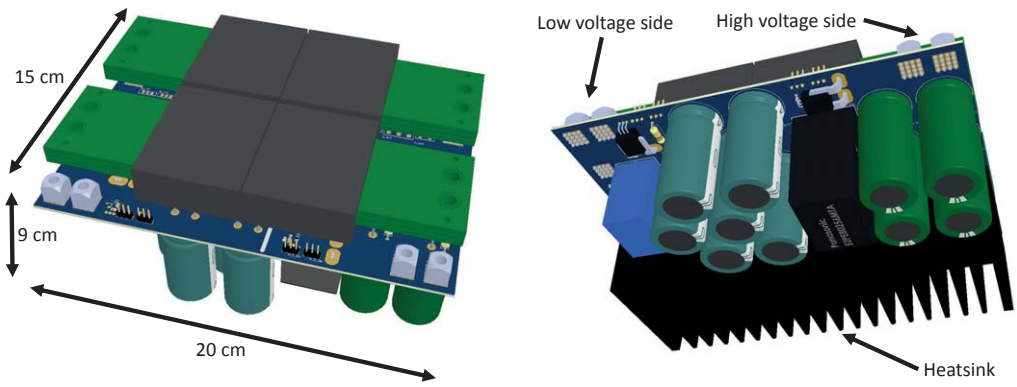
Figure 5.11: Efficiency measurement setup.

5.6 Redesign for High Power Density

The converter prototype was designed to have easy access to the different converter components. A rearrangement of the converter layout can significantly increase the

converter power density, while maintaining the same converter components. The layout of the critical paths, such as low voltage and high voltage side bridges, is maintained as in the original prototype. This also implies that the new layout, shown in Figure 5.12a and 5.12b, has the same efficiency performance as the previous design. The control board and the power semiconductors gate drivers are placed between the magnetic components and the main power board.

The new converter layout can achieve peak efficiency above 98% with a power density of 2.2 kW/l.



(a) Top view. **(b)** Bottom view.

Figure 5.12: New converter layout.

Chapter 6

Conclusion

The presented work analyzes the electrical systems of an energy storage system based on bidirectional SOEC/SOFC cells. The main focus was the bidirectional operation of the dc-dc converter, which directly interfaces with the SOEC/SOFC cells stack. The design of this converter is particularly challenging due to the converter wide operating conditions and economic profitability of the system. The analysis includes both system and power converters electric efficiency, including the detailed design of the dc-dc converter and its components.

The major challenges that have been addressed are:

- The design of high efficiency dc-dc converters for fuel cells is challenging due to the low voltage high current characteristics typical of fuel cells. These operating conditions are further stressed in SOEC/SOFC due to even wider operating ranges.

- Selecting the most suitable topology for a specific application is a key component in designing high efficiency converters. However, there is no proved straight forward methodology.

- Converter design and optimization are complex problems which have to take into account several factors such as application, cost and time. The solution to the problem is not unique.

- New power semiconductors have been recently introduced on the market. These devices are proven to be superior compared to Si semiconductors however, their selection is not trivial due to their limited availability, increased costs and unknown long term reliability.

- Planar magnetics can represent a solution for low cost magnetic components and high power density converters. However, designing highly efficient planar magnetics is challenging mostly due to the low fill factors and large stray parameters of this technology.

In order to prove that a simple topology, if properly designed, can provide high efficiency over a wide operating range, the design of a high efficiency dc-dc converter for bidirectional operation of SOEC/SOFC cells is performed. The analysis firstly studies the system on its overall taking into account the voltage-current characteristics of the SOEC/SOFC cell stacks. These characteristics are used to define the converter topology, to characterize the converter efficiency for the given application and to design the converter components.

The outcome from the studies highlights that:

- High conversion efficiency is achieved by distributing the converter losses over the major converter components. In this case simple non-resonant topologies are capable of very high conversion efficiencies (with peak efficiencies above 98%), even when the converter is designed for wide operating ranges.
- Integrated ac-dc and dc-dc converters based on matrix-type PFC topologies represent a valid alternative in SOEC/SOFC systems. However, this significantly increases the number of active components in the power converter and complexity of the control.
- Dc-dc converter efficiency is required to be characterized based on the specific application. In SOEC/SOFC systems the voltage-current characteristics of the SOEC/SOFC cell stacks determine the dc-dc converter operating points, affecting its efficiency curve.
- In the 600-1200 V range, replacing Si power devices with SiC power semiconductors can easily reduce the converter switching losses up to 80% and also provide a reduction of the converter conduction losses at light loads. This gives a significant efficiency improvement over the entire converter operating range.
- High current planar magnetics can be designed for high efficiency and high power density. This requires high fill factors of the magnetic components, which are achieved by copper foil or thick copper PCB windings (e.g. with 6 oz).
- High current planar transformers with high turns ratio can be achieved by hybrid transformer winding structures, such as combining copper foil and Litz wires.
- Modern power MOSFETs are avalanche tolerant, therefore converter clamping circuitry may be omitted, simplifying the converter circuitry and reducing the converter cost. This is valid as long as the additional avalanche losses are taken into account during the design phase of the converter cooling system and the device's absolute maximum operating conditions are respected.

6.1 Perspective and Future Work

Further research work is required to bring the design to a final product, to perform further optimizations and to achieve even higher power densities. Issues that have

not been addressed in this thesis are related to the different control methodologies and modulation techniques which can be investigated on the developed converter. Moreover, depending on the application, converter EMI compliance might be required, therefore requiring a dedicated EMI filter.

Further research should be addressed on:

- Thermal management: Analyzing reliability issues in connection with planar magnetics focusing thermal management issues especially for PCB vias interconnections (hot spots) between the PCB layers.
- Interconnections: Analysis of high current low inductive connections for rapid converter assembly (e.g. inductor and transformer terminations).
- Power density: Optimize the layout of the converter components in order to increase further more its power density. This can be achieved by using a smaller heatsink with high CFM fans and rearranging the fundamental converter components.
- Converter control: Analyzed advanced control techniques for the IFBBC topology. This could include phase-shift modulation of the high voltage full bridge in order to achieve soft switching.
- Electromagnetic compatibility (EMC/EMI): In applications which require to comply EMC regulations, an EMI filter is required. This will reduce the converter power density and also affects its efficiency.

Chapter 7

Other Research Topics

Research performed during the PhD studies was not entirely focused on high efficiency dc-dc converters. Thanks to collaborative discussions with colleagues and supervisors new ideas and concept were developed and demonstrated.

7.1 High Voltage High Step-Up Flyback Topology

A new flyback–based topology has been proposed for low power applications which requires very high voltages with high step-up ratios. The topology named "Primary Parallel Secondary Series Flyback Converter" (PPSSFC), shown in Figure 7.1, was developed to achieve very high step-up ratios minimizing the converter complexity and cost. The topology is presented and analyzed in Appendix O and compared with other solutions in Appendix P.

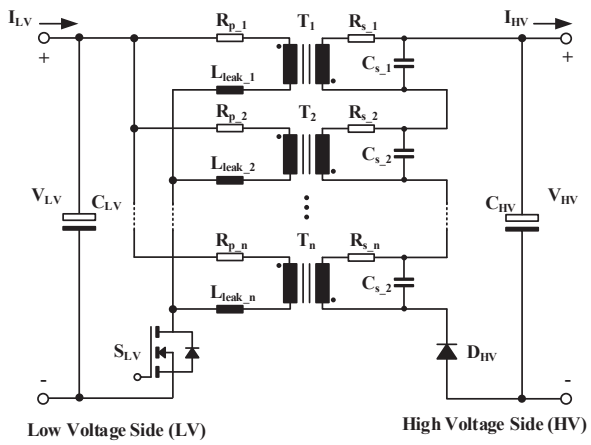
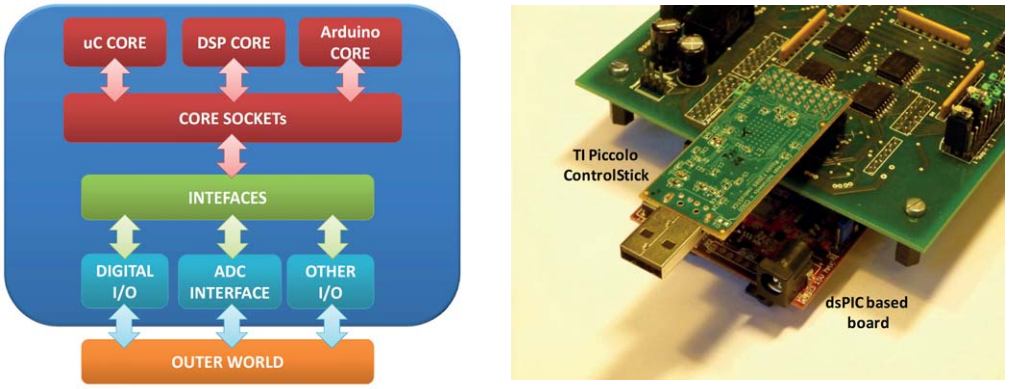


Figure 7.1: Primary Parallel Secondary Series Flyback Converter (PPSSFC) topology.

7.2 Modular Concept for Power Electronics Control Board

A new modular concept for implementing a prototyping converter control board for testing power electronics is presented in Appendix Q. The concept has an approach similar to the Arduino; the interface board for power electronics provides the flexibility of using the desired developing platform between the Arduino, a dsPIC based Arduino and the TI piccolo DSP controlSTICK, as presented in Figure 7.2a and 7.2b.



(a) Block view. **(b)** Control board prototype.

Figure 7.2: Developed control board.

Bibliography

[1] A. Richter, E. van der Laan, W. Ketter, and K. Valogianni, "Transitioning from the traditional to the smart grid: Lessons learned from closed-loop supply chains," in *Smart Grid Technology, Economics and Policies (SG-TEP), 2012 International Conference on*, pp. 1–7, Dec 2012.

[2] J. Barton and D. Infield, "Energy storage and its use with intermittent renewable energy," *Energy Conversion, IEEE Transactions on*, vol. 19, pp. 441–448, June 2004.

[3] M. Harfman Todorovic, L. Palma, and P. Enjeti, "Design of a wide input range dc-dc converter with a robust power control scheme suitable for fuel cell power conversion," *Industrial Electronics, IEEE Transactions on*, vol. 55, pp. 1247–1255, March 2008.

[4] SMA solar inverters, SUNNY TRIPOWER 15000TL/20000TL high efficiency series.

[5] J. Rabkowski, D. Peftitsis, and H.-P. Nee, "Design steps toward a 40-kva sic jfet inverter with natural-convection cooling and an efficiency exceeding 99.5pp. 1589–1598, July 2013.

[6] C. Zheng, R. Chen, H. Ma, B. Chen, C.-L. Chen, W. Yu, J.-S. Lai, and E. Faraci, "An optimization design for 5-kw centralized pv inverter to achieve 99efficiency," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, pp. 2967–2970, March 2013.

[7] M. Nymand and M. A. E. Andersen, "High-efficiency isolated boost dc-dc converter for high-power low-voltage fuel-cell applications," *Industrial Electronics, IEEE Transactions on*, vol. 57, pp. 505–514, Feb 2010.

[8] N. Sharma, J. Gummeson, D. Irwin, T. Zhu, and P. Shenoy, "Leveraging weather forecasts in renewable energy systems," *Sustainable Computing: Informatics and Systems*, vol. 4, no. 3, pp. 160 – 171, 2014.

[9] M. Swierczynski, R. Teodorescu, C. N. Rasmussen, P. Rodriguez, and H. Vikelgaard, "Overview of the energy storage systems for wind power integration enhancement," in *Industrial Electronics (ISIE), 2010 IEEE International Symposium on*, pp. 3749–3756, July 2010.

[10] C. Baumann, R. Schuster, and A. Moser, "Economic potential of power-to-gas energy storages," in *European Energy Market (EEM), 2013 10th International Conference on the*, pp. 1–6, May 2013.

[11] S. Aso, M. Kizaki, and Y. Nonobe, "Development of fuel cell hybrid vehicles in toyota," in *Power Conversion Conference - Nagoya, 2007. PCC '07*, pp. 1606–1611, April 2007.

[12] V. Mehta and J. S. Cooper, "Review and analysis of {PEM} fuel cell design and manufacturing," *Journal of Power Sources*, vol. 114, no. 1, pp. 32 – 53, 2003.

[13] A. Stambouli and E. Traversa, "Solid oxide fuel cells (sofcs): a review of an environmentally clean and efficient source of energy," *Renewable and Sustainable Energy Reviews*, vol. 6, no. 5, pp. 433 – 455, 2002.

[14] S. Martin, P. Garcia-Ybarra, and J. Castillo, "High platinum utilization in ultra-low pt loaded pem fuel cell cathodes prepared by electrospraying," *International Journal of Hydrogen Energy*, vol. 35, no. 19, pp. 10446 – 10451, 2010. Indo-French Workshop on Biohydrogen: from Basic Concepts to Technology.

[15] A. Rodrigues, J. Amphlett, R. Mann, B. Peppley, and P. Roberge, "Carbon monoxide poisoning of proton-exchange membrane fuel cells," in *Energy Conversion Engineering Conference, 1997. IECEC-97., Proceedings of the 32nd Intersociety*, pp. 768–773 vol.2, Jul 1997.

[16] X. Cheng, Z. Shi, N. Glass, L. Zhang, J. Zhang, D. Song, Z.-S. Liu, H. Wang, and J. Shen, "A review of pem hydrogen fuel cell contamination: Impacts, mechanisms, and mitigation," *Journal of Power Sources*, vol. 165, no. 2, pp. 739 – 756, 2007. IBA HBC 2006 Selected papers from the International Battery Association, Hawaii Battery Conference 2006 Waikoloa, Hawaii, USA, 9-12 January 2006.

[17] P. Mocoteguy and A. Brisse, "A review and comprehensive analysis of degradation mechanisms of solid oxide electrolysis cells," *International Journal of Hydrogen Energy*, vol. 38, no. 36, pp. 15887 – 15902, 2013.

[18] J. Hartvigsen, S. Elangovan, L. Frost, A. Nickens, C. M. Stoots, J. E. O'Brien, and J. S. Herring, "Carbon dioxide recycling by high temperature co-electrolysis and hydrocarbon synthesis," *ECS Trans.*, vol. 12, no. 1, pp. 625 – 637, 2008.

[19] J. P. Stempien, O. L. Ding, Q. Sun, and S. H. Chan, "Energy and exergy analysis of solid oxide electrolyser cell (soec) working as a {CO2} mitigation device," *International Journal of Hydrogen Energy*, vol. 37, no. 19, pp. 14518 – 14527, 2012. {HYFUSEN} Special Issue for the 4th National - 3rd Latin American Conference on Hydrogen and Sustainable Energy Sources (HYFUSEN), 6-9 June 2011, Mar Del Plata, Argentina.

[20] D. Stimoniaris, D. Tsiamitros, N. Poulakis, T. Kottas, V. Kikis, and E. Dialynas, "Investigation of smart grid topologies using pilot installations experimental results," pp. 1–8, 2011.

[21] J. Van Mierlo, Y. Cheng, J.-M. Timmermans, and P. Van Den Bossche, "Comparison of fuel cell hybrid propulsion topologies with super-capacitor," in *Power Electronics and Motion Control Conference, 2006. EPE-PEMC 2006. 12th International*, pp. 501–505, Aug 2006.

[22] P. Garcia, L. Fernandez, C. Garcia, and F. Jurado, "Energy management system of fuel-cell-battery hybrid tramway," *Industrial Electronics, IEEE Transactions on*, vol. 57, pp. 4013–4023, Dec 2010.

[23] W. Gao, "Performance comparison of a fuel cell-battery hybrid powertrain and a fuel cell-ultracapacitor hybrid powertrain," *Vehicular Technology, IEEE Transactions on*, vol. 54, pp. 846–855, May 2005.

[24] R. Herrera, P. Salmeron, and H. Kim, "Instantaneous reactive power theory applied to active power filter compensation: Different approaches, assessment, and experimental results," *Industrial Electronics, IEEE Transactions on*, vol. 55, pp. 184–196, Jan 2008.

[25] R. Zimmerman and H. Lokay, "Economic comparison of secondary voltages; single- and three-phase distribution for residential areas [includes discussion]," *Power Apparatus and Systems, Part III. Transactions of the American Institute of Electrical Engineers*, vol. 75, pp. –, Jan 1956.

[26] T. Rump, H.-G. Eckel, and D. Weis, "Efficiency comparison of 690v-converter topologies for wind power plants with dfig," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, pp. 1–7, Sept 2013.

[27] G. Orfanoudakis, S. Sharkh, M. Yuratich, and M. Abusara, "Loss comparison of two and three-level inverter topologies," in *Power Electronics, Machines and Drives (PEMD 2010), 5th IET International Conference on*, pp. 1–6, April 2010.

[28] S. Igarashi, S. Miyashita, H. Wakimoto, H. Nakazawa, and Y. Okuma, "Advanced three-level converter with newly developed 1200v reverse blocking igbts," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, pp. 1–7, Aug 2011.

[29] T. Friedli, M. Hartmann, and J. Kolar, "The essence of three-phase pfc rectifier systems - part ii," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 543–560, Feb 2014.

[30] M. Salato, A. Zolj, D. Becker, and B. Sonnenberg, "Power system architectures for 380v dc distribution in telecom datacenters," in *Telecommunications Energy Conference (INTELEC), 2012 IEEE 34th International*, pp. 1–7, Sept 2012.

[31] A. Pratt, P. Kumar, and T. Aldridge, "Evaluation of 400v dc distribution in telco and data centers to improve energy efficiency," in *Telecommunications Energy Conference, 2007. INTELEC 2007. 29th International*, pp. 32–39, Sept 2007.

[32] P. Cortes, L. Fassler, D. Bortis, J. Kolar, and M. Silva, "Detailed analysis and design of a three-phase phase-modular isolated matrix-type pfc rectifier," in

Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), 2014 International, pp. 3864–3871, May 2014.

[33] A. Forsyth, "Review of resonant techniques in power electronic systems," *Power Engineering Journal*, vol. 10, pp. 110–120, June 1996.

[34] R. Beiranvand, M. Zolghadri, B. Rashidian, and S. Alavi, "Optimizing the llc-lc resonant converter topology for wide-output-voltage and wide-output-load applications," *Power Electronics, IEEE Transactions on*, vol. 26, pp. 3192–3204, Nov 2011.

[35] N. Frohleke, R. Mende, H. Grotstollen, B. Margaritis, and L. Vollmer, "Isolated boost full bridge topology suitable for high power and power factor correction," in *Industrial Electronics, Control and Instrumentation, 1994. IECON '94., 20th International Conference on*, vol. 1, pp. 405–410 vol.1, Sep 1994.

[36] L. Zhu, "A novel soft-commutating isolated boost full-bridge zvs-pwm dc/dc converter for bidirectional high power applications," *Power Electronics, IEEE Transactions on*, vol. 21, pp. 422–429, March 2006.

[37] R. De Doncker, D. Divan, and M. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications," *Industry Applications, IEEE Transactions on*, vol. 27, pp. 63–73, Jan 1991.

[38] J. Everts, J. Van den Keybus, F. Krismer, J. Driesen, and J. Kolar, "Switching control strategy for full zvs soft-switching operation of a dual active bridge ac/dc converter," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, pp. 1048–1055, Feb 2012.

[39] L. Petersen and M. Andersen, "Two-stage power factor corrected power supplies: the low component-stress approach," in *Applied Power Electronics Conference and Exposition, 2002. APEC 2002. Seventeenth Annual IEEE*, vol. 2, pp. 1195–1201 vol.2, 2002.

[40] V. Menon, V. M. Janardhanan, and O. Deutschmann, "A mathematical model to analyze solid oxide electrolyzer cells (soecs) for hydrogen production," *Chemical Engineering Science*, vol. 110, no. 0, pp. 83 – 93, 2014. Mackie-2013 Pushing the boundaries.

[41] S. Njoya, O. Tremblay, and L.-A. Dessaint, "A generic fuel cell model for the simulation of fuel cell vehicles," in *Vehicle Power and Propulsion Conference, 2009. VPPC '09. IEEE*, pp. 1722–1729, Sept 2009.

[42] F. Krismer and J. Kolar, "Accurate power loss model derivation of a high-current dual active bridge converter for an automotive application," *Industrial Electronics, IEEE Transactions on*, vol. 57, pp. 881–891, March 2010.

[43] R.-Y. Duan and J.-D. Lee, "High-efficiency bidirectional dc-dc converter with coupled inductor," *Power Electronics, IET*, vol. 5, pp. 115–123, January 2012.

[44] C. Mueller and J. Hilibrand, "The "thyristor" amp: A new high-speed switching transistor," *Electron Devices, IRE Transactions on*, vol. 5, pp. 2–5, Jan 1958.

[45] M. Adler, K. Owyang, B. Baliga, and R. Kokosa, "The evolution of power device technology," *Electron Devices, IEEE Transactions on*, vol. 31, pp. 1570–1591, Nov 1984.

[46] B. Baliga, M. S. Adler, R. Love, P. Gray, and N. Zommer, "The insulated gate transistor: A new three-terminal mos-controlled bipolar power device," *Electron Devices, IEEE Transactions on*, vol. 31, pp. 821–828, Jun 1984.

[47] D. Huber, "Technology and market trends for silicon wafers for power devices," in *Power Semiconductor Devices and ICs, 1995. ISPSD '95., Proceedings of the 7th International Symposium on*, pp. 2–7, May 1995.

[48] P. Gammon, "Silicon and the wide bandgap semiconductors, shaping the future power electronic device market," in *Ultimate Integration on Silicon (ULIS), 2013 14th International Conference on*, pp. 9–13, March 2013.

[49] H. Mantooth, M. Glover, and P. Shepherd, "Wide bandgap technologies and their implications on miniaturizing power electronic systems," *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol. 2, pp. 374–385, Sept 2014.

[50] M. A. Briere, "Gan-based power devices offer game-changing potential in power-conversion electronics," 2008, www.eetimes.com, document id 1272514, consulted on 2014-10-13.

[51] O. Semiconductor, "Gan /sic /si /gaas high power rf transistors comparison," 2014, www.oki.com, consulted on 2014-10-13.

[52] A. Itoh, T. Kimoto, and H. Matsunami, "Efficient power schottky rectifiers of 4h-sic," in *Power Semiconductor Devices and ICs, 1995. ISPSD '95., Proceedings of the 7th International Symposium on*, pp. 101–106, May 1995.

[53] N. Kaminski and O. Hilt, "Sic and gan devices - wide bandgap is not all the same," *Circuits, Devices Systems, IET*, vol. 8, pp. 227–236, May 2014.

[54] P. Friedrichs, "Silicon carbide power devices - status and upcoming challenges," in *Power Electronics and Applications, 2007 European Conference on*, pp. 1–11, Sept 2007.

[55] CREE, "Cree introduces 150-mm 4hn silicon carbide epitaxial wafers," 2012, www.cree.com/News-and-Events, consulted on 2014-10-10.

[56] G. Bulman, J. Edmond, H. Kong, M. Leonard, V. Dmitriev, K. Irvine, V. Nikolaev, A. Zubrilov, and D. Tsvetkov, "Recent progress in gan/sic leds and photopumped lasers," in *Lasers and Electro-Optics Society Annual Meeting, 1995. 8th Annual Meeting Conference Proceedings, Volume 1., IEEE*, vol. 2, pp. 100–101 vol.2, Oct 1995.

[57] N. Ikeda, Y. Niiyama, H. Kambayashi, Y. Sato, T. Nomura, S. Kato, and S. Yoshida, "Gan power transistors on si substrates for switching applications," *Proceedings of the IEEE*, vol. 98, pp. 1151–1161, July 2010.

[58] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 2155–2163, May 2014.

[59] E. E. P. Conversion, "Enhancement-mode gallium nitride transistors," 2014, epc-co.com/epc, consulted on 2014-10-13.

[60] Y. Developpement, "Wide band gap power electronics: A path toward co2 emission decrease," 2014, www.semiconwest.org, consulted on 2014-10-13.

[61] B. Baliga, "Trends in power semiconductor devices," *Electron Devices, IEEE Transactions on*, vol. 43, pp. 1717–1731, Oct 1996.

[62] R. Singh, J. Cooper, J.A., M. Melloch, T. Chow, and J. Palmour, "Sic power schottky and pin diodes," *Electron Devices, IEEE Transactions on*, vol. 49, pp. 665–672, Apr 2002.

[63] S. Round, M. Heldwein, J. Kolar, I. Hofsajer, and P. Friedrichs, "A sic jfet driver for a 5 kw, 150 khz three-phase pwm converter," in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, vol. 1, pp. 410–416 Vol. 1, Oct 2005.

[64] Y. Li, P. Alexandrov, and J. Zhao, "1.88- $m\omega \cdot \mathrm{cm}^2$ 1650-v normally on 4h-sic ti-vjfet," *Electron Devices, IEEE Transactions on*, vol. 55, pp. 1880–1886, Aug 2008.

[65] G. Kelner, M. Shur, S. Binari, K. Sleger, and H.-S. Kong, "High-transconductance beta;-sic buried-gate jfets," *Electron Devices, IEEE Transactions on*, vol. 36, pp. 1045–1049, Jun 1989.

[66] R. Kelley, A. Ritenour, D. Sheridan, and J. Casady, "Improved two-stage dc-coupled gate driver for enhancement-mode sic jfet," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, pp. 1838–1841, Feb 2010.

[67] A. Mihaila, F. Udrea, P. Godignon, G. Brezeanu, R. Malhan, A. Rusu, J. Millan, and G. Amaratunga, "Towards fully integrated sic cascade power switches for high voltage applications," in *Power Semiconductor Devices and ICs, 2003. Proceedings. ISPSD '03. 2003 IEEE 15th International Symposium on*, pp. 379–382, April 2003.

[68] J. Biela, D. Aggeler, D. Bortis, and J. Kolar, "Balancing circuit for a 5-kv/50-ns pulsed-power switch based on sic-jfet super cascode," *Plasma Science, IEEE Transactions on*, vol. 40, pp. 2554–2560, Oct 2012.

[69] D. Aggeler, F. Canales, J. Biela, and J. Kolar, "D v /d t -control methods for the sic jfet/si mosfet cascode," *Power Electronics, IEEE Transactions on*, vol. 28, pp. 4074–4082, Aug 2013.

[70] K. Tone, J. Zhao, L. Fursin, P. Alexandrov, and M. Weiner, "4h-sic normally-off vertical junction field-effect transistor with high current density," *Electron Device Letters, IEEE*, vol. 24, pp. 463–465, July 2003.

[71] B. Wrzecionko, D. Bortis, J. Biela, and J. Kolar, "Novel ac-coupled gate driver for ultrafast switching of normally off sic jfets," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 3452–3463, July 2012.

[72] Y. Kondo, T. Takahashi, K. Ishii, Y. Hayashi, E. Sakuma, S. Misawa, H. Daimon, M. Yamanaka, and S. Yoshida, "Experimental 3c-sic mosfet," *Electron Device Letters, IEEE*, vol. 7, pp. 404–406, Jul 1986.

[73] J. Casady, A. Agarwal, L. Rowland, S. Seshadri, R. Siergiej, D. Sheridan, S. Mani, P. A. Sanger, and C. Brandt, "Silicon carbide power mosfet technology," in *Compound Semiconductors, 1997 IEEE International Symposium on*, pp. 359–362, Sep 1998.

[74] CREE, "Cree sic c2m0025120d 2nd-generation z-fet mosfets," 2014, www.cree.com/Power/Products/MOSFETs/TO247/C2M0025120D, consulted on 2014-10-10.

[75] Y. Tang, J. Fedison, and T. Chow, "An implanted-emitter 4h-sic bipolar transistor with high current gain," *Electron Device Letters, IEEE*, vol. 22, pp. 119–120, March 2001.

[76] C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, and P. Mattavelli, "Characterization and comparison of 1.2 kv sic power semiconductor devices," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, pp. 1–10, Sept 2013.

[77] J. Wang and B. Williams, "Evaluation of high-voltage 4h-sic switching devices," *Electron Devices, IEEE Transactions on*, vol. 46, pp. 589–597, Mar 1999.

[78] CREE, "Cree announces volume production of second-generation sic mosfet, bringing significant cost savings to power-conversion systems," 2013, www.cree.com/News-and-Events/, consulted on 2014-10-10.

[79] Y. Shen, J. Jiang, Y. Xiong, Y. Deng, X. He, and Z. Zeng, "Parasitic inductance effects on the switching loss measurement of power semiconductor devices," in *Industrial Electronics, 2006 IEEE International Symposium on*, vol. 2, pp. 847–852, July 2006.

[80] N. Locci, F. Mocci, and M. Tosi, "Measurement of instantaneous losses in switching power devices," *Instrumentation and Measurement, IEEE Transactions on*, vol. 37, pp. 541–546, Dec 1988.

[81] R. Pittini, S. D'Arco, M. Hernes, and A. Petterteig, "Thermal stress analysis of igbt modules in vscs for pmsg in large offshore wind energy conversion systems," in *Power Electronics and Applications (EPE 2011), Proceedings of the 2011-14th European Conference on*, pp. 1–10, Aug 2011.

[82] S. Round, M. Heldwein, J. Kolar, I. Hofsajer, and P. Friedrichs, "A sic jfet driver for a 5 kw, 150 khz three-phase pwm converter," in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, vol. 1, pp. 410–416 Vol. 1, Oct 2005.

[83] E. Amoiralis, M. Tsili, and A. Kladas, "Transformer design and optimization: A literature survey," *Power Delivery, IEEE Transactions on*, vol. 24, pp. 1999–2024, Oct 2009.

[84] S. Tang, S. Hui, and H.-H. Chung, "Coreless printed circuit board (pcb) transformers with multiple secondary windings for complementary gate drive circuits," *Power Electronics, IEEE Transactions on*, vol. 14, pp. 431–437, May 1999.

[85] W. Chen, Y. Yan, Y. Hu, and Q. Lu, "Model and design of pcb parallel winding for planar transformer," *Magnetics, IEEE Transactions on*, vol. 39, pp. 3202–3204, Sept 2003.

[86] I. Josifovic, J. Popovic-Gerber, and J. Ferreira, "A pcb system integration concept for power electronics," in *Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International*, pp. 756–762, May 2009.

[87] Z. Ouyang and M. Andersen, "Overview of planar magnetic technology fundamental properties," *Power Electronics, IEEE Transactions on*, vol. 29, pp. 4888–4900, Sept 2014.

[88] P. Group, "Planar transformers and inductors size 5000," 2014, http://www.paytongroup.com/, consulted on 2014-10-13.

[89] C. Quinn, K. Rinne, T. O'Donnell, M. Duffy, and C. Mathuna, "A review of planar magnetic techniques and technologies," in *Applied Power Electronics Conference and Exposition, 2001. APEC 2001. Sixteenth Annual IEEE*, vol. 2, pp. 1175–1183 vol.2, 2001.

[90] V. Power, "Vi chip bcm bus converter family," 2014, www.vicorpower.com, consulted on 2014-10-13.

[91] M. Quirke, J. Barrett, and M. Hayes, "Planar magnetic component technology-a review," *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on*, vol. 15, pp. 884–892, Oct 1992.

[92] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics, Chapeter 15.* Boulder, USA: Springer, 2001.

[93] N. R. Coonrod, "Transformer computer design aid for higher frequency switching power supplies," *Power Electronics, IEEE Transactions on*, vol. PE-1, pp. 248–256, Oct 1986.

[94] J. Biela, U. Badstuebner, and J. Kolar, "Design of a 5-kw, 1-u, 10-kw/dm3 resonant dc-dc converter for telecom applications," *Power Electronics, IEEE Transactions on*, vol. 24, pp. 1701–1710, July 2009.

[95] J. Muhlethaler, J. Kolar, and A. Ecklebe, "Loss modeling of inductive components employed in power electronic systems," in *Power Electronics and ECCE Asia (ICPE ECCE), 2011 IEEE 8th International Conference on*, pp. 945–952, May 2011.

[96] P. Dowell, "Effects of eddy currents in transformer windings," *Electrical Engineers, Proceedings of the Institution of*, vol. 113, pp. 1387–1394, August 1966.

[97] W. Roshen, "Fringing field formulas and winding loss due to an air gap," *Magnetics, IEEE Transactions on*, vol. 43, pp. 3387–3394, Aug 2007.

[98] W. Roshen, "High-frequency fringing fields loss in thick rectangular and round wire windings," *Magnetics, IEEE Transactions on*, vol. 44, pp. 2396–2401, Oct 2008.

[99] M. Youssef and P. Jain, "A cost effective magnetic design for a 900 khz high frequency voltage regulator module: analysis and experimentation," in *Electrical and Computer Engineering, 2005. Canadian Conference on*, pp. 1496–1500, May 2005.

[100] G. Bertotti, "General properties of power losses in soft ferromagnetic materials," *Magnetics, IEEE Transactions on*, vol. 24, pp. 621–630, Jan 1988.

[101] W. Roshen, "A practical, accurate and very general core loss model for nonsinusoidal waveforms," *Power Electronics, IEEE Transactions on*, vol. 22, pp. 30–40, Jan 2007.

[102] R. Pry and C. Bean, "Calculation of the energy loss in magnetic sheet materials using a domain model," *Journal of Applied Physics*, vol. 29, pp. 532–533, Mar 1958.

[103] J. Reinert, A. Brockmeyer, and R. De Doncker, "Calculation of losses in ferro- and ferrimagnetic materials based on the modified steinmetz equation," *Industry Applications, IEEE Transactions on*, vol. 37, pp. 1055–1061, Jul 2001.

[104] K. Venkatachalam, C. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only steinmetz parameters," in *Computers in Power Electronics, 2002. Proceedings. 2002 IEEE Workshop on*, pp. 36–41, June 2002.

[105] J. Muhlethaler, J. Biela, J. Kolar, and A. Ecklebe, "Improved core-loss calculation for magnetic components employed in power electronic systems," *Power Electronics, IEEE Transactions on*, vol. 27, pp. 964–973, Feb 2012.

[106] Z. Ouyang, O. Thomsen, and M. Andersen, "Optimal design and tradeoffs analysis for planar transformer in high power dc-dc converters," in *Power Electronics Conference (IPEC), 2010 International*, pp. 3166–3173, June 2010.

[107] B. Cougo and J. Kolar, "Integration of leakage inductance in tape wound core transformers for dual active bridge converters," in *Integrated Power Electronics Systems (CIPS), 2012 7th International Conference on*, pp. 1–6, March 2012.

[108] G. Guidi, M. Pavlovsky, A. Kawamura, T. Imakubo, and Y. Sasaki, "Improvement of light load efficiency of dual active bridge dc-dc converter by using dual

leakage transformer and variable frequency," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, pp. 830–837, Sept 2010.

[109] Z. Ouyang, O. Thomsen, and M. A. E. Andersen, "The analysis and comparison of leakage inductance in different winding arrangements for planar transformer," in *Power Electronics and Drive Systems, 2009. PEDS 2009. International Conference on*, pp. 1143–1148, Nov 2009.

[110] P. Kong and F. Lee, "Transformer structure and its effects on common mode emi noise in isolated power converters," in *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, pp. 1424–1429, Feb 2010.

[111] D. Fu, S. Wang, P. Kong, F. Lee, and D. Huang, "Novel techniques to suppress the common-mode emi noise caused by transformer parasitic capacitances in dc-dc converters," *Industrial Electronics, IEEE Transactions on*, vol. 60, pp. 4968–4977, Nov 2013.

[112] J. Biela and J. Kolar, "Using transformer parasitics for resonant converters - a review of the calculation of the stray capacitance of transformers," in *Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005*, vol. 3, pp. 1868–1875 Vol. 3, Oct 2005.

[113] Magnetics, "Ferrite shapes and materials," 2014, http://www.mag-inc.com, consulted on 2014-10-14.

[114] Ferroxcube, "Ferrite shapes," 2014, http://www.ferroxcube.com//, consulted on 2014-10-14.

[115] J. Wilson, T.G., E. Whelan, R. Rodriguez, and J. Dishman, "Dc-to-dc converter power-train optimization for maximum efficiency," *Aerospace and Electronic Systems, IEEE Transactions on*, vol. AES-19, pp. 413–427, May 1983.

[116] F. Jauch and J. Biela, "Generalized modeling and optimization of a bidirectional dual active bridge dc-dc converter including frequency variation," in *Power Electronics Conference (IPEC-Hiroshima 2014 - ECCE-ASIA), 2014 International*, pp. 1788–1795, May 2014.

[117] H. Tamaki, H. Kita, and S. Kobayashi, "Multi-objective optimization by genetic algorithms: a review," in *Evolutionary Computation, 1996., Proceedings of IEEE International Conference on*, pp. 517–522, May 1996.

[118] C. Chew and S. Rama Rao Kondapalli, "Modeling, analysis, simulation and design optimization (genetic algorithm) of dc-dc converter for uninterruptible power supply applications," in *Power Electronics and Drives Systems, 2005. PEDS 2005. International Conference on*, vol. 2, pp. 1530–1535, Nov 2005.

[119] N. Mohan, *Power Electronics: A First Course.* Wiley, 2011.

[120] J. Kolar, J. Biela, and J. Minibock, "Exploring the pareto front of multi-objective single-phase pfc rectifier design optimization - 99.2efficiency vs. 7kw/din3 power density," in *Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International*, pp. 1–21, May 2009.

[121] R. Burkart and J. Kolar, "Comparative evaluation of sic and si pv inverter systems based on power density and efficiency as indicators of initial cost and operating revenue," in *Control and Modeling for Power Electronics (COMPEL), 2013 IEEE 14th Workshop on*, pp. 1–6, June 2013.

[122] D. Gautam, D. Wager, F. Musavi, M. Edington, W. Eberle, and W. Dunford, "A review of thermal management in power converters with thermal vias," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, pp. 627–632, March 2013.

[123] J. Lutz, "Igbt-modules: Design for reliability," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, pp. 1–3, Sept 2009.

[124] T. Anzawa, Q. Yu, M. Yamagiwa, T. Shibutani, and M. Shiratori, "Power cycle fatigue reliability evaluation for power device using coupled electrical-thermal-mechanical analysis," in *Thermal and Thermomechanical Phenomena in Electronic Systems, 2008. ITHERM 2008. 11th Intersociety Conference on*, pp. 815–821, May 2008.

[125] A. Hensler, J. Lutz, M. Thoben, and K. Guth, "First power cycling results of improved packaging technologies for hybrid electrical vehicle applications," in *Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on*, pp. 1–5, March 2010.

[126] V. Smet, F. Forest, J. Huselstein, A. Rashed, and F. Richardeau, "Evaluation of vrm ce monitoring as a real-time method to estimate aging of bond wire-igbt modules stressed by power cycling," *Industrial Electronics, IEEE Transactions on*, vol. 60, pp. 2760–2770, July 2013.

[127] A. Kosonen, L. Aarniovuori, J. Pyrhonen, M. Niemela, and J. Backman, "Calorimetric concept for measurement of power losses up to 2 kw in electric drives," *Electric Power Applications, IET*, vol. 7, pp. 453–461, July 2013.

[128] D. Christen, U. Badstuebner, J. Biela, and J. Kolar, "Calorimetric power loss measurement for highly efficient converters," in *Power Electronics Conference (IPEC), 2010 International*, pp. 1438–1445, June 2010.

[129] W. Yu, H. Qian, and J.-S. Lai, "Design of high-efficiency bidirectional dc-dc converter and high-precision efficiency measurement," *Power Electronics, IEEE Transactions on*, vol. 25, pp. 650–658, March 2010.

Appendix A

A review and design of power electronics converters for fuel cell hybrid system applications

Technoport 2012 - Renewable Energy Research Conference (RERC 2012)

Available online at www.sciencedirect.com

ScienceDirect

Energy Procedia 00 (2011) 000–000

Energy Procedia

www.elsevier.com/locate/procedia

Technoport RERC Research

A review and design of power electronics converters for fuel cell hybrid system applications

Zhe Zhang*, Riccardo Pittini, Michael A. E. Andersen and Ole C. Thomsen

Department of Electrical Engineering, Technical University of Denmark, Ørsteds Plads Building 349, 2800 Kgs. Lyngby, Denmark

Abstract

This paper presents an overview of most promising power electronics topologies for a fuel cell hybrid power conversion system which can be utilized in many applications such as hybrid electrical vehicles (HEV), distributed generations (DG) and uninterruptible-power-supply (UPS) systems. Then, a multiple-input power conversion system including a decoupled dual-input converter and a three-phase neutral-point-clamped (NPC) inverter is proposed. The system can operate in both stand-alone and grid-connected modes. Simulation and experimental results are provided to show the feasibility of the proposed system and the effectiveness of the control methods.

Keywords: Fuel cells, electrolysis cell, super-capacitors, converter, inverter, control.

1. Introduction

Sustainable energy is the main driving force for all renewable energy sources applications. Due their nature, energy supply from renewable energy sources is fluctuating depending on the availability of the energy source. Availability of the energy sources is mostly unpredictable (e.g. wind energy, solar energy, etc.) therefore, it is essential to have other energy sources that are more predictable to guarantee energy availability during periods of low energy supply from renewable sources. During period of energy surplus it is advantageous to store energy and make it available during the periods of low energy production and high energy demand. An efficient and high density way of storing energy is to produce fuel to accumulate the energy surplus.

* Corresponding author. Tel.: +45 45253486; Fax: +45 45880117.
E-mail address: zz@elektro.dtu.dk.

According to the energy strategy by the Danish government "A visionary Danish energy policy" published on January 2007, the goal is that wind energy should contribute for 50% of the national electricity consumption by 2025 [1]. Large scale integration of wind power and other renewable energy sources will require the development of a suitable grid infrastructure for handling the variability of the generation and load conditions. During periods of high wind the energy surplus from the wind parks is required to be stored or redirected towards other loads in order to avoid wasting precious energy. Large scale integration of solid oxide electrolysis cells (SOECs) and solid oxide fuels cells (SOFCs) based systems represent and attractive solution for handling energy surplus and pitfalls.

SOEC and SOFC operate at high temperatures nearly ~1000°C, compared to other fuel cell technologies (e.g. proton exchange membrane fuel cells, PEM FCs) SOFCs are made of hard solid materials which allow the cell to have different shape and not being limited to a flat plane structure. One of the main advantages of operating at such high temperatures is that there is no need for precious-metal catalyst reducing the costs. Moreover the SO cells can run on a variety of fuels including hydrocarbons; a major advantage is that pure hydrogen is not required however, since the main reactions involved require hydrogen, the fuel must contain hydrogen atoms.

Fuel cells can be operated in reversed mode with reduced efficiency; this type of cells are known as regenerative fuel cells and the main drawback of this reversibility comes from the low efficiency. This is the main reason why SOFC and SOEC systems for generating and storing energy are mostly based on independent fuel cell and electrolyser [2]. One of the main drawbacks of operating at such high temperature is the long thermal ramp-up required for the cell to avoid damage (due to thermal strains) to the cells.

In newly developments SOEC/SOFC have been allowed to operate at more manageable temperatures (<~800°C) allowing using common metallic materials (such as stainless steel) allowing reducing manufacturing cost and increasing reliability of the cell stacks. Operating at high temperatures allows SOEC/SOFC to have very high efficiency [3-4]; for this reason SOEC/SOFC systems are becoming more and more interesting as energy storage and energy source.

Power electronics converters, as the interfacing circuits between renewable energy sources, storage elements, utility grid and customers, have been more and more important for power control, energy saving and system reliability. Integration of power electronic converters as interface for fuel cell (FC) and electrolyser cell (EC) based systems with the grid introduces new challenging issues related to the slow cell dynamics and transient response, therefore, hybrid generation systems are required for obtaining fast transient response. Additional energy storage elements, such as battery and super capacitor banks, are expected to be a core element for increasing the system dynamic performance. Efficient energy management and control of the system power flows in the various system components is a key point for system performance. The highest reported efficiency for a fuel cell converter is up to ~98% [5] however, no previous research has been found on bi-directional FC/EC applications. In such applications where wide input voltage and high current are required, very high efficiency DC-DC conversion remains a challenge [6]. Novel power semiconductor devices based on silicon carbide (SiC), gallium nitride (GaN), advanced magnetic components and magnetic material could provide a significant difference.

Hereby, a diagram block to demonstrate the hybrid generation system based on fuel cell, super capacitor and battery system is presented in Fig. 1.

2. Power Electronics Converters for Fuel Cell Hybrid Energy Systems

According to the characteristics of the distributed generation systems based on the fuel cells, interface converters are necessary to boost the low variable voltage from the fuel cells and other auxiliary power sources (APS) such as batteries and super-capacitors, in order to provide the high quality, regulated dc

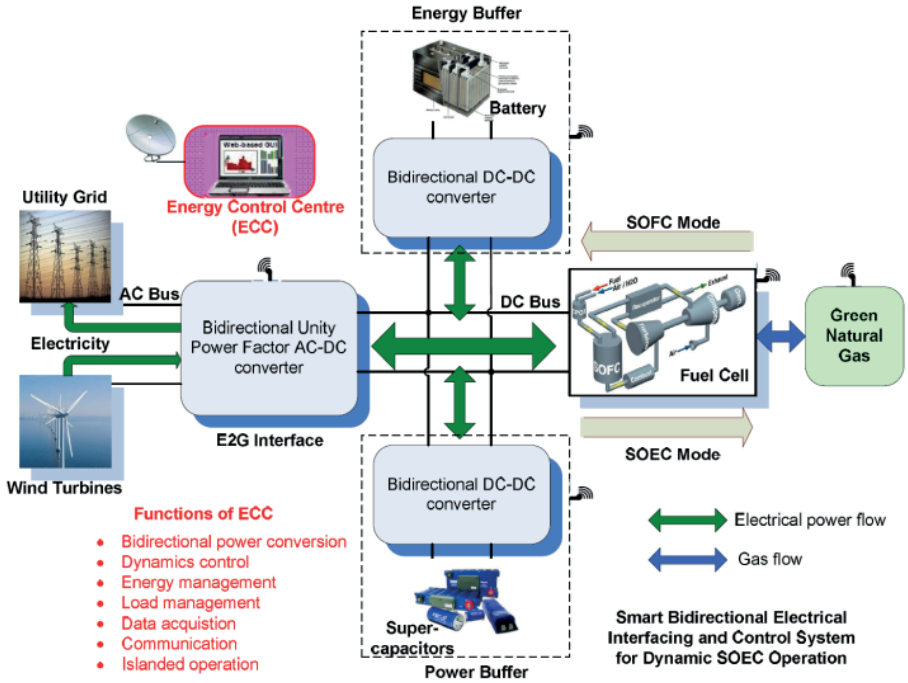


Fig. 1. Block diagram of a fuel cell battery and super-capacitor powered line-interactive renewable generation system.

voltage to the cascaded inverter for grid-connecting purposes. Hence, a large number of alternative converter topologies and implementations for low voltage high power applications have been proposed [5], [7]-[8].

2.1. DC-DC converters

Basically, DC-DC converters can be divided into two categories depending on using the galvanic insulation or not: non-isolated converter or isolated converter. As to the non-isolated converters, normally, boost-type converters are favourable to fuel cell application [9]. These topologies are simple, but they require a bulky input inductor to limit the current ripple in the components, especially with high voltage gains are required. To minimize the input inductor size and the current ripple, as well as to reduce the switch current stress, the converter can be designed with multiple legs interleaving each other by means of the input coupling inductors, and high efficiency can be obtained. For isolated DC-DC converters, in [5], the low voltage high power isolated converters have been overviewed and compared very well. The high efficiency full-bridge boost type fuel cell converter without any auxiliary snubber circuit is designed in [10]. Moreover, a novel parallel method is proposed in [11] to increase the power level to 10 kW. Summarily, as with typical designs, tradeoffs exist in choosing the optimum DC-DC converter, so the designers must establish the exact requirements of the fuel cell system in question to determine the most advantageous design.

As for the interfacing circuits of APS, generally, bidirectional DC-DC converters are needed. Theoretically, all the isolated unidirectional DC-DC converters overviewed in [5] and [7] can achieve bidirectional power delivering ability, through changing the diode-rectifiers to synchronized rectifiers which are based on gate-controlled semiconductors, such as MOSFETs or IGBTs.

2.2. Hybrid DC-DC conversion systems

The block diagrams of the widely utilized DC-DC hybrid systems with FCs and APS are summarized in Fig. 2 (a) and (e) [12]. In Fig. 2 (a) and (b), the DC bus is fixed by the fuel cell or by the APS [13]. In this case, the main advantage is related with the fact that the current flows through APSs only during the transients, enlarging the lifetime of the APS. The critical disadvantage is that the usual dc bus conditions impose that the DC voltage cannot vary strongly. In Fig. 2 (c), only one power converter is used. The main characteristic of this direct connection is that both elements, the fuel cell and the APS, share the same voltage value. This will reduce the weight and will increase the reliability of the system. But it is difficult to control the fuel cell current flexibly [14]. Fig. 2 (d) and (e) show the block diagrams of the two voltage source power conversion system with two individual DC-DC converters, and hereby the two input power sources are decoupled completely. While, obviously, the cost and complexity of the whole system are increased [15].

Hence, in terms of system cost, complexity, fuel cell protection, super-capacitor management, load peaking capability and parameter matching, the different structures analyzed above are compared in the spider plot as shown in Fig. 2 (f).

In order to simplify the hybrid power conversion system and reduce the system cost, the multiple-input DC-DC converters can be used. The input voltage sources or current sources (voltage source cascaded with large inductance) can be connected either in series or in parallel for the DC-DC converters to transfer the desired power to the load. Furthermore, some parts of the DC-DC converter (such as filter or rectifier) can be shared by different input sources, so it has the potential to achieve higher power density [16], [17].

2.3. DC-AC inverters

The DC/AC converter technology is mature and uses mainly the hard-switching voltage source inverter (VSI), with single-phase, dual-phase or three-phase output, controlled by means of sinusoidal pulse-width-modulation (SPWM) or space vector PWM (SVPWM) [18]. Multilevel voltage-source

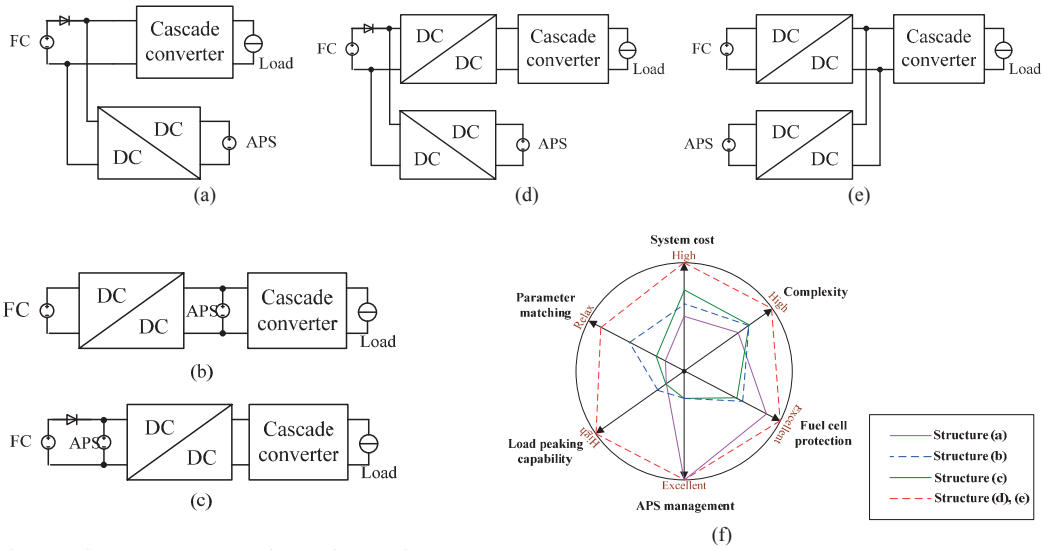


Fig. 2. Various converter connections and comparison.

inverters [19] provide a cost effective solution in the medium voltage energy management market. Nowadays, there exist three commercial topologies of multilevel voltage-source inverters: neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitors (FCs). Among the high-power converters, the NPC inverter introduced 25 years ago is the most widely used in all types of industrial applications, such as wind power generation, UPS and so on, in the medium and high voltage range.

3. Proposed topology and System Design

The authors and other researchers from the Electronics Group, Technical University of Denmark (DTU), have given many contributions on analysis and design of the fuel cell converters. Based on our research results in this topic, a dual-input two-stage power conversion system, including DC-DC and DC-AC is proposed, analyzed and verified in this paper.

3.1. The proposed hybrid power conversion system

The topology of the proposed fuel cell hybrid power conversion system is shown in Fig. 3. A fuel cell is used as the primary source and an APS (supercapacitor or battery) is employed as the transient energy storage. The dual-input DC-DC converter interfaces the fuel cell and the APS to the three-phase NPC inverter and manages the power flow in the system. The inverter output can be connected to the grid or the local loads depending on the grid condition.

Unlike conventional power converters, this new DC-DC stage for a fuel-cell power conditioning system has two power inputs. In this paper, the dual-input isolated boost converter [20] was chosen. The converter topology consists of four individual and uniform transformers and four bridges. The topology is bidirectional due to the active rectifier bridge on the secondary side. In addition to galvanic isolation, this converter can easily match the different voltage levels at the ports. Moreover, the two input ports are decoupled completely by the phase-shift PWM modulation strategy. Based on the modeling of the proposed dc converter, the control scheme can be designed for the DC-DC stage which aims to simultaneously regulate the dc-link voltage and the fuel-cell power with two bridge duty cycles as control variables. The APS sinks/sources the power difference between the inverter and the fuel cell to keep the power of fuel cell constant and match the variations of the power drawn by the inverter [21].

A three-phase voltage source NPC inverter is used for dc-ac power conversion and grid interfacing. The main function of the inverter is to maintain a regulated output voltage when operating in stand-alone mode, and when operating in grid-connected mode, to inject an optional real power as well as reactive and harmonic current into the grid. Because of the boost function in the DC-DC stage, low-voltage fuel cell and energy-storage devices as APS can be utilized in the whole system. A new SPWM modulation strategy based on the circuit-level decoupling algorithm is employed in the NPC inverter. This modulation scheme can not only simplify the closed-loop controller design but also reduce the switching losses [22].

3.2. Simulation analysis and experimental results

The proposed topology is simulated by Simulink/PLECS where a supercapacitor (SC) bank is used as the APS, and simulation parameters are listed in Table 1. Fig. 4 shows relevant waveforms in different operating conditions. During T1, the fuel cells are in warm-up stage and have no output power, so the load is fully powered by the SC bank. The fuel cells start to provide the power and recharge SC bank in T2 in which the bidirectionality of the proposed converter structure can be shown clearly. During T3, the power of fuel cells is constant and the voltage of SC bank is increasing slowly. The load response of the

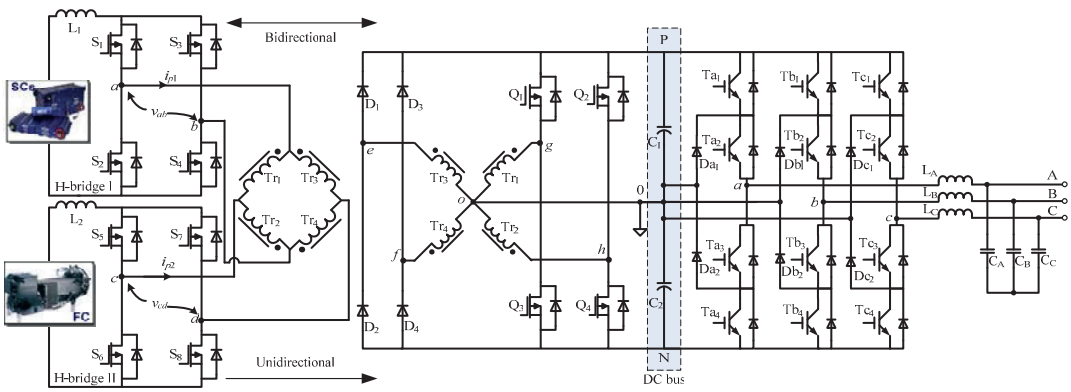


Fig. 3. Proposed DC-DC-DC-AC dual input power conversion system.

system is presented in the subinterval of T4 and the transient power is fully taken over by the SC bank rather than the fuel cells.

In order to verify the theoretical analysis, a laboratory prototype of the proposed topology is implemented and tested. The specifications and component details of the tested prototype are given in Table 2.

Table 1. Parameters in the simulation

Name of the Parameters	Value
Fuel cell voltage	50 V DC
SC bank voltage	100 V DC
Dc-link voltage	400 V DC
Output ac voltage	120 VAC
Output power	1000 W

Table 2. Specifications and component details of the tested prototype

Rated input voltage, V1 and V2	30 – 60 VDC
Rated output voltage, Vo	400 VDC
Rated output power, Po	2 kW
Switching frequency of DC-DC converter	50 kHz
Boost inductors, L_1 and L_2	22 µH, N87 ferrite core, copper foil winding
Dc-link film capacitor	6.8 µF/250V Film Cap: 4 in parallel
Dc-link electrolytic capacitor	2820 µF
MOSFETs S_1-S_8	IRFP4568, 150V/171A
Diodes D_1-D_4	HFA15TB60, 600V/15A
Ac output filters	L_A=L_B=L_C=120 μH, C_A=C_B=C_C=40 μF
Switching frequency of NPC inverter	20 kHz
IGBT Ta1-Tc4	600 V/40 A

Fig. 5(a) shows the experimental waveforms of the voltages $v_{ab\text{-}DC}$ and $v_{cd\text{-}DC}$ as well as the currents i_{p1} and i_{p2} on the primary side of the DC-DC stage, as denoted in Fig. 3, under the dual-input mode with input voltages of 50 V and 30 V. Fig. 5(b) shows the output voltage response to transients of the two input currents. A small super-capacitor bank (60 V / 14.6 F) is used as input source V_{g2} and then the experimental waveforms can be obtained and present in Fig. 5(c). At t_0, the converter starts and i_{ref1} is 0, which is to simulate the warm-up stage of the primary power source V_{g1}, so converter operates under single-input mode. The required load power is provided by super-capacitor bank and output voltage keeps constant; after t_1, i_{ref1} is given according to voltage of V_{g1} and the required output power, and thereby i_{g2} starts to reduce until it reaches zero at t_2.

Fig. 6(a)-(c) show the experimental waveforms obtained on the NPC inverter with the circuit-level decoupling SPWM modulation strategy. The converter three phase line output voltage after the PWM filter is shown on Fig. 6(a); Fig. 6(b) shows the output PWM phase voltage and Fig. 6(c) the output PWM line to line voltage.

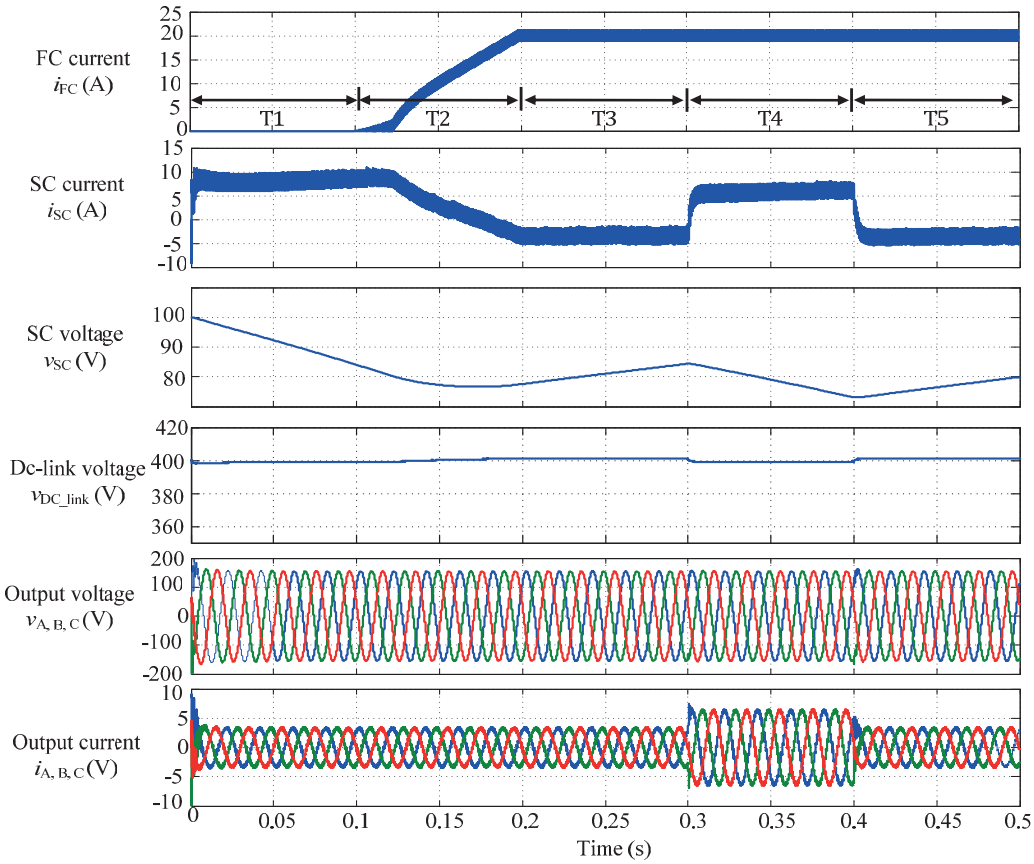


Fig. 4. Simulation results: fuel cell warm-up (T1), fuel cell transient period (T2), SC recharging (T3 and T5) and load disturbance (T4).

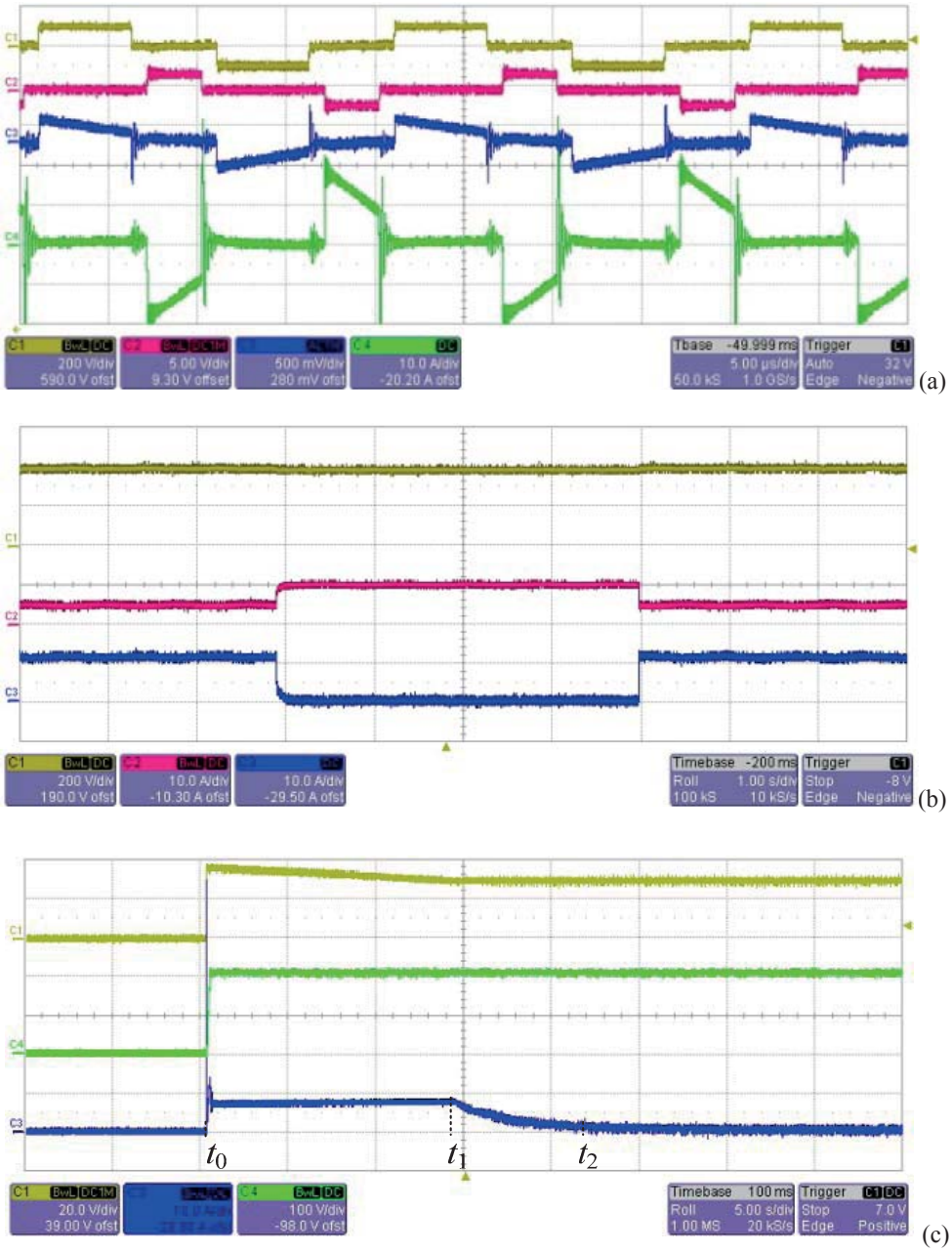


Fig. 5: Experimental results: (a) Ch1: vab-DC [200 V/div], Ch2: vcd-DC [250 V/div], Ch3: ip1 [10 A/div], Ch4: ip2 [10 A/div]. (Time base: 5 µS/div); (b) Transient response with respect to the input current disturbances under conditions: Vg1=50V, Vg2=30V. Ch1: vo-DC [200 V/div], Ch2: ig1 [10 A/div], Ch3: ig1 [10 A/div]. (Time base: 1s/div); (c) Transient period, Ch1: vg2 [20 V/div], Ch3: ig2 [10 A/div], Ch4: ouput volage vo-DC [100 V/div]. (Time base: 5s/div).

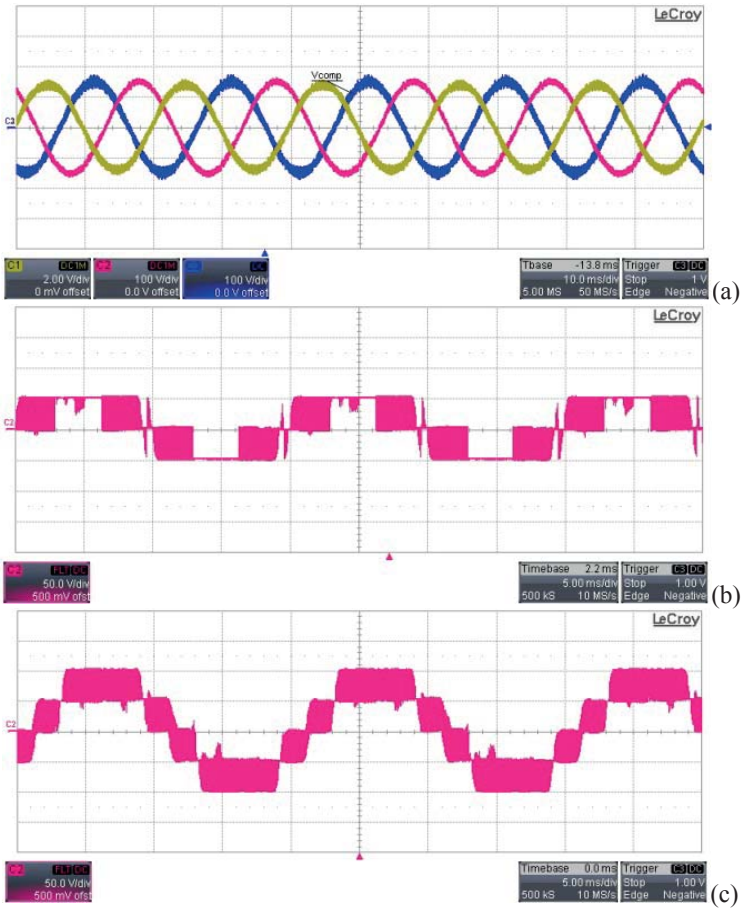


Fig. 6. Experimental results: (a) three-phase output voltage, vAO, vBO and vCO (10 ms/div); (b) switched waveform for phase voltage vaO (5 ms/div), and (c) switched waveform for line to line voltage, vl-l-ab (5 ms/div).

4. Conclusions

In this paper, an overview of power electronics converters and inverters for fuel cell hybrid power conversion system is given. Based on the previous research carried out at Electronics Group, Technical University of Denmark (DTU), a topology proposed here is composed of a dual-input DC-DC converter and three-level NPC inverter. The system can operate in both the stand-alone and grid-connected modes providing fast dynamic response and high efficiency. The benefits of using super-capacitors have been shown clearly in the improved transient response compared to a system with no energy storage elements. Further research will analyse hybrid energy storage solutions with three or more in converter ports.

References

[1] Zhao Xu; Gordon, M.; Lind, M.; Ostergaard, J.; , "Towards a Danish power system with 50% wind — Smart grids activities in Denmark," Power & Energy Society General Meeting, 2009. PES '09. IEEE , pp.1-8, 26-30 July 2009.

[2] P. Iora, M.A.A. Taher, P. Chiesa, N.P. Brandon, "A novel system for the production of pure hydrogen from natural gas based on solid oxide fuel cell-solid oxide electrolyzer", International Journal of Hydrogen Energy, Vol. 35, no. 22, pp. 12680-12687, 2010.

[3] W. Donitz, E. Erdle, "High-Temperature Electrolysis of Water Vapour – Status of Development and Perspectives for Application", International Journal of Hydrogen Energy, Vol. 10, no. 5, pp. 291-295, 1985.

[4] J. Hartvigsen, S. Elangovan, L. Frost, A. Nickens., C. Stoots, J. O'Brien, J. S. Herring, "Carbon Dioxide Recycling by High Temperature Co-Electrolysis and Hydrocarbon Synthesis", ECS Transactions, Vol. 12, Issue: 1, pp. 625-637, 2008.

[5] M. Nymand, "High efficiency power converter for low voltage high power application", PhD thesis, Technical University of Denmark, 2010.

[6] F. Krismer, J. Biela, J. W. Kolar, "A Comparative Evaluation of Isolated Bi-directional DC/DC Converters with Wide Input and Output Voltage Range", Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005 , vol.1, no., pp. 599- 606 Vol. 1, 2-6 Oct. 2005.

[7] P. Klimczak, "Modular power electronic converters in the power range 1 to 10 kW," PhD thesis, Aalborg University, 2009.

[8] P. Thounthong, B. Davat, S. Rael, and P. Sethakul, "Fuel cell high-power applications – An overview of power converters for a clean energy conversion technology," IEEE Industrial Electronics Magazine, vol. 3, no. 1, pp. 32-46, March 2009.

[9] M. Nymand, M. A. E. Andersen, "High-efficiency isolated boost DC-DC converter for high-power lowvoltage fuel cell applications," IEEE Transactions on Industrial Electronics, vol. 57, no. 2, pp. 505-514, Feb. 2010.

[10] M. Nymand, M. A. E. Andersen, "New primary-parallel boost converter for high-power high gain applications," in Proc. IEEE APEC, Washington, USA, 2009, pp. 35-39.

[11] M. Nymand, R. Tranberg, M. E. Madsen, U. K. Madawala, M. A. E. Andersen, "What is the best converter for low voltage fuel cell applications- A buck or boost?," in Proc. IEEE IECON, Porto, Portugal, 2009, pp. 959-964.

[12] Z. Zhang, "Powering the future data centre," PhD thesis, Technical University of Denmark, 2010.

[13] Z. Zhang, Z. Ouyang, O. C. Thomsen and M. A. E. Andersen, "Analysis and design of a Bidirectional isolated DC-DC converter for fuel cells and supercapacitors hybrid system," IEEE Transactions on Power Electronics, vol. 27, no. 2, pp. 848-859, Feb. 2012.

[14] Z. Zhang, O. C. Thomsen and M. A. E. Andersen, "Analysis and design of bi-directional DC-DC converter in extended run time DC UPS system based on fuel cell and supercapacitor," in Proc. IEEE 24th Annual Applied Power Electronics Conference and Exposition (APEC), pp.714-719. Feb. 2009.

[15] Z. Zhang, O. C. Thomsen and M. A. E. Andersen, "A two-stage DC-DC converter for the fuel cell-supercapacitor hybrid system," in Proc. IEEE Energy Conversion Congress and Exposition (ECCE), pp. 1425-1431, Sept. 2009.

[16] H. Tao, A. Kotsopoulos, J. L. Duarte and M. A. M. Hendrix, "Family of multiport bidirectional DC–DC converters," IEE Proc.-Electrical Power Application, vol. 153, no.3, pp.451-458, 2006.

[17] Y. Li, X. Ruan, D. Yang, F. Liu and C. K. Tse, "Synthesis of multiple-input DC/DC converters," IEEE Trans. Power Electron., 2010, 25, (9), pp. 2372–2385.

[18] D. G. Holmes and T. A. Lipo, "Pulse width modulation for power converters," A John Wiley & Sons. ISBN: 0-471-20814-0, 2003.

[19] J. Rodriguez, J.-S. Lai, F. Z. Peng, "Multilevel inverters: a survey of topologies, control and applications," IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724-738, 2002.

[20] Z. Zhang, O. C. Thomsen, M. A. E. Andersen and H. R. Nielsen, "A novel dual-input isolated current-fed DC-DC converter for renewable energy system," in Proc. IEEE Applied Power Electronics Conf. and Exposition (APEC), 2011, pp. 1494-1501.

[21] Z. Zhang, O. C. Thomsen and M. A. E. Andersen, "Modeling and control of a dual-Input isolated full-bridge boost converter," in Proc. IEEE Applied Power Electronics Conf. and Exposition (APEC), 2012. (in press)

[22] Z. Zhang, O. C. Thomsen and M. A. E. Andersen "The circuit-level decoupling modulation scheme for three-level neutral-point-clamped inverter," in Proc. the 14th International European Conference on Power Electronics and Applications (EPE), 2010.

Appendix B

Analysis and Comparison on a Grid-Tie Fuel Cell Energy Storage System Based on Si and SiC Power Devices

IEEE International Power Electronics and Applications Conference and Exposition (PEAC 2014)

Analysis and Comparison on a Grid-Tie Fuel Cell Energy Storage System Based on Si and SiC Power Devices

Riccardo Pittini, Alexander Anthon, Zhe Zhang and Michael A.E. Andersen
Technical University of Denmark, Department of Electrical Engineering
Oersteds Plads 349, 2800 Kgs. Lyngby, Denmark
Email: ripit@elektro.dtu.dk, jant@elektro.dtu.dk, zz@elektro.dtu.dk, ma@elektro.dtu.dk

***Abstract*—In renewable energy applications power conversion efficiency is major concern. This is especially true for grid-tie energy storage systems based on bidirectional dc-dc and dc-ac converters where the power always flows through these system components. Latest developments in power semiconductors allowed to significantly reduce the switching and conduction losses in dc-dc and dc-ac converters. This paper analyzes the efficiency improvement that is achieved by the introduction of SiC power semiconductors in dc-dc and dc-ac converters used in fuel cell grid-tie energy storage systems. Results highlight dc-dc conversion efficiencies up to 98.2% with an isolated topology and dc-ac conversion efficiencies up to 97.7%. Overall system efficiency improvements above 1% are achieved compared to traditional Si devices. Efficiency improvements are analyzed based on two laboratory converter prototypes of an isolated full bridge boost converter (IFBBC) and a three level T-type inverter (BSNPC).**

I. Introduction

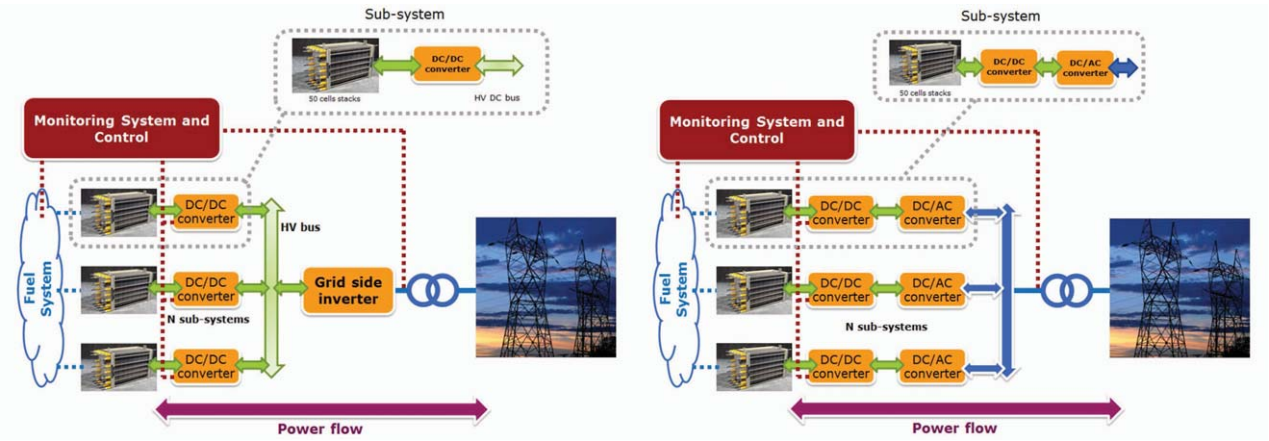
Energy produced from renewable energy sources is fluctuating depending on the availability of the energy source [1]. For this reason, grid-tie energy storage systems are expected to play an important role in the future energy systems. Different energy storage technologies are nowadays available, such as pumped hydro, compressed air systems, battery systems and other chemical-based processes. In these applications, bidirectional fuel cells represent a very attractive technology since they allow storing energy in a fuel form (high energy content) [2]. For all energy storage systems efficiency is an important aspect in power conversion especially in dc-dc converters and dc-ac inverters where power semiconductor devices are key components. Apart from different converter topologies, loss contributions are mainly determined by the choice of the power semiconductors. One way to increase efficiency in converters with voltage levels in the 600 V-1200 V range is to replace commonly used silicon (Si) devices with silicon carbide (SiC) devices [3].

The introduction of SiC Schottky diodes represented a first breakthrough for SiC technology. Even though SiC Schottky diodes are significantly more expensive compared to their equivalent Si devices, they have been widely employed in multi-kW power converters due to their nearly-zero reverse recovery current. Since then, SiC power semiconductors have become more attractive, more mature and more accessible. SiC MOSFETs have extremely low switching losses [4] compared to Si IGBTs which, whether possible, makes them the preferred power semiconductors over Si IGBTs. Their performance has been evaluated in previous work [5][6] however, it is always challenging to quantify the real expected efficiency increase without proper full power converter prototypes.

This paper presents the results achieved with dc-dc and dc-ac converters designed for an energy storage system based on bidirectional fuel cells. The designed converters have been characterized in efficiency terms with both Si IGBTs and SiC MOSFETs power semiconductors. Efficiencies achieved with the converter prototypes are presented and analyzed taking into account the entire system efficiency. Efficiency improvements up to 1% were achieved for the entire operating range of the system. While for the single converters, efficiencies improvements up to 1%-3% range were observed depending on the converter operating point.

II. Energy Storage System Based on Bidirectional Fuel Cells

Grid-tie energy storage systems require power conditioning units (both dc-dc and dc-ac) to process the energy to and from the grid. System topology is strongly influenced by the maturity of the candidate fuel cell technology and by the economic feasibility of the system. The fuel cell technology determines also the power conditioning unit operating conditions (I-V characteristics [7] for the dc-dc converters in Fig. 1a and 1b). The system topology and the dc-dc /dc-ac converters efficiency will strongly affect the overall system performance since both in power generation mode and power regeneration mode energy flows through the power conditioning units. In order to ensure long term system reliability and high efficiency it is desired to operate the cells stacks in optimal conditions in terms of cells current density, of temperature and fuel distribution. Therefore, a dc-dc converter is required for each cells stack. The system in Fig. 1a has a single dc-ac inverter unit which minimized the system complexity and cost. However, at light systems loads the overall system efficiency is limited by the light load efficiency of the inverter unit. The system in Fig. 1b can provide higher efficiency especially at light loads. In fact, light load efficiency of a large dc-ac converter is typically lower than the efficiency of a small



(a) Centralized inverter

(b) Distributed inverter

Fig. 1: SOEC/SOFC system topologies.

TABLE I: SOEC/SOFC cells and converter specifications

Specification	SOEC	SOFC	Converter
Voltage LV-side	50-80 V	30-50 V	30-80 V
Current LV-side	0-80 A	0-40 A	0-80 A
Power	0-6000 W	0-1500 W	0-6400 W
Power flow	⇐ from the grid	⇒ to the grid	⇔ bidirectional

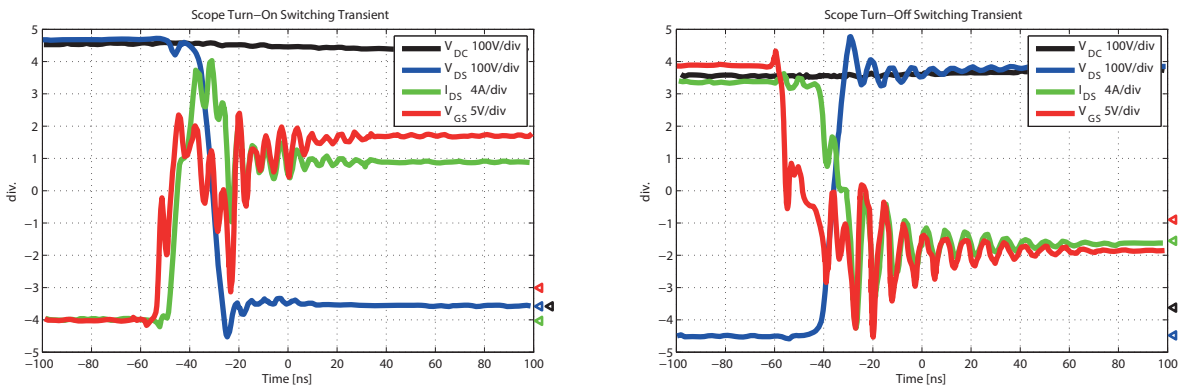
inverter unit operating in mid or high load conditions.

The analysis of the overall system efficiency is based on Fig. 1b system topology where a single sub-system is considered. The I-V characteristics of a 50 cells stack of bidirectional fuel cells is summarized in Table I. Multi-kW dc-dc and dc-ac converter prototypes have been established according to the characteristics of cells stack of solid oxide fuel cells /electrolyzer cells (SOFC /SOEC). The cells stack electric specifications determine the dc-dc converter characteristics, while the dc-ac inverter characteristics are determined by the grid specifications.

III. Si and SiC Power Devices

The introduction of SiC power semiconductors in dc-dc and dc-ac converters significantly increases the cost of the converter power devices. This increase has to be justified by an efficiency improvement or by a reduction of the cost of other converter components, such as magnetic and capacitive components.

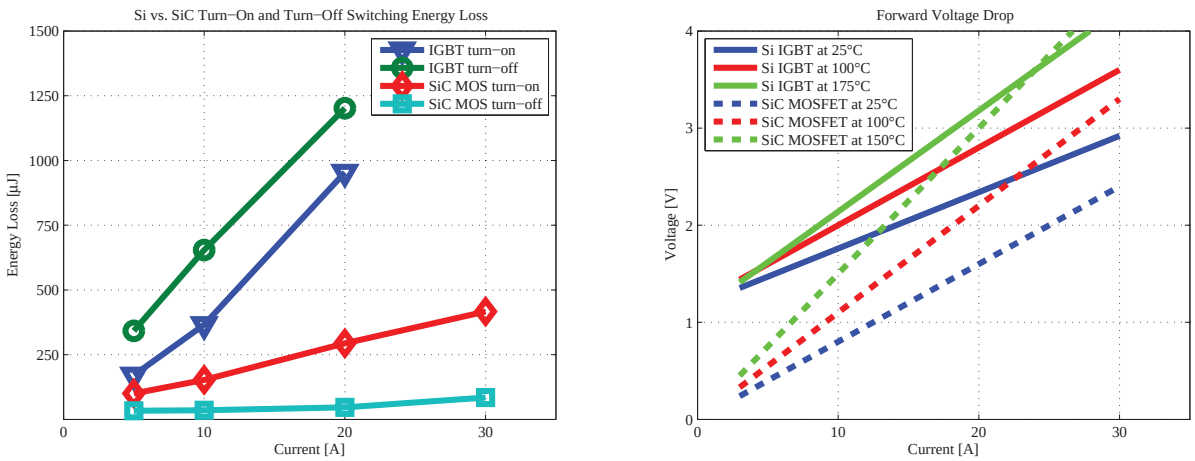
The investigation performed on Si IGBTs (IGW15N120H3 and IKW12N120T2) and SiC MOSFETs (Cree C2M0080120D and ST SCT30N120) considered both conduction and switching losses. Switching losses are the most challenging to model and to estimate, therefore, switching measurements based on double pulse test (DPT) has been performed. Switching waveforms for SiC MOSFET



(a) Turn-on

(b) Turn-off

Fig. 2: SiC MOSFET switching transients.



(a) Switching losses

(b) Conduction losses - Forward voltage drop

Fig. 3: Si IGBTs and SiC MOSFETs loss comparison

at 800 V and 20 A are presented in Fig. 2a for device turn-on and in Fig. 2b for device turn-off. Even though of the highly optimized layout, the devices have a strong tendency to gate oscillations due to the extremely high *dV/dt* and large package stray inductances (TO-247). A complete view of the reduction of switching losses achieved with SiC devices is shown in Fig. 3a. The largest reduction of switching losses is achieved at high current levels; in this case, the reduction can reach up to ∼80%. Even though the latest generations of Si IGBTs can operate with switching frequencies up to 100 kHz, the tail current gives a large contribute in the turn-off switching losses.

For both Si IGBTs and SiC MOSFETs the conduction losses can easily be characterized with information retrieved from the devices datasheets. The reduction of conduction losses achieved with SiC MOSFETs (C2M0080120D) over Si IGBTs (IGW15N120H3) is represented by the device forward voltage drop show in Fig. 3b. In this case the largest reduction is observed at low current levels where the IGBT forward voltage drops dominates. As the current increases the difference is progressively reduced by the higher on-state resistance of SiC MOSFETs compared to IGBTs. The gap between IGBTs and SiC MOSFETs is also reduced at high junction temperatures. In this case for both devices the on-state resistance increases however, for the IGBTs this is compensated also by the lower threshold voltage V_{T0} (bipolar behavior).

IV. Dc-dc Power Converter

The dc-dc converter in the system in Fig. 1a and 1b is designed based on an isolated full bridge boost converter (IFBBC) topology [8]. The converter prototype is shown in Fig. 4 where its main components are highlighted. The converter low-voltage side (30-80 V) power stage is based on Si MOSFETs (120 V 4.1 $m\Omega$ two devices in parallel for each switch of the full bridge) and is connected to the cells stack. The converter high voltage side (700-800 V) represents the dc-link bus for the dc-ac converter. The full bridge of the high voltage side of the dc-dc converter has been tested with Si IGBTs (IGW15N120H3) and with SiC MOSFETs (ST microelectronics SCT30N120 which are equivalent to Cree C2M0080120D). The dc-dc converter magnetic components are designed based on high current planar cores for an operating switching frequency of 40 kHz. The transformer cores

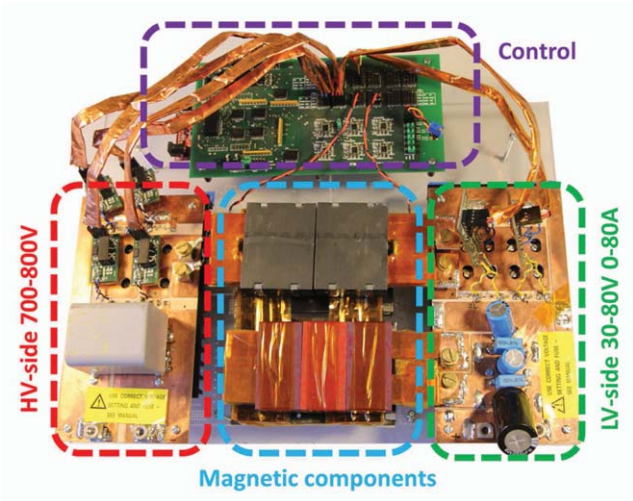
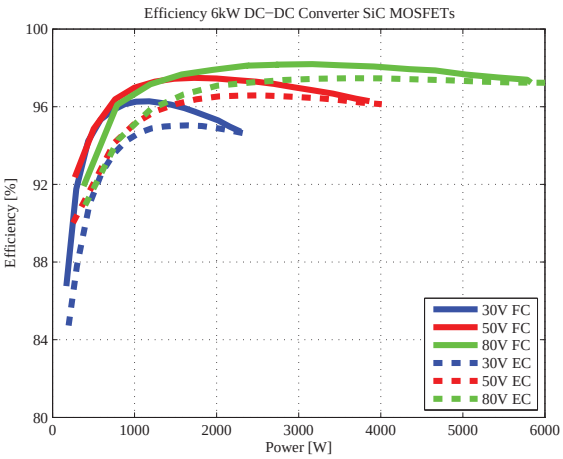
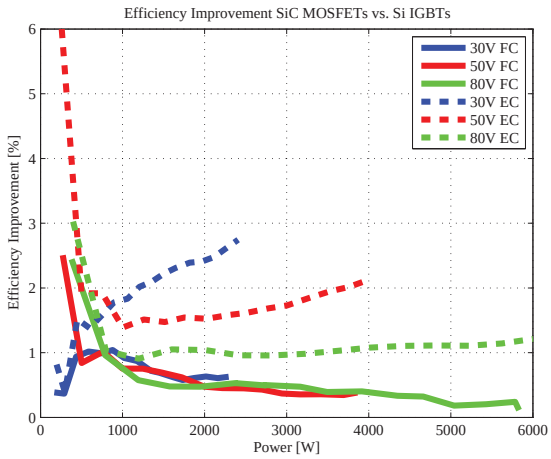


Fig. 4: 6 kW bidirectional isolated full bridge boost dc-dc converter. Highlighted its main components: low voltage side (LV-side), high voltage side (HV-side), control board, boost inductor and high frequency isolation transformer (magnetic components).



(a) Measured dc-dc converter efficiency with SiC MOSFETs, bidirectional power flow



(b) Dc-dc converter efficiency improvement

Fig. 5: Dc-dc converter efficiencies measured with Si IGBTs and with SiC MOSFETs.

are two E64 pairs in Magnetics R-type material while the boost inductor use three E6030 stacked core pairs in KoolMu material. The test setup for measuring the system efficiency is based on four $6\frac{1}{2}$ high precision multimeters synchronized and connected with a PC. Two multimeters measured the LV-side and the HV-side voltages while the other two measured the converter currents through calibrated precision shunt resistors. The absolute error on the measured efficiency is less than 0.1%.

The absolute dc-dc conversion efficiency of the converter based on SiC MOSFETs for both power flow directions is presented in Fig. 5a. In this case, the efficiency takes into account also the gate driver and the cooling losses. With SiC MOSFETs the dc-dc converter was just above 96% at 30 V on the converter LV-side and reached a peak of 98.2% at 80 V. Converter efficiency based on SiC MOSFETs is compared with the first converter prototype based on Si IGBTs in Fig. 5b.

The efficiency improvement is presented at 30 V, 50 V and 80 V, but it has been investigated for the entire converter operating range (30-80 V). A limited improvement is observed in fuel cell mode (FC-mode) in Fig. 5b (continuous lines). In this mode, the SiC MOSFETs are operating in active rectification; the efficiency improvement (monotonic function trend) is mostly noticeable at light converter loads and it slowly decreases at high power levels. At light loads, IGBTs antiparallel diodes have significant losses due to the forward voltage drop while SiC MOSFETs have only resistive voltage drop. For this reason, higher efficiency improvements are observed at converter light load. Large efficiency improvement is observed in electrolyzer cell mode (EC-mode) in Fig. 5b (dashed lines). In EC mode the high voltage power semiconductors are operating in hard switching conditions, therefore, the major improvement is given by the large difference in switching losses between the IGBTs and SiC MOSFETs switching losses [9]. The efficiency improvement is in the 1-3% range (dashed lines in Fig. 5b) with a peak at converter light load.

V. DC-AC Power Converter

The dc-ac converter is the second power stage in the conversion process. The dc-ac converter is designed as a 3 kW single phase low-power variant, the dc-link is specified as 700-800 V to comply a 230 V_{RMS} grid with a fundamental

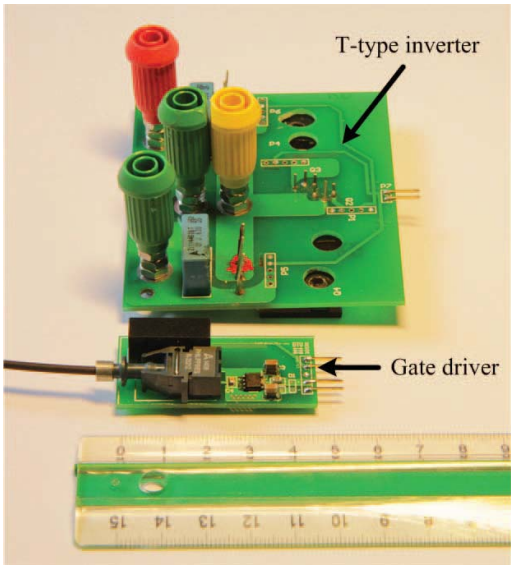


Fig. 6: 3 kW dc-ac inverter based on T-type (BSNPC) topology [11]. Heatsink is removed.

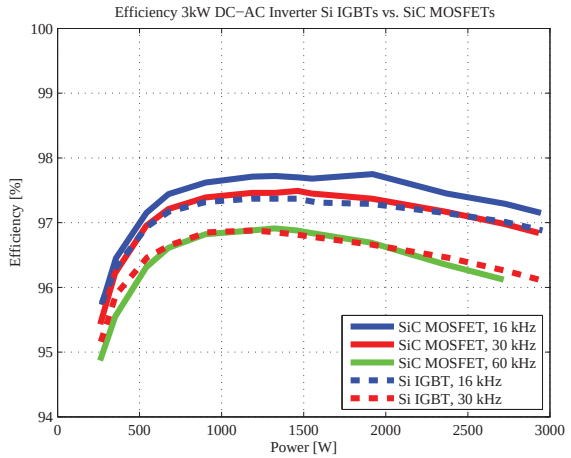


Fig. 7: Measured dc-ac converter efficiency comparison with Si IGBTs and SiC MOSFETs at 30 kHz and 60 kHz.

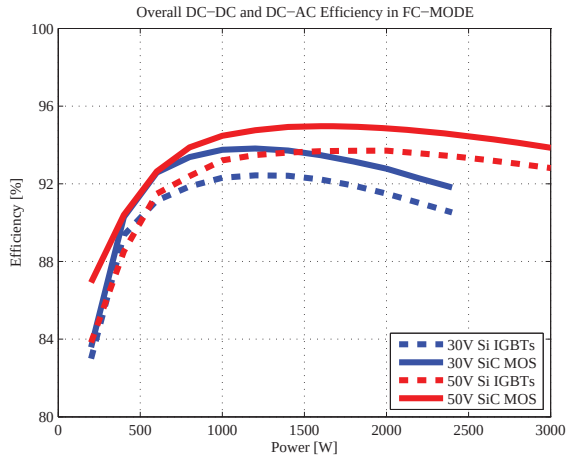


Fig. 8: Comparison of the total system efficiency with Si IGBTs and SiC MOSFETs when the system power flows from the fuel cells stack to the grid.

frequency of 50 Hz. Several different inverter topologies could be considered however, for low voltage grid, two- and three-level topologies are the most common ones due to their good trade-off between cost, complexity and efficiency. Multi-level topologies are mostly interesting because it is possible to reduce the size of filtering components [10].

A converter prototype of a 3 kW single phase T-type inverter [11] (also known as Conergy or BSNPC) has been developed and tested [12], shown in Fig. 6. The T-type inverter is a three level topology derived from the neutral point clamped (NPC) topology. The topology has the middle branch switches connected to the mid-point of the dc-link and they operate at the same frequency as the grid (50 Hz). For this horizontal branch, the conduction losses are dominating and the switching losses can be neglected. Devices employed in this branch are Si IGBTs (IKP15N60T) rated at 600 V. The vertical branch of the T-type single phase inverter has been tested with both Si 1200 V (IKW15N120T2) and with SiC MOSFETs (C2M0080120D). These are the high frequency devices of the dc-ac inverter, in this case the switching frequencies have been 16 kHz and 30 kHz for Si IGBTs and up to 60 kHz for SiC MOSFETs. In this case to measure the efficiency of the dc-ac converter a N4L PPA5500 power analyzer was used. The instrument has a basic accuracy of 0.01% and can measure harmonics up to 2 MHz.

Dc-ac conversion efficiencies are measured up to the nominal converter power with an LC output filter (3 mH, 4.4 µF). Results from the measurements are presented in Fig. 7 at different switching frequencies for both Si IGBTs and SiC MOSFETs. An overall, the adoption of SiC MOSFETs can provide an efficiency improvement of ∼0.8% for a major part of the converter operating range. This results that at 30 kHz at full converter power (3 kW) the total power semiconductor losses (conduction and switching) of the vertical leg are reduced by 72% and of the total converter power semiconductor losses by 70%. This efficiency improvement is mostly due to the reduction in switching losses rather than conduction losses [12]. This also allows reducing the size of the converter cooling system by a similar amount. From Fig. 7 it is also observed that with SiC MOSFETs it is possible to almost double the converter switching frequency and achieve a similar efficiency as achieved with Si IGBTs. This results that the size of the converter filtering components can be reduced.

VI. System Efficiency

The overall system efficiency is determined by the series efficiency of the dc-dc and dc-ac converter stages. From the system operating point, the fuel cell mode represents the most critical. In fact, in this mode the system provides power to the grid and the fuel cell efficiency is limited to ∼50%. The remaining power from the fuel cell is dissipated as heat (used for distributed heating). Moreover, in this operating mode, the maximum cells stack current is limited to ∼40 A to limit the cells degradation (as presented in Table I).

The fuel cell operating mode limits are 30-50 V on the low voltage side of the dc-dc converter. The total dc-ac system efficiency of the two stages presented in Fig. 8.

The system efficiency improvement given by the introduction of SiC MOSFETs as replacement of Si IGBTs is above 1% for the entire range in Fig. 8. At 1.5 kW the efficiency gain is ∼1.5% and at light load reaches a peak of 3% at 50 V. At converter light load the gain is more pronounced this is due to the large reduction of switching losses and forward voltage drop (conduction losses) achieved with SiC MOSFETs. However, in light load conditions efficiency is also strongly influenced by the losses in the magnetic components (e.g. high frequency transformer in the dc-dc stage and filtering components in the dc-ac stage) which are not affected by the power semiconductor type. This efficiency improvement

can be used to estimate the economic gain given by SiC power semiconductors. It should be also considered that the cost reduction in size terms of passive components and raw materials is a major advantage.

VII. Conclusion

In this paper, efficiency investigations on a grid-tie energy storage system for bidirectional fuel cells have been conducted. Efficiency improvements for both the dc-dc and the dc-ac power stages are investigated when the 1200 V Si IGBTs are replaced by SiC MOSFETs.

In fuel cell mode (SiC MOSFETs operating in active rectification mode), the dc-dc converter maximum efficiency improvement of 2.5% is achieved, this is due to the rather large forward voltage drop of the SiC antiparallel diodes. In electrolysis cell-mode (SiC MOSFETs in hard switching conditions), maximum efficiency improvements of 3% are achieved thanks to the significant reduction of the switching losses of SiC MOSFETs compared to Si IGBTs. On overall the dc-dc converter with SiC MOSFETs was capable of achieving a absolute maximum efficiency of 98.2% in fuel cell mode. The dc-ac converter based on a T-type topology achieved a maximum efficiency 97.7% with SiC MOSFETs. Compared to Si IGBTs this has been an efficiency improvement of $\sim$0.8% over almost the entire converter operating range, this also allows to significantly reduce the size of the converter cooling system (easily up to 50%). It is also observed that SiC MOSFETs can be used to double the switching frequency of the dc-ac converter and therefore reduce the size and cost of the filtering components.

On a system point of view, the introduction of SiC MOSFETs allowed to increase the overall system efficiency of $\sim$1% over the entire power range in fuel cell mode with peaks up to 1.5-3% depending on the converter operating point.

Acknowledgment

Authors would like to thank the Danish Energy Technology Development and Demonstration Programme (EUDP) number 64011-0036 “Green Natural Gas” and the Danish HTF grant number 008-2011-4 Intelligent Efficient Power Electronics (IEPE) strategic research center between the industry and universities for sponsoring the projects.

References

[1] Barton, J.P.; Infield, D.G., ”Energy storage and its use with intermittent renewable energy,” *IEEE Transactions on Energy Conversion*, vol.19, no.2, pp.441,448, June 2004.

[2] Price, A.; Bartley, S.; Male, S.; Cooley, G., ”A novel approach to utility scale energy storage [regenerative fuel cells],” *Power Engineering Journal*, vol.13, no.3, pp.122,129, June 1999.

[3] Biela, J.; Schweizer, M.; Waffler, S.; Kolar, J.W., ”SiC versus SiEvaluation of Potentials for Performance Improvement of Inverter and DCDC Converter Systems by SiC Power Semiconductors,” *IEEE Transactions on Industrial Electronics*, vol.58, no.7, pp.2872,2882, July 2011

[4] Peftitsis, D.; Rabkoswki, J.; Tolstoy, G.; Nee, H.-P. ”Experimental comparison of dc-dc boost converters with SiC JFETs and SiC bipolar transistors,” *Proceedings of the 2011-14th European Conference on Power Electronics and Applications EPE 2011*, 2011, pp. 1-9.

[5] Zapico, A.; Gabiola, I.; Apaniz, S.; Santiago, F.; Pujana, A. Rodrguez, A.; Briz, F., ”SiC and Si transistors comparison in boost converter” *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, 2012.

[6] Franke, W.-T.; Fuchs, F. ”Comparison of switching and conducting performance of SiC-JFET ad SiC BJT with a state of the art IGBT” *13th European Conference on Power Electronics and Applications EPE 2009*, 2009, pp. 1-10.

[7] Pittini, R.; Zhang, Z.; Andersen, M.A.E., ”Analysis of DC/DC converter efficiency for energy storage system based on bidirectional fuel cells,” *4th IEEE/PES Innovative Smart Grid Technologies Europe (ISGT EUROPE)*, 2013, pp.1,5, 6-9 Oct. 2013.

[8] Chongming Q.; Smedley, K.M., ”An isolated full bridge boost converter with active soft switching,” *IEEE 32nd Annual Power Electronics Specialists Conference PESC. 2001*, 2001, vol.2, pp.896,903 vol.2, 2001.

[9] Pittini, R.; Zhang, Z.; Andersen, M.A.E., ”Switching performance evaluation of commercial SiC power devices (SiC JFET and SiC MOSFET) in relation to the gate driver complexity,” *ECCE Asia Downunder (ECCE Asia 2013)*, 2013, pp.233,239, 3-6 June 2013.

[10] Teichmann, R.; Bernet, S., ”A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications,” *IEEE Transactions on Industry Applications*, vol.41, no.3, pp.855,865, May-June 2005.

[11] Schweizer, M.; Lizama, I.; Friedli, T. and Kolar, J. W., ”Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies, *36th Annual Conference on IEEE Industrial Electronics Society IECON 2010*, 2010, pp. 391-396.

[12] Anthon, A.; Zhang, Z.; Andersen, M.A.E.; Franke, T., ”Efficiency Investigations of a 3 kW T-Type Inverter for Switching Frequencies up to 100 kHz,” *International power Electronics Conference IPEC 2014 - ECCE Asia*, 2014, pp.78,83, 18-21 May 2014.

Appendix C

Comparative Evaluation of Three-Phase Isolated Matrix-Type PFC Rectifier Concepts for High Efficiency 380VDC Supplies of Future Telco and Data Centers

16th *European Conference on Power Electronics and Applications (EPE 2014)*

Comparative Evaluation of Three-Phase Isolated Matrix-Type PFC Rectifier Concepts for High Efficiency 380VDC Supplies of Future Telco and Data Centers

Patricio Cortes[1], Dominik Bortis[1], Riccardo Pittini[2] and Johann W. Kolar[1]
[1] Power Electronic Systems Laboratory, ETH Zurich
Physikstrasse 3, 8092 Zurich
Switzerland
Phone: +44 632 80 49
Email: cortes@lem.ee.ethz.ch
URL: http://www.pes.ee.ethz.ch
[2] Department of Electrical Engineering, Technical University of Denmark
Kgs. Lyngby, Denmark

Keywords

<<DC power supply>>, <<Matrix converter>>, <<Power factor correction>>, <<Power supply>>, <<Efficiency>>.

Abstract

Due to the high energy consumption in data and telco centers, the use of 380V or 400V DC facility-level distribution has been proposed as an alternative to the conventional AC distribution for a more efficient power delivery structure. The DC voltage is powered from the three-phase mains by a PFC rectifier and in many cases a mains transformer is used to provide galvanic isolation. In order to achieve a high efficiency in the DC voltage generation and to implement the required isolation, a single-stage concept, such as a matrix-type rectifier that enables PFC functionality and galvanic isolation in a single conversion, can be beneficial. In addition, due to the fact that with the matrix-type rectifier the galvanic isolation is performed with a high-frequency transformer, this results in a more compact rectifier system compared to conventional systems where the mains-frequency isolation transformer is located at the input of the PFC rectifier.
In this paper, an overview of isolated matrix-type PFC rectifier topologies is given and a new converter circuit is proposed, analyzed and comparatively evaluated against another promising PFC rectifier concept, the phase-modular IMY-rectifier.

1 Introduction

To improve the energy efficiency in telco and data centers, the use of a DC power distribution architecture (PDA) instead of an AC PDA has been proposed in the literature [1, 2]. The basic structures of a conventional AC PDA and a facility-level DC PDA are shown in **Fig. 1**. As can be noticed, the conventional AC PDA (cf. **Fig. 1(a)**) includes multiple conversion stages, which lead to a strongly reduced overall power distribution system efficiency. Typically, at the AC distribution system's input a double conversion Uninterruptible Power Supply (UPS) in combination with a bulky 50/60 Hz main transformer is utilized. The UPS rectifies the 400/480V AC into a DC voltage where an energy storage system, e.g. battery backup system, is connected. Then, the DC voltage is inverted back to 400/480V AC voltage that supplies the Power Distribution Unit (PDU). At the PDU, the voltage is stepped down to a voltage suitable to the Power Supply Units (PSU), typically between 90 and 264 V AC. In the PSU this AC voltage is then

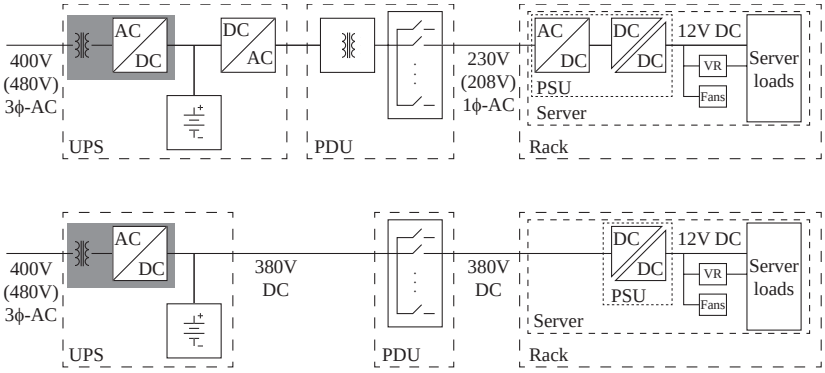


Fig. 1: Power distribution architectures (PDA) for data and telco centers, **(a)** conventional AC power distribution and **(b)** 380V DC facility-level power distribution.

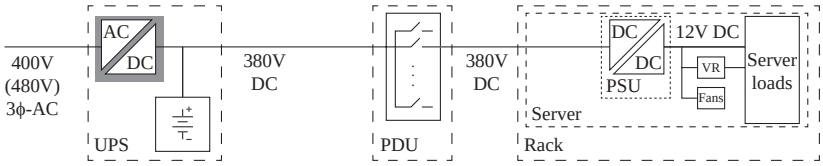


Fig. 2: 380V DC facility-level PDA with an isolated three-phase buck-type PFC rectifier that features PFC functionality and provides galvanic isolation with a high-frequency transformer.

again converted to a DC voltage which is finally – due to the large conversion ratio – stepped down by an isolated DC/DC converter to the 12V DC required by the different loads in the servers. Depending on the efficiency of the different components, the overall efficiency of such an AC PDA is between 50 % and 70 % [1].

In a facility-level DC PDA, however, several conversion steps can be avoided. As shown in **Fig. 1(b)**, the DC/AC conversion in the UPS, the transformer in the PDU and the AC/DC conversion in the PSU are eliminated, resulting in a higher efficiency of the power distribution system, e.g. 72.7 % efficiency [1] (assuming 95.3 % efficiency of the AC/DC converter).

In the last years, the selection of the optimal voltage level for the facility-level DC PDA has been discussed in the literature and also several organizations are working on the standardization of low voltage DC grids, where mainly the use of 380V DC [2, 3, 4] or 400V DC [1] is proposed for a more efficient DC power distribution architecture. However, a discussion about the optimal converter topology that supplies the facility-level DC power distribution is still missing in the literature.

Since the facility-level DC PDA is also powered from the three-phase 400V/480V mains, with the mentioned DC voltage selection of either 380V or 400V DC boost-type PFC rectifiers are no more suitable because the DC output voltage of boost-type PFC rectifiers has to be at least above the peak value of the mains line-to-line voltage; thus, with a wide input voltage range up to 480Vrms, the output voltage is typically selected to 700V to 800V DC. Consequently, a three-phase buck-type PFC topology has to be selected which allows to directly step down the varying input voltage to the proposed 380-400V DC. In addition, the overall system volume can be strongly reduced by omitting the bulky mains-frequency transformer if the galvanic isolation is realized with a subsequent DC/DC conversion stage which contains a high-frequency isolation transformer (cf. **Fig. 2**). Furthermore, in order to achieve a high overall AC/DC conversion efficiency, instead of this conventional two-stage conversion concept, a three-phase matrix-type buck rectifier topology which provides PFC functionality and galvanic isolation in a single conversion can be used; thus also no large DC-link capacitance for intermediate energy storage is required.

In this paper, a review of different three-phase matrix-type buck-type isolated PFC rectifier topologies is presented in **Section 2** and the most promising topology, regarding efficiency and realization effort, is

ISBN: 978-1-4799-3014-2 and 978-9-0758-1520-7

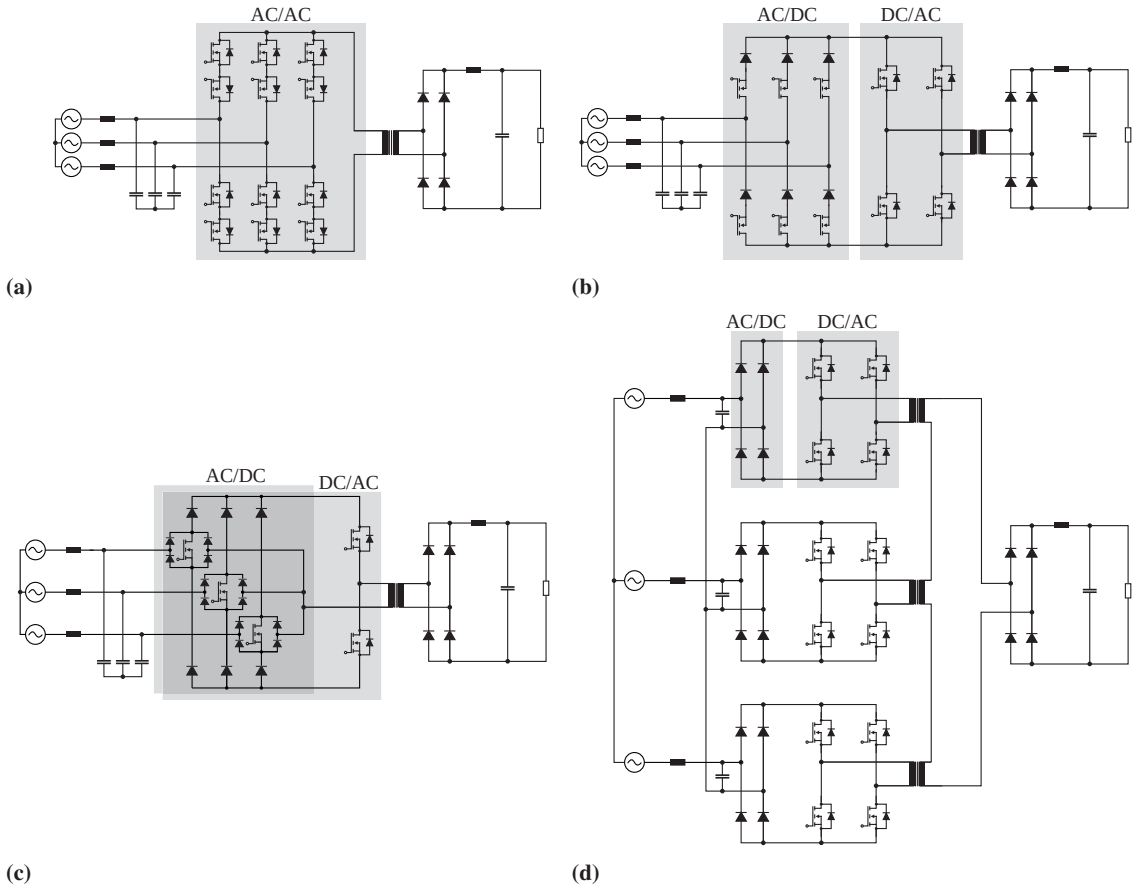


Fig. 3: Topologies of isolated matrix-type three-phase AC/DC converters, **(a)** direct matrix converter. **(b)** indirect matrix converter. **(c)** VIENNA rectifier III and **(d)** IMY-rectifier.

further analyzed in **Section 3**, and is compared in **Section 4** with a previously analyzed phase-modular matrix-type PFC rectifier system, the IMY-rectifier [5].

2 Isolated Matrix-Type PFC Rectifiers

Typically, the single-stage power conversion can be realized with a direct matrix-type PFC rectifier that directly converts the mains-frequency AC voltage into a high-frequency AC voltage which is supplied to a high-frequency isolation transformer and whose secondary voltage is then rectified to the desired DC output voltage as proposed in [6] (cf. **Fig. 3(a)**). As can be noticed, in this topology for the direct AC/AC conversion a large number of semiconductor devices is needed, thus, also the control and modulation scheme complexity are high.

In order to strongly reduce the system complexity and in most of the cases also the number of switches, the direct AC/AC conversion stage can be split into an AC/DC and a DC/AC conversion, which is then due to the still missing intermediate energy storage a so called indirect matrix-type PFC rectifier. As proposed in [7, 8], e.g. a conventional buck-type PFC rectifier in combination with a phase-shift DC/DC converter could be used (cf. **Fig. 3(b)**). In this case, however, the conventional buck-type PFC rectifier suffers from high conduction losses in the high-frequency diodes which are needed in series to the switches [9]. Nevertheless, since with the indirect matrix-type rectifier also other more efficient AC/DC converter topologies can be combined, it offers a high flexibility and is attractive for the realization of the active front end of the DC PDA. Therefore, in order to fully utilize the potential of indirect matrix-type isolated PFC rectifiers, in this paper it is proposed to substitute the conventional buck-type PFC rectifier by a simple diode rectifier with an integrated active filter as presented in [10, 11], which in combination with

ISBN: 978-1-4799-3014-2 and 978-9-0758-1520-7

the isolated DC/DC converter provides galvanic isolation and a highly efficient PFC functionality (cf. **Fig. 4**, [12]).
As an alternative, the indirect matrix-type converter in **Fig. 3(b)** could be modified in such a way that one bridge-leg of the DC/DC converter is again integrated into the input rectifier stage, thus results in the VIENNA rectifier III [13] which could be seen as hybrid combination of a direct and an indirect matrix-type rectifier (cf. **Fig. 3(c)**). However, even if the system complexity and the number of switches are further reduced – only five instead of ten switches are needed – the large number of diodes leads to high conduction losses. Consequently, this topology is not further considered in this paper.
Utilizing the indirect matrix-type rectifier concept, a different approach is to use phase-modular converters, e.g. the isolated matrix-type Y-rectifier (IMY-rectifier) as proposed in [5, 14], where the three-phase indirect matrix-type converter is split into three separated single-phase indirect matrix-type converters (cf. **Fig. 3(d)**). Besides the advantage of modularity, since to each of the single-phase converters only the single-phase voltage is applied, 600V instead of 1200V semiconductor devices can be used, which feature a lower on-state resistance and improved switching behavior. In addition, the converter can be controlled with a simple modulation scheme that enables soft-switching for each switching transition. Hence, due to the low system complexity and the expected high efficiency, the phase-modular IMY-rectifier is another suitable option to supply the DC PDA.
Therefore, in the next section the proposed three-phase Isolated Integrated Active Filter Matrix-type (I^2AFM) PFC rectifier is presented and will be evaluated in comparison to the phase-modular IMY-rectifier.

3 Isolated Integrated Active Filter Matrix-type PFC Rectifier

3.1 Operating Principle

As shown in **Fig. 4**, the rectifier stage of the proposed I^2AFM PFC rectifier consists of a simple three-phase diode bridge rectifier with an additional injection circuit, the integrated active filter (IAF), comprising a high-frequency bridge-leg with the switches S_1 and S_2, the inductance L and the low-frequency bidirectional switches S_a, S_b and S_c. As can be noticed, as long as the injection circuit is not enabled, that means S_1 and S_2 are not switched, the input stage of the I^2AFM rectifier is working as a simple three-phase diode bridge rectifier and a highly distorted input current is flowing through the two diodes connected to the highest and lowest input voltage (cf. **Fig. 5(c)** for $t < 40\,\text{ms}$). However, in order to achieve sinusoidal input currents drawn from the mains, the switches S_1 and S_2 of the injection circuit can be controlled in such a way that always a third harmonic current is impressed into the phase with the smallest input absolute voltage, i.e. the input phase which would not conduct current at that time (cf. **Fig. 5(d)** for $t > 40\,\text{ms}$). Since in the three-phase mains every 60° of the mains period the smallest absolute input voltage (v_a, v_b or v_c) alternates between the input phases a, b and c, the proper phase has to be selected by turning on one of the switches S_a, S_b or S_c (cf. **Fig. 5(b)** for $t > 40\,\text{ms}$). As analytically described in [10, 11], if during each 60° interval the injected current is proportional to the smallest input voltage, i.e. a 60°-portion of a sine wave, and a constant output power is delivered by the DC/DC converter stage, with this modulation scheme all input currents will show a sinusoidal shape (cf. **Fig. 5(c)** for $t > 40\,\text{ms}$). The major advantages of the IAF rectifier are the relatively low implementation effort with the low component count, the simple modulation scheme and the high expected efficiency, since on the one hand for the bridge rectifier slow switching rectifier diodes with a low on-state voltage drop can be used and on the other hand in the injection circuit always only the phase current with the lowest instantaneous value has to be processed. However, assuming a certain needed intermediate capacitance C_{dc} in order to keep the inductance in the commutation path of the injection circuit and the DC/DC converter low, the output voltage v_{dc} will not be constant but will vary with a sixfold mains-frequency (cf. **Fig. 5(e)**). In fact, the output voltage is always equal to the maximum phase-to-phase input voltage since it is now defined by the diode rectifier and thus the average output voltage can also vary with the possible wide input voltage range of the local mains. Therefore, in order to eliminate the sixfold mains-frequency and to avoid large output voltage variations, the highly promising IAF rectifier has to be combined with a subsequent DC/DC converter that provides an isolated and constant output voltage. In the DC/DC stage, both half-bridges are modulated with a 50 % duty cycle, whereas the output voltage is controlled by the phase shift between the two half-bridge voltages. As already mentioned, since the instantaneous input voltage is varying

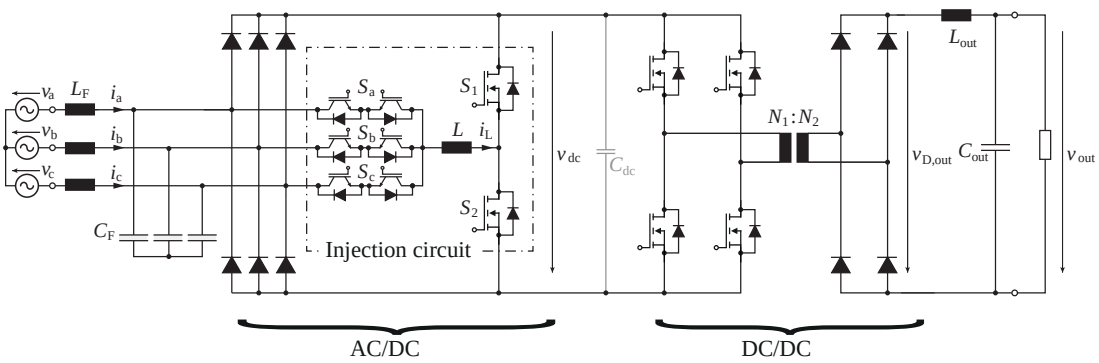


Fig. 4: Proposed Isolated Integrated Active Filter Matrix-type (I^2AFM) PFC rectifier.

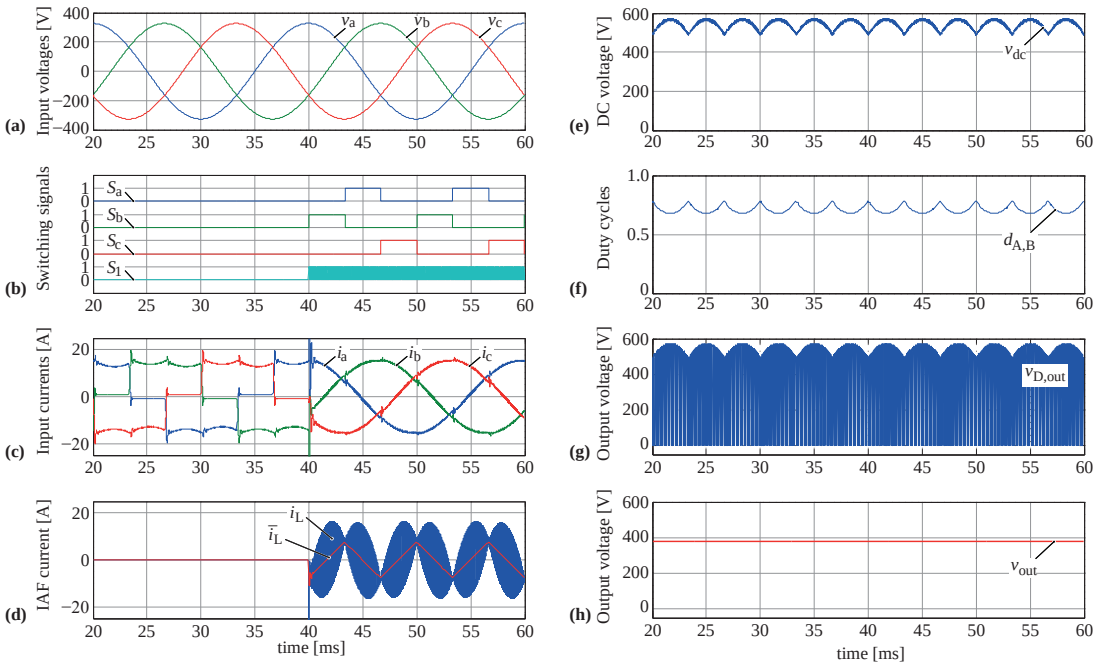


Fig. 5: Simulated waveforms of the I^2AFM PFC rectifier, where the IAF rectifier is turned on at time $t = 40$ ms, while the DC/DC stage is already in steady-state operation at $t = 0$ ms, **(a)** phase input voltages, **(b)** switching signals of the IAF rectifier, **(c)** phase input currents, **(d)** inductor current in the injection circuit, **(e)** intermediate DC-link voltage, **(f)** duty cycle of the DC/DC converter, i.e. the phase shift between the half-bridge voltages, **(g)** rectified output voltage of the transformer and **(h)** controlled output voltage.

over time, the phase shift between the two half-bridge, i.e. the duty cycle, has to be properly adapted in order to obtain a constant output voltage (cf. **Fig. 5(f)-(h)**). In addition, it is assumed that the leakage inductance of the isolation transformer is large enough and thus enables soft-switching for each switching transition. This almost eliminates all switching losses and only slightly increases the conduction losses in the switches, thus results in high overall system efficiency.

ISBN: 978-1-4799-3014-2 and 978-9-0758-1520-7

Table I: Current stresses in the semiconductor devices of the I^{2}AFM PFC rectifier. ($\hat{I}_{\mathrm{in}}$ denotes the mains phase current amplitude and I_{dc} is the output current).

Component	Average current	RMS current
Input diodes	$\hat{I}_{\mathrm{in}}\frac{\sqrt{3}}{2\pi}$	$\hat{I}_{\mathrm{in}}\sqrt{\frac{1}{6}+\frac{\sqrt{3}}{8\pi}}$
Injection circuit switches $S_{\mathrm{a}}, S_{\mathrm{b}}, S_{\mathrm{c}}$	$\frac{\hat{I}_{\mathrm{in}}}{\pi}\left(1-\frac{\sqrt{3}}{2}\right)$	$\hat{I}_{\mathrm{in}}\sqrt{\frac{1}{12}-\frac{\sqrt{3}}{8\pi}}$
Half-bridge switches S_1, S_2	$\frac{3\hat{I}_{\mathrm{in}}}{\pi}\left(\frac{\sqrt{3}}{2}\ln(\sqrt{3})-\frac{\sqrt{3}-1}{2}\right)$	$\hat{I}_{\mathrm{in}}\sqrt{\frac{3}{\pi}\left(\frac{\sqrt{3}}{2}-\frac{\pi}{6}+\frac{\sqrt{3}}{2}\ln\left(\frac{2}{\sqrt{3}}\right)\right)}$
Antiparallel diodes of switches S_1, S_2	$\frac{3\hat{I}_{\mathrm{in}}}{\pi}\left(\frac{\sqrt{3}}{2}\ln\left(\frac{1}{\sqrt{3}}\right)+\frac{1}{2}\right)$	$\hat{I}_{\mathrm{in}}\sqrt{\frac{3}{\pi}\left(\frac{3\sqrt{3}}{8}-\frac{\pi}{6}-\frac{\sqrt{3}}{2}\ln\left(\frac{2}{\sqrt{3}}\right)\right)}$
DC-DC converter switches	$\frac{N_2}{N_1}\frac{I_{\mathrm{dc}}}{2}$	$\frac{N_2}{N_1}\frac{I_{\mathrm{dc}}}{\sqrt{2}}$
DC-DC converter output diodes	$\frac{I_{\mathrm{dc}}}{2}$	$\frac{I_{\mathrm{dc}}}{\sqrt{2}}$

3.2 Converter Design

For the design and optimization of the proposed I^{2}AFM PFC rectifier, first the current stresses in the different components have to be calculated, which for the IAF PFC rectifier was already done in [11]. A summary of the current stresses in the semiconductor devices of the I^{2}AFM PFC rectifier is shown in **Table I**. There, a large output inductor of the DC/DC stage is assumed, whereby the switching frequency ripple of the output current can be neglected.

In order to enable a fair comparison of the proposed I^{2}AFM PFC rectifier and the IMY-rectifier, the design of the I^{2}AFM PFC rectifier is performed for the same operating conditions as described in [5] which are listed again in **Table II**.

Since in the I^{2}AFM PFC rectifier the voltage stress of all semiconductor devices is defined by the peak phase-to-phase input voltage of the three-phase mains, 1200V instead of 600V semiconductor devices have to be used. A major part of the losses in the IAF PFC rectifier result due to the conduction losses in the input bridge rectifier, which rectifies the low frequency input voltage. Therefore, silicon diodes with low forward voltage drop have to be selected, in order to keep the efficiency high. Based on the specification given in **Table II**, with the selected 1200V/45A diodes (DSP45-12A) the conduction losses in the input rectifier are 23.6 W.

For the bidirectional switches S_{a}, S_{b} and S_{c} of the injection circuit which also switch at low switching frequency – two times the mains frequency – the switching losses are negligible and therefore can be implemented with two standard IGBTs connected in anti-series that feature a low forward voltage drop. Alternatively, it would be also possible to use reverse blocking IGBTs in antiparallel connection, which would reduce the conduction losses from 6.6 W to 5 W. However, due to the limited availability of RB-IGBT, 1200V/40A standard IGBTs (IHW40T120) with integrated antiparallel diodes are used.

In contrast to the bidirectional switches S_{a}, S_{b} and S_{c}, for the switches S_1 and S_2 of the high-frequency bridge-leg, that controls the current over the IAF inductor L, the switching losses have to be considered. Due to the needed blocking voltage of 1200V silicon MOSFETs are not applicable, thus the selection of the proper switch technology is limited to either IGBTs which are optimized for fast switching applications (e.g. 1200V, 40A, IGW40N120H3) or Silicon Carbide (SiC) MOSFETs (1200V, 80 mΩ, C2M0080120D). Although the conduction losses in both cases are low (4.6 W with IGBTs and 1.6 W with SiC-MOSFETs),

Table II: Electrical specifications used for the comparative evaluation of the I^{2}AFM PFC rectifier and the IMY-rectifier.

Parameter	Value
Nominal power P_0	7.5 kW
Output voltage V_{out}	380 V
Input voltage V_{N}	400 $\mathrm{V}_{\mathrm{ph-ph,rms}}$
Switching frequency f_{sw}	48 kHz

Table III: Main components of the I^2AFM PFC rectifier prototype.

Component	Value/details
Input diodes	1200 V/45 A rectifier diodes (DSP45-12A)
Inj. circuit switches S_a, S_b, S_c	1200 V/40 A IGBTs (IHW40T120)
Half-bridge switches S_1, S_2	1200 V/31.6 A SiC MOSFETs (C2M0080120D)
DC/DC converter switches	1200 V/31.6 A SiC MOSFETs (C2M0080120D)
DC/DC converter output diodes	1200 V/54 A SiC diodes (C4D40120D)
IAF inductor L	380 µH, 1 pair E55 N87 cores, 3x1.4 mm air gap, 36 turns of 2 mm, 0.1 mm/175 strands litz wire
Isolation transformers	Stack of two E55 N87 cores, $N_1/N_2 = 16/16$, 40 µm/270 strands litz wire (4 in parallel)
Filter inductor L_{out}	2x497 µH, E55 N87 cores, 3x0.8 mm air gap, 34 turns of 2.5 mm solid copper wire

the switching losses in the IGBTs (36 W) are five times higher than for the SiC-MOSFETs (6.7 W) assuming a switching frequency of 48 kHz.

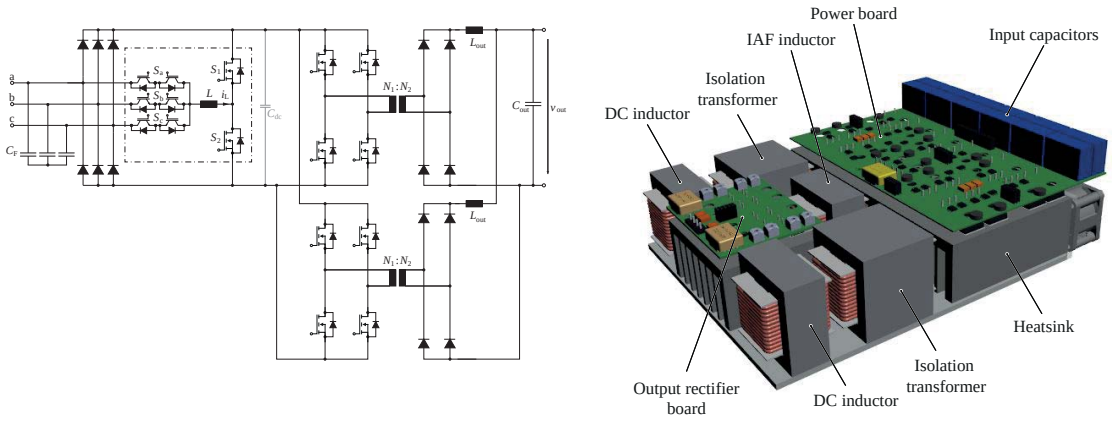
Consequently, the switches S_1 and S_2 of the injection circuit as well as the switches of the DC/DC converter's full-bridge are realized with SiC-MOSFETs, even if the full-bridge can be operated in soft-switching at nominal output power. However, namely at low load conditions, where the current in the leakage inductance is no more sufficient to charge/discharge the output capacitances of the switches, soft-switching is lost resulting in high switching losses. The conduction losses in the DC/DC converter's full-bridge are calculated to 44.9 W at nominal output power.

Due to the high switching frequency and the hard commutation of the output rectifier, which would lead to high reverse recovery losses if silicon diodes would be used, the output diode bridge is realized with 1200V SiC Schottky diodes (C4D40120D). Even if the reverse recovery losses can be neglected in this case, the conduction losses in the output rectifier of 83 W (together with the conduction losses of the full-bridge) are dominating the achievable efficiency of the DC/DC stage, since the forward voltage drop of SiC Schottky diodes compared to silicon diodes is relatively high.

In order to keep the input filter effort low and due to reasons of system controllability, the inductor L of the IAF rectifier's injection circuit is designed with respect to a maximum current ripple which has to be below 50 % of the peak input current. Based on this assumption, an inductor optimization considering different core types and wires (solid and litz wire) is performed, and the inductor design offering the best compromise between losses and volume is selected. The same optimization procedure of the magnetic components was also applied for the design of the output inductor L_{out}, however with a lower current ripple of 2.5A (25 %), as well as for the isolation transformer. The turns ratio of the isolation transformer was selected to $N_1/N_2 = 1$, which still allows a 15 % voltage margin for the output voltage control at minimum input voltage. Details concerning the design of the magnetic components and a list of the selected semiconductor devices are summarized in **Table III**.

The corresponding 3D CAD model of the designed laboratory prototype is visualized in **Fig. 6(b)**. In order to show the placement of the described power components, the top board containing the EMI filter, control board and output capacitors has been omitted. Based on this design, a total volume of 4.68 dm^3 and/or a power density of 1.6 kW/dm^3 is achieved.

For the sake of completeness, it has to be mentioned that the DC/DC stage of the laboratory prototype is advantageously realized with two parallel DC/DC converters (cf. **Fig. 6(a)**). Consequently, on the one hand the efficiency can be further increased, especially in part load below 50 % where e.g. one DC/DC converter can be turned off, and on the other hand the current ripple in the output capacitor can be reduced by interleaving the switching signals of two parallel DC/DC converters.



(a) **(b)**

Fig. 6: I^{2}AFM PFC rectifier 7.5 kW laboratory prototype, **(a)** circuit diagram with two parallel interleaved DC/DC converters, **(b)** 3D CAD model of the converter without the top PCB.

4 Comparative Evaluation of Three-Phase Isolated Matrix-Type PFC Rectifiers

Based on the specifications given in **Table II**, now the performance of the proposed and designed I^{2}AFM PFC rectifier is compared to the also promising phase-modular IMY-rectifier presented in [5] (cf. **Fig. 3(d)**). Two alternative implementations for each PFC rectifier topology are considered for the comparative evaluation:

- I^{2}AFM PFC rectifier with a DC/DC stage consisting of only one DC/DC converter;
- I^{2}AFM PFC rectifier with a DC/DC stage consisting of two parallel DC/DC converters;
- IMY-rectifier where each switch of the full-bridge is implemented with only a single MOSFET of the CFD-CoolMOS series from Infineon (IPW65R041CFD);
- IMY-rectifier where each switch of the full-bridge is implemented with two parallel MOSFETs of the CFD-CoolMOS series (IPW65R041CFD).

For the efficiency calculations of the two considered implementations of the I^{2}AFM PFC rectifier, the analytical equations for the current ratings given in **Table I** and the devices listed in **Table III** are used. The efficiency of the phase-modular IMY-rectifier is calculated according to the design presented in [5]. In addition, for both PFC rectifier topologies it is considered that in the full-bridges soft-switching is only achieved above a certain minimum output power and thus in low load operation the switching losses have to be taken into account.
The calculated efficiencies of the different implementations as a function of the load power are shown in **Fig. 7(a)**. At nominal load, with the I^{2}AFM PFC rectifier and a DC/DC stage consisting of only one DC/DC converter an overall efficiency of 97 % can be achieved, which can be increased to 97.6 % if a second DC/DC converter is connected in parallel. The maximum efficiency of 97.7 % is achieved at 25 % of the nominal load, whereas 20.8 % (12.1W) of the losses are generated in the AC/DC stage and 79.2 % (45.9W) in the DC/DC stage. As already mentioned, in order to improve the low load behavior of the I^{2}AFM PFC rectifier, the second DC/DC stage is turned off when the load current is below a certain limit and therefore the efficiencies of both implementations, with either one or two DC/DC converters, are the same (cf. **Fig. 7(a)**).
In contrast, the achievable efficiency of the IMY-rectifier is considerably lower, which is 95.3 % if only one MOSFET is used per switch and 96 % if two parallel MOSFETs are used per switch [5] (cf. **Fig. 7(a)**). The main reasons for the difference in efficiency can be found in the conduction losses of the input diode rectifier, the full-bridge and the transformer, which in the IMY-rectifier are almost twice to three times higher than those of the I^{2}AFM PFC rectifier (cf. **Fig. 7(b)**). In all three cases this can principally be

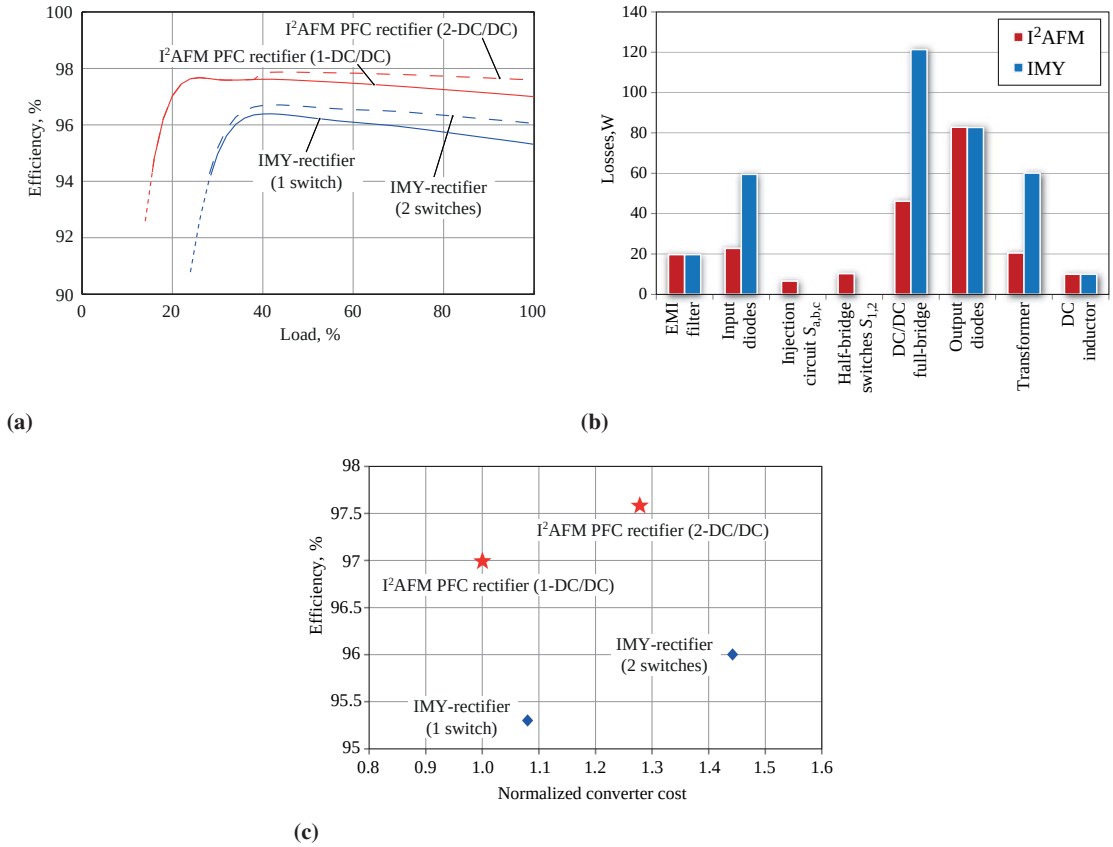


Fig. 7: Comparative evaluation of the I^{2}AFM PFC rectifier and the IMY-rectifier, **(a)** achievable efficiency at different load conditions, **(b)** calculated loss distribution at nominal load of 7.5 kW and **(c)** resulting efficiencies at nominal load of 7.5 kW with respect to the normalized converter costs considering the power semiconductors and main passive components.

explained by the higher number of components which are needed in the IMY-rectifier compared to the I^{2}AFM PFC rectifier; 12 instead of 6 input diodes, 12 instead of 4 switches in the full-bridge and 3 transformers instead of 1 transformer. In addition, each input diode of the IMY-rectifier is conducting the input current during one half-cycle of the mains voltage, while in the I^{2}AFM PFC rectifier an input diode is only conducting during one third of the mains period. Hence, due to the same input current amplitude in both converter topologies, for the IMY-rectifier this results in higher average and RMS currents and consequently in higher conduction losses. Furthermore, even if in the IMY-rectifier 650V-CoolMOS devices with a superior low on-state resistance can be used, the three times larger number of switches results in more than twice the conduction losses in the full-bridge compared to the I^{2}AFM PFC rectifier. Despite the fact that additional losses are generated in the injection circuit (cf. **Fig. 7(b)**), the IMY-rectifier can't compete in efficiency, since the losses in the injection circuit are moderate compared to the overall I^{2}AFM PFC rectifier losses (cf. **Fig. 7(b)**).

Besides the achievable efficiency the comparative evaluation also considers another aspect, namely the resulting material costs of each PFC rectifier topology. In **Fig. 7(c)** a normalized cost comparison considering the costs of the power components is shown, where the prices for the semiconductor devices and passive components have been extracted from distributor's data, i.e. the price for 1000 pieces. It can be noticed that for both PFC rectifier topologies the costs are very similar (difference of only 8 %) if in the IMY-rectifier only one MOSFET per switch and in the I^{2}AFM PFC rectifier only one DC/DC converter is used (**Fig. 7(c)**). Improving the efficiency of both rectifier topologies by approximately 0.6 % (45W), by either adding a second MOSFET per switch in the IMY-rectifier or a DC/DC converter in the I^{2}AFM PFC rectifier, increases the corresponding costs by 33 % and 28 %, respectively. This relatively strong increase in costs clearly shows that the expensive semiconductor devices account for the largest share of the overall costs.

ISBN: 978-1-4799-3014-2 and 978-9-0758-1520-7

5 Conclusions

This paper gives an overview of isolated matrix-type PFC rectifier topologies suitable for facility-level DC PDA for more efficient telco and data centers. In the comparative evaluation of isolated three-phase PFC rectifier systems it is shown that matrix-type PFC rectifier topologies offer the advantage of performing PFC functionality and galvanic isolation in a conversion single-stage. On the one hand, this potentially enables higher system efficiency compared to two-stage concepts and on the other hand, the bulky mains transformer, which is typically used in existing power distribution systems, can be omitted. Furthermore, in this paper a new isolated matrix-type PFC rectifier topology is proposed, the I^2AFM PFC rectifier. The I^2AFM PFC rectifier features an indirect matrix converter structure which basically is a combination of an AC/DC stage and a subsequent DC/DC stage without intermediate energy storage elements. The rectification with PFC functionality is performed with a simple three-phase diode rectifier circuit with an additional injection circuit, the IAF-rectifier. The major advantages of the IAF-rectifier are the relatively low implementation effort with the low component count, the simple modulation scheme and its high efficiency.
The performance of the designed I^2AFM PFC rectifier is evaluated in comparison with the phase-modular IMY-rectifier, which is also a promising solution for the realization of the active front end of the DC PDA. It is shown that with the proposed I^2AFM PFC rectifier an almost 2 % higher efficiency can be achieved compared to the IMY-rectifier, even if the material costs are approximately the same. With a single DC/DC output stage of the I^2AFM system the achievable efficiency at nominal load is 97 %, and can be improved up to 97.6 % if a second DC/DC converter is used in parallel. Future work includes the realization of a 7.5 kW laboratory prototype to experimentally verify the presented converter performance.

References

[1] A. Pratt, P. Kumar, and T. Aldridge, "Evaluation of 400v dc distribution in telco and data centers to improve energy efficiency," in *Proc. of 29th International Telecommunications Energy Conference (INTELEC)*, 2007, pp. 32–39.

[2] E. Waffenschmidt and U. Boeke, "Low voltage dc grids," in *Proc. of 35th International Telecommunications Energy Conference (INTELEC)*, 2013, pp. 1–6.

[3] M. Noritake, T. Ushirokawa, K. Hirose, and M. Mino, "Verification of 380V dc distribution system availability based on demonstration tests," in *Proc. of 33rd International Telecommunications Energy Conference (INTELEC)*, 2011, pp. 1–6.

[4] M. Salato, A. Zolj, D. Becker, and B. J. Sonnenberg, "Power system architectures for 380V dc distribution in telecom datacenters," in *Proc. of 34th International Telecommunications Energy Conference (INTELEC)*, 2012, pp. 1–7.

[5] P. Cortes, L. Fässler, D. Bortis, M. Silva, and J. W. Kolar, "Detailed analysis and design of a three-phase phase-modular isolated matrix-type PFC rectifier," in *Proc. of International Power Electronics Conference - ECCE Asia (IPEC)*, 2014, pp. 3864–3871.

[6] V. Vlatkovic, D. Borojevic, X. Zhuang, and F. Lee, "Analysis and design of a zero-voltage switched, three-phase PWM rectifier with power factor correction," in *Proc. of 23rd Annual IEEE Power Electronics Specialists Conference (PESC)*, vol. 2, 1992, pp. 1352–1360.

[7] S. Manias and P. Ziogas, "A novel sinewave in ac to dc converter with high-frequency transformer isolation," *IEEE Transactions on Industrial Electronics*, vol. IE-32, no. 4, pp. 430–438, 1985.

[8] K. Wang, F. Lee, D. Boroyevich, and X. Yan, "A new quasi-single-stage isolated three-phase ZVZCS buck PWM rectifier," in *Proc. of 27th Annual IEEE Power Electronics Specialists Conference (PESC)*, 1996, pp. 449–455.

[9] A. Stupar, T. Friedli, J. Miniböck and J. W. Kolar, "Towards a 99% efficient three-phase buck-type PFC rectifier for 400-V dc distribution systems," *IEEE Transactions on Power Electronics*, Vol. 27, No. 4, pp. 1732–1744, April 2012.

[10] H. Yoo and S.-K. Sul, "A new circuit design and control to reduce input harmonic current for a three-phase ac machine drive system having a very small dc-link capacitor," in *Proc. of 25th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 611–618.

[11] T. Soeiro, T. Friedli, and J. W. Kolar, "Three-phase high power factor mains interface concepts for electric vehicle battery charging systems," in *Proc. of 27th Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2012, pp. 2603–2610.

[12] T. Soeiro, "High efficiency electrostatic precipitator systems with low effects on the mains," PhD. Dissertation, ETH Zurich, 2012.

[13] J. W. Kolar, U. Drofenik, H. Ertl, and F. Zach, "VIENNA Rectifier III - A novel three-phase single-stage buck-derived unity power factor ac-to-dc converter system," in *Proc. of IEEE Nordic Workshop on Power and Industrial Electronics (NORPIE)*, 1998, pp. 9–18.

[14] P. Cortes, J. Huber, M. Silva, and J. W. Kolar, "New modulation and control scheme for phase-modular isolated matrix-type three-phase ac/dc converter," in *Proc. of 39nd Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 2013, pp. 4897–4904.

Appendix D

Component Stress Factor: Analysis of Dual Active Bridge and Isolated Full Bridge Boost Converter for Bidirectional Fuel Cells Systems

IEEE International Power Electronics and Applications Conference and Exposition (PEAC 2014)

Analysis and Comparison Based on Component Stress Factor of Dual Active Bridge and Isolated Full Bridge Boost Converters for Bidirectional Fuel Cells Systems

Riccardo Pittini, Maria C. Mira, Zhe Zhang, Arnold Knott, Michael A.E. Andersen
Technical University of Denmark, Dept. of Electrical Engineering
Oersteds Plads 349, 2800 Kgs. Lygnby, Denmark
ripit@elektro.dtu.dk

***Abstract*—This paper presents an analysis and comparison of isolated topologies for bidirectional fuel cell systems. The analyzed topologies are the dual active bridge (DAB) and the isolated full bridge boost converter (IFBBC). The analysis is performed based on the component stress factor (CSF). Results highlight that the DAB has lower CSF than the IFBBC for narrow converter operating points. On the other hand the IFBBC presents a more homogeneous CSF over the entire converter operating range. Finally, experimental results obtained from a 30-80 V 80 A 6 kW 40 kHz IFBBC are presented. The converter achieves efficiencies up to 98.2% and 97.45% depending on the converter power flow.**

Keywords—Dual Active Bridge (DAB), Isolated full Bridge Boost Converter (IFBBC), Component Stress Factor (CSF), High Efficiency, Bidirectional Fuel Cells.

I. Introduction

Power converter's efficiency has been one of the major driving forces in power electronics especially over the last two decades. The latest developments in the power semiconductor technologies allowed developing converters with efficiency above 98% even with isolated topologies [1],[2]. However, selecting the latest silicon carbide (SiC) power semiconductors [3] it is not sufficient to achieve high efficiency. It is necessary to perform an analysis and optimization of different solutions in terms of converter topology, power semiconductors, magnetic component design as well as converter optimization.

Large scale integration of renewable energies requires grid tie energy storage to balance the energy production and consumption [4]. For these applications bidirectional fuel cells represent an attractive technology [5]. However, bidirectional fuel cells, also called regenerative or reversible fuel cells (RFCs), have wider operating conditions than conventional unidirectional fuel cells. Choosing the most suitable topology that can guarantee good performance over the entire system operating range is always troublesome and challenging. This is especially true for fuel cells applications where power converters are expected to operate at low-voltage and high-current levels.

This paper presents an analysis of two isolated dc-dc converter topologies: the isolated full bridge boost converter (IFBBC) [2] and the dual active bridge (DAB) [6]. The two topologies are analyzed in terms of component stress factor [7],[8] and compared based on the converter specifications for bidirectional fuel cell applications. Based on the analysis, a 6 kW bidirectional dc-dc IFBBC has been developed. The converter prototype achieves peak efficiencies of 98.2% and 97.45% depending on the converter power flow.

II. System Analysis and Specifications

An energy storage bidirectional system based on regenerative fuel cells requires high efficiency dc-dc and dc-ac converters to effectively operate the system at its maximum performance. The cell technology strongly affects the system topology in fact, the voltage of a single cell is too low to realized multi-kW energy storage systems. It is necessary to stack several cells to achieve voltage levels that can better be processed by multi-kW power converters. Stacking a large number of cell increases the manufacturing challenges, such as homogeneous operating conditions of the cells stack and fuel pressure equalization. Moreover, not all fuel cells are suitable for bidirectional operation since operating in the two modes could significantly change the stress conditions of the cells and affect their reliability.

Based on a close cooperation with a large fuel cells manufacturer, it was determined that new solid oxide cell technology can be operated in both fuel cell mode (SOFC) and electrolyzer cell mode (SOEC). Table I shows the dc-dc converter specifications, which are defined based on a laboratory prototype of SOFC/SOEC cells stack. A 50 kW

TABLE I
SOFC AND SOEC DC-DC CONVERTER SPECIFICATIONS

	SOFC	SOEC
Low Voltage (LV) side	30-50 V	50-80 V
Current (LV) side	40-0 A	0-80 A
High Voltage (HV) side	700-800 V	700-800 V
Power Rating	~1500 W	~6000 W

978-1-4799-6768-1/14/$31.00 ©2014 IEEE

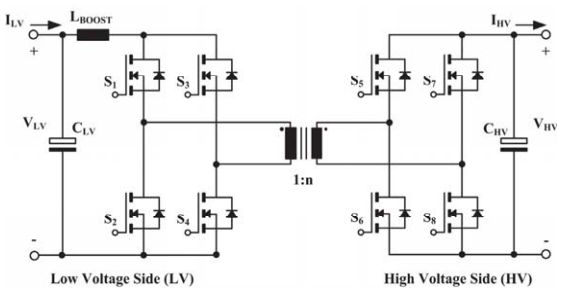


Fig. 1 IFBBC topology.

system for grid connected energy storage applications is presented in [9]. The system is composed by 10 cells stacks and each stack has a dc-dc converter. The operating mode of the system (SOFC or SOEC) determines the operating conditions of the dc-dc converter (I-V curve, [9]) and therefore, the system efficiency for the different operating points.

III. Isolated Topologies for Bidirectional Fuel Cells Systems: Selection and Analysis

Different isolated topologies can be candidate for energy storage systems based on bidirectional fuel cells. However, resonant topologies have difficulties to achieve suitable high efficiency when the converter ports voltage varies significantly (e.g. in this application by a factor 2.6). Another factor that influences the selection of the topology is its complexity in terms of number of power semiconductors, passive components and control. All these parameters will significantly affect also the cost of the converter and the economical sustainability of the system.

The results from the analysis of different isolated dc-dc converter topologies highlighted two candidate topologies suitable for the system: the isolated full bridge boost converter (IFBBC) and the dual active bridge (DAB).

A. Isolated Full Bridge Boost Converter (IFBBC)

The IFBBC topology shown on Fig. 1, has proved to achieve efficiency up to 98% [2] in fuel cell applications. The main CCM operating waveforms are presented in Fig. 2. The boost inductor L_{BOOST} is the component that controls the energy transfer from the converter low voltage side to the high voltage side and it has to handle the high current level I_{LV} on the converter low voltage side. Given an operating point, the duty cycle (0.5<D<1) is calculated according to (1).

$$D = 1 - \frac{nV_{LV}}{2V_{HV}} \tag{1}$$

For a given converter switching frequency $f_{SW}=1/T_{SW}$, the maximum and minimum boost inductor currents are expressed by (2) and (3) respectively. The transformer rms current of the low voltage side (4) can be calculated using (2) and (3).

$$i_0 = I_{LV} - \frac{V_{LV}T_{sw}(2D-1)}{4L} \tag{2}$$

$$i_1 = I_{LV} + \frac{V_{LV}T_{sw}(2D-1)}{4L} \tag{3}$$

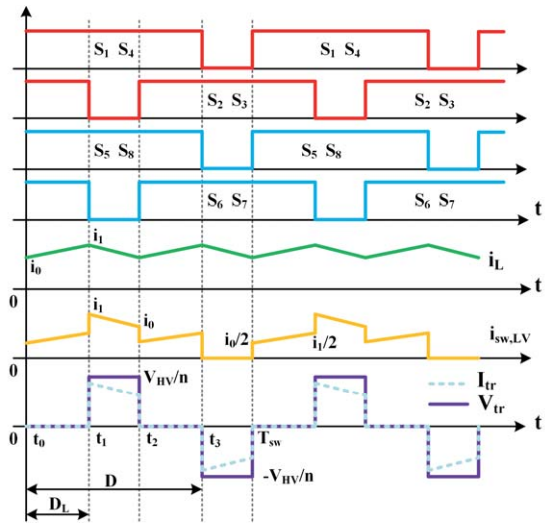


Fig. 2 IFBBC CCM main operating waveforms.

$$I_{tr.LV,rms} = \frac{\sqrt{2}}{\sqrt{3}}\sqrt{(1-D)(i_0^2 + i_1^2 + i_0 i_1)} \tag{4}$$

By neglecting the ripple in the boost inductor, it is possible to simplify (4) obtaining the transformer current in the low voltage winding as shown in (5).

$$I_{tr.LV,rms} = I_{LV}\sqrt{2(1-D)} \tag{5}$$

Assuming ideal current distribution in the converter switches, during the intervals t0-t1 and t2-t3 each switch on the converter low voltage side carries $I_{LV}/2$. During the intervals t1-t2 and t3-Tsw the full I_{LV} current flows through the switch. This results that the rms current of the low voltage side switches can be calculated as in (6).

$$I_{sw.LV,rms} = I_{LV}\sqrt{\frac{3}{4} - \frac{D}{2}} \tag{6}$$

The rms current of the high voltage side transformer winding and of the high voltage switches is expressed as a function of the current in the low voltage winding as in (7).

$$I_{tr.HV,rms} = \frac{I_{tr.LV,rms}}{n}; \quad I_{sw.HV,rms} = \frac{I_{tr.LV,rms}}{n\sqrt{2}}; \tag{7}$$

B. Dual Active Bridge (DAB)

In the DAB topology, shown in Fig. 3, the power flow is controlled through the ac-inductance in series with the transformer. Phase-shift modulation allows controlling the power flow in the converter with the phase-shift angle. By defining φ the phase-shift angle between the primary full bridge and the secondary full bridge, the power transfer between the low-voltage and the high voltage sides of the converter can be expressed as in (8). The maximum power transfer is achieved for $\varphi = \pi/2$; it can be observed that large

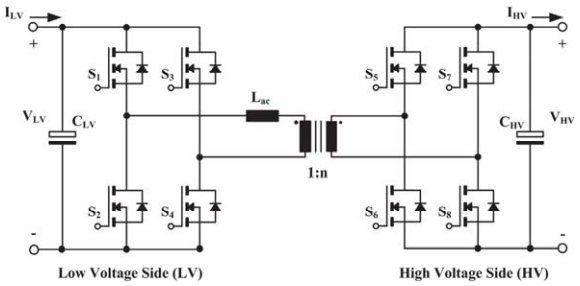


Fig. 3 DAB topology.

values of the L_{ac} would limit the maximum power flow in the converter.

$$P = \frac{V_{LV} V_{HV}}{n\omega L_{ac}} \varphi \left(1 - \frac{\varphi}{\pi}\right) \tag{8}$$

Defining the voltage transfer ratio as in (9) allows expressing the transformer current at time intervals t0 and t1 as in (10) and in (11) respectively.

$$M = \frac{V_{HV}}{n\, V_{LV}} \tag{9}$$

$$i_0 = \frac{-V_{LV}}{2\omega L_{ac}} [(1 - M)(\pi - \varphi) + (1 + M)\varphi] \tag{10}$$

$$i_1 = \frac{V_{LV}}{2\omega L_{ac}} [(1 + M)\varphi + (1 - M)(\pi - \varphi)] \tag{11}$$

The symmetry of the transformer current (12) allows expressing the rms transformer low voltage side current as in (13). The transformer current on the high voltage winding is related to the rms current on the transformer low voltage side by the turns ratio *n*. The ac-inductor current rms current is the same as the rms current of the transformer low voltage side winding. It is a common design procedure to integrate the ac-inductor in the transformer by tuning the transformer leakage inductance.

$$i_2 = -i_0; \qquad i_3 = -i_1; \tag{12}$$

$$I_{tr.LV,rms} = \frac{1}{\sqrt{3}} \sqrt{i_0^2 + i_1^2 - i_0 i_1 + 2\frac{\varphi}{\pi} i_0 i_1} \tag{13}$$

The rms current of both low voltage and high voltage switches is defined as a function of the transformer low voltage windings rms current as in (14).

$$I_{sw.LV,rms} = \frac{I_{tr.LV,rms}}{\sqrt{2}}; \quad I_{sw.HV,rms} = \frac{I_{tr.LV,rms}}{n\sqrt{2}}; \tag{14}$$

IV. Component Stress Factor Analysis

Component stress factor (CSF) is an analytical method used to evaluate and compare different converter topologies for a specific application. The method provides an estimation of the converter stresses and gives a quantitative measure of converter performance. The CSF method is similar to the component load factor (CLF) [4],[5], the difference in the two methods lies in how the individual and total components are calculated. In order to perform a fair comparison of the topologies, CSF assumes that the same amount silicon, magnetic material and capacitor volume are used on the analyzed topologies. This is

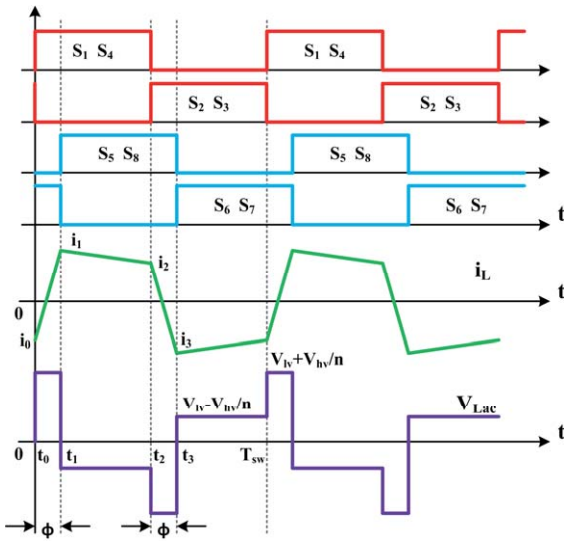


Fig. 4 DAB main operating waveforms with phase-shift modulation.

ensured by applying weighting factors to each component. The CSF analysis is performed based on three separate components: the semiconductor component stress factor (SCSF) (15), the winding component stress factor (WCSF) (16) and the capacitor component stress factor (CCSF) (17). The total stress over the different components is computed separately by adding together the relative components of the semiconductors (18), windings (19) and capacitors (20).

The different CSF values are calculated based on the devices voltages and rms currents. For power semiconductors the maximum voltage that the devices have to withstand over the entire converter operating range is considered. For wounded components, such as inductors and transformers, V_{max} represents the maximum averaged value (based on duty cycle). For capacitive components V_{pk} is the maximum peak value. All the CSF values are scaled with the processed power, making the CSF a dimensionless quantity.

$$SCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{{V_{max}}^2 \cdot {I_{rms}}^2}{P^2} \tag{15}$$

$$WCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{{V_{max}}^2 \cdot {I_{rms}}^2}{P^2} \tag{16}$$

$$CCSF_i = \frac{\sum_j W_j}{W_i} \cdot \frac{{V_{pk}}^2 \cdot {I_{rms}}^2}{P^2} \tag{17}$$

$$SCSF = \sum_{Semiconductors} SCSF_i \tag{18}$$

$$WCSF = \sum_{Windings} WCSF_i \tag{19}$$

$$CCSF = \sum_{Capacitors} CCSF_i \tag{20}$$

In (15)-(17) $\sum_j W_j$ represent the total available resources for each component and W_i represent the amount of resources assigned to the specific component. In order to minimize the different CSF values, the resources can be differently

distributed by using the W_i weighting factors however, as first iteration the resources are supposed equally distributed. In (18)-(20) each component represents a specific stress; therefore, a CSF comparison requires to compare only components of the same type.

A. CSF Analysis for the Candidate Topologies

The results from the CSF analysis are presented in Fig. 5. The plots are shown as function of the converters operating voltages and currents on the low voltage side. The converter voltage on the high voltage side is fixed at 750 V and a summary of the dc-dc converter specifications used for the analysis is presented in Table II. The maximums values have been limited in order to have more comprehensive plots.

From Fig. 5 it can be observed that the values of the IFBBC's CSF (SCSF, WCSF and CCSF shown in Fig. 5a, 5b and 5c respectively) increase as the converter operating voltage on the LV-side decreases and the values are independent on the operating current. The transformer turns ratio also affects the values of the CSF; in the case of the IFBBC, the transformer turns ratio n=8 is chosen in order to minimize the voltage stress on the LV-side power semiconductors. Similarly, the SCSF, WCSF and CCSF values for the DAB topology are presented in Fig. 5d, 5e and 5f respectively. In this case, all the CSF values vary with both converter voltage and current. This is due to the variation of the phase-shift angle that controls the power flow in the DAB. For all the CSF values of the DAB, there is a minimum defined by the transformer voltage transfer ratio between primary and secondary. In this case, the optimal transformer ratio n=14 was selected in the middle of the converter voltage operating range on the LV-side. By varying the number of transformer turns, it is possible to move the CSF minima to other converter operating points.

TABLE II
DC-DC CONVERTER PARAMETERS FOR CSF ANALYSIS

LV-side voltage	30-80 V
LV-side current	0-80 A
HV-side voltage	750 V
Transformer turns ratio	8 (IFBBC), 14 (DAB)

There is a major difference in the distribution of the CSF values within the two analyzed topologies: for specific operating points, the minimum value of SCSF and CCSF is lower for the DAB topology compared to the IFBBC. However, the IFBBC has lower WCSF over the entire converter operating range. In all the CSF values the DAB has a minimum at 54 V and 7 A; while, the IFBBC has always a minimum at 80 V on the converter LV-side. The major difference in the CSF values is observed for the WCSF: the IFBBC has very low WCSF while these values for the DAB are large due to the large ac-currents and voltages that continuously stress the magnetic components. The CSF values of the IFBBC increase at low voltage levels; this trend is homogeneous over the entire converter operating range. On the other hand, in the DAB, the CSF values widely increase especially at low current levels, when the converter is operating outside its optimal voltage transfer ratio, e.g. 54 V with n=14.

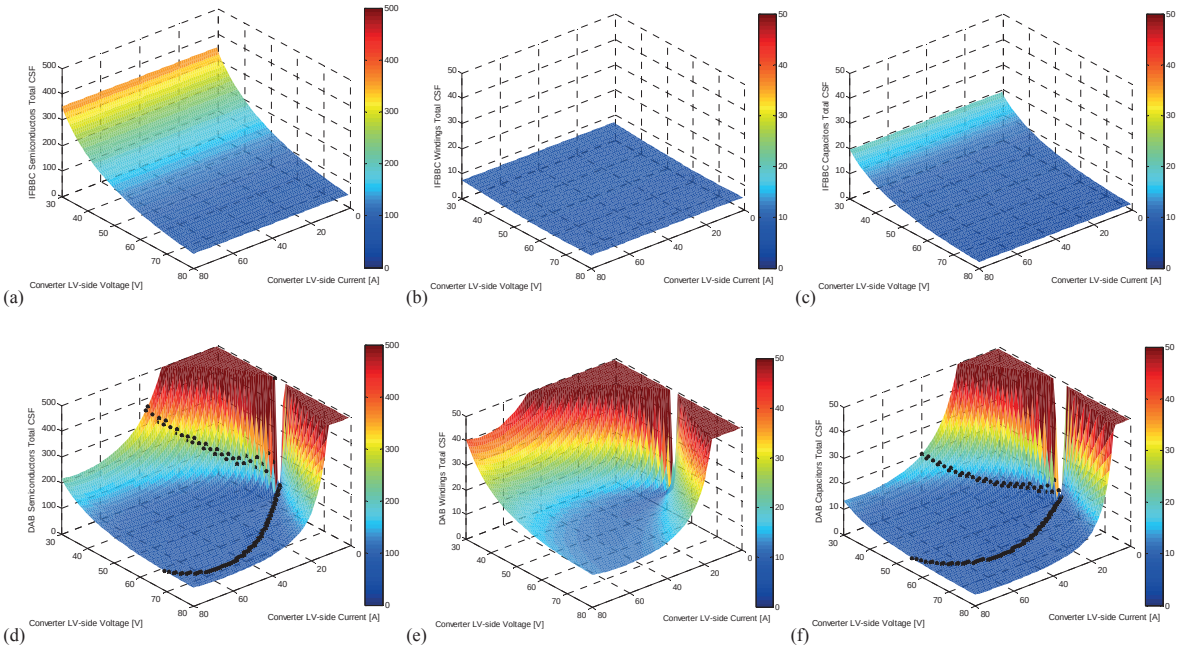


Fig. 5 IFBBC topology CSF: SCSF in (a), WCSF in (b) and CCSF in (c). DAB topology CSF: SCSF in (d), WCSF in (e) and CCSF in (f). Black dots in (d) and in (f) represent the intersection between the IFBBC CSF and the DAB CSF values.

TABLE III
AVERAGE CSF VALUES DEPENDING ON THE OPERATING MODE

Topology	SCSF	WCSF	CCSF
IFBBC FC-mode	217.8	6.5	11.3
DAB FC-mode	816.3	153.1	51.0
IFBBC EC-mode	109.0	5.5	5.3
DAB EC-mode	259.7	48.7	16.2

In order to select the most suitable topology, it is not only necessary to perform a CSF analysis, but it is also necessary to consider the overall system in which the dc-dc converter is expected to operate. Based on the cells stack characteristics presented in Section II, an I-V curve of the cell stack is built for both SOFC and SOEC operating modes [9]. The I-V model is used to determine all converter operating points. The converter CSF values are computed and averaged for all SOFC operating points and for all SOEC operating points. The obtained CSF values for SOFC and SOEC operation of the dc-dc converter are presented in Table III.

From the averaged CSF values it is interesting to observe that for both system operating modes (SOFC and SOEC) the average CSF of the IFBBC is significantly lower than the DAB. The IFBBC's average SCSF in FC-mode is 1/4 of the DAB's average SCSF in the same mode. The difference in average SCSF is to 1/2-1/3 in EC-mode. Similar differences are observed also in the average CCSF values. The IFBBC's average CCSF is about five times lower in FC-mode than the DAB; this difference is reduced down to three times for the EC operating mode. The largest difference is observed in the magnetic components stress factor, in this case the IFBBC has an average WCSF which is almost 1/20th in FC-mode and 1/10th in EC-mode compared to the DAB's average WCSF. The DAB has a high average WCSF due to the ac current circulating in the transformer windings and to the fixed duty cycle of the phase-shift modulation.

On overall, the IFBBC has lower CSF values and a more homogeneous variation over the entire converter operating range. It should be observed that for fixed operating points the DAB would be preferable. However, when computing averaged values, the large CSF values that are observed in non-optimal operating points of the DAB give large contribution and therefore, they have a large weight on the overall average.

TABLE IV
IFBBC DC-DC CONVERTER CHARACTERISTICS

Voltage primary side (LV)	30-80 V
Maximum current primary side	80 A
Voltage secondary side (HV)	700-800 V
Maximum power	2400-6400 W
Low Voltage (LV) side MOSFETs	120V 4.1mΩ TK72E12N1 2 in parallel
High Voltage (HV) side SiC MOSFETs	SCT30N120 SiC MOS C4D15120 SiC diode
Inductor	20 µH
Inductor core size/material	3xE6030 KoolMu 90-26-90
Turn ratio n	1:8
Transformer core size/material	2xE64 pairs/Magnetics R
Switching frequency	40 kHz

V. EXPERIMENTAL PROTOTYPE OF A ISOLATED FULL BRIDGE BOOST CONVERTER

The dc-dc converter for fuel cells is expected to operate with a variety of cells stacks; therefore the dc-dc converter is required to operate over the entire I-V specification in Table I. This requirement is necessary since the SOEC/SOFC technology if not fully mature and variations in the I-V characteristics are expected. Moreover, the I-V curve of SOEC/SOEC stacks depends also on the stack operating conditions (temperature, fuel composition, etc.). The IFBBC topology is selected since it has a more homogenous distribution of the CSF thus, a more homogeneous distribution of the converter efficiency is expected.

The converter prototype of a high efficiency IFBBC for bidirectional fuel cells, shown in Fig. 6a, has been developed and tested. The initial converter prototype was based on Si MOSFETs, Si IGBTs and SiC diodes. This prototype was capable of achieving efficiencies up to 97.8% and 96.5% [9][10] depending on the power flow direction. The converter was then updated with SiC MOSFETs in the full bridge of the converter HV-side. Its main operating waveforms at 60 V 80 A are shown in Fig. 6b and a summary of the converter

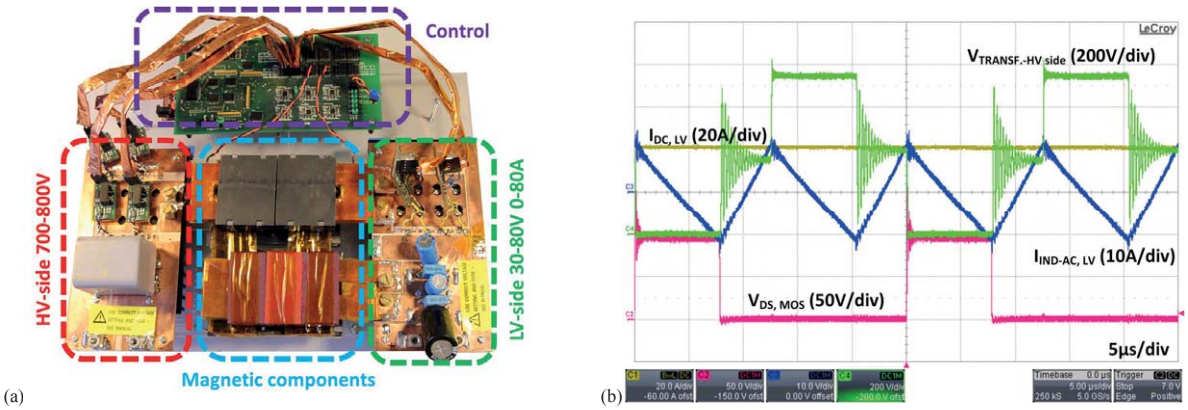
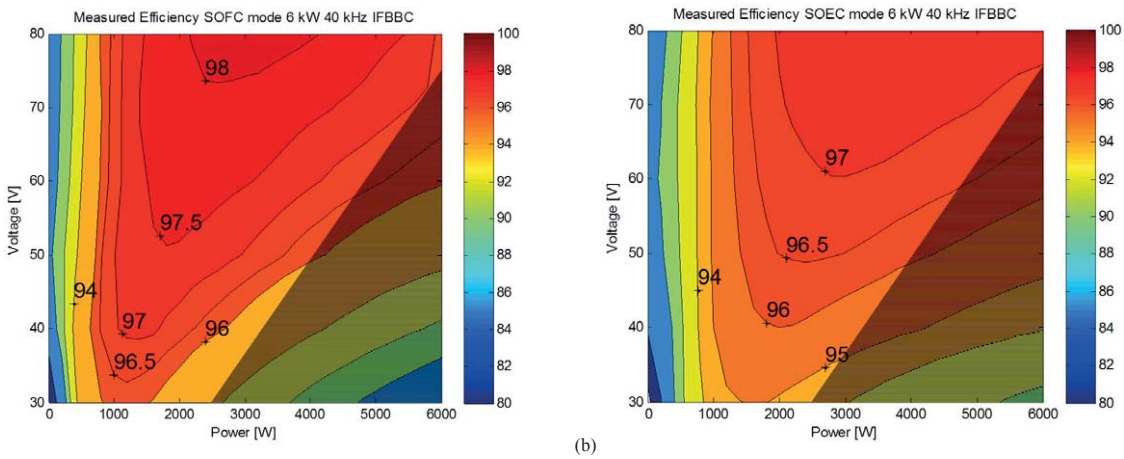


Fig. 6 IFBBC prototype highlighted its main components (a) and main operating waveforms at 60 V 80 A (b).



(a) (b)

Fig. 7 Measured efficiency of the IFBBC prototype for fuel cell operating mode (a) and for electrolyzer cell operating mode (b). Peak efficiency in SOFC mode 98.2% and in SOEC mode 97.45%. Darkened area indicates current limitation of the dc-dc converter.

characteristics is presented in Table IV. The converter magnetics are based on custom planar cores in high frequency ferrite for the transformer (Magnetics R-type material) and in distributed gap material (Magnetics KoolMu) for the boost inductor.

The new converter based SiC active switches is capable of achieving efficiencies up to 98.2% when operating in fuel cell mode (power flow from the converter LV-side to the HV-side) and up to 97.45% with reversed power flow, as shown in Fig. 7a and 7b respectively. The highest dc-dc conversion efficiencies are always measured with a current of ~40 A and at the highest converter voltage on the LV-side (80 V). At the lowest voltage on the LV-size (30 V) the converter achieved an efficiency above 96% and 95% depending on the direction of the converter power flow, as shown in Fig. 7a and 7b.

VI. Conclusions

This paper presents a component stress factor (CSF) analysis of the isolated full bridge boost converter (IFBBC) and of the dual active bridge (DAB) operating with phase-shift modulation. The analysis focuses on bidirectional dc-dc converters for fuel cell applications since they require wide operating voltage and current ranges.

The analysis highlights that the DAB has a lower absolute CSF however, the CSF in the DAB rapidly increases as the operating conditions deviate from the optimal operating point. In the DAB, the CSF varies along with both converter voltage and current; while in the IFBBC it depends only on the converter operating voltage. The IFBBC has a lower at average CSF which is also independent from the converter current. The bidirectional fuel cell I-V characteristic has been used to compute an average CSF for both fuel cell and electrolyzer cell operating modes. This highlighted that the IFBBC is a preferable topology for wide operating voltage ranges.

A 6 kW (30-80 V 80 A boosted up to 700-800 V) converter prototype of an IFBBC has been developed. The converter is based on high current fully planar magnetics and is capable of achieving peak efficiency of 98.2% in fuel cell mode and of 97.45% in regenerative mode.

References

[1] Hirose, T.; Nishimura, K.; Kimura, T.; Matsuo, H., "An ac-link bidirectional DC-DC converter with synchronous rectifier," IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society, pp.351,357, 7-10 Nov. 2010.

[2] Nymand, M.; Andersen, M. A E, "High-Efficiency Isolated Boost DC–DC Converter for High-Power Low-Voltage Fuel-Cell Applications," IEEE Transactions on Industrial Electronics, vol.57, no.2, pp.505,514, Feb. 2010.

[3] Biela, J.; Schweizer, M.; Waffler, S.; Kolar, J.W., "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors," IEEE Transactions on Industrial Electronics, vol.58, no.7, pp.2872,2882, July 2011.

[4] Barton, J.P.; Infield, D.G., "Energy storage and its use with intermittent renewable energy," Energy Conversion, IEEE Transactions on , vol.19, no.2, pp.441,448, June 2004.

[5] J. D. Maclay, J.Brouwer, G. S.Samuelsen, "Dynamic modeling of hybrid energy storage systems coupled to photovoltaic generation in residential applications", 2007 Journal of Power Sources, vol.163, issue 2, pp. 916-925.

[6] Kheraluwala, M.N.; Gascoigne, R.W.; Divan, D.M.; Baumann, E.D., "Performance characterization of a high-power dual active bridge DC-to-DC converter," IEEE Transactions on Industry Applications, vol.28, no.6, pp.1294,1301, Nov/Dec 1992.

[7] Bruce Carsten, "Converter Component Load Factors; A Performance Limitation of Various Topologies," in PCI, Munich, 1988.

[8] Petersen, L.; and Michael Andersen, "Two-Stage Power Factor Corrected Power Supplies: the Low Component-Stress Approach," in Applied Power Electronics Conference and Exposition (APEC), 2002.

[9] Pittini, R.; Zhe Zhang; Andersen, M.A.E., "Analysis of DC/DC converter efficiency for energy storage system based on bidirectional fuel cells," Innovative Smart Grid Technologies Europe (ISGT EUROPE), 2013 4th IEEE/PES, pp.1,5, 6-9 Oct. 2013.

[10] Pittini, R.; Zhe Zhang; Andersen, M.A.E., " Isolated Full Bridge Boost DC-DC Converter Designed for Bidirectional Operation of Fuel Cells/Electrolyzer Cells in Grid-Tie Applications" 15th European Conference on Power Electronics and Applications (EPE-ECCE Europe 2013), 3-5 September 2013.

Appendix E

Analysis of DC/DC Converter Efficiency for Energy Storage System Based on Bidirectional Fuel Cells

IEEE 4th European Innovative Smart Grid Technologies (ISGT 2014)

Analysis of DC/DC Converter Efficiency for Energy Storage System Based on Bidirectional Fuel Cells

Riccardo Pittini, Zhe Zhang and Michael A.E. Andersen
Technical University of Denmark
Dept. of Electrical Engineering
Oersteds Plads 349
Kgs. Lyngby, Denmark
ripit@elektro.dtu.dk, zz@elektro.dtu.dk, ma@elektro.dtu.dk

***Abstract*—Renewable energy sources are fluctuating depending on the availability of the energy source. For this reason, energy storage is becoming more important and bidirectional fuel cells represent an attractive technology. Fuel cells require high-current low-voltage dc-dc or dc-ac converters as power interface to the grid. In power electronics, the converter efficiency is characterized at fixed operating voltage for various output power. This type of characterization is not suitable for fuel cells, since as the power from the fuel cell increases, the cell voltage decreases. This paper analyses how the fuel cell I-V characteristics influences the power electronics converter efficiency and their consequence on the overall system. A load-dependent efficiency curve is presented based on experimental results from a 6 kW dc-dc converter prototype including the most suitable control strategy which maximizes the dc-dc conversion efficiency.**

***Index Terms*—Fuel cells, Energy storage, Smart grids, Dc-dc power converters, Energy efficiency.**

I. Introduction

Renewable energy sources are expected to play and important role in the future energy market. However, large scale integration of dynamic renewable energy sources introduces new stress on the old electric grid. Most of the renewable sources are unpredictable (e.g. wind, solar and tidal energy) leading to an increasing need for sustainable grid-tie energy storage. Bidirectional fuel cells, often referred as regenerative fuel cells (RFCs), represent an attractive technology capable of storing energy with high energy density since, electricity is stored as a fuel [1]. Conventional fuel cells are based on polymer electrolyte membrane (PEM); these cells are not suitable for bidirectional operation and they are often combined with supercapacitors or batteries for increasing the system performance [2][3].High temperature solid oxide fuel cells /electrolyzer cells (SOFC /SOFC) have been proven to be capable of operating bidirectionally and with high efficiency making this technology particularly interesting for large scale integration of grid-tie energy storage.

One of the main challenges of RFCs is related to the manufacturing and design of the cells. Designing high power stacks of RFCs is challenging in terms of reliability, long term degradation and fuel /gas-pressure equalization. Moreover, as the number of series stacked cells increases, higher is the probability that the single cell stresses vary since the same current flows through all the cells (series connection) and different degradation rates are expected to be observed. Dc-dc and dc-ac converters are used for power conditioning in order to avoid too large cells stacks and for properly utilizing the stacks at the desired operating point. In an energy storage system based on RFCs the power flows through the dc-ac and dc-dc converters every time energy is produced or stored, Fig. 1. For this reason, the system efficiency is strongly dependent on the power converters efficiency. Having a dedicated dc-dc converter for each cell stack is advantageous in order to allow controlling each cells stack at a different operating point and allowing high system efficiency since each dc-dc converter is optimized for the single RFC stack.

In most of power electronics applications, dc-dc and dc-ac converters efficiency is characterized at different voltage and power levels [4]. This type of characteristic does not take into account the nature of the source which can strongly affect the operating point and efficiency of the converter. In fact the I-V characteristic of the RFC stack determines the dc-dc converter operating points and, therefore, efficiency characteristic. This paper presents the efficiency characteristics of an experimental dc-dc converter for RFCs rated at 6 kW. The dc-dc converter efficiency is discussed in relation to peak and infield efficiencies. The converter prototype is capable of a peak efficiency of 97.8% however, the I-V characteristics of the RFC stack limits its efficiency to 96.8% at best. A new efficiency characterization of dc-dc converter based on I-V characteristics of the RFCs is proposed. Moreover, a comparison of the calculated and experimental efficiency is presented and discussed.

II. System Topology for Renewable Energy Storage Based on Fuel Cells

There are several system topologies that would be suitable for grid-tie energy storage systems based on bidirectional fuel cells. The system configuration and system components will

Project sponsored by the Energy Technology Development and Demonstration Programme (EUDP) "Green Natural Gas", 2011-2014.

978-1-4799-2984-9/13/$31.00 ©2013 IEEE

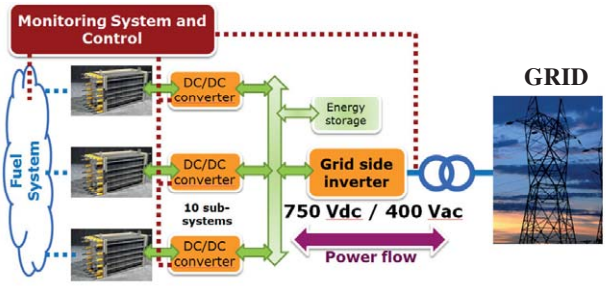


Fig. 1. Overview of the energy storage system based on bidirectional fuel cells.

affect the performance and controllability of the system. The case scenario is a 50 kW energy storage system based on SOFC /SOEC cells, Fig. 1. The selected system topology considers a single grid-tie inverter however, for better system performance at low power levels, small paralleled inverters are recommended.

In the analyzed case each cell stack is composed of 50 solid oxide fuel cells /electrolyzer cells (SOFC /SOEC) capable of operating up to 75 V 80 A in SOEC mode and up to 35 V 40 A in SOFC mode (50 cell stack). The maximum continuous power that the cells can handle is about 5-6 kW in SOEC and 1.5 kW in SOFC; higher power and current would reduce the lifetime of the cells stack. The cells stack characteristics represent the minimum requirements for the dc-dc converter design. Each cells stack has its own dc-dc converter in order to have optimal control and monitoring of each cells stack. During high energy production the system is operated in SOEC mode while during low energy production the system operates in SOFC mode. This type of operation mode also reflects the electricity spot price (low spot price when there is a surplus of energy production and vice versa when the energy production is low). An additional energy storage element is added to the system in order to compensate the low dynamic behavior of the SOFC /SOEC cells. This element increases the dynamic response of the system but also increases the system cost.

TABLE I
SOFC AND SOEC DC-DC CONVERTER SPECIFICATIONS

	SOFC	SOEC	
Low Voltage (LV) side	30-50	50-80	[V]
Current (LV) side	40-0	0-80	[A]
High Voltage (HV) side	700-800	700-800	[V]
Power Rating	~1500	~6000	[W]

III. DC/DC CONVERTER: BIDIRECTIONAL ISOLATED FULL BRIDGE BOOST CONVERTER

The influence of the dc-dc converter efficiency is analyzed based on a developed prototype of an isolated full bridge boost converter (IFBBC [5]), Fig. 2a. This topology proved to be suitable for fuel cell applications achieving very high efficiency up to 98% at low voltage and high current [4]. One of the main drawbacks of the selected topology is its startup problem when the output voltage (inverter side) is lower than the specified minimum voltage [6]. Several solutions have been proposed to solve this issue [7][8] however, the selected system topology is not affected by this issue since the control loop of the grid tie inverter maintains the high voltage bus in the specified range.

The converter is designed according to the RFCs specifications on Table I. The developed converter is characterized by a low voltage side (RFCs interface) of 30-80 V and 0-80 A, while the high voltage side is defined at 700-800 V for a 400 Vrms grid-tie inverter. The converter has a maximum power of ~6 kW limited by the maximum current on the low voltage side and a switching frequency of 40 kHz, Fig. 2b. The developed dc-dc converter prototype is based on fully planar magnetics (Kool Mu material for the boost inductor and R type material for the transformer, both from Magnetics). The power devices on the low voltage side are Si MOSFETs (IPP041N12N3) and on the high voltage side are Si IGBTs (IGW15N120H3) with SiC diodes (C4D15120A) in antiparallel. The converter efficiency is characterized by laboratory measurements at different voltage levels for the RFCs side (30-80 V) and for both power flow directions. The high voltage dc-bus was kept constant at 750 V.

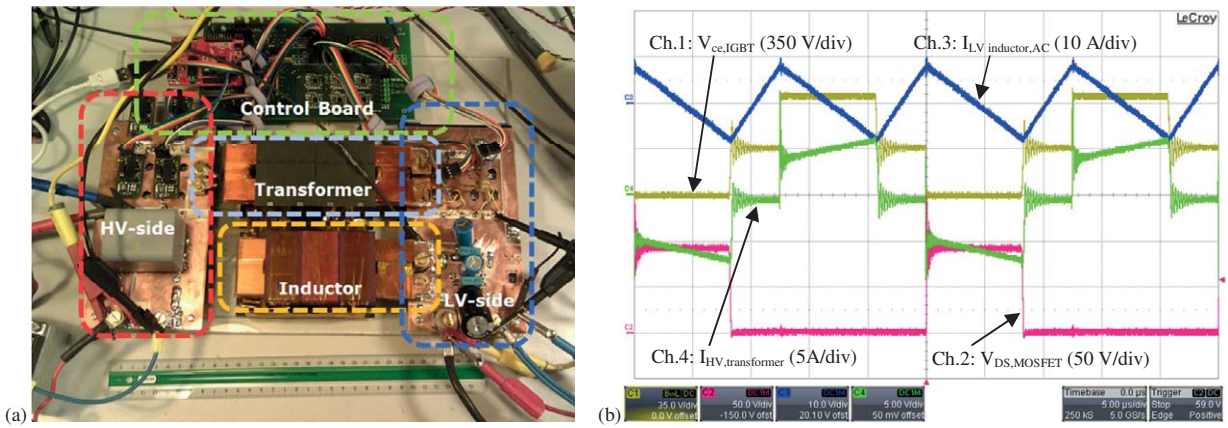
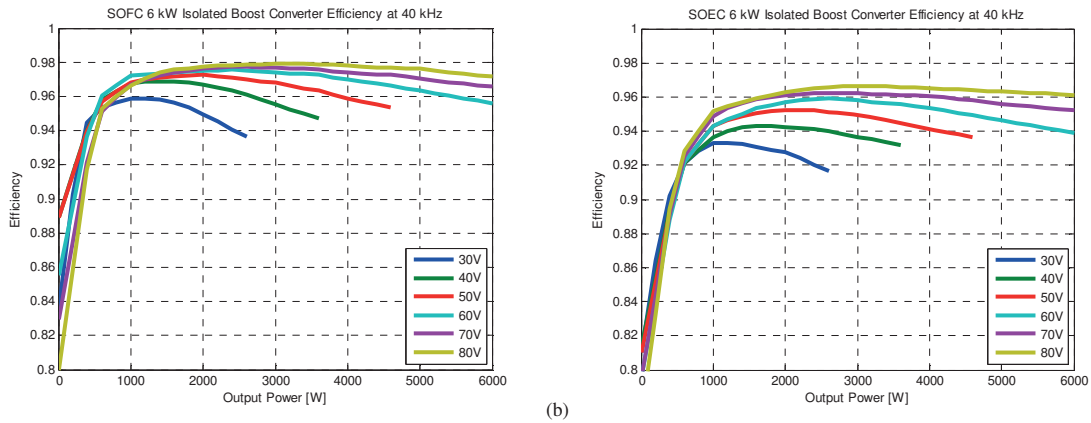


Fig. 2. Developed prototype of the dc-dc converter (a) and switching waveforms (b) at 60 V 40 A on the low voltage side and 750 V on the high voltage side in SOFC mode. Ch.1(yellow): $V_{ce,IGBT}$ (350 V/div), Ch.2(red): $V_{ds,MOSFET}$ (50 V/div), Ch.3(blue): $I_{LV\ inductor,AC}$ (10 A/div), Ch.4(green): $I_{HV,transformer}$ (5 A/div). Time 5μs/div.



(a) (b)

Fig. 3. Measured dc-dc converter efficiency for SOFC (a) and SOEC (b), 30-80 V and 0-6000 W.

IV. Influence of DC/DC Converter Efficiency on System Performance

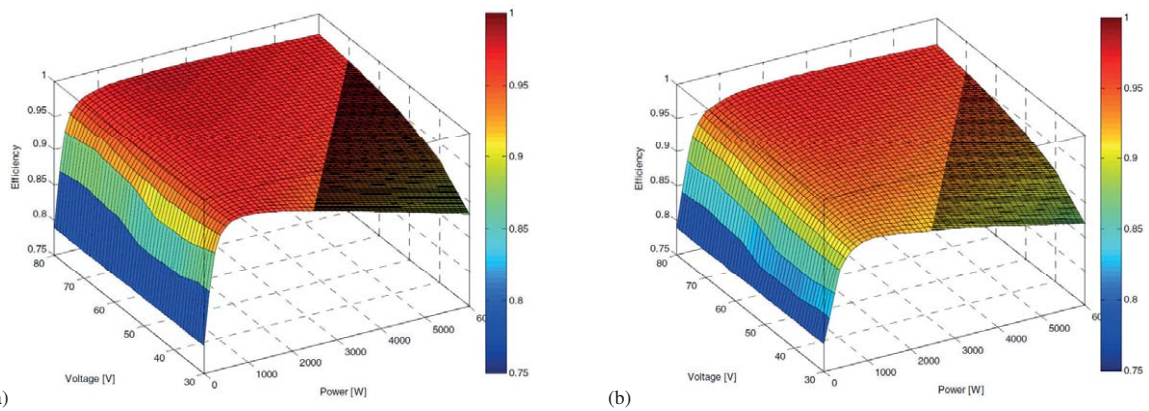
In power electronics dc-dc and dc-ac converters efficiency is often characterized as a function of the output power for different input voltage levels [4]. This type of characterization is commonly used for solar inverters, converters for wind power and also for commercial power adapters. The conventional characterization [4] does not take into account the surrounding system around the dc-dc converter and therefore, the impedance of the energy source; the converter efficiency can vary due to different operating conditions depending on the application. As the current from the fuel cell increases, its terminal voltage decreases and the dc-dc converter efficiency is typically reduced. When the fuel cell is operated as an electrolyzer cell, the cells stack terminal voltage increases as the current and the power increase. For this reason two types of converter characterization are presented: a conventional one and a load dependent one that takes into account the nature of the source.

A. Modeling and Simulation Method

The methodology used for the analysis is based on experimental measurements and results. A dc-dc converter was designed and prototyped; its performance in efficiency terms was characterized based on a conventional efficiency characterization [4]. The RFC parameters and model were extracted from measurements on RFC prototypes. The models were combined in order to obtain an efficiency characterization of the dc-dc converter that includes the source impedance. As a last step, the dc-dc converter efficiency was compared and validated with the calculations performed during the design phase of the dc-dc converter (a MATLAB script was used to perform the calculations and estimate the dc-dc converter efficiency).

B. Efficiency Characterization of the Converter Prototype

The developed converter prototype, Fig. 2a, is characterized for the entire voltage range on the RFCs side (30-80 V). The high voltage side is fixed to 750 V (constant) since it is connected to a dc-ac converter and its control loop maintains the dc-link voltage constant. The power flow direction affects the efficiency. When the power flow is from the low voltage to the high voltage side (SOFC), the power flows through the low voltage MOSFETs and then through the SiC diodes. Vice versa, when the power flow is reversed, on the high voltage side the power flows through the Si IGBTs and on the low voltage side through the MOSFETs (active rectification).



(a) (b)

Fig. 4. Measured dc-dc converter efficiency for SOFC (a) and SOEC (b), 30-80 V and 0-6000 W. Measured values have been interpolated in order to obtain an efficiency surface plot. Darkened area represents a forbidden operating condition for the dc-dc converter (current overload).

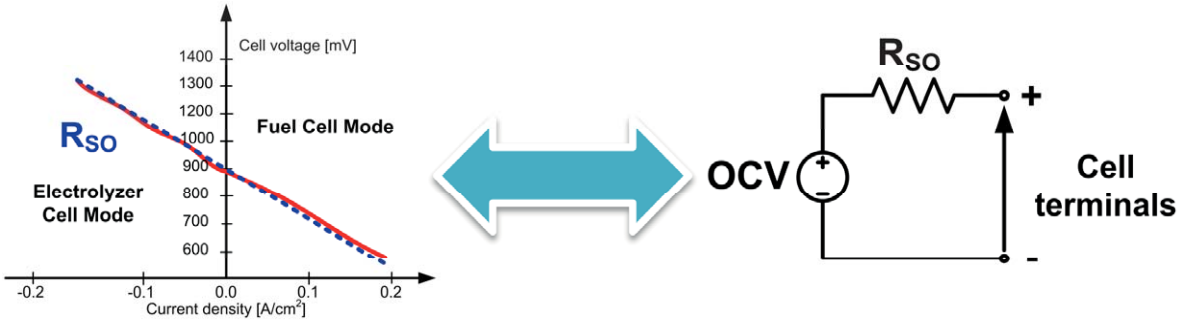


Fig. 5. Measured steady-state characteristics (in red on the left graph, low frequency) of a single SOFC/SOEC cell and simplified equivalent electrical model used for characterizing the efficiency of the dc-dc converter prototype.

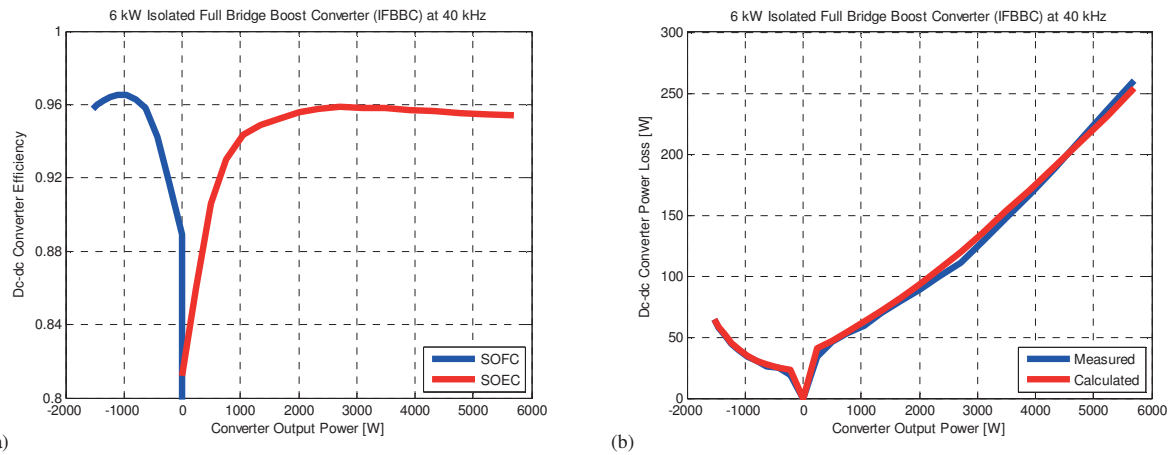
It is observed that in SOFC mode, Fig. 3a, the converter efficiency is significantly higher than in SOEC mode, Fig. 3b. This is explained by the fact that in SOEC mode the power flows through the IGBTs and these devices generate a significant amount of losses (both conduction and switching losses). As expected, as the voltage on the RFC converter port increases also the converter efficiency increases for the same power level. In this case, the conduction losses decrease as well as the switching losses. At low input voltages the maximum power is limited by the maximum converter current (e.g. Fig. 3a and Fig. 3b 30 V characteristics). With this conventional characterization the converter peak efficiency is about 97.8% in SOFC mode and 96.8% in SOEC mode (including the power required for the gate drivers and the control). The measurements are imported in MATLAB and interpolated for obtaining the complete efficiency characteristic of the converter prototype (Fig. 4a and Fig. 4b).

C. Introducing the RFCs Model into the Efficiency Characterization

The RFC stack model is introduced to determine the converter efficiency in a real application scenario. Based on the SO-cells I-V characteristic (Fig. 5) it is observed that the electrical behavior of the cells stack is like a voltage source with a series impedance. Since the RFC stack is composed of 50 series connected cells, the series impedance will be the sum of the series impedance of the single cells. The model series impedance is dominated by the resistive component which is will determine the static I-V characteristic of the RFC stack, Fig. 5. The I-V characteristics of the RFC stack is determined based on the I-V characteristics of single cells; this results in a stack open circuit voltage (OCV, Fig. 5) of 46.3 V and a series resistance (R_{SO}) of 0.3125 Ω. These parameters for the SO-cells stack are obtained from measurements performed on two sample stacks of 10 and 20 cells.

This simple model is included in the original efficiency measurements to determine the dc-dc converter efficiency when this is connected to the RFC stack. The dc-dc converter will never operate in all possible cases presented on Fig. 4a and Fig. 4b, but it will only operate on a line that describes the I-V characteristics of the RFC on the surfaces of Fig. 4a (SOFC mode) and Fig. 4b (SOEC mode). This line is plotted in 2D, Fig. 6a, giving a clearer view on the real dc-dc converter efficiency when connected to the RFC. It becomes clear that even if the dc-dc converter has a peak efficiency of 97.8 %, in the real application its maximum efficiency is limited to 96.4% in FC-mode and 95.9% in EC-mode (Fig. 6a).

In the presented characteristics it is observed that positive power flow in Fig. 6a indicated that the system is operating in SOEC mode vice versa for negative power flow the system operated in SOFC. The efficiency dip at low power levels is caused by the low power processed by the dc-dc converter.



(a) (b)

Fig. 6. (a) Measured dc-dc converter efficiency including model of the cells stack and (b) comparison of the measured and calculated dc-dc converter power loss.

Even though the overall converter losses are low they represent a large component in the overall power processed by the converter. The new presented characteristics can be used for operating the system around its maximum efficiency and obtaining better system performance.

D. Dc-dc Converter Modeling and Analysis

During the design phase the different components of the converter losses were analyzed in detail. The loss calculations for the magnetic components were based on the generalized Steinmetz equation (GSE [9]) and on Dowel's equations for taking into account ac-resistances in the inductor and transformer windings, [10]. The switching losses of the MOSFETs (power semiconductors on the RFC stack side) are calculated based on inductive driven commutation [11]. On the high voltage side the losses are calculated based on datasheet values and on switching loss reference measurements [12]. The calculated converter efficiency is compared to the measured one and the dc-dc converter losses are presented on Fig. 6b. It is observed that there is a good match between the two curves in Fig. 6b; this indicated that it is possible to predict the converter efficiency with fair accuracy. A mismatch is observed especially at low power levels where power semiconductor switching losses and inductive component core losses are dominating. This is due to the simplifications used in the models that assume fixed components operating temperature while in a converter prototype temperature varies continuously depending on the converter operating point.

E. High Dc-dc Efficiency System Operation

It is desirable to operate the system at high efficiency in order to have the lowest energy loss in a storage-generation complete cycle. In fact, every storage-generation cycle, energy flows through the dc-dc converter twice having a strong impact on the system performance in both terms of energy efficiency and profitability.

For this reason, the presented system in Fig. 1 has to be operated in order to have the highest number of sub-systems operating close to their maximum efficiency. In each sub-system maximum dc-dc electrical efficiency is defined by the characteristics on Fig. 6a (500-1500 W for SOFC and 1500-5500 W for SOEC). Having wide windows with high dc-dc conversion efficiency increases system controllability and efficiency for various power levels. A flat dc-dc converter efficiency curve represents a good converter design however, this is especially challenging in SOFC mode. Operating each subsystem at low power levels (range 0-500 W) would not result in a good overall system efficiency since the low dc-dc converter efficiency at this point would significantly impact the overall system efficiency.

In this application, the realized converter prototype has peak efficiencies of 95.9% and 96.4% depending on the converter operating point. Since efficiency is one of the major concerns for this application, the replacement of the high voltage power semiconductors with SiC JFETs or SiC MOSFETs would be beneficial in order to further increase the dc-dc converter efficiency. However, this will significantly increase the cost of the dc-dc converter due to the more expensive power devices and gate drivers [13].

CONCLUSIONS

The paper presented an energy storage system for renewable energy applications based on regenerative fuel cells. A high efficiency dc-dc converter prototype was presented and experimentally characterized in efficiency terms. The influence of the dc-dc converter efficiency was discussed and a new dc-dc converter load-dependent efficiency curve was presented. The converter has peak efficiencies of 97.8% and 96.8% depending on the power flow direction. The paper highlight that load-dependent converter efficiency is a key factor for having high system efficiency and the I-V characteristics limits the converter efficiency to 96.4% in fuel cell mode and to 95.9% in electrolyzer cell mode.

REFERENCES

[1] J. D. Maclay, J.Brouwer, G. S.Samuelsen, "Dynamic modeling of hybrid energy storage systems coupled to photovoltaic generation in residential applications", 2007 Journal of Power Sources, vol.163, issue 2, pp. 916-925.

[2] X. Yu, M.R. Starke, L.M. Tolbert and B. Ozpineci; "Fuel cell power conditioning for electric power applications: a summary" *IET Electric Power Applications*, 2007, vol.1, no.5, pp. 643–656, Sept. 2007.

[3] Zhang, Zhe; Pittini, Riccardo; Andersen, Michael A.E.; Thomsen, Ole C.; "A Review and Design of Power Electronics Converters for Fuel Cell Hybrid System Applications", *Energy Procedia 2012*, Volume 20, pp. 301-310.

[4] Nymand, M.; Andersen, M. A E, "A new very-high-efficiency R4 converter for high-power fuel cell applications," *2009 International Conference on Power Electronics and Drive Systems(PEDS)*, pp.997-1001, 2-5 Nov. 2009.

[5] Vaisanen, V.; Riipinen, T.; Silventoinen, P.; , "Effects of Switching Asymmetry on an Isolated Full-Bridge Boost Converter," , *IEEE Transactions on Power Electronics*, vol.25, no.8, pp.2033-2044, Aug. 2010.

[6] Mihalic, F.; Hren, A., "Safe start-up procedures of isolated bi-directional DC-DC converter," *2010 14th International Power Electronics and Motion Control Conference (EPE/PEMC)*, pp.T2-67,T2-173, 6-8 Sept. 2010.

[7] Zhu, L.; Kunrong Wang; Lee, F.C.; Jih-Sheng Lai, "New start-up schemes for isolated full-bridge boost converters," *IEEE Transactions on Power Electronics*, vol.18, no.4, pp.946,951, July 2003.

[8] Lindberg-Poulsen, K.; Ouyang, Ziwei; Sen, G.; Andersen, M. A E, "A new method for start-up of isolated boost converters using magnetic- and winding-integration", *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp.340,345, 5-9 Feb. 2012.

[9] Ouyang, Ziwei; Thomsen, O.C.; Andersen, M. A E, "Optimal Design and Tradeoff Analysis of Planar Transformer in High-Power DC–DC Converters," *IEEE Transactions on Industrial Electronics*, vol.59, no.7, pp.2800,2810, July 2012.

[10] P. L. Dowell, "Effects of eddy currents in transformer windings," *Proceedings of IEEE*, vol.113, no.8, August 1966, pp. 1387-1394.

[11] Ziwei Ouyang; Sen, G.; Thomsen, O.C.; Andersen, M. A E, "Analysis and Design of Fully Integrated Planar Magnetics for Primary–Parallel Isolated Boost Converter," *IEEE Transactions on Industrial Electronics*, vol.60, no.2, pp.494,508, Feb. 2013.

[12] Pittini, R.; D'Arco, S.; Hernes, M.; Petterteig, A.; , "Thermal stress analysis of IGBT modules in VSCs for PMSG in large offshore Wind Energy Conversion Systems," *Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011)*, pp.1-10, Aug. 30 2011-Sept. 1 2011.

[13] Pittini, Riccardo;Zhang, Zhe; Andersen, Michael A.E.; "Switching Performance Evaluation of Commercial SiC Power Devices (SiC JFET and SiC MOSFET) in Relation to the Gate Driver Complexity", *ECCE Asia DownUnder 2013*, pp.233,239, 3rd-6th June 2013.

Appendix F

SiC JFET Cascode Loss Dependency on the MOSFET Output Capacitance and Performance Comparison with Trench IGBTs

2013 Applied Power Electronics Conference and Exposition (APEC 2013)

SiC JFET Cascode Loss Dependency on the MOSFET Output Capacitance and Performance Comparison with Trench IGBTs

Riccardo Pittini
Technical University of Denmark
Dept. of Electrical Engineering
Kgs. Lyngby, 2800, Denmark
ripit@elektro.dtu.dk

Zhe Zhang
Technical University of Denmark
Dept. of Electrical Engineering
Kgs. Lyngby, 2800, Denmark
zz@elektro.dtu.dk

Michael A.E. Andersen
Technical University of Denmark
Dept. of Electrical Engineering
Kgs. Lyngby, 2800, Denmark
ma@elektro.dtu.dk

***Abstract*— In power electronics there is a general trend to increase converters efficiencies and power densities; for this reason new power semiconductors based on materials such as Silicon Carbide (SiC) and Gallium Nitride (GaN) are becoming more popular. This is especially valid for renewable energies applications where the generated energy has a higher cost than with conventional energy sources. This paper proposes an experimental analysis of the switching performance of a high voltage SiC JFET connected in cascade connection with a low voltage MOSFET. The analysis focuses on the influence of the MOSFET output capacitance on the switching performance of the SiC Cascode connection in terms of switching energy loss, *dV/dt* and *dI/dt* stresses. The Cascode connection switching performances are compared with the switching performance latest Trench IGBTs. The analysis is based on a set of several laboratory measurements and data post-processing in order to properly characterize the devices and quantify whether the SiC JFET Cascode connection can provide good performances with a simple MOSFET gate driver.**

I. Introduction

In the last years a large growth of power electronics has been experienced mainly driven by the huge interest in renewable energy sources and smarter energy use. Moreover, in many applications there is and increasing trend to improve systems efficiencies supported by state policies and by economical benefits.

Silicon Carbide (SiC) together with Gallium Nitride (GaN) have been known to be attractive wide band gap semiconductors especially suited for increasing the efficiency and power density of switch mode power supplies (SMPS) compared to silicon (Si) based SMPS [1]. They have the potential of providing power semiconductors characterized by high band-gap, higher mobility and higher thermal conductivity than Si, leading to lower conduction and switching losses, higher breakdown voltage, possibility to operate at high temperatures, increased switching frequency and power density.

The recent improvements in the crystal fabrication, fabrication yield increases and availability of new low-cost power devices based on SiC have made SiC-based power semiconductors more competitive [2][3]. However, there are still a limited number of power semiconductors available in SiC; they are limited to SiC Schottky barrier diodes, SiC Junction Effect Field Transistors (JFETs) available in both normally-on and normally-off variants, SiC Bipolar Junction Transistors (BJTs) [4] and recently SiC Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) [5][6].

SiC-diodes have become price competitive as Si-diodes; SiC-diodes are often used as replacement of Si-diodes in applications characterized by high efficiency and high voltage due to their almost zero-recovery losses at device turn-off [7]. SiC JFETs have really become price competitive and they can provide very low switching losses and low on-state resistance [8]. The main drawbacks related to the use of SiC JFETs are related to the driving circuitry: SiC JFETs are voltage driven devices with threshold and driving voltages that differ from Si-MOSFETs. Moreover, SiC JFETs require a low continuous power from the driver (high leakage current) and therefore they do not represent a direct and easy replacement for Si-MOSFETs or Silicon Insulated Gate Bipolar transistors (Si-IGBTs). The driver complexity [9] and the limited the availability of commercial drivers suited for Si-JFETs also contribute to limit the device diffusion in different applications. The driver issue in terms of continuous power from the driver is even worse for SiC-BJTs moreover, the limited availability of SiC-BJTs have also reduced their success. During 2011, SiC-based MOSFETs has been released thorough commercial channels [5]; the devices have with similar ratings as SiC JFETs promising good performance making the devices suited for significantly increase the switching frequency and the power density of power electronics converters. However, also in this case to properly take advantage of the new device a custom designed driver is required and it will probably limit the device diffusion due to the lack of commercial available drivers.

978-1-4673-4355-8/13/$31.00 ©2013 IEEE

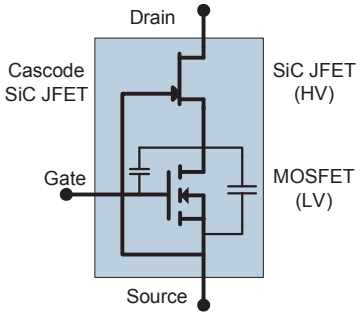


Fig. 1 High voltage (1200 V 85 mOhm, normally ON) SiC JFET in Cascode connection with a low voltage (60 V 1.5 mOhm) MOSFET showing the MOSFET's output capacitances .

One common solution for easily driving SiC JFETs require using a low voltage MOSFET series connected with the SiC JFET in a Cascode connection [10]. The Cascode allows creating a high voltage valve that can be easily driven with a simple and commercially available MOSFET driver. The main drawbacks of the solution are that requires an additional low-$R_{DS,on}$ MOSFET which increases the conduction losses and has a tendency to oscillations especially at turn-off increasing the overall switching losses.

This paper focuses on performing an analysis based on experimental results of the influence of the low voltage MOSFET's output capacitance on the switching performance of the SiC JFET Cascode configuration. The analysis focuses on switching energy loss, transition times and maximum stresses in terms of *dV/dt* and *dI/dt*. Moreover, the paper also presents a comparison of the switching losses of the Cascode SiC JFET configuration with the switching performance of recent Trench IGBTs with similar ratings as the Cascode. The typical application is a 5 kW DC/DC isolated boost converter for fuel cell where the low voltage (~50 V) primary stage is designed based on MOSFETs and the high voltage (700-800 V) stage is designed based on IGBTs or SiC devices.

II. JFET CASCODE CONFIGURATION

The circuit showing the SiC normally-on JFET in Cascode connection with a low voltage MOSFET is presented in Fig. 1. The Cascode connection allows using normally-on JFETs for creating normally-off valves which are desirable in many applications where in case of failure on the gate driver a normally-on valve would create a critical and dangerous condition (e.g. short-circuit in a voltage source converter). The scalability of the Cascode connection has also been proven [11] making the Cascode connection a possible candidate for realizing high voltage SiC switches.

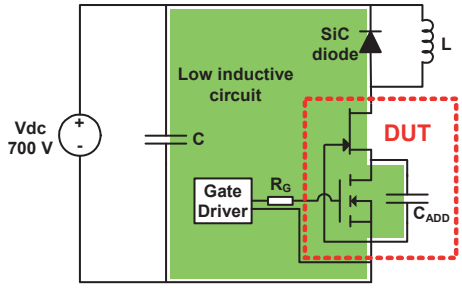


Fig. 2 Inductive clamp test circuit. Highlighted in green the leakage inductance critical loop.

When the voltage applied to the MOSFET gate-source is below the MOSFET's threshold, the valve is in off-state or blocking mode. The gate of the JFET is connected to the source of the MOSFET; when a low voltage is applied across the valve drain-source the MOSFET will support most of the voltage but as soon and the voltage over the valve is increased the JFET becomes pinched off and it will support most of the voltage. The valve can be turned on by applying a voltage greater than the MOSFET's threshold across the MOSFET's gate-source. As soon as the MOSFET turns on it will subsequently, the voltage applied to the JFET's gate-source will become low turning on the JFET. In this case the JFET's turn-on/turn-off are delayed compared to the MOSFET's turn-on/turn-off.

III. SETUP CONFIGURATION AND TESTED DEVICES

The test setup is a simple pulse clamped inductive circuit shown in Fig. 2. The inductive provides an easy way to test power devices up to their nominal ratings without heating them up. To perform this, the Device Under Test (DUT), is turned on for a small time interval, during this interval the current through the load inductor (L) builds up and the desired value is reached, the DUT is turned off (Fig. 3). At this interval is possible to measure the device switching losses for the selected current value. Immediately after that the device has been turned it is possible to turn it on again. When the

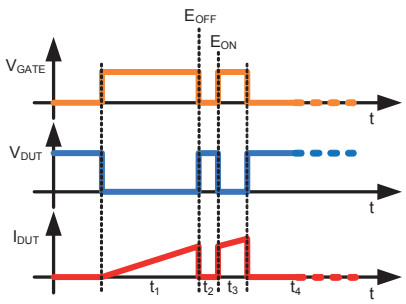


Fig. 3 Ideal double pulse testing waveforms.

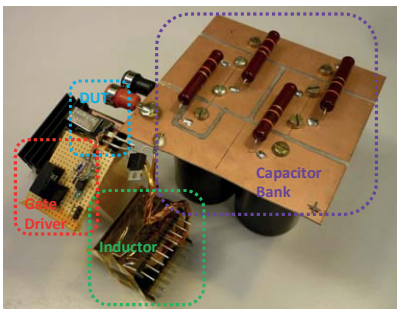


Fig. 4 Hardware used for the tests. Highlighted the capacitor bank, the inductor, the gate driver and the DUT.

TABLE I
TESTED DEVICE CHARACTERISTICS

JFET SJDP120R085	MOSFET IPB017N06N3	IGBT no.1 IGW15N120H3	IGBT no.2 IRG7PH30K10
1200 V	60 V	1200 V	1200 V
85 mOhm	1.7 mOhm	2.05 Vce	2.05 Vce
27 A*	180 A*	30 A*	33 A*
17 A**	180 A**	15 A**	23 A**

*Parameter at 25 ° C
**Parameter at 100 ° C

device off-time is sufficiently low, the inductor current decay is small (the inductor discharges slightly through its resistance and through the freewheeling diode) and allows turning on the DUT for measuring a turn-on event at the same current level as the turn-off event. After this second turn-on event the device is switched off permanently and kept in off state until the inductor is completely discharged. After that it is possible to vary the first pulse width to increase or reduce the desired current and at which the measurement should be performed.

The test setup (Fig. 4) characteristics are summarized:

- DC voltage source: 700 V
- Capacitor bank: 1000 V 300 µF
- Load inductor: 285 µH
- Freewheeling diode: SiC 1200 V 20 A

A. Tested Devices

The paper focused on analyzing devices with similar characteristics in order to establish references for converters with DC voltages of 700-800 V. At this voltage levels CoolMOS provide a limited voltage margin (available up to 900 V) and their on state resistance is significantly high compared to SiC devices or Si IGBTs. Since for the candidate application efficiency is one of the most important factors, 1200 V SiC JFETs (SJDP120R085) were one of the first candidates for achieving high efficiency. Alternatively, 1200 V SiC MOSFETs could have been used however, the price performance ratio of the SiC JFET looked well application-suited. The low voltage MOSFET was selected due its very low on resistance (IPB017N06N3) that would give a minimum impact on the total on state resistance of the Cascode connection. The large availability of IGBT devices in the 1200 V range made the selection of IGBTs more complex. However, among all, trench IGBTs can provide both fast switching with limited tail current and low $V_{CE,on}$. The selected devices have similar current ratings as the selected SiC JFET and are produced by two different manufacturers identified as IGBT no.1 (IGW15N120H3) and IGBT no.2 (IRG7PH30K10) in the measurements and in the comparison plots. A summary of the main device characteristics is presented on Table I.

B. Instrumentation and Measurements

All measurements were performed with the comparable test conditions in terms of voltage, current, time intervals and temperature. The power connection from the DC-link capacitor to the power components was realized with flat copper conductor to obtain as low inductance as possible as visible on Fig. 4. The gate driver was placed close to the DUT, the wires were twisted in order to reduce the loop inductance and it was connected to a digital control card used to generate test pulses. The minimum resolution of the pulses is 1 µs with a basic accuracy of 0.25 µs. The digital control card ensured test repeatability having well defined pulses width for each current level. All measurements were performed with the same probe configuration with an exception for the IGBT measurements where there was no MOSFET's drain-source voltage measurement.

The oscilloscope features allow saving measurements directly in Matlab format for post-processing. The oscilloscope configuration was the following (examples of measured switching transients on Fig. 5):

- Ch.1: DUT source/emitter current. Current probe is a ultra miniature Rogowsky coil with a bandwidth of 20 MHz (20mV/A) measuring the Cascode source current excluding the gate driving current.
- Ch.2: Gate-source/gate-emitter voltage of the Cascode configuration/IGBTs; 100 MHz 1X voltage probe.
- Ch.3: DUT drain-source/collector-emitter voltage. High voltage probe 100X (LeCroy PPE 4 kV) measuring the Cascode drain-source voltage.
- Ch.4: drain-source voltage of the low voltage MOSFET in the Cascode configuration;100 MHz 1X voltage probe. Not used with IGBT's.

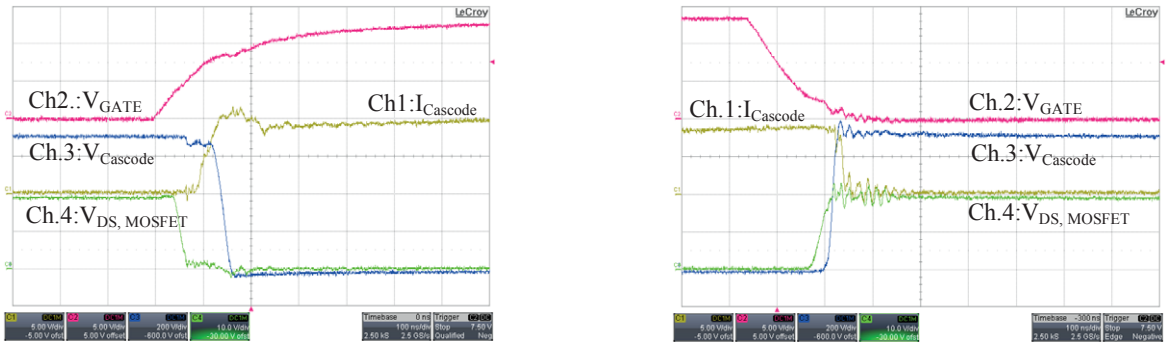


Fig. 5 Cascode JFET measured turn-on (left) and turn-off (right) detail 700 V 9 A, MOSFET gate resistance 2.5 ohm. Ch.1: 5 A/div, Ch.2: 5 V/div, Ch.3: 200 V/div and Ch.4: 10 V/div, time: 100 ns/div.

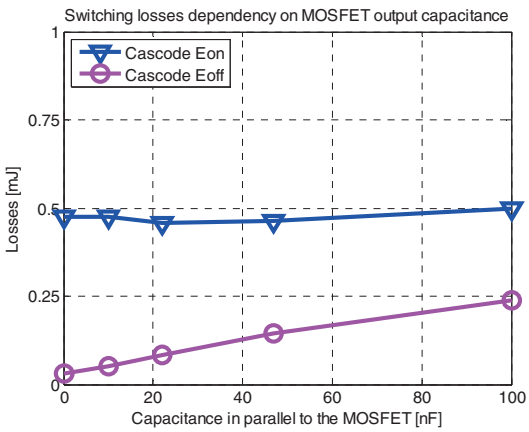


Fig. 6 Cascode switching loss dependency on MOSFET's output capacitance.

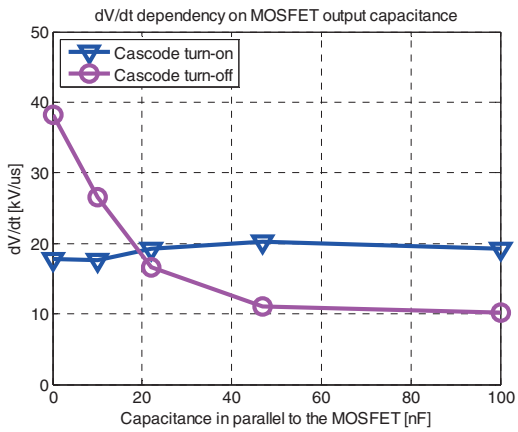


Fig. 7 Cascode *dV/dt* stress dependency on MOSFET's output

The Rogowsky coil delay was measured in a reference comparison measurement with a shunt resistor where it was quantified in 24 ns; this value is verified also in probe manual. The oscilloscope features de-skew compensation, however, this was not used but implemented digitally during data post-processing. Measurements were performed at different current levels (from 5 A to up to 20 A) for the selected DC voltage (700 V).

C. Methodology and Data Post-Processing

The first set of measurements focused on analyzing the effect of the MOSFET output capacitance on the switching performance of the Cascode configuration. The main focus was to observe if it is possible vary the switching performance with simple low voltage components instead of using components rated at high voltage [11]. To simulate a large MOSFET's output capacitance, additional capacitors of different values (0-100 nF range) were added in parallel to the low voltage MOSFET used in the Cascode connection. The capacitors were connected directly on the MOSFET's leads in order to reduce the leakage inductance to the minimum and to avoid possible unwanted oscillations. In the second step, the switching performance of the Cascode valve were measured at different current levels and as last phase the Cascode valve was replaced with the selected IGBTs for characterizing their switching performance.

All measured waveforms were stored in MATLAB format in order to allow post-processing of the measurements and create adequate plots. Light filtering was applied to the measurements for reducing the measurement noise; after filtering the waveforms were verified to ensure that the filtering process did not change the measurement information. MATLAB functions were developed for extracting the desired information from the measurement files, such as switching energy loss, the transition intervals (turn-on and turn-off times), the voltage and current stresses in terms of *dV/dt* and *dI/dt* and instantaneous peak power loss.

IV. Cascode Switching Loss Dependency on MOSFET's Output Capacitance

In the first set of measurements the switching losses of the Cascoded devices are measured by varying the MOSFET's output capacitance for a fixed current (9 A). For reasonably low additional capacitances (0-100 nF range) the turn-on losses have a minimal dependency on the MOSFET's output capacitance as observed in Fig. 6. In this case, at the Cascode turn-on the MOSFET's delay and switching speed determine the turn-on instant of the JFETs. The turn-off losses on Fig. 6 increase more than the turn-on losses, in fact as the MOSFET's output capacitance increases, the turn-off losses increase with a linear trend. This could be explained by analyzing the Cascode configuration a bit more in detail.

At device turn-on the MOSFET's output capacitance discharges through the low ohmic low voltage MOSFET and the voltage change across the JFET's gate-source (also output capacitance terminals) varies as in a capacitor discharge through a resistor with the RC-time constant defined by the MOSFET's output capacitance and the MOSFET's on-state resistance.

Vice versa, at device turn-off the MOSFET's output capacitance is slowly charged through the JFET's on-state resistance; at the start of the JFET's turn-off process the

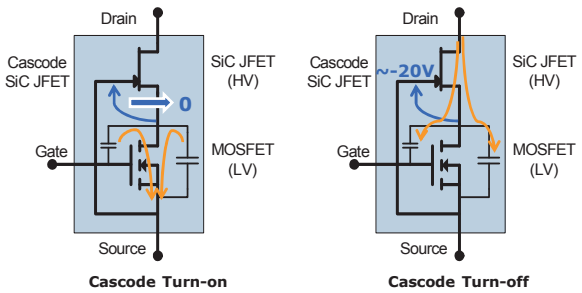


Fig. 8 Cascode turn-on (left) and turn-off (right) transients. Highlighting charge/discharge of MOSFET's output capacitance.

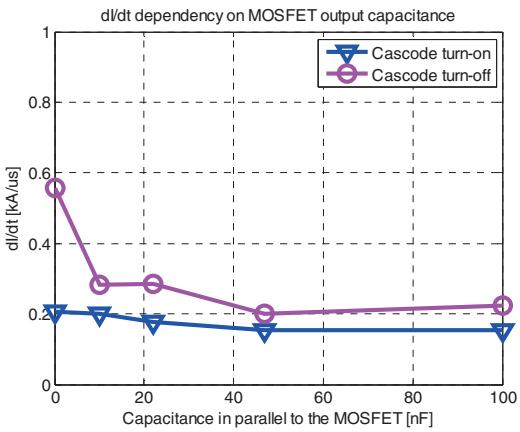


Fig. 9 Cascode *dI/dt* stress dependency on MOSFET's output capacitance.

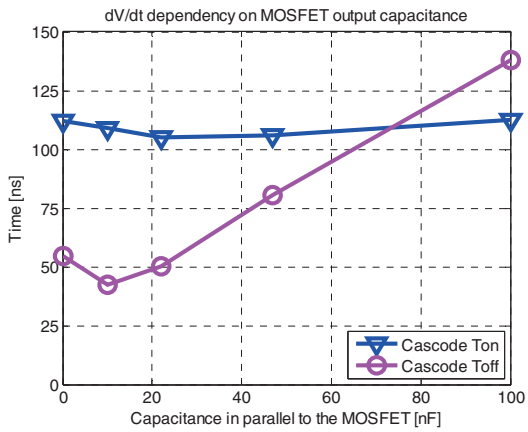


Fig. 10 Cascode turn-on and turn-off times dependency on MOSFET's output capacitance.

voltage rises over the MOSFET with an initial RC time constant defined by the JFET's on state resistance and the total output capacitance. As soon as the voltage over the MOSFET's start to increase, the JFET's on resistance increases giving an additional contribute to the JFET's turn-off losses until the JFET becomes completely pinched off. For this reason, an increase of the MOSFET's output capacitance slightly influences the Cascode turn-on performance and will strongly influence the turn-off performance.

This effect is also observed in the *dV/dt* stress at device turn-on and turn-off on Fig. 7. The *dV/dt* stress at turn-on is slightly influenced by the MOSFET's output capacitance while the *dV/dt* stress at turn-off is significantly reduced with a large MOSFET's output capacitance. The *dV/dt* stress reduction at turn-off is large, in fact the *dV/dt* stress is reduced from 38 kV/us down to 10 kV/us with the largest tested capacitance value. According to the measurement a small capacitor can be placed on parallel to the low voltage MOSFET to reduced the turn-off *dV/dt* and balance it with the turn-on *dV/dt* reducing the immunity requirements for the gate driver. However, it is also necessary to observe how other parameters are affected by a large MOSFET output capacitance.

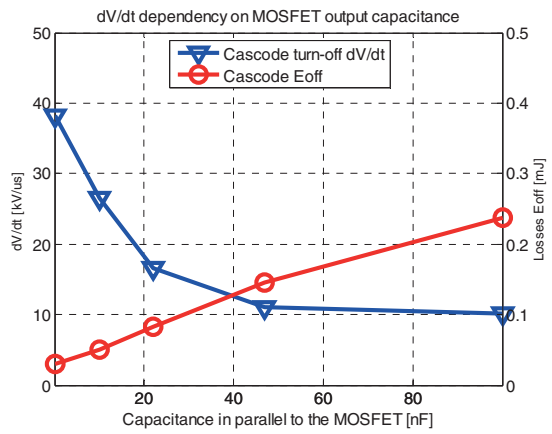


Fig. 11 Cascode turn-off switching loss and *dV/dt* dependency on MOSFET's output capacitance.

It is also interesting to observe how the *dI/dt* stress varies as a function of the MOSFET's output capacitance. On Fig. 9 it can be observed that the turn-on *dI/dt* has a light variation (small reduction), however, large output capacitance mainly influences the turn-off *dI/dt*. This stress can be reduced down to about 33% or the initial value. Therefore, it can be deduced that a large MOSFET's output capacitance can reduce both *dV/dt* and *dI/dt* at turn-off. This result is also confirmed by taking a look at the transition times (turn-on and turn-off times) of the Cascode configuration on Fig. 9.

It was observed that in the Cascode configuration, the turn-on losses are dominating over the turn-off losses (Fig. 6 700 V 9 A); by increasing the MOSFET's output capacitance the Cascode turn-off time increase as seen in Fig. 11. Therefore, it is possible to find a balance between the turn-on *dV/dt* and the turn-off *dV/dt* with a slight increase of switching losses (Fig. 11). Depending on the application and on the desired performances in terms of switching losses and maximum *dV/dt* and *dI/dt* stresses, this could be advantageous for reducing the immunity requirements of the gate driver which are normally very high (recommended immunity for SiC gate drivers is about ~50 kV/us).

V. Comparison of the Switching Losses of SiC Cascode with Si IGBTs

In multi-kW applications with DC-link voltage level of 700-800 V SiC normally-on JFET in Cascode connection with a low voltage MOSFET has to be compared with newly developed high speed trench IGBTs which, especially for the latest series (3rd generation); these devices can provide very low $V_{CE,sat}$ and low switching losses (or operation up to ~100 kHz). The IGBTs switching performance were measured with different gate resistors values; starting with a large values as used in their datasheets (e.g. 35-22 Ohm), down to a very low values (2.5 Ohm). To analyze the switching performance, the turn-on and turn-off losses are analyzed independently for IGBT no.1 and IGBT no.2. Subsequently, the total switching

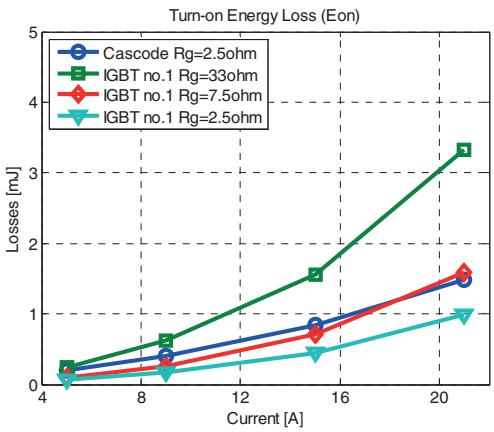


Fig. 12 IGBT no.1 and Cascode turn-on energy loss.

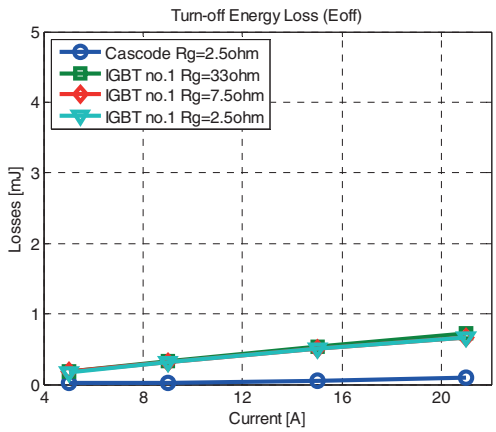


Fig. 13 IGBT no.1 and Cascode turn-off energy loss.

losses are analyzed in comparison with the Cascode configuration.

IGBT no.1 is a fast switching IGBT (IGW15N120H3) rated for operation up to 100 kHz; its turn-on and turn-off switching losses are presented on Fig. 12 and Fig. 13 respectively. When the IGBT is operated with large gate resistors as characterized in the datasheet, the switching losses losses are significantly higher than the SiC Cascode configuration. However, by reducing the gate resistor the turn-on losses are significantly reduced. With a minimum gate resistor the reduction can be down to 33% of the losses specified in the datasheet. The performance achieved in terms of turn-on losses are also better than the ones obtained with the SiC Cascode. Vice versa, the IGBT turn-off losses are independent form the gate resistance and vary linearly with the device current (Fig. 13). The turn-off losses are always larger than the SiC Cascode turn-off due to the IGBT tail current.

In a similar way the switching losses of IGBT no.2 are compared with the switching losses of the SiC Cascode on Fig. 14 and Fig. 15. The measured turn-on losses of IGBT no.2 are significantly lower than the ones measured for IGBT no.1 (Fig. 12 and Fig. 14) for large gate resistor values. Also in this case, with reduced gate resistors compared to the value specified in the datasheet, it is possible to reduce the IGBT turn-on losses even lower than the turn-on losses of the SiC Cascode. The turn-on losses with low gate resistors become lower than the SiC Cascode for all measured current levels. As observed in the previous case, the IGBT no.2 turn-off losses are almost not influenced by the reduction of the gate resistance and, also for this case, their value is significantly larger than the SiC Cascode turn-off losses for the entire range of tested currents. Therefore, it is observed that even though latest generation of trench IGBT have very low switching losses, the tail current is still one of the main sources of turn-off losses in IGBTs.

As observed until now is clear that when IGBTs are used up to their boundaries in terms of switching speed, they can provide good performances even in comparison to the new power semiconductors based on SiC. It is required to analyze the total switching losses (both turn-on and turn-off energy loss) to evaluate the overall performance of the devices. To achieve a complete comparison the total losses (turn-on and

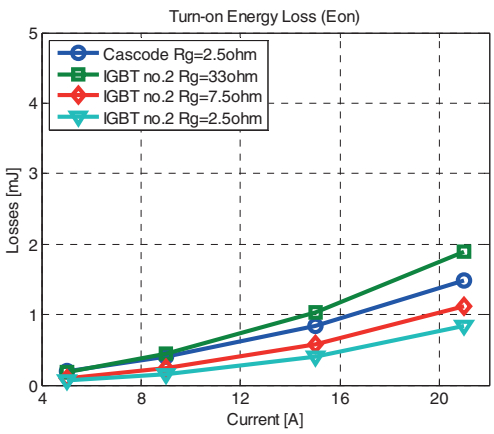


Fig. 14 IGBT no.2 and Cascode turn-on energy loss.

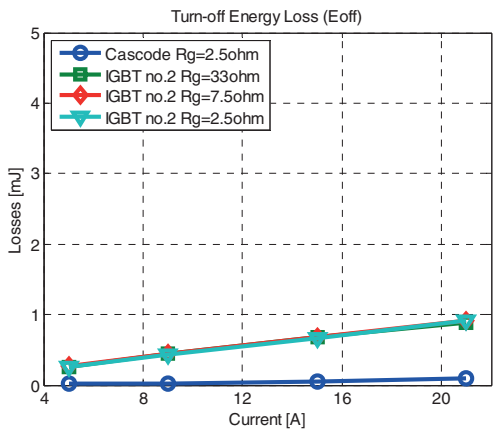


Fig. 15 IGBT no.2 and Cascode turn-off energy loss.

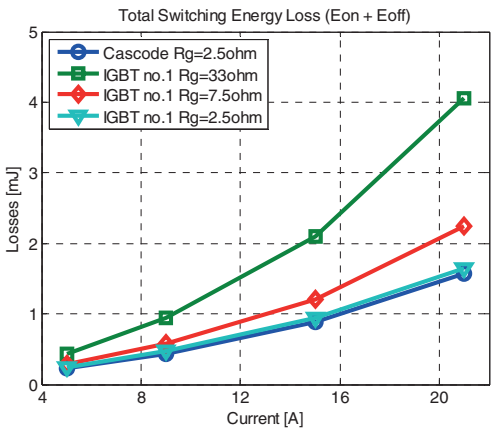


Fig. 16 IGBT no.1 and Cascode total switching energy loss.

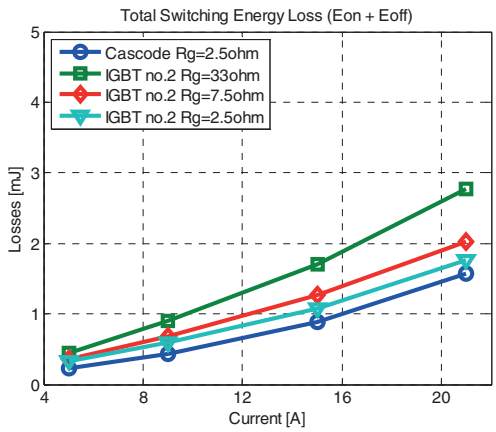


Fig. 17 IGBT no.2 and Cascode total switching energy loss.

turn-off) have to be evaluated.

A comparison of the total switching losses of IGBT no.1 with SiC Cascode and IGBT no.2 with SiC Cascode are presented on Fig. 16 and Fig. 17 respectively. Both IGBTs types are rated for high-speed (IGBT no.1 up to 100 kHz and IGBT no.2 up to 30 kHz), however, it is observed that IGBT no.1 has higher switching losses compared to IGBT no.2 when this ones are used with the gate resistors specified in the datasheet, this is observed especially at high current values (above 10 A). In both IGBTs it is possible to significantly reduce the total losses by decreasing their gate resistor to a very low value. In this case the energy loss reduction in IGBT no.1 is larger compared to IGBT no.2. The IGBTs switching performance can be increased to a level where the energy loss during the switching transient is very close to the one observed for the SiC Cascode (Fig. 16).

VI. Conclusions

The paper presented the effects of increased MOSFET's output capacitance on the switching behavior of the Cascode configuration.

It was observed that in the Cascode configuration the turn-off *dV/dt* stress can be significantly reduced with a limited increase of the switching losses by a larger MOSFET's output capacitance; e.g. by adding an additional capacitor in parallel to the MOSFET. The additional capacitor influences mainly the turn-off losses with little influence on the turn-on losses.

The Cascode configuration was characterized in terms of switching losses and compared with newly 3rd generation trench IGBTs. This latest IGBTs proved to be very competitive also towards SiC devices in the multi-kW power range. In fact, when IGBTs are switched very fast the measured switching losses are very close to the switching losses of a SiC Cascode configuration. Undoubtedly, pure SiC power devices provide lower losses, however, there is still a big lack of available integrated gate-driver solutions for these devices. For this reason, the Cascode configuration or latest IGBT generations are still very appealing for many applications.

References

[1] Elasser, A.; Chow, T.P.; , "Silicon carbide benefits and advantages for power electronics circuits and systems", Proceedings of the IEEE , vol.90, no.6, pp. 969- 986, Jun 2002.

[2] Ostling, M.; Ghandi, R.; Zetterling, C.; , "SiC power devices — Present status, applications and future perspective", IEEE 23rd International Symposium on Power Semiconductor Devices and ICs (ISPSD 2011), pp.10-15, 23-26 May 2011.

[3] Khan, M.A.; Simin, G.; Pytel, S.G.; Monti, A.; Santi, E.; Hudgins, J.L.; "New Developments in Gallium Nitride and the Impact on Power Electronics", IEEE 36th Power Electronics Specialists Conference (PESC '05), pp.15-26, 16-16 June 2005.

[4] Franke, W.-T.; Fuchs, F.W.; , "Comparison of switching and conducting performance of SiC-JFET and SiC-BJT with a state of the art IGBT", 13th European Conference on Power Electronics and Applications (EPE '09), pp.1-10, 8-10 Sept. 2009.

[5] http://www.cree.com/

[6] Fan Xu; Ben Guo; Tolbert, L.M.; Wang, F.; Blalock, B.J.; , "Evaluation of SiC MOSFETs for a high efficiency three-phase buck rectifier," Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2012), pp.1762-1769, 5-9 Feb. 2012.

[7] Ho, C.N.M.; Breuninger, H.; Pettersson, S.; Escobar, G.; Serpa, L.; Coccia, A.; , "Practical implementation of an interleaved boost converter using SiC diodes for PV applications," IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE & ECCE Asia 2011), pp.372-379, May 30 2011-June 3 2011.

[8] Wilhelm, C.; Kranzer, D.; Burger, B.; , "Development of a highly compact and efficient solar inverter with Silicon Carbide transistors," 6th International Conference on Integrated Power Electronics Systems (CIPS 2010), pp.1-6, 16-18 March 2010.

[9] Kelley, R.; Ritenour, A.; Sheridan, D.; Casady, J.; , "Improved two-stage DC-coupled gate driver for enhancement-mode SiC JFET," Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2010), pp.1838-1841, 21-25 Feb. 2010.

[10] Mihaila, A.; Udrea, F.; Azar, R.; Brezeanu, G.; , "Analysis of static and dynamic behaviour of SiC and Si devices connected in cascode configuration," Proceedings International Semiconductor Conference (CAS 2001), vol.2, pp.333-336 vol.2, Oct 2001.

[11] Biela, J.; Aggeler, D.; Bortis, D.; Kolar, J.W.; , "5kV/200ns Pulsed Power Switch based on a SiC-JFET Super Cascode," Proceedings of the IEEE International Power Modulators and High Voltage Conference, pp.358-361, 27-31 May 2008.

Appendix G

Switching Performance Evaluation of Commercial SiC Power Devices (SiC JFET and SiC MOSFET) in Relation to the Gate Driver Complexity

5th *Annual International Energy Conversion Congress and Exhibition (ECCE Asia DownUnder 2013)*

Switching Performance Evaluation of Commercial SiC Power Devices (SiC JFET and SiC MOSFET) in Relation to the Gate Driver Complexity

Riccardo Pittini
Technical University of Denmark
Dept. of Electrical Engineering
Oersteds Plads 349
Kgs. Lyngby, Denmark
ripit@elektro.dtu.dk

Zhe Zhang
Technical University of Denmark
Dept. of Electrical Engineering
Oersteds Plads 349
Kgs. Lyngby, Denmark
zz@elektro.dtu.dk

Michael A.E. Andersen
Technical University of Denmark
Dept. of Electrical Engineering
Oersteds Plads 349
Kgs. Lyngby, Denmark
ma@elektro.dtu.dk

***Abstract*—Silicon Carbide (SiC) power devices can provide a significant improvement of power density and efficiency in power converters. The switching performances of SiC power devices are often a trade-off between the gate driver complexity and the desired performance; this is especially true for SiC BJTs and JFETs. The recent introduction of SiC MOSFET has proved that it is possible to have highly performing SiC devices with a minimum gate driver complexity; this made SiC power devices even more attractive despite their device cost. This paper presents an analysis based on experimental results of the switching losses of various commercially available Si and SiC power devices rated at 1200 V (Si IGBTs, SiC JFETs and SiC MOSFETs). The comparison evaluates the reduction of the switching losses which is achievable with the introduction of SiC power devices; this includes analysis and considerations on the gate driver complexity and cost.**

Keywords—Silicon Carbide (SiC), SiC JFET, SiC MOSFET, Gate Driver, Switching losses.

I. INTRODUCTION

Research in power electronics has been driven by new renewable energies applications and requirements for smarter and more efficient energy use. In all these applications there is a trend to increase the system efficiency and therefore, the efficiency of the power electronics converters. The introduction of power devices based on wide band gap semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN), has allowed to increase the efficiency and power density of switch mode power supplies (SMPS) [1]. In the latest years improvements in the SiC crystal fabrication and fabrication yields has allowed cheaper SiC power devices and therefore, they have become more competitive towards their silicon (Si) competitors [2][3]. However, there is a limited number of commercially available SiC power devices: SiC Schottky barrier diodes, SiC Junction Effect Field Transistors (JFETs, available in both normally-on and normally-off variants), SiC Bipolar Junction Transistors (BJTs) [4] and, recently introduced, SiC Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) [5][6]. SiC-diodes have already become widely diffused in many applications thanks to their competitive price and quasi zero-recovery losses [7]; however, for other SiC power devices, their diffusion has been mostly limited by device and gate driver price and availability. Si IGBTs represent a mature technology, these devices dominate the active switch market are widely spread in most of medium-high power applications. Latest developed Si Trench IGBTs can operate up to 100 kHz switching frequency [8]. SiC JFETs and SiC MOSFETs are significantly more expensive than newly Si Trench IGBTs but they can provide a significant reduction of the switching losses in a converter [9][10]. The performance of SiC devices, in particular of JFETs, is a trade-off between the gate driver complexity and the switching performance therefore, gate drivers represents a key component when using SiC devices. Cascode connection [11] can reduce the gate driver complexity; however, this does not provide the best performance and introduces an additional power device.

This paper presents an analysis based on experimental results of the switching losses of various commercially available Si and SiC power devices rated at 1200 V (Si IGBTs, SiC JFETs and SiC MOSFETs). The comparison evaluates the reduction of the switching losses, which is achievable with the introduction of SiC power devices; moreover, this includes considerations and analysis on the gate driver complexity. SiC BJTs are not considered for the analysis due to their limited commercial availability. Results highlight that SiC JFETs with a tailored driver provide the lowest losses, while newest SiC MOSFET provides switching losses just above SiC JFETs but with a lower gate driver complexity. The study has been performed to investigate the possible performance enhancement that could be achieved by replacing Si IGBTs with SiC devices in a dc/dc converter tied to a three phase inverter (400 $V_{AC,RMS}$); the two converter share a DC bus rated at 700-800 V [12][13] therefore, measurements are performed at this voltage level.

II. SIC POWER DEVICES AND TESTED DEVICES

Si-based power semiconductors are still the most diffused devices among all power semiconductors available due to their low cost and thanks to a well-established technology. In the latest years SiC-based devices started to be commercialized

TABLE I
TESTED DEVICE CHARACTERISTICS

	Si IGBT IGW15N120H3	SiC JFET (on) SJDP120R085	SiC JFET (off) SJEP120R100	SiC MOSFET CMF20120D
$V_{DS,max}$	1200 V	1200 V	1200 V	1200 V
V_{CE} or $R_{DS,on}$	2.05 Vce	85 mOhm	100 mOhm	80 mOhm
I_C or I_D	30 A*	27 A*	30 A*	42 A*
I_C or I_D	15 A**	17 A**	17 A**	24 A**

*Parameter at 25 ° C
**Parameter at 100 ° C

and, due to technology improvements, their price has been significantly reduced and their availability increased. However, through the distributors channels there are a limited number of commercially available devices, these are limited to SiC Schottky diodes, SiC JFETs both normally-on (on-JFET), and normally-off (off-JFET) and, recently, SiC MOSFETs. Most of the devices are available in two main voltage ratings: 600 V and 1200 V.

The switching performance comparison is performed on four 1200 V devices: one Si IGBT and three SiC-based devices (Table I). The Si IGBT is used as state of the art reference for Si power devices, it is based on the latest Trench technology and designed for operating up to ~100 kHz (Infineon IGW15N120H3). Regarding the SiC power devices, they have been selected among the commercially available ones with similar current ratings as the Si IGBT. SiC JFETs both normally-on and normally-off (Semisouth SJDP120R085 and SJEP120R100 respectively) are tested; the normally-on devices are tested with a non-pulsed gate driver while the normally-off devices are driven with a pulsed gate driver which can strongly reduce the switching performance. The last SiC device is a newly SiC MOSFET from Cree (CMF20120D) which was recently introduced on the market in 2011.

One of the main concerns regarding new SiC power semiconductors it is the device availability; for this reason, the analysis considered only devices that have been commercialized on the market during 2012 and excluding the ones that are available only as engineering samples (e.g. SiC BJTs).

III. GATE DRIVER FOR SIC DEVICES

Gate drivers are probably the most important component after the power semiconductor itself. Driving SiC power semiconductors with not properly selected or tailored drivers would mean losing the possible performance enhancement that SiC devices can provide. Therefore, each power semiconductor (SiC JFETs, SiC MOSFETs and Si IGBTs on Table I) must to be tested with a driver that can properly highlight the device performance. It should be considered that the power semiconductor switching performance is often a trade-off with gate driver complexity. For example, Si-based devices such as IGBTs have minimal gate driver complexity, while gate driver complexity of SiC devices is slightly higher, Fig. 1.

The approach used in this paper considers two main gate driver topologies. A simple gate driver that drives the device under test (DUT) with two voltage levels (e.g. +15 V and 0 V or hv-gnd) through a gate resistor. This driver and its variants (different voltage levels) are used for driving Si IGBTs (Fig. 1a), SiC on-JFETs (Fig. 1b) and SiC MOSFETs (Fig. 1d). In

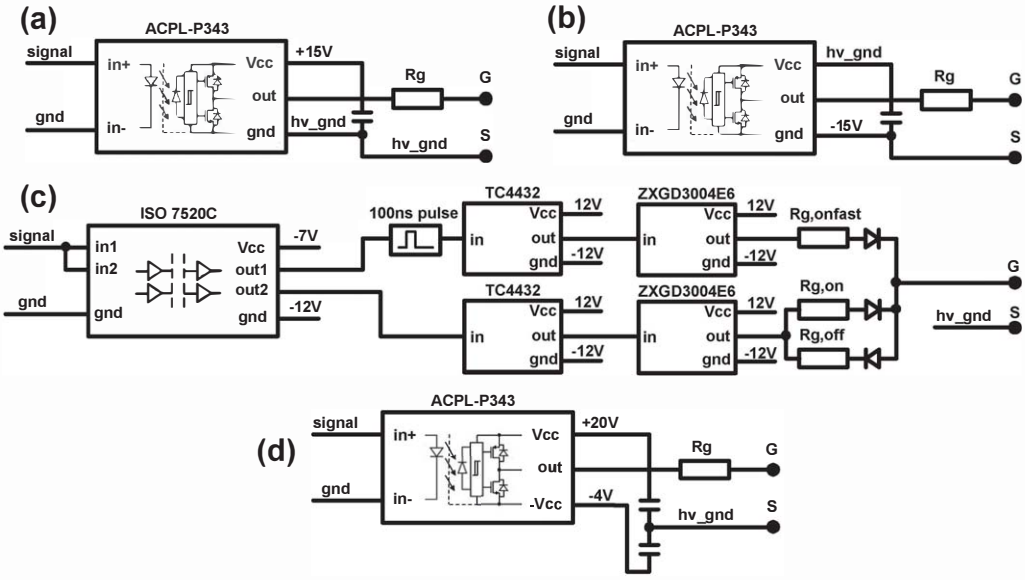


Fig. 1. Gate drivers used for testing the devices: IGBT gate driver (a), SiC on-JFET gate driver (b), SiC off-JFET gate driver (c), and SiC MOSFET gate driver (d).

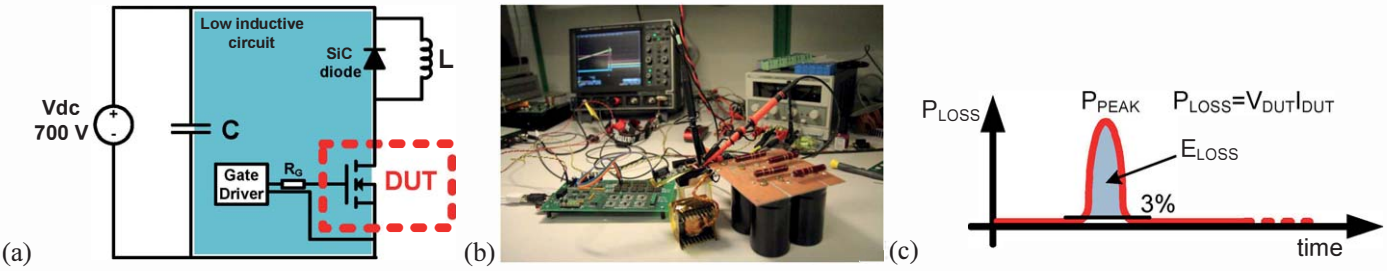


Fig. 2. Inductive clamp test circuit used for testing the devices (a) and overview of the test setup (b). Example of recorded waveforms of a SiC off-JFET turn-on switching transient with Rg=2.5 Ohm at 700 Vdc and 15 A(c), *100ns/div*. Picture showing how the switching loss energy is calculated (d).

these cases, the gate driver components are reduced minimizing also the complexity and cost of the circuitry. A more complex gate driver is used for SiC off-JFETs, Fig. 1c; these devices require a short high current pulse to quickly turn-on the device and a small dc-current for maintaining the low-ohmic channel. The typical 2 V required for keeping the normally-off JFET in on state were generated from the 12 V with a 120 Ω gate resistor. This solution limits the JFET's gate current to ~80-100 mA, sufficient to maintain the channel in a low ohimic conduction state. The main drawback of this solution is that the on-state gate resistor has to dissipate a small amount of power (max ~0.6 W for a bridge configuration where the maximum duty cycle is 0.5). A slightly more efficient gate driver would use a dc-dc converter (buck) to generate the 2-3 V from the 12 V, this solution would be slightly more energy efficient despite an increase of the gate driver complexity and cost. A simple regulator based on a zener diode was used to obtain the intermediate voltage level (-7 V) required for the digital isolator, Fig. 1c. With a small adaptation the pulsed gate driver can also be used for SiC on-JFETs to reduce its turn-on switching losses. However, it was desired to highlight that an on-JFET could be considered a drawback in a bridge configuration (normally-on) and a simple gate driver could represent a good compromise for the device selection.

IV. Test Setup and Data Processing

The test setup is based on an inductive clamped circuit (Fig. 2a and 2b). The performed test is a typical double pulse test [9]

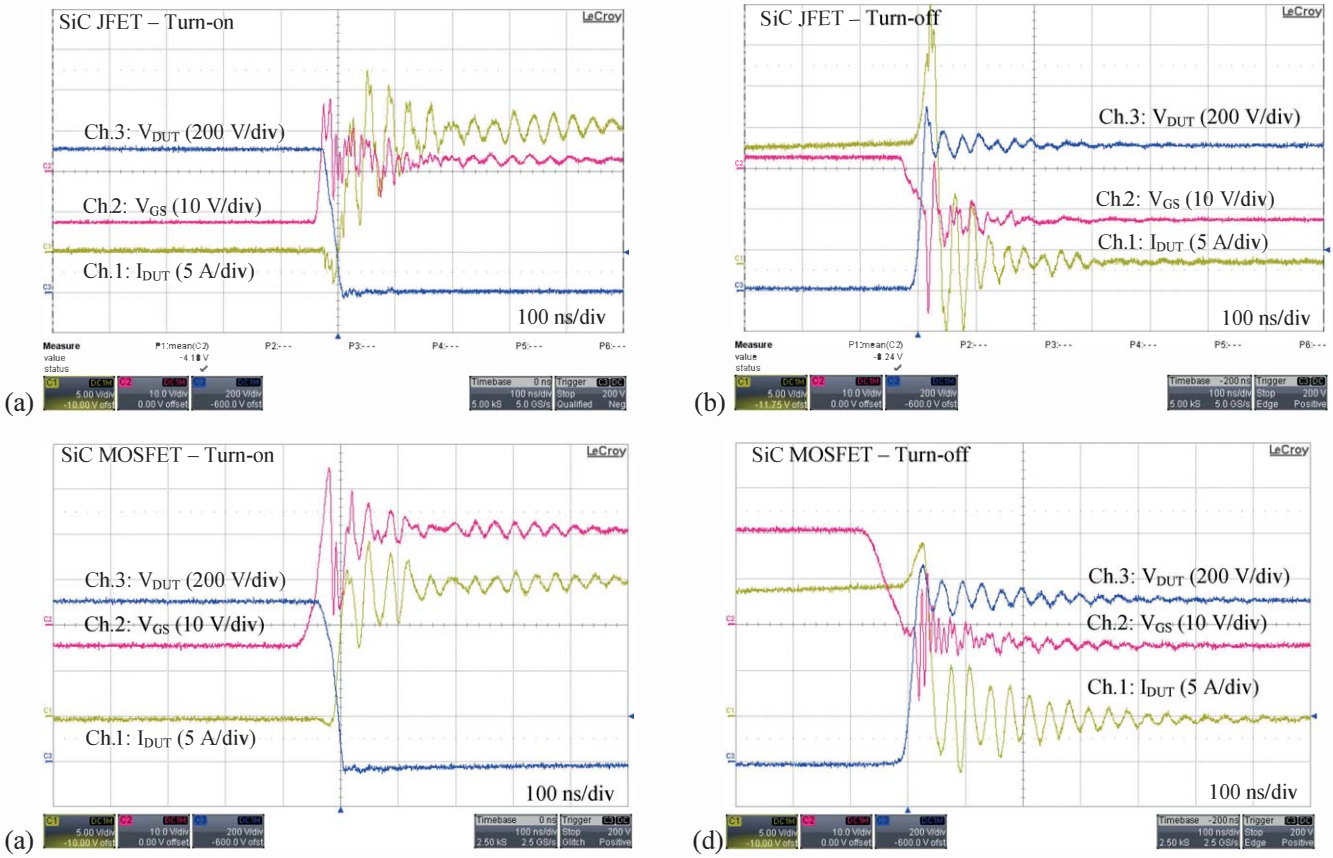


Fig. 3. Measured switching waveforms at 700 V 15 A Rg=2.5 Ohm *100ns/div*. SiC JFET turn-on (a) and turn-off (b) transients. SiC MOSFET turn-on (a) and turn-off (b) transients. Ch.1: DUT source current *5A/div*, Ch.2: gate-source voltage *10V/div* and Ch.3: drain-source voltage *200V/div*.

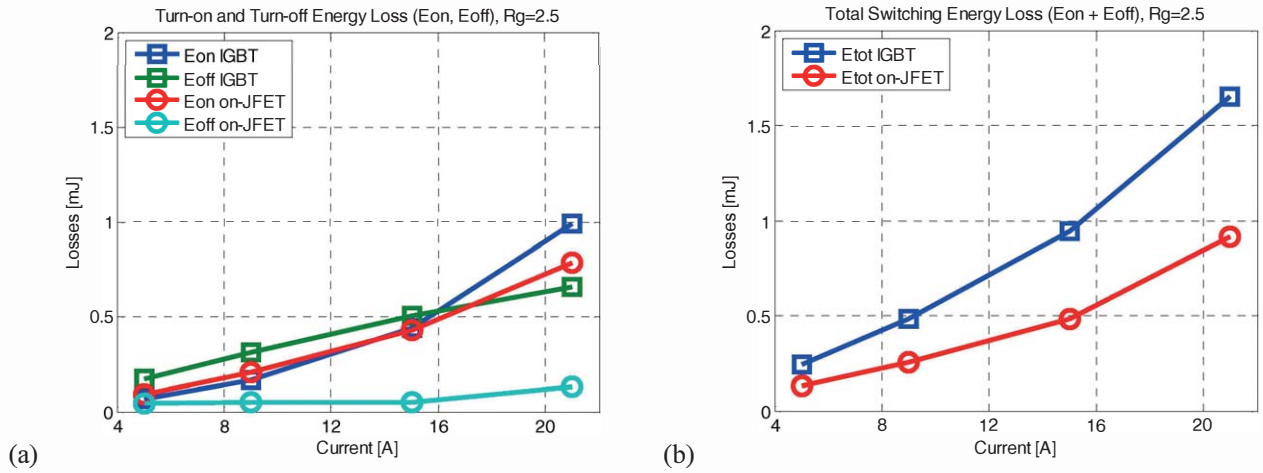


Fig. 4. Turn-on and turn-off switching losses for IGBT and SiC on-JFET with simple gate driver (a) and total switching losses (b). Current range 5-21 A, dc-link voltage 700 V, scale 0-2 mJ.

widely used for characterizing the switching performance of power semiconductors. This test applies two short current pulses to measure the turn-on and turn-off behavior of the DUTs; the pulse duration is small (1-10 µs) and the overall energy dissipated during the pulses is not sufficient to increase the device temperature.

The test setup was designed in order to have a low stray inductance loop from the dc-link capacitor to the DUT, (Fig. 2a). Gate drivers were placed in proximity of the DUT with short and twisted connections for reducing the gate-loop inductance. For all measurements the DC-link voltage is kept constant at 700 V and each device is tested at different current levels in the 3-21 A range. The test circuit remains unchanged for all measurements and only the DUTs and the gate drivers are replaced from test to test. For each measurement turn-on transients (Fig. 3a SiC off-JFET and Fig. 3c SiC MOSFET) and turn-off transients (Fig. 3b SiC off-JFET and Fig. 3d SiC MOSFET) of each device were recorded.

The measurements are performed in similar environmental test conditions at room temperature (20-25°C); all original data from the measurements are stored in Matlab format and post processed. The post-processing includes delay compensation of the current probe and loss calculation as shown in Fig. 2c (integral of the instantaneous power loss around the maximum instantaneous power loss with a threshold level of 3%). After post-processing, data are plot separately as turn-on and turn-off losses and, in a second step, together for an overall view.

Measurements were performed with a LeCroy oscilloscope (5GS/s) using 500 MHz 10x voltage probes for measuring the gate and DUT voltage. An ultra mini Rogowsky coil was used for measuring the emitter /source current. The probe was placed directly on the DUT excluding the gate return current. This type of probe has a bandwidth limited to 20 MHz which is just sufficient for measuring the transients observed in this setup (excluding the high frequency oscillations).

V. Measurements Results and Analysis

The first set of measurements compares the switching performance of the latest IGBTs with normally-on SiC JFETs (Fig. 4). In this case, the investigations are focused on the possible performance improvement that can be achieved with SiC devices without changes to the gate driver. In fact, the gate driver used for IGBTs is the same used for on-JFET but in this case the JFET's gate is tied to the ground of the gate driver allowing the gate to source voltage of the JFET to reach -15 V turning off the on-JFET. From Fig. 4a it can be observed that the turn-on losses for both IGBT and on-JFET are similar, slightly lower for the on-JFET at high current levels. On the other hand, the turn-off losses of the IGBT are quite above the turn-off losses of the on-JFET; in fact even the latest trench IGBTs have a significant component of the losses that is given by the IGBT tail current phenomenon. On an overall picture, the total losses of the IGBT and the on-JFET (Fig. 4b) show that with the same gate driver complexity and no additional changes (in the case of an isolated gate driver) the on-JFETs can provide a reduction of the switching losses of about 40% compared to IGBTs. This come with a minimum cost increment since SiC on-JFETs are more expensive; however, there is a main drawback with is that the devices are normally-on and therefore, in some converter topologies this is not desired since a failure of one gate driver would be destructive for the system.

In a similar way the switching performance of the SiC off-JFET driven with a fast pulsed gate driver (optimal for this device) is compared with the performance of a SiC MOSFET (no special driver requirements for these devices expect for the voltage swing levels: from -4 V up to 20 V). The turn-on losses of the SiC MOSFET show a very linear behavior in the measured current range; for all current values the turn-on losses are higher than the SiC off-JFET ones. In this case, the JFET turn-on losses show a light exponential behavior. For both devices the turn-off losses are very similar with minimal differences (Fig. 5a); the difference is so small that for some points the two curves are almost overlapping. The overall device losses (Fig. 5b) highlight that properly driven SiC off-

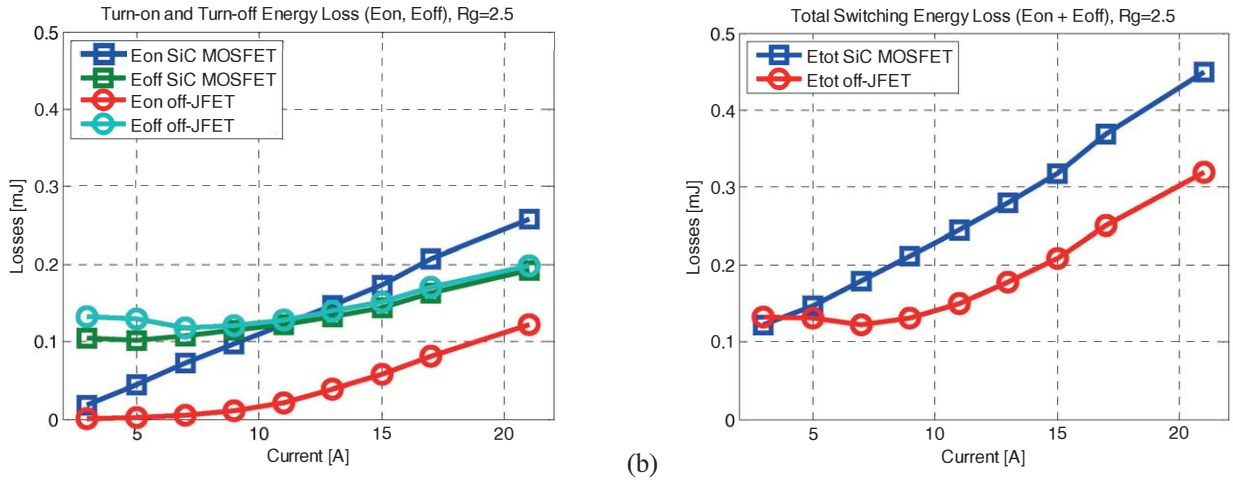


Fig. 5. Turn-on and turn-off switching losses for SiC off-JFET and SiC MOSFET (a) and total switching losses (b). Current range 3-21 A, dc-link voltage 700 V, scale 0-0.5 mJ.

JFET can provide better performance than the SiC MOSFET with a switching loss reduction of up to 33% depending on the current level.

As final, a comparison of the total switching losses of all analyzed devices is presented in Fig. 6. The graph highlights that at low current levels the switching performances of IGBTs are not far from the switching performance of the SiC devices. Despite the simple gate driver, normally-on JFETs can provide a significant switching loss reduction over IGBTs. The switching performance of on-JFETs can be significantly improved with a more suitable gate driver. It was also observed that SiC off-JFETs proved to provide extremely low losses and fast switching transients. Newly SiC MOSFETs provide very low switching losses (slightly higher than the off-JFETs) with a minimal driver complexity. In a general purpose application the introduction of SiC devices with optimized drivers as replacement of Si IGBTs can provide a reduction of the switching losses up to 70-80% depending on the considered converter and on the voltage and current levels.

VI. Reference Converter and Switching Performance in Correlation to the Gate Driver

A. *Reference Converter*

A dc-dc converter (isolated full bridge boost converter, Fig. 7a) is used as reference for analyzing the gate driver performance. The converter has a power rating of 6 kW and its high voltage side is rated at 700-800 V. The converter reference design is based on Si IGBTs for the high voltage side and Si MOSFETs on the low voltage side switching at 50 kHz.

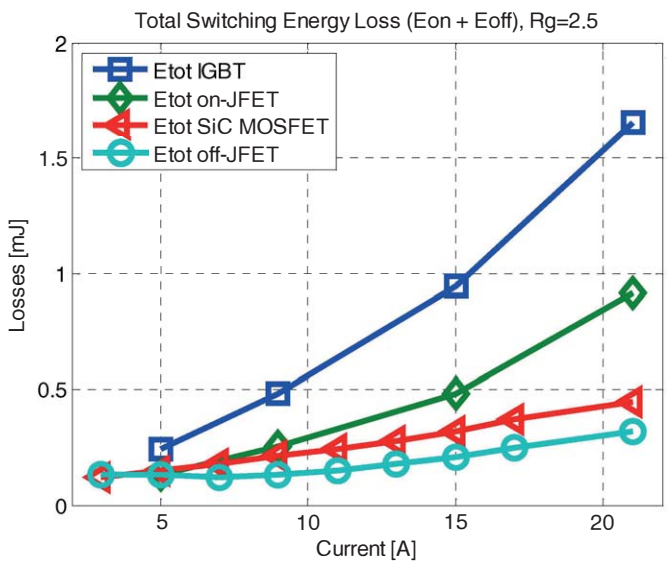


Fig. 6. Comparison of the total switching losses for all considered devices (Si IGBT, SiC on-JFET with simple gate driver, SiC off-JFET with pulsed gate driver and SiC MOSFET). Current range 3-21 A, dc-link voltage 700 V, scale 0-2 mJ.

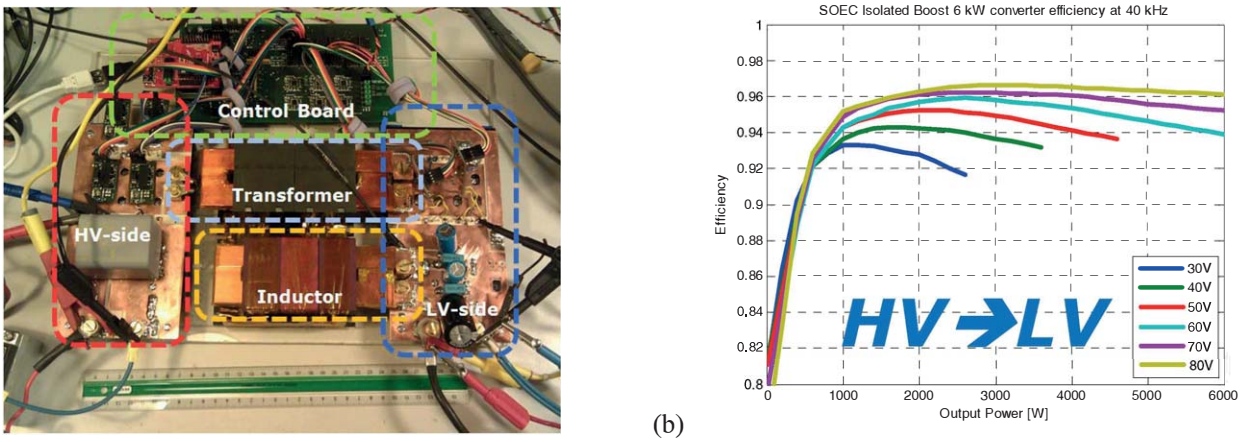


Fig. 7. Dc-dc isolated full bridge boost converter (IFBBC) used as reference for the calculations highlighting its main components (a). Measured efficiency with power flow from the high voltage to the low voltage side at different voltage levels (b).

Peak efficiency is ~96% with power flow from the high voltage to the low voltage side, Fig. 7b. In this case, the power devices used on in the high voltage side strongly limits the converter efficiency. In fact, when the power flow is reversed, the current flows through the IGBTs antiparallel SiC diodes resulting in a peak efficiency of ~97.7%. Introducing SiC JFETs or SiC MOSFETs would be beneficial for the converter in order to increase the efficiency and to have active rectification for both power flow directions.

B. Switching Performance in Correlation to the Gate Driver Cost and Complexity

The performances of the devices are evaluated in relation to the cost of the gate driver and its complexity. One factor that can be used to take into account the gate driver complexity is the number of components present on the gate driver board. A larger number of components on the gate driver is also an indicator of the number of features implemented on the board. An example is represented by gate drivers for large IGBT modules where the gate drivers also perform device protection and monitoring functions. In the multi-kW power range power device and gate driver cost plays an important role in terms of performance-cost. The analysis and trade-off considerations take into account the power semiconductor losses, the gate driver complexity and cost, and, the overall cost (gate driver and power semiconductor). For having an evaluation of the cost, devices are considered in large quantities as April 2013 from a commercial website. For convenience of interpretation, values are analyzed on a normalized scale based on the maximum observed value. As comparison a second reference for the prices of power semiconductors is referred to mid-2012.

As expected Si IGBTs are the devices with the largest losses and with the lowest gate driver complexity and overall cost, Fig. 8. Using normally-on JFET with a simple gate driver represents good trade-off between the gate driver complexity and the performance increase in terms of loss reduction. This limits the gate driver cost and also provides an increase of the converter efficiency. However, in this case the device cost significantly increases the overall cost resulting in a cost increase by a factor ~4 compared to the IGBT case. Moreover,

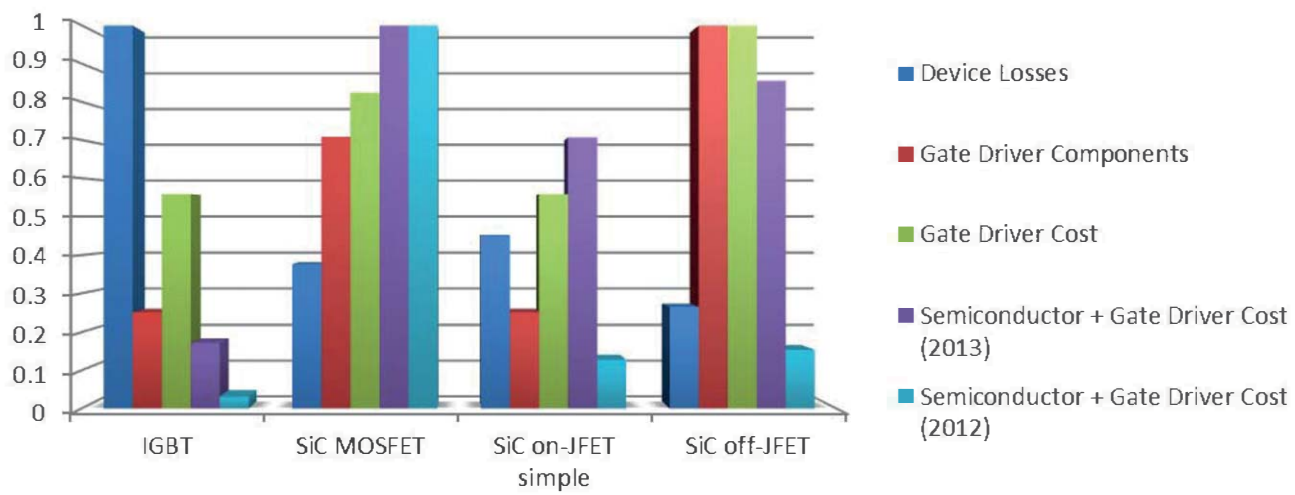


Fig. 8. Comparison of different device and gate driver performance taking into account the gate driver complexity and cost. Values are normalized from 0 (min) to 1 (max). Respectively from left to right: device losses (blue), number of discrete components on the gate driver (red) and total gate driver cost (green). Maximum values: 127 W for device power loss, 24 for number of gate driver components and 10.6 € for the gate driver cost. Overall cost 48.7€ for year 2013 and 271€ for year 2012.

on-JFETs are often not desirable in power converters due to the normally-on behavior.

SiC off-JFETs were observed to be the most performing devices, however, to properly drive these devices a tailored gate driver with a large number of components is required, Fig. 8. This results that the off-JFETs gate driver is also the most expensive driver.

The recently introduced SiC MOSFETs can reduce the gate driver cost despite a higher price for the power semiconductor. It is observed that the switching losses of SiC MOSFETs are slightly higher than the SiC off-JFETs however, well below the Si IGBT ones. The measured SiC MOSFETs were of the first generation; as 2013 the second generation of these devices is available. The evolution from one generation to the other one introduced a significant cost reduction for the power semiconductors. This is observed in Fig. 8 where the overall price of the gate driver and the power semiconductor for the first (2012) and second (2013) generation is compared. In both cases, the SiC MOSFET with its gate driver is the most expensive combination (values normalized to the maximum) however, the second generation of devices significantly reduced the power semiconductor cost getting SiC MOSFETs closer to SiC JFETs and to Si IGBTs.

CONCLUSIONS

The paper presented a brief comparison of the switching performance of the most relevant 1200 V power devices (Si IGBTs, SiC on-JFETs, SiC off-JFETs and SiC MOSFETs) based on experimental results. The results highlighted that SiC JFETs are the most performing devices with the lowest losses. However, the main drawback of these devices is that they require a more complex gate driver (pulsed gate driver) for achieving such low losses and a small DC-current for keeping the device in conduction state (off-JFETs). It was observed that using a simple gate driver for a normally-on JFET significantly limits the JFETs performance, but this could represent a good trade-off and significant performance increase over the Si IGBTs. SiC MOSFETs can provide very low losses and still maintain a low gate driver complexity, these devices represents a good trade-off among the tested devices despite a larger unitary cost for the power semiconductor itself. As expected, trench IGBTs of the latest generation have the worst performance among the tested devices; however, especially at low current levels, they could represent preferable choice for having the lowest gate driver complexity and high reliability due to a well proven technology.

On overall it was observed that for designs based on SiC devices the gate driver cost has a minimal influence on the overall cost and the majority of the cost is given by the power semiconductor itself. Since, the gate driver for SiC MOSFETs is more like an IGBT driver and thanks to the significant price reduction of SiC MOSFET occurred during 2013 made SiC MOSFETs more attractive and competitive power semiconductors for new designs.

REFERENCES

[1] Elasser, A.; Chow, T.P.; , "Silicon carbide benefits and advantages for power electronics circuits and systems", Proceedings of the IEEE , vol.90, no.6, pp. 969- 986, Jun 2002.

[2] Ostling, M.; Ghandi, R.; Zetterling, C.; , "SiC power devices — Present status, applications and future perspective", IEEE 23rd International Symposium on Power Semiconductor Devices and ICs (ISPSD 2011), pp.10-15, 23-26 May 2011.

[3] Khan, M.A.; Simin, G.; Pytel, S.G.; Monti, A.; Santi, E.; Hudgins, J.L.; "New Developments in Gallium Nitride and the Impact on Power Electronics", IEEE 36th Power Electronics Specialists Conference (PESC '05), pp.15-26, 16-16 June 2005.

[4] Franke, W.-T.; Fuchs, F.W.; , "Comparison of switching and conducting performance of SiC-JFET and SiC-BJT with a state of the art IGBT", 13th European Conference on Power Electronics and Applications (EPE '09), pp.1-10, 8-10 Sept. 2009.

[5] http://www.cree.com/

[6] Fan Xu; Ben Guo; Tolbert, L.M.; Wang, F.; Blalock, B.J.; , "Evaluation of SiC MOSFETs for a high efficiency three-phase buck rectifier," Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2012), pp.1762-1769, 5-9 Feb. 2012.

[7] Ho, C.N.M.; Breuninger, H.; Pettersson, S.; Escobar, G.; Serpa, L.; Coccia, A.; , "Practical implementation of an interleaved boost converter using SiC diodes for PV applications," IEEE 8th International Conference on Power Electronics and ECCE Asia (ICPE & ECCE Asia 2011), pp.372-379, May 30 2011-June 3 2011.

[8] Rylko, M.; Egan, M.G.; Hayes, J.G.; Power, D.; , "A soft-switched bi-directional DC-DC converter," European Conference on Power Electronics and Applications, 2007, pp.1-10, 2-5 Sept. 2007.

[9] Knop, A.; Franke, W.-T.; Fuchs, F.W.; "Switching and conducting performance of SiC-JFET and ESBT against MOSFET and IGBT," Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th, pp.69-75, 1-3 Sept. 2008.

[10] Safari, S.; Castellazzi, A.; Wheeler, P.; , "Evaluation of SiC power devices for a high power density matrix converter," Energy Conversion Congress and Exposition (ECCE), 2012 IEEE, pp.3934-3941, 15-20 Sept. 2012.

[11] Pittini, R., Zhang, Z., Andersen, A. E. M., "SiC JFET Cascode Loss Dependency on the MOSFET Output Capacitance and Performance Comparison with Trench IGBTs", Applied Power Electronics Conference and Exposition (APEC 2013), 17-21 March 2013, Long Beach, California, USA.

[12] Zhang, Zhe ; Pittini, Riccardo ; Andersen, Michael A. E. ; Thomsen, Ole Cornelius; "A review and design of power electronics converters for fuel cell hybrid system applications" conference Technoport 2012 – Sharing Possibilities: Renewable Energy Research Conference, Energy Procedia (ISSN: 1876-6102) vol: 20, pages: 301-310, 2012.

[13] Tadros, Y.; Salama, S.; Hof, R.; "Three level IGBT inverter," 23rd Annual IEEE Power Electronics Specialists Conference, 1992. PESC '92 Record., pp.46-52 vol.1, 29 Jun-3 Jul 1992.

Appendix H

Analysis of Planar E+I and ER+I Transformers for Low-Voltage High-Current DC/DC Converters with Focus on Winding Losses and Leakage Inductance

IEEE 7th International Power Electronics and Motion Control Conference ECCE Asia (IPEMC 2012)

2012 IEEE 7th International Power Electronics and Motion Control Conference - ECCE Asia
June 2-5, 2012, Harbin, China

Analysis of Planar E+I and ER+I Transformers for Low-Voltage High-Current DC/DC Converters with Focus on Winding Losses and Leakage Inductance

Riccardo Pittini, Zhe Zhang, Ziwei Ouyang, Michael A. E. Andersen, Ole C. Thomsen

Department of Electrical Engineering, Technical University of Denmark, Kgs. Lyngby, Denmark
Email: ripit@elektro.dtu.dk

***Abstract*— In this paper an analysis of two planar transformers designed for high-current switching applications is presented. Typical converter application is represented by fuel and electrolyser cell converters. The transformer designs are based on E+I and ER+I planar cores while the analysis focuses on winding resistance and leakage inductances which represent the main concerns related to low-voltage high-current applications. The PCB winding design has a one to one turn ratio with no interleaving between primary and secondary windings. The main goal was to determine if ER planar core could provide a significant advantage in terms of winding losses compared to planar E cores. Results from finite element analysis highlight that low frequency winding resistance is lower for the ER core since it is dominated by the lower mean turn length however, as the AC-resistance becomes dominating the winding eddy current losses increases more in the ER core than in the E core design. Calculated and simulated leakage inductances for the analyzed cores do not show relevant differences. A laboratory prototype based on E64 planar core is used as reference. Laboratory measurements highlight that FEM analysis provides more realistic results when computing the winding AC-resistance.**

***Keywords*— Planar Magnetics, Transformer Parasitics, DC/DC Switching Converters, High-Current.**

I. Introduction

As renewable energies are getting more important, power electronics converter are becoming more diffused and are demanded to operate in more critical applications. Non isolated Switch Mode Power Supplies (SMPS) are a limited in their applications and transformer based SMPS can provide several advantages in terms of safety (input to output isolation), reducing the component stresses (e.g. minimizing voltage and current peaks) and flexibility since they can provide easily multiple outputs and voltage regulation (turn ratio selection). Their main disadvantage is to introduce additional cost, losses and increase the volume and converter weight. The main drawbacks of transformer based SMPS are highly compensated by their advantages, therefore the market of wounded components is growing in parallel to the power supplies market [1].

Many efforts have been performed for reducing the cost and the size of magnetic components in power supplies [2] and planar structure provides an excellent solution for magnetic components into SMPS. In fact, in planar transformers windings have a flat structure commonly made with Printed Circuit Board (PCB) layers or copper foils [3]; PCB windings are easily integrated in mass production reducing costs and giving a low-profile high-power density structure. The natural flatness of the winding cross section is more suitable for operation at high frequencies since it is less sensible to skin effect compared to traditional wires, moreover, the leakage inductance can be significantly reduced by heavy interleaving [4][5][6][7] compared to traditional wounded components. The main disadvantages of planar transformers comes from their high capacitive coupling between the windings [8], difficulties for designing high voltage due to limited clearance and creepage distances, and challenging high current designs since it is difficult to laminate thick copper tracks on PCB. In some applications it is desirable to operate at low-voltage and high-current (e.g. fuel cells [9][10]) and as the converter power ratings increase the design of high-current planar transformers based PCB windings becomes more and more challenging. Most of the previous research on high-current low-voltage transformers focuses on conventional high-power and wounded transformers moreover, a limited number of publications were found on high-current planar transformers [11][12] highlighting that the topic requires further investigations and analysis for determining which are the most suitable cores for these applications.

The selected application is a transformer for a full bridge isolated boost converter which represents one of the most suitable topologies for high-current and low-voltage applications with wide input voltage window. This paper will present an analysis of two planar cores, E64/10/50 and ER64/13/51, aiming to highlight which is the most suitable core in terms of winding losses and leakage inductance for high current planar transformers. Since the most suitable core is application and topology dependant, the paper will not state which is the best core, however, will give a clear picture of the differences in terms of stray parameters when the two selected cores are used for designing high current planar magnetic. Analytical and finite element analysis results are compared with a laboratory prototype.

978-1-4577-2087-1/11/$26.00@2012 IEEE

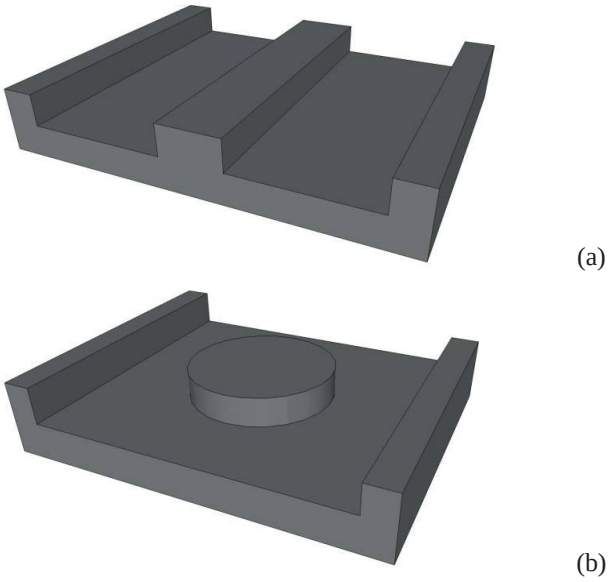


Fig. 1. Planar transformer cores used in the analysis, E64/10/50 (a) and ER64/13/51 (b).

II. Selected Planar Cores

As general rule, rounded core cross section transformers are preferred in many applications due to their lower mean turn length and leakage inductance. However, round core cross section transformers might not be the best for all applications and selecting the best core for the candidate application might not be straight forward but, it would require more design and optimisation cycles for different core shapes.

In planar transformers for high current applications the smaller winding area width can represent significant issue in terms of increased winding resistance, in fact a winding resistance of few *mOhm* at high current (e.g. 50-100 A) can easily produce power losses in the range of tenths of Watt and more. For this reason to verify the possible advantages and disadvantages of rounded core planar transformers requires an accurate analysis of different transformer designs.

The two selected cores for the analysis are E64/10/50 and ER64/13/51 from Ferroxcube in 3F3 material, Fig. 1. The cores have been selected since they have similar effective area and minimum area; their base footprint is the same (64*50.8 mm) however, their main difference is in their height that differs by ~3 mm giving a substantial difference in the core volume. For this reason for obtaining a better trustworthy analysis the ER64/13/51 core height has been clipped to 10.2 mm obtaining an ER64/10/51. The cores main characteristics as specified from the manufacturer are summarized in Table I.

TABLE I. Selected Core Characteristics

Core Type	E64/10/50	ER64/13/51	ER64/10/51[b]
Material	3F3	3F3	3F3
Effective area [mm^2]	519	566	566
Effective volume [mm^3]	40700	52600 [a]	~43700
Effective length [mm]	79.9	93	~80
Core min area [mm^2]	519	507	507
Core mass [g]	~100	~152	~125
Gapped	No	No	No

a. Volume difference is due to the different core height.
b. Clipped ER64 core.

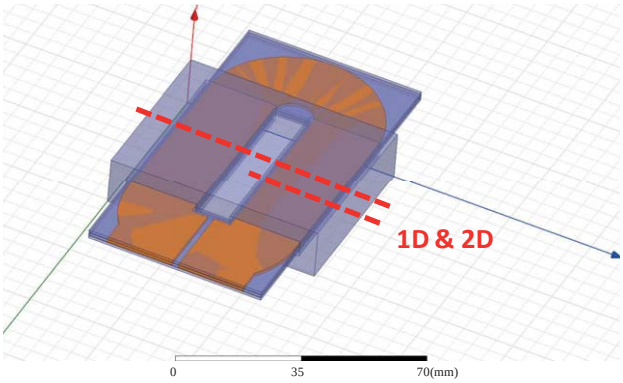


Fig. 2. Planar transformer E64/10/50 core, 3D model with high current winding: highlight axes used in 1D & 2D analysis.

III. Methodology

It is essential that the method used to analyze the two transformers is coherent, therefore, for performing a more trustworthy analysis purely based on the transformer core geometry and not on the winding topology, a simple Primary-Secondary (P-S) winding topology has been considered. More complicated winding arrangements can be designed however, this is not in the scope. The high current primary windings on Fig. 2 and Fig. 3 were designed for using the maximum available winding area width in order to reduce as much as possible the winding resistance since it is the most critical factor regarding integration of high current tracks on PCB. In the ER core the winding width was selected as in the E core case however, due to geometrical limitations of the ER core the winding width was reduced in proximity of the core centre, as visible in Fig. 6. The same creepage and clearance constrains were used for designing the transformer windings.

A. Analytical Approach

Analytical approach is often performed considering core

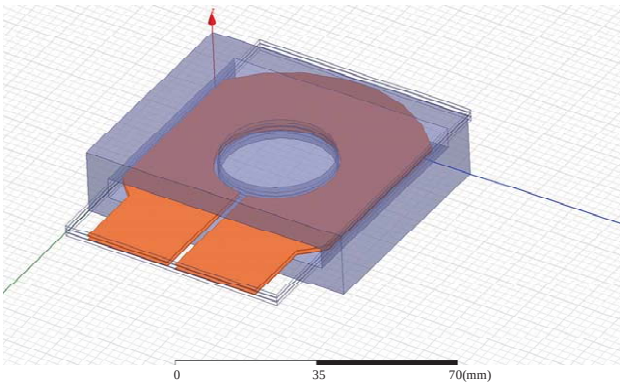


Fig. 3. Planar transformer ER64 core, 3D model with visible high-current winding geometry.

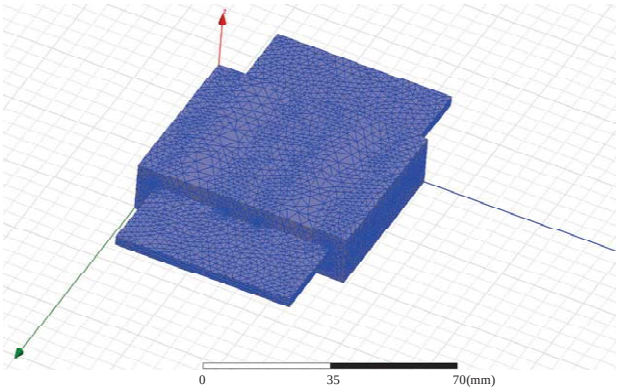


Fig. 4. Example of a planar transformer based on E64/10/50, 1:1 turns ratio, modeled with 3D FEM

symmetries to simplify the analytical expressions, 1-D or 2-D as in Fig. 2; this allows to easily calculate the main stray parameters in planar transformers.

In planar transformers the windings consist of parallel and flat conductors creating a parallel plane capacitor structure. In this type of transformers the intra-winding capacitance can often be neglected due to the dominating primary-secondary winding capacitance. This capacitance can be the main issue for common mode noise and it can be simply estimated as (1) [4].

$$C_i = \varepsilon_0 \varepsilon_r \frac{(l + 4b \cdot i)}{h_\Delta} \qquad (i = 1,2,3 \ldots, n) \qquad (1)$$

Where ε_0 is the permittivity in free space, ε_r is the relative permittivity of the insulating material, l is the length of the center leg cross-section, b is the conductor width, h_Δ is the distance between the conductive plates and n is the number of overlapping turns.

The most used analytical approach for estimating the winding leakage inductance considers the energy stored in the transformer windings. From the transformer winding generic expression of the leakage inductance can be extracted as in (2) [4].

$$L_{ik} = \mu_0 \frac{l_w}{b_w} \frac{N^2}{M^2} \left(\frac{\sum x}{3} + \sum x_\Delta \right) \qquad (2)$$

Where μ_0 is the permeability, l_w is the length of one turn, b_w is the width of each turn, N is the number of turns on the winding which the leakage inductance is to be referred, M is the number section interfaces, $\sum x$ is the sum of all section layer heights (windings) and $\sum x_\Delta$ is the sum of all inter-section layer heights (insulator). This approach computes the leakage inductance considering the magneto motive force (MMF) linear between non-interleaved sections. Therefore, the approach provides identical leakage inductance values for different winding arrangement (e.g. P-P-S-S-S-S-P-P provides the same leakage inductance as P-P-S-S-P-P-S-S considering the same insulation thickness). Inaccuracies due to this approach can be reduced by using a piecewise linear approach described and proven in [3]. However, in this paper the most diffused methodology is used for comparison with FEM methodology.

For a simple two winding topology as in the selected case scenario (P-S) with only one interface layer between primary and secondary the leakage inductance can be estimated with (3) [4].

$$L_{ik} = \mu_0 \frac{l_w}{b_w} N^2 \left(\frac{h_1 + h_2}{3} + h_\Delta \right) \qquad (3)$$

Where h_1 and h_2 are the heights of the primary and secondary windings respectively, h_Δ is the height of the insulation layer between the primary-secondary traces. Winding losses represent the main concern regarding high current integrated magnetics; in a transformer the skin effect and the proximity effect strongly influences the Joule losses especially at high switching frequencies. Planar transformers have the advantage of having flat conductors which sensibly reduces the sensitivity to skin effect. Proximity effect is caused by current flowing in adjacent conductors, also this effect contributes to increase the conductor AC-resistance moreover, and the proximity effect can dominate over the skin effect. The ratio between the AC-resistance and the DC-resistance that takes into account the skin and proximity effects can be expressed as in (4) [4].

$$\frac{R_{ac}}{R_{dc}} = \frac{\xi}{2} \left[\frac{\sinh(\xi) + \sin(\xi)}{\cosh(\xi) - \cos(\xi)} + (2\mathrm{m} - 1)^2 \frac{\sinh(\xi) - \sin(\xi)}{\cosh(\xi) + \cos(\xi)} \right] \qquad (4)$$

Where $\xi = \mathrm{h}/\delta$, h is the conductor height, δ is the skin depth in the conductor and m is >1 for non interleaved multilayer windings.

B. FEM Analysis (FEA)

Finite Element Method (FEM) can be used for calculating transformer characteristics and stray parameters. FEM can be performed based on two different approaches:

- 2-D approach
- 3-D approach

2-D simulations perform an analysis on the transformer based on its symmetry axes. The simulation can be performed on the entire transformer cross section or only on half of it considering its symmetry, as shown on Fig. 2. This approach requires limited computation time however it can only partially consider the flux linkage in free air (without end effects) since it cannot take into account that the core geometry is limited.

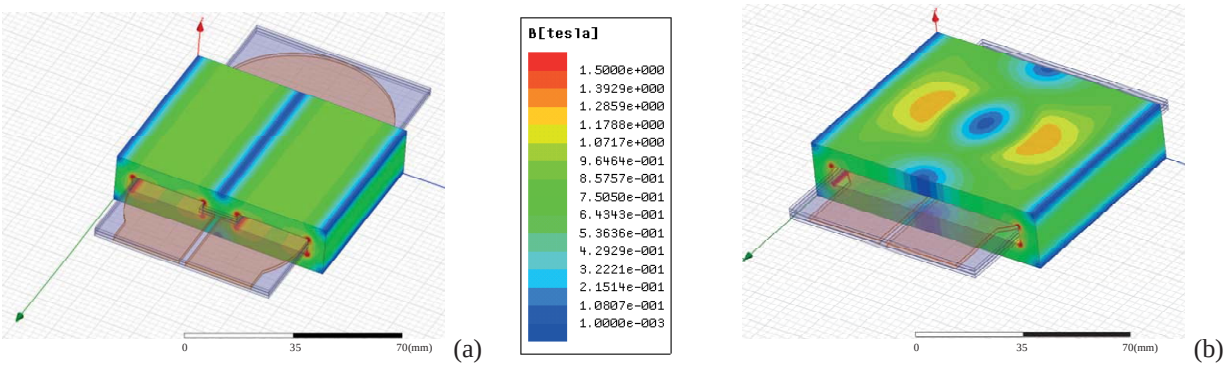


Fig. 5. Magnetic flux in the E+I core transformer (a) and in the ER+I core transformer (b).

3-D approach performs a FEM analysis over the entire transformer model as on Fig. 4. This type of analysis is the most accurate since it computes the transformer parameters considering also part of the windings that is exposed to free air. However, this type of computation requires very long computation times since the entire geometry has to be modelled with a fine mesh. Moreover, when a model is composed by large and small geometries the mesh used for the analysis should be selected properly to achieve the desired analysis accuracy.

IV. Methodology Applied to the Analysed Case

This analysis was performed based on three approaches: analytical, 3D FEM and experimental. Since performing an accurate analytical analysis of a complex geometry requires geometrical simplifications especially when modelling rounded geometries, a simple case analysis is selected. The transformer is specified to have a 1 to 1 turn ratio and a simple P-S structure with no interleaving, Table II. The analysis focused on determining the AC-resistance and the leakage inductance for the two proposed geometries and comparing the obtained values with analytical calculations and laboratory measurements on a prototype.

An adequate analytical analysis of the rounded cross section planar core has to consider minimal geometrical approximations in order to reduce computational errors. It is possible to analyse transformer resistance and leakage inductance with a piece-wise approach which require dividing the winding into several sectors and execute the calculations for each sector. The selected approach considers and equivalent rectangular winding where the winding length is defined by the core mean turn length (MTL) and the winding width by the ratio between the effective surface of the winding and the MTL of the core. The effective winding surface can be easily computed by considering surface of an annulus with width equal to the winding width used in the E64 design and removing to that value the two sector regions highlighted on Fig. 6. The geometrical approach simplifies the computation since avoids performing an analytical analysis for many winding sections.

In the 3D FEM approach the two transformers were designed and simulated with Ansoft Maxwell v15, as shown on Fig. 5 where the magnetic flux for the two analysed cases is plotted on the core surface. Since the complete 3D model for E64 and ER64 core based transformed does not represent a very complex structure to analyse the simulation was defined with a minimum convergence of 0.1% without requiring too long computation time (also limited by the few analysed frequencies). The FEM simulations allow extracting directly the transformer parameters; both the AC-resistance and the leakage inductance were extracted for different frequency values: 50 Hz as low frequency reference and 50-150 kHz as

TABLE II. Transformer Specifications

Core Type	E+I 64/10/50	ER+I 64/10/51[a]
Material	3F3	3F3
Material relative permeability (μ_r)	1760	1760
Transformer turn ratio	1:1	1:1
Winding structure	P-S	P-S
Primary copper thickness [mm]	0.2	0.2
Secondary copper thickness [mm]	0.2	0.2
Primary copper width [mm]	20	20~11[b]
Secondary copper width [mm]	20	20~11[b]
Dielectric material	FR4	FR4
Dielectric thickness [mm]	0.8	0.8
Temperature [°C]	25	25

a. Core volume reduced for having same height/volume as E64.
b. Winding width limited by winding area width.

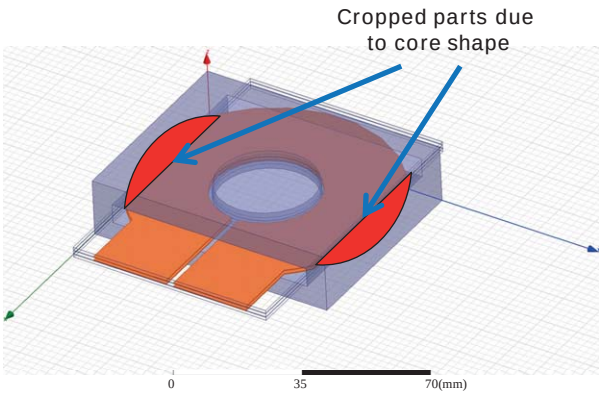


Fig. 6. ER 3D model highlighting (red) cropped winding sectors.

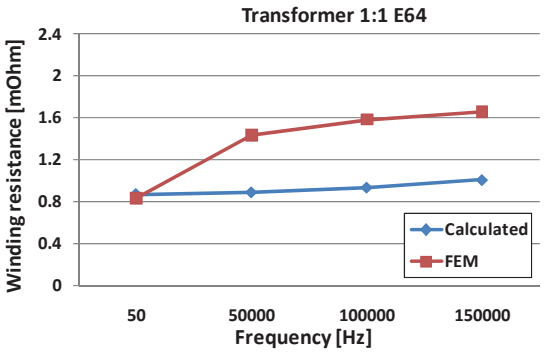


Fig. 7. Comparison of calculated winding resistance and FEM analysis for E64 core, 1:1 turns ratio.

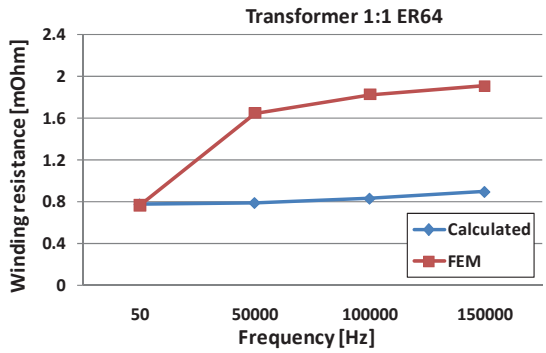


Fig. 8. Comparison of calculated winding resistance and FEM analysis for ER64 core, 1:1 turns ratio.

the expected operating frequency range of the power converter. The AC-resistance is extracted from the winding losses, its value at 50 Hz represents a DC-resistance reference and at 50-150 kHz represents the actual winding resistance (AC). With a similar procedure it is possible to extract the transformer leakage inductance form the sum of the energies stored in the transformer leakage layers. However, since the FEM simulations can provide the transformer coupling matrix (L_{11}, L_{12}, L_{21} and L_{22}), extracting the leakage inductance from these values is a direct procedure.

The experimental approach has been used for establishing concrete references to validate the analytical computations and the analysis performed in 3D FEM. During the initial phase, the aim was to develop two prototypes that would have been used as reference however, due to the lack of availability of ER64 cores, only a prototype based on E64 core was developed highlighting that the availability of specific core shapes and materials might represent an important issue related to transformer design. The prototype based on E64 core is used to verify that the analytical and FEM approach produce coherent values.

V. Analysis of the Results

The analysis of the results is divided into two parts: in the first part results from the analytical approach and the FEM analysis are compared, while in the second part the results obtained with the laboratory reference prototype are analysed.

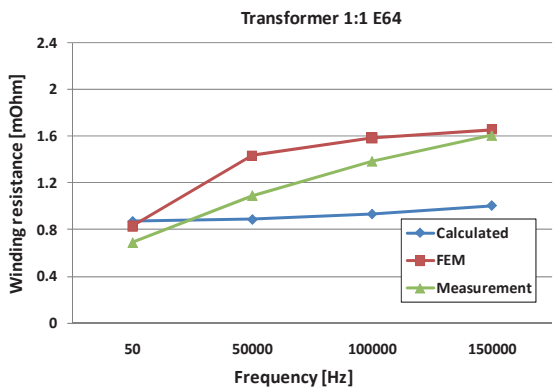
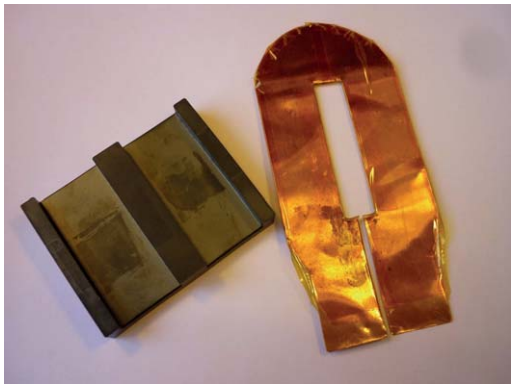


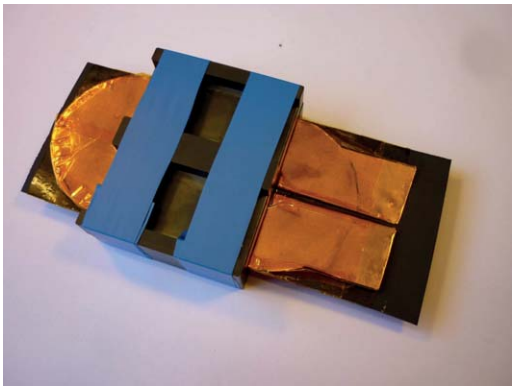
Fig. 9. Comparison of calculated winding resistance, FEM analysis and measurement for E64 core, 1:1 turns ratio.

The analytical and FEM results are presented on Fig. 7 and Fig. 8, which allow comparing the transformer winding AC-resistance: the E core based transformer has a slightly higher low frequency primary resistance (DC-resistance) compared to the ER solution, this is due to the higher mean turn length of required for the E core windings. Nevertheless, at higher frequencies the AC-resistance significantly increases and becomes dominating for the ER core. The ER core windings width is not constant, in fact winding width is limited by the narrow winding area width in proximity of the core centre while, away from the core centre the width is defined as in the E core case. For the analysed case the proximity effects in the narrow winding area width of the ER core dominate compared to E core. The calculated resistance at low frequencies matches (DC-resistance) good the FEM analysis however, at high frequencies the mismatch significantly increases highlighting that geometrical approximations and assumptions used in the calculation introduce large inaccuracies (e.g. Dowell's equation (4) considers infinite MLT length and uniform turn current density). The comparison with the reference prototype (Fig. 9) highlights that FEM analysis can produce results which are more realistic compared to analytical calculations based on (4). The relevant differences observed between analysis and measurement can be explained by the prototype accuracy (realised with copper foil and dielectric layers, on Fig. 10), the contact point resistance and the instrument resolution when measuring such low-resistance values.

The leakage inductances referred to the transformer primary are presented on Table III. The two analysed cases show similar leakage inductance at the expected operating frequencies with a slightly higher value for the E core compared to the ER core in the calculations. The higher mean turn length of the E core is compensated by the wider winding giving comparable leakage inductances for the two designs. The opposite effect is observed on the ER core design, where the limited winding width is balanced by a lower mean turn length. The calculated leakage inductance was evaluated based on geometrical approximation introducing significant approximations, while the FEM analysis provided a difference between the E64 and ER64 core of less than 0.1% which also



(a)



(b)

Fig. 10. Pictures of E64 core and realized winding (a) and assembled transformer (b).

is the defined FEM accuracy for convergence. The experimental results have a large deviation from the expected value, in fact the laboratory prototype based on copper foil windings has an insulation layer thickness which is slightly inhomogeneous compared to the designed case, giving a larger measured inductance. Even though, low-inductance Kelvin probes have been used, they introduce significant stray inductance (~<10 nH) due to the measuring system which justifies the observed difference.

TABLE III. LEAKAGE INDUCTANCE

	Leak_pri @100 kHz (nH)	
	E-core	***ER-core***
Calculated	11.84	10.64
FEM Analysis	9.998	9.998
Measured	~22	-

VI. CONCLUSIONS

Designing planar transformers for high current SMPS require analysis and selection of the most suitable core for the selected application. This is not a straight forward choice and it is required a detailed analysis that can be performed as described in this paper. Different analysis can produce significantly different results making the selection of the most application-suitable core even more complicated. The proposed analysis does not define which is the best core (application dependent) however, gives a clear indication for winding losses and leakage inductance on transformers based on planar E or ER cores.

For the selected designs, high current planar transformers based on E cores have shown lower winding losses compared to the ER cores. This effect is observed mainly due to proximity and skin effects which significantly increase the winding resistance in the narrow winding area width of the ER, in fact E cores are less sensible to this effect since the winding area width is significantly higher than ER cores. In the analysed cases both core designs have shown similar leakage inductance values; differences can be enhanced by increasing the number of turns. Differences observed with the laboratory prototype (leakage inductance) are mainly related to the slightly different and inhomogeneous insulation layer thickness and to stray inductance introduced by the measuring system.

REFERENCES

[1] Aime, J.; Cogitore, B.; Meunier, G.; Clavel, E.; Maréchal, Y.; , "Numerical Methods for Eddy Currents Modeling of Planar Transformers," IEEE Transactions on Magnetics, vol.47, no.5, pp.1014-1017, May 2011.

[2] Pavlovsky, M.; de Haan, S.; Ferreira, J.A.; , "Reaching High Power Density in Multikilowatt DC–DC Converters With Galvanic Isolation," IEEE Transactions on Power Electronics, vol.24, no.3, pp.603-612, March 2009.

[3] Ziwei Ouyang, “Advances in Planar and Integrated-Magnetics”, Danish Technical University, PhD Thesis, ISBN: 978-87-92465-88-7, pages: 228, 2011.

[4] Z. Ouyang; O.C.,Thomsen; M. A. E., Andersen; , "Optimal design and tradeoff analysis of planar transformer in high-power dc-dc converters," IEEE Transactions on Industrial Electronics, vol.59, no.7, July 2012.

[5] Carsten, B.W.; , "The low leakage inductance of planar transformers; fact or myth? ," Applied Power Electronics Conference and Exposition, APEC 2001. Sixteenth Annual IEEE, vol.2, pp.1184-1188 vol.2, 2001.

[6] Jianbing Li; Changchao Hu; Xuemin Pang; , "Analysis of the leakage inductance of planar transformer," 9th International Conference on Electronic Measurement & Instruments, ICEMI 2009, pp.1-273-1-276, 16-19 Aug. 2009.

[7] Cove, S.R.; Ordonez, M.; Quaicoe, J.E.; , "Modeling of planar transformer parasitics using design of experiment methodology," 23rd Canadian Conference on Electrical and Computer Engineering, (CCECE) pp.1-5, 2-5 May 2010.

[8] Shahabi, N.; Zare, F.; Ghosh, A.; Ledwich, G.; "A new configuration for planar magnetic elements to reduce capacitive couplings," 14th International Power Electronics and Motion Control Conference, EPE/PEMC 2010, pp.T6-126-T6-130, 6-8 Sept. 2010.

[9] Morten Nymand, “High Efficiency Power Converter for Low Voltage High Power Applications”, Danish Technical University, PhD Thesis, ISBN: 978-87-92465-33-7, pages: 164, 2010.

[10] Ziwei Ouyang; Sen, G.; Thomsen, O.C.; Andersen, M.A.E.; Björklund, T.; , "Fully integrated planar magnetics for primary-parallel isolated boost converter," Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition, APEC 2011, pp.174-181, 6-11 March 2011.

[11] Peng Xu; Mao Ye; Pit-Leong Wong; Lee, F.C.; , "Design of 48 V Voltage regulator modules with a novel integrated magnetics," IEEE Transactions on Power Electronics, vol.17, no.6, pp. 990-998, Nov 2002.

[12] Yi Wang; de Haan, S.W.H.; Ferreira, J.A.; , "Design of low-profile nanocrystalline transformer in high-current phase-shifted DC-DC converter," IEEE Energy Conversion Congress and Exposition, ECCE 2010, pp.2177-2181.

Appendix I

High Current Planar Transformer for Very High Efficiency Isolated Boost DC-DC Converters

2014 International Power Electronics Conference (IPEC 2014) - ECCE Asia

High Current Planar Transformer for Very High Efficiency Isolated Boost DC-DC Converters

Riccardo Pittini
Technical University of Denmark
Dept. of Electrical Engineering
Oersteds Plads 349
Kgs. Lyngby, Denmark
ripit@elektro.dtu.dk

Zhe Zhang
Technical University of Denmark
Dept. of Electrical Engineering
Oersteds Plads 349
Kgs. Lyngby, Denmark
zz@elektro.dtu.dk

Michael A.E. Andersen
Technical University of Denmark
Dept. of Electrical Engineering
Oersteds Plads 349
Kgs. Lyngby, Denmark
ma@elektro.dtu.dk

***Abstract*— This paper presents a design and optimization of a high current planar transformer for very high efficiency dc-dc isolated boost converters. The analysis considers different winding arrangements, including very high copper thickness windings. The analysis is focused on the winding ac-resistance and transformer leakage inductance. Design and optimization procedures are validated based on an experimental prototype of a 6 kW dc-dc isolated full bridge boost converter developed on fully planar magnetics. The prototype is rated at 30-80 V 0-80 A on the low voltage side and 700-800 V on the high voltage side with a peak efficiency of 97.8% at 80 V 3.5 kW. Results highlights that thick copper windings can provide good performance at low switching frequencies due to the high transformer filling factor. PCB windings can also provide very high efficiency if stacked in parallel utilizing the transformer winding window in an optimal way.**

Keywords*— *Planar Magnetics, High Current DC-DC Converter, High Efficiency, PCB windings.

I. Introduction

The major trends in power electronics have been focused on increasing converters efficiency, increasing switching frequencies and power densities, decreasing converter weight and cost. Power semiconductors technology has seen large improvements due to the introduction of new wide bandgap materials and due to the improvements in the conventional silicon technology. However, this is not the case for passive components such as inductors and capacitors. The developments in the magnetic and dielectric materials have been more limited compared to the ones in the power semiconductors. Moreover, passive components represent a significant part in the volume, cost and weight of a power electronic converter.

Planar magnetics [1] have large potential for reducing the magnetic components manufacturing cost, increased component integration and increasing converter power density due to their good thermal performance. Planar transformers are often used for small low power dc-dc converters since the transformer windings are easily integrated on the same PCB with the power semiconductors and the control circuitry [2]. One of the major drawbacks of this type of magnetics comes from its large stray capacitance which is often unwanted in many commercial applications (e.g. due to increased EMI filter size) [3]. Moreover, for medium power or high current applications it is challenging to achieve high efficiency due to the low transformer window filling factor usually achieved with PCB windings [4].

This paper presents the design approach utilized for a high current planar transformer in a high current high efficiency dc-dc converter. Several winding arrangements are presented and the analysis is focused on winding ac-resistance and on winding leakage inductance. The analysis is validated based on an experimental prototype of a 6 kW dc-dc isolated full bridge boost converter (IFBBC, 30-80 V 0-80 A on the low voltage side and 700-800 V on the high voltage side) achieving a peak efficiency of 97.8 % with power flow from low voltage to high voltage side.

II. Planar Transformer and PCB Technology

Planar transformers are very suitable for low current applications moreover, creating an interleaved winding structure becomes natural with multilayer PCBs reducing ac-winding resistance and leakage inductance. One of the major challenges in the design of high current PCB windings [5] is the limitation in the PCB manufacturing technology in terms of copper thickness. In order to integrate high currents into PCB windings it is necessary to utilize multilayer PCB and even in this case with conventional copper thicknesses (from 1 oz. to 3 oz. or 35 µm to 105 µm) it is difficult to minimize the winding losses due to the rather low filling factor. After a study of the current production capabilities of several PCB manufacturers it was observed that copper thicknesses up to 6 oz. (210 µm) are easily achievable. Above this value the PCB production cost increases exponentially since it most of the machinery is not capable of handling such high copper thickness.

The following analysis and design are performed on a high current transformer for a dc-dc converter. The analyzed reference cases considers a multilayer PCB (6 layers) with 210 µm of copper thickness and 200 µm of insulation thickness. The multilayer PCB is compared

with very high copper thickness custom made PCBs (400 µm and 1500 µm copper bar).

III. DC-DC Converter for Fuel Cell Applications

The reference design is a 6 kW bidirectional IFBBC for bidirectional solid oxide electrolyzer/fuel cells (SOEC/SOFC) [6]. The converter specifications are defined according to the SOEC/SOFC stack characteristics as specified on Table I. For this topology a complete loss analysis was performed in [7] where it was highlighted how the power loss distribution varies depending on the converter operating point. In the selected topology, the transformer is beneficial since it allows achieving high efficiency with a high converter step-up ratio. However, the transformer design is critical since in the IFBBC the transformer is required to have low leakage inductance in order to minimize the current commutation loop which strongly affects the switching losses on the power semiconductors in the converter low-voltage side [8]. For this reason, in order to achieve high dc-dc conversion efficiency special care has been taken in order to minimize the transformer leakage inductance and ac-resistance.

IV. Transformer Design and Optimization

Transformer optimization procedures are focused on minimizing the transformer overall losses by minimizing the sum of the winding losses with the core losses [7].

TABLE I
SOFC and SOEC specifications for DC-DC converter design

	SOFC	SOEC	
Low Voltage (LV) side	30-50	50-80	[V]
Current (LV) side	40-0	0-80	[A]
High Voltage (HV) side	700-800	700-800	[V]
Power Rating	~1500	~6000	[W]

However, this paper does not analyze the complete transformer losses but highlights the differences for the analyzed winding topologies. Up-front calculations determined that a good balance between core losses and winding losses is achieved with three primary turns when the converter is operating with a switching frequency of 40 kHz. The analyzed transformer has a turn ratio of 8 defined by the topology, by the converter specifications and by the components ratings. Since the transformer leakage inductance is very critical for the candidate topology the goal was to analyze the trade-offs in the winding arrangements, leakage inductance and winding ac-resistance.

The structures that have been considered for the analysis are presented on Fig. 1: a simple primary-secondary structure (PS) Fig. 1a, a fully interleaved structure (PSPSPS) Fig. 1b, an interleaved structure with very thick windings for primary and secondary (PSPSP) Fig. 1c and a similar structure (PSPSP) only with thinner copper (2*400 µm in parallel, Fig. 1d). This last structure

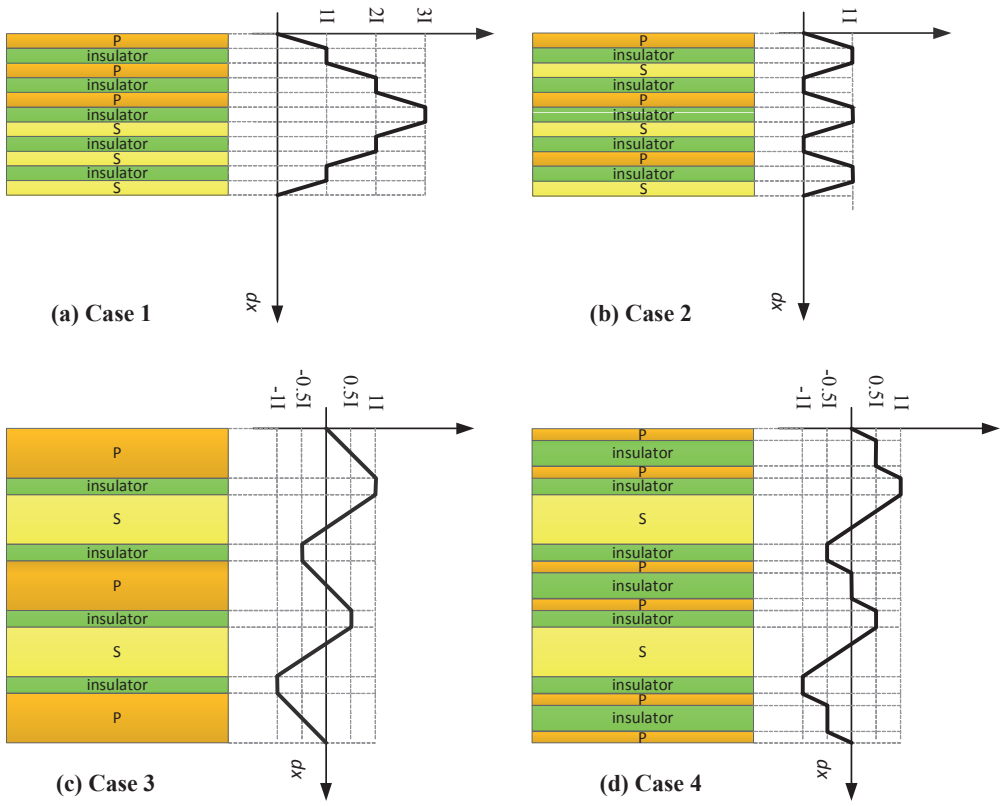


Fig. 1 Analysed windings arrangements, Case 1 and Case 2 with PCB copper thickness of 210 µm, Case 3 with very thick copper (1500 µm) and Case 4 with intermediate copper thickness (400 µm two layers in parallel for the primary winding).

aims to highlight the trade-offs between the windings copper thickness and their ac-resistance.

A. Theoretical Background and Analytical Analysis

The four cases are analyzed focusing on the windings ac-resistance and on the leakage inductance for the different configurations. The winding ac-resistance is calculated according to Dowels equations [9]; this takes into account the effect of the skin depth and the proximity effects (1) on the ac-resistance. The proximity effects (2) are included through the magneto-motive force (MMF) of each transformer layer. The totals ac-resistance is computed for each layer of the transformer windings based on (3). The transformer leakage inductance is calculated from the energy stored in the windings and leakage layers (4). This approach considers the MMF varying linearly in the conductor layers and constant in the insulation layers (as presented in [10]), as shown on Fig. 1. In the analyzed cases based on PCB windings the main assumptions are that the primary and secondary windings have the same copper and insulation thicknesses and that the winding window is completely filled.

$$\left(\frac{R_{ac}}{R_{dc}}\right)_{layer} = \frac{\xi}{2}\left[\frac{\sinh(\xi)+\sin(\xi)}{\cosh(\xi)-\cos(\xi)} + (2m-1)^2\frac{\sinh(\xi)-\sin(\xi)}{\cosh(\xi)+\cos(\xi)}\right] \quad (1)$$

$$m = \frac{\mathrm{MMF(h)}}{\mathrm{MMF(h)}-\mathrm{MMF(0)}} \quad (2)$$

$$R_{ac} = \sum_{layers}\left(\frac{R_{ac}}{R_{dc}}\right)_{layer}\cdot R_{dc,layer} \quad (3)$$

Where $\xi = \mathrm{h}/\delta$, h is the conductor height or copper thickness, δ is the skin depth in the conductor and m is >1 for non-interleaved multilayer windings, $\mathrm{MMF(h)}$ and $\mathrm{MMF(0)}$ are the MMFs values for the analyzed layer. In a similar way the transformer leakage inductance is computed starting from the overall energy stored in the primary and secondary windings and in the insulation layers, calculated from (4) and (5).

TABLE II
TRANSFORMER LEAKAGE INDUCTANCE

	Leakage	
Case 1	136.8	[nH]
Case 2	19.5	[nH]
Case 3	88.3	[nH]
Case 4	69.1	[nH]

$$E_{leakage} = \frac{1}{2}\mu_0\int_0^{h_w} H^2 l_w b_w dx \quad (4)$$

$$L_{leak} = \mu_0\frac{\mathrm{l_w}}{\mathrm{b_w}}\sum_{i=1}^{n} MMF_{layer}^2 h_{layer} \quad (5)$$

Where H the magnetic field of the layer, h_W is the total winding height, l_W is the transformer mean turn length, b_W is the winding width, MMF and h_{layer} are respectively the magneto motive-force and the height of the considered layer.

Cases three and four require more specific considerations in order to perform a proper analysis. These two cases consider the secondary winding realized with litz wire (two secondary winding sections with 12 turns each) and the primary winding with thick copper foil. The selection of litz wire for the transformer secondary was necessary due to the complexity of realizing a large number of turns with thick copper strands. The litz wire has 30 strands of 0.2 mm in diameter. In this case, different values of ξ has to be used for primary and secondary winding (1). Assuming ideal litz wires (woven and twist), with the ξ coefficeint for the litz wire is given by the litz wire stand diameter over the skin depth (6). This allows to properly calculate the ac-resistance for an ideal litz wire winding.

$$\xi_{\mathrm{litz\ wire}} = \frac{\mathrm{d_{litz\ strand}}}{\delta} \quad (6)$$

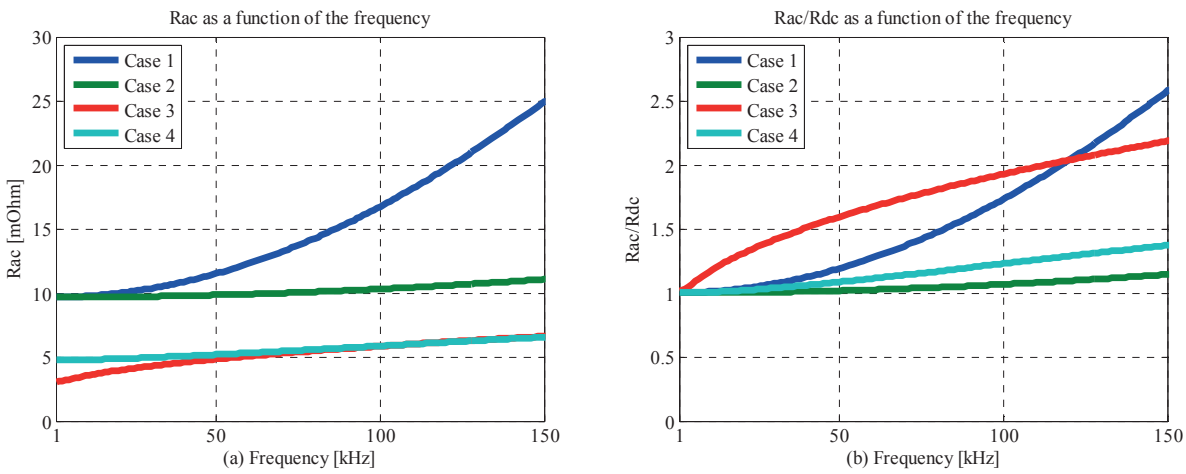


Fig. 2 Results from the analytical calculation of the ac-resistance for the four different cases in the 1-150 kHz range (a) and calculated ac-resistance over dc-resistance for all the analysed cases (b).

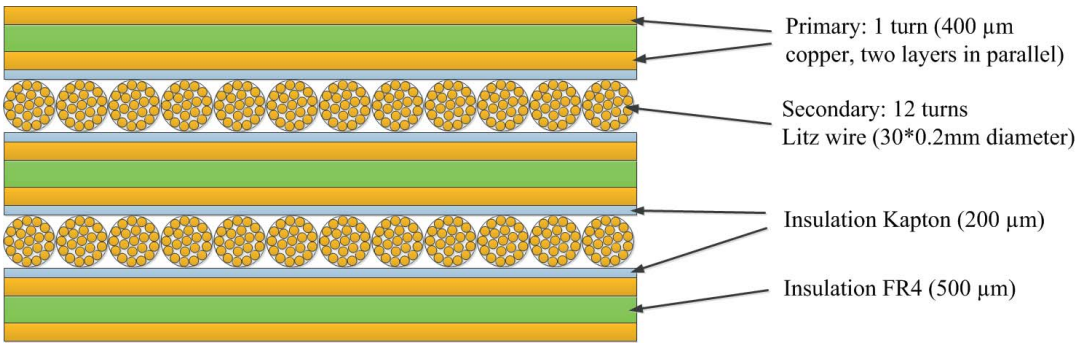


Fig. 3 Winding cross section of the realized transformer prototype according to Case 4, primary winding with thick copper and secondary winding with litz wires.

B. Analysis of the Designs

The cases analyze the stray parameters of different configurations in the 1-150 kHz frequency range; this is the expected operating range of magnetic components in hard-switched multi-kW converters. Results from the analytical analyses of the winding ac-resistance are presented on Fig. 2a and 2b; for the leakage inductance on Table II.

Case 1 and Case 2 (6 layers PCB windings with copper thickness of 200 µm) provide the highest ac-resistance due to the low winding window filling factor in for the planar E64 core pairs. The non-interleaved Case 1 (PS winding structure) suffers of high ac-resistance due to proximity effects, in facts the fully interleaved version Case 2 (PSPSPS winding structure) has minimal variation in ac-resistance over the analyzed spectrum range (Fig. 2a).

Case 3 and Case 4 have similar ac-resistance values even though Case 3 has a significant higher filling factor for the primary winding (a single layer of 1500 µm of copper in Case 3 vs. two layers of 400 µm in Case 4). The difference increases at lower frequencies: ac-resistance of Case 3 is lower than Case 4 due to the increase of the skin depth layer which allows to better utilize the thick copper layers. The increase of ac-resistance over dc-resistance is presented on Fig. 2b. Winding ac-resistance in the extreme thick copper (Case 3) rapidly increases mostly due to the large influence of the skin depth effect. However, even though the frequency increases (e.g. frequencies in the 100-150 kHz range) the thick copper interleaved structures of Case 3 and Case 4 can provide lower ac-resistance than the non-interleaved structure of Case 1.

The structure of Case 2 thanks to the fully interleaving provides the lowest increase in ac-resistance over the analyzed frequency range. However, also Case 4 has a similar gives an increase of ac-resistance close to the fully interleaved Case 2. Therefore, Case 4 represents a good trade-off for achieving a low ac-resistance and minimizing the amount of un-used copper due to due to skin and proximity effects. In fact, the low increase of ac-resistance over the dc-resistance observed in Case 4 is due to the

Transformer leakage inductance is another factor that significantly affects the converter performance. The leakage inductance for the analyzed cases is summarized on Table II. As expected Case 1 has the highest leakage inductance of the analyzed cases due to the large MMF values which give a large contribute in the leakage inductance calculations (5). Case 2 provides the lowers inductance thanks to a full interleaving structure and to the minimal thickness of each layer (both copper and insulation layers). The last two cases have similar leakage inductance however, separated parallel primary winding layers in Case 4 can provide a lower leakage inductance the 1500 µm copper thickness of Case 4.

The most interesting observation can be performed by analyzing the transformer equivalent winding ac-resistance (referred to the primary, Fig. 2a). Even though the windings are realized with thick copper, their ac-resistance at the converter switching frequency (40 kHz) is well below the winding resistance of the Case 1 and Case 2. This is due to the fact that by using a single PCB of 6 layers and with a copper thickness of 6 oz. (210 µm) per layer the transformer filling factor is low and its winding resistance is relatively high compared to the thick copper cases. On the other hand, the PCB windings (6 layers, Case 1 and Case 2) have a finished thickness of ~2.5 mm where the height of the transformer winding window is 10.2 mm (planar E64 pair). This would allow stacking three identical PCB windings (same winding geometry) in order to increase the transformer winding window filling factor and decrease both ac-winding resistance and leakage inductance. With the assumption of equal current distribution in the paralleled layers, it

TABLE III
TRANSFORMER CHARACTERISTICS

Turns ratio	8
Primary	3 turns
Secondary	24 turns
Core	2*E64 pairs
Core material	Magnetics R
Structure	P-S-P-S-P
Primary winding (P)	PCB 2*400 µm
Secondary winding (S)	30*0.2 mm litz wire
Insulation P-S	2*0.1 mm Kapton

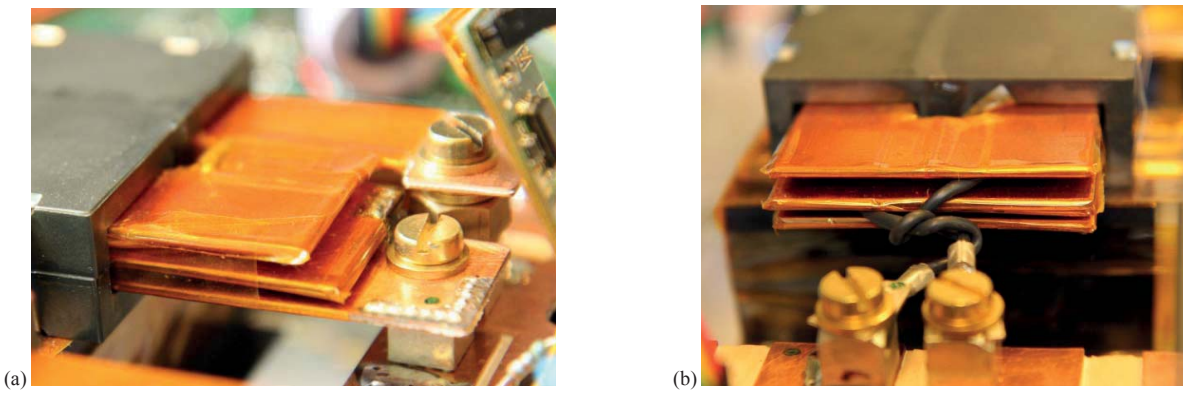


Fig. 4 Realised transformer prototype according to Case 4 design and specification according to Table III. Primary winding terminations shown on (a) and secondary winding terminations shown on (b).

would result in a reduction by a factor 3 and for both interleaved and non-interleaved case (Case 1 and Case 2). In this theoretical case, the ac-resistance would be reduced below the one achieved in Case 3 and Case 4, as well the leakage inductance.

C. *Transformer Prototype Constuction Details and Analysis*

In order to validate the performed design transformer was manufactured based on the winding arrangement of Case 4. This case combines the advantages of thick copper foil for the primary windings and minimizes the complexity of the construction by using litz wires for achieving a high number of secondary turns. The design is performed for a converter switching frequency of 40 kHz, as presented in [7].

A detailed cross section of the transformer winding is presented on Fig. 3; the transformer windings have three primary sections interleaved with two secondary sections (PSPSP structure). Each section of the primary winding is realized based on a custom two layer thick copper PCB where each copper layer has a thickness of 400 µm. Each section of the primary winding has one transformer turn composed by two copper layers in parallel. An insulation layer of FR4 (500 µm) separates the two copper layers (Fig. 3). Each secondary section accommodates 12 secondary turns of 30x0.2 mm litz wire for a total of 24 secondary turns. High voltage insulation between primary and secondary is guaranteed by a 200 µm layer of Kapton. The transformer core is based on two planar E64 core pairs of material R-type from Magnetics. The transformer characteristics and specifications are summarized on Table III.

The realized prototype is presented on Fig. 4a and 4b; where the details of the transformer primary terminations (Fig. 4a) and secondary terminations (Fig. 4b) are highlighted. Case 4 was used as a reference design since it could provide good performance within the analyzed cases and it was possible to realize a custom made laboratory prototype without encountering the manufacturing costs of a single PCB unit. Moreover, calculations in Case 4 were explicitly tuned for the real design case.

A precision impedance analyzer (Agilent 4294A) was

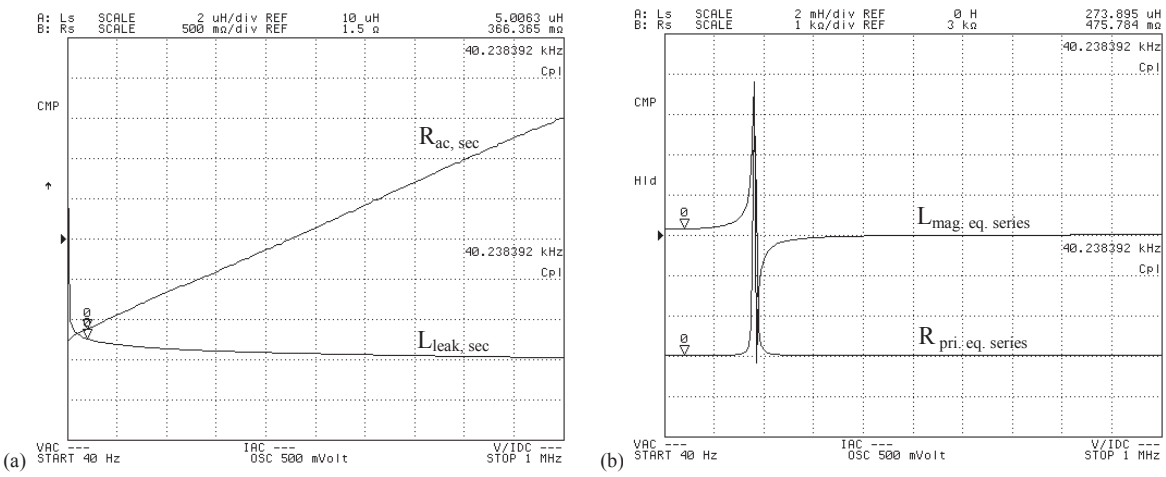


Fig. 5 Short circuit measurement of the transformer prototype characterized from the secondary side, ac-resistance and leakage inductance at 40 kHz. Open circuit measurement performed from the transformer primary side highlighting the magnetizing inductance at 40 kHz. Transformer characterization in the 40 Hz-1 MHz range. First resonance frequency at 180 kHz.

used to measure the transformer windings resistance and leakage inductance. Transformer parameters have been measured referred to the secondary. This was necessary since the parameters measured from the transformer primary side are very small (in the range of mΩ for the transformer resistance and of nH for the transformer leakage inductance). Measuring the transformer parameters on the secondary side significantly reduced the error due to terminations and allowed the impedance analyzer to operate in a measurement range with better accuracy. In fact, it is possible to observe that the high current screw terminations would introduce several nH of stray inductance.

D. Analysis of the Measurements on the Transformer Prototype

Measurements are performed in short and open circuit conditions in the 40 Hz to 1 MHz band to determine the electrical characteristics of the realized prototype, shown on Fig. 5a and 5b. With the transformer primary shorted by a low stray inductance connection, the total transformer leakage inductance was 5 µH with a total winding resistance of 366 mΩ (measured from the secondary, Fig. 5a). Transformer magnetizing inductance is relatively large compare to the transformer stray parameters, for this reason, the open circuit measurement is performed from the transformer primary side with the transformer secondary side open (Fig. 5b). The transformer magnetizing inductance is 273.9 µH at the converter switching frequency (40 kHz, Fig. 5b). The transformer has a first resonance at a frequency of 180 kHz however, this is not critical case since at this frequency the transformer has high impedance (impedance peak).

The transformer leakage values measured from the secondary side are reflected to the transformer primary side based on the transformer turns ratio Table III obtaining 5.72 mΩ and 78.2 nH. For the realized prototype, the leakage inductance is only 0.0286% of the magnetizing inductance. This value is low compared to regular transformers for dc-dc converters, in fact, leakage inductance is usually 0.1% or more compared to the magnetizing inductance. This also indicates a very high coupling between primary and secondary of the transformer.

A comparison of the ac-resistance and leakage inductance for the analyzed cases and for the transformer prototype is presented on Fig. 6a and 6b. The calculated ac-resistance at the converter switching frequency is 5.06 mΩ, this leads to an error of about 13%, Fig. 6a. The same error (in this case 13.2%) is observed between the calculated leakage (69.1 nH) inductance and the measured one (78.2 nH), shown on Fig. 6b.

The error observed in the ac-resistance can be explained by analyzing the litz wire structure and the current distribution in the litz wire strands. The calculations for the winding ac-resistance were performed considering a fully transposed litz wire, this is an ideal condition and ensures an optimal current distribution in the litz wire strands (minimum ac-resistance). The transposition of the litz wire strands in the transformer prototype is not ideal; in fact, inner strands are less transposed than the outer strands. This leads to an inhomogeneous current distribution in the litz wire strands and therefore, to a higher ac-resistance. Moreover, ac-resistance calculations for the ideal litz wire neglected the proximity effects of the litz wire inner strands on the outer strands which also increase the ac-resistance.

The error observed in the leakage inductance can be explained by analyzing the construction of the transformer prototype on Fig 4a and 4b. The transformer has not a coil former or a support to contain the windings in a predefined shape. This leads that the windings "relaxed" and filled completely the winding area of the EE64 core pairs. The relaxation led to an increase of the effective secondary winding height (the primary windings were assembled in a glued PCB structure) that gave a slightly larger leakage inductance than the expected calculations. Moreover, also transformer terminations have a large effect when measuring stray inductances in the range of nH.

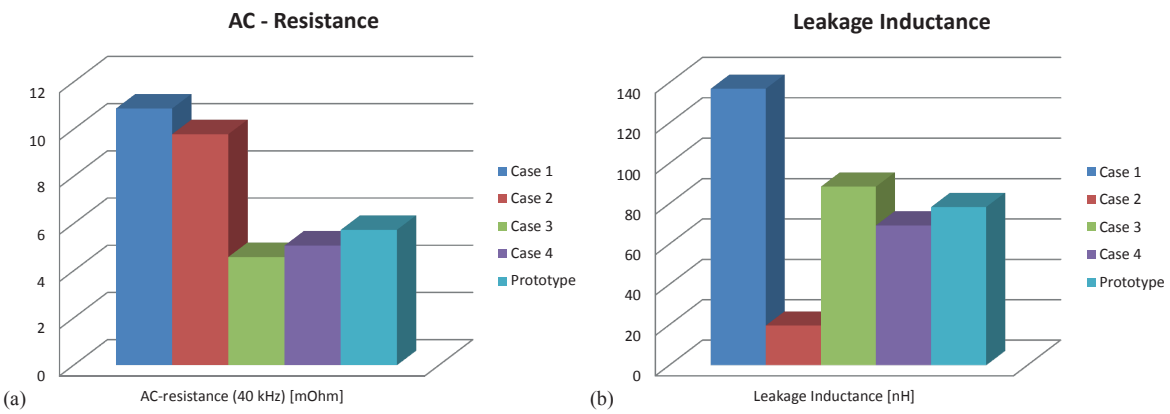


Fig. 6 Picture of the realized converter prototype with highlighted in blue the transformer prototype (a) and complete efficiency characterization with power flow from the low voltage to the high voltage side (b). Darkened area highlights the current limitation area of the converter.

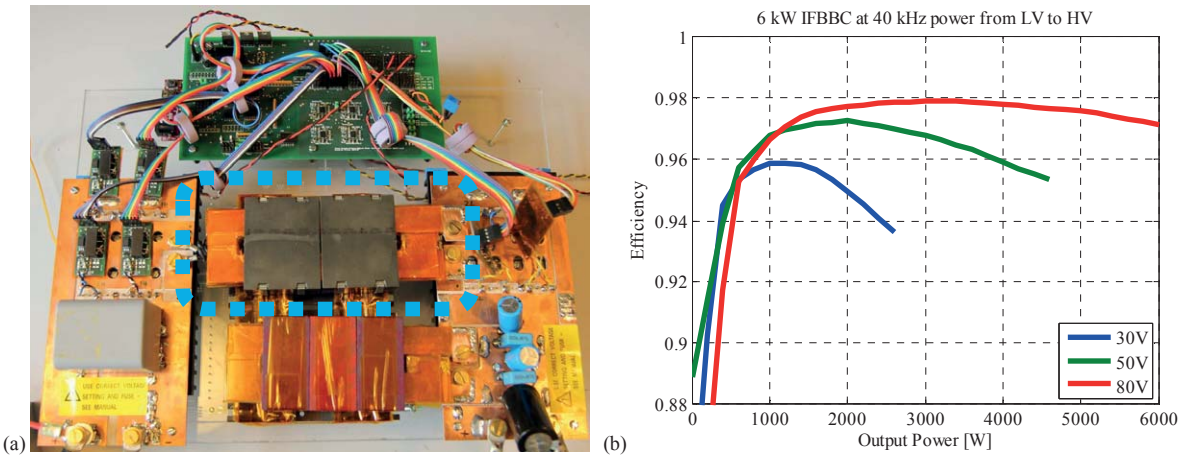


Fig. 7 Picture of the realized converter prototype with highlighted in blue the transformer prototype (a) and complete efficiency characterization with power flow from the low voltage to the high voltage side (b). Peak efficiency is 97.8% at the maximum converter input voltage (80 V 40 A). Efficiencies above 97% are already measured at 50 V. Maximum current: 80 A.

V. Experimental Results Based on a 6 kW Converter Prototype

The transformer design and optimization was performed as part of the design process of a high efficiency bidirectional dc-dc converter for fuel cell applications. The realized converter prototype is show Fig. 7a, where it is highlighted the main power transformer. The converter characteristics are defined by the fuel cell characteristics on Table I. The converter low voltage side is characterized by voltage ranged between 30 V up to 80 V with a maximum current of 80 A. The converter was designed for a switching frequency of 40 kHz.

The converter uses 4.1 mΩ MOSFETs on the low voltage side (8 devices arranged two in parallel for each switch in a full bridge) and 1200 V Si IGBTs with anti-parallel 1200 V SiC Schottky diodes on the high voltage side. The boost inductor is also realized with planar KoolMu material (three E6030 core pairs stacked in series) and thick copper PCB windings (custom designed). The transformer prototype was developed with custom made PCBs milled out from a PCB stack for the primary windings (as specified in Case 4). The initial design goal was to achieve a high current planar transformer fully based on PCB windings. However, due to manufacturing complexity and issues encountered during the milling process, the converter secondary windings were realized with litz wires, Table III. Therefore, the analytical analysis has to be updated based on these new constrains.

The transformer leakage inductance has been a major concern since in the selected topology it directly limits the primary MOSFETs current commutation time and therefore, their switching losses [7]. A complete loss analysis of the converter was presented in [7].

On Fig. 7b is presented a complete efficiency characterization of the converter. The design resulted in a dc-dc converter prototype with a peak efficiency of 80 V at ~3.5 kW of 97.8%. At the lowest input voltage (30 V) the peak efficiency was limited to 95.5%. Peak efficiencies are always measured when the current on the converter low voltage side is in the range of 40 A,

The converter is designed for bidirectional power flow however, efficiencies with power flow from the high voltage side to the low voltage side were lower than the ones measured with opposite power flow. The lower efficiency observed in this operating mode was due to the large switching losses of the high voltage power semiconductors (IGBTs). In this other operating mode the maximum measured efficiency was 96.5% at 80 V and 93.4% at 30 V. In this operating mode, a significant improvement in efficiency can be achieved by introducing SiC power semiconductors as replacement for Si IGBTs.

It is interesting to observe the influence of the transformer leakage inductance on the overall converter losses. Based on the four analyzed cases, the converter losses determined by the leakage inductance are calculated at different current levels (40 A, 60 A and 80 A); these are presented on Fig. 8a. It is observed that large leakage inductance values as in Case 1 would introduce large converter losses especially at high current levels (quadratic dependency, as observed in Fig. 8a and as presented in [7]). Case 2, thanks to full interleaving and to the low thickness of each layer, introduces very minimum additional losses in the converter. The realized transformer prototype based on Case 4 introduces an acceptable amount of losses for a converter with target efficiency around 98 %. The leakage inductance introduces a significant amount of losses only at high current levels, as shown on Fig. 8a. The leakage inductance in the transformer causes short avalanche transients of the MOSFETs on the converter low voltage side, as shown on Fig. 8b. The duration of the short avalanche condition depends on the input current level that determines the time interval required to commutate the input current through the transformer primary side windings (low voltage side). In this case, the avalanche interval with an input current 60 A is around 50-55 ns, as shown on Fig. 8b.

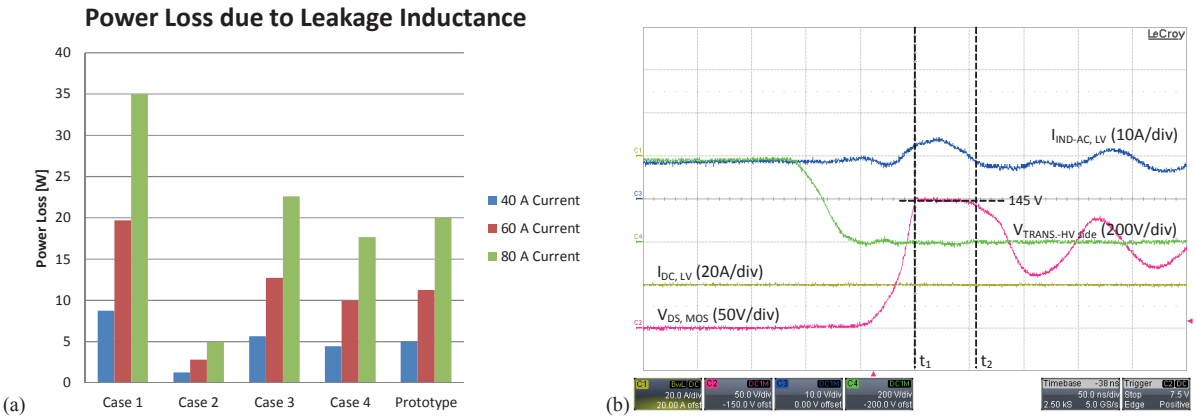


Fig. 8 Converter power loss due to transformer leakage inductance for the different analysed cases and at different current levels, shown on (a). Avalanche interval at 60 A current for the low voltage side MOSFETs, shown on (b). Low voltage side DC-current (Ch.1: 20 A/div), drain to source voltage of the low voltage side MOSFET (Ch.2: 50 V/div), boost inductor AC-current (Ch.3: 10 A/div) and high voltage side transformer voltage (Ch.4: 200 V/div).

VI. Conclusions

A design and analysis of a high current transformer based on planar magnetics has been presented. The analysis considered different windings structures and different copper thicknesses from 210 µm up to 1500 µm. Results highlighted that the larger copper thicknesses were preferable for achieving low ac-resistances at frequencies ranges around 40 kHz since this type of winding could achieve high filling factor. Cooper foil or thin copper bars become beneficial in transformers for low voltage high current converters especially at frequencies below 100 kHz.

Simple PCB windings struggle to provide the desired transformer performance in high current high efficiency dc-dc converters. However, state of the art PCB technology with copper thicknesses up to 6 oz. (210 µm) and allowing paralleling of multiple PCBs (e.g. three PCBs stacked on top of each other) would also allow to achieve high filling factor and high flexibility for interleaving. This would reduce both ac-resistance and leakage inductance down to levels that are only achievable with copper foil.

A transformer prototype was developed based on thick copper (400 µm) windings. The prototype was utilized in a dc-dc isolated boost converter achieving a peak dc-dc conversion efficiency of 97.8% at the highest input voltage and a peak efficiency of 95.5% at the lowest input voltage.

References

[1] Quirke, M.T.; Barrett, J.J.; Hayes, M., "Planar magnetic component technology-a review," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol.15, no.5, pp.884,892, Oct 1992.

[2] Ziwei Ouyang; Sen, G.; Thomsen, O.C.; Andersen, M. A E, "Analysis and Design of Fully Integrated Planar Magnetics for Primary–Parallel Isolated Boost Converter," Industrial Electronics, IEEE Transactions on , vol.60, no.2, pp.494,508, Feb. 2013.

[3] Pahlevaninezhad, M.; Das, P.; Djilali, H.; Jain, P.; Bakhshai, A.; Moschopoulos, G., "A novel planar transformer with integrated EMI suppression Y-caps applicable to high frequency high power DC-DC converters for automotive applications," Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2012), pp.346,351, 5-9 Feb. 2012.

[4] Gunewardena, T.R., "Manufacturing design considerations for planar magnetics," Electrical Insulation and Electrical Manufacturing & Coil Winding Conference Proceedings, 1997,pp.309,311, 22-25 Sep 1997.

[5] Pittini, Riccardo; Zhe Zhang; Ouyang, Ziwei; Andersen, Michael A. E.; Thomsen, Ole C.; "Analysis of planar E+I and ER+I transformers for low-voltage high-current DC/DC converters with focus on winding losses and leakage inductance," 7th International Power Electronics and Motion Control Conference (IPEMC 2012), vol.1, pp.488-493, 2-5 June 2012

[6] Zhang, Zhe; Pittini, Riccardo; Andersen, Michael A.E.; Thomsen, Ole C.; "A Review and Design of Power Electronics Converters for Fuel Cell Hybrid System Applications", Energy Procedia 2012, Volume 20, pp. 301-310.

[7] Pittini, Riccardo; Zhe Zhang; Andersen, Michael A. E.; " Isolated Full Bridge Boost DC-DC Converter Designed for Bidirectional Operation of Fuel Cells/Electrolyzer Cells in Grid-Tie Applications" 15th European Conference on Power Electronics and Applications (EPE-ECCE Europe 2013), 3-5 September 2013.

[8] Nymand, M.; Andersen, M.A.E.; "High-Efficiency Isolated Boost DC–DC Converter for High-Power Low-Voltage Fuel-Cell Applications," IEEE Transactions on Industrial Electronics, vol.57, no.2, pp.505-514, Feb. 2010.

[9] P. L. Dowell, "Effects of eddy currents in transformer windings," Proceedings of IEEE, vol.113, no.8, August 1966, pp. 1387-1394.

[10] Ziwei Ouyang; Thomsen, O.C.; Andersen, M.A.E.; "Optimal Design and Tradeoff Analysis of Planar Transformer in High-Power DC–DC Converters," IEEE Transactions on Industrial Electronics, vol.59, no.7, pp.2800-2810, July 2012.

Appendix J

High Current Planar Magnetics for High Efficiency Bidirectional DC-DC Converters for Fuel Cell Applications

2014 Applied Power Electronics Conference and Exposition (APEC 2014)

High Current Planar Magnetics for High Efficiency Bidirectional DC-DC Converters for Fuel Cell Applications

Riccardo Pittini
Technical University of Denmark
Dept. of Electrical Engineering
Kgs. Lyngby, 2800, Denmark
ripit@elektro.dtu.dk

Zhe Zhang
Technical University of Denmark
Dept. of Electrical Engineering
Kgs. Lyngby, 2800, Denmark
zz@elektro.dtu.dk

Michael A.E. Andersen
Technical University of Denmark
Dept. of Electrical Engineering
Kgs. Lyngby, 2800, Denmark
ma@elektro.dtu.dk

***Abstract*—Efficiency is one of the main concerns during the design phase of switch mode power supply. Planar magnetics based on PCB windings have the potential to reduce the magnetic manufacturing cost however, one of their main drawbacks comes from their low filling factor and high stray capacitance. This paper presents an analysis of different planar windings configurations focusing on dc and ac resistances in order to achieve highly efficiency in dc-dc converters. The analysis considers different copper thicknesses form 70 µm up to 1500 µm (extreme copper PCB) taking into account manufacturing complexity and challenges. The analysis is focused on a high current inductor for a dc-dc converter for fuel cell applications and it is based on FEM simulations. Analysis and results are verified on a 6 kW dc-dc isolated full bridge boost converter prototype based on fully planar magnetics achieving a peak efficiency of 97.8%.**

I. Introduction

Fuel cells represent an attractive technology for energy storage and energy production in grid-tie applications [1]. However, fuel cells typically operate at low voltage and high current and require a dc-dc converter as power interface to other components in the system [2][3]. Achieving high efficiency for these converter types is challenging and it often represents a trade-off between the dc-dc converter efficiency and its cost [4][5]. One of the largest cost figures in power electronics converters is represented by passive components. A solution for reducing the size of the passive components is to increase the switching frequency of power electronics converters despite a reduction in the converter efficiency [6]. High switching frequencies [7] are widely used in low power applications were efficiency around 90% are usually considered a high value. This is not the case for multi-kW applications for renewable energies where the demand of high efficiency resulted in commercial products with 98%+ efficiency (e.g. solar inverters [8]). New power semiconductors allow higher switching frequencies, high efficiency and at the same they allow smaller passive components [9]. However, at multi-kW power levels current magnetic components such as inductors and transformers, tend to become bulky, difficult to manufacture and expensive as most of the magnetic components are custom designed.

Planar magnetics represent an attractive technology for reducing the magnetic components manufacturing cost and for increasing components integration [10]. This advantage is due to the good thermal performance of planar magnetic core and to the possibility of integrating the inductor or transformer windings in printed circuit boards (PCB) together with the other converter circuitry [11] (e.g. with the power and control stages). These types of magnetics are often used in low power or low current converter. Designing magnetics components based on multilayer PCB windings allows easily creation of interleaved structures which might be beneficial for reducing leakage inductance and ac-resistance. On the other hand, it is very challenging to design high current high power planar magnetics (e.g. for fuel cell dc-dc converters [12]) since copper thicknesses used in standard PCB productions are very low (typically between 18 and 70 µm). This would result in high winding losses or in an oversized magnetic component. Paralleling multiple PCB would increase the winding area filling factor, but PCB's with standard copper thicknesses do not allow achieving high filling factor [13]. Increasing copper thickness is a key element for achieving high filling factor, reduce magnetic components size and achieve high efficiency.

The paper presents an analysis of different planar winding technologies and configurations performed during the design phase of a high current planar inductor. Each case is analyzed based on 2D finite element analysis (FEM) performed with Ansoft Maxwell. Analysis and calculations are validated on an experimental prototype of an isolated full bridge boost converter (IFBBC) for bidirectional fuel cells applications. The prototype uses a high current planar inductor which was developed based on very thick copper PCB windings and planar KoolMu cores. The converter prototype has a power

Project sponsored by the Danish Energy Technology Development and Demonstration Programme (EUDP) "Green Natural Gas", 2011-2014.

rating of 6 kW, the low voltage side is characterized by 30-80 V and currents up to 80 A while the high voltage side is designed as interface to a grid tie inverter (700-800 V). The developed converter prototype is based on fully planar magnetics and it was proved to achieve very high efficiency (up to 97.8% peak).

II. Planar Magnetics and PCB Windings Technology

In the latest years PCB technology had significant improvements; this allowed large cost reductions for conventional PCB productions. These are mostly limited to copper thicknesses in the 0.5-2 oz. range (17.5-70 µm) and multilayer boards. Most of the current machinery used in the PCB production process can operate with high copper thicknesses (typically up to 6 oz. or 210 µm), however above these values the manufacturing cost significantly increase since only a limited number of companies are prepared to support higher copper thickness. In order to evaluate the differences between multilayer PCBs with ultra-thick copper (e.g. 1500 µm and 400 µm, Fig 1a, 1b and 1c), thick copper (210 µm, Fig. 1d) and thin copper (e.g. 70 µm, Fig. 1e) are considered.

Thin copper (70 µm) cases are taken into account since they represent an economic and easy to manufacture solution. Thick copper (210 µm) represent a slightly more expensive solution however, this has large potentials since it is supported by most of the current production lines. Ultra-thick copper (>210 µm) is analyzed in order to verify if it could provide a significant advantage over thick copper (210 µm). This could justify larger manufacturing costs. In general, thin and thick copper PCBs have high one-off setup cost; these costs have minimal influence on the overall production cost when several panels are manufactured. All the analyzed cases are summarized in Table I. For all cases the insulation is FR4 material with a thickness between 200 µm (minimum value) and 500 µm.

TABLE I
Analyzed Cases for a Five Turns Inductor

	Copper Thickness	Isolation(FR4) Thickness	Layers (in parallel)
Case 1	1500 µm	200 µm	1
Case 2	400 µm	200 µm	3
Case 3	400 µm	500 µm	2
Case 4	210 µm	200 µm	4
Case 5	70 µm	200 µm	7

The presented work focuses on a high current inductor for dc-dc converters for fuel cell applications. The analysis is performed around an EE core pair, as shown on Fig. 1f. The selected core (E6030) has a winding window of 10x20 mm and is available both as ferrite and as a distributed gap (KoolMu) materials. The inductor was designed for a dc-RMS current of 80 A with an inductance of 20 µH.

III. Methodology and Theoretical Background

Designing a high current inductor for a high efficiency converter require taking into account both inductor core losses

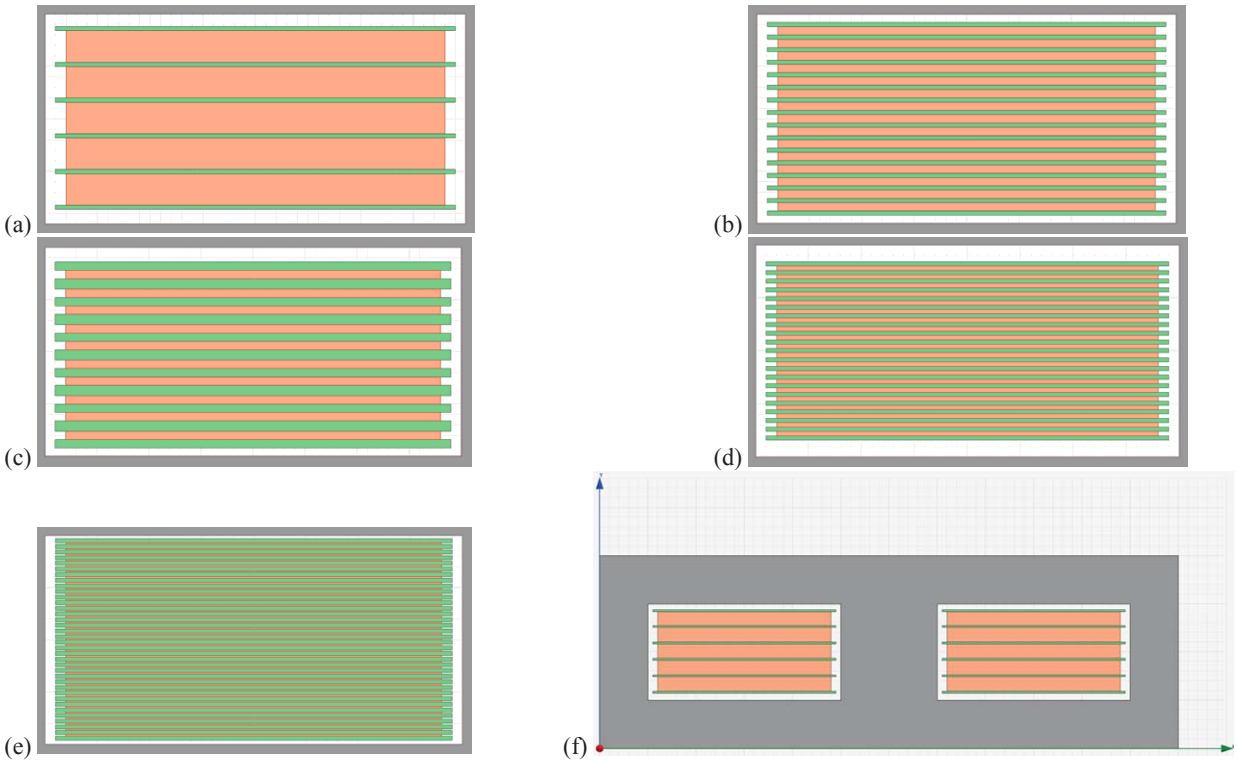


Fig. 1: Different analysed cases: 1500 µm (a), 400 µm three layer in parallel (b), 400 µm two layer in parallel and increased isolation thickness (c), 210 µm (d) and 70 µm (e). Isolation layers in green and cupper layers in orange. Example of a 2D structure implemented in Ansoft Maxwell (f).

and winding losses. Core losses are determined by the ac inductor current which derived from the inductor turns and inductance value. With upfront calculation it was determined that the inductor is required to have five turns over a stack of three sets of EE6030 core pairs. The following analysis focuses on the winding losses, the current density distribution and on the relationship with the filling factor. One assumption used in the analysis is that parallel windings of the same turn are equipotential and therefore, there is no energy stored in the stray capacitance within paralleled windings of the same turn. This results that the inductor stray capacitance is given by the capacitance between each turn, this is independent from the number of parallel layers of each turn. For this reason, the winding stray capacitance is the same in all analyzed cases and, therefore it is not analyzed.

A. Analytical Approach

Winding dc-resistance can be easily calculated from the winding cross sectional area (A_{cu}), the inductor turns (N) and the inductor mean turn length (MLT). This is simply expressed by (1) and it assumes constant cross sectional area of the conductor (interconnections between different layers in a planar inductor are neglected).

Slightly more complex is the analysis of the ac-resistance, this has to take into account the operating frequency, the winding arrangement-geometry, the conductor material and temperature, skin and proximity effects. The most common approach is based on Dowell's analysis [14]; this is considered a 1D approach which assumes that the magnetic core winding area is completely filled by the windings. In this case the ratio between the ac and dc resistances is calculated as in (2). The two parts of the equation takes into account the skin effect which is represented by the left side term of (2) in the squared brackets and the proximity effects which are taken into account by the right term in (2) in the squared brackets. In order to take into account the proximity effects it is necessary to consider the winding structure. Arranging the windings in a single layer structure can significantly reduce the ac-resistance since proximity effects are minimized [14]. This effect is due to the magneto motive force (MMF) of each winding layer; it is taken into account in the second term of equation (2) with the m factor from equation (3). The MMF varies depending on which inductor layer is analyzed and therefore, dc and ac resistances are computed for each single layer. Therefore, the total winding ac-resistance is obtained as in equation (4).

$$R_{dc} = \delta_{\mathrm{cu}} \cdot \frac{N \cdot MLT}{A_{cu}} \tag{1}$$

$$\left(\frac{R_{ac}}{R_{dc}}\right)_{layer} = \frac{\xi}{2}\left[\frac{\sinh(\xi) + \sin(\xi)}{\cosh(\xi) - \cos(\xi)} + (2\mathrm{m} - 1)^2 \frac{\sinh(\xi) - \sin(\xi)}{\cosh(\xi) + \cos(\xi)}\right] \tag{2}$$

$$m = \frac{\mathrm{MMF(h)}}{\mathrm{MMF(h)} - \mathrm{MMF(0)}} \tag{3}$$

$$R_{ac} = \sum_{layers} \left(\frac{R_{ac}}{R_{dc}}\right)_{layer} \cdot R_{dc,layer} \tag{4}$$

Where $\xi = \mathrm{h}/\delta$, h is the conductor height or copper thickness, δ is the skin depth in the conductor and $\mathrm{m} > 1$ for non-interleaved multilayer windings, $\mathrm{MMF(h)}$ and $\mathrm{MMF(0)}$ are the MMFs values for the analyzed layer.

B. Finite Element Analysis or Method (FEA or FEM)

Finite element analysis is used to evaluate the different cases and to verify the selected design prototype. There are mostly there 1D, 2D and 3D.

1) 1D FEM

1D finite element analysis performed similarly to the analytical approach; it is commonly used for analysis of chemical processes. 1D analysis is often referred as a 2D analysis taking into account that the magnetic flux has a single one-dimensional component [15].

2) 2D FEM

2D analysis considers a two dimensional representation of the analyzed component. The approach can consider two symmetries: an axial symmetry over a revolution axis (e.g. when analyzing a toroid) or axial-infinity symmetry (e.g. when the component 2D section is small compared to its extension over the third axis). In the analyzed case simulations are performed on the inductor cross section (two-dimensional magnetic flux). The major advantage of this approach is its limited computational time however, it cannot take into account the end effects due to the limited core geometry.

3) 3D FEM

3D FEM is the most suitable analysis for complex geometries and it can provide the highest accuracy compared to 1D and 2D FEM. 3D FEM takes into account the limited core geometry and its effects on the magnetic structure (e.g. part of the windings no covered by the magnetic core). However, it is very time consuming especially when a fine mesh is required for solution convergence. Symmetry axis can be beneficial for analyzing only a small section of the complete object and reducing the computation time.

C. Windings Configurations and FEM Analysis

Different windings configurations and manufacturing techniques are considered [16], as shown in Table I. As reference case an inductor based on a planar magnetic core E6030 is used. The analyzed frequency range is from 10 kHz up to 250 kHz which represents the interesting frequency range for a multi-kW dc-dc converter. Cases, shown in Fig. 1, are simulated in with 2D finite element analysis using Ansoft Maxwell; the case inductors have 5 turns and the ac current amplitude is 10 A_{RMS}.

IV. Analysis of the Results

Results from the 2D FEM analysis of the different cases are presented below focusing on ac-current density, dc and ac resistances and relation with the filling factor.

A. AC-Current Density Distribution

At first the ac-current density in the windings for the different configurations is analyzed. The current density distribution in the inductor windings for the five analyzed configurations are presented on Fig. 2: 1500 µm, 400 µm (3 layers in parallel), 400 µm (2 layers in parallel and higher insulation thickness), 210 µm (4 layers in parallel) and 70 µm (7 layers in parallel).

At low frequencies (10 kHz, left on Fig. 2) the thick copper configuration is beneficial in terms of ac-resistance since a large portion of the copper is used. However, there is still a large part of the copper where the current density is low, as shown on Fig. 2a left. This is not the case for paralleled PCB layers with thinner copper thicknesses; in this case the current density is much more homogeneous with minor areas with lower current density, as shown on Fig. 2d left. In this case some winding layers have completely homogenous current density. At higher frequencies (50 kHz, in the middle on Fig. 2) the current density decreases in the central part of the windings and it is possible to observe high negative current densities due to proximity effect of neighbor layers. These effects increase the winding ac-resistance especially for the thick copper windings. This phenomenon is well known and increases as the ac current frequency increases (eddy current effects) as observed on the right of Fig. 2. It is possible to observe that the current distribution in the layers is very similar independently on the copper thickness. The current is concentrated on a thin layer on Fig. 2a and this layer thickness is close to the current density in the thinner PCB layers as in case Fig. 2d.

One major difference between thick copper windings and conventional multilayer PCB windings is that the filling factor is very different from one configuration to the other therefore, for the same magnetics size the dc and ac resistances are affected. For these reasons, the filling factor is used in the

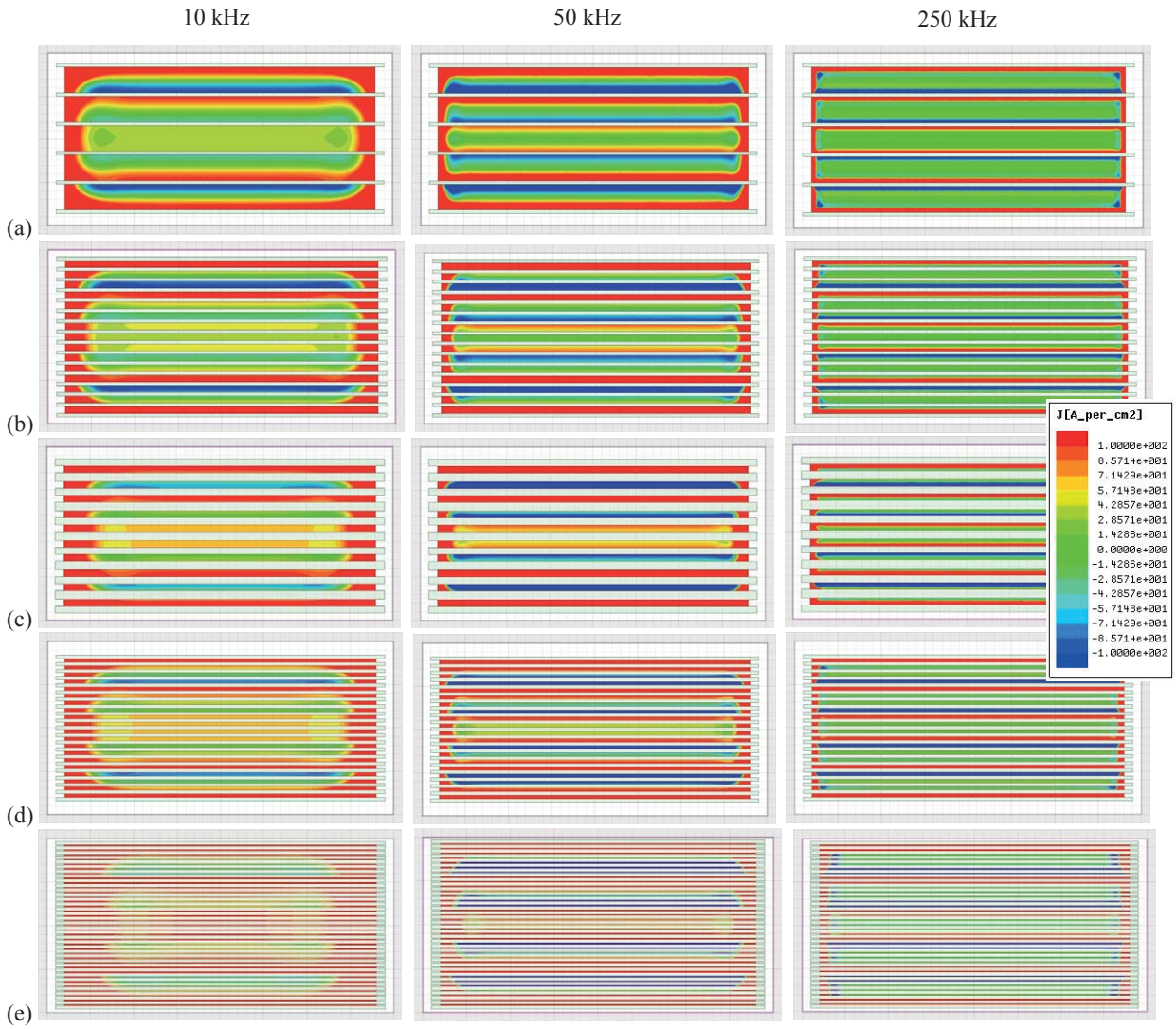
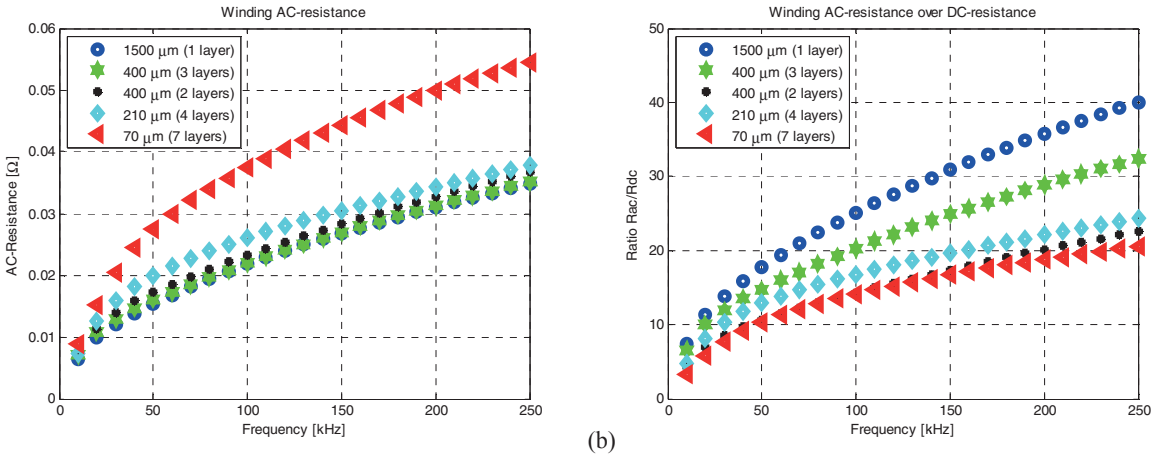


Fig. 2: Current density distribution for four cases of a 5 turns inductor: Case 1 1500 µm (a), Case 2 400 µm 3 layers in parallel (b), Case 3 400 µm 2 layers in parallel (c), Case 4 210 µm 4 layers in parallel (d) and Case 5 70 µm 7 layers in parallel (e). On the left current density at 10 kHz, in the centre at 50 kHz and on the left at 250 kHz. Current density from 100 A/cm^2 (red) to -100 A/cm^2 (blue); green colour corresponds to low current density (~0 A/cm^2).



(a) (b)

Fig. 3: Winding ac-resistance of the different configurations as a function of the frequency as shown in (a). Ratio between the ac-resistance and the dc-resistance as a function of the frequency as shown in (b).

analysis of the different configurations.

B. *Winding AC-Resistance*

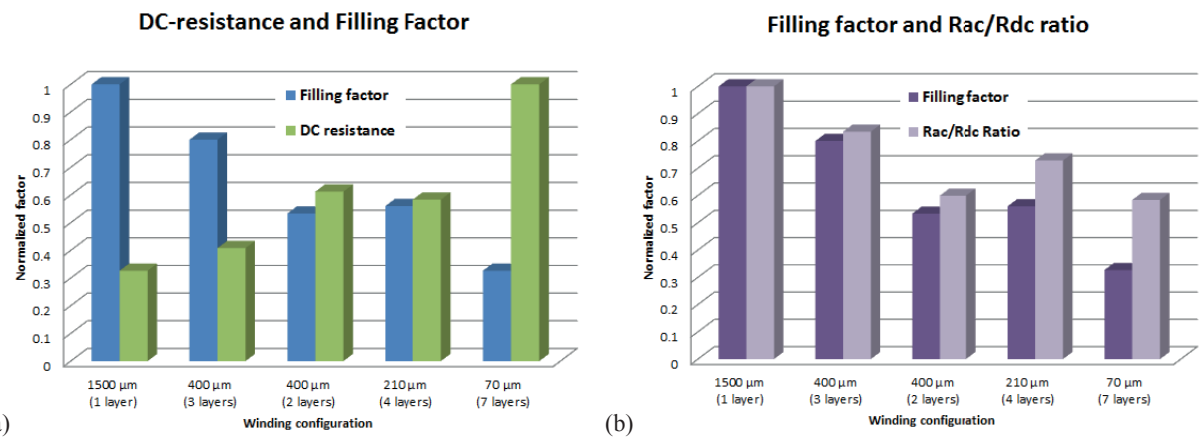
The analysis performer on the ac-current density can also be used for evaluating the winding ac-resistance. More uniform current densities results in lower winding ac-resistance; vice versa large variations in the current density and large areas with low current density results in high ac-resistances.

Based on the analyzed cases, on Table I, the winding resistance at different frequencies is extracted from the Joule winding losses. The windings ac-resistance is presented on Fig. 3a covering the entire 1-250 kHz range. It is observed that the highest copper thicknesses are also providing the lowest ac-resistance; this is valid for all the analyzed frequency range this is due to the large amount of copper provided by the thick copper cases (higher fill factor). This is interesting because it shows that thin copper layers could not really provide a significant benefit in this frequency range.

Another factor that as to be taken into account it is the ratio between the ac-resistance and the dc-resistance. This is presented on Fig. 3b. As expected the increase in ac-resistance over the dc-resistance is higher in the cases with large copper thickness (e.g. Case 1 and Case 2, shown on Fig. 3b). However, in the analyzed frequency range the increase in ac-resistance is compensated by the high filling factor and therefore, by the large amount of copper (lower absolute ac-resistance as shown on Fig. 3a). It is interesting to observe that Case 2 and Case 3 have the same copper thickness (400 µm) and different number of paralleled layers (3 and 2 paralleled layer). In these cases the increase of the ac-resistance is lower in the in the two parallel layers case (as shown on Fig. 3b).

C. *Filling Factor and Relation to Winding AC and DC-Resistance*

The winding area filling factor has a strong influence on both ac and dc resistances. High copper thickness can provide high filling factor (e.g. up to 0.68 for Case 1) and, therefore, low dc-resistance, Fig 4a. Having very large filling factor allows reducing the conduction losses in the inductor or



(a) (b)

Fig. 4: Window filling factor and dc-resistance for the analysed cases (a). AC-resistance of the different configurations as a function of the frequency (b). Values normalized to the maximum: normalize filling factor value (1) corresponds to 0.675, normalized dc-resistance value (1) corresponds to 3.03 mΩ and normalized Rac/Rdc ratio value (1) corresponds to 17.7. Reference frequency 50 kHz.

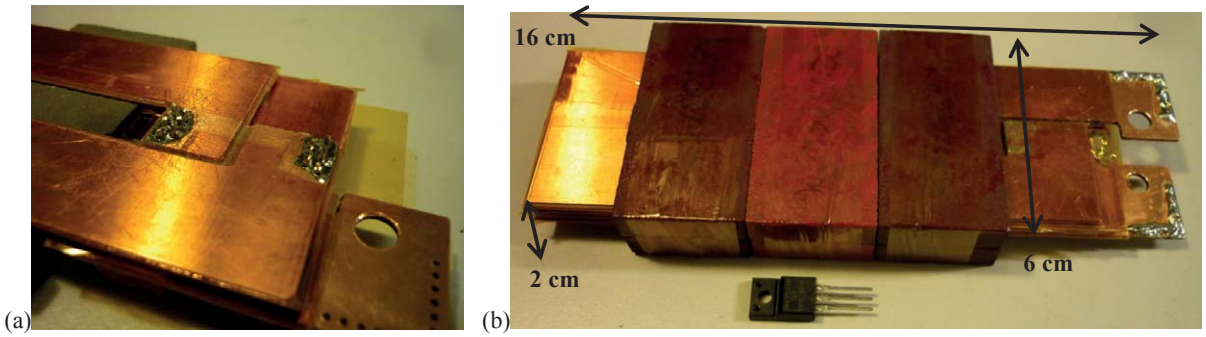


Fig. 5: Pictures of the realized inductor prototype, details of the interconnections (soldered pin-vias) between the inductor turns (a) and complete inductor compared to a TO-220 package (b). The large holes in the copper layers are the high current terminals of the inductor.

decreasing the inductor volume compared to lower filling factors. It is important to observe the relation between the filling factor and the increase of ac-resistance over dc-resistance for the analyzed cases. It is possible to contain the increase of ac-resistance over the dc-resistance by using two instead of three paralleled layers and increase the insulation layer between these ones, as shown on Fig. 4b columns two and three. The case with two parallel layer instead of three has lower Rac/Rdc ratio, this results that even though the filling factor is reduced the ac-resistances in the two cases are comparable (as shown in Fig. 3a).

V. Experimental Prototype and Validation

Based on the case studies a high current inductor prototype was designed for an IFBBC topology. The major focus in the converter design and optimization was to limit the overall converter power loss and achieve high efficiency with planar magnetics.

The inductor prototype was realized with two paralleled copper foil conductors of 400 µm thicknesses separated by a 500 µm layer of FR4. The inductor's five turns were manufactured with a CNC machine and interconnected with high current vias, Fig. 5a. The inductor is designed at 20 µH and rated for dc-currents up to 80 A with ripple currents of 15 A_{RMS}. The inductor prototype is presented on Fig. 5b.

The inductor was characterized with a precision impedance analyzer (Agilent 4294A rev. 1.1). The instrument can measure impedances with frequencies from 40 Hz up to 110 MHz with a basic impedance accuracy of ±0.08%. The inductor winding dc-resistance was measured at 100 Hz, as shown on Fig. 6a and the ac-resistance was measure at the inductor operating frequency (80 kHz) shown on Fig. 6b. The measurement was performed by removing the inductor core in order to remove the core losses from the measurement. This can be observed from the inductance measurements in Fig. 6b where the inductance value is only 1.3 µH (inductor without core). At low resistance values (around 1-2 mΩ) the instrument is at its limits for the specified operating range and therefore, larger error compared to the absolute impedance accuracy is expected. A comparison of the calculated results from the 2D FEM analysis and the measurements performed on the inductor prototype are presented on Table II. The FEM values have a good match with the measurements; the mismatch is less than 10% which is good considering that 2D FEM is less accurate than 3D FEM.

The inductor cores are three core pairs of KoolMu

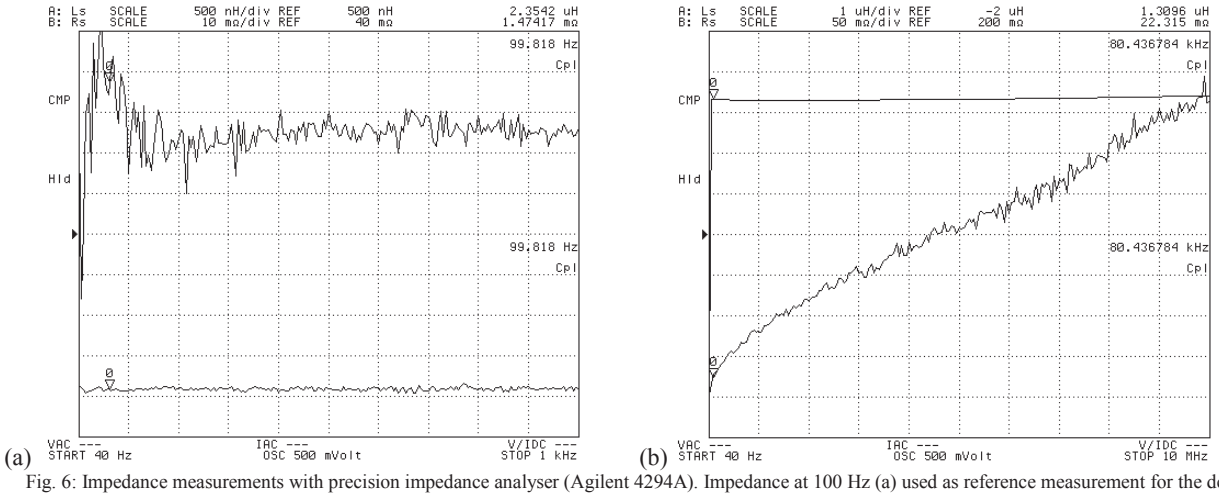


Fig. 6: Impedance measurements with precision impedance analyser (Agilent 4294A). Impedance at 100 Hz (a) used as reference measurement for the dc-resistance (40 Hz-1 kHz sweep) and measurements at 80 kHZ (b) (40 Hz-10 MHz sweep). Measurement performed on the inductor windings with no core.

TABLE II
ANALYZED AND PROTOTYPE OF CASE 3 FOR A FIVE TURNS INDUCTOR

	Calculated (FEM 2D)	Measured	Mismatch
R_{DC}	1.6 mΩ	1.47 mΩ	8.5%
R_{AC}	20.99 mΩ	22.3 mΩ	6.3%
R_{AC}/R_{DC}	12.9	15.1	17%

material: two pairs have a relative permeability of 90 and one pair has a relative permeability of 26. A measurement of the ac-resistance and inductance at 80 kHz is performed on the complete inductor (including the cores) and shown on Fig. 7. The measured inductance is 19.7 µH and the ac-resistance which includes also core losses is 82.8 mΩ.

The inductor is part of a dc-dc bidirectional isolated full bridge boost converter for fuel/electrolyzer cells, Fig. 8a. The dc-dc converter uses 120 V 4.1 mΩ MOSFETs (eight devices, two in parallel in a full bridge configuration) in the low voltage side bridge; 1200V Si IGBTs rated at 15 ARMS in the high voltage side bridge and a transformer with a 1:8 turns ratio. The dc-dc converter's efficiency was characterized at different voltage levels in the 30-80 V range. Peak efficiencies up to 97.8 % in boost mode (Fig. 8b) have been measured. The efficiency in buck mode (power flow from the high voltage side to the high voltage side) is limited to ~96.5% due to the high IGBT's switching losses.

VI. CONCLUSIONS

The paper analyzed different planar winding configurations and technologies for high current planar magnetics. It was proved that selecting thin copper layers for PCB windings it is not always beneficial for achieving low dc and ac resistances for high current high power dc-inductors with operating frequencies in the 10-250 kHz range. Good results in terms of both ac and dc resistance were achieved by using 400 µm copper layers or by increasing the insulation thickness between the layers and reducing the number of paralleled layers. This last solution limited the increase of the ac-resistance as a function of the frequency and provided at

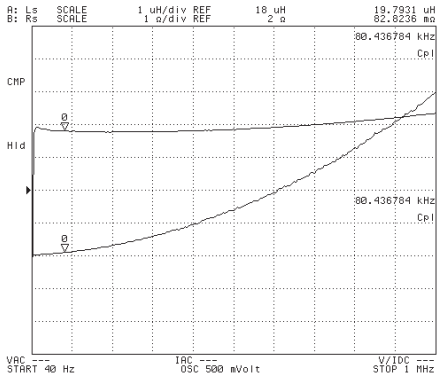


Fig. 7: Impedance measurements with precision impedance analyser (Agilent 4294A). Inductor characteristics at 80 kHz (cursor) and over the entire frequency sweep 40 Hz-1 MHz).

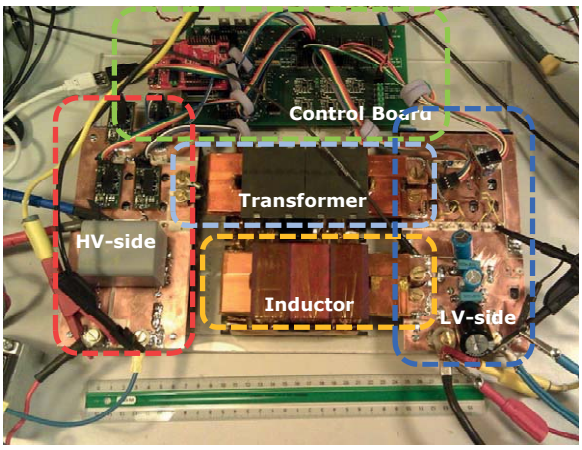
the same time a suitable high filling factor which is essential for low dc-resistance. It was observed that even though the Rac/Rdc resistance increases more in the thick copper windings compared to the thin ones, thick copper winding are still advantageous due to their high filling factor in the analyzed frequency range (10-250 kHz).

Based on the performed analysis a prototype of a high current planar inductor based on distributed gap material was developed. The inductor prototype was used on an isolated full bridge boost converter for bidirectional fuel cells. The prototype is based on thick copper PCB windings and it was capable of achieving peak efficiencies up to ~97.8% and ~96.5% depending on the converter power flow. Good match between simulations and experimental results was achieved.

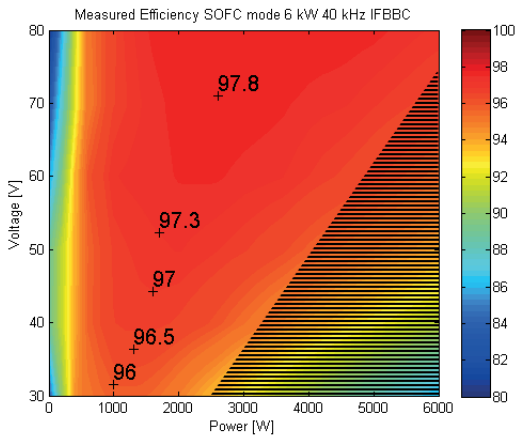
REFERENCES

[1] Lee, J.; Han, B.; Cha, H., "Operational analysis of DC micro-grid using detailed model of distributed generation," 2009 Transmission & Distribution Conference & Exposition: Asia and Pacific, pp.1,4, 26-30 Oct. 2009.

[2] Han, B.-M.; Jun-Young Lee; Yu-Seok Jeong, "Power conditioning



(a)



(b)

Fig. 8: Pictures of the realized converter prototype (a) (30-80 V 0-80 A low voltage side, 700-800 V high voltage side, rated power 6 kW current limitation 80 A) and measured efficiency with power flow from the low voltage to the high voltage side (b). Darkened area indicates current limitation of the dc-dc converter, only transient operation allowed in this area.

system for fuel cell with 2-stage DC-DC converter," Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2010), pp.303-308, 21-25 Feb. 2010.

[3] Zhang, Zhe; Pittini, Riccardo; Andersen, Michael A.E.; Thomsen, Ole C.; "A Review and Design of Power Electronics Converters for Fuel Cell Hybrid System Applications", Energy Procedia 2012, Volume 20, pp. 301-310.

[4] Kim, K.A.; Lertburapa, S.; Chenyang Xu; Krein, P.T., "Efficiency and cost trade-offs for designing module integrated converter photovoltaic systems", IEEE Power and Energy Conference at Illinois (PECI 2012), pp.1,7, 24-25 Feb. 2012.

[5] Sharma, R.; Hongwei Gao, "Low cost high efficiency DC-DC converter for fuel cell powered auxiliary power unit of a heavy vehicle", IEEE Transactions on Power Electronics, vol.21, no.3, pp.587,591, May 2006.

[6] Pavlovsky, M.; de Haan, S.; Ferreira, J.A., "Reaching High Power Density in Multikilowatt DC–DC Converters With Galvanic Isolation," IEEE Transactions on Power Electronics, vol.24, no.3, pp.603,612, March 2009.

[7] Knott, Arnold; Andersen, Toke M.; Kamby, Peter; Madsen, Mickey P.; Kovacevic, Milovan; Andersen, Michael A.E., "On the ongoing evolution of very high frequency power supplies", Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2013), pp.2514,2519, 17-21 March 2013.

[8] Mallwitz, R.; Engel, B., "Solar power inverters", 6th International Conference on Integrated Power Electronics Systems (CIPS 2010), pp.1,7, 16-18 March 2010.

[9] Biela, J.; Schweizer, M.; Waffler, S.; Kolar, J.W., "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors", IEEE Transactions on Industrial Electronics, vol.58, no.7, pp.2872,2882, July 2011.

[10] Quirke, M.T.; Barrett, J.J.; Hayes, M., "Planar magnetic component technology-a review", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol.15, no.5, pp.884,892, Oct 1992.

[11] Ouyang, Z.; Acanski, M.; Popovic, J.; Ferreira, J.A.; Thomsen, O. C.; Andersen, M. A E, "Design Considerations of Very Low Profile Coupled Inductors for Flexible Photovoltaic Module", 7th International Conference on Integrated Power Electronics Systems (CIPS 2012), pp.1,8, 6-8 March 2012.

[12] Pittini, Riccardo; Zhe Zhang; Andersen, Michael A. E.; " Isolated Full Bridge Boost DC-DC Converter Designed for Bidirectional Operation of Fuel Cells/Electrolyzer Cells in Grid-Tie Applications" 15th European Conference on Power Electronics and Applications (EPE-ECCE Europe 2013), 3-5 September 2013.

[13] Nymand, M.; Madawala, U.K.; Andersen, M.A.E.; Carsten, B.; Seiersen, O.S.; "Reducing ac-winding losses in high-current high-power inductors", 35th Annual IEEE Conference of Industrial Electronics (IECON 2009), pp.777-781, 3-5 Nov. 2009.

[14] P. L. Dowell, "Effects of eddy currents in transformer windings," Proceedings of IEEE, vol.113, no.8, August 1966, pp. 1387-1394.

[15] Pernia, A.M.; Nuno, F.; Lopera, J.M., "1D/2D transformer electric model for simulation in power converters", 26th Annual IEEE Power Electronics Specialists Conference (PESC '95), vol.2, pp.1043,1049 vol.2, 18-22 Jun 1995.

[16] Gunewardena, T.R., "Manufacturing design considerations for planar magnetics", Electrical Insulation and Electrical Manufacturing & Coil Winding Conference Proceedings, 1997,pp.309,311, 22-25 Sep 1997.

Appendix K

Isolated Full Bridge Boost DC-DC Converter Designed for Bidirectional Operation of Fuel Cells/Electrolyzer Cells in Grid-Tie Applications

15th *European Conference on Power Electronics and Applications (EPE 2013)*

Isolated Full Bridge Boost DC-DC Converter Designed for Bidirectional Operation of Fuel Cells/Electrolyzer Cells in Grid-Tie Applications

Riccardo Pittini, Zhe Zhang, Michael A.E. Andersen
Technical University of Denmark
Department of Electrical Engineering
Kgs. Lyngby, Denmark
Tel.: +45 45 25 36 06
Fax: +45 45 88 01 17
E-Mail: ripit@elektro.dtu.dk
URL: http://www.elektro.dtu.dk/

Keywords

Isolated Full Bridge Boost Converter (IFBBC), Loss Analysis, Fuel and Electrolyzer Cell, Power Semiconductors, Energy Storage.

Abstract

Energy production from renewable energy sources is continuously varying, for this reason energy storage is becoming more and more important as the percentage of green energy increases. Newly developed fuel cells can operate in reverse mode as electrolyzer cells; therefore, they are becoming an attractive technology for energy storage grid-tie applications. In this application dc-dc converter optimization is very challenging due to the large voltage range that the converter is expected to operate. Moreover, the fuel-electrolyzer cell side of the converter is characterized by low voltage and high current. Dc-dc converter efficiency plays a fundamental role in the overall system efficiency since processed energy is always flowing through the converter; for this reason, loss analysis and optimization are a key component of the converter design.
The paper presents an isolated full bridge boost dc-dc converter (IFBBC) designed for this new application focusing on losses analysis. The system topology is briefly discussed and the major concerns related to the system, cells stacks and converter operating points are analyzed. The dc-dc converter losses are modeled and presented in detail; the analysis is validated on adc-dc converter prototype rated at 6 kW 30-80 V 0-80 A on the low voltage side and 700-800 V on the high voltage side (for a grid-tie application). The prototype is based on fully planar magnetic, Si MOSFETs, Si IGBTs and SiC diodes; efficiencies up to ~96.5% and ~97.8% were demonstrated depending on the converter operating point.

Introduction

The energy production from renewable energy sources, such as wind, solar and tidal energy, is strongly fluctuating daily and seasonally, this is due to the nature of these energy sources. During high energy demand peaks or during low energy production from renewable energy sources it is necessary to relay on other more predictable energy sources. Vice versa, when the energy demand is low or there is an energy surplus from renewable sources it is desirable to store this energy. For this reason, smart grids and energy storage started to play an important role in today's energy market and energy policies.
Fuel cell technology was initially discovered in the late 19th century, and still nowadays is considered one of the most promising sources for distributed energy. Fuel cells are an attractive solution for distributed high-power density clean energy generation however, in order to have a bidirectional system they are often combined with electrolyzer cells [1]. In fact, conventional fuel cells cannot operate in reverse mode (with reversed current direction [2]) without incurring in low-efficiency and complex system design. Recent developments in fuel cell /electrolyzer cell technology, especially in Solid Oxide Fuel Cells (SOFC) and Solid Oxide Electrolyzer Cells (SOEC), have enabled these cells to operate in both modes with high efficiency. These cells could represent an attractive solution for the

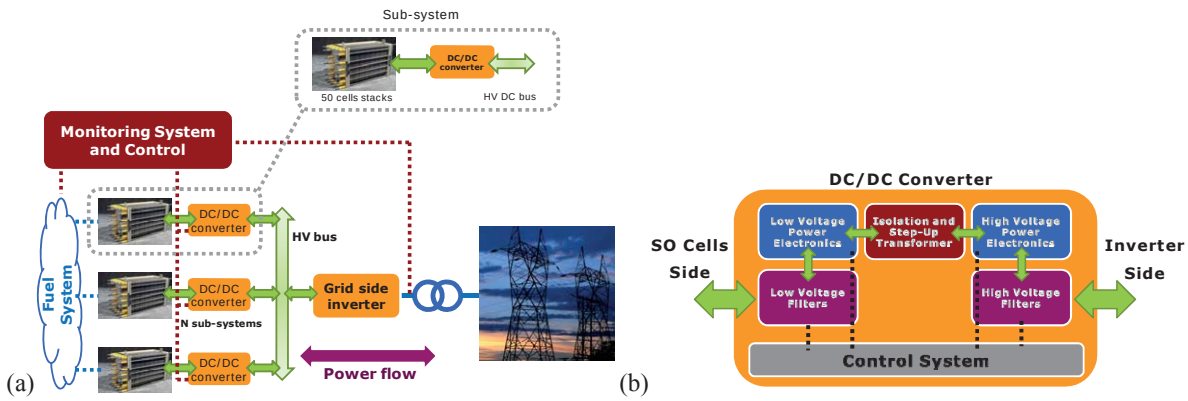


Fig. 1. System overview for fuel cell/electrolyzercell operation (a) and DC-DC converter structure (b).

next generation of smart grids since they can be used both as energy source and as energy storage depending on the market demands.

Realizing high power stacks of SOFC/SOEC represents a big challenge in terms of fuel /gas-pressure equalization within the cells, reliability and long term degradation. Therefore, in most cases fuel or electrolyzer cells are stacked in a limited number, which result in low voltages and high currents. For this reason a power conditioning system is required to adapt the voltage and current levels of the cells stack to a grid interface. DC-DC converters are used for power conditioning in several applications such as solar inverters, uninterruptible power supplies (UPS) and battery systems [3]; they represent the ideal interface for matching the SOFC/SOEC V-I characteristic to the grid interface.

This paper presents a complete loss analysis of an isolated boost DC-DC converter (IFBBC), suitable for bidirectional operation of SO cells. The analysis is verified on a 6 kW prototype with peak efficiency up to ~96.5 % and 97.8% depending on the converter operating mode. Results are discussed and analyzed in relation to the specified application.

System Specification and Converter Topology

The system topology strongly depends on the technology level reached by the SO cells; this defines the number of cells that can be stacked and, therefore, the low voltage interface of the DC-DC converter. As the number of stacked cells increases, cells reliability decreases and degradation increases due to different cell characteristics and unbalances in the fuel system. After a close discussion with SO-cells manufacturer and based on the state of the art a cells stack of 50 cells was considered as the most suitable for this application. With these specifications it was possible to define the DC-DC converter specifications as presented in Table I. The system can be scaled to various power levels by paralleling different SO cells stack and DC-DC converters as presented in Fig. 1a. Each DC-DC converter, Fig. 1b, allows operating each stack at its optimal point independently from the other stacks.

A simple bidirectional non-isolated boost converter could be sufficient however, for high step-up ratios its design becomes challenging making difficult to achieve high converter efficiency for wide operating voltage and power range. Moreover, another drawback of this topology is the lack of galvanic isolation: electric isolation from the fuel cell to the other part of the system is often desired in order to protect the cells stack especially when high voltages are present in the system. For this reason, isolated boost full bridge dc-dc converter represents a good candidate for this application (Fig. 2). It is capable of providing electric isolation with a small high frequency transformer moreover, the transformer provides voltage scaling allowing achieving high efficiency also with large step-up ratios. This topology when properly optimized can achieve very high efficiency and it proved to have the top-efficiency performance for these applications [4]. Most of the boost derived topologies suffer of start-up problems [5], this occurs whenever the output voltage is lower than the input voltage. In this application, the start-up is not critical since the DC-link voltage range is guaranteed by the grid-tie inverter and SO cells have a slow ramp-up time compared to the converter time constants which allow a soft start of the converter.

TABLE I
SOFC AND SOEC SPECIFICATIONS FOR DC-DC CONVERTER DESIGN

	SOFC	SOEC	
Low Voltage (LV) side	30-50	50-80	[V]
Current (LV) side	40-0	0-80	[A]
High Voltage (HV) side	700-800	700-800	[V]
Power Rating	~1500	~6000	[W]

Isolated Full Bridge Boost DC-DC Converter Design and Loss Analysis

The design and optimization of the converter should consider the different operating modes of the system. One of the main concerns related to energy storage is the profitability of the system; this has to be taken into account as weighting factors in the converter design and optimization. Supposing an electric energy conversion efficiency of 90% for both power flow directions, an electricity price of 35 €/MWh during periods of large availability from renewable energies and 50 €/MWh during high electricity demand [6]; with these values is possible to calculate the economic loss due to the convert efficiency:

- SOFC mode (energy production) ➔loss 5 €/MWh
- SOEC mode (energy storage) ➔loss 3.5 €/MWh

In both operation modes the energy conversion efficiency would cause a significant economic loss however, in SOFC mode low converter efficiency would cause more economical losses than in SOEC mode. For this reason it is preferable to have higher efficiency in SOFC mode than SOEC mode. Converter losses can be minimized for one operating point however, the converter has still to be capable of operating in the entire voltage range (30-80 V).
In the following sub-section an analysis of the converter losses when the converter is operating. This analysis is performed on a 6 kWdc-dc converter prototype designed for a maximum input current of ~80 A and capable of operating in the whole 30-80 V range. The converter high voltage side is rated at 700-800 V and it is suitable for a 400 $V_{AC,rms}$grid-tie inverter.

DC-DC Converter Loss Categorization

In order to perform a suitable converter design where the losses are minimized; it is essential to identify all the major loss sources, create models and verify the achieved results. When the major sources of losses are identified it is possible to tune the converter design in order to achieve high efficiency and minimize the losses. In order to obtain accurate models design-measurement loop iterations are required. These are time and cost demanding therefore, it is often desired to minimize these iterations. In this paper, the approach that has been used tried to gather as many information as possible from datasheet and minimize the number of measurements. In a second step the losses are evaluated for different converter operating points and the calculated converter efficiency is compared with the measured one.

Transformer Losses

The transformer is a key component to achieve high efficiency in an IFBBC. The low voltage side of the converter is characterized by high current therefore, particular care should be taken to minimize the winding losses. Moreover, the transformer leakage inductance acts as common source inductance in the selected topology limiting the current commutation time at MOSFET's turn-off and also the

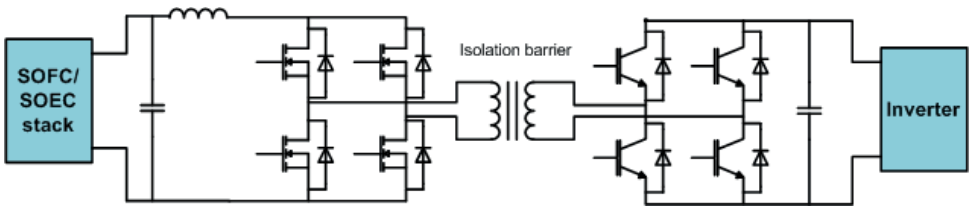


Fig. 2: Bidirectional isolated boost DC-DC converter.

converter efficiency. An interleaved winding structure for minimizing both winding losses (ac-resistance) and leakage inductance was selected for the transformer; the selected interleaved structure is P-S-P-S-P. The main drawbacks of introducing an interleaved structure are that the transformer P-S stray capacitance increases that the manufacturing process of the transformer is more complex. Large transformer stray capacitance is usually unwanted since it increases the common mode noise. However, for the intended application EMC requirements are not included and the EMC filter is not part of the study.

The transformer is designed based on planar cores (E64), two cores are stacked "in series" on in order to increase the overall core cross section and minimize the number of transformer primary turns (low voltage high current winding). The overall transformer design is performed for a switching frequency of 40 kHz minimizing the losses (1) around this switching frequency. Core losses are computed with the generalized Steinmetz equation (2)[7] and the winding losses are calculated based on Dowel's equation that takes into account skin and proximity effects (3)[8][9]. The transformer characteristics are summarized in Table II.

TABLE II
TRANSFORMER CHARACTERISTICS

Turns ratio	8
Primary	3 turns
Core	2*E64 pairs
Core material	Magnetics R
Structure	P-S-P-S-P
Primary winding (P)	PCB 2*400 µm
Secondary winding (S)	30*0.2 mm litz wire
Insulation P-S	2*0.1 mm Kapton

For the 6 kW prototype the design procedure resulted in 3 primary turns and 24 secondary turns on a two series E64 R-material planar transformer cores (for a frequency range around 40 kHz, K=0.074, α=1.43 and β=2.85, with B in kG and f in kHz, result in mW/cm^3). The primary transformer turns are realized with two parallel layers of 400 µm copper (custom thick copper PCB) insulated from each other by 500 µm layer of FR4. The 24 secondary turns are created with litz wires (30 strands of 200 µm diameter) interleaved with the primary winding in a P-S-P-S-P structure. Insulation between primary and secondary is created with two layers of Kapton tape (100 µm each layer). Very thick copper PCB windings (primary) were selected in order to achieve high filling factor in the transformer (in this case ~32%) which is normally not achievable with conventional PCBs. For modeling the transformer losses, the transformer windings resistance was reflected to the primary. A transformer short circuit measurement identified $R_{ac,pri\ eq.} = 5.6\ m\Omega$ and $L_{leak,pri\ eq.} = 82\ nH$ at the switching frequency.

$$P_{tr.} = P_{core} + P_{wind.} \quad (1)$$
$$P_{core} = K \cdot f^{\alpha} \cdot B^{\beta} \quad (2)$$
$$P_{wind.} = R_{ac,pri\ eq.} \cdot I_{pri,rms}^2 \quad (3)$$

Low Voltage Side: Conduction and Switching Losses

The maximum stress over the power semiconductors of the low voltage side of the converter is defined by the converter high voltage side (700-800 V) reflected to the low voltage side (87.5-100 V). At this voltage levels MOSFETs are the most suitable devices. The MOSFETs rating should be just above the maximum voltage stress plus a margin factor. MOSFETs are available rated at 120 V and 150 V, however, due to the low voltage high current the 120 V (lower $R_{DS,on}$) were preferred over the 150 V. Another advantage of the low $R_{DS,on}$1 120 V MOSFETs is that they are available in TO-220 package which has a lower stray inductance than the TO-247 package (used for low $R_{DS,on}$ 150 V devices). In order to decrease the conduction losses two MOSFETs are paralleled, each MOSFET has its independent gate resistor (2.5 Ω) and they are driven by a common driver with a 9 A capability. The selected MOSFETs are Infineon 120 V 4.1 mΩ TO-220. Since they converter does not have an active clamp, the devices may observe avalanche during switching; the selected power semiconductors have avalanche capability of 900 mJ for a single pulse and for repetitive pulses is thermally limited.

The primary low-voltage power semiconductor losses (4) are classified into: conduction ($P_{cond.}$), turn-on ($P_{turn-on}$) and turn-off ($P_{turn-off}$) losses. Conduction losses are simply calculated based on the MOSFETs RMS current($I_{pri\ SW,rms}(D)$) dependent on the duty cycle(5). Turn-on losses are limited to the discharge of the MOSFET's output capacitance ($C_{oss,V_{DS}}$)(6) since the current commutation is delayed by the common source inductance [10][11]. The MOSFET's turn-off losses are due to the limited current commutation speed due to the common source stray inductance which also includes the transformer leakage inductance (in series during in the commutation path). The MOSFETs body diode (10) conducts only when the converter power flow is from the high voltage to the low voltage side. In this case we have both conduction losses (11) and reverse recovery losses (12); dead time is applied to both rise and fall edges (factor two in (11)) and the current flowing through the device is the dc-current plus the ac-current component (first dead time interval) and the dc-current minus the ac-current (second dead time interval). The equivalent conduction losses of the body diode can be approximated with the average dc-current (11).

$$P_{MOS\ LV} = P_{cond.} + P_{turn-on} + P_{turn-off} \tag{4}$$
$$P_{cond.} = R_{DS,on}(T) \cdot I^2_{pri\ SW,rms}(D) \tag{5}$$
$$P_{turn-on} = \frac{1}{2} \cdot C_{oss,V_{DS}} \cdot \left(\frac{V_{HV}}{n_{tr}}\right)^2 \cdot f_{sw} \tag{6}$$
$$dt_{L\ leak} = (L_{leak\ tr.} + L_{leak\ LV\ switch}) \cdot (I_{DC,LV} + I_{AC,peak\ LV}) \cdot \frac{n_{tr}}{V_{HV}} \tag{7}$$
$$P_{turn-off} = \frac{1}{2} \cdot \frac{V_{HV}}{n_{tr}} \cdot \frac{I_{DC,LV} + I_{AC,LV\ peak}}{2} \cdot dt_{L\ leakage} \cdot f_{sw} \tag{8}$$
$$= \left(\frac{I_{DC,LV} + I_{AC,LV\ peak}}{2}\right)^2 \cdot (L_{leak\ tr.} + L_{leak\ TO-220}) \cdot f_{sw} \tag{9}$$
$$P_{bd.MOS} = P_{cond.bd.MOS} + P_{rev.rec.} \tag{10}$$
$$P_{cond.bd.MOS} = V_{fwd.bd.MOS} \cdot I_{DC} \cdot 2 \cdot t_{dead\ time} \cdot f_{sw} \tag{11}$$
$$P_{rev.rec.} = \frac{1}{2} \cdot Q_{rr} \cdot \frac{V_{HV}}{n_{tr}} \cdot \frac{I_{DC}}{I_{rr,ref}} \cdot f_{sw} \tag{12}$$

High Voltage Side: Conduction and Switching Losses

The converter high voltage side uses 1200 V 3rd generation Trench IGBTs from Infineon (IGW15N120H3) and SiC Schottky diodes (Cree C4D15120A) in antiparallel to the IGBTs. The IGBTs conduction and switching losses are introduced in the model based on datasheet values. The IGBTs conduction losses ($P_{fwd,IGBT}$) are calculated based on the IGBTs forward characteristic (datasheet); linearized to a threshold voltage (V_{ce}) and an on state resistance ($R_{on,IGBT}$) as shown in (14). The IGBTs switching losses are initially extracted from datasheet and then corrected based on a reference measurement in order to have higher accuracy in the calculation. From datasheet it is possible to scale the IGBTs losses for different temperatures, different gate resistors and different device switching voltage. This type of scaling is often linear and commonly used for simple loss modeling [12].In this case, the IGBT datasheet values also included the reverse recovery losses of the antiparallel diode which for the designed converter is a SiC diode. For this reason, the IGBT switching losses were scaled based on a reference measurement at 15 A 700 V [13]with a linear coefficient $K_{SW\ on,ref}$aand $K_{SW\ off,ref}$ (15).
In SOFC mode the current flows through the full bridge created with SiC Schottky diodes (IGBTs they do not have free-wheeling diodes and in this mode they do not contribute to the losses). The diodes losses (16) due to the forward voltage drop and due to the diodes resistance are included in $P_{fwd,diodes\ HV}$ (17). SiC Schottky diode are often claimed to have zero-recovery charge ($Q_{rr,HV\ diode}$) compared to conventional silicon diodes however, they also give a small contribute to the high voltage side losses due to the energy stored in their stray capacitance ($P_{HVdiod.rev.rec.}$) (18).

$$P_{IGBT} = P_{fwd,IGBT} + P_{sw,IGBT} \tag{13}$$
$$P_{fwd,IGBT} = V_{ce} \cdot I_{avg} + R_{on,IGBT} \cdot I^2_{HV\ SW,rms} \tag{14}$$
$$P_{sw,IGBT} = E_{on,IGBT}\left(I_{IGBT,turn-on}\right) \cdot K_{SW\ on,ref} \cdot f_{sw} + E_{off,IGBT}\left(I_{IGBT,turn-off}\right) \cdot K_{SW\ off,ref} \cdot f_{sw} \tag{15}$$
$$P_{diodes\ HV} = P_{fwd,diodes\ HV} + P_{HVdiod.rev.rec.} \tag{16}$$

$$P_{fwd,diodes\ HV} = V_{fwd}(T) \cdot I_{avg} + R_{on,IGBT} \cdot I^2_{diode\ HV\ SW,rms} \quad (17)$$
$$P_{HVdiod.rev.rec.} = \frac{1}{2} \cdot Q_{rr,HV\ diode} \cdot V_{HV} \cdot f_{sw} \quad (18)$$

Boost Inductor Losses

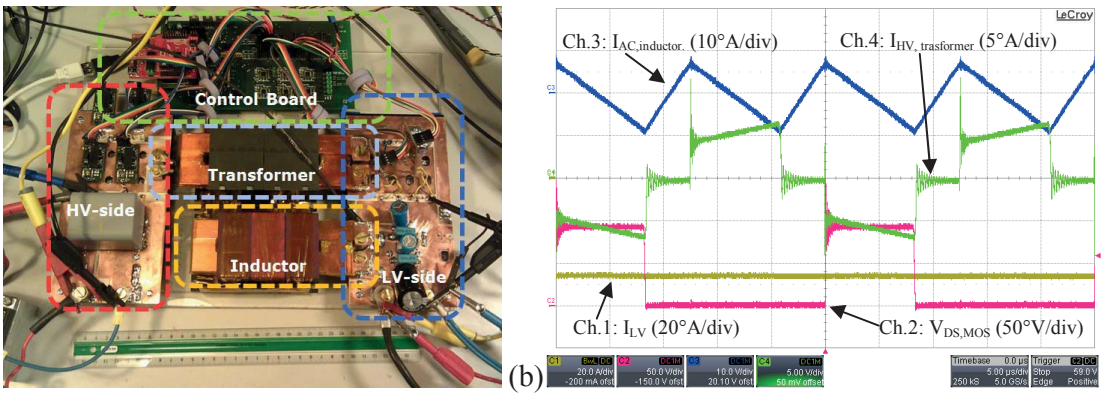
The boost inductor has to carry all the input current for this reason it is important to analyze and try to minimize the losses in this component. The losses in the boost inductor (19) are due to dc-resistance ($P_{DC,wind.}$), ac-resistance [9]($P_{AC,wind.}$) and core losses(P_{core}). The inductor winding losses are computed based on the dc-resistance ($R_{DC,ind}$) and the dc inductor current ($I_{LV,DC}$) (20). The resistance is easily calculated based on the copper cross section and the total length of the inductor windings. The ac-current ripple ($I_{LV,AC\ rms}$) strongly influences the converter efficiency especially at low power levels therefore, it has to be taken into account (21).According to Dowels [8], in a conventional inductor with concentric windings the ac-resistance rapidly increases due to proximity effect. In this design planar (PCB) windings are used, windings are not concentric anymore and the ac-winding resistance can be approximated based on the conductor thickness (h_{Cu}) times the dc-resistance (22). Inductor core losses strongly depend on the core material: high frequency materials such as gapped 3F3 cores provide low core losses however, they significantly increase the winding losses due to fringing flux in proximity of the gap. In this case the inductor was designed based on planar Kool Mu cores. This material has a distributed gap and it does not generate losses in the windings due to fringing flux. The main drawback of this material is its higher hysteresis core losses. The designed inductor has three planar Kool Mu E6030 cores pairs, two pairs in 90µ material and one pair with 26µ material. The cores are arranged in "series" in order to increase the overall core cross section. The winding structure is based on thick copper PCB windings (400 µm copper thickness); the inductor has five turns and each of them is realized by two parallel layers of 400 µm copper track. Core losses have been calculated from Steinmetz equation based on the coefficients for Kool Mu material (Kool Mu 26µ K=120, α=1.46, β=2.09 and Kool Mu 90µ K=193, α=1.26, β=2.01 with f_{sw} in kHz and flux density in T) according to (2).

$$P_{boost\ ind.} = P_{DC,wind.} + P_{AC,wind.} + P_{core} \quad (19)$$
$$P_{DC,wind.} = R_{DC,ind} \cdot I^2_{LV,DC} \quad (20)$$
$$P_{AC,wind.} = R_{AC,ind} \cdot I^2_{LV,AC\ rms} \quad (21)$$
$$R_{AC,ind} = \frac{h_{Cu}}{\delta} \cdot R_{DC,ind} \quad (22)$$

Control and Driver Losses

Control and driver losses have to be included in the loss analysis (23). Gate driver losses are easily calculated from the input capacitance (both for MOSFETs and IGBTs gate drivers (24)). This approximation simply considers the power required for driving the devices and not the overall power required by the gate driver (other circuitry on the gate driver). Moreover, the overall control power (P_{ctrl}) is difficult to calculate since it also depends on the power used by the DSP board with depends on the control loop and DSP features that are used (P_{DSP}) (25). In addition, cooling fans are used on the converter heatsinks (on the bottom of Fig. 3a), these fans have a power consumption of 3.8 W (P_{fans}). At low power level they have a strong impact on the converter efficiency, and therefore, to increase the overall efficiency, temperature control is desired.

$$P_{ctrl} = P_{gate-drivers} + P_{DSP-control\ -card} \quad (23)$$
$$P_{gate-drivers} = (Q_{g,tot,MOS} \cdot V_{g,MOS} + Q_{g,tot,IGBT} \cdot V_{g,IGBT}) \cdot f_{sw} \quad (24)$$
$$P_{DSP-control\ -card} = P_{DSP} + P_{fans} \quad (25)$$



(a) (b)

Fig. 3: 6 kW prototype of isolated boost converter (a) and switching waveforms at 60 V 40 A. Ch.1(yellow): I_{LV} (20 A/div), Ch.2(red): $V_{DS,MOS}$ (50 V/div), Ch.3(blue): $I_{AC,inductor}$ (10 A/div) and Ch.4(green): $I_{HV,\ transformer}$ (5 A/div).

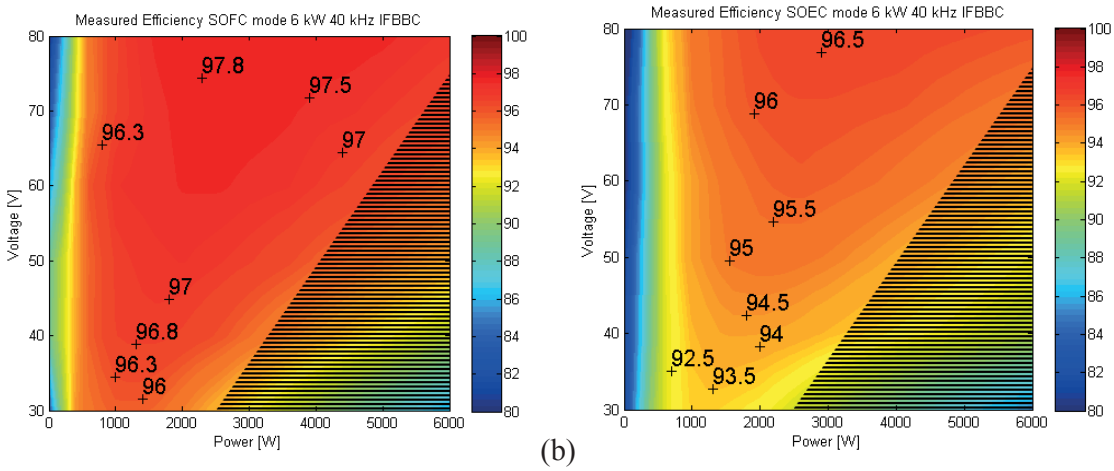
Overall Converter Losses

The converter efficiency depends on the power flow direction; in fact in one operating mode the converter is operating as a boost converter (power flow from the low voltage to the high voltage side, SOFC mode), while with the opposite power flow the converter acts as a buck (SOEC mode). In SOFC mode the body diode of the low voltage side MOSFETs will never conduct and therefore, it will not have a contribution to the converter losses. In this operating mode, the current in the high voltage side bridge will flow uniquely through the SiC Schottky diodes and IGBTs will not contribute to the losses since they are bipolar devices and they cannot be used for active rectification. Similarly, in SOEC mode the diodes in the high voltage bridge are not used and, therefore, only the diode capacitance will contribute to the losses (no conduction losses). Moreover, the MOSFETs will have very low switching losses since during turn-off the MOSFETs body diode will start carrying the current and will maintain a low-voltage across the MOSFET (close to soft switching).
The other components of the losses remain unchanged and they do not depend on the converter operating mode. This results that the total converter losses for the two operating modes are given by:

$$P_{SOFC} = P_{tr} + P_{MOS\ LV} + P_{diodes\ HV} + P_{boost\ ind.} + P_{ctrl} \tag{25}$$
$$P_{SOEC} = P_{tr} + P_{bd.MOS} + P_{cond.MOS} + P_{IGBT\ HV} + P_{HVdiod.rev.rec} + P_{boost\ ind.} + P_{ctrl} \tag{26}$$

Experimental Results and Analysis

Experimental results are based on a developed 6 kW prototype (Fig. 3a and Fig. 3b). The goal of the prototype was to verify the expected performance of the converter and identify the main source for losses with experimental verification.
The converter was operated in SOFC and SOEC mode and its efficiency measured with a precision power analyzer (N4L PPA5530) using 1 mOhm 100 A current shunts for the entire 30-80 V range at different power levels. Measured efficiencies are presented on Fig. 4a and Fig. 4b for both power flow direction (SOFC = boost mode, SOEC = buck mode). At low voltage levels the power on the developed prototype is limited by its maximum current (80 A_{RMS}). Efficiency measurements were exported and interpolated with MATLAB to obtain a smoother plot. The darkened area on Fig. 4a and Fig. 4b indicates a prohibited operating point for the converter (current overload). In this darkened area(current overload)the efficiency was extracted based on a fit of the measured values in the normal converter operating range (30-80 V and 0-80 A).At the lowest input voltage (30 V) efficiency is limited by the high current flowing in the converter that give significant contribute in the conduction and switching losses. In this case the efficiency is limited to 95.9% in SOFC and 93.3% in SOEC mode. At the highest input voltage (80 V) the converter efficiency reaches a peak of 97.8% in SOFC and 96.5% in SOEC. It is observed that the efficiency is SOEC is always lower than in SOFC. In SOFC the MOSFETs are hard switching and the IGBTs do not give contribution to the losses, while in SOEC the IGBTs are giving large contribute to the losses (both switching and conduction losses) and the MOSFETs are used for active rectification (close soft switching).



(a) (b)

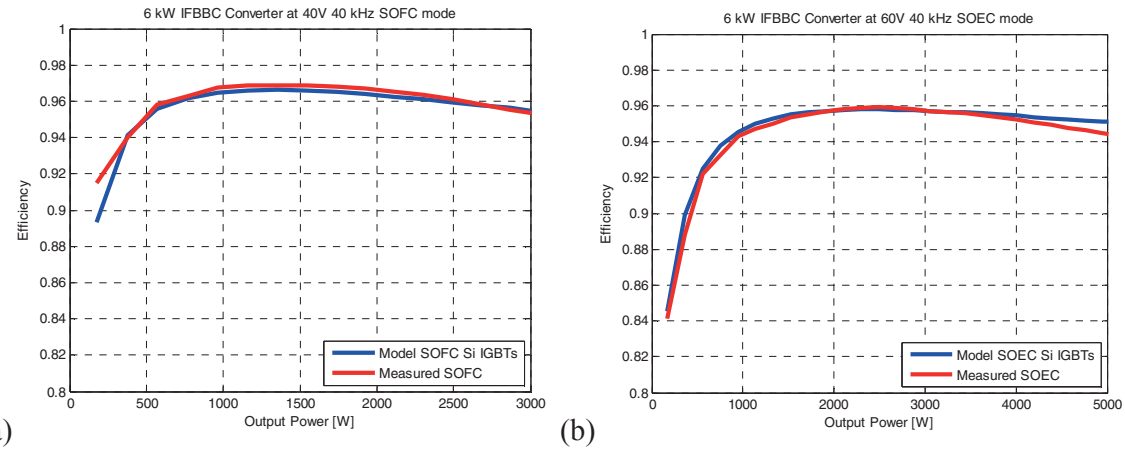
Fig. 4: Measured efficiency of the 6 kW IFBBC prototype at different voltage and different power levels, SOFC mode (a) and SOEC mode (b). Darkened area indicates that the converter is not allowed to operate in these conditions due to over current on the low voltage side (80 A current limitation).

Measured vs. Modeled Efficiency

The operating point of the dc-dc converter is defined by the SOFC /SOEC cells stack. In SOFC mode the voltage of the cells stack decreases as the power increases, vice versa in SOEC mode. The modeled converter efficiency is compared with the measured one. Two characteristic curves are presented: one at 40 V for SOFC mode (Fig. 5a) and one at 60 V for SOEC mode (Fig. 5b).Based on the presented loss model of the IFBBC a small difference is observed. It should be considered that the presented model assumed constant device temperature for power semiconductors, magnetic components and for copper. This assumption introduces an error since the converter component temperatures will vary continuously depending on the voltage and power flow through the converter. It is interesting to observe that the peak efficiency at 40 V and SOFC mode is ~96.8% at 1-1.5 kW(Fig. 5a); at 60 V in SOEC the peak efficiency is observed at 2-3 kW and it is ~95.9% (Fig. 5b).

Components of the Converter Losses

In proximity of the peak efficiency at 40 V in SOFC and 60 VSOEC, the different sources of losses in the converter are presented based on the modeled values (Fig. 6). It is observed that in SOFC mode at 1 kW and 40 V (Fig. 6a) the main source of losses is the boost inductor. At this power level the main



(a) (b)

Fig. 5: Comparison of measured versus calculated efficiency of the 6 kW IFBBC based on the presented models. Efficiency comparison at 40 V (a) SOFC mode (power flow from the low voltage side to the high voltage side) and 60 V (b) SOEC mode (power flow from the high voltage side to the low voltage side). 80 A current limitation.

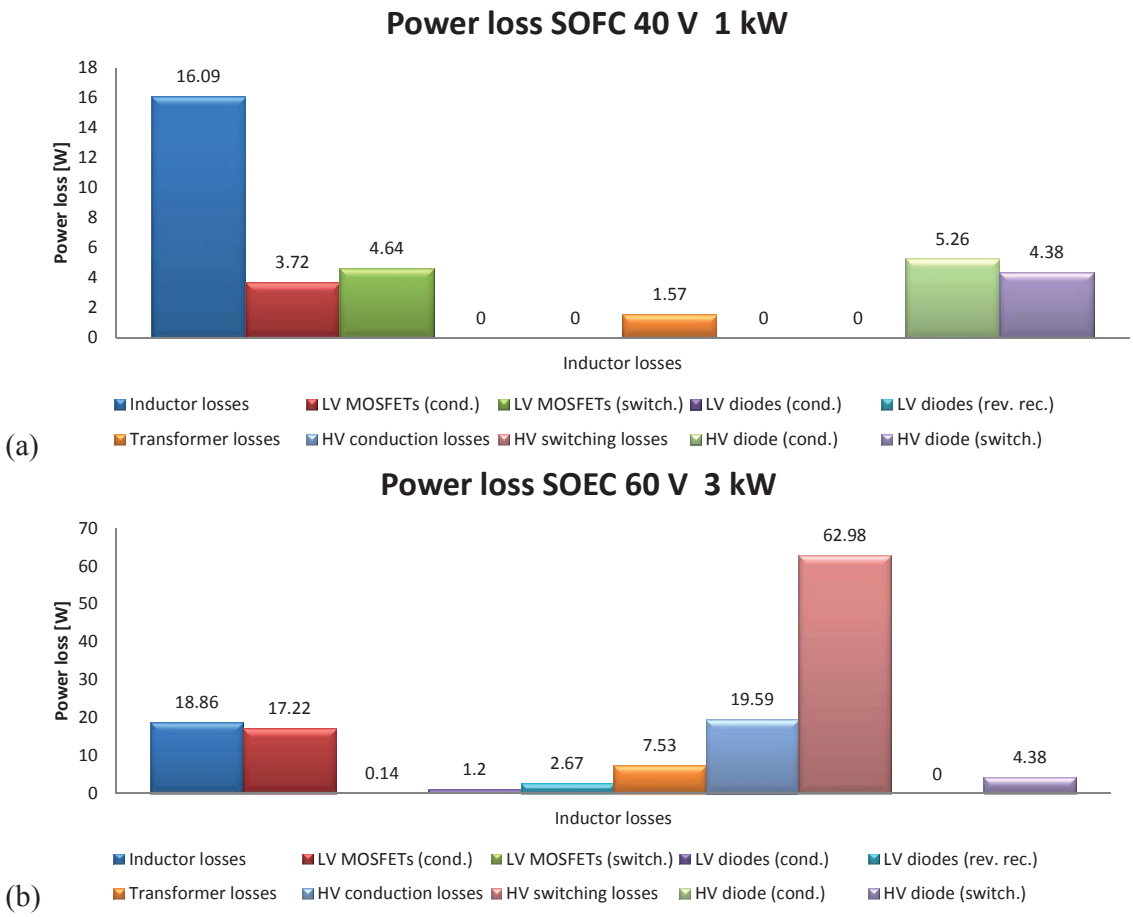


Fig. 6: Calculated loss components of the 6 kW IFBBC prototype at 40 V 1 kW in SOFC mode (a) and at 60 V 3 kW in SOEC mode (b). Based on the developed loss model.

inductor losses are due to the core losses; in fact even though the ripple current is limited, ac inductor flux produces significant losses (Kool Mu material has larger losses than traditional ferrites). As the power increase (e.g. 1.5 kW 40 V) the inductors losses have a minimal increase mostly due to winding losses. However, the losses in the other components significantly increase especially the ones in the power semiconductors. MOSFET's turn-off commutation time increases due to the large current to be commuted. Then above 1.5-2 kW (Fig. 5a) the efficiency starts decreasing due to the significant increase of the conduction losses at large current.

The loss components at 60 V 3 kW (Fig. 6b) in SOEC mode significantly change. The MOSFET's main loss contribution is given by the conduction losses (active rectification). The MOSFET's body diode conducts only for a short time (dead time) and their total contribution (conduction and reverse recovery) is minimal compared to other losses. The main sources of loss are the high voltage power semiconductors (IGBTs in hard switching condition); dominant are the switching losses which account up to ~45% of the total losses at this operating point, Fig. 6b.

On overall, it is observed that even with a limited variation of the voltage on the converter low voltage side (from 40 V up to 60 V) compared to the overall operating voltage range the distribution of the converter losses varies significantly. It is observed that the lowest efficiency in SOEC operating mode is due to the large losses generated by the IGBTs on the converter high voltage side. This operation mode would significantly benefit by the introduction of SiC devices which would increase the converter efficiency. Vice versa, in SOFC mode there is a significant component of the losses that is given by the boost inductor (mostly core losses). The inductor could be designed based on a gapped ferrite core which would significantly reduce the core losses but, would increase the inductor winding losses due to fringing flux in the core air gap.

Conclusions

The paper presented a new challenging application for bidirectional isolated boost DC-DC converters boost with wide low-voltage input and high-current. The developed converter is based on fully planar magnetic and has peak efficiency of 97.8% and 96% depending on the converter operating mode. The design procedure has taken into account the operating mode (SOFC/SOEC) of the cells stacks and a loss analysis for the converter prototype was presented. The presented loss models were evaluated based on a 6 kW converter prototype; measured and modeled efficiency had a good match validating the models. The converter losses were analyzed for two different operating points (40 V 1 kW and 60 V 3 kW) which are determined by the SOFC/SOEC stack characteristics.
The design highlighted how the two different converter operating modes (SOFC and SOEC) have significant variation in the distribution of the losses in the converter. Latest Trench IGBTs proved to be suitable for designing high efficiency converters achieving peak efficiency up to 96 %.However, it was observed the IGBT losses were still a large loss component and they are the main cause of the lower efficiency in SOEC mode compared to the SOFC mode. The introduction of new power semiconductors based on SiC (e.g. SiC JFETs or SiC MOSFETs) is required in order to further increase the converter efficiency especially in SOEC operating mode.

References

[1] P. Iora, M.A.A. Taher, P. Chiesa, N.P. Brandon;“A novel system for the production of pure hydrogen from natural gas based on solid oxide fuel cell–solid oxide electrolyzer”, International Journal of HydrogenEnergy, Volume 35, Issue 22, November 2010, Pages 12680-12687, ISSN 0360-3199.

[2] X. Yu, M.R. Starke, L.M. Tolbert and B. Ozpineci; “Fuel cell power conditioning for electric power applications: a summary” IET Electrc Power Applications, 2007, 1, (5), pp. 643–656.

[3] Zhang, Zhe; Pittini, Riccardo; Andersen, Michael A.E.; Thomsen, Ole C.; “A Review and Design of Power Electronics Converters for Fuel Cell Hybrid System Applications”, Energy Procedia2012, Volume 20, pp. 301-310.

[4] Nymand, M.; Andersen, M.A.E.; "High-Efficiency Isolated Boost DC–DC Converter for High-Power Low-Voltage Fuel-Cell Applications," IEEE Transactions on Industrial Electronics, vol.57, no.2, pp.505-514, Feb. 2010.

[5] Mihalic, F.; Hren, A., "Safe start-up procedures of isolated bi-directional DC-DC converter," 2010 14th International Power Electronics and Motion Control Conference (EPE/PEMC), pp.T2-67,T2-173, 6-8 Sept. 2010.

[6] European Energy Exchange, www.eex.com, December 2012.

[7] Ziwei Ouyang; Thomsen, O.C.; Andersen, M.A.E.; "Optimal Design and Tradeoff Analysis of Planar Transformer in High-Power DC–DC Converters," IEEE Transactions on Industrial Electronics, vol.59, no.7, pp.2800-2810, July 2012.

[8] P. L. Dowell, "Effects of eddy currents in transformer windings," Proceedings of IEEE, vol.113, no.8, August 1966, pp. 1387-1394

[9] Pittini, Riccardo; Zhe Zhang; Ouyang, Ziwei; Andersen, Michael A. E.; Thomsen, Ole C.; "Analysis of planar E+I and ER+I transformers for low-voltage high-current DC/DC converters with focus on winding losses and leakage inductance," 7th International Power Electronics and Motion Control Conference (IPEMC 2012), vol.1, pp.488-493, 2-5 June 2012.

[10] Ziwei Ouyang; Sen, G.; Thomsen, O.C.; Andersen, M. A E, "Analysis and Design of Fully Integrated Planar Magnetics for Primary–Parallel Isolated Boost Converter," IEEE Transactions on Industrial Electronics, vol.60, no.2, pp.494,508, Feb. 2013.

[11] Nymand, M.; Madawala, U.K.; Andersen, M.A.E.; Carsten, B.; Seiersen, O.S.; "Reducing ac-winding losses in high-current high-power inductors", 35th Annual IEEE Conference of Industrial Electronics (IECON 2009), pp.777-781, 3-5 Nov. 2009.

[12] Pittini, R.; D'Arco, S.; Hernes, M.; Petterteig, A.; , "Thermal stress analysis of IGBT modules in VSCs for PMSG in large offshore Wind Energy Conversion Systems," Proceedings of the 2011-14th European Conference on Power Electronics and Applications (EPE 2011), pp.1-10, Aug. 30 2011-Sept. 1 2011.

[13] Pittini, R.; Zhang, Z.; Andersen, M.A.E.; "SiC JFET Cascode Loss Dependency on the MOSFET Output Capacitance and Performance Comparison with Trench IGBTs", Applied Power Electronics Conference and Exposition (APEC 2013), pp.1287-1293, 17-21 March 2013..

Appendix L

Investigation of Heat Sink Efficiency for Electronic Component Cooling Applications

Elektronika IR Elektrotechnika, Vol. 20, No. 1, 2014, p. 49-54

Investigation of Heat Sink Efficiency for Electronic Component Cooling Applications

Z. Staliulionis[1], Z. Zhang[2], R. Pittini[2], M. A. E. Andersen[2], P. Tarvydas[1], A. Noreika[1]
[1]*Department of Electronics Engineering, Kaunas University of Technology, Studentu St. 50, LT-51368 Kaunas, Lithuania*
[2]*Department of Electrical Engineering, Technical University of Denmark, Kgs. Lyngby, DK-2800, Denmark*
alius.noreika@ktu.lt

***Abstract*—Research and optimisation of cooling of electronic components using heat sinks becomes increasingly important in modern industry. Numerical methods with experimental real-world verification are the main tools to evaluate efficiency of heat sinks or heat sink systems. Here the investigation of relatively simple heat sink application is performed using modelling based on finite element method, and also the potential of such analysis was demonstrated by real-world measurements and comparing obtained results. Thermal modelling was accomplished using finite element analysis software COMSOL and thermo-imaging camera was used to measure the thermal field distribution. Ideas for future research involving improvement of the experimental setup and modelling verification are given.**

***Index Terms*—Finite Element Method, heat sinks, temperature measurement.**

I. INTRODUCTION

All components including capacitors, inductors and semiconductor devices which are used in power converters have maximum operating temperatures defined by manufacturer. Increased power density is the main factor which influences the thermal management to become so important. Researchers look for new methods how to increase the systems cooling efficiency and engineers try to optimize the placement of components on PCB which improves cooling possibilities as well. In modern industry, the cooling efficiency of a system is primarily determined by using numerical modelling techniques [1].

There is a wide range of numerical methods used in thermal analysis like boundary element method, finite difference method, and finite element method. Nowadays the finite element method is most widely used to analyse, simulate, optimize and design electronic devices and their systems. Most material properties are temperature-dependent, and this effect introduces multi-physics modelling, for example connecting electrics and heat transfer physics in one area. Finite element analysis software *COMSOL Multiphysics* was selected to perform modelling in our case.

Manuscript received January 28, 2013; accepted April 4, 2013.

II. COMPONENTS USED FOR THE EXPERIMENTS

The heat sink made by company *Wakefield Thermal Solution* was selected (Table I) [2].

TABLE I. SPECIFICATIONS OF THE USED HEAT SINK.

Standard P/N	Dimensions of heat sink, (mm)	Number of fins	Natural convection, Power dissipation [W], 60 ºC rise heat sink to ambient	Forced convection Thermal resistance at 300 ft/min, (ºC/W)
517-95AB	57.9x61x24.1	8	11 W	2 ºC/W

After heat sink selection the transistor and the diode were selected. In this work the heat sink is investigated in environments containing natural and forced convection types. From the specifications of heat sink it is known, that the dissipated power of heat sink is 11 W when the natural convection is used. Also from specifications we know that the thermal resistance is equal to 5.45 ºC/W. As it can be seen from Table I the thermal resistance of the forced convection is equal 2 ºC/W which means that the dissipated power can be 2.72 times larger than under natural convection. So, the theoretical total dissipated power can be achieved around 30 W. When the maximum dissipated power is known, the transistor and the diode can be chosen. In order to investigate the thermal management, it is better to choose the transistor with larger on-resistance value.

TABLE II. SPECIFICATIONS OF THE USED TRANSISTOR AT T_C = 25 ºC.

On-resistance, [Ω]	Maximum continuous drain current, [A]	Operating and storage temperature, ºC	Maximum power dissipation, [W]	Thermal resistance junction to case, ºC/W	Thermal resistance junction to ambient, ºC/W	Max Drain to source voltage, [V]
0.85	8	-55 to 150	125	1	62.5	500

Of course, transistor typically dissipates much more power than the diode. In this case, when the 30 W power is required, the diode power loss almost doesn't influence the total power. Thus, transistor is the predominant power

dissipator and should be selected primarily. Both components were selected to produce the total dissipated power a little larger than 30 W.

The chosen transistor is IRF840 with TO-220 package type, produced by *Fairchild semiconductor* and the main specifications of the transistor regarding to thermal management are presented in Table II [3].

When the transistor is chosen, the diode can be selected. The diode was selected regarding to the maximum current of the transistor. The diode is 10TQ045 with TO-220 package type from *International Rectifier*. The main specifications of the diode regarding thermal management are presented in Table III [4].

TABLE III. SPECIFICATIONS OF THE USED DIODE.

Maximum $I_{F(AV)}$ at 50 % rectangular waveform and T_J=151 ºC, [A]	Maximum forward voltage drop at T_J=125 ºC and 10 A, [V]	Operating and storage temperature, ºC	Thermal resistance junction to case, ºC/W
10	0.49	-55 to 175	2

As it can be seen, the diode dissipated power could be around 2 W in this case. So, it is just few watts comparing with the theoretical total dissipated power.

TABLE IV. SPECIFICATIONS OF THE USED FAN.

Size, [mm]	Voltage rating, [V]	Current, [mA]	Consumed power, [W]	Speed, [RPM]	Air flow, [CFM]	Static pressure, [Inch-H_2O]
50x50x10	5	181	0.9	4300	11	0.11

Eventually, the DC axial flow fan was chosen from *Multicomp*. The main specifications of the fan are given in Table IV [5].

III. EXPERIMENTAL SYSTEM

The experiments and simulations were accomplished using selected transistor, diode, heat sink and fan. Additional thermal interface material (TMI) of type *MK3306-Insulating kit* from *Multicomp* was used between the transistor or diode and the heat sink and was applied to TO-220 components. The TMI is made from mica which has the thermal conductivity equal to 0.71 (W/m*K) and its dimensions are 19mm x 15 mm x 0.1 mm. The transistor and the diode are screwed to the heat sink. For experiments the thermo-imaging camera was used and all experiments were made under steady state condition. Gate to source voltage applied to the transistor is equal to 12 V.

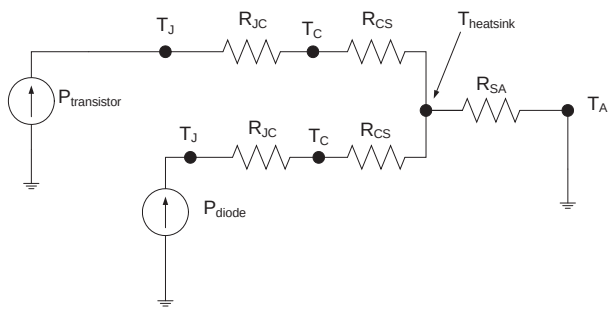


Fig. 1. Thermal circuit of the experimental system.

The thermal circuit of the experimental system is shown in Fig. 1, where T_J – junction temperature [ºC], T_A – ambient temperature [ºC], R_{SA} – heat sink thermal resistance [ºC/W], R_{JC} – thermal resistance of junction to case [ºC/W] which is defined by the manufacturer, R_{CS} – thermal resistance case to heat sink [ºC/W]. R_{CS} resistance is user defined and it is defined by thermal interface material which is used between component and heat sink. This resistance is very small and sometimes is neglected in the calculation. The thermal circuit is shown without resistances values, because it represents only how the resistances of the all system are interconnected. Certainly, values of some resistances are fixed and don't change in the circuit. These resistances are the junction to case and case to heat sink (TMI resistance). The ground of the thermal circuit is chosen equal to the ambient temperature.

Before experiments and simulations in *COMSOL Multiphysics* the flow rate of the fan is estimated (expressed in m/s). The radiation emissivity of the black anodized heat sink is in the range from 0.82 to 0.86 and in the emissivity for experiment setup is chosen equal to 0.85 [6]. These values have to be defined during the modeling. The same 0.85 emissivity is defined in thermo-camera.

Firstly the flow rate it is converted from CFM into m/s. The square-shaped fan has dimensions 50 mm x 50 mm.

Then LFM is estimated and the correction factor is chosen equal to 80 % which is introduced into the equation

$$LFM = \frac{CFM}{A}, \tag{1}$$

where A is fan area.

Value of LFM is recalculated into m/s (1.66 m/s) has to be applied when the forced convection is investigated.

Detailed experimental system modelling algorithm using *COMSOL* is given in [1].

IV. SYSTEM MODEL IN *COMSOL*

Dimensions of components are presented in [2]–[5]. Exact dimensions are used to develop the spatial model in the *COMSOL Multiphysics* [7], [8]. M3 type screw is used. The silicon chip of the transistor and the diode has dimensions 3 mm x 3 mm x 0.3 mm. In Fig. 2 the created spatial model of experimental system is presented with designated materials. The geometry model with generated finite element mesh is shown in Fig. 3. The thermal conductivities of all designated materials in *COMSOL* are given in Table V.

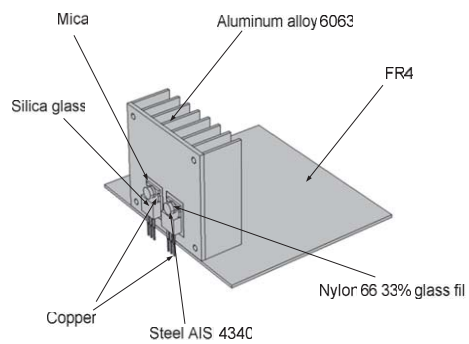


Fig. 2. Geometry model with designated materials.

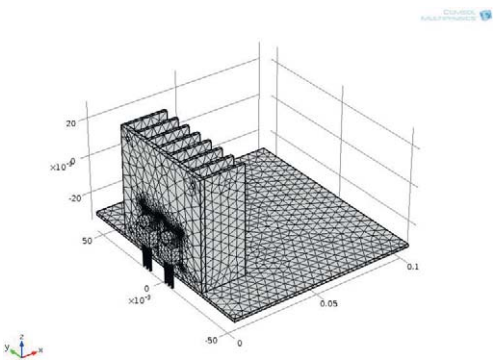


Fig. 3. Model with finite element mesh.

TABLE V. THERMAL CONDUCTIVITY OF EACH MATERIAL.

Material	Thermal conductivity (W/m*K)
Silica glass	1.38
Aluminium alloy 6063	200
Mica	0.71
Copper	400
Steel AISI 4340	54
Silicon	150
Nylon 66 33 % glass fill	0.27
FR4	0.3

Real measurements were taken when the system was placed on top of paper book; during modeling PCB made from FR4 was used as a base. Its conductivity is poor (0.03 W/m*K) and it was assumed that it doesn't influence the thermal distribution. Additional verification of thermal conductivity of different base materials should be made in future investigations.

The estimated convective coefficient is applied for vertical orientation and the radiation is used 0.85 for transistor encapsulation, heat sink, the top of the surface of PCB and bush, because they are main contributors of the radiation. It is assumed that other surfaces don't radiate the power. The average ambient temperature for all simulations cases is applied equal to 27 ºC which is chosen from measurements with the *FLIR T200* thermo-camera. However in each case the boundary conditions can vary dependent on the situation. The variable parameter is the dissipated power of each component chip. In simulations the current is not applied to pins of the transistor and the diode (the total resistance of all pins approaches zero), because silicon chips of both components dissipate relatively a lot of power.

V. MEASUREMENTS UNDER NATURAL CONVECTION

At first measurements were made without fan. The results were measured using thermo-camera and the multimeter *AMPROBE 38XR-A*. The emissivity in thermo-camera was defined equal to 0.85. The voltage drop on the diode and the transistor was measured using multimeter.

All experiments are done when heat sink is placed on the plane as it is shown in Fig. 2. Three distances between the transistor and the diode were used (16.51 mm, 26.00 mm, 33.50 mm). The maximum temperature of the transistor reached close to 123 ºC in all experiments.

At first analysis was performed when one heat sink outflow is covered and the distance between the transistor and the diode is equal to 16.51 mm (first case). The results are presented in Table VI. The heat sink temperature is measured at the centre of the heat sink. The results when the distance between components is equal to 26 mm are given in Table VII, and for distance equal to 33.5 mm are given in Table VIII.

TABLE VI. RESULTS WHEN THE DISTANCE BETWEEN THE TRANSISTOR AND THE DIODE IS EQUAL TO 16.51 MM.

I, [A]	$V_{transistor}$, [V]	V_{diode}, [V]	R_{ON}, [Ω]	$P_{transistor}$, [W]	P_{diode}, [W]	$T_{transistor}$, [ºC]	T_{diode}, [ºC]	$T_{Heatsink}$, [ºC]
0.506	0.341	0.370	0.673	0.172	0.187	34.2	32.3	31.5
1.005	0.705	0.389	0.701	0.708	0.391	36.4	34.7	33.9
1.492	1.156	0.394	0.775	1.725	0.588	46.0	40.8	39.0
2.0	1.791	0.396	0.896	3.582	0.791	61.4	48.5	47.5
2.498	2.910	0.391	1.165	7.269	0.976	86.3	60.8	60.1
2.855	4.327	0.38	1.516	12.354	1.085	123.0	78.0	77.4

TABLE VII. RESULTS WHEN THE DISTANCE BETWEEN THE TRANSISTOR AND THE DIODE IS EQUAL TO 26 MM.

I, [A]	$V_{transistor}$, [V]	V_{diode}, [V]	R_{ON}, [Ω]	$P_{transistor}$, [W]	P_{diode}, [W]	$T_{transistor}$, [ºC]	T_{diode}, [ºC]	$T_{Heatsink}$, [ºC]
0.521	0.349	0.371	0.670	0.182	0.193	33.2	31.9	31.3
1.010	0.7048	0.390	0.698	0.712	0.394	35.1	33.6	32.3
1.498	1.167	0.395	0.779	1.748	0.591	44.9	39.0	37.9
2.012	1.837	0.396	0.913	3.696	0.797	60.4	47.5	46.9
2.504	2.912	0.390	1.193	7.292	0.977	86.2	60.5	60.1
2.814	4.293	0.382	1.526	12.081	1.075	123.0	75.5	77.6

TABLE VIII. RESULTS WHEN THE DISTANCE BETWEEN THE TRANSISTOR AND THE DIODE IS EQUAL TO 33.5 MM.

I, [A]	$V_{transistor}$, [V]	V_{diode}, [V]	R_{ON}, [Ω]	$P_{transistor}$, [W]	P_{diode}, [W]	$T_{transistor}$, [ºC]	T_{diode}, [ºC]	$T_{Heatsink}$, [ºC]
0.510	0.338	0.373	0.663	0.172	0.190	33.9	32.1	30.9
1.005	0.694	0.391	0.690	0.697	0.393	35.8	33.7	32.9
1.492	1.135	0.397	0.761	1.693	0.592	43.4	38.0	37.2
1.990	1.743	0.398	0.876	3.469	0.792	58.3	46.4	45.1
2.501	2.890	0.394	1.156	7.228	0.986	86.2	59.0	59.1
2.833	4.309	0.381	1.521	12.207	1.079	123.0	74.4	77.0

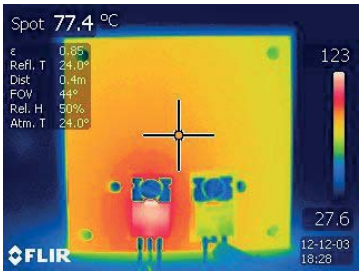


Fig. 4. The temperature distribution when the distance between the transistor and the diode is 16.51 mm, one outflow covered.

Picture of thermal field measured using thermo-camera is shown in Fig. 4. The temperature increase of the diode in respect of the distance between the transistor and the diode is shown in Fig. 5. The dissipated power dependent on distance at 123 ºC transistor temperature is shown in Fig. 6.

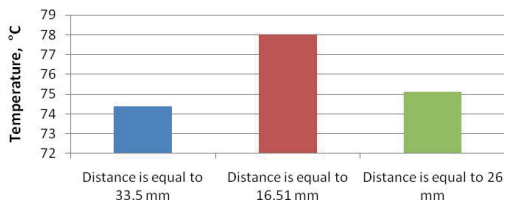


Fig. 5. Temperature of the diode: dependency on distances.

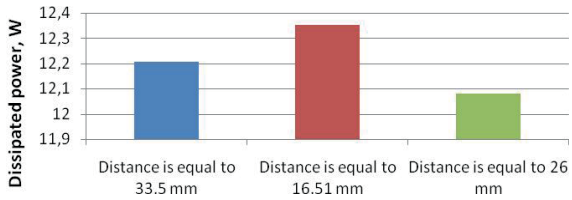


Fig. 6. Dissipated power of the transistor in respect of distances from the diode.

The largest dissipated power can be achieved when the distance between components is 16.51 mm and the transistor is placed almost in the centre of the heat sink.

In simulation the heat conduction, heat convection and the radiation are used. The convection coefficient comprised of limited (between fins) and free convection is applied equal to 4 (W/m2*K). The radiation coefficient is used 0.85 as in experiments case. The dissipated power for diode is applied equal to 1.1 W and for transistor it is chosen to use 12.2 W. These dissipated powers are chosen same for all three distance values for the purpose of comparison of the temperature distribution. The result of simulation when the distance between the transistor and the diode is equal to 26 mm is presented in Fig. 7.

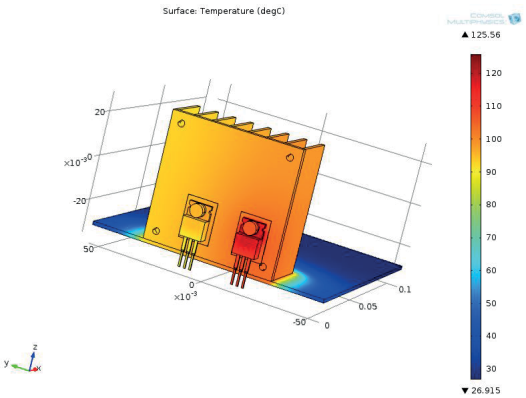


Fig. 7. Temperature distribution when the distance between the transistor and the diode is equal to 26 mm.

It was obtained that when the distance between components was 16.5 mm, the transistor temperature was the lowest (119.03 ºC) from all three simulations. In this case the heat sink can dissipate more power. When the distance was 26 mm, the temperature of the transistor was the highest (125.56 ºC), and this approximately matches real measurements. And when the distance was 33.5 mm, the temperature was equal to 123.39 ºC.

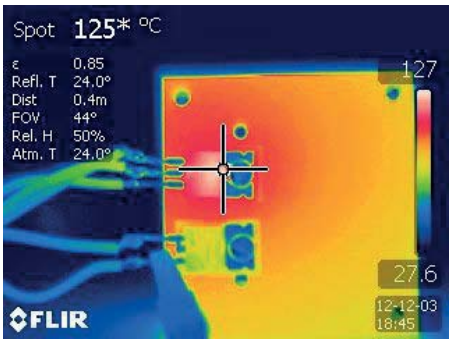


Fig. 8. Measured temperature distribution with both heat sink outflows open.

Also the experiment was made when both heat sink sides were open for airflow (Fig. 8). Firstly the maximum temperature of transistor (123 ºC) was reached and then the orientation of heat sink was changed. Then the temperature increased to 127 ºC and current dropped from 2.855 A to 2.72 A.

VI. Reference Ppoint of the Ttemperature and Real Junction Temperature Evaluation

After experiments under natural convection the reference point measurement was made. This measurement was done to find approximate value of maximum temperature of transistor chip. The temperature was compared with the thermocouple readings. The thermocouple was inserted under the screw on the transistor. The picture of the measurement setup is shown in Fig. 9.

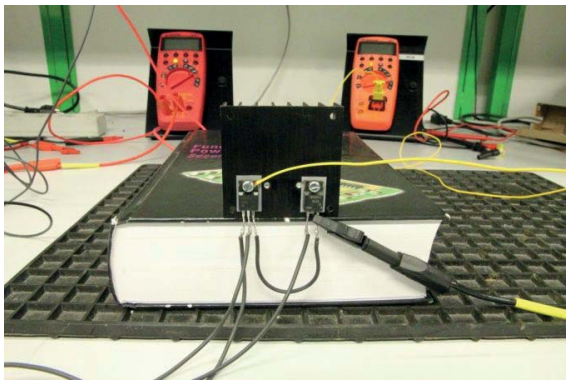


Fig. 9. Measurement of the reference point.

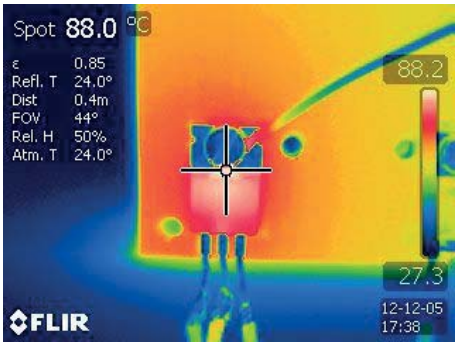


Fig. 10. Measurements when emissivity is ε = 0.85 at the largest distance between components.

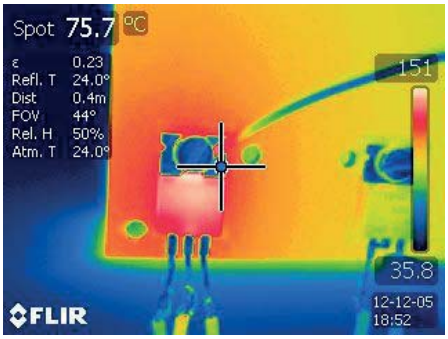


Fig. 11. Measurement of temperature on the transistor case.

The temperature of transistor case was measured when the distance between the transistor and the diode was the largest.

The current of 2.5 A was applied. It is known that the encapsulation of the TO-220 package has emissivity around 0.92 [6]. Thermal images made with the thermo-camera at different emissivity are shown in Fig. 10. The error of temperature measurements due to difference of emissivity (0.85 and 0.92) was checked for ambient temperature and maximum operating temperature of transistor encapsulation and it ranged from 2 ºC to 5 ºC.

From IRF840 transistor datasheet it is known that the junction to case thermal resistance is equal to 1º C/W. The thermocouple mounted on the case of the transistor is very close to the chip and the maximum temperature point of the transistor. It can be assumed that the thermal resistance junction to case is the same (1º C/W) on that point. The temperature measured with thermocouple at that point was 74 ºC. In this case the dissipated power in the transistor was estimated equal to 7 W. When the necessary values are known the junction temperature can be calculated

$$T_J = 7 \cdot 1 + 74 = 81°C. \quad (2)$$

It can be seen from Fig. 11 that the reference temperature measured by thermo-camera very close to thermocouple is around to 75 ºC. The emissivity of the copper was used equal to 0.23.

VII. Measurements Under Forced Convection

Measurements with fan were made when the distance between the transistor and the diode is shortest (16.51 mm), because from earlier results it could be seen that it is the best choice in order to have better thermal distribution.

Three measurement cases were selected: 1) Fan placed on top of heat sink, both sides open for airflow; 2) Fan placed on top, one heat sink air outflow side covered; 3) Fan mounted on the side of heat sink and airflow is parallel to base of heat sink.

At first the fan was attached to the top of the heat sink and for the first case the analysis was made when the heat sink base is perpendicular to airflow with one outflow covered. Firstly the maximum temperature of the transistor was reached around 123 ºC and after that the fan was switched on. At the maximum temperature of the transistor the current reached 2.810 A. When the fan was turned on, the temperature was lowered and transistor current capacity increased until the maximum temperature (123 ºC) was reached again. The same method is used for other cases of investigation. Results are presented in Table IX.

TABLE IX. RESULTS WITH FAN WHEN HEAT SINK BASE IS PERPENDICULAR TO AIRFLOW, ONE OUTFLOW COVERED.

I, [A]	3.279	3.385	3.496
$V_{transistor}$, [V]	4.085	4.646	5.597
V_{diode}, [V]	0.426	0.424	0.422
R_{ON}, [Ω]	1.246	1.373	1.601
$P_{transistor}$, [W]	13.395	15.727	19.567
P_{diode}, [W]	1.395	1.435	1.476
$T_{transistor}$, [ºC]	94.3	105.0	123.0
T_{diode}, [ºC]	45.2	47.1	51.0
$T_{Heatsink}$, [ºC]	41	43	47

When the fan was on, the current was larger, because of the smaller on-resistance achieved due to forced cooling.

The next experiment was made when the heat sink base was perpendicular to air flow and both air outflows were open.

TABLE X. RESULTS WHEN THE HEAT SINK IS PERPENDICULAR TO AIRFLOW AND BOTH OUTFLOWS ARE OPEN.

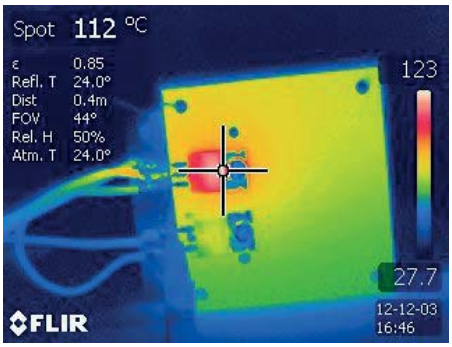
I, [A]	3.326	3.432	3.587
Vtransistor, [V]	4.078	4.636	6.007
Vdiode, [V]	0.428	0.427	0.424
RON, [Ω]	1.226	1.351	1.675
Ptransistor, [W]	13.563	15.911	21.547
Pdiode, [W]	1.422	1.465	1.521
Ttransistor, [ºC]	87.7	98.2	123.0
Tdiode, [ºC]	39.5	44.2	47.9
THeatsink, [ºC]	40	42	46

It can be seen from Table X that applied current is a little larger than before, because we have airflow flowing through both sides of the heat sink.

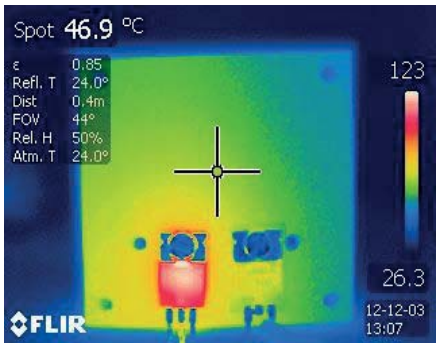
The last experiment with fan was when airflow is parallel to the heat sink base, i.e. fan attached to the side of heat sink.

TABLE XI. RESULTS WHEN THE HEAT SINK BASE IS PARALLEL TO AIRFLOW.

I, [A]	3.315	3.441	3.565
$V_{transistor}$, [V]	4.167	4.801	5.595
V_{diode}, [V]	0.425	0.424	0.425
R_{ON}, [Ω]	1.257	1.395	1.569
$P_{transistor}$, [W]	13.814	16.520	19.946
P_{diode}, [W]	1.407	1.459	1.515
$T_{transistor}$, [ºC]	87.5	101.0	123.0
T_{diode}, [ºC]	42.1	43.9	49.3
$T_{Heatsink}$, [ºC]	41	45	48



(a)



(b)

Fig. 12. Temperature distribution when airflow of the fan is: a) parallel to heat sink base; b) perpendicular to heat sink base, one outflow covered.

From Table XI it can be seen that the current is almost equal comparing with previous investigations even if the used airflow of fan is lower than in other types. It is correct

regarding theory, because the airflow is in parallel to fins and therefore can dissipate more power. Images made by thermo-camera for this are shown in Fig. 12.

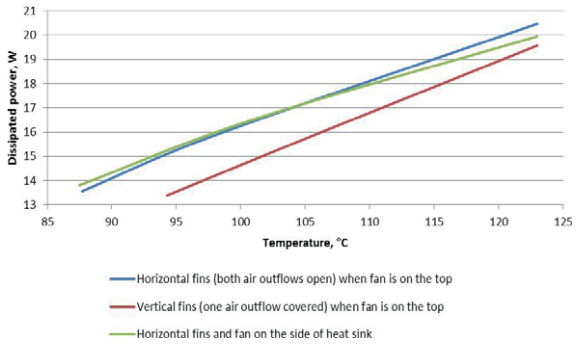


Fig. 13. Dissipated power of the transistor vs. temperature.

In Fig. 13 the dissipated power of the transistor vs. temperature of each type of experiment is shown. The dissipated powers of the diode are also not compared, because the powers are almost equal.

As it can be seen from Fig. 13, the dissipated power is the largest when airflow is perpendicular to the heat sink base and heat sink fins are horizontal.

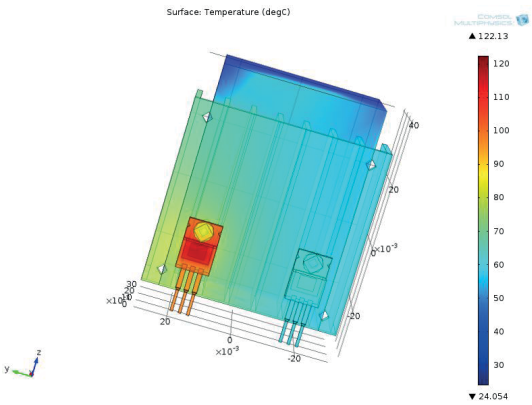


Fig. 14. Temperature distribution of the heat sink when the total dissipated power is equal to 23.5 W.

In simulation the velocity of air was applied equal to 1.66 m/s and the maximum dissipated power was selected according to measured value. Figure 14 shows the simulation results, i.e. temperature distribution when with airflow perpendicular to heat sink base and with one outflow. In simulation the PCB was not evaluated (only heat sink with the transistor and the diode). The applied dissipated power for transistor and the diode was 22 W and 1.5 W.

Since the real values of main heat sink parameters were used in simulations (dissipated power, fan air velocity), such FEM-based model with certain improvements could be used to verify the cooling capacity of different heat sink and fan combinations.

VIII. CONCLUSIONS

Three setup types with different distances between components and one or to air outflows open were investigated under natural convection. The largest dissipated power was achieved when the transistor was in the centre of the heat sink with distance between transistor and diode equal to 16.51 mm. In this case the dissipated power of the transistor was by 0.147 W larger compared to case when distance was 33.5 mm and by 0.273 W when distance was 26 mm. When the distance between components was changed, the diode temperature was by 3.6 ºC larger compared to distance of 26 mm.

By comparing results obtained with one and two air outflows (when the temperature of the transistor reached 123 ºC with one outflow covered) the temperature with both outflows open was 4 ºC larger. The dissipated power was 0.64 W lower as well. This may be influenced by varied component placement locations in respect of air movement under natural convection. This factor should be investigated thoroughly in future.

Comparing the theoretical dissipated power calculation of the heat sink with the real dissipated power, in real case the dissipated power was by 2.5 W larger because in this case we also have the cooling through the plane where the components are placed. In theoretical case it is assumed that the back side of the heat sink has perfect connection with component.

In case of forced convection it was obtained that the largest power was dissipated with both outflows open and with the airflow perpendicular to heat sink base. The dissipated power of the transistor is by 0.897 W larger compared to test with one outflow covered and by 0.518 W larger compared to case when airflow was parallel to the heat sink base.

Comparing the theoretical dissipated power calculation under airflow given by manufacturer with the real dissipated power, the dissipated power was approximately 8 W less. That was due to smaller fan attached compared to heat sink specifications. The heat sink area was 1.5 times larger than area of the fan.

In future research a detailed comparison of measurement and simulation results should be performed using fine-tuned heat sink test system with minimized number of uncontrolled experimental variables, such as electronic component location in relation to the heat sink or control of ambient temperature. Also, a method for real-world verification of modelling results should be developed.

REFERENCES

[1] P. Tarvydas, A. Noreika, Z. Staliulionis, "Analysis of heat sink modeling performance", *Elektronika ir Elektrotechnika (Electronics and Electrical Engineering)*, no. 3, pp. 49–52, 2013.

[2] Wakefield thermal solutions. *Extruded heat sinks. Chapter: Extruded heat sinks for DC/DC converters, series 517, 527, 518 & 528*.

[3] *Fairchild Semiconductor. IRF840 Data sheet*, Jan. 2002.

[4] *International rectifier, 10TQ data sheet Bulletin PD-20057 rev. B 06/06*.

[5] *DC Axial Flow Fan MCKD0505PFS2.11.GN datasheet*, Multicomp. [Online]. Available: http://datasheet.octopart.com/MCKD0505PFS2.11.GN-Multicomp-datasheet-5331633.pdf

[6] *Material Emissivity Properties* [Online]. Available: http://snap.fnal.gov/crshield/crs-mech/emissivity-eoi.html

[7] *COMSOL Heat Transfer Module User's Guide*, COMSOL, Apr. 2010, p.184.

[8] *COMSOL Multiphysics Reference Guide*, COMSOL, Apr. 2010, p. 426.

Appendix M

Thermal Modeling and Design of On-board DC-DC Power Converter using Finite Element Method

Elektronika IR Elektrotechnika, Vol. 20, No. 7, 2014, p. 38-44

http://dx.doi.org/10.5755/j01.eee.20.7.8022 ELEKTRONIKA IR ELEKTROTECHNIKA, ISSN 1392-1215, VOL. 20, NO. 7, 2014

Thermal Modelling and Design of On-board DC-DC Power Converter using Finite Element Method

Z. Staliulionis[1], Z. Zhang[2], R. Pittini[2], M. A. E. Andersen[2], A. Noreika[3], P. Tarvydas[3]
[1]*Department of Mechanical engineering, Technical University of Denmark, Kgs. Lyngby, DK-2800, Denmark*
[2]*Department of Electrical Engineering, Technical University of Denmark, Kgs. Lyngby, DK-2800, Denmark*
[3]*Department of Electronics Engineering, Kaunas University of Technology, Studentu St. 50, LT-51368 Kaunas, Lithuania*

***Abstract*—Power electronic converters are widely used and play a pivotal role in electronics area. The temperature causes around 54 % of all power converters failures. Thermal loads are nowadays one of the bottlenecks in the power system design and the cooling efficiency of a system is primarily determined by numerical modelling techniques. Therefore, thermal design through thermal modelling and simulation is becoming an integral part of the design process as less expensive compared to the experimental cut-and-try approach. Here the investigation is performed using finite element method-based modelling, and also the potential of such analysis was demonstrated by real-world measurements and comparison of obtained results. Thermal modelling was accomplished using finite element analysis software COMSOL and thermo-imaging camera was used to measure the thermal field distribution. Also, the improved configuration of power converter was proposed.**

***Index Terms*—Power electronic converters, temperature measurement, thermal modelling, finite element method.**

I. Introduction

This paper discusses about thermal design of boost isolated DC-DC converter. The thermal design was accomplished in order to evaluate the accuracy of the simplified power converter model compared to temperature measurement readings. To model the thermal distribution of power converter, it is very important to have a reasonable power converter model. Then, such modelling principles of power converter can be used for any type of power converter thermal investigation and design. Therefore, the temperature measurements of power converter were done which define the operating condition of power converter and helps to create a substantiated thermal model. Also, the power losses were estimated in order to have actual results for thermal modelling [1]. Then, this paper discusses the creation of the simplified component models which can be used to perform a thermal design of the whole power as a system of interacting components. Finally, the power converter thermal design results are compared with actual temperature readings.

Manuscript received December 16, 2013; accepted April 19, 2014.

II. Temperature Measurements of Full Bridge Boost Isolated Power Converter

For investigation purposes, the Full-bridge boost isolated power converter was used which is shown in Fig. 1. The converter mainly consists of the transformer, four transistors (TO-220), four diodes (TO-220), inductor, three output capacitors and two input capacitors.

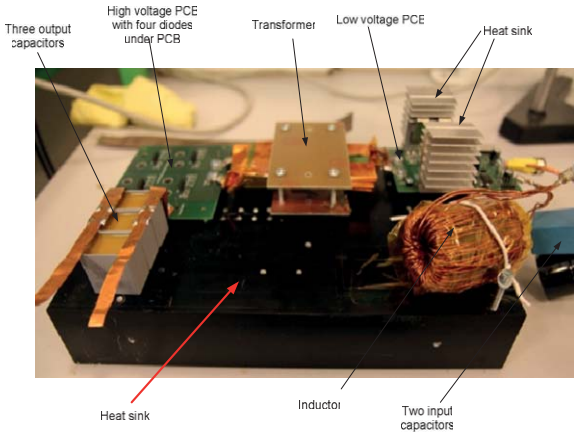


Fig. 1. Investigated Full-bridge boost isolated converter.

In order to find the hottest spot in the components of converter for temperature measurements, the TROTEC IC080LV infrared camera was used. The radiation emissivity of the black anodized heat sink is in the range from 0.82 to 0.86 and the emissivity was set equal to 0.85 on IR camera [2]. The images obtained by thermo-camera are shown in Fig. 2. The scale of temperature is different and fluctuating due to emissivity and other factors.

However the main aspect is not to measure the temperature as a physical quantity, but to find hot spots that affect the thermal load of entire system. The heat sinks seem colder in the images only due to emissivity, because they have the lowest emissivity comparing with transformer, inductor or PCB.

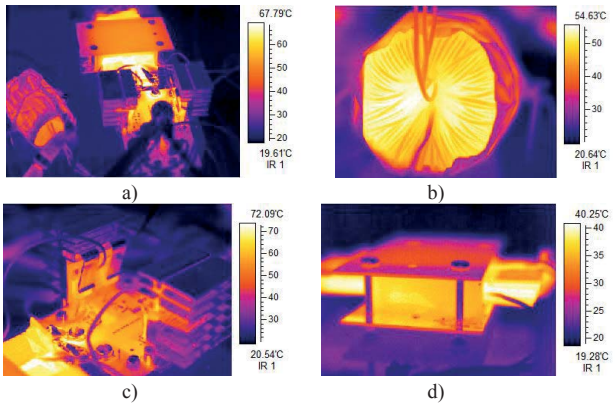


Fig. 2. The thermal view of whole converter (a); inductor temperature distribution (b); transistor and heat sink temperature distribution (c); transformer temperature distribution (d).

As it can be seen the hottest spot is in the inside of the inductor. Transformer has also hottest spots inside the core and around its windings. The transistor and the points which are very close to it reach highest temperature values. Other components of the converter are neglected, because they have a very low temperature and therefore are not investigated.

The thermocouples are chosen for use in temperature measurements; the thermocouple type is K-type (Chromel +, Alumel -). They are used with a multimeter Meterman 38XR in order to get the temperature readings. The attached thermocouples for whole converter are shown in Fig. 3. The temperatures were measured on transistor tab/case, on both heat sinks between transistors, inside of the inductor, inside the transformer, under the top winding layer and bottom layer.

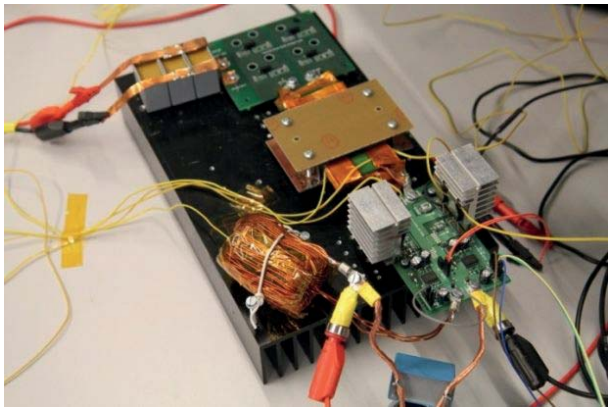


Fig. 3. Full-bridge isolated boost converter with attached thermocouples (yellow wires).

The thermocouple on the transistor tab/case was attached by soldering. On the heat sink, a small hole was drilled and a thermocouple was glued inside the hole. The thermocouple used on inductor was attached between inside windings with slightly covered thermal grease. In case of the transformer, the attachment principle was the same as for the inductor.

Afterwards, the measurements were performed when converter reached the steady-state conditions (constant temperature reading), but the values in this case contained an interference component due to electrical/magnetic noises which significantly influence correct temperature readings. Therefore the temperature measurements were made when converter is turned off and the readings immediately were registered in order to avoid errors caused by converter-generated interference. For this reason a simple test was made to check how fast the temperature decreases by 1 ºC degree on each measured component. While 1 ºC degree was lower than initial temperature, the time was approximately in the range 5 seconds-7 seconds for all thermocouples. Then, the measurements were accomplished and repeated 10 times for taking average measurement readings from multimeters. So, the maximum error according to taken readings could be 1 ºC degree. It can be assumed that the errors can be neglected, because they don't influence the measurement significantly.

The measurements were also repeated 10 times under each different output power in order to account for the random experimental errors and to obtain the average temperature value. The measurements were made under variable output load, input voltage and at 790 V output voltage with 750 ohm resistive load and 50 V input voltage. Table I presents several of temperature measurement cases and other important readings.

TABLE I. MEASURED TEMPERATURES UNDER EACH CASE OF INPUT AND OUTPUT POWER.

Resistive load, [Ω]	Output voltage, [V]	Input voltage, [V]	Temperature inside the transformer, [ºC]	Temperature at the top of transformer windings, [ºC]	Temperature of the bottom side of transformer core, [ºC]	Inductor temperature, [ºC]	Heat sink temperature, [ºC]	Tab (case) of transistor temperature, [ºC]	Heat sink temperature, [ºC]
380	620.3	50	70	61	54	58	70	77	69
750	789.1	50	79	67	63	60	72	78	71
750	790.1	60	72	63	58	46	53	55	52
750	789.5	40	77	67	60	65	71	77	70
950	790.9	50	73	62	57	45	55	61	54

Almost in all cases the temperature variation was relatively small; when a smaller output resistance value (380 Ω) was used, in order to get output 790 V, the temperature can be much higher (see Table I).

After temperature measurements, one particular case was chosen which was used for power loss estimation and modelling in COMSOL Multiphysics. The measurement parameters in this case were: resistive load 750 ohm, output voltage – 789.1 V, input voltage – 50 V. These operating parameters are common for this type of converter.

III. THERMAL MODELLING OF SEPARATE COMPONENTS OF POWER CONVERTER IN COMSOL MULTIPHYSICS

In order to proceed with the thermal modelling of power converter, the individual components of power converter should be created in order to ensure the modular structure of the entire model. The following most critical components are used: the transformer, inductor and two shiny aluminium heat sinks with attached transistors. Each heat sink has two attached transistors. Each component of the converter is modelled by a simplified geometry, in order to obtain a

number of degrees of freedom of the entire model as low as possible.

Primarily, in order to find a simplified model of each power converter component, the temperature difference was compared between accurate and simplified models.

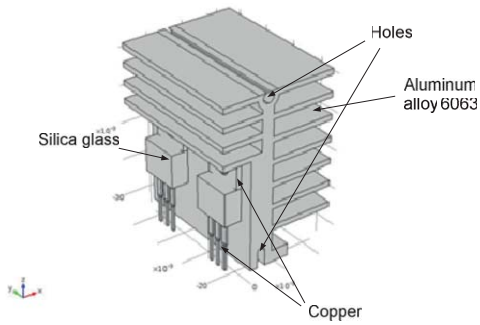


Fig. 4. Model of two transistors attached to the heat sink with designated materials (accurate model).

Firstly, the two transistors attached to the heat sink were investigated in order to compare accurate and simplified heat sink models and determine how much the simplified model impacts the thermal modelling of this component. The heat sink type OS515 from AAVID THERMALLOY Company [3] was used. The accurate model of heat sink with two transistors created in Comsol Multiphysics is presented in Fig. 4.

The simplified heat sink model was designed without thermal interface material (TMI), because it introduces an error of approximately 1 ºC at 5,031 W power losses (value obtained from modelling results); therefore we chose to neglect the absence of TMI. The thermal conductivities of all materials designated using Comsol Multiphysics are listed in Table II [4], [5].

TABLE II. THERMAL CONDUCTIVITY AND EMISSIVITY OF EACH MATERIAL.

Material	Thermal conductivity [W/m*K]	Emissivity
Heat sink and transistors		
Silica glass	1.38	0.92
Aluminum alloy 6063 (shiny)	200	0.1
Copper	400	0.2
Silicon	150	-
FR4	0.3	0.6
Inductor		
Core material (Carbonyl E Iron powder)	50.16	-
Copper	400	0.2
Kapton tape	0.12	0.08
Transformer		
Core material 3F3 (MnZn)	3.5	0.78
Copper	400	0.2
FR4	0.3	0.2
Steel AISI 4340	54	0.04

The heat transfer in solid physics and steady state condition is used for modelling, both for transformer and inductor modelling. In description of physics and boundary condition in COMSOL simulation, the convective coefficient and emissivity were applied; however the emissivity can be neglected due to insignificant impact on the total heat transfer (ε = 0.1). The average ambient temperature for all simulations cases, including transformer and inductor, was selected equal to 20 ºC; this value was chosen from the ambient temperature measurements. The convective coefficient is applied equal to 7.23 W/m^2*K. For comparison of simplified and detailed model, the temperature was measured on the transistor chip.

Also, the chip size of transistor was investigated. The purpose of this investigation was to analyse how the chip temperature varies dependent on chip size with the same boundary conditions as in previous modelling. After investigation, it was noticed that the size of transistor chip can influence the maximum value by approximately 0.45 ºC degree between small (3 × 3 mm) and larger (5 × 7 mm) chip. Small chip had higher temperature than the large one.

The power loss impact of transistor pins for temperature increase was evaluated, because the pins are subjected to a flow of strong electrical current. The electrical current was measured using oscilloscope and the power per each pin was estimated [6] to be equal to 0.067 W and during modelling it was applied only to drain and source pins. After modelling the chip temperature was higher 2.3 ºC than when heat power wasn't applied for transistor pins. Also, comparing accurate and simplified heat sink models, the transistor chip temperature was lower by approximately 2 ºC for accurate model.

After the heat sink modelling, the same was accomplished for the inductor component. The spatial model of the inductor is shown in Fig. 5 [7].

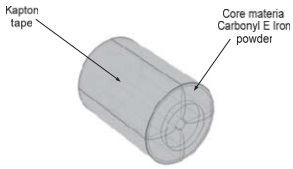


Fig. 5. Spatial geometry of inductor with designated materials.

The inductor was modelled when Kapton tape covers the component, as in real-world case. The used materials and their properties are listed in Table II. The winding block of the same geometry as in real case with the same volume, wrapped around the magnetic core, has been evaluated. The wrapped block is treated as a uniform power source [8]. Thermal conductivities and emissivities are given in Table II.

TABLE III. ESTIMATED POWER LOSSES OF EACH COMPONENT.

Transistor		Inductor		Transformer	
Parame-ter	Value	Parame-ter	Value	Parame-ter	Value
P_{cond}	1.334 W	P_{core}	0.478 W	P_{core}	4.611 W
P_{sw}	3.697 W	P_{DC}	6.464 W	P_{pri}	1.114 W
P_{tot}	5.031 W	P_{AC}	0.635 W	P_{sec}	0.878 W

The convective coefficient is applied equal to 8.1 W/m^2*K, however, heat convection of magnetic devices can vary in the range 6-10 W/m^2*K [9]. The estimated power losses are applied for core and windings (Table III).

The transformer was modelled and the final model is shown in Fig. 6. The transformer type E64/10/50 was used

[10].

The transformer winding block length is 98.5 mm, width – 53.80 mm, height – 10.2 mm. PCB (FR4) thickness is 1.6 mm, length – 100 mm, width – 60.7 mm. The PCB is used on both core sides. The properties of selected materials are presented in the Table II [11].

The convective coefficient is applied equal to 6.52 W/m^2*K. The estimated power losses are applied for core and winding block from Table III [12].

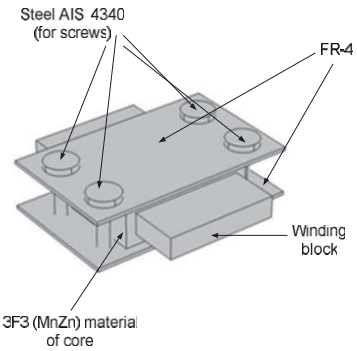


Fig. 6. Spatial model of transformer with designated materials.

The dimensions of windings and insulators are relatively small, what leads to a denser finite element mesh and, subsequently, modelling can take very long time. Therefore it is necessary to make some model simplifications. One method can be used when thermal conductivity of the winding block is estimated as equivalent [13], [14]. Each conductor is defined as a heat source inserted within the block. The internal heat transfer mechanism of the planar transformer is dominated by conduction; thus the equivalent thermal conductivity of a uniform block can be calculated by integrating the conductors and insulators. Firstly, thicknesses of conductor and insulator should be known. The equivalent thermal conductivity (k_{eq}) is estimated by equation

$$k_{eq} = \frac{h_{Cp} + h_{Dp} + h_{Cs} + h_{Ds}}{\frac{h_{Cp}}{k_C} + \frac{h_{Dp}}{k_{Dp}} + \frac{h_{Cs}}{k_C} + \frac{h_{Ds}}{k_{Ds}}}, \quad (1)$$

where h_{Cp} – thickness of conductor (primary side – 0.2 mm), h_{Cs} – thickness of secondary side conductor (70 µm), h_{Dp} – thickness of insulator (FR-4 – 0.2 mm), h_{Ds} – Kapton tape thickness (0.1 mm), k_C – thermal conductivity of conductor (400 W/m*K), k_{Dp} – thermal conductivity of Kapton tape (0.12 W/m*K), k_{Dp} – FR4 thermal conductivity (0.3 W/m*K). The equivalent thermal conductivity was obtained equal to 0.38 W/m*K.

In modelling, a large chip and 0.067 W heat power per each transistor pins was used in order to make modelling results as close as possible to measurement results. Despite the potential error of temperature values, the simplified heat sink was chosen for use in modelling due to advantages given by geometry simplification. Mentioned temperature errors could be evaluated by separate approximations, because sophisticated geometry influences the modelling duration and can introduce additional mesh generation issues. Also, the modelled transformer had quite a high temperature, because there was no heat sinking through screws. Next subchapter discusses the thermal design of the entire power converter and how previously designed models of separate components are introduced into the overall converter thermal design.

IV. THERMAL MODELLING OF POWER CONVERTER

The whole power converter placed on the heat sink which acts as cooling pad/board was modelled. All constituting components were placed on the heat sink in order to decrease their temperature which was higher compared to previous modelling of separate components. Then, the whole converter was modelled and results were compared with actual experimental temperature readings which also will be summarized below.

During the modelling procedure, all previous modelled components are imported into Comsol Multiphysics. The transistors with heat sinks are placed on the PCB, and PCB is attached to the main heat sink using four screws (see Fig. 7). Transformer was also attached to the heat sink using four screws. For inductor attachment the Kapton tape was used under it on the heat sink. The Kapton tape was used in modelling to reflect the real practical case, when additional shielding is required, despite the fact that the inductor temperature without tape can be decreased dramatically by the heat sink. Therefore, the Kapton tape with dimensions 0.06 m × 0.08 m was also used to cover the inductor in this case.

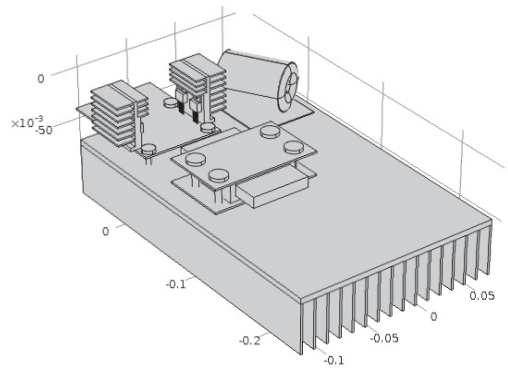


Fig. 7. Spatial geometry of power converter.

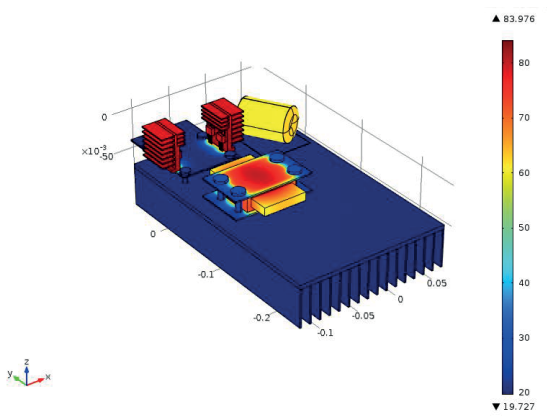


Fig. 8. Temperature distribution in entire power converter (temperature is in ºC scale).

When describing the boundary conditions, the ambient temperature was applied equal to 20 ºC degrees. All components were defined with the same convection boundary condition values as previously, because all pins

attached to the main heat sink had very small surface for convection. However, heat sink and PCB are used with 6.24 W/m^2*K and 5.31 W/m^2*K, respectively. Also, the inductor and two heat sinks touch the main heat sink via very small area, because one of them has circular form and other has small flat area which covers PCB. The black anodized aluminium (ε = 0.85) was used for the main heat sink. Furthermore, the emissivity for all three components is very low compared with the main heat sink emissivity, therefore the emissivity of the main heat sink plays a decisive role in heat transfer.

The modelling results can be seen in Fig. 8. Actual measured temperatures were compared with simulated temperatures at the same points of the converter. The comparison is shown in Fig. 9. The inside temperature of transformer, top winding of transformer, bottom side layer of transformer, inside inductor, heat sink 1, case of transistor, heat sink 2 are denoted as ITT, TWT, BSLT , II, HS1, CT, HS2, respectively.

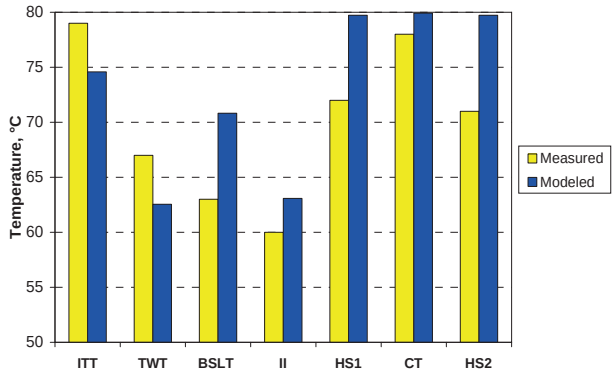


Fig. 9. Comparison of simulated and measured temperatures (with mesh of 1535771 elements).

The simulated temperatures were very close to actual measured results. The maximum error of temperature simulation was 8.17 ºC (with mesh of 1535771 elements) and is quite a reasonable value, because such difference in temperatures can still be used for prediction of the overall converter temperature trends. Usually, power converter is designed to keep temperature below 100 ºC, so the 8.17 ºC degrees error in this case is a significant value for temperature estimation, therefore this issue should be solved in further works by improving mesh refinement or modelling methodology.

V. IMPROVING THERMAL DESIGN AND INTEGRATION OF POWER CONVERTER

This chapter discusses how to improve thermal design and cooling of boost isolated power converter and to suggest the layout of components with higher integration compared to the model shown in Fig. 1. The simulated temperatures were compared with results for previous power converter.

This type of power converter has input filter consisting of two capacitors and its heat is neglected, because in experiments the filter was cold (see Fig. 1 and Fig. 10). The dimensions of two capacitors are: diameter 35 mm, height 30.5 mm, another one – 41 mm × 20 mm × 37 mm. Also, output filter consist of three same type capacitors which are modeled together as a block (see Fig. 10). The dimensions of capacitor block are 30.5 mm x 20.5 mm x 30.5 mm. The heat power also is neglected for this component as for input filter due to low temperatures. The high voltage PCB (see Fig. 1) was used with four diodes placed under the low-voltage PCB in order to reach higher integration. Each of the diodes contributes the heat power around 1 W [1]. The high-voltage PCB dimensions are 0.105 m x 0.088 m x 0.0016 m.

The heat sink was used of the same type as in previous case, with different length of 0.2 m. The heat sink is covered with mica (0.17 m x 0.18 m x 0.001 m) in order to ensure electrical insulation; for example, inductor, transformer and four diodes which are attached to the heat sink. The mica is used in a form of a large sheet in order to simplify the design in Comsol Multiphysics. Also, the output and input filters are placed on mica, although in practice it is not used in all cases. The output and input filters were placed in touch with inductor (the wires were covered by lacquer) in order to increase the thermal conductivity through them to the main heat sink. Furthermore, filters can improve cooling by heat convection [9].

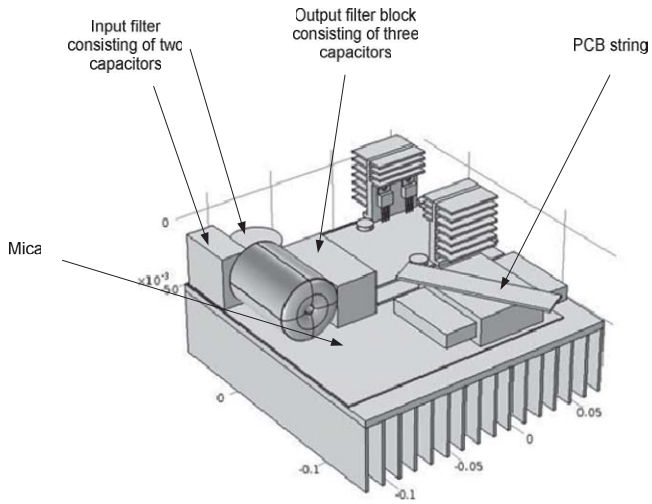


Fig. 10. Spatial geometrical model of proposed converter integration mode.

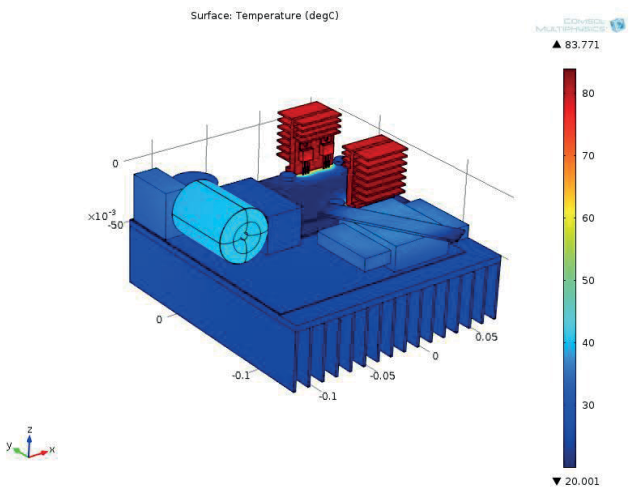


Fig. 11. The thermal distribution in power converter (temperature is in ºC scale).

The transformer was laid on the mica, in order to increase the thermal conduction to the heat sink. The vertical position was considered, but discarded as not reliable in this case due to contacts and stress for connecting wires, especially, in case of on-board applications. Thus, the bottom PCB plate of transformer was removed and the transformer can be fixed with PCB strip on the top by using two screws. The strip was chosen to be placed diagonally in order to get a stronger fixation. Moreover, a tightly attached strip could increase convection-based cooling. The two mentioned screws are neglected in modelling due to their relatively poor cooling impact on the heat sink (see Fig. 8, also verified by practical measurements). Also, these screws make the geometry more complex for modelling purposes and thus not so effective.

The structure which consisted of transistors attached to the heat sink, low-voltage PCB and four screws as fixing elements remained the same as in previous modelling (see Fig. 1 and Fig. 7).

The same boundary conditions are used as previously [15], however only for introduced capacitors the convection was applied equal to 5 W/m^2*K. The temperature modelling results are shown in Fig. 11.

The modelling results are shown in Fig. 12, where they are compared to the first modelling. Since, the low-voltage PCB had the same properties and the same heat sink, the temperatures of these components remained the same.

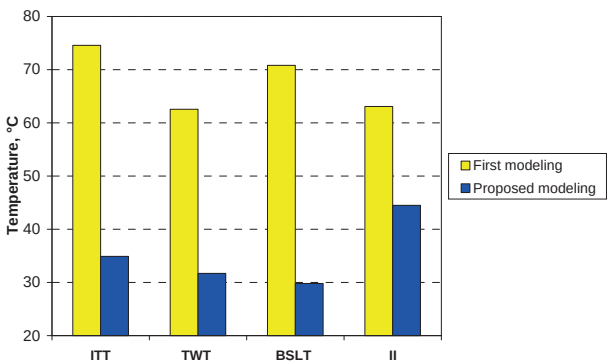


Fig. 12. Comparison of temperatures of previous modelling and proposed layout (with mesh of 1535771 elements).

Next modelling was accomplished with AlN and Al_2O_3 Direct Bonded Aluminum (DBA) substrate which has thermal conductivity equal to 170 W/m*K and 28 W/m*K, respectively. This is used in order to decrease temperatures of transistors together with heat sinks. The transistor temperatures are compared in Fig. 13.

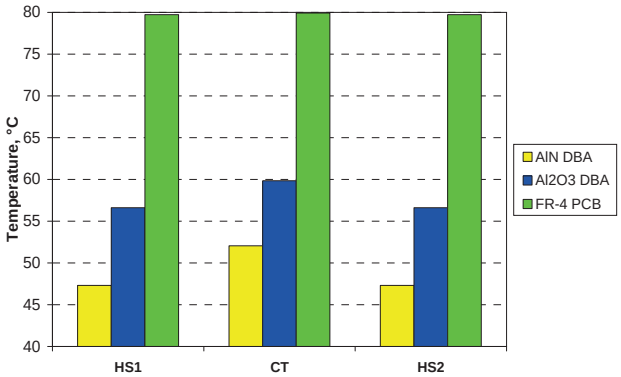


Fig. 13. PCB versus DBA technology with AlN and Al_2O_3.

To summarize, the new layout decreased the temperature of magnetic devices and integration was increased in power converter. As discussed previously, the filter helps to decrease the temperature of inductor; however, one capacitor influences that mostly, because it has the largest contact area and directly touches wires. Output capacitor and input circular capacitor has a very small contact area and even if the thermal conductivity can be quite high, the cooling is poor. In case of transformer, the cooling was improved very strongly. Comparing the PCB, AlN, Al_2O_3, it can be seen that AlN material gives the best thermal cooling improvement and thermal distribution over substrate. Also, comparing the thermal conductivities of different DBA materials, the Al_2O_3 material doesn't have a very large difference comparing with AlN, however thermal conductivities differ around 6 times.

VI. CONCLUSIONS

The library of thermal models of power converter components was created, which can be used for any type converter with the same components.

Comparing the measured and simulated temperatures of power converter components, it was found that the

temperatures differ within 8.17 ºC, compared to experimental temperature readings. The thermal modelling could be made more accurate and the mesh refinement or improved modelling methodology could be used in order to reduce the temperature error. It is also quite difficult to estimate the convection coefficient, but the thermal modelling can help to vary this coefficient if geometry or boundary conditions are defined quite accurately.

A new layout was proposed for the entire power converter design which provides an improved cooling for most critical components. The inductor temperature was decreased the least – it was 1.41 times less compared to previous model; the inside temperature of transformer was 2.13 times less, top winding of transformer – 1.97 less, the side of bottom winding was 2.37 less. In case of AlN DBA substrate, the temperature of transistor and heat sink was lowered with ratio 1.53 and 1.68, respectively. In case of Al_2O_3 DBA substrate, the temperature of transistor heat sink was lowered with ratio 1.33 and 1.4, respectively. Also, the area of boost isolated power converter placed on heat sink was reduced 1.5 times compared to the previous version, however the height remained the same.

ACKNOWLEDGMENT

The authors thank CELCORR/CreCon consortium (www.celcorr.com) for thermal imaging camera used in this work.

REFERENCES

[1] P. Tarvydas, A. Noreika, Z. Staliulionis, "Analysis of Heat Sink Modeling Performance", *Elektronika Ir Elektrotechnika*, vol. 19, no. 3, pp. 49–52, 2013. [Online]. Available: http://dx.doi.org/10.5755/j01.eee.19.3.3695

[2] *Emissivity values*. [Online]. Available: http://www.design1st.com/ /Design-Resource-Library/engineering_data/ /ThermalEmissivityValues.pdf.

[3] *Heat sink dimensions*. [Online]. Available: http://www.aavidthermalloy.com/cgi-bin/process.php?pf=euro_exdisp.pl&Pnum=0s515&LengthUnits=mm&ExLength=150.00&TReff=0.000.

[4] *Materials property data*. [Online]. Available: http://www.matweb.com/.

[5] *Emissivity of material*. [Online]. Available: http://www.everestinterscience.com/info/emissivitytable.htm.

[6] R. W. Erickson, D. Maksimovic, *Fundamentals of Power Electronics* p. 883.

[7] *Specifications of toroids*. [Online]. Available: http://toroids.info/T157-2.php.

[8] N. Delmonte, M. Bernardoni, P. Cova, R. Menozzi, "Thermal Design of Power Electronic Devices and Modules", in *Proc. COMSOL Conf* Milan, 2009.

[9] A. Van den Bossche, V. Valchev, "Thermal Design of Transformers and Inductors in Power Electronics", *Quatrième Conférence Internationale sur le Génie Electrique (CIGE 2010)*, Algerie, 2010. (in French)

[10] *Magnetic core dimensions*, Ferroxcube. E64/10/50 datasheet. 2008-09-01.

[11] *Magnetic material properties*, Ferroxcube. Soft ferrites, Ferrite materials survey. 2008-09-01

[12] Z. Zhang, R. Pittini, M. A. E. Andersen, O. C. Thomsen, "Analysis of Planar E+I and ER+I Transformers for Low-Voltage High-Current DC/DC Converters with Focus on Winding Losses and Leakage Inductance", in *Proc. Int. Power Electronics and Motion Control Conf. (IPEMC)*, 2012, pp. 488–493.

[13] P. Cova, N. Delmonte, "Thermal modelling and design of power converters with tight thermal constraints", *Microelectronics Reliability*, vol. 52, no. 9–10, pp. 2391–2396, 2012. [Online]. Available: http://dx.doi.org/10.1016/j.microrel.2012.06.102

[14] W. Zhang, "Integrated EMI/Thermal Design for Switching Power Supplies", Virginia Polytechnic Institute and State University, 1998.

[15] *COMSOL User's Guide* (version 4.3), chapter 13, "The Heat Transfer Branch", COMSOL. p. 1292, 2012.

Appendix N

Power Cycling and Thermal Stresses Analysis for High Efficiency DC/DC Converter (IFBBC) in Repetitive Avalanche Conditions

18th International Conference ELECTRONICS 2014

Power Cycling and Thermal Stresses Analysis for High Efficiency DC/DC Converter (IFBBC) in Repetitive Avalanche Conditions

R. Pittini[1], Z. Zhang[1], Ž. Staliulionis[2], M. A.E. Andersen[1]
[1]*Department of Electrical Engineering, Technical University of Denmark, Oersteds Plads 349, DK-2800, Kgs. Lyngby, Denmark*
[2]*Department of Mechanical engineering, Technical University of Denmark, Produktionstorvet Building 425, DK-2800, Kgs. Lyngby, Denmark*
ripit@elektro.dtu.dk, zz@elektro.dtu.dk, zygsta@mek.dtu.dk, ma@elektro.dtu.dk

[1]***Abstract*—Recent improvements in power electronics converters resulted in power converter efficiencies higher than 99%. The reduction of converters power loss reduces the need for converter cooling minimizing also the overall costs. Nowadays, a common practice in some high efficiency converter topologies is to rely on MOSFET avalanche ruggedness in order to minimize the converter complexity and cost. This paper presents an analysis of the short repetitive avalanche pulses in an isolated full bridge boost converter (IFBBC). The analysis aims to verify if short repetitive avalanche stresses can represent a reliability issue concerning converter power cycling. Moreover, the design of the cooling system is analysed based on 3D finite element method (FEM) simulations for balanced and unbalanced power dissipation. Experimental validation is based on a 6 kW converter prototype for bidirectional fuel cells applications achieving a peak efficiency of 97.8%.**

***Index Terms*—Power Semiconductor Devices, DC-DC Power Converters, MOSFET's Avalanche Breakdown, Power Cycling, Thermal Analysis.**

I. INTRODUCTION

Renewable energy sources and new applications for power electronics are driving the development of power converters. Large improvements have been achieved over the last decade, such as, new power semiconductors [1][2], new converter topologies and modulation strategies, which resulted in commercial power converters with efficiencies over 99% [3]. Power loss reduction in power converters allows minimizing the converter cooling system, which decreases the converter size and volume [4].

Fuel cells technology is a promising technology for renewable energy applications and electric mobility. Bidirectional fuel cells have large potentials in energy storage systems especially for grid connected applications [5]. Fuel cell typically operate at low voltage and high current levels therefore, they require high efficiency dc-dc converters to adapt the voltage-current levels.

The isolated full bridge boost converter (IFBBC) is a suitable topology for achieving high step-up ratio and high efficiency [6]. The IFBBC is often used in combination with passive or active clamps in order to limit the low voltage MOSFET stress. In order to achieve high efficiency, it is essential to optimize all the components in the power converter. For this topology, special care is required for the magnetic components design and circuit layout. This contributes to minimize the stresses over the power semiconductors. However, due to the circuit and transformer parasitics, short repetitive avalanche power loss pulses over the low voltage MOSFETs are observed [6]. In state-of-the-art power MOSFETs, the avalanche is purely limited by the maximum junction temperature and by the maximum power dissipation of the device. However, the repetitive high power loss pulses could represent an issue, not only for power dissipation, but also for the converter reliability. In many cases, the design of a power electronic converter considers the size and optimization of the cooling system and does not take into account continuous temperature variations of the power semiconductor junction and of the package layers. Continuous and periodic temperature variations could have a significant impact on the converter reliability due to thermal and power cycling stresses [7]. The avalanche of a power MOSFET represents a critical condition where the power semiconductor is dissipating a large amount of power which causes the junction temperature to rise. Depending on the duration and on the power dissipated during repetitive avalanche conditions, the phenomena could cause power cycling stress of the power devices influencing the power converter reliability.

This paper presents an analysis of the avalanche stress conditions of the low voltage MOSFETs in an IFBBC. The analysis aims to verify that the repetitive avalanche condition does not represent a reliability issue in terms of converter power cycling of the low voltage side MOSFETs. Moreover, thermal analysis of the power stage is performed in finite element method (COMSOL) in order to validate the converter thermal design. The analysis is based on an experimental IFBBC prototype optimized for bidirectional fuel cells applications and capable of achieving peak efficiency of 97.8% [6].

II. POWER SEMICONDUCTORS POWER AND TEMPERATURE CYCLING

Power and temperature cycling of power semiconductors are a well know source of failure of power electronics

Project sponsored by the Energy Technology Development and Demonstration Programme (EUDP) "Green Natural Gas", 2011-2014

converters. Failure mechanisms are related to mechanical stresses that are generated between the different materials in the power semiconductors packages. These are caused by the different thermal expansion coefficients of the various package layers.

Power cycling occurs due to the heat that is generated by the power semiconductor itself (switching and conduction losses). The heat generated by the power semiconductor chip flows through the various layers in the package until it reaches the heatsink. Power semiconductors conduction and switching losses do not generate power cycling if the converter is operated in steady state conditions (except in specific topologies and applications, as presented in [8]). This occurs because the layers of the power semiconductor package act as a low pass filter allowing only the average component of the power loss to flow through the heatsink. However, repetitive light and full load cycles would cause temperature cycling of the power semiconductor package layers.

Thermal cycling is another cause of failure of power semiconductors. Similar to power cycling the failure is related to the repetitive stress of the power semiconductor package layers. However, in this case the source that causes the temperature cycles is external and not due to the semiconductor's power loss itself.

Repetitive high power dissipation during short periods (e.g. during avalanche conditions) can represent a source for semiconductor power cycling, which will affect the reliability of power electronics converters.

A. *Bond Wire Lift-Off*

Bond wires are used for interconnecting the package leads to the chip. Due to the repeated temperature cycles of the junctions and bond wires, large mechanical stresses are accumulated at the bond wire-chip interface. Micro-fractures at this interface start growing until the bond wire cracks and detaches from the chip. This phenomenon can be monitored by measuring the on-state resistance of the power semiconductor. An increase of the on-state resistance of more than 5% indicates degradation of the bond wire connections and imminent failure of the power semiconductor [9][10].

B. *Solder Layer Fatigue*

A thin solder layer is used to attach the chip to the package tab (e.g. TO-220 package) or on a direct bonded copper substrate (DBC [10]). Repetitive temperature cycles of the chip and this layer causes strains in the solder layer that lead to micro-fractures. Micro-fractures cause an increase of the junction-to-case thermal resistance (R_{jc}) and limit the power dissipation capabilities of the device [10]. The increase of R_{jc} increases the junction temperature and its temperature swings during on-off operation worsening the phenomenon. An increase of R_{jc} of 20% [10] indicates a significant degradation of the solder layer.

III. ANALYSIS OF MOSFETS POWER CYCLING FOR IFBBC

The developed high efficiency dc-dc converter is an IFBBC as shown in Fig. 1, which is designed for bidirectional fuel cells applications. The converter is designed to operate in a wide voltage and current ranges (30-80 V up to 80 A on the low voltage side and 700-800 V on the high voltage side) [6]. The transformer has been optimized to have low leakage inductance since this would limit the current commutation time of the low voltage side MOSFETs. No active or passive clamp is used in the topology and therefore, high power semiconductor stresses are expected on the converter low voltage side.

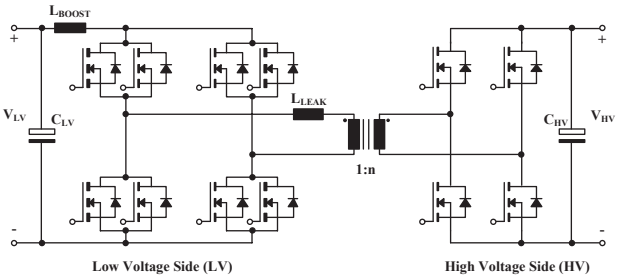


Fig. 1. Analysed converter topology: isolated full bridge boost converter (IFBBC) presented in [6].

Repetitive avalanche conditions occur every switching cycle at every turn-off event. Fig. 2 shows the first time interval (charging interval) where all low voltage side MOSFETs are active and the current in the input inductor rises. Fig. 3 shows the inductor's discharging interval. Two diagonal switches are turned off, which creates a current path through the transformer and allow the energy to be transferred to the secondary side. The current commutation time (current *di/dt*, from the charging cycle to the discharging one) is limited by the leakage path of the transformer, by the MOSFET package (stray inductance of TO-220) and by the circuit interconnections/layout. During this transition, as shown in the interval *t1-t2* on Fig. 4, the MOSFETs that are switching off are operating in avalanche conditions. The avalanche produces large power loss since the power devices are stressed with high voltage (above its nominal ratings) and high converter current. This is highlighted in Fig. 4 where the MOSFET on the converter low voltage side goes into avalanche conditions for about 60 ns (interval *t1-t2*).

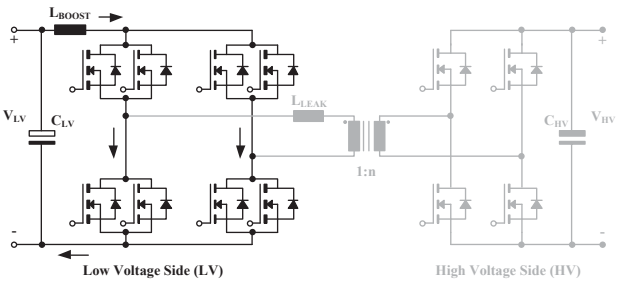


Fig. 2. IFBBC: Current path during boost inductor charging cycle.

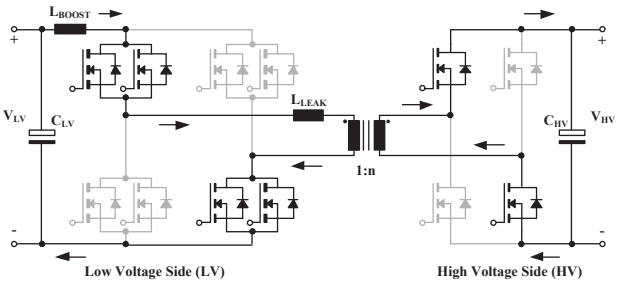


Fig. 3. IFBBC: Current path during boost inductor discharging cycle.

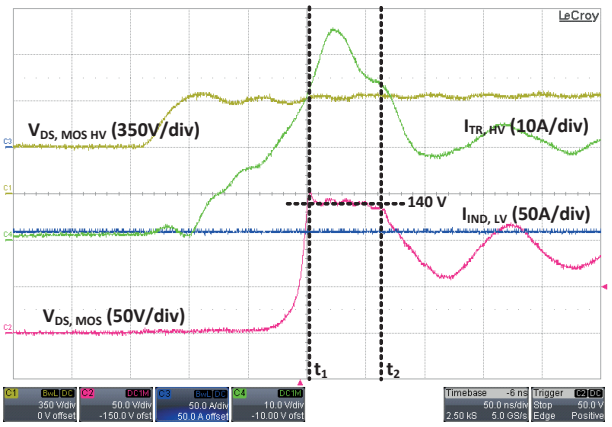


Fig. 4. IFBBC switching waveforms during avalanche at 80 A input current. Voltage over the high voltage switches (Ch.1: 350 V/div). Voltage over the low voltage switches (Ch.2: 50 V/div). Dc-current on the converter low voltage side (Ch.3: 50 A/div). Ac-current on the transformer winding on the high voltage side (Ch.4: 10 A/div).

In the developed converter each switch of the full bridge configuration on the low voltage side is composed by two parallel MOSFETs (Toshiba TK72E12N1). However during avalanche it is not possible to ensure that the current is equally shared between the two parallel devices due to differences in avalanche thresholds [11]. For this reason the worst case scenario has to be considered (the entire converter current is handled by a single device). The energy dissipated during a single avalanche event is calculated as in (1), which assumes that the current varies linearly during the avalanche period (inductive commutation). Considering the converter operating at its maximum current (80 A) the MOSFETs avalanche occurs at 140 V and 90 A (MOSFETs turn-off current including the inductor ripple). In these conditions, each avalanche event produces a power loss of 378 µJ. The MOSFETs are rated for a single pulse avalanche of 256 mJ, which is almost a factor 1000 below the verified stress condition. Lower converter current levels will have lower avalanche energy loss and therefore, they will represent less critical conditions.

$$E_{av} = \int_{t_1}^{t_2} V_{MOS}(t) I_{MOS}(t) dt = \frac{1}{2} V_{av} I_{av} t_{av} \qquad (1)$$

A. *Derivation of the Thermal Model for the Power Semiconductors Package and Heatsink*

The analysis requires a complete thermal model of the power semiconductors and of the converter cooling system. Since only the low voltage power devices are subject to avalanche conditions only the package used in these switches (TO-220) is analysed in detail. One device package has been open in order to verify the silicon chip size and tab dimensions since these have significant influence on the circuit thermal transient response.

A Foster thermal equivalent network could be extracted from the thermal transient response of the components datasheet. However, this type of thermal equivalent network is only a mathematical representation and it does not have any correlation to the physical layers of the of the device package. For this reason, a Cauer network representing all the package layers is built. Each layer of the package is represented by a thermal π equivalent; this representation considers the layer interfaces and it equally distributes the layer thermal capacitance at the layer boundaries.

Each layer is based on the material properties shown in Table I, the equivalent thermal capacitance are calculated as in (2) and in a similar way its thermal resistance is given by (3).

TABLE I. MATERIALS PROPERTIES.

Material	Thermal Conductivity $\left[\frac{W}{m \cdot K}\right]$	Density $\left[\frac{Kg}{m^3}\right]$	Specific Heat Capacity $\left[\frac{J}{Kg \cdot K}\right]$
Silicon	130	2330	703
Solder (SnAgCu)	57.3	7500	230
Copper	400	8940	385
Silicone Pad	1	2100	1300
Aluminum	237	2700	897

$$C_{th} = C_{spec} m_{av} \qquad (2)$$

$$R_{th} = \frac{1}{\lambda} \frac{l}{A} \qquad (3)$$

Where C_{spec} is the specific heat capacity, m is the mass, λ is the thermal conductivity, l is the length, A is the area of the layer assuming the heat flow perpendicular to all the layers.

Based on the dimensions of the silicon chip (chip size 4 mm x 6.5 mm x 0.25 mm) it is calculated that the mass m_j of a single silicon chip is 1.51 µg and its thermal capacitance is 11 mJ/K. Based on (3) the thermal resistance of the Si chip is 0.072 K/W. The silicon chip is soldered on the tab of the TO-220 with a thin layer (~40 µm) of lead free solder (SnAgCu). Given these values it is possible to calculate the thermal resistance and capacitance of the solder layer assuming that the area perpendicular to the heat flow is the same as the junction-chip area. This results in a thermal resistance of 0.026 K/W and a thermal capacitance of 1.85 mJ/K. The copper tab of the TO-220 package that transports most of the heat is just below the silicon chip; the tab active area is about 5.8 mm x 8.4 mm and it has a thickness of 1.3 mm. This results in a tab thermal resistance of 0.067 K/W with a thermal capacitance of 218 mJ/K.

The overall calculated thermal resistance from junction to tab is 0.165 K/W while the maximum value one specified in the datasheet of the device is 0.49 K/W). The silicone pad and heatsink thermal capacitances and resistances are calculated as in (2)(3). The thermal capacitance and resistance of each layer are summarized in Table II. Based on these values the Cauer thermal model shown in Fig. 5 is built. In the simplified thermal, shown in Fig. 6, C_1 represents the interface between the junction and the solder layer, C_2 represents the interface between the solder layer and the package tab, C_3 represents the interface between the package tab and the silicone pad, and, C_4 represents the interface between the silicone pad and the heatsink.

TABLE II. SUMMARY OF THE THERMAL EQUIVALENT PARAMETERS.

Property	Thermal Resistance [K/W]	Thermal Capacitance [J/K]
Junction	0.072	11e-3
Solder	0.026	1.85e-3
Tab	0.067	218e-3
Pad	1.6	105e-3
Heatsink*	14.4	39

* With natural cooling considering the heatsink thermal resistance and capacitance are considered equally distributed between all the power MOSFETs

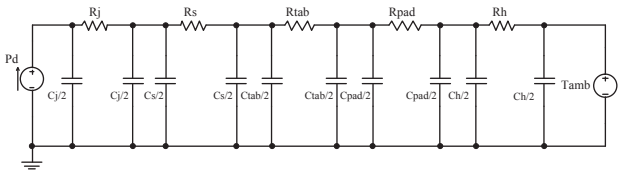


Fig. 5. Complete distributed thermal network.

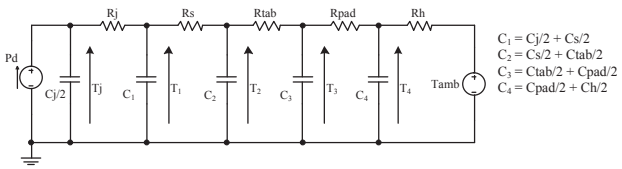


Fig. 6. Simplified distributed thermal network.

B. Power Cycling Analysis

The analysis is based on the complete thermal model of the MOSFET-heatsink assembly. It is assumed that avalanche is the only phenomena that generates heat during the avalanche interval (interval t1-t2, $\Delta Q = E_{av}$) and it is entirely generated in the MOSFET chip. Therefore, it is possible to calculate the chip temperature rise according to (3). Each avalanche pulse produces a temperature rise of the MOSFET chip of 0.06 ℃. This is based on the assumption that avalanche and the generated heat are an instantaneous event. Moreover, the generated heat is considered to increase the temperature over the thermal capacitance *Cj/2* (half-layer distribution of the junction thermal capacitance).

$$\Delta T = \frac{\Delta Q}{C_{th}} = \frac{E_{av}}{C_{spec} m_{MOS}} \tag{4}$$

Power cycling is observed when layers in a structure are subject to continuous significant temperature variations. Temperature variations below 1 ℃ are in general not sufficient to cause significant strains to damage the layers in the structure. The stress analysis is followed up since other MOSFETs types (e.g. with smaller chip size) can be subject to higher temperature cycles and, therefore, sensitive to power cycling.

Based on the thermal equivalent shown in Fig. 6, it is observed that the dissipated avalanche power *Pd* in parallel to half the junction capacitance *Cj/2* are the source of the temperature cycles. Once the junction operating temperature has been reached (operating point dependant), based on the assumption that the avalanche loss generation an instantaneous event, the temperature oscillations over the junction will simply be determined by the dissipated avalanche energy (4). This indicates that in steady state conditions, the parallel of *Pd* and *Cj/2* in Fig. 6 can be replaced by an ac-source representing the temperature oscillations at the junction, T_{j-ac}.

The critical layers for power cycling are the junction-solder interface and the solder-tab interface. Therefore, the temperature at these interfaces is the most relevant and it is represented by the temperatures across C_1 and C_2 in Fig. 6. The temperatures at interfaces T_1 and T_2 can be studied based on a Laplace transform/anti-transform or with a transient analysis. An ac-analysis of the thermal equivalent circuit in Fig. 6 highlights that large R-C values will result in large thermal time constants. The converter is operating at a switching frequency of 40 kHz therefore, also the avalanche period is 25 µs. Time constants significantly larger than the avalanche period will allow only the averaged dissipated power to flow through the structure. One of the largest thermal time constants is encountered at the pad-heatsink interface; this is due to the large thermal resistance of the thermal interface material and the large mass of the aluminium heatsink. Therefore, it can be assumed that at the previous interface shown in Fig. 6 (tab-pad interface, T_3) only the average power loss is flowing through the structure. With the previous assumption, the capacitance C_3 is paralleled to a low impedance network. The ac-analysis can be performed based on a Laplace transformation giving the temperature swings at the desired interfaces (T_1 and T_2). The temperature swings at interface T_1 can be expressed as in (5) and a similar derivation can be performed also for the interface T_2.

$$\frac{T_1}{T_{j-ac}} = \frac{Z_{C_1} \| [Z_{R_s} + Z_{C_2} \| Z_{R_{tab}}]}{Z_{R_1} + Z_{C_1} \| [Z_{R_s} + Z_{C_2} \| Z_{R_{tab}}]} \tag{5}$$

With this method it is possible to obtain a simplified analysis of the thermal swings across the layers in the power semiconductor and in the cooling system structure. When temperature swings in the critical layers (e.g. in the power semiconductor junction or in the solder layers) are in the range of 5 ℃ or above, then, the components are subject to power cycling. This stress, if not properly taken into account, could lead to a device and converter failure.

IV. THERMAL ANALYSIS OF THE LOW VOLTAGE POWER SEMICONDUCTORS AND CONVERTER PROTOTYPE

Aforementioned the repetitive avalanche conditions in the IFBBC do not represent an issue for power cycling of the low voltage power semiconductors. The avalanche phenomenon is entirely limited by the converter cooling system and by the maximum power dissipation of the single power semiconductor (package limitation). For this reason the converter cooling system is modelled in COMSOL and results are validated on an experimental prototype.

The primary power stage model is built in COMSOL according to the package layers and to the model shown in Fig. 6. The switches are mounted on a heatsink SK44-100 (100 mm x160 mm x 15 mm) with forced air cooling from the bottom side of the heatsink, as shown in Fig. 7. Losses are calculated according to [6] and based on the converter low voltage side operating point (40 V 80 A). At this operating point the low voltage side MOSFETs are dissipating ~20 W due to conduction losses and ~54 W due to avalanche losses/switching losses. Two cases are analysed in the thermal simulations: the first case considers the losses equally distributed between all the primary MOSFETs and the second case considers the avalanche unevenly distributed between the MOSFETs.

Assuming balanced loss power dissipation over the MOSFETs (due to asymmetric positioning of the power semiconductors compared to the heatsink) the junction's temperatures are in the 79-73 ℃ range. The hottest power devices are in the middle location on the heatsink on the top part as shown in Fig. 8. The heatsink temperature was in the 53-32 ℃ range where the hottest temperature is observed in

the semiconductors center part. In the second case unbalanced power dissipation is investigated on Fig. 9. A large difference in the junction temperatures of the power devices is observed: the devices with the largest power dissipation reach temperature in the range or 98 ℃, while for the other devices the junction temperatures are limited to ~54 ℃ as shown in Fig. 10. The heatsink temperature remains in the same range (54-32 ℃).

One important consideration is that as the temperature of the power semiconductor increases, the avalanche voltage increases [12][13]. This phenomenon leads that in a MOSFET parallel connection, the hottest MOSFET will be less likely to be the one subject to avalanche condition. Therefore, the phenomenon will try to balance the avalanche losses over all the power MOSFETs.

The converter thermal design is verified on a dc-dc converter prototype, as shown in Fig. 11. The designed converter [6] has the power semiconductors assembled on a heatsink mounted under the PCB board, as shown in Fig. 11. Due to this fact, it is not possible to measure the temperature of all eight low voltage power devices with the thermo-camera. The layout allows monitoring the temperature of two power semiconductors representing the devices on the right side of Fig. 12. Temperatures are monitored with a thermo-camera Flir T650 positioned on the right side of the converter prototype. It is verified that there is an unbalance in the power loss distribution of the power devices. In fact, one device reaches a temperature of 100 ℃ while the other one 71.4 ℃ (spot 2 in Fig. 13). This confirms the 3D FEM analysis with the unbalanced case, where the device temperature can reach peaks of ~100 ℃. The measured heatsink temperature is 47.6 ℃ (spot 1 in Fig. 13) compared to a simulated temperature of ~48 ℃ (maximum temperature on the right side of the heatsink in Fig. 12).

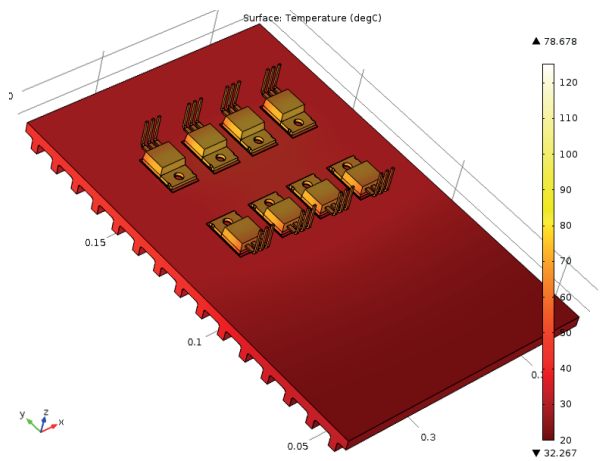


Fig. 7. COMSOL model of the power semiconductors and of the cooling system (heatsink) for the converter low voltage side. Steady state thermal analysis considering equal power dissipation over the power MOSFETs.

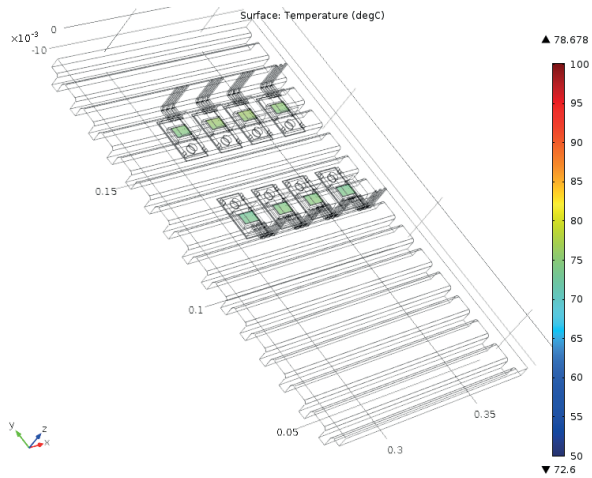


Fig. 8. COMSOL model: junction temperatures at steady state for equal power dissipation over the power MOSFETs.

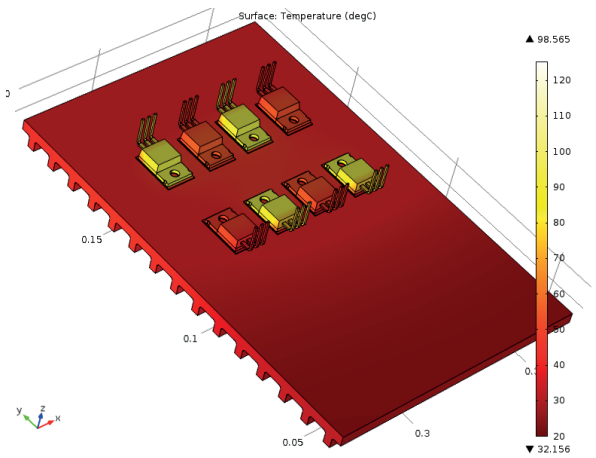


Fig. 9. COMSOL model: steady state thermal analysis considering uneven power dissipation over the power MOSFETs.

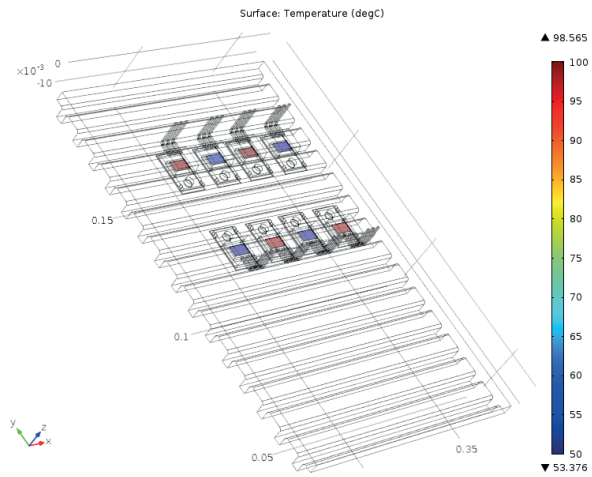


Fig. 10. COMSOL model: junction temperatures at steady state for uneven power dissipation over the power MOSFETs.

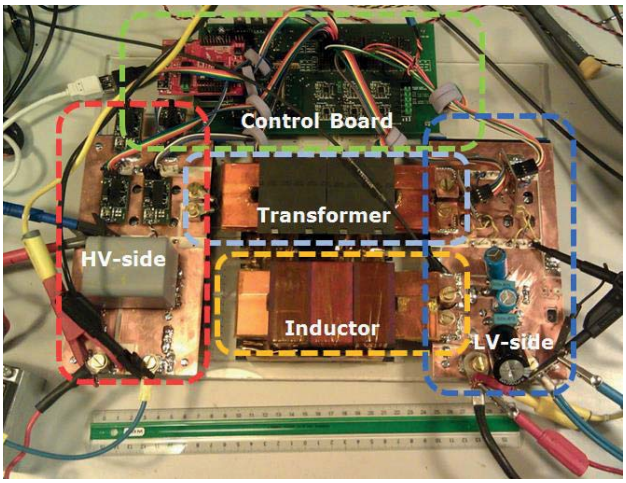


Fig. 11. Developed 6 kW dc-dc converter prototype (30-80V 0-80 A and 700-800 V, [6]).

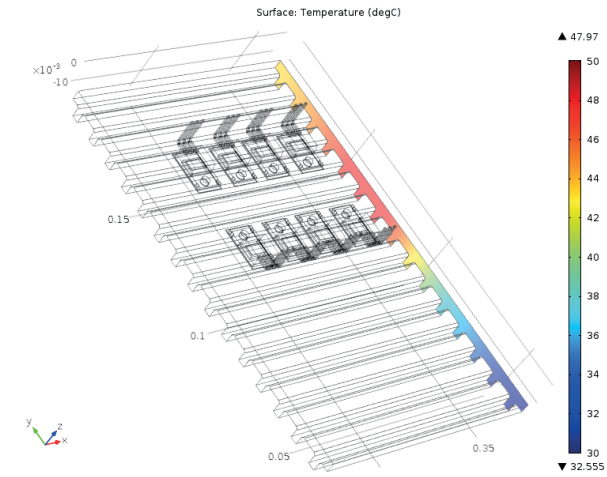


Fig. 12. COMSOL model: steady state temperature on the right side of the heatsink.

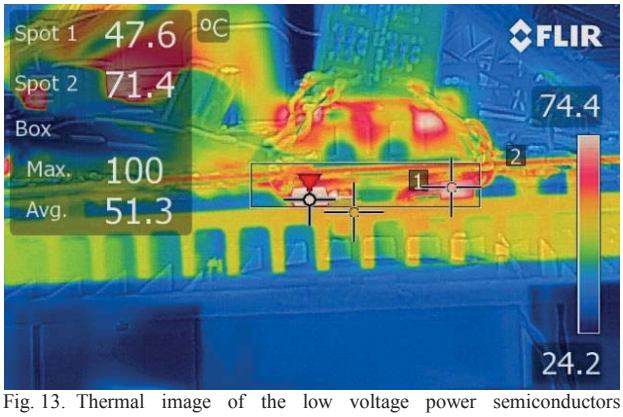


Fig. 13. Thermal image of the low voltage power semiconductors highlighting uneven power dissipation. Hottest MOSFET 100 °C, coldest MOSFET 71.4 °C, heatsink wall temperature 47.6 °C

V. CONCLUSIONS

The paper presents a thermal analysis of the repetitive avalanche in a high efficiency isolated full bridge boost converter (IFBBC). The methodology to verify the impact of the avalanche pulses on the converter power cycling has been presented. Short repetitive avalanche conditions do not represent an issue for power cycling of power semiconductors in IFBBC since the energy dissipated during these pulses is not large enough to create relevant temperature oscillations over the junction temperature. Moreover, large thermal time constants act as a low pass filter minimizing even more the temperature oscillations.

The thermal design of the converter prototype is verified with COMSOL simulations. This verified that even in unbalanced avalanche conditions (dissipated power not even between the power semiconductors) the MOSFETs are operating within the maximum temperature ratings. The FEM analysis is verified based on an experimental prototype of a dc-dc converter highlighting that in the experimental prototype unbalance power loss occurs.

REFERENCES

[1] Ostling, M.; Ghandi, R.; Zetterling, C.; , "SiC power devices — Present status, applications and future perspective", IEEE 23rd International Symposium on Power Semiconductor Devices and ICs, ISPSD 2011, pp.10-15, 23-26 May 2011.

[2] Khan, M.A.; Simin, G.; Pytel, S.G.; Monti, A.; Santi, E.; Hudgins, J.L.; "New Developments in Gallium Nitride and the Impact on Power Electronics", IEEE 36th Power Electronics Specialists Conference 2005, PESC 2005, pp.15-26, 16-16 June 2005.

[3] SMA Solar Technologies AG, www.sma.de.

[4] Pavlovsky, M.; Tsuruta, Y.; Kawamura, A., "Pursuing high power-density and high efficiency in DC-DC converters for automotive application", IEEE Power Electronics Specialists Conference 2008, PESC 2008, pp.4142,4148, 15-19 June 2008.

[5] Pittini, R.; Zhe Zhang; Andersen, M.A.E., "Analysis of DC/DC converter efficiency for energy storage system based on bidirectional fuel cells", 4th IEEE/PES Innovative Smart Grid Technologies Europe 2013, ISGT EUROPE 2013, 6-9 Oct. 2013.

[6] Pittini, R.; Zhe Zhang; Andersen, M.A.E., "Isolated full bridge boost DC-DC converter designed for bidirectional operation of fuel cells/electrolyzer cells in grid-tie applications", 15th European Conference on Power Electronics and Applications 2013, EPE 2013, pp.1,10, 2-6 Sept. 2013.

[7] Anzawa, T.; Qiang Yu; Yamagiwa, M.; Shibutani, T.; Shiratori, M., "Power cycle fatigue reliability evaluation for power device using coupled electrical-thermal-mechanical analysis", 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems, 2008. ITHERM 2008, pp.815,821, 28-31 May 2008.

[8] Pittini, R.; D'Arco, S.; Hernes, M.; Petterteig, A., "Thermal stress analysis of IGBT modules in VSCs for PMSG in large offshore Wind Energy Conversion Systems", Proceedings of the 2011-14th European Conference on Power Electronics and Applications EPE 2011,, pp.1,10, Aug. 30 2011-Sept. 1 2011.

[9] Smet, V.; Forest, F.; Huselstein, J.; Rashed, A.; Richardeau, F., "Evaluation of V_{\rm ce} Monitoring as a Real-Time Method to Estimate Aging of Bond Wire-IGBT Modules Stressed by Power Cycling," Industrial Electronics, IEEE Transactions on , vol.60, no.7, pp.2760,2770, July 2013.

[10] Lutz, J., "IGBT-Modules: Design for reliability," 13th European Conference on Power Electronics and Applications 2009, EPE 2009, pp.1,3, 8-10 Sept. 2009.

[11] Buttay, C.; Brevet, O.; Allard, B.; Bergogne, D.; Morel, H., "Paralleling of low-voltage MOSFETs operating in avalanche conditions," 2005 European Conference on Power Electronics and Applications, pp.9 pp.,P.9.

[12] Azoui, T.; Tounsi, P.; Dorkel, J.M., "Temperature Sensing for Power MOSFETs in Short Duration Avalanche Mode," IEEE Transactions on Device and Materials Reliability, vol.PP, no.99, pp.1,1.

[13] Alatise, O.; Kennedy, I.; Petkos, G.; Heppenstall, K.; Khan, K.; Parkin, J.; Koh, A.; Rutter, P., "The Impact of Repetitive Unclamped Inductive Switching on the Electrical Parameters of Low-Voltage Trench Power nMOSFETs", IEEE Transactions on Electron Devices, vol.57, no.7, pp.1651,1658, July 2010.

Appendix O

Primary Parallel Secondary Series Flyback Converter (PPSSFC) with Multiple Transformers for Very High Step-Up Ratio in Capacitive Load Charging Applications

2014 Applied Power Electronics Conference and Exposition (APEC 2014)

Primary Parallel Secondary Series Flyback Converter (PPSSFC) with Multiple Transformers for Very High Step-Up Ratio in Capacitive Load Charging Applications

Riccardo Pittini, Lina Huang, Zhe Zhang and Michael A. E. Andersen
Department of Electrical Engineering
Technical University of Denmark
Oersteds Plads, Building 349, Kgs. Lyngby, Denmark
Email: ripit@elektro.dtu.dk, huang@elektro.dtu.dk, zz@elektro.dtu.dk, ma@elektro.dtu.dk

***Abstract*— Flyback converters are widely used in several applications, however, with this topology it is very challenging to achieve high voltage operation especially with very high step-up ratio (>500) within limited space. This paper presents a new flyback-based topology which utilizes primary parallel and secondary series transformer connection in order to achieve very high step-up ratio (up to 650) as well as high voltage operation (~2 kV) in a small volume. The topology is presented and analyzed. The advantages and disadvantages of the proposed topology are discussed. A prototype used to verify the proposed topology has been implemented. Finally, experimental results are used to validate the performance of the proposed topology.**

I. Introduction

Power electronics converters are used in an increasing number of fields and applications. The improvements in power electronic devices and semiconductor materials have significantly reduced the cost of power converters and increased their efficiency. The research concerning the power converters, however, is mostly focus on processing the power for resistive or resistive-inductive load. In recent years, capacitive load applications have been gradually brought into the view of researchers as well as engineers. One successful application is the photoflash capacitor inside the camera [1]. In addition, capacitive smart material, such as piezoelectric material and Dielectric Electro Active Polymer (DEAP) [2][3], have gained extensive attention from academia and industry and they can be potentially used in a variety of applications [4][5]. The major advantage given by these materials is that it is possible to have non-magnetic actuator which can be applied in some magnetic sensitive occasions, e.g. in magnetic resonance imagining (MRI). These types of actuators have a capacitor-like structure where the dielectric material is confined between two electrodes. By applying a voltage difference between the electrodes, charge is stored in the device. Then the induced electrostatic force creates an attraction between the two electrodes and causes a displacement of the dielectric material. This movement can be used to create a non-magnetic linear actuator that behaves as a variable capacitor in electrical terms. One common issue for above-mentioned capacitive loads is that they require relatively high voltage to be operated [6]. In the case of photoflash and piezoelectric material applications, this voltage is in the range of hundred volts. However, in the case of DEAP actuators, the voltage level is in the multi-kV range (typically 2.5 kV) [7].

Flyback converters are widely used in a large variety of industrial and consumer applications, such as laptop chargers, mobile phone chargers, standby power supplies for computers and other low power (<250 W) switch mode power supplies (SMPSs). The success of the flyback topology is due to its simplicity, low component count and cost. In fact, flyback converters are also often used for achieving high step-up ratios. However, in low power high voltage applications, the converter design becomes challenging mostly due to parasitic elements and component stresses. In high voltage applications [8] one of the major factors that affects converter performance is the flyback transformer. The transformer leakage inductance causes significant stresses over the primary power semiconductors. In addition, the transformer end-to-end capacitance (or stray capacitance) becomes one of the main concerns for high voltage applications (>1 kV) [4][9][10]. This is mostly due to the large amount of energy that is stored in this stray capacitance at high voltages. Limiting the energy stored in this interwinding stray capacitance can significantly improve the converter performance in terms of efficiency as well as increasing the working voltage. One solution to achieve this is to have an optimized transformer winding

978-1-4799-2325-0/14/$31.00 ©2014 IEEE

configuration which results in a higher manufacturing cost. Besides, a small value of stray capacitance can be easily achieved by using a large core volume which would provide flexibility in the winding arrangement and in the selection of the wire diameter.

In this paper, in order to have a high voltage converter within a small converter volume, a new topology based on primary parallel secondary series flyback converter (PPSSFC) is presented. The new topology uses series and parallel connection of multiple transformers to achieve very high step-up ratio (up to 650) and low energy stored in the transformer output stray capacitance. A low-power high-voltage converter prototype has been designed for DEAP actuator (capacitive load) in heating valve applications. The converter is characterized by an input voltage of 3 V and an output voltage of 2 kV with a size of ~3.5x2.5 cm. Experimental results validate the proposed topology achieving a step-up ratio of ~650 times (from a 3 V battery up to 2 kV).

II. Proposed Topology: Primary Parallel Secondary Series Flyback Converter (PPSSFC)

It is challenging to achieve a low winding stray capacitance for a high voltage flyback transformer without applying complex winding configurations or without a highly optimized transformer design. This is especially true in the case of small transformers.

It is well known that capacitors series connection results in a smaller equivalent total capacitance. Based on this basic principle, the series connection of several transformer secondary windings is beneficial for reducing the equivalent secondary winding stray capacitance. In capacitive load charging applications, the energy stored in flyback transformer during each charging cycle can be used as criteria for evaluating the capacitive load charging capability. That means, the more energy the transformer can store, the higher output voltage the converter can achieve in the case of same winding stray capacitance. For this reason, the parallel connection instead of series connection for primary windings tends to be beneficial in increasing the transferable energy to the secondary side.

The primary in parallel secondary in series based flyback converter has been derived and depicted in Fig. 1. Assuming N transformers, each transformer has a secondary winding stray capacitance C_s, then the secondary equivalent stray capacitance (C_{seq}) can be obtained through (1), which results in a capacitance is reduced by a factor of N.

$$C_{seq} = \frac{C_s}{N} \tag{1}$$

Similarly, the total primary equivalent inductance (L_{prieq}) can be calculated through the following equation

$$L_{prieq} = N \cdot (L_{p\_m} + L_{p\_l}) \tag{2}$$

where L_{p_m} and L_{p_l} are the primary magnetizing inductance and the leakage inductance, respectively. Considering the same peak current as in the single transformer case, the energy stored in the PPSSFC configuration will be N times larger than the energy stored in only one transformer.

Minimizing the energy stored in the windings stray capacitance is extremely beneficial for high voltage applications. However, this advantage is reduced by the increased secondary series resistance. In fact, the windings series connection at the transformers secondary sides results in higher winding losses since the total secondary winding

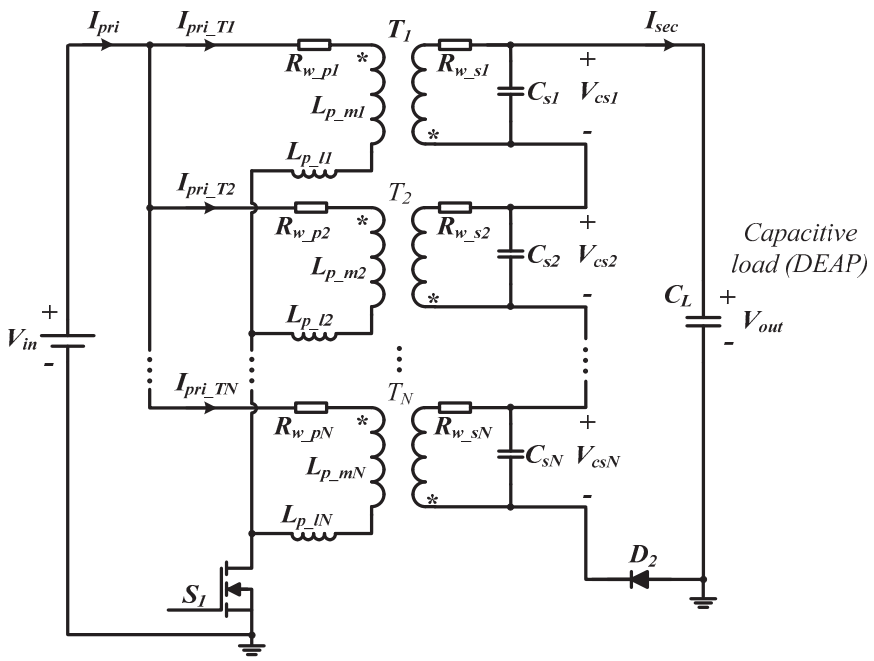


Fig 1. Circuit scheme of the proposed primary parallel secondary series flyback converter (PPSSFC) topology.

resistance ($R_{w\_s\_eq}$) is N times the single transformer secondary winding resistance (R_{w_s}), as in (3). Therefore, there will always be a trade-off between the energy stored in the output capacitance and the total secondary winding resistance.

$$R_{w\_s\_eq} = N \cdot R_{w\_s} \tag{3}$$

III. Operating Principles and Analysis

A. Assumption and General Information

In this investigation, the N-transformers are supposed to be identical. Possible mismatches of primary inductances due to parameters variation in the transformer production will cause different peak current in each transformer but, the secondary series connection forces the current in the transformers to be equal. Therefore, to simplify the analysis, the current in each transformer stage can be considered to be equal. Similarly, the mismatches of secondary stray capacitances will result in the unbalanced voltage sharing. The primary parallel connection forces the voltage over winding to be equal. For this reason, it is reasonable to assume that the voltage is balanced for the secondary windings.

Commonly, converters used in charging capacitive load applications stops working when the pre-set output voltage is reached and do not regulate the output voltage like in regular converters operating in steady state. In fact, the entire charging process consists of a series of consecutive charging cycles. In order to improve the charging efficiency, reduce the overall duration of the charging process and effectively limit the maximum flux density, the boundary mode control as well as primary peak current control methodology are the most suitable candidates and they have been widely employed in ongoing capacitive load charging applications [11-13]. Another advantage of these control modes is that it is possible to operate the converter in closed loop by using feedback from the converter primary side. This does not require a feedback loop that crosses the converter galvanic insulation barrier.

It is possible to analyze the working principle based on one charging cycle with the initial output voltage $V_{outInitial}$ due to the similarity in behavior for all charging cycles during the entire charging period. The behavior under high voltage condition represents the general case for the analysis. To some extent, the low voltage operation can be considered as a special case of high voltage operation. For these reasons, the high output voltage operation will be investigated in detail and the difference between high voltage and low voltage operation will be discussed briefly later.

B. Operation Modes Under High Output Voltage

The operation modes in one charging cycle under high output voltage condition can be expressed in four time intervals, presented on Fig. 2. And the corresponding critical operating waveforms are shown in the right side of Fig. 3.

Mode 1 [$t_0' \le t \le t_1'$: Fig. 2(a)]: At the beginning of this time interval, primary MOSFET S_1 is switched on. Due to the resonance between the secondary winding inductance and stray capacitance during the last operation mode [t_3' t_4'] of previous charging cycle, a negative minimum primary winding current is induced at time instant t_0', which can be roughly estimated through the following equation

$$I_{pri\_min} = -\sqrt{\frac{C_s}{L_{p\_m}+L_{p\_l}}} \cdot \frac{V_{outInitial}}{N} \tag{4}$$

where $V_{outInitial}$ not only represents the initial output voltage for the current charging cycle, but also stands for the final output voltage of previous cycle. C_s, L_{p_m} and L_{p_l} are the secondary winding stray capacitance, primary magnetizing inductance and primary leakage inductance for one transformer. N represent the total transformer number in the PPSSFC configuration.

In this operation mode the primary winding current increases from I_{pri_min} until it reaches the pre-set peak current I_{pri_p}. Considering the influence of the on-resistance of S_1 (R_{dson}), this current for each transformer I_{pri_T} can be expressed as

$$I_{pri\_T}(t) = \frac{V_{in}}{N \cdot R_{dson}} + \left(I_{pri\_min} - \frac{V_{in}}{N \cdot R_{dson}}\right) \cdot e^{-\frac{N \cdot R_{dson}}{L_{p\_m}+L_{p\_l}} \cdot (t-t_0')} \tag{5}$$

where V_{in} is the input voltage for the proposed converter.

Correspondingly, the on-time of S_1 can be calculated through the following equation

$$t_{0-1}' = -\left[\ln\left(\frac{I_{pri\_p} \cdot N \cdot R_{dson} - V_{in}}{I_{pri\_min} \cdot N \cdot R_{dson} - V_{in}}\right)\right] \cdot \frac{L_{p\_m}+L_{p\_l}}{N \cdot R_{dson}} \tag{6}$$

For this interval, neglecting the impact of winding resistances, the secondary winding voltage for each transformer can be expressed as

$$V_{cs}(t) = -(V_{in} - N \cdot I_{pri\_T}(t) \cdot R_{dson}) \cdot n_{ratio} \tag{7}$$

where n_{ratio} stands for the turns ratio for one transformer and it is equal to the secondary winding turns divided by the primary winding turns.

Mode 2 [$t_1' \le t \le t_2'$: Fig. 2(b)]: When S_1 is switched off at time t_1', the stored energy in the transformers cannot be transferred instantaneously to the capacitive load due to the influence of C_s. The voltage over C_s needs to build up until it reaches $V_{outInitial}/N$ before the current freewheeling period can start; this assumes that the voltage drop of freewheeling diode D_2 is negligible. The energy used for charging C_s comes from the energy stored in the transformers. This also means that the secondary peak current I_{sec_p} cannot be obtained through the direct reflection from I_{pri_p}, and can be approximately estimated by

$$I_{sec\_p} = \sqrt{\frac{{I_{pri\_p}}^2}{{n_{ratio}}^2} + \frac{C_s \cdot V_{cs}(t_1')^2}{{n_{ratio}}^2 \cdot L_{p\_m}} - \frac{C_s \cdot {V_{outInitial}}^2}{{n_{ratio}}^2 \cdot N^2 \cdot L_{p\_m}}} \tag{8}$$

where $V_{cs}(t_1')$ is the voltage over C_s at the time instant t_1'. In this time interval, the circuit is driven by the resonance between the secondary magnetizing inductance and C_s. The initial energy comes from the secondary peak current.

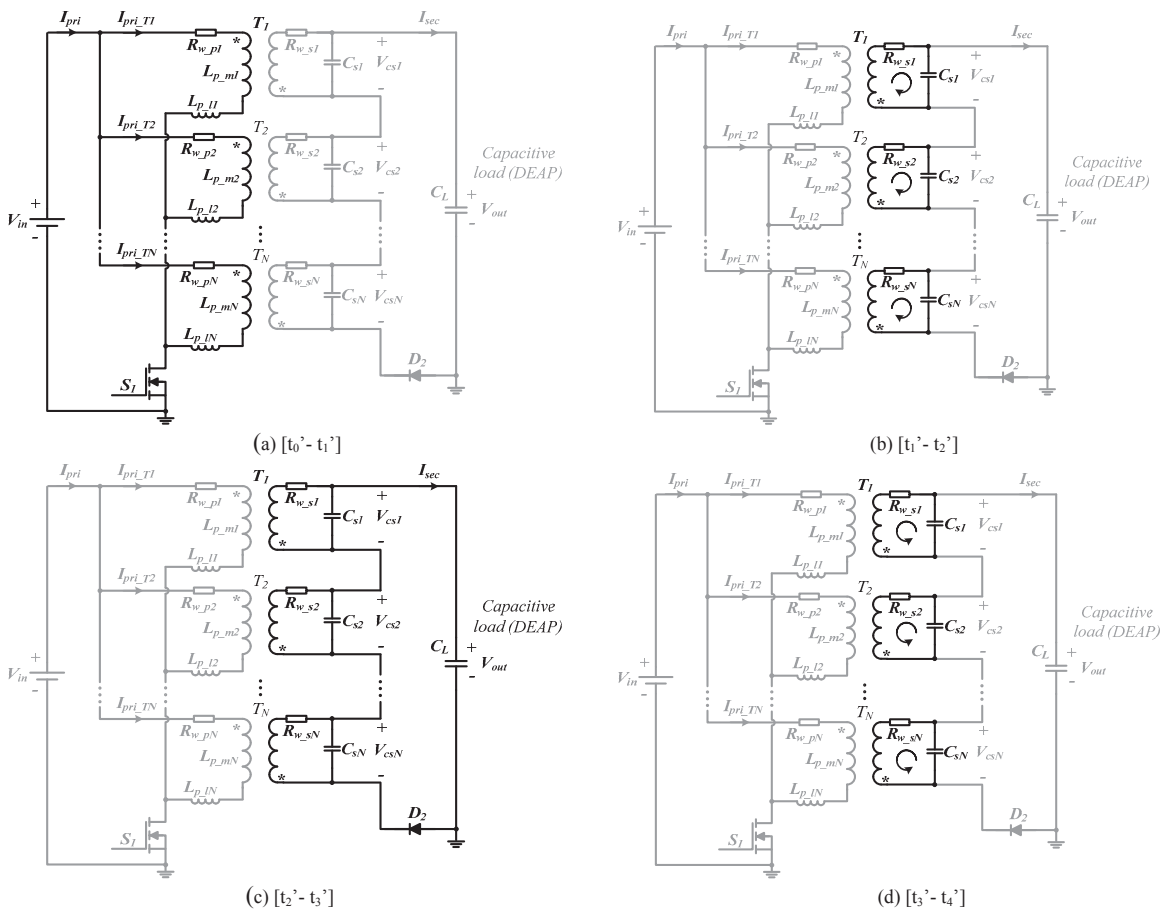


Fig. 2. Equivalent circuit schemes of the operation modes in PPSSFC under high output voltage condition.

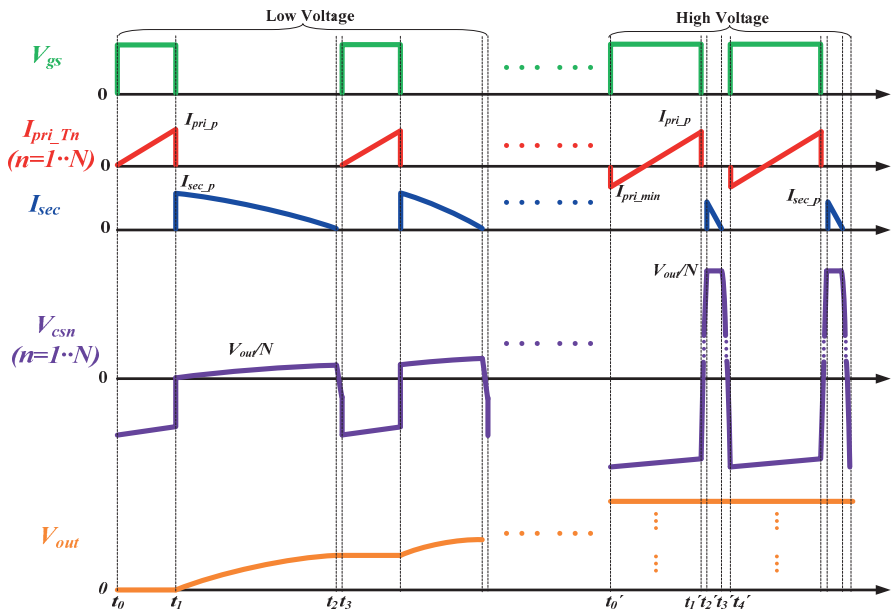


Fig 3. Converter critical operating waveforms at low voltage (left side) and at high voltage (right side).

Assuming negligible the influence of resistance and core losses, the voltage over C_s can be roughly estimated as in (9).

$$V_{cs}(t) = V_{cs}(t_1') \cdot \cos[\omega_r \cdot (t - t_1')] + I_{pri\_p} \cdot \sqrt{\frac{L_{p\_m}}{C_L}} \cdot \sin[\omega_r \cdot (t - t_1')] \quad (9)$$

where ω_f is the resonant angular frequency of secondary magnetizing inductance and C_s and can be calculated as

$$\omega_r = \frac{1}{n_{ratio} \cdot \sqrt{L_{p\_m} \cdot C_s}} \quad (10)$$

Mode 3 [$t_2' \le t \le t_3'$: Fig. 2(c)]: When V_{cs} reaches $V_{outInitial}/N$ at the time instant t_2', the secondary current freewheeling starts. If neglecting the impact of resistances in the secondary side and the voltage drop of D_2, the freewheeling current can be expressed as

$$I_{sec}(t) = I_{\sec\_p} \cdot \cos\left[\omega_f \cdot (t - t_2')\right] - \frac{V_{outInitial} \cdot C_L}{\omega_f} \cdot \sin\left[\omega_f \cdot (t - t_2')\right] \quad (11)$$

where C_L is the capacitance of the capacitive load and ω_f is the resonant angular frequency of secondary magnetizing inductance and C_L, which can be calculate by (12).

$$\omega_f = \frac{1}{n_{ratio} \cdot \sqrt{L_{p\_m} \cdot C_L}} \quad (12)$$

Correspondingly, output voltage for this time interval can be calculated as in (13).

$$V_{out}(t) = V_{outInitial} \cdot \cos\left[\omega_f \cdot (t - t_2')\right] + I_{\sec\_p} \cdot n_{ratio} \cdot \sqrt{\frac{L_{p\_m}}{C_L}} \cdot \sin\left[\omega_f \cdot (t - t_2')\right] \quad (13)$$

This time interval ends when $I_{sec}(t)$ reaches 0, then the duration time for this period can be calculated through

$$t_{2-3}' = \frac{1}{\omega_f} \cdot \left[\arctan\left(\frac{I_{sec\_p} \cdot \omega_f}{V_{outInitial} \cdot C_L}\right)\right] \quad (14)$$

Mode 4 [$t_3' \le t \le t_4'$: Fig. 2(d)]: After the secondary freewheeling current reaches 0 at the time t_3', due to the stored energy in C_s, the drain voltage of S_1 is still larger than V_{in}, based on the basic principle of boundary mode control, S_1 cannot be switched on at this time instant. In fact, similar to *Mode 2*, at this time interval the circuit is driven by the resonance between secondary magnetizing inductance and C_s however in this case, with the initial energy from C_s.

The voltage over C_s in this period can be calculated through

$$V_{cs}(t) = \frac{V_{out}(t_3')}{N} \cdot \cos[\omega_r \cdot (t - t_3')] \quad (15)$$

where $V_{out}(t_3')$ is the voltage over C_s at the time t_3'.

Neglecting the impact of the body diode in S_1, this time interval ends when V_{cs} reaches $-n_{ratio} \cdot V_{in}$, then the duration time can be calculated as

$$t_{3-4}' = \frac{1}{\omega_r} \cdot \left[\arccos\left(\frac{-n_{ratio} \cdot V_{in} \cdot N}{V_{out}(t_3')}\right)\right] \quad (16)$$

The presented analysis is simplified, a more detailed analysis of the time intervals is presented on [14].

C. Low Output Voltage Operation Discussion

At low output voltages, the key operating waveforms are presented in the left side of Fig. 3.

In *Mode 1*, the current starts from 0 and not from negative. This happens because of the small amount of energy stored in C_s at low output voltage, this is not sufficient to force the energy be transferred back to the primary creating a negative peak current.

In the case of low output voltage, the time used to charge C_s tends to be really short, therefore, the *Mode 2* does not need to be considered and the secondary peak current is the primary peak current divided by the transformer turns ratio, as illustrated in (17).

$$I_{sec\_p} = \frac{I_{pri\_p}}{n_{ratio}} \quad (17)$$

Furthermore, in *Mode 4*, at low output voltage, V_{cs} cannot reach $-n_{ratio} \cdot V_{in}$, the time interval can be estimated by half of the resonance period of secondary magnetizing inductance and C_s, shown in (18).

$$t_{2-3} = \frac{\pi}{\omega_r} \quad (18)$$

IV. PPSSFC Topology Discussion

A. Topology Advantages

Conventional flyback converters for high voltage capacitive charging applications require an optimized transformer design or large volume core in order to limit the secondary winding stray capacitance (C_s). As the converter output voltage (V_{out}) increases, the energy stored in the secondary stray capacitance ($E_{s,stray\ cap.}$) increases with the quadratic of the converter output voltage, shown in (19). This will limit the maximum achievable output voltage for the converter.

$$E_{s,stray\ cap.} = \frac{1}{2} \cdot C_s \cdot {V_{out}}^2 \quad (19)$$

The proposed topology is derived from a flyback topology by replacing the flyback transformer with two or more primary parallel secondary series connected transformers. In this case the converter output voltage is shared between the series connection of N secondary windings. This results that the energy stored in the winding stray capacitance is halved in case of $N = 2$, it is 1/3 in case of $N = 3$ and so on, as in equation

$$E_{s,stray\ cap.,PPSSFC} = N \cdot \frac{1}{2} \cdot C_s \cdot \left(\frac{V_{out}}{N}\right)^2 \quad (20)$$

where $E_{s,stray\ cap.,PPSSFC}$ stands for the total energy stored in the winding stray capacitances of N transformers. This characteristic greatly improves the charging ability of the converter.

Assuming an ideal flyback converter topology loss-less and without any parasitic elements, using peak current and boundary mode control schemes, the energy transferred by the flyback transformer in every charging cycle is constant, shown in (21).

$$E_{cycle} = \frac{1}{2} \cdot L_{p\_m} \cdot {I_{pri\_p}}^2 \quad (21)$$

Assuming a complete charging process for output voltage from 0 V up to V_{out}, the total energy required to charge the capacitive load is expressed as

$$E_{CL} = \frac{1}{2} \cdot C_L \cdot V_{out}{}^2 \tag{22}$$

Therefore, for a conventional flyback topology, the number of successive charging cycles, $N_{charging\ cycles}$, required to complete the entire charging process can be calculated as

$$N_{charging\ cycles} = \frac{C_L \cdot V_{out}{}^2}{L_{p\_m} \cdot I_{pri\_p}{}^2} \tag{23}$$

In the presented PPSSFC topology, assuming the primary current is maintained constant for each transformer, then in each charging cycle, the energy transferred by the flyback transformers increases by N times, as shown in (24).

$$E_{cycle\ PPSSFC} = \frac{1}{2} \cdot N \cdot L_{p\_m} \cdot I_{pri\_p}{}^2 \tag{24}$$

This eventually results that the PPSSFC topology requires N times less cycles for charging the capacitive load under same conditions, illustrated in (25).

$$N_{charging\ cycles\ PPSSFC} = \frac{C_L \cdot V_{out}{}^2}{N \cdot L_{p\_m} \cdot I_{pri\_p}{}^2} \tag{25}$$

Moreover, with PPSSFC configuration, the major advantages are that it is possible to achieve a high voltage converter within limited space and with a low price by employing small size off-the-shelf transformers. A large transformer with optimized for low stray capacitance can also be used to obtain high output voltage. This can normally be achieved by separating the windings in different sectors in a coil former or applying complex winding configurations, which will result in high transformer manufacturing cost. Small off-the-shelf transformers are not required to be highly optimized and therefore, they can be manufactured with very low cost. Besides, the PPSSFC with small transformers can provide higher flexibility in the PCB layout compared to the flyback configuration based on a single large transformer. This tends to be especially useful when converter power density optimization is required or large transformer cores are not available in the desired size.

B. Topology Disadvantages

Compared to one single transformer operated at the same peak current, like the transferrable energy stored in the transformer magnetizing inductance increases by N times, the non-transferrable energy stored in the leakage inductance will increase by N as well, illustrated in (26) and (27).

$$E_{leak} = \frac{1}{2} \cdot L_{p\_l} \cdot I_{pri\_p}{}^2 \tag{26}$$

$$E_{leak\ PPSSFC} = \frac{1}{2} \cdot N \cdot L_{p\_l} \cdot I_{pri\_p}{}^2 \tag{27}$$

where E_{leak} is the energy stored in the leakage inductance for one transformer, and E_{leak} represents the total leakage inductance energy in the PPSSFC configuration. The N times larger leakage inductance energy will bring much more pressure for the voltage stress of S_1. Fortunately, a variety of low-voltage power MOSFETs are available on the market. The impact of this disadvantage can be minimized by carefully calculating the voltage stress caused by the energy stored in the leakage inductance and selecting the power semiconductors with suitable voltage rating.

Assuming identical current sharing between all the transformers primary stages, the current through S_1 can be expressed as

$$I_{S1}(t) = N \cdot I_{pri\_T}(t) \tag{28}$$

This means the power MOSFET S_1 has higher current stress compared with one transformer case. However, low voltage MOSFETs are available with very low on-resistances and for these reasons, this disadvantage has very limited impact.

The series connection of the transformers on the high voltage side provides increased loss due to the series connection of the secondary winding resistances, which will, to some extent, limit the benefit from reducing stray capacitance. The increased number of components (transformers) is another disadvantage of the PPSSFC configuration.

V. Prototype Implementation

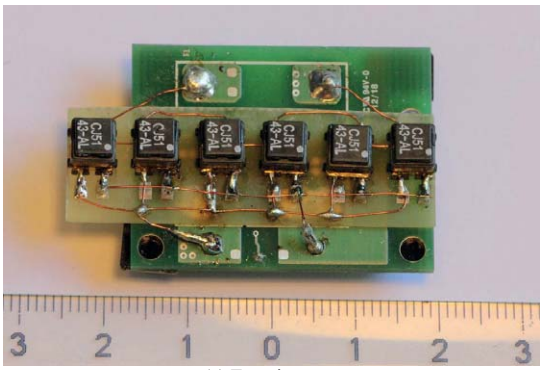
In order to validate the proposed topology, a small size prototype with the ability to charge the capacitive load to a high voltage has been implemented, as shown in Fig. 4 (a) and (b). An off-the-shelf flyback transformer CJ5143-AL from Coilcraft is employed in this prototype [15]. The critical parameters for the converter, capacitive load as well as the flyback transformer are summarized in Table I. Peak current as well as boundary mode control schemes are implemented by the capacitor charger controller LT3750 from Linear Technology [13]. An optimized design and layout can furthermore reduce the converter volume.

VI. Experimental Results

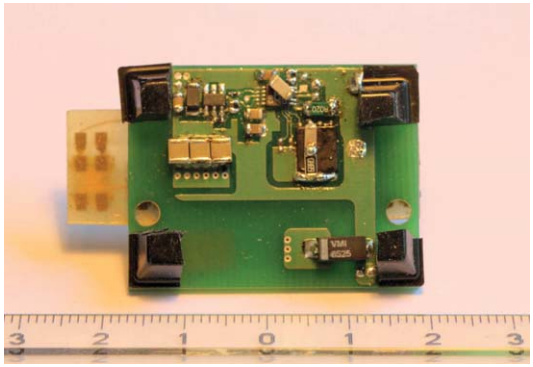
The experiments have been carried out to verify the proposed topology as well as the implementation of the prototype. The overall charging process for a 220 nF capacitive load is shown in Fig. 5. The maximum output voltage (2 kV) is achieved through a 3 V input voltage within 400 ms continuous charging time.

TABLE I.
Parameters of PPSSFC Prototype, DEAP Actuator and Flyback Transformer

Parameters	*Values*
V_{in}	3 V
Maximum V_{out}	2 kV
Transfomer number	6
Converter size	3.5x2.5 cm
C_L	220 nF
n_{ratio}	15
L_{p_m}	15 µH
L_{p_l}	250 nH
C_s	18.5 pF
R_{w_p}	1 Ω
R_{w_s}	25 Ω
I_{pri_p}	1.2 A



(a) Top view



(b) Bottom view

Fig. 4. Converter prototype (reference scale in cm).

The detailed operating waveforms for three successive charging cycles at low voltage are shown in Fig. 6 (a) and (b), including both current and voltage waveforms. From the primary winding currents in transformer T_1 and T_6, it can be seen that good current sharing between transformers is achieved. Moreover, it also can be observed that the peak current and the boundary mode control are achieved. At low output voltage, the resonance current at the beginning of each switching cycle is caused by the primary leakage inductance and secondary winding stray capacitance. Due to the impact of parasitic capacitors in the secondary side, it is difficult to measure the real voltage waveform over C_s for one of the transformers. Instead, the overall transformers secondary voltage is measured. These voltage waveforms are presented on Fig. 6 (b), where the three operation modes at low output voltage can be observed.

In a similar way, the experimental waveforms for three charging cycles at high voltage operation are shown on Fig. 7. The realization of current sharing between transformers can be confirmed through the winding current waveforms in Fig. 7 (a). Moreover, at the beginning of each charging cycle a negative current spike can be observed. This was mentioned in the analysis and it is also verified in the current waveforms. At high output voltage, a resonance is observed at the beginning of every switching cycle due to the secondary winding leakage inductance and secondary winding stray capacitance. In the voltage waveforms on Fig. 7 (b), the charging of the intra winding capacitance C_s can be observed.

The experimental results verify that the converter prototype operates accordingly to the analysis performed in the previous section.

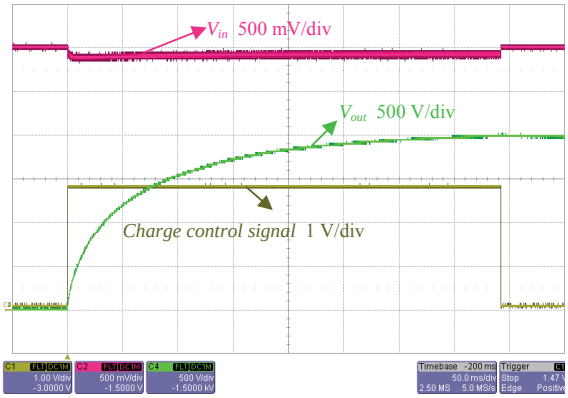
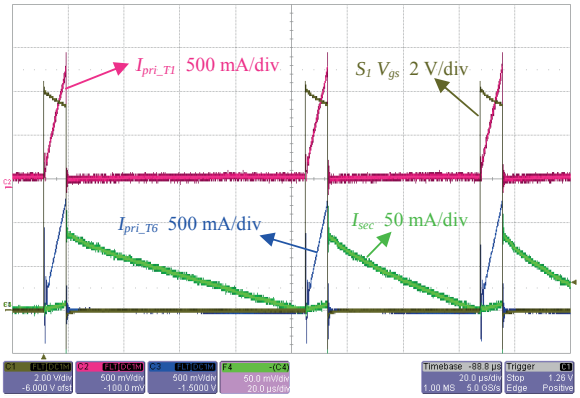
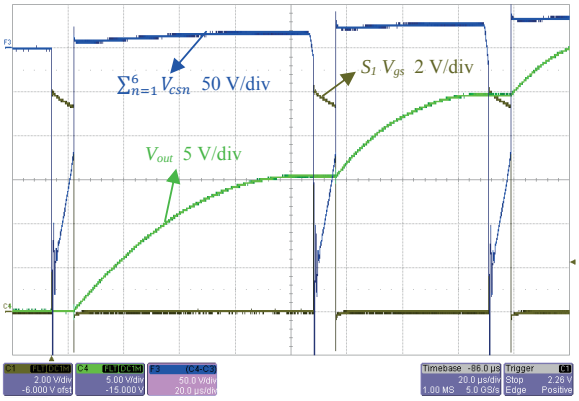


Fig. 5. Overall experimental waveform for the entire charging process.

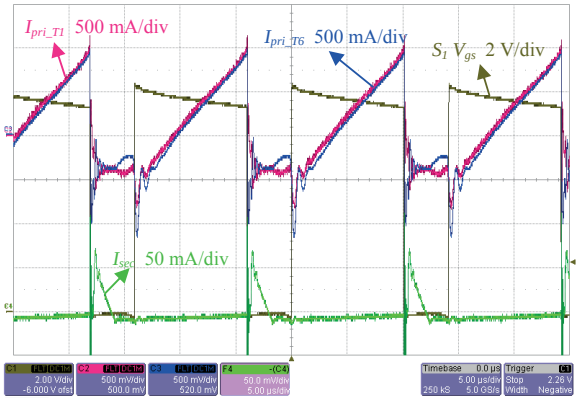


(a) Current waveforms

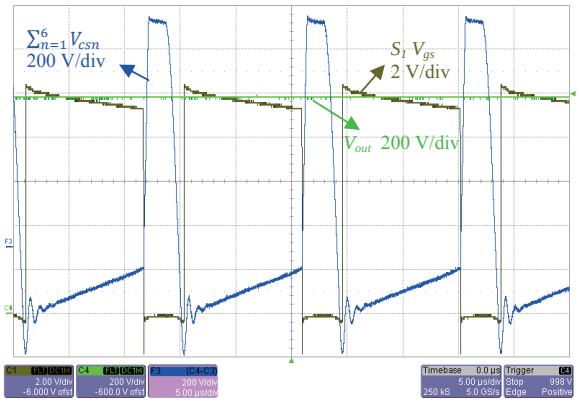


(b) Voltage waveforms

Fig. 6. Detailed experimental waveforms for charging cycles at low output voltage.



(a) Current waveforms



(b) Voltage waveforms

Fig. 7. Detailed experimental waveforms for charging cycles at high output voltage.

VII. Conclusions

The paper presents a primary parallel secondary series flyback converter (PPSSFC). The new topology is derived from the conventional flyback converter and uses multiple transformers to mitigate the effects of the secondary stray capacitance. The topology is very suitable for applications which require very large step-up ratios, low end-to-end capacitance and high output voltage within limited space.

The operating principles and switching cycle based analysis are presented for both high and low voltage operation. The advantages and disadvantages for the proposed topology are discussed in terms of energy stored in the secondary stray capacitance, transferrable and non-transferrable energy stored in the flyback transformers as well as the voltage and current stress for semiconductor components. Compared to a single large transformer case, the proposed topology can be beneficial for reducing the transformer winding complexity and for providing high flexibility in PCB layout.

The proposed PPSSFC topology has been verified on a converter for a DEAP actuator (capacitive load). The PPSSFC achieved very high step-up ratio (650x) and high voltage operation (2 kV) and it is based on six off-the-shelf transformers. It is observed that the switching cycle based operating analysis of the proposed converter is exactly validated by the experimental results.

References

[1] Sokal, N.O.; Redl, R., "Control algorithms and circuit designs for optimal flyback-charging of an energy-storage capacitor (e.g., for flash lamp or defibrillator)," IEEE Transactions on Power Electronics, vol.12, no.5, pp.885-894, Sep 1997.

[2] Das-Gupta, D.K.; Doughty, K., "Electro-Active Polymers in Non-Destructive Dielectric Evaluation," IEEE Transactions on Electrical Insulation, vol.EI-20, no.1, pp.20,28, Feb. 1985.

[3] Shankar, Ravi, Tushar K. Ghosh, and Richard J. Spontak. "Dielectric elastomers as next-generation polymeric actuators." Soft Matter 3.9 (2007): 1116-1129.

[4] D. Campolo, M. Sitti, and R. S. Fearing, "Efficient charge recovery method for driving piezoelectric actuators with quasi-square waves," IEEE Transactions on Ultrasonics, Ferroelectrics and Frequency Control, vol. 50, pp. 237-244, 2003.

[5] R. Sarban, B. Lassen, and M. Willatzen, "Dynamic Electromechanical Modeling of Dielectric Elastomer Actuators With Metallic Electrodes," IEEE/ASME Transactions on Mechatronics, vol. 17, pp. 960-967, 2012.

[6] Eitzen, L.; Graf, C.; Maas, J., "Cascaded bidirectional flyback converter driving DEAP transducers," IECON 2011 - 37th Annual Conference on IEEE Industrial Electronics Society, pp.1226-1231, 7-10 Nov. 2011.

[7] L. Huang, Z. Zhang, and M. A. E. Andersen, "A review of high voltage drive amplifiers for capacitive actuators," in 47th International Universities Power Engineering Conference (UPEC), 2012, pp. 1-6.

[8] S.E. Thomas; C. W. Tipton, and D. Porschet, "Fabrication and Practical Considerations of a Flyback Transformer for Use in High Pulsed-Power Applications,", Thirty-Eighth Southeastern Symposium on System Theory (SSST), 2006, pp.406-409.

[9] S.-K. Chung, "Transient characteristics of high-voltage flyback transformer operating in discontinuous conduction mode," IEEE Proceedings - Electric Power Applications, vol. 151, pp. 628-634, 2004.

[10] Dalessandro, L.; da Silveira Cavalcante, F. and Kolar, J. "Self-Capacitance of High-Voltage Transformers," IEEE Transactions on Power Electronics, vol.22, no.5, pp.2081-2092, Sep. 2007.

[11] Sokal, N.O.; Redl, R., "Control algorithms and circuit designs for optimally flyback-charging an energy-storage capacitor (e.g. for a flash lamp)," Fifth Annual Applied Power Electronics Conference and Exposition, APEC '90 Conference Proceedings, pp.295-302, 11-16 March 1990.

[12] Wong, K., "Energy-Efficient Peak-Current State-Machine Control With a Peak Power Mode," IEEE Transactions on Power Electronics, vol.24, no.2, pp.489-498, Feb. 2009.

[13] "LT3750 Capacitor Charger Controller Datasheet," Linear Technology Corporation, USA.

[14] L. Huang, Z. Zhang, and M. A. E. Andersen, " Detailed Behavior Analysis for High Voltage Bidirectional Flyback Converter Driving DEAP Actuator," IECON 2013 - 39th Annual Conference on IEEE Industrial Electronics Society, pp.623-628, Nov. 2013.

[15] "CJ5143-AL flyback transformer datasheet", Coilcraft Incorporated, USA.

Appendix P

Design Comparison of Autonomous High Voltage Driving System for DEAP Actuator

IEEE International Power Electronics and Applications Conference and Exposition (PEAC 2014)

Design Comparison of Autonomous High Voltage Driving System for DEAP Actuator

Lina Huang, Riccardo Pittini, Zhe Zhang and Michael A. E. Andersen
Department of Electrical Engineering
Technical University of Denmark
Oersteds Plads, Building 349, Kgs. Lyngby, Denmark
Email: huang@elektro.dtu.dk, ripit@elektro.dtu.dk, zz@elektro.dtu.dk, ma@elektro.dtu.dk

***Abstract*—As a new type of smart material, the Dielectric Electro Active Polymer (DEAP) is introduced in terms of configuration, working principle and potential applications. The design of autonomous high voltage driving system for DEAP actuator is investigated. The system configuration and the design methodology of high voltage converter are discussed in detail. Based on the heating valve application, three different high voltage converter solutions have been proposed. Different proposals have been compared in terms of energy loss, volume and cost. Finally, the design selection suggestions are provided to be a reference for the future designers.**

Keywords—high voltage; driving system; DEAP actuator; autonomous; design comparison

I. Introduction

With the advancement of material science, recently, a new kind of smart material, called DEAP (Dielectric Electro Active Polymer) material, increasingly arouses concerns from academia and industry [1-2]. The chemists and material scientists are focusing on improving the performance of the material. Mechanical researchers are investigating possible configurations based on the material as well as the various application occasions. Mathematicians are making effort to establish the math model for DEAP and to build the simulation toolbox. In order to properly utilize the DEAP material, electrical researchers are trying to design and develop highly efficient, small size and low cost electronics circuits.

DEAP material has similar structure to that of the capacitor – the soft dielectric silicone polymer is placed between the compliant electrodes. In most operation cases, the material can be considered with purely capacitive property. When voltage difference is applied on the conducting plates, according to Coulomb's law, a certain amount of electrostatic force is induced, which compresses the flexible insulation layer in thickness direction and expands the size of the polymer. The basic configuration and the working principle are illustrated in Fig. 1. According to this characteristic, DEAP material can be utilized to form an actuator [3]. In addition, when the material is stretched, the capacitance changes accordingly, which enables the material to be a sensor. Furthermore, by using the reverse energy conversion of actuation, the material can be used to constitute a generator, which can transform the mechanical energy to electrical energy.

When applying DEAP based actuator, compared to its conventional counterparts, such as the hydraulic, pneumatic and electromagnetic actuators, it is much lighter and with noise free operation as well as faster electromechanical response speed [4]. This kind of actuator is especially suitable for the weight and noise sensitive applications, such as the aerospace, automobile industry and dwelling space.

In order to design and develop feasible DEAP actuation system, especially in the autonomous applications, not only the compact DEAP actuator is needed, the highly efficient, small size and low cost driving system for the actuator is required as well. The recent research progress of the material indicates, for the current version of DEAP material, the voltage to fully elongate the actuator needs reach 2 kV. A high output voltage converter with high efficiency, compact size and low cost design, therefore, needs to be investigated. These general requirements for power electronics converters, however, are normally contradictory. In general, it is impossible to achieve the small volume converter with lowest cost and highest efficiency. The trade-off evaluation needs to be carried out in order to achieve the optimum design. The high driving voltage and the capacitive load property make the design methodology of DEAP actuator driving converter diverse from that of the conventional low output voltage steady-state operation converters.

In this paper, the autonomous driving system and the high voltage converter design are discussed. Different design solutions are proposed for a specific application. The solutions are compared in terms of energy consumption, volume and cost to summarize the design selection suggestions for future use.

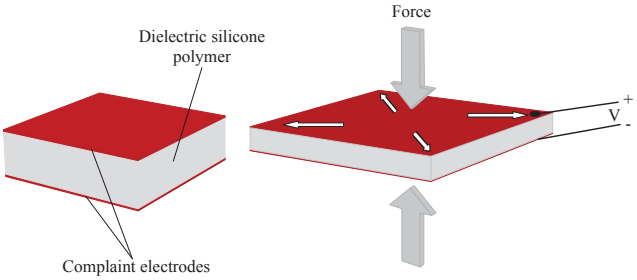


Fig. 1. Basic structure of DEAP material and the illustration of its fundamental working principle.

978-1-4799-6768-1/14/$31.00 ©2014 IEEE

II. Autonomous High Voltage Capacitive Actuator Driving System Design Metholodogy Discussion

A. System Configuration

The autonomous high voltage DEAP actuator driving system consists of five major parts: the power source, the high voltage converter, DEAP actuator, terminal mechanical load and the system level sensing and control unit. Considering different terminal application cases, the entire driving system is depicted in Fig. 2.

In autonomous situation, battery normally tends to be the only energy source. The capacitive property of the actuator and the low electrical energy to mechanical work transformation efficiency result in that most effective energy is stored in the actuator [5]. In such case, the introduction of the energy recovery technique is beneficial in improving the energy utilization on the system level. In order to deal with the recycled energy in a highly dynamic condition and to stabilize the input voltage for the high voltage converter, a dynamic energy storage element, such as super capacitor, need to be employed.

High voltage DC-DC converter transforms the low voltage from the power source to high output voltage in order to drive the DEAP actuator. The converter consists of three parts: the power stage to provide the energy path, the control stage to generate the PWM signal and realize the inner current loop control and the auxiliary power supplies to provide power for the ICs employed in the control stage.

As an electromechanical device, DEAP actuator transform the electrical energy from high voltage converter to mechanical force in order to actuate the terminal mechanical load, such as the aircraft wind flap, automotive mirror or indoor heating valve, etc. The connection between high voltage converter and actuator is electrical, while actuator and mechanical load are mechanically coupled.

The ultimate goal of the system is to regulate the terminal control parameter, such as the displacement, rotation angle or temperature according to the requirement. To achieve this goal, the feedback control of terminal parameter needs to be implemented with the help of corresponding sensors. Alternatively, if the relationship between the terminal control parameter and the output voltage of high voltage converter is known, and the terminal parameter cannot easily be obtained, with the help of high voltage sensing circuit, the output voltage closed loop control can be employed to replace the terminal parameter based feedback control. The measurement of high voltage normally consumes large amount of energy and is not desired in the autonomous system with limited energy resource. If the output voltage has the relationship with other parameter, such as the charging time considering the capacitive property of actuator, the other parameter based open loop control can be beneficial for saving energy.

In this paper, the attention will be focused on the critical electrical part in this entire electromechanical coupling system, i.e. the high voltage DC-DC converter.

B. High Voltage Converter Design Discussion

Traditionally, flyback converter has been employed to achieve high output voltage and high step-up ratio. Recently, with the penetration of piezoelectric technology, the piezoelectric transformer (PT) based converter tends to be another option in the field of low power high voltage generation. Even though, for the same output voltage level, PT can be much smaller than the traditional flyback transformer, the extra space and cost for more active semiconductor devices and the complex control circuits in the PT based solution make the flyback topology to be a more reasonable choice in the current stage of product development.

1) High voltage flyback topology discussion

As aforementioned, the energy recovery technique can be applied to improve the overall efficiency. Shown in Fig. 3 a),

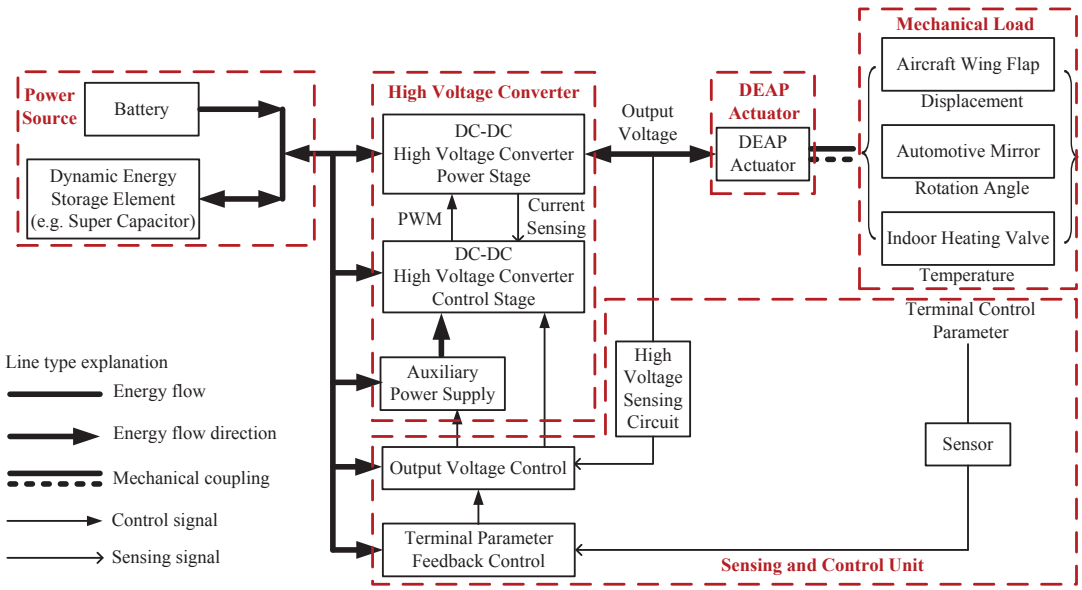
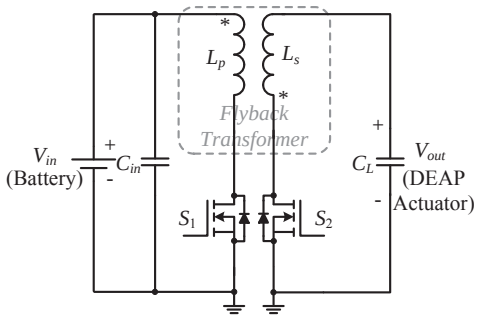


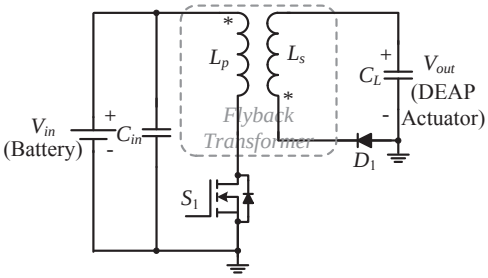
Fig. 2. System level configuration of autonomous high voltage DEAP actuator driving system with terminal loads.

the traditional bidirectional flyback topology which can provide the path for the energy flow back and forth, therefore, can be one option for the power stage in the high voltage converter. However, the active semiconductor component in the secondary side and the control circuits to realize the energy recovery introduce extra cost, space occupation and energy consumption. The unidirectional flyback topology, shown in Fig. 3 b), therefore, tends to be another option in some cases.

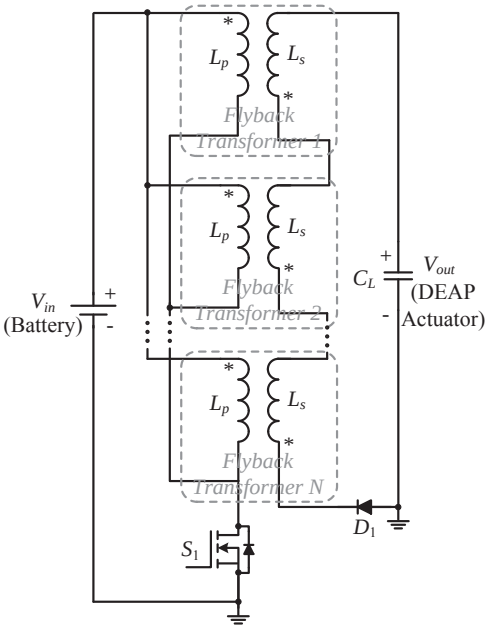
The large number of winding in the high voltage transformer leads to high self-capacitance of the winding [6].



a) Bidirectional flyback topology



b) Unidirectional flyback topology



c) Primary parallel secondary series flyback topology

Fig 3. High voltage converter topologies.

In the capacitive load charging application, the high winding stray capacitance results in lower achievable output voltage, longer charging time as well as the lower charging efficiency. One possible solution to weaken the influence of this capacitance is proposed, i.e. the multiple flyback transformer based topology with primary windings in parallel and secondary windings in series, shown in Fig. 3 c) [7]. If the self-capacitance of secondary winding for one transformer is denoted as C_s, the equivalent secondary side stray capacitance of N transformer based configuration can be calculated as

$$C_{seq} = \frac{C_s}{N} \tag{1}$$

In addition, this structure can provide more flexibility in space utilization if small size flyback transformer is applied compared to one single transformer based configuration.

The high output voltage and the capacitive feature of the actuator load limits the utilization of the commercial flyback transformer. As the most critical part in the power stage, the high voltage flyback transformer, therefore, needs to be designed and implemented on one's own. The detailed design methodology and the practical skills to implement the transformer can refer to [8]. Compared to single transformer structure, the lower secondary side winding voltage of each transformer in multiple transformers based configuration enable the adoption of the small size commercial flyback transformer. The parallel configuration in the primary side can guarantee the equal voltage sharing over secondary windings. If the output voltage is denoted as V_{out}, the voltage over the secondary winding of each transformer is expressed as

$$V_{sw} = \frac{V_{out}}{N} \tag{2}$$

2) High voltage flyback converter control strategy discussion

In capacitive load charging application, the flyback based configuration has simple working principle. In each switching cycle, when primary active semiconductor is turned on, the electrical field energy is transferred to the magnetic field energy and stored in the flyback transformer. When the primary MOSFET is turned off, the stored magnetic energy is automatically released to the capacitive load through the freewheeling diode in the secondary side, which corresponds to the increase of the output voltage. The successive switching cycles leads to the accumulation of the output voltage until it reaches the preset value. If energy recovery technique is employed, the same working concept is applied to the discharging process of capacitive load, which corresponds to the release of the actuator.

With the help of current sensing circuits, the current closed loop control can be implemented to generate PWM signals for driving the MOSFETs in the power stage. Compared to the average current control, the peak current control is more suitable due to its quick response and cycle-by-cycle current limit to avoid the saturation of magnetic core.

In each switching cycle, in order to achieve the complete transfer of the stored energy in flyback transformer to capacitive actuator, the current Discontinuous Conduction Mode (DCM) or Boundary Conduction Mode (BCM) needs to

be adopted. Some commercial ICs with the BCM or DCM function can be directly applied in the control stage of the high voltage converter.

3) Auxiliary power supplies

For high input voltage and fixed low output voltage DC-DC converter, normally, the auxiliary power comes from the output voltage instead of input voltage to achieve lower power loss. This strategy, however, cannot be applied for high output voltage converter with capacitive load, since the output voltage is high and variable. In this case, the switching power supply based commercial ICs, which can directly be powered by the battery, tends to be good candidates in terms of size and efficiency.

III. Case Study and Design Solutions Comparison

In an indoor heating valve application, a 3 V battery powered autonomous high voltage DEAP actuator driving system needs to be investigated. The design specifications of high voltage converter are summarized in Table I.

A. Power Stage

The high voltage topologies shown in Fig. 3 can lead to three different solutions for the autonomous high voltage DEAP actuator driving system: solution 1 can be the system with bidirectional flyback topology; solution 2 corresponds to the traditional single transformer based unidirectional flyback topology as the power processing stage; solution 3 is the multiple flyback transformers toplogy based driving system. Solution 1 is with intrinsic discharging ability to release the energy stored in DEAP actuator when it is needed. Solution 2 and 3, however, need extra discharging circuits to realize the controllable energy release for the actuator. The circuits can be formed by the series connection of the high voltage resistors and active high voltage MOSFET and are connected to the actuator in parallel. When the MOSFET is triggered on, the energy in actuator can be discharged through the high voltage resistors.

Concerning the critical flyback transformer design, solution 1 and 2 can share the same design and implementation. The detailed design and implemented parameters can refer to [8]. 6 small size commercial flyback transformers CJ5143 from Coilcraft are adopted in solution 3. The detailed transformer parameters can refer to [9].

B. Control Stage

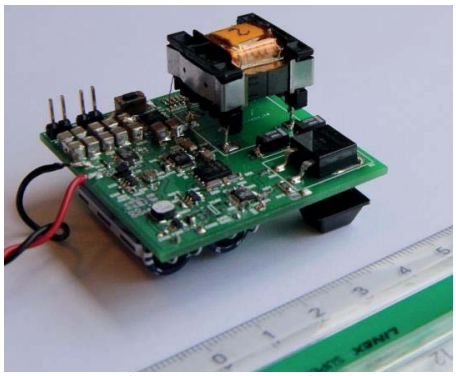
As stated before, the terminal parameter feedback control can be employed to regulate the terminal control parameter. The output voltage closed loop control can also be utilized to indirectly regulate the terminal parameter. However, this approach tends to be inefficient in terms of energy utilization.

TABLE I. High Voltage Converer Design Specifications

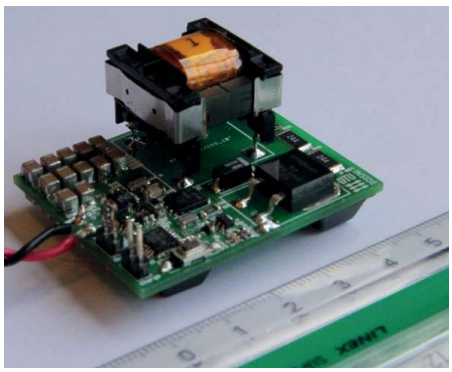
Parameters	Specifications
Input voltage	3 V
Maximum output voltage	1.8 kV - 2 kV
Capacitance of DEAP actuator	200 nF
Maximum continuous charging / discharging time	5 s

System level burst mode control, therefore, is proposed to save energy as well as to directly regulate the terminal control parameter.

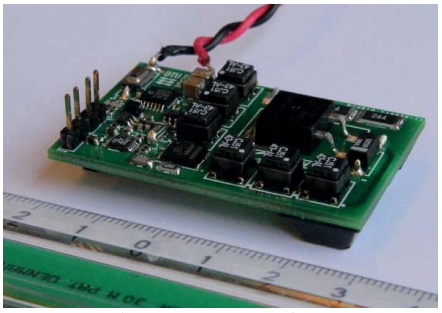
In burst control mode, the terminal parameter tends to be sensed at regular intervals instead of continuously. The output voltage closed loop control is absent in order to save energy and improve overall energy efficiency. Instead, the high voltage converter only works when there are trigger commands from the terminal parameter closed loop control. When the charging trigger signal is captured, the high voltage converter starts to charge the actuator until the output voltage reaches the preset voltage. Then the entire driving system shuts down to save energy. In the same way, the converter needs to discharge the actuator to 0 V when the discharging trigger signal is captured. Then the whole system goes to sleep mode again until the arrival of next trigger signal. This strategy is



a) Solution 1 prototype (50mm×50mm×32mm)



b) Solution 2 prototype (50mm×40mm×20mm)



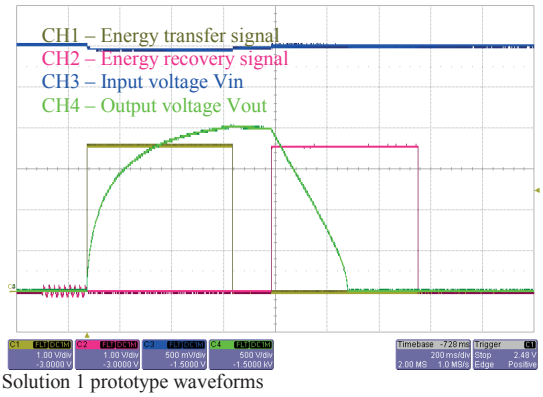
c) Solution 3 prototype (50mm×30mm×6mm)

Fig 4. High voltage converter prototypes.

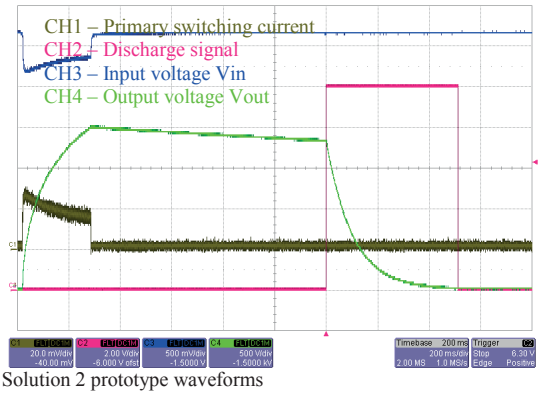
especially beneficial for heating valve application, since temperature control system is normally with large inertia constant and does not need to regulate so frequently.

C. High Voltage Converter Implementation

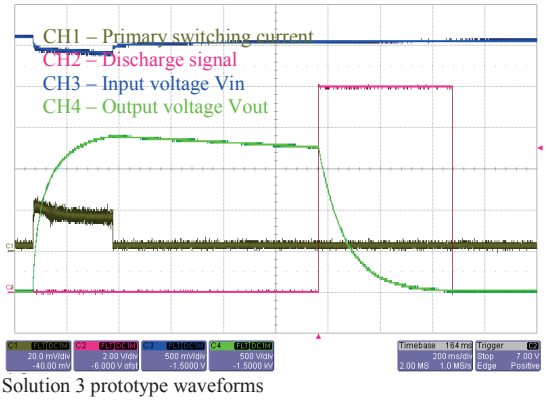
Corresponding to three different solutions mentioned above, three prototypes have been implemented and the pictures are shown in Fig. 4 a) b) and c), respectively. In addition, the converter dimensions are indicated in the figure caption. The functionality of each solution has been experimentally verified and the experimental waveforms are shown in Fig. 5 a) b) and c), respectively.



a) Solution 1 prototype waveforms



b) Solution 2 prototype waveforms



c) Solution 3 prototype waveforms

Fig. 5. Experimental waveforms of prototypes.

D. Aquasition of Critical Evaluation Parameters

In order to evaluate the performance of different solutions, some critical assessment indicators need to be obtained experimentally. One important indicator tends to be the efficiency of the power stage in high voltage converter. The capacitive property of the actuator calls for the energy efficiency rather than the power efficiency for the converter powering resistive load. In this case, for charging process, the energy efficiency is defined as the final stored energy in the actuator (E_{stored}) divided by the total input energy to the converter (E_{in}) and is expressed as

$$\eta_{charge} = \frac{E_{stored}}{E_{in}} \tag{3}$$

Likewise, for bidirectional topology, the discharge efficiency is defined as the total recovered energy ($E_{recovered}$) divided by the energy stored in the actuator

$$\eta_{discharge} = \frac{E_{recovreed}}{E_{stored}} \tag{4}$$

The measured efficiency for different solutions is shown in Fig. 6. Since solution 1 and 2 share the same high voltage transformer and have used the same components in the power stage, the charging efficiency of these two solutions tends to be equal. In addition, the charging and discharging time used to evaluate the energy loss of auxiliary power supplies as well as the maximum achievable voltage are another two critical evaluation parameters, which can be obtained from the waveforms in Fig. 5 and are summarized in Table II.

E. High Voltage Converter Comparison

For battery operated autonomous system, one of the primary concerns tends to be the battery life time. This parameter can be evaluated through calculating the energy consumption of the high voltage converter. The efficiency data, charging and discharging time and maximum output voltage

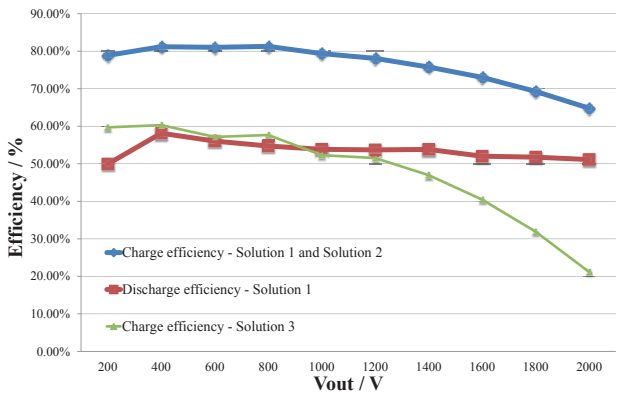
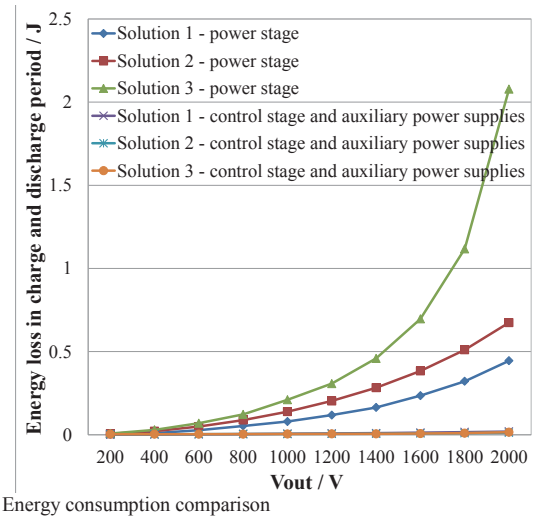


Fig. 6. Measured efficiency of three solutions.

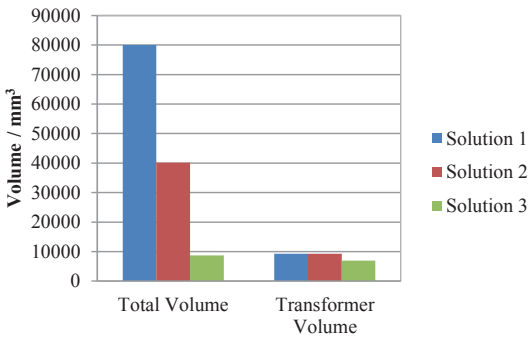
TABLE II. CHARGING AND DISCHARGING TIME AND MAXIMUM OUTPUT VOLTAGE OF HIGH VOLTAGE CONVERER

Solutions	Charging Time / ms	Discharging Time / ms	Maximum Voltage / kV
Solution 1	500	300	2
Solution 2	300	500	2
Solution 3	300	500	1.9

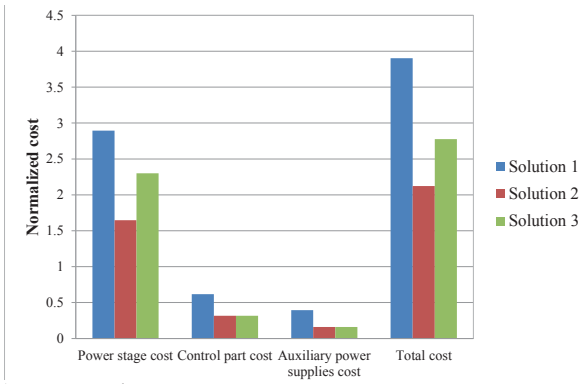
can be applied to obtain the total energy loss for the entire charging and discharging period. The energy consumption comparison of 3 solutions is shown in Fig. 7 a), which indicates that energy dissipated in the control stage and auxiliary power supplies can be neglected when compared to the energy dissipation in the power stage, and this is mainly due to the employment of the system level burst mode control. The curves of power stage for solution 1 and 2 can prove that if the battery life time is the concern with highest priority, the energy recovery technique is worthy to be implemented.



a) Energy consumption comparison



b) Volume comparison



c) Cost comparison

Fig. 7. Implemented prototypes comparison.

In order to achieve high power density, low volume power converter is desired. The volume comparison for 3 three solutions is shown in Fig. 7 b). Combining the energy loss information in Fig. 7 a), it can be concluded that the volume reduction corresponds to the increases of the energy loss in the power stage. This phenomenon becomes more and more severe with the increase of the output voltage. Fig. 7 b) also indicates that if volume distribution can be practically implemented, such as replacing the large single transformer with several small independent transformers, it will be greatly beneficial for the reduction of the total volume.

The cost comparison of different solutions is illustrated in Fig. 7 c), which indicates that the cost of the power stage dominates the cost of the entire high voltage converter, since normally high voltage semiconductor devices tend to be more expensive compared to other components. With the advancement of the material, if the driving voltage can be decreased, the expenses to build the corresponding driving system will decrease dramatically.

IV. Conclusion

In this paper, the structure, working principle and application fields of the DEAP material are introduced first. The design of the autonomous high voltage driving system for DEAP actuator is discussed in detailed, especially the most critical part in the system, i.e. high voltage converter. The investigation of autonomous system for heating valve application has been carried out and three possible solutions have been proposed. The different solutions are compared in terms of energy consumption, volume and cost. The design selection suggestions are provided to be a reference for the future designers to achieve optimum design.

References

[1] R. Sarban, B. Lassen, and M. Willatzen, "Dynamic Electromechanical Modeling of Dielectric Elastomer Actuators With Metallic Electrodes," *IEEE/ASME Transactions on Mechatronics*, vol. 17, pp. 960-967, 2012.

[2] L. Huang, L.; P. Thummala, Z. Zhang, and M. A. E. Andersen, "A.Battery powered high output voltage bidirectional flyback converter for cylindrical DEAP actuator," in *IEEE International Power Modulator and High Voltage Conference (IPMHVC)*, 2012, pp. 454-457.

[3] M. J. Tryson; R. Sarban, and K. P. Lorenzen, "The dynamic properties of tubular DEAP actuators," in *Proceedings of SPIE*, vol. 7642, 2010.

[4] R. Sarban, and R. W. Jones, "Physical model-based active vibration control using a dielectric elastomer actuator," *Journal of Intelligent Material Systems and Structures*, vol. 23, pp. 473-483, 2012.

[5] M. J. Tryson; R. Sarban, and K. P. Lorenzen, "The dynamic properties of tubular DEAP actuators," in *Proceedings of SPIE*, vol. 7642, 2010.

[6] L. Dalessandro, F. da Silveira Cavalcante, and J. Kolar, "Self-Capacitance of High-Voltage Transformers," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 2081-2092, 2007.

[7] R. Pittini, L. Huang, Z. Zhang, and M. A. E. Andersen, "Primary Parallel Secondary Series Flyback Converter (PPSSFC) with Multiple Transformers for Very High Step-Up Ratio in Capacitive Load Charging Applications," in *IEEE 2014 Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 1440-1447.

[8] L. Huang, Z. Zhang, and M. A. E. Andersen, "Design and Development of Autonomous High VoltageDriving System for DEAP Actuator in Radiator Thermostat," in *IEEE 2014 Applied Power Electronics Conference and Exposition (APEC)*, 2014, pp. 1633-1640.

[9] "CJ5143 flyback transformer datasheet", *Coilcraft, Inc.*, USA.

Appendix Q

An Interface Board for Developing Control Loops in Power Electronics Based on Microcontrollers and DSPs Cores – Arduino, ChipKit, dsPIC, DSP, TI Piccolo

14th *IEEE Workshop on Control and Modeling for Power Electronics (COMPEL 2014)*

An Interface Board for Developing Control Loops in Power Electronics Based on Microcontrollers and DSPs Cores –Arduino /ChipKit /dsPIC /DSP /TI Piccolo

Riccardo Pittini
Dept. of Electrical Engineering
Technical University of Denmark
2800 Kgs. Lyngby, Denmark
ripit@elektro.dtu.dk

Zhe Zhang
Dept. of Electrical Engineering
Technical University of Denmark
2800 Kgs. Lyngby, Denmark
zz@elektro.dtu.dk

Michael A.E. Andersen
Dept. of Electrical Engineering
Technical University of Denmark
2800 Kgs. Lyngby, Denmark
ma@elektro.dtu.dk

***Abstract*—In this paper a new control-interface card for developing simple control loops and generating test signals for power electronic converters is presented. The control board can operate with two computational cores (Texas Instruments and Microchip) allowing using the preferred DSP architecture and development environment. Moreover, the interface board can operate with open hardware Arduino-like boards such as the ChipKit Uno32. The paper also describes how to enhance the performance of a ChipKit Uno32 with a dsPIC obtaining a more suitable solution for power electronics. The basic blocks and interfaces of the boards are presented in detail as well as the board main specifications. The board operation has been tested with three core platforms: TI Piccolo controlSTICK, a Microchip dsPIC and a ChipKit Uno32 (Arduino-like platform). The board was used for generating test signals for characterizing 1200 V Si and SiC power semiconductors. A 6 kW dc-dc converter prototype is presented; the converter is based on the developed interface board.**

I. Introduction

As green energy is getting more important, developing optimized power electronic converters is becoming more and more complex. Developments in new power semiconductors such as silicon carbide (SiC) together with new topologies and control strategies resulted in commercially available 99%+ efficiency power converters (examples of 99%+ efficiency SMA solar inverter [1], and converter prototypes [2][3]). High efficiency designs are challenging, require advance knowledge in power electronics and also in digital electronics. In fact, novel and complex modulations strategies are mostly implemented on microcontrollers (uCs) or more commonly digital signal processors (DSPs [4]) and field programmable gate arrays (FPGAs [5]). Boards hosting DSPs require variety of auxiliary circuitry for signal conditioning and powering all auxiliary peripherals which are required for a proper operation of the power electronics converter. On the market there is a large availability of control boards for power electronics: some solutions allow focusing on development-optimization of control loops and modulations strategies without having detailed knowledge about DSP architectures [6]. These solutions are very flexible and suited for developing prototypes or proof of concepts however, they often tend to be costly and not always suited for the single research groups. Other available solutions are represented by development kits provided by several microcontrollers, DSPs and FPGAs manufacturers. These boards necessitate of various external components and the developer is often designing his own interface boards, since commercial boards are often overwhelmed with functions. The lack of availability is mainly due to the fact that each application is different and requires a custom-designed controller board depending on the design needs.

In recent years Arduino-like platforms have seen enormous diffusion both in amateur applications and in research environments due to their simplified programming language and low-cost [7]-[9]. The spreading of the new open hardware platform led to an increase of available "interface shields"; this increased furthermore the flexibility of the Arduino platforms which started to spread in most of the academic environments. In the development of control loops for power electronic converters, the platform was not really successful probably due to the limited performances of the microcontrollers which the boards are based on or the lack of availability of suitable interface boards for power electronics.

The paper presents an interface board that can be used for developing power electronics test platforms and control loops. The interface board can operate with the low-cost TI Piccolo controlSTICKs or with an Arduino-based platform like the Arduino 2009 or the ChipKit Uno32. For increasing the performance of the Arduino-like platforms the paper proposes the replacement of the original microcontroller on ChipKit Uno32 boards with a more performance dsPIC which performance are similar to the TI platform. The interface board can be operated with the desired core and simply

Project sponsored by the Energy Technology Development and Demonstration Programme (EUDP) "Green Natural Gas", 2011-2014.

978-1-4673-4916-1/13/$31.00 ©2013 IEEE

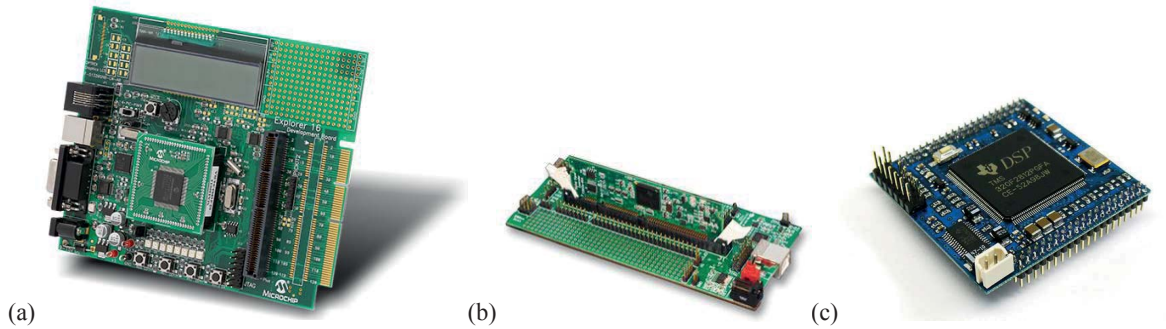


Fig. 1. Commercially available development boards for power electronics and signal conditioning applications. Microchip dsPIC development board (a), TI controlCARD F28035 (b) and DSP header board F2812 (c).

programmed with the available tools from the manufactures (e.g. Texas Instruments Code Composer Studio or Microchip MPLAB). The developed interface board was used for generating test signals and characterizing the switching performance of 1200 V Si and SiC power semiconductors [10][11]. Moreover, a 6 kW dc-dc isolated boost full bridge converter prototype was developed and tested with the presented interface board [11].

II. Conventional Power Electronics Control Boards and Interfaces

Conventional platforms utilized for developing control loops for power electronic converter prototypes have a main core (e.g. uC, DSP, FPGA) surrounded by additional signal conditioning circuitry, general I/O interfaces and ports (Fig. 1a). These boards tend to have a large number of features and during the development of a converter prototype most of these features remains unused. Moreover, these boards tend to be costly also due to the large number of embedded features. Some development boards have minimal embedded circuitry which is just sufficient for generic data transfer and for board programming (Fig. 1b). This approach often utilizes a daughter board which can be used to develop customized signal conditioning circuitry depending on the project needs. Another approach utilizes "core boards" (Fig. 1c); in this case the board hosts uniquely the main core (e.g. uC, DSP, FPGA), the core power stage and the programming interface. All other I/Os are directly interfaced to the main core with no signal conditioning circuitry along the path. In some products, different cores are implemented on a single board (e.g. DSP with FPGA) providing additional functionality and enhanced possibilities for customization of the core functionalities. All these platforms have a common structure that can be summarized as Fig. 2a. This structure is based on a fixed core which cannot be exchanged with other cores. These solutions often limit the developer to the development tools from the board supplier or manufacturer moreover, migrating towards another DSP architecture is complex and time demanding.

III. A New Concept for a Flexible Power Electronics Control Boards

A new controller card for quick prototyping and developing control loops for power electronic converters was developed. The main concept behind the developed board is its multi-platform support, Fig. 2b. The interface board is compatible with the two most used DSP development tools in power electronics: Code Composer Studio from Texas Instruments and MPLAB from Microchip. Moreover, in order to allow fast prototyping, the board has an interface compatible with an Arduino board (e.g. Arduino 2009 or

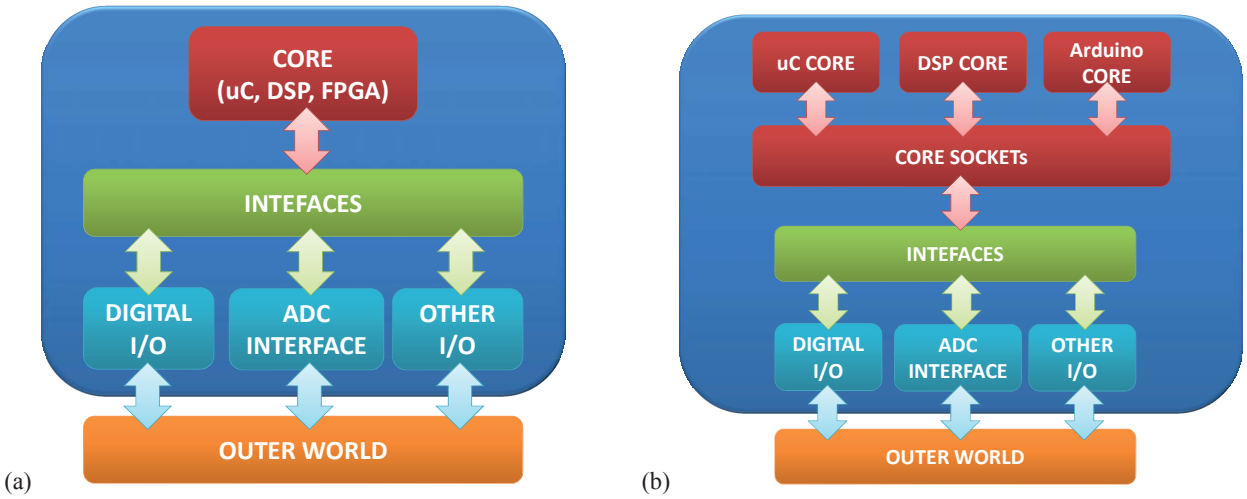


Fig.2. Conventional block structure for power electronics control boards (a) and structure of the designed interface board based on multi-platform support (b).

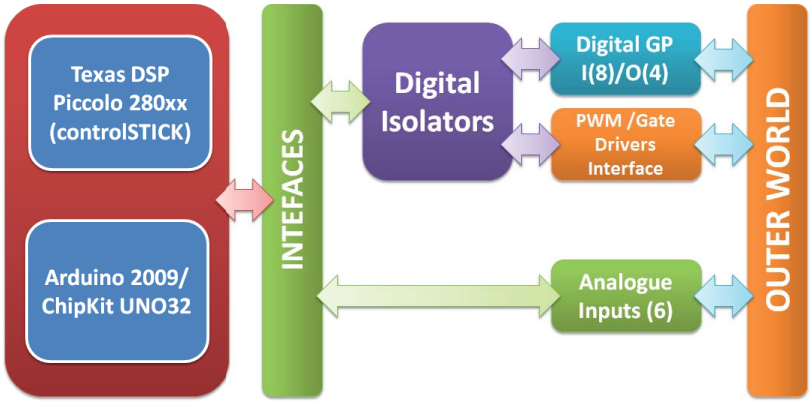


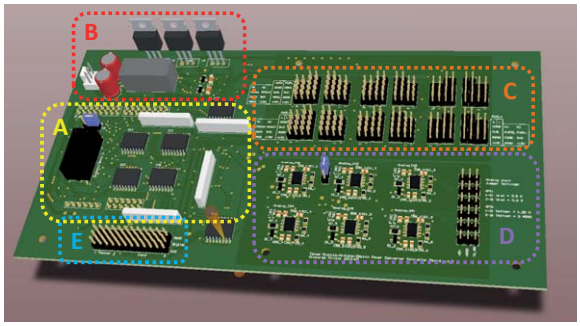
Fig. 3. Block overview of the designed interface board for TI Piccolo controlSTICK /Arduino 2009 /ChipKit Uno32 /dsPIC.

ChipKit Uno32). The board has different interface sockets, these allow the board to interface to different commercial DSP boards such as the TI Piccolo controlSTICK of the ChipKit Uno32 (Arduino-like platform). Only one of the selected platforms can be used on the interface board; operating with multiple cores at the same time it is not possible due to interface sharing. The designed interface board offers the possibility of developing test signals or control loops based on the preferred core architecture. Moreover, the support of Arduino-like boards and, therefore, of the Arduino environment (simplified C programming) allows fast prototyping.

The development has been focused on maintaining wide application-flexibility, contained costs and simplicity. The desired interface board can operate with two different DSP cores (block structure on Fig. 3); it is suitable for developing test signals and control loops for hard switching power electronic converters in the 1-10 kW range which usually has switching frequencies below 200-300 kHz [12][13] for hard switched converters. The board is developed for being used with ac/dc or dc/dc converter and, in general, with isolated or non-isolated converters. The board main requirements are: 4 PWM channels (complementary), 4 analog input channels (min 10 bit), A/D >500 kS/s, digital isolation and some additional GPIO.

Most of the commercially available DSPs match these specifications; however, the development has been focused on two main platforms: TI Piccolo controlSTICK [14] and Arduino /ChipKit Uno32 [15]. The TI Piccolo controlSTICK is often used in power electronics due to its relatively low cost, flexibility and features. The open hardware Arduino /ChipKit Uno32 can represent a suitable starting point for amateur use. However, in power electronics, the Arduino platform has several computational and timing limitations due to the limited performance of the onboard microcontrollers. The Uno32 is based on a 32 bit microcontroller which is pin to pin compatible with other DPSs from Microchip (dsPIC [16]). This makes the Uno32 board a good backbone for a dsPIC-based board (e.g. 33FJ64GS606) which is more suited for power electronics.

All platforms require external circuitry to be able to develop a complete control system for a power electronic converter (external power supplies for gate drivers, filtering of A/D channels, isolation of digital signals, voltage references, etc). In power converters the control circuitry can be located far from the converter power stage; however, some components such as gate drivers and sensors (current and voltage) have to be located close to the power circuitry. For this reason, the interface board does not integrate gate drivers and sensors. Since Arduino-like platforms are widely spread, the developed interface board will be compatible with Arduino 2009 systems. However, the main target cores will remain a Uno32 based on a dsPIC33 and a TI Piccolo controlSTICK.

(a) 

(b) 

Fig.4. 3D model of the designed interface board highlighting its main interface blocks (a) and developed prototype (b).

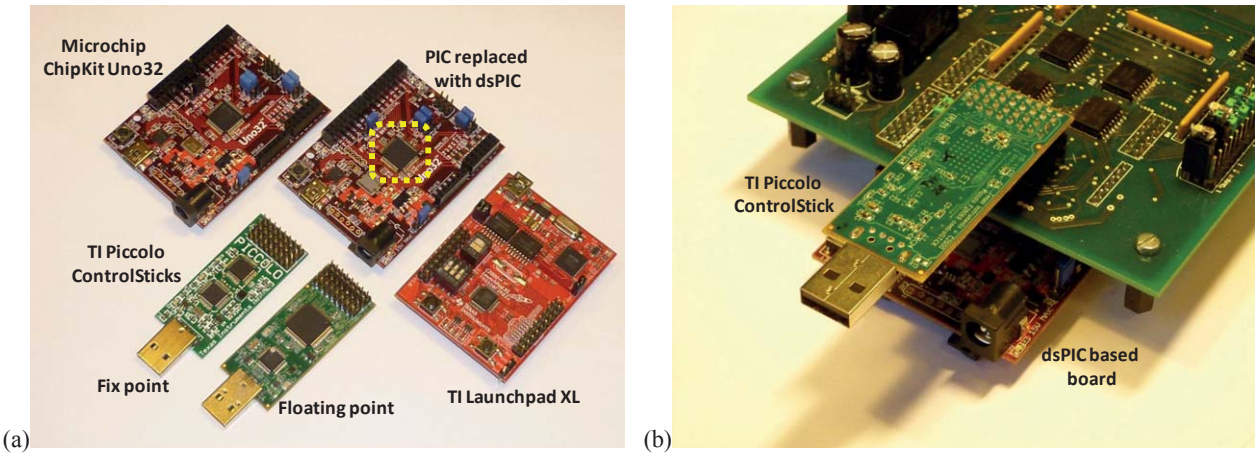


Fig. 5. Core boards (a) and core boards installed on the interface board (b). NB: the core boards cannot be used simultaneously.

IV. Description of Main Blocks and Interfaces

The developed board is an interface board whose main functional blocks (Fig. 4a) are described below and an overview of the board prototype is presented on Fig. 4b.

A. Arduino /dsPIC /DSP TI Piccolo controlSTICK Connectors

The board features the capability of operating with a TI Piccolo controlSTICK or with an Arduino /ChipKit Uno32 /dsPIC which represent the computational cores of the board. All digital I/O of the platforms are isolated through high speed capacitive isolators providing also voltage level shifting (up to 5 V) and higher I/O current capability (up to 15 mA per I/O). I/O capability is limited by the selected platform. On one ChipKit Uno32 the original microcontroller was replaced with a more powerful dsPIC more suitable for controlling power electronic converters (Fig. 5a). The interfacing sockets are located on top and on the bottom of the board, Fig. 5b.

B. Integrated Power Supply and Voltage References

The board is supplied with dual 12-15 V. The +12/15 V rail directly powers the gate driver connectors and has to ensure sufficient power for driving the power semiconductors (gate drivers). Additional dual 5 V are used for powering the onboard op-amps. The board features a 3 W isolated dc/dc power supply for generating the digital rail voltages required for the DSP and the digital ICs (5 V and 3.3 V).

The board grounds (analog and digital) were kept separately; however, since low-cost DSP boards like the TI Piccolo controlSTICK does not have separate analog and digital grounds, there is always one point of common coupling for the two grounds (DSP board). Ferrite beads can be placed between the two board grounds (maintaining the common coupling point); alternative, 0-Ohm resistors can be replace the ferrite beads depending on the system ground configuration. This section of the board also integrates two auxiliary voltage reference required as auxiliary reference for the A/D converter (+2.5 V) and +1.25 V used as DC-bias.

C. Gate Driver/PWM Interface

The gate driver interface (PWM connectors on Table I) provides up to six complementary PWM channels. The connectors also provide analog supply (+12/15 V depending on the board supply voltage) and digital supply (+5 V) useful for powering directly the gate drivers and local signal conditioning logic. The gate driver connectors are grouped into three main categories depending on the PWM signals they provide. The complementary connectors provide two PWM signals (complementary connector CPWMx) suited for a phase-leg of a voltage source converter. The boost full bridge PWM connectors provide two independent PWM signals (e.g. PWM1 and PWM2, connector BPWMx) ideal for driving the phase legs in a full bridge isolated boost converter and the single gate driver connectors are a general purpose single-PWM channel.

TABLE I. Gate Driver - PWM connectors

		PWM1H	PWM1H			PWM2H	PWM2H		
NC	NC	DGND	DGND			DGND	DGND	NC	NC
PWM1L	PWM1H	5V0	5V0			5V0	5V0	PWM2L	PWM2H
DGND	5V0	AGND	AGND			AGND	AGND	DGND	5V0
AGND	+15V	+15V	+15V			+15V	+15V	AGND	+15V
CPWM1		PWM1H	PWM1H			PWM2H	PWM2H	CPWM2	

		PWM1L	PWM1L			PWM2L	PWM2L		
NC	NC	DGND	DGND			DGND	DGND	NC	NC
PWM2H	PWM1H	5V0	5V0			5V0	5V0	PWM2L	PWM1L
DGND	5V0	AGND	AGND			AGND	AGND	DGND	5V0
AGND	+15V	+15V	+15V			+15V	+15V	AGND	+15V
BPWM1		PWM1L	PWM1L			PWM2L	PWM2L	BCPWM1	

D. Analog Input Interface

The board has the capability of receiving six unipolar analog signals. When the board is powered by a TI Piccolo, the internal ADC operates at 12 bit resolution while, with a dsPIC, the resolution is limited to 10 bit. The analog connectors provide also a 5 V supply for powering the sensor (e.g. LEM module). Each analog channel has signal conditioning circuitry: operational amplifiers add dc-bias, moreover they perform a second order active filtering (Sallen–Key filter) and scaling. The op-amps have a dual power supply to ensure linear operation in the 0-3.3 V range (min-max ADC range).

E. General Purpose I/O

The interface board also provides 12 isolated 5 V general purpose inputs (8) and outputs (4) (GPIO). Since the selected digital isolators are unidirectional devices, the input /output pins cannot be reconfigured.

V. Development Tools and New dsPIC-based ChipKit

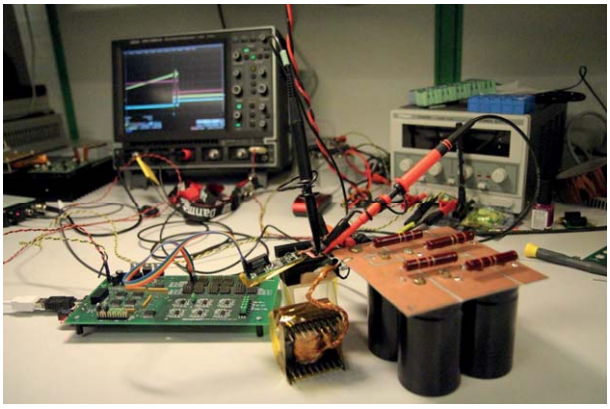
The standard Arduino development environment cannot provide suitable performances for developing complex control systems. Moreover, the performances of on board microcontroller on Arduino-like platforms are too low for the specified requirements. This reduces the choice to two main solutions: the TI Piccolo controlSTICK and a ChipKit Uno32 based on a dsPIC. For these platforms the manufacturers provide suitable development tools with some limitations for the free versions (TI Code Composer Studio [14] and Microchip MPLAB [16]).

The use of Arduino environment is limited to the supported microcontrollers. This represents the main limitation in terms of performance and resources. Moreover, the Arduino development environment (or Arduino-like environments) does not provide support for dsPICs. A commercial Arduino platform can still be used with the designed interface board; this will have some limitations in terms of performances (e.g. low A/D sampling rate), available resources and DSP features.

On one ChipKit Uno32, the original onboard microcontroller (PIC32MX320F128H) was replaced with a dsPIC (33FJ64GS606, Fig. 5a) which is a digital signal controller with features for power electronics. The replacement of the original microcontroller was possible since the pin layout of the PIC32 and dsPIC families (e.g. 33F series 64-pin TQFP package) are compatible for the same package type. This solution is more suitable for designing control loops for power electronic converters, since it is possible to benefit of all DSP functionalities of the dsPIC family. The main drawback of this solution is that it is not possible to program the platform with the Arduino environment as previously done for the PIC32 (simplified C programming language). With the new dsPIC it is required to use development tools that support these devices such as MPLAB. The solution gives a significant performance and features increase thanks to the DSP functionalities of the dsPIC (e.g. faster PID execution due to the dedicated DSP functionalities).

VI. Experimental Tests and Prototype of a DC-DC Converter

The functionality of the interface board was tested with a TI Piccolo controlSTICK, a ChipKit Uno32 and a ChipKit Uno32 modified with a dsPIC. When using the ChipKit Uno32 the board was programmed in Arduino-like environment for generating double pulse test signals for measuring the switching performance of 1200 V Si and SiC power semiconductors, Fig. 6a. The Arduino-like environment allowed to easily creating a USB-serial interface that could vary the pulse width and, therefore, the test conditions for the power semiconductor through a computer interface. This setup on Fig. 6a is often referred as double pulse test circuit; it was used to characterize the switching performance of power semiconductors such as Si IGBTs, SiC JFETs and SiC MOSFETs in [10][11]. During these test it was important to maintain exactly the same pulse width (therefore, the same testing current, Fig. 6b, to guarantee that the test conditions were maintained the same for different power semiconductors. In this case, the main advantage was that the pulse and test repeatability was higher than when an analog pulse generator is used.

(a) 

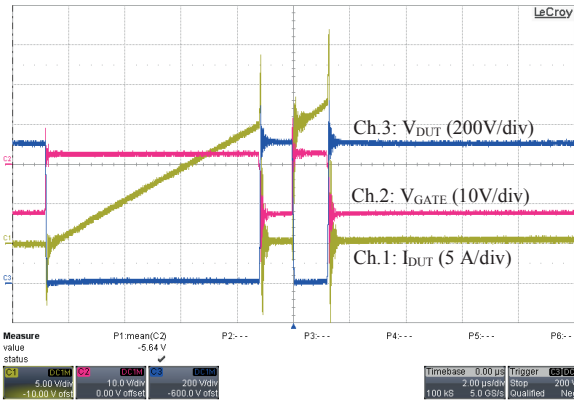
(b) 

Fig. 6. Interface board used in a test bench for characterizing 1200 V Si and SiC power semiconductors switching performance (a) and measured waveforms across the power semiconductors. Pulses were generated with the control card and a gate driver for properly driving the power semiconductors (b).

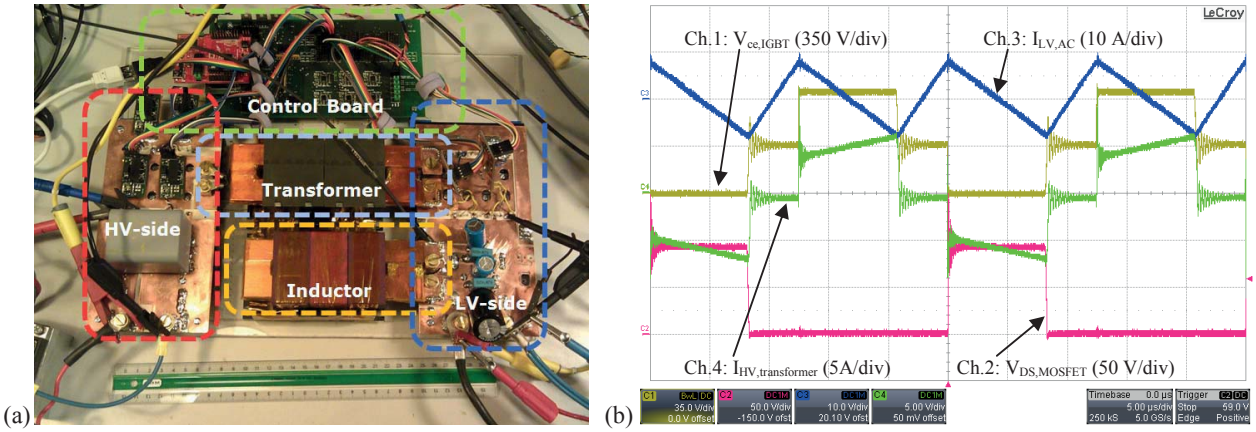


Fig.7. Developed prototype of the dc-dc converter with the interface board (a) and switching waveforms (b) at 60 V 40 A on the low voltage side and 750 V on the high voltage side in SOFC mode. Ch.1(yellow): $V_{ce,IGBT}$ (350 A/div), Ch.2(red): $V_{ds,MOSFET}$ (50 V/div), Ch.3(blue): $I_{LV,AC}$ (10 A/div), Ch.4(green): $I_{HV,transformer}$ (5 A/div). Time 5µs/div.

A 6 kW bidirectional dc-dc isolated full bridge boost converter (IFBBC) prototype was developed [11], Fig. 7a. The converter low voltage side is characterized by and 30-80 V range with current up to 80 A (current limitation). The converter high voltage side is designed as dc-link for a 400 V_{rms} grid-tie inverter with a dc-link voltage in the 700-800 V range. The converter uses Si MOSFETs on the low voltage side and Si IGBTs with SiC antiparallel diodes on the high voltage side. The converter is switching at 40 kHz and its main waveforms are presented on Fig. 7b. The converter control boards is based on the developed interface board and the main core is a ChipKit Uno32 modified with a dsPIC. The converter was tested at different voltage levels, power levels and characterized in efficiency terms. Efficiency characterization is shown on Fig 8a with the power flow from the low voltage to the high voltage side and on Fig. 8b with the power flowing form the high voltage side to the low voltage one. Respectively the peak efficiencies are 97.8% and 96.5% both at 80 V (maximum voltage on the converter low voltage side). At lower voltages (30 V) the peak efficiency is limited to ~96% and to 93% depending on the power flow direction.

VII. Conclusions

When developing control loops and test setups for power electronics converters choosing the suitable development tool is often a challenge that takes into account personal skills, available time and cost. The paper has presented a simple and flexible solution for developing controls of power electronics converters which can operate with different microcontrollers or DSP platforms (open hardware Arduino /ChipKit Uno32 /TI Piccolo controlSTICK). The board has the potential to reduce the prototyping time since it allows using the preferred DSP /microcontroller technology and development tools (e.g. Arduino, Texas Code Composer Studio or Microchip MPLAB). The support of the Arduino environment can

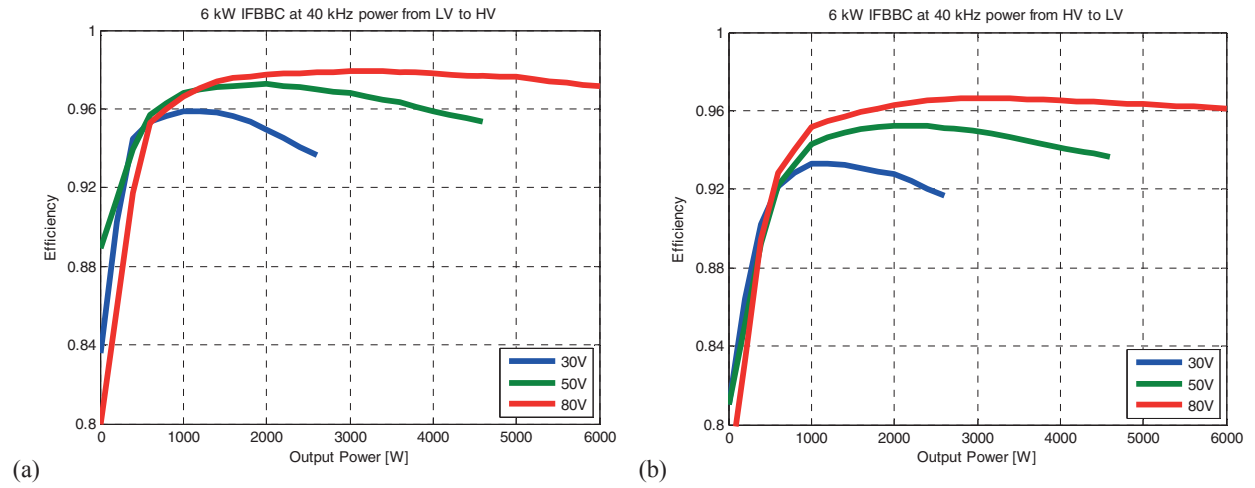


Fig. 8. Dc-dc converter efficiency characterization at different voltage and power levels. Power flow from the low voltage to the high voltage side (a) and from the high voltage to the low voltage side (b).

significantly reduce the development time due to the simplified programming language. Moreover, to overcome the limitations of the conventional platforms based on Arduino-supported microcontrollers, the paper recommends replacing the PIC32 on a ChipKit Uno32 with a dsPIC of the "33FxxxGSxxx" family. In this way the interface board would benefit from enhanced DSP functionalities especially suited for closed loop control of power electronics converters.

The developed interface board was successfully used for generating test signals to characterize the switching performance of 1200 V Si and SiC power semiconductors. Moreover, the board was used in the development of a high efficiency dc-dc isolated full bridge boost converter prototype achieving peak efficiencies of 97.8% and 96.5% depending on the converter power flow.

REFERENCES

[1] Regine Mallwitz, "First 99% PV Inverter with SiC JFETs on the market – future role of SiC", Power Conversion Intelligent Motion Conference, PCIM Europe 2012, 8-10 May 2012, Nurenberg, Germany.

[2] Rabkowski, J.; Peftitsis, D.; Nee, H.-P.; , "Design steps towards a 40-kVA SiC inverter with an efficiency exceeding 99.5%", Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2012), pp.1536-1543, 5-9 Feb. 2012.

[3] Badstuebner, U.; Biela, J.; Kolar, J.W.; , "Design of an 99%-efficient, 5kW, phase-shift PWM DC-DC converter for telecom applications",Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2010), pp.773-780, 21-25 Feb. 2010.

[4] Kirubakaran, K.; Jain, S.; Nema, R.K.; , "DSP-Controlled Power Electronic Interface for Fuel-Cell-Based Distributed Generation", IEEE Transactions on Power Electronics, vol.26, no.12, pp.3853-3864, Dec. 2011.

[5] Sugahara, K.; Oida, S.; Yokoyama, T.; , "High performance FPGA controller for digital control of power electronics applications", IEEE 6thInternationalPower Electronics and Motion Control Conference, 2009 (IPEMC '09), pp.1425-1429, 17-20 May 2009.

[6] Li Weichao; Hu An; Geng Shiguang; Sun Chi, "Rapid control prototyping of fifteen-phase induction motor drives based on dSPACE," International Conference on Electrical Machines and Systems (ICEMS 2008), pp.1604-1607, 17-20 Oct. 2008.

[7] Sarik, J.; Kymissis, I.; , "Lab kits using the Arduino prototyping platform," IEEE Frontiers in Education Conference (FIE), 2010, pp.T3C-1-T3C-5, 27-30 Oct. 2010.

[8] Buechley, L.; Eisenberg, M.; , "The LilyPad Arduino: Toward Wearable Engineering for Everyone," IEEE Pervasive Computing, vol.7, no.2, pp.12-15, April-June 2008.

[9] Kioumars, A.H.; Liqiong Tang; , "Wireless network for health monitoring: heart rate and temperature sensor", Fifth International Conference on Sensing Technology (ICST 2011), pp.362-369, Nov. 28 2011-Dec. 1, 2011.

[10] Pittini, Riccardo; Zhang, Z.; Andersen, A.E.M., "SiC JFET Cascode Loss Dependency on the MOSFET Output Capacitance and Performance Comparison with Trench IGBTs", Twenty-Eight Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2013), pp.1287-1293, 17-21 March 2013.

[11] Pittini, Riccardo; Zhang, Z.; Andersen, A.E.M., "Switching Performance Evaluation of Commercial SiC Power Devices (SiC JFET and SiC MOSFET) in Relation to the Gate Driver Complexity", 5thAnnual International Energy Conversion Congress and Exhibition in Asia (ECCE Asia 2013), 3-6 June 2013.

[12] Sanbo Pan; Mi, C.; Lin, T.; , "Design and testing of silicon carbide JFETs based inverter," IEEE 6thInternational Power Electronics and Motion Control Conference, 2009. IPEMC 2009, pp.2556-2560, 17-20 May 2009.

[13] Simanjorang, R.; Yamaguchi, H.; Ohashi, H.; Nakao, K.; Ninomiya, T.; Abe, S.; Kaga, M.; Fukui, A.; , "High-efficiency high-power dc-dc converter for energy and space saving of power-supply system in a data center," Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2011), pp.600-605, 6-11 March 2011.

[14] Texas Instruments Piccolo controlSTICK, www.ti.com.

[15] Digilent ChipKit Uno32, www.digilentinc.com.

[16] Microchip dsPIC series, www.microchip.com.

www.elektro.dtu.dk

Department of Electrical Engineering
Electronics Group (ELE)
Technical University of Denmark
Oersteds Plads bygning 349
DK-2800 Kgs. Lyngby
Denmark
Tel: (+45) 45 25 25 25
Fax: (+45) 45 88 01 17
Email: info@elektro.dtu.dk