#### Technical University of Denmark



#### Upscaling of Indium Tin Oxide (ITO)-Free Polymer Solar Cells

Performance, Scalability, Stability, and Flexibility

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# Upscaling of Indium Tin Oxide (ITO)-Free Polymer Solar Cells

Performance, Scalability, Stability, and Flexibility

# Ph.D. Dissertation

Dechan Angmo

September 2013

#### **Upscaling of Indium Tin Oxide (ITO)-Free Polymer Solar Cells** Performance, Scalability, Stability, and Flexibility

September, 2013

#### By Dechan Angmo

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## Preface

Roskilde, September 2013

Sometimes life takes you on a journey only to prepare you for what you wished for. I have always wanted to combine my love and aptitude for science to do something meaningful to the underprivileged part of the world, having grown up in one. Second year in college, I knew I wanted to study renewable energy. Ever since then, I had carved my way to lead me to solar cells. And today, I hand in my thesis with much pride.

It would not have been possible without my supervisor, Professor Frederik C. Krebs. I am indebted to him for giving me this opportunity and also for his tireless support throughout the last three years. His commitment and passion to his work is very contagious and has kept me motivated throughout all these years. Dr. Mikkel Jørgensen is also specially thanked for always being there when I struggled with scientific problems or with the LBIC instrument.

This Ph.D. has been a part of European Commission funded FP7 collaborative project titled HIFLEX. I would like to acknowledge all the people I met under HIFLEX from whom I learnt a lot. Especially, I would like to thank Dr. Yulia Galagan and Dr. Ronn Andreissen for making my research stay at Holst Center in Eindhoven, Netherlands, a productive and a memorable one.

I also extend my gratitude to all my dear colleagues who have never turned a deaf ear to my incessant questions. The camaraderie of this group is unparalleled to any other groups that I have previously worked with. Particularly, I thank Markus Hösel for reading my dissertation and more importantly for catapulting me to my current illustrator skills and being my walking-talking Wikipedia on industrial processing. He is always willing to listen to my questions and musings, no matter how trivial. Suren Gevorgyan, Henrik Friis Dam, Morten V. Madsen, Thue T. Larsen-Olsen, and Thomas R. Anderson are especially thanked for listening to my scientific problems and sharing their knowledge without any hesitation. Nieves Espinosa is also thanked for fruitful comments on Chapter 8. I thank Birgitta Andreasen, my only female counterpart in our group for more than 2 years, for being a friend in this far away land. Thanks for listening to me in hard times and sharing laughter in good times.

I thank my family for their pride in me and supporting me in whatever I do, wherever I go, and whoever I become. Their love remains unconditional.

Finally but most importantly, I thank my late mother. Her 3 o'clock tea in the morning when I used to pull an all-nighter during school was inexpressibly missed this time around. Words have always fallen short when I talk of my mother. Having very little education herself and coming of very remote region of the world, she has instilled in me the value of education and the need of perseverance and perspiration required to attain it. I am her sacrifices. To her, I dedicate this thesis with a note: my best is yet to come.

### Abstract

Polymer solar cells (PSCs) aim to produce clean energy that is cost-competitive to energy produced by fossil fuel-based conventional energy sources. From an environmental perspective, PSCs already compares favorably to other solar cell technologies in terms of fewer emissions of greenhouse gases during production. The costcompetitiveness of PSCs is envisioned achievable by the use of inexpensive materials and high throughput roll-to-roll (R2R) printing and coating techniques. The state-ofthe-art of the laboratory PSCs is, however, far removed from the vision of the widely disseminated low-cost solar cells as the laboratory solar cells are mostly focused on increasing the power conversion efficiency through materials design with little emphasis on the choice of materials, operational stability and large-scale processing. Indium-tinoxide (ITO), the commonly used transparent conductor, represents majority of the share of cost and energy footprint in terms of materials and processing in a conventional PSC module. Furthermore, the scarcity of indium is feared to create bottleneck in the dawning PSC industry and its brittle nature is an obstacle for fast processing of PSCs on flexible substrates as well as for applications in flexible end products. Thus, the replacement of ITO with low-cost alternatives is crucial for the commercial feasibility of PSCs.

Encompassing these concerns, my PhD study has *contributed* to the development and evaluation of alternatives to ITO in laboratory cells, upscaling of ITO-free concepts from laboratory cells to R2R produced large-area modules, and integration of these module in demonstrator consumer applications. Accordingly, this dissertation is organized into nine chapters. Chapter 1 is aimed at contextualizing PSCs on the world energy map. It aims to address the question: why should PSCs be pursued? Chapter 2 attempts to provide a concise yet encompassing introduction to PSCs; and the problem with ITO and possible solutions. It also lays out specific targets that were set before the beginning of PhD study which provides a frame-of-reference for the later chapters. A holistic evaluation of several ITO-free concepts was carried out to determine low-cost upscaling compatibility of these concepts (Chapter 3). The results highlighted three architectures that represented different competencies with regards to photovoltaic performance, stability, and low-cost processing. These three architectures were upscaled (Chapter 5-7) using R2R techniques described in detail in Chapter 4. One of the three upscaled architecture (Chapter 7) represented an efficient alternative to ITO in terms of photovoltaic performance and were further investigated for stability and flexibility. These modules were then integrated in a credit-card size laser pointer for demonstration purposes. A colleague, Nieves Espinosa, has conducted life-cycle analyses (LCA) on all the three upscaled ITO-free architectures. Drawing upon the data from her published work, Chapter 8 provides concise and comparative LCA of the three upscaled ITO-free architectures in order to determine which technology can be pursued further among the three architectures. LCA results of the ITO-free architectures are also compared against ITO-based upscaled PSCs as well as against other photovoltaic technologies. Finally, the last chapter (Chapter 9) puts everything in the nutshell and identifies future challenges.

### Resumé

Plastsolceller (PSC) har til formål at producere ren energi, der er prismæssigt konkurrencedygtig sammenlignet med energi produceret af konventionelle fossile brændsler. Fra et miljømæssigt perspektiv sammenlignes PSC allerede positivt til andre solcelle-teknologier i form af færre emissioner af drivhusgasser under produktionen. Konkurrenceevnen for prisen på PSC opnås ved brug af billige materialer og høj hastigheds rulle-til-rulle (R2R) trykning samt coating teknikker. De bedste PSC produceret i laboratorieforhold er langt fra visionen om den meget udbredte billige solcelle, da disse mest er fokuseret på at øget effektiviteten gennem design med lille vægt på valget af materialer, driftsstabilitet og omfattende behandling. Indium-tin-oxid (ITO), den mest almindeligt anvendte transparente leder, repræsenterer størstedelen af omkostningerne og energi fodaftrykket i form af materialer og forarbejdning i et konventionelt PSC modul. Desuden vil manglen på indium skabe en flaskehals i PSC industrien og samtidig er ITOs struktur en hindring for hurtig behandling af PSC på fleksible substrater, samt for fleksibiliteten af slutproduktet. Udskiftning af ITO med billige alternativer er således afgørende for den kommercielle succes for PSC.

Med disse bekymringer i mente, har mit ph.d.-studie bidraget til udvikling og evaluering af alternativer til ITO i laboratorieceller, opskalering af ITO-fri koncepter fra laboratorium til R2R produceret –moduler med stort areal og integration af disse moduler i forbruger-applikationer til demonstration. Derfor er denne afhandling organiseret i ni kapitler. Kapitel 1 placerer PCS på et energiforsynings-verdenskort. Det ledende spørgsmål i kapitel 2 er hvorfor skal PSC videreføres? Her gives en kortfattet, men omfattende introduktion til PSC, samt problemet med ITO og mulige løsninger. Det indeholder også konkrete mål, der blev sat før begyndelsen af ph.d.-studiet, som giver en ramme for de senere kapitler. En helhedsvurdering af flere ITO-fri koncepter blev udført for at bestemme deres opskalerings kompatibilitet (kapitel 3). Resultaterne fremhævede tre arkitekturer, der repræsenterede forskellige fordele med hensyn til solcellernes ydeevne, stabilitet og lave forarbejdningsomkostninger. Disse tre arkitekturer blev opskaleret (kapitel 5-7) ved hjælp R2R teknikker beskrevet i detaljer i kapitel 4. En af de tre opskalerede arkitekturer (kapitel 7) udgjorde et effektivt alternativ til ITO i form af solcelle præstation og blev yderligere undersøgt for stabilitet og fleksibilitet. Disse moduler blev yderligere integreret i en kreditkortformat-laserpointer til demonstration. Nieves Espinosa, en kollega, har gennemført livscyklusanalyser (LCA) på alle tre opskalerede ITO-fri arkitekturer. Data fra hendes offentliggjorte arbejde (kapitel 8) er kortfattet beskrevet og sammenligner LCA for de ITO-fri arkitekturer med henblik på at afgøre hvilken teknologi kan videreføres. LCA resultaterne for ITO-fri arkitekturer er også sammenlignes med opskalerede ITO-baserede PSC samt mod andre fotovoltaiske teknologier. Endelig sætter sidste kapitel (kapitel 9) afhandlingen i perspektiv og identificerer fremtidige udfordringer.

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# 1. Why Polymer Solar Cells?

#### 1.1 World Energy Scenario

Modern society is built upon energy consumption. Energy enables access to basic amenities such clean drinking water, sanitation, healthcare, food, shelter, etc. which improve our living conditions. Furthermore, it enables the functioning of all modern technologies which has become an integrated part of our everyday existence. Running out of fuels to power the engine of the modern age would have unimaginable consequences on our quality of life and would render all technological innovations futile. Unfortunately, the threat is imminent. In 2011, total world power consumption was 12.27 million tons of oil equivalent (MTOE) of which 87% was generated from natural gas, oil, and coal. Calculations have shown that the known reserves of oil, natural gas and coal can sustain the current consumption pattern for 52, 64, and 112 years, respectively [1]. However, the world's fuel consumption is rapidly increasing primarily due to improving living standards in emerging markets and increasing world's population (Figure 1). A United Nations report estimates that the current population of 7 billion will reach 9.6 billion in the year 2050 [2]. During the same time, the world energy consumption is projected to increase to 30 TW in 2050- twice that of current world consumption of 15 TW [3]. It is the economic expansion and population growth in the non-OECD (Organisation of Economic cooperation and development) countries that will dictate the future global energy demand (Figure 1-1). If the production of the fossil fuels were allowed to increase to meet the increasing demand, then the predicted lifetime of the fossil fuels (estimated as reserve to production ratio) will be significantly shorter. Instead, fossil fuel companies attempt to maintain the lifetime of fossil fuels constant by restricting supply as new reserves are increasingly becoming harder to discover. This practice consequently leads to rapid increase in fuel prices [4]. Either scenario are disastrous and calls for the development of alternate, sustainable, energy sources in order to satisfy the increasing world demand and to ensure availability of energy to our future generations.



Figure 1-1 The historical trend of increasing global energy consumption displaying the contributions from various sources in the global energy mix (left) [5]. The projected growth in energy demand driven mostly by non-OECD countries (right). © RSC publishing. Reprinted, with permission rom ref. [3].

#### **1.2** Renewable Energy Resources

Renewable energy resources are inexhaustible sources of energy that are clean and do not contribute to greenhouse gas emission. Sun is the ultimate source of all renewable energy forms: solar energy, wind energy, geothermal energy, biomass, hydro and tidal energy. In 2011, renewable energy constituted only 8.0% of the global energy consumption, of which 6% came from hydroelectricity [5]. The rest of the renewable energy technologies remain the least exploited. The lack of economic incentives despite their environmental benefits has prohibited renewable energy technologies to significantly contribute to world's energy supply. This is because fossil fuels have been the cheapest source of energy. Increasing fossil fuel prices, however, have enabled alternate energy sources to enter the market. Renewable energy sources, particularly wind energy and solar cells, are currently experiencing a rapid growth. From 2010 to 2011, the net renewable energy excluding hydroelectricity share to global energy consumption increased by 17.7%. During this period, power generation by solar cells experienced an increase of 86.71% while wind energy experienced a growth of 26% [1,5].



#### Where is solar cells?



Despite these impressive numbers, the net impact of such a rapid growth of renewable energy resources in the global energy mix remains marginal with a dismal 2.2% contribution in the global energy mix in 2011. Of this, solar cells contribution to global energy mix is horrifically only 0.12% [1,5]. However, this scenario is changing as the cost of energy produced by renewable energy is becoming cheaper with rapid scientific innovations while the cost of energy produced by fossil fuels remains increasing. It is very likely the two trends will meet in the near future, making energy produced by renewable energy technologies competitive with fossil fuels.

#### 1.3 Solar cells: What impedes?

Even the most conservative estimates suggest that solar cells have the capacity to meet future global energy demand. One such estimate based on the assumption that even if only 2% of the land area on earth is allocated to solar cell plants operating at an average power conversion efficiency of 12%, the energy produced would be twice than the projected world energy demand in the year 2050 [3]. Of all the renewable energy resources, solar cell remains the most reliable yet least exploited renewable energy technology. Solar cells or photovoltaic cells convert sunlight or solar energy directly in-

to electricity and possess several advantages to any other forms of energy conversion including other renewable energy technologies:

1) It is the most benign form of energy and do not generate greenhouse gases, radioactive waste or noise pollution.

2) It the most scalable technology which can be integrated in pocket calculators or installed in large power plants. It doe necessarily not depend on large infrastructure development such as power transmission lines.

3) It runs on solar energy which is abundant and free. In fact, solar cells can potentially lead to decentralization of energy production having potential geopolitical repercussions on energy independence of nations. Microcosmically, solar cells can allow energy independence of households and businesses.

4) Solar energy is reliable and predictable. Cloudiness, humidity, pollution and other temporal variables that affect the insolation at a specific location provide a small amount of almost random perturbation [6]. In comparison, power produced from wind turbines is unreliable due to wind intermittency.

Despite these obvious advantages and despite being commercially available since 1950s, solar cells currently contribute a dismal 0.1% to the total global energy consumption with a current total world installed capacity of 55.7 TWh (Figure 1-2). Figure 1-3 shows the current world per capita energy consumption and the world distribution of average yearly global irradiance. As it can be seen, the emerging markets of Asia, south America, and Africa (apart from some developed regions such as middle-east and Australia) receives the highest annual solar irradiation. It is this part of the world that currently constitutes the 1.4 billion people that have no access to electricity and the 1.1 billion that have intermittent access as is evident in Figure 1-3a [7]. Solar cells are particularly suited in these regions and can significantly contribute to satiating to-day's unmet needs while at the same time contributing to tomorrow's increasing demand. In other words, these are the regions that represents markets with most potential for solar cells if provided at affordable cost.



Figure 1-3 (a) World distribution of per capita energy consumption in tonnes oil equivalent (TOE). © 2013 BP. Adapted from, ref.[5]. (b) World distribution of annual global irradiance. Source: NASA.

The impact of solar cells in the world energy scenario has been stifled by their high production cost which in turn is driven by highly energy intensive materials and processing requirements. Indeed, the need for minimizing materials and processing costs is the impetus that has driven the evolution of photovoltaic technology from the first to the third generation (Figure 1-5). The first generation of solar cells is based on thick films of monocrystalline (160-240  $\mu$ m) and polycrystalline silicon (100-180  $\mu$ m). While these forms of silicon solar cells have excellent performance in terms of efficiency (average performance 15-18% and a lifetime of 20-25 years), their production is slow and involves several highly energy and labor intensive processes [8]. High purity monocrystalline silicon are grown in form of column ingots via the Czochralski process



Figure 1-4 The LCOE for Photovoltaics (PV), Concentrating solar power (CSP) and wind power at locations in Germany and Spain. The values underneath the technologies refers to: solar irradiance in kWh/m<sup>2</sup>year at optimal angle for PV, at optimal direct normal irradiance or DNI for CSP, full-load hours per year for wind. © 2013 Fraunhofer ISE, Germany. Adapted (Original image tweak ed for higher resolution for reproduction here), with permission from ref.[15]

that requires molten silicon typically achieved at 2000 °C. Silicon wafers are then sliced from the ingots-- a process that results in greater than 40% material wastage [9]. As a result, silicon wafers account for more than 70% of the cost of monocrystalline silicon solar cell modules [9]. This also translates to the fact that despite their highest efficiency among all solar cell technologies, the cost of electricity produced from the first generation solar cells still remains very far from being competitive with conventional energy sources (Figure 1-4).

The need to reduce production cost has led to the development of second generation solar cells. Second generation solar cells are thin film solar cells based on:  $\alpha$ -Si (amorphous and micromorphous silicon, maximum efficiency 9.5% and 11.7% respectively on laboratory scale), CdTe (Cadmium Telluride, maximum efficiency 16.5% on laboratory scale) and CIGS (Copper Indium Gallium Diselenide, maximum efficiency 20.3% on laboratory scale) [10]. The manufacturing of second generation solar cells is



Figure 1-5: The evolution and classification of solar cell technology. The list is not exhaustive and the timeline is to roughly demonstrate the period when each generation recorded the most rapid development. All types of solar cells are still undergoing research and development.

highly simplified, incurring 100 times less source materials than first generation, and involves largely dry techniques such as sputtering and chemical vapour deposition processes. Furthermore, they can be deposited in roll-to-roll inline on flexible substrates such as metal foils or cheaper substrates such as soda-lime glass, and avoid labor intensive assembling of discrete silicon wafers as required in the first generation of solar cells [10]. The impact of these manufacturing advances is, however, dampened by the reduced efficiency of thin films technologies as compared to first generation cells. As a result, the final electricity cost and energy pay-back time of thin film technologies are not markedly different from the first generation solar cells. Furthermore, the use of environmental hazardous and rare elements such as cadmium makes some of the thinfilm technologies less competitively advantageous to the first generation solar cells.

Based on the experiences of the first and the second generation solar cells, it becomes clear that further development of the solar cells have to follow a cost-toperformance optimization where performance is defined by photovoltaic response and stability; and cost is defined by an all-inclusive materials and processing cost. Accordingly, the development of third generation has bifurcated into two independent approaches. One development line attempts to dramatically increase the efficiency of inorganic solar cells beyond that of Shockley- Queisser limit (31-41% for single junction solar cells) and is addressed via four approaches: multi-junction cells, intermediateband cells, hot carrier cells and spectrum conversion. Apart from multi-junction solar cells, the other approaches are in early stages of research [11]. The second branch aims to dramatically reduce cost by employing cheaper materials and faster processing techniques. This is accomplished in the form of organic solar cells that be processed in a very fast, high throughput processing using printing and coating techniques such as those employed in the graphics industry (e.g. newspapers, magazines, packaging, textiles, etc.). Among the third generation organic solar cells, polymer solar cells (PSCs) have demonstrated the most potential to deliver energy on a meaningful scale. It has an unmatched increasing trend in power conversion efficiency over the last decade reaching now to 11%, bringing PSCs on the same pedestal as amorphous thin film silicon solar cells in terms of efficiency [12]. Yet there remain many unresolved challenges on the path to achieve the cost and environmental targets that would enable PSC's competitiveness with conventional energy. One of the challenges facing is upscaling from laboratory to large-scale using fast processing methods and low-cost materials at ideally no loss to efficiency and stability in comparison to laboratory cells—this is the theme of this dissertation.

#### **1.4** Polymer solar cells: Scope of the thesis

The discovery of conducting polymers in the late 1970s laid the genesis of today's polymer solar cells [13]. Conducting polymers, particularly polyacetylene, could be doped to form all three classes of electronic materials: insulators, semi-conductors, and metals. The possibility of combining the electronic properties of semiconductors with lowcost processing advantages of polymers has since motivated research in PSCs. Initially, the prime focus was in the optimization of the photoactive polymer to enable power conversion efficiencies that were meaningful in the context of global energy supply and in comparison to other solar energy conversion means. In this context, the facets

#### Chapter 1 - OBWhy Polymer Solar Cells?

that make PSCs an attractive technology, the use of low-cost materials and simple processing conditions, were largely ignored and efforts were mostly concentrated on increasing power conversion efficiencies. This scenario was justified for long since early studies on PSCs reported rather poor power conversion efficiency in the order of  $10^{-2}$  % [14]. Today, the efforts into improving the inherent electronic properties of the photoactive polymer semiconductors have fructified with the technology currently reported to have a power conversion efficiency of 11% on laboratory cells [12]. Now, the challenge lies in translating such efficiency achieved on devices with an active area significantly less than 1 cm<sup>2</sup> to large area modules produced by roll-to-roll (R2R) processing while ensuring that the low-cost objective of PSCs is achieved [12].

My Ph.D. study has been dedicated to bridging the gap between laboratory cells and R2R processed large-area module in order realize the overall aim of economicallyand environmentally profitable PSCs. Following a brief introduction to PSCs and an overview on the problem with indium and possible solutions (Chapter 1), this dissertation journeys through the development and evaluation of laboratory cells based on various ITO-free architectures (Chapter 3); the process of upscaling of various ITOfree architectures highlighting the difference between laboratory processing and lowcost upscaling via roll-to-roll processing techniques; and the implications of processing adaptions with low-cost processing methods on the overall performance of each upscaled architecture (Chapter 5-7). A comparative post-analysis of the environmental feasibility based on life-cycle analysis of these upscaled architecture is also presented (Chapter 8) providing feedback for future improvements. It is noted that significant improvement has been made in realizing a cost-effective ITO-free large-area flexible PSCs.

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# 2. Polymer Solar cells: An Introduction

#### 2.1 Scope of the chapter

This chapter attempts to present a brief background on polymer solar cells (PSCs) including a brief history, basic principles, device architecture, and device characterization. A brief introduction on the need for replacement of Indium tin oxide (ITO) and possible alternatives to ITO are summarized. Finally, specific targets were laid out before the beginning of this Ph.D. study. These are listed at the end of the chapter and provide a frame of reference for the endeavors on upscaling reported in the subsequent chapters.

#### 2.2 A brief history

Several landmark discoveries and milestones have led to the PSCs that we know today. In 1839, Edmond Bacqueral, a French experimental physicist, was the first to discover the photovoltaic effect. He discovered current generation upon shinning lights of different wavelengths in his electrolyte-semiconductor cell that comprised of two platinum electrodes covered with semiconductors AgCl or AgBr which were dipped in an aqueous solution [1,2]. In 1905, Albert Einstein explained the photoelectric effect that laid the foundation our understanding of the physics of photovoltaic effect. For his "discovery of the law of photoelectric effect," Einstein was awarded Nobel Prize in 1920. The next leap in history was the first inorganic solar cell developed by Bell laboratories in 1954. Based on Silicon, the cell had a reported efficiency of 6% [2]. Although the photoconductivity in various organic compounds have been reported since 1903 including in chlorophyll, anthracine, phorphyrins etc., it was the discovery of semiconducting polymers, particularly polyacetylene, that paved the way for today's PSCs. Polyacetylene could be doped to tailor its semiconducting properties as was first demonstrated by Alan J. Heeger, Alan Macdiarmid, and Shirakawa [2]. Since then, semiconducting polymers have been developed by leaps and bounds, having implications in all forms of organic electronics such as organic light emitting diodes (OLEDs), organic thin film transistors (OTFTs), organic thin film memory transistors (OTFMTs), and organic photovoltaic cells (OPV) including PSCs, to name a few. Recognizing the growing implication of the discovery of semiconducting polymers, Alan J. Heeger, Alan Macdiarmid, and Shirakawa were awarded the Nobel Prize in Chemistry "for the discovery and development of conductive polymers" two decades later in the year 2000.

#### 2.3 Basic principles

Soon after their discovery, polyacetylene were investigated in solar cells. The earlier forms of these solar cells investigated comprised of the semiconductor polymer material sandwiched between two electrodes with different work-functions; one of the electrodes a transparent conductor that permits light into the device. However, the earlier devices based on polyacetylene resulted in limited power conversion efficiency typically below 0.1% [2]. While more soluble polymers were being developed, it was the understanding of the nature of photoexcited states in organic semiconductors that lead to two subsequent breakthroughs in polymer solar cells that boosted the confidence of the field. Tang et al. discovered that introducing a bilayer of two semiconducting materials like a p-n junction –a heterojunction-- where one semiconductor had a higher affinity for holes and the other for electrons led to creation of a local field that enhances exciton dissociation and increases current [2,3]. Tang reported a power conversion efficiency of 1% which was significant improvement to what was otherwise being reported. Such a result with heterojunction consequently led to the intermixing of two such polymers or a polymer and a soluble fullerene molecule such as Buckminsterfuller or buckyball (C60) in solution before casting into a thin film [3,4]. The resulting interpenetrating morphology-now termed as the bulk heterojunction (BHJ)- paved for advancement of organic electronics in general and PSCs in particular; consequently, the leading to a rapid increase in efficiency of PSCs to 11% today [5].

The basic principle of current generating mechanism in organics solar cells are based on some fundamental differences in comparison to inorganic solar cells such as silicon solar cells. In inorganic solar cells, photon absorption upon illumination of the device results in excitons (bound hole-electrons pairs) with low binding energy (0.1 eV) which can spontaneously dissociate at room temperature into charge carriers. The high charge mobilities allow them to be transported to their respective electrodes to be collected. In PSCs, photon absorption by semiconducting polymer molecules results in excitons with high binding energy (1 eV) due to their spatial confinement to a single polymer molecule domain and have a lifetime of few nanoseconds. Furthermore, the charges when generated in a semiconductor polymers has orders of magnitude lower mobilities than inorganic solar cells. For example, silicon has an electron mobility of 1000 cm<sup>-2</sup> V<sup>-1</sup> s<sup>-1</sup> and a hole mobility of 450 cm<sup>-2</sup> V<sup>-1</sup> s<sup>-1</sup>. In comparison, semiconducting polymers have charge mobility in the range of 10-6 to 1 cm<sup>-2</sup> V<sup>-1</sup> s<sup>-1</sup> [3]. Hence, without an external impetus, the exciton generated in semiconducting polymer rapidly decay to their ground state within a matter of nanoseconds. The introduction of another semiconductor polymer or acceptor molecules with high electron affinity delivers this impetus due to the creation of a localized field between the donor and the acceptor molecules. This is realized when the LUMO of the acceptor molecule is higher than the HOMO of the donor polymer. Bulk hetero-junction morphology (BHJ) allows the most effective and practical method of achieving large interfaces between donor and acceptor module as well as allows the creation of an interconnected pathway, facilitating not only exciton dissociation but also efficient charge transport to the electrodes. Figure 2-1 demonstrates the operational mechanism of PSCs.

Poly(3-hexylthiophene-2,5-diyl (P3HT) and [6,6]-phenyl-C61-butyric acid methyl ester (PCBM) are extensively studied and commonly used donor polymer and acceptor molecule respectively. A comprehensive overview of all photoactive polymers and acceptor molecules could be found elsewhere [4,6]. Similarly, several reviews could be consulted for deeper understanding of device physics of PSCs, for example ref. [7].



Figure 2-1Schematic illustration of operational mechanism of (bulk) heterojunction polymer solar cells. © 2013. Adapted, with permission from ref. [26].

#### 2.4 Device architectures

A polymer solar cell comprise of a thin film of the photoactive material sandwiched between two electrodes of different work functions. One of the electrodes is a transparent conductor from where light is permitted to the photoactive layer. Two different architectures are commonly used: a normal structure and an inverted structure (Figure 2-2). In normal structure, the electron accepting electrode is a low work-function metal, usually Aluminum. Illumination can be achieved either through the top or the bottom electrodes. The terms 'top' and 'bottom' are usually used with reference to the processing sequence on the substrate. The bottom electrode is the first material to be deposited on the bare substrate and the last deposited electrode forms the top electrode, thus sandwiching the thin film photoactive material in in between. In normal structures (sometimes, referred as traditions or conventional structures), the bottom



Figure 2-2 Schematic illustration of PSC device geometries. The differences between normal and inverted architecture is shown. The architectures in either type can be illuminated from either the bottom electrode (a, c) or the top electrode (b, c). Notice that in inverted architectures, an electron transport layer such as ZnO is a crucial addition to the materials in comparison to normal architecture. The back electrode in normal architectures is a low-work Al whereas in inverted structures, higher work function metal such as Ag and Au are employed.

electrode is the transparent conductor, usually ITO. However, several other geometries are also possible including a reverse stacking of the materials as shown in Figure 2-2.

In inverted structure, the direction of charge transport is reversed in comparsion to the normal device structure: the electron accepting electrode is the transparent conductor and the back electrode is higher work function metal which collects holes. Buffer layers provide charge selectively and also contribute to tuning the electric field in the device. Poly(3,4-alkenedioxythiophenes):poly(styrenesulfonate) (PEDOT:PSS) is the most commonly used hole transport layer in both structures. Zinc oxide (ZnO) is of-



Figure 2-3 The equivalent electric circuit that approximates the operation principle of organic photovoltaic cells (left); The IV curve of solar cells is shown in the (left) where all key photovoltaic are demonstrated.

ten used as electron selective buffer layer in inverted structure while LiF is the most commonly employed as buffer layers in normal devices. PEDOT:PSS also functions as a surface planarization on ITO or other electrodes. Inverted structure is most popular when studying large scale low-cost processing of PSCs while normal structure is mostly used in the development of PSCs, for example, in the evaluation of new polymers and other materials. The most popular geometries of the solar cells are shown in Figure 2-2.

#### 2.5 Photovoltaic Characterization

In dark, an organic solar cells acts like a diode. The equivalent circuit that approximates the operation of organic solar cells is demonstrated in Figure 2-3. It comprises of a diode with an ideality factor (n) and a saturation current ( $I_o$ ); a source that induces current upon illumination ( $I_L$ ); a series resistor ( $R_s$ ) that takes into account all the resistances at the interfaces, in the bulk materials, and due to the lateral conductivity or sheet resistance of the electrodes; and shunt resistance ( $R_{sh}$ ) which that takes into account dark current leakage. The corresponding current-voltage (*IV*) curve is also shown in Figure 2-3. In the dark, the IV curve is similar to a diode. Upon illumination, the curve simply shifts on the y-axis with a magnitude that corresponds to current generated upon illumination. The key photovoltaic parameters are Open circuit Voltage  $(V_{oc})$ , Short circuit current  $(I_{sc})$ , Fill factor (FF), Power Conversion Efficiency (PCE), and Maximum Power Point (MPP).

The origin of voltage in PSCs is still a matter of active investigation. While it is affirmed that the voltage is a direct function of the differences in the energy level between the HOMO of donor polymer and the LUMO of the acceptor molecule, there is loss factor whose exact magnitude and origin is still unclear. Empirically it has been found to be 0.3 V and generally attributed to device architecture, including the work function of the electrodes [8,9].

$$V_{oc} = (1/e)\{(E^{donor}HOMO) - (E^{acceptor}LUMO)\} - 0.3 V$$
(1)

e is the elementary charge.

Some other relations between key photovoltaic properties are as follows:

$$MPP = J_{max} \times V_{max} \tag{2}$$

 $J_{max}$  current density and  $V_{max}$  is the maximum voltage on the IV curve. MPP describes the maximum power output possible in the solar cell. The unit of MPP is Watt (W). FF describes the ratio of MPP to that of maximum theoretically possible power generation.

$$FF = \frac{MPP}{J_{SC} \times V_{OC}} = \frac{J_{max} \times V_{max}}{J_{Sc} \times V_{Oc}}$$
(3)

The figure of merit comparison of various solar cell technologies is given by the power conversion efficiency (PCE) which is the ratio of the power of the incident light to that of power generated in the solar cell.
$$PCE = \frac{MPP}{P_{in}} = \frac{FF \times J_{max} \times V_{max}}{P_{in}}$$
(4)

# 2.6 Indium tin oxide

#### 2.6.1 The problem of indium tin oxide in polymer solar cells

Indium tin oxide (ITO) is a metal oxide transparent conductor that is commonly used in most optoelectronic applications such electronic displays. Until recently, ITO was a ubiquitous material in organic solar cells as well. ITO has a high conductivity with a commonly reported sheet resistance of 10  $\Omega^{-1}$  and transmission of greater 80% in the visible region of the solar spectrum. However, the scarcity of indium resources in the world and its high demand from the display industry has created large cost fluctuations and future supply concerns. An official report on the market trend of minerals United States Geological Survey (USGS) suggests that the price of indium has fluctuated anywhere between 10-40% annually in the past 5 years [10]. Apart from the volatility of indium prices, its incorporation in the processing of ITO requires vacuum-based highly energy intensive deposition techniques such as sputtering, thus further increasing the cost footprint of ITO. In the upscaling, ITO substrate needs to be patterned which results in large material wastage. Apart from cost, ITO brings other disadvantages particularly for use in PSCs: its brittle nature limits flexibility and its low thermal expansion coefficient results in poor interfacial compatibility between the organic materials and the ITO surface [11-13].

The initial upscaling experiments on PSCs using roll-to-roll (R2R) processing and subsequent life cycle analyses studies demonstrated that the use of ITO and vacuum processing are not feasible for the low-cost production of PSCs. ITO was observed to incur 90% of the cumulative energy demand (total embedded energy due to materials and processing) in the PSC modules produced [14]. In an industrial setting, the figure may go down but it is still expected to be the prime determinant of cost and environmental footprint in polymer solar cells owing to its processing requirements when the rest of the materials in the polymer solar cells are solution-based and can be processed

at very high throughput. It is therefore crucial to find a low-cost replacement to ITO that bears no supply concerns, is flexible, and is preferably solution-based involving vacuum-free processing.

# 2.6.2 Alternatives to Indium tin oxide

Indium tin oxide is a ubiquitous material in most optoelectronic devices and as such the efforts in finding an alternative to ITO is exhaustive. In general, the alternatives of ITO could be categorized into four broad material groups: 1) nanomaterials; 2) polymers; 3) metals; and 4) metal oxides. Nanomaterials can further be classified into carbon nanotubes, graphene, metal nanowires, and metal nanogrids. These material groups are not mutually exclusive and are often used in some combination with each other. Particularly, Poly(3,4-ethylenedioxythiophene):poly(styrenesulfonate) or PE-DOT:PSS often used in combination with many of these alternatives. Figure 2-4 summaries material categories that are investigated as alternatives to ITO. A comprehensive literature reviews on the alternatives of ITO could be found in our publication [15].

## 2.6.3 Figure of merit qualifications for transparent conductors

Various figure-of-merit (FoM) relationships have been suggested to set a benchmark for transparent conductors in general. In 1976, Haacke first quantified a FoM relationship that combines the two most important properties of a transparent conductor –the transmittance (T) and sheet resistance (R<sub>st</sub>)-- as given in equation 5 [16].



Figure 2-4 Flow-chart illustrating the classification of alternatives to ITO.

$$\phi_H = T^q R_{st} = T^q \sigma d \tag{5}$$

q is an exponent whose value determines the magnitude of transmittance required for a specific application. A q value of 10 results in a transmittance of 0.9 which is sufficient for most application.  $\sigma$  is conductivity and d is the film thickness. This relationship is valid for free standing films and traditionally employed for metal oxide and ultra-thin metal film where sheet resistance is a directly function of film thickness [17,18]. It does not account for percolation driven materials such as carbon nanotubes and nanowires. With the recent surge of interest in finding replacements to ITO, many FoM relationships have been suggested [17,19-21]. One such relationship is the ratio of DC to optical conductivity  $\sigma_{DC}/\sigma_{OP}$  that is found to be even applicable for percolation driven materials [20]. ITO with a sheet resistance of 10  $\Omega^{-1}$  and 90% transmittance results in  $\sigma_{DC}/\sigma_{OP}$  ratio of ~350; ultra-thin Ag and aluminum has a FoM of around 250 and 75 respectively [17]; and carbon nanotubes and graphene 6-14 and 75,



Figure 2-5: A summary of reported properties of TCO alternatives. Solid lines are fits according to some figure of merit equations. The dotted rectangle shows the target region for transparent conductive electrode application. © 2013 Nature Publishing Group. Reprinted, with permission from ref. [17]

respectively; while Ag nanowires have been reported to have superior properties than doped metal oxides with the FoM ratio of 500 demonstrate thus far [22]. Figure 2-4 shows a comparison of different transparent electrode materials based on FoM reported in the literature. It must be mentioned that although the novel transparent electrodes such as Ag nanowires may be able to deliver superior properties in standalone films, their adoption in functional multilayer structures such as in polymer solar cells however has been met with several challenges due to high surface roughness and weak adhesion to substrates [23,24].

## 2.7 Toward low-cost polymer solar cells: Project Targets

The primary goal of this Ph.D. study was to contribute in the development of a robust ITO-free alternative that is employable in the upscaling of PSCs using fast-throughput R2R printing and coating techniques, ideally in ambient conditions. Some specific aims were:

1. Investigating upscaling of ITO-free modules on the path to develop a robust ITO-free process.

2. A PCE of >1% on large-area modules (100 cm<sup>2</sup>) with a P3HT:PCBM based photoactive layer and a geometric fill factor on modules of >60%. Geometric fill is defined as the active area to the total area of a module and has implications on cost (discussed in Chapters 5-8).

3. Understanding and improving stability of the modules with regards to shelf life and indoor and outdoor applications.

4. Cost- and environmental-footprint of the ITO-free architectures must be lower than ITO-based processes such as ProcessOne that our group had previously reported [25].

5. Ultimately, the process should be robust enough to be integrated in ITO-free demonstrator applications.

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# 3. An evaluation of ITO-free architectures for determining upscaling compatibility

#### 3.1 Introduction

Often, the record efficiencies reported of various solar cells are based on devices with small active area and fabricated under controlled laboratory conditions. Particularly, in solutionbased solar cells such as polymer solar cells (PSCs), the majority of the scientific reports (>86%) are based on devices with less than 1 cm<sup>2</sup> active area [1]. For some solar cell technologies such as crystalline Si, the upscaled cells or wafers can realistically have similar efficiency as the record cells since materials and processing in both cases are similar; the former involving silicon and its doping and the latter involving discrete controlled steps. Hence, such devices when upscaled results in minor losses in efficiency. For example, the commercially available crystalline silicon have a record efficiency of 25% on 4 cm<sup>2</sup> area [2]; an upscaled Si cell/wafer (135 mm x135 mm) has a reported record efficiency of 22.5%; and a corresponding silicon solar cell panel (2067 x 1046 cm<sup>2</sup>) with 128 wafers have a reported efficiency of 20% (Maxeon E-series, Sunpower) [2,3]. In PSCs, however, the fabrication of laboratory cells are carried out using 'exotic' materials and processing methods (for example, spin coating, evaporation, atomic layer deposition) that are far removed from the ultimate commercially feasible roll-to-roll (R2R) printing and coating processing that is envisioned for the technology. The performance of PSCs, in terms of both stability and efficiency, is highly dependent on primarily the active material and also crucially on the film and interface properties (for example, donor acceptor morphology, interfaces, roughness, etc.) which in turn are determined to a large extent by the materials and the processing methods employed. Hence, the record laboratory cells efficiency of PSCs (11%), fabricated on small area (0.159 cm<sup>2</sup>) [2] under controlled conditions using 'exotic' photoactive polymers and delicate processing conditions is very far-off from an all-ambient processed module (active area efficiency of ~2%) fabricated in a commercially-likely conditions [4].

Hence, it is very important to evaluate the upscaling compatibility of laboratory scale prototypes before upscaling. A holistic evaluation should be based on the photovoltaic performance, stability, and materials and processing methods incurred in the prototype to determine if upscaling is warranted. To reiterate from Chapter 1, the ultimate aim of PSCs is low-cost energy production which, given the lower lifetime and expected efficiency of PSCs, will be best accomplished using ambient processing on flexible substrates and ideally using only benign solvents such as water. The use of inert conditions, clean room, or vacuum processing, and the use of rigid substrates such as glass have not been dismissed while it is likely that their use will imply that the technology requiring these will be less competitive unless balanced by higher performance in some aspects (e.g., stability and photovoltaic properties, technical yield, material parsimony).

Based on this frame of reference, this chapter aims is based on a study in which the upscaling compatibility of five different ITO-free architectures based on their photovoltaic properties, stability, and materials and processing conditions were evaluated. To focus on the architectures, the active material was controlled in all the devices. The devices are studied in detail. The aim was to find the best architecture suitable for low-cost upscaling. Such a process can be thought of as a screening process for selecting the best ITO-free device architecture that is worth investing resources in their upscaling. The subsequent chapters are based on the upscaling of device architectures based on the recommendations from the study presented in this chapter.

#### 3.2 The Architectures

Five different ITO-free devices were contributed by four different institutions--ECN (Netherlands), ISE (Germany), Holst Center (Netherlands) and DTU (Denmark)-- each having a rich experience in their respective devices supplied to this study. As such, all devices compared in this work are optimized and can be regarded as the state-of-the art of their respective design. Schematic illustrations of the device architecture are shown in Figure 3-1. An ITO-based inverted device was also included as reference. All ITO-free devices are based on an inverted structure apart from the Holst-type device which is based on a normal or conventional structure.



Figure 3-1 Schematic illustration of the layer stacking in five different ITO-free architectures evaluated. ITObased reference device (REF) is also shown.

# 3.3 Materials and Processing

Table 2-1 provides information on materials, suppliers, deposition methods, and deposition conditions for all device architectures. Layer thicknesses are given in the schematic illustrations in Figure 3-1. Further details can be found in the literature cited under the following subheading that briefly describes the architectures studied.

# 3.3.1 Reference ITO-based devices

The ITO on glass substrates (10  $\Omega$  $^{-1}$ ) were first thoroughly cleaned with ultra-sonication in isopropanol and water and dried at 200 °C. The functional layers were then spin-coated at 1000 rom in the sequence: ZnO; P3HT:PCBM (1:1 *wt:wt* ratio in cholorbenzene with a total concentration of 60 mg ml<sup>-1</sup>); and PEDOT:PSS (dilution in isopronanol in 2:1 v/v ratio). ZnO and PEDOT:PSS deposition were followed by annealing step at 140 °C -5 minutes. Finally, the Ag electrode was evaporated.

# 3.3.2 NORM

NORM devices are based on normal structure that directly replaces ITO with a composite current collection grid comprising a inkjet printed metal grid overlaid by inkjet printed highly conductive (HC) PEDOT: PSS. P3HT: PCBM (1:1 *wt:wt* ratio with a net concentration of 52 mg ml<sup>-1</sup> in 1, 2-dichlorobenzene) is then spin coated at 1000 rpm. Finally, LiF and Al were consecutively evaporated to complete the device stack [5,6].

# 3.3.3 ASP

ASP devices utilize the composite electrode as described for NORM structure in an inverted architecture. ZnO is then spin coated at 1000 rpm on the Ag grid/PEDOT:PSS composite electrode to form the electron selective layer followed by P3HT:PCBM (same as NORM). PEDOT: PSS (1:1 dilution with Isopropanol) forms the hole the transport layer that is spin coated at 1000 rpm and dried at 120 for 5 minutes. Finally, Ag grid is screen printed. It has been found crucial to deposit one layer (often ZnO) in the glove box and the device requires activation by application of high voltage after processing.

## 3.3.4 ALCR

ALCR devices utilize a low work function metal substrate Cr-Al-Cr as electron contact as previously reported [7]. The purpose of the first Cr layer is for ensuring good adhesion to glass and to protect the highly reactive Al and can be omitted if a substrate conditioned for Al deposition such as when Mitsubishi RNK PET film is used. The second Cr layer acts as an electron selective layer while also providing protection for the Al layer. The photoactive layer of P3HT:PCBM (20 mg:14 mg in 1ml of o-Xylol) is then deposited on the Cr layer followed by a hole transporting PEDOT:PSS layer and a suitable work function metal contact such as Ag or Au. In this case, Au was used as the second metal contact.

## 3.3.5 AGNP

AGNP is an inverted ITO-free device that utilizes a solution processed semi-transparent Ag as the front electrode developed under this PhD study [8]. The rest of the stack is exactly similar to the REF device (section 3.3.1)

#### 3.3.6 WT

The wrap through (WT) device architecture known from inorganic solar cells was redeveloped and adopted for flexible organic solar cells by Fraunhofer ISE [9]. A parallel circuitry is formed by a so called wrap through (WT) circuitry. The ALCR device structure (described in section 3.3.4) is built on a thin plastic substrate, where the Cr/Al/Cr contact forms the negative terminal of the solar cell. The complete stack including the substrate is perforated and a second metallized substrate is laminated to the backside of this device. The last deposited material, PEDOT:PSS, is led through the perforated vias in the device to the second metallized substrate, which collects the current from the PEDOT:PSS and forms the positive terminal. In this way, an easily scalable WT device structure is accomplished.

### 3.4 Encapsulation method

One method of encapsulation was adopted across all device structures to limit variability in stability due to barrier properties of the encapsulating material and the encapsulation method. The devices were encapsulated by sandwiching each devices between two glass slides (the substrate and encapsulation glass) using a UV curable DELO-ALP adhesive (LP655). The glue was homogeneously distributed by sliding two foldable clips with some force from the centre of the device toward the edge. Finally, the device with the adhesive was exposed to UV radiation for a short time under a solar simulator (1 min with consequent heating to around 70 °C) or under UV light to achieve curing of the adhesive. For DTU ProcessH device, the PET substrate was mounted on a glass substrate using the same adhesive. The rest of the encapsulation was similar to all other devices.

ALCR Sigma Aldrich Evaporation Vacuum		
Electrode 1 ASP Ag Suntronic U5714 Ink jet printed	Ambient	
(electron contact) AGNP Ag Kunshan Hisense Electronic (SC-100). Spin coated Ambient		
REF ITO Lumtec/Naranjo substrate As received/sputter coated Vacuum		
ALCR Cr Sigma Aldrich Evanorated Vacuum	Vacuum	
NORM LIF		
Electron transport/hole blocker ASP In house prepared nanoparticles in IPA N2		
AGNP ZnO In house prepared papoparticles Spin coated Ambient	Ambient	
REF Amblent		
ALCR Reike Metals Inc. 4002e N <sub>2</sub>		
NORM	Ambient	
ASP P3HT:PCBM Playtrapias Playage OS2100, Salarna P.V. Spin coated Ambient		
AGNP Plextronics Plexcore OS2100: Solenne B.V.		
REF		
ALCR Clevios F010 and Agfa customized Formulation Evaporated N <sub>2</sub>		
NORM	Ambient	
Agra Orgacon EL-P 5015 Spin coated Ambient		
AGNP Agfa Orgacon EL-P 5010		
REF Agfa Orgacon EL-P 5010/5015		
ALCR Au Sigma Aldrich Evaporated		
Electrode 2 NORM AI Suntronic U5714 Inkjet printed Vacuum		
(Hole contact) ASP Toyo Rexalpha RA FS FD 018 (paste) Screen printed Ambient		
AGNP Ag	Vacuum	
REF Vaporated vacuum		
ALCR		
NORM Glass -		
Substrate ASP		
AGNP PET Melinex PET		
REF Glass -		

# Table 3-1 Materials and processing specification of the various architectures investigated.

#### 3.5 Photovoltaic properties:

To allow a logical comparison of the architectures, it is necessary to control the photoactive material. P3HT:PCBM was used in all architectures as it is a commercially available material. Since independent laboratories were involved, a round-robin method was adopted in the evaluation of photovoltaic performance of the solar cells. Under a round-robin study, all devices are collected at one institution and the first round of measurements is initiated. Then, the devices are sent around at the participating institutions in rotation for photovoltaic measurements. Finally, the devices are sent back to the starting institution where the last measurement is carried out. For this study, the devices were measured at four institutions following the scheme shown in Figure 3-2. All devices were masked to achieve an active area of 1 cm<sup>2</sup> which was proven more reliable than a smaller active area. In a preliminary round robin investigation, ITO-based reference devices with two different active areas  $-1 \text{ cm}^2$  and 0.36 cm<sup>2</sup> – were evaluated. Devices with smaller active area (0.36 cm<sup>2</sup>) were found to show high level of disagreement, particularly with J<sub>sc</sub> measurements. At some institutions, the 0.36 cm<sup>2</sup> devices showed  $J_{sc}$  values that were significantly higher (12 mA cm<sup>-2</sup>) than theoretically expected. A 400 nm thick P3HT:PCBM active layer cannot realistically give more than 12 mA cm<sup>-2</sup> even at 100% internal quantum efficiency according to a modeling result that evaluates photon absorption under AM 1.5G by P3HT:PCBM in a similar device structure [10]. The exaggerated current could be caused by interplay of small aperture area, thickness of the mask, the uniformity and the diffuse content of the light from the lamp of the solar simulator—all of which may result in overestimation of photocurrent [11]. As a result of this uncertainty with smaller aperture area, 1 cm<sup>2</sup> was selected for photovoltaic and stability measurements of the ITO-free architectures. It must be noted that 1cm<sup>2</sup> is also the optimal width of cells for ITO-based substrates in a serially integrated module- a module design used in the upscaling (introduced in the next chapter). The round-robin data of ITO-based reference devices are given in the Appendix 10.2 (Table A-1).

All ITO-free were fabricated with an area of 1 cm<sup>2</sup> except WT which was supplied to this study with an area of 2.2  $\text{cm}^2$ . All devices (2 devices of each architecture) were masked with an aperture of  $1 \text{ cm}^2$  and were studied in the round-robin method. In the absence of certification, a round-robin is a facile method to gain consensus on claimed photovoltaic properties and establish credibility. Devices were measured at 1 sun illumination (1000 W m<sup>-2</sup>; AM1.5G) at all institutions while only DTU had the facility to conduct measurement under low-light conditions (0.1 sun). All institutions demonstrated good agreements on the photovoltaic performance of all the architectures under 1 Sun with a maximum standard error in PCE of 10% except for WT. Figure 3-3 shows the distribution of PCE of all the devices studied under the round-robin while standard error is listed in Table 3-2 (See Appendix 10.2 for the complete data). This level of disagreement in PCE is mostly attributed to the variation in J<sub>sc</sub> for which a standard error of ~12% is observed; V<sub>oc</sub> and FF have the highest consensus with a maximum standard error of 3% and 5%, respectively. While J<sub>sc</sub> could vary to some extent because of degradation over the course of the round robin studies (25 days), however, other factors such as the light sources and their calibration, operator's handling, etc. may all contribute to this variability. Nevertheless, the 10% standard error in PCE is the highest consensus reported of any round robin study conducted on PSCs [12,13]. Furthermore, the relative difference among the various architectures remained the same at all stages of round-robin measurement. WTs devices mark a large uncertainty ~30% in its performance, has a different active area, and were not considered for further evaluation. Although WT devices represent a highly scalable design but at this stage but the processing was not yet robust enough at the time of this study. They are continually being developed at the home institution (ISE Fraunhofer) and it is likely that in future they will emerge as a successful architecture.



Figure 3-2 Schematic diagram of the round-robin procedure followed for this study. The blue lines represents the ITO-free architectures submitted while the paths in black shows the rotation in which the ITO-free device were measured at different locations. The numbers is brackets denote the sequence and the number of measurements carried out.

With the consensus gained in the round robin study, all devices can be comparatively evaluated. The key photovoltaic parameters under 1 sun (1000 W m<sup>-2</sup> AM 1.5G) and under low-light/indoor conditions (0.1 sun; 100 W m<sup>-2</sup>) is given in Table 3-2 and the corresponding IV curves are shown in Figure 3-3. Despite the common photoactive materials and the active area, large differences in the photovoltaic performance are observed. ALCR emerges as the best architecture in terms of photovoltaic performance with PCE equaling to- or greater than- the reference ITO-based cells under 1 sun and low-light, respectively. On the other hand, AGNP have the lowest PCE under 1 Sun and low-light conditions. To account for the observed differences in the PCE of the various architectures, it is necessary to delve into the reasons for the variation in short circuit current density (J<sub>sc</sub>), Open-circuit voltage (V<sub>oc</sub>) and fill factor (FF).



Figure 3-3 Round robin measurement of PCE of reference devices and the ITO-free architectures (two cells each) at four institutions is shown. The ovals are intended as aids for visualizing the spread in data. The legend corresponds to the institutions in Figure 3-2 (a); and the IV curves of the devices (b). The IV curves are from the first measurement during the round robin study.

#### 3.5.1 Short circuit current density

The largest variation among the different architecture is observed in J<sub>sc</sub>. The variation in J<sub>sc</sub> is mostly a direct consequence of the differences in the optical transmission of the different transparent electrodes (TE) employed in each architecture (Figure 3-4). Nevertheless, there are certain differences in J<sub>sc</sub> among the various architectures that the differences in transmittance of the TE do not account for. For example, ASP and NORM employ the same TE yet ASP have lower J<sub>sc</sub> than NORM. J<sub>sc</sub> in PSCs is determined not only by the photons hitting the photoactive layer (PAL) but the multitude of mechanisms that take place thereafter that determine the final charge carrier harvest. Broadly, these mechanisms involve exciton generation, diffusion, separation, and charge transport. These mechanisms are not only dependent on the photoactive material, its morphology, and the transparent electrode but also on the architecture itself including other constituent materials, their placement in the architecture, and their characteristics (layer thickness, optical properties, layer quality, electrical interfaces, etc.). To account for how current generation occurs in the four architectures considered here, an external quantum efficiency data (EQE) can provide valuable information.

EQE informs the conversion efficiency with which photons incident upon a solar cell gets converted into electrons. In other words, it is the electrons collected per photon absorbed and is defined by [14]:

$$EQE = \eta_{abs} \times \eta_{exharvest} \times \eta_{CT} \times \eta_{GS} \times \eta_{CC}$$
(1)

where *abs* is the absorption efficiency of the photons by the photoactive material, *exharvest* is exciton harvest, *CT* is charge transfer, *GS* is germinate separation and *CC* is charge collection.

In an ideal scenario, EQE spectra should reflect the absorption trend of the photoactive polymer; that is, the highest absorption region of the photoactive material should correspond to the maximum peak region in the EQE spectra (a symbatic response) due to highest amount of charge carrier generation possible in this region. This is most realistically achievable in an architecture with thick photoactive layer when: 1) TE has a uniform transmission in the absorption range of the photoactive polymer and 2) TE is the electron collecting electrode (cathode) such that the electrons generated in the most photoactive region in the photoactive layer, that is, the interface of the PAL facing the TE, is readily collected by the cathode. A symbatic response is clearly discernible in the REF. device while it is less so pronounced in ALCR, ASP, and AGNP (Figure 3-4). The differences in the EQE spectral shape of the inverted structures can be explained by considering the vertical gradients in the photocurrent generation efficiency and/or recombination. In thick P3HT:PCBM layers, incident photons with energy corresponding to the peak absorption region of P3HT (around 500 nm) is absorbed within the first 100 nm from the TE (henceforth, term as the "most potential region"); while the remaining photons away from absorption peak of P3HT (i.e., in the 400 and



Figure 3-4. The transmission profile of the transparent electrodes is shown (left). ALCR transmission profile is not available but it is expected to be similar to ASP and NORM. The absorption of P3HT:PCBM is shown for reference. The inset shows a rescaled transmission profile of the TE used in AGNP. The EQE curves of the various architectures are shown (left).

600 nm regime) are more uniformly absorbed throughout the thickness of the layer [15].

ITO has a uniform transmittance in the visible spectrum. As a result, a symbatic photo-response is seen in the reference cells and the shape of the EQE spectra is similar to the absorption profile of P3HT with the peaks in EQE graph corresponding to the peaks in P3HT absorption spectrum except for the peak at 365 nm. The small peak at 365 nm is attributed to the ZnO:P3HT interface that forms an additional photoactive interface and contributes to current in this region. ZnO is an n-type semiconductor with a band gap of 3.42 eV (~365 nm) that directly corresponds to the peak at 365 nm in the EQE spectrum.

In AGNP devices, current harvest in the most potential region is hampered by the trench in the transmission of the TE electrode. EQE graph indicates that most electrons are collected away from the most potential region, that is, deeper into the PAL layer toward the back of the cell. This corresponds well with the transmittance profile of the TE used in AGNP, a semitransparent Ag electrode, that has a significantly higher transmittance in the ~ 400 and ~ 600 region than in the 500-550 nm region (Inset in

Figure 3-4 *left*). Furthermore, the opposite electrodes are similar in AGNP which reduces in electric field within the device, suppressing charge carrier drift velocity, and inducing higher recombination.

ALCR devices are an up-side down or directly inverted NORM. In comparison to other architectures, ALCR employs much thinner active layer which is accommodated by the evaporated Al/Cr bottom electrode due to its low roughness. As a result, the photocurrent from the most potential region seems to be efficiently transported to the Al/Cr electrode. The reflection from the Al/Cr further enhances current generation. The transmission spectra is not available but a similar graph as the ASP and NORM is expected due to the same PEDOT:PSS thickness. The dip in the current collection between 350-400 nm is unusual and is attributed to poor ordering in the P3HT:PCBM blend in the this architecture [16,17]. This could be induced by the P3HT:PCBM ratio which in ALCR was 1.43:1 (wt/wt) while in all other architectures was 1:1 (wt/wt).

In spite of the same TE employed in both ASP and NORM devices, much lower current is harvest in ASP devices than the NORM devices. This is partly due to the additional ZnO layer in the path of incoming light that represent scattering sites for the incident photons. Unlike in NORM device, the lack of reflective back electrode further contributes to lower photocurrent generation in the ASP devices. Moreover, the screen printed back electrode in ASP device causes damage to the photoactive layer beneath the screen printed Ag lines due to the diffusion of the solvent from the screen printing grid into the device as clearly evident in Figure 3-5. NORM devices employ evaporated back electrode and therefore do not suffer such loss. Lastly, ASP device employ symmetric Ag grid/PEDOT:PSS electrodes across the photoactive layer results in reduced charge carrier drift, inducing further recombination. All these factors impede current harvest in ASP devices than in NORM devices. In ASP, the problem of screen printed Ag ink is an avoidable challenge and can be improved by using better screen printing inks such as UV curable ones [4], by other printing techniques such as



Figure 3-5 LBIC images of ASP device. The arrows show shading losses due to the Ag grid used in the transparent electrode. A one-to-one correspondence of each Ag grid line in the transparent electrode to the lines in LBIC image is shown (arrows of the same color point to the same grid in both image). The remaining grid lines are destruction of the photoactive polymer due to the solvent diffusion from the screen printed Ag grid back electrode.

inkjet printing that is observed to eliminate this problem [18], and/or by optimizing PEDOT:PSS formulation.

NORM architecture is based on normal or 'conventional' device structure. It uses the same TE as ASP but the polarity of the architecture is reversed in NORM in comparison to ASP. This explains the antibatic characteristic of the NORM devices in comparison to ASP as is evident in the dip in the peak absorption region of P3HT in NORM architecture. The charge carriers produced in the most potential region need to transverse through the bulk of the photoactive layer to be collected by the electrode and therefore current from this region is visibly suppressed due to recombination. Electrons are thus more efficiently produced in toward the back of the PAL where the electrons are more readily collected and also enhanced by the reflection from the back electrode. All these factors render more charge carrier harvest in NORM architecture than in ASP.

# 3.5.2 Open Circuit Voltage:

Open circuit voltage in PSCs is directly related to the energy difference between the HOMO level of the donor polymer and the LUMO of the acceptor materials with a loss factor of ~0.3; the origin and the exact magnitude of the loss factor is a matter of active investigation [19-22]. Electrodes have a minor influence when they form ohmic contact. Ohmic contacts are formed when there is no energy barrier (or small barrier >0.2 eV that can be overcome by thermal activation) in the transport of charge carriers to their respective electrode). That is, when the work-function of cathode (negative terminal of the device) is lower than the LUMO of the acceptor and the work function of the counter electrode is higher with respect to HOMO of the donor polymer. When both electrodes form ohmic contact with the active material, the electrode materials have negligible influence on the device  $V_{oc}$  [19]. Figure 3-6 shows the energy level diagram of all the architectures based on literature-collected values of work functions.

Since all architectures employ the same photoactive layer (P3HT:PCBM) and form ohmic contact at both of the immediate interfaces across the PAL (Figure 3-5), it is not surprising that  $V_{oc}$  in all architecture is similar in all architectures except ALCR. Especially, the interfaces across the photoactive layer in ASP, AGNP, and ITO reference cells are exactly similar which is why their  $V_{oc}$  are similar and within standard deviation. ALCR has significantly higher  $V_{oc}$  and this effect can be elucidated by a comparison with NORM architecture.

Architecture	Measurement	J <sub>sc (mA cm</sub> )	V <sub>oc (V)</sub>	FF (%)	PCE (%)
	1 sun	7.29 (7.18)	0.58 (0.93)	63.02(1.77)	2.65 (6.28)
ALCR	Indoor	0.84	0.52	69.63	3.0
NORM	1 sun	7.15(10.23)	0.53 (1.04)	61.58 (0.89)	2.34 (10.33)
NORIVI	Indoor	0.78	0.45	68.83	2.4
	1 sun	6.10 (9.57)	0.53 (1.36)	54.04 (2.18)	1.75 (10.55)
ASP	Indoor	0.74	0.449	60.72	2.02
	1 sun	3.81 (5.70)	0.54 (1.02)	56.26 (0.79)	1.16 (5.91)
AGNE	Indoor	0.41	0.47	54.57	1.044
WT	1 sun	5.89 (21.59)	0.57 (2.64)	35.50 (6.71)	1.19 (22.58)
DEE	1 sun	8.47 (11.55)	0.55 (1.85)	40.13 (4.88)	1.86 (8.87)
NEF	Indoor	1.0	0.4821	62.24	2.98

Table 3-2 Key photobvoltaic parameters of the different architectures under 1 Sun illumination (1000 W  $m^{-2}$  AM1.5G) and under indoor conditions 0.1 Sun (100 W  $m^{-2}$ )

ALCR and NORM have the similar interfaces and electrode materials. The difference is then attributed to several factors: firstly, the work function at the PEDOT:PSS is dependent on the sequence of deposition of PEDOT:PSS with respective to the absorber layer. PEDOT:PSS deposited on top of the absorber layer as in the case of ALCR has a higher work function than when deposited under the absorber layer as in NORM devices [19,23]. As a result, ALCR has a higher work function difference across its electrode. Secondly, LiF/Al is evaporated on active material which may increase trap states in NORM devices while Al/Cr forms the bottom electrode in ALCR, upon which organic materials are spin coated in ambient temperature. Finally, 1 nm of LiF is known to aggregate while Cr form more interconnected network, thus resulting is a larger insulator (oxidized Al)/PAL interface in NORM than in ALCR [24]. These effects explain why V<sub>oc</sub> in ALCR is slightly higher than in NORM.



Figure 3-6 Energy level diagram of all the different PSC architectures.

## 3.5.3 Fill Factor

The loss in fill factor is a direct consequence of low shunt resistance and high series resistance. In organic solar cells, these parasitic resistances can originate from several different factors. Low shunt resistance can originate from micro-shorts in the device due to, for example, the interconnection between positive and negative PEDOT: PSS layer in ASP architecture or spikes in one metal electrode intercalating into the opposite electrode. Shunts are usually caused by manufacturing defects. On the other hand, series resistance may originate from contact resistance between all interfaces, bulk resistance in PAL layer or the other material layers, and the lateral conductivity/sheet resistance of the electrodes. Series resistance (R<sub>s</sub>) and shunt resistance (R<sub>sh</sub>) for all the architectures extracted from their respective IV curves in Figure 3-3 is listed in Table 3-3. In general, PSCs for both indoor and outdoor applications, a shunt resistance of 85 k $\Omega$  cm<sup>-2</sup> or higher and a serial resistance of 3  $\Omega$  cm<sup>-2</sup> or lower is recommended to prevent large power loss [25]. All ITO-free architectures have lower R<sub>s</sub> than ITO. This is a direct consequence of lower sheet resistance of the new electrodes in the ITO-free architectures used in place of ITO. ITO has a sheet resistance of  $10 \ \Omega^{-1}$  while both electrodes in all ITO-free architectures have less than  $1 \ \Omega^{-1}$ . In all, for outdoor application, series resistance is more crucial as high series resistance causes dramatic loss in PCE due to power loss (P<sub>loss</sub>~Rl<sup>2</sup>). It has been shown that under 1 sun, a shunt resistance of 1 k $\Omega$  cm<sup>-2</sup> or higher is sufficient while a serial resistance of 3 k $\Omega$  cm<sup>-2</sup> or lower is required to prevent power losses [25]. All ITO-free architectures demonstrate higher than 1 k $\Omega$  cm<sup>-2</sup> of R<sub>sh</sub> and lower series resistance than the reference device. Hence, all ITO-free architectures are suitable for outdoor applications, if not more so than ITO-based REF.

On the other hand, the R<sub>sh</sub> of all ITO-free architectures is higher than ITO. ALCR has the highest R<sub>sh</sub> which is explained by the evaporated substrates that are less prone to defects. In printed metal electrodes as used in NORM, AGNP, and ASP, presence of spikes the Ag film leads to shunting [26]. The reduced R<sub>sh</sub> of ASP in comparison to others could be due to Ag migration through diffused solvent from the screen printed silver as seen in LBIC image (Figure 3-4)[27]. High R<sub>sh</sub> is more important than Rs for indoor applications [25] and from this point of view; the ITO-free architectures are suitable for indoor applications.

	ALCR	NORM	ASP	AGNP	ITO. Ref
FF (%)	63.02	61.58	54.04	56.26	40.13
$R_s (\Omega \text{ cm}^{-2})$	4.65	7.38	6.88	3.84	10.97
$R_{\rm sh}(K\Omega~{\rm cm}^{-2})$	2.28	1.843	1.15	1.86	0.25
Sheet resistance of					
bottom/top electrode	<1/<1	1/1	1/<1	5/<1	10/<1
$(\Omega \square^{-1})$					

Table 3-3 Factors determining FF: Series resistance ( $R_s$ ) is calculate by taking the inverse slope on IV curves between 0.9-1.0 V; Shunt resistance ( $R_{sh}$ ) is determined by inverse of the slop between - 0.6V to 0.6V; and sheet resistance measured by a four point probe.

# 3.5.4 Summary of photovoltaic properties

From the purely architectural point-of-view, ALCR represents a well-rounded architecture in terms of its materials, their surface and film properties, and the processing sequences— all of which enable ALCR architecture to higher Jsc, Voc, and FF than any of the other architectures. It presents a >2.5% efficiency in both indoor and outdoor conditions, which remains higher than the ITO-based reference device. Among the rest, NORM and ASP also exhibit similar performance to ITO-based reference device and may be suitable over ALCR if they bring competitive advantage in stability or processing. AGNP and WT device represents the lowest PCE (around 1%), AGNP represents the most robust technology in that it has the lowest standard error in the measurements conducted over the round-robin study (~5%) while WT represents the other end of the spectrum with a standard error of (>20%). Hence, AGNP could be investigated further for upscaling compatibility while WT is deemed not yet robust to pursue upscaling on a large scale. The detailed comparative analysis is important for it elucidates the implications of materials and processing choices on the devices performance and highlight the opportunities for improvement in some architectures or sacrifices that might be required in others once processing is carried out with a common goal low-cost processing.

## 3.6 Stability

The real world application of PSCs demands sufficient stability under operational and storage conditions to justify its use as a power source in various applications. The International Summit on Organic photovoltaic Stability (ISOS) has laid out a framework for stability testing under various operational and shelf-life conditions [28]. Accordingly, the stability of the P3HT:PCBM based PSCs in normal and inverted architectures have been reported by independent groups [29-33].

A PSC is as stable as its weakest link (material or interface) in its stack and therefore all material components play a crucial role in determining the overall stability of a complete solar cell. A holistic stability evaluation of the ITO-free architectures is essential in-order to make informed decisions about the choice of architecture for upscaling. Hence, the ITO-free architectures have been evaluated based to ISOS protocols under several standard and accelerated testing conditions as defined in Table 3-4. The tests are carefully selected to represent diverse real world conditions, representing locationand application-specific stability. For example, for indoor application in ICT, stability under indoor lighting conditions is more relevant than under 1 sun conditions (1000 W m<sup>-2</sup>, AM 1.5). Such an evaluation allow for identification of causes of device failure and

Category	Light (Sun)	Temperature (°C)	Relative Humi- dity (%)	Deviations from ISOS Pro- tocols
ISOS-D-1	0	25	20-35	-
ISOS-LL	0.1	30	10 - 15	-
ISOS-L-1	1	37±3	10 - 15	Temperature was control- led
ISOS-L-2	1	80	10 - 15	Testing was performed in Room environment
ISOS-L-3	0.7	65	50	Modules were kept at open circuit

Table 3-4 Stability test conditions accor	rding to ISOS protocols employed in this study
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#### Chapter 3 - 2BAn evaluation of ITO-free architectures for determining upscaling compatibility

in making concrete recommendations on the improvement in device architectures for improving stability.

Degradation of a PSC can be complex with several mechanisms at play in tandem. The photoactive polymers decay when subjected to chemical and physical stresses. Chemical stresses induce decay via photo-oxidation, thermo-oxidation, photolysis and thermolysis. In P3HT films, photo-oxidation is the prominent degradation mechanism [34]; thermolysis or thermal decomposition is negligible below 400  $^{\circ}$ C [34,35]; photolysis in the absence of oxygen takes place in the time scale of years and P3HT estimated to retain 80% of its absorbance properties up-to 5 years [36]; and thermooxidation is temperature dependent. Based on the processing and operational temperature expected of PSCs on low-cost flexible substrate such as PET, thermo-oxidation has been shown to be significantly slower process than photoxidation. Manceau et al. found that the degradation rate of P3HT when treated with 100 °C is several orders of magnitude slower than photolysis of P3HT when subject to UV below 300 °C [37]. Apart from UV light and the presence of oxygen, the photo-oxidation of P3HT is influenced by other environmental conditions, particularly humidity, ozone, and temperature [34]. Similarly, metal used in electrodes can decay due to oxidation as well as due to various organo-metallic chemistry [38-40]. Physical stress, on the other hand, is more relevant to the mechanical handling of a finished product and induces failure or loss in performance in a solar cell due to bending under tension or compression, shear stress, delamination etc [41-43]. Interfacial mechanical stress may also be induced intrinsically due to, for example, morphological evolution of photoactive polymer [44]. Morphological stability of PSCs is also another issue that depends on the chemistry of the photoactive materials as well as on the processing. Generally, chemical degradations relates to the intrinsic stability of the photoactive polymer and other material components, which is primarily dependent on their chemical structure and secondarily on their processing and their operational or storage environmental conditions. Under uncontrolled ageing environment, a confluence of several or all of these mechanisms is

likely to take place. The mechanisms of degradation in PSCs are holistically reviewed in various publications [45,46].

## 3.6.1 Stability under storage conditions

In this evaluation, the ITO-free architectures are stable in dark storage (ISOS-D-1) which is a testament to the fact that thermo-oxidation of the active material is negligible at room-temperature and that all materials and interfaces in all architectures under dark storage conditions are stable. At the end of 1700 hours, architectures are within 80% of its initial PCE (Figure 3-7). Due to the manual measurement, there are large fluctuations (up to 10%) between each measurement points and it is hard to discern a decaying trend if there is any. However, AGNP is disguisable among the rest as it shows a rather stable PCE despite the manual measurements and may point toward its superior stability than the others. For a complete picture, the operational stability of the various architectures will elucidate the difference in the stability of various architectures.

## 3.6.2 ISOS-LL

Under operational conditions, PSCs are usually observed to decay in two stages: an initial exponential decay known as the "burn-in" is followed by a linear degradation trend as schematically represented in Figure 3-7. Lifetime is then defined by the time it takes for the PSCs to degrade by 20% (T80) from the onset of the linear decay (T100). The origin of burn-in period is still widely disputed. In general, burn-in is caused by a degradation mechanism that becomes self-contained or cease over the course of ageing. Because it can originate from various mechanism, the magnitude of burn-in period ranges from 100 hours to over 1000 hours [27,47]. Both have implications on the effective efficiency of a device in real world applications and therefore, the reported efficiency of various architectures must account for loss in burn-in, if significant.

A characteristic decay pattern is observed in all devices when aged under indoor lighting conditions (ISOS-LL). Common to all devices is that they have a burn-in lasting

~100 hours. However, the efficiency loss in this duration vary among the various architectures with ALCR, NORM, REF., AGNP and ASP showing a loss of 20%, 22%, 25%, 28%, and 33% respectively (Appendix 10.2, Figure A-1). Further analysis of the degradation pattern of Voc, Jsc, and FF reveals that the burn-in has different origins in different architectures which could be attributed to their materials and processing. All devices show a degrading J<sub>sc</sub> at haphazard relations to each other and it is attributed to the lack of edge sealing and the differences in adhesive thickness which lead to loss of active area at different rate in the various architectures. ALCR shows no degradation in FF and V<sub>oc</sub> which is attributed to the fabrication and encapsulation in nitrogen environment. On the other end of the spectrum, ASP shows the highest loss in FF and  $V_{oc}$ . The loss in V<sub>oc</sub> and FF among the various architecture can be inferred from their fabrication environment and the use of PEDOT:PSS layer on top of the PAL layer. PE-DOT:PSS deposited on top of P3HT:PCBM has very poor adhesion with PAL and is also highly hygroscopic [45,48]. Accordingly, ALCR fabricated in nitrogen shows the least burn-in degradation. NORM devices, fabricated in air and no PEDOT:PSS on top of PAL stands second to ALCR. Both AGNP and ASP have thick PEDOT:PSS layer on top of PAL and are processed in ambient conditions. Hence, they show the most burn-in loss. The use of vacuum in deposition of the top electrode in AGNP and ITO could reduce the



Figure 3-7: (a) the degradation pattern under storage conditions is shown (ISOS-D-1). (b) Illustration of the a typical decay pattern demonstration key lifetime determinants: T100 is the onset of linear decay while T80 marks the end of the lifetime. ©2013 Amercian Chemical Society. Adapted,

concentration of adsorbed moisture in PEDOT:PSS which explains their lower amount of degradation in  $V_{oc}$  and FF than the ASP [49].

Once the degradation agents introduced in the layers during the processing runs out, the burn-in effect on  $V_{oc}$  and FF extinguishes and the devices appears to be stable thereafter. The fluorescence lamps have very little UV emission and device will remains stable beyond 1000 hours. Due to large intensity fluctuations, the extrapolation of lifetime is conducted between 600-700 hours (~400 data points). The two arbitrary points were selected because the intensity fluctuation of the lamps (as judged from sudden  $J_{sc}$  fluctuations) between these two points were less than 5%. This reveal stability (T80) of 1880, 2200, 3600, and 10,700 hours for ITO-REF, NORM, ALCR, and AGNP respectively. ASP do not degrade during this time indicating infinite stability unless limited by catastrophic failure and this is attributed to better encapsulation than the others. In future, measurement of lamp intensity is recommended for more accurate estimation of lifetime. ITO-REF. Is expected to have some contact problem as revealed by the fast degradation of FF. Nonetheless, regardless of where the regression is performed, the comparative stability of the architectures remains the same and that AGNP and ASP show the highest stability while NORM shows the least which is at-





Figure 3-8. The degradation trend/stability of the different ITO-free architectures under various operational conditions. ITO reference devices are also shown for comparisons.

tributed to oxidation of aluminum. The combination of very limited UV content in the fluorescence light and the room temperature limits degradation of the photoactive polymer. Hence, all architectures are suitable for indoor applications from a stability perspective.

### 3.6.3 ISOS-L-1/-2/-3

The devices tend to degrade faster when subjected to higher illumination, temperature, and humidity as in ISOS-L-1/-2/-3 than under low-light conditions (Figure 3-8). NORM devices cannot sustain any of these ageing environments and completely degrades within 100 hours in all these tests. The rapid decay in the remainder of the architectures is due to encapsulation failure and the lack of UV filter in the glass barriers used. Only a comparative and qualitative evaluation of the stability can be made among the various architectures. AGNP device are the most stable of all followed by ALCR. It was observed that AGNP has constant  $V_{oc}$  and FF over the ageing duration among all architectures in both ISOS-L-1 and –L-3 tests, thus attesting to the stability of all material constituents and interfaces in these ageing environments. AGNP electrodes have silver films on both sides of the devices which may act as barrier to oxygen or water diffusion. The only channel for oxygen and water infiltration is permitted through the edge cross section where the adhesive is exposed to the ambient atmosphere. At high temperature, the adhesive yields and results in accelerated degradation under ISOS-L-2.



Figure 3-9 LBIC images of the ALCR devices after ageing tests: ISOS-D-1? (a), ISOS-L-1 (b), ISOS-L-2 (c) and ISO-L-3 (d). Devices seem to degrade due to a combination of yielding of the adhesive and the lower edge sealing margin (direction B) in ISOS-L-2 and ISOS-L-3. Scale bar is 1 cm.

Second to AGNP is ALCR which has a constant V<sub>oc</sub> in all three ageing tests, while FF degrades rather rapidly in all the three tests. The degradation in FF is primarily attributed to chemical changes in the exposed surface of PEDOT:PSS due to uptake of water which reduces its conductivity [50,51]. This is caused by moisture diffusion through the adhesive from the unsealed edges to the top surface of PEDOT:PSS. PE-DOT:PSS forms a large interface with the adhesive that fixes the top glass barrier slide. LBIC images of the cells after the ageing tests confirm this hypothesis (Figure 3-9).

ASP architecture contains two PEDOT:PSS layers at the opposite terminal of the device which accelerate the degradation in the photovoltaic properties. While the top electrode is similar to ALCR, the bottom is printed Ag grid on glass overlaid by PE-DOT:PSS. Large pockets of current inhibition are observed in regions adjacent to the inkjet printed grids in the LBIC image (not shown). This is attributed to the poor adhesion of the ink-printed grid on the glass substrate resulting in voids that allow easy passage for moisture infiltration from the edges of the device.
#### 3.6.4 Summary of stability results

When evaluating the stability following the many different test protocols employed, it became evident that there are large differences between the different architectures. All ITO-free architectures are stable under dark storage conditions and have high stability under low-light conditions. As such, all devices architectures are suitable for indoor applications such as power source for various gadgets such as pocket calculators, lamps, e-readers, smart packaging, etc. When it comes to high intensity sunlight, high temperatures and humidity (ISOS-L-1/2/3) it is clear that the normal architecture device (NORM devices) fails quickly in all tests as expected and it is primarily attributed to the failure initiated by the oxidation of low work function Al electrode due to moisture and oxygen diffusion through the edges and the pin holes [52-54]. Since the device does present stability under both shelf life and low-light conditions, it is likely that this technology could be improved but the success of its use would depend on the development of efficient and low cost encapsulation methods (encapsulation with qualities beyond the method employed here) and/or on design improvement, for example, with the use of alternate interfacial buffer layer to LiF such as Cr [54],  $C_{60}$  or MoO<sub>3</sub> [55,56] that has been shown to improve the stability by as much as a factor of 100. In its current form, upscaling of NORM devices is not warranted in comparison to the other architectures. The rest of the architectures can only be evaluated relatively with oneanother while absolute lifetime cannot be meaningfully deduced from the data as it clearly became apparent that the improvement in edge sealing and addition of a UV filter in the barrier material can significantly prolong the lifetime of all architectures. Nevertheless, AGNP devices demonstrate the highest stability in ISOS-L-1 and -3 tests, while no architecture could sustain the rigorous conditions as employed under ISOS-L-2. ISOS-L-2 is unlikely to be met in real-world application. PEDOT:PSS emerged to be important constituent whose hygroscopic nature renders fast degradation of the devices. Edge sealing of the devices against water and oxygen would therefore greatly enhance the stability of all devices.

### 3.7 Architecture selection for upscaling

Based on the photovoltaic properties and the stability data described above, there is no clear winner architecture that shows distinctly high photovoltaic performance and high stability in comparison to the rest. The above studies can be viewed as way to reduce the number of candidates for up-scaling as well as to shed light on the implications of the processing methods and material components other than the photoactive material on the overall performance of architecture for use in polymer solar cells. After the degradation studies employing the five ISOS tests, the ASP, ALCR and AGNP devices still stand with the ALCR being the highest performer in terms of PCE and the AGNP architecture the best performer with respect to overall stability. The ASP architecture can be considered an intermediate with respect to ALCR and AGNP in regard to both stability and performance. These three architectures outperform ITO REF. with respect to either PCE or stability, or both. The choice among these three contenders to up-scaling is not an easy one to make and will require some consideration also of the materials and processing advantages and disadvantages for each of the architectures from the point of view of upscaling via facile and fast low-cost R2R processing. While all architectures are prototypes, several (but not all) of the materials and processing in each device architecture as employed in the prototype can be directly transferred to or adapted for low cost up-scaling. For example, the ALCR prototypes employ glove box environment as well as uses vacuum processing steps in the processing of AI/Cr and Au grid electrodes. In the upscaling, Au grid can be replaced with a screen-printable silver grid; however, Al/Cr has to be processed either by sputtering or evaporation or other such techniques where the use of vacuum is an absolute requisite. On the other hand, the ASP and AGNP architectures in principle do not require vacuum processing and can both be all printed/coated. As such, a comparative evaluation of upscaling compatibility of the three ITO-free architectures based holistically on device photovoltaic and stability performance as well as on low-cost processing compatibility must be carried out. Table 2-4 summarizes the properties of the three architectures in their suggested prototype form for low-cost upscaling compatibility. Listed in the second rows under each property is potential at low-cost upscaling compatibility that takes into account if

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low-cost techniques can be used to replace techniques that are used in the prototype development. Plus sign (+) shows positive result and the negative sign (-) shows otherwise. For PCE and stability parameters, no negative signs are used because all devices show good photovoltaic properties with a PCE of >1% and none of the devices degrades completely (PCE to 0%) in any of the stability tests. In such a case, the relative difference among the three architecture is shown by using +++; ++; and + to indicate the best, the intermediate, and the weakest among the three architectures, respectively.

If upscaling of the three prototypes is carried out using materials and processing exactly similar to those used in the prototypes development, all three architectures warrants upscaling as demonstrate by similar total points. However, none of the architecture delivers both PCE and stability distinctly high enough to sacrifice processing speed and employ glove-box and vacuum-based processing. Therefore, upscaling compatibility of the three architectures is evaluated upon adoptability of low-cost processing techniques. Based solely on adoptability of low-cost processing techniques, ALCR is the least desirable as ambient processing cannot be carried out for all layers. ASP and AGNP can all be R2R processed using coating and printing under ambient conditions and therefore both warrants upscaling. Dropping ALCR is a hard call since it does represent >2.5% PCE and has intermediate stability in comparison to ASP and AGNP. Therefore, it may be investigated further in upscaling.

Property	ASP	ALCR	AGNP
PCE	++	+++	+
	n.a	n.a.	n.a
Stability	+	++	+++
	n.a.	n.a.	n.a.
Printability	+	-	-
	+	-	+
Metal-free	-	-	-
	+	-	-
Vacuum-free	+	-	-
	+	-	+
Ambient Processing	+	-	+
	+	-	+
Flexible substrate	-	-	+
	+	+	+
Post-processing free-	-	+	+
dom <sup>1</sup>	-	+	+
Total	6	6	7
(as is prototype form)			
Total	5	2	5
(low-cost R2R pro-			
cessing compatability)			

Table 3-5. Comparison of the three final architectures evaluated for upscaling suitability. The conclusions presented in the second row for each property reflect adoptability or adaptability to lowcost roll-to-roll upscaling.

<sup>1</sup>Devices with two PEDOT:PSS layers require post-processing functionalization by application of a short pulse high voltage to switch the property of one of the PEDOT:PSS layers through de-doping [57]

## 3.8 Summary

This chapter presented a comparative study on various state-of-the-art ITO-free architectures contributed by various institutions. Detailed discussions on the observed differences in the photovoltaic property and stability are presented. Such a discussion highlights the limitations and the possibilities of improvement in each architectures. Based on the photovoltaic property and stability results, a qualitative evaluation is carried out to determine the low-cost upscaling suitability of all architectures in their current processing form as proposed by the contributing institutions. The adoptability or

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lack thereof of several of the processing steps used the prototype development in the low-cost roll-to-roll processing of the architectures is discussed. Finally, it emerges that an architecture that presents a high score in only one aspect of solar cell performance is not sufficient to justify an investment in up-scaling. Many will require further technical development. This study also highlights that when developing device architectures, one must take into account the upscaling suitability of the adopted processing technique in their development. Ideally, an all solution ambient processing like the ASP devices is the most bankable processing method in prototype development because upscaling of such structure are not likely to cause dramatic changes in the properties as drastic changes in processing are not required in upscaling.

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## 4. The Upscaling Process: A background

#### 4.1 Introduction

This chapter aims to present an overview of the upscaling process of polymers solar cells (PSCs) which include module design, R2R printing and coating processes, R2R encapsulation, and finally R2R characterization. It presents a prelude to the next chapters (Chapter 5-7) which are based on the upscaling of three different ITO-free architectures as selected from the initial prototype evaluation presented in Chapter 3.

#### 4.2 Module design

Ideally, a solar cell should deliver the same power conversion efficiency (PCE) irrespective of the device area. In reality, however, this is hard to achieve. Scalability of a single cell is limited by the resistance of the electrodes. Particularly, the common metal oxide transparent electrode used in thin films (such as ITO and FTO) often has high sheet resistance which, in turn, results in large ohmic losses upon upscaling and manifests in decreasing fill factor with increasing cell area in a solar cell. In order to minimize the series resistance upon upscaling, individual cells are electrically interconnected to form modules. A serially-integrated module based on inverted architecture (sometime also referred as monolithically-integrated) allows low-cost processing due to an all-solution processing possibility as well as achievement of interconnection during processing itself. Figure 4-1 demonstrates such a serially-integrated module design. The width of each cell can be optimized to allow maximum active area in each cell with minimum ohmic losses. For ITO on PET which commonly has a sheet resistance of 60  $\Omega$  -1, a cell width ~1 cm is found optimum [1,2]. The active area can also be increased by elongating the length of the cells since the direction of current is along the width of the cell and therefore increasing length of the cells do not contribute to ohmic losses. The gaps between the cells are inactive (or passive) regions and represents aperture loss; however, these gaps are necessary for establishing interconnection between the individual cells in a module. The gaps should be as small as possible to avoid losses in geometric fill factor while also achieving electrical isolation of each cell as well as ac-



Figure 4-1. Schematic illustration of an inverted architecture based serially-integrated module comprising of three cells/stripes. Only the active area contributes to the power generation. Photogenerated current is injected into the cathode and is then driven laterally to one edge of the device where contact to the back metal electrode of the adjacent device is made. Either cathode or anode can be transparent.

commodating processing adjustments (such as layer offsets) required in the processing of each subsequent layers in a PSC stack. In our group, a 2 mm gap is found to be optimum for a cell width of ~1 cm in a module structure based on ITO electrode [1]. Geometric fill factor is defined by the ratio of the current generating area to the complete module area. The areas allocated to contacts, interconnections, edges, etc. result in low geometric fill actor and the aim is to achieve >60% geometric fill factor.

#### 4.3 Roll-to-Roll Processing

A roll-to-roll (R2R) implies a continuous process in which a flexible substrate (known as the web) is subjected to four consecutive steps on a R2R machine: 1) unwinding from a roll (unwinder); 2) passing through printing or coating station(s); 3) then through drying unit(s) after each printing or coating sessions if required; 4) rewinding on a second roll. A surface treatment step such as corona treatment may follow before Step no. 2 and the printing of registration marks and barcodes may be incorporated before the final rewinding of the web once the solar cell stack is complete. A PSC is a stacked multilayer structure which allows the possibility of a multitude of printing and coating techniques to be employed in the processing of each individual layers. Ideally, an inline all-ambient R2R processing of all layers is desirable for PSCs. However, an all in-line R2R processing of PSCs is not feasible due to different process speed and drying re-



Figure 4-2. A roll-to-roll processing unit at DTU comprising of: 1) Unwinder; 2) Web-guide; 3) Corona station 4) Flexo- station; 5) Slot-die coating; 6 and 8) convection ovens; 7) Rotary screen printer; 9) Inkjet for identification barcodes; and 10) Rewinder. Either 4 or 5 is used during one R2R run. Figure not drawn to scale.

quirements of each layer and therefore a combination of inline and discrete processes are used in practice. A schematic illustration of our (DTU's) R2R line which was employed in the processing of all ITO-free modules described in the succeeding chapters is shown in Figure 4-2. Table 4-1 lists the R2R printing and coating techniques that are employed in the processing of PSCs of the three different ITO-free architectures reported in the next chapters. A comprehensive review on many roll-to-roll coating and printing techniques applicable in the processing of PSCs is published elsewhere [3,4]. Henceforth, only the techniques that were used in upscaling of ITO-free PSC modules as a part of this PhD study are described.

### 4.3.1 Slot-die coating

Among the myriad of techniques available, slot-die coating has proven to be a facile and fast coating method for various layers in a PSC stack including the photoactive material, charge selective buffer layers such as nanoparticle solutions such as ZnO and PEDOT:PSS, and electrodes such as nanoparticle based Ag inks. Slot-die coating is a one-dimensional technique that allows patterning only in the form of stripes along the direction of the web-movement in the R2R line. However, such a dimensionality has sufficed in the fabrication of serially-integrated PSC modules especially when consider-



Figure 4-3 (a) A side-view picture of an assembled slot-die head. The parts are shown in (b) comprising of: (from left) half of the head, meniscus guide, flow mask, and second half with T-shape flow channel. The flow mask is designed for printing of 3 sets of modules along the width of the web, each with 16 stripes/cells.

ing the significantly lower running cost of the machine compared to other techniques such as flexographic printing. The parts and assembly of a slot-die head is shown in Figure 4-3. The width of the stripes can be easily controlled by designing the flowmask. The alignment of the pattern in subsequent layer is accomplished by simply moving the coating head perpendicular to the direction of the web movement. Slot-die coating is a pre-metered technique: the layer thickness can be controlled by simple processing input parameters. The dry layer thickness can be estimated with the following empirical expression [3];

$$d = \frac{\mathrm{f}}{\mathrm{s}\cdot\mathrm{w}} \left(\frac{\mathrm{c}}{\mathrm{\rho}}\right)$$

where *d* is the dry layer thickness in cm, *f* is the flow rate in cm<sup>3</sup> min<sup>-1</sup>, *s* is the web speed in cm min<sup>-1</sup>, *w* is the coated width in cm, c is the solid concentration in the ink in g cm<sup>-3</sup> and  $\rho$  is the density of the dried ink material in g cm<sup>-3</sup>. The term  $\frac{f}{s \cdot w}$  is simply the wet-layer thickness.

### 4.3.2 Screen-printing

Screen printing is a versatile and simple printing technique that allows for 2dimensional patterning of the printed layer. It exists in two types: rotary and flat-bed; both can be mounted on a R2R line although rotary is more compact (Figure 4-4). Screen printing is mostly suitable for printing of relatively thick layers with inks of higher viscosity and solvents with low volatility. Screen printable formulations of Ag are commercially available and are used for R2R screen printing of interconnects between cells in a module, busbars, and Ag electrodes in inverted geometry [5-8]. In the processing of ITO-free modules in this Ph.D. study, screen printing is used in the printing of silver back electrodes and interconnections, as well as for printing of PEDOT:PSS layers in some cases. Others have utilized screen printing in the processing of one or more functional components of a PSCs [9,10] including an all screen printed PSCs by our group used in the first public demonstration on PSCs [11].

The screen printing process involves a screen made of a mesh of a woven material (i.e., synthetic fiber or steel), held in tension to a frame. The mesh is filled with an emulsion that is impervious to the coating solution (stencil). The image print is achieved on the screen by removing the stencil by a photochemical process using a shadow mask, thus leaving the image area open and permeable to ink. Printing is achieved by forcing the ink through the open areas in the screen by using a squeegee. In this manner, the pattern (print image) on the screen is reproduced onto the substrate (Figure 4-4). During printing, the screen in placed above the substrate at a certain 'snap-off' distance of few millimeters. The diameter and the thread count of the mesh determine the amount of ink deposited on the substrate. Layer thickness is influenced by force of squeegee, screen parameters, the snap-off distance, the speed of squeegee, and rheology of the printing paste. Generally, screen printing is used for printing thicker layers often above 500 nm to several microns range; however, few reports suggest that a 40 nm active layer can be achievable [9]. Nonetheless, these reports are on less than  $1 \text{ cm}^2$  of active area. In large scale setting, it may be difficult to maintain homogenous layer thickness for extremely thin layers.



Figure 4-4: Schematic illustration of two forms of screen printing process (left) and a picture of an actual flat-bed R2R screen printing of silver paste in progress (right). The squeegee is captured in motion.

#### 4.3.3 Flexographic printing

Flexographic printing is a two-dimensional printing technique consisting of four main parts: printing plate cylinder, anilox roller, impression roller, and an inking unit (Figure 4-5). The printing plate, also referred as printing form, is made of an elastomeric polymer and carries the relief image (image positive as protruding features) on its surface. The inking unit is comprised of either a chambered doctor blade or a fountain roller in an ink bath and a doctor blade. The surface of the anilox roller contains engraved cells of certain geometry and volume. During printing, the cells in the anilox roller are evenly filled with ink via the chambered doctor blade or the fountain roller. Excess ink in the latter case is scraped off with the doctor blade (a steel blade). The ink from the anilox roller is transferred to the image relief on the plate cylinder. Only the relief gets inked, the recessed areas remain ink-free. Finally, the ink from the printing plate is transferred to the web rolling over the impression roller with the use of nip pressure, thus reproducing the image onto the web. Flexographic printing is typically used in printing presses for the packaging industry. It is a fast printing method with maximum web speed of greater than 500 m min<sup>-1</sup> achievable. Only two instances have been reported: a modified PEDOT: PSS formulation was printed at 30 m min<sup>-1</sup> to process de-



Figure 4-5: Schematic illustration of flexography printing (a); a flexo printing plate cylinder with relief image (b); and flexography printing of Ag paste in progress on a PET (c).

vices with area of 0.09 cm<sup>2</sup> [12] and the printing of conductive Ag micro grid network on ITO coated PET [13]. Our group had earlier used flexographic printing to apply noctanol as a wetting agent prior to slot-die coating of PEDOT PSS [14]. As a part of this PhD study in conjunction with various other projects in our group, we have used flexographic printing in the processing of Ag grid for ITO-replacement in the upscaling of one of the ITO-free architecture (Chapter 7). Web-speed up-to 20 m min<sup>-1</sup> has been employed.

#### 4.3.4 Inkjet printing

Inkjet printing is a two dimensional technique that allows the formation of fine patterns of inks from suspensions or solutions with high resolution up-to 1200 dpi and frequency of 100 kHz [15]. It is a non-contact printing method wherein printing is achieved by directing a steady jet of ink droplets to the substrate. The mechanism of ink generation classifies inkjet printers into two main categories: drop-on demand and continuous. In continuous ink jet, a continuous stream of ink is forced through a microscopic nozzle by a high pressure pump. The stream is broken down into equal droplets by application of acoustics and is subsequently charged either with binary or variable charges. The charged droplets are directed to the substrate with the use of an electrostatic field. The deflection of the droplets in the electrostatic field directs some to the substrate in a desired pattern while most (98%) are deflected into a 'catcher' or a 'gutter' which is the recycled back to the ink reservoir. Controlling the tendency of the drops to recombine is difficult and recycling adds complexity to the system. Hence, continuous ink jet printing systems are replaced by newer techniques such as drop-on-demand (Figure 11), which is also used in some of our processing.

In drop-on-demand (DoD), the required amount of ink droplets are generated with the use of a piezoelectric or by a thermal actuators that are located in the ink chambers. In piezoelectric based systems, an electric signal controls the mechanical deformation of the piezo-plate. Upon the application of voltage, the piezoelectric material deforms and sends a pressure pulse to the ink forcing it out of the nozzles in the form of droplets (Figure 4-6). Each ink requires optimization of the waveform of the applied voltage to form stable droplets. The applied frequency determines the amount of drops released per second and therefore the printing speed. In thermal jet process, a heating element (resistor) is used to induce localized vaporization of a small amount of the ink in the enclosed ink chamber. This results in pressure build-up causing displacement of some of the ink in the chamber and ejection of a droplets through the nozzles.

Ink jet printing offers precision printing of inks with high resolution up-to 1200 dpi. Being a non-contact printing method, the risk of contamination of inks is also eliminated. Furthermore, printing is digitally controlled which means the no costly printing form is required and processing is relatively simple than other techniques. In comparison to other techniques, the major disadvantage is possibly the limited printing speed. The dry layer thickness of ink jet printed film is given by number of droplets delivered per area, the single droplet volume, and the concentration of the solute in the ink with the following empirical relationship [3];

$$d = N_d V_d \frac{c}{\rho}$$

 $N_d$  is the number of droplets per area (cm<sup>-2</sup>) printed,  $V_d$  is the volume of each droplet (cm<sup>3</sup>), c is the concentration of the solid material in the ink in g cm<sup>-3</sup> and  $\rho$  is the density of the material in the final film in g cm<sup>-3.</sup>

During this Ph.D. study, inkjet printing is employed in the printing Ag electrodes, as a front electrode printed directly on a substrate [16,17] or as a back electrode printed as the last layer on top of an inverted PSC stack [18], or both. Others have also used bench-top inkjet printers in the processing of front electrodes in normal architectures [19-21]. Inkjet printing of silver nanoparticle on flexible foil is a widely researched subjected because of its interested to printed electronics; however, inkjet printing can also be employed in the processing of various organic materials such as photoactive materials [22-26]; PEDOT:PSS [23,27,28]; and inorganic nanoparticle solutions such as TiO<sub>2</sub> [29] ITO [30], InZnSO [31], ZnO [32]. Inkjet printing has been particularly studied as a cost-efficient up-scalable technology that allows freedom in two dimensional patterning, particularly sought-after in the field of organic photodiode (OLEDS), memory devices, transistors (OTFTs), sensors, etc. [33]. In PSCs, slot-die coating has proven to be a facile and fast coating method for low viscosity solutions such as P3HT:PCBM, ZnO, and PEDOT:PSS [3,4,34-36]. It is unlikely that inkjet printing of these layers will rival the ease and low maintenance of slot-die coating for very large scale production for PSC modules, where one dimensional patterning offered by slot-die coating has sufficed and in fact is more robust and tolerable to a wide range of ink properties. Inkjet printing requires research on the ink development as the mechanism of droplet generation causes constraints on the ink formulations. In general, inks ought to be with lower viscosity (4-30 cp) and high surface tension (>35 mN min-1) with solvent of high boiling point [3]. However, the inks of PSC materials are often composed of a complex mixture of many solvents with different volatility which may introduce problem in droplet formations. Low boiling point solvents cause printing head clogging and coffee strain effects [37]. As such, additives are used to module the ink properties. Excellent reviews on inkjet printing in organic electronics can be consulted for more information [38,39].



Figure 4-6 Schematics of piezoelectric drop-on-demand (DOD) inkjet printing (right); a photograph of inkjet print-head (top right) and a photograph of a full roll-to-roll ink-jet printed pattern (resolution of 600 DPI) using a DOD system on a web width of 305 mm (bottom right).

#### 4.3.5 Sputtering

Metals such as aluminum or chromium are highly reactive metals in the presence of oxygen and water, and cannot be deposited using solution processing under ambient conditions. Such metals are deposited using a vacuum-based methods such as evaporation and sputtering. R2R magnetron sputtering was employed in the processing of Al and Cr electrodes in the upscaling of one of the architectures (Chapter 5).

Sputtering is a physical vapor deposition technique that involves bombardment of a source material (target) by energetic ions generated in glow discharge plasma of Ar which is situated in front of the target. The bombardment leads to removal of target atoms (sputtering) which then condenses onto a substrate resulting in a thin film (Figure 4-7). Secondary electrons are also emitted by the target surfaces which are constrained to the plasma using magnetic fields parallel to the target surface. The trapping of these electrons increase the probability of electron-atom collision which in turn leads to increase ion bombardment of the target, giving higher sputtering rates and higher deposition rates. A magnetron sputtering operates at a typical pressure of  $10^{-2}$ mbar and at voltages of 500 V [40]. The web speed during film deposition by sputtering is significantly slower (in cm min<sup>-1</sup> range) in comparison to other printing and coating techniques which can process in the unit of m min<sup>-1</sup>.



Figure 4-7. Schematic illustration of a R2R sputtering system showing deposition of two metals (targets). The figure is not to scale and system is generally more compact because of the large vacuum requirement.

#### 4.3.6 Thermal Imprinting for processing of embedded metal grids

Thermal imprinting has been used in the processing of embedded Ag grids in the flexible substrate. It is a pattern transfer multistep processing that involves: 1) Preparation of mold stamp; 2) Pattern transfer from the stamp to the flexible substrate by imprinting with the application of heat and pressure; 3) metal filling by doctor blading and 4) removal of excess ink; and 5) drying/sintering (Figure 4-8) [16,41,42]. In our study, a flexible nickel master with a diagonal line print pattern with a line spacing of 2 mm was used. The nickel stamp is electroformed and the resulting pattern is stands as protruding features on the surface of the stamp. During printing, the flexible metal mold stamp is attached to a heated roll and pressure is applied as the flexible substrate such as PET is passed through the nip of the heated roller. In this manner, the pattern on the stamp is reproduced/imprinted on the substrate in the form of engraved channels, the width of which is dependent on the mold design. The substrate properties (such as the glass transition temperature, surface tension, etc.) are very crucial for successful replication of the pattern from the mold onto the substrate within reasonable processing temperature and pressure [43]. In our experiment, the temperature of the roll was 110°C and a force of 100 KgF was applied and the resulting width of channels was 10 µm. Once this step is completed which is accomplished at low web-speed (up-to 12



Figure 4-8. Schematic diagrams of the fabrication process of Ag-embedded TCF: (a) fabrication of flexible stamp mold, (b) wrapping the stamp mold on the thermal roll, (c) roll-to-roll thermal imprinting of polymer film, (d) dropping of conductive nano-silver paste on the patterned polymer film, (e) doctor blading of nano-silver paste, and (f) roll cleaning and drying of the Ag-filled film. ©2013 American Scientific Publishers. Adapted, with permission from ref. [41]

m min<sup>-1</sup>), silver is filled in the imprinted pattern by doctor blading. The excess ink is cleaned by using roll cleaning and finally, the embedded metal is sintered. A schematic illustration of the R2R imprinting method employed in the preparation of embedded silver grids is shown in Figure 4-8.

#### 4.4 Encapsulation

Encapsulation of PSC modules involves sealing the module between two sheets of barrier foils. This is accomplished by using three sealing methods: cold lamination, hotmelt lamination, and UV-lamination. All three methods can be carried out on a R2R line comprising of two unwinder rolls and a rewinder roll and some support rolls as shown in Figure 4-8. One of the unwinder is used for a roll of barrier foil. In cold lami-

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nation, barrier foil is pre-coated with a pressure sensitive adhesive and protected by a glossy paper liner which does not adhere to the glue. During lamination, the glossy paper is removed and the glue is exposed. The barrier foil with the adhesive is then place over exposed side of the modules between two support rolls. The lamination is completed by the application of nip pressure. The next step is to repeat the process for the back side behind the substrate if required. Sometimes, we have fabricated solar cells directly on the barrier film in which case only one side of the modules can to be laminated. Hot-melt uses the same principle as cold lamination except that the glue requires heat for curing instead of pressure. This is achieved by passing the barrier with adhesive and the module foils stack between heated rollers that melts the adhesive and tightly seals the module. UV lamination is the most cumbersome encapsulation method in comparison to the other two methods. It involves consecutively coating the barrier film with a UV curable adhesive, lamination of the module, and curing of the adhesive under UV lamp. All three techniques are schematically shown in Figure 4-9. Among the three techniques, cold lamination is the fastest method and a web-speed >20 m min-1 is easily accomplished. As discussed in Chapter 3, the adhesives do not have barrier properties. It is therefore crucial to maintain as low thickness of the adhesive. Edge sealing can be accomplished by maintaining a larger margin of the barrier foils that extends beyond the module area. Such simple methods can significantly prolong the stability of the modules. A comparison of these three techniques and the implications of different adhesives on the photovoltaic properties and stability of PSC modules and cells are published elsewhere [44,45].



Figure 4-9 Step-wise processing of R2R encapsulation of PSC modules. Shown are three different methods: cold lamination that uses pressure sensitive adhesive (PSA); UV lamination, and hot-melt. ©Wiley. Reprinted, with permission from ref. [44].

#### 4.5 Roll-to-roll characterization

A single roll of R2R processed solar cell module consists of a large number of solar cells (from a few hundred to thousands depending on the motif and the length of the roll). Manual electrical characterization of all solar cell modules on a roll is tedious and incurs unnecessary resource wastage. A R2R characterization set up is a fast and an inexpensive method for automatic characterization of solar cell module from a R2R processed roll. Such a set-up can be used for IV characterization and electrical imaging methods such as light beam induced current (LBIC), Dark lock in thermography (DLIT) etc. Operator is only required during the initial starting up (mounting the roll and turning on the characterization unit) and shutting down of the instrument (unmounting, collecting the data, and turning of the instrumentation) once the characterization is completed. The instrumentation is simple and is schematically illustrated in Figure 4-9 [1]. It comprises of a R2R line comprising of an unwinder and a rewinder; a solar simulator and the necessary electric components such as source meter unit (SMU) and a computer; a positioning system, electrical contacting system which includes vacuum table with electrical contacts to the SMU and pneumatic contact pads. The system is



Figure 4-10 Schematic illustration of a R2R characterization unit. The electrical components are given in the second row.

fully automated and controlled by a computer. The positioning of the module on the vacuum table is achieved reading the register marks printing during R2R fabrication of the PSC modules.

During operation, solar cell modules are automatically positioned under a solar simulator (we use 1000 W m<sup>-2</sup>, AM 1.5 powered by a Steuernagel KHS1200). Electrical contacting is achieved by a combination of vacuum-table and pneumatic cylinders that force contact between the module bus bars and the conducting strips on the table that relays the connection to the source-meter. IV characterization is then automatically carried out by a Keithley 2400 sourcemeter and custom built software collects IV data, performs photo-annealing tests by taking multiple IV curves, and determines when to move to the next module [3].

Under this PhD work, R2R characterization could seldom be employed due to edge sealing of the encapsulation which requires contacting to be made with a punchthrough push button which requires manual operation. For such button contacts, the modules need to be isolated from the roll by a laser cutter or by using scissors. Charac-

Upscaled de- nomination	Fraunhofer-type (ALCR)	lOne (ASP)	ProcessH (AGNP)
Structure	Substrate/Al/Cr/ P3HT:PCBM/PEDOT :PSS/Ag	Substrate/Ag/PEDOT:PSS /ZnO/P3HT:PCBM/PEDOT:PSS/Ag	Substrate/Ag/ZnO/P3HT: PCBM/PEDOT: PSS/Ag
Substrate	Kapton foil	Barrier PET	Barrier PET
Bottom elec-		1. Flexography	
trode	Sputtering	(Ag grids)	Slot-die
	(Al/Cr)	<ol> <li>Rotary screen printing (hc PEDOT:PSS)</li> </ol>	(Ag)
Electron transport lay- er	-	Slot-die (ZnO)	Slot-die (ZnO)
Photo-active	Slot-die	Slot-die	Slot-die
layer	(P3HT:PCBM)	(P3HT:PCBM)	(P3HT:PCBM)
Hole transport lay- er	Slot-die (PEDOT:PSS)	Slot-die/ rotary screen printing (PEDOT:PSS)	Slot-die (PEDOT:PSS)
Top elec- trode (anode)	Screen printing (Ag)	Screen printing (Ag)	Screen printing (Ag)

Table 4-4-1 R2R processing techniques applied in the upscaling of three different architectures.Given in brackets in the first row is their prototype abbreviation.

terization of the rolls is manually done by randomly selecting modules from the roll and testing under a solar simulator. Nonetheless, the R2R characterization unit can be employed in the future pending investment on R2R contacting of encapsulated modules.

## 4.6 Summary

This chapter provides a comprehensive background of upscaling process. It also discusses R2R processing techniques that are employed in the upscaling of ITO-free modules under this Ph.D. study. Different combinations of some or all of these techniques are employed in the processing of individual layers of the three ITO-free architectures investigated for upscaling (Chapter 5-7). Here, each processing technique is discussed in detail and presented along is a review of their use in the literature. In addition to the techniques presented here, there are a myriad of R2R processing techniques available which we have holistically reviewed in several publications [3,4]. To complete the picture, R2R encapsulation techniques and R2R characterization techniques are also discussed although the later could not be used during this PhD study due to the lack of R2R contact for edge sealed devices. Nonetheless, this is a technical problem that can easily be overcome and remains pending further investment. The ideal scenario of low-cost processing of PSCs involves high throughput ambient processing where the beginning of processing starts with feeding a bare PET foil through a R2R machine and the final R2R processing run returns a fully encapsulated module that can readily be integrated in various applications or installed for power generation. The ideal scenario is within grasp by using a combination of several of these processing steps.

### 4.7 Summary

Among the plethora of coating and printing that are available, some are comparatively advantageous than others. Hence, it is critical to identify the techniques that are most suitable for low-cost processing of functional organic multilayer structures such as polymer solar cells. This means that the techniques should be evaluated on the basis of processing speed, requirement for ink preparation, running cost and maintenance. So far, slot-die coating remains unparalleled to any other technique for coating of lowviscous solutions due to its low-cost running cost and ability to coat low thicknesses suitable for solar cells. Two dimensional techniques such as flexographic printing, inkjet printing, thermal imprinting, and rotary screen printed have been explored in the upscaling in this PhD study and each techniques brings different advantages as it is discussed in the later chapters.

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# 5. Upscaling of Architecture 1: The Fraunhofer-type

### 5.1 Introduction

The upscaled ALCR with several processing modifications is denominated as the Fraunhofer-type (Fraunhofer ISE first suggested the architecture [1]). The ALCR prototypes described in Chapter 3 were based on several processing conditions that are beyond the objective of our low-cost production. Specifically, the prototypes were fabricated in glove-box environment and using vacuum-based deposition method (evaporation) in the processing of Cr/Al/Cr bottom electrodes and Au top electrodes. Low-cost R2R processing implies ambient processing and avoidance of vacuum-based methods. Hence, prior to R2R large-scale processing, laboratory test-cells (active area 3 cm<sup>2</sup>) were revisited to optimize and evaluate their performance upon ambient processing and vacuum-free methods wherever accommodable. The optimized parameters can then be readily adopted in R2R processing of large-area modules. The test-cells set a true benchmark against which the performance of R2R processed modules can be compared. The difference in the materials and processing methods used in the development of the prototype, test-cells (R2R process optimization) and R2R processing are listed in Table 5-1.

#### 5.2 The test cells

#### 5.2.1 Materials

Kapton polyamide foil was purchased from Skultuna Flexibles AB (Sweden). Poly(3hexylthiophene) was purchased as Sepiolid P200 from BASF and [60]PCBM was purchased from Solenne BV (purity of 99%). PEDOT:PSS was purchased as Orgacon EL-P 5010 from Agfa and was diluted with isopropanol until a viscosity of 270 mPa s was obtained. The silver ink was a heat curable one (Dupont PV410) and used as received. The barrier foil was purchased from Amcor.

#### 5.2.2 Processing

The test cells were fabricated on R2R sputtered Al/Cr on polyamide Kapton foil. The electrode foil was prepared for R2R processing. Small pieces (25 x 50 mm) were cut from one Al/Cr roll and mounted on a glass substrate. P3HT:PCBM solution in choro-
Materials	Prot	otype	Те	st-Cells	R2R modules
Bottom electrode	Cr/Al/Cr	Evaporated	Al/Cr	R2R sputter	sputtered
Active layer	P3HT:PCBM	Spin-coated/ glove box	P3HT:PCBM	Spin-coating/ ambient	slot-die /ambient
Hole- transport Layer	PEDOT:PSS	Spincoated/ glove-box	PEDOT:PSS	Spin-coating /ambient	slot- die/ambient
Top- electrode	Au	Evaporated	Ag	Screen-printing/ ambient	screen- print/ambient
Substrate	Glass		Kapton		

Table 5-1 Adapting processing toward low-cost upscaling: changes in materials and processing conditions from prototype to the test cells and finally to the R2R large-area modules is shown.

benzene was spin-coated at 600 rpm on the substrate. PEDOT:PSS were subsequently spin-coated and dried at 140 °C for 5 minutes. Finally, silver grid was screen-printed using a small laboratory screen printer and dried immediately after printing at 140°C for 3 minutes. All devices were manually encapsulated using a barrier foil that was prelined with pressure sensitive adhesive on one side. Apart from the sputtered Al/Cr electrode, the processing of all other layers were carried out in air and the final device active area was 3 cm<sup>2</sup>. Three discrete parameters were optimized on test-cells: active layer concentration, P3HT: PCBM ratio, and PEDOT: PSS thickness. Table 5.2 lists the impact of processing conditions on the photovoltaic properties of the solar cells. All cells were characterized under 1 sun illumination (1000W m<sup>-2</sup>; AM 1.5) under a solar simulator equipped with a metal-halide lamp.

## 5.2.3 Results

Firstly, the concentration of P3HT:PCBM in the active ink was optimized. This was done by varying the weight of P3HT and PCBM in the solvent simultaneously while keeping the ratio of P3HT:PCBM constant at 1.5:1 (w/w). The intermediate concentration of 35 mg mL<sup>-1</sup> (21 mg of P3HT and 14 mg of PCBM per 1 ml of chlorobenzene) results in the highest photovoltaic performance. Secondly, the influence of PCBM content relative to P3HT was investigated. This was done by varying weight fraction of PCBM against a constant weight of P3HT at 21 mg mL<sup>-1</sup> (the optimum from the first experiment). Three sets were prepared with P3HT:PCBM ratio of 1.5:1; 1:1; and 1:1.5 (*wt/wt*).All three ratios results in very similar performances. This is in agreement with a previous study in which the mixing ratio of P3HT.PCBM was investigated on a gradient scale in R2R processing using slot-die coating [2]. In the third experiment, the thickness of PEDOT:PSS was investigated. PEDOT:PSS thickness optimization requires a trade-off between maximizing transmittance and minimizing harmful solvent diffusion from the screen printable Ag ink through the PEDOT:PSS layer and into the photoactive layer [3]. Both of these phenomena impose opposing requirements on the PEDOT:PSS layer thickness: too thick layers lead to low current densities because of significant transmission loss while solvent destruction can be minimized; on the other hand, too thin layers lead to s destruction of active layer and sometime even short circuit as result of Ag migration with the solvent of the screen printed Ag toward the opposite electrode. The latter is also observed in the test-cells with the thinnest PEDOT:PSS (2000 rpm) explored in this experiment. Hence, it is crucial to find an optimum layer thickness that allows maximum optical transmission while minimizing the damage to the photoactive layer. This

	P3HT:PCBM (mg mL <sup>-1</sup> )	PEDOT:PSS Spin coating (rpm)	V <sub>oc</sub> (V)	J <sub>sc</sub> (mA cm⁻²)	FF (%)	PCE (%)
A ative con	15:10		0.35	3.91	31	0.42
Active con-	21:14	1000	0.35	5.92	35	0.72
centration	30:20		0.32	3.41	24	0.26
	21:14	1000	0.36	7.43	30	0.80
P3H1:PCBIM	21:21		0.35	5.92	35	0.72
ratio	21:18.5		0.37	7.30	30	0.81
	21:18.5	700	0.41	6.42	35	0.92 (0.85)
		1000	0.43	8.00	30	1.03 (1.20)
Thicknoss		1250	0.40	7.71	36	1.11 (1.40)
THICKIESS		1400	0.40	8.01	33	1.05 (1.35)
		2000	-	-	-	-

 Table 5-2 Overview of processing optimization on test cells and the corresponding influence on key

 photovoltaic parameters. The parenthesis gives values after photo-annealing.

optimum PEDOT:PSS layer thickness in the test cells was achieved at a spin-coating speed of 1250 (~800 nm) that led to the highest efficiency after annealing of ~1.4%.



Figure 5-1 *IV*-curve typical evolution during photo-annealing of an encapsulated test device at 1000 W m<sup>-2</sup>, 72 +/- 2°C from as-produced having an inflection (red) to less severe inflection after photoannealing (blue). The curves corresponding to the first phase (decreasing IV) are omitted (*left*); A typical evolution of the photovoltaic parameters upon photo-annealing time ( $\Box$ ) V<sub>oc</sub>, ( $\Delta$ ) FF,( $_{O}$ ) Jsc; and ( $\blacksquare$  PCE (*right*).

The efficiency of all test-cells were limited (maximum 1.4%) in comparison to the prototype (PCE >2.5%) due to several reasons. Firstly, the prototypes employed evaporated back electrode which allows extremely thin PEDOT:PSS layer (~200 nm) and the width of the prototype cells to the busbar was 0.5 cm. These factors results in the higher current density (10-12 mA cm<sup>-2</sup>) and also contribute to higher FF (>50%) in the prototypes compared to the test-cells. However, the main difference between prototype and the test-cells is found in V<sub>oc</sub> and FF and this is attributed to the presence of an inflection point in the IV curves of all the test-cells which is absent from the prototypes (Figure 5-1). Such an inflection in the IV curve is characteristic of barrier to charge transport between the photoactive material and the electrodes, caused by an insulating interface or a poorly conducting interfacial layer [4-7]. Since no intentional barrier introduced and the material selected for this architecture were based on work function matching it can be inferred that the inflection in the IV curve is due to barrier to charge extraction emerging from an interface that has changed its properties during processing. A similar inflection point is observed when ZnO is used as electron transport layer in inverted PSC devices [3,8]. In such ZnO- based devices, the inflection is attributed to O<sub>2</sub> adsorption on the ZnO surface which can be eliminated by UV illumination (excitation in n-type ZnO semiconductor) or by application of reverse bias

	P3HT:PCBM (mg mL <sup>-1</sup> )	PEDOT:PSS Spin coating (rpm)	V <sub>oc</sub> (V)	J <sub>sc</sub> (mA cm⁻²)	FF (%)	PCE (%)
Active con-	15:10		0.35	3.91	31	0.42
contration	21:14	1000	0.35	5.92	35	0.72
centration	30:20		0.32	3.41	24	0.26
	21:14	1000	0.36	7.43	30	0.80
P3HT:PCBIM	21:21		0.35	5.92	35	0.72
ratio	21:18.5		0.37	7.30	30	0.81
	21:18.5	700	0.41	6.42	35	0.92 (0.85)
		1000	0.43	8.00	30	1.03 (1.20)
PEDUT:PSS		1250	0.40	7.71	36	1.11 (1.40)
THICKNESS		1400	0.40	8.01	33	1.05 (1.35)
		2000	-	-	-	-

Table 5-3 Overview of processing optimization on test cells and the corresponding influence on key photovoltaic parameters. The parenthesis gives values after photo-annealing.

(charge injection) [3,9]. In the test-cells, however, UV illumination achieved by constant exposure of the devices to the illumination from the solar simulator alleviates the inflection point albeit never completely eliminates it. This suggests that the inflection in test-cells is caused not only by the adsorbed gas species on chromium [10] but also by another mechanism, probably due to the formation of poorly conducting  $Cr_2O_3$  layer [11]. We note that such an inflection is not observed in the prototype devices which were completely fabricated in the glovebox. The fabrication in air introduces the inflection resulting in much reduced FF and  $V_{oc}$  of the test-cells (FF: <40%; Voc: <0.4V) compared to the Prototypes (FF: >55%; Voc: >0.55V).

The severity of the inflection is dependent on the thickness of the chromium metal. In a separate study, it was observed that 100 nm Al/ 5 nm Cr electrode based device (exactly similar to the prototypes) resulted in a more acute S-shape curve while increasing the thickness to 15 nm as used in here in the test-cells alleviates the S-shape nature. This is simply due to increasing bulk to surface ratio. Furthermore, simply rinsing the Al/Cr surface with ethanol immediately prior to deposition of the successive layers may alleviate the problem during ambient processing. However, none of these trials results in complete elimination of the inflection phenomena. It was observed that annealing in glovebox after ambient processing of P3HT:PCBM and PEDOT:PSS resulted

in no inflection in the IV curve (Figure 5-2). This observation signals toward two possible cases: 1) the high susceptibility of chromium to thermally induced oxidation or gas adsorption or (2) reduction of chromium oxide upon annealing in N<sub>2</sub> environment [12]. Chromium is a complex transition metal and is known to oxidize in various states depending on the processing environment-- some form semi-conductor of either p-type and n-type nature and with various charge motilities [10-13]. Complete understanding of its role in our PSCs demands an elaborate study on the properties of chromium oxide that forms during ambient and glovebox processing. This was beyond the scope



Figure 5-2 The influence of processing conditions on the on the inflection in the IV curve of testdevices with chromium interlayers. Here, Al/Cr thickness was 100 nm/5 nm. The inflection is less severe for thicker Cr layer as shown in Figure 5-1.

and duration of my PhD study; however, suffice to state here that the incorporation of chromium in a PSC device requires glovebox processing to harvest its full potential as observed in our study as well as seen in another independent study where P3HT:PCBM was slot-die coated in ambient conditions but annealed in the N<sub>2</sub> environment [14].

## 5.3 The R2R Produced Modules

The Fraunhofer-type is a top illuminated inverted architecture that utilizes metal bottom electrode and a PEDOT:PSS/Ag grid top transparent electrodes. Two different large-area device designs were investigated: serially-integrated module and monolithic module. In the serially-integrated module, 16 cells were serially connected in each module during the R2R printing process and final total area of the module was 235 cm<sup>2</sup>. This was accomplished by patterning the bottom Al/Cr electrode in the forms of strips along the length of the roll using shadow mask during sputtering of Al/Cr. Monolithic modules were based on large-area single cells (100 cm<sup>2</sup>). We chose to investigate monolithic modules primarily on account of the significantly lower sheet resistance of the bottom electrodes (Al/Cr) of <1  $\Omega$ <sup>-1</sup> in comparison to ITO on PET (30-60  $\Omega$ <sup>-1</sup>) and because monolithic modules are easier process with coating and/or printing in a R2R line, thus enabling higher yield. The size of the module was arbitrarily determined so that two monolithic modules can fit along the width of the foil although devices as wide as the web-width could have been made. Furthermore, four designs of top electrodes in monolithic structures were investigated to optimize the trade-off between current collection and optical losses due to shading from the top Ag grid. Figure 5-3 schematically illustrates the serially-integrated and monolithic structures and Table 5-2 lists their specifications.



Figure 5-3 Schematic illustration of serially-intergrated module and monolithic modules with four different top electrode designs.

Table 5-4 Illuminated and active area of the different modules prepared in this study. Seriallyintegrated module design leads to large active area loss due to interconnection gaps as well as shadow losses from the top Ag grid electrode. Monolithic design incurs active area loss only due to shading from the top metal grid. The main busbars (contacts) are not counted in the total area.

		Grid spacing Of the top Ag grid (mm)	Total Ar- ea (cm <sup>2</sup> )	Active Ar- ea (cm <sup>2</sup> )	Geometric fill factor (Active area/Total area)
16-stripes Serially-integrated			235	160	68.1
	Comb	0.5	100	95.8	95.8
Monolithic	Grid	5	100	87.8	87.8
wononthic	Honey Comb	7	100	94.7	94.7
	Large Honey Comb	15	100	97.3	97.3

## 5.3.1 Processing

Both serially-integrated module and monolithic modules were R2R processed following similar processing conditions. The difference was in patterning of the Al/Cr bottom electrode upon which the subsequent layers were processed. Al/Cr layer were sputtered coated on Kapton foil in two geometries. For serially-integrated modules, the Al/Cr was sputter deposited through shadow masks to process 16- stripes, each 13 mm wide and separated from the adjacent by a gap of 2 mm. We note that the same specification was found optimum in the processing of an ITO-based upscaling module known as the ProcessOne and as discussed earlier in Chapter 4. For monolithic modules, the 200 mm wide Al/Cr layer was sputter coated in the center along the webwidth (web width = 305 mm). Two monolithic modules were processed along the

Layers	Deposition	Web-speed	Drying time	Dry-layer thick-
	method	(m min <sup>⁻1</sup> )	(temperature/time)	ness
Al/Cr	Sputtering	0.01	-	100 nm/ 15 nm
P3HT:PCBM	Slot-die coating	2 .0	90 °C/ 30 sec	300 nm
PEDOT:PSS	Slot-die coating	0.30	110 °C/ 3 min	~2 μm
Ag	Screen-printing	2.0	140 °C/ 1.2 min	<5 μm

Table 5-5. R2R processing methods and parameters used in upscaling of the Fraunhofer-type modules.

width of the web. This is done by patterning during the slot-die coating of active material in two stripes, each of 98 mm wide and separated from the other by 20 mm. The rest of the stack in both serially-integrated and monolithic modules were processed using similar conditions following the patterns of the underlying layer and incorporating necessary layer offsets in the consecutive layers. Table 5-5 carries a compilation of processing methods and parameters as using in upscaling of the Fraunhofer-type modules. Layer-wise R2R processing images are shown in Figure 5-4.

In R2R processing, the drying time is limited by the oven-length. We selected the parameters that best reflected the processing conditions employed in the test cells while maintaining reasonable web-speed. The active layer was P3HT:PCBM in chlorobenzene with a mixing ratio of 21:18.5 (*wt/wt*) per ml of chlorobenzene as found optimum in the test study, however, PEDOT:PSS could not be processed to the optimum thickness determined in the test cells.



Figure 5-4 Layer-wise R2R processing of serially-integrated design: patterned sputtered AI/Cr substrate comprising of 16 stripes (a) on-to which P3HT:PCBM active layer slot-die coated (b) followed by slot-die coating PEDOT:PSS (c). The corresponding steps in the processing of monolithic modules are shown in (d-f). Screen printing of serially-integrated module (g) and MM (h) is also shown.

## 5.3.2 Photovoltaic properties of the modules

The photovoltaic properties of the large-area modules are listed in Table 5-5. The modules also show an inflection in the IV curves similar to the IV characteristics of the test-cells. Upon photo-annealing, the inflection alleviates and performance of the modules improves. serially-integrated modules demonstrates the best photovoltaic properties with the highest PCE of 0.5% on total area which corresponds to a PCE of 0.73% on active area. The poor performance of the serially-integrated modules in comparison to the test cells is as a result of difficulties encountered during processing. R2R processing of PSCs is an additive process, where one layer is juxtaposed over the previous one. The alignment of each subsequent layer is easily accomplished when the patterning of the preceding layers is straight and homogenous. In the case of serially-integrated modules, the patterns in the AL/Cr electrode ought to be perfectly straight and regularly spaced over the entire length of the roll so as to avoid alignment prob-

lems during processing of the subsequent layers. Unfortunately, this was not fully realized and the position of the Al/Cr stripes was shifted along the length of the foil. This led to problems in the ensuing processing steps, especially during the screen printing of Ag. Flat-bed screen printing is a non-continuous process where adjustment in the alignment of the screen can only be made between two printing steps and each printing step can produce several modules depending on the number of print image on the screen-printing mask. In our case, each print step processed 5 modules as the mask carried 5 print images. As a result, a large number of the modules had print defects due to misalignment causing 'shorting' of several cells in a module. This is confirmed by LBIC image (Figure 5-4). The average photovoltaic properties listed in Table 5-5 are of modules with Voc >3.5%. Of the 40 modules processed over the length of 6 m foil, only 21 modules had such a V<sub>oc</sub>.

In a serially-integrated module,  $V_{oc}$  of a module is the summation of  $V_{oc}$  of each cell whereas total current of a module is found to be a closer to the average of all the cells [15]. Therefore, a true comparison of the R2R produced module to that of the test-cells is best made with the performance of a single cell in the SI-M module. The SI-M with 16 cells should ideally give a  $V_{oc}$  of 0.4 X 16 = 6.4V based on the  $V_{oc}$  of the testcells; however, only 6.0V at best is obtained which means that even the best module has one non-functioning cell. Furthermore, PCE of the test cell should be compared with PCE on active area of the serially-integrated modules since the performance of the test cells are based active area. Hence, the PCE on active area for seriallyintegrated module is 0.74% which is nonetheless significantly lower than the test cells (1.4%). The loss in PCE is attributed to the higher PEDOT:PSS layer thickness (2  $\mu$ m) in the serially-integrated compared to the optimized test-cell (~800 nm) that results in the loss of light transmission to the photoactive layer and consequently decreases the current generation in the device. As a result, significantly lower current is harvested in the up-scaled module (4.7 mA cm<sup>-2</sup>) than the test-cells (8.0 mA cm<sup>-2</sup>). However, the PEDOT:PSS thickness was found to be critical during slot-die coating because the high viscosity of the PEDOT:PSS limits web-speed and flow-rate. Serially-integrated modules, however, display improved FF in comparison to the test-cells because of the

higher thickness of PEDOT:PSS which means higher conductivity as well as due to the lower current which means less resistive power losses ( $P_{loss} = R_s I^2$ ). If progress is made on improving coating of PEDOT: PSS and screen printing of Ag so that the optimized condition can directly be adopted, an total area efficiency of 0.90% can be expected; the difference to that of PCE obtained on test-cells is therefore as a consequence of low-geometric fill factor in serially-integrated modules in which >30% of the total area do not contribute to current generation (dead regions). A monolithic module is precisely made to avoid active area loss due to low geometric fill factor as well as to alleviate alignment problem during processing as no fine patterning is required. The low-sheet resistance of the Al/Cr electrode (500 m $\Omega \Box^{-1}$ ) as well as of the current collecting Ag grid on the top electrode (<1  $\Omega \Box^{-1}$ ) would ideally allow realization of a monolithic module.

Table 5-6 also lists the photovoltaic properties of the monolithic modules. The PCE of the monolithic modules are lower than theserially-integrated modules mainly due to lower FF and J<sub>sc</sub>. Both this effect is associated with power losses due to the top PEDOT:PSS/Ag electrode. When such a composite transparent electrode is employed, the performance of the solar cell can be affected by three prime factors attributable to the PEDOT:PSS/metal grid transparent electrode: 1) the resistive losses due to PE-DOT:PSS; 2) active area loss due to shading from the metal grids; and 3) ohmic loss due to the resistance in the silver grid lines. The contact resistance of PEDOT:PSS and Ag is also an important factor but it has been known to impose negligible resistance. Compared to the serially-integrated, monolithic modules employed varied Ag grid designs. The resistive losses that are manifested in the significantly lower FF of all monolithic and serially-integrated modules are due to several design shortcomings including larger than optimum grid spacing and the resistive losses in the grid lines. This is elaborated in the following paragraph.

	V <sub>oc</sub> (V)	J <sub>sc</sub> (mA cm⁻²)	FF (%)	PCE (%) On Total area	PCE (%) On active area
16-stripes Serial- ly-integrated	6.00 (5.9)	4.7 (4.0)	41.00 (41.00)	0.50 (0.41)	0.74 (0.60)
Monolithic					
Comb	0.33 (0.32)	2.60 (2.25)	25.3 (25.6)	0.22 (0.18)	0.23
Grid	0.45 (0.44)	3.30 (3.30)	24.4 (24.4)	0.36 (0.34)	0.41
Honey Comb	0.34 (0.34)	2.60 (2.35)	24.7 (25.2)	0.22 (0.20)	0.24
Large Honey Comb	0.43 (0.42)	2.30 (2.01)	24.1 (24.2)	0.24 (0.20)	0.24

Table 5-6 Overview of the key photovoltaic parameters after photoannealing measured under 1 Sun illumination (1000 W m<sup>-2</sup>, AM 1.5G). The best module properties are listed along with average performance (in brackets).

A study that delves into electrical modelling on composite PEDOT:PSS/Ag grid transparent electrode, while taking into account the shading losses due to Ag grids, resistive loss due to PEDOT:PSS, and resistive losses due to Ag grid lines, shows that larger than optimum grid spacing leads to rapid losses in PCE of the PSCs (Figure 5-6). An inkjet printed Ag grid structure (comb-like) with a grid width of 325  $\mu$ m and a grid height of 500 nm printed in combination with a PEDOT:PSS is found to have an optimum grid spacing (distance between two adjacent Ag lines) of 2.5-3.3 mm for use in a 2 x 2 cm<sup>2</sup> laboratory cell [16]. Lower than optimum grid spacing results in large optical loss due to shading from the metal grid dominates while larger than optimum spacing leads to large loss power losses due to resistance. In the monolithic modules explored in this experiment, grid spacing ranged between 5 mm (Grid design) up-to 15 mm (Large Honeycomb design) (See Table 5-3). Furthermore, 200  $\mu$ m wide Ag grid lines are used to transport high current in monolithic modules (up-to nearly 500 mA can be expected while only 340 mA is achieved) to a minimum distance 9 cm (distance to the



Figure 5-5 A typical 16-stripe serially integrated module (a) and its corresponding LBIC image (c). Stripe number 7, 13, 14, and 16 do not exhibit photovoltaic behavior and it is due to the misalignment during processing that lead to short circuit. A monolithic module with large honey-comb top electrode is also shown (b) along with its corresponding LBC image (d) showing homogenous current generation. Color contrast between the background (blue) and the current generation parts (yellow) in each LBIC image represents the relative amount of current

busbar/contact). The same grid lines transport much lower current (2 orders of magnitude lower) to a distance of only 1 cm in the serially-integrated modules. The resistive losses in the Ag grid lines and PEDOT:PSS is therefore the dominating mechanism for power loss ( $P_1 \approx R_s I^2$ ) in the monolithic modules which manifests in decreasing FF and reduced current in comparison to the serially-integrated modules. Among the four designs, the Comb and the Honeycomb shares a similar shading loss (Table 5-4), has similar grid spacing, and therefore display similar photovoltaic characteristics.

The Large Honeycomb based monolithic modules demonstrates relatively lower current and FF despite its significantly lower shading loss than the other designs suggest that the grid spacing in this design (15 mm) is more than optimum and large resistive losses emerge from the PEDOT:PSS. The Grid based monolithic modules with a grid spacing of 2 mm and highest shading loss (15%) demonstrate the highest current owing to its unique design where the top Ag grid which minimizes the resistive loss. The



Figure 5-6 Measured (open square) and calculate (cross) efficiency of solar cells with Ag grid/PEDOT:PSS transparent conductor in a normal architecture. The grid lines are 325  $\mu$ m wide. The curve in the solid lines accounts for ohmic loss in the PEDOT:PSS layer and optical loss due to shading from the grid lines, but does not account for the ohmic losses in the gridlines. Crosses account for all three factors. © 2013 Wiley. Adapted, with permission from ref. [16].

Grid design comprise of isolated networks of grid lines which allows current from only a small area to be harvested and transferred to a 'secondary busbar' which then channels it to the primary busbar (Figure 5-7). In the other designs, however, the Ag grids form an interconnected network throughout the module and supports very high current transport incurring large resistive losses. Hence, a higher current is collected in the Grid design despite its highest shading loss (15%) among the four designs. In all, several shortcomings in the Ag grid design can truly be evaded using mathematical models such as that demonstrated in ref. [16] to plan the best grid design for maximizing performance of the module. Furthermore, simple design elements such as varying the thickness of the Ag lines and incorporating busbars around the monolithic module to reduce the distance of the current transportation through preferably thin networks of Ag grid lines would likely improve the performance of the monolithic modules.



Figure 5-7 Grid design and Large Honeycomb designs as used in the large area monolithic modules (100 cm<sup>2</sup>) are schematically illustrated in (a) and (b) respectively. Figures are not to scale.

#### 1.5 Summary

In summary, the drawback of upscaling Fraunhofer-type modules lies in the use of chromium. Chromium oxidizes when processed in ambient conditions. In fact, when thinner chromium layer (5 nm) is used as suggested for the prototype and remaining stack is processed in ambient conditions, a severe irrecoverable inflection in IV curve is observed. Thicker Cr layer alleviate the inflection and enables ambeint processing albeit at an expense to the performance as evident in the difference in PCE of the test cells here (1.5%) to the prootypes (> 2.5%). Upscaling of the test-cells to large-area modules in a serially-intergrated structure reveals losses are mainly caused due to printing errors and inability to transfer optimum PEDOT:PSS thickness, both of which can be avoided now alleviated. In fact, currently improved formulations of PEDOT:PSS (e.g. Agfa PEDOT:PSS 5015, Clevios F010, etc.) are available which allows higher flexibility in processing maneauvers which was not present when we did this experiment. Furthermore, the comparison of the upscaling module geometries reveals that a serially-intergrated module is likely to allow full scalability of active area PCE from a laboratorty test-cell to the upscaled module but the total area PCE will always be bottlenecked by passive regions allocated for interconnections. In all, a loss of 30-40% of maximum achievable PCE will always be sacrified on the total area in a seriallyintegrated module design. The loss in geometric fill factor, of course, has implications on the cost of production. Finally, a monolithic geometry may be feasible for metal based electrode with high conductivity and can maximize geometric fill factor. In our investigation, both current and voltage are sustained in the monolithic modules as compared to the test-cells, the losses are primarily due to FF. Therefore, rigorous optimization in the grid design is necessary to recover FF. This is a topic of future investigation.

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# 6. Upscaling of Architecture 2: ProcessH

## 6.1 Introduction

ProcessH is an all-solution processed large-area module adapted from the AGNP prototype (**Chapter 3**). It is a bottom-illuminated inverted architecture and employs a simplified R2R processing scheme in the upscaling requiring only slot-die coating and screenprinting in the processing of a complete module. The transparent electrode is based on solution-processed ultra-thin Ag film. Thin metal films were explored as transparent conductor prior to the discovery and subsequent dominance of ITO and are also currently being revisited as a replacement to ITO [1]. However, the solution processing of transparent metal has not been demonstrated earlier to the best of my knowledge. The upscaling process of ProcessH was carried out in three segments: 1) development, evaluation, and optimization of the properties of the Ag semi-transparent electrode; 2) application of Ag transparent electrode in the fabrication of test cells for process optimization and setting a reference against which the upscaled modules can be evaluated; 3) Upscaling via an all-ambient R2R processing and evaluation of the performance of the upscaled modules. All three segments are consecutively reported in this section.

### 6.2 The solution-processed transparent Ag electrode

The processing and properties of the semi-transparent silver film forms the most crucial step in determining their applicability as transparent electrode in solar cells. The transparent silver film is processed by diluting an as-received non-particle based Ag ink with different solvents. The pristine Ag ink has 18 wt% loading and was purchased from Kunshan Hisense Electronic (SC-100). 1-butanol and isopropanol were found to be the most suitable solvents for dilution. Customized inks were prepared by varying the dilution factors in both solvents. The diluted inks were spin coated at 1500 rpm for 30-45 seconds on PET substrate affixed on a glass slide. Once coated, the film is transparent which upon drying/annealing at 140 °C on a hot-plate immediately transforms into a highly reflective semi-transparent Ag film. All silver transparent films were annealed at 140 °C for 2 minutes. The resulting film, henceforth termed as Ag transparent electrode or Ag TE, is highly homogenous and smooth with an rms line roughness



Figure 6-1 Optical transmittance profile of semi-transparent Ag electrode based on ink prepared with isopropanol and 1-batonal dilutions (left). IV curve of the best test-device is shown (right) which is based on isopropanol dilution of the Ag ink.

of 2 nm measured over a length of 1  $\mu$ m. These films of Ag TE were studied for sheet resistance and optical transmission.

Figure 6-1 shows the transmission profile the Ag diluted with the two different solvents. Although the transmittance of 1-butanol based dilution is much higher compared to isopropanol at all dilution factors, however all films with 1-butanol exhibit higher sheet resistance (Table 6-1). Therefore, Ag/isopropanol with 1:5 (v/v) dilution was used in the subsequent processing of semi-transparent Ag electrode primarily on account of its lower sheet resistance at a relatively lower expense to optical transmission.

#### 6.3 The Test-cells

### 6.3.1 General Materials

Silver for the semi-transparent back-electrode is a non-particle based conductive ink (loading of 18 wt%) purchased from Kunshan Hisense Electronic (SC-100). The aqueous zinc oxide solution was precursor-based prepared as described earlier [2]. The active layer was a mixture of poly (3-hexylthiophene) (P3HT) (Sepiolid P200, BASF) and phe-nyl-C61-butyric acid methylester (PCBM) (99%, Solenne B.V.). The active ink was pre-pared by dissolving P3HT:PCBM (1:1; wt/wt) with a total solid concentration of 60 mg



Figure 6-2 Transmittance profile of the semi-transparent Ag electrode used in ProcessH modules. The addition of ZnO layer causes ~50% increase in transmittance of the Ag TE. The transmittance of PEDOT:PSS transparent electrode as used in Fraunhofer-type modules is given for comparison as well as the absorbance profile of P3HT is shown to depict the region of interest (*left*). A typical evolution of IV curve of an as-produced ProcessH modules (*right*)

in 1 ml of solvent. The solvent was a mixture of 1-chloronaphthalene (5 vol%) and (95 vol%) chlorobenzene. PEDOT:PSS (Orgacon EL-P 5010) was purchased from Agfa and diluted with isopropanol in a ratio of 2:1 by weight. A UV curable silver paste from Toyo (Rexalpha RA FS FD 018) was used for screen printing the interconnections between the cells in a module. The substrate for the test-cells was polyethylene terephthalate (PET) from Melinex and the substrate for upscaling was barrier foil purchased from Amcor. Amcor barrier foil was also used for encapsulation of the modules. The barrier had a thickness of 55  $\mu$ m and a UV filter (cut-off at 390 nm). The barrier performance was 0.01 cm<sup>3</sup> m<sup>-2</sup> bar<sup>-1</sup> day<sup>-1</sup> with respect to oxygen (measured according to ASTM D 3981) and 0.04 g m<sup>-2</sup> day<sup>-1</sup> with respect to water vapor (measured according to ASTM F 372-78). For the module encapsulation the barrier foil was pre-laminated with a pressure sensitive adhesive (467MPF) from 3M.

#### 6.3.2 Processing and photovoltaic properties

Upon the semi-transparent Ag film, test cells of 0.25 cm<sup>2</sup> (0.5 X 0.5 cm<sup>2</sup>) were fabricated by spin coating ZnO, P3HT:PCBM, and PEDOT:PSS consecutively at 1000 rpm, 600 rpm and 1000 rpm respectively. The deposition of ZnO and PEDOT: PSS was each followed by a drying step at 140 °C for 5 minutes while P3HT:PCBM was left in the air for

2 minutes to dry. The back Ag electrode was evaporated. The IV curve of a best cell is shown in Figure 5-1 along with the key photovoltaic parameters. All test cells on semitransparent silver substrate were marked by high FF in access of 50% owing to the low roughness and high sheet resistance of the Ag film. However, current density is much lower due to the limited transmittance of the Ag film. Nonetheless, the photovoltaic properties of the best test-cells are much higher and on average are similar to those observed in the Fraunhofer-type test cells (Table 6-1). Furthermore, no inflection was observed in the IV curves. Note that the AGNP prototypes evaluated in Chapter 3 and the test-cells reported herein had no changes in the processing conditions. The only difference was in the area of the cell, which was scaled down according to the intended upscaling structure (reported in the next section). Nonetheless, the scaling of device area in the test cells from 0.25 cm<sup>2</sup> to 1 cm<sup>2</sup> does not significantly change results and on average a power conversion efficiency of ~1% is achieved.

## 6.4 The R2R Produced Modules

#### 6.4.1 R2R Processing of silver transparent electrode

The optimized Ag ink for transparent electrode with isopropanol dilution as used in the test cell could not be employed in the R2R processing. This was purely a technical issue. In our R2R setup, the slot-die head is located directly above the convection oven (Chapter 4, Figure 4-2). The combination of low boiling point of isopropanol (80 °C) and the hot air from the oven results in defects (big pores) in the freshly printed semi-

Table 6-6-1	Sheet	resistance	of semi-transpa	rent Ag fil	ms upor	dilution	with	1-butanol	and	iso-
propanol at	differer	nt volume r	atio.							

Ag:solvent	Ag: 1-butanol		Ag: isoprop	anol	Ag:1-butanol		
(v:v)	(spin coated)		(spin coate	d)	(R2R gradient test)		
	Sheet re- sistance $(\Omega \square^{-1})$	Transmittance at 550 nm	Sheet resistance $(\Omega \square^{-1})$	Transmittance at 550 nm	Sheet re- sistance (Ω □ <sup>-1</sup> )	Transmittance at 550 nm	
1:5	29	43 %	5	28 %	17	20 %	
1:6	46	51 %	9	38 %	34	30 %	
1:7	1000	53 %	10	38 %	103	39 %	

transparent Ag film. In order to avoid it, 1-butanol which has higher boiling point (117 <sup>o</sup>C) was used as the preferred solvent for dilution although it was not the optimized choice in the test cells. A more refined and accurate optimization of the ink was carried out by a R2R gradient coating analysis wherein solutions from two sources are differentially pumped and mixed en route to the slot-die head which is ultimately coated on PET substrate. In this way, Ag films are coated on the substrate with varying mixing ratio of the two ink sources. A complete R2R gradient analysis set-up is described elsewhere [3]. Such a screening method enables the probing of a wide parameter space and allows accurate reproducibility of the processing conditions as the gradient test was done on the same R2R equipment using slot-die coating which similar to that employed in the processing of the modules. In this test, Ag:1-butanol (1:5 v/v) was one of the ink source which was linearly diluted with 1-butanol before slot-die coating on barrier foil at 2 m min<sup>-1</sup>. The resulting Ag films were studied for transmission and sheet resistance. Silver ink dilution with 1:5 (v/v) was found most suitable for further processing of the modules. It had a sheet resistance of 17  $\Omega$   $\Box^{-1}$  at a transmittance of 20% (at 550 nm). Note that the R2R test shows different results than the test optimization with spin coating due to different thicknesses of the films in the two cases despite the similar ink. The thickness of the films could not be measured either with AFM or Dektak due to their ultra-low thickness and the use of the plastic substrate. Nonetheless, the R2R coated films are thicker than spin coated as optical transmission is reduced while the sheet resistance is improved compared to the spin-coated film at the same mixing ratio of the solvent to the Ag ink. .

The addition of ZnO layer causes improvement in the transmission of Ag TE/ZnO to 30% at 550 nm. This enhancement in transmittance upon addition of ZnO to the Ag film is most likely caused by surface plasmon resonance (SPR) effects at the Ag/ZnO interface [4]. SPR effects in multilayer structures of ZnO with noble metals can enhance both transmittance and conductivity of ZnO and is a widely studied material for its potential as an ITO replacement [5]. SPR relies on surface plasmons of metal nanoparticles whose effect is sensitive to size and shape of the nanoparticles. The effect of SPR diminishes with larger size of Ag islands/particles as studied by Zhang et al. [4]. SEM



Figure 6-3 Microstructure of Ag semi-trnasparent film. Porosity and interconnected network of Ag islands could be seen; (b) Magnified image of porous regions as seen in (a). Un-coalesced dispersed Ag nanoparticle (size <10nm) are visible; (c) EDS taken in the open areas confirming the presence of Ag in these area albeit at lower amount. (d) EDS on Ag particle. The silver island of <10 nm areascribed to the enhancement in transmission upon the addition of ZnO.

analysis revealed the presence of un-coalesced Ag islands of <10 nm sizes within the large pores in the morphology of the Ag TCE. It is likely that these islands are mostly responsible for transmittance enhancement due to SPR as sizes in other studies (Figure 6-3). Subsequently, the R2R optimized Ag ink with 1-butanol dilution (1:5 v/v) was applied in the fabrication of large-area modules.

## 6.4.2 Module Design

A serially-integrated module architecture was selected that comprised of 16 interconnected cells. The resulting total aperture area of the module was 54 cm<sup>2</sup> and the corresponding active area was 35.5 cm<sup>2</sup>. Hence, the geometric fill factor was 66%. The width of the active part of the strip was 3 mm which was kept similar to the test-cells while the interconnection gap was 1 mm. Because of the narrow width of the cells, the top Ag electrode was printed only for interconnection between the cells.

Layer	Deposition	Web-speed	Drying conditions	Dry-layer
	method		Temperature/Time	thickness
Semi-transparent Ag	Slot-die	2.0 m min <sup>-1</sup>	140 °C /2 min	100 nm
ZnO	Slot-die	2.0 m min <sup>-1</sup>	140 °C /3 min	100 nm
P3HT:PCBM	Slot-die	1.4 m min <sup>-1</sup>	140 $^{\circ}$ C /3 min	~425 nm
PEDOT:PSS	Slot-die	0.5 m min <sup>-1</sup>	140 °C /8 min	<mark>~2 μm</mark>
Ag	Screen-print	2.0 m min <sup>-1</sup>	UV curing (2X420 mJ cm <sup>-2</sup> )	<5 μm

Table 6-6-2 R2R processing details as employed in the upscaling of ProcessH

## 6.4.3 R2R Processing of the ProcessH modules

The modules were directly fabricated on barrier foil, thus eliminating the need for a separate PET substrate. Once processed, the module need be encapsulated only from one side. PET imposes a large environmental foot-print in the raw materials incurred in the fabrication of PSCs [6,7]. Prior to processing of the functional layers, the barrier foil (web-width of 305 mm) was heat stabilized to avoid shrinkage that could otherwise lead to registration problems in the subsequent coating and printing steps. This was accomplished by running the web through the ovens (4 m) with a temperature 140 °C with a web speed of 1 m min<sup>-1</sup>. The cross-directional shrinkage was ca. 0.6 %. Thereafter, subsequent layers were processed in an all-ambient R2R process using only slotdie coating of all layers apart from the top silver for interconnection which was screen printed. Figure 6-4 shows pictures of step-wise R2R processing of each functional layer and Table 6-2 summarizes the processing parameters.

#### 6.4.4 The photovoltaic properties of ProcessH modules

Unlike the test cells, all modules displayed a dynamic photovoltaic behavior. The initial IV curve when the modules were illuminated under the solar simulator (1000 W m<sup>-2</sup> AM 1.5) was marked by a strong S-shape. Prolonged exposure under the solar simulator (light soaking) causes evolution of the IV curve to a normal J-shape IV curves. The dynamic photovoltaic performance of the modules is caused by metastable photoconductivity of ZnO [8,9]. The conductivity of ZnO improves upon photo illumination as a result of elimination of adsorbed oxygen on the surface of ZnO. UV exposure induces photo excitation in ZnO (band gap of 3.2 eV) and the resulting hole-generation leads to oxygen desorption, consequently increasing conductivity of ZnO. Furthermore, the UV

filter in the barrier foil/substrate (cut off at 390 nm) also slows down the mechanism of oxygen desorption from ZnO surface as less than 2% of the light wavelength that could induce photo-excitation in ZnO (363 nm) is transmitted to the ZnO layer [10]. The UV filter in the barrier foil is essential for prolonging the stability of the device as UV induces photo-degradation in the organic solar cell. While conductivity improvement of ZnO upon UV exposure is a gradual process and even more so for our modules receiving limited amount of UV light. However, directly injecting holes by increasing reverse bias also results in oxygen desorption and ultimate increase in ZnO conductivity [11]. Table 6-3 shows the effect of increasing reverse bias on the on the duration of evolution to peak efficiency. The absence of inflection in the IV curves of the test cells could be due to the evaporation of the back electrode which can minimize the ad-



Figure 6-4. Step-wise R2R processing of ProcessH modules with slot-die coating of semitransparent Ag electrode, ZnO, P3HT:PCBM, and PEDOT:PSS respectively in (a-d); screen printing of Ag showing 6 modules are being printed in each print step (e); R2R encapsulation (f). The transparency of the slot-die coated highly conductive Ag film on barrier foil is shown in (g) and a complete module is shown in (h).

sorbed oxygen on ZnO surface. Based on the result of the test cells, the up-scaled module should ideally deliver:  $V_{oc}$ : 8V;  $J_{sc}$  : 5.3 mA cm<sup>-2</sup>; FF: >50%. However, the best module demonstrated a peak photovoltaic performance with PCE: 0.44%;  $V_{oc}$ : 5.8V, FF: 40.3 % and  $J_{sc}$  = 2.6 mA cm<sup>-2</sup>. Analysis of the IV curves at the peak performance reveal that the series and shunt resistance in the modules suffer by 33% and 400% respectively in comparison to the best test-cell. The increased series resistance in the modules is a direct consequence of the much lower conductivity of the R2R processed Ag TE in comparison to the ones employed in test-cells (Table 6-3). On the other hand, the decrease in shunt resistance by 400% is more significant as it was not expected.

Further investigation revealed that the use of the barrier substrate was primarily responsible for reduced shunt resistance. Figure 6-5 shows the surface roughness of Alcan barrier foil and Melinex PET used in processing of modules and the test devices, respectively. The surface of the barrier foil is highly inhomogeneous and carries spikes reaching 2  $\mu$ m in height. On the other hand, Melinex PET is very smooth with no spikes. When Ag ink is deposited on these substrates, the surface topology of the Ag film mirrors those of the substrates. Furthermore, the loss of current in the modules compared to the test-cells and the prototypes are due the active area destruction from screen printed Ag used for interconnection as evident in the LBIC images (Figure 6-6).

Table 6-3 IV characteristic of modules at peak performance during photo-annealing. The brackets for test cells shows the average while modules shows the current of the whole module (=average of the cell)

	Applied	V <sub>oc</sub>	$J_{sc}$	FF	PCE	Time to peak efficiency
	bias	(V)	(mA cm )	(%)	active	during photoannealing
					area	(h)
					(%)	
Test cell	-	0.51	5.34	51.48	1.61	-
			(4.38)	(51.45)	(1.22)	
Module 1	- 20 V	6.8	2.81(5.8)	40.3	0.44	21.15
Module 2	- 30 V	6.8	1.45(2.9)	41.9	0.23	10.07
Module 3	- 40 V	5.7	1.4 (2.8)	41.8	0.23	5.66

As discussed in Chapter 3, due to the transmittance profile of the Ag TE that had higher transmission in the 500-600 nm range, a significant contribution to photocurrent was expected from toward the back of the cell (cf. Figure 3-4). The destruction of the active layer in this region therefore limits the current harvest.



Figure 6-5 Optical profilometry (white light interferometry) images showing the surface roughness of Alcan barrier foil (left) and Melinex PET (right).

#### 6.5 Summary

ProcessH has a comparative advantage in comparison to any of the known architectures (ITO-based ProcessOne, and all archtiectures architectures upscaled under this PhD study) in that: 1) it is a complete solution-based process free of vacuum steps; 2) it does not need glovebox and can be processed under ambient conditions; 3) it is resourceful in terms of the amount of Ag required in the processing of the Ag TE and in the number of different materials or layers in the stack; 4) it incurs only two printing or coating techniques (slot-die coating, and screen printing), both of which are the least expensive and efficient methods where material wastage often is very little or nil; and 5) it can be processed directly on barrier foil eliminating the need for a separate PET substrate such as that required in ITO-based ProcessOne or expensive Kapton foil required in Fraunhofer-type module.



Figure 6-6 LBIC mapping of a module from the semi-transparent Ag side( left) and from the PE-DOT:PSS side (right). Image of the actual module is displayed to the right of the LBIC images. The right LBIC shows more than half of each cell when images from the back side with reduced current generation while this effect is observed in the front cell affirming that the harmful solvent has not diffused completely through the 425 nm thick active layer.

In this upscaling experiment, the test-device demonstrated a PCE of >1%, thus passing the threshold we had set as minimum requisite for upscaling. In the upscaling, however, several technical problem emerged which ultimately limited the performance of large-area R2R processed The main challenge was the fact that the optimized processing conditions of the test device especially the processing of Ag TE could not be directly transferred to R2R processing, and the roughness of the barrier substrate further limited the PCE of the large-area modules. Nevertheless, both challenges are surmountable and it is safe to say that ProcessH can deliver a PCE of 1% when these challenges are overcome.

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# 7. Upscaling of Architecture 3: IOne

## 7.1 Introduction

IOne modules are adapted from ASP architecture as introduced in Chapter 3. It is a bottom illuminated inverted architecture where the transparent electrode is a combination of silver grid/PEDOT: PSS. The subsequent layers are processed on top of this transparent electrode. While the printing of silver grids on flexible foil is widely pursued in the printed electronics industry; however, these grids are generally standalone circuits for which conductivity is the only parameters to be optimized. In solar cells, however, the printed Ag grids need to be optimized for competing parameters when used as transparent electrode. These parameters are: conductivity, surface coverage or shading, and topology and roughness. The printed grid should be as narrow as possible to minimize shading losses, which inadvertently requires raising the topography (height) of the grid lines to gain conductivity. However, the raising of the grid lines could lead to short circuits due to "shunting" of the solar cells due to the intercalation of bottom Ag grids electrode into the opposite electrode. Polymer solar cells (PSCs) are less tolerable to high roughness of the bottom electrode as the opposite electrodes are merely separated by a distance determined by the thickness of the inbetween layers, that is, a thin metal oxide buffer layer (>100 nm) and the photoactive layer (usually < 400 nm). Therefore, the surface planarization of the grids is critical for it can become fundamentally impossible to erase a rough structure when the roughness of the preceding layer is larger than the film thickness of the succeeding layer(s) [1]. Taking all these arguments into account, it is empirically safe to say that the grid height should be around 100 nm which is the intended thickness of the planarization PEDOT: PSS layer [2]. Although higher grid height can be planarized using thicker PE-DOT:PSS planarization layer but this would reduce light transmission due to absorption by the PEDOT:PSS planarization layer [2]. Hence, in the development of Ag grids/PEDOT:PSS as transparent electrodes, the design and topology of the grid is a major concern as larger surface coverage of the metal grids lead to loss of active area due to shading from the grids and raised height of the grids can result in shunting as subsequent layers are processed on top of this electrode. A rigorous optimization is required among several parameters: 1) grid aspects (height versus width) that dictates conductivity and shading; 2) grid design that dictates surface coverage and shading loss; 3) the type of silver ink that can affect conductivity, the roughness, and the quality of the surface of the printed grids: 4) the roll-to-roll (R2R) processing techniques employed in the printing of the grids which can determine the feasibility and adoptability of a particular design depending on the dimensionality and the resolution limit of the technique. Furthermore, the processing techniques can cast influence on the film properties of the printed grids as well as on the low-cost overall objective of pursuing Ag grid/PEDOT:PSS as ITO-replacement in the first place.

Prior to this PhD study, various techniques have been reported on the processing of Ag grids as transparent electrodes (TCE) in small area laboratory cells such as diffusion transfer reversal [3], screen printed with embedded grids in the substrate [4]; evaporated [5], inkjet printed [5,6]; however, seldom were they pursued on flexible substrates and on large-area. In fact, only 0.5% of all reported scientific papers of PSCs have been demonstrated on flexible substrates [7]. Additionally, none of the reported literature employed a complete solution processing as the back electrodes in all cases were evaporated.

In the upscaling of IOne, the main challenge in the realization of functional modules or cells based on Ag grids/PEDOT:PSS transparent conductor was in finding the most suitable R2R processing technique that allows the realization of the desired properties of the Ag grids TCE on large-area flexible substrates. The uses of flexible substrates imply limited thermal capacity of the substrate to withstand high temperature sintering conditions. For example, PET can sustain its dimensional stability up-to 150 °C. Hence, the most time consuming part in development of IOne was in the finding the most suitable technique in the printing of the Ag grids TCE suitable for application in PSCs. Accordingly, the development of IOne comprised of three consecutive

stages that include: 1) the evaluation of three R2R techniques in the printing of Ag grids on flexible substrate for application in PSC; 2) the evaluation of the functional feasibility of the Ag grids as TCE in test cells and determining the most suitable method for use in upscaling of large-area modules; and 3) the R2R processing and investigation of large-area IOne modules. All three segments are consecutively reported in this chapter.

### 7.2 R2R Processing of Ag grids for transparent electrode

Three R2R processing techniques were evaluated in the printing of Ag grids on flexible substrate PET: inkjet printing, flexographic printing, and thermal imprinting. All three techniques are described in Chapter 4. Thermal imprinting was carried out at a partner institution. The pattern comprised of 14 stripes with a length of 250 mm and width of 13 mm. These stripes were patterned with the diagonal print with 14 stripes spaced by 2 mm. The processing comprised of two steps. The first step was thermal imprinting of the intended grid design and was accomplished oat a web speed of 0.96 m min<sup>-1</sup> and force of 100 KgF. The imprinted pattern was filled with silver at the same web speed and dried at 110°C for 3 minutes. The nominal width was 15 µm and height was 10 µm. The inkjet printing and flexographic printed grid were based on a hexagonal pattern with a repeat of 2 mm and the intended line-width was 100 nm. In the flexographic printed grids, the nominal grid width of 100 nm resulted in the effective printed line-width of 130  $\mu$ m. The nominal grid width in inkjet printed silver was set as 80 µm as the printed grid was expected to possess a larger effective width due to ink spreading. The final printed lines had an actual width of 130  $\mu$ m as well, similar to the flexography printed lines (Figure 7-1). The height of inkjet printed grids (lineheight) was 300 nm whereas inhomogeneities due to viscous fingering in flexographic printing were observed to result in line-height up-to 700 nm. 16 stripes were printed with a width of 13 mm each and a gap of 2 mm. The surface profiles of the printed grids are shown in Figure 7-1. All three techniques employed water-based Ag ink and were all processed on 130 µm thick PET Melinex foil. Further details on the processing could be allocated in ref. [8].
Table 7-1 A comparison between conducting electrodes based on thermally imprinted and silver filled, flexographically printed, and ink jet printed grids using parameters covering cost, easy, processing and physical parameters. The table first appeared in our publication. © RSC Publishing. Adapted, with permission from ref. [8]

	Thermally imprinted	Ink jet printed	Flexo printed
Speed (m min <sup>-1</sup> )	0.48	2	25
Maximum possible speed (m min <sup>-1</sup> )	6	70	200
Number of steps	2	1	1
Ink type	Nanoparticles	Nanoparticles	Nanoparticles
Water as solvent	Yes	Yes	Yes
Cost of master	Medium	Free (digital)	Low
Optical transmission of substrate/grid	82%	77%	75%
Resolution (micron)	16 (XX)	100 (42)	100 (32)
Printed height (nm)	0 ± 25	+150 ± 25	+200 ± 150
Spikes (nm)	20	50	1000
Technical yield	High	High	High
Conductivity ( $\Omega \Box^{-1}$ )	10	60	11

Each technique has its own advantages and disadvantages. Embedding the silver grids in the substrate by thermal imprinting allows a controlled solution to the issue of topology, conductivity, and shading loss. The embedded grids are characterized by smooth surface and high aspect ratio, thereby enabling higher conductivity at relatively lower shading loss than the non-embedded grids processed via inkjet or flexo-graphic printing. However, the processing of embedded grids is more intricate and is based on two processing steps involving thermal imprinting and silver filling. Each of the processing steps is accomplished at lower web-speed speed compared to ink-jet printing and flexographic printing. The maximum achievable web-speed for thermal imprinting is significantly lower than either inkjet or flexographic printing. Here, a processing speed of 0.96 m min<sup>-1</sup> was applied in both processing steps which were performed in discrete steps. Inkjet printing and flexography printing, on the other hand, are fast processing methods. However, they offer lower resolution and much less control over aspects of the printed features than thermal imprinting (such as ink

spreading etc.). A holistic comparison of the three techniques is presented in Table 7-1.

#### 7.3 The Test cells

#### 7.3.1 Processing

Unless reported herein, all materials are similar to that described in Chapter 6. In order to determine the functional feasibility of the R2R printed grids in PSCs, they were incorporated in fabrication of R2R single cell test devices. The foils with inkjet printed, flexographically printed and thermally imprinted silver grids were spliced into one roll with a length of 150 m. All subsequent processing was carried out on the same roll in the same processing step in order to keep variation as low as possible. PEDOT:PSS (Hereaus PH1000) was rotary screen printed on top of the grid structure with a printing speed of 10 m min<sup>-1</sup> and dried using a 1.5 kW infra-red heater and a 2 meter oven at 140 °C. The remainder of the processing involved slot-die coating of a ZnO nanoparticle suspension in acetone with a web speed of 5 m min<sup>-1</sup>, followed by drying through two through two sets of 2 m long convection ovens at 70 °C and 140 °C respectively. This was followed by slot-die coating of active (1:1 wt/wt with a total concentration of 2 wt% in cholorobenzene) at 2 m min<sup>-1</sup> and drying through the first oven at 90 °C and the second oven at 140 °C. PEDOT:PSS (EL-P 5010) was subsequently slot-die coated at 0.6 m min<sup>-1</sup> through the first oven at 120 °C and a 1.5 KW infra-red heater, followed by a second oven set at 140 °C. Finally silver back electrode with linear grid lines and bus bar (comb structure) with a thickness of 0.2 mm and a repeat of 1 mm was screen printed through a flat-bed R2R screen printing station at a webspeed of 1 m min<sup>-1</sup> and dried at 140 °C through a 1.2 m oven, making the residence time in the oven of 1.2 min. All devices required functionalization that was achieved by running a short pulse of high voltage through the device as explained later in the chapter. The solar cells were then encapsulated using UV curable adhesive between two sheets of barrier foil. Running the foil through a laminator with a nip pressure of 150 kg over the width of the foil allows the adhesive to flow over the device resulting



Figure 7-1 Schematic illustrations of the different grid structures printed by three the three defferent techniques--the thermally imprinted grid with Ag filling (top), Inkjet (middle) with an illustration of the occasional presence of misfired ink droplets and the irregular structure of the grid lines, as compared to the more regular flexographically printed grids (bottom). Shown alongside are optical pictures (scale bar is 100 mm) and surface profile line-scan across the grid lines showing typical width and height. The last column are the topography image taken from confocal microscope. Figure reprinted from the original publication. ©2013 RSC Publishing. Adapted, with permission from ref [8].

in homogenous and thin adhesive on both sides of the cells. Finally, the adhesive was cured under a metal halide based solar simulator (1000 W m<sup>2</sup>, 85 °C) for two minutes.

# 7.3.2 The photovoltaic Properties

All devices were then characterized under a metal halide lamp equipped solar simulator (1000 W m<sup>2</sup>, AM 1.5G, 85 °C). The key photovoltaic parameters are listed in Table 7-2 and the corresponding IV curves are shown in Figure 7-2. The photovoltaic performance of previously reported ITO-based R2R processed single cell on flexible substrate, known as ProcessOne [9], is also listed for comparison.



Figure 7-2 IV characteristics of the three types of devices, as measured in the lab at 1000 W m-2; AM1.5G; 85 oC (a). The transmittance profile through the different grids are shown in (b) and a picture of a R2R processed test- cell (6 cm x 1 cm) seen from the screen printed back Ag electrode (c). Figure reprinted from the original publication. ©2013 RSC Publishing. Adapted, with permission from ref. [8].

Among the three different processing methods used in the printing of Ag grid TCE, the test cells based on the embedded grids gave the highest PCE, closely followed by the flexographic grids; the test cells with inkjet printed grids showed less than half the PCE in comparison to the other two techniques. The solar cells based on flexographic and imprinted grids are characterized by high fill factor in excess of 50% ascribed to the high sheet resistance of Ag grids of ~10  $\Omega$ <sup>-1</sup> while test cells on inkjet printed grids are marked by low FF due to the higher sheet resistance (60  $\Omega$ <sup>-1</sup>). The conductivity of the inkjet printed grids can be improved in future experiments by improving upon the sintering and wetting conditions. The difference in the sheet resistance of the inkjet printed girds and the other two techniques can be explained by the difference in their materials and processing.

In this experiment, inkjet printing of the grids employed a different ink system (SunChemical Suntronics U7508) than used in the other two techniques (PChem associaciates, PFI-722). Furthermore, they were annealed only for 2 minutes at 140 °C (web-speed of 2 m min<sup>-1</sup> and combined oven length of 4 m) in convection ovens. The flexographically printed grids, on the other hand, were annealed under IR ovens in addition to annealing in two convection ovens (albeit for much shorter duration in the convection oven owing to the fast web-speed 25 m min<sup>-1</sup>), while the embedded grids

	Imprinted	Flexo	Inkjet	ITO-based Proces-
				sOne*
PCE (%)	1.92	1.83	0.75	0.97
J <sub>sc</sub> (mA cm⁻²)	7.06	7.02	4.27	7.10
V <sub>oc</sub> (V)	0.50	0.51	0.50	0.48
FF (%)	54.7	51.2	35.1	28
Width of the	13	13	13	9

Table 7-2 IV-data comparison for the three device types, measured both under simulated light 1000 W  $m^{-2}$  AM 1.5G

were annealed only in convection over at 140 °C for 3 minutes. Hence, a more rational comparison of the inkjet printable grids can be made with the embedded grids as processing of Ag employed similar sintering conditions in both these methods. The inkjet printed grids employ inks having smaller Ag nanoparticle size as well as are highly stabilized Ag nanoparticle suspensions containing varied organic stabilizing compounds such as ethylene glycol and polyvinyl polypropylene. Particle size distribution analysis showed that inkjet printed silver have a size distribution of 45 ± 9 nm whereas Ag used in embedded grids have a size distribution of 217 ±37 nm. The larger net grain boundaries in inkjet printed can impede charge transport especially if organic compounds are not completely eliminated and tend to remain at the grain boundaries around the surface of the nanoparticles [10].

Using faster heating methods such as flash sintering or IR annealing as employed in the flexographic printed grids would allow overcoming this challenge. IR annealing allows faster heating than convection ovens as evident in the difference between the surface morphology of the Ag nanoparticles (Figure 7-3) between the embedded grids and the flexo- grids. Both these technique employed the same ink, however, the embedded grids were annealed only in convection oven at 140 °C for 3 minutes and the flexographic printed grid which were annealed at 140 °C for 10 seconds in convection oven followed by IR annealing in 2x1.5 KW dryers. Despite the similar ink, the Ag nanoparticles in the flexographically printed Ag grids have coalesced whereas the Ag nanoparticles in the embedded grids have not. While this



Figure 7-3 SEM images of the nanoparticles for the three different silver electrodes (top) with corresponding optical images below. The grids prepared by thermal imprinting and silver filling are shown with a low degree of magnification due to larger particle size (right). The ink jet printed (middle) and flexographically printed grids (right) are shown with the same magnification. Figure reprinted here from our original publication. ©2013 RSC Publishing. Adapted, with permission from ref. [8]

should result in higher conductivity of flexographic printed grids than the embedded ones; however, similar sheet resistance of the Ag grid is observed for both techniques. This is because the Ag nanoparticles in the embedded grids are marked by higher densification whereas flexographically printed silver have coarsened leading to large pores in the morphology. Nonetheless, the effect of IR annealing may be sufficient to remove organic compounds in inkjet printed grids.

Lastly, the inkjet printed grids were prone to large defects and inhomogeneities in the print quality due to misfiring of the ink droplets, blocked nozzle (s) as well as poor coalescing of the printed lines as observed in the separation between the printed lines that are perpendicular to the printing direction (Figure 7-4). The latter can be evaded in future by further optimization in the wetting properties of the substrate and the ink. All these effect explain the high sheet resistance of the inkjet printed grids.



Figure 7-4 LBIC images of devices based on the thermally imprinted grid (a), ink jet printed (b), and flexographic printed (c). The small inserts show photos of the actual cell with strong backlighting. Flexographic printed grids are most uniform while inkjet printed grids and have comparatively smaller shading loss despite the similar line width as inkjet printed Ag grids. Inkjet printed grids lines have identifiable defects due to misfired ink-droplets (green circle) and uncoalesced printed lines (red circle). The arrow shows the printing direction. The picture is first appeared in our original publication. 2013 RSC Publishing. Adapted, with permission from ref. [8].

Nonetheless, the solar cells based on all three different printed grids were functional and the photovoltaic performance in the case of flexographically printed and embedded grids far exceeded the photovoltaic properties reported of R2R processed single cells based on ITO (ProcessOne). This is possible because of higher FF (>50%) achievable with the use of Ag grid/PEDOT:PSS transparent electrode than reported on ITO-substrates [9]. The relative difference in the photovoltaic properties of the test cells based on the three Ag grid printing techniques is a direct consequence of their difference in the properties of the printed films --optical transmission, conductivity, as well as surface properties as noted in Table 7-1. Among the three different techniques, the embedded grids and the flexographic grids resulted in similar PCE of the test-cells(Figure 7-2; Table 7-2) while the inkjet- printed grids led to the poorest performing devices due to the high sheet resistance of the grids which manifest as the lowest FF compared to the other two techniques. In case of the latter, improvement in annealing, for example, by flash sintering, would improve the conductivity as discussed in the preceding paragraphs. In all cases, further improvement in the printing of the grids including the lowering of the thickness and width of the grids to minimize shading loss, a PCE exceeding 2% can be realistically expected.

In all, the R2R test cells based on IOne presented the highest performance compared to the test cells of the other two architectures: the Fraunhofer-type (Chapter 5) and the ProcessH (Chapter 6). In fact, the IOne test cells showed higher photovoltaic properties than reported for flexible ITO-based R2R coated devices by our group. In the upscaling into large-area modules, flexographic printing was adopted as the most cost-effective method toward the achievement of low-cost processing of ITO-free modules on account of its highest web-speed compared to the other two techniques despite at a slight compromise in photovoltaic properties as compared solar cells processed on embedded grids.

#### 7.4 The R2R produced IOne modules:

This section describes the process of upscaling of the *IOne* structure from the R2R single test cells as reported in the previous section to R2R processed large-area modules with areas exceeding 180 cm<sup>2</sup>. The modules are processed completely under ambient conditions in an all-solution process using a combination of R2R printing and coating methods. Several cost improvement measures were adopted in the large-area processing. The variations observed in the properties of prototypes, the R2R test cells, and the R2R large-area modules are also discussed. This section reports that IOne modules deliver a PCE above >1% on >100 cm<sup>2</sup> module area, thus satisfying the target of this Ph.D. study. These modules are further investigated for operational stability under rigorous simulated and real conditions following several ISOS protocols [11]. The IOne modules are further investigated for mechanical stability under several bending tests. All results on scalability, stability, and flexibility of IOne modules are comprehensively presented in this section.



Figure 7-5 Schematics of a representative module with three serially- interconnected cells. The number and length of cells were varied depending on the required module area (left); and a picture of a module with 7 serially connected cells taken from the transparent electrode side. The picture is adapted from our first publication. © Elsevier. Adapted with permission from ref. [21]

# 7.4.1 Module design

A serially-integrated module design was fabricated starting with the patterning of the flexographically printed Ag grid in the form of several stripes (13 mm wide, 2 mm gap) similar to that used in the upscaling of Fraunhofer-type. The Ag grid was printed in hexagonal pattern. The grid had a nominal line width of 100  $\mu$ m, a thickness of 200 nm, and the distance between two parallel sides in a hexagon of 2 mm. The active area width was 10 mm. The length of the stripes were varied (6, 10.3, and 13.5 cm) to get modules with three different total areas of 175.5, 102.0, and 32 cm<sup>2</sup>. The design is schematically shown in Figure 7-5 along with a picture of the final module.

# 7.4.2 Processing

The processing of all layers were carried out using R2R printing and coating in ambient conditions. The processing methods were similar to those used in the IOne test cells except the substrate employed in the large-area modules was a thin barrier foil from Amcor (45  $\mu$ m). The web-width was 305 mm. Stepwise processing of the Ione module is shown in Figure 7-6. At the time of this experiment, DTU lacked R2R encapsulation. Therefore, the modules were randomly cut from the roll and were manually encapsulated between two sheets of Amcor barrier foil using a UV curable adhesive from DE-LO<sup>®</sup>. The modules were then passed under nip pressure in a R2R machine with <1 m min<sup>-1</sup> to achieve homogeneous distribution of the adhesive over and under the mod-



Figure 7-6: Photographs of the stepwise R2R printing and coating processes in fabrication of the modules: (a) flexography printing of Ag grid; (b-d) slot die coating of hcPEDOT:PSS, P3HT:PCBM, and PEDOT:PSS respectively; (e) flat-bed screen printing of Ag paste; and (f) final module after step (e). The picture is adapted from our first publication. © Elsevier. Adapted, with permission from ref. [19]

ule and to eliminate any air bubbles. Finally, the modules were placed under a metalhalide based solar simulator for 5 minutes to cure the adhesive from the UV present in the light. After UV curing, the final thickness of the encapsulated module was 200  $\mu$ m.

# 7.4.3 Photovoltaic properties and scalability

The modules were characterized under a solar simulator supplying 1 sun illumination (1000 W  $m^{-2}$ ; AM 1.5G). The light source was a sulfur plasma lamp with A class spectrum in the absorption range of the active material. Prior to characterization, the simulator was calibrated using a reference photodiode.



Figure 7-7 R2R switching set-up for lone modules (a); close-up of electrical contacting process on individual cells in a module (b-c). © Elsevier. Adapted, with permission from ref.[13]

Freshly fabricated module showed no or very poor photovoltaic functionality in agreement with similar observations noticed in the prototypes and in the test cells. By running a short pulse of high current density-high electric filed through the IOne cells in the modules revives functionality leading to a J-shaped IV curve. Doing so is hypothesized to involve a process of 'switching' (permanent change) of the electrical properties of PEDOT:PSS at the PEDOT:PSS/P3HT:PCBM interface by in-situ formation of a rectifying layer at this interface [12]. The activation of the test-cells can be easily accomplished manually with the use of a power supply; however, the activation of the serially integrated IOne modules is a tedious task as a roll of R2R processed solar cells carries several hundred serially-integrated modules depending on the design of the module, the web-width, and the length of the roll; and each module have many cell (up-to 16 in each modules in this study) where each cell requires activation. Manual functionalization of each module is a tedious task. As such, a custom built R2R switching set-up was put together in as part of another project as shown in Figure 7-7 [12]. The switching head comprised on an electrical contact pin array designed according to a specific module design and connects to the bus bars of the Ag back electrode. Proprietary software controls the whole switching procedure that includes contact testing, applying the individual switching pulse per single cell, resistance measure-



Figure 7-8: IV curves of ITO-free modules of three different sizes- large (176 cm<sup>2</sup>); medium (102 cm<sup>2</sup>) and small (31.1 cm<sup>2</sup>) (left). The corresponding IV parameters are listed in table x. The transmission profile of the front electrode (right).

ment or dark *IV* curve and further switching cycles, if necessary in case of insufficient switching. All steps are performed in parallel for all cells and take about 15 s for a 16-cell module. Therefore, the switching of 10 m roll carrying 130 IOne modules takes about 32 min. More information on the switching process can be found elsewhere [12,13].

With the use of the R2R switching machine, it is easy to acquire functional modules and to explore the robustness of the IOne process. Scalability is analysed by simply elongating the length of the strips/cells during processing. Three different sizes of the modules were fabricated: Small (under 100 cm<sup>2</sup>), Medium (100 cm<sup>2</sup>), and Large (over 100 cm<sup>2</sup>). The modules were randomly selected from the roll of switched modules and encapsulated as described in the section 7.4.2. Table 7-3 lists the physical characteristics of the modules and Table 7-4 the key photovoltaic parameters of randomly selected modules from the roll. The corresponding IV curve is shown in Figure 7-8.

As Table 7-4 indicates, the IOne process is highly scalable. Increasing the module area has no significant effect on the photovoltaic properties as it can be expected

Module	Total Area <sup>a</sup> (cm <sup>2</sup> )	Active area (cm <sup>2</sup> )	No. Of stripes/cells	Length (cm)	Width of a cell (cm)
Small	31.1	24.0	4	6	1
Medium	102.0	70.00	7	10	1
Large	175.5	121.5	9	13.5	1
Test cell <sup>b</sup>	-	6	1	-	1
Prototype <sup>c</sup>	-	1	1	-	1

Table 7-3: Physical aspects of the modules analysed to evaluate scalability.

<sup>a</sup>Total area does not included contact made with copper tape. <sup>b</sup> from section 7.3, R2R single cell. <sup>c</sup> From hapter 3, ASP structure.

ideally in serially-integrated module. All different sizes have PCE exceeding 1% on the total area and 1.5% on the active area. All parameters in the modules are similar to the R2R test cells except current density, which is slightly lower than the test cells. In a serially-integrated PSC module, the current of a module is an average of all cells/stripes and hence a weak performing single cell can undermine the overall current of the module. Furthermore, R2R processing of large-area solar cells renders higher variations in layer thicknesses and defects. This is much likely on the barrier substrate used in the upscaling in comparison to PET used in the R2R test cells. All these factors explain the lower current density in all the modules compared to the R2R test cells. Nonetheless, the largest module selected randomly demonstrates a loss of only 7% as compared to the best prototype supplied by an independent institution as described in Chapter 3. Furthermore, serially-integrated modules on ITOsubstrate (known as ProcessOne) having similar design parameters as used in the upscaling of IOne modules have resulted in a maximum PCE of 1.36-1.69% on active area >100 cm<sup>2</sup> [14]. With these results, one can conclude that DTU has developed a robust IOne process that is highly scalable and that is an efficient alternative to ITO.

Module	l <sub>sc</sub> (mA)	<sup>a</sup> J <sub>sc</sub> (mA cm <sup>-2</sup> )	V <sub>oc</sub> (V)	V <sub>oc</sub> of each cell (V)	FF (%)	Module PCE (%)	Active area PCE (%)
Small	29.6	5.73	2.106	0.53	53.59	1.07	1.39
Medium	53.85	5.48	3.709	0.53	54.27	1.06	1.55
Big	74.92	5.3	4.759	0.53	55.57	1.13	1.63
Test cell <sup>b</sup>		7.02		0.51	51.2		1.83
<b>Prototype</b> <sup>c</sup>		6.10		0.53	54.04		1.75

Table 7-4 Key photovoltaic parameters of ITO-free modules studied measured under 1000 W m<sup>-2</sup>: AM 1.5G

<sup>a</sup>Current density was estimated for each module by measuring the photocurrent of a masked stripe in each module and dividing by mask area  $J_{sc} = I_{sc}/Mask$  area; <sup>b</sup>from table 7-2; <sup>c</sup>ASP prototype data from Table 3-2 (Chapter3)

#### 7.4.4 Discussion

IOne process is a scalable technique. Unlike in the upscaling of the Fraunhofer-type and ProcessH, no unforeseen difficulties were encountered in the adoption of the R2R test cells to R2R large area modules. The only time-consuming step was in adapting the prototype to R2R compatible technique which was predominately finding the most suitable R2R technique in the processing of the Ag grids. The prototypes were based on inkjet printed grids on glass substrates. In the upscaling, the inkjet printing was found to be the least desirable technique owing to large defects when processed on flexible substrate as well as due to the low conductivity of the grids. In the prototype development, discrete control over the printing can be maintained. For example, the substrate in the prototypes was glass whose surface properties were meticulously changed using repeated cleaning steps and treatment in nitrogen plasma. Furthermore, the printing was carried out on heated substrate (30-40 °C) and the printed grids were sintered under high temperature often up-to 190 °C for 30 minutes. Such sintering conditions are not feasible on a flexible PET substrate with a working temperature of less than 150 °C. Furthermore, it is not possible to drastically change the substrate properties (for example, by cleaning or other surface treatment) and printing conditions (for example, changing heating of the substrate, changing the print direction) whilst an ongoing R2R processing which is fast (web-speed up-to 25 m min<sup>-1</sup> has been employed in the upscaling of IOne). It is therefore always necessary to conduct a preliminary test in order to determine the true R2R compatibility of a prototype and to identify changes and improvements that might be necessary and to note the effect on the photovoltaic properties once such changes are incorporated. Once the method of processing of grid was determined, the subsequent processing in the R2R test cells as well as large area module proceeded without difficulties except in the switching of the IOne modules. IOne modules were marked by high FF compared to ITO-based counterparts which made-up for the slightly lower optical transmittance of the Ag/grids: PEDOT:PSS transparent electrode as compared to ITO substrates. Further improvement rest in further tuning the design aspects and shading losses of the front electrode including PEDOT:PSS thickness and grid width and spacing while maintaining or improving the processing speed achieved in this study (up-to 25 m min<sup>-1</sup>).

#### 7.5 Stability of IOne modules

Stability of polymer solar cells marks one of the three primary facets that ought to be developed in tandem with other two–efficiency and low-cost processing— if the commercial vision for PSCs is to become a reality. In solar cells, stability has implications in terms of application, cost, and the environment. Once the efficiency target is met, IOne modules were extensively and intensively evaluated for stability under several rigorous accelerated and real-world operational and storage conditions following ISOS protocols [11]. Prior to the stability tests, the modules were encapsulated in a simple food packaging barrier (Amcor) having a UV filter (cut-off at 390 nm) and a barrier performance of 0.01 cm<sup>3</sup> m<sup>-2</sup> bar<sup>-1</sup> day<sup>-1</sup> with respect to oxygen (measured according to ASTM D 3985-81) and 0.04 g m<sup>-2</sup> day<sup>-1</sup> with respect to water vapor (measured according to ASTM F 372-78). This section reports on the results of the stability tests, presents a discussion of the observations, and attempts to inform what could to be improved.

#### 7.5.1 The stability test set-up

The modules were evaluated for stability under eight different tests. The test conditions are listed in Table 7-5. The modules were either placed under continuous exposure to light and continuously measured with an automated system (ISOS-L-2/-LL/-O) or periodically removed from their test systems and measured under calibrated sun simulator under 1 sun illumination (1000 W m<sup>-2</sup>; AM 1.5G) by recording three IV curves and taking the average values (ISOS-D-1/-D-2/-D-3/-L-3/-TC-3). The solar cell modules were stored in a drawer for ISOS-D-1 test. The high temperature storage tests (ISOS-D-2) were performed in an oven, while a climate-control chamber (Q-SUN Xenon Test Chamber from Q-LAB) was used for the damp heat tests (ISOS-D-2/-D-3/-L-3). A thermal cycling chamber (Thermotron) was used to perform ISOS-TC-3. For the outdoor test (ISOS-O), the modules were placed on a solar tracker and connected to an automated system for continuous IV recording (every 10 min). To perform ISOS-L-2 the modules were placed under a metal halide lamp based solar simulator (B class spectrum) with intensity close to 1 sun and the IV curves were automatically recorded every 10-15 minutes. Additionally, modules were placed under fluorescent light with intensities close to 0.2 sun for ISOS-LL. Prior to the initiation of the stability tests, all modules were characterized under a solar simulator with a sulphur plasma lamp supplying 1 sun illumination and having an A class spectrum in the absorption range of the P3HT. Then, they were distributed to their respective tests. At the end of the stability tests, the modules were measured again under 1 sun illumination.

Category	Light	Tempera-	Relative	T <sub>80</sub> (hrs)	Deviations from ISOS
	(Sun)	ture	Humidity		Protocols
		(°C)	(%)		
ISOS-D-1	0	25	20 – 35	1000-2800	-
ISOS-D-2	0	65	10 - 15	~ 5000	-
ISOS-D-3*	0	50	85	100 - 200	Lower storage- tempera- ture by 15 °C
ISOS-L-2	1	70	10 – 15	450-560	Testing was performed in room environment
ISOS-L-3	0.7	65	50	100 - 200	Modules were kept at open circuit
ISOS-LL	0.2	30	10 – 15	1800-1900	-
ISOS-TC-3	0	-40 to 85	55	520-650	-
ISOS-O**	0-1	10 – 25	20 - 100	1500-2000	-

Table 7-5 T80 of the modules for each type of ISOS tests conducted. The color gradation demonstrates the gradation in stress intensity with respect to temperature, relative humidity and radiation for each test.

\*Modules under D-3 demonstrated inconsistent behavior. While one module showed linear degradation, the other remained stable upto 500 hours followed by a catastrophic failure to PCE of 0%.

#### 7.5.2 Stability results

Figure 7-9 presents the stability graphs of the most stable modules in each ISOS test and the corresponding T80 values are given in Table 7-5 while Table 7-6 lists the key photovoltaic parameters before and after the stability tests measured under 1 sun illumination. In the calculation of T80, the first measurement is assumed to be T100 since burn-in duration and amount was not consistent in all the tests. It could possibly be due to the UV curing required in the encapsulation which inadvertently eliminates or alleviates the burn-in effect. Nonetheless, the maximum burn-in duration was observed to be 20 hours or less and the net impact on PCE was less usually than 10%. Hence, T100 is taken as the initial measurement and the reported T80 values in Table 7-5 is either directly noted from the measurements when T80 fell within the test period or it is deducted from linear extrapolation. At least two modules were monitored under each test and the range of T80 noted in Table 2 represents the variation ob-



Figure 7-9: Degradation trend the key photovoltaic parameters of IOne modules subjected to 8 different ISOS stability tests.

served. The variations in the T80 values are attributed mainly to defects and variability introduced by manual encapsulation such as the thickness of the adhesive layer. Such a defect might not alter the initial measurements but can severely undermine the stability of the modules over longer duration as discussed later on. As such, automated encapsulation is encouraged which was not available at the time of this experiments. However, now DTU has R2R encapsulation facilities described in Chapter 3 and reported in detail elsewhere [15].

Over the course of the stability study, the modules in all tests were performing above T80 at 1000 hours except under high humidity conditions of ISOS-D-3 and ISOS--3 and under constant 1 sun illumination (ISOS-L-2). The fast decline in performance in humid environment is an inherent failure of the encapsulation due to the diffusion of water molecules into the device, which affects all photovoltaic parameters. The degradation of the module performance under high humidity conditions is dictated by the highly hygroscopic nature of PEDOT:PSS which is known to swell and cause delamination [16]. Optical images of the modules after ISOS-D-3 and L-3 test show moisture



Figure 7-10 Bright field optical image of a module after ISOS-L-3 test showing moisture diffusion into the device (a). The defect-prone region of the module next to the button contact (b) where delamination occurs and results in increased rate of photodegradation as observed in (e) which shows high density and growing photooxidized regions (white spots) imaged under transmission mode. Bubbles in the module after high temperature ISOS-L-2 test (c) also leads to delamination and increased photo-oxidation as evident in (f). The white spots are not present in a freshly prepared modules or are comparatively and significantly smaller in size in the rest of the modules imaged after stability tests (d).

spots all across the modules penetrating from back electrode side into the device (Figure 7-10). This back electrode side is indeed the most susceptible route to entry of water molecules as the back electrode is in direct contact with adhesive holding the barrier. The adhesive is not water resistant. Water micro droplets are also observed to enter from scratches in the foil. Such obvious concentration of water molecules is not observed in any other tests.

The lifetime of the modules under ISOS-L-2 is limited by other mechanisms than those under high humidity conditions. Unlike under high humidity conditions, the modules in ISOS-L-2 have very stable  $V_{oc}$  and FF, and only  $J_{sc}$  seem to degrade which suggest photo-oxidation of the photoactive polymer. Three factors accelerate photooxidation of the active polymer under ISOS-L-2. Firstly, the light spectrum of the metal halide lamp has significantly higher UV content compared to real world conditions



Figure 7-11 LBIC images of a module showing defect emerges near button contact (a) and propagates over time (b). These modules are tested under outdoor conditions (ISOS-O). (a) is taken 1000 hours and (b) is taken at 3000 hours.

and is further accelerated by the temperature of 70 °C used in the test. Such a rigorous condition is unlikely to be met in real world indoor or outdoor operational conditions. Therefore, T80 of the modules determined for ISOS-L-2 is a very conservative estimate and the real lifetime of the module is expected to be significantly higher in real world operational conditions.

Secondly, a visible discoloration in the solar cell around the button contacts is observed which suggest moisture infiltration leading to delamination of the top PE-DOT:PSS and acceleration in photo-oxidation of adjacent cells to the contacts in the modules. Such a degradation of even one cell that is adjacent to the contacts not only decreases J<sub>sc</sub> of the module, but in severe cases can impede charge injection or extraction leading to inflection in the IV curve and ultimately undermining FF and V<sub>oc</sub>. Figure 7-11 shows an LBIC image of a module where such a localized degradation has occurred and is propagated over time. The oxidized regions of a module can also be evidenced with optical images also as these are marked by high density of photooxidized regions (discoloured or bleached spots) that are not present in the rest of the module or in a freshly prepared module (Figure 7-10). Such localized defects are a result of the variation in the adhesive thickness as well as lower barrier foil margins (edge-sealing) around the modules. Both of these can be avoided in future.

Thirdly, ISOS-L-2 modules had a unique visible defect that manifests as bubbles initiating from the silver interconnects/gap overlying area and leading into the back



Figure 7-12: (Left) ISOS-O Performance of an IOne module on a 45µm substrate placed on a tracker over a duration of ~1 year (20.06. 2012- 25.07.2013) in Roskilde, Denmark (left); the same module with larger edge-sealing margin (>1 cm). Current of the module on the *left* do not recover as sun starts shinning after winter, while the module on the *right* increases its PCE consistently with irradiance trend.

electrode side of the adjacent cell. The bubbles are observed in both modules under ISOS-L-2. Visible discoloration underneath and around the bubbles is also observed indicating enhanced photo oxidation of the photoactive polymer (Figure 7-10). Clearly, the bubbles are induced by merging of the remnant voids (oxygen and moisture entrapments or pockets) left behind during encapsulation, which is accelerated at high temperature due to lowering of the viscosity of the adhesive. The bubbles seem to cause delamination of the top PEDOT:PSS which is likely as PEDOT:PSS swells upon moisture adsorption and has a low adhesion strength with P3HT:PCBM [16,17]. All these bubbles lead to localized defects in the photoactive area contributing to decrease in  $J_{sc}$  of the module. Again, an operational temperature of 70 °C used in the ISOS-L-2 test is unlikely to be met in real world indoor or outdoor operational conditions and therefore this defect can be evaded.

The localized defects around contacts are a recurring issue and explain the lower end of the range of T80 values given in Table 7-5. The lifetime of the ISOS-O modules are also undermined by the defects around the contacts that lead to accelerated photo-degradation in the end cells leading to loss in  $J_{sc}$  and in severe cases causing loss of FF. On the other hand, generally  $V_{oc}$  and FF remain constant over a year as shown in Figure 7-12, *left*.

#### 7.5.3 Solutions to encapsulation defects

The first set of stability experiments highlighted the issue of localized defects in the end cell(s) of a module. These defects were an outcome of encapsulation flaws that include narrow edge sealing margins, the proximity of button contacts to the end cells in a module, and variation in the thickness of the adhesive layer as a result of manual encapsulation. The former two issues can be alleviated by simple measures that include extending the edge sealing margins and having the button contacts away from the end cells of a module. While altering the placement of button contacts requires redesigning the modules with elongated main busbar that will be incorporated in future R2R processing, the effect of increasing edge sealing margins can be readily studied.

Toward this end, a second batch of modules were encapsulated with a larger edge sealing margins (>1 cm) and tested under three tests ISOS-L-1, ISOS-D-1, and ISOS-O. The stability tests were performed at two different locations: at home (DTU, Denmark) and at an independent institution (ECN, Netherlands). All three tests were conducted in tandem at both the institutions. ISOS-L-1 is accelerated lifetime under a solar simulator (1000 W m<sup>-2</sup>; AM 1.5) at a temperature of 30-40 °C, in order to avoid the bubble formation as discussed in the previous section. ISOS-D-1 and ISOS-O are similar to that described in table 7-5. The tests were started in Oct 09, 2012 at both locations.



Figure 7-13 Comparative evaluation of IOne modules simultaneously tested at two different locations (ECN, the Netherlands and DTU, Denmark)

In both institutions, the modules in all the tests were found to be very stable and all modules at both institutions were performing at greater than their respective T80 values at 1000 hours. Under ISOS-L-1, all modules were operating above T80 value at 1000 hours which suggest an outdoor operational lifetime of a minimum of 1 year in northern and middle Europe which receive 1000-1200 hours of sunlight annually. The projection was indeed verified at DTU where the ISOS-O test were continued for over a year (~10,000 hours) and module's performance increases with time (Figure 7-12; *right*). Similar results were confirmed by ECN. ISOS-D-1 was also continued for a year at DTU and the modules were very stable. These stability results are compiled in a bar graph in Figure 7-13. Based on these results, it can be confirmed that IOne modules are stable under storage and outdoor operational conditions for a minimum of one year. The experiments are continuing and so far the modules are running steady under outdoor conditions.

Tests		Duration of	V <sub>oc</sub>	l <sub>sc</sub> (mA)	FF (%)	PCE on ac-
		test (nours)	(V)	(IIIA)	(70)	(%)
ISOS-D-1	Initial	1392	3.11	51.59	58.23	1.34
	Final		3.08	47.86	56.39	1.19
ISOS-D-2*	Initial	1560	2.00	33.01	52.33	1.20
	Final		1.91	33.94	49.55	1.15
ISOS-D-3	Initial	504	3.56	51.04	55.41	1.44
	Final		0.98	3.34	17.85	0.00
ISOS-L-2	Initial	1442	3.56	51.37	59.36	1.55
	Final		3.36	28.18	48.15	0.65
ISOS-L-3**	Initial	116	1.99	28.57	53.93	1.38
	Final		1.99	23.77	48.74	1.04
ISOS-LL	Initial	1582	3.53	51.85	52.43	1.35
	Final		3.42	46.76	48.48	1.11
ISOS-TC-3	Initial	385	3.55	50.52	61.29	1.57
	Final		3.46	57.25	47.72	1.36
ISOS-O	Initial		3.57	56.14	56.15	1.43
(Denmark)	Final-1	1554	3.4825	38.86	54.62	1.05

Table: 7-6: Initial and final photovoltaic parameters of ITO-free modules (active-area 70 cm<sup>2</sup> with 7 cells in each module) subjected to various ageing conditions as measured under 1000 W m<sup>-2</sup> (AM 1.5) solar irradiation at room temperature.

\*module area = 28.8 cm<sup>2</sup> with four cells/strips;\*\*module area = 22 cm<sup>2</sup> with four cells/strips

It is to be further noted that the food packaging barrier foil that we used here for IOne modules provide efficient encapsulation under most operational and storage conditions. The Achilles heel in the encapsulation is the exposed edges of the adhesive at the perimeter of the encapsulation. Since the adhesive which does not bear any barrier properties, often localized defects start propagating from the edges of the modules. Although extending the edge sealing margins may circumvent this issue to some extent, it is not altogether eliminated. New solutions ought to be found.

#### 7.6 Mechanical flexibility of IOne modules

IOne modules were further evaluated for mechanical flexibility. The transparent electrode in IOne comprising of substrate/flexographically printed Ag grids/hcPEDOT:PSS/ZnO, now termed as the Flextrode, is first tested for flexibility under bending test. An ITO on PET is also tested for reference. A makeshift set up was



Figure 7-14 A schematic illustration for the bending test set-up. The sample is mounted between two pinch grips, one of which can be displaced allowing control over bending radius and the number of cycles. During each bend cycle, resistance of the sample is measured by the multimeter at the cue from the contact once it is hit by the moving pinch grip during each bend cycle. The resistance measurement data then is recorded by a custom-built software.

put-together by incorporating our available adhesion test instrument (Mecmesin) and a Keithley sourcemeter. Samples were mounted in the adhesion test instrument between two pinch grips. The displacement and the number of cycles of the one of the pinch grips can be controlled by the software available with the adhesion test instrument. This feature can be used to bend samples at different radius by simply controlling the displacement of the top pinch grip. The samples could not be bent in a Ushape but had three bending radii as visible in Figure 7-14. Nonetheless, the set-up was sufficient for comparison purpose as ITO reference substrate was also tested under the exact conditions. Copper tapes were fixed at both ends of each sample to which crocodile clips were attached leading electrical connection into the Keithley sourcemeter. An external contact was placed on top of the starting position of the pinch grip such that when the top pinch grip returns to its starting position during each bending cycle, it briefly hits the contact. The resistance of the contact is monitored Using the second channel on the sourcemeter. As the contact is hit during each bend cycle, the resistance measurement of the sample is cued. The resistance measurement from the Keithley is then recorded in a custom built software (courtesy of a



Figure 7-15 (a-b) Mechanical flexibility of ITO-replacement used in the IOne modules -- the Flextrode (PET/Ag grid/PEDOT:PSS/ZnO). The bending radius is 7.5 mm. The flexibility or the lack thereof of ITO on PET sample is also shown for reference (c) which is due to the brittle nature of ITO causing cracks upon bending (d).

colleague, Morten V. Madsen). For simplicity, a schematic illustration of the set-up is shown in Figure 7-14.

The samples were bent in the forward and in the backward direction that determined the stress at the bending core as either tension or compression. The bending radius was 7.5 mm. The resistance of the Flextrode sample remained unchanged over the course of 10,000 bend cycles. On the other hand, the resistance of ITO on PET increased by an order of magnitude within 100 bending cycles. Optical images showed cracks emerging in ITO from the core of the bend and propagating toward the ends with increasing bending cycles (Figure 7-15). Clearly, ITO on PET is not feasible for flexible applications while the Flextrode substrate is mechanically and electrically robust.



Figure 7-16 Effect of bending on the photovoltaic properties of IOne modules. Bending in compression at a bending radius of 2.3 cm (left). A highly flexible unencapsulated IOne module (substrate thickness of 45  $\mu$ m) in which the front transparent electrode side (honeycomb) and the back electrode side (the screen printed silver grid lines and interconnections silver) can be differentiated.

The next step was in the evaluation of IOne modules was to determine if the photovoltaic properties changes upon bending. A 7-stripe module was bent at a bending radius for 2.3 cm for 1200 cycles. The stress at the core of the bend in the so-lar cell stack was compression. The modules were measured under a calibrated 1 sun illumination (1000 W m<sup>-2</sup>, AM 1.5G) intermittently by pausing the bending test. Before each measurement, the modules were kept under the solar simulator for 2-3 minutes to equilibrate. No degradation in performance was observed (Figure 7-16). This is an on-going experiment and the modules will be evaluated under bending in compression and tension from two different directions (i.e. bending core will be either parallel to the stripes or perpendicular to the stripes).

#### 7.7 Demonstrator application

Previously, the ITO-based upscaled architecture—ProcessOne--- has been the first truly scalable fully R2R processed technology that has been developed in demonstrator applications (Ref) and it is also commercially available from Mekoprint A/S, Denmark.



Figure 7-17. The schematic diagram of the electronic circuit of the demonstrator with Zener diode (Z) to prevent overcharging of the lithium polymer battery (Batt.); blocking diode (D) prevents discharge of the battery through the polymer solar cell (PV). ON/OFF (SW) switch to the laser diode and a printed resistor (R) is placed to avoid overloading the laser diode. The actual printed circuitry (middle) and the finish laser power lamp are also shown (right). The circuit designs are © RSC Publishing. Adapted, with permission from ref. [25]

ITO-free upscaled process, IOne, represent a huge leap forward in comparison to ProcessOne in that it is not only ITO-free but it also employs an all-solution processing of all layers including the electrodes using facile and fast coating methods. Credit-card size laser power pointers (250 units) were developed as a consumer electronics demonstration. The demonstrator was powered by a variant of IOne modules in which the front Ag grid was inkjet printed with conductivity improved by the use of flash sintering. The solar cell modules comprised of 16 serially integrated cells with a total area of 35.5 cm<sup>2</sup>. The width of bottom transparent electrodes was 3 mm and a gap width of 1 mm. A PCE of 1.7% on active area was accomplished when characterized under 1 sun conditions (1000W m<sup>-2</sup>; AM 1.5). The modules were integrated in all printed circuitry enabling direct charging of the lithium polymer batteries to power a laser diode. The operating voltage of the laser diode was 3V and an operating current of 10 mA. The circuit and the final product is shown in Figure 7-17. Detail description of the production process, module integration into product, cost and life-cycle analysis can be found elsewhere [18-20]. In all, the IOne modules were not the cost-driving factor in the demonstrator. The estimated cost of each IOne module was 0.25 € which represented a very low share (2 %) of the total cost of the demonstrator.

# 7.8 Summary

Detail summary is given under photovoltaic and stability separately. In all, One modules is now a readily scalable ITO-free technique that is processed in an all ambient environment using only R2R printing and coating techniques. A PCE of 1.5 -2% on active area and >1% on >100  $\text{cm}^2$  of total module area is achieved, thus fulfilling the practical targets of this PhD study. The modules were further assessed for stability using ISOS protocols. IOne modules are stable in most test conditions except where high humidity and/or high temperatures were involved which highlight the need to develop encapsulation methods. Improvement in encapsulation would significantly prolong the lifetime, particularly from the edge sealing and contacting need immediate attention . As of now, with a simple food package barrier, the modules have withstood one year of harsh northern European climate (rain, snow, winter, very less sun) while still operating above 90% of its initial performance. However, the encapsulation procedure has to be made more robust to increase reproducibility. All modules were manually encapsulated that lead to variations in stability owing to the adhesive thickness. Automated encapsulation with very thin outlines of adhesive is encouraged. A small maneuver by increasing the edge sealing margins shows a marked improvement in the stability. The modules are further integrated in demonstrator application powering laser points.

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Chapter 8 - 7BA comparative evaluation of the ITO-free upscaled devices based on life-cycle analyses

# 8. A comparative evaluation of the ITO-free upscaled devices based on life-cycle analyses

# 8.1 Introduction

The primary motivation in the development of photovoltaics is the production of clean energy. Polymer solar cells (PSCs) aim to achieve this goal while achieving costcompetitiveness against conventional energy sources. A life cycle assessment (LCA) can allow a priori evaluation of the environmental impacts of an emerging technology and therefore can enable identification of the scope for environmental improvement of the technology [1]. Furthermore, an LCA can also point toward the economic feasibility of an energy technology. In our development of ITO-free PSC concepts, LCA has been carried out after the upscaling of each ITO-free PSC concept. The LCA results, which has primarily been evaluated by a colleague Nieves Espinosa, have proven to be an effective tool in guiding our research and development on upscaling of the ITOfree concepts toward our greater objective of environmentally and commercially viable PSCs. The feedback provided by LCA effectively allows identification of arenas for improvements in our upscaling processes for cost-effective clean energy production. This chapter presents a comparative analysis on the environmental feasibility of three different upscaled ITO-free PSC architectures as described in Chapter 5-7 while identifying areas for improvement in clean energy production. Additionally, this chapter aims to present a comparison of the upscaled ITO-free architectures against an upscaled ITO-based process as well as of PSCs in general as a technology against other photovoltaic technologies.

# 8.2 A brief background on Life Cycle Analysis (LCA)

An LCA, also referred as cradle-to-grave analysis, is a tool for objectively assessing the environmental aspects and potential impacts associated with a product [2] over its entire lifecycle which involves raw materials acquisition, their transport, manufacturing, product transport, use and maintenance of the product, and final decommission

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and/or recycling while identifying and quantifying relevant environmental impact at each stage [1]. LCA is a ISO standardized methodology for evaluation of environmental impact which involves four stages--a) Goal and scope definition; b) Inventory analysis; c) Impact assessment; and d) Interpretation of the data. LCA of a clean energy system starts with an explicit statement of the aim of the study, which sets the context and provides a description of the product system. A functional unit is defined which provide a reference to which the inputs and outputs of the system are related. Then, LCA requires setting up a data inventory on the inflows and outflows of energy, materials, and greenhouse gases associated during an entire lifetime of a system and as relevant to the defined goal and scope of the LCA; and evaluating the feasibility of 'clean energy potential' based on the energy and greenhouse gases offset against conventional primary energy means achieved by the use of the particular clean energy system. Commercial software allows compilation and reporting of the data, as well as contains database of emission of greenhouse gases and energy input in various chemicals and processes.

The inventory analysis is very critical as its reliability impacts the final assessment. It includes: 1) a painstaking construction of raw material inventory and finding out the energy and pollutants associated with each raw-material that is used as an input material in the production of a particular product and 2) figuring out the associated energy and pollutants that are further invested in the production into a final product (direct process energy) and the use of a product throughout its lifetime. While a lot of this information on various materials and processes is available in databases, some need to be constructed.

The lack of real data on the processing of PSCs due to the technology being nascent has until recently prohibited a comprehensive LCA on PSCs. The ones that have delved on it have been rather limited in their scope: for example, only specific materials [3] or laboratory solar cells prepared by spin-coating and evaporation are assessed Chapter 8 - 7BA comparative evaluation of the ITO-free upscaled devices based on life-cycle analyses

[4]. At this point, no other academic institution employs a complete R2R processing of PSCs. The upscaling of ITO-free architectures has been carried out our pilot R2R plant at DTU which allows us first-hand access to factual data on the materials and processing parameters that have been employed in the R2R production of PSCs. Hence, the LCA based on our upscaling initiative is a good starting point to get an idea of the environmental feasibility of the PSCs as a technology in general and of our specific PSC architectures and processes in particular. Many argue that due to the pilot nature of our R2R production facilities for academic purposes, the LCA results do not reflect the true environmental impact of PSCs as a technology. We acknowledge that economies-of-scale in a true industrial production will definitely improve the environmental impact of the PSC technology in general. Nonetheless, our LCA results can be regarded a conservative scenario on a semi-industrial production scale, which nonetheless is based on factual data— a choice we prefer over speculation without demonstration.

#### 8.3 Methodology

Life cycle analyses of all the three architectures up-scaled in chapter 5 have been carried out and reported: Fraunhofer-type in ref. [5]; ProcessH in ref. [6] and IOne in ref. [7]. Furthermore, LCA of the upscaled ITO-based PSCs, known as the ProcessOne, had been reported by our group previously [8]. Herein, a compact summary all these LCA results are presented with a primary focus on ITO-free alternatives. ProcessOne is used as a benchmark against which the ITO-free architectures have been evaluated. For complete information on the methodology and inventory of each LCA analysis, please refer to the relevant publications. All processes have been developed at DTU. The system boundary considered in all the LCA studies, as schematically shown in Figure 6-1, incorporate direct energy used in the production of raw materials and in the manufacturing of the PSC modules. The energy used for manufacturing of the roll-toroll machinery, transportation, maintenance, and decommissioning and/ or recycling is not considered.
In the LCA studies, the inventory analysis is based on data acquired *in situ* from materials consumption and equipment specification that are actually employed in their production at DTU. Data on raw material and the relevant upstream processes are collected from the database Ecoinvent 2.0-2.2 – an integrated database with commercial LCA software, SimaPro. Unavailable data in Ecoinvent are compiled from relevant literature or other databases. The functional unit for solar cells is always defined as 1 m<sup>2</sup> of processed area. This a standard unit used in other photovoltaic technologies as well. Due to spatial limitations of processing methods and the solar cell module designs, the ratio of active area ratio is generally much lower to the web area is (45-70%). In in this chapter, the results presented are based on asincurred materials, module design, and processing parameters used in the upscaling of each of the architectures as detailed in Chapter 5-7<sup>1</sup>.

Two different forms of energy are employed in the production of PSC modules: thermal energy (for example, for drying and annealing process) and electrical energy (for running the machines, or flash sintering, *etc*). In order to holistically evaluate the energy-costs and energy-savings of an energy technology, one common unit of energy ought to be defined that can be compared with conventional energy means. Hence, thermal and electrical budgets were converted to a single unit, the equivalent primary energy (EPE) expressed in mega Joules (MJ). The conversion is dependent on the time and the energy mix of the country. Here, conversion factors 0.37 and 0.80 were used in the conversion of electricity and heat respectively into EPE. The factors are based on the Danish energy mix as of 2008. Lastly, the interpretation of results requires knowledge on the following terminologies [5,10]:

<sup>&</sup>lt;sup>1</sup> For this chapter, I have compiled the data from our original LCA studies publications [[5,6,8,9] or consulted the LCA concerned individual in our group for information on the IOne process [7].



Figure 8-1 Life-cycle events of a polymer solar cell. The dashed line is the system boundary considered in the LCA studies of the different architectures of PSC. © 2013 Elsevier. Adapted, with permission from ref. [5].

- Cumulative Energy Demand (CED): Total energy consumed in the production of 1 functional unit of PSC modules. It is a summation of <u>embodied energy in the raw</u> <u>materials</u> and <u>direct process energy</u>. It is expressed in mega joules (MJ).
- Energy Payback Time (EPBT): It is the ratio of CED to annual energy output. The result gives the number of years it takes for the energy technology to pay back the energy spent on its production, installation, use and maintenance, and recycle and/or decommission.

$$EPBT = \frac{E_{EMB}}{E_{GEN}}$$

• Energy Return Factor (ERF): The ratio of energy produced over the entire module lifetime (L) to the embedded energy. It is a ratio of the lifetime of the energy technology to EPBT.

$$ERF = \frac{E_{GEN}}{E_{EMB}}L = \frac{L}{EPBT}$$

Greenhouse gas emissions (GHG): All climate relevant emissions during the life cycle expressed as CO<sub>2</sub>-equivalents. The values can be derived from the embedded energy by multiplication with an emission factor (46.5g CO<sub>2</sub>-eq/MJ= 530g CO<sub>2</sub>-eq/kWh for an average EU electricity mix). For expressing climate relevant emissions other than CO<sub>2</sub> as "CO<sub>2</sub> equivalents" weighting factors relative to CO<sub>2</sub> are applied, e.g., N<sub>2</sub>O = 298, SF<sub>6</sub> = 22.800 [10].

#### 8.4 LCA results

All the PSCs architectures used in this study can be represented comprising of the functional layers as schematically shown in Figure 8-2. The difference among the architectures is one of the electrodes, represented as Electrode 1. The actual schematic



Figure 8-2 The general structure of the all upscaled solar cells architectures. ZnO is not present in the Fraunhofer-type while PET+adhesive excluded in IOne and ProcessH that were processed directly on barrier PET foil.

illustration of the architectures along with information on layer thicknesses and design can be found in the respective upscaling chapters (Chapter 5-7).

# 8.4.1 Cumulative Energy Demand

The three up-scaled ITO-free processes— Fraunhofer-type, ProcessH, and IOne—are evaluated against upscaled ITO-based process, ProcessOne. Each of the upscaling processes is analyzed for embodied energy in the raw materials and direct process energy incurred in each functional layer in the respective PSC stack. The embodied energy in the raw materials of each functional layer is constructed by a summation of the embodied energy in their respective constituent materials while the direct process energy is derived by summation of energy invested in all the processing steps incurred in the preparation of each layer. The raw material constituents of each layer and the processing steps used each layer is as follows:

## 1. Input materials breakdown

- Substrate: PET
- Electrode 1
  - ProcessOne: ITO on PET
  - Fraunhofer-type: Al target, Al production, Cr target, Chromium production, Argon production
  - ProcessH: non-particle based Ag; 1-butanol
  - IOne: Ag grid (PEDOT:PSS planarization layer is considered with hole-transport PEDOT:PSS layer)
- Electron transport layer: ZnO (It is not used in Fraunhofer-type)
  - Zn(OAc)<sub>2</sub>
  - КОН
  - MeOH
  - Acetone
  - MEA
- Photoactive layer
  - P3HT
  - PCBM

- Cholorobenzene
- Hole transport layer
  - PEDOT:PSS
  - Isopropanol
- Electrode 2
  - Ag (screen printable ink)
- Encapsulation
  - Barrier foil (PET)
  - Adhesives

## 2. Processing breakdown

- Electrode 1
  - ProcessOne:
    - Only patterning is considered which comprise of:
      - o Screen printing of etch resist
      - o UV curing
      - o Etching
  - Fraunhofer type
    - Sputtering of Al/Cr
  - ProcessH:
- o Slot-die coating of Ag non-particles
- o Drying
- IOne:
- o Flexographic printing of Ag grid
- o Drying
- o Rotary screen printing of hcPEDOT:PSS
- o Drying
- 0
- Electron transport layer: ZnO (not used in Fraunhofer-type)
  - o Ink preparation
  - Slot-die coating
  - o Drying
- Photoactive layer: P3HT:PCBM
  - o Ink preparation
  - Slot-die coating
  - o Drying

- Hole transport layer: PEDOT:PSS
  - Rotary screen printing in IOne process; slot-die coating in the rest.
  - o Drying
- Electrode 2: Ag PV410
- Rotary screen printing in IOne processing; Flatbed in the rest.
- o Drying
- Encapsulation
  - Encapsulation by R2R lamination

The embodied energy of the raw materials and other upstream processing that constitute each functional layer in the PSC stack can be located in the publications. For example, the individual energy footprint of P3HT, PCBM, and cholorobenzene –the three of which altogether constitute the raw materials for the photoactive functional layer –can be found. Similarly, the processing is categorized according to processing of each functional layer. Further breakdown of energy invested in processing including upstream processes as well as equipment specifications can be located in the publications.

The cumulative energy demand per functional unit (1 m<sup>2</sup>) of each ITO-free architecture is shown in Figure 8-3 in which the share of embodied energy in the raw materials and direct process energy can be also distinguished. At first glance, IOne



Figure 8-3 A comparison of total embedded energy in the production of a functional unit (1 m<sup>2</sup>) of PSCs based on three different ITO-free processes (ProcessH, Fraunhofer-type, and IOne). ITO-based upscaled (ProcessOne) is also shown as a benchmark. The contribution of raw materials and direct process energy incurred in each architecture can be distinguished.

and ProcessH are significantly better than either ProcessOne or Fraunhofer-type and represent ten times lower net embedded energy than either ProcessOne or Fraunhofer-type. The embedded energy in ProcessOne is primarily driven by ITO on PET which constitutes >70% of the net embedded energy. Raw materials constitute more than

three-fourths of the CED in ProcessOne of which ITO accounts for 88% share of the embodied energy in the raw materials. ITO on PET is considered as an input material while only patterning of ITO is carried out at DTU which constitutes the numbers allocated for processing of ITO (Figure 8-4).

The Fraunhofer-type possesses the highest CED of all the architectures including the ProcessOne. The direct process energy of Fraunhofer-type represents two-third of the net embodied energy, of which 80% is imposed by the processing of Al/Cr (Electrode 1). The processing of Al/Cr incurs such a high energy footprint due to its sputtering requirement. Magnetron sputtering is an energy-intensive processing method which is based on instrumentation that operates at very high voltages (248 MJ EPE in our processing) and high vacuum (88.53 MJ EPE in our processing) as well as



Figure 8-4 The share of each functional layer in the Input materials (top row) and the direct process energy (bottom row) is given for the four different upscaled PSCs architectures.

the throughput is very low owing to low web-speed (1 cm min<sup>-1</sup>). Furthermore, Al/Cr also represents 60% of the net share of embodied energy in the raw materials of which 99% is levied by Argon gas which is used in the sputtering. In total, Al/Cr electrode represents 78% of the net embedded energy in the Fraunhofer-type. Both Pro-

cessH and IOne represent low CED and have a more balanced distribution between and within the direct process energy and the embodied energy in the raw materials (Figure 8-4). The transparent electrode in ProcessH, a semi-transparent silver film based on a customized Ag ink, shares only 7% of the CED; the raw material contribution of the transparent electrode is only 1%. The transparent electrode of IOne (Ag grid and PEDOT:PSS) represents a slightly higher energy footprint than ProcessH with a share of 11% in the CED. Nonetheless, the electrodes are not the primary determinants of the net embedded energy in either IOne or ProcessH. The pie-charts reveal that IOne and ProcessH can be further improved by addressing PEDOT:PSS whose drying requirement bears the largest share in the energy incurred in processing (due to its high thickness) as well as PET marks the biggest share in the embodied energy in the raw materials of all ITO-free architectures. We have been investigating the latter by employing barrier film directly as the substrate which leads us to forgo a separate PET layer completely. Nonetheless, this is presented with some challenges (shrinkages, surface properties, etc.) which are constantly being solved. Finally, replacing silver, which marks a similar abundance issue as ITO, has to be resolved. Toward this end, graphite and carbon-paste have been explored in our experiments [9].

The situation discussed thus far is based on as-upscaled processes as described in Chapter 5-7. The active area percentage per functional unit therefore was different for each architecture: ProcessOne (67%); ProcessH (45%), Fraunhofer-type (67%) and IOne (50%). Furthermore, the different architectures have been investigated over the course of the past three years and the latest one, the IOne, represents several advancements in the processing. For a fair comparison, we can assume that the common layers in all the architectures-- the electron transport layer (ZnO), the hole-transport layer (PEDOT:PSS), the screen printed silver layer, the substrate, and the encapsulation method--are similar to Ione in all the different architectures. The active layer thickness is optimized in each architecture and it is not assumed to be the same. Furthermore, a constant active area of 67% can be assumed as used in the pro-





Figure 8-5 A comparison of CED in the different upscaled PSC processes between asincurred and with feasbile assumptions. As-incurred is based on as-employed materials and processing in the upscaling experiments. Active area ratio of ProcessOne and Fraunhofer type was 67% while ProcessH and IOne had an active area of 45% and 50%, respectively. The different architectures were upscaled in different point of time and therefore the feasible assumptions simply assume our latest advancement in processing of ZnO, PEDOT:PSS, screen printing of Ag, substrate, and encapsulation and a common active area ratio of 67% in all architectures. The feasible assumptions do not make a profound impact on ProcessOne and Fraunhofer-type which remains the least desirable architectures for further development.

cessing of ITO-based benchmark, the ProcessOne. These feasible assumptions, nonetheless, mark only minute improvement in the CED of ProcessOne and Fraunhofertype while IOne is emerges as the cleanest process of all, closely followed by ProcessH (Figure 8-5).

#### 8.4.2 Energy payback time (EPBT)

The energy payback time is the time required for a PSC system (or any other photovoltaic system) to generate the same amount of energy as is incurred during all stages of its lifetime. In order to calculate the energy produced by a PSC system, few assumptions are made. Firstly, the annual isolation level used in the calculation of the energy produced by the PSC system is set as 1700 KWh m<sup>-2</sup>, typical of European southern countries and representative of the world average [8]. Based on ex-

perience of the performance of the solar cells based on the different architectures, a PCE of 1-2% with the P3HT:PCBM-based active layer is assumed and is realistic. While ProcessOne and IOne have readily shown these power conversion efficiencies in our experiments as described in Chapter 5 and ref. [11] respectively, the ProcessH and the Fraunhofer-type have shown that 1% is realistic and therefore is a feasible assumption for these architectures. Finally, the photovoltaic systems do not operate at all full capacity throughout the year. Therefore, a performance ratio of 0.75 is assumed [10]. Finally, the calculation of EPBT assumes that 1 kWh of annual electricity output of a solar module avoids the generation of 1 kWh conventional electricity and is therefore equivalent to 11.4 MJ primary energy (which is an averaged primary energy value required for the production of 1 kWh conventional electricity)[10].

The EPBT of the different architectures is given in Figure 8-6 and is listed in Table 8-1. For a PCE of 1-2%, the Fraunhofer-type requires an EPBT of 3-1.5 years, closely followed by ProcessOne. Hence, these processes are only feasible over the ProcessH and IOne if 1) they demonstrate comparatively and significantly longer lifetime than the other architectures; and/or 2) their PCEs can be significantly improved. The former is unlikely as it can be inferred from the stability studies on the prototypes (Chapter 4) in which ProcessH emerged as the architecture with highest stability and both ProcessOne and Fraunhofer-type do not necessarily possess significantly higher stability the other two architectures; the latter could be accomplished with the use of new low-band gap polymer that deliver higher PCE. Nonetheless, the latter case will have proportionately similar impact on any of the other architectures and therefore further development of ProcessOne or Fraunhofer-type is not uniquely demanded for PSCs. In the laboratory devices, P3HT:PCBM shows an average PCE 3% as revealed by data collected from all scientific publications [12]. The laboratory devices are based on very small area, often less than 1 cm<sup>2</sup>, and are most often processed with a combination of spin-coating (seldom in ambient conditions) and evaporation of the back electrodes. Furthermore, they almost exclusively employ ITO as the transparent con-

ductor which allows achieving of high short circuit current 10-12 mA cm<sup>-2</sup> in a P3HT:PCBM system. When upscaling, however, ohmic losses set-in due to the high sheet resistance of ITO, layer thicknesses are not as homogenous as spin-coated layers, and processing is mostly carried out in ambient conditions. Furthermore, the loss of active area in upscaling which can amount to 50% implies that a PCE of 1.5% on a functional unit is the most expected of a P3HT:PCBM-based PSC system. Considering these boundary conditions, IOne appears to be most environmental-feasible process that is operating at its highest capacity as it has already demonstrated a PCE of close to 1.5% for active area coverage of 50% per functional unit. Furthermore, the initial assessments of the stability of IOne modules have already demonstrated an operational lifetime of a minimum of 1 year in outdoor conditions (Chapter 7). Given the EPBT of IOne is 2.3 months, the process as it stands right now is also environmentally and cost favorable to ITO-based ProcessOne. Answering how feasible is IOne requires

	PCE/ Architecture	ProcessOne	Fraunhofer- type	ProcessH	IOne
	1%	2.53	3.24	0.31	0.29
As-incurred	2%	1.26	1.62	0.15	0.15
	5%	0.51	0.65	0.06	0.06
	10%	0.25	0.32	0.03	0.03
	1%	2.24	2.91	0.42	0.39
With feasible assumptions**	2%	1.12	1.46	0.21	0.19
	5%	0.45	0.58	0.08	0.08
	10%	0.22	0.29	0.04	0.04

 Table 8-1: Energy Payback Time (EPBT) of different architecture with currently achieved power conversion

 efficiency of 1-2%, and future projections of a PCE of 5-10% that assuming no further development in the

 architecture and PCE achievable only by novel polymers having energy footprint similar to P3HT:PCBM

evaluation of the energy return factor (ERF). At this juncture, however, only inference can be made as the true lifetime of the modules is still under characterization (next section).

## 8.4.3 Comparison with photovoltaic technology

Today, a plethora of photovoltaic (PV) technologies are present, some are commercially available while others are under development. Despite the more mature PV technologies that have high power conversion efficiencies (reaching 25%) and higher stability (reaching 25 years), they have been unable to compete with conventional energy means in the last >50 years of their development. The reason is their exorbitant materials and processing costs as discussed in the introduction (Chapter 1). Over the course of development of PV technologies, PSCs have emerged in the last two decades as a means to overcome the bottleneck that the more mature PV technologies have experienced in terms of further cost reduction in materials and processing (the dumping of solar cells from China in the year 2011-2012 is considered an anomaly as these cells are highly subsidized, thus misrepresenting the true cost [13] and are widely reported to be highly defective rarely operating at their given specification [14]). PSCs represents a breakthrough in the photovoltaic technology in terms of its potentially cost-competitive energy generation to conventional energy means owing to its low-cost raw materials and manufacturing requirements and unprecedented in the PV sector, albeit at a cost to efficiency and stability. Nonetheless, a goal of 10-10 (that is, 10% efficiency with 10 years of lifetime) for PSCs has been suggested to be comparatively advantageous, both commercially and environmentally, than the 25-25 goal threshold shown by inorganic first generation solar cells.



Figure 8-6 The chart compares the EPBT of the different upscaled PSC processes and shows projections when PCEs can be improved within the boundary of current raw materials and processing parameters. The chart is based on feasible assumptions as shown in Table 8-1

Figure 8-7 shows the EPBT time of some established PV technologies in comparison to ProcessOne and IOne. One thing to keep in mind while evaluating the EPBT of various technologies is that the first generation solar cells have reached their peak efficiencies. But for a marginal improvement, the PCE and lifetime of these technologies is unlikely to show significant improvement as they are operating close to their theoretical limit (the third generation of inorganic solar cells as shown in Chapter 1 (Figure 1-6) are too nascent to be considered at this point). The second generation thin films PV such as CIS and CdTe have similar EPBT as the first generation and therefore have not necessarily attained a significant cost-competitiveness against the first generation Si solar cells. With increasing efficiency and advancement in processing, however, the EPBT of the second generation PVs is decreasing. In its current form, the third generation represent here by ITO-free PSCs (IOne) already demonstrate significantly lower EPBT by a factor of 10 compared to any of the other technologies. Unlike other technologies, PSCs have a large potential to have higher efficiency resting on the development of novel low band-gap polymers. Low band-gap polymers have been reported to give efficiency exceeding 10% in laboratory devices but are thus far not available commercially or in significant quantities to be used in

upscaling experiments. Nonetheless, it is only a matter of time that low-band gap polymers will become widely available. Just by increasing the efficiency to 5% assuming no further development in processing and cost-reduction in raw materials, PSCs can have an EPBT of less than 1 month using IOne architecture.

EPBT is a common indicator for 'greenness' of the product as EPBT reflects the energy invested in the product. The energy invested is supplied by fossil fuels which in-turn is the prime determinant of greenhouse gases. However, EPBT does not take into account the energy savings during the rest of the lifetime of the technology and therefore cannot assess the magnitude of 'greenness.' ERF is a more suitable indicator for this purpose as it takes into account the operational lifetime of the technology. Considering a first or second generation solar cell with an average of 2 years of EPBT and 20 years of lifetime, an ERF of 10 is achieved. The current IOne PSCs with a lifetime of 2 years (based on our lifetime assessment) and an EPBT of 0.19 year (2.33 months) results in an ERF of 10.52. From this perspective, PSCs are already competitive with mature photovoltaic technologies in terms of 'greenness.' In terms of greenhouse gases, the early assessment suggest these PSC processes generate 14-23 kg CO<sub>2</sub>-eq/m<sup>2</sup> (~350-580g CO<sub>2</sub>-eq/W<sub>p</sub>) which compares rather favorably to other established technologies that typically generate 35-80 kg CO<sub>2</sub>-eq/m<sup>2</sup> (~350-800g CO<sub>2</sub>eq./W<sub>p</sub>) [10].



Figure 8-7 The Energy Payback time of various photovoltaic technologies of three different generations are compared. The data is located from ref. [12]. In its current state, PSC IOne process represents the lowest EPBT of merely 0.23 years (2.7 months).

In terms of cost, Azzorpardi et. al have conducted a comprehensive economic assessment on the energy production based on ProcessOne modules in a domestic setting and have shown that with a 7% efficiency and a 5 year of lifetime will enable a levelized cost of electricity (LCOE) between 0.19 €/kWh and 0.50 €/kWh for a 1kWp system which is competitive with silicon solar cells [15]. The raw materials cost of ITO is shown to be the main determinant of the cost of a household PSC-based photovoltaic system incurring 40% of the total system cost. Although the economic assessment based on IOne is pending, nonetheless it can extrapolated assuming ITOfree electrodes incurs 8 times less cost than ITO electrodes (a factor derived from embedded energy ratio), that the new ITO-free PSCs will deliver the same LCOE with an efficiency of 5% and a lifetime of 3 years which is indeed realistic the very near future. Emmott et al. have shown the implications of replacing ITO with several ITO-free alternatives and concluded that silver nanowires and hcPEDOT:PSS can reduce electricity cost per watt peak by up-to 20% and EPBT by 30% respectively [16]. Our results show that higher margins with PEDOT:PSS/grid is achievable because of high processing speed and improvement properties compared a to standalone hcPEDOT:PSS transparent conductors.

# 8.5 Summary

The initial comprehensive LCA of the three different upscaled ITO-free architectures reveal that the IOne is the clear winner demonstrating a PCE exceeding 1% on total area and 1.5-2% on active area for a P3HT:PCBM based system, and therefore embodying a corresponding EPBT of 2 months and an ERF equaling to established PV technologies. Furthermore, the breakdown of raw-materials and processing incurred in each layer in each of the architectures reveal that further environmental (and cost) improvements are possible by:

- 1. Increasing the active area ratio. In the ITO-based ProcessOne, a serialintegrated module design is an absolute requisite owing to the limited conductivity of the ITO. However, a monolithic design is a more cost favorable design as the active area ratio can reach above 90%. Monolithic module design may be possible with the new ITO-free architectures as the front-electrodes can reach very high conductivity (sheet resistance of  $1 \Omega \Box^{-1}$ ) in comparison to ITO on PET (60  $\Omega \Box^{-1}$ ). This is a subject of current investigation.
- 2. Reducing the layer thicknesses which imply energy-savings on raw materials and on processing. Particularly, the embodied energy in the raw materials is predominantly dictated by PET and the adhesives for encapsulation in IOne. Reducing their thicknesses can bestow large cost-savings. It is therefore that we have been investigating barrier films directly as substrate while also serving as encapsulation. In the processing, currently drying time incurs 90% of the direct process cost. The hole-transport layer PEDOT:PSS has the highest thickness which requires longer drying time and therefore represents the majority share of energy embedded in processing.

- 3. Avoiding silver. Not only does silver represents a large share of embedded energy in raw materials and processing, but also it has similar abundance as ITO. One can therefore argue that if we have an indium problem, we have a silver problem. In the long term, metal-free PSCs will be more feasible. Toward this end, carbon paste and graphite or other organic materials are being investigated.
- 4. Water-based processes. Water is most environmental-friendly and the least expensive solvent.
- 5. Improving stability toward the 10 year lifetime goal. In the calculation of ERF presented in this chapter, a two year lifetime is used based on our ongoing stability experiment thus far but a 5 year efficiency in the short run and a 10 year efficiency in the long run is expected of PSC technology. This will pave a long way in furthering the competitiveness of PSCs not only against its PV counterparts but also against conventional energy means.'
- 6. Last but not the least, the torchbearer of PSC are the chemical engineers whose ingenuity and success in tailoring stable low-band gap polymers will results in breakthroughs in the PSCs.

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# 9. Conclusion and Outlook

This PhD thesis reports a leap forward in the realization of ITO-free PSCs that can directly be adopted to power niche applications. Based on a rigorous evaluation of several prototypes, upscaling of three was carried out. One of the upscaled architectures, IOne, demonstrated photovoltaic performance comparable to a previously reported ITO-based R2R processed module, ProcessOne. With the current performance and stability achievements with IOne, it is clear that ITO-free IOne modules are already positioned for niche applications. IOne modules displayed >1 % efficiency on a total area of >100 cm<sup>2</sup> similar to those reported for ProcessOne modules. Furthermore, IOne shows >10,000 hours of lifetime under operational and storage conditions. It has an energy payback time of less than 3 months and has a similar energy return factor as conventional inorganic solar cells. PSCs in general and IOne in particular are unprecedented in 'greenness' in terms of emission of greenhouse gases as well as in their flexibility. In the Ph.D. study, the applicability of IOne modules in niche application was demonstrated by integrating them in credit card sized laser pointers.

Additionally, this PhD study has highlighted the need to be conscientious in the choice of materials and processing in the development of PSCs toward a low-cost objective. Whatever the efficiency of the solar cells, PSCs will never realistically have life-time comparable to other established inorganic technologies. Hence, reducing the cost of materials and production in conjunction with increasing the efficiency by the use of novel low-band polymer are the only way that would catapult PSCs on the same platform as the plethora of solar cell technologies that are on the market today. Additionally, this will pave way for competitiveness of PSCs against conventional fossil fuels in the long run. Often, it is difficult to judge whether a better performing architecture at a higher processing cost is worthwhile or not. In such cases, a life-cycle analysis even on laboratory cells can give useful feedback on the feasibility of the particular architecture or system in question.

A running theme throughout the stability studies points toward the need to develop more robust encapsulation methods. Low-cost encapsulation of PSCs has barely been investigated save for few scattered reports. While the food packaging barrier seem sufficient under most realistic indoor and outdoor applications, the contacting methods and edge sealing in our module remains the Achilles heel of initiating the degradation in the modules. Under high humidity conditions, the food packaging barrier may not be sufficient. Hence, new solutions are demanded.

Finally, all the concrete goals of this PhD study as described in Chapter 2 section 2.7 have been met. At the same time, new challenges and new opportunities remain unveiled.

# 10. Appendix

#### **10.1** List of Publications

Hösel, M., Søndergaard, R. R., Angmo, D., & Krebs, F. C. (2013). Comparison of Fast Roll-to-Roll Flexographic, Inkjet, Flatbed, and Rotary Screen Printing of Metal Back Electrodes for Polymer Solar Cells. *Advanced Engineering Materials*, DOI: 10.1002/adem.201300011

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Angmo, D., & Krebs, F. C. (2013). Flexible ITO-Free Polymer Solar Cells. *Journal of Applied Polymer Science*, 129(1), 3-16. DOI: 10.1002/app.38854

Angmo, D., Sweelssen, J., Andriessen, R., Galagan, Y., & Krebs, F. C. (2013). Inkjet Printing of Back Electrodes for Inverted Polymer Solar cells. *Advanced Energy Materials*. DOI: 10.1002/aenm.201201050

Angmo, D., Gonzalez-Valls, I., Veenstra, S., Verhees, W., Sapkota, S., Schiefer, S., Zimmermann, B., Galagan, Y., Sweelssen, J., Lira- Cantu, M., Andriessen, R., Kroon, J. M., & Krebs, F. C. (2013). Low-Cost Upscaling Compatibility of Five Different ITO-Free Architectures for Polymer Solar Cells. *Journal of Applied Polymer Science*, DOI: 10.1002/app.39200

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Angmo, D., Larsen-Olsen, T. T., Jørgensen, M., Søndergaard, R. R., & Krebs, F. C. (2013). Roll-to-Roll Inkjet Printing and Photonic Sintering of Electrodes for ITO Free Polymer Solar Cell Modules and Facile Product Integration. *Advanced Energy Materials*, 3(2), 172-175. DOI: 10.1002/aenm.201200520

Angmo, D., Gevorgyan, S., Larsen-Olsen, T. T., Søndergaard, R. R., Hösel, M., Jørgensen, M., Gupta, R., Kulkarni, G. U., & Krebs, F. C. (2013). Scalability and stability of very thin roll-to-roll processed large area indium-tin-oxide free polymer solar cell modules. *Or-ganic Electronics*, 14, 984-994. DOI: 10.1016/j.orgel.2012.12.033

Angmo, D., Hösel, M., & Krebs, F. C. (2012). All solution processing of ITO-free organic solar cell modules directly on barrier foil. *Solar Energy Materials & Solar Cells*, 107, 329-336. DOI: 10.1016/j.solmat.2012.07.004

Espinosa Martinez, N., García-Valverde, R., Urbina, A., Lenzmann, F., Manceau, M., Angmo, D., & Krebs, F. C. (2012). Life cycle assessment of ITO-free flexible polymer solar cells prepared by roll-to-roll coating and printing. *Solar Energy Materials & Solar Cells*, 97, 3-13. DOI: 10.1016/j.solmat.2011.09.048

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Manceau, M., Angmo, D., Jørgensen, M., & Krebs, F. C. (2011). ITO-free flexible polymer solar cells: From small model devices to roll-to-roll processed large modules. *Organic Electronics*, 12(4), 566-574. DOI: 10.1016/j.orgel.2011.01.009

#### Book chapters:

Hösel, M; Angmo, D, Krebs, F. C. (2013). Organic Solar Cells (OSCs). In O. Ostroverkhova (Ed) *Handbook of organic materials for optical and optoelectronic devices*. (pp- 473– 507), United Kindom--Woodhead Publishing Limited .

Angmo, D., Espinosa, N., Krebs, F., (2013). Indium Tin Oxide (ITO)-Free Polymer Solar Cells. In Zhiqun Lin and Jun Wang (Ed.) *Low-cost Nanomaterials: Toward Greener and More Efficient Energy Applications (submitted)*. Springer Verlag.

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## **10.2** Appendices to Chapter 3.

Table A-1. Round-robin data of ITO-based inverted devices with two different active areas.Two devices of each size were evaluated and the result of both devices is given in table.

Device area	0.36 cm <sup>2</sup>				1 cm <sup>2</sup>			
Laboratory	J <sub>sc</sub>	V <sub>oc</sub>	FF	PCE	J <sub>sc</sub>	V <sub>oc</sub>	FF	PCE
	(mA cm <sup>2</sup> )	(V)	(%)	(%)	(mA cm <sup>2</sup> )	(V)	(%)	(%)
DTU-1	12.32	0.53	56	3.66	8.09	0.55	41	1.84
	12.85	0.51	58	3.82	8.47	0.55	40	1.86
ISE-2	9.71	0.50	56	2.75	8.21	0.54	41	1.82
	10.30	0.51	57	2.99	8.49	0.54	40	1.83
Holst-3	9.82	0.50	60	2.94	6.61	0.53	45	1.58
	10.27	0.50	59	3.04	6.91	0.53	45	1.65
ECN-4	9.89	0.51	60	3.01	7.94	0.54	42	1.80
	10.63	0.51	59	3.19	6.74	0.55	42	1.56
DTU-5	11.00	0.51	59	3.05	8.49	0.54	43	1.95
	11.53	0.52	57	3.11	7.04	0.54	42	1.59

Laboratory	ITO-free	J <sub>sc</sub> (mA cm <sup>2</sup> )	V <sub>oc</sub> (V)	FF (%)	PCE (%)
	architecture				
	NORM	7.15/7.35	0.53/0.52	62/57	2.34/2.18
	ASP	6.10/6.04	0.53/0.53	54/52	1.75/1.66
DTU-1	AGNP	3.55/3.81	0.50/0.54	57/56	1.01/1.15
	ALCR	7.29/6.91	0.58/0.57	63/62	2.66/2.44
	WT	/	/	/	/
	NORM	6.71/7.02	0.53/0.52	61/56	2.17/2.04
	ASP	6.02/5.81	0.52/0.53	51/52	1.60/1.60
ISE-2	AGNP	3.34/3.52	0.49/0.54	61/57	1.00/1.08
	ALCR	6.42/6.42	0.59/0.57	63/62	2.39/2.27
	WT	6.73/6.56	0.58/0.58	38/38	1.48/1.45
	NORM	5.56/5.77	0.52/0.51	62/56	1.79/1.65
	ASP	4.80/4.66	0.51/0.51	53/56	1.30/1.33
Holst-3	AGNP	3.24/3.39	0.48/0.53	55/57	0.86/1.02
	ALCR	6.61/6.29	0.59/0.58	61/61	2.37/2.23
	WT	4.70/4.00	0.57/0.56	38/37	1.00/0.83
	NORM	6.01/7.14	0.52/0.52	62/56	1.94/2.08
	ASP	6.03/5.99	0.52/0.53	52/53	1.63/1.68
ECN-4	AGNP	2.94/3.81	0.50/0.54	57/57	0.84/1.17
	ALCR	7.49/7.02	0.59/0.58	61/61	2.70/2.48
	WT	5.57/6.70	0.58/0.58	27/34	0.87/1.32
	NORM	5.94/7.20	0.53/0.53	61/56	1.92/2.10
DTU-5	ASP	5.99/5.98	0.52/0.53	52/59	1.60/1.64
	AGNP	3.29/3.86	0.50/0.53	51/57	0.83/1.17
	ALCR	7.48/7.06	0.58/0.58	61/60	2.67/2.45
	WT	5.10/6.30	0.54/0.55	27/33	0.74/1.15

 Table A-2: Round-robin data of ITO-free architectures. The results are given for two cells of each architecture that were evaluated, cell 1/cell 2.



Figure A-1: Burn-in region of ISOS-LL stability test of the various ITO-free prototypes. The burn-in loss trend in Voc and FF is suspected to be a direct consequence of the fabrication environment and the use of PEDOT:PSS deposited on top of the photoactive layer as discussed in Chapter 3, section 3.6.2.