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Rasappa, Sozaraj; Schulte, Lars; Borah, Dipu; Morris, Michael A.; Ndoni, Sokol

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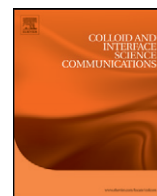
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Rapid Communication

Rapid, Brushless Self-assembly of a PS-*b*-PDMS Block Copolymer for NanolithographySozaraj Rasappa^{a,b}, Lars Schulte^{a,b}, Dipu Borah^{c,d}, Michael A. Morris^{c,d}, Sokol Ndoni^{a,b,*}^a Department of Micro and Nanotechnology, Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark^b Center for Nanostructured Graphene CNG, Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark^c Materials Section, Department of Chemistry, University College Cork, Cork, Ireland^d AMBER, Trinity College Dublin, Dublin-2, Ireland

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ABSTRACT

Block copolymers (BCP) are highly promising self-assembling precursors for scalable nanolithography. Very regular BCP nanopatterns can be used as on-chip etch masks. The first step in the processing of BCP thin films is usually the chemical modification of the substrate surface, typically by grafting of a brush layer that renders the surface energy neutral relative to the constituent blocks. We provide here a first study on rapid, low temperature self-assembly of PS-*b*-PDMS (polystyrene-*block*-polydimethylsiloxane) on silicon substrates without a brush layer. We show that it forms line and antidot patterns after short solvo-thermal annealing. Unlike previous reports on this system, low temperature and short annealing time provide self-assembly in homogeneous thin films covering large substrate areas. This on-chip mask was then used for pattern transfer to the underlying silicon substrate. SEM (scanning electron microscope) images reveal silicon nanowires relative to the PDMS patterns of the BCP mask.

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The modern semiconductor industry continues the goals of ever smaller nanoscopic devices at increasing densities [1–4]. Conventional UV-lithography is significantly challenged to reach the targeted feature size of device components [5–7] and these top-down methodologies are facing critical issues such as cost, time consumption and resist material usage [8]. Alternatively the bottom-up approach based on block copolymer (BCP) self-assembly might lead to the manufacture of similar device dimensions with high precision and nanostructure aspect ratio [9]. Microphase separated BCP thin films in the form of well-arranged, positionally defined nanopatterns can act as scalable nanolithographic masks [10,11]. For diblock copolymer thin films of hexagonal morphology, the minority block cylinders can orientate either perpendicular or parallel to the substrate plane depending on conditions [12, 13]. Some of the diblock copolymers most commonly reported are polystyrene with polyethylene oxide, polymethylmethacrylate and polydimethylsiloxane (PS-*b*-PEO, PS-*b*-PMMA and PS-*b*-PDMS) with PS as majority block for asymmetric copolymers. Of these, PS-*b*-PDMS is of particular interest due to its relatively large Flory–Huggins interaction parameter ($\chi \sim 0.26$), which allows for sub-10 nm feature size [10].

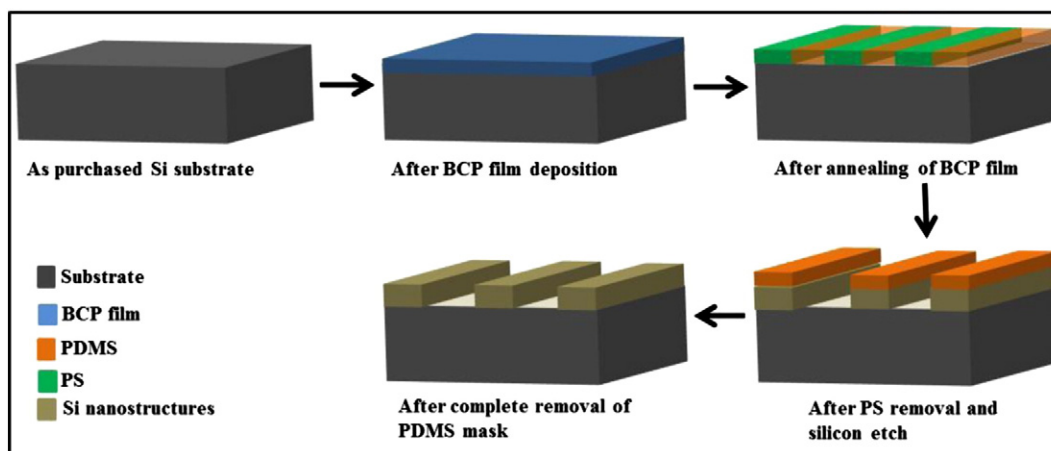
Another attractive property of the PDMS block is that it transforms into a hard mask during oxygen plasma treatment [14]. However, PS-*b*-PDMS films can be difficult to form and usually require the pre-application of a polymer brush to avoid preferential interaction of one block with the substrate [15].

In order to gain acceptance in manufacturing, BCP lithography must conform to strict pre-requisites beyond feature size and defectivity issues. Importantly, large area coverage, pattern orientation control and short total processing time are key parameters for industrial use. Here we report the preparation of large area nanopatterns from PS-*b*-PDMS (30 k–11 k) that fulfils many of these requirements; facile method with no need for a brush layer, short film processing times (<60 s) and a low process temperatures (<60 °C). We also show that the films can be used to produce well-defined silicon features using conventional etch procedures and so demonstrate that the methodology affords a number of clear advantages over accepted techniques.

Scheme 1 describes the overall process for forming pattern transferred silicon features from the microphase separated BCP. Briefly, solvo-thermal annealing is used to generate well-defined PS-*b*-PDMS arrangements. This film is then etched to remove exposed PS and oxidize the PDMS to a silica-like pattern. This is then used as a ‘hard mask’ to allow etching of silicon and produce silicon topography at the substrate.

* Corresponding author at: Department of Micro and Nanotechnology, Technical University of Denmark, DK-2800 Kgs. Lyngby, Denmark. Tel.: +45 4525 8146.

E-mail address: sond@nanotech.dtu.dk (S. Ndoni).



Scheme 1. Process of PS-*b*-PDMS block copolymer self-assembly under solvo-thermal annealing and its use as on-chip mask for silicon nanofabrication.

1. Deposition of Diblock Copolymer and Thin Film Fabrication

Silicon substrates as received within clean room environment and with no prior surface treatment or cleaning were cut into 2.0 cm² pieces. Water contact angle measurements on untreated substrates and on control substrates cleaned by sonication in acetone yielded indistinguishable results, as shown in the supplementary Fig. S1. The PS-*b*-PDMS (30 K–11 K) block copolymer was synthesized following already reported procedure [16,17]. Thin films were prepared by spin casting from a 1 wt.% toluene solution at various spin speeds and spin times as discussed below. The BCP films were initially solvo-thermal annealed at 21 °C (room temperature), 35 °C, 45 °C and 55 °C for 5 to 20 min under toluene vapours in a covered steel chamber mounted on a hot plate to control temperature via a thermocouple in the solvent reservoir. In a separate series of experiments we also tried solvo-thermal annealing at 35 °C at very short times, 10–50 s. After annealing at a given time all the samples were immediately removed from the chamber and left to cool and dry at ambient conditions.

2. BCP Template and Si Nanopattern Fabrication

The solvo-thermal annealed PS-*b*-PDMS films were subjected to selective PS etch using O₂ plasma for 15 s with 2000 W power in ICP and 400 W power in RIE at 2.0 Pa pressure. SF₆ and CF₄ plasma at 70 sccm and 35 sccm flow rate with ICP (Inductively coupled plasma) and RIE (Reactive ion etching) powers of 1200 W and 200 W at 1.9 Pa pressure was used to etch silicon. The final PDMS removal was done by just CF₄ plasma with 15 sccm for 10 s with ICP and RIE powers of 1200 W and 30 W at 1.6 Pa pressure.

3. Characterisation of Materials

Film thickness. PS-*b*-PDMS film thickness was determined by ellipsometry (VASE system). Average values at three locations on the substrate are reported as film thickness in Table S1. Film thickness decreases at increased spin speed and spin time and the difference is about ~5 nm from initial to final spin parameters.

4. Scanning Electron Microscopy

Top-down and tilted SEM images of BCP, oxidised PDMS and silicon nanofeatures were obtained by using a Field Emission Zeiss Ultra Plus scanning electron microscope with a Gemini column operating at an accelerating voltage of 3 kV. Unless otherwise stated, all SEMs shown are following PS removal by O₂ plasma and consequential oxidation of PDMS.

The block copolymer thin films of PS-*b*-PDMS (30 k–11 k) spin-coated at a spin speed of 3200 rpm for 30 s, annealed at various temperatures and times, are described in Fig. 1 (following removal of the PS/PDMS oxidation). The images of samples annealed at 35 °C or higher are consistent with a predominantly horizontal orientation of the PDMS cylindrical domains, observed as white lines in the images. Annealing at 21 °C (room temperature) resulted into poorly defined patterns for all the four annealing times. These observations can be understood as due to a combination of two effects: (1) PDMS has a much lower surface tension ($\gamma_c = 24 \text{ mN m}^{-1}$) than PS ($\gamma_c = 32.8 \text{ mN m}^{-1}$) [18] that would lead to preferential PDMS surface segregation; (2) this may be compensated by the fact that the annealing solvent is toluene ($\delta_{\text{Hildebrand}} \equiv \delta_H = 18.2 \text{ (MPa)}^{1/2}$), which is a preferential solvent for PS ($\delta_H = 18.7 \text{ (MPa)}^{1/2}$) over PDMS ($\delta_H = 14.9 \text{ (MPa)}^{1/2}$) [18]. At room temperature the low toluene vapour pressure is insufficient to fully compensate for the PDMS surface segregation, while the compensation is realized at the higher temperatures. It is clearly observed that annealing at 35 °C for 10 min provided the greatest selectivity to line patterns compared to the other process conditions described in Fig. 1. At higher temperatures and times the lines become less continuous and the persistence length diminishes. However the trend is not very pronounced; for example the images at 20 min annealing are very similar for both 35 °C and 45 °C.

Curiously, ring-like patterns, or antidots are also seen in most of the conditions; in some cases these form local antidot meshes, like the image at 20 min, 35 °C (see also Figs. 3 and S2). We speculate that the antidots are formed by a combination of a PS wetting layer at the polymer-substrate interface superimposed by a perforated PDMS lamella structure formed during annealing. Similar structures were also observed in the case of brushless lamellar PS-*b*-PEO thin films [19]. The possibility to control antidot pattern formation through understanding of the responsible mechanism would open up for an exciting fabrication route of antidot lattice masks.

Fig. 2 shows tilted SEM images of the samples depicted in Fig. 1 excluding the samples annealed at room temperature with no clearly arranged nanopatterns. The cross-sections are consistent with uniform block copolymer film thickness as will also be shown later on in Fig. 4. The periodicity of the line patterns is optimal following annealing at 35 °C for 10 min, as confirmed by fast Fourier transform (FFT) analysis of the images in Fig. 1. At these same annealing conditions the average line segment length between two defects is largest and exceeds 600 nm.

Figs. 1 and 2 show that the oxidised PDMS lines formed by plasma treatment have feature sizes of 12–15 nm. The SEM images suggest a single layer of cylinders was present since the height is uniform and

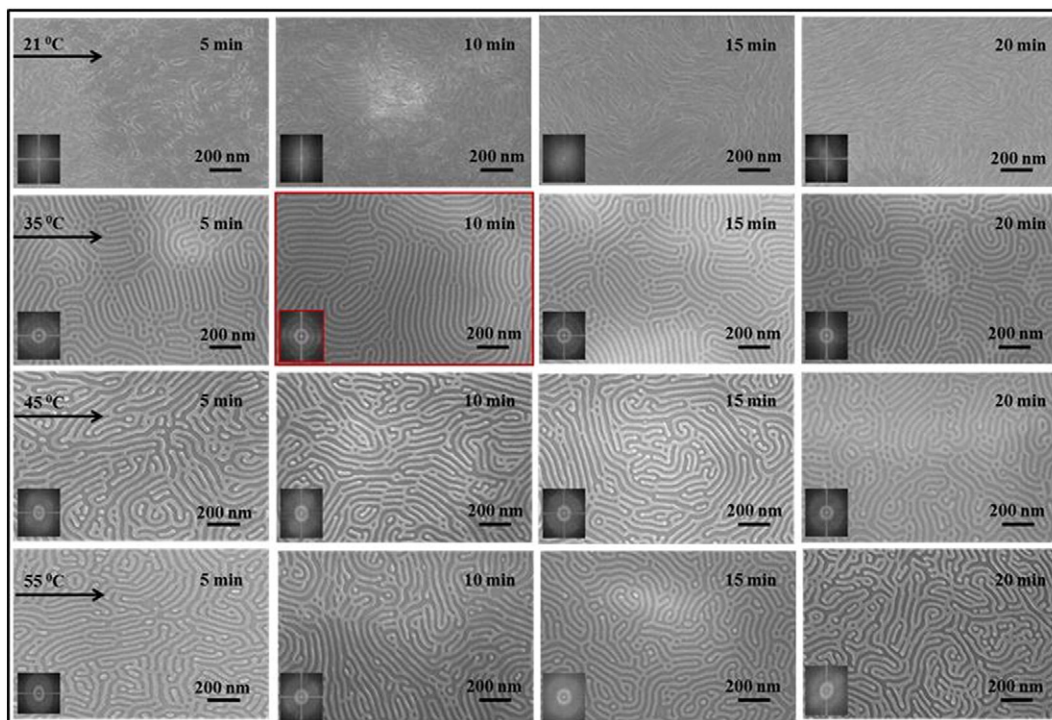


Fig. 1. Top-down SEM images of PS-*b*-PDMS (30 k–11 k) spin coated on silicon substrate at 3200 rpm for 30 s and annealed, after PS removal. Left to right: annealed from 5 min to 20 min. Top to bottom: annealed at 21 °C to 55 °C. The insets at the bottom-left corner of each image show fast Fourier transforms (FFT) of the respective images. The three harmonics most neatly visible for the FFT of image at 35 °C, 10 min confirm the optimum annealing conditions. At the other extreme the FFT-s relative to samples annealed at 21 °C do not show any characteristic structural periodicity, with the possible exception of the sample annealed for 20 min.

consistent with the domain spacing noted above. It should be noted that in the present solvo-thermal annealing no dewetting or island formation could be observed in contrast with previous studies [10]. The absence of dewetting and island formation could be due to the shorter

anneal times used compared to lengthy solvent or thermal annealing processes applied in earlier studies [4,10].

A slight increase in oxidised PDMS feature size with anneal temperature can be seen and the width of oxidised PDMS lines is 2–

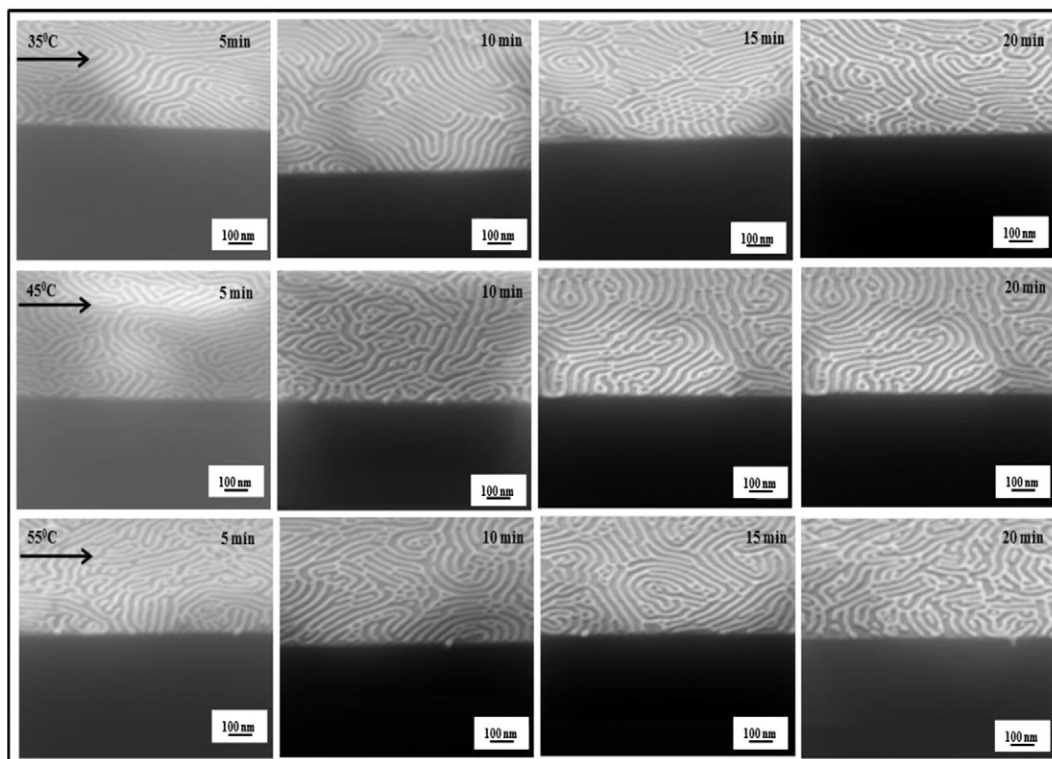


Fig. 2. Tilted SEM images of PS-*b*-PDMS (30 k–11 k) after PS removal. Spin coated on silicon substrate at 3200 rpm for 30 s. Left to right: annealed from 5 min to 20 min. Top to bottom: annealed at 35 °C to 55 °C.

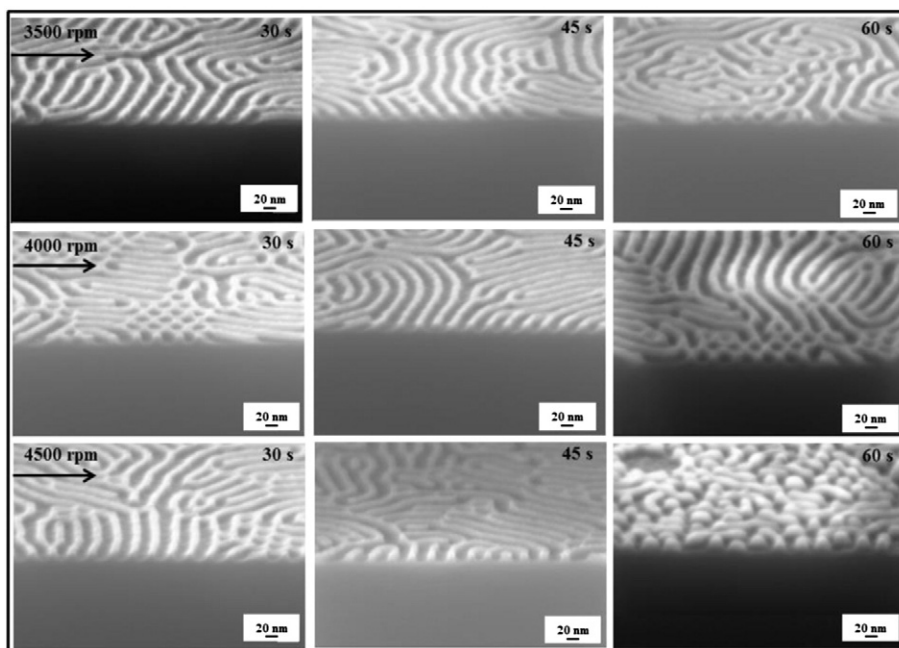


Fig. 3. Tilted SEM images of silicon nanowires fabricated from PS-*b*-PDMS (30 k–11 k). Left to right: Spin coated on silicon substrate at 30 s to 60 s. Top to bottom: Spin coated on silicon substrate from 3000 rpm to 4500 rpm.

3 nm larger at 45 °C and 55 °C than at 35 °C. This might suggest that higher temperature annealing results in inclusion of free volume, which would increase the period length-scale. Optimum annealing conditions at 35 °C for 10 min have been used for the experiments described in Figs. S1 and 3.

Fig. S2 shows top-down SEM images of PS-*b*-PDMS films (after the usual plasma etch) spin-coated at various spin speeds and times, and annealed at the optimum time and temperature defined above. The film thicknesses of the as-cast films were determined by ellipsometry and the data compiled in Table S1. The total variation in film thickness is around 5.3 nm but this largely did not seem to have a significant contribution to the quality of the pattern, suggesting this thickness is close to optimum. The pattern formed at spin speed 4500 rpm and time 60 s does seem noticeably worse than others with pronounced line discontinuity and short persistence length, suggesting that the film thickness is less than the optimum for a single layer of cylinders. Note also the presence of antidot patterns in these images, especially well-developed at 4000 rpm and 60 s. The quality of the patterns obtained at optimum annealing conditions was assessed relative to the

concentration of three types of defects, dots, antidots and dead ends, as shown in Figs. S2 and S3.

The resultant oxidised PDMS cylinders were used as an effective mask to transfer the BCP pattern to the substrate as shown in Fig. 3. A statistical defect analysis for the fabricated silicon nanostructures at optimised condition is shown in supplementary Fig. S4. The final silicon nanostructures show average depth of 19 nm and width of 12 nm in all structures, as illustrated in the graphical abstract. Both the line and antidot arrangements observed in the top-down images are transferred to the substrate in a similar way, which is compatible with a homogeneous monolayer BCP film covering the surface.

A PS wetting layer at the polymer-substrate interface mentioned in the discussion of Fig. 1 is compatible with the PDMS nanopattern transfer to the substrate. It should be noted that the optimum pattern transferred film is formed following spin-coating at 4000 rpm for 45 s. The data confirm again that the film formed at 4500 rpm and 60 s is below optimum thickness with clearly seen film discontinuities and ‘holes’.

Since it was clearly shown in Fig. 1 that well-arranged PDMS lines were formed at anneal times as low as 5 min, we investigated self-

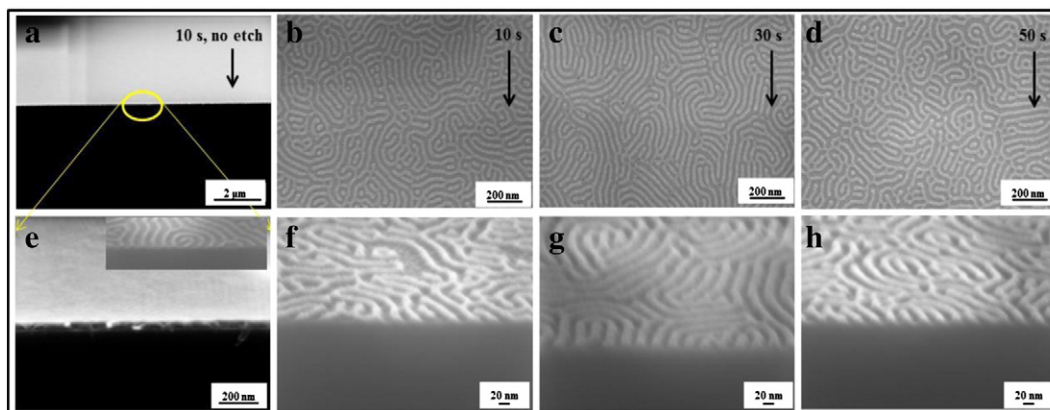


Fig. 4. Top-down and tilted SEM images of PS-*b*-PDMS after 10–50 s annealing times. a and e: low and high magnification of cross-sectional SEM image annealed for 10 s prior to O₂ plasma etching (inset shows PDMS lines after PS etching). b–d: PDMS structures annealed for 10 s, 30 s and 50 s after PS removal. f–h: Corresponding silicon nanostructures fabricated.

assembly at 35 °C and sub-60 s anneal time. Fig. 4 shows the top-down SEM images of the plasma treated BCP thin films after 10–50 s anneal times. The images clearly prove that even at such short annealing times line nanopatterns are formed (b–d). In all cases, the films are coherent and of uniform thickness. These can also be used for pattern transfer to the substrate (f–h). The silicon features formed from these short anneal patterns have feature sizes of 12 nm.

In conclusion, we have demonstrated for the first time that very short time and low temperature solvo-thermal annealing are effective in producing line patterns from PS-*b*-PDMS films on untreated silicon substrates. The self-assembly is extremely rapid with well-arranged patterns formed in time periods as low as 10 s. No surface functionalization (e.g. using a brush or other methods) is required to see high substrate coverage and highly uniform film thickness across the substrate, which is a significant process simplification relative to accepted procedures. A distinct advantage over systems using PDMS brushes is that these can complicate the pattern transfer process through formation of thick silica like passive layers. One of the reasons that brushes may not be needed is that the agglomeration of polymer into 3D island structures (a mass transport limited process) cannot occur quickly enough in these short anneal periods. It is also worth noting that the diameter of the PDMS cylinders and corresponding lines are strongly related to anneal time with the shorter times and lower temperatures resulting in smaller features. We postulate that this might be due to free-volume inclusion at the PS domains and at the PS-PDMS interface formed during solvent annealing and drying. As the solvent swells, the degree of swelling increases with time and temperature. When the samples are removed, the solvent quickly evaporates (since the films are thin), effectively freezing the PS and interface arrangement and resulting in free-volume inclusion which increases the domain volume. The data also suggest microphase separation is rapid, which is consistent with the high Flory–Huggins parameter.

After this first demonstration of swift brushless silicon nanopatterning by PS-*b*-PDMS masks there is a clear need for further work to assess the applicability of the method to other block copolymers.

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Appendix A. Supplementary data

Supplementary data to this article can be found online at <http://dx.doi.org/10.1016/j.colcom.2014.07.001>.

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