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Efficiency Optimization by Considering the High Voltage Flyback Transformer Parasitics using an Automatic Winding Layout Technique

Prasanth Thummala*, *Student Member IEEE*, Henrik Schneider, *Student Member IEEE*, Zhe Zhang, *Member IEEE*, Ziwei Ouyang, *Member IEEE*, Arnold Knott, *Member IEEE*, and Michael A. E. Andersen, *Member, IEEE*

***Abstract*—This paper presents an efficiency optimization approach for a high voltage bidirectional flyback dc-dc converter. The main goal is to optimize the converter for driving a capacitive actuator, which must be charged and discharged from 0 V to 2.5 kV dc and vice versa, supplied from a 24 V dc supply. The energy efficiency is optimized using a proposed new automatic winding layout (AWL) technique and a comprehensive loss model. The AWL technique generates a large number of transformer winding layouts. The transformer parasitics such as dc resistance, leakage inductance and self-capacitance are calculated for each winding layout. An optimization technique is formulated to minimize the sum of energy losses during charge and discharge operations. The efficiency and energy loss distribution results from the optimization routine provide a deep insight into the high voltage transformer design and its impact on the total converter efficiency. The proposed efficiency optimization approach is experimentally verified on a 25 W (average charging power) with 100 W (peak power) flyback dc-dc prototype.**

***Index Terms*—switched-mode power supply, high voltage dc-dc power converter, transformer design, optimization, energy efficiency, actuators, dielectric films**

NOMENCLATURE

a_{uC}, b_{uC}	Coefficients of Fourier series of the magneto motive force (MMF) during charge process (AT: Ampere-turns)
B_{mC} / B_{mD}	Maximum flux density during charge / discharge process (T)
B_{nC}	Magnitude of negative flux density at the beginning of a switching cycle during charge process (T)
ΔB	Peak-to-peak flux density of the current excitation (T)
C_{in} / C_{load}	Input capacitance / Capacitance of the load or actuator (F)
C_s	Self-capacitance of secondary winding (F)
C_{ossp} / C_{osss}	Output capacitance of low voltage MOSFET M_p / high voltage MOSFET M_s (F)
C_{Db}	Junction capacitance of high voltage diode D_b (F)
d_p / d_s	Diameter of primary / secondary winding of transformer (mm)
D_2 / D_b	High voltage (5 kV) freewheeling diode / blocking diode
$d_{insulation}$	Uniform spacing or thickness of the insulating tape, between secondary layers (mm)
D_{onC} / D_{offC}	On-time / Off-time duty cycle of low voltage MOSFET M_p during charge process
D_{onD} / D_{offD}	On-time / Off-time duty cycle of high voltage MOSFET M_s during discharge process
$E_{load}(V_{out})$	Stored energy in the load at an output voltage V_{out} (J)
f_{swC} / f_{swD}	Switching frequency during charge / discharge process (kHz)
FF_{LL}	Fill factor of the last layer in the high voltage winding
$F_{uC}(0)$ / $F_{uC}(h)$	MMF amplitude of u^{th} harmonic at x=0 / x=h, h is the thickness of layer
G_1, G_2	Constants used in the power loss expressions and are functions of ε_u
H_W	Window height of transformer bobbin (mm)
i_{in} / i_p / i_s	Input current / Primary current / Secondary or load current (A)
i_{mp} / i_{ms}	Primary / Secondary magnetizing current (A)
I_{ppkC} / I_{ppkD}	Primary peak current during charge process / discharge process (A)
I_{spkC} / I_{spkD}	Secondary peak current during charge process / discharge process (A)
i_{min}	Magnitude of the negative primary current at the beginning of charge process (A)
I_{pavgC} / I_{savgC}	Primary / Secondary average current during charge process (A)
k_z	Core loss constant in the improved generalized Steinmetz equation (*i*GSE)
L_{mp} / L_{ms}	Primary / Secondary magnetizing inductance of transformer (H)
L_{lkp} / L_{lks}	Leakage inductance referred to primary / secondary side of transformer (H)
M_p / M_s	Low voltage MOSFET / High voltage (4 kV) MOSFET

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All authors are with the Electronics Group, Department of Electrical Engineering, Technical University of Denmark, Kongens Lyngby, DK-2800 Denmark.

E-mail: *pthu@elektro.dtu.dk, hensc@elektro.dtu.dk, zz@elektro.du.dk, zo@elektro.dtu.dk, akn@elektro.dtu.dk, ma@elektro.dtu.dk.

*Indicates the corresponding author.

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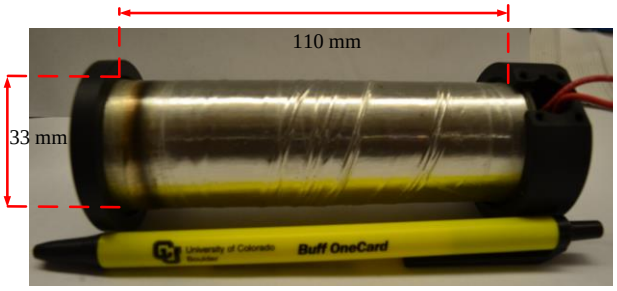
N_p / N_s / n	Number of primary / secondary turns / Turns ratio of transformer from secondary to primary
n_{lp} / n_{ls}	Number of layers in primary / secondary winding of transformer
n_{parp} / n_{pars}	Number of parallel wires in primary / secondary winding of transformer
N_h / N_c	Total number of harmonics considered / Total number of switching cycles during charge process
P^k_{layerC}	Power loss in k^{th} layer during charge process (W)
P_{windC} / P_{TwindC}	Winding loss at each switching cycle / Total winding loss during charge process (W)
P_{swC} / P_{swD}	Capacitive switching loss due the self-capacitance during charge / discharge process (W)
P_{snC} / P_{snD}	Snubber loss due leakage inductance during charge / discharge process (W)
R_p / R_s	dc resistance of primary / secondary winding of transformer (Ω)
R_{psense} / R_{ssense}	Primary / Secondary current sense resistance (Ω)
R_{layer}	dc resistance of a given layer (Ω)
t_{onC} / t_{offC}	On-time / Off-time of low voltage MOSFET M_p during charge process (s)
t_{onD} / t_{offD}	On-time / Off-time of high voltage MOSFET M_s during discharge process (s)
T_{sC} / T_{sD}	Switching period during charge / discharge process (s)
T_{ch}	Charging time to reach the target output voltage from 0 V (s)
T_{layer}	Number of turns in a given layer (primary or secondary) of transformer
V_{leakD}	Increase in the steady state drain-to-source voltage of M_s due to leakage inductance L_{lks} (V)
V_{in} / V_{out}	Input voltage / Output or load or actuator voltage (V)
W_W	Window width of bobbin (mm)
W_{sqp} / W_{sqs}	Width of square for primary / secondary in the automatic winding layout generator routine (mm)
γ_s / γ_p	Height allocation factor for secondary / primary winding with γ_p=(1-γ_s)
δ_u / δ	Skin depth of the conductor at u^{th} harmonic frequency / fundamental (u=0) frequency (mm)
ε_u	Ratio of conductor diameter to the effective skin depth of u^{th} harmonic
$\varphi_{uC}(0)$ / $\varphi_{uC}(h)$	Phase of u^{th} harmonic of the MMF during charge process at x=0 / x=h (h is thickness of layer)
ρ / μ_0	Resistivity of copper (Ω-m) / Magnetic permeability of vacuum (H/m)
α, β, k	The constants related to core material which are provided by the core manufacturer
δ_C	Capacitance ratio factor on the high voltage side

I. Introduction

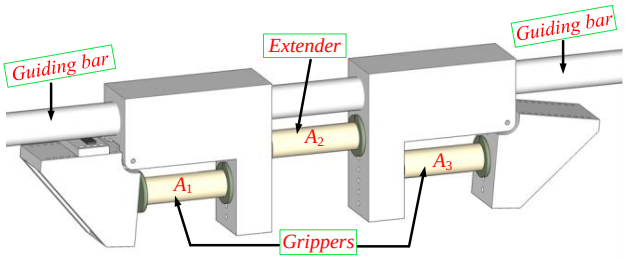
DIELETRC electro active polymer (DEAP) [1]-[3] is an evolving smart material that can be used in actuation, sensing and energy harvesting applications [4]. DEAPs, when used as linear actuators, have the potential to be an effective replacement for many conventional linear actuators because of their unique properties, including light weight, low noise operation, high flexibility, large strain, and autonomous capability. The axial DEAP actuator as shown in Fig. 1(a) is ideally equivalent to a capacitive load. When a DEAP actuator is driven with high voltage (2-2.5 kV), it converts a portion of the electrical energy into mechanical displacement, which is of the order of mm (~1-1.5 mm) [5]-[7]. Three of such axial DEAP actuators are used to create a DEAP incremental actuator [8] as shown in Fig. 1(b). The DEAP incremental actuator technology has the potential to be used in various industries, e.g. automotive, aeronautics, and medicine. For using the DEAP actuators in such applications, the high voltage drivers should have low volume to fit inside or above the actuators. The overall energy efficiency of battery powered, high voltage driver influences, the distance travelled by the incremental actuator. Hence, for DEAP actuator applications, both volume and energy efficiency of high voltage drivers are extremely important and need to be optimized.

The flyback converter is suitable for high voltage and low power applications due to its simple structure and a low component count [9]. High voltage switch-mode power supplies for charging the capacitive loads are implemented in [10]-[12]. Bidirectional dc-dc power converters are needed for the DEAP based capacitive actuators [13], to increase the lifetime of the battery, also to discharge the high voltage across them. Bidirectional flyback converter [14]-[17], and a forward-flyback bidirectional converter [18] are implemented for various applications. Due to high reverse recovery time (~2.6 μs) of high voltage MOSFET, a modified high voltage bidirectional flyback converter topology [19] as shown in Fig. 2, is proposed and implemented for driving a DEAP actuator. The loss analysis of the same converter is performed in [20].

Transformer design plays a very important role in high voltage dc-dc power converters employed in low, medium and high power applications. The design methodologies for transformers used in conventional switch-mode power supplies are well documented [9], [21]-[23]. Often, a transformer for a given application is designed based on some assumptions such as, constant switching frequency, maximum



a)



b)

Fig. 1. a) DEAP actuator; b) DEAP incremental actuator.

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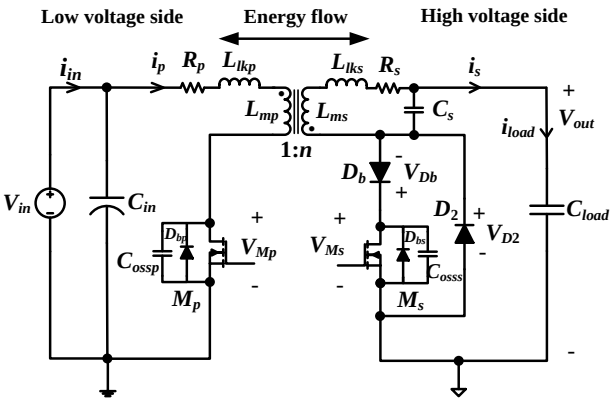

Fig. 2. Circuit configuration of the high voltage bidirectional flyback converter for driving a capacitive load.

temperature rise, estimated converter efficiency, winding fill factor, and winding current density. However, these assumptions are not valid or suitable for some applications. Hence, more customized procedures are needed to design efficient transformers, for specific applications. In a high voltage capacitor charge and discharge application, the high voltage transformer will have a large amount of (> 200) secondary turns. For such application, it is very difficult to select an optimum winding diameter and number of winding layers beforehand, which decide the values of the transformer parasitics. To avoid this difficulty, an automatic winding layout (AWL) technique is introduced in [24], for the winding design of a high voltage transformer. The high voltage flyback converter operation is very sensitive to the transformer parasitics. The proposed AWL technique, utilizes the entire available space in a given transformer bobbin and provides an optimum winding diameter that minimizes the total loss due to the transformer parasitics.

In the initial design phase, it is difficult to predict which core type is optimal for a given application. In a flyback converter, a long transformer window width is often preferred, in order to minimize the leakage inductance and ac resistance by providing a close coupling between windings, and to decrease the number of winding layers. For high output or input voltage flyback converters, this could be different, since the self-capacitance of the high voltage winding has significant impact on the performance of the converter. In this paper, an efficiency optimization algorithm is proposed, which provides an optimum solution for a given transformer core, by using the proposed AWL technique and the comprehensive loss model. Different transformer winding architectures (TWAs) for the high voltage capacitor charge and discharge application are investigated in [25]. In [26], a digital control technique is proposed for improving the energy efficiency and charge/discharge speed. Control algorithms for optimal-flyback charging of a capacitive load are proposed in [27]. A number of switch-mode power supply design optimization methods have been described in the literature [28]-[34].

The proposed efficiency optimization technique has the following features:

1) an automatic winding layout (AWL) technique, which produces the
2) information about winding diameters, number of layers, and number of parallel windings, for both primary and secondary windings;
3) an accurate calculation of transformer parasitics using the outputs of AWL technique;
4) calculation of energy losses during charge and discharge modes using a comprehensive loss model;
5) an objective function that minimizes the sum of energy losses during charge and discharge modes, over a range of operating points.

This paper is organized as follows: Section II describes the proposed automated winding layout (AWL) technique. Section III provides the loss modeling of the bidirectional flyback converter. Section IV discusses the proposed optimization routine. Section V provides the optimization and experimental results, followed by the conclusions in Section VI.

II. Automatic Winding Layout (AWL) Technique

The bidirectional flyback converter design specifications are provided in Table I. The magnetic transformer is the most critical component in the high voltage bidirectional flyback converter. The leakage inductance causes voltage spikes across the drain-to-source of the MOSFET, and this can be avoided by a dissipative snubber circuit or by using an over rated MOSFET. The self-capacitance of the secondary winding creates large resonating current spikes in the leading edge of the MOSFET current waveform [19]. Additional switching losses will be created due to those two parasitics, respectively [30]. The remaining losses in the transformer are core loss, and the winding loss due to dc and ac resistances. The losses due to the high voltage transformer need to be minimized to improve the bidirectional flyback converter efficiency and reliability.

TABLE I
Converter Design Specifications

Parameter	Value
Input voltage V_{in}	24 V
Output voltage V_{out}	0-2500 V
Capacitance of load C_{load}	400 nF
Stored energy in the load E_{load} at 2.5 kV	1.25 J
Target charging time T_{ch}	50 ms
Turns ratio of the transformer n	25
Primary magnetizing inductance L_{mp}	44 μH
Primary peak current during charge process I_{ppkC}	4.2 A
Primary peak current during discharge process I_{ppkD}	5.3 A

The transformer design decisions considered for the proposed AWL technique are given in Table II. The core types are limited to ETD, EFD, E, RM and PQ. The N87 core material is chosen for most of the cores, due to its lower core losses at high frequency up to 500 kHz. For those cores for

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which N87 material is not available, other core materials which are suitable for operation up to 500 kHz are considered. A simple, non-interleaved winding structure (P/S; P: Primary, S: Secondary), is considered in this paper to limit the complexity of the proposed AWL technique. Nevertheless, the proposed AWL technique can be easily extended for the interleaved transformer structures (P/S/P or S/P/S). The proper insulation between the low voltage (primary) and high voltage (secondary) windings is achieved by using a triple insulated (TEX-E) solid wire for primary winding. To avoid the high insulation thickness (0.2 mm) of TEX-E wire, single insulated solid wire is used for a large number of secondary turns. A maximum transformer temperature limit of 130 °C is chosen. These limitation values can be altered based on the experience of the user or the initial design specifications.

The AWL technique is described below:

A. AWL technique:

The space allocated for the primary and secondary windings for a given transformer bobbin with winding width W_W and window height H_W are shown in Fig. 3(a). Different steps associated with the proposed AWL technique for an example of N_p=6 primary turns and N_s=18 secondary turns, are explained below:

1) The first step is, to split the available winding space for primary (see Fig. 3(a)) and secondary (Fig. 3(f)) into a number of squares, with a square width equal to height allocated for that winding. As shown in Figs. 3(d) and 3(g), it results into 4 squares and a crossed non-square, which is considered as an unusable space for both primary and secondary windings. In each square, a solid round wire could be placed with a diameter equal to the width of a square or a bundle of round wires with an outside bundle diameter equal to the width of a square.
2) Since the number of available squares is 4 in Figs. 3(d) or 3(g), which is less than the required 6 primary and 18 secondary turns, more squares are required to fill the needed turns. Hence, the width of square for primary or secondary is decreased from its maximum value of $\gamma_p H_W$ or $\gamma_s H_W$, respectively.
3) The fill factor of the last layer FF_{LL} for a given winding is defined as the ratio of the number of squares used in the final layer to the number of squares available in it. For example, in Fig. 3(i), 9 squares are available and 9 squares are occupied in the final layer, hence FF_{LL}=1. Similarly, in Fig. 3(j), 16 squares are available and 13 squares are occupied in the final layer, hence FF_{LL}=0.81. In the proposed AWL technique a maximum limit of 0.85 is set for FF_{LL}, since the calculation of transformer parasitics is based on fully occupied layers.
4) When the square width is reduced as shown in Figs. 3(e) and 3(h), the new square size limits the use of a shaded space above the squares. For primary winding since only 6 turns are needed, this will be a valid solution. However, for secondary winding, since 18 turns are needed, the shaded space can be occupied by the other windings, by reducing the square width further.
5) When the square width is reduced further as shown in Fig. 3(i), the winding space contains 18 squares in 2 layers, and a shaded space. The non-square horizontal space is utilized to provide an insulation tape (with thickness $d_{insulation}$) between the secondary layers. This is the final step of the AWL technique for 6 primary and 18 secondary turns.
6) If 45 turns are required for the secondary winding, the square width is decreased again, as shown in Fig. 3(j), the solution contains 3 layers and 16 squares in each layer. The last layer fill factor FF_{LL} in this case is 0.81, which is less than 0.85. Hence, this is not a valid solution and the square width needs to be decreased further.
7) In Fig. 3(b), a solution from the AWL technique is shown. The primary and secondary squares are filled with triple isolated and single isolated solid wires, respectively. The same steps described above apply for the real high voltage transformer design which will have more than 200 secondary turns.
8) Finally, the outputs of AWL technique are various winding implementations, including specific winding details such as, diameters of primary and secondary windings, number of primary and secondary winding layers, and insulation thicknesses for placing between secondary windings, for which FF_{LL}>0.85, respectively.

TABLE II
TRANSFORMER DESIGN DECISIONS

Description	Design decision	Comments
Ferrite core and bobbin type	ETD, EFD, E, RM and PQ	Typically used in switch-mode power supplies.
Core material	N87	Suitable for switching frequencies up to 500 kHz.
Winding structure	P/S	Simple implementation and decreases analytical complexity.
Primary winding type	Solid wire	Flexible winding type in terms of design and prototyping.
Primary winding insulation	Triple insulation (TEX-E)	Edge tape can be avoided. No need for interlayer insulation tape between the primary and secondary windings.
Secondary winding type	Solid wire	Suitable winding type, for a large number of turns. Flexible winding type in terms of design, prototyping and different winding structures.
Secondary winding insulation	Single insulation	Provides minimum insulation thickness for a large number of turns.
Air gap	All legs	Simplifies the prototyping.
Maximum transformer temperature	130 °C	With a predicted ambient temperature of 35 °C, this enables transformer temperature rise of 95 °C.

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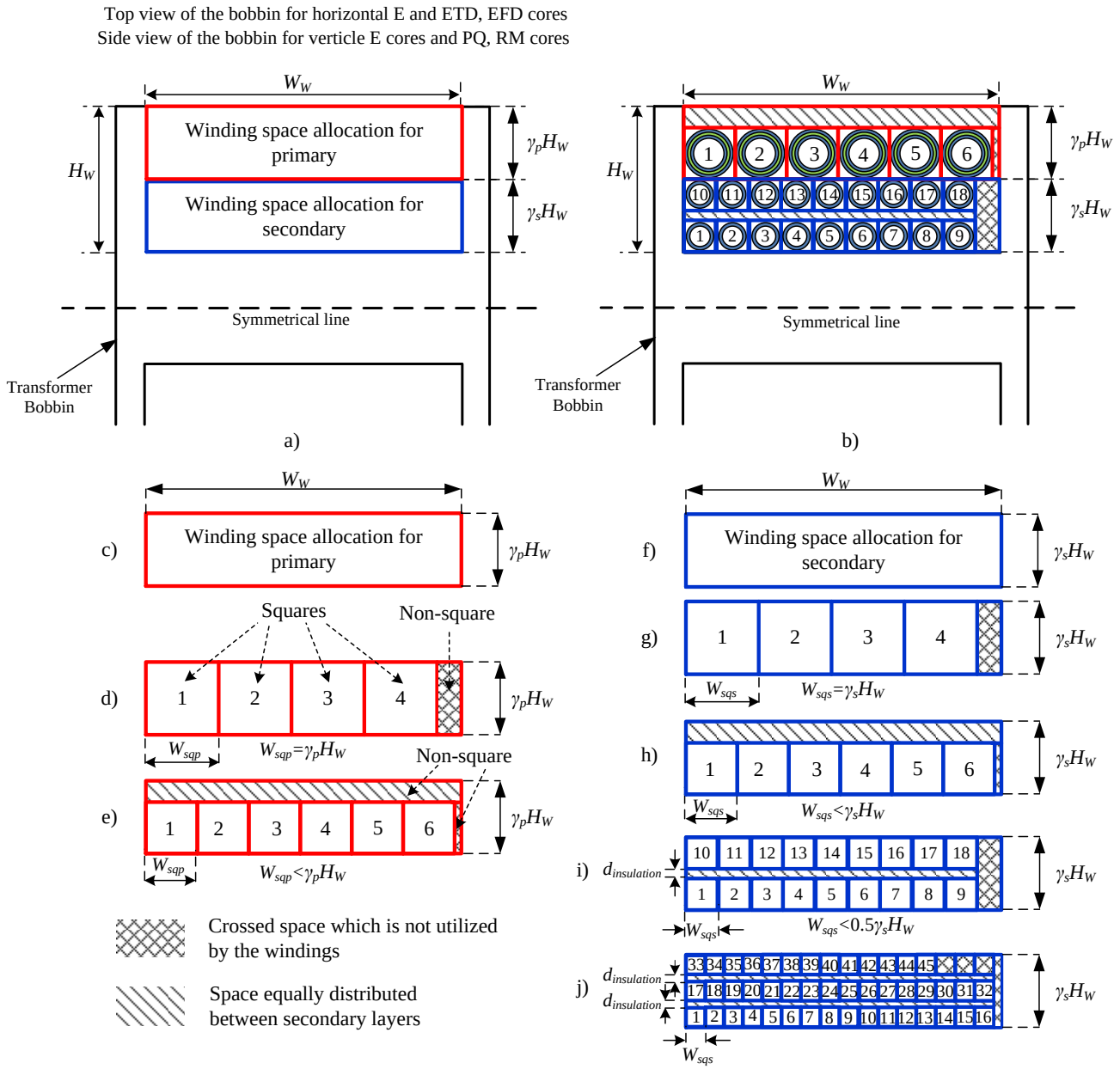

Fig. 3. a) Allocated winding space a) before applying AWL technique; b) after applying AWL technique; c) - e) Different steps involved in AWL technique for primary winding; f) - j) Different steps involved in AWL technique for secondary winding;

B. Calculation of transformer parasitics using the results of AWL technique:

The outputs of the AWL technique are used to calculate the transformer parasitics [20], [24], [35]-[37] such as dc resistance, leakage inductance and self-capacitance. In Fig. 4, one output of AWL technique such as the insulation thickness ($d_{insulation}$) for a PQ 20/20 core, and calculated transformer parasitics are shown with respect to square width (W_{sqs}) of secondary winding. As the width of the secondary square (or secondary winding) decreases, the insulation spacing $d_{insulation}$ between secondary winding layers increases, dc resistance R_s increases, leakage inductance L_{lkp} slightly decreases, and the self-capacitance C_s decreases.

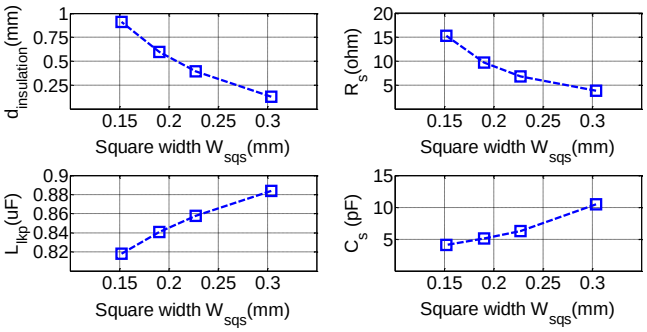

Fig. 4. Variation of transformer parasitics with the diameter of secondary winding, for PQ 20/20 core (when γ_s=0.8).

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III. Loss Modelling

In order to investigate the bidirectional flyback converter efficiency, it is necessary to calculate the losses associated with each circuit component in the converter. The loss model is a function of transformer parasitics. Different losses in the bidirectional flyback converter are given below:

A. *Transformer winding loss:*

In a flyback converter the primary and secondary currents are 180° out of phase, hence the conventional equations cannot be used to calculate the ac resistance [38], [39]. The calculation of the total winding loss in a flyback converter using the magneto motive force (MMF) analysis [40], [41] is described below.

1) Winding loss in a flyback transformer during charge process:

For the winding loss modeling, a non-interleaved transformer with 2 layers on the primary side (P_1 and P_2) and 5 layers on the secondary side (S_1, S_2, S_3, S_4 and S_5), is considered as an example. The MMF distribution in a flyback transformer is different from that of a normal transformer [40]. Figure 5 shows different MMF distributions during both turn-on ($0<t<t_{onC}$) and turn-off ($t_{onC}<t<t_{onC}+t_{offC}$) periods in a non-interleaved flyback transformer. In Fig. 5, N_{p1} and N_p, are the number of turns in the primary layer 1 and the total primary turns, respectively, and H_0, H_1,….H_7 are the magnetic field intensities between the layers. The terms N_1, N_2, N_3, N_4, N_5 are defined as follows: $N_1=N_{s1}$, $N_2=N_{s1}+N_{s2}$, $N_3=N_{s1}+N_{s2}+N_{s3}$, $N_4=N_{s1}+N_{s2}+N_{s3}+N_{s4}$, and $N_5=N_{s1}+N_{s2}+N_{s3}+N_{s4}+N_{s5}=N_s$ where N_{s1}, N_{s2}, N_{s3}, N_{s4}, N_{s5} and N_s are the number of turns in the secondary layers 1, 2, 3, 4, 5, and the total number of secondary turns, respectively. The primary $i_{mp}(t)$ and secondary $i_{ms}(t)$ magnetizing current waveforms in a given switching cycle, during charge and discharge processes are shown in Figs. 6(a) and 6(b), respectively. The MMF distribution in each transformer winding layer in the time

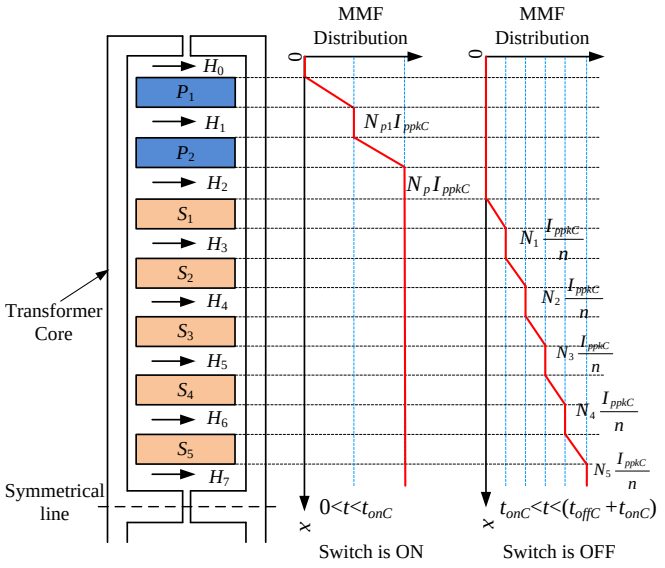

Fig. 5. MMF distribution of the non-interleaved (P-P-S-S-S-S-S) flyback transformer with respect to space.

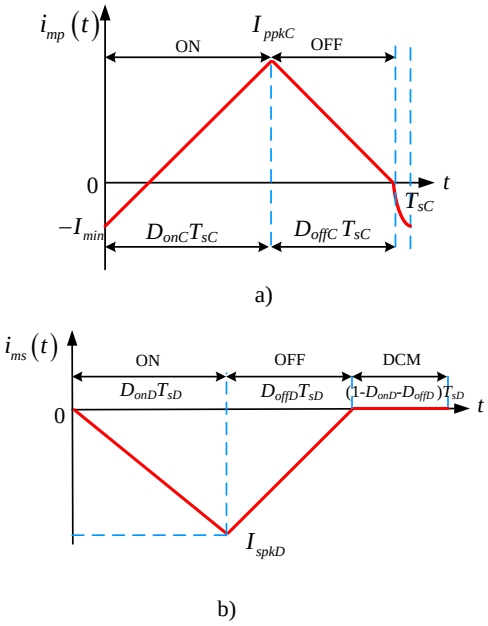

Fig. 6. a) Primary magnetizing current in a given switching cycle during charge process, and b) Secondary magnetizing current discharge process.

domain is decomposed into sinusoidal harmonics by Fourier series analysis [24]. The power loss is then computed for each harmonic, and the power loss densities over all harmonics are summed to find the power dissipated in each layer.

The power loss expression in k^{th} layer P^k_{layerC} is given by [24], [40], [41]

$$P^k_{layerC}=\frac{R_{layer}}{2T^2_{layer}}\sum_{u=1}^{N_h}\varepsilon_u\begin{bmatrix}\left(\left|F_{uC}(h)\right|^2+\left|F_{uC}(0)\right|^2\right)G_1(\varepsilon_u)-\\ 4\left|F_{uC}(h)\right|\left|F_{uC}(0)\right|\cos(\Delta\varphi)G_2(\varepsilon_u)\end{bmatrix} \quad (1)$$

$$\delta_u=\sqrt{\frac{\rho}{\pi\mu_0 u f_{swC}}} \quad (2)$$

$$\varepsilon_u=\left(\frac{\pi}{4}\right)^{0.75}\sqrt{\frac{T_{layer}}{W_W}}\left(\frac{d^{1.5}}{\delta_u}\right) \quad (3)$$

where $F_{uC}(0)$ and $F_{uC}(h)$ are the MMF amplitudes of the u^{th} harmonic at the beginning (x=0) and end (x=h) of a layer, respectively, d is the diameter of the given winding, h is the thickness of a given layer, with the suffix u being the harmonic number [24].

The magnitude $|F_{uC}|$ and phase φ_{uC} of u^{th} harmonic of the MMF during charge process are given by

$$|F_{uC}|=\sqrt{a^2_{uC}+b^2_{uC}} \quad (4)$$

$$\varphi_{uC}=\begin{cases}\tan^{-1}\left(-\frac{b_{uC}}{a_{uC}}\right), & \text{if } a_{uC}\geq 0\\ \pi+\tan^{-1}\left(-\frac{b_{uC}}{a_{uC}}\right), & \text{if } a_{uC}<0\end{cases} \quad (5)$$

$$\Delta\varphi=\varphi_{uC}(0)-\varphi_{uC}(h) \quad (6)$$

where a_{uC} and b_{uC} are the coefficients of the Fourier series of the MMF during charge process and are provided in [24], and $\Delta\varphi$ is the difference between the phase angles of the u^{th}

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harmonic at the beginning (x=0) and end (x=h) of a layer, respectively.

The expression for the winding loss in a flyback transformer at each switching frequency (each switching cycle) index j during charge process is

$$P_{windC}(j) = I^2_{pavgC}(j) R_p + I^2_{savgC}(j) R_s + \sum_{k=1}^{n_{ls}+n_{lp}} P^k_{layerC}(j) \quad (7)$$

The total winding loss during charge process having N_c switching cycles is

$$P_{TwindC} = \sum_{j=1}^{N_c} P_{windC}(j) \quad (8)$$

2) Discussion:

The winding loss during discharge process is calculated similar to that during charge process. The AC loss due to air-gap fringing field [28] has not been considered because of difficulties in interfacing the 2-D/3-D finite element analysis (FEA) simulation results with the optimization process. The negative current at the beginning of the turn-on process during charge process in Fig. 6(a) is due to the high voltage winding self-capacitance. When the secondary winding current becomes zero, the drain to source voltage V_{Mp} tends to decrease. Since the control IC, LT3751 [42] operates under boundary mode control, the next switching cycle starts before the high voltage winding capacitance completely discharges. Hence, the current flows in the reverse direction to discharge the high voltage winding capacitance.

B. Transformer core loss:

The time-average core loss per unit volume P_v due to non-sinusoidal excitation is calculated using the improved generalized Steinmetz equation (*i*GSE) [43] which is given by

$$P_v = \frac{1}{T_s}\left[\int_0^{T_s} k_z \left|\frac{dB(t)}{dt}\right|^{\alpha} (\Delta B)^{\beta-\alpha}\, dt\right] \quad (9)$$

where $\left|\frac{dB(t)}{dt}\right|$ is the absolute value of the change rate of the flux density, ΔB is the peak-to-peak flux density, T_s is the switching period, and k, α and β are the constants provided by the core manufacturer. The core loss coefficient k_z in (9) is calculated using the following expression

$$k_z = \frac{k}{(2\pi)^{\alpha-1} 2^{\beta-\alpha}\left[\int_0^{2\pi} |\cos\theta|^{\alpha} \,\mathrm{d}\theta\right]} \quad (10)$$

The angle θ in (10) represents the phase angle of the sinusoidal excitation. For a given values of k, α and β, the value of coefficient k_z in (10) is fixed, irrespective of shape of the flux density waveform.

The core loss per unit volume using *i*GSE during charge operation (where $\Delta B = B_{mC} + B_{nC}$ during the turn-on period and $\Delta B = B_{mC}$ during the turn-off period), in each switching cycle is given by

$$P_{vC} = \frac{k_z}{T_{sC}}\left[(B_{mC} + B_{nC})^{\beta} \cdot {t_{onC}}^{1-\alpha} + {B_{mC}}^{\beta} \cdot {t_{offC}}^{1-\alpha}\right] \quad (11)$$

Similarly, the core loss per unit volume during discharge operation (where $\Delta B = B_{mD}$), in each switching cycle is given by

$$P_{vD} = \frac{k_z}{T_{sD}} {B_{mD}}^{\beta}\left[{t_{onD}}^{1-\alpha} + {t_{offD}}^{1-\alpha}\right] \quad (12)$$

C. Switching loss due to transformer self-capacitance

The capacitive turn-on or switching loss due the self-capacitance when the converter employs valley switching/boundary conduction mode (BCM) control during charge process is given by [26], [44], [45]

$$P_{swC} = \frac{1}{2}\left(n^2 C_s\right)\left(V_{in} - \frac{V_{out}}{n}\right)^2 f_{swC} \quad (13)$$

When the output voltage V_{out} is greater than nV_{in}, the capacitive switching loss P_{swC} is 0 W, since the converter operates with zero voltage switching (ZVS). The capacitive switching loss due the self-capacitance when the converter employs DCM control during discharge process is [26]

$$P_{swD} = \frac{1}{2} C_s (V_{Ms})^2 f_{swD} \quad (14)$$

In DCM, the drain-to-source voltage V_{Ms} at the beginning of the next switching cycle can be anywhere between $V_{out} + \delta_C n V_{in} + \delta_C V_{leakD}$ and $V_{out} + (2\delta_C - 1) n V_{in} + \delta_C V_{leakD}$. The expression for δ_c is given by [26]

$$\delta_c = \frac{C_{osss}}{C_{osss} + C_{Db}} \quad (15)$$

The output capacitance C_{osss} of M_s and junction capacitance C_{Db} of diode D_b are approximately 15 pF and 1 pF, respectively.

D. Switching loss due to transformer leakage inductance

The loss due to the dissipative RCD snubber during charge process is given by

$$P_{snC} = \frac{1}{2} L_{lkp} I^2_{ppkC} \frac{V_{snC}}{V_{snC} - \frac{V_{out}}{n}} f_{swC} \quad (16)$$

The loss due to the dissipative RCD snubber during discharge process is given by

$$P_{snD} = \frac{1}{2} L_{lks} I^2_{spkD} \frac{V_{snD}}{V_{snD} - nV_{in}} f_{swD} \quad (17)$$

where V_{snC} and V_{snD} are the snubber clamp voltages for low and high voltage MOSFETs, respectively.

E. Remaining losses in the bidirectional flyback converter

The remaining losses in the converter during charge process are: switching loss of M_p, conduction losses of M_p, D_2 and R_{psense}, gate drive loss of M_p, and power consumption of charge control IC. Similarly, the remaining losses in the converter during discharge process are: switching loss of M_s, conduction losses of M_s, D_b and R_{ssense}, gate drive loss of M_s, and power consumption of discharge control IC. Since during both charge and discharge operations the converter employs BCM and DCM control, respectively, there are no diode reverse recovery losses in both modes.

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IV. Efficiency Optimization for a DC-DC Converter Driving Capacitive Load

Efficient design of a high voltage bidirectional flyback converter, necessitates many trade-offs and iterations with a large number of design variables. The first step of the optimization routine is to determine the design specifications of the converter. The low voltage and high voltage MOSFETs, high voltage diode, turns ratio and magnetizing inductance are used as the constraints in the optimization, and are kept constant throughout the optimization routine. The flow chart of the proposed optimization routine is shown in Fig. 7. The converter specifications are used to calculate the number of primary and secondary turns, for a given ferrite core. The outputs of AWL technique are used to calculate the transformer parasitics. The energy losses during both charge E_{lossC} and discharge E_{lossD} modes are calculated and added to represent the total energy loss for that specific core. Finally, the energy efficiencies during charge η_C and discharge η_D modes are calculated as a function of output voltage.

The design decisions presented in Table II are used, to limit the solution space of the optimization routine. The ranges for the cores and parameters to be optimized are shown in Table III. The optimization routine iterates through all design possibilities, and finally presents an optimized (most efficient) solution for each core. The outputs of the AWL technique are represented as O_{AWL}.

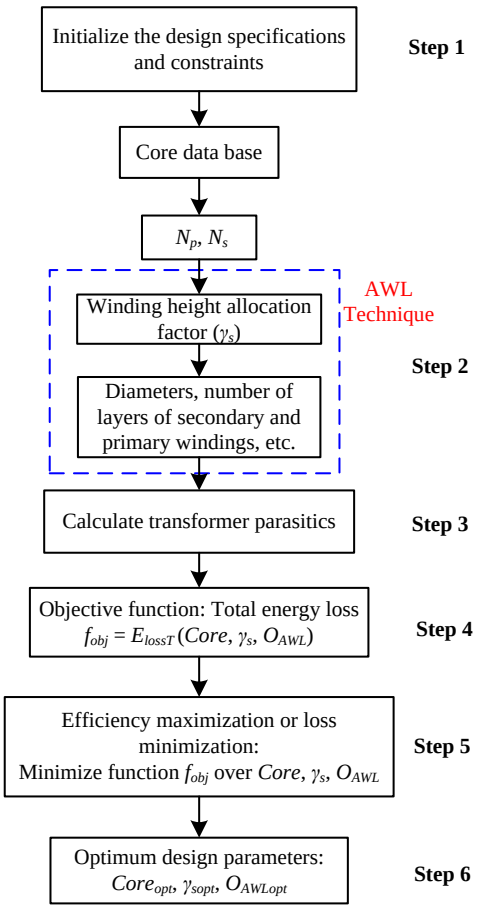

Fig. 7. Flow chart of the proposed efficiency optimization procedure.

TABLE III
Ranges of the Design Parameters

Parameters	Ranges for optimization
Transformer cores	EFD12, EFD 15, EFD 20, EFD 25, E 16, E 20, E 25, E 30, ETD 29, ETD 34, ETD 39, RM 8, RM 10, RM 12, PQ 20/20 and PQ 26/20
Height allocation factors for secondary winding (γ_s)	[0.5, 0.6, 0.7, 0.8]
Outputs from AWL technique O_{AWL}	see Section II and Figure 7

The proposed optimization routine is described in the following steps:

1) Transformer turns ratio, peak currents (for charge and discharge operations), magnetizing inductance are selected from the design specifications and constraints. Number of primary and secondary turns are calculated for a given transformer core.
2) The proposed AWL technique is applied to calculate an array of the outputs (diameter, number of layers, turns per layer, number of parallel wires, for both primary and secondary windings). The condition for the last layer fill factor is FF_{LL}>0.85, this is to approximately make, equal number of turns per layer on final secondary layer and remaining secondary layers).
3) The transformer parasitics are calculated for each set of outputs resulted from AWL technique.
4) The objective function f_{obj} is defined as the sum of the total energy losses in the bidirectional flyback converter over a set of operating points, and is given by
$$f_{obj} = E_{lossT}(Core,\ \gamma_s,\ O_{AWL}) \tag{18}$$
5) The efficiency optimization or loss minimization of function f_{obj} is
$$\min_{Core,\ \gamma_s,\ O_{AWL}}\left[f_{obj}\right] = \min_{Core,\ \gamma_s,\ O_{AWL}}\left[E_{lossT}\right] = \min_{Core,\ \gamma_s,\ O_{AWL}}\left[E_{lossC} + E_{lossD}\right] \tag{19}$$
6) The end results of the optimization routine are the set of parameters which contributes to the minimum total energy loss. Finally, the optimum charge and discharge energy efficiencies are calculated as a function of output voltage
$$\eta_C(V_{out}) = \frac{E_{load}(V_{out})}{E_{load}(V_{out}) + E_{lossC}} = \frac{0.5C_{load}V_{out}^2}{0.5C_{load}V_{out}^2 + E_{lossC}} \tag{20}$$
$$\eta_D(V_{out}) = \frac{E_{load}(V_{out}) - E_{lossD}}{E_{load}(V_{out})} = \frac{0.5C_{load}V_{out}^2 - E_{lossD}}{0.5C_{load}V_{out}^2} \tag{21}$$

V. Efficiency Optimization Results and Experimental Validation

A. *Details of the optimization results:*

The components used in the bidirectional flyback converter except the transformer are shown in Table IV. All losses in the bidirectional flyback converter are calculated in MATLAB

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TABLE IV
COMPONENTS USED IN THE BIDIRECTIONAL FLYBACK CONVERTER

Component	Name / Manufacturer
Low voltage MOSFET M_p	IPB600N25N3 G [250 V, 25 A, 60 mΩ]
High voltage MOSFET M_s	IXTV03N400S [4 kV, 300 mA, 290 Ω]
High voltage diode D_2 or D_b	SP5LFG [5 kV, 400 mA, 50 ns (t_{rr})]
Film capacitive load C_{load}	WIMA [400 nF, 3 kV]
Analog control IC	LT3751

using the proposed comprehensive loss model. The winding loss is calculated during both charge and discharge processes, up to 100th order harmonics (N_h=100). The optimum secondary height allocation factor γ_s, for each core is provided in Fig. 8. Figure 9 provides the results of the optimum charge, discharge and overall (product of charge and discharge) energy efficiencies, and an overall energy efficiency of a typical design where 50% space is allocated for primary and secondary windings, at an output voltage of 2.5 kV, with respect to different core volumes.

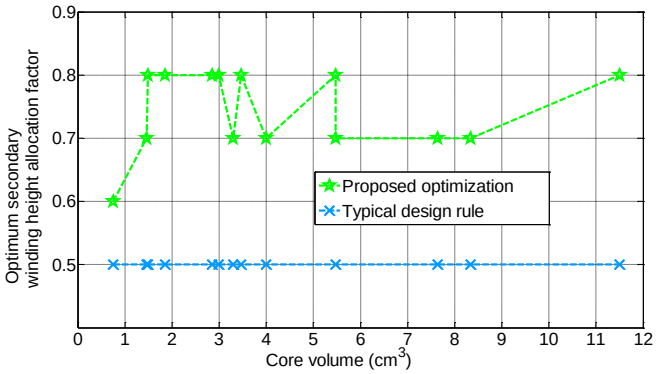

Fig. 8. Optimum secondary winding height allocation factor γ_s vs. core volume.

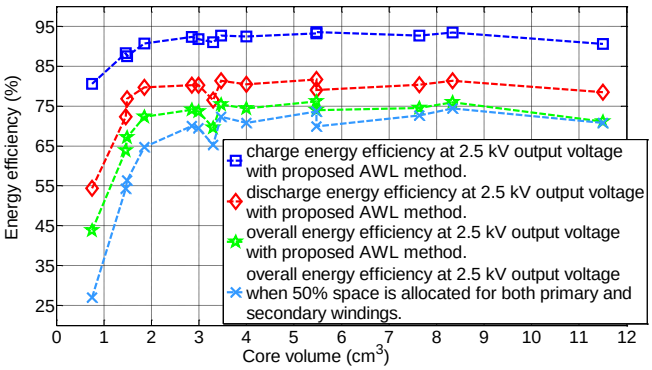

Fig. 9. Calculated optimized energy efficiencies at an output voltage of 2.5 kV vs. core volume. The sequence of the 14 cores is: [E 16, EFD 20, E 20, RM 8, PQ 20/20, E 25, EFD 25, RM 10, E 30, PQ 26/20, ETD 29, ETD 34, RM 12, ETD 39].

The total energy loss E_{lossC} at an output voltage of 2.5 kV is the loss occurred in all components of the converter, for charging the capacitive load from 0 V to 2.5 kV. Similarly, the total energy loss E_{lossD} at an output voltage of 2.5 kV is the loss occurred in all components of the converter, for discharging the capacitive load from 2.5 kV to 0 V. The most efficient and smallest transformer (or core) designs are two important outcomes of the proposed efficiency optimization routine. Table V shows a comparison of smallest core (SCD) and optimized core (OCD) designs.

The smallest and optimized core designs are described below:

1) Smallest core design (SCD)

The smallest core is selected as the core whose temperature rise is less than the maximum temperature limit (130 °C). Several small cores such as, EFD 12, EFD 15, E 16 have been used in the optimization routine, out of those E 16 is the smallest core with a maximum temperature rise of 94 °C (in a single bidirectional charge and discharge cycle). In the optimization routine, for all small cores (EFD 12, EFD 15, E 16), a maximum flux density of 0.33 T is chosen, hence for E 16, N_p becomes 29. As shown in Fig. 8, the optimum secondary height allocation factor for E 16 core is 0.6, this is for accommodating the 29 primary turns on the small core. The spacing between the secondary winding layers for SCD is 66 μm.

2) Optimized core design (OCD)

The core, which has a lower volume and a better overall energy efficiency compared with other cores, is selected as an optimized core. In Fig. 9, most of the cores whose volumes are above 2.85 cm^3 have an overall energy efficiency between 74% and 76%. The EFD 25 core with volume 3.3 cm^3 has a lower discharge efficiency (hence lower overall efficiency), since its window height H_W has been less compared with the neighboring cores, such as the EF 25 and RM 10 (see Fig. 9). For a better trade-off between the core volume and overall efficiency, the cores whose volume is between 2.85 and 4 cm^3 could be more suitable for the high voltage driver (with specifications shown in Table I). The cores with volumes 4 cm^3 (E 30) and 2.85 cm^3 (PQ 20/20) have overall efficiencies of 75% and 74%, respectively. However, PQ 20/20 core is selected as an optimized core, as a 40% increase in the core volume provides only 1% increase in the overall energy efficiency. In the optimization routine, a maximum flux density of 0.26 T is chosen for all cores whose volumes are greater than equal to 1.46 cm^3 (EFD 20). As shown in Fig. 8, for all cores except the smallest core, the optimum secondary winding height allocation factor varies between 0.7 and 0.8. For PQ 20/20 core, the secondary height allocation factor is 0.8. The spacing between the secondary winding layers for OCD is 0.9 mm.

The energy loss distributions for PQ 20/20 core during charge and discharge processes are shown in Figs. 10(a) and 10(b), respectively. During charge process, the converter operates with boundary conduction mode (BCM) control; hence the capacitive switching loss due to the self-capacitance is very low compared with other losses. The significant losses during charge process are: switching loss of low voltage MOSFET M_p, switching loss/snubber loss due to the transformer leakage inductance and transformer winding loss. During discharge process, the converter operates with discontinuous conduction mode (DCM) control; hence the capacitive switching loss due to the self-capacitance cannot be

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TABLE V
RESULTS OF THE OPTIMIZATION FOR SMALLEST CORE DESIGN (SCD) AND OPTIMIZED CORE DESIGN (OCD)

Parameter	SCD	OCD
Core name	E 16	PQ 20/20
Core volume	0.75 cm^3	2.85 cm^3
Maximum flux density B_{mC}	0.33 T	0.26 T
Total number of turns of primary N_p / secondary N_s winding	29 / 720	12 / 300
Number of layers of primary n_{lp} / secondary n_{ls}	2 / 8	1 / 4
Number of parallel wires (or squares) of primary n_{parp} / secondary n_{pars}	1 / 1	1 / 1
Number of turns (or squares) per layer of primary / secondary	15 / 90	12 / 75
Diameter of primary d_p / secondary winding d_s	0.4 mm / 0.1 mm	(0.5+0.2) mm / 0.143 mm
Primary magnetizing inductance L_{mp}	40 μH	44 μH
Height allocation for secondary winding γ_s	0.6	0.8
Spacing (or insulation) between secondary layers $d_{insulation}$	66 μm	0.9 mm
Transformer maximum temperature rise in a single bidirectional charge and discharge cycle	94 °C	30 °C

neglected. The significant losses during discharge process are: switching loss of high voltage MOSFET M_s, switching loss due to the transformer leakage inductance, and capacitive switching loss due to the transformer self-capacitance.

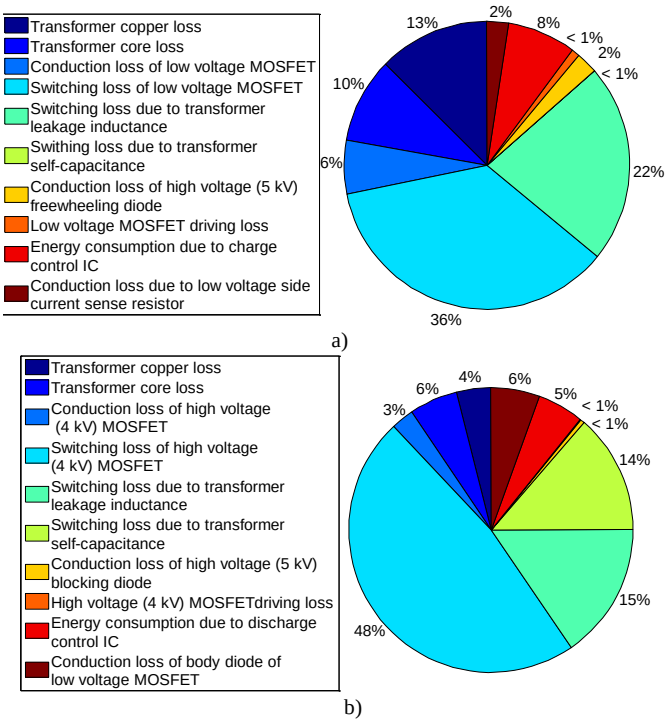

Fig. 10. Energy loss distribution of the optimized core (PQ 20/20), a) during charge and b) during discharge process.

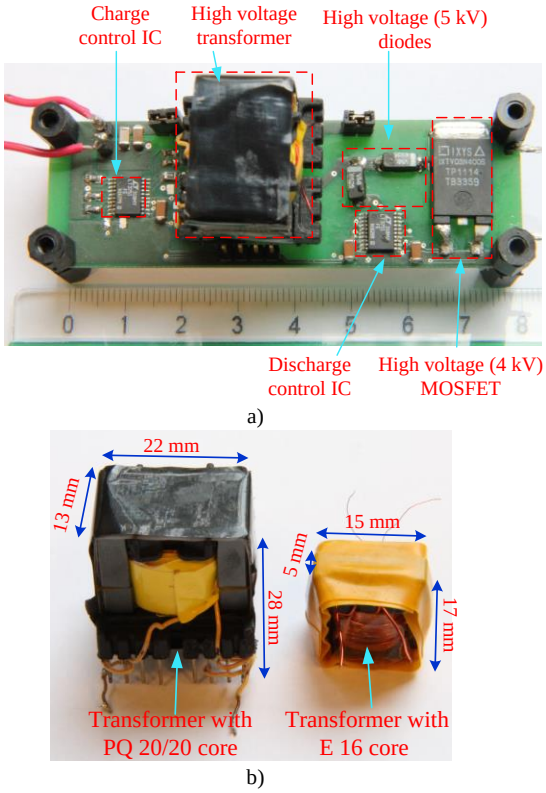

Fig. 11. a) Experimental prototype of the bidirectional flyback converter with PQ 20/20 core; b) Optimized (PQ 20/20) and smallest (E 16) transformers.

B. *Experimental Results*

The experimental prototype of the bidirectional flyback converter is shown in Fig. 11(a). The prototypes of optimized and smallest transformers are shown in Fig. 11(b). The comparison of measured [19] and calculated charge and discharge energy efficiencies for the smallest and optimized cores is provided in Figs. 12(a) and 12(b), respectively. In Figs. 12(a) and 12(b), the maximum difference between the calculated and measured energy efficiencies during charge and discharge modes is less than ±5%, except for the smallest core design at very high output voltage (>2.2 kV). The total loss due to the transformer parasitics for SCD is higher than that of OCD by 5 times, and the remaining losses in the converter, are the same for both designs.

In the bidirectional flyback converter an input capacitance C_{in} of 1800 μF (100 V) is used. The primary R_{psense} and secondary R_{ssense} sense resistors used in the converter are 25 mΩ and 0.5 Ω, respectively. The Z-type winding scheme [25] is implemented in the secondary winding of the flyback transformer, to reduce the self-capacitance. To remove the interlayer insulation tape between primary and secondary windings, triple insulated wire (TEX-E) from Furukawa [46]

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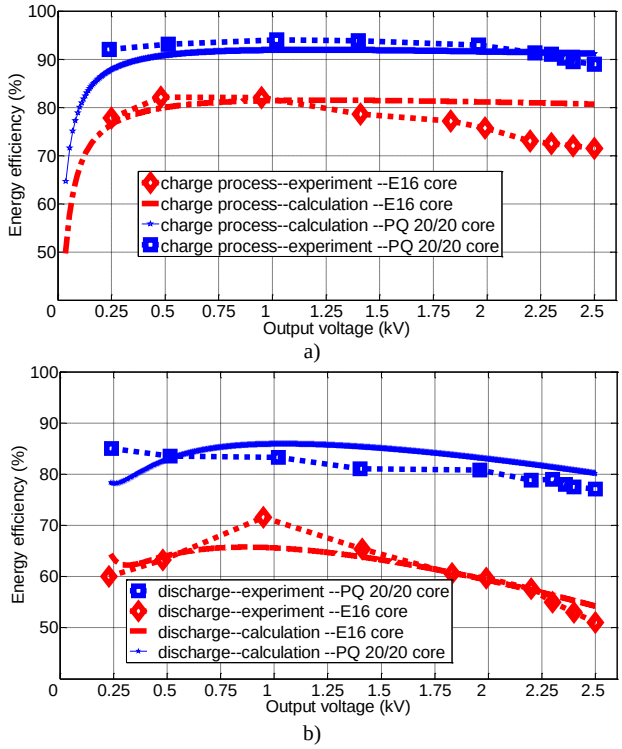

Fig. 12. Comparison of calculated and measured a) charge and b) discharge energy efficiencies for the optimized (PQ 20/20) and smallest (E 16) cores.

is used for the primary winding, and it has an insulation thickness of 0.2 mm. As shown in Table VI, 0.7 mm overall diameter wire (0.5 mm TEX-E wire) is used in the primary winding of PQ 20/20 core, and 0.4 mm overall diameter normal single insulated wire is used in the primary winding of E 16 core, due to non-availability of 0.2 mm TEX-E wire during practical implementation.

For PQ 20/20 core, no snubber is used in either low voltage or high voltage side. Since the leakage inductance of E 16 core is very high, RCD snubbers are used in both primary and secondary sides and the loss model is updated accordingly. The loss model automatically considers RCD snubbers, when the leakage inductance L_{lkp} in the optimization is higher than 1.2 μH. The low voltage V_{snC} and high voltage V_{snD} RCD snubber clamp voltages are chosen as $\frac{2V_{out,max}}{n}$ and $2nV_{in}$, respectively, with a maximum output voltage $V_{out,max}$ of 2.5 kV. The insulation between the secondary layers of transformer is provided by the Kapton tape which has a single layer thickness of 66 μm. The calculated and measured transformer parasitics for both SCD and OCD are provided in Table VI. The comparison shows that the model used for calculating the parasitics, for multiple solutions in the optimization routine is accurate enough.

TABLE VI
COMPARISON OF CALCULATED AND MEASURED TRANSFORMER PARAMETERS FOR SMALLEST AND OPTIMIZED CORE DESIGNS

Parameter of Transformer	SCD		OCD	
	Calculation	Measurement	Calculation	Measurement
Leakage inductance referred to primary L_{lkp}	3.22 μH	3.3 μH	818 nH	857 nH
Self-capacitance of secondary (high voltage) winding C_s	18.1 pF	21.62 pF	4.5 pF	6.23 pF
Dc resistance of secondary (high voltage) winding R_s	46.54 Ω	44 Ω	15.3 Ω	18.2 Ω

VI. CONCLUSIONS

This paper presents an efficiency optimization approach for a high voltage bidirectional flyback dc–dc converter. The energy efficiency is optimized using a proposed new automatic winding layout generator technique and a comprehensive loss model. The proposed optimization technique is experimentally validated on a 25 W (charging power) high voltage bidirectional flyback converter. The measured charge and discharge energy efficiencies of the converter, with PQ 20/20 core at an output voltage of 2.5 kV are 89% and 77.1%, respectively. For both optimized and smallest core designs, energy efficiency during discharge process is less compared to that during charge process, mostly due to the switching loss of the output capacitance of high voltage MOSFET.

The important conclusions of this paper are as follows:

1) The proposed AWL technique is highly recommended for high input or high output voltage applications which need a transformer with many turns (primary or secondary). It automatically calculates and provides the necessary winding design data such as wire sizes, number of winding layers, number of turns per layer, and the number of parallel wires.
2) The AWL technique can be easily extended to interleaved and/or sectioned transformer structures.
3) Transformer parasitics are calculated for each set of outputs from AWL technique, which are needed to estimate the energy efficiency. By iteratively changing the spacing between secondary winding layers, the loss due to self-capacitance, leakage inductance and dc resistance of the transformer are balanced.
4) Providing a very thick insulating tape between the secondary winding layers reduces the self-capacitance. The self-capacitance can be reduced significantly by allocating more space (or height) for the secondary winding.
5) Non-sectioned bobbins with larger window height are suitable for minimizing the self-capacitance, hence are recommended for high voltage capacitor charge and discharge application.
6) The output of the proposed efficiency optimization (overall energy efficiency vs. core volume curve) gives the flexibility for the designer to choose the necessary core and winding configurations.

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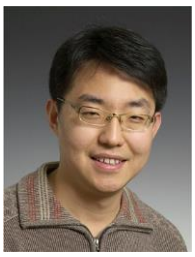
Prasanth Thummala (S'11) was born in India in 1987. He received the B.Tech. degree in electrical and electronics engineering from Acharya Nagarjuna University, Guntur, India, in 2008, and the M.Tech degree in control systems engineering, at the department of electrical engineering, from the Indian Institute of Technology Kharagpur, Kharagpur, India, in 2010. He was a Ph.D. student in the electronics group, department of electrical engineering, Technical University of Denmark (DTU), Denmark, from Nov. 2011 to Nov. 2014.

From Sept. 2013 to Jan. 2014, he was a Visiting PhD student in Colorado Power Electronics Center (CoPEC), at the University of Colorado Boulder, Boulder, CO, USA. He received the first prize UTRC best student paper award at the IEEE ECCE USA conference held in Denver, CO, USA, 2013. His research interests include modeling and control of power electronic converters, high-voltage switch-mode power converters for driving capacitive loads, magnetic design, digital control and system identification.

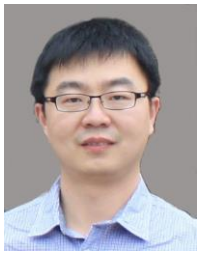
Henrik Schneider (S'11) was born in Denmark and received a master's degree in electrical engineering from the Technical University of Denmark in 2009. The following two years he worked as an R&D engineer within power electronics.

In 2011 he was enrolled as a Ph.D. at the Technical University of Denmark with a focus on switch mode power supplies and audio amplifiers. He received the best paper award at the IEEE ECCE Asia conference held in Melbourne, Australia, 2013 and a best presentation award at the IEEE APEC conference in Dallas, USA, 2014. His research interests include, efficiency and power density optimization of power electronics, audio system integration, magnetic design and finite element modeling.



Zhe Zhang (S'07, M'11) received the B.Sc. and M.Sc. degrees in power electronics from Yanshan University, Qinhuangdao, China, in 2002 and 2005, respectively, and the Ph.D. degree from the Technical University of Denmark, Kgs. Lyngby, Denmark, in 2010.

He is currently an Associate Professor with the Department of Electrical Engineering, at the Technical University of Denmark. From 2005 to 2007, he was an Assistant Professor with Yanshan University. From June 2010 to August 2010, he was with the University of California, Irvine, CA, USA, as a visiting scholar. He was a Postdoctoral Researcher and Assistant Professor at the Technical University of Denmark between 2011 and 2014. He has authored or co-authored more than 70 transactions and conference papers. His current research interests include DC/DC converters, multiple-input converters, and multi-level inverters for renewable energy systems (RES), hybrid electric vehicles (HEV) and uninterruptable power supplies (UPS).



Ziwei Ouyang (S'07, M'11) received the B.S degree in electrical engineering from the Naval University of Engineering, Wuhan, China, in 2004, the M.S degree from the Tianjin University of Technology, Tianjin, China, in 2007, and the Ph.D. degree from the Technical University of Denmark (DTU), Denmark, in 2011. He worked as a Postdoctoral Researcher at DTU from 2011 to 2013 and is currently assistant professor in the Department of Electrical Engineering at DTU.

His current research interests include advanced magnetics design, modeling and integration in switch mode power supplies, dc/dc converters, and digital control in high-power reversible converters. He has over 30 peer-reviewed journal and conference publications and currently he is the holder of three US/EP/PCT patents. He received the Young Engineer Award at PCIM Asia 2014 and Best Paper Awards in ECCE-Asia conferences in 2010 and 2012, respectively. He is a member of the IEEE PELS, IES and Magnetics societies.

Arnold Knott (M'10) received the Diplom-Ingenieur (FH) degree from the University of Applied Sciences in Deggendorf, Germany, in 2004. From 2004 until 2009 he has been working with Harman/Becker Automotive Systems GmbH in Germany and USA, designing switch-mode audio power amplifiers and power supplies for automotive applications.

In 2010 he earned the Ph.D. degree from the Technical University of Denmark, Kongens Lyngby, Denmark working on a research project under the title "Improvement of out-of-band Behaviour in Switch-Mode Amplifiers and Power Supplies by their Modulation Topology". From 2010 to 2013 he was Assistant Professor and since 2013 Associate Professor at the Technical University of Denmark. His interests include switch-mode audio power amplifiers, power supplies, active and passive components, integrated circuit design, acoustics, radio frequency electronics, electromagnetic compatibility and communication systems.

Michael A. E. Andersen (M'88) received the M.Sc.E.E. and Ph.D. degrees in power electronics from the Technical University of Denmark, Kgs. Lyngby, Denmark, in 1987 and 1990, respectively. He is currently a Professor in power electronics and head of the Electronics group at the Technical University of Denmark (DTU). Since 2009 he has been the Deputy Head of the Department at the Department of Electrical Engineering, Technical University of Denmark.

He received the best poster prize in UPEC 1991 conference. He has authored and co-authored more than 280 publications. From 2010, he is serving as an Associate Editor of IEEE Transactions on Power Electronics. His research areas include switch mode power supplies, piezoelectric transformers, power factor correction, and switch mode audio power amplifiers.