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Characterising the CMOS Image Sensor for the JANUS Camera on ESA's JUICE Mission to Jupiter

by Daniel-Dee Lofthouse-Smith

Thesis Submitted in Partial Fulfilment of the Requirements for the Degree of Doctor of Philosophy

in the

Centre for Electronic Imaging School of Physical Sciences

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Abstract

The subject of this thesis is the characterisation of a scientific Complementary Metal Oxide Semiconductor (CMOS) image sensor to be used on the JANUS camera on ESA's JUICE mission to Jupiter.

The first part of this thesis investigates the initial characteristics of the device to better understand how changes in these characteristics manifest themselves over a range of tests.

Initially, following total ionising dose and displacement damage, an increase in the dark current is observed. At temperatures above room temperature, it is theorised that the dark current is proportional to the exponent of the band gap of silicon. Following thermal annealing of these irradiated devices a slight recovery in the average dark current is noticed, which can be credited to the annealing of some radiation induced defects.

The second part of this work investigates how image lag manifests in the image sensor, where a transitionary point to high level image lag is observed, referred to as the image lag 'knee-point'. The signal that this knee point occurs is studied with varying total ionising dose and transfer gate voltages, allowing the cause to be hypothesised and an optimum operating condition to be recommended.

The image lag is also investigated on a pixel-by-pixel basis, which is a novel approach compared to the typical average level across the whole image sensor. Measurements with devices exposed to total non-ionising doses demonstrate the creation of a population of pixels that exhibit higher levels of image lag than average, an effect that has been attributed to displacement damage in the image sensor.

Declaration

I hereby declare that no part of this thesis has been previously submitted to this or any other university as part of any other degree or professional qualification. This thesis has been wholly written by the undersigned, except for colleagues and others acknowledged in the text.

Daniel-Dee Lofthouse-Smith

2021

Dedic	ation
	This thesis is dedicated to my family, Christina, and my late Grandfather Fred

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List of Acronyms

3T / 4T 3-Transistor / 4-Transistor

APS Active Pixel Sensor
BI Back Illuminated
BOL Beginning Of Life

CCD Charged Coupled DeviceCDS Correlated Double SamplingCEI Centre for Electronic Imaging

CIS CMOS Image Sensor

CMOS Complementary Metal Oxide Semiconductor

CTI Charge Transfer Inefficiency
CVF Charge to Voltage Factor

DC Dark Current
DN Digital Numbers

DSNU Dark Signal Non-Uniformity **EFWC** Equilibrium Full Well Capacity

e-h pairs Electron-hole pairs
EM Electromagnetic
EOL End Of Life

ESA European Space Agency

eV Electron Volt

FBVS Flat Band Voltage Shift **FD** Floating Diffusion

FF Fill Factor

FI Front Illuminated FM Flight Model

FPN Fixed Pattern Noise

ISE-TCAD Integrated Systems Engineering Technology Computer Aided Design

JANUS Jovis Amorum ac Natorum Undique Scurtator

JUICE JUpiter Icy moons Explorer

KE Kinetic Energy

MOS Metal Oxide Semiconductor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

NASA North American Space Agency
NIEL Non-Ionising Energy loss

NIR Near Infra-Red
OU Open University
PD Photodiode

PMD Pre-Metal Dielectric PPD Pinned Photodiode

PRNU Pixel Response Non-Uniformity

PTC Photon Transfer Curve
QE Quantum Efficiency
RTS Random Telegraph Signal

SEE Single Event Effect

SEFI Single Event Function Interruption

SEL Single Event Latch up
 SEU Single Event Upset
 SF Source Follower
 SRH Shockley-Read-Hall
 STI Shallow Trench Isolation

SW Storage Well

TG Transfer Gate
TID Total Ionising Dose
TNID Total Non-Ionising Dose
VTS Visual Telemetry System

Chapter 1: Introduction

1.1 Context

The JUpiter ICy moon Explorer (JUICE) mission is a European Space Agency (ESA) Large-class mission destined for the Jovian system with a scheduled arrival of 2030 following a 2022 launch. The mission will be used to address some of ESA's wider "cosmic vision" themes, where characterisation of the Jovian system will be carried out by a host of instruments.

One such instrument is the Jovis Amorum ac Natorum Undique Scrutator (JANUS) optical camera system that will be used to study the Galilean moons of Jupiter alongside mapping of the Jovian atmosphere. Due to the requirements on the detector for high-speed readout, high resolution, and high radiation hardness the logical option for the JANUS camera was thought to be a Complementary Metal Oxide Semiconductor (CMOS) Imaging Sensor (CIS). The detector that is the subject of the research element of this thesis is the CIS115, a 4-Transistor (4T) CIS fabricated by Teledyne e2v. To ensure that the JANUS camera will perform suitably for the mission means that a detailed study into the performance of the image sensor is required. This is done at beginning of life (BOL) and following irradiation during transit to the Jovian system and during science operations.

1.2 Aims

This thesis aims to characterise key performance metrics of the CIS115 and in doing so help to understand how well the CIS115 can expect to operate at the start, during and at the end of the mission lifetime in key electro-optical parameters. This thesis describes some of these factors in greater detail with focus on the image lag and dark current of the device, key factors when considering the need for high quality images output from the sensor.

As the CIS115 has not been previously flown on a space mission at time of writing, this thesis can also be used as a precursor of how well one can expect a device to respond to Total Non-Ionising Doses (TNID) and Total Ionising Doses (TID). This may lead to the use of the CIS115 in other space instruments in the future.

1.3 Thesis organisation

This thesis is organised into a total of 10 chapters, with Chapter 1 forming the introduction of this work. Chapter 2 provides details on the history of solid-state imagers, the main features of Active Pixel Sensors (APS) where interest is paid to the 4-Transistor (4T) variant. The chapter summarises key electro-optical performance metrics for these devices which characterise an imager's performance.

Following on from what is contained in Chapter 2, Chapter 3 builds on this by investigating how these key operational components of APS can become damaged following a host of irradiative sources culminating in explanations of how this is thought to affect the electro-optical performance of these imagers.

Chapter 4 describes the European Space Agency's (ESA) Jupiter Icy Moons Explorer (JUICE) mission where a more detailed explanation is given for the JANUS instrument on JUICE which is an optical camera system using a 4T Teledyne e2v CMOS Image Sensor (CIS). This chapter introduces and explains this sensor, the CIS115, which is investigated during this thesis, with details on the expected performance of the device for the mission. This chapter ends by specifying the expected amount of radiation to be accumulated by the device during the mission phase.

Chapter 5 describes the equipment and experimental procedures that are used in the characterisation of the CIS115. Here key experimental methods like image lag and dark signal data acquisition are introduced alongside radiation testing procedures used for the device. In addition to this, chapter 5 also introduces a key part of this doctoral work: the creation and planning of a Total Ionising Dose (TID) irradiation campaign.

Chapter 6 introduces the initial testing and characterisation of key electro-optical performance characteristics of the CIS115. The works in this chapter form a baseline for the performance of the CIS115 to be able to succinctly compare the results here to others following a range of varied testing.

Chapter 7 outlines a detailed investigation into the dark current performance of the CIS115. The first section characterises the dark current and activation energy performance of beginning of life (BOL) devices used in this study. Following that, the chapter investigates the dark current response following total non-ionising dose (TNID) and TID including a study on

some of the damage sites causing this dark current increase using a dark current spectroscopy technique.

Chapter 8 describes an investigation into the image lag of the CIS115. The first section investigates current research into image lag following radiation effects and image lag reduction studies. Following this, discharging lag at BOL is investigated where features of the image lag performance of the detector is obtained. The next section explores the image lag response from the device following TNID and TID. The chapter concludes by studying the change in image lag whilst varying key device voltages culminating in recommendations for the JANUS camera on JUICE.

Chapter 9 describes a novel pixel by pixel image lag characterisation on the CIS115, where key features that have been seen in the mean image lag response of the CIS115 are studied using data obtained at BOL and following ionising and non-ionising radiation. This chapter concludes with the significance of this investigation for the JANUS camera and the direction that further work in this field can go.

Chapter 10 summarises the key findings of this thesis and describes the implications of this work for the JANUS camera on JUICE. Outstanding issues of this work are offered and are concluded to be points for further research following on from this thesis.

1.4 Publications arising from this study

During the completion of this thesis, two first author papers were published. The first paper investigated the dark current response of the CIS115 and some of the results from it are included in chapter 7 of the thesis. The second investigated the image lag response of the CIS115, where some of the results from that paper are included in chapter 8 of this thesis.

Lofthouse-Smith, D. D., Soman, M. R., Allanwood, E. A. H., Stefanov, K. D., Holland, A. D., Leese, M., & Turner, P. (2018). Thermal annealing response following irradiation of a CMOS imager for the JUICE JANUS instrument. *Journal of Instrumentation*, *13*(03), C03036.

Lofthouse-Smith, D. D., Soman, M. R., Allanwood, E. A. H., Stefanov, K. D., Holland, A. D., Leese, M., & Turner, P. (2018, July). Image lag optimisation in a 4T CIS image sensor for the JANUS camera on ESA's JUICE mission to Jupiter. In *High Energy, Optical, and Infrared Detectors for*

Astronomy VIII (Vol. 10709, p. 107091J). International Society for Optics and Photonics.

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Chapter 2: Solid State Imagers for Space

2.1 Semiconductor imager origins

Semiconductor imagers are used in place of film in a range of cameras, including microscopes, telescopes, scanners etc. This chapter identifies and explains the operational mechanisms and structures found in semiconductor imagers. Most detail in this chapter will focus on one type of silicon imager: the Complementary Metal Oxide Semiconductor (CMOS) Image Sensor, with attention paid to its Four-Transistor (4T) variant. In addition, this chapter discusses the key electro optical metrics that typically govern the performance of these CMOS Image Sensors (CIS).

Semiconductor imagers rely on the conversion of light to electronic signals via the photoelectric effect due to their inherent light sensitivity (Noble 1968). Semiconductor sensors that were first developed using semiconductor light sensitivity were known as "Scanistors" (Horton, Mazza, and Dym 1964) with output signal proportional to the local incident light intensity. These sensors did not perform any sort of integration on the optical signal, resulting in low light sensitivity, and did not offer good performance as scientific imagers. However, Weckler et al. (Weckler 1967) operated a semiconductor structure (p-n junction, see 2.3.1) in photon flux integration mode where illumination in this region can be related to the voltage in this semiconductor structure resulting in a proportionality between the change in voltage in this region and the illumination in a given time period. This discovery formed the basis of modern scientific Active Pixel Sensors (APS) which will be discussed in further detail in the rest of this chapter.

2.1.1 Charged Coupled Device (CCD)

Shortly after the discovery of APS technology, the Charge-Couple-Device (CCD) was proposed by Boyle and Smith in the late 1960's (Boyle and Smith 1970) and was fabricated to primarily operate as memory storage. However, since the structure is sensitive to light, its use as an imager was studied. This finding culminated in the discovery of three phase CCDs, which were fabricated, tested and first documented in Tompsett et al. 1971.

Modern CCDs are constructed using an array of Metal Oxide Semiconductor (MOS) capacitors separated by a doped or undoped region known as "channel stops". Charge can be accumulated and stored in the depletion region of these MOS capacitors.

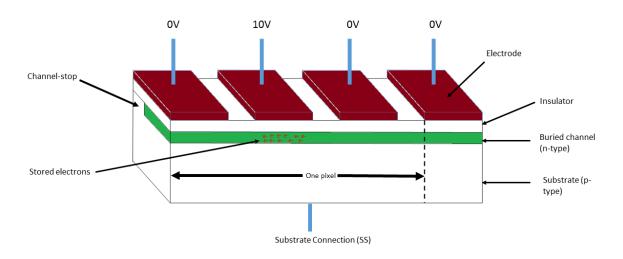


Figure 2-1: Cross section of a three-phase CCD pixel where charge is stored under the pixel region with the highest potential. Sequential change of voltage on the gate attached to the electrode will transfer charge across the device (adapted from Dryer, 2013).

Three-phase devices operate through the transfer of charge via the change of potential in adjacent MOS capacitor regions. Figure 2-1 shows a cross section of a basic three phase CCD pixel. During charge collection one or two of these electrodes is held at a higher potential than the other two. The collected charge packet can be transferred by sequentially moving the potential minimum (Early 1974) to be read out in a section of the CCD known as the readout register, producing a recorded image.

In the early stages of the work following from Weckler et al. (Weckler 1967) which introduced the APS, the CCD (due to the ability to obtain improved images compared to their APS counterparts) was a favourable option as a scientific imager compared to CMOS APS through most of the 1970s and 1980s. However, in the early 1990s, research into CMOS APS increased due to a shift in imager requirements to low cost, low power miniature imaging systems. The increased level of research led to the development of APS with performance comparable to their CCD counterparts in particular applications. These newer versions of APS will be discussed in the following section.

2.1.2 Complementary Metal Oxide Semiconductor (CMOS) Imager

Modern scientific-quality CMOS Image Sensors (CIS) are commonly known as Active Pixel Sensors (APS) due to fact that each pixel has a photodetector and an active amplifier. This circuitry involves a complex method of light collection and requires a minimum of three transistors (3T) for light to voltage conversion and repeated readout of the pixel. Each pixel in an APS possesses its own individual circuit for readout compared to column and row readout in their CCD counterparts.

As discussed previously, as the research in CMOS APS began to increase in the early 1990s, they began to become a more and more favourable image sensor for scientific imagers. Due to the exponential shrinkage of the feature size in integrated circuits as described by Gordon Moore (Moore 1998), CMOS APS performance (in read noise, dynamic range, responsivity for example) became comparable to CCDs. These CMOS APS became more favourable to CCDs in the fields of high-end space applications, where the low power requirement was invaluable e.g., in NASA's Deep Space 1 mission (Bai et al. 2004). The next section will look to further describe CMOS APS/CCDs that have been used in early space applications.

2.2 Technologies used for Imaging in space: A brief history

Research into space imaging is typically driven by the scientific needs of the missions, and from these requirements, the most suitable detectors are selected for use on a mission. Other factors that are key in driving space imaging research includes the cost of the device itself, the time scale for development and the space mission heritage of the device too.

2.2.1 Early space imaging

Some of the earliest images taken in space arose from the Soviet LUNA 3 spacecraft, where in 1959 it returned the first images of the "dark" side of the moon (Lissauer and De Pater 2013) albeit with high noise and low resolution. LUNA 3 transmitted images taken in space back to Earth using the "Yenisey-2 Phototelevision System" (Huntress and Marov 2011). This system scanned images taken on a 35 mm film developed inside the spacecraft and transmitted the digitised images back to Earth via radio waves using a television system. Using a CCD however means that there is no reliance on the development of film to transmit any images.

2.2.2 CCDs in space

CCD cameras showed great promise as scientific astronomical imagers and were first used in scientific imaging experiments as early as 1979, where a CCD was used in the Kitt Peak National Observatory telescope for astronomical imaging (McGuire 1983).

In 1991 the Nikon NASA F4 HERCULES (Hand-held Earth-oriented Real-time Cooperative, User-friendly Location, targeting and Environmental) system was flown on shuttle mission STS-48 (and on some others that year) and was used to image the Earth through the shuttle window. The benefit of using a CCD in this instance means it removed the long delay between taking photos and processing them for distribution where they do not rely on film whilst processing. These CCDs also profit from high dynamic range, large full well capacity (the pixels' ability to store charge) which amongst other factors make it almost perfect as an astronomical imager.

2.2.3 CMOS / APS in space

During its infancy, CIS development was largely abandoned in favour of CCDs in the 1970s and 1980s because of their high Fixed Pattern Noise (FPN) and temporal noise compared to their CCD counterparts. Therefore, CIS were not used in scientific experiments until as late as 1997, with the launch of the visual telemetry system (VTS) on the TEAMSAT mission. It consisted of a 512x512 pixel APS, used for monitoring of spacecraft activities.

2.3 Semiconductor Imager Structures

CCD and CIS gain their functionality through the combination of a range of semiconductor structures. These structures have some similarities across CIS and CCDs where this section will predominantly focus on the structures (and the physics behind them) related to CIS although some overlap is expected.

2.3.1 p-n Junction

CMOS APS make use of a combination of the p-n/n-p-n junction which is used to convert light into electronic signals (Titus, Cheung, and Chodavarapu 2011) via the photoelectric effect (see 2.4.1). Essentially a p-n junction is a two terminal device formed from the combination of a p-type region with a given ionised acceptor concentration (N_a) and an n-type region with a given donor concentration (N_d). The p-doped region has an excess number of holes given

by the acceptor concentration and conversely the n-doped region has an excess number of electrons given by the donor concentration. The combination of these two regions into a device with an abrupt change is shown in Figure 2-2 and is known as an ideal abrupt p-n junction (Dalven 2012).

When a p and n-type semiconductor are brought together the concentration gradient causes the diffusion of both electrons and holes to the p-type and n-type, respectively. When these electrons and holes diffuse across the junction, they can recombine in a region close to the junction removing the free majority carriers from the respective p and n-type side to a given depth. These positive and negative space charge regions form what is known as the "depletion layer" in p-n junctions due to it becoming free of mobile carriers.

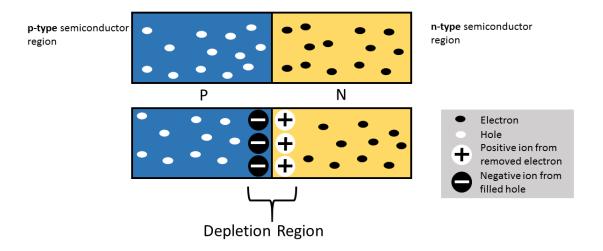


Figure 2-2: Schematic of a p-n junction diode before and after the formation of the depletion region occurring when the p and n regions are brought into contact via the recombination of the majority carriers in the p and n regions, respectively.

The positive and negative space charge regions create an electric field in the structure directed from the n-type region toward the p-type region. This electric field hinders the further diffusion of electrons out of the n-type side and of holes out of the p-type side, which is known as the equilibrium condition. An external voltage source (power supply) can be connected to a p-n junction to alter the equilibrium condition of the p-n junction diode. The device can be operated in either "forward bias" or "reverse bias". These conditions refer to the bias voltage applied to the p-n junction diode, with a positive voltage applied to the p terminal of the device (forward bias) supplying the electrons occupying the depletion region enough energy to overcome the coulomb barrier and flow in the forward direction (right to

left in Figure 2-2), decreasing the size of the depletion region. A negative voltage applied will do the opposite, resulting in the device operating in reverse bias. In this mode, electron flow across the junction becomes inhibited and the width of the depletion region increases.

2.3.2 Pinned Photodiode

The Pinned Photodiode (PPD) is a type of photodetector that is implemented in 4T CIS. Essentially it is a normal p-n junction with an additional p+ layer on the top. The modern PPD was used in over $2x10^{16}$ pixels in 2013 (Fossum and Hondongwa 2014) and strongly resembles the PPD in the interline transfer CCD where this structure is shown for the first time in Teranishi et al. 1984.

The PPD is shown in Figure 2-3 and can be thought of as a bipolar pnp device with the main elements being a highly doped n-type signal charge storage well (SW) enclosed between a lower p-type epitaxial and a p+ pinning layer on top.

The difference in doping concentrations in the p+ and n regions respectively (where one is significantly higher than the other) allows for the assumption that this junction can be approximated to a one-sided junction. This means that the depletion region is pushed away from the surface, confining it predominantly to the SW. The maximum potential reached under equilibrium is the pinning potential V_{pin} of the PPD.

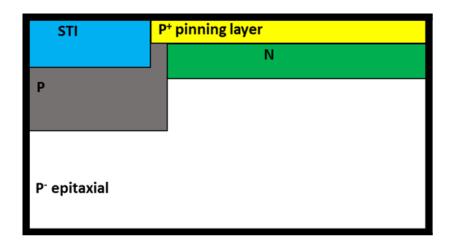


Figure 2-3: Cross section of Pinned Photodiode,

The V_{pin} of a PPD can be seen in Figure 2-4, where the energy band diagram is shown. Due to the doping concentration present in these p and n regions, the conduction band (E_c) and the valence band (E_V) bend and are at a minimum in the n-doped PPD region where it is fully

depleted of majority carriers. Therefore, carriers can be accumulated in this depleted region, where the total amount of charge that can be stored is related to the depth of this potential well. The depth of this potential is therefore characterised by the pinning potential of the photodiode (V_{pin}).

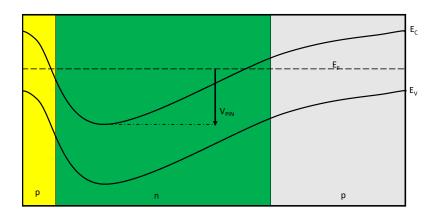


Figure 2-4: Energy band diagram of the PPD across the p+, n doped storage well and the p epitaxial layer. V_{pin} is the pinning potential of the PPD, E_F is the silicon fermi level, E_C is the silicon conduction band and E_V is the silicon valence band. Doping concentration differences in these regions result in the band bending, creating a potential well in the n region of the device.

Key electro-optical performance characteristics of 4T CIS are discussed in Section 2.6. Due to the isolation of the PPD depletion region from the interface states at the Si-SiO₂ interface, dark current in the device is reduced as these interface states could have been generation sites for dark current. Inclusion of the pinning implant also reduces the image lag as the potential maximum in the PPD cannot increase above the pinning voltage. A detailed review of the PPD for CIS was carried out in 2014 in Fossum and Hondongwa 2014 discussing the evolution, function and improvements of the device in greater detail.

2.3.3 Metal Oxide Semiconductor (MOS) Capacitor

The Metal Oxide Semiconductor (MOS) capacitor is typically made on a n- or p-type semiconductor substrate (e.g., silicon) and a conductive electrode typically referred to as a gate, often constructed of heavily doped polysilicon behaving as a 'metal' separated by a dielectric layer (e.g., SiO_2).

A MOS capacitor is typically referred to as n- or p-type dependent upon the substrate used. A p-MOS capacitor employs n-type silicon for the substrate (in this instance silicon doped with a group 5 element, typically phosphorus) and n-MOS capacitors make use of p-type silicon for the substrate (silicon doped with a group 3 element e.g., boron).

For an n-MOS capacitor, there are three distinct operational modes (Figure 2-5) that are determined by the potential difference between the gate and the substrate. These three operational modes are:

- Accumulation
- Depletion
- Inversion

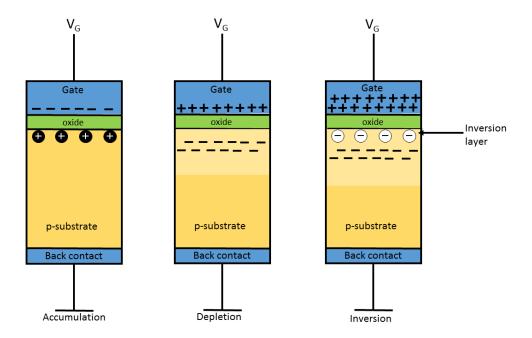


Figure 2-5: Three regimes of charge build-up in n-MOS structure following V_G application: Accumulation, Depletion, and Inversion.

Accumulation occurs when a negative voltage is applied to the gate and involves the accumulation of majority carriers (holes in n-MOS) to be attracted to the Si-SiO₂ interface.

2.3.3.1 Flat Band Voltage (V_{FB})

The gate voltage at which the MOS capacitor enters depletion is known as the flat band voltage (V_{FB}) i.e., the voltage applied to the gate electrode that yields a flat energy band in the

semiconductor. This voltage is related to the work function of the gate and the semiconductor substrate where the difference in work functions present in the semiconductor and the (polysilicon) gate provides the bending of the energy bands at zero applied bias voltage (Ytterdal, Cheng, and Fjeldly 2003). A voltage applied equal to the flat band results in a flat energy band within the semiconductor structure. However, in realistic MOS capacitors surface states at the semiconductor-oxide (Si-SiO2) interface also contribute to the effective gate voltage applied to a MOS capacitor. Therefore, the mathematical relationship of V_{FB} in a MOS device is determined by the equation:

$$V_{FB} = \Phi_{MS} - \frac{Q_i}{C_{ox}} - \frac{1}{\varepsilon_{ox}} \int_0^{t_{ox}} \rho_{ox}(x) x \, dx$$
 Equation (2.1)

where Φ_{MS} is the work function of the semiconductor material, $\frac{Q_i}{c_{ox}}$ is the voltage applied across the oxide (where Q_i is the charge and C_{ox} the capacitance) and $\int_0^{t_{ox}} \rho_{ox}(x) \, dx$ is the total charge in an oxide of thickness t_{ox} with ρ_{ox} being the charge density of the oxide .

Equation (2.1) shows that any change in the charge density in the oxide will alter the flat band voltage of the MOS capacitor.

2.3.4 MOSFET

A MOS capacitor can be developed into a Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET) structure which allows for the structure to perform basic switching and analogue functions. A MOSFET is a four-terminal device which can be used as an amplifier, active load, switch, or a capacitor in CIS. A MOSFET is a transistor which is either a p-type or n-type, dependent on the doped semiconductor material that makes up the channel.

A basic n-MOSFET consists of a main substrate formed from a p-type semiconductor below an oxide layer, implanted with two smaller regions of n-type dopant which are called source and drain, respectively. The structure is shown in Figure 2-6 where voltages applied to the gate (V_G) , source (V_S) and drain (V_D) control the current flowing through the device.

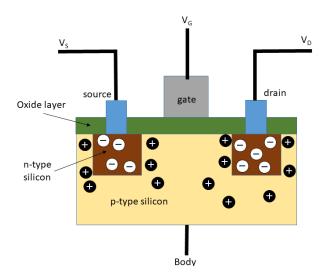


Figure 2-6: Cross section of n-MOS field-effect transistor identifying the four terminal structure (Source, Gate, Drain and Body) where p type silicon in the MOSFET is shown to have an excess of holes and the n-type silicon regions shown to have an excess of electrons.

When a positive voltage is applied to the gate of an n-MOSFET above the threshold voltage $V_{\rm TH}$ a depletion region is formed at the p region/oxide layer interface (between the n regions in Figure 2-6). The application of a gate voltage creates an inversion layer and results in the movement of electrons between the source and the drain. The drain current I_D is proportional to the gate to source potential difference, V_{GS} if $V_{GS} > V_{TH}$ and V_{DS} (drain to source potential difference) is small ($V_{DS} < V_{GS} - V_{TH}$). Whilst these conditions are satisfied, the MOSFET operates in what is known as a 'linear regime' denoted by Equation (2.2) (Toole, Plett, and Cloutier 2004)].

$$I_D = \mu C_{\text{ox}} \frac{W}{L} \left((V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right), \qquad V_{GS} > V_{TH}, V_{DS} < V_{GS} - V_{TH} \quad \text{Equation (2.2)}$$

Where W and L are the channel width and length, μ is the carrier mobility and $C_{\rm ox}$ is the gate capacitance per unit area. This clearly shows that the current across the transfer gate is dependent on both the width and length of the MOSFET.

2.3.4.1 Transfer Gate

The transfer gate in 4T CIS is a MOSFET used to transfer charge generated in the Pinned Photodiode (PPD, see Figure 2-3) to the Floating Diffusion (FD). This function is carried out through the application of a voltage known as the transfer gate voltage (V_G).

The transfer gate is connected to the PPD whilst also being in contact with the floating diffusion (FD). When a transfer gate voltage is applied, it permits the drift of electrons stored in the PPD across to the FD. The FD can be considered as a capacitor and as such charge accumulated on it causes an observable change in its voltage (due to the Q=CV relationship). As the voltage on FD decreases it will eventually reach a point known as sub-threshold, where V_{GS} becomes lower than V_{TH} . In this region charge diffusion from the PPD to the FD (i.e., the drain to source current) becomes governed by the following equation:

$$I_D = I_0 e^{\frac{V_{GS} - V_{TH}}{nV_T} \left(1 - e^{\frac{V_{DS}}{V_T}}\right)}$$

Where I_0 is the current at $V_{GS} = V_{TH}$ and V_T is the thermal voltage given by $V_T = kT/q$ (Sharroush et al. 2009)

2.3.4.2 Source Follower

The Source Follower (SF) is used to buffer the signal on the FD. A schematic of the SF circuit is shown in Figure 2-7. Each pixel in a 4T CIS device employs its own source follower MOSFET; the 'follower' (which 'follows' the signal on the FD). The input onto the Source Follower (SF) comes from the FD and the output is at the source of the MOSFET (the drain is biased at a voltage V_{DD} during operation). As discussed in 2.3.4.1, the voltage on the FD changes with respect to the charge converted on it. This means that the V_G of the SF changes during charge accumulation. V_S and V_D are connected to fixed voltages that means in order to maintain a constant drain to source current (I_{DS}) the V_{GS} voltage must change since $V_{GS} = V_{IN} - V_{OUT}$ in the structure and the relationship between V_{OUT} and I_{DS} is given by Equation (2.4):

$$V_{OUT} = V_{IN} - V_{TH} - \sqrt{\frac{2I_D}{\beta}}$$
 Equation (2.4)

Where
$$\beta = \mu C_{\text{ox}} \frac{W}{L}$$
 Equation (2.5)

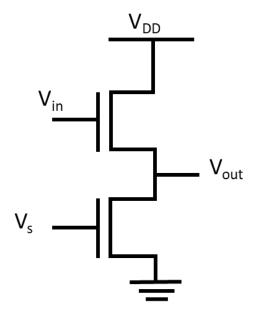


Figure 2-7: Schematic diagram of the source follower

2.4 The imaging process

2.4.1 Charge Generation

CIS pixels are arranged as photodetectors that deliver electronic signal related to photon count incident on the devices during a given 'integration' time. CIS employ the photoelectric effect (Figure 2-8) to convert the incoming photons into an electric signal.

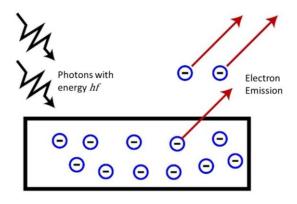


Figure 2-8: The (external) photoelectric effect

The photoelectric effect was first described by Einstein in 1905 and relates to the phenomena of electron emission from matter (particularly metals) when energy from electromagnetic

radiation incident on the surface is absorbed. Emission of the electrons in the semiconductor in an image sensor is therefore governed by the following formula:

$$hf = \phi + E_k$$
 Equation (2-6)

Here ϕ is the work function of the material (energy required to emit an electron from the valence band), E_k is the Kinetic Energy (KE) of the emitted electron, h is the Planck constant (6.63x10⁻³⁴ m² kg s⁻¹) and f is the frequency of the light incident on the surface. This formula means materials have a minimum frequency and therefore a maximum wavelength above which electron emission does not occur. In silicon image sensors, the band gap is 1.14 eV, so photons below this energy do not interact via the photoelectric effect meaning silicon image sensors are transparent from the far infrared.

2.4.2 Charge collection

After the electron hole pair has been created in the photosensitive area the electric field present in the PPD moves the electron and holes into different regions of the device due to their respective charge. Holes can be swept away by the electric field present in the n-type silicon (Figure 2-3) SW in the PPD. Electrons present in this SW region are collected, awaiting transfer across the TG for readout.

As discussed in 2.3.2 charge collection in 4T CIS is carried out in the n doped storage well region of the PPD. These charges can accumulate up to a maximum level (known as the full well capacity).

2.5 4T APS pixel operation

This section describes the typical operation of 4T APS through discussion of its structure, the method for charge transfer conversion to voltage and readout sequence.

2.5.1 Structure

A 4T CIS pixel is based on a four-transistor architecture with photon detection implemented through a PPD. The structure of a 4T CIS is shown in Figure 2-9 and is made up of the following:

- Source-follower transistor (M_{SF})
- Reset transistor (M_{RS}) (Φ_{RS}) is the reset voltage)

- Row select transistor (M_{SEL}) (Φ_{SEL}) is the select voltage)
- Transfer gate (M_{TG}) (Φ_{TG}) is the transfer gate voltage)
- V_{dd} (power supply)
- Floating Diffusion (FD) (V_{FD} is across it)
- V_{PIXELOUT} (readout voltage of the pixel)

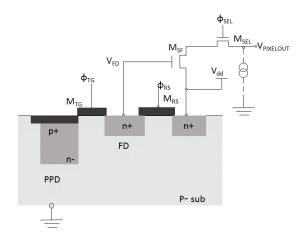


Figure 2-9: Schematic view of a 4T pixel

2.5.2 Transfer

Charge collection in the 4T pixel occurs in the n-type storage well. Charge is confined to this region of the device by the transfer gate (where during charge collection Φ_{TG} is biased to 0 V) through the creation of a 'barrier' at the PPD-TG vicinity (Sarkar, Buttgen, and Theuwissen 2013). Following integration, the signal charge accumulated on the PPD is transferred out of the photodiode through clocking the transfer gate high (to a voltage of Φ_{TG} , for a transfer time t_{tra}) across the TG to the FD.

Charge transfer in an idealised PPD-TG-FD structure is shown in Figure 2-10.

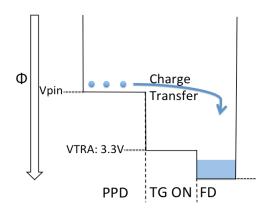


Figure 2-10: Idealised structure of the PPD-TG-FD structure where the TG is operating in accumulation mode. Charge transfer from the PPD across the TG to the FD occurs when the transfer gate is switched to a given Φ_{TG} voltage, shown by VTRA in the figure. Potential well limit in the PPD is governed by the pinning potential of the PPD.

Charge transfer out of the PPD is largely governed by electron diffusion and can be affected by the Φ_{TG} , pulse time (t_{tra}), the barrier height and the voltage on the FD (Han, Yao, and Theuwissen 2015). Charge transfer out of the PPD can therefore be described by the equation of sub-threshold transistor current:

$$I_{PPD-FD} = A \cdot SA \cdot T^2 e^{-qV_{bf}/kT}$$
 Equation (2-7)

Where I_{PPD-FD} is the current out of the PPD, with A being the Richardson constant which models thermionic emission expressed as $A=4\pi m^*\,k^2/h^3$ with m^* being the effective mass of the electron, k the Boltzmann constant and k the Planck constant, S_A is the area of the charge transfer path at the barrier and T is the temperature. Additionally, q is the electron charge, the voltage difference between the conduction band and valence band fermi level is V_{bf} and k the Boltzmann constant. Equation (2-7) however makes some assumptions about the operational characteristics of this transfer, some of which include that the number of transferred electrons is much less than the Equilibrium Full Well Capacity (EFWC) of the device, charge transfer within the PPD is neglected and that S_A is fully depleted. This relationship shows that the charge transfer out of a PPD is proportional to the temperature squared, and the exponent of the temperature.

2.5.3 Conversion to voltage

Conversion of charge to voltage occurs through the FD. As discussed in 2.3.4.2 charge accumulation on the FD following charge transfer causes a voltage step due to the Q=CV

relationship. The SF follows the voltage induced on the FD (with a certain amplification factor, typically less than one) and the voltage change on the SF is therefore related to the carrier build-up on the FD.

2.5.4 Readout sequence

Readout sequence in a 4T CIS typically involves the resetting of the FD (with TG held at low potential) and subsequent readout of the reset voltage level immediately before charge transfer from the PPD. Following charge accumulation, the signal in the PPD is transferred across the TG to the FD where the new voltage on the FD can be obtained. The FD is read out twice to carry out an image processing technique known as Correlated Double Sampling (CDS) where the signal before transfer can be subtracted from the signal after transfer to effectively eliminate the reset noise (the variation in the reset voltage level).

2.6 Imager performance characteristics

2.6.1 Noise Sources

2.6.1.1 Readout Noise

The readout noise is known as the 'noise floor' and defines the minimum observable signal. The three most important noise components are the thermal, 1/f (flicker noise) and random telegraph noise generated in the SF circuitry (Janesick et al. 2015).

The thermal noise component is also known as Johnson noise. This noise is not unique to 4T CIS however, and occurs in any conductor or semiconductor structure because of the random motion of the majority carriers. The thermal noise from the reset transistor causes a fluctuation in the reset level of the FD, which is eliminated by the reset level subtraction during CDS in a 4T pixel.

2.6.1.2 Fixed Pattern Noise

Fixed pattern noise (FPN) arises from any signal variance that occurs spatially across the device and is not a temporal noise like the readout noise. The difference in pixel outputs across the device can be influenced by a host of reasons such as difference in MOSFET thresholds; PPD size; dark current defects and differences in charge collection efficiency. FPN

due to process-induced variability in the PPD structure can introduce Photo-Response-Non-Uniformity (PRNU) and Dark-Signal-Non-Uniformity (DSNU).

2.6.1.3 Dark Signal

Dark signal is a thermally generated charge produced without any external illumination. The dark signal in 4T CIS is well studied and its major contributors are discussed in McGrath et al. 2018, where the dominant locations for dark current generation are:

- Surface dark current, which is heavily suppressed by the p+ pinning layer (Fossum and Hondongwa 2014))
- Depletion dark current
- Diffusion (bulk) dark current

Therefore, this section will concentrate on the origin of depletion and diffusion dark current. The dark current in 4T CIS is a sum of the depletion and diffusion dark currents, where in Sze and Ng 2006 diffusion is shown to dominate the dark current above room temperature due to the small value of n_i (the number of intrinsic carriers) in silicon.

2.6.1.3.1 Dark Signal generation

Dark signal generation occurs through the thermal excitation of majority carriers through the Shockley-Read-Hall (SRH) mechanism from the valence band into the conduction band. Defects and impurities in the silicon lattice result in trap-assisted dark signal where these defects/impurities (typically introduced during device fabrication) occupy energy states that are within the band gap of silicon, providing a defect site that was previously a 'forbidden' energy level E_t . The generation rate U is (Sze and Ng 2006):

$$U = \sigma v_{th} N_t \frac{pn - n_i^2}{n + p + 2n_i \cosh \frac{E_t - E_i}{kT}}$$
 Equation (2-8)

Which is under the simplified condition that $\sigma = \sigma_n = \sigma_p$ (the capture cross section of electrons and holes respectively). v_{th} is the thermal velocity of the carrier, N_t is the trap density, E_i is the intrinsic fermi level, and n and p are the electron and hole densities, respectively. In a fully depleted PPD all majority and minority carriers are swept away by the electric field. This means that $n \approx 0$ and $p \approx 0$, therefore the generation rate in Equation (2-8) can be simplified to:

$$U = -\left(\frac{\sigma v_{th} N_t}{2 \cosh \frac{E_t - E_i}{kT}}\right) n_i$$
 Equation (2-9)

2.6.1.3.2 Depletion Dark Current

From the relationship shown in Equation (2-9), the current due to the generation in a depletion region with size W_D can be expressed as

$$J_{dep} = \int_0^{W_D} q|U|dx \approx qUW_D = \frac{qn_iW_D}{\tau_e}$$
 Equation (2-10)

where τ_e is known as the generation lifetime of a carrier and is equal to the inverse of the term in brackets in Equation (2-9). From the relationship in Equation (2-10) the depletion dark current is shown to have the same temperature dependence as n_i where Sze and Ng 2006 shows n_i is governed by the following equation:

$$n_i = A T^{3/2} e^{-Eg/2kT}$$
 Equation (2-11)

Here A is a constant proportional to the effective density of states in the conduction and valence bands and E_g is the semiconductor band gap. This relationship shows that the dark current generation from the depletion region is proportional to the exponential of half the band gap of silicon.

2.6.1.3.3 Diffusion Dark Current

Diffusion dark current is generated in the field-free region of the device (Widenhorn et al. 2002) where the equilibrium electron density on the p-side n_{po} is much less than the equilibrium hole density on the n side p_{no} due to the heavy doping concentration of the n layer (meaning the DC from hole diffusion is negligible) the diffusion dark current is:

$$J_n \approx \frac{q D_n n_{po}}{L_n} \approx q \frac{n_i^2}{N_A} \sqrt{\frac{D_n}{\tau_n}}$$
 Equation (2-12)

Where we have used that in the field-free p-type semiconductor $n_i^2 = n_{po}N_A$, and the expression for the diffusion length $L_n = \sqrt{D_n \tau_n}$ (Sze and Ng 2006). The electron diffusion coefficient (D_n) over the carrier lifetime (τ_n) is proportional to temperature raised to a constant, (γ) , denoted T^{γ} and from this relationship the diffusion dark current can be expressed as

$$I_n \propto T^{3+\gamma/2} e^{\frac{-Eg}{kT}}$$
 Equation 2-13

The exponential term in diffusion dark current includes the full band gap of silicon, compared to half the band gap that in the depletion dark current.

2.6.1.4 Image Lag

In an ideal solid-state imager, all photons will be converted to a voltage and transferred for readout. However, in a real device, charge transfer can be incomplete where this phenomenon is referred to as image lag. Image lag often occurs during the sudden change in light intensity incident on the detector, typically in a bright to dark transition although it can also arise during a dark to bright transition. These two types of image lag are referred to as discharging and charging lag respectively, with discharging lag being the dominant lag source in 4T CIS devices.

In 4T CIS the typical method of charge transfer in the device takes majority carriers accumulated in the PPD and transfers them to the FD across the TG as seen in 2.5.2. Therefore, image lag in these devices arises from the incomplete transfer of charge from the photodiode to the floating diffusion after the transfer time has elapsed. This incomplete transfer of charge can be from a host of reasons (Bonjour, Blanc, and Kayal 2012; Fossum and Hondongwa 2014), some of which include:

- Potential barriers or pockets around the intersection of the transfer gate and the pinned photodiode
- Trapping of majority carriers by defects present in the photodiode or under the transfer gate.
- Spill back from the floating diffusion to the photodiode
- Poor charge drifts out of large photodiodes.
- Improper bias voltage selection

Potential pockets in the transfer pathway can trap electrons as they transfer across the PPD-TG-FD structure and can reemit these later (likely in a subsequent frame) resulting in image lag. Defects that have been introduced in the detector typically during fabrication can trap majority carriers as they pass from the PPD to the FD. When the emission time constant of the traps is greater than or equal to the transfer time, the probability of charge being deferred to a successive image resulting in image lag is most likely.

Spill-back occurs when charges that are transferred across the PPD-TG-FD structure during the transfer time spill-back into the photodiode resulting in a lower signal read out than is accumulated on the PPD. The remaining photon-generated charge carriers will be left over in the PPD to be read out in subsequent frames. This spill back phenomena is correlated to the potential on the FD and as such is expected to be most prevalent when the charge accumulated is close to or above the Equilibrium Full Well Capacity (EFWC) of the device. Spill-back will also occur when the potential of the FD at charge transfer is close to the pinning potential of the PPD.

Spill back has been identified in works by Han, Yao, and Theuwissen 2015 where a charge transfer mechanism which considers the effect of the FD potential during transfer, electron diffusion and thermionic emission theory supplemented with a conduction band correction. From these theories Han et al. suggest the emission current from the TG tunnel to the PPD (I_{back}) in simulated 4T pixels is governed by Equation (2-14).

$$I_{back} = I_0 exp\left(\frac{-q(\varphi_{fFD} - \varphi_{pin} + E_g/2q)}{kT}\right)$$
 Equation (2-14)

$$I_0 = AS_A T^2$$
 Equation (2-15)

Where A is the Richardson constant, S_A is the area of cross section of the charge transfer path at barrier position (assumed identical in the forward and reverse direction), φ_{fFD} is the Fermi level potential of the TG tunnel and FD, φ_{pin} is the lowest potential in the n- type region at the PPD-TG vicinity, E_g is the band gap width, q is the elementary charge, k is the Boltzmann constant and T is the temperature.

Equation (2-14), shows that the spill back current is proportional to the exponential of the inverse temperature, so when the device is dominated by charge spill back, one can expect the image lag to be fractionally higher for a larger temperature.

From Han, Yao, and Theuwissen 2015 the conditions of Equation (2-14) however, state that if ϕ_{FFD} - ϕ_{pin} is sufficiently large, (i.e. when transferred electrons is low) that the potential under the flat region of the TG is depleted. This means that the condition for spill back of being in proximity to EFWC is not reached and spill back can be neglected (meaning image lag will be dictated by poor charge transfer out of the PPD Equation (2-7). When the number of electrons

transferred increases (approaches EFWC), lowering the potential ϕ_{fFD} this can result in TG tunnel inversion meaning spill back dominates in the device.

In larger pixel devices, electron drift time out of the photodiode is large. This means that image lag can arise in situations where the duration of the applied transfer gate pulse is not sufficiently long. Image lag in this instance can be improved by increasing the transfer time of the majority carriers out of the photodiode, or by increasing the drift velocity of electrons, typically through an increase in temperature.

2.6.1.5 Random Telegraph Signal (RTS)

Random Telegraph Signal (RTS) occurs through the 1/f noise variance on the SF output circuitry of the device. Traps that are introduced during fabrication can capture and release free carriers passing between the drain and the source in the MOSFET causing the voltage (V_{OUT}) to fluctuate. These single traps result in the fluctuation between two distinct levels as an electron is released. This gives rise to three-pixel outputs (because of CDS on the device) of:

- Reset level readout trap is occupied, signal readout level trap is unoccupied.
- Reset level readout trap is unoccupied, signal level readout trap is occupied.
- In both the reset level readout and the signal level readout the trap is either occupied or unoccupied

This phenomenon is known as RTS and results in a difference in the signal level for readout based on the trap occupancy.

2.6.2 Photon Transfer Curve

The photon transfer curve (PTC) is used to obtain the Charge to Voltage Factor (CVF) of the device. The expected shape of a PTC is dictated by 4 primary regions and shown in Figure 2-11.

- Readout Noise Floor
- Shot noise (when gradient of curve is 0.5)
- FPN (when gradient of curve is 1)
- Saturation

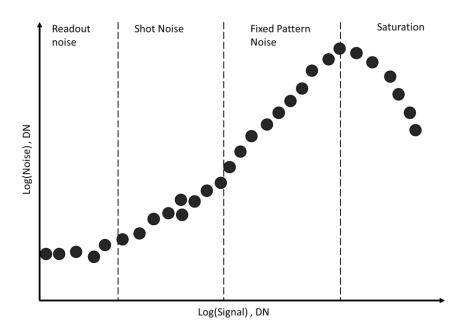


Figure 2-11: Model Photon Transfer Curve

The readout noise, σ_R (combination of the noise floor of the PTC) is characterised by a flat region in the PTC. If the PTC is plotted in a pixel-by-pixel basis, there will be no region in the device that is FPN dominated with a gradient of 1, however if the CMOS PTC is taken over the mean of the device, there will be a region of the device which has a gradient proportionality of 1 in the mean-variance curve, where FPN is dominating the signal in the device.

For a PTC which has no FPN region, the conversion gain of the device can be obtained from the relationship that the variance of the signal is equal to the number photons observed during integration and thus the standard deviation of the signal is equal to the square root of the number of photons observed during integration. From Janesick (Janesick 2007) the relationship between the signal variance and the signal mean can be determined by the following equation:

$$\sigma_S^2(DN) = \frac{S}{G} + \sigma_R^2$$
 Equation 2-16

Where G is the system gain, used to convert the converted signal in DN (ADC code) into physical units of electrons N_e :

$$N_e = S(DN)G$$
 Equation 2-17

Ignoring the flat region of the PTC, a linear fit to the shot noise dominated region can be used to extract the conversion gain (G) of the device, which is equal to the inverse of the gradient of the linear fit.

2.7 Summary

In this chapter, the concept of 4T CIS is introduced. Here key structures which govern the operation of the device are included. The pinned photodiode is used as the photosensitive element for charge collection, where this charge is transferred out through a MOSFET known as the transfer gate. This charge is stored on a capacitor known as the floating diffusion, where correlated double sampling is employed to measure the voltage on the FD before and after charge transfer to reduce thermal noise. The concept of the pinning potential on the PPD is also introduced, with the pinning voltage being related to the total amount of charge capable of being stored in a pixel.

In addition to thermal noise present in 4T CIS, this chapter also introduces other noise sources in these devices that hinder image quality. Dark signal occurs as the result of thermal excitation of majority carriers and can contribute to the total amount of signal observed during readout. The main components of dark signal in 4T CIS is shown to be from depletion and bulk dark signal. Another noise concept that effects the image quality in 4T CIS is also introduced in this chapter, where this noise results in spurious charge being read out in subsequent frames in the device. This phenomenon is known as image lag and is predominantly caused by pockets or barriers in the transfer pathway and spill back of signal charge from the FD to the PPD across the TG.

Since the first use of CMOS APS in space in 1997, modern day scientific imagers now require higher precision imagers and understanding the physics that govern how these devices operate will be invaluable in the development and characterisation of any high-quality imager. Although this is the case, if these imagers operate in space, they can be expected to be exposed to certain levels of irradiation. Merely understanding how these devices operate will therefore not assist in characterisation of CMOS APS for space missions as the possible degradation of a device because of an irradiative source will not be understood. The following chapter therefore looks to characterise the response to CMOS APS and their structures following a mixture of irradiative sources.

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Chapter 3: Space radiation damage in CIS

3.1 Introduction

This thesis involves the characterisation of the CIS115, a 4T CIS which is the imager to be used in JANUS camera on the JUICE mission. The radiation environment that the JANUS camera is expected to be present in leads to a host of requirements on the performance of the CIS115. This chapter introduces typical radiation sources and where Chapter 2 introduced the structure of CIS, this chapter will also include the radiation damage one can expect on CIS and their structures.

3.2 Radiation Sources

Radiation can be identified through a specific source or particle type. Typically, these particle types can be either charged particles (like protons and electrons), uncharged particles (like neutrons) or photons (like γ -rays). These radiation sources are known to interact in silicon through ionising and non-ionising interactions where interactions can be with the nuclei or the electrons in the lattice. Interactions with the nuclei can first result in displacement damage and interactions with the electrons can first give ionising damage. Although this is the case, displaced nuclei can cause secondary ionisation if they possess enough kinetic energy, and ejected electrons too can cause further ionisation and displacement if they possess enough kinetic energy.

3.2.1 Space Radiation Environment

Classically, radiation in space can be categorised into two different sources: transiting radiation and trapped radiation. Trapped radiation is present around bodies with a sufficiently strong magnetic field to 'trap' charged radiation around them. The JUICE mission is destined for the Jovian system containing the largest magnetic field in the solar system surrounding a planetary body. The size of this magnetic field extends approximately 7 million km in the direction toward the sun and almost to the orbit of Saturn in the other (Russell et al 1997).

Transiting radiation is known as such because the radiation 'transits' an area of space uniformly and typically is made up of particles known as 'cosmic-rays'. These cosmic rays are

split into a 'galactic' component (i.e., the source of these cosmic rays lies outside of our Solar System) alongside a component coming from 'solar wind' (particle flux originating from the sun).

Any CIS used for the JUICE mission will therefore be damaged through both ionisation damage and displacement damage. During this mission, the total amount of displacement damage is typically expressed as a Total Non-Ionising Dose (TNID) and the total amount of ionisation damage as Total Ionising Dose (TID).

3.3 Displacement damage mechanisms

Displacement damage in materials is from the result of nuclear interactions between an incoming particle with the atomic lattice, resulting in an elastic scattering between the projectile and the lattice. As high energy particles interact with matter, they can displace an atom from its original lattice position, and the amount of energy deposited from nuclear interactions within a target material (which can create defects) is typically expressed in terms of Non-Ionising Energy Loss (NIEL).

3.3.1 Non-Ionizing Energy Loss

The NIEL of a particle interacting with a material is a metric for expressing the energy loss of the particle in that material due to non-ionising processes i.e., collisions (both elastically and inelastically). As the particle travels through the material lattice, it can displace atoms. For a given particle, the product of its fluence and its NIEL (at a certain KE) will give the displacement damage energy deposition per unit mass of the material. NIEL is dependent on the target material (in this instance silicon) and is expressed typically with units of keV cm² g⁻¹. NIEL of a particle depends on both the particle type (for example protons and neutrons) and its energy. It is useful in the field of bulk damage since NIEL can be used to correlate displacement damage effects of varying particle types/energies by normalising them to a certain fluence. NIEL values are extensively documented for Si for most space radiation sources over a wide energy range (proton, neutron and electrons) with their respective NIEL values collated in (A Vasilescu 2000) and shown in Figure 3-1.

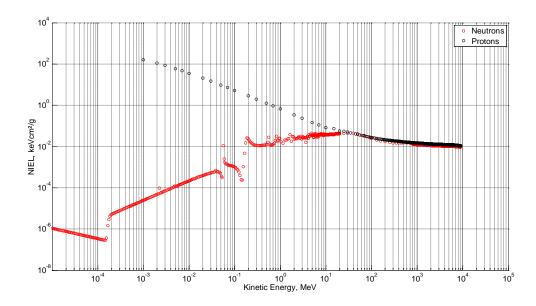


Figure 3-1: NIEL scaling for neutrons and protons within Silicon, with values taken from (A Vasilescu 2000)

Typically protons are scaled to an equivalent dose of 10 MeV protons using NIEL scaling for comparison, however this NIEL scaling is not entirely accurate in silicon where Huhtinen 2002 shows that some non-negligible deviations from real data to theoretical calculations of NIEL exists. This highlights that NIEL is not the perfect model for representing displacement interactions in silicon. Although this is the case, NIEL can still be used for normalisation for a good approximation to the damage induced by a given particle spectrum.

3.3.2 Displacement damage in silicon

Radiation can interact elastically (i.e., no net loss in KE between the radiation source and the target material) through the phenomena of Rutherford Scattering. If the incoming particle has enough energy, atoms can be released from the lattice resulting in displacement damage. Removing an atom from its lattice position is known as a 'vacancy' with the displaced atom being known as an 'interstitial'. The stable combination of a vacancy and an interstitial is a 'Frenkel-Pair'. In silicon, the typical displacement damage effects are shown in Figure 3-2.

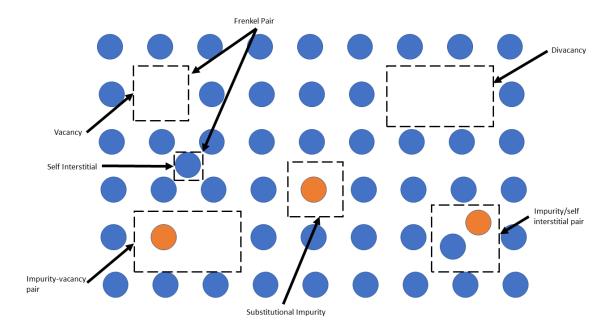


Figure 3-2: Schematic view of some of the defect types that can arise in a silicon lattice following TNID. Blue circles represent silicon atoms, and orange circles represent any impurity atoms.

Displacement damage effects in silicon is greatly studied in (Moll 1999), where some of the key defects in silicon with respect to TNID/TID are listed. These include:

- A-centre, a vacancy-oxygen defect
- E-centre, a vacancy-phosphorous defect
- Silicon Divacancy

The first two defects appear in Figure 3-2 as a vacancy in the form of the impurity-vacancy pair, and the divacancy is already clearly labelled in the figure.

If a displaced atom in the lattice has been given enough energy, it can continue displacing surrounding atoms resulting in a 'defect cluster', i.e., a concentration of defects in a given volume. Neutrons can penetrate more deeply into matter than charged particles of similar KE since they do not interact with electrons and are therefore more likely to displace lattice atoms in the silicon bulk and create vacancies, interstitials, and defect-clusters. It should be noted that neutrons of a few MeV are more effective at creating defect clusters than their charged counterparts (protons) at the same energy and are also more effective at creating these defect clusters than electrons (Smith 2003). Protons and electrons are more likely to

create isolated or point defects. As such, one would expect a higher number of defect clusters in a neutron irradiation of the same NIEL scaled energy than protons or electrons.

3.3.3 Effects of displacement damage on imager characteristics

Displacement damage in CIS can affect a multitude of characteristics in 4T CIS that can alter image quality. Some of these include the dark current and the charge transfer inefficiency of the imager, which will be discussed here.

3.3.3.1 Dark current

Displacement damage effects on the dark current largely arise from lattice defects that are created, inducing energy levels that occupy a region in the band gap of silicon. These new defect sites alter the recombination rates (U from Equation (2-7)) in the bulk silicon acting as a defect site for thermal electrons moving from the valence to the conduction band within the forbidden energy region (within the band gap of silicon). Due to the nature of these displacement damage induced defects, it results in a non-uniform increase in dark current in the device, creating 'bright-pixels' with high dark current (Srour, Marshall, and Marshall 2003).

Radiation-induced bulk defects which affect the dark current of the device is shown in the works of (Belloir et al. 2016) where following alpha irradiation many traps are created in the silicon bulk. Trap induction rate is studied in (Hönniger 2008) where a proton fluence shows that many trap species can be created in the bulk of silicon (e.g. A-centre, E-centre, divacancy etc). These species can act as Shockley-Read-Hall (SRH) dark current generation sites, enhancing the DC in the device.

3.3.3.2 Charge Transfer Inefficiency

Defects in silicon following TNID can trap charge in the device. When this charge trapping occurs during the transfer of a charge packet in a CCD and is reemitted in a subsequent charge packet, this results in Charge Transfer Inefficiency (CTI). The amount of CTI is related to the electron capture and the emission time of this trapped charge, and is discussed in further detail in (Holland 1993). If these defects exist in 4T CIS and can trap electrons from the transferred charge packets (with an emission time in the order of the transfer time) these

trapped electrons will be read out in subsequent frames in the device, contributing to the image lag or charge transfer inefficiency in 4T CIS.

3.4 Ionising damage

When charged particles interact inelastically in a CIS, it can be through a displacement damage process as already discussed, or through an ionising process. Ionisation occurs when the energy of the incoming particle is sufficient to excite an electron into the conduction band, which takes ~ 3.73 eV in silicon (Mazziotta 2008), and ~ 18 eV (Ausman Jr and McLean 1975) in SiO₂.

The amount of energy lost through ionisation events from a radiation source is measured by the Linear Energy Transfer (LET) of the charged particle. This electron hole pair creation within the Si or SiO_2 can either be direct or indirect. Direct ionisation occurs when charged particles of enough energy eject an electron from around an atom. This high energy particle can continue to travel through the material ionising other atoms until its kinetic energy is lost. Indirect ionisation can occur from uncharged particles where, for example, a photon or a neutron ejects a high energy (secondary) electron from the atom which can in turn ionise many other atoms.

3.4.1 Ionising damage in CMOS sensors

Ionising damage in CIS is known to change the operational parameters of the device. Ionisation damage involves the creation of electron hole (e-h) pairs which are often created in either the bulk silicon or in the SiO_2 layer.

Electron hole pairs arising in the bulk silicon have little damaging effects on CIS, where the electrons are collected as signal charge and the holes swept away by the substrate potential. As a result of this, e-h pairs created in the bulk silicon will pose a problem if the imager is being integrated during irradiation, contributing to the transient noise background in the image. Although this is the case, e-h pairs created in this region can give rise to a parasitic current between the source and the drain which can persist in the MOSFET indefinitely without reset. This phenomenon is known as latch-up and is damaging to CIS. Latch up is discussed further in 3.4.3.

E-h pairs generated in the SiO_2 layer however can be damaging to the imager. Electrons present in this region have an increased mobility to their hole counterparts and as such can be swept out of the oxide (Oldham and McLean 2003) leaving behind the less mobile holes. These holes are then repelled toward the $Si-SiO_2$ interface due to the applied electric field and become trapped by the high concentration of impurities at this region.

At the $Si-SiO_2$ boundary, the Si and the SiO_2 do not form perfect bonds, which leaves 'dangling bonds' present at the interface (Ytterdal, Cheng, and Fjeldly 2003). These dangling bonds can be damaging to image quality and as such are found to be greatly reduced if the device is annealed (at around $500^{\circ}C$) in a hydrogen atmosphere (Swaroop 1973), where the hydrogen reacts with silicon dangling bonds substituting these for a new Si-H bond. However, following ionising radiation, holes that accumulate at the interface can have an anti-annealing effect, recreating these 'dangling-bonds' in the device (where the leftover hydrogen diffuses out of the device).

3.4.2 Effects of ionising damage on imager characteristics

Ionising radiation has shown to cause damage to CMOS devices, where this damage can hinder key electro-optical performance characteristics in the device. Some of the degradation mechanisms for select electro-optical parameters are discussed here.

3.4.2.1 Dark current

As discussed in 2.6.1.3 dark current arises from the thermal excitation of electrons from the valence band to the conduction band. Dark current in a CIS can also be assisted from any trap species creating intermediary energy levels that exist between the conduction and the valence band of silicon. One such intermediary energy level can be created following Total Ionising Dose (TID) due to the anti-annealing effect of holes at the Si-SiO₂ interface. The dangling bonds left behind following TID can act as an energy level in the forbidden region of the silicon band gap and as such increase the dark current.

Many works exist investigating the effect of ionising damage on 4T CIS, some of which are discussed here. In (Rao, Wang, and Theuwissen 2008) they investigate the response of a 4T CIS following exposure to γ -rays. They find that following TID, dark current increase is shown to be dominated by changes to the Si-SiO₂ interface and degradation at the Shallow Trench Isolation (STI). Rao et al. also suggest that the latter dark current source is very susceptible

to damage caused by these γ -rays, increasing the STI leakage current, hence enhancing the dark current. Isolation of potential dark current sources following TID in CIS is carried out in (Goiffon et al. 2011) where they summarised that (up to 150 krad) TID dark current sources come from the PPD (most likely as a result of damage in the top oxide) and the region of the TG near the STI, similar to what was shown in Rao, Wang, and Theuwissen 2008. Additional works (Wang et al. 2016) also confirmed the degradation on the STI where they also state that TID DC degradation occurs due to trapped positive charges and interface states caused by TID in other regions of the CIS which include the Pre-Metal Dielectric (PMD), nitride spacer, TG and the gate oxide.

Essentially these works suggest that DC increase following TID arises from a level of charge build-up and creation of interface states in the device in locations such as

- Pre-Metal Dielectric (PMD)
- Nitride Spacer
- Shallow Trench Isolation (STI)
- Transfer Gate (TG)
- Gate Oxide

These locations are shown in Figure 3-3.

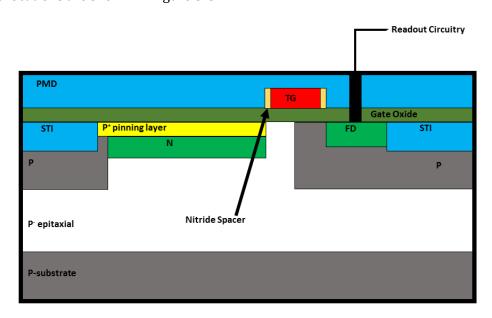


Figure 3-3: Cross sectional view (not to scale) of a 4T PPD pixel. Charge collection occurs in the N well below the P+ pinning layer, known as the Storage Well (SW), where the structure in this region is the pinned photodiode (PPD). DC degradation can occur in this pixel structure following TID from the creation of interface states at the PMD, nitride

3.4.2.2 Flat band voltage shift (FBVS)

As discussed in 2.3.3.1 the flat band voltage in a semiconductor is the voltage at which the MOS capacitor enters depletion. In Equation (2.1) it was shown that this voltage V_{FB} has a contribution from the integral of charge density of the oxide thickness given by Equation (3-1).

$$\frac{1}{\varepsilon_{ox}} \int_0^{t_{ox}} \rho_{ox}(x) x \, dx$$
 Equation (3-1)

If holes are accumulated at the Si-SiO₂ interface, this will result in the charge density of the oxide increasing, which in turn results in a flat band voltage decrease. Typically, this is expressed in 4T CIS through a change in the threshold voltage (the voltage applied to the gate of a MOSFET resulting in current flow from the source to the drain) of the MOSFET. The threshold voltage of a MOSFET is dependent on the V_{FB} and as such changes in V_{FB} will therefore be observed in changes in the threshold voltage of the MOSFET. In extreme cases sizeable shifts in the V_{FB} of the device through hole accumulation at the interface from TID can result in the MOSFET's operational failure (Winokur et al. 1987).

3.4.2.3 Lag

Image lag in 4T CIS is defined as the incomplete transfer of charge from the PPD to the FD across the FD. As mentioned in 2.6.1.4 incomplete charge transfer can be for several reasons where some of these image lag sources cannot be influenced by TID and as such can be assumed to be unchanged following TID. However, TID can cause a build-up of charge in the gate oxide and can alter the effective bias voltage due to the flat band voltage shift phenomena. Changes in bias voltages under the PPD/FD/TG induced by TID will therefore be expected to alter the image lag by changing the potential profile across the pixel. Further details in radiation effects following TID is discussed in 8.2.1 with details into other research by Goiffon et al 2012, 2014 (Goiffon et al. 2014; Goiffon et al. 2012) detailed.

3.4.3 Single Event Effects

Single Event Effects (SEEs) occur in CMOS devices as the result of the transition of ions through a device. This can result in a variety of SEEs such as

- Single Event Upset (SEU)
- Single Event Function Interrupts (SEFI)
- Single Event Latch up (SEL)

A single event upset occurs in device memory where a bit flips in the device, changing the memory state from a 1 to a 0 or vice versa. A single event functional interrupt causes a component to malfunction in a detectable way however differs in response to a single event latch up which can result in permanent damage and will require power cycling to restore normal operation. These effects can have serious implications to the operation of CIS. Studies on SEEs in the CIS115 are beyond the context of this thesis, and further work on SEEs can be found in (Rushton 2018) where SEEs are studied in greater detail. It should be noted however that the CIS115 is immune by design to SEUs, as it lacks any internal storage.

3.5 Summary

In this chapter ionising and non-ionising radiation is introduced with respect to its interaction with silicon. This chapter categorises radiation damage in 4T CIS as either displacement damage or ionising damage.

The concept of NIEL is also introduced in this chapter which is a metric that is used for expressing the energy loss of the particle in a material due to non-ionising processes. Displacement damage in 4T CIS involves the removal of an atom from the lattice and can result in a range of defects which are shown in Figure 3-2. In this chapter, displacement damage effects on imager characteristics are also discussed, where displacement damage is shown to increase the dark current and the image lag in 4T CIS.

Ionisation damage in 4T CIS is also discussed where the creation of electron hole pairs within the device is shown to induce numerous types of damage in detectors. Some of the damage on the detector will directly worsen image quality such as an increase in the dark current and image lag of the device, whereas others are shown to change the operational characteristics of the device such as the introduction of a flat band voltage shift and single event effects.

Radiation sources clearly influence key electro-optical performance metrics in 4T CIS. Understanding the heritage of radiation interactions between silicon imagers is vital in understanding how new devices will be expected to behave in a radiation environment and to also understand their response following exposure to one. For space missions, this knowledge is vital, where an image sensor that has excessive degradation in performance would be catastrophic to a space mission in an irradiative environment. One such space environment is the Jovian radiation environment. The following chapter discusses the Jovian radiation environment, the science mission that is scheduled to arrive there in 2030 (The JUpiter ICy moons Explorer (JUICE) mission) and the 4T CIS that will be used to take detailed images during the mission.

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Chapter 4: The Jupiter Icy Moons Explorer (JUICE) Mission

4.1 Mission Introduction

In 1995 the Galileo spacecraft conducted the first detailed exploration of the Jovian system. The satellite took interest mainly in the four Galilean satellites, Io, Europa, Ganymede and Callisto. From this mission it was revealed that these unique moons were worthy of further investigation, particularly the icy moons of Jupiter (Ganymede, Europa and Callisto). This was because of Galileo presenting strong evidence of sub-surface oceans (especially on Europa). Evidence suggested Europa possessed a melted sea water ocean under an ice layer on its surface and indicated that both Ganymede and Callisto possessed layers of liquid saltwater (Meltzer 2007).

From this analysis of the system and the results the Galileo spacecraft presented, a more detailed study into the Jovian system was proposed: the JUpiter ICy moons Explorer (JUICE) mission. This is an ESA L-class mission destined for the Jovian system, which will explore the system in greater detail than was presented by the Galileo spacecraft. Whilst present in the Jovian system, the hope is to study (Grasset et al. 2013):

- the planet Jupiter and its magnetosphere.
- the giant icy moon Ganymede.
- Callisto and Europa.

The planned mission lifetime is three years with an expected schedule shown in Table 4-1.

Data	Mission Profile		
06/2022	Launch by Ariane-5		
01/2030	Jupiter orbit insertion and Jupiter tour		
	Transfer to Callisto (11 months)		
	Europa Phase: 2 Europa and 3 Callisto flybys (1 month)		
	 Jupiter High Latitude Phase: 9 Callisto flybys (9 months) 		
	Transfer to Ganymede (11 months)		
09/2032	Ganymede orbit insertion and Ganymede tour		
	Elliptical and high-altitude circular phases (5 months)		

	Medium altitude (500 km) circular orbit (3 months)
	Low attitude (200 km) circular orbit (1 month)
06/2033	End of Nominal mission

Table 4-1: Nominal Mission profile for the JUICE Mission, from (Team 2012)

4.2 JUICE Scientific requirements

The Jovian characterisation, as discussed in 4.1 hopes to explain some of ESA's 'cosmic visions'. The intent is to obtain further information into the following themes (Grasset et al. 2013):

- What are the conditions for the planet formation and the emergence of life?
- How does the solar system work?
- What are the fundamental physical laws of the Universe?
- How did the Universe originate and what is it made of?

Alongside ESA's wider 'cosmic vision' for this and other scientific missions it undertakes, key scientific parameters have also been identified for detailed research on JUICE (Team 2012):

- Emergence of habitable worlds around gas giants
- The Jupiter system as an archetype for gas giants

which can be subdivided into the mission relevant scientific aims and how it is hoped can be achieved by a scientific instrument on JUICE. More details on the scientific aims can be found in Table 1.1 of the JUICE Red Book, (Team 2014).

These scientific goals are hoped to be achieved by a wide variation of instruments present on JUICE. A total of 11 instruments (shown in Table 4-2) have been planned for the JUICE mission. The Centre of Electronic Imaging (CEI) has a Co-Investigator role on the JANUS camera (the optical camera system), with a contribution of the imaging sensor to the instrument. Characterisation, optimisation, and radiation studies of the image sensor has been a key project for the group, and the work contained in this thesis has added to this study.

Instrument	Purpose
JANUS: Camera System	An optical camera

MAJIS: Moon and Jupiter Imaging Spectrometer	A hyper-spectral imaging spectrometer	
UVS: UV Imaging Spectrograph	A UV spectrometer	
SWI : Sub-millimetre Wave Instrument	A sub-millimetre wave instrument	
GALA : GAnymede Laser Altimeter	A laser altimeter	
RIME: Radar for Icy Moons Explorer	An ice penetrating radar	
J-MAG : A magnetometer for JUICE	A magnetometer to characterise the Jovian magnetic field	
PEP : Particle Environment Package	A plasma package with sensors to characterise the plasma environment in the Jovian system.	
RPWI: Radio and Plasma Wave Investigation	A radio plasma wave instrument	
3GM : Gravity and Geophysics of Jupiter and Galilean Moons	A radio science package comprising a Ka transponder and an ultra-stable oscillator.	
PRIDE: Planetary Radio Interferometer and Doppler Experiment	PRIDE will use the standard telecommunication system of the JUICE spacecraft and VLBI - Very Long Baseline Interferometry - to perform precise measurements of the spacecraft position and velocity to investigate the gravity fields of Jupiter and the icy moons.	

Table 4-2: Instruments planned for the JUICE mission, from (Team,2014) (ESA, 2013)

4.3 Jovis Amorum ac Natorum Undique Scurtator (JANUS) Camera

The JANUS camera is required to take detailed multispectral images of the surfaces of the Galilean moons of Jupiter and the atmosphere of Jupiter itself. The detector will be required

to take detailed images of these surfaces at between 2 km per pixel to as low as around 10 m per pixel of local and regional morphology.

4.3.1 Design

The JANUS optical design parameters taken from Della Corte et al. 2014 are shown in Table 4-3, where the detector used employs approximately 3 million 7-micron pixels for image capture over a spectral range from around 350 nm to 1050 nm.

Specification	Value
Detector format	2000×1504
Pixel size	7 μm
Spectral range	350 – 1050 nm

Table 4-3: JANUS main parameters

For the JANUS camera to image over a varied spectral range, the design of the optical head unit includes a filter wheel with 13 filters for varied spectral observations. These filters will be used to identify different characteristics in the Jovian system (for example a near infrared filter for looking at the lava spots on Io) and as such the detector will need good Quantum Efficiency (QE) response within the spectral range shown in Table 4-3.

4.3.2 JANUS Camera Imager Requirements

As aforementioned, the detector selected will require good QE within the JANUS spectral range to obtain high quality scientific images of the Jovian system. This however is not the only limiting characteristic on the JANUS camera as many other electro-optical performance parameters have minimum requirements in order to meet the goals shown in Table 1.1 of the JUICE Red Book, (Team 2014). Studies at The Open University have characterised the performance of the image sensor for the JANUS camera, with some of these works contained within this thesis.

4.3.3 Selection of the CIS115

Any solid-state imager that is used for the JANUS camera must be able to meet most of the selection criteria for the imager. The imager benchmarked for the JANUS camera on JUICE was the CIS107, a 4T CIS test device constructed by Teledyne e2v. From analysis on the CIS107 it was apparent that one of the pixel designs could be developed into a suitable sensor

for the mission, and started the development of the CIS115, ultimately the detector for the JANUS camera on JUICE. From the datasheet for the CIS115 the key electro-optical parameters of the detector can be extracted and are shown in Table 4-4 alongside the mission requirements set on the detector.

Parameter	Typical	Mission Requirement
Number of pixels	1504×2000 pixels	1504×2000 pixels
Pixel size	7×7 μm	7×7 μm
Peak Linear Charge per pixel	27000 e ⁻ /pixel	23000 e ⁻ /pixel
(Q-LIN)		
Mean readout noise	5 e- RMS	<8 e- RMS
Dark current at 293 K	12 e- / pixel/ s	< 90 e-/ pixel/ s
Image Lag (at 50% Q _{LIN})	1%	≤1%

Table 4-4: Electro-optical characteristics from Teledyne e2v CIS115 datasheet and mission requirements (Teledyne e2v 2016)

Alongside the parameters shown in Table 4-4 another reason for the selection of the CIS115 is its inherent radiation hardness. Radiation hardness in Teledyne e2v CIS has been extensively studied in works such as Greig 2008; Pike, Pratlong, and Greig 2013, where the radiation test structures have been characterised shaping the development of other e2v CIS. The harsh Jovian environment (see 4.5) requires the device to have a high radiation tolerance to ensure mission quality toward EOL hence the use of a 4T CIS.

4.3.4 Motivation for CIS115 Characterisation

The electro-optical characteristics shown in Table 4-4 taken from the CIS115 datasheet was carried out at Teledyne e2v, typically at 293K. The JANUS camera on JUICE will operate at 238K ± 10K and will operate in a harsh radiation environment. None of the results presented in Table 4-4 were measured at the mission temperature or following any irradiative source, where ensuring device operation and performance after accumulating varied Total Ionising Doses (TIDs) and Total Non-Ionising Doses (TNIDs) is essential to mission success. The CIS115 will provide ample quality for the mission at BOL so therefore characterisation of the imager following TNID and TID will study the detector behaviour at EOL, determining if it is able to meet the minimum detector requirements.

4.4 CIS115 Heritage

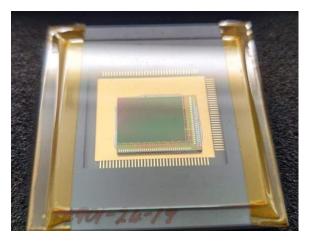
4.4.1 CIS107

Scientific imagers typically undergo several revisions and experience many design changes carefully selected through many types of testing carried out on the device. The CIS115 is no different to this and one of these early iterations is CIS107, a 4T CIS that the CIS115 is derived from.

The CIS107 is made up of 10 different pixel design variants made similarly to the CIS115 with 7 μ m size pixels manufactured in the 0.18 μ m imaging process (Wang et al. 2014). These back illuminated 4T pixel variants underwent testing in Soman et al. 2014; Wang et al. 2014; Pike, Pratlong, and Greig 2013 and the best pixel variant was used in the development of the CIS115 Rev A.

4.4.2 CIS115 Revision A

The first iteration of the CIS115 was a revision A CIS115 based on the 'optimal' pixel type present in the CIS107, maintaining 7 μ m pitch pixels and a pixel array of size 1504×2000. The device is reviewed in Soman et al. 2014 and key details from this testing shows that the device meets the mission requirements shown in Table 4-4. The CIS115 Revision A however needed adjustment as extended work on the detector showed blooming characteristics where charge spilled out of a pixel onto neighbouring pixels at high illumination levels. This blooming problem was ultimately resolved by fixing of an implant in the pixel that was shown to be incorrect and causing charge to spill into adjacent pixels. This solution culminated in a second manufacturing iteration of the CIS115, referred to as the Revision B CIS115 where these detectors are shown side by side in Figure 4-1.



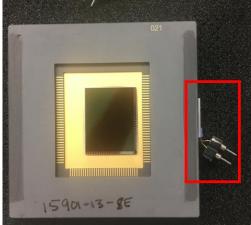


Figure 4-1: CIS115 Revision A, front illuminated (left) and CIS115 Revision B, back illuminated (right). Highlighted in the red box is a PT1000 platinum resistance thermometer attached to the CIS115, used to obtain temperature values during testing.

4.4.3 CIS115 Design

Following the early iterations of the CIS107, an optimum pixel design was implemented in the CIS115 Revision A, finally culminating in the development of the CIS115 Revision B. These devices were then supplied to the CEI for electro-optical testing which is carried out using the same experimental setup used on the Rev A CIS115, Chapter 5:.

4.4.3.1 Back Illuminated

The CIS115 employs a back illuminated (BI) 4T CIS pixel. The front side of the device is deemed to be the side with the metal, wiring and transistors, therefore meaning a back illuminated pixel avoids passing light through this metal circuitry, improving transmission. The difference between front illumination and back illuminated sensors is shown in Figure 4-2, where sensitivity of front illuminated (FI) devices is greatly reduced by the semi-transparent regions (lenses, filters, and metal circuitry) on the device. As a result, one can expect an improved Fill Factor (FF) in BI devices compared to their FI counterparts due to a higher photosensitive area present on the pixel. Implementation of anti-reflective coating on FI detectors is also more difficult than in BI sensors meaning BI also offers improved absorption of light compared to the FI counterparts.

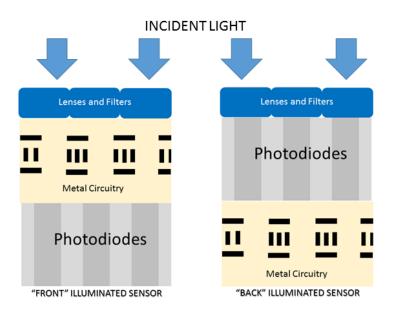


Figure 4-2: Back vs Front illuminated sensor.

4.4.3.2 Readout scheme

The readout scheme for the CIS115 follows a typical readout seen for a wide range of 4T CIS devices, which makes use of a feature known as Correlated Double Sampling (CDS) for noise reduction. CDS used in 4T CIS is a readout scheme used to reduce 'Johnson Noise' in 4T CIS which arises from the reset level of the Floating Diffusion (FD) being a slightly different potential every time it is reset. During readout the reset level of the FD can be sampled before readout (SHR Figure 4-4) and subtracted from the signal following readout (SHS Figure 4-4) removing the random noise arising from the varied reset potential. CDS is only achievable on pixels of 4T and above, as their 3T and lower counterparts do not possess the necessary architecture for on chip CDS.

The CIS115 readout involves the selection of a pixel (through row/column selection) that has been integrating charge to be read out. The readout of the device is operated on a row-by-row basis, where each pixel in a row is sequenced before moving onto the next row. Following the sampling of the FD reset level a Transfer Gate (TG) pulse transfers charge on the PPD in the pixel to the FD. The accumulated signal gives rise to a different voltage at the FD (due to the charge capacitance relationship V = Q/C (Fossum and Hondongwa 2014)) and is sampled through Sample Hold Signal (SHS). The readout pathway for a single CIS115 pixel is shown in Figure 4-3, where the CDS subtraction occurs at the 'CDS buffer' in the pixel. The

reset level of a pixel can be stored in these capacitors (through a Sample Hold Reset, SHR) along with the signal charge on the photodiode on the other capacitor (SHS).

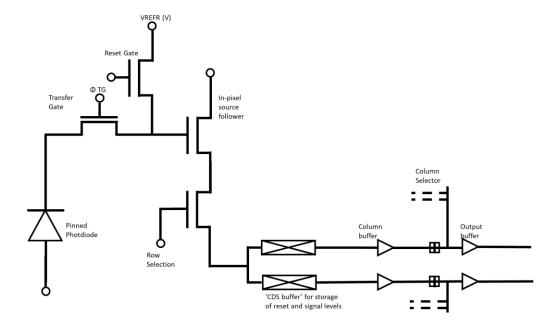


Figure 4-3: Readout pathway for a single pixel for the CIS115 adapted from (Soman et al. 2014)

Following this readout, the FD is reset, and the pixel can be read out again after a period of charge accumulation. The suggested readout for the CIS115 is shown in the CIS115 datasheet and is detailed in Figure 4-4 where durations for different stages in the readout sequence are denoted by t_x and typical times implemented on the CIS115 during CEI testing shown in Table 4-5.

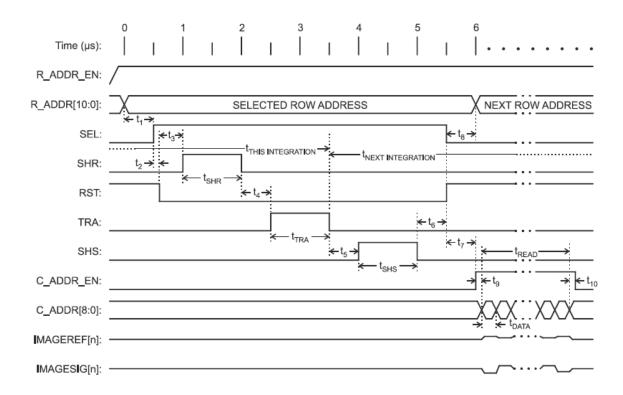


Figure 4-4: CIS115 recommended timing diagram taken from Teledyne e2v 2016.

Timing	Purpose	Value	Unit
t_1	Minimum setup time from stable row	0.5	μs
	address to SEL rising edge. Reset must be		
	high during this time and for the following t_2 .		
t ₂	Hold time on reset pulse to avoid soft reset	100	ns
	from SEL feed through		
t ₃	Suggested time between RST falling edge and	500	ns
	t _{SHR}		
t ₄	Suggested time between t_{SHR} and t_{TRA}	500	ns
t ₅	Suggested time between t_{TRA} and t_{SHS}	500	ns
t ₆	Suggested time between t _{SHS} and SEL falling	500	ns
	edge		
t ₇	Suggested time between SEL falling and	0.5	μs
	column address (C_ADDR_EN rising edges)		
t ₈	Minimum time between SEL falling edge and	0.5	μs
	row address change		

t ₉	Setup time of column address (C_ADDR_EN)	<100	ns
	to new column address input		
t ₁₀	Hold time from last column address to	<100	ns
	C_ADDR_EN falling edge		
t_{SHR}	Pulse time to sample reset level	1	μs
t _{TRA}	PPD to FD transfer pulse time	10	μs
t _{SHS}	Pulse time to sample signal after integration	1	μs
t _{READ}	Time to read out 376 columns	66.25	μs
t_{DATA}	Data time per pixel	161	ns
T _{THIS} INTEGRATION and	Effective integration time	~132	ms
t _{NEXT} INTEGRATION			

Table 4-5: Timings for CIS115 operation from CEI testing and taken from CIS115 datasheet.

4.5 Jovian Radiation Environment

4.5.1 Dominant source of radiation

Due to the Jovian magnetosphere, like other sizeable planets possessing a magnetosphere, a trapped particle radiation belt exists in the Jovian system. The dipole magnetic moment surrounding Jupiter is around $1.6 \times 10^{20} \, \text{T}$ m³ (around 20,000 times larger than Earth's (McDonald 2005)) and, due to the lack of solar wind pressure which could decrease the size of this magnetic field, encases all the Galilean satellites. In the Jovian system, these high levels of trapped particles interact with spacecraft within the system and damage the instruments within the spacecraft. JUICE is no different to this, and as such all instruments will be subject to high levels of radiation.

In the Jovian system, models that currently exist suggest a high level of trapped particles in the system with the source of this radiation dominated by heavy ions and high energy electron fluxes (Evans et al. 2013) that have become trapped in the magnetic field. These trapped particles are significantly more energetic than the ones found at Earth with heavy ion trapped particles arising from secretion of material into the atmosphere from the volcanic eruptions on Io which become ionised by photoionization from sunlight and electron impact ionisation (Morrison 1982).

4.5.1.1 Ionising Radiation in the Jovian Environment

Ionising radiation is charged radiation that can knock out electrons from atoms or molecules. In silicon imagers, incoming particles will need to possess energy of at least 3.6 eV (Scholze, Rabus, and Ulm 1998) in order to create an electron-hole pair in the silicon of the device. This ionising radiation can have many damaging effects in 4T CIS devices, and these effects are documented in 3.4.

In the Jovian system, ionisation will largely arise from the trapped proton and electron populations present in the Jovian radiation belt. During the mission lifetime shown in Table 4-1, the device was originally expected to accumulate a total of 100 krad (Si) TID (Soman et al. 2016) meaning characterisation of electro-optic performance of the CIS115 is required at least up to twice this TID, using the industry standard x2 factor of safety for testing.

4.5.1.2 Displacement damage in the Jovian Environment

Displacement damage is a result of energy deposition from particles incident on the material into the bulk of the semiconductor through interactions with the nuclei of the crystal lattice, which in the instance of the CIS115 is silicon. Displacement damage in CIS115 is expected to be dominated by high energy electrons and protons (which are abundant during the mission lifetime in the Jovian system) where TNID is expected to be a total fluence of 1×10^{10} protons cm⁻² (10 MeV equivalent) during mission lifetime.

4.6 Summary

From this chapter, it identifies that the CIS115 will be subject to a harsh radiation environment whilst operating on the JANUS camera. The device is expected to be irradiated with a total EOL fluence of approximately 1×10^{10} protons cm⁻² and total EOL ionising dose of 100 krad (Si). From the detailed goals of the JANUS camera on JUICE as stated in Table 4-2, characterisation of the CIS115 requires testing that is also carried out to these fluences and doses. To carry out these tests, certain experimental procedures and set up is required, which is introduced in the upcoming chapter.

4.7 References

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Chapter 5: Experimental procedures and setup

5.1 Intro

As discussed in 4.3.3, the CIS115 is the detector to be used for the JANUS camera on JUICE, where during its lifetime it will be subject to a harsh radiation environment. From Chapter 3:, degradations in the performance of the CIS115 can be expected following exposure to radiation. As a large part of the characterisation of the device revolves around testing the device performance at different equivalent stages of the JUICE mission, an experimental setup to obtain the electro-optical characteristics of the device before and after radiation and in varying conditions is essential.

5.2 Inherited equipment and experimental procedures

Experimental observations on the electro-optical performance of the CIS115 are carried out in a specifically designed experimental setup. This setup is based in the CEI labs at The Open University. The experimental setup was designed before the commencement of this PhD by the JANUS team at the OU, alongside front-end electronics development by $XCAM^{TM}$ Ltd. The setup is described in the upcoming sections.

5.2.1 Laboratory camera setup

During the JUICE mission, the JANUS camera is expected to be operated at -35±10°C, therefore, to replicate these conditions cooling equipment is required for the CIS115 test setup. The experimental setup (front) is shown in Figure 5-1. The CIS115 during testing is housed in a vacuum chamber. The temperature of the CIS115 is adjusted by a Lakeshore temperature controller, where cooling is provided by a CryoTigerTM and heating through a resistive element. Each CIS115 that is used for testing has a PT1000 glued to it (as seen in Figure 4-1, right). The PT1000 is a platinum resistance thermometer and the resistance across it will vary linearly respect to temperature, where at 0°C resistance will be measured as 1000Ω . This resistance can be monitored by a Lakeshore temperature controller, where it is converted to a temperature. Temperature adjustment is carried out by comparison of the temperature set point and the CIS115 actual temperature where a resistive heater is adjusted in a closed feedback loop to alter the temperature. The CIS115 is housed in a Printed Circuit Board operated via camera electronics designed by XCAMTM Ltd which is shown in Figure 5-2,

with camera input and output controlled though an XCAM™ Ltd drive electronics and power supply. Tests that require detector illumination is carried out by red LED (approximately 700 nm), where the light from this LED passes through a neutral density filter on the filter wheel to vary the intensity of the light from the LED. The typical filters used in setup is no filter (100%), and filters at 50%, 1% and 0.1%. During testing, to minimise light leakage, a dark sheet is placed over the setup and foil tape is applied to the seals on the vacuum and the connection of the filter wheel to the vacuum chamber.

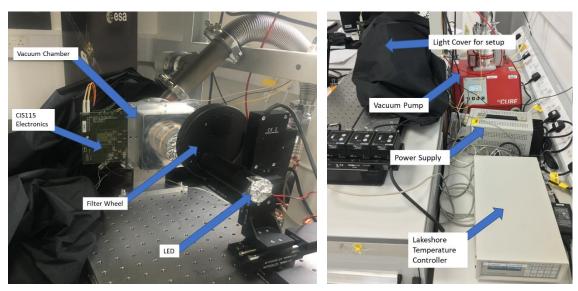


Figure 5-1: Experimental setup used at the CEI. Different components in the experimental setup are clearly labelled in the figure.

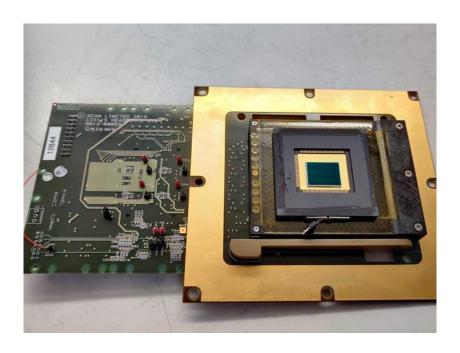


Figure 5-2: CIS115 shown contained within the front electronics designed by XCAM $^{\text{m}}$ where the copper coating around the ZIF socket is used for creating a vacuum seal with a rubber o-ring.

5.2.2 Experimental procedures

The CIS115 camera setup shown in Figure 5-1 is controlled and operated using MATLAB on a computer connected to the $XCAM^{TM}$ drive electronics box. During the testing presented in this thesis, the bias voltages shown in Table 5-1 were used, unless otherwise stated. The device readout timing sequence used is found in Figure 4-4.

Bias	Setting (V)	Comments
VPIX_1/ 2	3.3	Source Follower power supply for pixels
VREFR_1 / 2	3.3	Reset level power supply for pixels
VTRA	3.3	Supply used to drive transfer gate control
		gate
VRESET	3.8	Select and reset driver supply
VANA_OP 1 / 2	3.6	Analogue power supply to output buffers
VANA_RD 1 / 2	3.6	Analogue power supply to read circuits

Table 5-1: Power supply voltages and their explanation for the CIS115 (Teledyne e2v 2016)

The different tests used during this thesis are described in more detail in this section. The capability of the cooling setup means that all tests can be carried out at approximately -50°C to -25°C and 25°C to 40°C. As a result of the large temperature regime available during testing,

experimental methods presented here will be expressed without any temperature, as this will be stated explicitly when results of these tests are analysed and presented.

5.2.2.1 Image Lag

Image lag testing carried out on the CIS115 involves a specific image acquisition procedure unique to image lag data collection. During image lag data acquisition, only the first 200 rows are read out for the detector, meaning that the total image area is only 200 by 1504 pixels. In this windowed area, 10 different frames of capture are taken. The first five of these windowed captures are taken with the LED on and the last five are taken with the LED off. These two imaging types allows for a bright to dark transition which will permit for the study of discharging lag in the CIS115. Each of these ten frames are taken with identical timing sequences, integration times, bias voltages, and temperature.

In addition to this, all ten frames are repeated 50 times. In calculation of image lag of the detector, the median of these 50 frames is used. During data collection, median images are output by the script which can be used to determine if the test is running correctly. An example figure for the output from the CIS115 using this acquisition method is shown in Figure 5-3.

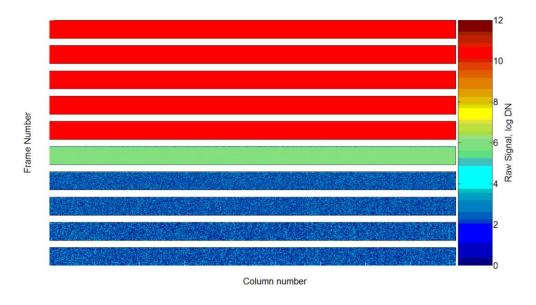


Figure 5-3: Median image lag of the CIS115.

5.2.2.2 Dark Signal

Dark signal characterisation requires the integration of the detector devoid of any illumination. In this data acquisition mode, full frames of the detector are read out at a range of integration times, where 20 repeat measurements are taken at each integration time. The relationship between the dark signal and the integration time on a mean or a pixel-by-pixel basis can then be used to express the dark current of the CIS115, where the gradient of the dark signal versus integration time is the dark current of the detector.

5.2.2.3 Noise

Read noise measurements use the repeated measurement procedure. In noise data collection, ten full frame readouts of the CIS115 are taken. At each of the ten full frame readouts, the image acquisition is repeated 20 times, with each full frame readout taken at short integration times. To ensure that the measurement accurately represents the readout noise of the detector, there is a reset of the photodiode before the reset, transfer, and signal sampling of the pixels. This will ensure that there is no contribution on the signal from dark current or stray light (provided the setup does not have any major defects which allow in an abundance of stray light). The standard deviation of a pixel value across the ten images can then be used to express the noise of the device. In the CIS115 this can either be represented as a median or mean of all the pixels or displayed in a noise histogram across all pixels.

5.2.2.4 Random Telegraph Signal

Random Telegraph Signal (RTS) data acquisition involves the collection of dark frames of the CIS115 for 2000 readouts. The large number of readouts permits for a statistically significant data set to be created in the time domain to observe any RTS transitions within a pixel. Each pixel is read out for a given integration time (set to be 0.1 s, 1 s or 10 s) meaning that the pixel is read out for a total of 200 s, 2000 s or 20,000 s, enough to observe RTS transitions within a pixel.

5.2.2.5 Mean-Variance Curve

The Photon Transfer Curve or PTC (sometimes called the mean-variance curve) is a method of extraction of a conversion gain of an image sensor. A PTC is typically a graph of the log signal (x-axis) against the log noise (y-axis) of the device/pixels whereas a mean-variance

curve is the mean signal (x-axis) against the mean variance (y-axis). Typically, a PTC is made up of four distinct regions; the readout noise floor; shot noise region; fixed pattern noise region and saturation. The photon transfer curve is further described in Section 2.6.2

Mean-variance data acquisition for the CIS115 involves the full readout of the CIS115 under illumination to ascertain the device responsivity. The sensor is illuminated by the LED shown in the CIS115 camera setup with a rough flat field. Images are taken at a range of illumination times from 0.001 s, extending to longer integration times (approximately 6 s) with 20 images being taken at each integration time. The purpose of the large range of integration times is to ensure that one can collect data points from the readout noise dominated region of the PTC all the way to above the FWC of the detector.

5.2.2.6 Pinning Voltage Characterisation

The pinning potential of the photodiode in the CIS115 is measured through determining the voltage at which signal is injected from the floating diffusion to the photodiode across the transfer gate. This test is carried out by varying the VREFR voltage (see Figure 4-3) applied to the reset transistor as seen in Figure 4-3. This VREFR will inject current through the reset transistor of the pixel (whilst Φ TG and VRESET is held high) to the floating diffusion. When the injection voltage is low enough, charge can be injected directly onto the PPD which can subsequently be read out as output signal. The VREFR voltage at which the charge is first injected onto the PPD is the pinning voltage of the PPD.

5.3 Proton irradiated devices

The proton irradiation was carried out at the Proton Irradiation Facility (PIF) at the Paul Scherrer Institute (PSI) close to Zurich in Switzerland by a member of the JUICE team (M.R. Soman, E. Allanwood, 2017). Devices were irradiated with protons of energy 72.8 MeV using a 58 mm diameter collimator with a flux of approximately $2x10^7$ protons s^{-1} cm⁻².

The devices used for this test were placed one at a time in the beam and irradiated. The devices were irradiated as described in Table 5-2, with the fluence level being related to the mission expected fluences.

Device	Irradiation	Effective	Irradiation	Lifetime
	Fluence,	Fluence,	Time, s	Factor
	72.8 MeV, p cm ⁻²	10 MeV, p cm ⁻²		
15901-10-12	1.038 × 10 ¹⁰	5×10 ⁹	520	Half EOL
15901-17-03	1.039×10^{10}	5×10 ⁹	640	Half EOL
15901-10-13	2.077 × 10 ¹⁰	1×10¹0	1050	EOL
15901-10-19	4.152 ×10 ¹⁰	2×10 ¹⁰	2097	Twice EOL

Table 5-2: Delivered fluence levels during the proton radiation.

5.4 Neutron Irradiation

In addition to a proton irradiation a neutron irradiation was also carried out on the CIS115. This was carried out at the National Physical Laboratory (NPL) in London and used a Californium 252 (Cf²⁵²) source for the irradiation. This was carried out on one CIS115 device, (CIS115-15901-12-04) and the irradiation was to a total fluence of 5.25×10^9 1 MeV neutrons cm⁻². This was calculated to a proton 10 MeV effective fluence of 1.09×10^9 p cm⁻².

5.5 Gamma campaign

To replicate the conditions that the CIS115 is expected to face in the Jovian system, a gamma irradiation campaign is carried out on the CIS115. A key contribution of this doctoral work involved the planning and delivery of the gamma irradiation campaign, and therefore will be described in more detail in the following sections.

5.5.1 Facility

The gamma irradiation of the CIS115 was carried out at the ESA-ESTEC Co-60 facility in Noordwijk, Netherlands. The facility regularly updates the Co-60 source that it uses for irradiations, and as such was loaded with a 2000 Curie Co-60 source in May 2016 (Agency, 2016).

Cobalt-60 is a radioactive nuclide with a half-life of approximately 5.25 years which decays through beta minus emission to excited Ni-60. This excited Ni nucleus has a probability of emitting several gamma photons in a range of energies with varying prevalence where the most common emission (99% emission probability) occurs at energies of 1.173 MeV and 1.332 MeV. The source at the facility is stored in a specifically designed double-welded steel container with integral lead shielding. During irradiation, the source is raised out of the

chamber to the irradiation position, with gamma rays exiting the irradiator unit through a collimator window. Total dose and dose rate measurements in the irradiation cell is carried out via a dosimeter placed in the same physical plane as the items being irradiated with the layout of the cell shown in Figure 5-4.



Figure 5-4: ESTEC Co-60 Radiation Cell where the steel container containing the source is shown in the foreground, with a positioning trolley shown capable of positioning DUTs between 40 cm and 815 cm. The CIS115 during testing are placed 55 cm from the source.

5.5.2 Irradiation

The CIS115s used in the irradiation were placed in the cell in the positions as shown in Figure 5-5, where they are left in the cell for a given time (dictated by the calculated dose rate received at this distance from the source) to accumulate the required levels of TID. In total five CIS115s were irradiated at the facility.

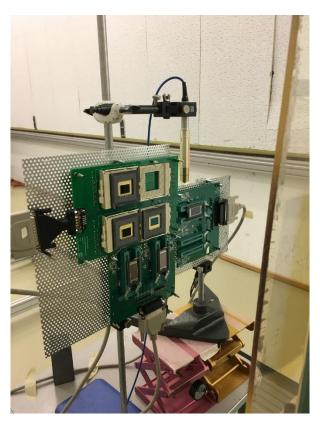


Figure 5-5: The CIS115 set up for being placed in the irradiation cell. Devices are placed on a bias board with their cover glass removed and left for a specified period to accumulate the correct dosages on each detector.

The devices under test (DUTs) for irradiation and their doses are shown in Table 5-3.

Device	Irradiation Dose
15901-10-11	50.0 ± 2.1 krad
15901-17-02	50.0 ± 2.1 krad
15901-17-13	100.4 ± 4.2 krad
15901-17-19	100.4 ± 4.2 krad
15901-10-03	200.4 ± 8.4 krad

Table 5-3: Delivered gamma doses from the gamma irradiation. These doses along with their error were suppled in a private communication from the ESTEC Co-60 facility

The irradiation was approximately at around 55 cm from the source acquiring a total dose of approximately 203 krad from an irradiation area of 484 cm^2 (22 cm by 22 cm). Under the assumption that the radiation is coming from a point source, at the extremity of the irradiation area one can expect the dose to be approximately 93% of what is expected at the centre of the irradiation area. Due to the accessibility of the Co-60 cell, to achieve the required

doses for the five detectors, the irradiation was broken down into three time periods and the schedule is shown in Figure 5-6

	Date & Time								
Davisa	20-Jun-17				21-Jun-17			7	
Device	09	09:02		:02 17:48 10:20		:20	18	3:29	Dose
	IN	OUT	IN	OUT	IN	OUT	IN	OUT	
15901-10-11									50 krad
15901-17-02									50 krad
15901-10-03	-10-03						200 krad		
15901-17-13									100 krad
15901-17-19									100 krad

Figure 5-6: Schedule for placing and removing the devices in the radiation cell.

Following standard procedures for the research group at the time, the irradiation was undertaken with no shielding material or cover glass placed in front of the CIS115 during irradiation. The lack of material reduces the dose received at the exposed surface of the CIS115, as the chain of secondary particles produced by the gamma photons require a certain thickness to build up into a depth-dose relationship known as Charged Particle Equilibrium (CPE). The dosimeter used incorporates a sheathing material that ensures CPE is reached, and so it is possible that the dose delivered at the most sensitive layers of the CIS115 (at approximately $10~\mu m$ depth) were in fact lower than those measured by the dosimeter. To understand the differences between dose delivered and dose at the sensitive volume of the sensor without shielding material, detailed Monte Carlo particle transport simulations (e.g., Geant4) could be undertaken, or further comparative experimental measurements, however these are beyond the scope of this thesis and the dosimeter measured values have been used in the analysis that follows.

5.5.3 Bias board design

During irradiation, the devices were biased to mimic the irradiation conditions of the device during operation in the Jovian system and since TID effects on the detector may be worsened when biased (Wang et al. 2018). To bias the devices, a board required fabrication. This board was designed as part of the preparation of this thesis in DesignSpark® PCB, printed and periphery parts soldered to it at The Open University. This board was designed to supply the CIS115 with certain bias voltages, where during the radiation testing the voltages were set on the board using a power supply. Probing these voltages using a multimeter confirmed their values and are presented in Table 5-4, which match the typical operational voltages shown in Table 5-1.

Bias	Datasheet	Measured
	Value	Value
VPIX	3.3V	3.301V
VREFR	2.9V	2.905V
VTRA	3.3V	3.308V
VANA	3.6V	3.595V
VRESET	3.9V	3.90V
ENABLE	3.3V	-
IPIX	14μΑ	14.0μΑ
IREAD	60μΑ	60.2μΑ

Table 5-4: Bias voltages values used for CIS115 during gamma irradiation testing.

The bias board shown in Figure 5-7 was designed with the capability to bias up to a maximum of four devices at any one time. Although only a maximum of three CIS115s were present in the gamma cell at any one point, the board permits for the thermal annealing of four devices simultaneously.

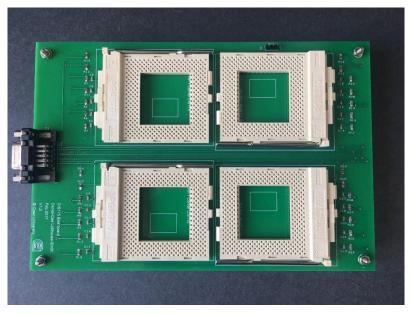


Figure 5-7: Bias board designed in DesignSpark® PCB and populated at The Open University. Modified 370-way socket were used to connect to the CIS115's package pins.

5.6 Annealing setup

As part of the device radiation qualification for the JUICE environment, thermal annealing testing of the CIS115 is carried out at The Open University. This testing requires the detector to be heated at a temperature of 100 °C for 168 hours, where heating is carried out using the setup that can be seen in Figure 5-8. To measure the temperature during the testing, the PT1000 that is glued to the left side of all CIS115 detectors is connected to circuitry which can measure the resistance on the PT1000 and hence the temperature of the device. In circumstances where annealing involves more than one device, only one of the devices annealed is connected to the output circuitry and the temperature is assumed to be uniform inside the whole annealing oven.



Figure 5-8: The annealing setup used for the CIS115. Inside the oven (left) where the CIS115 is contained within the bias board to be biased during anneal, and the external view of the oven (right). The proton device annealing does not require a power supply as the annealing is carried out unbiased.

The temperature logging equipment is shown in Figure 5-9. This uses a potential divider in series with a PT1000, where the voltage across the PT1000 is monitored by the picologger. This voltage is converted into a temperature using the resistance temperature relationship for a PT1000 that can then be plotted to confirm the oven maintains a consistent temperature during the anneal. To mimic their respective radiation testing, the proton irradiated devices were annealed without bias, and the gamma irradiated devices were annealed with bias.

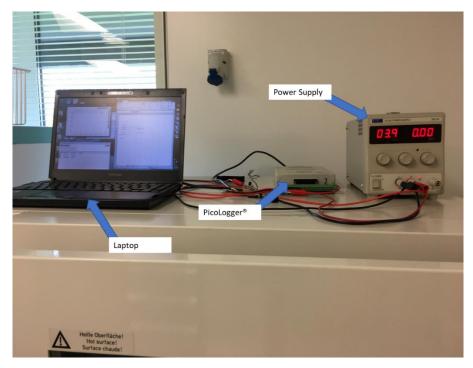


Figure 5-9: Setup outside of the oven used for supplying power supply for bias and for measuring the temperature of the detectors using a PicoLogger®.

5.7 Summary

In this chapter, the experimental setup that is used to carry out testing for the CIS115 is introduced. This was inherited, where it was designed and commissioned prior to the commencement of this work. This setup allowed for testing on the CIS115 to be carried out in a vacuum at a range of temperatures. This chapter also specified the bias voltages that are used in operation of the CIS115 following the timing sequences introduced in Chapter 4:.

Following on from the setup, this chapter also introduced key experimental procedures for the CIS115 that are used in further testing. To acquire the necessary data to study electro optical parameters of the CIS115, experimental procedures are introduced here. These include image lag, dark signal, noise analysis, random telegraph signal, mean variance and pinning potential. These studies will be included in later parts of the thesis.

To mimic the conditions, the detector is expected to be subject to during the mission lifetime, irradiation of the CIS115 is required. This chapter introduces two different irradiations carried out on the CIS115. The first is a proton irradiation and the second is a gamma irradiation. More details are available on the gamma irradiation since this irradiation was carried out as part of the preparation of this thesis.

This chapter concludes with the introduction of an annealing setup used to thermally anneal the detector which replicates the long-term annealing the device may undergo during operation. Alongside this, it presents a custom designed "bias board" used during both the anneal and the gamma campaign to bias the detector.

From the works presented in this chapter, full characterisation of the CIS115 is possible to determine its capabilities when being used as the JANUS camera on JUICE. These experimental procedures are first used to complete an initial characterisation of the device, which forms the focus of the upcoming chapter.

5.8 References

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Chapter 6: Initial Sensor Characterisation

It is important to document and characterise the key electro-optical aspects of the CIS115 to better understand how the device is expected to operate during the JUICE mission. Characterisation typically involves many baseline tests using the electromagnetic (EM) radiation that the device will be using for imagery which in the case of the CIS115 is visible light.

To obtain the CIS115 performance metrics, initial sensor characterisation using numerous experimental methods (detailed in 5.2.2) were carried out. Results presented in this section consist of the analysis of a control detector (i.e., the device has not been subjected to damaging radiation and thus can be used to give a good understanding of the behaviour of Beginning Of Life (BOL) performance). The control device, CIS115-15901-13-08 (hereafter referred to as 13-08), is a Revision B version of the CIS115, the same type as the flight model.

The testing setup that was used to characterise the detector (as discussed in Chapter 5:) was inherited, however the analysis methods that are described in this chapter were carried out independently from the development of the equipment.

The control CIS115 is shown in Figure 6-1. The main parameters of the CIS115 are that the device is a back illuminated 4T CIS image sensor, with 1504 by 2000 49 μ m² pixels with 4 parallel analogue output ports.

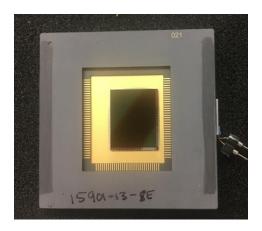


Figure 6-1: CIS115 13-08 used in testing, where a PT1000 is glued to the right side of the detector to measure device temperature during testing.

6.1 Experimental Setup

The experimental setup for specific tests is shown in Figure 5-1. The mission operational temperature of the detector in the JANUS camera is -35±10°C. The characterisation of the CIS115 was carried out at a range of temperatures in two regimes coins as above room temperature (30°C to 40°C in 2.5°C increments) and mission temperature regime (-30 to 50°C in 5°C increments, however this regime may also include measurements at 2.5°C increments between -40°C and -25°C).

6.2 Image Sensor performance metrics

Performance metrics for image sensors are key in understanding how the device can be expected to perform when making scientific observations. Key operational metrics for the CIS115 are examined and parameterised for the control device here, with relation to the specifications of the JANUS camera on JUICE also discussed. The parameters that will be discussed are.

- System Gain
- Readout Noise
- Fixed Pattern Noise
- Dark Signal
- Image Lag
- Photodiode Pinning Potential

6.2.1 System Gain

Conversion Gain is an important metric in image sensors as it describes how the output signal of a device in digital numbers is related to an output charge (in electrons). This can be done in 4T CIS through the Photon Transfer Curve (PTC) or mean-variance curve, which is described here, with results from CIS115 13-08 also documented.

6.2.1.1 Photon Transfer Curve

For the 13-08 control CIS115, an example mean variance curve is shown in Figure 6-2. The gain is calculated on a pixel-by-pixel basis for data points that exist in the region bounded by the red lines on the figure, where gain is equal to the inverse gradient in this region. From this analysis (at a temperature of $40\,^{\circ}$ C) it results in a mean conversion gain across the device of 1.84 ± 0.03 e-/DN, where error on this value is calculated using the standard error on the

mean. This value is used to convert digital numbers to electrons for other figures in this chapter. Moreover, other OU testing supports this conclusion with system gain calculated using the characteristic emission from an ⁵⁵Fe source.

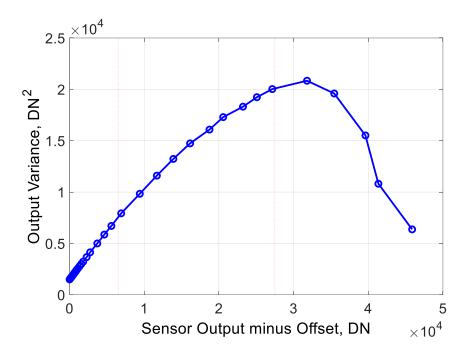


Figure 6-2: Mean-Variance plot for the CIS115 as an average across the pixels in the device. Calculating the inverse gradient of pixels with output signal bound between the two red regions gives the conversion gain of the device.

6.2.2 Noise Sources

6.2.2.1 Readout Noise

The readout noise of an image sensor is the noise in the output signal that is contributed by the readout chain of the device, without illumination. Due to the nature of CIS, readout noise in the CIS115 is calculated on a pixel-by-pixel basis. The readout noise distribution is measured at the full mission temperatures and is shown in Figure 6-3. Two main features can be observed from the plot, a Gaussian envelope which fits to most of the pixels in the device and an exponential "tail" of pixels with increasing read noise. From the Gaussian fit the peak noise is approximately 5 e-RMS across mission temperatures. This suggests that the source behind this noise is largely independent of the temperature. The second feature seen in the plot is an exponential-like tail of pixels which extend to higher values (up to approximately 20 e-RMS). This tail does show a small change with temperature, with lower noise values occurring at higher temperatures.

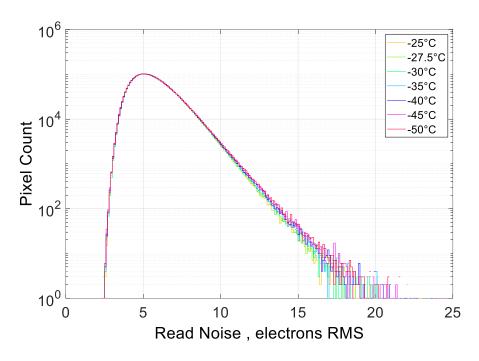


Figure 6-3: Readout noise of CIS115 13-08 control across the mission temperature range. The noise behaves as a combination of a Gaussian and an exponential distribution, with a peak in the distribution occurring at 5 e⁻RMS. The appearance of this distribution is largely the same for every temperature with only the 'pixel tail' showing variation over the temperatures studied.

Under the assumption that the characterisation carried out on CIS115 13-08 is representative of flight model devices, the peak noise can be concluded to be 5 e $^{-}$ RMS. As mentioned in Table 4-4, the mean readout noise of the CIS115 needs to be less than 8 e $^{-}$ RMS. Therefore, the read noise of the CIS115 can further be represented in terms of a cumulative histogram, which highlights the number of pixels that have a noise at or below 8 e $^{-}$ RMS. This is shown in Figure 6-4, where the vertical red line is at a value of 8 e $^{-}$ RMS noise (the qualification requirements discussed in Table 4-4). From this plot and using the standard error on the mean, it is identified that 93.62 \pm 0.04 % of all pixels have noise which is less than 8 e $^{-}$ RMS.

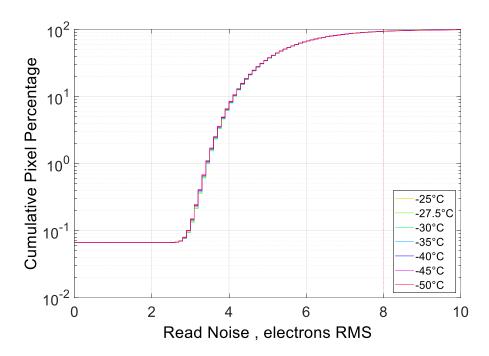


Figure 6-4: Cumulative read noise of CIS115 13-08 control in the cold temperature regime. The vertical red line represents a noise value of 8 e RMS. 93.62% of pixels have a noise value at or below this point.

The readout noise of the detector therefore shows it is within specification, however, this is not the only noise present in CIS115 output, and other noise sources will be discussed further in the upcoming sections.

6.2.2.2 Fixed Pattern Noise

Fixed Pattern Noise (FPN) in 4T CIS is a noise source that arises from spatial variations in the output of the device. This FPN can be seen in the left-hand plot of Figure 6-5 which is a simple readout of the detector at -50°C in dark conditions. The pixels all suffer from their own fixed offset that can be subtracted to remove FPN for future data analysis, where the offset subtracted frame is seen in Figure 6-5, right. This data has therefore been fixed pattern offset corrected, with a column-based component of FPN seen in the left-hand side plot in Figure 6-5 removed.

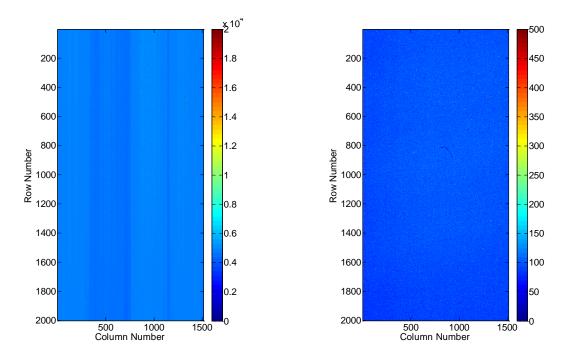


Figure 6-5: Fixed Pattern Noise schemes of the CIS115. Where on the left, the column FPN can be seen in a dark image of the detector. The figure on the right will therefore be dominated by Photo Response Non-Uniformity, due to the offset subtraction.

The response of the detector in the absence of light has been discussed here briefly but as discussed in 2.6.1.3 dark current can also arise when the detector is integrated in dark conditions.

6.2.2.3 Dark Current

Dark current in the CIS115 is typically expressed at a specific temperature. Dark Current (DC) is equal to the dark signal over a given time. In a plot of dark signal against integration time, the gradient of the linear region is equal to the dark current. Dark current performance of an imager is usually expressed as mean value over the image area of the device. For the CIS115 13-08 this mean DC for the CIS115 is shown in Figure 6-6.

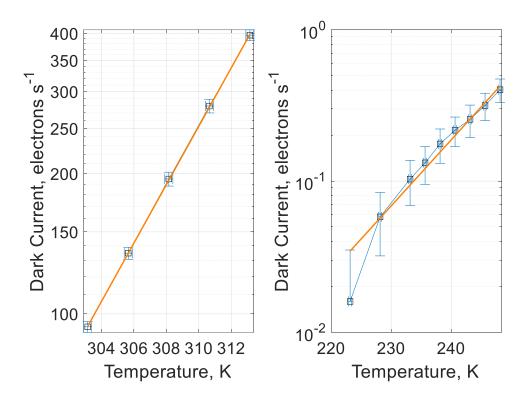


Figure 6-6: Dark current of the CIS115 over the full temperature range studied. The behaviour in the two temperature regimes are fitted with separate exponential functions. Error bars are calculated from the standard error on the mean.

Dark current in the CIS115 at mission temperatures is <1 e⁻s⁻¹ for each temperature studied. As a result of this, one can expect the noise arising from DC in an image taken at this temperature with high illumination levels and low integration times to be negligible. In Table 4-4 the mission requirement for DC is shown at 293 K (20°C) to be <90 e⁻s⁻¹. The 'warm' regime testing has a minimum temperature of 303 K, but an exponential fit to the mean dark current performance in this region (shown in Figure 6-6, the orange line on the warm data) will mean the dark current at 293 K can be determined.

Temperature (°C)	30	32.5	35	37.5	40
Mean DC (e-s-1)	93.8	135.0	194.8	279.4	396.6
Error on DC (e-s-1)	2.5	4.0	6.7	9.4	10.6

Table 6-1: Mean dark current Values of CIS115 13-08 in the 'warm' temperature regime. Mean DC represents the generation rate of dark current in electrons/s.

The DC rate in Table 6-1 shows the mean DC generation rate of the control CIS115 device in the 'warm' temperature regime. McGrath et al (McGrath et al. 2018) suggest that a doubling temperature exists in 4T CIS DC values. From Table 6-1, it appears that the dark current

doubles approximately every 5 K, where the exponential fit in the warm regime from Figure 6-6 confirms this doubling temperature to be 4.83 K. Therefore, from the exponential relationship the dark current at 20°C is calculated to be 22.5 e·s·¹. At mission temperatures from Figure 6-6, the dark current for the CIS115 is shown to be less than 1 e·s·¹ and at 293 K approximately 23 e·s·¹. The mission requirements in Table 4-4 confirm the CIS115 will meet the BOL JANUS criteria for dark current.

Although the dark current is often represented in terms of the average pixel behaviour across the whole device, the mean dark current may not completely represent the DC behaviour and therefore investigation of the DC spectrum at each temperature can be used to identify the DC on a pixel-by-pixel basis. At mission temperatures the DC spectrum is shown in Figure 6-7. The lowest DC clearly correlates with the lowest temperature, where the width of the distribution is smaller at lower temperatures. These distributions are assumed to be Gaussian, and the fit parameters are shown in Table 6-2. Figure 6-7 however highlights that the pixel response is not completely governed by a Gaussian but includes a small exponential-like tail too. This can be attributed to defect pixels in the device with unusually high DC.

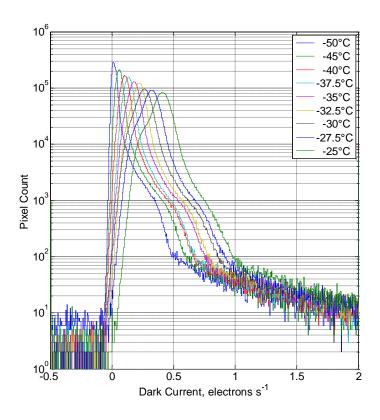


Figure 6-7: Dark current spectrum of the device at mission temperatures. Distributions at each temperature can be approximated to be Gaussian distributions, characterising the DC generation from a single population. Increasing temperature shows the widening of this DC distribution, standard deviation of these distributions increases along with temperature.

Temp	-50	-45	-40	-37.5	-35	-32.5	-30	-27.5	-25
(°C)									
Peak DC	0.016	0.058	0.103	0.132	0.176	0.217	0.256	0.316	0.402
(e-s ⁻¹)									
σ (e-s-1)	0.019	0.026	0.034	0.037	0.045	0.048	0.062	0.065	0.071

Table 6-2: Peak dark current and standard deviation values extracted from Gaussian fits on the 'cold' regime data.

The DC spectrum above room temperature is shown in Figure 6-8. It clearly indicates that on a pixel-by-pixel basis, the main population of DC increases, suggesting the increase in DC with respect to temperature is a global shift of all pixels in the device. Furthermore, the DC distribution widens as the temperature increases (like the behaviour observed at mission temperatures), with the whole population shifting to higher DC. The mean DC and the standard deviation are shown in Table 6-3. These values are approximately the same as the

mean values shown in Table 6-1, suggesting that the Gaussian distribution is an accurate representation of the DC. Interestingly, the distributions show small peaks and an exponential tail which exist outside the Gaussian envelope of the DC. Like at mission temperatures, this is thought to be because of defect pixels. Investigation of the DC image will be able to determine how the defect pixels are distributed across the device.

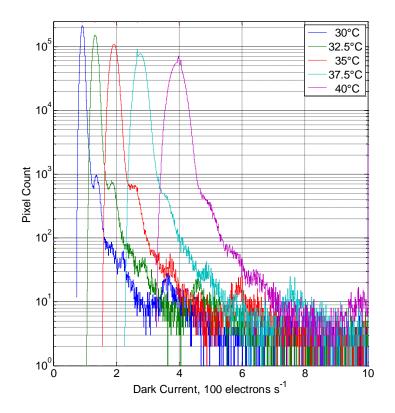


Figure 6-8: Dark Current Spectrum of the device above room temperature. Distributions at each temperature can be approximated by a Gaussian. Increasing temperature shows the widening of this DC distribution i.e., an increase of the standard deviation.

Temp (°C)	30	32.5	35	37.5	40
Peak DC (e-s-1)	92.0	132.8	192.2	276.0	393.4
σ (e-s ⁻¹)	5.4	7.7	10.8	14.9	20.0

Table 6-3: Peak dark current values extracted from Gaussian fits at above room temperature data along with the standard deviation of the fits.

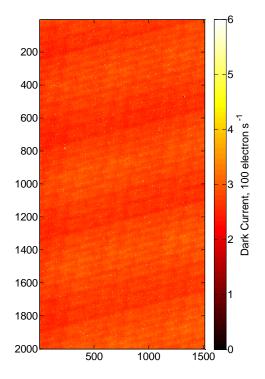
The dark current defect pixels can be determined as pixels that have a dark current over 3σ greater than the peak dark current (from Figure 6-8) at approximately 267 e-s-1. Above room

temperature, the pixels outside the main Gaussian envelope are shown in Table 6-4. Although the mean response of the DC is shown to increase with temperature, the size of this tail remains largely the same with shift in temperature.

Temperature (°C)	30	32.5	35	37.5	40
Dark Current Tail	2.55	2.52	2.54	2.55	2.65
Pixel Percentage					

Table 6-4: Percentage of pixels in the image that are 3σ outside of the main Gaussian envelope.

Since the number of pixels with dark current greater than 3 σ outside the main Gaussian envelope is independent of temperature, another point of interest is to investigate the location of these high dark current pixels. This is highlighted in Figure 6-9, where it shows the dark current of pixels at 37.5 °C on the left and then the high dark current pixels at this temperature on the right. The figure suggests the tail pixels appear to be distributed in four regions on the device suggesting no preferential location of the high dark current pixels across the four output regions of the device.



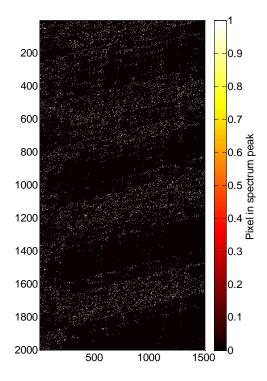


Figure 6-9: Dark current Image at 37.5°C. The left plot shows the DC of the whole device, with DC in the device resulting in a pattern across the imaging area. The right plot shows the location of the pixels that exist in the peak at around 267 electrons s^{-1} .

The dark current image shown in Figure 6-9 (left) shows a pattern possibly due to the back illumination process employed by Teledyne e2v, where a UV laser raster scans across the wafer (to anneal the implantation of boron on the back surface) and causes this pattern. This pattern is common on BOL Teledyne e2v CCD and CIS. McGrath et al. 2018 suggests that a source of dark current can be due to the diffusion from the back interface. Therefore, this pattern suggests that a dominant source in the dark current in BOL CIS115 is from back interface diffusion.

6.2.2.4 Image Lag

Image lag in the device is described in 2.6.1.4 where it is defined as incomplete transfer of charge out of the pixel from the PPD to the FD. This can be for a host of reasons as described in 2.6.1.4.

The testing procedure for the image lag is shown in 5.2.2.1 with transfer gate on (Φ TG) voltage of 3.3 V and a transfer on time of 10 μ s. In Goiffon et al. 2012 it is suggested that very low levels of image lag at BOL imply that the device is devoid of any major traps, pockets or potential barriers. This means that image lag will be governed by spill-back, poor charge drifts out of the PPD and improper bias voltage selection. The CIS115 however profits from high levels of device heritage, where the design of the PPD was studied in the CIS107 and optimised for the CIS115. This means that for the CIS115 image lag at Beginning of Life (BOL) is expected to be dominated by spill-back effects and poor bias voltage selection.

Image lag for the CIS115 13-08 is shown at mission temperatures in Figure 6-10. From the results presented in the figure, there appears to be three regimes for the image lag of the CIS115: one at signal levels below approximately 0.5×10^4 electrons signal where the image lag appears independent of signal level, a transition between 0.5×10^4 electrons signal and 1×10^4 electrons where there is a linear dependence between signal and image lag and a final region occurring beyond 1.5×10^4 electrons signal where gradient of the relationship between image lag and signal level is significantly reduced. The transitional point between the first two regimes is referred to as the image lag knee point. Below this knee-point the image lag response is shown to be approximately constant for signal, and above the knee point (but below the third region) the image lag appears to have a linear proportionality between the signal level and image lag. The image lag is therefore thought to be governed by three different responses, two above this knee-point and one below.

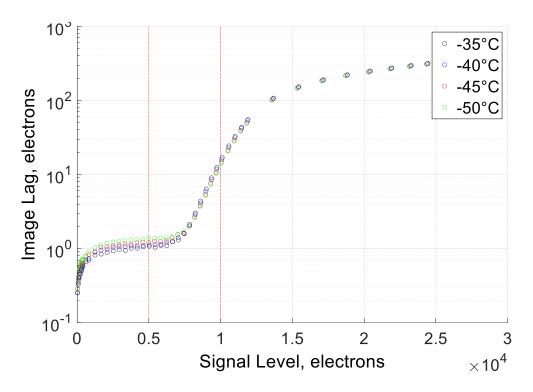


Figure 6-10: Signal level against Image lag in electrons for control device 13-08 at mission temperatures. Low illumination image lag is approximately constant. Above knee-point image lag increases in a linear fashion.

Below the knee point in Figure 6-10, the low levels of image lag (<1 e⁻) suggest lag is not limited by a potential barrier or pocket as seen in (Goiffon et al. 2012) and as such the lag mechanism is concluded to be dominated by imperfect diffusion of the electrons out of the PPD. Electrons stored in the PPD possessing greater energy will more easily diffuse out of the PPD, highlighting the trend that at higher temperature the increased thermal energy of the electrons increases the speed of charge transfer, reducing image lag.

Above the knee point the device is spill-back dominated. This means that charge transferred to the FD from the PPD during readout spills back onto the PPD and is not read out until the subsequent frame. The rate of spill back is proportional to the initial charge that is present in the device. As a result of this, the image lag is expected to increase linearly with the signal level incident on the device, which is seen in Figure 6-10 above the knee-point.

Table 6-5 presents image lag at a value of 50% of the linear charge capacity (Q_{LIN}) of a pixel in the device. The value of Q_{LIN} (taken from the Teledyne e2v datasheet) is 27,000 e-/pixel and therefore image lag is expressed at 13,500 e-. The image lag at this signal level is computed through a linear fit to the data bound by the dashed red lines in Figure 6-10 and results are shown in Table 6-5.

Temperature	-35	-40	-45	-50
(°C)				
Image Lag (e ⁻)	105.0	104.0	102.4	101.0
Image Lag (%)	0.78	0.77	0.76	0.75

Table 6-5: Image Lag in % and e^- at half Q_{LIN} for CIS115

The data shows that at the mission temperature of -35°C the image lag at ½ Q_{LIN} is less than 1%, meaning that the device at BOL will comfortably meet the mission requirements of 1% lag. The trend observed in Table 6-5 is fitted with a linear function and from this, one can determine that at the highest operational temperature of the JANUS camera (-25°C), the lag at 50% Q_{LIN} will remain below the 1% threshold. The maximum operational temperature of JANUS was not used in CIS115 characterisation. This is because of the characterisation testing carried out on the CIS115 showing that at -35°C the device operates well within the tolerable ranges for the JANUS camera. As a result, the maximum operational temperature was raised to reduce the power requirements of the cooling system within the JANUS camera. Initial characterisation of the image lag is stated here, with more detailed characterisation of image lag in the device shown in Chapter 8: and Chapter 9: with details of the performance following TID and TNID also included. Under the assumption that lag of approximately 100 e- is shot noise limited, one can expect the noise contribution to the overall noise budget to be 10 e- RMS. However, at this signal level (13,500 e-) the shot noise on this signal level will be approximately 116 e- RMS, suggesting that at this signal level, the overall noise profile on the signal of the device will be dominated by the shot noise on the signal electrons.

6.2.3 Photodiode Pinning Potential

The method for extraction of the photodiode pinning potential is discussed in 5.2.2.6 where the results for the initial characterisation device are shown here. The pinning potential for CIS115-13-08 is extracted from the x-intercept of the region of Figure 6-11 (approximately between 0.8V and 1.3V, shown by the blue line). This gives a mean pinning potential for one row of pixels in the CIS115 as 1.35±0.01 V.

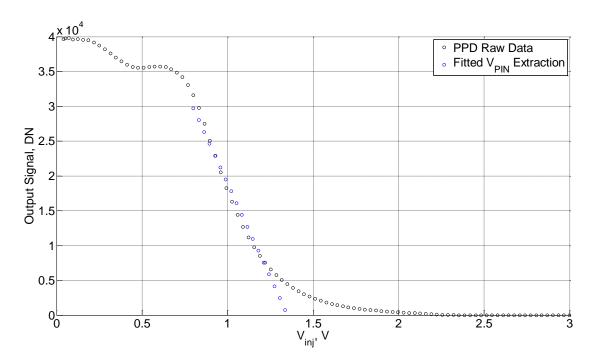


Figure 6-11: Pinning Potential for the CIS115 for given charge injection via the reset transistor, output node and transfer transistor. V_{pin} is extracted from the region of the graph where the value of V_{inj} is approximately between 0.8V and 1.5V in the value of x and y as the x-intercept.

6.3 Summary

Characterisation of a BOL CIS115-13-08 has resulted in the documentation of a range of features on the CIS115. These electro-optical parameters are all useful factors in describing the behaviour of the CIS115. In this chapter mission requirements have been compared with the measured performance of the device. This comparison of key electro optical parameters is presented in Table 6-6. This chapter shows that for the readout noise, dark current and image lag, the detector operates within the mission requirements for the JANUS camera on JUICE.

Test	Mission	Datasheet Value	Calculated value
	Requirement		
Mean Readout Noise	<8 e- RMS	5 e- RMS	5 e- RMS
Dark Current (20° C)	<90 e- s-1	20 e- s-1	22.4 e ⁻ s ⁻¹
Image Lag at ½Q _{LIN}	1%	1%	0.78%

Table 6-6: Electro optical performance characteristics calculated on the CIS115 datasheet values are taken from (Teledyne e2v, 2016)

In this chapter, the system gain is calculated as 1.84 ± 0.03 e⁻/DN across the whole device. This allows other results to be expressed in terms of electrons as opposed to digital numbers. This is used when presenting the results of noise, image lag and dark current of the device. However, the results presented in Table 6-6 only show the mean response of the device. This chapter also carried out a more detailed characterisation of the noise, lag and dark current of the 13-08 CIS115.

The noise characterisation involved obtaining the noise on a pixel-by-pixel basis across the whole device. Here, it showed that the noise can be approximated by a Gaussian distribution with a tail of pixels with high noise. The mission requirements state that noise of the CIS115 is required to be less than 8 e- RMS, and here the device has 93.62±0.04 % of pixels below this value over the range of mission operational temperatures.

Dark current is also characterised in the device on a pixel-by-pixel basis over mission temperatures and above room temperature. At the mission temperatures, the dark current is represented by a Gaussian with a tail of defect pixels with high dark current. In addition to this, a dark current image identifies the UV raster scan pattern on the back surface which is used to suggest BOL dark current is dominated by back surface diffusion.

Mean image lag is characterised for the control device and presented for mission temperatures. The image lag of the CIS115 is shown to behave differently below and above a knee point of approximately 10 ke⁻. Below the knee point the change in image lag with respect to signal is negligible, and above this knee point the image lag seems to increase linearly with signal. Image lag above this knee point is determined to be dominated by spill back and shows a small temperature dependency where lower temperatures have a reduced spill back.

6.4 Conclusions

These initial electro-optical parameters studied attach expected values to BOL CIS115 devices. In addition, this characterisation has allowed for key conclusions to be drawn about the CIS115. Firstly, that the CIS115 meets performance requirements at BOL. Secondly, these studies show that pixel-by-pixel performance has been integral in understanding the behaviour of noise and dark current, and as such, this thesis will extend this into an unique study into the pixel-by-pixel performance of the image lag for the CIS115. Furthermore, behaviour of the device following exposure to radiation is still undefined, and therefore will be studied in the next chapters with respect to the dark current performance and image lag.

Moreover, a tail of poorly performing pixels has been noted in both the noise and the dark current of the CIS115, so this tail will be of interest following irradiation not just for dark current but also in the pixel-by-pixel image lag characterisation.

6.5 References

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McGrath, Dan, Steve Tobin, Vincent Goiffon, Pierre Magnan, and Alexandre Le Roch. 2018. 'Dark current limiting mechanisms in CMOS image sensors', *Electronic Imaging*, 2018: 354-1-54-8.

e2v, T. (2016). "CIS115 Back-Side Illuminated (BSI) CMOS Image Sensor." Retrieved November, 2019, from https://www.teledyne-e2v.com/content/uploads/2016/07/A1A-785580 1 v1.pdf.

Chapter 7: Dark Current Characterisation of the CIS115

7.1 Introduction

Dark current in 4T CIS is a fundamental noise source which affects the output signal of a scientific imager. Since dark current is a parasitic noise source that can be worsened when operational conditions in the device are changed, studying the dark current of the CIS115 is vital. Furthermore, as discussed in Chapter 3:, dark current can also be worsened following TID and TNID making investigation of the dark current of the CIS115 an important performance characteristic to ensure the best performance for the JANUS camera on JUICE.

As discussed in 2.6.1.3, Dark Current (DC) in CIS originates from three primary sources:

- dark current arising from the depletion layer (depletion dark current)
- dark current arising at the silicon surface (surface dark current)
- dark current arising in the bulk neutral region (diffusion dark current)

However, since the CIS115 employs a pinned photodiode structure the surface dark current is largely supressed and the dark current at Beginning-Of-Life (BOL) is expected to be largely dominated by both depletion and diffusion-based sources. In addition to this, 2.6.1.3 also states that the diffusion current will dominate at temperatures above room temperature whereas depletion dark current tends to dominate at temperatures below this.

Studies into the dark current in the CIS115 are expected to confirm that the activation energy of depletion dark current and diffusion dark current will be dominated by an activation energy at the mid band gap and the band gap of silicon (1.12 eV) respectively. This dark current activation energy in imagers is discussed in (Widenhorn et al. 2002) where dark current activation energy is calculated from a relationship between dark current and temperature. Dark current sources can also arise from 'defect' sites and are known as 'defectgenerated' dark signal. For the SRH mechanism shown in Equation (2-8) it is evident that defect sites with energy E_t result in maximum values of the generation rate, U, when their energy E_t is equal to E_i (minimising the value of cosh), with emission decreasing exponentially as the defect location approaches the band edges.

A dark current study on the CIS115 has already been carried out and published in the paper "Thermal annealing response following irradiation of a CMOS imager for the JUICE JANUS instrument" (Lofthouse-Smith et al. 2018), where data following a Total Non-Ionising Dose (TNID) were published before and after a thermal anneal of several CIS115 devices. This chapter involves characterisation of BOL CIS115s, investigating the dark current behaviour of the CIS115 and sources of dark current. After this the behaviour of CIS115 devices following TNID, Total Ionising Dose (TID) sources and a thermal anneal is studied for specific End Of Life (EOL) irradiation levels (with results from Lofthouse-Smith et al. 2018 included), investigating the sources of any DC changes in the detector. This chapter then concludes if these changes replicate the behaviour in current literature of other 4T CIS.

7.2 Non-irradiated device dark current

Since dark current is a thermally activated electron emission process in both diffusion and depletion, the dark current of the device can be expressed as a function of temperature and is shown in Equation (7-1) and Equation (7-2).

$$J_{dep} \propto T^{3/2} e^{-E_g/_{2kT}}$$
 Equation (7-1)

$$J_{diff} \propto T^3 e^{-E_g/kT}$$
 Equation (7-2)

For semiconductors where n_i (the intrinsic carrier concentration) is small, which is the case for silicon, the depletion current will dominate at room temperature and below (Sze and Ng 2006) whereas above this temperature the diffusion current will dominate. Therefore, in the CIS115, in studies carried out above room temperature as opposed to JANUS operation temperatures, the dark current of the device can be expected to be diffusion dominated, with a dark current activation energy equal to the full band gap of silicon (E_g) and therefore one would expect to see two slopes of the dark current when plotted on a log scale against 1/T.

Initial characterisation of an unirradiated control device is carried out in 6.2.2.3, where two temperature regimes of dark current are studied. This chapter focuses on several Devices Under Test (DUTs) that are subject to different sources of radiation: ionising (gammas) and non-ionising (protons, neutrons). These devices are shown in Table 7-1. For ease of reference, the second two numbers of each device serial number are used to define each device in this chapter, for example device 15901-10-12 is referred to as 10-12. In addition to this, in the

'10-12' formalism, the first two numbers reference the silicon wafer and the last numbers the chip number on the wafer.

Device serial	Radiation	Anneal	Mission
number			Equivalent
15901-10-12	Protons: 5x109 10MeV, p/cm ²	Yes	Half EOL
15901-17-03	Protons: 5x109 10MeV, p/cm ²	No	Half EOL
15901-10-13	Protons: 1x10 ¹⁰ 10MeV, p/cm ²	Yes	EOL
15901-10-19	Protons: 2x10 ¹⁰ 10MeV, p/cm ²	Yes	Twice EOL
15901-12-04	Neutrons: 5.25x10 ⁹ 1MeV	No	-
	n/cm ²		
15901-10-11	Gamma: 50 krad (Si)	No	Half EOL
15901-17-02	Gamma: 50 krad (Si)	Yes	Half EOL
15901-17-19	Gamma: 100 krad (Si)	Yes	EOL
15901-17-13	Gamma: 100 krad (Si)	No	EOL
15901-10-03	Gamma: 200 krad (Si)	No	Twice EOL

Table 7-1: The DUTs used for the dark current device characterisation alongside their irradiative dose and their comparative mission equivalent fluence/dose represented as a fraction of expected mission 'End Of Life' (EOL) fluence/dose.

Figure 7-1 presents the average pixel BOL DC for the DUTS studied in the remainder of this chapter. Testing at mission temperatures show there is minor correlation between the temperature and the DC, where increasing the temperature fractionally increases the dark current. This is predominantly since at these temperatures the dark current rate is typically less than 1 electron s⁻¹ meaning that dark current measurements become dominated by other systematics such as stray light in the experimental setup. This is shown in the figure, where at the lower temperatures, the error on the dark current is significantly larger than the dark current itself. Due to this reason, the dark current analysis on DUTs in this chapter will involve analysing data collected above room temperature (30 to 40 °C) as the dark current measured has greater statistical significance (see Figure 7-1).

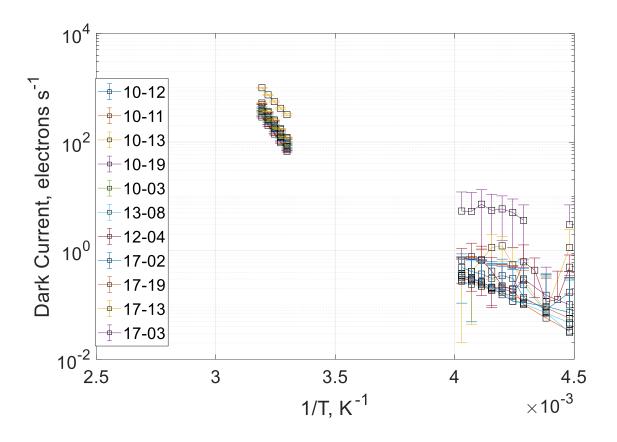


Figure 7-1: Mean Dark current for DUTs in the studied temperature regimes, where error is calculated as the standard error on the mean.

7.2.1 Dark Current Spectrum

The CIS115 is made up of over 3 million pixels, and as such simply expressing the dark current in terms of the mean is not the only method to express it for the DUTs. Taking the results on a pixel-by-pixel basis allows for a dark current histogram of each device to be created. These results will be displayed in the upcoming section.

Due to the nature of dark signal emission in 4T CIS, the dark current spectrum for each device can be thought to be represented by a simple Gaussian distribution, with a certain peak dark current value occurring in each device. For the DUTs the dark current histogram at 30 $^{\circ}$ C is shown in Figure 7-2.

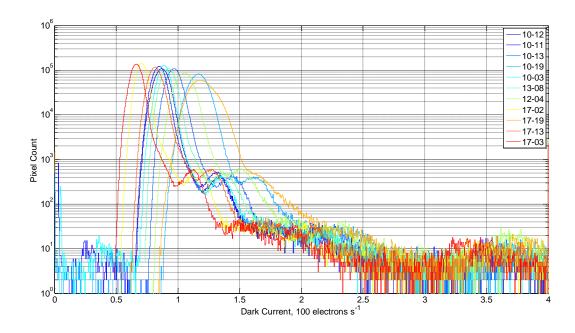


Figure 7-2: Dark current spectrum of BOL CIS115 DUTs at 30 °C, where the devices used have gone on to be tested in proton, gamma, and neutron irradiations. Dark current in these devices can be represented by a Gaussian distribution.

The differences observed across the DUTs can be attributed to many factors. One factor could be the slight difference in the temperature used during the dark signal acquisition. During the test, the temperature accuracy was ± 0.2 K. Although this is the case, much larger differences (the difference in DC between 17-19 and 17-03 is a factor of two) can possibly be attributed to a fabrication difference between the two devices. Dark current generation from areas such as at the STI, substrate, p $^+$ layer or contact diffusion can result in difference in dark current generation rates from device to device in addition to differences in the purity of the silicon wafer which can result in trap assisted dark current. Furthermore, 6.2.2.3 suggests that a dark current source in a BOL CIS115 can occur from back interface diffusion, meaning differences across devices can therefore arise from this variation of dopant implantation and annealing.

The main peak of the dark current distribution can be attributed to the dominant source of dark current in the device. However, Figure 7-2 shows that there are further peaks in the spectrum which are not part of the main population of pixels. These peaks are thought to arise from defect sites present in the device (Kwon et al. 2004) possessing their own, independent distribution function and generation rate (U).

7.2.2 Behaviour with temperature

The dark current of a device at BOL is thought to be dominated by a combination of both diffusion and depletion dominated sources. In the 'warm' regime, as discussed in 7.1, the assumption is that the dark current is diffusion dominated, therefore for testing carried out in this 'warm' regime dark current is assumed to be represented exclusively by Equation (7-2).

7.2.2.1 Activation Energy

From the works carried out in (Widenhorn et al. 2002) and the proportionality of the diffusion dark current from Equation (7-2) one can determine that the gradient of a plot of the natural logarithm of the dark current (J) over T^3 against the inverse temperature (1/T) in K^{-1} will be proportional to the activation energy (E_a) of the DC over the Boltzmann constant (Equation (7.3)). This equation can provide a more accurate measurement for the activation energy of the dark current than the works presented in (Lofthouse-Smith et al. 2018) due to the inclusion of the temperature term in the left hand side of Equation (7.3).

$$ln(\frac{J}{T^3}) \propto \frac{E_a}{kT}$$
 Equation (7.3)

Dark current is calculated at all temperatures on a pixel-by-pixel basis, and the relationship shown in Equation (7.3) is then used to calculate E_a for every pixel in the device. The dark current activation energy of each pixel in the device can be plotted in a histogram, and a Gaussian distribution can be fitted to these E_a values, shown in Figure 7-3. The activation energy of the device can therefore be determined as the peak value of this fitted distribution, with the error approximated as the standard deviation of the fit.

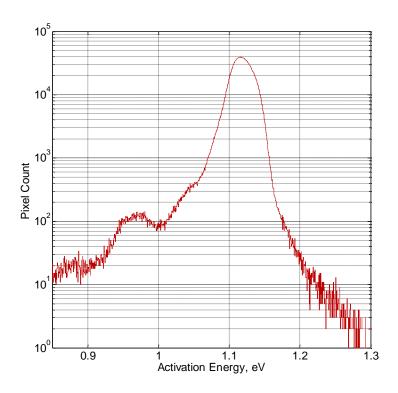


Figure 7-3: Activation Energy histogram of CIS115 15901-10-12. From a fitted Gaussian distribution to this data the mean and standard deviation of the activation energy of the CIS115 can be calculated. This is used to express the final E_a of the device, where this method is carried out on all DUTs.

For the remaining DUTs the same analysis method is carried out, where E_a values for all DUTs are presented in Table 7-2.

Device	Dark Current	
	Activation Energy in	
	the 30°C to the 40°C	
	regime (eV)	
10-12	1.12±0.03	
10-11	1.11±0.03	
10-13	1.11±0.03	
10-19	1.10±0.04	
10-03	1.11±0.03	
13-08	1.11±0.03	
12-04	1.10±0.03	
17-02	1.13±0.04	

17-19	1.12±0.03
17-13	1.13±0.03
17-03	1.12±0.03

Table 7-2: Activation Energy, eV, for the DUTs measure at BOL using the relationship shown in Equation (7.3).

Activation energy is taken as the mean value from the Gaussian fitted to the activation energy histogram, with the error the standard deviation of this fitted distribution.

At room temperature the band gap of silicon is approximately 1.12 eV (Sze and Ng 2006) so the activation energy values for the diffusion dark current are expected to be approximately this value. Table 7-2 presents these values, where each device is shown to agree with this figure for the activation energy. These results support the assumption that the dark current above room temperature is largely diffusion dominated.

7.3 Dark Current behaviour following TID.

Section 5.5 shows that 5 CIS115 devices were irradiated to varying levels of TID (between50 krad (Si) to 200 krad (Si)) with two of these devices undergoing a 168 hour 100 °C thermal anneal afterwards. The devices undergo irradiation testing to represent the ionising environment they are expected to be subject to during the JUICE mission and the thermal annealing is required to satisfy the space qualification requirements for a scientific image sensor. The gamma irradiated devices alongside their TID are shown in Table 7-1.

7.3.1 Mean Dark Current response following TID.

The mean response of the dark current across the whole device following TID is shown in Figure 7-4. The trend is that an increase in the TID incident on the detector increases the mean DC of the device. One of the devices studied (50 krad (Si): 10-11) appeared to have DC larger than a device irradiated up to 200 krad. Further investigation into 10-11 post radiation DC suggested that for this detector, during data acquisition, light leakage exists in all dark signal data. As a result, dark current of device was excluded when presenting results. As shown in the figure, at each TID, there is a linear relationship between the dark current and the temperature that is within the error bars shown for each device.

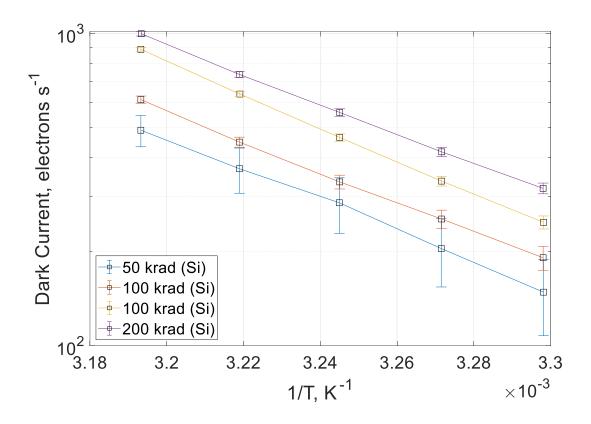


Figure 7-4: Mean dark current (electrons s^{-1}) of the gamma TID DUTs plotting against the inverse of the measurement temperature (K^{-1}) for the 'warm' temperature regime.

The DC increase following TID is thought to arise from the trapping of positive charge and the creation of interface states at the pre metal dielectric (PMD), STI, Transfer Gate (TG) and gate oxide (Wang et al. 2016) where McGrath et al. 2018 showed that these are dominant contributing sources in BOL CIS dark current. Dark current increase from TID at the gate oxide can arise from the de-passivation of dangling bonds. Hydrogen is added to the Si-SiO₂ interface during manufacture of devices to neutralise dangling bonds (due to imperfect interface bonding) that can act as DC generation sites. TID is shown to excite the deposited hydrogen permitting its diffusion out of the device, increasing the DC due to the addition of previously inactive traps.

7.3.2 Dark current spectrum

The DC spectrum for the gamma irradiated devices at 30 °C is shown in Figure 7-5. DC response following TID is typically thought to be characterised by a widening of the overall DC distribution present in the device as opposed to the creation of a large tail of pixels that is seen following a TNID irradiated CIS115 presented in (Lofthouse-Smith et al. 2018). The

widening of the pixel distribution is largely observed in Figure 7-5 alongside some clear and obvious peaks in the spectrum.

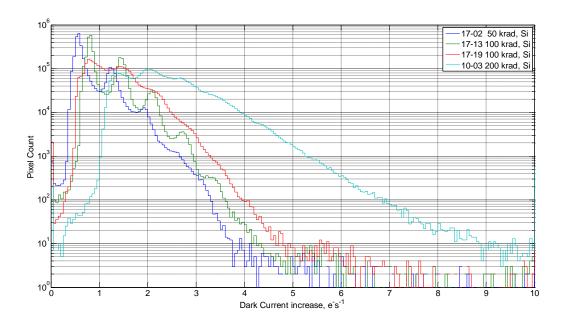


Figure 7-5: Dark Current increase spectrum of the gamma irradiated devices at 30 °C.

As mentioned in 7.2.2.1, the peaks in the DC spectrum of a CIS are thought to arise from defect sites present in the device. To investigate these peaks a discrimination technique that can be used is 'Dark Current Spectroscopy (DCS)'. This relies on these peaks arising from a defect site in the device with a given temperature dependence. Equation (7.3) can be used to determine the activation energy of these peaks which can assist in their identification. The DCS relies on the assumption that the capture cross section of both the electrons and the holes being identical for the traps, which means that the simplified formula for the generation rate (U), Equation (2-9) can be used. The devices irradiated to 50 krad and 100 krad have clear peaks in their DC spectrum (Figure 7-5) which are suitable for analysis using the DCS technique.

7.3.3 Temperature dependence of dark current

Using DCS to investigate the peaks occurring in Figure 7-5, further investigation into the nature of these peaks (and if there is a possible point defect source causing the peaks) are carried out at two TID levels: 50 krad and 100 krad. The first device characterised is a 50 krad device (17-02). The DC for 17-02 is presented in Figure 7-6, together with the differenced dark current, where the DC at BOL is subtracted on a pixel-by-pixel basis from the dark

current following TID. The dark current following TID is thought to be a combination of radiation induced dark current and DC sources that existed at BOL, with differenced DC expected to be representative of just the dark current because of TID.

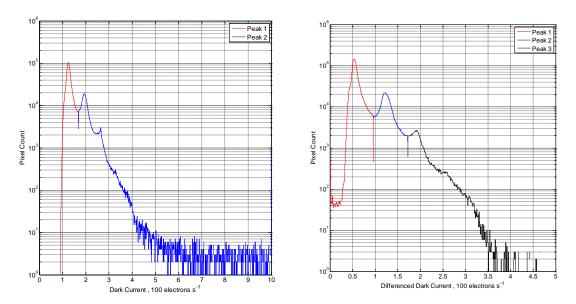


Figure 7-6: The Dark current at 30 °C for the irradiated device (left) and the differenced dark current data (right) for 17-02 (50 krad (Si)). The differenced data is calculated on a pixel-by-pixel basis where each pixel has its BOL dark current subtracted from its post radiation value. The number of peaks is determined by the thresholding used in analysis.

Using the data at 30 °C (303.15 K), pixel populations are determined from the peaks in this data set. The pixels that occupy these peaks at 30 °C (303.15 K) are then used to determine separate activation energies for these dark current populations. The activation energy is calculated from the relationship in Equation (7.3). The different peaks in the post radiation data are identified and the activation energy of these peaks are shown in Figure 7-7.

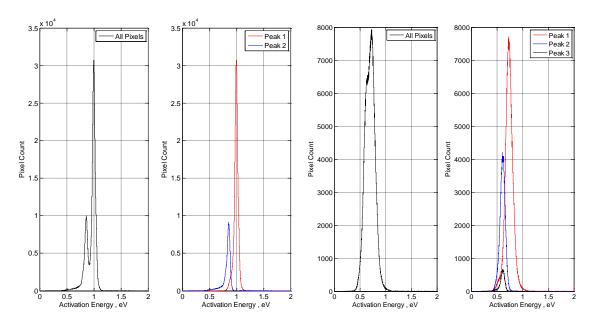


Figure 7-7: Activation Energy (17-02 50 krad (Si) in the warm regime for post radiation (left, centre left) and the differenced dark current data (right, centre right). Two peaks are seen in both data sets.

Investigation of the activation energy of these peaks involves the fitting of a Gaussian to each population to determine the mean activation energy and its standard deviation. The results are presented in Table 7-3.

Peak	Activation Energy of	$E_c - E_t (eV)$
	Peak (eV)	
Peak 1 Half EOL	1.00 ± 0.03	0.12
Peak 2 Half EOL	0.85 ± 0.03	0.27
Peak 1 Differenced	0.74 ± 0.07	0.38
Peak 2 Differenced	0.61 ± 0.05	0.51
Peak 3 Differenced	0.61 ± 0.04	0.51

Table 7-3: Dark current activation energy generated from a Gaussian fit to the peaks in Figure 7-7, and its standard deviation.

Firstly, in both the differenced and the non-differenced DC data, the lower activation energies occur at the highest dark current, with the smaller populations of pixels at higher DC having the lower activation energy levels in both data sets. Moreover, the differenced DC data taken at 30 °C shows the existence of three clear and obvious peaks (Figure 7-6, right) as opposed to the two that can be seen in Figure 7-6, left. Activation energy investigation here shows that the last two peaks have identical values for activation energy, suggesting that the trap species

responsible for this dark current site are identical and more than one trap per pixel are present.

Under the assumption that the differenced DC data better represent a trap species found in the device, one can use the difference of activation energy values from the conduction band to infer the activation energy of the trap species responsible. These are shown in the third column of Table 7-3, and can be used to identify the source of the trap. For the first peak the E_c - E_t value is 0.38 ± 0.07 eV. This first peak can potentially be attributed to the Divacancy (V_2) trap species with an energy level of approximately 0.39 - 0.43 eV (Hall et al. 2017), as the value E_c - E_t for this peak when including the error falls within this energy range. Although this is the case, the error on the measurement means this could also be attributed to the E-centre (a vacancy trapped next to a substitutional group-V atom) with an energy level below the conduction band of 0.45, 0.44 and 0.47 eV (Madelung, Rössler, and Schulz 2003). In addition to this, works by Hönniger 2008 have shown this to be a trap species induced in silicon from a 60 Co- γ ray irradiation. Moreover, because of the energy levels found for the E-centre, it means that the second and third differenced peaks can also be attributed to this defect, where the e-centre energy level of 0.47 eV below the conduction band is within the E_c - E_t error.

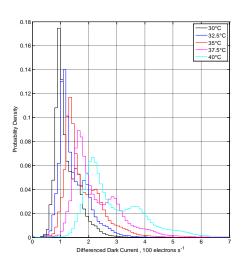
Using the same DCS discrimination technique for the 100 krad differenced DC data yielded three clear peaks in the DC spectrum which results in three corresponding activation energies. The value of the activation energy of these peaks along with their difference from the conduction band (E_c - E_i) is shown in Table 7-4. Due to the traps all having similar values for E_a it can be suggested that all DC peaks in the spectrum have arisen from a defect containing many of the same trap. Due to the errors involved in the measurement of this trap species however, it is difficult to determine what trap species this could be. Similarly, to the results shown for the 50 krad irradiated device: 17-02, both the E-centre and the divacancy (V_2) can be given as candidates for this defect since both energy levels of these trap species lie within the error on the E_c - E_t values given.

Peak	Activation energy of Peak	$E_c - E_t (eV)$
	(eV)	
1	0.63 ± 0.07	0.49
2	0.64 ± 0.05	0.48
3	0.66 ± 0.03	0.46

Table 7-4: Dark current activation energy from a Gaussian fit to the activation energy peaks in a 100 krad irradiated device, where the error on the activation energy is given as the standard deviation of these fits.

7.3.4 Thermal annealing response of TID irradiated devices

Two of the gamma irradiated devices (17-02 Half EOL 50 krad Si and 17-19 EOL 100 krad Si) underwent a 168-hour 100°C thermal anneal. The development of the biasing setup for this anneal was described in Section 5.6. One of these devices is presented in this section following thermal anneal and is shown in Figure 7-8. The figure presents results for the differenced dark current between BOL and post thermal anneal (left), and the differenced dark current between EOL and post thermal anneal (right). The differenced data between EOL and thermal anneal shows that a significant number of pixels centred around a difference of zero. This suggests that for many pixels in the device the dark current has remained unchanged following a thermal anneal. However, Figure 7-8 (right) also has a substantial number of pixel where the differenced dark current is below zero, suggesting a reduction in the dark current of these pixels.



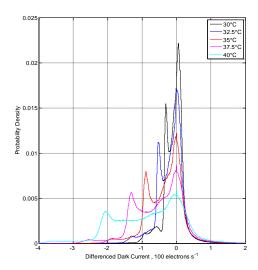


Figure 7-8: Differenced dark current between beginning of life and post thermal anneal (left) and between post end of life TID and thermal anneal (right). The plot on the right EOL indicates there is a proportion of pixels where the dark current has remained the same (centred around zero) and pixels where the dark current has improved following thermal anneal.

Due to the shape of the plot in Figure 7-8 (right) it can be suggested that the mean response over all the pixels of the device is an improvement in the dark current performance of the

device, which is seen in the mean dark current plot of the CIS115 in the warm temperature regime (Figure 7-9).

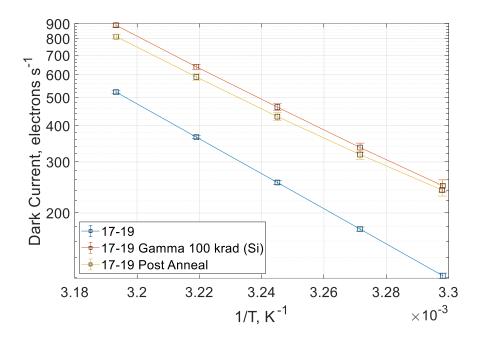


Figure 7-9: Mean Dark current of 17-19 device for BOL, EOL and post thermal anneal. A slight improvement in the mean dark current following a thermal anneal is seen.

7.4 TNID irradiated devices

As discussed in 4.5, one can expect a total non-ionising dose incident upon the JANUS camera during the lifetime of the JUICE mission. As shown in 3.3, TNID can degrade the performance of 4T CIS and worsen is abilities to function as a scientific imager. Therefore, it is of great importance for understanding the operation of the JANUS camera throughout its mission lifetime to replicate these conditions and carry out testing following exposure on important device characteristics. Here, dark current testing following TNID will provide information for the JUICE mission on the expected performance of the JANUS camera during the mission lifetime.

As mentioned in 5.3 and shown in Lofthouse-Smith et al. 2018 CIS115 devices were irradiated with 10 MeV equivalent proton fluences from $5x10^9 \, p/cm^2$ to $2x10^{10} \, p/cm^2$. In addition to this, one device (CIS115-12-04) was also irradiated with a TNID source of neutrons to a total fluence of $5.25x10^9 \, 1$ MeV equivalent n/cm^2 . Proton fluence shows an increased mean dark current which is shown in Figure 7-10.

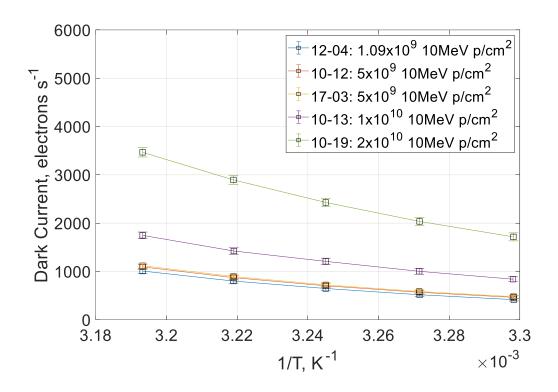


Figure 7-10: Dark current of devices irradiated with proton 10 MeV equivalent fluences.

Due to the displacement damage mechanism between protons or neutrons with silicon, it is thought that damage is localised to a fraction of the pixels. This means that DC increase will not occur through a global shift in the dark current across the whole device but be because of many bright pixels contributing to the increase in mean dark current of the detector. In addition to this, it also shows that the neutron fluence has the lowest mean DC following TNID at each temperature, which as seen in Figure 7-10 is the lowest 10 MeV equivalent proton fluence. At 30°C, the dark current of the CIS115 can be plotted with respect to the equivalent proton fluence received. This is shown in Figure 7-11.

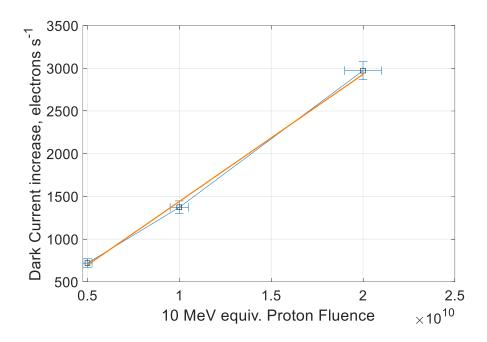


Figure 7-11: Dark current against proton fluence, showing a linear relationship between the dark current and the proton fluence.

The general trend of the plot shows a linear dependence between the total equivalent proton fluence and the mean DC of the device. It suggests that doubling the fluence doubles the mean DC. This can be explained if there is a linear relationship between the dark current increase and the damage on the detector relating to a dark current increase. One such formalism is found in Srour and Lo 2000 where it suggests that DC increase from TNID radiation can be expressed through Equation (7-4):

$$\Delta J = \frac{q n_i \Phi x_d}{2K_{qn}}$$
 Equation (7-4)

Where x_d is the width of the depletion region, q is the elemental charge, n_i is the intrinsic carrier density, Φ is the particle fluence and K_{gn} is the generation lifetime damage coefficient.

7.4.1 Proton and Neutron DC Spectra

As discussed previously, a better understanding of the DC in a TNID irradiated 4T CIS occurs when investigating the DC spectrum. This can be used to identify the nature of any hot pixel tail that has been induced in the device following TNID. The DC spectrum for the TNID DUTs

is shown in Figure 7-12 and shows the characteristic exponential tail for DC that is seen in other TNID irradiated CIS and Charged Coupled Devices (CCDs). The size of this 'tail' and hence the number of hot pixels has shown an increase with the TNID meaning that the increase in the mean response of the DC in a displacement damaged device at a given temperature is governed by the size of the hot pixel tail in dark current.

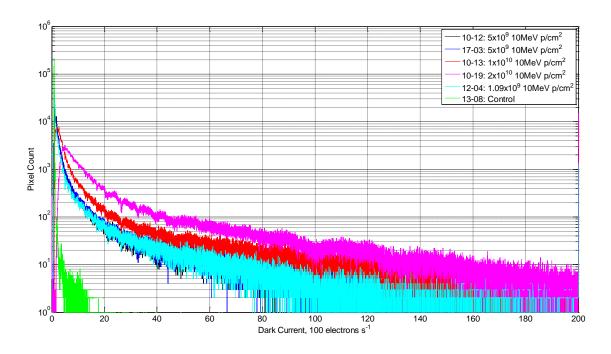


Figure 7-12: Dark Current spectrum of the CIS115 after non-ionising radiation at 30°C.

Although the exponential tail is generated from displacement damage, one cannot ignore the levels of ionising damage from the positively charged protons when investigating the dark current spectrum. The levels of TID are shown in Table 7-5. The TID at the twice EOL is only 10% of the TID level at the lowest gamma dose, so the same level of ionising damage will not be seen. Furthermore, the unbiased nature of the proton irradiation will lessen the effect of any TID effect.

Beamline Fluence (72.8	Lifetime Factor	TID
MeV p/cm ²)		(krad)
1.038x10 ¹⁰	Half EOL	1.272
1.039x10 ¹⁰	Half EOL	1.273
2.077x10 ¹⁰	EOL	2.545
4.152x10 ¹⁰	Twice EOL	5.088

Table 7-5: TID from the proton fluences used in the proton irradiation calculated from their 10 MeV equivalent fluence.

As a result of the TID associated with the proton irradiation, a small increase in the mean dark current can be expected, in addition to the creation of hot pixels from non-ionising damage.

7.4.1.1 Thermal Annealing response of dark current spectrum

Section 5.6 shows that three proton irradiated devices underwent a 168 hour 100 °C thermal anneal. The results for three devices (half EOL, EOL and twice EOL proton fluence) are shown in Figure 7-13. In Figure 7-13 the graphs from left to right represent the data collected at half EOL, EOL and twice EOL proton fluence, respectively.

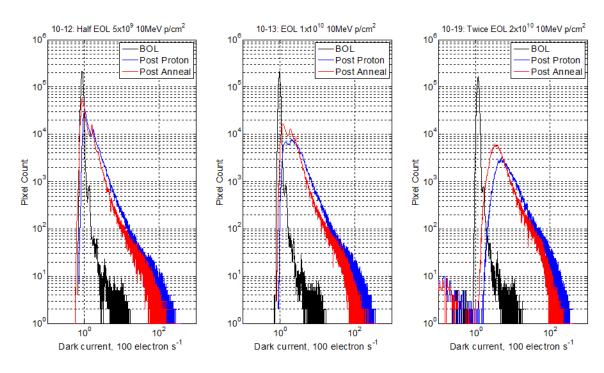


Figure 7-13: Dark current at 30 °C of each the three annealed devices where the left device is half EOL proton fluence, middle is EOL proton fluence and right is twice EOL proton fluence. Thermal anneal has shown to increase the population of pixels at lower dark current in the device, with the number of pixels occupying the hot-pixel tail also shown to decrease.

Thermal anneal indicates a partial recovery in the DC performance of each device as shown by the shift of the spectrum to lower DC values and the decrease of the hot pixel tail. At half EOL and EOL proton fluence the thermal anneal recovers some pixels to dark current values that occupy the main pixel population at BOL. The TNID induced damage at twice EOL however does not recover to the same extent. The partial recovery would suggest that some pixels had their DC increased following proton fluence by a degradation mechanism that has

been annealed at 100 °C. An investigation of the activation energy of these pixels will likely present more information into the dominant source of the DC.

7.4.2 Temperature dependence of dark current

Following proton irradiation, one can expect that the dominant radiation damage effects are caused by bulk defects created within the pixel (Virmontois et al. 2010) and as such are expected to have an activation energy in a form similar to Equation (7.3). Using this relationship, the DC activation energies can be obtained. This is carried out on a pixel-by-pixel basis and shown for each device in Figure 7-14. To obtain data with the best statistical significance, the activation energy is only plotted for pixels that have a goodness of fit parameter R² of greater than 0.95. Clearly as the proton fluence increases, the activation energy becomes less represented by a single Gaussian peak that is characteristic of the CIS115 BOL as shown in Figure 7-3, suggesting multiple traps contributing to the DC.

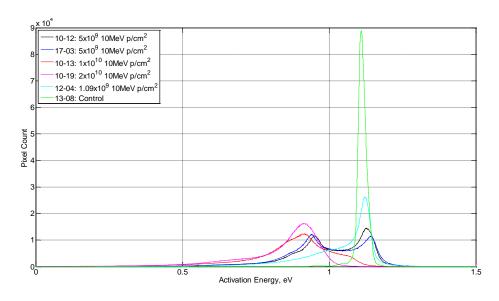


Figure 7-14: Dark current activation energy spectrum of each device.

As seen in Figure 7-14 increasing the fluence reduces the main pre-irradiation peak in the activation energy and increases the activation energy at peak of around 0.9 eV. Little information can be inferred about the nature of the dark current exclusively from the results presented in Figure 7-14, but one can suggest that the peak in E_a at 0.9 eV can be attributed to a dark current defect induced by TNID. The neutron device is largely characterised by a peak at the band gap of silicon, with increasing fluence decreasing the size of the population

at the band gap of silicon and introducing a new peak that exists at approximately 0.90 eV (as reported in Lofthouse-Smith et al. 2018)

7.4.2.1 Temperature dependence of dark current after thermal anneal.

As discussed in Lofthouse-Smith et al. 2018 the thermal annealing response to the dark current is studied through the investigation of activation energy. Due to the more accurate formula presented in Equation (7.3), the effect that annealing has on dark current when compared to the works in Lofthouse-Smith et al. 2018 is expected to be shown more precisely. The E_a results for the thermal anneal of the devices are shown in Figure 7-15, where from left to right the fluence increases from half EOL, to EOL finishing with twice EOL.

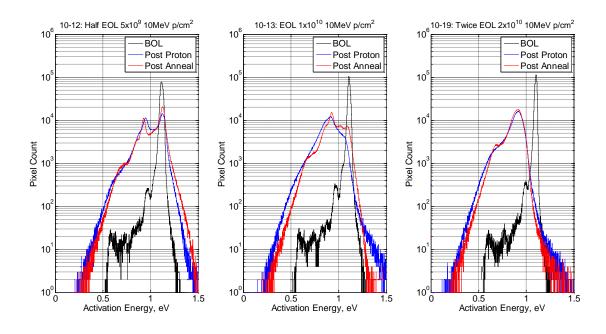


Figure 7-15: Dark current activation energy histograms produced for devices at BOL, following proton fluence and post anneal. The left figure is at half EOL fluence, middle is at EOL fluence and right is at twice EOL fluence.

The effect of the proton fluence on the E_a histogram is discussed in 7.4.2 and shown in Figure 7-14, where post proton results for the annealed devices is included in Figure 7-15. Following a thermal anneal, there is a slight change in the activation energy, meaning that when comparing it to the dark current results presented in Figure 7-13 it suggests that the thermal anneal changes the shape and appearance of the DC distribution at 30 °C but only a small number of defects induced by TNID responsible for these DC pixel values has annealed. Pre radiation the device is largely dominated by activation energy of the band gap of silicon, as

seen in Figure 7-3. However, it includes values below this likely due to defects in the device. Following TNID the size of the population at the band gap of silicon decreases with respect to fluence, and the population size at the defects are shown to increase with respect to fluence. Thermal anneal shows only small changes in the activation energy histogram, where changes have limited effect on the activation energy suggesting thermal anneal has not annealed a significant number of defects created by TNID.

7.5 Summary

In this chapter a range of difference results following the analysis of the dark current of the CIS115 were presented. Initially the dark current of the CIS115 was presented with respect to temperature, showing here two factors of the dark current of the CIS115. Firstly, that the dark current is shown to improve following temperature decrease, with the lowest temperature used in the study (-50°C) offering the best dark current performance. Secondly, this temperature dependence also revealed a characteristic about the dark current in the CIS115. Two temperature regimes were used in the dark current study, and at the warmer temperature regime (25°C to 40°C) the activation energy of the dark current showed a dependency on the band gap of silicon. This implied that the predominant source of the dark current in the CIS115 at this temperature regime is largely diffusion dominated.

The testing for dark current of the CIS115 also involved characterisation following several irradiative sources. These came following three irradiation campaigns which exposed the CIS115 to gamma rays (TID), protons (TNID) and neutrons (TNID).

Following TID the dark current of the CIS115 is shown to increase. The identity of this increase is studied in this chapter where it is suggested that defect sites which occupy a forbidden level in the band gap of silicon have been introduced increasing the trap assisted dark current. Using a DCS technique, possible candidates for these defect sites can be suggested from their energy position in the band gap. The candidates for these are suggested to be the E-centre or the divacancy. The effect of TID is also studied following a thermal anneal, where results presented suggest that some pixels where DC has shown to worsen following TID are returned to their BOL DC levels.

Following TNID the mean DC increase following proton irradiation shows a linear dependence between the TNID and the DC increase. The spectral response following TNID is largely dominated by an exponential tail of high DC pixels increasing in size with respect to

TNID, with the largest TNID showing the highest number of pixels in this tail. The low levels of ionisation even at the highest fluence (approximately 5 krad at twice EOL proton) show that ionisation damage can be neglected in these results and the dark current increase can be attributed to damage induced by displacement damage. Following thermal anneal, partial recovery of DC is seen at half EOL, EOL and twice EOL. This recovery of dark current is also seen when looking at the activation energy of the dark current too, where following thermal anneal partial recovery of some pixels to BOL activation energy values is seen. It is thought that this DC arises from bulk level defects or traps with activation energy close to the band gap of silicon.

The difference in the dark current spectra of TNID vs TID irradiated devices is such that the DC degradation following TID arises from a global increase in dark current across the pixels in the device, whereas an increase in the mean dark current of a TNID irradiated device occurs due to defects generating high levels of bright pixels.

7.6 Conclusions

Many dark current studies have been undertaken in 4T CIS to investigate their response following TNID and TID. In works carried out by Belloir et al. 2016 DCS was used on neutron, proton and ion irradiated devices. Largely the trend for the DC spectra showed the creation of a tail of high DC pixels which is like the results presented in this chapter following TNID. In addition to this, works by C. Virmontois show the displacement damage effects on DC and compare the DC distributions of neutron and proton irradiated detectors, again finding this exponential hot-pixel tail. However, they also describe the damage from protons in terms of ionisation, suggesting that the actual dark current distribution of proton devices include an ionising and coulombic scattering component (due to the charge on the particle) impacting and causing a DC increase in all pixels. Again, this is an effect that has been reported here in the CIS115, suggesting the CIS115 DC performance following proton and neutron fluence is like that observed in other DC studies on 4T CIS.

The works in Wang et al. 2016; Goiffon, Estribeau, et al. 2012; Goiffon, Virmontois, et al. 2012 all demonstrate that the dark current increases following TID. The works carried out by Goiffon however investigate the location of these DC sources in the pixel to assist in identification of the dominant source of DC degradation. Dominant locations of DC degradation cannot directly be obtained from the mean DC works on the CIS115 due to the

lack of variation of the structure during testing, however the results presented in Goiffon, Estribeau, et al. 2012; Goiffon, Virmontois, et al. 2012 can be used to suggest the location of DC degradation in the device to be predominantly in the silicon bulk for displacement damage. DC is also thought to degrade in the CIS115 due to the creation of defect sites (determined by DCS) that act as an intermediate energy level within the silicon bandgap resulting in trap assisted dark current.

7.7 Further Work

From the results presented in 7.3.3, an interesting aspect of future work here could involve further research to assist in the identification of the candidate for trap species in greater detail. Typically, these traps are stable at room temperature (and to the 40 °C used in testing) and are known to have annealing temperatures above 100 °C used in the thermal anneal. Further work on the TID irradiated devices could involve the annealing of these devices at elevated temperatures to ascertain if these traps are removed at higher annealing temperatures, and if successful provide further identification of the trap species responsible for these dark current peaks. One such species suggested as a possible candidate for all the dark current peaks in the TID irradiated devices is the E-centre, which is known to anneal at 150 °C (Moll, 1999).

From the activation energy plot shown in Figure 7-14 a new peak population has shown to appear at approximately 0.9 eV. Further investigation of the dark current of the pixels in this peak can be compared to known defects and traps that are created following TNID incident on other silicon imagers, may give further information on the reason behind this increase, e.g., if it is cause by defects, clusters, or interfaces. These works however are beyond this thesis in its current state.

7.8 References

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Chapter 8: Image Lag in CIS115

8.1 Introduction to image lag

Image Lag in image sensors employing a pinned photodiode is a phenomenon that occurs when there is an incomplete transfer of charge within the pixels. Image lag is typically presented as the ratio of the non-transferred signal to the initial signal charge. Typically, one can refer to two image lag mechanisms known as charging lag and discharging lag (Fossum 2003) from the dark-light and the light-dark image transitions respectively. These occurrences have been discussed in greater detail in 2.6.1.4 and are a source of noise in the image, which can deteriorate image quality. The image lag testing procedure described in 5.2.2.1 focuses on the bright-to-dark transition image lag and will form the focus of this chapter.

This chapter introduces the historical context of image lag in 4T CIS devices following radiation damage and methods of image lag reduction in 4T CIS. The way in which this lag manifests itself in the CIS115 will be investigated here, with further detail into the way this lag changes following ionising and non-ionising radiation. Investigation into methods for image lag reduction in the CIS115 is presented.

8.2 Image lag in CMOS APS

This section reviews the literature surrounding the current studies carried out on 4T CIS. This will look at the radiation effects of image lag on 4T CIS, and current studies that have shown methods to reduce image lag.

8.2.1 Radiation effects on image lag – current studies

Image lag in 4T CIS following Total Ionising Dose (TID) was studied in a paper written by Goiffon et al. 2012 in 2012. Here, image lag was studied for six 4T CIS fabricated in two different foundries on $0.18 \, \mu m$ process, with details of the two sensors shown in Table 8-1. Devices in this experiment were irradiated using $10 \, \text{keV}$ X-rays to a maximum total dose of $100 \, \text{krad}$ (SiO₂), and a minimum of $5 \, \text{krad}$ (SiO₂) using a dose rate of approximately $100 \, \text{rad}$ (SiO₂)/s. All irradiations were isolated to the image area, meaning readout electronics degradation is avoided and cannot be responsible for the change in device performance.

Features	Sensor A	Sensor B
Array Size	256×256	256×256
Pitch (μm)	7	4.5
PPD Area (μm²)	6.25	2.2
PPD Perimeter (μm)	10	7.7
CVF (μ V/ e ⁻¹)	57	38
V _{LOTG} (V)	-0.65	-0.5
MOVS (mV)	88.5	354
Full Well (ke ⁻¹)	15.5	9.1

Table 8-1: The CMOS Image Sensors Studied in (Goiffon et al. 2012)

Signal generation in this study was performed using a pulsed LED, meaning signal electrons can be entirely isolated to one frame in a readout.

Goiffon et al. 2012 presented results for image lag at a single signal level of 4000 electrons for each DUT at each of the TID levels studied. Before irradiation, the two devices studied show differences in image lag, where image lag in sensor A is approximately 10% of illumination, and sensor B approximately 0.1%. They attribute this difference to the way in which the devices were constructed in their respective foundries. In addition to this, the differences in the two could be attributed to the PPD area of the devices, as it has been shown in Park and Uh 2009, which observed that smaller buried photodiodes are easier to drain of charge and have a lower pinning voltage, which assists in charge transfer. Moreover, both pixel types A and B employ a simple rectangle photodiode shape, which has been shown to be sub optimal for charge transfer in 7 μ m pixel size sensors (Park and Uh 2009) but may not largely affect charge transfer in the smaller pixel size in Sensor B.

Following irradiation, the change in image lag is different for the two devices. Sensor A displays an improvement in image lag, dropping to less than 5% (from 10%), and sensor B increasing to a level of around 1% (from around 0.1%). The paper proposes two mechanisms for this change in image lag, and these can be seen in Figure 8-1. Figure 8-1 shows the electrostatic potential in a 4T pixel and shows a device exhibiting a potential barrier in the transfer pathway shown in panels 1 and 2 and a potential pocket shown in panel 3. The ideal transfer for 4T pixel, is seen in (4), with complete electron transfer.

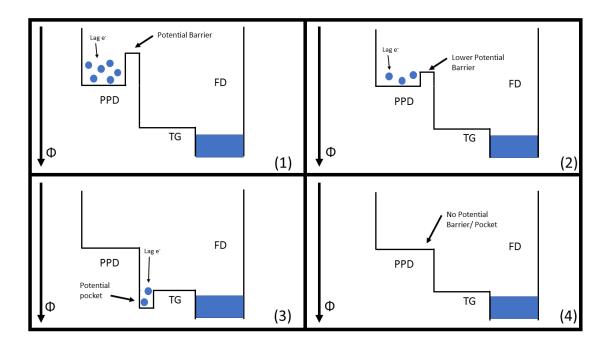


Figure 8-1: Image lag mechanisms in 4T CIS as suggested in and adapted from (Goiffon et al. 2012) shown via a simplified potential diagram at end of electron transfer (TG high).

Goiffon et al. 2012 suggest that in sensor A, pre irradiation, a potential barrier between the PPD and the Floating Diffusion (FD) pathway existed (panel 1) which hindered the transfer of electrons. Following TID, this barrier is reduced through the trapping of positive charge in the oxide in that region, allowing for the improved transfer of electrons, and thus decreased image lag (panel 2). Conversely, in sensor B, they theorise that due to the low levels of image lag seen before TID, there is no potential pockets or barriers creating the image lag in the device. Following TID, the creation of a potential pocket in the overlap region of the PPD and the Transfer Gate from the trapping of positive charges in the oxide increases the image lag. It should also be noted that in this study, no noticeable difference in lag can be seen in biased and unbiased devices.

Following on from the work produced in Goiffon et al. 2012, Goiffon produced another paper in 2014 (Goiffon et al. 2014) on the influence of transfer gate design and bias on the radiation hardness of pinned photodiode CMOS image sensors. This delved into the image lag performance of 4T CIS, where different TG and PPD designs were employed in pixels manufactured using a $0.18~\mu m$ CIS process.

Radiation effects were studied at room temperature using a Cobalt-60 (60 Co) gamma ray source at a dose rate of 600 rad (SiO_2)/h accumulating a maximum TID of 1000 krad (SiO_2) for seven pixel designs on (Goiffon et al. 2014)

- Reference (Ref)
- Long Transfer Gate (LongTG)
- Wide Transfer Gate (WideTG)
- Shallow Trench Isolation 0.7 (STI0.7)
- Enclosed Layout Transfer Gate Shallow Trench Isolation (ELTGSTI)
- Enclosed Layout Transfer Gate Active (ELTGActive)

Most of the pixel types in this study (except the enclosed layout devices) have a square PPD with approximate dimensions of $2.5\times2.5~\mu\text{m}^2$. The main differences arise from the TG shape or its immediate vicinity.

Characterisation of these devices were carried out at 22° C with transfer gate bias (Φ TG) voltage of 3.3 V and low transfer gate voltage (V_{LOTG}) of -0.6V. Lag measurements were performed on devices in accumulation regime, i.e., with a low TG bias. Image Lag tests used a pulsed LED, like the tests used in (Goiffon et al. 2012) to ensure light is temporally located in one frame for accurate measurements.

Pixels that were fabricated using a bottleneck in the pathway between the PPD and the TG in fabrication (Ref, LongTG, LongBN and STI0.7) show poor image lag pre-irradiation, which agrees well with the hypothesis that a potential barrier exists under the TG which limits charge transfer, as shown in Bonjour, Blanc, and Kayal 2012. Moreover, further experimental evidence supporting this hypothesis shows that the longest bottleneck (LongBN and STI0.7) and thus the largest potential barrier, have the greatest image lag. Other pixel structures showed very low levels of image lag before TID and it can be assumed that their image lag is not dominated by a potential barrier.

Following TID (up to a dose of 300 krad) the different features of the pixels studied can be seen in their image lag performance. Pixels that have the largest potential barrier have shown the greatest improvement in their image lag performance following TID. This can be associated with the lowering of the potential barrier following radiation. Pixels that exhibit low image lag before TID, and thus have no potential barrier limiting charge transfer have shown the greatest degradation in their image lag performance where this increase in image

lag can be attributed to the creation of potential pockets or oxide interface states able to trap charges during readout.

Goiffon et al. 2014 also used this work to identify pixel features that can be eliminated as candidates for lag sources in irradiated devices. Comparisons of image lag made between Ref pixel against Long TG pixel (who vary only in TG area and perimeter) show almost identical image lag response following TID, suggesting that TG area and perimeter largely do not alter image lag. In addition, pixel comparison between WideTG and the ELTG pixels, who vary in TG width and area, alongside PPD perimeter and area, show a similar image lag response following TID. These results are used to suggest that charge trapping at the STI interface or gate oxide interface do not contribute to image lag degradation, meaning a candidate for image lag increase can be suggested as potential pocket creation. It should be noted that in Goiffon et al. 2014 all pixel types observe image lag degradation when exposed to TID over 300 krad, which can be concluded as the creation of potential pockets in the transfer pathway.

From these works' conclusions about image lag performance following TID in 4T CIS devices can be obtained. The work in Goiffon et al. 2012 showed that image lag performance in the 4T devices used is highly dependent on the structure and design of the pixel (e.g. transfer gate or PPD measurements), with changes in image lag (up to 300 krad) dependent on the initial dominant lag mechanism.

8.2.2 Image Lag Reduction- current studies

Image lag arises from the incomplete charge transfer of electrons across the PPD-TG-FD structure in 4T CIS devices (2.6.1.4). Using an understanding of this structure, electron transfer improvement methods discussed in Xu and Theuwissen 2013 suggest electron charge transfer can be optimised through

- Technology Optimisation, where it is shown in Junting et al. 2010 that idealised doping concentrations of the pinned photodiode and transfer gate channel can reduce image lag
- Pixel Operation Optimisation, where with the optimisation of ΦTG voltage;
 ΦTG time and readout sequence, image lag can be improved. These changes however may have adverse effects on the noise of the device, with Wang, Rao, and Theuwissen 2006 suggesting that hot-carrier induced impact ionisation will increase noise in devices for longer ΦTG times.

Pixel Design Optimisation, the distance between the TG to n-layer photodiode
and between TG and the surface doping layer can affect the size and the
location of the potential barrier or pocket in the device, with image lag being
optimal when ideal values for these parameters are chosen. The design also
relates to the shape of the PPD, with Xu and Theuwissen 2013 showing varied
image lag for different PPD shapes and sizes, with optimal values for these
parameters existing too.

Technology optimisation in 4T CIS devices investigated in Junting et al. 2010 identified two strategies for reducing image lag using ISE-TCAD simulations:

- transfer gate channel threshold voltage doping adjustment; and
- PPD n-type doping dose.

Transfer gate channel boron atom varied implant doping was carried out in Junting et al. 2010 and TCAD simulations found that decreasing the boron implant dose within a specified range can reduce the potential barrier and thus improve the transfer of electrons out of the photodiode.

In PPD n-type region doping optimisation, Junting et al. 2010 showed that for different PD n-type implant doses, from 3.0×10^{12} cm⁻² to 7×10^{12} cm⁻², that higher doses result in a decrease in the potential barrier between the PD and the TG. Image lag improvement from this lowered potential barrier is inferred by the PPD potential following electron transfer. Here, the higher n-type dopant doses having the highest PPD potential after electron transfer indicates a lower number of electrons remaining and therefore a lower level of image lag. The n-type region doping however is shown to reduce depletion layer width and well capacity and as a result Junting et al. 2010 suggests that a PPD n-type doping increase for image lag improvement should be increased only within a specific range.

Pixel operation optimisation in 4T CIS can involve the selection of optimal transfer gate voltages and transfer times. A study into the fixed-pattern noise in 4T CIS induced by the transfer gate (Wang, Rao, and Theuwissen 2006), found that in order to reduce it, shorter transfer times and lower TG voltages were required. The study however concluded that at these lower transfer gate voltages and times, image lag increased. This observation is supported by the work carried out in Junting et al. 2010, where different TG bias (Φ TG = 3.0 V, 3.2 V and 3.3 V) were simulated, with the largest transfer gate voltage shown to reduce the

potential barrier, concluding that at the highest TG bias (3.3 V) the optimum image lag performance is reached.

Pixel design optimisation refers to the design of a pixel, and how changes to structure can improve image lag in the device. Yonemoto and Sumi 2000 realised that in their Hole Accumulation Diode (HAD), charge transfer efficiency was affected by the HAD structure and potential distribution. They identified a maximum width of the readout gate which prevents incomplete charge transfer caused by the short-channel effect, with the overlap of the corner of the readout gate being optimised and close to the point of maximum potential in the HAD. At the maximum potential in the HAD it produces no barriers or dips in the signal charge transfer path from the HAD to the FD and therefore improves charge transfer efficiency.

Pixel design optimisation can also relate to the design of the photodiode in 4T CIS devices. Work by Xu 2015 investigated the image lag of 4T CIS with different photodiode shape, attempting to optimise the photodiode shape for reduced image lag. At its edge, the photodiode in 4T CIS has a reversed pn junction which is formed by the n-doping of the photodiode and the surrounding p-well. This creates an electric field that controls the behaviour of charge transfer from the PPD to the TG, and as a result, relates to the image lag performance. Xu, 2015 found that above a certain PPD length the image lag drastically increases. Shorter PPD lengths however reduce the FWC and light sensitivity of the photodiode meaning that optimisation of these longer PPD lengths was required. Xu, 2015 proposed a new "W" shaped photodiode with lower lag than its traditional long PPD length rectangular counterparts. The improvements in the "W" shaped photodiode is shown to arise due to the increased electrical field in the centre of the PDD in the "W" shape, improving the charge transfer out of the PPD. Xu, 2015 shows this arises from total integrated photocarriers in a PPD not exclusively relying on the PPD area, but on the PPD perimeter, area surrounding the PPD and the junction depth. Therefore a "W" shaped PPD compared to a rectangular PPD will have similar FWC to device even though its area is 19% less.

Since the CIS115 is already fabricated, the only image lag reduction methods that can be implemented are through pixel operation optimisation. Changes in the bias potentials, readout sequences and gate turn-on times are the only methods for image lag reduction in a device that has already been manufactured. Early model iterations of the pixel design used in CIS115 (CIS107) were thoroughly tested and subsequently formed the basis of the final CIS115 design. Revision B CIS115 devices are used in image lag testing in this chapter.

In a private communication with Teledyne e2v the CIS115 is shown to be fabricated with a W shaped photodiode. The pixel for CIS115 was selected after a characterisation from a host of test structures, where a structure employing a W shaped PPD was shown to have the best image lag. These test structures also investigated the dopant levels within the PPD, where an ideal dopant concentration and profile (through different implant dose and energy) was also discovered and was ultimately used in CIS115.

8.3 Discharging Lag in non-irradiated CIS115

To supplement current research into understanding how different sources of radiation affect image lag, lag at beginning of life (BOL) must be characterised. The testing procedure for image lag is described in 5.2.2.1 and the results are presented here.

Initial characterisation of the CIS115 for image lag is carried out in 6.2.2.4 where the relationship between temperature and image lag is discussed. In this chapter it is suggested that at BOL two lag regimes exist. These regimes exist below and above a certain knee-point in the image lag of the device, suggesting that, different phenomena are responsible. Above this knee point the dominant mechanism is thought to be through a charge spill back effect, and below this knee point thought to be dominated by poor drift out of the PPD.

8.3.1 Measured behaviour

The general trends of image lag performance as a function of signal level across all the DUTs are shown in Figure 8-2, demonstrating the overall similarities in image lag between devices. However, there is a slight variance between the absolute lag performance for the DUTs. One artefact in the image lag of the CIS115 that is similar across all wafers is the existence of a knee-point in the image lag performance. This knee-point occurs between approximately 5000 e- to 10000 e- and is thought to exist due to the changing of the dominant cause of image lag in the CIS115 from one source to another.

From Figure 8-2 a correlation between the image lag performance and the fabrication wafer can be seen; devices coming from wafer 17 have the best image lag and the devices constructed from wafer 10 have the worst. In addition to this, smaller variance is seen across devices from the same wafer, with a smaller chip number (seen in the wafer 10 devices) offering better image lag. These differences likely arise from small variations in intrinsic impurities present in the starting silicon that can trap electrons for reemission and the small

variation in fabricated PPD-TG-FD structure that can create potential barriers or pockets affecting the transfer of charge out of the PPD.

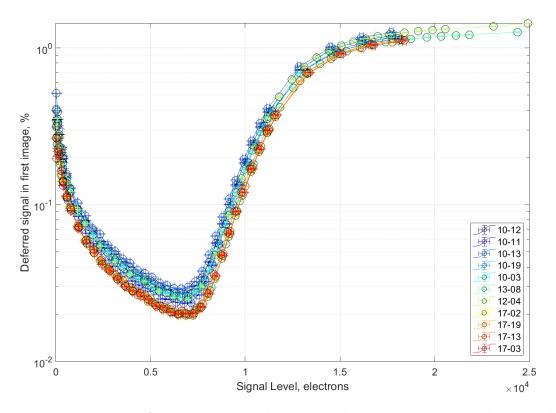


Figure 8-2: Mean Image Lag of DUTs at -50 °C. Across the DUTs image lag shows light variation which relates to the wafer of silicon used in fabrication with wafer 17 having lower lag than wafer 10.

8.4 Discharging lag in irradiated devices

Following characterisation of the behaviour of CIS115 image lag for unirradiated devices, investigation into the mechanisms for image lag response following TID and TNID is discussed in this section. Devices are irradiated with protons, neutrons, and gamma rays (Table 8-2) [See Chapter 5:] and data is obtained using the same methods as described in Section 5.2.

Device	Dose level	Comments			
15901-10-12	5×10 ⁹ 10 MeV equivalent	Half EOL proton irradiated, thermal			
	protons cm ⁻²	anneal			
15901-17-03	5×10 ⁹ 10 MeV equivalent	Half EOL proton irradiated			
	protons cm ⁻²				

15901-10-13	1×10 ¹⁰ 10 MeV equivalent	EOL proton irradiated, thermal anneal		
	protons cm ⁻²			
15901-10-19	2×10 ¹⁰ 10 MeV protons cm ⁻²	Twice EOL proton irradiated, thermal		
		anneal		
15901-12-04	1.09×109 10 MeV equivalent	Neutron irradiated device, 5.25 x10 ⁹ 1		
	protons cm ⁻²	MeV neutrons cm ⁻²		
15901-10-11	50 krad (Si)	Half EOL gamma irradiated		
15901-17-02	50 krad (Si)	Half EOL gamma irradiated, thermal		
		anneal		
15901-17-19	100 krad (Si)	EOL gamma irradiated		
15901-17-13	100 krad (Si)	EOL gamma irradiated		
15901-10-03	200 krad (Si)	Twice EOL gamma irradiated		

Table 8-2: Devices used in image lag study along with their respective accumulated radiation and nominal lifetime factor.

8.4.1 Discharging Lag in Irradiated device

Figure 8-3 shows the image lag behaviour following TNID of 10 MeV protons equivalent at two fluences of $1x10^{10}$ and $2x10^{10}$ protons cm⁻². The general behaviour seen below the kneepoint is an increase of the lag following TNID. This appears to scale with the fluence suggesting that TNID has created a type of trap species present in the transfer pathway (able to trap one or many electrons) preventing electron transfer to the FD. The behaviour above the knee point appears identical, suggesting that TNID has not significantly affected the spill-back mechanism thought to dominate image lag behaviour.

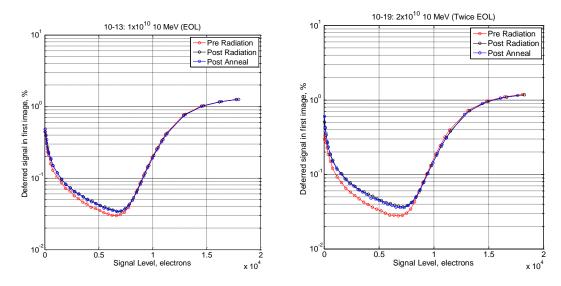


Figure 8-3: Image Lag at -50 °C in proton EOL and proton Twice EOL irradiated device. Error bars have been calculated on the standard error of the mean but are too small to be visible.

Image lag performance over all TNID devices is shown in Figure 8-4, however due to the difference in BOL shown in Figure 8-2, it is merely shown for information, as quantitative comparison is difficult due to the devices starting with different BOL lag.

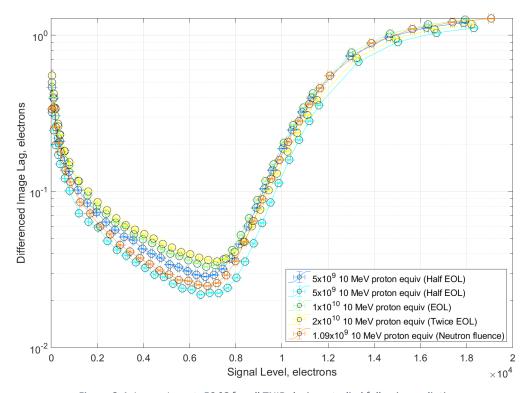


Figure 8-4: Image Lag at -50 °C for all TNID devices studied following radiation.

Figure 8-5 displays the image lag for two devices that have been subjected to a TID from γ -rays of 100 krad (Si) and 200 krad (Si) respectively. The general behaviour of the device following TID is a shift in the knee point to a higher signal level and an increase in the image lag below the knee point. The shift in the knee point can potentially be attributed to an accumulation of charge in an insulating layer in the device. Charge trapping in a 4T CIS is also seen in Goiffon et al. 2012 where charge trapping occurs in the PPD-TG region which would increase the potential under the TG and would reduce the knee point, similar to what is seen in 8.5.3. The increase in the image lag at below the knee point of the device has likely occurred from the creation of potential pockets or traps in the transfer pathway, hindering the transfer of electrons out of the PPD, seen in other work in 4T CIS involving TID (Goiffon et al. 2012) and discussed in 8.2.1. This increase in lag at below the knee point is seen following TID, and the size of this increase is related to the TID. The general behaviour of all the TID devices is shown in Figure 8-6, with knee point higher in devices with greater TID, and pre-knee-point lag increase scaling with TID.

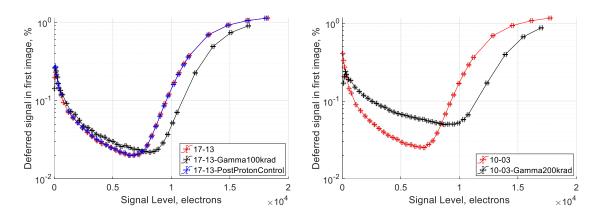


Figure 8-5:Image Lag at -50 °C in gamma EOL and gamma Twice EOL irradiated device

Image lag performance is shown in Figure 8-6 over all CIS115 devices irradiated with TID, however due to their differing BOL performance it is shown for reference only.

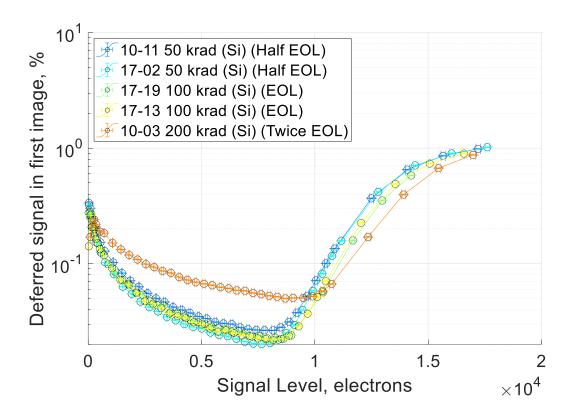


Figure 8-6: Image Lag at -50 °C of all TID devices studied following radiation.

8.4.2 Discharging Lag with varied temperature

Figure 8-7 shows the temperature dependence of the image lag in proton EOL, post thermal anneal device. It shows two clear regions and behaviours of image lag existing above and below the knee-point.

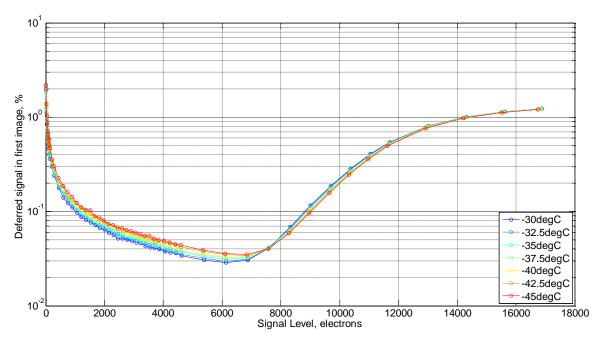


Figure 8-7: Image Lag at for varied temperatures of proton EOL device 10-13 following radiation and thermal anneal at -varied temperatures. Error bars are calculated from the standard error on the mean but are too small to be visible.

Due to the degradation of the image lag in proton-irradiated devices (see Figure 8-3) largely occurring at below the knee point one can infer that this increase is due to traps that exist in the transfer pathway that can trap signal electrons for re-emittance in subsequent frames. Trap species and clusters in silicon imagers are studied widely, such as in Hall et al. 2014 and show an increased emission time constant for trapped electrons at lower temperatures. This suggests any traps or clusters present following TNID are likely to be less active at lower temperature. However, Figure 8-7 shows that the trend of the image lag performance below this knee-point is identical to Figure 6-10, with lower temperature having worsened image lag. Therefore, the image lag resulting from traps can also be related to how long the emission time constant is with respect to the transfer time and the frame time. At emission times that are much shorter than the transfer time, any electrons that are trapped will be released in that readout and not cause any lag. For emission times longer than transfer time they are unlikely to reemit during readout and will affect the image lag. For emission times that are significantly larger than the integration time, the trap is likely to stay filled for many frames, so once filled in the first exposure is unlikely to release and cause image lag in later frames.

8.5 Study of the image lag knee-point

8.5.1 BOL and TID behaviour

The results presented in Figure 8-6 show the relationship of image lag before and after TID. The results show that TID induces a shift in the knee point of the image lag. This figure suggests that the shift in signal level at which the knee-point occurs is approximately proportional to increasing TID. TID in NMOS transistors, such as the in-pixel transistors in the CIS115, induces a net positive charge build-up increasing the effective potential under TG and/or FD.

8.5.2 Proposed spill-back mechanism

The spill back mechanism for 4T CIS is discussed in further detail in Section 2.6.1.4, however it should be noted that spill-back is expected to manifest itself at signals above the characteristic knee-point of the CIS115. As the signal charge accumulated approaches the difference between the pinning potential and the potential under the floating diffusion the charge is more likely to spill back from the FD to the PPD during charge transfer when Φ TG is held high. Spill back occurs at signal levels appearing between 5,000 electrons and 10,000 electrons signal (see Figure 8-2). This spill-back is expected to be related to Φ TG (High/Low), the pinning potential of the PPD and the reset voltage of the FD.

8.5.3 Low Φ TG measurements

The observations seen in image lag following TID suggest that the TID effect on the knee point is related to a flat band voltage shift within the device. Since the image lag knee point is thought to be related to the potential profile under the FD-TG-PPD, testing the effect of varying Φ TG on the image lag performance of the CIS115 will identify if this voltage will affect the image lag knee point in the same fashion as TID accumulation.

8.5.3.1 Experimental procedure

To investigate the contribution of ΦTG on image lag, testing at a range of transfer gate voltages was carried out. Testing a varied ΦTG is carried out on three CIS115 devices that vary in their exposure to radiation.

- CIS115 13-08 (Control, non-irradiated device)
- CIS115 10-13 (Proton EOL device, annealed)

CIS115 10-03 (Gamma 200 krad, 2EOL device)

These devices attempt to replicate the conditions expected in the Jovian environment by studying a device at BOL, following EOL protons, and following twice EOL gamma. The irradiated devices are also annealed to facilitate their space qualification. The Φ TG used for device 10-13 is carried out at voltages between 2.02 V and 3.50 V at varying increments. The testing continued for devices 10-03 and 13-08, operating these devices over a reduced range, starting at 2.02 V and 2.65 V respectively, varied from its standard 3.3 V.

8.5.3.2 Discharging Lag with varied ΦTG

The lag measurements with a range of high Φ TG applied for a non-irradiated device (13-08) are shown in Figure 8-8. The general trend of this graph highlights a reduction of image lag as the Φ TG is decreasing, alongside a shift of the knee-point.

This can be explained if the charge transfer process is treated with respect to the idealised PPD-FD-TG structure (see Figure 8-1, panel4). Lower Φ TG voltages alter the potential difference between the FD and the TG region, where one can expect an increased difference between the Φ TG bias and the reset level of the FD to hinder the rate at which the charge is spilled back onto the PPD. However, as this Φ TG voltage approaches the value of the pinning potential of the PPD (V_{pin}) one can expect to hinder the charge transfer out of the PPD as the potential difference between Φ TG ON and V_{pin} is too small to make charge transfer favourable.

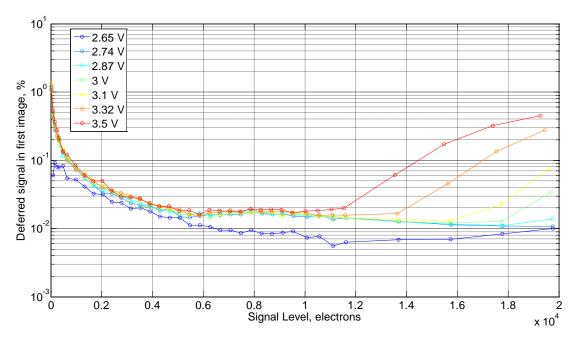


Figure 8-8: Image Lag at different Φ TG ON voltage for CIS115-13-08 at -50 °C. Error bars were calculated from the standard error on the mean but are too small to be visible.

8.5.3.3 Discharging Lag with TNID and TID

Similar plots to the ones presented in Figure 8-8 can be produced for the data collected using low Φ TG (see 8.5.3.1). From these plots, image lag at specific signal levels can be extracted through interpolation. This interpolation is carried out on three devices at a signal level of 15,000 electrons signal and is shown in Figure 8-9. The benefit of investigating the image lag at 15,0000 electrons signal is that one can expect the image lag signal to be dominated by spill-back since this signal level is significantly above the image lag knee point, both at BOL and twice EOL TID.

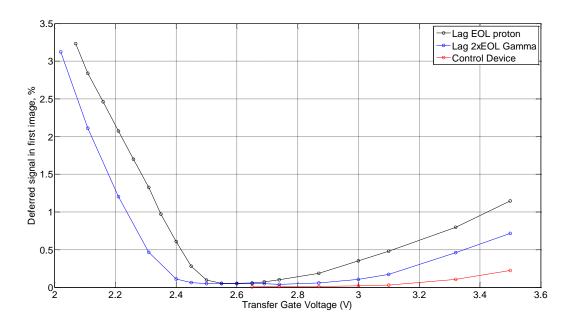


Figure 8-9: Image Lag at different Transfer gate voltages for control device and proton and gamma irradiated device for 15,000 electron signal at -50 °C. Error bars were calculated from the standard error on the mean but too small to be visible.

Figure 8-9 shows that there is an optimal region of Φ TG with respect to image lag. It appears this region exists from approximately 2.5 V to 2.9 V, with the range being extended to approximately 2.4 V in 10-03, the twice EOL gamma-irradiated device.

Figure 8-9 shows that decreasing the Φ TG ON voltage beyond a given point will increase the image lag. When the voltage is too low, the potential on the TG is too close to the potential on the PPD (V_{pin}) so the electron transfer out of the PPD will be less favourable. Previous works (Xu 2015) show that decreasing the Φ TG voltage increases image lag at 10,000 electron signal in a 4T CIS device. This is not what is seen in CIS115 where Figure 8-9 suggests that to a certain extent reduction of image lag occurs through lowering Φ TG.

8.5.4 Discharging Lag with a varied VREFR

Currently the hypothesis is that image lag is related to the potential under the PPD-TG-FD. Therefore, one can infer that any adjustments of external biases known to alter this potential profile can be expected to alter the image lag performance in the CIS115. In the CIS115 the potential that the FD is reset to is governed by the reference drain voltage (VREFR). As a result of this, changing VREFR alters the potential of the FD, which in turn will affect the PPD-TG-FD potential profile. Changes in this profile have shown to change the image lag of the

device (as seen previously at different Φ TG) and as such warrant further study. Lag measurements were carried out for VREFR voltages from 2.90 V to 3.40 V in approximately 0.1 V increments. This testing involved characterisation at two transfer gate voltages: 3.30 V and 2.65 V. These results are presented in Figure 8-10.

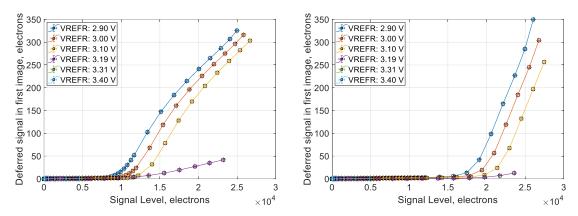


Figure 8-10: Image Lag at different VREFR for 13-08 control device at -50 °C for ΦTG 3.30V (left) and 2.65V (right)

Increasing the reference gate voltage increases the potential difference between the TG and the FD and in turn increases the point at which spill-back dominates. At both the transfer gate voltages used, an increased VREFR is shown to increase the image lag knee point. As can be seen in Figure 8-10, above 3.10 V VREFR, the device appears to be working improperly as for the same integration time as at other voltages, the device does not reach the same signal level. This could be since at these high levels of VREFR, the device is unable to operate as the voltage difference between the gate and drain is insufficient to allow current flow. As such, data above 3.10 V VREFR will not be used in further studies on the VREFR shift. To confirm that these changes are due to a real effect in the image lag of the device, and not due to a shift in the conversion gain in the device due to altering the reset voltage of the FD, the conversion gain at each of these VREFR voltages must be investigated.

The mean variance curves are shown in Figure 8-11, where the pixel-by-pixel values for gain can be calculated for each VREFR voltage. This gives the gain values shown in Table 8-3, where the error on these is the standard deviation from the linear fit to the data. At 2.9 V, 3.0 V and 3.1 V the gain values are shown to be approximately the gain that is quoted for the CIS115. At 3.1 V and below, the shift in the knee point of the image lag with a changing VREFR (seen at both Φ TG) can be attributed to a real performance of the device instead of due to a significant shift in the CVF at these operational voltages. The gain values calculated for a Φ TG

of 3.3 V are different since there is a dip in the PTC of the CIS115 (thought to be attributed to the device entering the spill-back regime) as seen in Figure 8-11.

VREFR Voltage	Gain (e ⁻ /DN)		
(V)	ФТG: 3.3 V	ФТG: 2.65 V	
2.9	2.2±0.1	1.9±0.1	
3.0	2.2±0.1	1.8±0.1	
3.1	2.2±0.1	1.7±0.1	

Table 8-3: Gain Values, with standard error on the mean calculated from mean-variance curves for different VREFR voltage and two different Φ TG voltages. At voltages above 3.1V the conversion gain is either impossible to be calculated, or the error is larger than the value of conversion gain itself.

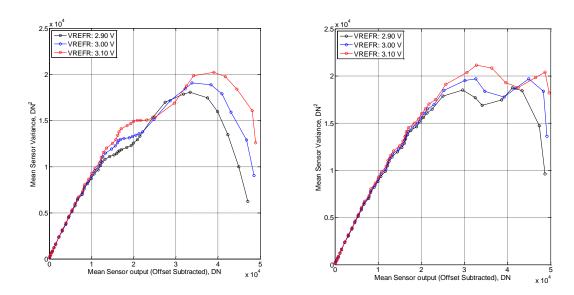


Figure 8-11: Photon Transfer Curve for 13-08 control device at -50°C at VRESET: 3.80V where Φ TG voltage on the left figure is 3.3 V and Φ TG voltage on the right figure is 2.65 V.

8.5.5 Concluding cause of lag knee-point

An idealised potential profile for the CIS115 PPD-TG-FD structure is shown in Figure 8-12. This is useful in explaining how the knee point of the image lag in the CIS115 changes.

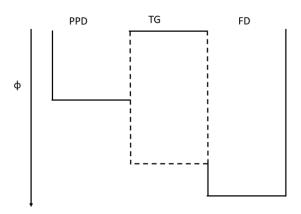


Figure 8-12: Potential profile under the PPD-TG-FD region. The dotted lines under the TG region show the potential the TG changes to when Φ TG is applied.

For half the dynamic range of the CIS115, image lag is dominated by this spill back mechanism occurring above the knee point of the device. Using the potential profile shown in Figure 8-12, the knee point is thought to manifest itself when the signal charge accumulated on the FD is high enough that it can spill back onto the PPD across the TG. This begins to dominate the image lag when the charge accumulation approaches the difference between the potential under the FD and the TG.

The image lag knee point is shown to shift following TID, but not following TNID. This shift is thought to occur through certain voltage shifts in the PPD-TG-FD structure. Since this shift shows improvement in image lag, there is potential that this effect can be harnessed to optimise the performance of the CIS115.

The image lag knee point is shown to shift with a change in VREFR voltage (the voltage that the FD is reset to), the Φ TG and with an increase in TID. The knee point shift following TID can be characterised through a build-up of positive charges in an oxide layer. This knee-point shift is characterised in Lofthouse-Smith et al. 2018 and is calculated as 0.84 mV krad-1. Due to the proton testing being carried out on unbiased devices with a maximum TID of approximately 5 krad at twice EOL, the effect of TID from the proton fluence is not expected to affect charge build-up in the PPD-TG-FD structure.

The knee point of the image lag can be determined as a function of Φ TG and is shown in Figure 8-13, left, where the relationship between the change in the knee point due to the change in Φ TG is calculated to be approximately -13 e⁻ m V⁻¹.

The change in the knee point caused by a change in VREFR is shown in Figure 8-13, right. The change in knee point caused by a change in VREFR voltage is calculated to be approximately 15 e⁻ m V⁻¹. Due to the similarity in the magnitude of knee point shift with respect to both Φ TG and VREFR their effect on the potential profile of the CIS115 may be similar.

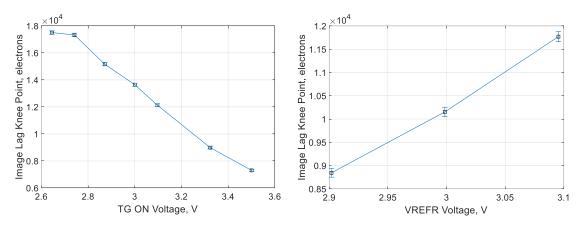


Figure 8-13: Image Lag knee point of the CIS115 control 13-08 device calculated for the mean image lag data when varying Φ TG voltage (left) and varying VREFR (right).

From the results presented in Figure 8-8 and Figure 8-10 the trend in the image lag knee-point with respect to bias voltages Φ TG and VREFR is observed. Decreasing the voltage of the transfer gate to 2.65 V (see Figure 8-9) is shown to increase the signal level at which the knee-point of the image lag occurs. It has been proposed that this increases the amount of charge that can be converted by the FD before the potential well in the FD reaches the potential to spill-back into the PPD. A behaviour which matches this hypothesis has been seen when the VREFR voltage is increased, by effectively increasing the reset potential on the FD, meaning that the voltage difference between Φ TG and the FD makes charge transfer more favourable. This therefore has the same effect as reducing the Φ TG voltage, increasing the signal level at which spill-back begins to dominate the image lag mechanism on the CIS115.

8.5.5.1 Optimisation for mission

For the mission requirements of the JANUS camera on JUICE, image lag is required to be minimised. As such, minimal image lag is seen when operating the device at a transfer gate voltage of approximately 2.6 V to 2.8 V (Figure 8-9). Within the region of minimum, selection of a Φ TG voltage of 2.65 V offers the best performance in the control device, alongside being in the region of minima for irradiated devices. Therefore, recommendation of Φ TG for

minimum image lag for the CIS115 is suggested to be 2.65 V. As discussed in 8.2.2 changing the Φ TG voltage has been shown in previous works to increase the readout noise of 4T CIS (Wang, Rao, and Theuwissen 2006). Therefore, it is important to measure the readout noise at the suggested image lag 'optimum' TG voltage. The measured noise performance of CIS115 is shown in Figure 8-14, where the noise is shown to be almost identical for both values of Φ TG, with the lower Φ TG providing a slight improvement.

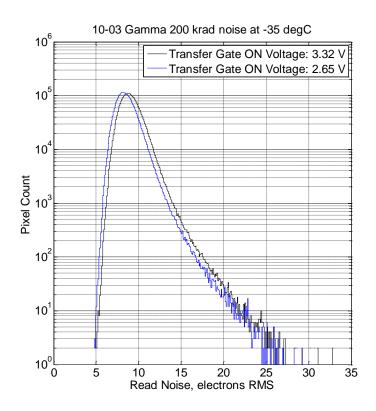


Figure 8-14: Read Noise for 200 krad gamma irradiated device at -35 °C.

From the unchanged read noise seen at these new voltages and improved image lag performance at varied VREFR voltages for the device (Figure 8-10) recommendations can be made for the operation of the CIS115. A VREFR voltage of 3.1 V has shown to reduce image lag performance of the CIS115 when operated with a Φ TG of 3.3 V and extension of this VREFR optimisation to a Φ TG of 2.65 V shows a continued improvement of image lag (Figure 8-10, left). Due to the large number of devices tested at this low Φ TG (proton EOL, gamma twice EOL) optimal mission operational voltage can be recommended to be a Φ TG of 2.65 V. However, the low number of devices tested at different VREFR means that until further tests are undertaken on a wide range of devices, VREFR changes are not recommended.

8.5.5.2 Image Lag knee point shift from Flat Band Voltage Shift (FBVS)

From the results presented in Figure 8-5 a shift in the image lag knee-point is seen following an accumulation of TID. In silicon 4T imagers, TID is shown to result in a build-up of net positive charge in the oxide layers, inducing a flat band voltage shift. From the results presented in this section 8.5, the flat band voltage shift induced following TID in the CIS115 appears to localise the charge build-up to a region under the FD as opposed to the TG. This is however contrary to previous research, where charge build-up is related to oxide thickness (Schwank et al. 2008) suggesting that the relatively thicker oxide present under the TG in the CIS115 compared to the FD has an increased number of trapped charge present following TID. As a result of this, the damage mechanism in CIS115 following TID requires further investigation.

8.6 Conclusions and further work

The image lag in the CIS115 depends on the Φ TG and VREFR voltages. Optimum selection of these voltages shows improvement of the image lag, and as such offer the best performance for the CIS115 as a scientific imager. The optimum transfer gate voltage has shown to be 2.65 V, where the best image lag performance has been seen for CIS115 devices unirradiated and following TID and TNID. The optimum VREFR voltage has been shown to be 3.1 V. As a result of this best performance for the CIS115 JANUS camera on JUICE will be achieved using a Φ TG ON voltage of 2.65 V, however optimum VREFR recommendation requires further device testing heritage to ensure differences in performance across a range of devices will not occur.

When the CIS115 is subject to ionising radiation, the image lag knee-point is shown to shift to a higher signal level. This shift is not observed in other literature in 4T CIS and does not follow the observation that TID induces more positive oxide charge in thicker oxide layers. The shift in the knee point suggests that there has been an increase in the FD reset voltage or the potential under the FD (Figure 8-10). The fabrication of the CIS115 is expected to have a thicker oxide layer under the TG compared to the FD so the favourable build-up of charge under the thinner oxide layer is not well understood. Further investigation of this charge accumulation is therefore required to characterise the TID response of the CIS115. Moreover, a shift in the knee point of the image lag is seen in the CIS115 when changing the Φ TG. The shift in the knee point when varying both the VREFR and the Φ TG are shown to be

approximately equal at -15 e -mV-1 and 13 e - mV-1 respectively. From the results presented in 8.5.4, the image lag has shown improvement when increasing the reference gate voltage, where mean-variance analysis confirms the consistency of gain across the voltages used in the study, suggesting that the VREFR shift in knee point is due exclusively to varying VREFR.

Subjecting the CIS115 to a TNID fluence has shown to leave the image lag on the device beyond the knee-point unaltered. However, below this knee point, image lag has shown to increase. The suggestion is that it is due to the creation of bulk defects in the device. However, due to the statistical non-uniformity of proton damage, these are not expected to be uniform across the device and one should assume that there will be certain pixels with an increased image lag due to proton damage than some of their neighbours. As a result, a pixel-by-pixel method for analysis (typically seen when analysing dark current in 4T CIS) will be investigated in the next chapter to study further details about how the image lag increases below the knee point.

8.7 References

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Chapter 9: Pixel-by-pixel image lag analysis

9.1 Introduction

Image lag has been presented in Chapter 8: in terms of the average response of the CIS115, i.e., image lag is calculated across the whole photosensitive area. Individual pixels are known to differ in their fabrication and hence image lag should not be expected to be identical across the whole device. Several other detector characteristics are known to exhibit pixel-by-pixel variance, for example the dark current and readout noise. Due to these pixel variances, investigation of image lag through a pixel-by-pixel approach is implemented to better understand how image lag manifests.

9.2 Why consider a pixel-by-pixel approach?

To characterise image lag some data interpolation is required to obtain lag at the same signal for each pixel. Taking 'slices' at specific points in the signal level (x-axis) against image lag (y-axis) for each pixel will shed light on the way these pixels behave. This method is carried out in the following way:

- Specify signal level for lag calculation of a pixel, denoted as a "query point"
- Compute a logical operator to find electron signal level data points that are ±10% away from the query point
- Obtain the corresponding image lag data for these newly found electron signal level data points
- Obtain a linear equation in the form y=mx+c relating the signal (x) to the image lag (y) from these data points
- Substitute the query point into the determined relationship to obtain the image lag at the query point signal level for this pixel
- Repeat for all pixels in the device

Using this method, the pixel-by-pixel image lag is calculated. In section 6.2.2.4 the image lag was shown to have two regimes: before and after a knee-point. In Section 8.4 changes in

device performance with respect to TID and TNID is seen in the image lag on a macroscopic level and pixel-by-pixel analysis will investigate this in greater detail.

The image lag below the knee point in a BOL device is thought to be dominated by poor diffusion out of the photodiode. After TID little change is seen on the macroscopic level and with displacement damage, a small change is observed, as seen in Figure 8-4. Investigation of below the knee-point region following TNID on a pixel-by-pixel basis can identify whether this change is a global shift in all the pixels or a significant change in only a fraction of them. This could infer the degradation mechanism following TNID.

Above the knee-point at BOL, image lag is shown to be spill back dominated. The mean image lag in proton irradiated devices is shown to be largely unchanged in this region, however, a large shift in the image lag is seen in devices irradiated with TID. Investigating the image lag at this level on a pixel-by-pixel basis for TID devices will show if the change in image lag is the result of a global shift in the pixel population or due to the creation of a new image lag pixel population with a different, dominant lag source.

9.3 BOL behaviour

A BOL image lag histogram at 5000 electrons signal is shown in Figure 9-1. The data suggests there is a Gaussian-like distribution across the pixels with a mean centred at approximately 1.5 electrons lag. The width of the distribution is expected to arise from the noise on the measurement and due to the inherent difference in the pixels. This distribution clearly shows negative values, however in reality pixels are not expected to have a negative value for image lag and can be attributed to noise sources in the pixel output.

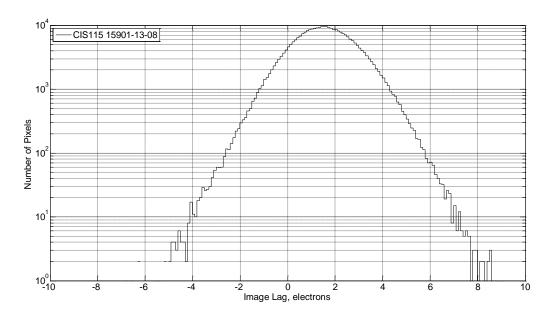


Figure 9-1: Pixel image lag at 5000 electrons signal of device 13-08 (control) at -50 °C. Distribution width characterised by the measurement error on the image lag/signal and the spread of the pixel behaviour of the device.

9.3.1 BOL behaviour with temperature

Slight improvements in the image lag performance with increasing temperature are seen in Figure 6-10. It is understood that the decreases in image lag is a result of the improvement of diffusion out of the photodiode and is expected to be a global shift across the device. The pixel-based image lag of the device in the range -50°C to -35°C is shown in Figure 9-2. The figure clearly shows that the temperature change affects the pixels across the whole device. This supports that at 5000 electrons signal, where the image lag behaviour is dominated by poor diffusion out of the photodiode (which has a dependence on temperature) the image lag increase is consistent for every pixel in the device.

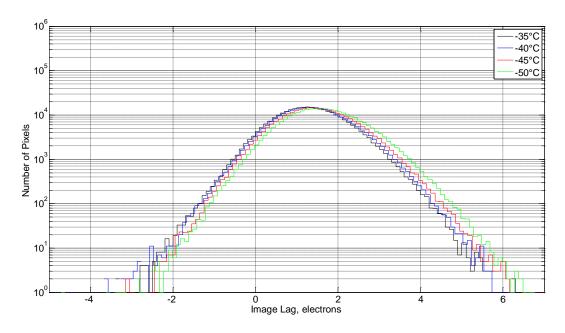


Figure 9-2: Pixel-by-Pixel Image Lag of device 13-08 at varying temperature at 5000 electrons signal.

At 5000 electrons signal image lag is dominated by poor diffusion out of the PPD at a BOL CIS115 this diffusion out of the PPD is thought to be governed by a thermionic emission. Han, Yao, and Theuwissen 2015 described this emission from the PPD to the TG as listed in Chapter 2, equation 7. As a result of I_0 being greater at higher temperatures, and the exponential function being minimised, this explains why the lag is improved at higher temperatures. In a plot of the natural logarithm of lag divided by the temperature squared, against the inverse temperature, one would expect there to be a linear relationship between the two which is seen in Figure 9-3.

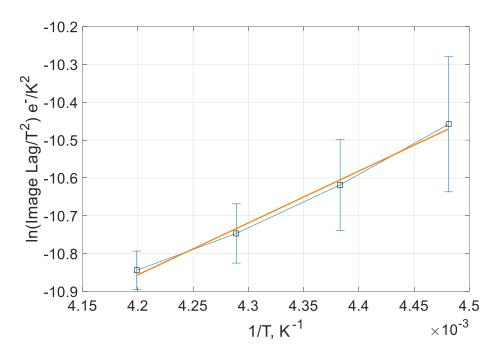


Figure 9-3: Natural log of the image lag over temperature squared against the inverse temperature. Error here is defined as the standard error on the mean.

9.4 Behaviour following displacement damage

Following displacement damage, the mean image lag (seen in Figure 8-4) has shown to increase below the knee point. Investigation into the response of image lag following TNID from protons at a signal interpolation level of 5000 electrons is shown in Figure 9-4. The small change in mean lag of proton DUTs seen in Figure 8-3 is therefore the result of the creation of a population of pixels that display high image lag. This is shown by a one sided 'tail' in the image lag, where pixels are shown to exhibit image lag well above 10 electrons. The high-lag pixels are believed to be induced by displacement defects induced by the TNID since the population grows with increasing levels of TNID,

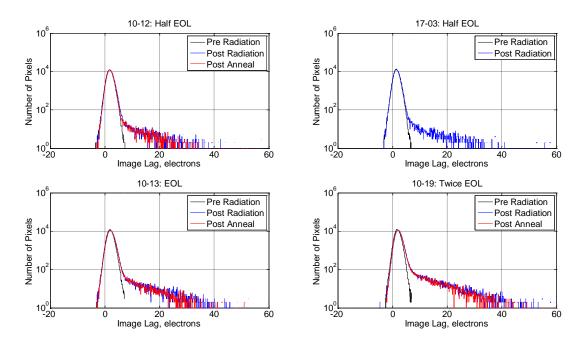


Figure 9-4: Pixel image lag at 5000 electrons signal of proton irradiated devices at -50°C for half End Of Life (EOL), EOL and twice EOL proton radiation. A 'tail' of pixels with exceptionally high lag is seen in each device, appearing to scale with fluence.

Figure 9-5 shows the pixel-by-pixel image lag in a device irradiated with neutrons. The same high-lag tail is present following irradiation, supporting the argument, that it is induced by displacement damage.

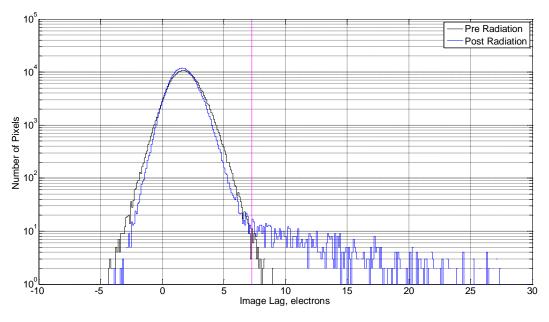


Figure 9-5: Pixel image lag at 5000 electrons signal for neutron irradiated device at -50 $^{\circ}$ C, where the pink line is the 5-sigma value from the Gaussian pre irradiation.

9.4.1 High lag pixels following TNID

9.4.1.1 Neutron and protons

Analysing the results presented in Figure 9-4 and Figure 9-5, pixels that exist outside a 5 σ deviation (to extract anomalous pixels exhibiting lag outside the Gaussian envelope fitted to the majority population of pixels) from the mean of a Gaussian fit to data at BOL are determined as high-lag pixels. Comparison of this neutron high-lag pixel count with respect to the proton fluence will assist the identification of the source of these high lag pixels. The relationship between the high lag pixels and fluence can be obtained from the sum of the pixels at above this 5σ level and is assessed here. The percentage of pixels exhibiting this high lag against the effective 10 MeV proton fluence is plotted. These results are presented in Figure 9-6, where a linear relationship is seen between the equivalent 10 MeV proton fluence (for proton DUTs) and the fraction of high lag pixel percentage. The neutron irradiated device has not been included in this plot since as discussed in Chapter 3:, neutrons are expected to create a higher number of defect clusters than their proton counterparts. Under the assumption that these high lag pixels are because of defect clusters, one would expect greater numbers of high lag pixels for the same NIEL scaled dose when comparing protons and neutrons.

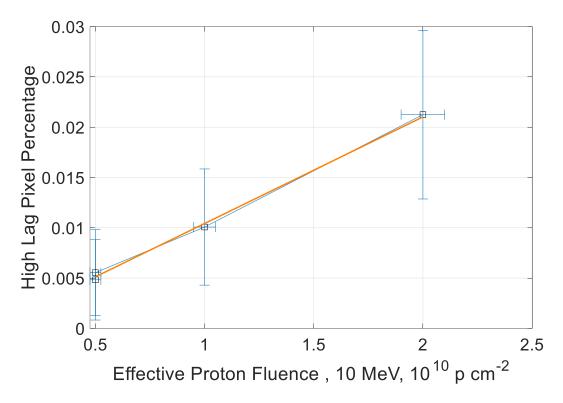


Figure 9-6: High Lag pixel percentage against effective 10 MeV proton fluence for TNID irradiated devices. A clear linear relationship is seen between high lag pixel count and proton fluence. Error bars are calculated as from the standard error on the bin count.

From Figure 9-6 the relationship between high lag pixel count and proton fluence (for devices irradiated with protons) is obtained. The linear relationship observed from Figure 9-6 as an equation is represented as:

$$y = 0.106x - 2 \times 10^{-4}$$
 Equation 9-1

Where x represents the effective proton fluence (10 MeV ×10¹⁰ protons cm⁻²) and y is the high lag pixel percentage.

9.5 Response following gamma irradiation

Investigation of the pixel-by-pixel image lag at 5000 electrons signal for gamma irradiated devices can determine if this high-lag pixel tail is exclusively a TNID effect or if the damage by γ -rays create these defects too. The analysis on gamma irradiated devices presented in Figure 9-7 show that the tail of high-lag pixels does not exist suggesting that TID does not induce any high-lag pixels. The pixel image lag at twice EOL has shown an increase in the mean of the image lag which can be attributed to a creation of a potential pocket in the

transfer pathway that can trap electrons during readout and has shown to occur at high TID in Goiffon et al. 2012 (see chapter 8 for more detailed explanation).

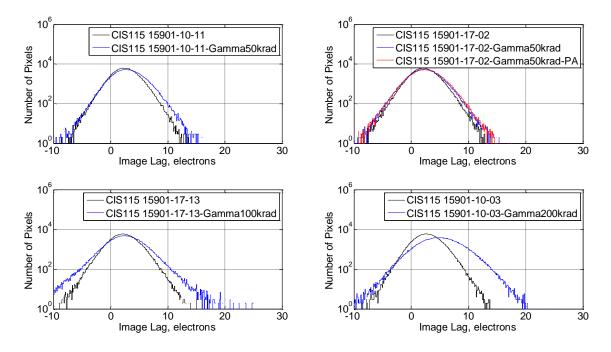


Figure 9-7: Pixel image lag at 5000 electrons signal for gamma irradiated device at -50 °C.

9.5.1 Studies to show high lag pixels are not correlated with DC defects or RTS

These high-lag pixels require further identification to determine their origins. Certain defects in pixels can be attributed to defects that are seen in the dark current of the device (Chapter 7) or can be attributed to Random Telegraph Signal (RTS) effects. Investigation of the relationship between high lag, dark current or RTS behaviour is detailed in this section. Due to the tail only existing on one side of Figure 9-7, one can expect these pixels to have no RTS like behaviour. Furthermore, since image lag data analysis involves subtracting an offset frame from both the lag frame and the signal frame, one can also expect that any bright defect pixels observed in lag will not be included in image lag analysis. However, for clarity into the behaviour of the device and to unequivocally rule these out as a source, these effects are still studied.

9.5.1.1 Dark current

The dark current of the high lag pixels for the twice EOL proton irradiated device is shown in Figure 9-8, and is shown alongside the dark current for all pixels. The results show that for

all pixels that exhibit this 'high-lag' the dark current is approximately within the mean response. As discussed in 7.4, proton damage is thought to alter the dark current through the creation of a high dark current pixel tail. Since the majority of these high lag pixels are shown to exist outside this high dark current pixel tail, the traps responsible for lag and dark current can be expected to be different. However, these traps may be identical, but only increase lag if they are present in a particular region of the PPD or TG channel, as opposed to traps anywhere in the epi that can result in high dark current.

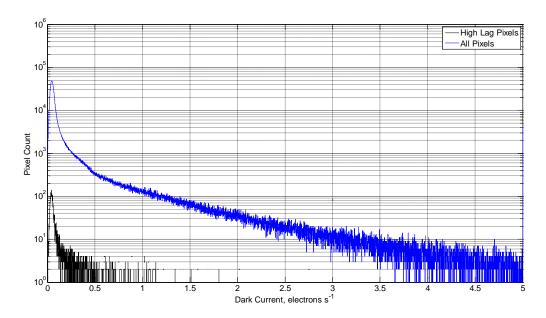


Figure 9-8: Dark current for the pixels that exist within the high lag pixel tail (black) alongside dark current for all pixels. High lag pixels are shown to predominantly have dark current within the main envelope and not in the dark current tail induced by TNID effects.

Most of these high-lag pixels shown in Figure 9-8 therefore have dark current representative of the main pixel population. Due to the known damage mechanisms of dark current increase following TNID (3.3.3.1) it can be postulated that the source of this high image lag does not arise from one of these damage species typically associated with DC increase.

9.5.1.2 Random Telegraph Signals

As stated previously, one can likely not consider Random Telegraph Signal (RTS) transitions within the pixel being a source for these high lag pixels. To provide further evidence of this, the output signal over time of some of the pixels exhibiting high-lag is studied, with pixels with both the highest lag and the highest dark current studied.

The method used in ascertaining the nature of RTS pixels is like the work on RTS presented in Dryer 2013. The analysis in this chapter does not hope to ascertain information about the nature of any RTS pixels (RTS work has already been carried out on the CIS115 in 2015, Winstone et al. 2015) but merely to confirm that pixels with high-lag are not falsely identified due to an RTS effect. Selecting the highest dark current pixels from the high-lag pixel population will investigate the pixels thought to be most damaged following TNID and will be used for RTS assessment.

Many images were recorded within stable illumination and temperature conditions over a long period of time to permit RTS analysis on the CIS115. This allows potential transitions of the dark current into another dominant state to occur and subsequently be observed. The pixel noise over a given time is obtained from the data and can be smoothed with a Gaussian filter. The signal can then be normalised and plotted into a histogram. A device where there are many signal transitions will possess multiple peaks in the histogram, whereas pixels exhibiting no RTS transitions will possess only one peak. Analysis on the 'high-lag high-dc' pixels show none of the RTS characteristics, with an example plot for RTS analysis of one of these 'high-lag high-dc' pixels shown in Figure 9-9. Clearly in the normalised noise amplitude (i.e., the smoothed amplitude divided by the maximum smoothed amplitude), only one peak in the histogram exists, suggesting there are no RTS transitions in the pixel.

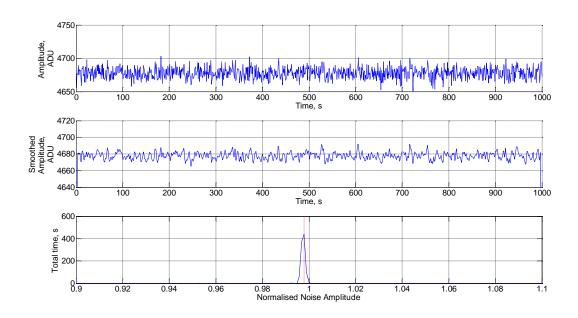


Figure 9-9: A representative RTS Analysis of High Lag and DC pixel for 10-13 proton EOL at -50°C

9.5.1.3 Spatial distribution of the high-lag pixels

To study the nature of the interaction of displacement damage with the introduction rate of high lag pixel, the spatial distribution of the high lag pixels was investigated. This can suggest if the high lag pixels have any preferential locations within the CIS115. If the high-lag pixels were simply caused by the displacement damage, then the distribution would be expected to be as uniform as the irradiating proton beam (better than 10% uniformity). The high lag pixels for each column and row at the twice EOL protons is shown in Figure 9-10. It appears that in both the columns and rows of the device there is no significant spatial correlation for high lag pixels confirming no preferential location for the damage. From this, it can be concluded that the high-lag pixels are not due to a particular defective column or region of the device that could have stemmed from manufacture.

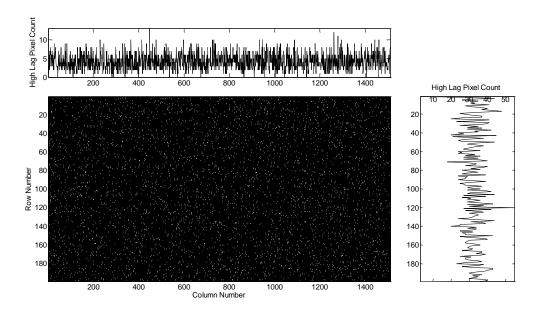


Figure 9-10: High Lag pixel placement in the CIS115 alongside the column and row plots of sum of high lag pixels. From the sum of pixels in the rows/columns there is no preferential location for these high lag pixels in the CIS115.

9.6 Pixel-by-pixel study of the knee-point shift with TID

The same technique that probes the signal at 5000 electron illumination is used to probe the transition of the knee point of the image lag in the DUTs. The results shown in Section 8.5 suggest that TID is responsible for inducing a knee-point shift in the mean image lag. As discussed in Section 9.2, pixel-by-pixel analysis of this knee-point shift will identify this shift being either a global shift that affects every pixel in the device equally or is a new population of pixels responsible for this shift in the knee point. Section 8.5 suggests this knee-point shift

occurs primarily in gamma-irradiated devices and as such these will be investigated first here.

Image lag behaviour at 17500 signal electrons level for the control device is shown in Figure 9-11, where it is thought to be spill back dominated. Image lag ranges from around 140 electrons to 240 electrons which represents around 0.8% to 1.4% of the signal. Noise contributions can arise from both read noise and from the shot noise along with the probability of spill-back. As the signal level here (17,500 electrons) is greater than the results presented in 9.4, the noise, and therefore the width of the distributions here are expected to be wider.

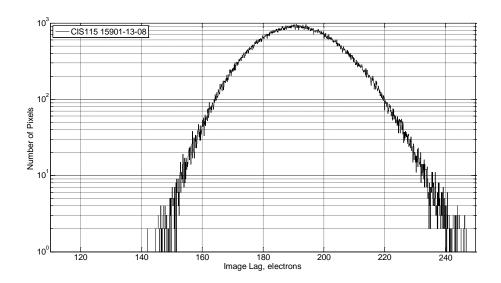


Figure 9-11: Pixel Image Lag of control device 13-08 at 17,500 electrons signal. Image lag at this illumination level governed by a distribution bounded at image lag of approximately 150 electrons and 240 electrons with a mean at approximately 190 electrons.

Following on from the behaviour of the device at 17,500 electrons, interpolation in the y axis at 0.5% image lag on data which includes percentage lag (y axis) against illumination signal (x axis) can be used to determine the knee-point by extrapolating an x-intercept since this region is thought to be where signal level and image lag are linearly related. Performance at BOL (CIS115 13-08) with respect to the image lag knee point is shown in Figure 9-12. The image lag knee point for this device is shown to vary from approximately 8500 electrons to approximately 10500 electrons. It is thought that the width of the distribution is governed by the contribution of varying noise sources in the device such as the shot noise on the illumination, the pixel read noise.

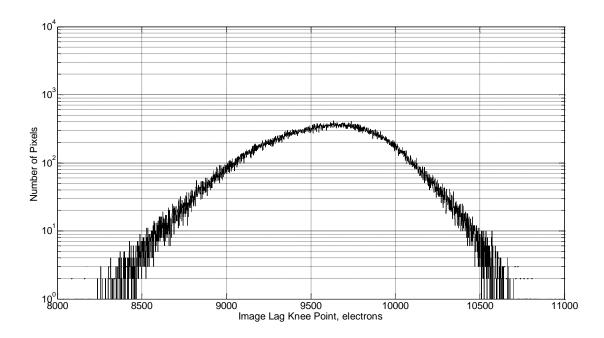


Figure 9-12: Image lag knee point signal level at BOL performance for CIS115 13-08 calculated through an extrapolation at 0.5% lag. At this lag level, the knee point is taken as the x intercept of this extrapolation.

9.6.1 TID pixel image lag knee point investigation

When the signal in the device is approximately 17,500 electrons the image lag is largely spill-back dominated. Therefore, image lag analysis at this signal level for TID irradiated devices delves into the spill-back regime of CIS115 devices. The results are shown in Figure 9-13.

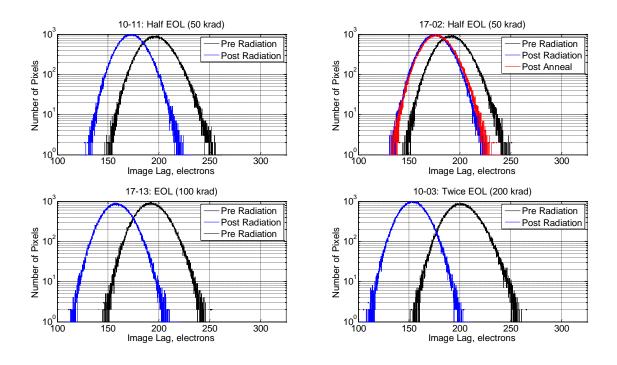


Figure 9-13: Pixel image lag response of TID irradiated devices test pre-radiation, post radiation and post anneal (PA) at 17,500 electrons signal.

Figure 9-13 shows that the change in the image lag that occurred in the gamma-irradiated DUTs can be attributed to a global shift of the image lag of the device as the pre and post radiation distributions appear to be identical, and scales with TID. This means that the mechanism for decreasing the image lag induced by TID occurs uniformly across the whole device, where the whole pixel population image lag is decreased by approximately 50 electrons at the highest TID and approximately 25 electrons at the lowest TID. This means that γ -rays from the Co-60 source damage uniformly across the device as opposed to being localised to a given region. In the same way, the observations in the non-irradiated 13-08 device (Figure 9-12), the knee point of the TID device is extracted to better explain how this shift occurs. A knee point occurring at a higher signal level means that the spill-back regime in the CIS115 occurs later in the device, and as such explains the reduced levels of image lag at a pixel-by-pixel level seen in Figure 9-13. This is shown in Figure 9-14, where clearly following TID the knee point of the device is shown to move toward higher signal.

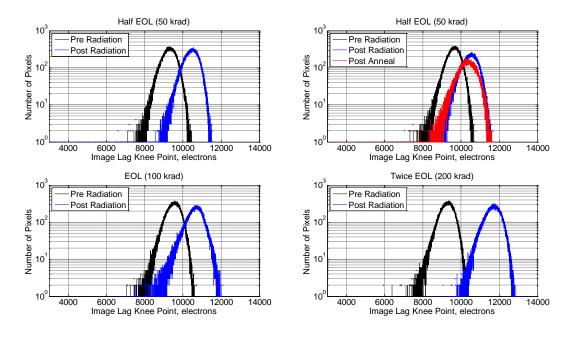


Figure 9-14: Image lag knee point of TID DUTs calculated using the same technique applied for Figure 9-12.

The shape of the distributions before and following TID appear to be identical, with the change in the image lag knee point represented by a shift in the pixel response in the positive x-direction. The largest change is clearly visible in the 200 krad gamma-irradiated device, and the results presented in Figure 9-13 and Figure 9-14 show that the knee point shift following TID is a global shift across the device. From Figure 9-14, the appearance of the distribution pre and post TID still appears to be approximately the same shape, where differences can predominantly be noted in the width of the distribution. This can be explained if one considers the noise to be larger following TID. The similarities between pre and post TID means the radiation damage is uniform across the device.

9.6.2 TNID image lag at knee point investigation

No knee point shift is seen in the mean response of the image lag in proton and neutron irradiated devices (Figure 8-4) but as already shown in Section 9.4 protons can induce a species of high lag pixels that may not be seen in the mean response of the device. The results of the proton irradiated devices image lag response at 17,500 electrons signal are shown in Figure 9-15. No observable change is seen in the TNID devices which can suggest that there has been no change in the image lag on the device at this signal level, or that at this signal level, the spill-back mechanism for image lag dominates the lag performance of the device, where the cause of these 'high-lag' pixels (e.g. defect clusters) seen in 9.4 are significantly less dominant than spill back in the CIS115.

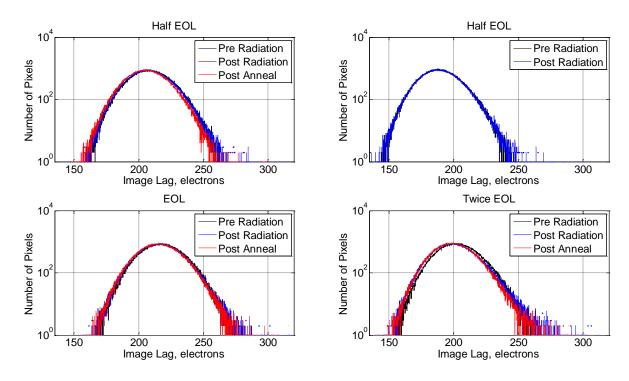


Figure 9-15: image lag of proton irradiated devices at 175000 signal tested pre-radiation post-radiation and post anneal.

From the results at 17,500 electrons signal, a small shift in the pixel-by-pixel image lag is seen at twice EOL ($2x10^{10}$ 10MeV protons cm⁻² equivalent), suggesting that there has been some improvement in the image lag at this fluence. One can suggest this shift is due to the TID from the protons where the TID at $2x10^{10}$ 10 MeV equivalent protons cm⁻² is 5.088 krads. Figure 9-16 shows the response from TNID neutrons. Since the 10MeV proton equivalent fluence shown here ($1.09x10^9$ 10 MeV protons cm⁻²) is less than the lowest proton fluence (where nearly zero change in pixel lag is seen pre and post radiation) it cannot be used to ascertain if this shift is due to the TID from protons, however a shift in the neutron irradiated device is observed, potentially suggesting that TID from protons is not responsible for the shift. This means that the difference seen at twice EOL ($2x10^{10}$ 10MeV protons) could also be due to systematic error on the CIS115 camera setup as the results are taken at different times. As no change is observed on a pixel-by-pixel basis at 17,500 electrons signal, that there will be no shift in the image lag knee-point, so the results presented at 17,500 suffice to show that the image lag of the device following TNID is unchanged in the spill-back image lag dominated regime.

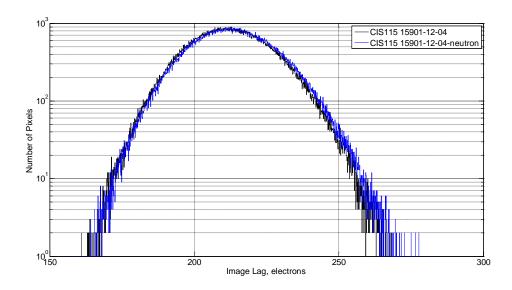


Figure 9-16: Pixel image lag response of neutron irradiated device at 175000 electrons signal tested pre-radiation and post-radiation.

9.7 Discussion

Pixel image lag at 5000 electrons signal following TNID shows high-lag pixels have been introduced into the device. In addition, the shift in the mean image lag of the device that was seen in Section 8.4 was not due to a global change in the behaviour of the device. Due to the work carried out in Section 9.5.1 it is determined that the origin of the high lag is not correlated to dark current defects or a feature induced by RTS transitions within the pixel. Point defects have been ruled out as a candidate for the cause of this image lag as these only have the capability of trapping very few numbers of electrons and cannot account for the high levels (some of these high-lag pixels have lag exceeding 20 electrons) of lag observed. A more likely candidate for the cause of these 'high-lag' pixels is a trap site that can trap multiple electrons for emission in later frames.

As the high lag pixels are shown to have DC like the mean response, these traps can therefore be ruled out as dark current traps located at the PPD space charge region as this is shown to increase DC following TNID (Virmontois et al. 2014). Further work into the trap responsible for the high lag pixels, will shed further light into them. In Section 9.4.1.1 a linear relationship is shown between high-lag pixel count and proton fluence. Extending the testing to higher proton fluences (greater than $2 \times 10^{10} \, 10$ MeV proton equivalent cm⁻²) will generate more data points and confirm if this linear fit is accurate, or if the behaviour can be represented by an alternative relationship.

9.8 Conclusions and further work

9.8.1 Novel method

Image lag analysis on a pixel-by-pixel basis has not been reported in other studies into image lag for 4T CIS and is a novel method for analysis of image lag. This method allows for the characterisation of the way that image lag manifests itself in a more detailed way and helps to identify more accurately discrepancies that are seen in the mean response of the device, determining potential candidates for image lag changes seen following TID and TNID.

9.8.2 Charge trapping capability of high lag pixels

Following TNID, a tail of high-lag pixels is seen in the CIS115. The population in this tail has been shown to scale linearly with the TNID when analysing a single irradiation species (and energy). The image lag of these 'high-lag' pixels at 5000 electrons signal is shown to contain many tens of electrons. Following the work shown in Section 9.5.1, which rules out dark current and random telegraph signal as a potential source for these high-lag observations, it is likely that these pixels are the result of defects in the bulk silicon, with the capability of trapping many electrons. Further work into the characterisation of these pixels is required to determine the type of traps. Due to the expectation that these traps may be thermally active, one could attempt to operate the CIS115 at progressively lower temperatures to ascertain if the defect source resulting in these high-lag pixels can be frozen out and determine a list of potential candidates through this method.

9.8.3 Implications for JANUS

Due to the low number of pixels seen to exhibit this 'high-lag' performance (3.6 % at twice JUICE EOL fluence) it is expected that they will have a negligible effect on the overall performance of the detector. Image lag has shown to be more greatly affected by the TID (where image lag is shown to decrease on a pixel-by-pixel basis). One can therefore say that although this pixel-by-pixel image lag study has obtained new information about the image lag performance of the detector, the effects observed following TID at low signal level, are thought to be a low contributing factor to the overall performance of the device.

9.8.4 Implications for future CIS high performance applications

Although it has been shown previously that the implications of these high-lag pixels are largely insignificant for the JANUS mission due to their low number, these results may still be

significant for future high-performance CIS applications. When CIS are required for specific applications in environments with high displacement damage, these high lag pixels may become significant when very high accuracy images are required and as such, this phenomenon may need to be corrected for.

Further work for high lag pixels generated from TNID in the CIS115 can involve characterisation of these high lag pixels with higher neutron fluences. Since a neutron irradiation generated more high lag pixels than its proton equivalent fluence would suggest given the relationship found in Equation 9-1, testing at higher neutron fluences will mean that a better relationship between neutron fluence and high lag pixels can be determined. In addition to this, if the damage responsible for these high lag pixels has a specific temperature dependence, testing at lower temperatures than the ones used in the testing may suggest a temperature where these high lag pixels no longer manifest.

9.9 References

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Chapter 10:Conclusions and Future work

This work has involved the characterisation and optimisation of the CIS115 for the JANUS camera on JUICE. Explanation of the development of the gamma irradiation is discussed in 10.1, the main mission optimisation discoveries of this work are summarised in 10.2 with the main scientific discoveries shown in 10.3 and 10.4. Future work and prospects concerning the CIS115 are discussed in 10.6.

10.1 Test development

Characterisation of the CIS115 required the development of many test procedures. A key part of the work in this thesis involved the organisation of the gamma irradiation of the CIS115. The careful planning and scheduling allowed for the CIS115 to be irradiated to three different total ionising doses of 50 krad, 100 krad and 200 krad at the Co-60 facility ESTEC, Netherlands.

10.2 Sensor Optimisation

From the work that has been carried out, key operational parameters for the device have been established. Chapter 8: investigated the possibility of image lag reduction in the CIS115 and concluded that operation with a lower Φ TG (set to 2.65 V) can drastically reduce the image lag. Moreover, this Φ TG reduction has increased the knee-point of the device, i.e., the point at which the CIS115 image lag performance becomes spill-back dominated. This knee point shift has shown to significantly improve the image lag of the CIS115 at higher signal levels. From the research carried out here (with a host of devices undergoing full characterisation) this voltage has been recommended to the JANUS camera team for use on the CIS115.

10.3 Image lag

The mean lag of the CIS115 was characterised at Beginning of Life (BOL) and following a range of irradiative sources. Following TID an accumulation of trapped charge in the device resulted in the increase in the image lag knee-point of the CIS115. Due to the image lag results, this charge build-up in the region under the transfer gate can be ruled out, as increasing the voltage under the transfer gate would in fact reduce the image lag knee-point in the CIS115.

As a result, TID in the CIS115 (up to 200 krad) has shown to improve the image lag performance of the device at high signal levels.

A novel pixel-by-pixel characterisation method was developed and carried out on the CIS115 allowing a population of high lag pixels induced in the device following TNID to be identified. The number of these high-lag pixels has shown to scale linearly with the proton fluence's 10 MeV proton equivalent displacement damage dose but does not correlate to that of neutron fluence. If these high lag pixels originate from a bulk defect cluster, the difference between the proton and the neutron high lag pixel count is inferred since neutrons are more likely to create bulk defects when compared to protons. In addition, these high-lag pixels are uniformly spatially distributed, and have not shown any correlation to anomalous dark current or random telegraph signal behaviour.

10.4 Dark current

The dark current of the CIS115 at BOL in the warm regime (+30 °C to +40 °C) is investigated and using the dark current activation energy analysis can be concluded to be diffusion dominated, with a potential source of this dark current being from back surface diffusion, where a back surface pattern appears in Figure 6-9.

It is demonstrated that gamma irradiation induces common trap sites within the band gap which increases the dark current of the detector. Thermal annealing of the device has also shown a slight reduction to the dark current of some of the pixels suggesting the source of dark current created during radiation has been partially annealed.

The dark current of the CIS115 following TNID is also investigated. A clear exponential tail in the dark current spectrum of the device is seen, suggesting that, similarly to other CIS, the dark current increase following TNID can be explained through the creation of high dark current pixels outside the main dark current population. Thermal annealing has shown to reduce the dark current of some of the pixels in the device, suggesting the source of dark current within those pixels can be partially annealed at 100°C. The activation energy of proton and neutron irradiated devices also suggest that a dark current species scales with proton fluence, where a peak in Figure 7-14 increases after proton irradiation.

10.5 CIS115 Mission performance

In Chapter 4: the mission performance of the device was introduced in Table 4-4, which shows the image lag requirement of the CIS115 is less than 1 % at 50 % of the linear full well capacity of the device ($50 \% Q_{LIN}$, 13,500 electrons). Figure 8-3 shows that the mean image lag performance following TNID at this signal level is almost unchanged, and Figure 8-5 shows that the mean image lag of the device following TID at this signal level has improved where both figures show the image lag to be less than 1 % at signal levels as high as 15,000 electrons. As both irradiative sources have shown almost no change in the image lag between BOL and EOL besides an increase in the image lag knee-point, even the combination of TNID and TID on a device will result in mean image lag within mission requirements i.e., less than 1 % at $50 \% Q_{LIN}$.

10.6 Future Prospects

From the work carried out during this thesis the CIS115 has been shown to be within specification in key electro-optical parameters for the duration of the JUICE mission and following some operational changes the device has shown to outperform the initial requirements placed upon it in areas such as dark current and image lag. As a result of this, the design of the CIS115 and the knowledge obtained from this thesis can be used in the operation of other 4T Teledyne e2v CMOS Image Sensors, where these devices may profit from differing bias voltages to improve their performance.

In addition to this, due to the heritage that the CIS115 will obtain on JUICE, and the host of research that has been carried out on the device the detector has become a candidate for other missions. Some of these include the ALTIUS (Atmospheric Limb Tracker for the Investigation of the Upcoming Stratosphere) mission to be used as a visible imager and the Hera Saturn entry probe (Mousis et al. 2016) for example. In addition to this, the CIS115 has been selected as the prime detector for the visible imager on ESA's Comet Interceptor Mission, which will take images of a comet.

Both the dark current and image lag analysis has led to these methods developed being adopted for further analysis of the CIS115 in the JANUS team. The pixel image lag characterisation will form the base for how the image lag is presented in the CIS115 for the JANUS camera and can become an important metric for expressing the image lag in all 4T CIS.

The dark current characterisation at warmer temperatures led to the understanding that the CIS115 quite easily meets the mean requirements for the JANUS camera. Further work on dark current at cold temperatures is required as this is predominantly the limiting factor in the dark current performance of the CIS115.

10.6.1 Further work

As discussed in Section 10.3 the image lag following TID is shown to decrease. The origin of this degradation is not well understood as is not observed on another 4T CIS. Further work following on from this thesis should include a study into the location of the net positive charge build up that induces a shift in the knee point of the device, a knee point shift also seen when changing the Φ TG and VREFR voltages. This could be carried out by characterisation of image lag performance of the CIS107, where different pixel structures are employed in the device with different TG sizes (length and width) and varied PPD sizes (perimeter, length, and width).

Following on from the image lag results, the correlation between high lag pixel count and neutron fluence should be investigated. This will likely involve irradiation of the CIS115 with greater neutron fluences to investigate the hypothesis that neutrons are more effective at inducing high lag pixels than protons of the same equivalent displacement damage dose. One such facility that could be used to irradiate the CIS115 to higher neutron fluences is the ISIS Neutron and Muon Source (more specifically the ChipIR instrument) that offers the capability for rapid testing of high energy neutron effects.

10.7 JUICE

At time of writing, flight model CIS115s have been delivered to DLR Germany (The German Aerospace Centre) where they are currently being integrated into front end camera electronics. The engineering model of the telescope has also been assembled at spacecraft prime in Toulouse. The JANUS team are currently working toward an instrument delivery scheduled for Q 4 of 2020. JUICE is due to launch in 2022 and will start returning science data from approximately 2030, something everyone on the team, myself included is looking forward to.

10.8 References

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