A PLL-BASED FREQUENCY SHIFT MEASUREMENT SYSTEM FOR CHEMICAL AND BIOLOGICAL SENSING

A Thesis

by

WILLIAM JAMES TORKE

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2011

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Samuel Palermo
Committee Members,	Kamran Entesari
	Xing Cheng
	Terry Thomas
Head of Department,	Costas Georghiades

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ABSTRACT

A PLL-Based Frequency Shift Measurement System for Chemical and Biological Sensing. (December 2011)

William James Torke, B.S.E.E., Purdue University

Chair of Advisory Committee: Dr. Samuel Palermo

A PLL-based frequency shift measurement system for chemical and biological sensing was developed and implemented in the form of two discrete electronic assemblies. One of the assemblies consists of a VCO which contains a microwave resonator sensor while the other assembly contains commercially available PLL and MCU devices, as well as various other discrete components. When mated together, a PLL-based frequency synthesizer is realized, the output frequency of which is ∼4.5 GHz. The system is used to measure the frequency shift exhibited by the frequency synthesizer when several commonly-known chemical substances are applied to the microwave resonator sensor test fixture. Because the amount of measured frequency shift is proportional to the dielectric constant of a given material under test (MUT), this system can potentially be used as part of a chemical identification system. This measurement system is also attractive in that it represents a stand-alone or 'self-contained' system which does not require usage of any additional expensive and bulky electronic diagnostic equipment such as a network analyzer or signal generator, making it a relatively inexpensive and portable solution. Attempts to use the system to measure frequency shift resulting from application of various common chemical substances to the sensor fixture results in derivation of dielectric constant values which hold very close agreement (±2%) to the published/theoretical dielectric constant values for each respective chemical substance.

To my family, without whose support this work would not have been possible.

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I would also like to express particular gratitude to my research partner, Vikram Sekar, with whom I worked closely throughout this research. His advice and consultation were extremely beneficial to my day-to-day progress. It was a great pleasure to work with Vikram because of his incredibly amicable personality. Special appreciation is also directed to Vikram's graduate advisor and a participating member of my graduate committee, Prof. Kamran Entesari. Prof. Entesari was the conceptual leader and visionary of this research project. His guidance was most critical to the successful completion of this research.

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CHAPTER I

INTRODUCTION

A. Motivation

Development of sensors based on microwave resonator structures continues to expand, out of motivation to develop accurate and reliable measurement/detection devices targeted for numerous commercial and research applications. Such applications include:

- substance identification, in applications such as forensics and customs inspection at ports of entry [1][2]
- measurement of chemical purity, in applications such as the manufacture of pharmaceuticals [3][4]
- measurement of moisture content various materials [5] such as crude oil [6][7] and grains [8][9]
- measurement of purity of gasoline in storage tanks [10]

The essential mechanism which allows a microwave resonator to function as a chemical sensor pertains to the alteration of the resonator's impedance characteristic when a particular chemical, referred to as the material under test (MUT) is placed around, over, or in the vicinity of the resonator structure. This concept is illustrated in Fig.1, in which a liquid chemical substance is being deposited over a *planer* microwave resonator. A planer microwave resonator consists of a two-dimensional geometric pattern of metallic conductive traces (such as copper) etched onto a printed circuit

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´The journal model is *IEEE Transactions on Microwave Theory and Techniques.*

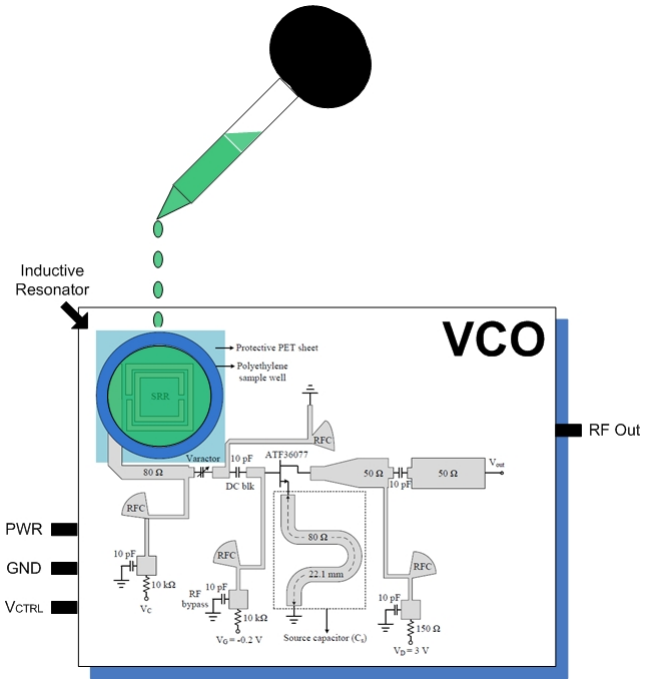


Fig. 1. Deposition of a chemical substance over a planer microwave resonator.

board (PCB), placed in the vicinity of another trace which functions as a transmission line within a resonator circuit.

Another promising application which could employ a planer microwave resonator-based sensor pertains to bio-medical sensors intended for detection of genetic diseases and conditions, bio-threats, and food and drug safety [11][12][13]. Similar to the case for chemical sensors, the resonator structure can function as the sensor component for such applications due to the resonator network's tendency to exhibit a change in its impedance characteristic. In this case the alteration of the resonator's impedance characteristic is caused by successful hybridization of DNA molecules occurring on resonator structure.

For both of the applications described above (chemical sensing and DNA detection), the alteration of the resonator's impedance characteristic is caused by the change in the strength of the electric fields which exist between the neighboring metal-

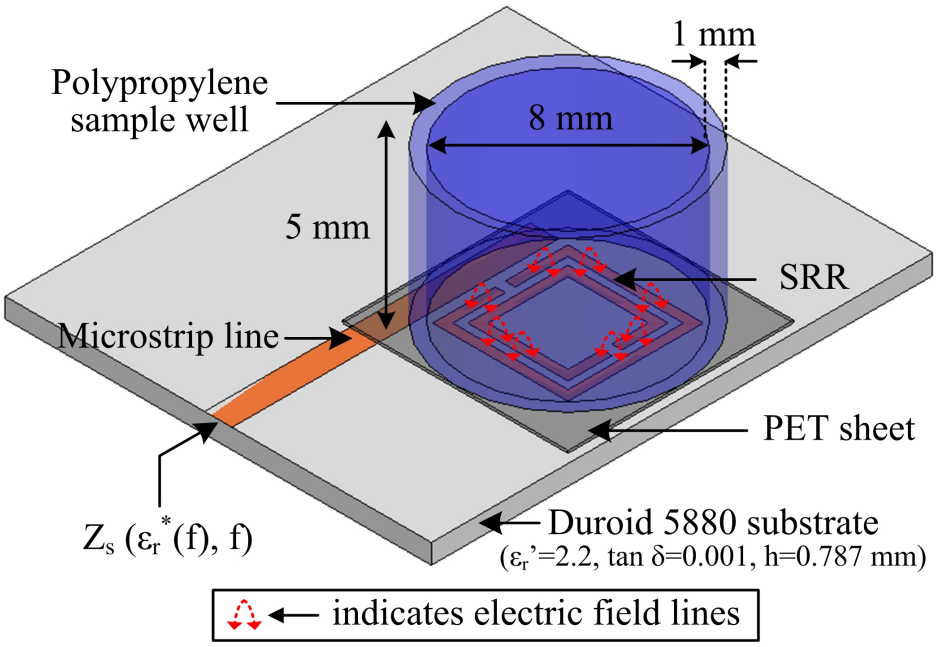


Fig. 2. Illustration of altered electromagnetic fields caused by presence of liquid substance placed over planer resonator structure.

lic traces which make up the resonator structure, when the MUT is introduced to the sensor. The direction and strength of these electric fields which exist in the vicinity of the resonator structure are altered due to the MUT's unique dielectric properties. This phenomenon is illustrated in Fig. 2. This figure depicts a typical implementation of a planar microwave resonator. The double-arrowed indicators in this figure represent exemplary lines of electric field existing between the metallic resonator traces, which oscillate in strength and direction in unison with the resonators oscillation frequency.

Such alterations in a microwave resonator's impedance characteristic upon application of the MUT will also result in a shift in the resonant or "natural" frequency of the resonator structure. The magnitude of this shift in resonant frequency is directly related to the MUT's dielectric constant (ϵ_r'). Therefore, various different chemical substances (or alternatively, various unique DNA samples) can potentially be identi-

fied with a high degree of certainty by performing a reasonably precise measurement of the shift in the resonator's natural frequency.

Measurement and detection devices which employ microwave resonator-based sensors have the potential to achieve comparable, perhaps even superior detection and measurement capability in comparison to existing sensor technologies [14]. At the same time, it is likely that such microwave resonator-based sensor devices could allow for more compact and less expensive commercially available sensor equipment, in comparison to existing technologies.

Numerous recent research efforts have investigated use of *passive* resonators for chemical detection (identification) and chemical spectroscopy [3][15][16], which essentially apply the approach described above. While there are numerous variations of the exact technique by which the resonant frequency shift measurement is performed, essentially the approach is to experimentally obtain the input impedance characteristic (S_{21} or S_{11}) of the resonator network, and to then graphically identify a numeric measurement of the network's resonant frequency. This is often achieved using a network analyzer. The impedance characteristic is obtained both *before* and *after* deposition of the MUT to the resonator. Then the shift in resonant frequency can be computed as the difference in the resonant frequencies measured under these two conditions.

One limitation of the usage of passive resonator sensors concerns a decrease in the sharpness of the impedance characteristic as larger volumes of the MUT are deposited onto the resonator. The shape of the impedance characteristic can become so flat or 'dull' that the resonant peak of the characteristic can no longer be identified with reasonable accuracy. This effect is illustrated below in Fig. 3. Another potential issue associated with usage of passive resonators for chemical detection pertains to its economic practicality. The need for an expensive and bulky network analyzer

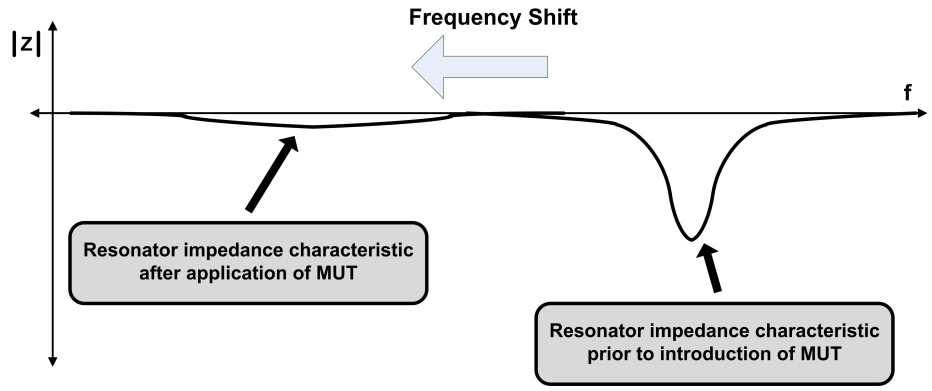


Fig. 3. Illustration of flattening in passive resonator's impedance characteristic upon deposition of chemical substance.

to obtain the passive resonator's impedance characteristic and from that identify its resonant frequency poses challenges for realization of a relatively low-cost and portable measurement system.

The limitations pertaining to usage of passive resonators mentioned above can be mitigated by employing an *active* resonator (essentially, an oscillator) instead of a passive resonator network. Such an oscillator will contain a passive resonator network at its core, and typically will include an active device to allow for sustained oscillation within the resonator tank. This alleviates the need to provide an external signal source to the resonator network. More than one of the common negative-resistance LC oscillator topologies can be implemented to realize a practical active resonator circuit, in which the resonator onto which the MUT is applied constitutes at least part if not all of the oscillator's LC tank. One such architecture is shown in Fig. 4.

By including a simple DC voltage source, power can be provided to the circuit to bring about a sustained oscillating output signal, the frequency of which is [primarily] determined by the resonator's natural frequency. Additionally, because such a negative-gm oscillator can easily be designed for a very high Q-value by matching the -1/gm value of the active device to the resonator network's passive resistance,

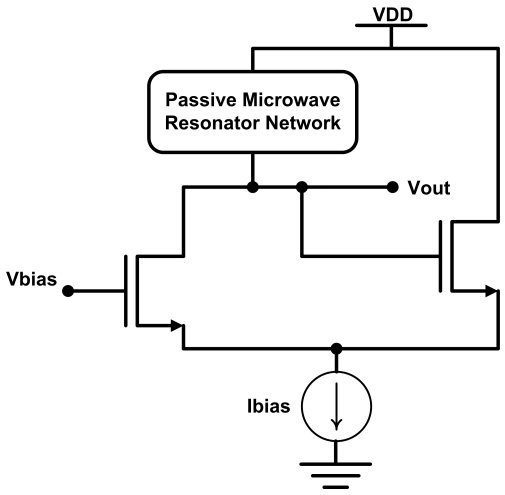


Fig. 4. Simple example of oscillator circuit architecture with passive microwave resonator tank core.

R, ($Q = \sqrt{L/R^2C}$), the phase noise profile of the oscillator output will maintain a relatively discernible peak even when the resonator's natural frequency suffers a significant shift (i.e., due to introduction of a relatively large volume of MUT onto the resonator). Therefore a chemical detection system using an oscillator with an active resonator sensor core to measure shift in the resonator's natural frequency can conceivably be realized by connecting such an oscillator to a frequency counter, as shown in Fig. 5. A low-cost microcontroller could easily read the digital frequency counter output value both before and after the MUT is applied to the resonator, and then the shift in resonant frequency can be obtained by computing the difference in the two frequency measurements. Since this approach would not require use of a spectrum analyzer, it represents a much less expensive solution, compared to the passive resonator technique described previously.

B. Proposal of Research

1. Implementation of PLL Architecture with ADC and MCU for a Frequency Shift Measurement System

Realization of a monolithic frequency counter device which can accurately measure signal frequencies in the 5+ GHz range (a nominal output frequency range for such microwave resonator-based oscillators) is certainly achievable. However, depending on the silicon technology that is used, realization of this function is not necessarily trivial at such a relatively high frequency. Additionally, phase noise in the oscillator output can present difficulties in a frequency counter's ability to accurately measure the oscillator's output frequency, and therefore represents a source of measurement error. One possible alternative which could alleviate the need to use a frequency counter for measurement of the resonator's frequency shift would be to deploy the resonator as the core of a *voltage-controlled oscillator (VCO)* circuit. The VCO provides a voltage input which allows the output frequency to be varied in a linear fashion with respect to the voltage level applied to this input. The VCO output frequency can *also* be varied by the introduction of the MUT to the microwave resonator structure. The VCO can then be incorporated within a phase-locked loop (PLL). In this configuration, time-domain measurement of the relatively low-frequency PLL control voltage can be

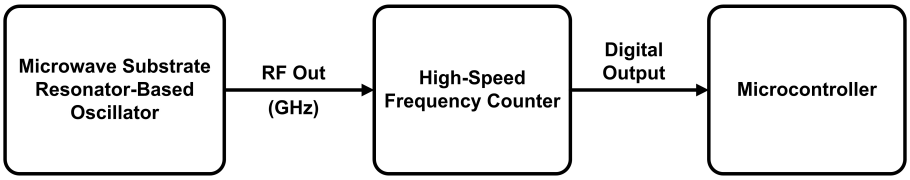


Fig. 5. System diagram of open-loop frequency shift measurement system. The microwave substrate resonator within the oscillator constitutes the chemical sensor apparatus.

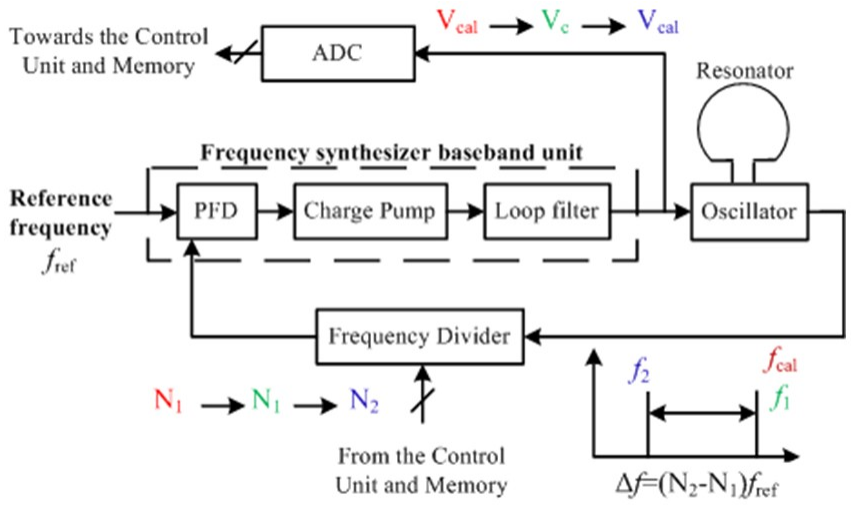


Fig. 6. Block diagram of proposed PLL-based frequency-shift measurement system using ADC and MCU.

used to indirectly measure the frequency shift of the resonator. The control voltage could be measured by an analog-to-digital converter (ADC) and a microcontroller (MCU) could store the digitally sampled voltage measurements both *before* and *after* the MUT is applied to the resonator. A block diagram of such a system is shown in Fig. 6.

In comparison to use of the active oscillator in an open-loop configuration (Fig. 5), such a PLL-based frequency shift measurement scheme potentially provides more than one appealing features:

- As just mentioned, such a solution provides a relatively low-frequency voltage signal which varies in proportion to the VCO output frequency. This voltage signal could be digitally sampled using an analog-to-digital converter (ADC), thereby providing a convenient method for quantitative measurement of the frequency shift exhibited by the VCO when the MUT is applied to the microwave resonator. Oversampling (averaging) techniques can be deployed to reduce the effects of noise on the voltage measurement, thereby providing increased preci-

sion of the frequency shift measurement.

- With strategic selection of the PLL bandwidth characteristic, it may be possible to further suppress the effect of oscillator phase noise on the control voltage output, and thereby achieve greater precision of the frequency shift measurement in comparison to the open-loop solution depicted in Fig. 5.

The frequency shift measurement system described just above, which incorporates a VCO containing a microwave resonator sensor into a PLL with capability to digitally sample the control voltage, may represent a practical solution for a chemical and/or DNA detection device. Furthermore, in comparison to other recent approaches, this solution could prove the viability for manufacture of a low-cost, standalone, portable, reasonably accurate chemical sensor system which does not presently exist.

2. Formal Proposal of Research

The proposal for (i.e., the primary goal of) this Master of Science Thesis Research Project was to develop an electronic frequency-shift measurement system consisting of a PLL, an ADC and MCU. This required development of a discrete electronic assembly which contains an ADC, MCU, and all functional components of the PLL with the exception of the VCO block, which was to be implemented on a separate assembly. The VCO is connected to/from the PLL assembly through SMA coaxial cables. Referring to Fig. 6, the VCO assembly contains the critical planer microwave sensor, onto which the MUT is deposited. The ADC will measure the voltage level of the control voltage fed to the VCO input. The digitized ADC measurement of the control voltage will be the quantity used to indirectly calculate the shift in frequency exhibited by the VCO due to introduction of the MUT. Appropriate MCU firmware

was to be written which enables the MCU to process the ADC data as well as to administer the various other system level operations required to perform the sequential frequency-shift measurement procedure. Additionally, this electronic assembly was to support digital communication to/from a local PC, from which a user can initiate the frequency-measurement process and view the frequency-shift measurement results. Finally, a PC software application was to be developed to realize the user interface.

The VCO assembly was developed by a fellow graduate student. A pictorial diagram of the VCO assembly is shown in Fig. 1.

The primary intended use for this frequency-shift measurement system pertains to chemical detection applications. However, this system could potentially also be used as a frequency-shift measurement system for DNA detection applications.

Note that incorporation of a PC within the proposed measurement system solution was done primarily out of convenience and to reduce the total system development time. It is worthwhile to mention that a truly 'stand-alone' system which does not require connection to a PC could easily be achieved by integrating the PC software functionality into the MCU firmware. One or more hardware push-button controls could be included within the system assembly to allow for initiation of the frequency shift measurement process, while a liquid crystal display (LCD) could be included within the system assembly to display the measurement results.

Note about terminology: Note that the assembly containing the VCO and SRR sensor will hereafter be referred to as the *VCO Board* while the remaining components of the frequency-shift measurement system will be referred to as the *PLL Board*.

3. Concerning Usage of the Frequency Shift Measurement System for DNA Detection Applications

As was suggested previously, it is likely that this frequency shift measurement system could potentially be used for other similar applications such as DNA detection. Such DNA detection devices have applications in the health industry for diagnosis of various genetic dispositions such as Alzheimer's disease, Parkinson's Disease, etc. A relatively portable, low-cost device which is able to perform such DNA detection with reasonable accuracy could allow for easy, comparatively rapid, and convenient testing in point-of-care clinics which serve the general public. In fact, originally the objective of this research was to develop such a system for DNA detection. In this respect, this research project was intended to progress in tandem with the research of one or more other individuals who were attempting to achieve a reliable method for performing DNA hybridization, so that this detection system could be tested and characterized. However, due to problems encountered with attempts to achieve successful DNA hybridization, along with time constraints for completion of this thesis research, the primary application for which this frequency measurement system was developed had to be changed to chemical detection.

C. Organization

This thesis documents efforts to successfully develop and test the proposed PLL-based chemical detection system with ADC, MCU, and off-board microwave resonator VCO, as described in the above proposal. The remainder of this thesis is comprised of the following chapters:

Chapter II discusses the frequency shift measurement system's theory of design. Emphasis is placed on derivation of the desired PLL characteristics and parameters,

as well as modeling and computer-aided simulation of the PLL. Issues pertaining to the expected precision of the system's frequency shift measurement capabilities are also considered. These issues include various noise sources within the system, and the potential benefits of digital oversampling of the control voltage.

Chapter III describes the physical implementation of the frequency shift measurement system on a printed wire assembly (PWA). (Note that a PWA is merely an assembled PCB assembly.) This section includes a detailed schematic diagram of the system assembly, discussion of the commercially available devices which are contained within the discrete electronic system assembly, discussion of various physical design issues such as PCB layout and routing, as well as the PCB layout diagrams, etc. This chapter also includes discussion of various additional relevant system-level topics such as usage and configuration of the ADC for digital measurement of the PLL control voltage, additional system level functionality, MCU firmware, PC Software, etc.

Chapter IV documents the experimental performance of the constructed frequency-shift measurement system PWA. This includes experimentally measured PLL performance as well as the system's frequency shift measurement capabilities (e.g., range, precision, sensitivity, etc.).

Chapter V documents the results of efforts to use the frequency-shift measurement system for chemical detection. Several common chemical substances were applied to the resonator substrate contained within the VCO assembly to determine the level of reliability and accuracy to which this system can measure the frequency shifts exhibited by the VCO, upon application of the various chemical substance. The quantitative results of those tests are presented and discussed. Additionally, note that homogeneous mixtures consisting of paired combinations of these chemical substances (in varying percentage of concentration) were formulated, and then the frequency shifts caused by application of the various mixture concentrations were

measured, to determine the system's capability to reliably and accurately quantify the relative concentrations of the constituent chemical substances within each mixture. These results are presented and discussed. Additionally, some efforts were made to measure the change in the power of the VCO output signal, in attempt to identify the complex permittivity of the various chemical substances. While this last measurement effort lies beyond the primary objective of this research, the results of these efforts are briefly discussed as well.

Chapter VI provides conclusions obtained from this research effort, as well as contemplation of how the research effort could have been improved (if it could be done all over again). Finally, some brief commentary about on-going research efforts and/or future research efforts related to this research project is provided.

CHAPTER II

SYSTEM THEORY AND DESIGN OF PLL BOARD

A. Introduction

This chapter provides a detailed description of the frequency-shift measurement system's theory of operation. It also contains a discussion of the PLL design considerations. The design parameters of the PLL were primarily determined from the included analysis of the system's theoretical accuracy and expected sources of error.

B. Theory of Operation

A more technical version of the frequency shift measurement system diagram presented earlier in Fig. 6 is shown in Fig. 7. To reiterate, the system consists of a PLL-based frequency synthesizer core, along with an analog-to-digital converter (ADC) and a microcontroller (MCU). The ADC is used to digitally sample the loop filter output or equivalently, the control voltage (V_{ctrl}) fed to the VCO. The MCU administers the frequency shift measurement process and provides a digital communication interface between the measurement system and an externally connected PC (not shown). It is also worth reiterating that the *VCO Board* assembly consists of the VCO block and the SRR sensor, while the *PLL Board* assembly contains all remaining circuitry represented in Fig. 7.

The system measures the amount of frequency shift exhibited by the VCO due to introduction of the MUT onto the SRR sensor. The frequency shift measurement is accomplished by digitally recording the control voltage fed to the VCO input both *before* and *after* introduction of the MUT.

Hypothetically, if the MUT was placed onto the VCO with the loop open, the

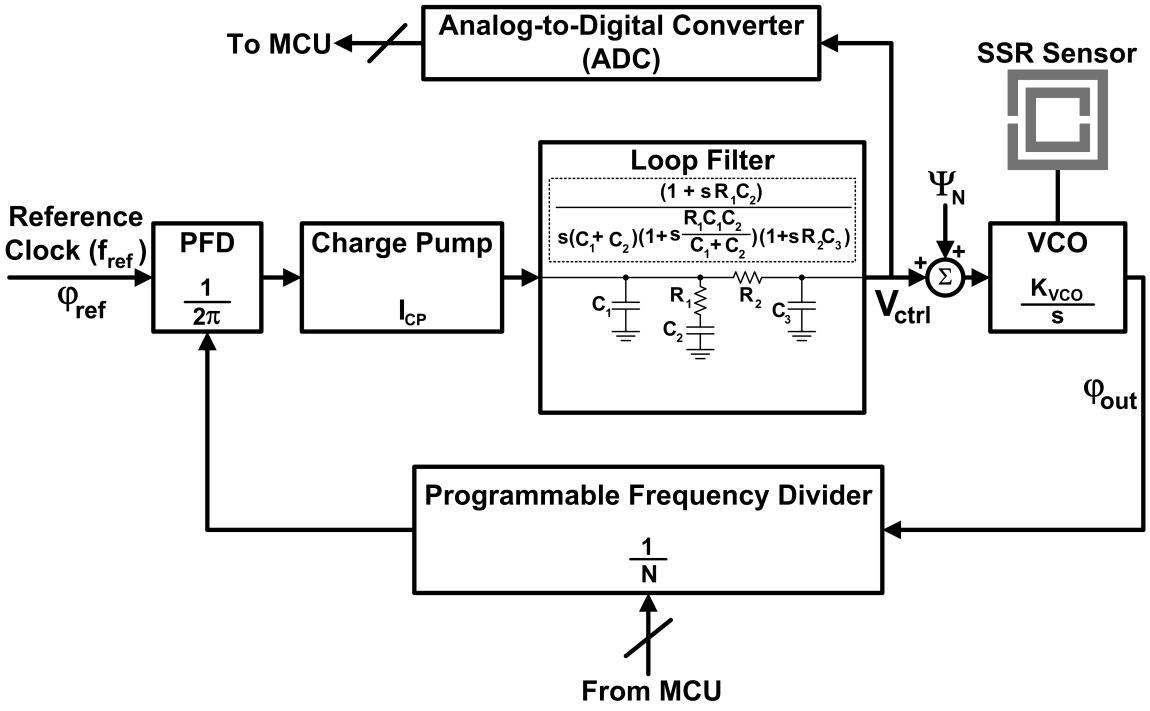


Fig. 7. Linear phase model of frequency-shift measurement system.

VCO output frequency would exhibit a negative shift in proportion to the MUT's dielectric constant. However because the VCO is contained within a PLL, note that as the MUT is introduced onto the sensor, the PLL will dynamically adjust V_{ctrl} such that a lock state is maintained with respect to the input reference clock (f_{ref}). That is, the PLL will force the VCO output frequency to remain constant. After introduction of the MUT, the MCU+firmware is commanded to incrementally adjust the programmable frequency divider value (N) until V_{ctrl} is returned to the level that was recorded prior to introduction of the MUT. This achieves an indirect measurement of the frequency shift which *would* be exhibited by the VCO if it was operating in an open-loop configuration.

The sequence of the frequency shift measurement procedure is illustrated graphically in Fig. 8(a). Fig. 8(b) provides a tabulature form of the procedure. The

measurement procedure consists of three fundamental phases, which are described in the following:

1. Initialization

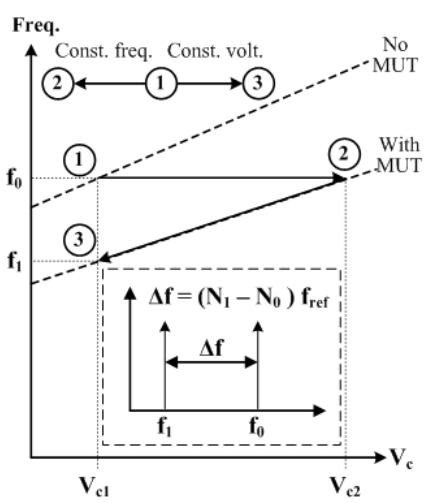
The programmable frequency divider is initially set to a value, N_0 so that the frequency synthesizer is locked to a frequency $f_0 = 4.48$ GHz with no MUT applied. The MCU digitally records the control voltage level at this time which is denoted as V_{ctrl1}.

2. Detection

A known volume of MUT is dispensed into the sample well of the VCO. Although the oscillation frequency of the VCO initially decreases, the PLL will dynamically adjust the control voltage in attempt to maintain the lock state at frequency f_0. By increasing the control voltage to the oscillator from V_{c1} to V_{c2}, the PLL eventually returns to the locked state and maintains the output frequency at f_0. The voltage V_{c2} is then digitally sampled and stored in the MCU.

3. Calculation

Using a binary search algorithm, the MCU digitally alters the frequency division value from N_0 to N_1 so that the oscillator control voltage returns from a value V_{c2} to its original value, V_{c1}. As a result, the output frequency of the synthesizer system changes from f_0 to f_1. The oscillation frequency shift, Δf, caused by the MUT is then computed as $\Delta f = f_0 - f_1 = (N_1 - N_0) \cdot f_{ref}$.



(a)

Phase	1 - Initialization	2 - Detection	3 - Calculation
Process	Start → Initialize divider value ($N_1 = f_0/f_{ref}$) → Digitally store initial control voltage (V_{c1}) → End	Start → Apply MUT to the sensing VCO → Digitally store control voltage in the presence of MUT (V_{c2}) → End	Start → Change divider value from N_1 to N_2 so that control voltage returns from V_{c2} to V_{c1} → Calculate the frequency shift as $\Delta f = (N_2\text{-}N_1)\, f_{ref}$ → End
Divider value	N_0	N_0	N_1
Control voltage	V_{c1}	V_{c2}	V_{c1}
Output frequency	f_0	f_0	f_1

(b)

Fig. 8. (a) Graphical illustration, and (b) detailed description, of the frequency shift measurement procedure.

C. PLL Design

1. Design Approach

While it would ultimately be desirable to develop a monolithic integrated solution for the proposed frequency shift measurement system, the objective of this research project was to realize the system as a discrete electronic assembly. Because of this, the emphasis was not focused on the transistor-level design of the circuitry. For this discrete solution, the strategy was to identify commercially available devices and components which could be employed to achieve the desired functionality. This approach allowed for realization of a functional system in a relatively short period of time, in comparison to the time that would be required to design a completely integrated solution 'from scratch' (at the transistor level) and then to fabricate the integrated solution.

2. PLL Device Selection

While the microwave resonator sensor-based VCO is the most critical and novel component of this measurement system, the next most critical aspect of this system is the PLL functionality. At present, only a few commercially available integrated PLL devices exist which are capable of supporting the intended frequency synthesizer solution. This is primarily due to the relatively high operating frequency range at which the frequency synthesizer must be able to operate. This output frequency requirement is dictated by the output frequency range that can be generated by the VCO Board, which is in the range of $\sim$4.4 GHz to $\sim$4.8 GHz.

After considering several possible devices, the ADF4157 High Resolution 6 GHz Fractional-N Frequency Synthesizer device manufactured by Analog Devices was selected for use in this system. A block diagram of this device is shown in Fig. 9. While

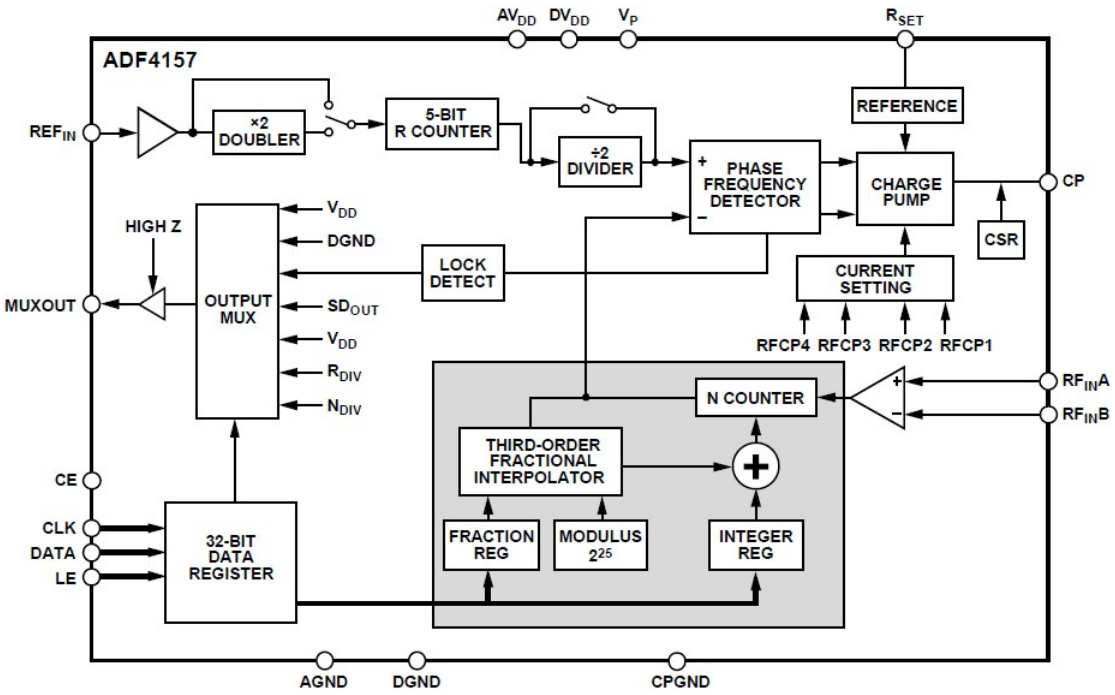


Fig. 9. Functional block diagram of ADF4157 device[17].

certain details concerning this device will be discussed further in later sections of this document, for the time being it is sufficient to mention several key features of this device, which made it a very attractive solution for this application.

Referring again to Fig. 7, note that the ADF4157 is capable of realizing the programmable frequency divider, phase-frequency detector (PFD), and charge pump functional blocks. The programmable frequency divider within the AD4157 is a *fractional-N* divider, which means that the high-frequency output signal provided from the VCO Board can be divided by a fractional divider value, as opposed to being restricted to division by integer values only. The ADF4157 supports an extremely high resolution (25 bits) of fractional division. In consideration of how this system is to achieve the frequency shift measurement (as just described in Section B), this fractional division feature is desirable because it allows for a very high precision of frequency shift measurement. Assuming that the PLL reference clock frequency is

14.8 MHz, the ADF4157 can provide a frequency resolution of $\frac{f_{ref}}{2^{25}} = \sim 0.441 Hz$.

The ADF4157 achieves the fractional-N frequency division functionality by means of a Σ-Δ modulator scheme. Because the order of the Σ-Δ modulator was configured as a second-order modulator, the ADF4157 Data Sheet recommends that the loop filter should be at least of third-order to assist in the noise-shaping of the Σ-Δ spectrum[17]. The circuit topology of the loop filter is shown schematically in Fig. 7.

3. PLL Performance Considerations

A listing of the critical PLL parameter values which were implemented for the PLL is provided in Table I. Note that the experimentally measured K_{VCO} value was determined by the VCO Board characteristics and could not be changed. An explanation of how the remaining PLL parameters were determined is provided in the following discussion.

When designing a PLL-based frequency synthesizer, emphasis is typically placed on the quality of the VCO output, as this is usually the critical output signal. However for this application, it is the behavior of the control voltage that is most critical because this is the signal that is to be monitored, to achieve the frequency shift measurement. Design of this PLL was therefore based on the desired behavior of the V_{ctrl} signal. In particular, a priority was placed on minimizing the noise at the V_{ctrl} node, in effort to achieve the highest possible frequency shift measurement sensitivity.

For this chemical detection application, the chemical sensing process is relatively slow (on the order of milliseconds). Therefore the transient behavior of the PLL is not very important, insofar as the measurement system's performance requirements are concerned. The settling time requirements for this PLL can be very relaxed. It is therefore acceptable for the PLL to have a relatively low loop bandwidth, if desired.

The PLL reference clock frequency was nominally set to be 16.0000 MHz. Obser-

Table I. Design parameters for the phase-locked loop.

Output frequency	4.48 GHz (nominal)
Ref. frequency	14.86453 MHz
Freq. division ratio (N_1)	301 (nominal)
Loop bandwidth	23 kHz
Charge pump current (I_{CP})	5 mA
Settling time (to $< 1°$)	395 μs
Phase Margin	55 °
R_1	185 Ω
R_2	718 Ω
C_1	7.3 nF
C_2	185 nF
C_3	1.8 nF
K_v	60 MHz/V

vation of Gardner's Stability Criterion [18] mandates that the loop bandwidth should therefore be no greater than 1.6 MHz.

In general, note that with respect to a PLL's loop bandwidth, there exists a trade-off between the extent to which reference clock phase noise is attenuated versus the extent to which phase noise originating from the VCO is attenuated. Referring to Fig. 7, the VCO phase noise is modeled as a noise voltage source, Ψ_N, presented as an input to the VCO. This noise voltage is added to V_{ctrl} to comprise the composite input control voltage fed to the VCO. The transfer function relating the VCO output, $V_{ctrl}(s)$, to $\Psi_N(s)$ is denoted as the *VCO noise transfer function*. As will be shown mathematically just below, the gain magnitude of this transfer function has a high-pass or bandpass characteristic with cutoff frequency approximately equal to the loop bandwidth. In contrast, while the gain magnitude of the noise transfer function relating $V_{ctrl}(s)$ to noise from the reference clock (call this $\varphi_N(s)$) has a low-pass characteristic with cutoff frequency equal to the loop bandwidth [19]. Therefore, a general rule for PLL design is to select a relatively low bandwidth to achieve significant attenuation of phase noise originating from the reference clock, and conversely to select a relatively high loop bandwidth to achieve significant attenuation of phase noise originating from the VCO [20].

For this application, the magnitude of phase noise energy originating from the VCO is expected to be significantly greater than the phase noise energy originating from the reference clock source as well as from any of the other blocks within the PLL. The amount of phase noise originating from the reference clock will be relatively low because the reference clock is sourced by either a very stable crystal-based canned oscillator circuit or alternatively from a laboratory signal generator (see Chapter III). Based on the facts discussed just above, selection of a relatively high loop bandwidth would be appropriate for typical PLL-based frequency synthesizer applications, as

this would further reduce phase noise at the VCO output (or equivalently, timing jitter) which is caused by VCO phase noise, as opposed to emphasizing the reduction of phase noise at the VCO output caused by reference clock phase noise.

However as mentioned previously, for this application priority was placed on minimization of voltage noise in the V_{ctrl} signal, as opposed to minimization of phase noise at the VCO output. With respect to their noise contributions at the V_{ctrl} node, the same bandwidth trade-off exists between VCO phase noise and reference clock phase noise, except that the bandwidth characteristics are reversed with respect to the phenomenon described just above. In this case a lower bandwidth will achieve further attenuation of noise at V_{ctrl} caused by VCO phase noise, while a higher loop bandwidth will achieve further attenuation of noise at V_{ctrl} caused by reference clock phase noise. The noise transfer functions for both of these noise sources with respect to the V_{ctrl} node can be computed using the s-domain parameters displayed in Fig. 7. The expression for the VCO noise transfer function to V_{ctrl} is defined to be $\frac{V_{ctrl}(s)}{\Psi_N(s)}$, and can be expressed as:

$$\frac{-(sK_vI_{CP}R_1C_2 + K_vI_{CP})}{s^4NR_1R_2C_1C_2C_3 + s^3N[C_{tot}R_2C_3 + R_1C_1C_2] + s^2NC_{tot} + sK_vI_{CP}R_1C_2 + K_vI_{CP}} \tag{2.1}$$

In the above equation, note that $C_{tot} = C_1 + C_2$.

A bode plot of this transfer function is shown in Fig. 10. It can be seen that this transfer function exhibits a low-pass characteristic with cutoff frequency approximately equal to the loop bandwidth, which is ∼23 kHz when the PLL loop parameters listed in Table I are plugged into the equation. Meanwhile the transfer function relating the reference clock noise to V_{ctrl} is defined as $\frac{V_{ctrl}(s)}{\varphi_N(s)}$. An expression for this transfer function using the given s-domain loop parameters is:

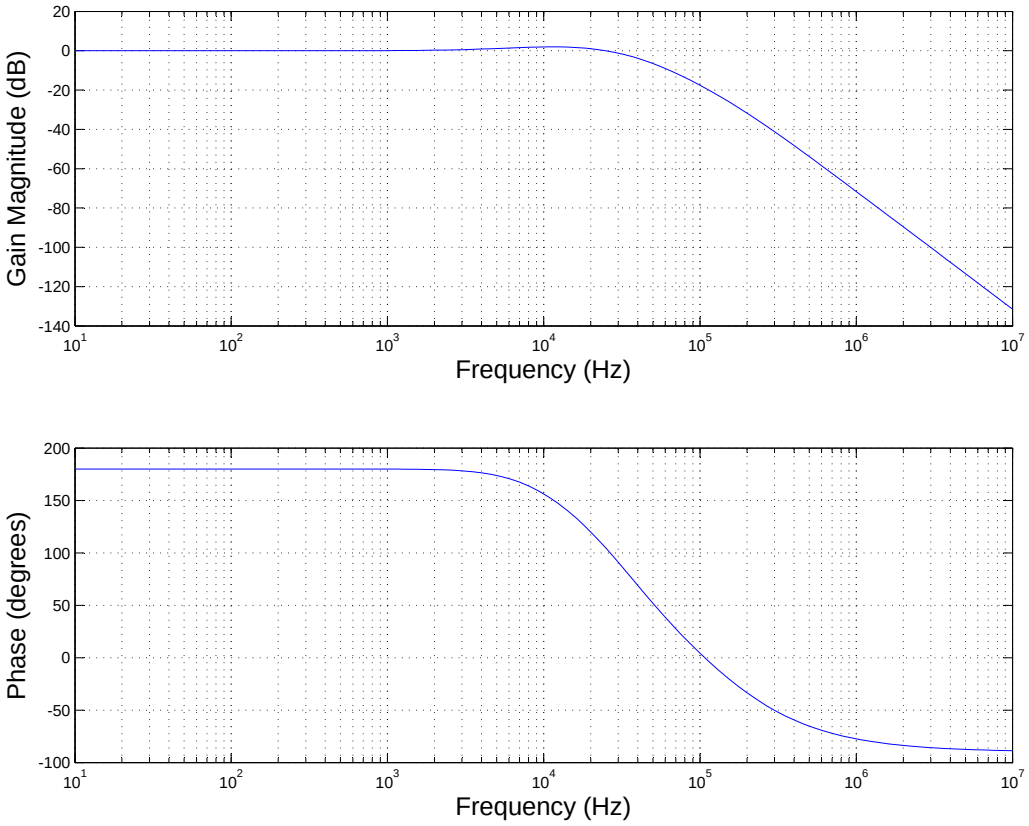


Fig. 10. Bode plot of VCO noise transfer function translated to V_{ctrl} node.

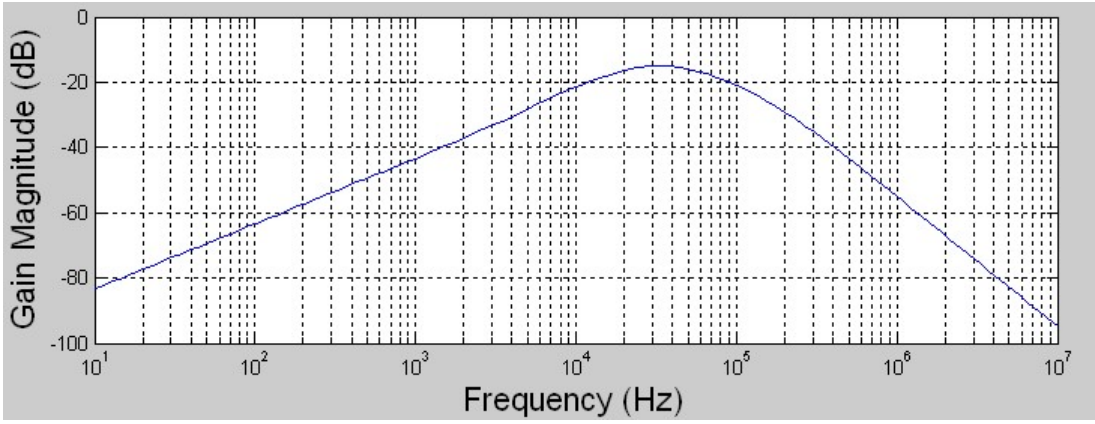


Fig. 11. Bode plot of transfer function relating PLL reference clock phase noise translated to V_{ctrl} node.

$$\frac{(\frac{1}{2\pi}) \cdot (s^2 N I_{CP} R_1 C_2 + s N I_{CP})}{s^4 N R_1 R_2 C_1 C_2 C_3 + s^3 N [C_{tot} R_2 C_3 + R_1 C_1 C_2] + s^2 N C_{tot} + s K_v I_{CP} R_1 C_2 + K_v I_{CP}} \tag{2.2}$$

In the above equation, note that $C_{tot} = C_1 + C_2$.

A bode plot of this transfer function is shown in Fig. 11. It can be seen that this transfer function exhibits a bandpass characteristic, with lower cutoff frequency approximately equal to the PLL loop bandwidth.

Based on the above analysis then, the PLL loop bandwidth was selected with the intent of prioritizing suppression of the VCO phase noise at the V_{ctrl} node. Based on the above theoretical analysis, this design priority warrants implementation of a minimal PLL loop bandwidth. However there do exist practical limitations regarding the extent to which the loop bandwidth can be minimized. First, realization of an excessively low PLL bandwidth would require usage of excessively large loop filter capacitor and/or resistor values. Additionally, the settling time of the PLL increases as the loop bandwidth is decreased. Because the calculation step of the frequency shift measurement process (as described in Section B) must only be performed after

the PLL has re-attained a stable lock state, implementation of an excessively low loop bandwidth would therefore require an unacceptable amount of time for the frequency shift measurement algorithm to complete.

Ultimately a loop bandwidth of 23 kHz was selected, although it could be argued that selection of an even smaller bandwidth would be justified. The idea here would be to switch back and forth between two different loop bandwidth settings during different phases of the frequency measurement process. The loop bandwidth could be set to a moderately low frequency (i.e., $\sim$23 kHz) during those times in which the PLL is in the process of re-acquiring a lock state. Since the frequency shift measurement procedure requires that the V_{ctrl} signal should be measured only under steady state conditions, it would theoretically be reasonable to decrease the loop bandwidth even further during those time periods in which V_{ctrl} is actually being digitally sampled (i.e., when the PLL has re-acquired a lock state). The PLL would then achieve an even greater degree of averaging or 'smoothing' of the V_{ctrl} signal.

Numeric values for the passive loop filter components were obtained using the ADIsimPLL software available from Analog Devices, Inc. By providing parameters for several known key PLL parameters including K_{VCO}, the charge pump current value (selected to be 5 mA), the desired phase margin (55 °), and the desired bandwidth (23 kHz), the ADIsimPLL software calculated an appropriate set of R and C component values for the loop filter. These filter component values are listed in Table I.

Fig. 12 is a screenshot of frequency-domain simulation results that were generated by the ADIsimPLL software.

Fig. 13 is a screenshot of time-domain simulation results that were generated by the ADIsimPLL software.

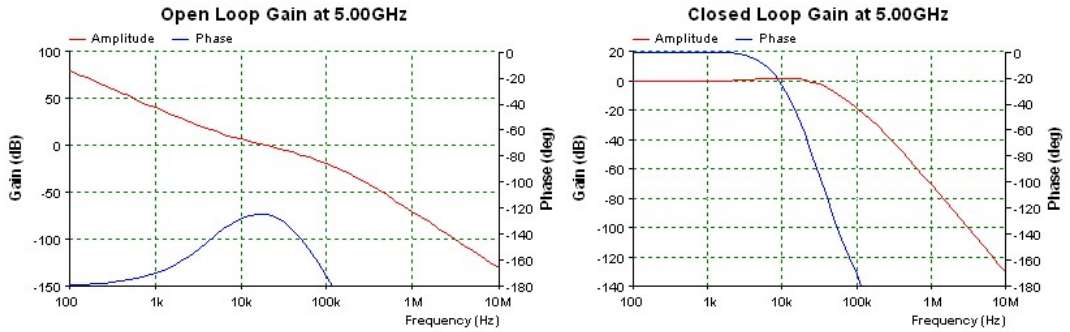


Fig. 12. Bode plot of open and closed loop PLL transfer functions.

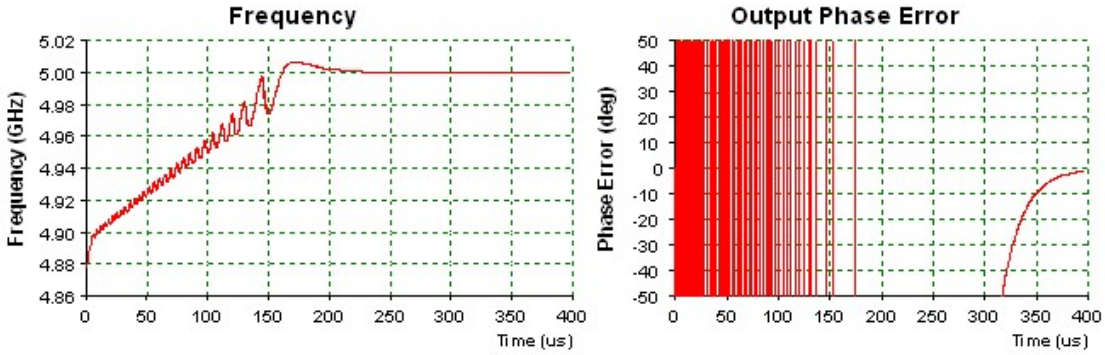


Fig. 13. Time domain plots illustrating transient behavior of frequency and phase error in response to frequency step.

CHAPTER III

HARDWARE IMPLEMENTATION OF PLL BOARD ASSEMBLY

A. Introduction

This chapter contains a detailed description of the PLL Board printed wire assembly (PWA). The PWA is comprised of the PCB as well as the various commercially available components which are populated on the PCB. Detailed technical documentation of the PWA is provided, including a circuit-level schematic diagram, diagrams of the critical PCB layers, and a bill of materials (BOM). This chapter also includes discussion of various relevant design issues which were considered during the development of this PWA.

B. PLL Board Development Procedure

The major steps taken to develop this system assembly include:

- Conceptualization
  - ◇ Define desired system functionality
  - ◇ Identify system-level components
- Component Selection
- Compose Schematic
  - ◇ Create component models
  - ◇ Realize required component connectivity
- Compose Layout
  - ◇ Create footprints
  - ◇ Component placement
  - ◇ Trace routing

- PCB Fabrication
- Procurement of Parts
- Board Assembly
- Board Test/Verification

C. PLL Board Functional Requirements

At this point it is worthwhile to recall the required functionality that was to be achieved by the PLL Board, as described in Chapter I. To serve as a guide to the PLL Board design, those requirements were expanded to the following more detailed listing of functional requirements:

- The PLL Board is to provide the phase-comparator, charge pump, reference clock, and frequency divider blocks of the PLL.
- The PLL Board is to provide an ADC to monitor the loop filter output (i.e., the VCO control voltage).
- The PLL Board is to include an MCU which will:
  - administer system level control of the PLL Board assembly.
  - collect the digitized VCO control voltage data (from ADC) both before and after the MUT is deposited onto the SRR.
  - upon introduction of the MUT onto the SRR, force the digitized VCO control voltage level back to the level at which it had been prior to introduction of the MUT, by performing an iterative incremental adjustment the PLL loop divider value (N).
  - provide a PC interface to allow transfer of ADC data to PC, and to possibly provide PC-based control of the PLL Board assembly.

Several additional features were ultimately included within the PLL Board. All of these various features will be described in later sections of this chapter.

D. System-Level Description of PLL Board

A block diagram of the PLL Board is shown in Fig. 14. Referring to this diagram, it can be seen that the output signal from the VCO Board is to be provided as the RF input. The RF input will be an oscillating signal in the frequency range of approximately 4.4 GHz to 4.7 GHz. This RF input is directed to a integrated PLL device manufactured by Analog Devices. Note that in reference to Fig. 7, this device contains the frequency divider block, the phase-frequency detector (PFD), and charge pump blocks of the PLL. The charge pump output from this device is then directed to the passive loop filter. The output from the passive loop filter constitutes the VCO control voltage (V_{ctrl}) which is provided as an off-board output to be connected to the control voltage input terminal of the VCO Board. This completes the phase-lock loop. Note that an on-board signal source is also included to provide the reference clock source to the PLL device. However, the reference clock source can alternatively be provided from an external signal source.

To allow for digital sampling of the V_{ctrl} voltage, note also that the V_{ctrl} voltage node is connected to the input of an active amplifier block. This amplifier functions as a unity-gain buffer, the purpose of which is to prevent this voltage tap from presenting any significant additional loading to the V_{ctrl} node. That is, connection of any additional resistive-inductive-capacitive load to the V_{ctrl} node must be minimized to avoid significant alteration of the intended loop filter characteristics, as well as alteration of the overall PLL performance characteristics.

The output from this voltage buffer is then passed to a voltage scaling block,

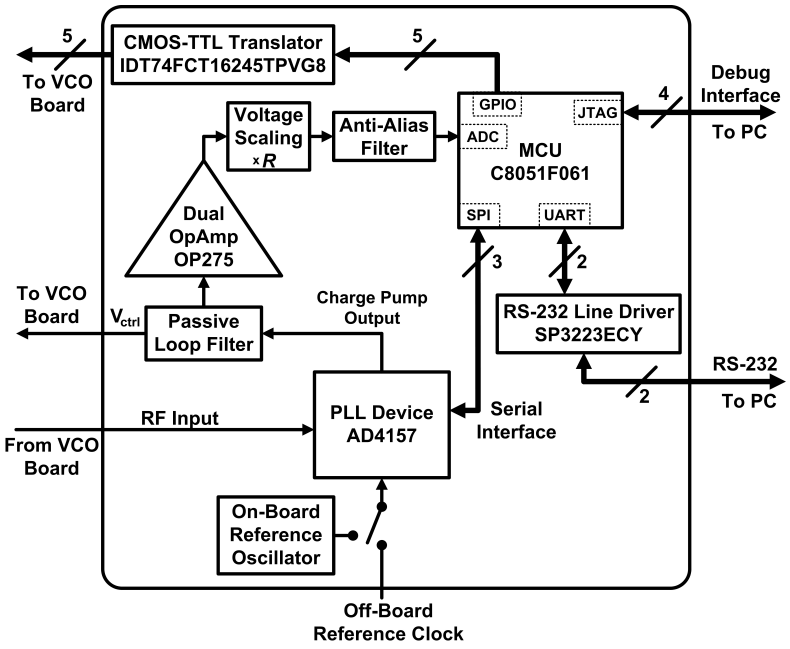


Fig. 14. Block-Level diagram of PLL Board.

with scaling factor of R=∼0.672. The voltage scaling block is necessary due to a difference in the maximum possible voltage level at V_{ctrl} which can be generated by the charge-pump V_{ctrl} (∼5V) and the ADC's maximum permissible input voltage level (∼3.3V). This buffered version of V_{ctrl} is therefore scaled to avoid clipping of the ADC input. The buffered version of V_{ctrl} is then passed through an anti-aliasing filter and finally connected to the input of the ADC. The anti-aliasing filter attenuates frequency content in the ADC input signal which exists beyond the Nyquist frequency, which is one-half of the ADC sampling frequency

Note also from Fig. 14 that a communication interface exists between the MCU and the PLL device. This allows the MCU to configure various aspects of the PLL device's operational mode.

The MCU also supports a separate two-wire UART interface which is connected to an RS-232 line-driver device. This provides an off-board communication interface

connection to/from a PC COM port, thereby affording a user with PC-based control of PLL Board operations as well as an ability to acquire the frequency-shift measurement data from the MCU.

In addition to the RS-232 interface described just above, a separate hardware interface on the PLL Board supports a second connection between the MCU and a PC. This second interface provides a means by which the firmware object code can be uploaded to the MCU, as well as a firmware debug interface. Note that this interface is not utilized for any aspect of the actual frequency shift measurement functionality.

Several general purpose I/O (GPIO) pins from the MCU are connected to a CMOS-to-TTL translator device. More information about this feature will be described in a later section.

In the next section, implementations of the various blocks shown in Fig. 14 are described in more detail.

E. Block-Level Description of PLL Board

1. PLL Device

It was necessary for the PLL device to provide a frequency divider for the RF input, as well as the phase comparator and charge pump functions of the PLL. Only a handful of commercially available PLL devices support input frequencies as high as 5GHz. Several of these devices were considered. Ultimately, the ADF4157 High Resolution Fractional-N Frequency Synthesizer device manufactured by Analog Devices was selected. A functional block diagram of this device is shown below in Fig. 15.

Along with a programmable integer-value frequency divider, the ADF4157 device provides a modulo-25 fractional-N divider as well. This allows the ADF4157 to achieve an extremely high resolution of frequency divider values. This feature is desirable

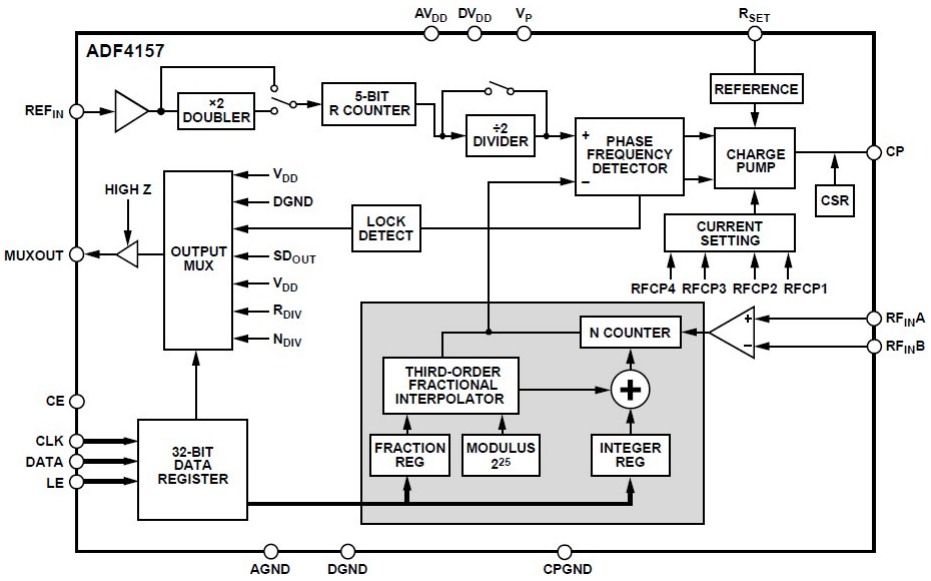


Fig. 15. Functional block diagram of ADF4157 PLL device[17].

because it provides the ability to characterize the voltage-to-frequency characteristic of the resonator circuit with much higher resolution. This will in turn allow for a more precise measurement of the frequency shift exhibited by the VCO, when the MUT is introduced onto the VCO's SRR sensor.

Primary power is provided to the ADF4157 through +3.3V (nominal) analog and digital power supply pins. However, Analog Devices stipulates that the analog and digital supplies should be equal. Note also that a separate pin is provided for the charge pump power supply. This allows the output voltage range of the charge pump circuit to vary over the somewhat larger (and more conventional) range of 0V - 5V. (Actually, the practical range is limited to approximately 0.2V - 4.8V.)

Configuration of the ADF4157 is achieved via a 3-pin serial peripheral interface (SPI). These pins are connected to three port I/O pins on the MCU. This allows the MCU to perform write operations to program the various control registers within the ADF4157.

2. PLL Reference Clock Source

As previously mentioned, the reference clock for the PLL can be provided from either of two sources. The PLL Board includes a footprint for a standard DIP-14 package canned oscillator. A CW53AF-16.000MHz canned oscillator manufactured by Cal Crystal, Inc.[1] was selected. This is a 16.00000 MHz oscillator which exhibits very low drift/variation in output frequency (15ppm/deg C), over a wide temperature range (-10 deg C to +70 deg C). It therefore can provide a very stable and robust reference clock source for the PLL. Alternatively, the clock source can be provided via connection of an external signal generator to an SMA connector on the PLL Board by disabling the oscillator or simply by de-populating the canned oscillator from the PLL Board.

3. PLL Loop Filter

The loop filter is implemented as a third-order passive filter with high-precision resistor and capacitor components. More details on the loop filter will be discussed in the circuit-level description of the PLL Board.

4. OpAmp Buffer, Voltage Scaling, and Anti-Aliasing Filter for ADC Input

The buffer amplifier circuit is realized using an OP275 dual low-noise opamp device. Both of the opamps are individually wired in a unity-gain inverting feedback configuration and then connected in cascade fashion, to achieve an effective gain of positive unity. The voltage scaling is realized as a simple resistor divider network. The anti-aliasing filter is implemented as a single-pole R-C Butterworth filter.

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[1] more information at www.calcrystal.com

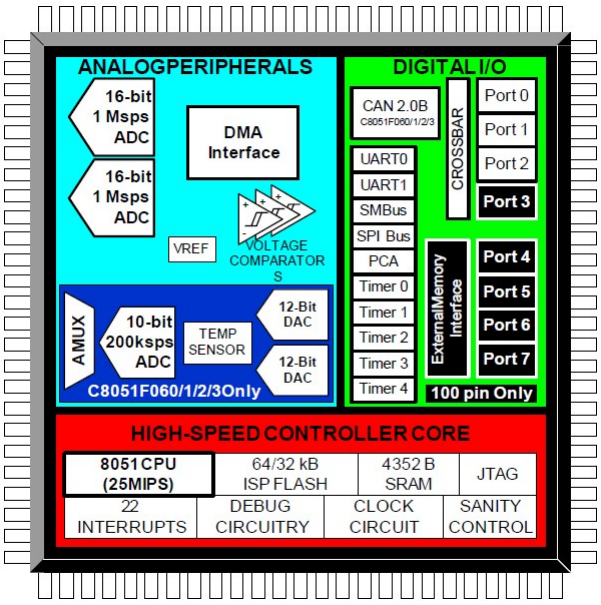

Fig. 16. Functional block diagram of C8051F061 MCU device[21].

5. MCU Device

The C8051F061 MCU manufactured by Silicon Labs, Inc. was selected as the on-board MCU. This is a pipelined 8051-core 8-bit microcontroller, with a 25 MHz system clock. A functional block diagram of this MCU is shown in Fig. 16[21].

Along with 64 KB of FLASH code memory and 4352 bytes of RAM, the C8051F061 MCU provides a host of useful on-chip peripherals, most of which are not utilized for this PLL Board application. For this application, one of the two available on-chip 16-bit 1 Msps ADCs are utilized, to monitor the V_{ctrl} signal that is fed back to the input of the VCO Board.

One of the MCU's two available on-chip UART peripherals is utilized to support the RS-232 communication between the PLL Board and a personal computer (PC). It is conceded that it would be preferable to support USB communication to/from a PC, since most modern PCs are no longer equipped with a DB9 connector for RS-

232 communication (i.e., a "COM" port) and MCUs which can support such USB communication certainly do exist. However, for the sake of reducing firmware development time, the significantly more simple UART protocol was selected, noting that more than one commercially available RS232-to-USB adapters can be purchased from multiple consumer electronics vendors. Therefore, RS-232 communication to/from a PC should be sufficient.

As mentioned earlier, several I/O pins on the MCU are configured to realize the 3-wire communication interface to the ADF4157 PLL device. The MCU functions as the 'master' device for such communication, while the ADF4157 is the 'slave' device. This allows the MCU firmware to write to the various configuration registers within the ADF4157, to control the device's operation.

The MCU supports several other minor PLL Board functions:

- Several MCU pins are connected to LEDs, which were included to indicate certain board status conditions.

- A push-button switch was included on the board, to allow for at least a basic hard-ware based user input. This push-button switch is connected to one of the MCU's general-purpose I/O pins, so that the firmware can sense actuation of this push-button by the user. It will therefore be possible for a user to toggle through one or more different modes of board operation.

The C8051F061 MCU provides a versatile debug interface. Firmware debug can be performed real-time. With the aid of the Silicon Labs IDE Software for PC[2] and by connecting the Silicon EC2 Adapter between a user PC and a 10-pin header included on the PLL Board, a variety of useful MCU debug operations can be performed. Some

[2]see www.silabs.com

of these debug features available are listed below.

- Firmware execution can be halted, and then resumed.
- Breakpoints can be inserted.
- View contents of various MCU control/data registers, data/program memory.
- Watch variables can be created.
- During halt of firmware execution, the states of all clocks and timers are suspended and remain intact upon resumption of firmware execution.

6. CMOS-to-TTL Translator

Referring again to Fig. 14, note that several of the MCU's I/O pins are also made available to the VCO Board, through an IDT74FCT164245T CMOS-to-TTL translator device (manufactured by Integrated Device Technologies). It is possible that future versions of the VCO Board might contain multiple resonator circuits on the same board assembly, during this exploratory phase of this on-going research effort. These logic signals are provided to support MUXing of such multiple resonator outputs to the primary RF output, so that only one of the resonators is connected to the primary RF output on this board, at any given time. This output is then connected to the single RF input of the PLL Board. A conceptual diagram which illustrates such a multiple sensor system is shown in Fig. 17.

Such a multiple sensor array can increase the accuracy of the frequency-shift measurement, through statistical averaging of the results from each individual sensor. Note that for this research effort, such a multiple sensor array was not utilized. However for this research, such improvement in measurement accuracy through statistical averaging *was* achieved by running multiple trials of each test (i.e., by applying

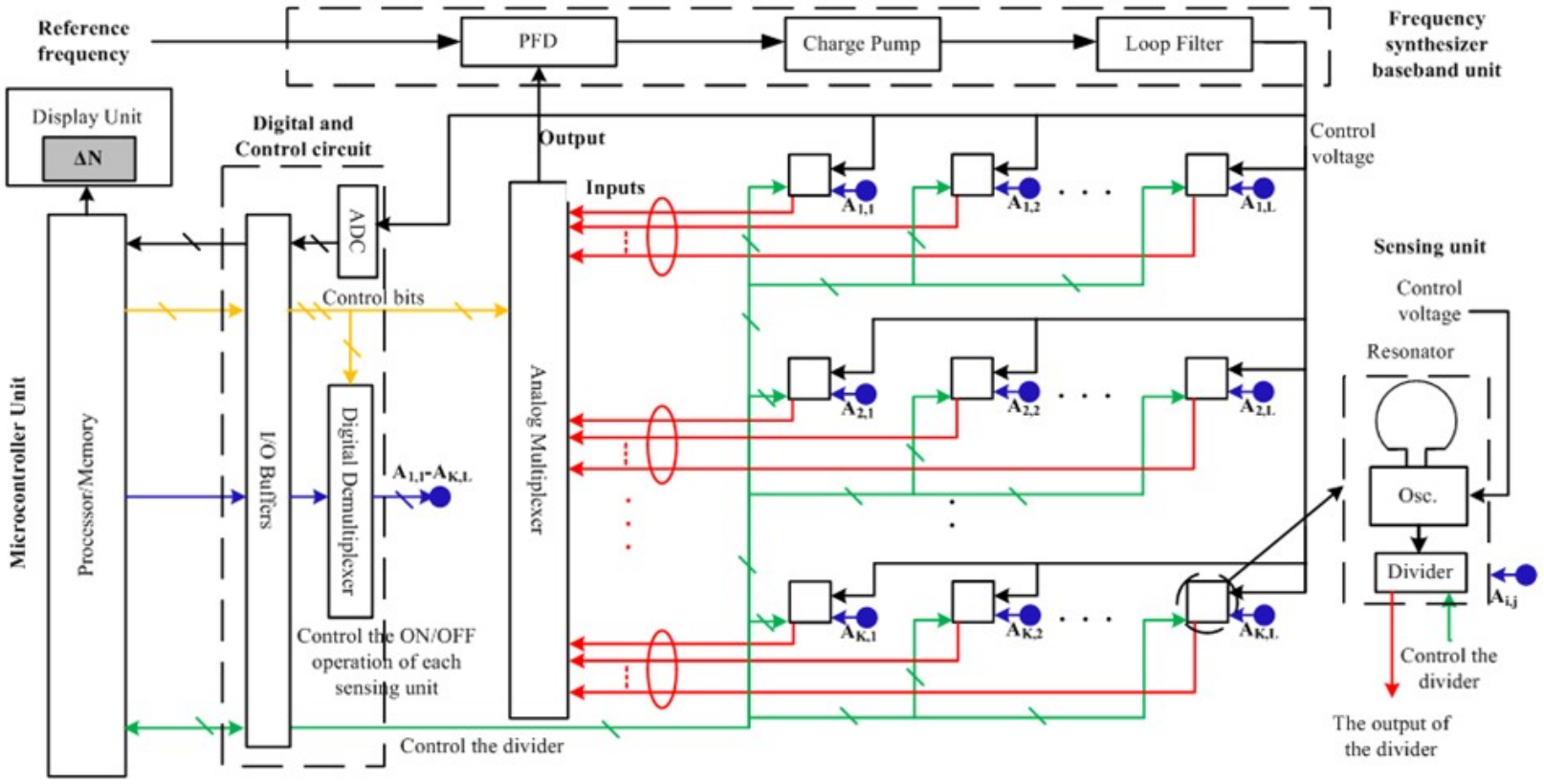

Fig. 17. Illustration of multiple SRR sensor array.

the same MUT to the single sensor VCO Board multiple times and averaging the frequency shift results from the multiple trials).

F. Circuit-Level Description of PLL Board

This section provides circuit-level descriptions of the various functional blocks discussed in the previous section. A complete schematic diagram of the actual PLL Board assembly is shown in Fig. 18. The schematic and layout were created using the DIPTRACE software[3].

1. Circuit-Level Description of PLL Device Connectivity

The off-board RF input is fed to the PLL Board through the J4 SMA connector, and is connected directly to the main $RF_{IN}A$ input pin of the ADC4157 device (U1). Note that this RF input will be DC coupled using an off-board DC clocking capacitor. Per advisement from the AD4157 Data Sheet, because the off-board RF input is a single-ended signal and not a differential signal, note that a 100pF DC blocking capacitor has been placed off of the unused $RF_{IN}B$ input pin.

Decoupling capacitors C32, C33, C9, C27, C10 and C28 are respectively connected to the analog, digital, and charge pump power supply pins of the ADC4157 device.

The charge pump current can be varied by adjusting the resistance value of the 30 kΩ potentiometer (VR1) connected to the RSET pin. This potentiometer was set to $\sim$5 kΩ.

The CLK, DATA, and LE pins have been connected to three of the MCU pins, to allow the MCU to administrate the 3-wire communication to/from the PLL device.

[3]More information at www.diptrace.com

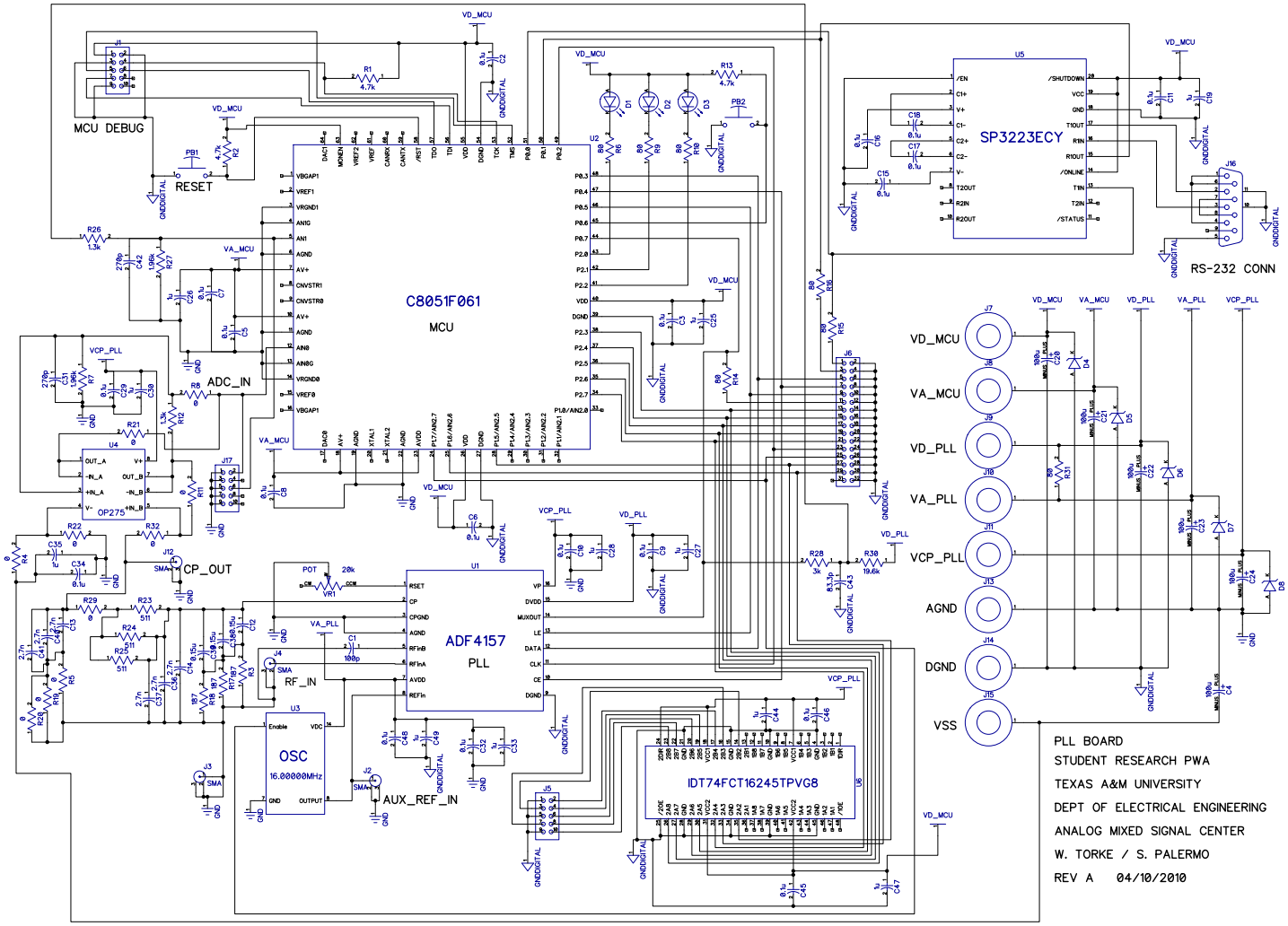

Fig. 18. Schematic diagram of PLL Board.

2. Circuit-Level Description of PLL Reference Clock Source Connectivity

As mentioned previously, the PLL reference clock (U3) is realized with a 16.00000 MHz canned oscillator device produced by CalCrystal. The output is connected to the REF_{IN} input pin of the PLL device (U1).

Note that pin 1 of the U3 oscillator is an ENABLE/DISABLE input, which is connected to one of the MCU's I/O pins. This enable/disable capability was included to allow connection of an alternate off-board reference clock source to the REF_{IN} input. For this reason, an additional SMA connector (J2) was provided so that a signal generator can be connected to the PLL Board, to provide this alternate reference clock. In such cases, the on-board reference oscillator can be disabled by the MCU firmware, or by manually connecting pin 27 of the J6 header to GND.

For the majority of testing performed using this PLL Board, the output from an external laboratory signal generator was connected to the J2 SMA connector to provide the reference clock signal, while the U3 footprint on the PLL Board was simply not populated.

3. Circuit-Level Description of PLL Loop Filter Connectivity

The passive PLL loop filter components consist of C12, C38, C39, R3, R17, R18, C14, C36, C37, R23, R24, R25, R29, R5, R19, R20, C13, C40, and C41.

Note that some redundancy is included for the various loop filter resistors and capacitors. To realize the pending loop filter characteristic, note that R17, R18, C38, C39, R24, R25, C40, and C41 are not populated. This redundancy of loop filter components was included for two reasons:

- The multiple parallel and series network configurations allow for realization of non-standard R and C values, using standard available R and C component

values. If there is a desire to achieve a very specific loop filter characteristic, more exact R and C filter values can be obtained by populating more than one of the parallel and/or series resistor and capacitor footprints.

- It is likely that during development, further optimization and/or refinement of the PLL loop filter will be performed. It is therefore likely that one or more of the R and C components will need to be removed and replaced with a different valued R/C. Repeated replacement of such components can eventually degrade and even destroy the PCB footprints for these components. Providing multiple footprints therefore provides extra solder pad locations in which various replacements can be soldered to the board, if one of the associate duplicate set of footprints is destroyed over time.

4. Circuit-Level Description of MCU Device Connectivity

The MCU device (U2) has multiple connections.

Capacitors C2, C3, C5, C7, and C8 are all 0.1uF decoupling capacitors placed near the multiple analog and digital supply pins of the MCU device. Additionally, two 1uF decoupling capacitors (C25 and C26) are respectively placed off of the digital and analog power supply pins, in the region of this device.

The PB1 RESET push-button switch and pull-up resistor R2 are provided to allow the user to initiate a hardware reset of the MCU.

The P0.1 and P0.2 I/O pins comprise the standard two-wire UART lines which are connected to U5, which is a SP322ECY RS232 driver device manufactured by the SIPEX corporation. This device creates the necessary +/-12 volt level signals to transmit serial data to/from the COM port of a connected PC, presumably by means of a capacitor-based charge pump circuit. The TX and RX output signals from U5

are directed to a standard DB-9 connector (J16), for connection to the user's PC. This allows for RS-232 communication between the PLL Board and a PC.

MCU general purpose I/O pins P2.3-P2.7, as well as P1.5 and P1.6 are connected to the IDT74FCT16245 voltage translator device (U6), to provide the MUX control signals to a (yet-to-be-fabricated) multiple sensor array VCO Board. They corresponding TTL-level outputs from U6 are connected to a 10-pin header, so that these MUX signals can be ported over to the resonator board via a 10-pin ribbon cable/connector.

Note that resistor R1 and the 10-pin header J1 comprise the debug interface connection to/from the user's PC. The 10-pin ribbon connector provided with the SiLabs EC2 adapter assembly can be connected to J1 and then also connected to an available USB port on the user PC, to achieve the MCU debug connection.

5. Circuit-Level Description of OpAmp Buffer, Voltage Scaling, and Anti-Aliasing Filter for ADC Input

The opamp is actually realized as the cascade of two OP275 Low-Noise Opamps manufactured by Analog Devices contained in the same package (U4). Both opamps are connected in a non-inverting unity-gain configuration. The +5V charge pump power supply is used to provide the positive power supply connection for these opamps. For the negative opamp supply, one of two options is possible. The negative power supply can be connected to GND if the R22 resistor option is populated, in which R4 should be de-populated. Alternatively, a VSS power connection was also included on the board, if a negative voltage power supply is to be used (such as -5V). In this case, the R4 resistor should be populated and R22 should be de-populated.

Decoupling capacitors C29, C30, C34, and C35 are attached to the positive and negative power supply pins of this opamp device.

The voltage scaling is achieved by means of the resistive divider combination of R12 and R7, to achieve a voltage scaling of ∼0.672. Additionally, R12 and C31 form the anti-aliasing filter for the primary ADC input. At present, the -3dB frequency of this filter is at ∼453 kHz, although the exact R and C values may eventually be modified in the future, to shift the 3 dB cutoff frequency. Note that the ADC can operate at up to 1 MHz.

Note that R8 and R11 are to be depopulated. These resistor options are provided if there is a desire to bypass the opamp and/or anti-aliasing filter.

6. Power Supplies and Other Connections

Power is provided through the various banana connectors (J7-J11 and J13-J15). A separate digital and analog supply are provided for both the PLL device and the MCU. Additionally, a separate connector is provided for the +5V charge pump power supply and for the optional negative power supply for the low-noise opamps. Note that separate analog and digital ground connections were included. It was decided that provision of separate analog and digital ground returns might allow for reduction of noise on the critical analog circuitry, which might otherwise by radiated from the various digital circuitry on the board.

The J6 header is included to provide the ability to probe various nodes on the PLL Board using a logic analyzer, spectrum analyzer, oscilloscope, or even a multimeter. For the same reasons, the J17 10 pin header provides a probe point for the primary and secondary loop filter output signals which are fed to the on-board ADCs.

7. PLL Board Bill of Materials (BOM)

A bill of materials for the PLL Board assembly is shown in Fig. 19.

#	RefDes	Description	Quantity	Value	Vender	Vender Part #	Manufacturer	Manufacturer Part #	Price
1	C1	cap ceramic 100pF X7R 0805 630V 10%	1	100p	Digi-Key	399-5571-1-ND	Kemet	C0805C101KBRACTU	0.519
2	C10, C11, C15, C16, C17, C18, C2, C29, C3, C32, C34, C45, C46, C48, C5, C6, C7, C8, C9	cap cer 0.1uF 50V 10% X7R 0805	19	0.1u	Digi-Key	490-1666-1-ND	Murata Electron	GRM21BR71H104KA01L	0.042
3	C12, C38, C39	cap ceramic 1.2uF X7R 1206 10% 10V	3	0.15u	Digi-Key	478-1558-1-ND	AVX Corporation	12065C272KAT2A	0.303
5	C14, C13, C36, C37, C40, C41	cap ceramic 2700pF X7R 1206 10% 50V	6	2.7n	Digi-Key	478-1535-1-ND	Yageo	12065C272KAT2A	0.303
6	C19, C25, C26, C27, C28, C30, C33, C35, C44, C47, C49	cap, ceramic, 1.0uF, 10%, 10V, 0805	11	1u	Digi-Key	490-1695-1-ND	Murata Electron	GRM21BR71A105KA01L	0.111
7	C20, C21, C22, C23, C24, C4	cap, 100uF, 20%, electrolytic, through-hole, radial, series EB	6	100u	Digi-Key	P13455-ND	Panasonic - ECG	EEU-EB1A101S	0.11
8	C31, C42	cap, 0.1uF, 20%, X2Y, ceramic, X7R, 0805	2	270p	Digi-Key		Yageo	CX0805MRX7R7BB104	
9	C43		1	83.3p					
10	D1, D2, D3	LED, red, surface mount	3		Digi-Key	P500CT-ND	Panasonic-SSG	LN1251CTR	0.33
11	D4, D5, D6, D7, D8	transient voltage suppression diode, 5.8V, DO-204AC package	5		Littlefuse	P6KE6.8-B	Littlefuse	P6KE6.8-B	
12	J1, J17, J5	header, 2x5, 100 mil spacing	3		Digi-Key	SAM1048-50-ND	Samtec Inc	TSW-150-08-T-D	4.19
13	J10, J11, J15, J7, J8, J9	Banana Connector, red	6		Digi-Key	7004K-ND	keyelco	7004	4.312
14	J12, J2, J3, J4	SMA connector	4		Digi-Key	J806-ND	Emerson Networ	142-0761-871	7.52
15	J13, J14	banana connector, black	2		Digi-Key	7005K-ND	keyelco	7005	4.312
16	J16	connector, DSUB, RS232, 9-pin, female, RSPT,	1		Digi-Key	A32107-ND	Tyco Electronics	5745781-6	3.9
17	J6	header, 2x16, 100 mil spacing	1		Digi-Key	SAM1048-50-ND	Samtec Inc	TSW-150-08-T-D	4.19
18	PB1, PB2	push-button switch, STDP, surface mount	2		Digi-Key	P12961STR-ND	Panasonic-ECG	EVQ-Q2Y03W	0.39
19	R1, R13	RES, 4.7kOhm, 0.25W, 5%, 1206	2	4.7k	Digi-Key	RHM4.7KECT-ND	Rohm Semicond	MCR18EZHJ472	0.102
20	R10, R14, R15, R16, R31, R6, R9	RES, 1.3kOhm, 0.25W, 5%, 1206	7	80	Digi-Key	P80.6FCT-ND	Panasonic-ECG	ERJ-8ENF80R6V	0.117
21	R11, R19, R20, R21, R32, R5, R8	P0.0.ECT-ND	7	0	Digi-Key	P0.0.ECT-ND	Panasonic-ECG	ERJ-8GEY0R00V	0.94
22	R12, R26	RES, 1.3kOhm, 0.25W, 5%, 1206	2	1.3k	Digi-Key	P1.30KFCT-ND	Panasonic-ECG	ERJ-8ENF1301V	0.094
24	R17, R18, R3	RES, 187Ohm, 1%, 0.25W, 1206	3	187	Digi-Key	RHM187FCT-ND	Rohm Semicond	MCR18EZHF1870	0.052
25	R2	RES, 4.7kOhm, 0.125W, 5%, 0805	1	4.7k	Digi-Key	P4.7KACT-ND	Panasonic-ECG	ERJ-6GEYJ472V	0.077
26	R22, R29, R4	RES, 0.0 Ohm, 0.5W, 5%, 1210	3	0	Digi-Key	541-0.0VCT-ND	Vishay-Dale	CRCW12100000Z0EA	0.261
27	R23, R24, R25	RES, 511 Ohm, 0.5W, 1%, 1210	3	511	Digi-Key	541-511AACT-ND	CRCW	CRCW1210511RFKEA	0.289
28	R27, R7	RES, 1.3kOhm, 0.25W, 5%, 1206	2	1.96k	Digi-Key	P1.96KFCT-ND	Panasonic-ECG	ERJ-8ENF1961V	0.117
29	R28	RES, 3.00kOhm, 0.25W, 1%, 1206	1	3k	Digi-Key	541-3.00KFCT-ND	Vishay-Dale	CRCW12063K00FKEA	0.102
30	R30	RES, 19.6kOhms, 0.25W, 1%, 1206	1	19.6k	Digi-Key	541-3.00KFCT-ND	Vishay-Dale	CRCW12063K00FKEA	0.102
31	U1	IC, PLL device	1		Digi-Key	ADF4157BRUZ-ND	Analog Devices	ADF4157BRUZ	
32	U2	IC, MCU, 8-bit	1		Mouser	C8051F061	Silicon Labs	C8051F061	
33	U3	oscillator, 16.00000 MHz, metal can	1		Cal Crystal	CT53AF	Cal Crystal	CT53AF	
34	U4	IC, dual opamp, low-noise	1		Digi-Key	OP275GSZ-ND	ADI	OP275GSZ	2.25
35	U5	IC, RS-232 driver	1		Exar	SP3223ECY-L	SIPEX Corporatio	SP3223ECY	
36	U6	Translator_CMOS_TTL_16ch	1		Digi-Key	800-1606-1-ND	IDT	IDT74FCT16245TPVG8	4.41
37	VR1	potentiometer, 20k	1		Digi-Key	490-2039-1-ND	Murata Electron	PVZ2A303A01R00	0.152

Fig. 19. PLL Board bill of materials.

G. PCB Layout

Like the schematic, the PCB layout was created using the DIPTRACE software. The PCB has two copper trace layers (top-side and bottom-side). It was fabricated on FR4 substrate of 0.062 inch thickness. A diagram showing the top and bottom signal traces is provided in Fig. 20. The top layer signal traces are colored black while the bottom layer signal traces are colored gray.

Note that the widths of the primary RF input trace from the J4 SMA connector as well as the alternate reference clock input from the J3 SMA connector were intentionally increased, to achieve an appropriate impedance matching of approximately 50 ohms.

A plot of the top copper and silkscreen layers is shown in Fig. 21, this time with the copper fill included. Note that the copper fill on the left-hand side of the board consists of the analog ground plane while the copper fill on the right-hand side of the board consists of digital ground plane.

A rather uninteresting plot of the bottom copper layer is shown in Fig. 22, this time with the copper fill included.

A photograph of the assembled PLL Board is shown in Fig. 23.

H. MCU Firmware and PC Software

The firmware developed for the MCU was designed to accept various commands from a PC Software application. This allows a user to initiate execution of the various relevant operations. These include various configuration operations pertaining to configuration of the ADF4157 device. Recalling the proposed frequency measurement procedure, the PC software can also initiate the operations which command the MCU to commence with digital sampling of the V_{ctrl} node before and after introduction of

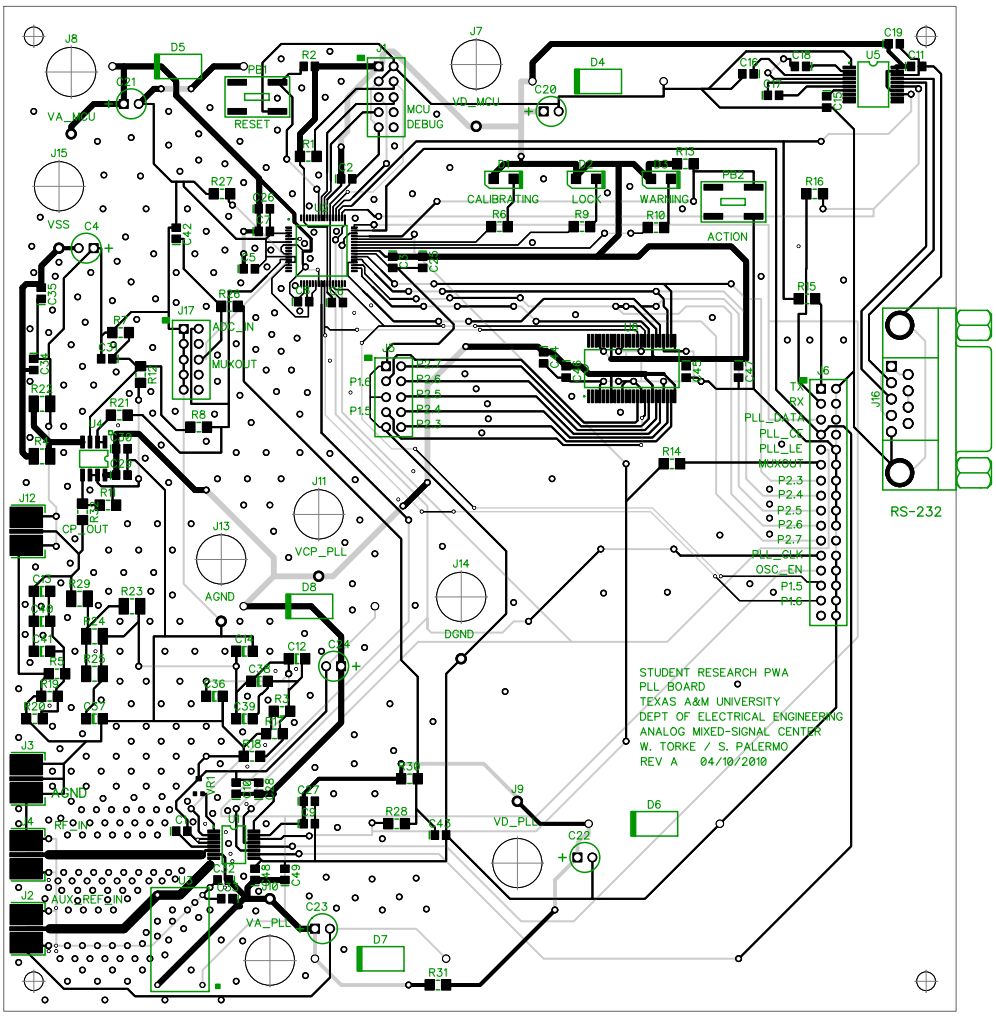

Fig. 20. PCB diagram of PLL Board indicating component footprints, top- and bottom-side traces.

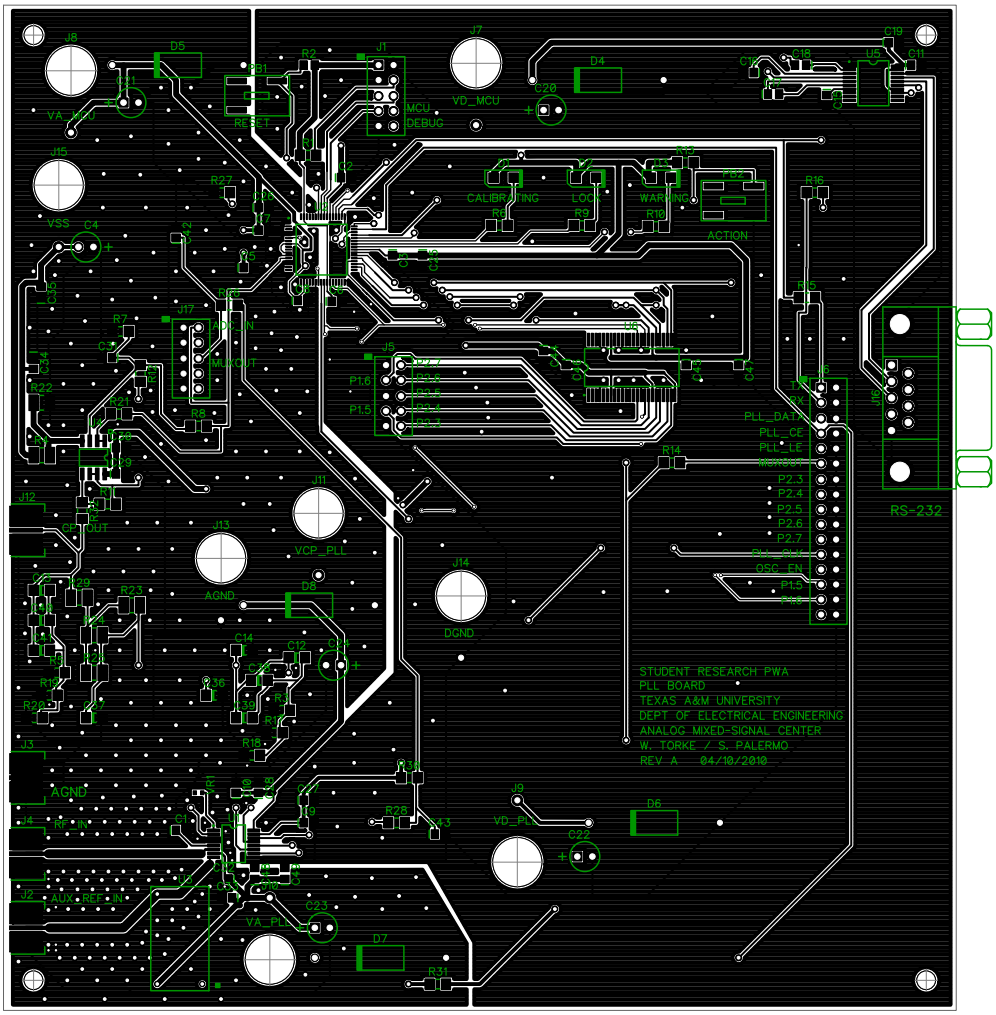

Fig. 21. PCB diagram of PLL Board indicating top-side copper, including ground planes.

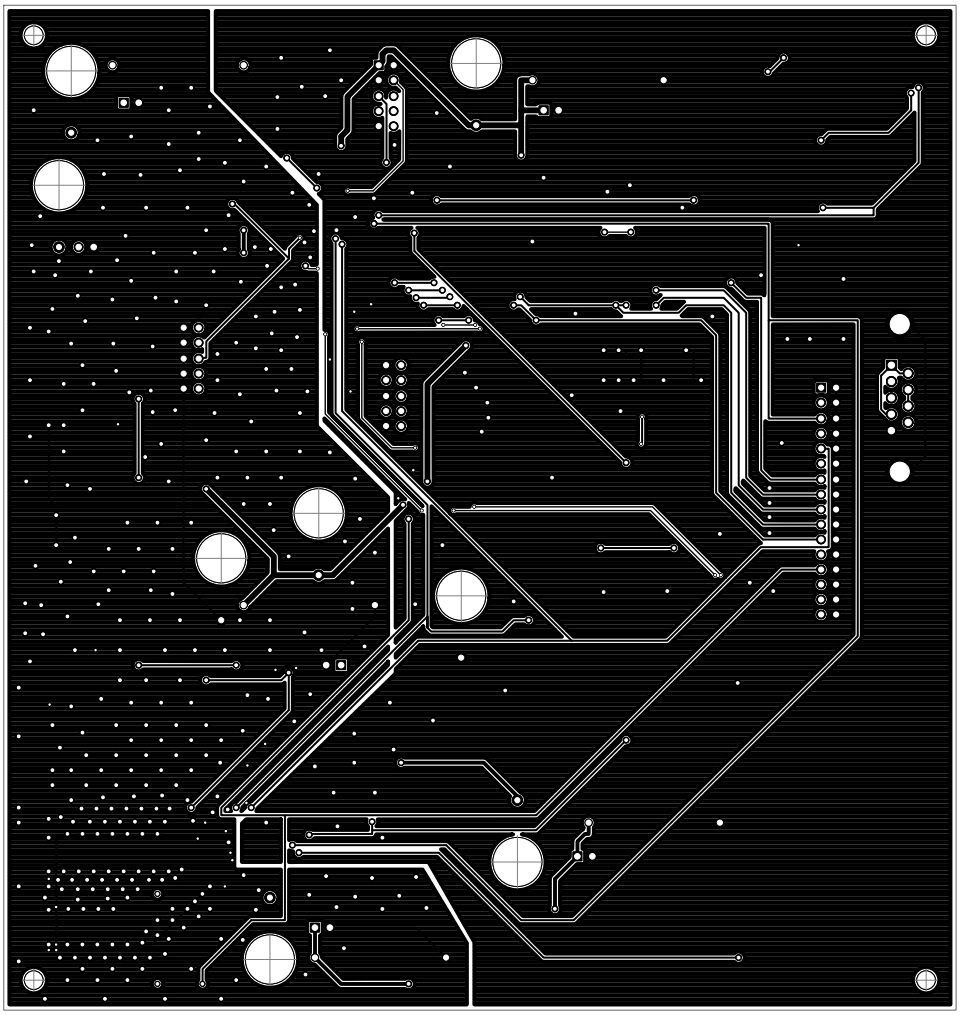

Fig. 22. PCB diagram of PLL Board indicating bottom-side copper, including ground planes.

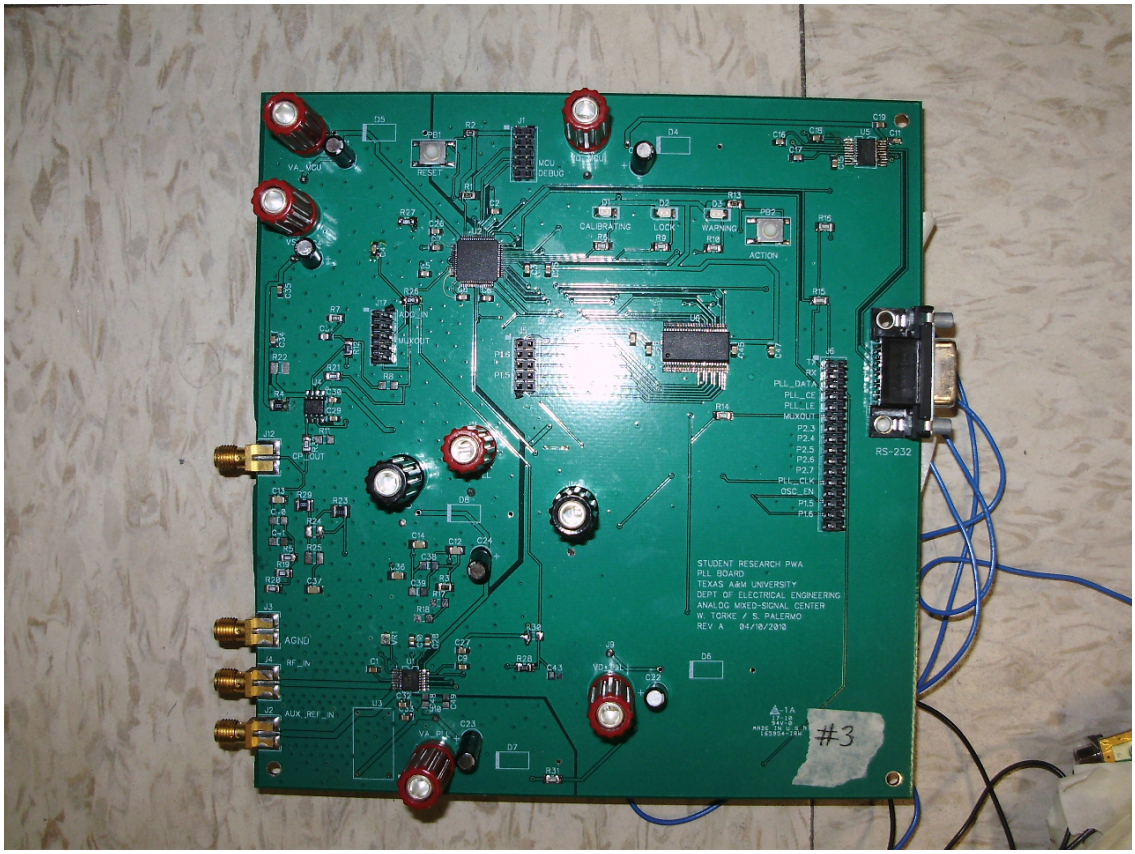

Fig. 23. Photograph of assembled PLL Board.

the MUT, and then later to manipulate the ADF4157 divider value until the V_{ctrl} voltage level has been returned to its original value.

The detailed aspects of the MCU firmware and PC software code are not included in this thesis, as they do not possess any particular relevance to the emphasis of this research effort. A screenshot of the PC software control panel is shown in Fig. 24 to provide a sense of the various operations which can be initiated by the user. This PC software was developed using the National Instruments LabView development software.

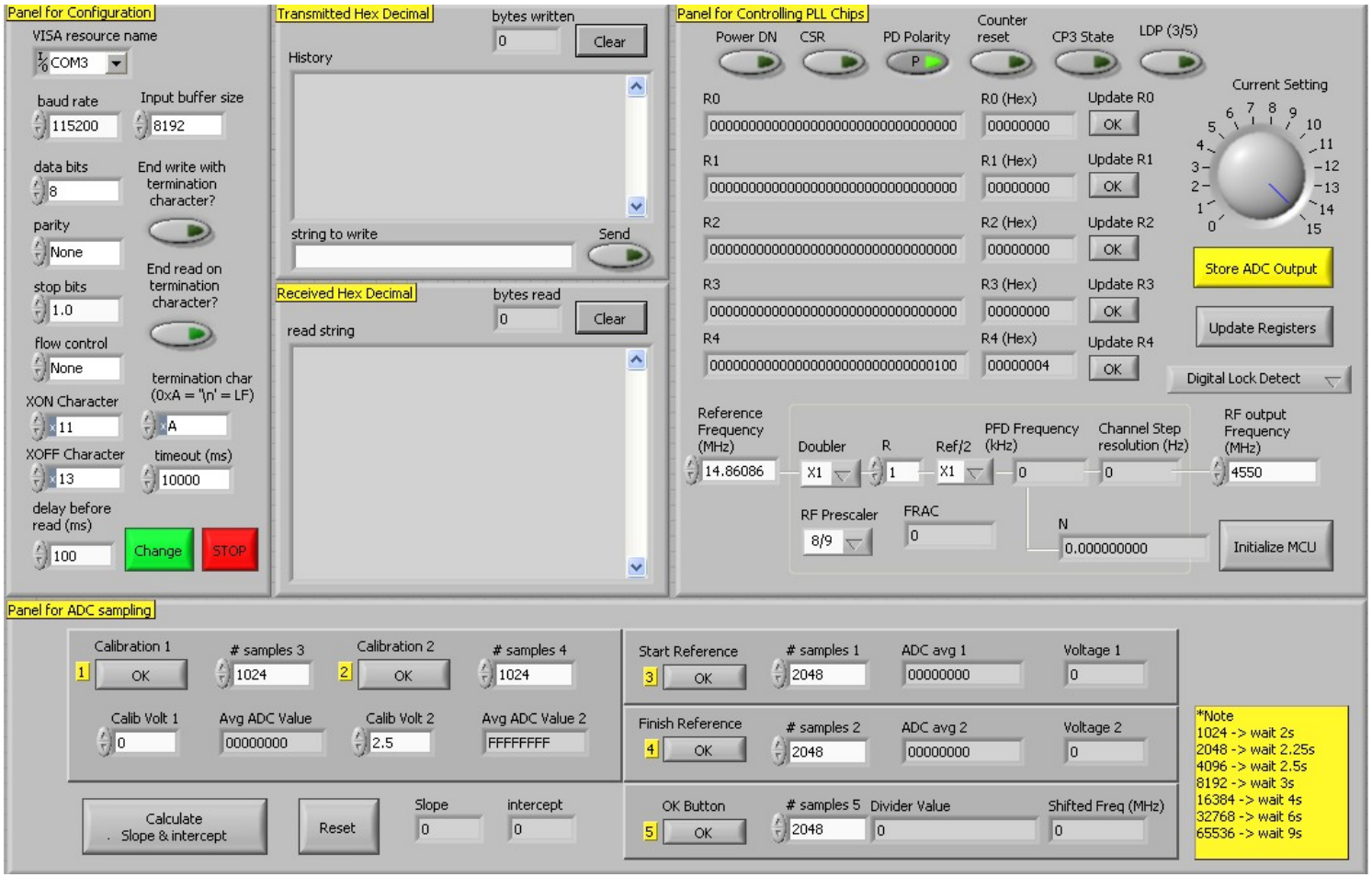

Fig. 24. Screenshot of control panel provided for the PC software application.

CHAPTER IV

SYSTEM PERFORMANCE

A. Introduction

In this chapter, various aspects of the system's performance are presented to confirm that the system operates in the anticipated manner and to quantify the system's frequency shift measurement sensitivity and dynamic range. The connectivity between the PLL Board and VCO Board assemblies is described first, to furnish a visual conceptualization of the actual physical frequency shift measurement system that was depicted in block diagram form in Fig. 7 and Fig. 14.

B. Interconnections Between PLL Board and VCO Board

A picture of the VCO Board and PLL Board assemblies is shown in Fig. 25. This diagram also illustrates the essential connections between these two assemblies. The high-frequency output from the VCO Board is connected via SMA cable to the RF input of the PLL Board. The V_{ctrl} voltage generated on the PLL Board is connected to the voltage control input of the VCO Board.

Note from the photograph of the VCO Board that a hollow plastic cylindrical tube has been affixed directly over the planer split-ring resonator sensor pattern on the VCO Board. This constitutes the test fixture into which the various liquid MUTs will be deposited during the test process.

C. PLL Transient Performance

To verify that the PLL exhibits the expected transient behavior, an 'artificial' frequency step at the VCO output was generated, during which time the V_{ctrl} voltage

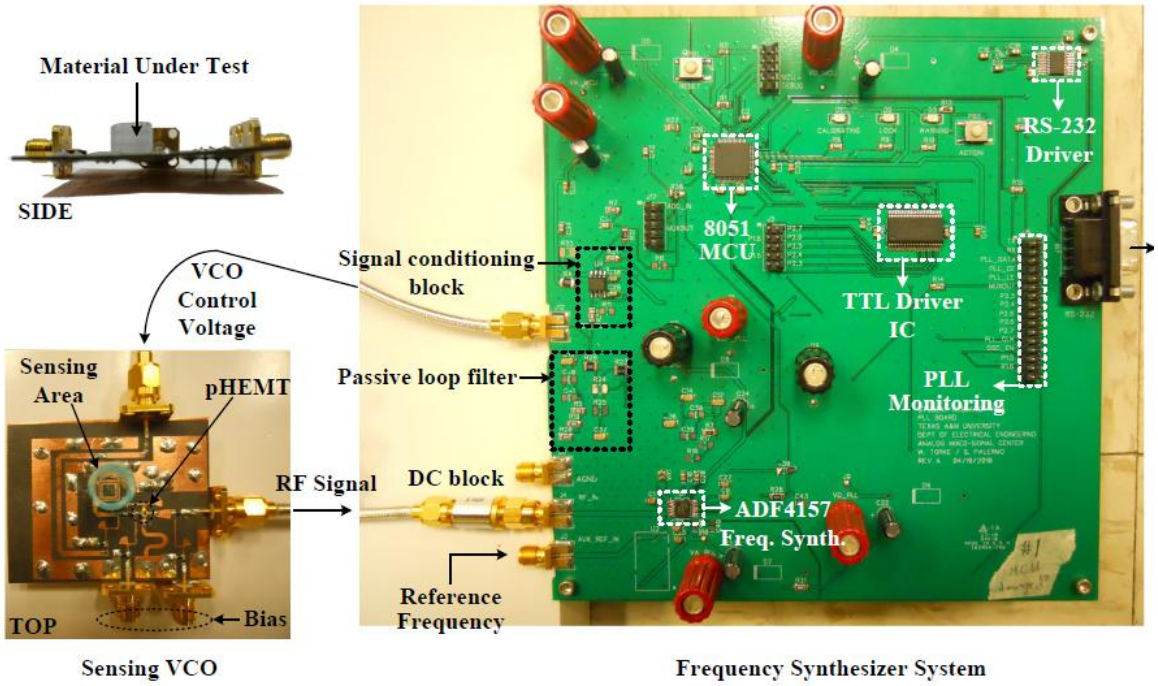

Fig. 25. Illustration of the VCO Board and PLL Board and the essential interconnections.

signal activity was monitored using a digital oscilloscope. The artificial frequency step was generated by using the PC software application to abruptly change the ADF4157 frequency divider value, such that the VCO output frequency would in turn exhibit a sudden shift in output frequency. The shift in the divider was chosen such that the VCO output frequency would transition from an initial frequency near the low end of the PLL lock range up to a frequency near the upper end of the PLL lock range. This was done in attempt to verify that the PLL is able to track and re-attain the lock state when a worst-case frequency step is imparted on the PLL. If the PLL is excessively sluggish in its attempt to track such a frequency step, such would indicate that the PLL bandwidth is too low and needs to be increased. Conversely, if this step in frequency causes the V_{ctrl} signal to exhibit a state of permanent oscillation, such would tend to indicate loop instability, in which case the bandwidth is likely too high and needs to be decreased.

A single-shot trace acquisition captured by the digital oscilloscope which illustrates the transient behavior of the V_{ctrl} node voltage during this frequency step event is shown in Fig. 26. This trace indicates that the V_{ctrl} signal exhibits an appropriate response to the frequency step by eventually settling to a new and greater DC voltage level. The PLL's ability to track this frequency step was further confirmed by using a spectrum analyzer to verify that the VCO output frequency had changed to the new expected value, based on the new frequency division value and the reference clock frequency. (The VCO output was connected to a signal splitter, such that one of the splitter outputs was connected to the ADF4157 $RF_{IN}A$ input pin while the other splitter output was connected to the spectrum analyzer.) Additionally, the ADF4157 can be configured to provides a digital Lock Detect output signal at the device's MUXOUT pin. The logic voltage level at this pin can be (and indeed was) checked as a confirmation that the PLL re-acquired a lock state.

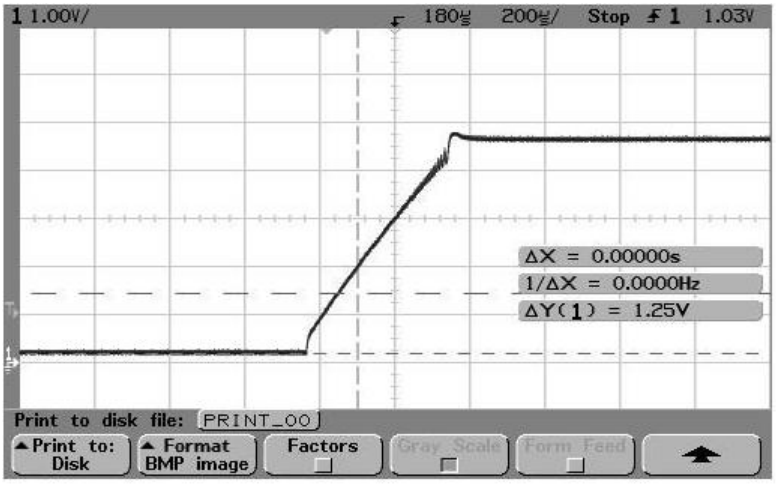

Fig. 26. Scope trace capture of V_{ctrl} transient behavior in reaction to frequency step.

The scope trace in Fig. 26 also indicates that the phase lock settling time appears be approximately 400 μs, which closely matches the predicted $\leq 1^\circ$ phase lock settling time of 395 μs predicted by the ADIsimPLL software.

D. PLL Lock Range

The lock range of the PLL was found to be ∼310 MHz, spanning from ∼4420 MHz up to ∼4735 MHz.

E. Analysis of Dynamic Range

A conservative assessment of the frequency measurement system's dynamic range would be based on the PLL lock range described just above. The conservative figure for the dynamic range would therefore be ∼310 MHz. But the system is actually capable of measuring frequency shifts which go well beyond the PLL lock range. For situations in which application of the MUT causes the V_{ctrl} voltage level to saturate at the upper extreme of its linear range, the PLL will temporarily fall out of the lock state. However, note that upon initiation of the firmware-controlled calculation

phase of the measurement process in which the loop divider value is adjusted until the original V_{ctrl} level is restored, the PLL will re-acquire a lock state as the V_{ctrl} voltage is pushed back into its available linear range. As long as the VCO continues to oscillate (noting that the range of input control voltages over which the VCO will maintain oscillation significantly exceeds the PLL lock range), the PLL can re-acquire a lock state, and the measurement of the frequency shift will be successful.

The practical dynamic range of the frequency measurement system is therefore significantly greater than the PLL lock range. However, the practical dynamic range is ultimately limited by the sensitivity degradation of the frequency shift measurement which occurs with increasing frequency shift. As will be seen in the next chapter regarding the actual test results, the sensitivity (or accuracy) of the frequency shift measurement system does in fact decrease in a non-linear fashion, as the magnitude of frequency shift caused by a particular MUT increases. Additionally, the measurement sensitivity also decreases in a similar non-linear fashion as the volume of MUT applied to the test well fixture increases. (This can be explained by visualizing that as the height of MUT fluid in the test well fixture increases, the electric field strength at the higher elevations above the planar microwave resonator decreases.) Therefore, the dynamic range is ultimately a quantity that must be defined in terms of the desired minimum sensitivity that can be tolerated. For example, if it is determined for a given application that the accuracy of frequency shift measurement can be relaxed (i.e., lower accuracy), the dynamic range of the frequency shift measurement system will increase.

F. Analysis of Measurement Sensitivity

1. Theoretical Measurement Sensitivity

A theoretical measurement sensitivity can be calculated. Here the term 'sensitivity' would be synonymous with 'resolution' or 'precision'. The sensitivity figure quantifies the increment of frequency shift measurement per LSB. Therefore the sensitivity would be expressed as Hz/LSB. The theoretical sensitivity is limited by the number of ADC bits. The ADC used for this application has a resolution of 16 bits. To calculate this sensitivity, we first note that the maximum input voltage to the ADC is 3.25V, which corresponds to the full-scale ADC value of 0xFFFF. We then note that the V_{ctrl} signal is scaled by a ratio of $\sim$0.672 before it is fed to the ADC input. Therefore, a full-scale ADC reading corresponds to a voltage level of 3.25V / 0.625 = $\sim$4.84V. We then divide this equivalent full-scale voltage level by the resolution of the ADC to get $\frac{4.84V}{2^{16}} =\sim$ 73.8 μV/LSB.

The sensitivity figure obtained just above can now be used to compute the sensitivity in terms of Hz/LSB by multiplying this result by the experimentally measured K_{VCO} of the VCO, which is $\sim$60 MHz/V. The sensitivity is therefore 73.8 μV/LSB $\cdot$ 60 MHz/V = $\sim$4.43 kHz/LSB. This figure represents a minimum quantization error for the frequency shift measurement. However, as will soon be discussed, the actual measurement sensitivity of the system is predominantly determined by the noise level present at the V_{ctrl} node.

G. Example of ADC Time Domain Data

It was possible to capture a limited number of consecutive ADC data samples. A typical example of the ADC data taken for 1024 consecutive data samples is shown in Fig. 27. This particular bust of ADC data was taken with no MUT applied to the

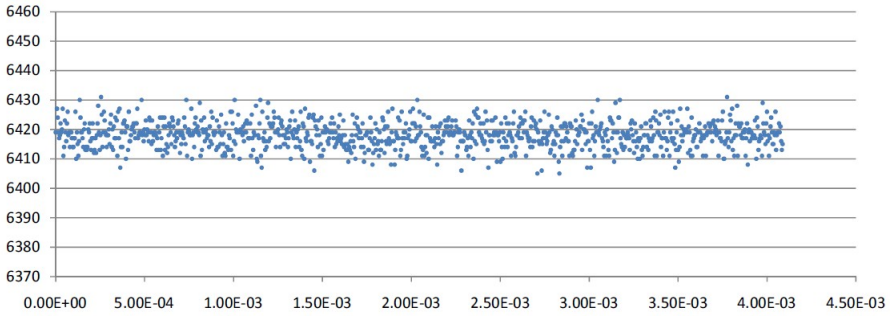

Fig. 27. Example of raw digital samples acquired by ADC.

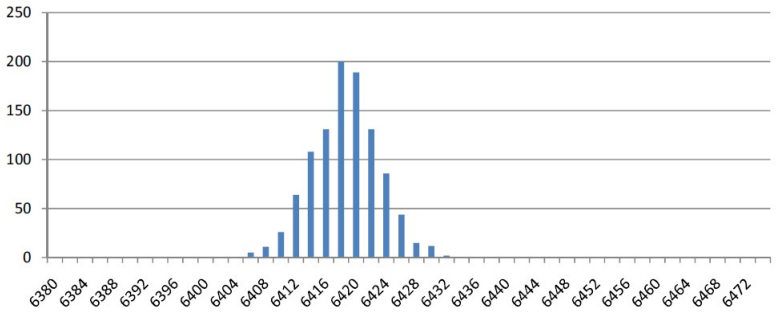

Fig. 28. Example of raw digital samples acquired by ADC.

sensor fixture. Note that the y-axis in this plot indicates the raw ADC code values.

A histogram of the ADC sample values captured in the above transient plot is provided in Fig. 28. It can be seen that the distribution of samples resembles a normal distribution. The standard deviation of these ADC values as computed from the sample variance is ∼4.56 LSBs. We can use the theoretical sensitivity figure computed in Section 1 measured in terms of V/LSB to conclude that the standard deviation of the real-time ADC data samples translates to 4.56 LSBs · 73.8 μV/LSB = ∼337 μV.

H. Actual Measurement Sensitivity

Recall that the frequency shift measurement performed for any given test 'trial' (referring to a application of a given MUT to the fixture) is to be performed by computing the average value of a set of consecutive raw ADC samples which are collected before and after the MUT is introduced to the sensor fixture. In effort to quantify the minimum number of raw ADC samples that should be averaged to insure that the variance of this average result is not determined primarily by the sample size, a experimental analysis of the system was performed. In this analysis, the number of ADC samples to be averaged was increased by powers of 2, starting with a sample size of 2048. For each sample size value, 32 averages were obtained. For each of the sample sizes which were tested, the standard deviations of these 32 average results were computed. These standard deviations are plotted in Fig. 29. This figure would indicate that a sample size of at least 32768 raw ADC samples should be used to compute the average for any given 'trial'. It can be seen from this plot that the standard deviation of multiple trials would seem to asymptotically approach a final value in the vicinity of 55mV. Therefore, as long as the size of each sample set is greater than 32768 samples, the variation in any given measurement result will not be dominated by the size of the sample set, but will instead be primarily attributable to one or more actual physical noise phenomena present within electronic measurement system.

To summarize, these results indicate that to avoid excessive variance in a given measurement of V_{ctrl} which is caused by averaging an insufficient number of raw ADC samples, the minimum sample size of raw ADC samples which should be averaged for any such measurement trial should not be less than 32768. As long as this condition is met, the remaining variation in any such measurement trial should be predominantly caused by other *physical* system errors.

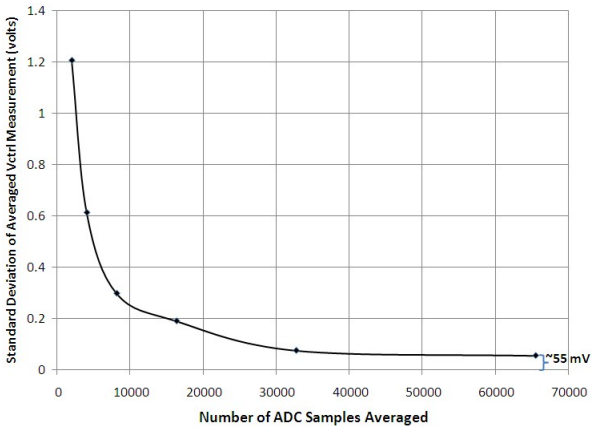

Fig. 29. Example of raw digital samples acquired by ADC.

It is worth noting at this point that for all such testing, the size of the ADC sample set for all trials was held at $2^{16} = 65536$ samples.

The experimental results obtained using this measurement system to perform actual chemical detection are presented in the next section. Additionally, it should be mentioned that the effective sensitivity or precision of the measurement results can be improved by running multiple trials of the same exact test. During virtually all of the testing which is described in the next section, note that five test trials were conducted for any particular test condition, and for any given MUT. Assuming that the measurement results from trial to trial are statistically independent, the standard deviation of the frequency shift measurement computed from the *average* of the five frequency shift measurement trials will be reduced (i.e., improved) by a factor of $\sqrt{5}$ [22].

An attempt was made to quantify the VCO phase noise using an HP8142SP Spectrum Analyzer. A screen shot which shows the VCO's a typical phase noise profile of the VCO as measured by spectrum analyzer is shown in Figure 30. The integrated phase noise was measured to be 464.1 mRad.

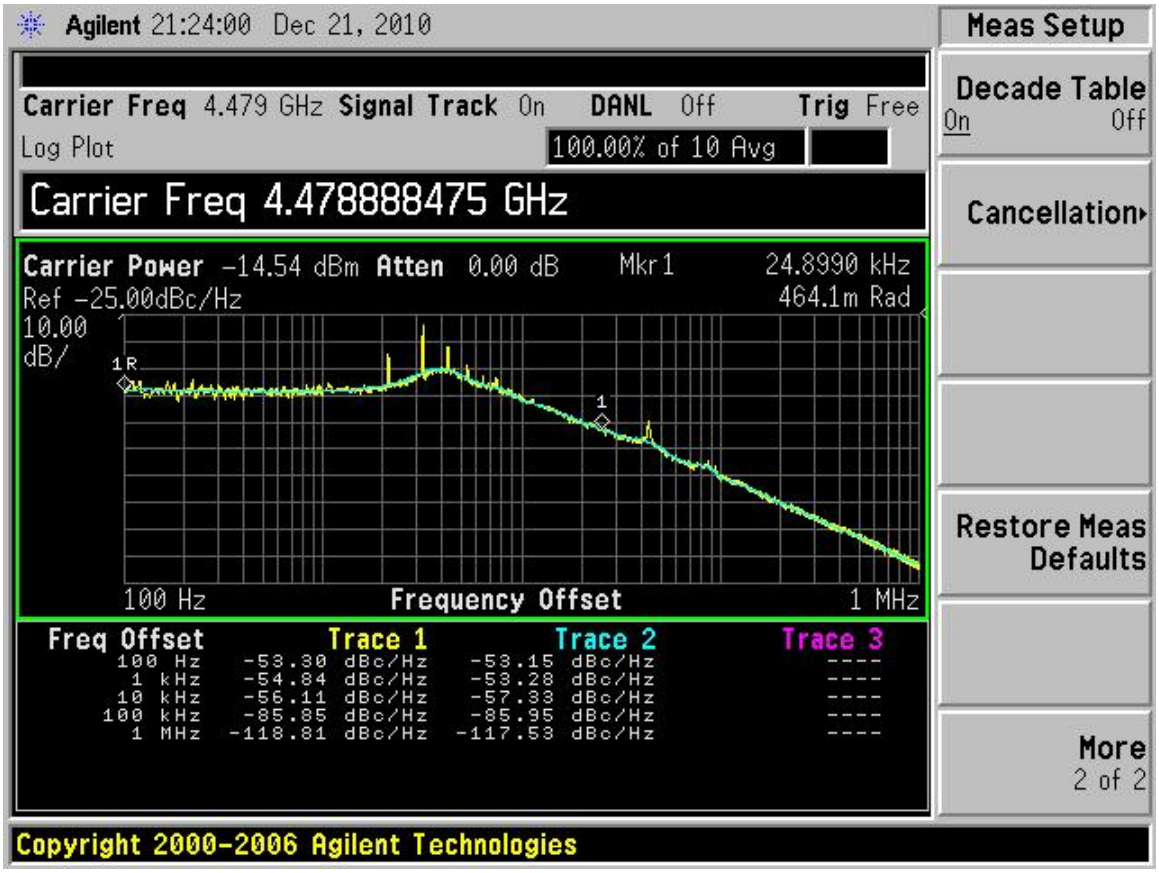

Fig. 30. Phase noise profile of VCO.

CHAPTER V

TEST RESULTS

A. Introduction

Two types of testing were performed to evaluate the merit of this frequency shift measurement system:

- Several common liquid chemical substances were individually applied to the sensor fixture and the frequency shift caused by the introduction of each substance was measured. These frequency shift measurements were used to construct a mathematical characteristic relating the magnitude of frequency shift to a projected dielectric constant, for each respective substance. The experimentally derived dielectric constant values were then compared with the published dielectric constant values for each respective substance.

- Several pairs of the liquid substances mentioned just above were homogeneously mixed together in various known concentrations. An effective dielectric constant value of each homogeneous mixture was computed using the well-known Maxwell-Garnett Mixture Formula. The various mixtures were then individually applied to the sensor fixture and the frequency shift measurements were recorded. Based on these frequency shift measurements, values for the effective dielectric constant were projected for each mixture concentration and these dielectric constants were compared to the effective dielectric constant values predicted by the Maxwell-Garnett Mixture Formula. The goal of these tests was to evaluate the system's ability to reliably and accurately quantify the relative concentration of two known substances when they are homogeneously mixed together in unknown relative concentration.

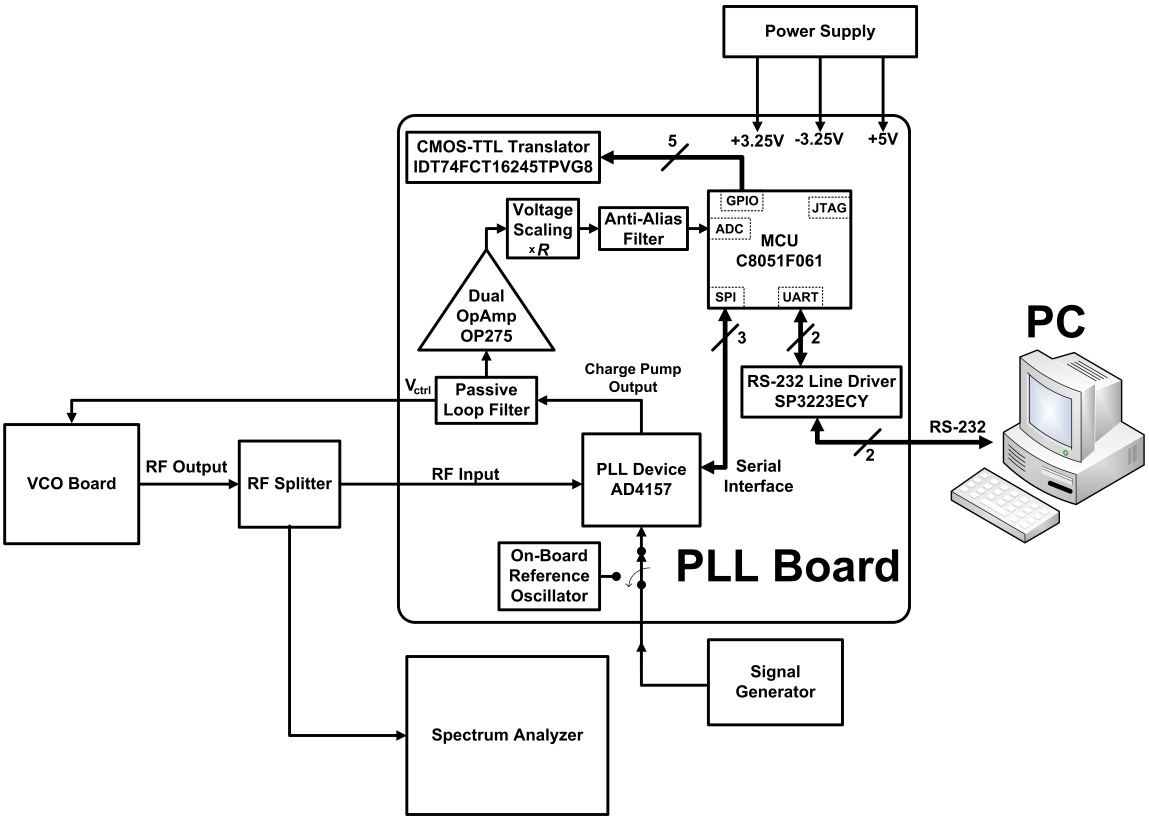

Fig. 31. Diagram of laboratory test setup.

B. Test Setup

A diagram of the laboratory setup used to conduct these tests is provided in Fig. 31.

The output from the VCO Board is sent to a signal splitter. One of the splitter's outputs is connected to the RF input of the PLL Board, to complete the phase-lock loop. The other splitter output is connected to a spectrum analyzer, to allow for visual monitoring of this output signal.

For these tests, a laboratory signal generator was used to provide the PLL reference clock signal, although the on-board canned oscillator option could have been used.

The ±3.25V and +5V power supplies are provided using two laboratory DC

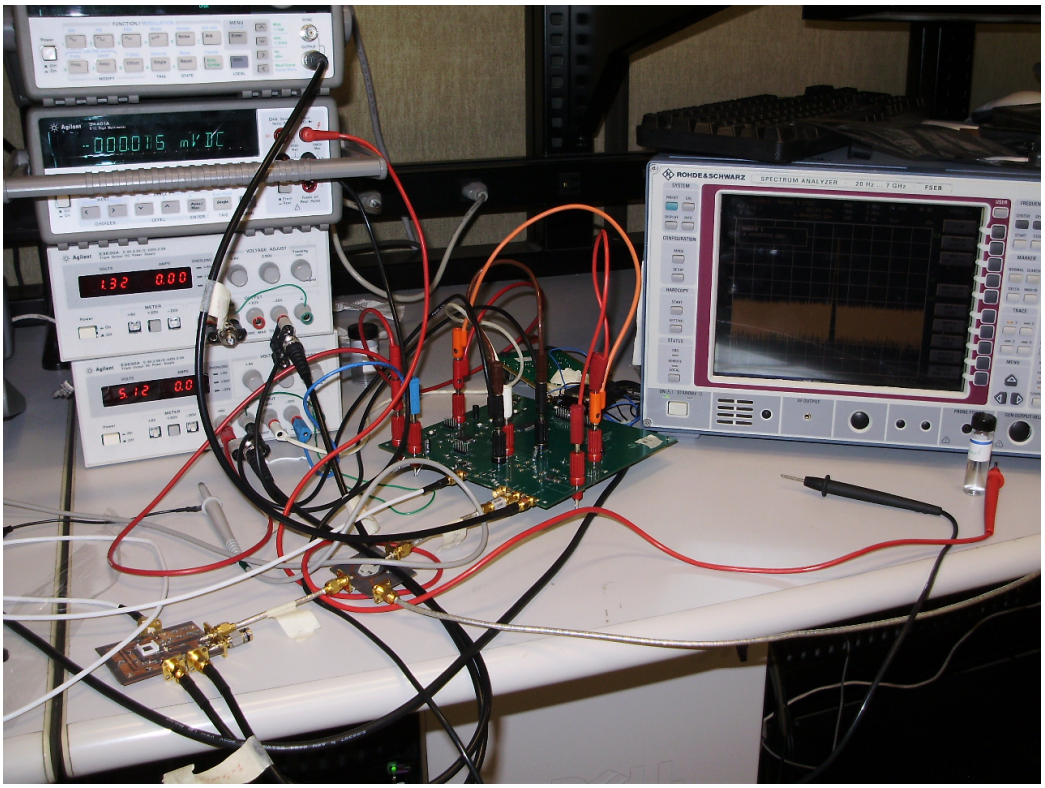

Fig. 32. Photograph of laboratory test setup.

power supplies.

The PLL Board is connected to a PC through the RS-232 connector to allow for control of the system from the PC. Note however that the PC connection and software application were developed out of convenience. To realize a complete stand-alone system, the firmware could be enhanced to provide full control of system operations through actuation of one or more on-board push-buttons, and an LCD display could be added to the PLL Board assembly to display relevant input and output information. The point here is that the addition of the PC and laboratory equipment was made out of convenience. But a true stand-alone version of this system could certainly be achieved within additional effort.

A photograph of the test setup is shown in Fig. 32

In the remainder of this chapter, the testing is described in more detail, and the results of these tests are presented.

C. Tests for Quantitative Identification of Dielectric Constant

For this testing, several distinct chemical substances were individually applied to the sensor fixture and the resulting frequency shift was measured. Such testing was performed on each chemical substances over a range of specific volumes. That is, the frequency shift was measured as incremental volumes of the given chemical substance were gradually added to the well fixture. Five independent trials were performed for each chemical substance, at each volume level. The chemical substances which were tested are listed just below.

- Xylene
- Ethanol
- Methanol
- 2-Butyl Alcohol
- Ethyl Acetate
- Ethylene Glycol

The frequency shift data points acquired at each test volume quantity for each of the tested chemical substances are displayed in the upper plot of Fig. 33. As was mentioned in Chapter IV, five trials were run at each test volume for each individual chemical. The lower plot in Fig. 33 indicates the standard deviation of the five trials at each volume level for each individual chemical.

Two of the chemical substances listed above, ethanol and methanol, were designated as 'calibration' substances. To develop a characteristic between the frequency shift measured for a given MUT with respect to that MUTs dielectric constant value,

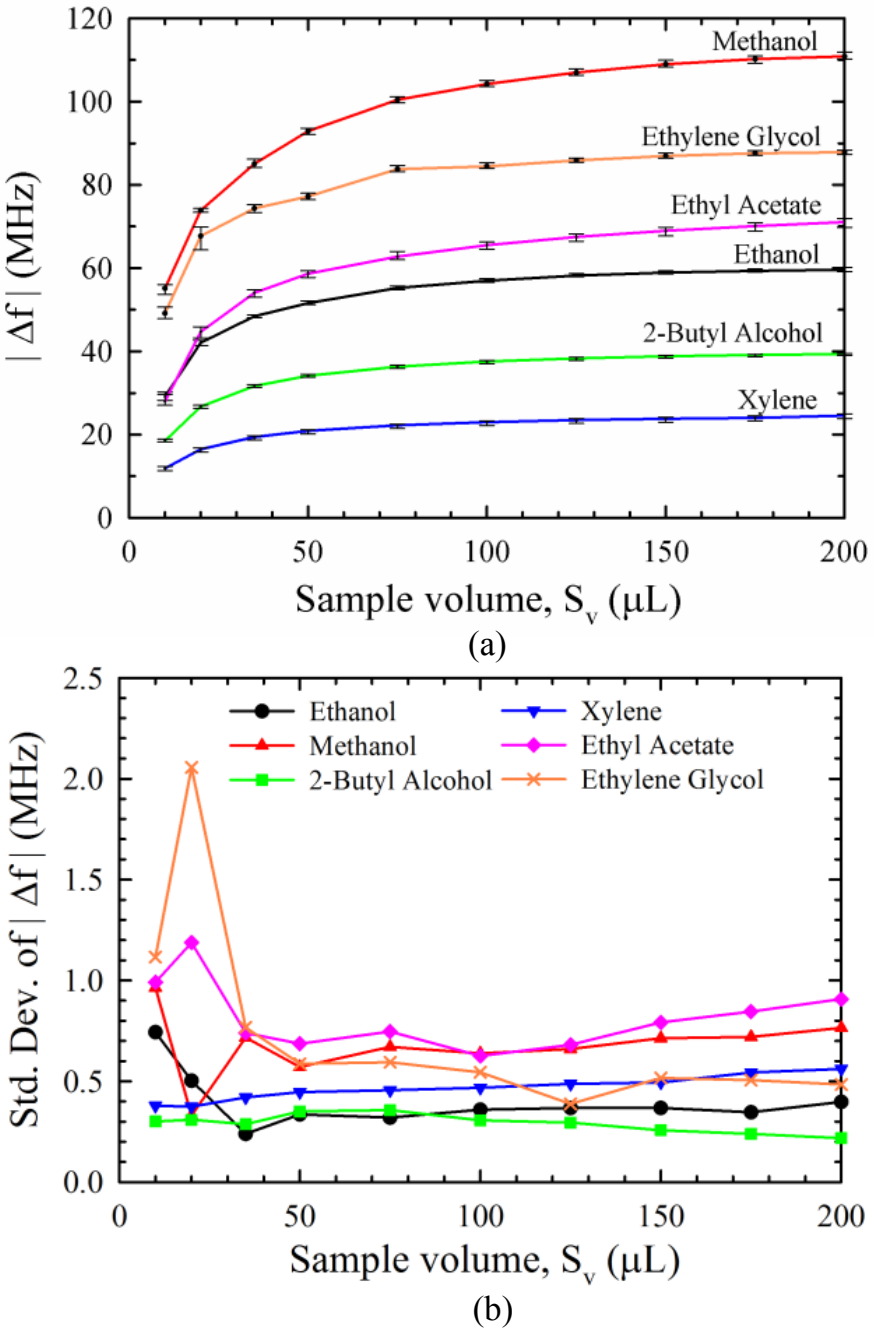

Fig. 33. Photograph of laboratory test setup.

it was necessary to identify at least two of the MUTs as calibration substances. Ethanol and Methanol were selected as calibration substances because the dielectric constant values for these two chemicals have been quantified to a high degree of certainty. The frequency shift measured for these two substances, along with were equated to the published dielectric constant values for these substances. Then these two data points were taken along with the zero frequency shift data point (when no MUT is applied to the test fixture) to generate curve-fit equations at each of the volume levels which were run for every chemical substance. The curve-fit equation derived at each test volume level (S_V) has the following quadratic form:

$$|\Delta f(S_V)| = a(S_V)\epsilon_r'^2 + b(S_V)\epsilon_r' + c(S_V) \tag{5.1}$$

This equation can be rearranged to yield an expression for the experimental dielectric constant (ϵ_r') for any given chemical, at a particular test volume level (S_V). The expression is:

$$\epsilon_r' = \frac{-b(S_V) + \sqrt{b(S_V)^2 - 4a(S_V)c(S_V)}}{2a(S_V)} \tag{5.2}$$

The coefficients for the curve-fit equations derived at each test volume level are listed in Table II.

Graphical plots of the quadratic curve-fit equations whose coefficients are listed in Table II are shown in Fig. 34.

The frequency shift measurements obtained for the remaining four chemical substances that were tested were then used as the input parameter to the curve fit equations, and an experimental ϵ_r' value was derived, at each test volume level. Plots of these experimentally derived ϵ_r' values are shown in Fig. 35. Note that the circular data point markers represent the average value of the five trial runs, while the verti-

Table II. Chemical calibration coefficients.

S_v (μL)	$a(S_v)$	$b(S_v)$	$c(S_v)$
10	$-0.316 \pm 10.5\%$	$8.98 \pm 5.30\%$	$-8.67 \pm 5.10\%$
20	$-0.511 \pm 4.2\%$	$13.31 \pm 2.30\%$	$-12.80 \pm 2.20\%$
35	$-0.588 \pm 1.2\%$	$15.32 \pm 0.55\%$	$-14.59 \pm 0.56\%$
50	$-0.605 \pm 1.4\%$	$16.19 \pm 1.10\%$	$-15.59 \pm 1.10\%$
75	$-0.637 \pm 1.1\%$	$17.27 \pm 0.87\%$	$-16.63 \pm 0.86\%$
100	$-0.652 \pm 1.2\%$	$17.79 \pm 0.97\%$	$-17.14 \pm 0.97\%$
125	$-0.660 \pm 1.0\%$	$18.14 \pm 0.80\%$	$-17.48 \pm 0.80\%$
150	$-0.663 \pm 1.2\%$	$18.33 \pm 0.75\%$	$-17.66 \pm 0.73\%$
175	$-0.663 \pm 1.4\%$	$18.43 \pm 0.80\%$	$-17.77 \pm 0.77\%$
200	$-0.664 \pm 1.1\%$	$18.50 \pm 0.85\%$	$-17.83 \pm 0.85\%$

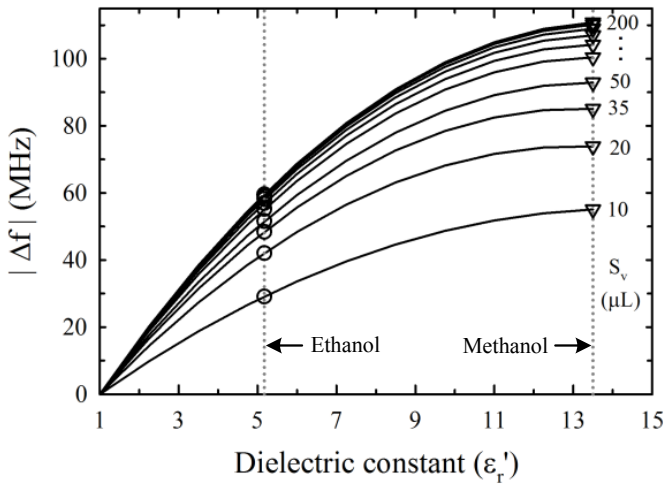

Fig. 34. Family of quadratic calibration curve equations. Coefficients for these equations listed in Table II. Each curve denotes a specific test volume level.

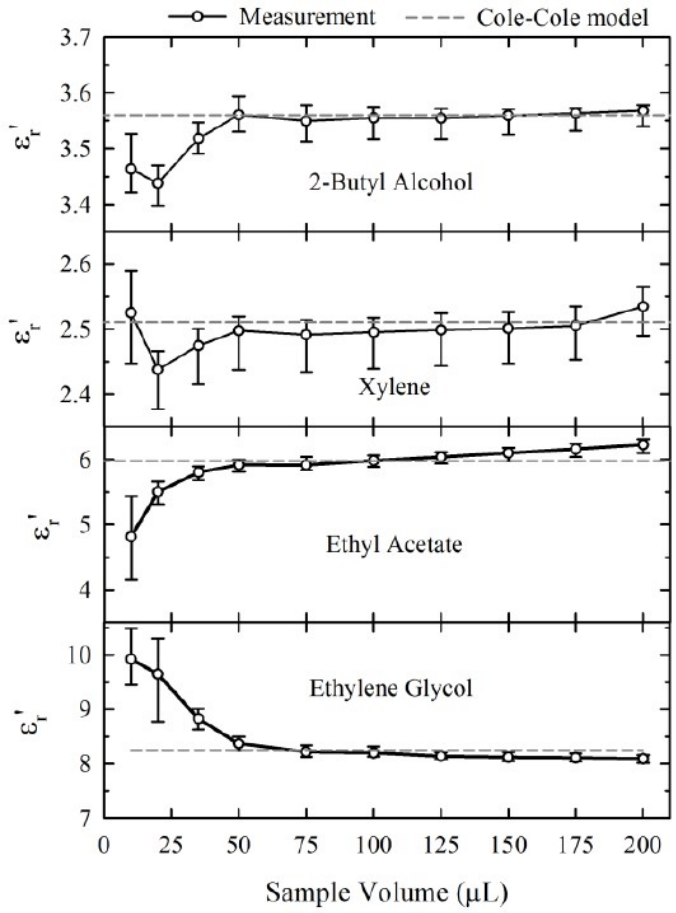

Fig. 35. Experimentally derived ϵ_r values for the four 'non-calibration' chemical substances, at each test volume level.

cal bars represent the range of the five test trials, at each data point. In each of the four plots, the theoretical ϵ_r' value for each chemical is represented by the horizontal dotted line.

These results indicate that for test volume levels above 50 μL, the experimentally derived ϵ_r' values obtained for each chemical substance are relatively constant over volume, and they closely match the theoretical ϵ_r' values [23] for each respective chemical substance. The derived ϵ_r' values for the four test substances are shown numerically in Table III. The agreement of the experimentally derived ϵ_r' values

with the theoretical ϵ_r' values is impressive, and these results indicate that the test system would seem to be capable of consistent and reasonably accurate quantitative measurement of the dielectric constant of liquid chemical substances.

Table III. Extracted dielectric constants of organic MUTs for sample volumes from 50–200 μL.

-	Theory	Measurements						
Organic MUT	Cole-Cole	50 μL	75 μL	100 μL	125 μL	150 μL	175 μL	200 μL
2-Butyl Alcohol	3.56	3.56 ± 0.033	3.55 ± 0.036	3.55 ± 0.038	3.55 ± 0.037	3.56 ± 0.033	3.56 ± 0.030	3.57 ± 0.028
Xylene	2.51	2.50 ± 0.060	2.49 ± 0.057	2.50 ± 0.056	2.50 ± 0.055	2.50 ± 0.054	2.51 ± 0.052	2.53 ± 0.044
Ethyl Acetate	5.98	5.92 ± 0.103	5.91 ± 0.124	5.98 ± 0.095	6.04 ± 0.103	6.09 ± 0.119	6.16 ± 0.121	6.22 ± 0.127
Ethylene Glycol	8.25	8.37 ± 0.129	8.22 ± 0.118	8.20 ± 0.115	8.14 ± 0.070	8.12 ± 0.093	8.11 ± 0.077	8.08 ± 0.071

D. Mixture Tests

Various homogeneous mixtures of ethanol and 2-butyl alcohol were formulated. The system was then used to obtain frequency shift measurements for each of the unique mixture concentrations. The volume of MUT dispensed for each test frequency shift measurement trial was 100 uL. Five trials were run for each unique mixture concentration. A plot of the average frequency shift measurement over the five trials for each unique mixture concentration is shown in Fig. 36. The x-axis of this plot denotes the 'effective' theoretical ϵ_r' value for each mixture, which was computed using the standard Maxwell Garnett Mixture Formula:

$$\epsilon_{eff} = \epsilon_e + 3\epsilon_e \frac{\epsilon_i - \epsilon_e}{\epsilon_i + \epsilon_e - f(\epsilon_i - \epsilon_e}$$

where:

ϵ_e is the ϵ value of the environment substance

ϵ_i is the ϵ value of the inclusion substance

f = volume of fraction of inclusion

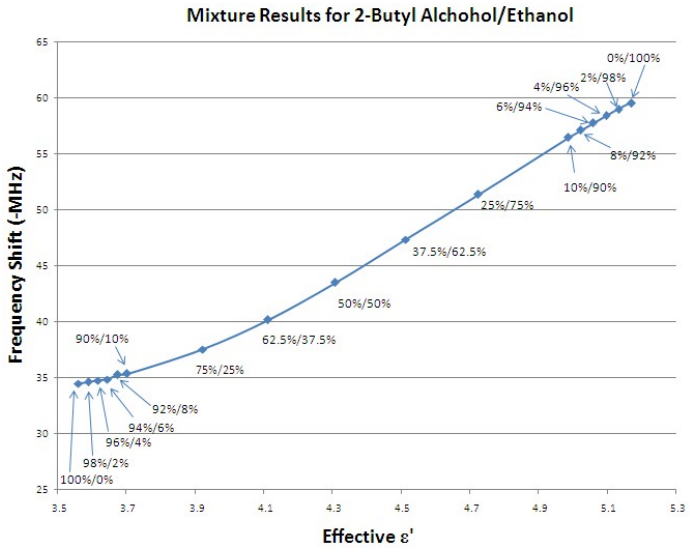

Fig. 36. Frequency shift measurements for homogeneous ethanol/2-butyl alcohol mixtures of varying concentrations.

ϵ_{eff} = effective ϵ of the given mixture

These results are quite consistent and they exhibit an expected monotonic increase in the frequency shift with increasing effective ϵ_r value. However, a straight line characteristic was expected. The trend of these results does exhibit a somewhat tapered characteristic, especially near the extreme ends of the characteristic, which are the regions in which the mixtures are relatively unbalanced. An explanation for the slight non-linear characteristic of these results has yet to be obtained. It is possible that the slightly non-linear trend may be due to certain non-ideal aspects of the microwave sensor test fixture as well as the amount of area coverage that is achieved by the MUT over the planer sensor trace pattern on the VCO Board. Despite this, the repeatability of these test results tends to suggest that this measurement system is potentially capable of consistently distinguishing the relative concentrations of two-chemical homogeneous mixtures.

CHAPTER VI

CONCLUSIONS AND FUTURE WORK

A. Conclusions

This thesis work consisted of the design, implementation, and test of a PLL-based frequency shift measurement system for chemical and biological sensing. This research was motivated by a proposal to employ a novel sensing technology consisting of a planer microwave resonator integrated within an active voltage controlled oscillator (VCO). Such a VCO assembly was included within a PLL-based frequency synthesizer and an ADC was used to digitally sample the PLL control voltage fed to the VCO. Computation of the change in control voltage measured before and after introduction of the MUT was used to indirectly calculate the shift in the resonator sensor's natural frequency. The frequency shift measurement results can can in turn allowed for quantitative determination of the MUT's dielectric constant. Experimental results indicate that the dielectric constant of various MUTs can be measured to within an accuracy of $\pm 2\%$.

The experimental results indicate that such integration of a VCO containing a microwave resonator sensor within a PLL achieves a chemical sensor solution which is reasonably accurate as well as relatively inexpensive and portable, in comparison to other microwave resonator-based sensor solutions. This sensor technology could also be deployed for biological sensing applications pertaining to DNA detection, which has proven to be a valuable tool for early detection of genetic predispositions such as Down's syndrome, Alzheimer's disease, Haemophiolia, etc. The portability and economic feasibility of this technology could potentially allow for ubiquitous usage of such sensor equipment in point-of-care health clinics throughout the world.

Additionally, in comparison to use of the same VCO to measure frequency shift in an open-loop configuration, incorporation of the VCO into a PLL as described herein enabled measurement of frequency shift to a significantly improved degree of precision. The improved measurement precision in turn allowed for a more accurate quantitative assessment of a MUT's ϵ_r' value [24]. This improvement is presumably due to prudent selection of the loop bandwidth to achieve significant attenuation of the VCO phase noise.

B. Future Work

Opportunities for future work include development of a modified version of the VCO which contains the microwave resonator sensor, such that the loss factor of the MUT could also be quantitatively measured. The ability to measure a MUT's loss measurement combined with the proven ability to measure the MUT's dielectric constant would constitute a system which is capable of complete characterization of the MUT's permittivity. Such a system would thereby constitute a sensor product which is capable of absolute identification (i.e., conclusive detection) of various chemical substances. Additionally, it is likely that this sensor technology could be implemented in the form of a partially integrated [possibly even a completely integrated] monolithic device. The results of this work would suggest that development of an integrated version of this sensor technology would be warranted. In this sense, this research was intended to serve as a proof of concept which could justify the subsequent development of an integrated version of this sensor system.

It is also likely that a more accurate version of frequency shift measurement system could be achieved by constructing a more sophisticated sensor test fixture. In particular, incorporation of an enclosed fluidic circulation apparatus located in close

vicinity to the planer microwave resonator would likely allow for more consistent and precise measurement of the MUT's dielectric constant. Such a fluidic circulation system would insure more precise control of the volume of MUT substance that is presented to the SRR sensor. It would also eliminate measurement error caused by gradual evaporation of the MUT, which proved to be an issue in this research effort. Additionally, the circulation of the liquid MUT would arguably provide a more homogeneous MUT sample.

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VITA

William James Torke received his Bachelor of Science in Electrical Engineering from Purdue University (West Lafayette, IN, USA) in 1995. During his undergraduate study he also worked as a Co-Op employee at Thomson Consumer Electronics. He has worked at several companies in Austin, TX including AMD, Cygnal Integrated Products, Inc. (since acquired by Silicon Labs, Inc.) and Cirrus Logic, Inc. He has worked primarily as an applications engineer supporting power metering products and microcontrollers, and also as a software/firmware engineer. He started pursuing his master's degree in electrical engineering at Texas A&M University under the guidance of Dr. Samuel Palermo in August 2009. William's primary masters research topic pertains to phase-locked loops. His mailing address is Analog Mixed Signal Center; Department of Electrical and Computer Engineering; Texas A&M University; College Station, TX 77843. He can be contacted via email at wtorke@gmail.com.