A 3-BIT CURRENT MODE QUANTIZER FOR CONTINUOUS TIME DELTA SIGMA ANALOG-TO-DIGITAL CONVERTERS

A Thesis

by

ARUN SUNDAR

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2011

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jose Silva-Martinez
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ABSTRACT

A 3-Bit Current-Mode Quantizer for Continuous Time Delta Sigma Analog-to-Digital Converters. (December 2011)

Arun Sundar, B.E., Anna University, Chennai

Chair of the Advisory Committee: Dr. Jose Silva-Martinez

The summing amplifier and the quantizer form two of the most critical blocks in a continuous time delta sigma (CT ΔΣ) analog-to-digital converter (ADC). Most of the conventional CT ΔΣ ADC designs incorporate a voltage summing amplifier and a voltage-mode quantizer. The high gain-bandwidth (GBW) requirement of the voltage summing amplifier increases the overall power consumption of the CT ΔΣ ADC.

In this work, a novel method of performing the operations of summing and quantization is proposed. A current-mode summing stage is proposed in the place of a voltage summing amplifier. The summed signal, which is available in current domain, is then quantized with a 3-bit current mode flash ADC. This current mode summing approach offers considerable power reduction of about 80% compared to conventional solutions [2]. The total static power consumption of the summing stage and the quantizer is 5.3mW. The circuits were designed in IBM 90nm process. The static and dynamic characteristics of the quantizer are analyzed. The impact of process and temperature variation and mismatch tolerance as well as the impact of jitter, in the presence of an out-of-band blocker signal, on the performance of the quantizer is also studied.

To Dr. P.V. Ramakrishna and Mrs. N. Vijaya

(College of Engineering, Guindy, Anna University, Chennai, India)

who inspired me into Analog Circuit Design

To my ever loving amma and appa

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I was fortunate to attend all the courses that Dr. Silva offered namely VLSI Circuit Design, IC Design for Broadband Communication Circuits and Mixed Signal Interfaces. They covered pretty much all the challenging aspects which analog design had to offer. I built a strong base for my professional career in analog design with the help of these courses, for which I am greatly indebted to Dr. Silva. If there ever were one course for which I had worked the hardest (and spent the most time), it was for Advanced Analog Circuit Design. I would like to thank Dr. Sanchez who, through this course, taught me one of the most important lessons for life – “to be successful, one needs to put in 10,000 hours of hard work”.

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and Hyung-Joon Jeon, who guided me and helped me with my research. I would also like to thank all my friends in AMSC, with whom I did coursework and research, for the wonderful learning experiences they provided. Special mention goes to Jesse Coulon, Will Torke, Ahmed Ragab, Ehsan Zhian Tabasy, Ayman Amin, Hajir Hedayati, Alejandro Vera, Yang Su, Chen Ma and Shweta Jindal.

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1. INTRODUCTION

1.1. Motivation

Present day wireless data communication devices demand a wireless receiver which accommodates various data standards [1]. Numerous communication standards are being used for various applications as shown in Figure 1. The advantages of digital signal processing coupled with improvements in the processing technology, encourage RF systems to be designed with a lot of emphasis on digital processing. This is further catalyzed by the tremendous growth of semiconductor processing technology which keeps pushing the technology node down to few tens of nanometers, thereby decreasing the total area of integrated circuits and the power consumption.

Figure 1 Current generation wireless applications and standards

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This thesis follows the style of *IEEE Journal of Solid State Circuits*.

Digital circuits are also more robust to process variations and provide a large dynamic range at a low cost. But for the digital world to interface with the real world of analog signals, analog-to-digital converters (ADCs) are needed. Figure 2 shows a generic wireless receiver chain [2]. Placing the ADC as close to the antenna as possible, helps reduce the receiver's complexity and increase the programmability of the receiver for various standards. In this case, operations like frequency translation and filtering which are traditionally performed in the analog/RF domain can be done in digital domain, resulting in considerable power savings too. Hence, the ADC needs to digitize an RF, intermediate frequency (IF) or baseband signal based on its location in the chain.

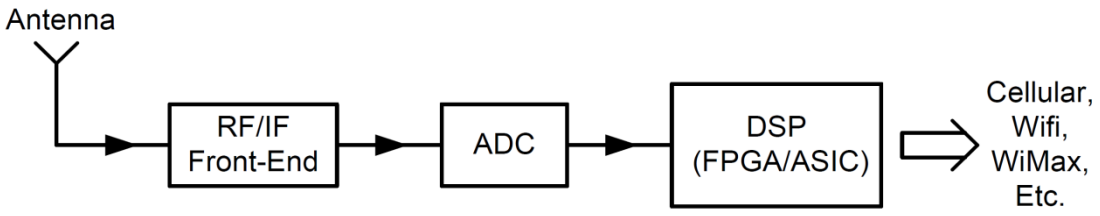


Figure 2 Generic radio receiver architecture

A flexible receiver needs to accommodate the narrowband / high dynamic range requirements of cellular standards and the wideband / low dynamic range requirements of WLAN and WiMAX. This calls for high performance ADC architectures such as the continuous time (CT) delta sigma (ΔΣ) ADCs. In addition to providing anti-alias filtering, CT ΔΣ ADCs are typically well suited for high-resolution (12 - 14 bits) and wide bandwidth (10 - 25 MHz) applications like WiMAX and WLAN. As in the case of

any circuitry for portable wireless devices, the power consumption of the delta sigma ADC needs to be very low (≈ 20 mW).

A very popular continuous time delta sigma (CT ΔΣ) ADC architecture is the feed forward architecture [3]. Further, a secondary feedback DAC path *(fast path)* is incorporated in one of the common implementations of the CT ΔΣ ADC. This path needs to be very fast, making the design of a summing amplifier extremely critical [2]. Conventional summing amplifiers consume a very high power to meet this high GBW requirement. For example, the power consumption of the summing amplifier design given in [2] is 10mW!

In this work, these issues with the summing amplifier are addressed. A novel method of performing the summing operation in current-mode is introduced. This is followed by a 3-bit current-mode quantizer, designed in IBM 90nm process, which maps the information in current domain to digital domain. The method used here offers considerable power savings compared to conventional summing amplifier based architectures. The proposed solution is then characterized across process and temperature.

1.2. Organization of the thesis

The organization of the thesis is presented in this sub-section. Section 2 starts with the fundamental principles of analog-to-digital conversion. The concepts of oversampling and noise shaping are discussed and an introduction to delta sigma ADCs is provided.

Section 3 discusses the various types of quantizer architectures available and explains in detail two versions of the flash architecture. Then, various static and dynamic performance measures of the ADC are presented. The section concludes with some of the state-of-the art quantizer designs reported in literature.

Section 4 presents the motivation for the current work and proposes the principle of current-mode summing and quantization. The circuit level description and design of each individual block of the proposed current-mode summing stage and 3-bit current-mode flash ADC is provided. The overall operation of the quantizer is also presented.

Results of various simulations and characterizations of the designed current-mode quantizer are given in Section 5. Various simulations including INL, DNL, overdrive recovery test, comparator delay and dynamic characterizations like SNR and jitter analyses are provided. A summary of the thesis is presented in Section 6.

2. DELTA SIGMA ANALOG-TO-DIGITAL CONVERTERS

In this section, an introduction to the process of sampling and quantization, which is fundamental to analog-to-digital conversion, is provided. Then, the advantages of oversampling and noise shaping are presented. A delta sigma modulator, which is an oversampled ADC, is introduced and a comparison is made between two variants available in them.

2.1 Introduction to analog-to-digital conversion [4]

Real world signals like temperature, pressure, sound and electromagnetic waves are analog in nature, that is, their amplitudes have a continuous variation with respect to a continuous increase in time. But digital signals, which are binary in nature, are more robust to noise and easier for signal processing. With progress in semiconductor manufacturing technology, the cost and power consumption of signal processing in the digital domain keeps going down. By definition, digital signals take up discrete values of amplitude at discrete time instances only. Thus, analog signals are continuous time, continuous amplitude signals while digital ones are discrete time, discrete amplitude signals.

The block that acts as the interface between these two domains is the analog-to-digital converter (ADC). As discussed in Section 1.1, in a RF receiver chain, the ADC comes at the end of the chain, just before the digital signal processor (DSP). Figure 3 shows a typical signal processing chain which performs analog-to-digital conversion.

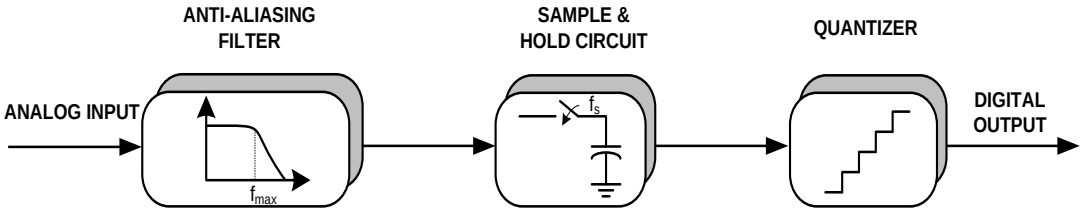


Figure 3 Signal processing chain – analog-to-digital conversion

Let us assume that the analog input has frequency components up to f_{max} (i.e., the bandwidth of the input analog signal is f_{max}). The operation of time discretization or *sampling* is carried by a sample and hold block, which samples the input signal at a frequency of f_s, satisfying the equation,

$$f_s \geq f_{max} \tag{2.1}$$

Called the *Nyquist-Shannon Sampling Theorem*, the above condition (2.1) is a fundamental result in information theory, which states that as long as the sampling frequency is at least twice the maximum frequency component present in the input, the original input signal can be recovered from the sampled version without any loss of information. However, it should be noted that high frequency components present above f_{max}, can be translated down to lower frequencies, by a process called *aliasing*. In other words aliasing is the same as *mixing* between f_s and the frequency components above f_{max}. This corrupts the sampled signal by *aliasing* out-of-band signals back to in-band. To overcome this effect, an *anti-aliasing filter* (AAF) is used at the beginning of the signal processing chain to limit the bandwidth of the input analog signal to f_{max}.

The output of the sample and hold circuit is discrete-time in nature but still has a continuous amplitude variation. The conversion of the sampled signal from continuous

amplitude to discrete amplitude is called *quantization* and is achieved by the quantizer. But, because of the finite number of amplitude levels used for quantization, this process introduces an error called the *quantization error*.

If a full-scale voltage of $\pm V_{ref}$ is quantized using N bits (i.e., 2^N quantization levels), the step size of the quantizer (Δ) is given by [5]

$$\Delta = \frac{2\,V_{ref}}{2^N} \tag{2.2}$$

This is the smallest value to which the input can be quantized, alternatively called the resolution or least significant bit (LSB) of the quantizer. Each analog input is quantized to within $\pm\Delta/2$ of a quantization level. Thus, the quantization error, ε, lies in the range $(-\Delta/2, \Delta/2)$. This error is always deterministic as the actual value of the input signal at the sampling instant can be known and hence only a function of the signal.

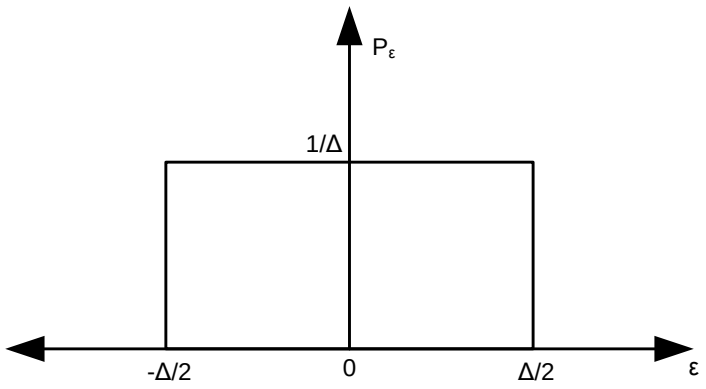


Figure 4 Probability density function of the quantization noise

But if the signal statistics is such that it is uniformly distributed, all the levels will assigned with equal probability. Then the quantization error can be assumed to be a

white noise process with a uniform probability density function [4] as shown in Figure 4. Under this assumption of uniform distribution of the quantization noise, for a ramp input signal, the noise power is given by the variance of the quantization error as follows

$$\sigma_\varepsilon{}^2 = \int_{\frac{-\Delta}{2}}^{\frac{\Delta}{2}} \epsilon^2 . \frac{1}{\Delta} \, d\varepsilon = \frac{\Delta^2}{12} \tag{2.3}$$

For a full-scale input to the quantizer, the signal power is$(V_{ref}{}^2/2)$. The signal to quantization noise ratio is calculated in dB as, [5]

$$\text{SQNR (dB)} = 6.02N + 1.76 \tag{2.4}$$

The above discussion forms the working principle of ADCs with sampling rate equal to twice the input signal bandwidth. Such ADCs are called *Nyquist rate ADCs*.

2.2 Oversampling

There are another set of ADCs, called *oversampling ADCs*, in which the sampling frequency used is many times higher than the Nyquist rate (2 * f_{max}). It should be noted that the quantization noise calculated by (2.3) is white in nature, implying it is constant over the two-sided signal band from $-f_s/2$ to $f_s/2$ (i.e., - f_{max} to f_{max}). The noise power spectral density of the quantization *'noise'* is as shown in Figure 5. When the same input signal is sampled at a higher rate than f_s and quantized, the amplitude of the noise power spectral density (PSD) is reduced while the bandwidth over which it is spread is increased by the same factor. The total integrated quantization noise power is thus maintained at the same value as before ($\frac{\Delta^2}{12}$).

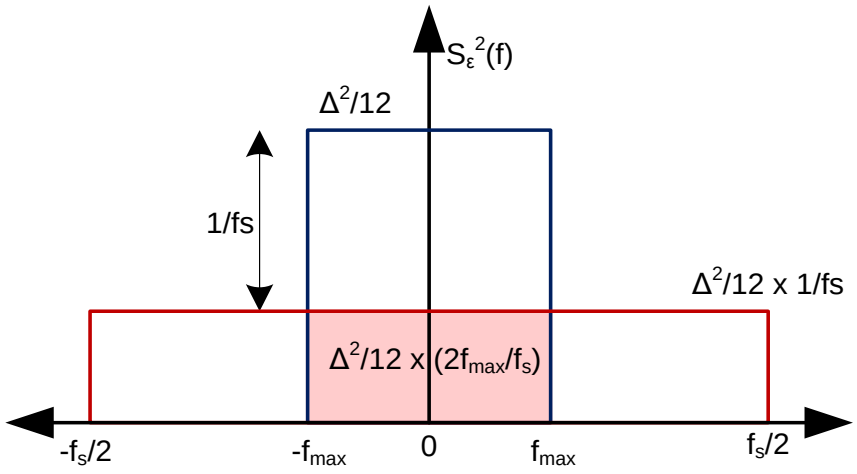


Figure 5 Oversampled quantization noise power spectral density

But the in-band noise is reduced by a factor equivalent to the *over-sampling ratio (OSR)*, defined as

$$\mathrm{OSR} = \frac{f_s}{2 \times f_{max}} \tag{2.5}$$

An improvement in SQNR is achieved as given by [5]

$$\mathrm{SQNR\ (dB)} = 6.02N + 1.76 + 10\log_{10}\mathrm{OSR} \tag{2.6}$$

In other words, an OSR factor of 2 reduces the in-band quantization noise by 3dB or results in an increase of 0.5 bits of resolution.

2.3 Noise shaping

Oversampling offers a great advantage in terms of increasing the SNR (resolution) without the obvious increase of the number of bits used for quantization. But the cost paid in turn is too high. For example, to achieve a 14-bit resolution using a 6-bit

converter over a bandwidth of 4MHz, the OSR required is 65,463 and hence the sampling frequency is 261.854 Gsamples/s! This is near impossible to implement.

Instead of just depending on oversampling to improve the SQNR, a way to further reduce the in-band noise would be to *shape* the quantization noise out of the signal band. ADCs which make use of this *noise shaping* to improve upon the advantages of oversampling are *delta sigma (ΔΣ) modulators.*

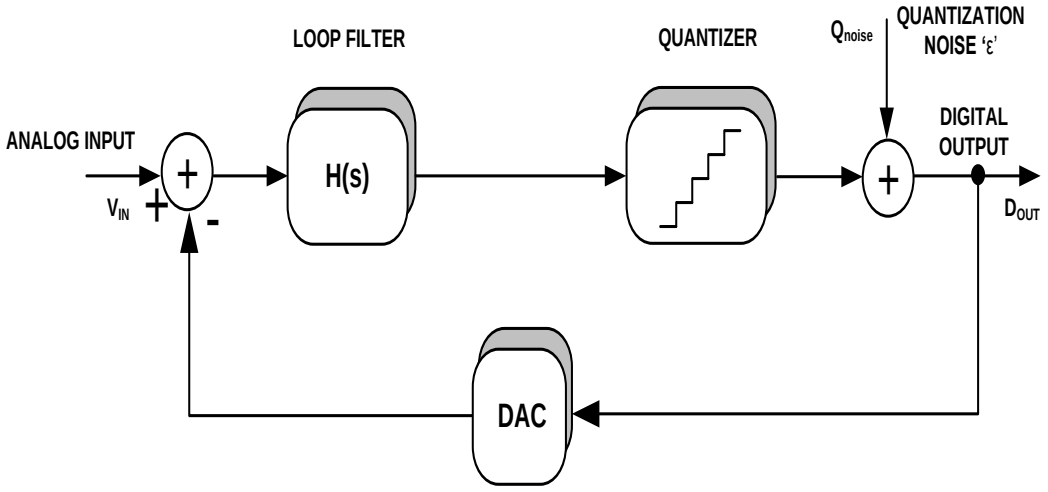


Figure 6 An ideal continuous time delta sigma modulator

In a delta sigma modulator, a continuous time version of which is shown in Figure 6, the noise shaping is done with the help of a loop-filter H(s). The quantizer is a low resolution one which performs the actual quantization, while the DAC feeds the analog equivalent of the quantized output back to the input. The ADC is termed low pass or band pass based on the transfer function of loop filter, H(s).

The quantization noise, Q_{noise}, is assumed to be white and uniformly distributed as discussed earlier in this section. The quantizer and DAC ideally perform complementary domain conversions, without altering the signal amplitude; hence a gain of unity (1) is assumed for them. A linear model based on these assumptions is shown in Figure 7.

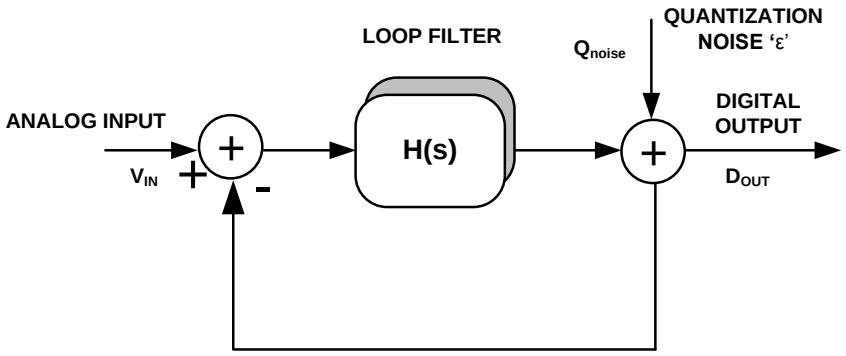


Figure 7 A linear model assuming unity gain for the quantizer-DAC combination

The functioning of the delta sigma loop becomes clear once we write up the signal transfer function (STF) and the noise transfer function (NTF), based on very basic feedback theory.

$$\mathrm{STF} = \frac{\mathrm{D_{OUT}}}{\mathrm{A_{IN}}} = \frac{\mathrm{H(s)}}{1 + \mathrm{H(s)}} \approx 1 \tag{2.7}$$

$$\mathrm{NTF} = \frac{\mathrm{D_{OUT}}}{\mathrm{Q_{noise}}} = \frac{1}{1 + \mathrm{H(s)}} \approx \frac{1}{\mathrm{H(s)}} \tag{2.8}$$

(The approximations are valid only if H(s) >> 1)

Thus, we see that as long as the in-band gain of H(s) is high, the in-band input signal has a gain 1, while the in-band noise is attenuated by the factor equal to gain of

the loop filter {H(s)}. Thus, the in-band quantization noise is suppressed and pushed out-of-band and hence, the digital output is a very good approximation of the analog input. However, it should be noted that, the total integrated noise power within $f_s/2$, remains the same as in the oversampling case ($\frac{\Delta^2}{12}$). A simple illustrative diagram for the STF and NTF is shown in Figure 8.

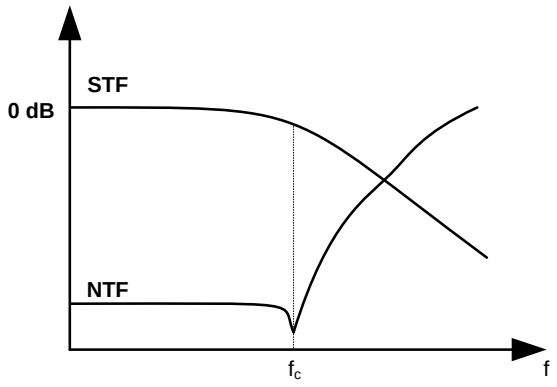


Figure 8 STF and NFT for a low pass delta sigma modulator

The modified expression for SQNR which includes the advantages of oversampling and noise shaping is given by the following equation [4]

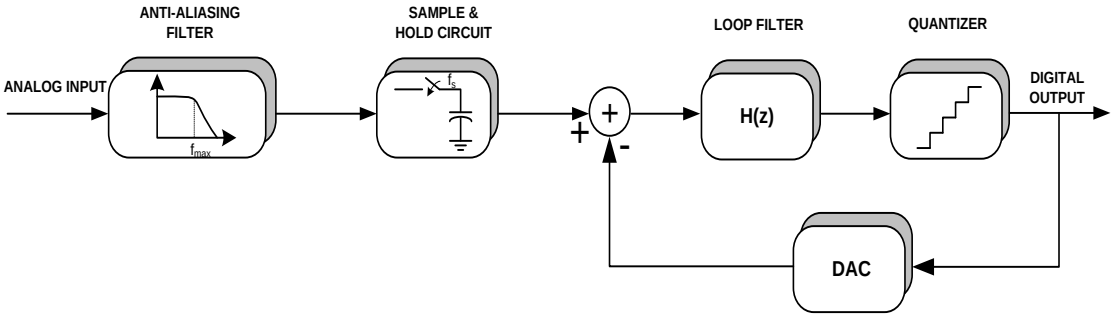
$$\text{SQNR (dB)} = 6.02\text{N} + 1.76 + (20\text{L} + 10)\log_{10}\text{OSR} - 10\log_{10}\frac{\pi^{2\text{L}}}{2\text{L}+1} \tag{2.9}$$

where N is the number of bits in the quantizer, L is the order of the low-pass loop filter (as well as the delta sigma modulator) and OSR is the oversampling ratio defined by equation (2.5). Thus, SQNR increases at the rate of (L+0.5) bits/octave of oversampling in the case of an L^{th} order delta sigma modulator. [4]

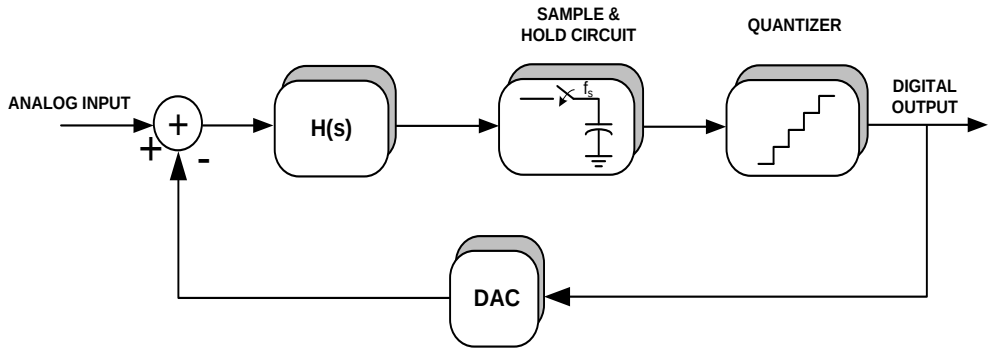
2.4 Discrete time vs. continuous time modulator

If the loop-filter discussed in the previous sub-section, is a discrete-time integrator, the modulator is called a discrete-time (DT) delta sigma (ΔΣ) modulator. This case, being a sampled data system, sampling happens at the input of the modulator using a sample and hold block as shown in Figure 9. The discrete-time integrators are realized using switched-capacitor techniques. These DT ΔΣ modulators are best suited for audio signal processing applications where the signal bandwidth is very low (< 20kHz). With an OSR of the order of 64 or more and using an inherently linear single bit quantizer/DAC, a resolution of 20 or more bits is obtained.

Amplifiers used in switched-capacitor circuits, needs to have a gain bandwidth (GBW) product (or unity gain frequency) of about 10 times the sampling frequency [4]. This is to ensure that the signals settle to the final value within a desired accuracy range, as soon as possible. Now, if we try extending this technique for wide-band applications like Wi-MAX (bandwidth ≥ 10MHz), even with a low OSR, the GBW requirement is very high. This translates to increase in the transconductance of the amplifier stages and hence an enormous increase in power consumption.



(a)



(b)

Figure 9 (a) Discrete-time (DT) and (b) continuous-time (CT) delta sigma modulator [3]

As shown in Figure 9, discrete-time structures require a sample and hold (S/H) block at the input to make the sampled data available for the DT. If this sampling operation is performed after the loop filter, then we have a continuous-time (CT) delta sigma modulator (ΔΣ). The prefix continuous-time is because of the nature of the loop-filter which process continuous time data and not sampled data. Hence, the requirements on settling time and bandwidth (GBW) are very much relaxed in this case. Wide-band applications require such ADC's which can provide a high resolution (> 12 bits) over a

high input bandwidth (> 20MHz). Thus, a low-pass continuous time delta sigma analog-to-digital converter (LP CT ΔΣ – ADC) is a very attractive solution for current and futuristic wireless multi-standard receivers, which have high resolution, high dynamic range and wide bandwidth requirements.

2.5 Conclusion

ADCs act as an interface between the real (analog) world and the digital world. Analog signals are converted into digital by the process of sampling and quantization. There is an error associated with quantization which is termed quantization noise. This quantization noise is a function of the number of levels used for quantization or the resolution. Oversampling helps in reducing the in-band quantization noise, by spreading it across a wide frequency range. Noise shaping conveniently pushes the quantization noise power from inside the bandwidth of interest to out-of-band. A delta sigma modulator combines the methods of oversampling and noise shaping, to make a low-resolution ADC (quantizer) perform like one with a higher resolution. Among the two flavors available, the continuous time solution suits applications where the bandwidth of the input signals extends up to several tens of megahertz.

3. INTRODUCTION TO QUANTIZERS

As discussed in the previous section, sampling and quantization form the fundamental principles for converting an analog signal into digital. The process of quantization involves mapping information from the continuous variations of the analog world into discrete levels. Due to the finite number of levels involved in this process of quantization, there is an inherent error called quantization error or quantization *noise*.

A widely used method to reduce this quantization noise is the use of delta sigma modulation. The fundamental components of the continuous time delta sigma modulator were discussed in Section 2. These include a loop filter which defines the transfer function for noise shaping, a quantizer (ADC) which converts the signal into a digital code and a feedback DAC which converts the digital word into an equivalent analog signal. The quantizer is fundamentally a low-resolution analog-to-digital converter. The resolution of the quantizer, when placed inside a delta sigma loop, is increased due to the principles of oversampling and noise shaping as seen in the previous section. Thus, while referring to a quantizer, we are in fact referring to an ADC, which is not stand alone but forms part of the delta sigma modulator loop.

3.1 Types of ADCs

Analog-to-digital converters (ADCs) can be classified into various types based on various criteria. Fundamentally, based on the sampling rate employed by the ADC, they can be divided into Nyquist rate and oversampling converters. Another way of

classification is based on the constraints that dictate the design of an ADC and the target application. Figure 10 shows the various ADC architectures [6] that are commonly employed and the mutual tradeoffs involved between power consumption, resolution and speed of operation.

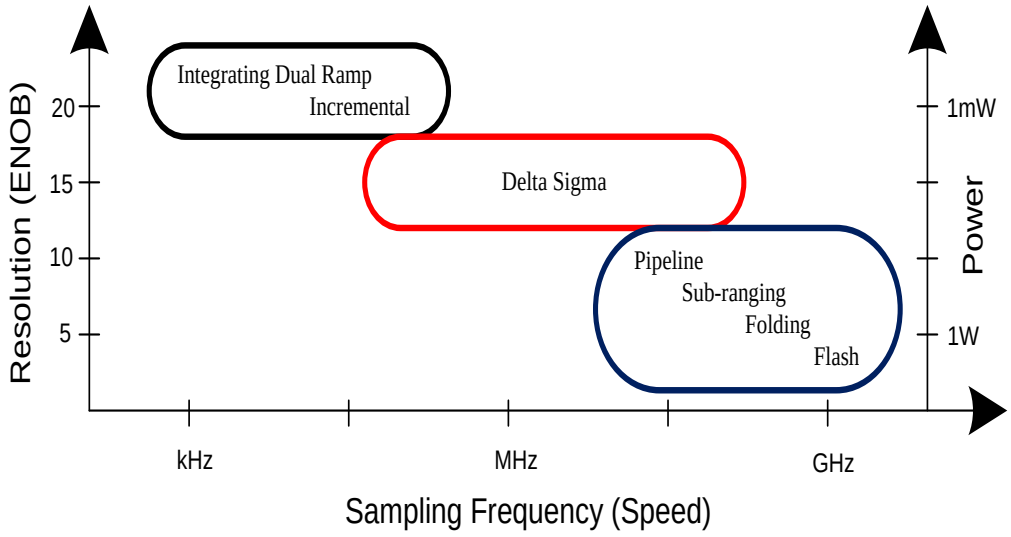


Figure 10 ADC architectures classified with respect to speed, power and resolution

For applications where the speed of conversion is of utmost importance, high speed ADC architectures are used (outlined in blue). Flash ADCs are the fastest but as will be discussed later, they are suited only for low resolution. The folding, sub-ranging (includes two-step) and pipeline ADCs fall under the category of high speed ADCs with low to medium resolution. Delta sigma ADCs can be classified under the category of medium to high speed ADCs with high resolution. For very low frequency and high

precision applications, integrating and incremental ADCs offer the highest resolution but at very slow rates of conversion.

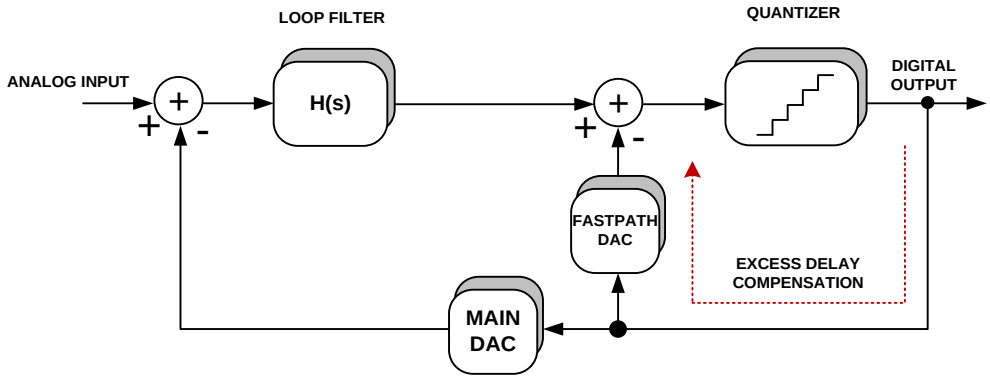


Figure 11 A CT ΔΣ modulator with excess loop delay compensation

The quantizer plays a very critical role in a delta sigma modulator. If the negative feedback loop is functional, then the error signal, which is the difference between the analog input and the feedback signal, is close to zero (very low).This implies that the quantizer acts in conjunction with the feedback DAC to produce a signal which is a replica of the input signal. Since the quantizer-DAC combination just performs conversion from one domain to another, the signal at the input of the quantizer is also equal to the analog input. Further, to compensate for excess loop delay, a *fast* feedback path is also incorporated [3]. The DAC used in this fast path injects a feedback signal at every clock edge as shown in Figure 11. Hence, the quantizer is required to quantize these signals within one clock cycle so that it can be fed back again. This means that an

architecture which is very fast should be chosen for the quantizer. Flash ADC [7] is a common quantizer architecture which offers high speed but low resolution.

3.2 Flash ADCs

Flash ADCs exploit the massive parallelism in their architectures and perform analog-to-digital conversion at the fastest speed possible. The results of the conversion are available at the end of one clock cycle, hence the name '*flash'*. There are two types of flash ADCs found in use – the traditional flash ADC which operates in voltage-mode and the relative newer – current-mode flash.

3.2.1 Voltage-mode flash

In conventional flash ADCs, the input signal is compared against a set of reference voltages. Figure 12 shows a generic N-bit flash ADC [8]. There are 2^N-1 equal size resistors making up a resistor ladder. This divides the full scale voltage V_{FS} into (2^N-1) set of reference voltages. The input voltage signal is compared with these reference voltages by 2^N-1 comparators. The comparators are generally high speed open-loop high gain op-amps. The outputs of the comparators together form a *thermometric code* representation of the input. An encoder converts this into binary representation. It should be noted that though this ADC architecture is the fastest, the number of comparators increase with increasing resolution, N. Also there is an increase in the power consumption and area. Hence, usually the design is limited to 3-8 bit resolutions. Note that in the Figure 12, $\Delta = \frac{V_{FS}}{2^N}$ is the least significant bit (LSB).

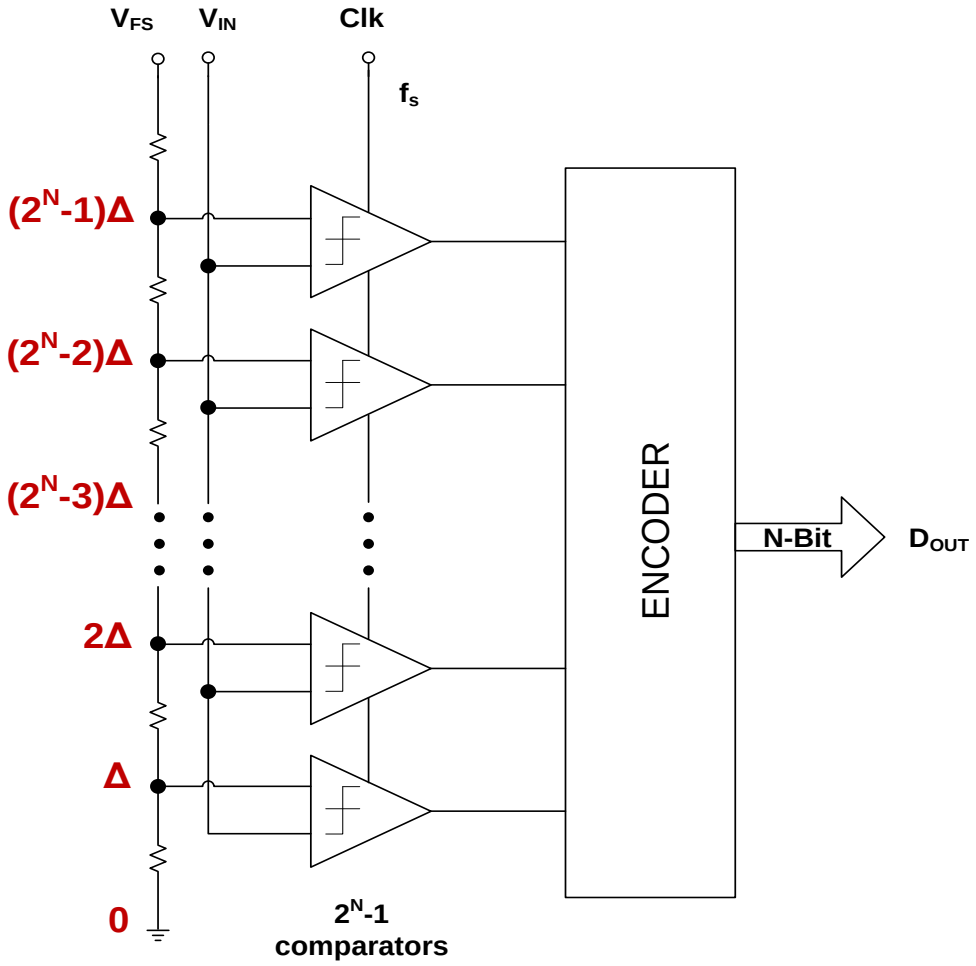


Figure 12 Voltage-mode flash ADC

3.2.2 Current-mode flash

Current comparators in the form of current-mode sense amplifiers are widely used in RAM memories [9], [10]. This principle of current-mode sense amplification was combined with the concept of FLASH to give rise to flash ADCs with current comparators as shown in Figure 13 [11].

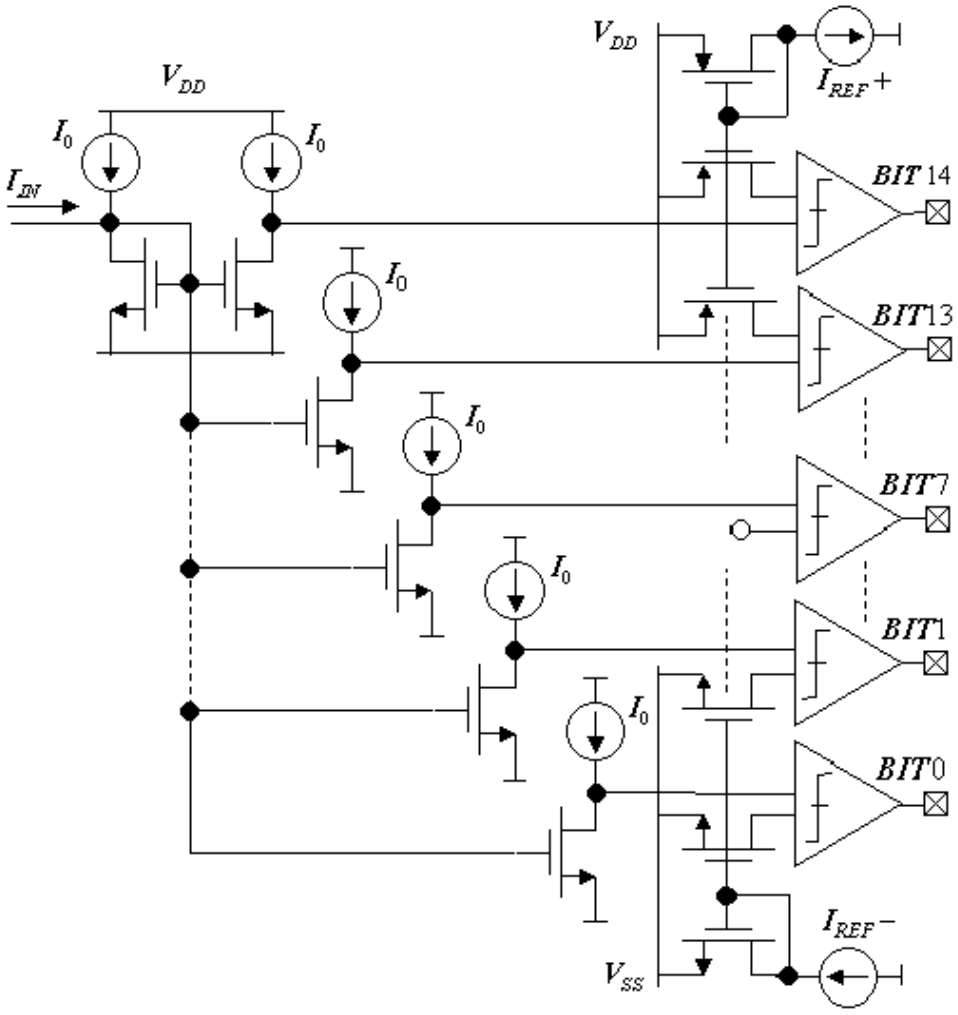


Figure 13 Current-mode flash ADC [11]

Instead of having a resistor ladder, there are $2^N - 2$ reference current sources realized using PMOS current mirrors for positive references and NMOS current mirrors negative references. The different reference current values are obtained by varying the (W/L) ratios of the current mirrors. The reference current for the level 2^N-1 is null. [11]

The input signal is copied and distributed to all the comparators using identical (1:1) current mirrors. There are 2^N-1 current comparators, which compares the input

current with the references. The mirror transistors should be well matched to make sure that the non-linearity due to mismatch is less than the quantization noise floor of the ADC.

The quantizer discussed in this thesis also uses a similar architecture where the input signal is mirrored and compared against current references. Section 4.4 elaborates this in detail.

3.3 Static characteristics [5]

There are some commonly used terminology and performance measures for an ADC. The transfer response of an ADC can be defined as the line joining the midpoints of the quantization intervals for each of the digital output words. But transitions are easier to measure than midpoint values and can be alternatively used for the definition of certain errors. The static characterization of the ADC is done with the aid of its input-output (transfer) response. *'Resolution'* of the ADC is the number of bits the ADC uses to represent the analog input. For example, if the number of levels used for the digital representation is 2^N, then the resolution is N bits. Note that resolution is not an indication of *accuracy* of the converter, but just refers to the number of output bits in it.

3.3.1 Gain and offset error

The deviation of the first transition level $V_{0\ldots01}$ from 0.5 LSB is defined as the *offset error* for the ADC. Similarly, g*ain error* is defined as the difference at full-scale between the ideal and actual transfer curves after the offset error has been reduced to

zero. As shown in Figure 14, the slope of the transfer curve with gain error is different from the ideal transfer curve.

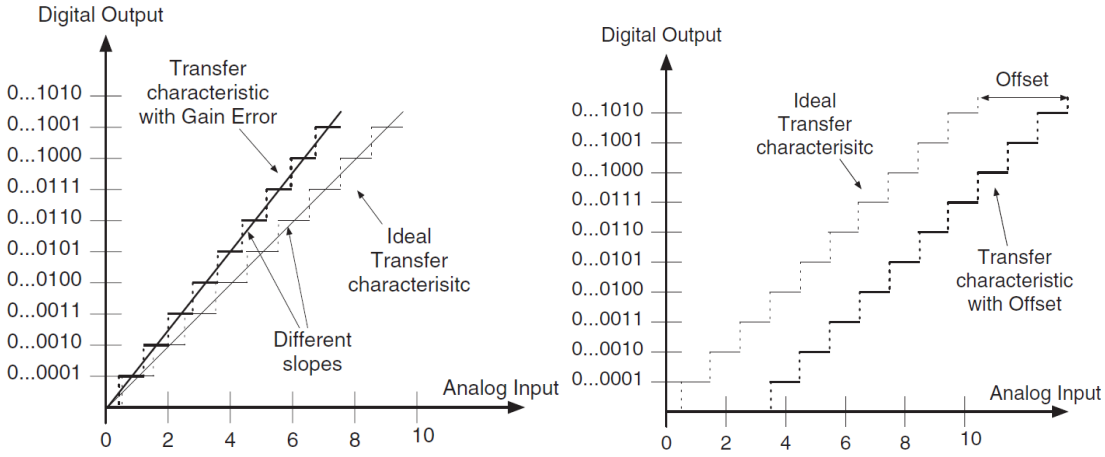


Figure 14 Gain and offset errors [12]

3.3.2 Accuracy

The *absolute accuracy* of a converter is defined as the difference between the actual and ideal transfer curves. Hence, absolute accuracy includes the offset, gain and non-linearity errors.

Relative accuracy is defined as the accuracy after the gain and offset errors have been removed. It is a measure of the non-linearity of the converter. Accuracy of an ADC is often mentioned in terms of the effective number of bits. For example, a 14-bit accuracy implies that the converter's error is less than ($\frac{V_{FS}}{2^{14}}$). Also, note that an ADC with 14-bit resolution may have just 10 bits of accuracy while a 10 bit ADC may have 14-bit

accuracy. An accuracy greater than the resolution implies the ADC's transfer function is very precisely controlled.

3.3.3 INL & DNL

Integral Non-Linearity (INL) is the deviation of the actual transfer curve from the straight line. There are two ways to draw the straight line – use the end points of the ADC transfer response or find a *best-fit* line such that the mean squared error is minimized.

In an ideal ADC, the transition values are precisely 1 LSB apart. The variation in the analog step size from 1 LSB is called *Differential Non-Linearity (DNL)*. Thus, for an ideal converter the DNL is 0, while ± 0.5 LSB is the maximum DNL that can be obtained.

Mathematical relationship for DNL and INL:

Let the transfer characteristics of the ADC be represented by $X(i),\ i = 0 \ldots (2^n-1)$. Then, DNL (in LSB) is the derivative of the ADC transfer curve, given by

$$\mathrm{DNL(i)} = \frac{\mathrm{X(i+1)} - \mathrm{X(i)} - \Delta}{\Delta} \quad ; \qquad (3.1)$$

$$\mathrm{i} = 0 \ldots (2^{\mathrm{n}} - 2)$$

where Δ is the ideal step size.

The end-point line method to calculate INL relates it to DNL with the following summing average relation given by,

$$INL(k) = \sum_{i=1}^{k} DNL(i) \tag{3.2}$$

A DNL error more than 1LSB or a maximum INL error greater than 0.5 LSB giving rise to *missing codes* in the ADC. Figure 15 shows the transfer curves of an ideal and a non-ideal 3-bit ADC. While DNL calculations are made for each code by comparing the actual code width with the ideal code width, the INL is calculated by as the difference between the midpoints of the ideal and actual transfer curves in LSBs.

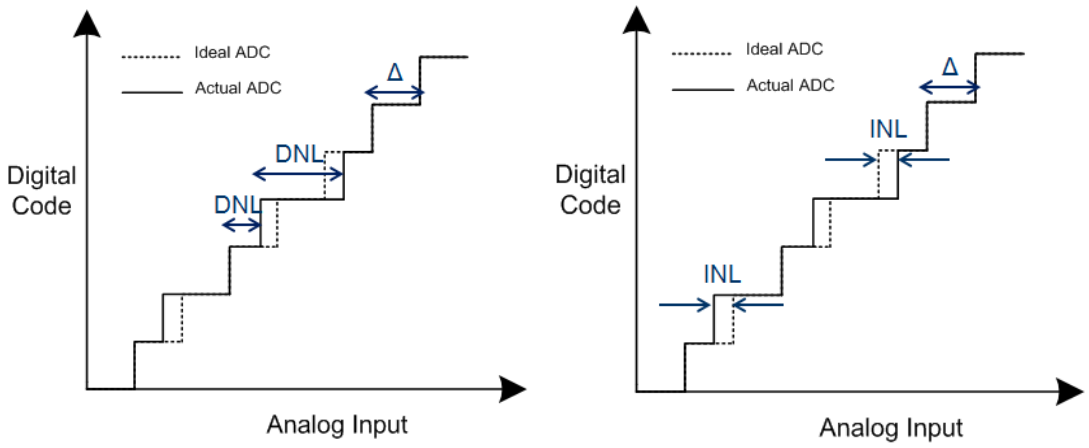


Figure 15 Transfer curve of a 3-bit A/D converter showing DNL and INL

3.4 Dynamic characteristics [12], [13]

The frequency response and speed of analog components in an ADC determines its dynamic performance.

3.4.1 SNR

The ratio between the power of the input signal and the total noise due to quantization and the noise of the circuit is defined as the signal-to-noise ratio (SNR). SNR includes all the noise sources within the Nyquist bandwidth. SNR is further subdivided into SQNR (signal-to-quantization noise ratio) given by equations 2.4, 2.5 or 2.6 as the case may be and SNR due to thermal noise of the circuit elements. It should be ensured that, by proper design, SQNR component dominates over the thermal noise.

3.4.2 SNDR

Signal-to-noise-and-distortion-ratio (SNDR) is similar to SNR but the non-linear distortion components are taken into account in addition to noise. The distortion components are calculated as the root of the sum of the squares of the individual harmonics. The variation of SNDR with input power is shown in Figure 16.

3.4.3 ENOB

Effective number of bits (ENOB) is the same as SNDR measured in bits.

$$ENOB = \frac{SNDR\ - 1.76}{6.02} \tag{3.3}$$

3.4.4 Dynamic range

It is the difference between the maximum possible signal input and the minimum possible signal input. The maximum value is limited by the non-linearity that sets in as the input amplitude increases. The minimum value is set by the noise floor.

3.4.5 SFDR

Spurious Free Dynamic Range (SFDR) is ratio of signal power to the power of the highest spurious spectral component. Measured in dB, SFDR is thus the difference in amplitude between the signal and highest spur. As the input power is increased, the SNDR first increases and reaches a maximum and then decreases because of distortion components/spurs. The range of input for which the SNDR is greater than zero is termed SFDR as shown in Figure 16.

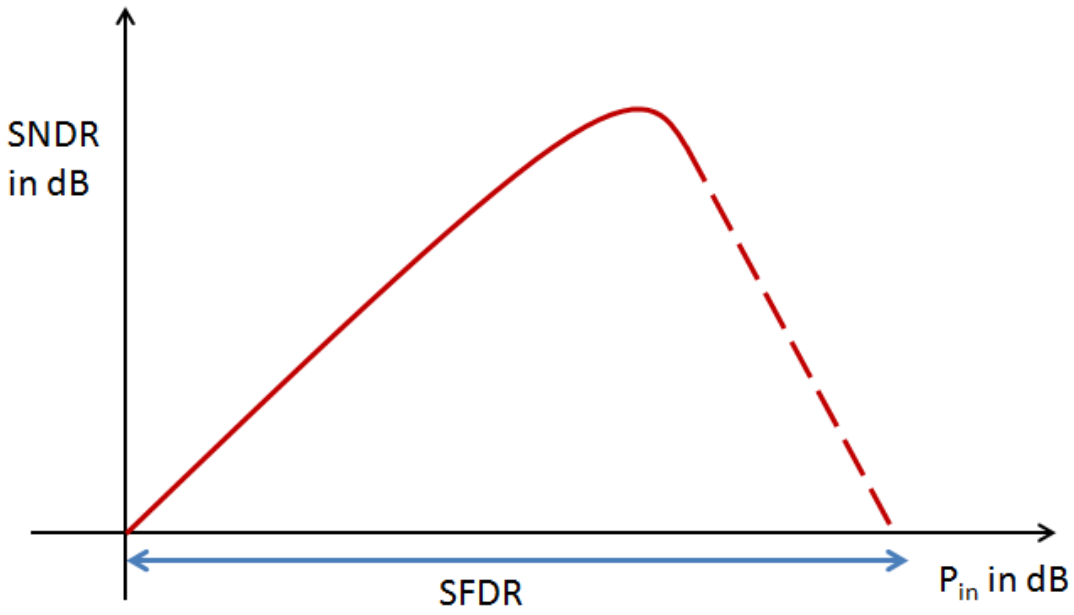


Figure 16 Definition of spurious free dynamic range (SFDR)

3.5 State-of-the-art solutions

Various quantizer architectures are being reported in recent times. A multi-phase voltage-controlled oscillator (VCO) based quantization approach is followed in [14].

When used within a CT ΔΣ modulator structure, it achieves an SNR/SNDR of 86/72 dB in 10MHz of input bandwidth with a clock rate of 950 MHz and 40mW power consumption in 0.13 μm CMOS. Figure 17 shows the conceptual representation of a VCO based quantizer. There is an inherent noise-shaping provided by this VCO based quantizer which reduces the phase noise and quantization noise in-band. The VCO is non-linear and hence, to improve the harmonic distortion performance, it is placed in ΔΣ loop.

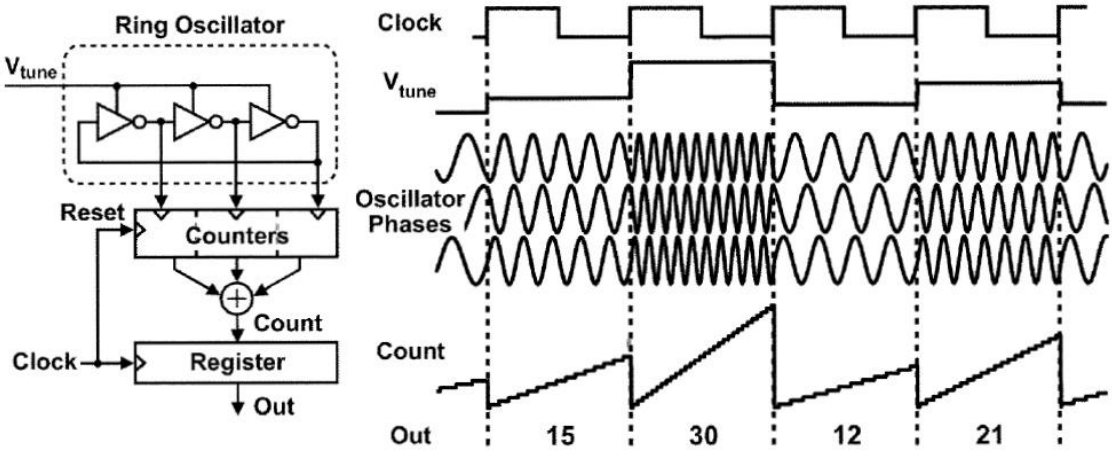


Figure 17 VCO based quantizer leveraging multi-phase oscillator [14]

The previous method can be called frequency domain quantization as the analog signal information is converted into frequency information before being quantized. An alternate method is to use a time domain quantizer as in [15].

The analog signal to be quantized is represented as a pulse-width modulated (PWM) signal and then a time-to-digital converter (TDC) is used to quantize the

information as shown in Figure 18. The TDC generates both the digital code as well as a "time-quantized" version of PWM pulse to be fed back to the input. A single-bit DAC which is inherently linear is sufficient for performing the feedback. The modulator, implemented in 65nm CMOS technology, achieves a 68 dB dynamic range in 20 MHz bandwidth.

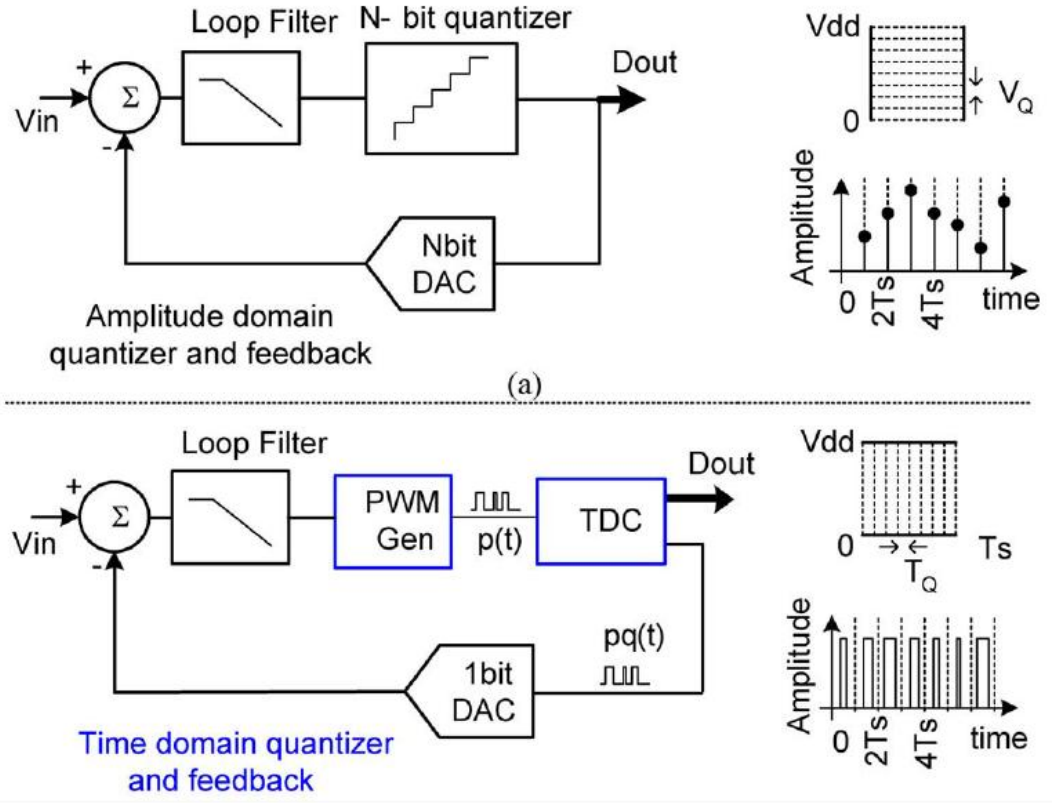


Figure 18 (a) Conventional multi-bit and (b) time domain quantizer/DAC based ΔΣ modulators [15]

A four-bit conventional flash ADC, which acts as the quantizer in a 20-mW 600-MHz continuous-time delta sigma (CT ΔΣ) modulator, is presented in [7]. The ΔΣ ADC has a 12-bit ENOB with 20 MHz signal bandwidth and 80-dB dynamic range. A 3-bit

two step quantizer embedded in a 5th-order continuous-time delta sigma (CT ΔΣ) modulator, which provides a 67.8dB SNDR over a 25MHz signal bandwidth, is proposed in [16]. The quantizer is a conventional two-step flash ADC making use of the output bits from two low-resolution ADCs, which when combined gives higher resolution while reducing the number of comparators.

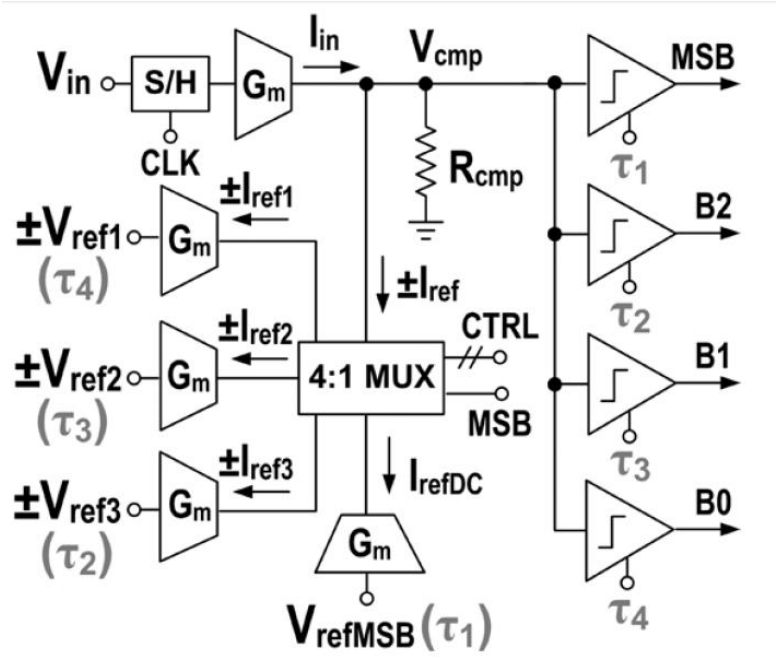


Figure 19 Two step 3-bit quantizer – single ended equivalent block diagram [16]

The flash topology has been combined with a successive approximation technique in an efficient manner as shown in Figure 19. The MSB is available at the end of the first step and then the three LSBs are determined in a successive algorithmic manner. The input and reference signals are converted into currents by a transconductance stage and the comparison is done in current-mode. The present work

extends this idea and makes use of the signal information in the current domain to do the summing and quantization as explained in the following section.

3.6 Conclusion

Among the various quantizer architectures available, flash ADCs are highly suited as quantizers for delta sigma modulators. There are two variants of flash ADC (quantizer) - the voltage mode flash and the current mode flash. The quantizer is characterized in terms of various static and dynamic characterization measures. Various state-of-the art solutions for quantizers include VCO-based quantization, time-domain quantization and two-step flash architecture.

4. DESIGN OF CURRENT MODE QUANTIZER WITH CURRENT SUMMING

This section first describes the issues with conventional voltage-domain summing amplifiers used in continuous time delta sigma modulators. Then, the novel idea of current mode summing and quantization is presented. The overall architecture and design specifications of the quantizer are discussed. Finally, the circuit level details of each individual block of the quantizer are presented.

4.1. Issues with conventional summing amplifiers

In continuous-time delta sigma (CT ΔΣ) modulators, the excess loop delay needs to be compensated by means of a secondary feedback DAC path [17]. The summing amplifier provides a direct path to the quantizer input for feeding the signal back from a second DAC (*fast-path* DAC).

Further, in a feed forward architecture, weighted addition of the outputs of various integrators of the loop filter needs to be done using a summing amplifier as shown in Figure 20. The summing amplifier is also required for the injection of test tones into the ADC which is needed for digital calibration. All these make the summing amplifier a critical component in the design of a CT ΔΣ modulator.

The *fast path* used to combat the excess loop delay introduced by the parasitic poles of the integrators in the loop filter should not add any additional delay i.e., it should be *very fast*. Thus, the unity gain-bandwidth (UGB) of the summing amplifier should be higher than the sampling frequency, by at least five to six times as a rule of

thumb. To meet this requirement, the transconductance of the summing amplifier should be increased, resulting in increased power consumption. Also, because of parasitic poles, which can cause stability issues in the fast path, the design of the summing amplifier stage is non-trivial. [2]

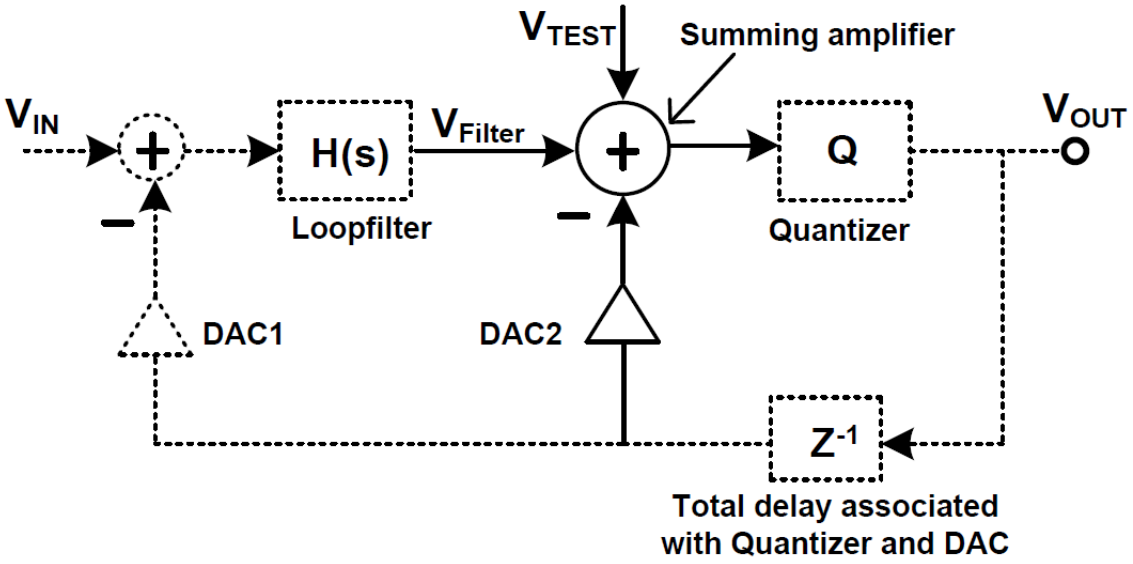


Figure 20 Block diagram showing the summing node in the CT ΔΣ modulator [2]

4.2. Current-mode summing and quantization

A conceptual diagram of a single ended summing amplifier is shown in Figure 21. The voltages v_A, v_B, v_C … are the node voltages at the output of the integrators in the loop filter. The resistors R_A, R_B, R_C … are determined by the feed-forward coefficients of the delta sigma loop. If the op-amp is ideal, the node v_X is a virtual ground and the input impedance of the op-amp is infinite. Consequently, the currents i_A, i_B, i_C … are added up at node v_X and the total current i_T flows through the feedback resistor R_F.

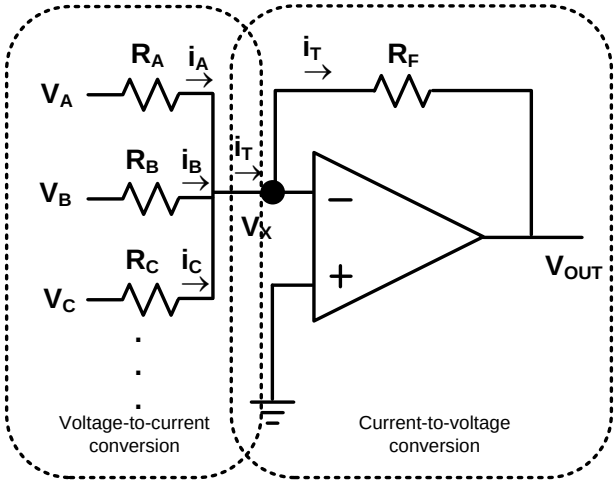


Figure 21 Single-ended summing amplifier

The output voltage v_{out} is then,

$$v_{out} = -R_F i_T \tag{4.1}$$

where

$$i_T = i_A + i_B + i_C + \ldots \tag{4.2}$$

and

$$i_A = \frac{v_A}{R_A}; \qquad i_A = \frac{v_B}{R_B}; \qquad i_A = \frac{v_C}{R_C}; \qquad \ldots \tag{4.3}$$

Thus, the output of the summing amplifier is given as

$$v_{out} = -\left(\frac{R_F}{R_A}v_A + \frac{R_F}{R_B}v_B + \frac{R_F}{R_C}v_C + \ldots\right) \tag{4.4}$$

We see that the resistors act as a voltage-to-current converter, while the op-amp with the feedback resistor (R_F) acts as a current-to-voltage converter. Thus, the op-amp primarily aids the conversion of the input signal from current domain to voltage domain.

The *power hungry* op-amp can be eliminated if the signal available in current domain can be utilized for further processing and quantization. In this work, the individual currents add up at a low impedance node and are passed on to the latter stages which process this current information. The total input current i_T, given by (4.2), enters the current summing stage, which offers a low input impedance and has a current gain of 1. This is conceptually shown in Figure 22. The output current, which is also i_T, is then mirrored using a set of current mirrors and compared with a set of current references. This '*current mirror - current reference'* combination forms the core of the current mode quantizer as discussed in Section 3.2.2.

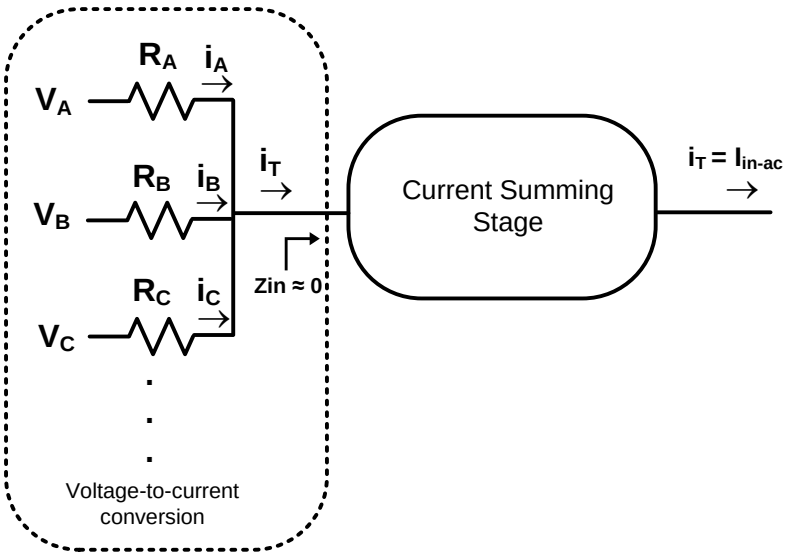


Figure 22 Conceptual single-ended current summing

The overall architecture is shown in Figure 23. The current mode quantizer adopts a flash architecture [11], which is the fastest among various available quantizer

architectures. In a conventional voltage mode flash architecture, the continuous time analog input is compared with a set of reference voltages. Typically, the references are obtained by a resister ladder while the actual comparison is done by comparators – (high-speed op-amps operating in open loop). An N-bit flash quantizer (ADC) requires $2^N - 1$ voltage comparators as discussed in Section 3.2.1.

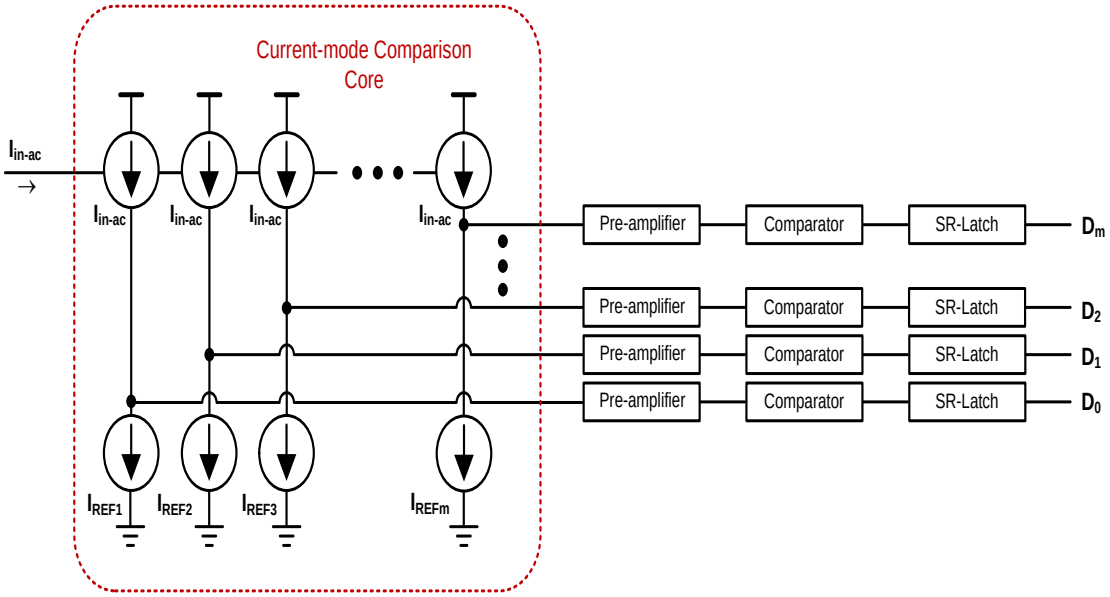


Figure 23 Overall architecture of the current-mode quantizer

In the present work, the comparison is done in current mode with the help of current mirrors. The input current, added up at the low impedance node provided by the current summing stage, is mirrored by a set of m (= $2^N - 1$) current mirrors. The currents in the $2^N - 1$ branches are then compared with current references.

The difference between the AC input current and the reference current is integrated on the parasitic capacitor at each current comparison node. The resulting

voltage is amplified using a conventional *preamplifier* followed by a *comparator*. The actual process of sampling happens at this comparator stage. The output of the comparator is held for an entire clock period by using an *SR-latch* which acts as the last stage in this chain. The outputs of all the $2^N - 1$ latches is the digital (thermometric) code corresponding to the analog input signal.

4.3 Quantizer specifications

This work presents the design of a 3-bit quantizer to be used in a 5-th order continuous time delta sigma (CT ΔΣ) modulator loop. The bandwidth of interest is 20MHz. The sampling frequency is chosen to be 500MHz so that the oversampling ratio (OSR) is 12.5.

The current-mode quantizer is designed to be equivalent to a conventional voltage-mode quantizer whose full-scale differential input voltage equals ±400mV. Note that the conventional voltage-mode quantizer is preceded by a voltage-mode summing amplifier. Initial system level simulations for the entire delta sigma ADC were done assuming that the summing amplifier has feedback resistance of 10kΩ.

The current mode quantizer replaces this summing amplifier and voltage mode quantizer. Thus, from equation (4.1),

$$v_{out} = -R_F i_T = 400\text{mV (single ended)}$$

$$\Rightarrow i_T = -40\mu\text{A, single ended (since, } R_F = 10\text{k }\Omega)$$

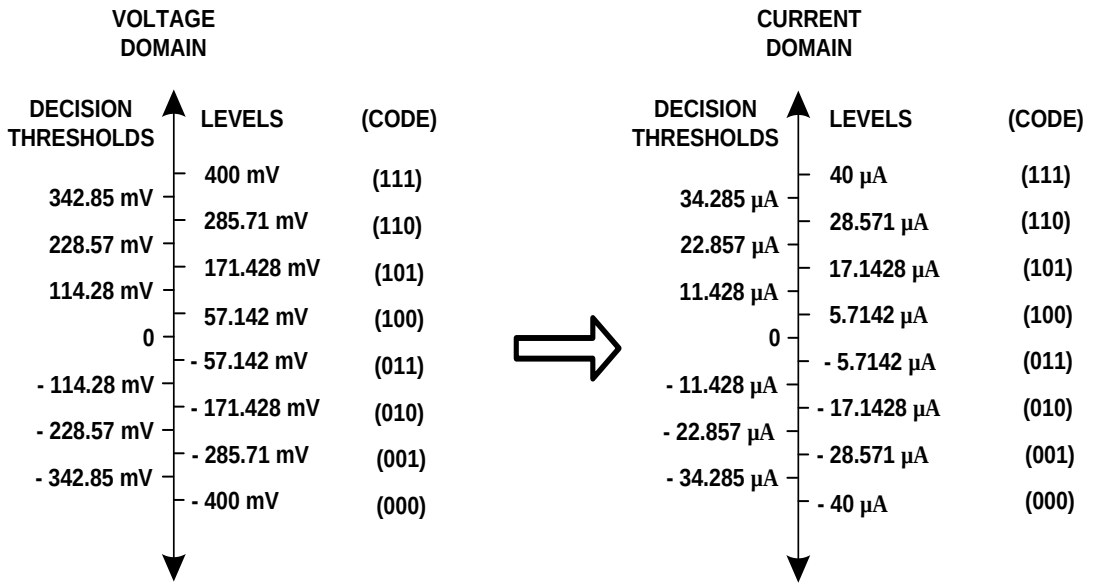


Figure 24 Voltage domain vs. current domain – equivalence of decision thresholds and levels of the conventional quantizer and the proposed current mode quantizer

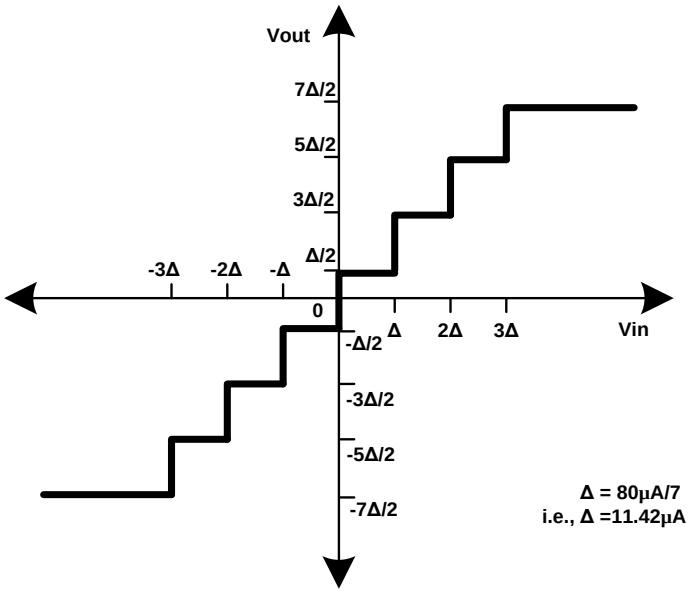


Figure 25 Transfer characteristics of the proposed quantizer

Hence, the full-scale differential input current for the current-mode quantizer is ±40μA. As the architecture for the quantizer is a thermometric-coded flash-based architecture, there are 7 decision thresholds for the 3-bit quantizer. Figure 24 shows the decision thresholds and levels associated with each region for both the voltage-mode quantizer and the equivalent current-mode quantizer. The transfer characteristics of the proposed quantizer indicate that it is a *mid-rise* quantizer as shown in Figure 25.

4.4. Circuit implementation of the current summing stage

A low impedance node can be implemented by making use of the source node of a MOS transistor. The inherent impedance looking into source is $1/g_m$, which can be designed to be low. To further reduce this impedance, we employ a *gain boosting* amplifier in feedback as shown in Figure 26. The gain boosting amplifier (A) forms a negative feedback loop around the common gate (CG) transistors M_{C1} and reduces the impedance by a factor equal to the 'gain' of the amplifier. If the gain offered by the amplifier is A, then the effective impedance looking into the input node of the current summing stage is given by

$$Z_{in} \approx \frac{1}{g_m(A+1)} \tag{4.5}$$

The actual impedance required is calculated based on the total impedance offered by the input resistors. From Table1, the net resistance is found out to be 847.5Ω. If 95% of the current has to enter the current summing stage, then the impedance should be less than 50Ω. We should bear in mind the fact that the fast path signal (current pulses) is injected at every clock edge i.e., at the rate of 500MHz. So, the input impedance should

be low (≈50Ω) up to 500MHz. This implies that the gain boosting amplifier should primarily be a wide-band amplifier.

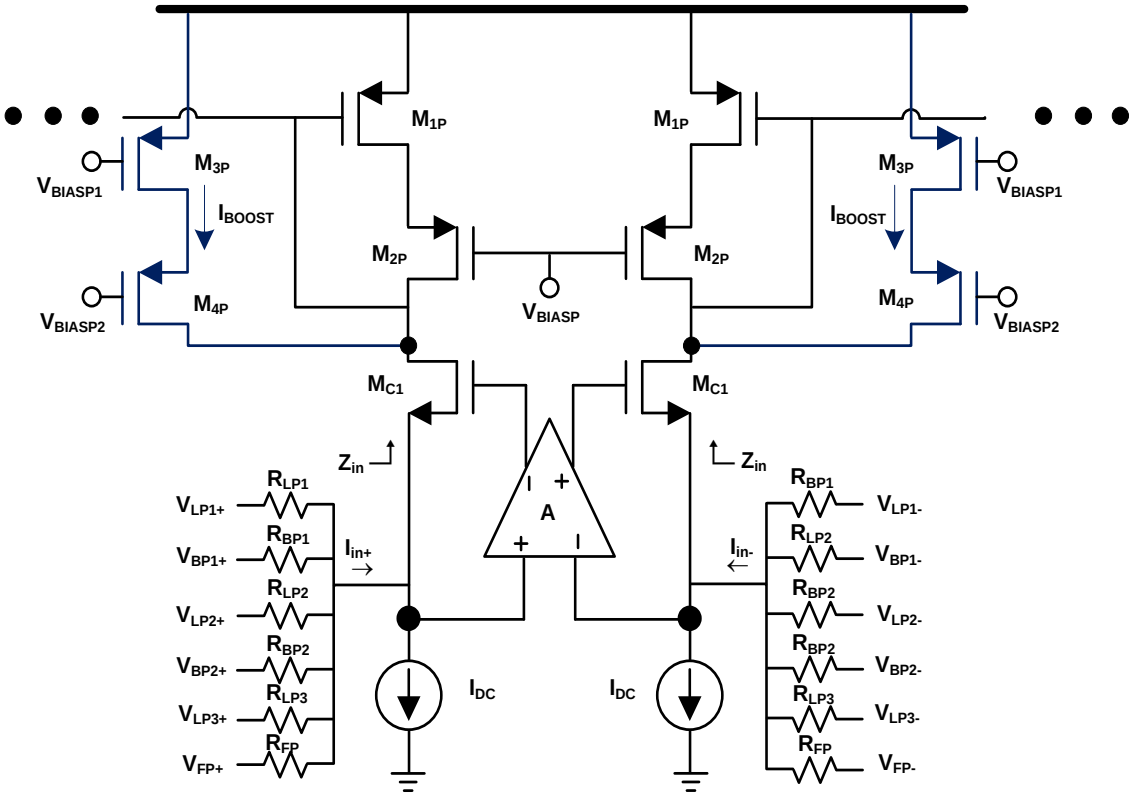


Figure 26 Input current summing stage

Table 1 Values of resistors used at the input of the summing stage

Device	Dimensions/Value	Device	Dimensions/Value
R_{LP1}	5.9099364kΩ	R_{BP1}	6.865602kΩ
R_{LP2}	2.02652365kΩ	R_{BP2}	9.93440011kΩ
R_{LP3}	6.75425533kΩ	R_{FP}	5.507584kΩ

To have a low input impedance, the common gate transistors M_{C1} should also have a high g_m. This can be achieved by increasing both its dimensions (W/L) and the drain current (Ids). The transistors M_{3P} and M_{4P} serve to pump in additional current (I_{BOOST}) into the cascode transistors M_{C1}, increasing the g_m of M_{C1}. The DC current source I_{DC} is 200µA. The dimensions of the transistors are tabulated below in Table 2.

Table 2 Transistor dimensions, device values and bias currents for the current summing stage in Figure 26

Device	**Dimensions/Value**	**Device**	**Dimensions/Value**
M_{C1}	12 x 2µm/250nm	M_{3P}	7 x 2µm/100nm
M_{4P}	4 x 2µm/100nm	I_{BOOST}	80 µA

4.4.1. Gain boosting amplifier

The gain boosting amplifier consists of a simple differential pair formed by transistors M_{1N}. To increase the bandwidth without compromising on the gain, the g_m of the differential pair has to be increased. This is done by pumping in additional current through the I_{BOOST} branch. The cascode device M_{2N} decouples the input and output node so as to reduce the capacitance in the signal path (closed loop) and helps is achieving the maximum bandwidth achievable.

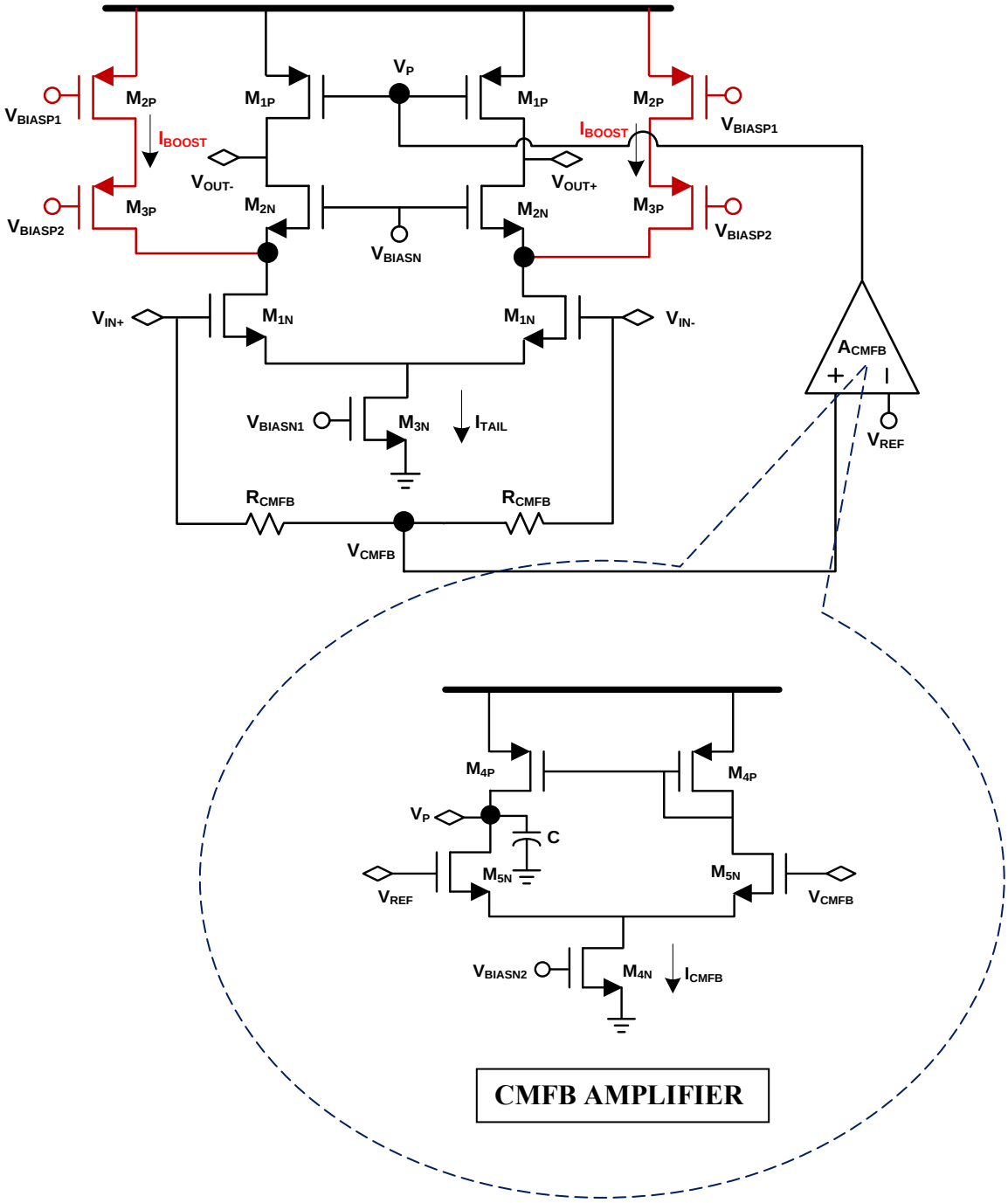


Figure 27 Gain boosting amplifier with CMFB loop

The tail current I_{TAIL} is 600 μA while I_{BOOST} is 180 μA on each branch. The transistors M_{2P} and $M_{3P,}$ used to supply the boosting current $I_{BOOST,}$ and the tail transistor M_{3N}, mirror current from a master bias current source. The master bias current source is used to bias all the current sources of the references.

The output of the integrators of the loop filter is at common mode level, which is at 600mV (V_{DD}/2). Thus, we need to maintain the common mode level at the input of the current summing stage also at 600mV in order to avoid the flow of any DC current through the set of input resistors. This is achieved with the help of a common-mode feedback (CMFB) loop around the gain boosting amplifier, as shown in Figure 27. The input node of the summing stage and the input of the gain boosting amplifier is the same. The voltage at this node is sensed by a pair of resistors and this common-mode voltage is controlled by a CMFB amplifier. The CMFB amplifier is a simple differential amplifier, the output of which controls the bias voltage (V_P) for the PMOS load M_{1P}. This in turn sets the output common-mode voltage of the gain-boosting amplifier, which is one V_{gs} above the common-mode voltage at the input of the current summing stage (or the gain-boosting amplifier).

$$\text{i.e., } V_{CM\_out\_Gain\_Boost} = V_{CM\_input\_GainBoost} + V_{gs\_Mc1,2} \tag{4.6}$$

It should be noted that there are two loops being formed – a gain-boosting loop and a CMFB loop. The transistors M_{1N}, M_{2N} and $M_{C1,2}$ form the gain-boosting loop while the transistors M_{5N}, M_{4P}, M_{1P}, and $M_{C1,2}$ form the CMFB loop. Thus, we see that the CMFB loop consists of two gain stages, one due to the differential pair M_{5N} and the other due to M_{1P} which acts like a common source amplifier inside the CMFB loop. The

two-stage amplifier formed in the CMFB loop is compensated with the help of the miller capacitor C at the node V_P. The dimensions of the transistors used in the design of the gain boosting and CMFB loops are given in Table 3.

Table 3 Transistor dimensions, device values and bias currents for the gain boosting amplifier and the CMFB loop in Figure 27

Device	**Dimensions/Value**	**Device**	**Dimensions/Value**
M_{1N}	18 x 2µm/250nm	M_{1P}	12 x 2µm/250nm
M_{2N}	9 x 1µm/100nm	M_{2P}	15 x 2µm/100nm
M_{3N}	30 x 1µm/200nm	M_{3P}	8 x 2µm/100nm
M_{4N}	1 x 1µm/200nm	M_{4P}	6 x 1µm/400nm
M_{5N}	2 x 2µm/400nm	C	300fF
I_{TAIL}	600 µA	R_{CMFB}	48 kΩ
I_{BOOST}	180 µA	I_{CMFB}	20 µA

The gain of the gain-boosting amplifier and the two-stage common mode feedback loop is given below

$$A_{Gain-boost} = g_{m1N}R_{out} \tag{4.7}$$

$$R_{out} = (1 + g_{m2N}r_{o2N})r_{o1N} \parallel r_{o1P} \tag{4.8}$$

$$A_{CMFB\_loop} = [g_{m5N}(r_{o5N} \parallel r_{o14P})].[g_{m1P}R_{out}] \tag{4.9}$$

The AC response of the gain boosting amplifier is shown in Figure 28, while that of the CMFB loop is shown in Figure 29. The results are tabulated in Table 4.

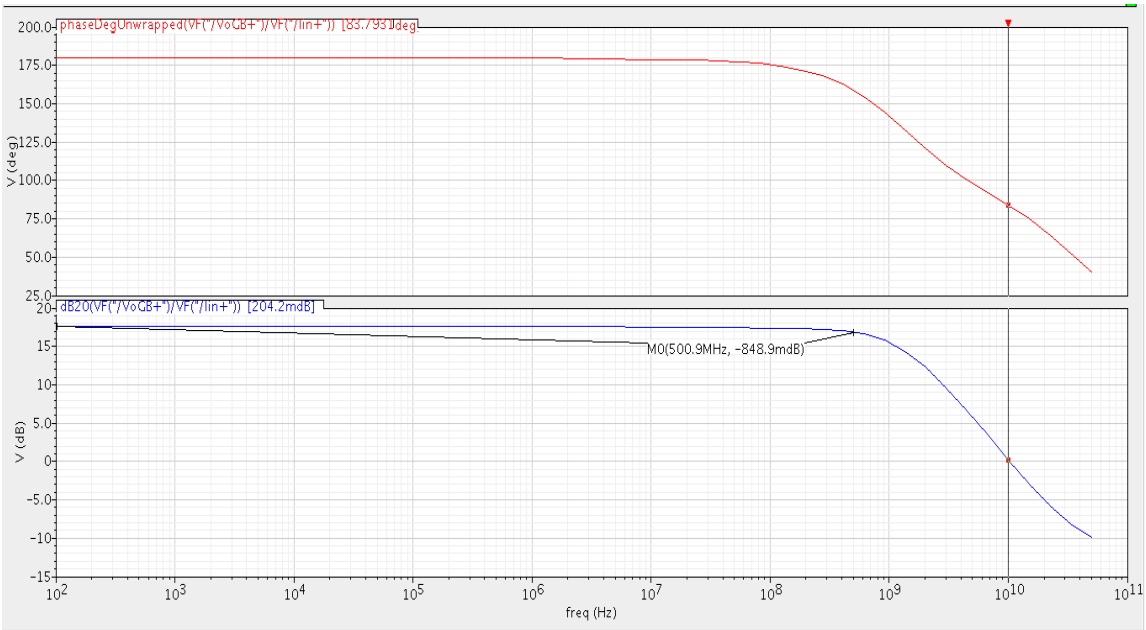


Figure 28 AC response of gain boosting loop - gain = 18dB, phase margin = 84^{o}, GBW = 1.01 GHz

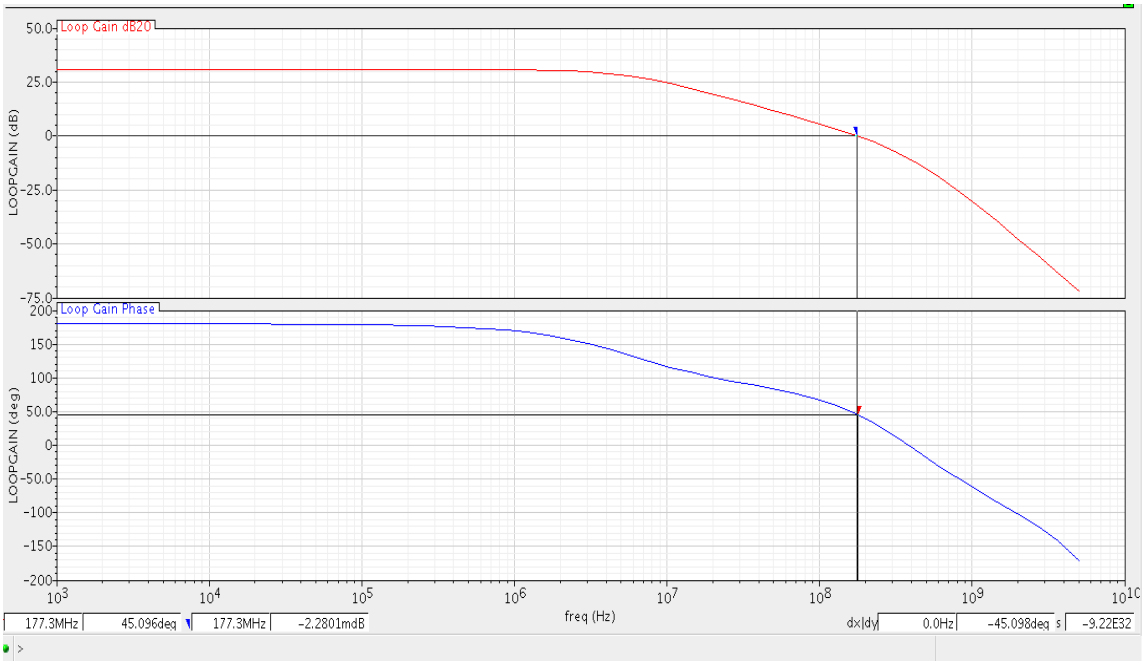


Figure 29 AC response of CMFB loop - gain = 31 dB, phase margin = 45^{o}, GBW = 177.6 MHz

Table 4 Parameters of the gain boosting loop and CMFB loop

Gain Boosting Loop		**CMFB Loop**	
Parameter	**Value**	**Parameter**	**Value**
Gain	18 dB	Gain	31 dB
Phase Margin	84^o	Phase Margin	45^o
GBW	1.01 GHz	GBW	177.6 MHz
Current consumption	600 μA	Current consumption	20 μA

From the above figures, we find that the gain boosting loop has a gain of around 18dB till 500 MHz. The GBW of the CMFB loop is pretty low but it is not an issue as the CMFB loop operates only for low frequencies and not at the rate of injection of fast path signals.

The input impedance of the current summing stage due to the gain-boosted cascode input is observed as a function of frequency as shown in Figure 30. It is seen that the input impedance at 500 MHz is 50Ω while for in-band input signal (20 MHz) the input impedance is 35Ω.

The gain boosting amplifier consumes 600μA while the CMFB amplifier consumes 20μA. The current consumed by the branches that support the input common gate transistors is 400μA (including the additional g_m boosting current). Thus, the total current consumption of the current summing stage is 1.02mA. The summing amplifier design carried out in 0.18μm in [2] consumes a total current of 5.6mA. That was mainly

because of the high GBW requirement of the op-amp used in the summing amplifier design. Thus, the proposed current summing stage consumes just 20% of the current consumption of conventional summing amplifier stage, offering huge power savings.

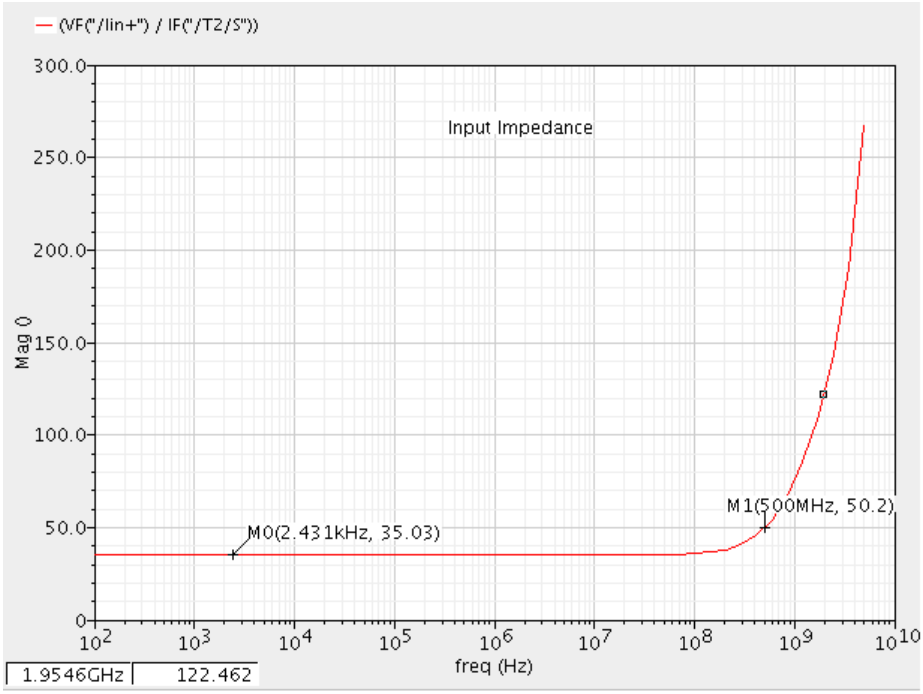


Figure 30 Input impedance of the current summing stage as a function of frequency

4.5. Current mode comparator – circuit implementation

This block forms the core of the current-mode quantizer. The input signal current which enters the current summing stage through the common gate transistors M_{C1}, is passed onto the next stage of the quantizer – the current mode comparator. The input signal is mirrored by using wide-swing cascode current mirrors [5] to several branches. Our present design is a 3-bit quantizer, which has 8 levels and seven decision regions

and the architecture is flash – hence the current is mirrored to seven branches. This input (AC) current is then compared with a set of reference current sources which carry currents from +3LSB to -3LSB.

The PMOS transistor M_{1P}, which mirrors the input current to seven branches, is critical in the design. Because of the flash nature of the quantizer, the mirroring ratio is 1:1. The frequency of pole formed at this mirroring node is given by

$$\omega_p = \frac{g_{m1P}}{8 \times C_{gsp}} \tag{4.10}$$

where C_{gsp} is the gate-source parasitic capacitance of each of the mirror PMOS transistor and g_{m1P} is the transconductance of the PMOS transistors.

Note that the maximum frequency of the input current is given by the rate of injection of the fast path signals which occurs at every clock edge (i.e.,) at 500 MHz. The quantizer should not introduce much delay in the loop formed by the quantizer and the *fast path* DAC. Hence, the poles should be at least 3 times the sampling frequency so that the quantizer does not introduce delay in the loop.

A DC current of 120μA is chosen to support a full scale current of 40μA (single ended) which is mirrored to each branch and to give transistor M_{1P} sufficient current to have a good g_m and hence high bandwidth. The input stage NMOS tail transistors thus carry a total DC current of 200μA each (including I_{BOOST} of 80μA). The total current carried by the NMOS current sources is $I_{DC} + I_{REF}$, where I_{REF} = (+3LSB,-3LSB). The mid-code current comparison cell compares the input signal with a reference current of 0A. The biasing current sources and reference current sources have a wide swing cascode current mirror structure [5]. The device dimensions for the various transistors

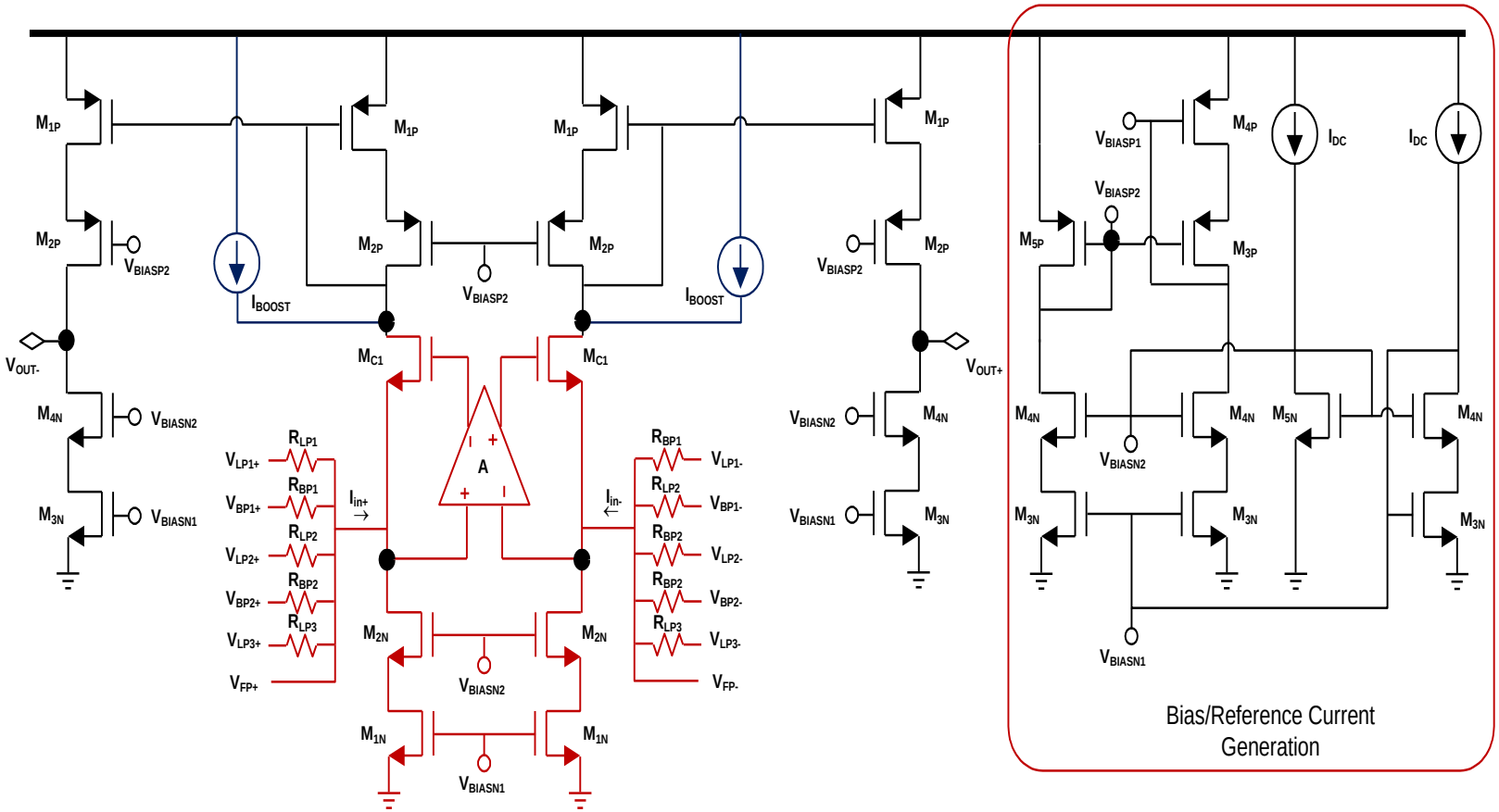


Figure 31 Current mode comparator (unit cell) with bias current sources

used in Figure 31 are shown in Table 5. The other parallel differential branches are also designed in a similar fashion.

Table 5 Transistor dimensions, device values and bias currents for the current mode comparator cell in Figure 31

Device	**Dimensions/Value**	**Device**	**Dimensions/Value**
M_{1N}	10 x 1µm/200nm	M_{1P}	15 x 2µm/160nm
M_{2N}	5 x 1µm/100nm	M_{2P}	5 x 2µm/100nm
M_{3N}	6 x 1µm/200nm	M_{3P}	5 x 2µm/100nm
M_{4N}	3 x 1µm/100nm	M_{4P}	10 x 2µm/100nm
M_{5N}	1 x 500nm/100nm	M_{5P}	1 x 2µm/100nm
I_{DC}	120 µA	I_{BOOST}	180 µA

The differential output nodes of the current comparator have a pair of reset switches. This resets the node to V_{CM} = 600mV at the beginning of every cycle. This resetting prevents the accumulation of offsets voltages due to mismatch in the current mirrors. The reset switch is designed to be a CMOS transmission gate as shown in Figure 32. The CMOS transmission gate is designed to have same PMOS and NMOS dimensions of (W/L) = (2µm/150nm). This selection makes the parasitic capacitances of the PMOS and NMOS to be same, and thereby help eliminate the effect of clock feed-through. The feed-through through from Clk is equal in magnitude but opposite in direction to that from Clk_b this cancelling the effect of each other. Figure 33 shows the

variation of the in resistance of the CMOS switch with input voltage as against equivalent NMOS only and PMOS only switches.

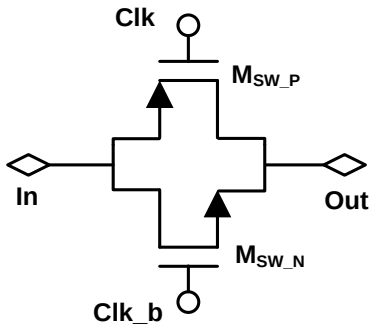


Figure 32 CMOS transmission gate used as reset switch

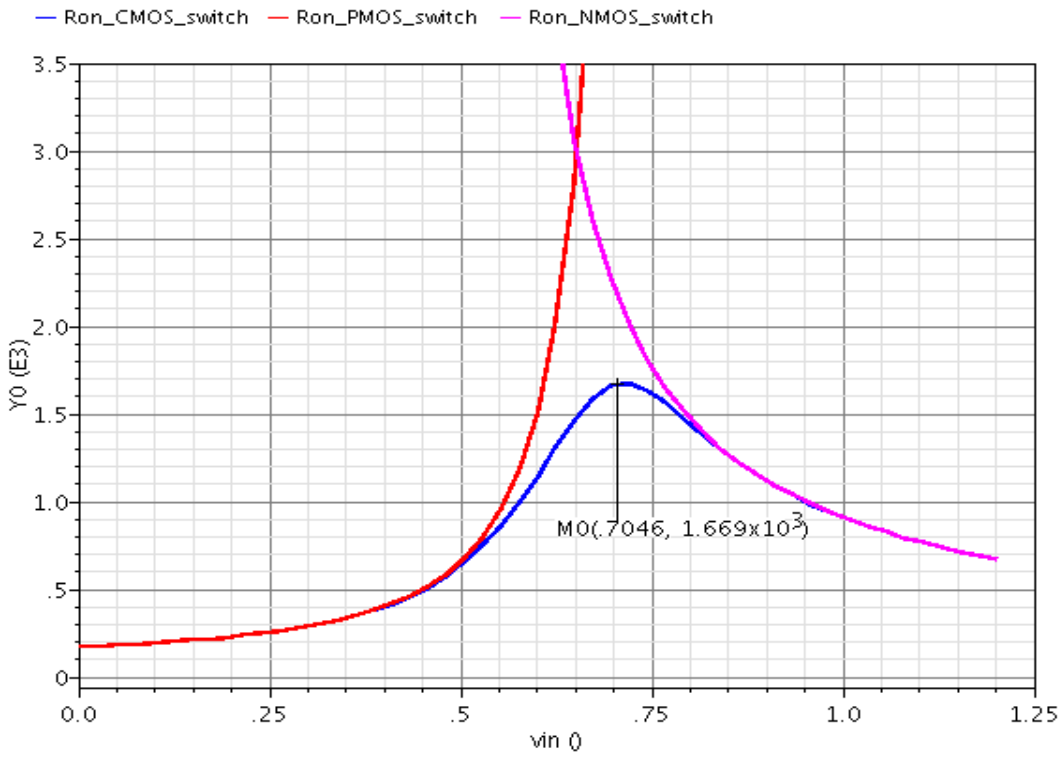


Figure 33 Variation of the on-resistance of PMOS only, NMOS only and CMOS transmission gate switch with the input voltage.

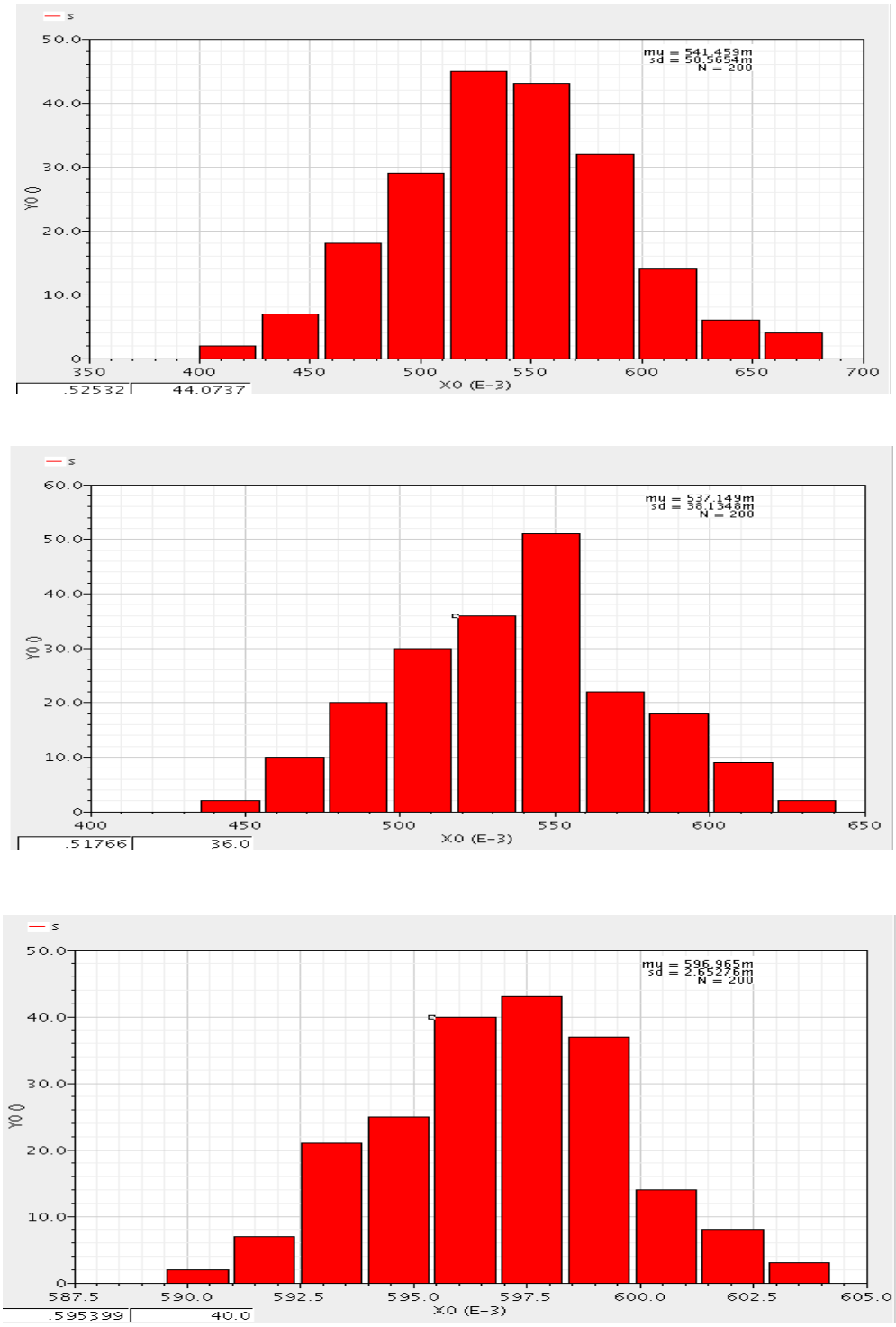


Figure 34 Variation of the voltage at the output node when (a) no resistor is used (b) 10kΩ resistor is used and (c) when 10kΩ resistor is used and the ends are connected to V_{CM} = 600mV. (200 runs of Monte-Carlo assuming 5% mismatch)

In addition to the reset switch, a pair of 10kΩ resistor loads is connected to the output node of the current comparator. The other end of the resistors is not grounded but connected to V_{CM}. This aids in maintaining the DC output voltage output nodes close to 600mV.

The variation of the DC voltage (common mode) at the output node, in the presence of 5% mismatch (no correlation was assumed between transistors), was observed by using 200 runs of Monte-Carlo Simulation. The results of the simulation are shown in Figure 34. The variation was observed for three different cases – (a) when the output node has just the reset switches and no resistive load, (b) when a 10kΩ resistive load is used at the output and (c) when a 10kΩ resistor is used with the ends tied to 600mV (V_{CM}). It is seen that the standard deviation for case (c) is just 2.65mV with a mean of about 597mV. Hence, it is advantageous to use a resistive load that fixes the DC voltage of the output node close to V_{CM}, in spite of device mismatch.

4.6. Design of preamplifier

The preamplifier offers to amplify the differential voltage that develops at output of the current comparator as a result of current-mode comparison. In addition to this primary use, preamplifier also serves as a buffer between the *"noisy"* comparator/latches the follows it and the clean analog stages preceding it. In this current work, the preamplifier, shortly called preamp, employs a structure similar to the one given in [18]. This is a simple differential pair with a modified load as shown in Figure 35.

In addition to contributing to the gain of this preamplifier, the resistors R_L help establish the common-mode output voltage. The input common mode required by the comparator, which follows the preamp, determines the output common mode voltage to be designed for.

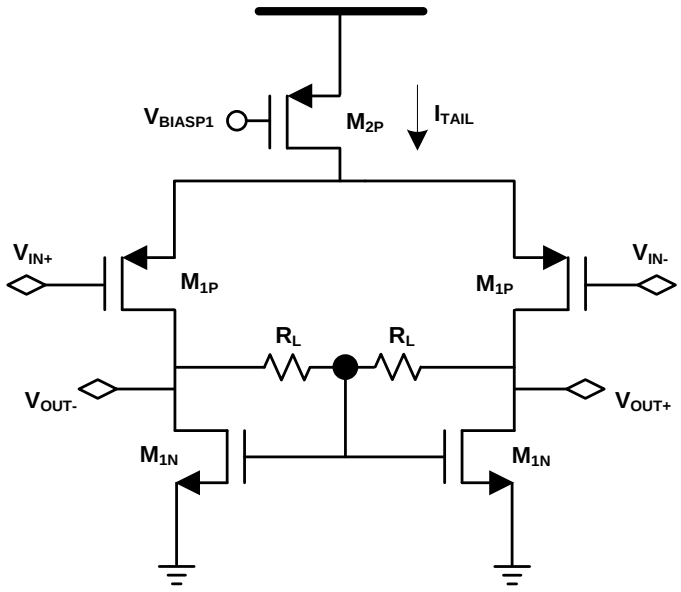


Figure 35 Self biasing fully differential pre-amplifier

The differential mode voltage gain is given by

$$A_{V_{DM}} = -g_{m1N}.(r_{o1P} \parallel r_{o1N} \parallel R_L)$$

$$\approx -g_{m1N}R_L \tag{4.11}$$

It should be kept in mind that we design this preamp to provide a nominal gain while make sure that the bandwidth is high compared to the sampling frequency (i.e., the

rate of injection of the fast path signal). The dimensions of the transistors used in the preamp design are given in Table 6.

Table 6 Transistor dimensions for the pre-amplifier shown in Figure 35

Device	**Dimensions/Value**
M_{1P}	8 x 2µm/150nm
M_{2P}	10 x 2µm/100nm
M_{1N}	1 x 500nm/100nm
R	5kΩ
I_{TAIL}	120µA

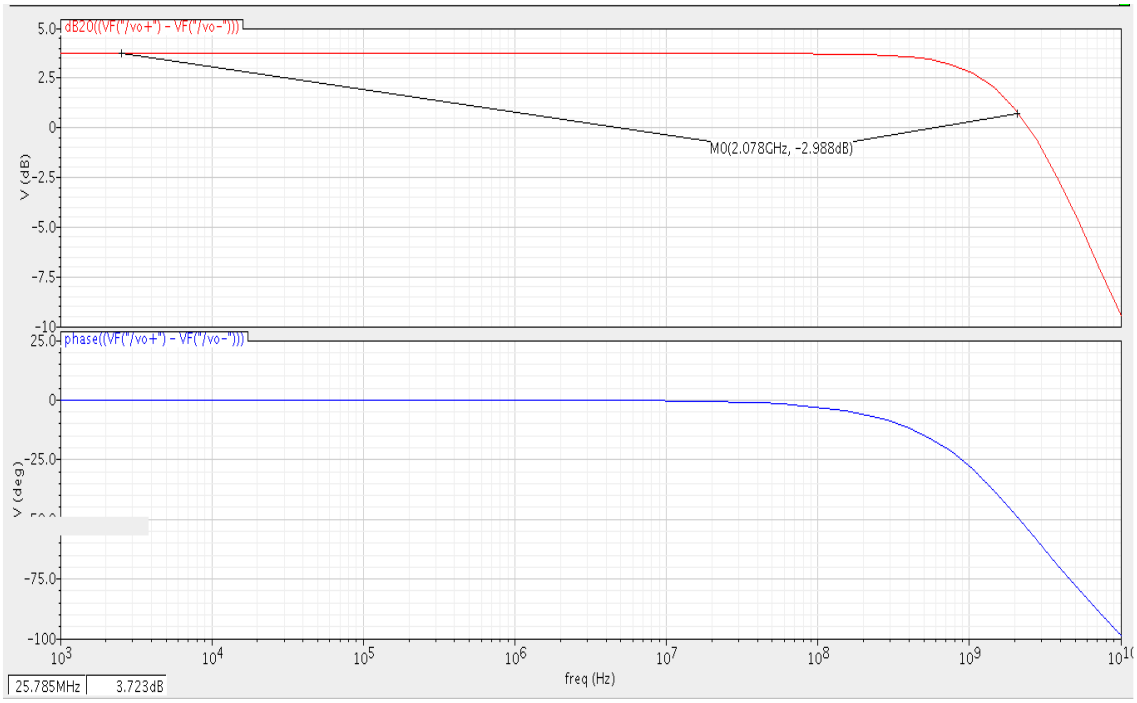


Figure 36 AC response of the preamplifier: gain ≈ 3dB, BW = 2.078 GHz

The ac response of the pre-amp is shown in Figure 36. The preamp has a small gain of 3dB and a bandwidth of 2.07GHz. The main requirement here is that the preamp needs to be fast even if it means it can offer only a low gain. The bandwidth achieved is four times the sampling frequency.

4.7. Comparator – operation and circuit design

The comparator used in the current work is based on the one reported in [19]. It is a robust architecture for sub-nanometer designs operating with low supply voltages. The comparator is a modification of the conventional latch which has two inverters connected back-to-back. Figure 37 shows the circuit diagram of the comparator. This comparator architecture is faster compared to the conventional one, especially at low supply voltages [19]. The additional circuitry (shown in red) aids in this aspect.

There are three phases of operation – reset, sampling, and regeneration. During the reset phase, the clock (CLK) is low, M_{TAIL} is OFF and the input transistors are disabled. M_{1P} and M_{2P} are ON and the output nodes V_{OUT+} and V_{OUT-} are connected to V_{DD}. Also, M_{5N} and M_{6N} are ON, grounding the nodes FB+ and FB-. This switches M_{3P} and M_{4P} ON, thus resetting both the outputs V_{OUT+} and V_{OUT}- to V_{DD}. During the positive edge of the clock, for a short period of time, the sampling phase occurs and when the CLK is logic 1 (high), regeneration phase occurs. The events during the sampling and regeneration phases are described below.

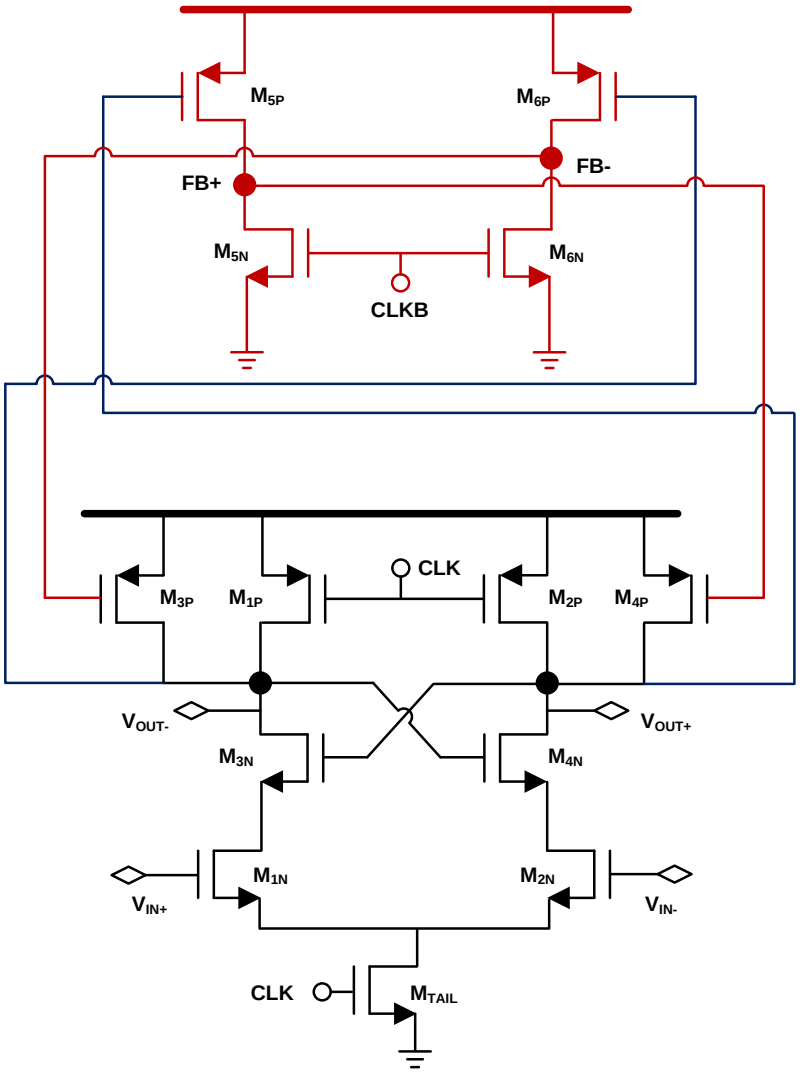


Figure 37 Circuit diagram of the *Goll* comparator [19].

During sampling, (i.e., while the CLK edge is rising), the transistor M_{TAIL} is momentarily in saturation and acts like a current source. The input transistors M_{1N} and M_{2N} are also momentarily in saturation and act like a differential pair. They sample the input signal and dictate the latch decision. Suppose V_{IN+} is greater than V_{IN-}, then V_{OUT-}

is discharged from V_{DD} through M_{3N}, faster than how M_{4N} discharges V_{OUT+}. This causes M_{6P} to conduct more than M_{5P} and FB- to charge faster than FB+. Thus, M_{3P} switches OFF faster than M_{4P}, bringing the node V_{OUT-} lower than V_{OUT+}. This has now ensured a positive feedback to be set up, quickly discharging V_{OUT-} to ground while pulling V_{OUT+} to V_{DD}. Thus, V_{OUT+} is latched onto V_{DD} while V_{OUT-} to ZERO. When V_{IN+} is less than V_{IN-}, the vice versa happens. The three phases of operation are shown in Figure 38.

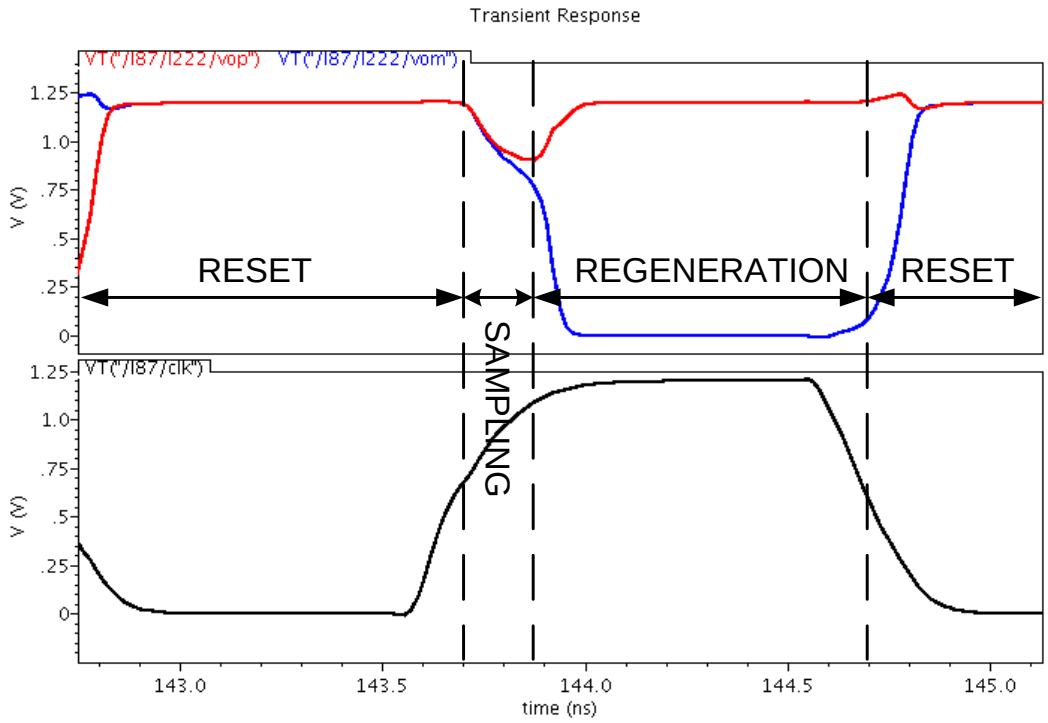


Figure 38 Transient response of the comparator showing three phases of operation

The comparator is designed with large input devices, $M_{1,2N}$, to minimize offset. The transistors M_{3N} and M_{4N} act as a cascode device preventing the capacitance of the input transistor from affecting the speed of latching at the output. This means we can

maximize the input device dimensions without concerning about a reduction in speed. The designed transistor dimensions are listed in Table 7.

Table 7 Transistor dimensions for the comparator shown in Figure 37

Device	**Dimensions/Value**	**Device**	**Dimensions/Value**
$M_{1,2N}$	10 x 1.88µm/100nm	$M_{1,2P}$	3 x 760nm/100nm
$M_{3,4N}$	10 x 760nm/100nm	$M_{3,4P}$	3 x 760nm/100nm
$M_{5,6N}$	2 x 760nm/100nm	$M_{5,6P}$	4 x 760nm/100nm
M_{TAIL}	10 x 1.88µm/100nm		

The advantage of this comparator architecture is that the auxiliary circuit helps regenerate the outputs at a very high speed, especially at low supply voltages. But the main issue in this comparator is that the sampling instant is not well defined as in the case of a circuit with a sample and hold. The sampling phase discussed earlier is in fact a *tracking* phase where the comparator tracks the input before regeneration. This means there is no exact sampling edge at which the data is sampled. This is a major source of non-linearity in this quantizer, as seen from the DNL/INL plots shown in Section 5.1.

4.8. SR latch

The SR latch is the final stage in the quantizer chain. The comparator before the latch actually acts like a sense amplifier and this combination is called a *sense amplifier*

based flip-flop (SAFF) [20]. The combination is a flip flop in the sense that it latches on to the value of the data at the positive edge of the clock.

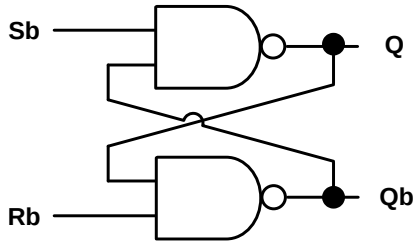


Figure 39 Circuit diagram of the conventional S-R latch.

In a conventional SR latch, as shown in Figure 39, a low level on both Sb and Rb is not allowed. This is guaranteed by the comparator, described in the previous section. A low level at Sb sets the Q output high, which in turn forces Qb to low. Conversely, a low level at Rb sets Qb high, which in turn forces Q to low. Therefore, one of the output signals will be delayed with respect to the other. Additionally, the delay of Q depends on the load on the complementary output Qb and vice versa. This limits the performance of the SR- latch.

In the modified structure used in the present work, a symmetrical structure is obtained. The logical equations for the new outputs Q^+ and Qb^+ is as follows: [20]

$$Q^+ = S + \overline{R}.Q \tag{4.12}$$

$$\overline{Qb^+} = R + \overline{S}.\overline{Q} \tag{4.13}$$

(Note: $Qb \equiv \overline{Q}$, $Sb \equiv \overline{S}$ & $Rb \equiv \overline{R}$)

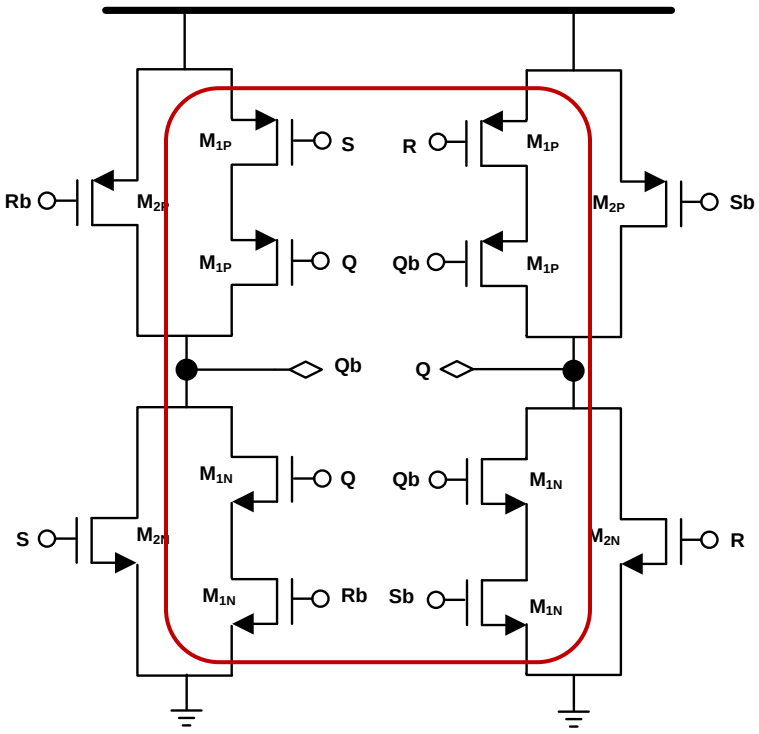


Figure 40 Circuit diagram of the modified S-R latch.

Table 8 Transistor dimensions for the SR-latch shown in Figure 40

Device	**Dimensions/Value**
M_{1P}	1 x 500nm/100nm
M_{2P}	4 x 500nm/100nm
M_{1N}	1 x 250nm/100nm
M_{2N}	2 x 500nm/100nm

Both the equations can be implemented using AND-OR structures. Equations (4.5) and (4.6) will be used for the PMOS transistors. These equations are for *ones* of the Karnaugh Map expression for Q^+ and Qb^+ the SR-latch [20]. For the NMOS, the zeros of the Karnaugh map are covered, and we can get expressions for Q^+ and Qb^+. The final structure, as shown in Figure 40, is thus symmetrical. Transistors are designed such that the *keeper* transistors (shown in red), M_{1P} and M_{1N}, are small [20]. The dimensions of the transistors are as shown in the Table 8 above.

4.9 Overall operation

There are two phases of the overall operation of the quantizer – Reset phase and Sampling phase, as shown in Figure 41. In the reset phase, the differential outputs of the current comparators are all reset to the common mode voltage of 600mV. This avoids any accumulation of offsets/errors at that node from one cycle to the next. The output of the strong-arm latch is also reset to V_{DD} = 1.2V during this phase. During the sampling phase, the differential outputs of the current comparator is leveraged from V_{CM} = 600mV to the actual voltage at the node. This is then amplified by the preamp and sampled by the strong-arm latch.

The fast path signal, which is a current pulse from the fast path DAC, is injected at the beginning of the reset phase (falling edge of the clock). This allows the relatively slow current summing stage and current mirrors to mirror the input current before the sampling edge arrives. The signal is available at the current comparison node right

before the rising edge of the clock. Thus, there is a delay of T/2 between the injection of the fast path signal and the sampling edge.

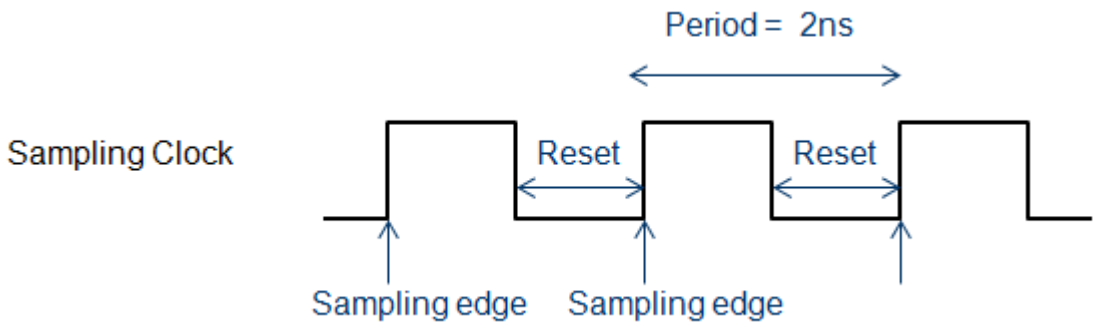


Figure 41 Timing diagram showing overall operation

4.10 Total power consumption

Static power is consumed only by the current comparison branches and the set of preamplifiers. The current consumption of each preamplifier is 120µA, while that of each comparison branch is 240µA (differential). There are seven such branches and preamplifiers in the present flash architecture, giving rise to a total static current consumption of 2.52mA. If we include the bias current sources the current consumption rises to 3.36mA.

The current consumption of the current summing stage is 1.02mA, while that of the current mode quantizer is 3.36mA, giving rise to a total static current consumption of 4.38mA. This is compared to summing amplifier design in 0.18µm [2], where the static current consumption of the summing amplifier alone was 5.6mA. The supply voltage used in that 0.18µm design was 1.8V implying a total power consumption of 10mW.

The entire design of the proposed quantizer was carried out in IBM 90nm CMOS process with a supply voltage of 1.2 V. Thus, the static power consumption is 5.3mW for the current summing stage and the current-mode quantizer. Dynamic power consumption for the case when a sinusoid of 20 MHz is applied along with a fast path signal at 500 MHz is 7mW.

4.11 Conclusion

Conventional voltage-mode summing amplifiers use high-power op-amps while the proposed summing stage operates in current domain and offers considerable savings in power consumption. The summed currents are then quantized using a 3 bit current-mode quantizer. The circuit implementation of the current-summing stage and quantizer was discussed in detail and the overall operation of the quantizer was provided.

5. CHARACTERIZATION OF THE CURRENT MODE QUANTIZER

Static characterization of the quantizer is presented at first. The non-linearity measures of DNL and INL are analyzed across temperature and process. Results of overdrive recovery test and comparator delay test are provided. Then, the sensitivity of the quantizer with respect to mismatch is analyzed with the help of Monte Carlo simulations. Next, the dynamic performance of the quantizer is presented. The impact of clock jitter in the presence of a blocker is then studied. Finally, the quantizer designed in this work is compared with other solutions.

5.1 Ramp Test – DNL/INL

An input current ramp signal (triangular wave) of 1MHz from -40 μA (-FS) to +40 μA (+FS) is applied. The output bit transitions during the ramp test are as shown in Figure 42.

A macro-model for the 3-bit thermometric coded quantizer was written using Verilog-A and the ramp test results of the actual designed quantizer is compared with those of the macro-model. It is to be noted that the ideal values for the transition levels shown in the tables that follow are not theoretical ideal values, but those which the marco-model outputs. Both the quantizers are clocked using the same sample clock.

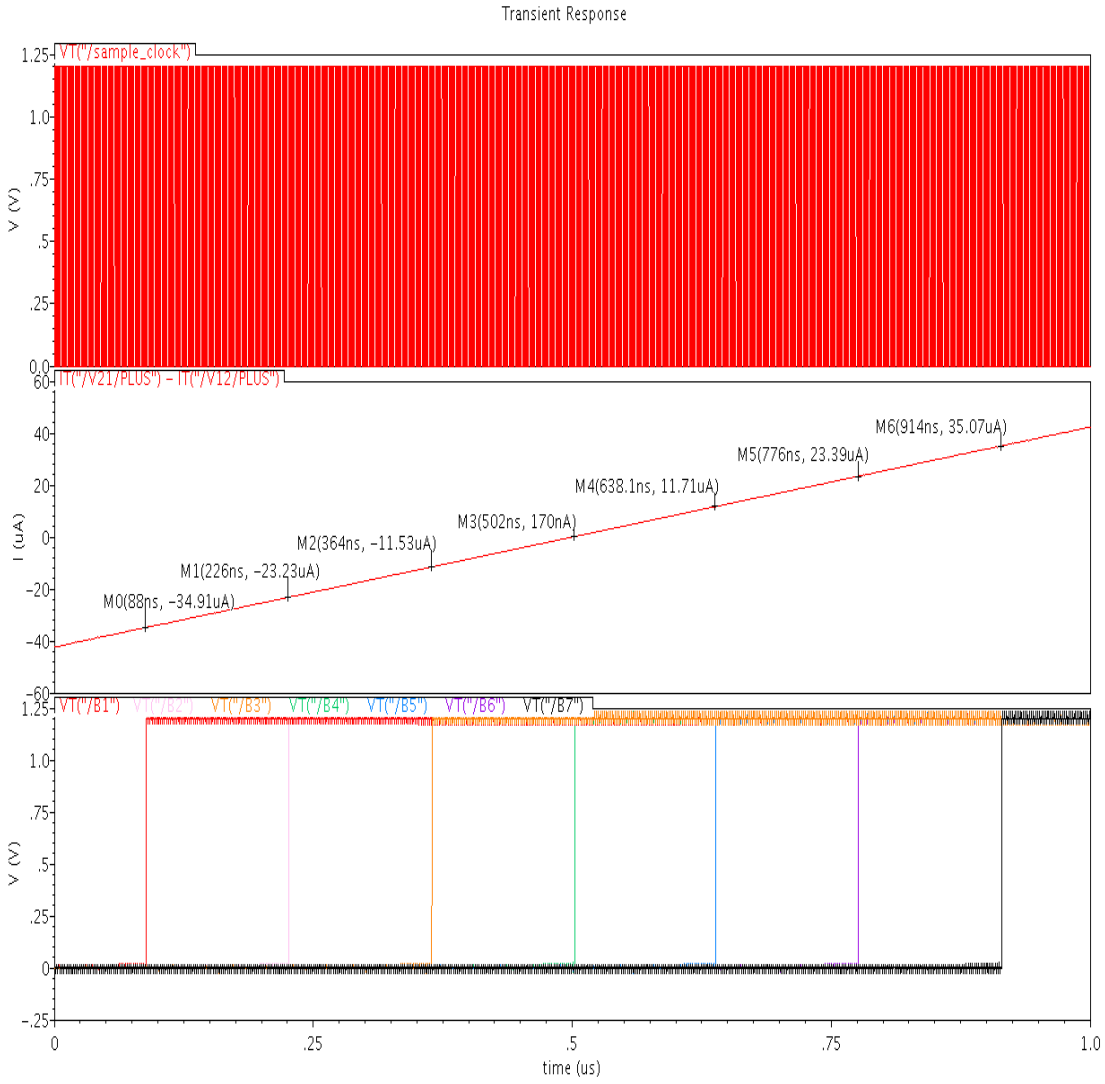


Figure 42 Ramp test output bit transitions with input ramp from -40 µA to +40 µA. Top-to-Bottom: clock signal, input differential current ramp, bits B1, B2… Quantization levels: -34.91 µA, -23.23 µA, -11.53 µA, 0.170 µA, 11.71 µA, 23.39 µA, 35.07 µA

The ramp test is used to measure the relative accuracy of the ADC. The nonlinearity measures of DNL and INL are calculated as given by equations (3.1) and

(3.2). The plot for DNL and INL for the typical process (TT) at room temperature of 27°C is shown in Figure 43.

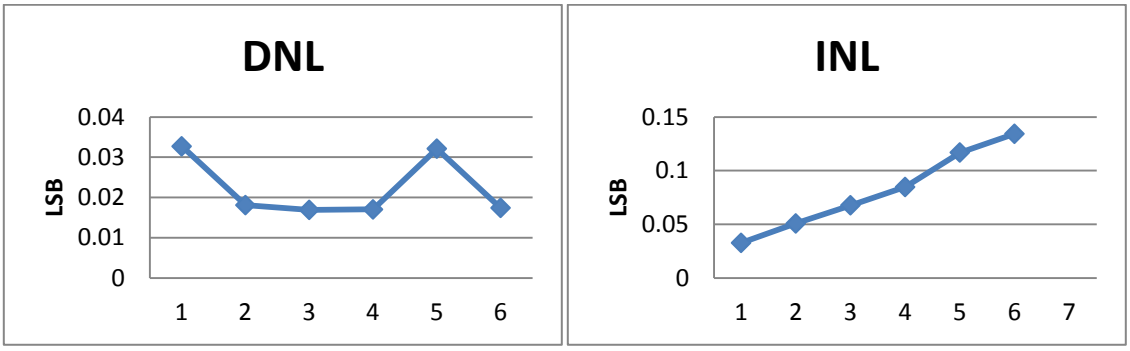


Figure 43 DNL and INL at 27°C for the typical process

5.1.1 Effect of temperature on DNL/INL

The dependence of the non-linearities of the quantizer on temperature is studied. The ramp test is performed as mentioned earlier, for the typical corner, for four different temperature conditions {-40° C, 27° C, 50° C and 80° C}.

Table 9 Variation of the transition levels, DNL and INL with temperature

Ideal Transition levels	**Actual transition levels across temperature**			
	-40° C	**27° C**	**50° C**	**80° C**
-34.14	-35.97	-34.91	-34.63	-34.49
-22.83	-24	-23.23	-23.1	-22.94
-11.3381	-12	-11.53	-11.55	-11.39
-9.00E-09	1.66E-07	1.70E-07	1.69E-07	1.69E-07
11.504	12.17	11.7	11.72	11.56
22.83	24.16	23.39	23.27	23.11
34.31	36.3	35.07	34.8	34.65

Table 9 (continued)

Code number	DNL			
	-40° C	**27° C**	**50° C**	**80° C**
1	0.058355	0.032714	0.019452	0.02122
2	0.044214	0.018108	0.005056	0.005056
3	0.058378	0.016925	0.018689	0.004578
4	0.057893	0.017038	0.018776	0.004868
5	0.058626	0.032138	0.019778	0.019778
6	0.057491	0.017422	0.004355	0.005226

Code number	INL			
	-40° C	**27° C**	**50° C**	**80° C**
1	0.058355	0.032714	0.019452	0.02122
2	0.102569	0.050823	0.024508	0.026276
3	0.160948	0.067748	0.043197	0.030853
4	0.21884	0.084786	0.061973	0.035721
5	0.277467	0.116924	0.08175	0.055499
6	0.334958	0.134346	0.086106	0.060725

From the above analysis shown in Table 9, we can conclude that even in the worst case condition of a very low temperature of -40° C, the DNL_{max} is 0.058 LSB and INL_{max} is 0.335 LSB. Hence, there are no missing codes. Figure 44 shows these results plotted.

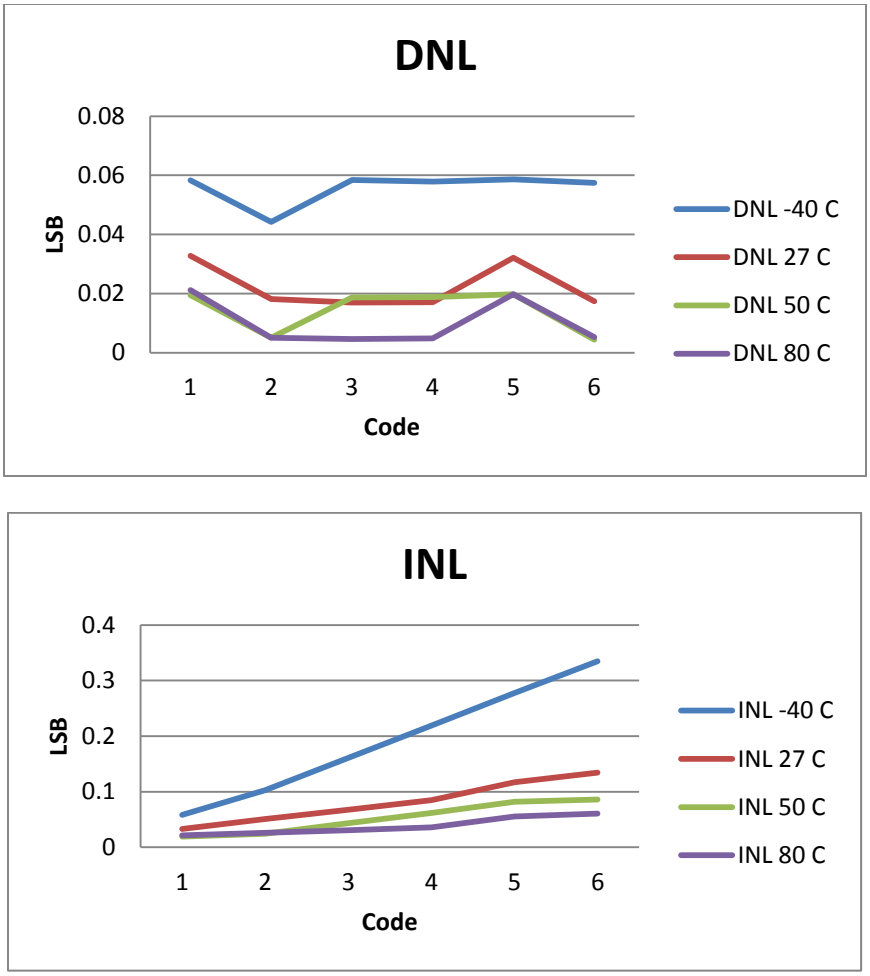


Figure 44 Variation of DNL and INL with temperature

5.1.2 Effect of corners on DNL/INL

The dependence of the non-linearities of the quantizer on various corners is studied. The ramp test is performed as mentioned earlier, at a room temperature of 27^{o}C, for the four corners {FF, SS, FS and SF} in addition to the typical case (TT).

Table 10 Variation of the transition levels, DNL and INL with corners

Ideal Transition levels	Transition levels across Corners @ 27^o C				
	TT	FF	SS	FS	SF
-34.14	-34.91	-34.25	-35.7	-35.06	-34.64
-22.83	-23.23	-22.84	-23.7	-23.45	-22.92
-11.3381	-11.53	-11.42	-11.88	-11.64	-11.38
-9.00E-09	1.70E-07	1.72E-07	1.52E-07	1.68E-07	1.69E-07
11.504	11.7	11.59	12.03	11.81	11.72
22.83	23.39	23.01	23.85	23.62	23.09
34.31	35.07	34.43	35.86	35.23	34.8

Code Number	DNL				
	TT	FF	SS	FS	SF
1	0.032714	0.008842	0.061008	0.026525	0.036251
2	0.018108	-0.00626	0.028551	0.02768	0.004186
3	0.016925	0.007223	0.047795	0.026627	0.003696
4	0.017038	0.007476	0.045723	0.026599	0.018776
5	0.032138	0.008299	0.043616	0.042734	0.003885
6	0.017422	-0.00523	0.046167	0.011324	0.020035

Code Number	INL				
	TT	FF	SS	FS	SF
1	0.032714	0.008842	0.061008	0.026525	0.036251
2	0.050823	0.002585	0.089559	0.054206	0.040437
3	0.067748	0.009809	0.137353	0.080833	0.044132
4	0.084786	0.017284	0.183076	0.107432	0.062908
5	0.116924	0.025584	0.226693	0.150166	0.066793
6	0.134346	0.020357	0.27286	0.16149	0.086828

From Table 10 shown above, we can conclude that even in the worst case corner (SS), the DNL_{max} is 0.061 LSB (< 1LSB) and INL_{max} is 0.273 LSB (<0.5LSB). The DNL and INL plots for the various conditions are shown in Figure 45.

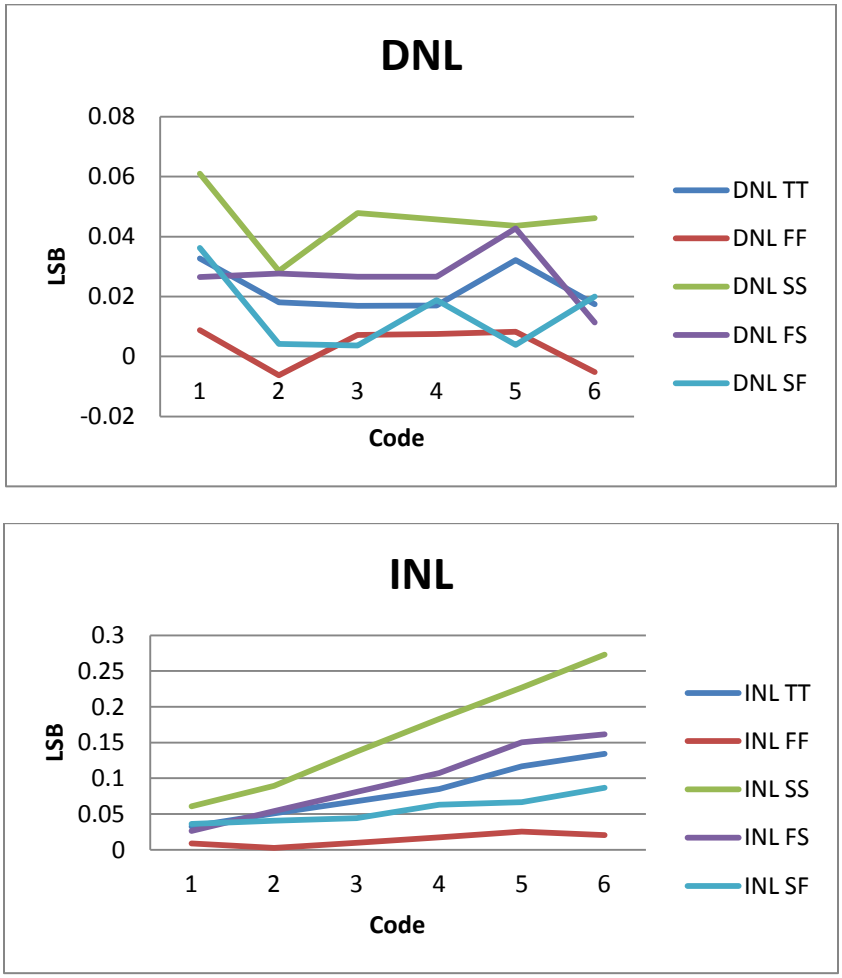


Figure 45 Variation of DNL and INL with corners

5.2. Overdrive recovery test

A small signal of ±0.5LSB is applied right after a full scale signal is applied and it is seen whether the comparator is able to resolve the output correctly [8]. This actually

tests the reaction speed of the quantizer when a strong input in one direction, say +FS/2, is followed by a weak input signal in the opposite direction such as –LSB/2. This pulse is given at the moment of fast path signal injection i.e., falling edge of the clock, as it is the fast path signal that will have instantaneous changes in the signal amplitude and sign.

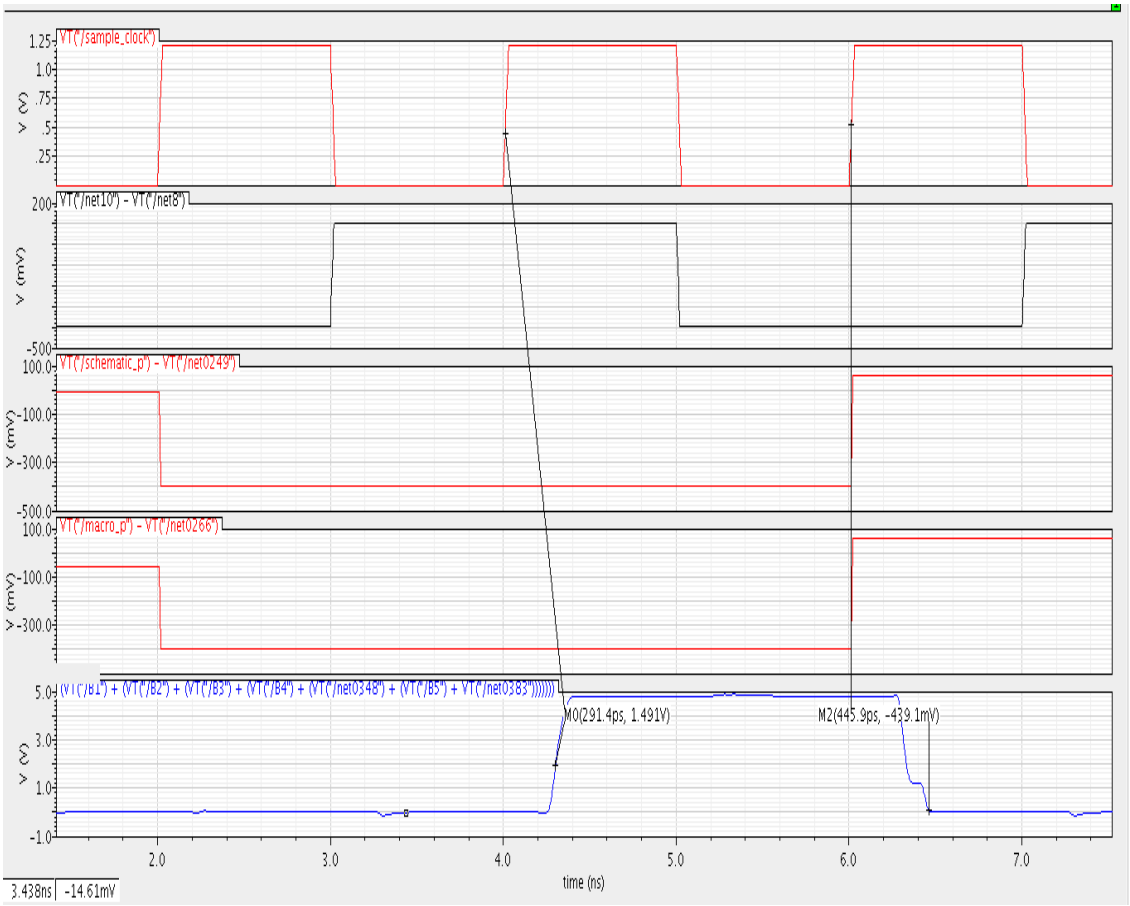


Figure 46 Overdrive recovery test

The recovery time for both the rising and falling edges of the signal is less than T/4 (i.e., < 500ps) as seen from Figure 46. Hence, the quantizer will be able to feed these

signals, through the fast path DAC, back to its input when the next fast path injection occurs at T/2.

5.3. Comparator delay test

When the quantizer is used as a part of the delta sigma loop, it has a slowing varying input (<20MHz) from the output of the integrators and a fast path signal every clock edge from the auxiliary DAC. A test bench modeling this actual scenario is used wherein a 20MHz full scale input signal is given and a 250MHz pulse of ±LSB signal is applied, modeling the fast path signal.

Table 11 Variation of comparator delay with temperature

Clock Data Delay (ps)	-40° C	27° C	50° C	80° C
Rising edge	791.6	463.5	396.6	486.2
Falling Edge	551.4	443.2	450.7	443.6

Table 12 Variation of comparator delay across corners

Clock Data Delay (ps)	TT	FF	FS	SF	SS
Rising edge	463.5	350.8	494.2	502.9	612.6
Falling Edge	443.2	323.5	503.2	455.3	477.7

The worst cases occur around the zero crossing, when the input signal and the fast path signal tend to move in opposite directions and the net (summed) signal is to be quantized. The delay between 50% of the sampling clock edge and final value to which output bit settles is calculated. This represents the delay in the comparator, where the

actual sampling occurs. Figure 47 and Figure 48 shows an example of how the delay is measured. The impact of temperature variation and corners on the delay of the comparator is analyzed and are tabulated above in Table 11 and Table 12.

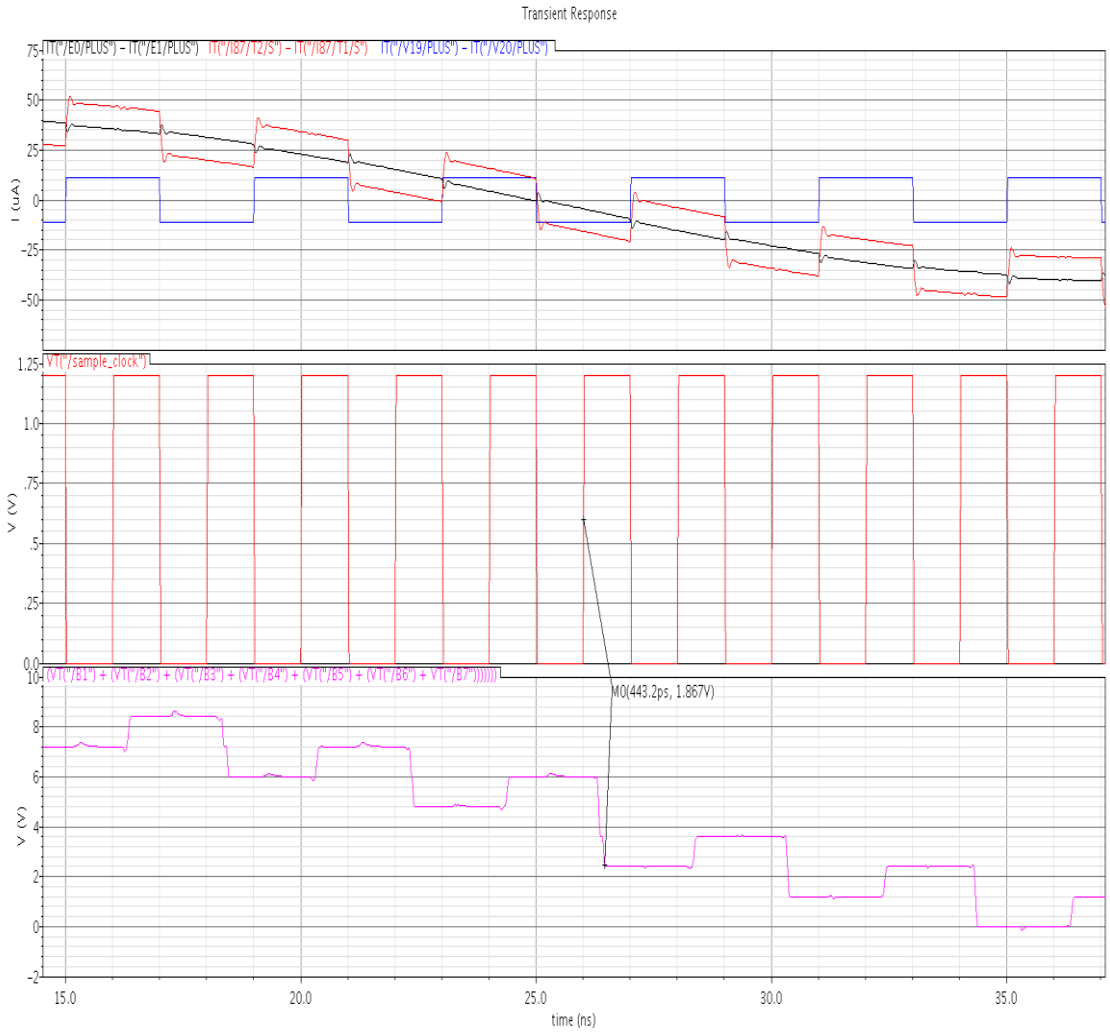


Figure 47 Falling delay of the comparator for the typical case (TT) at 27^{o}C

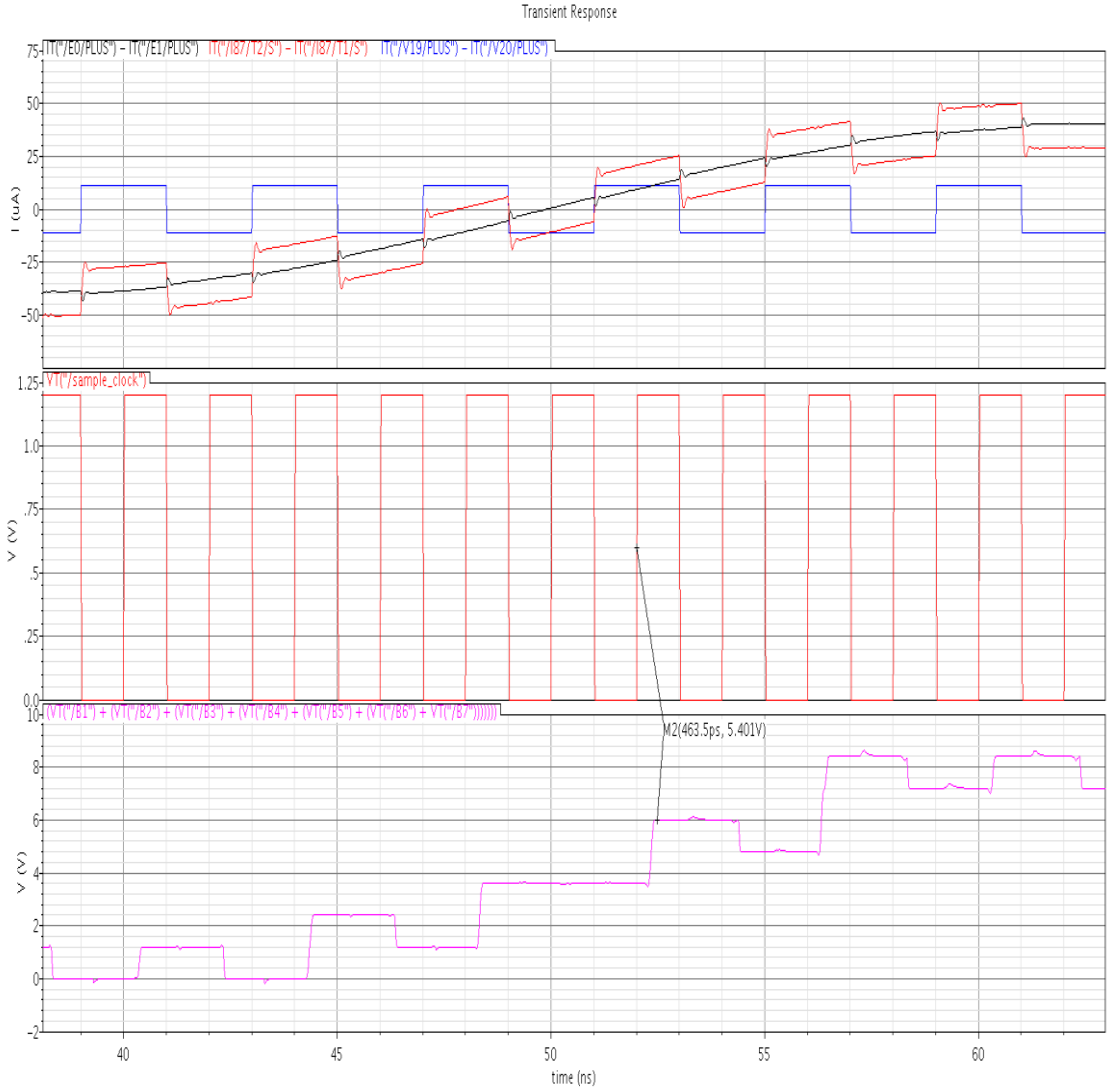
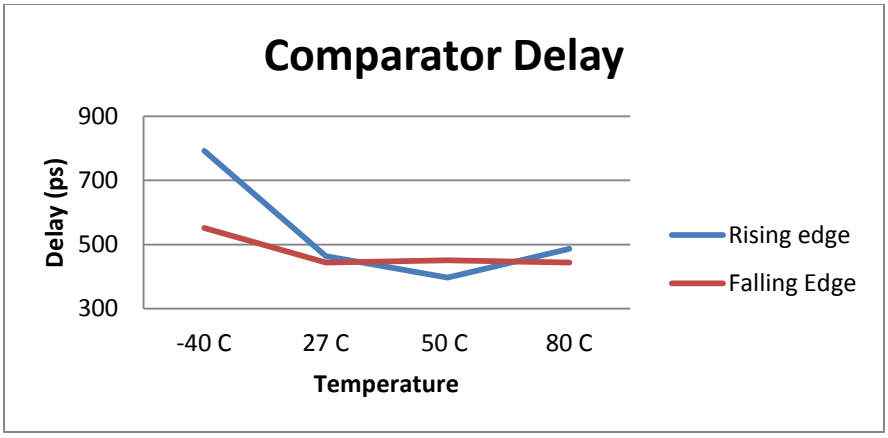
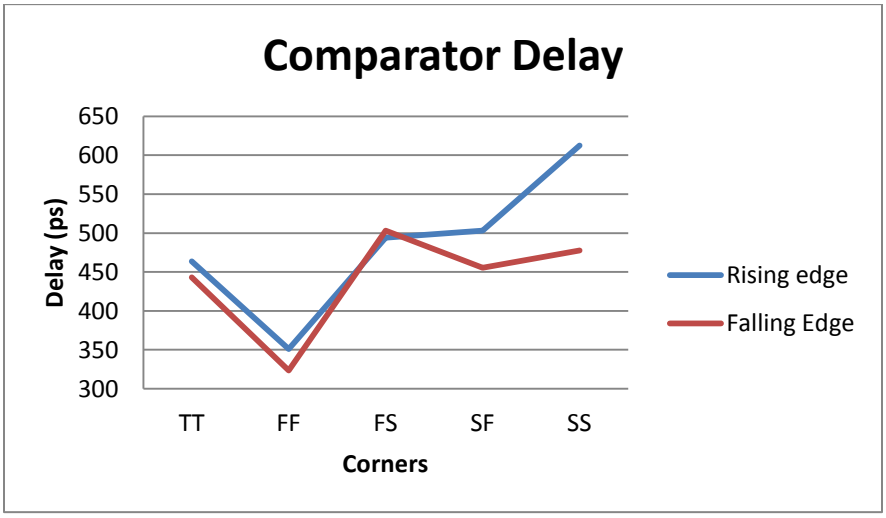


Figure 48 Rising delay of the comparator for the typical case (TT) at 27^{o}C

Figure 49 plots the variation of the comparator delay with temperature and corners. From the above analysis, the worst case delay occurs at -40^{o}C and for the SS corner and has values of 793ps and 613ps respectively. Even in these worst case scenarios, the quantizer outputs the correct value before clock edge at T/2, at which a flip-flop must be able to drive the fast path DAC.



(a)



(b)

Figure 49 Variation of comparator delay with (a) temperature (b) corners

5.4. Monte Carlo simulations

A ramp test is performed with full-scale signal and the output is observed till the first transition level. The ideal value is -34.14µA while the actual designed quantizer gives -34.91µA @ 27^{o}C. With the calculator tool in Cadence, the rising edge of the first

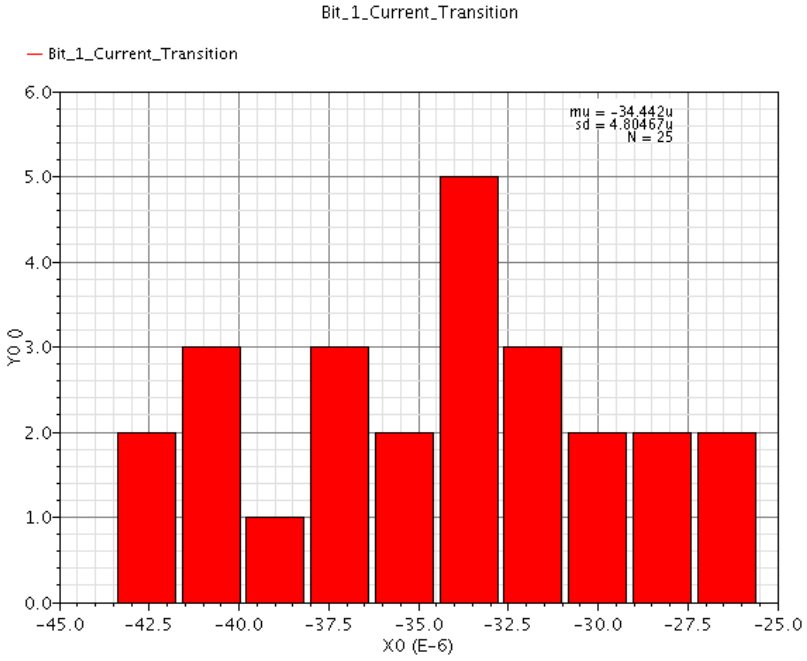
transition level is detected by nesting the cross() function within the value() function as follows:

value((IT("/V21/PLUS") – IT("/V12/PLUS")) cross(VT("/B1") 0.6 1 "rising" nil nil))

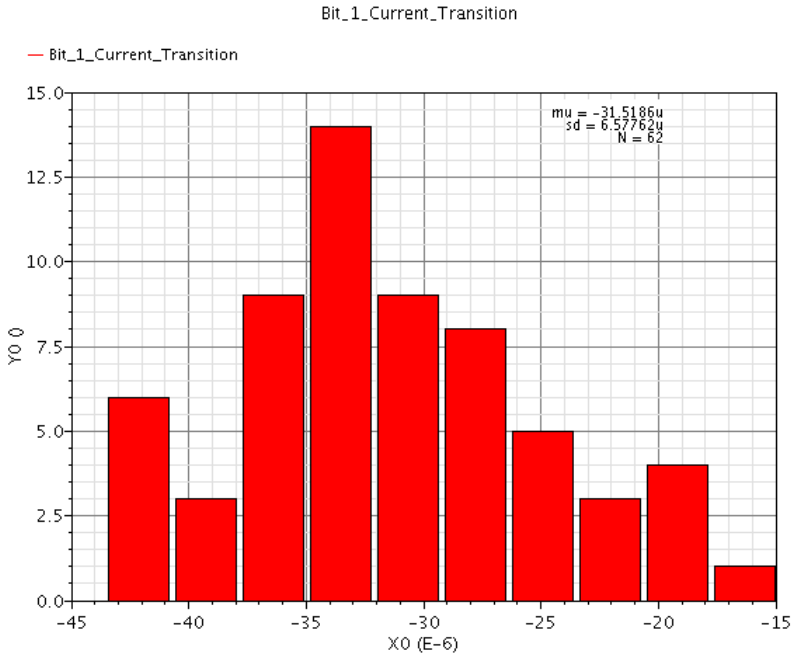
Using this function, the statistical variation of first transition level is observed. This is taken as representative for the variations in all the other levels.

The Monte-Carlo simulations were performed assuming no correlation between any of the transistors used in the design. But in reality, by employing good layout techniques, the transistors used in the current mirrors (current comparators) and in all the differential pairs (in the preamps) are matched. So, this set of simulations reveal the worst case condition when there is 100% mismatch between transistors. Figure 50 shows the simulation results for 25 and 62 runs respectively.

If we assume that the results follow a Gaussian distribution (which is true as the number of runs increases), we can conclude that roughly 5% of the output transition levels would be shifted by 13μA. This reiterates the higher impact of mismatch in sub-nanometer technologies like 90nm and also highlights need to have external current references for post-fabrication tuning/calibration of the reference current.



(a)



(b)

Figure 50 Monte Carlo simulations for (a) N = 25 runs and (b) N = 62 runs

5.5. Dynamic performance

The dynamic performance measures include SNR and inter-modulation distortion. The SNR is calculated with a single tone input of -3dBFS at 7MHz. Note that, a -3dBFS tone corresponds to 40µA full-scale input current to the quantizer. The value of SNR is calculated over a bandwidth of 20MHz. The spectrum got in cadence for this simulation is shown in Figure 51. The in-band SNR in this case is 37.52 dB. To test for inter-modulation distortion a two tone test is performed with 5MHz and 6MHz signals. The inter-modulation products at 4MHz and 7MHz are 35 dB below signal level. This corresponds to IM3. Figure 52 shows the output spectrum of a two-tone test.

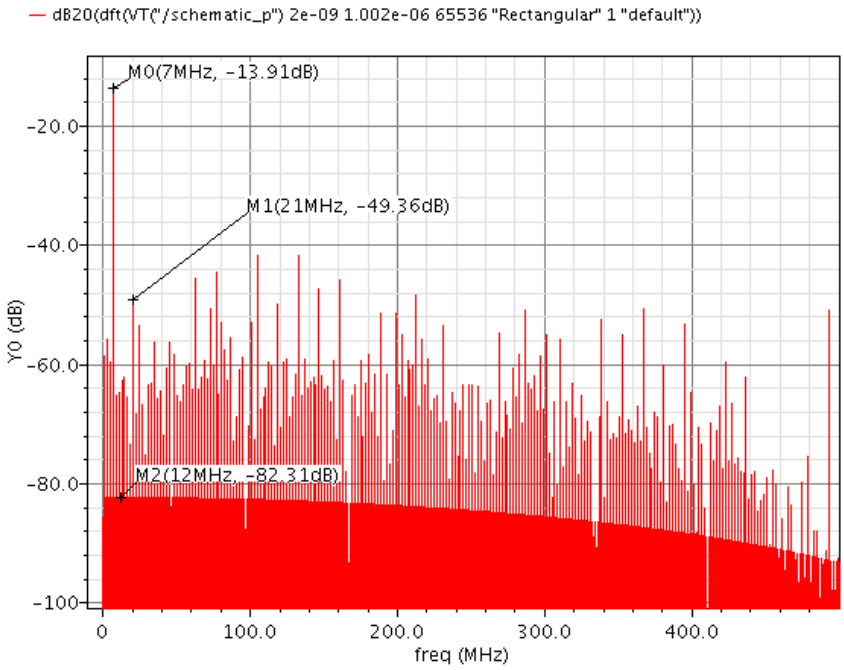


Figure 51 FFT of quantizer output in cadence for a 7MHz -3dBFS input tone.

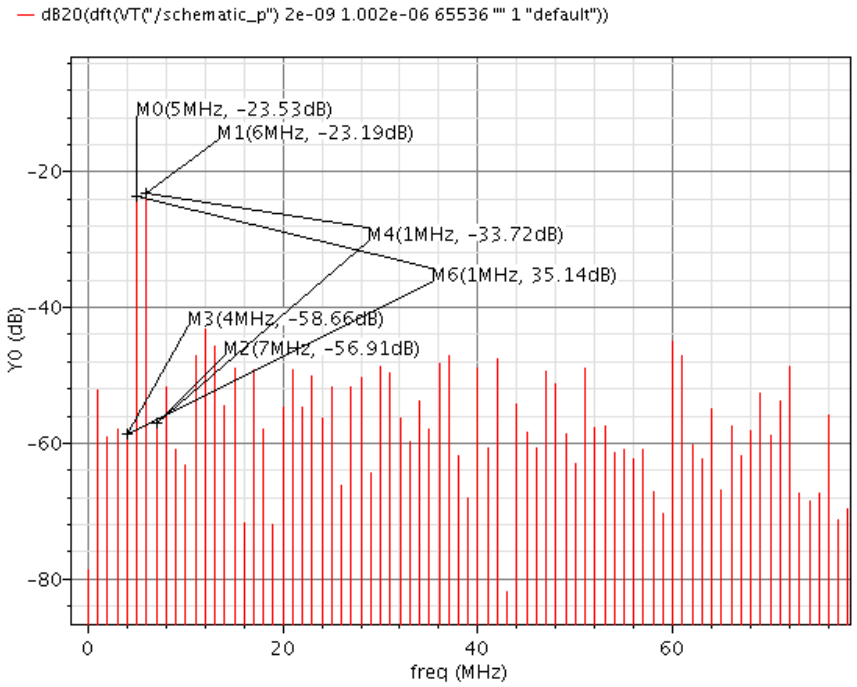


Figure 52 Two-tone test – inputs at 5MHz and 6MHz.

5.6. Jitter Analysis

The sampling clock signal which drives the quantizer core is generated using an on-chip voltage controlled oscillator (VCO). A VCO converts variations in voltage domain into frequency (phase) domain. Hence, voltage noise at the input of the VCO gets converted into frequency domain and manifests itself as *phase noise*. In the time domain, this corresponds to random variations in the sampling clock edge and is termed *jitter*.

To understand how jitter/phase noise affects the output spectrum of the quantizer, let us revisit the process of sampling [21]. As shown in Figure 53, x(t) represents the continuous time analog input, p(t) is the ideal sampling function and $x_p(t)$, the sampled

output. The process of sampling can be viewed as the product of the input waveform and the sampling function, written as follows:

$$x_p(t) = x(t)p(t) \tag{5.1}$$

where

$$p(t) = \sum_{n=-\infty}^{+\infty} \delta(t - nT) \tag{5.2}$$

In the frequency domain, as shown in Figure 53, this can be represented as the convolution between the spectrum of x(t) and p(t) as follows:

$$X_p(\omega) = \frac{1}{2\pi} [X(\omega) \circledast P(\omega)] \tag{5.3}$$

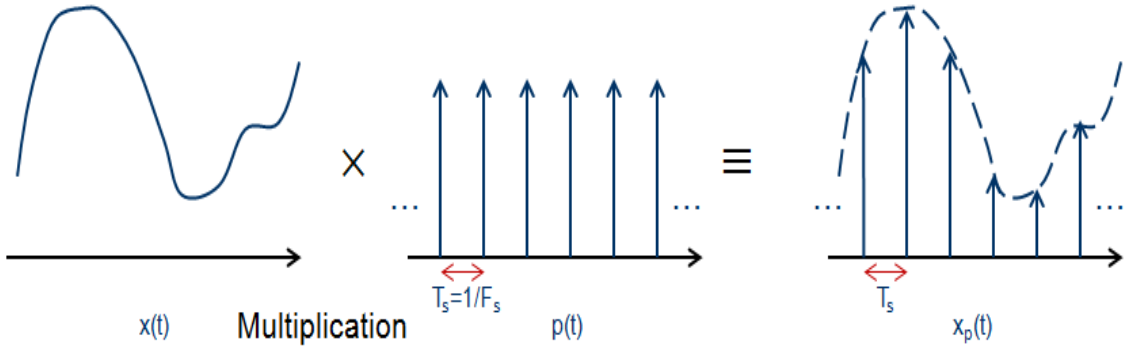
The sampling signal p(t) is an impulse train and hence the frequency domain representation is also an impulse train.

$$P(\omega) = \frac{2\pi}{T} \sum_{k=-\infty}^{+\infty} \delta(\omega - k\omega_s) \tag{5.4}$$

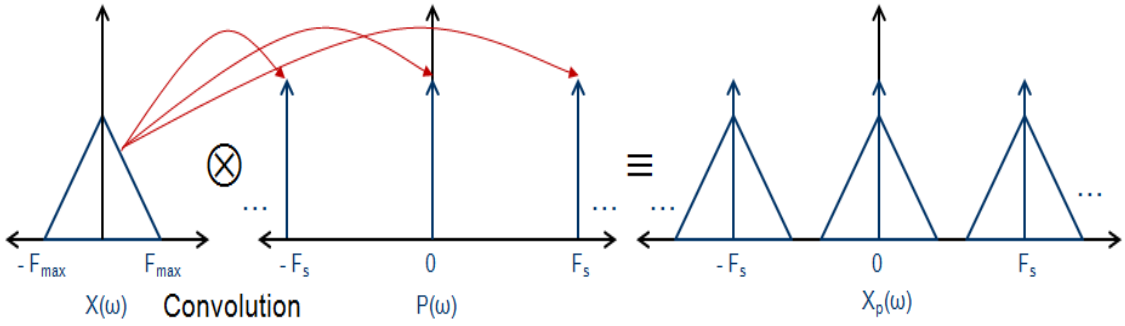
where ω_s is the sampling frequency.

Substituting equation (5.4) in (5.3), we get

$$X_p(\omega) = \frac{1}{T} \sum_{k=-\infty}^{+\infty} X(\omega - k\omega_s) \tag{5.5}$$



(a)



(b)

Figure 53 Process of sampling – (a) time domain and (b) frequency domain.

Equation (5.5) shows that the sampled spectrum is nothing but the input spectrum repeated at intervals of the sampling frequency ω_s. In other words, this operation of sampling can be thought of as a *mixing* or convolution that occurs between the analog input signal and the sampling pulse (i.e., clock). But in reality, the sampling clock is not ideal and has a phase noise associated with it. As shown in Figure 54, the phase noise profile of the clock has a high value of *close-in* noise followed by a wide-band thermal noise floor. The thermal noise floor is usually less than the quantization noise floor.

Any unwanted signal in the spectrum is termed *blocker*. The blocker may be a strong adjacent channel signal or a signal close to the clock frequency. In the first case shown in Figure 54, the blocker signal is at a low frequency (adjacent channel). The blocker convolves with the thermal noise region of the phase noise profile of the clock and the result appears in-band. This increases the in-band noise floor and hence, causes a degradation in SNR.

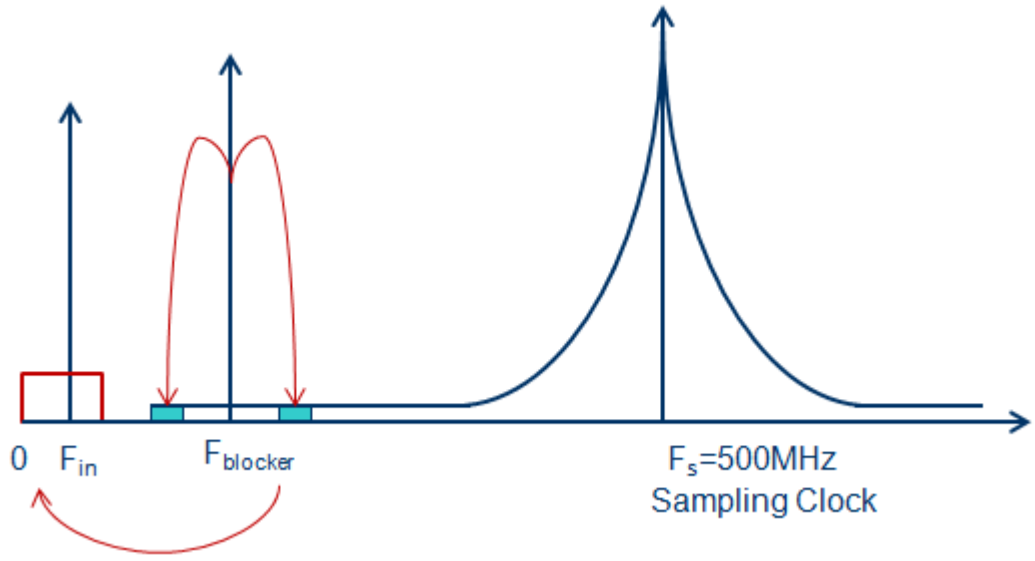


Figure 54 Impact of a low frequency blocker on the in-band noise floor

In another case, the blocker signal may appear at very high frequencies, even close to the clock frequency (500 MHz), as shown in Figure 55. The blocker signal now convolves with the *close-in* phase noise which is high. The result of convolution falls close to the clock frequency and is aliased back in-band. The increase in the noise floor and hence SNR degradation is much higher in this case.

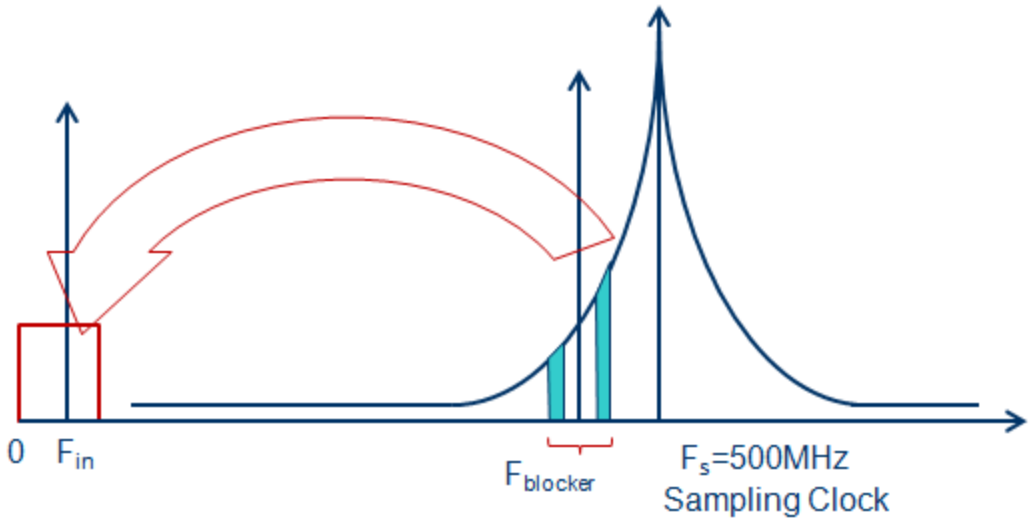


Figure 55 Impact of a high frequency blocker on the in-band noise floor

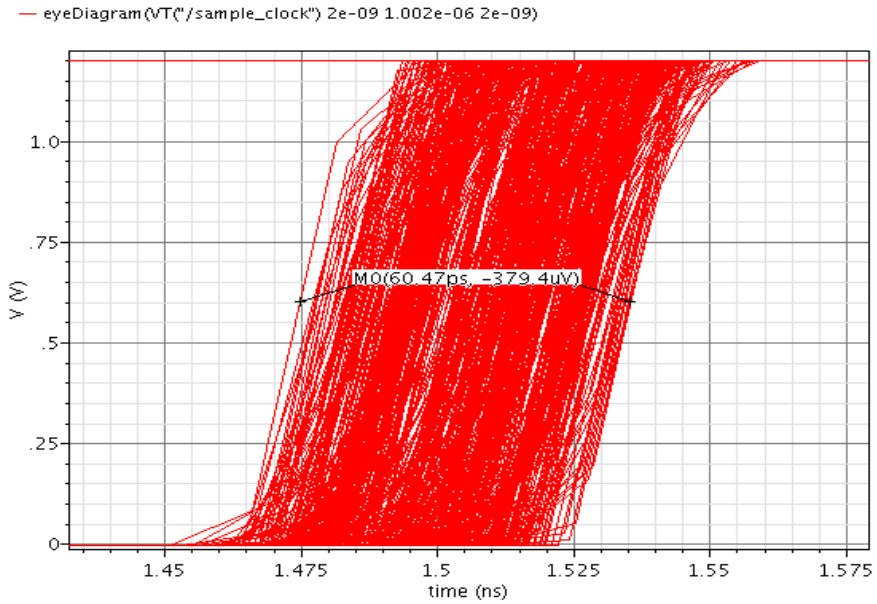


Figure 56 Eye-diagram of the 500MHz sampling clock with a peak-to-peak jitter of 60.4ps equivalent to 1% RMS jitter

Thus, the performance of the quantizer needs to be evaluated in the presence of a jittery clock and in the presence of a blocker at low and high frequencies. In the test bench, a verilog-A model [22] is used to simulate a VCO with phase noise. A typical value of 1% is assumed for the RMS-jitter. The output of this VCO, who eye-diagram is shown in Figure 56, is used to provide the sampling clock to the quantizer. The equivalent spectrum of the sampling clock is shown in Figure 57.

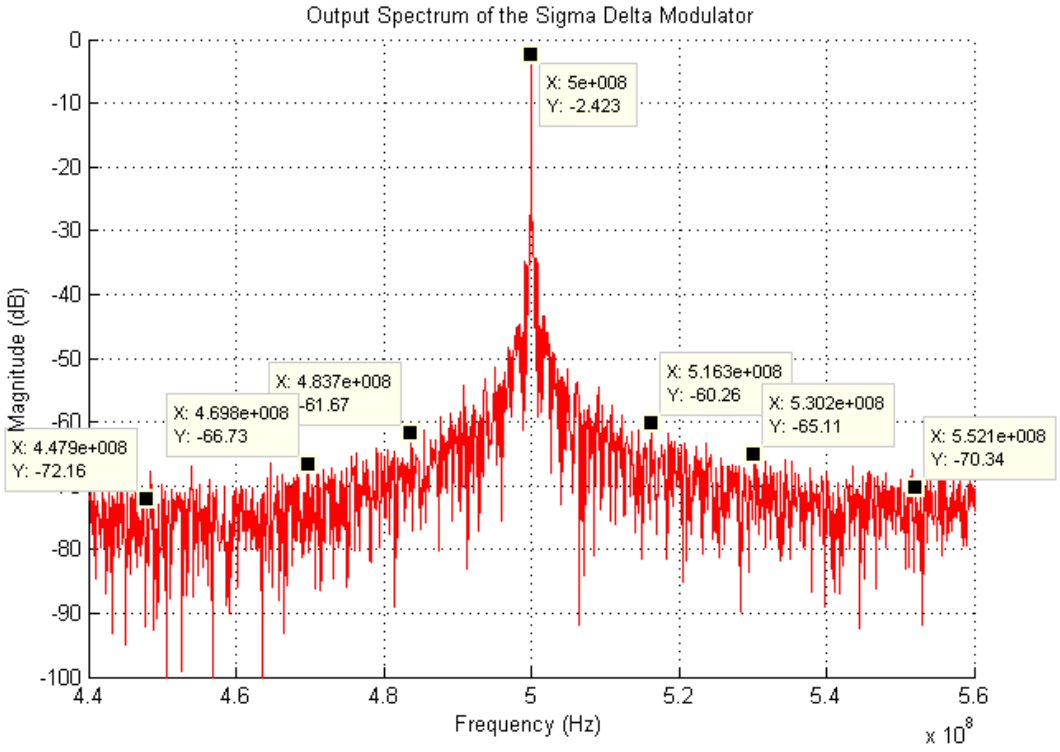


Figure 57 Spectrum of the clock at 500 MHz showing the phase noise profile

The in-band signal-to-noise ratio (SNR) is calculated for different input power levels for four different cases as illustrated in Figure 58:

(a) Ideal case – a 7MHz input signal with zero jitter clock and no blocker signal,

(b) A 7MHz input signal with clock having 1% RMS jitter but no blocker signal,

(c) A 7MHz input signal with 1% RMS jitter clock and a -13dBFS blocker signal at 40MHz, and

(d) A 7MHz input signal with 1% RMS jitter clock and a -13dBFS blocker signal at 460MHz.

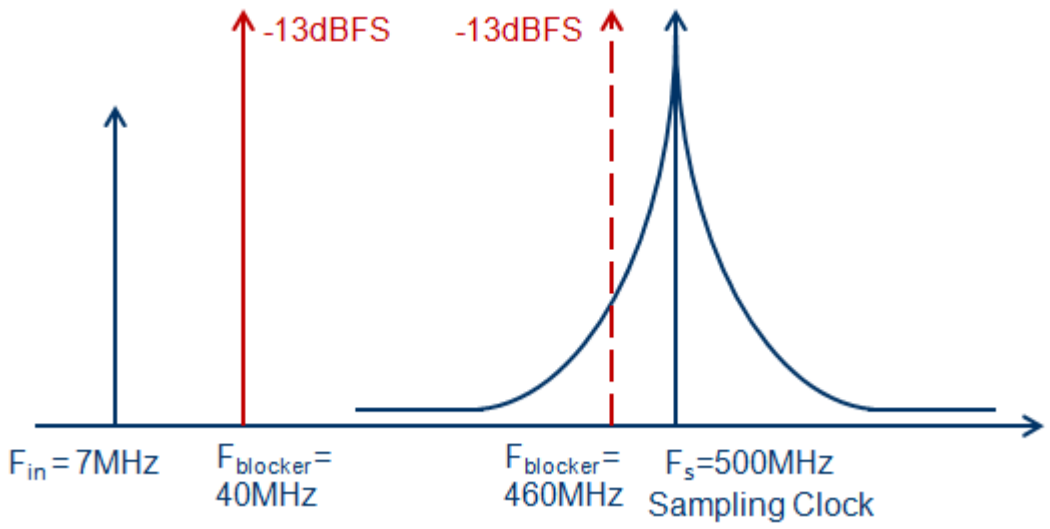


Figure 58 Illustration of the various test conditions for analyzing the impact of clock jitter in the presence of blocker signal.

The results of these tests are plotted in Figure 59. The input signal power is not swept to -3dBFS but restricted to -5dBFS. This is because at an input power level greater than -5dBFS, the combined power of the signal and blocker will exceed the full-scale range of the quantizer and overload the quantizer. We observe that the impact of clock jitter alone, on the in-band SNR value, is insignificant. However, a blocker at 40 MHz degrades the SNR by 2.5 dB due to convolution of thermal noise region of the clock's

phase noise profile. A blocker at 460 MHz convolves the high close-in noise of the clock and degrades SNR by 5.98 dB. It should be noted that this high levels of SNR degradation is due to phase noise profile assumed in Figure 57. In reality, however, the clocks used will have a better phase noise profile and hence the impact will be less severe.

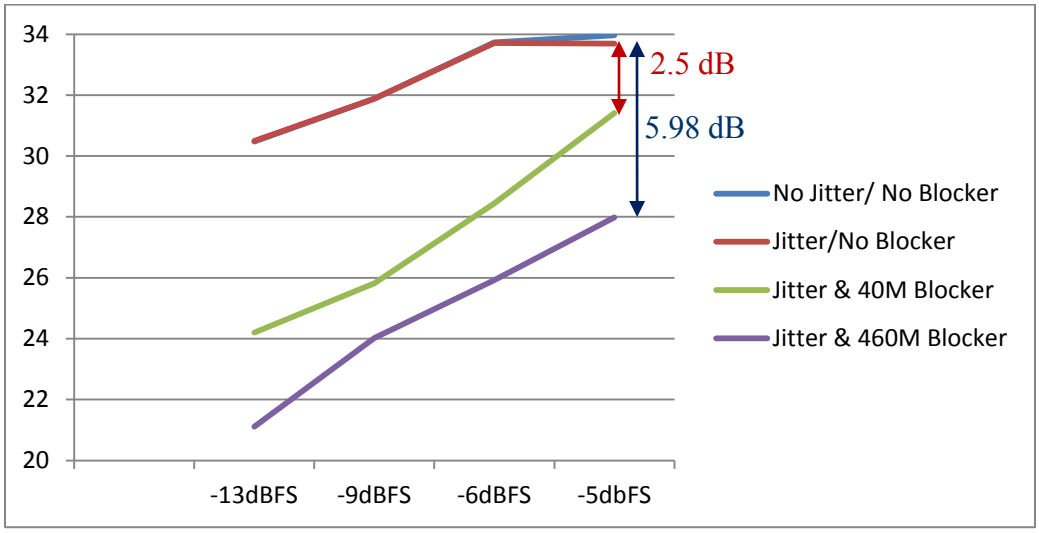


Figure 59 SNR vs. input signal power for three cases (a) ideal case zero jitter clock and no blocker signal, (b) clock having 1% RMS jitter but no blocker signal, (c) 1% RMS jitter clock and a -13dBFS blocker signal at 40MHz, and (d) 1% RMS jitter clock and a -13dBFS blocker signal at 460MHz.

Thus, we see that the jitter of the clock alone is not a major contributor to SNR degradation in a quantizer but when analyzed in conjunction with a blocker signal, we obtain very useful insights. The blocker, at frequencies close to the clock, impacts the SNR more than those that are adjacent channel (that is, close to the input signal).

5.7 Summary of results

A summary of the results of the quantizer designed is provided below in Table 13.

Table 13 Summary of results of the designed quantizer

Results	**IBM 90nm CMOS**
Static Power: Summing Stage	1.2mW
Static Power: Quantizer	4.1mW
Static power : Summing Stage + Quantizer	5.3mW
DNL_{max}	0.061 LSB
INL_{max}	0.335 LSB
SNR degradation due to 1% Jitter clock in the presence of blocker @ 40 MHz	2.5 dB
SNR degradation due to 1% Jitter clock in the presence of blocker @ 460 MHz	5.98 dB
Clock Frequency	500 MHz
Supply Voltage	1.2 V

The power consumption of the designed quantizer is compared with other state-of-the-art solutions reported in literature and tabulated in Table 14. The table shows the relative position of the current work amongst other related works.

Table 14 Comparison of quantizer power consumption with reported designs

Reference	Technology (CMOS)	Fs	BW	Supply Voltage	Number of bits	Quantizer Power Consumption
[14]JSSC 2008	0.13µm	950M	10M	1.2	5 (31 levels)	6mW
[16] JSSC 2010	0.18µm	400M	25M	1.8	3	11.1mW
[23] JSSC 2011	90nm	500M	25M	1.2	4	3mW
[24] JSSC 2010	110nm	300M	10M	1.1	3	0.79mW
[25] JSSC 2009	0.13µm	900M	20M	1.5	4	1.5mW
This work	90nm	500M	20M	1.2	3	4.1mW

6. SUMMARY AND CONCLUSIONS

The delta sigma modulator is a very popular ADC architecture, as it is digital friendly and a substantial part of signal processing is done in the more robust digital domain. Continuous time delta sigma modulator (CT ΔΣ ADC) is highly suited for wide bandwidth and high resolution applications like WiMAX. The design of summing amplifiers in CT ΔΣ ADC involves designing power-consuming wideband op-amps. To overcome this issue of high power consumption, a novel method of current summing was proposed in this thesis. The information in current domain is then quantized using the proposed 3-bit current-mode quantizer based on flash architecture. The design was then characterized for static performance measures. Simulations were done across temperature and corner and mismatch analyses were also performed. Finally, the impact of sampling clock jitter and interferers *(blockers)* on the in-band SNR of the quantizer was analyzed. The circuit design was done in IBM 90nm CMOS process.

REFERENCES

[1] A. Rusu, B. Dong, and M. Ismail, "Putting the "FLEX" in the flexible mobile wireless radios – A wideband continuous-time bandpass sigma-delta ADC software radios," *IEEE Circuits & Devices Magazine*, vol. 22, no. 6, pp. 24-30, Dec. 2006.

[2] V. Gadde, "Filter design considerations for high performance continuous-time low-pass sigma-delta ADC," M.S. thesis, Dept. Electr. Comput. Eng., Texas A&M Univ., College Station, TX, Dec. 2009.

[3] C. Y. Lu, "Calibrated continuous-time sigma-delta modulators," Ph.D. dissertation, Dept. Electr. Comput. Eng., Texas A&M Univ., College Station, TX, May 2010.

[4] V. Periasamy, "System design of a wide bandwidth continuous-time sigma-delta modulator," M.S. Thesis, Dept. Electr. Comput. Eng., Texas A&M Univ., College Station, TX, May 2010.

[5] D. A. Johns and K. Martin, *Analog Integrated Circuit Design.* New York, NY: John Wiley & Sons Inc., 1997.

[6] F. Silva-Rivas, "High performance integrated circuit blocks for high-IF wideband receivers," M.S. thesis, Dept. Electr. Comput. Eng., Texas A&M Univ., College Station, TX, May 2009.

[7] G. Mitteregger, C. Ebner, S. Mechnig, T. Blon, C. Holuigue and E. Romani, "A 20-mW 640-MHz CMOS continuous-time ∑Δ ADC with 20-MHz signal bandwidth, 80-dB dynamic range and 12-bit ENOB," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2641-2649, Dec. 2006.

[8] J. Silva-Martinez, "Flash ADC," [Online]. Available: http://amesp02.tamu.edu/ ~jsilva/610/ Lecture%20notes/Flash.pdf

[9] T. N. Blalock and R. C. Jaeger, "A high-speed clamped bit-line current-mode sense amplifier," *IEEE J. Solid-State Circuits*, vol. 26, no. 4, pp. 542–548, April 1991.

[10] S. Yoo, C. Kim, S. Jung, K. Baek, and S. Kang, "New current-mode sense amplifiers for high density DRAM and PIM architecture," in *Proc. 2001 IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2001, pp. 938–941.

[11] J. Bonan, H. Aboushady and M.M. Louerat, "A 3mW, 250 Msamples/sec, 4-bit current-mode FLASH analog-to-digital converter," in *Proc. 46th IEEE Int. Midwest Symp. Circuits and Systems*, Dec. 2003, vol. 1, pp. 27-30.

[12] F. Maloberti, *Data Converters.* A.A.Dordrocht, The Netherlands: Springer, 2007.

[13] R. van de Plassche, *CMOS Integrated Analog-to-Digital and Digital-to-Analog Converters.* Norwell, MA: Kluwer Academic Publishers, 2003.

[14] M. Z. Straayer and M. H. Perrott, "A 12-bit, 10-MHz bandwidth, continuous-time ΣΔ ADC with a 5-bit, 950-MS/s VCO-based quantizer," *IEEE J. Solid-State Circuits*, vol.43, no.4, pp.805-814, April 2008.

[15] V. Dhanasekaran, M. Gambhir, M. M. Elsayed, E. Sanchez-Sinencio, J. Silva-Martinez, C. Mishra, L. Chen and E. J. Pankratz , "A continuous time multi-bit $\Delta\Sigma$ADC using time domain quantizer and feedback element," *IEEE J. Solid-State Circuits,* vol.46, no.3, pp.639-650, March 2011.

[16] C. –Y. Lu, M. Onabajo, V. Gadde, Y. –C. Lo, H. –P. Chen, V. Periyasamy and J. Silva-Martinez , "A 25 MHz bandwidth 5th-order continuous-time low-pass sigma-delta modulator with 67.7 dB SNDR using time-domain quantization and feedback," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1795-1808, Sep. 2010.

[17] S. Yan and E. Sanchez-Sinencio, "A continuous-time sigma-delta modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth," *IEEE J. Solid-State Circuits,* vol.39, no.1, pp. 75- 86, Jan. 2004.

[18] B. –S. Song, M. –J. Choe, P. Rakers and S. Gillig, "A 1V 6b 50MHz current-interpolating CMOS ADC," in *Symp. VLSI Circuits*, 1999, pp. 79-80.

[19] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65 V", *IEEE Trans. Circuits Syst. II*, vol. 56, no. 11, pp. 810-814, Nov. 2009.

[20] B. Nikolic, V.G. Oklobdzija, V. Stojanovic, J. Wenyan, C. J. Kar-Shing, and M. M. Leung, "Improved sense-amplifier-based flip-flop: design and measurements," *IEEE J. Solid-State Circuits*, vol. 35, no. 6, pp. 876-884, June 2000.

[21] B. Brannon, "Sampled systems and the effects of clock phase noise and jitter," AN-756, Application Note, Analog Devices Inc, Dec 2004.

[22] K. Kundeart, "Verilog-A model for a voltage controlled oscillator with jitter," [Online]. Available: http://www.designers-guide.org/VerilogAMS/functional-blocks/vco/vco.va (open source functional models).

[23] J. G. Kauffmann, P. Witte, J. Becker and M. Ortmanns, " An 8.5 mW continuous-time ΔΣ modulator with 25 MHz bandwidth using digital background DAC linearization to achieve 63.5 dB SNDR and 81 dB SFDR," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 1-13, Dec. 2011.

[24] K. Matsukawa, Y. Mitani, M. Takayama, K. Obata, S. Dosho and A. Matsuzawa, "A fifth-order continuous-time delta sigma modulator with single-opamp resonator," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 697-706, April 2010.

[25] M. Park and M. H. Perrott, "A 78 dB SNDR 87 mW 20 MHz bandwidth continuous-time ΔΣ ADC with VCO-based integrator and quantizer implemented in 0.13 μm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3344-3358, April 2009.

VITA

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