DESIGN OF A DIRECT-MODULATION TRANSMITTER WITH SELF-OPTIMIZING FEEDBACK AND A HIGHLY LINEAR, HIGHLY RECONFIGURABLE, CONTINUOUSLY-TUNABLE ACTIVE-RC BASEBAND FILTER FOR MULTIPLE STANDARDS

A Dissertation

by

HESAM AMIR ASLANZADEH MAMAGHANI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2009

Major Subject: Electrical Engineering

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Approved by:

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December 2009

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ABSTRACT

Design of a Direct-Modulation Transmitter with Self-Optimizing Feedback and a Highly Linear, Highly Reconfigurable, Continuously-Tunable Active-RC Baseband Filter for Multiple Standards. (December 2009)

Hesam Amir Aslanzadeh Mamaghani, B.S., Sharif University of Technology;
M.S., Sharif University of Technology

Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

This work consists of two main parts: i) Design and implementation of a compact current-reusing 2.4GHz direct-modulation transmitter with on-chip automatic tuning; ii) Design and implementation of a novel highly-reconfigurable, continuously tunable, power-adjustable Active-RC filter for multiple standards.

The design, analysis, and experimental verification of a proposed self-calibrating, current reused 2.4GHz, direct-modulation transmitter are introduced. A stacked arrangement of the power amplifier/voltage-controlled oscillator is presented along with a novel LC-tank-tuning algorithm with a simple, low-cost, on-chip implementation. To transmit maximum power, the tuning loop ensures the PA's resonant tank is centered around the operating frequency, and the loop requires no ADC, DSP, or external signal generator. This work also details the proposed tuning-loop algorithm and examines the frequency-dependent nonlinear power-detector. The system was implemented in TSMC 0.18μm CMOS, occupies 0.7 mm^2 (TX) + 0.1 mm^2 (self tuning), and was measured in a QFN48 package on FR4 PCB. Automatically adjusting the tank-tuning bits within their tuning range results in >4dB increase in output power. With the self-tuning circuit active, the transmitter delivers a measured output power of > 0 dBm to a 100-Ω differential load, and the system consumes 22.9 mA from a 2.2-V supply.

A biquad design methodology and a baseband low-pass filter is presented for wireless and wireline applications with reconfigurable frequency response, selectable order ($1^{st}/3^{rd}/5^{th}$), continuously tunable cutoff frequency (1MHz-20MHz) and adjustable power consumption (3mW-7.5mW). A discrete capacitor array coarsely tunes the low-pass filter, and a novel Continuous Impedance Multiplier (CIM) then finely tunes the filter. Resistive/capacitive networks select between the Chebyshev and Inverse Chebyshev approximation types. Also, a new stability metric for biquads, Minimum Acceptable Phase Margin (MAPM), is presented and discussed in the context of filter compensation and passband ripple considerations. Experimental results yield an IIP3 of 31.3dBm, a THD of -40dB at $447mV_{\text{pk, diff}}$ input signal amplitude, and a DR of $71.4dB$. The filters tunable range covers frequencies from 1MHz to 20MHz. In Inverse Chebyshev mode, the filter achieves a passband group delay variation less than $\pm 2.5\%$. The design is fabricated in $0.13\mu m$ CMOS, occupies $1.53mm^2$, and operates from a 1-V supply.

DEDICATED

To My beloved Father and Mother,

My sources of strength and wisdom

To Mr. Mohsen Zaryab,

My Math teacher in midschool

Who encouraged innovation and instilled a love of Math in me

and

To Mr. Mahmoud Bakhtavar,

My Electronics teacher in midschool

Who ignited my passion for Electronics when taught us assembling an FM transmitter kit.

ACKNOWLEDGEMENTS

I would like to thank several people who have enriched my graduate life in Texas A&M University by their friendship, support, encouragement, technical advice and words of wisdom.

It is with a profound sense of gratitude and appreciation that I wish to thank my advisor, Dr. Edgar Sánchez-Sinencio for his continuous support and encouragement. His technical teachings and research advice have made me a better engineer, but I am also eternally grateful to have learned from his vision and life experiences in achieving a fulfilling career and personal life. It was my pleasure to have shared many common interests with him including a passion for photography and world cultures.

I would like to extend my sincere thanks to Dr. Jose Silva-Martinez for serving in my committee and his helpful discussions. I have learned a lot from the technical discussions I have had with him. Also, I would like to thank my committee members, Dr. Aydin I. Karşilayan, Dr. Frederick J. Strieter and Dr. Alexander G. Parlos, for their invaluable comments and suggestions on my dissertation. I am also thankful to Dr. Samuel Palermo for his support and valuable discussions on the PVCO transmitter.

The fabrication and packaging of the PVCO transmitter and on-chip Self-Tuning System was possible through the support of Taiwan Semiconductor Manufacturing Company (TSMC) and the programmable filter project was fabricated through the support of United Microelectronics Corporation (UMC). Texas Instruments (TI) has provided additional measurement facilities. I am grateful for all their support.

I have been privileged to work with very intelligent and hardworking people in my research projects. I am deeply grateful to my friends, office mates and research partners, Erik Pankratz and Chinmaya Mishra. Erik has been a partner on both major parts of this dissertation. Chinmaya has contributed to the development of PVCO transmitter. I will

never forget their continuous support, sincere friendship and company during the long hours of work that we shared side by side. I also would like to express my deep gratitude to my friends, classmates and project partners, Faisal Hussein, Sangwook Park, Didem Turker, Rangakrishnan Srinivasan, Felix Fernandez, Mohammad Mobarak and Heng Zhang, with whom I have worked through the years. I will treasure their friendship for the rest of my life. Faisal also provided assistance for additional measurement of PVCO transmitter. Jason Wardlaw offered valuable feedback on programmable filter. Raghavendra Kulkarni has contributed to many technical and non-technical discussions. I thank them all.

I wish to thank all the professors and students in our AMSC group. They always welcomed technical discussions and kindly shared their time and knowledge. Their friendship and support is what made AMSC always feel like a big family. Ms. Ella Gallagher, secretary of AMSC, deserves a special thank for her cheerful presence and constant support over the years.

From my heart, I thank my dear brother and sister, Rasoul and Sarah, for their love and encouragement. My deepest gratitude is to my dear parents, Fereshteh and Ghassem, for their unwavering support and love and for teaching me to love human beings, to be noble, selfless and sincere.

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CHAPTER I

INTRODUCTION

Wireline/wireless communications are at the forefront of many advances in the analog/RF integrated circuit design. In recent years, communication devices (wireless or wireline) have advanced in increasing performance, integration, complexity at a lower cost. With the introduction of multiple portable communication devices in different standards and desire to reduce the time-to-market and the cost of finished products, demand for designing of low-power and low-cost multi-standard communication devices has significantly grown and there have been many attempts to address such demand. Introduction of dynamic applications such as software-defined radio are focused on reusing one transceiver structure to receive and transmitt information in different standards and hence increasing their utility at a lower cost. To that end, the work presented in this dissertation is detailing three novel approaches to make low-cost, low-power radios a reality both in the baseband and the front-end: i) designing and implementing a novel power-adjustable, highly reconfigurable, continuously-tunable baseband filter for multiple standards and ii) designing and implementing communication circuits operating at GHz frequencies to form a compact, low-power transmitter iii) designing and implementing a self-tuning system to reduce testing cost of RF circuits and its verification on transmitter deigned in (ii).

A. Reconfigurable Baseband Filter

Due to their higher level of integration, improved performance, reduced component count, simplicity of baseband design and hence lower cost, direct-conversion and direct-modulation are attractive choices for designing low power radio devices [1, 2, 3]. Figure 1 shows a gen-

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eral block diagram of a direct-conversion (zero-IF) transceiver architecture.

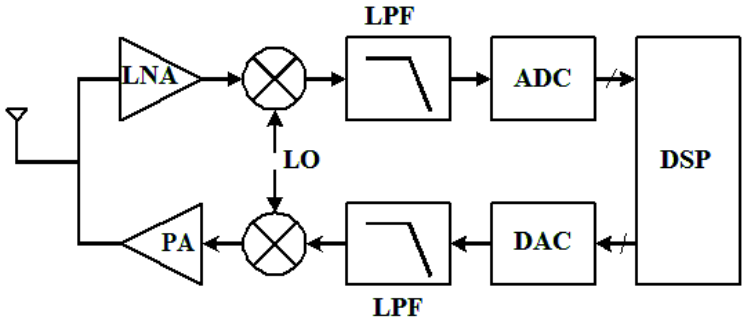


Fig. 1. General block diagram of homodyne transceiver architecture

Transceivers complying with multiple standards require control over different features of receiver and transmitter chain from front-end to the baseband. These architecture require flexible, highly programmable building blocks along the transmitter and receiver chain at the front-end and baseband. Figure 2 displays a general block-diagram of a multi-standard transceiver. At the front-end, this could involve controlling the low-noise amplifier (LNA) 's matching and loading tanks in narrowband applications, adjusting power amplifier (PA)'s output power, output matching and programming phase-locked-loop (PLL)'s divider or reference frequency. At the baseband, DSP should be able to control different aspects of low-pass filter (LPF) including, its degree, cut-off frequency and type and sampling rate and speed and effective dynamic range of data-converters. To realize low power, multi-standard transceivers it would be preferable if power consumption of these blocks also would scale with their frequency or SNR requirements. This work presents a highly-linear, highly reconfigurable, continuously-tunable, power-adjustable active-RC filter for multiple-standards. Chapter IV describes the overall architecture and system-level configuration of the proposed baseband filter, details new metrics to ensure biquad's stability and presents design guideline based on those principles. New techniques developed to continuously tune the cut-off frequency of active-RC filters and filter's building blocks

are presented in Chapter V. Layout techniques used to improve and maintain high-linearity of the fitler and minimize cross-talk and experimental results from the fabricated prototype chip in $0.13\mu CMOS$ technology are detailed in Chapter VI.

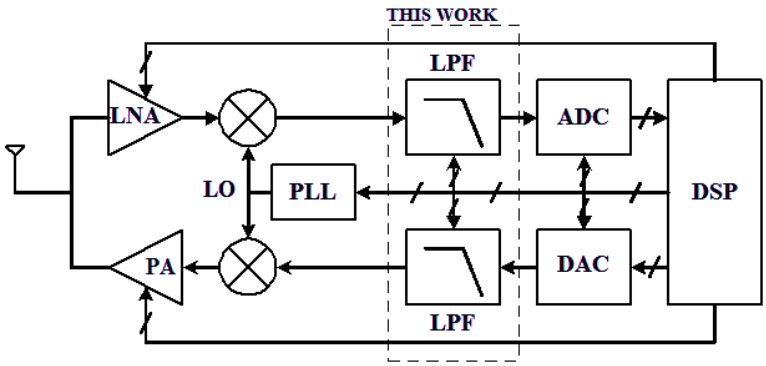


Fig. 2. General block-diagram of a multi-standard transceiver architecture

B. Direct-Modulation Transmitter

While direct-conversion simplifies the baseband implementation, direct-modulation practically obviates baseband processing. Direct modulation saves power and area by eliminating the DAC and up-conversion mixer in the transmitter chain. Figure 3 displays a general block diagram of a direct-modulation transmitter architecture. In low-output-power transmitters, power consumption of blocks before PA becomes comparable with output power and therefore minimizing their power consumption considerably increases the overall efficiency. So, the number and complexity of pre-PA blocks should be minimized in order to increase power efficiency. Based on these principles, simple architectures like injection-locked transmitters and direct-modulation transmitters are attractive choices in designing low-output-power, low-cost, compact transmitters [4]. In this work, a novel current-reused architecture is used to implement a compact direct-modulation transmitter that delivers $0\,dBm$ to a $100\,\Omega$ differential load. Chapter II discusses in details the architecture of the

proposed current-reused direct-modulation transmitter, system-level issues including the interactions between LC tank loadings in different blocks and transmitter building blocks.

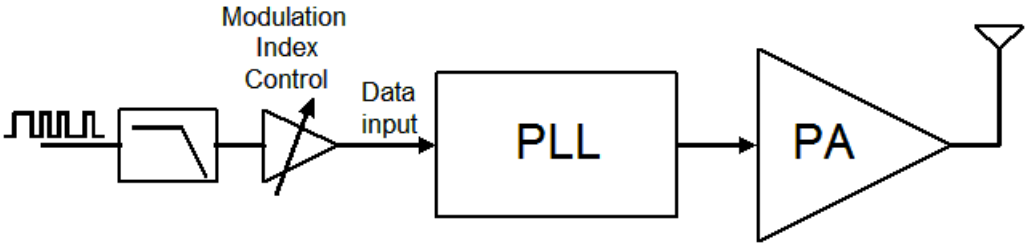


Fig. 3. General block diagram of direct-modulation transmitter architecture

C. Self-Tuning System

With recent advances in RF built-in self-test (BIST) combined with inexpensive CMOS technology, higher levels of integration of RF and baseband blocks with reduced cost is achievable [5, 6, 7, 8]. By eliminating expensive external automatic test equipment (ATE), and hence reducing test costs, these methods have helped to enhance production yield and hence reduce the price of radio devices at the consumer-end. Among these RF built-in self-test techniques, some [9, 10] tune the various resonant tanks in the transceivers from input-matching to load tanks of LNAs, VCOs and Power Amplifiers (PAs). Automatic tuning of resonant tank has a specific challenge of dealing with a non-monotonic (but single-peak) transfer function which makes producing the feedback correction signal somewhat difficult. In this work, a simple self-contained self-tuning system is proposed to tune the resonant tank of power amplifier to its optimum value. The tuning loop consists of a power detector followed by track and hold comparators and a state-machine. The decision-making algorithm in the state-machine overcomes the non-monotonicity of the tank transfer function. Figure 4 shows the block diagram of the proposed direct-modulation transmitter with self-tuning system. Design and implementation of the self-tuning system that automatically

calibrates resonating tank of power amplifier and its building blocks are presented in detail in Chapter II. The experimental results from the fabricated prototype chip in $0.18\mu CMOS$ technology are described in Chapter III.

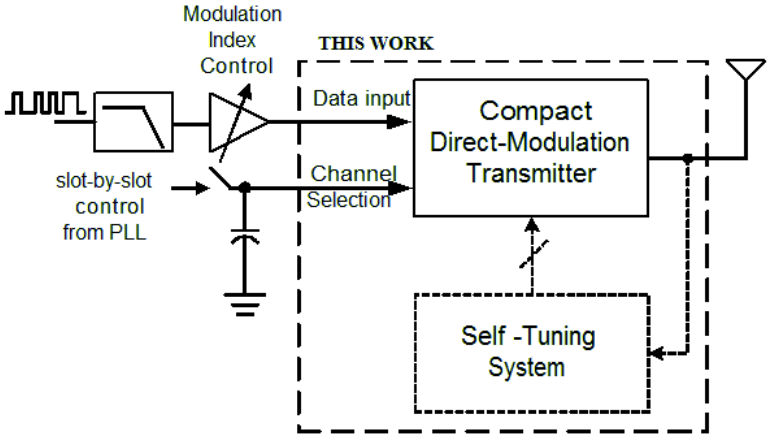


Fig. 4. Block-diagram of the proposed direct-modulation transmitter with self-tuning system

CHAPTER II

CURRENT-REUSED DIRECT-MODULATION TRANSMITTER WITH SELF-OPTIMIZATION FEEDBACK: ARCHITECTURE, THEORY AND BUILDING BLOCKS

A. Introduction

The rapid growth of radio transceivers and the prevalence of portable communication devices have driven demands for low-power, compact transceivers in low-cost CMOS processes. Especially in WPANs and sensor networks, a large number of devices must maintain wireless connectivity over a long period of time. Economic manufacturing of power-efficient and low-cost radio devices requires architecture and circuit optimization, as well as on-chip self calibration to obtain maximum output power with minimal wafer test cost.

Direct conversion and direct modulation transmitters' high levels of integration and reduced component counts suit them for low-cost applications [1, 2, 3]. Also, direct conversion simplifies and direct modulation practically obviates baseband processing by eliminating the DAC and upconversion mixer from the transmitter chain. These simplifications, along with constant-envelope modulation, result in more power-efficient system architectures. The use of FSK also simplifies (de)modulator implementation.

Power and area can be further conserved by co-designing circuit blocks, such as LNA/mixer [11], VCO/prescaler [12], and VCO/quadrature generator [13]. Recently, two classes of systems have arisen attempting to merge the PA and VCO: (i) oscillating PAs and (ii) cascaded VCO/PA. Method (i) employs RF feedback to destabilize the circuit, which although saving power and area, leads to frequency-control problems in addition to inflexible trade-offs between output power, operating frequency, and transistor sizes [14]. In this method the supply voltage and/or the DC bias of the output stage controls the output

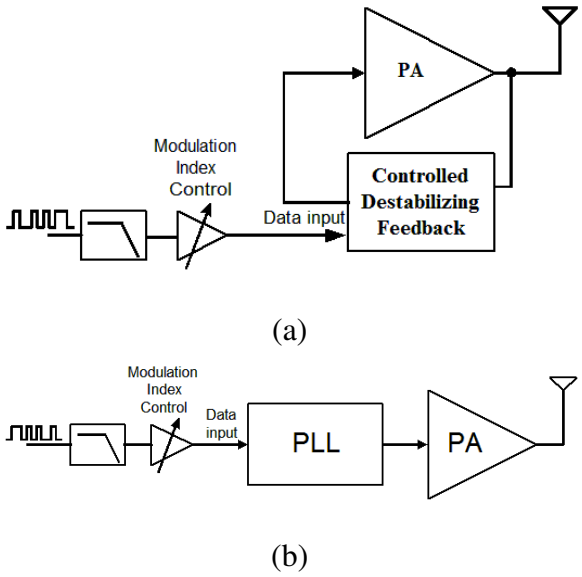


Fig. 5. Previous PVCO approaches: (a) method (i): power oscillator architecture, (b) method (ii): PA/VCO co-design

power, which in turn changes the frequency of operation. Method (ii) simply cascades the VCO and PA without any attempt to reuse current [15, 16, 17, 18, 19], as shown in Figure 5(b). This work proposes a merged, stacked PA/VCO (PVCO) structure to reuse current and save power, as illustrated by Figure 6 (a). Employing a current-reused configuration and utilizing FSK direct modulation yields a compact, low-power transmitter.

Also imperative for low-cost solutions is high manufacturing yield. Recent advances in RF built-in self test (BIST) have mitigated requirements for automatic test equipment (ATE), enhancing yield with on-chip tuning/trimming circuitry and diminishing overall test cost [5, 6, 7, 8]. These methods should be robust/transparent to the device under test, and have a small area/power footprint. Among these RF-BIST approaches, some have presented resonant-tank tuning techniques for LNAs' input matching and loads [9, 10]. Automatically tuninng a resonant task of calibrating a nonmonotonic (but single-peak) transfer function, complicating feedback-correction-signal generation. Previous approaches have either utilized an ADC and DSP [10], or have required two externally generated tones

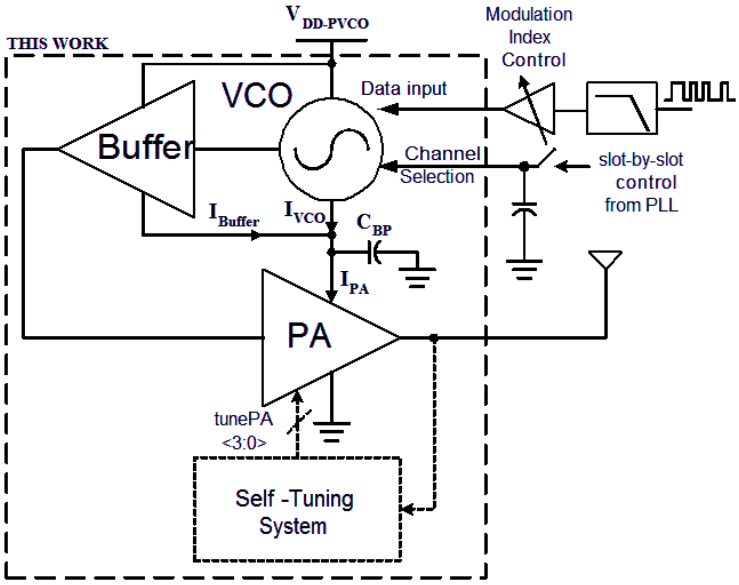
[9], one on each side of the desired resonant frequency. An ADC and DSP add considerable area/complexity to the design–particularly undesirable in simple, low-cost solutions. External generation of two tones requires expensive equipment, defeating the purpose of low-cost BIST.

In this work, a simple self-contained BIST technique tunes the resonant tank of power amplifier to its optimum value. The tuning loop consists of a power detector followed by track and hold comparators and a state-machine with a decision-making algorithm that overcomes the tank-transfer-function non-monotonicity. Also, because the free-running output tone of direct-modulation transmitter itself is used to self-tune the resonance tank of the power amplifier, the proposed technique requires no external signal source. Furthermore, the tuning loop finds the optimum value in real time, eliminating the need for an ADC or DSP and hence consuming little power. We experimentally demonstrate the proposed tuning algorithm for PA resonant-tank tuning; however, tuning-circuit core could conceivably be generalized to optimize other RF-block performance metrics with a single extremum as well.

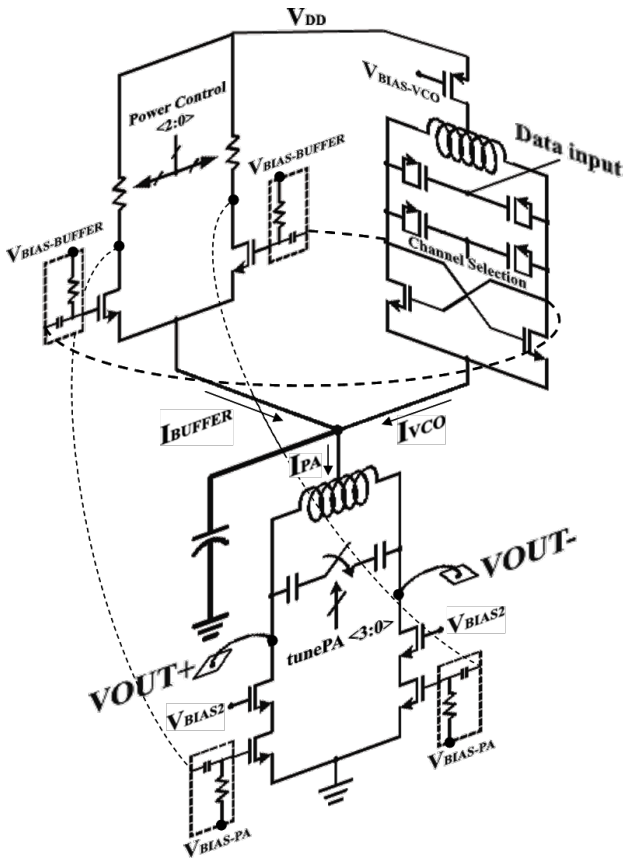
The work is organized as follows. Section B describes the general architecture of the PVCO. The merged PA/VCO blocks' circuit-level considerations are discussed in Section C, and the proposed self-tuning tuning circuitry along with power-detector design/analysis is described in Section D. Measurement results are presented in III Section A, and Section B concludes the paper.

B. Current-Reused Architecture

In low-power transmitters the pre-PA power consumption is often comparable with output power, so optimizing pre-PA power consumption can significantly improve overall efficiency. Therefore, to increase efficiency, the number/complexity of pre-PA blocks should



(a)



(b)

Fig. 6. Proposed current-reused transmitter: (a) architecture, (b) schematic

be minimized by, for instance, utilizing simple injection-locked or direct-modulation transmitter architectures [4]. This work employs direct-modulation and current reuse to design a compact, power-efficient transmitter. In contrast to previous approaches (Figure 5(b)), the current of the PA/VCO is shared to save power. Figure 6 (a) and (b) show the overall architecture and schematic of the proposed transmitter. The VCO is stacked on top of the power amplifier, and their common node is AC grounded with a large MOS capacitor. The DC level is set by the resistive buffer's gate bias. Both the VCO and PA have resonant tanks at their outputs tuned to the same frequency of operation. Section 1 elaborates on why the resistive buffer is necessary to reduce PA/VCO tank interaction and to attain a stable tone, proper gain, and favorable output-spectrum shape.

This architecture uses FSK direct modulation to save power and area by eliminating the baseband DAC and up-conversion mixers [15, 16, 18]. Furthermore, the prevalence of low-power FSK receiver demodulation techniques makes direct-modulation an attractive choice for low-power transmitter design [20]. Raw or encoded binary data are scaled by a modulation-index control amplifier, and are then applied to the VCO's data varactor, modulating its oscillating frequency. Depending on the application (e.g. Bluetooth), for spectral efficiency, data should pass through a pulse-shaping filter (e.g. Gaussian for Bluetooth) before modulation-index control. Another varactor is used to select the desired channel and could be intermittently connected to a PLL to improve phase noise/reduce temperature drift. The VCO output passes through a resistive buffer that isolates the VCO tank, provides gain, and delives the buffered signal to the output stage, which delivers > 0 dBm directly to a $100\ \Omega$ differential antenna without any external matching network. The self-tuning tuning loop adjusts a programmable capacitor array to trim the output stage's tank so as to achieve > 0 dBm output power. The tuning loop's algorithm and the power-detector theory of operation are discussed in Section D.

C. Merged PA/VCO Circuits

Two separate tanks tuned to almost the same frequency in consecutive stages can interact with each other due to reverse gain and degrade the frequency characteristics of both tanks. The common-source stage with resonant load in Figure 7(a) has a visible notch in its $|Z_{in}|$ due to C_{GD}. Hence, connecting two such stages in cascade, as shown in Figure 7(b), creates a null in the gain at the frequency of operation. Placing a resistive buffer between the resonant stages fixes the problem, as shown in Figure 7(c). Therefore, in designing the PVCO where the power amplifier follows the VCO, having a resistive buffer to isolate the PA's tank from the VCO's tank proves crucial. Section 1 elaborates on how these resonant effects arise, and Section 2 details circuit-level considerations.

1. LC Tank Impedance Interactions

To understand how reverse gain affects frequency behavior of each stage consider the input impedance Z_{in}[1] of a single stage with an LC tank load as shown in the Figure 7(a)(i):

$$Z_{in} = \left[sC_{GS} + \beta\left(g_m + Y_L\right)\right]^{-1}$$

where $\beta = \left(1 + \frac{Y_L}{sC_{GD}}\right)^{-1}$ (ideally zero) is a normalized interference factor indicating the degree to which Z_{in} depends on the LC-tank load admittance $Y_L = \frac{LCs^2 + \frac{L}{R}s + 1}{Ls}$ with a quality factor of $Q = \frac{R}{L\omega_0}$ at its resonance frequency. As can be inferred from the equation, when $\beta \to 0$, Z_{in} depends less and less on Y_L.

Figure 7(a)(ii) plots $|Z_{in}|$ for typical numerical values of a PA with an LC tank tuned to 2.4 GHz as tank Q varies from 0.75 to 15. As shown in the figure, the single stage presents a capacitive load except around the resonance frequency, where C_{GD} and the out-

[1] Since the PA is differential and hence the source node is a virtual ground, bondwire inductance has negligible effect on Z_{in}.

put tank create a notch. The Q of this notch corresponds directly to the Q of the output tank. Therefore, for higher quality-factor output tanks, the input impedance of the stage at the frequency of operation reduces, degrading the gain of the preceding stages. Figure 7(a)(iii) shows the magnitude of β (interference factor) vs. frequency for the same example. As can be seen from the figure, $|\beta(f)|$ is largest around the tank center frequency and grows (becomes worse) as Q increases.

To analyze the effect of this diminishing Z_{in} on preceding stage gain, consider the configuration in Figure 7(b)(i), where two stages with LC-tank loads tuned to the same frequency of operation are cascaded. These stages could be any narrowband RF blocks, such as an LNA, Mixer, VCO, or PA. Figure 7(b)(ii) and Figure 7(b)(iii) are typical examples of how Q_2 variation affects the impedance seen at the output of the first and second stages, respectively. As Q_2 grows, a null in $Z_{L1,2}$ forms, resulting in a malformed impedance frequency response and yielding two relatively low-Q peaks and a relatively high-Q zero at the desired frequency of operation.

In the PVCO architecture of Figure 5(b), because the PA could immediately follow the VCO, it is vital to protect the tank of the VCO from the impedance seen from the PA. In LC VCOs the tank quality factor and frequency characteristics determine the oscillation frequency and phase noise. Because in this case the cascaded tanks represent the VCO and PA, this undesired tank interaction would decrease the VCO tank's effective Q, deteriorating its phase noise and perturbing its oscillation frequency. Impedance interference of the VCO's LC tank seen from the PA output would also deform the frequency characteristics at the output of the PA (cf. Figure 7(b)(iii)), creating an undesired output spectrum.

To reduce the interference of the PA's tank on oscillator performance, a resistive buffer isolates the PA's and VCO's tanks. The resistive amplifier reduces the reverse gain from the PA to the VCO, alleviating impedance interactions and the resulting adverse performance effects. Figure 7(c)(i) depicts such a configuration. Intuitively speaking, the null formed

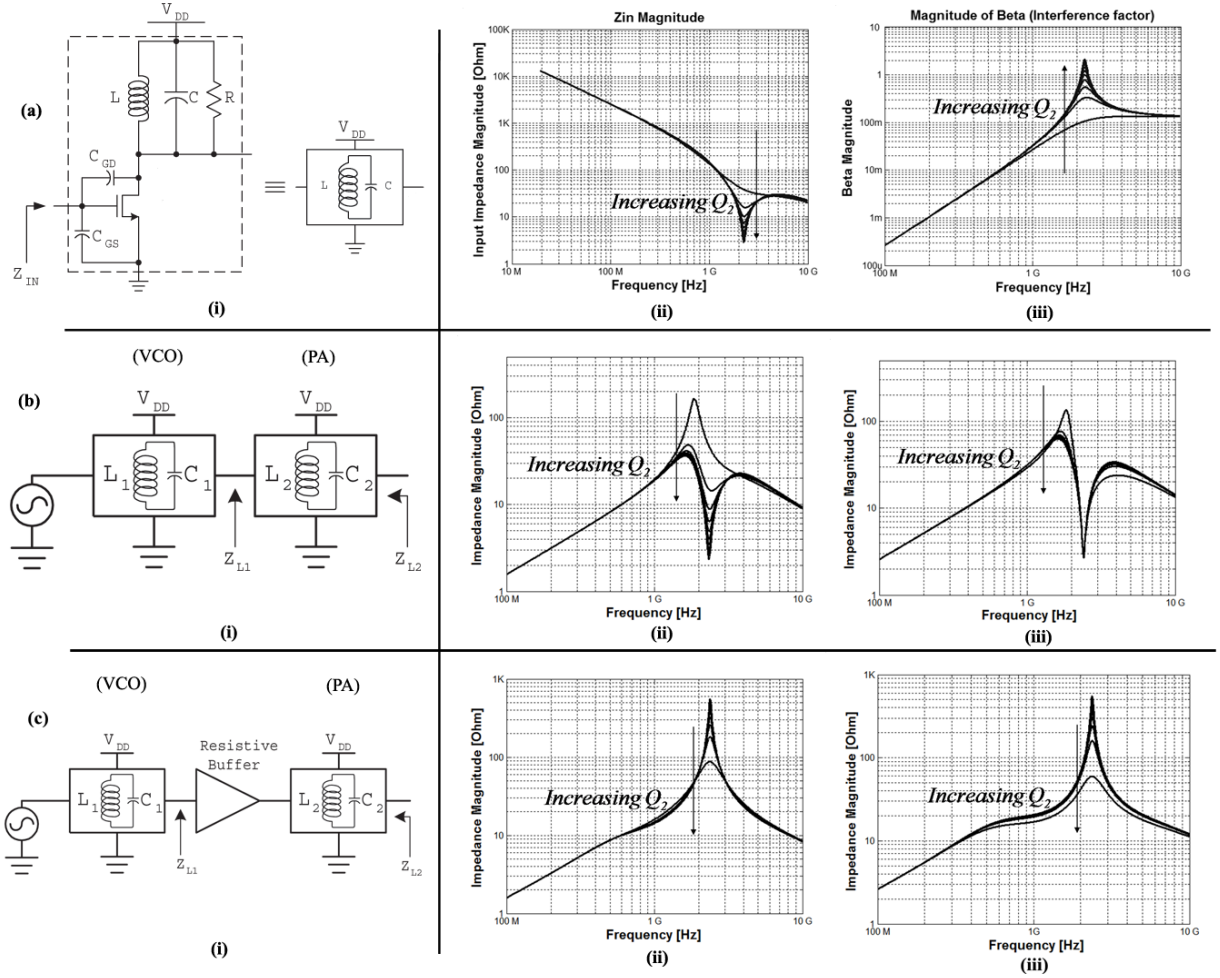


Fig. 7. (a)(i) Single common-source stage with LC tank load and magnitude of its (ii) input impedance and (iii) interference factor; (b)(i) two consecutive stages with tank loads and magnitude of impedances at (ii) the output of first stage and (iii) the output of last stage; (c)(i) a resistive buffer is placed between the two consecutive stages and magnitude of the impedance at (ii) the output of first stage and (iii) the output of last stage

in the load impedance of buffer is AC ground at the frequency of operation and hence first stage would only see the total capacitive parasitics of the resistive buffer, $C_{GS-Buffer} + C_{GD-Buffer}$. Figure 7(c)(ii) and (c)(iii) display the impedance magnitudes of both tanks at the outputs of the first and last stages in Figure 7(c)(i), where a resistive buffer is placed in between. As shown in Figure 7(c)(ii) and (iii), the resonance-frequency null does not appear in either response, and the quality factor of first stage's tank is a weaker function of Q_2, as desired.

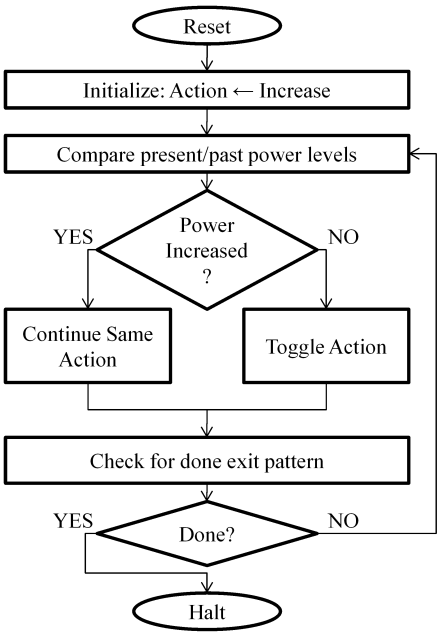
2. Circuit Design

This section briefly outlines the circuit-level design considerations. The VCO is an LC oscillator with NMOS cross-coupled transistors and a PMOS bias current to reduce flicker noise, as shown in Figure 6 (b). The LC tank comprises a symmetric, 3-turn, 2.83 nH inductor and MOS varactors to control the frequency. A smaller varactor is driven by data to generate the direct-modulated FSK signal, and a larger varactor, which is designed to be intermittently controlled by a PLL, compensates the frequency against process/temperature variations.

As displayed in Figure 6 (b), a resistive buffer is placed between the oscillator and PA output stage to (1) amplify the signal, (2) control the output power through a 3-bit resistive array at its load, (3) set the supply voltage of power amplifier through its gate DC bias, and (4) provide the necessary isolation between two tanks of the VCO and power amplifier. The output stage consists of a pseudo-differential cascode stage with an LC-tank load tuned to the frequency of operation. We designed the PA to drive a 100-Ω differential antenna directly without matching network to reduce the cost and the number of off-chip components; however, the addition of a matching network could further increase the transmitter's efficiency.

D. PA Self-Tuning Circuit

To maximize output power, the tuning loop centers the PA's resonant tank at the desired operating frequency. The self-tuning circuit adjusts the PA tank's 4-bit trim code, denoted **tunePA<3:0>**, as shown in Figure 6 (a), to compensate for PVT shifts and obtain maximum power. Since the output-power-vs.-tank-center-frequency curve is non-monotonic with a single maximum, we propose a novel tuning algorithm and simple circuit implementation that can find this maximum without need for a costly ADC or additional reference-tone generation. Figure 8 outlines the proposed algorithm: the key idea is that the algorithm monitors whether the output power improves as a result of the last **action**, or change in the tuning bits **tunePA<3:0>**. If the previous change in **tunePA<3:0>** reduced the output power, the loop reverses direction and automatically corrects itself. The tuning algorithm is robust in the sense that even if it begins changing the trim bits **tunePA<3:0>** in the wrong direction, the algorithm will automatically correct itself and still find the proper optimal power code. Upon passing the maximum power point, the trim codes will over- and undershoot the optimal code, at which point the termination logic senses the limit cycle, stores the optimal trim code, and deactivates the clock/trim circuitry to save power. Unlike more complicated optimization algorithms such as Newton-Raphson or Least-Mean-Squares, the proposed algorithm only checks the sign of the power change and requires no derivative/square/integration operations in the decision circuitry, simplifying implementation. Details of the state-machine logic and timing waveforms are discussed in Section 1. In addition, stable tuning-loop operation requires the power detector to generate a voltage monotonically related to the PA's RMS output level. Determining the sign of the slope of the power-detector output for a 2.4-GHz input is vital to ensure tuning-loop stability. Section 2 analyzes the power detector to gain insight into its frequency-dependent nonlinear behavior and, based on these principles, determines how to compensate for the frequency-



KEY

action	Description
Increase	**tunePA<3:0>**←**tunePA<3:0>**+1
Decrease	**tunePA<3:0>**←**tunePA<3:0>**−1

Fig. 8. PA self-tuning-system flowchart

dependent effects and ensure robust, reliable tuning-loop operation.

1. Tuning-Circuit Logic Operation

Figure 9(a) and (b) display the proposed algorithm implementation of Figure 8. The following procedure traces through the operation of this circuit implementation as displayed in the timing waveforms of Figure 10:

1. The power detector output V_{PN} settles to a steady-state value prior to $\mathbf{CLKB_{early}}$.
2. Oneshot $\mathbf{CLKB_{early}}$ triggers at the falling edge of **CLK**, and $V_{past} \leftarrow V_{present}$.
3. Once $V_{present}$'s old value is stored in V_{past}, then $V_{present} \leftarrow V_{PN}$ at $\mathbf{CLKB_{late}}$. This clock is a delayed version of $\mathbf{CLKB_{early}}$ where the delay is larger than the one-shot pulse width.
4. The state machine is triggered at the *rising* edge of **CLK** when the comparator output,

deltaPower, has settled. The signal **deltaPower** indicates whether the last adjustment increased or decreased the output power and updates **action** accordingly. (cf. also Figure 8).

5. The tank trim codes are modified shortly after the active edge of **CLK**. This event adjusts the PA's resonant tank, which triggers a change in the power-detector output. The T/H waits for a long delay (1/2 clock period) to ensure that the power-detector has settled before updating $V_{past/present}$ and repeating the above procedure.

The termination logic examines the past 4 values of **action** looking for the pattern 0110 to determine whether the optimal code has been reached, as illustrated in Figure 9(b) and Figure 10. Having found the optimal code, the tuning circuit deactivates itself to save power, preserves the optimal code, and sets the **done** bit.

2. Power Detector Design/Nonlinear-Freq. Dependent Analysis

For the tuning loop of Figure 9 to operate properly, the power detector output voltage should monotonically change (decrease in this case) with the power of the 2.4-GHz PA output. Figure 11 (a) and (b) show the conceptual and schematic diagrams of the power detector, respectively. This circuit constitutes a direct realization [21, 22] of an RMS detector, performing the squaring operation by (AC) shorting the RF/LO inputs and applying a low-pass filter at the output. Though static/DC nonlinear analysis may seem to indicate that V_{PP} in Figure 11 (a) and (b) would have a negative slope vs. input amplitude and seem to be the correct output, analysis of the frequency-dependent nonlinearity shows that V_{PN} instead has the proper slope (negative) at 2.4 GHz, but V_{PP} does not. As will be shown, the circuit is not symmetric, and $V_{PP/PN}$ [2] (plus-plus/plus-negative, respectively) have differ-

[2] N.B. $V_{PP/PN}$ are so named because the two FETs' gate voltages in the path(s) from $V_{PP/PN}$ to the tail element have the same phase/opposite phase, respectively.

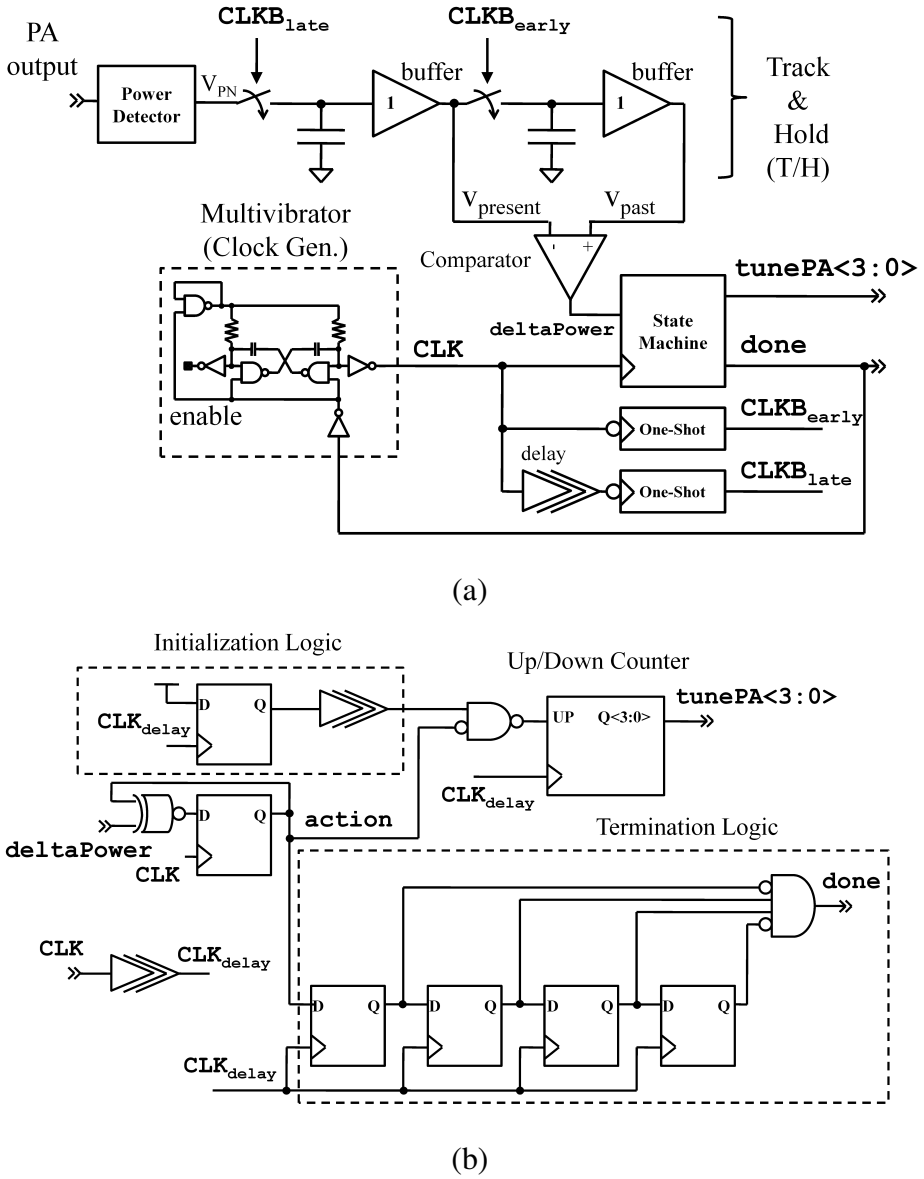


Fig. 9. PA self-tuning system: (a) overall architecture and (b) state-machine implementation

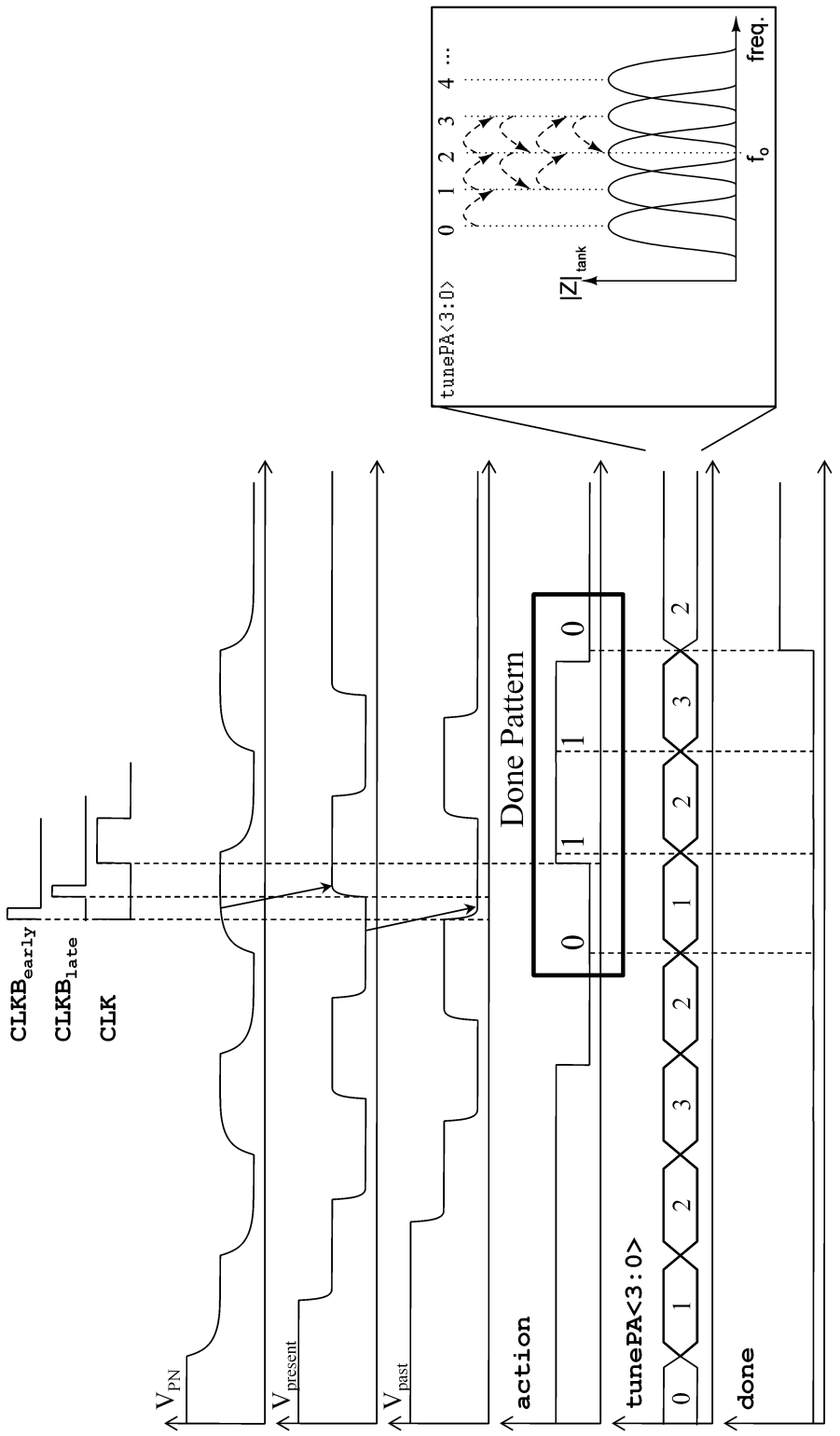


Fig. 10. Self-tuning circuit's conceptual tuning waveforms; inset: conceptual tank-tuning sequence

ent responses vs. input amplitude. Because incorrect slope can destabilize the tuning loop, understanding how and why this change with respect to frequency occurs is essential. It is also the authors' hope that an improved understanding of the Gilbert-cell-based power detector will allow to extend the useful frequencies of operation for similar RMS detectors in older technologies by recommending circuit compensation techniques based on the principles presented in this analysis.

As mentioned above, we chose direct realization for simplicity to have a low power, high-speed solution. Because the PA output power varies by around a decade, dynamic range is not much of an issue. Also, our proposed tuning loop only requires monotonicity w.r.t. output RMS level, so accuracy/crest-factor requirements are also relaxed. The input $V_{IN}^{P} - V_{IN}^{N} = V_A \cos(\omega t)$ of the structure in Figure 11 (b) is driven by the PA output. Depending on the operation (saturation/deep triode) of M_{TAIL}, the structure in Figure 11 (b) will behave fully differentially (FD) or pseudo-differentially (PD), respectively. Figure 12 displays the simulated detector outputs $V_{PP/PN}$ vs. input sinusoidal amplitude V_A as frequency varies from 10 MHz to 2.4 GHz for both FD and PD modes of operation. As evident in the figure, the outputs $V_{PP/PN}$ are asymmetric, and the signs of their slopes change with frequency, especially for the FD case. The following sections develop intuitive and analytical insight into this frequency dependent behavior as well as how to compensate for it at the circuit level.

a. Low-Frequency Operation

To understand the response for small sinusoidal input voltages, consider a small DC offset δ as shown in Figure 11 (c). First, suppose that $\delta > 0$, for which M_{BTM1} provides more current than M_{BTM2}, and M_{PP1}/M_{PN1} steer that current away from V_{PN} and towards V_{PP}, as illustrated by the dashed line in Figure 11 (c). On the other hand if $\delta < 0$, then M_{BTM2} provides the greater current, which is again steered to V_{PP}, this time by the M_{PP2}/M_{PN2}

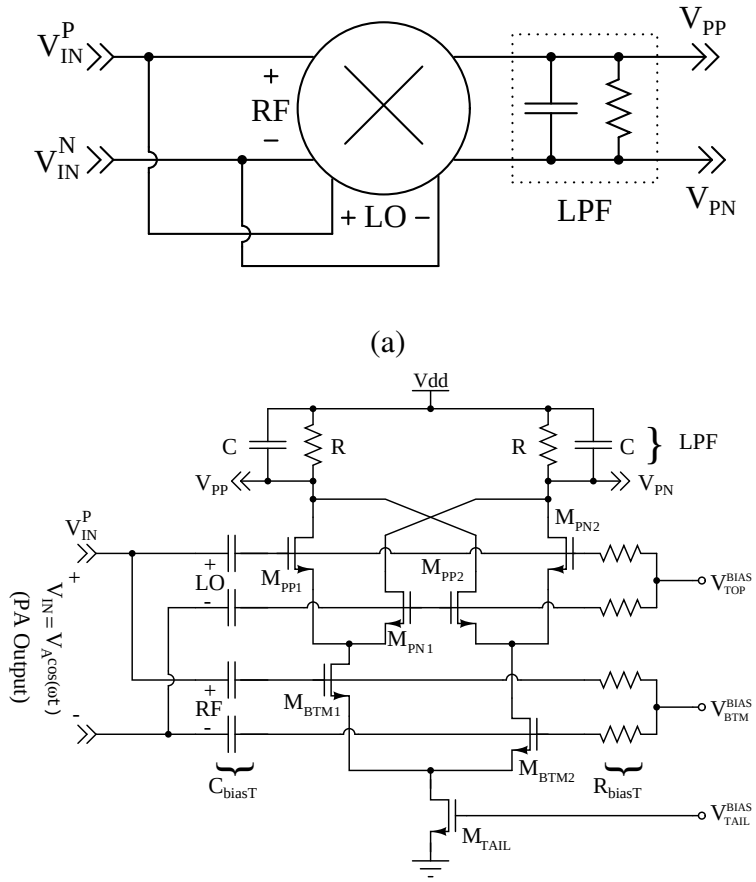
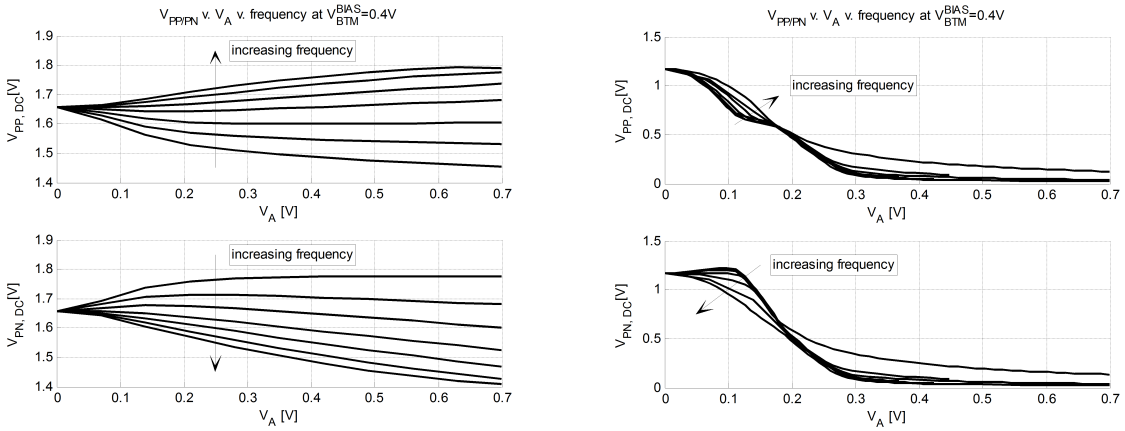


Fig. 11. Gilbert cell modified to act as power detector: (a) conceptual, (b) schematic, (c) current steering



(a) (b)

Fig. 12. Simulated $V_{PP/PN}$ vs. V_A vs. frequency for (a) FD-Mode and (b) PD-Mode

source-coupled pair, as shown by the dotted line in Figure 11 (c). For *both positive and negative* small DC offsets, $V_{PP/PN}$ reduces/increases, respectively, so it follows that when a sine wave $V_A \cos(\omega t) = V_{IN}^P - V_{IN}^N$ is applied, then as V_A increases, the output DC level of $V_{PP/PN}$ will initially drop/rise, respectively. This initial $V_{PP/PN}$ behavior is described analytically by assuming an ideal LPF at the output and obtaining the DC component from power-series analysis[3]:

$$V_{PP/PN}^{DC} = V_{DD} - R \sum_{k=0}^{\infty} \underbrace{\frac{f_{PP/PN}^{(2k)}(0)}{(2k)!}}_{H_{2k}} \binom{2k}{k} \left(\frac{V_A}{2}\right)^{2k} \tag{2.1}$$

where $f_{PP/PN}(V_d)$ represent the Gilbert-cell nonlinear output currents as a function of input differential voltage V_d, and are given in Table I for the case of square-law behavior. When the V_A^2 term dominates, the output represents a function of the PA's RMS output level. In the PD case, this low-frequency behavior is also evident in region (i) of Figure 13(a).

For larger perturbations, the FD-mode voltages $V_{PP/PN}$ continue monotonically w.r.t.

[3]N.B. this (Taylor) power series represents the memoryless-network special case of a Volterra series [23]. See Sections b and c for the general frequency-dependent case.

Table I. Gilbert cell static nonlinear transfer characteristics

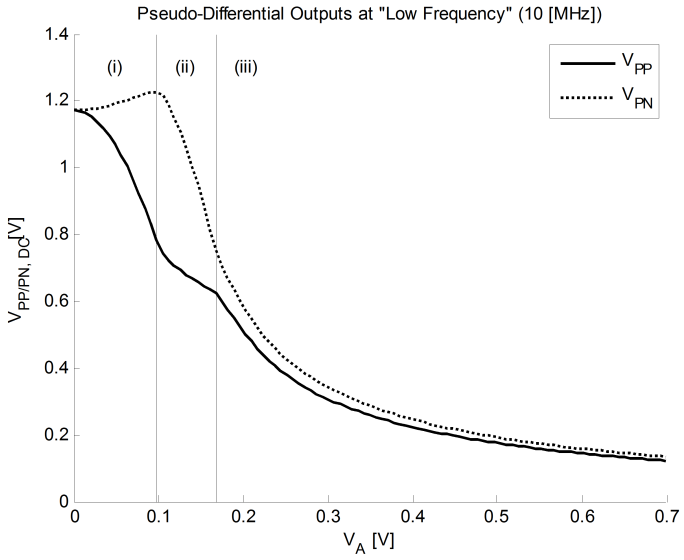
	Fully Differential (FD)	Pseudo Differential (PD)
$f_{PP/PN}(V_d)$	$I_{SS}\left[\frac{1}{2} \pm \frac{x\sqrt{1-x^2}}{4}\left(h(x)-h(-x)\right)\right]$	$\beta_{BTM}V_{dsatBTM}^2\left[\frac{1}{2}+\frac{x^2}{8} \pm \frac{x}{2\sqrt{3}}\left[h(x)-h(-x)\right]\right]$
$h(x)$	$\sqrt{1+\frac{x}{\sqrt{1-x^2}}}$	$\sqrt{1-\left(\frac{x-2/3}{4/3}\right)^2}$
$V_{dsatBTM}$	$\sqrt{\frac{I_{SS}}{\beta_{BTM}}}$	$V_{BTM}^{BIAS}-V_T$

where (i) $x \equiv V_d/V_{dsatBTM}$; (ii) above derived assuming $M_{BTM1,2}$ has twice the width of $M_{PP1,2}$/$M_{PN1,2}$: $\beta_{BTM} = 2\beta_{TOP} = 2\beta$; (iii) $I_{SS} = I_D$ of M_{TAIL}

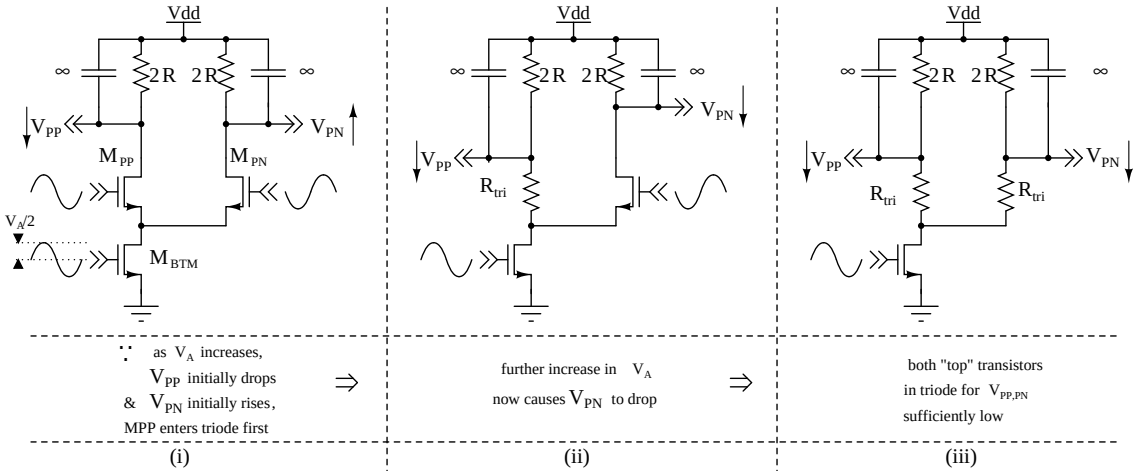
V_A, as shown in Figure 12. However, the PD-mode V_{PN} response is clearly non-monotonic, as emphasized in Figure 13(a). It can be shown that this particular configuration of non-linear circuits may be analyzed with a half circuit because the harmonic content from the two halves do not intermodulate with each other. Figure 13(b) details the half circuit's behavior in the three different regions of Figure 13(a). At the end of region (i), when V_{PP} is sufficiently low, transistor M_{PP} enters triode for a larger and larger fraction of each cycle of applied sinusoid, reducing its time-average g_m and r_{ds}. This change allows M_{PN} (still in saturation) to steer more of the current from M_{BTM} to V_{PN}, whose voltage drops as a result. The total current $I_{PP} + I_{PN}$ rises in PD operation (cf. also the PD equations in Table I), even though the ratio I_{PP}/I_{PN} reduces due to the current steering toward the V_{PN} node. Thus, voltage V_{PP} continues to drop in region (ii), albeit at a lower rate than V_{PN}. Eventually, V_{PN} drops low enough that M_{PN} also begins to enter triode. This point is the boundary of region (iii), indicated in Figure 13(a)/(b), where both outputs are roughly symmetric.

b. High-Frequency Operation

As shown in Figure 12, $V_{PP/PN}$ switch direction as frequency changes for both FD/PD cases. The change is more severe in the FD case, as the two output curves completely trade places as frequency increases. At higher frequencies, C_{GD} partially bypasses the bottom FET and shifts the phase of the current injected into the top transistors' source node(s) with respect to the phase of the upper transistors' gate voltages. The phase shift interferes with the mixing action, decreasing/increasing the DC components of $I_{PP/PN}$, respectively. This action is intuitively what causes the $V_{PP/PN}$ responses to trade places at higher frequencies. This C_{GD} effect could be mitigated by connecting cross-coupled capacitors to generate negative C_{GD}, or by using the V_{PN} output instead of V_{PP} to get the desired high-frequency slope. We choose the latter approach for simplicity and to save area.

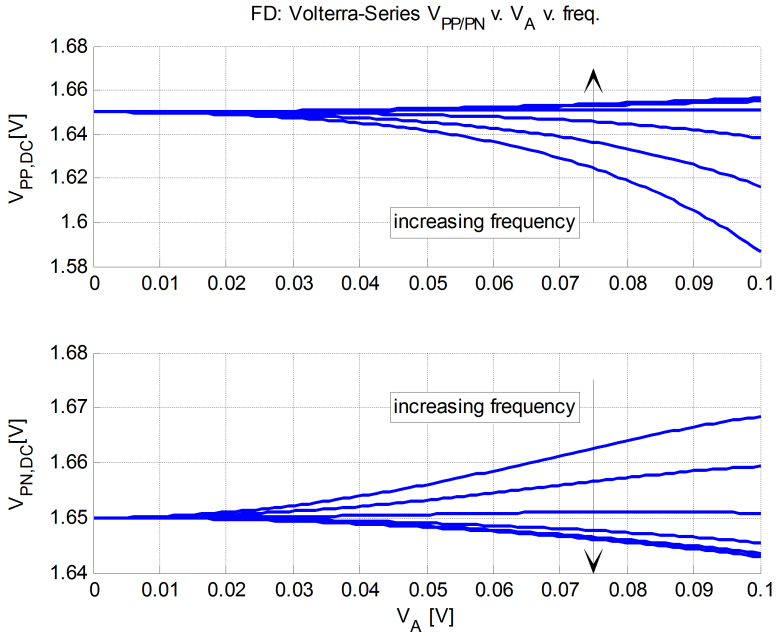


(a)

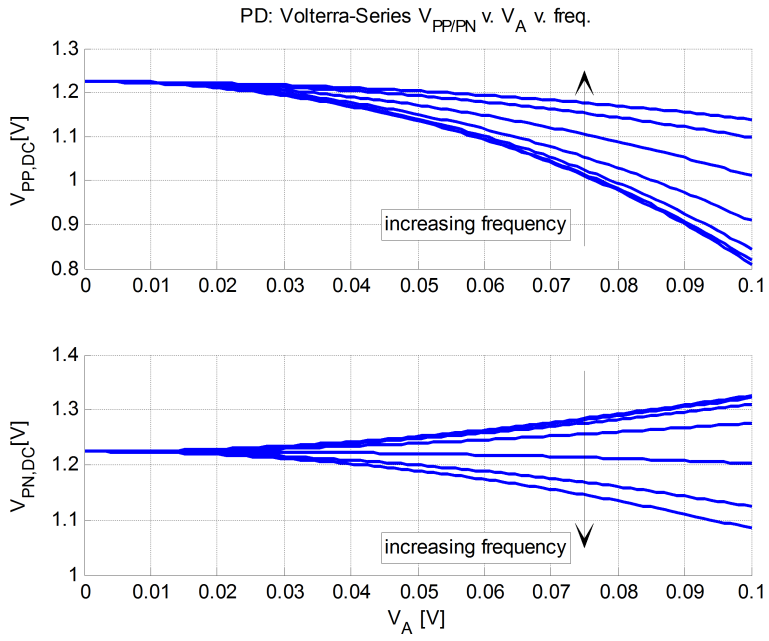


(b)

Fig. 13. Power-detector pseudo-differential regions of operation: (a) waveforms, (b) conceptual half circuits



(a)



(b)

Fig. 14. Volterra-series-calculated $V_{PP/PN}$ vs. V_A vs. frequency for (a) FD- and (b) PD–Mode

The effect of C_{GD} on $V_{PP/PN}$ response shape can be obtained analytically by applying Volterra series analysis, as detailed in the next section. Figure 14 plots the results of this analysis for small to moderate voltages, for which the system remains weakly nonlinear and hence for which Volterra analysis is valid [24, 25]. We observe the same trends in the analytical plot of Figure 14 as in the SPICE BSIM3 simulations of Figure 12.

c. Volterra-Series Analysis of Power Detector

This section derives the nonlinear, frequency-dependent behavior of the power-detector outputs $V_{PP/PN}$ using Volterra Analysis. Table II lists the nonlinear differential equations for both the FD and PD modes. To keep the equations tractable, we assume a square-law model and that all transistors remain in saturation. Hence, the analysis is valid for relatively small inputs s.t. the system remains "weakly nonlinear" [24]. It can be shown that the nonlinear conduction current of M_{BTM} is relatively independent of frequency despite appreciable C_{GS}.

Table III lists the $V_x(t)$ kernels from applying a Volterra analysis to the model described in Table II, where $V_x(t) \equiv V_{TOP}^{BIAS} - V_S(t) - V_T$ is chosen for ease of analysis. To simplify the expressions, we assumed $C_{GD/GS}$ are roughly constant, and that g_m is the main source of nonlinearity. For a single-tone sinusoidal input $V_d(t) = V_A \cos(\omega t)$, the $L^{\text{th}}-$harmonic component is given by [26]:

$$V_x(t) = \sum_{L=-\infty}^{\infty} V_{x,L} e^{jL\omega t};\ V_{x,L} \equiv \left[\sum_{n=L}^{\infty} \binom{n}{\frac{n+L}{2}\ \frac{n-L}{2}} \left(\frac{V_A}{2}\right)^n H_n(\underbrace{\omega, \ldots}_{\frac{n+L}{2}\text{ terms}}, \underbrace{-\omega, \ldots}_{\frac{n-L}{2}\text{ terms}}) \right] \quad (2.2)$$

where the sum is taken over even/odd n if L is even/odd, respectively. Hence,

$$V_{PP/PN}^{DC} = V_{DD} - 2RI_{PP/PN}^{DC} = V_{DD} - \beta R \left[|V_{x,0}|^2 + 2|V_{x,1}|^2 + 2|V_{x,2}|^2 + \frac{V_A^2}{8} \pm |V_{x,1}| V_A \cos(\angle V_{x,1}) \right] \quad (2.3)$$

Table II. FD/PD system differential equations

	Fully Differential (FD)	Pseudo Differential (PD)
System Differential Equation	$2(C_{gs}+C_{gd})\frac{dV_x(t)}{dt}+C_{gd}\frac{dV_d(t)}{dt}$	$2(C_{gd}+C_{gs})\frac{dV_x(t)}{dt}+C_{gd}\frac{dV_d(t)}{dt}$
	$+\quad \beta\left[V_x^2(t)+\frac{1}{4}V_d^2(t)\right]$	$+\quad \beta\left[V_x^2(t)+\cancel{\frac{1}{4}V_d^2(t)}\right]$
	$\approx\quad \frac{I_{SS}}{2}+\frac{g_{mBTM}}{2}V_d(t)\left(1-\frac{V_d^2}{8V_{dsatBTM}^2}\right)$	$=\quad \beta\left[V_{dsatBTM}^2+V_{dsatBTM}V_d(t)+\cancel{\frac{1}{4}V_d^2(t)}\right]$
Drain-Current Equation	$I_{PP/PN}(t)=\frac{\beta}{2}\left(V_x(t)\pm\frac{V_d(t)}{2}\right)^2+\underbrace{C_{gd}\frac{d}{dt}\left[V_{PP/PN}(t)\pm\frac{V_d(t)}{2}\right]}_{\text{can neglect when computing DC component}}$	
$V_x(t)$	$V_{TOP}^{BIAS}-V_T-V_S(t)$	
$V_S(t)$	voltage at source of M_{PP1}/M_{PN1} in Figure 11 (b)	
$V_{dsatBTM}$	$\sqrt{I_{SS}/\beta_{BTM}}$	$V_{BTM}^{BIAS}-V_T$
g_{mBTM}	$\sqrt{\beta_{BTM}I_{SS}}$	$\beta_{BTM}\left(V_{BTM}^{BIAS}-V_T\right)$

N.B. Assume bottom transistors 2x top because handle 2x current; Hence $\beta_{BTM}=2\beta_{TOP}=2\beta=2\mu_nC_{ox}\frac{W}{L}$; $C_{gd/gs}^{BTM}=2C_{gd/gs}^{TOP}=2C_{gd/gs}$

Note that all terms in (2.3) within the brackets are positive, except $|V_{x,1}|\, V_A \cos(\angle V_{x,1})$, whose sign can change with frequency. This term is analytically what causes the curves to trade direction: had the angle $\angle V_{x,1}$ not changed with frequency, then the change would not have been as pronounced. As seen in Table II, the difference between the FD/PD cases arises chiefly because even harmonics from M_{PP}/M_{PN} cancel those from M_{BTM} in PD but not in FD operation. FD mode's lack of cancellation augments the effect of frequency-dependent term $|V_{x,1}|V_A \cos(\angle V_{x,1})$ and thus causes the $V_{PP/PN}$ curves to trade places as frequency increases.

3. Remarks on Circuit-Level Considerations

This section outlines tuning-loop circuit-level issues. The buffers of the T/H in Figure 9 (a) are implemented with a single-stage differential pair in unity-feedback with NMOS input transistors and a PMOS current mirror load. The NMOS diff. pair/PMOS current mirror are sized to have low/high V_{dsat}, respectively, to minimize random offset [27]. Furthermore, the transistors are sized up and laid out in common centroid/interdigitized fashion with periphery dummies to improve matching. The buffer's R_{out} and slew rate are set so the track and hold can settle within 80% of the worst-case pulse width of the $\texttt{CLKB}_{\texttt{early/late}}$ one-shot signals over process corners. T-gates form the T/H switches and include 1/2-sized dummy switches to reduce charge injection [28]. We place a dummy switch clocked by $\texttt{CLKB}_{\texttt{early}}$ and a dummy hold capacitor at the output of V_{past} so V_{past} and $V_{present}$ nodes see identical parasitics and switching events.

The state machine consists of static CMOS logic gates. We chose a relatively low tuning-clock frequency ($\approx$ 1MHz) so that (1) the gate design is relatively relaxed and (2) the power detector has sufficient time to settle in half a clock period. The signal lines were shielded from the routed clock lines as much as possible, and the remaining digital

Table III. Volterra kernels for $V_x(t)$

	Fully Differential (FD)	Pseudo Differential (PD)
H_0	$V_{dsatBTM}$	$V_{dsatBTM}$
$H_1(\omega)$	$\frac{g_{mBTM}/2-j\omega C_{gd}}{2f(j\omega)}$	$\frac{g_{mBTM}/2-j\omega C_{gd}}{2f(j\omega)}$
$H_2(\omega_1,\,\omega_2)$	$\frac{-\beta[H_1(\omega_1)H_1(\omega_2)+1/4]}{\binom{2}{1\,1}f(j[\omega_1+\omega_2])}$	$\frac{-\beta H_1(\omega_1)H_1(\omega_2)}{\binom{2}{1\,1}f(j[\omega_1+\omega_2])}$
$H_3(\omega_1,\,\omega_2,\,\omega_3)$	$\frac{-\binom{2}{1\,1}\beta g(\omega_1,\,\omega_2,\,\omega_3)+\binom{3}{1\,1\,1}\frac{g_{mBTM}}{16V_{dsatBTM}^2}}{\binom{3}{1\,1\,1}f\left(j\left[\omega_1+\omega_2+\omega_3\right]\right)}$	$\frac{-\binom{2}{1\,1}\beta g(\omega_1,\,\omega_2,\,\omega_3)}{\binom{3}{1\,1\,1}f\left(j\left[\omega_1+\omega_2+\omega_3\right]\right)}$
$f(j\omega)$	$\beta H_0+j\omega(C_{gd}+C_{gs})$	
$g(\omega_1,\,\omega_2,\,\omega_3)$	$H_1(\omega_1)H_2(\omega_2,\,\omega_3)+H_1(\omega_2)H_2(\omega_1,\,\omega_3)+H_1(\omega_3)H_2(\omega_1,\,\omega_2)$	

circuitry is isolated from the analog/RF portion as much as possible. The PD mode of power-detector operation is selected to have larger gain/output range. We selected a CMOS astable multivibrator as the internal digital clock for simplicity and area efficiency, as shown in Figure 9 (a).

CHAPTER III

CURRENT-REUSED DIRECT-MODULATION TRANSMITTER WITH SELF-OPTIMIZATION FEEDBACK: MEASUREMENT RESULTS

A. Measurement Results

The PVCO-based compact transmitter was fabricated in TSMC 0.18μm CMOS, occupies 0.7 mm^2 (TX) and 0.1 mm^2 (tuning loop), was packaged in a QFN48 package, and was measured on an FR4 PCB. Figure 15 displays the die micrograph. Note that the inductors were placed as far away from one another as possible while still allowing the digital circuitry to be reasonably isolated from the RF circuitry. The transmitter consumes 22.9 mA from a 2.2-V supply. While active, the tuning loop consumes 600μA; however, the tuning loop is designed to deactivate once the optimal code is found.

As shown in Figure 16, the measured VCO frequency tuning range is about 500 MHz which is enough to cover the ISM band with sufficient margin for process/temperature variations. Figure 17 displays the free-running phase noise of the VCO, which achieves -108 dBc/Hz at 1 MHz offset. The phase noise is measured at the PA output, as the VCO's internal nodes are not brought out to a pin. Figure 18 shows the unmodulated PA output spectrum, where $P_{out} = 0.164$ dBm. Figure 19 shows how the PA output power is adjusted

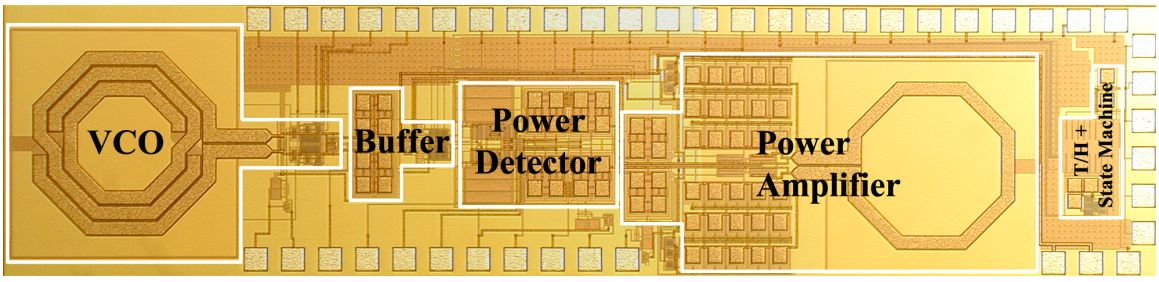


Fig. 15. PVCO chip micrograph

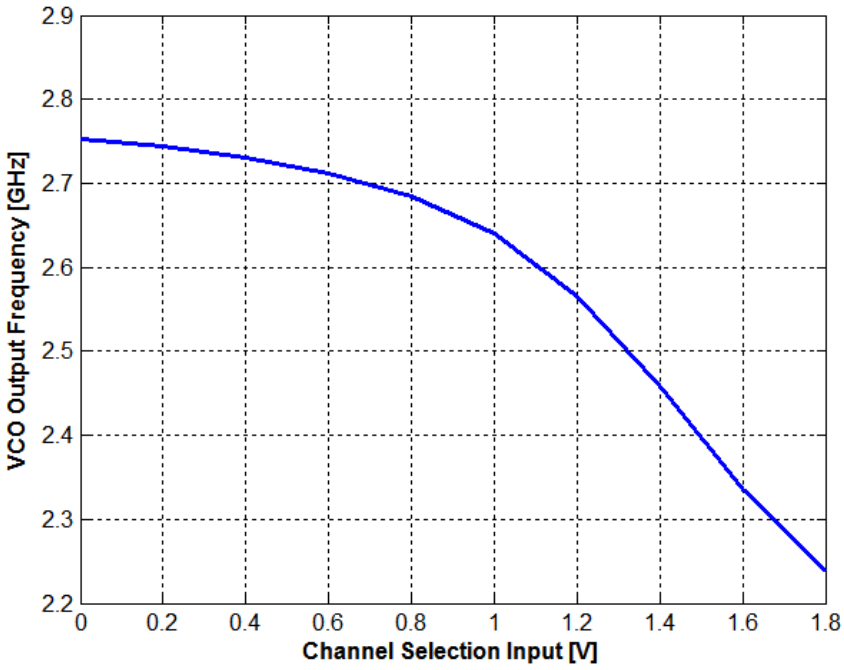


Fig. 16. Measured VCO channel-select tuning range

by the three-bit control word applied to the resistive buffer. To measure the output power of the transmitter accurately, the PA's output is double terminated at the far and near ends, as shown in Figure 20, and the losses of the bias-T, balun, and cabling have been deembedded.

To verify transmitter operation, we connect the output of the PVCO to a vector signal analyzer and apply 1 Mbps PRBS $(2^9 - 1)$ data through a Gaussian filter with BT=0.5. Figure 21 and Figure 22 display the modulated PSD and corresponding eye diagram, respectively, demonstrating the successful transmission/demodulation of 1 Mbps data on a 2.4 GHz carrier.

Figure 23(a) displays the measured tuning waveforms, and Figure 23(b) plots PA output power and power-detector output voltage vs. trim bits. In Figure 23(a), the trim-bit code **`tunePA<3:0>`** traverses the limit cycle twice before the **`done`** bit is set and the state machine terminates, selecting the optimal power trim code (0010=2 in this case). The manual measurements of output power vs. trim bits in Figure 23(b) verify that the hardware tuning

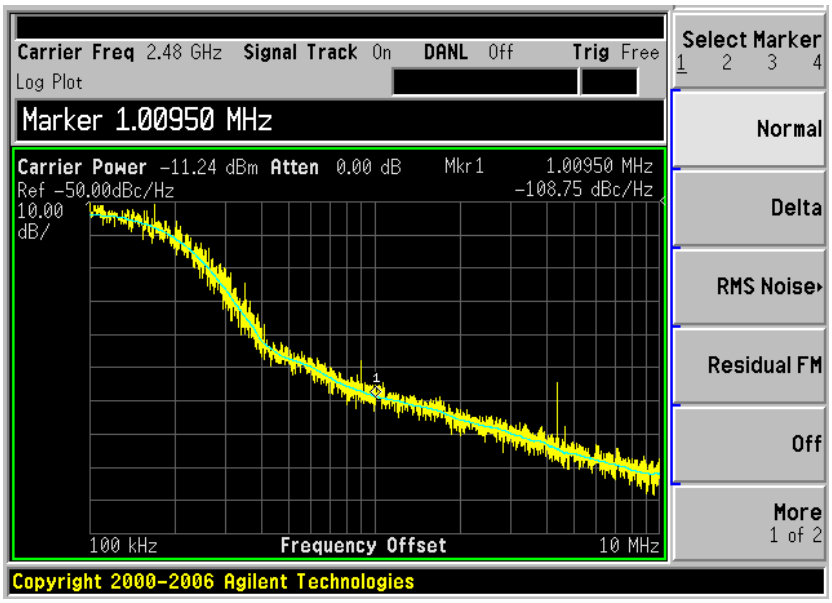


Fig. 17. Measured free-running VCO phase noise at the output of PA

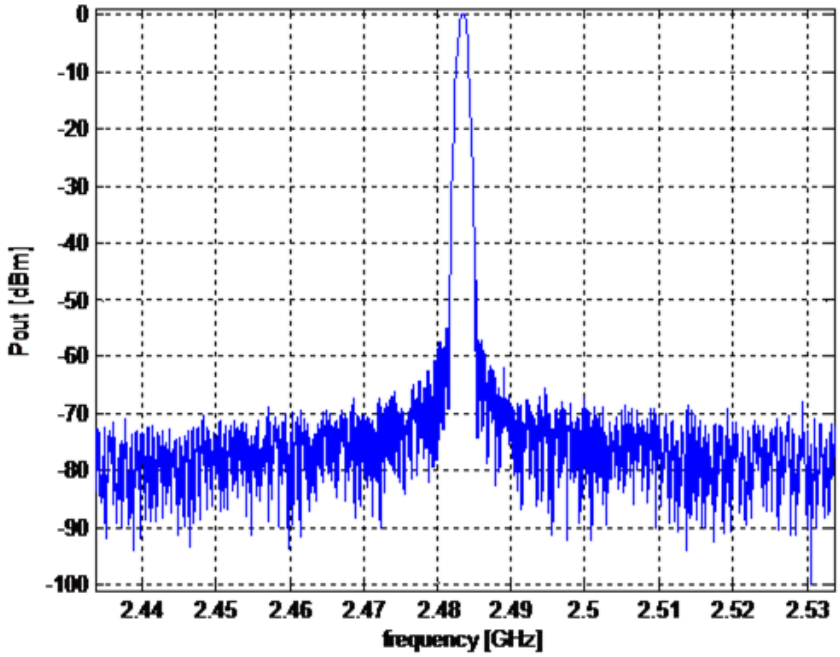


Fig. 18. Measured PA unmodulated output spectrum

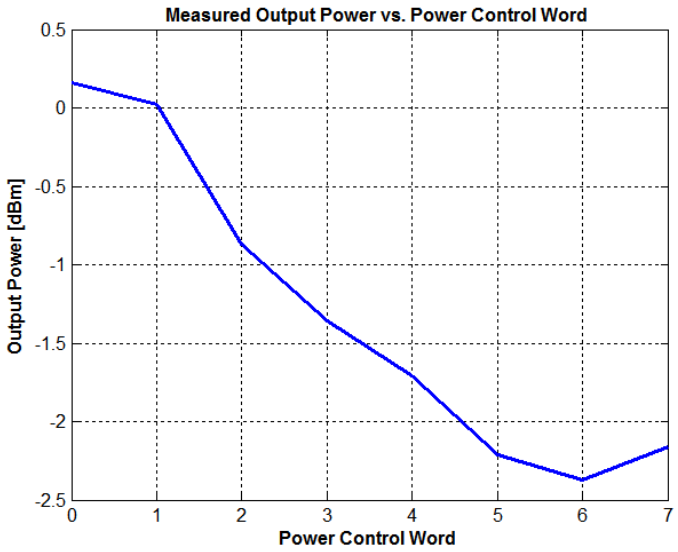


Fig. 19. Measured PA power adjustment

circuit's output trim code **tunePA<3:0>**=0010 indeed corresponds to maximum output power. Figure 24 displays the output power with and without the self-tuning circuitry activated. Tuning the tank does not actually change the VCO output frequency; in this figure, the curves have been purposely shifted for clarity of viewing. Adjusting the tank-tuning bits within their full range would result in >4 dB increase in output power. Furthermore, note that in our case, the PA directly drives a differential $100-\Omega$ load to avoid the complexity of an off-chip matching network, so the LC tank has low Q. In higher-Q tanks, even greater increases in tuned output power are expected.

Also, the measured behavior of V_{PN} (the power-detector output) is displayed in Figure 25, demonstrating a monotonic, negative-slope response as desired. The power-detector response was measured by applying a slowly-varying amplitude-modulated sine wave to the power detector's inputs and capturing the V_{PN} waveform on an oscilloscope.

Table IV compares this work's measured performance to those of recently published similar works in the literature. Our packaged solution with no special external resonators or off-chip inductors achieves comparable or superior performance in terms of average

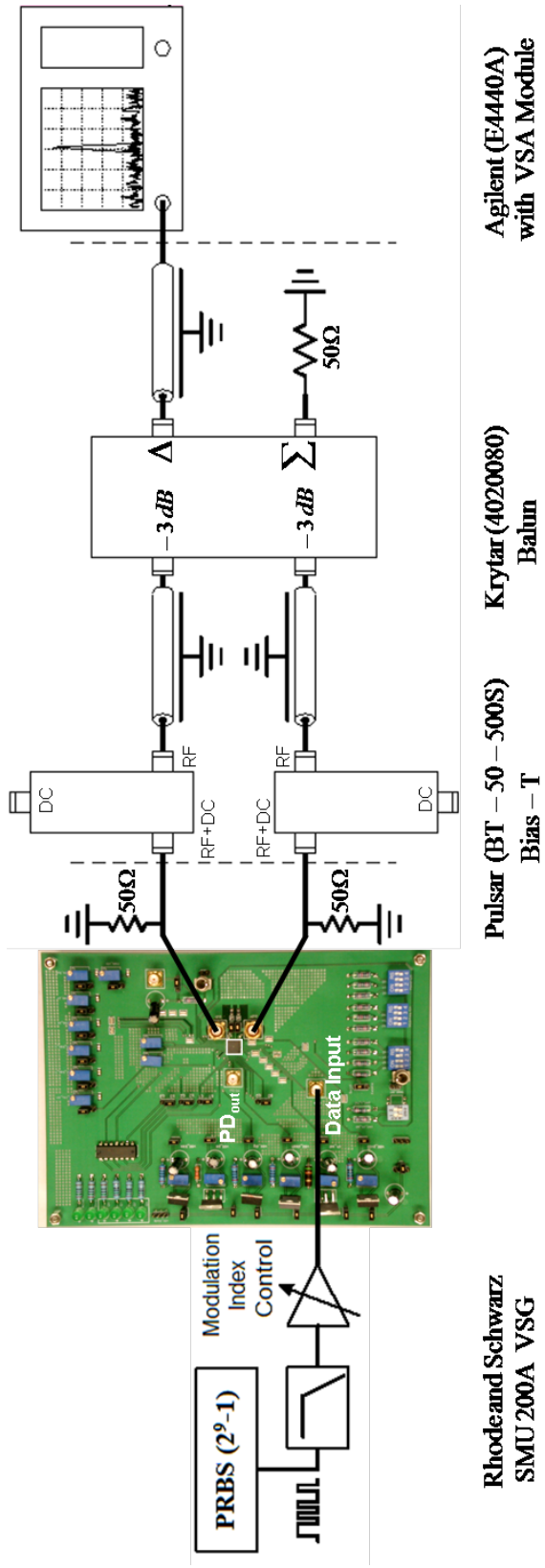


Fig. 20. PVCO measurement setup

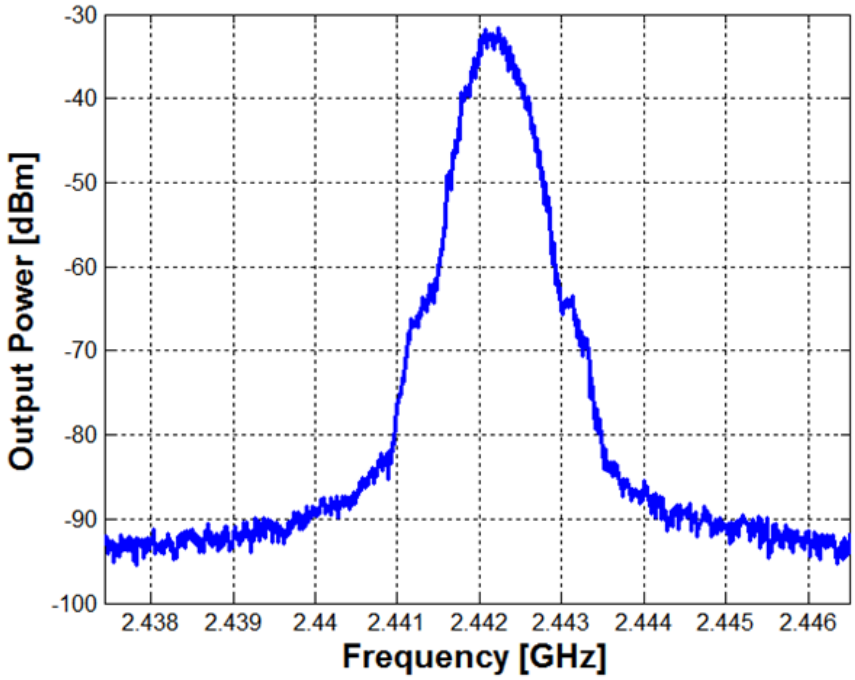


Fig. 21. Measured GFSK-modulated PA output spectrum

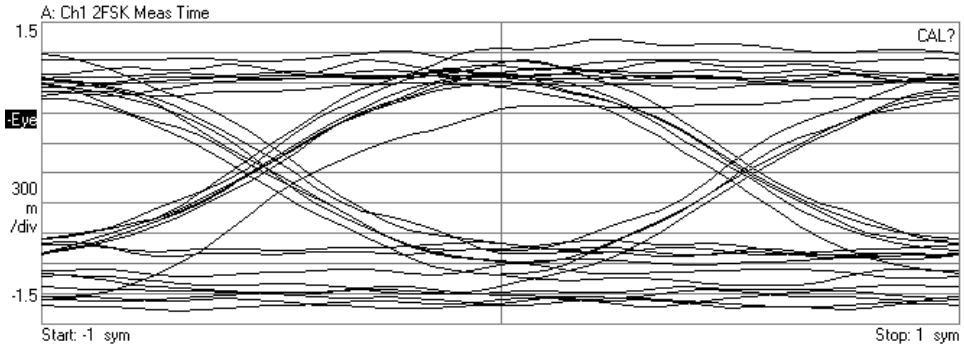
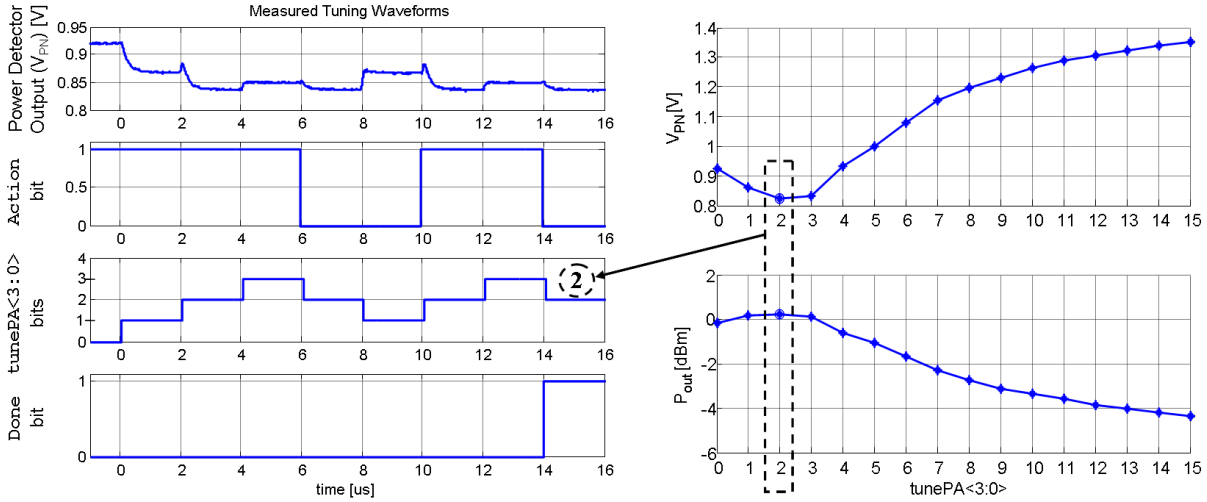


Fig. 22. Measured eye diagram



N.B. Power-detector output V_{PN} raw from oscilloscope

Fig. 23. Self-tuning circuit: (a) measured internal waveforms, (b) measured output power/power-detector output voltage vs. bits

transmitter power (P_{TX}^{avg}) and output power. Among those previous works without special customized off-chip resonators or chip-on-board (COB) assemblies, we attain the best average transmitter power, which is defined as the power the transmitter would consume when transmitting 1 packet/sec., 1000 bits/packet [29].

As none of the works in Table IV have commensurate self-calibration circuitry, we compare the performance of the self-tuning circuit to similar reported tuning works in Table V. The proposed tuning scheme is simpler; requires no external reference or any on-chip ADC/DSP; and successfully optimizes the output power of a 2.4-GHz PA.

B. Conclusion

The work explained in the Chapters II and III demonstrated a proposed stacked CMOS PA/VCO architecture with on-chip automatic-tuning in package at 2.4 GHz and with > 0 dBm output power.

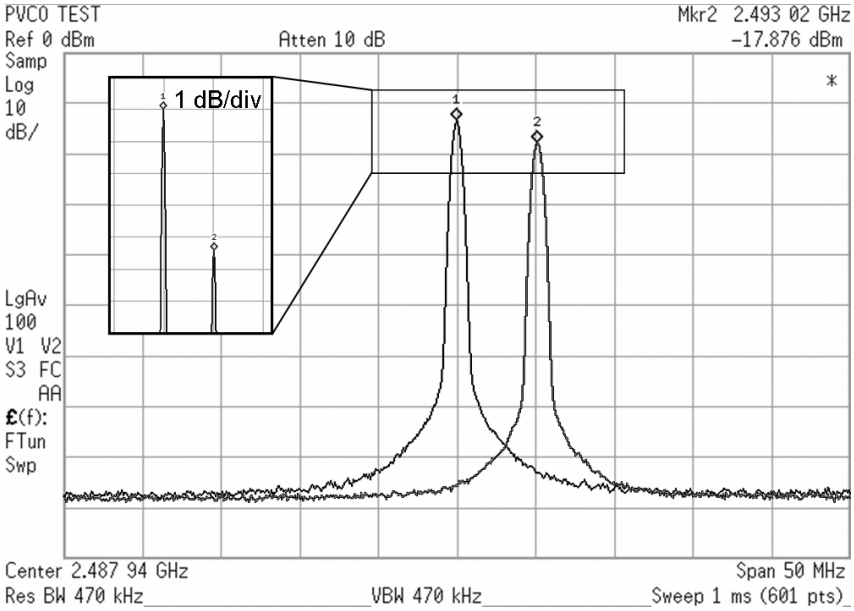


Fig. 24. TX output power with and without self-tuning system activated. (N.B. Frequency deliberately offset to distinguish between the two cases.)

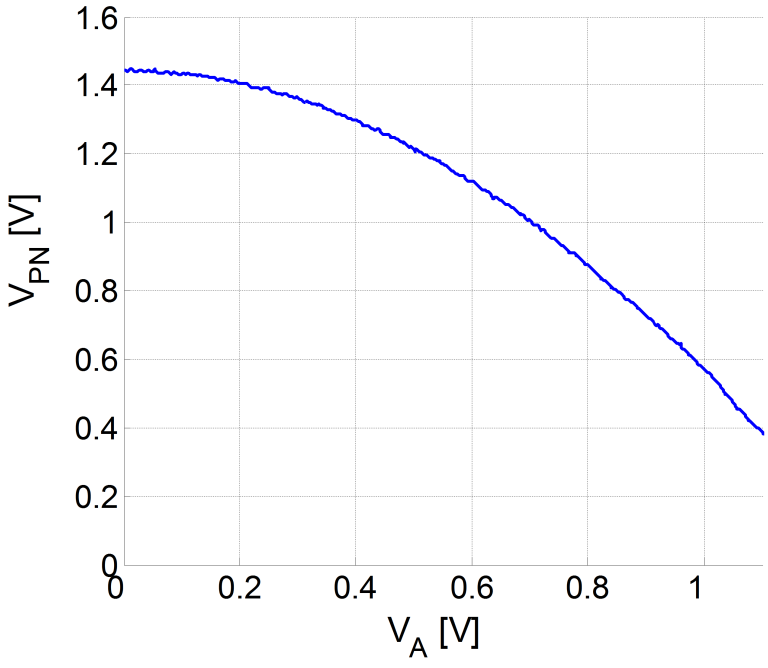


Fig. 25. Measured power-detector performance in pseudo-differential (PD) mode

Table IV. Comparison to similar recently published works

Ref.	Freq. [GHz]	Process [μm-CMOS]	TX Architecture	Modulation	TX Area [mm^2]	P_{out} [mW]	Data Rate [kbps]	P_{DC} [mW]	$\mathbf{P_{TX}^{avg}}$† [μW]	**Special Requirements**	**Packaging**
This Work	2.4	0.18	Direct Modulation	FSK	0.7	>1	1000	50.4	**50.4**	**none**	**QFN48 on FR4**
[30]	2.4	0.18	Direct Conversion	OQPSK	>2	1	250	30	**120**	**off-chip inductor**	**not packaged: COB**‡
[31]	2.4	0.18	Direct Conversion	GFSK	>2	1	1000	72	**72**	**none**	**QFN52**
[29]	1.9	0.13	Injection Locked	OOK	0.4	1	156	1.8	**11**	**FBAR***	**not packaged: COB**
[32]	1.9	0.13	Direct Modulation	OOK	0.4	0.5	83	1.1	**13**	**BAW******, bondwire inductor**	**not packaged: COB**
[33]	1.9	0.13	Direct Modulation	OOK	0.3	1	50	3	**60**	**MEMS resonator, off-chip inductor**	**not packaged: COB**
[34]	0.9	0.25	Direct Modulation	FSK	≈ 0.4	0.25	100	1.3	**13**	**off-chip inductor**	**not packaged: COB**

† $P_{TX}^{avg} \equiv$ power TX would consume when transmitting 1 packet/sec., 1000 bits/packet [29]; ‡ COB: Chip on Board
$*$ FBAR: Film Bulk Acoustic Resonator; $**$ BAW: Bulk Acoustic Wave Resonator

Table V. Comparison to recent tank self-calibration circuits

Ref.	Freq. [GHz]	Process [μm]	Tested?	Trimmed device	External Equipment?	ADC/DSP Required?
This Work	2.4	0.18	measured	capacitor	none	no
[9]	1.9	0.25	simulated	inductor	2-tone generator	no
[10]	2.4	0.18	simulated	capacitor	none	yes

The overall system, which requires no external resonators or special chip-on-board assemblies, compares favorably with existing state-of-the-art low-power transmitters in terms of average transmitter power, area, and output power.

The proposed calibration loop overcomes the LC tanks' non-monotonic output-power-vs.-tank-resonant-frequency characteristics without any ADC/DSP or external signal generators. The interactions of resonant PA/VCO tanks have been analyzed and an isolating resistive-buffer solution was presented. Furthermore, the frequency-dependent nonlinear operation of a Gilbert-cell-based power detector was examined and experimental validation was presented. Understanding the frequency-dependent nonlinear behavior of the power-detector cell proves vital to ensuring tuning-loop stability and moreover can extend the useful operating frequencies of older technologies by allowing design at frequencies where parasitics are appreciable.

CHAPTER IV

HIGHLY LINEAR, RECONFIGURABLE, CONTINUOUSLY TUNABLE, POWER-ADJUSTABLE FILTER: ARCHITECTURE AND STABILITY THEORY*

A. Introduction

The prevalence of wireless standards and the introduction of dynamic standards/applications, such as software-defined radio, necessitate filters with wide ranges of adjustable bandwidth/power, and with selectable degrees and shapes [35, 36, 37]. The baseband filters of transceivers often utilize a significant portion of the power budget, especially when high linearity is required. Likewise, a widely tunable filter designed for its highest achievable frequency consumes more power than necessary when adjusted to its lowest frequency. Because power consumption is proportional to the dynamic range and frequency of operation, power-adjustable filters have recently gained popularity [36, 38], as they can adapt their power consumption dynamically to meet the needs of the system.

Dynamic variation in filter attributes (e.g. frequency, order, type) coupled with companies' desire to reuse IP has popularized highly programmable filters. Figure 26 displays the low-pass-filter cutoff frequencies of several wireless/wireline standards within the 1MHz-20MHz frequency range. Many of these standards are irregularly spaced in frequency and do not lend themselves well to standard binary-weighted resistor arrays. In previous designs frequency is solely controlled digitally, and hence, digital circuitry or an ADC is used to tune the frequency of the filters. $G_m - C$ filters [37, 39] offer continuous frequency tunability and can operate at higher frequencies than their active-RC counterparts.

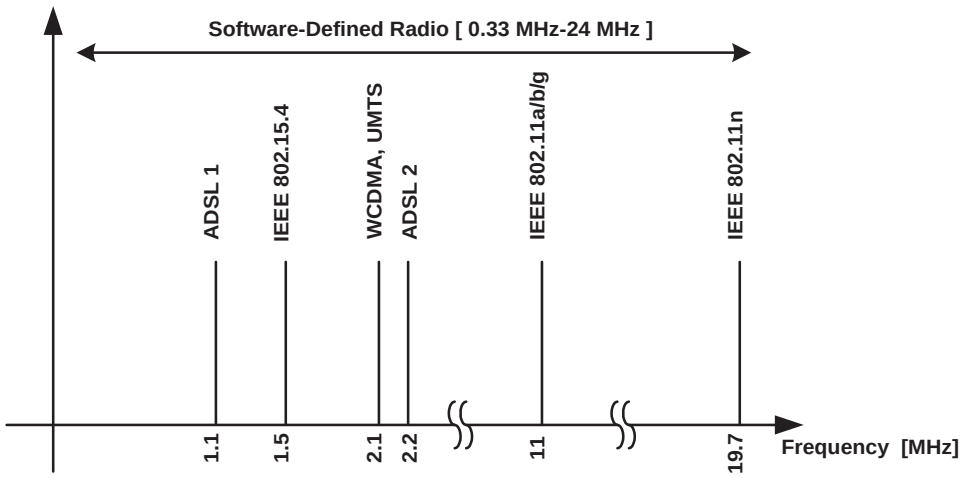


Fig. 26. Diverse wireless/wireline applications with unevenly spaced LPF cut-off frequencies (note: axis not to scale)

MOSFET-C filters [40] can also provide continuous frequency tuning, but both $G_m - C$ and MOSFET-C filters lack good linearity. MOSFET-C filters additionally suffer from reduced tuning range at lower supply voltages; also, in MOSFET-C most of the voltage drop occurs over nonlinear MOSFET triode resistors, which appreciably degrades its linearity [41]. Along these lines, filters with good linearity have been developed that tune on the basis of duty-cycle control in switched-R-MOSFET-C filters [41]; however, duty-cycle control by nature necessitates a *discrete-time* filter. Active-RC filters, known to have good linearity, have been used for *continuous-time* programmable filters. Some such filters have narrow frequency ranges [42, 43], with a few others providing wider but *solely discrete* ranges [38, 44, 45]. Purely discrete switched-resistor tuning limits filter frequency tuning to discrete frequencies determined by the overall frequency range and number of bits used. Tuning to different frequency bands precisely would require very fine resistor stripes to meet precision requirements for the low-frequency end. To avoid such a large bank of resistor stripes and switches, we propose an active-RC filter with continuously tunable frequency. With this tuning scheme, the filter obtains the linearity of the active-RC topology,

but provides continuous frequency tuning similar to $G_m - C$ filters by using a new circuit, a Continuous Impedance Multiplier (CIM).

Newer technologies offer increased integration with smaller feature sizes, allowing the filter to be on the same chip with other transceiver blocks. This integration especially promotes re-configurable architectures, as DSPs can be integrated with the transceiver and can control the mode of operation. However, as minimum feature size shrinks, supply voltages also reduce, which complicates classical linearization techniques of $G_m - C$ filters. In this respect, active-RC filters possess an intrinsic linearity advantage.

This work is organized as follows. Section B presents the overall filter architecture and defines new biquad stability metrics Minimum Acceptable Phase Margin (MAPM) and Effective Phase Margin (PM_{eff}). Section A introduces the Continuous Impedance Multiplier (CIM), and outlines how the CIM affects the filter's poles/zeros. The opamp design and filter layout considerations are discussed in Sections B and A, respectively. After that, Section B presents the experimental results. Conclusions are given in Section C.

B. System-Level Design

1. Top-Level Architecture

Figure 27(a) illustrates the top-level filter architecture, comprising a cascade of one first-order stage followed by two biquad stages (cf. Figure 27(b)) for ease of tuning. Figure 27 (c) and (d) show how discrete/continuous frequency tuning and filter shape selection (Chebyshev/Inverse Chebyshev) are performed. Signal inputs REF_IN and FILTER_IN represent the reference sinusoidal input and the filter input, respectively. Section A describes filter shape selection and frequency tuning in greater detail. Figure 28 shows the division of the transfer function, where a lower-order transfer function is obtained by tapping the output

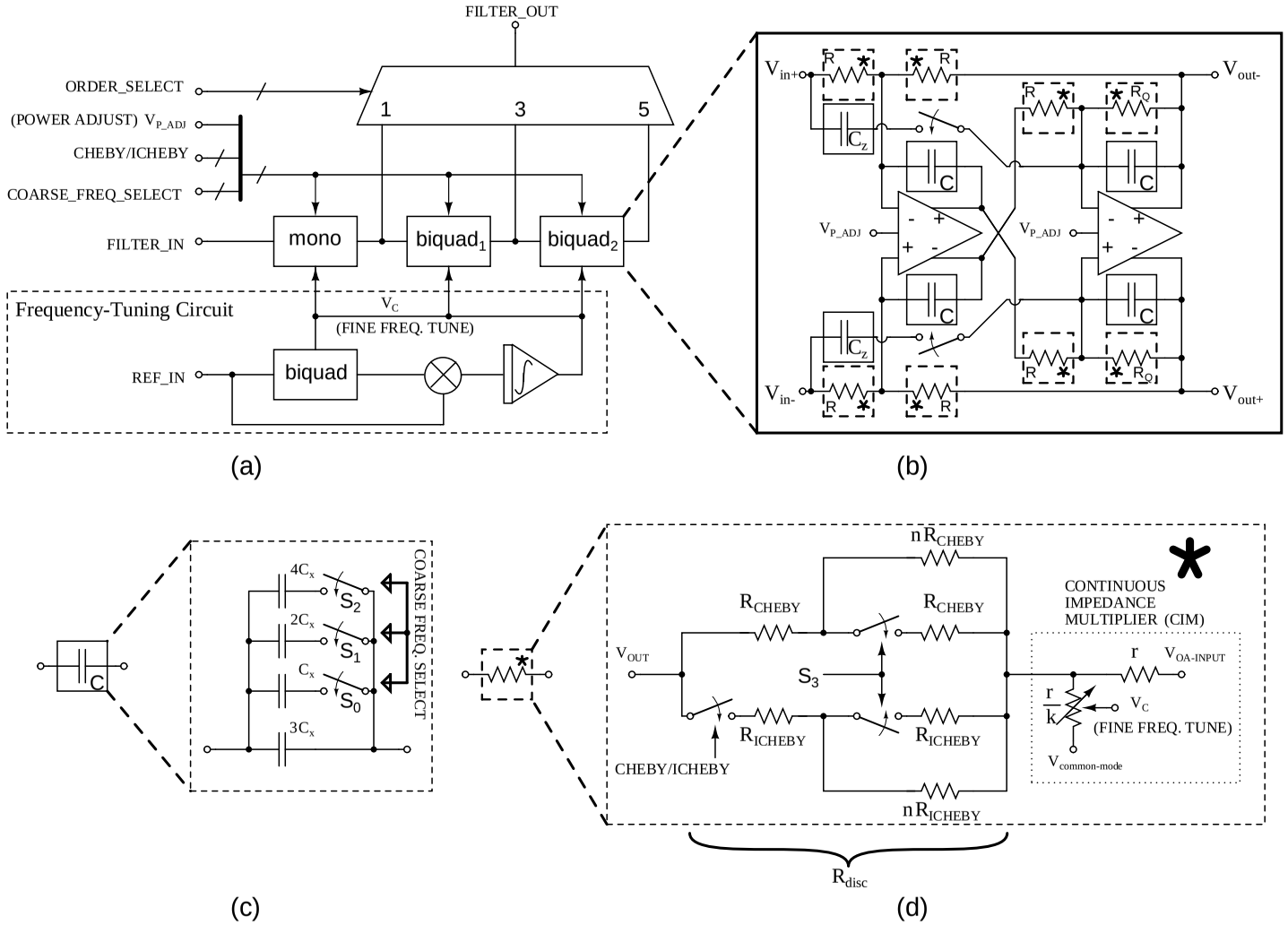


Fig. 27. Active RC low pass filter (a) top-level filter architecture, (b) biquad, (c) capacitor array for discrete frequency selection, (d) switched resistor network for filter type selection followed by Continuous Impedance Multiplier (CIM)

of intermediate stages. Unused stages may then be deactivated to save power. It can be shown that the equivalent single-ended impedance loading the biquad actually increases by $\frac{1}{4}\left(2R+\frac{1}{sC}+\frac{1}{sC+[QR]^{-1}}\right)$ when the opamp is deactivated.

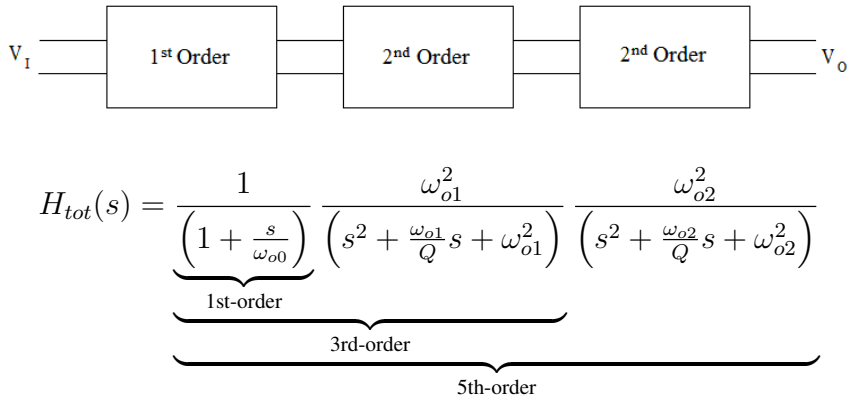


Fig. 28. Division of cascade stages transfer functions (for chebyshev approximation)

Because the impedance when the opamps are off is larger than that when they are on, negligible degradation of the response is predicted. Also, a power-adjustment signal V_{P-ADJ} controls the power consumption of each opamp. In the following sections, we analyze the influences of opamp GBW and PM on the stability of the filter. For simplicity, the analysis is presented in terms of all-pole biquads; however, the inclusion of finite transmission zeros does not affect the generality of the stability analysis.

2. Theory of Minimum Acceptable Phase Margin

Power-adjustable filters must remain stable even when their power is reduced. This section examines the effects of opamp GBW/phase margin (PM) on biquad stability and identifies minimum PM thresholds for biquad stability. As presented in Figure 29, the two-integrator-loop biquad has two local feedback loops in addition to one global feedback loop. Having so many loops complicates the biquad stability problem when using non-ideal opamps with finite GBW and non-ideal phase margin. Though $PM = 60^\circ$ is generally acceptable for good opamp settling and *single-loop* stability, a more detailed stability study shows

that for different biquad parameters (corner frequency ω_o and quality factor Q), different minimum opamp PMs are required to guarantee *biquad* stability. In some cases, even 60° is insufficient.

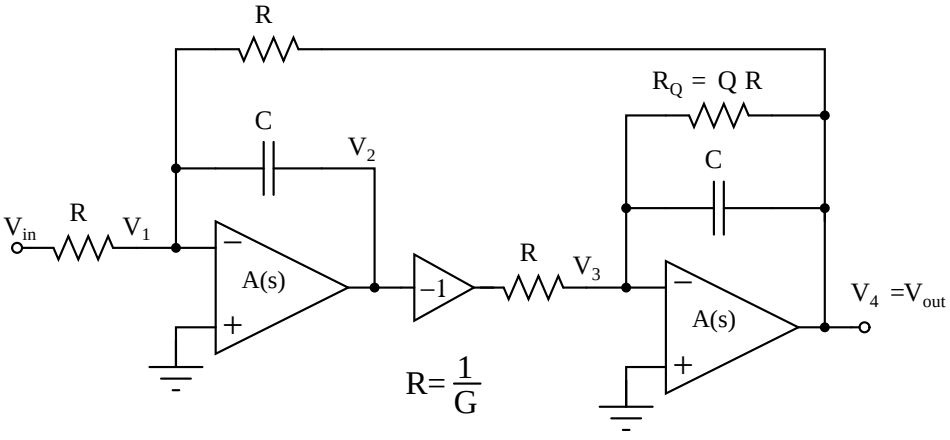


Fig. 29. Biquad circuit with annotated node voltages (for chebyshev approximation)

Our implementation uses fully differential circuits; however, we consider the single-ended case for simplicity. Analysis of the circuit in Figure 29 assuming identical opamp gains A(s) yields

$$H_{biquad}(s) \equiv \frac{V_4}{V_{in}} = \frac{-G^2}{D_{tot}(s)} \tag{4.1}$$

where

$$\begin{aligned} D_{tot}(s) \quad = \quad & +A^{-2}(s)[(1+Q^{-1})G+sC][2G+sC] \\ & +A^{-1}(s)[([1+Q^{-1}]G+sC)sC+(2G+sC)(Q^{-1}G+sC)] \\ & +s^2C^2+sCGQ^{-1}+G^2 \end{aligned}$$

Previous works have analyzed the effect of non-ideal opamps on stability [46], frequency deviation, and Q deviation [47] of biquads. However, these works have considered the amplifier to be a single-pole integrator (i.e. GBW/s), which neglects the critical effect of non-dominant poles. In this work a two-pole integrator model for $A(s)$ is used to account for the non-dominant pole (and hence phase margin):

$$A(s) \approx \frac{GBW}{s\left(1+\frac{s}{\omega_2}\right)} \Rightarrow A^{-1}(s) \equiv \frac{1}{A(s)} = \frac{s}{GBW}\left(1+\frac{s}{\omega_2}\right) \tag{4.2}$$

Consider the denominator polynomial (2) and substitute the non-ideal opamp gain from (4.2):

$$D_{tot,non-ideal} = \sum_{k=0}^{6} a_k s^k = \begin{array}{l} G^2+ \\ \left(2\frac{G^2}{QGBW}+\frac{CG}{Q}\right)s+ \\ \left(2\frac{G^2\left[1+Q^{-1}\right]}{GBW^2}+2\frac{G^2}{QGBW\omega_2}+\frac{CG\left[3+2Q^{-1}\right]}{GBW}+C^2\right)s^2+ \\ \left(4\frac{G^2\left[1+Q^{-1}\right]}{GBW^2\omega_2}+\frac{CG\left[3+Q^{-1}\right]}{GBW^2}+\frac{CG\left[3+2Q^{-1}\right]}{GBW\omega_2}+2\frac{C^2}{GBW}\right)s^3+ \\ \left(2\frac{G^2\left[1+Q^{-1}\right]}{GBW^2\omega_2}+2\frac{CG\left[3+Q^{-1}\right]}{GBW^2\omega_2}+\frac{C^2}{GBW^2}+2\frac{C^2}{GBW\omega_2}\right)s^4+ \\ \left(\frac{CG\left[3+Q^{-1}\right]}{GBW^2\omega_2^2}+2\frac{C^2}{GBW^2\omega_2}\right)s^5+ \\ \left(\frac{C^2}{GBW^2\omega_2^2}\right)s^6 \end{array} \tag{4.3}$$

The stability of the system can be determined by analyzing the sign changes of the first column of the Routh-Hurwitz (RH) array, which, for a 6^{th}-order polynomial, takes the following form:

$$RH = \left(\begin{array}{cc|cc} a_6 & a_4 & a_2 & a_0 \\ \hline a_5 & a_3 & a_1 & 0 \\ \hline \frac{a_4a_5-a_3a_6}{a_5} & \frac{a_2a_5-a_1a_6}{a_5} & 1 & 0 \\ \hline RH_{41} & RH_{42} & 0 & 0 \\ \hline RH_{51} & 1 & 0 & 0 \\ \hline RH_{61} & 0 & 0 & 0 \end{array}\right) \tag{4.4}$$

Carrying out the computation of the Routh Array in MATLAB, we obtain symbolic expressions for the first column $RH_{k,1},\ k = 1,\ldots,6$. For positive values of $G,\ C,\ \omega_2,\ GBW$, and for $k = 1..5,\ RH_{k,1} > 0$, implying system stability iff $RH_{61} > 0$.

We can write the RH_{61} expression in terms of system-level parameters $\omega_o \equiv G/C$, Q and *normalized* amplifier circuit parameters ω_o/GBW and ω_o/ω_2. System-level parameters ω_o and Q can be obtained from filter-design tools such as FIESTA [48] or MATLAB. Using the generalized expression of RH_{61}, we determine the minimum required phase

margin of the opamps given ω_o/GBW and Q to guarantee biquad stability. We term this threshold Minimum Acceptable Phase Margin (MAPM). The following procedure outlines how Minimum Acceptable Phase Margin is obtained:

1. MATLAB analysis shows that RH_{61} is a rational function of $x \equiv \omega_o/GBW$ and $y \equiv \omega_o/\omega_2$, and that the denominator of this rational function is always positive, $RH_{61} < 0$ iff the numerator is less than zero.

2. Partition numerator expression into blocks, each of which represents a term of the form $bx^m y^n;\ b \in \mathbb{R};\ m, n \in \mathbb{Z}^{nonneg}$, where b represents a coefficient, which itself is a polynomial function of Q alone.

3. Group the blocks and factor to obtain a (5^{th}-order) polynomial P in y: $P(y) = \sum_{k=0}^{5} c_k y^k$, where each coefficient c_k is a function of x and Q.

4. Substitute values of x, Q and solve the 5^{th}-order polynomial numerically for y.

5. With $y = \frac{\omega_o}{\omega_2}$, phase margin $\equiv PM = 90^\circ - \arctan\left(\frac{GBW}{\omega_2}\right) = 90^\circ - \arctan\left(\frac{GBW}{\omega_o}\frac{\omega_o}{\omega_2}\right) = 90^\circ - \arctan\left(\frac{y}{x}\right)$.

Because the value of phase margin obtained in the procedure above sets $RH_{61} = 0$, this value represents the Minimum Acceptable Phase Margin (MAPM) for system stability. Therefore, if the opamp's phase margin falls below this *minimum* threshold, then the biquad will have a right-half-plane pole and hence will become unstable.

Using the analysis procedure outlined, we have derived a set of generalized contours relating a given biquad Q and normalized amplifier GBW (ω_o/GBW) to the minimum acceptable phase margin (MAPM) required to maintain biquad stability. Figure 30 plots MAPM as a function of biquad Q and normalized GBW. The arrow on the figure indicates that the opamps' stability requirements are *more relaxed* for biquads with *lower* MAPM.

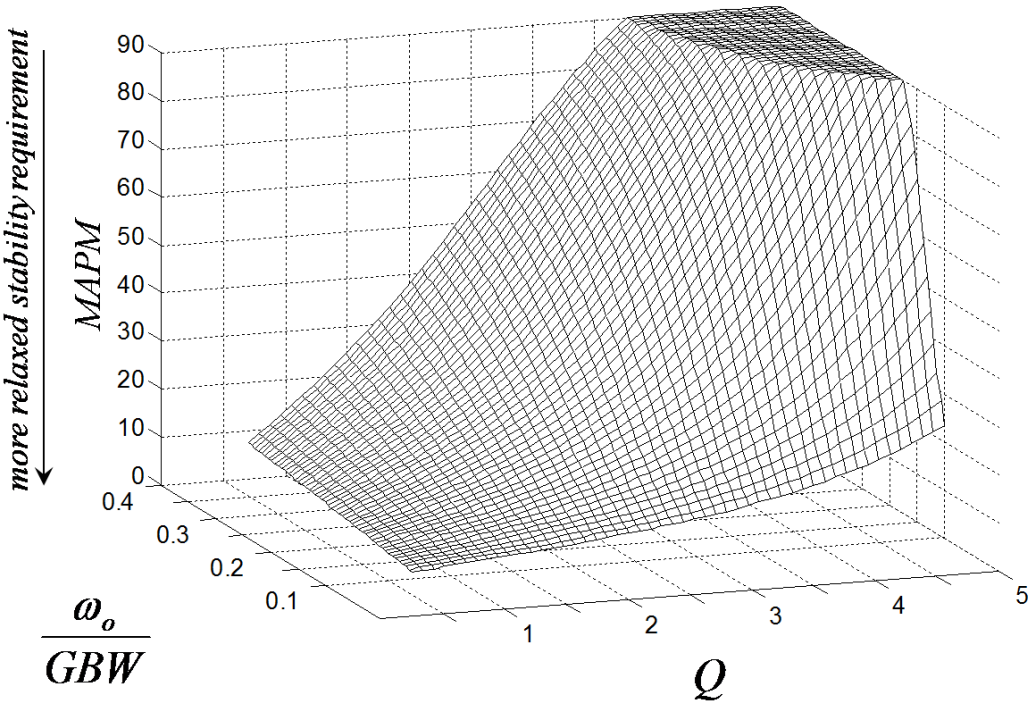


Fig. 30. Minimum Acceptable Phase Margin (MAPM) for biquad stability

The plateau at the top of the curve corresponds to combinations of normalized GBW and Q for which the biquad can *never* be stable.

3. Effective Phase Margin

Figure 31 illustrates how minimum acceptable phase margin MAPM can be applied to opamp design to obtain an *effective* phase margin PM_{eff}, where $PM_{eff} \equiv PM_{conv.} - MAPM$. Effective phase margin is the amount by which the opamp's "conventional" phase margin exceeds the *minimum* required phase margin to ensure biquad stability. PM_{eff} *must be positive* for the biquad to be stable. Figure 32 presents a possible flowchart for biquad opamp design using MAPM analysis and cross-sections of Figure 30 with planes of constant Q. For a given value of Q, a single curve on this set of cross-sections graphically

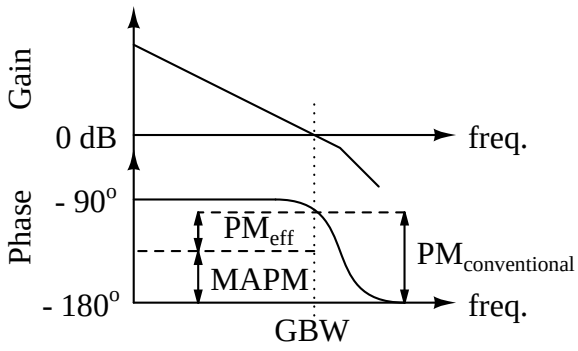
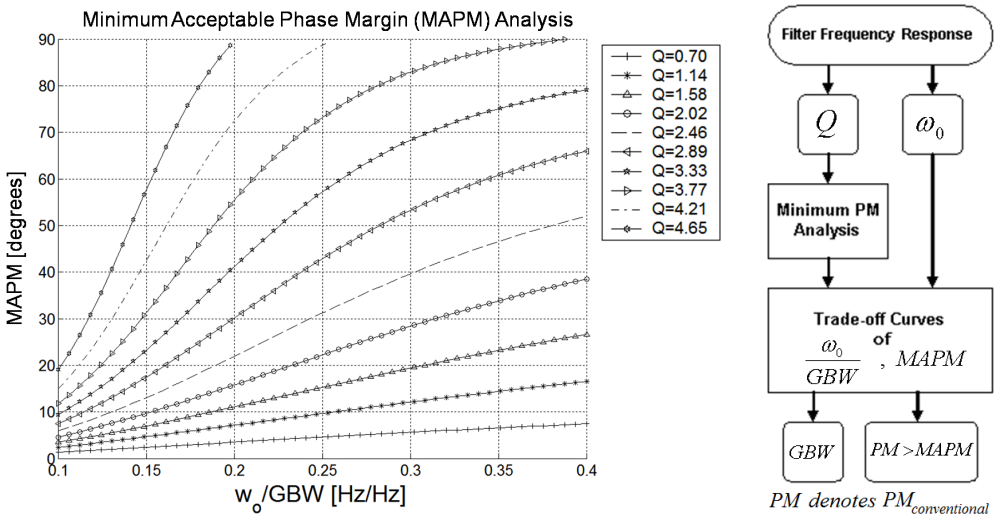


Fig. 31. Opamp effective phase margin

illustrates the tradeoff between MAPM and ω_o/GBW.



(a) (b)

Fig. 32. (a) Cross-sections of MAPM contour (Figure 30) and (b) possible MAPM-assisted design flowchart

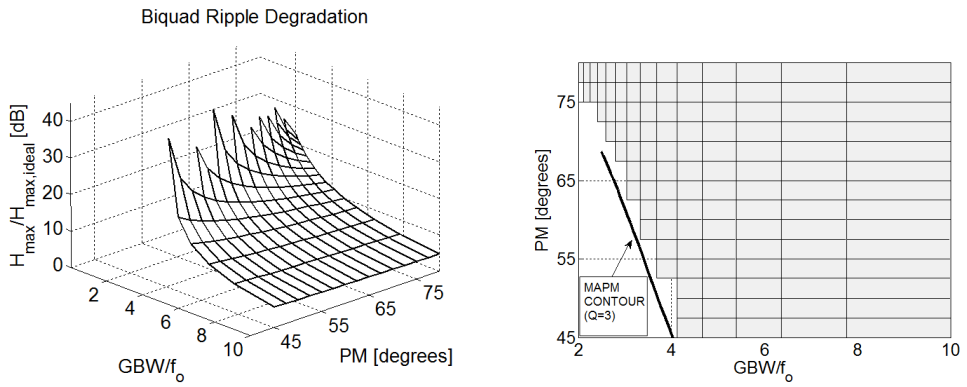
The following example traces through the design procedure given in Figure 32(b). Suppose we wish to design a biquad with $Q = 3.33$ and $\omega_o = 10MHz$. Looking at the Q=3.33 curve in Figure 32(a), we can see the tradeoff between GBW and MAPM required for stability. If, for instance, we choose $GBW = 50MHz$, then $\omega_o/GBW = 0.2$ and hence $MAPM = 40°$. Thus, the opamp's PM must *exceed* $40°$ in order to ensure biquad

stability, that is to have $PM_{eff} = PM - 40^\circ > 0^\circ$. Had we chosen a larger GBW, such as 100MHz, then $\omega_o/GBW = 0.1$ and, according to Figure 32(a), $MAPM = 10^\circ$. In this case, the opamp phase margin would only need to exceed 10°, yielding a more relaxed PM specification at the expense of larger GBW.

4. Passband Ripple and GBW Limitations

Many previous works have analyzed the relationship between amplifier GBW and effective biquad Q. It can be shown [49] that in a two-integrator-loop biquad, the effective biquad Q is enhanced by roughly a factor of $\left(1 - 2Q\frac{\omega}{GBW}\right)^{-1}$. This Q enhancement translates to ripple degradation. Based on the filter denominator expression of (4.3) derived in the 2, we can model biquad ripple degradation as a function of amplifier GBW, and we can add phase margin to the analysis. Solving for the maximum value of the biquad transfer function, we obtain the variation of ripple versus GBW and PM. The resulting plot in Figure 33(a) indicates the degradation in ripple ($H_{\max}/H_{\max,ideal}$) for a biquad with a nominal Q of 3 (i.e. $H_{\max,ideal} = 9.665dB$). Though the plotted ripple-degradation numbers are quite large, higher-order filters superimpose several biquad responses to obtain the desired ripple, so the actual ripple degradation of higher-order filters is more complex.

Reduction in GBW quickly degrades the biquad's ripple, which is computed by obtaining the maximum peak in the passband. The phase margin additionally degrades the ripple—note that the contour rises as phase margin is reduced towards 45 degrees. The sharp edges of the contour occur because the biquad destabilizes for those combinations of PM and GBW. As is seen in Figure 33(b), a bird's eye view of the surface in Figure 33(a) can be superimposed with the associated Minimum Acceptable Phase Margin contour for Q=3. The MAPM contour shown in Figure 30 corresponds to the location of the ripple-surface asymptote. This illustrates how MAPM relates to the degradation of biquad ripple and to the stability of the biquad. As noted in [43], even when $GBW > 10f_{cutoff}$, rip-



(a) (b)

Fig. 33. (a) Variation of biquad passband ripple with GBW, PM and (b) top-view of the surface from (a) with associated MAPM contour

ple degradation in excess of 8dB can occur. Also, as power increases, GBW eventually saturates, leading to diminishing improvements in ripple. Compensation at the filter level can help to mitigate the Q enhancement caused by finite amplifier GBW and PM. Multiple techniques can be employed to improve ripple based on application. Adding extra resistors/capacitors inversely proportional to the opamp's GBW can be added to the basic integrator structure to create a zero that cancels the effect of the amplifier's finite GBW [49, 50, 51]. In addition, Akerberg and Mossberg have proposed an active compensation scheme, where an additional amplifier placed in unity-gain feedback can more accurately track the main opamp's GBW and compensate the response, at the expense of reduced loop stability [52].

Alternatively, the response can be compensated using predistortion [49], such that when nonidealities are introduced, the net response has the desired shape. By using a slightly modified version of our CIM scheme, we could achieve independent Q and frequency tuning. As discussed in Section 3, the biquad Qs are preserved when all resistors are scaled by the same factor. However, because $Q_k = R_{Qk}/R_k$, we could compensate the Q enhancement by independently tuning the resistors R_{Qk}, provided that the control

voltage V_C for those resistors is separate from that for the remainder of the resistors. In this work, we have connected all of the control lines together for simplicity; however, for future work, this concept of Q tuning for filter compensation could be explored.

CHAPTER V

HIGHLY LINEAR, RECONFIGURABLE, CONTINUOUSLY TUNABLE, POWER-ADJUSTABLE FILTER: FREQUENCY TUNING AND CIRCUIT IMPLEMENTATION*

A. Frequency Tuning

1. Overview of Procedure

Frequency-response tuning occurs in three steps. First, the filter shape (Chebyshev/Inverse Chebyshev) is selected with the control bit CHEBY/ICHEBY (cf. Figure 27), and second, the frequency band is chosen with a digital control word $S_3S_2S_1S_0$. This digital word switches the appropriate resistor(S_3)/capacitor($S_2S_1S_0$) values to obtain the desired frequency-response. As shown in Figure 27(a), the filter's architecture includes a conventional frequency tuning circuit [53] to adjust the filter's corner frequency. In this tuning scheme a sinusoidal reference signal passes through a biquad with identical frequency behavior to the main 5^{th} order filter. Then, the biquad input and output are multiplied, generating the error voltage. The integrated error voltage controls the frequency of the 5^{th}-order filter and (master) biquad. This control voltage will remain constant if the input and output of the low-pass biquad are exactly 90° apart; otherwise, it varies such that the voltage-controlled-filter's and biquad's corner frequency are matched with the input reference signal. Accuracy of this tuning scheme depends on its loop gain which is a function of the biquad Q, reference signal amplitude and multiplier/integrator gain at the reference frequency [53]. The analog frequency scaling is achieved by continuously adjusting the

active-RC resistances with a Continuous Impedance Multiplier (CIM). Section 2 details the operation of the CIM, and Section 3 explains how the CIM preserves frequency-response shape as resistances and hence time constants are continuously scaled.

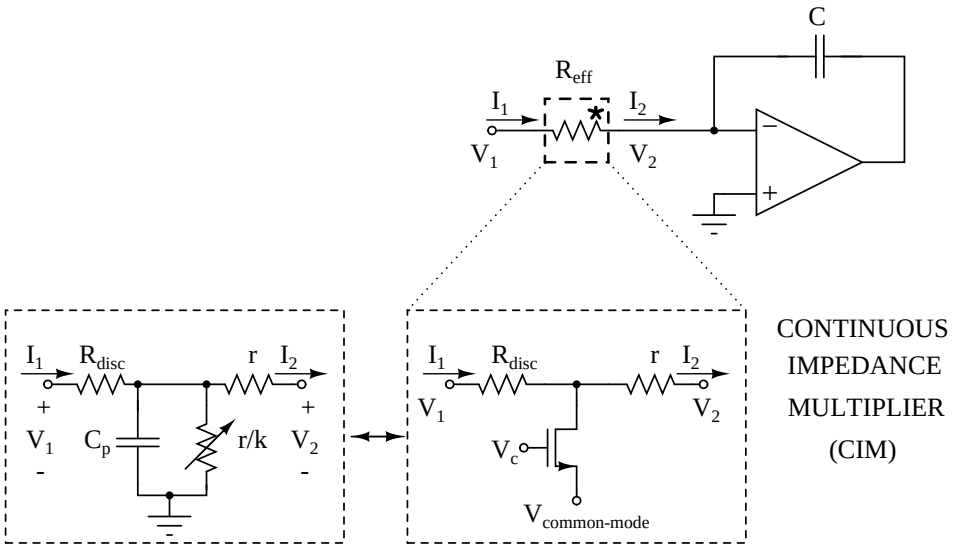


Fig. 34. Continuous Impedance Multiplier (CIM)

2. Continuous Impedance Multiplier (CIM)

The Continuous Impedance Multiplier (CIM) provides fine frequency tuning and allows for considerably smaller resolution than could be achieved with discrete adjustment alone. By combining coarse discrete frequency selection with continuous fine tuning, the frequency can be adjusted more precisely. Conceptually, the CIM continuously scales all resistances of the filter by the same value. By scaling all resistors by the same factor, the Qs and relative ratios of ω_o are preserved, and hence the filter shape is maintained. Figure 34 shows the CIM's conceptual block diagram, circuit-level implementation, and equivalent AC circuit with transistor parasitics. Feedback linearizes a system only if the feedback elements are themselves linear; hence, placing conventional nonlinear voltage-controlled resistors in feedback will severely degrade linearity. This novel approach to continuous tuning pre-

serves linearity performance by using the nonlinear resistor as a current-syphoning element and ensuring that its nonlinear resistance constitutes only a small percentage of the overall resistance. Moreover, because the CIM resistance $r \ll R_{disc}$, the swing on the triode transistor is small, which helps to preserve linearity. The common-mode (CM) voltage $V_{common-mode} = \frac{1}{2}V_{DD} = 0.5V$ is the CM reference level (also applied to the opamps' CMFB circuits). Port 2 of the CIM (denoted by (*) in Figure 27 and Figure 34) is *always* connected to an opamp input. In Figure 34, assuming that $r \ll R_{disc} \ll \frac{1}{sC_p}$, it can be shown that the transimpedance of the CIM is approximated by:

$$R_{eff} = \frac{V_1}{I_2} = \frac{R_{disc}(k+1)+r}{1-\left[1+k\frac{R_{disc}}{r}\right]\frac{V_2}{V_1}} \approx R_{disc}(k+1)$$

where $V_2 \approx 0$ because the opamp creates a virtual AC ground at its inputs. Note that resistance R_{disc} in Figure 34 is the equivalent resistance of a resistor network shown in Figure 27(d). The CIM magnifies resistance R_{disc} (made of combination of salicided/unsalicided poly resistors) by syphoning current before it reaches the virtual ground terminal of the opamp. Note that dividing the current affects the transimpedance $R_{eff} = \frac{V_1}{I_2}$. We reduce I_2 by bleeding away part of the current I_1 and feeding this portion $\frac{k}{1+k}I_1$ through the triode MOSFET (a thin-oxide core transistor). Adjusting V_C from $V_{common-mode}$ to V_{DD} changes k and hence continuously scales $R_{eff} \approx R_{disc}(k+1)$:

$$\frac{r}{k} \equiv R_{triode} \approx \frac{1}{\mu_n C_{ox}\frac{W}{L}\left(V_C - V_{common-mode} - V_{th}\right)}$$

$$k = f(V_C) = \mu_n C_{ox}\frac{W}{L}\left(V_C - V_{common-mode} - V_{th}\right)r$$

Table VI summarizes how digital controls S_3 and CHEBY/ICHEBY as well as continuous control $k = f(V_C)$ adjust the effective resistance R_{eff} seen by the opamp. If we also include the effects of parasitic capacitance C_p and finite amplifier GBW, then the tran-

Table VI. Discrete/continuous resistor adjustment

S_3	CHEBY/ICHEBY	R_{eff}
0	0	$(n+1)R_{CHEBY}(k+1)$
0	1	$(n+1)[R_{CHEBY}\|\|R_{ICHEBY}](k+1)$
1	0	$2R_{CHEBY}(k+1)$
1	1	$2[R_{CHEBY}\|\|R_{ICHEBY}](k+1)$

* $S_3 = 0$: Low-Frequency Mode, $S_3 = 1$: High-Frequency Mode
** $1 \ll n \in \mathbb{N};\ k \in \mathbb{R}$

simpedance becomes (assuming $V_2 = -V_o/A(s)$, $V_o = \alpha V_1$, and $|\alpha| \approx 1$ in the passband)

$$Z_{12} = \frac{V_1}{I_2} \approx \frac{\frac{1+k}{k} + \frac{s}{\omega_t}}{\frac{1}{kR_{disc}} + \frac{\alpha}{r}\frac{s}{GBW}\left(1 + \frac{s}{\omega_t}\right)}$$

where $\omega_t \equiv \frac{2\mu V_{DSAT}}{L^2} = \frac{2\mu C_{ox}\frac{W}{L}(V_C - V_{common-mode} - V_{th})}{C_{ox}WL} \approx \frac{k}{rC_p}$, and $\frac{W}{L}$ is chosen to be $\frac{1\mu m}{0.12\mu m}$. Hence, choosing small L minimizes the degradation at higher frequencies due to parasitic capacitance, while ω_t will improve with smaller size technologies; however, choosing this small L will slightly degrade matching. Also, choosing a sufficiently high amplifier GBW ensures that node V_2 is a virtual ground at the frequencies of interest.

3. Relative Pole Positioning

The key challenge behind a filter with both reconfigurable frequency response (Chebyshev/Inverse Chebyshev) and tunable cutoff frequency is to decouple the selection of the response shape from the frequency tuning. Once this separation has been accomplished, the frequency can be tuned independently of the shape of the response. This decoupling is important because it allows the reuse of the same tuning hardware for all filter configurations. Ideally we want to scale the frequency axis by a constant m, analogous to normalized filter design prior to modern software tools. It can be shown that scaling the frequency axis $m : s' = ms$ corresponds to reducing all filter cutoff frequencies by a factor of $m : \omega_c' = \frac{\omega_c}{m}$.

Thus, the design task reduces to adjusting the resistor/capacitor values in order to scale all center frequencies ω_{ok} by the *same* value, while keeping all Q_k constant. Because in a

biquad

$$\omega_{ok} = \frac{1}{R_k C_k},\ Q_k = \frac{R_{Qk}}{R_k}$$

multiplying all resistors R_k, R_{Qk} by a scale factor m will reduce ω_{ok} by m as desired (compensating process/voltage/temperature shifts), but will keep Q_k and the ratios $\frac{\omega_{ok}}{\omega_{oj}}$ unchanged:

$$\omega'_{ok} \equiv \frac{1}{(mR_k)C_k} = \frac{\omega_{ok}}{m},\quad Q'_k = \frac{mR_{Qk}}{mR_k} = Q_k,\quad \frac{\omega'_{ok}}{\omega'_{oj}} = \frac{(mR_j)C_j}{(mR_k)C_k} = \frac{\omega_{ok}}{\omega_{oj}}$$

The CIM accomplishes this resistance multiplication and therefore preserves the frequency response shape. As mentioned in Section 4, a slightly modified CIM scheme in which resistors R_{Qk} were tuned independently could mitigate Q enhancement.

B. Operational Amplifier Design

1. Fully Differential Three-Stage Opamp

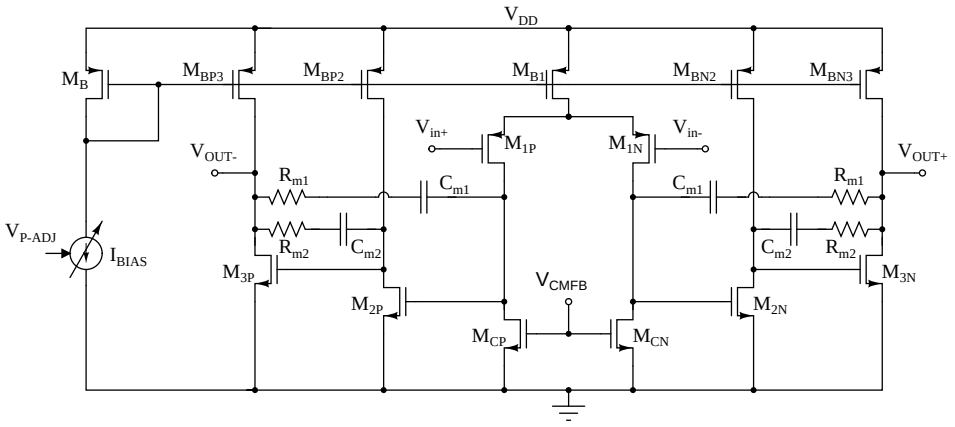


Fig. 35. Opamp schematics

The programmable filter consists of three cascaded stages: one 1^{st}-order filter and two 2^{nd}-order biquad stages, employing a total of five opamps. Each of these identical opamps consumes 0.7mW to 1.5mW, controlled by an adjustable current source (I_{BIAS}) from a sin-

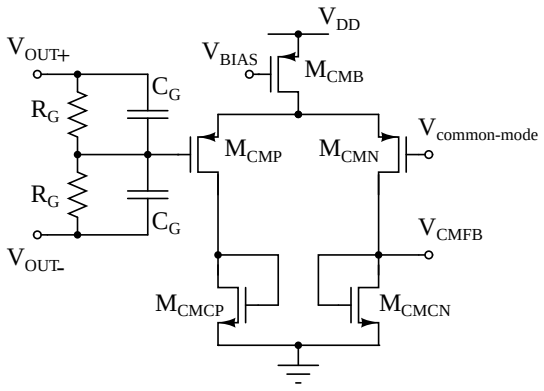


Fig. 36. Common Mode Feedback (CMFB) schematics

gle 1-V supply. Increasing the loop-gain in active-RC filters reduces non-linearities arising from the opamps, so the opamp's gain should be high enough to provide the required loop-gain for the filter's linearity. For different modes of operation, the filter's opamps should also be able to drive different ranges of resistive/capacitive loads (1.5-5.6kΩ||6-50pF). The low supply voltage and the moderately low load resistance necessitate cascading more than two stages to achieve high DC gain and maintain sufficient output swing. Figure 35 and Figure 36 show the schematic of the opamp and common-mode feedback circuit. To achieve higher swing/linearity, the CM level is detected by an RC network instead of two coupled differential pairs [54]. The amplifier employs Nested Miller frequency compensation; however, all stages are inverting. Stability is obtained by proper choice of $R_{m1,2}$ and by ensuring $C_{m1} \ll C_{m2}$.

2. Power Adjustment

Dynamically adjusting the filter's power consumption based on frequency/linearity/noise requirements utilizes power more effectively. For example, previous work [55] dynamically adjusts the tail current of a class-AB opamp in an active-RC filter to increase linearity when blockers are detected. The power-adjustment signal V_{P-ADJ} is used to reduce power consumption at low frequencies except when high linearity is required. The power-

adjustment signal controls the filter's power consumption by adjusting the bias currents of all opamps and CMFB circuits simultaneously.

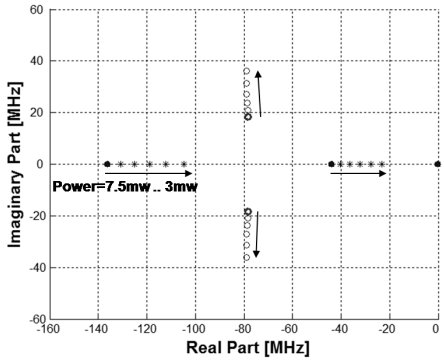
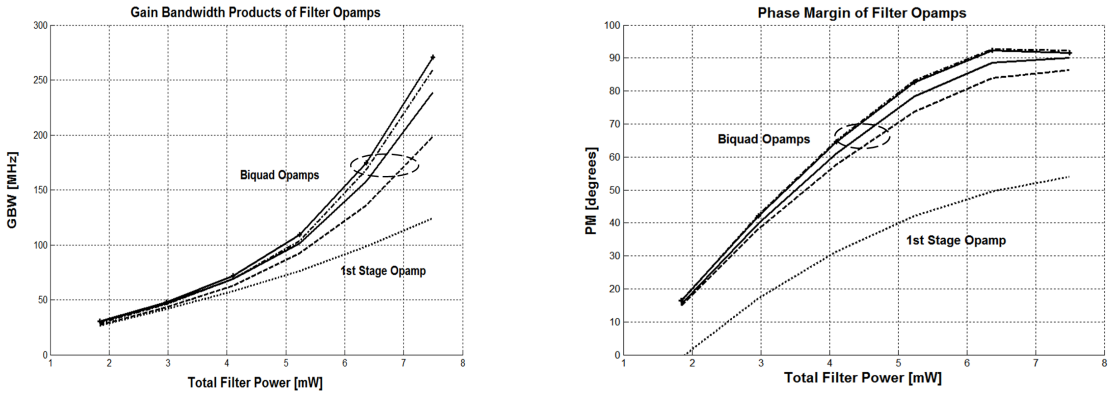


Fig. 37. Root loci of one opamp's poles/zeros w.r.t. power adjustment

Figure 37 and Figure 38 display the variation in pole/zero locations and the corresponding reduction in GBW/PM, respectively, as power consumption is reduced. Note that each opamp (of the five) has a different load. For a given Q, we have derived that MAPM varies with ω_o/GBW. Hence, to maintain a constant stability margin and optimal power, the power should be scaled so as to keep ω_o/GBW constant when ω_o is reduced.



(a) (b)

Fig. 38. Filter opamps' (a) GBW and (b) phase margin vs. total filter power

When the filter is tuned to operate in its highest frequency range, each opamp con-

sumes a maximum power of about 1.5mW (including CMFB circuitry), whereas each consumes approximately 0.6mW when the filter is tuned to operate at its lowest frequency range. A DSP output can adjust the filter's power based on the frequency of operation and linearity/noise requirements.

CHAPTER VI

HIGHLY LINEAR, RECONFIGURABLE, CONTINUOUSLY TUNABLE, POWER-ADJUSTABLE FILTER: LAYOUT CONSIDERATIONS AND MEASUREMENT RESULTS*

A. Layout Considerations

To achieve the proper filter shape, ratiometric matching of filter time constants among stages must be ensured. Time-constant matching hinges on both capacitor and resistor matching. Since all resistors are scaled by CIMs, those CIM cells should be matched as well. This CIM matching is achieved by placing all the CIM cells for the entire filter together at the center of the chip. The CIM cells are symmetrically laid out, and guard metal is placed over them to prevent parasitic coupling and crosstalk.

Capacitor matching within and among stages is ensured by making a common-centroid binary unit and arranging the binary units in as close to a common-centroid configuration as possible. The ratios among stages are more important than the 1x/2x/3x/4x weights of the binary units because the inter-stage ratios determine the shape of the response. Moreover, distribution of different segments within the common-centroid pattern is particularly important because the capacitor array is large. Larger arrays are more susceptible to mismatch due to process gradients and nonlinear stress/doping distributions [56].

Figure 39 illustrates the capacitor layout and floorplanning for common-centroid placement and routing. Because capacitors from different biquads are woven together to provide interstage matching, we include grounded metal shielding around each signal line to pre-

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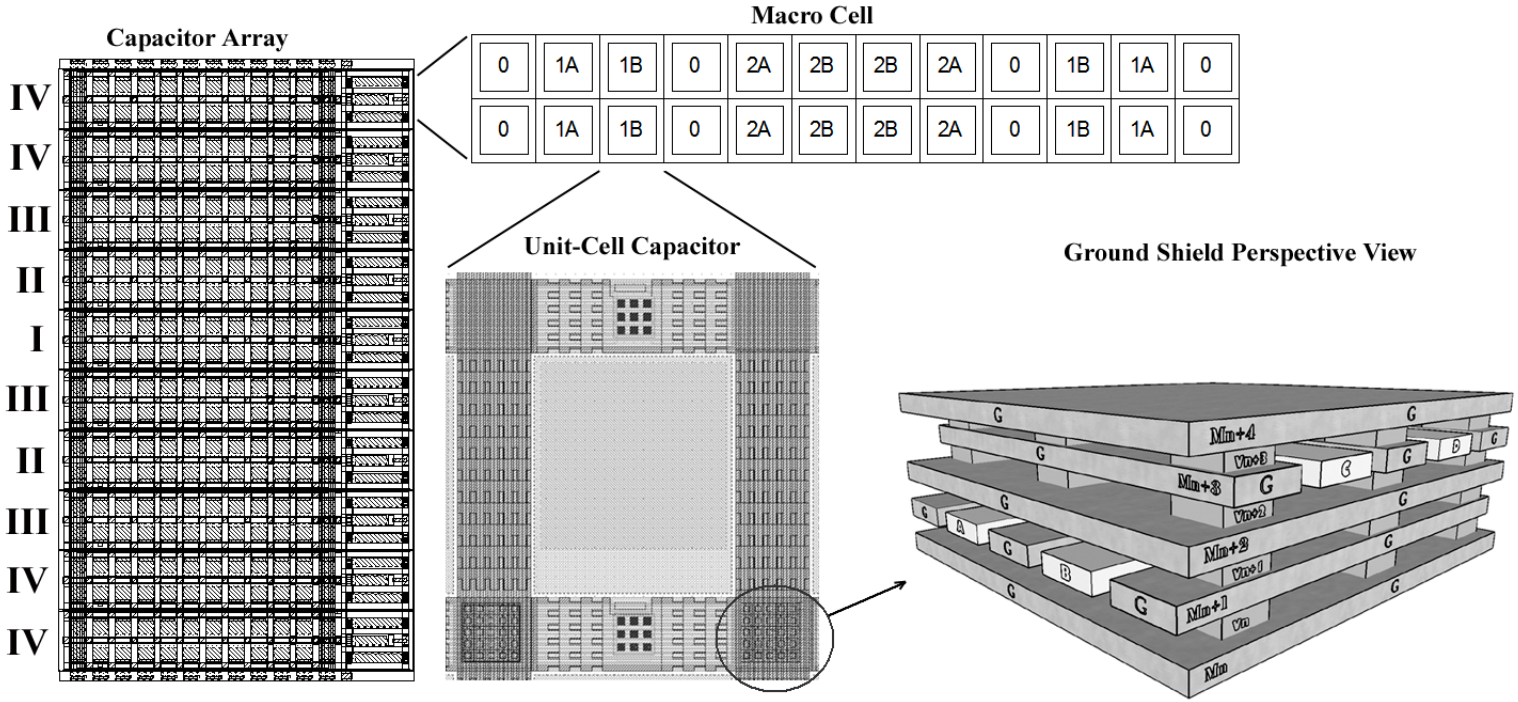


KEY

Capacitor Array		Macrocell		Ground Shield	
label	fingers for nx cap	label	unit cells in stage #	label	description
I	1x	0	1 (1^{st}-Order)	A,B,C,D	separate signal lines
II	2x	1A,B	2 (Biquad 1)	G	ground shield
III	3x	2A,B	3 (Biquad 2)	Mn(+k)	metal n(+k)
IV	4x			Vn(+k)	via b/t Mn(+k), Mn(+k)+1

Fig. 39. Capacitor layout and three-dimensional illustration of ground shield

vent crosstalk. To avoid parasitic coupling, we use as high a layer of metal as possible for the routing.

B. Experimental Results

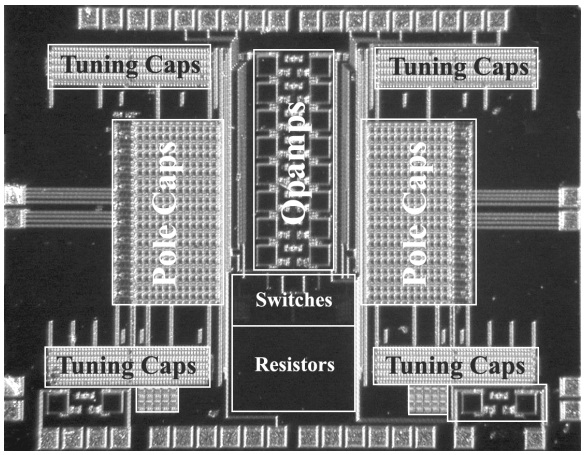


Fig. 40. Chip photograph of continuously tunable, reconfigurable low-pass filter

The programmable filter was fabricated in a $0.13\mu m$ 1P8M CMOS technology. The main filter and tuning circuit occupy 1.53mm^2 and 0.41mm^2, respectively. Figure 40 shows the chip microphotograph. The filter draws 3.0mA-7.5mA from a single 1-V supply. Table VII summarizes the filter performance metrics.

Figure 41 illustrates the setup for frequency response, noise, and linearity measurement– the output buffers and output balun have a total loss of 8dB, which has been deembedded from magnitude-response plots and noise calculations. Frequency adjustment occurs in two phases: coarse digital frequency selection and fine continuous tuning. Figure 42 displays the entire filter tuning range, combining both coarse and fine frequency adjustments. Solid lines represent frequencies achievable using only discrete frequency selection; dashed lines demonstrate continuous frequency tuning achieved by both the discrete frequency selection and the CIM. The filter's continuous tuning combined with discrete frequency selection

Table VII. Measured performance

	low-frequency mode	high-frequency mode
In-Band IIP3 [dBm]	31.3(300kHz, 330kHz)	26.02(4.5MHz, 4.6MHz)
Out-of-Band IIP3 [dBm]	52.8(10MHz, 21MHz)	8(25MHz, 35MHz)
Out-of-Band IIP2 [dBm]	89.5(9MHz, 10MHz)	23.5(25MHz, 35MHz)
Input-Referred Noise [$nV/\sqrt{Hz}$]	85	52
Frequency Range [MHz]	1-5	4-20
DR (@THD=40dB) [dB]	71.4	63.7
THD [dB]	>80 @ 300kHz	45.5 @ 4.5MHz, -2dBm 35 @ 15MHz, -2.6dBm 52.85 @ 15MHz, -14dBm

encompasses all frequencies between 1MHz and 20MHz. The slightly increased ripple at higher cutoff frequencies occurs due to GBW limitations.

The continuous frequency-tuning method preserves the filter shape as the filter corner frequency is adjusted. This tuning scheme facilitates multiple filter shapes: once the shape is selected, the frequency can be continuously scaled. Figure 43 shows the measured magnitude and group-delay responses for the Chebyshev and Inverse Chebyshev responses. The Chebyshev filter provides very sharp roll off but has large group-delay variation, whereas the Inverse Chebyshev filter has smoother roll-off but a flat group delay. The passband group-delay variation in Inverse Chebyshev mode is less than $\pm 2.5\%$ for $f_c/3 < f < f_c$. This filter allows the user to trade off group delay performance and roll-off dynamically by selecting the filter approximation that best suits the target application.

The cascade architecture both facilitates frequency tuning and allows us to tap intermediate filter outputs to generate lower-order filters. If, for example, only a third-order filter is necessary, the final biquad can be powered down and the first two stages can provide a third-order filter at reduced power. Figure 44 displays three different filter orders $(1^{\text{st}}/3^{\text{rd}}/5^{\text{th}})$ of Chebyshev filters attainable from this architecture.

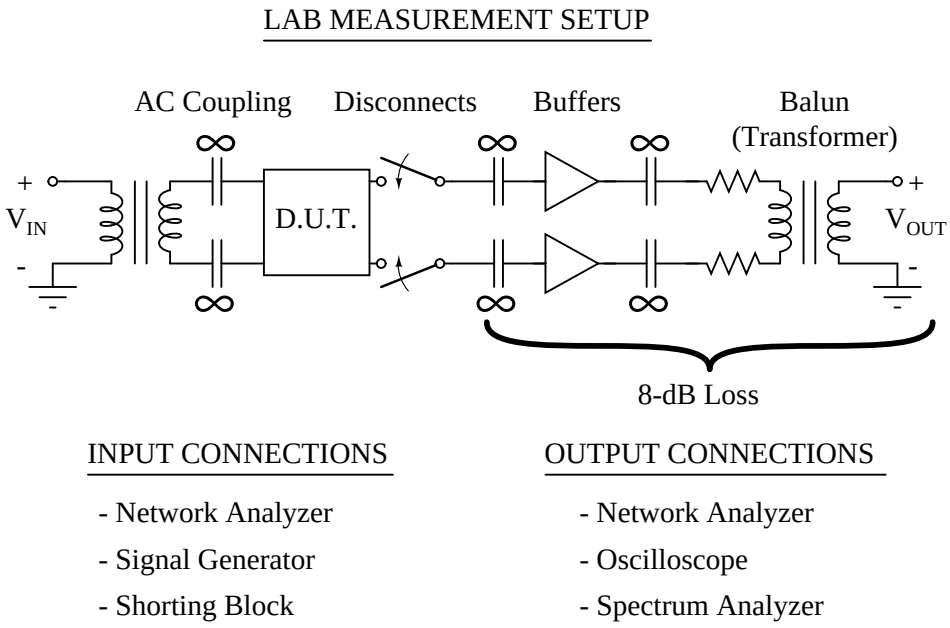


Fig. 41. Measurement setup

Figure 45 illustrates two-tone test(s) whose measurement results yield an inband IIP3 of 31.3dBm for 300kHz and 330kHz tones. Figure 46 shows IIP3 measurement results vs. power consumption. As shown in Figure 46, linearity deteriorates at lower power levels due to decreased opamp driving capabilities. Therefore, if linearity is not a concern, then power can be scaled with frequency. In addition, Figure 47 displays the out-of-band IIP2 and IIP3 performance of the filter for both low- and high-frequency modes. Out of band IIP2 is high as expected, given the fully differential architecture. Higher out-of-band IIP2/3 at lower frequencies is most likely due to increased opamp gain at those frequencies. Mobile wireless applications have specific linearity requirements. For example, analog baseband filters designed for GSM need both $2^{nd}-$ and $3^{rd}-$order high-linearity (IIP3 of around 20 dBm and IIP2 of around 45dBm) and a low cut-off frequency (around 115 KHz) [39]. Although in its present configuration, this filter does not cover that low of a cutoff frequency, this filter surpasses the linearity requirements for GSM application. In order to

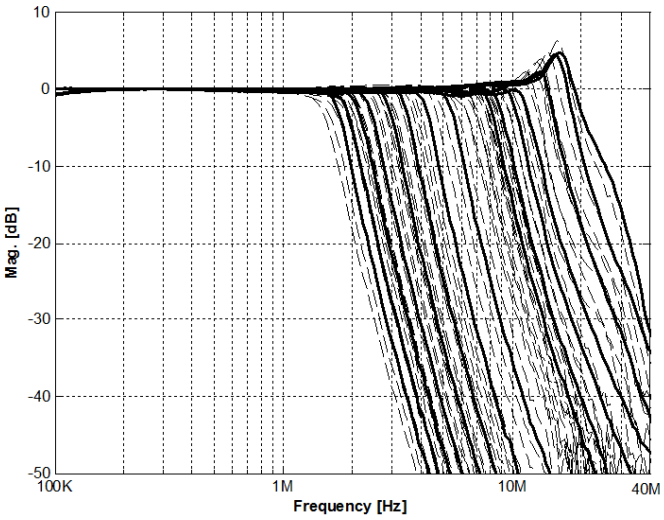


Fig. 42. Combined discrete (solid) and continuous (dashed) frequency tuning for low and high frequency modes

adapt the frequency coverage of the filter for GSM applications as well and further scale down the frequency, extension of the same techniques (combination of CIM and capacitor bank) could be employed.

Table VIII compares the filter performance to that of recently published works. The dynamic range of this work is slightly lower than some other works because the filter is higher order (hence more noise–as noise is reported for entire $5^{th} - order$ filter), and because this filter has greater reconfigurability (e.g. [43] has a fixed frequency). This work provides higher linearity and a greater level of flexibility in order/type selection, continuous frequency-tuning range, and power adjustment compared to recently published works.

C. Conclusion

This work has proposed a biquad design methodology, and has presented a highly reconfigurable filter with cut-off frequency tunable from 1MHz to 20MHz, which covers the range

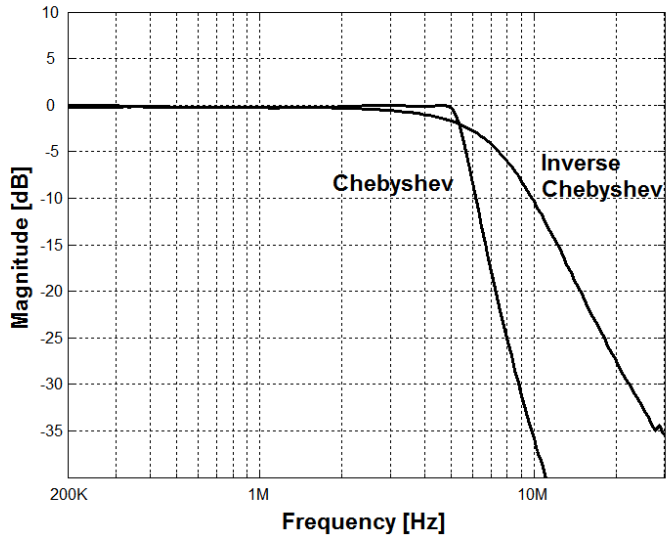
Table VIII. Comparison to recently published works

	Topology	Order	Type [*]	Power [mW]	Power/pole [mW/pole]	V_{DD} [V]	f_c Range [MHz]	Continuous Tuning?	Noise $[nV/\sqrt{Hz}]$	DR [dB]	IIP3 [dBm]
[57]	Source Follower	4	-	4.1	1.02	1.8	6-14	No	7.5	79	17.5
[43]	Active-RC	5	C	11.25	2.25	1.5	19.7	No	30	69	18.3
[42]	Active-RC	5(C)/3(E)	C/E	4.6	0.92	1.2	5, 10	No	85, 143	73	18.8-21.3
[38]	Active-G_m-RC	4	-	3.4 14.2	0.85 3.55	1.2	1.45-3.6 5.87-19.44	No	24.8	81	21
[39]	G_mC	3	B	2.5-3.1 6.5-7.3	0.83-1.03 2.16-2.43	2.5	0.05-0.35 0.25-2.2	Yes	35-700	-	22, 28
[37]	G_mC	3	B	1.57-1.92	0.52-0.64	1.0	0.135-2.2	Yes	65	-	16.3-20.1
This Work	**Active-RC**	**1/3/5**	**C/I**	**3.0-7.5**	**0.6-1.5**	**1.0**	**1-20**	**Yes**	**85, 52**	**71.4**	**31.3, 26**

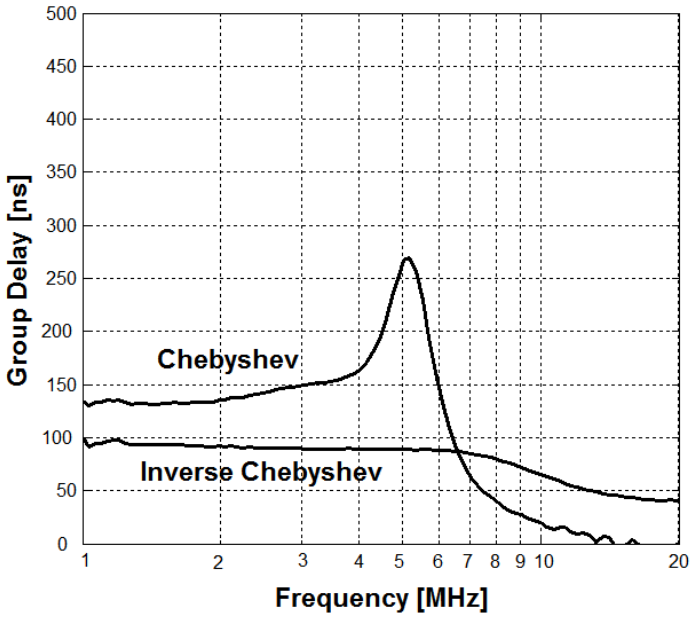
*B-Butterworth, C-Chebyshev, I-Inverse Chebyshev, E-Elliptic

**All the implementations are realized in $0.13\mu m$ CMOS technology except for [39], which is fabricated in $0.25\mu m$ SiGe BiCMOS and [37], which is fabricated in $0.18\mu m$ CMOS

of baseband LP filters for multiple wireless/wireline standards. The frequency response is reconfigurable (Chebyshev/Inverse Chebyshev), allowing better selection between group-delay or stopband roll-off performance. The filter's cascade architecture both facilitates tuning and provides dynamic order selection $(1^{\text{st}}/3^{\text{rd}}/5^{\text{th}})$, allowing the user to deactivate unnecessary stages and save power. Also, an efficient continuous frequency-tuning scheme for active-RC filters using a Continuous Impedance Multiplier (CIM) was proposed. Furthermore, a new biquad stability metric, Minimum Acceptable Phase Margin (MAPM), was introduced. This metric aids in the design of reconfigurable filters by providing tradeoff curves between phase margin and GBW for a given biquad ω_o and Q. Moreover, these tradeoff curves showed how the filter's power could be adjusted dynamically without risking instability. A large-scale common-centroid matched-capacitor-array layout was detailed with planned signal routing and shielding to reduce crosstalk and hence to maintain linearity at higher frequencies. These layout techniques coupled with a high-gain, low-voltage opamp design have yielded an IIP3 of over 31dBm, making the filter suitable for multiple highly linear wireless/wireline standards.



(a)



(b)

Fig. 43. Filter shape selection Chebyshev/Inverse Chebyshev (a) magnitude and (b) group-delay response

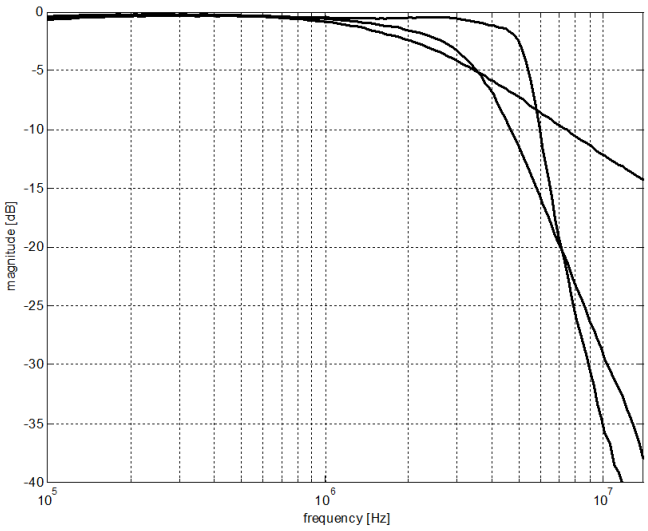
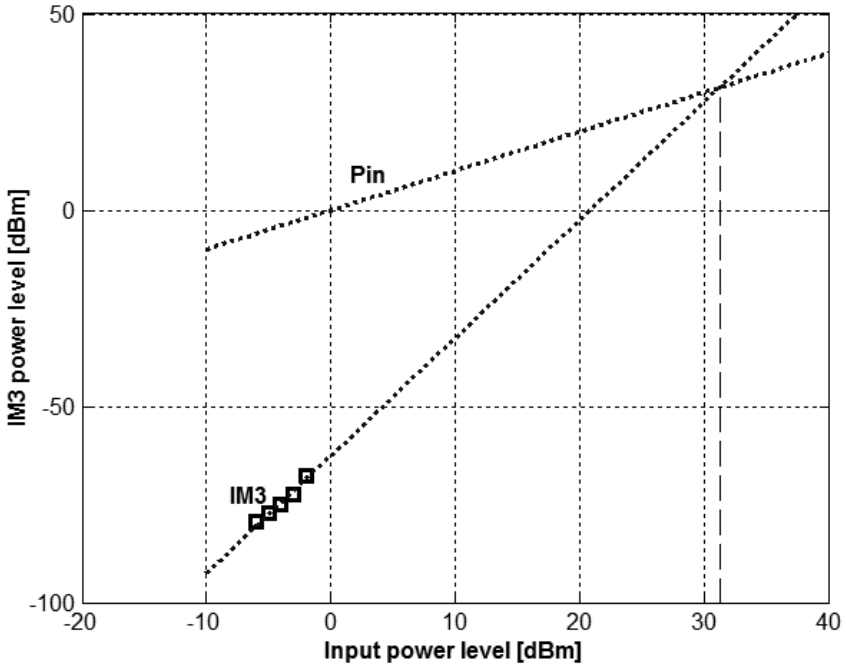
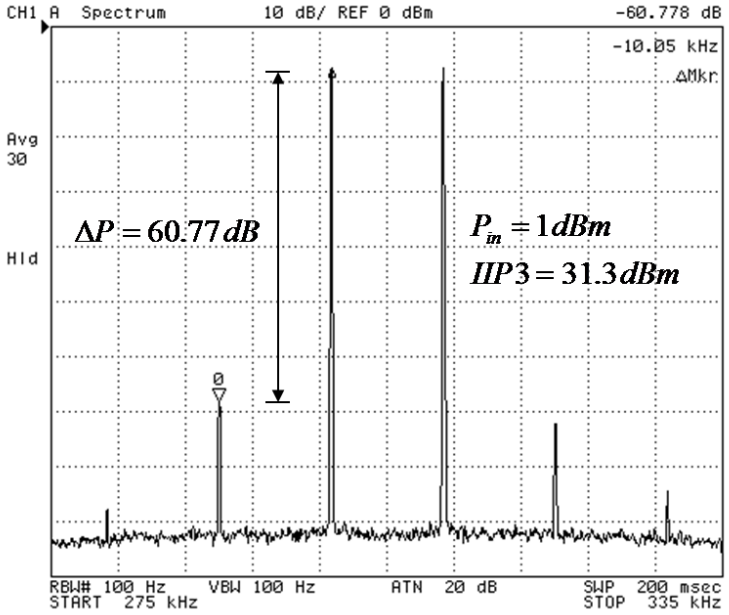


Fig. 44. Chebyshev filter order selection $(1^{st}/3^{rd}/5^{th})$



(a)



(b)

Fig. 45. IIP3 two-tone measurements: (a) sweep, (b) $P_{in} = 1dBm,\ f_{1,2} = 300kHz,\ 330kHz$

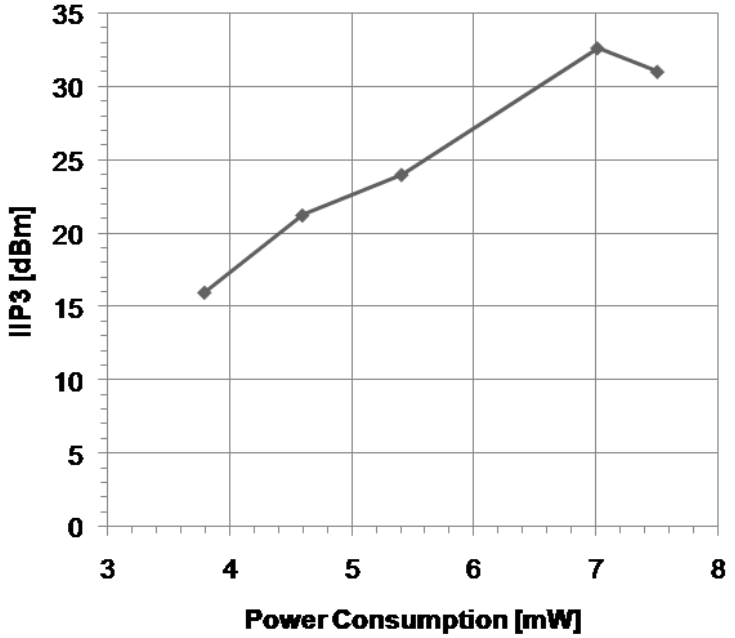
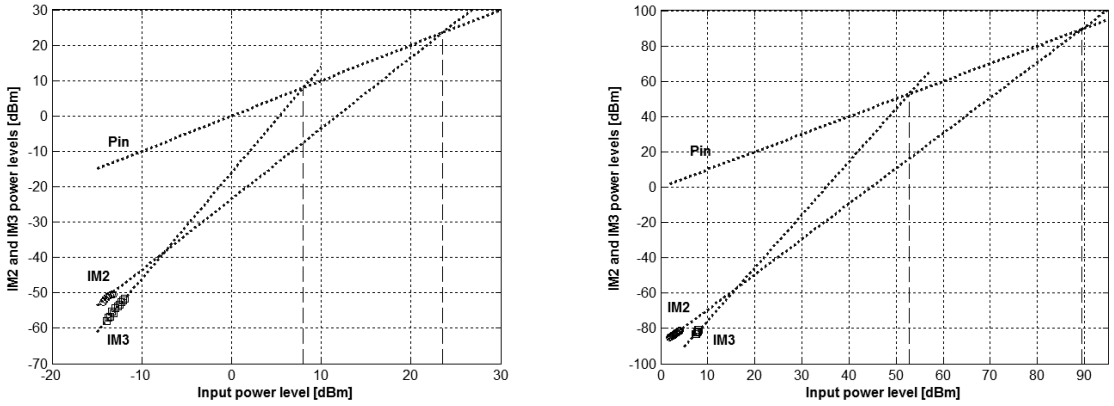


Fig. 46. Filter IIP3 vs. power consumption in low-frequency mode



(a) (b)

Fig. 47. IIP2 and IIP3 out-of-band in (a) HF Mode, (b) LF Mode

CHAPTER VII

SUMMARY AND FUTURE WORK

A. Summary

Rapid development of low-power portable wireless/wireline devices and competition-driven urge to decrease the cost of the finished products have pushed IC designers to adapt low-power techniques in circuit and system levels and introduce more cost-cutting methods to meet the such demands. Introduction of current-sharing architectures to lower power consumption, emergence of dynamic applications such as software-defined radio and multi-standard transceivers which try to lower their costs by increasing their utility, and prevalence of built-in self test (BIST) techniques which reduce post-fabrication costs, all could be interpreted in that light. This dissertation presented three major novel approaches both at the baseband and RF front-end to meet the goal of low-power, low-cost communication devices (wireless or wireline) possible.

1. A merged stacked PA/VCO (PVCO) architecture was proposed for application in a direct-modulation transmitter. A CMOS prototype was fabricated and tested operating at 2.4GHz and delivering 0 dBm output power to a 50 Ω antenna. The proposed architecture reuses the current and saves power. Current reuse saves power by sharing the same bias current and optimally distributing the supply voltage while using a single supply. Employing a current-reused structure and utilization of FSK direct-modulation yields a compact, low-power transmitter.

2. A simple, self-contained on-chip self-tuning system was proposed that automatically tunes the output resonance tank of the TX power amplifier to its optimum value (frequency of operation). The proposed BIST technique reduces the post-fabrication costs of trimming the resonant tanks by mitigating requirements for very costly au-

tomatic test equipment (ATE) and does not require any ADC, DSP or external signal generator. The overall system was fabricated and verified operating on the fabricated direct-modulation transmitter. Potential interactions of adjacent resonant tanks in transceiver architectures (PA and VCO in this case) were analyzed and an isolating resistive-buffer solution was presented. Also frequency-dependent no-linear operation of a Gilbert-cell-based power detector was examined and experimentally verified.

3. A novel biquad design methodology was presented and a highly linear, highly reconfigurable Active-RC filter with adjustable power was proposed with a continuously-tunable range of 1MHz-20MHz that covers the range of baseband LP filters for multiple wireless/wireline standards. Frequency response of the proposed baseband filter is reconfigurable, supporting better selection of a smooth group-delay or sharp stop-band roll-off. Cascade configuration provided with order selection of $(1^{\text{st}}/3^{\text{rd}}/5^{\text{th}})$ along with ease of tuning. Also, a novel efficient continuous frequency tuning scheme for Active-RC filters called Continuous Impedance Multiplier (CIM), was developed. Additionally, a new biquad stability metric, Minimum Acceptable Phase Margin (MAPM), was introduced to facilitate in the design of reconfigurable biquad filters by providing trade-off curves between phase margin and GBW of opamps for a given biquad ω_o and Q so power could be adjusted dynamically without risking instability.

B. Future Works

The ideas presented in this dissertation could be further extended and studied as future research topics. Extension of these ideas into different applications could be the next step in lowering cost and power consumption of communication devices.

The compact direct-modulation transmitter presented in this work was tested and ver-

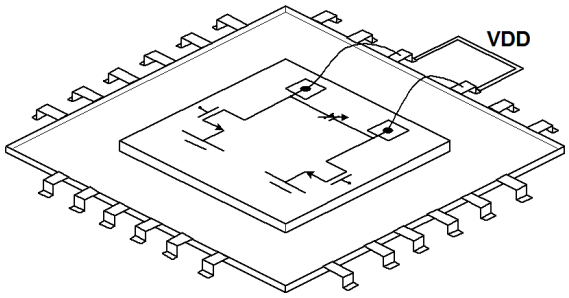


Fig. 48. An amplifier with an LC tunable tank at the output employing bondwires as high--quality inductors

ified with its free-running VCO. However, the remaining components of the intermittent PLL could be designed and verified to compensate for frequency drifts arising from process, temperature and voltage variations. Intermittent use of PLL would also reduce phase noise and would allow an increase bit rate for the same occupied bandwidth. Other components of this PLL (PFD, charge-pump, divider, etc) should also be designed power efficient. Slot-by-slot control of the VCO is when the loop closes to compensate for drift and then data is applied directly to VCO when the loop opens. Another idea could be to apply the binary data directly to divider. This means the loop is always closed and to switch between two frequencies, divider according to binary data switches between two different divisors. Studying the effect of data rate on the stability of the loop would be vital to such research. Also settling time of the loop and its relation with output data rate should be taken into consideration. This could potentially result in a power-and-bandwidth-efficient direct-modulation transmitter.

The automatic on-chip tuning method proposed in this dissertation, due to its simplicity, has great potential to be used in different applications like automatic and robust LNA input-matching or self-tuning of LC tank in the LNA output to maximize its gain. Another great application could be in resonant tanks in LNAs or PAs where a tank is formed using an array of on-chip capacitors and bondwire as an inductor. Bondwires when used as

inductor offer a high quality factor (Q) and hence are good in narrow-band applications candidates for reducing power, phase noise and distortions. However the value of the their inductance greatly depends on their physical attributes like length, diameter and could vary from one chip to another. Self-tuning system proposed in this work could greatly benefit such designs by automatically tuning these tanks to their optimum point and compensating for variations in packaging process while utilizing the high quality factor of bondwires. Figure 48 depicts an example of such applications.

The highly reconfigurable, multi-standard presented in this work could also be extended to include more approximations types in applications. Its frequency range could be easily modified to include even lower frequencies where GSM applications exist while meeting the required linearity. In this design, Q of each biquad is hard-wired by the ratio of resistors and the control knobs of their corresponding CIM are all connected together, being controlled by the same voltage (V_C). However as an extension to this work, a slightly modified CIM scheme in which resistors R_{Qk} were tuned independently could be designed to mitigate Q enhancement that occurs as a result of BW limitations.

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APPENDIX

Journal Publications based on this dissertation:

1. H. A. Aslanzadeh, E. Pankratz, E. Sánchez-Sinencio, "A 1-V +31dBm IIP3, Reconfigurable, Continuously Tunable, Power-Adjustable Active-RC LPF", *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 495-598, Feb. 2009 (Listed in Top 100 most accessed IEEE documents for February 2009)

2. H. A. Aslanzadeh, E. Pankratz, C. Mishra, E. Sánchez-Sinencio, "A Current-Reused, 2.4 GHz Direct-Modulation Transmitter with On-Chip Automatic Tuning," Under review for publication

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