AN OFF-CHIP CAPACITOR FREE LOW DROPOUT REGULATOR WITH PSR ENHANCEMENT AT HIGHER FREQUENCIES

A Thesis

by

SEENU GOPALRAJU

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2010

Major Subject: Electrical Engineering

An Off-Chip Capacitor Free Low Dropout Regulator with PSR Enhancement

at Higher Frequencies

AN OFF-CHIP CAPACITOR FREE LOW DROPOUT REGULATOR WITH PSR ENHANCEMENT AT HIGHER FREQUENCIES

A Thesis

by

SEENU GOPALRAJU

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Approved by:

Chair of Committee,	Edgar Sanchez-Sinencio
Committee Members,	Kamran Entesari
	Shankar P. Bhattacharyya
	Duncan Henry M. Walker
Head of Department,	Costas Georghiades

December 2010

Major Subject: Electrical Engineering

ABSTRACT

An Off-Chip Capacitor Free Low Dropout Regulator with PSR Enhancement at Higher Frequencies. (December 2010)

Seenu Gopalraju, B.E., Anna University

Chair of Advisory Committee: Dr. Edgar Sanchez-Sinencio

Low Dropout Regulators (LDOs) are extensively used in portable applications like mobile phones, PDAs and notebooks. These portable applications demand high power efficiency and low output voltage ripple. In addition to these, the radio circuits in these applications demand high power supply rejection (PSR). The output voltage of a conventional DC/DC converter (generally switched mode) has considerable ripple which feeds as input to these LDOs. And the challenge is to suppress these ripples for wide range of frequencies (for radio units) to provide clean supply.

Enhanced buffer based compensation is proposed for the fully on-chip CMOS LDO which stabilizes the loop for different load conditions as well as improve the power supply rejection (PSR) until frequencies closer to open loop's unity-gain frequency. The stability and PSR are totally valid even for load capacitor varying from 0 to 100 pF.

The proposed capacitor-less LDO is fabricated in On-Semi 0.5 µm fully CMOS process. Experimental results confirm a PSR of -30 dB till 420 KHz for the maximum load current of 50mA. The load transients of the chip shows transient glitches less than 90 mV independent of output capacitance.

DEDICATION

To my entire family for their complete support and encouragement

ACKNOWLEDGEMENTS

I would like to first thank my advisor Dr. Edgar Sanchez-Sinencio for his guidance, motivation and support throughout the course of my research. Without my advisor's graduate level courses and group meetings, this thesis work wouldn't have been initiated. I would like to extend my gratitude to my committee members, namely, Dr. Kamran Entesari, Dr. Shankar P. Bhattacharyya and Dr. Duncan Henry M. Walker.

Thanks to Dr. Aniruddha Datta for substituting Dr. Shankar P. Bhattacharyya on my thesis defense presentation.

I would also like to thank my peers, namely, Joselyn Torres, Shriram Kalusalingam, Miguel Rojas, Ahmed Amer, Mohamed El-Nozahi and Reza Abdullah for their valuable input and moral support.

Finally, thanks to my mother, father, sisters and friends for their encouragement and love without whom I wouldn't have completed my graduate degree.

TABLE OF CONTENTS

Page

LIST OF FIGURES

FIGURE Page

FIGURE Page

LIST OF TABLES

1. INTRODUCTION: THE IMPORTANCE OF RESEARCH

In the recent years, the world has seen a huge boom in portable electronic products like cell phones, notebooks, PDAs etc., Most of these products are powered by a battery which requires power management circuitry to optimize the performance. As a result, lots of extensive researches have been carried across the world in power management field to improve various performances and also to reduce the cost of ICs. A power management circuitry consists of linear regulators (mainly LDOs), switching regulators (buck, boost converters and charge pumps) and digital control logic. Control logic helps to change between different voltage levels depending on the demand to optimize the power consumption and hence extend the battery life. Moreover battery discharges its voltage with time, but for optimal performance a constant voltage is required for a circuit. Fig. 1.1 shows the primary role of voltage regulators in a power management IC.

Since low-dropout (LDO) regulators don't use a zener diode, they are the most efficient and highly accurate regulators under the class of linear regulators compared to shunt or series voltage regulators. Because of these advantages, LDOs are the widely used linear regulators in on-chip power management ICs.

This thesis follows the style of *IEEE Journal of Solid-State Circuits*.

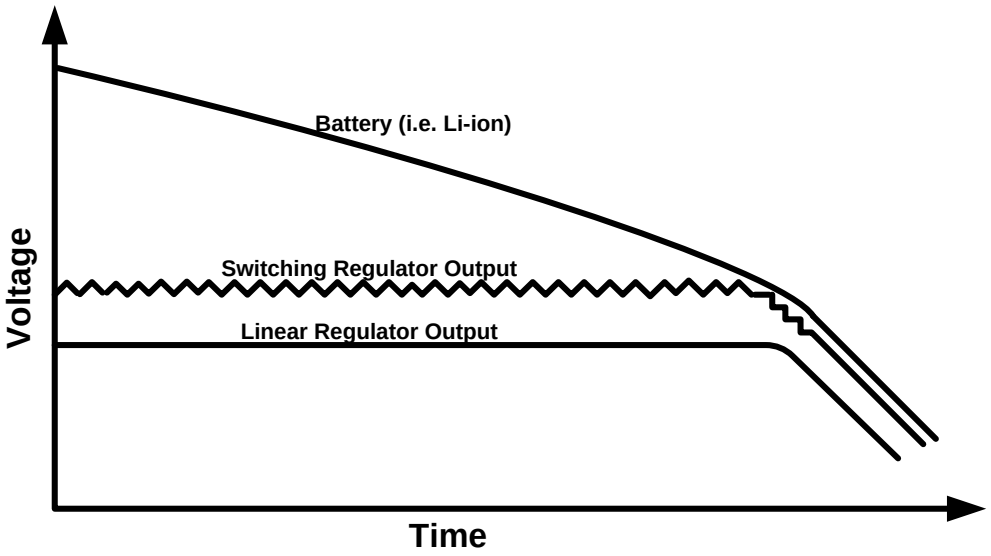


Fig. 1.1. Regulated Voltage vs. Battery Voltage

1.1. Increasing Linear Regulators Power Efficiency

Switching regulators output voltage has ripples at switching clock frequency. So LDOs have less noise compared to switching regulators but efficiency is lesser. Hence switching regulators can drive these LDOs before driving the load when the difference between the battery voltage and output voltage desired is larger. An example for the cascade of switching regulator and LDO is depicted in Fig. 1.2. The ideal efficiencies are also indicated.

Fig. 1.2. Increasing Power Efficiency of LDO

1.2. Application of LDO in Cell Phones

The detailed power management circuitry [1] for a basic cell phone is shown in Fig. 1.3. It is clear that LDOs supply current to Analog/Base Band, Digital and RF circuits like LNA, VCOs and PA. All these circuits in common demand a clean and fixed voltage which won't change with input voltage, output load current and temperature. Apart from these basic performances, LDOs driving RF circuits are expected to have better PSR at higher frequencies. The presented research is focused on improving the PSR of the LDO without using external components. The proposed LDO can be used to power up RF and analog blocks whose current consumptions are lesser than 50mA and can operate at 2.8V supply.

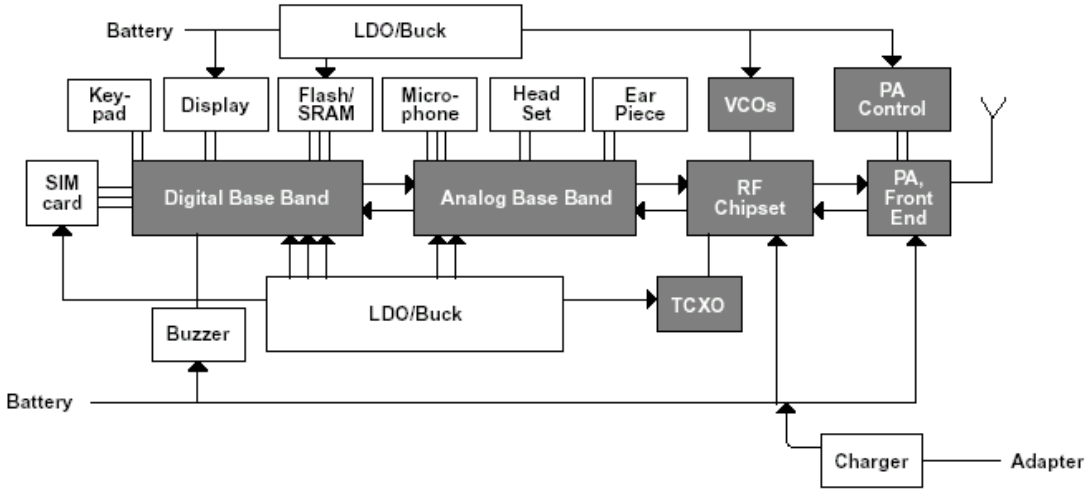


Fig. 1.3. Detailed Power Management Circuitry in Cell Phones

2. LOW DROPOUT REGULATORS IN GENERAL

2.1. Low Dropout Regulator Classification

LDOs can be classified based on the compensation mechanism used for their open loop stability. Conventional designs use huge off-chip capacitor at the output to create a dominant pole and hence increases cost of the LDO. And in some cases it utilizes the Electrical Series Resistance (ESR) of such capacitors for pole-zero cancellation. Stability achieved by this manner heavily depends on ESR value which changes with temperature. An internal zero can be generated to help compensation without the dependency on ESR and output capacitor. Using such a huge off-chip capacitor poses several integration issues. A simple Miller compensation guarantees stability in a capacitor-free fashion. This saves cost and lot of board area and makes the LDO suitable for SOC design. But this kind of internal compensation has poor load transient and PSR performances compared to the conventional one. A differential auxiliary loop can be added to reduce the undershoots and overshoots occurring during the load transients [2] as depicted in Fig. 2.1. Faster transient response time and hence a better figure of merit can be achieved by using replica biasing scheme [3] as shown in Fig. 2.2. The PSR can be improved in a capacitor-free LDO by using a NMOS cascode over the PMOS pass transistor but it requires charge pump to boost the input voltage [4]. Feed forward ripple rejection technique can be applied to conventional LDO to achieve good PSR over a wide range of frequencies [5] as shown in Fig. 2.3.

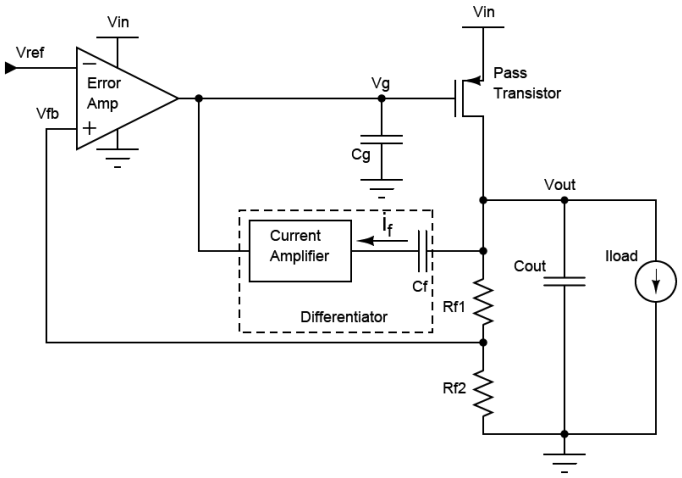


Fig. 2.1. Block Diagram of Differentiator Based LDO Proposed in [2]

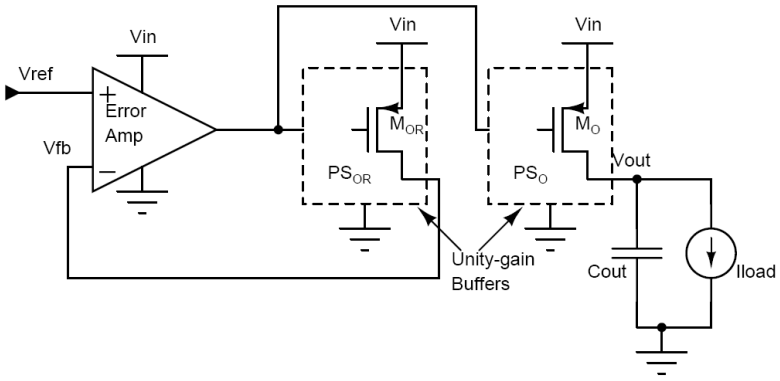


Fig. 2.2. Block Diagram of Replica Biased LDO Proposed in [3]

In this research an output capacitor-free compensation scheme is employed with the help of Miller capacitor and enhanced unity gain buffer. The proposed technique enhances the frequency range over which sufficient power supply ripples are rejected without affecting the load transient response and hence achieving a very good figure of merit defined in [3] which is indicated below as FOM.

$$\text{FOM} = \frac{[C_{out} + C_M] * \Delta V_{out}}{I_{LOAD,max}} * \frac{I_Q}{I_{LOAD,max}}$$

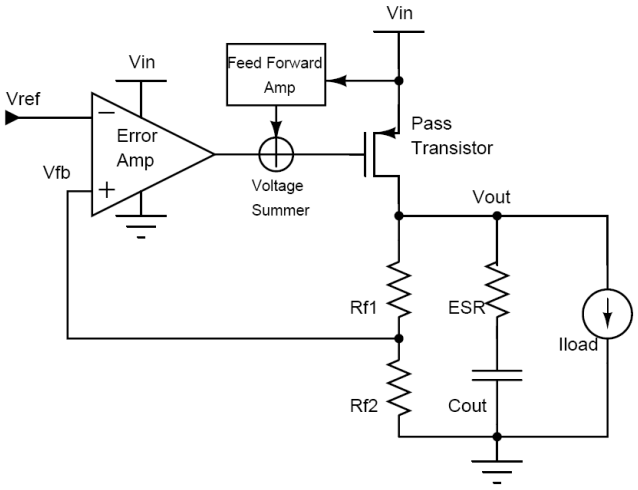


Fig. 2.3. Block Diagram of Feed-Forward LDO Proposed in [5]

2.2. LDO Design Parameters

A simple LDO architecture is shown in Fig 2.4. Power efficiency for a LDO is directly proportional to the dropout voltage (V_{DO}) which is the difference between the input and output voltage. In general power efficiency is given in (1).

$$\eta = \frac{V_{out} * I_{out}}{V_{in} * I_{in}} = \frac{(V_{in} - V_{DO}) * I_{out}}{V_{in} * (I_Q + I_{out})} \quad (1)$$

In (1), I_Q is the total quiescent current for the circuit, V_{in} is the input power supply voltage, I_{out} is the load current delivered and V_{out} is the regulated output voltage. When the load current is zero, power efficiency shown in (1) is not valid and in such case the quiescent current I_Q quantifies the performance.

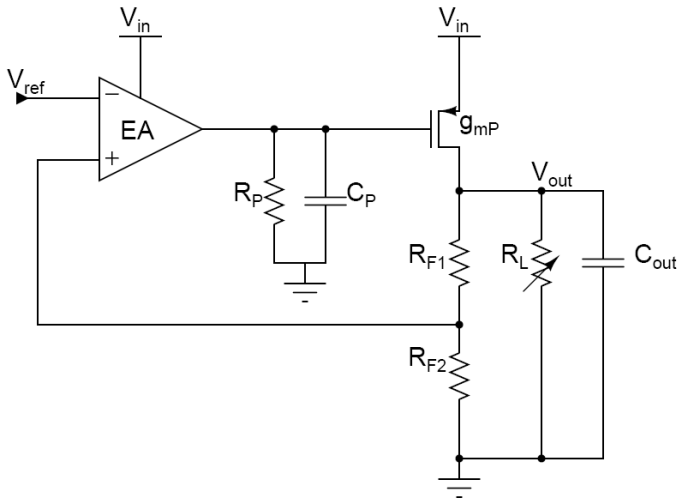


Fig. 2.4. Simple Two Pole LDO Architecture

In general, the regulated output voltage for V_{out} a LDO depends on the Bandgap reference voltage (V_{ref}) and is expressed in (2a). A_{OL} is the open-loop gain of the LDO and A_{EA} is the error amplifier gain. Assuming $A_{OL} \gg 1$, V_{out} can be simplified as shown in (2b). β is the feedback ratio which is given in (3).

$$V_{out} = \left(\frac{A_{OL}}{1 + A_{OL}}\right)\left(1 + \frac{R_{F1}}{R_{F2}}\right)\left[V_{ref} + \frac{V_{in}}{A_{EA}}\right] \tag{2a}$$

$$V_{out} \approx \frac{V_{ref}}{\beta} + \frac{V_{in}}{A_{OL}\beta} \tag{2b}$$

$$\beta = \frac{R_{F2}}{R_{F1} + R_{F2}} \tag{3}$$

The loop is usually broken in the feedback, at the positive input of the error amplifier (EA) to analyze the open-loop stability of the LDO. Line regulation is a measure of change in output voltage for a change in input voltage. From (2), line regulation can be derived and it is inversely related to the open-loop gain A_{OL} as given in (4).

$$\frac{\Delta V_{out}}{\Delta V_{in}} \approx \frac{1}{A_{EA}\beta} \tag{4}$$

Load regulation is defined as the ratio of change in output voltage to the change in load current and it is related inversely to the loop gain as given by (5). R_{out} is the effective output resistance of the LDO which is the parallel combination of the resistance of the pass element (r_{dsP}), total feedback resistance ($R_{F1} + R_{F2}$) and load resistance (R_L) as shown in (6a).

$$\frac{\Delta V_{out}}{\Delta I_{out}} = \frac{R_{out}}{1 + A_{OL}\beta} \tag{5}$$

$$R_{out} = r_{dsP} \big|\big| (R_{F1} + R_{F2}) \big|\big| R_L \tag{6a}$$

$$r_{dsP} \approx \frac{1}{\lambda I_{Load}} \tag{6b}$$

The dependency of r_{dsP} on I_{Load} is shown in (6b). So as load current increases R_{out} decreases for a given channel length modulation factor (λ).

In LDO, thus high open loop gain (A_{OL}) is required to achieve better line and load regulation. Load Transient is a behavior which occurs when there is a sudden change in the load current. In a LDO, change from minimum to maximum load current results in undershoots and maximum to minimum results in overshoots at the output voltage. The output voltage overshoot is generally limited by the supply voltage (V_{in}), but the undershoot can go all the way down to ground potential.

These transient glitches can be reduced by either having a huge output capacitance (C_{out}) or faster loop response time (Δt) and it is given by (7). Loop response time (Δt) is the sum of the inverse of the closed-loop bandwidth of the LDO (BW_{CL}) and

slew rate time (t_{SR}). Since the pass transistors are generally designed for low-dropout which means lowers V_{dsat} at maximum current, they are usually very huge in size and constitute big parasitic capacitance ($C_P \approx C_{gsP} + g_{mP}R_{out} * C_{gdP}$) at its gate. C_{gsP} and C_{gdP} are the gate-source and gate-drain parasitic capacitance of the pass transitor. Slew rate time (t_{SR}) which depends on C_P, EA's output stage maximum current capability (I_{SR}) and voltage variations (ΔV_P) across C_P can be expressed as given in (8).

$$\Delta V_{out} = \Delta I_{out} * \frac{\Delta t}{C_{out}} \tag{7}$$

$$t_{SR} = \frac{C_P \Delta V_P}{I_{SR}} \tag{8}$$

$$\Delta t \approx \frac{1}{BW_{CL}} + t_{SR} \tag{9}$$

Thus from (7), to minimize the transient glitches we need either large output capacitance or from (9), higher BW_{CL} which means higher quiescent current. Hence output capacitor-less LDOs shows poor load transients compared to conventional LDOs. Settling time for output voltage during load transients depends on Δt and phase margin of the open loop.

The open-loop transfer function for the LDO shown in Fig. 2.4 has two left hand plane (LHP) poles and one right hand plane (RHP) zero as indicated in the below equation.

$$H_{OL}(s) = \frac{A_{OL}\left(1 - \frac{s}{C_{gdP}}\right)}{(1 + sR_P C_P)(1 + sR_{out}C_{out})}$$

2.3. General PSR Analysis

Fig. 2.4 shows a simple LDO architecture with two poles given by, $P_{out} = \frac{1}{R_{out}C_{out}}$ and $P_{int} = \frac{1}{R_P C_P}$. Consider the two cases where $P_{out} \ll P_{int}$ (Conventional Compensation) and $P_{int} \ll P_{out}$ (Capacitor-Free Compensation). The PSR model for this simple LDO is shown in Fig. 2.5. The transfer function for the PSR is given by (10a).

$$\frac{V_{out}}{V_{in}} = \frac{P_{out}P_{int}A_P\left(1 + \frac{s}{P_{int}}\right)}{s^2 + s(P_{out} + P_{int}) + A_P A_{EA}\beta P_{out}P_{int}} \tag{10a}$$

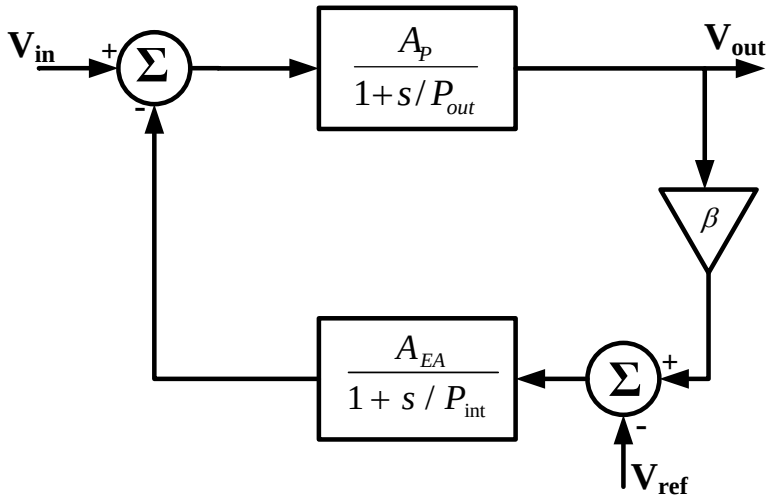


Fig. 2.5. PSR Model of Simple LDO Architecture

A_{EA} and $A_P = g_{mP}R_{out}$ are the error amplifier and pass transistor stage gain respectively and β is the feedback factor. In real case the off-chip capacitor used for external compensation has ESR (Equivalent Series Resistance) and ESL (Equivalent Series Inductance) as shown in Fig. 2.6 which makes the PSR curve to rise instead of

moving down at higher frequencies. Corresponding PSR plots for the two cases are shown in Fig. 2.7 which indicates that high PSR over a wide range of frequencies can be achieved only if LDO is externally compensated. The pole-zero locations for the conventional and capacitor-less LDO are shown in Fig. 2.8a and Fig. 2.8b respectively.

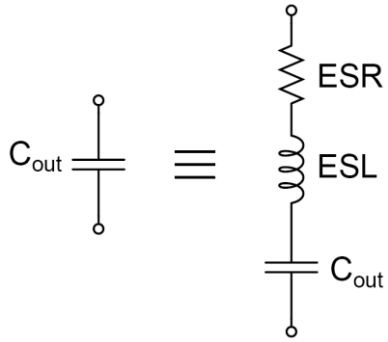


Fig. 2.6. Equivalent Model of Huge Capacitance

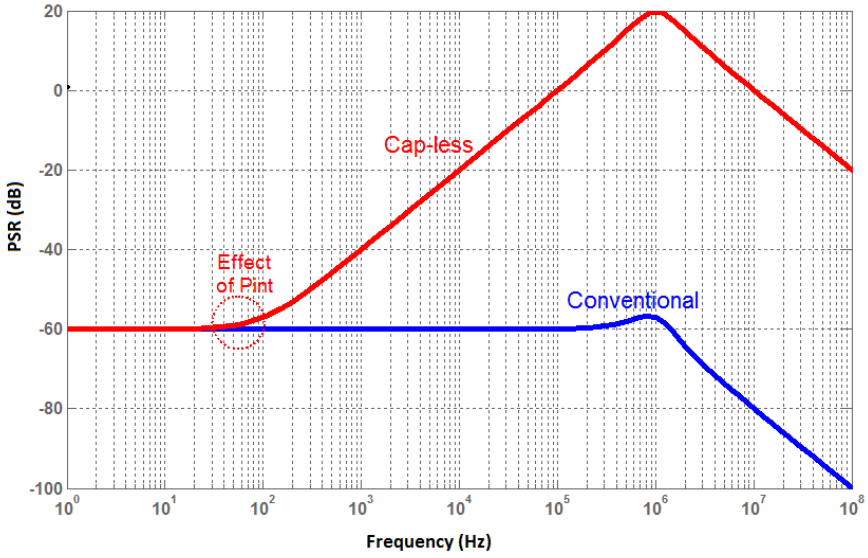
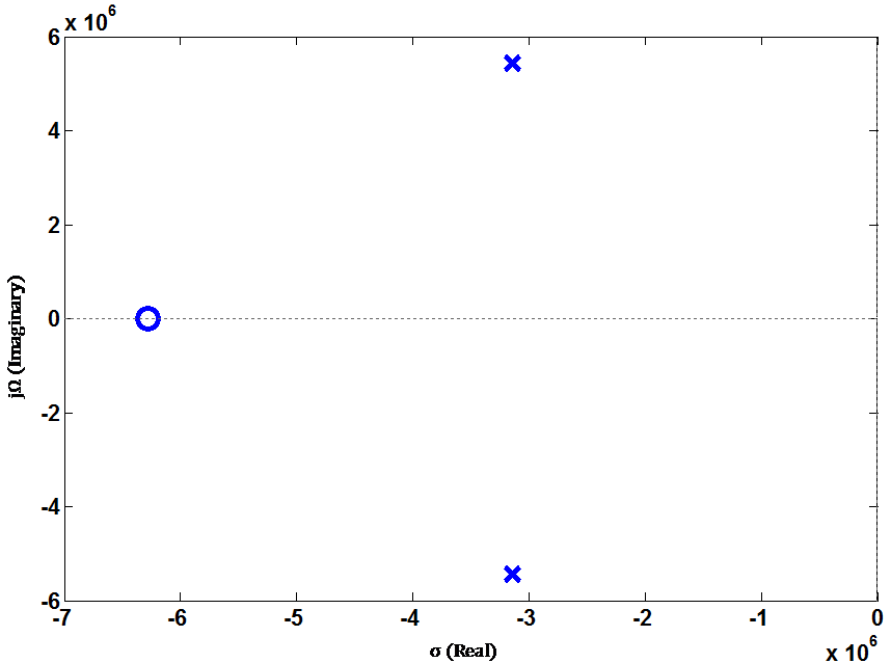
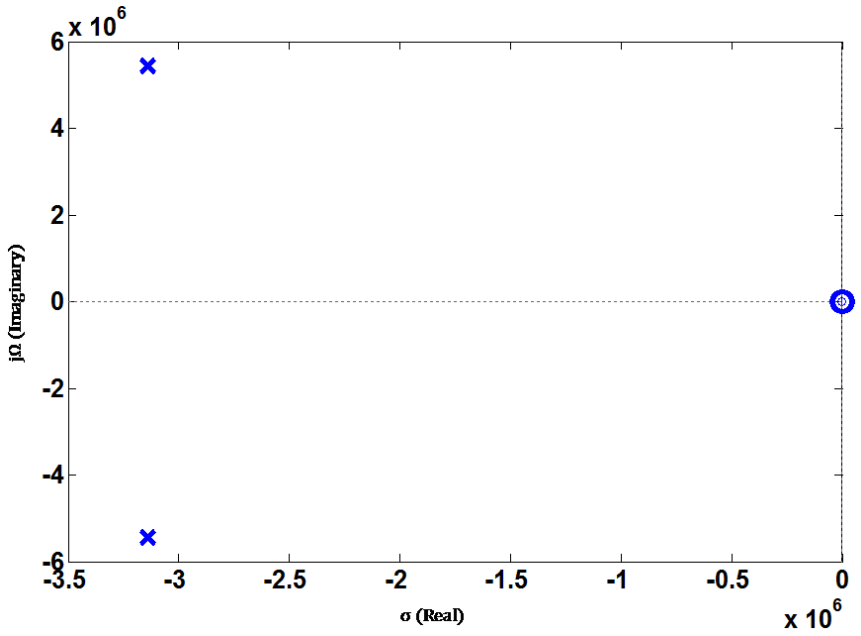


Fig. 2.7. PSR for Conventional and Capacitor-less Compensations



(a)



(b)

Fig. 2.8. PSR Pole-zero Map for (a) Conventional (b) Cap-less LDO

It is clear from (10a) and Fig. 2.7 that the PSR starts to degrade after P_{int} frequency for internally compensated capacitor-free LDO unlike the conventional LDO. So this means for the capacitor-free architecture dominant pole within the loop act as the zero in the PSR in the transfer function. This conclusion paves the way for a simple solution of nullifying the zero effect of P_{int} by introducing a pole in the PSR which means a zero in the loop. The required pole P_{req} in the PSR needs to be very close to P_{int}, so it should be a low frequency zero in the loop. The transfer function for the desired PSR looks like the one shown in (10b). Assuming a single dominant pole within the open-loop UGF, a low frequency zero leads to stability issues. Passive low frequency zero means huge resistance and capacitance, hence even if the stability is taken care, such a low frequency zero within the loop will affect transient performances due to slewing. The proposed topology introduces a zero within the loop which doesn't affect the stability at all but nullifies the effect of P_{int} in the PSR.

$$\frac{V_{out}}{V_{in}} = \frac{P_{out}P_{int}A_P\left(1+\frac{s}{P_{int}}\right)}{[s^2 + s(P_{out}+P_{int}) + A_P A_{EA}\beta P_{out}P_{int}](1+\frac{s}{P_{req}})} \quad (10a)$$

In the PSR model shown in Fig. 2.5, it is assumed that the only path from V_{in} to V_{out} is through the pass transistor. But the error amplifier used in the LDO loop also gets bias from the same noisy supply V_{in}. To get the actual PSR of the LDO, the error amplifier path should also be accounted. The following section 2.4 analyses the PSR of the error amplifiers.

2.4. Choice of Error Amplifier

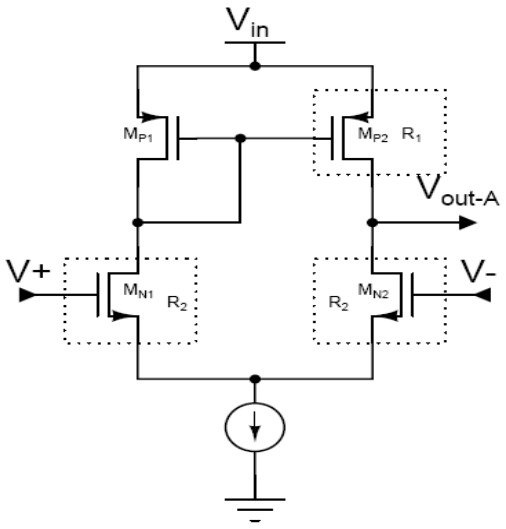
The error amplifier's output is going to drive the gate of the series pass transistor. The amount of power supply ripples at the output of the error amplifier depends on whether the gate to drain diode connected transistor is a PMOS or NMOS [6]. For the PMOS diode connected case as shown in Fig. 2.9a, the PSR can be derived as expressed in (12) with the help of small signal PSR model shown in Fig. 2.9b. R_1 and R_2 are the equivalent impedance of PMOS and NMOS transistors.

$$V_{out-A} = \frac{V_{in}R_2}{R_1 + R_2} + i_{R2}(R_2||R_1) = V_{in} \tag{11}$$

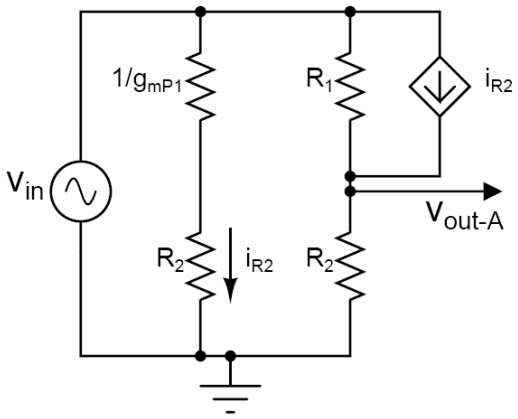
$$\text{where } i_{R2} = \frac{V_{in}}{R_2} \text{ (assume } \frac{1}{g_{mP1}} \text{ to be less)}$$

$$PSR = \frac{V_{out-A}}{V_{in}} = 1 \text{ (0 dB)} \tag{12}$$

From (12), PMOS diode connected error amplifier passes all the V_{in} noise to its output. For a PMOS pass transistor, the source of the pass element is connected to V_{in}. So if same ripples arrive at the gate then the PSR value will be very high at DC for the LDO since $\Delta V_{sg} \approx 0$. But the bandwidth of the PSR will be lesser [6].



(a)



(b)

Fig. 2.9. NMOS Error Amplifier (a) Circuit (b) Small Signal Model

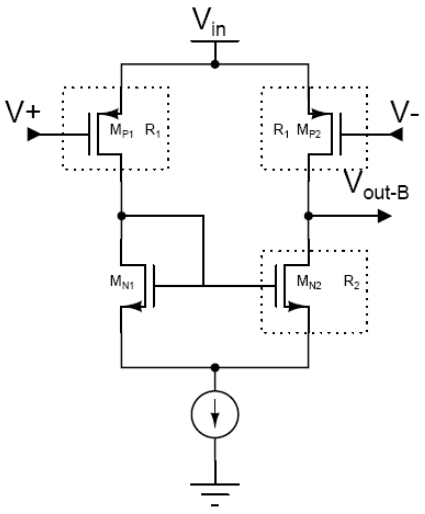
In the case of NMOS diode connected error amplifier as shown in Fig. 2.10a, the PSR can be derived as infinite in dB as shown in (14). The corresponding small signal model is shown in Fig. 2.10b.

$$V_{out-B} = \frac{V_{in}R_2}{R_1 + R_2} - i_{R1}(R_1||R_2) = 0 \quad (13)$$

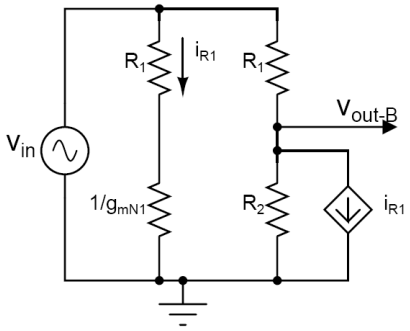
where $i_{R1} = \frac{V_{in}}{R_1}$ (assume $\frac{1}{g_{mN1}}$ to be less)

$$PSR = \frac{V_{out-B}}{V_{in}} = 0 \quad (14)$$

From (14), no noise from V_{dd} arrives at the output of the error amplifier with NMOS diode connection. For a NMOS pass device LDO, the source of the NMOS is the output of the LDO. So the output follows the signal at the gate of the NMOS. Hence very low supply ripples are required at the output of the error amplifier. For this case the NMOS diode connected error amplifier can be used. But NMOS pass device requires the gate voltage to be higher ($V_{out} + V_{th}$) which means boosted V_{in} for the error amplifier. For boosting the V_{in}, generally charge pumps are used which add cost and complexity to the circuit [4]. If PMOS pass device is used with the error amplifier shown in Fig. 2.10a, the DC PSR will be lesser but the bandwidth can be extended compared to a PMOS LDO using error amplifier shown in Fig. 2.9a [6]. The above discussion can be extended to folded cascode error amplifiers in the similar way [6]. Irrespective of the error amplifier architecture, its gain should be as high as possible to have very high DC PSR.



(a)



(b)

Fig. 2.10. PMOS Error Amplifier (a) Circuit (b) Small Signal Model

So for the LDO PSR model shown in Fig. 2.5 and related discussion, NMOS diode connected error amplifier will be a better choice. The summary for the section 2.4 is tabulated in Table I for PMOS pass transistor LDO.

TABLE I

PSR SUMMARY FOR PMOS PASS TRANSISTOR LDO

Architecture	DC PSR	BW
NMOS Error Amplifier	High	Low
PMOS Error Amplifier	Low	High

2.5. PSR Background Study in Cap-Less LDOs

In [7] different design methodologies as shown in Fig. 2.11 are discussed for improving the PSR of a LDO. In R-C filtering as shown in Fig. 2.11a there will be a increase in power losses and high dropout voltage due to resistance. Two LDOs can be connected in series like in Fig. 2.11b but there will be higher dropout voltage and increased power and there is no guarantee that BW of PSR will increase. NMOS cascode as depicted in Fig. 2.11c requires two charge pumps to boost the gate voltage of the cascading NMOS and power supply of error amplifier (to provide sufficient drive voltage for NMOS pass transistor). In the NMOS cascode approach, circuit complexity, area and power increases. And moreover the R-C filters employed in Fig. 2.11c are of high value to have very low corner frequency around the BW of the error amplifier. The circuit shown in Fig. 2.11d suffers from larger dropout voltage and increased power.

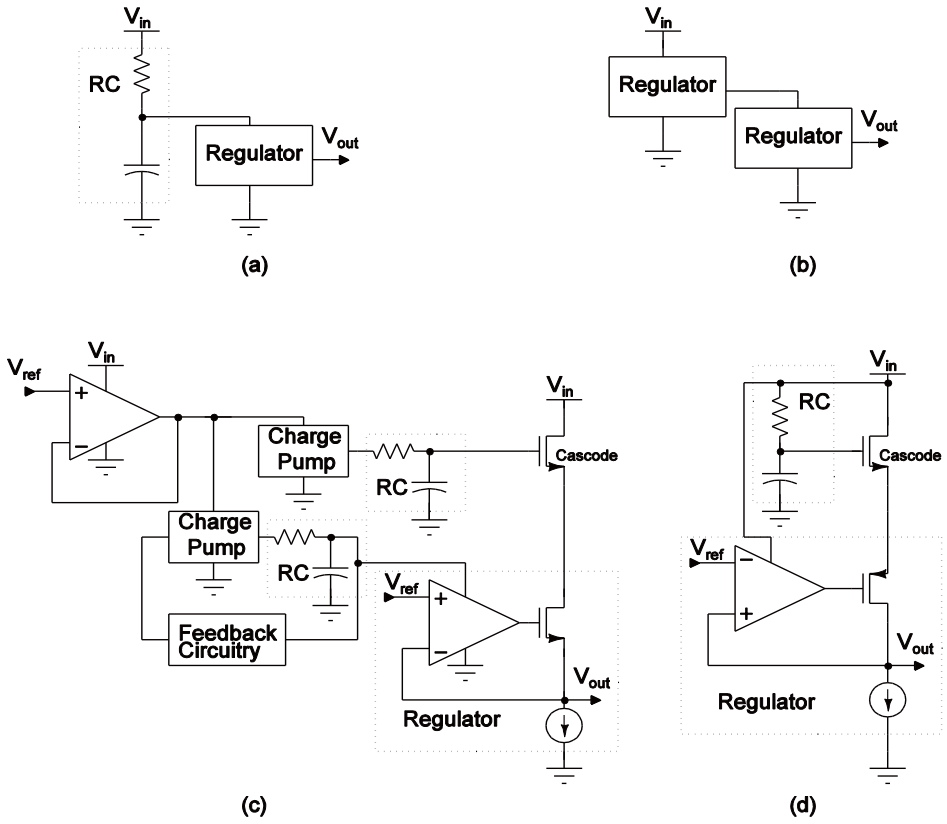


Fig 2.11. Previously Used Circuits to Improve PSR. (a)R-C Filtering (b) Series Connection of LDO, (c)NMOS Cascod with charge pupms (d) NMOS Cascode with just RC filtering

In [4], circuit shown in Fig. 2.11d is modified using a charge pump as shown in Fig. 2.12. The MNC transistor acts as a cascode to pass transistor MP21 and hence help to achieve high PSR by increasing the resistance from supply voltage to output. In order to bias the NMOS MNC the gate voltage need to be boosted with charge pump. RC filtering need to be carried at the gate of MNC to make ripple free bias or else the source will follow any ripples in the gate and thus degrades the performance of the LDO. The RC filtering shunts those ripples to ground. In this work the on-chip capacitance used is 60 pF. The worst case PSR achieved is -27 dB over the wide range of frequencies but the

maximum load current which it can deliver is just 5mA which is very less for today's RF circuits. The summary for the background study of PSR in reported cap-less LDOs is tabulated in Table II.

In the literature only very few Cap-less LDOs are concentrated on improving the PSR compared to conventional LDOs with huge capacitance. Though certain cap-less LDOs publications show good PSR, they are not supported by a solid mathematical explanation. In the presented research PSR analysis is carried for the proposed cap-less LDO which is supported by mathematical derivations and Matlab simulations proving the concept. The chip's experimental PSR results also confirm the working concept.

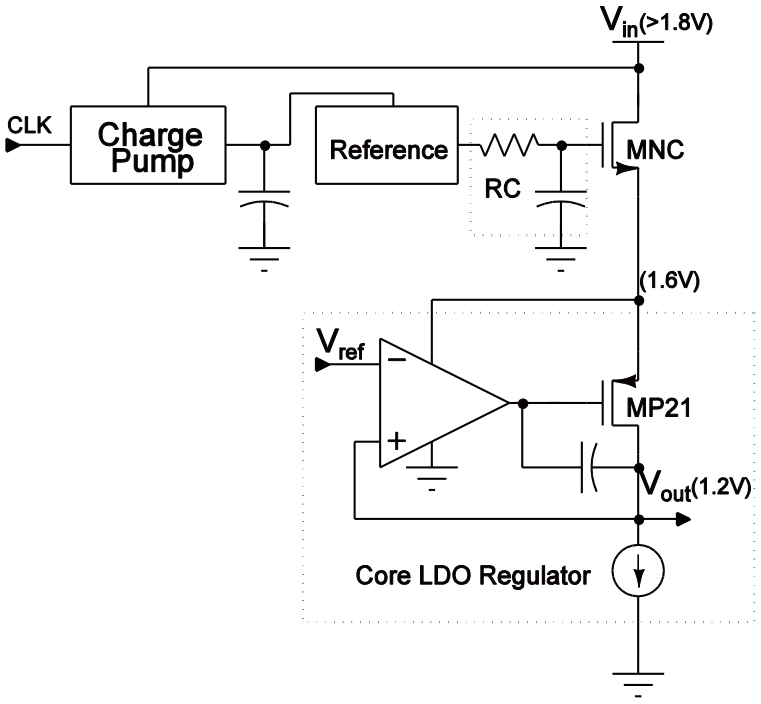


Fig. 2.12. PSR Enhancing Circuit [4]

TABLE II

STRENGTHS AND WEAKNESS OF REPORTED CAPACITOR-LESS LDOs

Reference	Architecture	Strengths	Weakness
[7]	Fig. 2.11a	High DC PSR	• Higher power loss • Larger drop-out
[7]	Fig. 2.11b	High DC PSR	• Higher power loss • Larger drop-out • PSR BW improvement not assured
[7]	Fig. 2.11c	High DC PSR	• Area, circuit complexity and power increases
[7]	Fig. 211d	High DC PSR	• Larger drop-out • Increased power
[4]	Fig. 2.12	-27 dB worst case PSR	• Increase in area and circuit complexity • Only 5mA load current capability • Large drop-out and hence poor power efficiency

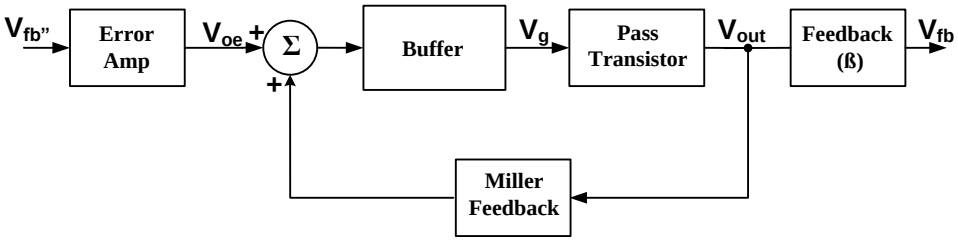
3. PROPOSED CAP-LESS LDO

3.1. Architecture

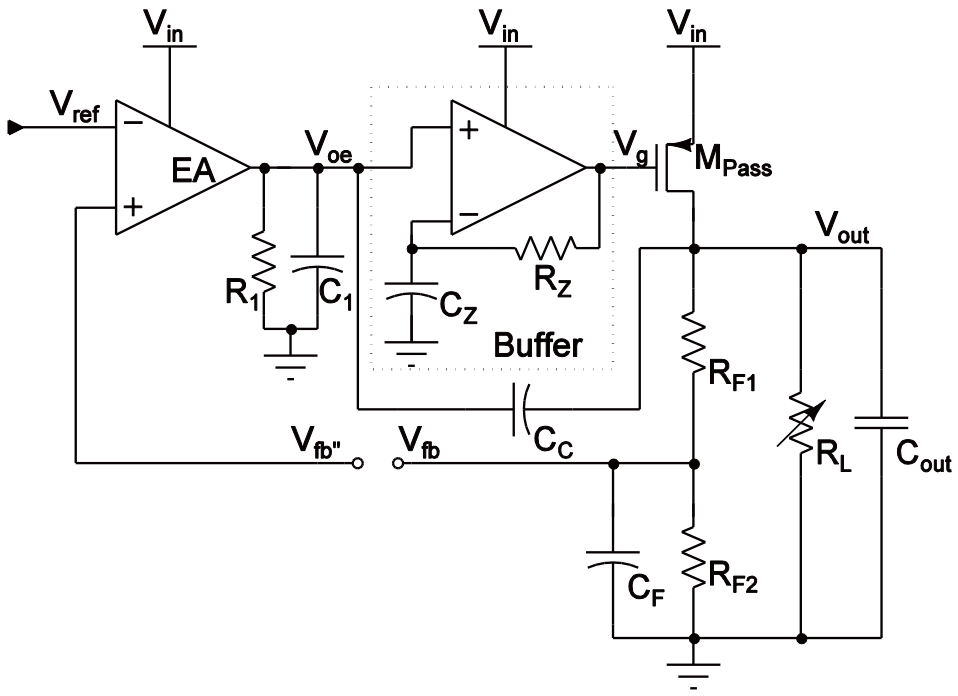
The conceptual block diagram of the proposed LDO is shown in Fig. 3.1a. The proposed LDO consists of an error amplifier, buffer and pass transistor in the forward path and in the feedback path Miller and main resistive feedback (β) are present. Fig. 3.1b shows the proposed LDO with the desired Unity Gain Buffer in between the error amplifier and the pass transistor. The transfer function for the buffer should have a single zero ideally which will create a pole effect in the PSR and compensates for the degradation due to the zero effect of the dominant pole with in the loop. The intended transfer function for the buffer is shown in the below equation.

$$\frac{V_g}{V_{oe}} = 1 + sR_ZC_Z$$

But after considering the transconductance and parasitic resistances and capacitors of each stage are included as shown in Fig. 3.2, the buffer has two poles along with the desired zero which will be discussed in detail in section 3.1.1. Miller capacitor C_C is added to create a dominant pole within the loop. Additional pole is created in the feedback loop using C_F whose purpose can be explained in the following stability analysis. g_{m1}, R_1 and C_1 are the transconductance, output resistance and output parasitic capacitance of the error amplifier respectively.



(a)



(b)

Fig. 3.1. Proposed Cap-less LDO's (a) Block Diagram (b) Architecture

Similarly g_{m2}, R_2 and C_2 corresponds to the buffer stage which is the second stage in the loop. Here C_2 is dominated by the sum of gate to source capacitance C_{gs} and miller multiplication of the gate to drain capacitance C_{gd} of the pass transistor as indicated in

(15a). g_{mP} is the transconductance of the pass transistor which acts as the third stage or output stage for the proposed LDO. The effective output resistance R_{out} of the LDO is related to (6). Assuming the pass transistor to be in saturation region, C_{gs} and C_{gd} can be expressed as shown in (15b) and (15c) where W_P, L_P, C_{OX} and C_{OV} are the width, length, gate-oxide capacitance and overlap capacitance per unit width for the pass transistor respectively.

$$C_2 \approx C_{gs} + (1 + g_{mP}R_{out})C_{gd} \tag{15a}$$

$$C_{gs} = \frac{2}{3}W_P L_P C_{OX} + W_P C_{OV} \tag{15b}$$

$$C_{gd} = W_P C_{OV} \tag{15c}$$

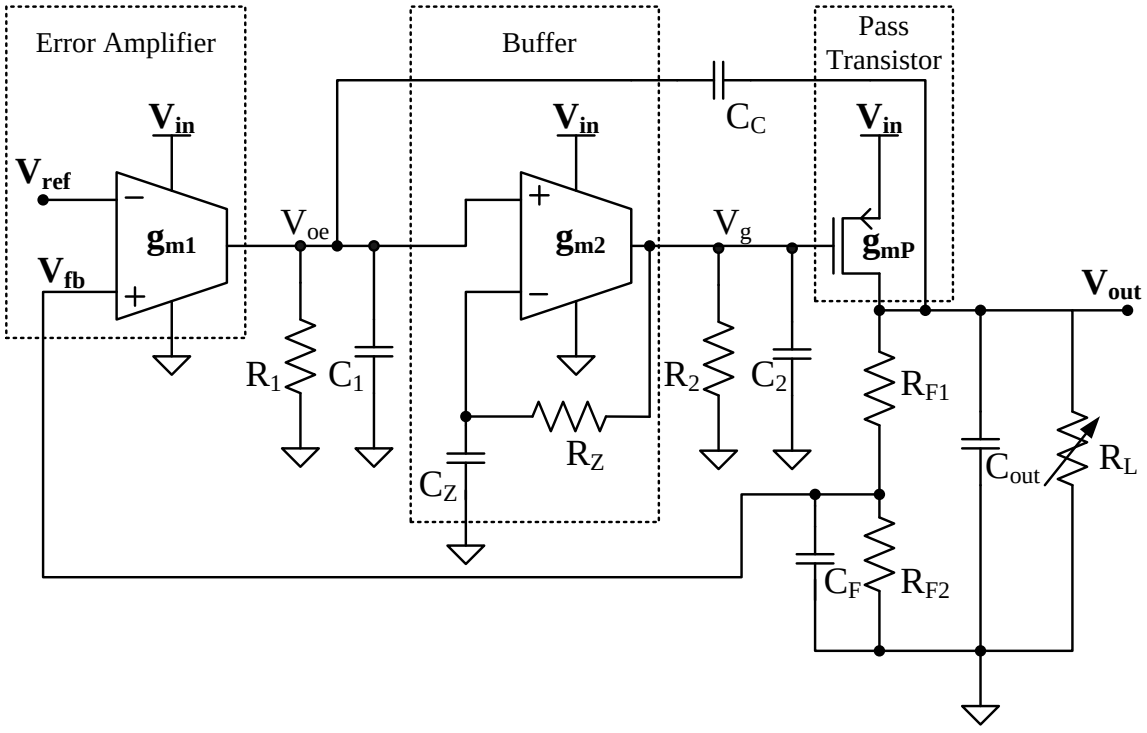


Fig. 3.2. Proposed Cap-Less LDO with Parasitics

3.1.1. Unity Gain Buffer

The buffer shown in Fig. 3.3a has resistor R_Z and capacitor C_Z which form the feedback network. The transfer function for the unity gain buffer can be indicated by (16) without making any assumptions. The transconductance g_{m2} stage should have very high input impedance, high output impedance and the parasitic pole at very high frequency.

$$\frac{V_g}{V_{oe}} = \frac{g_{m2}R_2(1 + sC_ZR_Z)}{1 + g_{m2}R_2 + s(R_ZC_Z + R_2C_2 + C_ZR_2) + s^2(R_2R_ZC_2C_Z)} \tag{16}$$

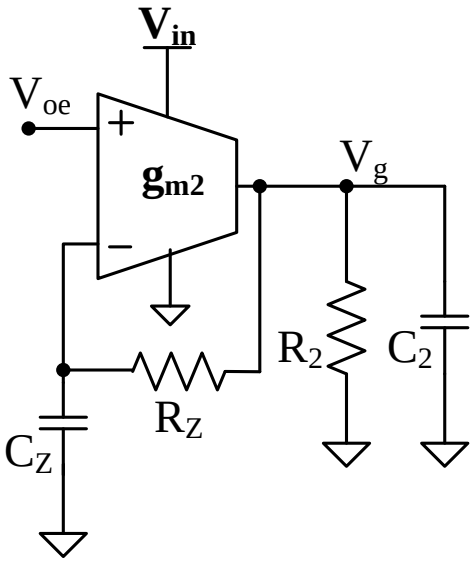
By assuming $(g_{m2}R_2) >> 1$, (16) can be simplified to transfer function shown in (17)

$$\frac{V_g}{V_{oe}} = \frac{1 + sR_ZC_Z}{1 + \frac{s}{g_{m2}}\left(C_2 + C_Z + \frac{R_ZC_Z}{R_2}\right) + \frac{s^2}{g_{m2}}(C_2C_ZR_Z)} \tag{17}$$

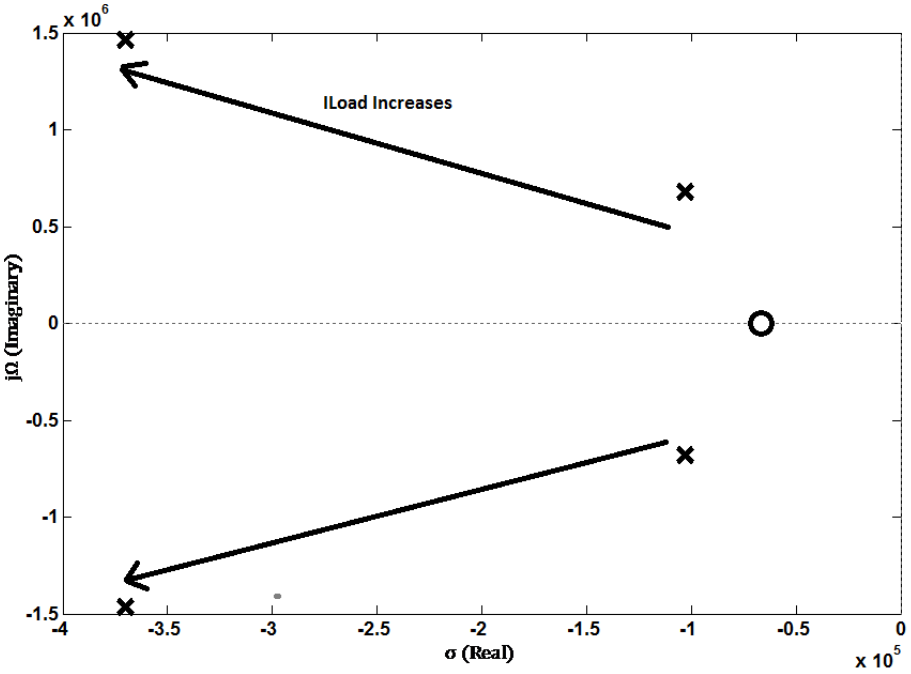
From the pole-zero plot of the buffer as shown in Fig. 3.3b and the buffer‘s transfer function indicated by (17) it is clear that the buffer has two complex poles and one zero. It is also clear that the gain of the buffer is unity from (17). Let A_1 and B_1 be the coefficients for the denominator polynomial of the transfer function of the buffer for simplification. The complex poles move to higher frequencies as load current increases because the parasitic capacitor C_2 decreases.

$$A_1 = \frac{C_2C_ZR_Z}{g_{m2}}$$

$$B_1 = \frac{1}{g_{m2}}\left(C_2 + C_Z + \frac{R_ZC_Z}{R_2}\right)$$



(a)



(b)

Fig. 3.3. Unity Gain Buffer (a) Architecture (b) Pole-Zero Map

3.1.2. Miller Feedback

The miller feedback network between the output of the LDO (V_{out}) and the output of the error amplifier (V_{oe}) depicted in Fig. 3.1b alone is shown in Fig. 3.4. Since any change in voltage difference across a capacitor results in a corresponding current through it, the miller capacitance can modeled as transconductance considering only the feedback path. The transfer function from V_{out} to V_{oe} is indicated in (18).

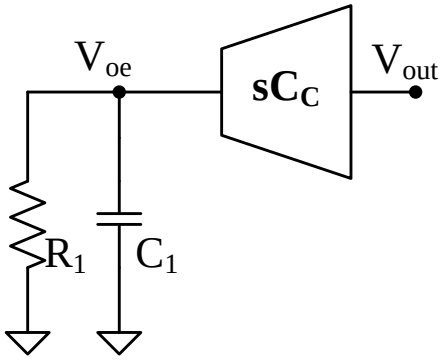


Fig. 3.4. Miller Feedback

$$\frac{V_{out}}{V_{oe}} = \frac{sC_C R_1}{1 + sR_1 C_1} \tag{18}$$

Generally C_1, the parasitic capacitance at the output of the error amplifier including the input capacitance of the buffer is smaller than the miller capacitance C_C. The feed forward path through C_C from the output of the error amplifier (V_{oe}) to the output of the LDO (V_{out}) results in a RHP zero (ω_{ZC}) whose frequency is indicated in (19).

$$\omega_{ZC} = +\frac{g_{mP}}{C_C} \tag{19}$$

The transconductance g_{mP} is related to the load current (I_{Load}) and size ($\frac{W}{L}$) by the following equation where μ is the mobility and C_{OX} is the gate-oxide capacitance of the pass transistor.

$$g_m = \sqrt{\frac{2 * I_{Load}}{\mu C_{OX}\left(\frac{W}{L}\right)_P}}$$

Since the size of the pass transistors are huge, even for a minimum load current the transconductance g_{mP} is higher and hence ω_{Zc} will be at very higher frequencies compared to the UGF of the LDO which can be related to (20). Hence ω_{Zc} can be neglected.

$$UGF_{LDO} = \frac{g_{m1}}{C_C}\,\beta \tag{20}$$

3.1.3. LDO Feedback Network

The feedback network as shown in Fig. 3.5 has the transfer function expressed in (21).

$$\beta = \frac{V_{fb}}{V_{out}} = \frac{\frac{R_{F2}}{R_{F1}+R_{F2}}}{1 + sC_F(\frac{R_{F1}R_{F2}}{R_{F1}+R_{F2}})} \tag{21}$$

In the design, let's assume $R_{F1} = R_{F2} = R_F$ which makes the feedback gain of 0.5 and so $V_{out} = \frac{V_{ref}}{2}$. With this assumption (21) can be simplified as indicated by (22).

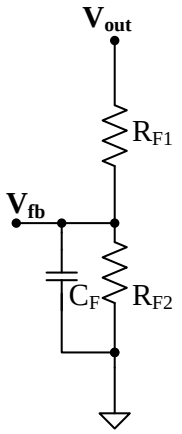


Fig. 3.5. LDO Feedback Network

$$\beta = \frac{1}{2 + sR_F C_F} \tag{22}$$

Let the pole introduced in the feedback network be ω_{P_2} which can be indicated by the following expression.

$$\omega_{P_2} = \frac{2}{R_F C_F}$$

3.2. Stability Analysis

The stability analysis can be carried for the proposed LDO by opening the loop in the main feedback at the non-inverting input of the Error Amplifier and it is shown in the Fig. 3.6 in block level. To make the analysis simpler, first consider the Miller feedback loop alone which consists of the unity gain buffer, pass transistor and the miller capacitance C_C.

The Miller feedback loop transfer function ($H_1(s)$) can be indicated using (23).

$$H_1(s) = \frac{V_{out}}{V_{oe}} = \frac{\left(\left(\frac{1 + sR_zC_z}{(1 + sB_1 + s^2A_1)}\right)\left(-\frac{g_{mp}R_{out}}{1 + sR_{out}C_{out}}\right)\right)}{\left(1 + \left(\frac{1 + sR_zC_z}{(1 + sB_1 + s^2A_1)}\right)\left(\frac{g_{mp}R_{out}}{1 + sR_{out}C_{out}}\right)\left(\frac{sC_CR_1}{1 + sR_1C_1}\right)\right)} \quad (23)$$

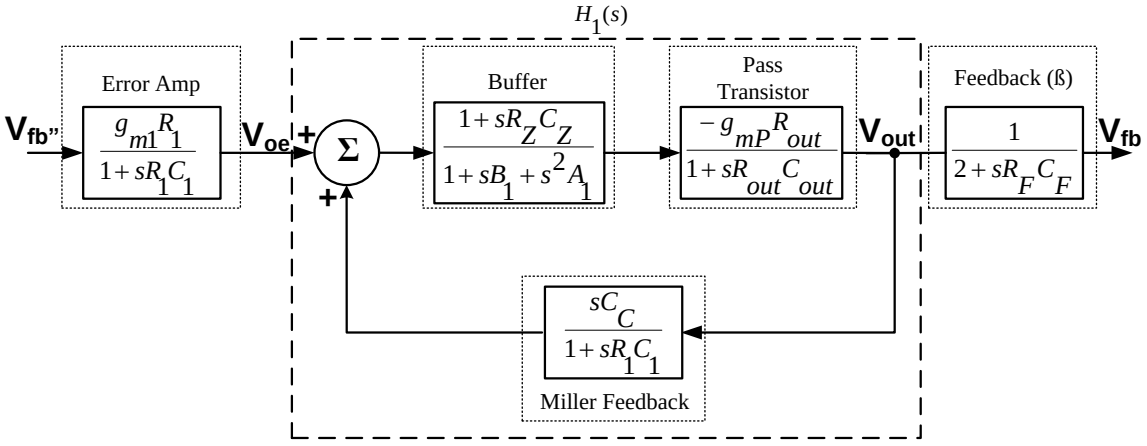


Fig. 3.6. Block Diagram of Proposed LDO

$$H_1(s) = \frac{V_{out}}{V_{oe}} = \frac{N_1(s)}{D_1(s)} \quad (24)$$

Now numerator polynomial $N_1(s)$ is given by,

$$N_1(s) = -g_{mP}R_{out}(1 + sR_zC_z)(1 + SR_1C_1) \quad (25)$$

Denominator Polynomial ($D_1(s)$)

$$D_1(s)$$

$$= \left(1 + \frac{s}{g_m}\left(C_2 + C_Z + \frac{R_ZC_Z}{R_2}\right) + \frac{s^2}{g_m}C_2C_ZR_Z\right)(1 + sR_{out}C_{out})(1 + sR_1C_1) + \quad (26)$$

$$(1 + sR_ZC_Z)g_{mP}R_{out}sC_CR_1$$

Thus $D_1(s)$ is a polynomial with degree 4.

Let's assume $D_1(s)$ in the following form for simplification,

$$D_1(s) = 1 + d_1 s + d_2 s^2 + d_3 s^3 + d_4 s^4$$

where d_n, n = 1 to 4 are the assumed coefficients of denominator polynomial $D_1(s)$.

TABLE III

DENOMINATOR $D_1(s)$ COEFFICIENTS WITHOUT SIMPLIFICATION

Coefficients	Expression
d_1	$R_1C_1 + R_{out}C_{out} + \frac{1}{g_{m2}}\left(C_2 + C_Z + \frac{R_Z C_Z}{R_2}\right) + g_{mP}R_{out}R_1C_C$
d_2	$R_1C_1R_{out}C_{out} + \frac{1}{g_{m2}}\left(C_2 + C_Z + \frac{R_Z C_Z}{R_2}\right)(R_1C_1 + R_{out}C_{out}) + \frac{1}{g_{m2}}C_2C_ZR_Z + g_{mP}R_{out}R_1C_CR_ZC_Z$
d_3	$\frac{1}{g_{m2}}\left[C_2C_ZR_Z(R_1C_1 + R_{out}C_{out}) + (C_2 + C_Z + \frac{R_Z C_Z}{R_2})R_1C_1R_{out}C_{out}\right]$
d_4	$\frac{1}{g_{m2}}(R_{out}C_{out}R_ZC_ZR_1C_1C_2)$

For all Load Currents the following assumptions can be made,

(i) $R_Z C_Z > R_{out}C_{out}$

(ii) $R_1 \gg R_Z > R_2 > R_{out}$

(iii) $C_2 > C_Z > C_C > C_1$

In the above assumptions, the maximum value of C_{out} is considered to be 100pF which is a fair assumption for a capacitor free LDO delivering 50mA of current. With these assumptions we can simplify $D_1(s)$ which is expressed in Table IV.

TABLE IV

DENOMINATOR $D_1(s)$ COEFFICIENTS WITH SIMPLIFICATION

Coefficients	Expression
d_1	$g_{mP}R_{out}R_1C_C$
d_2	$g_{mP}R_{out}R_1C_CR_ZC_Z$
d_3	$\frac{1}{g_{m2}}(C_2C_ZR_Z(R_1C_1 + R_{out}C_{out}))$
d_4	$\frac{1}{g_{m2}}(R_{out}C_{out}R_ZC_ZR_1C_1C_2)$

Now the denominator polynomial $D_1(s)$ can be expressed as shown in (27).

$$D_1(s) = 1 + sg_{mP}R_{out}R_1C_c + s^2g_{mP}R_{out}C_cR_zC_zR_1 + s^3\left(\frac{C_2C_ZR_Z(R_1C_1+R_{out}C_{out})}{g_{m2}}\right) + s^4\left(\frac{R_{out}C_{out}R_zC_zR_1C_1C_2}{g_{m2}}\right) \quad (27)$$

By taking $(1 + sg_{mP}R_{out}R_1C_C)$ in common and multiply and divide by $(1 + sR_ZC_Z)$ in (27) and at frequencies higher than $(\frac{1}{R_ZC_Z})$, $1 + sR_ZC_Z \approx sR_ZC_Z$ and $D_1(s)$ can be further modified as shown in (28).

$$D_1(s) = (1 + sg_{mP}R_{out}R_1C_c)(1 + sR_zC_z)\left(1 + s\left(\frac{C_2(R_1C_1 + R_{out}C_{out})}{g_{m2}g_{mP}R_{out}R_1C_c}\right) + s^2\left(\frac{C_{out}C_1C_2}{g_{m2}g_{mP}C_c}\right)\right) \quad (28)$$

By substituting $N_1(s)$ from (26) and $D_1(s)$ from (28) into $H_1(s)$ indicated by (24),

$$H_1(s) = \frac{V_{out}}{V_{oe}} = -\frac{g_{mp}R_{out}(1 + sR_1C_1)}{\left(1 + sg_{mp}R_{out}R_1C_c\right)\left(1 + s\left(\frac{C_2(R_1C_1 + R_{out}C_{out})}{g_{m2}g_{mP}R_{out}R_1C_c}\right) + s^2\left(\frac{C_{out}C_1C_2}{g_{m2}g_{mP}C_c}\right)\right)}$$

Now the open loop transfer function of the LDO ($H_{OL}(s)$) can be expressed as in (29)

$$H_{OL}(s) = \frac{V_{fb}}{V_{fb"}} = \left(\frac{g_{m1}R_1}{1 + sR_1C_1}\right)H_1(s)\left(\frac{1}{2 + sR_fC_f}\right) \quad (29)$$

$$H_{OL}(s) = \frac{V_{fb}}{V_{fb"}} = \frac{-g_{mp}R_{out}g_{m1}R_1}{\left[\left(1 + sg_{mp}R_{out}R_1C_c\right)\left(1 + s\left(\frac{C_2(R_1C_1 + R_{out}C_{out})}{g_{m2}g_{mP}R_{out}R_1C_c}\right) + s^2\left(\frac{C_{out}C_1C_2}{g_{m2}g_{mP}C_c}\right)\right)(2 + sR_fC_f)\right]} \quad (30)$$

At no load or minimum load condition, R_{out} will be higher in the range of few tens of Kilo ohms. Thus $R_{out}C_{out}$ cannot be neglected compared to the R_1C_1. Hence the open loop transfer function $H_{OL}(s)$ will be same as expressed in (30).

R_{out} will be in the range of few tens of ohms during the full load condition and hence $R_{out}C_{out} \ll R_1C_1$. Thus the open loop transfer function for the full load can be re-written as shown in (31).

$$H_{OL}(s) = \frac{V_{fb}}{V_{fb"}}$$

$$= -\frac{g_{mp}R_{out}g_{m1}R_1}{[(1 + sg_{mp}R_{out}R_1C_c)\left(1 + s\left(\frac{C_2C_1}{g_{m2}g_{mP}R_{out}C_c}\right) + s^2\left(\frac{C_{out}C_1C_2}{g_{m2}g_{mP}C_c}\right)\right)(2 + sR_fC_f)]} \quad (31)$$

From the open loop transfer function $H_{OL}(s)$ shown in (30) and (31), the following conclusions are clear,

(i) R_z and C_z have no effects on the loop stability

(ii) There are totally 4 poles effectively.

$$P_1 = \frac{1}{g_{mP}R_{out}R_1C_C}$$

where P_1 is the dominant pole

$$P_2 = \frac{2}{R_fC_f}$$

P_3 and P_4 form complex pole pair whose frequency ω_n is given in (32).

$$\omega_n \approx \sqrt{\frac{g_{m2}g_{mP}C_c}{C_{out}C_1C_2}} \quad (32)$$

Though R_z and C_z don't affect the loop stability, it helps to improve the PSR of the LDO which is explained in section 3.3. If the open loop transfer function $H_{OL}(s)$ is considered

without R_z and C_z in the buffer, the effect of complex pole pair will be lesser resulting in better gain margin (lower magnitude peaking). This is clear from schematic simulations shown in section 4.2.1.

3.2.1. Stability Condition

The non-dominant complex poles can be pushed to 5 to 6 times the UGF by keeping the transconductance of the buffer stage g_{m2} sufficiently high at the expense of power. The non-dominant complex poles result in magnitude peaking which will affect the gain margin GM and hence result in instability and poor transients. The pole P_2 can be placed in between the UGF and ω_n such that additional -20dB per decade can be achieved and hence the magnitude peaking can be reduced further. The condition expressed in (33a) should be satisfied for a phase margin PM > 60° and atleast a GM of 10dB in worst case. For a phase margin PM > 45°, $P_2 \geq 1.4 * \text{UGF}$. From (20) and (32), (33a) can be further written as (33b).

$$2.2 * \text{UGF}_{\text{LDO}} \leq P_2 \leq 0.6 * \omega_n \tag{33a}$$

$$2.2 * \frac{g_{m1}}{C_C}\ \beta \leq \frac{2}{R_F C_F} \leq 0.6 * \sqrt{\frac{g_{m2} g_{mP} C_c}{C_{out} C_1 C_2}} \tag{33b}$$

The dependency of ω_n on the load current variation can be explained with the relationship indicated in (34).

$$\omega_n \alpha \sqrt{\frac{g_{mP}}{C_2}} \approx \sqrt{\frac{g_{mp}}{g_{mp} R_{out} C_{gd}}} = \sqrt{\frac{1}{R_{out} C_{gd}}} \tag{34}$$

Though R_{out} for a LDO is given by (6), it can be approximated to $r_{ds,pass}$ roughly. The $r_{ds,pass}$ can be easily written as shown in (35) for saturation operation where λ is the channel length modulation factor which depends on the technology. Thus (34) can be modified to (36) which explain that complex poles move to higher frequencies when the load current is increasing. The bode plots of the $H_{OL}(s)$ shown in Fig. 3.7 for different load conditions proves the ω_n movement with load current. As expected in a capacitor less LDO, the worst case for the stability occurs for the minimum load condition.

$$r_{ds,pass} = \frac{1}{\lambda I_{Load}} \tag{35}$$

$$\omega_n \alpha \sqrt{\frac{1}{R_{out}}} = \sqrt{I_{Load}} \tag{36}$$

The pole-zeros movement with load current for the open-loop transfer function $H_{OL}(s)$ is shown in Fig. 3.8. As load current increases, the complex poles and the dominant pole move to higher frequencies as shown in Fig. 3.8a and Fig. 3.8b respectively.

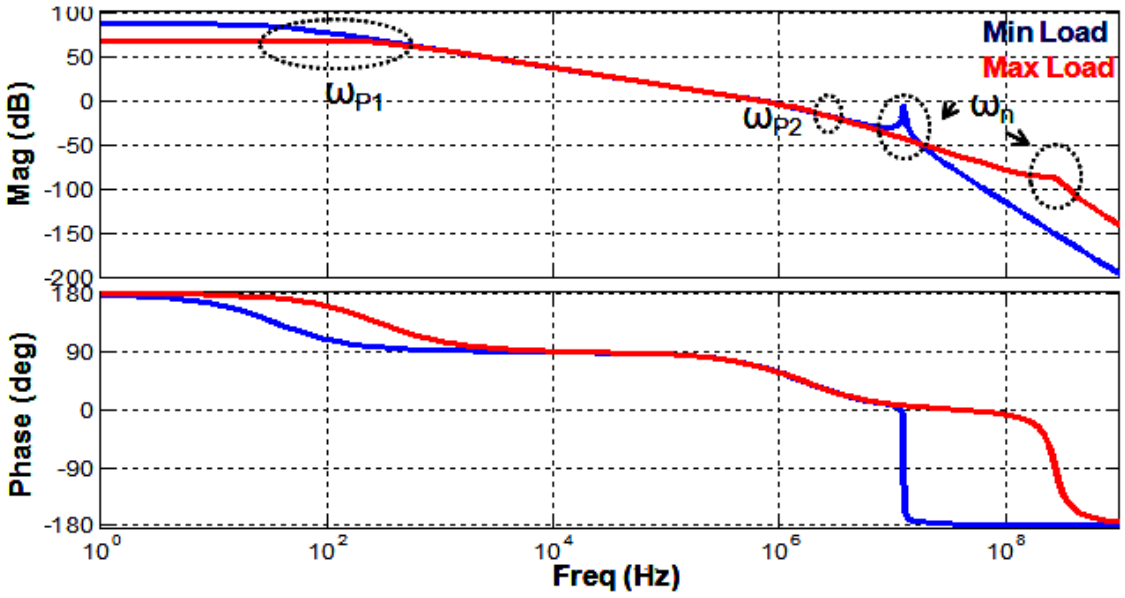
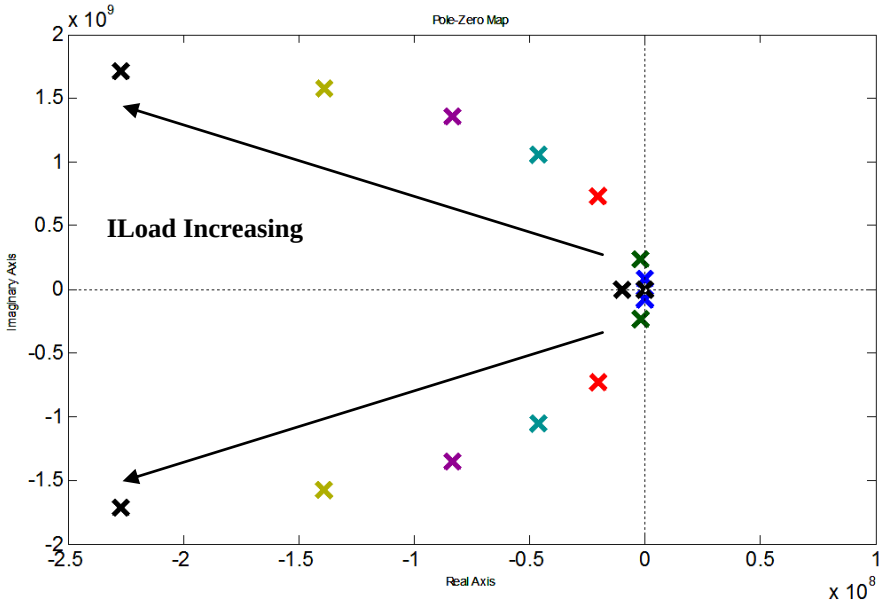
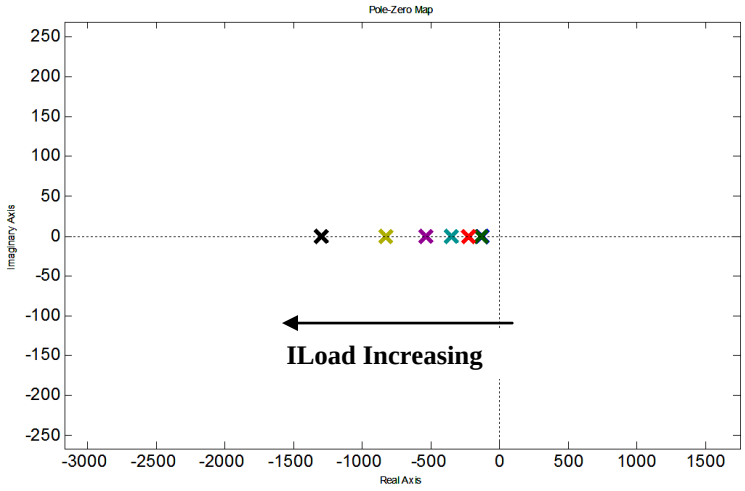


Fig. 3.7. Open Loop AC Response for $I_{LOAD,min}$ and $I_{LOAD,max}$



(a)

Fig. 3.8. Movement of (a) Complex Poles (b) Dominant Poles with I_{LOAD}



(b)

Fig. 3.8. Continued

3.3. PSR Analysis

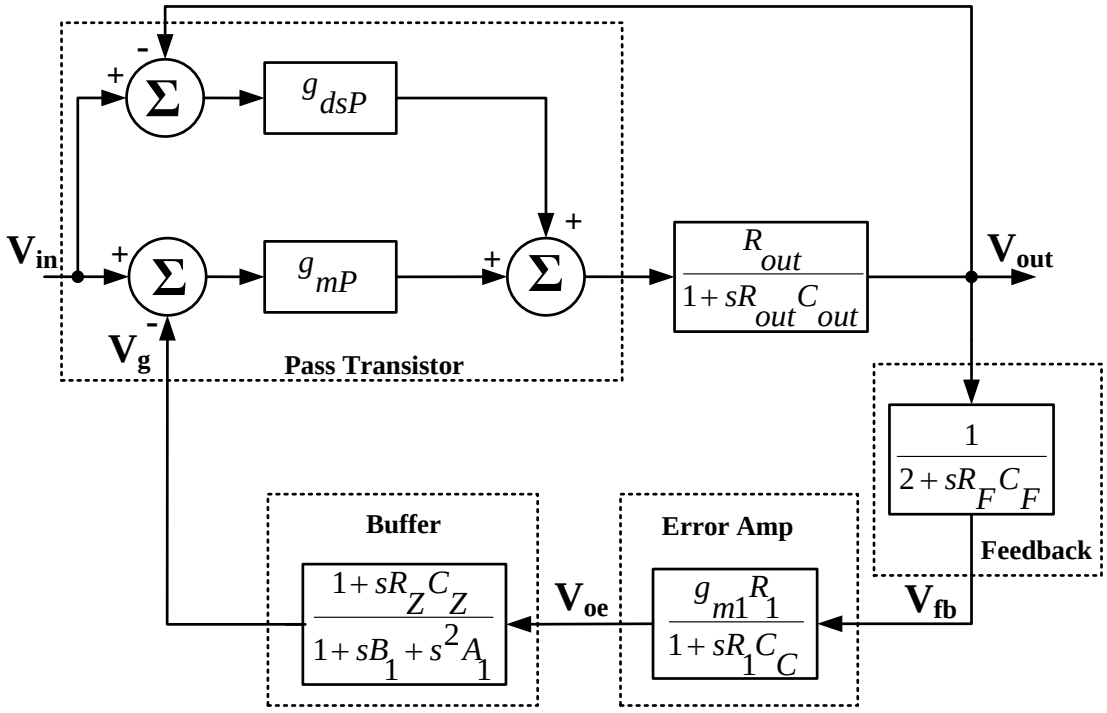


Fig. 3.9. PSR Modeling for the Proposed LDO

The PSR modeling for the proposed LDO is shown in Fig. 3.9. It is assumed in the model that the only path for the noise from supply V_{in} is through the pass transistor. g_{dsP} is also modeled to account its effect on the PSR. So from the previous discussion in section 2.4 about [6], to make the model valid PMOS error amplifier with NMOS diode connection need to be used in the design. Since the buffer is already in feedback by itself, its PSR is shaped and will have the DC gain as the inverse of the open-loop gain of the buffer ($g_{m2}R_2$). So the PSR of the buffer can be neglected assuming the open loop gain bandwidth of the buffer ($\frac{g_{m2}}{C_2}$) satisfies the condition indicated in (37a). UGF_{LDO} is the open loop unity gain frequency of the LDO. The condition (37b) need to be satisfied to improve the PSR and this determines the values of required R_Z and C_Z which will be clear at the end of the section 3.3.

$$\frac{g_{m2}}{C_2} > UGF_{LDO} = \frac{g_{m1}}{C_C}\beta \tag{37a}$$

$$P_1 \leq \left(\frac{1}{R_Z C_Z}\right) \leq UGF_{LDO} \tag{37b}$$

From (37a) and (32), increasing the g_{m2} helps both stability and makes the PSR of the buffer be neglected for sufficient high frequencies. But increasing g_{m2} means burning more power in the buffer stage because in general the transconductance $g_m$is related to the drain-source current I_{DS} by (38) where μ is the mobility, C_{OX} is the gate-oxide capacitance, W is the width and L is the length of the transistor.

$$g_m = \sqrt{\frac{2 * I_{DS}}{\mu C_{OX}\left(\frac{W}{L}\right)}} \tag{38}$$

3.3.1. Error Amplifier Transfer Function for PSR

From [6] it is also clear that if high PSR error amplifier is used for a simple miller compensated capacitor less LDO as shown in Fig. 3.10, the BW of the PSR is increased by the gain of the pass transistor ($g_{mP}R_{out}$). This means in the PSR transfer function, the zero which makes the PSR to degrade will be at frequency ($\frac{1}{R_1 C_C}$) instead of ($\frac{1}{R_1 g_{mP} R_{out} C_C}$).

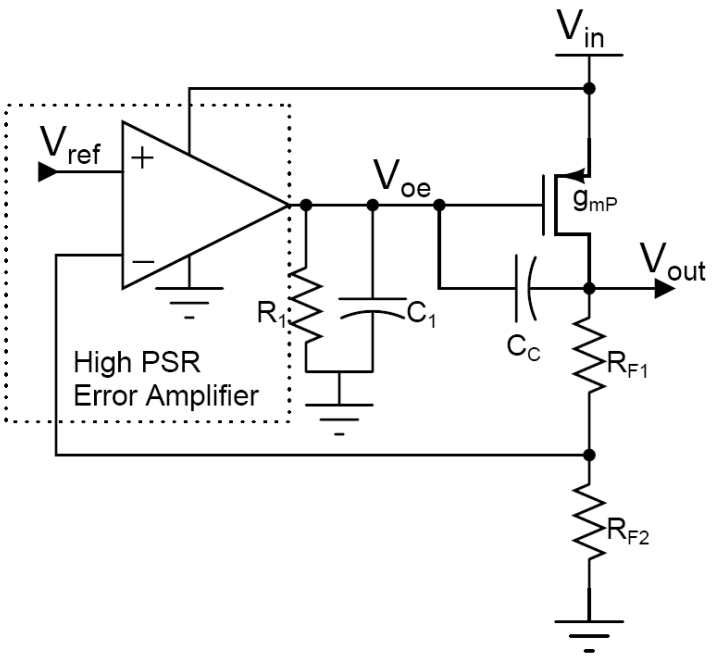


Fig. 3.10. Simple LDO with Miller Compensation

It can also be explained intuitively why the miller effect is not seen if a high PSR error amplifier is used using Fig. 3.11.

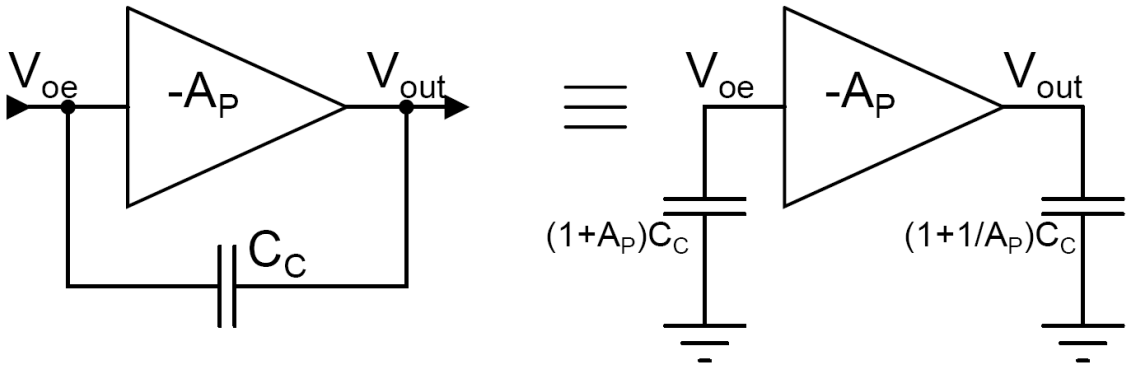


Fig. 3.11. Miller Multiplication

From Fig. 3.11 it is clear that the capacitance at the input node V_{oe} is multiplied by the gain $A_P = \frac{V_{out}}{V_{oe}}$. For PSR the input is considered to be the noise in supply V_{in} and if high PSR error amplifier is used, then it rejects most of the noise and so in that case no input V_{oe} to the pass transistor stage. If there is no input, there is no gain A_P which can be defined and hence the effective capacitance at the V_{oe} node is just C_C instead of $(1 + A_P)C_C$. This discussion can be easily extended to the proposed LDO for PSR modeling shown in Fig. 3.9 and thus the high PSR error amplifier is modeled with a pole indicated by (39) which doesn't show the miller effect.

$$P_{oe} = \frac{1}{1 + sR_1C_C} \tag{39}$$

3.3.2. PSR of Proposed LDO

On solving the transfer function from V_{in} to V_{out} the required PSR can be derived as expressed in (40) using Mason's rule.

$$\frac{V_{out}}{V_{in}} = \frac{\left(\frac{R_{out}(g_{mP}+g_{dsP})}{1+sR_{out}C_{out}}\right)}{1+\frac{R_{out}}{1+sR_{out}C_{out}}\left[g_{dsP}+\frac{g_{mP}g_{m1}R_1(1+sR_ZC_Z)}{(2+sR_FC_F)(1+sR_1C_C)\left(1+\frac{s}{g_{m2}}\left(C_2+C_Z+\frac{R_ZC_Z}{R_2}\right)+\frac{s^2}{g_{m2}}C_2C_ZR_Z\right)}\right]} \quad (40)$$

Let us represent (40) in the form shown in (41) for simplification.

$$\frac{V_{out}}{V_{in}} = \frac{N_2(s)}{D_2(s)} \quad (41)$$

With the assumption $C_2 > C_Z$ for all load currents the numerator polynomial $N_2(s)$ can be expressed as indicated in (42).

$$N_2(s) = R_{out}(g_{mP}+g_{dsP})(1+sR_1C_C)(2+sR_FC_F)\left(1+\frac{s}{g_{m2}}\left(C_2+\frac{R_ZC_Z}{R_2}\right)+\frac{s^2}{g_{m2}}C_2C_ZR_Z\right) \quad (42)$$

For the minimum load current the parasitic capacitance C_2 at the gate of the pass transistor is very large since the gain of the pass transistor is high and $g_{dsP} \ll g_{mP}$. Hence $N_2(s)$ for minimum load current can be modified as shown in (43). For maximum load condition $N_2(s)$ is still same as shown in (42).

$$N_2(s) = g_{mP}R_{out}(1+sR_1C_C)(2+sR_FC_F)\left(1+\frac{s}{g_{m2}}C_2+\frac{s^2}{g_{m2}}C_2C_ZR_Z\right) \quad (43)$$

The denominator polynomial $D_2(s)$ is represented in (44) without simplification

$$
\begin{aligned}
&D_2(s)\\
&= (1 + R_{out}g_{dsP} + sR_{out}C_{out})(2 + sR_FC_F)(1 + sR_1C_C)\\
&\left(1 + \frac{s}{g_{m2}}\left(C_2 + \frac{R_ZC_Z}{R_2}\right) + \frac{s^2}{g_{m2}}C_2C_ZR_Z\right) + g_{mP}g_{m1}R_1R_{out}(1 + sR_ZC_Z)
\end{aligned}
\tag{44}
$$

With the assumptions $R_1C_C \gg (R_{out}C_{out}, R_FC_F)$, $C_2 > C_Z > C_C$ and $R_1 \gg R_Z > R_2 > R_{out}$ for all the loading conditions $D_2(s)$ can be simplified as shown in (45)

$$
\begin{aligned}
&D_2(s)\\
&= g_{mP}g_{m1}R_1R_{out} + sg_{mp}g_{m1}R_1R_{out}R_ZC_Z\\
&+s^2\left[R_1C_C\left(2R_{out}C_{out} + (1 + R_{out}g_{dsP})\left(R_FC_F + \frac{R_ZC_Z}{g_{m2}R_2} + \frac{C_2}{g_{m2}}\right)\right)\right]\\
&+\frac{s^3}{g_{m2}}[2R_1C_C(1 + R_{out}g_{dsP})C_2C_ZR_Z]\\
&+\frac{s^4}{g_{m2}}[R_1C_CC_2C_ZR_Z(2R_{out}C_{out} + (1 + R_{out}g_{ds})R_FC_F)]\\
&+\frac{s^5}{g_{m2}}R_{out}C_{out}R_FC_FR_1C_CC_2R_ZC_Z
\end{aligned}
\tag{45}
$$

Assuming $g_{dsP} = \frac{1}{r_{dsP}}$ dominates in the output resistance R_{out} denoted by (6) for all load currents. Then $R_{out}g_{dsP} \approx 1$ and hence $D_2(s)$ can be simplified further as shown in (46).

$$D_2(s) = (1 + sR_ZC_Z)\Bigg(g_{mP}g_{m1}R_1R_{out} + \frac{2s}{g_{m2}}\left[\frac{R_1C_C}{R_ZC_Z}\left(g_{m2}R_{out}C_{out} + g_{m2}R_FC_F + \frac{R_ZC_Z}{R_2} + C_2\right)\right] + \frac{4s^2}{g_{m2}}R_1C_CC_2 + \frac{2s^3}{g_{m2}}[R_1C_CC_2(R_{out}C_{out} + R_FC_F)] + \frac{2s^4}{g_{m2}}R_{out}C_{out}R_FC_FR_1C_CC_2\Bigg) \quad (46)$$

By taking $g_{mP}g_{m1}R_1R_{out}$ in common (46) can be modified to (47).

$$D_2(s) = g_{mP}g_{m1}R_1R_{out}(1 + sR_ZC_Z)\Bigg(1 + \frac{2s}{g_{m2}g_{mP}g_{m1}R_{out}}\left[\frac{C_C}{R_ZC_Z}\left(g_{m2}R_{out}C_{out} + g_{m2}R_FC_F + \frac{R_ZC_Z}{R_2} + C_2\right)\right] + \frac{4s^2}{g_{m2}g_{mP}g_{m1}R_{out}}C_CC_2 + \frac{2s^3}{g_{m2}g_{mP}g_{m1}R_{out}}[C_CC_2(R_{out}C_{out} + R_FC_F)] + \frac{2s^4}{g_{m2}g_{mP}g_{m1}}C_{out}R_FC_FC_CC_2\Bigg) \quad (47)$$

Let's analyze $D_2(s)$ expressed in (47) for different load conditions. Let the maximum value for the C_{out} be 100pF. Even if no output capacitance C_{out} is added, still there will be parasitic drain to bulk (C_{dbP}) and drain to gate (C_{gdP}) capacitance of the pass transistor which will be in the order of few pFs depending on the technology. Thus

C_{out} can be related to (48) in which 0 to 100pF is the explicitly added capacitance contribution.

$$C_{out} = C_{dbP} + C_{gdP} + (0 \text{ to } 100\text{pF}) \tag{48}$$

For minimum load current condition $D_2(s)$ will have the same expression as shown in (47). When maximum load current is flowing through the pass transistor, R_{out} is in ohms range and C_2 will be smaller and hence $C_2 < \frac{R_Z}{R_2} C_Z$ can be assumed. The denominator polynomial $D_2(s)$ for full load condition can be represented using (49).

$$\begin{aligned} D_2(s) = g_{mP} g_{m1} R_1 R_{out} (1 + sR_Z C_Z) \Bigg(1 \\ + \frac{2s}{g_{m2} g_{mP} g_{m1} R_{out}} \left[\frac{C_C}{R_Z C_Z} \left(g_{m2} R_F C_F + \frac{R_Z C_Z}{R_2} \right) \right] \\ + \frac{4s^2}{g_{m2} g_{mP} g_{m1} R_{out}} C_C C_2 + \frac{2s^3}{g_{m2} g_{mP} g_{m1} R_{out}} [C_C C_2 R_F C_F] \\ + \frac{2s^4}{g_{m2} g_{mP} g_{m1}} C_{out} R_F C_F C_C C_2 \Bigg) \end{aligned} \tag{49}$$

From (47) or (49) and (42) or (43) it is clear that the PSR for the proposed LDO constitutes five poles and four zeros. By using Matlab and plotting the location of the poles and zeros as shown in Fig. 3.12, it is also clear that four poles and two zeros are complex for all loading conditions. Considering only the poles and zeros within the open-loop UGF of the proposed LDO for further simplification, all the complex poles and the zero ($\frac{2}{R_F C_F}$) can be neglected. Hence PSR of the proposed LDO for minimum load can be given by (50) and for maximum load by (51) which are valid till the UGF_{LDO}

of the regulator after which the loop dies. Simulink simulations for the PSR model shown in Fig. 3.9 are illustrated in Fig. 3.13 for different load conditions.

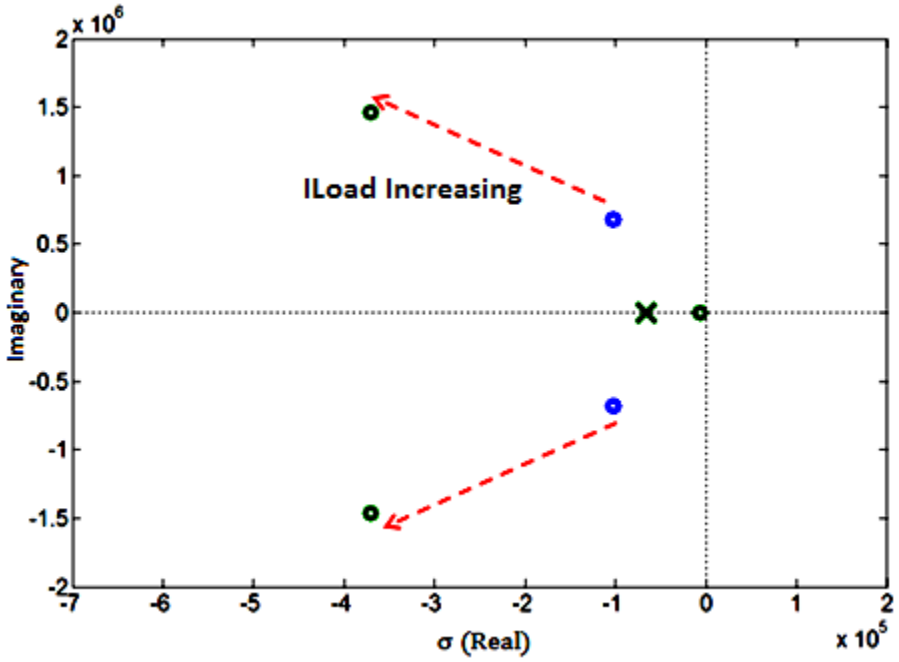


Fig. 3.12. Pole-Zero Map for $I_{LOAD,min}$ and $I_{LOAD,max}$

$$\frac{V_{out}}{V_{in}} = \frac{(1+sR_1C_C)\left(1+\frac{s}{g_{m2}}C_2+\frac{s^2}{g_{m2}}C_2C_ZR_Z\right)}{g_{m1}R_1(1+sR_ZC_Z)} \tag{50}$$

$$\frac{V_{out}}{V_{in}} = \frac{(g_{mP}+g_{dsP})(1+sR_1C_C)\left(1+\frac{s}{g_{m2}}\left(C_2+\frac{R_ZC_Z}{R_2}\right)+\frac{s^2}{g_{m2}}C_2C_ZR_Z\right)}{g_{mP}g_{m1}R_1(1+sR_ZC_Z)} \tag{51}$$

So within the UGF_{LDO} there is a pole at the frequency $(\frac{1}{R_ZC_Z})$, a zero at the frequency $\left(\frac{1}{R_1C_C}\right)$ and a complex zero pair. By applying the approximation $\frac{g_{dsP}}{g_{mP}} << 1$ to (51), the DC gain of the PSR is the inverse of the error amplifier gain $(g_{m1}R_1)$ for all load

conditions. The importance of R_Z and C_Z is clear from the PSR expressions and Simulink plots shown in Fig. 3.13. The pole effect created by R_Z and C_Z helps to nullify the effect of zero created by R_1 and C_C. Adding to this the complex zero pair will result in a magnitude dip. In a conventional capacitor free LDO, within the UGF there will be only a zero created by the dominant pole. Thus the proposed topology introduces a zero within the loop which doesn't affect the stability at all but improves the PSR till frequencies closer to the UGF_{LDO}. The pole created by R_Z and C_Z together with complex zeros play an effective role in improving PSR.

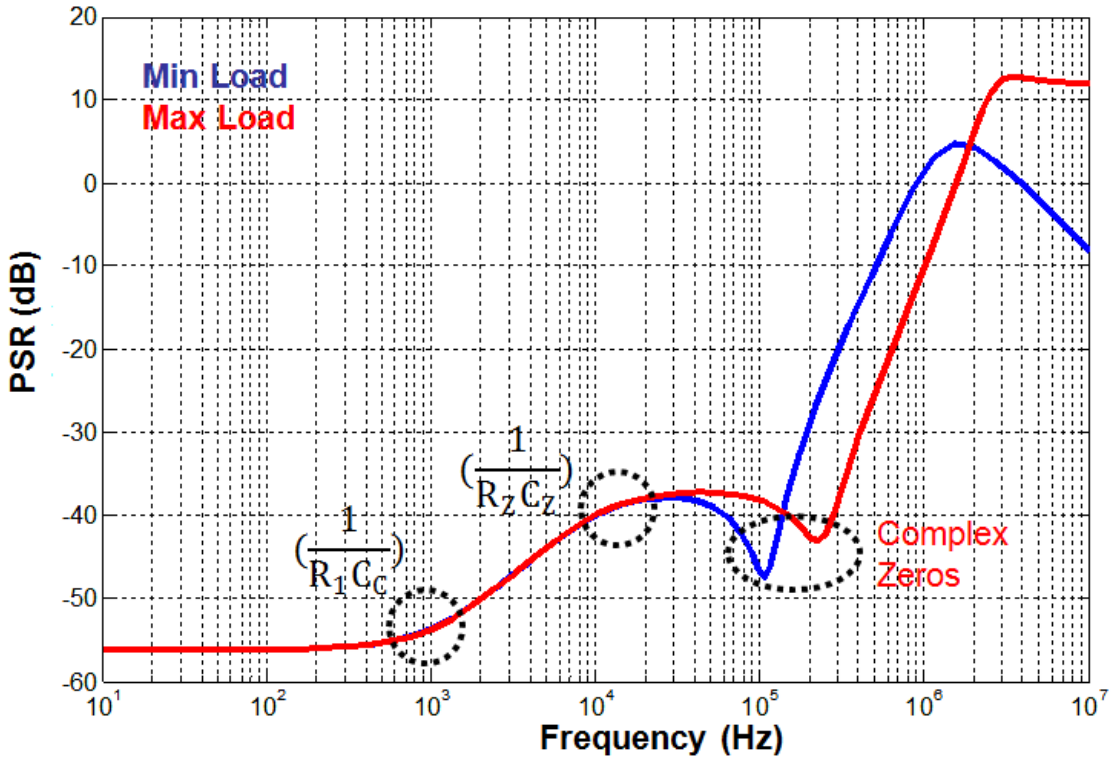


Fig. 3.13. PSR for Different I_{LOAD}

4. TRANSISTOR LEVEL DESIGN AND SIMULATION (0.5µm)

4.1. Transistor Level Design

The transistor level implementation of the proposed cap-less LDO using ON-Semi 0.5µm CMOS technology is shown in Fig. 4.1. The main specification for which the proposed LDO is designed is listed in Table V. Transistors M_1, M_{3-6} and M_9 forms the folded cascode error amplifier. Folded cascode architecture is chosen to achieve as much DC gain as possible from a single stage error amplifier. The transconductance of transistors M_1 defines the effective transconductance g_{m1} of the error amplifier. The buffer is designed using a simple differential pair formed by transistors M_2 and M_{7-8} .

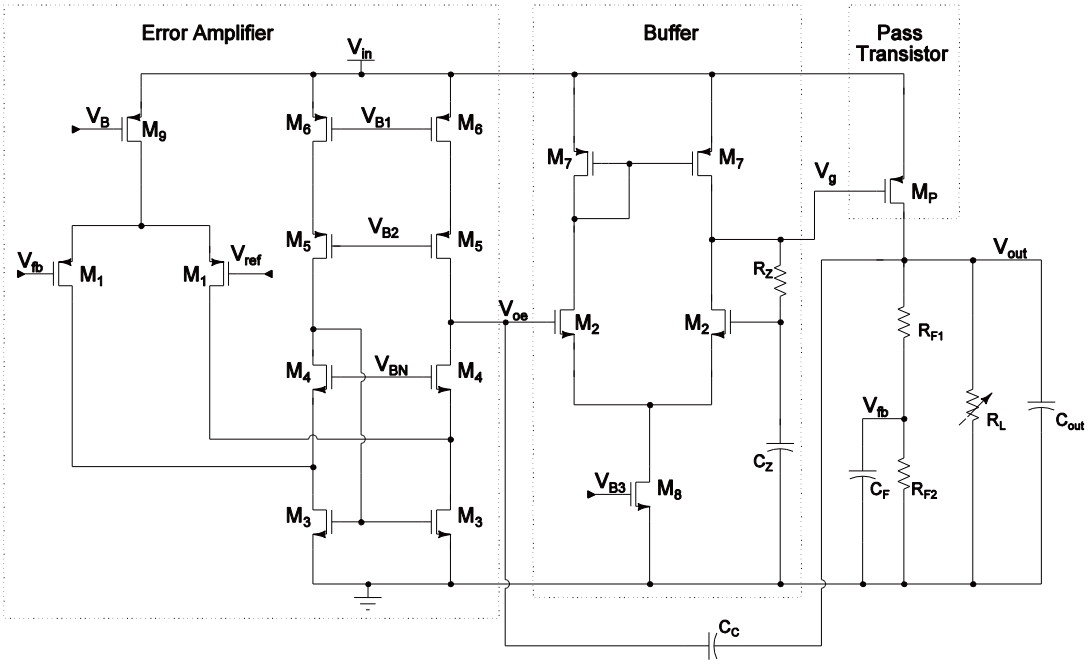


Fig. 4.1. Proposed Cap-less LDO Transistor Level Design in (0.5µm)

TABLE V

PROPOSED LDO MAIN SPECIFICATIONS (0.5µm)

PARAMETER	VALUE
V_{in} (V)	≥3.1
V_{out} (V)	2.8
$I_{LOAD,min}$ (µA)	100
$I_{LOAD,max}$ (mA)	50
C_{out} (pF)	0 – 100

The effective transconductance g_{m2} of the buffer is given by the transconductance of the transistors M_2. Transistor M_P indicates the pass transistor for the proposed LDO and its size is determined using (52). $V_{DO}$is the drop-out voltage defined by (53). Length is kept at its minimum value of 0.6µm available in this technology. μ_P and C_{OX} are the mobility and gate oxide capacitance of the PMOS respectively which can be found in the associated technology files. The transconductance g_{mP} corresponds to the transistor M_P. The biasing circuitry for the proposed LDO is shown in Fig. 4.2. The resistor R_B is externally connected resistance to generate the bias current for the LDO.

$$\left(\frac{W}{L}\right)_{Pass} = \frac{(V_{DO})^2 * \mu_P * C_{OX}}{2 * I_{LOAD,max}} \tag{52}$$

$$V_{DO} = V_{in,min} - V_{out} = 300mV \tag{53}$$

TABLE VI

DESIGN PROCEDURE

PARAMETER	DESIGN EQUATION	DESIGN SPECS
Pass Transistor	52	$V_{DO}, I_{LOAD,max}$
g_{m1}, R_1	20	DC Gain , UGF_{LDO}
C_C	20	UGF_{LDO}
C_F	33b	PM, GM
g_{m2}	33b	ω_n, PM, GM
R_Z, C_Z	37b	PSR

4.1.1. Step by Step Design Procedure

Step 1. The design of the LDO starts with the pass transistor. Using (52) and assuming V_{DO} = 300mV and maximum load current as 50mA, the size of the pass transistors are determined.

Step 2. Next the error amplifier stage is designed such that the DC gain ($g_{m1}R_1$) is greater than 60 dB. So from the DC gain of the amplifier, transconductance g_{m1} can be determined using generalized (38).

Step 3. This g_{m1} also helps to find the required C_C from (20) assuming the UGF_{LDO} as 800 kHz.

Step 4. From the determined C_C, condition indicated by (33b) is used to fix the capacitance C_F.

Step 5. Then g_{m2} of the buffer is calculated using condition (33b). Assuming a maximum current of 100μA through the buffer, the sizes of the transistors can be found using (38).

Step 6. Finally the R_Z and C_Z values can be found by using (37b) which will help to nullify the effect of the dominant pole P_1 on the PSR.

The design procedure for the proposed LDO is illustrated in Table VI. The biasing circuit showed in Fig. 4.2 is started with the assumption of reference bias current of about 2.5μA through the external resistor R_B. And this current is mirrored with 1:1 ratio through transistor M_{10} which results in 2.5μA bias current in all the transistors in the biasing circuit. The transistors are sized such that they operate in deep saturation. For robustness the operating conditions for each transistor are checked such that the minimum V_{dsat} is above 100mV, difference between V_{ds} and V_{dsat} is above 100mV and difference between V_{gs} and V_{th} is above 30mV. V_{dsat} is the drain-source saturation voltage and V_{th} is the threshold voltage for the transistor. The final circuit parameters are given in Table VII and Table VIII.

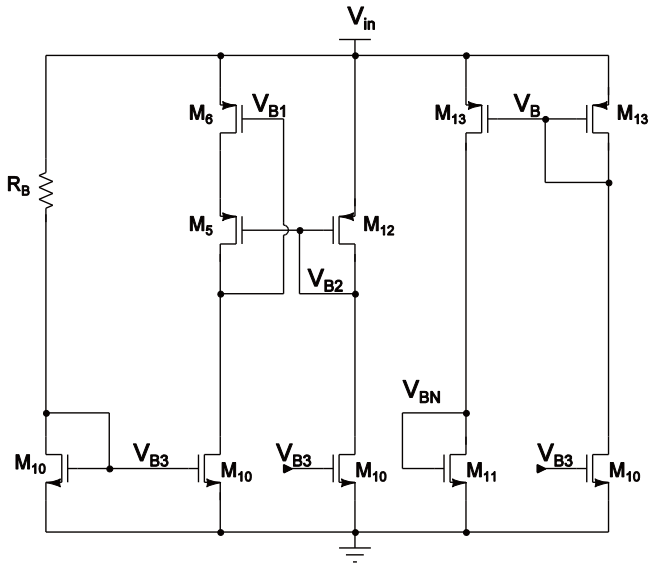


Fig. 4.2. Biasing Circuit for the Proposed LDO (0.5μm)

TABLE VII

FINAL ACTIVE CIRCUIT PARAMETERS (0.5µm)

TRANSISTOR	W(µm)	L(µm)	I_D(µA)
M_1	12	1.2	2.5
M_2	48	0.6	50
M_3	24	2.7	5
M_4	12	2.7	2.5
M_5	19.8	2.4	2.5
M_6	10.8	2.4	2.5
M_7	80.4	0.6	50
M_8	432	3.0	100
M_9	21.6	3.0	5
M_{10}	10.8	3.0	2.5
M_{11}	2.7	7.0	2.5
M_{12}	2.7	3.0	2.5
M_{13}	10.8	3.0	2.5
M_P	14400	0.6	14

TABLE VIII

FINAL PASSIVE CIRCUIT PARAMETERS (0.5µm)

PARAMETER	VALUE
C_C	3.46pF
C_F	1.4pF
C_Z	16.8pF
R_Z	900kΩ
R_{F1}, R_{F2}	100kΩ

4.2. Schematic Simulations

Spectre simulator is used in Cadence to simulate the designed capacitor-less LDO. Different LDO parameters require different kind of simulations which are presented in this section. The simulations are divided into open loop AC response which shows the frequency domain analysis of stability, steady-state line and load regulations,

load and line transients which shows the time domain analysis of stability, PSR and noise of the LDO.

4.2.1. Open Loop AC Response

The open loop AC response is shown in Fig. 4.3 for minimum and maximum load currents with no output capacitance connected externally and Fig. 4.4 shows the open-loop AC response with 100pF connected at the output. As expected from (36) and (32), the magnitude peaking occur at lower frequencies for minimum load current and is worse for C_{out}= 100pF compared to no external capacitor condition. The open-loop AC response for the worst case 100μA load current is shown in Fig. 4.5 for varying output capacitances to show the movement of ω_n. These AC simulations also prove that the LDO behaves like a single pole and no zero effect due to R_Z and C_Z within the UGF which is around 800 kHz for the designed LDO.

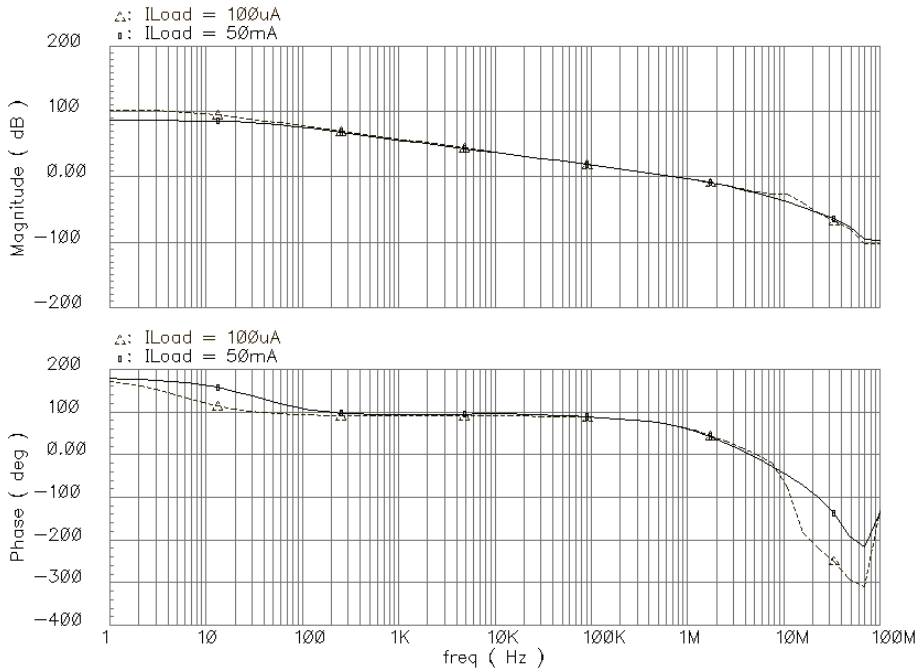


Fig. 4.3. Transistor Level Open-Loop AC Response with no C_{out}

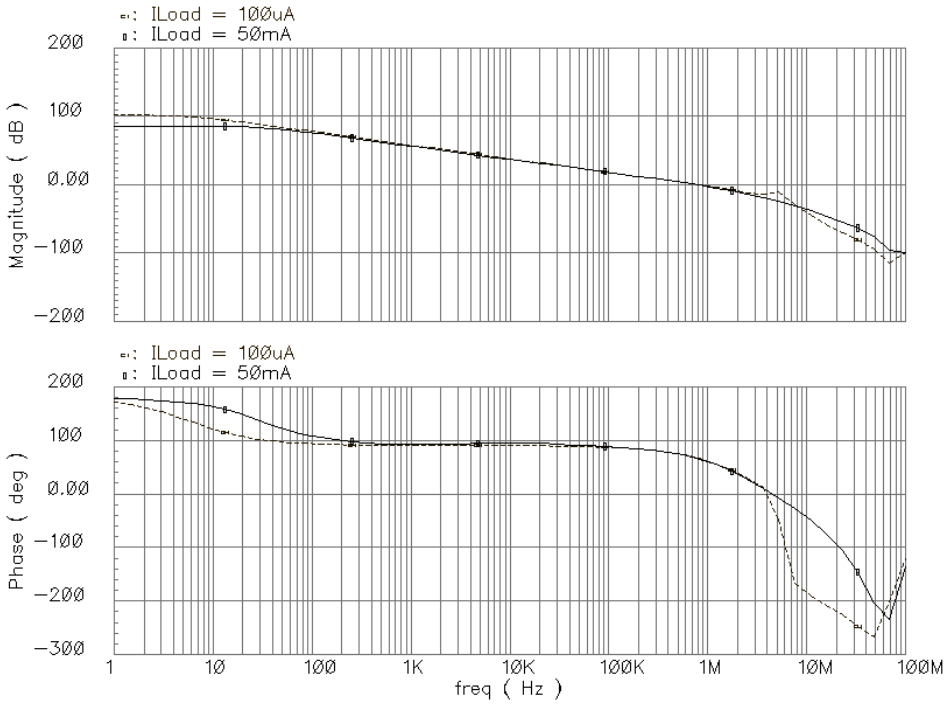


Fig. 4.4. Transistor Level Open-Loop AC Response with C_{out}= 100pF

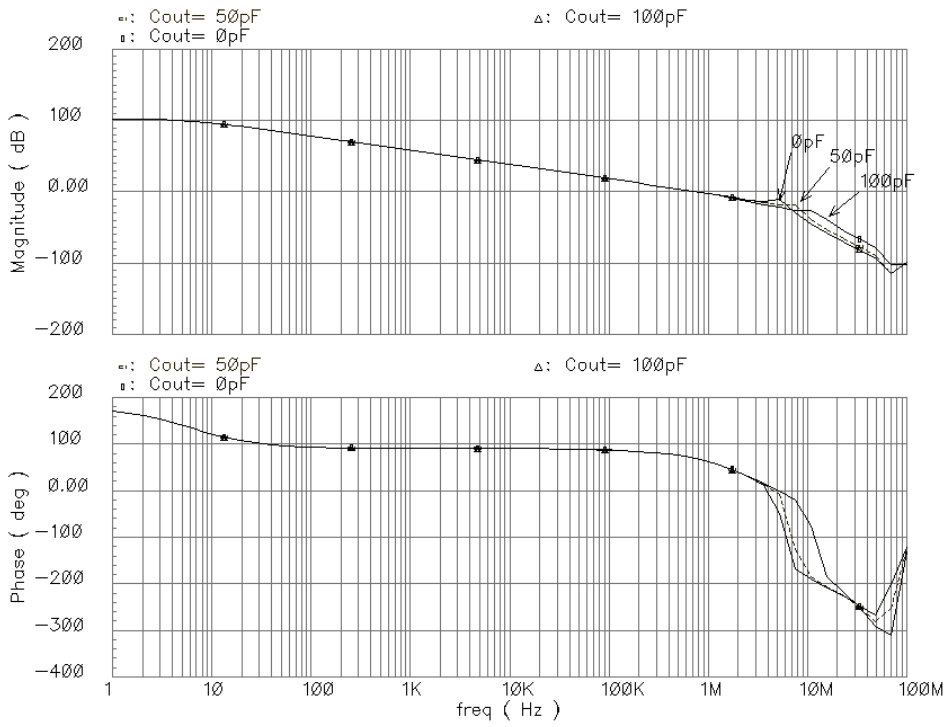


Fig. 4.5. Open-Loop AC Response for $I_{Load} = 100\mu A$ with varying C_{out}

From Fig. 4.5 and (32), C_{out}= 100pF is the worst case scenario for stability and so for all stability analysis simulations let's consider 100pF output capacitance. It is also important to look the open-loop AC response and hence check the stability for different load conditions starting from 100µA to 50mA. The DC gain, UGF, PM, GM and GMF for different load conditions with $C_{out} = 100pF$ are shown in Fig. 4.6. The minimum DC gain achieved is 86dB which is more than sufficient to achieve a better line and load regulation.

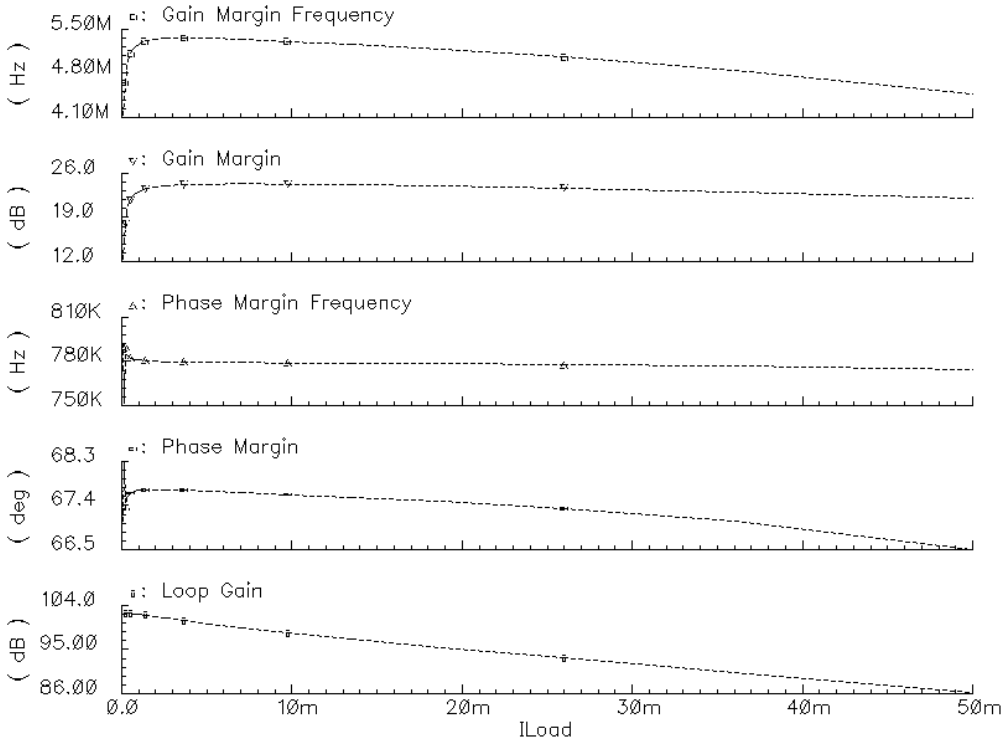
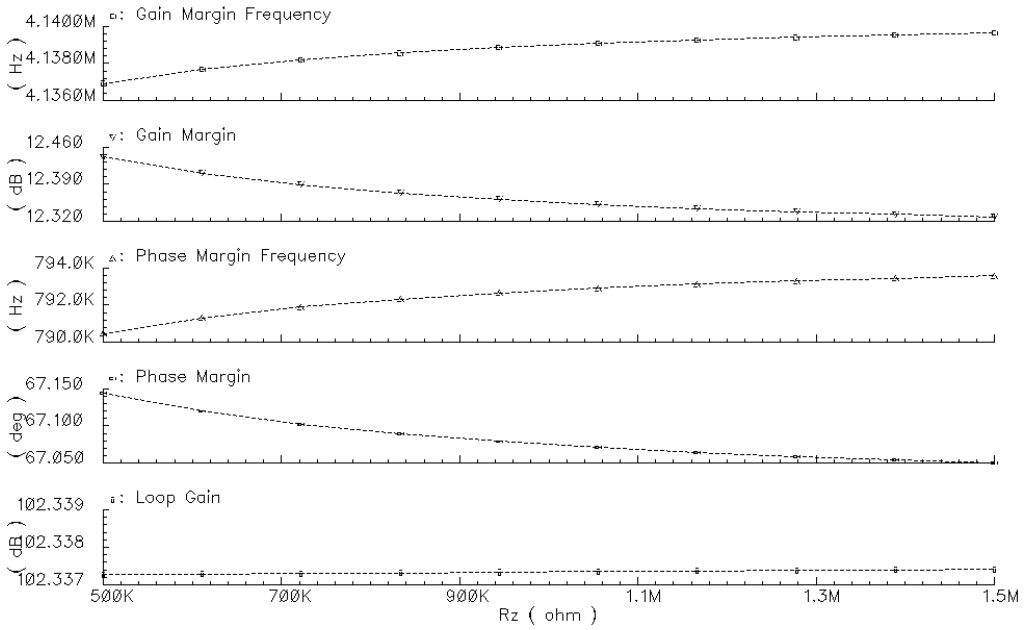
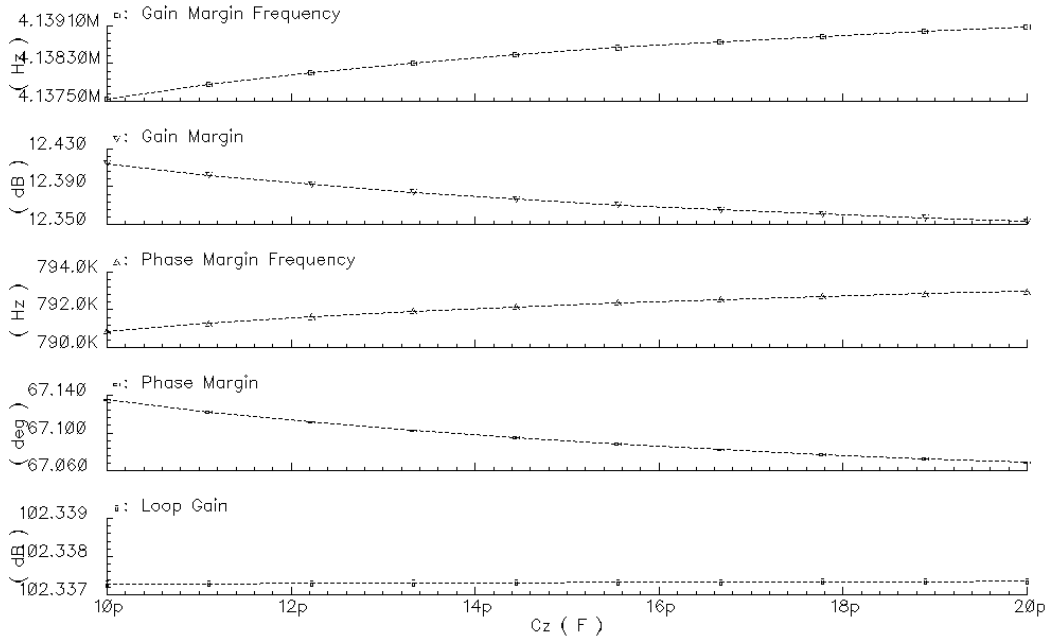


Fig. 4.6. AC Response Parameters for Different I_{Load} with C_{out} = 100pF

The designed LDO is very stable with a minimum phase margin of 66° at UGF of around 780KHz and minimum GM of 12dB. The UGF is shown as Phase Margin Frequency in Fig. 4.6. R_Z and C_Z which don't affect the stability is clear from the simulations shown in Fig. 4.7a (C_Z = 16.8pF) and Fig. 4.7b (R_Z = 900kΩ) where R_Z and C_Z are swept respectively and AC response stability parameters are plotted for worst case I_{Load} of 100μA.



(a)



(b)

Fig. 4.7. Stability Parameters for Varying (a) R_Z (b) C_Z

To complete the ineffectiveness of R_Z and C_Z on stability, open-loop AC response without R_Z and C_Z but still the buffer with unity feedback is compared with the actual AC response as shown in Fig. 4.8. The magnitude response corresponding to the no R_Z and C_Z case doesn't has the magnitude peaking for the minimum load current compared to the proposed LDO. Since a minimum GM of 10dB is maintained for the proposed LDO, the magnitude peaking shouldn't be a problem.

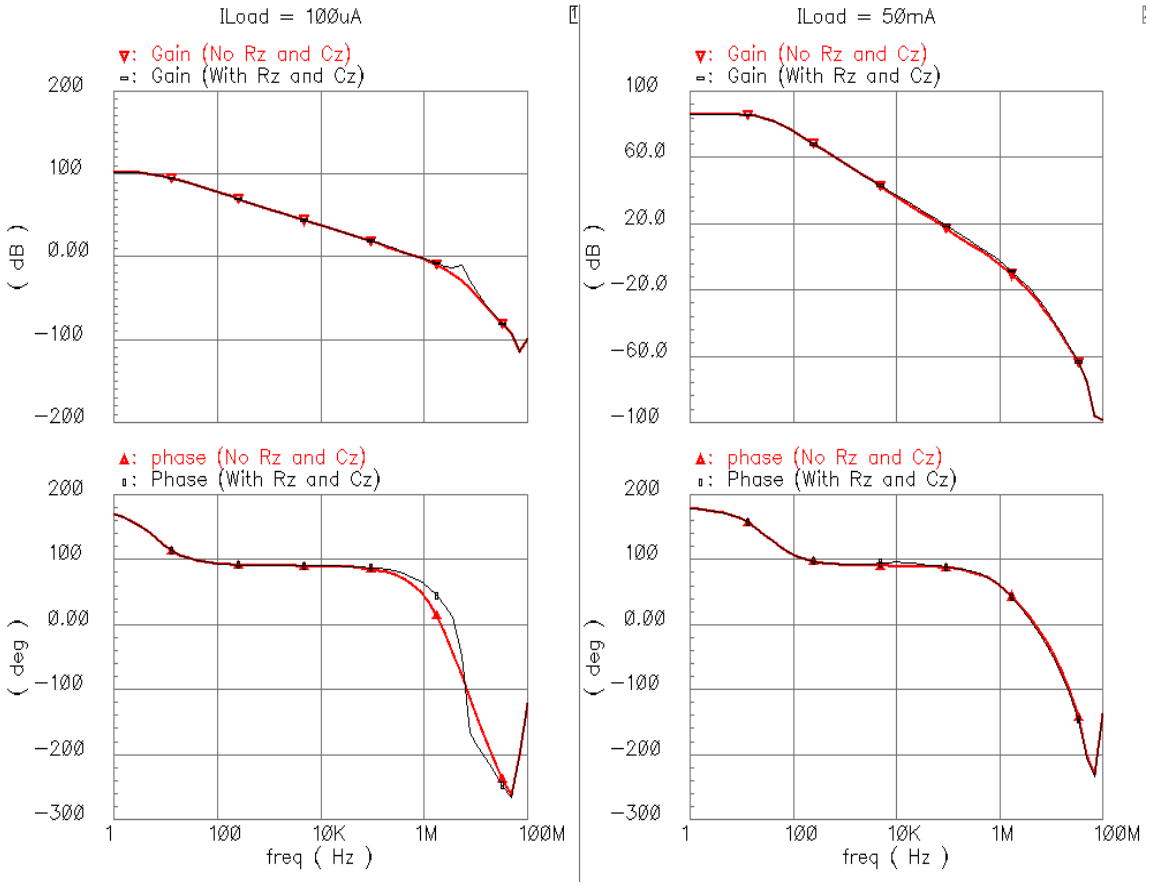


Fig. 4.8. AC Response with and without R_Z and C_Z

The variations of compensating capacitors C_C and C_F across process should be considered for stability. All the previously shown simulations doesn't take into account the variations for C_C and C_F. Fig. 4.9 and Fig. 4.10 show the effect of variation of C_C and C_F over stability respectively. Variation of about $\pm$30% about the actual value is carried for the compensating capacitors.

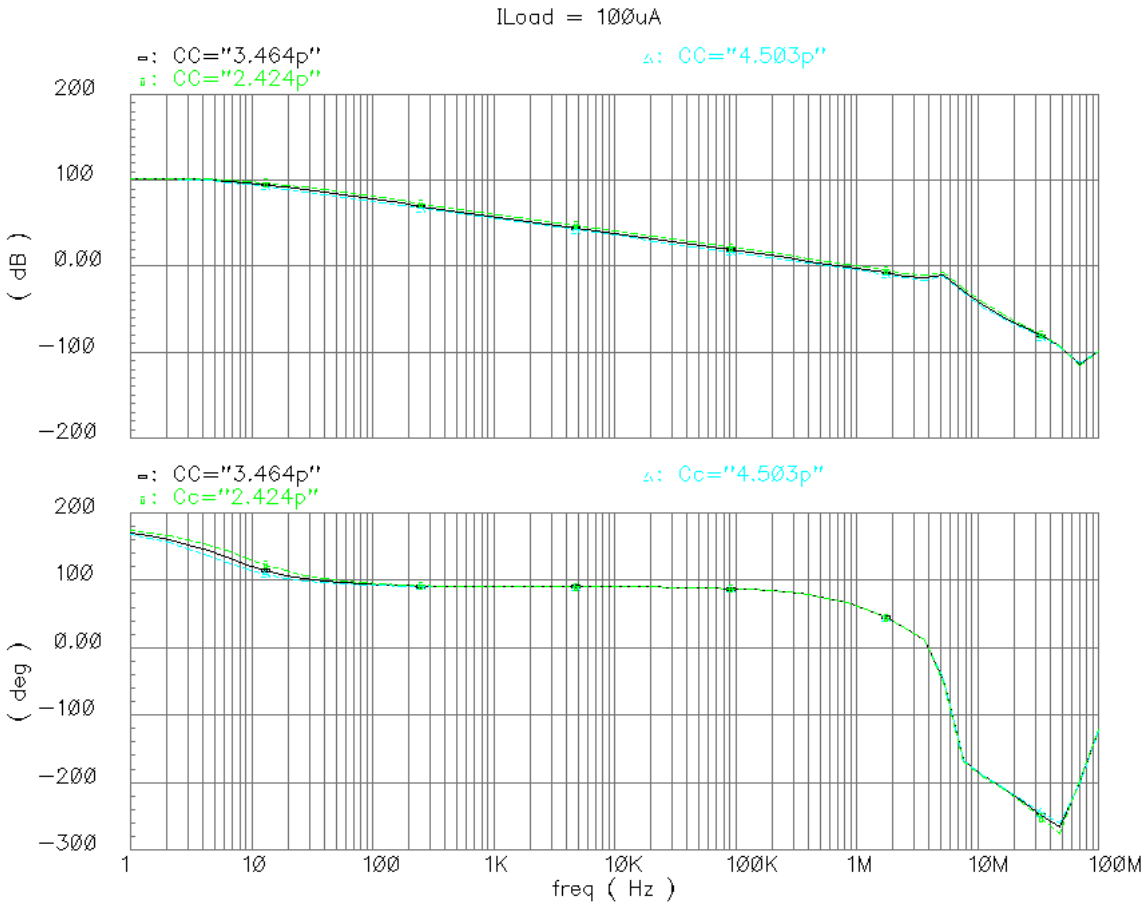


Fig. 4.9. Effect of C_C Variations on Stability for $I_{Load} = 100\mu A$

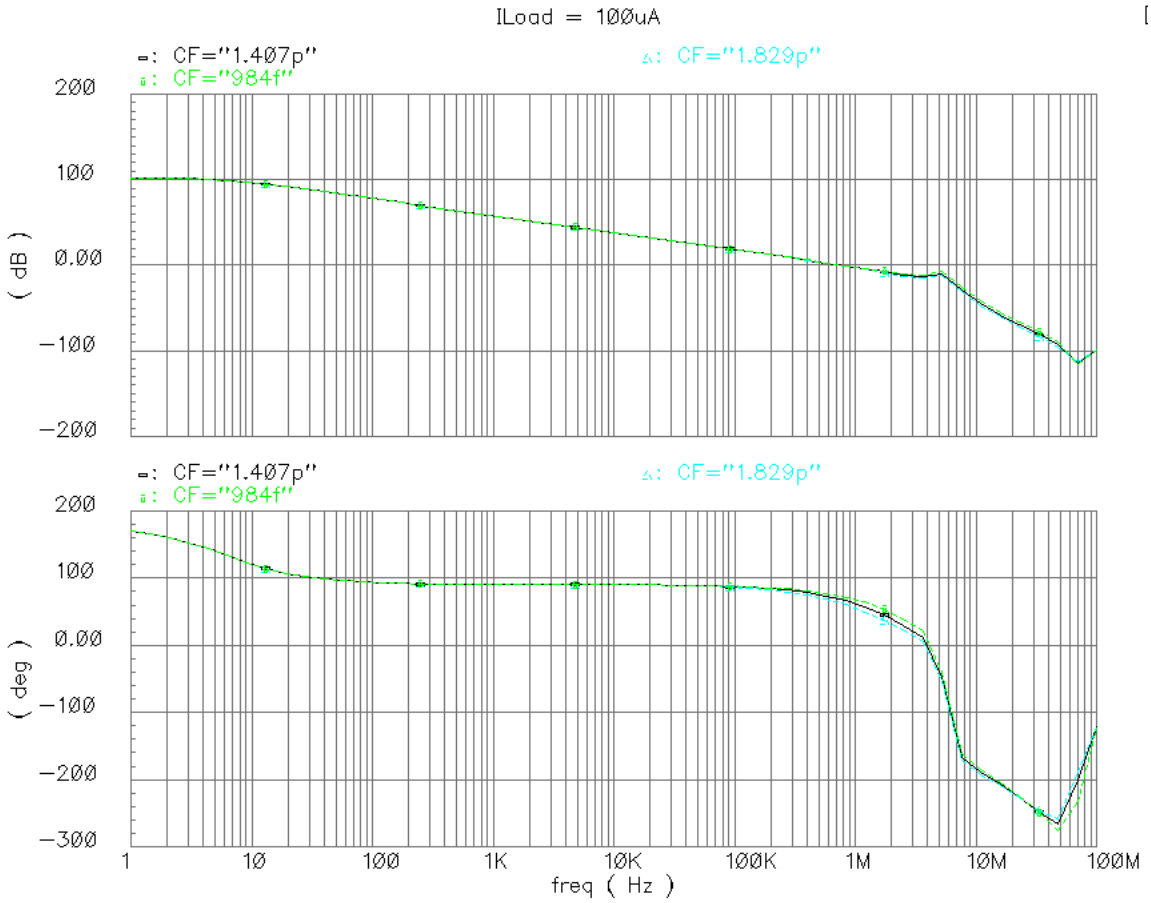


Fig. 4.10. Effect of C_F Variations on Stability for $I_{Load} = 100\mu A$

Decreasing the compensating capacitors increases the magnitude peaking and thus the GM is lower for -30% variations but still it is around 9 dB which is tolerable. From Fig. 4.11, it is also clear that a minimum phase margin of around 60° is maintained across the variations of the compensating capacitors.

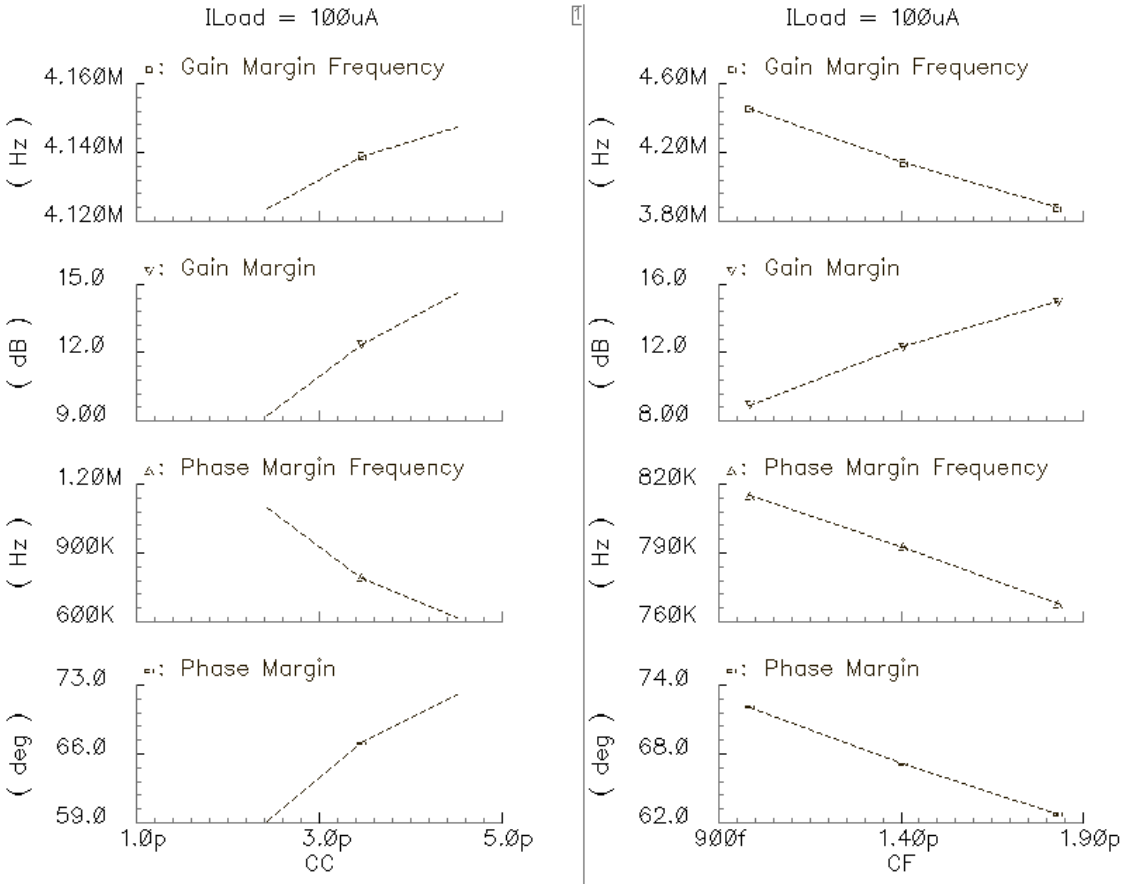
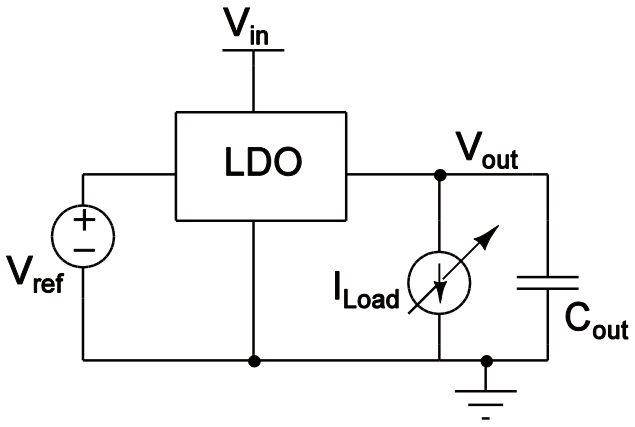


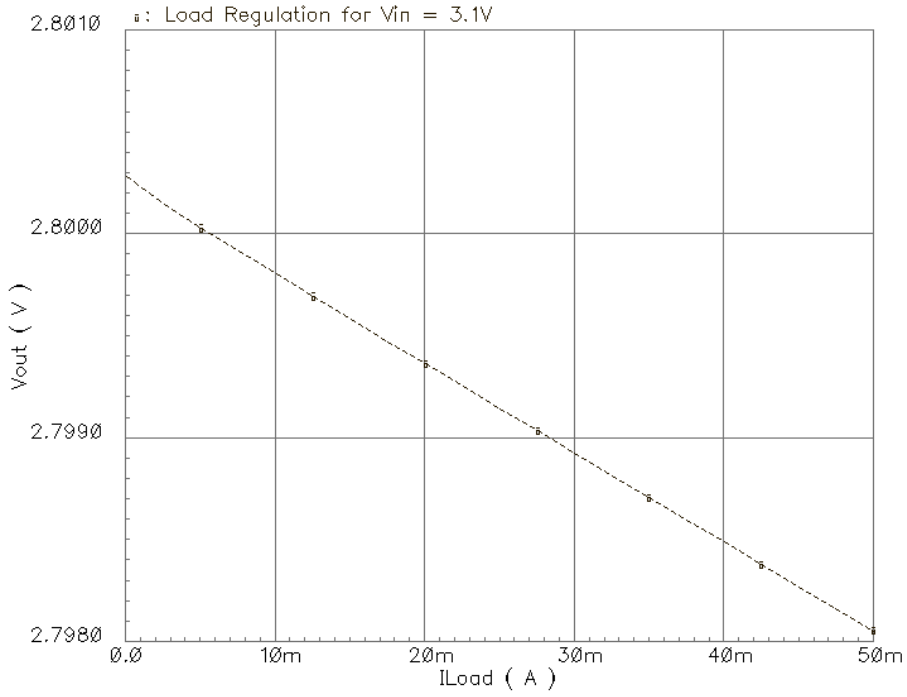
Fig. 4.11. Stability Parameters for Varying C_C and C_F

4.2.2. Load and Line Regulation

In steady state, simulations can be carried to measure the load and line regulation for a LDO. Load regulation setup is shown in Fig. 4.12a where the output voltage of the LDO is measured by sweeping the load currents from 100µA to 50mA and the simulation result is shown in Fig. 4.12b. The output voltage sees a delta change of just 2.2mV for a delta change of 50mA approximately in the load current when the supply is at 3.1V. The reason for such a good regulation is because of large DC gain for the proposed LDO's loop.

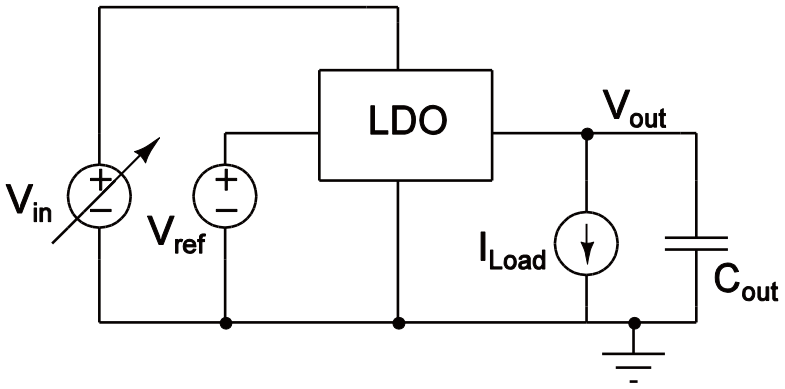


(a)

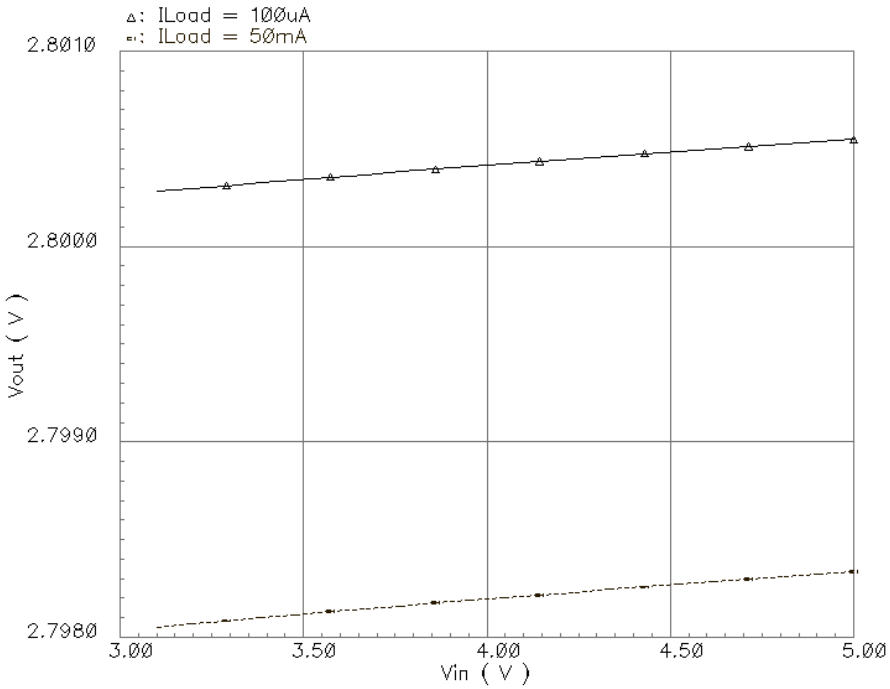


(b)

Fig. 4.12. Load Regulation (a) Setup (b) Simulation Plot



(a)



(b)

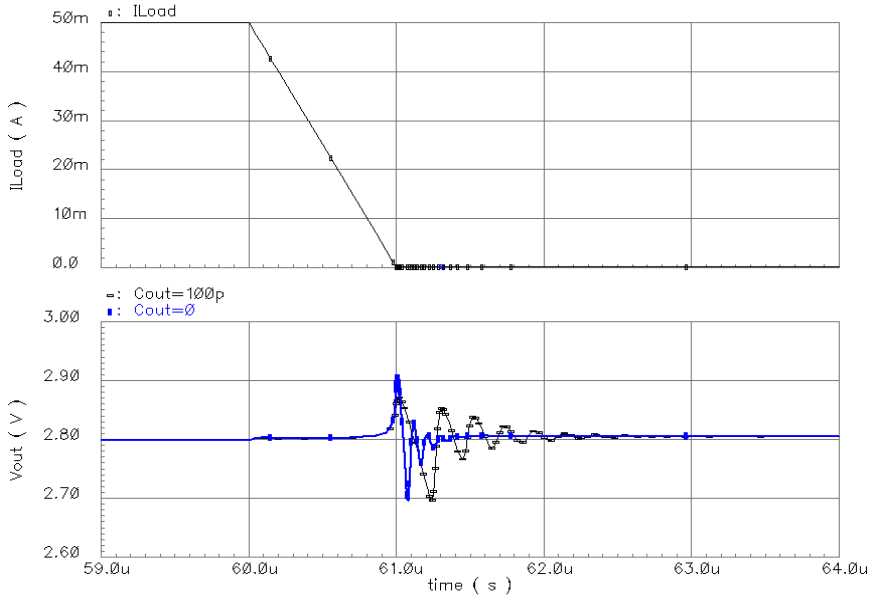
Fig. 4.13. Line Regulation (a) Setup (b) Simulation Plot

Line regulation is measured by sweeping the input supply voltage V_{in} from 3.1V to 5V. The simulation of line regulation for maximum and minimum load current is shown in Fig. 4.13b and the setup is shown in Fig. 4.13a. The output voltage showing a error within 1mV is also because of the huge DC gain in the loop.

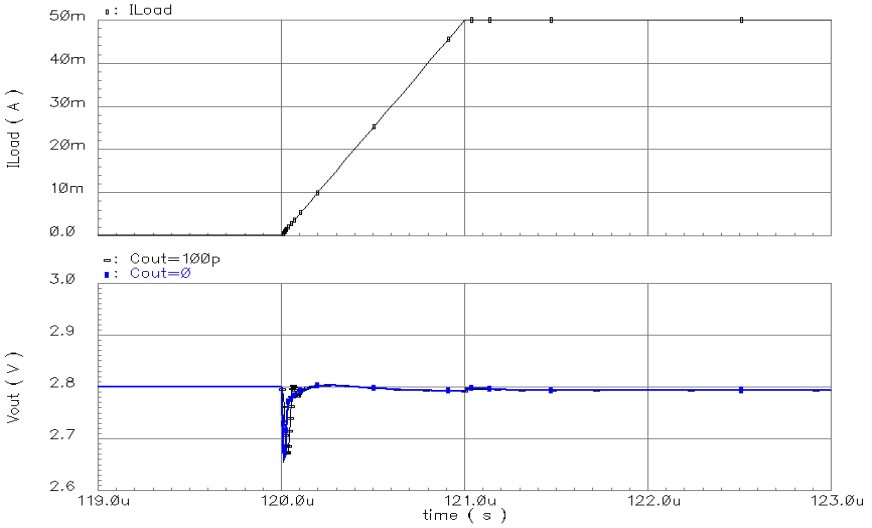
4.2.3. Load and Line Transients

Though the stability is checked with the help of the open loop AC response, it's always wise to check the stability through transient response. Transient response simulates the real time dynamic conditions for the LDO. Load transients simulations for $C_{out} = 0$ and 100pF are shown in Fig. 4.14a and Fig. 4.14b for load current switching between $100\mu A$ and 50mA with a rise and fall time of $1\mu s$. The transient glitches are almost the same for both the output capacitor conditions.

The line transient simulations involving the input supply V_{in} switching between 3.1V and 4V with a rise and fall time of $1\mu s$ are carried for minimum and maximum loading conditions. The results are shown in Fig. 4.15a and Fig. 4.15b.

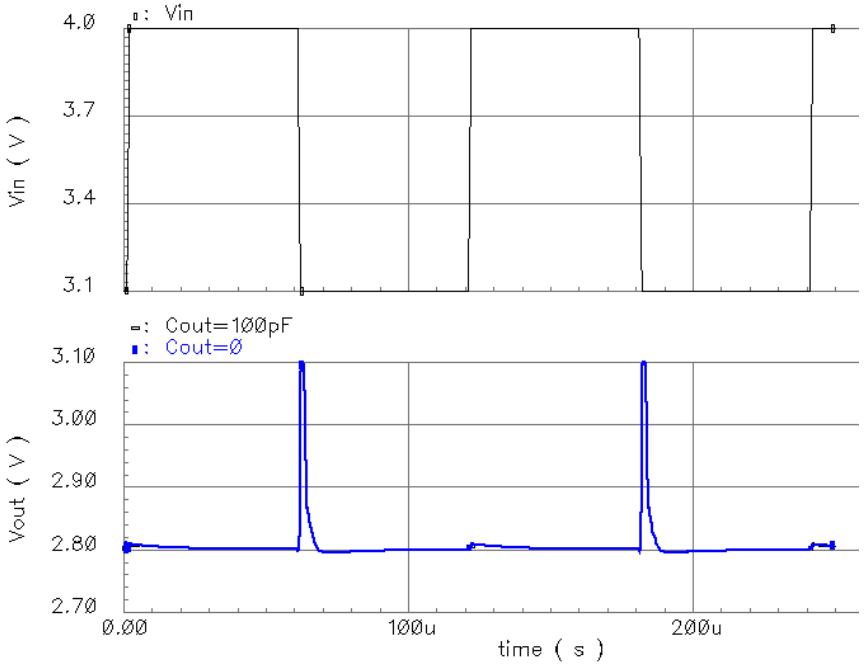


(a)

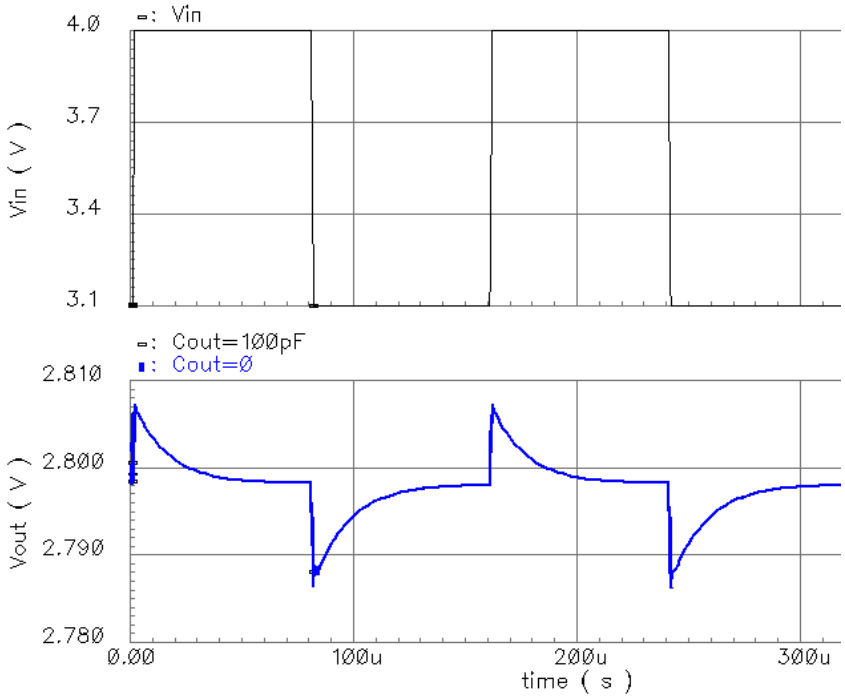


(b)

Fig. 4.14. Load Transient (a) (50mA to 100µA) (b) (100µ A to 50mA)



(a)



(b)

Fig. 4.15. Line Transient for (a) $I_{Load} = 100\mu A$ (b) $I_{Load} = 50mA$

4.2.4 PSR Simulations

The PSR simulations are carried for different output capacitors ($C_{out} = 0$ and $C_{out} = 100pF$) with different loading conditions in closed loop configuaration. The effect of C_{out} on the PSR is shown in Fig. 4.16 for 100µA and 50mA load currents. It is clear from Fig. 4.16 that the output capacitor has no effect on the PSR at 50mA load current and for 100µA the PSR is affected only after 2MHz frequencies. The $\pm$30% variation on R_Z and C_Z affects the PSR as shown in Fig. 4.17.

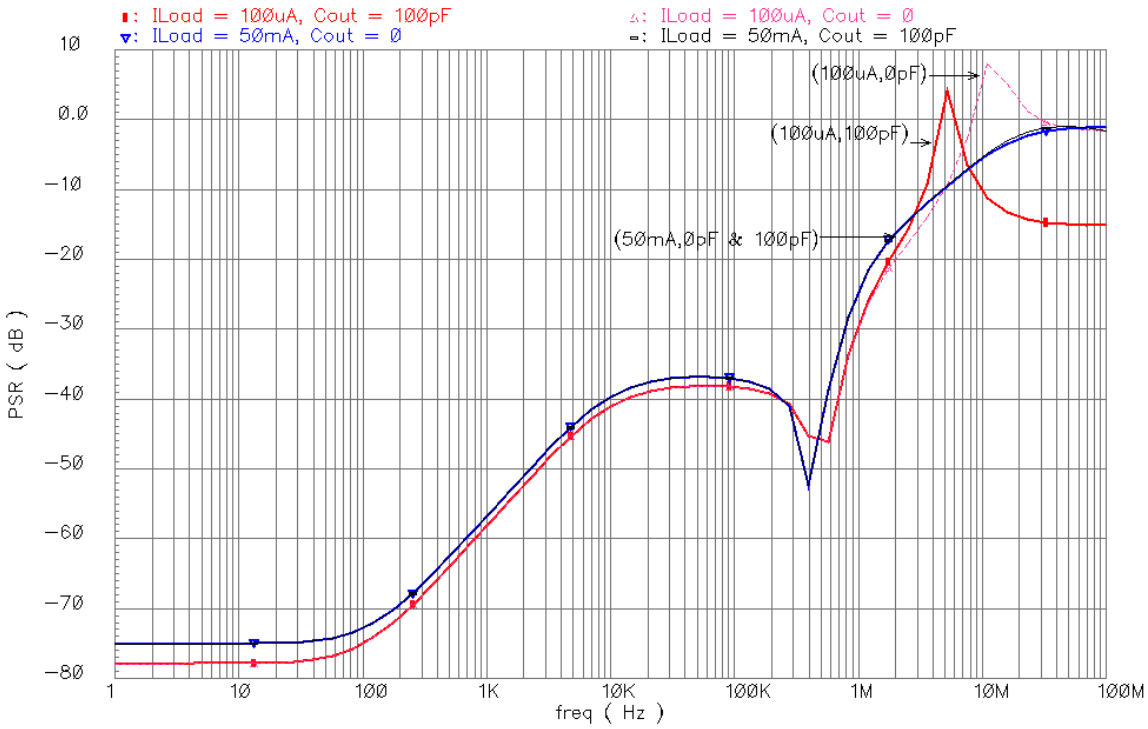


Fig. 4.16. PSR for Maximum and Minimum Load Currents for Different C_{out}

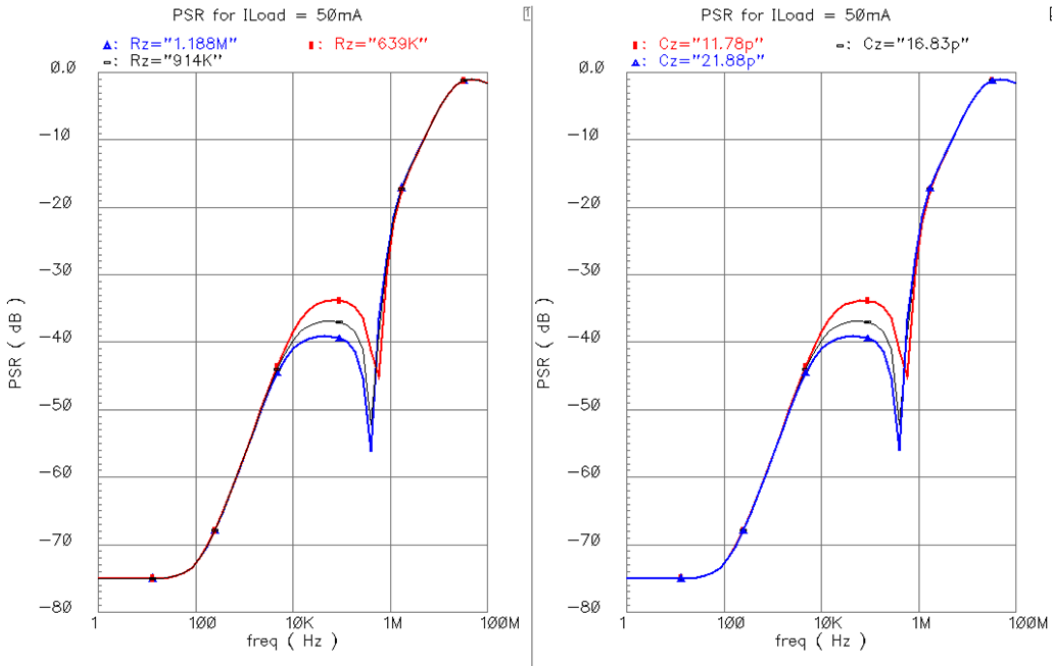


Fig. 4.17. PSR with R_Z and C_Z Variations for C_{out} = 100pF

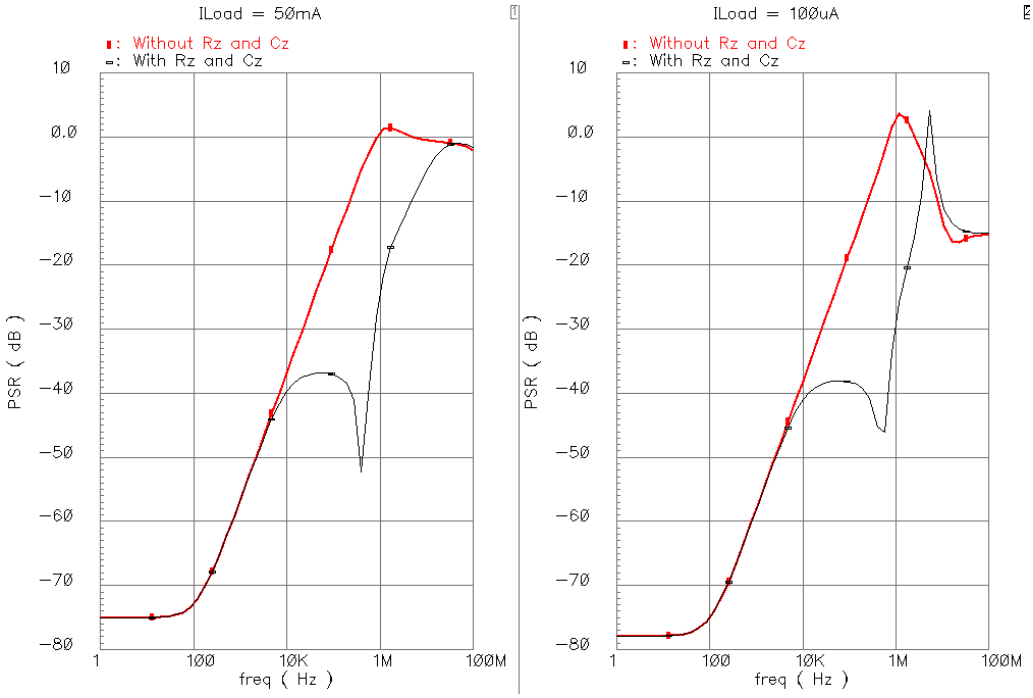


Fig. 4.18. PSR Comparison with and without R_Z and C_Z for C_{out} = 100pF

From Fig. 4.17, it is confirmed that the R_Z and C_Z play a major role for shaping the PSR. To prove the PSR enhancement which the proposed LDO has introduced, simulations are carried for the LDO with unity gain buffer (without R_Z and C_Z) and compared with the proposed buffer with R_Z and C_Z as illustrated in Fig. 4.18. The frequency for which the PSR is maintained at -35dB has been improved from 14kHz to 660kHZ with the proposed buffer compared to the conventional unity gain buffer. PSR simulations for 100µA, 1mA, 5mA, 25mA and 50mA load currents with $C_{out} = 100pF$ are plotted in Fig. 4.19.

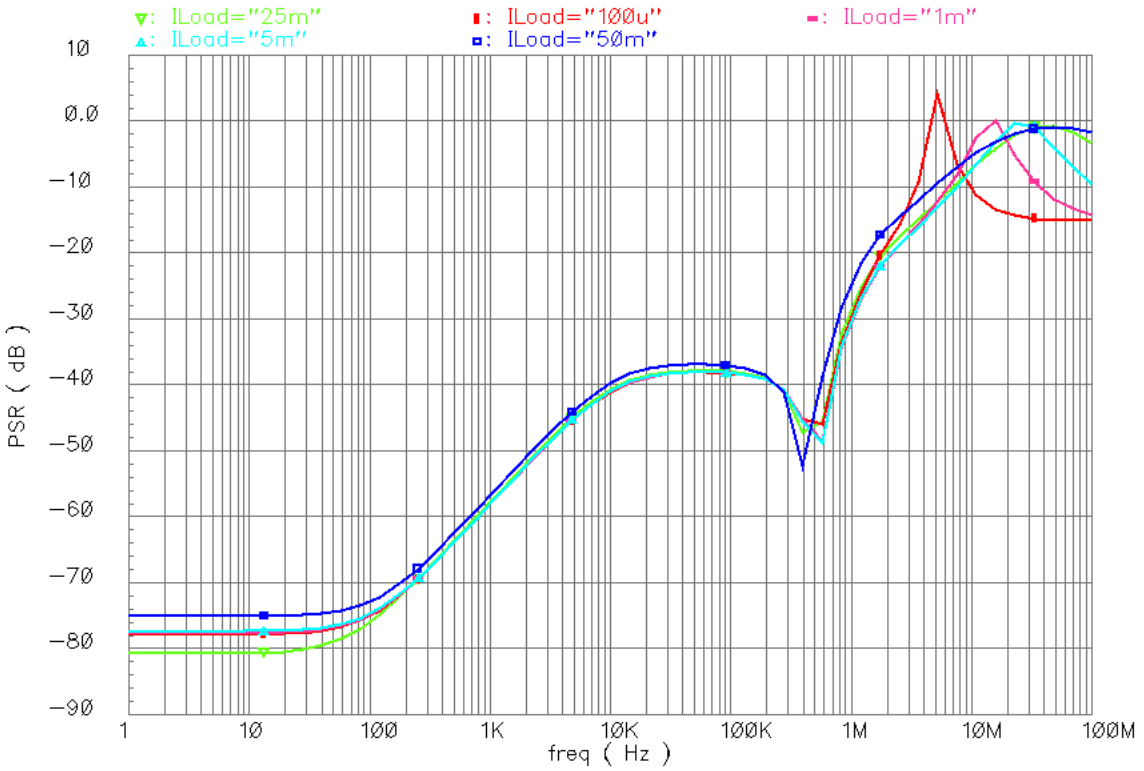


Fig. 4.19. PSR for Different I_{Load} with $C_{out} = 100pF$

4.2.5. Output Noise

The output noise for the LDO has been simulated in closed loop and plotted for minimum and maximum load currents in Fig. 4.20. The spectre model file for the On-Semi 0.5 µm doesn't have the flicker noise coefficients and hence the output noise appears almost flat because of just thermal noise till it get shaped by the output. The major noise contribution is from error amplifier and then from the feedback resistors. The buffer which act as the second stage and the pass transistor acting as third stage for the proposed LDO don't contribute to the output noise [8]. For the 100µA load current, the output noise shows a peak because the complex pole pair frequency ω_n comes closer to UGF_{LDO} according to (36). The integrated output noise from 1Hz to 100kHZ has been simulated and tabulated in Table IX for 100µA and 50mA loading conditions.

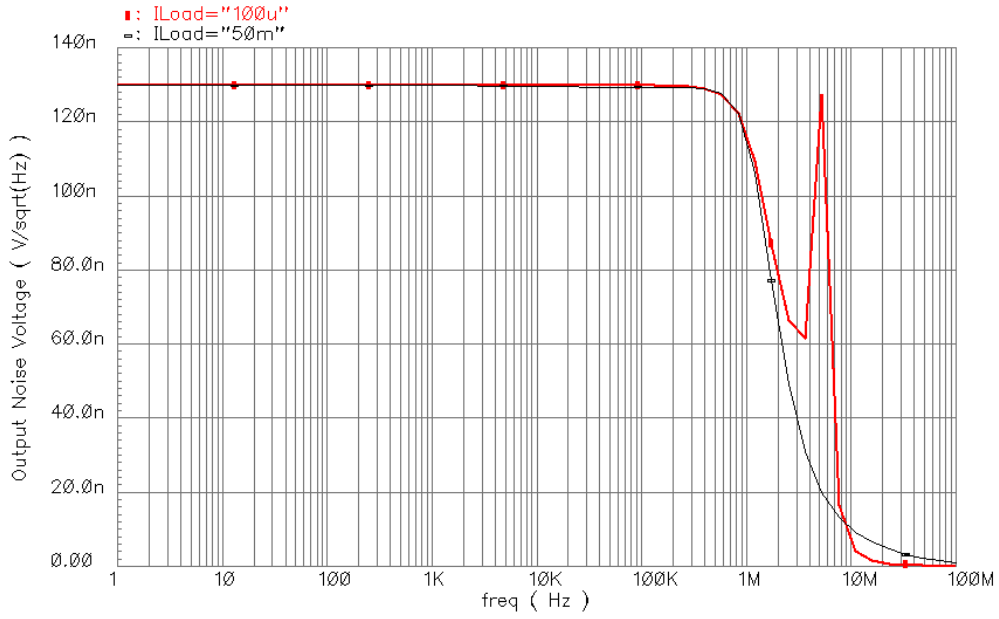


Fig. 4.20. Equivalent Output Noise for $C_{out} = 100pF$

TABLE IX

INTEGRATED OUTPUT NOISE FROM 1Hz TO 100KHz (ON-SEMI 0.5µm)

I_{Load}	Output Noise
100µA	41.04µV
50mA	40.93µV

4.3. Corner Simulations

So far all the simulations shown before are run using TT (Typical-Typical) model file. There are four other corner model files which should be used for the simulations to know the worst case LDO performance. The four corners are FF (Fast-Fast), SS (Slow-Slow), FS (Fast-Slow) and SF (Slow-Fast). Moreover so far the effects of temperature on the LDO performance has not be accounted. Table X and Table XI shows corner simulations values for 50mA / 100µA load currents at room temperature (27°C) and high temperature (85°C).

TABLE X

CORNER SIMULATION AT 27°C (0.5µm)

Parameter	TT	FF	SS	FS	SF
DC Gain (dB)	86/102	86/102	83/101	84/103	86/103
PM (°)	66/67	67/68	68/69	68/69	68/69
UGF (kHz)	774/792	787/800	714/727	737/752	724/736
GM (dB)	22/12	23/16	23/15	22/15	23/15
GMF (MHz)	4.5/4.1	4.9/4.8	4.5/4.5	4.5/4.6	4.7/4.6
Overshoot (mV)	71	58	63	60	62
Undershoot (mV)	126	102	113	107	111
DC PSR	75/78	75/78	74/78	74/77	76/80
-35 dB PSR (kHz)	666/802	751/1026	681/971	652/934	722/990

TABLE XI

CORNER SIMULATION AT 85℃ (0.5µm)

Parameter	TT	FF	SS	FS	SF
DC Gain (dB)	82/101	82/102	79/101	79/102	83/101
PM (°)	67/68	68/70	69/71	68/70	69/71
UGF (kHz)	672/732	685/705	623/641	640/660	633/648
GM (dB)	20/12	21/13	21/14	20/13	21/13
GMF (MHz)	3.5/3.6	3.8/4.1	3.5/4	3.4/4	3.7/4.1
Overshoot (mV)	94	77	84	78	81
Undershoot (mV)	172	141	154	144	152
DC PSR	74/78	74/77	72/76	72/77	76/79
-32 dB PSR (kHz)	548/793	585/1020	534/968	518/929	566/1017

In all the process and temperature corners, the proposed LDO seems to be stable with a minimum PM of at least 66° and GM of about 12dB. The PSR degrades at high temperature (85°) because of drop in the DC gain and also the transistors become slower because the threshold voltage and mobility decreases with temperature which in turn decreases drain current.

4.4. Final LDO Layout

The final layout for the proposed LDO has been laid out using On-Semi 0.5µm CMOS technology. Common centroid and interleaving techniques are employed for the layout of transistors, resistors and capacitors for better matching. The huge pass transistor's total width 14.4mm is split into 32 transistor blocks each of width 25x18µm. All the PMOS devices are surrounded by metal1 to n-well guard rings which act as the bulk and then by a layer of metal1 to p-sub guard rings. All the NMOS devices and

resistors are surrounded by a layer of metal1 to p-sub guard rings. The guard rings are necessary to avoid latch-up issues and discharge any charges trapped during the fabrication process. The final layout of the proposed capacitor-less LDO is shown in Fig. 4.21. The proposed LDO occupies an area of 550µm x 654µm while the entire chip with the pad frame measures 1.5mm x 1.5mm in area. The pass transistor occupies about ½ of the total effective area. The empty spaces inside the chip pad frame are filled with different metals and poly to meet the minimum metal density constraints. The feedback resistors R_{F1} and R_{F2} are interweaved to match in a better way and laid out using high resistance poly layer. The compensation capacitors are laid out using poly-elec layers. C_Z capacitor is split into 16 units each of value 1.052pF.

The chip is packaged using 40 pin dual-inline package. The pads with ESD protection are used for the chip. Critical nodes like V_{in} and V_{out} are connected to 4 pins each and ground node is connected to 8 pins. Connecting to multiple pins in parallel reduces the bond inductance and resistances.

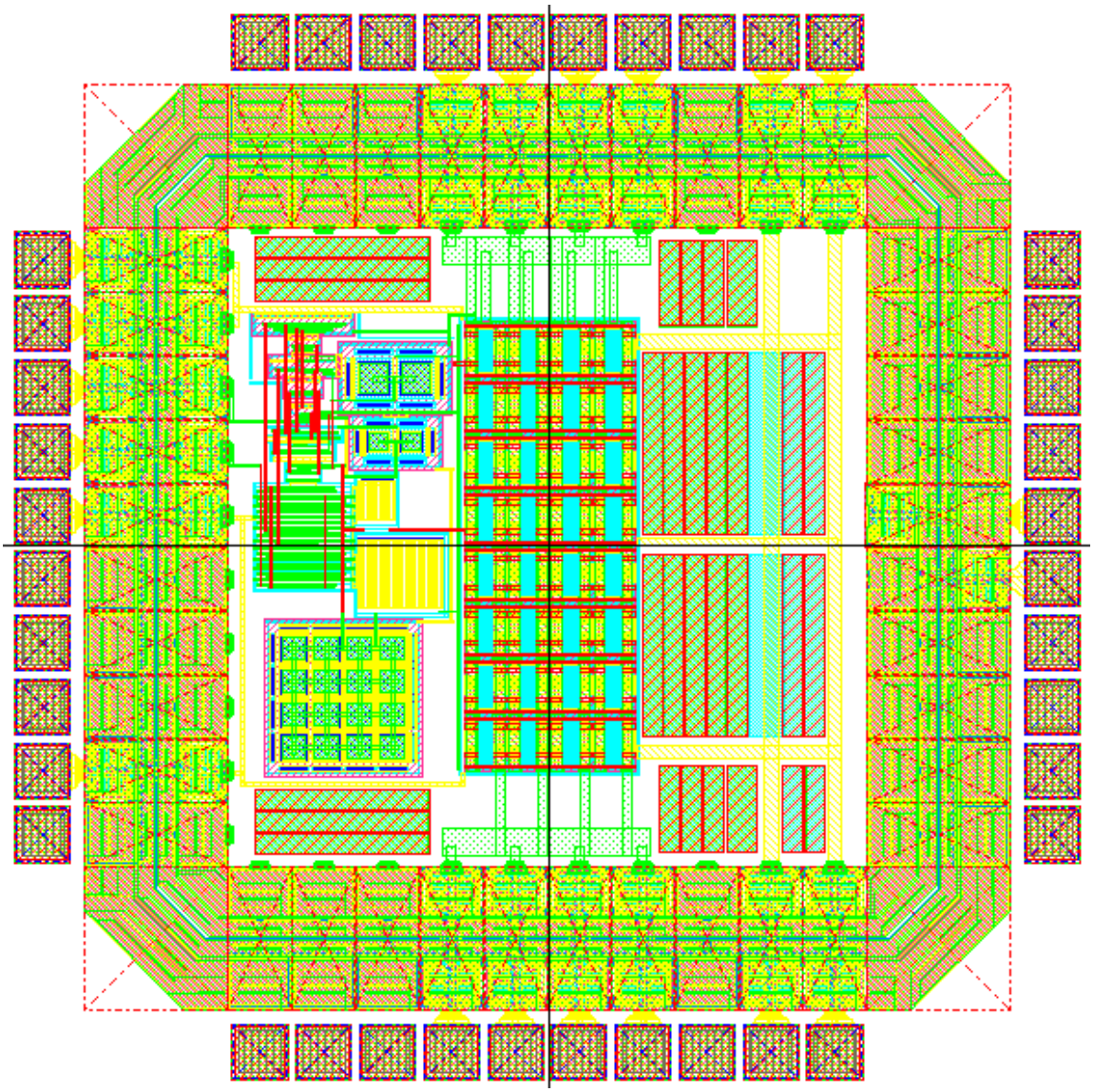


Fig. 4.21. Final LDO Layout (0.5µm)

5. TRANSISTOR LEVEL DESIGN AND SIMULATION (0.18µm)

5.1. Transistor Level Design

The transistor level implementation of the proposed cap-less LDO using TSMC 0.18µm CMOS technology is shown in Fig. 5.1. The bias for transistor M_6 is modified from the 0.5µm design. The biasing circuitry for the LDO is shown in Fig. 5.2. The resistor R_{B2} is an externally connected resistor to set the bias current for the buffer. The main specification for which the proposed LDO is designed is listed in Table XII. The design procedure followed is same as used for 0.5µm, listed in Table IV. The final circuit parameters are given in Table XIII and Table XIV.

TABLE XII

PROPOSED LDO MAIN SPECIFICATIONS (0.18µm)

PARAMETER	VALUE
V_{in} (V)	≥1.8
V_{out} (V)	1.6
$I_{LOAD,min}$ (µA)	150
$I_{LOAD,max}$ (mA)	50
C_{out} (pF)	0 – 30

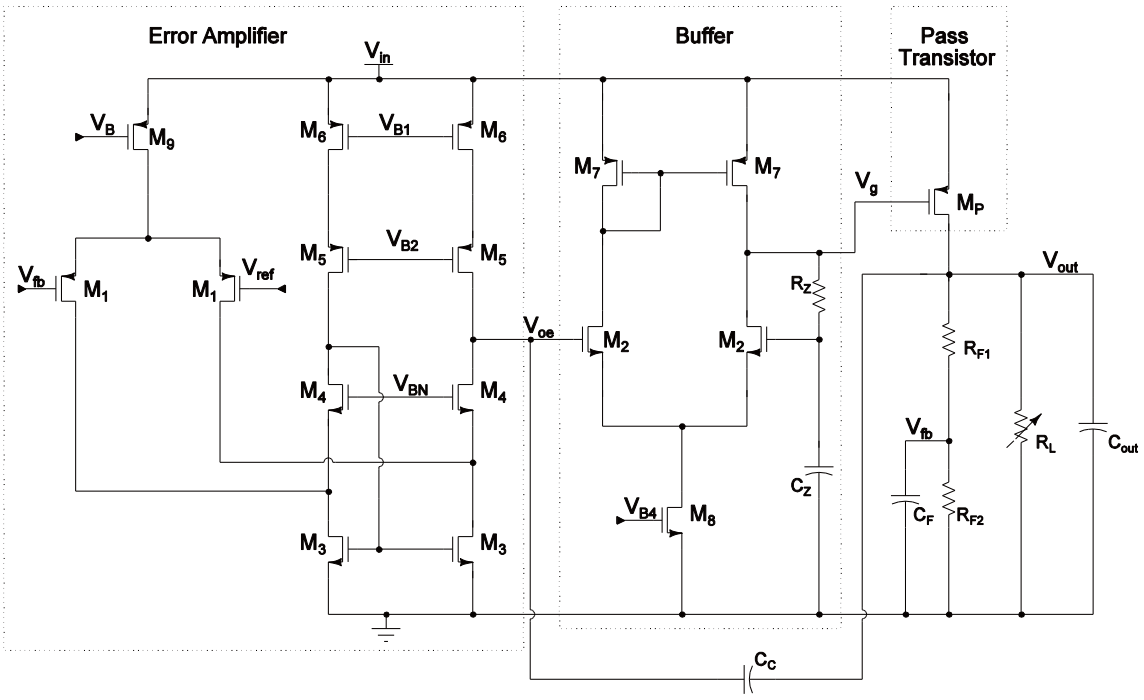


Fig. 5.1. Proposed Cap-less LDO Transistor Level Design in (0.18µm)

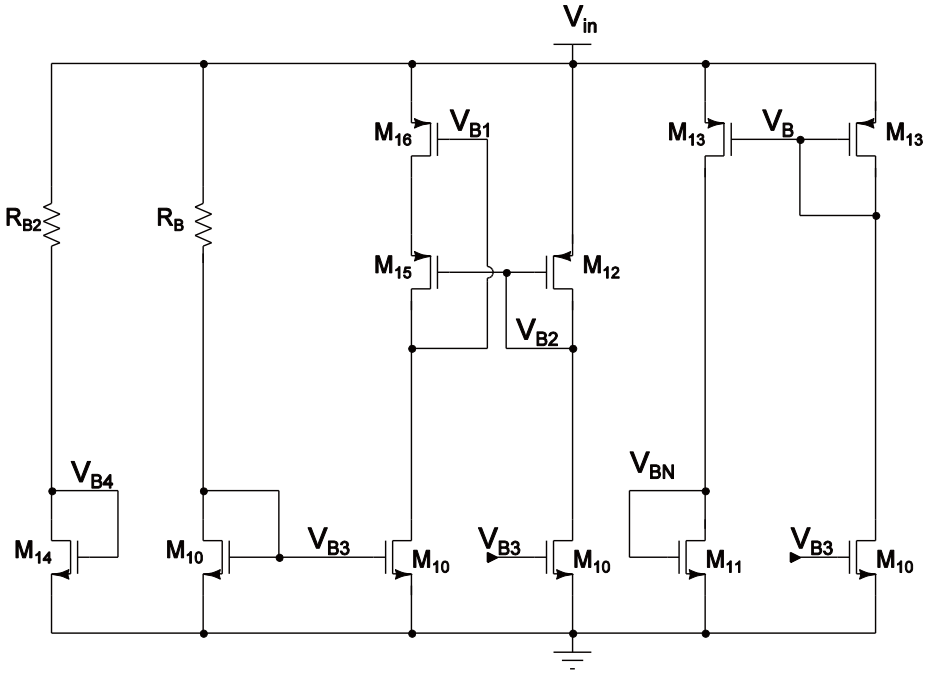


Fig. 5.2. Biasing Circuit for the Proposed LDO (0.18µm)

TABLE XIII

FINAL ACTIVE CIRCUIT PARAMETERS (0.18µm)

TRANSISTOR	W(µm)	L(µm)	I_D(µA)
M_1	8	0.8	2
M_2	21.6	0.6	30
M_3	7.2	2	4
M_4	4	2.4	2
M_5	11.2	1.5	2
M_6	9.6	1.5	2
M_7	4.8	0.18	30
M_8	112	2	60
M_9	32	2.5	4
M_{10}	4	4	1
M_{11}	0.9	13	1
M_{12}	2	7	1
M_{13}	8	2.5	1
M_{14}	8	2	4.3
M_{15}	5.6	1.5	1
M_{16}	4.8	1.5	1
M_P	3840	0.18	10

TABLE XIV

FINAL PASSIVE CIRCUIT PARAMETERS (0.18µm)

PARAMETER	VALUE
C_C	0.78pF
C_F	0.46pF
C_Z	9.6pF
R_Z	600kΩ
R_{FB}	1.8MΩ
R_{F1}, R_{F2}	80kΩ

The drop across the bond inductance and resistance in the output pin result in degraded load regulation. Such effects can be reduced by employing Kelvin connection for the output pin of the LDO as shown in Fig. 5.3. The drain of the pass transistor and

feedback resistors are connected separately to two pads which is connected to the same pin V_{out} in the package. Kelvin connection is another modification made in TSMC 0.18µm compared to the On-Semi 0.5µm design.

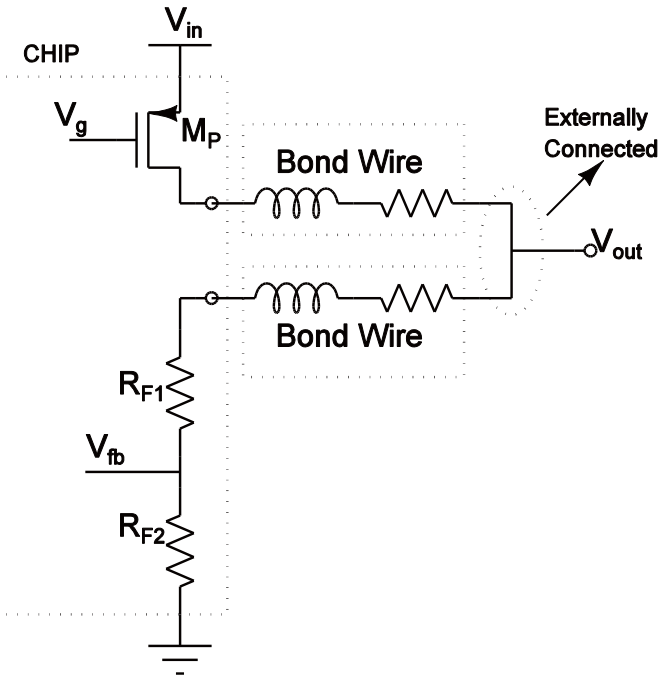


Fig. 5.3. Kelvin Connection for LDO

5.2. Schematic Simulations

The schematic level simulation values for 50mA/150µA carried using Spectre in Cadence are tabulated in Table XV for room temperature (27°C) and Table XVI for high temperature (85°C) across three corners [TT (Typical-Typical), FF (Fast-Fast) and SS (Slow-Slow)].

TABLE XV

SCHEMATIC CORNER SIMULATION AT 27℃ (0.18µm)

Parameter	TT	FF	SS
DC Gain (dB)	86/104	84/99	84/104
PM (°)	56/60	56/60	55/60
UGF (MHz)	3.1/3.28	3.84/4	2.56/2.68
GM (dB)	14/12	13/9	14/14
GMF (MHz)	9.6/11.4	11.7/12.4	7.8/10.3
Overshoot (mV)	39	37	42
Undershoot (mV)	63	60	68
Load Reg (µV/mA)	2.7	1.5	6
0.1% Settling Time (µs)*	3.1/3.5	2.6/3	3.4/3.8
DC PSR (dB)	-79/-85	-76/-82	-77/-85
-40 dB PSR (MHz)	1.22/1.61	1.57/1.84	1.05/1.47

TABLE XVI

SCHEMATIC CORNER SIMULATION AT 85℃ (0.18µm)

Parameter	TT	FF	SS
DC Gain (dB)	85/104	84/99	83/105
PM (°)	55/60	56/60	55/61
UGF (MHz)	2.95/3.17	3.66/3.95	2.44/2.58
GM (dB)	13/11	13/8	13/13
GMF (MHz)	8.8/10.7	10.8/11.4	7.1/9.7
Overshoot (mV)	48	47	50
Undershoot (mV)	77	75	80
Load Reg (µV/mA)	2.6	3	6
0.1% Settling Time (µs)*	3.7/4.2	2.9/3.5	4.4/4.8
DC PSR (dB)	-79/-86	-76/-82	-86/-77
-38 dB PSR (MHz)	1.18/1.7	1.51/1.93	0.99/1.54

*Settling time with 0.1% error during a load current step from $I_{LOAD,min}$ to $I_{LOAD,max}$ / $I_{LOAD,max}$ to $I_{LOAD,min}$ with 1µs rise and fall times.

5.3. Final LDO Layout

The final layout for the proposed LDO laid out using TSMC 0.18µm CMOS technology is shown in Fig. 5.4. Common centroid and interleaving techniques are employed for the layout of transistors, resistors and capacitors for better matching. The huge pass transistor's total width 3.84mm is split into 16 transistor blocks each of width 20x12µm. Guard rings are added in the layout as discussed earlier in section 4.4 to avoid latch-up. The proposed LDO occupies an area of 320µm x 254µm while the entire chip with the pad frame and seal ring enclosure measures 0.56mm x 0.41mm in area. High resistance poly is used for laying all the resistors and mim capacitors are used for all the capacitances in the layout. C_Z capacitor is split into 16 units each of value 0.6pF. The final chip's layout has been submitted for fabrication.

5. 4. Post-Layout Simulations

Table XVII and Table XVIII show corner post-layout simulation values for 50mA / 100µA load currents at room temperature (27°C) and high temperature (85°C). The worst case appears to be the SS corner at high temperature.

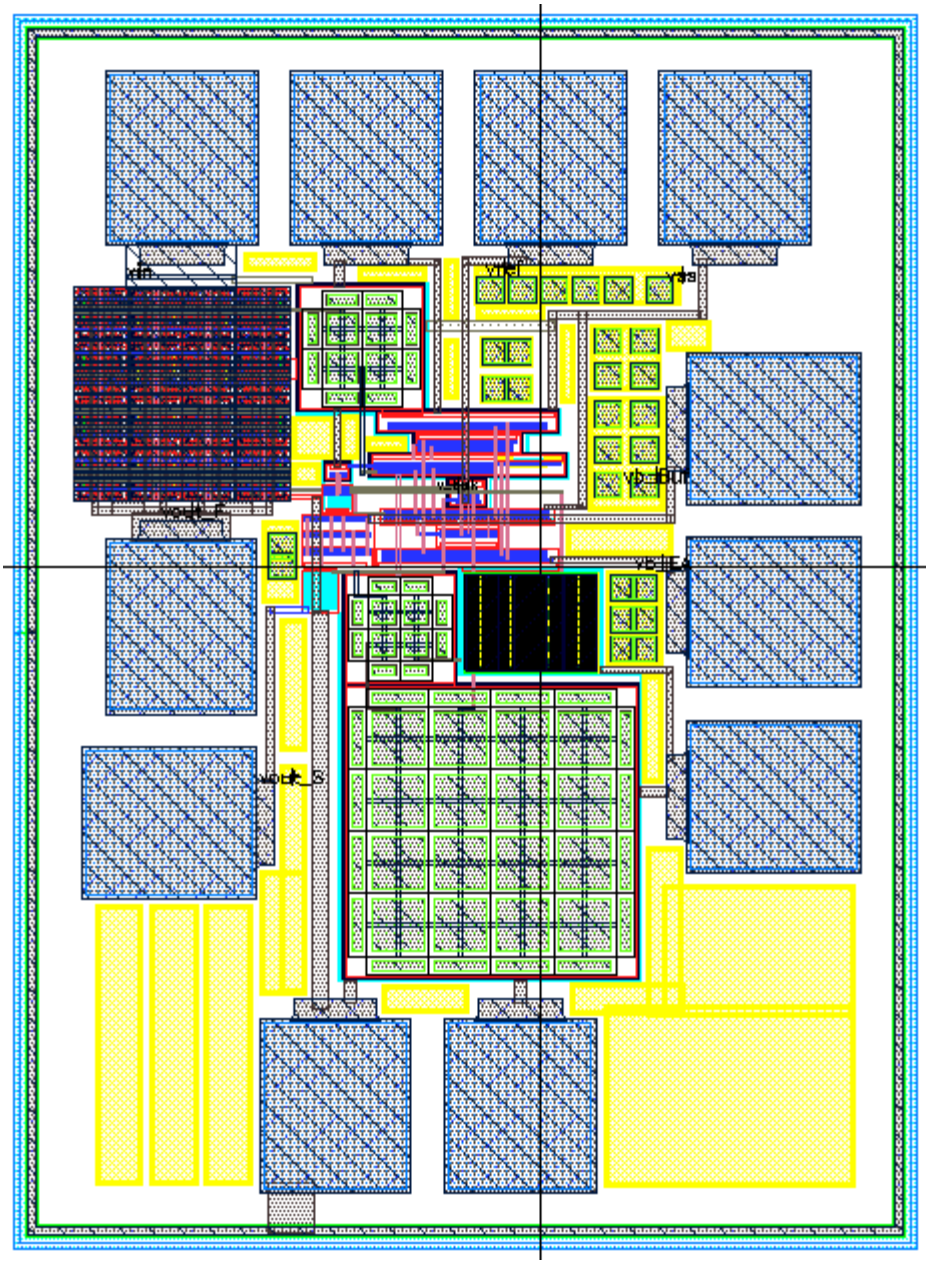


Fig. 5.4. Final LDO Layout (0.18µm)

TABLE XVII

POST-LAYOUT CORNER SIMULATIONS AT 27℃ (0.18µm)

Parameter	TT	FF	SS
Overshoot (mV)	48	49	53
Undershoot (mV)	80	78	87
DC PSR*	-83/-77	-90/-79	-79/-78
-38 dB PSR (MHz)	1.1/1.46	1.33/1.63	0.86/1.29
-30 dB PSR (MHz)	1.41/2.1	1.69/2.29	1.14/1.82
Load Reg (µV/mA)	3	1.6	6.4
0.1% Settling Time (µs)*	3.3/3.8	2.8/3.2	3.8/4.1

TABLE XVIII

POST-LAYOUT CORNER SIMULATIONS AT 85℃ (0.18µm)

Parameter	TT	FF	SS
Overshoot (mV)	59	59	63
Undershoot (mV)	100	96	105
DC PSR	-84/-77	-94/-79	-81/-77
-36.5 dB PSR (MHz)	1.04/1.5	1.23/1.66	0.82/1.32
-30dB dB PSR (MHz)	1.22/1.95	1.55/2.18	1.02/1.71
Load Reg (µV/mA)	3	1.6	7
0.1% Settling Time (µs)*	4.4/4.5	3.6/3.7	4.8/5.1

*Settling time with 0.1% error during a load current step from $I_{LOAD,min}$ to $I_{LOAD,max}$ / $I_{LOAD,max}$ to $I_{LOAD,min}$ with 1µs rise and fall times.

6. EXPERIMENTAL RESULTS

6.1. Test Board

The PCB for testing the regulator chip is fabricated using two-layer copper plate. The test setup for the PCB is illustrated briefly in Fig. 6.1. R_{fil} and C_{fil} act as low pass filter for the reference V_{ref}. The bias resistor is split into a fixed and variable resistor each of value 500kΩ to generate 2.5μA bias current. The final PCB with the chip and other required components for measurement and generating reference bias are soldered as displayed in Fig. 6.2a and Fig. 6.2b. The reference voltage V_{ref} is supplied by using a external power supply. SMA connectors are used to supply input voltage V_{in} and monitor output voltage V_{out}. The circuit board also contains passive components like potentiometers, resistors , headers and capacitors. A N – Channel 20V (D-S) MOSFET (SC-75A) is also soldered to measure load transients. The load transient setup circuit is explained in detail in Fig. 6.3.

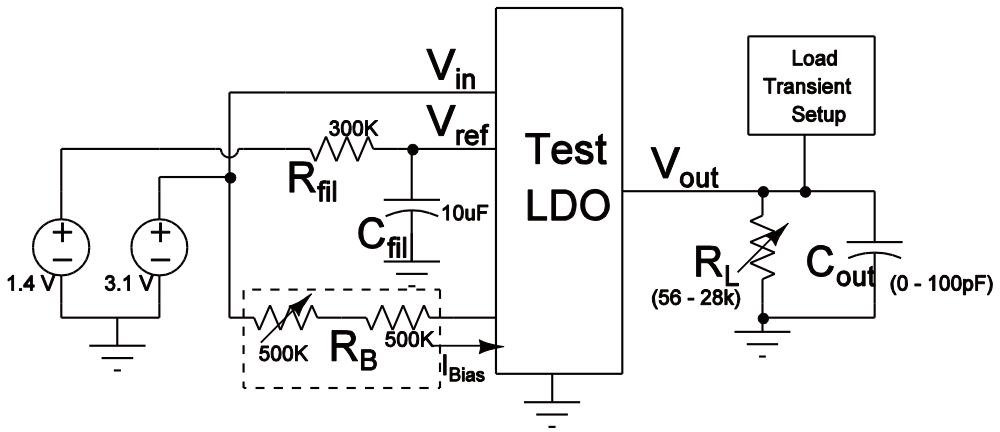


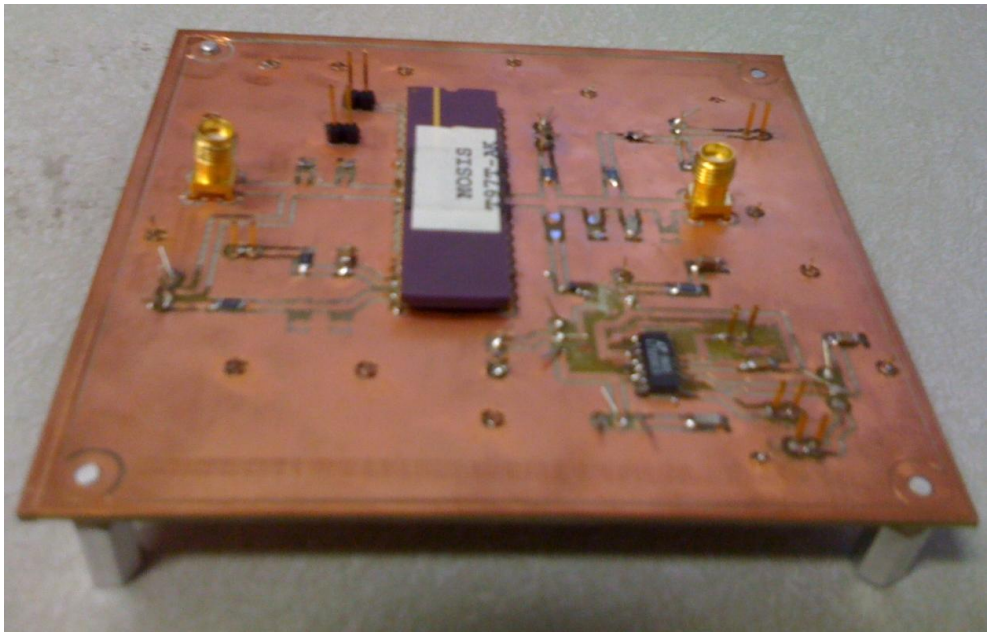
Fig. 6.1. PCB Test Setup

6.2. Transient Response

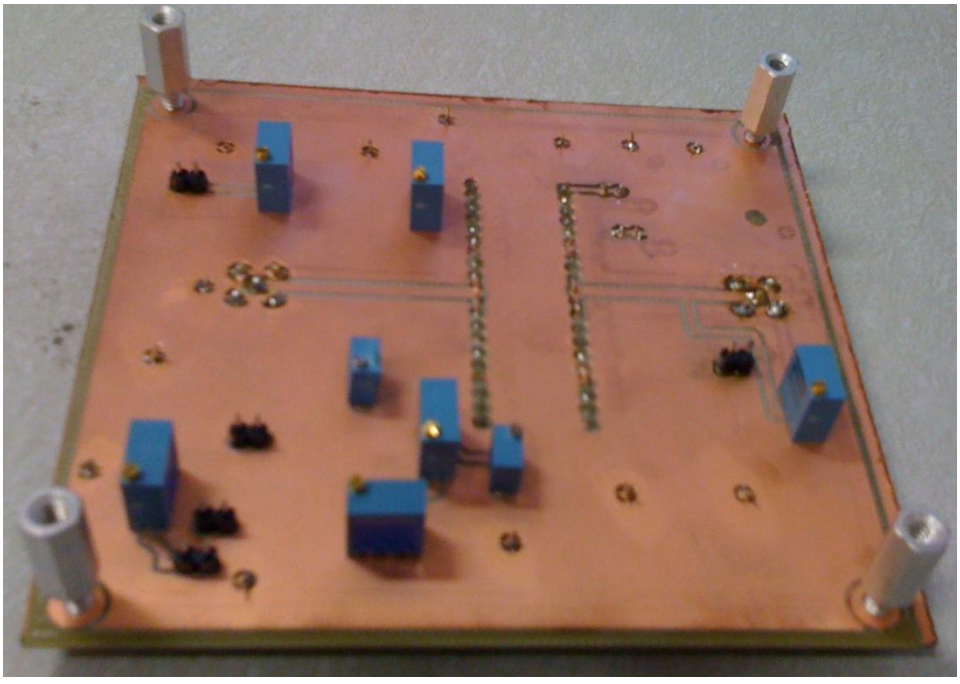
The measurement of the transient response of the proposed LDO requires a DC power supply, function generator and an oscilloscope. The function generator is used to generate clock which helps for switching between the load currents.

6.2.1. Load Transient Response

The load transient is measured by switching the load current between 100μA and 50mA. The test circuit is shown in Fig. 6.3. The rise and fall time are set as 500ns for the load transient current by changing the cut-off of the low pass filter connected to the gate of the SC-75A NMOS. The parasitic capacitance of SC-75A doesn't load the LDO since it is around 20 to 30 pF for our operating condition. The measured waveforms are shown in Fig. 6.4a and Fig. 6.4b for no external capacitor and for C_{out} = 100pF in Fig. 6.5a and Fig. 6.5b. It is clear from Fig. 6.4 and Fig. 6.5 that load transient is not affected by the output capacitance.



(a)



(b)

Fig. 6.2. (a) Top View (b) Bottom View of the Final PCB

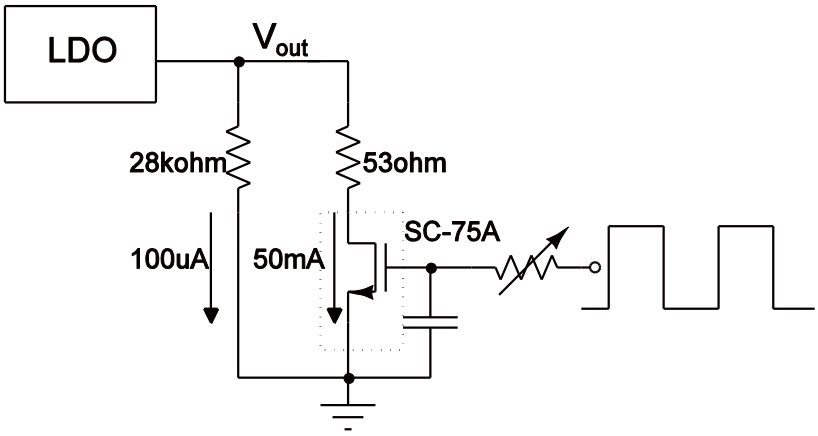
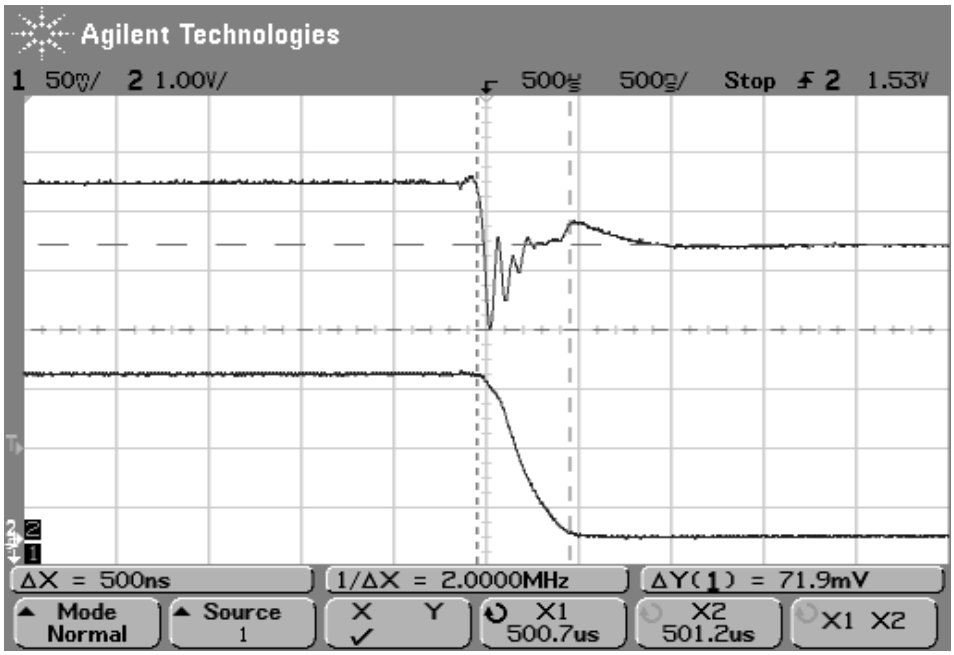
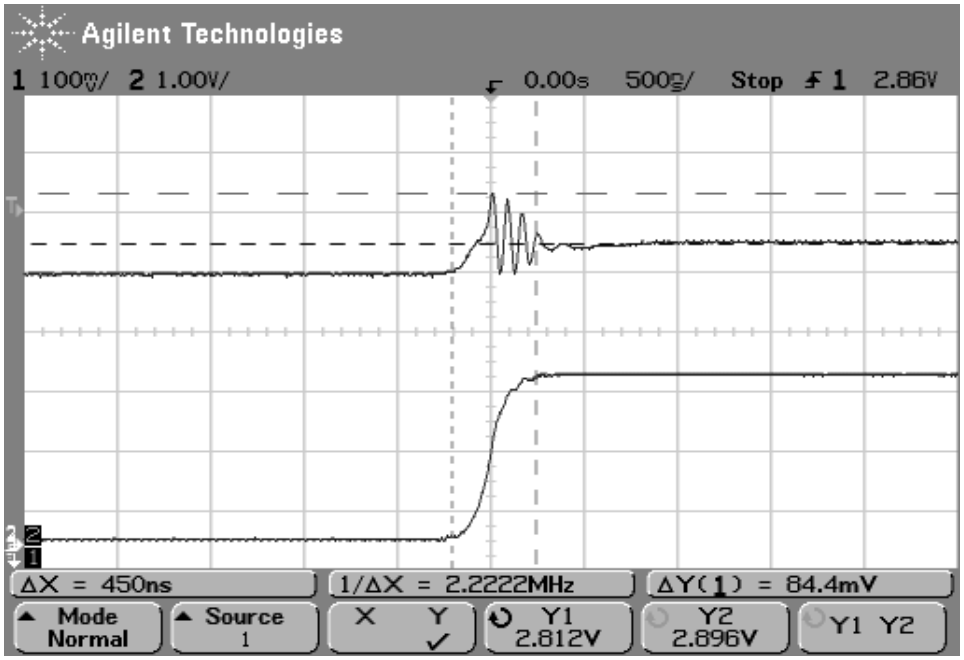


Fig. 6.3. Load Transient Test Setup

The second channel voltage as shown in Fig. 6.4 and Fig. 6.5 is the drop across the 53Ω resistor shown in Fig. 6.3. The measured results show better performance as against schematic results for both extremes of the output capacitor. The ringings in the load transients measured just last for 500ns and then the output voltage settles to its final value. This proves that the proposed capacitor-less LDO is stable for minimum to maximum load current. The final value for the output voltage at 50mA settles to a value about 40mV less compared to the simulated value. This is because of the absence of Kelvin connection for the output pin of the LDO in 0.5µm design.

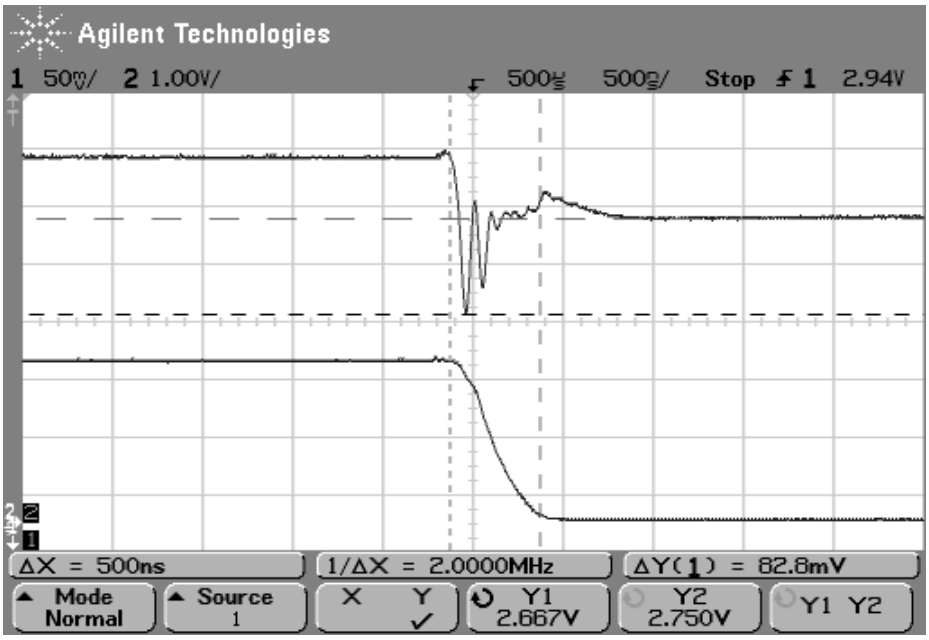


(a)

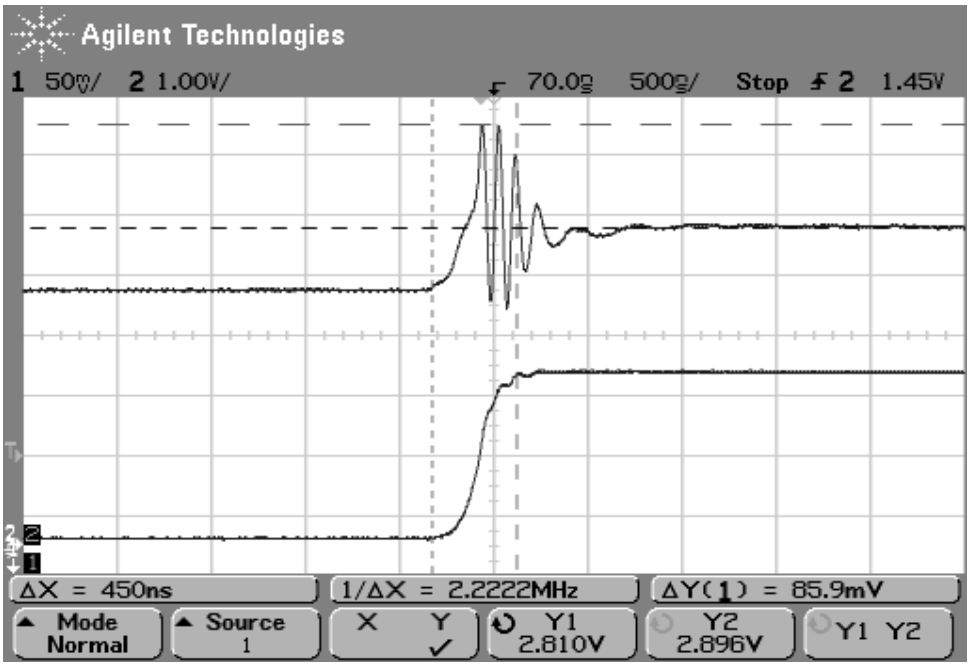


(b)

Fig. 6.4. Load Transient with no C_{out}. (a) 100µ A to 50mA (b) 50mA to100µA



(a)



(b)

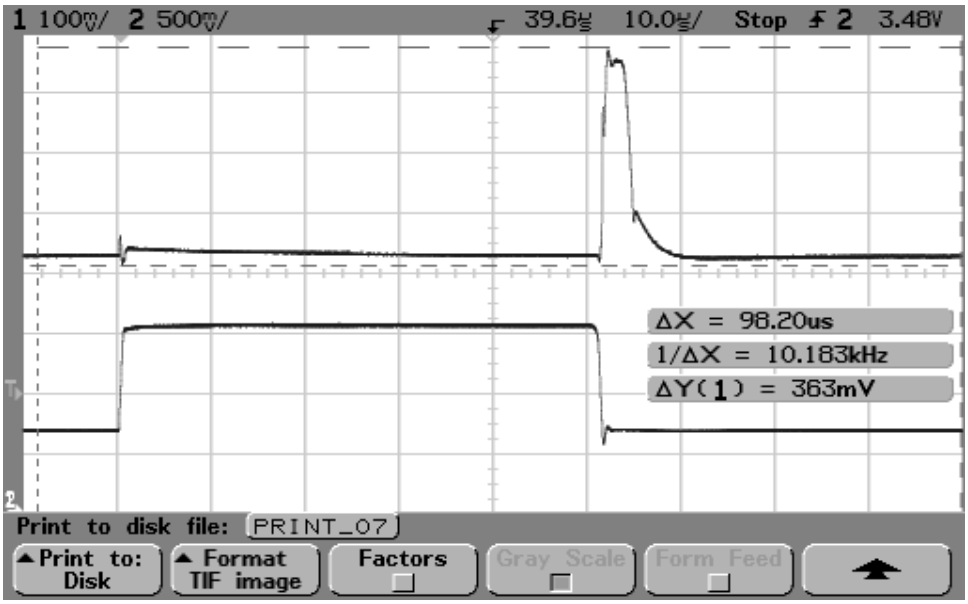
Fig. 6.5. Load Transient with C_{out} = 100pF. (a) 100µ A to 50mA (b) 50mA to100µA

6.2.2. Line Transient Response

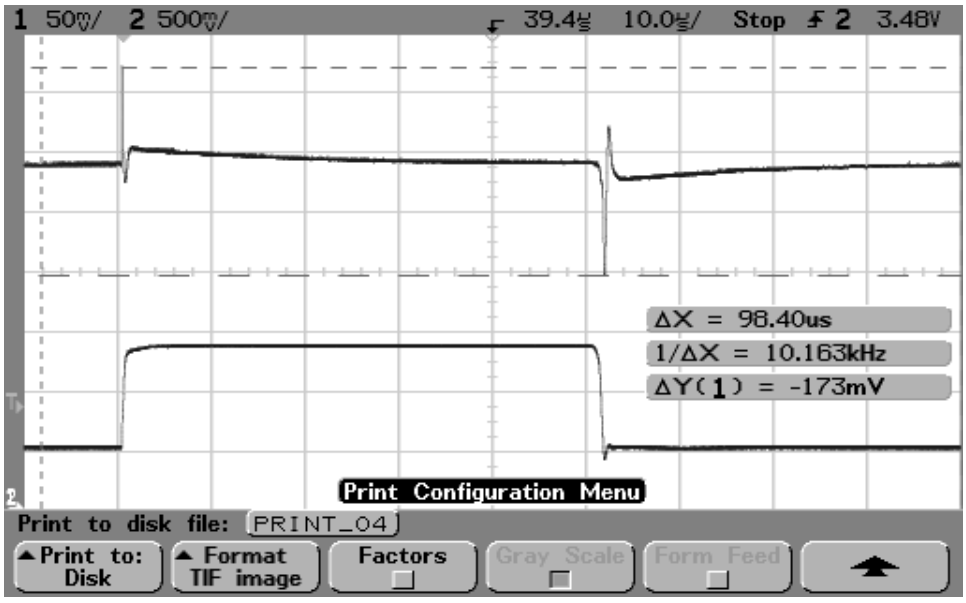
The function generator used can't supply 50mA of DC current. Thus the waveform is applied to a buffer connected in unity gain feedback which can supply the load current and act as the supply for the LDO. The setup is made in such a way that the supply voltage for the LDO switches between 3.1V and 4V. The results are shown in Fig. 6.6a and Fig. 6.6b with $C_{out} = 100pF$ connected at the output for 100µA and 50mA load currents respectively. The channel 1 represents the V_{out} and channel 2 shows V_{in}.

6.3. PSR Measurement

PSR can be measured by applying a tone in the supply V_{in} and measure the same tone at the output V_{out}. Difference between the power of the tones at V_{out} and V_{in} gives the required PSR for that tone frequency. T-bias has been used to couple the DC and AC (sine wave from function generator) and supply the V_{in} for the LDO. Spectrum analyzer with 1MΩ input impedance can be used to measure the power of the tones. The PSR measurement results for 100µA and 50mA load currents are shown in Fig. 6.7. The measurement shows 250kHz degradation in the PSR BW for -30dB rejection at full load condition compared to the schematic simulations.



(a)



(b)

Fig. 6.6. Line Transient for (a) $I_{LOAD} = 100\mu A$ (b) $I_{LOAD} = 50mA$

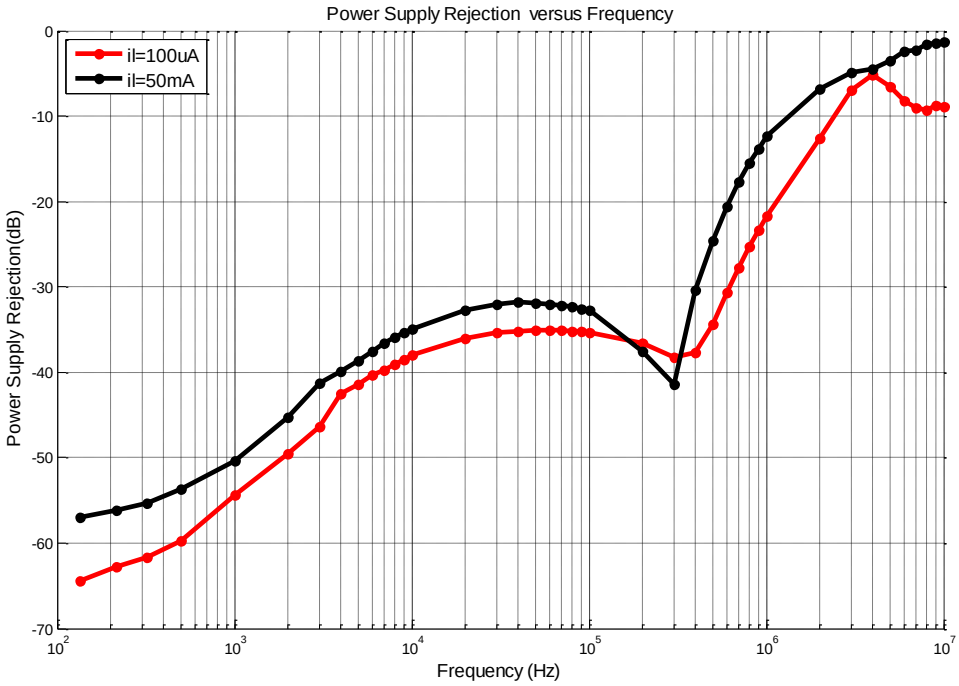


Fig. 6.7. PSR for $I_{LOAD} = 100\mu A$ and 50mA with $C_{out} = 100pF$

6.4. Comparison of Results

There have been many capacitor-less LDO topologies speaking about the compensation but not many speak about the PSR enhancement. The proposed LDO is compared with capacitor-less LDOs [4], [3], [9] and [10]. The comparison tabulated in Table XIX shows the significance of the proposed capacitor-less architecture. The experimental results imply that the proposed LDO has improved the transient response

(FOM) compared to [4] and [3] in a power efficient way and improved the PSR compared to [3], [9] and [10]. [4] shows better PSR but the maximum current capability of the LDO is just 5mA which is 10 times lesser than what the proposed LDO can deliver and more over the drop-out voltage of [4] is 600mV which result in about 25% power efficiency reduction. The figure of merit (FOM) reported in [3] has been used for comparison. The equation for FOM is shown in (54) in which C_M is any compensating capacitor used C_{out} and ΔV_{out} is the maximum of undershoot or overshoot voltage during load transients. FOM has been normalized with respect to [4] which has the lowest FOM. Higher the normalized FOM, better is the LDO's transient performance. [9] and [10] show higher normalized FOM compared to the proposed LDO but their minimum load currents for stability are in mA ranges which results in higher power dissipation during standby.

$$\mathrm{FOM} = \frac{[C_{out} + C_M] * \Delta V_{out}}{I_{LOAD,max}} * \frac{I_Q}{I_{LOAD,max}} \tag{54}$$

TABLE XIX

LDO COMPARISONS

Parameter	This Work		ISSCC'07 [4]	JSSC'05 [3]	JSSC'10 [9]	JSSC'10 [10]
V_{out} (V)	2.8	1.6	1.2	0.9	0.5	0.7
V_{DO} (V)	300m	200m	600m	300m	250m	250m
$I_{LOAD,max}$ (mA)	50	50	5	100	100	100
I_Q (µA)	120	80	70	6000	8	43
Power Efficiency (%)	90.1	88.7	65.75	85.2	66.67	73.65
Current Efficiency (%)	99.76	99.84	98.62	94.33	99.99	99.95
Load Transient ΔV_{out1} * (mV)	86	63	200	NA	114	~60
Load Transient ΔV_{out2} ** (mV)	83	105	737	90	77	~70
Settling Time T_S*** (µs)	0.7/0.8	4.8/5.1	NA	NA	NA	NA
Full Load PSR @ 135Hz (dB)	-57 @ 50mA	-77 @ 50mA	-70 @ 5mA	NA	-50 @ 100mA	NA
-30 dB PSR Frequency (Hz)	425k @ 50mA	826k @ 50mA	2M @ 5mA	NA	6k @ 100mA	NA
Load Regulation (µV/mA)	890	7	NA	NA	100	400
On-chip Capacitance (pF)	21.7	10.84	60	0	7	6
C_{out} (pF)	0 to 100	0 to 30	10	600	0 to 50	0 to 1000
C_{out} on-chip	No	No	Yes	Yes	No	No
Normalized FOM	286.8	1082.7	1	4.5	27702	4513
Area (mm^2)	0.359	0.081	NA	0.098	0.019	0.155
Technology (µm)	0.6	0.18^{++}	0.6	0.09	0.09	0.35

*Overshoot for a load step from $I_{LOAD,max}$ to $I_{LOAD,min}$
** Undershoot for a load step from $I_{LOAD,min}$ to $I_{LOAD,max}$
*** Settling time with 1% error during a load current step from $I_{LOAD,min}$ to $I_{LOAD,max}$ / $I_{LOAD,max}$ to $I_{LOAD,min}$
++ Worst-case post-layout simulations

7. CONCLUSION

A novel architecture has been proposed for the capacitor-less LDO which improves both the PSR at higher frequencies and transient response without the dependence on the output capacitor. This architecture delivers 50mA of maximum load current with 90% of power efficiency. The total quiescent current is 120µA (80µA) at full load current which scales to a current efficiency of about 99.76% (99.84%) at maximum load condition in 0.5µm (0.18µm) design. The minimum load current (100µA/150µA) which the proposed LDO (0.5µm/0.18µm) can handle satisfies the standby current in most of the cell phone applications. The proposed architecture designed using 0.5µm (0.18µm) technology regulates the output voltage at 2.8V (1.6V) from a minimum supply of 3.1V (1.8V), delivering current up to 50mA to the load. The load transient response has been improved resulting in undershoots and overshoots under 86mV (102mV) using 0.5µm (0.18µm) design.

The proposed capacitor-less regulator topology uses a modified unity gain buffer which helps stability compensation along with the Miller capacitor and also shapes the PSR at higher frequencies. The proposed LDO using 0.5µm (0.18µm) achieves PSR better than -30dB till 425kHz (826kHz) . R_Z used in the feedback of the buffer can be made tunable with trim bits so that PSR can be shaped according to the different applications. The experimental results also follow the stability and PSR analysis which have been carried.

The frequency for which the PSR is enhanced can be increased if more power is burnt in the buffer stage, so that stability can also be achieved. Hence by increasing the

power in the buffer stage, the minimum load current for which the stability is achieved can be relaxed further below 150µA.

On-Semi 0.5µm and TSMC 0.18µm CMOS technologies through MOSIS educational service has been used to design and fabricate the proposed capacitor-less LDO. The experimental results of this work in On-Semi 0.5µm and worst-case post-layout simulations of TSMC 0.18µm have been compared with other capacitor-less works [4] and [3] as illustrated in Table XIX. Thus a power, area and cost efficient off-chip capacitor free LDO has been proposed for the SoC applications with PSR enhancement.

REFERENCES

[1] T. Szepesi, K. Shum, Feb. 20, 2010, "Cell Phone Power Management Requires Small Regulators with Fast Response: News & Analysis: eetimes.com," http://www.eetimes.com/electronics-news/4164128/Cell-phone-power-management-requires-small-regulators-with-fast-response

[2] R.J. Milliken, J. Silva-Martinez, E. Sanchez-Sinencio, " Full on-chip CMOS Low-Dropout Voltage Regulator," *IEEE Trans. Circuits Syst. I*, Reg. Papers, vol. 54, no. 9, pp. 1879–1890, Sep. 2007.

[3] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-Efficient Linear Regulator with Ultra-Fast Load Regulation," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 933-940, Apr. 2005.

[4] V. Gupta, G. A. Rincon-Mora, "A 5mA 0.6um CMOS Miller-Compensated LDO Regulator with -27dB Worst-Case Power-Supply Rejection Using 60pF of On-Chip Capacitance," *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 520-521.

[5] M. El-Nozahi, A. Amer, J. Torres, K. Entesari, E. Sanchez-Sinencio, "High PSR Low Drop-Out Regulator with Feed Forward Ripple Cancellation Technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 565-577, Mar. 2010.

[6] V. Gupta, G. A. Rincon-mora, P. Raha, "Analysis and Design of Monolithic, High PSR, Linear Regulators for SoC Applications," in *Proc. of IEEE Int. SOC Conf,* Sept. 2004, pp. 311 – 315.

[7] V. Gupta and G. Rincon-Mora, “A Low Dropout, CMOS Regulator with High PSR over Wideband Frequencies,” *IEEE Int. Symp. Circuits and Systems (ISCAS),* vol. 5, May 2005, pp. 4245 - 4248.

[8] W. Oh, B. Bakkaloglu, B. Aravind, S. K. Hoon, “ A Low 1/f Noise CMOS Low-Dropout Regulator with Current-Mode Feedback Buffer Amplifier,” in *IEEE Custom Integrated Circuits Conf. (CICC)*, Sept. 2006, pp. 213-216.

[9] J. Guo and K. N. Leung, “A 6-μ W Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology,” *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1896-1905, Sep. 2010.

[10] P. Y. Or and K. N. Leung, “An Output-Capacitorless Low-Dropout Regulator with Direct Voltage-Spike Detection,” *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 458–466, Feb. 2010.

[11] S.K. Hoon, S. Chen, F. Maloberti, J. Chen, B. Aravind, “A Low Noise, High Power Supply Rejection Low Dropout Regulator for Wireless System-on-chip Applications,” in *Proc. of IEEE Custom Integrated Circuits Conf. (CICC),* Sept. 2005, pp. 759 - 762.

[12] E. Alon, J. Kim, S. Pamarti, K. Chang, M. Horowitz , “Replica Compensated Linear Regulators for Supply-Regulated Phase-Locked Loops,” *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 413-424, Feb. 2006.

[13] Xiaohua Fan, C. Mishra and E. Sánchez-Sinencio, “Single Miller Capacitor Frequency Compensation Technique for Low-Power Multistage Amplifiers,” *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 584-592, Mar. 2005.

[14] E. N. Y. Ho and P. K. T. Mok, "A Capacitor-Less CMOS Active Feedback Low-Dropout Regulator with Slew-Rate Enhancement for Portable On-Chip Application," *IEEE Trans. Circuits Syst. II*, Exp. Briefs, vol. 57, no. 2, Feb. 2010.

[15] T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok, and M. Chan, "Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC," *IEEE Trans. Circuits Syst. I*, Reg. Papers, vol. 55, no. 5, pp. 1392–1401, Jun. 2008.

[16] S. Heng, Cong-Kha Pham, "A Low-Power High-PSRR Low-Dropout Regulator with Bulk-Gate Controlled Circuit," *IEEE Trans. Circuits Syst. II*, Exp. Briefs, vol. 57, no. 4, Apr. 2010.

[17] M. Ho, K. N. Leung, L. K. Mak, "A Low-Power Fast-Transient 90-nm Low-Dropout Regulator with Multiple Small-Gain Stages," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, Nov. 2010.

[18] K. N. Leung, Y. S. Ng, "A CMOS Low-Dropout Regulator with a Momentarily Current-Boosting Voltage Buffer," *IEEE Trans. Circuits Syst. I*, Reg. Papers, vol. 57, no. 9, pp. 2312–2319, Sep. 2010.

[19] S. Yeung, J. Guo, K.N. Leung , "25 mA LDO with -63 dB PSRR at 30 MHz for WiMAX," Electronics Letters , vol.46, no.15, pp.1080-1081, July 22 2010.

VITA

Name:	Seenu Gopalraju
Address:	Texas A&M Department of Electrical Engineering, 214 Zachry, TAMU, College Station, TX 77843-3128
Email Address:	seenugece@gmail.com
Education:	B.E., Electronics and Communication Engineering, College of Engineering, Guindy, Anna University, Chennai- 600025, India, April 2007
	Master of Science, Electrical Engineering, Texas A&M University, College Station, TX 77843, December 2010