CASE STUDIES ON VARIATION TOLERANT AND LOW POWER DESIGN USING PLANAR ASYMMETRIC DOUBLE GATE TRANSISTOR

A Thesis

by

AMRINDER SINGH

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2010

Major Subject: Computer Engineering

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Approved by:

Chair of Committee,	Jiang Hu
Committee Members,	Xing Cheng
	Donald K. Friesen
Head of Department,	Costas N. Georghiades

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ABSTRACT

Case Studies on Variation Tolerant and Low Power Design Using Planar Asymmetric Double Gate Transistor. (August 2010)

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Chair of Advisory Committee: Dr. Jiang Hu

In nanometer technologies, process variation control and low power have emerged as the first order design goal after high performance. Process variations cause high variability in performance and power consumption of an IC, which affects the overall yield. Short channel effects (SCEs) deteriorate the MOSFET performance and lead to higher leakage power. Double gate devices suppress SCEs and are potential candidates for replacing Bulk technology in nanometer nodes. Threshold voltage control in planar asymmetric double gate transistor (IGFET) using a fourth terminal provides an effective means of combating process variations and low power design. In this thesis, using various case studies, we analyzed the suitability of IGFET for variation control and low power design. We also performed an extensive comparison between IGFET and Bulk for reducing variability, improving yield and leakage power reduction using power gating. We also proposed a new circuit topology for IGFET, which on average shows 33.8% lower leakage and 34.9% lower area at the cost of 2.8% increase in total active mode power, for basic logic gates. Finally, we showed a technique for reducing leakage of minimum sized devices designed using new circuit topology for IGFET.

To those who know how to convert adversity into opportunity

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CHAPTER I

INTRODUCTION

CMOS device scaling has been one of the major driving forces behind high performance and very high density integrated circuits. However, to maintain the same pace in nanometer technologies, process variation control and low power design have emerged as formidable challenges.

Device scaling increases the process variations leading to variations in threshold voltage, channel length and other circuit parameters. The variations in process parameters are induced due to the imperfections associated with the fabrication process. Factors such as random dopant fluctuations, line edge roughness and imperfections due to sub-wavelength lithography cause large variations in device circuit parameters [1]. According to ITRS [2], variation in V_{th} due to random dopant fluctuations for 45nm Bulk CMOS technology could be as high as 40%. Threshold voltage is an important circuit parameter which determines the operating speed and leakage power associated with individual transistors in the design. Process variations can be broadly classified into die-to-die (D2D) variations, within-die variations, wafer-to-wafer and lot-to-lot variations. For high performance ICs, D2D and within-die variations significantly impact the performance and power consumption [3]. Process variations lead to large variation in the operating frequency and leakage power consumption of an IC. After fabrication, each die must meet frequency and the maximum power consumption requirement. Dies operating at low frequency cannot be accepted and contribute to yield loss. Moreover, the power budget of an IC is fixed which puts constraint on the maximum allowed leakage power for a die, at its frequency of operation. This die must be either accepted at lower frequency, or discarded if the leakage power limit

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is exceeded.

Active power can be reduced by lowering the supply voltage but in order to maintain the same performance, the threshold voltage (V_{th}) is also scaled proportionally. Subthreshold leakage current of a transistor has exponential dependence on V_{th} which results in higher leakage.

In nanometer technologies, SCEs further aggravate the problem of leakage power. SCEs are secondary effects which come into picture when physical dimensions of transistor reach nanometer regime. In short channel devices, V_{th} decreases with reduction in channel length. This phenomenon is also known as V_{th} roll-off. It can lead to significant increase in leakage power. Drain induced barrier lowering (DIBL) is another phenomenon which reduces the V_{th} of the transistors causing higher leakage. In DIBL, drain bias now partly takes the role of gate voltage and lowers the built-in potential at source-substrate junction [4]. DIBL reduces the gate control of the channel and the device is not able to completely shut-off. Thus, in nanometer technologies, the contribution of leakage power to the total power of an IC is significant. This is a matter of concern for portable devices which spend a large amount of their time in the standby mode. Thus, it is crucial to reduce the leakage power for extended battery life.

In recent years, various techniques have been developed to counter the impact of process variations. The impact of process variations can be significantly reduced by adaptive circuit design for variation control. Body biasing can be used to dynamically modify V_{th} of a transistor. Reverse body biasing (RBB) increases the V_{th} of a device which reduces the leakage power. Similarly, forward body biasing (FBB) reduces V_{th} of a transistor which improves the transistor performance and thus can be used to increase the operating frequency of a design but at the cost of higher leakage power. Bidirectional adaptive body biasing (ABB) [5] makes use of both RBB and FBB on the same chip. Post-silicon tuning using body biasing can also be used to improve yield by increasing the number of dies which

satisfy the frequency and power constraints.

Adaptive supply voltage (ASV) [3] can be used as well for variation control by improving performance at the cost of power and vice versa. ABB and ASV can also be applied simultaneously for variation control [3]. Adaptive MTCMOS [6] is another technique for active mode leakage and frequency control. Multiple footer devices are inserted between the ground and the virtual ground terminal of the circuit. The total width of the footer devices can be dynamically controlled using a feedback mechanism.

In order to minimize leakage power, various techniques have been developed. Use of multi V_{th} devices [7] is one such approach in which the gates lying on non-critical paths are replaced by high V_{th} devices, and gates which lie on critical path are implemented using low V_{th} devices. RBB can also be used for reducing leakage power in standby mode.

Power gating [8] is an attractive scheme to reduce leakage power in standby mode. In power gating, the design is partitioned into different islands. The islands which are not in use can have their power supply temporarily switched off in order to minimize leakage power. During normal operation, the power supply is driven to its nominal value. The logic is implemented using low V_{th} devices but the switches used to gate the power supply and/or ground terminal are implemented using high V_{th} devices. The switches used to gate power supply and ground are called header and footer respectively. During active mode, the switches conduct but current flowing through them leads to IR drop which reduces the effective supply voltage thus reducing the logic performance. The performance penalty can be reduced by using larger widths for header and footer devices which reduces the leakage savings at the cost of higher area penalty. The delay and area penalty can be reduced by using body biasing for header and footer devices. In this thesis, we will study the performance of power gating in IGFET based circuits and contrast with power gating in Bulk technology. We will also show a new technique for eliminating the delay penalty in power gated circuits.

At device level, leakage power can be controlled by reducing SCEs through process level techniques. DIBL can be reduced by using shallow junctions and pocket implants at source and drain junctions to reduce the depletion layer widths. DIBL can also be mitigated by use of thin gate oxide (to increase the influence of the gate on the channel) [9]. But, it will aggravate the problem of gate leakage and would lead to unreasonable power increase. SCEs can also be controlled by using heavy channel doping but it will result in the degradation of device performance due to mobility degradation, larger depletion capacitance and subthreshold slope. It is clear that using Bulk technology, scaling will be very difficult to sustain and it is time to look for alternative devices which perform better in nanometer regime and are scalable as well.

Recently, planar double gate devices [10] [4] [9] have been proposed which minimize SCEs due to very thin body and lightly doped channel. It also reduces the random dopant fluctuations in channel and mobility degradation due to columbic scattering. These devices also show better sub-threshold slope than Bulk CMOS due to effective control of SCEs. Little attention has been paid to study the performance of variation control and low power techniques like ABB, power gating in circuits implemented using planar double gate devices. In this thesis, using case studies we have shown that these devices not only suppress SCEs but are also very suitable for process variation control and low power design as compared to Bulk technology. Techniques like ABB for variation control, post-silicon tuning for yield enhancement and power gating for leakage power minimization show very good results as compared to Bulk technology which proves their suitability for variation tolerant and low power circuit design.

In Double gate FET (DGFET), the passive substrate is replaced by an actively biased gate known as back gate. The primary gate terminal is known as front gate and the channel can be modulated using front and/or back gate [10]. Figure I.1 shows a planar double gate device. It consists of a very thin body and a lightly doped channel which eliminates the

leakage paths that are not well controlled by the gate, the ones that are physically far from the gate [4]. As a result, DGFET minimizes the SCEs effectively and provides better performance than conventional Bulk devices in sub-micron designs. An additional advantage is the reduction in capacitive load by the elimination of both depletion and junction capacitances. All these reasons make DGFET superior as compared to Bulk and an obvious choice to reap the benefits of scaling.

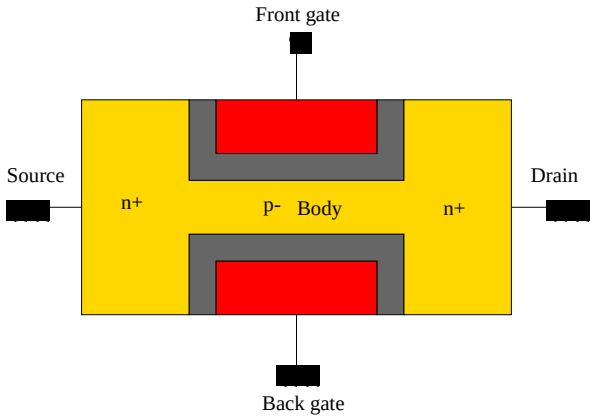

Fig. I.1. Planar double gate NFET

DGFETs can be broadly classified into two categories:

- *Symmetric*: In symmetrical DGFET, the front and the back gate are identical, having same oxide thickness and work function of the gate material. Symmetric DGFETs can be used as 3 terminal (3T) or 4 terminal (4T) devices [11]. In 3T mode, front gate and the back gate are connected together and provide better control of the channel by the gate. 3T DGFET can be directly used to replace conventional Bulk CMOS devices. In 4T mode, both the gates can be connected to different input signals and the device acts as two transistors in parallel. Such a structure is used to merge two parallel identical transistors which reduces area and power due to decrease in

diffusion capacitance. Another option is to use front gate only and the back gate can be connected to V_{dd} or V_{ss}. Due to less coupling between the front and back gates, the front gate V_{th} can't be modulated using back gate voltage.

- *Asymmetric*: Asymmetric DGFET (IGFET) consists of non-identical front and back gates. The back gate material has higher work function than front gate and thicker gate oxide [11]. IGFETs can be used like conventional Bulk CMOS devices. The back gate is used to modulate the V_{th} of the front channel by applying voltage across it. Back gate can also be connected to V_{dd} or V_{ss} like conventional CMOS in which case the V_{th} of the front channel is not affected. In this work, we will focus on asymmetric DGFET only.

In IGFET, the V_{th} of a device can be modulated using the back gate which can be used to control the circuit delay and leakage power. The ability to control V_{th} at transistor level (due to independent back gate terminal) and superior control of SCEs motivates us to study the performance of IGFET based circuits for variation control and low power design using various case studies. We will also show a new technique for eliminating delay penalty in power gated circuits. Finally, we will propose a new circuit topology for IGFET in which the front and back gates are connected to each other for leakage power and area benefits. We present thorough analysis to evaluate the trade-offs involved in the new circuit topology. The rest of the thesis is organized as follows. In Chapter II we discuss the previous work in this domain. In Chapter III we study V_{th} control in IGFET and Bulk. In Chapter IV we study the variation tolerance of IGFET and Bulk. In Chapter V we analyze the adaptability of IGFET and suitability of variation control using ABB technique in IGFET and Bulk. In Chapter VI we study yield enhancement using V_{th} control in IGFET and Bulk. In Chapter VII we compare the performance of power gating technique in IGFET and Bulk. We also propose a new technique for eliminating delay penalty in power gated

circuits. In Chapter VIII we present a novel circuit topology for IGFET based circuits. Finally, conclusion is presented in Chapter IX.

The key contributions of this thesis are:

- IGFET shows 3.8× lower σ for leakage power and 34% lower σ for delay than Bulk CMOS under process variations.
- We examine the use of V_{th} modulation for variation control and yield enhancement in IGFET. Results show that IGFET based circuits are highly adaptable and perform better than Bulk.
- We extend this study to power gated circuits. On average, IGFET shows 17× lower leakage in standby mode than Bulk CMOS.
- We also propose a new solution for eliminating delay penalty in power gated circuits. This method improves the leakage savings and lowers the area penalty.
- Finally, we propose a novel circuit topology for IGFET which on average shows 33.8% lower leakage and 34.9% lower area at the cost of 2.8% increase in total active mode power, for basic logic gates. Moreover, we showed a new technique for reducing leakage in minimum sized devices implemented using new circuit topology for IGFET.

CHAPTER II

PREVIOUS WORK

In [12], the authors propose the use of asymmetric, planar double gate FDSOI devices to control the front gate threshold voltage and to reduce the sensitivity of the threshold voltage to film thickness in FDSOI devices. They compare the threshold voltage, leakage current and drive currents for FDSOI and asymmetric, double gate FDSOI device.

The authors of [13] propose new double gate logic circuit schemes using only symmetrical gates to reduce the area and leakage/active power. The authors propose new circuit style for NAND and NOR logic gates. The parallel devices are implemented using split front gate and back gate devices while connected gate devices are used for stacked transistors.

In [14], authors evaluate the performance of connected gate and independent gate symmetric DGFET using benchmark circuits like NAND gate and ring oscillator. In connected gate, the front gate and back gate are shorted while in independent gate, the back gate is grounded for NMOS and connected to supply for PMOS device. The authors also design a VCO in which back gate voltage is used to control the VCO frequency.

In [11], the authors present various double gate devices including FinFET and discuss the various leakage mechanisms in symmetric and asymmetric DGFETs. Various circuit design techniques using 3T and 4T DGFETs are presented including Schmitt trigger and sense amplifier.

Similarly, in [15], the authors report various circuit design techniques specific to dynamic logic like keeper circuitry and precharge logic using independent gate DGFET. They also discuss a case study where they compare the performance of a tunable VCO designed using IGFET with Bulk CMOS.

All the previous work reported above only focuses on circuit design techniques using

3T and 4T *symmetric* double gate devices. Moreover, most of the analysis and comparison is based on standard logic gates and on circuits having very few gates. None of the previous works reported above focus on variation tolerance, variation control and yield enhancement of IGFET based circuits. In this thesis, we will extensively analyze suitability and adaptability of IGFET based circuits for variation control and yield improvement using case studies on complex benchmark circuits.

In [8], use of body biasing on power switches has been proposed for leakage minimization and lesser delay penalty. [16] discusses the use of high V_{th} footer and body biasing the footer device for delay penalty reduction in PDSOI based CMOS technology. We will examine the performance of IGFETs in power gated circuits and use of V_{th} modulation in logic instead of footer for delay penalty *elimination*.

CHAPTER III

V_{TH} CONTROL IN BULK AND IGFET

In Bulk CMOS devices, the body effect parameter γ plays a very important role in V_{th} control using FBB or RBB. However, with device scaling, the body effect parameter decreases which reduces the effectiveness of body biasing for dynamic V_{th} control. In IGFET, the back gate is strongly coupled to the front gate and can be used for threshold modulation. The back gate has very high threshold voltage as compared to the front gate. Unlike in Bulk CMOS, the V_{th} of IGFET does not depend on γ which provides effective V_{th} modulation even in nanometer technologies.

In Bulk CMOS, there is a fundamental limit to which the FBB can be applied due to the forward biasing of PN junction formed between drain, source junctions and substrate. The forward biasing of this PN junction leads to large current between drain, source junctions and substrate which significantly impacts the power. With scaling, the supply voltage also decreases and therefore further reduces the FBB range in Bulk CMOS devices. On the other hand, in IGFET, the back gate is isolated from the body through an oxide layer and the back gate can be used for FBB until the back surface becomes strongly inverted. Due to very high V_{th} of the back channel (about 1V higher than front channel), a large range of FBB can be supported in IGFET. RBB is used for sub-threshold leakage reduction in standby mode by increasing the V_{th} of the transistors. With scaling, RBB becomes less effective for Bulk due to higher SCEs in nanometer regime [17]. SCEs can be reduced in Bulk CMOS through the use of heavily doped substrate and halo implants but it increases the doping level near drain, source junctions which leads to increase in leakage due to band to band tunneling (BTBT) which reduces the leakage savings obtained by RBB. IGFETs minimize the SCEs due to lightly doped channel and very thin body. Therefore, the problem of BTBT in IGFETs is less pronounced as compared to Bulk CMOS and RBB using back

gate biasing can be effectively applied in nanometer IGFETs.

In this paper, all the experiments were conducted using 32nm process technology having V_{dd} = 1V. PTM [18] models were used for Bulk based circuit simulations while VerilogA based BSIM-IMG [19] models were used for IGFET. The NMOS and PMOS devices in both the technologies had comparable V_{th} and drive current around $V_{DS} = V_{GS} =$ 1V. Figure III.1 and III.2 show the plot of power-delay product versus NMOS body/back-gate bias for a FO4 inverter and a 51 stage ring oscillator designed using Bulk CMOS and IGFET for same area. The bias was used for both NMOS and PMOS. The curves are shown for extended range of FBB and RBB. From the plots it can be observed that for Bulk, after 0.5V, there is a sharp increase in the power-delay product due to forward biasing of the junction diodes which increases power significantly whereas for IGFET, the power-delay product increases sharply only after 1V (V_{dd}) due to inversion of the back channel but the slope of the curve is very less as compared to Bulk. With reverse bias, for FO4 inverter, the power-delay product is delay dominated and the slope of the curve for IGFET is comparable to that of Bulk and due to higher range of RBB, IGFET offers better delay control over Bulk. In ring oscillator, RBB increases the delay due to higher V_{th} and reduces power due to active mode leakage reduction. For Bulk, the percentage increase in delay is almost comparable to the percentage decrease in power due to which the curve remains relatively flat. However, for IGFET, the power savings are higher as compared to increase in delay due to which the power delay product decreases with RBB. Moreover, in both the cases above, the power-delay product curve for IGFET is always lower than Bulk suggesting low power and high performance design using IGFET.

Apart from this, there are various other reasons which make IGFET superior than Bulk CMOS. In stacked devices in Bulk CMOS, reverse body effect is observed which lowers the operating speed of wide input logic gates but in IGFET, reverse body effect does not occur because of the floating body [20]. In Bulk, all the devices share the same

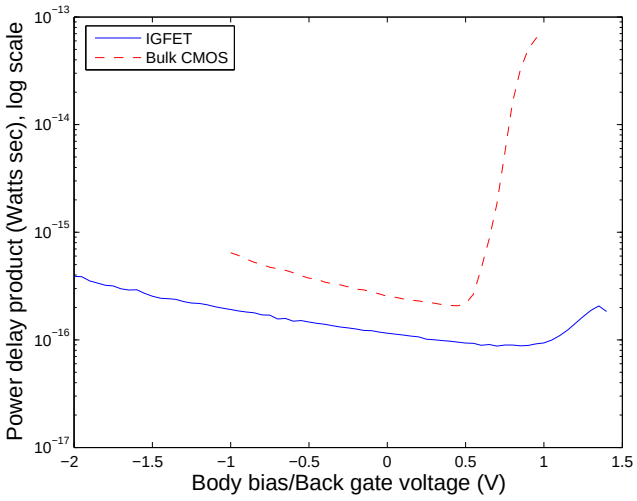

Fig. III.1. Power-delay product for FO4 inverter

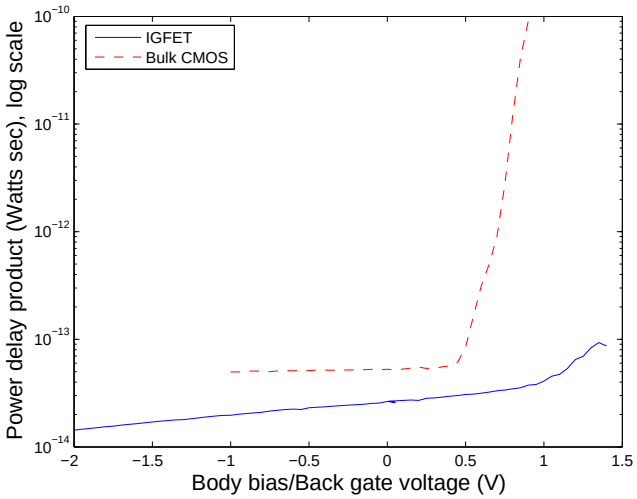

Fig. III.2. Power-delay product for 51 Stage ring oscillator

substrate due to which body biasing for *individual* transistors is highly impractical due to large area penalty. Whereas in IGFET, individual transistors can be controlled without any extra penalty. The frequency at which the substrate bias can be applied is limited by the RC delay of the substrate contacts whereas in IGFET, the maximum limit is imposed by the back gate capacitance and wire delay which is same as the main logic delay. Thus, leading to faster V_{th} modulation as compared to Bulk.

CHAPTER IV

VARIATION TOLERANCE

To compare the performance in the presence of process variations, we performed Monte Carlo (MC) simulations on an inverter chain circuit designed using Bulk and IGFET. In IGFET, the back gate of NMOS was tied to V_{ss} while for PMOS the back gate was tied to V_{dd}. The nominal value of supply voltage used was 1V. Based on ITRS predictions, parameter variations were induced in all the transistors of the circuit. The 3σ value of the parameter variations [2] is listed in Table IV.1.

Table IV.1. Parameter variations

Parameter	3σ (%)
Channel length	12
Gate oxide	10
Threshold voltage	40
Power supply	10

For a given MC run, same supply voltage was used for the combinational circuit. Thickness variation in the back gate oxide of IGFET was neglected due to its high thickness as compared to front gate. 1000 MC simulations were performed for Bulk and IGFET respectively.

For delay comparison, the circuits were designed to have delay of 1ns and identical inputs were applied. The plot in Figure IV.1 shows the histogram of delay distribution. The mean of the delay distribution is almost same for Bulk and IGEFT but for Bulk, σ is 67.9ps whereas IGFET shows σ of 44.6ps. The σ for Bulk is 52% higher than that of IGFET thus showing better variation tolerance in IGFET. Another experiment was performed to compare the variation in circuit leakage in idle mode under the effect of process variations. For a fair comparison, both the circuits were designed for same area and in idle mode, the inputs were tied to V_{ss}. Figure IV.2 shows the distribution of circuit leakage for Bulk

and IGFET. For IGFET, mean leakage is 2.81μw and σ is 0.27μw whereas for Bulk mean leakage is 6.64μw and σ observed is 1.05μw which is 3.8$\times$ that of IGFET.

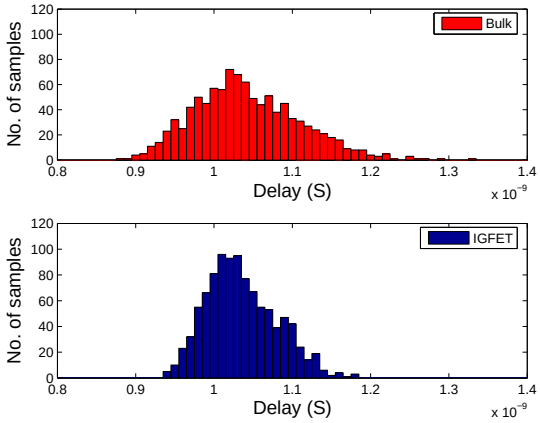

Fig. IV.1. Delay distribution histogram

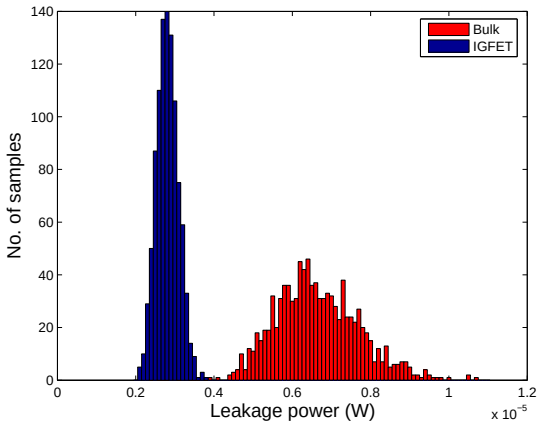

Fig. IV.2. Leakage distribution histogram

CHAPTER V

D2D VARIATION CONTROL THROUGH V_{TH} MODULATION

In chip design, the goal is to achieve highest frequency of operation while meeting the power constraints. But, process variations lead to distribution of die frequencies and leakages. ABB is an effective technique to meet the desired frequency and power constraints by dynamically modifying the V_{th} of the transistors. ABB trades off performance for power and vice-versa. Chips which do not meet the desired frequency require FBB for higher performance at the cost of higher leakage power. Whereas, chips which fail to meet the leakage constraint, need to be operated at lower frequency and RBB is used for leakage reduction.

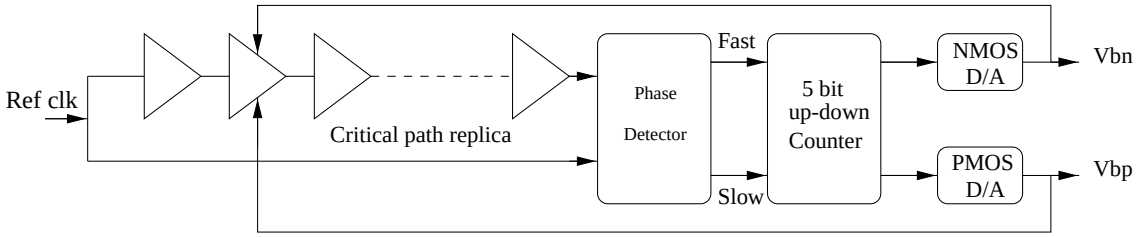

Fig. V.1. DLL using critical path replica for ABB

In order to compare the performance of Bulk and IGFET in variation control using bidirectional ABB, we implemented a critical path replica based delay locked loop (DLL) circuit [5]. The aim of the circuit is to minimize the leakage power while ensuring that the critical path meets timing. The circuit can also be used for leakage savings when the intended target frequency is lower than the maximum frequency like in dynamic frequency scaling based environment. The circuit is shown in Figure V.1. It consists of a critical path replica which is used to replicate the delay of the critical path in the circuit. Instead of replicating the critical path, the inputs and outputs of the critical path can also be used

directly but it is intrusive to the design. We created a critical path replica using a chain of buffers whose total delay is matched to the critical path delay of the circuit. Here, we assume that buffer chain can be effectively used for modeling the critical path. A phase detector is used to detect when the critical path replica is faster than the target frequency and vice-versa. The output of the phase detector is connected to a 5 bit up-down counter which digitally records the phase difference between input reference clock signal and output of the critical path replica. The counter increments or decrements dynamically. The output of the up-down counter is connected to digital to analog (D2A) converter which creates the body bias for NMOS and PMOS devices in the circuit and the critical path replica. For simplicity we have used only one up-down counter for NMOS and PMOS devices. One D2A converter is used for NMOS and PMOS respectively.

The DLL circuit was implemented in 32nm technology for target frequency of 1GHz. The critical path replica was designed to match delay of 1ns. In order to simulate the corner case, we induced 3σ variation (obtained from MC simulations) in the circuit corresponding to the worst case delay for Bulk and IGFET. For a fair comparison, same body bias range was used for Bulk and IGFET. The body bias range of +320mV for FBB to -320mV for RBB in 20mV steps was used. SPICE simulations were run to determine the locking behavior of the DLL for Bulk and IGFET.

Figure V.2 shows the plot of frequency vs. time units and PMOS body/back gate bias voltage vs. time units, for Bulk and IGFET (worst case). Due to better variation tolerance, under 3σ variations, IGFET operates at a higher frequency than Bulk when no bias is applied. The bias changes with time and the frequency rises towards the target frequency. The body/back gate bias curves for Bulk and IGFET almost overlap. The DLL locks within range of 10ps of the target clock period. From the curves it can be seen that Bulk and IGFET lock when the body bias reaches the maximum value. The locking time is also almost same for both the technologies suggesting effectiveness of adaptively modulating V_{th} in

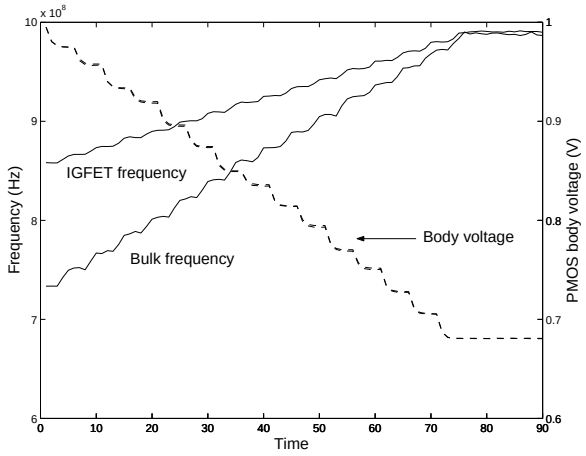

Fig. V.2. DLL operation

IGFET based circuits. The locking time for IGFET can be further reduced by increasing the maximum bias range. Similar experiments were done for best case delay variation as well and similar results were obtained but they have been omitted here for brevity.

CHAPTER VI

ENHANCING YIELD USING V_{TH} MODULATION

After fabrication, each chip should meet minimum frequency and maximum power constraints. But, process variations can lead to significant yield loss due to significant deviation in circuit delay and power from the intended target. The chips which operate at low frequency or consume excessive power contribute to yield loss. A die which violates the power constraint can be accepted at low frequency or it might be discarded if the leakage power is excessive. Post-silicon tuning using body biasing is effective for tightening the delay and power distribution for improving yield. In this section we compare the effectiveness of post-silicon tuning using body biasing for yield enhancement in Bulk and IGFET.

We implemented a combinational circuit having same area for Bulk and IGFET. For a fair comparison, the maximum and minimum body bias range of +320mV and -320mV was used for both. MC simulations were done using the parameter values listed in Table IV.1. The resulting device parameters were used to simulate the effect of process variations. Different samples (from MC simulations) have different delay and power. Samples which violate the maximum delay or maximum power constraint are compensated for delay and power using body biasing. For a violating sample, multiple SPICE simulations are done to find the optimum bias voltage. Due to high runtime requirements we performed this experiment on a set of 700 samples only.

Figure VI.1 shows the power-delay scatter plot for the combinational circuit implemented using Bulk technology. The delay and power numbers shown are normalized with maximum delay and power constraint. A large number of samples violate the delay or power constraints. After compensation, the sample which violates delay constraint is now accepted at higher power but within the maximum limit. Similarly, the samples which violate power constraint are accepted at higher delay but within maximum delay constraint.

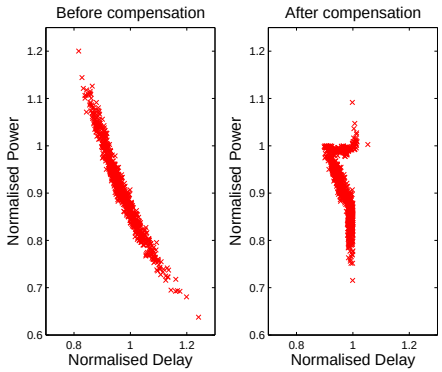

Fig. VI.1. Scatter plot for Bulk

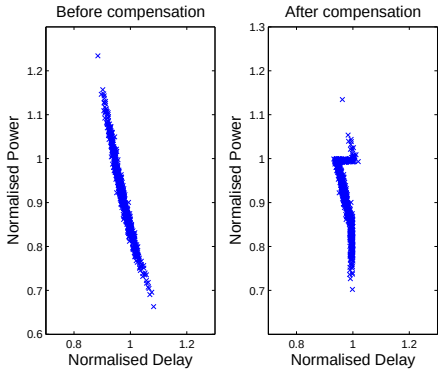

Fig. VI.2. Scatter plot for IGFET

A small number of samples are still not able to meet the delay and power constraint and contribute to yield loss. Figure VI.2 shows the scatter plot for IGFET based circuit and results after compensation for delay and power. A comparison of results after compensation for Bulk and IGFET reveals that IGFETs result in a tighter distribution than Bulk. In fact, better results can be obtained for IGFET by increasing the range of back gate bias which is not possible in Bulk due to reasons explained earlier.

CHAPTER VII

POWER GATING IN BULK AND IGFET

Power gating is an effective technique for leakage power reduction in sleep mode but it has a performance penalty associated with it. High V_{th} switches are used for power supply gating whereas the logic is implemented using low V_{th} devices. A PMOS or NMOS device can be used for power gating but NMOS is preferred due to lower area penalty. Figure VII.1 shows the block diagram of a power gated circuit.

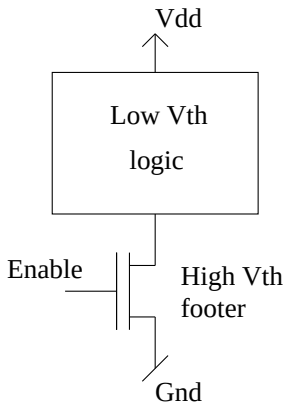

Fig. VII.1. Power gated circuit

In power gated circuits, due to the finite voltage drop across the footer, the virtual ground line bounces above ground potential. Ground bounce reduces the effective gate-to-source drive voltage which reduces the switching speed and hence the maximum operating frequency of the circuit. In Bulk devices, ground bounce also manifests as rise in V_{th} of the NMOS devices due to finite source-to-substrate voltage. This further lowers the operating speed whereas in IGFET, body effect is not present leading to faster operation in power gated circuits. Moreover, in Bulk devices, due to finite diffusion capacitance the capacitance associated with the virtual ground node is quite high if a common footer is used for all the logic gates which further reduces the switching speed but IGFET does not have

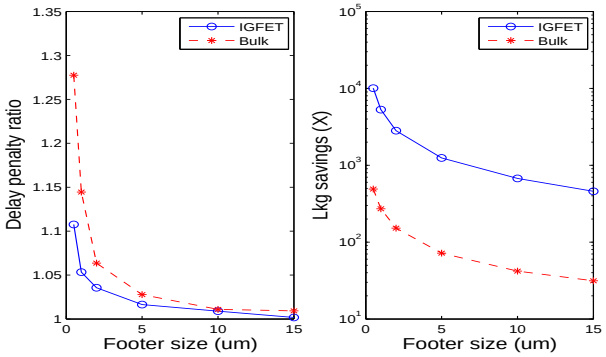

Fig. VII.2. Delay penalty and leakage savings comparison

diffusion parasitic capacitance. The delay penalty due to power gating can be reduced by using wider footer devices but it amounts to area penalty and most importantly diminishing returns on leakage power savings in sleep mode.

To analyze the delay, area penalty and sleep mode leakage savings in the two competing technologies, we implemented power gating in ISCAS85 benchmark circuit C432 having 150 logic gates. Single high V_{th} footer device was used for the entire circuit. The circuit was designed for same area. The left part of Figure VII.2 shows the change in delay penalty with the change in footer size. The delay penalty for IGFET is always lesser than Bulk and for small footer size, delay penalty is quite high for Bulk as compared to IGFET. The right part of Figure VII.2 shows the ratio of circuit leakage in sleep mode without power gating and leakage in sleep mode with power gating using different footer size. For IGFET, on average the leakage savings in sleep mode are 17$\times$ higher than Bulk. In sleep mode, the virtual ground terminal floats and slowly charges to V_{dd}. Due to lower DIBL effect, IGFET shows higher leakage savings.

The delay penalty due to power gating can be reduced by lowering the V_{th} of the high V_{th} footer device in active mode by FBB [8] [16]. For circuit C432, use of FBB for footer device, reduced the delay penalty for Bulk by 3.6% whereas for IGFET only 2.4%

improvement in delay was observed. FBB on footer reduces its resistance which in turn reduces the virtual ground bounce. The reduction in bounce improves the voltage drive and also reduces the negative effect of increasing the V_{th} of the Bulk NMOS devices. Due to this, Bulk shows better delay improvement with FBB on footer device. The delay penalty can be *reduced* by forward biasing the footer but cannot be *eliminated*.

Table VII.1. Using FBB in power gated circuit

Body bias (V)	Bulk dly (ps)	IGFET dly (ps)	Bulk pwr (μw)	IGFET pwr (μw)
0.00	405.3	238.3	112	82.1
0.05	391.2	237.5	113	84.3
0.10	378.2	234.0	116	86.4
0.15	366.3	229.8	118	87.7
0.20	353.8	225.0	120	89.5
0.25	343.9	221.2	122	91.3

We propose the use of applying FBB on the logic gates instead of footer in the active mode of operation. Table VII.1 shows the results of applying FBB on the logic gates (rather than footer) in benchmark circuit C432 for reducing delay penalty. Column I shows body bias voltage. Columns II and III show the delay of a path for Bulk and IGFET circuit having same area. Columns IV and V show the total power for Bulk and IGFET in active mode. Footer size of 1 μm was used for both the circuits. Without power gating the same path has a delay of 346ps and 225ps for Bulk and IGFET respectively. The total power for Bulk is 143μw and 93.5μw for IGFET. From the table it can be seen that the delay penalty for Bulk reduces to zero at 0.25V while for IGFET there is no delay penalty at 0.2V. Even after FBB the total power in active mode is lesser than without power gating. The ground bounce associated with virtual ground manifests itself as reduced leakage power in active mode for power gated circuits. The positive virtual ground voltage results in negative gate-to-source voltage for off-state NMOS devices in the circuit, which leads to exponential decrease in sub-threshold leakage of those devices. The percentage reduction in leakage due to ground bounce depends on the activity factor of the circuit. Figure VII.2 for the same circuit shows

that without any bias, the delay penalty reaches 1% for footer size of 10μm. Bigger footer device leads to higher dynamic power in active mode and lesser leakage savings. Thus, use of FBB on logic gates in power gated circuits *eliminates* delay penalty, reduces total active mode power (compared to non power gated case) and improves leakage power savings in sleep mode. The bias voltage can also be adaptively controlled using DLL based circuit. The area penalty of implementing body biasing in Bulk CMOS is high due to the use of triple well process but in IGFET the area overhead is limited by the additional routing resources required to connect the back gate of the devices on which FBB is applied.

CHAPTER VIII

TIED GATES TOPOLOGY FOR IGFET

Here, we propose a new circuit topology for IGFET which provides significant leakage and area savings at the cost of minimal increase in total active mode power. In IGFET, the channel associated with the back gate does not conduct due to very high threshold voltage but it can be used to vary the V_{th} of the front gate channel. In this novel circuit style, we connect the front gate and back gate of the IGFET device. This will modulate the V_{th} of the device depending on the input signal during the active mode operation. For NMOS, V_{th} can be reduced by applying a positive voltage on the back gate whereas for PMOS, positive voltage lower than Vdd is required.

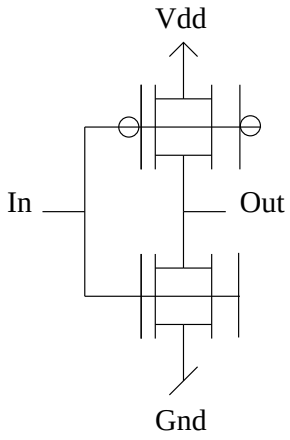

Fig. VIII.1. Inverter using tied gate IGFET

Figure VIII.1 shows an inverter implemented using tied gate IGFET. Consider a rising input at the input of the inverter, the output will have a corresponding falling transition. When the input is rising, the voltage at the back gate of the NMOS device will be higher than 0 which will modulate the V_{th} due to forward biasing thus reducing the propagation delay. Similarly for a falling input transition, the FBB on PMOS device reduces the prop-

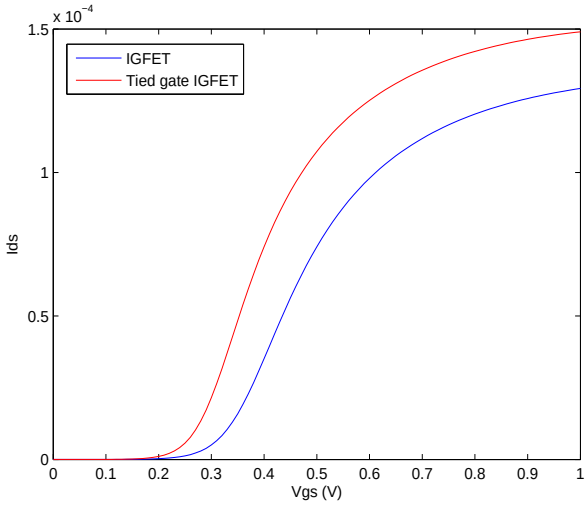

Fig. VIII.2. Ids vs. Vgs curve for NMOS, Vds=50mv

agation delay. It is interesting to note that for static inputs, the leakage of the logic gate is not affected. Consider an inverter having logic 0 as input. The leakage of the inverter is determined by the NMOS device. Since, the back gate is also connected to 0 in this case, the V_{th} of the NMOS device is not affected and it incurs no additional leakage penalty. Similar case holds for static input 1.

Figure VIII.2 shows the NMOS, Ids vs. Vgs curves for tied gate IGFET and basic IGFET. Vds=50mV was used for these curves. The results show that the linear region V_{th} of tied gate IGFET is around 95mV lower than basic IGFET.

We implemented an inverter and a 2 input nand gate using tied gate IGFET and basic IGFET. Table VIII.1 shows the results. T1 refers to the minimum size logic gate with back gate tied to V_{ss} for NMOS and tied to V_{dd} for PMOS. T2 refers to the same logic gate but implemented using tied gate IGFET. T3 refers to T1 upsized to match the same delay as T2. In Table VIII.1, Column I shows the type of logic gate. Column II shows average propagation delay and Column III shows average leakage power in standby mode. Column IV shows total power in active mode and Column V shows the ratio of total device width

to minimum device width.

For inverter (T2) there is a gain of 25.9% in delay over T1 and average gain of 35.2% in leakage over T3. For nand gate (T2), delay is 27.8% lower than T1 and average gain in leakage over T3 is 32.5%. Tied gates topology provides area savings of 37.8% for inverter and 32% for nand. But, the total power for T2 is 2.3% higher for inverter and 3.4% higher for nand gate. The total active mode power depends on the gate capacitance switched and the short circuit current. $T2_{inv}$ and $T2_{nand}$ have smaller area than $T3_{inv}$ and $T3_{nand}$ which means lower gate capacitance. But, the short circuit current increases due to dynamic V_{th} lowering. These logic gates provide leakage and area savings which is a significant advantage.

Table VIII.1. Tied gate topology for Inv and Nand

Logic gate	Avg dly (ps)	Avg lkg (nw)	Tot. pwr (μw)	Tot. fet width / w_{min}
$T1_{inv}$	21.2	0.22	0.80	2.8
$T2_{inv}$	15.7	0.22	0.90	2.8
$T3_{inv}$	15.7	0.34	0.88	4.5
$T1_{nand}$	22.3	0.29	1.14	6.8
$T2_{nand}$	16.1	0.29	1.20	6.8
$T3_{nand}$	16.1	0.43	1.16	10.0

This topology cannot be used in Bulk CMOS as it will forward bias the junction diodes and the device operation will fail. In order to support this argument, we designed two minimum sized inverters using Bulk technology. The first one is conventional CMOS inverter and in the second one, gate is tied to substrate for NMOS and PMOS respectively. For the same load, first inverter shows an average propagation delay of 20.5ps while for the second inverter the propagation delay is 12.7ps. But, the active mode power for the first inverter is 0.9μw whereas the active mode power for the second inverter is 5.18mw which is very high. This explains the infeasibility of this technique for Bulk. In IGFET, the back gate is isolated using oxide which makes this technique very suitable for IGFET.

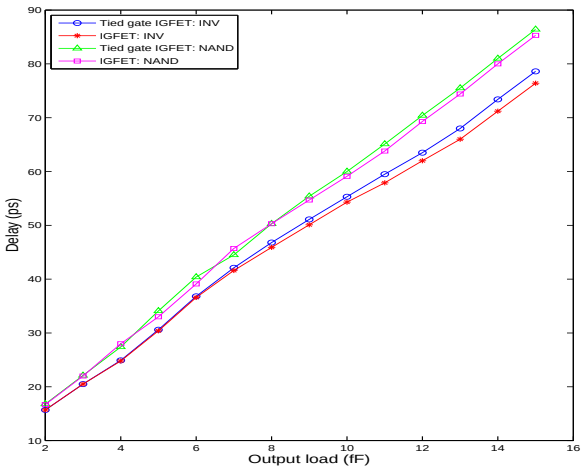

Fig. VIII.3. Delay vs. output load

VIII.1. Impact of output load and input slew rate

In this section, we analyze the impact of output load and input slew rate on the delay and power of logic gates implemented using tied gate IGEFT. We designed a minimum sized inverter and a 2 input nand gate using tied gate IGFET. We designed another inverter and nand gate but using normal IGFET such that their delay is identical to the gates implemented using tied gate IGFET, for same load and input slew rate. In the first experiment, we vary the output load only keeping input slew rate fixed and analyze the delay and power respectively.

Figure VIII.3 shows the delay vs. output load plot. For small values of load, the delay is same for gates implemented using tied gate IGFET and basic IGFET. For large values of load, the delay of tied gate IGFET is worse than IGFET by just 1-2ps. This plot shows the ability of tied gate topology to effectively drive large load. Figure VIII.4 shows the active mode power vs. output load plot for the same logic gates. The active mode power is mostly dominated by the output load hence all logic gates show almost similar power.

In the second experiment, we analyze the delay and power for these logic gates with

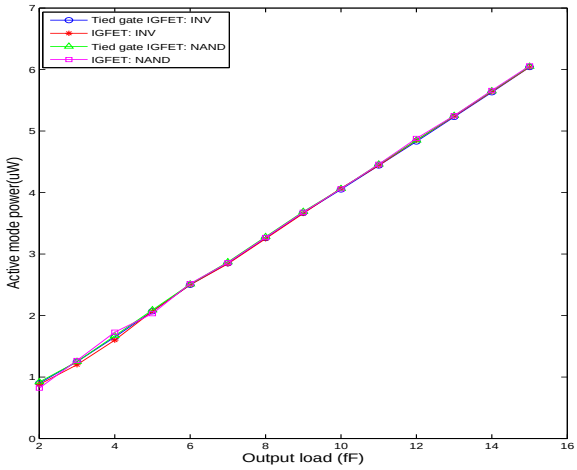

Fig. VIII.4. Active mode power vs. output load

change in input signal slew rate. Figure VIII.5 shows the plot for delay vs. input signal slew. For large values of input slew, logic gates implemented using tied gate IGFET show better delay than gates implemented using IGFET. The difference in delay becomes more prominent with further increase in the value of input slew. Figure VIII.6 shows the plot for active mode power vs. input slew. The plot shows that gates implemented using tied gate IGFET consume higher power than gates implemented using IGFET and the gap in power widens with increase in slew. The gates implemented using tied gate IGFET show better delay but worse power. In order to understand the behavior clearly, Figure VIII.7 shows the power delay product plotted against input slew for both the techniques.

The power delay product is higher for tied gate IGFET than IGFET. But, we saw that IGFET based logic gates have worse delay than tied gate IGFET for higher values of slew. In order to get same delay from IGFET based logic gate, bigger transistors will be required which will ultimately lead to higher active power, higher leakage and area. Whereas, tied gate IGFET based logic gates save leakage and area at the cost of small increase in active mode power.

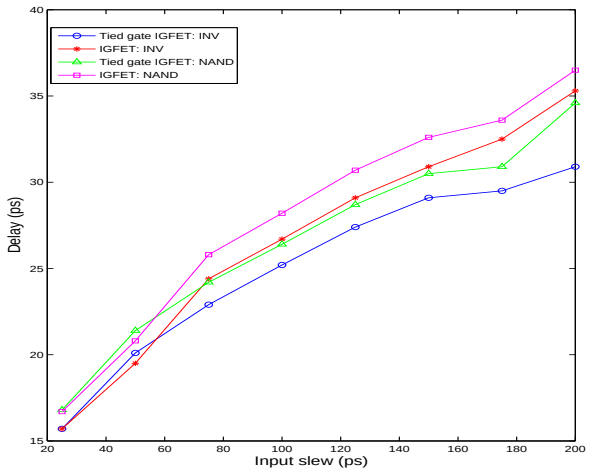

Fig. VIII.5. Delay vs. input slew

VIII.2. Impact of variation in gate oxide thickness

In this section, we study the impact of variation in gate oxide thickness on the delay performance of tied gate IGFET topology and IGFET. For this, we implemented a 51 stage inverter chain using minimum sized inverters for both the topologies. We introduced a 3σ variation of 10% in the front gate and back gate oxide thickness. For the inverter chain circuit designed using IGFET, variation was introduced in front gate oxide only whereas for the inverter chain circuit designed using tied gate IGFET, variation was introduced in front gate oxide and back gate oxide. 1000 MC simulations were done on inverter chain circuits designed for same area. For IGFET based circuit we observed mean delay of 299ps and σ of 3.6ps in delay. For tied gate IGFET based circuit, the mean delay is 247ps and σ of 4ps in delay is observed. The variation of oxide thickness for back gate does not impact the delay performance much due to thicker gate oxide whose thickness is around 5× the oxide thickness of the front gate.

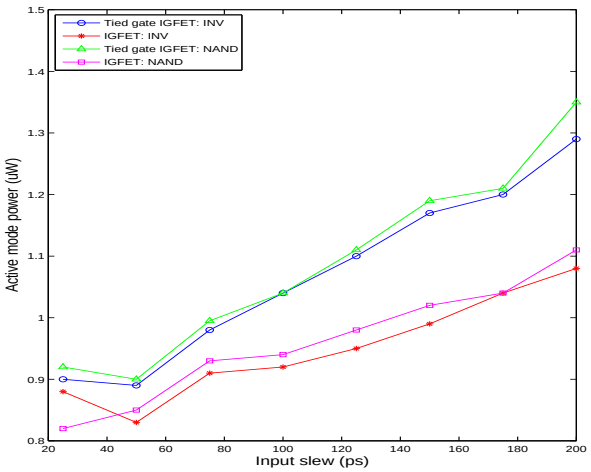

Fig. VIII.6. Active mode power vs. input slew

VIII.3. Leakage reduction using high Vth tied gate IGFET

Earlier, we showed that tied gate IGFET can be used for reducing area and leakage when designed for the same propagation delay as IGFET. In this section, we propose another technique to reduce leakage using tied gate IGFET. Consider a logic gate implemented using IGFET having delay $D1$, area A and leakage $L1$. Consider the same logic gate implemented using tied gate IGFET such that it has area A, delay $D2$ and leakage $L2$. In this case, $D2$ is lesser than $D1$ and $L2 = L1$. Since, $D2$ is lower than $D1$, we can achieve same delay as $D1$ but by increasing the V_{th} of the devices used in the logic gate.

Such a logic gate will have lower leakage. In active mode, the gate capacitance switched remains the same but the short circuit current might vary depending on the effective V_{th} of the devices and input signal slew. In order to quantify the leakage savings, we designed a minimum sized inverter and a 2 input nand gate as explained above. The results are shown in Table VIII.2. Column I shows the type of logic gate. Inv_{lvt} and $Nand_{lvt}$ refers to logic gates designed using low V_{th} devices. Inv_{hvt} and $Nand_{hvt}$ refer to the logic gates designed using high V_{th} devices. Column II shows the average propagation delay. Column

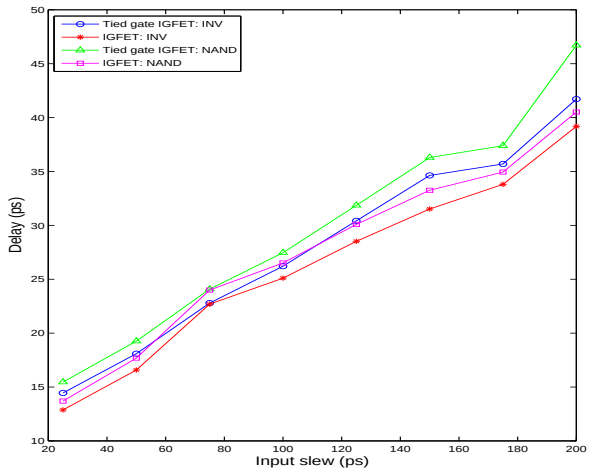

Fig. VIII.7. Power delay product vs. input slew

Table VIII.2. Hvt and Lvt gates designed using tied gate topology for Inv and Nand

Logic gate	Avg dly (ps)	Avg lkg (nw)	Tot. pwr (μw)
Inv_{lvt}	21.2	0.22	2.05
Inv_{hvt}	21.5	0.16	2.10
$Nand_{lvt}$	22.8	0.29	2.17
$Nand_{hvt}$	22.0	0.21	2.18

III shows average leakage in standby mode. Column IV shows total active mode power. Results show that Inv_{hvt} has 27.2% lower leakage than Inv_{lvt} for the same propagation delay but at the cost of 2.4% higher active mode power. Similarly, 2 input nand gate shows 27.5% lower leakage at the cost of 0.46% higher active mode power.

This technique is highly useful for minimum sized devices. For a given delay and area of a logic gate designed using IGFET, same delay can be achieved by using a smaller logic gate designed using tied gate IGFET. But, in minimum size devices, the size cannot be reduced further due to limitations on minimum device size which can be fabricated. An IC designed using standard cell based methodology contains a large number of minimum sized devices. For these logic gates, leakage can be substantially reduced by increasing the

V_{th} of the device while maintaining the same performance. Moreover, this technique can be used in memory arrays where due to area considerations the size of the bitcell devices is small. Use of high V_{th} devices impacts the performance but using tied gate IGFET based bitcell, same performance can be obtained while substantially lowering leakage.

Now, a question may arise that, how a tied gate IGFET based circuit compares with a circuit implemented using symmetric DGFET. A logic gate implemented using symmetric DGFET saves area by using a single device having two channels in place of two individual devices. It also reduces the dynamic power due to lower self loading but the total amount of leakage power of the logic gate remains the same. Whereas, logic gates implemented using tied gate IGFET saves area and leakage power as well. If both the gates of a symmetric DGFET are connected to each other, it lowers the propagation delay but it increases the dynamic power due to higher gate capacitance and the leakage power doubles. Whereas, in tied gate IGFET, the oxide thickness of back gate is around $5\times$ that of the front gate due to which the gate capacitance of the device does not get affected much and moreover the leakage in the standby mode remains completely unaffected.

CHAPTER IX

CONCLUSIONS

We have shown that planar asymmetric double gate transistors enable low power and high performance circuits in nanometer regime. IGFET provides better variation tolerance than Bulk and is highly suitable for variation control and yield enhancement using V_{th} modulation. Moreover, power gated circuits implemented using IGFET suffer from minimal delay, area penalty and we also showed how delay penalty can be completely eliminated while providing higher leakage savings. Finally, we proposed a tied gates topology for IGFET which provides very high leakage and area savings at the cost of minimal increase in total power.

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VITA

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Publications:

- A. Singh, K. Gulati and S. Khatri, "*Minimum Leakage Vector Computation using Weighted Partial MaxSAT*", 53rd IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Aug 1-4, 2010, Seattle, Washington.

- A. Singh, M. Handa, V. Pandey and M. Kathuria, "*Overcoming Verification Challenges for Low Power Implementation in SoCs*", 7th IDC, Freescale Technical Symposium, India, 2007.

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