A PLL DESIGN BASED ON A STANDING WAVE RESONANT OSCILLATOR

A Thesis

by

VINAY KARKALA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2010

Major Subject: Computer Engineering

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Approved by:

Chair of Committee,	Sunil P. Khatri
Committee Members,	Peng Li
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ABSTRACT

A PLL Design Based on a Standing Wave Resonant Oscillator. (August 2010)

Vinay Karkala, B. Tech., Indian Institute of Technology Madras, India

Chair of Advisory Committee: Dr. Sunil P. Khatri

In this thesis, we present a new continuously variable high frequency standing wave oscillator and demonstrate its use in generating the phase locked clock signal of a digital IC. The ring based standing wave resonant oscillator is implemented with a plurality of wires connected in a mobius configuration, with a cross coupled inverter pair connected across the wires. The oscillation frequency can be modulated by coarse and fine tuning. Coarse modification is achieved by altering the number of wires in the ring that participate in the oscillation, by driving a digital word to a set of passgates which are connected to each wire in the ring. Fine tuning of the oscillation frequency is achieved by varying the body bias voltage of both the PMOS transistors in the cross coupled inverter pair which sustains the oscillations in the resonant ring. We validated our PLL design in a 90nm process technology. 3D parasitic RLCs for our oscillator ring were extracted with skin effect accounted for. Our PLL provides a frequency locking range from 6 GHz to 9 GHz, with a center frequency of 7.5 GHz. The oscillator alone consumes about 25 mW of power, and the complete PLL consumes a power of 28.5 mW. The observed jitter of the PLL is 2.56%. These numbers are significant improvements over the prior art in standing wave based PLLs.

To my family

ACKNOWLEDGMENTS

I would like to take this opportunity to thank everyone who helped me with my research.

I would like to thank my advisor, Dr. Sunil P. Khatri, with a deep sense of gratitude for assigning me challenging projects and constantly guiding me. I am also thankful to him for providing a wonderful lab facility and an environment perfectly suited for research.

I would like to thank Dr. Peng Li and Dr. Eun Jung Kim for agreeing to be my committee members. I would also like to thank Dr. Donald Friesen for substituting Dr. Eun Jung Kim for my thesis presentation.

I would also like to thank Rajesh Garg, Kalyana Chakravarthy, Kanupriya Gulati, and Rajesh Kumar for their guidance and valuable comments when required.

I would also like to thank my parents for the confidence they had in me without which I would have never been able to pursue and complete my masters study.

I would like to thank Texas A&M University and the Department of Electrical and Computer Engineering for giving me an opportunity to pursue my masters degree.

I am grateful to God without whose blessings I would not have been here.

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CHAPTER I

INTRODUCTION

The work presented in this thesis is the first step in the development of a new technique suitable for clock distribution at high frequencies (6GHz - 9GHz). Digital integrated circuits typically require a global signal called *clock* that controls the flow of data within and across the circuit blocks. This *clock* signal is distributed over the chip using a clock distribution network which ensures that each end-point has the same clock frequency and phase. Conventional clock distribution topologies are as follows:

- *Trees:* Clock trees are a network of buffers and wires that connect a central clock source to a multitude of clock loads. The most commonly used tree distribution is the H-Tree. Figure I.1 shows a two level H-Tree. A H-Tree consists of wires arranged in a recursive-H geometric pattern. All the end points of the H-Tree are uniformly spaced with respect to the central clock driver. Hence all the end points receive their clock signals after traveling through identical wire segments (in terms of length and width) and the same number of identical drivers which are depicted as triangles in Figure I.1. A large buffer drives the clock signal to the center of the tree, while the length of the wires and sizes of the buffers are progressively reduced as we traverse each path from the center of the H-Tree to any end-point. Note that all the end-points can be reached from the center by traversing identical wires and identical buffers. Skew (which is defined as the maximum difference in the arrival time of the clock signal over all the pairs of end-points of the distribution network) in this structure arises due to non-uniform loads along the tree.

The journal model is *IEEE Transactions on Automatic Control.*

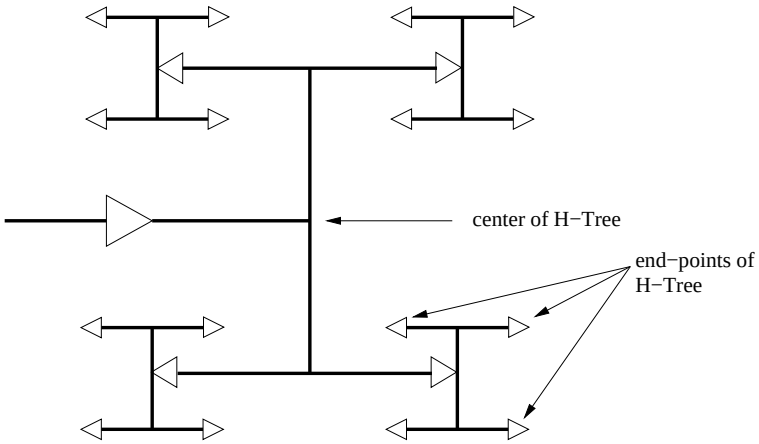


Fig. I.1. H-Tree Based Clock Distribution Network

- *Grids:* A clock grid is a set of horizontal and vertical metal wires, forming a mesh structure. Figure I.2 shows a 4X4 grid. The clock is injected either from the middle or from the edges. Horizontal and vertical segments are shorted whereever they intersect. Because a clock grid has a number of shorted redundant clock paths, it reduces clock skew at a cost of increased capacitance and hence power.

- *Hybrid:* In some recent digital ICs, hybrid topologies (which combine both H-trees and grids) are used. The first (global) level of the clock distribution network uses a H-Tree, ending in multiple points on the chip. The second (global) level of the clock network uses grids in order to reduce random and uneven load based skew.

The above mentioned techniques have been effectively used for the past few decades. As process technology scales and die sizes increase, applying these techniques has become increasingly difficult due to the following reasons:

- *Timing Uncertainty:* Keeping maximum timing uncertainty below a fixed percentage of the clock period is a significant challenge. The two categories of timing uncertainties are as follows

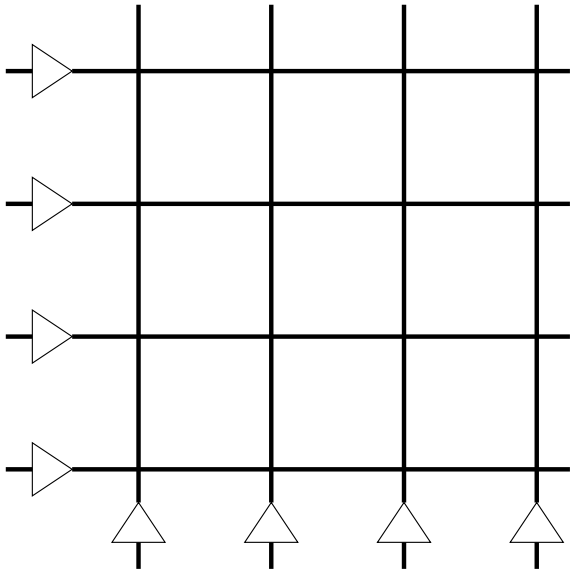


Fig. I.2. Grid Based Clock Distribution Network

– *Skew:* Clock skew refers to the maximum difference in the clock arrival time between any two different end-points in a clock distribution network. Clock skew is graphically shown in Figure I.3. In this figure, $node1$ and $node2$ are two different end-points of the clock distribution network. Nominally, the clock is expected to reach $node1$ and $node2$ at the same time. The main reasons for clock skew in a network are mismatches in device and interconnect, and temperature or voltage variations across the die. In an ideal scenario we would expect a clock distribution network to have zero skew.

– *Jitter:* Jitter refers to uncertainties in timing at a single end-point (clock load). Jitter is pictorially depicted in Figure I.4. In this figure, the clock period of $node1$ varies over time from a minimum value T_1 to a maximum value T_2, yielding a jitter of $T_2 - T_1$. Jitter is computed by measuring the difference between maximum and minimum clock period over a long duration of operation.

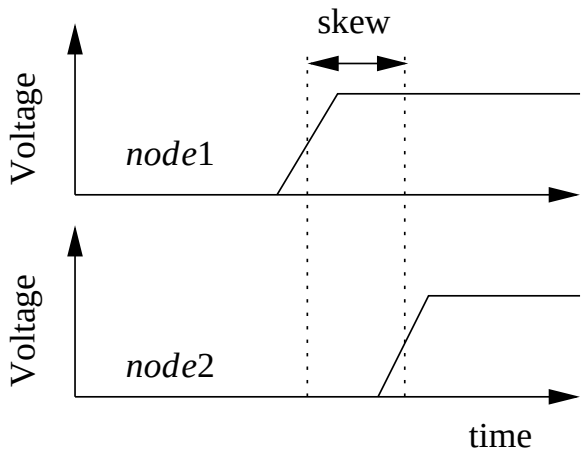


Fig. I.3. Clock Skew

Sources of jitter can be power supply noise or capacitive cross-talk induced noise.

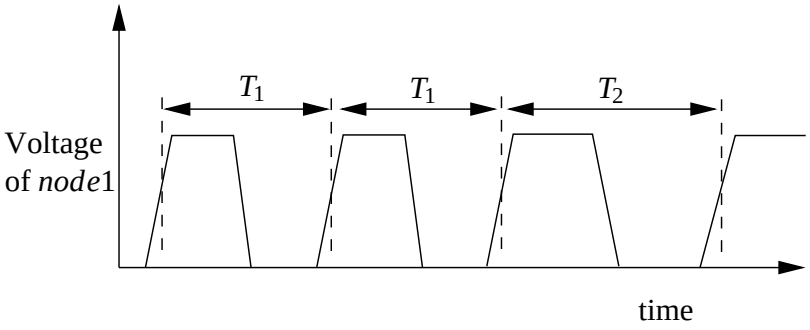


Fig. I.4. Clock Jitter

These timing uncertainties can result in setup time violations along the longest path, and hold time violations along the shortest path. Hence it is desirable to keep these uncertainties within bounds.

- Power: In the current digital ICs there is an increasing concern about power consumption. Since the clock distribution network drives a large amount of capacitance,

this results in a large power dissipation, which is a significant fraction of the overall chip power.

In this thesis we propose a novel technique to generate and distribute a phase-locked synchronous clock with low skew, jitter and reduced power dissipation. In recent times there has been much interest in mobius ring based resonant oscillators as a means to generate the clock signal for digital ICs. Both traveling wave [5, 6, 7, 8] and standing wave [1] oscillators have been proposed in the literature. The typical configuration of these oscillators is a pair of closely spaced wires configured in a ring topology, and implemented on the higher metal layers of an IC. At one end, these rings are connected in a mobius fashion. This structure has RLC parasitics, and for reasonable values of the perimeter of the ring, it can exhibit high frequency oscillations. A single pair (or a multitude of pairs) of cross coupled inverters is connected between the 2 rings of the mobius location, to provide a negative resistance and hence sustain the oscillation. Since charge is recirculated in these configurations, they exhibit a low power consumption. Resistive losses in the ring, as well as the power consumed by the inverter pair(s) contribute to the power consumption of these structures. By choosing the length of the ring carefully, oscillations of high frequencies can be sustained, as long as the inverter pair(s) can switch at these frequencies. The traveling wave structure has been fabricated and impressive performance was demonstrated [9].

Both the standing and traveling wave configurations provide a means to generate a *free-running clock signal*. In other words, the resonant standing or traveling wave structure oscillates at a fixed frequency, determined by the parasitics of the rings. In practice, however, it is crucial that any oscillator in a digital system has the ability to modify its phase and frequency in a predictable manner, so as to allow it to be integrated into a PLL.

A PLL is a negative feedback control system that generates an output clock which is both phase and frequency locked to the input reference signal. A block diagram of a basic

PLL is shown in Figure I.5. In this figure, *out* is the output clock generated by the PLL which is phase locked to $refclk$ (which is the input clock). The *out* clock is frequency divided to yield a $divided\_clk$ signal, which is phase and frequency locked to $refclk$. The operation of each of the blocks in the PLL has been discussed later in this thesis.

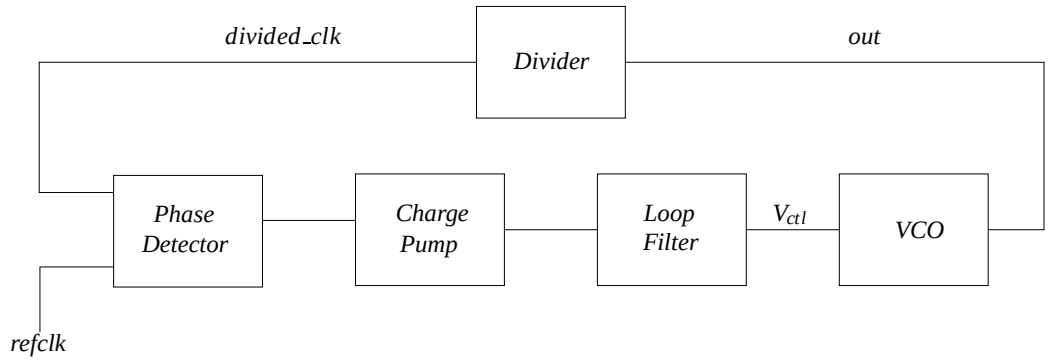


Fig. I.5. Block Diagram of a Basic PLL Design

There are numerous applications of a PLL in a digital system, of which clock synthesis and synchronization are the main applications.

- *Clock Synthesis:* Modern day digital systems require clock frequencies in the gigahertz range. The on-chip clock is generated from a reference (external) crystal oscillator (which typically generates a low-jitter clock in the frequency range of 100MHz). To generate a high frequency on-chip clock from a slower external crystal oscillator, a PLL is used as a frequency multiplier, as shown in Figure I.6.

- *Synchronization:* In a digital system, if $Data$ is received synchronous with respect to an external ref_clk, then the internal clock of digital system (shown in the Figure I.7) needs to be synchronized to ref_clk. A PLL phase and frequency locks the output of the clock buffer with respect to ref_clk and hence $Data$ is correctly captured. Without a PLL, a high frequency on-chip oscillator (such as a resonant standing or

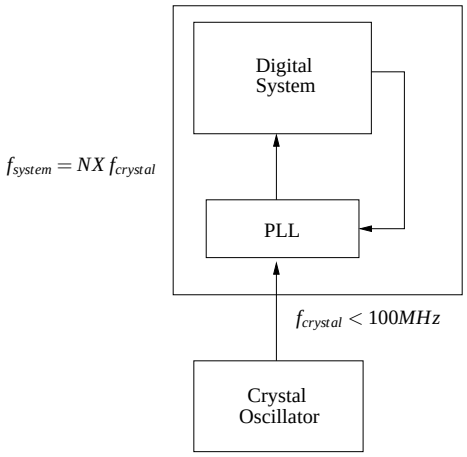


Fig. I.6. Clock Synthesis Using a PLL

traveling wave oscillator) can easily exhibit significant skew compared to the external (board or system) clock. This would make it impossible to design a synchronous system using an IC with a free-running, high frequency resonant oscillator.

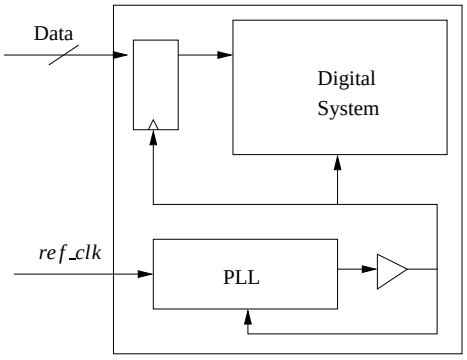


Fig. I.7. Clock Synchronization Using a PLL

Typical oscillators in a digital IC use some form of Voltage Controlled Oscillator (VCO) [10, 11, 12, 13, 14], and implement a PLL with the VCO in a closed-loop configuration (as depicted in Figure I.5). A phase frequency detector (PFD) determines the

phase error, and accordingly either speeds up or slows down the oscillation frequency of the VCO. VCOs are typically implemented in one of two ways

- *Analog* VCOs (ACOs) [15, 16], in which a ring oscillator with a small (odd) number of inverters is typically used. This ring oscillator's frequency is modified by means of a voltage or current signal. Figure I.8 shows an implementation of an Analog VCO. The frequency of oscillation of the ring oscillator is controlled by modulating the gate voltage (V_{ctl}) of the stacked NMOS transistors, thereby achieving a current-starved ring oscillator based ACO.

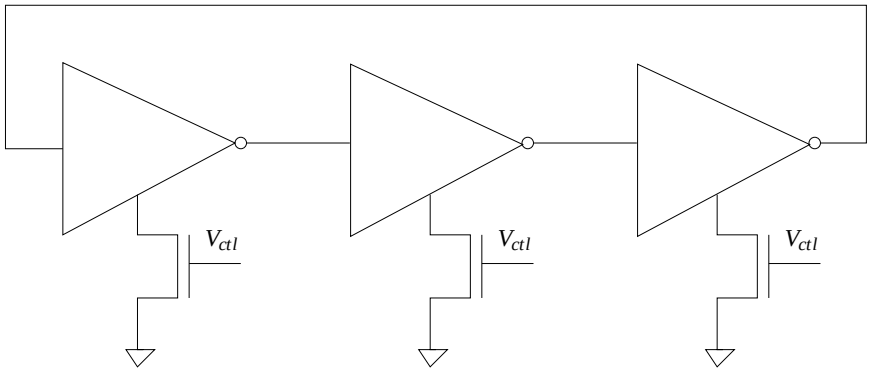


Fig. I.8. Analog Voltage Controlled Oscillator (AVCO)

- *Digitally Controlled Oscillators* (DCOs) [12, 13, 14], in which a large number of inverters are implemented such that inverter i drives the input to inverter $i+1$. By closing the loop at the k^{th} inverter (where k is odd), the oscillator can be made to oscillate at variable (discrete) frequencies. The oscillator can be sped up or slowed down by decrementing or incrementing k respectively, using a control signal b_k which closes the loop at the k^{th} inverter. Figure I.9 shows an example of a DCO implementation. The number of inverters that act as part of the ring is controlled by setting the values of b_3, b_5, b_7,...,b_k,...,b_n in a one-hot fashion.

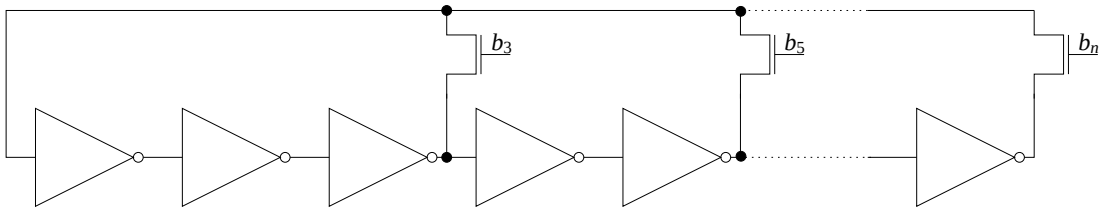


Fig. I.9. Digitally Controlled Oscillator (DCO)

In this thesis, we present a PLL which is implemented as a combination of both an ACO and a DCO, using a resonant standing wave topology. Since the mobius rings are made up of wires on (typically higher) layers of the metal stack of the IC, it is hard to modify the parasitic inductance or capacitance of the resonant rings in practice. The parasitic inductance and capacitance of the rings are fixed once the wire dimensions, metal layer and wire spacing are determined. The key observation that enables frequency to be varied is the use of n wires in each ring (i.e $2n$ wires in all). By selecting between various configurations in which a variable number m of these wires are programmed to carry the ring signal (with the other n - m wires connected to a virtual ground terminal), we are able to vary the parasitic inductance and capacitance significantly, allowing the structure to behave like a DCO. This gives us the ability to tune the oscillator frequency in a coarse manner. For finer tuning of the oscillation frequency, we modulate the reverse body bias voltage of the PMOS transistors of the cross coupled inverter pair. We found that this is an effective way to change the ring capacitance in a continuous manner, and hence achieve a continuous fine frequency control.

We have designed a PLL with a standing wave resonant oscillator as one of its components. The PLL consists of coarse and fine tuning circuits. The coarse tuning circuit, with the help of a threshold detector, a successive one detector and a thermometer converter, programs an appropriate number m of wires (out of n) to participate in the oscillation. The fine

tuning circuit is a conventional third order PLL consisting of a PFD, charge pump and low pass filter. The fine tuning circuit changes the body bias voltage of the PMOS transistors of the inverter pair in order to modify the oscillation frequency in a continuous manner.

The complete PLL has been simulated in HSPICE [17], using a 90 nm PTM [18] technology. Skin-effect adjusted parasitics of the mobius ring were extracted using Raphael [19].

The key contributions of this thesis are:

- By providing both a coarse and fine control over the frequency of the resonant oscillator, we are able to demonstrate a continuous frequency response from $\sim$6 GHz to $\sim$9 GHz (with a reduced power consumption due to the use of resonant standing wave oscillator).

- The PLL has been integrated with the proposed variable frequency standing wave oscillator, and is able to lock within the above-mentioned frequency range using the fine and coarse control circuits, based on our SPICE simulations.

The remainder of this thesis is organized as follows. Previous work is described in Chapter II, while Chapter III provides the details of our resonant standing wave oscillator and the PLL. Chapter IV presents results from experiments which we conducted to implement our PLL. In Chapter V we present discussions related to our work and in Chapter VI we conclude and present directions for future work in this area.

CHAPTER II

PREVIOUS WORK

Recently, a *traveling wave* resonant oscillator circuit (referred to as a *rotary clock*) was described and implemented [5, 9]. The key idea in this approach is to utilize a sufficiently long wiring ring, such that its capacitive and inductive parasitics result in a high frequency oscillatory network. This resonant clock topology is described in Figure II.1. Oscillations in this network are sustained by a plurality of inverter pairs spaced along the ring (Figure II.1). The key drawback of the rotary clock is that the phase of the generated clock varies along the ring (as shown in Figure II.2), making traditional synchronous clock based design extremely difficult. Also, the clock signal at every point of the ring is a full-rail signal, resulting in a larger power consumption.

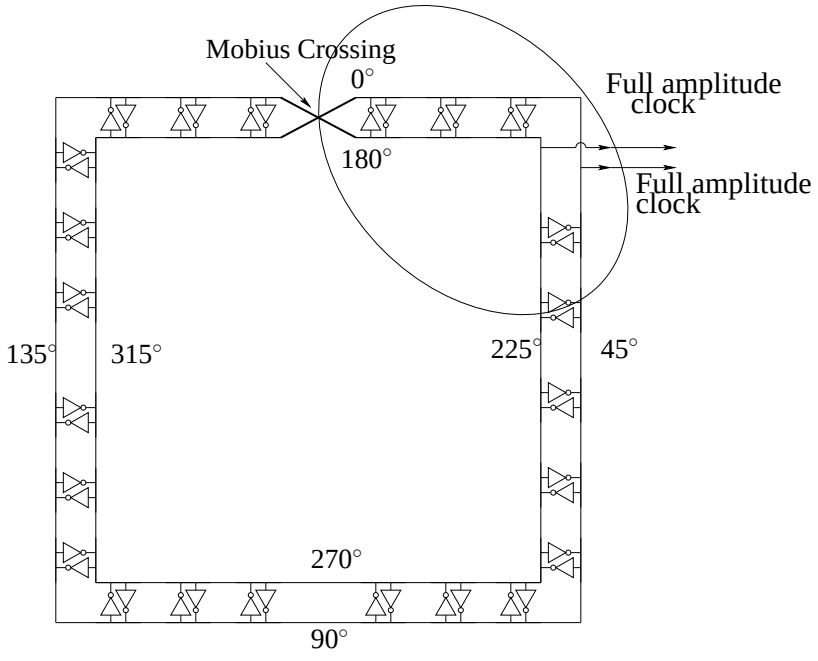


Fig. II.1. Circuit Topology

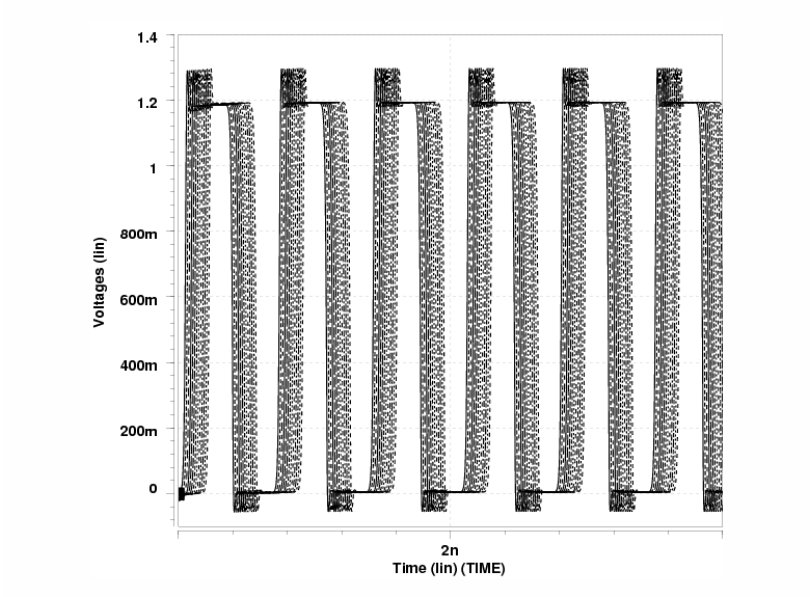
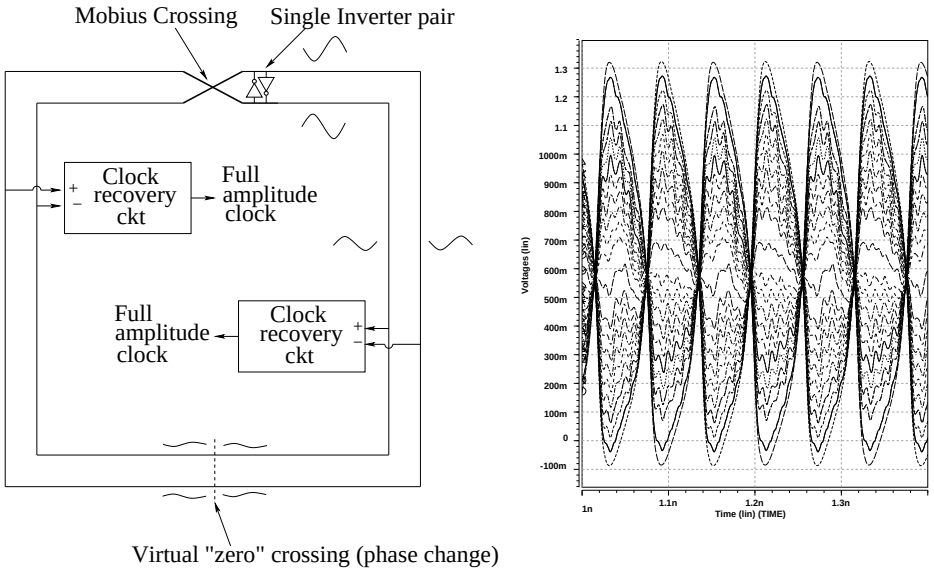


Fig. II.2. Sample Waveforms (Overlaid)

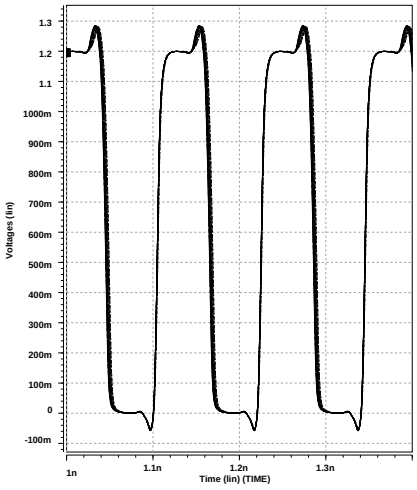
In [8], the authors present a 2.5 GHz PLL using a traveling wave oscillator, to sample input data and perform clock recovery using the 24-phase distributed VCO. The design recovers 16 bits within a clock period. Though it is advantageous for Clock Data Recovery (CDR), the varying phase of the traveling wave clock makes synchronous clock based design difficult.

In response to this, a *standing wave* resonant oscillator circuit was proposed [1]. In this approach, a long wiring ring is used, but oscillations are sustained in this resonant ring by just using a *single* inverter pair (Figure II.3 a). By making a mobius connection at the end of the ring, the clock signal at any point in the ring is sinusoidal, and has the *same phase* at all points along the ring (as shown in Figure II.3 b).

By using differential amplifiers at different points in the ring, full rail clock signals are extracted at the locations desired (Figure II.3 c). As a consequence, this approach yields clock signals that have the same phase everywhere along the ring. This is a key



(a) Standing-wave Resonant Clock [1] (b) Waveforms along the Ring (overlaid)



(c) Recovered Clock Waveforms (overlaid)

Fig. II.3. Standing Wave Resonant Clocking Concept [1]

improvement over the rotary clock of [5]. In addition, the reduced ring capacitance due to the use of significantly fewer inverters (in particular, just one), increases the operating speed and reduces power consumption as well. Note that there is an AC null (virtual ”zero”) point in the center of the ring as shown in Figure II.3 a). As a result, the phases of the signals on the right and the left of the null point are 180° apart. Therefore, clock recovery circuits on the left have their connections reversed compared to recovery circuits on the right of the null point. Note that clock recovery is not performed near the null point, since the signal amplitude is very low near the null point. Both Figure II.3 b) and c) were obtained using the same simulation conditions that were used in [1]

As described earlier, the resulting clock for all the above approaches is free-running, and since the inductive and capacitive parasitics of the ring are fixed, the above approaches do not lend themselves to realizing a variable oscillation frequency.

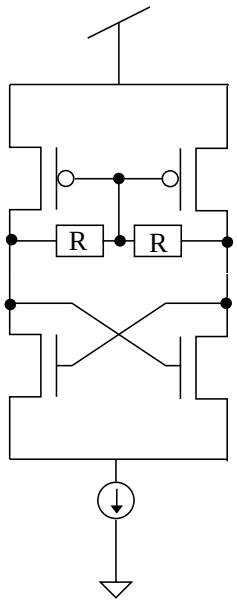


Fig. II.4. Cross-Coupled Pair Used in [2]

In [2], another high-frequency standing wave oscillator was proposed. It is based

on the use of multiple coupled oscillators (each comprised of an NMOS cross-coupled pair to sustain the oscillation, and a PMOS diode-connected load for setting the common mode voltage (Figure II.4)) as shown in Figure II.5. Each of the blocks labeled ”ccp” in Figure II.5 is a cross-coupled pair exhibiting negative conductance. It can also be noted that the approach of [2] does not use a mobius connection like our approach does. In [2], the frequency of the oscillator is modulated by *Injection Locking*. Injection locking involves injecting current (as shown in Figure II.6) to force oscillations at a specific frequency. This current can be dictated by an external source such as a PLL. The position of the injected current affects the strength of the coupling, with maximum strength at the center of the Standing Wave Oscillator (SWO). Unlike our approach, [2] achieves a very small (6.4%) locking range (In contrast, we achieve a $\sim$ 33% locking range from $\sim$6 GHz to $\sim$9 GHz).

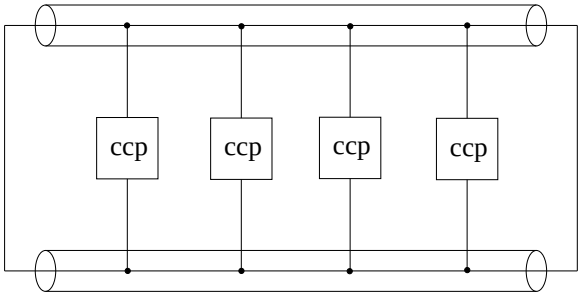


Fig. II.5. Standing Wave Oscillator of [2]

PLLs have been important blocks in the field of VLSI for the past few decades. As the operating frequencies increase while the supply voltage is being scaled down in the modern day CMOS technology, the VCO tuning gain has to increase considerably to achieve a good frequency range of the oscillator. But having a high VCO gain would degrade PLL performance in terms of noise. This issue can be tackled by having both coarse (DCO) and fine tuning (ACO) mechanisms in the VCO (as shown in Figure II.7). In Figure II.7 b) the tuning range achieved is the same as in Figure II.7 a). However, the fine tuning range (and

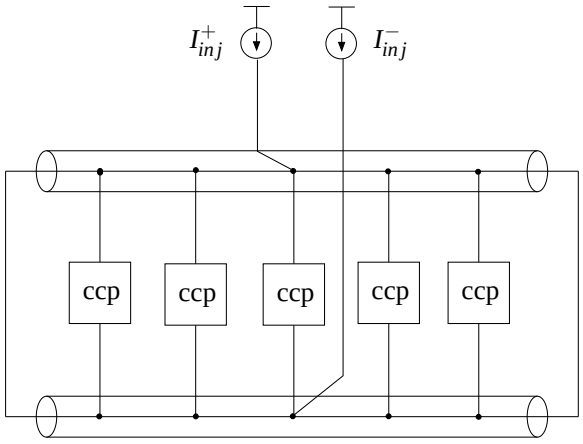


Fig. II.6. Injection Locking SWOs as Shown in [2]

the VCO gain) required in Figure II.7 b) is a small fraction (about 1/5) of that in Figure II.7 a). The authors of [4, 3, 20] have implemented a PLL using a combination of an ACO and a DCO. However, none of the oscillators in [4, 3, 20] were resonant.

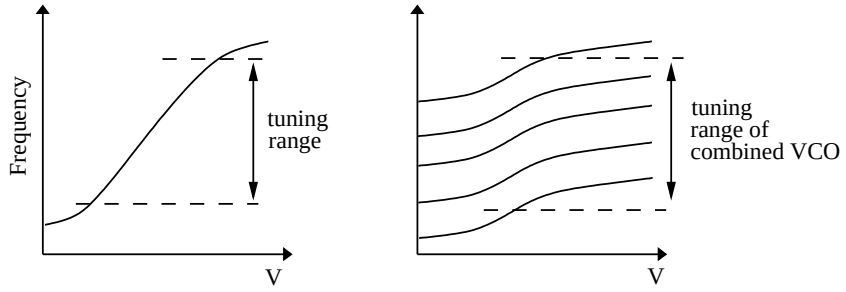


Fig. II.7. Technique to Achieve Large VCO Frequency Range With Small VCO Gain

In [3], the authors proposed an open loop coarse calibration PLL shown in Figure II.8. During the coarse tuning mode, the loop is opened at the loop filter and VCO is connected to a reference voltage. Counters for both *R* and *V* are triggered and both count until one of

the counters overflows. If the counter triggered by *R* overflows before the counter triggered by *V*, then the VCO is moved on to the next higher coarse configuration. If *V* finishes before *R* then the fine tuning loop is closed in order to lock to the required frequency. To ensure good accuracy, both counters should have a sufficiently large number of bits. Hence coarse tuning is slow. The block diagram of the VCO used in this method is shown in the Figure II.9. The coarse programmability is implemented by using a current multiplier. The PLL in this work was designed to operate around 1GHz.

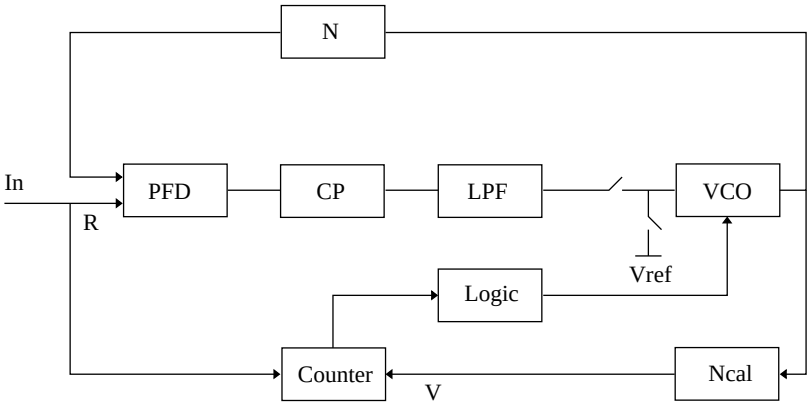


Fig. II.8. PLL Proposed in [3]

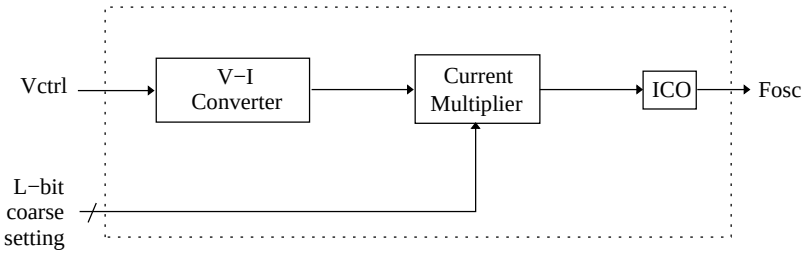


Fig. II.9. Digitally Programmable VCO Used in [3]

In [4] authors propose a closed loop coarse calibration technique shown in Figure II.10. In this method the VCO in the PLL tries to lock to the desired frequency under the given

fine tuning setting. When the loop settles, the control voltage is compared with a pair of predefined voltages. If the settled control voltage is outside the range of these two voltages then the VCO is moved on to the next coarse configuration. This repeats till the appropriate range is reached. In this approach the PLL has to settle to a valid control voltage before comparison. The VCO used in this work is an LC oscillator with switched-capacitors used for coarse configuration, and MOS capacitors used for fine tuning. In this paper the PLL operates at around 900MHz.

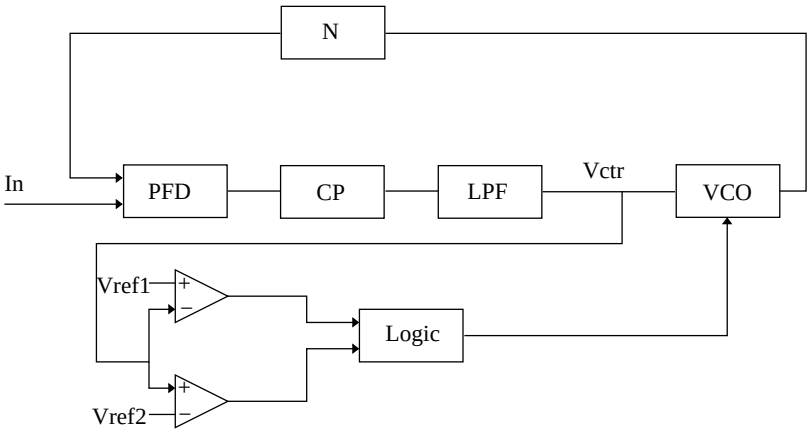


Fig. II.10. PLL Proposed in [4]

In [20] the authors proposed a coarse calibration mechanism which results in a small coarse calibration time. In this approach, during the coarse tuning mode, the loop is opened at the loop filter, and the VCO is operated at a constant frequency. Eight copies of the reference signal are generated, each with a phase difference of $k\pi/4$ from the reference, where k=0,1...7. A phase selector selects one of these copies which has a phase difference between $\pi/4$ and $\pi/2$ compared to the VCO signal. Based on this phase difference, one of 8 coarse frequencies is selected, after which fine tuning is invoked. The VCO used in this work operates on the same principles of [4] for coarse and fine tuning.

It can be noted that none of the above mechanisms use a resonant oscillator as a VCO. Also the operating frequencies of the PLLs proposed in [4, 3] are much lower (about 1GHz) compared to the frequency of operation of the PLL proposed in this thesis. The maximum power consumption of the PLL proposed in [20] is much higher (73mW) than what we achieved in our work (28mW). The center frequency of [20] is 9.4 GHz while ours is 7.5 GHz. Also, [20] has a smaller lock range (14%) compared to our 33%. Also, none of the previous approaches uses inductance based coarse tuning.

Using our approach, we can effectively control the ring inductance and capacitance (and hence the frequency of oscillation), making the resonant oscillator a good candidate for the oscillator block of a PLL.

CHAPTER III

OUR APPROACH

III-A. Design Goal

The design goals of our approach are to realize a resonant oscillator with a high center frequency and frequency tuning range, and to demonstrate the working of a PLL which incorporates this resonant oscillator.

The equivalent circuit for our resonant oscillator is shown in Figure III.1. In this figure, L_w and C_w refer to parasitic inductance and parasitic capacitance of the ring respectively. The capacitance due to the cross-coupled inverter pair (i.e. twice the sum of the diffusion and gate capacitances of any inverter in the pair) is C. Since C and C_w are in parallel, we obtain the equivalent circuit shown.

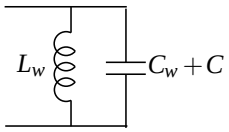


Fig. III.1. Equivalent Circuit for Our Resonant Oscillator

The oscillation frequency of the equivalent circuit is given by

$$f = \frac{1}{2\Pi\sqrt{L_w(C+C_w)}} \tag{3.1}$$

III-B. Standing Wave Oscillator Design

III-B.1. Coarse Frequency Control of the Standing Wave Oscillator

In order to realize a variable frequency oscillator, we modify the base design of [1]. The major modification is to use a large number n of wires in place of the single wire that is

used to implement each ring in [1]. By using a subset of the n wires for oscillation, we are able to modify the parasitic inductance and capacitance of the ring on the fly, allowing us to realize a variable frequency standing wave oscillator. The wires are used symmetrically about the midpoint of the $2n$ wire bundle for oscillation. Each subset of the n wires that we use for oscillation is referred to as a *coarse configuration*.

w_1	w_2	w_3	y_3	y_2	y_1	
1	1	1	1	1	1	← Coarse config 1
1	1	0	0	1	1	← Coarse config 2
1	0	0	0	0	1	← Coarse config 3
Wires of outer ring			Wires of inner ring			

Fig. III.2. Coarse Frequency Configuration

To simplify the coarse frequency control logic, we select a significantly reduced subset of the $2^n - 1$ possible coarse configurations. Figure III.2 illustrates the coarse configurations, for n = 3. In this figure, w_1 refers to the outermost wire of the outer ring, and y_1 is the outermost wire of the inner ring. In this figure, coarse configuration 1 (2) uses a total of 6 (4) wires for oscillation (indicated by a '1' in each of the positions). Note that the oscillating wires in a coarse configuration are symmetric around the midpoint of the bundle of $2n$ = 6 wires. We simulated our oscillator with n = 30.

In practice, the wire locations that are labeled as '0' in Figure III.2 are actually left floating by the control logic. Assuming that the supply voltage of the inverter pair is VDD, both rings oscillate around a DC value $VDD/2$, with sinusoidal waveforms which are always in phase, but whose amplitude vary as we traverse the ring. Since the null oscillation point (labeled as *virtual "zero" crossing* in Figure II.3) applies for *all* configurations, we short all $2n$ wires at this virtual ground location. As a result, all wires that are left floating by the control logic actually have a $VDD/2$ voltage on them due to the short at the virtual

ground location (and therefore these wires act as ground wires in an AC sense).

From Figure III.2, suppose we have two configurations with numerical indices P and Q respectively. Let $P < Q$. Then there are more oscillating wires in the inner and outer rings for P (as compared to Q). Also, the distance between oscillating wires in the two rings is lower for P. This has two effects.

- The capacitance of the oscillating wires is larger for P as compared to Q, since P has more oscillating wires.
- The inductance of P is lower than that of Q, since the current return loop is smaller in P compared to Q, due to proximity effect.

The ratio of the increase in capacitance of P over Q is less than the ratio of the increase in inductance of Q over P. As a result, based on the frequency of oscillation of the ring (Equation 3.1), P oscillates at a higher frequency than Q.

Our resonant standing wave oscillator is controlled by varying the values of the n-bit vectors **w** and **y**.

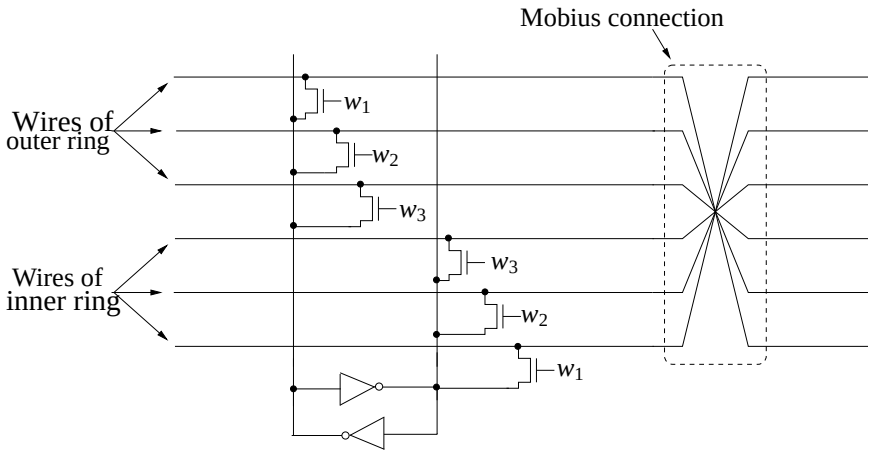


Fig. III.3. Coarse Configuration Selection and Mobius Connection of 2n Wires

The circuitry for coarse frequency control is illustrated in Figure III.3. This circuit takes as input the vectors **w** and **y**. Based on the values of these vectors, the appropriate wires among the 2*n* wires of the oscillators are made to oscillate. If coarse configuration 2 is chosen, for example, only the top 2 and the bottom 2 wires in Figure III.3 oscillate. Note that this circuit resides at the mobius point of the resonant oscillator, and the cross-coupled inverter pair is shown in the figure as well. The mobius connection of the 2*n* wires is illustrated to the right of Figure III.3. Note that in practice $w_i = y_i$.

In practice, the switches in Figure III.3 are NMOS passgates. We tried complementary passgates, but the diffusion capacitance of complementary passgates caused a noticeable drop in oscillation frequency. In order to decrease the body effect, we connect the source and bulk terminals of these NMOS passgates. The coarse tuning approach achieves a maximum (minimum) frequency of a 9.2 GHz (6.2 GHz) in our design.

III-B.2. Fine Frequency Control of the Standing Wave Oscillator

For fine frequency control, we take advantage of the fact that the capacitance of the cross coupled inverter pair contributes significantly towards the total capacitance of the resonant ring. One of the major contributors of cross coupled inverter capacitance is the drain to bulk depletion capacitance of both the PMOS and NMOS transistors. This depletion capacitance is varied by changing the bulk voltage. An increase (decrease) in the body bias voltage (i.e an application of reverse body bias) of a PMOS (NMOS) transistor would result in an increase in the depletion width, reducing the depletion capacitance and resulting in a decrease of the overall ring capacitance. This results in an increase in the frequency of oscillation of the ring.

In our implementation, we varied the body bias voltage of both the PMOS transistors from 1.2V to 2.4V to achieve fine tuning of the oscillator frequency. Fine frequency control could also be achieved by using varactors, but this would require additional components in

the design, and a more complex fabrication process.

III-B.3. Integrated Coarse and Fine Tuning

In this section, we describe the approach by which we designed an oscillator with a continuous frequency range from 6 GHz to 9 GHz, by combining coarse and fine tuning as shown in the Figure III.4. In the figure, f_0 is the operating frequency under current conditions and f is the final desired frequency. The dots in the figure are the coarse configuration points. In Figure III.4, in order to speed up from f_0 to f, fine tuning is done till a coarse point is reached. Because the oscillator has to speed up further after reaching this coarse point, a coarse jump takes place. Another coarse jump takes place since the oscillator has to speed up even further. After this, the oscillator has to slow down, and since the desired frequency is within the coarse range, fine tuning is done to reach f.

One important requirement to achieve integration of coarse and fine tuning is that the frequency range spanned by reverse body biasing the PMOS transistors of the inverters at every coarse configuration is greater than the difference in frequency between the two adjacent coarse frequency points. This is important as it enables us to achieve a continuously adjustable frequency in the range of 6 GHz to 9GHz without any ”holes” in frequency coverage.

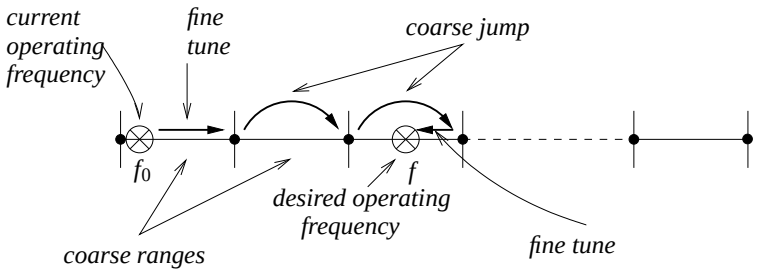


Fig. III.4. An Example to Show Coarse and Fine Tuning Integration

III-C. Proposed PLL Design

III-C.1. Overview

Figure III.5 shows the block diagram of our PLL with the resonant oscillator incorporated. All the components above the dotted line in the figure constitute the fine control circuit and the components below the dotted line constitute the coarse control circuit. The fine tuning circuit of the PLL is a conventional PLL consisting of a PFD, charge pump, low pass filter, VCO and a divider. The charge pump output is used to control the bulk voltage of the PMOS transistors of the cross coupled inverter pair, thereby achieving fine frequency control. The coarse tuning circuit consists of two threshold detectors, two successive one detectors and a thermometer converter. The threshold detector output goes high if the control voltage, which is the charge pump output (*bulk*) voltage, reaches its highest (lowest) value. The output of any successive one detector goes high if the output of the corresponding threshold detector stays high for more than a predetermined number of clock cycles. A rising transition in the output of either of the successive one detectors results in a change in the state of thermometer converter, which drives the digital word (**w** and **y**) that is used to program the oscillator to a particular coarse configuration.

III-C.2. Coarse Control

A brief description of each of the components of the coarse control is given below.

Threshold Detector: If the control voltage exceeds (or goes below) a predetermined threshold value, the threshold detector output goes high. Figure III.6 shows the circuit of the threshold detector that we used. Two threshold detectors have been used in the PLL circuit to detect when the control voltage (*bulk*) exceeds the threshold voltage ref_hi or when it goes below the threshold voltage ref_lo.

The threshold detector circuit has a pair of PMOS transistors (P_1 and P_2) whose gates

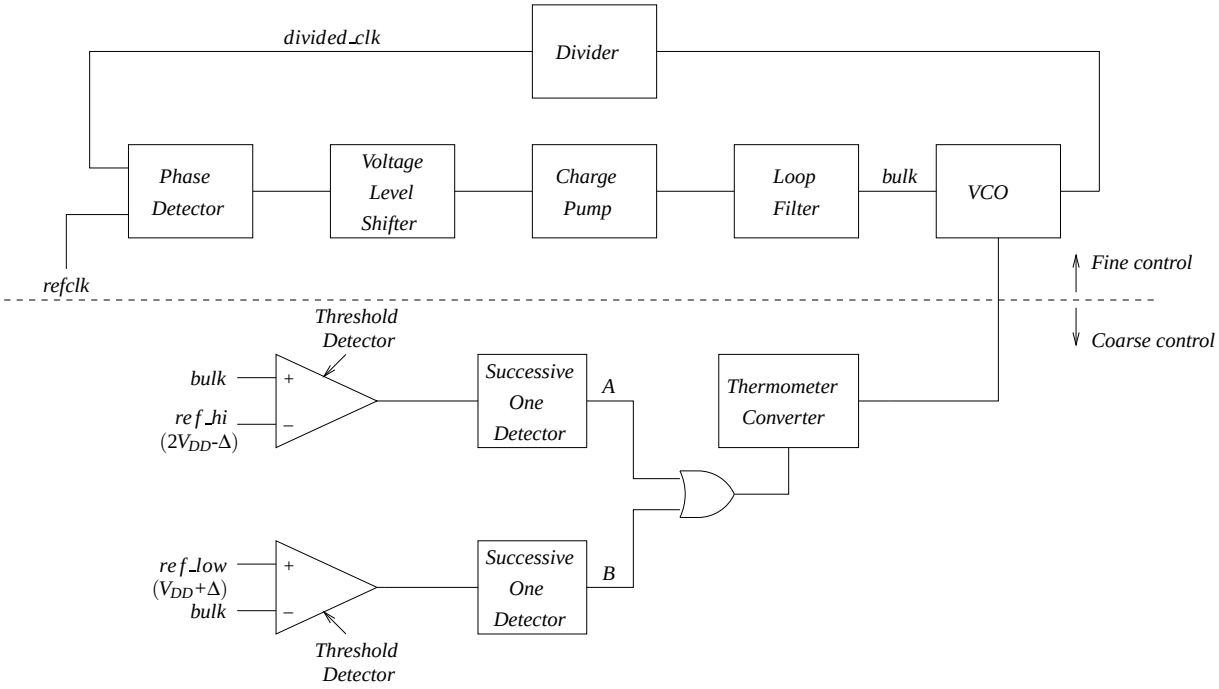


Fig. III.5. Block Diagram of the Proposed PLL Design

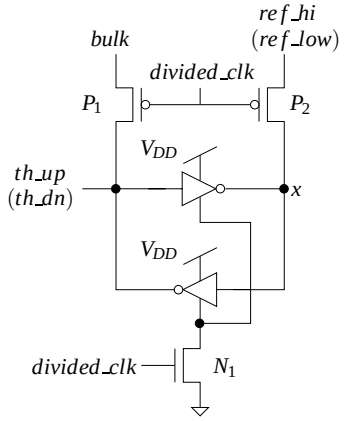


Fig. III.6. Threshold Detector Circuit

are driven by *divided_clk*, and source terminals of these transistors are connected to *bulk* and *ref_hi* (*ref_lo*). The drain terminals of the PMOS transistors are connected across a cross coupled inverter pair whose ground terminal is gated with a NMOS transistor (N_1) whose gate is driven by *divided_clk*.

The working of the circuit is as follows. When *divided_clk* goes low, the voltage on *bulk* and *ref_hi* (*ref_lo*) terminals is sensed by the nodes of the cross coupled inverters (whose ground terminal is floating as the NMOS transistor N_1 is off). When *divided_clk* goes high both the PMOS transistors are off and NMOS transistor is on, and hence the ground terminal is not floating anymore. The intermediate nodes *th_up* (*th_dn*) and *x* are pulled to either *VDD* or *GND*, based on which of these nodes was at a higher voltage when *divided_clk* went high.

In our simulations, the value of the voltage of reference nodes *ref_hi, ref_lo* was 2.3V and 1.3V respectively, we assume that these voltages are provided externally since the range of voltages of the *bulk* node is 1.2 V to 2.4 V.

Successive One Detector (SOD): Each successive one detector detects if the control voltage (*bulk*) exceeds (or goes below) the threshold voltage *ref_hi* (*ref_lo*) for more than a particular number of cycles of *divided_clk*. It is a shift register as shown in the Figure III.7. Its output *A* (*B*) goes high when the output of all the flip-flops in the shift register go high.

The outputs of successive one detectors drive the clock signal of the thermometer converter. All the flip-flops of the detector have to be reset after a particular number of cycles of *divided_clk*. This is because if there is a coarse jump in order to speed up (slow down) the clock, and if the oscillator needs to speed up (slow down) yet further, then *A* (*B*) needs to be reset before it rises again, since the rising edge of *A* (*B*) triggers a change to the next faster (slower) coarse configuration. This is achieved by having additional flip-flops in the shift register of the SOD. In Figure III.7, the *A* (*B*) signal rises if *th_up* (*th_dn*) is high for three consecutive cycles of *divided_clk*. This triggers a transition to

the next higher (lower) frequency coarse configuration. If another shift is required to the next higher (lower) frequency configuration, th_up (th_dn) continues to stay high, and after seven more consecutive cycles of $divided\_clk$, the *reset* signal resets the flip-flops of the SOD. Now if th_up (th_dn) stays high for three more cycles, A (B) rises again, causing a transition to the next higher (lower) coarse frequency configuration.

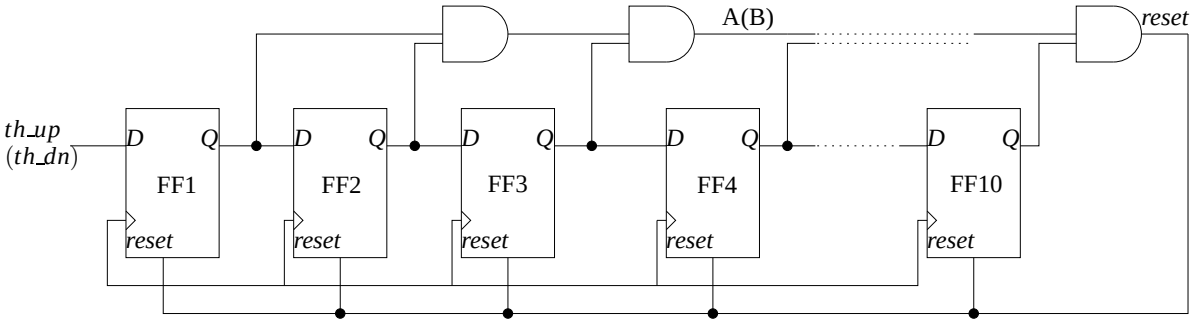


Fig. III.7. Successive One Detector Circuit

Thermometer Converter: The next coarse configuration can be arrived at by an arithmetic right shift of the current state (to speed up) or an arithmetic left shift of the current state (to slow down). The thermometer converter shown in Figure III.8 implements this logic. The thermometer converter consists of a series of D flip-flops connected through MUXes. The output of a particular flip-flop stage i is the input to the MUX $i+1$, and it drives the output of MUX $i+1$ when the control signal A (output of the successive one detector which goes high if there has to be a change in coarse configuration in order to speed up) is high. The input to the first MUX that is selected when A goes high is VDD. Hence when A goes high (indicating that we need to shift to the next faster coarse configuration), the 1's in the thermometer shift to the right. The other input to each MUX is the output of the D flip-flop two stages to the right of the current flip-flop being considered. The input to the last MUX that is selected when A goes low is GND. Therefore if A=0 and B goes high

(indicating that we need to change to the next slower coarse configuration), the 1's of the thermometer shift to the left with a 0 injected into the last stage. The clock signal of all the flip-flops is the output of an *OR* gate whose inputs are *A* and *B* (from the two successive one detectors).

As we used *n*=30 wires in our resonant ring, we used 30 flip-flops and 30 MUXes in order to configure the oscillator.

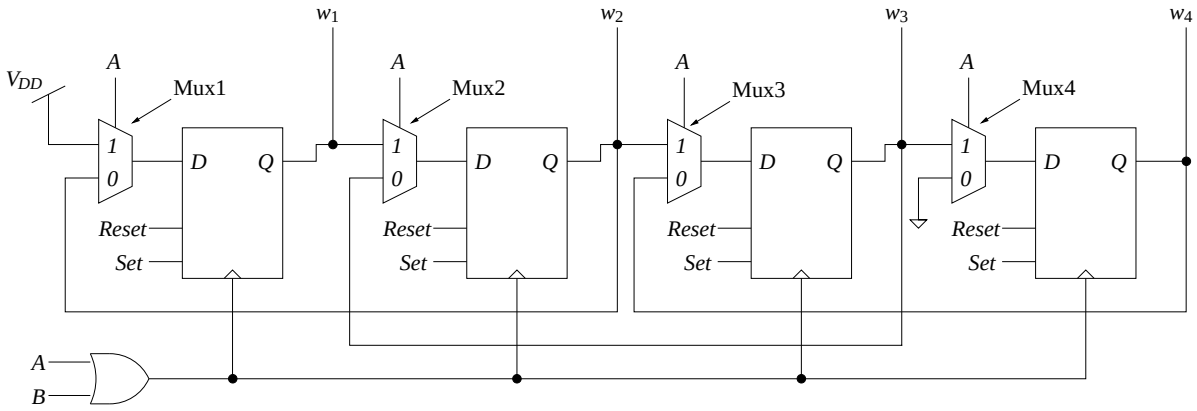


Fig. III.8. Thermometer Converter Circuit

III-C.3. Fine Control

The fine control circuit we used is a conventional third order PLL consisting of a PFD, charge pump and low pass filter, AVCO, and a divider. We had to use a voltage level shifter in order to drive the charge pump (which drives the bulk of the PMOS transistors of the cross coupled inverter pair) between the voltages *VDD* and 2*VDD*. A brief description of each of the components is shown below.

Phase Frequency Detector (PFD): The PFD consists of two flip-flops and an *AND* gate connected as shown in the Figure III.9. The output of the PFD, as its name suggests is dependent on both the phase and frequency difference between the input signals.

The PFD has two input clocks, the external crystal clock (ref_clk) and the divider output ($divided\_clk$) and produces two outputs UP and DN.

The PFD is a simple state machine which has three states. Consider that the UP and DN outputs are initially low. When ref_clk leads $divided\_clk$, the UP output is asserted on the rising edge of ref_clk. The UP signal stays high until a low to high transition of $divided\_clk$. At this point of time, DN rises, causing both the flip-flops to reset through the asynchronous reset signal. There will be a small pulse on the DN output, the width of which is equal to the sum of the delay through the AND gate and the Reset-to-Q delay of the flip-flop. The pulse width of the UP signal is the phase error between the two signals. A similar situation arises when $divided\_clk$ leads ref_clk (the phase error in this case is the width of DN pulse).

Under a lock condition, short pulses will be generated on both the UP and DN outputs.

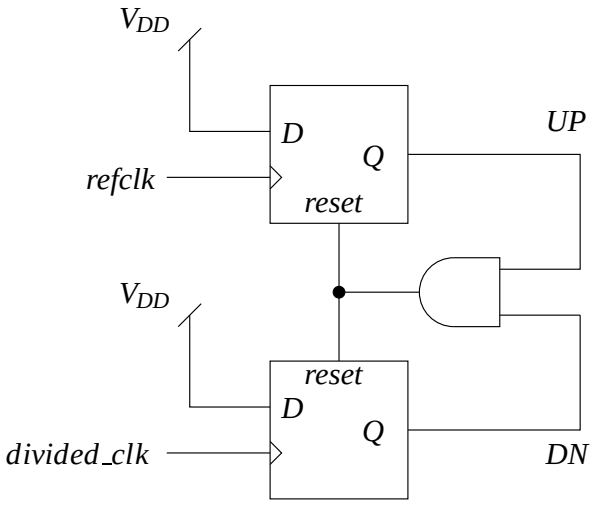


Fig. III.9. Phase Frequency Detector Circuit

Voltage Level Shifter: A voltage level shifter is not required in a conventional PLL.

In the fine tuning circuit that we used, we require a voltage level shifter in order to drive the charge pump (which is connected between $2VDD$ and VDD). The charge pump drives the bulk of the PMOS transistors of the cross coupled inverters with a voltage within this range (VDD to $2VDD$), to reverse body bias the PMOS transistors in a continuous fashion.

The outputs of the PFD are the inputs to the two voltage level shifters. The circuit for the voltage level shifter used for the UP signal is shown in the Figure III.10. The voltage level shifter for the DN signal is identical, except with different signal names. The voltage level shifter requires two power supplies, the input domain voltage supply (VDD) and the output domain voltage supply ($2VDD$). When the input signal UP (DN) is at VDD, MN1 turns on and MN2 is off, and this pulls the $UP\_shifted\_b$ ($DN\_shifted\_b$) signal to GND. This transition in $UP\_shifted\_b$ turns on MP2, which pulls the $UP\_shifted$ ($DN\_shifted$) signal to $2VDD$, as required.

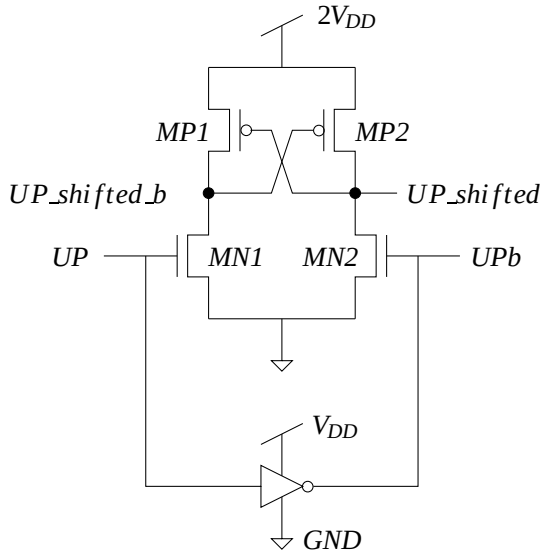


Fig. III.10. Voltage Level Shifter Circuit

Charge Pump and Low Pass Filter: The level shifted pulses $UP\_shifted\_b$ and

DN_shifted must be converted into an analog voltage that control the voltage of the bulk node of PMOS transistors of the cross coupled inverters. This has been implemented by making use of a simple charge pump and a second order filter as shown in the Figure III.11. The charge pump implemented is a pair of current sources being switched by using the *UP_shifted_b* and *DN_shifted* signals. A pulse on the *UP_shifted_b* signal adds charge to the capacitors at the output, proportional to the pulse width of *UP_shifted_b*. The *DN_shifted* pulse removes charge from the capacitors, proportional to its pulse width. If the width of the *UP_shifted_b* pulse is larger than the *DN_shifted*, pulse there is an effective increase in the output (*bulk*) voltage, which increases the reverse body bias and hence the frequency of the oscillator. Note that in our case, the *bulk* voltage varies between *VDD* and 2*VDD*.

The loop filter consists of a resistor R_1 and capacitors C_1 and C_2, and hence is a second order filter, making the system third order. Having only a capacitor at the output of the charge pump would result in a open loop transfer function of second order, with both poles located at the origin. This would render the system unstable as each of the poles contributes a constant phase shift of 90°, resulting in a 180° phase shift before the unity gain crossover frequency, causing the system to oscillate. Hence, in order to stabilize the system, the phase characteristics have been modified by introducing a zero in the loop gain by adding a resistor (R_1) in series with the loop filter capacitance (C_1). Even though the system is stable, the series combination of R_1 and C_1 could result in a large control voltage ripple that could perturb the oscillations. In order to suppress these ripples, an additional capacitance (C_2) was added. The values of R_1, C_1 and C_2 have to be chosen carefully, because the PLL is a third order system, which could result in instability. The procedure to choose values for R_1, C_1 and C_2 has been discussed in Chapter IV.

Divider: In order to achieve an oscillator running with a desired frequency in the range of 6 GHz to 9 GHz, the oscillator output frequency has to be divided by a constant

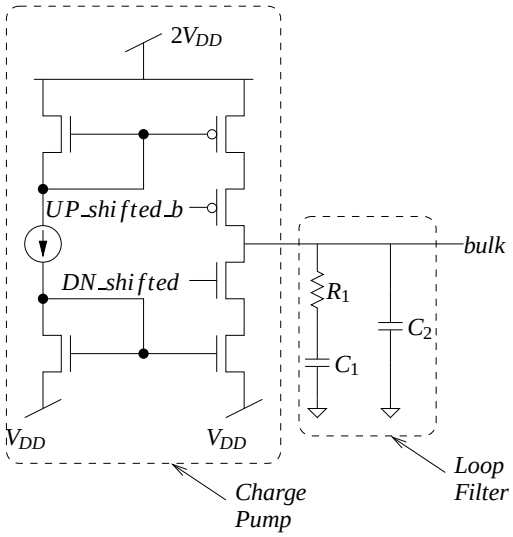


Fig. III.11. Charge Pump and Low Pass Filter Circuit

factor in order to compare the phase and frequency with the 50 MHz reference crystal clock. In our case the division factor was chosen to be 128. The divider that we used was a 7-bit ripple counter. The clock to the first stage of the ripple counter is the output from the oscillator (running at high frequency). A conventional static D flip-flop in the first stage of the counter might result in incorrect operation, as the value of $max(t_{setup} + t_{clktoQ})$ exceeds the minimum desired period of the oscillator. Hence a dynamic D flip-flop with carefully sized gates (shown in Figure III.12) was used. Starting from the second stage, we can use either static or dynamic D flip-flops. In our PLL, we used dynamic D flip-flops for the second and higher stages as well.

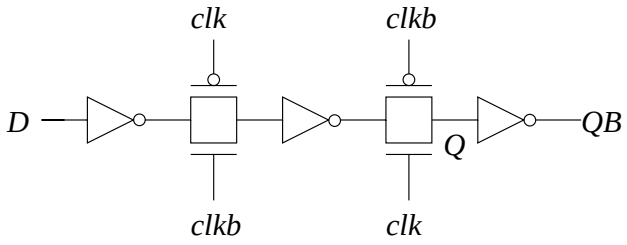


Fig. III.12. Dynamic D Flip-Flop Circuit Used in the Divider

CHAPTER IV

EXPERIMENTS

We implemented the PLL described in this thesis, using a 90nm BSIM3 PTM [18] process technology. The power supply voltage was 1.2V, and all simulations were conducted in HSPICE [17].

IV-A. Oscillator Design

The inner and outer wiring rings of the oscillator consist of $n = 30$ wires each. All the 60 wires were implemented on METAL8, and the total length of the ring was 1500 μm. Each of the 60 wires were 1 μm wide, with an inter-wire spacing of 1 μm. In all the results presented in this thesis, we ensured that at least 80% of the ring (except for the region near the virtual ground point) could be used to recover a rail-to-rail clock using a clock recovery circuit. All large MOSFETs were implemented using multiple *fingers* which shared diffusions, thereby reducing the parasitic capacitances in our design.

The 16 coarse configurations that we used are shown in Table IV.1. Note that for each configuration, we report the 30 values of $\mathbf{w}$. Note that the w_1 value is the leftmost bit of any row of Table IV.1. Also, the 6 highest order bits are always zero, and their corresponding NMOS devices are omitted from the circuit (see Figure III.3). Similarly the 9 lower order bits of $\mathbf{w}$ are always 1, and their corresponding NMOS devices are also omitted from the circuit of Figure III.3. These 9 outermost wires are statically connected to the cross-coupled inverter pair.

We next swept the size of the cross-coupled inverters in HSPICE. We observed that for larger inverter sizes, the inverters' diffusion and gate capacitance resulted in slower oscillations. For smaller inverter sizes, we found that not all of our coarse configurations could sustain oscillations in the ring. Sometimes, even if a smaller inverter size could

Table IV.1. Coarse Configurations Used in Our Experiments

Index	**w** value
1	11111111111111111111111000000
2	11111111111111111111110000000
3	11111111111111111111100000000
4	11111111111111111111000000000
5	11111111111111111110000000000
6	11111111111111111100000000000
7	11111111111111111000000000000
8	11111111111111110000000000000
9	11111111111111100000000000000
10	11111111111111000000000000000
11	11111111111110000000000000000
12	11111111111100000000000000000
13	11111111111000000000000000000
14	11111111110000000000000000000
15	11111111100000000000000000000
16	11111111000000000000000000000

sustain the oscillation, it allowed a rail-to-rail clock to be recovered from less than 80% of the ring. We eliminated these inverter sizes from consideration since they did not meet the 80% recovery requirement. We found that the optimal width of the cross-coupled inverters was 160μm (66μm) for the PMOS (NMOS) device. This allowed all configurations to sustain oscillation, and also passed the 80% recovery requirement.

To size the NMOS passgates of Figure III.3, we conducted a SPICE sweep starting with a minimum sized passgate. As we increased the passgate size, we found that more configurations were able to sustain oscillation. For an NMOS passgate of size 20μm, oscillations were sustained by every configuration of Table IV.1. Also, the 80% recovery rule was met in each case.

We have simulated the oscillator in HSPICE [17], with skin-effect adjusted wiring parasitics extracted using Raphael [19]. We demonstrate that our oscillator provides a continuous frequency response from $\sim$6 GHz to $\sim$9 GHz, with a center frequency of 7.5 GHz. Figure IV.1 illustrates the set of frequencies achievable by our coarse tuning approach. Note that the resulting range of frequencies achievable is quite large and substantially linear. Figure IV.2 illustrates the continuous frequency range achievable for one of the fine

configurations.

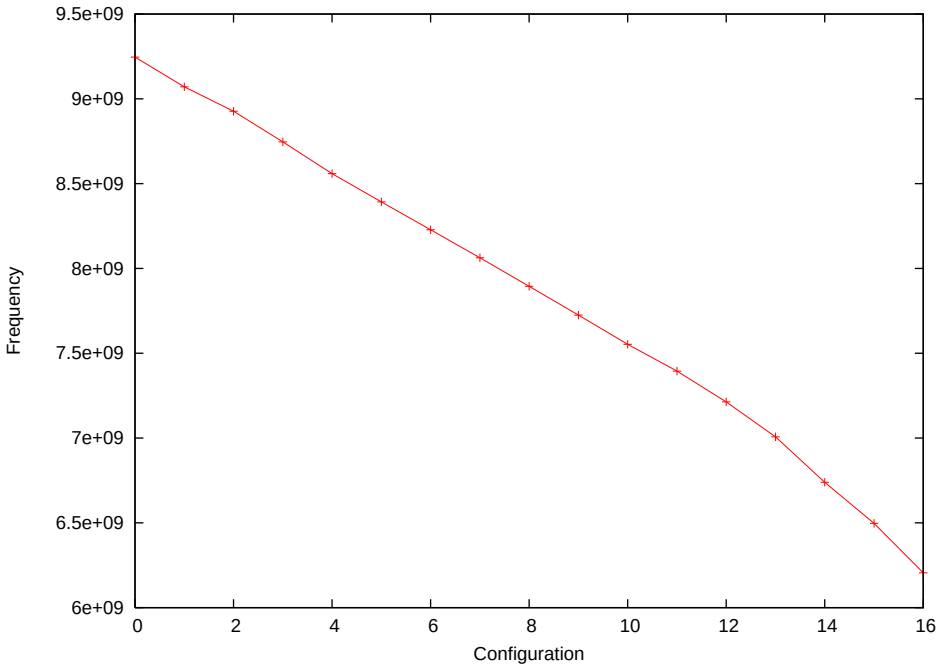


Fig. IV.1. Frequencies Achieved through Coarse Tuning

The power consumption of our oscillator is ∼25mW. This power varies between configurations, but the range of power consumption values stayed between 23.5mW and 25.5mW. As expected, more power was typically consumed at higher frequencies.

The two rings of our oscillator sustain a sinusoidal oscillation. To recover a rail-to-rail clock from any point on the ring, a clock recovery circuit (shown in block diagram form in Figure II.3 a) is required. This circuit is essentially a differential amplifier with a buffered output. The schematic view of our clock recovery circuit is shown in Figure IV.3. A plot of several recovered signals from around the ring is shown in Figure IV.4. From this figure, the rising skew is 3.44ps, while the falling skew is 3.99ps (for a clock of period 142ps).

An important parameter that determines the characteristics of an oscillator is its quality factor (Q factor). The Q factor is a dimensionless quantity that determines how under-

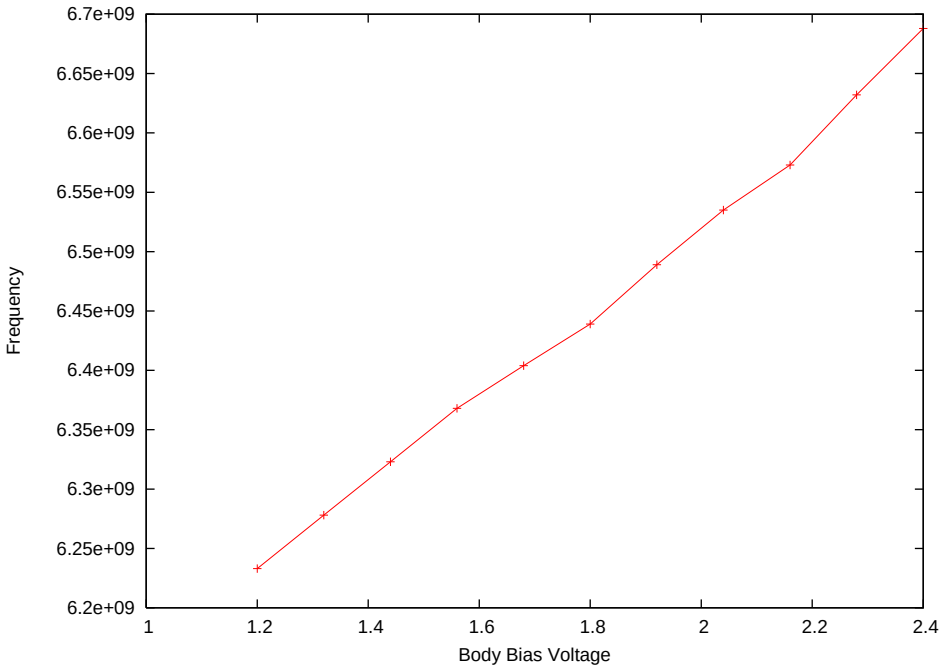


Fig. IV.2. Frequency Range Achieved through Fine Tuning for a Particular Coarse Configuration

damped an oscillator is. High Q and low Q oscillators have their own advantages. High Q oscillators oscillate with a smaller frequency range, and have very high amplitudes at the resonant frequency. Such an oscillator would do a better job of filtering out noise signals. For a network of coupled oscillators, the locking range is large for oscillators with low Q.

The Q factor of our oscillator is measured using the following procedure. First, the cross-coupled inverter pair (which provides negative resistance) is disconnected, and replaced by its equivalent average capacitance (the average capacitance when the bulk is connected to 1.8V was used for this purpose). Then an AC current signal of differential amplitude equal to 1 ampere across the terminals is applied where the cross-coupled inverter pair was connected. After that, the voltage difference across these terminals is measured. We plot this voltage as a function of frequency, for various coarse ranges, in the Figures IV.5, IV.6, and IV.7 (for coarse range 1, 7 and 15 respectively). It can be observed

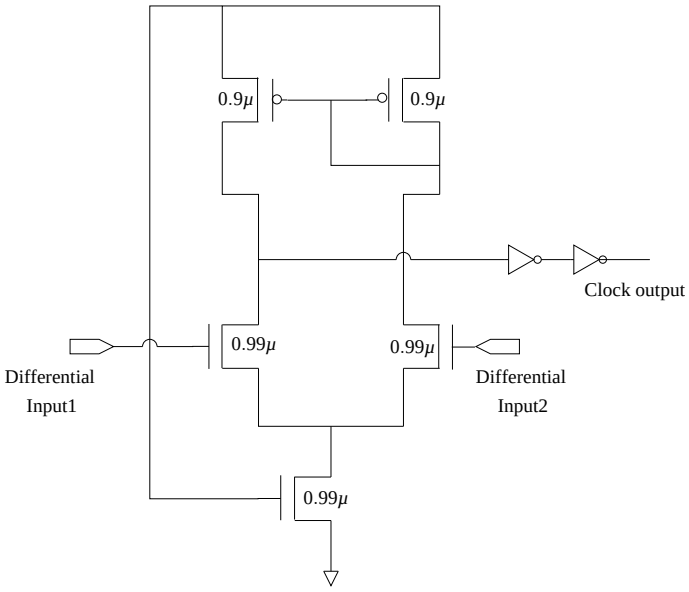


Fig. IV.3. Clock Recovery Circuit

from the plots that voltage makes a peak at the center oscillating frequency. The value of Q can be computed by measuring the center frequency (ω_0) and the 3dB bandwidth (BW) from each plot, computing Q = ω_0/BW. Figure IV.8 shows the values of Q for the different coarse ranges of our oscillator. The value of Q lies in the range of 3.4 - 6.4 for all our oscillator configurations. Hence, it can be concluded from these plots that our oscillator has a modest Q, with a good locking range and hence is a good candidate in designing coupled oscillator networks.

The cross-coupled inverter pair in our oscillator provides negative resistance which compensates for the resistive losses in the ring. An analysis of the negative resistance is shown below. The Figure IV.9 shows the AC equivalent circuit of a NMOS cross-coupled pair. From this equivalent circuit, the input impedance can be derived to be

$$Z_{in} = -\frac{2}{g_m - \frac{Z_{gs}+Z_{ds}}{Z_{gs}Z_{ds}}} \tag{4.1}$$

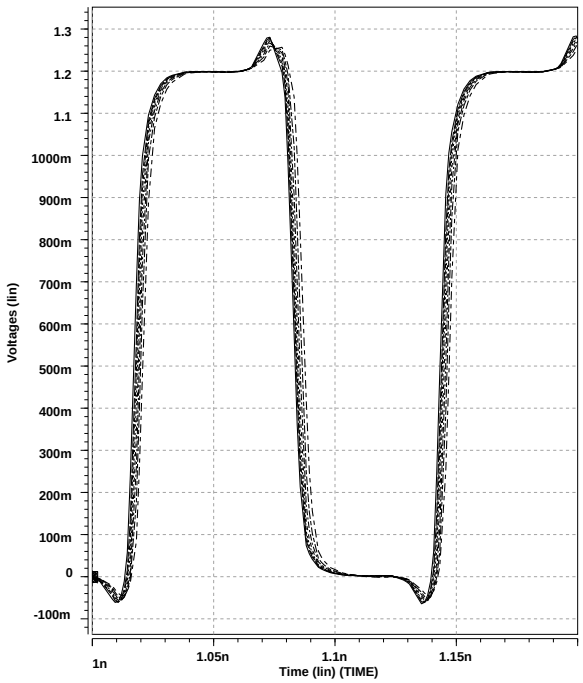


Fig. IV.4. Overlay of Recovered Waveforms

Similarly the corresponding equation for input impedance of the PMOS cross-coupled pair can be determined. Therefore, the total input impedance of the cross-coupled inverters is a parallel combination of the input impedances of NMOS and PMOS cross-coupled pairs. Based on the size of NMOS and PMOS transistors used, and the DC bias at the inputs (which is set to 0.6V), the 3dB bandwidth of the input impedance and its magnitude at low frequencies can be determined using Equation 4.1. The value of bandwidth comes out to be 41 GHz and the magnitude of impedance at low frequencies is about 19.8 Ω. These values agree with the simulated waveform shown in Figure IV.10

Hence, from the above observation it can be concluded that the Q factor is completely

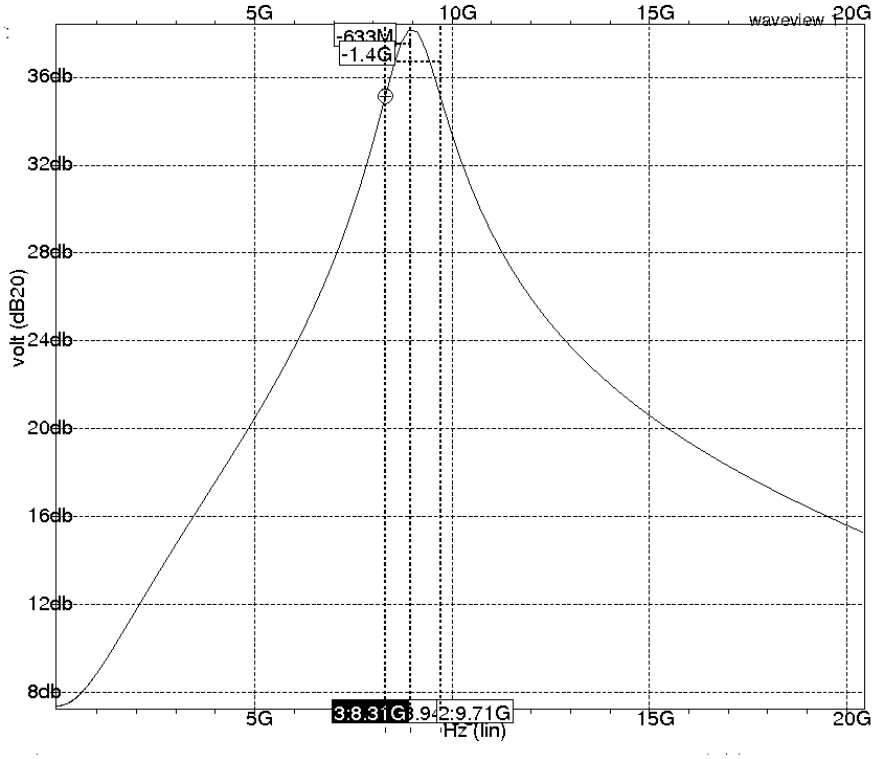


Fig. IV.5. Voltage vs Frequency Plot in Coarse Range 1

dependent on the impedance of the ring which makes a peak at its center frequency, while the impedance of cross-coupled inverters is almost constant in the frequency range of interest.

IV-B. Loop Filter Parameters

The PLL designed consists of coarse and fine tuning circuits. The fine tuning circuit is a conventional third order PLL design. The main parameters that determine the stability of the system are R_1, C_1 and C_2 which are the components of the loop filter as shown in the

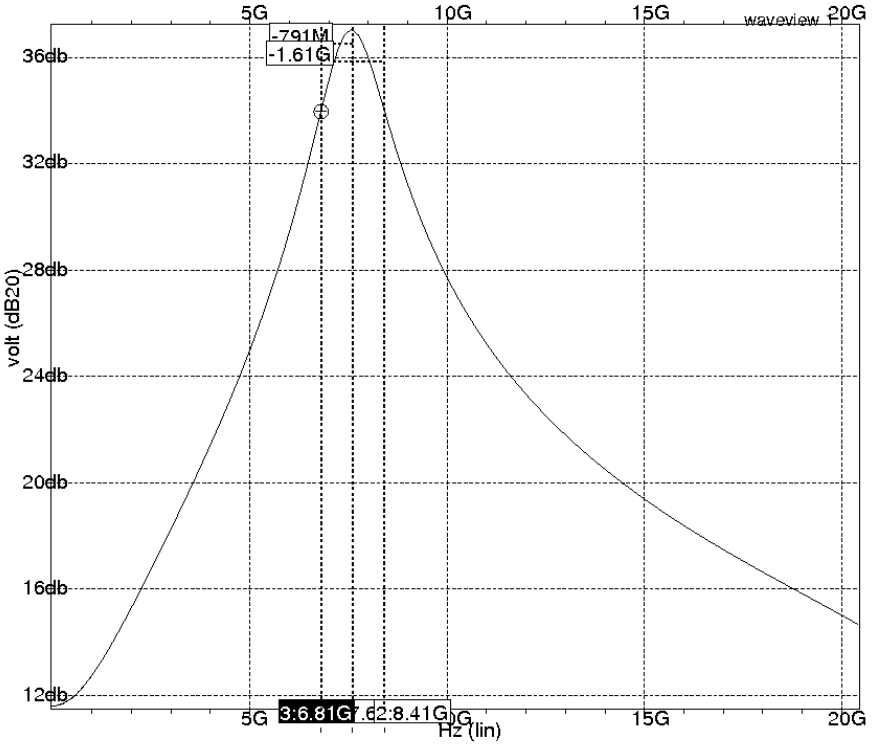


Fig. IV.6. Voltage vs Frequency Plot in Coarse Range 7

Figure III.11. These values have to be chosen with care in order to ensure that the system is stable. The set of design equations [21] that can be arrived at for maintaining a particular phase margin to ensure stability are as follows

$$PM = atan(\sqrt{b+1}) - atan(\frac{1}{\sqrt{b+1}}) \tag{4.2}$$

where

$$b = C_1/C_2 \tag{4.3}$$

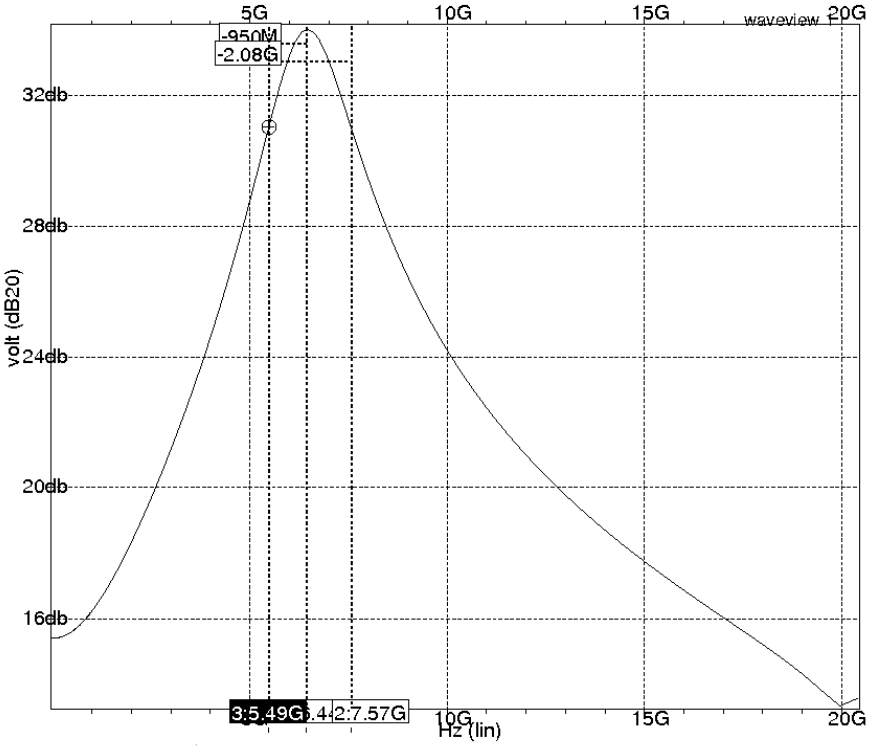


Fig. IV.7. Voltage vs Frequency Plot in Coarse Range 15

let

$$\omega_c = \frac{\sqrt{b+1}}{R_1 C_1} \tag{4.4}$$

then

$$C_1 = \frac{I_p}{2\pi}\frac{K_0}{N}\frac{b}{\sqrt{b+1}}\frac{1}{\omega_c^2} \tag{4.5}$$

In the above set of equations ω_c is the loop bandwidth, K_0 is the VCO gain, I_p is the charge pump current, and N is the factor by which the output clock of resonant oscillator is

divided. We choose ω_c = 5 MHz, which is one-tenth of the reference crystal frequency, and the phase margin (PM) was chosen to be 60°. The value of K_0 was calculated for all the coarse ranges. The value of K_0 varies from 125 MHz/V to 375 MHz/V across the coarse configurations. The highest of all these values was used in the above set of equations. These equations have four degrees of freedom R_1, C_1, C_2 and I_p. Choosing one of the values allows us to calculate the remaining. In our case we chose the value of I_p to be 1 mA, and the values of R_1, C_1 and C_2 turned out to be 9242 Ω, 16.067 pF and 1.24 pF respectively.

Figure IV.11 shows the control voltage waveform in the coarse range 15. The lock time from boot within this coarse range (based on the control voltage profile) shown in Figure IV.11 is 2 μs for the given reference crystal frequency (50 MHz). Note that the time to switch between adjacent coarse ranges is 1280 VCO cycles. For an operating frequency of 7.5 GHz the clock period is 0.13 ns. Hence the average time to switch between adjacent coarse ranges is 0.16 μs. Hence the lock time is dominated by lock time of the fine tuning circuit unlike the hybrid PLLs of [4, 3, 20]. We also verified that our PLL was able to correctly lock to the reference frequency when this required several coarse ranges to be traversed in order to lock.

The total power dissipated in the PLL at lock was found to be 28.5 mW and the jitter observed was 2.56%.

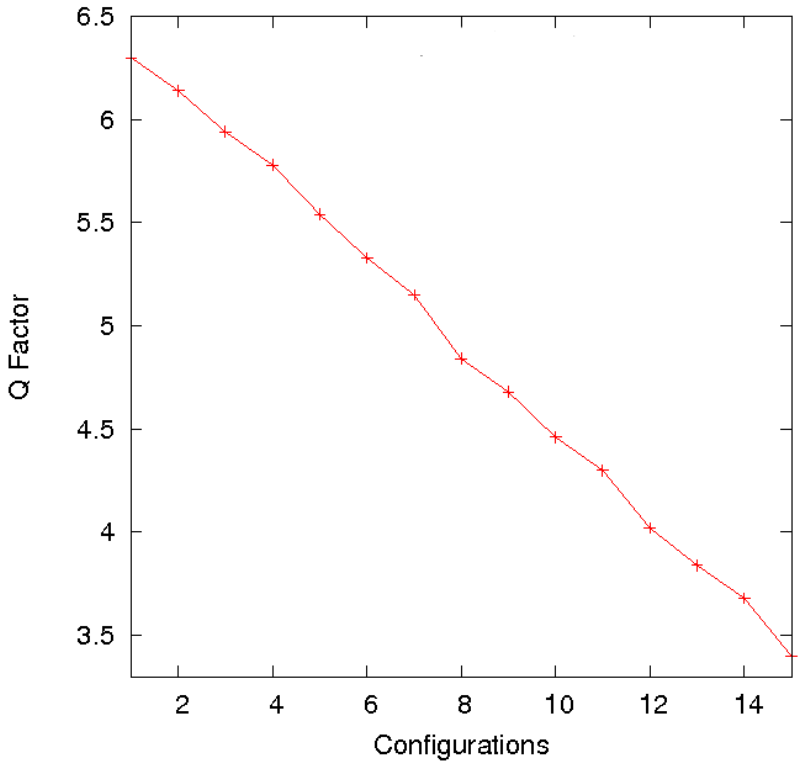


Fig. IV.8. Plot of Q factor for the Coarse Configurations used

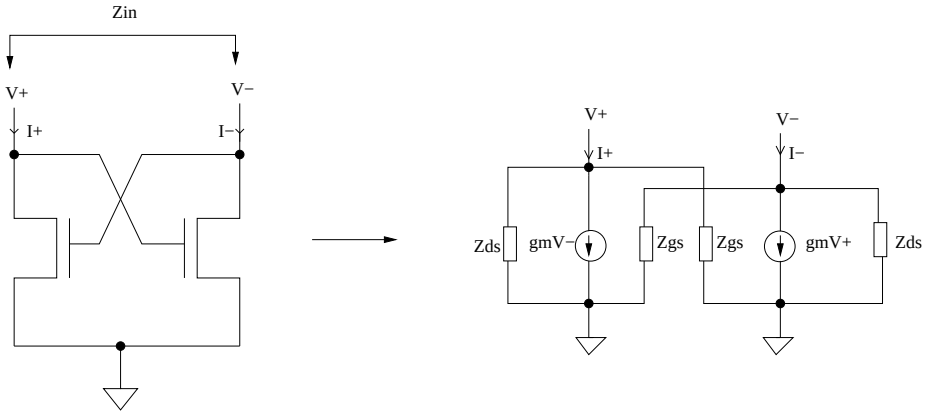


Fig. IV.9. AC Equivalent Circuit of Cross Coupled Pair

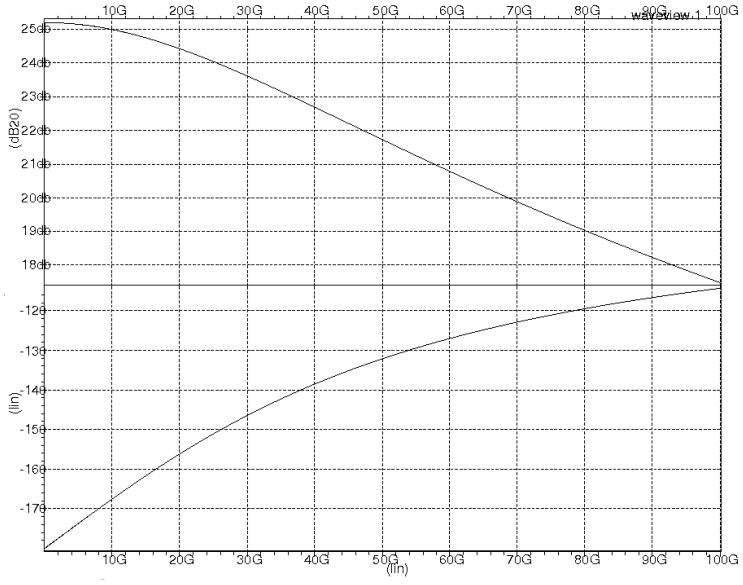


Fig. IV.10. Input Impedance vs Frequency of Cross Coupled Inverters

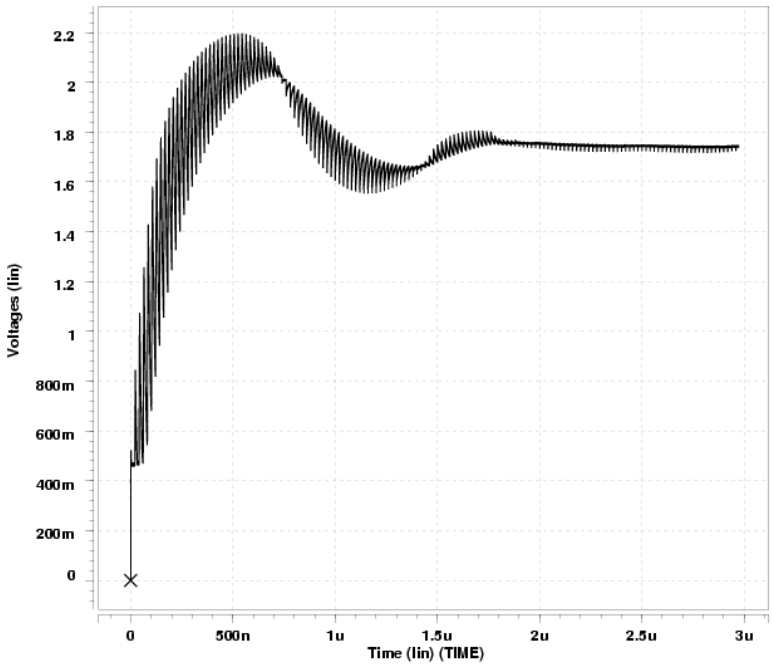


Fig. IV.11. Waveform of Control Voltage

CHAPTER V

DISCUSSIONS

V-A. Longer Standing Wave Resonant Oscillators

The area covered by the standing wave resonant oscillator described in the previous sections is very small compared to the area of a typical digital IC. Hence, there is a requirement to increase the size of the oscillator ring to cover a larger area of the chip. This cannot be achieved by simply increasing the length of the ring, since the frequency of oscillation of the ring decreases (due to increase in its parasitic capacitance and inductance). In this discussion, we propose a way by which the length of the ring can be increased without reducing its frequency of oscillation.

Longer rings which cover a greater area on the chip while not compromising the frequency of oscillation can be built by connecting the transmission lines and the cross-coupled inverters in the configuration shown in the Figure V.1. Figure V.1 shows a two wire standing wave resonant oscillator consisting of three cross-coupled inverter pairs, placed at an equal distance from each other. The distance L between cross-coupled inverter pairs in the longer ring shown in Figure V.1 is equal the length of the standing wave oscillator with one cross coupled pair of inverters. Hence, the length of the ring in Figure V.1 is three times that of an oscillator with one cross coupled pair of inverters but it oscillates at the same frequency. The rings are bootstrapped with a PMOS device as shown in the Figure V.1 to provide the initial condition to the ring for the system to oscillate. In this manner, the ring in Figure V.1 covers $\sqrt{3}$ times the chip area as compared with a ring with just one inverter pair in a similar manner, rings with 5,7,9... inverter pairs can be constructed to cover a larger chip area.

Figures V.2, V.3, and V.4 show the waveforms at various points along the oscillator

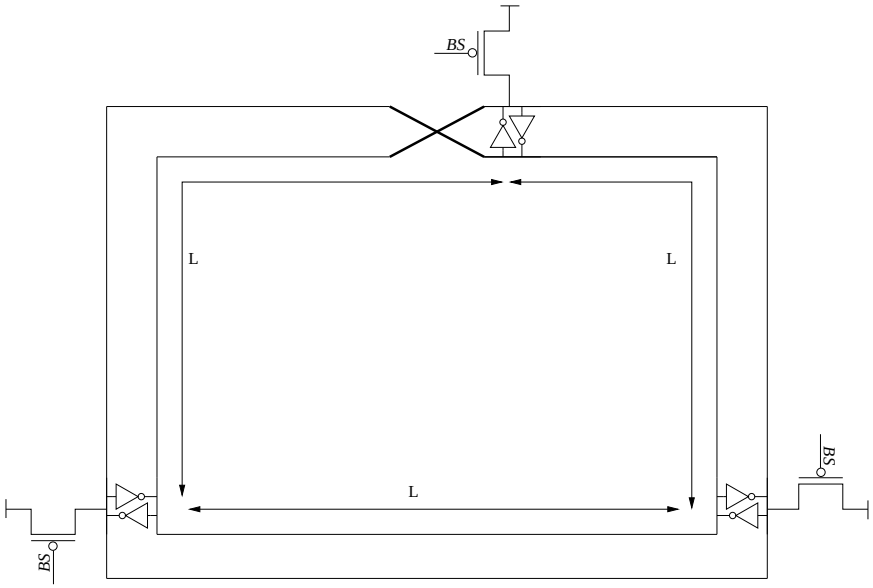


Fig. V.1. Longer Standing Wave Resonant Oscillator

rings with three, five and seven times the length of the ring with one cross coupled pair of inverters. It can be seen that the frequency of oscillation remains constant even with an increase in the total length of the ring. All the simulations were performed using M8 wires, and the distance between the inverter pairs, width and pitch of the wires considered was 1900 μm, 20 μm and 40 μm respectively. The widths of PMOS and NMOS transistors used in the inverters were 300 μm and 125 μm respectively.

V-B. Virtual Ground Options

As we discussed in the previous sections there is a AC null point (virtual ground) at the center of the ring (half way along the length of the ring from the cross coupled inverter pair) in a standing wave resonant oscillator. The phases of the signals on the right and the left of the null point are 180° apart. In the case of the oscillator that we have implemented (with 60 wires) there are three ways by which the virtual zero points of all the wires can be

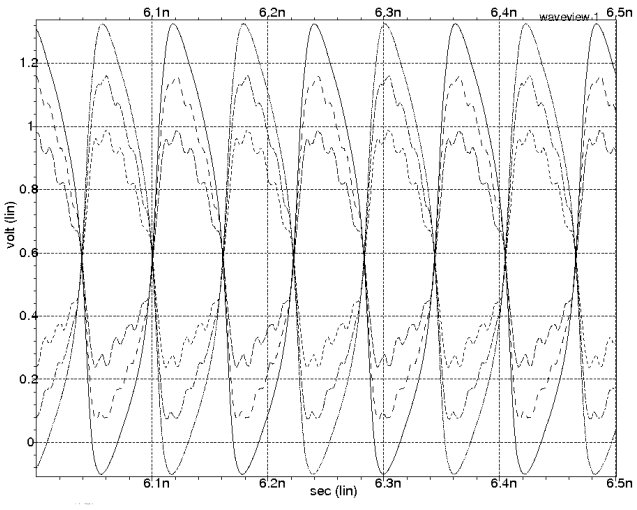


Fig. V.2. Waveforms of Ring Consisting of 3 Cross Coupled Inverter Pairs

connected.

- All the 60 wires are shorted at their virtual ground location (used in the PLL implementation discussed in previous sections).
- Wires are not shorted at virtual ground location, and the wires that are not oscillating as part of the system are left floating.
- Only the wires that are not oscillating as part of the system are shorted, and connected to $V_{DD}/2$.

The frequency of the standing wave resonant oscillator for each of the above three options has been plotted in Figure V.5 for all the 16 coarse configurations considered in our design. It can be observed from the plot that the frequency of oscillation of the ring changes slightly, based on the virtual ground option used. It can also be seen that the range of frequencies covered by the virtual ground option with all the wires shorted provides the maximum oscillator frequency range, and hence we used this in our design.

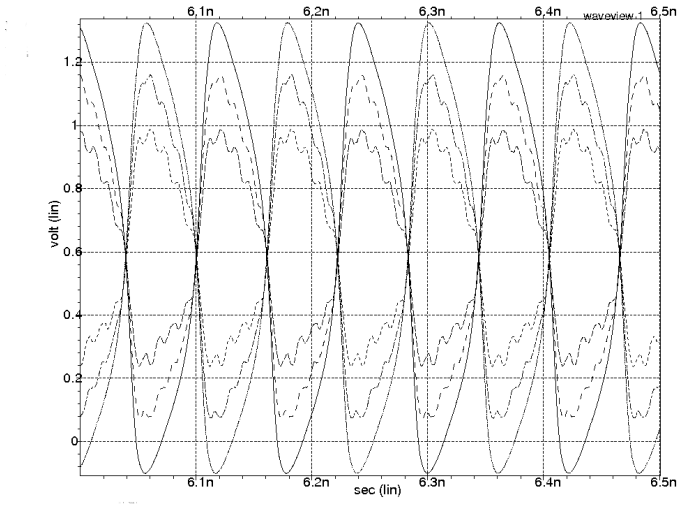


Fig. V.3. Waveforms of Ring Consisting of 5 Cross Coupled Inverter Pairs

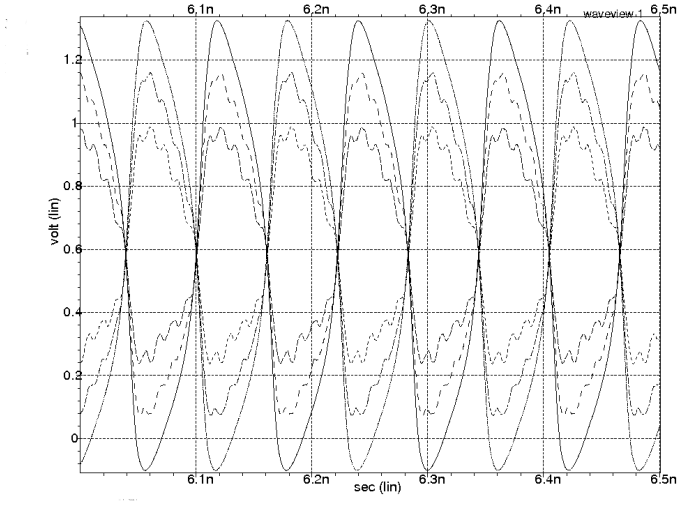


Fig. V.4. Waveforms of Ring Consisting of 7 Cross Coupled Inverter Pairs

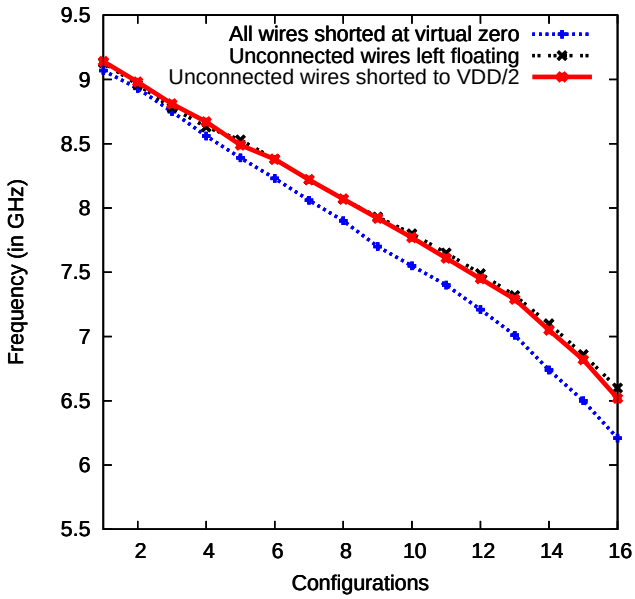


Fig. V.5. Frequency Plot for Virtual Zero Options

CHAPTER VI

CONCLUSIONS AND FUTURE DIRECTIONS

In this thesis, we presented a PLL design, based on a standing wave oscillator, for use in generating the clock signal of a digital IC. The resonant ring is implemented with a plurality of wires connected in a mobius configuration. The oscillation frequency is modulated by coarse and fine tuning. Our oscillator was implemented to provide a continuous frequency response from $\sim$6 GHz to $\sim$9 GHz The length of the ring considered was 1500 μm. Parasitic RLC extractions were performed for the wiring, with skin effect accounted for. The PLL with the standing wave resonant oscillator incorporated was validated, using a 90nm process technology. The total power dissipated in the PLL at lock is about 28.5 mW, of which the oscillator alone dissipates 25 mW, and the jitter observed at lock is 2.56%.

The area covered by a single ring with one cross coupled pair of inverters is much smaller compared to chip size. Therefore a possible future direction is to investigate solutions to distribute clock in a phase locked fashion over wider area on the chip using standing wave resonant oscillators. There are two possible ways by which the oscillator can be made to cover a larger area - a) make rings longer and use more cross coupled inverters as discussed in Chapter V, or b) couple the rings by shorting them at various points. For such an oscillator to be useful for synchronous digital design, it has to be integrated into a PLL. Hence the next main challenge would be to investigate techniques to integrate the bigger oscillator in a PLL. Supplying the analog control voltage to all the cross coupled inverters, and controlling the course configuration circuitry of each of rings in such a coupled oscillator are the key issues to be investigated.

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VITA

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