AN EFFICIENT SUPPLY MODULATOR

FOR LINEAR WIDEBAND RF POWER AMPLIFIERS

A Thesis

by

RICHARD TURKSON

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2011

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee, Jose Silva-Martinez
Committee Members, Edgar Sanchez-Sinencio
Aniruddha Datta
Rainer Fink
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ABSTRACT

An Efficient Supply Modulator for Linear Wideband RF Power Amplifiers.

(August 2011)

Richard Turkson, B.Sc., Kwame Nkrumah University of Science and Technology

Chair of Advisory Committee: Dr. Jose Silva-Martinez

Radio Frequency (RF) Power Amplifiers are responsible for a considerable amount of the power consumption in the entire transmitter-receiver (transceiver) of modern communication systems. The stringent linearity requirements of multi-standard transceivers to minimize cross-talking effects makes Linear Power Amplifiers, particularly class A, the preferred choice in broadband transceivers. This linearity requirement coupled with the fact that the Power Amplifier operates at low transmit power during most of its operation makes the efficiency of the entire transceiver poor. The limited transceiver efficiency leads to a reduction in the battery life of battery operated portable devices like mobile phones; hence drastically limiting talk time. To alleviate this issue, several research groups propose solutions to improve PA power efficiency. However, these solutions usually have a low efficiency at low power and are mostly limited to narrow bandwidth applications.

In this thesis, the efficiency of a class A Power amplifier in wideband wireless standards like WiMax is improved by dynamically controlling the bias current and supply voltage of the PA. An efficient supply modulator based on a switching regulator architecture is proposed for controlling the supply voltage. The switching regulator is found to be slew-limited by the bulky inductor and capacitor used to regulate the supply voltage. The proposed solution alleviates the slew rate limitation by adding a bang-bang controlled current source. The proposed supply modulator has an average power efficiency of 81.6% and is suitable for wireless standards with bandwidths up to 20MHz

compared to the relatively lower efficiencies and bandwidths of state of the art modulators. A class-A PA is shown to promise an average power efficiency of 21.3% when the bias current is controlled dynamically and the supply voltage is varied using the proposed supply modulator. This is a significant improvement over the poor average efficiency of 1.06% for a fixed bias conventional linear class A PA.

The project has been simulated using the TSMC 0.18μm technology.

to my mother and the memory of my late father

ACKNOWLEDGEMENTS

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1. INTRODUCTION

Radio Frequency (RF) Power Amplifiers (PAs) are at the heart of every wireless system playing a key role in transmitting information between places for communication purposes. These forms of communication could be between mobile phone handsets, base stations, computers or Bluetooth devices. The role of the PA is to greatly amplify the power of the baseband signal to be transmitted to make it capable of driving the low impedance of the antenna in the transmitter. However, the PA consumes most of the power in the entire transmitter-receiver (transceiver). In a mobile phone handset, the PA alone consumes about 40% of the entire battery energy [1]. Additionally, the PA suffers from a poor efficiency especially when transmitting low power. A high power consumption and poor efficiency reduces battery life, which is very critical in portable devices like mobile phones and laptop computers. A reduced battery life reduces talk time in mobile phone handsets and will require the mobile phone to be recharged frequently after the battery has been run down. This issue of poor power efficiency is also critical in base stations where high efficiency and low power consumption is important in determining the size of heat sinks for cooling purposes. As a result of all these issues, there is an increased focus on improving the power efficiency of PAs in the wireless industry.

Figure 1.1 shows the front end of a typical wireless transmitter. It shows the main building blocks that make up the transmitter. The typical transmitter mainly consists of a Digital Signal Processor (DSP), a supply modulator (or regulator), frequency synthesizer, RF mixer and the PA. The DSP generates the baseband signal (information to be transmitted) and the envelope signal (outline of the peak variations in the baseband signal). The information generated by the DSP is in digital format and requires a Digital to Analog Converter (DAC) to convert it to its analog equivalent. The frequency synthesizer generates an RF signal hich serves as the carrier for transmitting the

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This thesis follows the style of the *IEEE Journal of Solid-State Circuits*.

baseband signal. The generated RF signal is mixed with the baseband signal to generate a high frequency modulated signal which is transmitted by the PA. The supply regulator (or modulator) generates the proper supply voltage demanded by the PA using the envelope signal. The supply voltage is often modulated by the envelope of the baseband signal in order to control the dc power consumption of the PA, and to make its power consumption proportional to the transmit signal power. This way of modulating the supply voltage is typically how efficiency is improved in PAs; these techniques will be discussed in Section 2.

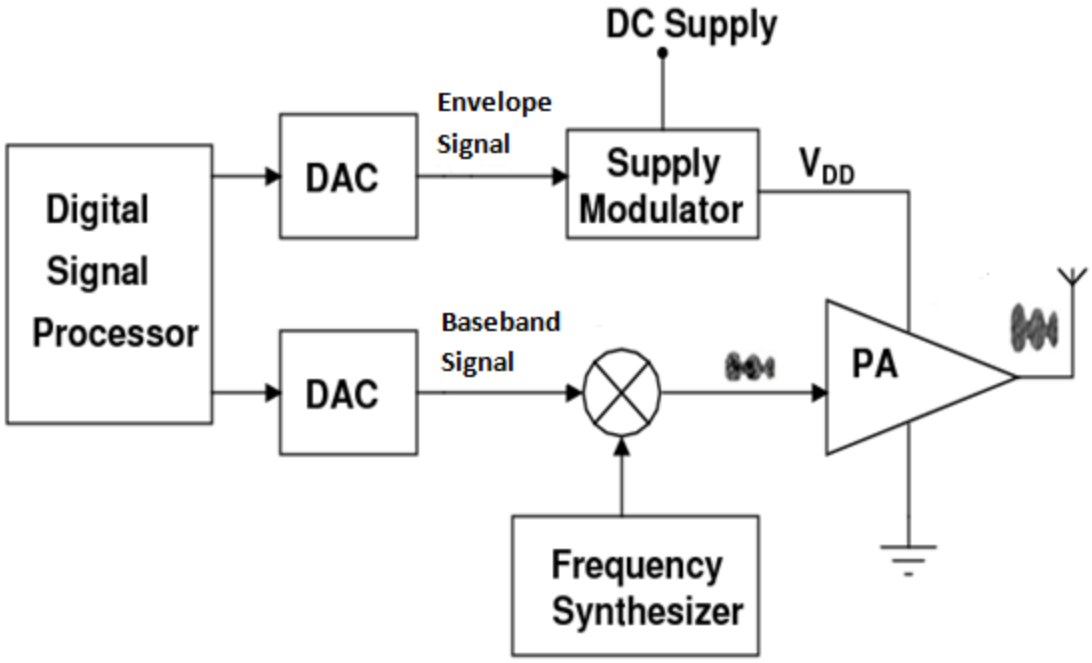


Figure 1.1 Simplified Block Diagram of a Transmitter Front End

One reason for the poor power efficiency of the PA is the nature of the baseband signal used in modern wireless systems. Thus we look at the current trend in wireless communication systems and how the nature of the baseband signal affects system performance in the next section.

1.1 System Design Considerations

The demand by consumers for high quality high-speed data in wireless systems has led to the transmission of information at faster rates while maintaining high linearity in the wireless industry. This requires the use of modulation schemes with higher data rates which results in the baseband information having high peak to average power ratio (a parameter which gives an indication of the peak power transmitted to the load compared to the average power transmitted to the load). The problem here is that the peaks in the information are infrequent but in order to accommodate the entire dynamic range of the baseband signal while maintaining high linearity, the PA needs is biased with a high quiescent current which increases the static power consumption of the PA. Thus the PA is not optimized for the transmission of average power as far as power efficiency is concerned. This issue will become clearer in Section 2. Table 1.1 shows a summary of some wideband wireless standards with their bandwidths and peak to average power ratio.

Table 1.1 Wireless Standards Showing their Peak to Average Power Ratio and Channel Bandwidth

Standard	Peak to Average Power Ratio	Channel Bandwidth
EDGE	3.2dB	200 kHz
CDMA	4-9 dB	1.25 MHz
WCDMA	3.5-7 dB	3.84 MHz
WLAN	10 dB	20 MHz
WiMax	10-12 dB	1.25 MHz – 20 MHz

This table shows an increasing trend in the bandwidth and peak to average power ratio in wireless systems, with WLAN and WiMax currently being the standards of choice. Power management techniques typically using a supply modulator to control the

supply voltage of the PA are required to optimize the PA for average power transmission and hence improve power efficiency. However, the design of the supply regulator (or modulator) becomes particularly challenging since it requires large and fast variations in the supply voltage and as a result is the focus of this thesis. In this thesis, a switching regulator architecture is proposed for use as a supply modulator. The challenges in designing efficient switching regulators for high speed applications are identified as a trade-off between output ripple voltage, slew rate, bandwidth and power efficiency. The inherent slew rate of the switching regulator is found to be limited by the bulky output inductor and capacitor used to regulate the supply. Efficient circuit techniques are needed to improve the limited slew rate of the switching regulator to prevent the peaks of the signal transmitted from being distorted. In this work, the switching regulator is designed to optimize its bandwidth and power efficiency for average power transmission. A bang-bang controlled current source is added to the switching regulator to improve its speed without compromising the ripple performance, stability and power efficiency of the system.

The thesis is organized as follows.

1.2 Thesis Organization

The main objective of this thesis is to develop power management techniques for improving the efficiency of linear PAs. A switching regulator architecture is identified as the preferred supply modulator in this thesis. The main challenge in designing an efficient switching regulator for this application is identified as power efficiency and the trade-off between ripple voltage and limited slew rate. As a result an efficient technique for enhancing the slew rate of switching regulators without sacrificing ripple performance that makes them applicable for use in variable output supply modulators is proposed.

Section 2 introduces linear Power Amplifiers. The Section begins with some basic metrics such as probability density functions, power consumption and average power efficiency which are associated with PAs. Next class A and B PAs are discussed

along with their efficiency limitations. The Section concludes with a discussion on dynamic biasing of PAs to enhance their efficiency.

Section 3 discusses supply modulators. The existing supply modulator architectures are discussed. Next buck switching regulators used as variable supply modulators are discussed. The main parameters associated with switching regulators such as bandwidth, ripple voltage and slew rate are discussed along with the bottlenecks in designing high speed switching regulators. These issues involve a tradeoff between ripple voltage, slew rate and regulator bandwidth. The limitations in the existing techniques such as quiescent power consumption, stability and power efficiency are discussed and an efficient bang-bang solution is then proposed to overcome its slew rate limitation. The proposed technique does not degrade the efficiency and the stability of the switching regulator.

Section 4 discusses the main design considerations in the transistor level implementation of the proposed supply modulator. Schematic simulation results in CADENCE are presented to demonstrate the feasibility of the proposed approach.

In Section 5, conclusions are made and the scope for future work in the thesis is discussed.

2. FUNDAMENTALS OF LINEAR POWER AMPLIFIERS

In this section the fundamentals of Linear PAs are discussed. The section starts with definitions of some basic terms and metrics such as probability density function, average power consumption and average efficiency which are associated with PAs. Next class-A and class-B PAs are discussed along with their efficiency limitations to emphasize the problem of poor efficiency. The section concludes with a discussion on dynamic biasing of PAs to enhance their efficiency.

2.1 Basic Definitions

This section provides some basic definitions of terms such as the envelope of a signal, conduction angle, peak-to-average-power-ratio, probability density function, average power and average efficiency.

2.1.1 Conduction Angle

If a sinusoidal signal is applied to the gate of a transistor, then the portion of the period of the sinusoidal signal that causes the transistor to conduct current in the drain is referred to as conduction angle. For instance, if the entire period of the sine wave causes the transistor to conduct then the conduction angle is 360^{o}. This term is usually used to distinguish between power amplifiers.

2.1.2 Envelope of a Signal

The envelope of a signal refers to the outline of the signal's peak variations. Consider an amplitude modulated signal, y(t), obtained by mixing a signal containing the message to be transmitted, $m(t)=\cos(\omega_m t)$, with an RF signal, $y_{RF}(t)=\sin(\omega_{RF} t)$.

$$y(t) = y_{RF}(t).m(t) \tag{2.1a}$$

$$y(t) = \sin(\omega_{RF} t).\cos(\omega_m t) \tag{2.1b}$$

$$y(t) = \sin(\omega_{RF} + \omega_m)t + \sin(\omega_{RF} - \omega_m)t \tag{2.1c}$$

The resulting signal and its envelope are shown in Figure 2.1.

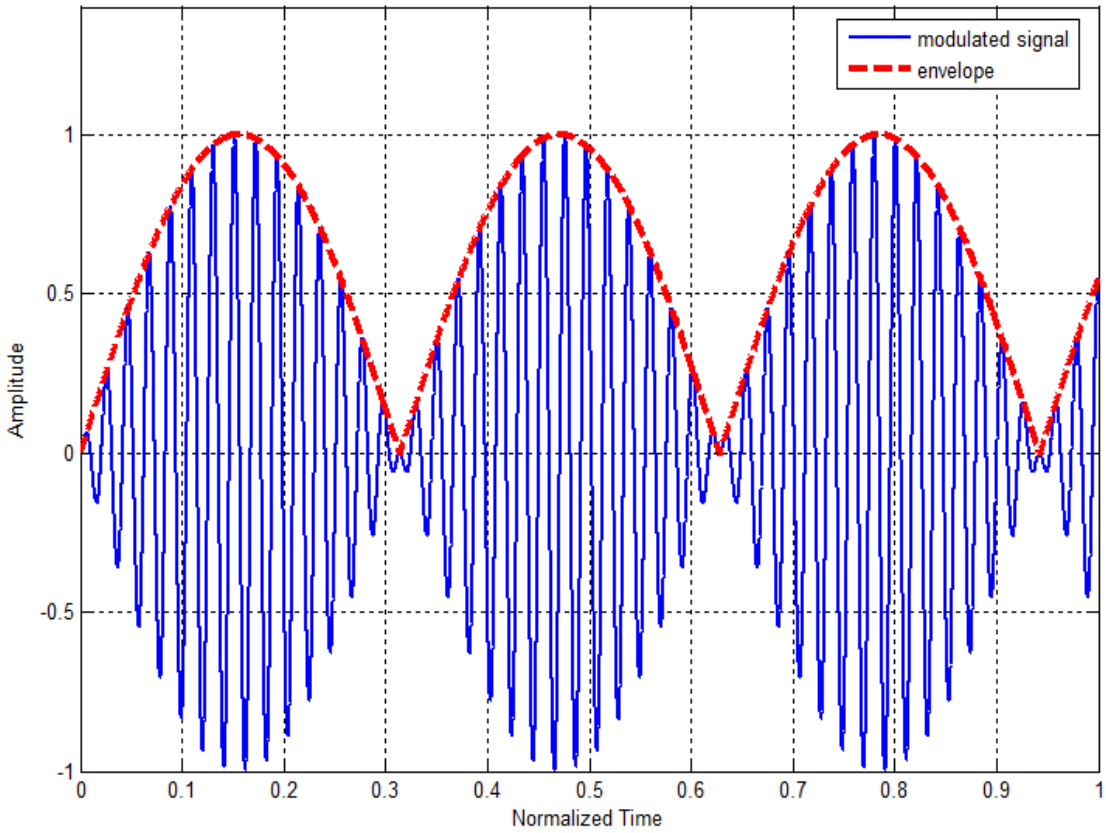


Figure 2.1 Plot of Modulated RF Signal and its Envelope

It should be noted that in this work, input envelope signal is used to refer to the envelope of the input baseband signal to be transmitted and output envelope signal is used to refer to the envelope of the output signal delivered to the load. The input envelope and output envelope signals are very important in improving efficiency. The role that they play in improving efficiency will be become evident in Section 2.3.

2.1.3 Probability Density Function and Cumulative Distribution Function

Probability density function and Cumulative distribution function are statistical parameters that are used to indicate the likelihood or tendency of occurrence of an event. For various wireless standards, the probability density function provides use case

information which indicates the probability of operating at a particular power level while the cumulative distribution function indicates the probability of transmitting power less than a particular power level. Figure 2.2 shows the probability distribution function of CDMA. This plot shows that during most of the operation of a CDMA handset, the power transmitted is less than 16dBm. To get more insight, we consider the cumulative distribution function of CDMA in Figure 2.3. It shows that the probability of transmitting power less than 16dBm is actually 90%. Similar trends have been observed for other relevant wireless communication standards[2]. Consequently, there is an increased focus on improving mid-power (16dBm) efficiency in the semiconductor industry[3]. Thus, any optimizations in the efficiency of a PA for CDMA handsets should be focused on power levels around and below 16dBm.

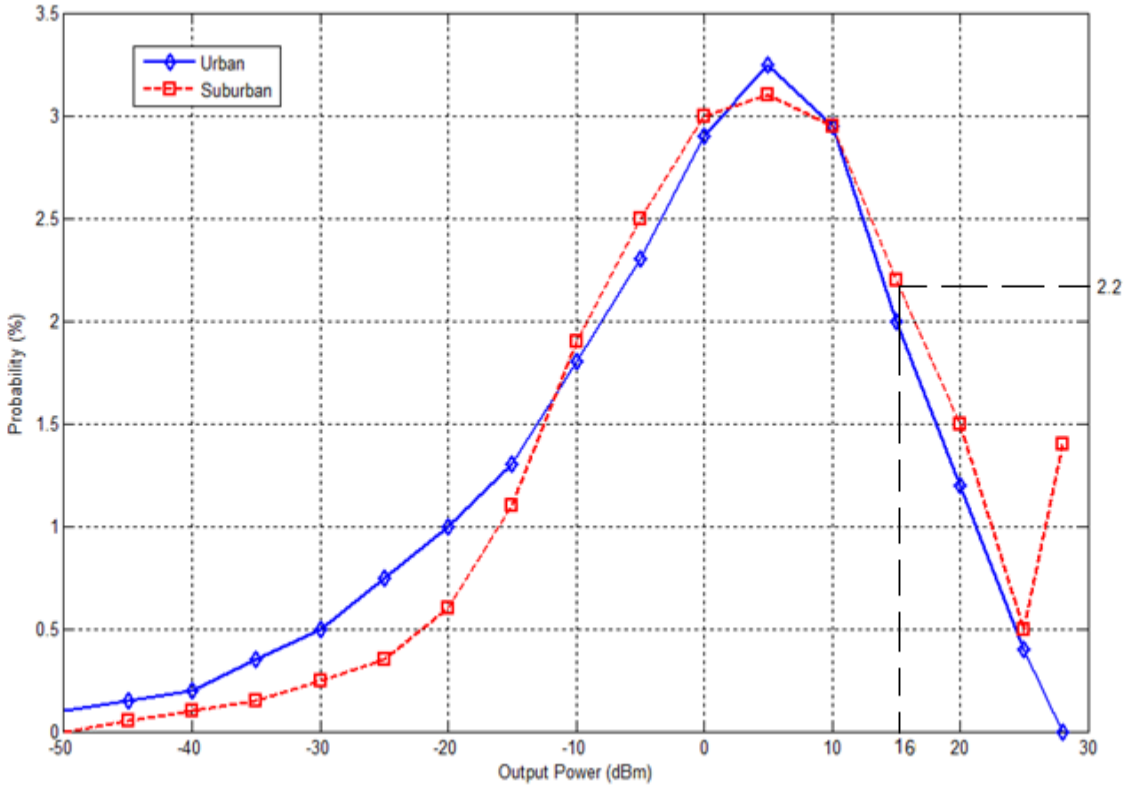


Figure 2.2 Probability Distribution Function of a Typical CDMA Transmit Signal [4]

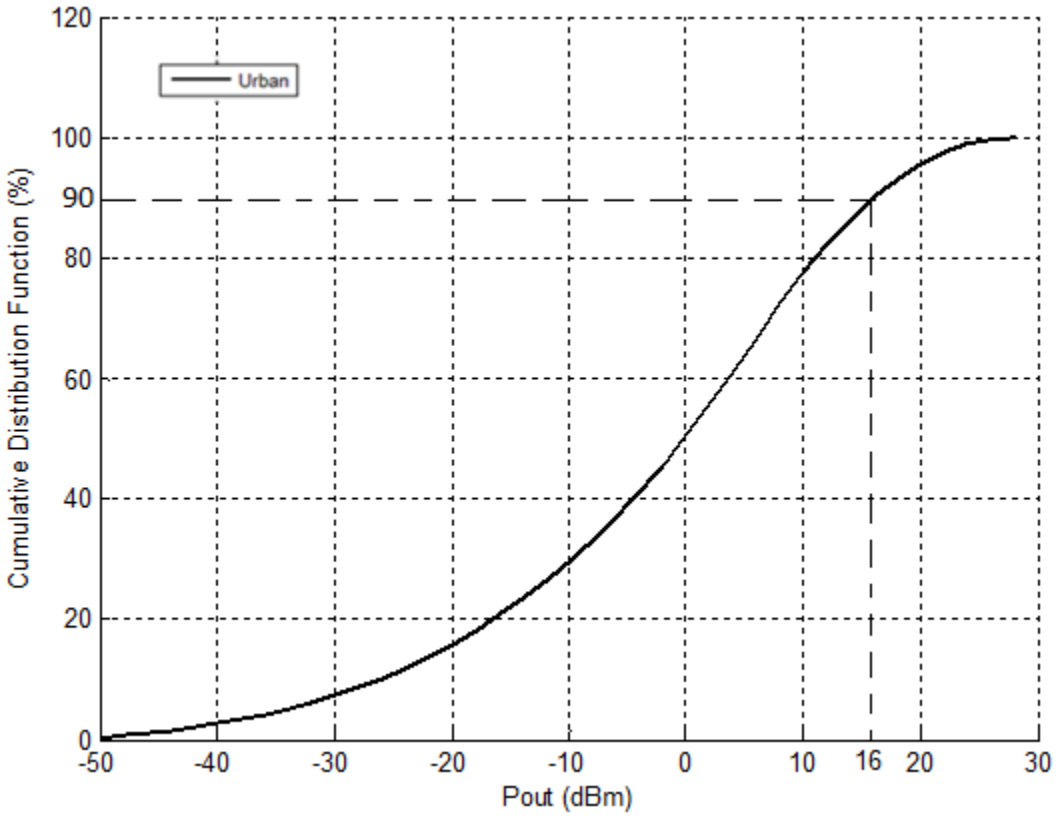


Figure 2.3 Cumulative Distribution Function of a Typical CDMA Transit Signal

2.1.4 Peak to Average Power Ratio

The peak to average power ratio (PAPR) is the ratio of the peak value of the power transmitted to the average value of the power. The signals transmitted by PAs in modern wireless communication systems employ different coding schemes to optimize the signal bandwidth in order to obtain the best possible bit-error-rate, and as a result may have PAPRs as high as 12dB. The problem with having a high peak to average power ratio is that the PA will need to have the power capability to transmit the peak power even though in average the PA transmits at low power[5]. Referring to the probability distribution function of CDMA in Figure 2.2, we notice that the probability of transmitting at peak power is actually 0.01%[6]. Clearly, this suggests that the PA is not optimized to transmit the average power and as a result the full-power capability of the PA is wasted leading to a poor power efficiency. The effect of this parameter on the

power efficiency of the PA will become clearer when linear PAs are discussed in Section 2.2.

2.1.5 Average Power Transmitted

The power transmitted by the PA in a CDMA handset is variable. Based on use case data in Figure 2.2, it was noticed that the power transmitted by the PA is mostly less than 16dBm. Consequently, the average power transmitted is a metric which gives a good indication on how the PA is used. It is given by

$$P_{ave,rf} = \int_{-\infty}^{+\infty} P_{out} \cdot p(P_{out}) dP_{out} \tag{2.2}$$

where P_{out} is the RF power transmitted and $p(P_{out})$ is the probability of transmitting power, P_{out}.

2.1.6 Average Power Consumption

The average dc power dissipated by the PA is given by

$$P_{ave,dc} = \int_{-\infty}^{+\infty} P_{dc}(P_{out}) \cdot p(P_{dc}) dP_{out} \tag{2.3}$$

where $P_{dc}(P_{out})$ is the dc power used at P_{out} and $p(P_{dc})$ is the probability of consuming Power, P_{dc}, when transmitting P_{out}. If the dc power consumed by the PA is constant (i.e. independent of the power transmitted) then, $P_{dc}(P_{out})=P_{dc}$ and

$$P_{ave,dc} = P_{dc} \int_{-\infty}^{+\infty} p(P_{dc})\, dP_{out} = P_{dc} \tag{2.4}$$

As a result the average static power consumed by a PA with a fixed bias is the same as the static power used to bias the PA. Also, if the drain supply voltage of a PA is varied such that it is proportional to the envelope signal under all operating conditions then $p(P_{dc})=p(P_{out})$ and the average dc power dissipated by the PA becomes

$$P_{ave,dc} = \int_{-\infty}^{+\infty} P_{dc}(P_{out}) \cdot p(P_{out}) dP_{out} \tag{2.5}$$

This is what we seek to achieve with efficiency enhancement techniques which are discussed in Section 2.3.

2.1.7 Average Power Efficiency

Since PAs rarely operate at peak power, using peak power efficiency to compare the different power amplifiers is not a fair comparison. A metric which gives a good indication of battery life and as a result is extremely important in choosing an optimum PA architecture especially for transmission of variable envelope signals is the average power efficiency. It is given by the ratio of average power transmitted to the dc power used by the PA. It is expressed as

$$\eta_{ave} = \frac{P_{ave,rf}}{P_{ave,dc}} = \frac{\int_{-\infty}^{+\infty} P_{out} \cdot p(P_{out}) dP_{out}}{\int_{-\infty}^{+\infty} P_{dc}(P_{out}) \cdot p(P_{dc}) dP_{out}} \quad (2.6)$$

2.2 Classification of Linear Power Amplifiers

A linear power amplifier attempts to preserve the original wave shape of the input[7]. Linear power amplifiers may be classified as class A or AB according to the conduction angle of the drain current. Class A and B PAs are explained in the following section.

2.2.1 Class A PA

The conduction angle of a class A PA is 360^{o}.This implies that the operating points are such that current continuously flows through the output device at all times. As a result, class A PAs are usually very linear. Figure 2.4 shows the schematic of a simplified class A PA with waveforms at the input and output. V_{DC} is the dc supply voltage, I_{DC} is the dc current to the PA, V_{GS} is the gate bias voltage, v_{gs} is the ac component of the input signal, v_{GS} is the combination of V_{GS} and v_{gs} and v_o is the RF output voltage.

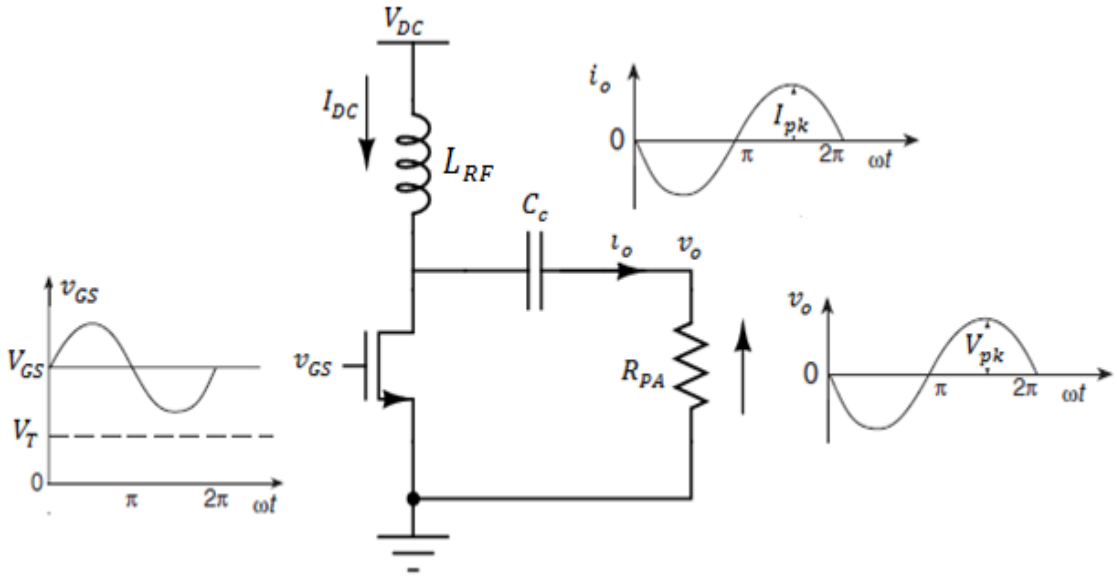


Figure 2.4 Schematic of a Simplified Class A PA with Input and Output Waveforms

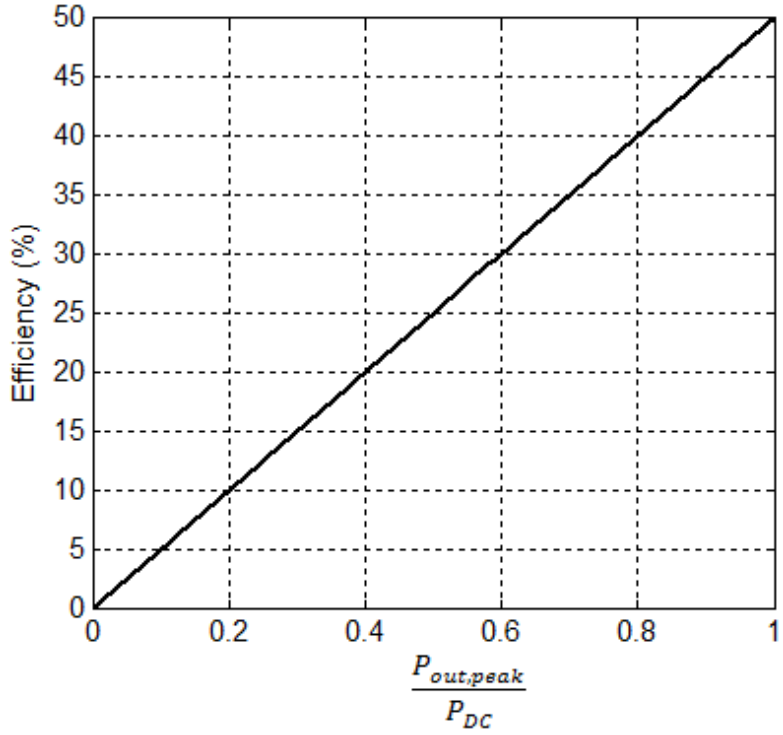
A class A PA has a fixed bias current,$I_{DC,}$ and supply voltage,V_{DC}. Hence its static power consumption is fixed. The power efficiency is defined as the ratio of the average value of the power delivered to the load to the DC power consumed by the PA expressed as a percentage. This is given by

$$\eta_A = \frac{P_{out}}{P_{DC}} \tag{2.7a}$$

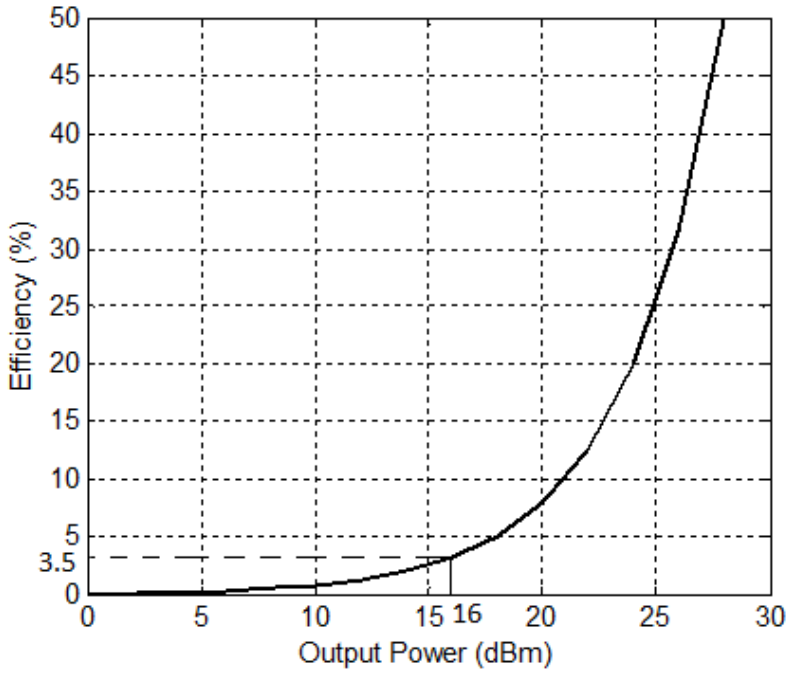
$$\eta_A = \frac{I_{pk}.V_{pk}}{2.I_{DC}.V_{DC}} \tag{2.7b}$$

$$\eta_A = \frac{P_{out,peak}}{2.P_{DC}} \tag{2.7c}$$

As a result the efficiency of a PA operating in class A is directly proportional to the power delivered to the load. Thus the PA power efficiency degrades as the output power reduces. It achieves a maximum efficiency of 50% only when transmitting at maximum power. Figure 2.5(a) and 2.5(b) show how the efficiency of a class-A amplifier varies with output power.



(a)



(b)

Figure 2.5 Plot of Power Efficiency of a Class A PA with (a) Normalized Power and (b) Output Power in dBm

From the plots, it is noticed that a class A PA with the capability to transmit 28dBm of power has efficiency less than 3.5% when the power transmitted is less than 16dBm. When a class A PA is used in a 28dBm CDMA handset, its average efficiency will be given by

$$\eta_{ave} = \frac{\int_{-50dBm}^{28dBm} P_{out} \cdot p(P_{out}) dP_{out}}{P_{dc}} \quad (2.8)$$

Using numerical integration in MATLAB with $p(P_{out})$ obtained from the probability distribution function of CDMA in Figure 2.2, the average efficiency is computed as $\eta_{ave} = \frac{0.0186}{0.631} = 2.91\%$.

Even though the class-A PA has a peak power efficiency of 50%, when used in a modulation scheme with high PAPR like CDMA the average efficiency is limited to less than 3%. Thus, finding linear PA architectures with better power efficiency figures is mandatory to extend the talk time of existing services.

2.2.2 Class B PA

The conduction angle of a class-B PA is 180^o. This implies that the operating points are such that current flows through the output device(s) for half the time. As a result, a class-B PA has theoretically zero quiescent current. Figure 2.6 shows the schematic of a simplified single transistor class B PA with waveforms at the input and output.

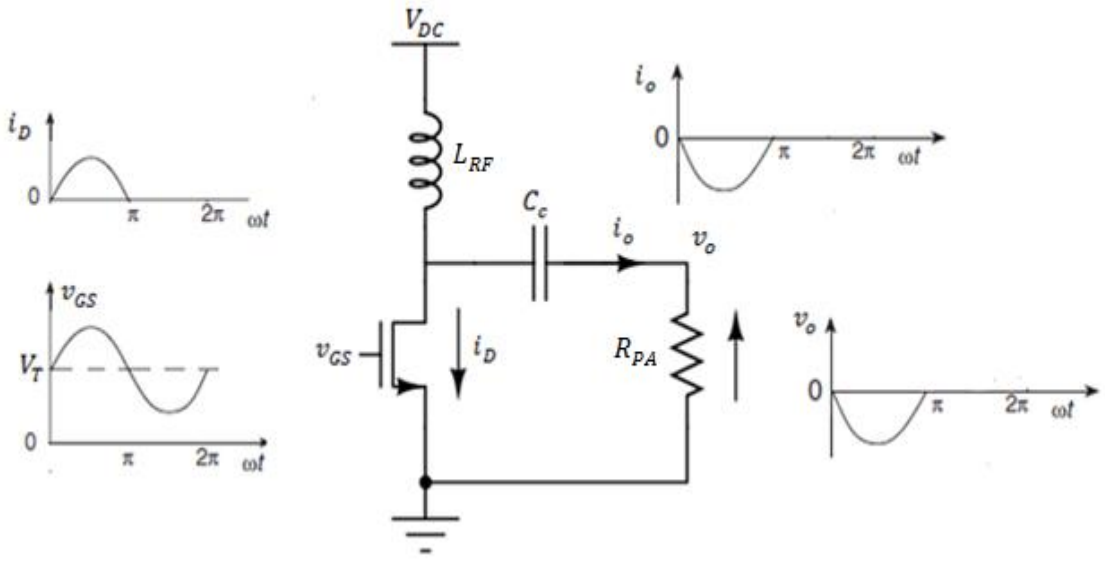


Figure 2.6 Schematic of a Class-B PA with Input and Output Waveforms

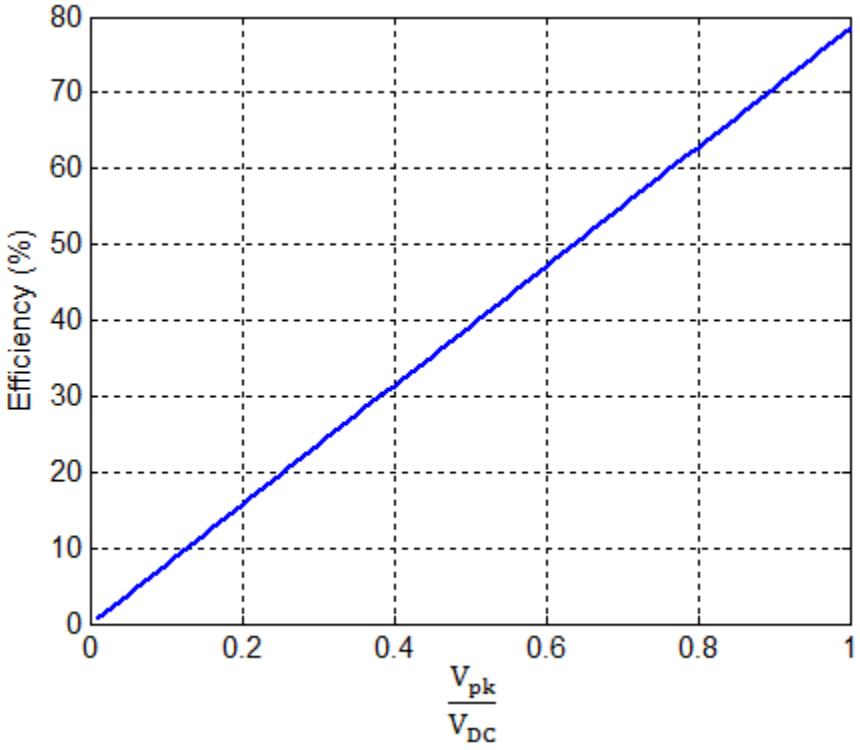
The average value of the drain current is proportional to the magnitude of the input signal. It is given by

$$I_{ave} = \frac{I_{pk}}{\pi} \tag{2.9}$$

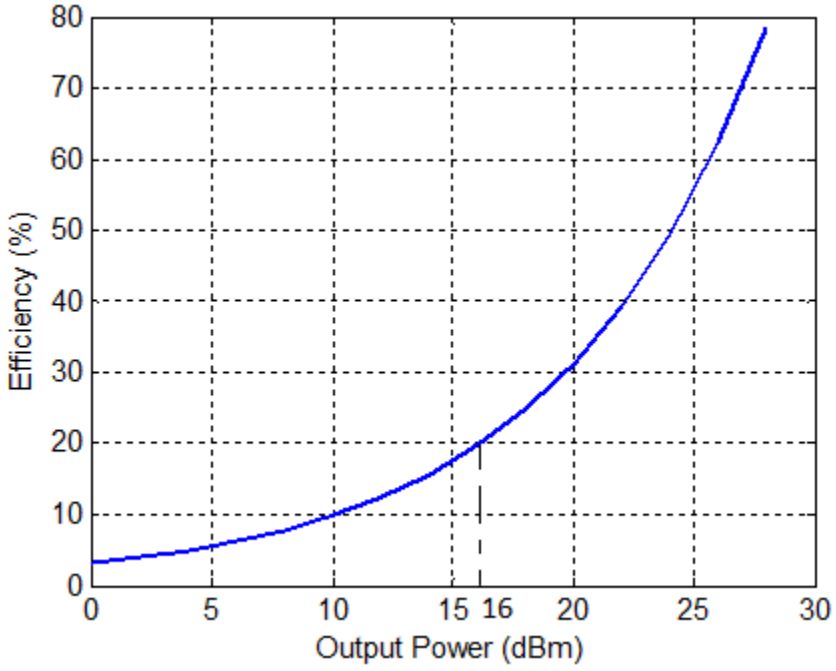
This makes class-B PAs more efficient than class A PAs. However, this benefit is achieved at the price of increased distortion since the class-B amplifier operates as a half-wave rectifier. Thus, the efficiency of a class B PA is given by [8]

$$\eta_B = \frac{\pi}{4}\frac{V_{pk}}{V_{DC}} \tag{2.10}$$

Thus the efficiency of a class-B PA is proportional to the amplitude of the signal delivered to the load. It achieves a peak efficiency of 78.5% when transmitting at maximum power. Figure 2.7(a) and 2.7(b) show how the efficiency of a class-B PA varies with the amplitude of the signal transmitted and the output power respectively.



(a)



(b)

Figure 2.7 Plot of Efficiency of a Class B PA vs. (a) V_{pk}/V_{DC} (b) Output Power

In summary, class B PAs are more efficient but less linear than class A PAs. A class B PA with the capability to transmit up to 28dBm of power has efficiency below 20% when the power transmitted is less than 16dBm. For CDMA handset applications, the class B PA average efficiency will be given by

$$\eta_{ave} = \frac{\int_{-50dBm}^{28dBm} P_{out} \cdot p(P_{out}) dP_{out}}{\int_{-50dBm}^{28dBm} P_{dc}(P_{out}) \cdot p(P_{dc}) dP_{out}} \tag{2.11}$$

Using numerical integration in MATLAB with $p(P_{out})$ obtained from the probability distribution function of CDMA in Figure 2.2 and $p(P_{dc}) = p(P_{out})$ since the bias current of the class B PA varies at the same rate as the envelope signal, the average efficiency is calculated to be 24.8%. It should be noted that the relatively high efficiency of the class B PA is achieved at the detriment of reduced linearity. The half-wave sinusoidal signal produced by the class B PA presents significant harmonic content which prevents them from being used in a CDMA handset. A Fourier series expansion of the half-wave sinusoid reveals the following harmonic components

$$v_o(t) = \frac{V_{pk}}{\pi} + \sum_{n=1}^{\infty} [a_n \cos(n\omega t) + b_n \sin(n\omega t)] \tag{2.12a}$$

where ω is the fundamental frequency, n is an integer and

$$a_n = \begin{cases} 0 & \text{if n is odd} \\ \dfrac{-2}{\pi(n^2-1)} & \text{if n is even} \end{cases} \tag{2.12b}$$

$$b_n = \begin{cases} 0.5 & \text{if n} = 1 \\ 0 & \text{if n is even} \end{cases} \tag{2.12c}$$

These non-linearities introduce spurs into adjacent communication channels which interferes with their proper operation[4]. Thus an alternative PA architecture with high linearity and a good average efficiency is needed.

The next section discusses some of the techniques that can be used to improve the efficiency of the linear PAs.

2.3 Efficiency Enhancement Techniques

In the previous section, it was realized that the efficiency of PAs is very limited. Efficiency enhancement techniques such class G and dynamic biasing can be used to improve the power efficiency of PAs but often at the expense of increased system complexity, silicon area and reduced linearity. However, these trade-offs are acceptable and as a result these techniques are widely used for improving the power efficiency of PAs. These methods are considered next.

2.3.1 Class G

From equation (2.7b), it is noticed that the efficiency of the linear power amplifier is the product of the current efficiency (I_{pk}/I_{DC}) and voltage efficiency (V_{pk}/V_{DC}) of the power amplifier normalized by 2. The goal of the class G technique is to ideally make the voltage efficiency 100%. In the class G technique, multiple supply voltages are made available to the PA and one supply voltage selected at a time according to the level of the envelope signal such that the supply selected is ideally equal to the magnitude of the output signal delivered to the load. If an infinite number of supply voltages are made available to the PA, then the supply voltage to the PA becomes continuous and the 100% voltage efficiency can be achieved under all operating conditions. However each additional supply needs to be generated which increases the cost and system complexity greatly if many supply voltage are used. As a result, practical class G's are usually limited to two supply voltages. Figure 2.8 shows a simplified schematic of a PA supply using the class G technique.

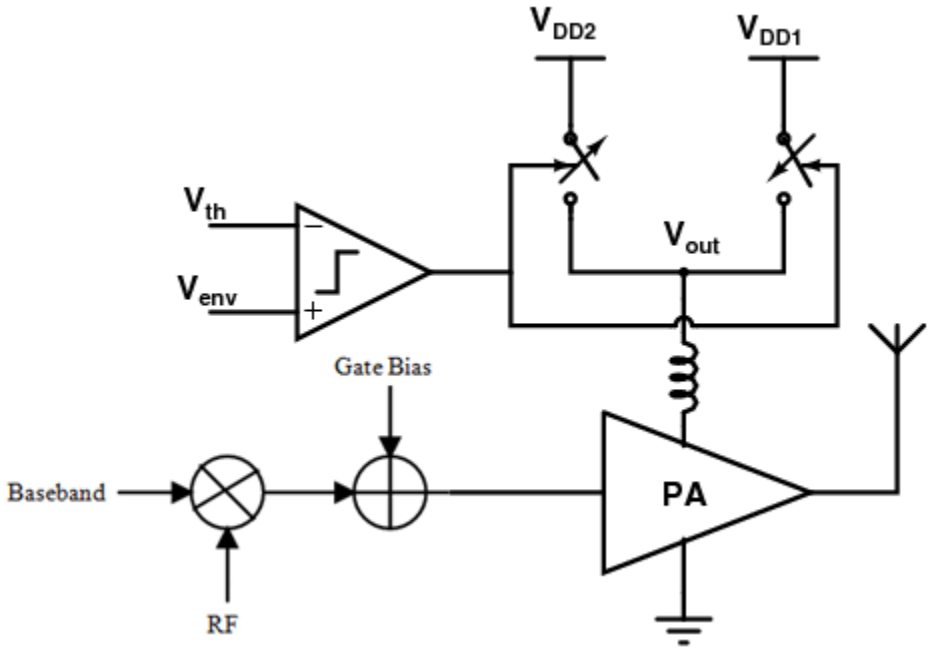


Figure 2.8 Simplified Schematic of a Class G Supply Modulated PA

In class G, the envelope signal is compared with a threshold voltage, V_{th}. When the envelope signal is less than V_{th}, a lower supply voltage (V_{DD2}) is selected and when the envelope signal is greater than V_{th} a higher supply voltage (V_{DD2}) is selected. The class G can be used for wideband applications since its speed response can be as fast as a clock period. However, it relies on appropriately choosing V_{th} so that the lower supply voltage is used most of the time in order to guarantee a high efficiency. Figure 2.9 shows how efficiency varies with output power in a class G modulator with V_{th} chosen to optimize efficiency at 16dBm.

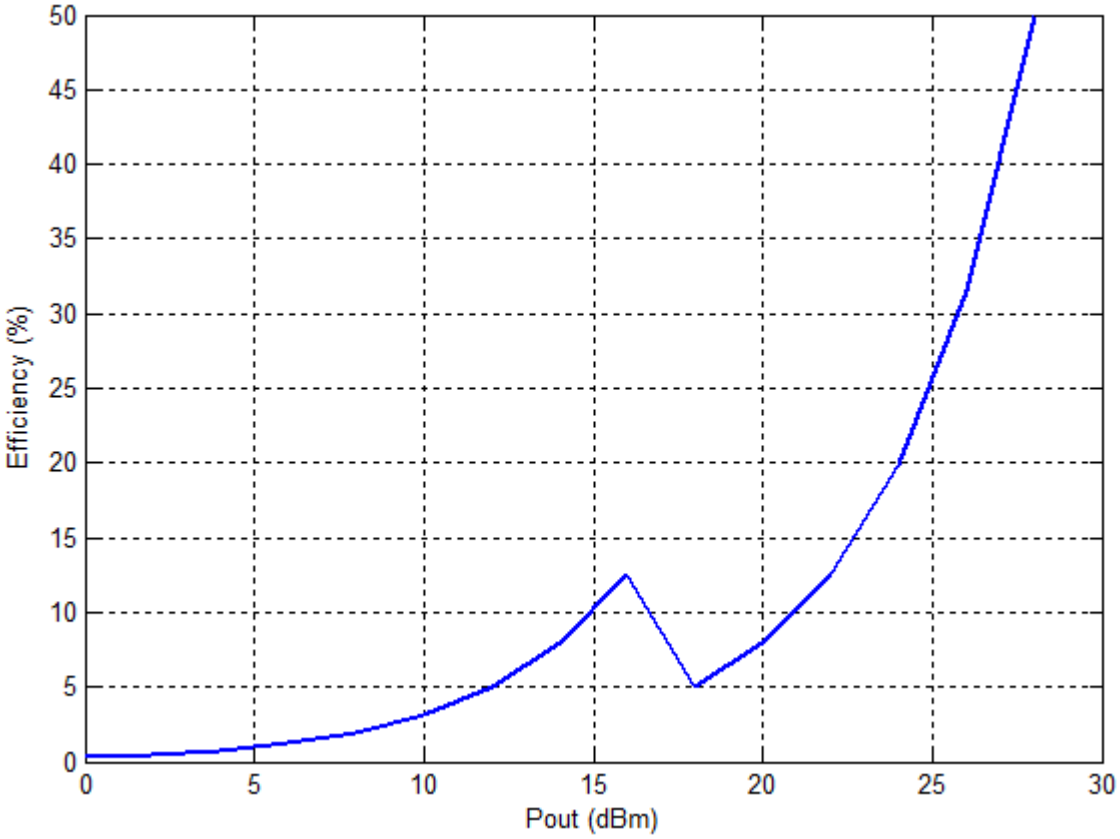


Figure 2.9 Variation of Efficiency with Output Power of a Class G Modulated PA

Note that the additional supply will not be generated with 100% efficiency and as a result further degrades the efficiency of the PA. A practical implementation of this technique is shown in reference [9]. It achieves an average power efficiency of 22.6% with an efficient non-linear PA.

2.3.2 Dynamic Drain Biasing

From the previous section, it was realized that a limitation to the class G technique was the fact that it was impractical to generate an infinite number of power supplies. A way around this problem is to use a continuously variable supply voltage by using Dynamic Drain Biasing. From equation (2.7b), if V_{DC} is varied such that $V_{DC}=V_{pk}$ under all operating conditions then the efficiency of the class A PA becomes

$$\eta_A = \frac{I_{pk}}{2I_{DC}} \tag{2.13}$$

Notice that this assumption is idealistic and unrealistic since the amplifier requires an overdriving drain-source voltage to operate properly. As a result, in a real implementation V_{DC} will be actually greater than V_{pk}. A supply modulator is required to vary the drain supply voltage. Figure 2.10 shows a simplified schematic illustrating the concept of dynamic drain biasing. The output envelope signal is applied to the input of the supply modulator for it to vary the drain voltage of the PA according to the level of the envelope signal.

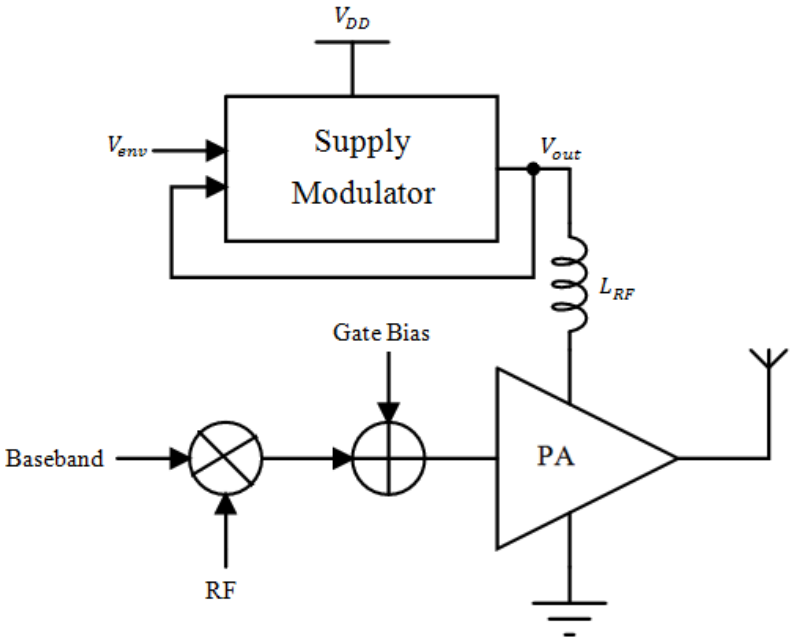


Figure 2.10 Simplified Schematic Illustrating Dynamic Drain Biasing

2.3.3 Dynamic Gate Biasing

The techniques discussed thus far seek to improve the voltage efficiency of the power amplifier without improving the current efficiency. The bias current of a PA is controlled by its gate bias voltage. As a result dynamic gate biasing can be used to improve the current efficiency of the power amplifier. This involves varying the bias

current of the PA according to the level of the baseband signal such that ideally $I_{DC}=I_{pk}$ under all operating conditions. If this is achieved, then the efficiency of the linear PA becomes

$$\eta_A = \frac{V_{pk}}{2V_{DC}} \tag{2.14}$$

Note that this will not be achieved in a real implementation since a bias current higher than peak current will be required for the PA to operate properly. The resulting efficiency then becomes similar to the class B example with the efficiency proportional to the amplitude of the signal delivered to the load. The gate bias voltage is varied with the envelope of the baseband signal and as such simple circuit components requiring little power consumption is needed. As a result dynamic gate biasing is simple to implement. However, varying the bias current causes variations in the gain of the PA and as a result introduces power gain non-linearities. To gain insight into this, note that the voltage gain of the power amplifier is given by

$$G = g_m . R \tag{2.15a}$$

$$G = R. \sqrt{2k_n \frac{W}{L} I} \tag{2.15b}$$

where g_m is the transconductance of the PA, W is the width of the PA transistor, L is the channel length, k_n is a process dependent parameter, I is the bias current and R is the output load impedance.

From equation (2.15b), we observe that as the bias current is reduced, the transconductance and gain of the PA also reduces as a square root of the bias current. As a result, the power gain is non-linear and exhibits some dependence on the bias current (voltage). Thus this method degrades the linearity of the class A PA. However its linearity performance is better than that of a class B PA since the bias point of the PA is varied such that a sinusoidal signal is always produced at the output of the PA. Figure 2.11 shows a simplified schematic illustrating dynamic gate biasing. A fixed bias voltage (V_{GG}) is used to bias the PA above the threshold voltage and the input envelope signal added for varying the gate bias voltage. Figure 2.12 shows a plot of bias current against

gate bias voltage for a PA with dynamic gate biasing. It shows the direction of movement of the operating point of the PA, Q, as the envelope signal changes from maximum to minimum. The maximum envelope swing ($V_{env,i\text{-}max}$) corresponds to the maximum operating point ,Q_{max} ,when transmitting at peak power and the minimum envelope swing corresponds to the lowest operating point, Q_{min} when transmitting at low power.

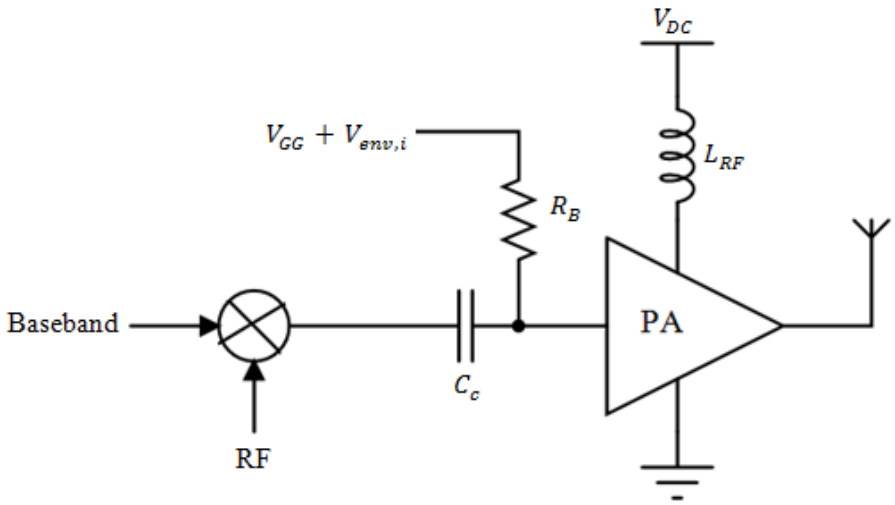


Figure 2.11 Simplified Schematic Illustrating Dynamic Gate Biasing

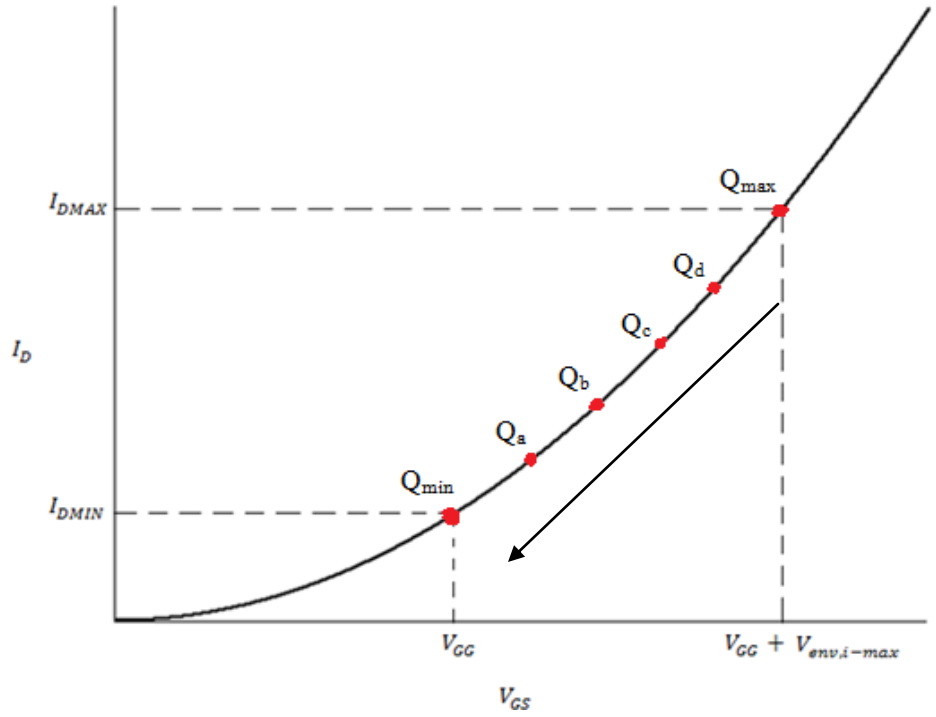


Figure 2.12 Plot of Bias Current vs. Gate Bias Voltage

2.3.4 Combination of Dynamic Gate and Drain Biasing

The efficiency enhancement techniques discussed either improve the voltage efficiency or the current efficiency of the PA. To improve both the current efficiency and voltage efficiency of the PA simultaneously, we can combine dynamic gate biasing and dynamic drain biasing to control the bias current and drain bias voltage of the PA[10]. Theoretically, a power efficiency of 50% can be maintained for all power levels if the dc supply voltage, $V_{DC}(V_{out})$, and dc current, I_{DC}, are varied such that they ideally follow V_{pk} and I_{pk} respectively. Figure 2.13 shows a simplified schematic illustrating a combination of dynamic drain and gate biasing.

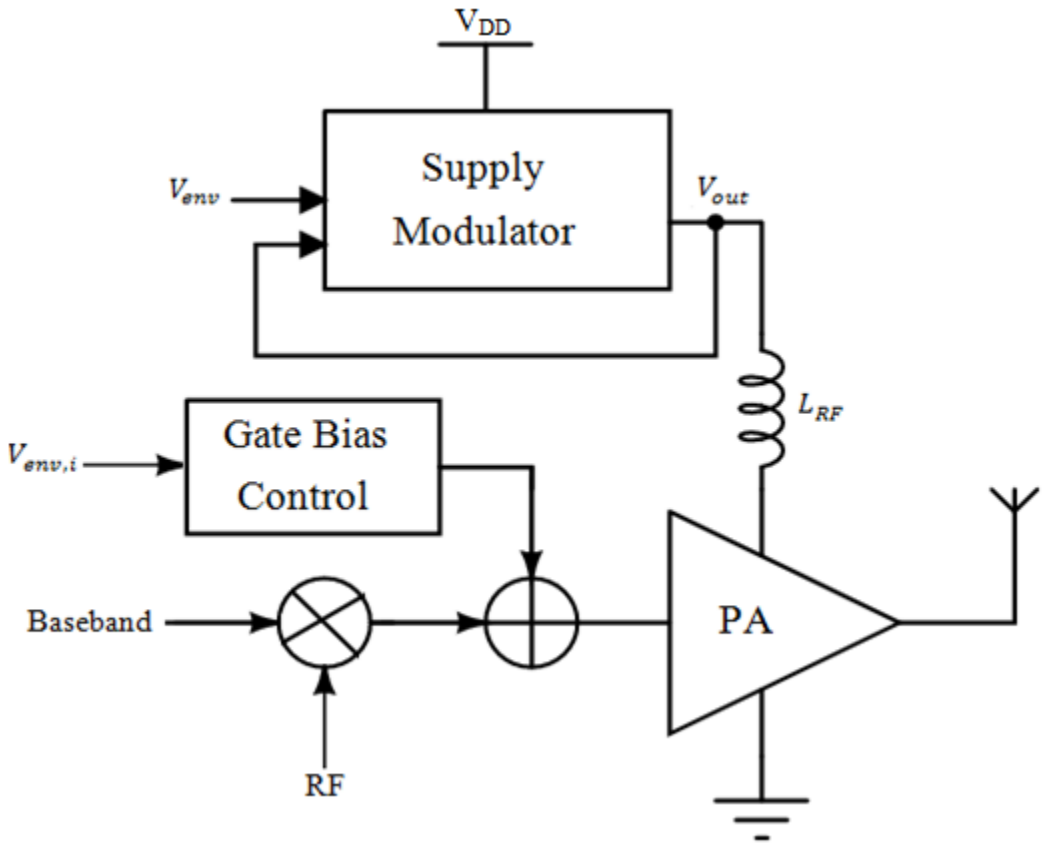


Figure 2.13 Simplified Schematic Illustrating Dynamic Gate and Drain Biasing

The output envelope signal is applied to the input of the supply modulator and the input baseband envelope signal to the gate bias control block. The supply modulator replicates the envelope of the output signal at the drain of the PA. Meanwhile the gate bias control block varies the bias current of the PA by adjusting the gate bias voltage according to the level of the input envelope signal. Figure 2.14 shows how the efficiency of a class A PA varies with output power for fixed bias, class G, dynamic gate bias, dynamic drain bias and a combination of both dynamic gate and dynamic drain bias.

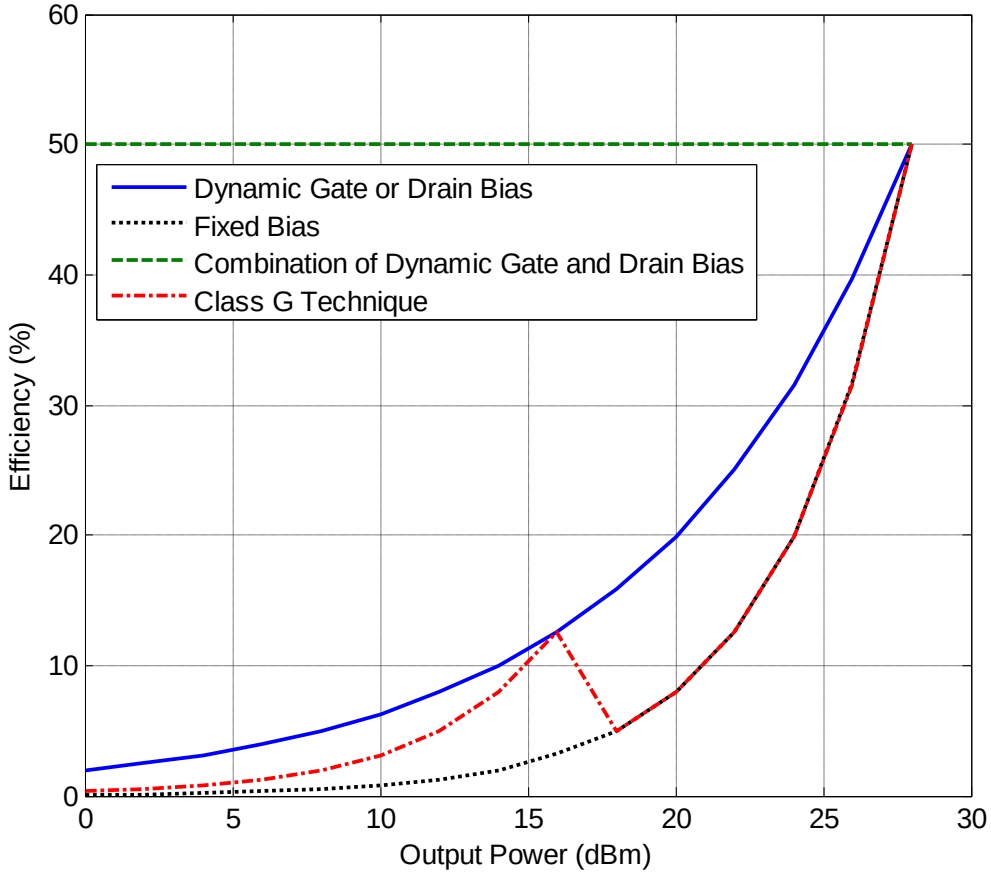


Figure 2.14 Theoretical Efficiency of a Class A PA with Various Efficiency Enhancement Techniques

It should be noted that these plots are idealized values and that in a real PA implementation, the efficiencies will be limited. For instance, the peak efficiency of the class-A PA will be less than 50% because the PA needs some headroom equal or greater than the saturation voltage, V_{DSAT}, of the transistor to maintain linearity. Also the techniques for improving the power efficiency consume power and as a result are not 100% efficient. Thus, the peak efficiency and the efficiency at each operating power will be less than the values shown in Figure 2.14.

Since the combination of the dynamic gate and dynamic drain bias architecture promises the best efficiency results, it is used in this thesis to improve the power

efficiency of the linear PA. The challenge however is to design an efficient supply modulator to control the supply voltage of the PA for wideband applications and is discussed in the next section.

3. SUPPLY MODULATORS

In this section, the operation of supply modulators is described. The existing supply modulation techniques are discussed and switching regulators identified as the most suitable for supply modulation because of their high efficiency. The challenges in designing high efficiency switching regulators for wideband applications are identified as a trade-off between ripple voltage, slew rate, bandwidth and efficiency and an architecture which alleviates these issues is described.

3.1 Definition

A supply modulator is a circuit in which the output node follows a signal applied to its input. Voltage regulators use feedback to force their output node to follow a reference voltage which is usually fixed. In this way, if the envelope of the baseband signal is used as the reference voltage then the output node of a voltage regulator will follow the signal power. Thus voltage regulators are usually used as supply modulators in the transmitter front end of RF PAs. The existing supply modulator architectures can be classified as:

a) Linear Regulators
b) Switching Regulators
c) Hybrid Regulators

The next section discusses these existing supply modulator architectures.

3.1.1 Linear Regulators

Linear Regulators are capable of achieving high bandwidths and as such can be used as supply modulators of wideband power amplifiers. Figure 3.1 shows a simplified diagram of a linear regulator used as a supply modulator.

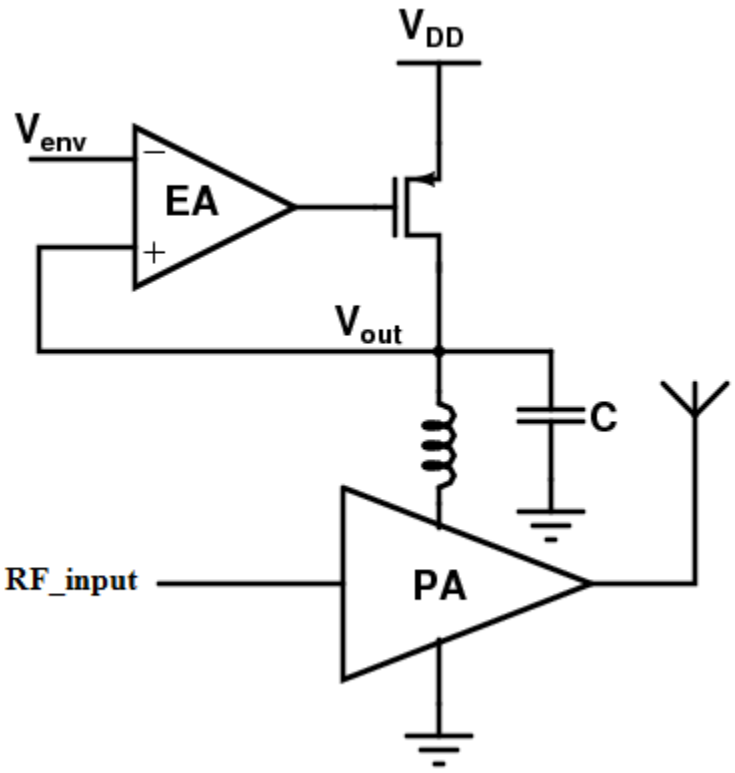


Figure 3.1 Simplified Diagram of a Linear Regulator Used as a Supply Modulator

The relationship between the envelope signal and the output voltage is given by

$$V_{out} = \frac{A(s).g_m.r_o}{1 + A(s).g_m.r_o} V_{env} \tag{3.1}$$

where A(s) is the gain of the error amplifier (EA), g_m is the transconductance of the PMOS pass transistor and r_o is the output impedance of the pass transistor. Therefore if $A(s).g_m.r_o \gg 1$, then $V_{out} \cong V_{env}$. However the efficiency of a linear regulator is in the best case given by [11]

$$\eta_{LR} = \frac{V_{out}}{V_{DD}} \tag{3.2}$$

Linear regulators can be classified within the class-A type regulators. They have a poor efficiency when the output voltage is significantly less than the supply voltage. Unfortunately, this is the scenario in modern wireless communication systems where the envelope signal is much less than the supply voltage during most of its operation. As a

result linear regulators are not suitable applications in which efficiency is a mjor concern. They are only used as supply modulators for highly efficient nonlinear PAs like class E PAs [12].

3.1.2 Switching Regulators

Switching regulators can produce an output voltage lower or higher than the battery supply voltage. When the output voltage produced is lower than the supply they are referred to as buck switching regulators and when the output voltage is higher than the supply they are referred to as boost switching regulators. In this application, the output voltage is required to be less than the battery supply so our discussion will be limited to the buck switching regulator. The buck switching regulator is the most efficient way of modulating a supply voltage. It achieves a maximum theoretical power efficiency of 100% but non-idealities such as losses due to the non-zero "on" switch resistance and dynamic power dissipation due to the turning on and off of the switches limits the efficiency usually to the range of 80-95%. Figure 3.2 shows a simple block diagram of a buck switching regulator used as a supply modulator.

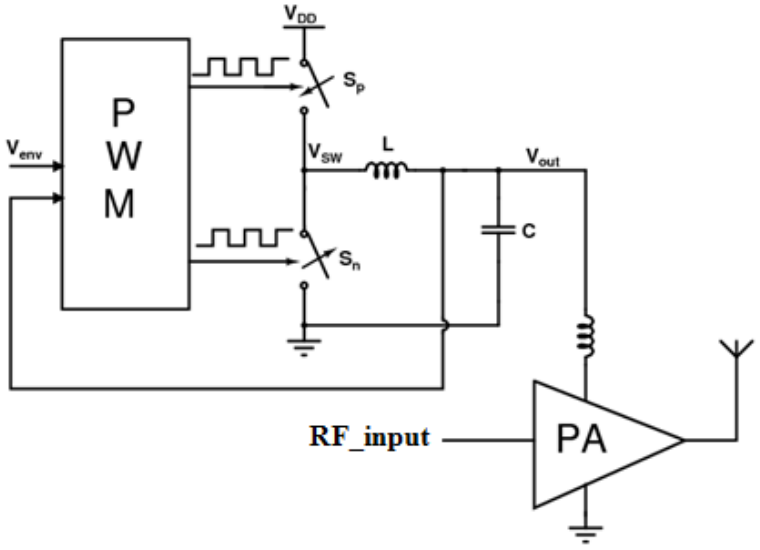


Figure 3.2 Block Diagram of a Buck Switching Regulator Used as a Supply Modulator

References [4],[13],[14] show a practical implementation of a switching regulator as a supply modulator. The envelope signal, V_{env}, is applied to the input of the Pulse Width Modulator (PWM) for it to generate pulse width modulated signals for controlling the power switches for the output voltage follow the envelope signal. However, for wideband applications the typical switching regulator is not fast enough to respond to envelope signals with high bandwidths because it is slew-limited by the bulky inductor and capacitor used to regulate the output voltage. Therefore switching regulators are usually limited to low speed applications. These limitations are discussed in more detail in Section 3.2 along with a more detailed description of the buck switching regulator.

3.1.3 Hybrid Regulators

This technique combines the high efficiency advantage of a switching regulator with the high speed advantage of linear regulators. Figure 3.3 shows a simplified schematic of a hybrid regulator.

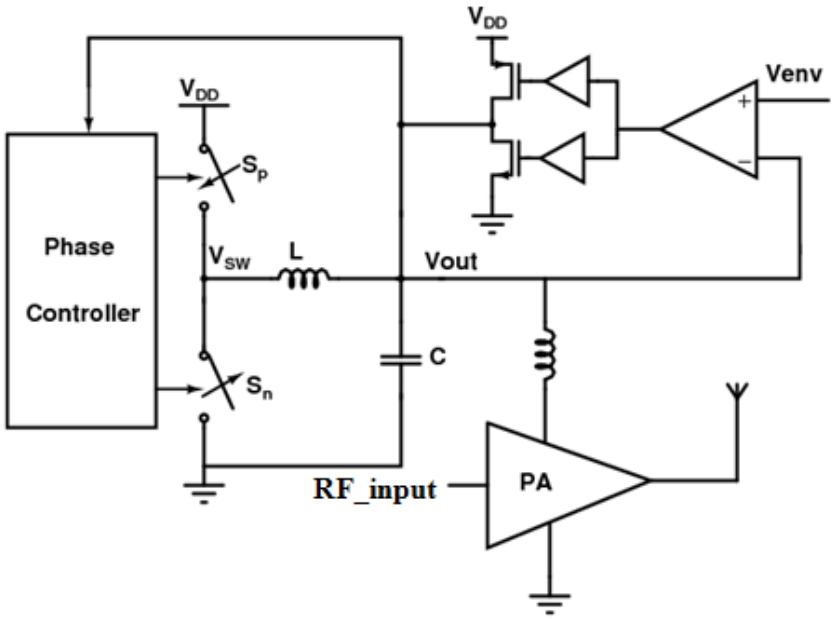


Figure 3.3 Simplified Schematic of a Hybrid Regulator Used as a Supply Modulator

The switching regulator is usually designed to handle the low frequency envelope signals and the linear regulator handles the fast envelope variations. This architecture seems to be the way forward with many research groups using this approach [15-22]. However this architecture usually has the following issues:

a) High Quiescent current consumption

The role of the class AB amplifier is to use feedback to reproduce the envelope signal with minimum distortion and also to attenuate the ripple voltage of the switching stage thus eliminating the need for an external capacitor[18]. As a result it is required to provide a path of very low impedance over a wide range of frequencies in order to absorb the ripple current in the inductor of the switching regulator which requires the class AB amplifier to have a very high bandwidth. Additionally, the class AB output stage has large transistors in order to supply current to the load when the switching stage is not able to do so [16]. As a result the current supplied by the class AB stage varies from zero to the maximum required by the load. This makes stabilizing the class AB amplifier very challenging since it has two low frequency poles which change locations with load current (one at the gates of the current source and sink and another at the output of the amplifier). This problem is similar to that of the external capacitor less LDO regulators[23]. In order to guarantee stable operation while maintaining wide bandwidth, the quiescent current is required to be several tens of milliamps[21]. The quiescent current consumption of the class AB amplifier can be as much as 24mA [20]. This high quiescent current consumption degrades the power efficiency of the supply modulator under low and mid-power regions. For instance reference [18] has a power efficiency of only 30% at 16dBm because of its high quiescent current consumption of 24mA.

b) Increased Power Losses

In the event of transients, the class AB amplifier should be capable of supplying or absorbing all the current demanded by the load since the bulky inductor will not be able to supply or absorb the fast current component. As a result the class AB output stage uses large PMOS and NMOS current sources and sinks respectively for enhancing

the positive and negative slew rates of the switching regulator. The current sink used for improving the negative slew rate increases the power loss in the system by quickly discharging the load capacitor to ground. As a result, power that could have been conserved by allowing the capacitor to discharge through the load is dumped to ground hence increasing the power losses.

Clearly, an efficient way of modulating the supply voltage for wideband standards is needed. To do this we start off by revisiting the most efficient supply modulator; the buck switching regulator. We identify the fundamental problems associated with designing high efficiency switching regulators for wideband applications and propose an efficient solution for solving the problems.

3.2 Buck Switching Regulators

A buck switching regulator consists mainly of two power switches and an LC filter for transferring power from a battery supply voltage to the load. Figure 3.4 shows the schematic of a buck switching regulator.

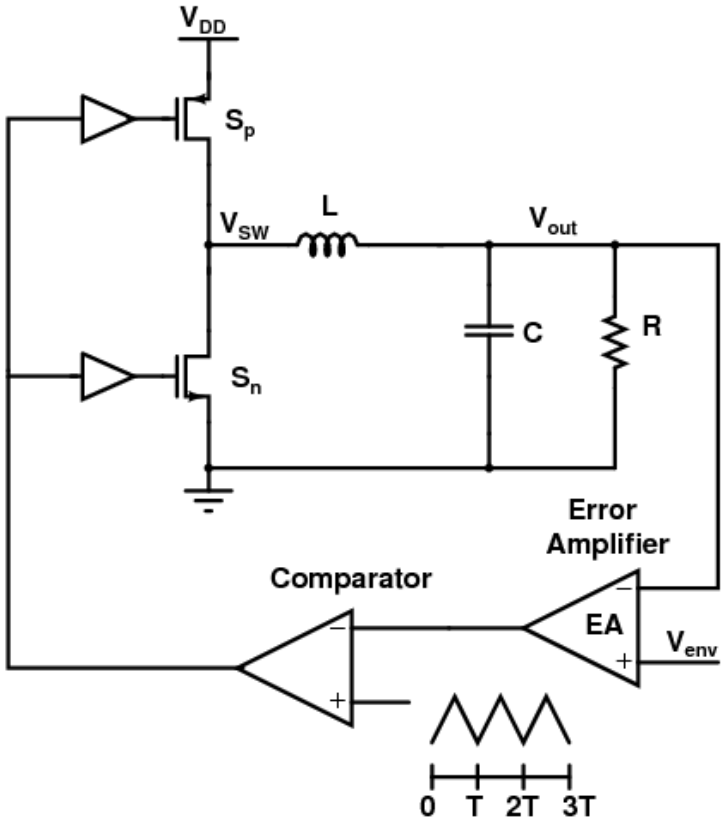


Figure 3.4 Simplified Schematic of a Switching Regulator

The error amplifier (EA) compares the output voltage,V_{out}, with the envelope voltage, V_{env}, and generates an error signal. The comparator compares the error signal with a triangular waveform reference to convert the error signal to a pulse width modulated on-off signal for controlling the power switches S_p and S_n. Since the power switches are large devices, they are buffered to make improve drive strength and minimize propagation delays. The pulse width modulated signal turns the power switches on and off in the right sequence to force the output voltage to follow the envelope signal. Notice that since the power switches are implemented with PMOS and NMOS transistors, they require the same clock phase to control them. That is, whatever clock phase turns on a PMOS device turns off an NMOS device and vice-versa. The LC filter on the output node acts as a low pass filter which minimizes out-of-band noise and

attenuates the high frequency harmonic components due to the switching, to extract the output envelope signal. The LC filter also plays the role of suppressing the ripple voltage on the output voltage. The DC output voltage of the switching regulator, V_{out}, is related to the supply voltage, V_{DD} , by

$$V_{out} = DV_{DD} \tag{3.3}$$

where D is defined as the duty cycle of the PWM waveform and is given by

$$D = \frac{V_{env}}{V_{DD}} \tag{3.4}$$

Even though the switching regulator is non-linear, it can be assumed to be linear for small signals if the bandwidth is significantly less than the switching frequency[24]. As a result, the PWM can be modeled as a simple gain block[24]. Thus the action of the feedback loop is such that the output voltage is forced to follow the envelope signal. To obtain this, let the gain of the error amplifier be given by A(s), the gain of the PWM by k_1 and that of the LC filter by H(s) then

$$\frac{V_{out}(s)}{V_{env}(s)} = \frac{Loop\ Gain}{1 + Loop\ Gain} \tag{3.5a}$$

$$\frac{V_{out}(s)}{V_{env}(s)} = \frac{k_1 A(s) H(s)}{1 + k_1 A(s) H(s)} \tag{3.5b}$$

If $k_1 A(s)H(s) \gg 1$,

$$V_{out}(s) \cong V_{env}(s) \tag{3.6}$$

Switching regulators are noisy and usually expensive because of the high area associated with using the inductor and capacitor which are off chip components. However, they are still preferred because they promise the best efficiency.

Designing power efficient switching regulators for use as supply modulators in modern wideband standards such as WiMax becomes very challenging because of the bandwidth and slew rate required to follow its envelope variations (the bandwidth can be as high as 20MHz). Another related issue is the high peak-to-average power ratio (up to 12 dB) present in typical OFDM schemes which introduce fast envelope variations that demand very high slew-rate figures. These challenges are discussed next.

3.2.1 Power Efficiency

The power efficiency of a switching regulator is given by

$$\eta_{SR} = \frac{P_{o,dc}}{P_{o,dc} + P_L} \tag{3.7}$$

where $P_{o,dc}$ is the power delivered to the load and P_L is the power loss in the switching regulator.

Maintaining a high power efficiency in the switching regulator under all operating conditions in this application is very important since a poor power efficiency degrades the overall system efficiency. To optimize the power efficiency, all the loss mechanisms in the switching regulator need to be analyzed and mechanisms devised to minimize them. The losses in the switching regulator are

a) Switching Losses: This occurs because of dynamic power dissipation in the parasitic capacitance of the power switches as a result of switching. Consider the simplified schematic of the switching regulator in Figure 3.5 with effective switch parasitic capacitance, C_p, given by

$$C_p = C_{x1} + C_{x2} + C_{x3} \tag{3.8}$$

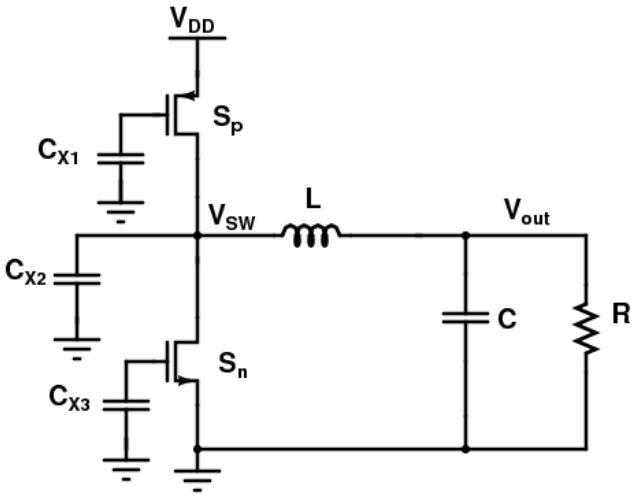


Figure 3.5 Simplified Schematic Showing Switch Parasitic Capacitance

The switching losses in a switching regulator are given by

$$P_{sw} = f_{sw} C_p V_{DD}^2 \quad (3.9)$$

where f_{sw} is the switching frequency and V_{DD} is the supply voltage.

It is noticed from equation (3.9) that the switching losses increase linearly with the switching frequency for a fixed switch parasitic capacitance and supply voltage. These losses degrade the efficiency of the switching regulator under light loads (i.e. when the power delivered to the load is typically less than 50mW) which is the region under which the switching regulator will be mostly operated for this application. The most critical thing here is to limit the switching losses when delivering average power to the load since in average the switching regulator will operate at average power. Considering a typical average power consumption of 70mW, it is important to limit the switching losses to a maximum of 5mW in order to guarantee good average power efficiency. In order to optimize the switching losses, we consider Figure 3.6 which shows a graph of the variation of the switching frequency with the switching losses for different values of C_p(C_{p1}<C_{p2}<C_{p3}). These different values of C_p were obtained from different transistor switch sizes with dimensions shown in Table 3.1 using the TSMC 0.18um technology with V_{DD}=2V.

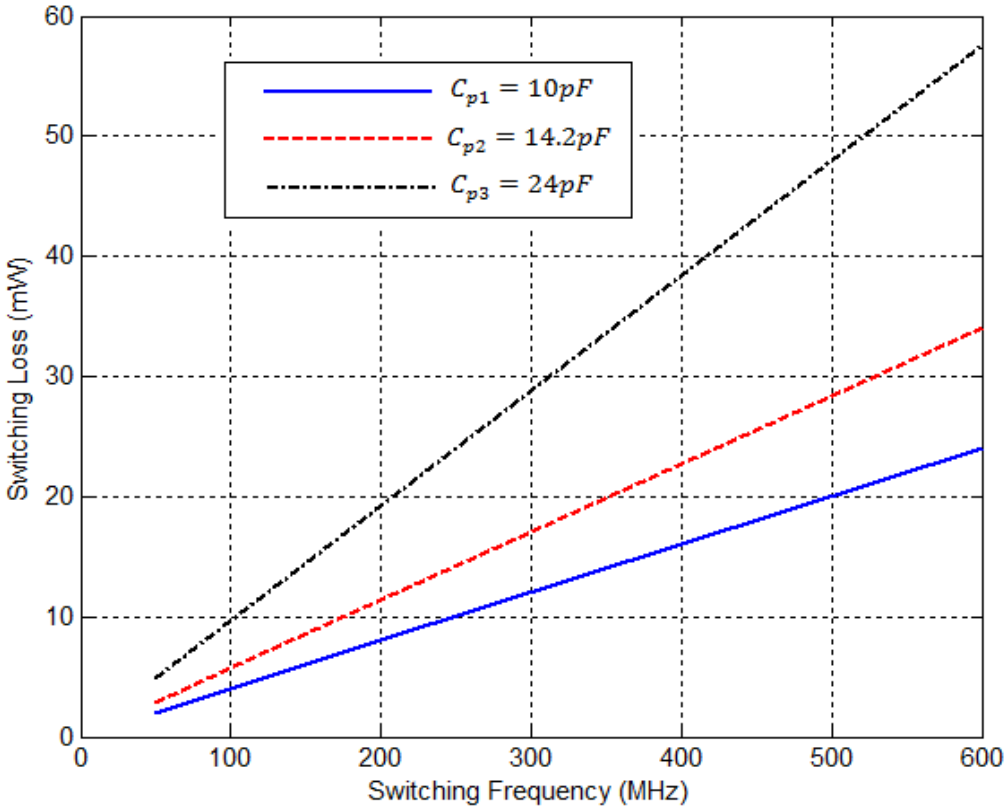


Figure 3.6 Plot of Switching Loss vs. Switching Frequency

Table 3.1 Power Switches and their Dimensions

Switch	Width(µm)	Length(µm)
S_{p1}	3072	0.18
S_{p2}	4096	0.18
S_{p3}	7168	0.18
S_{n1}	768	0.18
S_{n2}	1024	0.18
S_{n3}	1792	0.18

From Figure 3.6, it is noticed that the switching frequency must be less than 100MHz in order to guarantee that the switching losses are limited to a maximum of 5mW. Thus, the

switching frequency for this application must be less than 100MHz in order to obtain good average power efficiency.

b) Conduction Loss: This is due to the non-zero on resistance of the PMOS, R_{ON-P}, and NMOS, R_{ON-N}, power switches. It is given by

$$P_C = P_{C-P} + P_{C-N} \tag{3.10a}$$

$$P_C = D.I^2.R_{ON-P} + (1-D).I^2.R_{ON-N} \tag{3.10b}$$

If R_{ON-P}=R_{ON-N}=R_{ON}, then

$$P_C = I^2.R_{ON} \tag{3.10c}$$

where I is the load current.

The simplified assumption of equation (3.10c) is used in this work to evaluate the conduction loss. Figure 3.7 shows the variation of conduction loss with load current for different values of switch on resistance, R_{ON}, obtained from the different switch sizes in Table 3.1 using equation (3.10c).

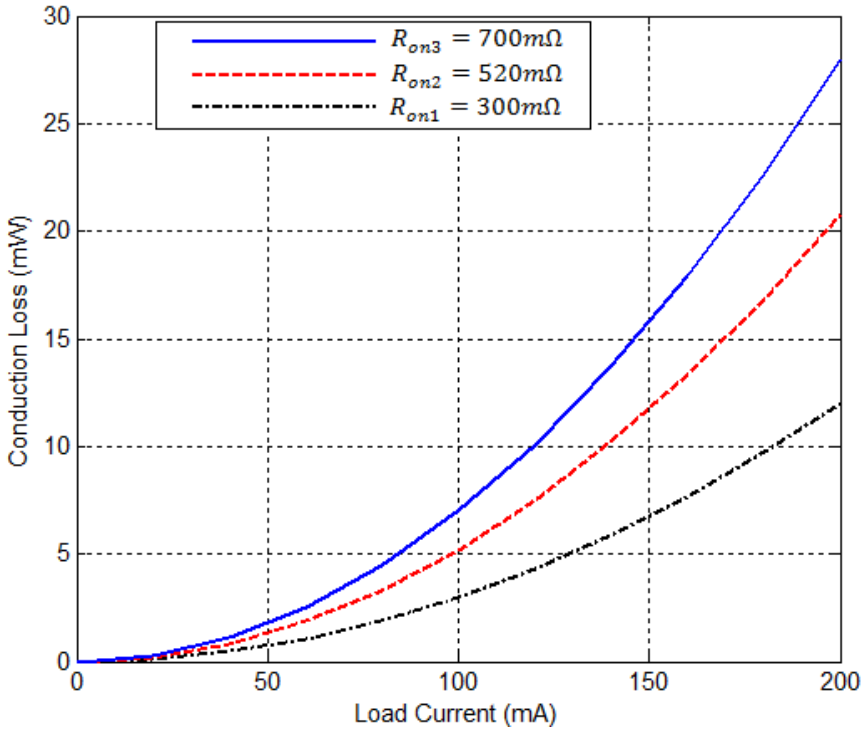


Figure 3.7 Conduction Loss vs. Load Current for Different Switch On-resistances

The conduction losses increase with load current making these losses significant at medium and heavy loads. It is noticed that while switching losses are independent of loading, the conduction losses increase with load current. There is also a tradeoff between the conduction losses and switching losses. The equations for the switch on resistance and the switch parasitic capacitance are given by

$$R_{ON} \cong \frac{L}{\mu C_{ox} W (V_{DD} - V_T)} \tag{3.11}$$

$$C_p \cong WLC_{ox} \tag{3.12}$$

where W is the width of the transistor switch, L is the channel length, V_T is the threshold voltage of the transistor, μ is the mobility of the carriers and C_{ox} is the oxide capacitance per unit area.

From these equations, it can be shown that,

$$R_{ON} = \frac{L^2}{\mu (V_{DD} - V_T) C_p} \tag{3.13}$$

It is observed that R_{ON} is inversely proportional to C_p. Thus, increasing the width of the switch reduces R_{ON} which consequently causes the conduction loss to reduce and increases C_p which causes the switching losses to increase. As a result of this, the power switches should be sized to get the best performance by equalizing the conduction loss and switching loss for average power transmission. Thus,

$$f_{sw} . C_p . {V_{DD}}^2 = I^2 . R_{ON} \tag{3.14a}$$

$$\frac{C_p}{R_{ON}} = \frac{I^2}{f_{sw} . {V_{DD}}^2} \tag{3.14b}$$

Figure 3.8 shows a plot of the optimum values of the ratio of C_p/R_{ON} for a fixed supply voltage, V_{DD}=2V, and different average load currents for three switching frequencies of f_{sw1}=40MHz, f_{sw2}=80MHz and f_{sw3}=120MHz.

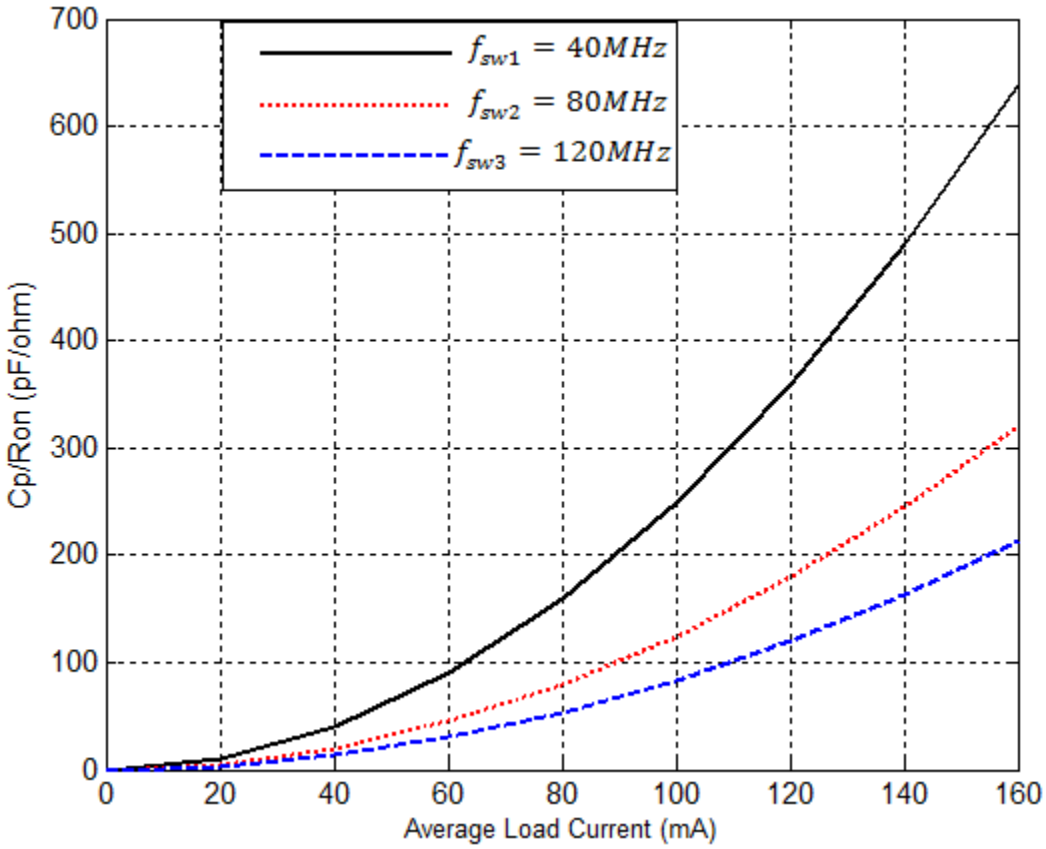


Figure 3.8 Plot of C/Ron vs. Average Load Current for Different Switching Frequencies

The optimum value of switch on resistance and parasitic capacitance can be obtained for a particular switching frequency and average load current from Figure 3.8. For a particular switching frequency after obtaining the average load current, the transistor dimensions should be varied until the desired value of C_p/R_{ON} is obtained.

c) Short Circuit Current Power Loss: This is due to the power switches being on at the same time. Consider the circuit diagram of Figure 3.9 in which logic 0 is required to turn on S_p and logic 1 is required to turn on S_n. The periods of time ΔT_1 and ΔT_2 for which the power switches S_p and S_n are simultaneously on causes a large amount of current I_{sc} to flow from supply to ground. This results in short-circuit power losses which are given by

$$P_{SC} = I_{SC} V_{DD} f_{sw} (\Delta T_1 + \Delta T_2) \tag{3.15}$$

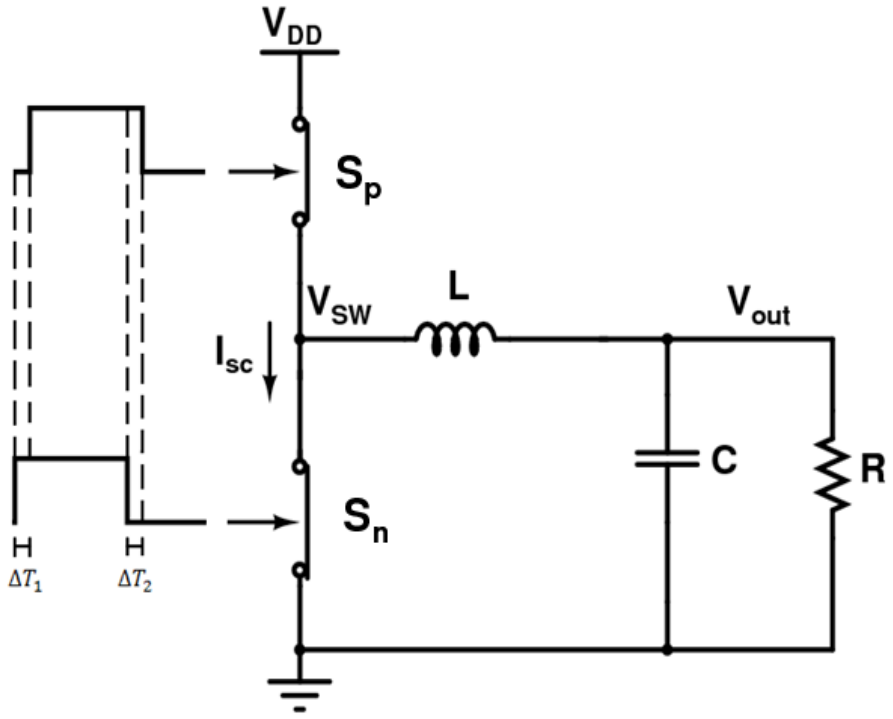


Figure 3.9 Diagram Illustrating Short-circuit Power Loss

However short-circuit currents in the power switches can be eliminated by using non-overlapping clocks for controlling the power switches. Figure 3.10 shows the timing diagram of ideal non-overlapping clocks.

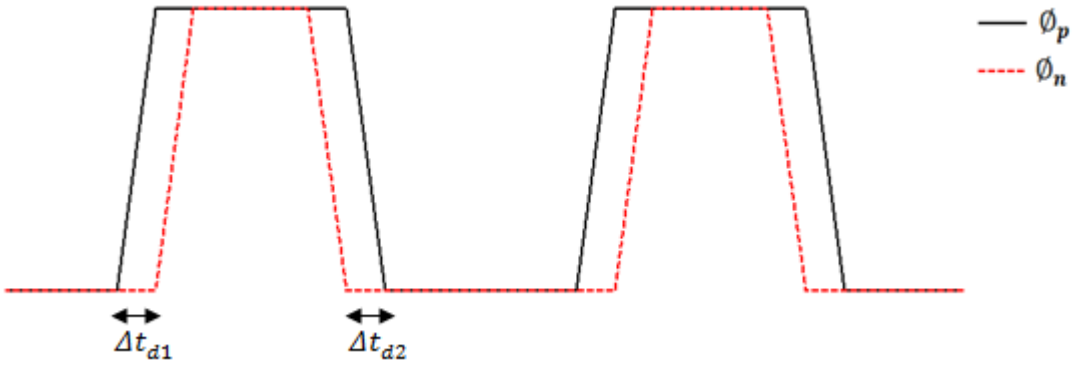


Figure 3.10 Timing Diagram of Non-overlapping Clocks

The non-overlapping clocks introduce dead-times (Δt_{d1} and Δt_{d2}) which prevent the occurrence of short-circuit power loss. The clock phase $\emptyset_p$ controls the high side switch, S_p, which is a PMOS switch and hence requires a logic 0 to turn it on while $\emptyset_n$ controls the low side switch, S_n, which is an NMOS switch and hence requires a logic 1 to turn it on. In order to avoid short-circuit currents, S_p must be turned off before S_n is turned on and S_n must turn off before S_p turns on.

d) Losses due to the power spent in biasing auxiliary building blocks. This is given by

$$P_{bias} = V_{DD}.I_{bias} \tag{3.16}$$

where I_{bias} is the current used to bias the auxiliary building blocks.

The switching regulator requires auxiliary building blocks such as an error amplifier and pulse width modulator (PWM) in a feedback loop as Figure 3.4 showed to enable it to perform its function as a voltage regulator. These auxiliary building blocks also consume power.

After, analyzing the various loss mechanisms in the switching regulator we arrive at the power efficiency which is given by

$$\eta_{SR} = \frac{P_{o,dc}}{P_{o,dc} + P_{SW} + P_C + P_{SC} + P_{bias}} \tag{3.17}$$

Note that for a fixed load resistance of R,

$$P_{o,dc} = I^2R \tag{3.18}$$

Now to illustrate the effect of bias power (quiescent power) on the efficiency of the switching regulator, we consider Figure 3.11 which shows a plot of the variation of power efficiency with output power for different values of P_{bias} with f=80MHz, R_{ON}=700mΩ ,C_p=10pF and R=8Ω.

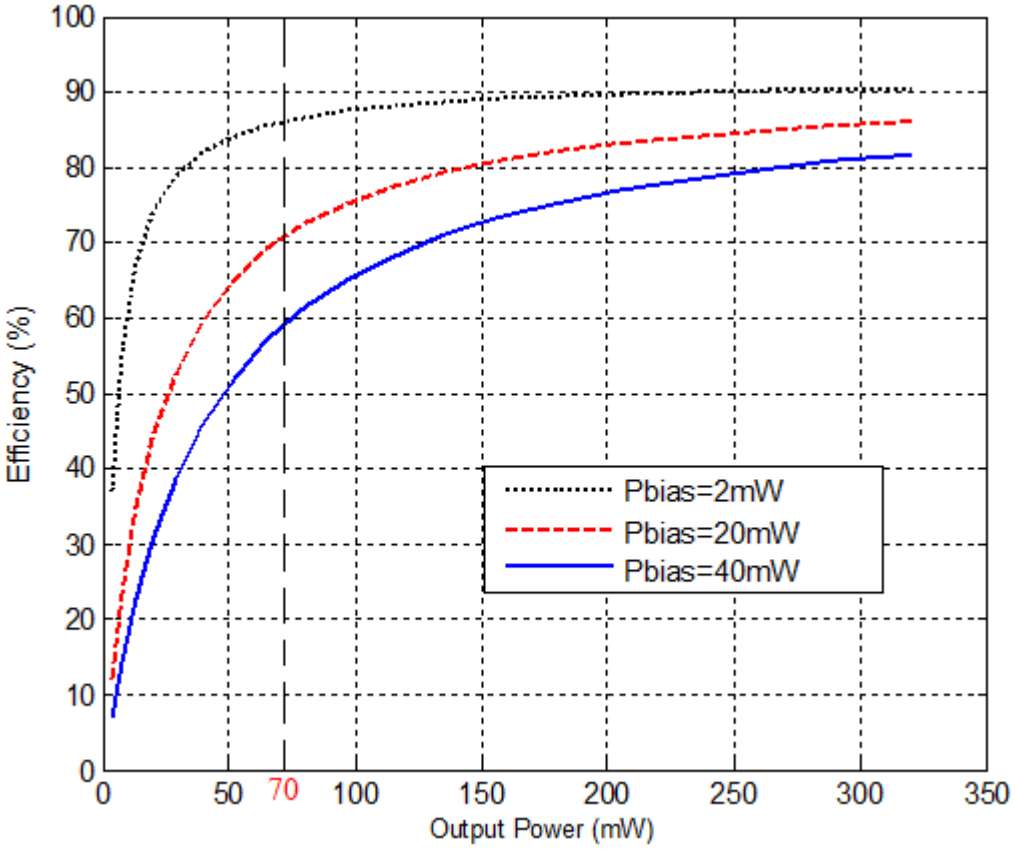


Figure 3.11 Plot of Efficiency against Pout for Different Values of Pbias

This plot shows that the bias power limits the power efficiency mostly when the output power is less than 100mW. Considering a typical average power of 70mW, we notice that the average power efficiency degrades severely as the quiescent power consumption increases. It is therefore important to minimize the quiescent current of the switching regulator in order to guarantee a high efficiency under all operating regions.

In summary, the limitations to the power efficiency of the switching regulator need to be analyzed and understood under different loading conditions in order to optimize efficiency. It has been identified that the switching losses and the quiescent current consumption particularly degrade the average power efficiency of the switching regulator. As a result, these losses need to be minimized in order to guarantee a high average power efficiency in the switching regulator.

3.2.2 Bandwidth

For WiMax applications, the bandwidth of the envelope signal can be as high as 20MHz. The bandwidth of a switching regulator is required to be higher than that of the envelope signal in order for it to track the envelope signal accurately. Referring to equation (3.5a), we noticed that the loop gain must be sufficiently greater than unity for the output voltage to be approximately equal to the envelope signal. Note that the bandwidth of the switching regulator is defined to be the unity gain frequency of the loop gain. For this reason, the modulator bandwidth is usually required to be at least four times the envelope bandwidth to be able to track the envelope signal with minimum distortion [4],[25].As a result, the minimum bandwidth of the switching regulator is required to be 80MHz. However, the PWM is a simple analog to digital converter and as a result it samples the error signal at a rate equal to the switching frequency. From the sampling theorem, the bandwidth of the supply modulator must be sufficiently less than half the switching frequency. The switching frequency is usually made 5-10 times the bandwidth of the switching regulator to prevent switching harmonics present in the output voltage and feedback signals from disrupting the operation of the PWM [4],[24]. So for an envelope bandwidth of 20MHz, a minimum switching frequency of 400MHz will be required. Switching at such high frequencies poses some challenges to the design of the switching regulator; the most critical one being the switching losses. These losses were discussed in Section 3.2.1 and it was realized that in order to optimize the efficiency the switching frequency has to be limited to a maximum of 100MHz.

Another issue related to increasing the switching frequency is the propagation delay of the auxiliary building blocks required for the switching regulator to operate properly. To gain more insight into this, consider the simplified switching regulator shown in Figure 3.4 operating at a switching frequency of 400MHz. This means that only a 2.5ns time window is available for making a switching decision. Any significant delays in the switching regulator loop limits the speed response. Reducing these delays usually require an increase in the power consumption of the auxiliary building blocks. As a result, designing a switching regulator for such high bandwidths is unrealistic

because of the increased switching losses and the increased power consumption required for designing fast auxiliary building blocks. As a result, it is important to limit the bandwidth of the switching regulator to handle envelope variations up to a maximum of 4MHz in order to guarantee a high efficiency.

3.2.3 Stability

The LC filter of the switching regulator in Figure 3.4 is a low pass second order system with transfer function

$$H(s) = \frac{V_o(s)}{V_{sw}(s)} = \frac{1}{s^2LC + s\frac{L}{R} + 1} \tag{3.19}$$

It has a natural frequency,

$$\omega_n = \frac{1}{2\pi\sqrt{LC}} \tag{3.20}$$

and damping factor,

$$\varepsilon = \frac{1}{2R}\sqrt{\frac{L}{C}} \tag{3.21}$$

This is a well known system with the following properties:

1) When $\varepsilon<1$, the system is underdamped and produces oscillations which eventually settle in the presence of transients
2) When $\varepsilon=1$, the system is critically damped and produces the fastest response without any overshoot in the presence of transients
3) When $\varepsilon>1$ the system is overdamped and has no oscillations in the presence of transients

Since oscillations are not desirable, the system is usually desired to be critically damped in order to obtain the best speed response. However, the typical switching regulator will have a filter that is underdamped if the load is a current source. This is because a current source load has a large output resistance (i.e. as $R\rightarrow\infty$, $\varepsilon\rightarrow0$) which makes the system exhibit poor transients whenever there is any disturbance in the load. As a result, a

switching regulator typically has an error amplifier(or more generally a controller) and a PWM in a feedback loop as shown in Figure 3.4 to regulate the output to the desired level and improve the transient response. However, stability becomes a major concern whenever there is a feedback loop. Feedback could potentially make the system unstable. Let us consider the case where the error amplifier in Figure 3.4 has a transfer function given by

$$A(s) = \frac{A}{1 + \frac{s}{\omega_p}} \tag{3.21}$$

Then the loop gain will be given by

$$L(s) = k_1 A(s) H(s) \tag{3.22a}$$

$$L(s) = k_1 \frac{A}{(1 + \frac{s}{\omega_p})} \frac{1}{(s^2 LC + s\frac{L}{R} + 1)} \tag{3.22b}$$

where k_1 is the gain of the PWM.

The stability of the resulting system is analyzed using the root locus(a stability analysis tool which gives a graphical representation of the closed loop poles as the loop gain is varied[26]). The location of the closed loop poles in the s-plane indicates whether the system is stable or not as well as the nature of the transient response. Poles in the left half of the s-plane indicate a stable system while poles in the right half plane indicate an unstable system. The root locus of equation (3.22b) is plotted in Figure 3.12 assuming ω_p=10Mrad/s, L=330nH, C=3.6nF and R=100Ω .

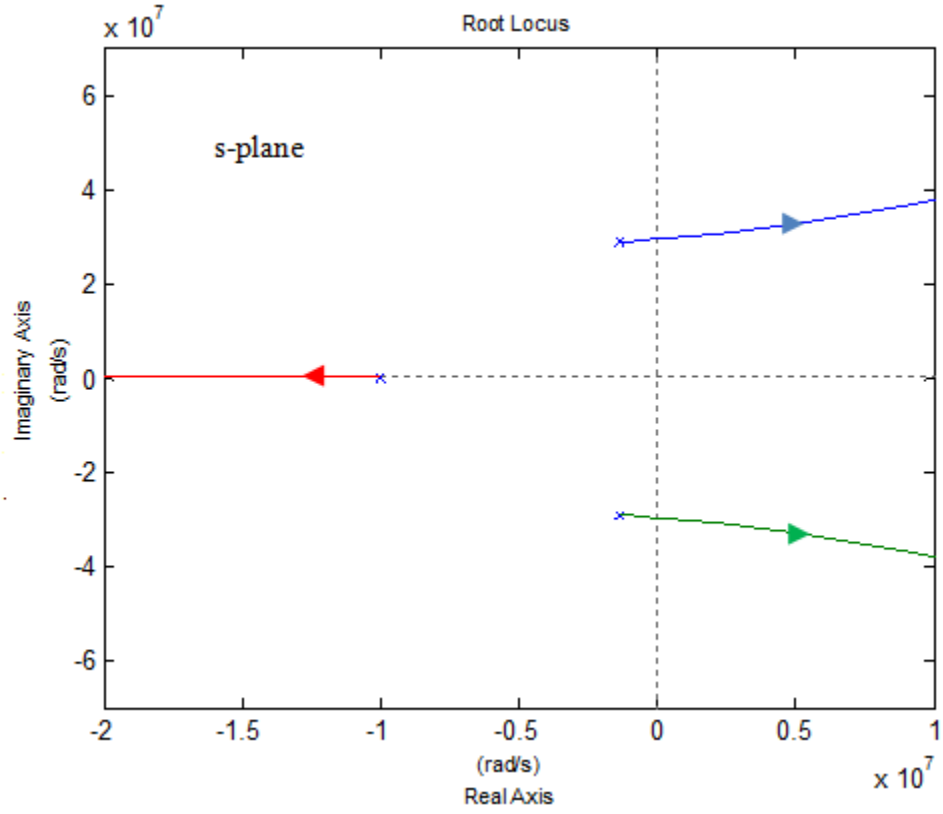


Figure 3.12 Root Locus of Loop Gain without any Zero

The root locus shows that as the loop gain,k_1A, varies the closed loop poles move into the right half plane resulting in an unstable system. As a result, a zero is needed in the feedback loop to guarantee stability. A zero implements a Proportional Derivative (PD) controller with transfer function given by

$$A_z(s) = k_P(1 + \frac{s}{\omega_{z1}}) \tag{3.23}$$

where k_P is the DC gain and ω_{z1} is the frequency at which the zero is located.

Now replacing A(s) with $A_z(s)$ in equation (3.22a), the expression for the loop gain becomes

$$L(s) = k_1 A_z(s) H(s) \tag{3.24a}$$

$$L(s) = k_1.k_P \frac{(1+\frac{s}{\omega_{z1}})}{(s^2LC + s\frac{L}{R} + 1)} \qquad (3.24b)$$

The root locus of the loop gain of equation (3.24b) is shown in Figure 3.13 assuming ω_{z1}=4Mrad/s, L=330nH, C=3.6nF and R=100Ω .

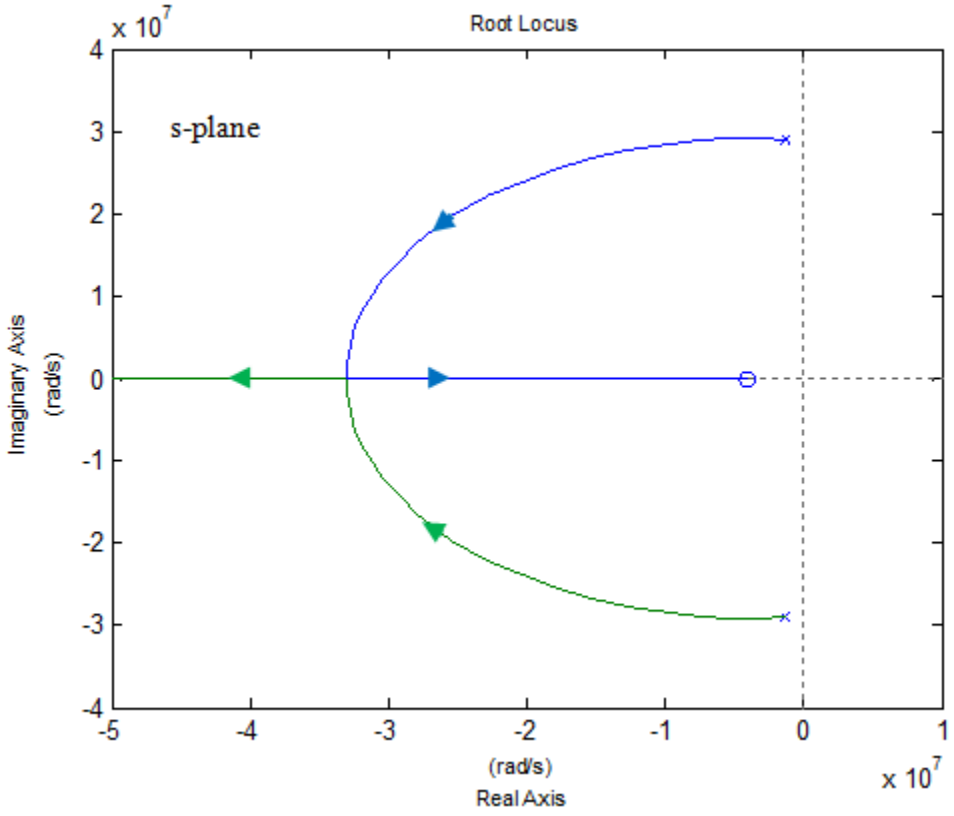


Figure 3.13 Root Locus of System with a Zero

This shows that as the loop gain,$k_1.k_P$, varies, the closed loop poles move away from the imaginary axis towards the left half plane thus guaranteeing stability and improving the transient response. However, the PD controller makes the system susceptible to high frequency noise from the switching harmonics present in the output voltage. A real implementation will require high frequency poles for attenuating this noise. Another disadvantage of using a PD controller is that it has a finite gain at DC which introduces

finite steady state errors in the output voltage. To gain insight into this effect, notice that from equation (3.24b), the loop gain at DC (i.e. when s=0) is given by

$$L(0) = k_1.k_P \tag{3.25}$$

Therefore, the error in the output voltage at DC will be given by

$$\text{DC error} = \frac{1}{1+L(0)} = \frac{1}{1+k_1.k_P} \tag{3.26}$$

Now if we assume that $k_1.k_P=1$, the output voltage will be in error by 50%. To alleviate these effects, a Proportional Integral Derivative (PID) controller can be used. The transfer function of a PID controller is given by

$$A_{Z2}(s) = \frac{K}{s}\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right) \tag{3.27}$$

where K is a finite gain and ω_{z1} and ω_{z2} are the frequencies at which the zeros are located.

Now replacing $A_z(s)$ with $A_{Z2}(s)$ in equation (3.24a), the expression for the loop gain becomes

$$L(s) = k_1 A_{Z2}(s) H(s) \tag{3.28a}$$

$$L(s) = \frac{k_1 K\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{s(s^2LC + s\frac{L}{R} + 1)} \tag{3.28b}$$

The root locus of the loop gain of equation (3.28b) is shown in Figure 3.14 assuming ω_{z1}=4Mrad/s, ω_{z2}=12Mrad/s, L=330nH, C=3.6nF and R=100Ω .

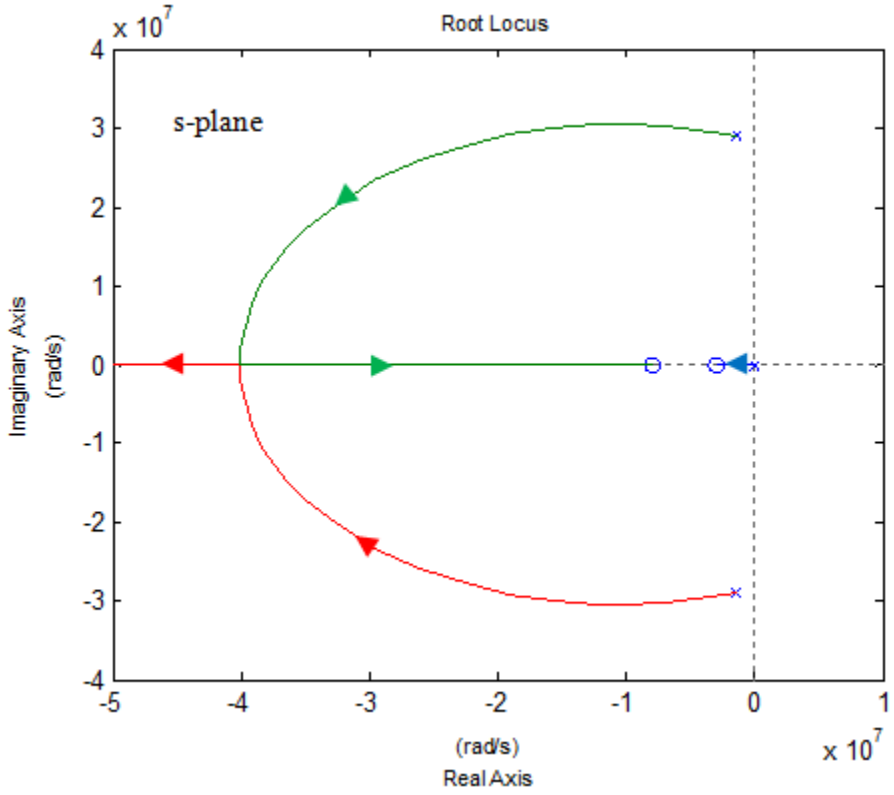


Figure 3.14 Root Locus of System with a PID Controller

The root locus shows that as the loop gain varies, the closed loop poles move away from the imaginary axis towards the zeros in the left half plane thereby guaranteeing stability and improving the transient response. The PID controller has a pole at the origin which has the advantage of eliminating steady state errors. To gain insight into this, notice that at DC, equation (3.28b) reduces to $L(0)=\infty$. Therefore, the error in the output voltage at DC will be given by

$$\text{DC error} = \frac{1}{1+L(0)} = 0$$

The pole at the origin thus increases the low frequency loop gain and ensures that a high loop gain is maintained over a wide frequency range. As a result of this a PID controller is used in this thesis to stabilize the switching regulator. A PID controller can be implemented using the circuit shown in Figure 3.15.

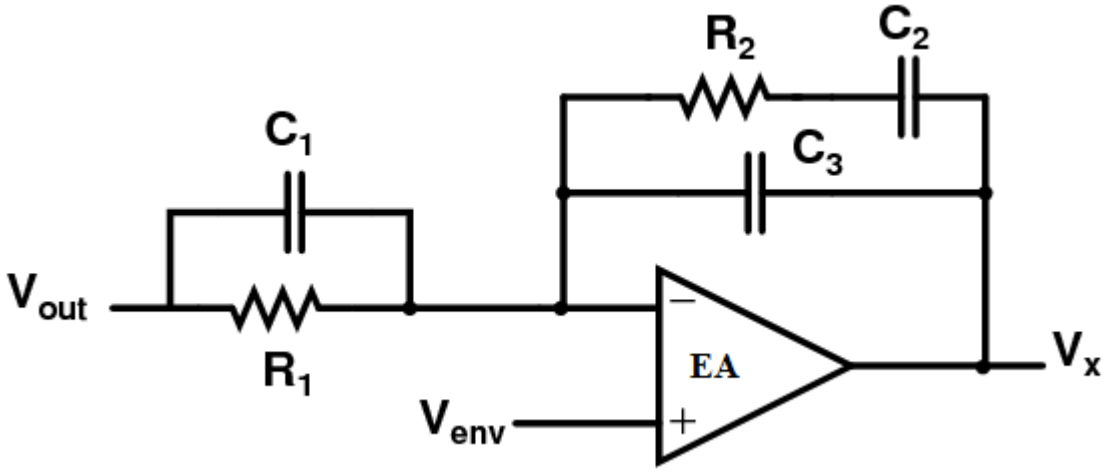


Figure 3.15 Circuit Diagram of a PID Controller

It can be shown that the transfer function of this circuit is given by [27]

$$\frac{V_x(s)}{V_o(s)} = \frac{-1}{sR_1(C_2+C_3)} \frac{(1+sR_1C_1)(1+sR_2C_2)}{(1+sR_2\frac{(C_2C_3)}{(C_2+C_3)})} \tag{3.29}$$

It should be noted that in this schematic implementation, a high frequency pole is added to attenuate high frequency noise from the switching harmonics present in the output voltage.

Even though the root loot locus gives a lot of insight into the transient analysis of the switching regulator, the stability of switching regulators is often analyzed using the magnitude and phase response of the loop gain since this information can be easily obtained in the lab. The stability of the switching regulator can be determined using the phase margin of the loop gain. Phase margin indicates the amount by which the phase of the system has to be reduced at unity gain before it becomes unstable. A positive phase margin usually guarantees stability. However, to guarantee good transient response with little ringing the phase margin should be greater than 45^0. This criterion is used in this thesis to evaluate the stability of the switching regulator. Consider a system with magnitude and phase response of the loop gain shown in Figure 3.16. The phase margin of the system is evaluated as

$$\emptyset_m = 180^0 + (\text{phase at } f_u) \quad (3.30)$$

where f_u is the unity gain frequency of the loop gain.

In this example, $\emptyset_m = 180^0 - 120^0 = 60^0$ thus guaranteeing stable operation.

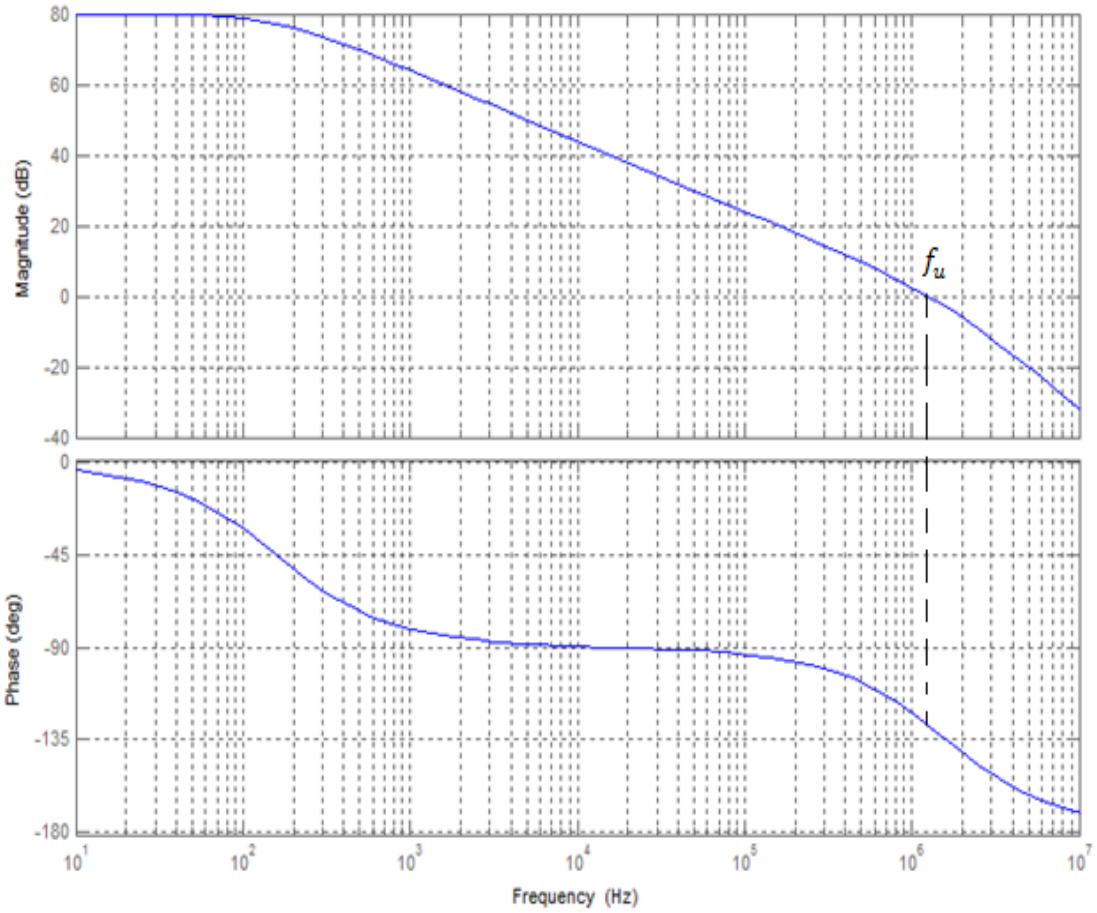


Figure 3.16 Magnitude and Phase Response

3.2.4 Slew Rate

Slew Rate is the maximum rate of change at which the output changes when input signals are large [28]. The maximum rate of change of the input signal is given by

$$SR_{env} = 2.\pi.B.A \quad (3.30)$$

where A is the amplitude of the signal and B is the maximum frequency of the signal. For a signal bandwidth of 20MHz and amplitude of 0.8V, the peak rate of change of the signal is given by SR≅100.5mV/ns.

As a result, the slew rate of the switching regulator is required to be greater than 100.5mV/ns. When large signal variations are applied to the input of a switching regulator, the output is not able to rise quickly to the desired level because it is slew limited by the bulky LC filter on its output node. This slew limitation stems from the fundamental property of the switching regulator; an inductor cannot change its current instantaneously. Consider the circuit diagram of Figure 3.17, the inductor is given by

$$i_L = \int \frac{(V_{sw} - V_o)}{\mathrm{L}} dt \tag{3.31}$$

Now if the voltage across the inductor is small and or the inductor is large, then the amount of current that the inductor can pump into the output node to charge up the load capacitor C is limited.

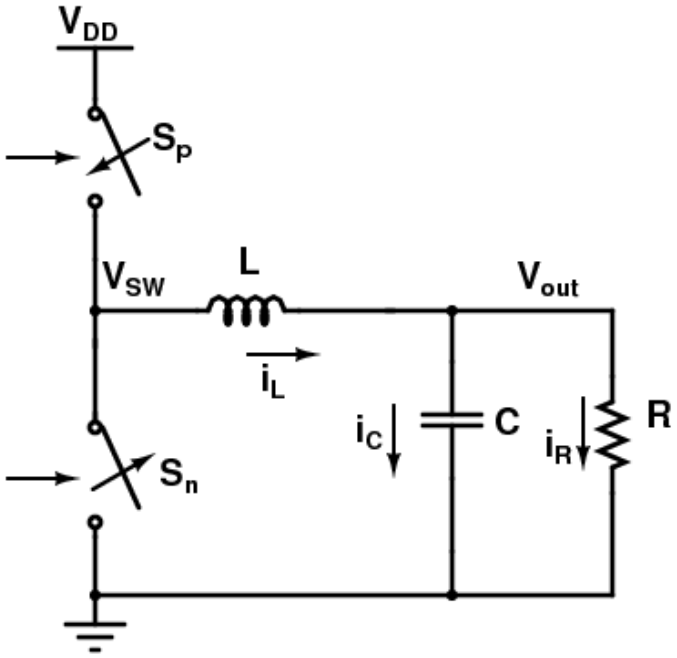


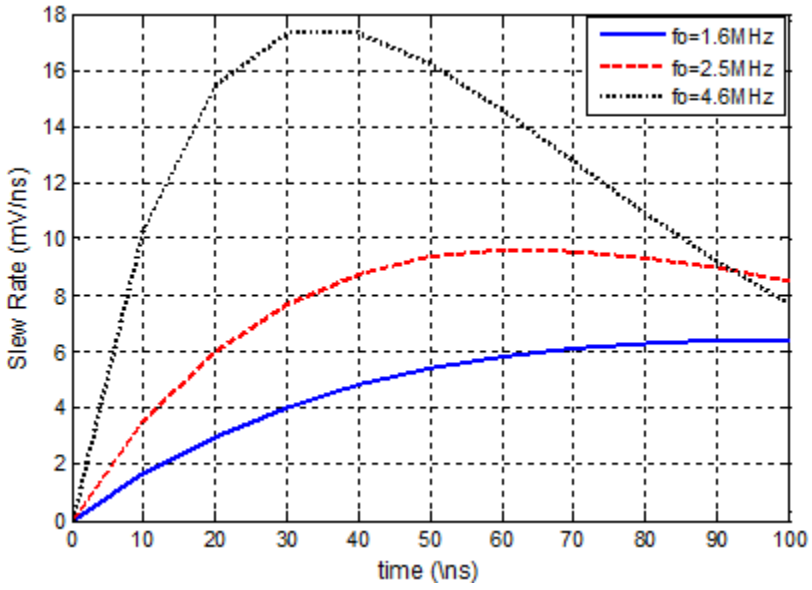
Figure 3.17 Simplified Schematic Illustrating Slew Limitation

The slew rate of a critically damped switching regulator is obtained in the Appendix as

$$\frac{dV_{out}(t)}{dt} = t\omega_o e^{-\omega_o t}\left(V_{sw} - V_o(0)\right) \qquad for\ 0 \le t \le DT \qquad (3.32)$$

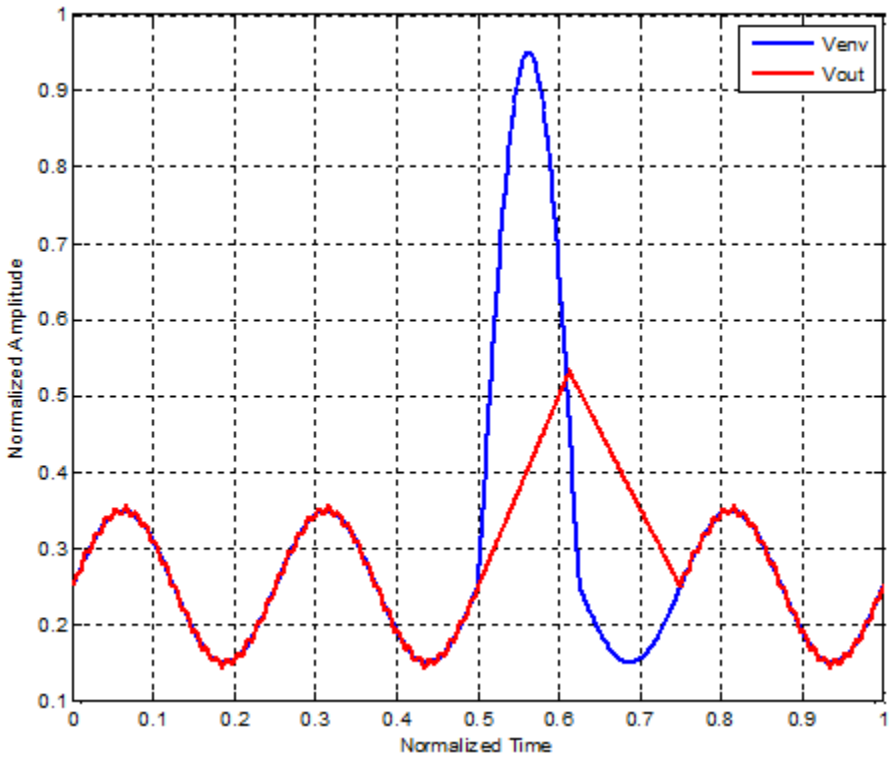
where D is the duty cycle and T is the switching period.

Figure 3.18(a) shows a plot of the slew rate of the switching regulator against time for different values of LC with initial conditions $V_o(0)$=0.35V and Fig 3.18(b) shows the output of the switching regulator slewing in the presence of large and fast envelope signal variations. These plots show that the inherent slew rate of the switching regulator is limited. It should also be noted from equation (3.32) that, the slew rate is dependent on the circuit initial conditions. If the initial conditions are such that $V_o(0)$ is close to the V_{DD} supply rail, then the slew rate figures will be lesser than those in Figure 3.18(a). Therefore, it is difficult to design a switching regulator to achieve the desired slew rate of 100.5mV/ns. As a result some mechanism for enhancing the slew rate of the switching regulator is required.



(a)

Figure 3.18 Plot of the (a) Slew Rate of the Switching Regulator Against Time for Different Values of Natural Frequency, f_o and (b) Output Voltage of Switching Regulator and Envelope Signal



(b)

Figure 3.18 Continued

3.2.5 Ripple Voltage

The output voltage of a switching regulator has a ripple component which results from the incomplete attenuation of the switching harmonics by the LC filter [24].The ripple requirements of a switching regulator are application dependent. Typically, it is required that the ripple voltage is limited to a few tens of millivolts. In this application, a low output ripple is critical for the overall system performance because any noise in the converter output directly couples to the PA output [4]. The expression for the output ripple voltage of the switching regulator can be obtained as follows [24]

The voltage across an inductor is given by

$$V_L = L\frac{di}{dt} \qquad (3.33a)$$

when the switching regulator is in steady state and switch S_p is connected to V_{DD},

$$V_{DD} - V_o = L\frac{\Delta I}{DT} \tag{3.33b}$$

Thus

$$L = DT\frac{(V_{DD} - V_o)}{\Delta I} \tag{3.33c}$$

$$L = \frac{(1-D)V_o}{f_{sw}\Delta I} \tag{3.33d}$$

where ΔI is the peak-peak inductor ripple current, T is the switching period, D is the duty cycle and f_{sw} is the switching frequency

Similarly, it can be shown that

$$C = \frac{\Delta I}{8f_{sw}\Delta V} \tag{3.34}$$

where ΔV is the peak-peak ripple voltage.

These equations are usually used as design equations to select L and C in the design of switching regulators for a given ripple current and ripple voltage specification. They show that a large L or high switching frequency is required to reduce the inductor ripple current and a large LC or high switching frequency is required to reduce the output ripple voltage.

Equations (3.33d) and (3.34) can be combined to obtain,

$$\Delta V = \frac{\left(1 - \frac{V_o}{V_{DD}}\right)V_o}{8f_{sw}LC} \tag{3.35a}$$

$$\Delta V = \frac{\pi^2}{2}\left(1 - \frac{V_o}{V_{DD}}\right)\frac{{f_o}^2}{{f_{sw}}^2} \tag{3.35b}$$

Equation (3.35a) is used in this work to select the switching frequency of the supply modulator after L and C have been selected to meet a specified output voltage ripple. Figure 3.19 shows a graph of the ripple voltage vs. output voltage for $f_{sw}=10f_o$ with $V_{DD}=2V$. It is observed that the maximum ripple occurs when $V_o=\frac{V_{DD}}{2}$. This plot shows that the switching frequency must be equal to ten times the natural frequency in order to guarantee a maximum ripple voltage of 25mV.

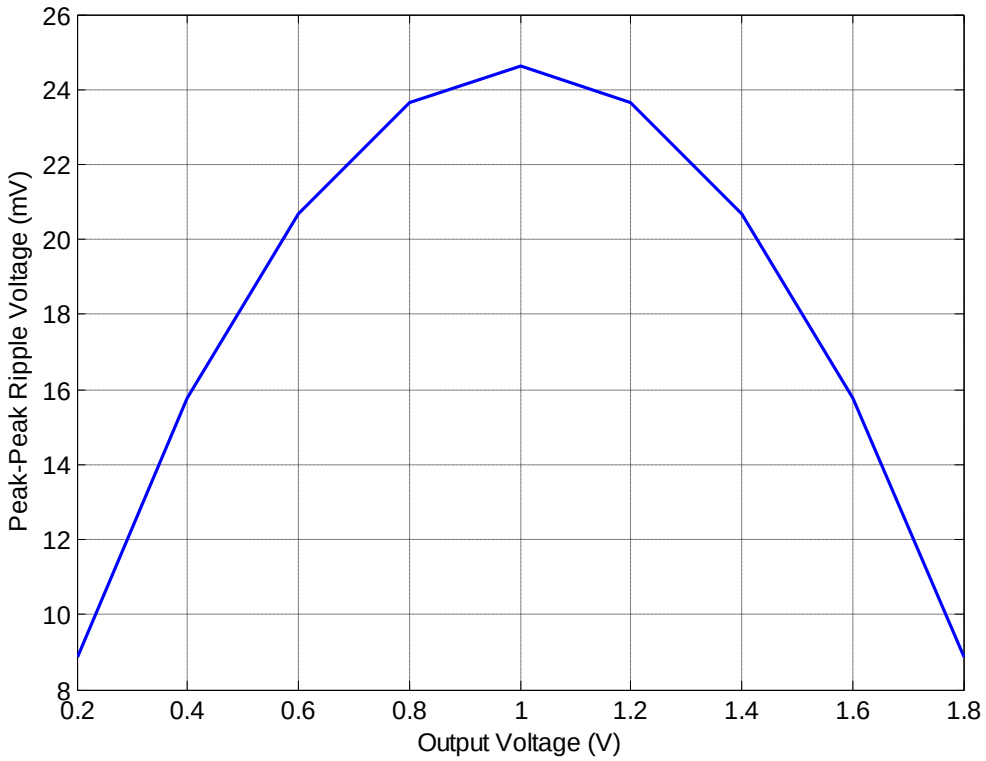


Figure 3.19 Plot of Peak-Peak Ripple against Output Voltage

It has been noticed that designing the switching regulator involves a trade-off between the output ripple voltage, bandwidth, slew rate and power efficiency. This makes the design of efficient high speed regulators particularly challenging. In the next section, a solution is proposed which potentially eliminates these limitations.

3.3 Proposed Solution

It was realized from Section 3.1 that state of the art implementations are mostly focused on using hybrid regulators as supply modulators. Even though these regulators usually eliminate the need for an external capacitor to achieve a low ripple voltage performance they usually have a poor power efficiency at low transmit power, are complex to design and suffer potential stability issues. As a result, an architecture which

alleviates these issues is proposed for use as a supply modulator is proposed in this section.

3.3.1 Conceptual Idea of Proposed Solution

The conventional switching regulator is the most efficient way of modulating a supply voltage so far as the switching losses and quiescent power consumption are minimized. As a result the proposed solution is based on the conventional switching regulator architecture. A dead time control circuit (DTC) implemented with a standard non-overlapping clock generator is added to prevent the occurrence of short-circuit currents due to the power switches being turned on simultaneously. Now if an auxiliary block is added to the switching regulator such that it supplies current to the output node only when the switching regulator is slew limited then the speed can be enhanced. Additionally, this auxiliary block should have negligible quiescent current consumption and should not degrade the stability of the switching regulator. Furthermore, only positive slew rate needs to be enhanced since enhancing negative slew rate increases the power losses in the system by quickly discharging the load capacitor to ground. All these features are desired to make the system more efficient. Note that this auxiliary block also takes advantage of the envelope statistics (i.e. the fast and large envelope variations are infrequent and occur only about 10% of the time) to make the system efficient. Figure 3.20 shows a conceptual diagram of the proposed solution.

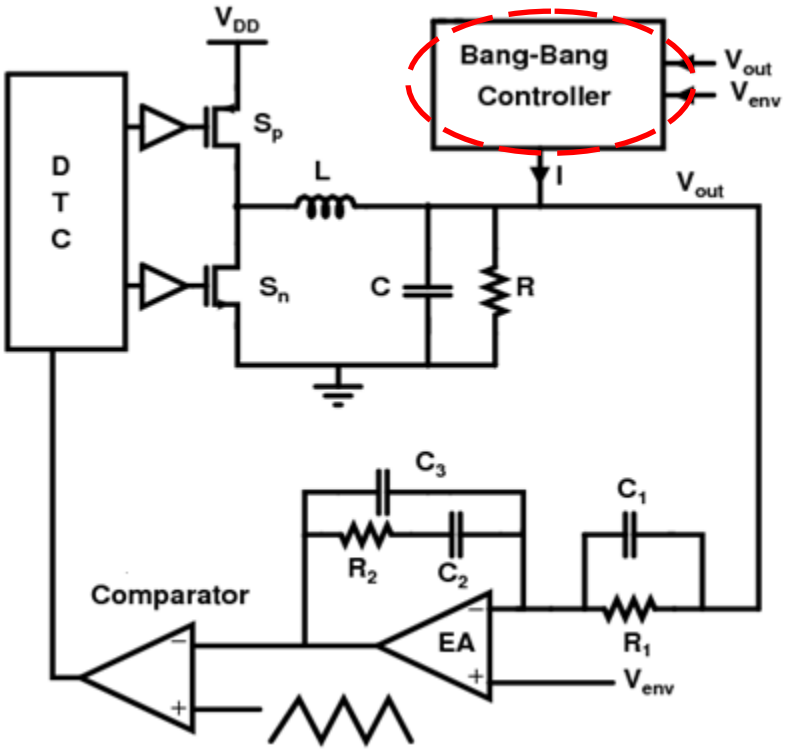


Figure 3.20 Schematic Diagram of Proposed Supply Modulator

The auxiliary building block takes the form of a bang-bang controlled current source. The role of the bang-bang controlled current source is to compare the output voltage of the switching regulator with the envelope signal and inject current into the output node when it is slew-limited. Figure 3.21 shows a simplified schematic of the bang-bang controller circuit.

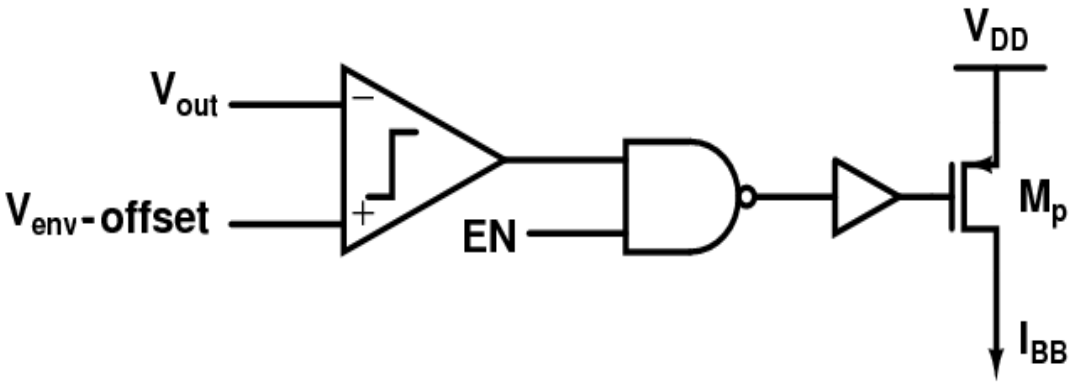


Figure 3.21 Simplified Schematic of Bang-bang Controller

It is made up of a comparator, current source,M_p, and drivers. The bang-bang controller is equipped with an enable (EN) control input which can be used to deactivate the bang-bang control circuitry. When this enable input is a logic zero (ground), the gate of M_p becomes V_{DD} and the current source is deactivated. This functionality is added for practical purposes to allow the user control to wait for the switching regulator to start-up before enabling the bang-bang controller. An offset voltage is subtracted from the envelope signal before comparing it with the output voltage in order to provide some safety margin for control. An offset of 100mV is used in this design. This offset masks the output ripple voltage and makes the bang-bang controller insensitive to the output ripple voltage. When the enable input is a logic one (V_{DD}) and the output voltage of the switching regulator goes below (V_{env} – offset), a logic one is produced at the output of the comparator. This signal is inverted by the NAND gate to produce a logic zero which turns on M_p to inject current into the output node of the switching regulator until output voltage becomes greater than the envelope signal. When the output voltage goes above (V_{env} – offset), M_p is turned off. The amount of current required by the bang-bang controller depends on the maximum slew rate required. Consider the circuit diagram of Figure 3.22.

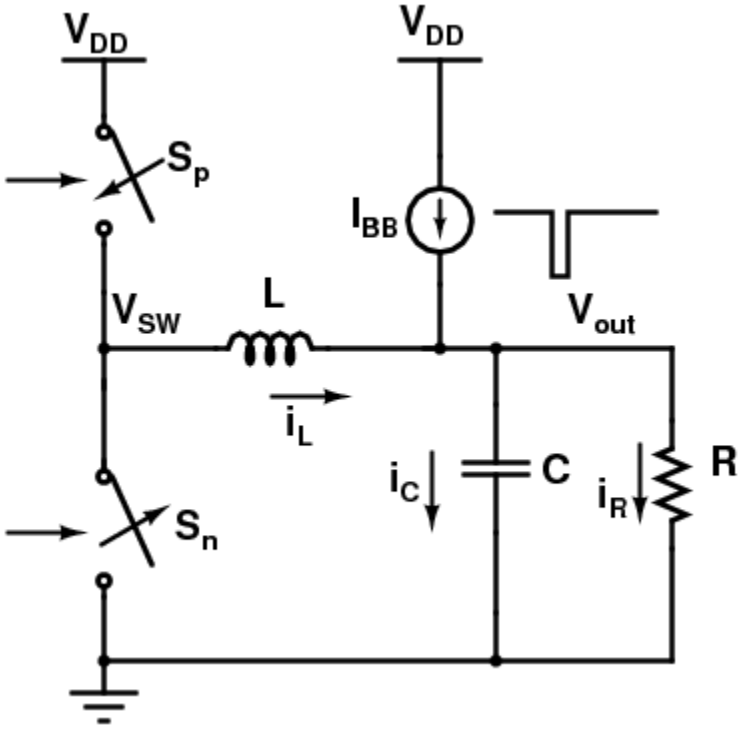


Figure 3.22 Schematic Illustrating Concept of Bang-bang Control

The slew rate required by the switching regulator can be expressed as

$$\frac{dV_{out}}{dt} = \frac{i_C}{C} \tag{3.36}$$

Now in the event that the inductor is not able to provide the fast current needed to charge up the load capacitor when there are fast and large envelope variations, the bang-bang controlled current should be able to provide the current required to meet the slew rate requirements. Thus the maximum slew rate of the bang-bang controller is given by

$$SR_{BB} = \frac{I_{BB}}{C} \tag{3.37a}$$

The current required by the switching regulator to meet the slew rate requirements will be given by

$$I_{BB} = C.SR_{BB} \tag{3.37b}$$

The bang-bang current source is sized to provide this current.

Figure 3.23 shows the ideal behavior of the supply modulator with and without the bang-bang controller. It is noticed that adding the bang-bang controller improves the positive slew rate of the switching regulator. The current used to charge up the capacitor during positive slew rate limitation is discharged from the capacitor through the load.

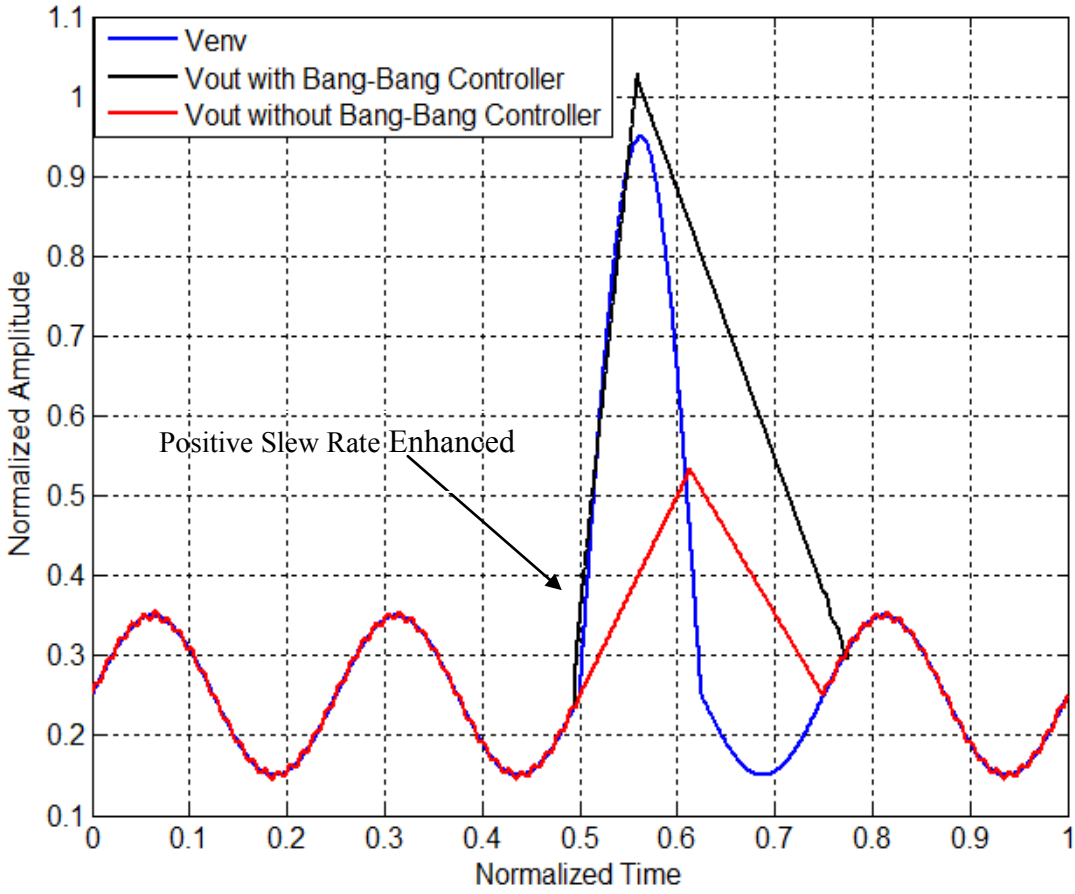


Figure 3.23 Plot of Envelope Signal and Ideal Output Voltage with and without Bang-bang Controller

The main highlights of the proposed solution are:

a) Current efficiency (Negligible quiescent current consumption): The supply modulator has little quiescent current consumption. By employing a bang-bang controller, the extra-circuitry used for slew enhancement is off under normal operating conditions and is activated only during fast or large PA input variations. Since these variations only

occur about 10% of the time, the supply modulator operates just like a switching regulator during normal operation and is assisted by the bang-bang current source only during fast or large PA input variations. Also since the proposed supply modulator has negligible quiescent power consumption, it promises a high power efficiency under all loading conditions.

b) Easy to stabilize: Adding a bang-bang controller to the switching regulator does not degrade stability. This is because the bang-bang controller is an open loop comparator with poles in the left half of the s-plane. As a result stability does not become a problem.

c) Area efficient (only positive slew rate enhancement): Improving both the positive slew rate and negative slew rate of the switching regulator requires a PMOS current source and an NMOS current sink respectively. But by improving only the positive slew rate of the switching regulator, only a PMOS current is used and the area that would have been consumed by the NMOS current sink is conserved. Also, improving the negative slew rate increases the power losses in the system by quickly discharging the charged capacitor to ground. But by just using a PMOS current source, area is conserved and power losses are also reduced.

The main design considerations in the transistor level implementation of the proposed supply modulator are shown in the next section.

4. DESIGN CONSIDERATIONS

In this section, we look at the main considerations in designing the proposed supply modulator. Since the role of the supply modulator is to produce a replica of the voltage applied to its input, it is important to apply the appropriate reference voltage to the input of the supply modulator. Thus we begin this section with the design and characterization of a simple class-A PA. The characterization exercise is needed to obtain the relationship between minimum drain voltage required by the PA to operate properly and the envelope of the signal delivered to the load. The efficiency and linearity performance of the fixed biased PA is extracted and then compared with the dynamic biased PA since the ultimate goal of this work is to improve the efficiency of the class-A PA using dynamic gate and drain biasing. Afterwards, some of the main design considerations in the transistor level implementation of the supply modulator are discussed.

4.1 Design and Characterization of PA

A simple class A PA without an input matching network and output matching network was designed to test the supply modulator and show the efficiency gained by using the proposed approach. Figure 4.1 shows the schematic of the PA used.

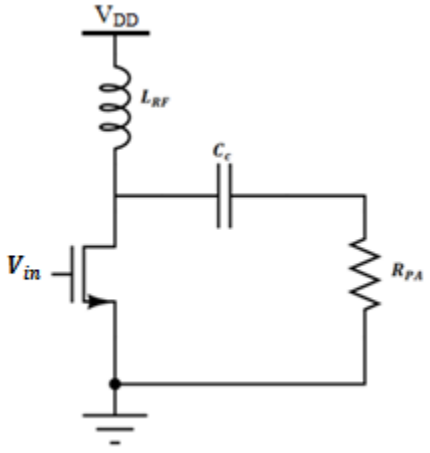


Figure 4.1 Simplified Schematic of PA

The PA is designed for a maximum output power of 19.5dBm using the TSMC 0.18um technology. In this design, the dc voltage supplied to the drain of the PA was limited to a maximum of 1.6V because of technology restrictions. Assuming that the PA is matched to an optimum output impedance of R_{PA}=6Ω, the peak ac voltage delivered to the load will be given by

$$V_{pk} = \sqrt{2.R_{PA}.P_{out}} \tag{4.1}$$

$$V_{pk} = 1.03\text{V}$$

And the peak ac current delivered to the load will be given by

$$I_{pk} = \frac{V_{pk}}{R_{PA}} \tag{4.2}$$

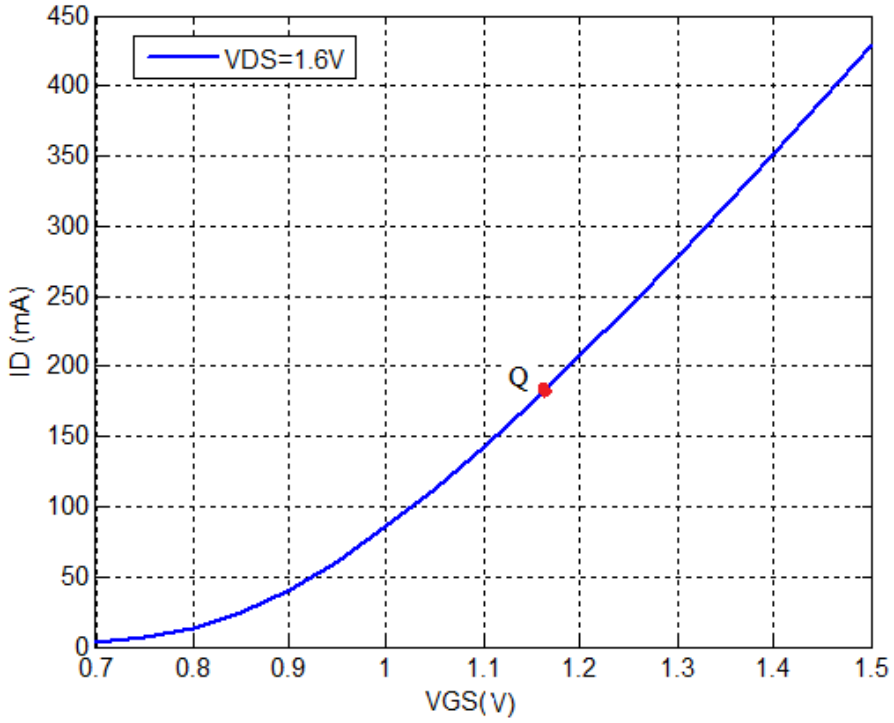
$$I_{pk} = 171.7mA$$

We allow some safety margin and size the transistor to provide a maximum dc current of 192mA in order for the transistor to operate properly. The PA is designed for a peak input signal of 320mV. To ensure that the PA operates in class-A mode, the PA needs to be biased such that for the maximum swing of the input signal, the gate voltage does not swing below the threshold voltage, $V_{T,}$ of the transistor. Thus, with V_T = 0.8V, a gate bias voltage, V_{GS} , of 1.16V is used to ensure that the PA operates in the saturation region with some margin to guarantee class-A operation. The dimensions of the transistor are obtained from

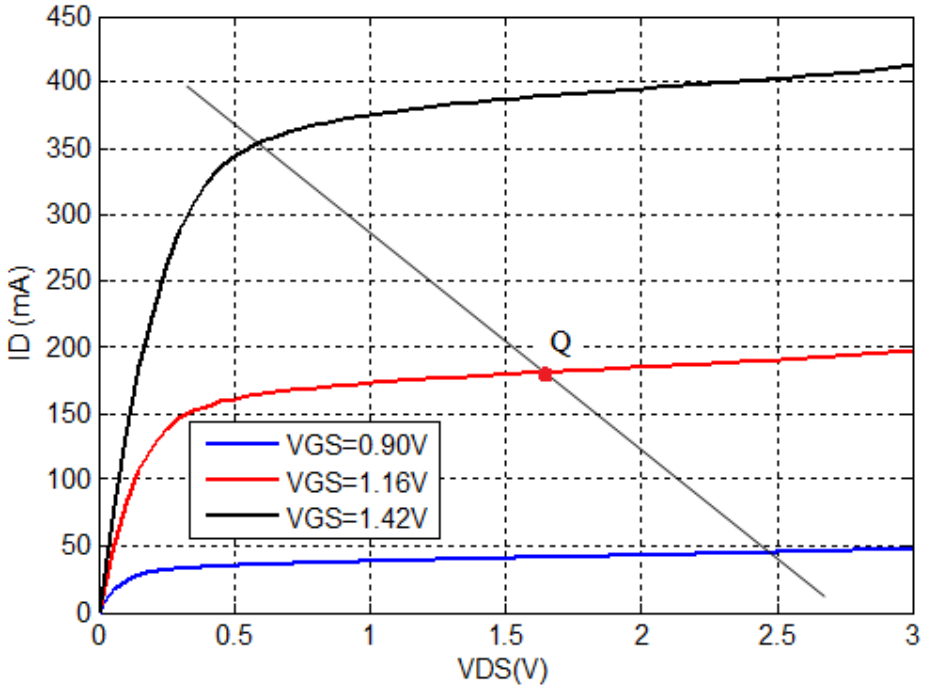
$$\frac{W}{L} = \frac{I_D}{\mu C_{ox}(\text{V}_{\text{GS}} - \text{V}_{\text{T}})^2} \tag{4.3}$$

where W is the width of the transistor, L is the channel length, μ is the mobility of the carriers, C_{ox} is the oxide capacitance per unit area and I_D is the drain current.

An NMOS transistor with W=3600μm and L=0.350um is used in this design. This transistor is characterized to extract its Drain ID, vs. VGS and ID vs. VDS (Drain voltage) curve. These curves shown in Figure 4.2(a) and 4.2(b) respectively show the operating point, Q, of the fixed bias PA.



(a)



(b)

Figure 4.2 Plot of ID vs. (a) VGS for Different Values of VDS and (b) VDS for Different Values of VGS

For a carrier frequency, f, of 1.9GHz, the values of coupling capacitor,C_c, and RF choke, L_{RF}, are selected as

$$C_c = \frac{1}{2.\pi.f.X_c} \tag{4.4}$$

$$L_{RF} = \frac{X_L}{2.\pi.f} \tag{4.5}$$

To reduce the ripple current in L_{RF} and the ripple voltage across C_c [8],

$$X_L \geq 10.R_{PA} \tag{4.6}$$

$$X_c \leq \frac{R_{PA}}{10} \tag{4.7}$$

Thus, this design uses C_c=100pF and L_{RF}=10nH.

In this application, we seek to control the bias current and supply voltage of the PA in order to optimize power efficiency. Controlling the bias current can be achieved by using the envelope of the input baseband signal to control the gate bias voltage using the approach discussed in Section 2.3.3. Figure 4.3 shows a plot of the operating point of the PA as the gate bias voltage varies for different values of V_{DS}. The arrow indicates the direction of the movement of the operating point,Q, as the amplitude of the envelope signal varies from maximum to minimum. The envelope varies the bias current between 192mA for maximum power transmission and 30mA for minimum power transmission.

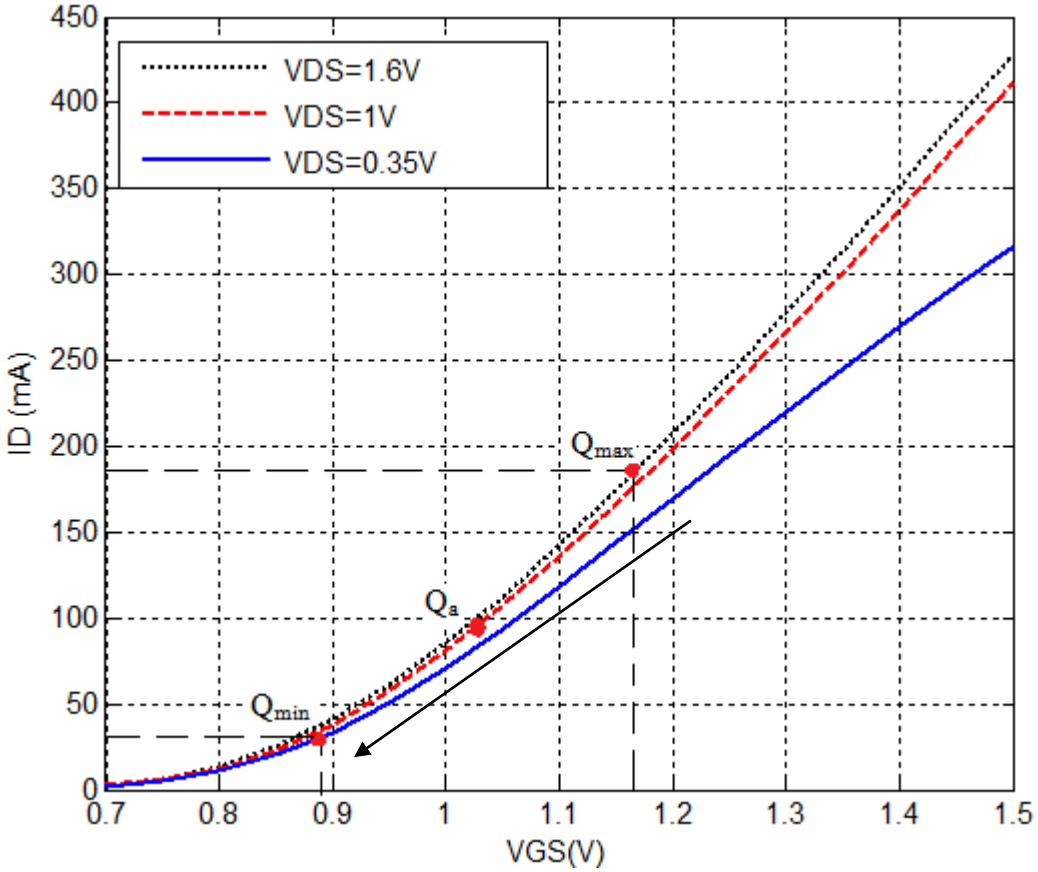


Figure 4.3 Plot of Bias Current vs. Gate Bias Voltage for Dynamic Biased PA

Now, the peak output voltage variations are measured by applying an amplitude modulated signal to the input of the PA with dynamic gate bias and measuring the corresponding peak variations in the output signal delivered to the load. The minimum drain voltage required at each operating point is obtained by adding V_{DSAT} to the peak output voltage variations and adding an offset between 50mV and 100mV to allow some safety margin. Figure 4.4 shows the relationship between the peak output voltage and the drain voltage.

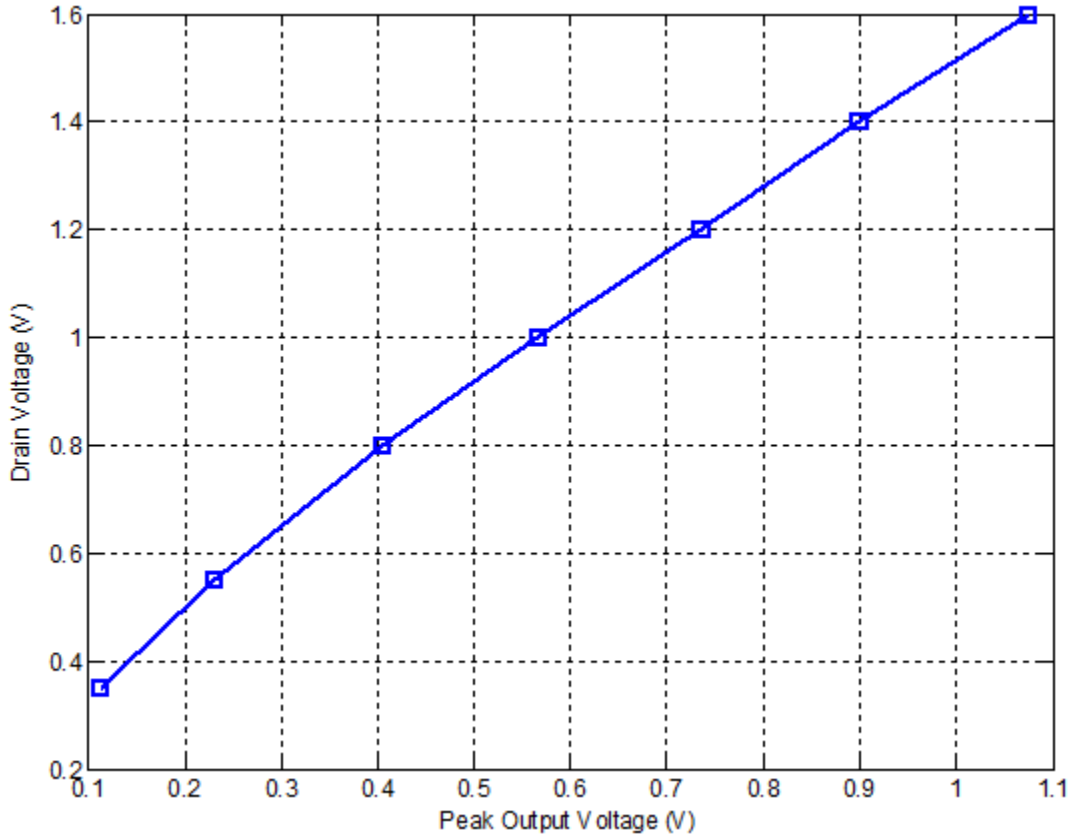
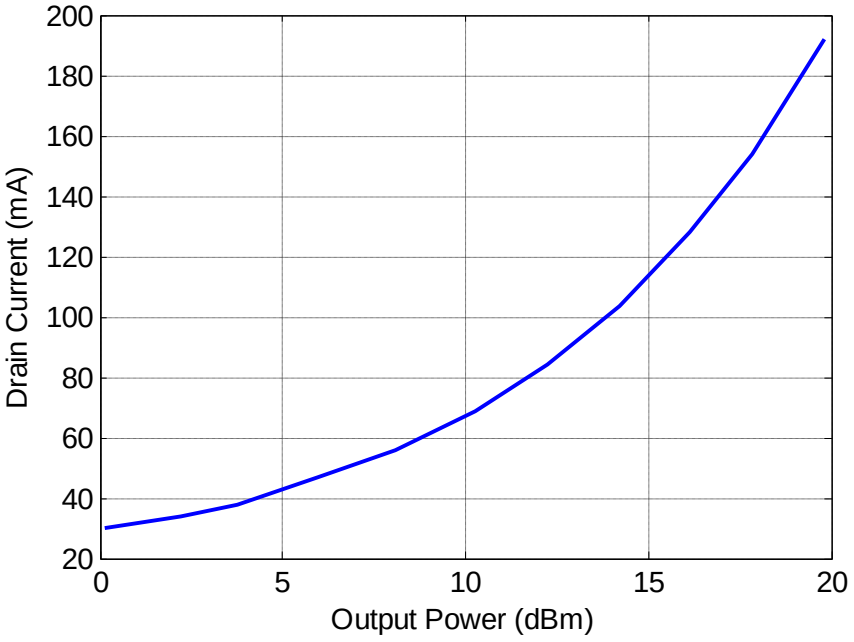
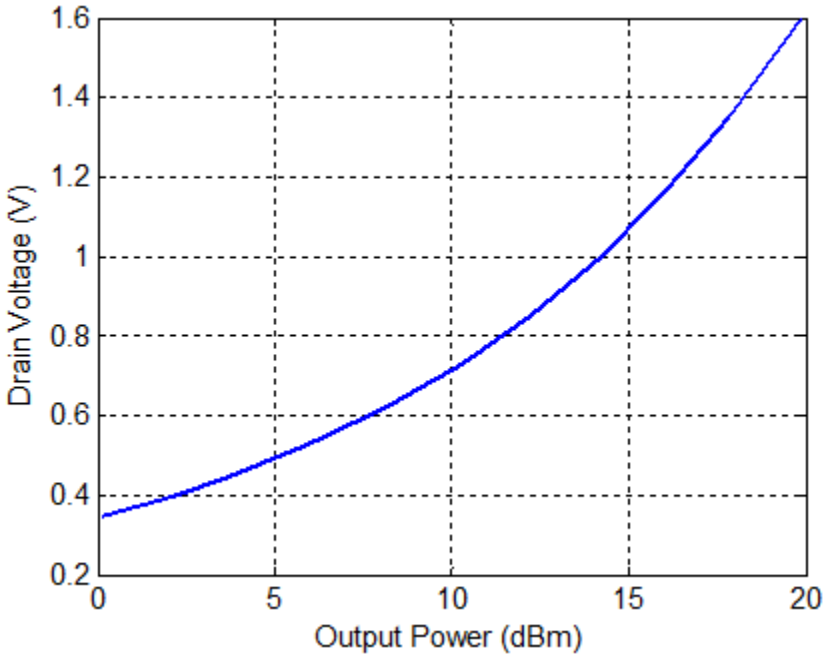


Figure 4.4 Plot of Drain Voltage against Peak Output Voltage

For each peak output voltage expected at the output of the PA, the supply modulator has to generate the corresponding drain voltage in Figure 4.4. Note that the minimum drain voltage is limited to 0.35V. Based on this characterization, a plot of the drain current and drain voltage against the output power delivered to the load is shown in Figure 4.5(a) and 4.5(b) respectively.



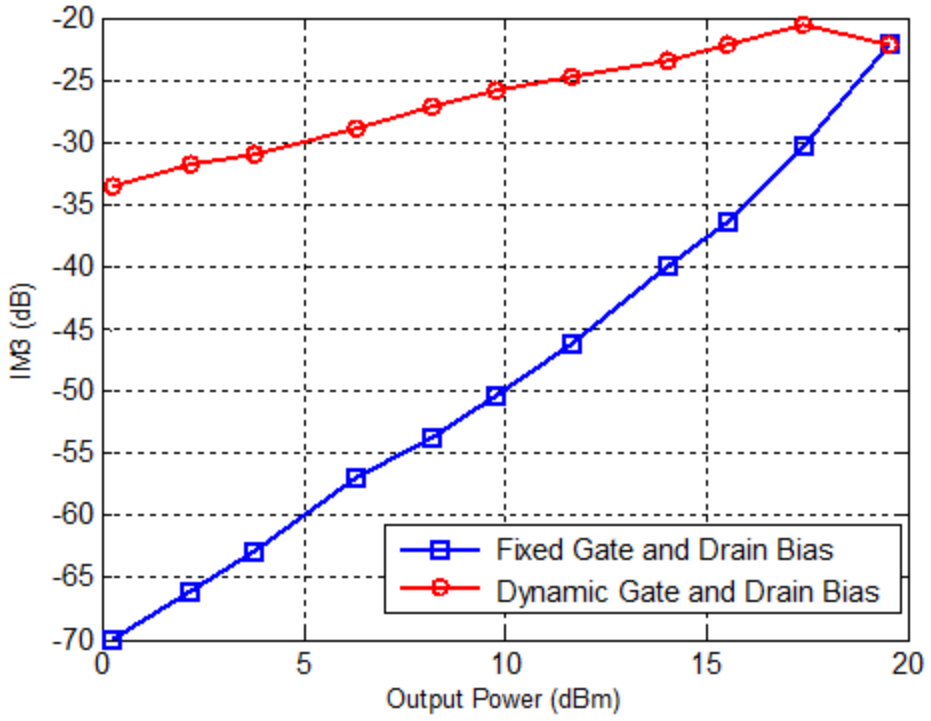
(a)



(b)

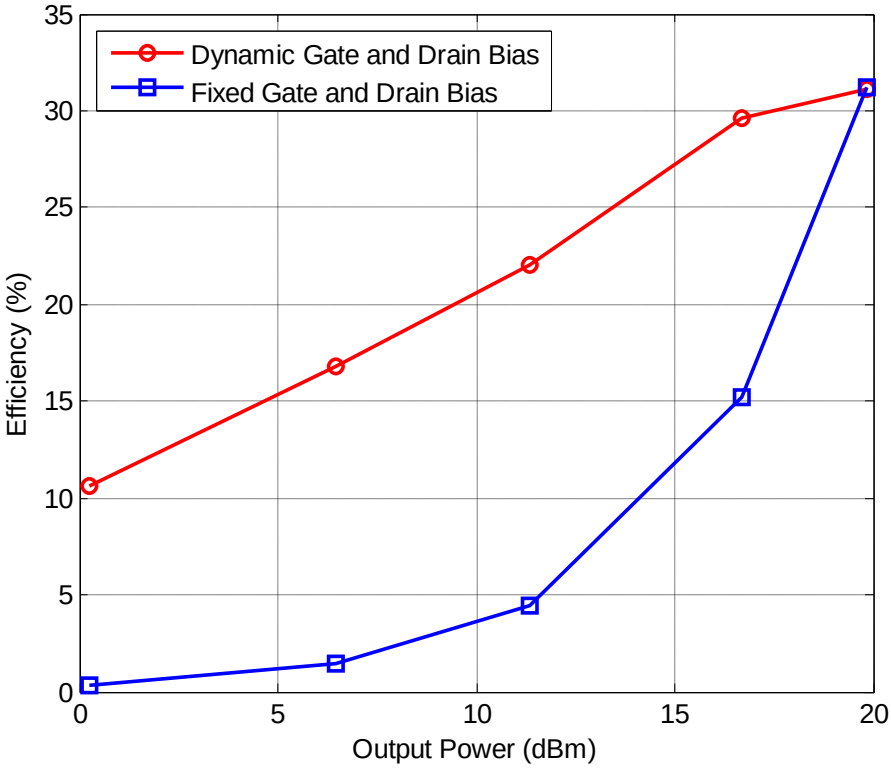
Figure 4.5 Plot of (a) Drain Current and (b) Drain Voltage against Output Power

The PA is characterized to measure its linearity performance and efficiency for a fixed bias and a combination of dynamic gate and drain bias. The linearity is measured by applying two tone signals of equal amplitude spaced equally at 4MHz from the carrier to the input and measuring the third order intermodulation distortion (IM3). This measurement is done for different signal amplitudes in order to observe how linearity varies with output power delivered to the load. Figure 4.6(a) and 4.6(b) show plots of the IM3 and efficiency of the fixed bias PA and dynamically biased PA against output power respectively.



(a)

Figure 4.6 Plot of (a) IM3 of PA vs. Output Power and (b) Efficiency of PA vs. Output Power



(b)

Figure 4.6 Continued

It is observed from Figure 4.6(a) and 4.6(b) that linearity is sacrificed for efficiency by using dynamic biasing. The improvement in efficiency at the expense of linearity is the price we pay for using dynamic biasing. However, it should be noted that typically at each output power, dynamic biasing is used to reduce the bias current and drain voltage until the linearity performance is just enough for a target application. In this work, an IM3 value better than -20 dB is used as the target reference specification for linearity. The linearity and efficiency of the fixed bias and dynamic bias PA become equal at maximum power. It should be noted that the efficiency values shown in Figure 4.6(b) for the dynamically biased PA will be obtained if the switching regulator is able to replicate the drain voltage with zero error and the switching regulator is 100% efficient. The linearity performance will also be maintained if the switching regulator is

able to replicate the drain voltage with zero error. If the drain voltage produced by the switching regulator is less than the ideal values shown in Figure 4.6 then its linearity performance will be worse than Fig 4.6(a) but its efficiency will be better than Fig 4.6(b). The TSMC 0.18um technology limits the maximum power to about 19.5dBm. So to calculate the average power efficiency of the PA in a CDMA handset, we extrapolate the plot of the drain voltage and drain current against output power up to 28dBm so we can calculate the expected efficiency of the PA up to 28dBm. The average power consumption and average power transmitted for the dynamically biased PA are plotted in Figure 4.7 using the urban probability distribution function for CDMA in Figure 2.2. The average efficiency is computed as

$$\text{Average Efficiency} = \frac{\text{Average Power Transmitted}}{\text{Average Power Consumption}} \tag{4.8}$$

$$= \frac{0.0186}{0.0712}$$

$$= 26.1\%$$

A fixed bias PA in a CDMA will have a static power consumption of 1.76W and hence the average efficiency will be 1.06%.

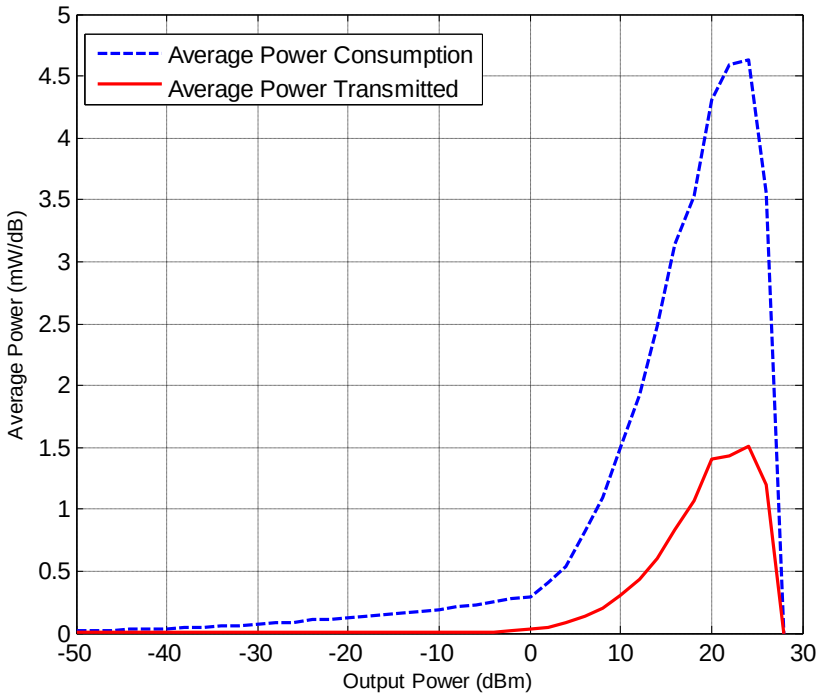


Figure 4.7 Plot of Average Power in a CDMA Handset

Now that we have observed the efficiency improvement gained by using dynamic biasing over a fixed bias PA, we look at the various design considerations for implementing the proposed supply modulator.

4.2 Selection of L and C Components

In the discussion on the slew rate of the switching regulator, it was realized that the size of the L and C components and the initial circuit conditions determine the slew rate of the switching regulator. It should be remembered that the proposed approach relies on the fact that the large and fast variations in the envelope signal are infrequent and occur only about 10% of the time. In this design, the switching regulator is designed to handle envelope variations with bandwidths up to 4MHz without any help from the bang-bang controller. As a result the inherent slew rate of the switching regulator should

be enough to handle such envelope variations. To achieve this, the slew rate required will be 16mV/ns. Thus from Figure 3.18(a), $f_o \geq 4.6MHz$ and hence $LC \leq 1.2*10^{-15}$.

Thus there seems to be a lot of flexibility in choosing L and C. This result suggests that a large L and small C might be a good option because it relaxes the amount of current required by the bang-bang controller to meet the slew rate requirements. However, it should be remembered that the PA presents a dynamic load to the switching regulator. As a result, for envelope variations within the natural bandwidth of the switching regulator, the load capacitor should be large enough to supply the current required by the PA when the inductor is not able to respond quick enough to supply the required current. From simulations, with $L = 330nH$ and $C = 3.6nF$, the switching regulator is able to support envelope variations up to 4MHz without any help from the bang-bang controller.

4.3 Design of Error Amplifier and Compensation Network

The main design considerations for the error amplifier (EA) are:

1) A high gain over a wide frequency range. This is required to make sure the loop regulates to the desired reference level across a wide frequency range. A DC gain greater than 60dB is used in this design.

2) A wide common mode range. The envelope signal is required to vary from 0.35 V to 1.6 V with a 2V supply. Thus the input common mode range of the amplifier is required to be wide so that the error amplifier can operate properly within this range of voltages.

3) The parasitic poles of the error amplifier must be located at frequencies much higher than the bandwidth of the switching regulator to prevent them from affecting the stability of the system.

Thus, the PMOS input two stage amplifier shown in Figure 4.8 is used as the error amplifier. The dimensions of the transistors used for implementing the error amplifier are shown in Table 4.1.

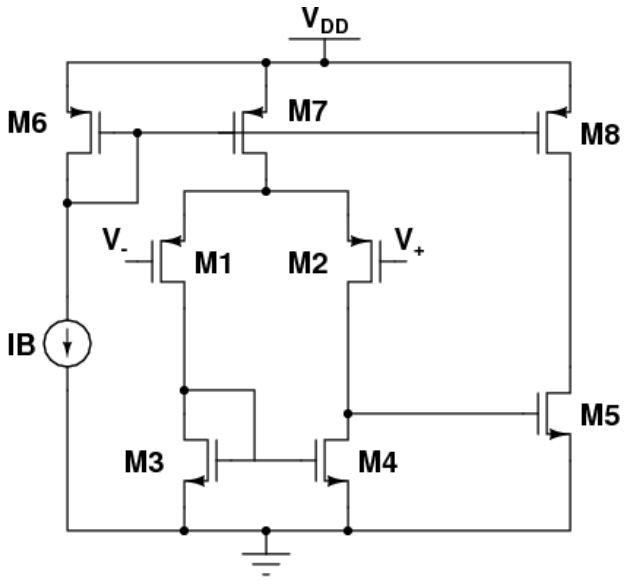


Figure 4.8 Schematic Diagram of Error Amplifier

Table 4.1 Circuit Parameters of Error Amplifier

Transistor	W(μm)	L (μm)	Bias Current (μA)
M1,M2	8	0.24	40
M3,M4	4	0.36	40
M5	16	0.36	160
M6	8	0.36	80
M7	8	0.36	80
M8	16	0.36	160

It should be noted that the switching regulator has an internal feedback loop formed by the error amplifier and the compensation network. The error amplifier by itself is not internally compensated since compensating the stand alone error amplifier limits the unity gain frequency of the loop and hence limits the bandwidth of the

switching regulator. However, the compensation network added to the error amplifier in Figure 4.9 compensates the error amplifier thus making it feedback stable.

During the discussion on stability, we realized that we needed a PID controller to compensate the feedback loop of the supply modulator. The PID controller shown in Figure 4.9 is used to stabilize the supply modulator.

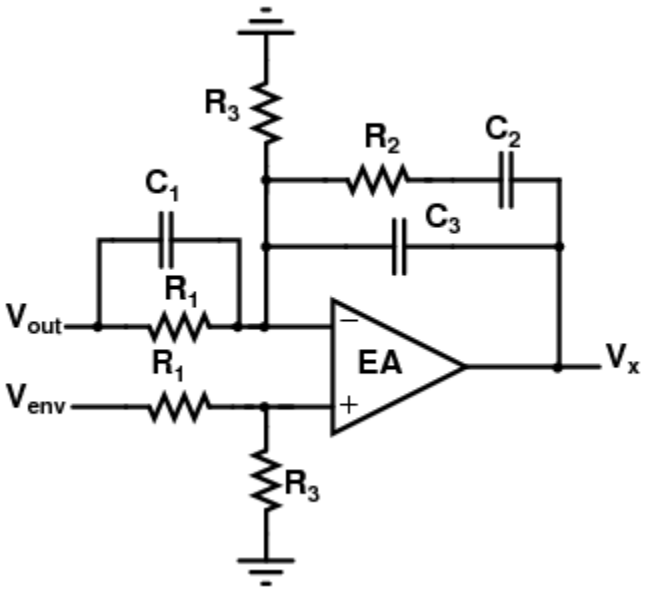


Figure 4.9 Schematic Diagram of Compensation Network

The transfer function of this network is given by[27]

$$\frac{V_x(\mathrm{s})}{V_{out}(s)} = \frac{-1}{sR_1(C_2+C_3)} \frac{(1+sR_1C_1)(1+sR_2C_2)}{(1+sR_2\frac{(C_2C_3)}{(C_2+C_3)})} \tag{4.9}$$

Note that the resistor divider formed by R_1 and R_3 scales down the output voltage and envelope signal before they are applied to the input of the error amplifier. Thus even though the output voltage and envelope signal vary within a wide range (0.35V-1.6V), the voltage variation at the inputs of the error amplifier is actually smaller. As a result, the input common mode requirements of the error amplifier are relaxed.

With the natural frequency of the LC filter located at 4.6MHz, the zeros of the compensation network are placed at 2.2MHz and 8.8MHz to stabilize the loop. A high frequency pole is placed around 100MHz to help attenuate high frequency switching harmonics present in the output voltage of the supply modulator. Table 4.2 shows the values of the components used to design the compensation network.

Table 4.2 Component Values of Compensation Network

Component	Value
R_1	18kΩ
R_2	18kΩ
R_3	95kΩ
C_1	4pF
C_2	1pF
C_3	100fF

The simulated loop magnitude and phase response is shown in Figure 4.10 and Figure 4.11 for maximum and minimum loading conditions respectively. This response is obtained by performing a periodic steady state analysis on the switching regulator in CADENCE for it to attain steady state and then performing a periodic stability analysis by inserting a probe in the loop of the switching regulator as shown in Figure 4.12. The frequency response shows that the loop has a unity gain frequency of 20MHz and a worse case phase margin of 49^0 thus guaranteeing stable operation.

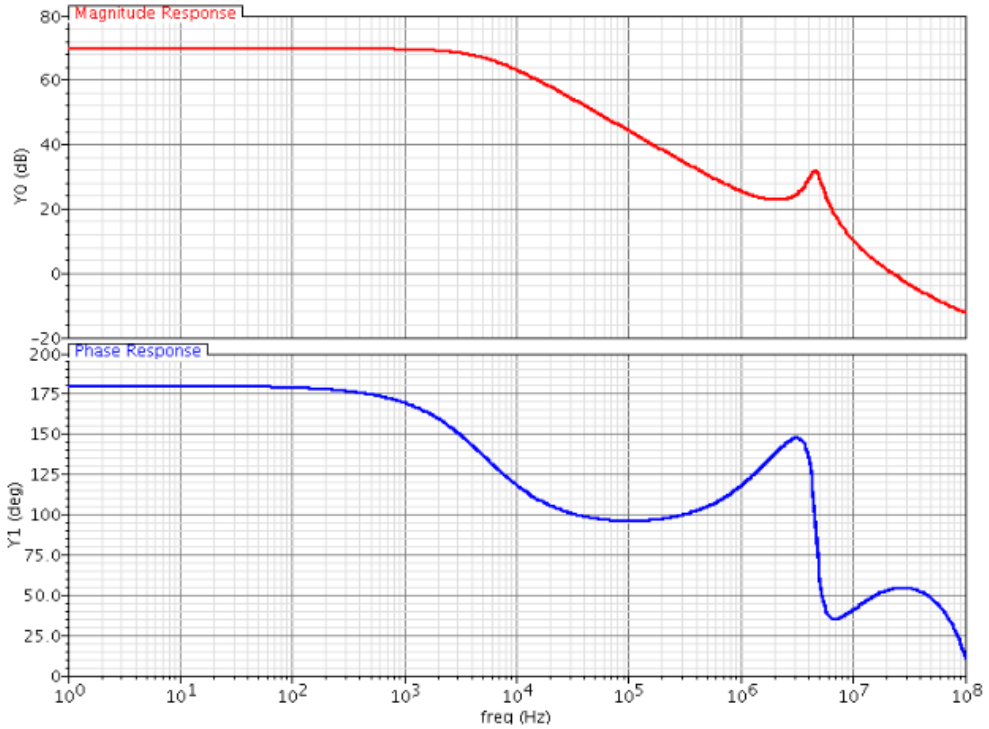


Figure 4.10 Loop Magnitude and Phase Response at Maximum Load

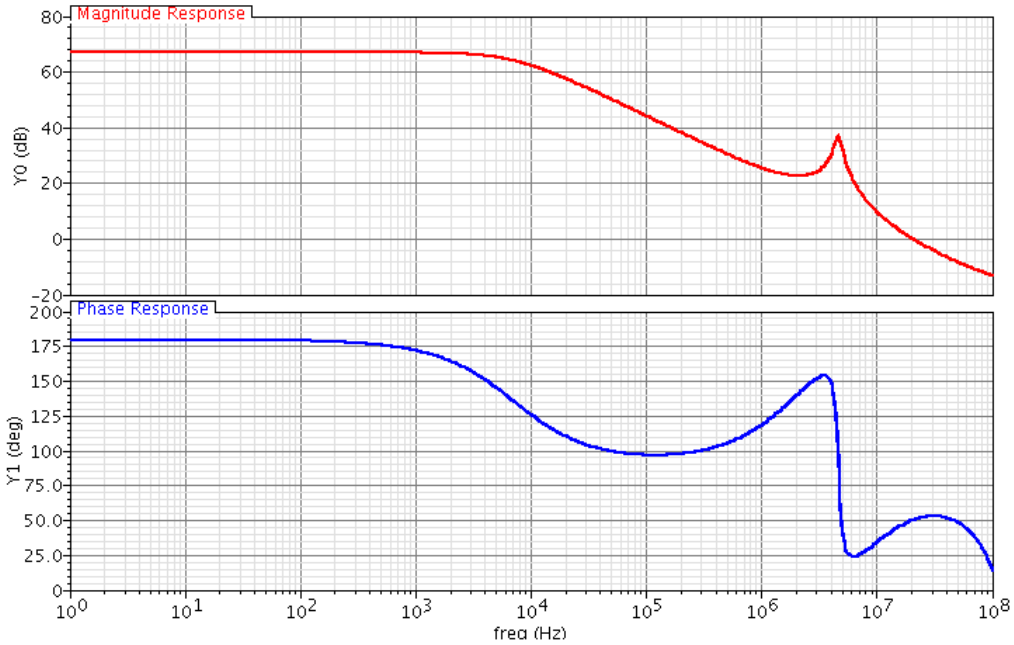


Figure 4.11 Loop Magnitude and Phase Response at Minimum Load

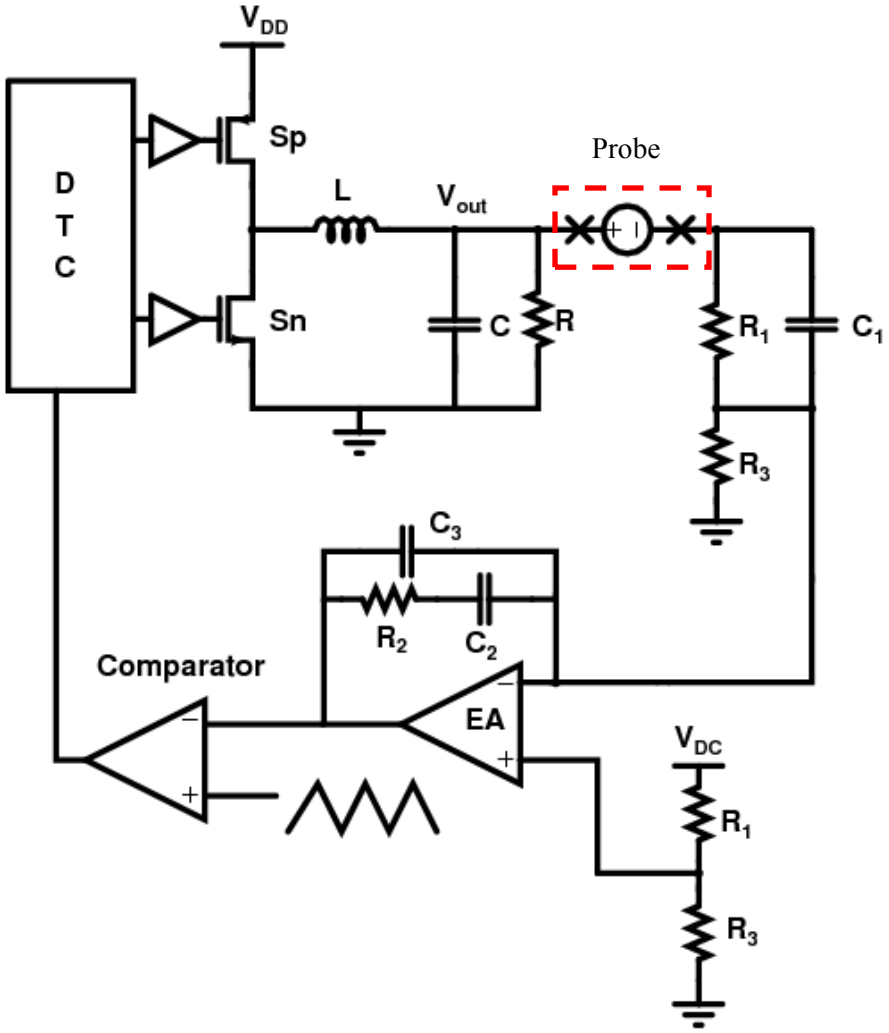


Figure 4.12 Set-up for Measuring Loop Magnitude and Phase Response

A step response is performed on the switching regulator by applying a voltage pulse from 0.35V to 1.6V with 80ns rise and fall times at the reference input of the switching regulator. The response of the switching regulator to this step is shown in Figure 4.13. This confirms that the loop is stable.

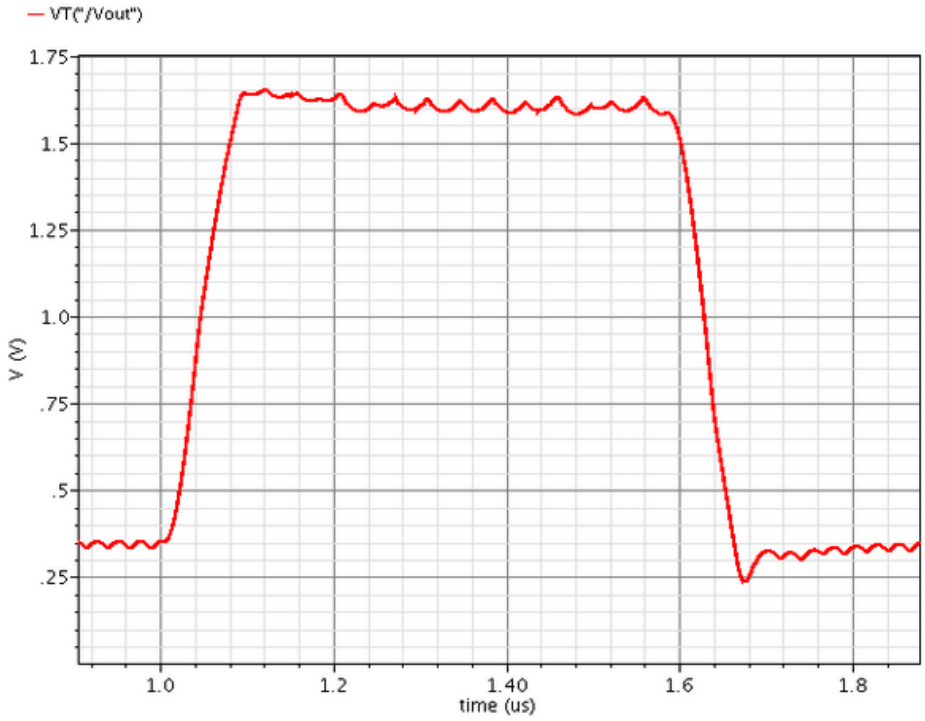


Figure 4.13 Step Response of Switching Regulator

4.4 Selection of Switching Frequency

Now that the L and C components have been selected, equation (3.33a) is used to select the switching frequency to obtain a maximum ripple voltage of 25mV. From this equation, the switching frequency can be expressed as

$$f_{sw} \geq \sqrt{\frac{\left(1-\frac{V_o}{V_{DD}}\right)V_o}{8LC\Delta V}} \tag{4.9}$$

Thus $f_{sw} \geq 46MHz$. Since the loop bandwidth is 20MHz, a switching frequency of 80MHz is used in this design in order to allow good rejection of switching noise and reduce the effect of switching harmonics on the operation of the PWM.

4.5 Design of Comparator

The most critical parameter of the pulse width modulator is propagation delay. The propagation delay of the comparator limits the response time of the switching

regulator. With a switching frequency of 80MHz, a 12.5ns time window is available for making a switching decision. Any delays in the comparator reduce the available time for making a switching decision. Thus the comparator is designed for a propagation delay less than 2ns with a 100mV overdrive. The schematic diagram of the comparator is shown in Figure 4.14.

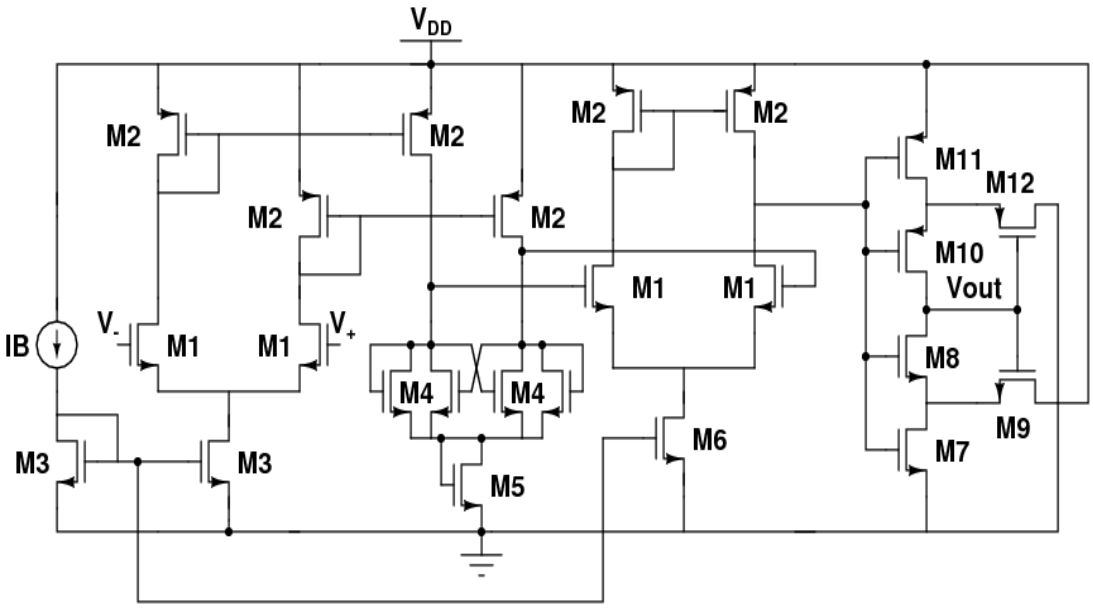


Figure 4.14 Schematic Diagram of Comparator

The input stage is designed to provide some gain to increase the minimum signal that the comparator needs to make a decision. This stage amplifies the difference between the input signals and the positive feedback loop formed by transistors M4 increase the gain and enables the circuit to arrive at a decision by determining which input signal is larger. This decision is amplified by a differential gain stage to restore the output to digital. The Schmitt trigger at the output of this gain stage helps restore the output signal to full logic level and makes the circuit more noise tolerant by adding hysteresis. Table 4.3 shows the transistor dimensions used in the design.

Table 4.3 Circuit Parameters of Comparator

Transistor	W(μm)	L (μm)	Bias Current (μA)
M1	1.6	0.24	40
M2	2.4	0.24	40
M3	8	0.40	80
M4	20	0.20	-
M5	8	0.40	80
M6	20	0.20	80
M7	1	0.18	-
M8	1	0.18	-
M9	0.4	0.18	-
M10	1	0.18	-
M11	2	0.18	-
M12	2	0.18	-

4.6 Design of Non-overlapping Control Signal Generator

From our discussion on short-circuit power losses, we realized that we needed non-overlapping clocks to introduce dead times into the clocks used to control the power switches to prevent the occurrence of short-circuit power loss. The non-overlapping clock generator shown in Fig 4.15 is used to implement the dead time control (DTC). The dead time is determined by the propagation delay through the NOR gates and the inverters at the output of the NOR gates.

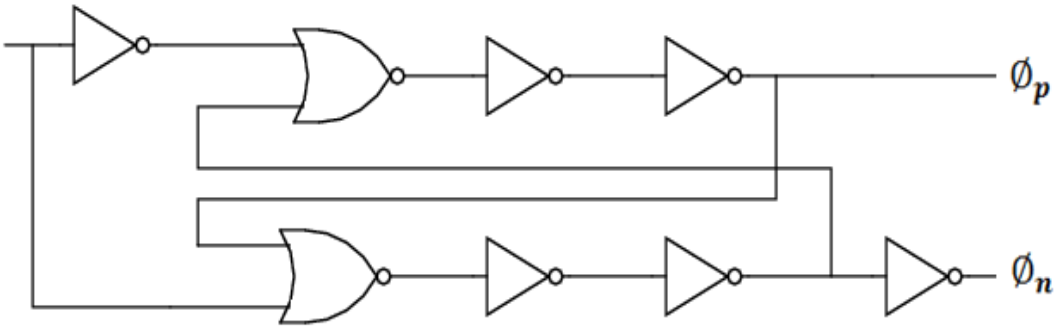


Figure 4.15 Logic Diagram of Non-overlapping Clock Generator

4.7 Design of Power Switches and Switch Drivers

The power switches S_p and S_n are implemented with PMOS and NMOS transistors respectively. They are sized to optimize switching losses and conduction losses. The switching regulator is designed for equal switching and conduction losses when the static power consumption is equal to an average power consumption of 71.5mW. This corresponds to a dc current of 80mA drawn from the PA and a drain voltage of 0.89V. From equation (3.14b), C_p/R_{ON}=20pF/Ω.

Thus the dimensions of the switch have to be adjusted until the ratio of C_p to R_{ON} is equal to about 20pF/Ω. The final dimensions of the power switches are shown in Table 4.4 with their switch on-resistance and parasitic capacitance.

Table 4.4 Switch Dimensions with their On-resistance and Parasitic Capacitance

Switch	W(μm)	L(μm)	R_{ON}(mΩ)	C_p (pF)
S_p	3072	0.18	713	8.15
S_n	768	0.18	695	2.56

The switch drivers are sized to optimize propagation delay and power dissipation.

4.8 Design of Bang-bang Controller

The transistor level design considerations for the bang-bang controller circuit of Figure 4.16 are shown in this section.

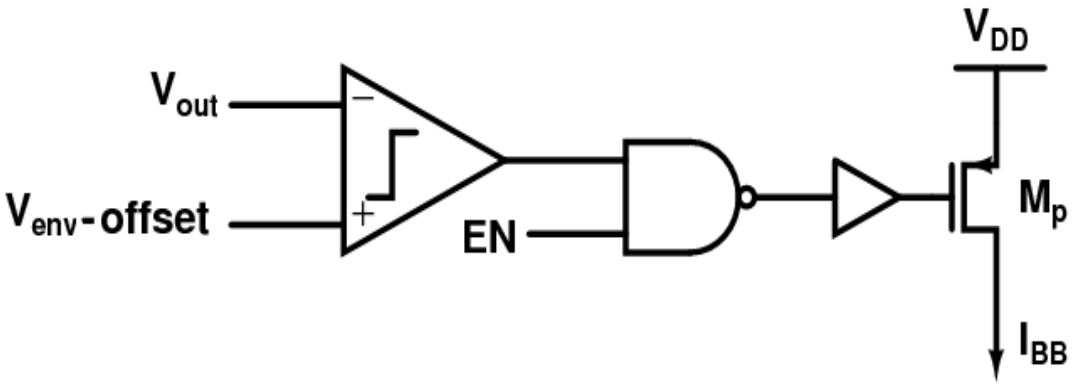


Figure 4.16 Schematic Diagram of Bang-bang Controller

The bang-bang controlled current source is required to help the switching regulator to meet the slew rate requirements. From equation (3.37b), $I_{BB}=SR_{BB}.C$. Thus with C=3.6nF and a required slew rate of SR_{BB}=100.5mV/ns,I_{BB}=361.8mA.

The bang-bang controlled current source is sized to produce this amount of current. The bang-bang current source is a PMOS transistor operating in the triode region. The size of the PMOS transistor is given by

$$\frac{W}{L}=\frac{I_{BB}}{\mu C_{ox}\left[(V_{DD}-V_T)V_{DS}-\frac{{V_{DS}}^2}{2}\right]} \tag{4.10}$$

with μC_{ox}=74μA/V^2, V_T=0.5V ,V_{DS}=0.5V and $\frac{W}{L}\cong$7824.

Using L=180nm, W=1.41m. The final dimensions of the PMOS transistor are L=0.18um and W=1664um.

The most critical parameters of the comparator used to control the current source are speed and common mode range. The propagation delay of the comparator limits the response time of the bang-bang controller and hence introduces errors in the voltage

produced by the supply modulator. As a result the propagation delay of the comparator is designed to be less than 1ns for a 100mV overdrive. The input common mode range of the comparator is required to be from 0.3V to 1.6V since the envelope signal varies within this range. As a result the comparator is designed to have a rail-rail input stage. The schematic diagram of the comparator is shown in Figure 4.17.

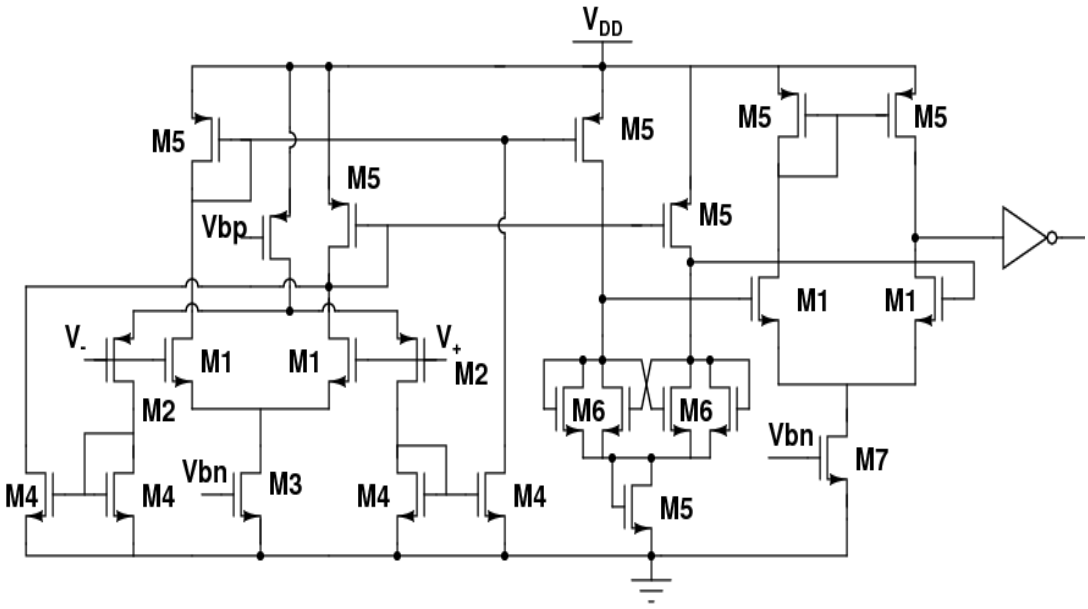
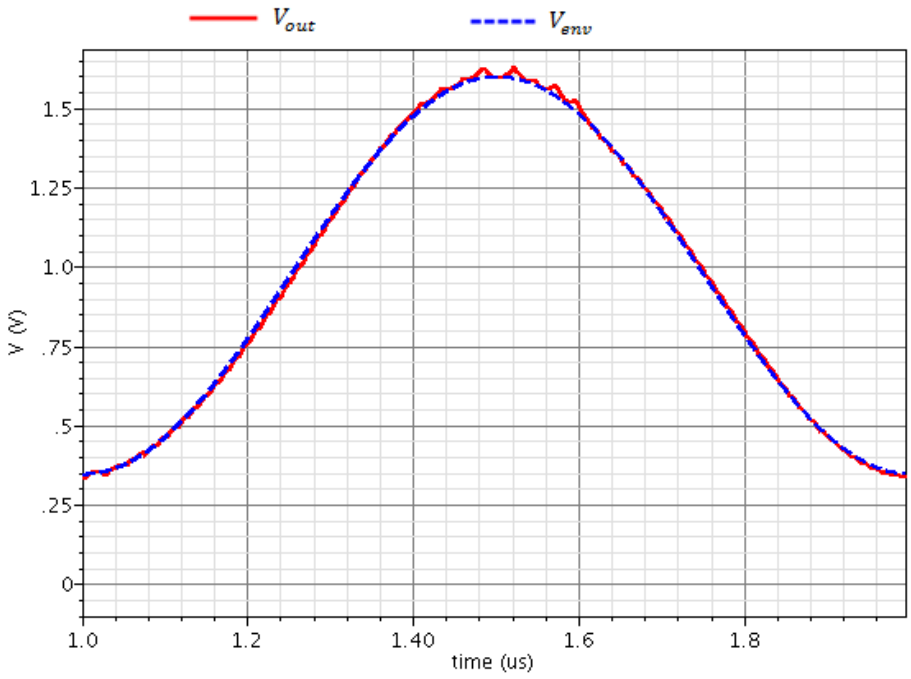


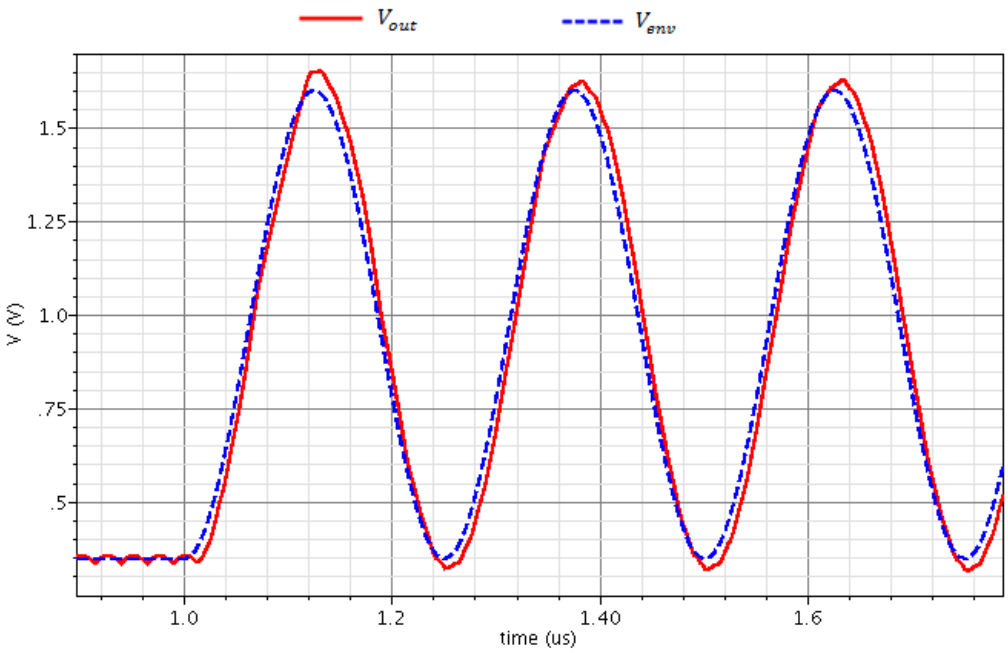
Figure 4.17 Schematic of Bang-bang Comparator [29]

4.9 Simulation Results

The simulation results for the proposed supply modulator are shown in this section. A reference signal is applied to the input of the supply modulator and the signal produced at the output plotted. Fig 4.18(a) and 4.18(b) shows a plot of the output voltage and the reference signal for a 1MHz and 4MHz signal respectively. These plots show that the proposed supply modulator is able to handle envelope variations up to 4MHz.



(a)



(b)

Figure 4.18 Plot of Envelope Signal and Output Voltage for a (a) 1MHz and (b) 4MHz Signal

Fig 4.19 shows a plot of the output voltage and a 20MHz reference signal with and without the bang-bang controller. It is noticed that without the bang-bang controller the output voltage is not able to follow the reference signal properly.

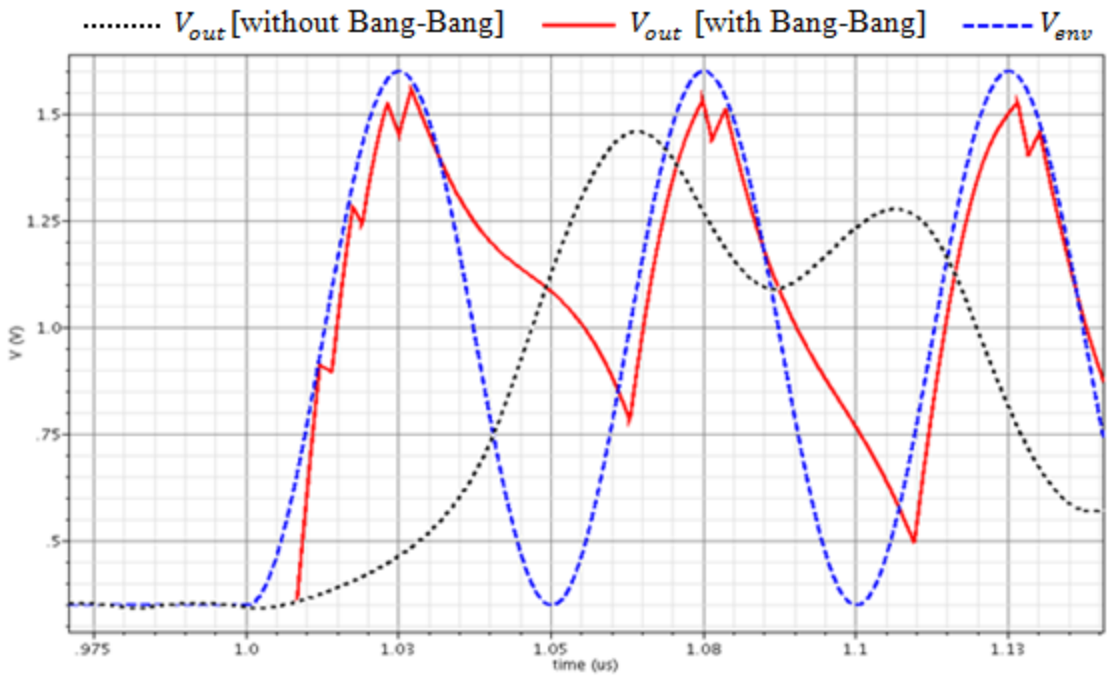


Figure 4.19 Plot of Envelope Signal and Output Voltage with and without Bang-bang Controller for a 20MHz Signal

Finally, the efficiency of the supply modulator is measured using CADENCE for dc signals as

$$Efficiency = \frac{I_{out} V_{out}}{I_{DC} V_{DD}} \tag{4.11}$$

where I_{out} is the DC current supplied to the PA, V_{out} is the DC drain supply voltage of the PA, V_{DD} is the battery supply voltage and I_{DC} is the average value of the current drawn from V_{DD}. The efficiency is obtained for different output power transmitted and plotted in Figure 4.20. The average power efficiency of the supply modulator is found to be 81.6%.

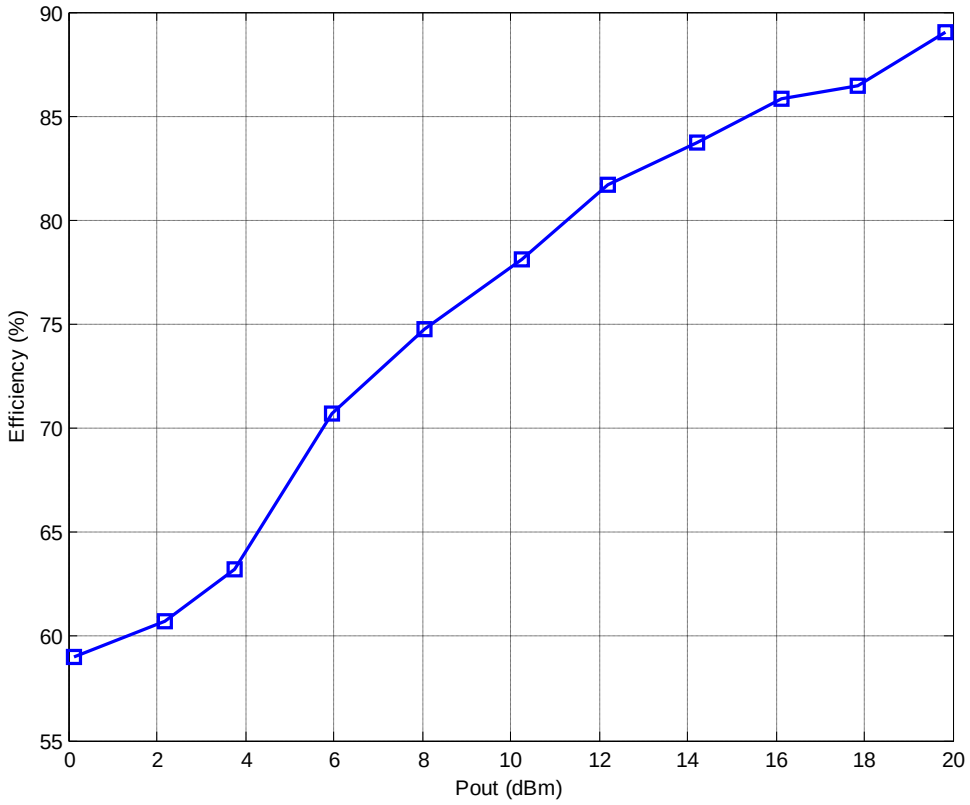


Figure 4.20 Plot of Efficiency of Supply Modulator vs. Output Power

A summary of the design parameters of the supply modulator are shown in Table 4.5. Table 4.6 shows how the proposed supply modulator compares with state-of-the-art. It is noticed that the proposed supply modulator simultaneously achieves a high bandwidth and high average power efficiency.

Table 4.5 Summary of Performance Parameters of Supply Modulator

Supply Voltage	2V
Output Voltage Range	0.35 – 1.6V
Maximum Output Power (RMS)	19.5 dBm
Quiescent Current (I_{bias})	0.92mA
Maximum Envelope Bandwidth	20MHz
Switching Frequency	80MHz
Output Inductance, L,	330nH
Load Capacitance, C	3.6nF
Average Efficiency of Supply Modulator	81.6 %
Average Efficiency with a Linear PA	21.3%

Table 4.6 Comparison of Results

Performance Parameter	**[15]**	**[18]**	**[20]**	**Proposed Architecture**
Technology	0.18um SiGe BiCMOS	0.065um CMOS	0.35um CMOS	0.18um CMOS
Maximum Envelope Bandwidth	20MHz	20MHz	2.5MHz	20MHz
Average Modulator Efficiency	65%	*59%	*30%	81.6%

* Efficiency at 16dBm

5. CONCLUSIONS

The design of an efficient supply modulator for wideband power amplifiers has been described in this thesis. A switching regulator with a bang-bang controlled current source has been proposed for use as the supply modulator for wideband linear RF PAs. The proposed supply modulator has been shown to work for bandwidths up to 20MHz. The supply modulator has negligible quiescent current consumption, is easy to stabilize, has high efficiency and is simple to design because of its bang-bang nature. It achieves an average power efficiency of 81.6%.

The performance of the proposed supply modulator is limited by the speed of the bang-bang controller. A slow bang-bang control will reduce the response time of the supply modulator and cause large ripple voltages in the output. More intelligent control schemes using software can be used to improve the performance of the system.

In summary, the speed response of the supply modulator is a tradeoff between ripple voltage, slew rate and power efficiency. Future research should focus on more intelligent control mechanisms for controlling the static power consumption of the PA while maintaining good linearity performance.

A class A PA in a CDMA handset is shown to achieve an average power efficiency of 21.3% when the gate and drain of the PA are dynamically biased with the proposed supply modulator compared to an efficiency of only 1.06% for a fixed bias PA.

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APPENDIX

The slew rate of the switching regulator is derived below for a step applied to the LC filter of the switching regulator.

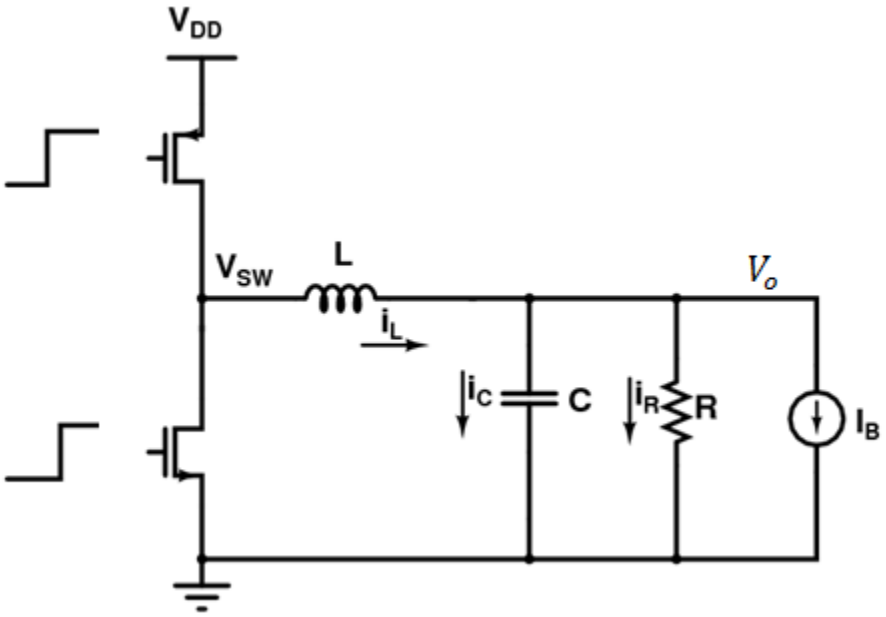

Figure A.1 Simplified Schematic for Obtaining Slew Rate

Figure A.1 shows a model of the switching regulator with the power amplifier modeled as a resistive load R in parallel with a current source I_B.

$$i_L = i_C + i_R + I_B$$

$$i_L = C\frac{dV_o(t)}{dt} + \frac{V_o(t)}{R} + I_B$$

$$\frac{di_L}{dt} = C\frac{d^2V_o(t)}{dt^2} + \frac{dV_o(t)}{Rdt}$$

$$\frac{di_L}{dt} = \frac{V_{sw} - V_o(t)}{L}$$

$$\frac{V_{sw} - V_o(t)}{L} = C\frac{d^2V_o(t)}{dt^2} + \frac{dV_o(t)}{Rdt}$$

$$\frac{V_o(t) - V_{sw}}{L} + C\frac{d^2V_o(t)}{dt^2} + \frac{dV_o(t)}{Rdt} = 0$$

$$V_o(t) + LC\frac{d^2V_o(t)}{dt^2} + \frac{L}{R}\frac{dV_o(t)}{dt} = V_{sw}$$

$$LC\frac{d^2V_o(t)}{dt^2} + \frac{L}{R}\frac{dV_o(t)}{dt} + V_o(t) = V_{sw}$$

$$V_o(t) = V_c(t) + V_p(t)$$

$$V_c(t) = A_1e^{s_1t} + A_2e^{s_2t}$$

$$V_p(t) = V_{sw}$$

$$Where\ s_1 = -\frac{1}{2RC} + \sqrt{(\frac{1}{2RC})^2 - \frac{1}{LC}}$$

$$And\ s_2 = -\frac{1}{2RC} - \sqrt{(\frac{1}{2RC})^2 - \frac{1}{LC}}$$

$$V_o(t) = A_1e^{s_1t} + A_2e^{s_2t} + V_{sw}$$

$$\frac{dV_o(t)}{dt} = s_1A_1e^{s_1t} + s_2A_2e^{s_2t}$$

$$V_o(0) = A_1 + A_2 + V_{sw} - - - - - (1)$$

$$\frac{dV_o(0)}{dt} = s_1A_1 + s_2A_2 = \frac{i_c(0)}{C} - - - - - (2)$$

$$i_c(0) = i_L(0) - \frac{V_o(0)}{R} - I_B$$

Solving the equation,

$$A_1 = \frac{s_2(V_{sw} - V_o(0))}{s_1 - s_2} + \frac{i_c(0)}{C(s_1 - s_2)}$$

$$A_2 = \frac{s_1(V_o(0) - V_{sw})}{s_1 - s_2} - \frac{i_c(0)}{C(s_1 - s_2)}$$

$$\frac{dV_o(t)}{dt} = \frac{(V_{sw} - V_o(0))s_1s_2}{s_1 - s_2}e^{s_1t} + \frac{(V_o(0) - V_{sw})s_1s_2}{s_1 - s_2}e^{s_2t} + \frac{i_c(0)s_1e^{s_1t}}{C(s_1 - s_2)} - \frac{i_c(0)s_2e^{s_2t}}{C(s_1 - s_2)}$$

$$\frac{dV_o(t)}{dt} = \frac{(V_{sw} - V_o(0))s_1s_2}{s_1 - s_2}e^{s_1t} - \frac{(V_{sw} - V_o(0))s_1s_2}{s_1 - s_2}e^{s_2t} + \frac{i_c(0)s_1e^{s_1t}}{C(s_1 - s_2)} - \frac{i_c(0)s_2e^{s_2t}}{C(s_1 - s_2)}$$

$$\frac{dV_o(t)}{dt} = \frac{(V_{sw} - V_o(0))s_1 s_2}{s_1 - s_2}(e^{s_1 t} - e^{s_2 t}) + \frac{i_c(0)s_1 e^{s_1 t}}{C(s_1 - s_2)} - \frac{i_c(0)s_2 e^{s_2 t}}{C(s_1 - s_2)} \qquad for\ 0 \le t \le DT$$

***CASE I*(*Underdamped Response*)**

$s_1 and\ s_2\ be\ complex\ conjugates\ such\ that\ s_1 = -a + jb\ and\ s_2 = -a - jb$

$$\frac{dV_o(t)}{dt} = \frac{\big(V_{sw} - V_o(0)\big)(a^2 + b^2)e^{-at}\sin bt}{b} + \frac{i_c(0)}{bC}[e^{-at}][\mathrm{b}\cos bt - \mathrm{a}\sin bt]$$

$$In\ this\ case\ a = \frac{1}{2RC}\ and\ b = \sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}}$$

$$\frac{dV_o(t)}{dt} = \frac{\big(V_{sw} - V_o(0)\big)e^{-\frac{t}{2RC}}\sin bt}{LC\sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}}} + \frac{i_c(0)}{C\sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}}}\left[e^{-\frac{t}{2RC}}\right][b\cos bt - asinbt]$$

$$\frac{dV_o(t)}{dt} = \frac{\big(V_{sw} - V_o(0)\big)e^{-\frac{t}{2RC}}\sin bt}{\sqrt{LC - \frac{L^2}{4R^2}}} + \frac{i_c(0)}{C\sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}}}\left[e^{-\frac{t}{2RC}}\right][b\cos bt - asinbt]$$

Considering $i_c(0) \cong 0\ for\ a\ very\ small\ ripple$

$$\frac{dV_o(t)}{dt} = \frac{\big(V_{sw} - V_o(0)\big)e^{-\frac{t}{2RC}}\sin bt}{\sqrt{LC - \frac{L^2}{4R^2}}}$$

$$\left|\frac{dV_o(t)}{dt}\right| = \frac{\big(V_{sw} - V_o(0)\big)e^{-\frac{t}{2RC}}}{\sqrt{LC - \frac{L^2}{4R^2}}}$$

$$\left|\frac{dV_o(t)}{dt}\right| = \frac{\big(V_{sw} - V_o(0)\big)e^{-\frac{t}{2RC}}}{LC\sqrt{\frac{1}{LC} - \frac{1}{4R^2C^2}}} \qquad for\ 0 \le t \le DT$$

***CASE II*(*Critically Damped Response*)**

$s_1 = s_2 = -a$

$V_o(t) = B_1 te^{-at} + B_2 e^{-at} + V_{sw}$

$$\frac{dV_o(t)}{dt} = -aB_1te^{-at} - aB_2e^{-at} + B_1e^{-at}$$

$$V_o(0) = B_2 + V_{sw}$$

$$B_2 = V_o(0) - V_{sw}$$

$$\frac{dV_o(0)}{dt} = B_1 - aB_2 = \frac{i_c(0)}{C}$$

$$B_1 = \frac{i_c(0)}{C} + aB_2 = \frac{i_c(0)}{C} + a(V_o(0) - V_{sw})$$

$$\frac{dV_o(t)}{dt} = -aB_1te^{-at} - aB_2e^{-at} + B_1e^{-at}$$

$$\frac{dV_o(t)}{dt} = e^{-at}(-aB_1t - aB_2 + B_1)$$

$$\frac{dV_o(t)}{dt} = e^{-at}\left(-a[\frac{i_c(0)}{C} + a(V_o(0) - V_{sw})]t + \frac{i_c(0)}{C}\right)$$

$$In\ this\ case\ a = \frac{1}{2RC}\ and\ L = 4R^2C$$

$$\frac{dV_o(t)}{dt} = e^{-\frac{t}{2RC}}\left(-\frac{1}{2RC}\left[\frac{i_c(0)}{C} - \frac{1}{2RC}\left(V_{sw} - V_o(0)\right)\right]t + \frac{i_c(0)}{C}\right)$$

$$\frac{dV_o(t)}{dt} = e^{-\frac{t}{2RC}}\left(\frac{t}{4R^2C^2}\left(V_{sw} - V_o(0)\right) + \frac{i_c(0)}{C} - \frac{i_c(0)t}{2RC^2}\right)$$

$$\frac{dV_o(t)}{dt} = e^{-\frac{t}{2RC}}\left(\frac{t}{LC}(V_{sw} - V_o(0)) + \frac{i_c(0)}{C} - \frac{i_c(0)t}{2RC^2}\right)$$

Considering $i_c(0) \cong 0\ for\ a\ very\ small\ ripple$

$$\frac{dV_o(t)}{dt} = \frac{te^{-\frac{t}{2RC}}}{LC}\left(V_{sw} - V_o(0)\right) \quad for\ 0 \le t \le DT$$

$$\frac{dV_o(t)}{dt} = \frac{te^{-\frac{t}{\sqrt{LC}}}}{LC}\left(V_{sw} - V_o(0)\right) \quad for\ 0 \le t \le DT$$

$$\frac{dV_o(t)}{dt} = t\omega_o e^{-\omega_o t}\left(V_{sw} - V_o(0)\right) \quad for\ 0 \le t \le DT$$

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