ELECTRO-THERMAL EFFECTS OF POWER TRANSISTORS ON CONVERTER PERFORMANCE

by

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In this work, a comparative study of the electrical and thermal performance of a silicon carbide (SiC) MOSFET and a silicon (Si) IGBT power transistor, operating in a DC/DC boost converter, is presented. Behavioral models of Powerex Inc. switching transistors were developed in Synopsys SaberRD and used to predict the converter electrical efficiency; ANSYS Icepak modeling software was used for thermal simulations to identify potential hot spots. This work provides an overall, electro-thermal analysis of both transistor types with respect to switching frequency in the boost converter circuit. Optimal switching frequencies for each device at a given current are observed, and thermal performance of the SiC MOSFET is quantified with comparable or greater electrical efficiency to the Si IGBT. Our SiC MOSFET temperature measurements further validated published mathematical expressions, which help, in this study, to identify the best operating frequency with respect to electrical and thermal performance.

Performance analysis and design considerations from the DC/DC converter were then applied to design a 2kW, high power density, gallium nitride (GaN) based, modular multilevel converter (M2C). Half-bridge submodules for a single-phase, low voltage, high power density inverter (450 V_{DC}, 2 kW, < 40in^3 volume) were designed, constructed, and analyzed. This power density is predicted through the utilization of the EPC2014C gallium nitride (GaN) transistor into the half-bridge submodules of the M2C. These submodules are configured in series and parallel, with a switching frequency of 24 kHz, to achieve the voltage and current requirements. Each arm

of the M2C was designed onto a double-sided, 6-layer, printed circuit board (PCB). The design and fabrications for these power boards are discussed as well.

The design, fabrication, and analysis of all three power conversion circuits presented here also include similar analysis for their gate drive circuits.

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PREFACE

The author would like to thank and acknowledge the following people for their support in the completion of this project: Dr. William Stanchina, Professor in the ECE department of the University of Pittsburgh for his unwavering support, constant advisement, and overall mentorship. Steven Mankevich, Dr. Philip Stone, and Dr. Kathleen Lentijo of Converteam Naval Systems, for the introduction to wide bandgap, power semiconductor devices, and sparking the curiosity to investigate their properties in power conversion systems.

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Finally, the author would like to thank his friends, family, and God.

1.0 INTRODUCTION

Power electronic systems have been dominated by silicon based devices, primarily the Insulated Gate Bipolar Transistor (IGBT), which was invented over thirty years ago [1, 2], and the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The power semiconductor industry is advancing transistor technology such that modern transistors are capable to switch faster, have a higher power rating, possess decreased switching losses, and greater thermal operating capabilities [3-5]. These improvements are achieved through the integration of wide bandgap (WBG) semiconductor materials (e.g. Silicon Carbide (SiC), Gallium Nitride (GaN), etc.) [2]. Research has been ongoing for many years on SiC MOSFETs to be used in applications where traditional silicon IGBTs or MOSFETS were used. SiC MOSFET devices have been introduced in the past ten years by companies such as Infineon and Cree [2, 6, 7] but their ratings are only now approaching comparable ratings (1kW- 10kW) with traditional Silicon IGBTs.

With the onset of newer devices and systems, simulation tools are utilized to decrease the design and troubleshooting time of a project. The work presented through this thesis includes the characterization of various wide bandgap, power, semiconductor transistors and their integration and performance in power electronic systems.

First, a comparative study of the electrical efficiency and thermal performance is conducted between a 1200 Volt, 100 Amp Powerex SiC MOSFET (QJD1210SA1) [8], and a 1200 Volt, 100 Amp Powerex Silicon IGBT (CM100TX-24S1) [9], in a dc/dc boost converter circuit [3, 10,

11]. For each device, the objective was to identify a desired operating switching frequency range to achieve high efficiency, while abiding to thermal constraints. Detailed behavioral models of the Powerex devices were constructed in Synopsys SaberRD and simulated within the dc converter topology to predict the electrical efficiency. These models include details provided from manufacture datasheets, to enhance the simulations with additional system intricacies.

The transistor's gate drive circuitry was specifically designed to ensure similar operating conditions for both the SiC MOSFET and Si IGBT. This design was analyzed using ANSYS Icepak to simulate the thermal performance of the designed gate driver printed circuit board. This analysis was to ensure the gate drive circuitry would not cause failure within the dc converter. The gate drive printed circuit board (PCB) was incorporated into a physical test-bed which was constructed to experimentally measure the effects of switching frequency on electrical efficiency and transistor operating temperature. The simulated results are compared against experimentally collected data in order to validate our models and their efficacy.

In addition, a mathematical model predicting the SiC MOSFET operating junction temperature with respect to switching frequency was evaluated. With increased integration of SiC MOSFETs over Si IGBTs, it is important to design power electronic systems such that the transistors operate in safe conditions. This methodology sweeps the operating frequency of the transistor device, while maintaining other system specific parameters constant, to predict the change in junction temperature from the ambient temperature. Based on the benchmarking here, this appears to be an important and beneficial design tool for future power conversion circuits using wide bandgap semiconductor devices.

The techniques used to integrate the SiC MOSFET into the dc/dc boost converter were then extrapolated to interface GaN high electron mobility transistors (HEMTs) into a modular

multilevel converter (M2C) topology. The objective of this project was to adapt a traditional M2C topology to utilize GaN HEMT devices, in order to significantly minimize size, and increase the power density of a single phase, dc/ac inverter. Similar gate driver techniques to those in the dc/dc converters were employed to ensure the transistor devices operated under safe conditions. Similar techniques analyzing the thermal stresses of the gate drive system were used within ANSYS Icepak. These losses were predicted and compared to experimental results. These results were also used to validate the M2C submodule design with GaN HEMTs. The work designing and testing the M2C submodules and power module, presented herein, was done as part of a larger project to create a power dense M2C converter. The team's work in finalizing the design and testing is ongoing; the design, preliminary experimentation, and analysis of the submodules and developed M2C power boards are discussed in Chapters 8.0 through 10.0 .

2.0 PROPERTIES OF SEMICONDUCTOR MATERIALS

2.1 WIDE BANDGAP AND SILICON PROPERTIES

The integration of wide band gap materials into power semiconductor devices is a necessary step to progress the power electronics systems to be lighter, smaller, and more reliable. SiC and GaN devices have most notable advantages in electrical breakdown field, thermal conductivity, electron saturation drive velocity, and irradiation tolerance [2, 3, 6, 7, 11-13]. Stevanovic in [2] indicates that the increase in critical electric field strength from utilizing SiC (or GaN), will decrease the size of insulating (or blocking) layers within transistor devices. The decrease of blocking layer size, in conjunction to higher doping concentrations, will also result in lower ON-resistance values in comparison to silicon devices [2]. Current research initiatives in the fabrication of SiC devices, are predicting that future devices will be 10x thinner, resulting in much greater power-dense devices [3, 5, 14, 15]. This will help meet the industrial trends desiring new systems to be smaller, lighter, and more robust. For example, any reduction in volume and weight of power electronic systems in hybrid electric vehicles (HEVs), photovoltaic inverters, or motor drive systems can improve the overall performance of the system [4]. In addition, devices capable of sustaining higher operating temperatures (SiC can on average maintain a 25°C higher operating temperature [6, 16]) are highly attractive for the previously

listed applications [12]. Superiorities in the thermal conductivity, electrical breakdown field and drift velocity are also very important in high power motor drive systems [6].

Gallium nitride (GaN), another of these wide bandgap semiconductors, offers a number of enhanced properties over silicon and is being integrated into various technological fields including high-power microwave devices, and power electronic applications. The major advantages that these materials can provide include higher breakdown fields, higher operational junction temperatures, and higher electron mobility [11, 17, 18]. While GaN does not offer better thermal conductivity, like silicon carbide (SiC), the other properties offer much better performance when fabricated into a high electron mobility transistor (HEMT), described in Section 2.2.

As the semiconductor fabrication technology continues to advance, the cost of production will decrease to allow more industries and applications for SiC and GaN devices. Cost of production and fabrication are leading issues with the integration of WBG devices in industrial applications. Only recently have devices that are cost competitive to Si counterparts have been introduced, and so only industrial applications where performance is prioritized over cost are WBG devices currently utilized.

2.2 IMPORTANT DEVICE CHARACTERISTICS

Power MOSFET and IGBT devices have distinct functions within the power electronic industry. MOSFETS have predominately been used in systems with relatively low voltage (< 10 kV) and high switching frequencies, while IGBTs are utilized in systems with higher voltages (> 10 kV) [5]. The MOSFET device configuration includes high input impedance, low ON-resistance,

physical ruggedness, and high switching speed capabilities [5]. Creating MOSFETs with silicon carbide instead of silicon changes many device parameters including breakdown voltage, thermal conductivity, electron mobility and more [11]. Both material and device characteristics influence the size, and ratings of passive components (capacitors and inductors) within a converter topology. These enhanced qualities enable MOSFETs to be used in applications where Si IGBTs have traditionally excelled (ex: medium voltage motor drivers, power converters, etc.) [1, 6].

IGBTs were first introduced in 1982 and consist of a "wide-base pnp transistor driven by an integrated short channel MOSFET" [5]. This configuration produces a high power gain because of the high input impedance. The switching speed can be adjusted by lifetime control processes. These characteristics allow the IGBT to be suitable for primarily medium and high-power applications [5].

The IGBT topology is built upon MOSFET and bipolar junction transistor (BJT) technology to include behaviors from both devices [19]. The additional p-n junction between the MOSFET and BJT is to inject high levels of excess minority carriers reducing the ON-state resistance and conductivity modulation [19]. The BJT is generally designed with low excess carrier lifetime in the base for faster turn-off [19]. One issue within the IGBT device overall, arises that the carriers (holes and electrons) must be vacant before the device can be turned on. This results in reverse recovery effects and losses [3]. IGBTs also have slower electron mobility through the conducting channel which limits their ability to operate at higher frequencies. This can increase the passive component ratings, and physical size [5, 15, 20].

The final device discussed and utilized throughout this work is the GaN high electron mobility transistor (HEMT). HEMT devices have traditionally been used in RF and amplifier applications, however, current research is enabling GaN HEMTs to replace low voltage (< 600 V) Si

MOSFETs in power electronic circuits [21, 22]. Transistors for use in power conversion technologies need to have three of four key qualities to be competitive: efficient, reliable, controllable, and cost effective [23]. GaN HEMTs provide very efficient, reliable, and controllable devices. Only now however, as GaN HEMT devices are grown on a silicon substrate will the devices be more cost effective and competitive in fields such as broadband wireless networks, HEVs, electric grid controllers, radar systems, etc [21, 24]. While GaN devices offer the highest power density per volume, fabrication techniques have not enabled for a device over 650 Volts. This is due to the difficulty of fabricating GaN substrate layers vertically; a necessary condition to reach over 1200 Volts. While GaN hosts many advantages over SiC and Si, this limits the device into low voltage applications allowing for SiC MOSFETs to enter the medium voltage (1.2kV – 10kV) market. Only continued advances in manufacturing and fabrication techniques will enable any device from overcoming the traditional Si in power electronic systems.

3.0 SYNOPSYS SABER DEVICE MODEL

Researchers identify many techniques to model transistors including “mathematical”, “semimathematical”, “behavioral”, and “numerical” [1]. A brief review was conducted to identify the best form of device modeling for the selected Si IGBT and SiC MOSFET. The purely, mathematical technique will not be used because it simulates each variable (resistance, capacitance, inductance) independently in a detailed, dynamic model. It also includes equations for the wide-base PNP section, current in the space charge layer, the MOS channel section, dynamic carrier behavior and dynamic electro-thermal effects [2]. This technique is valuable in observing transient effects from the specific device parameters, but not as effective at modeling long-term device operation within a power electronic system [1, 15, 16].

The *seminumerical* technique uses “finite element methods to model the wide base while the other device parts are modeled by earlier analytical methods” [1]. Hefner, in [25], offers examples of extrapolating necessary data that can be used for characterizing device physics models. Studies from [3, 15, 16, 25, 26] indicate device parameters such as channel modulation, and turn-ON/turn-OFF losses are critical for accurate device models. These parameters are both applicable for an IGBT and MOSFET device model.

A hybrid technique incorporating the *semimathematical* and *behavioral* techniques would best benefit this work’s modeling needs. These models can be created in Synopsys SaberRD. SaberRD is a physics based simulation platform that offers engineers capabilities to model, and

simulate power electronic systems. In addition, SaberRD offers a more detailed platform by incorporating transistor device models. Behavioral models which emulate the current-voltage, voltage-capacitance, and gate-charge properties are developed in SaberRD and detailed in Sections 2.1 and 2.2. Some parameters extrapolated from semiconductor device theory, a semi-mathematical approach, in addition to parameters expressed in manufacturer datasheets, behavior technique, are also incorporated into SaberRD models [1, 2]. Models were created for a Powerex 1200 Volt, 100 Amp SiC MOSFET (QJD1210SA1) [8] and a Powerex 1200 Volt, 100 Amp Silicon IGBT (CM100TX-24S1) [9].

3.1 MOSFET DEVICE MODEL

The Power MOSFET Tool was first used to develop the SiC MOSFET model. The tool creates a high fidelity, level-1 model with optimized parameters [27]. The tool is most widely used in studying switching transients and losses in power electronic systems. As seen in Figure 1, the model incorporates DC, capacitance, gate charge, and internal diode device characteristics. Primary values important in modeling MOSFETs, in addition to those incorporated in SaberRD are depicted in Table 1 [2, 4, 6, 12, 20].

The ranges of parameter values were identified from the manufacture datasheets and entered as preliminary results. The “scanned utility tool” was then utilized to alter these initial parameters to match the imported I-V output, turn on, and capacitance curves [16, 25]. This technique imports an image from the datasheet of the desired graphs- IV curve, Capacitance, Resistance, etc. such that a replica trace is manually entered into the program.

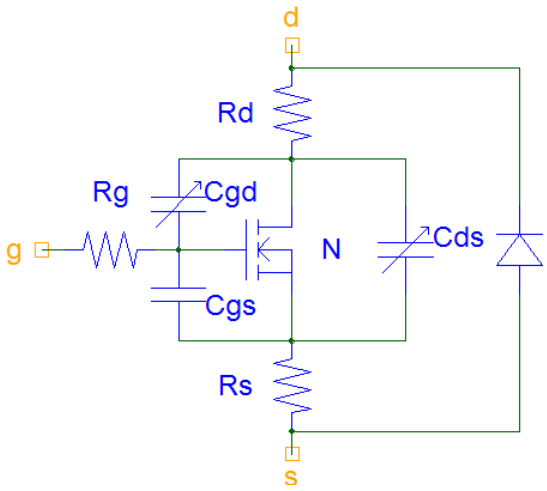


Figure 1: MOSFET Tool parameters from Saber

Each variable/component is characterized from data provided by the transistor manufacturer in their product datasheets. The exact datasheet curve can be seen in association with the modeled MOSFET tool parameters in Figure 2 and Figure 3.

Table 1: SaberRD Power MOSFET tool device parameters

Gate Threshold Voltage (V_{GS})
Drain-Source Voltage (V_{DS})
Drain Current (I_D)
Junction Temperature (T_j)
Drain-Source On Resistance (R_{DS})
Input Capacitance (C_{iss})
Output Capacitance (C_{oss})
Reverse Transfer Capacitance (C_{rss})

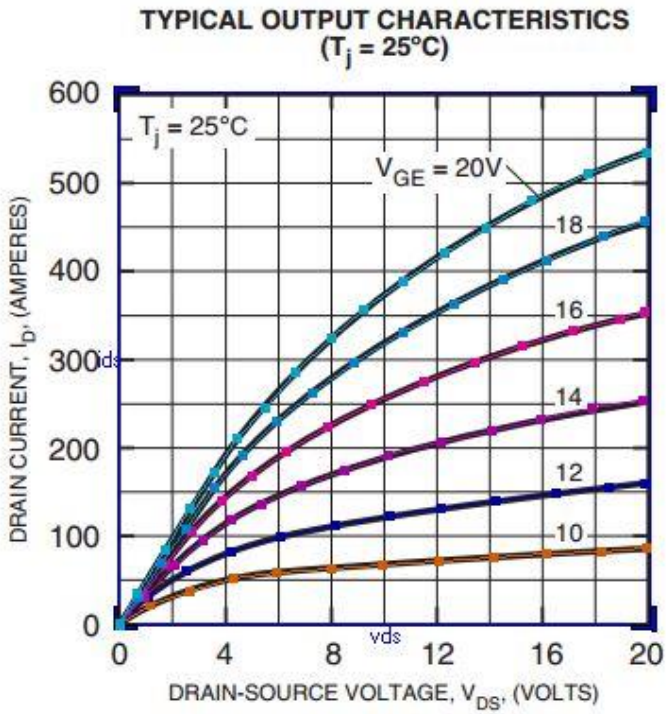


Figure 2: Imported MOSFET I-V Output Characteristic [8]

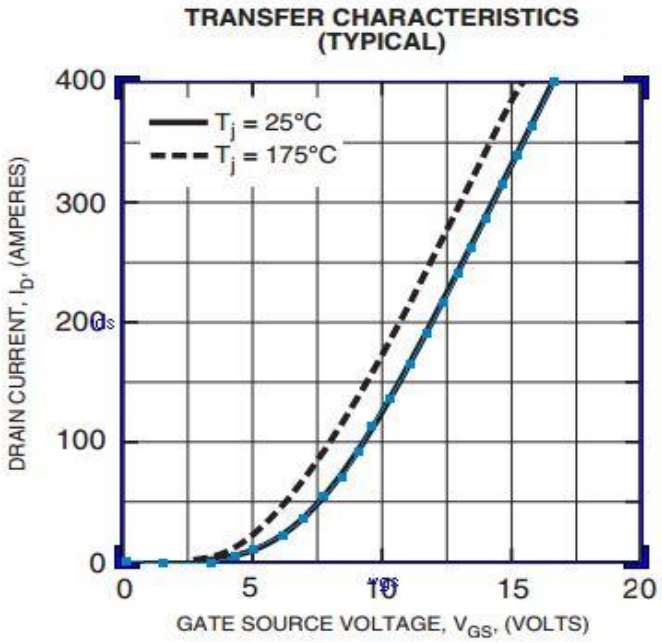


Figure 3: Imported MOSFET Turn--On Characteristic [8]

These traced curves are added to the DC Characteristics graphical interface (Figure 4) that shows the SaberRD model parameters. The optimization tool was then used to alter device parameters to match the imported/traced curve to the model. One such parameter, specifically Lambda, was found to be out of the bounds of physical relationships. Lambda is the channel-length modulation which is caused by an increasing drain-source voltage [28]. The lambda value was manipulated such that a realistic value would be represented, and a close match to the models would still be held [4, 16, 20]. Figure 4 through Figure 6 show the finalized results between the utility tool, and the SaberRD MOSFET model. It can be seen that in some figures, specifically Figure 6, there are discrepancies between the datasheet and device curves. The capacitance characteristics of the model do not support the level of detail necessary to approximate the curve to a higher degree. It is understood that the capacitance will dynamically change switching between ON-OFF states, through the inaccurate region (< 200V), however, it should be noted that the overall operating condition for the device is in the linear region of V_{DS} (> 200 V).

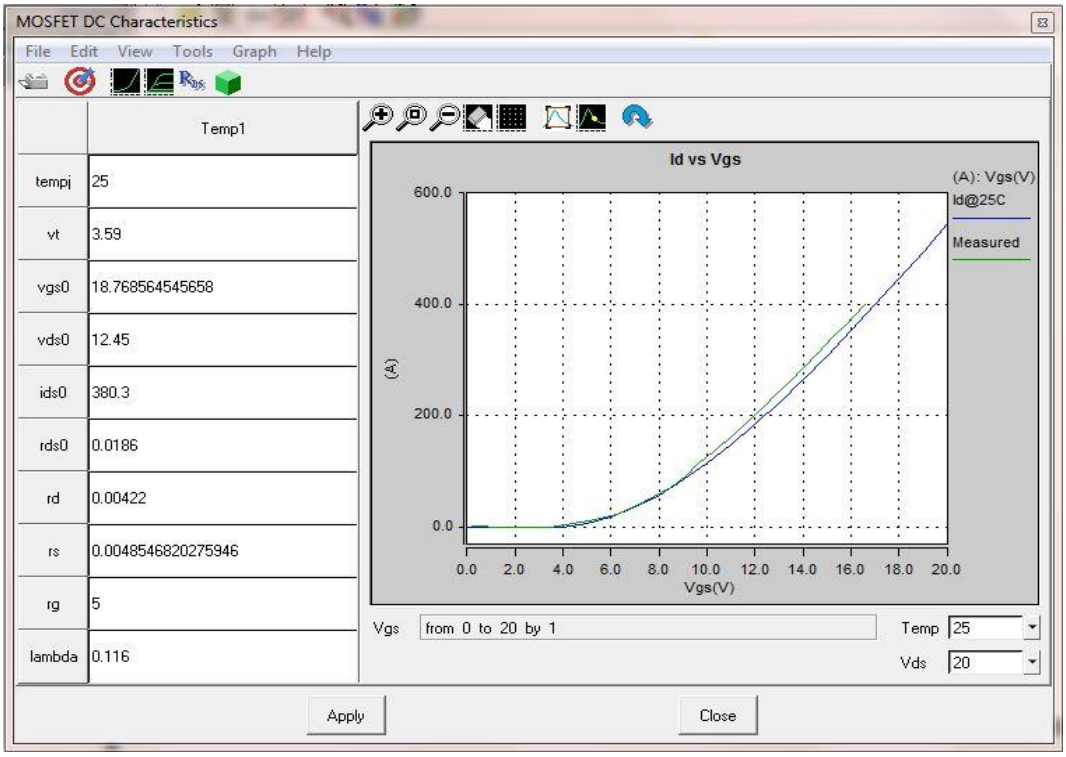


Figure 4: MOSFET DC Characteristics

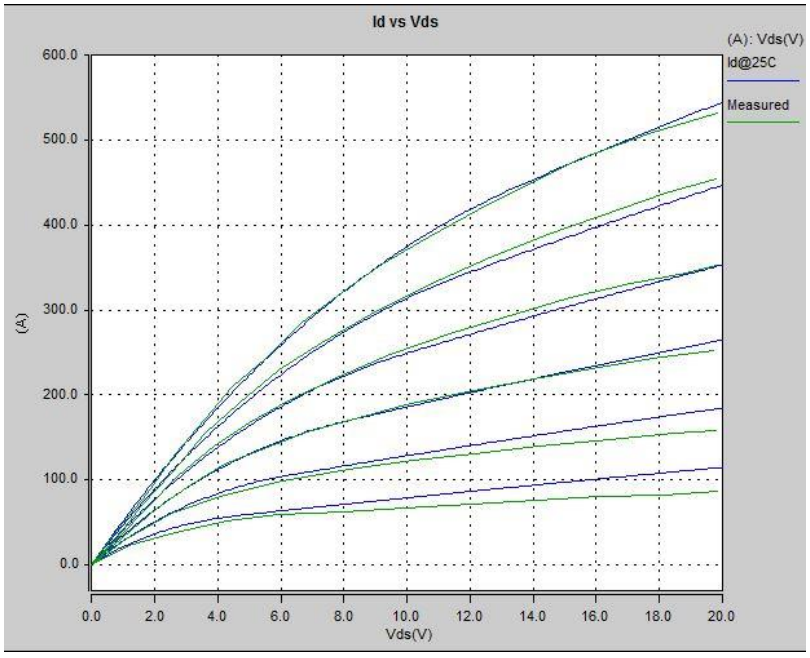


Figure 5: MOSFET Id v. Vds

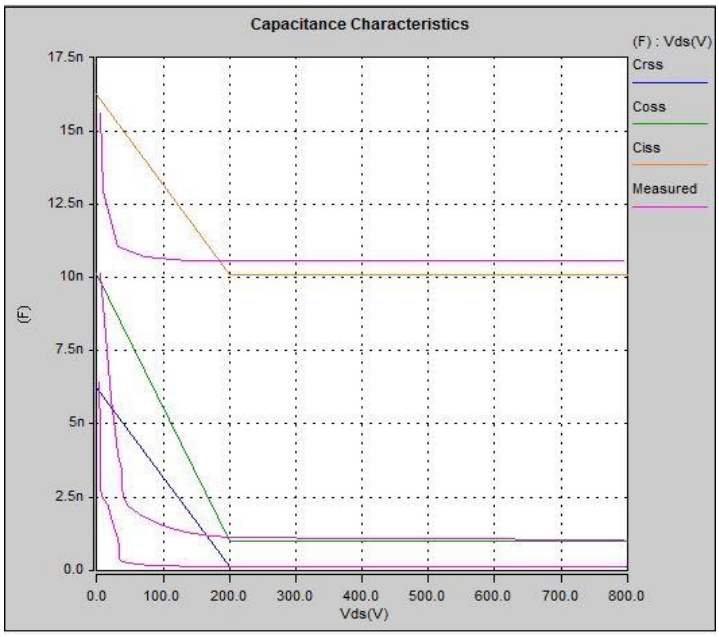


Figure 6: MOSFET Capacitance

While SaberRD has capabilities for Dynamic Thermal Modeling, the datasheets did not provide necessary detail to be added to the created models. In addition, the dynamic models include “thermal pin connections” [27] which allow for a resistive and capacitive network to be added emulating thermal transfer paths connected to the devices. This would include thermal pastes, heatsinks, and other thermal management systems. All data imported to the model was rated for 25 degrees Celsius.

Overall, the output characteristics were found to be very similar to those in the given data sheets from Powerex. One concern while creating this model specifically, was how the model handles a SiC device. While many parameters are device rating specific (drain-source voltage, capacitance, resistance), there were few parameters that emanated from the device’s material properties in the model. And so thermal conductivity, electron mobility, critical field strength and other parameters that offer benefits to use SiC, were ignored and did not provide enough

detail to accurately model the device using SaberRD. These benefits for this device did show themselves in experimental testing [2, 10, 11, 15, 29].

3.2 IGBT DEVICE MODEL

In comparison, the IGBT tool in SaberRD is more developed and includes additional parameters and customization. These models are capable of predicting the device behavior, including switching speeds and losses over the operating temperature range, and include characterizations of the internal diode and thermal impedance [27]. Similar parameters to the MOSFET were found to be key in modeling IGBTs and are expressed in Table 2 [1, 6, 25, 26, 30, 31]. The same overall technique used for modeling the MOSFET was used for the IGBT. Preliminary datasheet information was recorded, followed by the tracing of datasheet specific curves. Because the IGBT is a generally more complex device with additional internal semiconductor layers, additional details were added to the model to include specifically the tail current of the device. Figure 7 shows the general SaberRD model that was used to match I-V, turn on, gate charge and capacitance curves, as seen in Figure 8 through Figure 11.

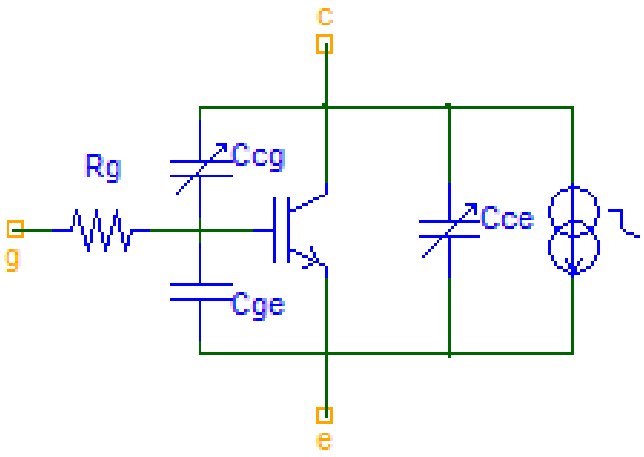


Figure 7: Saber IGBT model parameters

Table 2: Important IGBT Model parameters

Junction Temperature (Tj)
Collector Current (I_C)
Collector-Cuttoff Current (I_{CES})
Gate Leakage Current (I_{GES})
Gate-Emitter Threshold Voltage ($V_{GE(th)}$)
Collector-Emitter Saturation Voltage ($V_{CE(sat)}$)

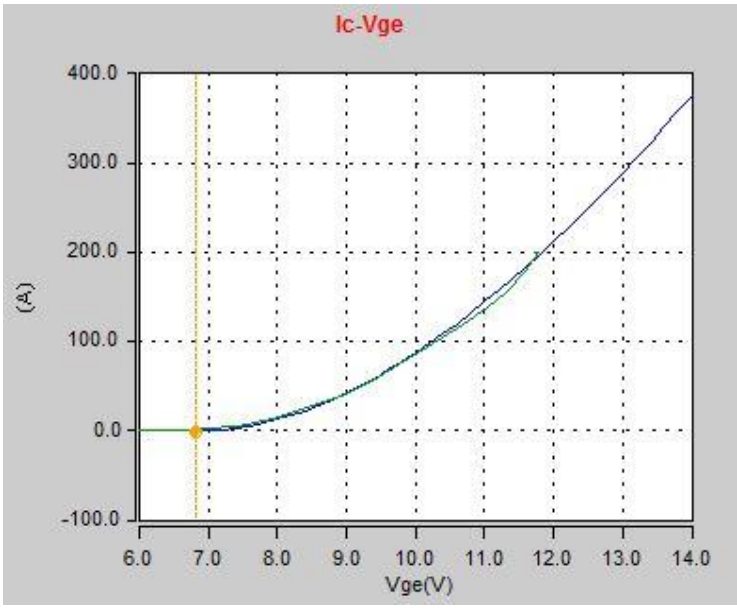


Figure 8: IGBT Ic v. Vge

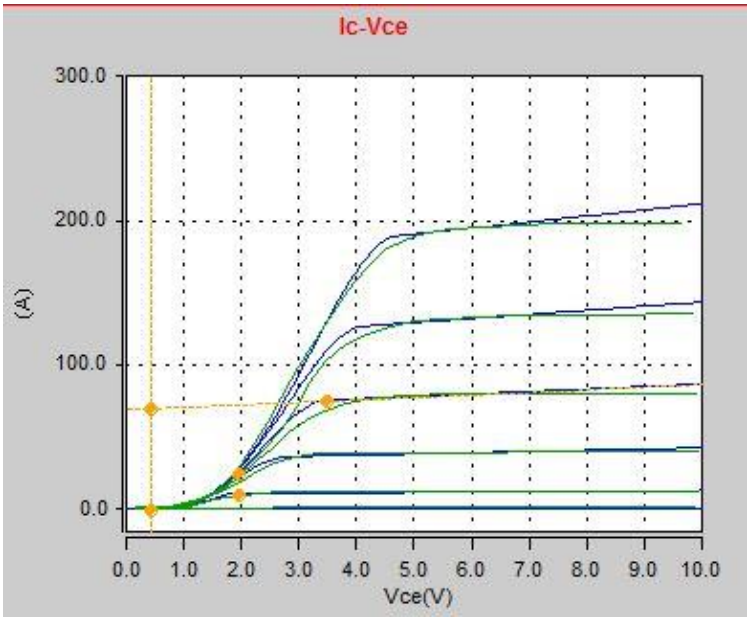


Figure 9: IGBT Ic v. Vce

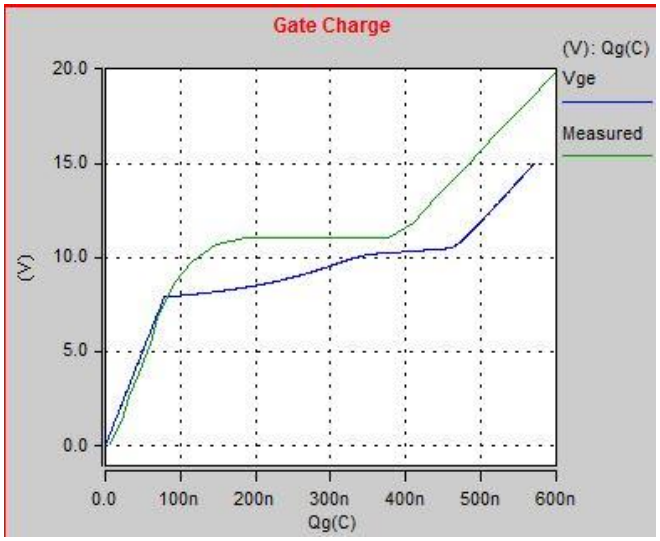


Figure 10: IGBT Gate Charge

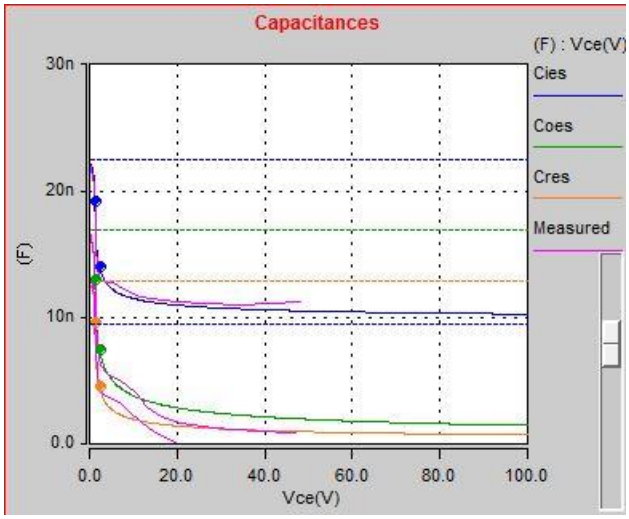


Figure 11: IGBT Capacitance

While the designed device characteristics are indeed similar to the traced datasheet curves, the confidence in this model is much greater than that of the MOSFET because the IGBT device is a silicon based device. Similarly to the MOSFET tool, no material property specific details were incorporated, however, silicon has been the traditional material for power transistor devices and other transistors in commercial models, increasing the accuracy of the model.

4.0 DC/DC CONVERTER CIRCUIT DESIGN

A dc/dc boost converter was chosen as the converter topology to validate the Synopsys SaberRD device circuit model because of its relatively simple design, and its presence in numerous applications like hybrid electric vehicles (HEVs), battery regulatory systems, and more [32-34]. The boost converter also allows distinct isolation of the switching transistor, which is critical for analyzing the switching frequency based thermal and electrical effects. This chapter will discuss the fundamentals of a dc/dc boost converter, how the specific converter components were chosen for our test circuit, the results of Synopsys SaberRD simulations of the converter, and the associated gate drive circuit design.

4.1 DC/DC CONVERTER DESIGN

DC/DC boost converters are simple switched-mode converters that are capable of amplifying an input dc voltage to a higher dc output voltage [35-37]. Depending on the desired rating of the converter, IGBT and MOSFET devices are commonly utilized. The relative simplicity of the circuit offers a unique opportunity to observe the thermal and electrical effects on the switching transistor. Converter parameter values were identified to match with current industry standards such that an appropriate, and applicable system could be studied [3, 32, 36, 37].

Table 3: DC/DC Boost Converter Design Parameters

Parameter	Numerical Quantity
Input Voltage, V_{in}	220 V (max)
Output Voltage, V_{out}	440 V (max)
Input Current, I_{in}	8 Amp (max)
Output Current, I_{out}	4 Amp (max)
Duty Cycle, D	50%
Frequency, f_s	1000 Hz – 25000 Hz
Load Resistor, R	103 Ω

Table 3 lists the parameters that were used in the preliminary design of the dc/dc boost converter. Using known equations for the boost converter [35, 38], the other system components were derived. These components are to ensure that the system operates in the continuous conduction mode (CCM). CCM suggests the system current never becomes negative between switching cycles and that the average current is greater than the change in current, expressed in eq. 4.0 -1. The inductor value was determined such that a change in current (Δi) would be contained within a manageable limit.

$$\Delta i < I_{DC} \tag{4.0 -1}$$

$$\Delta i = \frac{T_S D V_{in}}{2L} \tag{4.0 -2}$$

$$I_{DC} = \frac{V_{in}}{D'^2 R} \tag{4.0 -3}$$

$$I_{DC} > \frac{T_S D V_{in}}{2L} \tag{4.0 -4}$$

$$L > \frac{T_S D V_{in}}{\left(\frac{V_{in}}{D'^2 R}\right)} \tag{4.0 -5}$$

Table 4: Design variables to determine inductance

Variable	Value
$V_{in(max)}$	250 Volts
D=D'	.5
$f_s = 1/T_s$	1000 Hz
R	103 Ω

$$L > 0.0125\,H$$

$$\Delta i = \frac{DV_{in}}{2 f_s L} = 4\,Amps \qquad (4.0\text{ -}6)$$

Using the known CCM design considerations, with the variables listed in Table 4, a minimum inductance of 12.5 mH was determined. The necessary parameters to calculate the inductor value include the converter duty cycle (D), i.e. the percentage of the switching period during which time the transistor will be "ON", and the period of the switching event (T_s). This minimum inductor value was used to determine a resulting change in current, where it was found that a 4 Amp swing (50% of the average current value) would be created. As such, a larger inductor value was necessary to limit the current peaks and a 30 mH inductor was selected such that the resulting $\Delta i = 1.67 Amps$ in worst case scenarios. This would add 0.83 *Amps* to the steady state current for a maximum current rating at 1 kHz. As the switching frequency increased, this change in current would be decreased significantly.

A similar technique was used to determine the necessary system output capacitance. The mathematical derivation and assumptions are explained in equation 4.0 -7 through 4.0 -9. In this instance, a preliminary ΔV was decided to be 2.5% of the output voltage.

$$\Delta V = 0.025 V_{out}$$
$$\Delta V = 10 Volts$$

$$C_{out(\min)} = \frac{I_{out(\max)} D}{f_s \Delta V} \qquad (4.0\text{ -}7)$$

$$I_{out(\max)} = \frac{V_{out}}{R} \qquad (4.0\text{ -}8)$$

$$C_{out(\min)} = \frac{V_{out} D}{R f_s \Delta V} \qquad (4.0\text{ -}9)$$

$$C_{out(\min)} = 214\,\mu F$$

Similarly to the derivation of the inductance, a switching frequency of 1000 Hz was used for the capacitor value. 1000 Hz is the selected lower limit of the tested switching frequencies and was used for both derivations because it provides the lowest denominator in each set of equations. This indicates that for any higher switching frequencies the minimum value for inductance and capacitance would be lower, and so the chosen values satisfy the Δi and ΔV conditions for the complete range of switching frequency.

4.2 SYNOPSYS SABER CONVERTER SIMULATIONS

A DC/DC boost converter system was constructed in Synopsys SaberRD to simulate the electrical efficiency. Simulations for each of these transistor types were conducted with an input current source of 3, 5, 7 and 8 Amps, and switching frequencies ranging from 1 kHz to 25 kHz, to ultimately predict system efficiency. Figure 12 displays the designed converter parameters with the IGBT model in SaberRD. The converter parameters were chosen in accordance with Section 4.1, and to represent similarities with the physically constructed converter described in Chapter 5.0 .

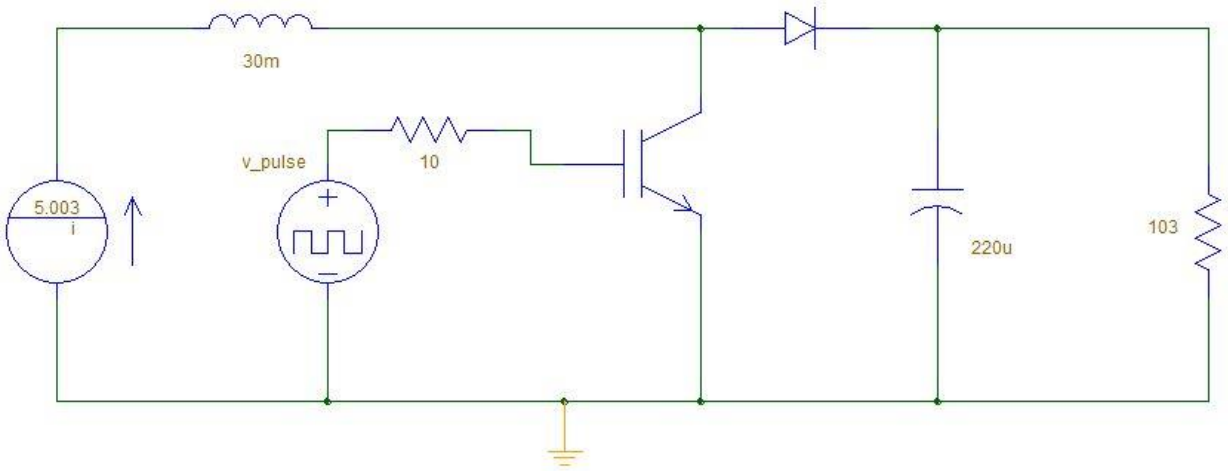


Figure 12: SaberRD simulated DC/DC boost converter

This converter design does not incorporate additional parasitic inductance and resistances that are added through the physical wiring. In addition, the gate drive circuitry is modeled through a single square wave pulse generator. The upper and lower limits of the gate voltage are consistent with those discussed in Section 4.3. Table 5 and Table 6 show the simulated electrical efficiency values for the SiC MOSFET and Si IGBT converters. These efficiencies were mathematically calculated from input and output powers measured within SaberRD. The input power was measured from the current source, while the output power was measured from the load resistor. Because additional loss parameters were not included in the SaberRD simulation, it is theorized that the simulated results are of a higher percent efficiency than a physical converter would operate. Self-heating effects, and parasitic inductance and resistance through wiring and device packaging are dynamic factors that could decrease the overall system electrical efficiency.

Table 5: Simulated DC/DC boost converter (SiC MOSFET) electrical efficiency

Switching Frequency (Hz)	% Electrical Efficiency (3 Amps)	% Electrical Efficiency (5 Amps)	% Electrical Efficiency (7 Amps)	% Electrical Efficiency (8 Amps)
1000	98.44	98.65	98.77	98.80
4000	97.68	97.88	98.01	97.96
7000	97.03	97.27	97.91	97.71
10000	96.54	96.89	97.71	97.34
13000	96.87	96.75	97.42	97.08
16000	95.79	96.37	96.32	96.57
19000	95.54	96.14	96.21	96.34
25000	94.39	95.10	95.72	95.83

Table 6: Simulated DC/DC boost converter (Si IGBT) electrical efficiency

Switching Frequency (Hz)	% Electrical Efficiency (3 Amps)	% Electrical Efficiency (5 Amps)	% Electrical Efficiency (7 Amps)	% Electrical Efficiency (8 Amps)
1000	98.10	98.52	98.69	98.71
4000	97.93	98.28	98.23	98.24
7000	97.79	98.06	97.92	97.95
10000	97.67	97.91	97.70	97.62
13000	97.54	97.75	97.36	97.40
16000	97.42	97.55	97.12	97.17
19000	97.29	97.37	96.94	96.77
25000	97.04	96.93	96.39	96.23

4.3 GATE DRIVE DESIGN

Gate drive circuitry is the cornerstone of the transistor operation. If the gate drive circuit does not provide necessary charge and power to the transistor it will not transition between switching states properly. It was found through [39], that both the Si IGBT and the SiC MOSFET could be operated from the same generic gate drive circuitry, seen in Figure 13.

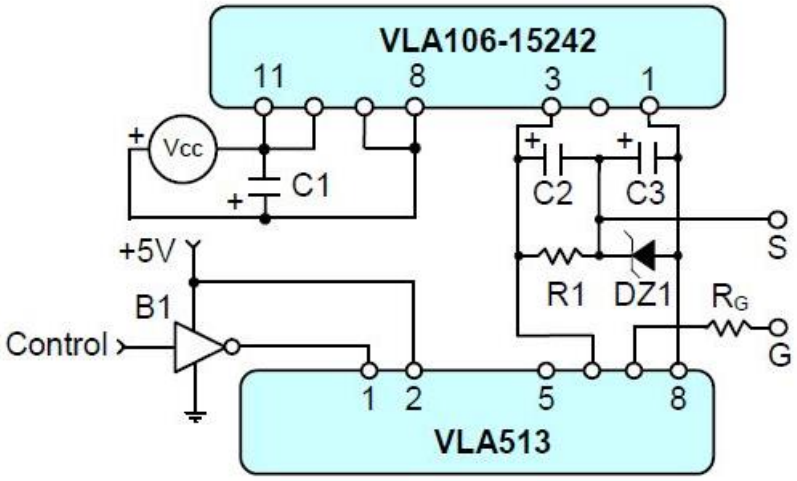


Figure 13: Proposed Gate Drive Circuitry [39]

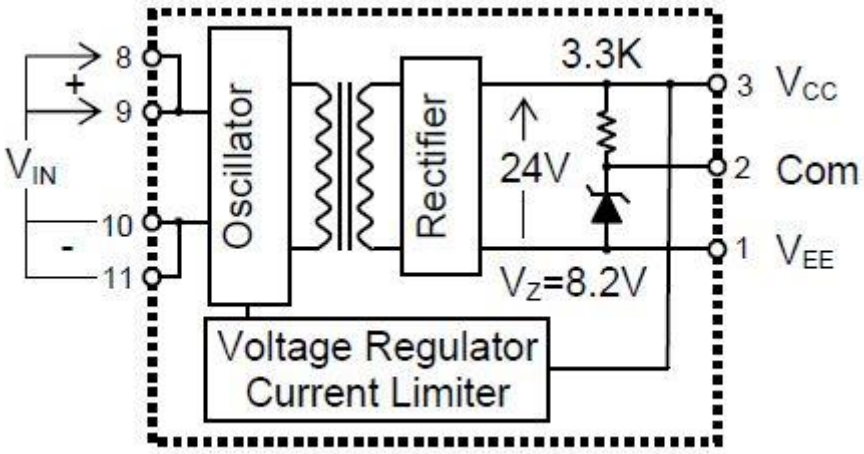


Figure 14: VLA106-15242 circuit diagram [39]

This circuitry provides both power and signal isolation to the transistors. Although this level of isolation is not necessary for a dc/dc boost converter application, it provided a basis for the gate drive design of a very different type of converter that will be presented in Chapter 7.0 . From Figure 13, two Powerex chips were used to provide both the power and signal isolation [39]. The VLA106-15242 is an isolated dc/dc converter (Figure 14), that provides a clean 24 Volt potential between pins 1 and 3. This potential is moderated through capacitors C2 and C3, and the maximum and negative voltages of the 24 volt swing are determined by R1 and the Zener diode (DZ1). The VLA513 (Figure 15) includes an isolated signal that will oscillate between the positive and negative potentials created by the VLA106 chip [39]. The primary sources of isolation are derived from both the oscillator/rectifier and opto-coupler circuits. A 5 Vpp square wave with a 50% duty cycle, and 2.5 V DC offset was generated from an external function generator, and used as the control input for the VLA513 circuit, as well as the basis for the converter switching waveform.

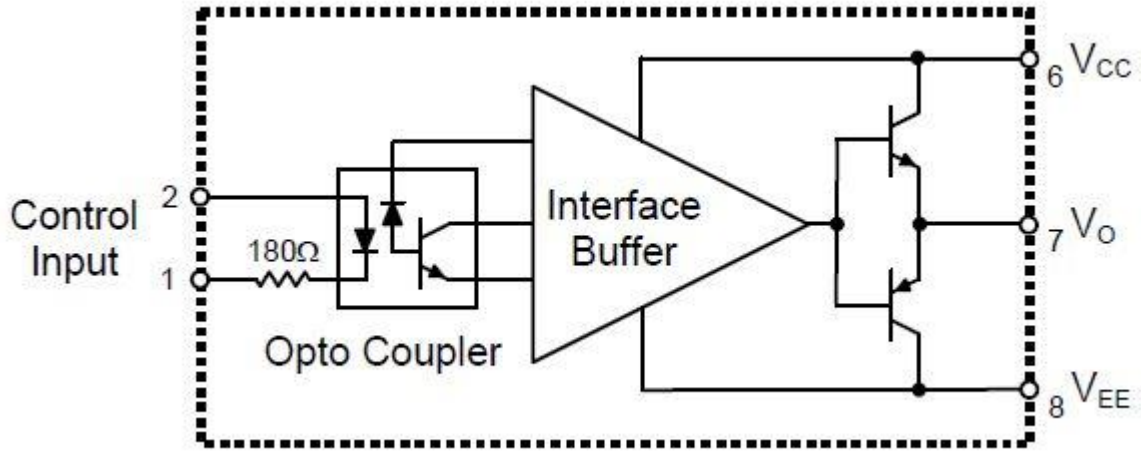


Figure 15: VLA513 Circuit Diagram [39]

The control signal is used to switch between the high and low potentials between R1 and DZ1, which creates the high and low potential signals that are sent between the transistor gate and source. To ensure direct comparisons of the transistor performance, the gate drive circuitry was kept identical except for the Zener diode (DZ1) as seen in Figure 13. With the 24 Volt potential output of the circuit, this Zener diode provides a negative clamp that limits the positive swing of the signal. For the SiC MOSFET, it is recommended to operate the device with a positive potential of 20.1 Volts, and so a -3.9 Volt Zener diode was selected [8]. Whereas, the IGBT requires a lower positive potential (15 Volts), but requires a lower negative potential because of the devices inherent tail current [26, 31, 40]. As such, the IGBT driver provides a +15, -7.9 Volt swing [9]. Table 7 shows the additional components and values used to complete the gate drive circuit.

Table 7: DC Converter Transistor Driver Components

Driver Component	Value	Selected Component
Driver Chip	N/A	Powerex: VLA513-01
Isolated DC/DC Converter	N/A	Powerex: VLA106-15242
C1, C2, C3	40 μF	UKL1H470KPDANA
R1	3.3 kΩ	ERA-6AEB332V
DZ1 (MOSFET)	3.9V, 1 W	DZ2W03900L
DZ1 (IGBT)	8.2V, 1 W	DZ2W08200L
Rg	10 Ω	TEH100M10R0JE
B1	Sink 16 mA	TC7S04F,LF

To provide 5 Volts for the VLA513, a 5 Volt regulator chip was added to the circuit such that only an external 15 Volt input would be required to operate the entire gate driver circuit. The gate drive circuit was designed onto a printed circuit board that also incorporates other aspects of the converter including the system diode, and output capacitors. The left half of Figure 16 shows the designed printed circuit board; the output capacitor, diode, and resistive load can be seen on the right half of the designed board. The PCB was designed as a two-layer, lead free board in

ExpressPCB. The trace width calculations were conducted to ensure trace current handling capabilities [41]. The core of the current traverses through cabling and not the PCB, so this calculation was not as critical as that in Section 10.1. The entire board is 4” x 5” (l x w), and has pin and screw terminals to connect the other converter components. The board was fabricated by ExpressPCB and manually populated. Both the fabricated and populated boards can be seen in Figure 17 and Figure 18.

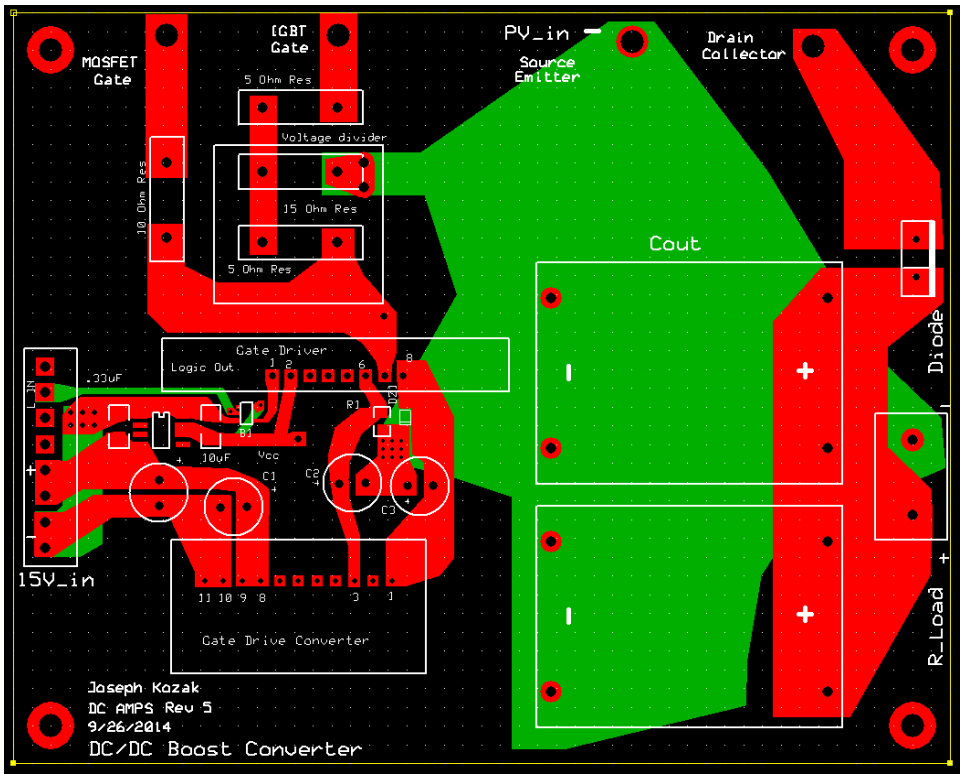


Figure 16: DC/DC Boost Converter Gate Driver and system PCB

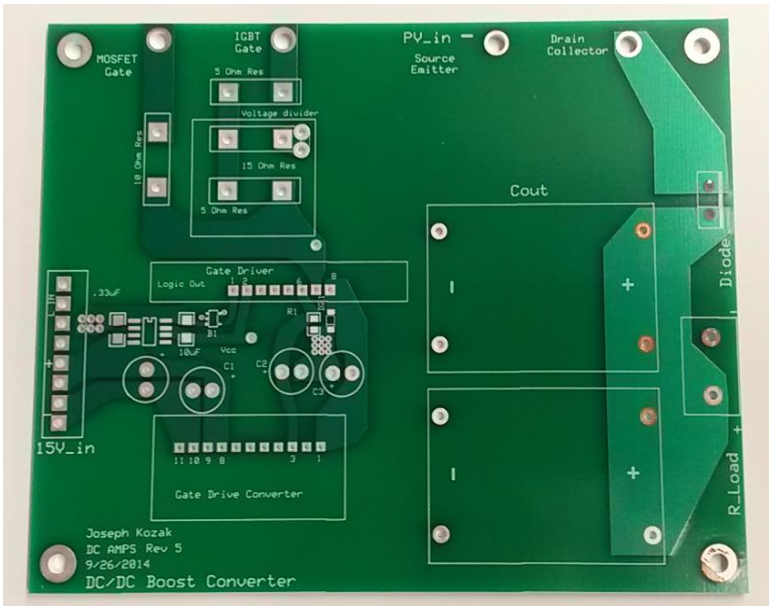


Figure 17: Fabricated DC/DC Boost Converter Gate PCB

Figure 18: Populated DC/DC Boost Converter Gate PCB

Tests to validate the circuit design were conducted, and the waveforms for both the MOSFET and IGBT systems are shown in Figure 19 and Figure 20. Both waveforms show a strong relationship with the desired values. Voltage divider prongs were used with a division of x2 such

that the recorded voltage is half the actual voltage seen by the probes. The cursors in Figure 19 show that the maximum and minimum are 9.52 Volts and -1.92 Volts respectively which translates to approximately 19 Volts and -3.8 Volts seen at the terminals. The same analysis can be made for the IGBT driver, where the measured output voltage ranges from 14.6 Volts and -8 Volts (Figure 20). With a desired of 20.1 and -3.9 Volts for the MOSFET, and 15 and -7.9 Volts for the IGBT, the small voltage discrepancies can be accounted for through the inefficiency of the isolating dc/dc converter, as well as losses through other surface mount components. A thermal analysis of the gate drive circuitry is discussed in Section 5.1.

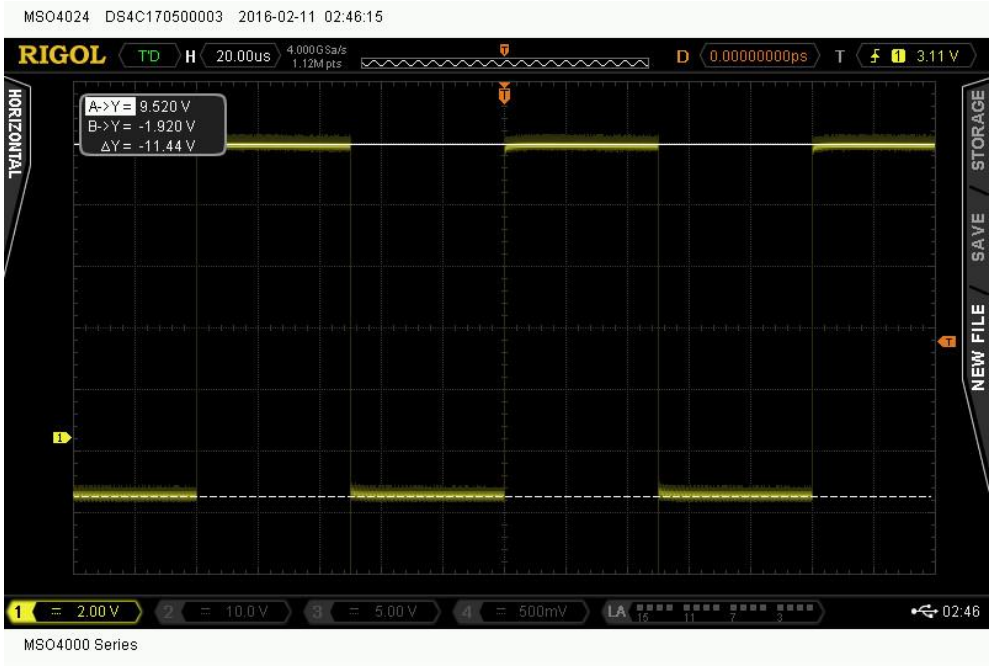


Figure 19: MOSFET Gate Input Signal

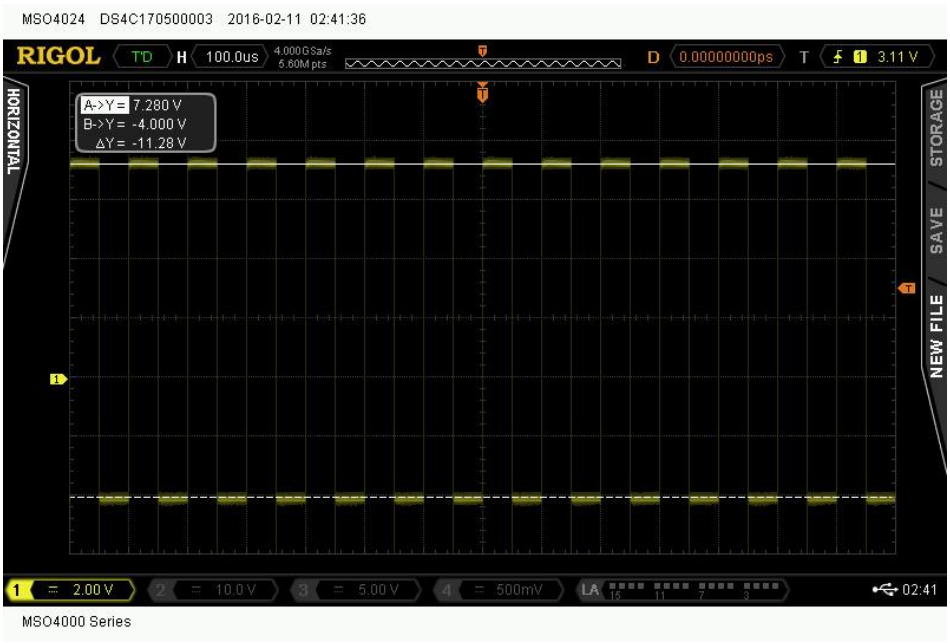


Figure 20: IGBT Gate Input Signal

5.0 EXPERIMENTAL FABRICATION AND TESTING

A full test bed was constructed to experimentally test the thermal and electrical performance of the dc/dc boost converter, seen in Figure 21. The gate driver PCB was used as the central hub to connect the inductor, transistor, power supply, and load resistors. The system was constructed such that the transistor's thermal and electrical performance would not be influenced by other components. All major component values, and part numbers are listed in Table 8.

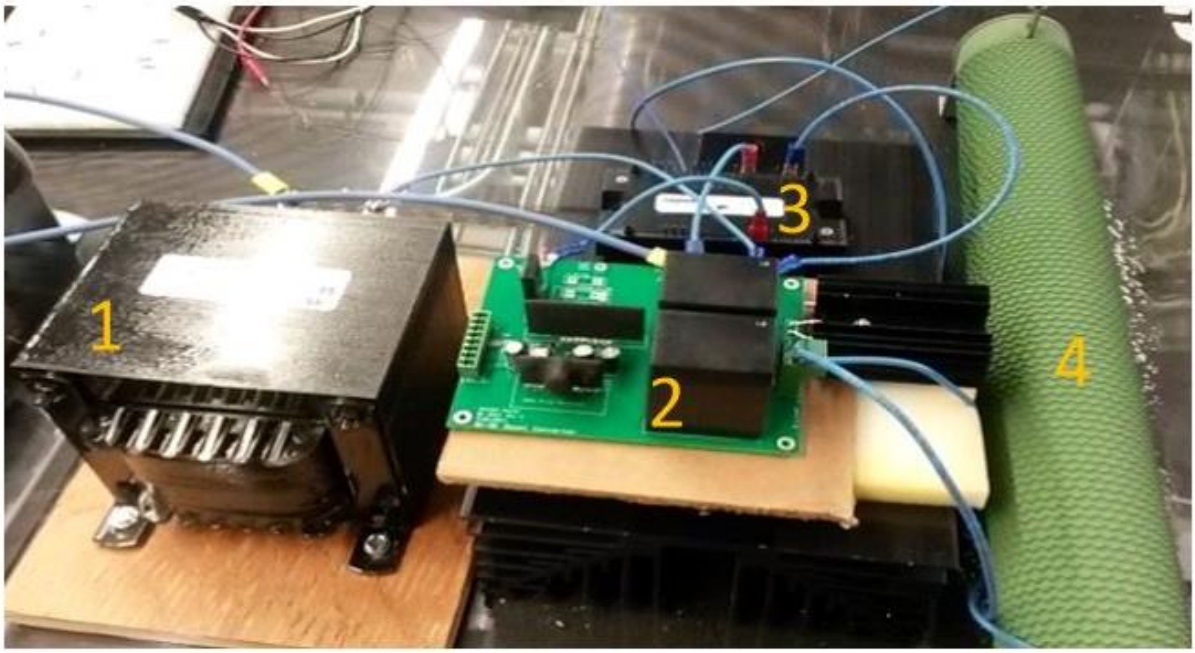


Figure 21: Experimental setup with 30 mH inductor (1), Gate Driver PCB (2), SiC MOSFET (3), Load Resistor (4)

Table 8: DC/DC Boost Converter Test Bed Components

Component	Manufacturer	Part Number
Inductor	Hammond	195P20
Output Capacitor	Panasonic Electronic	P15865
Load Resistor	TE Connectivity	2-1879456-5
System Diode	Fairchild Semiconductor	ISL9R18120G2
Power Supply	Magna Power	SL500-5.2/205+LXI

5.1 GATE DRIVER THERMAL TESTING

Thermal constraints are one of the leading causes of failure in power electronic systems [42]. The thermal stress in power semiconductors is closely linked to the heat sink size, converter power density, and overall converter efficiency. The use of WBG semiconductor devices reduces these constraints because of their lower sensitivity to high temperature. However, the associated gate drive circuits are critical to the operation of power transistors, and induced thermal stresses in the driver components can degrade performance of the switching semiconductors. As an example, cross coupling heat flow between components on the same plane contributes to higher operating temperatures [43].

5.1.1 ANSYS Icepak Printed Circuit Board Parameters

The PCB that was designed in Section 3.2 was first analyzed and imported into ANSYS Icepak, as seen in Figure 22. With the assumption that the power losses are distributed homogeneously throughout component volumes, estimated loss quantities (some as a function of frequency) for all major components were assigned and shown in Table 9. These were primarily derived from

datasheets, as well as a circuit analysis knowing the required voltage and current produced by the driver to turn the transistor on. The simulation used the SiC MOSFET configuration.

Table 9: Gate Drive Circuit Loss Parameters at 1 kHz

Component	Loss (W)
DZ1	0.1
Voltage Regulator	0.05
C1	0.0336
C2	0.0282
C3	0.0104
R1	0.125
10 µF Capacitor	0.0062
33 µF Capacitor	0.0062
C4	0.0336
VLA513	0.02
VLA106-15242	0.2075

5.1.2 Simulation and Experimental Results

ANSYS Icepak is a finite element analysis software that simulates the thermal performance of mechanical and electrical systems. The simulations were conducted in Icepak because the designed PCB could be imported directly from the original files into Icepak, seen in Figure 22. The parameters presented in Table 9 were imported into the FEA model and simulated at a 1 kHz operating frequency.

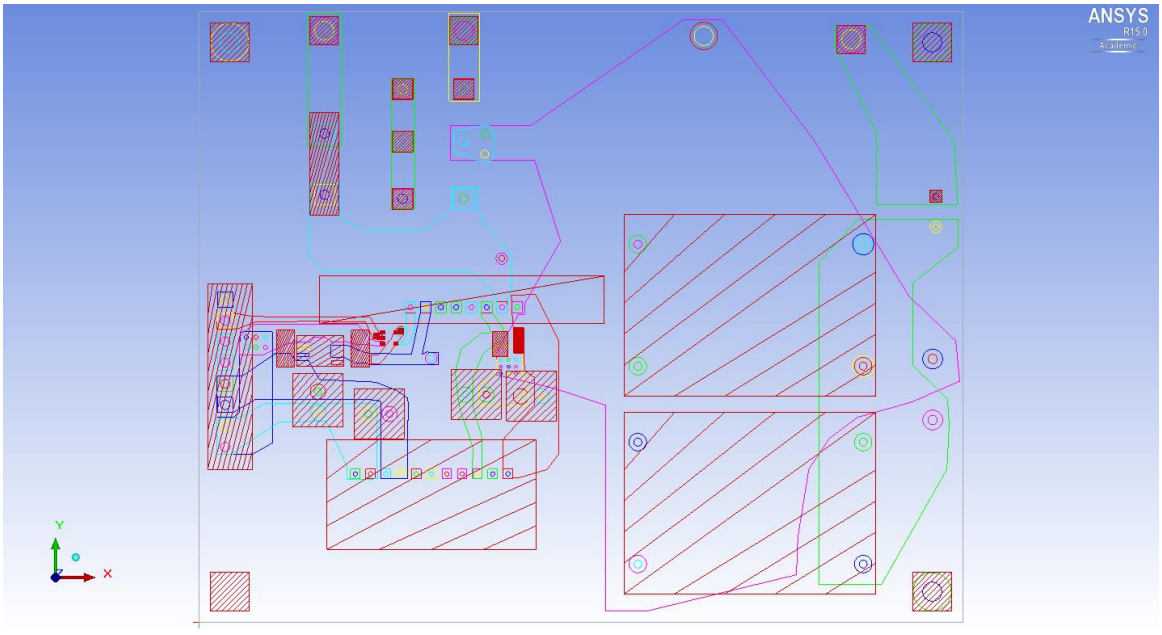


Figure 22: PCB design imported to ANSYS Icepak

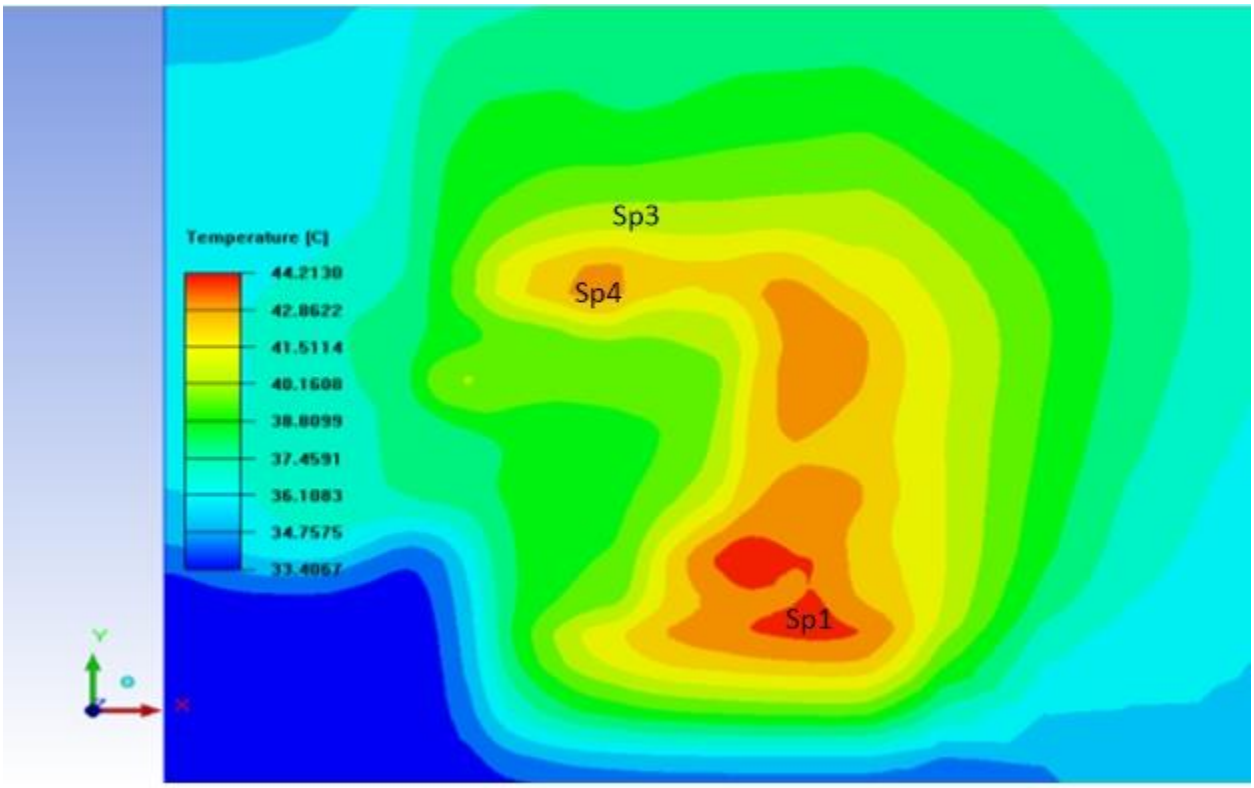


Figure 23: Icepak Simulation Results of Gate Drive Circuit

The simulation results concluded that the hottest components were the isolating DC/DC converter and the gate driver chip (Sp1 and SP4 of Figure 23). The general current path can be understood by the heat contour mapping, where the hotter locations identify more current or power dissipation. The simulation results were compared and validated against experimental results observed by a FLIR E-8 thermal imaging camera and seen in Figure 24. The experimental tests were conducted when the DC/DC boost converter was configured with the SiC MOSFET as the primary switching device, and boosted a 5 Amps (129 Volt) input. A strong relationship between the simulated and experimental results was identified. Simulated results provided a basis that the gate driver circuitry would not exceed thermal limitations as dictated by manufacturer datasheets, nor add undesired stresses to the switching transistor.

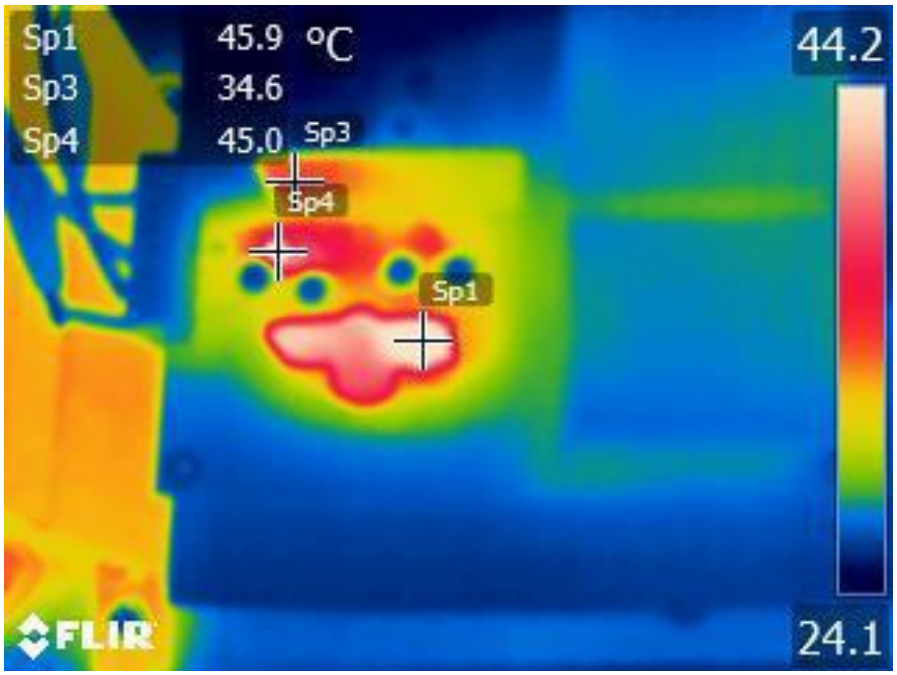


Figure 24: Experimental Results of Gate Drive Circuit

5.2 THERMAL SATURATION TESTING

Thermal equilibrium between the transistor junction and the baseplate was desired for the thermal experimentations; however, it was unclear after how long this would occur. As such, experimental tests were conducted on the Si IGBT to discover when a linear relationship of temperature, with respect to time, was established. Temperature measurements were taken using a K-type thermocouple that was connected onto the baseplate of the Si IGBT with thermally conducting tape. Temperatures were measured for a system operating at 10 kHz with 3 Amp, 5 Amp, and 7 Amp inputs at even increments for a total of 15 minutes. The recorded data is depicted in Figure 25. The desired testing method for full electrical and thermal testing would include transitioning between switching frequencies consecutively after set time intervals. Tests would be swept from the initial 1 kHz to 25 kHz.

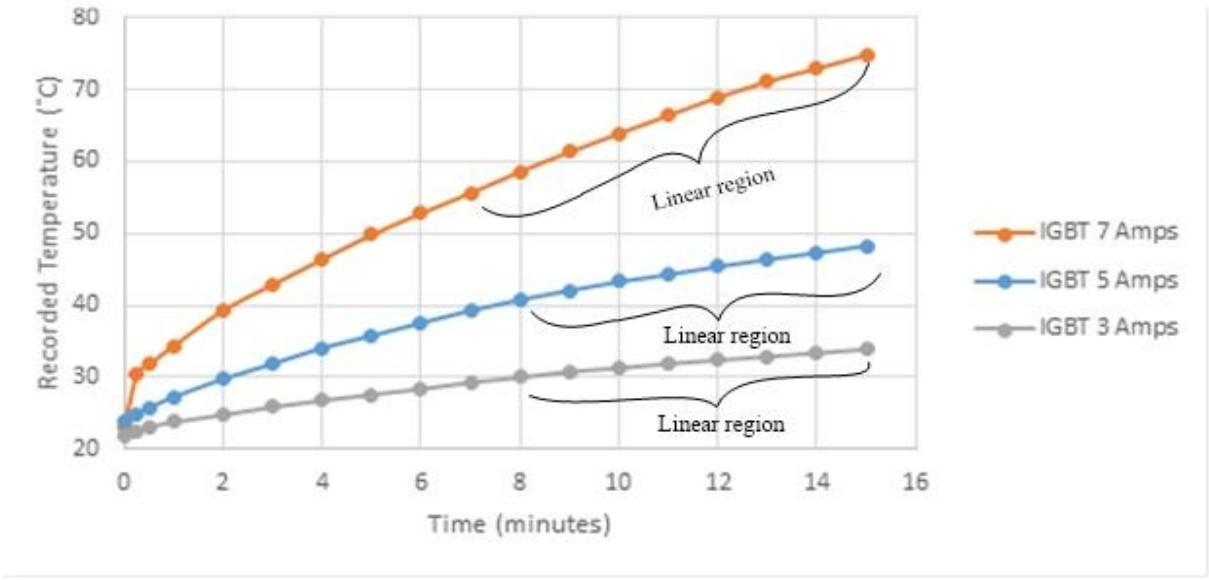


Figure 25: Si IGBT Thermal Saturation Results

It was observed that after 8 minutes of continuous operation, the transistor temperature increased linearly. This is assumed to provide a thermal equilibrium between the baseplate and transistor junction. Because of the linear trend observed in each power level, it was decided that each test would be conducted for 10 minutes. It was unclear, however, if the transistor would re-establish a linear relationship after increasing switching frequency in continuous operation. An experiment was conducted to observe the transition between consecutive switching frequency tests. Figure 26 shows the continuous operation of consecutive tests of the converter operating under a 5 Amp, 128 Volt input and between 10 kHz and 13 kHz.

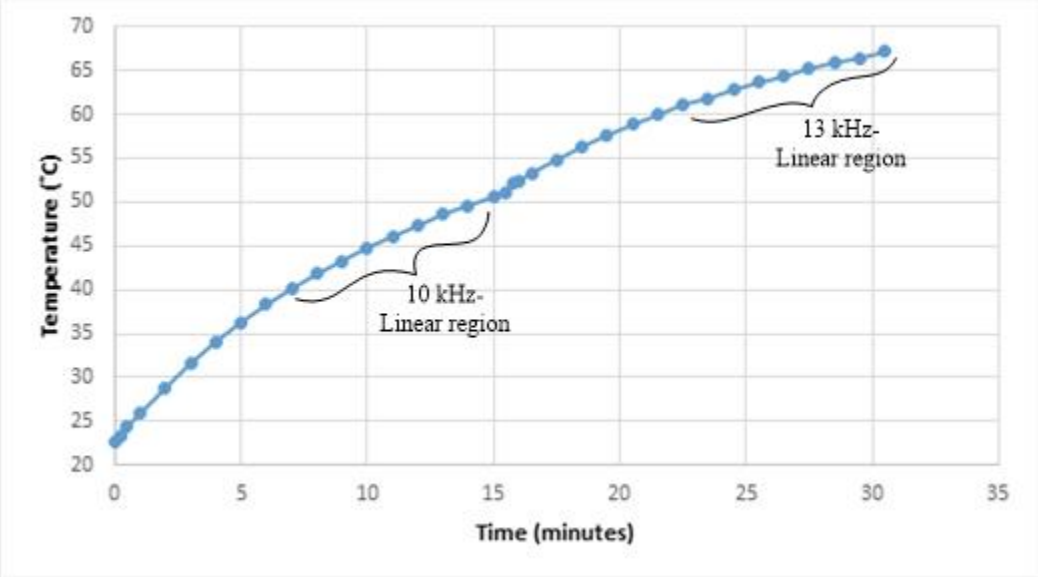


Figure 26: Switching Frequency Thermal Saturation Results between 10 kHz and 13 kHz

Following 15 minutes of continuous testing, the transistor was set to operate at 13 kHz and set to operate for an additional 15 minutes. It was found once again that a linear relationship developed after 8 minutes within the first 10 kHz range, and 8 minutes for the 13 kHz range. This test validated the assumption that 10 minute tests can be operated consecutively

5.3 ELECTRICAL AND THERMAL EXPERIMENTAL MEASUREMENTS

As described in Section 4.2, electrical and thermal tests were 10 minutes in duration to achieve thermal equilibrium between the transistor junction and baseplate. The averaged input current, input voltage, and output voltage across the load were recorded using a Rigol MSO4024 oscilloscope. The temperature was measured with a K-type thermocouple that was connected onto the power module's baseplate. No external heatsink is used, such that a stronger comparison of the operating temperatures can be made between the Si and SiC devices, and converter electrical efficiency.

The electrical efficiency measurements can be seen in Figure 27 and Figure 28. It is observed that the increase in switching frequency incurs additional losses in the transistors that reduces the overall efficiency of the converter and increases the operating temperature of the transistors. Efficiency results, for both devices, express a concave trajectory, exposing an optimal switching frequency to operate the converter. The overall operating conditions applied onto the transistor devices are minimal against the device ratings, but Figure 27 and Figure 28 both show a consistent trend that can be inferred to increase with higher voltages and currents.

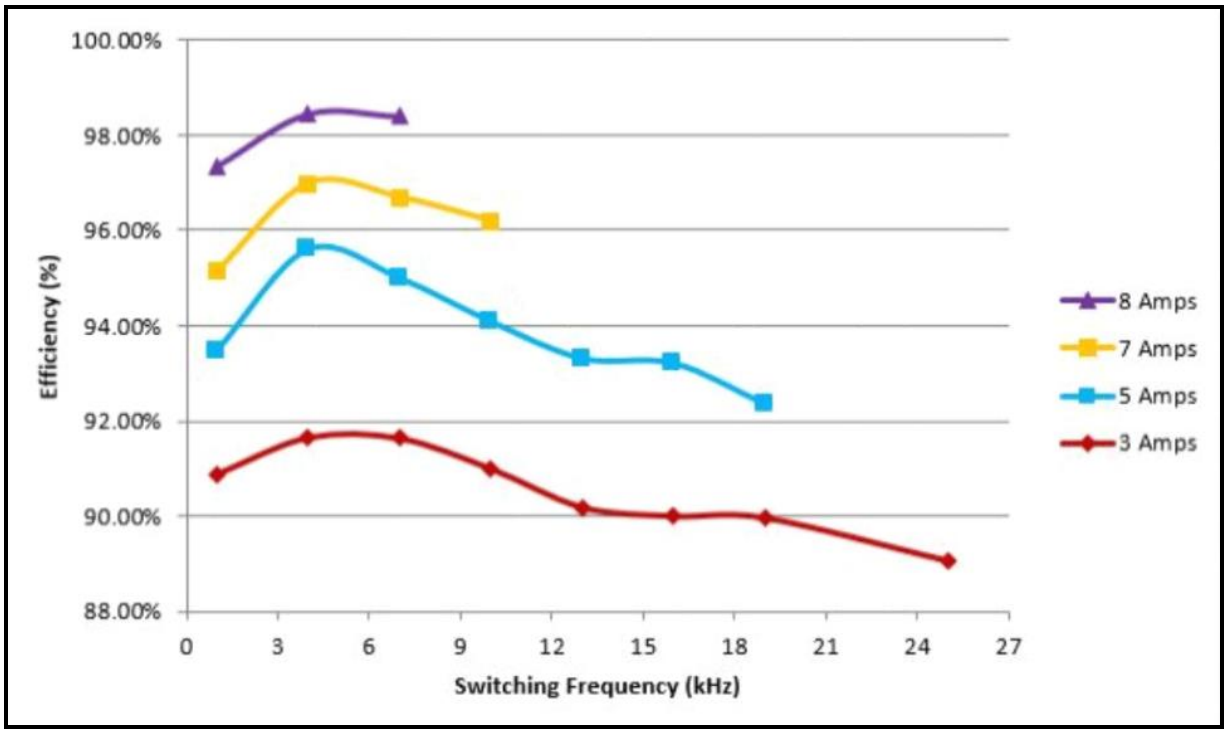


Figure 27: Si IGBT Experimental Efficiency vs. Frequency

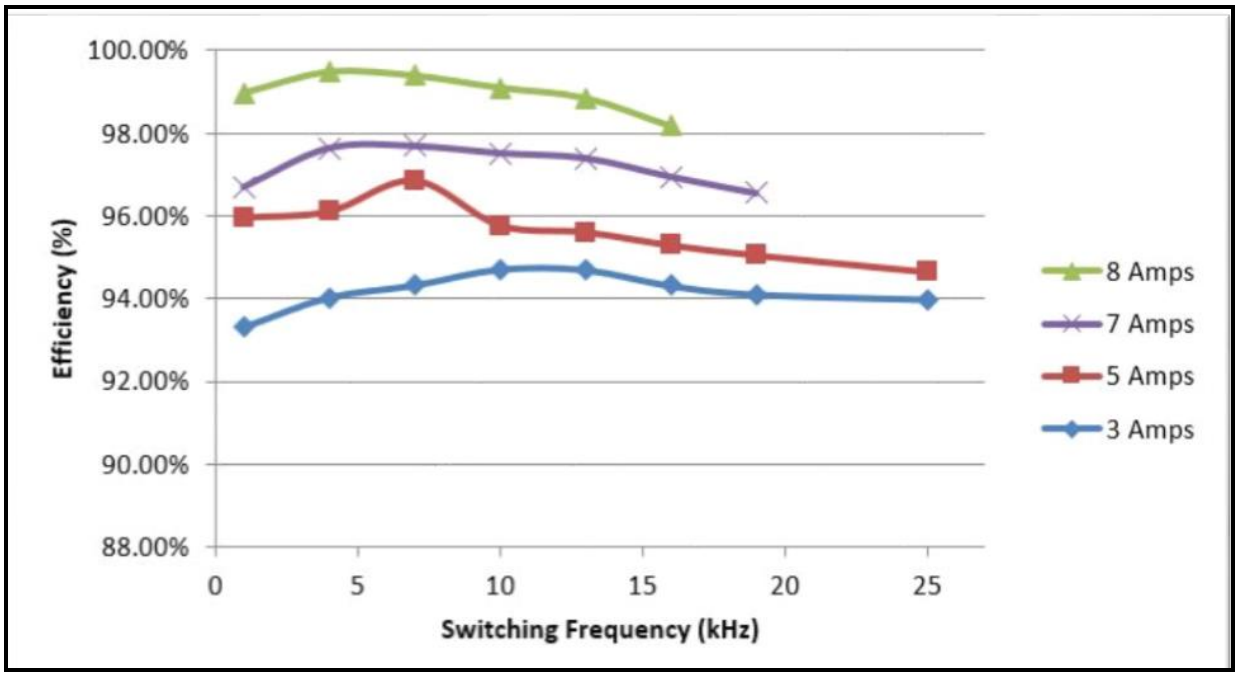


Figure 28: SiC MOSFET Experimental Efficiency vs. Frequency

Figure 29 and Figure 30 show the experimentally measured device temperatures, and as expected, the SiC MOSFET operates at much lower temperatures. The IGBT, seen in Figure 29, was unable to operate across the complete range of switching frequencies and currents due to the absence of a cooling system. While the SiC MOSFET operated at lower temperatures, the converter system diode failed from its own thermal stresses in the 7 and 8 amp tests, providing inconclusive values at 19 and 25 kHz (Figure 30).

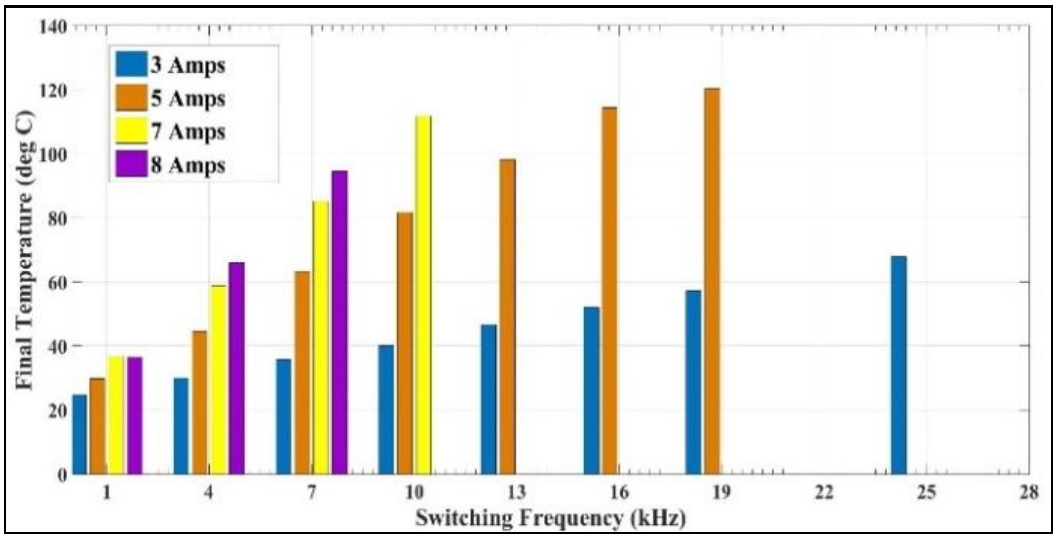


Figure 29: Si IGBT Experimental Temperature vs. Frequency

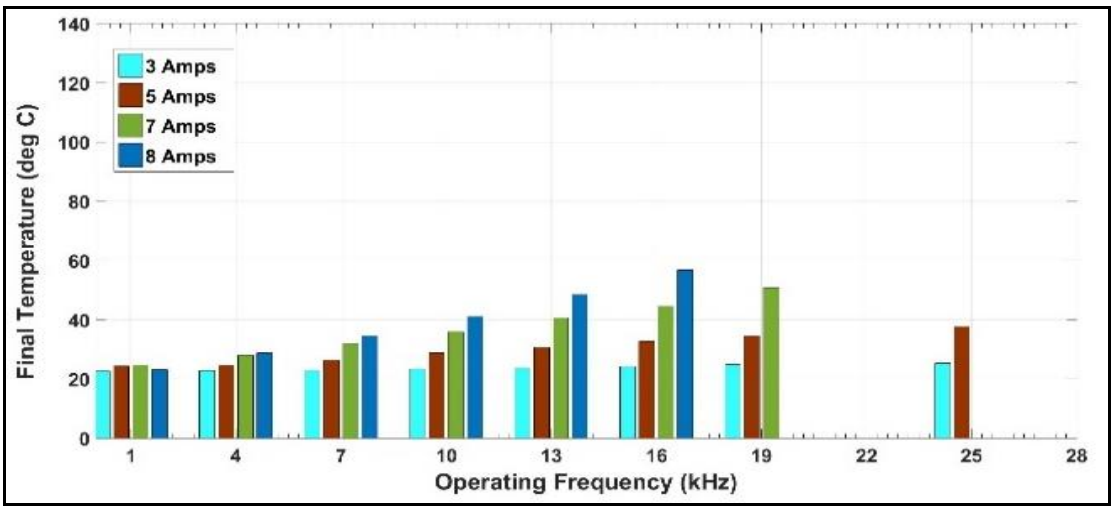


Figure 30: SiC MOSFET Experimental Temperature vs. Frequency

6.0 SIC MOSFET THERMAL PREDICTION

In power transistor devices, there are two major causes of thermal power dissipation- conduction losses and switching losses [11, 14, 35, 44]. The conduction losses are directly related to the electrical characteristics of the transistors application with respect to the ON-resistance, and the switching losses are associated to the switching energies and frequency of the switching events [14, 35, 45]. The summation of these losses expresses the total losses of the device which generates heat at the junction of the transistor. Equation 6.0 -1 shows the combination of the conduction losses ($E_s f_s$) where E_s is the device switching energy and f_s is the transistor switching frequency, and the conduction losses $R_{on} I_{DS}^2$ - where R_{on} is the on-resistance, and I_{DS}^2 is the transistor drain-source current. These losses correspond to an increase in junction temperature, T_J, with respect to ambient temperature, T_A, and the thermal resistance θ_{JA}.

$$E_s f_s + R_{on} I_{DS}^2 = \frac{(T_J - T_A)}{\theta_{JA}} \qquad (6.0\text{ -1})$$

6.1 PARAMETER IDENTIFICATION

Many of the variables in eq. 6.0 -1 are material properties detailed in a transistor manufacturer datasheet (E_s, R_{on}, θ_{JA}), or the designed electrical system (I_{DS}, f_s). The access of these parameters implies the junction temperature can be predicted using eq. 6.0 -1. This equation has been previously used to determine and optimize other operating parameters like I_{ds} or f_s [14, 44, 46]. This work, however, sweeps the transistor operating frequency to characterize the effects of the switching frequency on thermal performance. The junction temperature of a Powerex SiC MOSFET power module (QJD1210SA1) in the dc/dc boost converter system was analytically predicted strictly using the device properties found in the datasheet and electrical parameters determined from the converter topology. The results from eq. 6.0 -1 could then be used to identify the operating temperature of the transistor, and design an appropriate thermal management system to ensure transistor and converter operation.

Using the device datasheet, R_{on} and θ_{JA} were determined to be 23 mΩ, and 0.28 $R_{on}\frac{^oC}{W}$, respectively [8]. The switching energy, E_s, while not included on this particular datasheet, is characteristically included in standard datasheets. Because the switching energy was not included in the datasheets of the evaluated device, experimental tests were conducted to measure the appropriate switching energies. To calculate the switching energies, the transistor received a pulsed gate-source signal to briefly turn on the device. The pulse test was performed while the converter operated in the constructed dc/dc converter to observe the specific ON/OFF switching events. The traditional calculation to determine switching energies is shown in Equations 6.0 -2 through 6.0 -4 [14, 35, 44, 47, 48]. The turn on and off energies, E_{on} and E_{off}, are calculated

through an integration of the switching waveform of the voltage (V_{DS}) and current (I_{DS}), across and through the transistor between specific time increments. For turn ON, when the voltage decreases across the transistor between times t_1 and t_2, the current passes through the open device channel. This transition produces an overlap between the voltage and current, and it is the area beneath the overlap that is the on-switching energy. The OFF-switching energy is produced in the same way, except between times t_3 and t_4, and the voltage is increasing and the current decreasing across and through the transistor [47, 48].

$$E_s = E_{on} + E_{off} \tag{6.0-2}$$

$$E_{on} = \int_{t1}^{t2} (V_{DS}(on) I_{DS}(on)) dt \tag{6.0-3}$$

$$E_{off} = \int_{t3}^{t4} (V_{DS}(off) I_{DS}(off)) dt \tag{6.0-4}$$

The switching on and off waveforms were captured with a Rigol MS04024 oscilloscope and shown in Figure 31 through Figure 34. The oscilloscope's inherent mathematical function was used to integrate over the area t_1 and t_2 for turn ON and t_3 and t_4 for turn OFF of the captured waveform. Because the switching energies are temperature and current dependent, experimental testing was performed at each of the desired I_{DS} values of 3, 5, 7, and 8 Amps to be used in the predictive junction temperature calculations. The summation of the ON and OFF energies at each current rating are shown in Table 10 and finalizes the transistor parameters required to predict the transistor junction temperature from data sheet values.

Table 10: Measured Switching Energies for Transistor Drain-Source Currents

I_{ds} (Amps)	3	5	7	8
E_s (mJoules)	1.036	2.222	5.6	8.216

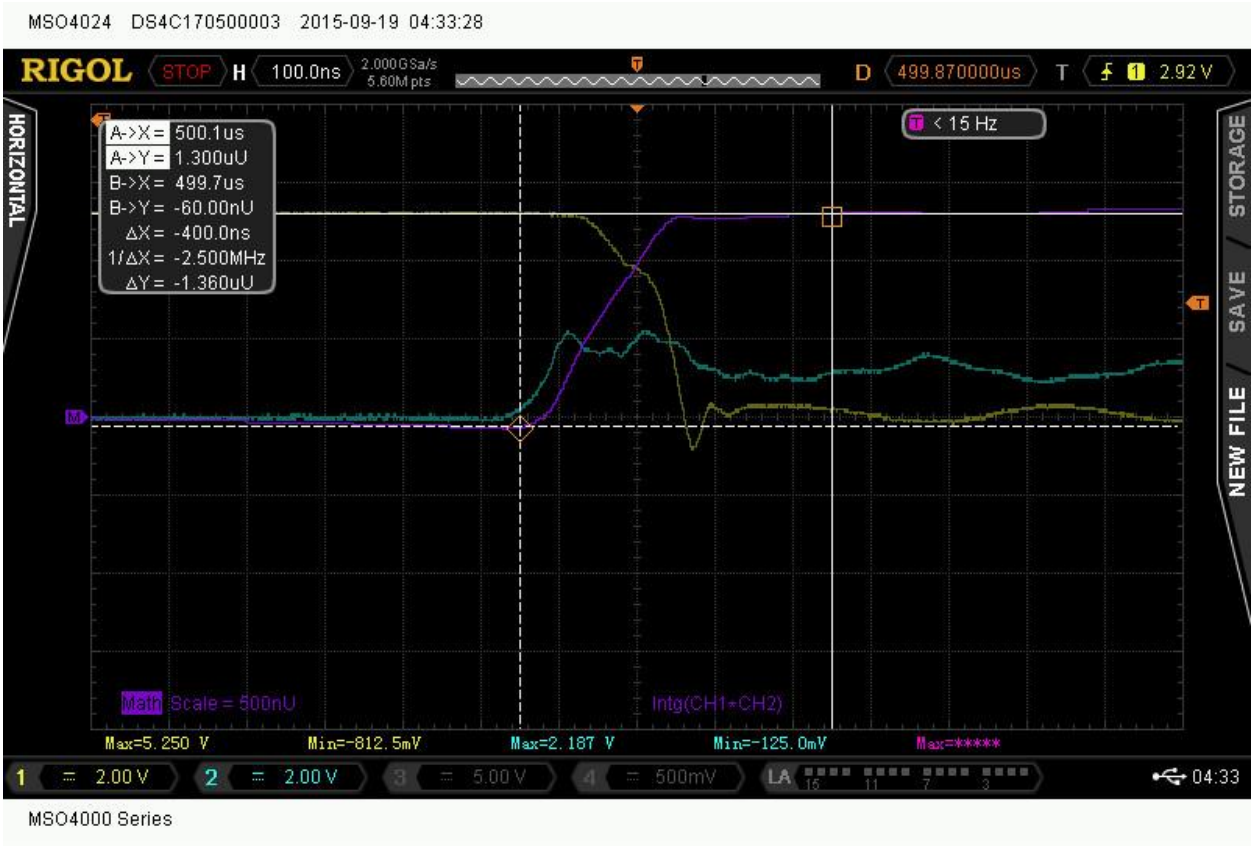


Figure 31: 3 Amp, Switching ON waveform

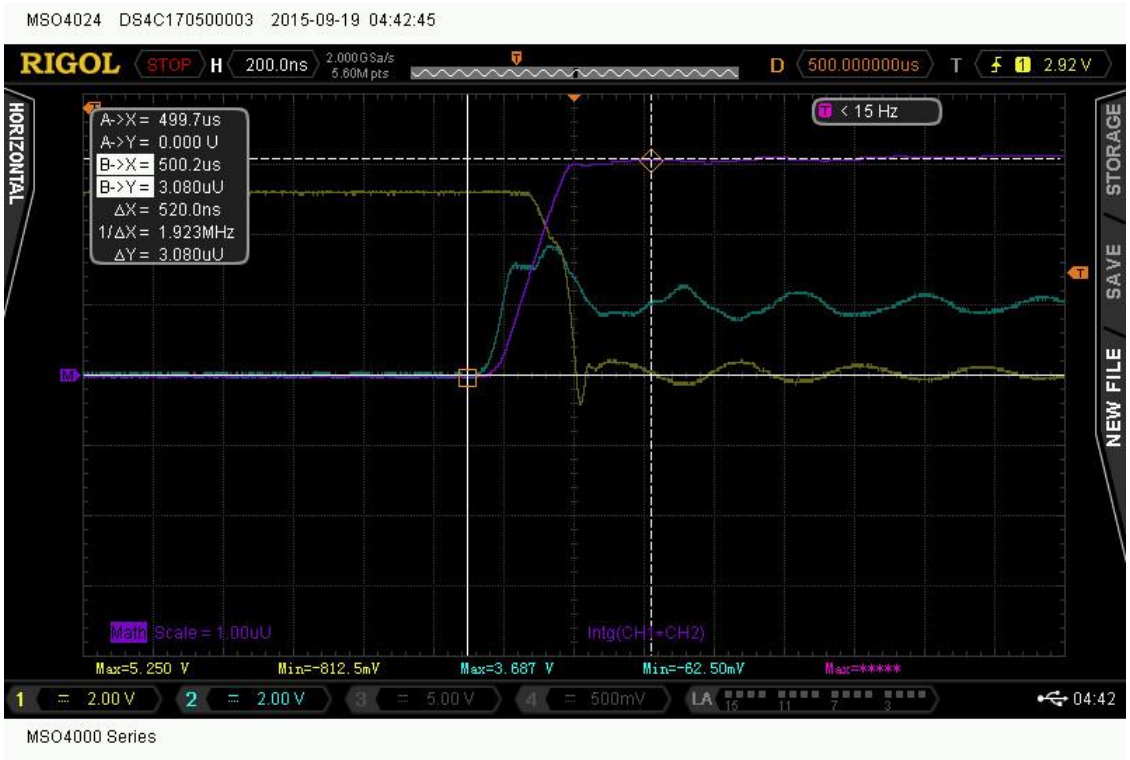


Figure 32: 5 Amp, Switching ON waveform

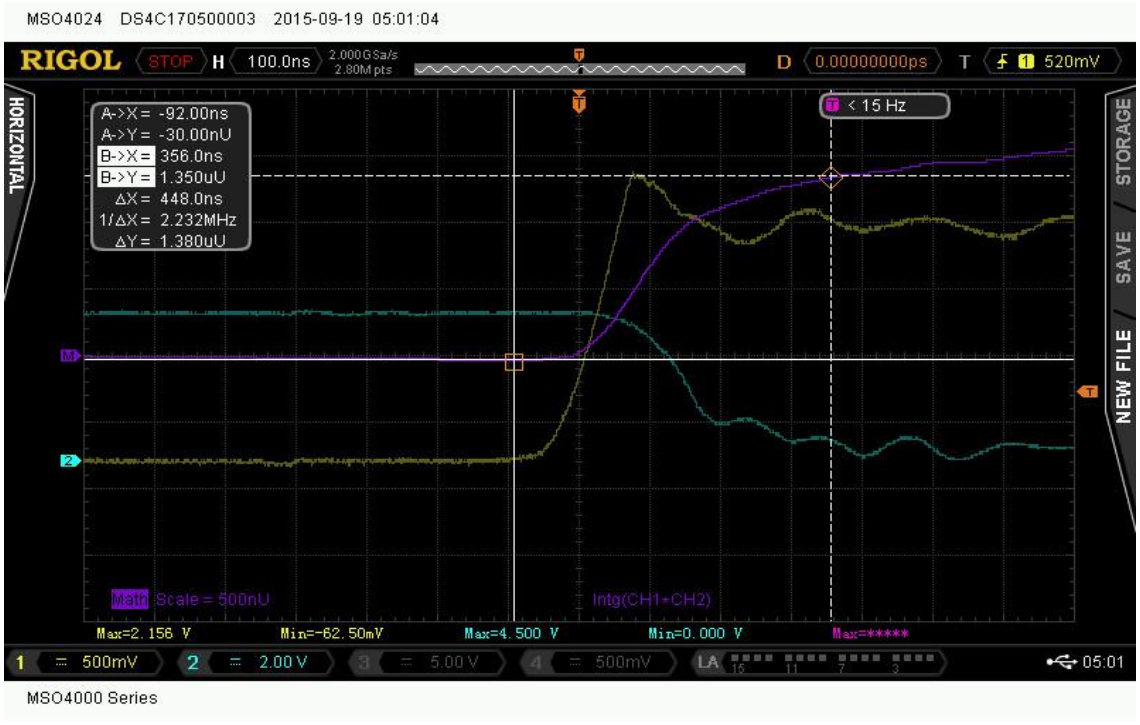


Figure 33: 7 Amp, Switching OFF waveform

Figure 34: 8 Amp, Switching OFF waveform with calculations

6.2 PREDICTED TEMPERATURE RESULTS

Table 11 shows the variables used to predict the temperature, and the predicted temperature results are shown in Table 12.

Table 11: Device and System Variables to Predict Junction Temperature

Parameter	Numerical Quantity
R_{on} (25℃)	23 mΩ
θ_{JA}	0.28 $\frac{℃}{W}$
I_{DS}	3,5,7,8 Amps
E_S	Table 10
f_s	1000-25000 Hz

Table 12: Predicted SiC MOSFET Junction Temperature (˚C)

Switching Frequency (Hz)	Calculated Junction Temp. (3 Amps)	Calculated Junction Temp. (5 Amps)	Calculated Junction Temp. (7 Amps)	Calculated Junction Temp. (8 Amps)
1000	22.348	23.582	24.784	23.513
4000	23.218	25.443	29.488	30.415
7000	24.089	27.304	34.192	37.316
10000	24.959	29.166	38.896	44.218
13000	25.829	31.027	43.599	51.119
16000	26.699	32.889	48.304	58.021
19000	27.570	35.750	53.008	82.873
25000	30.310	40.473	62.416	114.628

There are two conclusions that can be drawn from the results. First, the junction temperature can be mathematically predicted. This can be used as a tool to decrease design errors and increase operational performance of the transistors. Second, this method can help predict an optimal switching frequency in conjunction to electrical efficiency simulation results as discussed in Section 4.2.

7.0 ANALYSIS OF SIMULATED AND EXPERIMENTAL RESULTS

This section presents the comparison between simulated/predicted results with experimentally acquired data. Conclusions from each of the dependencies, converter efficiency and operating temperature, with switching frequency, are expressed in Sections 7.1 and 7.2 respectfully.

7.1 ELECTRICAL EFFICIENCY ANALYSIS

The relationship between all simulated and corresponding measured data are shown in Figure 35 through Figure 42. Table 13 and Table 14 explicitly shows the absolute error- absolute value of the difference in percentage between the electrical efficiencies. Overall, the results show very strong relationships, especially as the converters move into the designed region of operation (8 Amp input). The average difference between the simulated and measured SiC MOSFET results is approximately 1%, and 2.6% for the Si IGBT.

With the close relationship between the simulated and experimental data, it can be recognized that device models in Synopsys Saber can be used to determine converter efficiency, and increase accuracy in a project's design phase. Certain assumptions explain the absolute error between the results. Limitations of the SaberRD device models, and simulation parameters are theorized to be strong factors in the small error. The IGBT and MOSFET models do not include additional factors such as dynamic thermal parameters, in addition to the packaging parasitic

inductance and capacitances. It is known that continuous operation of a system will lead to increases in temperature through components, in addition to the wiring connecting components. This will alter the resistance through the connecting wiring and can incur additional losses and converter operation not detailed in these simulations.

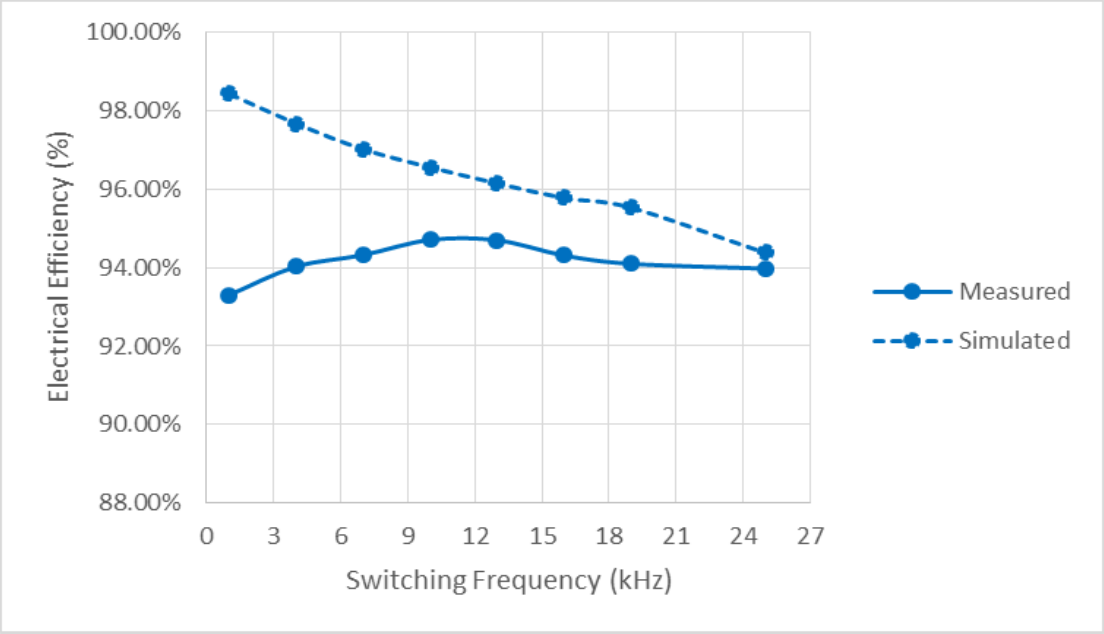


Figure 35: Efficiency comparison, SiC MOSFET- 3 Amps

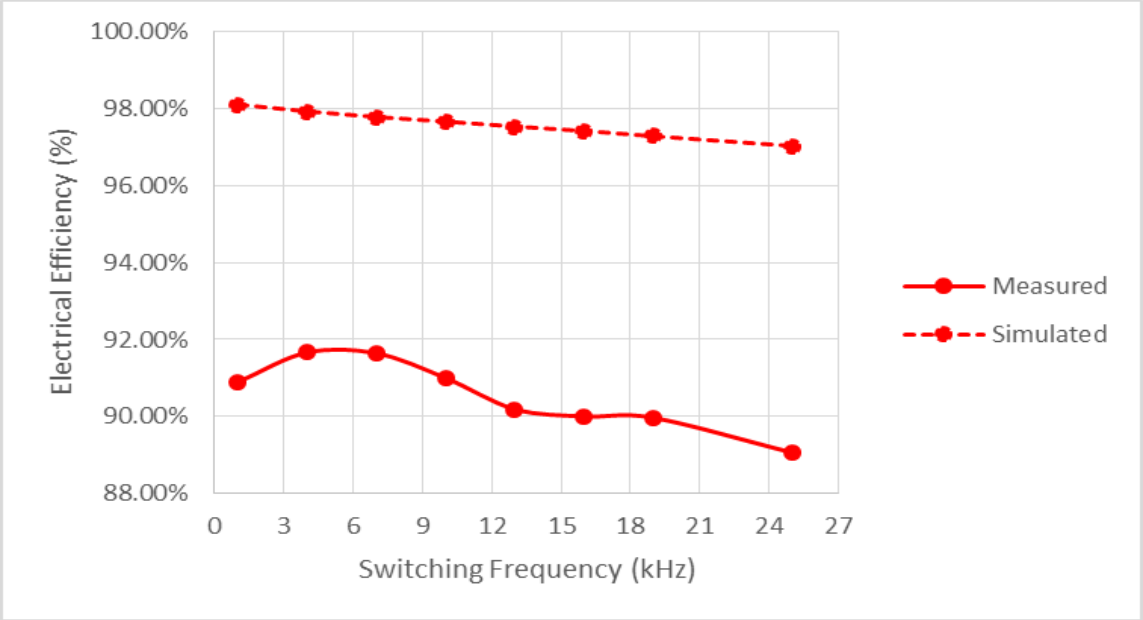


Figure 36: Efficiency comparison, Si IGBT- 3 Amps

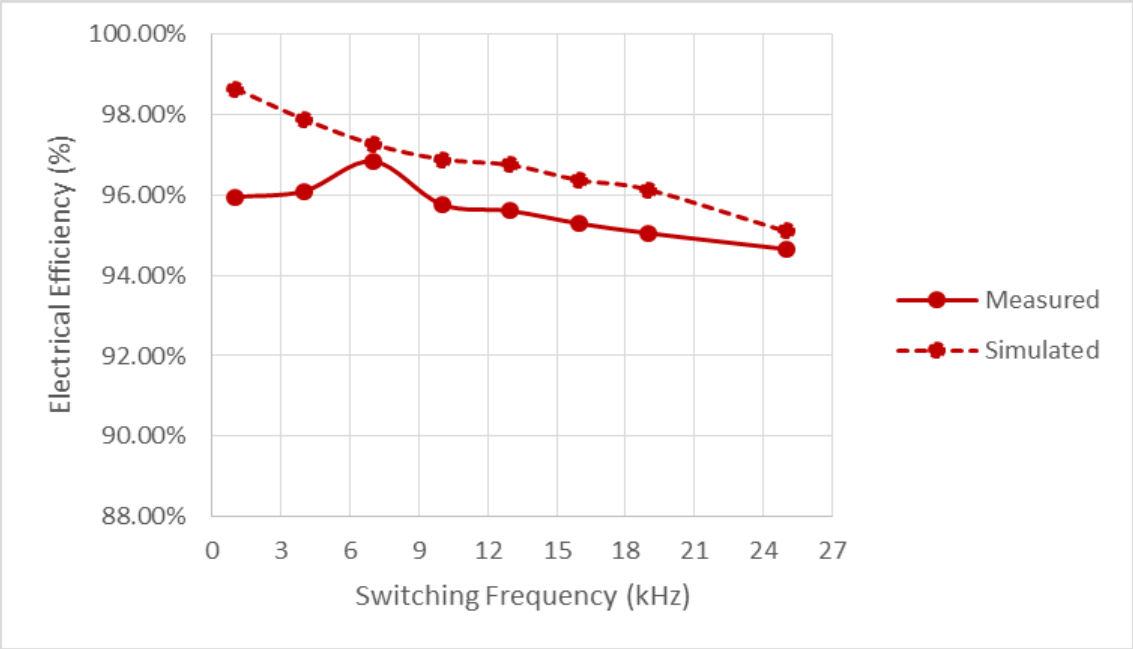


Figure 37: Efficiency comparison, SiC MOSFET- 5 Amps

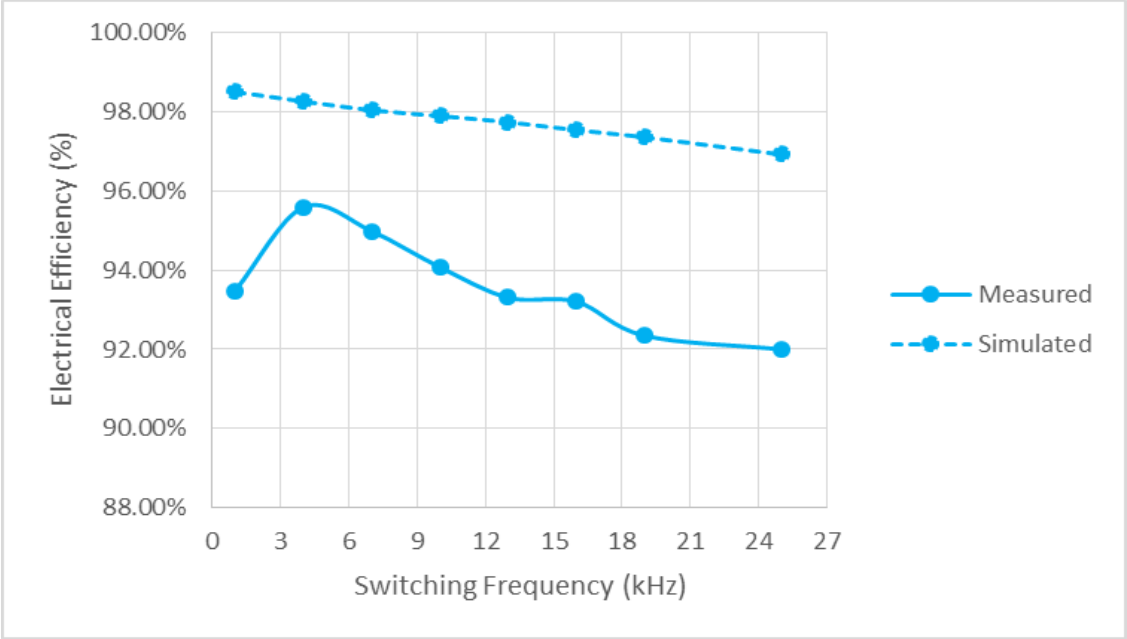


Figure 38: Efficiency comparison, Si IGBT- 5 Amps

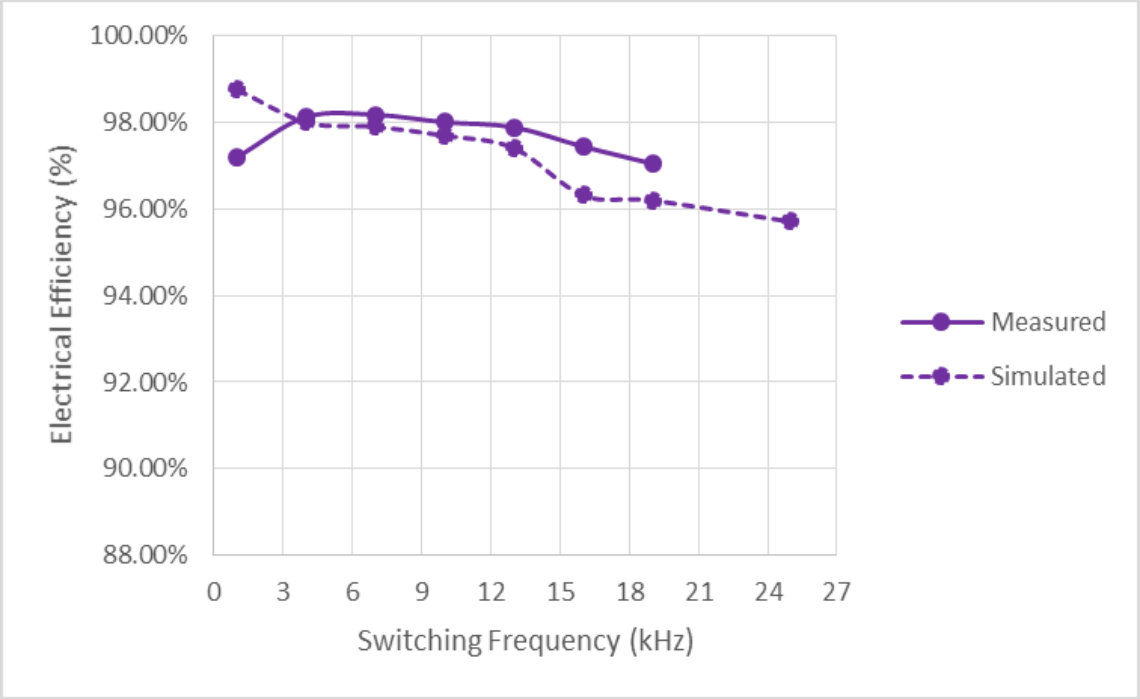


Figure 39: Efficiency comparison, SiC MOSFET- 7 Amps

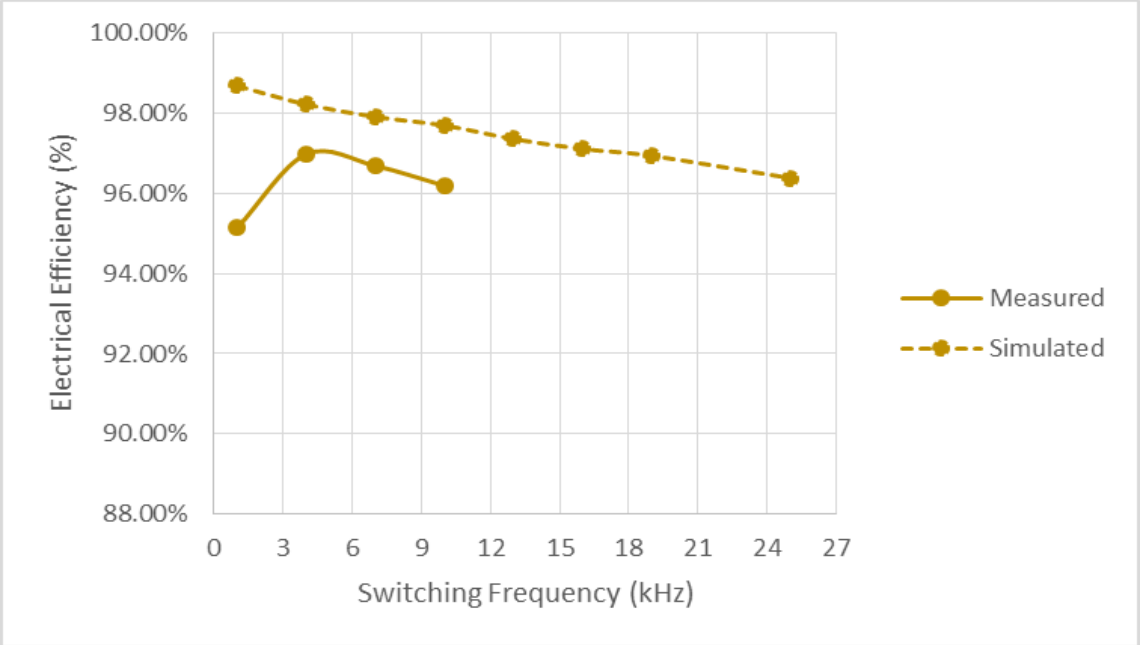


Figure 40: Efficiency comparison, Si IGBT- 7 Amps

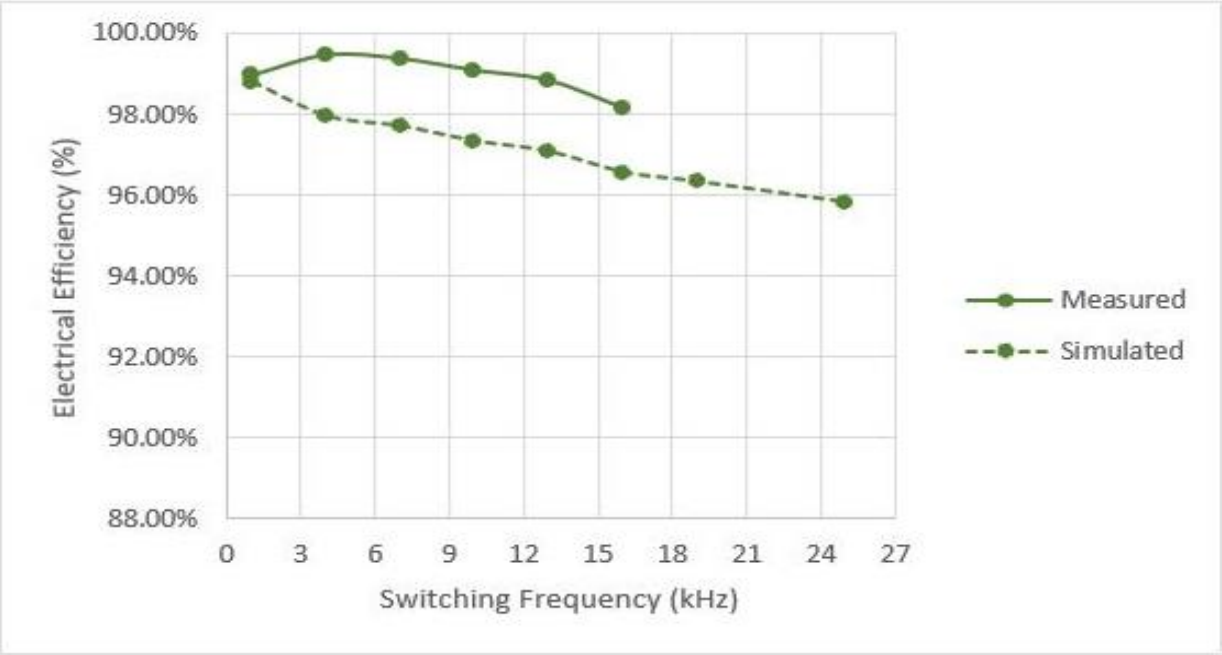


Figure 41: Efficiency comparison, SiC MOSFET- 8 Amps

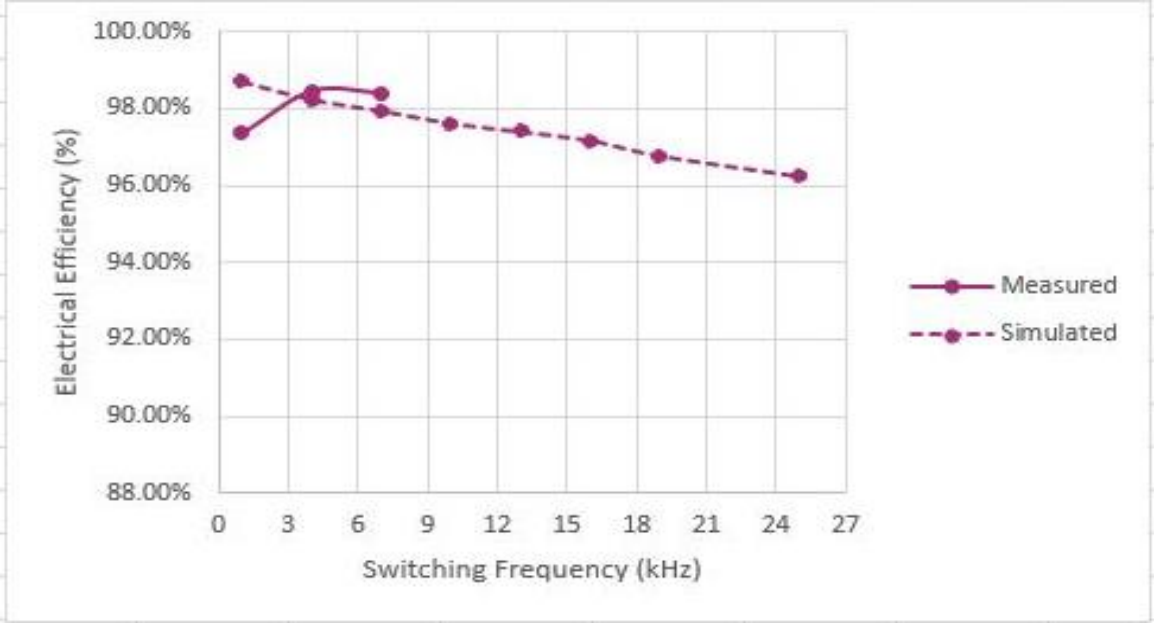


Figure 42: Efficiency comparison, Si IGBT- 8 Amps

Table 13: Absolute error between simulated and measured SiC MOSFET results

Switching Frequency (Hz)	Absolute Error (3 Amps)	Absolute Error (5 Amps)	Absolute Error (7 Amps)	Absolute Error (8 Amps)
1000	5.14%	2.69%	1.57%	0.33%
4000	3.65%	1.78%	0.12%	1.02%
7000	2.71%	0.42%	0.27%	1.18%
10000	1.86%	1.12%	0.31%	1.26%
13000	1.46%	1.14%	0.48%	1.27%
16000	1.47%	1.08%	1.12%	1.10%
19000	1.44%	1.08%	0.85%	N/A
25000	0.42%	0.45%	N/A	N/A

Table 14: Absolute error between simulated and measured Si IGBT results

Switching Frequency (Hz)	Absolute Error (3 Amps)	Absolute Error (5 Amps)	Absolute Error (7 Amps)	Absolute Error (8 Amps)
1000	7.22%	5.04%	3.55%	0.86%
4000	6.27%	2.68%	1.24%	0.70%
7000	6.14%	3.06%	1.22%	0.94%
10000	6.67%	3.83%	1.51%	N/A
13000	7.35%	4.44%	N/A	N/A
16000	7.42%	4.34%	N/A	N/A
19000	7.33%	5.02%	N/A	N/A
25000	7.98%	4.93%	N/A	N/A

7.2 THERMAL PERFORMANCE ANALYSIS OF SIC MOSFET

While individual thermal results are expressed in Section 5.3, Figure 43 shows the experimentally collected data for both the Si IGBT and SiC MOSFET together. Due to its ability to remain cooler with increasing switching frequency (and potentially higher power) environments, the SiC MOSFET can operate more safely thus reducing the need for a large heatsinking component. Conversely the Si IGBT requires a significant cooling system to handle

the 8 Amps (5% of the device's rated current limit) at a 7 kHz (28% of rating) switching frequency to operate with the highest electrical efficiency. Thermal constraints for safe transistor operation become significantly more important with the observation of an optimal switching frequency. This connection between electrical efficiency and thermal performance with respect to switching frequency has not been shown before in literature.

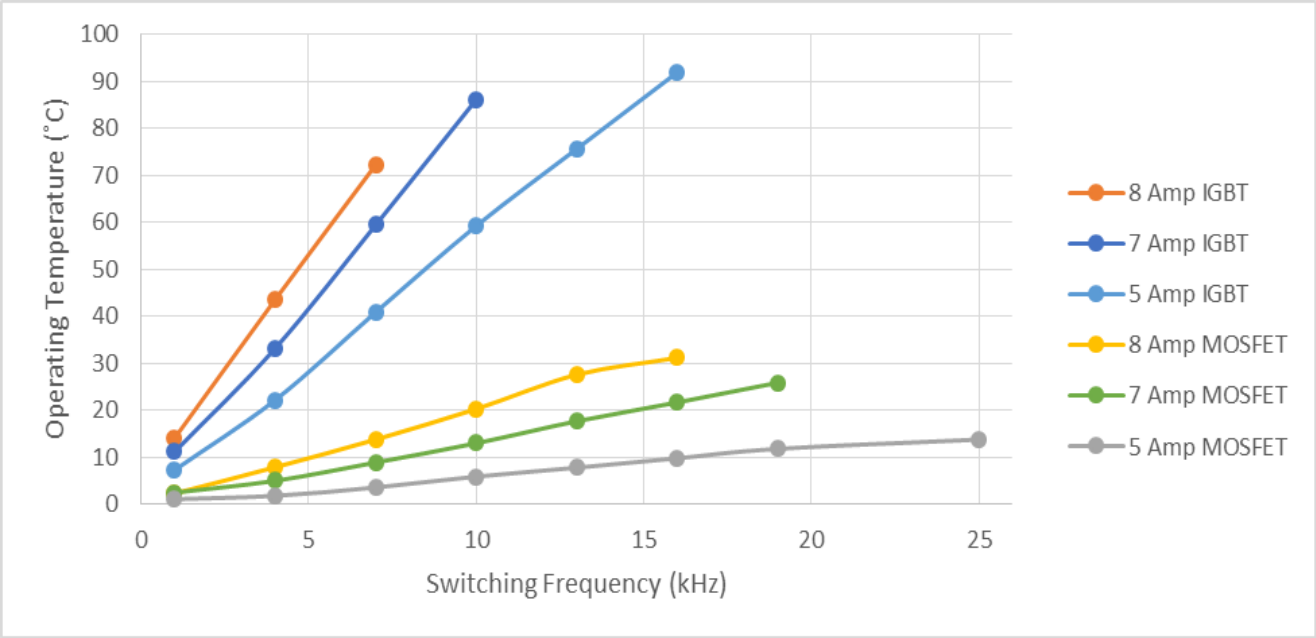


Figure 43: Comparison of experimentally collected IGBT and MOSFET operating temperatures

Experimental results for the SiC MOSFET are expressed in Section 5.3 while the mathematical predictions are derived in Section 6.2. The comparison of the results, shown in Table 15 through Table 18, proves the utility of the mathematical approach to predict the junction temperature with the switching frequency as the independent variable. The results show some small deviation between the experimental and predicted values, but these are within an

appropriate range. In nearly all cases the predicted temperature was slightly greater than the measured temperatures.

Table 15: Predicted and Measured Temperatures for SiC MOSFET (3 Amps)

Switching Frequency (Hz)	Calculated Junction Temperature (˚C)	Measured Junction Temperature (˚C)	Absolute Error (˚C)
1000	22.34	22.1	0.25
4000	23.22	22.8	0.42
7000	24.09	22.9	1.19
10000	24.96	23.4	1.56
13000	25.83	23.7	2.13
16000	26.70	24.2	2.50
19000	27.57	24.8	2.77
25000	30.31	25.3	5.01

Table 16: Predicted and Measured Temperatures for SiC MOSFET (5 Amps)

Switching Frequency (Hz)	Calculated Junction Temperature (˚C)	Measured Junction Temperature (˚C)	Absolute Error (˚C)
1000	23.59	23.9	-0.32
4000	25.44	24.6	0.84
7000	27.30	26.4	0.90
10000	29.17	28.7	0.47
13000	31.03	30.6	0.43
16000	32.89	32.6	0.29
19000	35.75	34.6	1.15
25000	40.47	36.6	3.87

Table 17: Predicted and Measured Temperatures for SiC MOSFET (7 Amps)

Switching Frequency (Hz)	Calculated Junction Temperature (˚C)	Measured Junction Temperature (˚C)	Absolute Error (˚C)
1000	24.78	25.4	-0.62
4000	29.49	27.9	1.59
7000	34.20	31.8	2.39
10000	38.90	35.9	2.99
13000	43.60	40.6	2.99
16000	48.30	44.6	3.70
19000	53.01	48.8	4.21
25000	62.42	N/A	

Table 18: Predicted and Measured Temperatures for SiC MOSFET (8 Amps)

Switching Frequency (Hz)	Calculated Junction Temperature (˚C)	Measured Junction Temperature (˚C)	Absolute Error (˚C)
1000	23.51	23.1	0.41
4000	30.41	28.7	1.71
7000	37.32	34.6	2.72
10000	44.22	41.1	3.12
13000	51.12	48.4	2.72
16000	58.02	52	6.02
19000	82.87	N/A	
25000	114.63	N/A	

It is theorized that the origins of the absolute error can be drawn from a number of assumptions taken in the analysis. These assumptions include accurate parameter values from the datasheets. There can be great fluctuation in thermal resistance (θ_{JA}) depending on the manufacturing of the embedded heatsink. It was also assumed that the ON-resistance was a constant, where it actually will change with respect to temperature [28, 29, 49]. It is also suspected that the switching energy would have some variation with temperature, a secondary effect of the ON-resistance change [11, 14, 29]. Nevertheless, it was shown that eq. 6.0 -1 can now be extended as a predictive tool for the electrical and thermal behavior of the SiC MOSFET in power switching circuits where the switching frequency was varied.

8.0 DESIGN AND IMPLEMENTATION OF A POWER DENSE MODULAR MULTILEVEL CONVERTER

8.1 MODULAR MULTILEVEL CONVERTER

The modular multilevel converter (M2C) is a power electronic converter topology that was originally developed for use in high voltage direct current (HVDC) converters [50]. The topology boasts several significant advantages over traditional multilevel designs, including its high modularity in hardware and software, low generation of harmonics, lower filtering requirements, easy scalability, and a stronger approximation of a sinusoidal output with increasing submodules. The M2C in Figure 44 consists of *n* series-connected half-bridge submodules on each single-phase arm. Each M2C submodule consists of a half bridge cell where its output voltage is either equal to its capacitor voltage or zero depending on the switching states (two states). A positive and a negative arm are connected to form one branch, with two branches forming the sending and receiving end of a single conversion block. By combining *m* conversion blocks in parallel, the DC current divides evenly between each branch, allowing higher power to be supplied by the inverter without increasing conduction losses.

A benefit of this topology is the small amount of energy that's expended during the switching events (on/off) for each device (transistor). Total semiconductor losses are the sum of two components: (1) conduction losses and (2) switching losses. Conduction losses are equal to

$I_D^2 R_{ON}$ [14, 44]. In this topology, the current flowing through each device is minimized due to the parallel combination of conversion blocks. In addition, switching losses, equivalent to $E_S f_s$ [44, 45] where E_s is the total switching energy (on/off states) of the transistor and f_s is the switching frequency in which the transistor is operating. GaN devices offer very low on/off switching energies [11, 13, 51, 52], and the system is operating the devices at 24 kHz which minimizes the overall effects of switching losses.

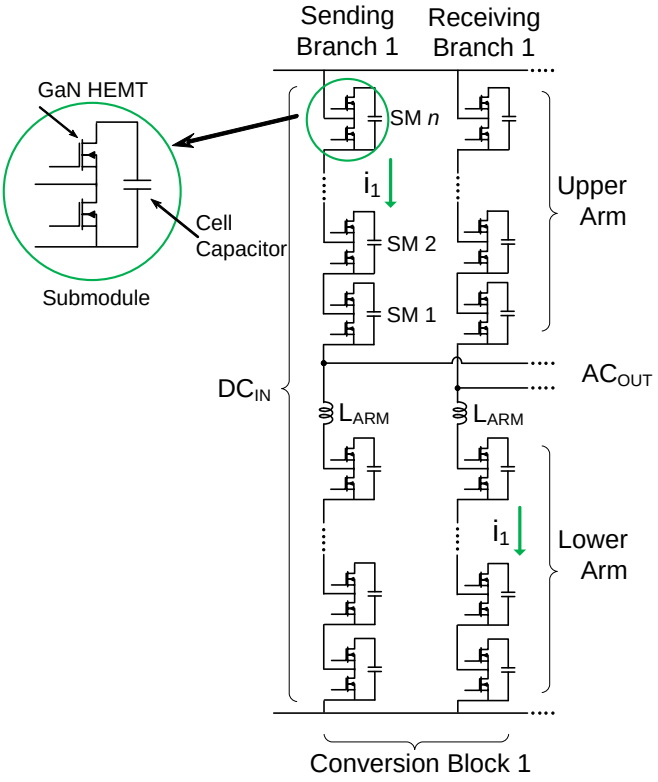


Figure 44: Modular Multilevel Converter (M2C) Topology

8.1.1 Adaptation of Modular Multilevel Converter with GaN HEMT devices

Employing WBG power semiconductor devices into a M2C circuit topology [53] enhances many of the benefits of the traditional MMC system where silicon IGBT devices have been used. These IGBT devices, used primarily in HVDC [50], as well as medium voltage motor drive systems, are operated at low switching frequencies. Defining a low carrier frequency, in conjunction with a low switching frequency, decreases the switching losses of the transistors [54]. These systems are designed with hundreds of cells per arm, as well as large cell capacitances. In the case of a high, power density design, it is desirable to avoid extreme numbers of cells or capacitor size, as both of these components require large amounts of additional physical space. In contrast, the converter design described here utilizes GaN enhancement-mode HEMT (normally OFF) devices instead of traditional silicon devices with the aim of reduced size. Because of the device's low intrinsic capacitance, low on-resistance and rapid state transition, a higher switching frequency of 24 kHz is used to further mitigate the total harmonic distortion (THD) levels in the M2C[11, 52, 55]. Along with improved THD performance, the transistor switching losses decrease resulting in overall improved system efficiency.

The MMC design described here utilizes a GaN HEMT manufactured by Efficient Power Conversion (EPC), the EPC2014c, which results in low conduction and switching losses [56]. This MMC design employs 2 parallel conversion blocks (configured in a vertically stacked arrangement), each consisting of 4 arms with 15 submodules per arm. Table 19 provides the overall design objectives for the converter.

Table 19: Modular Multilevel Converter Design Parameters

Parameter	Numerical Quantity
Input Voltage	225 Volts DC
Output Voltage	240 (±12) Volts AC
Power Output	2 kVA
Minimum Efficiency	>95%
THD	<5%

8.2 CONVERTER SUB-MODULE DESIGN

The M2C converter design offers many unique technical advances, but also presents numerous technological challenges to achieve efficiency in comparison to traditional converter systems. As can be seen in Figure 45, each submodule is interconnected between the top half-bridge lower source, and the bottom half-bridge upper source.

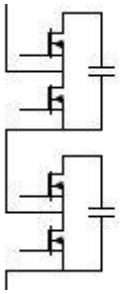


Figure 45: Half-Bridge Submodule Interconnection

When the top transistor is ON (bottom OFF), current passes through the capacitor bank charging the capacitors and building voltage across the converter. When the bottom transistor is on (top off), the system current bypasses the capacitors, in addition to the capacitors discharging. The changing states within an individual submodule alters the voltage potential and current across and through the interconnection. This effectively creates a floating voltage potential

between the bottom and top submodule pins. In a traditional M2C topology, robust IGBTs are used where the gate-source voltage can alter to a considerable degree, however, GaN transistors have very sensitive tolerances. Because of this, the gate drive circuitry must be specifically designed to ensure safety of the switching transistors [56].

8.2.1 Gate Drive Circuit

The M2C topology provides a unique challenge in gate drive design because of the changing voltage within the interconnection between submodules. Transistors have a sensitive, and defined range of V_{GS} that needs to be upheld to ensure proper and reliable operation. As mentioned in Section 4.3, transistors have a required voltage to enable the channel to be fully opened and allow current to pass. For the EPC 2014C, 5 Volts is the required voltage to fully turn the device on; however, the device has a maximum voltage of 6 Volts between the gate and source before device degradation occurs [22, 56]. An isolated gate drive system, similar to that in Section 4.3, was designed to enable transistor switching events while limiting the effects of the floating source of the half-bridge transistors.

An isolated control signal would be required for both transistors, however, it was found that isolated power would also be required. The isolated power is necessary to prevent a feedback loop between the necessary control power, and the output power across the submodules. With both measures of prevention, a theoretical gate drive system was designed for the submodules (Figure 46). This gate drive circuit technique, complete with signal and power isolation, is mimicked from Section 4.3 to provide power for the EPC 2014C transistors. The full design and submodule is discussed in Section 9.1.

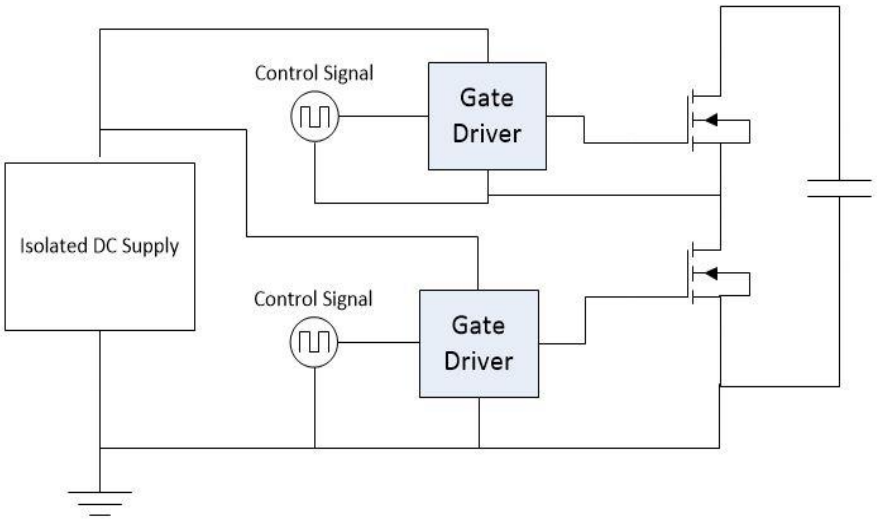


Figure 46: M2C Isolated Gate Drive Topology

9.0 MODULAR MULTILEVEL CONVERTER SUB-MODULE TEST CIRCUIT

To begin hardware development for the single-phase M2C, a single submodule board was designed to evaluate the gate drive circuitry and the layout thermal characteristics. This design was also helpful in demonstrating the theoretical capacitor sizing and layout.

Table 20: Modular Multilevel Converter Design Parameters

Parameter	Numerical Quantity
Submodule Voltage	30 Volts
Submodule Current	7 Amps
Capacitance	$\geq$ 800 μF

9.1 SUB-MODULE PRINTED CIRCUIT BOARD AND EXPERIMENTATION

Using the EPC2014C GaN transistor (specifications including: V_{DS} – 40 V; $R_{DS\,(ON)}$ – 16 mΩ; I_D – 10A), a submodule PCB was designed in Mentor Graphics PADS, as shown in Figure 47. The entire cell layout is 1.685 in. long and 0.325 in. wide and includes full voltage and signal isolation. An ADuM5240ARZ digital isolator from Analog Devices [57] and a LM5113 gate driver from Texas Instruments (TI) [58] are cascaded with the transistors to complete the gate drive circuitry. In addition to providing signal isolation, the Analog Devices digital isolator also includes full voltage isolation through an internal DC/DC converter. The voltage and control

signals are then propagated to the TI gate drive chip which is a half-bridge specific driver that produces internal isolation for the upper transistor through a bootstrap topology to clamp V_{GS} at 5.2 Volts (under the 6 Volt limit) [58]. Lidow, et. al, [22] provided great insight into printed circuit board layout for the EPC 2014C to minimize loop inductance, mitigate inrush current, and decrease overall parasitic effects.

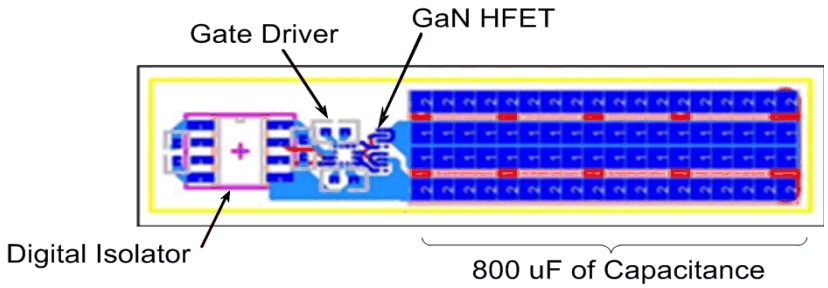


Figure 47: Printed Circuit Board Design for one half-bridge submodule

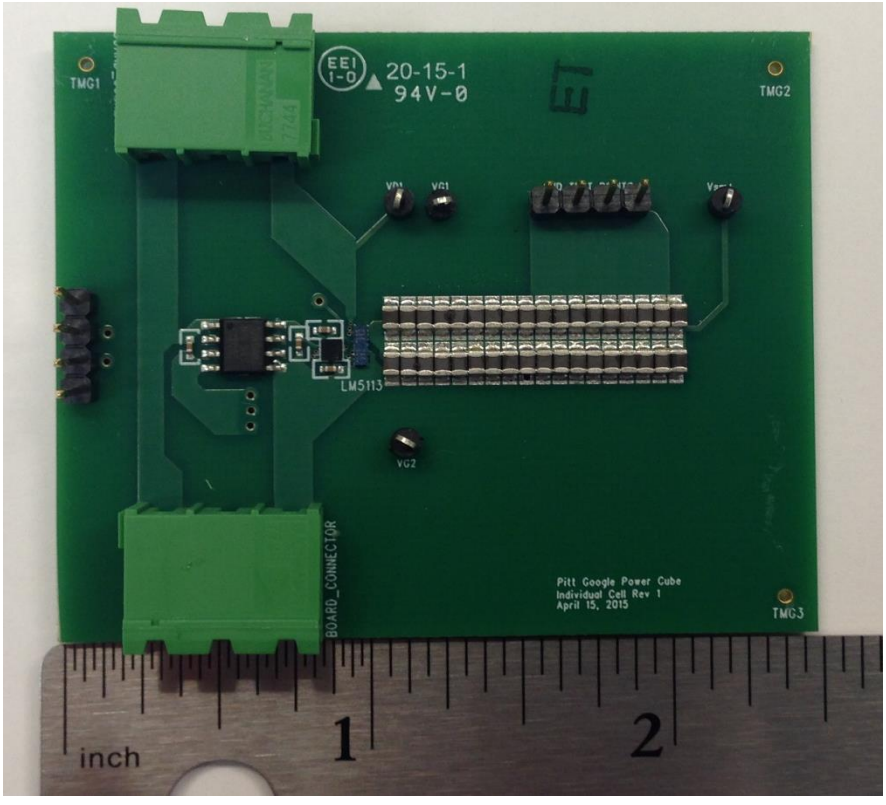


Figure 48: Fabricated M2C Submodule

Figure 48 shows the fabricated submodule based upon Figure 47. The PCB design (solder pads, layer-to-layer vias, and traces) were also exported from PADS Layout and imported into ANSYS Icepak for thermal behavioral modeling of the layout. An Icepak model was used to predict the thermal distribution under operating conditions within the submodule. Expected power loss metrics were assigned to each major electronic component. The power dissipation (conduction plus switching loss) through each GaN transistor was calculated and modeled in software to be 0.032W when switching at 24 kHz. The digital isolator and gate drive chips are expected to dissipate 0.42W and 0.01W, respectively. The module equivalent capacitance and bootstrap capacitors have equivalent series resistant (ESR) values of 8.43mΩ and 0.884Ω, respectively, resulting in dissipation values of 1.63μW and 6.2mW at 24 kHz. ESR is a key variable that represents the dielectric loss, and contact and lead resistances of a capacitor as a resistive component. This is a necessary factor to represent the overall losses from capacitive components. Simulation results of the temperature distribution throughout the compact layout predicted the gate drive chip and transistors to be the most thermally sensitive. The temperatures predicted for the chip and transistors were 51.8 ºC and 50.1 ºC, respectively, as seen in Figure 49.

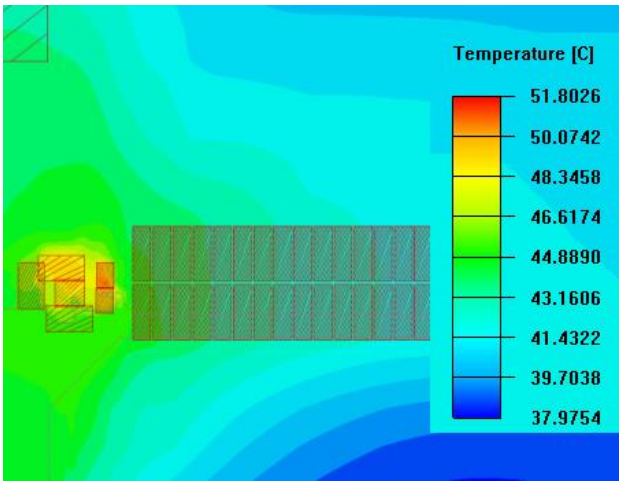


Figure 49: ANSYS Icepak thermal performance simulation results

Experimental tests were conducted to observe the effects of the power flowing through the submodule onto the individual transistor devices, as well as the thermal performance of the submodule. Two 24 kHz square waves, with 180˚ phase shift, were applied to the gate circuitry and 20 Volts across the whole submodule. Electrical waveforms of the turn on and turn off characteristics of both the upper and lower transistors are showing in Figure 50 and Figure 51.

Figure 50: Measured Turn ON (OFF) Characteristics of Upper (Lower) Transistors

Figure 51: Measured Turn OFF (ON) Characteristic of Upper (Lower) Transistors

When the upper submodule transistor turns on (bottom off), the capacitors are switched into the submodule system and produce a strong transient effect across the top transistor as seen in Figure 50. The isolation provided from the gate drive chip on the top transistor minimizes this transient such that the device can operate safely. When the lower transistor is on (upper off), the transient effects are much smaller as seen in Figure 51. It is thought that this is because there is no capacitance in the circuit, and the digital isolator is providing appropriate isolated grounding. Overall, the turn on/off characteristics provide insight that the gate drive circuitry does operate under safe parameters (<6 Volts gate-source), with the pseudo-grounded bottom transistor source.

Figure 52: Thermal image of the submodule performance

Using a FLIR thermal imaging camera, the temperatures recorded on the gate drive chip and transistors were recorded as 53.4 ^{o}C and 52.2 ^{o}C, respectively **(**Figure 52**)**. These values show a strong correlation between the simulated **(**Figure 49**)** and experimental results. With this validation of the model, simulations of operation at rated power in open air were performed; and temperatures were shown to rise to approximately 70^{o}C in the transistors and gate drive chip. This is well within thermal limits of the LM5113, EPC2014C, and typical GaN HEMT devices

[11, 22, 51, 56, 59]. The simulated and experimental results have been used to design a heatsink system (not included in this thesis) for the full power board networks.

10.0 MODULAR MULTILEVEL CONVERTER POWER BOARD

Having observed that the submodule circuit operates as expected, a full "power board" was designed to replicate one arm of the M2C topology. This arm consists of 14 submodule units in series designed onto one printed circuit board.

10.1 M2C POWER BOARD PRINTED CIRCUIT BOARD DESIGN

Having designed a working gate driver circuit to prove the working submodule, a printed circuit board with 14 interconnected submodules was designed. A number of challenges presented themselves through this design process. These included: regulation of maximum current through the transistors; elimination of current pathing between the interconnected submodules; incorporation of satisfactory capacitance to provide a clean waveform; and connections and isolation of communication signals from power busses.

A few modifications were made to the original submodule circuitry to provide more efficient and cooler operation as seen in Figure 53. The Digital Isolator was modified from the ADuM5240ARZ to the ADuM5210ARSZ. This change was instituted because the 5210 chip provides signal isolation for up to two signal channels [60] instead of the one that the 5240 chip offered [57]. In addition, the 5210 provides better thermal and electrical efficiency compared to the 5240, while maintaining the same overall functionality (isolated output voltage, isolated

control signal). Using the 5210 added significant physical size to this portion of the gate drive circuitry; however, this did not incur any overall system modifications because the height of the capacitor bank was comparable.

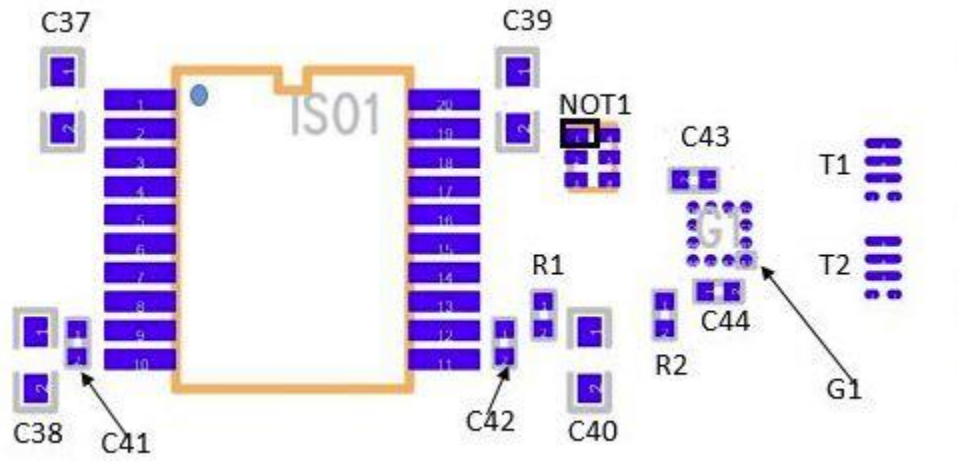
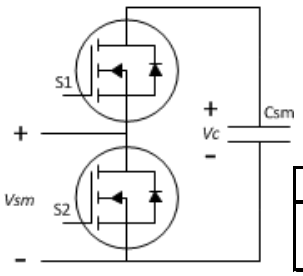


Figure 53: Updated Gate Drive circuitry with Digital Isolator (ISO1), inverter (NOT1), gate driver (G1), and transistors (T1 &T2)

Because of limitations of modern microcontrollers, it was found that each submodule would only have access to one input control signal. Each submodules would only ever have one transistor on at a given time, specifically meaning when a control signal is high on the top transistor, it would be low on the bottom, as seen in Figure 54. This offers a unique opportunity to use a digital inverting chip, seen as NOT1 in Figure 53, such that only one signal is needed as an input but two signals are generated and sent to the TI gate driver. The gate driver was held consistent between iterations as it provided sufficient charge to turn the transistors on/off; and it included a fixed ground state for the upper transistor source terminal.



State	S1	S2	Vsm
0	ON	OFF	Vc
1	OFF	ON	0

Figure 54: Submodule Half-Bridge (left), Submodule Switch States (right)

To determine the impact of submodule cell capacitance on the system total harmonic distortion (THD), a sensitivity analysis was performed in which the capacitance was varied from 200uF to 1 mF, in 200 µF steps. The voltage ripple on the capacitors, as well as the impact on the output THD, were simulated by Barchowsky in [61]; the results were plotted as can be seen in Figure 55, respectively. With physical size and the upper limit of 40 V_{DS} across the EPC2014C, the ideal submodule capacitance was found to be between 600 µF and 800 µF. Using 36, 0805 ceramic capacitors, 800µF of capacitance was implemented in the original submodule design.

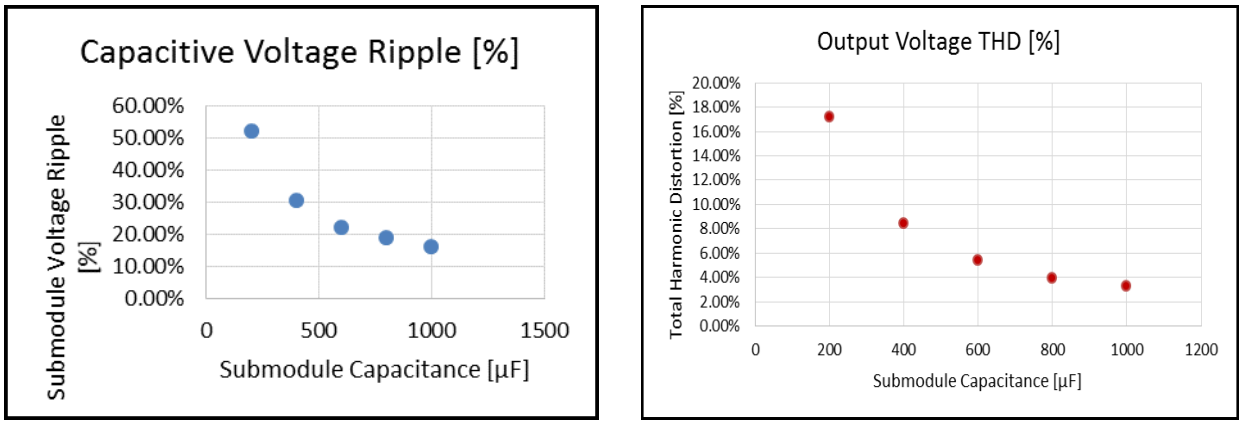


Figure 55: Submodule capacitance on Submodule Voltage Ripple (left) and Submodule Capacitance on Output Voltage THD (right)

Observing the three dimensional structure while stacking the submodules (discussed in detail below) a minor air gap was discovered where additional capacitance could be installed. A daughter PCB was designed to nearly double the overall submodule capacitance to utilize this

empty space, and increase the overall system performance. As can be seen in Figure 56, connectors were added to the side of the submodule design to bridge the two sets of capacitor banks. Thus, the overall submodule capacitance was ultimately designed to be 1.55mF.

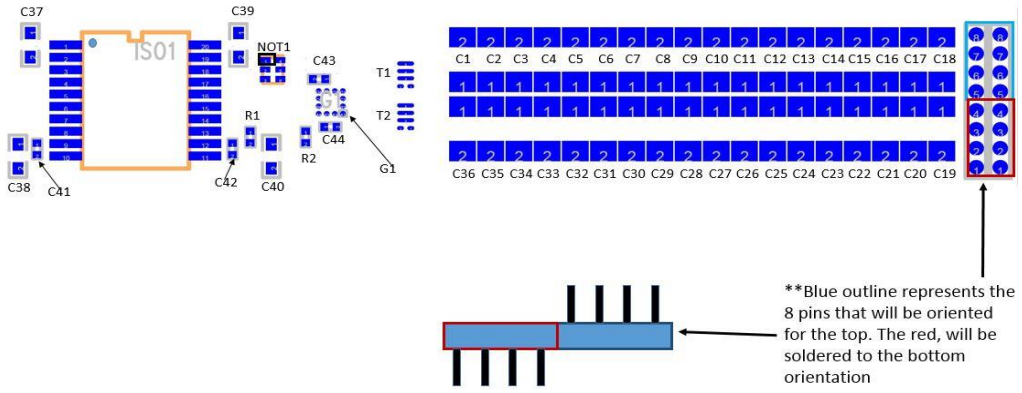


Figure 56: M2C Full Power Board Submodule with added standoffs for daughter capacitor boards

The final major PCB design constraints included limiting the gate loop inductance, and providing appropriate current load paths to the transistors and between the submodule interconnections. Multiple design options are presented in [22, 62] and "dual sided termination PCB layout" technique was chosen for this application and extensively described in [56]. This design was ultimately chosen because it offers the safest operation of current handling, while minimizing the gate loop inductance. Gate loop inductance can pose numerous problems by introducing transient events into the transistor control signal [47, 62]. With such sensitive devices, as discussed in Section 9.1, additional stresses to the EPC devices could cause device and ultimately system failure.

The path interconnecting the two submodules is required to handle up to 9 Amps continuously. With such a power dense design, this interconnection required special design parameters to handle the required current. Advanced Circuits PCB manufacturing tool provided

insight into calculating required trace widths for set copper plating, change in temperature, and trace length [41]. Equations 10.0 -1 and 10.0 -2 were used to derive the width required for the traces.

$$A = \frac{I}{(k\Delta T)^{1/c}} \qquad (10.0\text{ -1})$$

$$W = \frac{A}{(1.378 * \Delta T^{\frac{1}{b}})^{\frac{1}{c}}} \qquad (10.0\text{ -2})$$

A is the area of the trace, W is the width, I is the current through the path, ΔT is the temperature rise when current is flowing through the trace; k, b, and c are constants defined by the PCB fabrication material. To design for worst case scenarios, the trace width was designed such that either layer could handle the current independently. Table 21 shows the values used for the calculation, and required trace with for inner and external layered traces.

Table 21: Parameters to solve for interconnection trace width

Parameter	Value	Parameter	Value
Thickness	1 oz/ft^2	Trace Length	128 mil
I	9 Amps	k (internal) [external]	(0.024) [0.048]
ΔT	75 ˚C	b	0.44
$T_{ambient}$	25 ˚C	c	0.725

$$W(external) = 72.1mil$$
$$W(\text{int}ernal) = 188mil$$

Using the parameters in Table 21, the following results were found and implemented as seen in Figure 57. In addition, Figure 57 shows the two layers (one external and one internal) that

were used to help distribute the current pathway. The “pink” layer is the second layer of the 6 layer board which is connected through vias to the top copper layer (blue). The implementation of vias to mitigate drain and source currents for the transistors as discussed above can be seen in Figure 57.

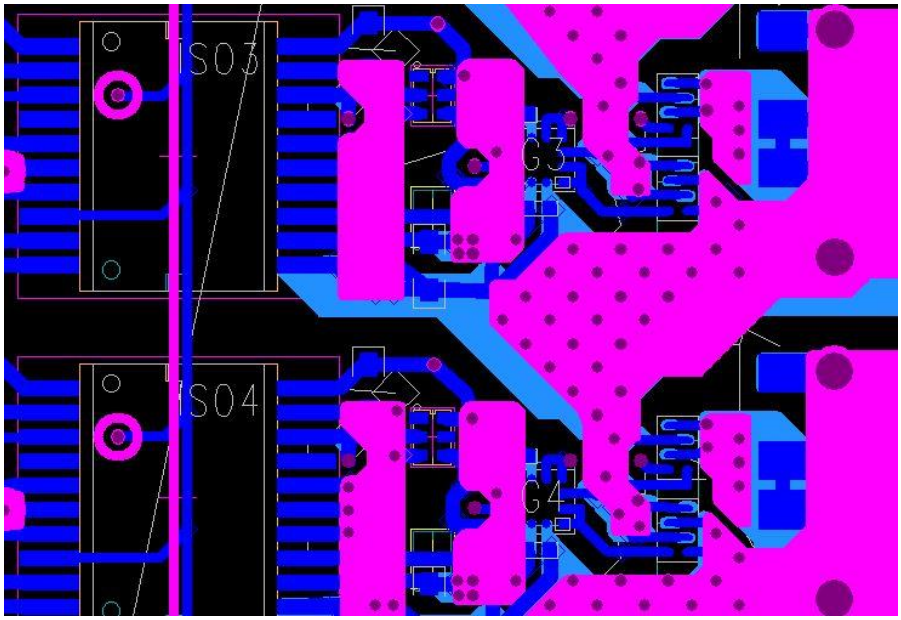


Figure 57: PCB Interconnection of multi-layered traces

The designed and fabricated PCBs are found in Figure 58 and Figure 59. The finalized design is 2.9 in. x 2.5 in. for a single arm of the M2C. Four of these single arm power boards are needed to construct the M2C converter, in addition to a centralized control and power board that house a micro-controller, 3.3 Volt and 5 Volt power supplies, and externally connecting input and output terminals. The projected volume of the converter is 20 in^3, resulting in a power density of 100 W/in^3. Initial test results providing validation for the boards and design are provided in Section 10.2.

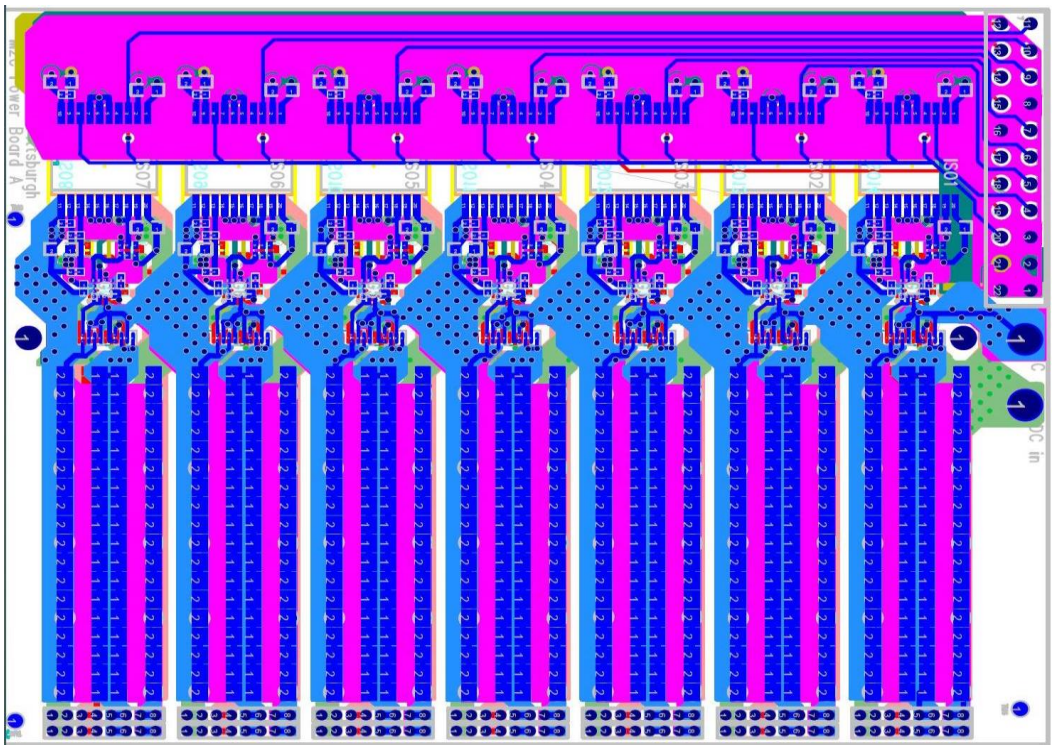


Figure 58: Designed single M2C arm PCB

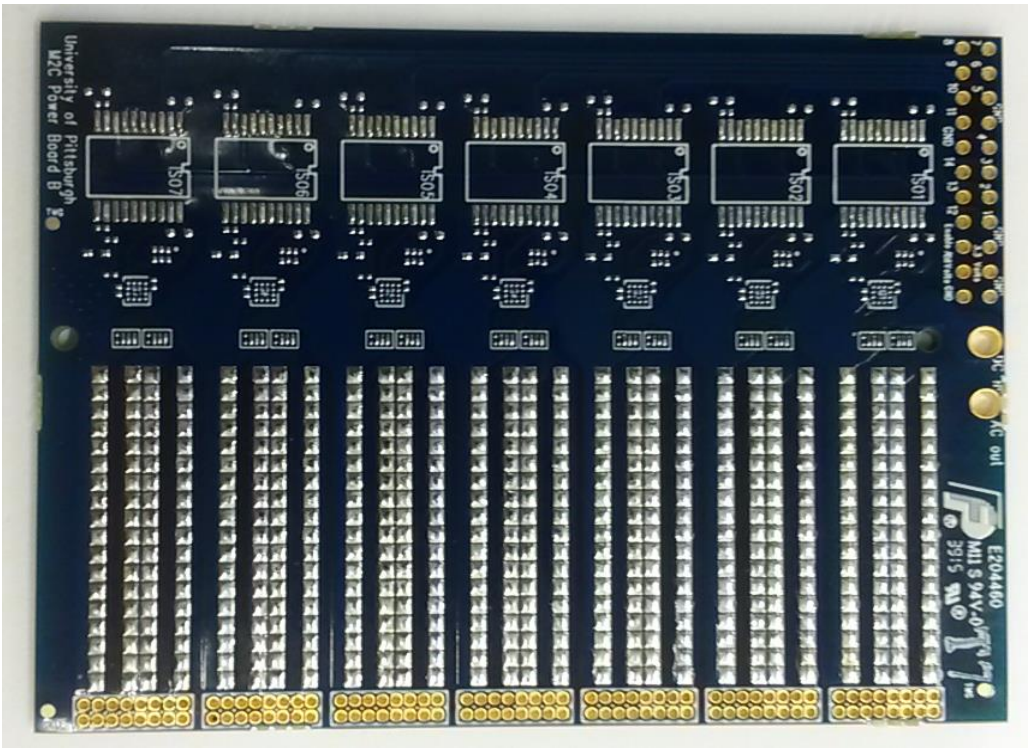


Figure 59: Fabricated single M2C arm PCB

10.2 PCB TESTING

TMG Manufacturing Inc. was responsible for populating the single M2C arm PCBs as seen in Figure 60. The design included very small components and so precise technology was necessary to place the components. The components were placed and fed through reflow ovens to solder the surface mount components onto the board. Through hole components and the daughter capacitor boards were then soldered manually. TMG provided quality assurance testing of the component connections to ensure appropriate connectivity between devices and the solder pads. They also performed x-ray tests to observe if any short circuits were created while applying solder paste to the surface mount, and specifically the ball grid array components. An example of an x-ray image of the gate driver chip and transistors can be seen in Figure 61.

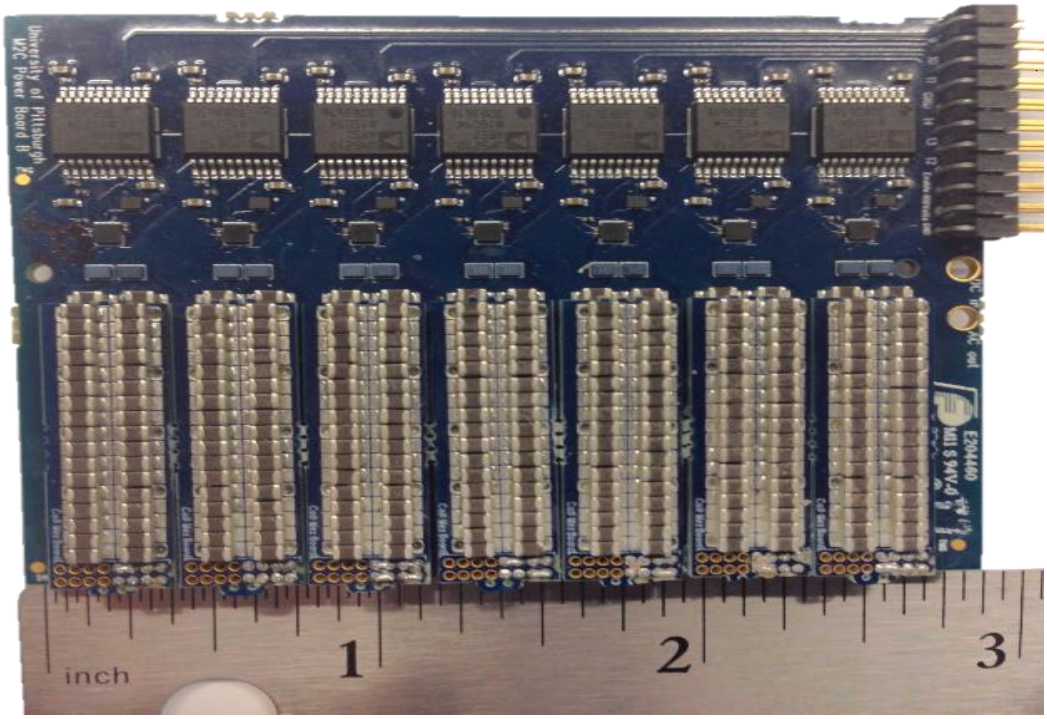


Figure 60: Fabricated and populated PCB

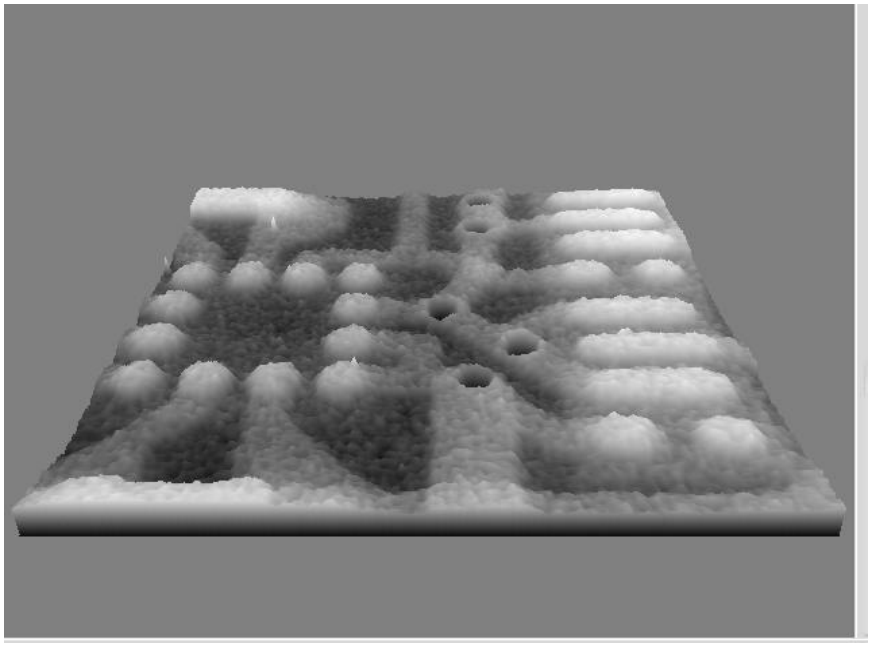


Figure 61: X-Ray image of gate driver chip and GaN transistors

Preliminary testing will include the testing of eight submodules (two per power board). Complementary pairs of submodules on diagonal power boards, will have connected input control signals, as seen in Figure 62. The purpose is to test two forms of functionality. The first is the functionality of the modified submodule design, which contains only one incoming gate control signal, and a different isolation chip from that in Section 8.2.1. The second, is the functionality of the overall power board design. While the power board design does meet theoretical constraints, it is unclear how the current will disperse through the submodule, interconnected pathways. Non-ideal current flow could cause increased stresses through one path, adding additional stresses to the transistors and other submodule components. Final M2C arm testing will be completed once the gate control algorithms are finalized, and implemented by other members of this project team.

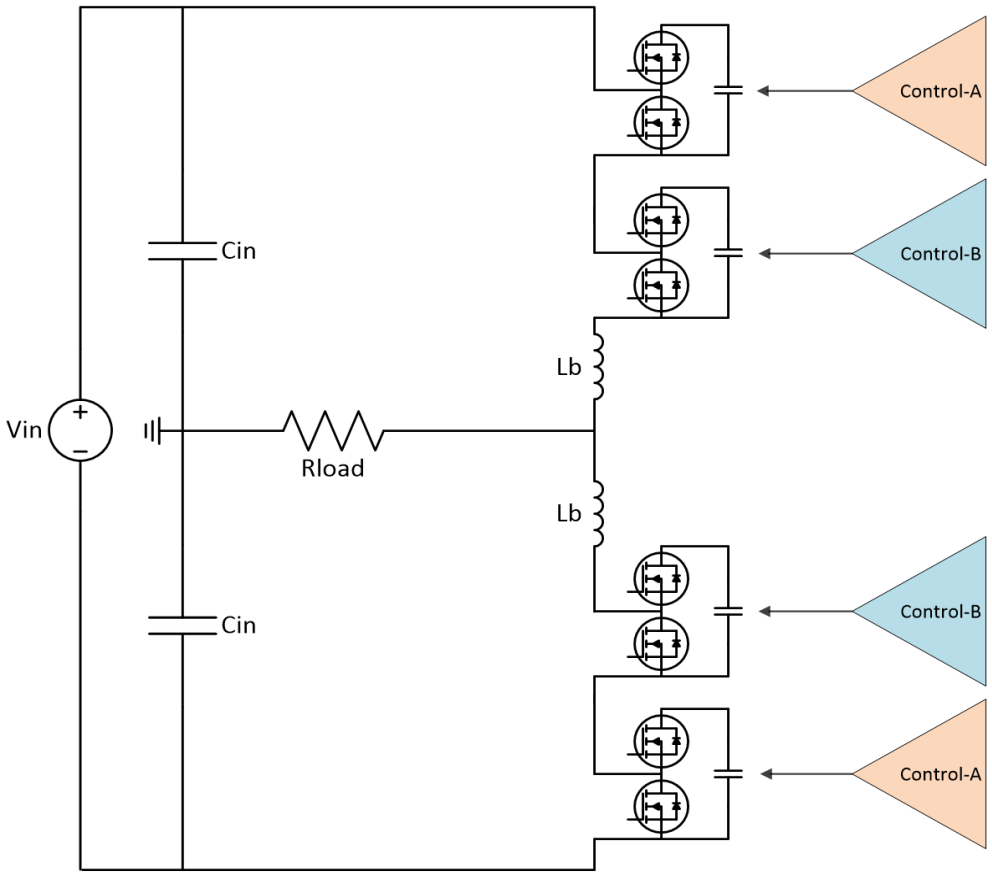


Figure 62: M2C power board test configuration

11.0 SUMMARY

The objective of this thesis was to investigate the electro-thermal effects of different power transistors on power converter performance. This was accomplished through simulation and experimental measurements of a Si IGBT and SiC MOSFET electrical and thermal behavior in a dc/dc boost converter, as well as the integration of GaN HEMTs in a modular multilevel converter. In Chapter 3.0 , equivalent device behavioral models for a Powerex SiC MOSFET and Powerex Si IGBT were developed in SaberRD. These models included device specific details, and were validated against published manufacturer datasheets.

A dc/dc boost converter topology was designed in Chapter 4.0 to provide a platform to test the Si IGBT and SiC MOSFET models in simulation and experimentation. The converter system components (inductor, output capacitor, and resistor) were derived such that the converter operated in the continuous conduction mode. Upon finalizing component values, simulations in SaberRD with the designed device models were conducted. The simulations swept the transistor switching frequency, and produced electrical efficiency estimations. Finally, upon designing the boost converter, an appropriate gate drive circuitry was designed to properly operate both the SiC MOSFET and Si IGBT [39].

The designed and simulated converter was physically constructed, as explained in Chapter 5.0. The converter was then tested using both the SiC MOSFET and Si IGBT as primary switching devices. Each test was conducted for 10 minutes, such that a thermal equilibrium was reached

between the transistor baseplate and junction. The switching frequency was swept for multiple input current/voltage ratings derived from modern converter applications [13, 14, 32]. The system electrical efficiency was calculated through measured currents and voltages. These electrical results showed there is an optimal switching frequency, at least at low voltage operation, for both of the transistor devices. The experimental results were compared to the simulated results, and discussed in Section 7.1.

Thermal modeling and experimentation was performed on both the gate driver circuitry as well as the SiC MOSFET. The gate driver was modeled in ANSYS Icepak to simulate any added stresses the driver circuit could provide to the switching transistor. A FLIR thermal imaging camera was used to experimentally measure the temperature of the gate driver circuitry, and these results validated the developed finite element analysis model. The rise in temperature of the SiC MOSFET was mathematically modeled in Chapter 6.0 . The relationship between transistor conduction and switching losses was related to thermal losses. The switching frequency was used as the independent variable, to predict the change in temperature of the MOSFET junction. The predicted results are compared to measured results in Section 7.2.

It can be concluded that there is a strong relationship between the electrical and thermal performance of the two devices from the modeled, simulated, and measured results. While an optimized electrical efficiency was related to a specific switching frequency, it was found that the thermal limitations can limit the transistor performance at the same frequency. And so, the electrical and thermal modeling techniques are critical tools in the development of modern power electronic systems. More specifically, it was shown that eq. 6.0 -1 can be extended as a predictive tool for the electrical and thermal behavior of the SiC MOSFET in power switching circuits where the switching frequency was varied.

Techniques similar to those for the SiC MOSFET and Si IGBT were used to integrate GaN HEMT into a high, power dense, M2C. While M2C topologies have been demonstrated in the past, the integration of small GaN HEMT devices was novel. With sensitive gate-source characteristics, the design of the gate drive circuity proved to be a critical design challenge. Chapter 8.0 explains the overall M2C topology, and the challenges associated with isolating communication, and power signals to the inter-connected half bridge submodules. Thermal modeling in ANSYS Icepak was conducted on individual submodules to observe the heating effects of the dense design. Fabricated PCBs were populated and tested to validate the thermal models, in addition to the electrical functionality of the submodule design. Fourteen submodules were then interconnected to form one power-arm of the M2C topology, and designed onto one, double sided, 6-layer, PCB. This power board PCB was designed and fabricated with the help of industry partners, and is currently ongoing electrical functionality tests.

Overall, the work in this thesis explored the integration of SiC and GaN power transistors in power electronic systems. It was shown that while highly-efficient electrical performance is desired, thermal limitations are a key design parameter for future, power-dense converter designs; and that utilization of simple mathematical models coupling electrical and thermal behavior, may be sufficient for designing converters with optimal levels of thermal management.

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