UNIVERSITI PUTRA MALAYSIA

DESIGN OF 8-BIT CMOS DIGITAL TO ANALOG CONVERTER

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Chairman : Dr. Bambang Surnayo Suparjo

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Digital to analog converter (DAC) is the main link between the digital and analog signal in the world of signal processing. High-speed DAC has been used widely as the data converter in video, radar and communication application. This project presents a high-speed current switching CMOS digital analog converter (DAC) that achieves 8-bit resolution with good differential non-linearity (DNL). The use of current switching creates a potential for speed improvement because current can be switch in and out of a circuit faster than the voltage. This converter is based on current division by using segmentation technique.

In this approach, low DNL and glitch energy can be achieved by segmenting the two or three most significant bits of the DAC with an array of equal current sources rather than a binary array of current sources. This proposed segmented DAC employs two internal DACs that have its own advantages. The first internal DAC is used for the

upper 3-bits MSBs. It is implemented by using equal current sources 0.25mA, with the incoming 3-bits MSBs converted to 7 control lines by the thermometer decoder, which will enable the 7-switched current cells. Thermometer decoder ensures good differential linearity for the DAC. The remaining 5 LSB bits of the converter will be controlled by the second internal DAC that use the R2R network to binary weight the 0.25mA current source.

The circuit of the DAC is designed by dividing into modules. The modules include thermometer decoder, latch, 5-bit LSB inverted R-2R ladder, 3-bit MSB current source, two-way CMOS current switch and the current to voltage converter. This circuit is simulated by using Tanner Tools Pro software, where the SCNA20um CMOS process with level-2 transistor parameters is used. The simulation results of the designed DAC shows a conversion rate of 7.2Mhz, a INL of ±1.36 LSB, a DNL of ±0.05 LSB and a glitch energy of 30pVs with the power supply of ± 5V. The reduced differential non-linearity (DNL) is achieved by utilizing the proposed technique.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Master Sains

REKABENTUK CMOS 8-BIT PENUKAR DIGIT KE ANALOG

Oleh

TAN GIM HENG

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Penukar digit ke analog (DAC) menjadi penjaling utama di antara digit dan analog dalam dunia pemprosesan isyarat. DAC yang berkelajuan tinggi semakin meluas digunakan sebagai penukar data dalam peggunaan video, radar dan alat komunikasi. Projek ini menyampaikan satu CMOS penukar digit ke analog (DAC) yang berkelajuan tinggi secara pensuisan arus yang boleh mencapai resolusi 8-bit dengan DNL yang baik. Penggunaan pensuisan arus mewujudkan satu keupayaan untuk mempertingkatkan kelajuan kerana arus boleh dialir dengan kadar lebih laju daripada kadar voltan berubah. Penukar ini adalah berdasarkan pembahagian arus dengan menggunakan teknik peruasan.

Dengan menggunakan pendekatan ini, DNL dan tenaga "glitch" yang rendah boleh dicapai dengan meruas dua atau tiga bit MSB DAC dengan satu susunan sumber arus yang bernilai sama daripada ke satu susunan arus yang bernilai secara binari. Peruasan DAC yang dicadangkan adalah dengan menggunakan dua DAC dalaman yang

menpunyai kebaikan tersendirinya. DAC dalaman yang pertama digunakan untuk 3-Bit MSB yang paling atas. Ia diimplementasi dengan menggunakan sumber arus 0.25mA, dengan 3 bit yang masuk akan ditukar kepada tujuh baris kawalan dengan menggunakan pengekod termometer di mana ia akan mengawal tujuh suis sel arus. Pengekod termometer memastikan pembezaan tidak sejajar yang baik untuk DAC. 5 bit LSB yang seterusnya daripada penukar akan dikawal oleh DAC dalaman yang kedua dengan menggunakan rangkaian R2R yang membahagi sumber arus 0.25mA secara binari.

Litar DAC ini direkabentuk dengan dibahagikan kepada beberapa modul. Modul-modul ini termasuklah pengekod termometer, "latch", 5-bit LSB penyongsang rangkaian R2R, 3-bit MSB sumber arus, suis arus CMOS berhala dua dan penukar arus ke voltan. Litar ini disimulasi dengan menggunakan perisian Tanner Tool Pro, di mana CMOS proses SCNA20um dengan transistor peringkat-2 digunakan. Keputusan simulasi daripada DAC yang telah direkabentuk menunjukkan kadar penukaran 7.2 MHz, INL ± 1.36 LSB, DNL ± 0.05 LSB dan tenaga "glitch" 30pVs dengan menggunakan sumber voltan ± 5V. Pengurangan DNL boleh dicapai dengan menggunakan teknik yang dicadangkan.

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I certify that an Examination Committee met on 17th July 2001 to conduct the final examination of Tan Gim Heng on his Masterof Science thesis entitled "Design of 8-Bit CMOS Digital to Analog Converter" in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 11980 and Universiti Pertanian Malaysia (Higher Degree) Regulation 1981. The committee recommends that the candidate be awarded the relevant degree. Members of the Examination Committees are as follows:

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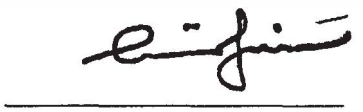

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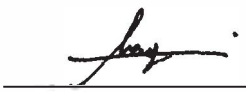
DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations, which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.



(TAN GIM HENG)

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LIST OF ABBREVIATIONS

ADC	Analog To Digital Converter
C	Capacitance
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital To Analog Converter
DNL	Differential Non-Linearity
Gnd	Ground
IC	Integrated Circuit
INL	Integral Non-Linearity.
K_n	NMOS Transconductance coefficient
K_p	PMOS Transconductance coefficient
L	Channel Length
LSB	Least Significant Bit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NMOS	n-channel Metal Oxide Semiconductor
PMOS	p-channel Metal Oxide Semiconductor
SPICE	Simulation Program with Integrated Circuit Emphasis
V_{dd}	Supply voltage
VLSI	Very Large Integrated Scale
V_R	Voltage Reference
W	Channel Width

CHAPTER 1

INTRODUCTION

Integrated Circuit

A collection of one or more gates fabricated on a single chip is called an integrated circuit (IC). IC chip may contain hundreds of diodes, transistors, resistors and capacitors. The conducting path that interconnects the components of an integrated circuit are contained entirely within the device and only leads are brought out for power supply connection, ground, circuit inputs and outputs. Integrated circuits have three advantages over digital circuit built from discrete components.

- Size – ICs are much smaller compare to discrete components. The transistors and wires are shrunk to micrometer sizes, compare to the millimeter or centimeter scales of discrete components. Small size of chip has the advantage of high-speed and less power consumption, since smaller components have smaller parasitic resistance, capacitance and inductance.
- Speed – The signals to be transmitted are much faster within a chip than they can between chips. Communication within a chip can be hundreds of times faster than the communication between chips on a printed circuit board. This is due to the wires have smaller parasitic capacitance to slow down the signals.
- Power consumption – Operation of the circuits within a chip consumes less power. This is because of the smaller parasitic capacitances and resistances, which require less power.

CMOS Technology

CMOS technology has steadily moved to occupy a central position in modern electronic design and wisely used in majority of leading-edged commercial application. It has rapidly embraced the field of analog integrated circuits, providing low cost and high performance. CMOS processes have emerged as viable choice for today's complex mixed signal system. With the channel length continue to scale down, CMOS technology will probably continue to serve circuit design for another decade. At the present, CMOS technology is more suitable for combining analog and digital technique. The low cost of fabrication and the possibility of placing both digital and analog circuits on the same chip to improve the overall performance has made CMOS technology to become very attractive.

Data Converter

Rapid development in microelectronic, particularly in VLSI (Very Large Integrated Scale) have brought about major shift in the techniques of handling, processing, transmission, measurement, control and display of electrical signal such as from digital to analog. However, both analog and digital techniques need to work in conjunction with these application areas. Therefore, it needs to have data converter, analog to digital converter (ADC) and digital to analog converter (DAC) to convert electrical signal from analog to digital and digital to analog.

What is DAC?

A DAC is a device that converts a digital input signal to an analog output voltage or current that is proportional to the digital signal. The digital information is in the form of a binary number with some fixed number of digits. DAC converter provides the interface between the analog signal domain and the binary digital computational domain. The results of the computational and decision-making digital equipment are converted by DAC to drive an analog actuator such as heating element, motor, speaker, or video display.

The principal relationship between the digital input and the analog output of a DAC is proportional as shown in equation 1.1

$$V_o = V_R (b_1 2^{-1} + b_2 2^{-2} + \ldots..+b_n 2^{-n}) \qquad (1.1)$$

Where V_R is the reference voltage of the DAC, and the coefficients b_1 (MSB) through b_n (LSB) are equal to 0 if a bit is off, and equal to 1 if a bit is on.

DAC Characteristics

For modern application, most DAC are integrated circuit (IC) assemblies, viewed as a black box having certain inputs and outputs characteristic. Figure 1.1 shows the important elements of a DAC.

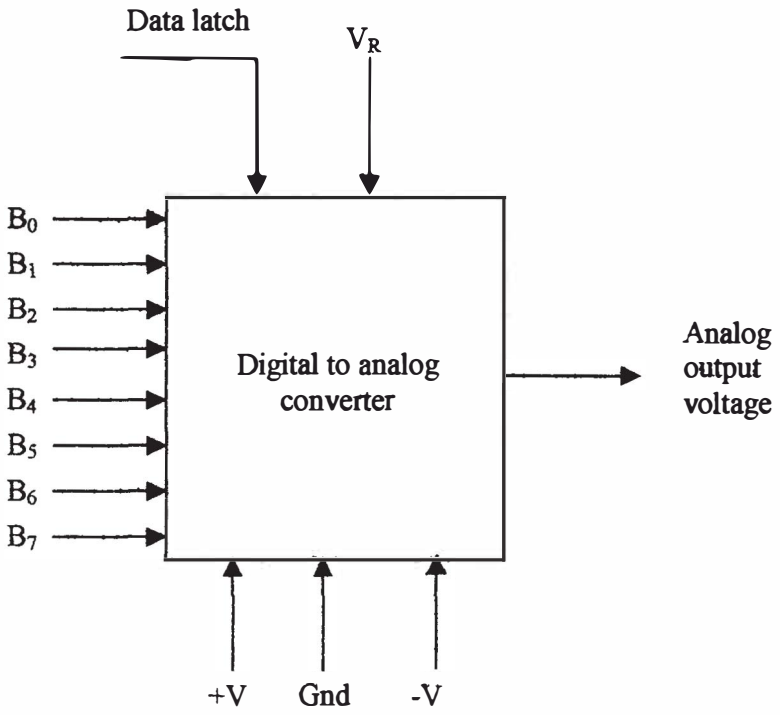

Figure 1.1: An 8-bit DAC diagram showing typical input and output.

The associated characteristic can be summarized by reference to this figure 1.1.

1. Digital input – Typically, a parallel binary word of a number of bits specified by the device specification sheet. Voltage levels and current drive capabilities corresponding to 0 and 1 states of the digital code are based on the logic family associated with the DAC. At the present state-of-the art, CMOS technology is the most popular and it has to be taken into account in the design of DAC.
2. Power supply – This is bipolar at a level of ± 5 as required for the internal amplifier. Power supply for analog and digital hardware in the DAC are

generally maintained separate and both of them are well regulated. Grounding is another important factor in DAC performance and it is common to have separate ground connection for digital and analog section. All the grounds have to be at true zero potential with respect to all inputs and outputs signals of the DAC.

3. Reference supply – Required to establish the range of output and resolution of the converter. This must be a stable, low ripple source.
4. Analog output – A voltage representing the digital input. This voltage changes in steps as the digital input changes by bits, with step determined by the equation (1.1). DAC output is in the form of voltage or current. In some cases, the conversion process in the DAC may directly produce a current output that is fast, linear and free from any offset. A built-in op-amp can be used to convert the output current to voltage.
5. Data latch - Many DAC have a data latch built into their inputs. When a logic command is given to latch data, whatever data are on the input bus will be latched into DAC and the analog output will updated for that input data. The output will stay at that value until new digital data are latched into the input.

Data Converter Specification

DAC is specified by a number of characteristic parameters, as summarized below. A clear understanding of these parameters is essential to enable the use of DAC in practical application in more effective manner.

1. Resolution – The resolution of a converter is a measure of the smallest basic increment the analog component can be divided. Resolution is not necessarily an indication of the accuracy of the converter, but instead it usually refers to the number of digital input bits.
2. Absolute accuracy – it is defined to be the difference between the expected and actual transfer responses. More typically accuracy is controlled by specifying offset error, gain error, integral, and differential linearity.
3. Relative accuracy – It is also referred as integral non-linearity (INL). It is defined as the deviation from an ideal transfer function of the converter after the offset and gain errors have been removed. It is largely a function of the non-linearity of the converter.
4. Differential non-linearity error (DNL) – It is defined as the deviation from one LSB analog difference between the outputs for any two adjacent code inputs. It is usually specified in term of a fractional part of one LSB. For perfectly linear, ideal converter, the differential linearity is zero, as all steps are one LSB. For a step of 1.5 LSB, the differential linearity would be ± 0.5 LSB.
5. Monotonic – A monotonic DAC is one in which the output always increases (remain the same) for an increasing digital input. This is made possible by minimizing the errors in the weighting components and the switches used in the DAC. In an analog digital converter (ADC), monotonic behavior of the internal DAC is necessary to ensure that no digital output codes will be mixed. Figure 1.2 shows the non-monotonic behavior of the DAC.

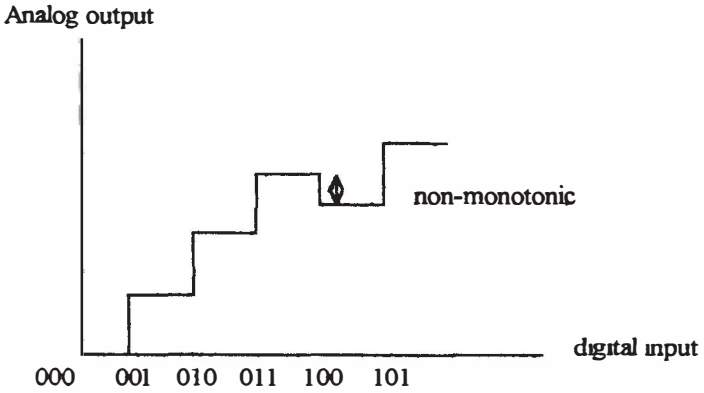

Figure 1.2: Non-monotonic DAC

6. Offset error – the deviation of the output from 0V when the digital input at that code should result in zero output.
7. Gain error – gain error is the error in slope of the DAC transfer function. The gain error is also not always specified, especially if an external reference and output amplifier are added to complete the full DAC. The gain would be adjusted by the added trim circuitry.
8. Settling time – is defined as the time for the converter to settle within some specified amount of the final value (usually ±0.5 LSB). Figure 1.3 shows the settling time of the DAC.

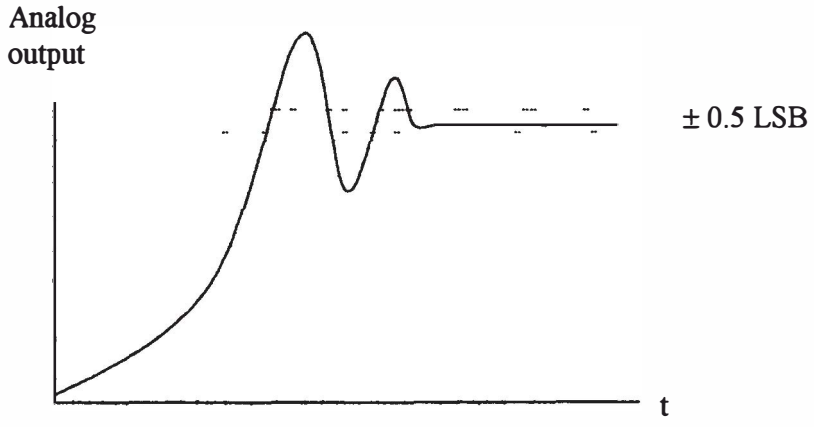

Figure 1.3: The settling time of the DAC

9. Slew rate – This refer to the rate of change of output voltage of the DAC and is governed by its circuit design. High slew rate is usually desired for the DAC, as it also reduces the conversion time.
10. Glitch – Glitch impulse error is an undesired amplitude overshoot (or undershoot) occurs at the analog output when the digital input number is changed from one value to another. They are transient in nature and are due to the difference in switching time of the DAC analog switches and timing skew and feed through of digital signal. Glitch is most troublesome in DAC where the output data is used continuously. One example is computer driven CRT display, where glitches show up as ragged character. Figure 1.4 shows the glitch during transition time from 001 to 110.

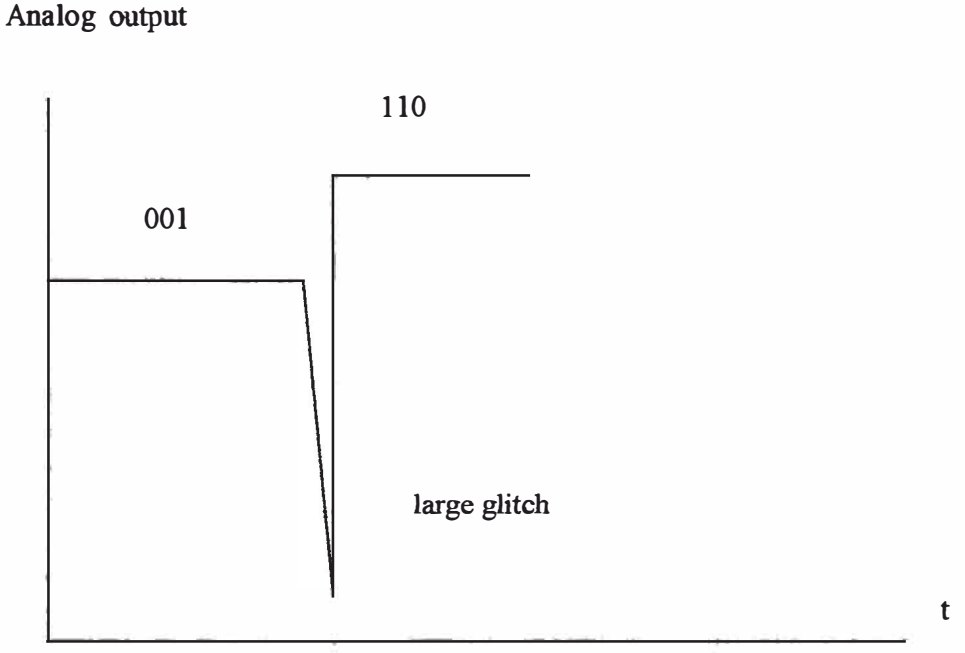

Figure 1.4: Glitch occur during transition from 001 to 110

Objectives of This Work

The objective of this project is to design a high-speed current switching CMOS digital analog converter (DAC) that achieves 8-bit resolution with good differential non-linearity (DNL), monotonic and low glitch energy. This converter is based on current division by using segmentation technique.

The proposed segmented DAC employs two internal DACs that have its own advantages. The upper 3-bit MSBs are implemented by using thermometer decoder, which will be converted to 7 control lines that connected to an array of equal current sources. Thermometer decoder ensures good differential linearity for the DAC. The remaining 5 LSB bits of the converter will control by the R2R network to binary weight the 0.25mA current source. The reduced differential non-linearity (DNL) and low glitch energy are achieved by utilizing the proposed technique