View metadata, citation and similar papers at core.ac.uk
brought to you by CORE
provided by Universiti Putra Malaysia Institutional Repository

UNIVERSITI PUTRA MALAYSIA

FAILURE ANALYSIS INVESTIGATION ON 2N7002LTI TMOS DEVICE DUE TO ELECTROSTATIC DISCHARGE(ESD) FAILURES

ABDUL HALIM ABDUL MANAF

FK 1998 5

FAILURE ANALYSIS INVESTIGATION ON 2N7002LT1 TMOS DEVICE DUE TO ELECTROSTATIC DISCHARGE(ESD) FAILURES

By

ABDUL HALIM ABDUL MANAF

Thesis Submitted in Partial Fulfilment of the Requirements for
the Degree of Master of Science in the Faculty of Engineering,
Universiti Putra Malaysia.

April 1998

Dedications:

This thesis is dedicated to my parents;

Abdul Manaf Hj Abdul Rahman

Zawiah Hj Yaacob

and my wife;

Aniqah Hashim

ACKNOWLEDGEMENTS

I would like to express my sincere and deepest gratitude to the Supervisory committee - Associate Professor Ir. Dr. Shahnor Basri (Chairman), Dr. Prithvi Raj Arora of Aerospace Engineering Department, Faculty of Engineering, Universiti Putra Malaysia, Dr. Abdel Magid Hamouda of Mechanical Manufacturing Department, Faculty of Engineering, Universiti Putra Malaysia, and Mr. Khairir Khalil of Motorola Seremban for their helpful advice, encouragement, constructive criticisms and time throughout the duration of the study.

I express my sincere appreciation to the staff of the Opto Signal Product Division Electrical Overstress Customer Quality Team (OSPD EOS CQT) of Motorola Seremban for discussions and constructive suggestions on the 2N7002LT1 TMOS device to make this project successful. The team members are Mr. Albert Loh (Product Manager), Mr. KY Lee (Product Engineer), Mr. HM Tan (Product Engineer), Mr. Mohd Nazri Baharudin (Process Engineer), Mr. KC Lim (Test Engineer), Mr. KC Lee (Test Engineer) and Mr. YM Lee (Test Engineer).

I thank you Mr. Mike Cairnes (Product Analysis Manager) and Mr. Joseph Disilvestro (Product Analysis Engineer) of Product Analysis Laboratory, Motorola Phoenix, USA. for their timely help and valuable discussions in failure analysis theory and methodology and feedback on the analysis of failed devices.

I thank to Mr. Abul Khair Yahya (Failure Analysis Manager, Motorola Seremban) for inspiring me to acquire a deeper knowledge in failure analysis. Thanks

are due to Mr. Gan Lim (Product Manager) for cooperating with me to pursue my work at a faster pace.

I thank my friends, Mr. Saat Shukri Embong, Mr. Nik Tajuddin Yusof, Mr. Mohabbatul Zaman and, Mr. Ghazali Omar for their encouragement. Finally I thank my wife and parents for understanding, patience, and support extended to complete my work in shortest possible time.

TABLE OF CONTENTS

Page

AKNOWLEDGEMENTS iii
LIST OF TABLES vii
LIST OF FIGURES viii
LIST OF PLATES xiii
LIST OF ABBREVIATIONS xv
ABSTRACT xix
ABSTRAK.. xxi

CHAPTER

1 INTRODUCTION 1

2 LITERATURE REVIEW 3

Definition,Derivation and Differences 4
Electrostatic Discharge(ESD) 4
Electrical Overstress(EOS) 5
Differences between Electrostatic Discharge(ESD) and Electrical Overstress(EOS) 6
Metal Oxide Semiconductor Field Effect Transistor(TMOS) Device 7
Electrical Discharge(ESD) and Electrical Overstress(EOS) Modelling Choices 15
Human Body Model(HBM) 16
Machine Model(MM) 17
Charge Device Model(CDM) 18
Additional Models 19
Failure Analysis Methodology, Tools and Techniques 20
Failure Mechanisms 27
Preventive Measures 31
Summary 33
Scope of the Present Investigation 33

3 EXPERIMENTAL FACILITIES 35

Test Methods 35
Breakdown Voltage between Gate to Source(BVGSS)
Stress Test 36
Parametric Abnormality Test(PAT) 39
Voltage Susceptibility Test 39
Subsidiary Test Techniques 43
Chemical Decapsulation Technique 43
Die Delayering Technique 45
Liquid Crystal Technique 47
Cross-Sectioning Technique 48
Instruments and Instrument Systems 51
Programmable Curvetracer 52
FET Tester 54
Allesi Probing Station Test System 56
Scanning Electron Microscope(SEM) 58
Optical Microscope 61
Failure Analysis Process 62
Test Procedures 65
Breakdown Voltage between Gate to Source(BVGSS)
Stress Test 65
Parametric Abnormality Test(PAT) 69
Voltage Susceptibility Test 72

4 RESULTS AND DISCUSSION 75

Preparation of Samples 75
Failure Analysis Results 84
Breakdown Voltage between Gate to Source(BVGSS)
Stress Test: Failure Analysis 86
Parametric Abnormality Test(PAT): Failure Analysis 92
Voltage Susceptibility Test: Failure Analysis 94
Cross Sectioning: Failure Analysis............................ 97

5 CONCLUSIONS 106

BIBLIOGRAPHY 108

VITA 114

LISTS OF TABLES

Table **Page**

2.1 Electrostatic Discharge Susceptibility Voltage[Unger, 1995].. 15

3.1 The typical setting on the FET tester for testing 2N7002LT1 TMOS device...................................... 38

3.2 Control setting details... 54

3. FET tester output printout (biased conditions portion)...................................... 67

3.4 FET tester output printout (results portion).. 68

LISTS OF FIGURES

Figure		Page
2.1	MOSFET DMOS structure [Baliga,	7
2.2	MOSFET VMOS structure[Baliga,	
2.3	Single cell cross-section of TMOS device	8
2.4	N-channel and P-channel TMOS enhancement mode	10
2.5	TMOS cell structure	11
2.6	Details of 2N7002LT1 TMOS device	12
2.7	Schematic of channel formation	13
2.8	Layout of TMOS device	14
2.9	Human Body Model(HBM)	16
2.10	Machine Model schematic diagram	17
2.11	Charge Device Model schematic diagram	19
2.12	Typical curvetracer I-V characteristics	21
3.1	Circuit details for BVGSS StressTest	37
3.2	Circuit details for HBM model	42

3.3	Shows two cell TMOS cross-section layer	45
3.4	Front control panel of curvetracer Tektronix-370A model	53
3.5	Flow chart for Failure Analysis Process..........................	64
3.6	Block diagram of BVGSS Stress Test	66
3.7	BVGSS Stress Test breakdown voltage I-V characteristics.....	69
3.8	Block diagram of PAT test	70
3.9	PAT dead short I-V characteristics	71
3.10	PAT resistive short I-V characteristics	71
3.11	PAT resistive short I-V characteristics	72
3.12	Block diagram of Voltage Susceptibility Test	73
3.13	Voltage Susceptibility Test breakdown voltage I-V characteristics	73
3.14	Voltage Susceptibility Test dead short I-V characteristics	74
4.1	Positive BVGSS Stress Test results	76
4.2	Negative BVGSS Stress Test result	77
4.3	Allowable BVGSS Voltage for the 2N7002LT1 TMOS..........	78

4.4	Leakage current versus biased voltage	80
4.5	Diagram shows how the IGSS leakage current form during negative BVGSS biasing	81
4.6	Diagram shows how the IGSS leakage current form during positive BVGSS biasing	81
4.7	Voltage Susceptibility level for the device	83
4.8	Shows the failure location sites of devices subjected to various tests...	85
4.9	Damage site in the device after passivation layer and metallisation layer removal (Specimen No.1)	87
4.10	Damage site in the device after passivation and metallisation layer removal (Specimen No.2)	87
4.11	Damage site in the device after passivation and metallisation layer removal (Specimen No.3)	88
4.12	Photos shows melting gate oxide on the failed positive and negative biased BVGSS stress test device.....................	89
4.13	Damage site in the device after passivation, metallisation and polysilicon layer removal (Specimen No.4)	90
4.14	Damage site in the device after passivation, metallisation and polysilicon layer removal (Specimen No.5)	90
4.15	Damage site in the device after passivation, metallisation and polysilicon layer removal (Specimen No.6)	91

4.16	Shows the cross section part of a TMOS device together with its material layer and dimension	91
4.17	Damage site in the device after passivation and metallisation layer removal (Specimen No.7)	93
4.18	Damage site in the device after passivation and metallisation layer removal (Specimen No.8)	93
4.19	SEM, Micrograph shows melting and rupturing of gate oxide at the cell location of the die (Specimen No.7)	94
4.20	Damage site in the device after passivation and metallisation layer removal (Specimen No.9)	95
4.21	Damage site in the device after passivation and metallisation layer removal(Specimen No.10)	96
4.22	SEM image shows melting gate oxide on the failed ESD Voltage Susceptibility Test device	97
4.23	Shows orientation and location of the following cross-section figures	98
4.24	Cross-section through gate bond pad.(location 1)	99
4.25	Close-up view of area indicated in figure 4.24. Blue arrow indicates location of failure sites where gate oxide thickness is reduced to 950 Angstroms	100
4.26	Cross-section through gate feed after staining.(Location 2)	101
4.27	Close-up view of gate feed seen in Figure 4.26. Vertical blue arrow indicates location of failure sites where gate oxide thickness reduces to 800 Angstroms	102

4.28	Cross-section through source cell after staining. Location 3)	103
4.	Close-up view of source cell seen in Figure 4.28	104

LIST OF PLATES

Plate		Page
3.1	FET Test tester	37
3.2	IMCS System-700 (ESD modelling equipment)	41
3.3	IMCS System-700 is connected to the curvetracer	42
3.4	Fume ventilated acid hood for decapsulation	43
3.5	Illustration of the soldering process	44
3.6	Illustrated view of soldered legs of the device on the strip	44
3.7	Illustration of decapsulation process	45
3.8	Die with probing needles	48
3.9	Cross sectioning technique work area	49
3.10	Die with sample block	50
3.11	Sample block mounted on a jig	50
3.12	Curvetracer Tektronix-370A model	52
3.13	Allessi Probing Station Test System and curvetracer	57
3.14	Schematics of probe connections to the die	57

3.15 Jeol Scanning Electron Microscope 58

3.16 SPI-Module Sputter Coater-11

3.17 Inter lock air chamber 59

3.18 SEM control panel 60

3.19 High and Low magnification microscopes 61

LIST OF ABBREVIATIONS

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect transistor
TMOS	A type of MOSFET transistor, letter "T"
DMOS	"D" type structure Metal Oxide Semiconductor
VMOS	"V" type structure Metal Oxide Semiconductor
NMOS	N type Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
SCR	Silicon Cathode Rectifier
ESD	Electrostatic Discharge
EOS	Electrical Overstress
SOT23	A surface mount package with three legs
PAT	Parametric Abnormality Test
HBM	Human Body Model
MM	Machine Model
CDM	Charge Device Model

SCM	Small Capacitance Method
TFM	Thermal Failure Modelling
STM	Simplified Thermal Model
BVGSS	Breakdown Voltage between Gate to Source
BVDSS	Breakdown voltage between drain to source
V_{ds}	Drain to source voltage
$V_{ds}(on)$	Drain to source on voltage
V_{gs}	Gate to source voltage
V_{gs}	Threshold voltage
V_g	Gate voltage or BVGSS
IGSS	Gate to source leakage current
IDSS	Drain to source leakage current
I_d	Drain current
I-V	Current versus Voltage
E-beam	Electron-beam
FALT	Failure Area Location Technique
SEM	Scanning electron microscope

ATE	Automatic test equipment
PC-AT	Personal computer, type AT
FIFO	First in first out
DOS	Disk operating system
FET	A trademark of a test machine
SiO_2	Silicon dioxide
$Si\text{-}SiO_2$	Silicon-Silicon dioxide
TEOS	Insulating oxide/ interlayer dielectric
N+	Heavily doped N type material
N-	Lightly doped N type material
P+	Heavily doped P type material
P-	Lightly doped P type material
V/cm	Volts per centimeter
Angstroms	10^{-10} meter
mA	miliampere, 10^{-3} Ampere
µA	microampere, 10^{-6} Ampere
nA	nanoampere, 10^{-9} Ampere

pA	picoampere,
ns	nanosecond,
ms	milisecond,
pF	picofarad,
Kohms	Kiloohms,
Mohms	Megaohms,

Abstract of thesis submitted to the Senate of Universiti Putra Malaysia in partial fulfilment of the requirements for the degree of Master of Science.

FAILURE ANALYSIS INVESTIGATION ON 2N7002LT1 TMOS DEVICE DUE TO ELECTROSTATIC DISCHARGE(ESD) FAILURES

by

ABDUL HALIM BIN ABDUL MANAF

APRIL 1998

Chairman:
Faculty:

The common failures in the electronic devices e.g. Metal Oxide Semiconductor(MOS),
and T type Metal Oxide Semiconductor Field Effect Transistor (TMOS) are due to Electrostatic Discharge(ESD) and Electrical Overseers(EOS). A
review is carried out giving an account of various types of failures and failure analysis philosophies.
investigation.
methodology developed here,
Seremban,
between Gate to Source(BVGSS) Stress Test,
Parametric Abnormality Test (PAT) to induce failure. It has been observed that the

2N7002LT1 TMOS device does not fail within 45 volts of positively as well as negatively biased voltage condition when applied to the gate and source of the device, during BVGSS Stress Test. On the other hand the Voltage Susceptibility Test has given a limiting voltage of 110 volts, for the device to fail. The failure of the devices have been studied using the failure analysis philosophy developed here and it is observed that the failure is due to thinning of the gate oxide layer. The detailed scanning electron microscope (SEM) study has been carried out to comment on the additional mechanics of failure. The amount thinning of the gate oxide layer in the various regions of the device has been found to be in the range of 800 to 950 Angstroms.

Abstrak tesis yang dikemukakan kepada Senat Universiti
sebagai memenuhi sebahagian daripada syarat ijazah Sarjana Sains.

KAJIAN PENGANALISAAN KEROSAKAN ALAT JENIS TRANSISTOR, 2N7002LT1 TMOS DISEBABKAN OLEH NYAHCASAN ELEKTROSTATIK(ESD)

Oleh

ABDUL HALIM BIN ABDUL MANAF

APRIL 1998

Pengerusi:

Fakulti:

Kegagalan yang biasa berlaku kepada perkakasan elektronik seperti MOS, MOSFET dan TMOS adalah disebabkan oleh Nyahcas Electrostatik (ESD)
Lebihan Elektrikal (EOS)
beberapa jenis kegagalan dan falsafah analisis kegagalan. Kaedah baru analisis kegagalan telah dibangunkan sebagai sebahagian daripada kajian ini. Sebagai penggunaan kepada falsafah semasa bagi kaedah analisis kegagalan yang telah dibangunkan,
telah dipilih. Perkakasan
(BVGSS)

menghasilkan kegagalan. Pemerhatian menunjukkan bahawa perkakasan 2N7002LT1 TMOS tidak gagal pada 45 volt pada keadaan voltan positif dan juga negatif. Pada sudut yang lain,

perkakasan tersebut untuk gagal. Kegagalan perkakasan telah dikaji menggunakan falsafah analisis kegagalan yang telah dibangunkan dan pemerhatian menunjukkan bahawa kegagalan adalah disebabkan oleh penipisan pada lapisan get oksida. Penelitian lengkap mikroskop imbasan elektron (SEM)

maklumat tambahan yang terperinci mekanik kegagalan. Jumlah penipisan lapisan get oksida telah ditemui dalam julat di antara 800 ke 950 Angstroms.

CHAPTER 1

INTRODUCTION

Now a days customers do insist to have reliable and robust electronic products. It has been observed that the majority of failures are due to Electrostatic Discharge(ESD)
scaled down to considerably,
susceptible to ESD and EOS events,
This in turn hampers the functionality of the subassemblies of the integrated circuit of the product.
integrated circuits are due to ESD and EOS events. It is also observed that the failures in the Metal Oxide Semiconductor(MOS)
prevent these failures it is necessary that one should understand,
events affect the failure process.

The purpose of this investigation is to carryout a systematic study of failure investigation process.
associate ESD event for study as this is easy to generate as compared to EOS event. There are many types of Metal Oxide Semiconductor(MOS)
Semiconductor Field Effect Transistor(MOSFET)
study a MOSFET device known as 2N7002LT1 TMOS,
Seremban had been chosen. This device is being used in audio/radio frequency circuits in high-frequency inverters,

A systematic study of failure investigation process has been carried out and the details of the thesis is presented as follows:

Chapter 2,

failures due to ESD and EOS events have been reviewed. The details about different models used by various investigators are also given. Various methods of failure analysis, tools and techniques along with remedial measures to avoid failures are also given. Finally the scope of the thesis is presented.

Chapter 3,

Source(BVGSS) Stress Test, Parametric Abnormality Test, and Voltage Susceptibility Test, to be conducted to induce the failure in the device. The chapter also enumerates various test techniques in support of main tests along with associated instrumentation. A new type of failure analysis methodology is developed and explained in detail. It is also discussed as to how to implement the methodology of testing for a particular electronic device. The failure analysis methodology developed definitely contributes to the knowledge and understanding of the failure analysis philosophy. Finally various test procedures are described which are used in this investigation.

Chapter 4, describes the results and discussions. Altogether three types of tests are given in Chapter 3. The test are carried out to induced the failures in the samples. In other words the outcome of these tests lead to preparation of samples. Subsequently the failure analysis is carried out on the samples obtained from three different tests. Finally, Chapter 5,