UNIVERSITI PUTRA MALAYSIA

SOFTWARE MODIFICATION IN A FAULT ANALYSIS TOOL FOR CRITICAL PATH DEBUGGING

HAN CHUNG DEAN

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By

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Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfilment of the Requirement for the Degree of Master of Science

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Abstract of thesis presented to the Senate of University Putra Malaysia in fulfilment of the requirement for the degree of Master of Science

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April 2009

Chairman: **Roslina Bt. Mohd. Sidek, PhD**

Faculty: **Engineering**

Microprocessor units caught with speed failure are becoming more and more eminent as the fabrication process shrinks according to Moore's Law. Failure Analysis (FA) engineers confront the problem using Critical Path Debug method utilizing special IC (Integrated Circuit) test system capable of testing various types of microprocessor's failure. But such test system does not come cheap, each costing more than USD 2.5 million. In order to bring down cost, a system to pull test data and locate critical path using personal computer (PC) is proposed.

This system is built upon Intel Penang's Internal FA tool called Personal Computer Failure Analysis (PCFA) which utilizes a host computer to collect data from Device Under Test (DUT) through TAP (Test Access Port). As PCFA was not originally build up to carry out critical path debug, hardware modification and software enhancement is required. The hardware modification involves platform rework and external FSB (Front Side Bus) frequency

injection. By doing so, microprocessor speed can be controlled during test pattern run. The software is modified to include critical-path-related test subroutines housed inside PCFA library. These subroutines collect, compare and display test results. The program is tested with a series of Intel's microprocessors to ensure that it is working as intended for current and future products. 1000 test vector results are recorded from both PCFA and ATE's system to carry out compare verification.100% matched is observed for all the test vector results thus prove the functionality of the project "Critical Path Fault Isolation Debug for Intel Microprocessor Using Personal Computer".

The PCFA hardware cost only USD 10 thousand which is 0.4% of the cost of an IC test system and is currently capable of running shmoo, performing cache test, I/O pin test and also macro Fault Isolation (FI) for each test pattern in a couple of seconds. Although in terms of functionalities; complex IC test system will certainly have the upper hand but in the case of solving common general microprocessors' failures, system based test solution is much more cost effective.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Master Sains

PENGUBAHSUAIAN PERISIAN DALAM PERALATAN ANALISA KESALAHAN NYAHPEPIJAT LALUAN KRITIKAL

Oleh

HAN CHUNG DEAN
April 2009

Pengerusi: **Roslina Bt. Mohd. Sidek, Ph.D**

Fakulti: **Kejuruteraan**

Bilangan Unit mikroprosesor yang gagal ujian kelajuan semakin ketara disebabkan proses fabrikasi yang semakin mengecil mengikut Falsafah Moore. Jurutera penganalisis kegagalan menangani masalah ini dengan mengaplikasikan kaedah Nyahpepijat Laluan Kritikal menggunakan sistem ujian litar bersepadu yang canggih. Sistem ini berkebolehan menguji pelbagai jenis kegagalan mikropemproses tetapi ianya tidak murah di mana kos mesin melebihi USD 2.5 juta. Untuk mengurangkan perbelanjaan, maka dicadangkan sebuah sistem untuk.mengumpul data ujian serta mencari laluan kritikal dengan menggunakan komputer peribadi.

Sistem ini dibina atas pelantaran Penganalisis Kegagalan Komputer Peribadi (PCFA) yang digunakan khas oleh Intel Penang. PCFA menggunakan komputer peribadi untuk mengumpul data melalui antaramuka pengaksesan ujian (TAP) daripada mikropemproses bawah ujian (DUT). Disebabkan PCFA pada asalnya bukan direka untuk melaksanakan Nyahpepijat Laluan Kritikal,

maka pengubahsuaian peralatan keras komputer dan peningkatan perisian perlu dilaksanakan. Fasa pertama projek melibatkan pengubahsuaian pelantaran untuk membolehkan penyuntikan frekuensi Linkaran Bus Halaman (FSB) dari sistem luaran. Dengan demikian, kelajuan mikropemproses boleh dikawal semasa ujian dijalankan. Fasa kedua menumpukan kepada atas penciptaan pengaturcaraan Laluan Kritikal dalam perisian pusat PCFA. Pengaturcaraan ini bertujuan mengumpul, membanding serta mempamerkan keputusan ujian. Dalam Fasa ketiga, penelitian terakhir dijalankan ke atas sesiri mikropemproses Intel untuk memastikan ianya serasi dengan produk intel sekarang dan yang akan datang. 1000 kes uji telah dijalankan dan keputusan dari PCFA serta sistem ATE dicatatkan untuk membuat perbandingan. Diperhatikan keputusan untuk semua kes ujian adalah 100% seiras. Ini membuktikan projek “Nyahpepijat Pengasingan Kesalahan Laluan bagi Micropemproses Intel Berasaskan Sistem Komputer Peribadi” adalah sesuai digunakan.

Kos perbelanjaan peralatan keras PCFA ialah USD 10 ribu iaitu hanya 0.4% dari kos sistem ujian litar bersepadu. Sistem ini berkemampuan untuk menjalankan operasi *shmoo*, ujian *cache*, ujian pin keluaran/masukan (I/O) dan juga pengasingan kegaglan makro untuk setiap satu corak ujian dalam beberapa saat sahaja. Dari segi fungsi, sistem ujian litar bersepadu yang kompleks memang mempunyai kelebihan tetapi dalam menangani kes kegagalan Laluan Kritikal, sistem berasaskan komputer peribadi merupakan pilihan yang lebih kos efektif.

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Beside EK, there are also technical supervisors guiding me throughout the project which I'm indebted to. They are Lim Yew Tee (Motherboard and Processor Specialist), Mak Mun Wai (Micorarchitecture Specialist) and Wong

Yik Choong (Automatic Test Equipment Specialist). Each of them guided me through a significant phase of the project, sharing invaluable knowledge they have; from hardware to software and finally testing the developed platform. Without their coaching, there is just no way I will be able to complete the project. I would also like to forward my thanks to Principle Engineer, Lim Seong Leong. He is the one who gave birth to SBTS (System Based Test Solution) and currently overseeing its development. It is an honor to be given chances working on his brainchild.

My buddy Faizal bin Omar also contributed greatly to the success completion of the project. He is a warmhearted person helping me assimilate to my working environment in such short time. Besides, his vast knowledge on programming aids me greatly in developing Window's application for my project. During my research period in Intel, I'm also given opportunity to attend job training program of a Fault Isolation Engineering. The tutors are Grace Khoo, Lee Jin Yee, Jeffery Ngan and Roziatul bt. Ishak. They are very sincere in sharing the knowledge and I benefit greatly from their training program.

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did quite an amount of paperwork to ensure that my postgraduates study and research in Intel can be undertaken smoothly.

Last but not least, I would like to extend appreciation to my family, relatives and friends. I would like to deliberately thank my parents and siblings that provide me with moral and financial support throughout my postgraduate studies. I am really grateful for all that they have done for me. Thank you.

I certify that a Thesis Examination Committee has met on 13 April 2009 to conduct the final examination of Han Chung Dean on his thesis entitled "Software Modification in a Fault Analysis Tool for Critical Path Debugging" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master of Science.

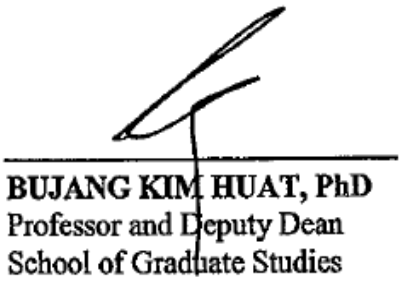
Members of the Thesis Examination Committee are as follows:

Senan Mahmod Abdullah, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Chairman)

Sudhanshu Shekhar Jamuar, PhD
Professor
Faculty of Engineering
Universiti Putra Malaysia
(Internal Examiner)

Mohd. Nizar Hamidon, PhD
Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Internal Examiner)

Mohamed Khalil Hj. Mohd Hani, PhD
Professor
Faculty of Electrical Engineering
Universiti Teknologi Malaysia
(External Examiner)



BUJANG KIM HUAT, PhD
Professor and Deputy Dean
School of Graduate Studies
Universiti Putra Malaysia

Date: 18 June 2009

This thesis submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfillment of the requirement for the degree of Master of Science.

The members of the Supervisory Committee are as follows:

Roslina bt. Mohd. Sidek, PhD
Associate Professor
Faculty of Engineering
Universiti Putra Malaysia
(Chairman of Supervisory Committee)

Rahman Wagiran
Senior Lecturer
Faculty of Engineering
Universiti Putra Malaysia
(Member of Supervisory Committee)

_____

HASANAH MOHD. GHAZALI, PhD
Professor and Dean
School of Graduate Studies
Universiti Putra Malaysia

Date: 9 July 2009

DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.

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Han Chung Dean

Date:

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LISTS OF ABBREVIATIONS

Abbreviation	Definition
ATE	Automatic Test Equipment
ATX	Advance Technology Extended (Motherboard form factor)
BIOS	Basic Input/Output System
CPU	Central Processing Unit
DFT	Design For Testability
DOE	Design On Experiment
DUT	Device Under Test
FA	Fault Analysis
FI	Fault Isolation
FUB	Functional Unit Block
FSB	Front Side Bus
FSM	Finite State Machine
GUI	Graphical User Interface
HTML	HyperText Markup Language use for webpage creation
IA-32	Intel Architecture – 32 bit (also known as x86)
ICH	I/O Controller Hub or Southbridge of Motherboard
IO	Input Output
IREM	Infrared Emission Microscope
ITP	In Target Probe (Intel's Internal Tools)
JTAG	Joint Test Action Group
LCP	Locate Critical Path

LSI	Large-Scale Integration
MCH	Memory Controller Hub or Northbridge of Motherboard
NFF	No Fault Found
PC	Personal Computer
PCFA	Personal Computer for Failure Analysis
Perl	Practical Extraction and Report Language
RAM	Random Access Memory
SBTS	System Based Test Solution
SBFT	System Based Functional Test
SIMD	Single Instruction, Multiple Data
ssucnt	Scheduler and Scoreboard Unit Counter
Std	Standard
SPI	1. Serial Peripherals Interface 2. Speed Path Identification
TAP	Test Access Port
VB.NET	Microsoft Visual Basic.NET programming
VID	Voltage Identity (CPU voltage indicator)

CHAPTER 1

INTRODUCTION

Chapter 1 provides a basic idea about the project Critical Path Fault Isolation Debug for Intel Microprocessor Using Personal Computer, and how it is able to change Intel's status quo in debugging. This chapter also outlines project's aim and objectives targeted to be accomplished.

1.1 Project Overview

The title 'Software Modification in A Fault Analysis Tool for Critical Path Debugging' can be explained in layman terms as using personal computer system to execute debugging activities on Intel's microprocessor with critical path failure. Personal computer or PC in this context refers to normal average computer working under standard operating system; not those suited on ATE (Automatic Test Equipment) or workstation for the sole purpose of running FA (Fault Analysis). Such system is named PCFA. Critical path failure is defined as a type of microprocessor defect dependent on operating frequency [1, 2]. Such defect rendered the unit unable

to operate at its intended speed or working region. Normally critical path failure happened when the unit is unable to run up to its default range but there is some sparse cases where unit is running fine at higher frequency but failed to run at the slower default range. This project is intended to catch such failures and isolate them to specific clock domain region inside the microprocessor.

Before the development of PCFA, conventionally when a faulty unit is pass down from production to the Quality and Reliability Department, the first thing to be done is to reproduce the same error that has been recorded by the production team using ATE which is configured to operate similar to their production floor siblings. If the error is non-reproducible, a NFF (No Fault Found) will be issued ending the process prematurely; else further analyze is carried out to gather relevant data about the fault [3]. The unit is run through various test patterns; these patterns are much extensive compared to those in the production system and take a longer time ranging from a few hours to even a full day to complete. The result is achieved and depending on the characteristic of the failures; some results are one liner, others in table or graphic form, and a few is displayed in shmoo plot. Shmoo plot is an organized display of the response of a component or system varying over a range of conditions and inputs such as voltage, temperature, frequency and etc [4].

Figure 1.1 shows some examples of shmoo plots which consist of both text and graphical plots. Based on these results obtained, engineers then perform FI (Fault Isolation), which is a process of minimizing fault region using the signal tracing approach. This process is normally carried out by experience engineers familiar with the microprocessor architecture. The region will be scrutinized up from FUB

(Functional Unit Block) level all the way down to individual circuits and finally components level [5]. A hypothesis is then derived and depending on the type of hypothesis, further analysis will be carried out inclusive of physical FA to further examine the failure.

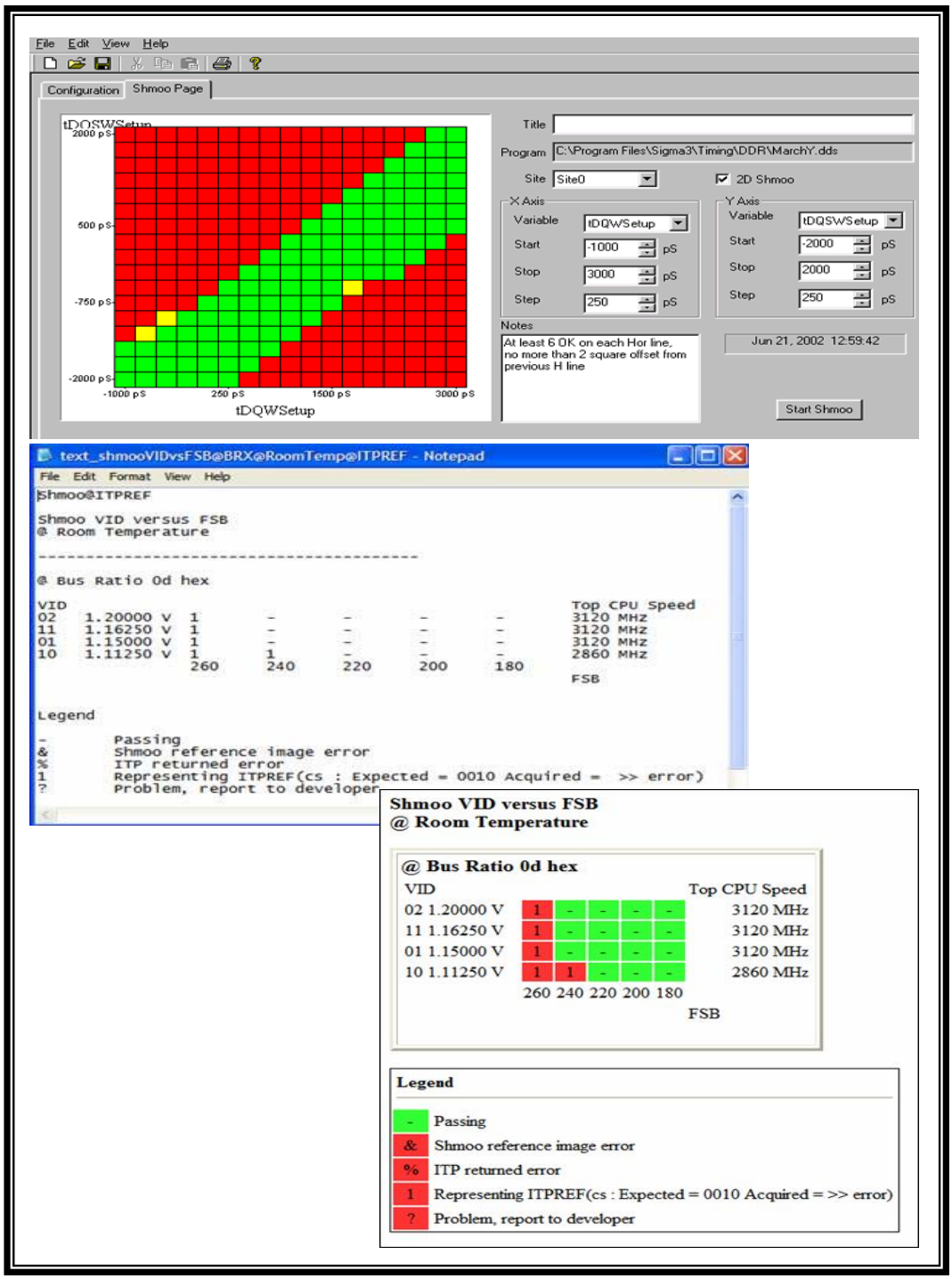

Figure 1.1: Shmoo Plot Examples

The problem with conventional method is that quite a handful of expensive ATEs need to be available from time to time to pull data, such routine only utilized very minimum of ATE's capabilities yet occupied large amount of its time. With the introduction of SBTS (System Based Test Solution), the approach of FA changes to be more economical and efficient. SBTS consists of 3 major parts, they are SBTS-IO (dealing with Input Output pins), SBTS-Cache (dealing with specialize RAM built on to the microprocessor) and finally SBTS-SBFT (which stands for System Based Functional Test) or more renown as PCFA in Intel.

The new methodology is that once the fault is reproducible by ATE in FA lab, the data gathering process is switch from using an ATE to the SBTS. It is well acknowledged that an ATE system is much capable and efficient in gathering FA data compared to SBTS; but when economic factor is taken into consideration, ATE costing more than half a million USD has to hands it over to SBTS costing only 10 thousand USD. On top of that, floor size of the equipments can be greatly reduced as PCFA is much more mobile, easier to handle and can be stacked up compare to ATE with the sheer size of a wall cabinet. Power consumption is also trimmed down significantly from a 3 phase power supply down to a single phase line.

Slow long data pulling session can now be executed using SBTS while ATE can be freed up to run verification on fault units or others much strenuous routines. By efficiently relocating the job loads of these machines, the numbers of ATE required can be significantly cut down which in the end is great news for the department in terms of costing. This is also the core motivation behind this project.

Despite the huge advantages of switching the data gathering process to SBTS, the transition is not as fast and as smooth duly because of the development of SBTS from ground up. The research background of SBTS can be traced back to 2003, where test access port is used to pluck test hole resolutions. Through this port, various microprocessors' states can be accessed and the idea of data pulling started from there. The few hurdles at the beginning that stall the project include hardware and software development. For hardware, a rounded computer mother board is designed from bottom up to suits other FA machineries in the lab, where as for software, a smart interface need to be created. The software needs to be robust yet modular enough to extend the capabilities of SBTS. It took 4 years for SBTS to reach product usage maturity but yet there are hiccups and plenty of room for SBTS capability to be further enhanced. Figure 1.2 shows the PCFA system:

When these 2 major problems are overcame, the project flourished and new features can be added in the form of modules. The project 'Critical Path Fault Isolation Debug for Intel Microprocessor Using Personal Computer' can be labeled as one of those modules that greatly enhance the capability of PCFA.

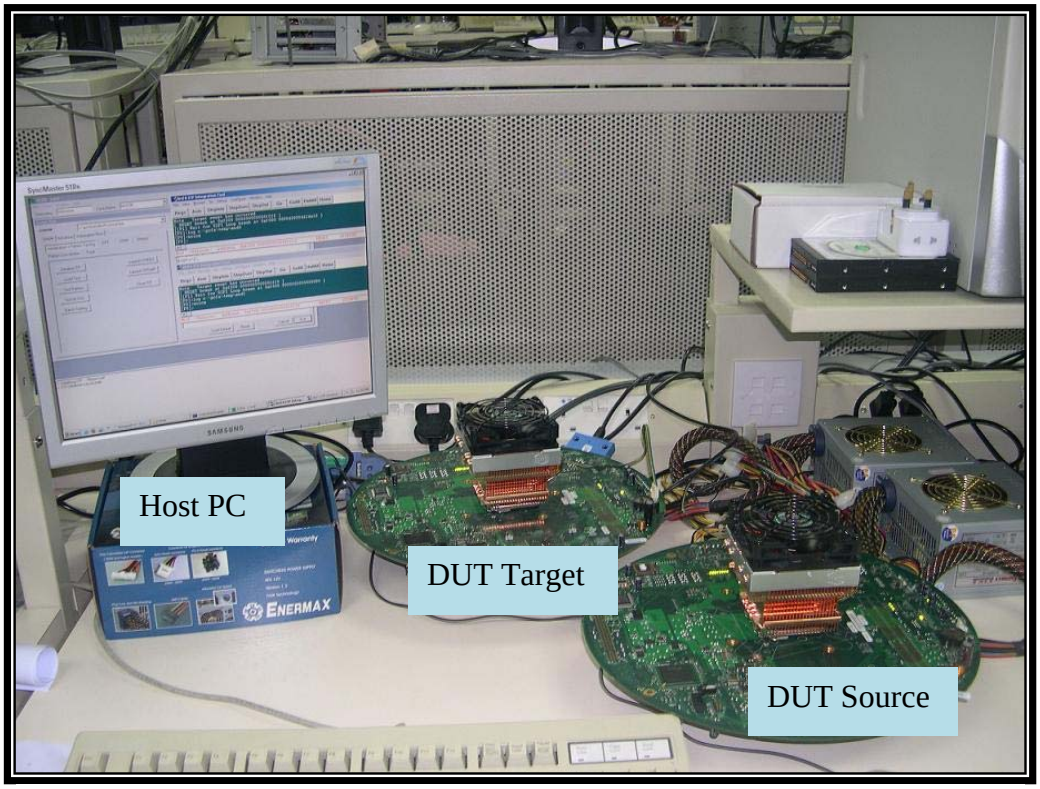

Figure 1.2: PCFA System

The first phase of the project deals with hardware rework and incorporation of function generator frequency into FSB (Front Side Bus) of the intended test system, this process is somewhat similar to overclocking/downclocking of a computer system [6]. A software module is also created to read and write data to and from the function generator. By using software implementation, all human errors of controlling the function generator manually can then be eliminated. Besides, there is also the added advantage of remote accessing the system which gives great mobility to engineers working with it. Phase one of the project is called a success when microprocessor seated in the test system can run shmoo with frequency variable controlled through FSB output by function generator.