UNIVERSITI PUTRA MALAYSIA

DESIGN OF LOW-VOLTAGE HIGH-PERFORMANCE SAMPLE AND HOLD CIRCUIT IN 0.18µm CMOS TECHNOLOGY

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DESIGN OF LOW-VOLTAGE HIGH-PERFORMANCE SAMPLE AND HOLD CIRCUIT IN 0.18µm CMOS TECHNOLOGY

By

WAEL A Y ALIHASAN

Thesis Submitted to the School of Graduate Studies, University Putra Malaysia, in Fulfilment of the Requirements for the Degree of Master of Science

June, 2009

DEDICATED TO

MY LATE FATHER

ABD ALFTAH

MY FAMILY AND UNCLE MAHMOUD

Abstract of thesis presented to the Senate of University Putra Malaysia in fulfilment
Of the requirement for the degree of Master of Science

DESIGN OF LOW-VOLTAGE HIGH-PERFORMANCE SAMPLE AND HOLD CIRCUIT IN 0.18μM CMOS TECHNOLOGY

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WAEL A. Y. ALIHASAN

June 2009

Chairman: Professor Sudhanshu Shekhar Jamuar

Faculty: Engineering

Over the last two decade, digital signal processing (DSP) has grown rapidly in electronic systems to provide more reconfigureability and programmability in the applications, compared to analog component, which allows easier design and test automation. Digital circuit usage is increasing because of scaling properties of very large scale integration (VLSI) processes. This has allowed new generation of digital circuit to attain higher speed, more functionality per chip, low power dissipation, lower cost. Analog world, analog to digital converter (ADC) are used to convert the signal from analog to digital domain. For interfacing with DSP sample and hold (S/H) circuit is a key building block in, and is often used in front end of the ADCs to relax their timing requirement. The function of S/H circuit is to take samples to its input signal and hold these samples in its output for some period of time.

The analog circuits in low voltage and low power have assumed great significance due to mixed-mode design required for modern electronic gadgets that demand portability and little power consumption. The mixed mode circuit has existence of both analog and digital circuits on the same chip and it is possible to have low

voltage digital circuit in modern scaled-down technologies. However the same is not always true with analog circuits due to the constrains of device noise level and threshold voltage (V_T) of MOSFET. Thus for analog circuit to co-exist on the same substrate along with digital system and share same supply voltage, the operation of analog circuit in low voltage environment is essential.

The objective of this research is to design a low-voltage, high-performance S/H circuit that will address the above problems. A typical switch capacitor S/H circuit needs amplifier, switches and capacitor. New amplifier have been designed by using the architecture of single stage fully differential folded cascode low voltage operation transconductance amplifier (OTA) which has high gain and speed; the gin boosting technique was used for purpose of increasing the gain of the OTA. This technique does not affect the speed of the single stage. The transmission gate switches using CMOS devices, which have higher linearity and higher speed over a single MOS switch, have been designed for use in the S/H circuit. The switches are operated by clock generator with two non overlapping clock signals having low rise and fall time offering low noise for the S/H circuit. The clock was designed with 77.17ps rise and fall time to reduce the errors of driving MOS switches which results in higher linearity.

The S/H circuit was designed to operate with 1.8V supply voltage in 0.18um technology. The sampling rate is 40MSPS with spurious free dynamic range (SFDR) 65.7dB and SNR 70dB .

Abstrak tesis dipersembahkan kepada Senat University Putra Malaysia bagi pemenuhan
keperluan bagi darjah Sarjana Sains

REKABENTUK LITAR VOLTAN RENDAH BERPRESTASI TINGGI 'SAMPLE AND HOLD' DI DALAM TEKNOLOGI CMOS 0.18µm

Oleh

WAEL A. Y. ALIHASAN

June 2009

Pengerusi: **Professor Sudhanshu Shekhar Jamuar**

Fakulti: **Kejuruteraan**

Lebih dua dekad yang lalu, pemprosesan signal digital (DSP) telah berkembang pesat di dalam menyediakan lebih kemampuan susunatur semula dan pengaturcaraan di dalam aplikasi, berbanding dengan komponen analog, yang memudahkan rekabentuk dan automasi ujian. Penggunaan litar digital semakin bertambah disebabkan cirri-ciri proses integrasi skala sangat besar (VLSI). Ini membenarkan generasi baru litar digital mencapai kelajuan yang lebih tinggi, lebih banyak kefungsian setiap cip, pelesapan kuasa rendah, kos rendah. Di dalam dunia analog, konvertor analog ke digital (ADC) digunakan bagi menukar isyarat dari analog ke domain digital. Bagi tujuan pengantaramukaan dengan DSP litar sampel dan pegang (sample and hold – S/H) adalah blok binaan utama di dalam ADC dan kerap digunakan dalam bahagian depan ADCs untuk merelaks keperluan masa mereka. Fungsi litar S/H adalah untuk mengambil contoh kepada isyarat inputnya dan menyimpannya di dalam output untuk jangka waktu tertentu.

Litar-litar analog dalam voltan rendah dan kuasa rendah telah menampakkan kepentingan besar disebabkan rekabentuk mod campuran bagi gajet-gajet elektronik

yang memerlukan kemudahalihan dan penggunaan kuasa yang rendah. Litar mod campuran mempunyai kewujudan kedua-dua litar analog dan digital di dalam cip yang sama dan adalah berkemungkinan menperolehi litar digital rendah voltan di dalam teknologi pengecilan moden. Walaubagaimanapun, perkara yang sama tidak selalunya benar bagi litar-litar analog disebabkan kekangan aras hingar peranti dan voltan ambang (V_T) MOSFET. Oleh itu untuk litar analog wujud bersama pada substrat yang sama dengan sistem digital dan berkongsi voltan bekalan, operasi litar analog dalam persekitaran voltan rendah adalah penting.

Objektif kajian ini adalah merekabentuk litar S/H bervoltan-rendah, berprestasi tinggi yang akan memberi perhatian kepada masalah-masalah di atas. Sesuatu litar suis kapasitor S/H tipikal memerlukan penguat, suis-suis dan kapasitor. Penguat baharu telah direkabentuk menggunakan tahap tunggal pembezaan sepenuhnya kaskod berlipat bervoltan rendah penguat transkonduktans operasi (OTA) yang mempunyai pulangan tinggi dan kelajuan tinggi; teknik peningkatan gin telah digunakan bagi meningkatkan capaian OTA. Teknik ini tidak mempengaruhi kelajuan tahap tunggal.

Suis-suis gerbang transmisi menggunakan peranti-peranti CMOS, yang mempunyai lineariti dan kelajuan lebih tinggi berbanding suis MOS tunggal, telah direkabentuk untuk digunakan di dalam litar S/H. Suis-suis dioperasi oleh penjana jam dengan dua isyarat-isyarat jam yang tidak bertindih yang mempunyai peningkatan dan penurunan rendah yang menawarkan hingar rendah bagi litar S/H tersebut. Jam tersebut direkabentuk dengan 77.17ps masa peningkatan dan penurunan bagi mengurangkan kesilapan-kesilapan panduan suis-suis MOS yang akhirnya menghasilkan lineariti tinggi.

Litar S/H telah direkabentuk beroperasi menggunakan voltan bekalan 1.8V di dalam teknologi 0.18μm. Kadar pengsampelan adalah 40MSPS dengan julat dinamik bebas andaian (spurious free dynamic range – SFDR) 65.7dB dan SNR 70dB.

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APPROVAL

I certify that an Examination Committee has met on **25/6/2009** to conduct the final examination of Wael A Y Alihasan on his Master of Science thesis "Design of Low Voltage Sample and Hold Circuit in 0.18µm CMOS Technology" in accordance with the Universities and University Colleges Act 1971 and the Constitution of the University Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master degree.
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This thesis submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfilment of the requirement for the degree of Master of Science.
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Date:16 novmber 2009

DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.

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WAEL A Y ALIHASAN

Date:

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LIST OF ABBREVIATIONS/ SYMBOLS

ADC	Analog to Digital Converter
BSIM	Berkeley Short-Channel IGFET Model
CMOS	complementary metal oxide semiconductor
DAC	Digital to Analog Converter
DC	Discrete Current
DSP	Digital signal processing
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NMOS	Negative Channel Metal Oxide Semiconductor
OTA	Operation Transconductance Amplifier
PMOS	Positive Channel Metal Oxide Semiconductor
RF	Radio Frequency
RMS	Root Mean Square
S/H	Sample and Hold
SC	Switch Capacitor
SDR	Software Defined Radio
SPICE	Simulation Programme with Integrated Circuit Emphasis
TG	Transmission Gate

F_s	Sampling rate
F_{in}	Input signal bandwidth
μ_n	Electron mobility
C_{OX}	Gate oxide capacitance per area
V_G	Gate voltage
g_m	MOSFET Transconductance
C_H	Sampling capacitor
R_{on}	ON-resistance of the MOS switch
SR_{max}	Maximum Slew rate
V_{DS}	The Volt between the drain and the source of the transistor
V_{OD}	Over drive voltage
V_{Ref}	Reference voltage
V_{dd}	Supply voltage
V_{in}	Source voltage
V_{out}	Output voltage
V_{th}	Threshold voltage
t_{ac}	Acquisition time
C_C	Compensation capacitor
K	Boltzmann constant
L	Effective length of the device
T	Temperature
W	Effective width of the device
SR	Slew rate

CHAPTER 1

INTRODUCTION

1.1 Background

There has been multi fold increase in the applications of digital signal processing (DSP) in all works of life over past few decades. This has been more pronounced and visible due to its reconfigureability, enhanced functionality and low power consumption. Since most of the natural phenomenons are analog, an interface is needed between analog signal and the DSP, to implement the full capability of digital signal processor. The bridging between the real world analog signal processing and DSP blocks is implemented by using Analog to Digital Converters (ADCs).

With the rapid advancement in CMOS fabrication technology, more and more signal processing functions are being implemented in the digital domain, and the analog to digital boundary is moving towards the antenna. There are several types of ADC used in wireless receivers, each one has different specifications, different use which yield in different architectures. Figure 1.1 shows example of block schematic of an ideal futuristic wireless receiver, in which the analog components (the band pass filter and the low noise amplifier (LNA)) are limited to antenna. The analog to digital conversion is carried out immediately after RF stage and the signals are processed digitally to provide flexibility in receiver design [Hickling, 2005].

Since different wireless standards have different channel bandwidth and dynamic range requirement, single wide bandwidth analog to digital converter with wide dynamic range is required. ADC's can be categorizing into two categories depending on the sampling rate.

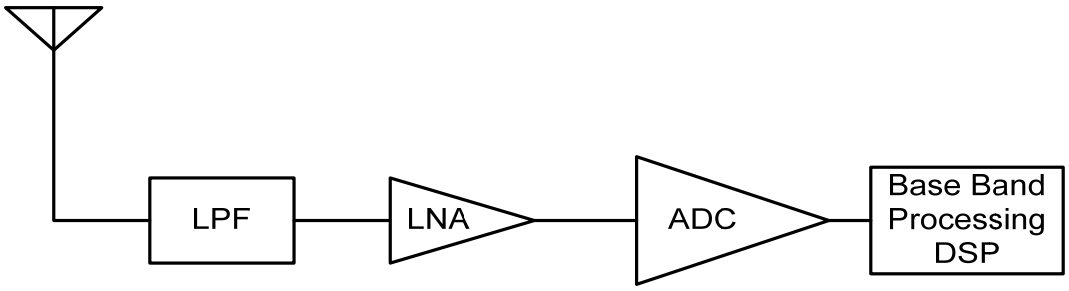

Figure 1.1: An Ideal wireless Radio receiver

The first category is with their sampling rate double of bandwidth input signal which is called Nyquist rate ADC's. The second type its wit sampling rate much higher than the input signal.

High resolution high speed data converters usually consume large power and integrating them with other blocks in RF transceiver is a major challenge with minimal power consumption [Zhang. et., al.,2008]. High speed Nyquist rate CMOS ADC with reasonable power consumption is available [Adeniran, 2005], but their resolution is limited. Low power consumption and low voltage operation are two important design constraints in portable system. The scaling down of CMOS technologies and system on chip (SoC) design requirements have driven researcher to investigate new circuits for ADC.

This thesis will focus on the pipeline ADC; it is a popular Nyquist rate ADC architecture for data conversion schemes having a compromise between speed and accuracy. Figure 1.2 shows the relation between the resolution and the ADC architecture. The sigma delta oversampled ADC has the best resolution but its speed is the lowest. Flash ADC is high speed architecture, but it has very low resolution. The recent trend is the pipeline ADC [Kester, 2005], which has reasonable resolution of 8 to 14 bits and sampling rate between 1MHz to 200MHz. Although

the pipeline architecture is inherently not as fast as a flash scheme, its serial nature results in a linear scaling of power and area with resolution, opposed to the exponential scaling which occurs in a flash. The pipeline architecture becomes a more attractive solution for resolution higher than 9 bits. Similarly, for very high resolution schemes sigma delta architectures are generally used, however the over-sampling nature of such schemes limits the maximum speed to a fraction of the fastest possible sampling rate. The concurrent nature of a pipeline removes the over-sampling required in effect converting the over-sampling speed limit into a latency problem.

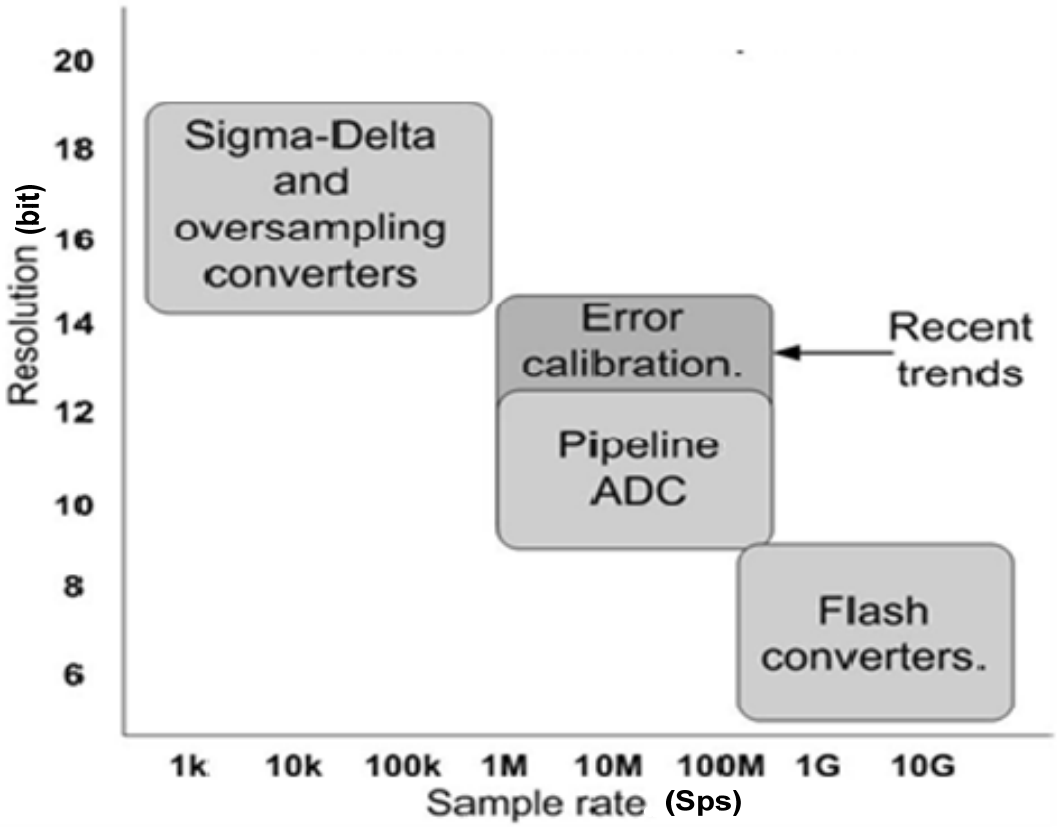

Figure 1.2: ADC architecture is a compromise between resolution and speed [Kester, 2005].

Sample and Hold (S/H) circuit is the most critical circuits in pipeline ADC. It allows the output of each stage to be used immediately to process its input sample. S/H circuit provides a constant output to the input of ADC, thus reducing the constraints

of high speed ADC and increasing the bandwidth. The noise and the distortion of the ADC are also reduced. This thesis addresses the design of low voltage high performance sample and hold circuit for use in 10 bit, 40 MSPs pipelined ADC.

1.2 **Motivation**

In mixed mode circuit design now days digital and analog systems are routinely integrated onto single chips. Digital circuits commonly employ various techniques, including low-voltage supply, to reduce power consumption. In order to have low power consumption in mixed mode circuit, it is desirable that analogue circuits must also be designed with low voltage supply and should consumes low power. Conventionally designed low supply voltage amplifier for Sample and Hold circuits suffer from performance trade-offs [Tsung-Sum Lee, 2005], resulting in low bandwidth and low dynamic range. This is because the design of any analogue circuit is a trade-off of various performance parameters such as power dissipation, supply voltage, gain, linearity and noise. All these parameters are important but for any one design, improving one parameter is likely to degrade another. The S/H circuit would require high performance operational Transconductance amplifier, transmission gate switch and a clock generator.

1.3 **Objectives**

The objectives of this research are:

1. To design and simulate low-voltage high- performance Operational Transconuctance Amplifier (OTA).
2. To design and simulate transmission gate switch.