



UNIVERSITI PUTRA MALAYSIA

**DESIGN OF LOW-VOLTAGE HIGH-PERFORMANCE SAMPLE AND
HOLD CIRCUIT IN 0.18 μ m CMOS TECHNOLOGY**

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FK 2009 47

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HOLD CIRCUIT IN 0.18 μ m CMOS TECHNOLOGY**

By

WAEI A Y ALIHASAN

**Thesis Submitted to the School of Graduate Studies, University Putra Malaysia, in Fulfilment of
the Requirements for the Degree of Master of Science**

June, 2009



DEDICATED TO

MY LATE FATHER

ABD ALFAH

MY FAMILY AND UNCLE MAHMOUD



Abstract of thesis presented to the Senate of University Putra Malaysia in fulfilment
Of the requirement for the degree of Master of Science

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June 2009

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Over the last two decade, digital signal processing (DSP) has grown rapidly in electronic systems to provide more reconfigurability and programmability in the applications, compared to analog component, which allows easier design and test automation. Digital circuit usage is increasing because of scaling properties of very large scale integration (VLSI) processes. This has allowed new generation of digital circuit to attain higher speed, more functionality per chip, low power dissipation, lower cost. Analog world, analog to digital converter (ADC) are used to convert the signal from analog to digital domain. For interfacing with DSP sample and hold (S/H) circuit is a key building block in, and is often used in front end of the ADCs to relax their timing requirement. The function of S/H circuit is to take samples to its input signal and hold these samples in its output for some period of time.

The analog circuits in low voltage and low power have assumed great significance due to mixed-mode design required for modern electronic gadgets that demand portability and little power consumption. The mixed mode circuit has existence of both analog and digital circuits on the same chip and it is possible to have low



voltage digital circuit in modern scaled-down technologies. However the same is not always true with analog circuits due to the constraints of device noise level and threshold voltage (V_T) of MOSFET. Thus for analog circuit to co-exist on the same substrate along with digital system and share same supply voltage, the operation of analog circuit in low voltage environment is essential.

The objective of this research is to design a low-voltage, high-performance S/H circuit that will address the above problems. A typical switch capacitor S/H circuit needs amplifier, switches and capacitor. New amplifier have been designed by using the architecture of single stage fully differential folded cascode low voltage operation transconductance amplifier (OTA) which has high gain and speed; the gain boosting technique was used for purpose of increasing the gain of the OTA. This technique does not affect the speed of the single stage. The transmission gate switches using CMOS devices, which have higher linearity and higher speed over a single MOS switch, have been designed for use in the S/H circuit. The switches are operated by clock generator with two non overlapping clock signals having low rise and fall time offering low noise for the S/H circuit. The clock was designed with 77.17ps rise and fall time to reduce the errors of driving MOS switches which results in higher linearity.

The S/H circuit was designed to operate with 1.8V supply voltage in 0.18 μ m technology. The sampling rate is 40MSPS with spurious free dynamic range (SFDR) 65.7dB and SNR 70dB .

Abstrak tesis dipersembahkan kepada Senat University Putra Malaysia bagi
pemenuhan
keperluan bagi darjah Sarjana Sains

**REKABENTUK LITAR VOLTAN RENDAH BERPRESTASI TINGGI
'SAMPLE AND HOLD' DI DALAM TEKNOLOGI CMOS 0.18 μ m**

Oleh

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Lebih dua dekad yang lalu, pemprosesan signal digital (DSP) telah berkembang pesat di dalam menyediakan lebih kemampuan susunatur semula dan pengaturcaraan di dalam aplikasi, berbanding dengan komponen analog, yang memudahkan rekabentuk dan automasi ujian. Penggunaan litar digital semakin bertambah disebabkan cirri-ciri proses integrasi skala sangat besar (VLSI). Ini membenarkan generasi baru litar digital mencapai kelajuan yang lebih tinggi, lebih banyak kefungsian setiap cip, pelepasan kuasa rendah, kos rendah. Di dalam dunia analog, konverter analog ke digital (ADC) digunakan bagi menukar isyarat dari analog ke domain digital. Bagi tujuan pengantaramukaan dengan DSP litar sampel dan pegang (sample and hold – S/H) adalah blok binaan utama di dalam ADC dan kerap digunakan dalam bahagian depan ADCs untuk merelaks keperluan masa mereka. Fungsi litar S/H adalah untuk mengambil contoh kepada isyarat inputnya dan menyimpannya di dalam output untuk jangka waktu tertentu.

Litar-litar analog dalam voltan rendah dan kuasa rendah telah menampakkan kepentingan besar disebabkan rekabentuk mod campuran bagi gajet-gajet elektronik

yang memerlukan kemudahan dan penggunaan kuasa yang rendah. Litar mod campuran mempunyai kewujudan kedua-dua litar analog dan digital di dalam cip yang sama dan adalah berkemungkinan memperolehi litar digital rendah voltan di dalam teknologi pengecilan moden. Walaubagaimanapun, perkara yang sama tidak selalunya benar bagi litar-litar analog disebabkan kekangan aras hingar peranti dan voltan ambang (V_T) MOSFET. Oleh itu untuk litar analog wujud bersama pada substrat yang sama dengan sistem digital dan berkongsi voltan bekalan, operasi litar analog dalam persekitaran voltan rendah adalah penting.

Objektif kajian ini adalah merekabentuk litar S/H bervoltan-rendah, berprestasi tinggi yang akan memberi perhatian kepada masalah-masalah di atas. Sesuatu litar suis kapasitor S/H tipikal memerlukan penguat, suis-suis dan kapasitor. Penguat baharu telah direkabentuk menggunakan tahap tunggal pembezaan sepenuhnya kaskod berlipat bervoltan rendah penguat transkonduktans operasi (OTA) yang mempunyai pulangan tinggi dan kelajuan tinggi; teknik peningkatan gain telah digunakan bagi meningkatkan capaian OTA. Teknik ini tidak mempengaruhi kelajuan tahap tunggal.

Suis-suis gerbang transmisi menggunakan peranti-peranti CMOS, yang mempunyai lineariti dan kelajuan lebih tinggi berbanding suis MOS tunggal, telah direkabentuk untuk digunakan di dalam litar S/H. Suis-suis dioperasi oleh penjana jam dengan dua isyarat-isyarat jam yang tidak bertindih yang mempunyai peningkatan dan penurunan rendah yang menawarkan hingar rendah bagi litar S/H tersebut. Jam tersebut direkabentuk dengan 77.17ps masa peningkatan dan penurunan bagi mengurangkan kesilapan-kesilapan panduan suis-suis MOS yang akhirnya menghasilkan lineariti tinggi.

Litar S/H telah direkabentuk beroperasi menggunakan voltan bekalan 1.8V di dalam teknologi 0.18 μ m. Kadar pengumpulan adalah 40MSPS dengan julat dinamik bebas andaian (spurious free dynamic range – SFDR) 65.7dB dan SNR 70dB.

ACKNOWLEDGEMENTS

First and foremost, I would like to express my sincere appreciation to my supervisor, Prof. Sudhanshu Shekhar Jamuar, to whom I am deeply indebted. His guidance, support, encouragement, availability, along with his understanding were essential to the completion of my degree

I would like to thank the members of my supervisory committee, Prof. Mohamed Adzir Mahdi, and Dr. Mohd Rais Ahmed for their valuable time , support and also agreeing to be on my committee.

I would also like to thank Ng menchin, for his inspiring knowledge of analog circuit design. His constant desire for excellence in analog IC designs.

For their invaluable guides and assistance at the beginning of my study. I would like to thank all members of the wireless Lab and technicians present and past.

Many people at faculty of Engineering and the library of UPM were helpful in my constant quest for knowledge, and for doing their work such a great ship, and helping me out when I needed it.

I would also to give a heartfelt thanks to all members of the health center of UPM for their high care , strong help and the expertness during my sickness, also for the health center management for their highly cooperation and their support during my hospitalized in SERDANG Hospital.

I would like to give great and special thank to the best of my friends, Nidhal Odeh, and Ahmed Hussein for their strong support, and good time we had spent together.

Also for everybody helped me in my study from the beginning till now.



APPROVAL

I certify that an Examination Committee has met on **25/6/2009** to conduct the final examination of Wael A Y Alihasan on his Master of Science thesis “Design of Low Voltage Sample and Hold Circuit in 0.18 μ m CMOS Technology” in accordance with the Universities and University Colleges Act 1971 and the Constitution of the University Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Master degree. Members of the Examination Committee are as follows:

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DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.

WAEEL A Y ALIHASAN

Date:

TABLE OF CONTENTS

DEDICATION	II
ABSTRACT	III
ACKNOWLEDGEMENTS	VIII
APPROVAL	IX
DECLARATION	XI
LIST OF TABLES	XV
LIST OF FIGURES	XVI
LIST OF ABBREVIATIONS/ SYMBOLS	XIX
1 INTRODUCTION	1
1.1 Background	1
1.2 Motivation	4
1.3 Objectives	4
1.4 Research Contributions	5
1.5 Thesis organization	5
2 LITERATURE REVIEW	7
2.1 Wireless receiver architectures	7
2.2 Analog to digital Converter (ADC) Architectures	11
2.2.1 Oversampling ADC	12
2.2.2 Flash ADC	13
2.2.3 Two-Step Flash ADC	14
2.2.4 Pipeline ADC	15
2.3 Pipeline ADC building blocks	17
2.3.1 Sub- Analog to Digital Converter	17
2.3.2 Multiplying Switched Capacitor Digital to Analog Converter (MDAC)	18
2.3.3 Digital Error Correction	19
2.3.4 Operation Transconductance Amplifier (OTA)	21
2.3.5 The Previous Work in Operational Transconductance Amplifier (OTA)	26
2.3.6 Sample and Hold Circuit	27
2.4 MOSFET Switches	30
2.4.1 Single MOS switch	31



2.4.2	Transmission Gate switch (TG)	32
2.4.3	Precision of MOS switches	34
2.4.4	Cancellation of MOS Switches Errors	35
2.4.5	Bootstrapped switch	36
2.5	Conventional Architectures of Sample and Hold (S/H)	38
2.5.1	Open loop Architecture	38
2.5.2	Closed Loop Architecture	39
2.5.3	Current-Multiplexed Architecture	40
2.5.4	The previous work in S/H Circuit	42
2.6	Low Voltage Low Power Design	43
2.7	Limits a Low Supply Voltage Usage	44
2.8	Techniques used for low-power low-voltage circuit design	45
2.8.1	Sub Threshold Operation	46
2.8.2	Bulk drive MOSFET	47
2.8.3	Self-Cascode Approach	47
2.8.4	Floating Gate MOSFET	48
2.9	Conclusion	48
3	METHODOLOGY	50
3.1	Finding specifications of the operational Transconductance Amplifier (OTA)	53
3.1.1	Signal levels and sampling capacitors	53
3.1.2	Settling time of the OTA	55
3.1.3	Slew Rate (SR)	55
3.1.4	Load capacitance	56
3.1.5	Unity Gain Frequency	57
3.1.6	DC-gain	58
3.1.7	Phase Margin	59
3.2	Design of Operational Transconductance Amplifier (OTA)	59
3.2.1	Design of Gain Boosting Amplifier	63
3.3	Bias Circuit Network	67
3.4	Sample and hold Circuit (S/H)	68
3.5	Design of Transmission Gate (TG) Switch	71
3.6	Clock Generator	72
3.7	Summary	74
4	SIMULATION RESULTS	75

4.1	OTA Architecture Simulation	75
4.2	Clock Simulation	84
4.3	Sample and Hold Simulation Result	88
4.4	Conclusion	93
5	CONCLUSION AND FUTURE WORKS	94
5.1	Introduction	94
5.2	Conclusion	94
5.3	Suggestions for Future Work	96
	APPENDIX 1	97
	APPENDIX 2	99
	APPENDIX 3	101
	REFERENCES	103
	BIODATA OF STUDENT	108
	PUBLICATIONS	109



LIST OF TABLES

Table	Page
2.1: Comparison of ADC Architecture	16
2.2: Performance comparison for different OTA's architectures [Razavi, 2001]	25
3.1: Specification of Track and Hold Circuit	51
4.1: Transistors Size of the Main OTA	76
4.2: Transistors Size of PMOS Gain Boosting OTA	77
4.3: Transistors Size of NMOS Gain boosting OTA	78
4.4: NMOS OTA	79
4.5: PMOS OTA	80
4.6: OTA Specifications	84
4.7: Clock Generator Size	88
4.8: Transmission Gate Switch Size	90
4.9: S/H Circuit Specifications	92

LIST OF FIGURES

Figure	Page
1.1: An Ideal wireless Radio receiver	2
1.2: ADC architecture is a compromise between resolution and speed	3
2.1: Categories of Wireless Receivers	7
2.2: Single Conversion Heterodyne	9
2.3: Dual-Conversion Heterodyne Receiver	10
2.4: Direct Conversion Receiver (Homodyne)	10
2.5: First Order Oversampling Converter	12
2.6: Flash ADC	13
2.7: Two-Step Flash ADC [Baker, 1997]	14
2.8: Pipeline ADC [Goes, 1998]	15
2.9: MDAC with two phases:(a) sampling and (b) residue amplification	19
2.10: Pipeline ADC with Digital Error Correction	20
2.11: Telescopic cascode OTA architecture	22
2.12: Folded Cascode OTA	23
2.13: Two Stages Amplifier	24
2.14: Fully Differential Folded Cascode with Gain Boosting OTA	25
2.15: Simple Implementation of S/H	27
2.16: Ideal wave Form of an Input Signal and Ideal Output Signal	29
2.17: Wave Form of Real S/H	29
2.18: MOS Switch	31
2.19: Transmission Gate Switch	33
2.20: a, b, c are On-Resistance of PMOS, NMOS and TG switches respectively	33



2.21: MOS Switch Charge Injection	34
2.22: Clock Feedthrough	35
2.23: Basic S/H with Dummy Transistor	35
2.24: Bottom Plate Sampling Circuit	36
2.25: Bootstrapped Switch circuit	37
2.26: Track and hold phase	37
2.27: Clock Scheme of the Bootstrapped Switch	38
2.28: Open Loop S/H Architecture	39
2.29: Closed Loop Architecture	40
2.30: Current-Multiplexed Architecture	41
2.31: Current Mirror Based on Sub Threshold MOSFETs	46
2.32: Bulk-Driven MOSFET	47
2.33: Self Cascode Structure and Equivalent Transistor	48
3.1: Algorithm of Design Procedure	52
3.2: Peak-Peak Voltage(V_{PP}) of the Input Signals (a,b), Full-Scale Voltage signal(c)	55
3.3: S/H with Parasitic Capacitance	56
3.4: (a) Folded Cascode, (b) Telescopic OTAs	61
3.5: Proposed OTA with common mode feedback circuit	61
3.6: Fully Differential OTA with PMOS input transistors	64
3.7: Fully Differential OTA with NMOS input transistors	65
3.8: The Main Amplifier With the Gain Boosting Amplifiers	66
3.9: Bias Network	68
3.10: Switch Capacitor S/H	69
3.11: Sampling mode	69



3.12: Amplification mode	70
3.13: TG switch	72
3.14: Clock Generator	72
3.15: Schematic of Clock	73
3.16: (a) Inverter, (b) NAND Circuits	73
4.1: DC Output of OTA	81
4.2: Bode diagram of AC-Response of the OTA	82
4.3: Open Loop configuration	83
4.4: Circuit used to measure the Settling Time (Closed Loop)	83
4.5: Settling Time of the OTA	84
4.6: Output of the Clock Generator	85
4.7: Difference Between ϕ_1 , ϕ_{1a}	86
4.8: The Rise Time of the Clock Signal	87
4.9: Fall time of the Clock Signal	87
4.10: Output Tracking Input in S/H Circuit(10MHz)	89
4.11: Output Tracking input in S/H circuit (15)MHz	90
4.12: Output Tracking Input in S/H Circuit (20MHz)	91
4.13: Output Spectrum	92



LIST OF ABBREVIATIONS/ SYMBOLS

ADC	Analog to Digital Converter
BSIM	Berkeley Short-Channel IGFET Model
CMOS	complementary metal oxide semiconductor
DAC	Digital to Analog Converter
DC	Discrete Current
DSP	Digital signal processing
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LO	Local Oscillator
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NMOS	Negative Channel Metal Oxide Semiconductor
OTA	Operation Transconductance Amplifier
PMOS	Positive Channel Metal Oxide Semiconductor
RF	Radio Frequency
RMS	Root Mean Square
S/H	Sample and Hold
SC	Switch Capacitor
SDR	Software Defined Radio
SPICE	Simulation Programme with Integrated Circuit Emphasis
TG	Transmission Gate



F_s	Sampling rate
F_{in}	Input signal bandwidth
μ_n	Electron mobility
C_{OX}	Gate oxide capacitance per area
V_G	Gate voltage
g_m	MOSFET Transconductance
C_H	Sampling capacitor
R_{on}	ON-resistance of the MOS switch
SR_{max}	Maximum Slew rate
V_{DS}	The Volt between the drain and the source of the transistor
V_{OD}	Over drive voltage
V_{Ref}	Reference voltage
V_{dd}	Supply voltage
V_{in}	Source voltage
V_{out}	Output voltage
V_{th}	Threshold voltage
t_{ac}	Acquisition time
C_c	Compensation capacitor
K	Boltzmann constant
L	Effective length of the device
T	Temperature
W	Effective width of the device
SR	Slew rate

CHAPTER 1

INTRODUCTION

1.1 Background

There has been multi fold increase in the applications of digital signal processing (DSP) in all works of life over past few decades. This has been more pronounced and visible due to its reconfigurability, enhanced functionality and low power consumption. Since most of the natural phenomena are analog, an interface is needed between analog signal and the DSP, to implement the full capability of digital signal processor. The bridging between the real world analog signal processing and DSP blocks is implemented by using Analog to Digital Converters (ADCs).

With the rapid advancement in CMOS fabrication technology, more and more signal processing functions are being implemented in the digital domain, and the analog to digital boundary is moving towards the antenna. There are several types of ADC used in wireless receivers, each one has different specifications, different use which yield in different architectures. Figure 1.1 shows example of block schematic of an ideal futuristic wireless receiver, in which the analog components (the band pass filter and the low noise amplifier (LNA)) are limited to antenna. The analog to digital conversion is carried out immediately after RF stage and the signals are processed digitally to provide flexibility in receiver design [Hickling, 2005].

Since different wireless standards have different channel bandwidth and dynamic range requirement, single wide bandwidth analog to digital converter with wide dynamic range is required. ADC's can be categorizing into two categories depending on the sampling rate.

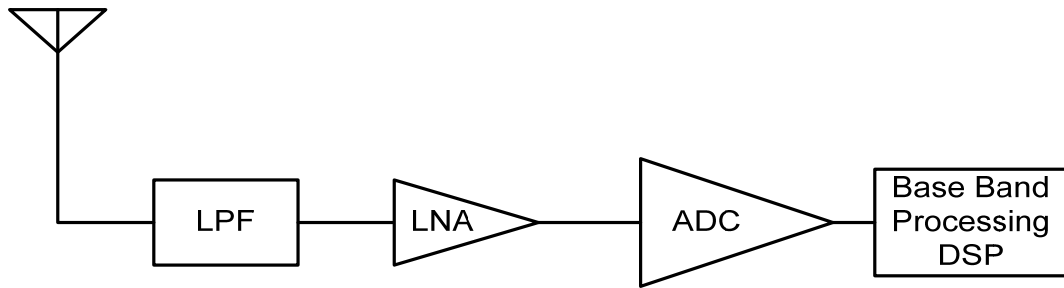


Figure 1.1: An Ideal wireless Radio receiver

The first category is with their sampling rate double of bandwidth input signal which is called Nyquist rate ADC's. The second type its wit sampling rate much higher than the input signal.

High resolution high speed data converters usually consume large power and integrating them with other blocks in RF transceiver is a major challenge with minimal power consumption [Zhang. et., al.,2008]. High speed Nyquist rate CMOS ADC with reasonable power consumption is available [Adeniran, 2005], but their resolution is limited. Low power consumption and low voltage operation are two important design constraints in portable system. The scaling down of CMOS technologies and system on chip (SoC) design requirements have driven researcher to investigate new circuits for ADC.

This thesis will focus on the pipeline ADC; it is a popular Nyquist rate ADC architecture for data conversion schemes having a compromise between speed and accuracy. Figure 1.2 shows the relation between the resolution and the ADC architecture. The sigma delta oversampled ADC has the best resolution but its speed is the lowest. Flash ADC is high speed architecture, but it has very low resolution. The recent trend is the pipeline ADC [Kester, 2005], which has reasonable resolution of 8 to 14 bits and sampling rate between 1MHz to 200MHz. Although

the pipeline architecture is inherently not as fast as a flash scheme, its serial nature results in a linear scaling of power and area with resolution, opposed to the exponential scaling which occurs in a flash. The pipeline architecture becomes a more attractive solution for resolution higher than 9 bits. Similarly, for very high resolution schemes sigma delta architectures are generally used, however the over-sampling nature of such schemes limits the maximum speed to a fraction of the fastest possible sampling rate. The concurrent nature of a pipeline removes the over-sampling required in effect converting the over-sampling speed limit into a latency problem.

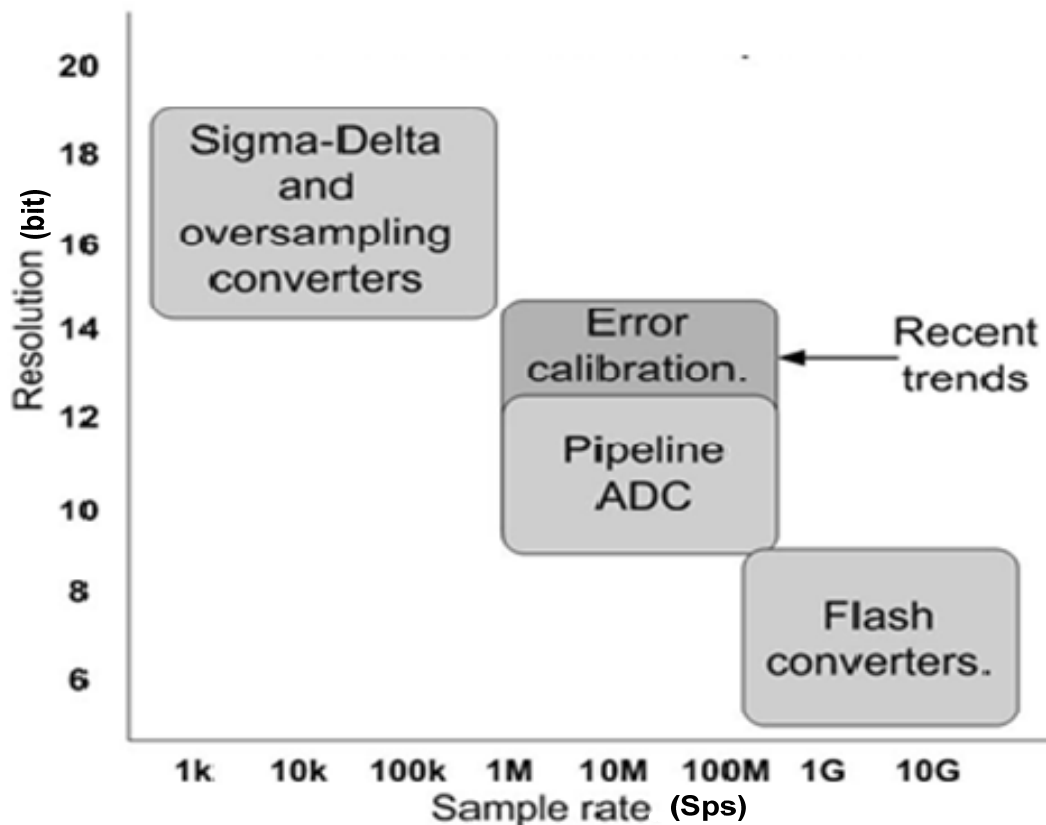


Figure 1.2: ADC architecture is a compromise between resolution and speed [Kester, 2005].

Sample and Hold (S/H) circuit is the most critical circuits in pipeline ADC. It allows the output of each stage to be used immediately to process its input sample. S/H circuit provides a constant output to the input of ADC, thus reducing the constraints

of high speed ADC and increasing the bandwidth. The noise and the distortion of the ADC are also reduced. This thesis addresses the design of low voltage high performance sample and hold circuit for use in 10 bit, 40 MSPs pipelined ADC.

1.2 Motivation

In mixed mode circuit design now days digital and analog systems are routinely integrated onto single chips. Digital circuits commonly employ various techniques, including low-voltage supply, to reduce power consumption. In order to have low power consumption in mixed mode circuit, it is desirable that analogue circuits must also be designed with low voltage supply and should consumes low power. Conventionally designed low supply voltage amplifier for Sample and Hold circuits suffer from performance trade-offs [Tsung-Sum Lee, 2005], resulting in low bandwidth and low dynamic range. This is because the design of any analogue circuit is a trade-off of various performance parameters such as power dissipation, supply voltage, gain, linearity and noise. All these parameters are important but for any one design, improving one parameter is likely to degrade another. The S/H circuit would require high performance operational Transconductance amplifier, transmission gate switch and a clock generator.

1.3 Objectives

The objectives of this research are:

1. To design and simulate low-voltage high- performance Operational Transconuctance Amplifier (OTA).
2. To design and simulate transmission gate switch.