UNIVERSITI PUTRA MALAYSIA

DESIGN OF QUATERNARY LOGIC CARRY LOOK-AHEAD ADDER

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DESIGN OF

QUATERNARY LOGIC CARRY LOOK-AHEAD ADDER

By

Nosratollah Lohrasb

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Partial Fulfillment of the Requirements for the Degree of Master of Science

March 2009

Dedicated to the Lord of my life

Who never leaves me alone and gives me the strength

Abstract of thesis presented to the Senate of
Universiti Putra Malaysia
in fulfillment of the requirement for the Degree of
Master of Science

DESIGN OF

QUATERNARY LOGIC ARRAY CARRY OOK-AHEAD ADDER

By

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March 2009

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In today's state-of-the-art VLSI technology, binary number system has been the choice for designing digital subsystems. Although technology development has made down scaling of devices possible, which in turn has resulted in a remarkable increase in density and functionality of VLSI systems, there are also significant drawbacks associated to the conventional binary number based system implementations.

As the number of devices in VLSI circuits increases to billion of transistors in a chip area of mm^2, interconnection between the active devices both on chip and outside of a chip becomes considerably complicated. In a typical VLSI chip, about 70 percent of the chip area is occupied by interconnections whereas just 10 percent of the chip area is devoted to the devices and the remaining 20 percent is used for insulation.

In this situation, multiple valued logics have attracted a considerable attention of researchers as a solution to overcome the above mentioned

problem. Since fewer digits are required to represent a number in higher radices than in the binary number system, multiple valued logic circuits have the potential to minimize the number of interconnections.

This thesis presents voltage-mode quaternary (4-valued) logic carry look-ahead adder design using Silicon-On-Insulator (SOI) MOSFETs. The choice of adder subsystem is made because addition operation is the most frequently used operation in a general purpose system and in application specific processors. Further more, the other operations like subtraction, multiplication and division are based on addition operation of the arithmetic unit. In this study, an efficient logic to realize 4-valued logic addition operation is proposed. The presented method is in conjunction with binary logic concepts and is easily developed for look-ahead logic. Following the proposed method has resulted in logic circuits with shorter gate depth and faster speed of operation as compared to what the other researchers have proposed.

To meet the design requirements of the proposed low-voltage low-power circuits, multiple threshold voltage SOI MOSFETs are used. This choice is made because of their capability to operate at low power supply voltages and their ability to remain at the adjusted threshold voltages while presenting better subthreshold characteristics compared to the bulk MOSFETs.

The proposed half and full adder blocks are divided into a few subblocks which could be considered as primitive gates. Transistor-Resistor Logic is used to implement each of them. Spice simulations have been performed on the proposed logic subblocks and their transient behaviors have been

studied. Finally, the propagation delay, power consumption and overall performance of the proposed circuits are compared with other adder circuits proposed by other researchers. The presented adder circuits in this work have shown up to 58% reduction in critical propagation delay and 20% less power dissipation resulting in 64% reduction in power-delay product in comparison with other reported work. When compared to the binary logic carry look-ahead adder using the same technology (SOI), 54.39% improvement in power dissipation was achieved.

Abstrak tesis yang dibentangkan kepada senat
Universiti Putra Malaysia
untuk memenuhi keperluan ijazah
Master Sains

REKABENTUK PENAMBAH PEMBAWA PANDANG-DEPAN

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Dalam teknologi VLSI terkini, sistem nombor perduaan perupakan pilihan untuk merekabentuk sub-sistem digital. Walanpun pembangunan teknologi telah memungkinkan penskalaan peranti dan seterusnya telah menghasilkan satu penambahan yang luar biasa dalam aspek kepadatan dan kefungsian sistem VLSI, namun terdapat kelemahan yang ketara mengenai pelaksanaan sistem yang berorientasikan nombor perduaan yang konvensional.

Dengan bilangan peranti dalam litar VLSI bertambah kepada bilion transistor dalam satu kawasan cip yang saiznya dalam mm^2, sambungan antara peranti aktif samada yang berada di dalam atau di luar cip menjadi sangat rumit. Dalam cip VLSI yang biasa, lebih kurang 70 peratus daripada kawasan cip adalah diliputi oleh rantaian sambungan, hanya 10 peratus

daripada kawasan cip terdiri daripada peranti dan 20 peratus lagi digunakan untuk penebatan.

Dalam situasi ini, logik berbilang nilai telah menarik perhatian para penyelidik sebagai salah satu penyelesaian untuk mengatasi masalah tersebut. Memandangkan beberapa digit diperlukan untuk mewakili satu nombor dalam radiks yang lebih tinggi berbanding dengan sistem nombor perduaan, logik berbilang nilai mempunyai potensi untuk mengurangkan bilangan rantaian sambungan.

Tesis ini membentangkan struktur logik penambah pembawa pandang-depan mod voltan perempatan (4 nilai) dengan menggunakan Silikon-Atas-Penebat (SOI). Subsistem penambah ini dipilih sebab operasi tambah merupakan operasi yang paling kerap digunakan dalam sistem gunaan umum dan juga dalam aplikasi pemproses khusus. Tambahan lagi, operasi-operasi yang lain seperti tolak, darab dan bahagi adalah berasaskan operasi tambah. Dalam kajian ini, logik yang efisyen untuk merealisasikan operasi tambah 4-nilai telah dicadangkan. Kaedah yang dibentangkan adalah selari dengan konsep logik perduaan dan ianya mudah dibangunkan untuk logik pandang-depan. Menggunakan kaedah tersebut, litar logik dengan kedalaman get yang lebih cetek dan kelajuan operasi yang lebih cepat telah dihasilkan berbanding dengan apa yang telah dibentangkan oleh penyelidik-penyelidik yang lain.

Untuk memenuhi syarat-syarat rekabentuk litar dengan voltan dan kuasa rendah, SOI MOSFET dengan voltan ambang berbilang digunakan. Pilihan

ini dibuat disebabkan keupayaan mereka untuk beroperasi pada bekalan voltan rendah dan berada tetap pada voltan ambang yang diselaraskan serta mempunyai ciri-ciri sub-ambang yang lebih baik berbanding dengan MOSFET pukal.

Blok penambah separuh dan penuh yang dicadangkan dibahagi kepada beberapa sub-blok yang boleh dianggap sebagai get primitif. Logik Transistor-Perintang digunakan bagi merealisasikan setiap daripada mereka. Simulasi telah dilaksanakan pada sub-blok bagi logik yang dicadangkan dan kelakuan seketika mereka telah dikaji. Akhir sekali, tempoh lengah perambatan, penggunaan kuasa dan prestasi keseluruhan litar yang dicadangkan dibandingkan dengan hasil kajian penyelidik yang lain. Litar penambah dalam kajian ini menunjukkan penurunan lambatan perambatan kritikal sehingga 58% dan pelepasan kuasa sebanyak 20% menghasilkan 64% penurunan hasil darab kuasa-lambatan dibandingkan dengan hasil kajian yang lain. Apabila dibandingkan dengan penambah penbawa pandang-depan logik perduaan menggunakan teknologi yang sama (SOI), 54.39% penambah baikan dalam pelepasan kuasa dapat dicapai.

ACKNOWLEDGEMENTS

I have God to thank for letting me to become a student and for giving me this fortune to get closer to him. Love you God, as much as very means and as long as eternity lasts.

I would like to take this opportunity to express my sincere gratitude and appreciation to my parents Mr. Ebrahim and Mrs. Leila Lohrasb for giving me life and making me what I am right now.

I would like to express my sincere gratitude to my supervisor Dr. Roslina Mohd. Sidek and my advisor Prof. Sudhanshu Shekhar Jamuar for giving me guidance in studies and on the professional front. Thanks for your valuable time, suggestions and ideas.

I wish to express my appreciation to the numerous individuals who have contributed towards the completion of this thesis.

I certify that an Examination Committee has met on …… to conduct the final examination of Nosratollah Lohrasb on his degree thesis entitled “DESIGN OF QUATERNARY LOGIC CARRY LOOK-AHEAD ADDER ” in accordance with Universiti Pertanian Malaysia (Higher Degree) Act 1980 and Universiti Pertanian Malaysia (Higher Degree) Regulations 1981. The Committee recommends that the candidate be awarded the relevant degree. Members of the Examination Committee are as follows:

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DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations, which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.

NOSRATOLLAH LOHRASB

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TABLE OF CONTENTS

		Page
DEDICATION		ii
ABSTRACT		iii
ABSTRAK		vi
ACKNOWLEDGEMENTS		ix
APPROVAL		x
DECLARATION		xii
LIST OF TABLES		xv
LIST OF FIGURES		xvi
LIST OF ABBREVIATIONS		xix
CHAPTER		
I	**INTRODUCTION**	1
	1.1 Research Motivation	4
	1.2 Research Objectives	6
	1.3 Thesis Outline	6
II	**LITERATURE REVIEW**	8
	2.1 Implementing Multiple Valued Logics Circuits	8
	2.2 Voltage-Mode Circuits	10
	2.2.1 Single Threshold Voltage Devices Circuits	11
	2.2.2 Multiple Threshold Voltage Devices Circuits	18
	2.3 Summary	26
III	**DESIGN OF QUATERNARY LOGIC ADDERS**	28
	3.1 Quaternary Logic Half Adder	28
	3.2 Threshold Voltage Adjustment for SOI MOSFETs	32
	3.3 Circuit Implementation for Half Adder Block	37
	3.3.1 Inverter Circuit	37
	3.3.2 Half Adder Carry (HAC) Generator Circuit	39
	3.3.3 Truncated Sum (TSUM) Circuit	42
	3.3.4 PSUM Circuit	46
	3.3.5 Mix Circuit	48
	3.4 Full Adder Block	49
	3.4.1 Successor Circuit	51
	3.4.2 Carry Out Generator Circuit	53
	3.5 Carry Look-Ahead Adder (CLA) Blocks	54
	3.6 Resistors and Resistors' Replacements	58
IV	**SIMULATION RESULTS**	60
	4.1 Inverter	61
	4.2 Half Adder Carry (HAC) Generator	61
	4.3 Simulation Results of TSUM and PSUM	62
	4.4 Half Adder	64
	4.5 Full Adder	67
	4.6 Carry Look-Ahead Adder (CLA) Blocks	72

4.7 Propagation Delay of CLA Blocks 77
4.8 Power Dissipation in quaternary CLA blocks 74
4.9 Four-Digit Quaternary Adder 79

V DISCUSSION 83
5.1 Design Specification 83
5.2 Comparison with Binary Logic Adders 85
5.3 Comparison with Other Proposed Adders 92
5.4 Summary 95

VI CONCLUSION AND FUTURE WORK 97
6.1 Conclusion 97
6.2 Future Work 99

REFERENCES 101

APPENDICES 108

BIODATA OF STUDENT 146

LIST OF TABLES

Table		Page
2.1	Correspondence between logical values and voltage levels	19
2.2	Parameters of 1.5 μm technology MOSFET devices	20
2.3	Threshold voltages of the transistors used in Figure 2.9	23
3.1	Truth table of quaternary logic half adder	31
3.2	Process parameters of the basic SOI device	34
3.3	Silicon thin film doping concentration and related threshold voltages	36
3.4	Truth table of HAC	40
3.5	Simplified form of Table 3.4	41
3.6	Truth table of TSUM function	43
3.7	Truth table of PSUM operation	47
3.8	Results of half addition operation	50
3.9	Truth table of level shifter in the case where $C_{in}=1$	52
4.1	Description of simulation inputs	62
4.2	Description of simulation inputs and outputs	72
4.3	Description of simulation inputs and outputs when measuring the maximum propagation delay	73
5.1	Design specifications of the proposed 4-bit quaternary logic CLA	85
5.2	Tabulated comparison results	88
5.3	Area estimation for binary and quaternary logic CRAs	90
5.4	Comparing binary logic and quaternary logic CLA both using SOI technology	92
5.5	Comparing current-mode and voltage-mode adders	93
5.6	Quaternary adders' comparison results	95

LIST OF FIGURES

Figure		Page
1.1	Reduced interconnection area by use of higher radices	3
2.1	Ternary inverter circuit	11
2.2	Splitting the function f(x) to n subfunctions	12
2.3	Typical circuit implementation using literal splitting technique	13
2.4	Use of pass transistor logic to realize quaternary function Z	15
2.5	The logic diagram of a nanoblock	16
2.6	Implementation of ternary logic (a) minimum and (b) maximum operators using CAEN technology	17
2.7	Minimum and maximum operators' circuits	20
2.8	Quaternary logic half adder circuit implementation	21
2.9	Implementing $\overline{\text{Min}}$ operator using CMOS circuit	23
2.10	Inverter operator: circuit schematic (a) and transfer characteristic (b)	25
2.11	Cyclic operators	26
3.1	Implementation of a ternary logic full adder using standard Method	30
3.2	Block diagram of the proposed quaternary logic half adder	32
3.3	Cross section of the FD SOI MOSFET	35
3.4	Quaternary logic inverter circuit	38
3.5	Karnaugh map of HAC	40
3.6	Half adder carry generator circuit	41
3.7	TSUM operator circuit	44
3.8	PSUM operator circuit	48
3.9	Schematic diagram of Mix circuit	49
3.10	Level shifter block	51

3.11	Successor circuit, SUM result generator	52
3.12	Carry out generator circuit	53
3.13	Gate level implementation of C_0	56
3.14	Gate level implementation of C_1	56
3.15	Gate level implementation of C_2	57
3.16	Gate level implementation of C_3	57
3.17	Schematic diagram of a four bit quaternary logic CLA	57
4.1	Waveform of inverter circuit	61
4.2	Waveform of HAC generator circuit	63
4.3	Waveform of $\overline{\mathrm{TSUM}}$ circuit	65
4.4	Waveform of $\overline{\mathrm{PSUM}}$ circuit	66
4.5	Waveform of the quaternary logic half adder circuit	69
4.6	Waveform of the quaternary logic full adder block	70
4.7	Average power dissipation of the quaternary logic full adder	61
4.8	The input waveforms of the quaternary logic CLA blocks	74
4.9	The output waveforms of the quaternary CLA blocks ($Cin = 0$)	75
4.10	The output waveforms of the quaternary CLA blocks ($Cin = 1$)	76
4.11	Propagation delay of CLA blocks	78
4.12	Power dissipation in the four bit quaternary logic CLA	79
4.13	Power consumption in a four bit quaternary CLA (a) and an 8-bit binary CLA (b) both using the same technology	81
4.14	Critical propagation delay (a) and mean power dissipation (b) of the four single bit quaternary adder	82
5.1	Five 2- bit binary numbers adder schematics	86
5.2	Adding four single bit quaternary number	86
5.3	Four bit quaternary logic carry-ripple adder	89

5.4 Distribution of circuit, insulator and interconnections on a same chip : (a)binary (b) quaternary logic design 91

LIST OF ABBREVIATIONS

VLSI	Very Large Scale Integration
IC	Integrated Circuit
ILD	Inter Layer Dielectric
RC	Resistor-Capacitor
CLA	Carry Look-ahead Adder
CAEN	Chemically Assembled Electronic Nanotechnology
CNFET	Carbon Nanotube Field Effect Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
SOI	Silicon On Insulator
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
HAC	Half Adder Carry
HAS	Half Adder Sum
TSUM	Truncated SUM
PDP	Power-Delay-Product
PD	Partially Depleted
FD	Fully Depleted
LDD	Lightly Doped Drain

CHAPTER 1

INTRODUCTION

The remarkable increase in the density of Very Large Scale Integrated (VLSI) circuits is the result of advanced Integrated Circuits (IC) fabrication processes and the development of automated design tools. As the number of devices accommodated on VLSI chips increases, many problems also arise. For instance, the interconnection between devices inside and outside a chip becomes significantly complicated and the area occupied by interconnections increases in haste. Aggressive interconnect scaling following Moore's law introduces many challenges in integration, performance and reliability. Inappropriate routing results in a larger chip size and cause timing and cross-talk problems. In deep submicron designs these problems are of outstanding importance.

The partial solutions to this problem in today's VLSI circuits are to use several metal layers, flip-chips and other methods. Although improvement in metal stack material have enabled industry to reduce interconnect resistance in narrow lines and at the same time changes in interlayer dielectric (ILD) material have lowered the line to line capacitance resulting in Resistor-Capacitor (RC) delay improvement and thus interconnect power consumption, however, deep submicron technology introduces formidable integration and reliability challenges such as higher narrow Cu line resistivity, higher current density and inferior thermo-mechanical properties which must be overcome.

It is well known that the binary number system is the leading choice for conventional voltage-mode design of digital systems [21]. However, in a typical binary number system based VLSI circuit about 70 percent of chip area is occupied by interconnections which occupy a large portion of physical area even when it is not in use [11, 22]. Therefore the interconnections will be more efficient if several levels of logic are injected into a single wire, as in multiple valued logics. Dissimilar to binary logic, multiple valued logics require more than two discrete levels of logic signals and allow more than two logical concepts to exist in a logic system. Thus, the direct benefit of such logics is the improved overall information efficiency. It is because each r-valued signal can carry $\log_2 r$ times more information than a binary signal does. As a result the routing area is reduced on a logarithmic scale-$\log_r 2$-as r increases. This reduction in number of interconnections and area of a chip is understood by referring to Figure 1.1. As can be seen, the routing area of a 4-valued logic design is two times smaller than the corresponding binary logic system.

The choice of the most favorable logic radix in term of implementation cost has been also studied by some researchers. According to S. L. Hurst [27], the circuit implementation cost is decreasing with increasing logic radix and according to C.M. Allen and D. Gioven [28], the optimal radix is greater than Euler constant, $e \approx 2.7$. Since in practice the radix r is an integer, it comprehends that the more advantageous radix must be at least 3 or in other words ternary logic. On the other hand conversion with binary is most efficient if special radices are chosen in such a way that no information is lost or left unused [11].

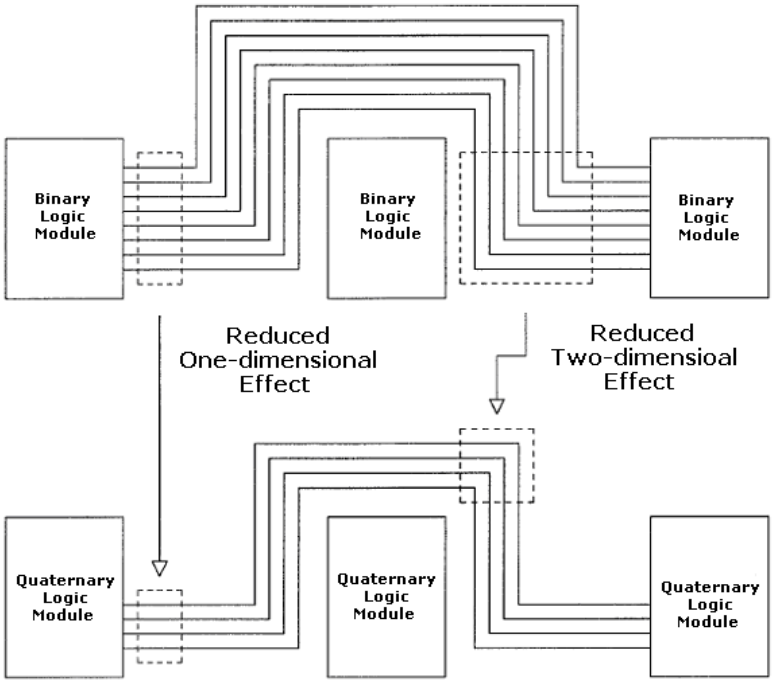

Figure1.1: Reduced interconnection area by use of higher radices

These radices are the exact power of two, that are 2^n, for n=1, 2, etc. Although higher radices give the possibility of more information per bit, nevertheless, technology restrictions limit the value of r. Regardless of the use of current-mode or voltage-mode approaches, the most practical choice of radix particularly for voltage-mode circuits is r=4.

In spite of the advantages of current-mode circuits to realize arithmetic functions, however their relatively large power consumption, their associated peripheral circuits and way of communicating with voltage signals retain as their significant drawback. In contrast, voltage-mode circuits are not suffering such problems and voltage-mode multiple valued logics designs have been made for commercial purposes. In 1997, Intel unveiled the first two bit /cell Strata Flash memory device based on their multiple levels per cell technology [33].

In summary, the main reason for using multiple valued logics designs in VLSI circuits is that the higher radices designs use the chip area more efficiently through the increase in functionality and the reduction in the number of wirings. This reduction in the number of interconnections requires fewer pins on IC packages and therefore reduced routing complexity.

1.1 RESEARCH MOTIVATIONS

Despite the above mentioned advantages of multiple valued logics designs, today's digital designs are still dominated by binary logic. Exploring the voltage-mode multiple valued logics designs reveals that there are problems making the development of multiple valued logics slow down and hindering them from growth. For instance, inefficient logics proposed to realize such functions, low noise margin, signal degradation, large circuits and other issues. Thus it has been difficult to convince digital system designers to replace multiple valued logics modules in data processing systems before these problems are overcome.

One of the fundamental operations in digital processing systems is addition operation. Addition is the most frequently used operation in processors and many VLSI designs. Moreover, since the other arithmetic operations such as subtraction, multiplication and division usually rely on addition operation, adders are seen as obligatory part of the arithmetic units. Addition is also a very crucial operation because it usually involves a carry ripple step which must propagate a carry signal from less significant bits to more significant bits resulting in a substantial circuit delay [22]. Hence the

adder lies in the critical delay path determining the system overall speed. On the other hand, reducing the power consumption of designed adders has come to prominence in recent times due to the increasing popularity of portable computing and communication systems. Therefore designing efficient adders has always been challenging. Different types of adders have been designed to address the speed and power dissipation and between them, carry look-ahead adder (CLA) is well known as a fast one because of concomitantly generating the carries by the means of look-ahead logic [22, 24]. Although diversity of designing multiple valued logics circuits covers a large spectrum but in particular, quite a few approaches for implementing voltage-mode adders were made.

The most significant reason for slow development of multiple valued logics designs is inefficiency of the proposed logics for realizing multiple valued logics functions. In fact, the logic itself is restricted by technology limitations and the choice of circuit family. The proposed logics to realize voltage-mode multiple valued logics functions have resulted into bulky circuits [5, 6, 8, 10] having relatively large delays and power dissipations. The larger circuits originate from the proposed logics to implement multiple valued operators used in such circuits. Since implementing just a few primitive gates have been possible in some approaches, excess operations are required to do a particular task. This problem in addition to the barriers of reducing supply voltages, are the reasons for large power dissipation.

The overall performance of the voltage-mode multiple valued logics circuits can be tackled from three levels: logic level, circuit level and device level. This thesis aims a novel logic for implementing addition operation at logic