UNIVERSITI PUTRA MALAYSIA

OPTIMIZATION OF DIGITAL ELECTRONIC CIRCUIT STRUCTURE DESIGN USING GENETIC ALGORITHM

CHONG KOK HEN

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OPTIMIZATION OF DIGITAL ELECTRONIC CIRCUIT STRUCTURE DESIGN USING GENETIC ALGORITHM

By

CHONG KOK HEN

Thesis Submitted to the School of Graduate Studies, Universiti Putra Malaysia, in Fulfillment of the Requirement for the Degree of Doctor of Philosophy

November 2008

This work is special dedicated to my wife Kheng Siew,
my daughter Yu En and my son Kai Qian
with love…

Abstract of thesis presented to the Senate of Universiti Putra Malaysia in fulfillment of the requirement for the Degree of Doctorate of Philosophy

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By

CHONG KOK HEN

November 2008

Chairman: **Associate Professor Ishak Aris, PhD**

Faculty: **Engineering**

The complexity of the digital electronic circuit is due to the number of gates used per system as well as the interconnection of the gates. Diminution of the total number of gates used and interconnection in the system would reduce the cost in the design, as well as increasing the efficiency of the overall system. As a result, the higher integration level, the better and the cheaper final product produced.

The conventional digital circuit design method is based on Boolean algebra. There are no specific procedure to choose the right theorem or postulate for the Boolean expression simplification and it is very impractical to design the digital circuits that have more than four variable. Karnaugh map can provide the simple minimization process for Boolean expression, but it encounters difficulties when the variable is more than four.

In this research, Genetic Algorithm (GA) technique is used as a tool to search for the optimal solution for the digital circuit structure. The GA process (Inter Loop GA), crossover operator (Fix Multiple Point Crossover), mutation operator (Random Discrete Mask Mutation) and fitness function (Constraint Fitness and Gate Optimization Fitness) were developed in this research.

The simulator called Optimal Digital Circuit Structure Designer (ODCSD) is also developed in this work. ODCSD is a digital circuit structure design simulation program. Further more, a prototype hardware has been designed and constructed to test the success chromosome string, which called as GA based Logic Implementer (GALI). GALI is programmed by the success chromosome bits obtained from the simulation phase. This chromosome bits are used to set up the gates arrangement in the hardware.

A number of experiments are implemented to design 3-bit, 4-bit, 5-bit and 6-bit circuits. The results show that the proposed method is able to produce the optimized circuit with lesser number of gates compared to the conventional methods. In the future development, the proposed system can be used as the discrete controller when it implemented in the process control application.

Abstrak tesis yang dikemukakan kepada Senat Universiti Putra Malaysia
sebagai memenuhi keperluan untuk ijazah Doktor Falsafah

PENGOPTIMAKAN REKABENTUK STRUKTUR LITAR ELEKTRONIK DIGIT DENGAN MENGGUNAKAN ALGORITMA GENETIK

Oleh

CHONG KOK HEN

November 2008

Pengerusi: Profesor Madya Ishak Aris, PhD

Fakulti: Kejuruteraan

Tahap kompleks sesebuah litar elektronik adalah bergantung kepada jumlah get logik yang digunakan dalam satu sistem dan juga litar penyambungan diantaranya. Dengan mengurangkan bilangan get logik dan meringkaskan litar penyambungan di dalam sistem tersebut, kos rekabentuk boleh dikurangkan, disamping meningkatkan kecekapan kepada keseluruhan sistem. Oleh itu, produk dengan tahap integrasi yang lebih tinggi dan murah boleh dihasilkan.

Cara konvensional untuk merekabentuk litar digit adalah menggunakan algebra Boolean. Tidak ada prosedur yang tertentu untuk memilih teorem yang betul untuk meringkaskan penyataan Boolean dan ia juga tidak sesuai digunakan untuk merekabentuk litar digit yang lebih dari empat pembolehubah. Peta Karnaugh memberikan proses ringkasan yang

senang bagi penyataan Boolean, tetapi ia mengalami kerumitan jika pembolehubah melebihi empat.

Dalam kajian ini, teknik algoritma genetik telah digunakan untuk mencari penyelesaian yang optima bagi struktur litar digit. Tesis ini telah memperkenalkan kajian tentang proses algoritma genetik (Inter Loop Genetic Algorithm), operator penyebrangan (Fix Multiple Point Crossover), operator mutasi (Random Discrete Mask Mutation) dan fungsi ketahanan (Constraint Fitness and Gate Optimization Fitness).

Tesis in juga memperkenalkan simulator "Optimal Digital Circuit Structure Designer" (ODCSD). ODCSD ialah program simulasi untuk mereka litar digit. Selain dari itu, sebuah perkakasan model percubaan telah direkabentuk dan dibina untuk menguji kromosom yang berjaya; model ini dipanggil GA based Logic Implementer (GALI). GALI diprogram oleh bit kromosom yang berjaya di fasa simulasi. Bit-bit kromosom ini digunakan untuk mensetkan susunan get pada perkakasan ini.

Ujikaji-ujikaji yang telah dilaksanakan untuk mereka bentuk struktur litar digit berbit 3, berbit 4, berbit 5 dan berbit 6. Keputusan ujikaji menunjukkan bahawa cara ini dapat menghasilkan struktur litar dengan bilangan get logik yang kurang dibandingkan dengan cara rekabentuk konvensional. Sistem ini boleh digunakan sebagai pengawal diskrik jika ia digunakan dalam bidang kawalan proses di masa depan.

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Special thanks to my beloved wife, Kheng Siew for her patience, encouragements and continuous support.

I certify that a Thesis Examination Committee has met on 24 November 2008 to conduct the final examination of Chong Kok Hen on his thesis entitled "Optimization of Digital Electronic Circuit Structure Design Genetic Algorithm" in accordance with Universities and University Colleges Act 1971 and the Constitution of the Universiti Putra Malaysia [P.U.(A) 106] 15 March 1998. The Committee recommends that the student be awarded the Doctor of Philosophy.

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This thesis was submitted to the Senate of Universiti Putra Malaysia and has been accepted as fulfillment of the requirement for the degree of Doctor of Philosophy. The members of the Supervisory Committee were as follows:

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DECLARATION

I hereby declare that the thesis is based on my original work except for quotations and citations which have been duly acknowledged. I also declare that it has not been previously or concurrently submitted for any other degree at UPM or other institutions.

CHONG KOK HEN

Date: 24 December 2007

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LIST OF ABBREVIATIONS

AI	Artificial Intelligent
BCD	Binary Coded Decimal
CBR	Case Base Reasoning
CF	Constraint Fitness
COF	Constraint Optimization Fitness
EA	Evolutionary Algorithm
EHW	Evolvable Hardware
F-MPX	Fix-Multiple Point Crossover
FPGA	Field Programmable Gate Array
GA	Genetic Algorithm
GALI	Genetic Algorithm Logic Implementer
GOF	Gate Optimization Fitness
GSS	Genetic Synthesis System
GUI	Graphic User Interface
LED	Light Emitting Diode
MGA	Multiobjective Genetic Algorithm
MG	Mentor Graphics
MP	Mutation Pool
NGA	n-Cardinality Genetic Algorithm
ODCSD	Optimal Digital Circuit Structure Designer
PCB	Printed Circuit Board
PFU	Programmable Floating Point Unit
PM	Parallel Multiobjectives

POS	Product of Sum
RDMM	Random Discrete Mask Mutation
RDM	Random Discrete Mask
RWS	Roulette Wheel Selection
SA	Simulated Annealing
SimE	Fuzzified Simulation Evolutions
SGA	Simple Genetic Algorithm
SOP	Sum of Product
SSR	Stochastic Sampling with Replacement
SUS	Stochastic Universal Sampling
XOVDP	Double Point Crossover
XOVDPRS	Double Point Reduced Surrogate Crossover
XOVMP	General Multi Point Crossover
XOVSH	Shuffle Crossover
XOVSHRS	Shuffle Reduce Surrogate Crossover

CHAPTER 1

INTRODUCTION

1.1 Introduction

The complexity of digital electronic circuits is due to the number of gates used per system as well as the interconnection of the gates. Diminution of the total number of gates used and interconnection in the system are able to reduce the cost in the design, as well as to increase the efficiency of the overall system. As a result, the higher the integration level is, the better and cheaper the final product can be produced.

The convention method to design a digital circuit is by using Boolean algebra and Karnaugh Mapping. Boolean algebra is an algebraic structure defined by a set of elements together with two binary operators, '+' and '·', which was introduced by George Boole in 1854. It can be used to obtain a simpler expression for the same function and thus reduce the number of gates in the circuit. Since there are 6 theorems and 4 postulates of Boolean algebra, to choose the right theorem or postulate for expression simplification is sometime depended on the previous experience of the designer. In other words, this procedure of minimization is awkward because it lacks specific rules to predict each succeeding step in the manipulative process (Mano, 2002)(Floyd, 2006).

Karnaugh Map provides a simple straightforward procedure for minimizing Boolean functions. The map presents a visual diagram which is made up of squares of all possible ways a function may be expressed in standard form. Maps for more than four variables are not simple to use. When the number of variables becomes large, the number of squares becomes excessively large and the geometry for combining adjacent square becomes more involved (Mano, 2002)(Floyd, 2006).

In this work the selected optimization method is based on Genetic Algorithm (GA). GAs are adaptive heuristic search algorithms premised on the evolutionary idea of natural selection and genetic. The basic concept of GAs is designed to simulate processes in natural system necessary for evolution, specifically those that follow the principles first laid down by Charles Darwin of survival of the fittest.

The GAs are operated by creating many random solutions to the problem. These solutions will then be subjected to an imitation of the evolution of species. All these solutions are coded as genetic chromosomes and it will be made to mate by hybridization, also throwing in the occasional spontaneous mutation. The offspring generated will include some solutions that are better than the original.

Designing logic circuits is often done using Karnaugh Maps to take the desired output values and place them in the table corresponding to the input logic. With GAs the designer does not really need to know anything about methods to do logic design because GAs use only the set of combination input and the desired output and continue to strive toward the best solution combining the gates in thousands of random ways.

1.2 Problems Statement

Many previous researches done on the digital circuit structure by using genetic algorithm, however there is limitation of some of the GA methods as stated below:

i) The combination of GA with knowledge-based systems and used a masked crossover operator to solve the combination logic circuit. But, this method can only solve the functional output for the combination logic but not on the optimization of the gate usage (Louis, 1993).

ii) The implementation of Genetic Synthesis System (GSS) in GA uses an encoding scheme to represent combinational logic designs are not functionally equivalent to the given specification (Vemuri, 1994).

iii) The implementation of CBR in GA in the digital circuit design can guide the GA's search by the information learned from a previous search and consequently improving the current search. However, this combination method needs bigger memory space to store the previous solution (Liu and Louis, 1996).

iv) The Fuzzified Simulated Evolution (SimE) algorithm uses Multilevel Logic Based Goodness Measure which is based on the assumption that the higher the level of a gate in a multilevel logic circuit, the more minterms are covered at the output of that gate. Therefore, the goodness of a gate is affected by the number of minterms covered at its output and the level where the gate is located (Sadiq et.al, 2002).