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Optimizing Grouped Convolutions on Edge Devices

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Abstract—When deploying a deep neural network on constrained hardware, it is possible to replace the network’s standard convolutions with grouped convolutions. This allows for substantial memory savings with minimal loss of accuracy. However, current implementations of grouped convolutions in modern deep learning frameworks are far from performing optimally in terms of speed. In this paper we propose *Grouped Spatial Pack Convolutions* (GSPC), a new implementation of grouped convolutions that outperforms existing solutions. We implement GSPC in TVM, which provides state-of-the-art performance on edge devices. We analyze a set of networks utilizing different types of grouped convolutions and evaluate their performance in terms of inference time on several edge devices. We observe that our new implementation scales well with the number of groups and provides the best inference times in all settings, improving the existing implementations of grouped convolutions in TVM, PyTorch and TensorFlow Lite by 3.4×, 8× and 4× on average respectively. Code is available at <https://github.com/gecLAB/tvm-GSPC/>

I. INTRODUCTION

The deployment of deep neural networks onto mobile and embedded edge devices (e.g. IoT boards, smartphones, robots, drones, etc) has been relatively slow due to the resource constraints under which these devices operate. Big, memory-intensive neural networks typically perform poorly on edge devices. Because of this, there is a wealth of work concerned with compressing these networks. However, the predominant focus on the machine learning side of the problem, where the main performance metric considered is accuracy, has led to a proliferation of methods with promising compression results but non-trivial implications for hardware efficiency. That is, many neural architecture compression techniques may not work as expected at the system level where one of the main metrics considered is the inference time. Turner et al. [1] demonstrated that compression at the neural architecture level may have negative effects further down the *Deep Learning Inference Stack*, depending on the choices of algorithmic transformation and the target hardware device.

Many compression techniques revolve around replacing the standard convolutions in a neural network with grouped convolutions [2]–[5]. These allow for substantial savings in memory with minimal loss of accuracy, and are becoming increasingly prevalent. However, when evaluating the implementation of grouped convolutions present in current state-of-the-art deep learning frameworks such as PyTorch [6], TensorFlow Lite [7] and TVM [8], we observe that the measured inference times are far from the expected ones. Figure 1 shows an initial experiment where we run WideResNet models using standard (S) and grouped convolutions (G) on the CPU of the Hikey 970 board for the previous frameworks (note that we use $G(g)$

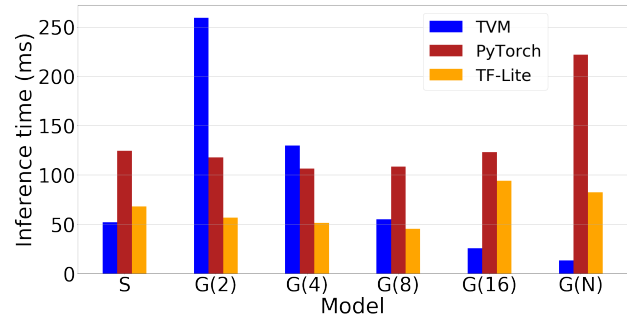


Fig. 1: Inference time for WideResNet models using standard (S) and grouped convolutions (G) on the CPU of the Hikey 970 board for three common deep learning frameworks. No framework shows the expected behavior: i) faster execution than standard when using grouped convolutions, $G(g)$ where g is the number of groups; ii) the time decreases as the number of groups increases.

to denote a grouped convolution using g groups). As we can see, none of the frameworks provides the theoretical expected behavior, that is: i) models using grouped convolutions should execute in less time than the initial model implementing standard convolutions (S), since the overall number of Multiply-Accumulate (MAC) operations decreases when using groups (see Section II); ii) as the number of groups increases (i.e. 2, 4, 8, etc), the number of MACs decreases and thus the execution time should also decrease.

Motivated by Figure 1, we propose a new implementation of grouped convolutions, that we call *Grouped Spatial Pack Convolutions* (GSPC), which: i) outperforms all the previous implementations of grouped convolutions present in current deep learning frameworks; ii) brings us closer to the theoretical optimal performance level according to the reduction in the number of MAC operations. As we will see in Section IV, although the behavior of our solution is consistent, there is still a small gap with respect to the theoretical expected times (we leave the investigation of this for future work). Note that since TVM is currently considered the state-of-the-art framework in terms of inference performance on edge devices, we integrate our GSPC implementation into the TVM source code.

The contributions of this paper are as follows:

- We propose a new algorithm for grouped convolutions, GSPC, and implement it in TVM.
- We evaluate the performance of GSPC using different network models on the CPU of several edge devices.
- We compare GSPC against implementations of grouped convolutions present in widely used deep learning frameworks, and we show that our solution outperforms them.
- We quantify the performance gap between the theoretically expected inference times and the measured ones.

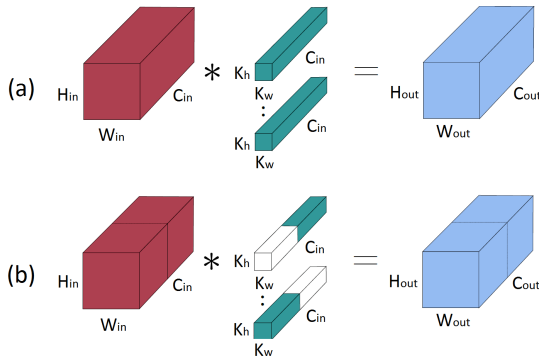


Fig. 2: Standard vs. grouped convolutions: (a) In a standard convolution S , each filter is convolved with all of the input’s channels; (b) In a grouped convolution with two groups $G(2)$, half of the filters are applied to each half of the input for a $2\times$ reduction in parameters used. More generally, a grouped convolution with g groups uses $g\times$ fewer parameters.

We briefly describe grouped convolutions in Section II. In Section III we discuss our GSPC and the details of the specific implementation in TVM. Section IV shows our experimental setup and a performance evaluation of several networks with grouped convolutions on three edge devices, discussing the time/accuracy trade off, analyzing different implementations on TVM and comparing GSPC with other existing implementations of grouped convolutions. In Section V we discuss previous related works. Finally, Section VI concludes the paper and briefly discusses potential ideas for future work.

II. COMPRESSION VIA GROUPED CONVOLUTIONS

Many works [2]–[5], [9], [10] have demonstrated the efficacy of replacing standard convolutions S with grouped convolutions for network compression. We denote these grouped convolutions as $G(g)$ where g is the number of groups. This allows for a trade off between increased model compression against reduced accuracy as we increase g .

Consider a standard convolution as depicted in Figure 2(a): its input consists of C_{in} channels. Each of C_{out} filters is convolved with **all** of these input channels to produce a single channel filter output. These outputs are concatenated to give the C_{out} channel output of our convolution. Each filter uses $C_{in} \times K_h \times K_w$ parameters, where $K_h \times K_w$ is the kernel size of our filters. As we have C_{out} filters in total then the overall parameter cost is $C_{out} \times C_{in} \times K_h \times K_w$.

Now, consider instead the case where **half** of our C_{out} filters are convolved with the first $C_{in}/2$ channels of the input, and the other half of our filters are convolved with the second $C_{in}/2$ channels of the input, as depicted in Figure 2(b). Our filters now only use half as many parameters since each is now of size $C_{in}/2 \times K_h \times K_w$. This is a grouped convolution using two groups, and the total parameter cost is two times less than a standard convolution. For g groups the parameter cost is reduced by a factor of g . A disadvantage of this grouping is that this prevents channels from mixing across groups; to counter this, practitioners typically follow grouped convolutions with a pointwise (kernel size 1) convolution [2], which incurs an additional $C_{out} \times C_{out}$ parameter cost.

III. GROUPED SPATIAL PACK CONVOLUTIONS

A. Motivation

There are a number of popular algorithms that implement standard convolutional layers in neural networks, with a myriad of trade-offs. For example, direct convolution is the simplest conceptually, requiring no data reshaping, and processes data using the “sliding window” that the convolution operation is often described as. Other approaches like GEMM convolution reshape and sometimes expand inputs or weights (which can improve performance by improving the locality of data), however this increases memory footprint and the reshape stages may have a non-negligible contribution to the inference time. For grouped convolutions, the algorithms available and their potential trade-offs have been explored less.

In TVM, the algorithm used for grouped convolutions on CPUs is grouped direct convolution. This is a variant of the standard direct convolution algorithm, and similarly has the advantage of requiring no additional memory footprint. However, without any reshaping of data or weights, it suffers from poor data locality, and thus performance can be sub-optimal, especially for large layers since parameters may need to be reloaded from higher levels of cache. For this reason, direct convolution is rarely used as the algorithmic primitive for standard convolutional layers. However their effectiveness for grouped convolutions may have different considerations.

If we observe Figure 1, we see that TVM’s grouped direct convolution scales well as the number of groups increases, and outperforms both PyTorch and TensorFlow Lite for large values of g . This scaling makes sense since the increased g reduces the number of MACs for grouped convolutional layers in the model. However, we observe that the time for $G(2)$, which reduces by 60% the number of MACs, is $4\times$ slower than the S model in TVM. Given the poor performance of $G(2)$, it is clear that an alternative approach to grouped convolutions is required to realize the potential performance improvements derived from the reduction in the number of MACs.

In this paper, we propose grouped spatial pack convolutions (GSPC), for the common NCHW data layout¹. We modify and extend the spatial pack convolutions (SPC) algorithm described in [11], which does not cover grouped convolutions. Like SPC, GSPC reshapes data, kernels, and outputs to exploit data locality for the computation. Our extension splits and computes data along an additional outer dimension for groups. Since there is no data dependency between groups, this outer dimension can be leveraged to efficiently divide data between processing cores. We implement the algorithm using TVM’s tensor compute language, as it is portable across a wide variety of platforms, and can generate code which achieves state-of-the-art performance on many common deep learning benchmarks. We favored implementing the GSPC algorithm in TVM, since the predictable scaling of its default grouped convolutions suggests that TVM’s code generator would be more likely to give us reasonable scaling.

¹Input and output data are 4D arrays in row-major order, where N is the batch size, C is the number of channels, H and W are height and width.

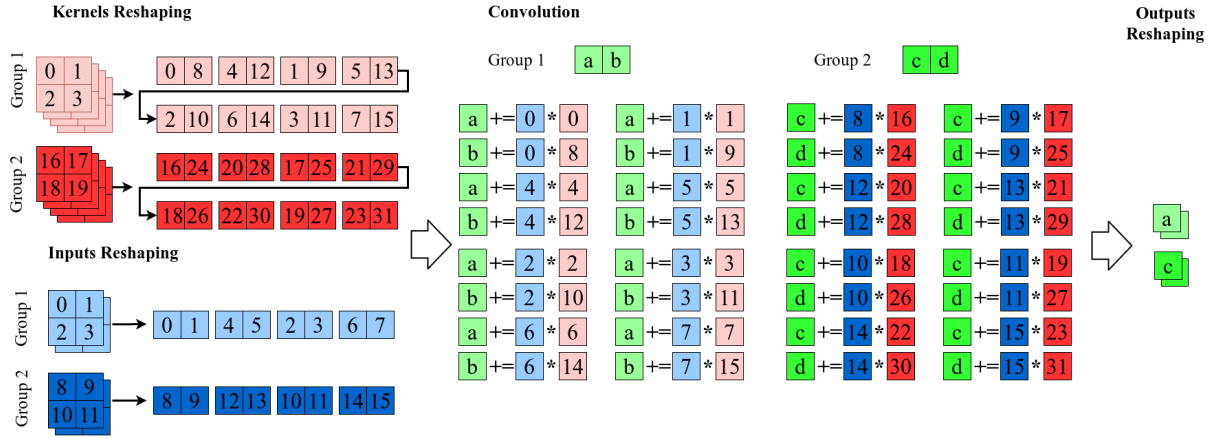


Fig. 3: Overview of GSPC using a concrete example: two groups, four filters, four input channels, strides of one, and no input padding. Note that the input size is $1 \times 4 \times 2 \times 2$, the kernels size is of dimension $4 \times 2 \times 2 \times 2$ and numbers represent indices in the NCHW format.

B. General description

At a high level, GSPC is comprised of four stages. We expect a 4D input volume of size $NC_{in}H_{in}W_{in}$, 4D kernels of size $C_{out}C_{in/g}K_hK_w$, and a 4D output volume of size $NC_{out}H_{out}W_{out}$ ². GSPC reshapes this data to improve locality. The reshape has two values which represent tile size: T_O and T_I , the former for tiling across output channels and the latter for tiling across input channels. Note that data in the same tile is related, and thus can enable further optimizations such as vectorization. We define KPG to be the number of kernels per group, and CPG as the number of input channels per group. The four stages of the GSPC algorithm are:

- Reshape 4D kernels into a new 7D volume: $C_{out}C_{in/g}K_hK_w \rightarrow g \lfloor \frac{KPG}{T_O} \rfloor \lfloor \frac{CPG}{T_I} \rfloor K_hK_wT_IT_O$.
- Reshape 4D padded input data into a new 6D volume: $NC_{in}H_{in}W_{in} \rightarrow gN \lfloor \frac{CPG}{T_I} \rfloor H_{in}T_IT_{in}$.
- Perform the grouped convolution using the 7D weights and 6D inputs, storing the output in a temporary 6D volume. The computed 6D volume is of shape $gN \lfloor \frac{KPG}{T_O} \rfloor H_{out}W_{out}T_O$.
- Reshape the 6D output volume to the desired 4D output.

The kernel reshaping stage can be computed ahead of time and stored on disk in lieu of the default layout, since it does not depend on the input data. By reordering our weights and inputs, we can improve the memory locality of our computation, which can reduce the cost of loads for elements being computed on. Similarly, accumulating the convolution on a 6D intermediate array, and reshaping to 4D output is preferable to accumulating directly onto 4D as improved locality can improve cache behavior. The tile sizes are constrained by:

$$\begin{aligned} 0 < T_O &\leq KPG \\ 0 < T_I &\leq CPG \end{aligned} \quad (1)$$

²These are standard layouts used for image data in convolutional neural networks. The $_{in}$ and $_{out}$ subscripts indicate input and output dimensions respectively. The $C_{in/g}$ dimension of the weights is one g^{th} of the input dimensions (the number of parameters decreased as g increases).

However, the ideal values for these tiles can vary. In the description of the stages of GSPC, observe that the inner dimension of the reshaped kernels and the intermediate outputs is T_O . Thus, the SIMD lane size for the target CPU can be a reasonable default for T_O , since data in the inner dimension is adjacent in memory and can thus be easily vectorized.

Figure 3 illustrates the GSPC algorithm with an example. We use tile sizes $T_O = T_I = 2$, as these are the maximum values allowed by the constraints (1). The initial data layout is shown on the left, with the channels split by group for clarity. The 6D and 7D volumes are shown flattened. We observe how the input data and kernels are reshaped to improve data locality. Even in the original data layout, data is divided between groups and the GSPC reshape stages maintain this division. The MAC operations can be ordered to reduce the number of loads for each tile. In this example, each input value is used twice, thus computing these MACs together is a load-efficient approach. The outputs reshaping stage is trivial in this case due to the small output size, and thus from a 1D memory perspective the reshape is the identity. In the case of depthwise convolution, output reshaping is also the identity, which saves $N \times C_{out} \times H_{out} \times W_{out}$ copy operations.

Algorithm 1 describes the grouped spatial pack convolutions for the NCHW layout. The stride hyperparameter is defined with S_h, S_w . Note that the number of input and output channels should be divisible by the number of groups, so we can evenly split data between the groups. The costs of the complex index arithmetic is reduced by TVM's ahead-of-time compilation for individual workloads. This means that expressions involving constants are simplified, which greatly reduces the number of computations at runtime.

The main loop of kernel reshaping (lines 2 – 4) is nested with depth 7, with each loop representing a dimension of the reshaped kernel volume. The same is true for inputs reshaping (6 – 8), with a nested loop depth of 6. The main convolution loop (10 – 18) is over the 6 dimensions of the temporary output volume, with an additional 3 loops over CPG and the kernel dimensions. For performance, these loops can be reordered.

Algorithm 1 Grouped Spatial Pack Convolutions (GSPC)

X : inputs of shape $NC_{in}H_{in}W_{in}$
 W : kernels of shape $C_{out}C_{in/g}K_hK_w$
 T_I, T_O : Tile sizes (constrained by equation 1)
 $KPG \leftarrow \frac{C_{out}}{g}, CPG \leftarrow \frac{C_{in}}{g}$

Kernels Reshaping

```
1: Allocate  $W'$  of dimension  $g \lfloor \frac{KPG}{T_O} \rfloor \lfloor \frac{CPG}{T_I} \rfloor K_h K_w T_I T_O$ 
2: for Dimensions of  $W'$  :  $j, k, c, h, w, ci, co$  do
3:    $w \leftarrow W[c \times T_O + co + j \times KPG][c \times T_I + ci][h][w]$ 
4:    $W'[j][k][c][h][w][ci][co] \leftarrow w$ 
```

Inputs Reshaping

```
5: Allocate  $X'$  of dimension  $gN \lfloor \frac{CPG}{T_I} \rfloor H_i T_I W_i$ 
6: for Dimensions of  $X'$  :  $j, n, C, h, c, w$  do
7:    $x \leftarrow X[n][C \times T_I + c + CPG \times j][h][w]$ 
8:    $X'[j][n][C][h][c][w] \leftarrow x$ 
```

Perform convolution

```
9: Allocate  $Y'$  of dimension  $gN \lfloor \frac{KPG}{T_O} \rfloor H_o W_o T_O$ 
10: for Dimensions of  $Y'$  :  $j, n, occ, oh, ow, ocv$  do
11:    $y \leftarrow 0$ 
12:   for  $c = 0$  to  $CPG$  do
13:     for  $kh = 0$  to  $K_h$  do
14:       for  $kw = 0$  to  $K_w$  do
15:          $x \leftarrow X'[j][n][\lfloor \frac{ic}{T_I} \rfloor][oh \times S_h + kh][c \bmod T_I][ow \times S_w + kw]$ 
16:          $w \leftarrow W'[j][occ][\lfloor \frac{ic}{T_I} \rfloor][kh][kw][c \bmod T_I][ocb]$ 
17:          $y += x \times w$ 
18:    $Y'[j][n][occ][oh][ow][ocb] \leftarrow y$ 
```

Outputs Reshaping

```
19: Allocate  $Y$  of dimension  $NC_{out}H_{out}W_{out}$ 
20: for Dimensions of  $Y$  :  $n, c, h, w$  do
21:    $y \leftarrow Y'[\lfloor \frac{c}{KPG} \rfloor][n][\lfloor \frac{c}{T_O} \rfloor \bmod \lfloor \frac{KPG}{T_O} \rfloor][h][w][(c \bmod T_O) \bmod KPG]$ 
22:    $Y[n][c][h][w] \leftarrow y$ 
```

C. Description of TVM compute and schedules

We implement GSPC in TVM³, as it generates efficient code for tensor programs, provides the best time for the S model, and scales well as g increases, despite the poor performance of $G(2)$. Figure 4 gives an overview of the TVM stack. Expressing new algorithms in TVM has two main stages.

The first stage is describing the algorithm in TVM’s compute language. This is conveniently accessed via a Python API. These compute descriptions are used to generate TVM intermediate representation (IR) code which can be compiled to a variety of backends such as LLVM, OpenCL, and CUDA. The algorithm implementation can be used as part of a computation graph generated from a neural network definition.

The second stage is manipulating the generated intermediate representation of the code to improve performance. This uses TVM’s schedule language, which is also accessible via a Python API. A schedule is a set of transformations applied to the IR for a given algorithm, and can be specialized for a given platform (e.g. CUDA, x86, ARM CPU, etc). This includes primitives for applying loop unrolling, loop fusion, loop fission, loop reordering, vectorization, and parallelization.

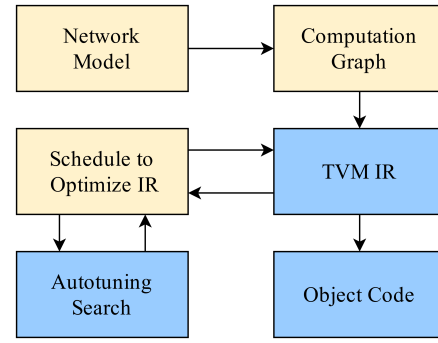


Fig. 4: Overview of the relevant parts of TVM’s stack. Light boxes are provided by us: including the benchmark models, and the definition for GSPC. Dark boxes are unaltered parts of the TVM compiler infrastructure.

A well designed schedule is key in reaching near optimal performance. In our experience, even small changes in the schedule have yielded large changes in the speed of the generated code, sometimes by an order of magnitude. However, the potential for improvement from a schedule is constrained by properties of the underlying algorithm. For example, the poor data locality of the standard direct convolution algorithm means that only modest improvements can be achieved. Whereas in some algorithms, for example GSPC, even simple transformations can yield large performance improvements. We reorder the nested loops of the convolution to make T_O the innermost loop. This can be leveraged for vectorization, hence why T_O is set to the SIMD lane size of the target CPU by default if this is permitted by the constraint.

The schedule language includes primitives to expose various aspects of the schedule as tunable parameters that can be adjusted for different data shapes on a given platform to improve performance. For example, exploring loop reordering may reduce inference time for some layer configurations but not others, or unrolling an inner loop may or may not give a performance boost depending on the number of iterations. A strength of TVM is the autoTVM project [12], which allows exploration of this tuning space (autotuning) to improve inference time performance for target architectures. For large models, the autotuning process is very time consuming, as the search space can be very large (e.g. individual models can take hours to tune, especially on constrained edge devices). Some autotuning algorithms can also get stuck in suboptimal manifolds of the search space and require restarting. More efficient autotuning, including the use of transfer learning to reuse knowledge about successful configurations for similar platforms or data shapes, is an area of active research.

Tuning parameters exposed by our GSPC schedule include varying the tile sizes, and optionally unrolling the K_w loop of the convolution stage. There may be scope for additional improvements to the GSPC schedule, which could further reduce inference time. For example, a potential optimization could investigate the impact of interleaving portions of the reshaping and computation stages to reduce the footprint of the intermediate arrays by reusing a subset of their memory.

³The source code is available at <https://github.com/gecLAB/tvm-GSPC/>

TABLE I: Hardware features of the devices used in the experiments.

Device	CPU	L1 Cache (I+D)	L2 (+L3) Cache	RAM	Instruction Set
Desktop	Intel i7-8700 (6 cores) @ 3.2 GHz	192K + 192K	1.5M (+12M)	16GB DDR3	x86 64-bit
HiKey 970	Arm Cortex-A73 (4 cores) @ 2.4 GHz Arm Cortex-A53 (4 cores) @ 1.8 GHz	256K + 256K 128K + 128K	2M shared 1M shared	6GB LPDDR4	ARMv8-A 64-bit
Raspberry Pi3B	Arm Cortex-A53 (4 cores) @ 1.2 GHz	64K + 64K	512K shared	1GB LPDDR2	ARMv8-A 64-bit

IV. EVALUATION

A. Experimental setup

1) *Datasets and Networks*: We consider two datasets widely adopted for image classification tasks, CIFAR-10 [13] and ImageNet [14], and we use the `float32` type to represent data values. We evaluate three deep neural network models, WideResNet-40-2 and ResNet-34 which are good representatives of residual network types, and MobileNetV2 which is a widely used model for edge devices. Some details of these models are the following:

- WRN-40-2: we use a Wide Residual Network (WRN) [15] with 40 layers and width-multiplier 2 that requires 2.2 million parameters. We use the network as defined for CIFAR-10 classification.
- ResNet-34: we use a Residual Network with 34 layers [16] that requires 21.8 million parameters. We use the ImageNet definition of the network.
- MobileNetV2: we use a Mobile Network [3] with 53 layers that requires 3.5 million parameters. We use its original ImageNet definition.

We train networks for the previous three models where the standard convolutions are replaced with a grouped convolution followed by a pointwise standard convolution (as discussed in Section II). We consider the following grouped convolutions: $G(g) \forall g \in \{2, 4, 8, 16, N\}$, where N is the number of input channels to each convolution. Note that the default architecture of MobileNetV2 uses $g = N$, so the original architecture is actually the MobileNetV2 $G(N)$ model. Also note that although pointwise convolutions incur a parameter cost, their inference time is negligible relative to grouped convolutions. This is because the operation is equivalent to a matrix multiplication over inputs and parameters, with a low number of MACs, and no data reshaping is required.

For WRN-40-2 and ResNet-34, networks were trained with attention transfer [17] on 1 and 4 NVIDIA TITAN X GPUs for 200 and 100 epochs respectively using Stochastic Gradient Descent (SGD) with momentum 0.9 to minimize cross-entropy loss, learning rate of 0.1 and weight decay 0.0005 (WRN-40-2) and 0.0001 (ResNet-34). For MobileNetV2, we trained networks with varying values of g on 1 NVIDIA TITAN RTX GPU for 150 epochs using SGD with momentum 0.9, learning rate of 0.05 and weight decay 0.0004.

2) *Hardware platforms*: The platforms used in this work are listed in Table I. There are two edge boards (Hikey 970, Raspberry Pi3B) that include both CPU and GPU, however in this work we focus on CPU evaluation, and we leave GPU investigation for future work. We also analyze a standard

TABLE II: Inference time in *ms* for WRN-40-2 models with standard (*S*) and grouped (*G*) convolutions when running on the platforms in Table I.

Model	Params	MACs	Top1	Desktop	HiKey	RPi3
S	2242.26K	328.30M	4.79	8.23	65	811
$G(2)$	1357.68K	198.15M	4.87	9.20	51	530
$G(4)$	813.36K	118.52M	5.00	5.84	34	307
$G(8)$	541.20K	78.71M	5.05	4.65	24	199
$G(16)$	405.12K	58.80M	5.13	4.51	20	158
$G(N)$	292.22K	44.83M	6.57	2.14	16	122

TABLE III: Inference time in *ms* for ResNet-34 models with standard (*S*) and grouped (*G*) convolutions when running on the platforms in Table I.

Model	Params	MACs	Top1	Desktop	HiKey	RPi3
S	21.79M	3.67G	26.73	107	1096	7466
$G(2)$	13.22M	2.25G	26.13	99	636	5700
$G(4)$	8.14M	1.39G	26.58	62	426	3334
$G(8)$	5.60M	0.97G	27.24	41	304	2344
$G(16)$	4.34M	0.75G	27.99	34	259	1749
$G(N)$	3.13M	0.56G	30.16	23	204	1285

TABLE IV: Inference time in *ms* for MobileNetV2 models with standard (*S*) and grouped (*G*) convolutions when running on the platforms in Table I.

Model	Params	MACs	Top1	Desktop	HiKey	RPi3
S	44.05M	5.56G	26.03	166	1207	13770
$G(2)$	23.75M	2.92G	25.90	135	776	7603
$G(4)$	13.59M	1.60G	26.34	75	733	4608
$G(8)$	8.52M	0.95G	26.84	47	495	2625
$G(16)$	5.98M	0.62G	27.06	37	429	1808
$G(N)$	3.50M	0.31G	28.20	15	134	812

desktop CPU. Therefore, we evaluate Arm and Intel processors that implement two different instruction set architectures with frequencies ranging from 1.2GHz to 3.2GHz. Note that the CPU of the Hikey board implements the *big.LITTLE* [18] architecture (4 *big* cores + 4 *LITTLE* cores), but in this work we only use the *big* cores. Finally, the memory hierarchy varies significantly across platforms. All these features give us a diverse set of configurations for evaluation.

B. Speed vs Accuracy analysis

Tables II, III and IV show the inference time in milliseconds for all the network models considered using standard (*S*) and grouped (*G*) convolutions for WRN-40-2, ResNet-34 and MobileNetV2 respectively when running on the three platforms under study⁴ using our GSPC implementation in TVM. The tables also show the total parameter cost, the number of MACs,

⁴Note that all times are for 1 thread execution, since we verified that threads affect quite differently the performance of each platform, thus not providing a completely fair comparison. We leave the threads analysis for future work.

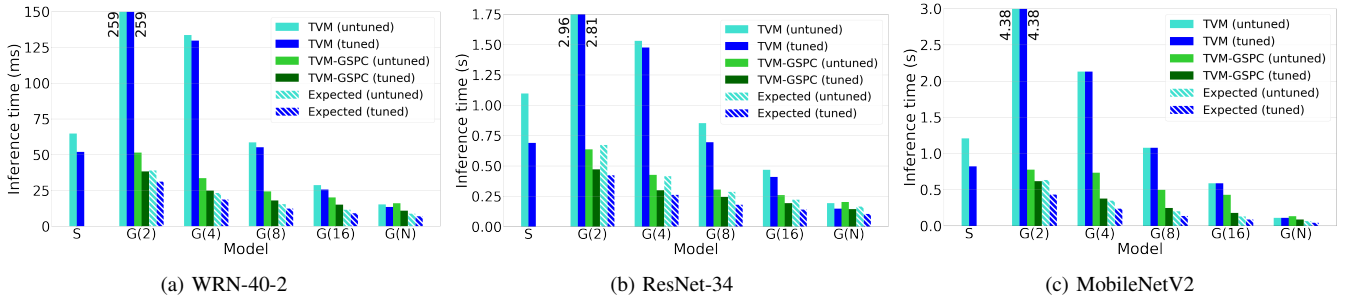


Fig. 5: Inference time in *ms* for network models with standard (*S*) and grouped (*G*) convolutions when running on the CPU of the Hikey 970 board. We compare the measured and expected times of our GSPC and the default TVM implementation for both tuned and untuned versions of the code.

and the Top1 error of each network model. The number of MACs is obtained with the following formula:

$$MAC_s = \frac{N \times C_{in} \times C_{out} \times K_h \times K_w \times H_{out} \times W_{out}}{g} \quad (2)$$

where N is the batch size ($N = 1$ for all experiments), C_{in} is the number of input channels, C_{out} is the number of output channels, H_{out} and W_{out} are the height and width of the layer’s output respectively, $K_h \times K_w$ is the kernel size of each convolution, and g is the number of groups.

As we can see in the tables, the reduction in the number of parameters, and thus the number of MACs, derived from using grouped convolutions provides between ~ 4 - $17\times$ of speedup in the inference time across platforms and networks, the Raspberry Pi device and the MobileNetV2 network being the combination that provides the highest improvements. We also observe that on the desktop the inference time for $G(2)$ is not reduced with respect to the corresponding S model as on the other two platforms, it even increases for WRN-40-2. However, the time decreases for every subsequent G model. This observation suggest that the schedule is not properly optimized for the Intel x86-64 architecture of the desktop. In TVM, the schedules can be optimized for a given hardware architecture and the default S model is taking advantage of this, as we checked that it has schedules for both Intel and Arm architectures. However, we optimized the schedule of our GSPC code primarily for the Hikey platform, as we performed most of our experiments on it. Optimizing GSPC for the Intel architecture should provide better times for the G models, but we leave this optimization for future work.

Related to the accuracy of the models, we see in Tables II, III and IV that the increase in Top1 error can vary from almost 2% for WRN-40-2 to 3.5% for ResNet-34 when we compare the S and G models. We also see that the overall error is much higher for the models using the ImageNet dataset ($\sim 30\%$ vs $\sim 7\%$), since a 1000-way classification is harder than a 10-way one. Therefore, these results provide different options to the user for selecting a model based on the time/accuracy trade off. The best solution for a given application will depend on its specific requirements and the hardware platforms available. For example, if the target platform is very constrained like the Raspberry Pi, it could be better to sacrifice some accuracy in

favor of speeding up the inference time. However, for a more powerful platform like the desktop it can be better to maximize accuracy, as the all times are below 166ms.

C. TVM analysis

Figure 5 shows the *Measured* versus the *Expected*⁵ inference time for all the models considered for the three networks under study when running on the Hikey 970 platform. We compare GSPC with the default implementation of grouped convolutions in TVM, and we consider the tuned (i.e. we use the autoTVM [12] tool mentioned in Section III-C) and untuned versions of the code in both cases. Note that the times in Tables II, III and IV correspond to GSPC untuned times. The reason is that the tuning process is very time consuming and error prone, especially in constrained devices. Based on our tuning experience on the Hikey board, we estimate that getting the required tuned times on the Raspberry Pi board using the same number of tuning iterations would take weeks. Our key observations in Figure 5 are as follows:

- GSPC improves the times of the default TVM implementation of the $G(2)$ - $G(16)$ models for the three networks for both tuned and untuned versions of the code. However, for $G(N)$ the default TVM implementation is slightly better than GSPC (~ 5 - 22% across networks) for the untuned version. Initially, we thought that the most likely reason for that could be the overhead created by the reshaping stages of GSPC, which for $G(N)$ are maximized relative to the computation time. However, we optimized these reshaping stages for our $G(N)$ models and we obtained the current differences. We leave for future work to investigate this problem further.
- When we consider the tuned versions of $G(N)$, GSPC provides better times than the default TVM implementation (~ 3 - 34% across networks). However, note that for MobileNetV2 the tuned times that we obtained for the default TVM implementation were worse than the untuned ones for all G models. For this reason, in Figure 5c the tuned times are the same as the untuned ones. We could not find an explanation for this strange result, but we double-checked it running the tuner several times.

⁵Computed from the inference time of the S model on a given platform by obtaining the time of a single MAC operation and then extrapolating.

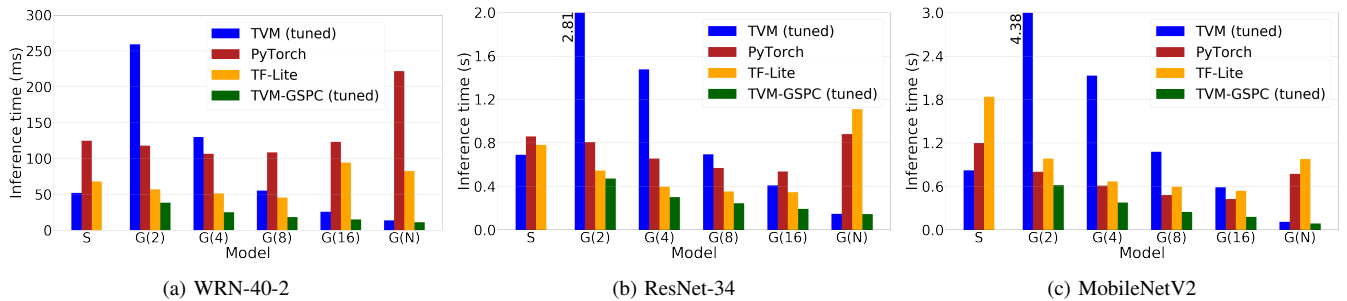


Fig. 6: Inference time in *ms* for network models with standard (*S*) and grouped (*G*) convolutions when running on the CPU of the Hikey 970 board. We compare the tuned version of GSPC and default TVM against PyTorch and TensorFlow Lite.

- There are differences between the expected and measured times for both tuned and untuned versions across all *G* models and networks. This performance gap is ~ 7 -99% for untuned and ~ 27 -72% for tuned versions respectively. Note that the expected times are theoretical estimations based on the structure of the code for the standard convolution, which should not be considered as true optimal values. In some cases, it can be possible to outperform the expected time (see *G*(2) in Figure 5b), for reasons such as more data fitting in a lower level of cache.

Overall, our GSPC implementation is on average $3.4\times$ faster than the default TVM code for all the tuned/untuned *G* models.

D. Frameworks comparison

Figure 6 shows the inference time of GSPC and other implementations of grouped convolutions in current deep learning frameworks for all the *G* models of the three networks under study when running on the CPU of the Hikey board. The figure also shows the times for the *S* models. We consider the tuned version of both GSPC and default TVM. The other frameworks analyzed are PyTorch [6] and TensorFlow Lite [7].

As we can see, GSPC provides the best results for all the *G* models of the three networks, clearly outperforming the default TVM and the other two frameworks, up to $8\times$ and $4\times$ better than PyTorch and TensorFlow Lite respectively. To the best of our knowledge, GSPC is the most efficient implementation, in terms of inference time, of grouped convolutions available. We also observe that TensorFlow Lite performs much better than PyTorch for all the *G* models of WRN-40-2 and for the *G*(2)-*G*(16) models of ResNet-34, whereas PyTorch is better for *G*(*N*) of ResNet-34 and all the *G* models of MobileNetV2. However, none of these frameworks scales as expected for the *G* models according to the number of MAC operations.

V. RELATED WORK

It is well-established that many modern neural networks are over-parameterized for inference [19]. A focus on achieving state-of-the-art results has led to bloated network architectures with diminishing returns when new parameters are added [20]. Given that most of the energy consumption and execution time in such networks is dedicated to convolution [21], it is desirable to reduce convolutional over-parameterization for use in resource-constrained settings. One popular method to

exploit parameter redundancy is to split standard convolutions into *groups* along the channel dimension. These *grouped convolutions* first appeared in AlexNet [22] due to GPU memory constraints, and have since featured prominently in the network compression literature [2]–[5], [9].

As the number of groups is increased, the parameter cost of a grouped convolution decreases at the expense of representational capacity. In the extreme case where there are as many groups as there are convolutional channels we obtain *depthwise convolutions*. In MobileNets [2] for example, the authors replace standard convolutions with pairs of depthwise convolutions and pointwise (1×1) convolutions, the latter of which allows for channel mixing to restore capacity. The technique is known as depthwise separable convolutions [23]. Similarly, in [4] the authors take the standard block used in ResNets [16] consisting of two standard convolutions, and replace each convolution with a grouped and pointwise pair. The number of groups can be varied to trade off accuracy against parameter total.

However, leveraging parameter reductions into better hardware performance remains difficult. Many frameworks transform convolution into matrix-matrix multiplication in order to exploit pre-existing, highly optimized subroutines [24], which may not be composable with any dimensionality perturbations caused by cheapening. Only recently has attention turned to direct convolution itself [25], and though code generation frameworks promise performance portability for custom convolutions [8], [26]–[28], they have been shown to lack the generality required to adopt such radical neural architecture changes to a vast hardware landscape [29].

Common approaches to convolution include direct convolution, Winograd convolution [30], and GEMM convolution. Winograd convolution involves mapping data into Fourier space to allow multiplications to become additions. GEMM convolution is especially popular on GPUs, where the input data is expanded and reshaped using a method known as *im2col*, so that convolution can be computed as a well optimized matrix multiplication with libraries such as OpenBLAS [31] and ATLAS [32]. TVM’s default approach to standard convolution on the CPU is an algorithm known as spatial packed convolution (SPC), described in [11]. Tradeoffs in performance can vary across platforms and architecture.

VI. CONCLUSION

In this paper we have proposed Grouped Spatial Pack Convolutions (GSPC) as a new and more efficient implementation of grouped convolutions. We have implemented GSPC in TVM, which provides state-of-the-art performance on edge devices. We have evaluated several network models implementing grouped convolutions for two datasets on three edge devices with different hardware architectures. We have also compared our implementation against existing solutions in current deep learning frameworks, outperforming them in all settings. Finally, we observed that even though models based on grouped convolutions significantly improve the performance of the initial standard model, the expected inference time, based on the number of MAC operations, does not translate into measured performance. We leave to further study this performance gap for future work. We also leave for future work to analyze the performance of GSPC on the *big.LITTLE* [18] architecture and embedded GPUs (e.g. Arm Mali) present in current edge devices. Additionally, translation of other approaches to standard convolution into the group convolution domain, e.g. Winograd, and investigation of their performance trade-offs across different benchmarks and devices. Finally, considering power [33] is also an area for future research.

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REFERENCES

- [1] J. Turner, J. Cano, V. Radu, E. J. Crowley, M. OBoyle, and A. Storkey, "Characterising cross-stack optimisations for deep convolutional neural networks," in *2018 IEEE International Symposium on Workload Characterization (IISWC)*, September 2018, pp. 101–110.
- [2] A. G. Howard, M. Zhu, B. Chen, D. Kalenichenko, W. Wang, T. Weyand, M. Andreetto, and H. Adam, "MobileNets: Efficient convolutional neural networks for mobile vision applications," *arXiv:1704.04861*, 2017.
- [3] M. Sandler, A. Howard, M. Zhu, A. Zhmoginov, and L.-C. Chen, "Mobilenetv2: Inverted residuals and linear bottlenecks," in *Proc. of the IEEE Conference on Computer Vision and Pattern Recognition*, 2018.
- [4] E. J. Crowley, G. Gray, and A. Storkey, "Moonshine: Distilling with cheap convolutions," in *Advances in Neural Information Processing Systems*, 2018.
- [5] G. Huang, S. Liu, L. Van der Maaten, and K. Q. Weinberger, "DenseNet: An efficient densenet using learned group convolutions," in *IEEE Conference on Computer Vision and Pattern Recognition*, 2018.
- [6] A. Paszke et al., "Pytorch: An imperative style, high-performance deep learning library," in *Advances in Neural Information Processing Systems*, 2019, pp. 8024–8035.
- [7] "TensorFlow Lite," <https://www.tensorflow.org/lite/>.
- [8] T. Chen, T. Moreau, Z. Jiang, L. Zheng, E. Yan, H. Shen, M. Cowan, L. Wang, Y. Hu, L. Ceze, C. Guestrin, and A. Krishnamurthy, "TVM: An automated end-to-end optimizing compiler for deep learning," in *13th USENIX Symposium on Operating Systems Design and Implementation (OSDI 18)*, Oct. 2018, pp. 578–594.
- [9] Y. Ioannou, D. Robertson, R. Cipolla, and A. Criminisi, "Deep roots: Improving CNN efficiency with hierarchical filter groups," in *IEEE Conference on Computer Vision and Pattern Recognition*, 2017.

- [10] J. Turner, E. J. Crowley, M. O'Boyle, A. Storkey, and G. Gray, "Blockswap: Fisher-guided block substitution for network compression on a budget," in *International Conference on Learning Representations*, 2020.
- [11] L. Zheng and T. Chen, "Optimizing Deep Learning Workloads on ARM GPU with TVM," in *Proceedings of the 1st on Reproducible Quality-Efficient Systems Tournament on Co-Designing Pareto-Efficient Deep Learning (ReQuEST)*, 2018.
- [12] T. Chen, L. Zheng, E. Yan, Z. Jiang, T. Moreau, L. Ceze, C. Guestrin, and A. Krishnamurthy, "Learning to Optimize Tensor Programs," in *Advances in Neural Information Processing Systems*, 2018.
- [13] A. Krizhevsky, "Learning multiple layers of features from tiny images," Master's thesis, University of Toronto, 2009.
- [14] O. Russakovsky, J. Deng, H. Su, J. Krause, S. Satheesh, S. Ma, Z. Huang, A. Karpathy, A. Khosla, M. Bernstein, A. C. Berg, and L. Fei-Fei, "ImageNet Large Scale Visual Recognition Challenge," *International Journal of Computer Vision (IJCV)*, 2015.
- [15] S. Zagoruyko and N. Komodakis, "Wide residual networks," in *British Machine Vision Conference*, 2016.
- [16] K. He, X. Zhang, S. Ren, and J. Sun, "Deep residual learning for image recognition," in *Proceedings of the IEEE Conference on Computer Vision and Pattern Recognition*, 2016.
- [17] S. Zagoruyko and N. Komodakis, "Paying more attention to attention: Improving the performance of convolutional neural networks via attention transfer," in *Int. Conference on Learning Representations*, 2017.
- [18] B. Jeff, "Big.little system architecture from ARM: saving power through heterogeneous multiprocessing and task context migration," in *Design Automation Conference (DAC)*, June 2012, pp. 1143–1146.
- [19] S. Han, J. Pool, J. Tran, and W. J. Dally, "Learning both weights and connections for efficient neural networks," in *Advances in Neural Information Processing Systems*, 2015.
- [20] Y. Huang, Y. Cheng, A. Bapna, O. Firat, D. Chen, M. Chen, H. Lee, J. Ngiam, Q. V. Le, Y. Wu, and z. Chen, "Gpipe: Efficient training of giant neural networks using pipeline parallelism," in *Advances in Neural Information Processing Systems*, 2019, pp. 103–112.
- [21] L. Lai, N. Suda, and V. Chandra, "Not all ops are created equal!" *arXiv:1801.04326*, 2018.
- [22] A. Krizhevsky, I. Sutskever, and G. Hinton, "ImageNet classification with deep convolutional neural networks," in *Advances in Neural Information Processing Systems*, 2012.
- [23] L. Sifre, "Rigid-motion scattering for image classification," Ph.D. dissertation, Ecole Polytechnique, CMAP, 2014.
- [24] S. Chetlur, C. Woolley, P. Vandermersch, J. Cohen, J. Tran, B. Catanzaro, and E. Shelhamer, "cudnn: Efficient primitives for deep learning," *arXiv:1410.0759*, 2014.
- [25] E. Georganas, S. Avancha, K. Banerjee, D. Kalamkar, G. Henry, H. Pabst, and A. Heinecke, "Anatomy of high-performance deep learning convolutions on simd architectures," in *Int. Conf. for High Performance Computing, Networking, Storage and Analysis*, 2018.
- [26] N. Vasilache, O. Zinenko, T. Theodoridis, P. Goyal, Z. DeVito, W. S. Moses, S. Verdoolaage, A. Adams, and A. Cohen, "Tensor comprehensions: Framework-agnostic high-performance machine learning abstractions," *arXiv:1802.04730*, 2018.
- [27] A. Venkat, T. Rusira, R. Barik, M. Hall, and L. Truong, "Swirl: High-performance many-core cpu code generation for deep neural networks," *Int. Journal of High Performance Computing Applications*, 2019.
- [28] R. Baghdadi, J. Ray, M. B. Romdhane, E. Del Sozzo, A. Akkas, Y. Zhang, P. Suriana, S. Kamil, and S. Amarasinghe, "Tiramisu: A polyhedral compiler for expressing fast and portable code," in *Proceedings of the 2019 IEEE/ACM International Symposium on Code Generation and Optimization*, 2019, p. 193205.
- [29] P. Barham and M. Isard, "Machine learning systems are stuck in a rut," in *Proceedings of the Workshop on Hot Topics in Operating Systems (HotOS)*, 2019, pp. 177–183.
- [30] A. Lavin and S. Gray, "Fast Algorithms for Convolutional Neural Networks," in *2016 IEEE Conference on Computer Vision and Pattern Recognition (CVPR)*, Jun. 2016, pp. 4013–4021.
- [31] "OpenBLAS: An optimized BLAS library," <http://www.openblas.net/>.
- [32] R. C. Whaley and J. Dongarra, "Automatically Tuned Linear Algebra Software," in *Ninth SIAM Conference on Parallel Processing for Scientific Computing*, 1999.
- [33] Y. Chen, T.-J. Yang, J. Emer, and V. Sze, "Understanding the limitations of existing energy-efficient design approaches for deep neural networks," in *The Conference on Systems and Machine Learning (SysML)*, 2018.