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Design Optimisation of a Current-Fed Solid-State Transformer for MV Grid-Connected Applications †

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Abstract: For integrating large batteries in the medium voltage grid, current fed solid-state transformers offer galvanic isolation and a significant weight and size reduction. While the power losses increase with frequency and flux density, the core volume is contrariwise. Therefore, a design optimisation to achieve minimum losses and/or a minimum volume is essential. An optimisation strategy is proposed in this paper to find the optimum operating frequency and core flux density under certain practical constraints such as winding voltage per turn, clearance between transformer windings, saturation flux density and minimum efficiency. Differently from previous works, the proposed strategy provides a holistic approach for the design considering all main power losses from all main components using nonsinusoidal voltage waveforms and different operating conditions. Analytical equations for the power losses calculation and the cores design are derived and validated using ANSYS and MATLAB Simulink software packages. Simulation results of the power loss calculation under different operating frequencies and duty cycles are presented and compared with the analytical results. A case study for designing a 1.0 MW, 0.6/18 kV current fed solid-state transformer is presented. The results of two optimisation objectives, minimum power losses or minimum total cores housing volume are also shown.

Keywords: optimisation; solid state transformer; power losses; grid connected

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1. Introduction

The Energy Storage System (ESS) is becoming a crucial element in smart grids. ESS can smooth Renewable Energy Source output power, and provide grid support such as frequency balancing and voltage control. Traditionally, BESS is connected to the medium voltage (MV) grid (1–35 kV) via a bidirectional DC/DC converter, DC/AC converter and line frequency step-up transformer. Due to the limited voltage and current capabilities of the power electronic devices (up to 6.5 kV/25 A [1]), different power electronics topologies have been proposed. In general, these topologies can be divided into two main categories: transformer and transformerless [2]. In the transformer topology, a two- or three-level converter is connected to a step-up line frequency transformer [3,4]. The main disadvantages of this topology are the large size/weight of the line transformer and relatively lower overall system efficiency compared to other transformerless topologies [2]. In the transformerless topologies, there are two main subcategories: a series connection of semiconductors; and series connection of converter modules. In the series connection of semiconductors, the power electronics switches are connected in series. This requires a special design of the gate driver to ensure synchronous switching. In series-connected converter modules topologies, cascaded modules such as half-bridge or full-bridge are connected in series to increase voltage capability, or in parallel to increase current capability. There are diverse configurations

such as Cascaded H-bridge [5] and Modular Multilevel Converter [6]. In these topologies, there is no gaelvanic isolation between the battery and the grid. Furthermore, they require a large number of battery cells to achieve a high dc voltage.

To realise the advantages of galvanic isolation, weight reduction and low battery voltage, SST can be employed [7]. An SST offers some advantages over the traditional line frequency transformer such as power flow control, voltage sag compensation, fault current limitation, reduced size and weight and improved power quality [1]. SST has mainly emerged from DAB technology. There are two main topologies for DAB, VF-DAB and CF-DAB [8]. In general, the term current-fed refers to an isolated converter where the filter inductor is on the primary side and the output filter consists of a single component capacitor [9,10]. Current-fed converters are boost-derived topologies. The term of current-fed converter first appeared in the early seventies, mainly on push-pull and flyback converters [11,12]. The voltage phase shift technique is employed to control power flow in VF-DAB. There are different control techniques to achieve the phase shift such as single-phase shift, dual-phase shift and triple-phase shift [13,14]. The dual-phase shift seems to be the most suitable control technique, according to [15]. VF-DAB suffers from several limitations of high input pulsating current, high circulating current through power electronic devices and magnetic components [4]. CF-SST topology, however, has been demonstrated to be meritorious over VF-SST, due to its lower input current ripple, lower transformer turns ratio and easier current control [16]. Moreover, not all H-bridges on both sides of the transformer are active as in the case of VF-SST. Only one H-bridge is acting as a boost/buck converter, and the other H-bridge is acting as a rectifier or passive rectifier (to reduce the current spike). Therefore, CF-DAB (also be referred to as Current Fed Solid State Transformer, CF-SST) is considered in this paper for grid-connected battery applications. In CF-SST, a choke coil is employed as intermediate energy storage [17]. The turn-off voltage spike is the main problem in CF-SST, due to the transformer leakage inductance. RCD snubber circuits, active clamp, zero current switching and secondary modulation can be employed to overcome this problem [16,18–20]. Despite the merits of CF-SST, flux saturation, core losses, thermal design and high voltages across power electronics switches are the main design challenges.

Therefore, achieving the optimum design goals is vital to obtain the benefits of CF-SST. A key parameter in the transformer design is the flux density. The optimum flux density value for the lowest power losses is normally found at the point where the copper losses and the iron losses are equal [21]. However, this method considers only sinusoidal waveforms, and hence ignores other harmonics.

The design optimisation of SST has been discussed extensively in the literature. Main objective functions are typically minimum losses [22–25] and or maximum power density (minimum volume) [26–29]. Other objectives include minimum dc-link capacitance [30] and minimum heatsink volume [31]. Typical optimisation parameters are flux density, current density, switching frequency, number of converter cells [22,25,26,28–31] and types of semiconductor devices [23,27]. In [22], the flux density is used as the main optimisation parameter, and the switching frequency is kept constant. In [25–31], however, switching frequency is used as the main optimisation parameter while the flux density is kept constant. Different methods are used for core power losses, including the General Steinmetz Equation, where sinusoidal waveforms are assumed [32], and the improved General Steinmetz Equation (iGSE) [33,34]. The Stiementz equation fails to give accurate results in the SST applications, as it mainly depends only on magnetic materials data provided by manufacturers, which are based on sinusoidal excitation. Moreover, the nonlinear nature of ferromagnetic materials means that adding the individual frequency components of a Fourier series is not possible to calculate the core losses. On the other hand, iGSE employing instantaneous flux density to calculate the core losses has proven to give good results for nonsinusoidal waveforms [35]. It is important to consider the effect of varying the switching frequency not only on the transformer losses but also on the power electronics, i.e., to consider the total losses of the system rather than the transformer losses on its

own. Power electronic losses can be determined analytically [25,27,31], numerically [23] or experimentally [26]. While the experimental method is the most accurate, it cannot be used during the design optimisation stage, and is only useful for design validation. Numerical methods are more accurate than analytical ones, but their long execution time makes them less attractive if they are to be used by an optimiser that will need to call the loss calculation process a high number of times. However, none of the above papers uses a holistic design approach, considering power losses from all main components assuming nonsinusoidal excitation waveforms, while concurrently using both switching frequency and flux density as the optimisation parameters. Furthermore, all previously reported papers considered VF-SST topology for design optimization, and none have considered CF-SST where the choke coil becomes an integral part of the overall system.

This paper presents a design optimisation procedure for a DC/DC CF-SST for a battery to MV grid applications. All the main losses in the conversion stage are considered, which include power electronics and core and copper losses in the transformer and the choke coil. Non-sinusoidal voltage waveforms in the transformer are used for loss calculations. Stray loss is not considered in this paper due to the complexity of calculation, which depends on the transformer tank and steel construction. Typically, the stray loss is around 10–15% of the total transformer losses and requires 3-D Finite Element Analysis (FEA) for accurate calculation [36]. Analytical equations for the power losses calculation are derived and validated using the ANSYS and MATLAB Simulink software packages. The optimisation objectives can be chosen by the user as maximum efficiency or minimum volume, and the design parameters are flux density and operating frequency. The total volume includes the cores of the transformer and choke coil, in addition to that of the heat sink. The constraints are maximum winding voltage per turn, the width of the winding allowing for clearances, saturation flux density and minimum efficiency (in the case of minimum volume objective). The proposed method will determine the core dimensions of the transformer and choke coil, as well as the operating frequency and flux density. Therefore, the proposed method will serve as a useful tool for designing a DC/DC CF-SST, while ensuring that the core dimensions and operating frequency are optimised to achieve the required aim of either minimum losses or volume.

The main merits of the proposed method can be summarised as follows: firstly, it optimises the switching frequency and flux density at the same time, taking into account a holistic approach for calculating the system's overall losses; and secondly, it provides the core dimensions of the transformer and coil choke.

2. CF-SST System Configuration

A CF-SST system consisting of a medium frequency transformer, choke coil and H-bridge converters connected in parallel at the low voltage side and series at the high voltage side is shown in Figure 1. The low voltage side is connected to the dc supply, and the high voltage side will be connected to a DC/AC Modular Multilevel Converter (MMC) (not shown in the figure) to interface the system to the MV grid. Figure 2 shows a circuit diagram for a simple CF-SST proposed in [16]. To transform the power from the dc supply to the grid, the choke coil and H-bridge 1 operate as a boost converter while in charging mode, H-bridge 2 operates as a buck converter regulating power and H-bridge 1 operates as a controlled rectifier. The inductance of the choke coil is assumed high enough to maintain a constant current through it. The switching events, currents and voltage waveforms are shown in Figure 3 [16,37] which will be used in the power loss calculations in the next sections.

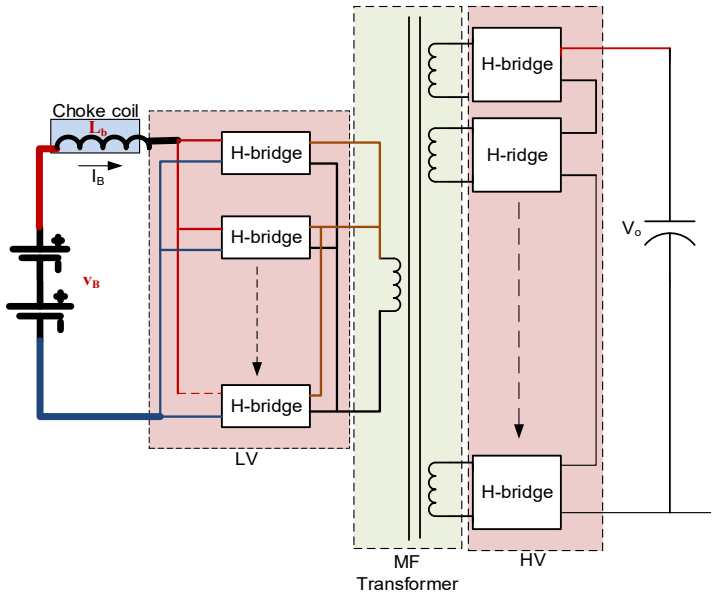

Figure 1. CF-SST configuration.

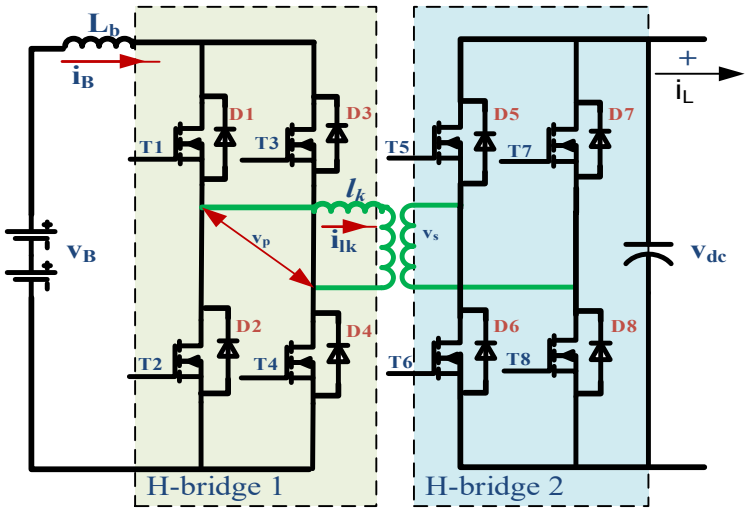

Figure 2. Simplified CF-SST circuit.

D1 and D2 are the duty ratios to generate the gate signals for H-bridge 1 and of H-bridge 2, respectively. The reader is referred to [16] for more information on the converter operation.

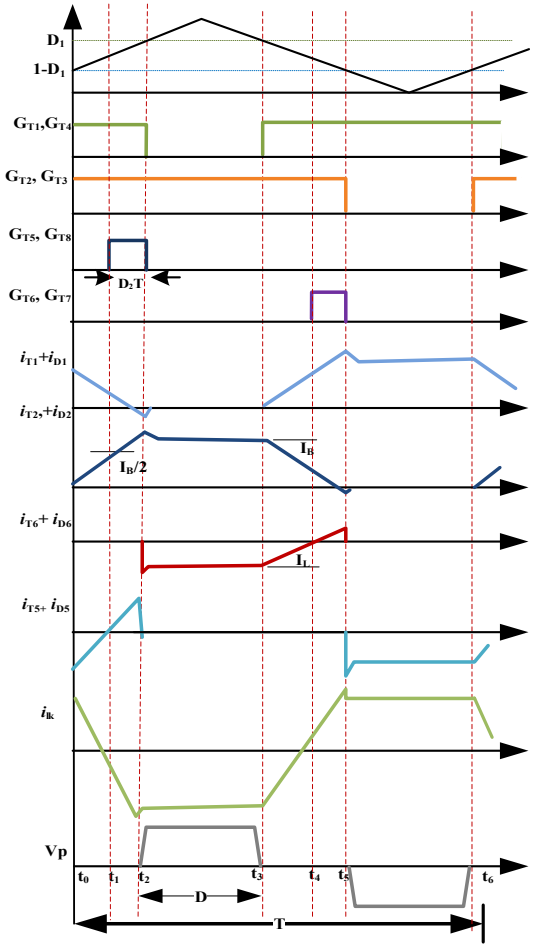

Figure 3. Details of CF-SST operation over one cycle [16].

3. CF-SST Power Losses Calculations

The CF-SST total losses include those of the transformer (core and copper), choke coil (core and copper) and power electronics (switching and conduction). More details about these losses and how they can be calculated are presented in the following subsections.

3.1. Transformer Core and Copper Losses

Core losses are normally calculated using empirical equations based on measured data, such as the Original Steinmetz Equation, which is applicable for sinusoidal excitation [32]. When the transformer is excited by non-sinusoidal waveforms, iGSE is used for square wave excitation, and it was shown that it gives accurate results compared to those obtained experimentally [38]. Iron losses by iGSE for square voltages can be shown to be given by [38]:

$$P_v = \frac{1}{T} k_i (\Delta B)^{\beta-\alpha} |2\Delta B|^{\alpha} (DT)^{1-\alpha}, \tag{1}$$

$$k_i = \frac{K}{(2)^{\beta-1}(\pi)^{\alpha-1}\left(1.1044 + \frac{6.8244}{\alpha+1.354}\right)} \tag{2}$$

ΔB can be calculated as [36,39]:

$$\Delta B = 2B_m = \frac{V_{max} DT}{2NA_i}, \tag{3}$$

The core losses in (1) are calculated per unit volume. To find the total core losses, the transformer core volume needs to be determined. This core volume is designed based on the operating frequency and core flux density, and can be calculated by [39–41]:

$$Vol_c = 2A_i\left(\sqrt{\frac{A_w}{r_w}}(r_w+1)+\frac{d_c}{\sqrt{K_c}}\right) \tag{4}$$

d_c is given by:

$$d_c = \sqrt{4A_i/(\pi K_c)} \tag{5}$$

The core dimensions A_i and A_w can be determined using the basic equations relating the design parameters such as B_m, $f\left(=\frac{1}{T}\right)$ and S, to the core dimensions as follows [40]

$$A_i = \frac{E_t}{4.44fB_mK_s} \tag{6}$$

$$A_w = \frac{S}{2.22JA_iK_sK_wB_mf} \tag{7}$$

where E_t can be calculated as

$$E_t = K_t\sqrt{S/1000} \tag{8}$$

where:

$$\mathrm{K}_t = \sqrt{4.44fr} \tag{9}$$

P_{Tco} can now be calculated by multiplying the power per unit volume using (1) by the core volume using (4), as shown in (10).

$$P_{Tco} = P_vVol_c \tag{10}$$

P_{Tcu}, can be calculated as in (11), based on the leakage inductance and winding ac resistances.

$$P_{Tcu} = {I_{lk}}^2R_p + \frac{{I_{lk}}^2}{N_a^2}R_s \tag{11}$$

I_{lk} can be calculated as [16]:

$$I_{lk} = \overline{I_B}\sqrt{\frac{5-4D_1}{3}} \tag{12}$$

R_p and R_s can be calculated as in (13)and (14) [42]:

$$R_p = \rho_c\frac{l_{pp}}{A_{cup}}\left[1+\left(\frac{(r_{op}/\delta)^4}{48+0.8(r_{op}/\delta)^4}\right)\right] \tag{13}$$

$$R_s = \rho_c\frac{l_{ps}}{A_{cus}}\left[1+\left(\frac{(r_{os}/\delta)^4}{48+0.8(r_{os}/\delta)^4}\right)\right] \tag{14}$$

l_{pp} and l_{ps} can be calculated as in (15) and (16):

$$l_{pp} = \pi\frac{V_p}{E_t}\left(d_c+0.5\sqrt{A_i/K_c}\right) \tag{15}$$

$$l_{ps} = \pi\frac{V_s}{E_t}\left(d_c+0.5\sqrt{A_i/K_c}\right) \tag{16}$$

3.2. Choke Core and Copper Losses

The fluctuation of the flux density of the choke is very small due to the low ripple in the choke coil current. Therefore, the core losses per unit volume of the choke coil can simply be calculated using the Steinmetz empirical equation (assuming the same core material as that of the transformer) as [32]:

$$P_{vc} = Kf^{\propto}B_{mc}^{\beta} \tag{17}$$

Based on (17) and the volume of the core, the choke coil core losses can be calculated as in (18):

$$P_{Cco} = MPL.A_{cuc}\, Kf^{\propto}B_{mc}^{\beta} \tag{18}$$

A_{cuc} can be calculated as in (19) (see Figure 4). MPL can be calculated as in (20):

$$A_{cuc} = W_c H_c \tag{19}$$

$$MPL = 2(W_w + H_w + H_c) \tag{20}$$

W_w, H_w, W_c and H_c are shown in Figure 4. Normally, core dimensions have their values related to each other by known constants such as:

$$K_{wH} = H_w / W_w \tag{21}$$

$$K_{wc} = A_{wc} / A_{cuc} \tag{22}$$

$$A_{pc} = A_{wc} \times A_{cuc} \tag{23}$$

A_{wc} equals $W_w \times H_w$, and A_{pc} can be calculated as in (24) [43]:

$$A_{pc} = \frac{2En \times 10^{-4}}{B_{mc} J K_u} \tag{24}$$

En can be calculated as

$$En = 0.5 L_B \overline{I_B}^2 \tag{25}$$

where L_B can be determined based on the D_1 (see Figure 3 [37]), f, V_B and ΔI_B as shown in (26) for the boost operation of the SST [16].

$$L_B = \frac{(D_1 - 0.5)V_B}{f \Delta I_B} \tag{26}$$

W_w H_w can be calculated based on (21). Based on (22) and (23), A_{wc} and A_{cuc} can be found. To find H_c, A_{cuc} is assumed as a square cross-section.

The choke coil copper losses can be calculated as in (27):

$$P_{Ccu} = {I_B}^2 R_c \tag{27}$$

I_B can be calculated as in (28), and R_c can be calculated as in (29):

$$I_B = \overline{I_B} \sqrt{\frac{(1 - 0.5\vartheta)^2 + (1 + 0.5\vartheta)^2}{2}} \tag{28}$$

$$R_c = \rho \frac{N_c \times MLT}{A_{cuc}} \tag{29}$$

MLT is calculated as in (30) and N_c can be calculated by (31) [34].

$$MLT \cong \pi \left[\sqrt{{H_c}^2 + {W_c}^2} + W_w \right] \tag{30}$$

$$N_c = \frac{K_{uc} K_f I_{B-rms}}{J\sqrt{A_{pc} K_{cc}}} \tag{31}$$

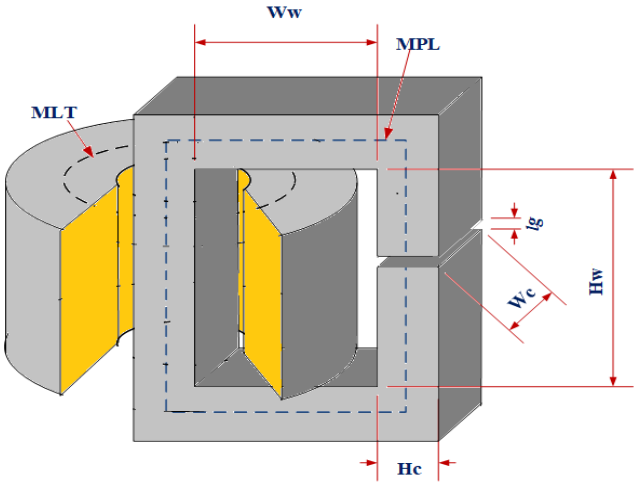

Figure 4. Choke coil geometry.

3.3. Power Electronics Losses

Power electronics losses have two main parts, conduction and switching. These losses can be calculated as [44,45]:

$$P_{cond\_T} = \frac{1}{T}\int_0^{ts} i_T(t).V_{ce}(t)dt \tag{32}$$

$$P_{sw\_T} = fE_{on+off}(V_{sw}, i_T, T_j) \tag{33}$$

$$P_{cond\_D} = \frac{1}{T}\int_0^{td} i_D(t).V_f(t)dt \tag{34}$$

$$P_{sw\_D} = fE_{rr}(V_d, i_D) \tag{35}$$

Based on the switching frequency, power electronics switches datasheets, average and RMS values of the current and voltage of the power electronics switches, the power electronics losses can be calculated as in [37]. The total power electronics losses can be calculated as in [37].

$$P_{PE} = P_{cond\_T} + P_{sw\_T} + P_{cond\_D} + P_{sw\_D} \tag{36}$$

4. CF-SST Design Optimisation Strategy

To find the optimum combination of the flux density and operating frequency, a design procedure is proposed. Two objective functions can be used: maximum efficiency, or minimum volume. The volume here is the combined volume of the transformer Vol_T, chock coil Vol_{Cc} and converters' heat sink Vol_{Hs}.

Vol_T and Vol_{Cc} are given in (36) and (37), based on the core dimensions of the transformer and chock coil calculated in Sections 3.1 and 3.2.

$$Vol_T = 2(2w_w + dc + l)(H_w + 2dc + 2l)(2w_c + dc + 2l) \tag{37}$$

$$Vol_{Cc} = 2(2w_{wc} + dcc)(H_{wc} + 2dcc)(2w_c + dcc) \tag{38}$$

Vol_{Hs} depending on the power electronic losses can be calculated as [46]:

$$Vol_{Hs} = Vol_r / \mathrm{R}_{th}, \tag{39}$$

R_{th} can be calculated as [46]:

$$R_{th} = \frac{T_j - T_A}{P_{PE}} \tag{40}$$

The optimisation constraints for both objective functions are voltage per turn ($E_t < \sigma$), clearance between two coils ($l > \xi$), transformer core flux ($B_{min} < B < B_{max}$) and the operating frequency ($f_{min} < f < f_{max}$). When the minimum volume objective function is used, a minimum efficiency constraint can be set. The flowchart of the design procedure is shown in Figure 5.

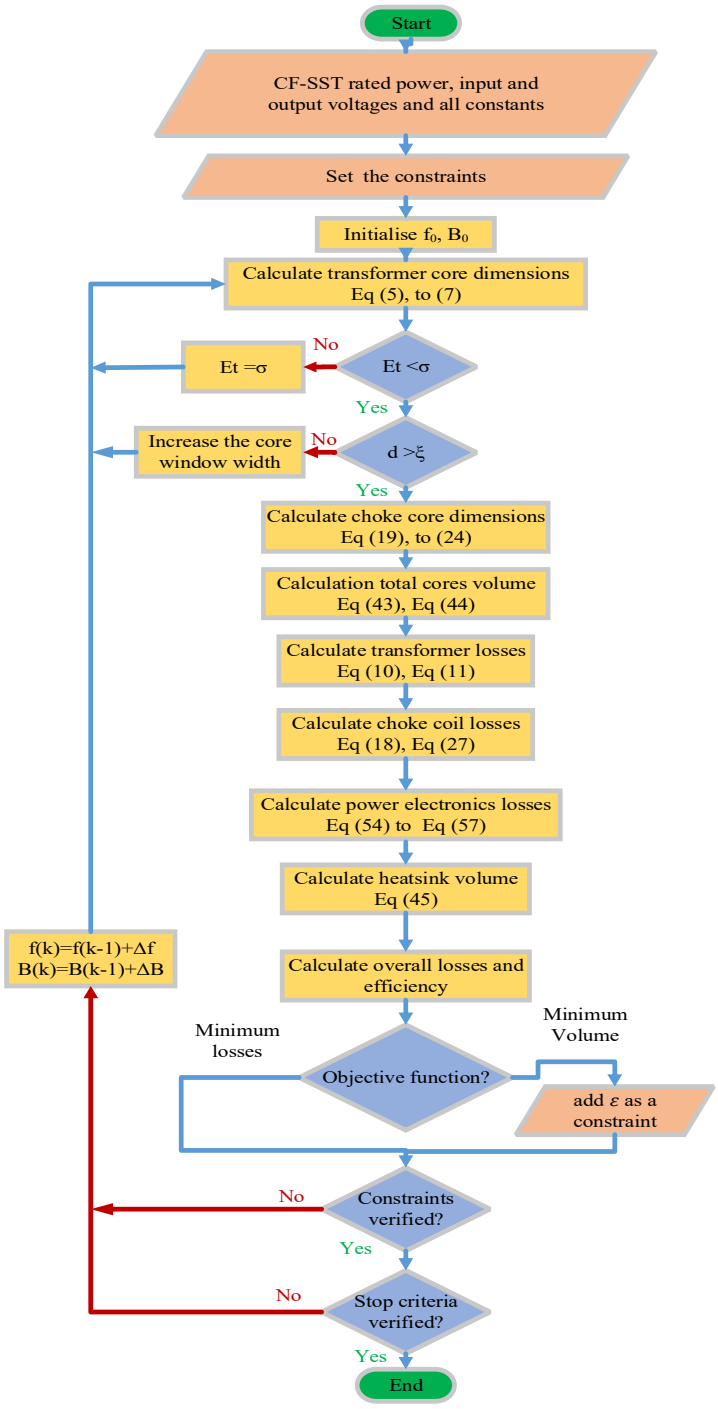

Figure 5. CF-SST optimisation flow chart.

Initially, CF-SST rated power, input and output voltages are entered into the algorithm. In addition, all constants used in the design are entered. The design constraints σ, ξ are set, as well as the initial flux density and operating frequency B_o and f_0. Using these initial values, the dimensions of the transformer core are calculated. If E_t is more than σ, E_t is set to equal σ. If l is less than ξ, the transformer window width is increased until $l > \xi$. The core dimensions of the transformer and choke coil are then calculated according to (19) to (24), (43) and (44). Using these dimensions, the core and copper losses are calculated as in (10), (11), (18) and (27). The power electronics losses are calculated using (54) to (57). Based on the power electronics losses and (45), the heat sink volume is then calculated. Now all the volumes and losses have been determined. Depending on the optimisation target (minimum losses or minimum volume), the optimisation is carried out until the end criteria are met. The end criteria are the value difference between successive iterations, number of iterations and constraints tolerance.

5. Simulation Results

Simulation work contains two parts; the first part is a validation of the analytical power losses calculation. The second part is a case study for designing a 1.0 MW DC/DC CF-SST using the proposed method.

5.1. Validation of Power Losses

A 1.0 MW DC/DC is considered with a low voltage (supply side) of 600 V and a high voltage of 18 kV. Due to the high supply current (1.7 kA), four parallel H-bridges are employed to reduce the switches currents to 417 A. For the high voltage side, six series H-bridges are employed to reduce the voltage stress on the switches. The transformer dimensions are shown in Table 1, and the choke coil dimensions are shown in Table 2.

Table 1. Transformer Dimensions.

Parameter	Value
Iron core cross-section	0.0147 m^2
Diameter of the core circumscribing circle	0.158 m
Width of winding window	0.216 m
Height of winding window	0.541 m
Number of primary turns	21 Turns
Number of secondary winding turns	325 Turns
Width of the winding allowing for clearance	0.004 m
Distance between windings	0.05 m
Height of winding	0.441 m

Table 2. Choke Coil Dimensions.

Parameter	Value
Iron core cross-section	0.0375 m^2
Diameter of the core circumscribing circle	0.25 m
Width of winding window	0.178 m
Height of winding window	0.265 m
Number turns	36 Turns
Area product	23.48 m^4

5.1.1. Transformer Core Losses

Core material SURA No18 [47] is used. Operating frequency and flux density values are set to 1.0 kHz and 0.96 T, respectively. Finite element analysis (FEA) is carried out using ANSYS Workbench to compare core losses against those calculated analytically. All the power losses curves at different frequencies from the core material datasheet are fed to ANSYS. ANSYS is employed to generate the constant of the power losses empirical Equations (1) and (17)) (K, α and β). Figure 6 shows ANSYS transformer core model.

The high voltage and low voltage windings are divided into two parts. The low voltage windings are placed near the core limb and the high voltage windings are placed over the low voltage windings to reduce the windings to ground voltage. A 1200 V input voltage waveform, as shown in Figure 7, is injected to the transformer primary winding. This voltage is the output of H-bridge 1 under discharging mode and 60% duty cycle. The FEA eddy current and hysteresis losses are shown in Figure 8 The average core losses of the transformer are determined by ANSYS for different duty cycles at the low voltage side and compared to those calculated analytically using (10); the results are presented in Figure 9. The difference between the analytical and numerical results is up to 18%. This is mainly due to the fact the parameters of the iGSE equation (K, β and α) are estimated by curves fitting of the materials losses curves under sinusoidal excitation, Equation (1). The difference decreases when the shape of the excitation voltage becomes closer to sinusoidal waveform.

It can be seen from Figure 9 that the core losses increase with the decreases in the duty cycle. This is due to the increase in the width of the injected voltage to the transformer.

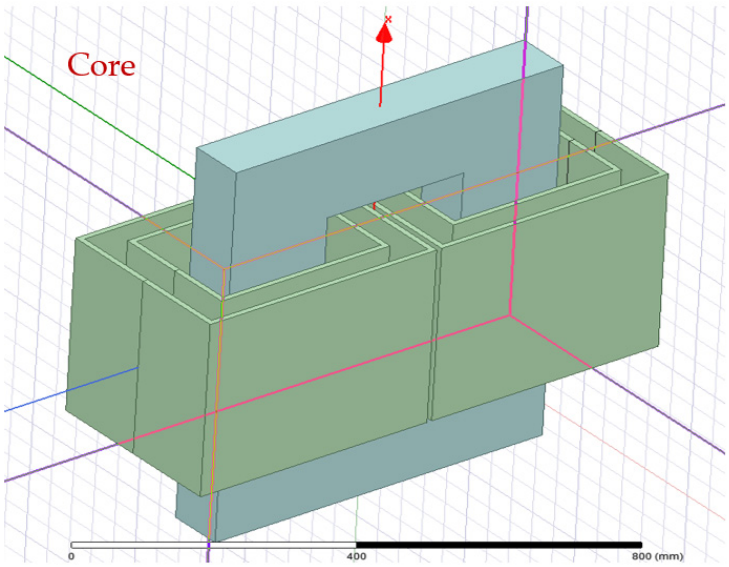

Figure 6. Ansys model for the CF-SST transformer core.

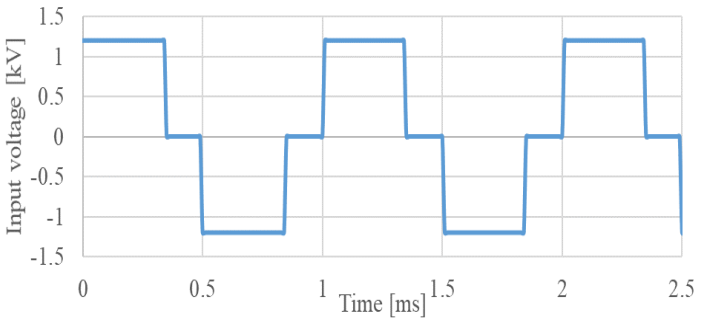

Figure 7. Injected voltage waveform to the CF-SST transformer primary voltage.

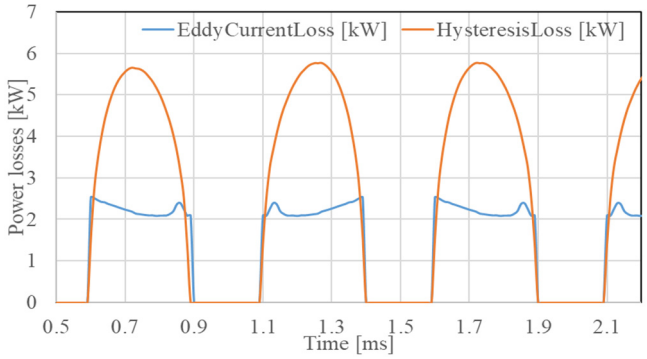

Figure 8. Eddy current and hysteresis losses by ANSYS.

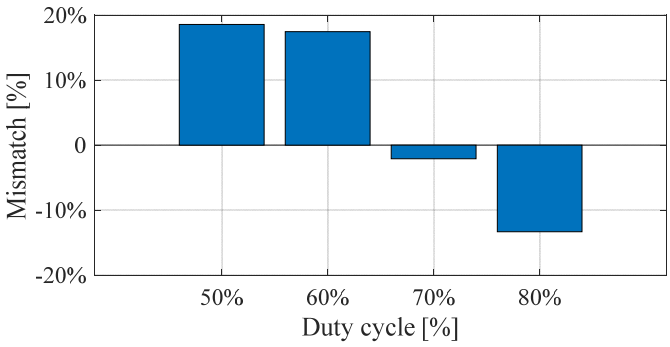

Figure 9. Core losses mismatching between ANSYS and analytical methods at different duty cycles.

5.1.2. Power Electronics Losses

A Simulink model for the CF-SST is built in the Matlab Simulink platform. The IGBT module 5SNG 0450X330300 [48] is used. The main parameters of this module are shown in Table 3. The IGBT junction temperature is assumed to be 125 °C. The on-state resistances for the IGBT (r_{CE}) and the diode (r_f) are calculated from the typical on-state characteristic relationship between V_{CE} and I_C . They are $r_{CE} = 3.2\ \text{m}\Omega$ and $r_f = 2\ \text{m}\Omega$ at 125 °C junction temperature. Matlab Simulink calculates the power electronics losses using a 3-D lookup table from the manufacturer datasheets [49], as shown in Figure 10 the switching instances, switch voltage, switch current and junction temperature are fed into a 3-D lookup table to obtain the instant switching losses. This table is based on the curves of the turn ON and OFF energy from the switches datasheet at different junction temperatures. The instant switching losses are averaged to obtain the switching losses. Similarly, for the conduction losses, the switch voltage, switch current and junction temperature are fed into another 3-D lookup table to obtain the instant conduction losses. This lockup table is based on the switch current and switch drop voltage at different junction temperatures Figure 11 shows the mismatch in power electronics losses calculated analytically, and by Matlab simulation at different switching frequencies and full load. The error is less than 11%. This error is due to the fact that in the analytical equations the switch current is assumed constant and equal to the supply or the load current while in simulation the switching transient current peaks are taken into account. Figure 12 shows the analytical results for the transformer copper and core losses, choke coil copper and core losses and power electronics losses at different operating frequencies and a fixed flux density of 1.0 T. At low frequencies, copper losses are dominant, while at frequencies higher than 200 Hz, power electronics losses become dominant. These curves depend on the core materials and power electronic devices technology. The core losses of the choke coil are small because the change of the flux density of the choke coil core is very small. The analytical equations are now validated, and can be used to design the SST.

Table 3. IGBT Main Parameters (125 °C).

Parameter	Value	Parameter	Value
V_{CE0}	3.1 V	E_{on+off}	1.43 J
I_{ref}	450 A	V_{f0}	2.25 V
V_{ref}	1800 V	E_{rr}	0.58 J

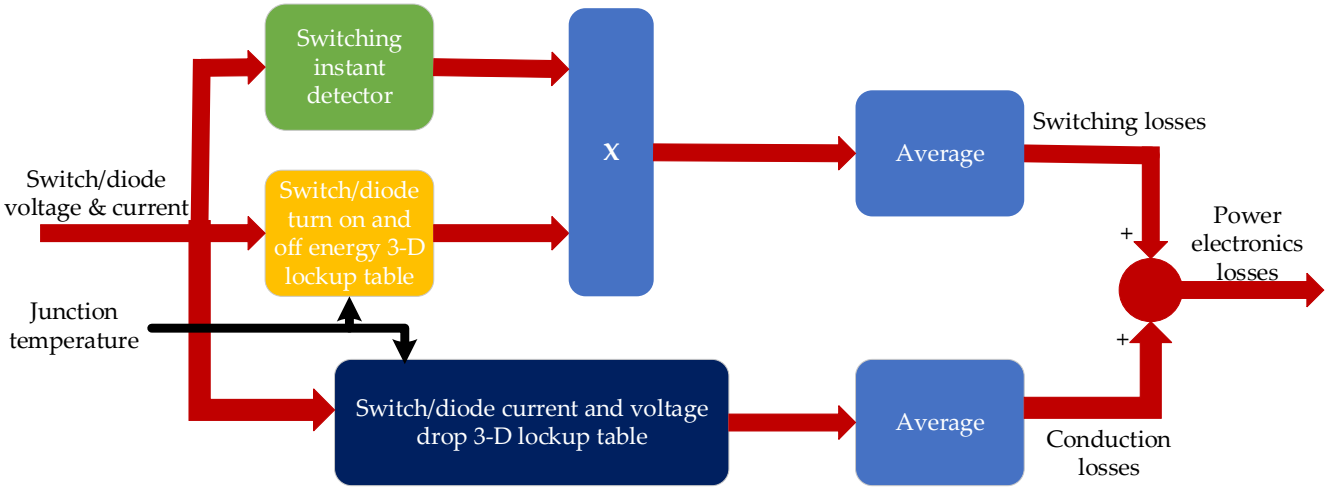

Figure 10. Power electronics losses methodology by Matlab Simulink platform.

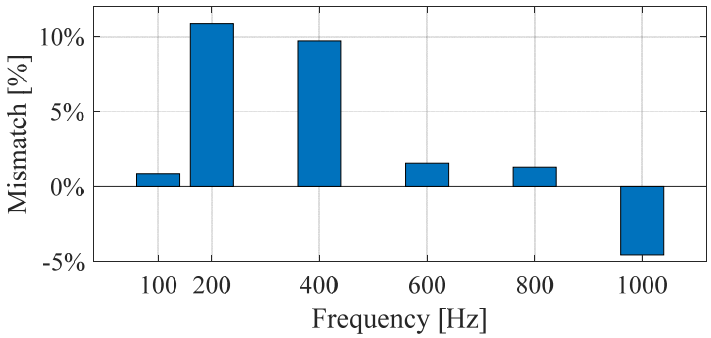

Figure 11. Power electronics losses mismatching between simulation and analytical method at different switching frequencies.

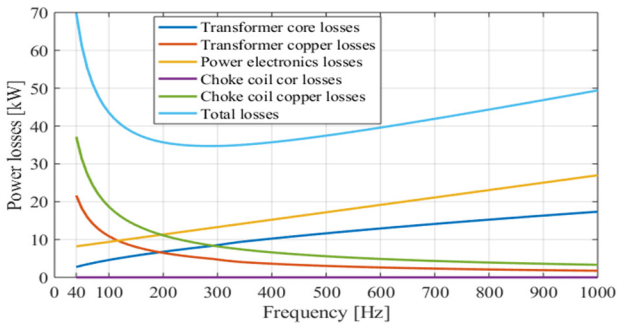

Figure 12. CF-SST copper, core and power electronics losses (Analytical).

5.2. CF-SST Design, Case Study

In this section, a case study for designing a new 1.0 MW CF-SST using the proposed optimisation strategy is presented. Before the design procedure is presented, however, the losses of the 1.0 MW CF-SST described in Table 2 under different operating frequencies

and a fixed flux density (1.0 T) are discussed first, in order to highlight the importance of considering all losses when searching for the optimum values of the flux density and frequency. The total transformer losses (copper & core), power electronics losses and the total CF-SST losses (total transformer, choke coil and power electronics losses) are shown in Figure 13. If the transformer losses, on their own, and are considered as the main factor to find the optimum operating frequency, it will lead to operating the CF-SST at a suboptimal frequency in terms of overall losses. For example, if only the transformer losses are considered, the optimum frequency is 240 Hz and the total CF-SST power losses, at this frequency, is 34.94 kW (96.51% efficiency). If the power electronics losses are added and ignoring the choke coil losses, the optimum frequency is 150 Hz and the total losses are 37.93 kW (96.2% efficiency). However, if the total CF-SST power losses are considered, the optimum frequency is 280 Hz and the total power losses are 34.72 kW (96.52% efficiency), which is about 3% less (0.1% efficiency higher) if the transformer losses only are considered and about 10.4% less (0.4% efficiency higher) if the choke coil losses are ignored. This shows the importance of considering all losses when designing the CF-SST. The total CF-SST losses under different operating frequencies and core flux densities are shown in Figure 14. An operating frequency of about 350 Hz seems to be the optimum value for minimum power losses over a range of flux density from 0.1 T to 1.2 T. The optimisation algorithm presented in Section 4 is employed under constraints shown in (41). The unconstrained nonlinear optimisation algorithm is employed as the optimisation solver. The optimum operating frequency for minimum losses (maximum efficiency) is 372 Hz and flux density is 0.249 T. At these values, the CF-SST system efficiency is 96.7%. In some applications, the volume/weight is the key parameter for the design. Figure 15 shows the total volume of the cores housing (transformer and the choke coil) under different frequencies and flux density values.

$$\left.\begin{array}{c} E_t < 100 \\ Vl > 0.5 \text{ mm} \\ 0.1 \text{ T} < B_m < 1.2 \text{ T} \\ 40 \text{ Hz} < f < 12 \text{ kHz} \end{array}\right\} \quad (41)$$

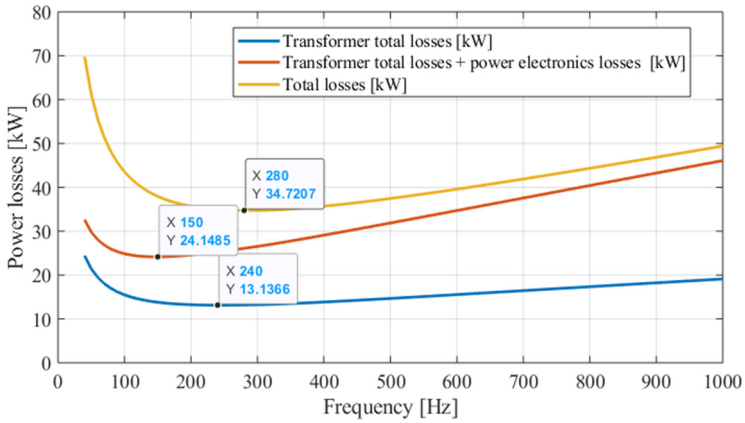

Figure 13. CF-SST transformer losses, transformer & power electronics and total CF-SST losses (Analytical).

The color of the surface represents the percentage of the total losses. The higher the operating frequency, the lesser the core volume, but at the expense of increased losses. Table 4 shows the design results when the objective function is selected as a minimum volume for different minimum efficiency constraints. Additionally, Figure 16 shows the volume for each core and heatsink at the minimum efficiency constraints. The volume of the cores increases with the increase of the minimum efficiency due to the decrease in the frequency, while the heat sink volume decrease due to the power electronics losses decrease with the decrease of the frequency. If the power losses are not the key factors in the design,

the lowest volume of the CF-SST cores can be achieved. If the system efficiency is the key factor, a tradeoff between the efficiency and the volume of the core can be considered. To gain a minimum core volume for maximum possible efficiency, the optimum operating frequency is 372 Hz and the flux density of 0.249 T. In this case, CF-SST efficiency is greater than 97.5%.

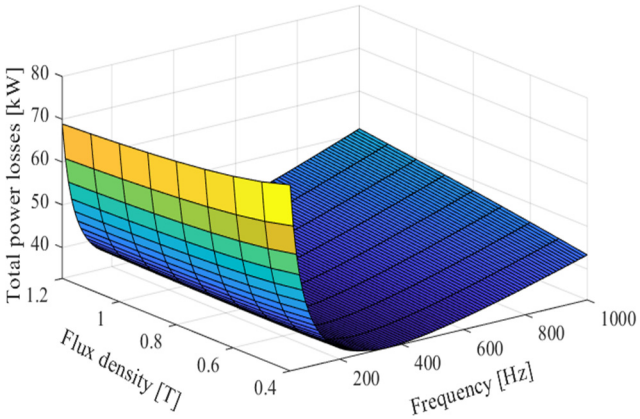

Figure 14. Total CF-SST losses at different operating frequencies and flux density (Analytical).

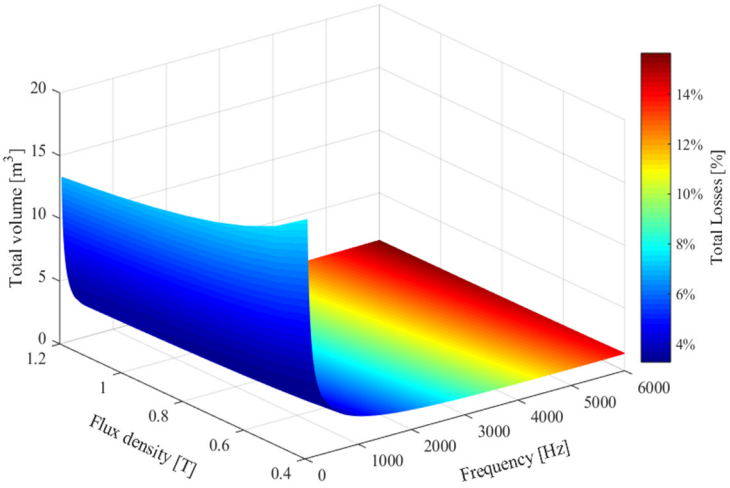

Figure 15. Total cores volume at a different frequency and flux density values (Analytical).

Table 4. Transformer Dimensions.

Efficiency	Optimum Flux [T]	Optimum Frequency [Hz]	Total Cores Volume [m^3]
>80	1.2	3613	1.142
>90	1.2	3275	1.144
>92	1.2	2318	1.199
>93	1.2	1840	1.274
>94	1.2	1359	1.419
>95	1.18	962	1.684
>95.5	1.056	809	1.8988
>96	0.903	647	2.245
>96.5	0.651	470	3.001
>97.5	0.249	372	5.245
>98		Not achievable	

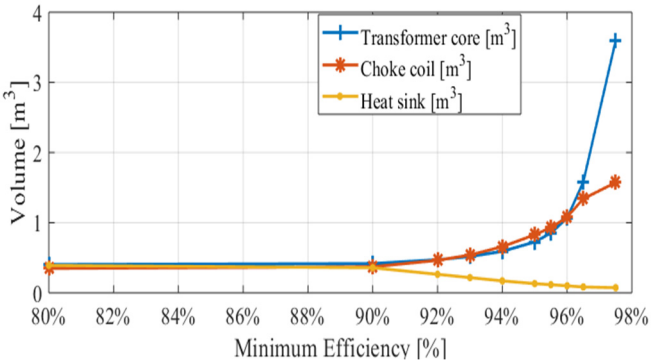

Figure 16. Cores and heat sink volume at optimum flux and frequency under minimum efficiency constraints.

6. Conclusions

The current source solid-state transformer (CF-SST) optimisation strategy for MV grid-connected systems is presented. Based on the manufacturer datasheets, core and power electronic losses equations are derived. The nonlinear nature of the transformer voltage waveforms is considered when calculating the core losses. Analytical equations are verified numerically using ANSYS and MATLAB. A design optimisation strategy has been presented, with the objective function being minimum power losses or minimum core housing volume.

The constraints are the voltage per turn for the transformer, the clearance between the transformer windings, the minimum and the maximum operating frequency and the flux density and the minimum efficiency. A 1.0 MW, 0.6/18 kV CS-SST is considered as a case study. Comparing the results in the last section, for fixed flux density 1.0 T, the optimum frequency is 284 Hz, which has 34.72 kW losses (96.53% efficiency) when employing the optimiser, which gives 0.01% higher than the value in the previous section.

For minimum losses, the optimum operating frequency is 372 Hz and the flux density is 0.249 T. In this case, the CF-SST efficiency is 96.7%. For a minimum total cores housing volume and converters heat sink volume, the minimum possible volume is 1.142 m^3 at operating frequency 3613 kHz and the flux density 1.2 T to achieve CF-SST minimum efficiency of 80%. For minimum possible volume for maximum possible efficiency (97.5%) is 5.245 m^3. The operating frequency, in this case, is 372 Hz and the flux density is 0.249 T.

The merit of the proposed method lies in its simplicity as it enables the designer to optimise the system parameters, including operating frequency, flux density and core dimensions fairly quickly using an algorithm that is based solely on analytical equations. This fast design procedure, however, produces less accurate results, mainly in terms of core losses, as compared to numerical methods. This is because the analytical equations used in the optimiser are based on empirical equations or some assumption for simplicity. Nevertheless, the proposed method would be very useful for practicing engineers as an initial fast optimisation step, enabling them to take design decisions before building a detailed numerical model. The numerical model can then be used for design verification and tuning.

This paper did not consider stray inductance and capacitance, and these will therefore be considered in future work. Furthermore, future work includes employing different core materials, power electronics parameters, converters configuration and cooling systems for the transformer and converters.

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Nomenclature

Notation	Nomenclature
A_{cuc}	Cross-sectional area of the choke coil core
A_{cup}	Transformer cross-sectional areas of the primary winding conductors
A_{cus}	Transformer cross-sectional areas of the secondary winding conductors
A_i	Transformer core cross-sectional area
A_{pc}	Area product of the choke coil core
A_w	Transformer core window area
A_{wc}	Choke coil core window area
B_m	Transformer maximum flux density
B_{max}	Maximum transformer core flux
B_{mc}	Choke coil maximum flux density.
B_{min}	Minimum transformer core flux
B_o	Initial flux density
CF-DAB	Current-fed Dual Active Bridge
D	Duty cycle of the transformer voltage
D_1	Duty cycle of the H-bridge 1
DAB	Dual Active Bridge
d_c	Effective core diameter of the transformer
dcc	Choke coil circumscribing circle
E_t	Transformer's voltage per turn
En	Energy in watt-seconds
ESS	Energy Storage System
f	Transformer operating frequency
f_{min}	Minimum operating frequency
f_{max}	Maximum operating frequency
f_0	Initial frequency
H_c	High of the choke coil core cross-section
H_w,	Height of the choke coil core window
I_B	RMS value of the supply current
I_{lk}	RMS value of the leakage inductance current (primary current)
i_T	Switch current when the switch is ON
$\overline{I_B}$	Average supply current
J	Current density
K_c	Ratio of the net core cross-sectional area to the circumscribing circle of the transformer
K_{cc}	Choke coil ratio of the winding area to the core cross-section area.
K_f	Choke coil filling factor
K_s	Transformer core staking factor
K_u	Choke coil window utilization factor
K_{uc}	Effective window factor for the choke coil core
K_w	Transformer winding fill factor.
K, α, β	Core material power losses constants

l	Clearance distance between the transformer windings
L_B	Choke coil inductance
l_{pp}	Total length of the primary winding of the transformer
l_{ps}	Total length of the secondary winding of the transformer
MLT	Choke coil mean length of the winding turn
N	Number of turns
N_a	Transformer turns ratio
N_c	Choke coil total number of turns
P_{Tco}	Transformer core losses
P_{Tcu}	Transformer copper losses
P_{cond_D}	Conduction losses of the diode
P_{cond_T}	Conduction losses of the switch
P_{sw_D}	Switching losses of the diode
P_{sw_T}	Switching losses of the switch
P_v	Transformer time-average power losses per unit volume
r	Constant depending on the flux and ampere-turn of the transformer.
RES	Renewable Energy Source
r_{CE}	On-state resistances for the IGBT
R_c	Choke coil resistance
r_f	On-state resistances for diode
r_{op}	Radii of the transformer primary winding conductors, respectively
r_{os}	Radii of the transformer secondary winding conductors, respectively
R_p	Transformer ac primary winding resistance
R_s	Transformer ac secondary winding resistance
R_{th}	Thermal resistance
r_w	Ratio of the winding window height to the width for transformer core
SST	Solid State Transformers
T	Switching period
T_A	Ambient temperature.
td	Time when the diode is OFF
T_J	Junction temperature
ts	Time when the switch is OFF
V_{ce}	Collector to emitter voltage, when the switch is ON
V_{max}	Maximum voltage.
Vol_{Cc}	Chock coilvolume
Vol_{Hs}	Converters' heat sink volume
Vol_T,	Total volume of the transformer
Vol_r	Volumetric resistance
VF-DAB	Voltage-fed Dual Active Bridge
V_p	Primary voltage of the transformer
V_s	Secondary voltages of the transformer
W_c	Width of the choke coil core cross-section
W_w,	Width of the choke coil core window
ΔI_B	Maximum allowed ripple in the dc supply current
ΔB	Transformer peak-to-peak flux density
ρ_c	Resistivity of the winding material
δ	Skin depth.
ξ	Clearance between two coils constraint
σ	Voltage per turn constraint
ϑ	Ratio of the supply ripple current over the average supply current

References

1. She, X.; Huang, A.Q.; Burgos, R. Review of Solid-State Transformer Technologies and Their Application in Power Distribution Systems. *IEEE J. Emerg. Sel. Top. Power Electron.* **2013**, *1*, 186–198. [CrossRef]
2. Wang, G.; Konstantinou, G.; Townsend, C.D.; Pou, J.; Vazquez, S.; Demetriades, G.D.; Agelidis, V.G. A Review of Power Electronics for Grid Connection of Utility-Scale Battery Energy Storage Systems. *IEEE Trans. Sustain. Energy* **2016**, *7*, 1778–1790. [CrossRef]

3. Krishnamoorthy, H.S.; Rana, D.; Enjeti, P.N. A New Wind Turbine Generator/Battery Energy Storage Utility Interface Converter Topology with Medium-Frequency Transformer. In Proceedings of the 2013 28th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 17–21 March 2013.
4. Jayasinghe, S.D.G.; Vilathgamuwa, D.M.; Madawala, U.K. A Battery Energy Storage interface for wind power systems with the use of grid side inverter. In Proceedings of the 2010 IEEE Energy Conversion Congress and Exposition, Atlanta, GA, USA, 12–16 September 2010.
5. Thomas, S.; Stieneker, M.; Doncker, R.W.D. Development of a Modular High-Power Converter System for Battery Energy Storage System. In Proceedings of the 2011 14th European Conference on Power Electronics and Applications, Birmingham, UK, 30 September–1 August 2011.
6. Trintis, I.; Munk-Nielsen, S.; Teodorescu, R. A New Modular Multilevel Converter with Integrated Energy Storage. In Proceedings of the IECON 2011—37th Annual Conference of the IEEE Industrial Electronics Society, Melbourne, VIC, Australia, 7–10 November 2011.
7. Jih-Sheng, L.; Maitra, A.; Mansoor, A.; Goodman, F. Multilevel Intelligent Universal Transformer for Medium Voltage Applications. Proceedings of 40th IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, Hong Kong, China, 2–6 October 2005.
8. Sha, D.; Xu, G. *High-Frequency Isolated Bidirectional Dual Active Bridge. DC–DC Converters with Wide Voltage Gain*; Springer: Singapore, 2019.
9. Pan, X.; Li, H.; Liu, Y.; Zhao, T.; Ju, C.; Rathore, A.K. An Overview and Comprehensive Comparative Evaluation of Current-Fed-Isolated-Bidirectional DC/DC Converter. *IEEE Trans. Power Electron.* **2020**, *35*, 2737–2763. [CrossRef]
10. Pan, X.; Rathore, A.K. Comparison of Bi-Directional Voltage-Fed and Current-Fed Dual Active Bridge Isolated DC/DC Converters Low Voltage High Current Applications. In Proceedings of the 2014 IEEE 23rd International Symposium on Industrial Electronics (ISIE), Istanbul, Turkey, 1–4 June 2014.
11. Redl, R.; Sokal, N.O. Push-Pull Current-Fed Multiple-Output DC/DC Power Converter with Only One Inductor and with 0 to 100% Switch Duty Ratio. In Proceedings of the 1980 IEEE Power Electronics Specialists Conference, Atlanta, GA, USA, 16–20 June 1980.
12. Thottuvelil, V.J.; Wilson, T.G.; Owen, H.A. Analysis and Design of a Push-Pull Current-Fed Converter. In Proceedings of the 1981 IEEE Power Electronics Specialists Conference, Boulder, CO, USA, 29 June–3 July 1981.
13. Baumann, E.D.; Kheraluwala, M.N.; Gascoigne, R.W.; Divan, D.M. Performance Characterization of a High-Power Dual Active Bridge DC-to-DC Converter. *IEEE Trans. Ind. Appl.* **1992**, *28*, 1294–1301.
14. Zhao, B.; Yu, Q.; Sun, W. Extended-Phase-Shift Control. of Isolated Bidirectional DC–DC Converter for Power Distribution in Microgrid. *IEEE Trans. Power Electron.* **2012**, *27*, 4667–4680. [CrossRef]
15. Zhao, B.; Song, Q.; Liu, W. Power Characterization of Isolated Bidirectional Dual-Active-Bridge. DC–DC Converter with Dual-Phase-Shift Control. *IEEE Trans. Power Electron.* **2012**, *27*, 4172–4176. [CrossRef]
16. Xuewei, P.; Rathore, A.K. Novel Bidirectional Snubberless Naturally Commutated Soft-Switching Current-Fed Full-Bridge. Isolated DC/DC Converter for Fuel Cell Vehicles. *IEEE Trans. Ind. Electron.* **2014**, *61*, 2307–2315. [CrossRef]
17. Xuewei, P.; Rathore, A.K. Novel bidirectional snubberless soft-switching naturally clamped zero current commutated current-fed dual active bridge (CFDAB) converter for fuel cell vehicles. In Proceedings of the 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, USA, 15–19 September 2013.
18. Chen, R.Y.; Lin, R.N.; Liang, T.J.; Chen, J.F.; Tseng, K.C. Current-fed full-bridge boost converter with zero current switching for high voltage applications. In Proceedings of the 40th IAS Annual Meeting. Conference Record of the 2005 Industry Applications Conference, Hong Kong, China, 2–6 October 2005.
19. Wu, T.-F.; Chen, Y.-C.; Yang, J.-G.; Kuo, C.-L. Isolated Bidirectional Full-Bridge. DC–DC Converter With a Flyback Snubber. *IEEE Trans. Power Electron.* **2010**, *25*, 1915–1922.
20. Miura, Y.; Kaga, M.; Horita, Y.; Ise, T. Bidirectional isolated dual full-bridge DC–DC converter with active clamp for EDLC. In Proceedings of the 2010 IEEE Energy Conversion Congress and Exposition, Atlanta, GA, USA, 12–16 September 2010.
21. Hurley, W.G.; Wolfle, W.H.; Breslin, J.G. Optimized transformer design: Inclusive of high-frequency effects. *IEEE Trans. Power Electron.* **1998**, *13*, 651–659. [CrossRef]
22. Petkov, R. Optimum design of a high-power, high-frequency transformer. *IEEE Trans. Power Electron.* **1996**, *11*, 33–42. [CrossRef]
23. Zhang, L.; Zhao, Z.; Qin, J. Efficiency optimization design of DC-DC solid state transformer based on modular multilevel converters. In Proceedings of the 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 1–5 October 2017.
24. Youngsil, L.; Vakil, G.; Feldman, R.; Goodman, A.; Wheeler, P. Design optimization of a high-power transformer for three-phase dual active bridge DC-DC converter for MVDC grids. In Proceedings of the 8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016), Glasgow, UK, 19–21 April 2016.
25. Jauch, F.; Biela, J. Generalized modeling and optimization of a bidirectional dual active bridge DC-DC converter including frequency variation. In Proceedings of the 2014 International Power Electronics Conference (IPEC-Hiroshima 2014—ECCE ASIA), Hiroshima, Japan, 18–21 May 2014.
26. Mogorovic, M.; Dujic, D. Sensitivity Analysis of Medium-Frequency Transformer Designs for Solid-State Transformers. *IEEE Trans. Power Electron.* **2019**, *34*, 8356–8367. [CrossRef]

27. Fritz, N.; Rashed, M.; Bozhko, S.; Cuomo, F.; Wheeler, P. Analytical modelling and power density optimisation of a single phase dual active bridge for aircraft application. *J. Eng.* **2019**, *17*, 3671–3676. [CrossRef]
28. Tian, H.; Vaisambhayana, S.; Tripathi, A. Multi-objective Optimization and Modeling of High. Frequency Transformers for DC-DC Stage in Solid State Transformer. In Proceedings of the 2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019—ECCE Asia), Busan, Korea, 27–30 May 2019.
29. Olowu, T.O.; Jafari, H.; Moghaddami, M.; Sarwat, A.I. Physics-Based Design Optimization of High. Frequency Transformers for Solid State Transformer Applications. In Proceedings of the 2019 IEEE Industry Applications Society Annual Meeting, Baltimore, MD, USA, 29 September–3 October 2019.
30. García, P.; Saeed, S.; Navarro-Rodríguez, A.; García, J. Switching frequency optimization for a solid state transformer with energy storage capabilities. In Proceedings of the 2016 IEEE Energy Conversion Congress and Exposition (ECCE), Milwaukee, WI, USA, 18–22 September 2016.
31. Beiranvand, H.; Rokrok, E.; Liserre, M. Volume Optimization in Si IGBT based Dual-Active-Bridge Converters. In Proceedings of the 2019 10th International Power Electronics, Drive Systems and Technologies Conference (PEDSTC), Shiraz, Iran, 12–14 February 2019.
32. Steinmetz, C.P. On the law of hysteresis. *Proc. IEEE* **1984**, *72*, 197–221. [CrossRef]
33. Li, J.; Abdallah, T.; Sullivan, C.R. Improved calculation of core loss with nonsinusoidal waveforms. In Proceedings of the IEEE Industry Applications Society Annual Meeting, Chicago, IL, USA, 30 September–4 October 2001.
34. Hurley, W.G.; Wölfle, W.H. *Transformers and Inductors for Power Electronics*; John Wiley & Sons Ltd.: Chichester, UK, 2013.
35. Yue, S.; Yang, Q.; Li, Y.; Zhang, C. Core loss calculation for magnetic materials employed in SMPS under rectangular voltage excitations. *AIP Adv.* **2018**, *8*, 056121. [CrossRef]
36. Park, K.; Lee, H.; Hahn, S. Finite-Element Modeling and Experimental Verification of Stray-Loss Reduction in Power Transformer Tank With Wall Shunt. *IEEE Trans. Magn.* **2019**, *55*, 1–4. [CrossRef]
37. Hussain, E.K.; Abusara, M.; Sharkh, S.M. Power Losses Calculation for Medium Voltage DC/DC Current-Fed Solid State Transformer for Battery Grid-Connected. In Proceedings of the 2020 22nd European Conference on Power Electronics and Applications (EPE'20 ECCE Europe), Lyon, France, 7–11 September 2020.
38. Montoya, R.J.G. High-Frequency Transformer Design for Solid-State Transformers in Electric Power Distribution Systems. Master's Thesis, University of Arkansas, Fayetteville, 2015.
39. Bean, R.L. *Transformers for the Electric Power Industry*; McGraw-Hill: New York, NY, USA, 1959.
40. Say, M.G. *Alternating Current Machines*, 5th ed.; Pitman: London, UK, 1983.
41. Hochart, B. *Power Transformer Handbook*, 1st ed.; Butterworths: London, UK, 1987.
42. Hurley, W.G.; Wölfle, W.H. *Transformers and Inductors for Power Electronics: Theory, Design and Applications*, 1st ed.; Wiley: Hoboken, New York, USA, 2013.
43. McLyman, C.W. *Transformer and Inductor Design Handbook*; Marcel Dekker, Inc.: New York, NY, USA, 1978.
44. Arendt Wintrich, W.T.; Reimann, T. *Application Manual Power Semiconductors*; Semikron: Ilmenau, Germany, 2015.
45. Wintrich, A.; Ulrich, N.; Tursky, W.; Reimann, T. *Application Manual Power Semiconductors*; SEMIKRON International GmbH: Nuremberg, Germany, 2015.
46. Seshasayee, N. Understanding Thermal Dissipation and Design of a Heatsink. 2011. Available online: https://www.ti.com/lit/an/slva462/slva462.pdf?ts=1622694013435&ref_url=https%253A%252F%252Fwww.google.com.hk%252F (accessed on 25 July 2019).
47. Sawir, E. Language difficulties of international students in Australia: The Effects of Prior Learning Experience. *Int. Educ. J.* **2005**, *6*, 567–580.
48. ABB. LinPak Phase Leg IGBT Module. Available online: https://library.e.abb.com/public/766b5fc8ed264c47ae634455dbade759/5SNG%200450X330300%205SYA%201458-02%2012-2018.pdf (accessed on 25 February 2019).
49. MathWorks, Loss Calculation in a Three-Phase 3-Level Inverter. Loss Calculation in a Three-Phase 3-Level Inverter-MATLAB & Simulin-MathWorks United Kingdom. Available online: https://www.mathworks.com/help/physmod/sps/ug/loss-calculation-in-a-three-phase-3-level-inverter.html (accessed on 25 July 2019).