Developing CMOS compatible ElectroWetting-on-Dielectric (EWOD) microfluidic technology

Yifan Li

Abstract

The work presented in this thesis is associated with the development of electrowetting on dielectric (EWOD) technology. One of the main issues of concern was robustly driving droplet movement using low voltage without device malfunction caused by poor dielectric quality. In this work, anodic Ta_2O_5 dielectric, an alternative insulator with a high κ (8 to 25) was used to fabricate low voltage EWOD systems. The uniform and pinhole-free layer has a surface roughness of a few angstroms, enabling an ultra thin Amorphous Fluoropolymer (aFP) layer to be employed to reduce the EWOD driving voltage to 13V. The result shows that, when the κ reaches a certain level, a smooth insulating surface and a thin layer of aFP is more important than a higher value of the dielectric constant in achieving low voltage EWOD droplet maniulation.

Further achievements of this work is the integration of an active EWOD device with CMOS technology. One of the motivations behind this approach is based upon the desire to increase the number of control electrodes, requiring the implementation of on-chip microelectronic line-column drivers. Increasing the number of electrodes is attractive as it provides the opportunity to finely adjust droplet size, and also increases the number of droplets that can be moved simultaneously. Moreover, the integration can provide on chip sensing, which is disirable in Lab-on-a-chip applications. The tradeoffs associated with minimising the drive voltage while keeping the postprocess simple and low cost are assessed. Taking issues into account, the first active EWOD device was successfully fabricated and used to demonstrate droplet manipulation.

This thesis also reports two applications related to lab-on-a-chip and microrobotics developed using the above technologies. The capability to expand the system by using low voltage and active EWOD technology is highlighted in discussing future work.

Acknowledgements

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Acronyms and abbreviations

AFM	Atomic Force Microscope
aFP	amorphous Fluoropolymer
ALD(ALCVD)	Atomic Layer Chemical Vapour Deposition
BST	Barium Strontium Titanate
BZN	Bismuth Zinc Niobate
CA	Contact Angle
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical mechanical polishing
DEP	Dielectrophoresis
DI	Deionised
EDL	Electric Double Layer
EP	Electrophoresis
EWOD(EWD)	ElectroWetting on Dielectric
FET	Field-effect Transistors
FOV	Field of View
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
IDT	Interdigitated transducer
ITO	Indium Tin Oxide
LGA	Land Grid Array
LOC	Lab on a Chip
LPCVD	Low Pressure Chemical Vapour Deposition
MALDI	Matrix-Assisted Laser Desorption/Ionisation
MEMS	Microelectromechanical systems
OET	Optoelectronic Tweezer
PCB	Printed Circuit Board
PCR	Polymer chain reaction
PECVD	Plasma Enhanced Chemical Vapour Deposition
PEALD	Plasma enhanced Atomic Layer Chemical Vapour Deposition

PET   polyethylene terephalate

RF   radio frequency

RIE   Reactive Ion Etching

SAW   Surface Acoustic Wave

SPAD   Single Photon Avalanche Diodes

TDBD   Time-dependent Breakdown

TNT   trinitrotoluene

TTL   Transistor-Transistor Logic

μTAS   micro total analysis system

Chapter 1
Introduction

1.1 Introduction

ElectroWetting-on-Dielectric (EWOD) is a micro-electromechanical system (MEMS) technology for digital micro scale fluidic systems. While developed in early the 1960s and firstly used for fabricating integrated circuits (IC) in 1968, CMOS is now ubiquitous in electronic devices. Both these technologies benefit from the miniaturisation that conventional devices have experienced for a long time. The history of their development and convergence, will be introduced in the following sections together with the motivation of this thesis work.

1.2 MEMS, microfluidics and CMOS

For a long time human-beings have dreamt of building smart machines by manipulating atoms. In the late 1960s, researchers started to notice that semiconductor materials, such as the silicon used in CMOS integrated circuit manufacture can also be used for constructing micro sensors and actuators [1, 2]. This provided a chance to miniaturise conventional machines and produce much more complex, sensitive and precise electro-mechanical systems with more functions. These systems containing micro devices are often referred to as microsystems or Micro-Electro-Mechanical Systems (MEMS). From automobiles to medical instruments, MEMS devices have the potential to improve our living standards in significant and far-reaching ways. It was reported in 2005, that the market for MEMS devices reached an estimated $5 billion in 2005, and will increase to $12.5 billion through 2010 [1].

In nature, millions of microfluidic systems already exist, for example capillary vessels in human bodies, metabolism systems in plants. As MEMS technology develops, it becomes possible for similar systems to be produced for manipulating microlitre and nanolitre scale volumes of fluids. The first microfluidic MEMS device was not controlling liquid flow but air flow as a gas chromatographic air analyser [3] in 1979.

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[1] Source from "MEMS - A Roadmap to Technologies and Applications", by Electronics.ca Publications' web site.

After nearly 30 years of development, applications for microfluidics can be found in many fields, for example inkjet printing, projectors, healthcare-related applications (such as high-throughput screening, diagnostics, and drug delivery), particularly chemical analysis and synthesis, proteomics, and optical devices. For microfluidic MEMS devices, the market value of this technology was $3.2 billion in 2006 and is estimated to be $6.2 billion by 2011, with an average annual growth rate of 14.1% over the next five years[2]. In a review of microfluidics by Gravesen et al. in 1993, the implantable microsystems capable of sensing biology parameters, chemical analysis and drug delivery were reported to have generated the most interest for future microfluidic systems [4]. These systems were later called Lab-on-a-Chip (LOC, also known as micro-Total-Analysis-Systems (μTAS)) and bio-MEMS systems, which can manipulate and analyse biological fluidic samples in micro- and nano-litre volumes. These have emerged in recent years as potential solutions for automating repetitive laboratory tasks such as chemical detection, point-of-care diagnostics, cell separation and sample preparation [5–7].

Initially the micro plumbing systems, including structures and devices such as channels, pumps and valves in millimeter and micrometer scales are widely used to fabricate these systems [4]. However, these systems have drawbacks such as dead volume and stiction. These issues and other potential advantages have made digital microfluidic devices of interest. They are based on technologies such as dielectrophoresis (DEP), electrowetting on dielectrics (EWOD) and surface acoustic waves (SAW). They provide a potentially reconfigurable method of obtaining a bio-MEMS system [6, 8]. Of these, Electro-Wetting-On-Dielectrics (EWOD) technology appears to be an attractive option since it has a low power consumption (only micro-Watt [9]) making it well suited for the design and manufacture of microfluidic systems [6].

CMOS IC technology, which had its fabrication processes borrowed by MEMS 40 years ago, has already been developed into a substantial and expanding market. The sales of IC devices in 2006 hit a new record of $247.7 billion [3]. Meanwhile, integrated circuitry (including CMOS) and MEMS hybrid systems have gained a lot of interest. One of the most successful products is the Digital Light Processing (DLP) system based on a Digital Micromirror Device (DMD) fabricated by Texas Instruments in 1995 [10]. Most of the MEMS-CMOS integrated systems contain array structures, such as uncooled IR imaging, reflective displays, high-density inkjet heads, and biochemical sensor arrays, where CMOS addressing circuitry can solve the interconnect problems [11]. The special benefits of CMOS technology integrated with microfluidics

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[2]http://www.bccresearch.com/pressroom/RSMC036C.htm
[3]Reported by Semiconductor Industry Association

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was discussed by Liu in [12]. The ability for on chip detection and data processing can increase the possibility of building a successful in situ microfluidic system in the future. However, there are challenges in the integration work. Witvrouw et al. pointed out that the most attractive way of inserting the MEMS processes into a CMOS standard process flow for a hybrid system is the post-metal processing approach. The biggest issue in this approach is the MEMS process compatibility, especially the temperature [11]. Hence the development of low temperature CMOS compatible MEMS fabrication processes is necessary.

1.3 Motivation

The continuous and successful development in some technologies leads to their commercialisation at which point industry takes ownership and drives future developments. This has not yet happened to most elements of the EWOD technology, especially digital Lab-on-a-chip technology [13]. Although numerous EWOD applications have been demonstrated over the last 10 years [14–20], there are still novel developments emerging every year. To the author's knowledge, EWOD electrode arrays are still all being driven in a passive manner (without integrated on-chip control) with each electrode requiring its own interconnect and bond pads. Clearly, successful integration of CMOS and EWOD technology will remove this limitation (and many others) on system design and consequently increase the number of potential applications.

The Scottish Microelectronics Centre, where this work has been undertaken, has a very success demonstration of CMOS foundry wafers being post-processed with another technologly. In this example Micro Emissive Displays (MED) [4] have integrated Organic Light Emitting Polymer (OLED) technology with foundry CMOS. This project aims to do the same for EWOD technology.

1.4 Project objectives

The focus of this thesis is on developing EWOD technology that can be integrated with CMOS technology.

Clearly an EWOD chip will be much larger than at typical electronic integrated circuit CMOS chip. and some have identified that this kind of hybrid system may potentially have a high

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[4]website: http://www.microemissive.com/

cost [21]. The logical requirements for electrode addressing circuitry in EWOD systems is relatively simple, and with switching time in the millisecond range, there is no need to employ cutting edge sub-100 micron CMOS for integration. Hence a reasonable price (e.g. < £10 − 100 for a centimeter square chip for low volume R&D) is believed to be achievable and acceptable, especially if not all the LOC and bio-MEMS chips are required to be disposable. Clearly this price has the potential to be greatly reduced for high volume production.

It is apparent that a technology based on large electrode arrays requires that digital microfluidic systems must be integrated with CMOS circuitry if large numbers of individual electrodes are to be addressed with a sensible number of input signal channels. Such an approach for a dielectrophoresis (DEP) system is reported in [22].

If EWOD systems are to be integrated with CMOS chips then there are design and fabrication issues, mainly related to the dielectric insulation. The trade-off is between choosing a sufficiently thick CMOS compatible insulation layer that prevents electrolysis failure while also having a low operation voltage suitable for standard CMOS technologies. The issue is that low voltage operation requires thinner insulation layers. These issues will be addressed at length when developing and demonstrating an integrated EWOD-CMOS system.

1.5 Thesis content summary and layout

This thesis contains 9 chapters, including this introduction. The contents of the following chapters is presented below:

- **Chapter 2** provides a literature review and highlights and details the EWOD technology background knowledge, and the current achievements and applications that relate to this project.

- **Chapter 3** evaluates a single layer aluminium electrode EWOD devices by reporting contact angle measurements and droplet manipulation experiments.

- **Chapter 4** introduces CMOS process compatible anodic Ta_2O_5 as a pin-hole free, high κ material for fabricating EWOD systems. A thin amorphous fluoropolymer layer (referred to hereafter as aFP) together with anodic Ta_2O_5 are used to achieve a robust EWOD system operating at 15 V.

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- **Chapter 5** addresses the importance of having large EWOD electrode arrays and demonstrates the multi-level metallisaion fabrication of an EWOD electrode array.

- **Chapter 6** discusses packaging issues of passive EWOD electrode arrays and introduces an active EWOD electrode array with CMOS integrated circuitry.

- **Chapter 7** presents a test structure design that facilitates characterise the relationship between operating voltage (in Chapter 5 also defined as critical voltage) and the electrode configuration in a coplanar EWOD systems. The information gained is used in the design of a new coplanar EWOD structure with an operating voltage of 15V.

- **Chapter 8** presents some applications; a micro-swimming robot and a digital droplet dispenser.

- **Chapter 9** summarises the work, presents some conclusions and proposes possible future developments.

Chapter 2
ElectroWetting-On-Dielectrics - Theory and Application

2.1 Manipulating liquid in droplet form

Unlike traditional MEMS microfluidic systems, digital microfluidic systems do not contain mechanically moving parts such as pumps and valves. Liquid moves into and through the device as droplets rather than as continuous flow, and mostly on a planar surface rather than in channels.

Micro droplet can be manipulated in different ways [23, 24]. For example, Chaudhury and Whitesides first demonstrated liquid movement in droplet form using chemical capillary force [25]. Baroud et al., used laser light induced thermocapillary force to enable droplet manipulations in channels filled with flowing oil [26]. Linke demonstrated a high speed droplet motion pumped in the Leidenfrost regime (film-boiling) to sustain speeds of order 5cms^{-1} over distances of up to 1m [24]. Figure 2.1 gives illustrations of the above examples.

There are three main technologies used to realise digital microfluidic systems by manipulating liquid in droplet form: Dielectrophoresis (DEP), Surface Acoustic Wave (SAW) and ElectroWetting-On-Dielectrics (EWOD).

2.1.1 Dielectrophoresis (DEP)

Dielectrophoresis (DEP) technology has been developed for microfluidic applications for over ten years. It can be used in bio-chemical analysis and applications e.g. cell separation [27] and digital microfluidic systems [22].

The DEP force is generated when a dielectric body is introduced into an non-uniform electric field. The inhomogeneous energy variation across the body due to the non-uniform field strength will exert an imbalance of the coulomb force and hence create a directional force [22].
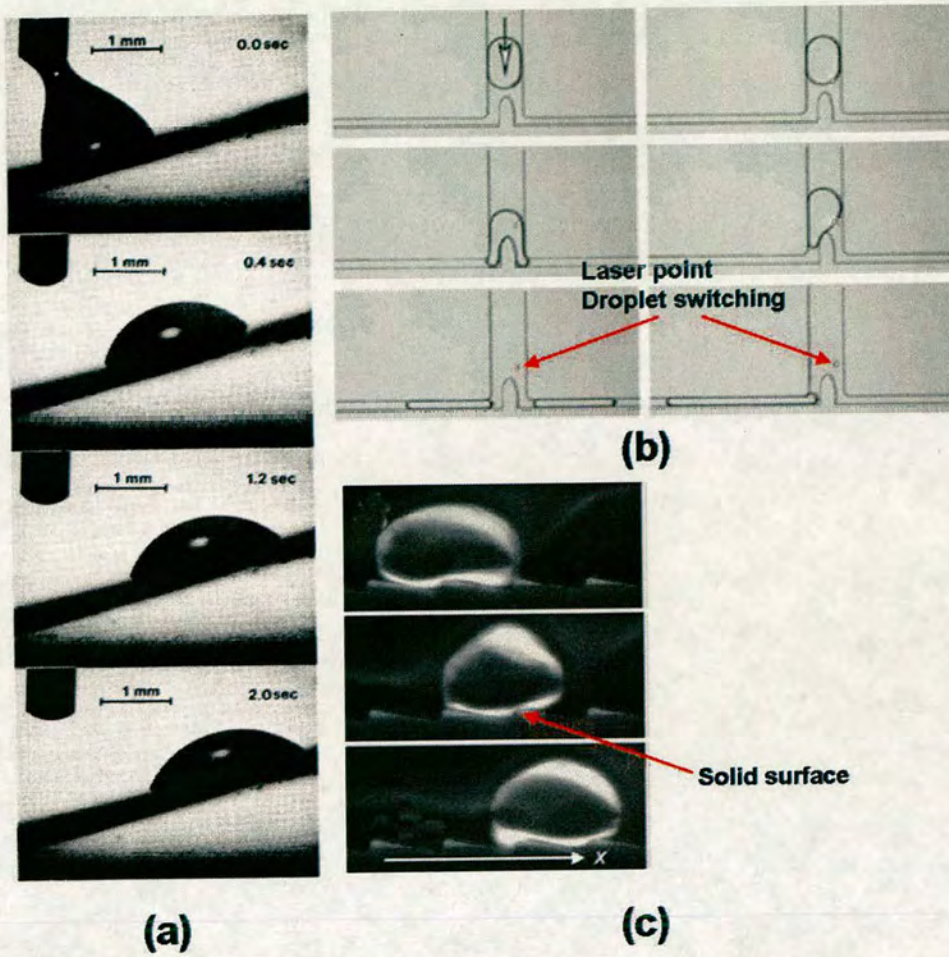
Figure 2.1: *Manipulating droplet in different ways. (a) Surface chemical capillary force enabled the droplet moving uphill [25]. (b) Switch on and off the laser point for droplet sorting using thermocapillary force [26]. (c) Propelling droplet in Leidenfrost regime (also called the film-boiling regime), where the droplet is separated from the supporting solid by a lubricating vapour layer [24].*

The DEP force generated on a polar droplet with a volume of V in a stationary, inhomogeneous electric field E can be calculated as:

$$\vec{F}_{DEP} = \frac{3}{2}V\epsilon_s f_{CM}\vec{\nabla}E^2 \tag{2.1}$$

where ϵ_s is the dielectric constant of the medium in which the droplet is suspended and f_{CM} is the real part of the Claussius-Mossotti factor which relates to the polarisation of the droplet assumed to be suspended in the medium.

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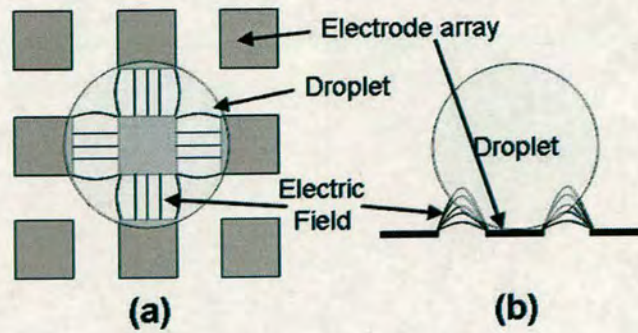
Figure 2.2: *Manipulating a polar droplet suspended in a non-polar partitioning medium using DEP force created by the fringing field of the electrode array. (a) Top view. (b) Side view. (refer to the work done in [22])*
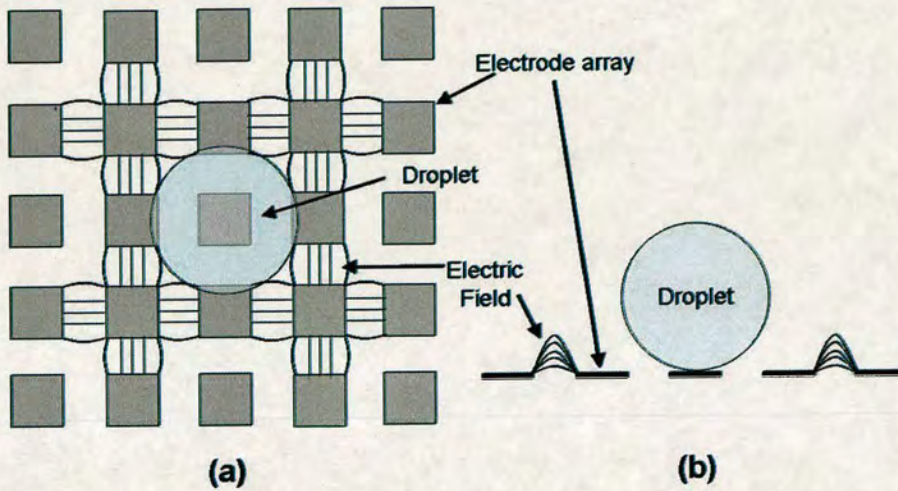
Figure 2.3: *Manipulating a non-polar droplet suspended in a polar partitioning medium using DEP force created by fringing field of the electrode array. (a) Top view. (b) Side view. (refer to the work done in [22])*

Manipulating droplets on the digital microfluidic DEP electrode arrays using $\vec{F}_{DEP}$ can be accomplished by two different methods. Figure 2.2 shows the manipulation of a polar droplet suspended in a non-polar partitioning medium. In this case, where the Claussius-Mossotti factor is positive, the droplet will be driven to the high electric field region by positive $\vec{F}_{DEP}$ [22].

On the other hand, if the droplet is non-planar and suspended in a polar medium, figure 2.3 illustrates the alternative DEP manipulation method. In this case, the droplet is trapped inside potential energy "cages". By moving the "cages" the droplet can be moved [22].

The application of both methods can lead to the manipulation of droplets on large electrode

arrays to perform different functions.

An example of a DEP system that has a 32 × 32 electrode array manipulating droplet size from 65pL to 110nL using 40 to 100V AC voltage with a frequency >2000Hz was reported in [22].

2.1.2 Surface Acoustic Wave (SAW)

Surface Acoustic Wave (SAW) technology is used in RF (radio-frequency) MEMS devices e.g. filters, oscillators, transformers [28] and image sensor surface cleaning in digital cameras.
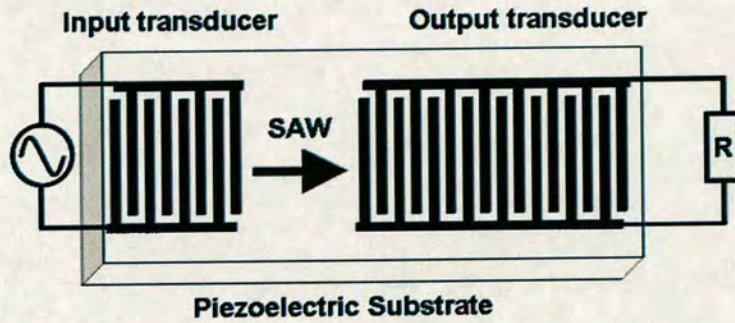
Figure 2.4: *Layout of a surface acoustic wave device. High frequency AC signals are input from the interdigitated transducers, creating a SAW across the piezoelectric substrate.*

A surface acoustic wave is a wave that travels along an elastic surface and which has an amplitude that typically decays exponentially with the depth of the substrate. Fig. 2.4 shows the layout of a SAW device. When applying an AC signal to the input of an interdigitated transducer (IDT) on a piezoelectric substrate, the high frequency signal will be converted into a periodic crystal deformation. If fed with the right frequency:

$$\lambda = \frac{v_{SAW}}{f} \tag{2.2}$$

then a monochromatic and coherent SAW will be launched (where v_{SAW} is the sound velocity of the substrate and λ and f are the frequency and the wavelength of the SAW) [8].

Figure 2.5 shows the basic interaction between a SAW and a fluid sitting on the piezoelectric substrate. When the wave meets the droplet, the wave energy will be partly transfered into the droplet. The damping of the SAW leads to the excitation of a sound wave in the droplet entering at an angle θ. If the amplitudes are high enough, the droplet can be moved [8].

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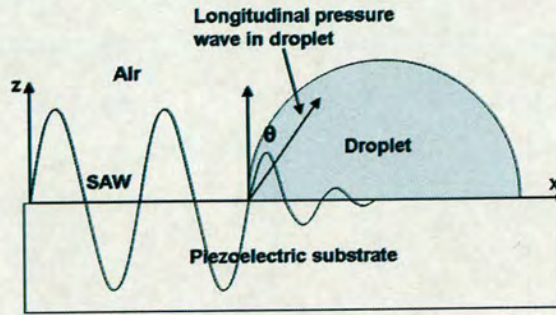
Figure 2.5: *Exciting a droplet using surface acoustic wave. (refer to the work done in [8])*
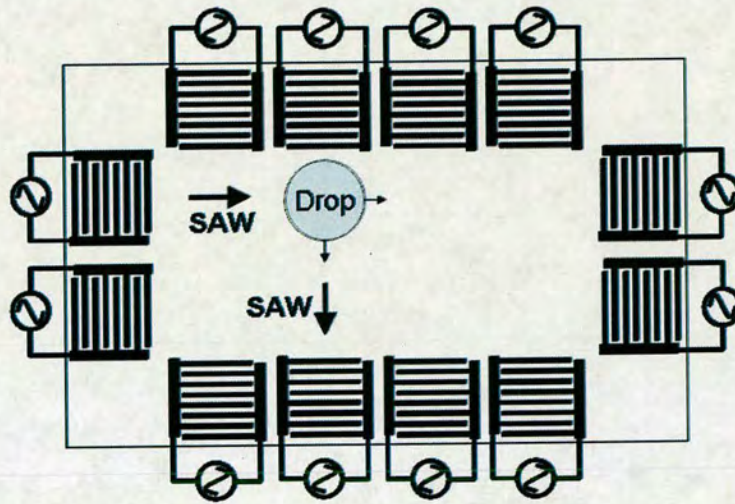
Figure 2.6: *Droplet manipulation array using SAW. The IDT electrodes are placed in x-y directions to achieve droplet 2-D movement. [8]*

By placing the IDT electrodes orthogonally, 2-D droplet movement on the plain surface can be initiated following the direction guided by surface acoustic waves, as shown in figure 2.6.

An example of a chip-based polymer chain reaction (PCR) digital fluidic bioprocessor using SAW technology was reported in [29].

2.2 Electro-Wetting on Dielectrics (EWOD)

In EWOD technology droplets are manipulated by electro-wetting of the dielectric (EWOD is sometimes called EWD), which changes the liquid-solid surface tension under the influence of an electric field. Before focusing on the technology, the relationship between the scaling of a

fluidic system size and the role of surface tension will be discussed.

2.2.1 Surface tension and system scaling

Surface tension is caused by the attraction between molecules of a liquid. It is a force proportional to the contact length between two immiscible media such as the solid-liquid interfacial tension. As a result, it scales down linearly with the system size. In the same system, gravity force scales down as the third power of the size while pressure scales down as the second power. For example, figure 2.7(a) [1] shows a droplet sticking to a tap by surface tension. It remains hanging until its size reaches a value such that the force of gravity detaches it. The force balance can be calculated using the following simple theory.

For the surface tension force F_σ holding the droplet:

$$F_\sigma = 2\pi r \sigma \tag{2.3}$$

where σ is the surface tension and r is the radius of the droplet.

For the gravity force:

$$F = \frac{4}{3}\pi r^3 \rho g \tag{2.4}$$

where r is the radius of the droplet, ρ is the density and g is the acceleration due to gravity. By combining equation (2.3) and (2.4), the critical droplet detaching radius can be determined:

$$r = \sqrt{\frac{3\sigma}{2\rho g}} \tag{2.5}$$

For typical liquids, the values of r are in the millimeter range [30]. If a $10\mu m$ mercury droplet ($\sigma = 484 mNm^{-1}$, $\rho = 13,550 kgm^{-3}$) is hanging, the required acceleration to remove it will be 55,000g. Obviously in sub-millimeter scale systems, the surface tension rather than the gravity force dominates droplet manipulation. Hence EWOD technology where nanolitre size droplets are manipulated using surface tension has great advantages.

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[1]This Wikipedia and Wikimedia Commons image is from the user Chris 73 and is freely available at http://commons.wikimedia.org/wiki/Image:Water_drop_animation.gif under the creative commons cc-by-sa 2.5 license.

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(a)   **(b)**   **(c)**
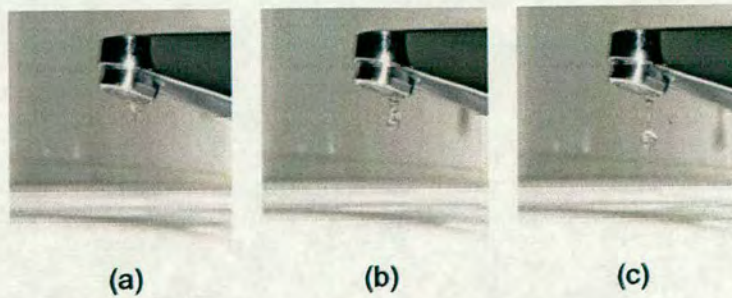
Figure 2.7: *(a) A small droplet initially attached to the tap. (b) When its size increases, it starts to detach. (c) After the critical radius is reached, the gravity force dominates and the droplet is detached from the tap.*

2.2.2 Contact angle and surface tension

2.2.2.1 Surface tension and surface free energy

Figure 2.8 shows a simple diagram of a droplet on a surface and can be used for studying the phenomenon in EWOD technology. The shape of the droplet viewed from the side is defined by the surface tensions (γ_{ls}, γ_{sg}, γ_{lg}, for calculation the environment is defined as a gas phase for convenience) at the three phase (solid-liquid, liquid-gas and solid-gas) contact line. Before providing more detail of this definition, the relationship between the terms surface tension and surface free energy needs to be understood.
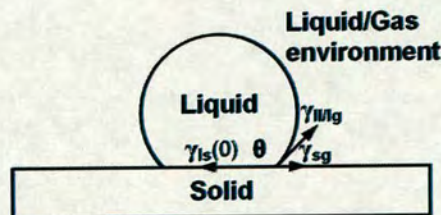
Figure 2.8: *Sessile droplet in EWOD system. The contact angle is defined by surface tensions at the three phase contact line.*

For a sessile droplet placed on a solid surface in a gaseous environment, the values of surface tensions at the three interfaces are related to the surface free energy. The terms surface tension and surface free energy are sometimes confused in the literature, leading to their interchangeable use to describe the same quantity. However, they can be equivalent under certain conditions.

Surface tension is strictly defined in [31], and is an excess quantity defined by

$$\left(\frac{\partial G}{\partial A}\right)_{T,\,p,\,n} = \gamma \tag{2.6}$$

where G is the Gibbs free energy and A is the interface area. Equation (2.6) is obtained by keeping the temperature T, pressure p and molecular number n (mass assigned to the model surface) constant [31]. When Gibbs first developed his theory, he showed that the surface tension cannot be equal to the surface free energy unless the adsorption at the surface is zero [32]. Hypothetically, only in a one-component system (a pure liquid in contact with its own vapour) can the above condition be achieved.

Considering the minor difference between these two during the practical work, the surface free energy is numerically estimated to be equal to the surface tension for convenience. Hence the term surface tension will be used to explain surface free energy related issues hereafter.

2.2.2.2 Contact angle and surface tension

Figure 2.8 shows the contact angle θ of a droplet defined by the three surface tensions in its equilibrium shape. The relationship between the θ and surface tensions can be derived through a thermodynamic variational approach [33].

If the equilibrium contact angle is changed, total surface free energy G in equation (2.6) will be altered. Assuming the change of angle θ to θ' is infitesimally small so that $\theta' = \theta$, dG will be:

$$dG = \gamma_{ls}dA - \gamma_{sg}dA + \gamma_{lg}dA\cos\theta \tag{2.7}$$

If G reaches a minimum in the equilibrium state, $dG/dA = 0$. Hence

$$\frac{dG}{dA} = \gamma_{ls} - \gamma_{sg} + \gamma_{lg}\cos\theta = 0 \tag{2.8}$$

This leads to Young's equation:

$$\cos\theta = \frac{\gamma_{ls} - \gamma_{sg}}{\gamma_{lg}} \tag{2.9}$$

Applying the knowledge of Young's equation, the contact angle can be used to study the solid-liquid surface tension and thus the wettability of the surface, and the values of γ_{sg} and γ_{lg}.

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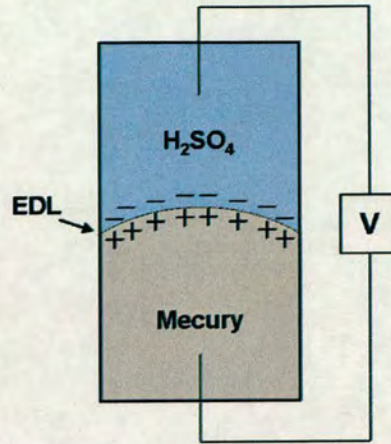
Figure 2.9: *Diagram of the electrocapillary setup in [34].*

2.2.3 Young-Lippmann equation

2.2.3.1 Electrocapillary

EWOD technology is based on the electro-capillary phenomenon discovered by Lippmann in 1875 [34]. Figure 2.9 illustrates the original experiment setup that had an electrolyte solution of H_2SO_4 over a mercury droplet in a container. By applying a potential across the two components, an electric double layer (EDL) builds up at the interface and the shape of meniscus changed [5, 34]. This is due to the reduction of the surface tension of the mercury droplet resulting from the applied potential and the charging at the EDL.

The experiment in [34] shows that the relationship between surface tension and the potential difference over the double layer can be expressed as:

$$d\gamma_{sl}^{eff} = -\rho_{sl}dV \qquad (2.10)$$

where $d\gamma_{sl}^{eff}$ is the reduction of surface tension, ρ_{sl} is the surface charge density at EDL and dV is the potential difference across the EDL.

2.2.4 Electro-Wetting on Dielectrics (EWOD)

More than 100 years after Lippmann's paper was published (1981), the term electrowetting was first introduced to describe an effect proposed for designing a new type of display device [35].

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From a thermodynamic view, the change of wettability at both the liquid/liquid or liquid/solid interface is due to the existence of electrical double layer (EDL). As a further development of electrowetting, EWOD technology uses dielectric layers between liquid and conducting electrodes, acting as EDLs. This allows both non-conductive (polar) liquids and conductive liquids (e.g. water) to be manipulated at a higher speeds and higher voltages without electrolysis taking place. For EWOD, the Lippmann equation (2.10) can be modified to [5]:

$$\gamma(V) = \gamma(0) - \frac{\varepsilon_r \varepsilon_0 V^2}{2t} \tag{2.11}$$

where for an EWOD system, t is the thickness of the dielectric layer [5, 34], V is the voltage across it, ε_r is the dielectric relative permittivity (κ), $\gamma(0)$ is the initial interfacial (solid-liquid in EWOD) surface tension and $\gamma(V)$ is the interfacial (solid-liquid in EWOD) surface tension when voltage V is applied.

Combining the Lippmann equation (2.11) and Young's equation (2.9), the relationship between the surface charge density (the dielectric property), the applied voltage, the solid surface initial hydrophobicity and the shape of the droplet can be obtained. This relationship is known as the Young-Lippmann equation which is given below:

$$\cos\theta(V) - \cos\theta(0) = \frac{\varepsilon_r \varepsilon_0}{2\gamma_{lg}t} V^2 \tag{2.12}$$

2.2.5 Droplet movement by changing contact angle

2.2.5.1 Two-plate EWOD system

Figure 2.10 shows an EWOD device consisting of a droplet sandwiched between two parallel plates. By driving the electrodes on the bottom plate in an EWOD system and grounding the top plate electrode (typically a piece of transparent indium-tin-oxide (ITO) coated glass), voltage can be applied to selected areas, to turn a hydrophobic surface hydrophilic (and vice versa) [5, 36–38]. If the electrode upon which a droplet sits is turned hydrophobic and an adjacent one switched to hydrophilic, the droplet will move to the hydrophilic electrode as shown in fig 2.10.
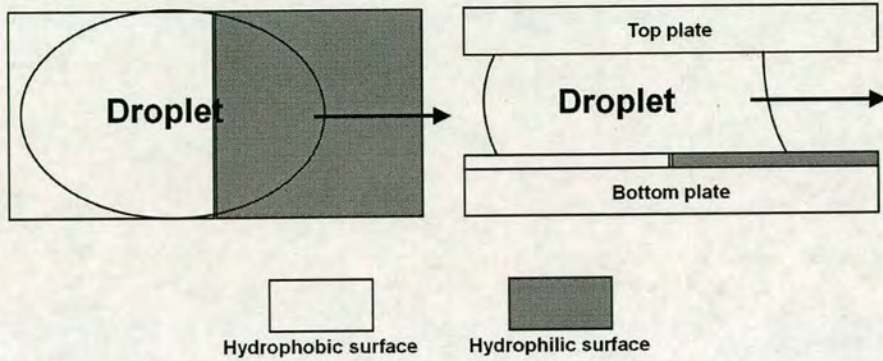
Figure 2.10: *Top view (left) and cross-section (right) of a droplet moving between two adjacent electrodes in a two-plate EWOD system.*
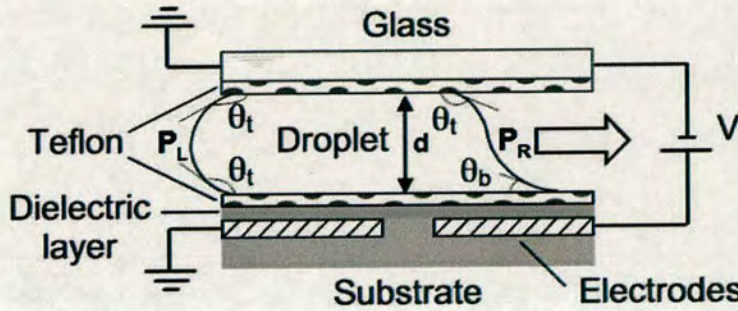
Figure 2.11: *The contact angles and pressure difference for a droplet moving between two adjacent electrodes in two-plate EWOD system. ($\theta_t = \theta(0), \theta_b = \theta(V)$) [40]*

2.2.5.2 Top free EWOD system

In some devices, the ground electrode can be positioned in a coplanar manner on the bottom plate with the driving electrode array and so no top plate is required. However, if the droplet is manipulated in a top free system, evaporation can rapidly affect the droplet size which is typically in the nanolitre to microlitre range.

2.2.5.3 Pressure difference for droplet moving

Manipulation parameters such as speed of droplet movement are determined by the pressure difference over the entire droplet surface. This pressure difference is directly related to the contact angle change on the hydrophilic electrodes discussed in [39]. Figure 2.11 shows the droplet contact angles and pressure difference in a typical two-plate EWOD system.

Using the approach presented in [39], the pressure difference ($P_L - P_R$) exerted by the contact
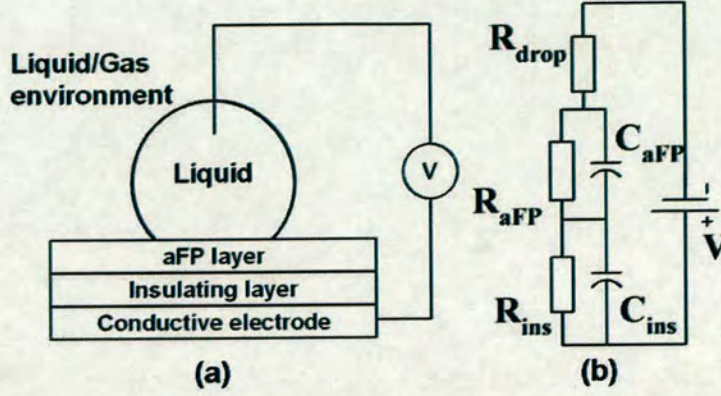
Figure 2.12: *(a) Cross-section of an EWOD structure (b) EWOD RC network model [5].*

angle change can be calculated as:

$$P_L - P_R = \Delta P = \frac{\gamma_{lg}}{d}(\cos\theta(V) - \cos\theta(0)) \tag{2.13}$$

where d is the channel height, the distance between the two parallel plates.

2.2.6   Critical voltage and dielectrics

From equation (2.12) and (2.13), a significant droplet motion (e.g. rapid movement, merging, splitting or shaping) requires a driving voltage greater than a critical value (V_c) to be applied. This causes the required change in the solid/liquid surface tension γ_{ls} and hence the contact angle. Individual structures or device technologies have their own distinct value of γ_{ls} and contact angle change due to the system requirements. In a typical droplet manipulation system, an applied voltage of V_c results in a contact angle change of 40° [41]. Equations (2.11) and (2.12) identify that this voltage is inversely proportional to the capacitance per unit area of the dielectric layers.

The dielectric usually consists of two layers as shown in Fig. 2.12(a). The hydrophobic layer, which is normally an amorphous fluoropolymer (referred to hereafter as the aFP layer), and the underlying dielectric (the insulating dielectric, modeled by R_{ins} and C_{ins} in Fig. 2.12(b)) provides an impervious barrier to the liquid that is manipulated by the EWOD device. Typical hydrophobic layers are Teflon-AF® and CYTOP®, while insulating dielectrics such as silicon dioxide and silicon nitrides are widely used [41, 42].

2.2.7 Contact angle saturation

Figure 2.13(a) shows the contact angle following the theoretical curve calculated from Young-Lippmann equation (2.12). However, the experimental measurements hit a saturation value θ_{sat} around 80° and a number of different explanations for this have been reported [33, 41–45]. Figure 2.13(b) and (c) show the thermodynamic limitation theory, which explains this phenomenon using a thermodynamic approach [42, 43]. Since the applied potential only reduces the solid-liquid surface tension γ_{ls}, the saturation contact angle θ_{sat} results when this surface tension reduces to zero (fig. 2.13(c)). The value of θ_{sat} predicted by the thermodynamic limitation theory for Teflon-AF®/Deionized water(DI water)/air is about 75°.
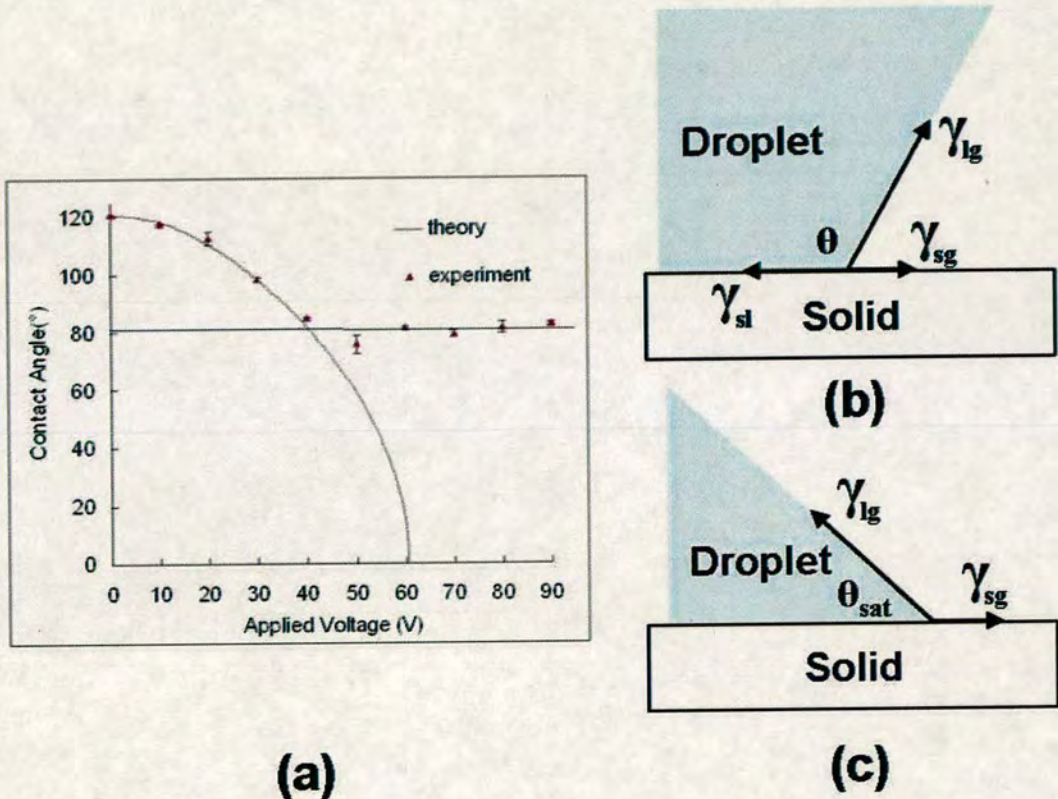
Figure 2.13: *(a) Contact angle as a function of applied voltage. The experimental results have a contact angle saturation phenomenon. (b) The initial state of contact angle in the thermodynamic limitation approach of contact angle saturation theory. (c) The saturation state of contact angle in thermodynamic limitation approach of contact angle saturation theory.*

2.2.8 Other droplet manipulations

Besides droplet movement, changing the surface wettability using EWOD technology can also implement other microfluidic functions using the same electrode array. Figure 2.14 shows droplets splitting and merging using three electrodes.

(a)   **(b)**

☐ Initial hydrophobic Electrode surface   ☐ Hydrophilic electrode surface Generated by EWOD voltage
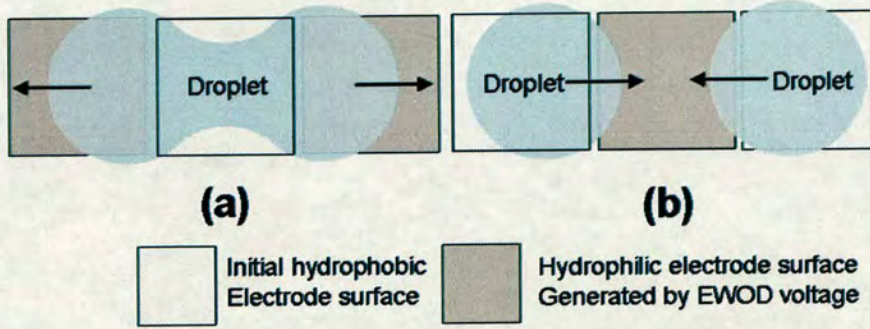
Figure 2.14: *Addressing three electrodes for (a) Splitting one droplet into two. (b) Merging two droplets into one.*

In fig. 2.14(a), the droplet begins to wet electrodes on both sides as they became hydrophilic, while splitting in the centre. Successful droplet splitting relies on a suitable electrode area A to channel height d ratio. This ratio has a threshold value of around 4:1 [20], and is normally set greater than 10:1 to ensure a reliable splitting function.

Fig. 2.14(b) shows that by switching the electrode between two droplets, they will be moved toward each other and merge. Droplet merging seems to be simple. However, mixing two solutions is not so simple due to the low Reynolds number in EWOD systems, which is given by:

$$Re = \frac{\rho v d}{\mu} \tag{2.14}$$

where ρ is the density of the droplet in kgm^{-3}, v is the fluid velocity in ms^{-1}, d is the channel height in the two plate EWOD system in m. Typically Re is less than 100, which is much smaller than the threshold number for turbulent flow. Since mixing of two liquid in laminar flow is very difficult, oscillation of the merged droplet was performed in [46] for successful mixing.

2.3 EWOD developments and applications

EWOD technology has rapidly developed over the last 10 years and is being applied in many fields. The following section details some of this work.

2.3.1 Developments

2.3.1.1 System design and modeling

Figure 2.10 shows the most popular EWOD droplet manipulation design. It is based on a two plate EWOD system, where the bottom plate consists an array of separately addressable driving electrodes coated with an insulating layer and an aFP hydrophobic layer. The top plate only has an aFP layer. Different sizes of bottom electrodes have been employed, typically ranging between 150 and 1500μm [47, 48]. EWOD systems have been designed to facilitate fundamental operations such as transporting, merging, and splitting droplets as well as dispensing liquid from reservoirs [47, 48]. Systems with the channel between two hermetically sealed plates have been demonstrated with various fluids such as water, whole blood, plasma, serum, urine, saliva, sweat, tears etc. These droplets have been manipulated at speeds of up to 250mms^{-1} in different mediums, such as in oil [47–49].

Top free EWOD systems have also been developed for applications which benefit from no top plate being present. This can be implemented by making the driving electrodes and ground electrodes coplanar [50], or by changing the signal driving scheme without pre-specifying the electrode role [51, 52]. Another option includes the insertion of a ground catena/wire in the droplet parallel or coplanar to the bottom electrode [50].

There are a number papers that provide design considerations for different EWOD operations [39, 53, 54]. Walker [39] provides a model of droplet splitting, mathematically interpreting the relationship between the gap height to electrode area ratio on EWOD droplet splitting. Berthier has presented a computer aided design of various EWOD systems and functions, including both two plate and coplanar systems. He simulated and demonstrated, that splitting can only be achieved when a droplet is in two plate system with coplanar architectures [39, 53].

2.3.1.2 Material optimisation

Driving voltage is one of the most critical parameters in EWOD technology. Initially operating at more than 200V, there were difficulties in implementing EWOD devices in many applications [5, 33, 41, 45, 55]. Seyrat first achieved a 20° degree change with 50V DC using a thin (1µm) Teflon-AF® layer [56]. By inserting an insulating layer (100nm SiO_2) and thinning the Teflon-AF® layer down to 50nm, Moon managed to obtain a 40° contact angle change using 25V without the occurrence of dielectric breakdown. This was followed by replacing the SiO_2 with a high-κ Barium-Strontium-Titanate (BST) layer for which only 15V DC was required to drive droplets [41]. By applying surfactant in the droplet, it was demonstrated that a greater contact angle change could be achieved (160° to 60°). This was achieved in a dodecane oil ambient with the application of only 3V [42].

Most of the reported EWOD devices use spin-coated aFP layers such as Teflon-AF® and CYTOP® as an hydrophobic layer [5, 20, 36, 51, 55]. Kim et al. produced a hydrophobic layer with R.F. atmospheric plasma deposition [57]. This can potentially be a viable alternative when spin coating is difficult to perform, such as when processing small dies and samples that are already in packages. Super hydrophobic surfaces have also been investigated and demonstrated [58].

For the electrode material, the use of single-walled carbon nanotube has been reported to enable transparent EWOD devices [59]. The ability to spray deposit and plasma pattern using conventional lithography on glass or flexible polyethylene terephalate (PET) substrates makes it potentially attractive in flexible EWOD device fabrication.

2.3.2 Applications

In recent years the application of EWOD technology has been continuously extended with applications in many different areas such as Lab-on-a-Chip (LOC), optics, displays and micro actuators.

2.3.2.1 Lab-on-a-Chip (LOC)

The first believed reported EWOD based microfluidic LOC platform for clinical diagnostic used chemical dilution [14] and was presented in [60]. It details the ability to perform glucose

concentration measurements on a droplet-based LOC chip. The results compare favourably with conventional methods and the system uses a much smaller sample volume. Based upon [14, 60], an improved system was developed with the ability to analyse human physiological solutions [49]. A very similar, but security related system with the ability to detect nitroaromatic explosives, such as trinitrotoluene (TNT) has been detailed in [15].

Kim's group has demonstrated the application of EWOD technology in proteomics [16, 61–63]. This EWOD electrode array system realised multiplexed sample preparation on a digital microfluidic chip [63]. The first Matrix-Assisted Laser Desorption/Ionisation (MALDI) device with the ability to move droplets containing protein or peptides to the required position on an analysis array was presented in [61]. The ability to perform sample purification, has been presented by [16]. The final device with multiplexed sample preparation and analysis which has a much higher throughput than conventional methods is reported in [62, 63].

EWOD technology can also be used for particle manipulation. Zhao provided a solution to microparticle sampling by using droplet sweeping enabled by EWOD technology [17]. Further particle manipulation functions were achieved by integrating EWOD technology with other methods. Shah et al. integrated optoelectronic tweezers (OET) in the EWOD devices, which enabled particle steering after the samples had been prepared, processed and transported to the OET electrode [64]. The micro particles can also be sorted by integrating electrophoresis (EP) electrodes and this has been demonstrated by the concentration and binary separation EWOD device [65].

For LOC application, different systems and their design have been reviewed in [20].

2.3.2.2 Liquid lens

EWOD devices are also employed in optical systems. One of the most developed is the liquid lens. In photographic, photonics, optical communications, optical sensors, as well as optical pick-up for CD/DVD reading or writing applications, conventional plastic or glass lens requires moving elements for focusing and zooming. The liquid lens technology which enables focusing and zooming without mechanical movement of optical elements works just like the human eye [18]. Figure 2.15 shows the schematic cross section of an electrowetting lens. The incident light focal distance can be altered by changing the meniscus between two immiscible liquids when the EWOD force occurs on the side wall dielectric surface [18]. Both focusing

22
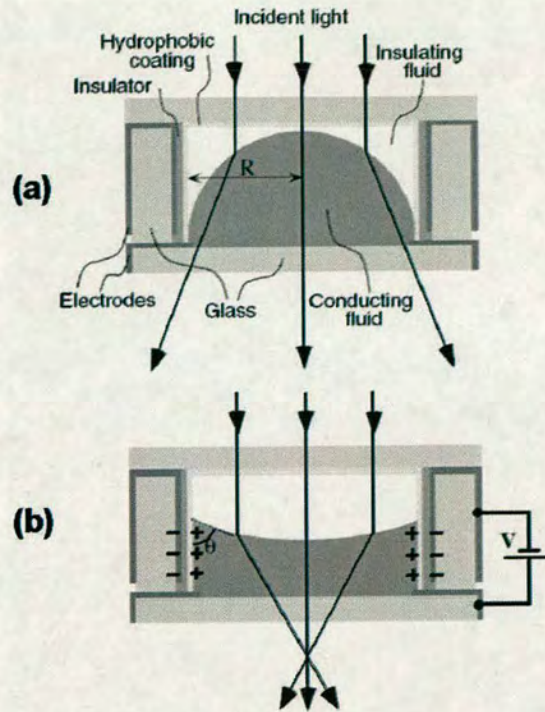
Figure 2.15: *Schematic cross section of an electrowetting liquid lens. (a) With out voltage. (b) With voltage applied on the side wall. [18]*

and zooming have been demonstrated with different designs [18, 37, 66–68]. A performance enhancement for the Blu-ray Disc optical pickup was suggested in [18], with the ability of reading both the 0.1mm and 0.075mm layers after inserting the EWOD liquid lens.

2.3.2.3 Display array and liquid-state FET

Optical EWOD technology is not just used for lenses but also in light emission and display applications. The first electrowetting (precursor of EWOD) device reported in this area was a display [35, 69]. Recently developed EWOD based displays have been demonstrated in reflective [70], transmissive [38] and emissive [19] formats with optical efficiencies superior to many conventional display technologies. Since the switching time is measured in milliseconds, it more than capable of driving video displays [71].

For fabricating an electrowetting display, most of the solid-phase processes can be performed on standard manufacturing equipment. The coloured oil filling process was the only difference. The scalable fabrication together with self-assembled oil dosing, which enables filling of an

~80,000 pixel display array, was demonstrated by Sun [71]. Typical driving voltages can also be reduced from previously reported values of 40 - 50V down to 10 - 15V by the addition of surfactant [71].

Based upon the technologies used in EWOD displays, a liquid-state field-effect transistor using an electrowetting switching mechanism was reported in [72]. This new concept helps the integration of microfluidics and microelectronics by enabling digital processing within the liquid system.

2.3.2.4 Others

There are also other applications such as IC chip cooling using EWOD driven droplets on planar surfaces [73] and electrowetting in microchannels [74]. Using droplets moved by EWOD force to carry micro mechanical devices, a micro conveyor system [75, 76] and micromirror driven by droplets underneath [77] have been reported. Another micro actuator has been demonstrated by Yi et al., showing a nanolitre droplet soft printing mechanism enabled by an EWOD device [78].

2.4   Conclusion

Digital microfluidic systems manipulating liquid in droplet form on a planar surface have developed rapidly in recent years. Among them, electrowetting on dielectric (EWOD) technology employs surface tension force which spans sub-millimeter scale systems. Changing the surface wettability by programming the voltage applied on the electrodes, different microfluidic function can be achieved. The literature reviewed in this chapter has reported a wide range of developments with applications ranging from lab-on-a-chip to optics to microactuators.

Chapter 3
Fabrication and Characterisation of Passive EWOD Electrodes

3.1 Introduction

Before the technologies presented in the next chapters were developed, some basic EWOD devices were fabricated and tested to benchmark the process and evaluate the system. This helped to establish the properties of the electrode dielectric materials, which are related to the system design and operation parameters. Different process conditions and their compatibility and their ability to be integrated with other technologies were of prime concern. This enabled critical system design parameters such as electrode size to be determined, and the system performance characterised.

3.2 Systems for EWOD device observation and characterisation

3.2.1 Contact Angle Measurement System

It can be observed from the Young-Lippmann equation (2.12), that the voltage required for a critical change of the droplet contact angle relates to the dielectric properties of the EWOD device. This critical value change can be used to study different sizes and the shape effect of electrodes and characterise the manipulation of droplets in different EWOD systems. Clearly, the widely used method of measuring contact angle as a function of voltage and the subsequent droplet manipulation on passive EWOD electrodes is a key component of experimental work for this initial evaluation of process architecture and layout design.

For this work, the contact angle (CA) of droplets was measured using the system shown in figure 3.1. A Sony XCD-X710 monochrome IEEE1394 firewire video camera views the side of the droplet with a small downward angle of around 3°, which gives a clear baseline for the measurements [79]. A light source is aligned at the rear of the droplet and directed toward the camera, to create a clear high contrast image. The contact angle is then extracted using the

droplet shape information from captured images. This operation can be performed manually or using specially designed software, and for the measurements reported in this thesis, the software FTA30 was used.
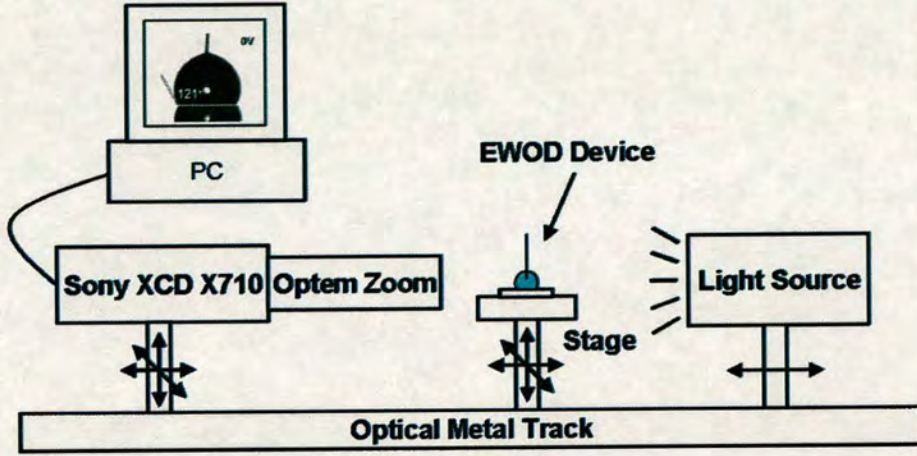
Figure 3.1: *The contact angle measurement system. The camera and sample carrier are both mounted on x-y-z 3-D stages with light source on a 1-D stage, all locate on an optical track*

Figure 3.1 shows a schematic of the contact angle measurement system with figure 3.2 showing enlarged details of the EWOD droplet with and without applied voltage.
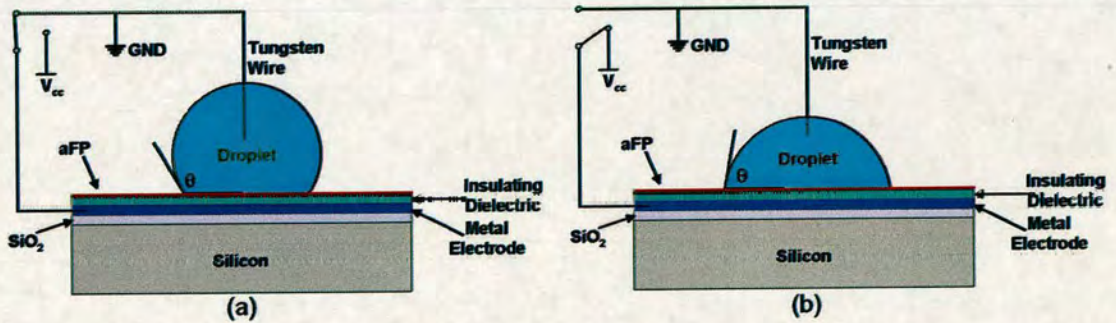
Figure 3.2: *EWOD device with a single metal electrode (plain electrode device) under contact angle vs. voltage test and the EWOD circuit. (a) No voltage applied. (b) Voltage applied.*

The EWOD tests were typically performed on 75mm silicon wafers or centimeter sized chips with thermal SiO_2 as the substrate insulation. The metal electrode material was sputtered and then covered by a selected insulating dielectric layer. The surface was made hydrophobic by spin-coating a layer of amorphous fluoropolymer (aFP) such as Teflon-AF®.

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For applying voltage to the EWOD device shown in figure 3.2, tungsten wire was inserted into the droplet as a top ground electrode (no obvious contact angle change was observed after wire insertion due to its small diameter). The bottom electrode (metal electrode covered by insulating dielectric and amorphous fluoropolymer layers) was first connected to ground potential. Since there was no voltage difference across the dielectric layer, there was no change in surface energy thus the contact angle (fig. 3.2(a)). The bottom electrode Shown in figure 3.2(b) was then switched to a positive DC voltage V_{cc}. As a result, the contact angle changed, the results recorded for later evaluation.

3.2.2 System for droplet manipulation observation

Figure 3.3 shows a microscope system built to observe EWOD droplet movement. The CCD video camera mounted on the microscope for sample observation gives a maximum record speed of 30framessec^{-1}. With an Optem zoom 125 lens, the FOV (field of view) ranges from around 4×6mm to 0.3×0.4mm at a maximum resolution of 1024×768 pixels on the PC screen. It was vertically mounted on a steel stand with its observation angle adjustable for providing both the top view and 3-D view of the samples. The sample was placed under the camera, on a stage with electrical connections to the control units. A personal computer was used to control both the video capture and the droplet manipulation.
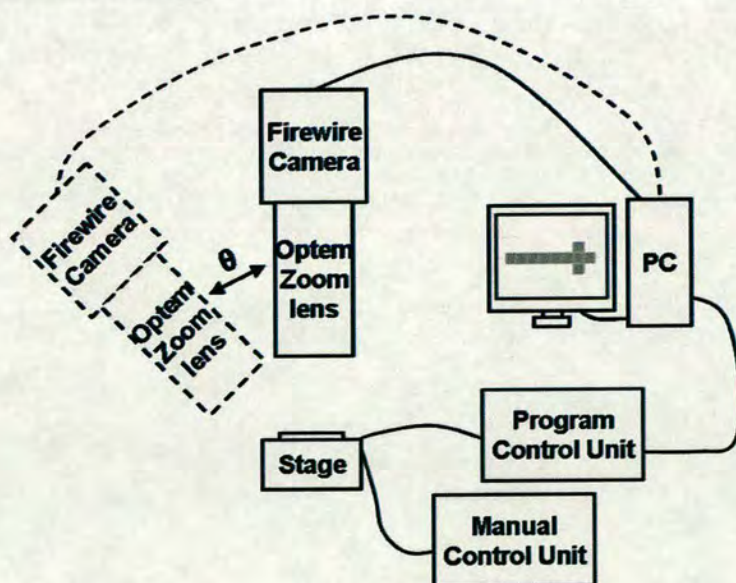
Figure 3.3: *Droplet manipulate observation system, showing a position adjustable camera and the stage and control units for holding and connecting the sample.*

3.3 Material evaluation for EWOD fabrication

3.3.1 Aluminium electrode EWOD devices

Reported EWOD devices have been fabricated with Cr, Au and Pt electrodes. In this work, sputtered aluminium was used, due to its wide spread adoption for CMOS integrated circuit fabrication.

Standard CMOS fabrication processes were performed on a 75mm silicon wafer to create an unpatterned electrode coated with insulating and hydrophobic dielectric layers (figure 3.4).
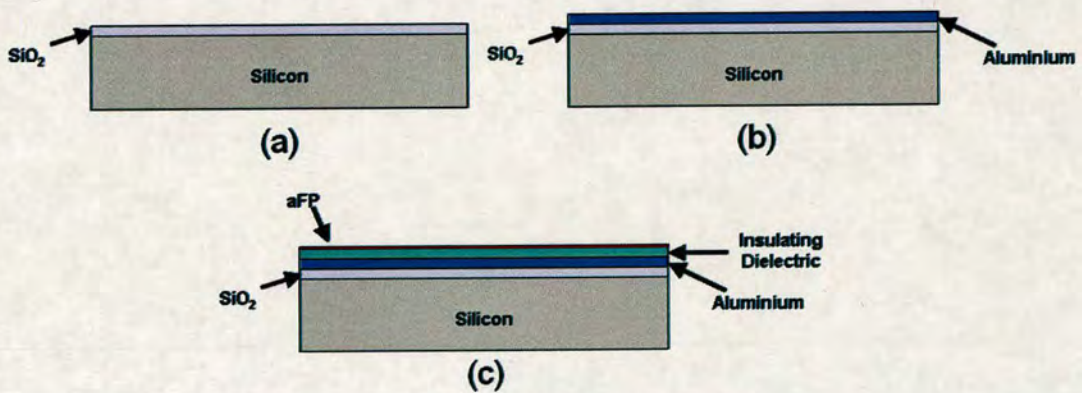
Figure 3.4: *Plain aluminium electrode EWOD device fabrication process flow. (a) Thermal oxidation. (b) Aluminium sputtering. (c) Dielectric deposition.*

The EWOD electrode fabrication starts with a layer of SiO_2 being thermally grown for insulating the substrate from electrical signals. Then a layer of pure aluminium (100nm to 1μm thick) is deposited using a Balzers BAS450PM sputterer (sputtering power 1kW, base pressure 6×10^{-6} mbar, no substrate heating).

After sputtering, aluminium hillocks were observed on the surface. This was due to the mismatch of thermal expansion coefficients between Al and Si or SiO substrate, and occurs during the sputtering of Al and its alloys [80–83]. The heights of the hillocks on as-sputtered Al depend on the film thicknesses. Figure 3.5 shows an AFM (Atomic Force Microscope) image of the hillocks on 1μm thick Al, which were around 50 to 200nm high.

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NanoScope          Tapping AFM
Scan size            10.00 µm
Setpoint              1.030 V
Scan rate             1.001 Hz
Number of samples       256
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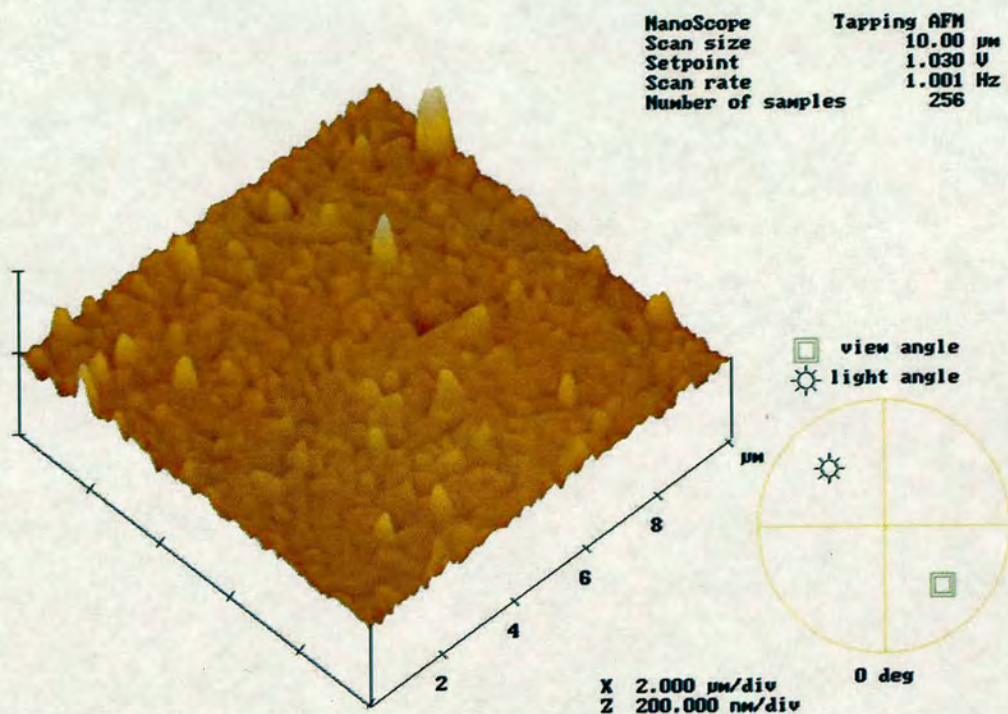
Figure 3.5: *Microscopic images of hillocks on Al surface by AFM (Digital Instruments D5000 AFM).*

3.3.2 Dielectrics and contact angle measurements

3.3.2.1 PECVD dielectrics

After the aluminium metallisation in standard CMOS processes, process temperatures are normally kept below 450°C and thus PECVD (Plasma Enhanced Chemical Vapour Deposition) SiN_x and SiO_2 deposited at 300 to 350°C are used as standard insulation and passivation dielectrics. With aluminium being used as the EWOD electrode material, dielectrics deposited at high temperature as used in other reported EWOD systems [41, 42, 57] were not suitable. PECVD SiN_x deposited at 300°C was used to deposit an insulating dielectric, and the thicknesses range from 0.5µm to 1µm.

Since the PECVD dielectrics are hydrophilic, hydrophobic Teflon-AF® was spin-coated subsequently, with thickness controlled by changing the solution concentration and spin speed. FC75-0.6% Teflon was used to coat the sample spinning at 1000rpm, providing a 40nm to

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50nm layer. This gave the DI water droplet an initial contact angle of 122°.

Switching the surface from hydrophobic to hydrophilic by applying a voltage sometimes caused electrolysis of the droplet. The water permeated the dielectric layers during the experiment, resulting in the voltage being directly applied to the liquid. Large current flow resulted in dots on the aluminium electrodes and dielectric layers due to heating, causing the device to malfunction, as shown in fig. 3.6).
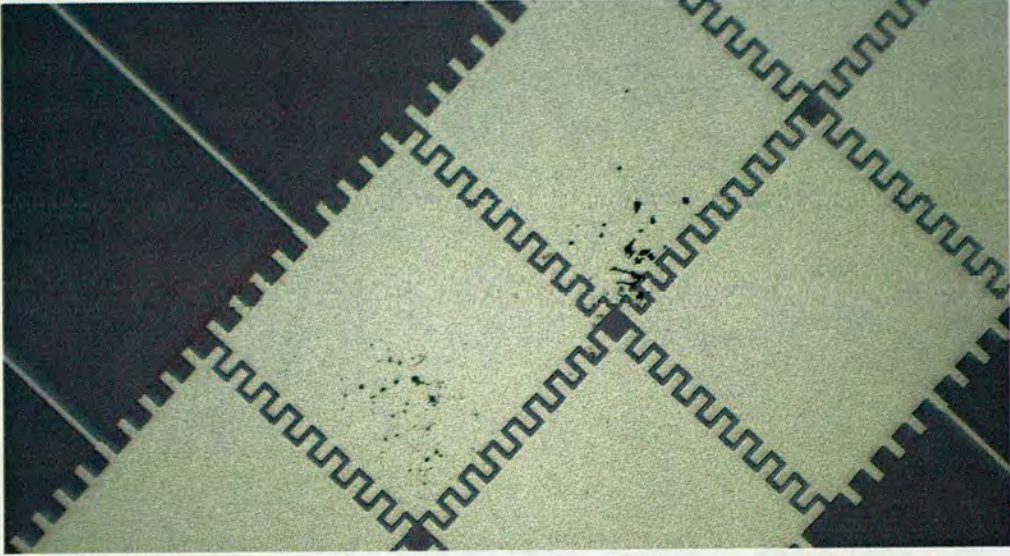
Figure 3.6: *The results of electrolysis failure on a porous dielectric layer that occurred during EWOD operation. The unwanted current flow causes burn marks on the dielectric layers and electrodes (black dots on white coloured electrodes).*

This shows that 50nm Teflon-AF® failed to cover the defects on the PECVD dielectrics which tend to have higher pinhole densities compared to LPCVD (low pressure chemical vapor deposition) [84, 85]. With large aluminium electrodes (millimeter scale in EWOD), more defects e.g. dielectric cracks could be generated during the 300°C PECVD deposition as the aluminium hillock size and density increases during the thermal processes. Similar phenomena can potentially cause short circuits in multilevel metallisation [80–83]. To solve this problem by lowering the possibility of electrolysis, a thicker layer of Teflon-AF® (150nm) could be used. To fully model the device, the Young-Lippmann equation (2.12) must be modified to include both the aFP and insulating dielectric layers. When there is a layer comprising two different dielectrics, the total capacitance can be calculated as two capacitors in series using $C = \frac{C_1 C_2}{C_2 + C_1}$, where C_1 and C_2 represent the capacitances due to the two dielectric layers, and equation (2.12) can be

re-written:

$$\cos\theta(V) - \cos\theta(0) = \frac{1}{2\gamma_{lg}}\left(\frac{\varepsilon_{r1}\varepsilon_{r2}\varepsilon_0}{t_1\varepsilon_{r2} + t_2\varepsilon_{r1}}\right)V^2 \tag{3.1}$$

where ε_{r1} and t_1 are the dielectric constant and thickness of the aFP material, ε_{r2} and t_2 are those of the insulating material. For 150nm Teflon-AF® (ε_{r1}=1.93) and 0.5μm PECVD SiN$_x$ (ε_{r2}=6), the calculated critical driving voltage (causing contact angle change from 121° to 81°) in around 42 V.

Equation (3.1) and experimental measurements of contact angle as a function of applied voltage for a sample with 0.5μm PECVD SiN$_x$ and 150nm Teflon-AF® are shown in figure 3.7, confirming a critical voltage between 40 and 50V which matches the theory.
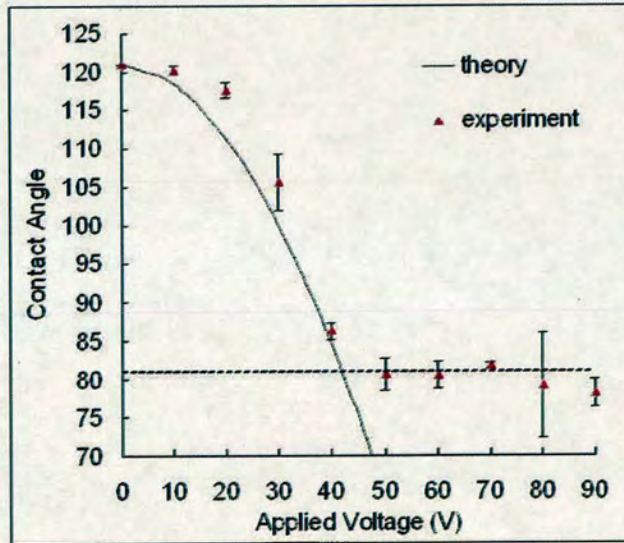
Figure 3.7: *Contact angle vs. voltage of a 5μL droplet on 150nm Teflon-AF® + 0.5μm PECVD SiN$_x$. Theoretical curve is given by the Young-Lippmann's equation (2.12).*

3.3.2.2 Parylene-C

Parylene-C (dielectric constant 3.1) is an inert, pinhole-free, hydrophobic, biocompatible polymer coating material, which is used for waterproofing and as a chemical resisting layer in both MEMS and bioMEMS applications[1]. Since it is vapour deposited, Parylene-C forms a confor-

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[1]http://www.vp-scientific.com/parylene_properties.htm

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mal and uniform thin dielectric layer at room temperature. Hence it can provide an alternative to PECVD dielectrics as the EWOD insulating dielectric layers.

Parylene-C product is sold in the form of dimer. During the vapour deposition, certain amount of dimer is vapourised, and then turned into monomer during pyrolysis at high temperature. The monomer is then transfered into the ambient temperature chamber, and a polymer formed which is deposited on all surfaces [86]. The thickness of the deposited layer, which in this work has been typically being 500nm and 1μm, can be controlled by weighing the dimer before vapourisation. After spin-coating with 50nm Teflon-AF®, contact angle measurements as a function of voltage were performed without any electrolysis failure.

As the film thicknesses of the samples were between 0.5 and 1μm, critical voltages were measured to be in the range between 46V to 62V. The low value of 27V was achieved on a sample with 120nm Parylene-C. However, the low dielectric strength of Parylene-C and hillocks on the aluminium surface reduced the yield by around 50%.

3.4 Passive single metal layer EWOD device

3.4.1 Device layout

After the contact angle characterisation on plain aluminium electrodes, EWOD electrode array devices were designed for droplet manipulation tests. Single metal layer EWOD electrode array devices were fabricated using aluminium as both the electrode and interconnect material. The electrode arrays were all based on a microscope slide chips (around 50 × 25mm). Figure 3.8 shows the layout of two EWOD chips (the dot-dashed box outlines a single chip) on a 75mm wafer. Different electrode arrays were located in the chip centre, and these were connected to the bond pads via the interconnect. The bond pads were 2 × 2mm with a pitch size of around 2.54mm, to enable electrical connection to be made with a 3M™ IC test clip connector.

3.4.2 Device fabrication and packaging

For fabricating passive EWOD electrodes, a layer of SiO_2 was thermally grown on silicon substrates followed by aluminium sputtering. The metal was then patterned by conventional optical lithography followed by $SiCl_4$ plasma etching, as shown in figure 3.9. Layers of 0.5μm to 1μm Parylene-C and 50nm Teflon-AF® were deposited to ensure a pin-hole free dielectric
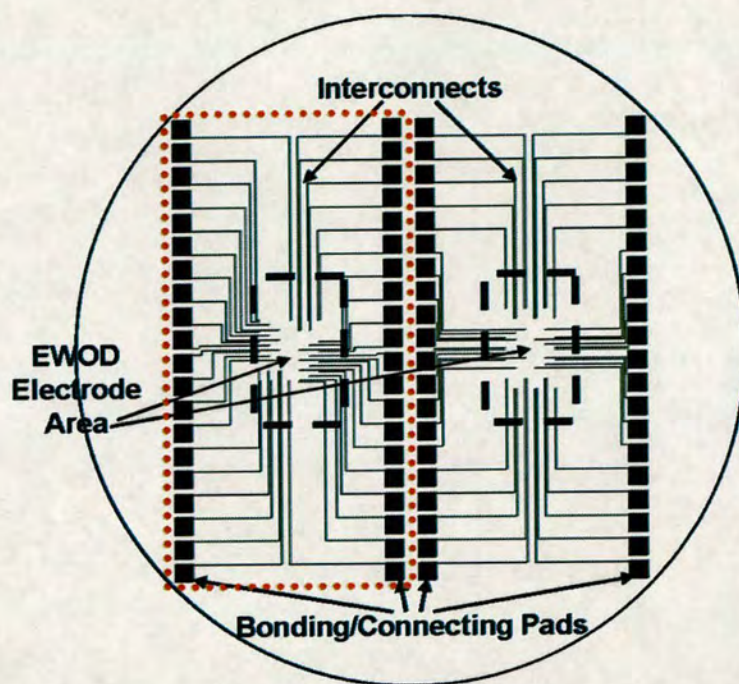
Figure 3.8: *Layout of microscope slide scale size EWOD chips on a 3" wafer. The dot-dashed line outlines a single chip. The EWOD electrode arrays electrically connected to the bond pads via interconnects, were positioned.*

insulating layers and a hydrophobic surface for robust EWOD operation. For performing two-plate EWOD operation, a top electrode plate (glass slide coated with indium tin oxide (ITO) and 50nm Teflon-AF®) was assembled to create the droplet gap. The height of the droplet is defined by the thickness of plastic shims ranging from 53μm to 1000μm. Other spacing materials such as dicing tapes (80μm) were also used when hermetic sealing was required.

3.4.3 Electrode array design

Single electrode arrays were designed to achieve basic EWOD droplet manipulation functions, such as droplet movement, merging and splitting. With reference to the electrode configurations required for these functions, cross-shape single column arrays and double columns arrays with electrode sizes range from 350μm to 1.4mm were designed and fabricated as shown in figure 3.10.

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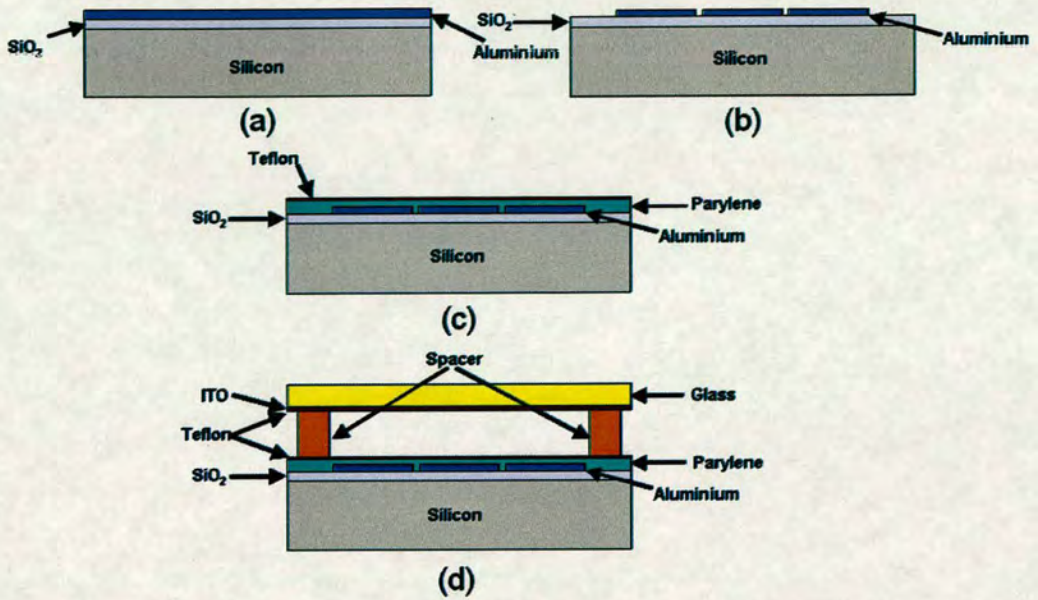
Figure 3.9: *Process flow of single metal layer EWOD device fabrication. (a) Thermal oxidation of silicon and aluminium sputtering. (b) Aluminium electrode patterning. (c) Dielectric layer deposition. (d) Assembly with a top conductive plate.*

3.4.3.1 Electrodes designed for droplet moving and merging

Transporting liquid simply involves moving a droplet from one electrode to the next. Theoretically, if the gaps between adjacent electrodes are small enough for the droplet to overlap, this motion will occur when the critical/driving voltage causes a sufficiently large wettability gradient. However, if the surface is not perfectly smooth, or there are some impurities, the motion may be impeded.

For this reason, figure 3.10 shows in both single column (cross-shape) and double column designs (2 × 4 array). For both designs there were square and interdigitated (also called microdents crenelated) electrodes [53]. Both designs exhibited successful motion, while the later design had a noticeably higher yield. By switching the electrode in between two droplets, which are also positioned on electrodes on either side of the electrode to be switched, merging of droplets can be achieved (figure 3.11(a)).
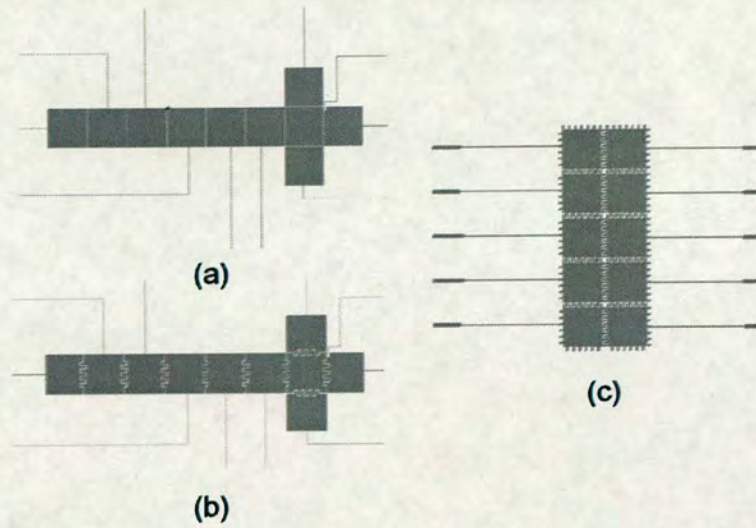
Figure 3.10: *Single metal layer EWOD electrode designs for basic droplet manipulation. (a)Cross shape single metal layer EWOD device, electrode sizes 1.4mm or 1mm, gap size 25μm (10 electrodes). (b)Cross shape single metal layer EWOD device, electrode sizes 1.4mm or 1mm, gap size 25μm, with interdigitated electrode shape (10 electrodes). (c) Two-row single metal layer EWOD device, electrode sizes from 1.25mm to 350μmm, gap size 25μm, with electrodes interdigitated.*

3.4.3.2 Droplet splitting

For splitting a big droplet into two droplets, both electrodes on either sides of the electrode where a big droplet is located need to be switched on simultaneously. Then hydrophilic forces will stretch the droplet apart while hydrophobic forces pinch in the centre to break it [48].

To create sufficient stretching and pinching force magnitude against the cohesive force in the droplet, the scales of the splitting electrodes and droplet channel heights (gap between EWOD top and bottom plates) need to be carefully considered. The ratio of channel height δ and electrode dimension e, should not exceed around 1:10 [39, 48, 53] when splitting a DI water droplet in atmosphere in Teflon-AF® surface EWOD two-plate devices [48].

By applying voltages on the 1250μm electrodes, a droplet was successfully split in a 140μm gap device (figure 3.11(b)).

35
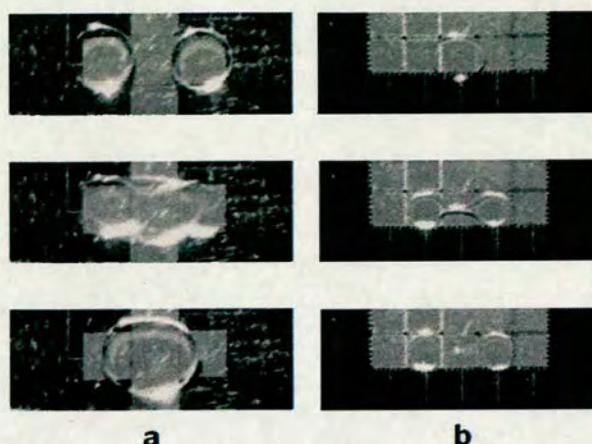
Figure 3.11: *Sequences showing (a) droplet merging and (b) splitting.*

3.4.3.3 Droplet dispensing

On-chip dispensing electrodes were also designed, for creating a smaller droplet with a defined volume (in this case 130nL) from a droplet reservoir (in this case 1μL). Figure 3.12 shows the electrodes designed for droplet dispensing. Two large "V" shape electrodes (No. 4 and 0) are the reservoir for holding large droplets. The electrodes with 1mm width and different lengths (1mm or 3mm) are located between the reservoir electrodes and can be used for delivering and splitting droplets (No. 1 to 3 and 5 to 6).

The dispense regime of a single droplet consists of three steps [53]. For example, a droplet being dispensed onto electrode No.3 from the reservoir No.0 would involves:

1. Apply voltage to electrodes No. 1 to 3, extruding the liquid from the reservoir until it reaches electrode No. 3.

2. Switch off electrodes No. 2 and then 1, and then switch on the reservoir electrode to back pumping the extruded liquid while creating a droplet on electrode No. 3.

3. Switch off all the electrodes.

An example of this is illustrated in figure 3.13. Following the first three steps, an 120nL droplet is successfully dispensed (fig. 3.13(d)) on the designed electrode array. The volume of dispensed droplets is determined by the dispense electrode sizes and the channel heights. The surface tensions and the lengths of cutting electrodes also have minor impact on the dispensed
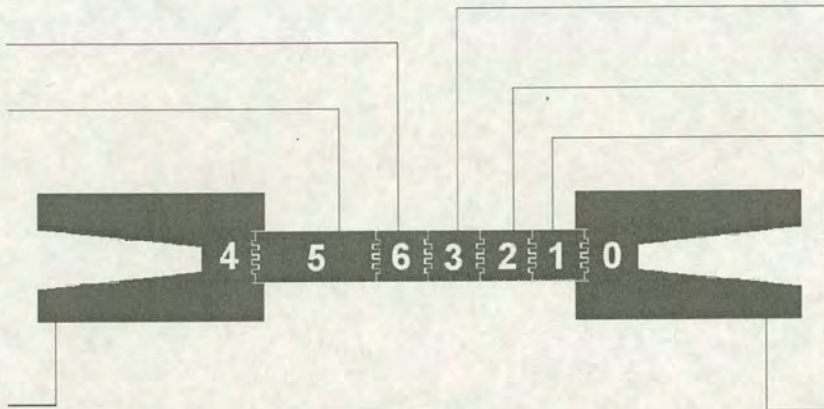
Figure 3.12: *Single metal layer EWOD device with reservoir (electrode number 4 and 0) struc-
ture. Electrodes number 1, 2, 3, 6 have sizes of 1mm × 1mm, number 5 has a size
of 1mm × 3mm, gap size 25μm. Electrodes are all interdigitated.*

droplet volumes [53].

3.4.3.4 Liquid input

Obviously, loading liquid samples from the outside world onto EWOD electrode arrays re-
quires an interface. For the passive EWOD electrode devices discussed in this chapter, this was
initially done by dispensing droplets directly onto the arrays using micropipettes or syringes
before assembling the top electrode plate [36, 61].

While in hermetically sealed systems and systems requires automatic liquid inputs from other
devices, this method is not appropriate. On the other hand, using pipettes and syringes dispens-
ing nanolitre droplets onto hydrophobic surface is practically difficult and potentially possible
to cause surface scratching. Other droplet input solutions for digital microfluidic systems have
been suggested and demonstrated in [22], showing different designs of liquid injectors. In
these designs, a combination of hydrostatic, interfacial and dielectrophoretic forces were used
to control injection of metered aliquots of reagents and samples into the droplet processor.

In EWOD, there is an alternative. A hole was drilled on the top plate, then a droplet was
pumped (using pressure) into the EWOD channel while switching the input area surface into

Reservoir droplet

(a)

(b)

Pinching and Splitting

(c)

Dispensed Droplet

(d)
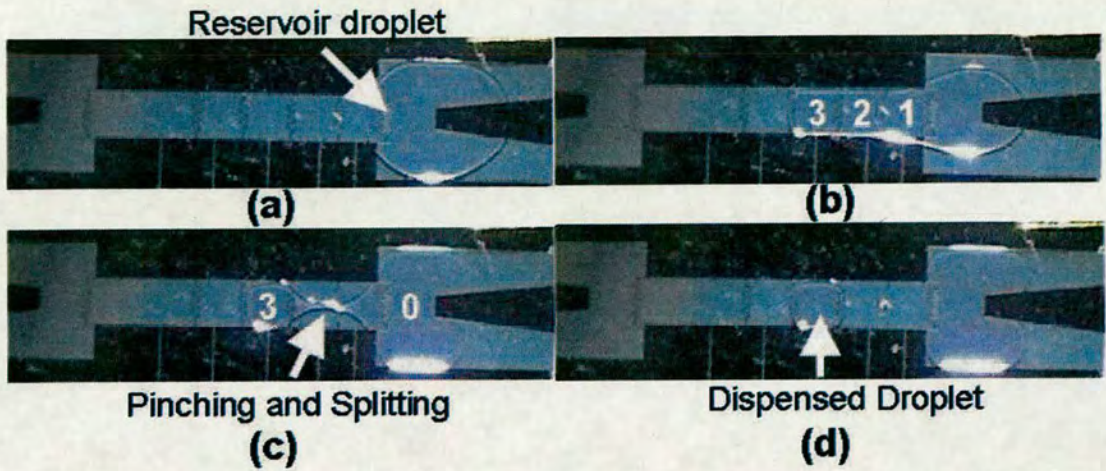
Figure 3.13: *Droplet dispensed from (a) the reservoir, in three steps: (b) Liquid extrusion by switching on the dispensing and cutting electrodes No. 1, 2 and 3. (c) Back pumping and creating the droplet by switching off electrodes No. 1 and 2, and then switching on the reservoir electrode. (d) A droplet was dispensed.*

hydrophilic mode [49]. The liquid in the EWOD channel can then be manipulated to generate droplets with required volume by using the droplet dispensing method discussed previously. Figure 3.14 shows an example of this method be implemented.

Input hole

Syringe Needle
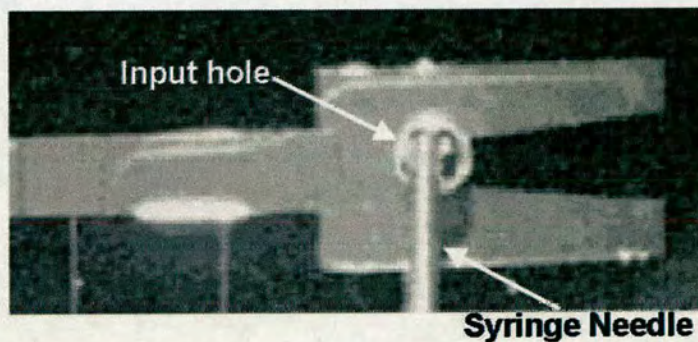
Figure 3.14: *Liquid input through a 1mm diameter hole on the EWOD top electrode plate.*

3.5 EWOD control system

3.5.1 Manual control unit

The EWOD results presented so far were controlled by the manual switch unit shown in figure 3.15. Negative (ground) or positive voltages can be manually switched to the electrodes of passive EWOD samples.

This unit includes a high voltage DC power supply unit (range from 0 to 100V), a 10-way electrical connection switch box and a 40-way electrical connection metal jig, shown in figure 3.15. The high voltage on and off signals up to 100V applied to up to 10 electrodes were controlled by 10 manual switches.
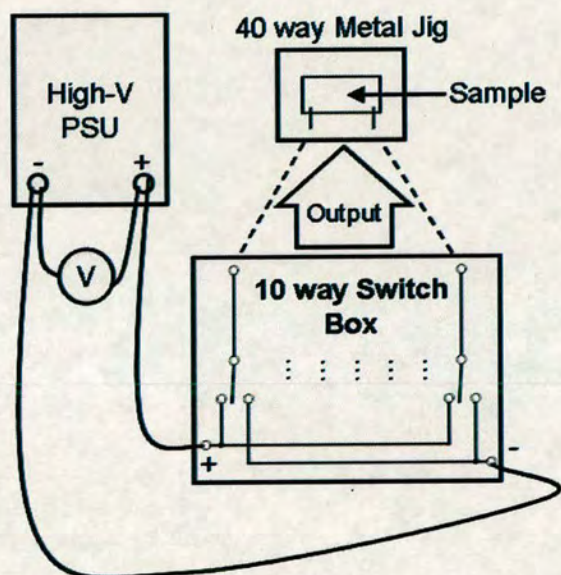
Figure 3.15: *Schematic view of the manual switch unit for manipulating droplets on EWOD electrode array.*

3.5.2 Program control unit

3.5.2.1 System Setup

For system automation and repeatable droplet manipulation, a computer based control system for up to 20 electrodes EWOD device has been developed.

Figure 3.16 shows the basic system. To replace the 10-way switchbox used in the manual con-
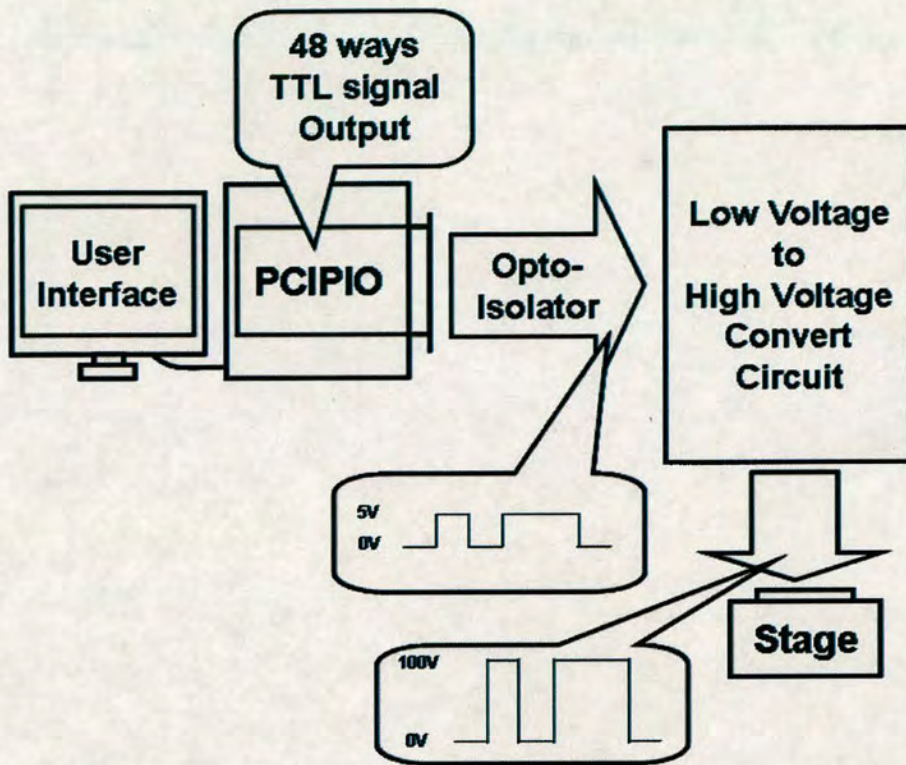
Figure 3.16: *System diagram of a EWOD system program control unit.*

trol unit, a multichannel digital input/output (I/O) device was chosen for generating individual control signals for each electrodes in the passive EWOD device. A Bluechip Tech. Ltd.[2] "PCI-PIO" card was selected, providing maximum 48 ways TTL signal output (in the first system, 20 of them were used) from a personal computer.

Since the TTL logic voltages are too low to drive the EWOD electrodes, a TTL to high-voltage conversion system has been designed and tested. The circuit is capable of converting TTL outputs into 15V to 100V driving signals. The PCIPIO digital I/O card and the personal computer were protected from the potential high voltage exposure by opto-isolators.

3.5.2.2 Control program and user interface

The control program translates user control requests into the digital output voltages on the PCIPIO card, which were then converted to required driving voltage (0 to 100V). These were electrically connected to the EWOD electrodes to execute droplet manipulation (fig. 3.15).

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[2]http://www.bluechiptechnology.co.uk/

For linking the user interface with PCIPIO card control, a C++ computer program was used. The programming environment was Microsoft® Visual C++ Express Edition software [3].

The basic objectives of these programs are:

- To enable the users choose to start, stop and change the parameter settings of repeatable automatic EWOD manipulations.

- To enable real-time control ("point and go" on EWOD electrode arrays), which is similar to manual switching but repeatable sequences (particularly timing).

The program organisation is shown in figure 3.17. The user interface is based on text menus in the command console in Windows for simplicity and graphical user interface (GUI) will be developed in the future. Examples of different programs are attached in the **Appendix B**, including an automatic EWOD demonstration program and a "point and go" multi-droplets manipulation program.
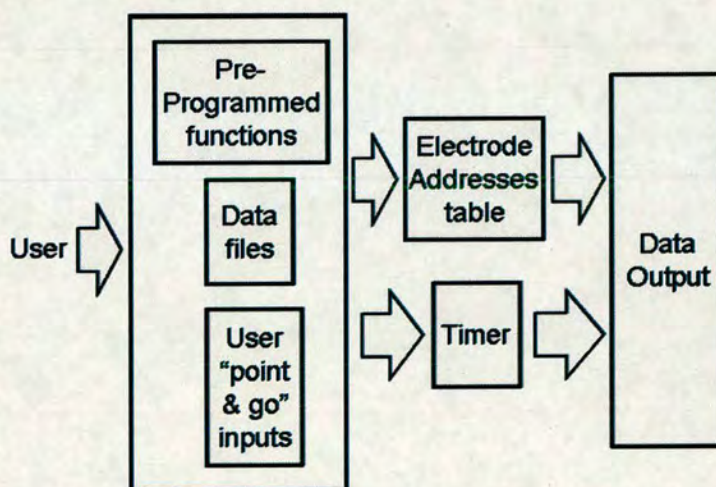
Figure 3.17: *Control programs.*

3.5.2.3 Switching time and pulse signal generation

Switching time is a key parameter in the EWOD control programs. During the droplet movement, the voltage should not be switched off until the movement finishes. The fastest droplet

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[3]the Microsoft® Platform SDK is also required, as some of the function libraries used by the PCIPIO card driving are included

movement speed observed under DC driving voltage is around 30mms^{-1} [48]. During the program testing experiments, it was noted that, on electrodes sized around 1 x 1mm, transporting a droplet to a second electrode took around 0.5 to 1 second, while droplet splitting could take up to 5 seconds.

According to reported results [48, 51], AC driving voltage has been used in EWOD systems for reducing hysteresis and increasing the driving speed. Generating AC pulse signals would potentially benefit the EWOD manipulation. From 0 to 25kHz AC driving signals were used in the experiments, reported by Cho et. al [48]. Hence the timing function used in the program need to be accurate to sub-milliseconds.

Using a time function which is able to provide delays range from nanosecond to second scales, the high reliability of the system was verified by an overnight test using pulse signals.

3.6 Summary

In this chapter, the fabrication and characterisation of passive aluminium EWOD electrodes have been presented. Insulating dielectric materials such as PECVD SiN$_x$, Parylene-C combined with hydrophobic amorphous fluoropolymer Teflon-AF® were evaluated. Contact angle vs. voltage experiments on plain electrode (testing droplet on a single electrode) showed sufficient contact angle change (from 121° to 81°) with 40 to 60V DC voltage applied. Based on these critical voltages, droplet manipulations such as transportation, merging, splitting and dispensing were demonstrated. During the experiments, some device malfunctions due to liquid penetrating the porous insulating layer on PECVD dielectric samples were spotted. As a result, the high yield Parylene-C samples of dielectrics were implemented.

In addition, measurement systems and the system control units for the characterisation and droplet manipulation have been developed.

Chapter 4
Low Voltage EWOD using Anodic Tantalum Pentoxide

4.1 Introduction

In the work presented in Chapter 3, passive EWOD devices using aluminium electrodes and interconnects were fabricated. One of the perceived disadvantages of these devices is the relatively high voltage (40 to 100V) required to robustly drive droplet movement. As most commercial operational amplifier circuits operate with voltages of 15V or less and digital logic with voltages significantly lower, there has been considerable interest in reducing the voltage [41]. This is especially an issue if EWOD is to be integrated with other technologies e.g. standard CMOS. For example the first prototype of the CMOS EWOD integrated device presented in Chapter 6 used a 100V foundry technology.

Hence, to take advantage of the opportunities available with lower voltage devices there is a requirement to significantly lower the drive voltage. This chapter reports on a robust combination of insulation dielectric and surface treatment that enables the operating voltage to be reduced.

4.2 Low voltage EWOD development

The critical voltage V_c for driving EWOD devices was introduced in Chapter 2. Historically, the driving voltages in most of the initially reported systems were high (200V) [5, 33, 41, 45, 55] due to the thickness and low permittivity of the dielectric layers that were used.

Typical EWOD devices consist of two dielectric layers on the bottom plate, as shown in figure 2.12. From the Young-Lippmann equation (2.12) it can be deduced that V_c can be reduces simply by decreasing the thicknesses of both dielectric layers. However, it is important to ensure that this thinning does not result in dielectric breakdown at voltages that are too low to enable successful droplet movement [41].

Another approach is to employ high dielectric constant (κ or ε_r) materials, which also have high breakdown strength. These enable a high capacitance to be obtained using a thicker dielectric layer, thus reducing the critical voltage while maintaining a sufficiently high breakdown voltage. Moon et al. have reported a driving voltage of 14V by coating 20nm Teflon-AF® onto a 70nm BST (Barium Strontium Titanate) insulating layer ($\kappa = 180$). for this device, the contact angle (CA) of a deionised (DI) water droplet in air changed from 120° to 80° [41]. Similarly Kim et al. used 100nm of RF reactive sputtered Ta_2O_5 and BZN (Bismuth Zinc Niobate) with 40nm Teflon-AF® or a hydrophobic RF atmospheric plasma treatment to achieve rapid droplet movement at 23V for Ta_2O_5 and 14V for BZN [57].

A dodecane oil ambient phase and mixing SDS surfactant in the droplet has been reported to lower V_c to 3V [42], demonstrating a contact angle change of over 100° by reducing the three-phase surface tensions combined with scaling down the dielectric thicknesses. This result indicates that electrowetting behavior is achievable with a very thin dielectric in the thickness range of tens of nanometers.

4.2.1 Anodic Ta_2O_5 as an insulating dielectric

Anodic Ta_2O_5 is very well established in the electronics industry, being widely used as the dielectric in electrolytic capacitors. It produces a dense, smooth, high κ and homogeneous oxide of well-defined and reproducible thickness at room temperature [87–89]. When formed in an electrolyte solution or gel, this layer can be produced pin-hole free making it very attractive for EWOD applications where any porosity in the dielectric layers causes electrolysis breakdown failures (e.g. BST layer reported in [90]).

Compared to the BST and BZN films mentioned previously, the permittivity of Ta_2O_5 is relatively low and typically between 8 and 25 [89]. However, the BST film suffers from time-dependent breakdown (TDBD) [41, 91] and has been reported to have fabrication difficulties [90]. In addition, BZN requires a high temperature anneal to obtain a high value of κ, and exhibits a large surface roughness [92] which causes contact angle hysteresis [93]. Unfortunately the RF sputtering method also tends to produce a porous layer requiring a thick aFP barrier.

Since the proposed high κ materials for lowering EWOD driving voltages have some non-optimum effects, it is necessary to determine the performance gain when increasingly high

values of κ are employed, and is illustrated in the following section.

4.3 Ultra thin aFP layer on high-κ dielectrics

4.3.1 aFP thicknesses and critical voltages

Figure 2.12 is a widely accepted model of the EWOD device, consisting of a capacitor and resistor network [5] which can be used to describe the relationship between aFP layers and insulating layers in the system. In most of the current low voltage EWOD systems, about 20 nm to 50nm thick low κ aFP films used with an insulating layer which is typically thinner than 100nm. The insulating layer typically has a κ greater than 3, helping to achieve a V_c around 20V [41, 57].

Equation (3.1) indicates that the total capacitance of the two capacitor in series is a function of the thickness of the aFP and insulating dielectric layers. For example an insulating dielectric layer (BST) of 22.8mFm^{-2} (70nm, κ=180) with a hydrophobic layer (Teflon-AF) of 0.84mFm^{-2} (20nm, κ=1.9) results in a device capacitance of just 0.81mFm^{-2} [41]. As the capacitance of the aFP layer is typically 30 times lower than BST, reducing its dielectric thickness will have the most dominant effect on lowering EWOD driving voltages.

Fig. 4.1 and 4.2 presents the driving voltage required for a 40° CA change (121° to 81°) as a function of (a) Teflon-AF® thicknesses and (b) the $κ/ε_r$ value of a thin (100nm) insulation layer. Equation (3.1) can be re-written as:

$$\cos 81° - \cos 121° = \frac{1}{2\gamma_{lg}}\left(\frac{1.9 \cdot κ \cdot ε_0}{t_{teflon} \cdot κ + 1 \times 10^{-7}m \cdot 1.9}\right)V_c^2 \qquad (4.1)$$

Equation 4.1 is plotted in fig. 4.1 and shows an almost linear relationship with the driving voltage dropping as the Teflon-AF® thickness reduces. Fig. 4.2 shows V_c reducing asymptotically with increasing insulating layer permittivity (κ). It is clear there is little reduction of V_c for 100nm thick insulating layers with a permittivity (κ) 100 no matter what the Teflon-AF® thickness is.

From figure 4.2 it can be observed that by thinning down the Teflon-AF® layer to below 20nm, the driving voltage can be reduced to less than 15V for an insulating layer with κ as low as 5. However, if the Teflon-AF® layer is thicker than 50nm, a κ as high as 1000 cannot meet this
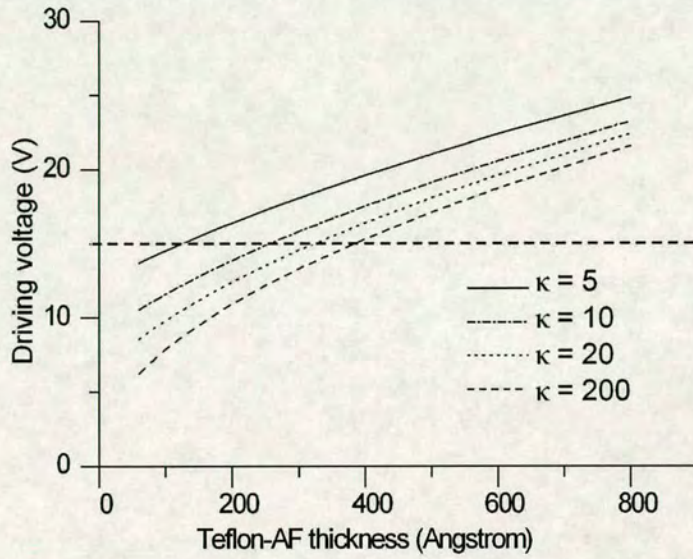
Figure 4.1: *Relationship between driving voltage and dielectric property calculated from (4.1) (horizontal dashed line indicates 15V): Driving voltage vs. the thicknesses of Teflon-AF® over 100nm insulating layers for a range of dielectric constants.*
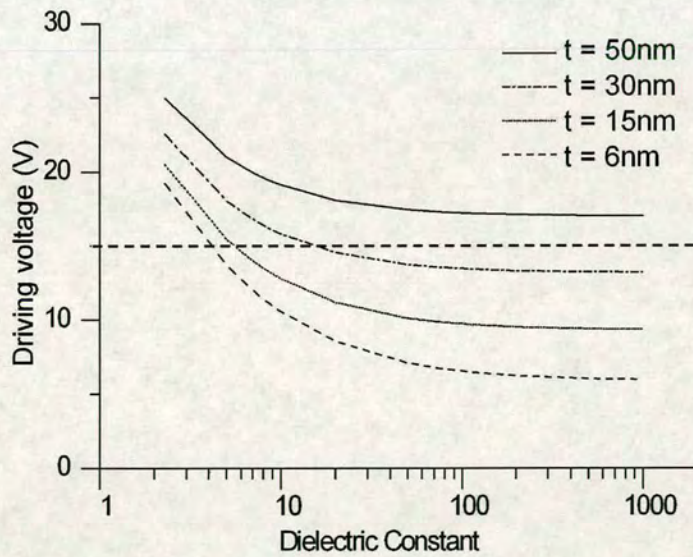
Figure 4.2: *Relationship between driving voltage and dielectric property calculated from (4.1) (horizontal dashed line indicates 15V): Driving voltage vs. the dielectric constant (κ) of 100nm insulating layers, for different Teflon-AF® thicknesses t.*

goal.

4.3.2 Insulating dielectric for ultra thin aFP

If a very thin aFP hydrophobic layer is to be used, it is evident that it will be more sensitive to the quality of the underlying insulation layer, specifically with regard to roughness and pinholes. Hence, if the insulating film is porous (or has pin-holes) then the barrier to the liquid will be breached causing electrolysis failure with the liquid seeping through the film [90]. In addition rough films also tend to exhibit a significant contact angle hysteresis during operation [93]. Rough and porous dielectric films tend to be produced by both PECVD (Plasma Enhanced Chemical Vapour Deposition) and reactive sputtering. Denser dielectric material with higher uniformity and lower roughness can be formed by processes such as LPCVD (Low Pressure Chemical Vapor Deposition) and thermal oxidation. However, the higher growth/deposition temperature required (up to 900°C) is an issue if interconnect metals used in standard CMOS (e.g. aluminium and copper) have been employed. If metals such as these are present, then the maximum process temperature that can be used is 450°C.

As mentioned previously, anodic Ta_2O_5 is a high κ pinhole free insulating dielectric material found at room temperature, which is suitable for integration with CMOS. Figure 4.3 shows the method of growing anodic Ta_2O_5 using a constant current anodisation at room temperature. The electrolyte used was citric acid mixed in a gel formed with DI water, digol glycol and sodium carboxy-methyl-celloluse. To fabricate electrodes with a Ta_2O_5 dielectric, tantalum is first sputtered and patterned using standard lithography on silicon wafers that had been thermally oxidised. The electrolyte gel preparation was carried out in a cleanroom to minimal any particulate based film defects. The anodisation process then followed and was performed in a standard laboratory environment at room temperature, and the low electrolysis failure rate achieved during EWOD operation (<1%) indicates that the resulting particulate defects are low. The equation governing anodic oxidation is given by [87, 88]:

$$J = D exp \frac{BV}{h} \qquad (4.2)$$

where J is the current density, V is the potential across the oxide film of thickness h, and D and B are constants. The current density to grow the Ta_2O_5 is normally fixed between 1 and $10mAcm^{-2}$ which sets the growth rate of the oxide [88]. For a given temperature the resulting
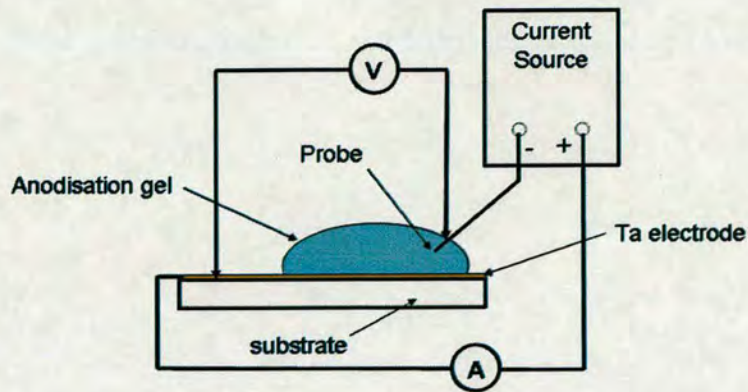
Figure 4.3: *The equipment setup for tantalum anodisation.*

film thickness is defined by the applied voltage, which for this work was in the range of 1.6 to 1.9 nmV^{-1} [87].

4.4   Sample fabrication for material evaluation

The EWOD structures used in this study for material evaluation were described in figure 3.2, and were fabricated by sputtering 300 to 700nm of tantalum onto 500nm of thermally grown SiO$_2$ on a silicon substrate. The tantalum was then anodised to form a uniform thin Ta$_2$O$_5$ layer on the electrode surface. The anodisation voltages used were 20 to 100V, which relate to a nominal thickness of 38 to 180nm. Once fabricated, samples were cross-sectioned and evaluated using a Hitachi 4500 SEM and the film thicknesses agree well with the estimated values. A thickness dependent dielectric constant for thin Ta$_2$O$_5$ has been reported [89]. Hence, capacitance rather than the thickness is monitored when forming anodic Ta$_2$O$_5$ [87] as this is the primary parameter of interest. The capacitance per unit area was measured on samples with different forming voltages and the results of these measurements are presented in fig. 4.4. Forming voltages higher than 50V result in layers thicker than 100nm and the dielectric constant stabilises at approximately 25 [88]. Compare to the dielectrics that have an unchanged dielectric constant (dashed line in fig. 4.4), the capacitance of anodic Ta$_2$O$_5$ reduces much slower when getting thicker. Hence a thicker layer was used in the device as it provided much higher breakdown strength while retaining a relatively high capacitance per unit area.

Figure 4.5(a) shows the anodic Ta$_2$O$_5$ leakage current density depending on applied voltage and its polarity. When 10V DC was applied to a film anodised at 30V (around 57nm thick) and
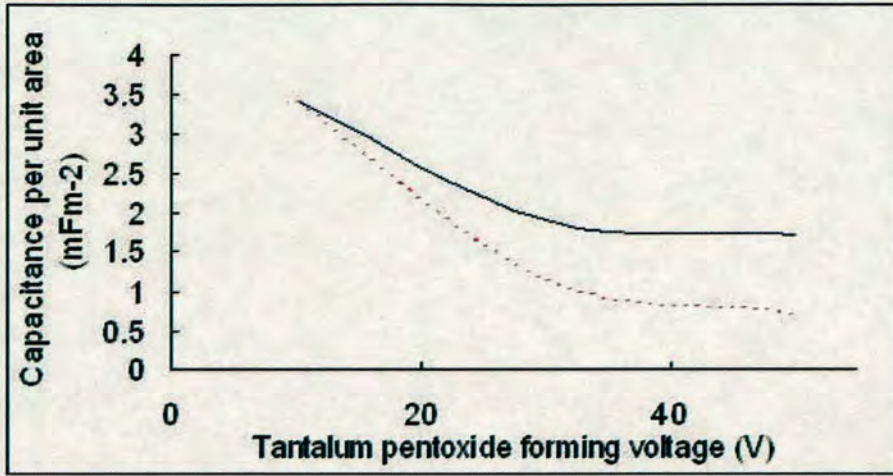
Figure 4.4: *Capacitance per unit area as a function of the anodic Ta_2O_5 forming voltage. The solid curve represents the measured value. The dashed curve shows the calculated value of a dielectric with the same κ value at all thicknesses for comparative study.*

50V (around 95nm thick) with the same polarity as the anodising voltage, leakage current was limited to a few $nAmm^{-2}$. When the applied DC voltage had the opposite polarity, the leakage current density increased dramatically with increasing voltage. Figure 4.5(b) shows the same data plotted against electric field and confirms that leakage current density is an effect intrinsic to the material properties of the anodic Ta_2O_5 layer.

4.4.1 Ultra thin aFP spin coating

As the aFP thickness is an important component in any structure intended for low voltage EWOD device, accurate thickness control and calibration exercises have been carried out to quantify this parameter. These spin-coated film thicknesses depend upon both solution concentration and spin speed [94]. A Laurell® programmable manual spinner was used for the spin coating of Teflon-AF® and CYTOP® layers. Spin times at certain speeds were fixed to 53sec.

Teflon-AF®1600 was diluted by Dupont® in a 6% solution in the solvent C-18. Similarly Asahi Glass Co. Cytop® CTL-809M was diluted in 9% solution by CT-Solv.180. Fluorinert solvent was used to dilute the original Teflon-AF® and CYTOP® solutions, to obtain the required concentration. There were three solvents used for Teflon-AF® dilution: FC75, FC40 and FC43. While with CYTOP® only CT-Solv.180 was used. Different fluorinert solvents have different viscosities and vapour pressures. It is to be expected that the relationship between the spin se-
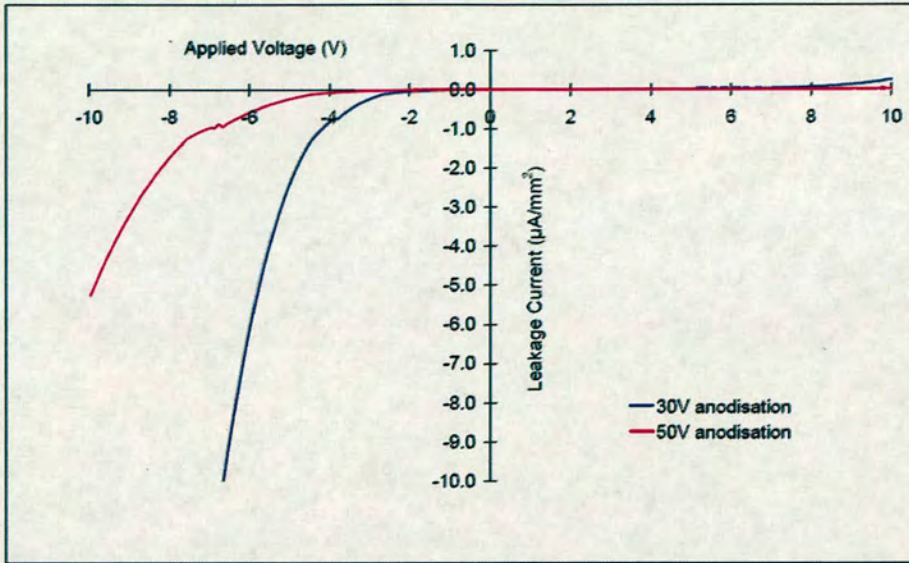
(a)
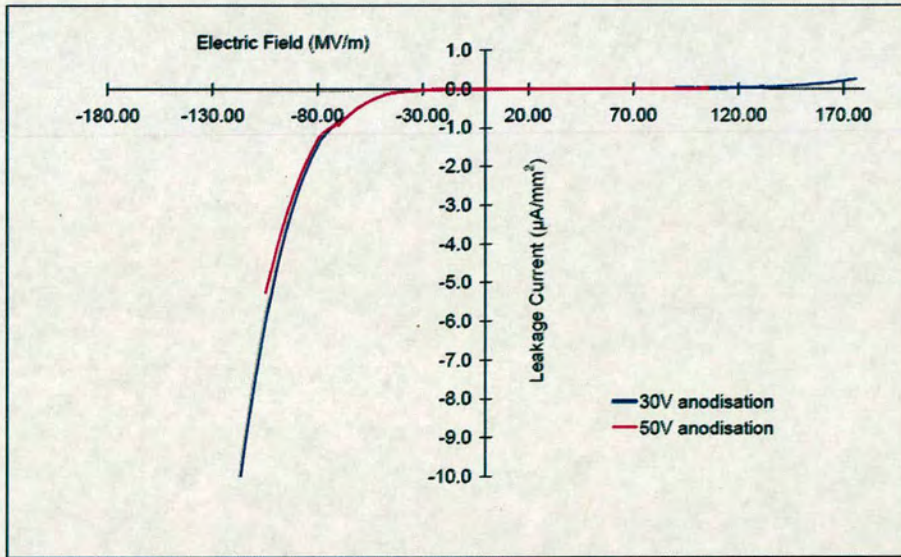
(b)

Figure 4.5: *Anodic Ta$_2$O$_5$ leakage current density as a function of (a) applied voltage and its polarity and (b) electric field.*

tups and the thicknesses will vary. Figure 4.6shows the aFP thickness as a function of different combinations of fluorinert solvents, concentration and spin speed.
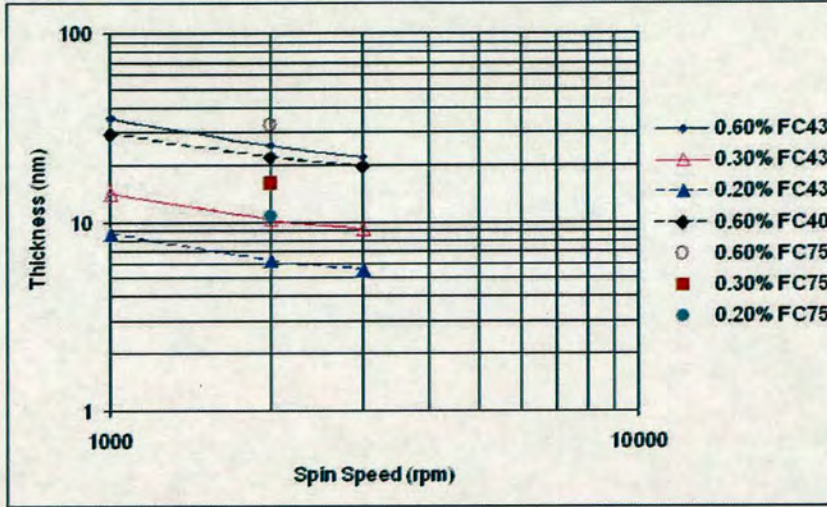
(a)
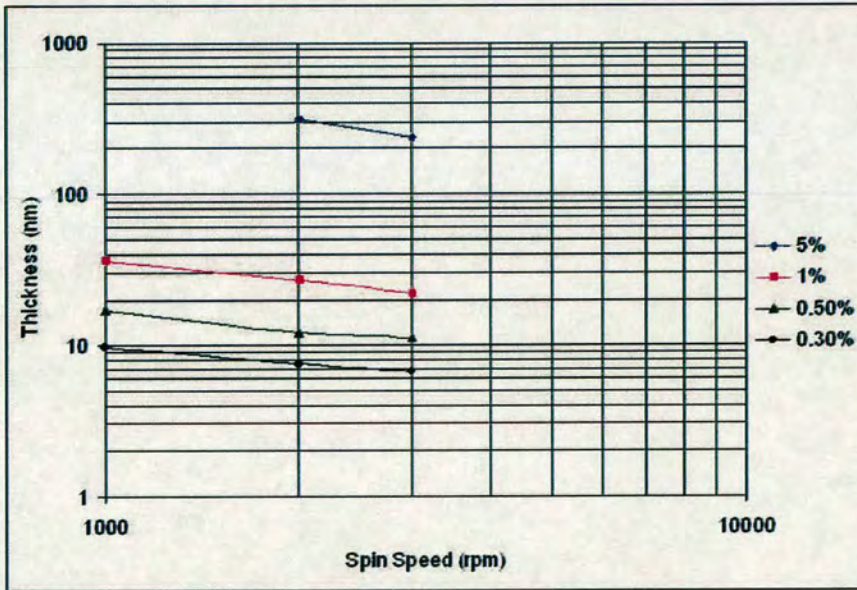
(b)

Figure 4.6: *Film thicknesses of aFP as a result of spin speed. (a) Teflon-AF® with different concentrations and types of solvent. (b) CYTOP® with different concentrations.*

The resulting thicknesses were measured optically using a Nanospec 3000 reflectometer, and a SOPRA SE-5 spectroscopic ellipsometer. The film step-height has been characterised using

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a Veeco 5000 AFM. The step in the Teflon-AF® and CYTOP® films required for this latter measurement was patterned by using 15% FSN (Zonyl Fluorosurfactant) mixed with SPR350 photoresist [94]. Standard photolithography was employed and an oxygen plasma used to etch the exposed Teflon-AF/CYTOP® on the SiO_2 substrate. Both aFP layers showed good uniformity (between 5% and 10%) across the wafer even when thinner than 10nm. For example a typical contour map of a nominally 16nm thick Teflon-AF® layer based on a 25 point thickness measurement on a 75mm wafer with the SOPRA SE-5, is shown in Fig. 4.7.
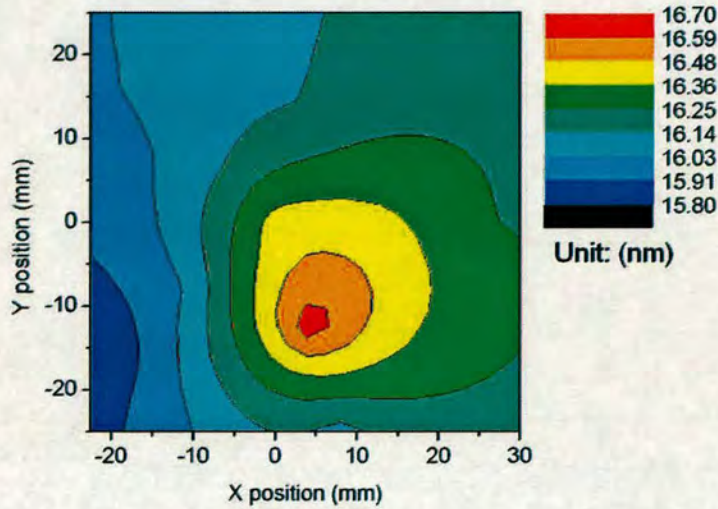
Figure 4.7: *Teflon-AF® coating thickness map of a 75mm wafer (nominal thickness 16nm)*

Teflon-AF® layers of 16nm and 33nm, together with 12nm and 26nm CYTOP® were used in combination with the anodic Ta_2O_5 to examine the performance of the proposed low voltage EWOD process. The mean surface roughness R_a of the samples was measured before and after anodisation and also after aFP coating. The as-sputtered Ta metal electrodes have the highest R_a (6nm), while for Ta_2O_5 R_a ranged between 0.4 and 0.6nm. After the aFP spin coating, the R_a change was negligible. This confirms that anodic Ta_2O_5 is a good candidate material for EWOD since the smooth surface reduces the contact angle hysteresis [42, 93].

4.5 Measurements

The EWOD phenomenon can be quantitatively characterised using a contact angle (CA) measurement system [41] on a sample such as that shown schematically in Fig. 3.2. In this work, the contact angle has been measured by placing a 5μL DI water droplet on samples coated with

different thicknesses of Teflon-AF$^{®}$/CYTOP$^{®}$ and Ta$_2$O$_5$ dielectric with the tantalum metal remaining from the production of the anodic Ta$_2$O$_5$ layer forming the bottom electrode. This structure, together with a thin tungsten wire placed into the droplet, provides the means to apply a potential difference across the liquid and dielectric layers.

The initial static contact angle on each aFP sample was measured using an optical DSA100 system from Kruss. The initial static CA on Teflon-AF$^{®}$ without any applied electric field is about 121°, and 114° on CYTOP$^{®}$. As the water-air surface tension is about 72mJm^{-2}, air-Teflon-AF$^{®}$ and air-CYTOP$^{®}$ are both approximately 18mJm^{-2}, the solid-water surface tension was calculated to be 18.5mJm^{-2} for Teflon-AF$^{®}$ and 17.6mJm^{-2} for CYTOP. The liquid-solid surface thermodynamic limitation (when liquid-solid surface tension is zero) [42, 43] predicts a theoretical saturation contact angle of around 75° for both Teflon-AF$^{®}$ and CYTOP. The contact angle has been reported to saturate at values that range from 60° to 80° [33, 41, 43–45]. (Contact angle saturation will be discussed in the next section.) In this work, the voltage which causes the contact angle on both the Teflon-AF$^{®}$ and CYTOP$^{®}$ systems to change to 81° as shown in figure 4.9 has been defined as the critical driving voltage, V_c.

4.6 Results and discussion

4.6.1 Dynamic contact angle with applied voltage

Performing dynamic contact angle measurements, on samples with different thickness combinations of Teflon-AF$^{®}$ CYTOP$^{®}$ and Ta$_2$O$_5$ has confirmed the relative contributions of the dielectric layers to the value of V_c. When the insulating dielectric layer in EWOD has a high dielectric constant κ (e.g. greater than 10) and a thickness less than 100nm, the hydrophobic fluoropolymer (in this case Teflon-AF$^{®}$ and CYTOP) thickness has the dominant effect on the driving voltage. Fig. 4.9 and Fig. 4.10 compare measured values of contact angle as a function of applied voltage with theoretical curves based on equation (4.1). The horizontal dashed line indicates the 81° contact angle that defines the critical voltage discussed in the previous section.

The contact angle changes (121° to 81°) illustrated in Fig. 4.8 were achieved by applying 13V to a film comprised of 16nm Teflon-AF$^{®}$ on 38nm Ta$_2$O$_5$ as shown in Fig. 4.9(a). Similarly 114° to 81° change was achieved with 11 to 12V applied to a 12nm CYTOP$^{®}$ film on both 38nm and 95nm Ta$_2$O$_5$ dielectrics (fig. 4.9(b)). It can be observed in Fig. 4.9(a) that samples with thicker Ta$_2$O$_5$ (up to 180nm) still achieve a 40° contact angle change for voltages less than
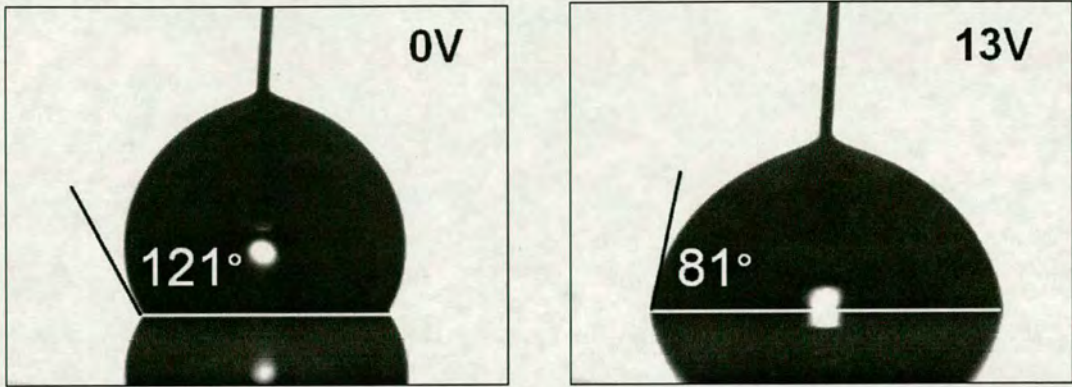
Figure 4.8: *5μl droplets on Ta$_2$O$_5$ (38nm) covered by Teflon-AF® (16nm) with (left) 0 volts and (right) 13 volts applied.*

15V DC.

Fig. 4.10 shows that for samples with identical Ta$_2$O$_5$ thicknesses, those with slightly thicker Teflon-AF® (33nm) and CYTOP® (26nm) clearly require a higher driving voltage. For example, fig. 4.10(a) indicates that more than 15V is required for a 40° contact angle change on the thicker Teflon-AF® (33nm) sample.

4.6.2 Contact angle saturation

In Fig. 4.9 and Fig. 4.10, the experimental data shows that the contact angle saturates when it reaches about 75° to 80° . This effect has been reported by many other authors [33, 41–45]. Proposed explanations include charge trapping [33], a natural thermodynamic limit [42, 43], energy balance [44], electrostatic force [95] and ionisation of air [45].

Quinn et al. and Berry et al. suggest that the contact angle changes following the Young-Lippmann equation were limited by the thermodynamic limitation. Beyond this thermodynamic limitation, the change of contact angle becomes unstable and alternation of the aFP layer properties has been noticed [42, 43].

Moon et al. observed that for the thinnest dielectric layers saturation occurred with the smallest change in the contact angle [41]. The contact angles on the 70nm BST sample started to saturate at around 90° [41], even earlier than the thermodynamic limitation. In this work, the availability
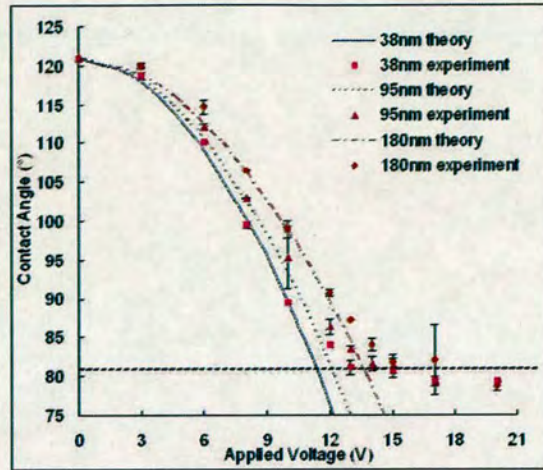
(a)
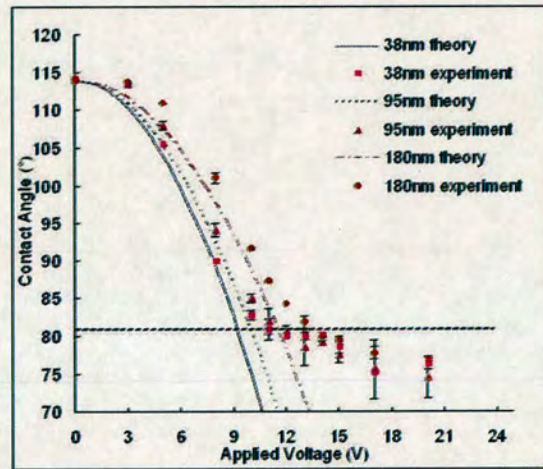
(b)

Figure 4.9: *(a) Contact angle vs. DC voltage for Ta_2O_5 samples (thickness 38, 95 and 180nm) with 16nm Teflon-AF® layer. (b) Contact angle vs. DC voltage for Ta_2O_5 samples (thickness 38, 95 and 180nm) with 12nm CYTOP layer.*

of even thinner aFP layer has enabled a fuller illustration of the phenomenon. In figure 4.11(a), the contact angle on a sample with thicker total dielectric layer thickness (187.5nm, consisting of 7.5nm CYTOP® and 180nm Ta_2O_5) saturates earlier than a thinner one (64nm, consisting of 26nm CYTOP® and 38nm Ta_2O_5), and is contrary to Moon's observations that contact angle saturates earlier on thinner insulating layers [41]. However, the aFP layer (7.5nm) on the 187.5nm sample where contact angle saturates earlier is thinner than the aFP layer (26nm) on the 64nm sample. Whether the early saturation is more sensitive to the aFP thickness rather

55
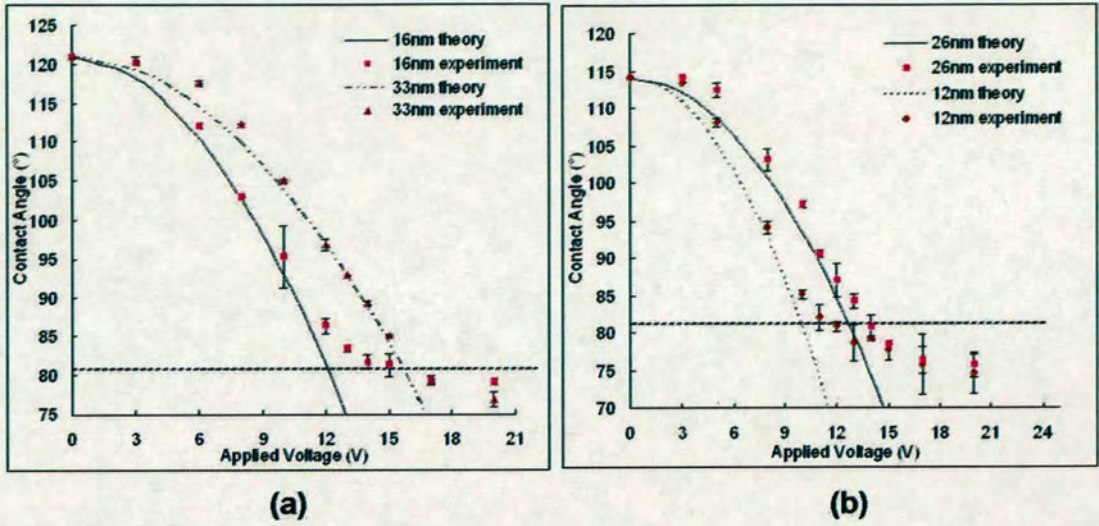
Figure 4.10: *(a) Contact angle for 5µL of DI water as a function of DC voltage for 95nm Ta$_2$O$_5$ with 16nm or 33nm Teflon-AF. (b) Contact angle for 5µL of DI water as a function of DC voltage for 95nm Ta$_2$O$_5$ with 12nm or 26nm CYTOP.*
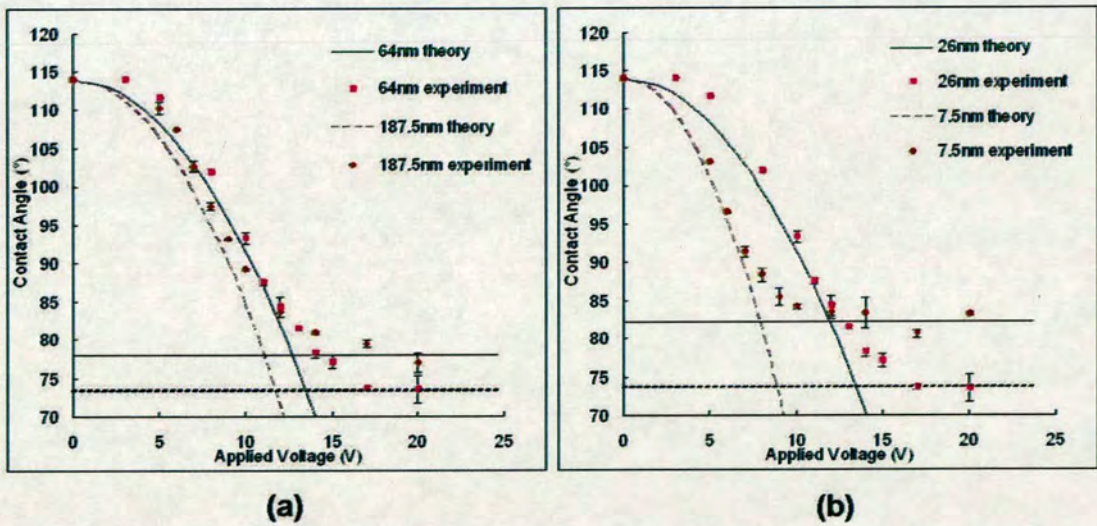
Figure 4.11: *(a) Contact angle for 5µL of DI water as a function of DC voltage for total dielectric thickness: 64nm and 187.5nm. (b) Contact angle for 5µL of DI water as a function of DC voltage for aFP layer only thickness: 7.5 and 26nm.*

than the total thickness needs to be examined.

In fig. 4.11(b), an earlier saturation contact angle can be clearly observed on a thinner CYTOP®
layer coated on a 38nm Ta_2O_5 layer. Thus in this case the aFP layer thickness appears to affect
the contact angle saturation more than the insulating layer. The exact model of contact angle
saturation phenomenon in this case remains unclear. The thermodynamic limitation hypothe-
sis [42] is not particularly successful in explaining the mismatching of saturation voltages in
data presented in both this thesis and [41]. Meanwhile, Berry et al. used ultra thin insulating
and aFP (less than 20nm) dielectric layers, but early contact angle saturation results were not
observed at all.

Further discussion for explaining this observation will be included in section 4.7.

4.6.3 Droplet manipulation demonstration
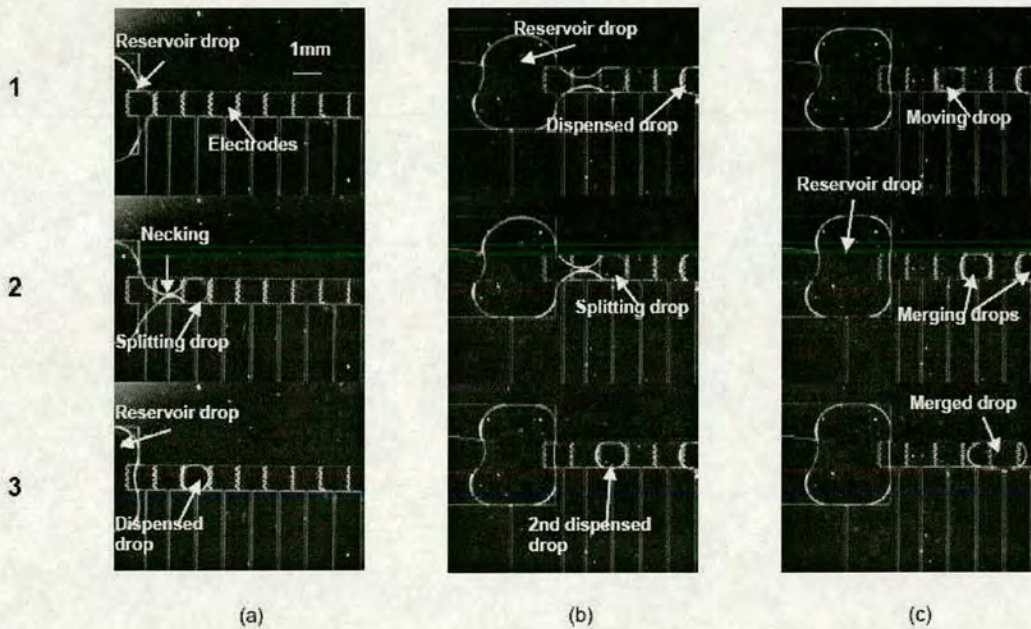
Figure 4.12: *Three frames in sequence (1-3) showing (a) first drop splitting from reservoir (b)
a second drop splitting from reservoir (c) two dispensed drops merging together.
The distance between top plate and electrode array is 125 μm and operating
voltage is 14V.*

As a demonstration of the Ta_2O_5/aFP system a droplet manipulation structure similar to the

design in [49] was used. Fig. 4.12 shows microdroplet splitting, moving and merging, which have all been achieved at a voltage as low as 14V[1]. Initially a relatively big droplet (~1.5μL) was dispensed onto a reservoir electrode. A conductive ITO (indium-tin-oxide) glass plate covered by 17nm Teflon-AF® was then placed in parallel on top of the EWOD chip, providing a ground connection [49]. The height of the ITO cover glass was determined by 125μm thick spacers.

Fig. 4.12 shows three 1mm square electrodes, next to the reservoir electrode, to which 14V is applied, with the liquid beginning to emerge from the reservoir (frame 1 in Fig. 4.12(a)). Once the first two square electrodes are switched off and the reservoir electrode being left on, the liquid is pulled back leaving a smaller drop (around 100nL) on the square electrode (frame 2 and 3 in Fig. 4.12(a)). This droplet can then be then moved forward, and a second droplet dispensed in a similar manner (Fig. 4.12(b)). These two small drops are then moved towards each other and merged (fig. 4.12(c)).

This demonstrates that the fundamental EWOD microfluidic manipulations such as splitting, moving and merging can be realised at a driving voltage lower than 15V using the thin aFP on anodic Ta_2O_5 fabrication technology. No dielectric failure was observed during these EWOD operations.

During an overnight test, the droplet had been continuously driven back and forward on an electrode array for more than 18 hours before the program was terminated. Using 10Hz pulsed 15V driving voltage and droplet in oil scheme, the hysteresis caused by charge trapping did not appear. This proved the high reliability of the anodic Ta_2O_5 technology.

4.7 Electric field induced Early Contact Angle Saturation

4.7.1 Electric fields in Ultra-thin aFP layers

The aFP and insulating dielectric double layers shown in figure 2.12 can be modeled as series capacitors. Hence, the voltages across each capacitor and then respective electric fields are related to their capacitances values. If the applied voltage is V, while the capacitances of the aFP layer and insulating layer are C_{aFP} and C_{ins} respectively, the voltage and electric field on the aFP layer will be:

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[1]More droplet movement: http://www.see.ed.ac.uk/IMNS/projects/MEMS/Microfluidics/Microfluidics.html

$$V_{aFP} = \frac{C_{ins}}{C_{ins} + C_{aFP}} \cdot V \qquad (4.3)$$

$$E_{aFP} = \frac{C_{ins}}{(C_{ins} + C_{aFP}) \cdot t_{aFP}} \cdot V \qquad (4.4)$$

During EWOD operation on ultra-thin(<50nm) aFP layers, E_{aFP} can easily be as high as a few hundred MVm^{-1}, much higher than the breakdown strength of aFP layers (around $110MVm^{-1}$). However, due to the existence of the insulating layer which typically has a much higher breakdown strength, the breakdown of aFP layers does not occur [42]. To the author's knowledge, the potential effect of this high electric field on the EWOD performance has not been considered in the literatures.

4.7.2 Early Contact Angle Saturation

As discussed in the previous section, contact angle saturation occurring before the thermal dynamic limitation were observed. All the samples having this phenomenon during characterising had a thin layer of aFP and a high-κ insulating layer. From equation (4.4), this combination has the majority voltage being applied across the aFP layer. Hence there is a possibility that the E_{aFP} may reach a threshold value causing early contact angle saturation.

Instead of the CA-V curves used previously, figure 4.13 and 4.14 show the contact angle plotted against electric field strength in the CYTOP® and Teflon-AF® layers.

Teflon-AF® samples start saturation when the electric field is around $450MVm^{-1}$, while for CYTOP® it is around $400MVm^{-1}$. This observation agrees with the BST result presented by Moon, where contact angle starts to saturate when electric field in Teflon went above $485MVm^{-1}$ [41].

It is suggested that the reason why Berry et al. did not observe this phenomenon was the relatively low electric field in their CYTOP® samples, which was below $375MVm^{-1}$ [42].

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(a)   **(b)**
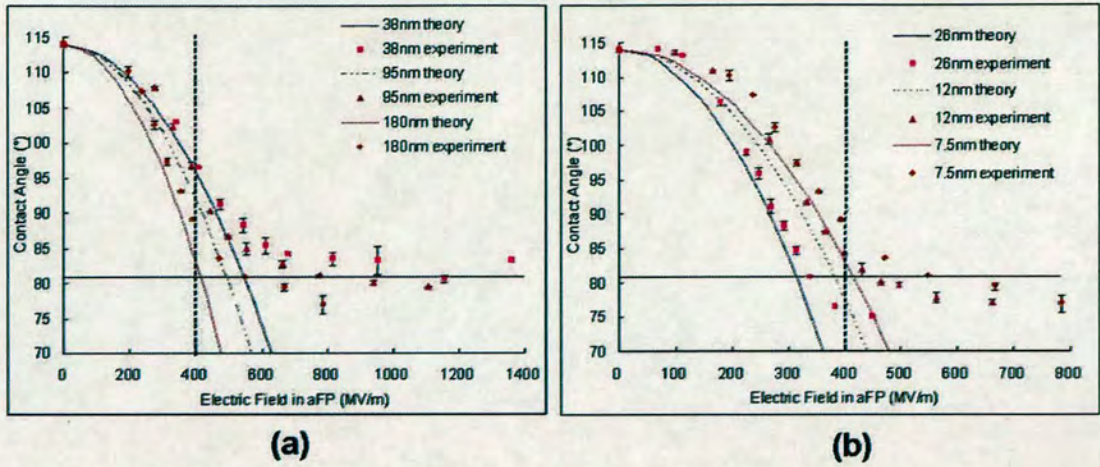
Figure 4.13: *Contact angle as a function of Electric field in CYTOP® layers. (Solid lines indicate the saturation value at thermal dynamic limitation. Dashed lines indicate the threshold E_{aFP} value of early saturation.) (a)Samples with 7.5nm CYTOP® and different thicknesses of anodic Ta_2O_5 layers. (b)Samples with 95nm anodic Ta_2O_5 and different thicknesses of CYTOP®.*
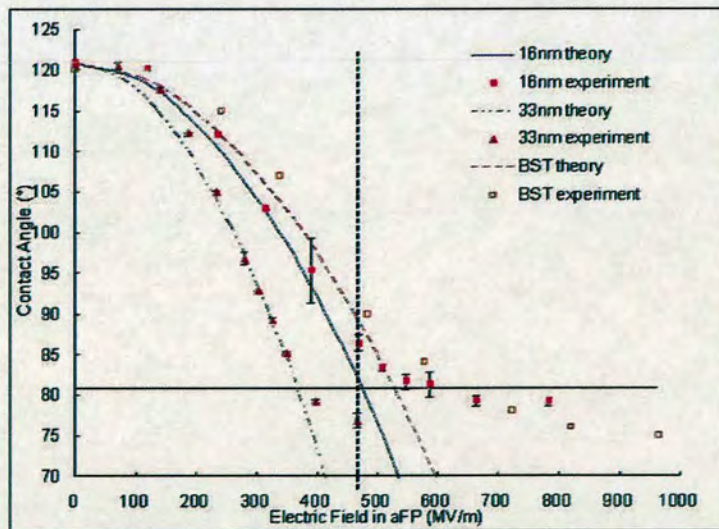
Figure 4.14: *Contact angle as a function of electric field in Teflon-AF® layers. (Solid lines indicate the saturation value at thermal dynamic limitation. Dashed lines indicate the threshold E_{aFP} value of early saturation.) BST results were obtained from [41]. Teflon-AF® with thicknesses of 16nm and 33nm both have 95nm anodic Ta_2O_5 as insulating layers.*

4.8   Conclusion and discussion

High-κ anodic Ta_2O_5 promises to be an extremely useful material for EWOD. Its smooth surface allows an ultra thin uniformly coated aFP top layer to enable robust sub-15V critical EWOD driving voltages. It has been shown that in this case, increasing the κ of the insulating layer is of less importance than decreasing the thickness of the aFP layer, which now becomes feasible due to the excellent properties of the Ta_2O_5 film.

Both Teflon-AF® and CYTOP® work well with anodic Ta_2O_5, producing results close to those predicted. CYTOP® is not as effective as Teflon-AF® because of a lower initial CA and a similar saturation value. The proposed dielectric sandwich that takes full advantage of the thin aFP has been demonstrated using an EWOD structure which has been able to successfully split, move and merge droplets with a driving voltage of 14V, bringing it within the range of more standard integrated circuit technologies.

Earlier contact angle saturation is found on thinner aFP samples, despite a thicker insulating dielectric layer underneath. Previous contact angle saturation theories such as charge trapping [33], a natural thermodynamic limit [42, 43], energy balance [44], electrostatic force [95] and ionisation of air [45] are not able to explain this phenomenon, and a new explanation has been presented. By examining the results in this work and in works presented earlier by Moon and Berry, an interpretation of electric field value and early contact angle saturation has been examined in detail.

Other high quality and high-κ film processes e.g. PLD (Pulsed Laser Deposition) and ALD (Atomic Layer Deposition) materials have the potential to be used in EWOD, for depositing both the insulating and aFP layers, due to their ability to control their thickness to a few Angstroms and relatively low deposition temperature (typically 30 to 500°C) [96–100]. However, it should be remembered that for many EWOD applications the electrode area is large and extremely low defectivity in the insulating dielectric film is required. The ability of these processes to meet this stringent demand remains to be demonstrated.

Chapter 5
EWOD Electrode Array

5.1 Large EWOD arrays

In recent years, there has been an increasing number of demonstrations of bioassays executed concurrently on a digital microfluidics-based biochip [6, 101]. Furthermore, it is clear that system integration and application complexity are expected to increase steadily.

One of the advantages of a digital microfluidic system based on EWOD technology is the ability to reconfigure the system. This means that the different manipulations required can be achieved on the same electrode array by simply modifying the control software. Examples of reconfigurable digital microfluidic systems based on EWOD technology and DEP technology have been reported for sample analysis that use reagent mixing [6, 21, 22, 102, 103].

Large electrode arrays have the potential to greatly increase the reconfiguration possibilities, including:

- **Greater system flexibility** Increases the defect tolerance capability in the system, allowing increased flexibility in route selection [6, 101]. More functional units, such as droplet mixers, consisting of different numbers of electrodes [6, 101].

- **Higher sample processing throughput** More droplet samples can be processed simultaneously.

- **Finer control of droplet volume** Enables the system to have a higher resolution of droplet volumes.

Several examples showing defect tolerant design and spontaneous multiple droplet manipulations on electrode arrays can be found in the literature [6, 101].

Obviously in a passive EWOD system, there is no internal control circuitry available, and each driving electrode in the device must be individually addressed from a contact pad via inter-

connect. While the interconnect for single and double rows of electrodes can be simply implemented on a single level of metallisation, the same is not the case for arrays with electrode counts of 3×3 or greater. The interconnects from the inner electrodes in the M × N array to the exterior control circuit must run between the electrode gaps. This is demonstrated in figure 5.1 which shows a single-level-metallisation micro-heater array using a passive single level metal addressing mechanism.
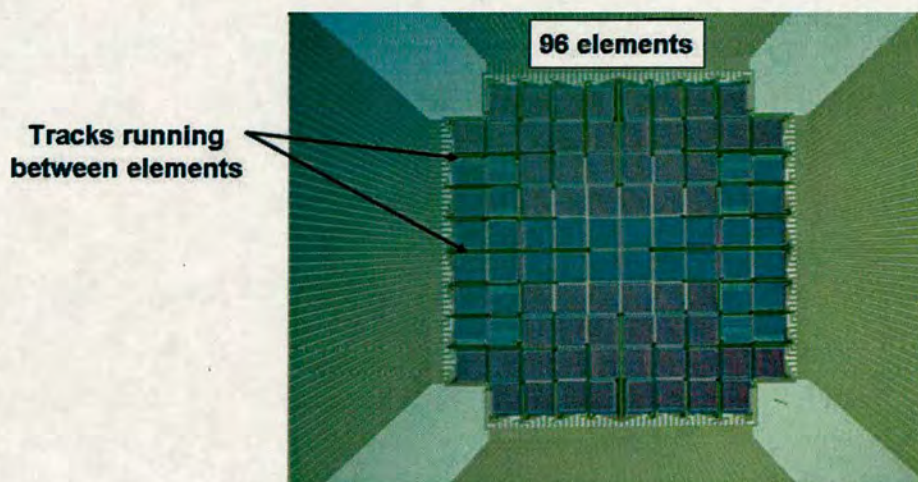
Figure 5.1: *96 element microheater array, an example of a single-level-metallisation large array having interconnect tracks running between elements/electrodes.*

In EWOD devices, the interconnects also often suffer from unwanted wetting because they are, in effect, just small electrodes (figure 5.2). This wetting phenomenon will potentially affect the droplet manipulation, especially when there are many tracks routed between two electrodes as shown in figure 5.1. Even when they are held at ground potential, the electrode gaps will be unacceptablely wide when several interconnects pass through.

Hence, for EWOD arrays equal to or larger than 3 × 3 electrodes, multilevel metallisation is required to avoid the influence of interconnects by burying them beneath the EWOD functional electrodes.

5.2 Multi-level metallisation EWOD array

Multi-level metallisation EWOD arrays using chromium and chromium/platinum on glass and silicon substrates have previously been fabricated for reconfigurable multi-functional microflu-
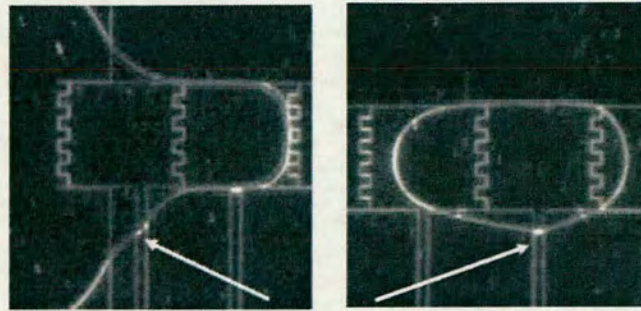
**Unwanted wetting of the
interconnect track causes
droplet distortion**

Figure 5.2: *Wetting phenomenon on interconnects in a single metallisation EWOD device*

idic systems [20, 30, 101].

Aluminium multilayer interconnect structures have been widely employed in standard CMOS circuitry fabrication, while a single layer of aluminium has been demonstrated as a passive EWOD electrode material in Chapter 3. Hence, a two-level aluminium metallisation process for M × N EWOD electrode array fabrication is clearly feasible. Figure 5.3 shows the similarity of using the multi-level metallisation aluminium as interconnects in standard CMOS chips and EWOD devices.
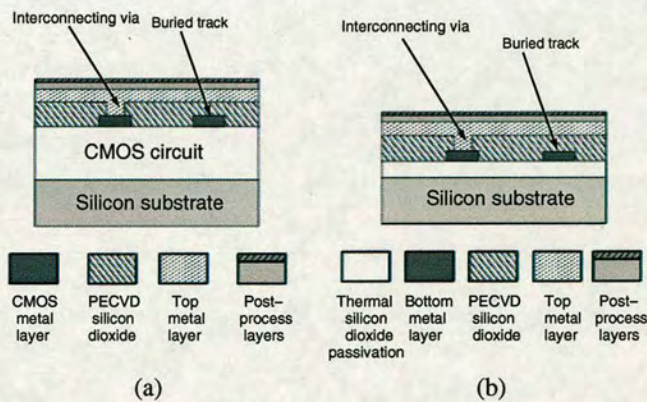
Figure 5.3: *(a) Cross-section of a CMOS chip using aluminium as interconnect material. (b) cross-section of a two-level metallisation EWOD chip using aluminium electrodes.*

The process flow for fabricating a 2-level metallisation EWOD electrode array is detailed below and illustrated in figure 5.4:

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(a) The bottom aluminium layer is sputtered on the SiO_2 insulated silicon substrate.

(b) It was then patterned to form the bond pads and the interconnects, thicknesses ranges between 0.1 and 1μm.

(c) After the patterning, the interconnect covered by 1 μm of PECVD SiO_2 for general electrical insulation between the metal layers. Interlayer vias are then opened by patterning the PECVD SiO_2. The second aluminium layer is then sputtered over the PECVD SiO_2, connecting to the bottom aluminium layer in the vias.

(d) After the patterning the second aluminium, insulating dielectric (500nm Parylene-C) and 50nm Teflon-AF® were finally deposited.

(e) The microscope slide sized chip was then packaged in the same manner as the single metal layer EWOD devices in Chapter 3.
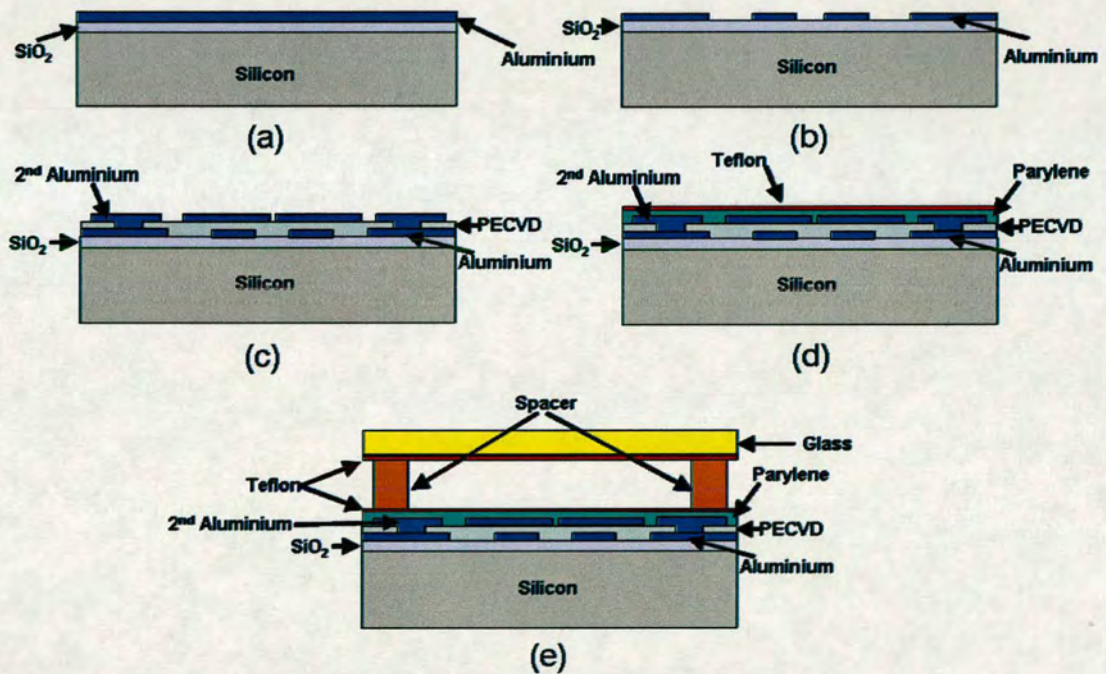
Figure 5.4: *Process flow of fabricating a 2-level metallisation EWOD electrode array using aluminium as interconnect and electrode material.*

Using the same bond pad layout and microscope slide size chip structure discussed in Chapter 3, a 5×8 EWOD electrode array was designed [104]. The bottom aluminium interconnect lines

were 10nm wide. Top metal electrodes were 1mm × 1mm interdigited square electrodes with 100nm wide gaps in between. Using 60V drive voltage, figure 5.5 shows droplet manipulation on a 5 × 4 EWOD electrode array.

(a)

(b)
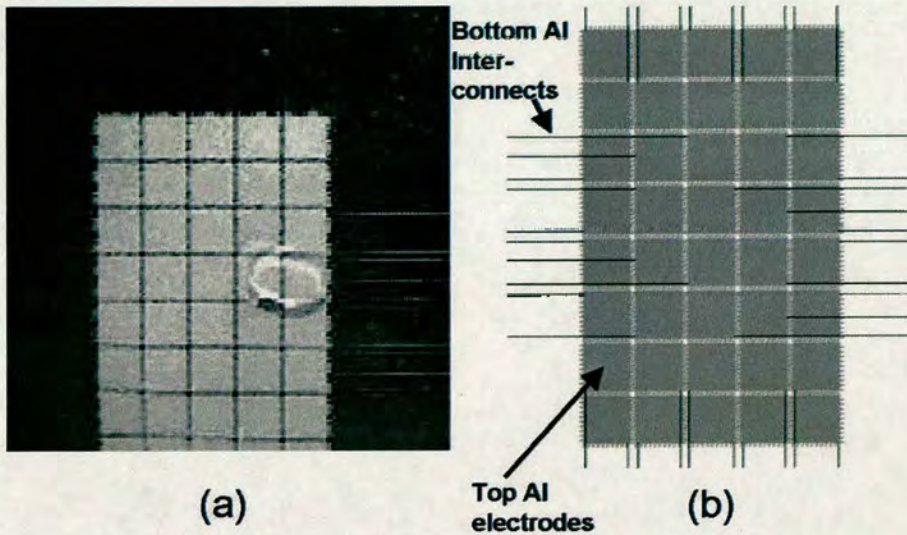
Figure 5.5: *(a)Photograph of a moving droplet on a two-level metallisation (aluminium) 5 × 4 EWOD electrode array with a driving voltage of 60V. This is a two-plate EWOD device with s 440µm droplet height (b) Layout of the 5 × 4 EWOD electrode array.*

5.3 Tantalum-aluminium structures for low voltage EWOD-CMOS systems

Having fabricated a high voltage multi-level metallisation EWOD array using aluminium, the challenge was to select an improved material system that was fully compatible with widely used multi-level aluminium interconnect technology, while at the same time being suitable for low voltage EWOD application.

As discussed in Chapter 4, a low voltage single level EWOD electrode array based upon a high-κ tantalum pentoxide insulating layer has been demonstrated. This material system, which involves no high temperature process, simply consists of $Ta/Ta_2O_5/Teflon\text{-}AF^{\circledR}$ or $CYTOP^{\circledR}$ layers. This is compatible with standard foundry CMOS IC technology for which the metallisation scheme is conventional aluminium interconnect. This section will focus on the fabrication of EWOD systems based on tantalum-aluminium structures.

5.3.1 Structure design and fabrication

To demonstrate the Ta_2O_5-Teflon-AF® dielectric system, the top aluminium layer in figure 5.4 was replaced by sputtered tantalum and patterned using the same mask. Tantalum can then be etched in fluorine-containing plasmas such as CF_4, SF_6, CF_3Cl with CH_3F, sometimes mixed with O_2 [105, 106]. The drawback is that these processes will potentially attack any underlying PECVD SiO_2 layer, which may be problematic if the tantalum etching is not uniform.

By using $SiCl_4$ mixed with NF_3 plasma, Shimada et al. obtained an etch selectivity greater than 80:1 between tantalum and SiO_2 (10:1 in absence of NF_3) [107].

An alternative is XeF_2 dry etching, which is commonly used for silicon etch release in MEMS fabrication, especially post-CMOS etch release due to its high selectivity to other materials (greater than 1000:1 for silicon to SiO_2 and aluminium) [108]. It has also been observed to rapidly etch tantalum as well. The etch process was evaluated using a Memsstar® tool and no aluminium or SiO_2 attack was observed. As shown in figure 5.6, the only potential issue is the degree of undercut with an average value of 3.0µm on each side being measured when etching 0.45µm thick tantalum. As the gap between EWOD electrodes in this case is 30µm, this undercut rate is acceptable and if need be, could be accounted for by a bias in the mask.

SiCl₄ Plasma Etch

-Anisotropic etching
-Poorer selectivity with SiO₂

XeF₂ Etch

- Isotropic etching
- Excellent selectivity with SiO₂
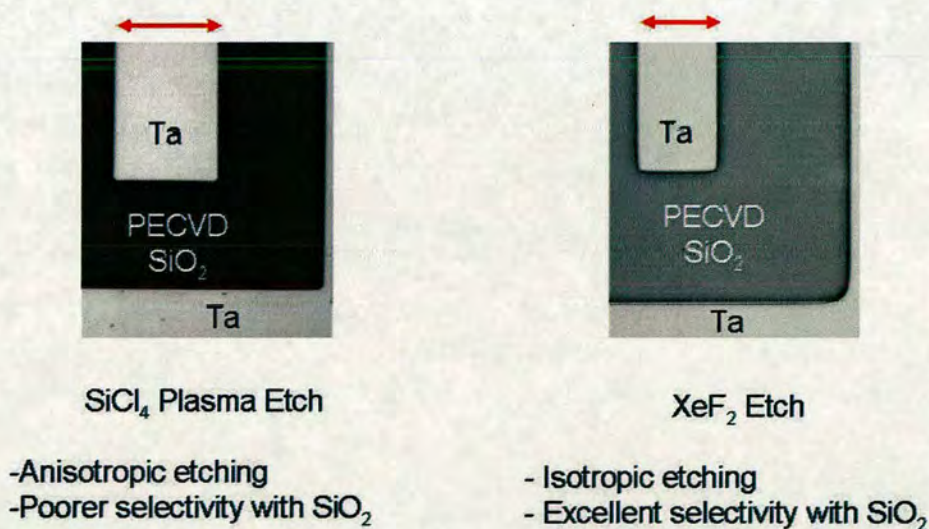
Figure 5.6: *A higher etching selectivity of tantalum to SiO_2 in XeF_2 gas (right) than in $SiCl_4$ plasma (left). Isotropically etched tantalum patterns in XeF_2 gas (right) have a smaller feature size than those anisotropically etched in $SiCl_4$ plasma (left).*

After patterning, the tantalum electrodes are anodised with a gel form citric acid solution as

previously described. The anodising voltage is applied to every electrode on the chip through the EWOD control circuit in same manner as required for droplet manipulation.

A thin Teflon-AF® layer is then deposited using a standard spin coater on the oxidised tantalum electrodes. The surface roughness of the anodic Ta_2O_5 has been measured to have a mean roughness R_a between 0.4 to 0.6nm with the Teflon-AF® layer thickness uniformity across the wafer within 10%.

The resulting EWOD array is a two-level metallisation structure which has aluminium as the bottom metal with tantalum as the second (top) metal electrode. A 50V anodisation voltage was used resulting in 95nm of Ta_2O_5. This was followed by a 0.3% Teflon-AF® solution (diluted in Fluorinert solvent FC-75) being spin coated at 2000 rpm for 50 sec, giving 16nm of Teflon-AF®.

5.3.2 Experiment and results

5.3.2.1 Low voltage droplet manipulation on large EWOD array

A common two-plate configuration EWOD chip [36] has been used in the experiments to evaluate the Ta_2O_5/Teflon-AF® system. A conductive indium tin oxide (ITO) covered glass plate coated with 20nm Teflon-AF® was placed above the EWOD electrode array. The EWOD device here used was the same 5×4 electrode array shown in previous chapter. Spacers were used to define the distance between the plates and hence the height of droplets. In this case the spacers were 258 microns.

This combination of dielectric materials on the EWOD device (95nm Ta_2O_5 and 16nm of Teflon-AF®) enabled deionized water to be moved with a driving voltage of 14V (figure 5.7).

5.3.2.2 Size controllable droplet manipulation using low voltage

Inserting a glass fibre capillary through a plastic ferrule into the two-plate system as a liquid input, a Ta_2O_5 low voltage EWOD system based on a tantalum electrode array with aluminium interconnects shows the ability to dispense and manipulate droplets of different sizes using 15V DC (figure 5.8). The liquid was pressurised through the fibre capillary from a syringe, extruded, cut into a droplet by manipulating the electrodes in the EWOD array in a similar manner to that described in Chapter 3.

Figure 5.7: *Three frames (left to right) showing a moving droplet on a two-level metallisation EWOD chip coated with 95nm Ta_2O_5 and 16nm Teflon-AF® (the outlines of the droplet have been enhanced for clarity).*

Figure 5.8 shows a digital droplet dispense unit dispensing and manipulating droplets with volumes of 80nL, 160nL and 320nL by switching on 1, 2 or 4 electrodes simultaneously. The unit is determining volume by the size of a single electrode and the gap between the two EWOD plates. In this case, each unit electrode was 1×1mm in size and the gap 80 μm. More volume choices are available if the number of electrodes in the array is increased.

(a) (b) (c)
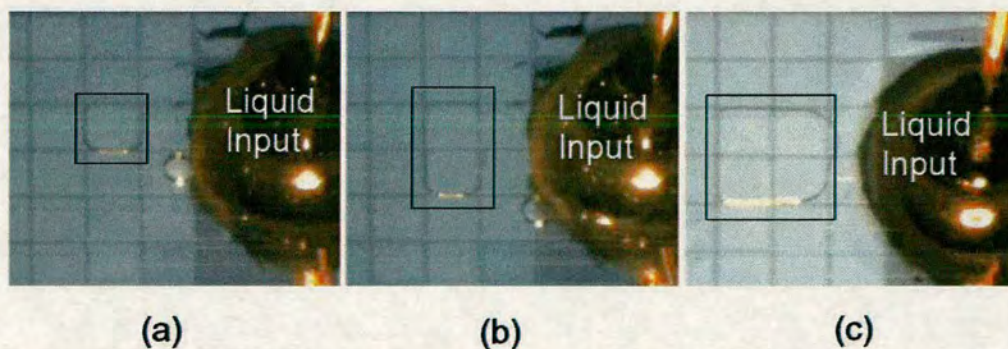
Figure 5.8: *Moving droplets (black boxed) with different volumes (a)80nL (b)160nL (c)320nL, dispensed from a liquid input capillary fibre (on the right of each figures).*

5.4 Conclusions and future work

In this chapter, EWOD electrode arrays larger than 3×3 have been discussed and demonstrated. As a digital microfluidic system that performs different functions on the same electrode array, electrodes in the array can be reconfigured separately or jointly during the operation. The

advantages discussed, such as greater system flexibility, higher sample processing throughput and finer control of droplet volume clearly show a larger electrode array is desirable.

The necessity of multi-level metallisation has been discussed with a 5×4 EWOD electrode array fabricated using a standard CMOS multilayer aluminium interconnect technology. Successful EWOD manipulation with 60V driving voltage has been demonstrated on this electrode array following the fabrication.

Another option for fabricating a large EWOD electrode array system that can drive liquid droplets using voltages less than 15V has then been described. The method of producing a thin uniform Ta_2O_5 film of high permittivity dielectric by the anodisation of tantalum, together with a reliable method of spinning thin uniform Teflon-AF® films that discussed in Chapter 4, are the keys to achieving the required low operating potential. The resulting system, with its robust and pinhole free anodised Ta_2O_5, provided a high dielectric constant and an impervious barrier to the liquids being transported.

Finally, size controllable droplet dispensing using 15V DC as driving voltage was enabled with an aluminium/tantalum/Ta_2O_5/Teflon-AF® structured 5×4 EWOD electrode array.

Integration of CMOS and EWOD Technologies

6.1 Active EWOD arrays

Chapter 5 has demonstrated how multi-level-metallisation is essential for large EWOD electrode arrays. However, the realistic maximum number of electrodes for these passive EWOD systems will ultimately be limited by the packaging considerations. Since there is no internal control circuitry, each EWOD electrodes require its own interconnect and bond pad. Large number of bond pads and interconnects occupy tremendous areas if large passive electrode array systems are implemented. For example, figure 6.1 shows a 96 elements microheater array and its package. When the scale of the array goes above 1,000, such as a 50×50 array, it would require a 2,500 pin package which is not practical with current technologies.
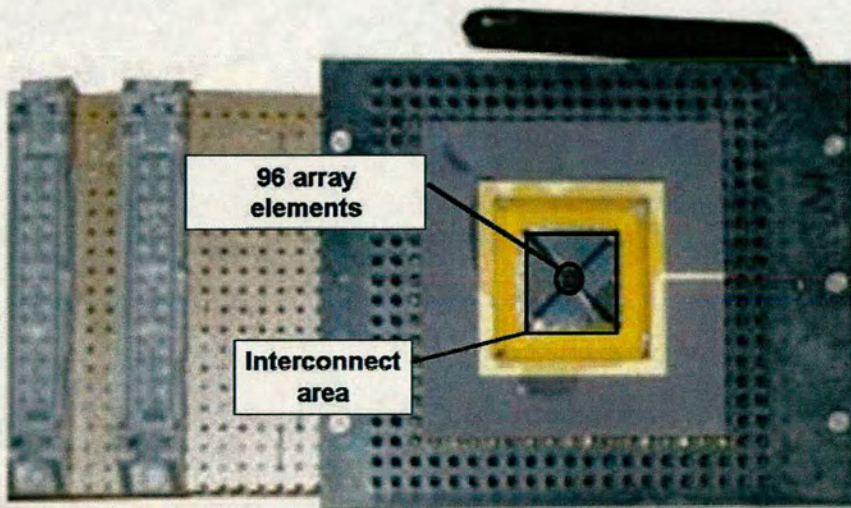
Figure 6.1: *Large interconnect area compare to the elements array in a chip packaging.*

Gong et al. partly address the packaging problem by using printed circuit board (PCB) technology together with land grid array (LGA) sockets [63]. The advantage of this solution is

low-cost and system flexibility (i.e., it is scalable).

However, this does not solve the practical aspect of the interconnect problem entirely as the upper limitation of LGA now is just above 1000. Moreover, the LGA pitch size (typically >1mm, >0.5mm for fine pitch LGA) will limit the electrode size. This is at the limit of a passive electrode drive system and any larger size really requires an active controlling backplane.

Obviously clear advantages exist using on-chip addressing for large two-dimensional arrays. These include a significant reduction in the number of bond pads as well as the simplification of packaging. CMOS technology has been widely used for row-column addressing of large numbers of elements, of which the largest application is related to memory devices. Others examples include CMOS imaging chips [22] and micro displays [109]. This approach to addressing arrays obviously lends itself to the realisation of EWOD arrays and, with a large matrix of electrodes, the use of CMOS for backplane row-column addressing enables the utilisation of existing technology. In addition it also makes it possible to provide the electrodes with additional capabilities such as sensing (e.g. pH, temperature, light, voltage etc) and actuation (e.g. temperature control).

A dielectrophoresis (DEP) system with a 32×32 array of individually addressable electrodes using a CMOS solution has already been demonstrated [22]. Manipulating droplets having more than a 100 fold volume range, it shows a scalable architecture of digital microfluidic systems based on CMOS technology [22].

In another comercialised prototype system, more than 600,000 electrodes have been embedded and separately controlled to create more than 100,000 DEP cages for droplet manipulation[1].

Similar achievements in EWOD systems, named active EWOD electrode arrays (with internal electrode control), can be made if successful integration with CMOS technology is available.

6.2 Comparative study of active EWOD fabrication processes

In CMOS technology enabled active EWOD array design, the droplet electrodes will form the top metal layer of the CMOS systems, similar to those in DEP and CMOS hybrid systems [22]. In this work, this design was potentially achievable, as most of the EWOD devices presented were fabricated using Al and Ta that are both widely used in CMOS fabrications. However, the

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[1]http://www/siliconbiosystems.com/DEPArray.page

variety of ways to integrate the fabrication processes need to be compared.

6.2.1 Compatibility with CMOS technology

Clearly, the process compatibility with CMOS technology is the most critical factor in material selection for fabricating an EWOD system containing CMOS circuitry. Next in priority, pinhole free dielectric layers are the most desirable property. A low driving voltage is preferred if the first two requirements are met, and then costs and process complexity should also be considered.

For selecting suitable insulating materials, a list of potentially suitable EWOD dielectrics with the relevant properties and process conditions are presented in table 6.1.

	Dielectric Constant	Dielectric Strength(MV/cm)	Process Temp. (°C)	Porosity of Thin Layers	Post-Process Complexity
BST	> 30 [a]	10	800	Non	N/A
LPCVD SiO_2	3.8	10	900	Non	N/A
LPCVD Si_3N_4	6 to 8	10	900	Non	N/A
PECVD SiO_2	3.8	8	300	Low	simple
PECVD SiN_x	6 to 9	6	300	Low	simple
Parylene-C	3.1	2.7	25	Non	simple
Anodic Ta_2O_5	8 to 25 [b]	6	25	Non	medium complex

[a] > 100 after annealing at higher temperature
[b] Increases with thickness (> 25 when thicker than 200nm)

Table 6.1: *A table of EWOD dielectrics, their properties and process conditions [41, 88, 110]*

Due to the temperature issues discussed in section 3.3.2, only PECVD dielectrics, Parylene-C and anodic Ta_2O_5 can be considered CMOS process compatible.

The advantages and disadvantages of each material need to be compared to make a decisions to whether they are suitable for current work or have potential for use in the future.

6.2.2 Critical driving voltage concerns

In CMOS devices, where working voltages are typically less than 5V or 5V, higher operating voltage requires a different fabrication process and are less common. Certainly EWOD devices with lower driving voltage is much more desirable when integrated with the CMOS technology. The dielectric layer coated on EWOD electrodes has been proved to have a key role in setting the critical driving voltage of the device.

PECVD dielectrics have medium value of dielectric constant and relatively high dielectric strength. However, since they potentially have defects when deposited as a thin thickness, a waterproof layer such as Parylene-C or thicker aFP hydrophobic layers need to be deposited to prevent electrolysis failure. For this implementation, the voltage required for droplet manipulation was between 40 to 50V.

PECVD dielectrics together with room temperature deposited Parylene-C resulted in a drive voltage around 46 to 62V. Note that Parylene has a relatively low dielectric constant and dielectric strength (table 6.1).

From table 6.1, a tantalum pentoxide with its high κ dielectric and the ability to grown pinhole free) looks promising. This material system, which involves no high temperature process, simply consists of Ta/Ta_2O_5/Teflon-AF® layers, is compatible with standard foundry CMOS IC technology. Droplets manipulation on tantalum aluminium multi-level metallisation samples has already been achieved with a driving voltage as low as 15V.

Hence, a 15V CMOS technology is suitable for active EWOD array fabrication with Ta_2O_5 as the insulating dielectric, while 50 to 100V CMOS technologies are necessary if PECVD dielectrics and Parylene-C are to be used.

6.2.3 Process flow suggestions

Broadly two ways of post processing the active EWOD system were considered.

- Using foundry CMOS with the wafers being delivered for EWOD post processing.

- Design and fabricate a backplane chip on a multi-project wafer in a foundry using post-processing to make the EWOD system.

The first way is obviously preferable, e.g. spin-coated hydrophobic aFP layers can have a better uniformity and easy for integrating anodic Ta deposition related processes. However, since foundry CMOS wafers are very expensive, the cost issue at the R&D stage make the second option attractive.

6.2.4   Post-process complexity

For typical CMOS processes, PECVD dielectrics such as silicon dioxide, silicon nitride or silicon oxi-nitride are widely used to both passivate the top metal (typically 0.5 - 2.0μm thick), and insulate the metal layers. As a vapour deposited polymer, Parylene-C can be uniformly coated on different topologies, such as a CMOS chip wire-bonded in its package. Depositing these two dielectrics as CMOS post-processing on a backplane chip is relatively straightforward.

Spin coated Teflon-AF® and CYTOP® is more difficult to perform on single chips. However, it was proved to be possible to spin coat packaged chips.

For anodic Ta_2O_5, since foundry CMOS is unlikely to have tantalum as a top metal layer, the required post-process is relatively more difficult as more aggressive lithography. .

PECVD and Parylene-C were chosen as the insulating dielectrics in the first active EWOD device fabrication, together with Teflon-AF® as a hydrophobic aFP layer. Issues with low voltage active EWOD system fabrication involving Ta_2O_5 will be discussed in the future work section in this chapter.

6.3   Post-process on an EWOD CMOS backplane chip

6.3.1   Backplane chip design

The first system with an active EWOD electrode array using row and column addressing used a standard 100V CMOS foundry process. As part of EWOD development at Edinburgh, an EWOD/CMOS chip has been fabricated and tested (figure 6.2) using conventional foundry processes and materials [111]. Preparing it for EWOD activation requires post-processing involving the deposition of appropriate dielectric and surface treatment layers.

As discussed previously, an effective EWOD implementation using post processed PECVD dielectrics and Parylene-C as EWOD insulating layers requiring a comparatively high operating
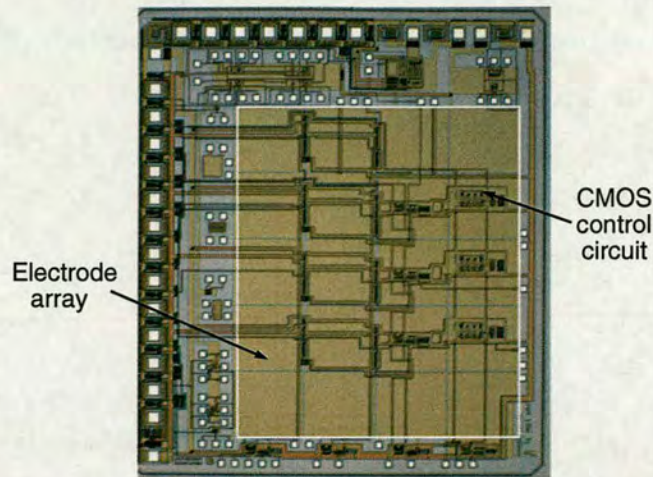
Figure 6.2: *A CMOS backplane chip to be post-processed for building a row-column control EWOD system*

voltage in the region of 40 to 100V to drive droplets. Hence the high drive voltage requirement determined the selection of 100V CMOS foundry process for the EWOD backplane.

The chip was fabricated with other designs on a multi-project wafer, with the cost of a single chip around £30 (118 chips in total). Details of circuit design and testing are presented in [40, 111].

The CMOS backplane chip was delivered from the foundry having a 4×5 electrode array (figure 6.2), with a 500μm × 500μm electrode size. The CMOS row-column addressing circuitry can be easily seen as shown in figure 6.3.

6.3.2 Post processes

The top aluminium metal of the backplane chip is pre-patterned as row/column addressing EWOD electrodes, covered by a passivation layer. The cross-section view is shown in figure 6.4. This foundry passivation could be removed during foundry processing if desired given by designing the electrode array as test pad area, or by suitable post-processes. However, it was retained as an additional layer of EWOD insulating dielectric to simplify the whole process flow. The passivation material is normally silicon oxi-hydro-nitride dielectrics (the exact compound in this case is unknown), and thickness is estimated to be between 0.5 and 2 μm. This is to the equivalent an extra 20 to 40V critical/driving voltage.

Close-up of electrode (500 μm)

**100 V drive circuitry
under the electrodes**
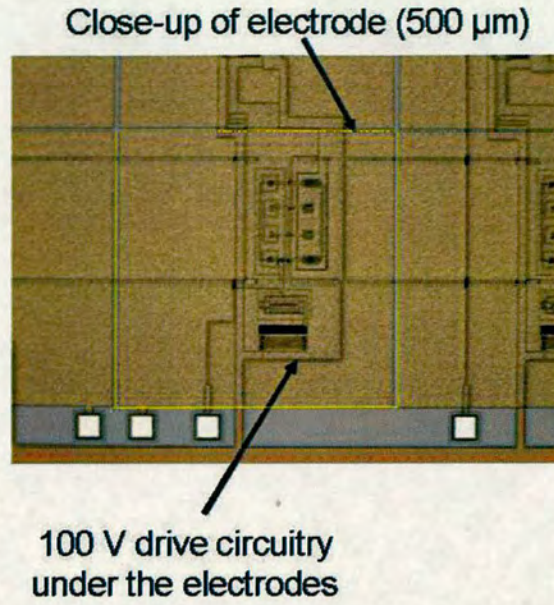
Figure 6.3: *Optical microscopic view of the CMOS row-column addressing circuitry beneath a single electrode. (magnification around 100×)*

Passivation

CMOS devices

Silicon

Aluminium electrodes
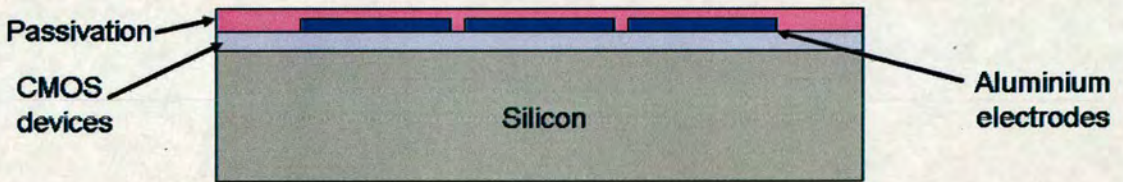
Figure 6.4: *A cross-section view of the EWOD backplane chip delivered from the foundry.*

For evaluating the post-processed active EWOD dielectrics, contact angle tests to establish the driving voltage were carried on passive electrodes containing combinations of similar dielectrics. A 0.5μm low frequency PECVD SiN_x was firstly deposited on the aluminium electrodes as a passivation layer. On some wafers, 150nm Teflon-AF® was deposited, similar to the dielectric evaluation tests in section 3.4. Other wafers had 100nm Parylene-C and 50nm Teflon-AF® layers to ensure the coverage of potential defects.

Both methods achieved a critical/driving voltage around 50V. The measured contact angle - voltage relationship and theoretical curve of the first combination have been previously presented in figure 3.7, while those of the second combination are shown in figure 6.5. Both

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combination of dielectrics exhibit a good yield.
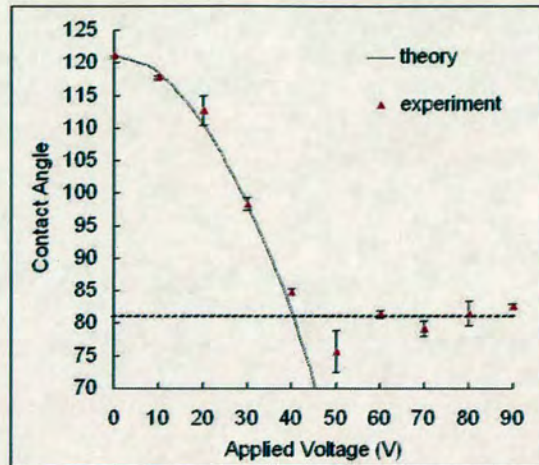
Figure 6.5: *Contact angle vs. voltage of a 5µL droplet on 123nm Parylene-C + 50nm Teflon-AF® + 0.5µm PECVD SiN$_x$. Theoretical curve is given by the Young-Lippmann's equation (2.12).*

The backplane chip was firstly packaged in a 40-pin ceramic package, using gold wire ball-bonding. Then the Parylene-C layer was vapour deposited and Teflon-AF® spin-coated on top. Both processes were performed on the packaged device. The edges and corners of the chip tend to have a thicker Teflon-AF® layer and some striations, due to the difficulties of uniformly spin-coating small rectangular chips. However, the coating at the centre, where electrodes are located was uniform.

6.3.3 Droplet manipulation test

The droplet was manipulated in a coplanar manner (as introduced in Chapter 2, and discussed in Chapter 7), avoiding the problems of assembling a top plate on this tiny chip with spacing materials in between. A 1µL droplet was dispensed from a micropipette onto the electrode array. Two columns of electrodes were addressed to control the droplet movement

One column of electrodes was grounded altogether, providing the reference signal. Another column of electrodes was addressed separately with 60V DC, providing the driving signal. The droplet moved when DC power on a previously driven electrode was switched off and the electrode next to it was connected to 60V, as shown in figure 6.6.

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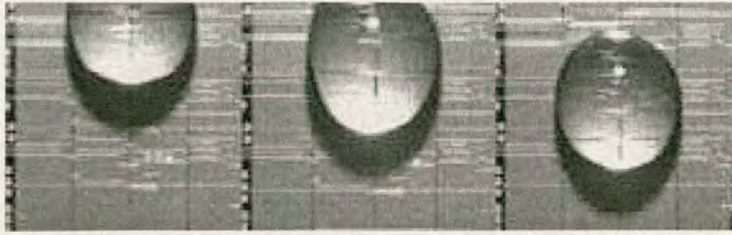
Figure 6.6: *Droplet moving on a backplane chip. (left) A sessile droplet is sitting on two columns of electrodes. One column is grounded and the electrodes in the other are individually connected to a 60V DC source via addressing circuitry. (middle) The electrode next to the droplet position on the powered column is switched on, attracting the droplet towards it. (right) After switching off the electrode on the powered column, where it was previously positioned, the droplet has moved onto the next electrode.*

6.4 Conclusions and future Work

6.4.1 Conclusions

Simple post-processing can enable a CMOS chip to become the basis workable EWOD device and this chapter has discussed how to fabricated a hybrid CMOS-EWOD digital microfluidic system. In addition, an EWOD post-process foundry CMOS chip has been processed and droplet movement demonstrated. However, there remain issues such as hydrophobic surface, high voltage etc.

6.4.2 Future work

As mentioned in table 6.1, the selection of post-processes for fabricating CMOS-EWOD systems after standard CMOS process also includes the process complexity concerns. Anodic Ta_2O_5 is not a standard CMOS process and is more complex than depositing Parylene-C. The design of CMOS circuitry also needs to consider the current flow (although normally in μA range) during anodisation. Decisions need to be made by judging whether a low critical/driving voltage or a simpler and cheaper process is more desirable. Alternatives to anodic Ta_2O_5 are ALD (Atomic Layer Deposition) high κ dielectrics such as ALD Ta_2O_5 and HfO_2 which are pin-hole free and can be deposited at temperatures $< 450°$.

The next step is to significantly increase the number of electrodes so that it becomes possible to implement a programmable electrode array size and start integrating further functionality into

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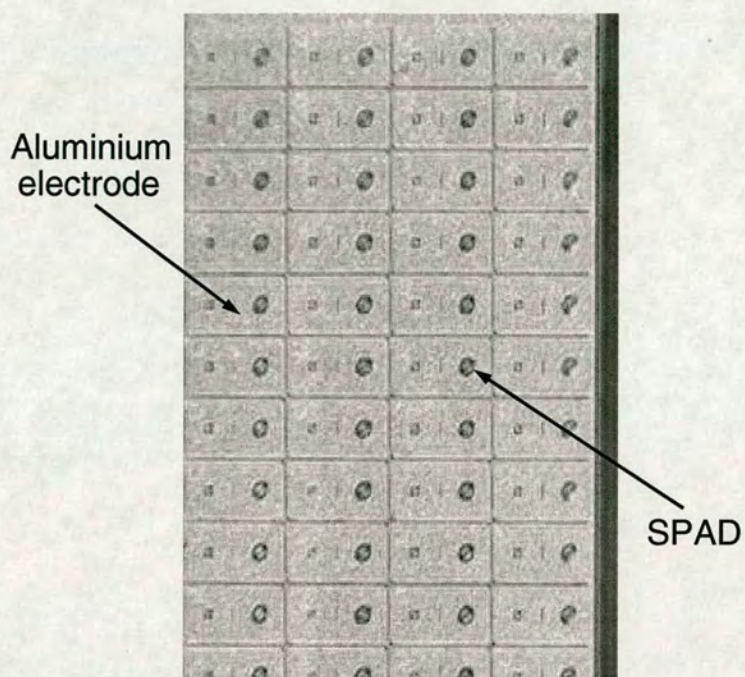
Figure 6.7: *A prototype design of an EWOD array with electrodes integrated with SPAD (Single Photon Avalanche Diodes).*

the electrodes. Figure 6.7 shows part of a prototype design that provides an example of both of these elements. It consists of an EWOD array with $200\mu m \times 100\mu m$ electrodes integrated with SPAD (Single Photon Avalanche Diodes) for light detection and this gives one example of the direction digital microfluidics will be moving in the future.

Chapter 7
Test Structures for Low Voltage Coplanar EWOD System Design

7.1 Introduction

EWOD droplet manipulation systems have two basic architectures, a system with two parallel plates (referred to as two-plate EWOD hereafter) which allows droplets to be manipulated in the gap between the plates, and a coplanar electrode arrangement (referred to as coplanar EWOD hereafter) where no top plate is required.

In practice, the top cover plate provides many advantages (e.g. reliable droplet volume control, gravity insensitivity) [51]. However, one drawback of using a two-plate system is the restrictions imposed by the top-plate, which needs to provide a conductive ground electrode. If this requirement can be removed, then other functions like contact sensing, other microfluidic actuators such as dielectrophoresis (DEP) and surface acoustic waves (SAW) can be integrated using the top plate. Moreover, the packaging processes is simplified when a cover plate can be assembled without a specific gap and no electrical connections.

Recently the increasing interest in developing coplanar EWOD devices has led to the need for test structures to characterise this technology [51]. However, the technology used to fabricate this test structure required nearly 100V DC to modify the contact angle from 110° to 80°. In addition 65V AC voltage was required to move droplets [51] and clearly a lower operating voltage is desirable. Other coplanar EWOD technologies that have emerged in recent years, which have not been characterised in a similar manner [20, 47, 52]. The work discussed in this chapter reports an improved test structure modified for characterising a range of coplanar systems, in particular low voltage device architectures.

7.2 EWOD electrode configurations

7.2.1 Coplanar EWOD systems

The major design difference between the two-plate and coplanar EWOD systems is the arrangement of electrodes. Generally, electrodes can be arranged in six possible ways [47]. Among them, figure 7.1 shows the three most frequently reported EWOD configurations in both architectures [5, 20, 47, 48, 51, 52].
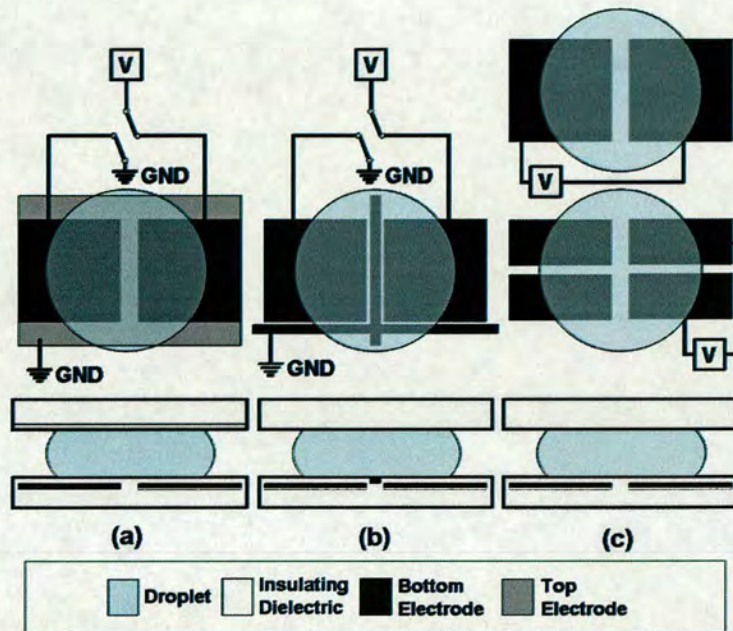
Figure 7.1: *Three electrode design configurations. The hydrophobic aFP layers coated for making the solid-liquid interface hydrophobic are not shown in this figure. Cross-section view (bottom) and top view (top) of (a) two-plate EWOD with no insulating layer on the top plate electrode. (b) coplanar EWOD with ground line. (c) coplanar EWOD using the same electrode arrangements as in the two plate system.*

(a) Two-plate EWOD system. The top plate consists of a single continuous ground electrode coated only with aFP. The bottom plate consists of independently addressable electrodes coated with both insulating and aFP layers. The droplet is sandwiched between them and surrounded by immiscible liquid or gas such as oil or air. Droplet manipulation is performed by controlling the bottom electrodes [5, 20, 47, 48, 51, 52].

(b) Coplanar system with ground line. The aFP coated ground electrode is coplanar with the independently addressable electrodes which are coated with insulating and aFP layers.

Droplet manipulation is achieved in a similar way, moving droplets by controlling the addressable electrodes [20].

(c) General coplanar system. This design only has rectangular electrodes on the bottom plate arranged in the same manner as in a two plate system. The coplanar function is realised by using a different voltage driving scheme in comparison to the configuration using a top electrode. Instead of addressing a single electrode when moving the droplet onto it and grounding the others, two electrodes are addressed with inverse voltage polarities in this scheme.

There are two ways of moving droplet in such a system and one illustrated in the middle of figure 7.1(c). The droplet will be attracted onto both of the addressed electrodes when the other surrounding electrodes are floating.

Another method is the one shown at the top of figure 7.1 where both the electrode where droplet is sitting and the forward electrode are addressed with applied voltages. The droplet will always be attracted onto the positive electrode according to the asymmetric EWOD phenomenon [52].

Obviously, the top plates in the two coplanar configurations are just for system sealing and have no role in the electrical aspect of EWOD manipulation. Hence, any design limitations related to the top plate are not present.
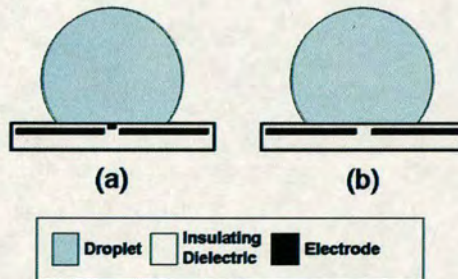
Figure 7.2: *Coplanar EWOD systems. (a) Coplanar with ground configuration. (b) General coplanar electrode configuration*

In previous chapters, most of the dielectric evaluation experiments for determining the critical driving voltage were based on the device shown in figure 2.12 which grounds the droplet using a fine metal wire contacting the top of the droplet in a similar manner to the standard two plate EWOD systems.

Since the electrode working mechanisms are different for coplanar configurations, both the process and electrode design need to be evaluated as well and the above approach is no longer valid.

7.2.2 Model of coplanar devices

Figure 7.3 shows a schematic representation of the system for measuring contact angle as a function of voltage and the related circuits used to model the coplanar configurations. The two plate configuration mode is included for the purpose of comparison. The model for this structure is shown in figure 7.3(b) and models the insulating and aFP layers as the capacitor C_3.

In the coplanar configuration with the ground line (fig. 7.3(c)), the ground line occupies some areas that are occupied by the driving electrodes in the two plate device. The device consists of two driving electrodes with the ground electrode in between and is modeled accordingly. The insulating and aFP layers on the driving electrodes are modeled as two parallel capacitors C_4 and C_5. The ground line only has aFP layer covering it, and is modeled by the capacitor C_{aFP}. Since the aFP layers are typically much thinner than the insulating layer and can not withstand large voltages, the majority of the potential will be dropped across C_4 and C_5 [41, 47].

In the general coplanar configuration, the capacitor on both addressed electrodes are modeled by C_1 and C_2 in figure 7.3(a). If the areas on both electrodes occupied by the droplet are equal then these capacitances are equal. Hence in this case the potential across these capacitors will be equal.

Since the wetting of droplets relates to the average charge density along, and the voltage across the dielectrics underneath the solid-liquid contact line, the area ratios of each electrodes and the gaps between them determine the critical voltage needed to drive the droplets.

7.3 Coplanar EWOD test structure design

7.3.1 Test structures for general coplanar configuration

Figure 7.4 shows a test structure reported for evaluating both the layout and the dielectric layers of a general coplanar configuration [51]. The two radially wedge shaped electrodes are the driving and ground electrodes and position the droplet in the centre. This keeps a constant
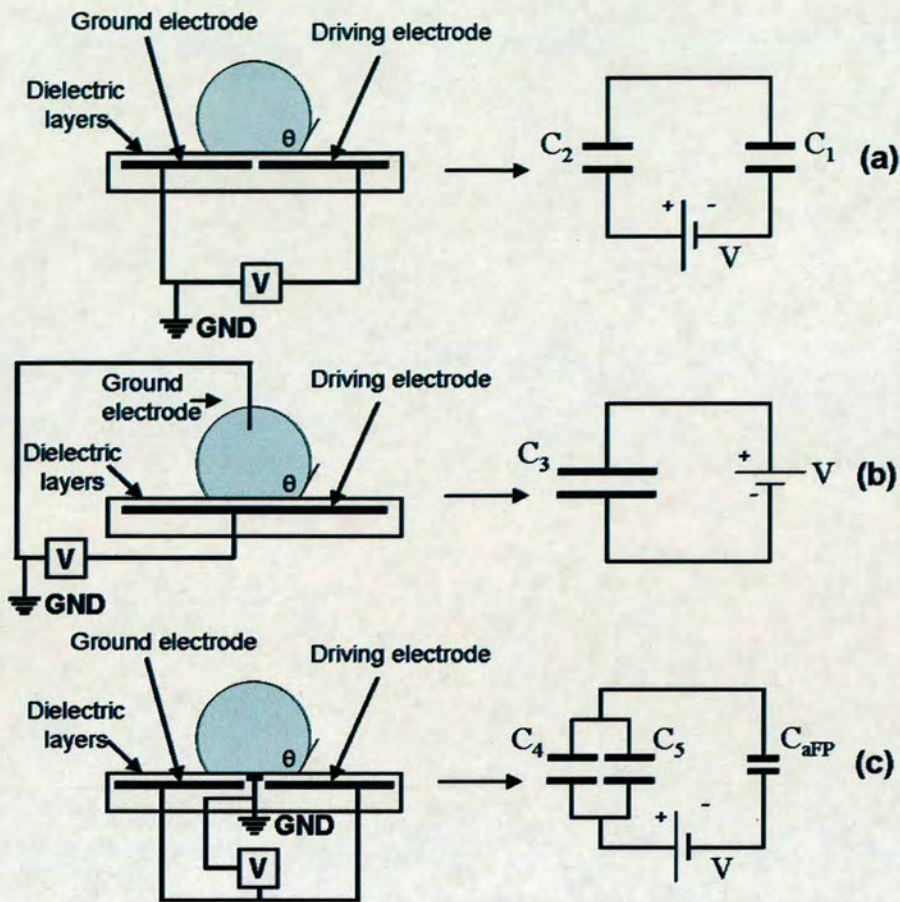
Figure 7.3: *The capacitor networks related to three EWOD electrode design configurations (right), and their contact angle as a function of voltage test devices with related EWOD circuits. (a) General coplanar EWOD model. (b) Two-plate EWOD model. (c) Coplanar EWOD with ground line model (C_4 and C_5 represent the capacitances of the dielectric layers above the ground and driving electrodes, C_{aFP} represents the capacitor model of the aFP layer above the central ground line).*

area ratio for each electrode and the gap area between the electrodes follows the wetting of the droplet (fig. 7.5). The driving electrodes in the test structure are all electrically connected at the centre (fig. 7.4(c)) with the ground electrodes connected around the circumference of the structure (fig. 7.4(d)).

On this test structure, the dependence of the solid-liquid surface tension γ_{sl} at applied voltage V on the entire area covered by the droplet can be modified from the original Lippmann's
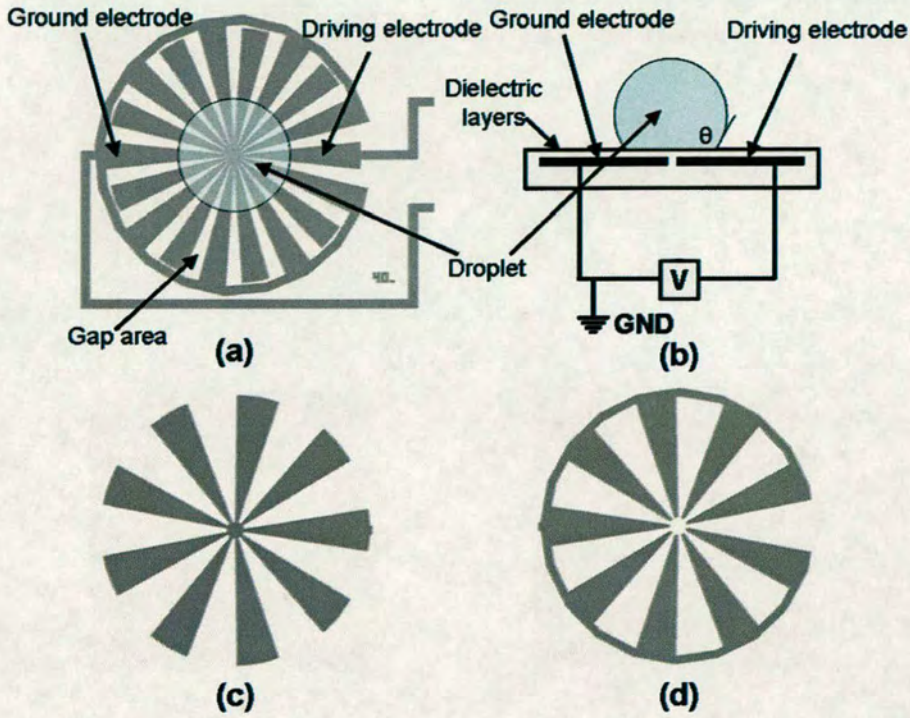
Figure 7.4: *(a) Top view and (b)cross-section (right) of a droplet sitting on a general coplanar configuration test structure with two radially wedge shaped electrodes.*
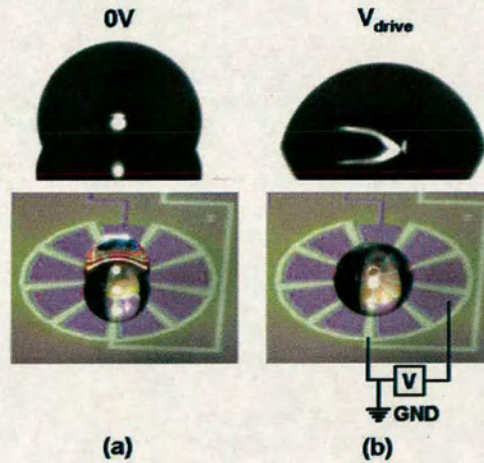
Figure 7.5: *Side view (top) and 3-D view (bottom) of a droplet sitting on a EWOD coplanar test structure with wedge shaped electrodes. (a) Without voltage applied. (b) With voltage applied.*

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equation (2.11):

$$\gamma_{ls}(V) - \gamma_{ls}(0) = \gamma_{ls}^d(V) + \gamma_{ls}^g(V) + \gamma_{ls}^{gap}(V) - \gamma_{ls}^d(0) - \gamma_{ls}^g(0) - \gamma_{ls}^{gap}(0) \qquad (7.1)$$

where $\gamma_{ls}^d(V)$, $\gamma_{ls}^g(V)$, $\gamma_{ls}^{gap}(V)$ and $\gamma_{ls}^d(0)$, $\gamma_{ls}^g(0)$, $\gamma_{ls}^{gap}(0)$ are the solid-liquid surface tensions with or without applied voltages (V or 0) and in different areas (driving electrode, ground electrode and gap area) respectively.

The area of each wedges covered by the droplet is much smaller than the total area covered by the droplet and thus averages the changes in surface tension above the electrodes and the gap area. Based upon this assumption, equation (7.1) can be re-written as [51]:

$$\gamma_{ls}(V) - \gamma_{ls}(0) = -\frac{\varepsilon_r \varepsilon_0}{2t}\left(\frac{A_d}{A_t}V_d^2 + \frac{A_g}{A_t}V_g^2 + \frac{A_{gap}}{A_t}V_{gap}^2\right) \qquad (7.2)$$

Combining equation (7.2) with Young's equation (2.9), the modified Young's-Lippmann equation for general coplanar structures becomes:

$$\cos\theta(V) - \cos\theta(0) = -\frac{\varepsilon_r \varepsilon_0}{2\gamma_{lg}t}\left(\frac{A_d}{A_t}\left(\frac{A_g}{A_d + A_g}\right)^2 + \frac{A_g}{A_t}\left(\frac{A_d}{A_d + A_g}\right)^2\right)V^2 \qquad (7.3)$$

where $\gamma_{ls}(0)$ is the interfacial tension with no voltage applied, A_d, A_g and A_{gap} are the areas over the driving electrodes, the ground electrodes and the gap areas between the electrodes, respectively, A_t is the total combined area, and V_d, V_g and V_{gap} are voltages across the dielectric layers above each electrode areas. [51]

When the area of the ground electrode is equal to the area of driving electrode, the voltage required for a given contact angle change in this design will reach a minimum value. Hence, the electrode sizes in the general coplanar systems were kept identical, and the test structure presented was only designed to study the gap ratio effect [51].

From equation (7.3), it can be determined that when the gap area is kept to a minimum, the minimum critical driving voltage can be achieved. Compared to the two plate configuration, the minimum value is doubled in the general coplanar system if the dielectric layers have the same thicknesses.

The experimental results reported in [51] confirmed the theoretical calculation. With 300nm

PECVD SiO_2 and 200nm CYTOP® and a 2% gap ratio, the critical driving voltage was between 100 and 120V and for droplet manipulation 65 to 80V AC driving voltages were required. Moreover, the high voltage required resulted in dielectric breakdown before contact angle saturation was achieved [51].

7.3.2 Modified test structure for low voltage coplanar configuration

Figure 7.6(b) shows the top electrode in a two plate EWOD systems that only has an aFP layer and so the majority of voltage is applied across the bottom dielectric. Hence, there will be a larger contact angle change at the bottom surface compare to those with insulating layers on either side (fig. 7.6(a)) when applying the same voltages. Since the driving electrodes which generate the wetting force are all located at the bottom plate, the two plate systems typically employs the structure shown in figure 7.6(b) to achieve a much lower critical driving voltage. This result suggested that coplanar with ground line devices could have a lower driving voltage than the general coplanar devices due to a larger potential drop across the dielectrics on driving electrodes, since the ground line is only coated with aFP.
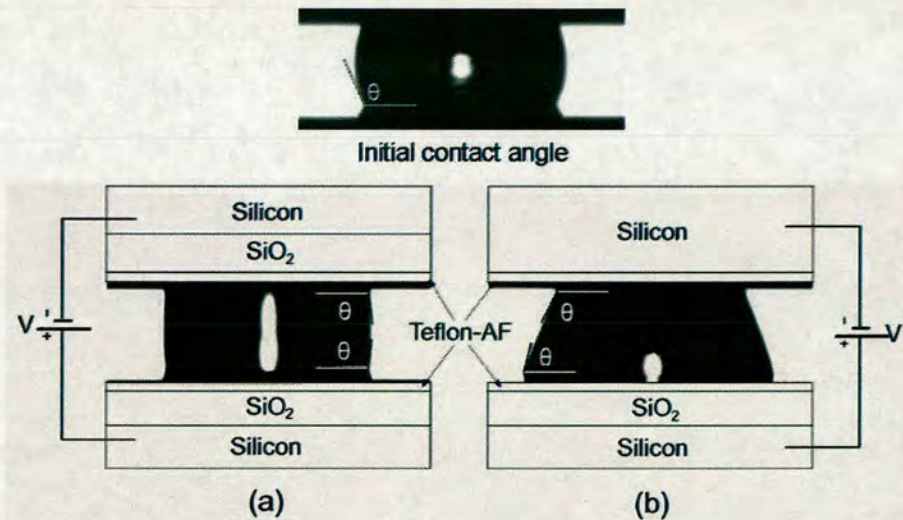
Figure 7.6: *Droplet contact angle changes in two plate EWOD systems when applied with same voltages (channel height = around 900mum) in (a) a configuration with both top and bottom electrodes covered by 500nm thermal SiO_2 insulating dielectric and 35nm Teflon-AF® aFP layers, and (b) a configuration with top electrode only covered by aFP layer.*

Ideally, if the ground electrode and the gap areas in the coplanar device with a ground line can

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be reduced to very close to zero, the critical driving voltage can approach that in the two plate systems. Such a system can facilitate a low voltage coplanar EWOD system, potentially having a critical driving voltage close to the 15V presented in Chapter **4**.

To enable full characterisation, a new test structure (shown in figure 7.7) architecture was designed to study the electrode area ratio effect and also quantify the performance improvement when the dielectric is removed from the ground electrode.
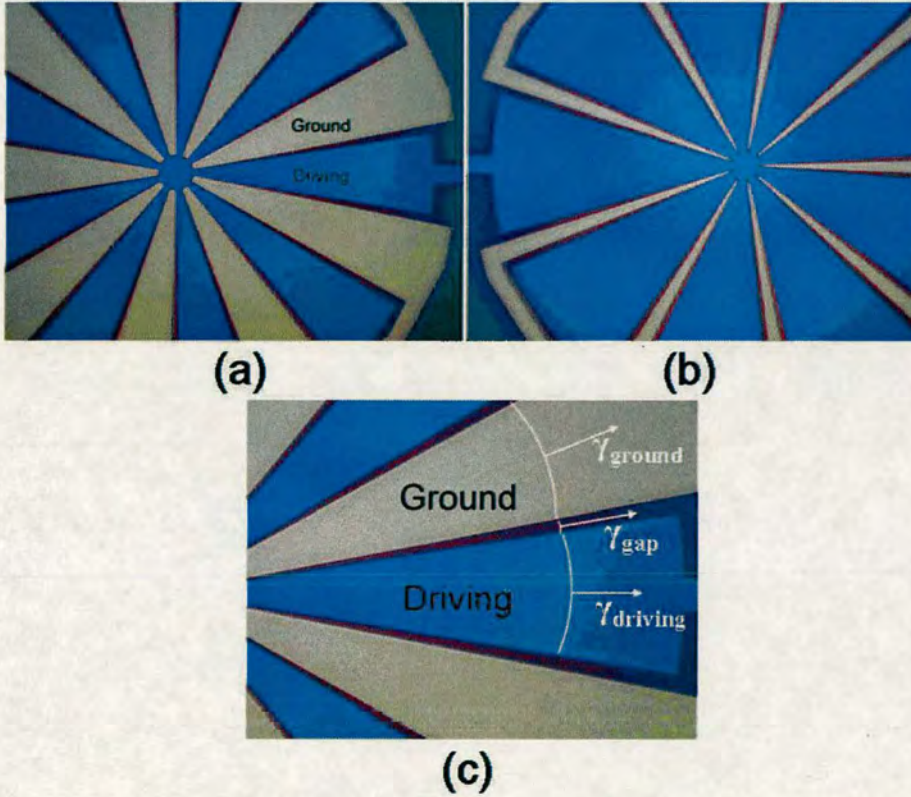
Figure 7.7: *EWOD coplanar test structure with: (a) Wedge shaped electrodes with identical sizes but no ground insulating coatings (driving electrode with Ta_2O_5 and CYTOP® - ground electrode has CYTOP® only); (b) Same type of dielectric coating as in (a), but with a different electrode area ratio ($A_{driving} : A_{ground} = 8 : 1$); (c) Surface tension distribution along the contact line (white curves show part of the droplet outline) when a droplet is wetting the surface.*

In this new design, anodic Ta_2O_5 was used as the insulating layer. The structure shown in fig. 7.7(a), is anodised by grounding the ground electrodes during the anodisation process. The creation of the dielectric using anodisation for coplanar devices with ground line structures is that Ta_2O_5 is only grown on the driving electrodes and so no lithography or etching is required

to remove unwanted dielectric on the ground electrodes.

Fig. 7.7(b) shows an example of a coplanar device with a ground line design with Ta_2O_5 coated driving electrodes that are larger than those shown in figure 7.7(a).

Changing the area ratio of both electrodes will result in a different surface tension distribution along the three phase contact line during wetting (fig. 7.7(c)). By looking for a maximum average surface tension change using the same voltage in equation (7.1), the optimum electrode ratio for low voltage coplanar EWOD can be determined. The shape of the droplet, when viewed in the horizontal plane, enabled the contact angle to be measured in the traditional manner.

Similar to the assumption made by Yi et al. [51], the changes in interfacial energy above each electrodes and the gap area were assumed to be averaged along the three-phase contact line. As discussed previously, the voltage drop across the aFP layers on the ground electrodes was neglected and so for the coplanar device with a ground line configuration, the relationship between the contact angle and applied voltage V can then be determined as:

$$\cos\theta(V) - \cos\theta(0) = -\frac{\varepsilon_r\varepsilon_0}{2\gamma_{lg}t}\frac{A_d}{A_t}V^2 \tag{7.4}$$

In this case A_d is the area of the driving electrode, and A_t is the total area (driving + ground electrode areas + the gap area). When A_d approaches A_t, the required driving voltage reduces to the levels reported for two-plate EWOD system.

For comparative studies, not only general coplanar test structures with gap ratios from 10% to 60%, but coplanar with ground line test structures with the electrode area ratios ($A_g : A_d$) from 1:1 to 1:8 (10% gap ratio)) were designed as well.

7.4 Sample fabrication and experiment results

7.4.1 Sample fabrication

The test structures were fabricated on Si substrates with a 0.5µm layer of SiO_2. A layer of 500nm tantalum was then sputtered and patterned to create the wedge shaped test electrodes. To prevent dielectric breakdown failure before contact angle saturation occurred [51], a thick
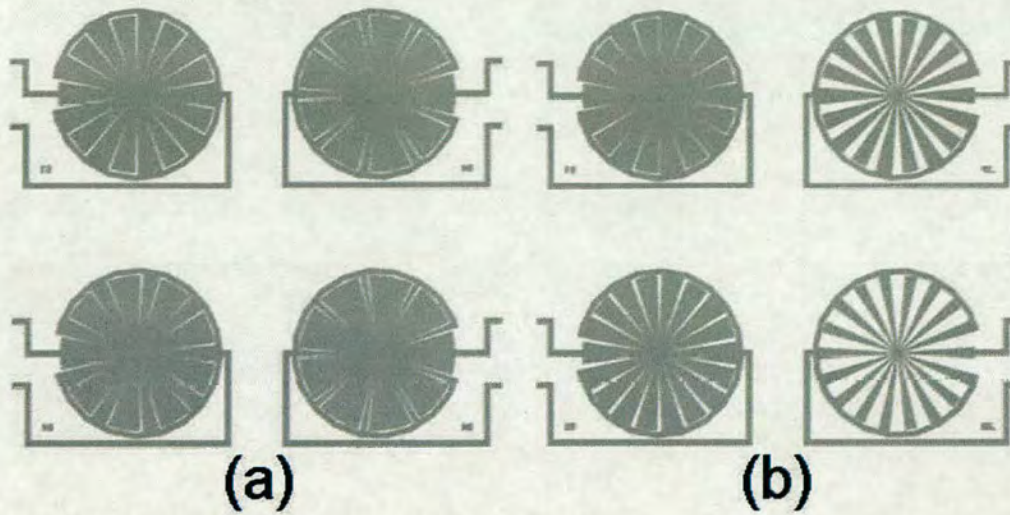
Figure 7.8: *(a) Electrode ratio test structures, with 1:1, 1:2, 1:5 and 1:8 electrodes area ratios (10% gap ratio). (b) Gap ratios test structures (10%, 20%, 40% and 60%) designed for comparative study.*

Ta$_2$O$_5$ layer (180nm) was anodised at 100V. A layer such as this can theoretically sustain 100V DC before breaking down (this voltage should have the same polarity as the anodisation).

Figure 7.9(a) shows the ground electrodes of a coplanar, with ground line, test structures which have not been anodised. For the general coplanar device, the ground electrodes in the devices were also anodised at the same voltage.
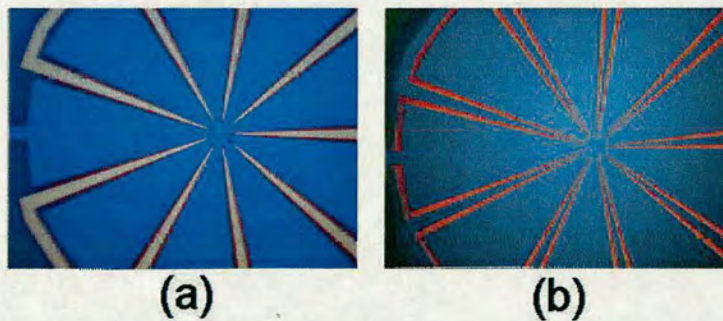
Figure 7.9: *Test structures with (a) Only driving electrode anodised for coplanar with ground line configuration tests. (b) Both electrodes anodised for general coplanar configuration tests (there was no electrode ratio change in these tests, this figure just illustrates how the different electrodes can be identified).*

After the anodisation, 35nm of CYTOP® was spin coated on the entire area to make the surface

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hydrophobic.

7.4.2 Experiments and results

The characterisation system used to study the contact angle as a function of applied voltage has been shown previously in figure 3.1. Additionally, the shape of the wetting droplet was observed from the top and side way with an angle, using the camera system in figure 3.3. Figure 7.5 shows the image obtained from both systems.

7.4.2.1 General coplanar configuration test and results

Performing contact angle as a function of voltage experiments on the general coplanar configuration test structures has demonstrated the advantages of anodic Ta_2O_5 over PECVD SiO_2. The thicker film, which can theoretically sustain 100V, enables the high-κ layer help the system achieved a critical voltage (voltage for changing the contact angle from 114° to 81°) of 35V DC with a gap ratio of 10%. This compares to the value of over 100V measured on samples with 300nm PECVD SiO_2 and 200nm CYTOP®. Moreover, there was no dielectric breakdown when voltages up to to 60V DC were applied, enabling the study of the saturation phenomenons on EWOD coplanar structures.

Figure 7.10 shows the contact angle changes follow the theoretical values given by equation (7.3) before saturation sets in. For structures with a 20% gap ratio, the critical driving voltage was around 40V DC. Due to early contact angle saturations, the contact angle of droplets operated on the 40% and 60% gap ratio test structures did not reach 81°. The reason will be discussed in the following discussion section.

7.4.2.2 Coplanar with ground line configuration results

Following the lower driving voltage results obtained in the general coplanar EWOD testing, coplanar with ground line configuration tests were performed. With the same dielectric coatings, the test structures with no Ta_2O_5 dielectric on the reference electrode and a 10% gap, $A_g:A_d = 1:1$ ($A_d:A_t = \sim1:2$), exhibited a reduced driving voltage of around 25V (figure 7.11). Changing the $A_g:A_d$ ratio to 1:8 ($A_d:A_t = \sim8:9$), reduces this voltage further to between 17 and 20V (figure 7.11). These results clearly indicated the driving voltage being reduced by half for the new coplanar architecture.
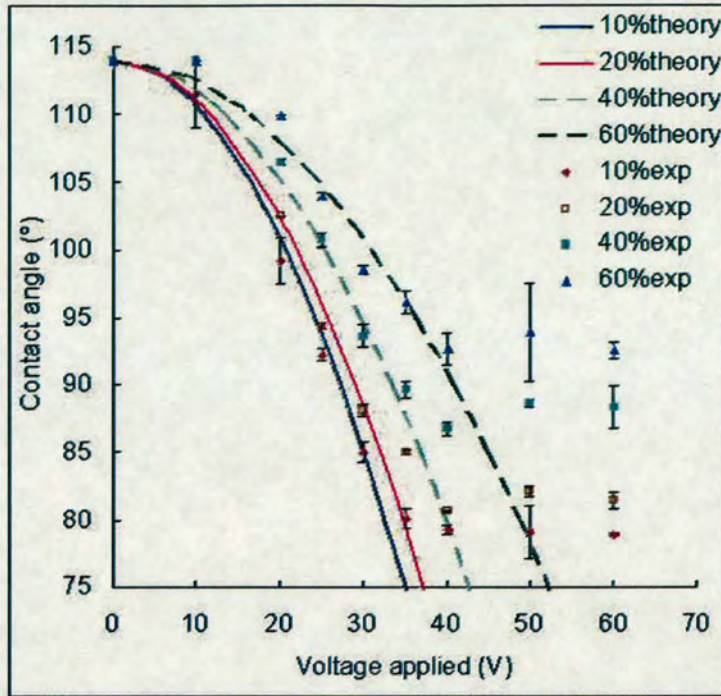
Figure 7.10: *Contact angle as a function of applied voltage for general coplanar configuration test structures as a function of gap ratio (10%, 20%, 40% and 60%), when $A_d:A_t$ = 1:2 ($A_d:A_g$ = 1:1);*

7.4.2.3 Comparison of Results

Figure 7.12 shows the relationship between contact angle change and applied voltage for EWOD coplanar electrodes. In terms of reducing the driving voltage, the coplanar with ground line design obviously has an advantage. By reducing the ground electrode size while increasing the driving electrode size, a lower critical voltage can be achieved. The lowest value achievable, which is roughly the same as the one achieved in two-plate configuration was around 15V.

7.4.3 Discussion

7.4.3.1 Early contact angle saturation in general coplanar configuration test

Before reaching 81°, early saturation was observed on the 40% and 60% gap ratio samples. This is due to the saturation of $\gamma_{driving}$ and γ_{ground}. Despite the different gap ratios, the voltage across the insulating and aFP dielectric layers on all the samples were same. Hence referring to the Lippmann's equation (2.11), $\gamma_{driving}$ and γ_{ground} on all the test structures consisting of the
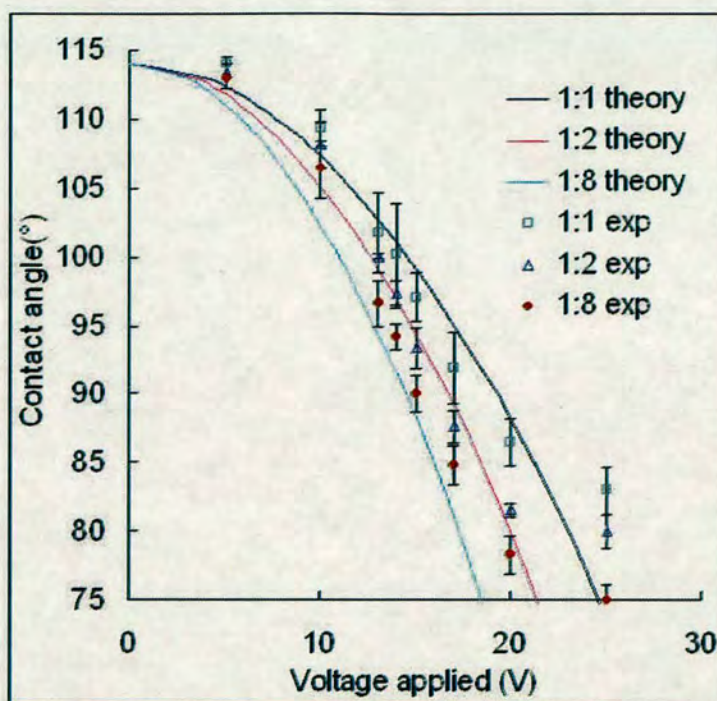
Figure 7.11: *Contact angle as a function of applied voltage for coplanar with ground line test structures as a function of A_g:A_d ($\frac{1}{1+A_d:A_t}$) ratio (from 1:1 to 1:8) with a 10% gap. (Since the results of electrode ratio of 1:5 were very close to those of ratio 1:8 , it was omitted for clairity.)*

same dielectric layers should reach the saturation value at the same applied voltage (in this case 35V to 40V). Since the wettability of the gap area did not change during the test, a larger area of unchanged γ_{gap} will result in an earlier overall contact angle change.

7.4.3.2 Surface tension distribution on coplanar EWOD structures

During the design evaluation test, the shapes of the droplets were observed not only from the side using the contact angle measurement system (figure 3.2), but also from the top using the droplet manipulation observation system (figure 3.3).

Figure 7.13 shows the top view of wetting droplets on the general coplanar test structure with different gap ratios. The liquid-solid contact line roughly followed a circular shape. Although there was no electrowetting force in the gap area, the Laplace pressure created by $\gamma_{driving}$ and γ_{ground} inside the droplet formed a γ_{gap}. When the gap ratio is relatively small, the assumption made previously that the contact angle measured can represent the average surface tension is
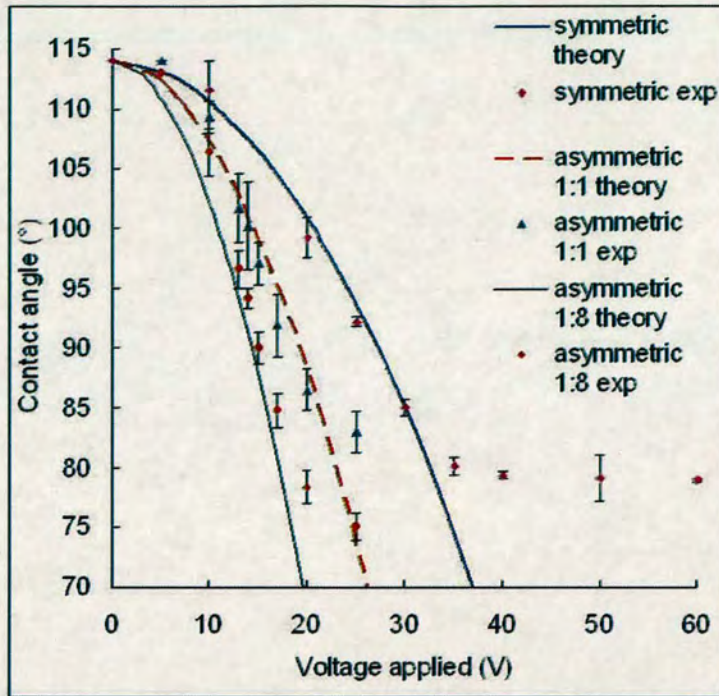
Figure 7.12: *Contact angle as a function of applied voltage for coplanar test structures with general coplanar configuration with 1:1 A_g:A_d ratio, and coplanar with ground line configuration with 1:8 coating A_g:A_d ratio (all gap ratios = 10%).*

still applicable. This can be confirmed in figure 7.10, where results of 10% to 40% gap ratio met the theoretical curve better than those of 60%. These results agreed with Wang et al.'s observation which showed the imbalance of electrowetting between identical dielectric surfaces with different electric field polarity [52].
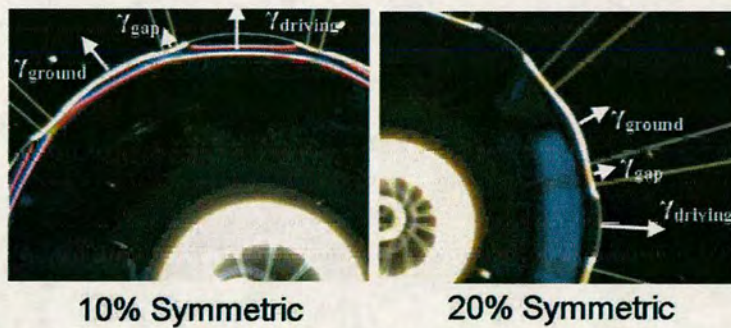
Figure 7.13: *Top view of wetting droplets on the general coplanar test structure with different gap ratios. (The nautilus shaped reflection is the droplet centre, while radial lines are the edge of the electrodes.)*

1:1 Asymmetric **1:2 Asymmetric**

1:5 Asymmetric
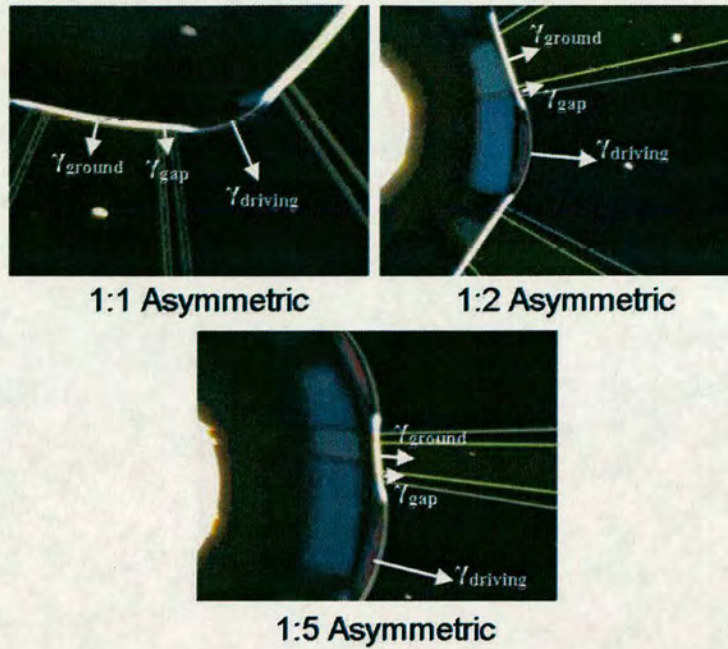
Figure 7.14: *Top view of wetting droplets on the general coplanar test structure with different gap ratios. (The reflection is the droplet centre, while radial lines are the edge of the electrodes.)*

In figure 7.14, the top view of wetting droplets on the coplanar with ground line test structure with different electrode ratios is shown. From this figure, the area with highest wettability was on the driving electrodes on both samples. The wetting on the ground electrodes and gap area could hardly be seen, due to the fact that most of the voltage applied was dropped across the dielectrics layers deposited on the driving electrodes.

Hence, γ_{gap} and γ_{ground} were both formed mainly by the Laplace pressure. When the electrode ratio $A_g:A_d$ was larger than 1:5, the liquid-solid contact line during wetting was not close to circular (clearly shown in figure 7.14). As a result, the contact angle measured can not accurately represent the average surface tension. This can be used to explain the slight mismatch of the experimental contact angle results in figure 7.11.

7.5 Droplet manipulation

7.5.1 Coplanar electrode array design

Based on the results from the coplanar test structures, coplanar EWOD electrode arrays were designed using parameters based upon the results obtained in the previous sections.
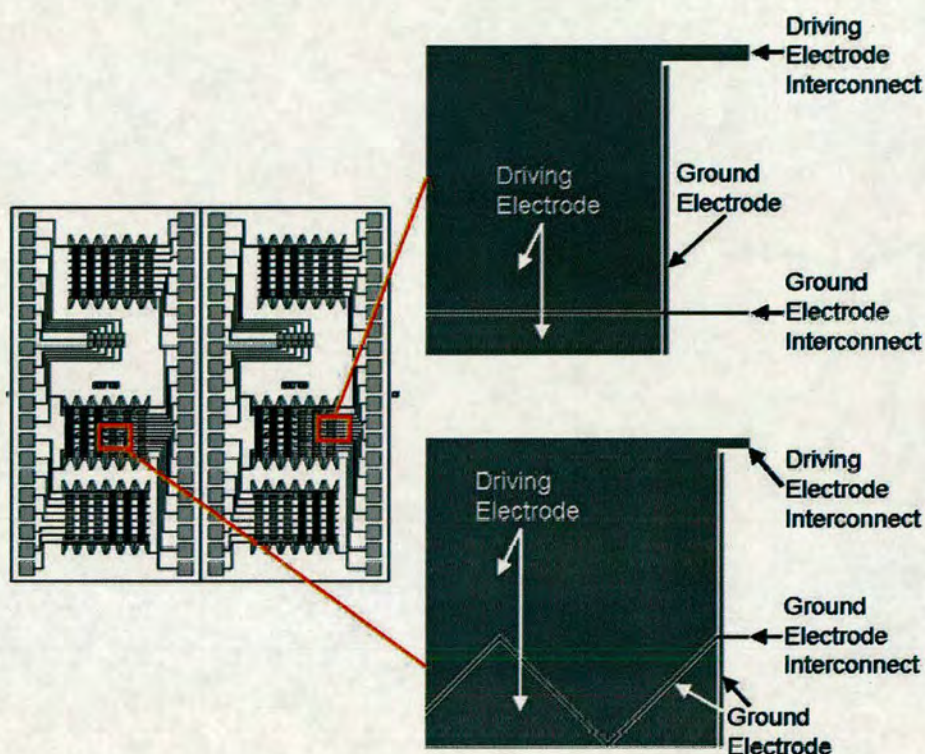
Figure 7.15: *The layout of the entire designed electrode arrays (left), and the close up view of the electrode area (right).*

Figure 7.15 shows EWOD electrode arrays arranged using coplanar with ground line configuration. For process simplicity, a passive single metal layer structure was chosen to evaluate the low voltage coplanar EWOD design. The close up view of the electrode layout shows that the ground electrodes were designed to surround the driving electrode and were placed in the gap between the driving electrodes. Since interconnects are on the same layer as the ground electrode in single metal layer structures, the driving electrodes cannot be completely surrounded as shown in figure 7.16(a) [20]. An alternative is shown in figure 7.16(b). Ground electrodes were routed in the gaps between the electrodes and interconnects. Each ground electrode was then connected to separate bond pads on the structures.

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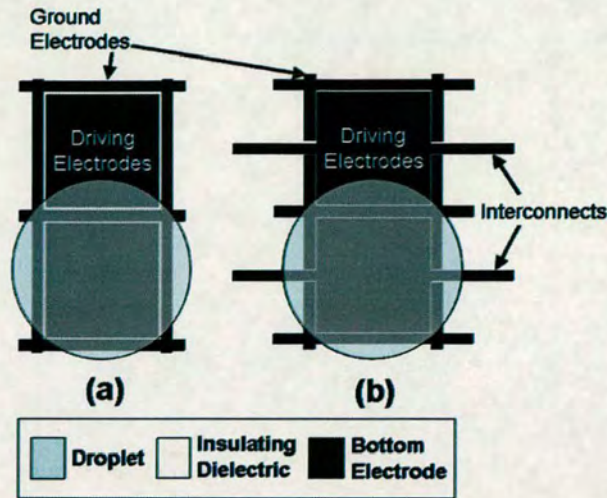
Figure 7.16: *Diagram shows coplanar with ground line EWOD electrode and interconnect arrangement suggestions in (a) multi-level metallisation structures [20], and (b) single metal layer structures.*

For fabricating this structure, tantalum was sputtered and patterned as 5µm wide metal tracks for the ground electrodes, and 1mm × 1mm squares for the driving electrodes. The gap between the driving electrodes and ground electrodes were 3µm. The driving electrodes were then anodised at 50V to form a 95nm anodic Ta_2O_5 insulating layer. After 16nm Teflon-AF® was spin coated, the droplet could be manipulated at a speed of ~16 mm sec^{-1} with applied voltage as low as 15V (figure 7.17).

7.6 Conclusions

In this chapter, an improved coplanar EWOD test structure has been presented. It has been modified for characterising low voltage coplanar EWOD device architectures and can be used to characterise electrode gap dimensions and the electrode area ratio. This characterisation was an important component in the development of a new EWOD architecture that reduced the droplet driving voltage.

Characterising the electrode gap dimensions in the general coplanar configuration test structures using anodic Ta_2O_5 for comparison with the work in [51], the significantly reduced critical driving voltage (reduced from around 100V to around 40V) shows the advantages of using Ta_2O_5 as a dielectric insulation in the coplanar EWOD structures. Changing the electrode ratio in the coplanar with ground line coplanar configuration test helped an optimum design that
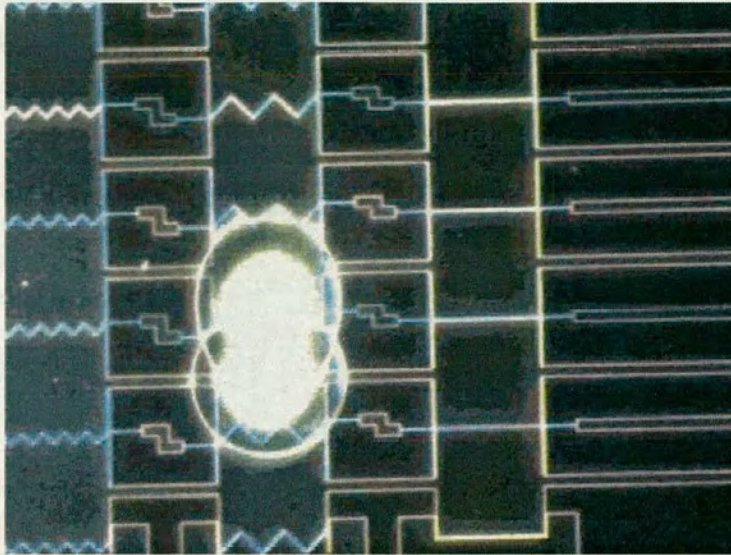
Figure 7.17: *Still image of a droplet moving across two $1 \times 1mm$ electrodes in one frame (frame rate 16 frame sec^{-1}, on a coplanar with ground line EWOD electrode array using 15V.*

reduced the critical voltage to less than 20V to be found, while having the same dielectric layer composition.

Meanwhile, other phenomena such as the contact angle saturation and the surface tension distribution during the coplanar EWOD testing have been discussed. The observed imbalanced electrowetting relates to the charging polarity on the dielectric layers and is consistent with the explanation presented in Wang et al.'s asymmetric EWOD work [52].

Finally, the successful low voltage coplanar EWOD droplet manipulation has been demonstrated as a result of the design and process optimisation.

Chapter 8
Examples of EWOD Applications

This chapter gives two examples of the EWOD devices that take advantage of the technologies developed in previous chapters.

8.1 An EWOD digital droplet dispenser

EWOD microfluidic systems have started to show their great suitability for lab-on-a-chip in recent years [20]. Based on the manipulation of nanolitre scale droplets, many conventional chemical, medical and biological lab functions can be achieved now using digital microfluidic chips. However, there are some applications requiring further operating stages following the EWOD manipulation. Hence, droplet output devices have been developed, such as a soft-printing system based on EWOD technology [78].

8.1.1 Droplet dispenser for electrospray

For this application, different technologies were integrated to design and build a bio-chemical MEMS system applied to proteomics. One of the objects was to generate pico-litre solution samples for measurement in a mass spectrometer.

Figure 8.1 shows that an EWOD device was chosen for on chip nanolitre sample preparation (e.g. sample dispensing, mixing), and to be integrated with electrospray technology for breaking up the output samples into picolitre droplets.

8.1.2 Droplet output from a capillary fibre

The liquid input and droplet creation using EWOD has been discussed in the previous chapters. The major issue remaining to be solved for this application was the output method.
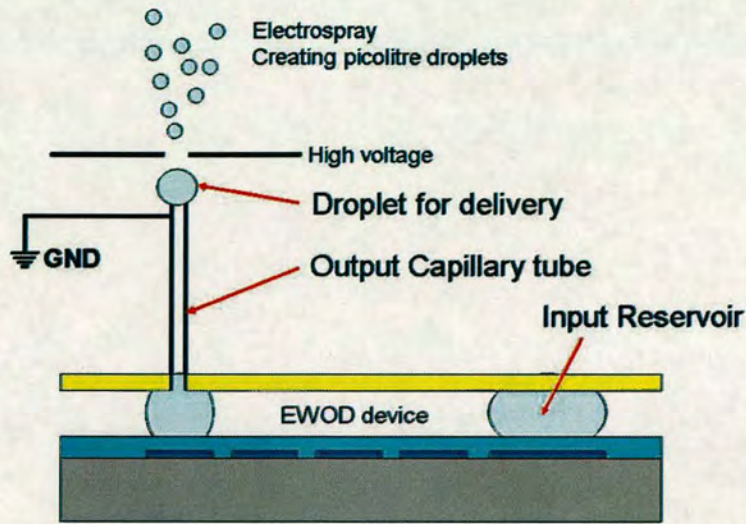
Figure 8.1: *The system design overview. Droplets were created from the input reservoir using EWOD manipulation. After the on chip sample preparation, the nanolitre droplet was output into an electrospray system. The output droplet was sprayed into a mass spectrometer in picolitre size.*

8.1.2.1 Hydrostatic imbalance

Yi et al. firstly reported an EWOD soft-printing device ejecting a droplet out of a 400μm diameter nozzle in a glass top plate. The ejection of the liquid droplet was achieved by manipulation of device geometries. The geometry of this device was to generate a pressure imbalance for droplet ejection at the nozzle, related to the original Young-Laplace equation [78]:

$$\Delta P = \gamma_{LG}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{8.1}$$

where R_1 and R_2 are the interface principal radii of curvature of a liquid-gas surface (figure 8.2), ΔP is the pressure difference across the surface and γ_{LG} is the liquid-gas surface tension [93].

Figure 8.3 shows the pressures on a droplet sandwiched between the two EWOD plates using the Young-Laplace model. Since the droplet and the environment medium such as air in this case are immiscible, the meniscus (radius R_{ch}) shown in fig. 8.3(a) at the the interface creates a pressure P_{ch}, while the meniscus (radius R_{liq}) shown in fig. 8.3(b) creates a pressure P_{liq}. Referring to Young-Laplace equation (8.1), the pressure on the top surface of the droplet will

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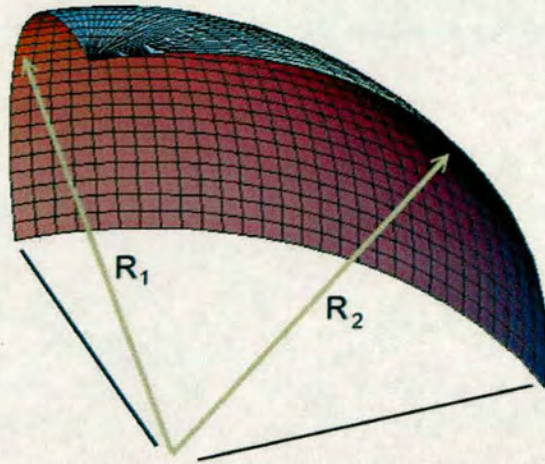
Figure 8.2: *A curved liquid-gas surface with the principal radii of curvature R_1 and R_2 [93]*

be:

$$P_{top} = \gamma_{LG}\left(-\frac{1}{R_{ch}} + \frac{1}{R_{liq}}\right) \tag{8.2}$$

From chapter 2, it was shown that here the gravitational force is negligible.

(a)   **(b)**
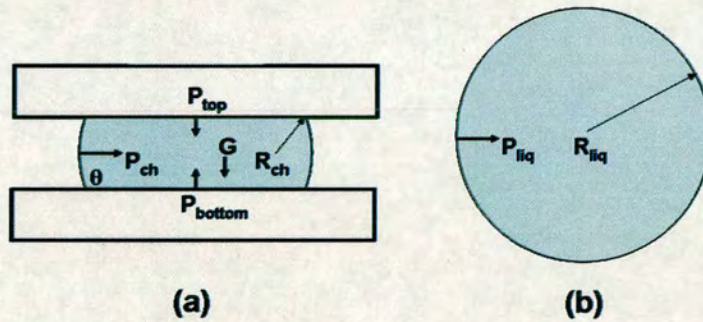
Figure 8.3: *Pressures on a droplet sandwiched between two EWOD plates. (a) Cross section view. (b)Top view.*

In Yi's design, when the droplet sandwiched between two plates was transported to the nozzle region, the pressure difference between the liquid-gas surface inside the hydrophobic EWOD channel and the exposed droplet surface at the nozzle was created by designing the channel height to be much smaller than the nozzle diameter. This pressure difference was greater than the force due to gravity and hence the droplet (around 100nL) was completely ejected [78].

Figure 8.4 shows a similar device to Yi's design for droplet output through capillary fibres

connected to an electrospray system. The proposed design enables liquid input from other fluidic sources via an input capillary fibre, allowing the creation and manipulation of droplets before the output stage.
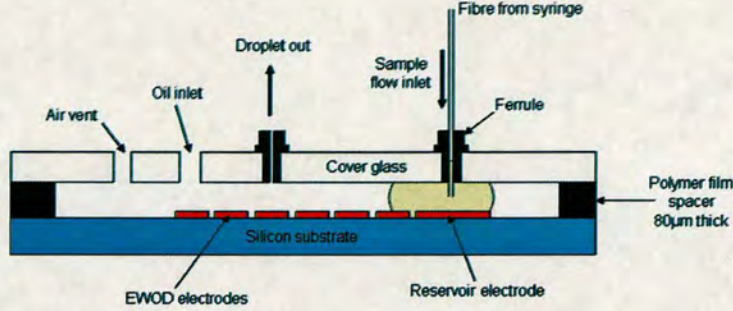
Figure 8.4: *The design of a EWOD micro dispenser for droplet creation, manipulation and output. The droplet samples can be sealed in oil or in air environment according to the application requirements.*

Figure 8.5(a) shows the cross-section of the EWOD output device designed for this project. The output port was created on the EWOD top plate, with the capillary attached through a ferrule. When the droplet was transported under the port, a pressure differential was created between P_{ch} (pressure at the liquid-gas interface in the channel) and P_{cap} (pressure at the interface in the capillary) causing the droplet to move into and along the capillary until it was ejected from the opposite end (fig. 8.5(b)).

The initial liquid level rising in the capillary shown in figure 8.5(a) can be explained in this case by calculating the pressure difference using equation (8.3) that is developed from (8.1):

$$\Delta P = P_{ch} - P_{cap} = \gamma_{LG}\left(-\frac{2cos\theta_2}{h} + \frac{1}{R_{liq}}\right) - \gamma_{LG}\left(\frac{2cos\theta_1}{D} + \frac{2}{D}\right) \qquad (8.3)$$

where θ_2 is the contact angle in the hydrophobic channel (in this case around 120°), θ_1 is the contact angle <90° in the capillary, h is the EWOD channel height, R_{liq} is the radius of the droplet inside the channel (fig. 8.5(c)) and D is the capillary diameter. The capillary fibres used in this case were all hydrophilic, hence the ΔP was always positive at this point. The liquid level therefore rose until the droplet emerged from the top of the capillary (fig. 8.5(b)).

Once the droplet emerged from the capillary top, it bulged in the same manner reported in [78]

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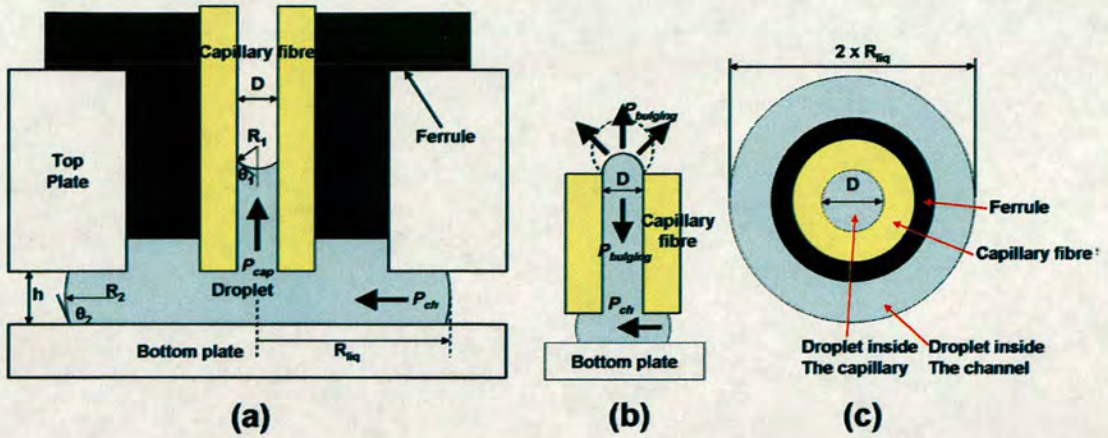
Figure 8.5: *Droplet output from a EWOD micro dispenser (figures are not in the same scale). (a) Cross-section of the designed EWOD device output port, all showing the droplet entering the capillary from the EWOD channel. (b) Bulging of the droplet from the other end of the capillary. (c) Top view of the capillary output port.*

(fig. 8.5(b)). The pressure difference could then be calculated using equation (8.4):

$$\Delta P = P_{ch} - P_{bulging} \geq \gamma_{LG}\left(-\frac{2cos\theta_2}{h} + \frac{1}{R_{liq}} - \frac{4}{D}\right) \qquad (8.4)$$

The bulging pressure $P_{bulging}$ reached its largest value ($4/D$) when the radius of curvature was the same as the internal radius of the capillary ($D/2$). Therefore if the EWOD channel height h was designed to be much smaller then the capillary internal radius, the droplet would be completely ejected from the capillary.

8.1.3 Device fabrication

Figure 8.6 shows the designed EWOD electrode array. Each microscope slide sized chip contains two dispensing arrays.

For the fabrication of the EWOD array, 95nm anodic Ta_2O_5 was deposited on the $1 \times 1mm$ tantalum electrodes as the insulating dielectric layer. A thickness of 16nm of Teflon-AF® was spin coated on the anodic Ta_2O_5 and the ITO top glass plate. The channel height between the two EWOD plates was 80μm. Two diameters of capillary, 170μm and 50μm respectively, were chosen to make a comparison.
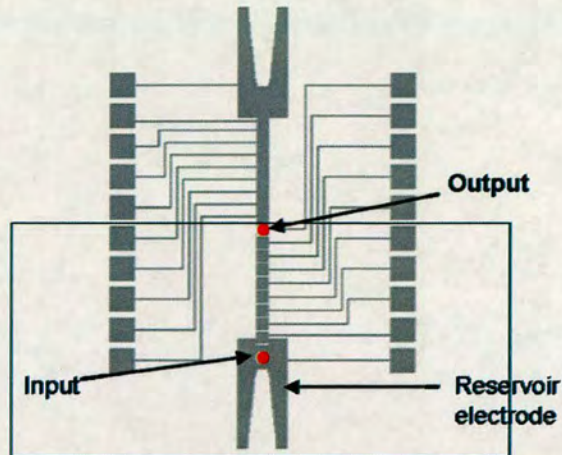
Figure 8.6: *Design of a microscope slide size EWOD dispenser chip. The boxed area is one of the two dispensing electrode arrays. Red dots are the position where the input and output capillaries were located.*

8.1.4 Test and result

During the tests using 15V DC operating voltage, droplets were created from the reservoir electrode and transported directly to the output capillary. The volumes of the droplets were controlled to be around 400nl by simultaneously operating five $1mm^2$ electrodes in an $80\mu m$ high channel. Figure 8.7 shows that two droplets were successfully and sequentially output from the $170\mu m$ internal diameter capillary. For the capillary with $50\mu m$ internal diameter, the droplet remained in the capillary, despite the adequate volume still in the channel, due to the insufficient pressure difference.

8.1.5 Conclusion and future work related to the electrospray system

By designing the channel height in the two-plate EWOD system to be much smaller than the internal diameter of the capillary, droplet output was achieved by operating the EWOD microdispenser device at 15V DC. The capillary with a smaller internal diameter than this channel height did not result in the droplet bulging out of it. The next step for this project will be device integration with the electrospray system.
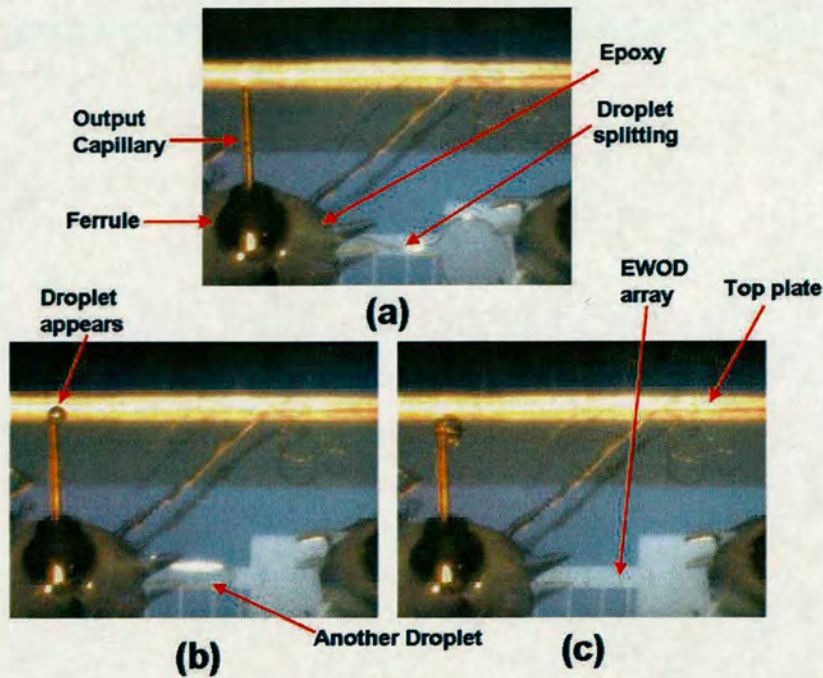
Figure 8.7: *Three sequential images showing droplet output from a capillary with 170μm internal diameter out of an EWOD dispenser. (a) A ~400nl droplet was created from the reservoir. (b) Another 400nl droplet was created while the first droplet was bulging from the top of the capillary. (c) Both droplets were output from the capillary.*

8.2 A MEMS pondskater

Distributed tiny robots such as smart dust [112] have long been postulated for the MEMS field. Towards that goal, sub-centimeter sized MEMS devices have already demonstrated the capability to walk [113] and fly [114]. However, to the author's knowledge swimming MEMS devices at such a scale have not yet been successfully fabricated. Such devices have the potential to open a large number of applications such as pollution sensing and purification. In the macro robotics field, a pondskater is a hot topic but reported devices are still centimeter sized.

For building a sub-centimeter swimming robot, several issues need to be considered. When the sizes of microsystems scale down to millimeters, molecular adhesion forces (e.g. surface tension) start to dominate rather than gravitational force [30]. At this stage, using micrometer scale light-weight movable parts e.g. fans and screw propellers to oppose solid-liquid surface tension becomes increasingly difficult. Power consumption control is also crucial due to the difficulties of integrating large power transfer devices in micro systems.

EWOD technology may be considered due to its ability to move objects using surface tension force [75], and low power consumption when using anodic Ta_2O_5 enabled low voltage operation. Without any movable mechanical structures, a millimeter size pond skater device floating on the water surface and based on EWOD technology has been developed.

8.2.1 Device design

Figure 8.8 shows that the required propulsion force can be created by reversing the 'normal' configuration of water droplets in air. In this device, force was created by bubbles of air escaping and the floating pond skater device moved forward while ejecting bubbles backwards. Ejection of a bubble results in the same volume of water being displaced in the same direction. If the mass of this amount of water is comparable with the pondskater mass, counter movement velocity will be observed.
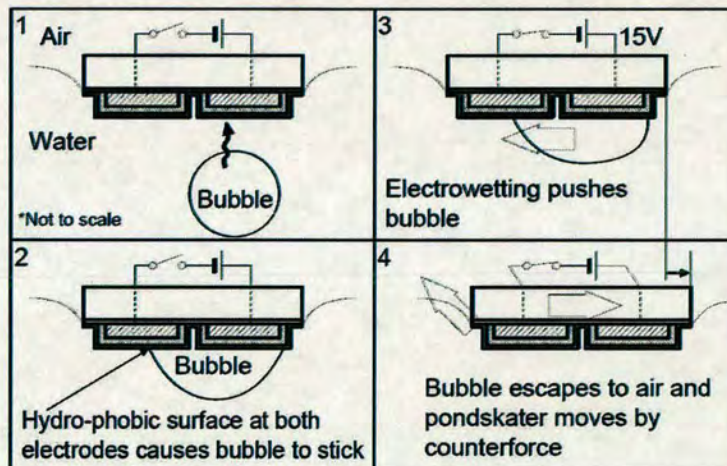
Figure 8.8: *Working principle of a EWOD MEMS pondskater. (1) The chip was placed inverted on the water surface. (2) Bubbles were dispensed from a micropipette and remained on the hydrophobic surface, (3) and low-voltage EWOD can eject the bubble to air so that (4) pondskater moves by counterforce.*

Figure 8.9 shows the first device which was composed of two 6.8mm×3mm adjacent electrodes having a 4µm gap in between. The hydro-phobic surface is air-philic [115] so that air bubbles dispensed from a micropipette will stick on the surface. When voltage was applied across the two electrodes, the surface of the positive electrode changes to hydrophilic and is thus airphobic. The air bubble was then pushed to the other end of the chip. It removed itself from the device when it reached the edge of the chip. The rapid bubble movement generated a

counterforce that moved the device forward.
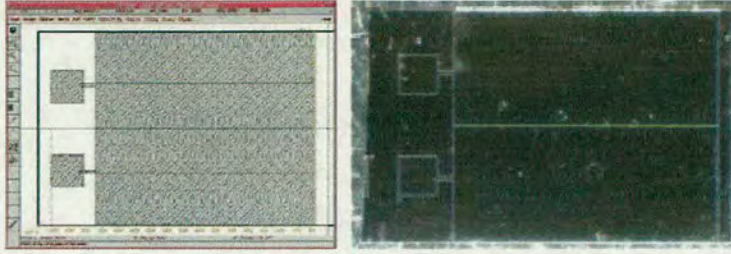
Figure 8.9: *Design layout (right) and the fabricated EWOD pondskater device (left).*

8.2.2 Sample fabrication

Figure 8.10 shows how low voltage EWOD technology using anodic Ta_2O_5 was applied to the fabrication. Tantalum was first sputtered onto the surface. Since the gap between two electrodes was only 4μm, anisotropic reactive ion etching using $SiCl_4$ plasma was performed for patterning the tantalum instead of the isotropic etchant XeF_2. The tantalum electrodes were then anodised, followed by Teflon-AF® spin coating and 330°C curing.

A 2cm gold wire (25μm diameter) was glued to each pad using conductive-epoxy, with the other end attached to a copper wire spring (100μm diameter) . The bond pads and the gold wires were then dip-coated with cured CYTOP to prevent short circuiting in the water.
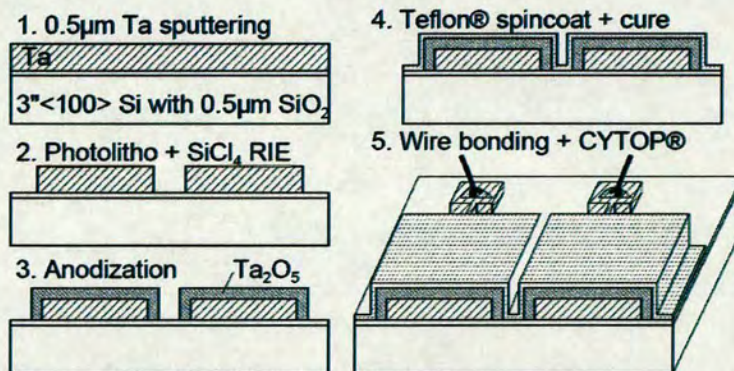
Figure 8.10: *Fabrication processes. (1) Tantalum sputtering. (2) RIE patterning of tantalum. (3) Anodisation for depositing anodic Ta_2O_5. (4) Teflon-AF® spin coating and cure. (5) Wire bonding using conductive epoxy and dip coating CYTOP® for electrical insulation.*

8.2.3 Experiments and result

The electrodes were flipped and placed on the DI water surface contained in a beaker(fig. 8.11). Copper wires were fixed to the stage and the wall of the beaker with the thin gold wires suspending in the air.
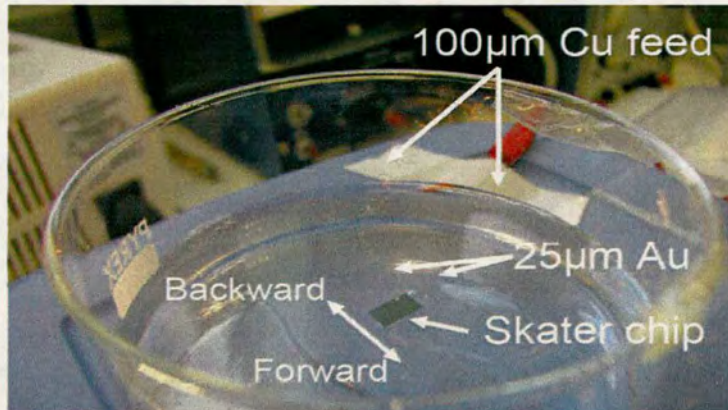
Figure 8.11: *EWOD pondskater experiment setup. The pondskater chip held by gold wires was floating on the DI water surface contained in a beaker. The movement of this chip was recorded by the microfluidic observation system presented in Chapter 3 and a digital video camera.*

The gold + copper interconnect worked as a pull-back spring so that back-and-forth oscillation was observed instead of permanent forward movement, which was clear evidence of EWOD bubble jet propulsion. The wetting and bubble jet ejection occurs in less than 100 milliseconds ($\leq$3 frames). The mass of pondskater chip was around 40mg (0.38mm×6mm×8mm silicon chip), while the volume of water displaced during bubble injection was estimated to be about 60mg (from size of the bubble, around 6µl). Calculation results following rules of the conservation of momentum predicted that the velocity of the pondskater would be a few millimeters per second.

Fig. 8.12 and 8.13 show two measurement results using different recording cameras. They confirm the speed to be around $7-8\text{mmsec}^{-1}$.

8.2.4 Conclusion

The first EWOD propulsion of a pond-skater was demonstrated. By ejecting a 6µl air bubble at the rear, the 40mg EWOD chip floating on DI water surface successfully moved forward with a
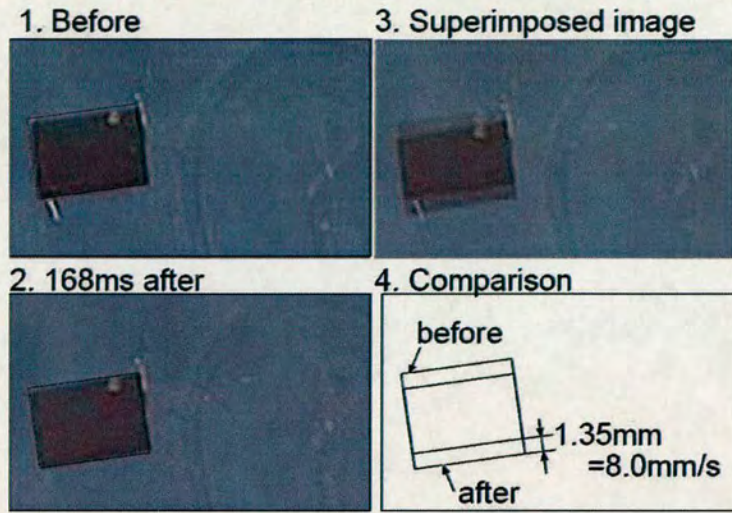
Figure 8.12: *Pond-skating demonstration. The chip moves by 1.35mm in 0.168 seconds (8mm·sec⁻¹). Note that the chip is stopped by a 25μm gold+100μm copper spring. Continuous movement would be possible without a spring.*
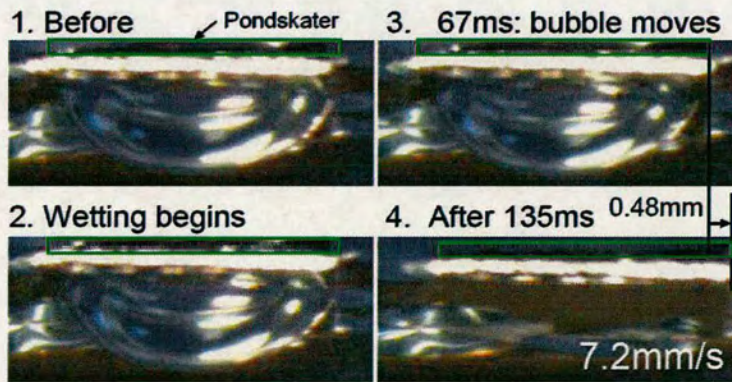
Figure 8.13: *Pond-skating demonstration using a high-magnification observation system described in Chapter 3. The pondskater chip was outlined with the green box. By comparing the reflection on the bubble surface, the bubble movement caused by the wetting water moving from the right hand side can be seen. When the bubble was released into the air, a displacement of the chip was observed.*

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speed of 7 to 8mmsec^{-1}. This device so far requires an external air bubble source and is held by the control wires. Hence continuous propulsion and total automation have not been achieved yet.

For future work, the wire related issues can be solved by integrating the pondskater with a power source such as solar cells or wireless power transforming devices as reported in [116]. For the bubble generation, the automation can be achieved using an on-chip electrochemical reaction, such as electrolysis of the water. However, this method would waste considerable power. Figure 8.14 shows an alternative to bubble injection. The device could be propelled by causing the bubble shape and position to change. A "breaststroke" type is being considered.
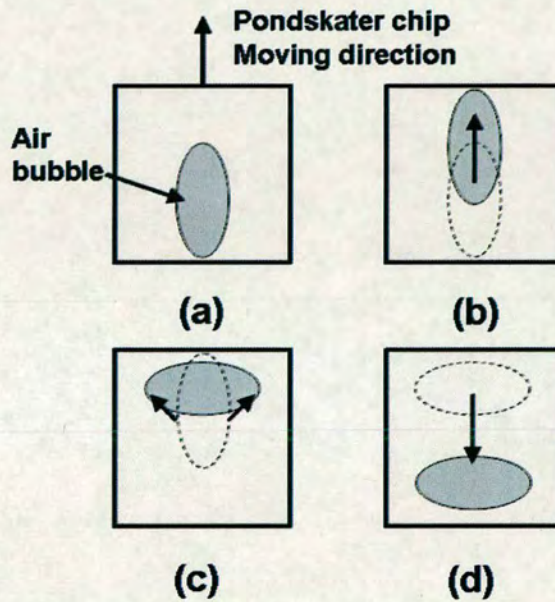
Figure 8.14: *Pondskater propelled in a "breaststroke" type bubble motion. (a) An air bubble sticking at back of the chip, with a long and narrow shape. (b) The air bubble moving slowly in the same direction as the pondskater. (c) Shape changed to wide and short. (d) The shape changed bubble moving rapidly to the back creating a propulsion force. This process can be repeated many times without the need to replacing the air bubble.*

Chapter 9
Summary and Conclusion

9.1 Summary

In this thesis EWOD technology has been reviewed and compared with other digital microfluidic technologies such as dielectrophoresis (DEP) and surface acoustic wave (SAW). EWOD uses surface tension as its driving force and when the dominance of this element in submillimeter microfluidic size systems is considered, this approach clearly has some advantages. The developments related to the present status of EWOD systems has been presented, and important issues, such as a driving voltage and dielectric material, droplet manipulation schema, system design, and contact angle saturation, identified.

The process and design evaluation presented in chapter 3 simply focused on fabricating a functional system on a silicon wafer to provide a benchmark (most of the early reported EWOD systems used chrome mask technology). The first issue to be addressed was fabrication process compatibility and suitability of various process steps for the fabrication of EWOD devices. The use of aluminium restricts the temperature of any following processes to less than 435 degC. The most typically used EWOD dielectric materials, such as furnace based LPCVD dielectrics, have a high deposition temperature which is well above that permitted. However, PECVD dielectrics are commonly used with aluminium metallisation in the CMOS industry. Unfortunately, in EWOD technology the existence of permeation paths in the insulator, which are easily avoided by suitable processing in CMOS technology. They can cause reliability issues, since electrolysis failure occurs when the liquid penetrates the dielectric effectively short-circuits the electrodes. The availability of pinhole free high quality uniform Parylene-C coatings effectively solved this problem enabling robust contact angle change to be achieved. This enable the demonstration of droplet manipulation on a single level aluminium electrode array.

After having developed the benchmark processes, two development theme were addressed. The voltages required to drive the benchmark electrode arrays were between 45 and 100V. While 100V CMOS processes are available these voltage levels bring in issues such as control circuitry design, future system integration and device portability. Low voltage EWOD is obviously

attractive and such technologies have been reported. To reduce the driving voltage down to 14V are the use of high-κ dielectric materials have been employed as the insulating dielectric layer. However, most of the reported low voltage EWOD fabrication processes required temperatures above 500° which makes integration with CMOS and aluminium electrodes impossible. Some of the dielectrics used also had other undesired disadvantages such as a rough surface. The development of anodic Ta_2O_5 technology tackled the aluminium compatibility issues since it is a room temperature process, while also having a high dielectric constant, high dielectric strength and high film quality. All of these attributes make it eminently suitable as a low voltage EWOD candidate. Moreover, the smooth surface enables ultra-thin aFP layers to be spin-coated uniformly. The relationship between driving voltage and the thickness of aFP layers was hence enabled to be experimentally addressed. By using an ultra thin aFP layer combined with CMOS compatible anodic Ta_2O_5, the driving voltage was successfully lowered to less than 15V.

Another objective addressed in chapter 5 is development of the design and technology for larger EWOD electrode array to take full advantage of the digital microfluidic architecture, such as greater system flexibility, multifunctionality, a higher sample throughput and higher resolution of sample volumes. Electrode arrays require a multilevel metallisation processes to enable electrodes in the centre of the passive electrode array to be addressed. The first device fabricated was an aluminium-aluminium two metal layer structure, with EWOD electrodes on top layer with the interconnects underneath providing the electrical connectivity. With the electrodes coated with Parylene-C and Teflon-AF®, droplet manipulation was demonstrated on a 5 × 8 EWOD electrode array used an applied DC voltage of 50V. The successful low voltage EWOD anodic Ta_2O_5 technology was then integrated with the multi-level-metallisation electrode array design using tantalum as the electrode material and aluminium and the underlying interconnect material. This approach reduced the voltage required for droplet manipulation to 15V. A sample volume controllable EWOD droplet dispensing device based on this technology was demonstrated as introducing droplets to the system is an essential component of any EWOD system.

One of the key objectives of this work was to develop the underpinning processes required to integrate EWOD technology with CMOS drive circuitry. A lack of electronic based addressing circuitry requires each electrodes to have its own bond pad and interconnect. When the electrode array is scaled up to the level other digital microfluidic devices such as the DEP system presented in [22], which has more than 1,000 electrodes, the passive scheme becomes

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extremely difficult to implement due to the packaging issues. On-chip row and column addressing has already been applied in array technologies such as displays and image sensors. Since the EWOD fabrication processing in this project was based on aluminium interconnects (or low temperature processes) typically used in standard CMOS fabrication, in theory makes the integration straightforward. The of the first integrated EWOD-CMOS system was accomplished in an economical and simple way. A backplane CMOS chip with on-chip electrode addressing function was fabricated on a multi-project wafer in a commercial foundry. After a few post-process steps, droplets were successfully manipulated on the active EWOD chip. However, because chip postprocessing was required this limited the process steps and the quality of the process steps that it was possible to implement. In addition, the CMOS process used did not have sufficient metal layers for screening and the chip suffered from some parasitic transistor action. The lower driving voltages achieved in this work provide access to CMOS processes with more metal layers and obviously processing on wafers will enable high quality lithography to be performed.

The coplanar EWOD system which does not require a top plate as a ground electrode, has been reported recently in the literature. However, to the author's knowledge, the low voltage devices that exist in the two-plate EWOD systems have not been replicated in coplanar systems. There are several droplet driving schemes in the coplanar Existing test structures, could only to characterise one type of coplanar system, and a new set of test structures was designed for studying the coplanar driving voltage and electrode design. Based upon the characterisation results, a new architecture was designed and fabricated using anodic Ta_2O_5 technology which achieved a 15V rapid droplet movement.

After the progress in developing low voltage passive and active EWOD devices integrated with CMOS circuitry, potential applications were examined. The low voltage two-plate EWOD system was firstly applied to implement a digital nanolitre dispenser and sample preparation stage to be integrated with electrospray technology for injecting picolitre size samples into a mass spectrometer.

A low voltage coplanar electrode array was used in a micro swimming robot or "pondskater". It was believed this was the first active swimming robot skating on the surface by generating its own force. Although many issues remain before achieving a continuous movement, using surface tension driven microrobots is believed to be valuable.

9.2 Conclusions

During the the course of research it became clear that the PECVD dielectrics being deposited by the STS system, while suitable for microelectronic applications, were not suitable for EWOD applications. Unfortunately, water permeated the dielectric resulting in the electrode metal being attacked. To solve this two approaches were successfully implemented:

1. PECVD oxide was replaced with Parylene-C.

2. A thin coating of Parylene was deposited on the PECVD oxide.

While it is believed Parylene has been used previously [36] in EWOD technology this is not a commonly used dielectric, and for this work high yielding pinhole free layers were achieved. Both Parylene and silicon dioxide have relatively low dielectric constants, which result in high EWOD driving voltages. The lowest achieved in this work were 45V and 27V volts respectively.

Clearly, if more standard CMOS technology is to be integrated with EWOD then there is good reason to develop a dielectric system that has has a lower EWOD driving voltage. Tantalum pentoxide was identified as a dielectric that would both be high yielding and with its high dielectric constant (8-25) would enable lower driving voltages to be achieved. This was successfully implemented and provided the underlying technology to enable the lowest reported driving voltage with a low temperature deposition dielectric (13V). In addition this was the first reported implementation of anodised Ta_2O_5 in an EWOD device. This innovation provides the underpinning technology that enables reliable operation and the basis for low voltage EWOD operation.

One of the key characteristics of anodised tantalum Ta_2O_5 is that it is are impervious to fluid ingress. The importance of the above characteristic enables thinner aFP layers to be employed which facilitates low driving voltages. The the ability to reduce the aFP thickness is specifically identified in chapter 4, which appears to have been overlooked by other research teams who have focused on the insulating dielectric permittivity. Being able to thin the aFP to 16nm was the key to obtaining the 13V driving voltage.

The thesis also reports the first example of an active EWOD device being driven by an underlying CMOS backplane. It allows the EWOD system to have a much higher electrode numbers

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without suffering the limitation related to the requirement for a large number of interconnects and bond pads. This development also facilitates the addition of on-chip sensing functions such as in situ sample diagnosis and droplet position detection. A simple post-process which results in a high driving voltage was chosen at the time for the EWOD-CMOS sample fabrication. Using the technology reported in this thesis a low voltage CMOS EWOD system is can now be easily developed in the future.

The coplanar EWOD test structure demonstrated in chapter 7 has helped to characterise the technology to help determine and optimise both the dielectric selection and electrode arrangement related to minimising the driving voltage. From these results, it is clear that a low voltage EWOD system not only requires a small gap between electrodes [51], but also relies on:

1. Using high-κ insulating dielectric material and ultra thin aFP hydrophobic layer.

2. No insulating layer on ground electrodes.

3. Minimisation of the ground to driving electrode area ratio.

9.3 Future work

One future development that the technology reported in this thesis has enabled is the integration of EWOD with a low voltage CMOS backplane using foundry post-processing. To do this the passivation layer on the backplane chip needs to be removed as without its removal this will result in a high driving voltage (discussed in chapter 3). After removal of the foundry passivation a pin-hole free low temperature high-κ dielectric is required to be deposited on the exposed electrode. Anodic tantalum pentoxide is proposed as the insulating dielectric layer. The anodisation process can be performed before the tantalum electrode patterning, with Ta_2O_5 being masked by photoresist and etched together with the tantalum metal. Anodisation can also be performed after electrode patterning, in which case the anodisation current will pass through the electrode addressing circuit and this needs to be considered as part of the circuit design Although the current for each electrode will be a few μA (depending on the electrode size, the total anodisation current density) typically ranges from 1 to 10mAcm^{-2} [88]), and this would need to be addressed as part of the circuit and design of the system.

Once the low voltage active EWOD system is demonstrated, further developments can be made. One is to integrate the electrodes with various sensors (e.g. temperature, pH, light). An example

would be single-photon-avalanche-diodes (SPAD) embedded(figure 6.7) for which a CMOS backplane has been designed and fabricated [117]. The integration of sensing and EWOD droplet functions will help to realise the goal of an in-situ μTAS example.

Since the active EWOD system supports a larger electrode arrays this enables greater system flexibility, higher throughput concurrent droplet manipulation and finer volume control to be achieved. For example, test structures for studying droplet volume control issues can be developed. Control software and algorithm design will be another interesting area. Other developments that will be of interest can be process optimisation related, such as adding chemical mechanical polishing (CMP) and damascene processes to planarise the surface reducing the droplet movement hysteresis.

Unfortunately there was not time to undertake a full characterisation of the technology that has been developed. Areas that could gainfully be addressed are a full characterisation of the relationship between electrode size and the gap, determination of the minimum electrode size, the parameters that affect droplet speed and last but not least reliability. The reliability and length of time an EWOD system will operate were both issues that are not reported in any great detail in the literature although liquid permeating PECVD dielectrics causing electrolysis is mentioned [51]. The systems reported in the thesis have an extremely robust insulating dielectric which causes no problems during operation and this coupled with an appropriate voltage driving scheme have enable a sealed EWOD device to operate continuously for 18 hrs. There is clearly a need to rigorously characterise and then optimise the reliability and lifetime of EWOD devices as this is of key importance for any commercial application.

Another further objective is to demonstrate a continuous movement of the pondskater. Current issues are the restraining force caused by the electrical wiring and the requirement for bubble generation. RF wireless signal and power transfer [114, 116] or solar cell technology are two options that remove the requirement for wiring. Both require the integration of EWOD and CMOS technology. The bubble generation could potentially be achieved using electro-chemical methods such as electrolysis. Figure 8.14 shows an alternative to bubble injection, with the device being propelled by altering the bubble shape and changing its position.

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Appendix A
List of Publications

A.1 Journal papers

1. Yifan. Li, William. Parkes, Les. I. Haworth, and Anthony. J. Walton, "Low Voltage Electro-Wetting on Dielectric (EWOD) using Ultra-thin Amorphous Fluoropolymer (aFP) and Anodic Tantalum Pentoxide Layers", *IEEE Journal of MEMS*, Submitted, May 2007

A.2 Conference papers

1. A.J. Walton, J.T.M. Stevenson, I. Underwood, J.G. Terry, S. Smith, W. Parkes, C.C. Dunare, H. Lin, Y. Li, R. Henderson, D. Renshaw, M.P. Desmulliez, B.W. Flynn, M.J. MacIntosh, W. Holland, A.F. Murray, T.B. Tang, A.S. Bunting, A.M. Gundlach, "Integration of IC technology with MEMS: Silicon+ technology for the future", *IET Seminar on MEMS, Sensors and Actuators,* 1-11, April 2007

2. Y. Li, Y. Mita, L.I. Haworth, W. Parkes, M. Kubota, A.J. Walton, "Test Structure for Characterising Low Voltage Coplanar EWOD System", *ICMTS 2008*, Accepted

3. Y. Li, W. Parkes, L.I. Haworth, A.A. Stokes, K.R. Muir, P. Li, A.J. Collin, N.G. Hutcheon, R. Henderson, B. Rae and A.J. Walton, "Anodic Ta_2O_5 for CMOS Compatible Low Voltage Electrowetting-On-Dielectric Device Fabrication", *ESSDERC*, 446-449, 2007/09

4. Y. Li, A. Kazantzis, L.I. Haworth, K. Muir, A.W.S. Ross, J.G. Terry, J.T.M. Stevenson, A.M. Gundlach, A.S. Bunting, A.J. Walton;"Building EWOD Microfluidic Array Technology on Top of Foundry CMOS", *IET Seminar on MEMS, Sensors and Actuators*, April 2006

5. Y. Li, P. Li, L.I. Haworth, A.J. Walton; "The integration of EWOD microfluidic technology with foundry CMOS", *Micro and Nanotechnology 2005*

Appendix B
Sample Programs

Appendix B

Multi-electrodes point and go program:

```
#include <stdio.h>
#include <stdlib.h>
#include <math.h>
#include <time.h>
#include <windows.h>
#include <winioctl.h>
#include <conio.h>
#include <string.h>
//should include above headers otherwise the declarations in bluechip.h will have errors

#include "bluechip.h"


//identifying boards:PIO0PortA~PortC and PIO1PortA
//identifying global variable: nOutVal


BCT_HANDLE nPciPio0PortAHandle;
BCT_HANDLE nPciPio0PortBHandle;
BCT_HANDLE nPciPio0PortCHandle;
BCT_HANDLE nPciPio1PortAHandle;
BCT_BOARD_ID pPciPioBoardId;
PBCT_BUFFER pPioBuffer;
BCT_BYTE nOutVal;
BCT_BYTE nOutV[4];
int digit; //relate to digit position on each PIO
int port; //relate to the PIO number
int d; //relate to delay time
int resvr; //relate to reservoir electrode output channel
int neck; //relate to neck electrode output channel
int targt; //relate to target electrode output channel
int array_N[20][4]; //relate to electrodes numbers switch on in sequence
                    //subelectrodes number for each big electrode is four
int array_D[20]; //relate to switch on delay time in sequence
int SC; //relate to total electrodes number in that sequence
int flagi; //relate to current switched on electrode

/* ----------------------------------------------------------- */
/* Define keystrokes.                                        */
/* ----------------------------------------------------------- */

#define   ESC 0x1B
/* BCT card PCI Status finction codes (by Michael)
#define BCT_NO_BCT_BOARDS 0x0000
#define BCT_NO_PCI_BIOS_PRESENT 0x0100*/

/* declare functions */
```

```c
void Initialise(void);
void Deinitialise(void);
void OutputPIO0PortA(void);
void OutputPIO0PortB(void);
void OutputPIO0PortC(void);
void OutputPIO1PortA(void);
void move(void); //moving function
void delay(void); //delay function (use variable 'd')
void menu(void); //menu function
void output(void); //output function
void clear(void); //clear all output to 0


int main()
{

`       // Initialise the PCI card

        Initialise();


        //prompt user to determine which electrode they wish to control
        move();


        //clear the voltage on all electrodes at the end and deinitialise the PCI card
        d=1000; //1s delay then deinitialise
        delay();
        clear();

        Deinitialise();

return 0;

}

/*function for dispensing a droplet from a reservoir:
    procedure:
                reservoir       neck electrode      target electrode
    1:          off                 on                  on
    2:          on                  off                 on
    3:          off                 off                 off

*/

void move(void)
{
    int i=0;
    menu();
    flagi=0;

    do
    {
```

```
                    for(i=0;i<4;i++) //refreshing 4 ports' output value
                    {
                            port = (array_N[flagi][i]-1)/5;    // calculation for the port the electrode refers to
                            digit = array_N[flagi][i]-(5*port);   // calculation for the individual digit in the
port
                            nOutV[port] = (1<<(digit-1))+nOutV[port];
                    }
                    d=array_D[flagi];
                    output();
                    delay();
                    clear(); //clear both nOutV and nOutVal
                    flagi=flagi+1;
            }while(flagi<SC);


}


//menu function for input 4 electrode with 1 delay time
void menu(void)
{
        int temp_n = 0;
        int temp_d = 0;
        int i = 0;
        SC=0;

        do
        {
                for(i=0;i<4;i++)
                {
                        printf("\nPlease enter the four subelectrode of a electrod you wish to turn on(enter
0 if absense ");
                        printf("\nEnter 99 when you have finished:");
                        scanf("%d",&temp_n);
                        if(temp_n==99)
                        {
                            return;
                        }
                        array_N[SC][i]=temp_n;
                }
                printf("\nPlease enter the delay you wish to use (ms):");
                scanf("%d",&temp_d);
                if(temp_d==99)
                {
                        return;
                }
                array_D[SC]=temp_d;
                SC++;

        }while(1);
}

//output refresh for all electrodes
void output(void)
{
```

```
                nOutVal=nOutV[0];
                OutputPIO0PortA();
                nOutVal=nOutV[1];
                OutputPIO0PortB();
                nOutVal=nOutV[2];
                OutputPIO0PortC();
                nOutVal=nOutV[3];
                OutputPIO1PortA();
                return;


}

void delay(void)
{
        //modified by Yifan 07Feb07 for switching frequency over 1KHz

                LARGE_INTEGER ticksPerSecond; //counter's accuracy on this PC in ses
                LARGE_INTEGER ticksPerMiliSecond; //counter's accuracy in msec
                LARGE_INTEGER tick; //total counter's tick after start counting

                LARGE_INTEGER time; //total milisec after start counting
                LARGE_INTEGER time_now; //total milisec till NOW

                //get the tick number for 1 second
                QueryPerformanceFrequency(&ticksPerSecond);
                //if one second 1000 tick, then one ms should be 1 tick
                ticksPerMiliSecond.QuadPart = ticksPerSecond.QuadPart/1000;

                //what time is it now?
                QueryPerformanceCounter(&tick);
                time.QuadPart = tick.QuadPart/ticksPerMiliSecond.QuadPart;
                do
                {
                                QueryPerformanceCounter(&tick);
                                time_now.QuadPart = tick.QuadPart/ticksPerMiliSecond.QuadPart;

                  }while((time_now.QuadPart-time.QuadPart)<d);

                // 1 is 1 milisecond delay, can be other number of miliseconds

return;
}
/* previous delay
void delay(void)
{

                time_t start_time,cur_time;
                time(&start_time);
                do
                {
                                time(&cur_time);
                  }while((cur_time-start_time)<d);
```

```
                // 1 is 1 second delay, can be other number of seconds

return;
}

*/


//clear '0' function
void clear(void)
{
        nOutV[0] = 0;
        nOutV[1] = 0;
        nOutV[2] = 0;
        nOutV[3] = 0;
        output();
}



//Yifan's board initialise function:
void Initialise(void)
{
        BCT_DWORD dwStatus;
        char szErrorText[120]; //for checking the dwstatus and do error display
        int nIndex;

        // Initialise the four handles we are going to use: P0ABC and P1A
        // This is to initialise the handle structions we are going to put PCI card directions in
        // (e.g. for puting MEM addresses afterwards)
        dwStatus = BCTInitHandle(&nPciPio0PortAHandle);

        //check point
        //printf("PciPio0PortAHandle is: [%d]\n", nPciPio0PortAHandle);

        if (dwStatus != BCT_OK)
        {
                BCTErr2Txt(dwStatus, szErrorText);
                printf("BCTInitHandle returned: %s\n", szErrorText);
        }
        dwStatus = BCTInitHandle(&nPciPio0PortBHandle);

        //check point
        //printf("PciPio0PortBHandle is: [%d]\n", nPciPio0PortBHandle);

        if (dwStatus != BCT_OK)
        {
                BCTErr2Txt(dwStatus, szErrorText);
                printf("BCTInitHandle returned: %s\n", szErrorText);
        }
        dwStatus = BCTInitHandle(&nPciPio0PortCHandle);

        //check point
        //printf("PciPio0PortCHandle is: [%d]\n", nPciPio0PortCHandle);
```

```c
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTInitHandle returned: %s\n", szErrorText);
    }
    dwStatus = BCTInitHandle(&nPciPio1PortAHandle);

    //check point
    //printf("PciPio1PortAHandle is: [%d]\n", nPciPio1PortAHandle);

    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTInitHandle returned: %s\n", szErrorText);
    }

    // Get the driver to fill out the board ID structure for initialisation
    dwStatus = BCTGetBoardId(&pPciPioBoardId, PCI_PIO, 0);

    //check point
    //printf("PciPioBoardId is: [%d]\n", pPciPioBoardId);

    if (dwStatus != BCT_OK)
    {

        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTGetBoardId returned: %s\n", szErrorText);
    }

    // Our program is to use PIO0Port_ABC and PIO1Port_A to be Output only
    // So PIO0_AB and PIO1_A should be set to OUTPUT, and PIO0_C to OUTOUT for 8bit
output
    // Mode 0 is going to be used, PIO1_BC is NOCARE
    // This is to write the setting registers in the PCI Card
    dwStatus = BCTInit8255Modes(&pPciPioBoardId, 0, MODE_0, OUTPUT, OUTPUT,
OUTOUT);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTInit8255Modes returned: %s\n", szErrorText);
    }
    dwStatus = BCTInit8255Modes(&pPciPioBoardId, 1, MODE_0, OUTPUT, NOCARE,
NOCARE);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTInit8255Modes returned: %s\n", szErrorText);
    }

    // Open the handles that will be used by the Digital Output calls we will make
    // This is to give the direction (e.g. address in MEM) to the PCI card for our variables
    dwStatus = BCTOpen(&nPciPio0PortAHandle, &pPciPioBoardId, BCT_8255, 0,
BCT_PORT_A);
```

```c
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTOpen returned: %s\n", szErrorText);
    }
    dwStatus  =  BCTOpen(&nPciPio0PortBHandle,  &pPciPioBoardId,  BCT_8255,  0,
BCT_PORT_B);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTOpen returned: %s\n", szErrorText);
    }
    dwStatus  =  BCTOpen(&nPciPio0PortCHandle,  &pPciPioBoardId,  BCT_8255,  0,
BCT_PORT_C);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTOpen returned: %s\n", szErrorText);
    }
    dwStatus  =  BCTOpen(&nPciPio1PortAHandle,  &pPciPioBoardId,  BCT_8255,  1,
BCT_PORT_A);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTOpen returned: %s\n", szErrorText);
    }

    // Allocate some space and fill in the buffer structure so that we
    // have data for the paced output, not necessary currently-----Yifan
    dwStatus = BCTAllocate(&pPioBuffer, 256);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTAllocate returned: %s\n", szErrorText);
    }
    for (nIndex = 0; nIndex < 256; nIndex++)
    {
        pPioBuffer -> Buffer[nIndex] = nIndex;
    }
}


/* ------------------------------------------------------------ */
/* Deinitialise - Close the board id structure and the          */
/*                      handles that we have been using.         */
/* ------------------------------------------------------------ */

void Deinitialise(void)
{
    BCT_DWORD dwStatus;
    char szErrorText[120];

    // Make sure that the memory we have been using for the pacer
    // is released
```

```
        dwStatus = BCTRelease(&pPioBuffer);
        if (dwStatus != BCT_OK)
        {
             BCTErr2Txt(dwStatus, szErrorText);
             printf("BCTRelease returned: %s\n", szErrorText);
        }


        // Close all the four handles
        dwStatus = BCTClose(&nPciPio0PortAHandle);
        if (dwStatus != BCT_OK)
        {
             BCTErr2Txt(dwStatus, szErrorText);
             printf("BCTClose returned: %s\n", szErrorText);
        }
        dwStatus = BCTClose(&nPciPio0PortBHandle);
        if (dwStatus != BCT_OK)
        {
             BCTErr2Txt(dwStatus, szErrorText);
             printf("BCTClose returned: %s\n", szErrorText);
        }
        dwStatus = BCTClose(&nPciPio0PortCHandle);
        if (dwStatus != BCT_OK)
        {
             BCTErr2Txt(dwStatus, szErrorText);
             printf("BCTClose returned: %s\n", szErrorText);
        }
        dwStatus = BCTClose(&nPciPio1PortAHandle);
        if (dwStatus != BCT_OK)
        {
             BCTErr2Txt(dwStatus, szErrorText);
             printf("BCTClose returned: %s\n", szErrorText);
        }


        // Release the board ID structure
        dwStatus = BCTReleaseBoardId(&pPciPioBoardId);
        if (dwStatus != BCT_OK)
        {
             BCTErr2Txt(dwStatus, szErrorText);
             printf("BCTReleaseBoardId returned: %s\n", szErrorText);
        }
}

//Output functions ----Yifan
void OutputPIO0PortA(void)
{
        BCT_DWORD dwStatus;
        char szErrorText[120];   //for checking the dwstatus and do error display

        //Output the value to PIO_0 Port_A
        //check point
        //printf("OutVal=[%d]", nOutVal);

        dwStatus=BCTWritePort(&nPciPio0PortAHandle, nOutVal);
        if (dwStatus == BCT_IO_PENDING)
```

```
        {
            dwStatus=BCTWait(&nPciPio0PortAHandle, INFINITE);
        }
        if ((dwStatus != BCT_OK) && (dwStatus != BCT_IO_PENDING))
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTWritePort returned: %s\n", szErrorText);
        }
        return;
}

void OutputPIO0PortB(void)
{
        BCT_DWORD dwStatus;
        char szErrorText[120];   //for checking the dwstatus and do error display

        //Output the value to PIO_0 Port_B
        //check point
        //printf("OutVal=[%d]", nOutVal);

        dwStatus=BCTWritePort(&nPciPio0PortBHandle, nOutVal);
        if (dwStatus == BCT_IO_PENDING)
        {
            dwStatus=BCTWait(&nPciPio0PortBHandle, INFINITE);
        }
        if ((dwStatus != BCT_OK) && (dwStatus != BCT_IO_PENDING))
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTWritePort returned: %s\n", szErrorText);
        }
        return;
}

void OutputPIO0PortC(void)
{
        BCT_DWORD dwStatus;
        char szErrorText[120];   //for checking the dwstatus and do error display

        //Output the value to PIO_0 Port_C
        //check point
        //printf("OutVal=[%d]", nOutVal);

        dwStatus=BCTWritePort(&nPciPio0PortCHandle, nOutVal);
        if (dwStatus == BCT_IO_PENDING)
        {
            dwStatus=BCTWait(&nPciPio0PortCHandle, INFINITE);
        }
        if ((dwStatus != BCT_OK) && (dwStatus != BCT_IO_PENDING))
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTWritePort returned: %s\n", szErrorText);
        }
        return;
}
```

```c
void OutputPIO1PortA(void)
{
    BCT_DWORD dwStatus;
    char szErrorText[120];   //for checking the dwstatus and do error display

    //Output the value to PIO_1 Port_A
    //check point
    //printf("OutVal=[%d]", nOutVal);

    dwStatus=BCTWritePort(&nPciPio1PortAHandle, nOutVal);
    if (dwStatus == BCT_IO_PENDING)
    {
        dwStatus=BCTWait(&nPciPio1PortAHandle, INFINITE);
    }
    if ((dwStatus != BCT_OK) && (dwStatus != BCT_IO_PENDING))
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTWritePort returned: %s\n", szErrorText);
    }
    return;
}
```

Loop program:

```
#include <stdio.h>
#include <stdlib.h>
#include <math.h>
#include <time.h>
#include <windows.h>
#include <winioctl.h>
#include <conio.h>
#include <string.h>
//should include above headers otherwise the declarations in bluechip.h will have lot errs
#include "bluechip.h"

//identifying boards:PIO0PortA~PortC and PIO1PortA
//identifying global variable: nOutVal

BCT_HANDLE nPciPio0PortAHandle;
BCT_HANDLE nPciPio0PortBHandle;
BCT_HANDLE nPciPio0PortCHandle;
BCT_HANDLE nPciPio1PortAHandle;
BCT_BOARD_ID pPciPioBoardId;
PBCT_BUFFER pPioBuffer;
BCT_BYTE nOutVal; //Use global variable nOutVal to replace pointers
BCT_BYTE nOutV[4];
BCT_BYTE digit; //relate to digit position on each PIO
BCT_BYTE port; //relate to the PIO number
int d; //relate to delay time
int array_N[20][4]; //relate to electrodes numbers switch on in sequence
                    //subelectrodes number for each big electrode is four
int array_D[20]; //relate to switch on delay time in sequence
int SC; //relate to total electrodes number in that sequence
int flagi; //relate to current switched on electrode

/* ------------------------------------------------------------ */
/* Define keystrokes.                                        */
/* ------------------------------------------------------------ */

#define  ESC 0x1B

/* declare functions */
void Initialise(void);
void Deinitialise(void);
void OutputPIO0PortA(void);
void OutputPIO0PortB(void); //only use two port in this function
void OutputPIO0PortC(void);
void OutputPIO1PortA(void);
void dispense(void);
void loop(void);
void finish(void);
void move(void);
void move1(void);
```

```c
void output(void);
void delay(void);
void clear(void);

int main()
{
    /* declare variables   */

    // Initialise the PCI card
    Initialise();
    nOutVal=0;

    //dispense(); //switch on 2,3,4,5; then 1,5; then all off
    //d=1000;
    //delay();

    loop(); //switch on 5, then 6 and 5 and 6 again
    d=1000;
    delay();

    //finish(); //switch on 5&4, then 4$3, then 3&2, then 2&1
    //d=1000;
    //delay();

    nOutVal=0;
    OutputPIO0PortA();
    OutputPIO0PortB();
    OutputPIO0PortC();
    OutputPIO1PortA();

    Deinitialise();

return 0;

}

void dispense(void)
{

    SC=2;
    array_N[0][0]=17; //electrode #2
    array_N[0][1]=18; //#3
    array_N[0][2]=19; //#4
    array_N[0][3]=0;

    array_N[3][0]=16; //#1
    array_N[3][1]=19; //#4
    array_N[3][2]=0;
    array_N[3][3]=0;

    d=2000;
    move1();
}
```

```
void loop()
{
    //Loop running till counter=300 (5minutes)
    do
    {
        /*initscr(); cbreak();*/

    /*    nodelay();   does not work */
/* halfdelay(1); */
/* noecho(); */
/*    nonl(); */
/*    intrflush(stdscr, FALSE); */
/*    keypad(stdscr, TRUE); */

        //upper
        SC=5;
        array_N[0][0]=4; //electrode #2
        array_N[0][1]=7; //12
        array_N[0][2]=0;
        array_N[0][3]=0;

        array_N[1][0]=3; //electrode #3
        array_N[1][1]=6; //11
        array_N[1][2]=0;
        array_N[1][3]=0;

        array_N[2][0]=2; //electrode #4
        array_N[2][1]=16; //10
        array_N[2][2]=0;
        array_N[2][3]=0;

        array_N[3][0]=1; //electrode #5
        array_N[3][1]=17; //9
        array_N[3][2]=0;
        array_N[3][3]=0;

        array_N[4][0]=20; //electrode #6
        array_N[4][1]=18; //8
        array_N[4][2]=0;
        array_N[4][3]=0;

        d=1000;
        move();

        //down
        SC=8;
        array_N[0][0]=20; //#6
        array_N[0][1]=18; //8
        array_N[0][2]=0;
        array_N[0][3]=0;

        array_N[1][0]=1; //5
        array_N[1][1]=17; //9
        array_N[1][2]=0;
```

```c
            array_N[1][3]=0;

            array_N[2][0]=2; //electrode #4
            array_N[2][1]=16; //10
            array_N[2][2]=0;
            array_N[2][3]=0;

            array_N[3][0]=3; //electrode #3
            array_N[3][1]=6; //11
            array_N[3][2]=0;
            array_N[3][3]=0;

            array_N[4][0]=4; //electrode #2
            array_N[4][1]=7; //12
            array_N[4][2]=0;
            array_N[4][3]=0;

            d=1000;
            move();

            if(kbhit())break;

    }while(1); //loop till keyboard

}

void finish(void)
{

    SC=4;
    array_N[0][0]=19; //electrode #4
    array_N[0][1]=0;
    array_N[0][2]=0;
    array_N[0][3]=0;

    array_N[1][0]=18; //electrode #3
    array_N[1][1]=0;
    array_N[1][2]=0;
    array_N[1][3]=0;

    array_N[2][0]=17; //electrode #2
    array_N[2][1]=0;
    array_N[2][2]=0;
    array_N[2][3]=0;

    array_N[3][0]=16; //electrode #1
    array_N[3][1]=0;
    array_N[3][2]=0;
    array_N[3][3]=0;

    d=200;
    move();

}
```

```
void move(void)
{
    int i=0;
    int j=0;
    //menu();
    flagi=0;


    do
    {
        d=1000;
        //for(j=0;j<5;j++) //create AC wave form, 2s per period, first 1s 2.5HZ pules
        //{
            for(i=0;i<4;i++) //refreshing 4 ports' output value
            {
                port = (array_N[flagi][i]-1)/5;      // calculation for the port the electrode
refers to
                digit = array_N[flagi][i]-(5*port);    // calculation for the individual digit in
the port
                nOutV[port] = (1<<(digit-1))+nOutV[port];
            }
            output();
            delay();
            clear(); //clear both nOutV and nOutVal
            /*output(); //switch off for same amount of time
            delay();*/
        //}

        /*d=1000; //Next 1s no pulse
        clear();
        output();
        delay();*/
        flagi=flagi+1;

    }while(flagi<SC);

}

void move1(void)
{
    int i=0;
    int j=0;
    //menu();
    flagi=0;


    do
    {

        for(i=0;i<4;i++) //refreshing 4 ports' output value
        {
            port = (array_N[flagi][i]-1)/5;      // calculation for the port the electrode
refers to
```

```
                              digit = array_N[flagi][i]-(5*port);   // calculation for the individual digit in
the port
                              nOutV[port] = (1<<(digit-1))+nOutV[port];
                       }
                output();
                delay();

        flagi=flagi+1;

    }while(flagi<SC);

}

//output refresh for all electrodes
void output(void)
{
    nOutVal=nOutV[0];
    OutputPIO0PortA();
    nOutVal=nOutV[1];
    OutputPIO0PortB();
    nOutVal=nOutV[2];
    OutputPIO0PortC();
    nOutVal=nOutV[3];
    OutputPIO1PortA();
    return;


}

void delay(void)
{
    //modified by Yifan 07Feb07 for switching frequency over 1KHz

        LARGE_INTEGER ticksPerSecond; //counter's accuracy on this PC in ses
        LARGE_INTEGER ticksPerMiliSecond; //counter's accuracy in msec
        LARGE_INTEGER tick; //total counter's tick after start counting

        LARGE_INTEGER time; //total milisec after start counting
        LARGE_INTEGER time_now; //total milisec till NOW

        //get the tick number for 1 second
        QueryPerformanceFrequency(&ticksPerSecond);
        //if one second 1000 tick, then one ms should be 1 tick
        ticksPerMiliSecond.QuadPart = ticksPerSecond.QuadPart/1000;

        //what time is it now?
        QueryPerformanceCounter(&tick);
        time.QuadPart = tick.QuadPart/ticksPerMiliSecond.QuadPart;
        do
        {
                QueryPerformanceCounter(&tick);
                time_now.QuadPart = tick.QuadPart/ticksPerMiliSecond.QuadPart;

        }while((time_now.QuadPart-time.QuadPart)<d);
```

```
                // 1 is 1 milisecond delay, can be other number of miliseconds

return;
}

void clear(void)
{
      nOutV[0] = 0;
      nOutV[1] = 0;
      nOutV[2] = 0;
      nOutV[3] = 0;
      output();
}


//Yifan's board initialise function:
void Initialise(void)
{
      BCT_DWORD dwStatus;
      char szErrorText[120]; //for checking the dwstatus and do error display
      int nIndex;

      // Initialise the four handles we are going to use: P0ABC and P1A
      // This is to initialise the handle structions we are going to put PCI card directions in
      // (e.g. for puting MEM addresses afterwards)
      dwStatus = BCTInitHandle(&nPciPio0PortAHandle);

      //check point
      //printf("PciPio0PortAHandle is: [%d]\n", nPciPio0PortAHandle);

      if (dwStatus != BCT_OK)
      {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTInitHandle returned: %s\n", szErrorText);
      }
      dwStatus = BCTInitHandle(&nPciPio0PortBHandle);

      //check point
      //printf("PciPio0PortBHandle is: [%d]\n", nPciPio0PortBHandle);

      if (dwStatus != BCT_OK)
      {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTInitHandle returned: %s\n", szErrorText);
      }
      dwStatus = BCTInitHandle(&nPciPio0PortCHandle);

      //check point
      //printf("PciPio0PortCHandle is: [%d]\n", nPciPio0PortCHandle);

      if (dwStatus != BCT_OK)
      {
            BCTErr2Txt(dwStatus, szErrorText);
```

```
        printf("BCTInitHandle returned: %s\n", szErrorText);
    }
    dwStatus = BCTInitHandle(&nPciPio1PortAHandle);

    //check point
    //printf("PciPio1PortAHandle is: [%d]\n", nPciPio1PortAHandle);

    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTInitHandle returned: %s\n", szErrorText);
    }

    // Get the driver to fill out the board ID structure for initialisation
    dwStatus = BCTGetBoardId(&pPciPioBoardId, PCI_PIO, 0);

    //check point
    //printf("PciPioBoardId is: [%d]\n", pPciPioBoardId);

    if (dwStatus != BCT_OK)
    {

        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTGetBoardId returned: %s\n", szErrorText);
    }

    // Our program is to use PIO0Port_ABC and PIO1Port_A to be Output only
    // So PIO0_AB and PIO1_A should be set to OUTPUT, and PIO0_C to OUTOUT for 8bit
output
    // Mode 0 is going to be used, PIO1_BC is NOCARE
    // This is to write the setting registers in the PCI Card
    dwStatus = BCTInit8255Modes(&pPciPioBoardId, 0, MODE_0, OUTPUT, OUTPUT,
OUTOUT);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTInit8255Modes returned: %s\n", szErrorText);
    }
    dwStatus = BCTInit8255Modes(&pPciPioBoardId, 1, MODE_0, OUTPUT, NOCARE,
NOCARE);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTInit8255Modes returned: %s\n", szErrorText);
    }

    // Open the handles that will be used by the Digital Output calls we will make
    // This is to give the direction (e.g. address in MEM) to the PCI card for our variables
    dwStatus = BCTOpen(&nPciPio0PortAHandle, &pPciPioBoardId, BCT_8255, 0,
BCT_PORT_A);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTOpen returned: %s\n", szErrorText);
```

```c
        }
        dwStatus  =  BCTOpen(&nPciPio0PortBHandle,  &pPciPioBoardId,  BCT_8255,  0,
BCT_PORT_B);
        if (dwStatus != BCT_OK)
        {
                BCTErr2Txt(dwStatus, szErrorText);
                printf("BCTOpen returned: %s\n", szErrorText);
        }
        dwStatus  =  BCTOpen(&nPciPio0PortCHandle,  &pPciPioBoardId,  BCT_8255,  0,
BCT_PORT_C);
        if (dwStatus != BCT_OK)
        {
                BCTErr2Txt(dwStatus, szErrorText);
                printf("BCTOpen returned: %s\n", szErrorText);
        }
        dwStatus  =  BCTOpen(&nPciPio1PortAHandle,  &pPciPioBoardId,  BCT_8255,  1,
BCT_PORT_A);
        if (dwStatus != BCT_OK)
        {
                BCTErr2Txt(dwStatus, szErrorText);
                printf("BCTOpen returned: %s\n", szErrorText);
        }

        // Allocate some space and fill in the buffer structure so that we
        // have data for the paced output, not necessary currently-----Yifan
        dwStatus = BCTAllocate(&pPioBuffer, 256);
        if (dwStatus != BCT_OK)
        {
                BCTErr2Txt(dwStatus, szErrorText);
                printf("BCTAllocate returned: %s\n", szErrorText);
        }
        for (nIndex = 0; nIndex < 256; nIndex++)
        {
                pPioBuffer -> Buffer[nIndex] = nIndex;
        }
}


/* ------------------------------------------------------------ */
/* Deinitialise - Close the board id structure and the          */
/*                         handles that we have been using.              */
/* ------------------------------------------------------------ */

void Deinitialise(void)
{
        BCT_DWORD dwStatus;
        char szErrorText[120];

        // Make sure that the memory we have been using for the pacer
        // is released
        dwStatus = BCTRelease(&pPioBuffer);
        if (dwStatus != BCT_OK)
        {
                BCTErr2Txt(dwStatus, szErrorText);
```

```c
            printf("BCTRelease returned: %s\n", szErrorText);
        }

        // Close all the four handles
        dwStatus = BCTClose(&nPciPio0PortAHandle);
        if (dwStatus != BCT_OK)
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTClose returned: %s\n", szErrorText);
        }
        dwStatus = BCTClose(&nPciPio0PortBHandle);
        if (dwStatus != BCT_OK)
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTClose returned: %s\n", szErrorText);
        }
        dwStatus = BCTClose(&nPciPio0PortCHandle);
        if (dwStatus != BCT_OK)
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTClose returned: %s\n", szErrorText);
        }
        dwStatus = BCTClose(&nPciPio1PortAHandle);
        if (dwStatus != BCT_OK)
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTClose returned: %s\n", szErrorText);
        }

        // Release the board ID structure
        dwStatus = BCTReleaseBoardId(&pPciPioBoardId);
        if (dwStatus != BCT_OK)
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTReleaseBoardId returned: %s\n", szErrorText);
        }
    }

//Output functions ----Yifan
void OutputPIO0PortA(void)
{
    BCT_DWORD dwStatus;
    char szErrorText[120];   //for checking the dwstatus and do error display

    //Output the value to PIO_0 Port_A
    //check point
    //printf("OutVal=[%d]", nOutVal);

    dwStatus=BCTWritePort(&nPciPio0PortAHandle, nOutVal);
    if (dwStatus == BCT_IO_PENDING)
    {
        dwStatus=BCTWait(&nPciPio0PortAHandle, INFINITE);
    }
    if ((dwStatus != BCT_OK) && (dwStatus != BCT_IO_PENDING))
```

```
                {
                    BCTErr2Txt(dwStatus, szErrorText);
                    printf("BCTWritePort returned: %s\n", szErrorText);
                }
            return;
        }

void OutputPIO0PortB(void)
    {
        BCT_DWORD dwStatus;
        char szErrorText[120];   //for checking the dwstatus and do error display

        //Output the value to PIO_0 Port_B
        //check point
        //printf("OutVal=[%d]", nOutVal);

        dwStatus=BCTWritePort(&nPciPio0PortBHandle, nOutVal);
        if (dwStatus == BCT_IO_PENDING)
        {
            dwStatus=BCTWait(&nPciPio0PortBHandle, INFINITE);
        }
        if ((dwStatus != BCT_OK) && (dwStatus != BCT_IO_PENDING))
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTWritePort returned: %s\n", szErrorText);
        }
        return;
    }

void OutputPIO0PortC(void)
    {
        BCT_DWORD dwStatus;
        char szErrorText[120];   //for checking the dwstatus and do error display

        //Output the value to PIO_0 Port_C
        //check point
        //printf("OutVal=[%d]", nOutVal);

        dwStatus=BCTWritePort(&nPciPio0PortCHandle, nOutVal);
        if (dwStatus == BCT_IO_PENDING)
        {
            dwStatus=BCTWait(&nPciPio0PortCHandle, INFINITE);
        }
        if ((dwStatus != BCT_OK) && (dwStatus != BCT_IO_PENDING))
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTWritePort returned: %s\n", szErrorText);
        }
        return;
    }

void OutputPIO1PortA(void)
    {
        BCT_DWORD dwStatus;
```

```c
        char szErrorText[120];   //for checking the dwstatus and do error display

        //Output the value to PIO_1 Port_A
        //check point
        //printf("OutVal=[%d]", nOutVal);

        dwStatus=BCTWritePort(&nPciPio1PortAHandle, nOutVal);
        if (dwStatus == BCT_IO_PENDING)
        {
            dwStatus=BCTWait(&nPciPio1PortAHandle, INFINITE);
        }
        if ((dwStatus != BCT_OK) && (dwStatus != BCT_IO_PENDING))
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTWritePort returned: %s\n", szErrorText);
        }
        return;
}
```

Data file I/O program:

```c
#include <stdio.h>
#include <stdlib.h>
#include <math.h>
#include <time.h>
#include <windows.h>
#include <winioctl.h>
#include <conio.h>
#include <string.h>
//should include above headers otherwise the declarations in bluechip.h will have errors

#include "bluechip.h"


//identifying boards:PIO0PortA~PortC and PIO1PortA
//identifying global variable: nOutVal


BCT_HANDLE nPciPio0PortAHandle;
BCT_HANDLE nPciPio0PortBHandle;
BCT_HANDLE nPciPio0PortCHandle;
BCT_HANDLE nPciPio1PortAHandle;
BCT_BOARD_ID pPciPioBoardId;
PBCT_BUFFER pPioBuffer;
BCT_BYTE nOutVal;
BCT_BYTE nOutV[4];
BCT_BYTE digit; //relate to digit position on each PIO
BCT_BYTE port; //relate to the PIO number
int d; //relate to delay time
int resvr; //relate to reservoir electrode output channel
int neck; //relate to neck electrode output channel
int targt; //relate to target electrode output channel
int array_N[20][4]; //relate to electrodes numbers switch on in sequence
                    //subelectrodes number for each big electrode is four
int array_D[20]; //relate to switch on delay time in sequence
int SC; //relate to total electrodes number in that sequence
int flagi; //relate to current switched on electrode

/* ------------------------------------------------------------ */
/* Define keystrokes.                                        */
/* ------------------------------------------------------------ */

#define   ESC 0x1B
/* BCT card PCI Status finction codes (by Michael)
#define BCT_NO_BCT_BOARDS 0x0000
#define BCT_NO_PCI_BIOS_PRESENT 0x0100*/


/* declare functions */
void Initialise(void);
void Deinitialise(void);
void OutputPIO0PortA(void);
void OutputPIO0PortB(void);
void OutputPIO0PortC(void);
```

```c
void OutputPIO1PortA(void);
void move(void); //moving function
void delay(void); //delay function (use variable 'd')
void menu(void); //menu function
void output(void); //output function
void clear(void); //clear all output to 0




int main(int argc,char *argv[])
{

    FILE *fp;
    int ch=0;
    int i=0;
    flagi=0;

    // Initialise the PCI card

    Initialise();


    if(argc!=2)
    {
        printf("You forgot to enter the filenames. \n");
        exit(1);
    }

    if((fp=fopen(argv[1],"r"))==NULL)
    {
        printf("Cannot open file. \n");
        exit(1);
    }
    printf("ch=%d. \n",ch); //check point
    printf("array_N[0][0]=%d. \n",array_N[0][0]); //check point
    printf("flagi=%d. \n",flagi);
    printf("fp=%d. \n",fp);
    rewind(fp);
    printf("fp=%d. \n",fp);

    while(1)
    {
        for(i=0;i<4;i++) //can switch 4 electrodes at the same time (in one sequence)
        {   printf("I'm inside now!!! \n");//check point

            if(fread(&ch,sizeof(int),1,fp)!=1)
            {
                printf("File read error. \n");
                exit(1);
            }
            printf("I'm before ch=99 checking! \n"); //check point
```

```c
                if(ch==99)break;

                printf("First round not breaking out! \n"); //check point

                printf("ch=%d. \n",ch);
                array_N[flagi][i]=ch; //file read out check point
                if(feof(fp))break;
            }
        if(ch==99)break;
        if(feof(fp))break;
        flagi=flagi+1;

    }

    fclose(fp);
    SC=flagi;//remember how many sequences in this time's droplets motion
    printf("SC=%d. \n", SC);

    //read delay file
/*  flagi=0;
    if((fp=fopen(argv[2],"r"))==NULL){
        printf("Cannot open file. \n");
        exit(1);
    }
    fread(&ch,sizeof(int),1,fp); //read one character

    while(ch!=EOF){
            array_D[flagi]=ch; //electrode number
            fread(&ch,sizeof(int),1,fp);
            if(feof(fp))break;
            flagi++;
        }

    fclose(fp);
*/
    //prompt user to determine which electrode they wish to control


    move();


    //clear the voltage on all electrodes at the end and deinitialise the PCI card
    d=1000; //1s delay then deinitialise
    delay();
    clear();

    Deinitialise();

    printf("ch=%d. \n",ch); //check point
    printf("array_N[0][0]=%d. \n",array_N[0][0]); //check point
    printf("flagi=%d. \n",flagi);
```

```
        return 0;

    }

/*function for dispensing a droplet from a reservoir:
    procedure:
                    reservoir        neck electrode      target electrode
        1:              off                  on                      on
        2:              on                   off                     on
        3:              off                  off                     off

*/

void move(void)
{
    int i=0;
    //menu();
    flagi=0;


    do
    {
        for(i=0;i<4;i++) //refreshing 4 ports' output value
        {
            port = (array_N[flagi][i]-1)/5;     // calculation for the port the electrode refers to
            digit = array_N[flagi][i]-(5*port);   // calculation for the individual digit in the
port
            nOutV[port] = (1<<(digit-1))+nOutV[port];
        }
        d=1000;
        output();
        delay();
        clear(); //clear both nOutV and nOutVal
        flagi=flagi+1;
    }while(flagi<SC);

}


//menu function for input 4 electrode with 1 delay time
/*void menu(void)
{
    int temp_n = 0;
    int temp_d = 0;
    int i = 0;
    SC=0;

    do
    {
        for(i=0;i<4;i++)
        {
            printf("\nPlease enter the four subelectrode of a electrod you wish to turn on(enter
0 if absense ");
            printf("\nEnter 99 when you have finished:");
```

```c
            scanf("%d",&temp_n);
            if(temp_n==99)
            {
                    return;
            }
            array_N[SC][i]=temp_n;
        }
        printf("\nPlease enter the delay you wish to use (ms):");
        scanf("%d",&temp_d);
        if(temp_d==99)
        {
                return;
        }
        array_D[SC]=temp_d;
        SC++;

    }while(1);
}*/


//output refresh for all electrodes
void output(void)
{
    nOutVal=nOutV[0];
    OutputPIO0PortA();
    nOutVal=nOutV[1];
    OutputPIO0PortB();
    nOutVal=nOutV[2];
    OutputPIO0PortC();
    nOutVal=nOutV[3];
    OutputPIO1PortA();
    return;



}

void delay(void)
{
    //modified by Yifan 07Feb07 for switching frequency over 1KHz

        LARGE_INTEGER ticksPerSecond; //counter's accuracy on this PC in ses
        LARGE_INTEGER ticksPerMiliSecond; //counter's accuracy in msec
        LARGE_INTEGER tick; //total counter's tick after start counting

        LARGE_INTEGER time; //total milisec after start counting
        LARGE_INTEGER time_now; //total milisec till NOW

        //get the tick number for 1 second
        QueryPerformanceFrequency(&ticksPerSecond);
        //if one second 1000 tick, then one ms should be 1 tick
        ticksPerMiliSecond.QuadPart = ticksPerSecond.QuadPart/1000;

        //what time is it now?
        QueryPerformanceCounter(&tick);
        time.QuadPart = tick.QuadPart/ticksPerMiliSecond.QuadPart;
```

```
                do
                {
                        QueryPerformanceCounter(&tick);
                        time_now.QuadPart = tick.QuadPart/ticksPerMiliSecond.QuadPart;

                }while((time_now.QuadPart-time.QuadPart)<d);

        // 1 is 1 milisecond delay, can be other number of miliseconds

return;
}
/* previous delay
void delay(void)
{

        time_t start_time,cur_time;
        time(&start_time);
        do
        {
                time(&cur_time);
        }while((cur_time-start_time)<d);

        // 1 is 1 second delay, can be other number of seconds

return;
}

*/


//clear '0' function
void clear(void)
{
    nOutV[0] = 0;
    nOutV[1] = 0;
    nOutV[2] = 0;
    nOutV[3] = 0;
    output();
}


//Yifan's board initialise function:
void Initialise(void)
{
    BCT_DWORD dwStatus;
    char szErrorText[120]; //for checking the dwstatus and do error display
    int nIndex;

    // Initialise the four handles we are going to use: P0ABC and P1A
    // This is to initialise the handle structions we are going to put PCI card directions in
    // (e.g. for puting MEM addresses afterwards)
    dwStatus = BCTInitHandle(&nPciPio0PortAHandle);
```

```
//check point
//printf("PciPio0PortAHandle is: [%d]\n", nPciPio0PortAHandle);

if (dwStatus != BCT_OK)
{
    BCTErr2Txt(dwStatus, szErrorText);
    printf("BCTInitHandle returned: %s\n", szErrorText);
}
dwStatus = BCTInitHandle(&nPciPio0PortBHandle);

//check point
//printf("PciPio0PortBHandle is: [%d]\n", nPciPio0PortBHandle);

if (dwStatus != BCT_OK)
{
    BCTErr2Txt(dwStatus, szErrorText);
    printf("BCTInitHandle returned: %s\n", szErrorText);
}
dwStatus = BCTInitHandle(&nPciPio0PortCHandle);

//check point
//printf("PciPio0PortCHandle is: [%d]\n", nPciPio0PortCHandle);

if (dwStatus != BCT_OK)
{
    BCTErr2Txt(dwStatus, szErrorText);
    printf("BCTInitHandle returned: %s\n", szErrorText);
}
dwStatus = BCTInitHandle(&nPciPio1PortAHandle);

//check point
//printf("PciPio1PortAHandle is: [%d]\n", nPciPio1PortAHandle);

if (dwStatus != BCT_OK)
{
    BCTErr2Txt(dwStatus, szErrorText);
    printf("BCTInitHandle returned: %s\n", szErrorText);
}

// Get the driver to fill out the board ID structure for initialisation
dwStatus = BCTGetBoardId(&pPciPioBoardId, PCI_PIO, 0);

//check point
//printf("PciPioBoardId is: [%d]\n", pPciPioBoardId);

if (dwStatus != BCT_OK)
{

    BCTErr2Txt(dwStatus, szErrorText);
    printf("BCTGetBoardId returned: %s\n", szErrorText);
}

// Our program is to use PIO0Port_ABC and PIO1Port_A to be Output only
// So PIO0_AB and PIO1_A should be set to OUTPUT, and PIO0_C to OUTOUT for 8bit
```

output

```
    // Mode 0 is going to be used, PIO1_BC is NOCARE
    // This is to write the setting registers in the PCI Card
    dwStatus = BCTInit8255Modes(&pPciPioBoardId, 0, MODE_0, OUTPUT, OUTPUT,
OUTOUT);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTInit8255Modes returned: %s\n", szErrorText);
    }
    dwStatus = BCTInit8255Modes(&pPciPioBoardId, 1, MODE_0, OUTPUT, NOCARE,
NOCARE);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTInit8255Modes returned: %s\n", szErrorText);
    }


    // Open the handles that will be used by the Digital Output calls we will make
    // This is to give the direction (e.g. address in MEM) to the PCI card for our variables
    dwStatus = BCTOpen(&nPciPio0PortAHandle, &pPciPioBoardId, BCT_8255, 0,
BCT_PORT_A);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTOpen returned: %s\n", szErrorText);
    }
    dwStatus = BCTOpen(&nPciPio0PortBHandle, &pPciPioBoardId, BCT_8255, 0,
BCT_PORT_B);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTOpen returned: %s\n", szErrorText);
    }
    dwStatus = BCTOpen(&nPciPio0PortCHandle, &pPciPioBoardId, BCT_8255, 0,
BCT_PORT_C);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTOpen returned: %s\n", szErrorText);
    }
    dwStatus = BCTOpen(&nPciPio1PortAHandle, &pPciPioBoardId, BCT_8255, 1,
BCT_PORT_A);
    if (dwStatus != BCT_OK)
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTOpen returned: %s\n", szErrorText);
    }


    // Allocate some space and fill in the buffer structure so that we
    // have data for the paced output, not necessary currently-----Yifan
    dwStatus = BCTAllocate(&pPioBuffer, 256);
    if (dwStatus != BCT_OK)
    {
```

```c
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTAllocate returned: %s\n", szErrorText);
        }
    for (nIndex = 0; nIndex < 256; nIndex++)
    {
            pPioBuffer -> Buffer[nIndex] = nIndex;
    }
}


/* ------------------------------------------------------------ */
/* Deinitialise - Close the board id structure and the          */
/*                    handles that we have been using.          */
/* ------------------------------------------------------------ */

void Deinitialise(void)
{
    BCT_DWORD dwStatus;
    char szErrorText[120];

    // Make sure that the memory we have been using for the pacer
    // is released
    dwStatus = BCTRelease(&pPioBuffer);
    if (dwStatus != BCT_OK)
    {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTRelease returned: %s\n", szErrorText);
    }

    // Close all the four handles
    dwStatus = BCTClose(&nPciPio0PortAHandle);
    if (dwStatus != BCT_OK)
    {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTClose returned: %s\n", szErrorText);
    }
    dwStatus = BCTClose(&nPciPio0PortBHandle);
    if (dwStatus != BCT_OK)
    {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTClose returned: %s\n", szErrorText);
    }
    dwStatus = BCTClose(&nPciPio0PortCHandle);
    if (dwStatus != BCT_OK)
    {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTClose returned: %s\n", szErrorText);
    }
    dwStatus = BCTClose(&nPciPio1PortAHandle);
    if (dwStatus != BCT_OK)
    {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTClose returned: %s\n", szErrorText);
    }
```

```c
        // Release the board ID structure
        dwStatus = BCTReleaseBoardId(&pPciPioBoardId);
        if (dwStatus != BCT_OK)
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTReleaseBoardId returned: %s\n", szErrorText);
        }
}

//Output functions ----Yifan
void OutputPIO0PortA(void)
{
        BCT_DWORD dwStatus;
        char szErrorText[120];   //for checking the dwstatus and do error display

        //Output the value to PIO_0 Port_A
        //check point
        //printf("OutVal=[%d]", nOutVal);

        dwStatus=BCTWritePort(&nPciPio0PortAHandle, nOutVal);
        if (dwStatus == BCT_IO_PENDING)
        {
            dwStatus=BCTWait(&nPciPio0PortAHandle, INFINITE);
        }
        if ((dwStatus != BCT_OK) && (dwStatus != BCT_IO_PENDING))
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTWritePort returned: %s\n", szErrorText);
        }
        return;
}


void OutputPIO0PortB(void)
{
        BCT_DWORD dwStatus;
        char szErrorText[120];   //for checking the dwstatus and do error display

        //Output the value to PIO_0 Port_B
        //check point
        //printf("OutVal=[%d]", nOutVal);

        dwStatus=BCTWritePort(&nPciPio0PortBHandle, nOutVal);
        if (dwStatus == BCT_IO_PENDING)
        {
            dwStatus=BCTWait(&nPciPio0PortBHandle, INFINITE);
        }
        if ((dwStatus != BCT_OK) && (dwStatus != BCT_IO_PENDING))
        {
            BCTErr2Txt(dwStatus, szErrorText);
            printf("BCTWritePort returned: %s\n", szErrorText);
        }
        return;
}
```

```c
void OutputPIO0PortC(void)
{
    BCT_DWORD dwStatus;
    char szErrorText[120];   //for checking the dwstatus and do error display

    //Output the value to PIO_0 Port_C
    //check point
    //printf("OutVal=[%d]", nOutVal);

    dwStatus=BCTWritePort(&nPciPio0PortCHandle, nOutVal);
    if (dwStatus == BCT_IO_PENDING)
    {
        dwStatus=BCTWait(&nPciPio0PortCHandle, INFINITE);
    }
    if ((dwStatus != BCT_OK) && (dwStatus != BCT_IO_PENDING))
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTWritePort returned: %s\n", szErrorText);
    }
    return;
}

void OutputPIO1PortA(void)
{
    BCT_DWORD dwStatus;
    char szErrorText[120];   //for checking the dwstatus and do error display

    //Output the value to PIO_1 Port_A
    //check point
    //printf("OutVal=[%d]", nOutVal);

    dwStatus=BCTWritePort(&nPciPio1PortAHandle, nOutVal);
    if (dwStatus == BCT_IO_PENDING)
    {
        dwStatus=BCTWait(&nPciPio1PortAHandle, INFINITE);
    }
    if ((dwStatus != BCT_OK) && (dwStatus != BCT_IO_PENDING))
    {
        BCTErr2Txt(dwStatus, szErrorText);
        printf("BCTWritePort returned: %s\n", szErrorText);
    }
    return;
}
```