Amorphous Silicon Memory Devices: the forming process and filamentary conduction.

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A thesis submitted for the degree of Doctor of Philosophy at the University of Edinburgh

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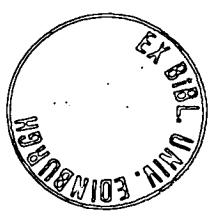

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Abstract

The electrical properties of hydrogenated amorphous silicon (a-Si:H) memories in both the unformed and formed states, have been investigated.

It has been found that conduction in unformed p^+-type samples is contact limited at room temperature for applied biases of less than 3-4V. The dependence of the device current on voltage and current has been analysed in terms of conduction across the Schottky contacts at the a-Si:H to metal interfaces. It has been proposed that the electro-forming of these samples gives rise to a conductive filament that penetrates both Schottky barriers.

Measurements of the conductance of formed p^+-n-i samples at 4.2Kelvin strongly indicate that in these samples the filament extends continuously through the a-Si:H film. The observation at 4.2K of superconductivity in samples with Al top contacts and of anomalous zero bias resistance peaks in samples with Cr, Fe and Au top contacts is thought to be evidence of metal injection from the electrodes into the filament. Investigations of the forming process in n^+-type devices in which the metal electrodes had been replaced by conductive silicon suggests that the migration of metal into the a-Si:H film may not just be a consequence of forming but may instead be instrumental in initiating it. Simulations of the temperature increase in the filament occuring during forming imply that it it highly probable that in parts of the filament the dehydrogenation and crystallisation temperatures of the a-Si:H will be exceeded.

Dedication

I would like to dedicate this thesis to the memory of Patrick St.John-Ives. (Patrick died in May, 1989 aged 27).

Acknowledgments

There are many people whose contributions to this thesis deserve acknowledgment and thanks. In particular I am indebted to my supervisors Prof. Alan Owen and Dr. Tony Snell and to my collegues Dr. Janos Hajto, Dr. Steven Reynolds, Dr. W. K. Choi, Prof. Peter LeComber and Mr. Mervin Rose for their encouragement and assistance throughout.

I am also most grateful to the University of Dundee for their considerable work in providing samples.

Final thanks go to Dr. George Scott, Dr. Peter Hockley and others at BP Research Centre, Sunbury for their support of and contributions to the project.

Declaration

This thesis is the original composition of the author's work, unless stated otherwise, and has not been submitted previously for any other degree.

Contents

Chapter 1

Introduction

1. **Introduction**

References

1. Introduction

The subject of this thesis is memory switching in electroformed thin films of hydrogenated amorphous silicon (a-Si:H).

Memory switching was first observed in a-Si:H at Edinburgh University in 1982[1] This was in thin film devices with a p+-n-i structure, where p+ denotes heavily doped p-type a-Si:H, n is n-type and i is undoped. It soon became obvious that the switching characteristics of these devices were potentially well suited to applications in the field of digital non-volatile memories i.e. the high resistance Off state and the low resistance On state differed in conductance by a factor thousand , both high and low states were apparently permanent until reprogrammed and the switching was polarity dependent, fast (<10ns) and required voltages of less than 5V.[2,3]

Since these initial discoveries the attempts to produce a reliable memory have, however, been frustrated by the failure to gain a clear understanding of the switching mechanism involved. What has become clear is that structures other than the p+-n-i configuration, for example p+-i, p-i-n and most recently single layers of p+, n+ or i material, all yield memory switching with varying degrees of success.[4] The presence of an a-Si:H heterojunction does not, therfore, appear to be a necessary criteria for switching. Of greater importance to switching, however, are the changes taking place in the device during the initial electroforming stage. This process, achieved by applying sufficiently large volatge pulses across the device, has been shown to give rise to a highly conducting filament with a diameter <0.5μm. Conduction in the low resistance On state of the devices has been found to be take place almost exclusively along this filament. In the high resistance Off state, however, the device resistance shows some dependence on the area of the device indicating that the filament resistance is now sufficiently high for a significant part of the current to pass through the surrounding bulk material. The action of switching appears, then, to be the mechanism by which the

resistance of the filament or possibly material close to the filament, is changing as a result of switching voltage pulses.

This thesis sets out to investigate a number of aspects of the physical and electrical properties of the filament. Following the first three chapters which review switching in thin films, switching in a-Si:H and the basic properties of a-Si:H ,the experimental part of the thesis follows three distinct strands. In chapters 6 and 7 the elctrical properties of the unformed and the formed devices are compared making use of static I-V vs. temperature measurements and a.c. capacitance and conductance measurements. Observations of the forming process itself are also described in these chapters. From these observations some general conclusions can be made about the conduction processes in both the unformed and formed devices and from the latter one can make some deductions about the likely composition of the filament. The second strand to the work, dealt with in chapter 8, looks at the role played by the contacts in the forming process. It has long been speculated both within this project and by many other workers in related fields that filament formation involves the migration of metal from the electrodes in to the dielectric film. To investigate this possibility devices with crystalline and micro-crystalline silicon contacts have been made and their forming characteristics compared to those devices with metal contacts. It appears from these experiments that the contact metal does, indeed, play an active role during forming.

The third and final aspect to the work attempts, by means of numerical simulations, to estimate the temperature increases occuring in the filament during forming and switching. The high current density associated with filamentary conduction can cause Joule heating sufficient to crystallise or even melt the amorphous material. Indeed many switching mechanisms are based on reversible thermal processes, such as the amorphous to crystalline transition. It is of importance to be able to predict the temperatures attained within the filament of the a-Si:H device during normal opera-

tion. As, in practice, it is difficult to measure the internal temperature of the filament I have made use of a computer model to simulate the conditions of heat generation and loss. These calculations reveal that temperatures in excess of the crystallisation and melting temperature are feasable during forming if not during switching.

The final chapter, no. 10, is a discussion and summary of all the work described in the thesis.

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Chapter 2

Switching in thin films

2. Introduction

One the most remarkable features of switching in thin films is the wide range of materials in which these effects have been observed. The list is extensive including TiO,[1,2] chalcogenide glasses,[3] ZnSe,[4,5] SiO,[6,7] SiO_2 doped with transition metals,[28] a–Si:H,[8] NiO,[9] ZnTe,[10,11] metal semiconductor junctions,[12,13] Langmuir-Blodgett films[14] and more. Yet despite the apparent ease with which switching can be induced in thin films, in a great many cases arriving at a clear and detailed mechanism for the switching process has proved rather more difficult. In this chapter I have tried to outline the rudimentary aspects of switching, introducing the processes required to achieve switching, the different types of switching and the mechanisms that are used to account for these effects; the interested reader is also refer to a number of the good reviews of switching effects to be found in the literature [15,16,17,18]. The final sections give examples of switching that are of particular relevance to the work reported in this thesis.

2.1. The device structure

Most thin film switching devices are two terminal sandwich structures similar to that shown in fig.2.1. The dielectrics vary in thickness from a few nm to a few μm and the device areas generally range from $10^{-2}cm^2$ to $10^{-6}cm^2$. The contacts are usually made of metal deposited by evaporation, sputtering or sometimes metal loaded pastes are used. Substrates of semiconducting materials have also been used as the bottom contact.

2.2. Forming:the process of inducing switching

Newly fabricated devices rarely show switching effects without an initial modification of their electrical make-up. This modification process which is usually performed

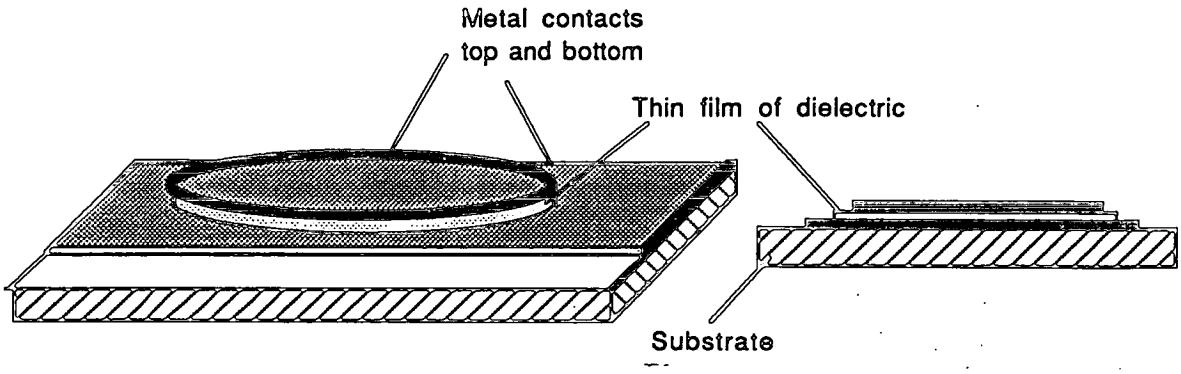

Fig.2.1 Sandwich *structure of a thin film switching device. The switching film thickness range from tens of Angstroms to a few micrometers.*

at the start of the device's life, is referred to as 'forming'. It is achieved by the application of suitable voltage pulses and invariably results in an irreversible change in the device's electrical characteristics, often with a sharp decrease in the overall terminal resistance.

The physical processes involved in forming depend largely on the thin film itself, the device structure and in some cases the electrode material. The physical changes that result can be structural, involving the movement of material from one part of the device to another,[6,11,9] they can involve a change of phase of the material such as the crystallisation of amorphous material[3] or they can be electronic in nature when a quasi-permanent change in the occupancy of some electronic states takes place.[5] The changes can occur throughout the bulk of the film[7] or in localised regions.[11] A common localised effect is the formation of a filament of highly conductive material that extends at least part of the way through the device. Although the filament may have a cross-sectional area many times less than the device area the effective conductance along its path is often so much higher than that of the remainder of the device that it becomes the preferred current path.[19] There are many reports of filament formation with a variety of processes cited to account for their presence including the crystallisa-

tion of an amorphous thin film,[3] stoichiometric changes,[9] diffusion of the electrode material in to the film[6,11] and the ionisation of deep traps.[5] Reports of bulk changes occuring during forming are less common; one example is the bulk diffusion of the electrode material into the thin film.[7]

The modifications caused by forming play such an intimate part in the subsequent switching that without a reasonably clear understanding of them the elucidation of the switching mechanism becomes a difficult task. Regrettably there is disagreement within the literature on many aspects of forming; as Dearnaley[20] notes in his review of the subject 'there are almost as many theories as there are theorists'.

2.3. Current - voltage characteristics of switching devices

Switching in thin films is associated, explicitly or implicitly, with negative differential resistance (NDR).[18] Two types of NDR exist, current controlled NDR (CCNDR) shown in fig.2.2a and voltage controlled NDR (VCNDR) shown in fig.2.2b. Conduction in CCNDR involves the creation of material filaments in which the current density differs from that found in the surrounding material. This often involves the creation of a filament of material that through Joule heating has become significantly warmer than the bulk material.[21,16,22] In the case of VCNDR the form of the I-V characteristics is associated with domains of different field strengths.[23] Both types of curves, as will be seen in the following sections, can give rise to switching.

2.4. Switching: memory and threshold

Switching devices demonstrate at least two states distinguishable by a difference in their resistances: the low resistance On state and the high resistance Off state. Switching phenomena fall into one of two categories:

Threshold switching; in which continuous electrical power is required to maintain at least one of the two states, or

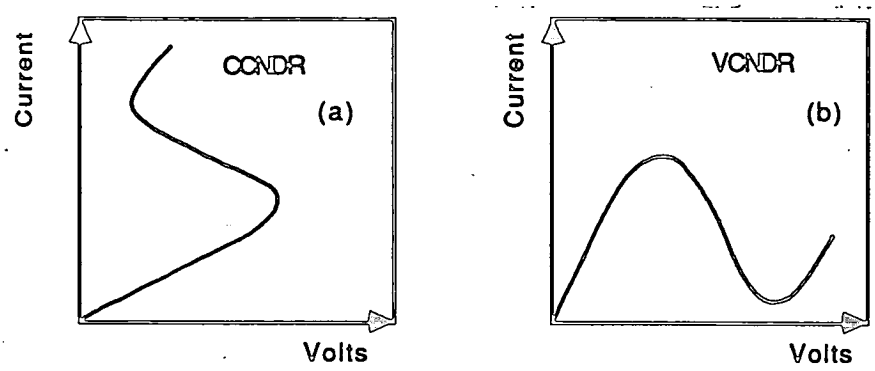

Fig.2.2. I-V characteristics showing negative differential resistance;. (a) current controlled (CCNDR) or S-type and (b) voltage controlled (VCNDR) or N-type.

Memory switching; in which both On and Off states can be preserved without power.

2.4.1. Threshold switching

Fig.2.3 shows a schematic of two sets of switching characteristics for threshold devices showing CCNDR.

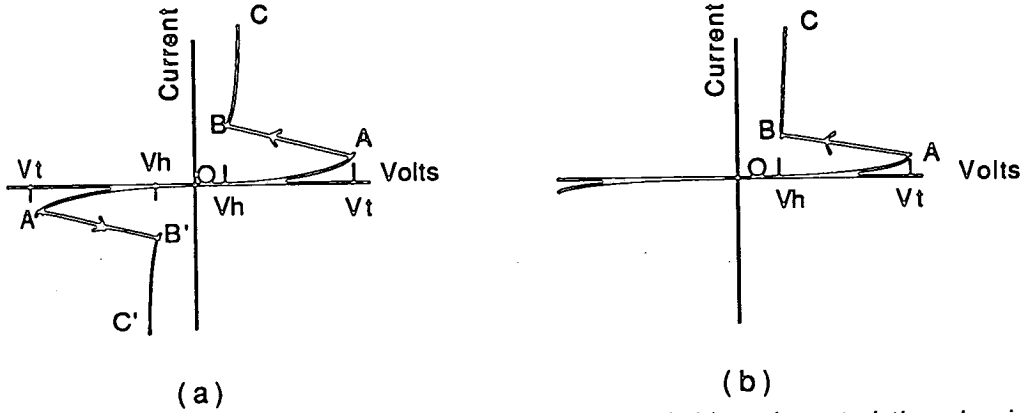

Fig.2.3. Symmetrical (a) and asymmetrical (b) threshold switching characteristics showing the Off states,(OA) ,and the On states ,(BC). The OFF to ON transition occurs at Vt, and the ON state will be maintained as long as the holding voltage, Vh ,is exceeded. The asymmetric characteristics, (b), show a low resistance state in one quadrant only.

In both sets of curves as the bias is increased from zero, section OA of the Off state I-

V curve is followed until the threshold voltage, V_t, is reached . At this point there is a sudden drop in the device resistance and the I-V curve moves along the load line to section BC which is the On state. The device stays on curve BC as long as the holding voltage, V_H is exceeded. If the applied voltage falls below V_H the device undergoes another sudden change in resistance and reverts to the Off state. This type of switching action is described as 'volatile' as the device, in this case, reverts to the Off state in the absence of a holding voltage. Applying negative voltages in cases where the switching characteristics are symmetrical, as in fig.2.3a, produces a similar jump to a high conducting state, B'C'. In many cases threshold devices only show a high conducting state for one bias direction, as depicted in fig.2.3b.

2.4.2. Memory switching

In contrast to threshold behaviour, devices showing memory switching remain indefinitely in either the On or Off states without the need for a holding voltage. Fig.2.4 shows three states of memory devices labelled 'On', 'Off' and 'Intermediate' for two types of devices one showing symmetrical and the other asymmetrical switching characteristics. Switching between these states is achieved by applying the appropriate write (Off to On) or erase (On to Off) voltage pulse. The write and erase pulses differ from each other by at least one parameter such as their magnitude, length, leading edge rise time or trailing edge fall time and in addition the polarity of the write and erase pulses may be of the opposite sign.

It is common when describing switching phenomena to talk in terms of On and Off states, but as fig.2.4 attempts to show, switching devices are not always rigidly bistable in their operation and intermediate states lying between the On and Off can occur.

Most devices, threshold or memory, can sustain many hundreds of cycles and the

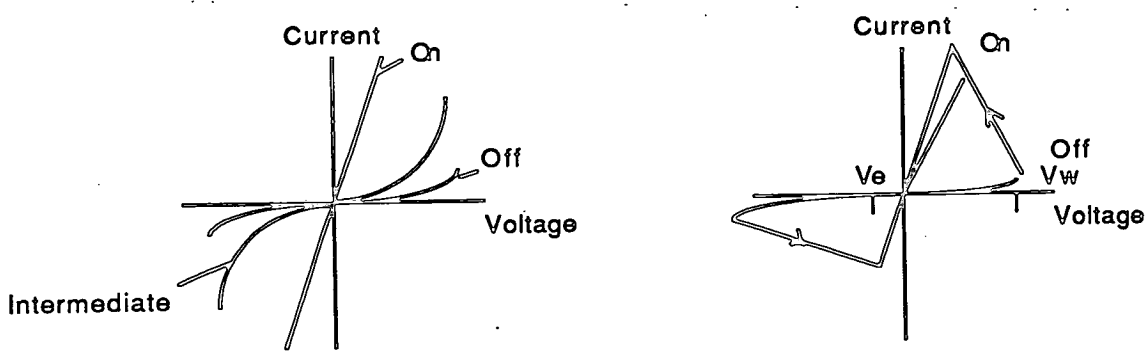

Fig.2.4. The dynamic I-V characteristics of a memory device with (a) symmetrical switching curves and (b) asymmetrical curves. In (b) the switching is polarity dependent with the OFF to ON transition occuring at a positive voltage Vw. The reverse transition back to the OFF state occurs at a negative voltage of Ve.

better ones up to 10^9 cycles before they fail. The commonest failure mode manifests itself in a device becoming stuck in one state.

2.5. Switching mechanisms

The models devised to explain threshold and memory switching in thin films are of three types; Electronic, Thermal and Electrothermal. These are discussed in turn below.

2.5.1. Electronic models for switching

In an electronic model the difference in conductance between the On and Off states is attributed to the effect of a difference in the electronic nature of the device. In the case of threshold switching the Off to On transition is generally explained in terms of a change from a low conducting transport mechanism to one with a higher resultant conductance. An example of this is the model suggested by Henisch et al.[24] for threshold switching in chalcogenide glasses in which it is proposed that double injection of

carriers in the Off state gives rise to space charge regions near the electrodes. This can cause an instability and a transition to the On state.

Electronic models for memory switching rely on the long term storage of charge to account for the non-volatile nature of the switch. The most commonly proposed charge storage sites are traps, either in the bulk or at an interface between two dissimilar materials. A necessary characteristic of such traps is that they have a release time comparable to the retention time of the memory which may range from a few hours to many months. Wherever and however the charge is stored in the device it can affect the conductance of the device in a number of ways. When stored in the bulk or at interfaces it can cause band bending which in turn modifies the conductance.

Simmons and Verderber[7] have used an electronic model to explain their observations of memory switching in thin (20 to 300nm) films of silicon monoxide (which they refer to as SiO) prepared by vacuum deposition, fitted with gold electrodes. After the devices had been formed, a process during which, the authors suggest, gold ions migrate into the bulk of the SiO, the I-V characteristics of the devices showed VCNDR as shown in fig.2.5.

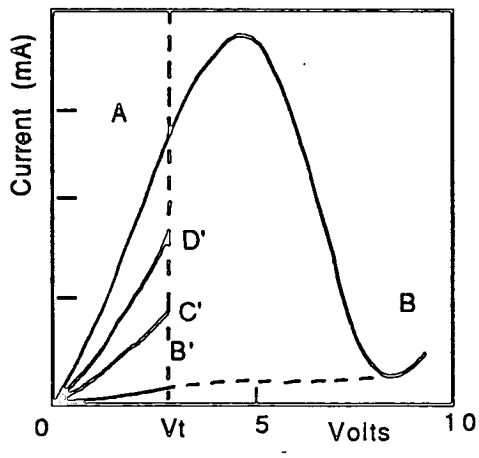

Fig.2.5. Dynamic I-V characteristics of a thin film SiO memory device. If 8V is applied to the device and the trailing edge of the pulse is <0.1ms the next I-V curve will be along 0B'. If the threshold voltage Vt is exceeded the device reverts to the high conducting state of 0A. A continuum of states between OA' and OB' could be accessed (e.g. OC' and OD') by applying the correct voltage pulses. The life time of each state appeared to be of the order (Fig. taken from ref. 7). of two weeks.

The device could be switched to a continuum of resistance states (see fig.2.5) which

persisted for a few weeks. Simmons and Verderber suggested that the switching behaviour of this VCNDR device arose from charge trapping in the bulk of the SiO which in turn modified the conductance of the metal/SiO barrier.

Hovel and Urgell[5,4] have also suggested an electronic model to explain their observations of memory switching in epitaxial ZnSe films grown on crystalline Ge. The I-V characteristics of the devices were implicitly of the CCNDR type. The switching characteristics are shown in fig.2.6a. According to their model, the band diagram for the device in the high resistance state resembles that shown in fig.2.6b; the current flow through the device is limited mainly by the high-resistance ZnSe layer. In the On state they suggest the band diagram is modified to that of fig.2.6c. The barrier at the ZnSe/Ge interface has been narrowed by the ionisation of traps at the interface from neutral to +1 thereby permitting easy tunnelling through it. They also suggest that one or more highly conductive filaments are formed through the ZnSe layer and that this also occurs by electron emission from neutral traps.

2.5.2. Thermal models for switching

In thermal and electrothermal models the temperature increase associated with Joule heating is regarded as the principal driving force of the switching mechanism.[25,17] The explanation of threshold switching in terms of thermal processes often involves the feed back loop shown in fig.2.7.[26] This shows how, in materials with a thermally activated conduction process, thermal runaway can occur causing a sharp drop in the device resistance. Referring back to the switching curves in fig.2.3, in this type of model the threshold voltage, V_t, corresponds to the onset of the thermal runaway.

In the case of memory effects the elevated temperatures are seen as being the cause of atomic movement or re-ordering. These atomic rearrangements are 'frozen'

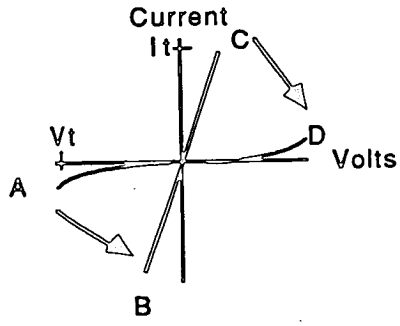

Fig.2.6a Static I-V of nZnSe-pGe memory device. Switching occurs from A to B at a voltage threshold Vt and back again from C to D at a threshold current It. (After ref5)

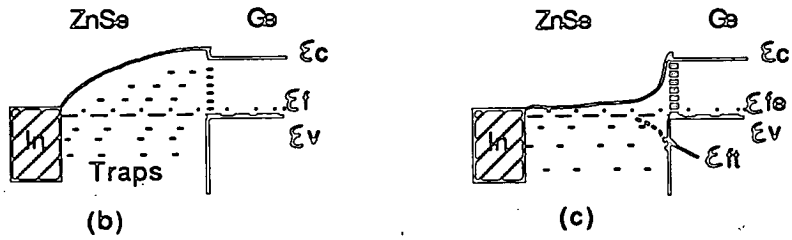

Fig.2.6b and c Energy band diagrams of nZnSe-pGe heterojunctions at zero bias, (b) in the high resistance state and (c) in the low resistance state. (After ref. 5)

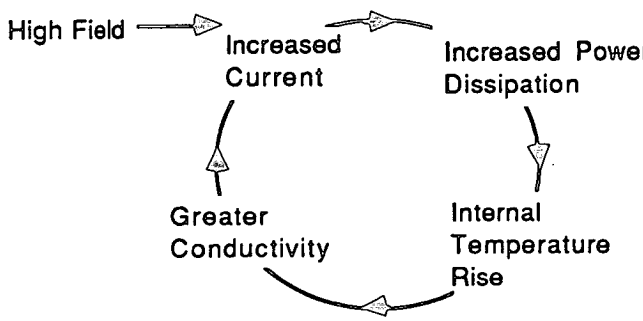

Fig.2.7. The feedback loop leading to thermal runaway in thin films with thermally activated conduction processes.

in place once the switching pulse is removed and the device has cooled making this an attractively easy means of explaining the long life time of memory states. Models of this type are most often proposed where conduction has been shown experimentally to be filamentary. This is because the current densities in a filament during a switching operation can cause sufficiently high temperatures to melt the filament material. This permits a range of phase change and mass transfer processes that are well suited to the

explanation of memory effects. Perhaps the most thoroughly investigated thermal switching mechanism is that found in chalcogenide glasses.[26,3,27,21] During initial forming pulses a filament of material crystallises; this normally happens near the centre of the device where the highest temperatures are attained. This modified material has a higher conductivity than the bulk and so becomes the preferred current path during subsequent voltage pulses. The switching process , according to the generally accepted model, is illustrated in fig.2.8.

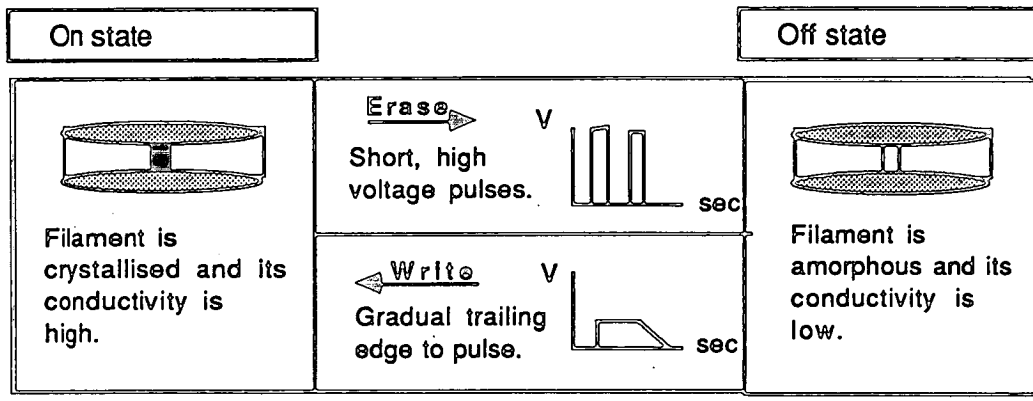

Fig.2.8. The switching process in chalcogenide glass memory devices. In the erase operation large voltage pulses with steep trailing edges are applied. These melt the crystalline filament causing it to solidify in an amorphous form. To write the device pulses with more gradual trailing edges are used. These melt the filament too but allow the material to solidify in a crystalline form.

The important variable is the rate of cooling of the filament material which as shown above can be controlled by the voltage pulse shape. Very rapid cooling from above the melting point of the chalcogenide favours solidification in an amorphous phase whereas gradual cooling gives time for crystal growth to occur.

Manhart[6] has proposed a thermal model to explain memory switching in SiO. In these samples a forming pulse was again used to reduce the device resistance from its initial value of 10^9 to 300Ω. According to Manhart's model, the forming process gives rise to temperature increases sufficient to encourage silver from the electrodes to

migrate into the SiO to produce a metal filament. Thus the linear I-V characteristics and positive temperature coefficient of resistance of the low resistance state are accounted for. Two models are put forward for the subsequent switching mechanism, as illustrated in fig.2.9.

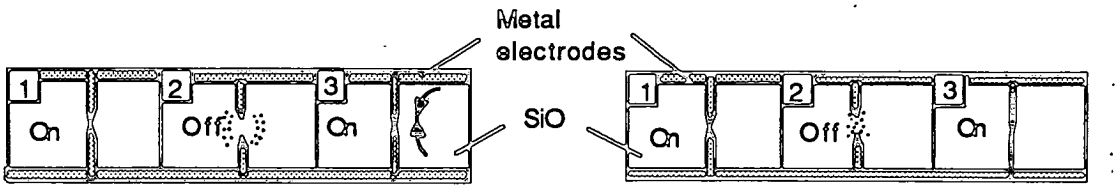

Fig.2.9.a. Suggested switching mechanism no.1. An erase pulse (10V, trailing edge < 1000ns) melts the metal filament [1]. The metal disperses into the SiO breaking the link [2]. To remake the filament a write pulse (6-8V, trailing edge > 0.1ms) encourages more metal from the electrodes to enter.

Fig.2.9.b. Suggested switching mechanism no.2. The erase pulse melts the metal filament[1]. The rapid cooling as the pulse is removed creates an amorphous, high resistance metal:SiO mixture[2]. To write, the material is re-melted then cooled more gradually. The difference in the freezing points of the metal and the SiO cause them to seperate re-forming the filament[3].

Memory switching in thermally grown microcrystalline NiO has been reported by Gibbons and Beadle.[9] They too suggest that a metallic filament is formed in their samples, not by the diffusion of metal from the electrodes, but by the collection of nickel atoms at a structural defect in the oxide.They propose that this occurs during the forming stage of the device when a filament of material becomes sufficiently hot for this stoichiometric change to take place. The switching characteristics of the formed device are outlined in fig.2.10 below.

The final example of a thermal switching model I wish to discuss is that proposed by Ota and Takahashi for ZnTe.[11] Following a by now familiar pattern their model involves filaments made in this case by the injection of metal from the electrodes. In the On state conduction is along one of these filaments. To regain the Off state the filament is ruptured by melting. Returning to the On state is by the formation of a

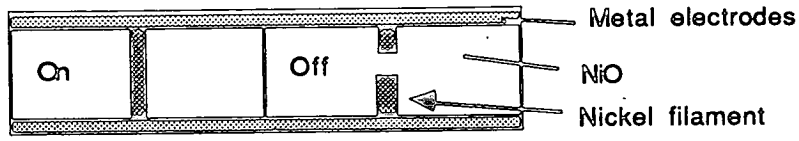

Fig.2.10. Suggested switching mechanism in NiO. Forming causes Ni from the bulk to conglomerate to produce a filament. The erase pulse (150mA,10ns) re-oxidises the Ni to resistive NiO thus breaking the filament.The write pulse (200V,40ms) causes the re-migration of NiO into a filament.

completely new filament and not by healing the old: the life time of this type of device is obviously rather limited.

2.5.3. Electrothermal models of switching

This type of switching model encompasses aspects of both purely thermal mechanisms and purely electronic mechansims. As with the thermal models described in the previous section electrothermal models are usually invoked where conduction is filamentary as it is in these cases that large local temperature increases can occur. In contrast to a purely thermal model where Ohmic conduction mechanisms are assumed to prevail, in an electrothermal model the conduction mechanism is strongly non-Ohmic. When the bias across the sample is increased there are, therefore, two mechansims by which the current in the device increases; (1) the field strength dependence of the conductivity and (2) self-heating which enhances conduction by thermally activated processes. In a simple thermal mechanism only the second of these is assumed to be relevant and in a purely electronic mechanism only the first is of importance. At an appropriate applied bias a temperature is attained sufficient to initiate switching of either the threshold or memory type. The final stages of the switching mechanisms can be generally similar to those described in the previous section on thermal models i.e. memory switching might involve compositional or structural rearrangements and thres-

hold switching the creation of a sustainable hot filament.

2.6. Summary

The phenomenon of switching in thin films has been reviewed. There are two distinct types of switching: (1) Threshold switching, in which a continual supply of power is required to operate the device, and, (2) Memory switching, in which both On and Off states can be retained for long periods without the consumption of power.

Many types of switching devices require an initial forming process to initiate switching; this process is usually performed using a voltage pulse and can give rise to electronic, structural or compositional changes to the device. Despite the importance of the forming process in determining the subsequent switching a detailed knowledge and understanding is absent in many cases. A common product of the forming stage is a filament of highly conductive material. The high conductance of the filament has been attributed to one or more of several processes e.g. crystallisation of the amorphous material, the injection of metal into the thin film, the compositional rearrangement of compounds and the ionisation of the filament material.

The switching mechanisms of both threshold and memory devices are based either on electronic processes, thermal processes or a mixture of the two - electrothermal processes. For the case of memory effects, electronic processes account for the longevity of the memory state in terms of charge trapping somewhere within the film. Thermal and electrothermal models for memory switching usually assume that the elevated temperatures caused by the current flowing through the device initiate some material movement or cause a phase change in a part of the thin film material that becomes 'frozen' in to place once the temperature falls. Thermal models are frequently proposed when conduction is filamentary, as the high current density enables high temperatures to be attained which permit the necessary changes.

The speed of the switching transitions vary from device to device and cover a range from <10ns to >1ms. There is no indication from the reports of memory switching whether electronic switching processes are fundamentally any quicker than thermal processes.

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Chapter 3

Switching in amorphous silicon

3. Introduction

In the first half of this chapter the reports of both threshold and memory switching in a-Si:H are reviewed with particular emphasis being given to the properties of the memory device jointly under investigation at the Universities of Edinburgh and Dundee. In the second part of this chapter some of the recent unpublished results from these two groups and our colleagues at BP Sunbury are presented so as to place work reported in this thesis in context.

3.1. Switching in a-Si: published results

The earliest reports of switching in a-Si were made in 1970 by Feldman and Moorjani [1] and Moorjani and Feldman.[2] Their descriptions are primarily of threshold switching although they make a passing reference to memory effects. The devices they studied were made of electron beam evaporated a-Si fitted with Ti contacts; they did not require a forming stage to initiate the threshold switching. From this and further work reported by Feldman and Charles in 1974 [3] and Charles and Feldman [4] in 1975, it was established that the On state was associated with a filamentary region of heated a-Si extending at least part way through the device. An electrothermal model similar to those being used contemporaneously to describe threshold switching in chalcogenide glasses [5] was suggested as an explanation of switching in these a-Si devices.

Dey and Fong[6] and Dey [7] describe similar observations of threshold switching in Ti-Si-Ti devices. In contrast to the previous observations, however, they allude to a forming process occurring in their devices in so far that the initial switching voltage was higher than subsequent switching voltages. No specific details are given, however, of the changes brought about in the device by this initial switching.

In 1982 three publications appeared by, den Boer,[8] Gabriel and Adler,[9] and Owen et al.,[10] the latter being the first from the joint project between the Universities

of Edinburgh and Dundee. Den Boer's reports concerned threshold switching in n+-i-n+ sandwich structures of hydrogenated a-Si. He mentions the need for an initial forming process and that this gave rise to a permanent spot on the device several micrometers in diameter. This region, he suggests, acts as a nucleus for filamentary conduction in the On state.

Gabriel and Adler, working with notionally homogeneous layers of sputtered a-Si:H fitted with molybdenum contacts, reported no evidence of reversible switching in their devices and concluded that in contrast to amorphous chalcogenides, a-Si lacked the suitable electronic or structural properties for reversible switching.

The report by Owen et al. however, showed that in heterogeneous (p+-n-i) samples of a-Si:H prepared by RF glow discharge it was possible to observe reproducible memory switching. Three years later in 1985, Gangopadhyay et al. reported similar memory switching in p-n-i structures made of sputtered a-Si:H. [11] The observations reported in Owen et al.'s paper of 1982 and two subsequent publications by LeComber and Owen et al.[12,13] are outlined in the following sections.

3.1.1. Structure.

The earliest devices were made by depositing Al or Au top contacts with areas of about $1mm^2$ on to glow discharge a-Si:H prepared on stainless steel substrates. Later structures have been made to the design shown in fig.3.1 with the 'pore' diameter varying between 300 and 10μm and the total thickness of the a-Si:H varying between 0.5 and 1μm. The a-Si:H is variously doped to make devices with a p+-n-i, p+-n or p+-i structure.

3.1.2. Static I-V characteristics of the unformed device

The as-prepared I-V characteristic of the p+-n-i device, as shown in fig.3.2. is

rectifying as expected for a structure containing a p-n junction (the forward biased direction being when the p+ silicon is positively biased).

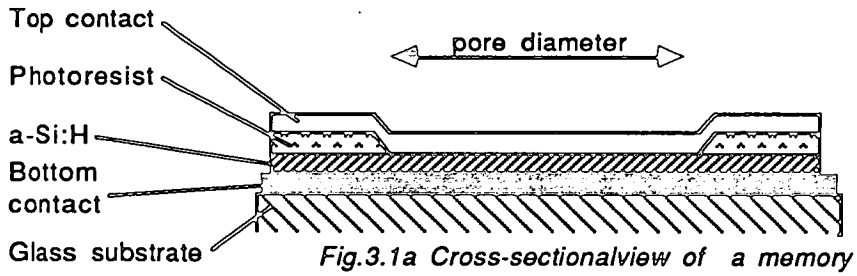

Fig.3.1a Cross-sectionalview of a memory device showing the 'pore' structure.

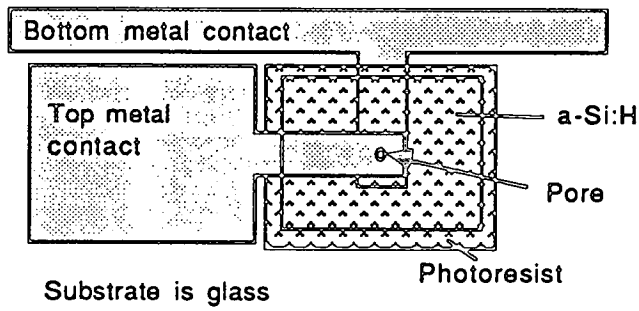

Fig.3.1b Plan view of the normal 'pore' structure

3.1.3. Forming

The devices require an initial forming stage. This is achieved by forward biasing the device to about 24V at which point it becomes unstable and switches to a non-volatile low resistance On state of less than 2kΩ. Forming does not necessarily occur the instant the forming pulse is applied but can involve a delay. This delay is found to be very sensitive to voltage as shown in fig.3.3. During the delay time the device current is found to remain constant at a level expected for the Off state with the appropriate voltage across the device.

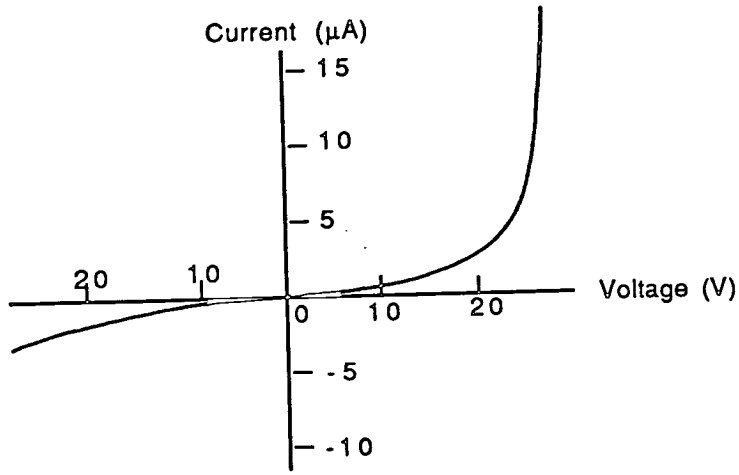

Fig.3.2 The static I-V characteristics of an unformed p+-n-i device measured at 30 ^{o} C. (After ref.12)

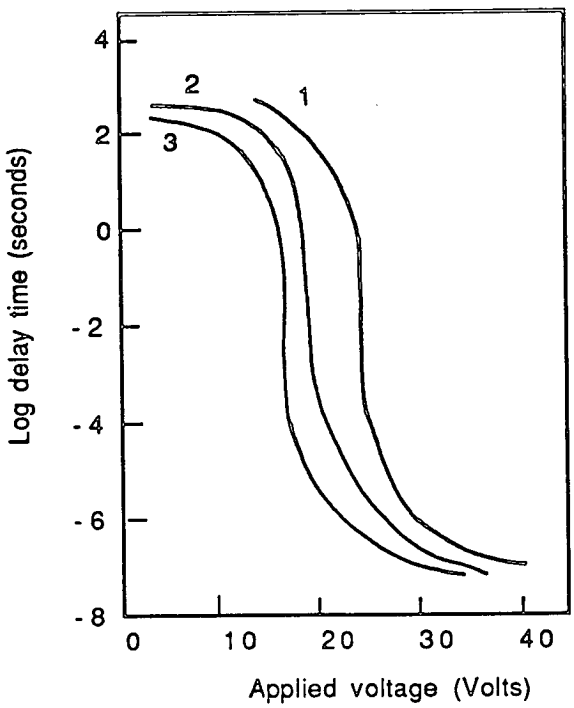

Fig.3.3 The delay time for forming of a typical p+-n-i device. measured at 30 ^{o}C (curve 1), 80 ^{o}C (curve 2), and 160 ^{o}C (curve 3). (After ref.12)

3.1.4. Filament

Forming is found to give rise to a highly conducting filament which, from measurements made using thermochromic liquid crystals, is shown to have a diameter of

less than 0.5μm. The composition and structure of the filament has not been determined with any great certainty but it was suggested that it may arise from the migration of metal from the electrodes into the a-Si:H.

3.1.5. Switching

The switching characteristics are shown in fig.3.4. The switching is polarity dependent with the On to Off transition occurring at a reverse bias threshold voltage, V_{thr}, and the opposite transition from Off to On occurring at a forward bias threshold V_{thf} ('forward' and 'reverse' bias are referred to the p-n junction i.e. reverse bias is when the p+ is negatively biased).

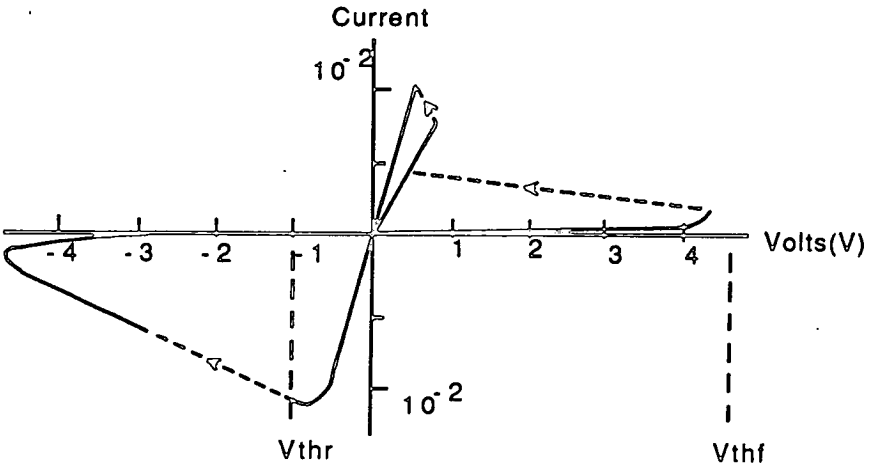

Fig.3.4 Complete static current - voltage characteristics of a formed a-Si p+-n-i device, showing the forward and reverse threshold voltages, Vthf and Vthr, respectively.

3.1.6. Switching speed

The erase operation appears to be instantaneous on the time scale of 1 ns. For normal operation pulses of 10 ns are used. The Write operation shows a delay time t_d which has an inverse exponential dependence on the Write pulse magnitude i.e. $t \propto exp(\frac{V}{V_0})$. Data presented in reference 13 shows the delay time varying between

100ns for a 5V Write pulse to 10ns for a 15V pulse.

3.1.7. On state

The resistance of the On state is less than 1kΩ and sometimes as low as a few tens of Ohms. The On state resistance is found to be independent of the device area and, thus, it has been assumed this state is associated with conduction along a filament. The temperature dependence of the On state resistance is weak, the resistance decreasing by only 10% as the temperature is increased from 230K to 400K.

3.1.8. Off state

In contrast to the On state, the Off state resistance scales inversely with area implying conduction is through the bulk and not preferentially along the filament. The temperature dependence of the Off state resistance is greater than the On state with the resistance decreasing by a factor of three as the temperature is increased from 230K to 400K.

3.1.9. Switching Energy

The energy dissipated during a switching transition has been estimated at between 10^{-8} and 10^{-6} J.

3.1.10. Volatility

Both the On and Off states are found to be effectively permanent. No appreciable change in the resistance of either state has been noticed in devices left unbiased at room temperature for 18 months, nor is any change seen in devices held at 95°C for 24 hours.

3.1.11. Mechanisms

Despite the considerable effort by both the Edinburgh and Dundee groups from 1982 to 1985 they were unable to establish with any certainty a mechanism that could satisfactorily account for the switching effect. The discussions of the mechanism generally ran along one of three lines; (1) Thermal models, (2) Charge trapping models and (3) Novel models involving atomic motion.

3.1.11.1. Thermal Models

A mechanism similar to that used to explain memory switching in amorphous chalcogenide devices, namely, the reversible creation and destruction of a crystalline filament (see §2.5.2/), has been dismissed for a number of reasons. These include (i) the difficulty such a model has in accounting for the observed polarity dependence of the switching, (ii) the switching energies of the a-Si:H devices ($<10^{-6}J$) were considerably lower than those found in chalcogenide devices ($10^{-4}-10^{-3}J$), (iii) the switching speed of the a-Si:H devices, typically $10^{-8}sec$, are much faster than those found in chalcogenide devices which generally require $10^{-3}sec$.

3.1.11.2. Charge Trapping

Analogies have been drawn between the structures and performance of the p+-n-i devices and crystalline silicon MISS devices. Although the MISS devices have only ever been found to exhibit threshold switching it has been tentatively suggested that the memory effect found in the a-Si:H devices are caused by charge storage in deep states at the i-type to n-type interface. It must be appreciated, however, that accounting for the very long life-time of the a-Si:H devices requires a trap with an exceptionally low release probability and that no such trap is known to exist in a-Si:H.

3.1.11.3. Other suggestions

It was tentatively suggested that field assisted diffusion of hydrogen within the a-Si:H network may give rise to switching effects; the polarity dependence of the switching could certainly be understood in terms of such a process. One possible mechanism might involve the hydrogen reversibly altering the height of the metal/a-Si:H barrier, a process that has been observed in ambient sensors.[14]

3.2. Recent unpublished results

A number of interesting observations have been made in recent months that, although unpublished, should be mentioned so as to provide a context for the new work described in this thesis. (Thanks are due to my co-workers for letting me make use of this information.) Possibly the most significant observation is that memory switching has been found to occur in homogenous a-Si:H devices i.e. in structures containing single layers of either i, n or p type a-Si:H.[15] The multilayer structure of the p+-n-i devices is not, therefore, necessary to the switching process. It is interesting to recall that Gabriel and Adler[9] failed to observe switching in homogenous a-Si:H prepared by sputtering in an H_2/Ar gas mixture.

Of the different types of a-Si:H investigated i.e. i, n and p type, it has been found that p+ material exhibits particularly reliable switching characteristics and for this reason has received the greatest share of interest. The forming process of these devices shows certain phenomenological differences from that of p-n-i devices even though the voltage pulses used in both cases are of comparable duration and magnitude. Unlike p-n-i devices which form directly to an On state the p+ devices can be formed to an Off state of 100kΩ to 1MΩ.[15] This process, because of its gradual nature, has become known as 'soft' forming. A subsequent switching pulse of the appropriate polarity results in the usual transition to the On state. Subsequent switching charac-

teristics are remarkably similar to those of the p-n-i devices: switching voltages of 2-4V are used, the On state can be as low as 1kΩ and the Off state as high as 1MΩ, the memory operation is polarity dependent, the memory states are stable for as long as they have been measured i.e. up to months. It has been found that the devices operate most successfully when the polarity of the Write pulse is the same as the forming pulse.

It has also become clear that devices of all types are not always strictly bi-stable in their operation but can exist in a continuum of resistance states lying between the On and Off states. These states can be accessed by using pulses that are a few hundreds of millivolts less than those required to make a direct On to Off or Off to On transition.[15]

The structure of the filament has continued to be a subject of investigation. Using X-Ray microprobe analysis on formed devices that have had their top contact removed, it has been established that metal from the contact is present in the silicon of the filament region.[16] This measurement, however, only probes the composition of the surface layer and there has been little success in finding a direct means of determining the filament composition below the surface.

A final observation of great relevance to the discussion of the switching mechanism is the apparent insensitivity of the memory states to the exposure to high energy radiation. A number of p-n-i devices in both On and Off states were exposed to 5Mrad of Co^{60} γ rays with no resultant change to the resistance of devices in either state. This seriously mitigates against switching mechanisms based on charge storage as it would reasonably be expected that radiation of this energy would cause the release of any trapped charge and so substantially alter the resistance of the On state and possibly even that of the Off state.

3.3. Summary

Early observations of both threshold and memory switching in a-Si have been reviewed. The details of memory switching reported by the Universities of Edinburgh and Dundee have been looked at in some detail. This work has focussed on sandwich structures with a-Si:H layers prepared by glow discharge between 50nm and 1μm thick. The earliest of these devices had a heterogeneous structure, such as p-n-i, but in recent times there has been a shift to samples with a homogenous a-Si:H layer, in particular p+ type a-Si:H.

The switching characteristics of the devices with heterogeneous and homogenous a-Si:H layers show many similarities: they require an initial forming process which is achieved with a voltage pulse of 10-15V and 100ns to 1s duration, switching is polarity dependent i.e. the Erase and Write operations require voltage pulses of the opposite polarity, the required switching voltages lie between 2V and 4V and the pulse width can be as short as 10ns for both Write and Erase operations, the On state is associated with a conductive filament that has a diameter of less than 0.5μm, both the On and Off memory states appear to remain indefinitely if the devices are left at room temperature with zero applied bias. Probably the largest difference in the behaviour of the single layer and multi-layer devices is in the forming process; the p-n-i devices invariably form in a single transition to an On state of a few kΩ whilst the p+ devices can be 'soft' formed to an Off state as well as being 'hard' formed to an On state.

Despite the considerable effort invested since the discovery of memory switching by the Edinburgh and Dundee groups in 1982, the switching mechanism remains unclear, to the extent that it has not even been decided whether it is a structural or electronic process. The discovery of switching in homogenous a-Si:H layers has been a helpful step in that it has made it clear that heterojunctions such as the n-p, i-p or i-n junctions are not necessary for switching, although the role of the metal-a-Si:H

heterojunction has yet to be established. The apparent indefinite life-time of the memory states, even at elevated temperatures and under exposure to radiation, strongly suggests a structural mechanism is at work. But if so how can the polarity dependence and high switching speed be accounted for? And is Joule heating in the filament playing a part in the switching mechanism? These and other questions will be addressed in this thesis.

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Chapter 4

Amorphous silicon: basic properties

4. Introduction

For more than a decade hydrogenated amorphous silicon (a-Si:H) has found considerable technological application in the fields of solar cells, Xerography , flat screen displays and others where large areas of silicon are required. There is a wealth of information accumulated on basic properties and this chapter provides a brief overview of some of this information dealing with methods of preparation, the density of states, conduction mechanisms and the a-Si:H to metal Schottky barrier. It also discusses the effects of elevated temperature on the structure of a-Si:H and the electrical properties of amorphous silicon/metal alloys, these last two subjects being of particular relevance to the discussion of switching and related phenomena in a-Si:H.

4.1. Preparation

There are three methods in common use for preparing a-Si:- evaporation in a high vacuum, cathodic sputtering and glow discharge (g.d.) decompostion of silane gas, the latter being the process used to prepare the silicon studied here and the one I shall concentrate on. A schematic representation of a g.d. chamber is shown in fig.4.1.

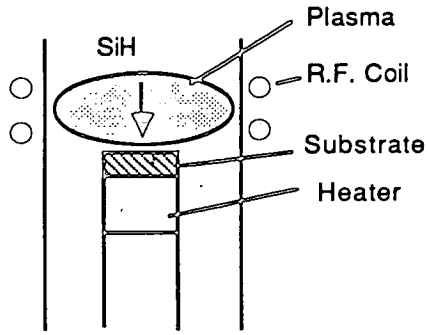

Fig.4.1 A schematic representation of the preparation of an a-Si specimen by glow discharge decomposition of silane. using inductive coupling.

Silane gas (SiH_4) is passed through the chamber where, under the stimulation of the radio frequency field, the silane gas decomposes into Si and Si-H fragments which are deposited at the heated substrate. Amorphous silicon prepared in this way contains between 8% and 50% atomic hydrogen, and is more accurately described as

hydrogenated amorphous silicon (a-Si:H). The electrical and optical properties, and the hydrogen content of g.d a-Si:H depend critically on the preparation conditions, in particular on the substrate temperature during deposition, the RF power, the reaction chamber pressure and of course the exact composition of the chamber gases.

Doping of a-Si:H is achieved by mixing, with the silane gas, diborane (B_2H_6) to provide boron as a p-type dopant or phosphine (PH_3) as an n-type dopant. The doping concentration of the a-Si:H films is determined by the relative concentrations of the silane and dopant gas. A useful feature of the doping technique is that the doping type and concentration can be varied without interrupting the growth of the film and so structures such as a p-n junction can be grown in a continuous process.

4.2. Structure

Elemental silicon bonds via four sp^3 hybrid orbitals, and in the crystalline form has a tetrahedral structure. In the amorphous phase the long range order of the crystal is absent but short range order persists, extending as far as the third nearest neighbour, a distance of 0.8 to 1nm.[1] In contrast to the crystalline phase where each atom is surrounded by four others, many silicon atoms in the amorphous material are bonded to less than four. A possible structure for amorphous silicon prepared by evaporation or sputtering is shown in fig.4.2a, in which the unsatisfied silicon bonds are labelled 'dangling bonds'. Fig.4.2b shows a similar structure for hydrogenated a-Si in which many of the dangling bonds have been terminated by hydrogen atoms. The number of dangling bonds, as determined by electron spin resonance in glow discharge a-Si:H is about $10^{16}cm^{-3}$ whilst in evaporated films it is many times higher[2](typically $10^{19}cm^{-3}$). Although only about 1% of the hydrogen is required to saturate the dangling bonds, in good quality a-Si:H films more like 5% of the hydrogen is incorporated into H-Si bonds. The remainder is found either interstitially as H_2 molecules, see fig.4.2b, or it bonds to two silicon atoms as Si-H-Si, a configuration which helps to relax strained Si-Si bonds.

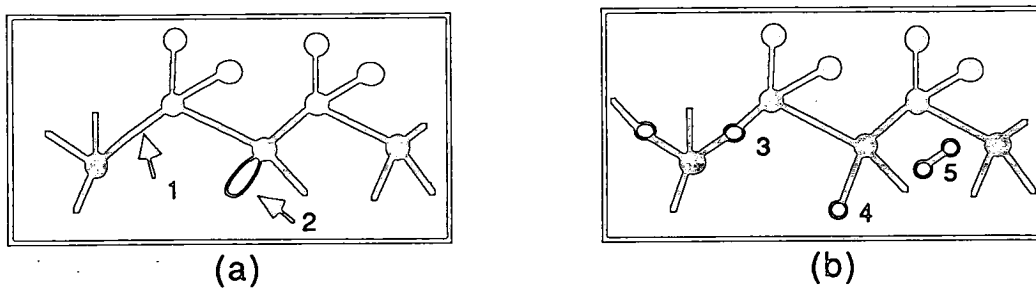

Fig.4.2 The structure of a-Si. (a) Shows a possible atomic configuration for evaporated a-Si. The arrows highlight the presence of strained bonds (1) and dangling bonds (2) both of which contribute to states in the forbiden gap. (b) shows how hydrogen in a-Si:H can relax strained bonds (3) and satisfy dangling bonds (4). Molecular hydrogen is also present in a-Si:H (5).

4.3. Density of states

The density of states of a-Si:H deduced by field effect measurements is shown in curve 1 of fig.4.3.[3,4] The diagram has been divided according to the nature of the states into the extended states of the conduction and valence bands, the tail states and the gap states.[5] The extended states are delocalised and extend throughout the material as in the valence and conduction bands of crystalline silicon. The disordered nature of the amorphous material means, however, that carriers in the extended states of the amorphous material are scattered more frequently than in the crystal. This has the effect of reducing the extended state mobility from that found in crystalline silicon which is of the order of $1000 cm^2/Vs$, to about $10\ cm^2/Vs$. The tail states are states at the edge of the valence and conduction bands that due to the disorder of the silicon matrix have become localised,[6] that is to say their electron wavefunctions are confined to a localised region of space and do not extend throughout the whole material. The gap states are caused by structural defects such as dangling bonds and like the tail states are localised.

An important feature of curve 1 is the deep minimum in the density of states near the mid-gap. This feature is in contrast with the density of states of evaporated a-Si

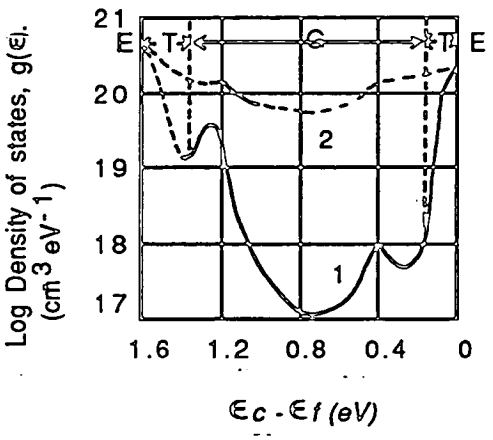

Fig.4.3. Density of states distributions for a-Si:H specimens. Curve 1: glow discharge specimen, deposition substrate temperature, Td = 520K; Curve 2: evaporated specimen. Full lines: determined by field effect experiment. E, extended states, T, tail states, G gap states (after ref 8).

which is shown in curve 2. The difference between these two is largely attributable to the presence of hydrogen. The evaporated films, which are hydrogen free, contain a high density of dangling bonds which in turn give rise to states in the band gap. In a-Si:H, hydrogen joins with the dangling bonds to form Si-H bonds which have an energy that lies not in the band gap but in the valence band. Thus the states associated with the dangling bond are removed from the gap. Hydrogen also helps to relax strained bonds with the effect of reducing gap states caused by defects other than the dangling bond.

4.4. Doping

Doping a-Si:H results in a change in the Fermi level position.[7,8] To appreciate how this happens consider fig.4.4 which shows the density of states and Fermi level position for p-type material doped with boron. Electrons from the gap states in the shaded region can be considered to have fallen to occupy the acceptor levels at energy ϵ_{db}. In doing so the Fermi level is shifted from its intrinsic position at ϵ_{fi} to its doped position at ϵ_f . The occupancy of the tail and valence band states is thus reduced, and the hole concentration is increased with a consequent increase in conductivity. Fig.4.5 shows a plot of conductivity versus doping concentration for both n-type and p-type

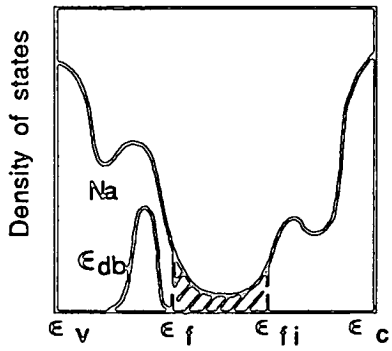

Fig.4.4 The density of states of -Si:H showing the incorporation of acceptor states. Electrons from gap states just below the intrinsic Fermi level, ϵ_{fi}, fall to occupy the acceptor states Na thereby pulling the Fermi level of the doped material closer to the valence band edge.

doping.[8] It is clear that over certain ranges g-d a-Si:H can be doped with considerable effectiveness.

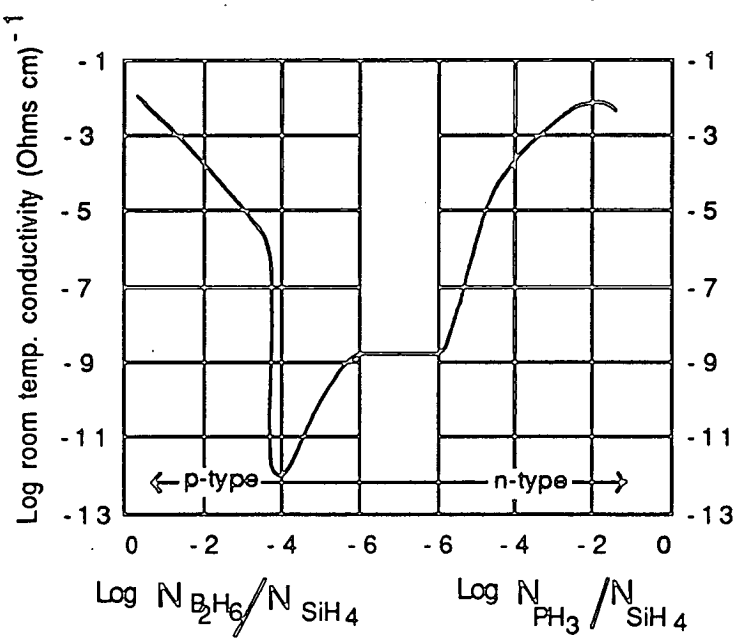

Fig.4.5 Room temperature conductivity of n and p-type a-Si specimens, plotted as a function of the gaseous impurity ratio. For the right hand curve, this is the ratio of phosphine to silane molecules in the gas mixture used to prepare the specimen. On the left it is the ratio of diborane to silane. (After ref.8)

4.5. Conduction mechanisms

Electrical conduction can take place via the three types of states shown in fig.4.3 namely in the extended states, the tail states and the gap states.[9] Throughout the following section these conduction mechanisms are discussed in terms of electron flow but

the mechanisms also apply in kind to hole transport.

4.5.1. Extended state conduction

Electrons can be thermally or optically excited from filled states below the Fermi level into the conduction band. In thermal equilibrium the conductivity in the extended states is given by

$$\sigma(\epsilon_c)=\sigma_0 \exp\left(\frac{\delta}{k}\right)\exp\left(\frac{-(\epsilon_c-\epsilon_f)_0}{kT}\right) \quad (1)$$

where ϵ_c and ϵ_f are the conduction band edge and Fermi level energies respectively, and the pre-exponential factor σ_0 is defined as

$$\sigma_0 = eg(\epsilon_c)kT\,\mu(\epsilon_c) \quad (2)$$

where $\mu(\epsilon_c)$ is the electron mobility in the extended states. The variation of the Fermi level position is given by $(\epsilon_c-\epsilon_f)=(\epsilon_c-\epsilon_f)_0-\delta T$ where $(\epsilon_c-\epsilon_f)_0$ refers to T = 0. The constants $\sigma_0 exp(\delta/k)$ have a value of about $100\Omega cm^{-1}$. Under an applied bias the overall drift mobility of the electrons is controlled by trapping and thermal release from the tail states as indicated by fig.4.6. Trapping reduces the mobility of the elctrons and, assuming a quasi-thermal equilibrium exists between electrons in the conduction band and in the traps, the modified mobility can be written:

$$\mu_d = \mu(\epsilon_c)\beta exp\left(\frac{-(\epsilon_c-\epsilon_x)}{kT}\right) \quad (3)$$

where β depends on the form of the localised states distribution between ϵ_c and ϵ_x defined in fig.4.6, and the exponential term describes the trap release time for a trap at energy ϵ_x. Inserting this modified value for the mobility into equation 1 reduces the pre-exponential factor to about $10\Omega cm^{-1}$.

4.5.2. Tail state conduction

Conduction in the tail states takes place by phonon assisted hopping between localised states of electrons thermally excited from ϵ_f. This hopping process is illustrated in fig.4.7 in which the energy required by the electron to hop between states is W and the mean hopping distance is R_o. Conduction of this kind occurs almost exclusively at the bottom of the tail states as it is these states that are the most densely populated with electrons. The hopping mobility is

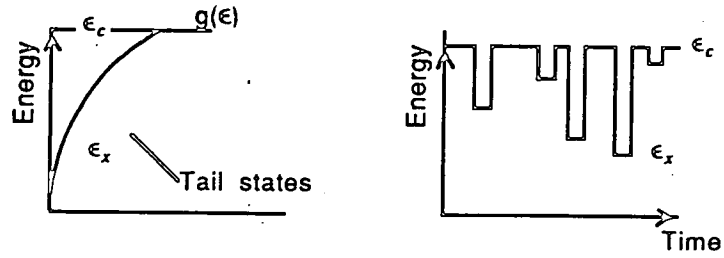

Fig.4.6. A schematic representation of electron multi-trapping in the tail states of the conduction band. The mobility of the electrons is limited by this process.

$$\mu_H = (\mu_H)_0 \exp\left(\frac{-W}{kT}\right) \tag{4}$$

where the overall conductance is

$$\sigma(\epsilon_x) = \sigma_0 \exp\left(\frac{\delta}{k}\right) \exp\left(\frac{-[(\epsilon_x - \epsilon_f)_0 + W]}{kT}\right) \tag{5}$$

and $\sigma_0 exp\,(\delta/k)$ is about $0.1\Omega cm^{-1}$.

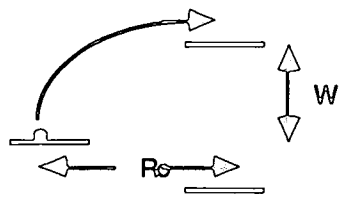

Fig.4.7 A schematic representation of phonon assited hopping. W is the phonon energy and Ro the average nearest neighbour hopping distance.

4.5.3. Hopping in the gap states

At lower temperatures fewer carriers can thermallise to the tail states and so the predominant conduction path falls below the tail states to the gap states, eventually tending towards the Fermi level itself as the temperature is lowered still further. Electron transport is again by phonon assisted hopping between nearest neighbour sites except at the very lowest temperatures at which point variable range hopping takes over. In this conduction process, as illustrated in fig.4.8, it becomes energetically more

favourable for an electron to hop beyond the nearest neighbour site in order to find a final site close in energy to its initial site. Mott has shown that the conductivity for this type of conduction

$$\sigma = \sigma_0 \exp\left[\left(\frac{-T_0}{T}\right)^{\frac{1}{4}}\right] \tag{6}$$

with

$$T_0 \approx \frac{18\alpha}{kg(\epsilon_f)} \tag{7}$$

where α represents the spatial decay of a localised wavefunction.[10]

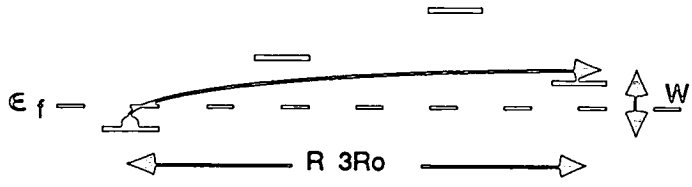

Fig.4.8 Variable range hopping between localised states in the gap. The phonon energy is W and the hopping distance is R. Ro is defined in fig.4.7.

In many cases more than one conduction mechanism contributes to carrier transport in a-Si:H. It is often found, however, that over a particular temperature range one mechanism dominates all others and an activation energy characteristic of that process is observed.

4.6. The a-Si:H to metal contact

4.6.1. Introduction

The following section gives a brief account of the conductive and capacitive properties of the a-Si:H Schottky barrier (a-barrier). Where a more detailed approach is required the reader is referred to the literature in particular references 11, 12. Fig.4.9

shows the band diagram at zero applied bias for a metal to n-type contact.

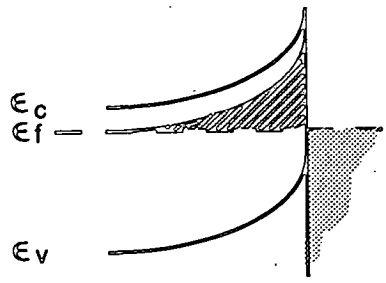

Fig.4.9 Energy bands in the barrier region of an n-type amorphous semiconductor. For a description of the various regions in the barrier see the text.

To maintain continuity in the Fermi level across the contact, electrons from gap states immediately below the bulk a-Si:H Fermi level move to the metal thus setting up a space charge region. The states in the a-Si:H that have been emptied during this electron transfer are forced above the Fermi level as indicated by the hatched area of fig.4.9. The barrier profile depends directly on the density of states in the gap, and in particular on those states directly below the bulk Fermi level which become emptied during the formation of the barrier. This is in contrast to the crystalline counterpart where the barrier profile is dependent on the dopant concentration. [13] Fig.4.10 from Spear et al.,[12] shows theoretically derived barrier profiles for a-Si:H with various doping levels. These curves show that with increasing doping the barrier profiles become steeper and narrower.

4.6.2. D.C conduction

Under forward bias the band diagram of the junction looks something like that in fig.4.11. Electrons in the conduction band can easily surmount the lowered potential barrier into the metal. In reverse bias, fig.4.12, the flow of electrons is impeded by the potential barrier. At low reverse biases the most probable means of overcoming the barrier is by thermionic emission over the top of the barrier. As the reverse bias is increased the the upper part of the barrier becomes thin enough for appreciable tunnel-

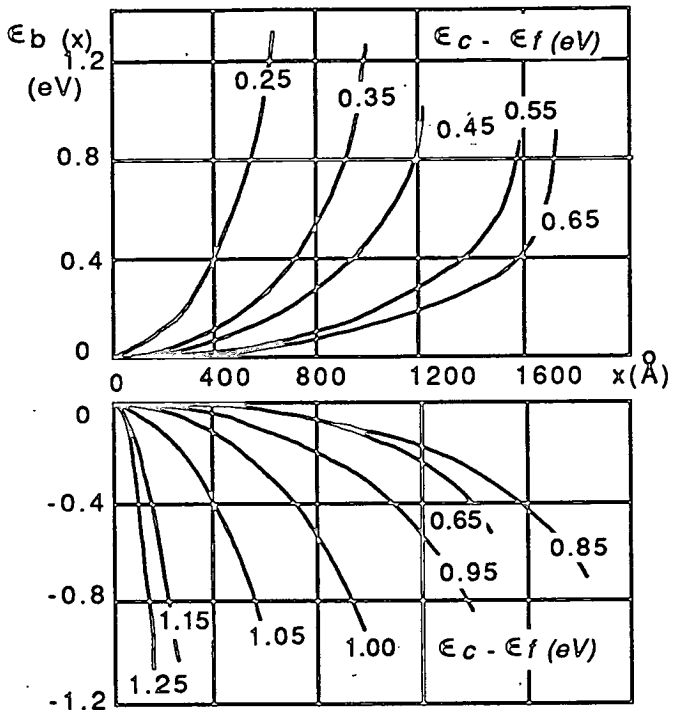

Fig.4.10 Barrier profiles ∈b(x) for a-Si:H taken from ref 12 The upper curves for ∈c - ∈f values between 0.25 and 0.85eV represent n-type depletion layers. These have been calculated for a high work function metal such as Au or Pt. The lower curves for ∈c - ∈f between 0.85 and 1.25eV show p-type depletion layers. These have been calculated for a low work function metal such as Al.

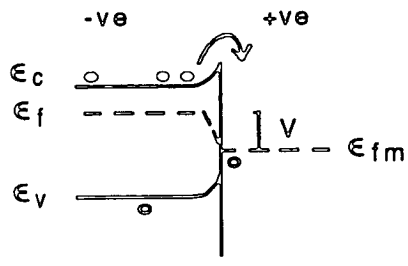

Fig.4.11 a-barrier for an n-type semiconductor under a forward bias of V Volts.

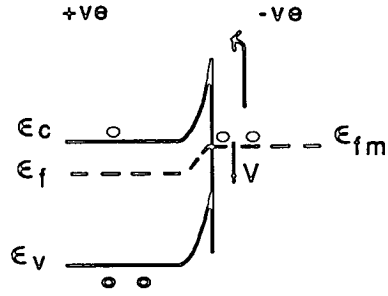

Fig.4.12 a-barrier for an n-type semiconductor under a reverse bias of V Volts.

ling of electrons from the metal to the semiconductor to take place; this is field assisted thermionic emission. At still higher biases the barrier becomes thin enough for electrons to tunnel directly from the Fermi level of the metal to the semiconductor; this is field emission. An example of forward and reverse bias characteristics of an a-SiH

barrier are shown in fig.4.13a. Rectification ratios at 1V of between 10^3 and 10^4 are commonly achieved. Fig.4.13b shows the reverse bias breakdown curves for two samples with different doping concentrations.

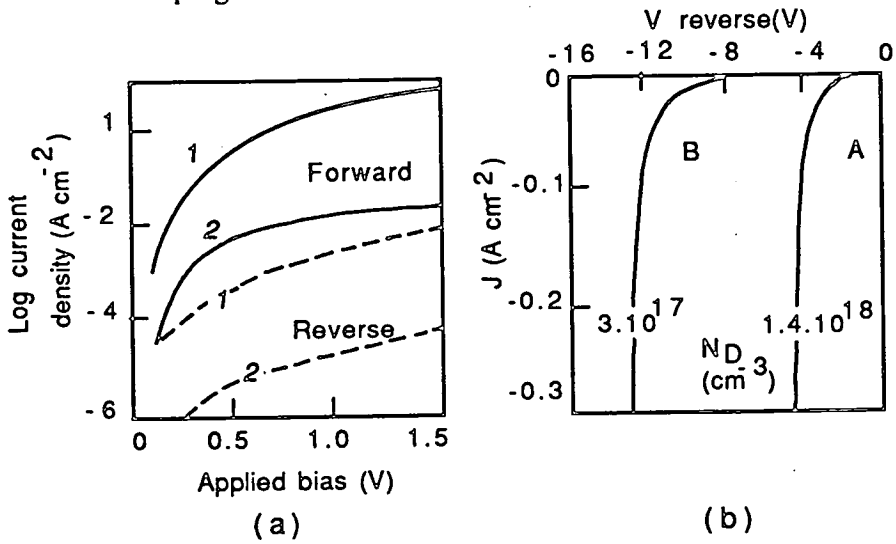

Fig.4.13 (a) Forward bias current-voltage characteristics for two a-Si/metal diodes corresponding to different doping levels. The dashed curves show the reverse characteristics. Curve 1 has a doping level of 1.4.10 ^{18}cm^{-3}and curve 2 1.5.10 ^{17}. cm^{-3} (b) Reverse bias characteristics of two a-Si/metal barriers showing the effect of doping on breakdown voltage. (After ref.11)

4.6.3. Differential capacitance

Measurement of the differential capacitance under forward and reverse bias conditions is achieved by superimposing a small a.c. modulation onto the d.c. bias and monitoring the a.c. current caused by the partial charging and discharging of the barrier capacitance. Fig.4.14 from Snell et al. [11] illustrates the experimentally observed bias dependence of the capacitance and also shows that the measured capacitance decreases with increasing frequency of the measurement signal. The bias and frequency dependence of the barrier capacitance will now be explained.

4.6.4. Frequency dependence of the barrier capacitance

Fig.4.15 shows an a-barrier with an applied a.c. voltage of amplitude ΔV and frequency f (Hz). During one half-cycle of the sinusoidal signal, filled states are lifted

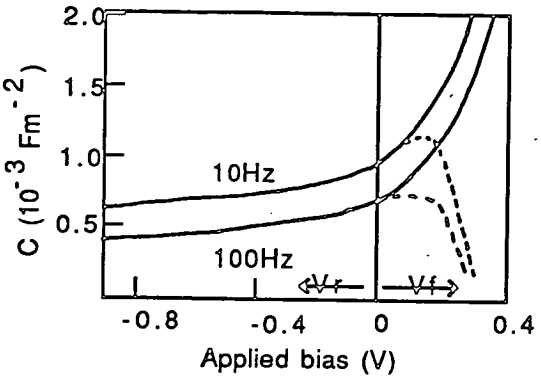

Fig.4.14 a-Si:H Barrier capacitance as a function of bias. The solid lines show the calculated barrier capacitance for a sample with $\in c - \in f = 0.6eV$. The dashed lines show the experimentally observed values. (After ref.11)

above the Fermi level by an energy ΔVe; these are indicated by the hatched area. These states are now out of thermal equilibrium and as they empty the space charge in the barrier region will be modified. The electrons in the hatched region have three ways of vacating their states (i) by thermalisation into the extended states of the conduction band, (ii) diffusion into the metal and, (iii) recombination with minority carriers.

Each of these processes has a characteristic time constant which reflects the time taken for an electron to leave its state. If an electron cannot leave its state in a time less than the duration of the half-cycle of the a.c. signal then it will not contribute to the measured value of the capacitance. As the frequency is increased, therefore, fewer and fewer carriers will be able to respond to the a.c. signal and so the measured signal decreases. Spear et al. [12] have taken the thermal excitation to the conduction band as the limiting process in determining the response of the electrons. Using this approach they achieve a good match between experimental data and calculated capacitance values under reverse biased conditions as illustrated by fig.4.14 - the discrepency between theory and experiment under forward bias is explained below.

4.6.5. Capacitance under forward and reverse bias

Fig.4.14 shows that the capacitance of the a-barriers increases steeply under forward bias, as the space charge layer becomes thinner. In reverse bias the capacitance

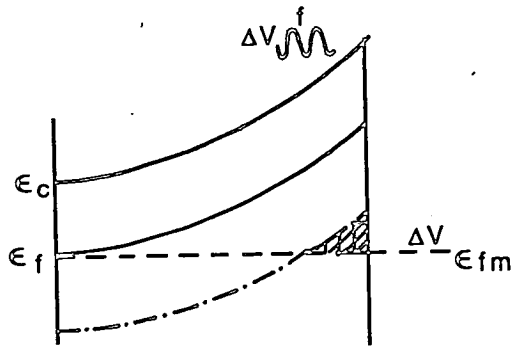

Fig.4.15 Energy bands in the barrier region of an n-type amorphous semiconductor at zero d.c. bias but with an a.c. voltage of amplitude ΔV and frequency f. During one half cycle of this alternating potential filled states will be lifted above the Fermi level by an energy \e\V, these are shown as the cross-hatched area. These states will have to empty before they can contribute to the modification of the space-charge region. (Based on ref.11)

decreases relatively slowly. A detailed analysis of the cause of these changes can be found in ref..[12,11] The departure of the experimental data from the theoretical curves under forward bias has been shown to be due to the response of the specimen as a whole to the test signal. Snell et al.[11] have made use of the equivalent circuit in fig.4.16, in which the capacitance and the resistance of the barrier region and bulk are represented by separate quantities, to show that the measured capacitance will be that of the barrier only whilst the barrier resistance is sufficiently high. When the forward bias barrier resistance falls , the measured capacitance tends to the geometric capacitance of the bulk,(C2 in fig.4.16) which for the sample referred to in fig.4.14 is much smaller than the barrier capacitance.

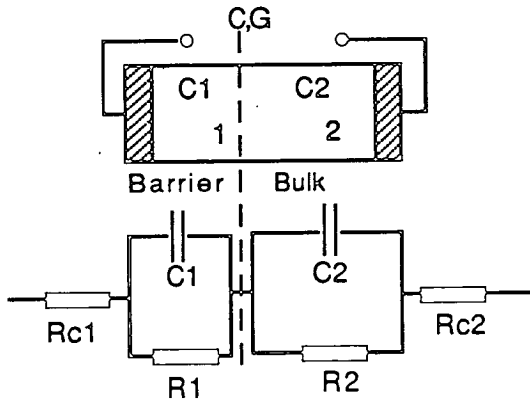

Fig. 4.16 The equivalent circuit used to analyse the capacitance and conductance data of the a-Si:H Schottky barrier.R1 and C1 represent the barrier resistance and capacitance and C2 and R2 the bulk capacitance and resistance. Rc1 and Rc2 are contact resistances. The dashed line marks the edge of the barrier region. (After ref. 11)

4.7. The effect of elevated temperature on a-Si:H

At elevated temperatures a-Si:H undergoes three distinct structural changes before the onset of melting at 1414°C:

1 150 to 450°C. Defect annealing.

2 300°C to crystallisation temp. Dehydrogenation.

3 640 to 770°C. Crystallisation.

The effect of these three changes on the electrical conductivity of the a-Si:H can be followed in fig.4.17 which shows the variation of the conductivity measured at 60°C as a function of anneal temperature.[14] In region (I) some of the defects in the silicon matrix are annealed out. This has the effect of reducing the number of states in the gap and so the overall conductivity of the material decreases.[∇] At the onset of region (2) (at about 350°C) weakly bound hydrogen such as interstitial hydrogen molecules and hydrogen in the three centre Si-H-Si bond, starts to leave the material.[15] Above about 520°C the tightly bound hydrogen in the Si-H bond also leaves. The desorption of hydrogen increases the strain in the amorphous network and leaves behind dangling silicon bonds: the net effect is an increase in the density of gap states. This results in an increase in the conductivity as seen in section (2) of fig.4.17. The loss of hydrogen also causes a narrowing of the optical gap causing a darkening of the material at certain frequencies.[16,17] For temperatures above 640°C, region (3), crystallisation occurs.[18]

Crystallised a-Si melts at 1414°C, the normal melting point of crystalline silicon. If a-Si is heated sufficiently rapidly with, for example, a laser or an electron beam, it is possible to melt it without it first crystallising at the lower temperature of 897°C.[19]

Quenching molten silicon results in almost every instance in the formation of micro-crystalline material and not an amorphous material, as the quench rate neces-

∇.It should be appreciated that the sign of the change in the conductivity of a-Si:H with annealling depends on the type of the starting material; broadly speaking annealling p-type material results in an initial decrease in the conductivity whilst annealling n-type material results in an increase.

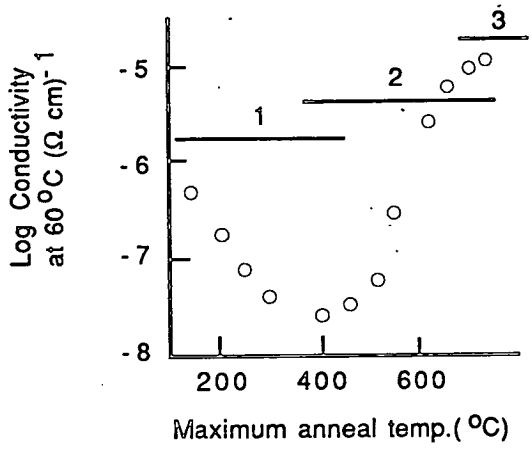

Fig.4.17 Variation of conductivity of a-Si prepared by glow discharge measured at 60 °C versus annealing temperatue. For an explanation of the three regions see the text. (After ref. 14)

sary to produce the amorphous phase is unattainable by most experimental techniques. One exception to this is the use of pico-second laser pulses. A volume of silicon exposed to such a short burst of energy experiences a rapid temperature increase and, once the pulse is over, cools rapidly. By this method amorphous silicon has been produced on thin film micro-crystalline substrates.[20] The reluctance of silicon to solidify in the amorphous phase is in contrast to the other important group of amorphous semi-conductors, the chalcogenide glasses.[21] The difference between the two in this respect is of particular relevance to memory switching as it is the reversible transition between the crystalline and amorphous phases that is responsible for the non-volatile memory switching effect in chalcogenide devices.

4.8. Amorphous silicon and metal mixtures.

4.8.1. Introduction

It will become apparent when the conduction and switching mechanisms of a-Si:H memory devices are discussed that it is relevant to consider the properties of silicon:metal mixtures. The following sections give a brief survey of the properties of such binary mixtures.

Metal can be incorporated into an amorphous film in two distinct ways:

(i) it can remain in its metallic form and exist as granules embedded in the amorphous matrix or,

(ii) if the mixing is more intimate it can form an alloy with the amorphous material.

Which of these two types of mixing occurs depends largely on the preparation conditions.

4.8.2. Granular combinations of metal and a-Si

There are in general three distinct structural regimes in granular metal:dielectric mixtures, as shown schematically in fig.4.18.[22]

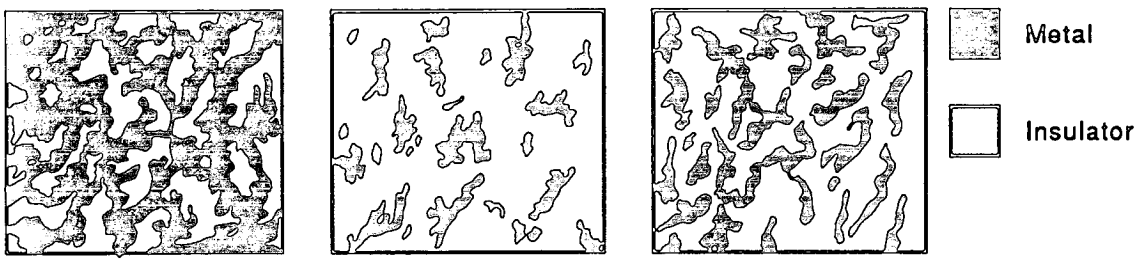

Fig.4.18a
Metallic regime

Fig.4.18b
Dielectric regime

Fig.4.18c
Transition regime

Metallic regime: the overlapping metal granules form a continuum with dielectric inclusions. Electrical conduction is through the metal but the overall resistivity of the film is higher than that of the pure metal because the dielectric scatters the electrons thereby reducing their mean-free path. The temperature coefficient of resistance (TCR) is positive as in a metal. **Dielectric regime:** this is the converse of the metallic regime where now there is a dielectric continuum with metallic inclusions. Electrical conduction is by thermally activated tunnelling between the metal islands with any additional contribution to the current occuring solely through 'leakage' in the dielec-

tric.[23,24,22] The TCR is now negative. Transition regime: this is the regime in which the structural inversion between the metallic and dielectric regimes takes place. Electrical conduction takes place by percolation of electrons along the metallic maze and by tunnelling between isolated metal particles. The TCR is negative.

Overall the conductivity of the films changes smoothly from being close to a metallic value for the metal rich films to a value similar to that of the dielectric in the metal sparse compositions.

4.8.3. Amorphous silicon : metal alloys

In contrast to a granular metal:Si mixture an amorphous metal:Si alloy has a reasonably homogenous structure. Amorphous Si:metal alloys incorporating a number of metal elements have been investigated. These include Fe, Ni, Mn,[25,26] Cr,[27,28,29] and Au.[30] Although the exact structure of these films is not certain they remain amorphous at least down to a scale of 3nm. Morigaki[30] has proposed that in Au:Si mixtures prepared by electron beam evaporation the gold gives rise to a band of deep accepter states in the Si band gap. The variation in the room temperature conductivity and thermal activation energy with Au content is shown in fig.4.19.

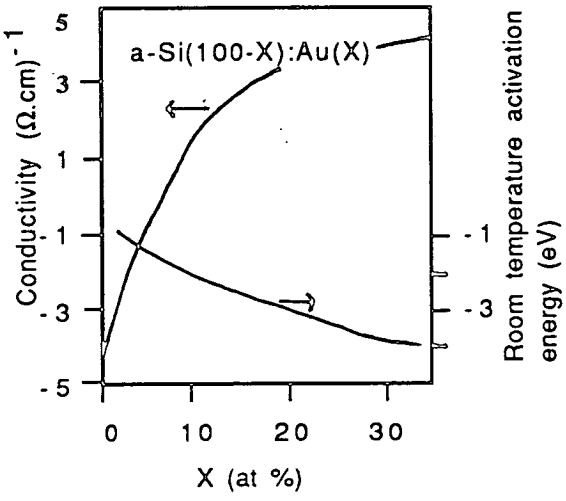

Fig4.19 Room temperature conductivity of a-Si(100-x):Au(x) films and their activation energy taken at room temp. as a function of Au content (After ref 30)

4.9. Summary

In this chapter I have introduced the background material to be used later in the thesis. I have described the preparation of a-Si:H by the glow discharge of silane and the structure of the a-Si:H films. Electrical conduction in these films has been shown to take place in the extended states of the valence and conduction bands, by phonon assisted hopping in the localised states of the gap and the valence and conduction band tails, and by variable range hopping in the gap states at the Fermi level.

The metal - a-Si:H Schottky barrier has been discussed in some detail. The barrier profile and width is determined by, amongst other things, the density of gap states of the a-Si:H. Heavily doped a-Si:H forms thinner and steeper barriers than lightly doped material. The differential capacitance of the a-barrier shows a frequency dependence which reflects the response time of carriers to the a.c. measuring signal. Under forward bias the barrier capacitance increases rapidly whilst under reverse bias it decreases slowly.

The effects of elevated temperature on the structure of a-Si:H have been reviewed. Four major processes can be identified as the temperature is increased. From 150°C to 450°C defects in the a-Si:H are annealed, between 300°C and the crystallisation temperature dehydrogenation takes place, from 640°C to 770°C the a-Si:H crystallises, finally at 1414°C the Si melts.

The final section dealt with the properties of Si:metal mixtures. Irrespective of whether the Si and metal mix on an atomic scale to form an alloy or whether they remain aggregated in their atomic form, the properties of the material vary smoothly from metallic like i.e.with low positive TCR's, to semiconductor like with negative TCR's as the metal concentration is reduced.

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Chapter 5

Experimental methods

5. Sample Preparation

Fig.s 5.1 and 5.2 show the two generic groups of devices described throughout this thesis. The device of fig.5.1 has a pore structure: the active area of the device is circular and is defined by the electrically insulating layer of photoresist. The layer of a-Si:H has metal contacts at top and bottom. The top contact is connected to a probe pad, the bottom contact to a metal track that runs the length of the sample to probe pads at either end. The device of fig.5.2 differs fundamentally from that of 5.1 in that the contacts to the a-Si:H layer are made of Si rather than metal. The bottom contact is the crystalline Si substrate which is doped to a high conductivity. The top contact is the microcrystalline layer of Si. The latter is prepared by the glow discharge of silane in the same reactor as the a-Si:H layer and so can be grown continuously with the a-Si:H layer. It too is doped heavily to ensure it provides a low resistance contact. A layer of metal is used to overlay the microcrystalline silicon but only away from the active area of the device i.e. away from the pore.

All the samples, both those shown in fig.5.1 and 5.2, were prepared on substrates measuring 2 × 4.5cm in eight rows of ten devices. The thickness of the a-Si:H layers of the two types of devices ranges from 50nm to 1μm. Homogenous layers of p^+ and n^+ type a-Si:H, and heterogeneous layers with a p-n-i configuration have been used. A variety of metals have been used as the contact material namely Cr, NiCr, Al, Fe and Au. Tables 5.1 and 5.2 give a brief processing schedule for both types of device. The word 'pattern' in these tables implies the use of normal photolithographic techniques in conjunction with either a wet or plasma etch. Most samples were prepared at the University of Dundee. R.F. glow discharge of silane was used to prepare the a-Si:H and microcrystalline silicon.

Pore structure : normal configuration.

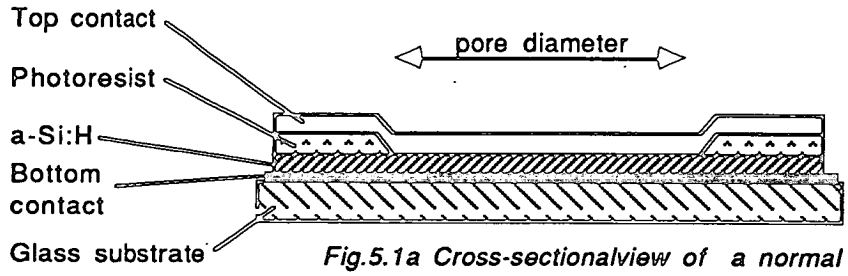

Fig.5.1a Cross-sectionalview of a normal memory device showing the 'pore' structure.

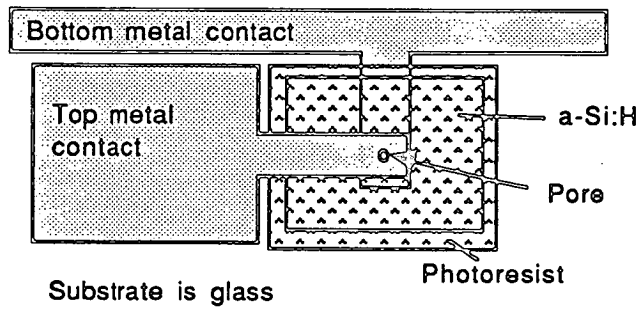

Fig.5.1b Plan view of the normal 'pore' structure

(Not to scale)

Pore structure : silicon contact configuration.

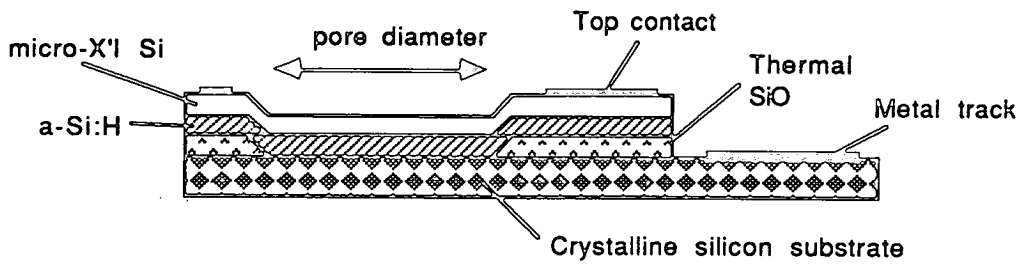

Fig.5.2a Cross-sectional view of the silicon contact device.

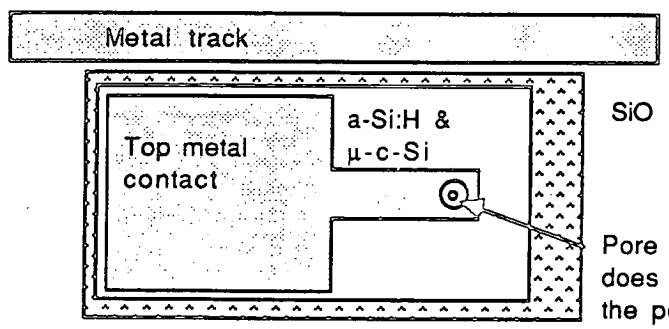

Fig.5.2b Plan view of the silicon contact device.

(Not to scale)

NORMAL PORE DEVICES Substrate Corning 7059 glass	
1	Deposit bottom metal contact by evaporation or sputtering
2	Pattern metal
3	Deposit a-Si:H by glow discharge
4	Pattern a-Si:H
5	Spin on photoresist
6	Pattern resist then hard bake at 120C for 20min
7	Deposit top metal
8	Pattern top metal
9	Deposit Al for bond pads
10	Pattern Al

Table 5.1 The processing schedule for normal pore structures as shown in fig.5.1a

Si contact pore devices Substrate p-type crystalline silicon with an n-type surface implant	
1	Grow thermal oxide
2	Pattern oxide
3	Deposit a-Si:H and mico X'l Si in a single process
4	Pattern a-Si:H & micro X'l Si
5	Deposit top metal
6	Pattern top metal

Table 5.2 The processing schedule for the Si contact devices as shown in fig.5.1b.

5.1. Packaging of samples

In a number of instances it was necessary to mount the devices in chip carriers. This involved dicing the substrate in to groups of 9 devices with a diamond scribe or saw, glueing the sample piece to a 24 pin DIL ceramic package and then wire-bonding to the Al bond pads on the devices.

5.2. D.C electrical measurements

All d.c measurements were made using a Hewlett Packard Semiconductor Parameter Analyser (4145A). This machine had an operating range of 10pA to 10mA and 10mV to 20V with a measurement accuracy of at least $\pm 1\%$ over most of this range.

5.3. Transient electrical measurements

Fig.5.3 shows a schematic representation of the apparatus used to investigate the initial electro-forming process and the subsequent switching characteristics of the devices. This delivered to the device voltage pulses of either polarity with durations ranging from 10ns to a few ms and amplitudes from 10mV to 100V. The device current and voltage during the switching and forming operations were monitored with the oscilloscope (Hewlett Packard Digitising 10MHz). The d.c resistance of the devices could be measured using the digital voltmeter (Keithley 610C); this was done at a fixed voltage of 0.5V. The use of the computer allowed a degree of automation in the testing of the device's switching performance and also offered an easy means of accumulating and recording data on the devices. For both forming and switching operations a current limiting resistor was placed in series with the device; typically 1kΩ for forming and 100Ω for switching.

5.4. Capacitance and conductance measurements

Capacitance and conductance measurements as a function of frequency were per-

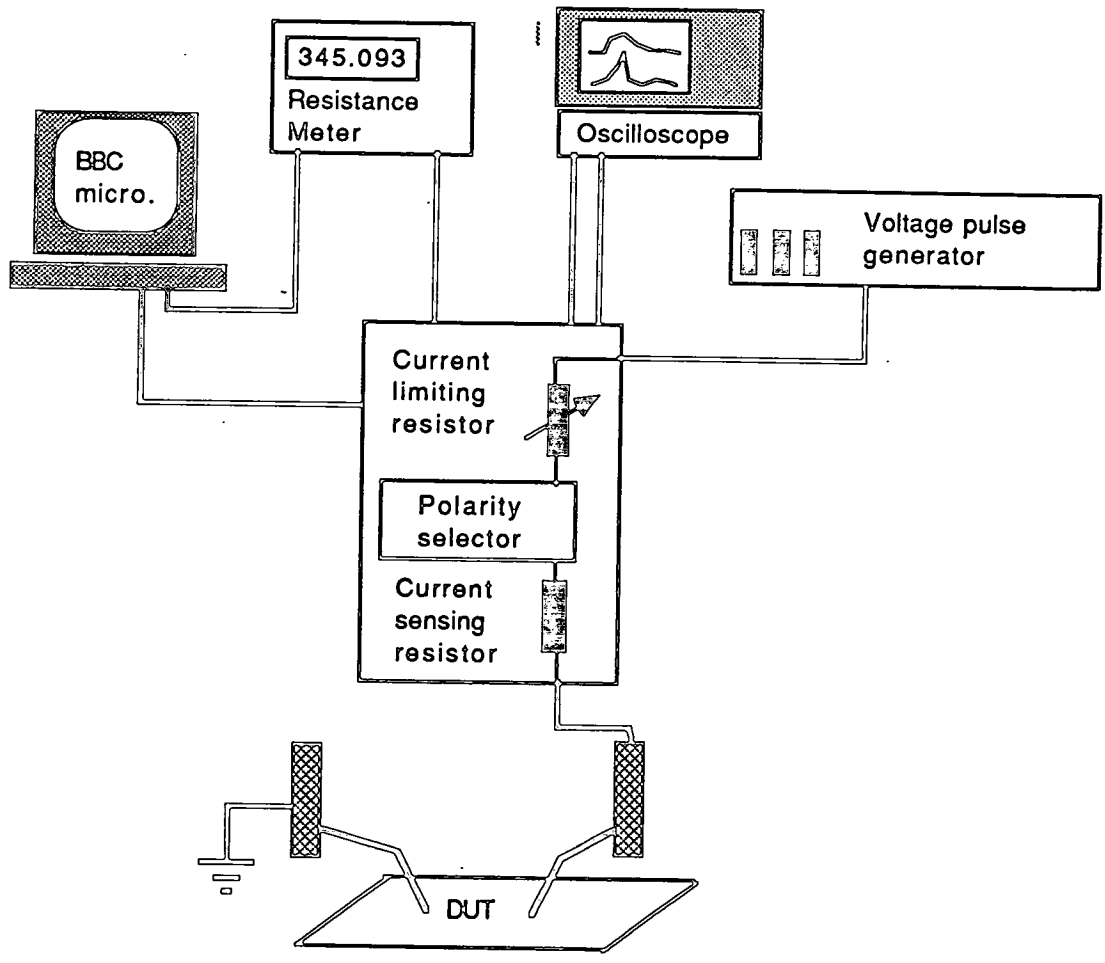

Fig.5.3 The experimental set up used to form and switch the devices. The BBC micro. was used to select the polarity of the voltage pulses.

formed using two Hewlett Packard LCZ (4276A & 4277A) meters which between them covered a frequency range from 100Hz to 1MHz. Both machines provided a d.c bias of ± 10V. A low capacitance probe station was used to make connection to the devices.

5.5. Resistance measurements below 77K

The electrical measurements at temperatures near 4.2K were made under constant current modulation conditions using a phase sensitive detector to enhance the measurement sensitivity. Fig.5.3 shows the arrangement used. The voltage applied across the sample comprised two parts; (1) a d.c bias provided by the parameter analyser and, (2) a sinusoidal voltage from the oscillator. The a.c. voltage across the sample, i.e. as measured between point A and earth, is proportional to the dynamic resistance, dV/dI, of the sample. This a.c. signal is selectively amplified by the phase sensitive detector and the output sent to the parameter analyser where the dynamic resistance is plotted against the d.c. bias across the sample.

5.6. Cryogenic measurements

5.6.1. To liquid nitrogen temperatures

An Oxford Instruments liquid nitrogen cryostat and digital temperature controller were used to make measurement from 450K to 77.4K. The samples were packaged in 24 pin chip carriers and then mounted in a plastic socket at the end of the sample rod. Electrical connections to all 9 devices were possible.

5.6.2. To liquid helium temperatures.

The arrangement for the liquid helium cryostat was rather more involved and is shown in fig.5.5. Helium was pumped out of the Dewar, along the inner part of the transfer tube (solid dark line in fig.5.5) and into the sample chamber of the cryostat. From here it passed back out of the cryostat along the outer part of the transfer tube to be vented to the air. The rate of flow of helium was controllable by a needle valve at the bottom of the transfer tube and a second valve mounted in a separate box. The samples were packaged and mounted on the sample rod in the same way as with the

liquid nitrogen cryostat.

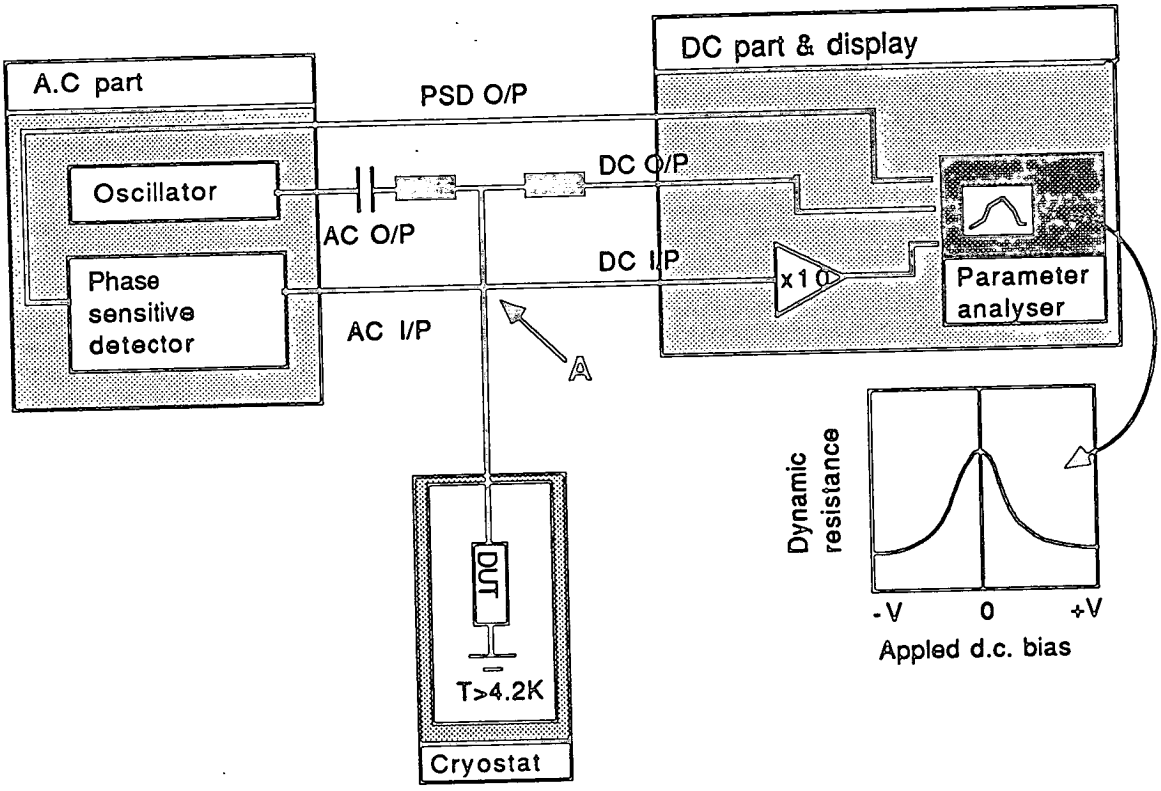

Fig.5.4a The system used to measure the dynamic resistance (dV/dI) of samples at low temperatures.

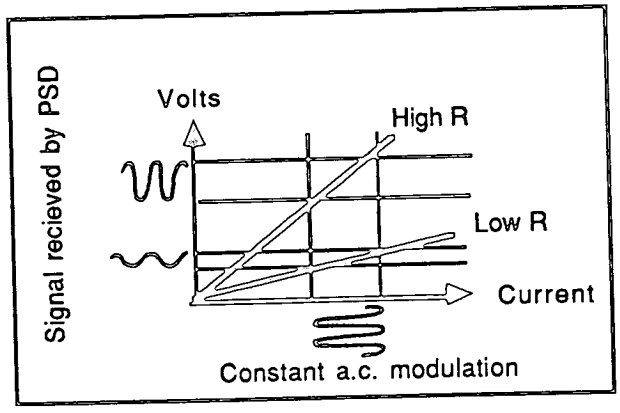

Fig.5.4b A schematic representation of the measurement of dV/dI using a sinusoidal voltage modulation.

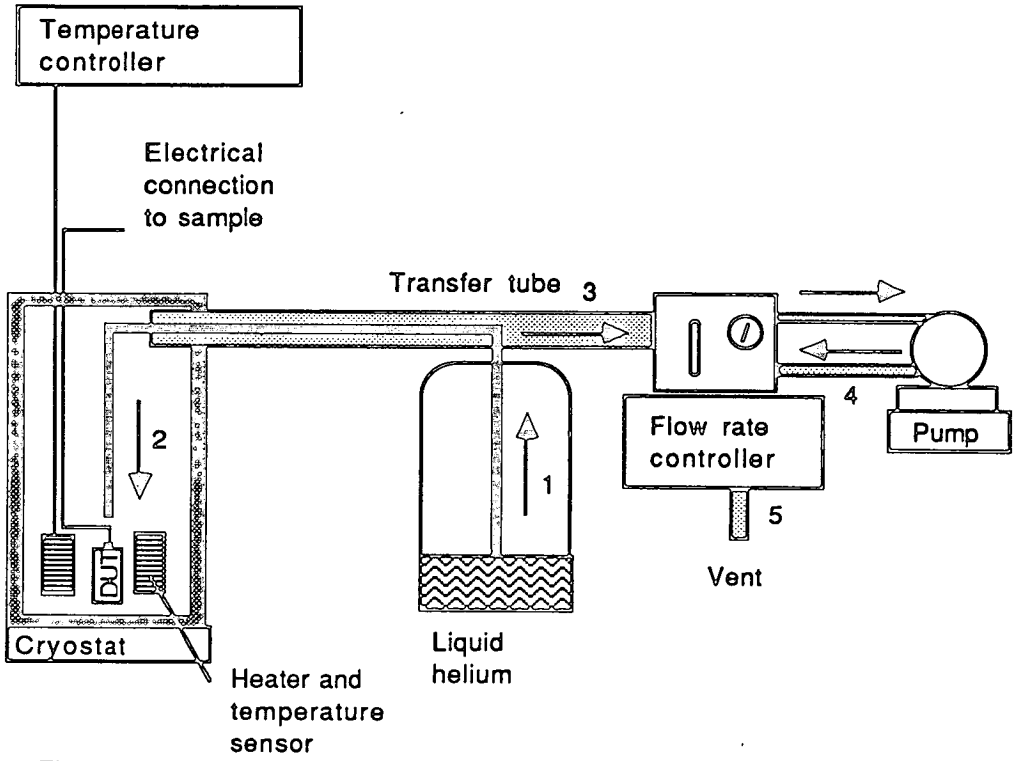

Fig.5.5 Schematic representation of the liquid Helium cryostat showing the circulating system.

Chapter 6

Experimental observations of the pre-formed state, forming and the post-formed state

6. Introduction

The newly prepared a-Si:H memory devices require an initial electro-forming stage before they show switching behaviour; this was discussed earlier in chapter 3. Prior to forming the devices are refered to as 'pre-formed' and after forming they are refered to simply as 'formed'. In this chapter I describe the results of investigations into the electrical properties of the pre-formed and formed states of the device and also the forming process. All the results were obtained using devices with a single layer of p+ a-Si:H with the 'normal' pore structures as illustrated in fig.5.1a of §5.0 i.e. the a-Si:H layer had metal contacts both top and bottom. A range of pore areas and a-Si:H layer thicknesses were used. The aim of this series of experiments was to establish a picture of the electronic processes occurring in the device to give some insight into the subsequent forming and switching processes.

6.1. Static current-voltage characteristics

The conductivity of the unformed p^+ samples (prepared with a B_2H_6 impurity concentration $10^4 vppm$) was found to vary widely from one sample batch to the next. Fig.6.1 shows I-V characteristics of two Cr-p+-Cr devices with 10μm diameter pores. Although the structure of these two devices is nominally very similar the conductances are obviously quite different. Despite this variation in the conductances the I-V characteristics showed many common features. As expected for a nominally symmetrical structure the curves were roughly symmetrical about zero volts. Often the current showed a near Ohmic dependence on the voltage from 0 to 0.1V followed by a non-linear dependence, where it is common to find $I = V^n$ with $1<n<2.5$. Beyond about 2V the current increases even more rapidly until irreversible breakdown occurs at 3-4V.

The resistance of all samples at low biases was considerably higher than that

expected for the layer of a-Si:H alone i.e. the resistance was higher than if the resistance of the device was determined entirely by the resistance of the bulk a-Si:H. To highlight this the hatched area of fig.6.1 shows the current-voltage relationship expected for the a-Si:H layer of the pore if its resistance is calculated simply using $R = \rho d/A$ where ρ is its resistivity which should lie between $10^{2}\Omega cm$ and $10^{3}\Omega cm$,[1] d its thickness and A its area. The large discrepancy between the measured and the 'expected' current levels strongly suggests the contacts between the a-Si:H and the metal are introducing considerable additional resistance.

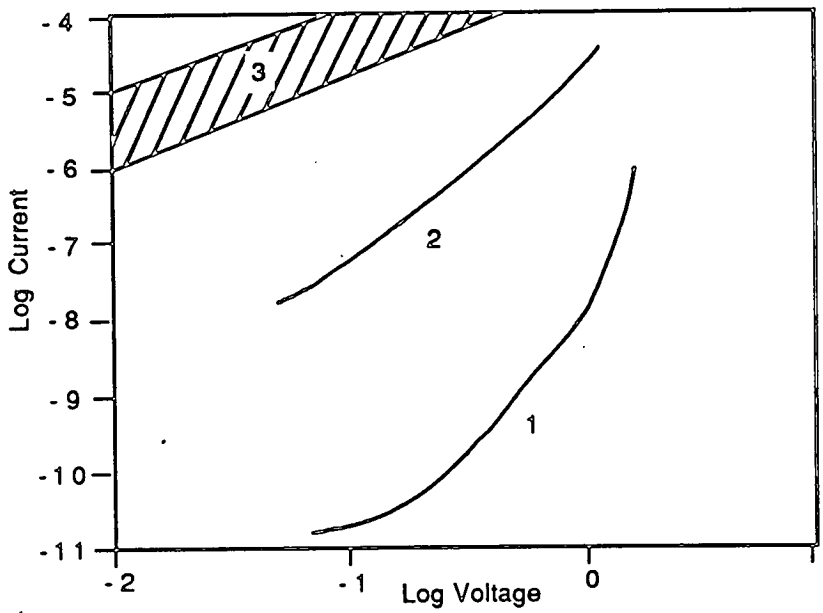

Fig.6.1 I-V characteristics of Cr - p+ - Cr samples from two similar samples. The pore diameters are 10μm, both samples are doped to a conductivity of between 10^{-2} and 10^{-3} $(\Omega cm)^{-1}$ Sample 1 has a thickness of 180nm and sample 2 a thickness of 120nm. The hatched area represents the expected current in these devices assuming low resistance contacts between the electrodes and the a-Si:H and an a-Si:H conductivity of between 10^{-2} and 10^{-3} $(\Omega cm)^{-1}$

6.2. Thickness dependence of conductance

In fig.6.2 is shown the device current against the average field strength across the device, defined by (applied bias) /(a-Si:H thickness), for three sample thicknesses. These samples were prepared by thinning the a-Si:H layer of a single batch of samples

using a Vacutec plasma etcher. Although the range of thicknesses is rather small it appears from the lack of superposition of the three curves that the device resistance at this bias does not scale linearly with device thickness. This again suggests that at these biases the resistance of the device is determined not by the bulk a-Si:H but by the contacts.

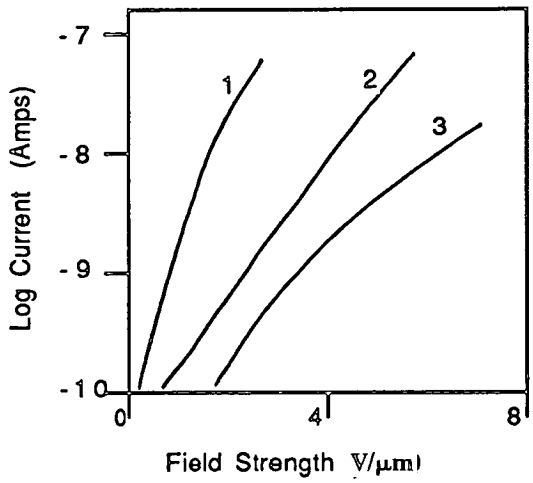

Fig.6.2 Current vs. average field strength across the a-Si:H for a Cr - p+ - NiCr sample that had been progressively thinned by plasma etching. The average thicknesses of the p+ layers are: Curve 1 779nm, curve 2 714nm, curve 3 303nm.

6.3. Current vs. voltage and temperature from 200K to 370K

Fig. 6.3 shows the averaged LogI vs. 1000/T data from six samples all from the same sample piece, the error bars indicating the standard deviation on each point. The thermal activation energies have been calculated in the normal way. For comparison, the room temperature activation energy of p^+ a-Si:H prepared with the same gaseous impurity ratio, N_{B2H6}/N_{SiH4}, of 10^{-2} but measured in a gap cell is known from previous work[1] to be around 0.2eV. It is clear, therefore, that whilst gap cell measurements may give an activation energy of about 0.2eV, measurements on the sandwich structures, using notionally similar material, give a range of room temperature activation energies that at most are around 0.2eV but may be considerably less depending on the applied bias.

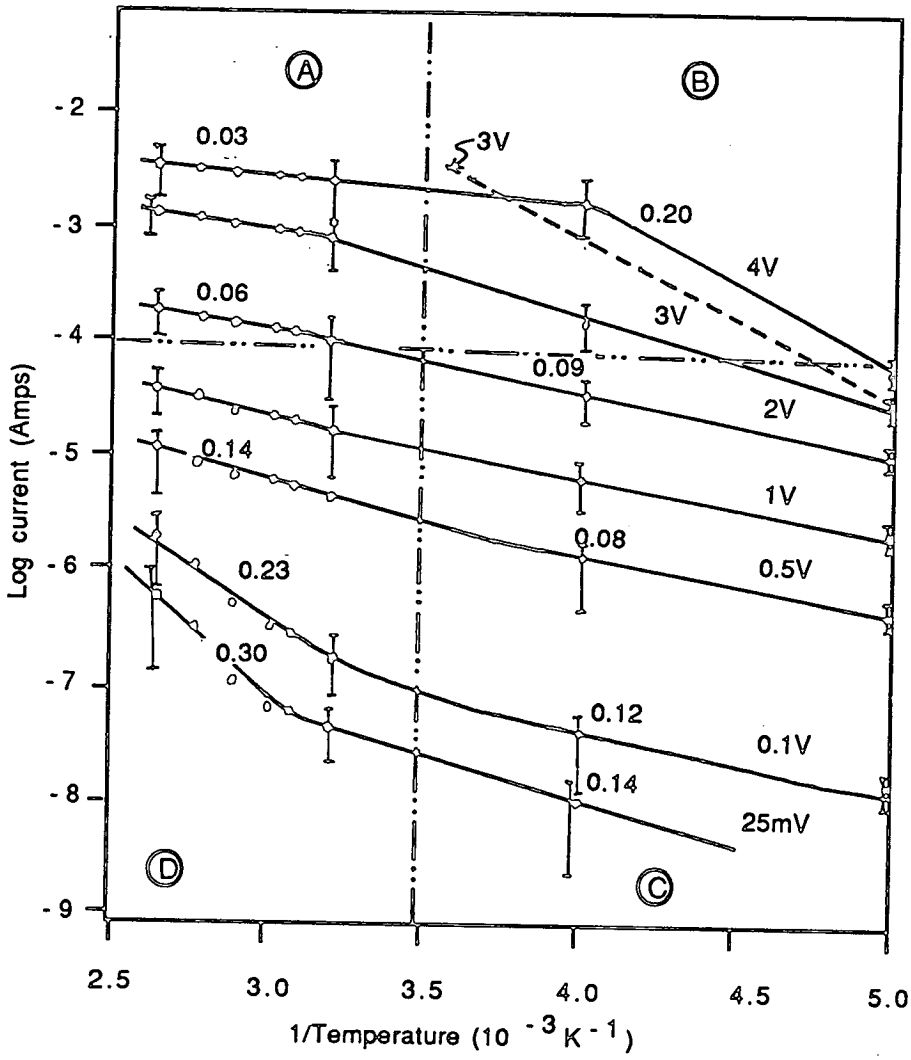

Fig.6.3 Log.I vs. 1000/T for Cr - p+ - Cr samples in the unformed state. The pore diameter was 10μm and the a-Si:H film thickness 80nm. The biases at which the data has been taken and the activation energy in eV at various points of the curve are marked. The dashed curve corresponds to the expected behaviour of a piece of p+ a-Si:H with a room temperature resistance of 1kΩ and a thermal activation energy of 0.2eV.

6.4. Discussion of the d.c. characteristics

The three pieces of evidence described in sections 6.1,6.2,6.3 all suggest that the current in the p+ devices is limited not by the resistance of the a-Si:H itself but by the resistance of the contacts to the metal electrodes. There seems to be two possible explanations for this; (1) the Schottky contacts at the metal to a-Si:H interface are blocking the current or, (2) an insulating layer of oxidised silicon or metal is present at

a contact.

The Schottky contact formed between a-Si:H and metals was discussed in §4.6. [2,3] In the Cr-p+-Cr device we expect to find Schottky barriers at both a-Si:H to metal interfaces, both nominally identical to each other and arranged back to back. Fig.6.4a shows the expected band diagram, with the Fermi level of the p+ a-Si:H taken as being 1.25eV below ϵ_c. The barrier profiles have been calculated using the method described by Spear et al. [2] making use of the same density of states curve for the a-Si:H and taking the work function of the electrode metal to be 4.5eV for Cr.

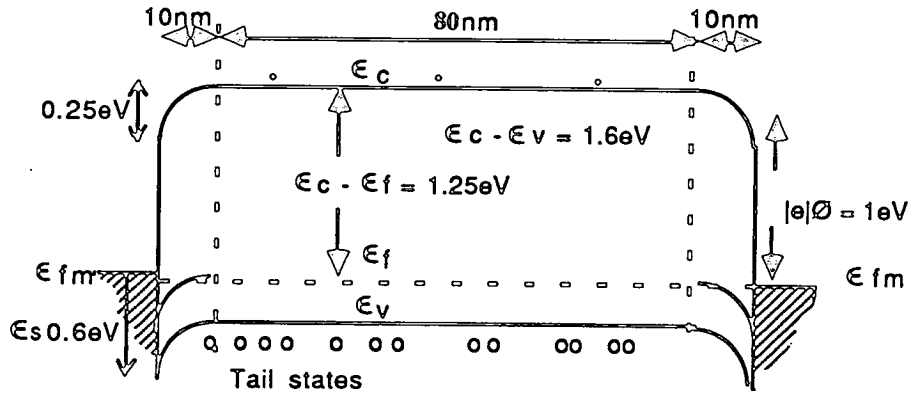

Fig.6.4a The expected band diagram for a metal - p+ - metal device with a p+ layer thickness of 100nm and the p+ a-Si:H doped to give Ec - Ef = 1.25eV. The |e|Ø value for the metal has been taken to be 1eV, equivalent to Cr. See text for further details.

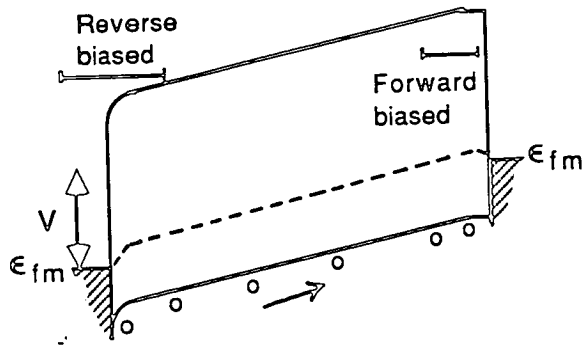

Fig. 6.4b A sketch of the metal - p+ - metal device under a bias of V volts showing the reverse and forward biased barriers.

It appears from this that the barrier regions are about 10nm in extent. Under an

applied bias one barrier will be forward biased and the other reverse and the band diagram will look more like that sketched in fig.6.4b. Of the two barriers the one reversed biased presents the greatest impedance to the flow of the majority carriers, the holes. Although it is difficult to calculate the resistance of the reverse biased barrier it seems probable that it could impede the current sufficiently to account for the overall resistance of the samples.

As the field strength across the reverse biased barrier is increased from zero the current flowing across it will increase, at first gradually, and then as breakdown is reached, much more rapidly. This increase in the current can be related to the conduction mechanisms across the barrier. As shown in fig.6.5, carriers can cross the barrier by three mechanisms: thermionic emission, field enhanced thermionic emission and field emission.

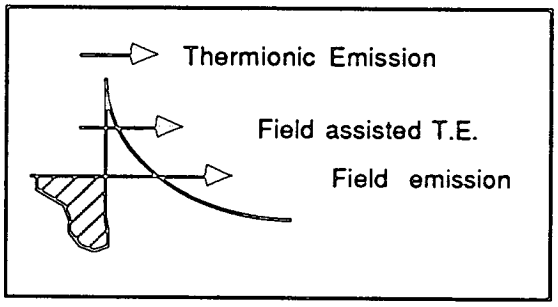

Fig.6.5 The three processes by which carriers (in this case electrons) can cross the potential barrier at a metal to semiconductor interface.

At the lowest biases carriers cross the barrier by thermionic emission. With increasing field strength the barrier becomes narrower and they start to tunnel through the barrier at an energy above the Fermi level: this is field assisted thermionic emission. At still higher field strengths the barrier is even narrower and they tunnel through the barrier at the Fermi level: this is field emission.

Some idea of the voltage ranges over which these processes take place can be gained from fig.6.6.taken from Snell et al..[3] In this figure $|e|V_B$ is defined by

$|e|V_B = \epsilon_s + |e|V_R$ where ϵ_s is defined in fig.6.4a and is equal to 0.6eV, and V_R is the applied reverse bias. Heavily doped p-type a-Si:H prepared from a gaseous mixture with a diborane to silane ratio of 10^{-2} is expected to have a dopant density of $10^{18}-10^{19} cm^{-3}$. Fig.6.6 suggests, therefore, that at low biases i.e. $V_R \approx 0$ (and thus $|e|V_B \approx 0.6eV$) conduction is likely to be by thermionic field emission. By about $V_R = 1V$ (i.e. $|e|V_B = 1.6eV$) field emission will start to come into play and by $V_R = 2V$ (i.e. $|e|V_B = 2.6eV$) conduction will be entirely by field emission. Breakdown in the reverse biased junction occurs once field emission has set in, thus we can expect this to happen at a voltage in excess of about 2V.

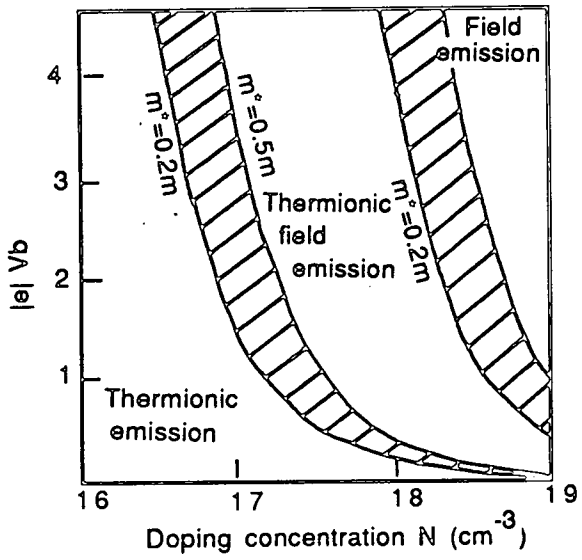

Fig.6.6 Theoretical predictions of the predominant conduction mechanism across a reverse biased semiconductor to metal contact as a function of band bending Vb (eV) and the doping level of the semi-conductor. (After ref. 3.)

The other possible explanation of the high resistance of the samples is an oxide layer. It is well known that crystalline Si forms an oxide layer of about 2nm when left in air at room temperature. The presence of hydrogen in a-Si:H, however, greatly reduces surface oxidation. Oxidation of the metals used for the contacts, particularly the bottom contact, might be taking place. Conduction through these oxide layers, as they are probably rather thin (<5nm), is likely to be by tunnelling.

To summarise , it appears that the resistance of the reverse biased Schottky barrier might account for the observed resistance of the samples. As the bias is increased

from zero volts this barrier becomes increasingly conductive and the overall device resistance falls. The indications are that by 1.5V to 3V the barrier will have broken down. The current may then be controlled by the resistance of the bulk a-Si:H. If an oxide layer is present this will add to the overall resistance and as part of the applied voltage will fall across this insulating layer the field strength at the reverse bias barrier for a given applied voltage will be reduced which may cause the device to breakdown at a higher voltage.

Turning now to the I-V-T results: how can the thermal activation energies obtained from fig.6.3 be accounted for in terms of the band diagram of fig.6.4a and b? If conduction at biases below the breakdown voltage is limited by transport across the reverse biased junction then the thermal activation energy measured under these conditions of bias should reflect the predominant conduction mechanism across this junction. The data for low biases, found in quadrants D and C of fig.6.3, indicates that at temperatures between 310K and 200K the thermal activation energy is close to 0.1eV. This is less than the predicted barrier height of around 0.6eV shown in fig.6.4a and suggests, therefore, that at these biases holes are not thermallising over the top of the potential barrier but are undergoing field enhanced thermionic emission at an energy level 0.1eV above the metal's Fermi level. Above 310K, and presumably as more thermal energy becomes available, the activation energy increases (quadrant D) indicating that holes are penetrating the barrier at higher energies.[∇] At biases in excess of about 2V the reverse bias junction is expected to have broken down and the device current to be limited by the bulk resistance of the a-Si:H; indeed in quadrant B an activation energy of 0.2eV is measured. Furthermore the current level in the device is now very close to that expected for the a-Si:H layer with low resistance contacts as shown by the dotted line marked on fig.6.3. The levelling off of the curves in quadrant A is due to the onset of the limiting effect of the track resistance which is typically 800Ω. To conclude, the I-V-T data appears to be in broad agreement with the suggestion that conduction is contact limited until the reverse bias junction has broken down.

∇.It has been pointed out since writting this thesis that the upturn in the activation energies seen in quadrant D may reflect the increase in the activation energy of the bulk a-Si:H which is commonly observed at temperatures of around 350K.

the I-V-T data appears to be in broad agreement with the suggestion that conduction is contact limited until the reverse bias junction has broken down.

6.5. Capacitance and conductance vs. frequency and voltage

Two sets of measurements have been made on the p^+ samples: capacitance (C) and conductance (G) as a function of frequency (f) from 100Hz to 1MHz, and capacitance as a function of applied bias at a fixed frequency of 1kHz. These measurements were made on large area devices with a pore diameter of 325μm using an a.c. signal of 20mV amplitude. The first of these measurements, C and G versus f, is shown in fig.6.7.

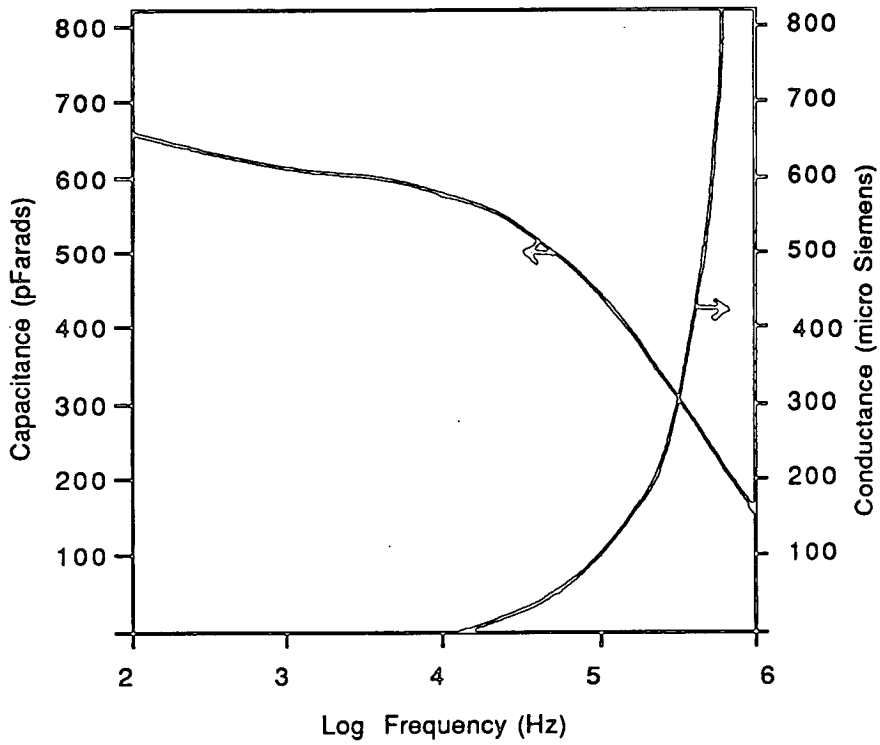

Fig.6.7 Capacitance and conductance vs. frequency for a Cr - p+ - Cr sample. The pore diameter is 325μm and the a-Si:H film thickness 90nm. The measurements were made at zero applied d.c. bias and at room temperature.

The capacitance shows a gradual decrease as the measurement frequency is increased

from 100Hz to 10kHz then proceeds to decrease rapidly. The conductance was too small to measure on our equipment at frequencies below $10^4 Hz$. Above this frequency, however, it increases steeply, as shown in fig.6.7. The second set of data, C versus applied bias, is shown in fig.6.8. As can be seen the capacitance shows a minimum centred at and symmetrical about zero volts. Two maxima appear at ±1.5V after which the capacitance falls rapidly.

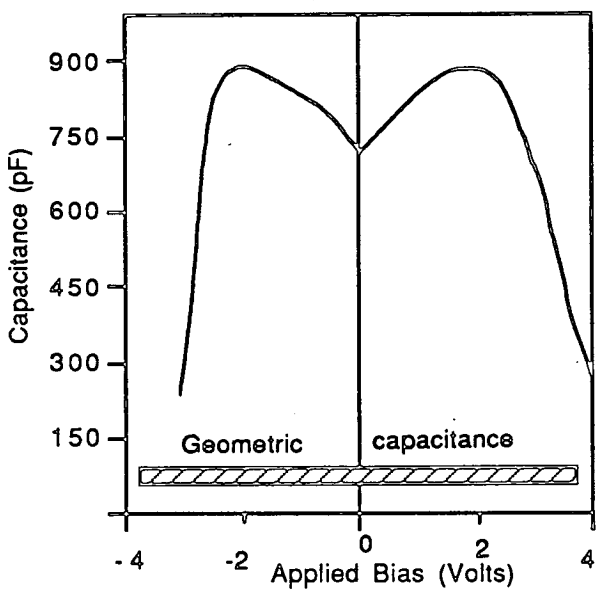

Fig.6.8 Capacitance vs. applied bias for a Cr - p+ - Cr sample. The a-Si:H thickness is 70-90nm and the pore diameter 320μm. The measurement frequency was 1kHz and the modulation 20mV

6.6. Discussion of capacitance and conductance measurements

6.6.1. Capacitance with zero applied bias

To interpret the data in these graphs and so relate these measurements to the physical properties of the device we need to recognise that the overall response of the device to an a.c. signal depends on both the frequency dependent properties of the a-Si:H and of the device as a whole i.e. a-Si:H plus the two contacts (this follows the methods used in §4.6.5 and by Snell et al.[3] to explain the capacitance measurements

on Schottky barriers). To do this it is useful to make use of an equivalent circuit for the device; this is shown in fig.6.9. The outer two sections represent the two barrier regions whose capacitances and resistances are denoted C1 and C3 and R1 and R3 respectively. The mid-section corresponds to the bulk a-Si:H between the barrier regions whose capacitance is C2 and resistance R2.

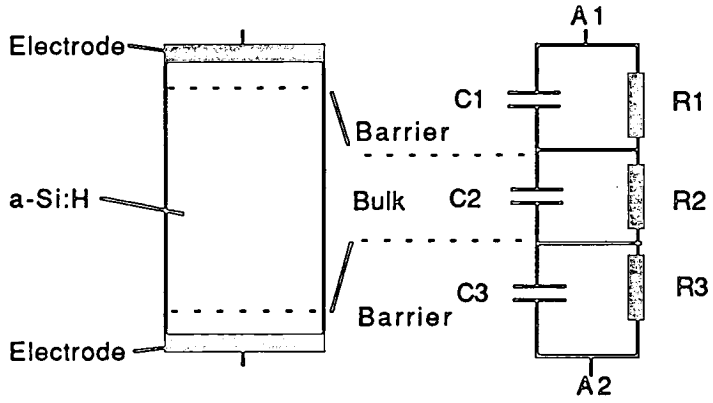

Fig.6.9 The equivalent circuit used to describe a metal - a-Si -metal device.

The capacitance and conductance of this circuit measured between terminals A1 and A2 can be deduced algebraically and it is found, not surprisingly, that both quantities depend explicitly on the values of every component in the circuit and on the frequency at which the measurement is made (see for example Grant & Phillips),[4] i.e.

$$C = C(C1,C2,C3,R1,R2,R3,f)$$

$$G = G(C1,C2,C3,R1,R2,R3,f)$$

When the magnitudes of the six R and C components appropriate to the p^+ devices are considered along with the frequency this complicated relationship becomes simpler and much more useful. The geometric capacitance of the bulk material situated between the two barriers, C2, can be found using $C = \epsilon\epsilon_0 A/d$ where A is the device area, d is the width of the a-Si:H outside the depletion regions and ϵ, the relative permittivity of silicon, is 11. For the devices used for these measurements C2 was about 65pF. R2 is the resistance of the bulk a-Si:H between the barriers and is equal to

$(d/\sigma A)$ where σ is the room temperature conductivity of the a-Si:H and d and A have the same values as before. The values of R1 and R3 are not known precisely although at zero-bias one can assume: (i) R1 and R3 are roughly equal (neither is forward or reverse biased), (ii) that both are much larger than R2 and , (iii) that R1 and R3 are each equal to half the zero-bias d.c resistance, i.e. $R1=R3=\frac{1}{2}(R\,|_{V=0})\gg R2$. The capacitances C1 and C3 should also be roughly equal to each other at zero-bias and comparing previous data for a-Si:H barrier capacitances [3] it is expected they will be much larger than C2, i.e. $C1=C3\gg C2$. Accounting for all these assumptions the analysis of the circuit reveals that at zero-bias and at frequencies below $10^4 Hz$ the measured capacitance is dominated by the two barrier capacitances C1 and C3 i.e. $C=C(C1,C3)$, and because they are in series the measured value is half that of either C1 or C3. At frequencies above $10^4 Hz$ the measured capacitance tends to the geometric capacitance, C2.

From fig.6.7 the measured capacitance per cm^2 at 100Hz is $780 nF/cm^2$ so the actual barrier capacitances will be twice this i.e. $1.6\mu F/cm^2$. Using the simplified representation of the barriers as flat plate capacitors the barrier width can be estimated from the equation $C=\epsilon_0\epsilon A/d$ to be around 4nm. As the frequency is increased the capacitance decreases first gradually up to $10^4 Hz$ and then much more rapidly. The gradual decline reflects the frequency dependence of the carriers' response to the a.c. signal, a process that has been outlined in §4.6.4. The more dramatic fall for frequencies above $10^4 Hz$ reflects the overall response of the specimen as the measured capacitance tends to that of the geometric capacitance which can be calculated to be about 65pF.

6.6.2. Capacitance and conductance with applied bias

The form of this curve can be explained in the following way. When a bias of either polarity is applied to the device one barrier is forward biased and the other

reverse. The capacitance of the forward biased junction increases rapidly with increasing bias (see §4.6.5) but at the same time its resistance decreases rapidly. This resistance drop has the effect of 'shorting' out the barrier capacitance such that it no longer contributes to the measured capacitance. The capacitance of the reverse biased junction decreases slowly with increasing bias and its resistance, whilst two or three orders of magnitude higher than that of the forward biased junction, also decreases. With the forward biased barrier resistance now low the capacitance of the reverse biased barrier dominates the overall device capacitance. As a result the measured capacitance increases as seen in fig.6.8 for biases up to ± 1.5V to 2V. Beyond these voltages the measured capacitance starts to decrease. This can be related to the reistance of the reverse biased junction which at these voltage levels is expected to fall quite quickly as breakdown approaches. The capacitance of the reverse biased barrier will contribute less and less to the measured capacitance and the overall device capacitance will fall, eventually reaching the geometric capacitance.

To summarise the capacitance measurements, it appears that the observed C and G vs frequency and bias data of the unformed p^+ device can readily be explained in terms of the equivalent circuit in fig.6.9 if account is taken of the changing values of the barrier resistances and capacitances as the applied bias is changed. The barrier capacitance for devices made with p^+ a-Si:H with a doping of $10^4 vppm$ has been found to be $1.6\mu F/cm^2$and there are indications from the C-V measurements that the onset of reverse biased breakdown is around 2V.

6.7. Summary of results from unformed samples

The results from both d.c. and a.c. measurements on the unformed Cr-p^--Cr devices have been presented and discussed, and a picture of the electrical make up of the device has been established. The main conclusions are:

(1) For biases up to 2-3V conduction in the device is contact limited.

(2) The high resistance of the contact appears to be accounted for in terms of a Schottky type potential barrier which, under reverse bias, is blocking to the hole current. Calculations of the zero bias barrier width using the method of Spear et al. [2] put it at 10nm whilst experimental observations coupled with an approximate calculation put it at less than this, perhaps perhaps around 4nm.

(3) Up to 4V the activation energy of the device appears to be that of conduction across the reverse biased barrier and is found to be 0.1eV. This probably indicates holes are crossing the barrier by field assisted thermionic emission at 0.1eV above the Fermi level of the metal.

(4) The reverse biased barrier appears to break down at 2-3V; once this has happened the current seems to be limited by the bulk resistance of the a-Si:H.

6.8. Forming

The forming circuit, described in §5.3, was used to apply a voltage pulse across the devices. The pulse, and the associated device current, were monitored on a double trace oscilloscope. As mentioned in §3.2, it is possible, using a string of pulses, to gradually reduce the resistance of p^+ devices from their virgin resistance of about $10^8\Omega$ to around $10^6\Omega$; this has become known as 'soft forming'.[5] (This behaviour contrasts with the forming of p-n-i devices which, with a single pulse, show a discontinuous drop in resistance to a lower value of $10^4-10^3\Omega$.) With most of the p^- samples this gradual forming step was achieved using less than five pulses of 10-15V height and 100ns-1μs duration. It was found that applying positive voltages to the top contact of the device gave the most successful subsequent switching, although devices formed with the opposite polarity were also found to work. Once the p^+ devices had undergone

this initial modification they were switched using pulses of around 2-4V. A set of I-V characteristics for a p^+ device in its pre-formed and post-formed states is shown in fig.6.10; the details of the switching are discussed in the next section. If a slightly larger or longer pulse than that required to perform the soft forming was used the p^+ devices formed to a low resistance state of between $10^4-10^3\Omega$. In this respect their behaviour closely resembled the forming process of the p-n-i devices.

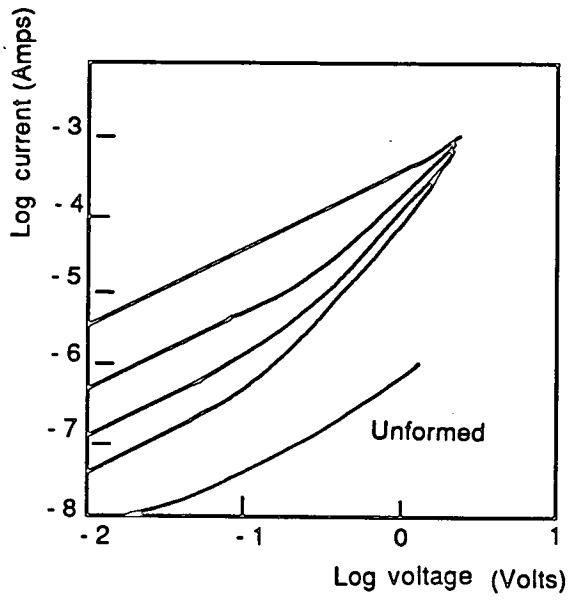

Fig.6.10 A set of I-V characteristics for a Cr - p+ -Cr sample showing it in the pre-formed state and a number of subsequent memory states.

Forming of p^+ devices created a filament similar in outward appearances to that produced in the p-n-i devices,[6] namely it showed up as a dark spot around the centre of the pore area with a diameter of about 0.5μm when viewed in transmission with a light microscope. Some devices also showed a spot of surface damage on the top electrode directly above, or close to, the filament. It is unclear at this stage whether the filament is created by the initial soft forming process or by the subsequent switching.

6.9. Discussion of forming

From the I-V characteristics of fig.6.10, it's clear that the formed state is at least two orders of magnitude more conductive than the unformed state. It was established in the previous chapter that, at biases below 2-3V, the current in the unformed device is limited by the resistance of the Schottky barriers. In the formed state it seems reasonable to conclude that the Schottky barriers have, in some way, been modified and become more conductive. The measurements made with thermochromatic liquid crystals on formed p-n-i devices,[6] revealed that in these samples the device current was concentrated along the filament. Although these measurements have not been repeated for p^+ devices, there are no obvious reasons why, as a similar filament appears to be formed, that the same should not hold true in this instance. The modification of the Schottky barriers may, therefore, amount to their penetration by the conductive filament. A schematic representation of this situation is shown in fig.6.11.

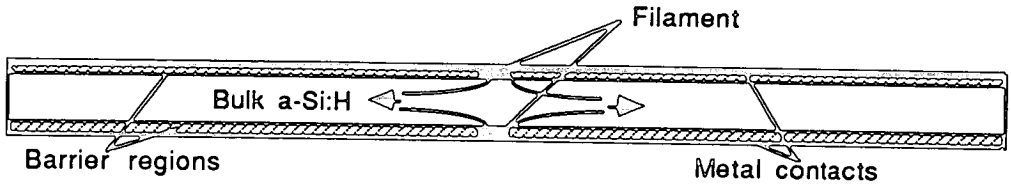

Fig.6.11 A schematic representation of the formed a-Si:H device showing the penetration of the two Schottky barrier regions by the filament and the spreading of the current into the a-Si:H layer, as indicated by the arrows.

As will be seen in the next section the I-V characteristics of the formed samples are symmetrical about zero volts, it appears probable, therefore, that both Schottky barriers have been penetrated by a filament.

6.10. Switching and current-voltage characteristics

Once the forming stage had been completed the subsequent switching was achieved using voltage pulses of $\pm$2-4V with a minimum duration of 10ns. It was

found that the devices switched most readily if the Write (Off to On) pulse polarity was the same as the forming pulse. The Erase (On to Off) was of the opposite polarity. Fig.6.10 shows a set of I - V characteristics in which the unformed device has been formed with the positive voltage applied to the top contact, and then switched with a further pulse to a range of resistance states. The intermediate states were obtained by using voltage pulses that were a few hundreds of millivolts less than those required to make a direct transition between an Off and On state.

6.11. Discussion of switching

An interesting feature of the curves in fig.6.10 is that at higher voltages they appear to converge to a single point at a voltage virtually identical to the switching voltage. This implies that , although at a low voltage of say 0.5V there may be three orders of magnitude difference between an On and Off state resistance, at the voltage used to switch the device there is little difference. At this voltage the resistance of the sample is around 3kΩ. This observation is important when considering the power dissipation in the device during a switching pulse. As the I-V characteristics of fig.6.10 are symmetric about zero volts it implies there is little difference between the power dissipated in Erasing and Writing the device. (The energy dissipation during switching is dealt with in more detail in Chapter 9.)

6.12. Capacitance and conductance vs. frequency for different memory states

Using p^+ pore devices with a diameter of 50μm, it was possible to measure the device capacitance as a function of memory state resistance. The results, shown in fig.6.12, demonstrate a continuous decrease in the device capacitance with decreasing memory state resistance and also with increasing frequency. The frequency dependence of the capacitances appears to be of the same order in the unformed and formed devices. The dependence of the device conductance on frequency for different memory states is shown in fig.6.13. Included is a curve for the conductance of the virgin device

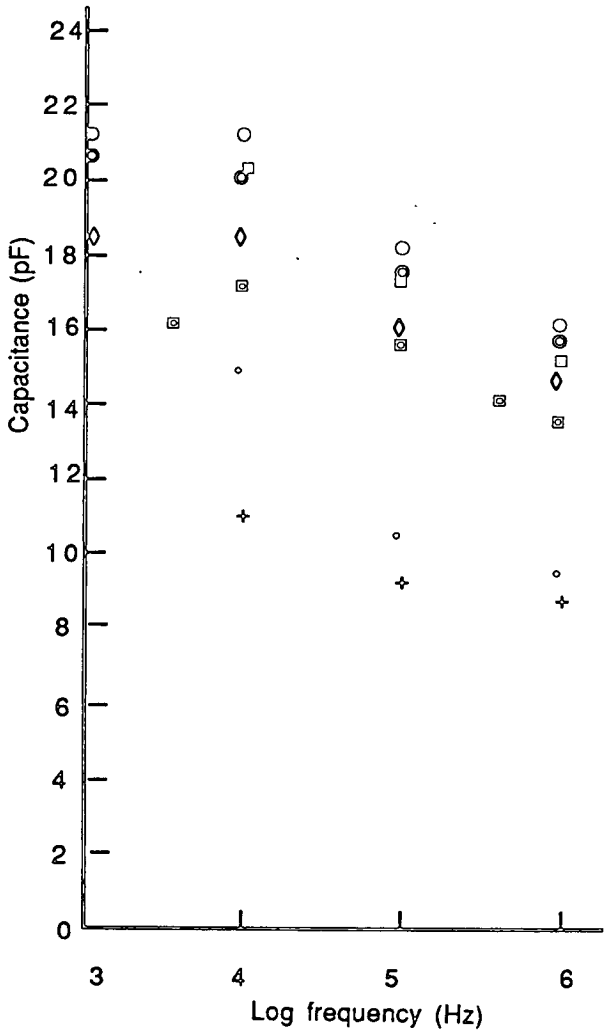

Fig.6.12 Capacitance versus frequency for the pre-formed device (○) and different memory states of a p+ device with a 50micron diameter pore. The room-temp. resistance of the memory states measured at 0.5V is :
(◦) 2.2kOhm, (+) 5kOhm, (⊠) 11kOhm, (◊) 20kOhm, (□) 0.1MOhm, (⊙) 5MOhm.

as a function of frequency. As can be seen the conductance increases, at all frequencies, in moving from high resistance Off states to low resistance On states. It also increases with increasing frequency, this increase being much more dramatic in the Off states than the On states.

6.13. Discussion of the capacitance and conductance data

It was established in §6.6 that the C and G versus frequency dependence of the unformed devices could be described by the equivalent circuit of fig.6.9. In the

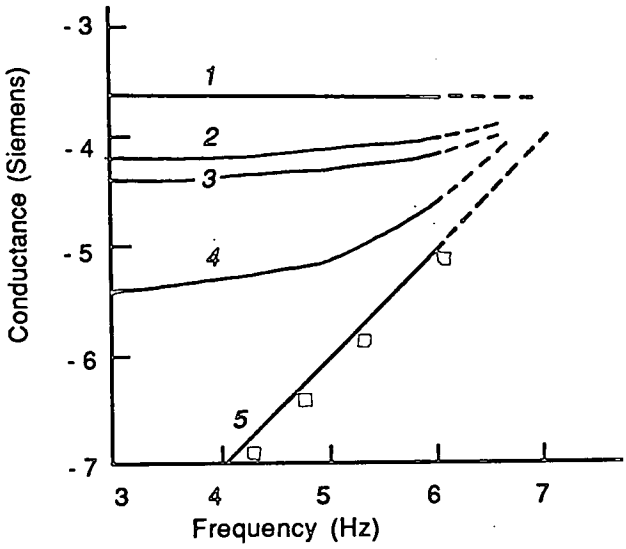

Fig.6.13 Conductance versus frequency for a Cr - p+ - Cr device with a pore diameter of 50μm in a range of memory states. Also shown is the conductance of the unformed device as indicated by the □ . The individual curves are refered to in the text.

formed state this circuit needs to be modified to account for the presence of the filament. It was suggested in the previous section that the filament extends at least as far as to penetrate the two barrier regions, as shown by the black filled areas of fig.6.11. In doing so the filament provides a current path from the metal electrodes to the bulk a-Si:H, as shown by the arrows. In the equivalent circuit of fig.6.9 the resistors R1 and R3 represent the overall resistance across the barrier capacitances C1 and C3. In the virgin device this was the contact resistance but in the formed device R1 and R3 must now account for both the contact resistance and the contribution of the filament. As the filament resistance is less than the contact resistance and is effectively in parallel with it the values of R1 and R3 will be reduced. If they are reduced to a sufficient extent the measured value of the capacitance will fall because, as was pointed out in §6.6.1 previously, the measured capacitance is a function of R1 and R3. In fact the lower the values of R1 and R3 the lower the measured capacitance values will be. Overall, if with decreasing device resistance the resistance of the filament material shown in fig.6.9 also decreases, the measured capacitance will decrease as is seen in the data of fig.6.12. Although this line of argument offers a qualitative explanation of the

results, difficulties in modelling the device quantitatively have meant that it has not yet been established whether the presence of the filament alone can account for the size of the changes in the capacitance observed. If it is found that this explanation is incorrect then the most obvious alternative would seem to be that changes outwith the filament are resulting in a modification of the barrier profille, and therefore its capacitance. In these modified areas the barrier profile would, broadly speaking, be expected to be at its narrowest and therefore with its highest capacitance when the device was in the Off state. The mechanism by which this sort of change might occur is uncertain; it could conceivably be either an electronic or structural effect.

The conductance of the device, again as shown in §6.6.1, is a function of frequency and the various resistive and capacitive elements of the device. The data of fig.6.13 shows that the conductance of the most conductive samples (curves 1,2 and 3) is relatively frequency independent and matches quite closely the d.c. value of the conductance. This reflects the fact that the device conductance in these memory states is dominated by the resistive elements whilst the capacitative elements (the ones that introduce the frequency dependence) are not noticeably affecting the measured value. Curves 4 and 5 for more resistive memory states, however, show a much greater frequency dependence. Broadly speaking this reflects the diminished contribution of the resistive elements and the enhanced contribution of the capacitative elements. To account for the form of the data in fig.6.13 in a quantative way requires a description of the effect of the filament on the equivalent circuit of fig.6.9, i.e. one would follow similar arguments to those outlined in the previous paragraph in the discussion of the capacitance. If this is done the same conclusions are arrived at as in the previous paragraph, namely that if the filament material acts to provide a conductive path across the barrier regions and, that during the switching the resistance of this filament material scales with the device resistance, then qualitatively we expect curves similar to those

shown in fig.6.13. As in the case of the capacitance, however, difficulties in adequately accounting for the filament in an equivalent circuit have prevented quantitative predictions to be made and so a degree of uncertainty in the interpretation of these results remains.

6.14. Summary of observations of forming and the post-formed state

The forming process and the electrical characteristics of the formed state of Cr-p^+-Cr devices have been described. These samples can be 'soft' formed to a resistance of about $10^6\Omega$ using pulses of 10V to 15V with a duration of 100ns to 1μs. Using slightly higher forming pulses the device forms to a lower resistance of $10^4-10^3\Omega$. A filament is formed which appears in a light transmission microscope as a dark spot and sometimes has associated with it a region of damage at the surface of the top contact. It has been suggested that at the very least the filament penetrates both the Schottky barriers at the metal to a-Si:H interfaces i.e. a distance of at least 4nm at each barrier.

Switching the formed devices has been achieved with pulses of 2V to 4V with a minimum duration of 10ns. The switching is polarity dependent with the Write pulses (Off to On) being of the same polarity as the forming pulse and the Erase pulses (On to Off) of the opposite polarity. The devices can be switched to a continuum of states whose resistances, measured at 0.5V, can range from 1kΩ to 1MΩ and whose I-V characteristics are symmetrical about 0V to within a factor two. An interesting feature of the I-V characteristics of different memory states is that they tend to converge at voltages of 2V to 3V i.e. at these voltages the resistance of all memory states is roughly equal.

The zero bias capacitance and conductance of devices with a pore diameter of 50μm has been found to be dependent on the resistance of the memory state. The capacitance decreases with decreasing memory resistance and increasing frequency

whilst the conductance increases with frequency. A complete explanation of the capacitance and conductance data has not yet been found although a qualitative explanation relating these observations to the changing resistance of the filament has been proposed.

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Chapter 7

On-state conductivity at 4.2K

7. Introduction

At temperatures close to the normal boiling point of helium i.e. 4.2K, kT falls to below 1meV forcing electrical conduction to take place in states at, or close to, the Fermi level. Measurement of the conductance of a material at these temperatures, therefore, offers a means of probing the density of states at the Fermi level. In this chapter I describe such an investigation made on formed p-n-i devices in the On state with room temperature resistances of less than 5kΩ. The results reveal interesting information about the composition and structure of the filament.

7.1. Experimental procedure

All the devices used in this series of experiments were p-n-i devices with a 10μm diameter pore (p-type doping 10^4 vppm 300nm, n-type doping 30vppm, 700nm, i-type undoped, 700nm). Four different metals, Al, Cr, Au and Fe, have been used for the top electrode material, the bottom contacts were all made of Cr. Devices were formed and switched a number of times in the usual way and left in the On state. They were then packaged in 24 pin DIL chip carriers and mounted in the liquid helium cryostat, the operation of which was detailed in §5.6. The electrical measurements were made using a phase sensitive detector in conjunction with a d.c source and a sinusoidal voltage signal generator; again the details are found in §5.5. The data obtained from this set up is in the form of (dV/dI), the dynamic resistance of the device, versus the d.c bias across the device. A magnetic field of up to 0.2 Tesla could be applied to the sample by a magnet situated outside the cryostat sample chamber.

7.2. Introduction to results

During the course of these investigations it became clear that over certain temperature ranges the samples with Al top contacts were behaving in a fundamentally different way to the samples with Cr , Fe and Au top contacts. For this reason the

description and discussion of the results for Al devices have been separated from that of the other samples.

7.3. Results from Al top electrode samples

The typical temperature dependence of the dynamic resistance, (dV/dI), measured at a moderate bias ($=40mV$) is shown in fig.7.1, the resistances having been normalised to the value at the lowest temperature.

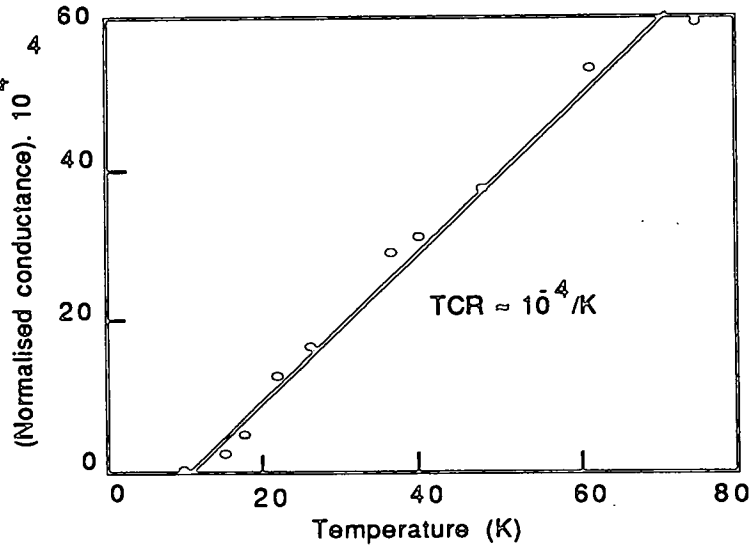

Fig.7.1 The change in conductance with increasing temperature (normalised to the conductance at the coldest temperature) for a formed p-n-i sample with a Cr bottom and Al top contact. The resistance of the sample at room temperature was less than 1kΩ.

Over this temperature range the dependence is linear with a temperature coefficient of resistance of $10^{-4}/K$, i.e. conduction is weakly thermally activated.

The bias dependence of the dynamic resistance (dV/dI) at low bias ($<\pm 15$ mV) around at 4.2K is shown in fig.7.2. It can be seen that (dV/dI) peaks symmetrically about 0V, and has a plateau region at 0V. The maximum change in (dV/dI) over this region was

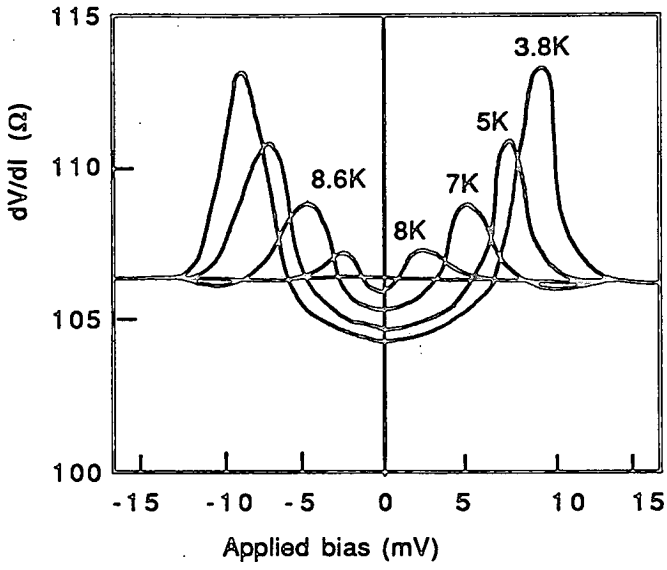

Fig.7.2 (dV/dI) versus temperature and bias for a sample with Al top contacts. The a.c. modulation voltage across the sample is 0.2mV.

found to vary from sample to sample in a range of between 1 to 10 % at 4K. The raw data of fig.7.2 can be transformed to a plot of resistance (rather than (dV/dI)) versus current by a numerical process described in appendix I. This new plot is shown in fig.7.3 and as can be seen the picture is reduced to one in which the sample resistance increases by about 1% as the current through the sample is increased.

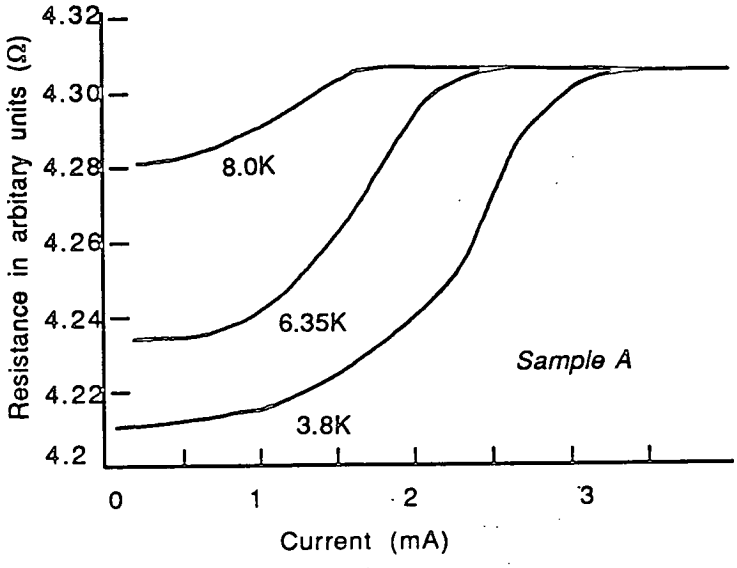

Fig.7.3 Resistance versus current and temperature for a sample with an Al top contact.

(These curves are deduced from dV/dI versus bias data.)

Plotting the zero bias resistance against temperature reveals a similar transition taking place as the temperature is increased, as shown in fig.7.4.

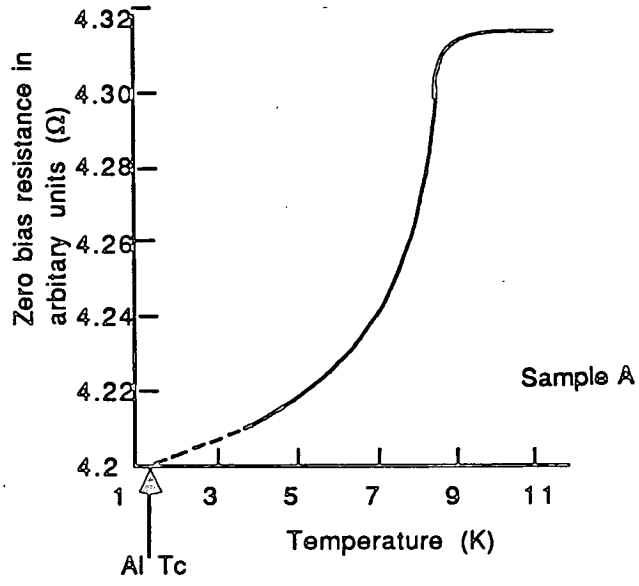

Fig.7.4 Zero bias resistance versus temperature for a sample with an Al top contact.

It was also found that the transition from a low to high resistance took place when a magnetic field was applied across the device, as shown in fig.7.5.

7.4. Results from Cr ,Fe and Au top electrode samples

For the samples with Cr electrodes the variation in (dV/dI) as a function of temperature (up to 100K), measured at a bias of 100mV, was found to behave as T^n, where $1 \leq n \leq 2$. The Cr top electrode samples showed a greater fractional decrease in (dV/dI) per unit rise in temperature than the Al top electrode samples. The averaged TCR values over the temperature range 100K to 4K was about $10^{-3}/K$. The (dV/dI) of the Au samples measured at a bias of 150mV showed a similar temperature dependence to the Cr samples with a similar TCR value of around $10^{-3}/K$. (No measurement of the high bias (dV/dI) of samples with Fe top electrodes were made).

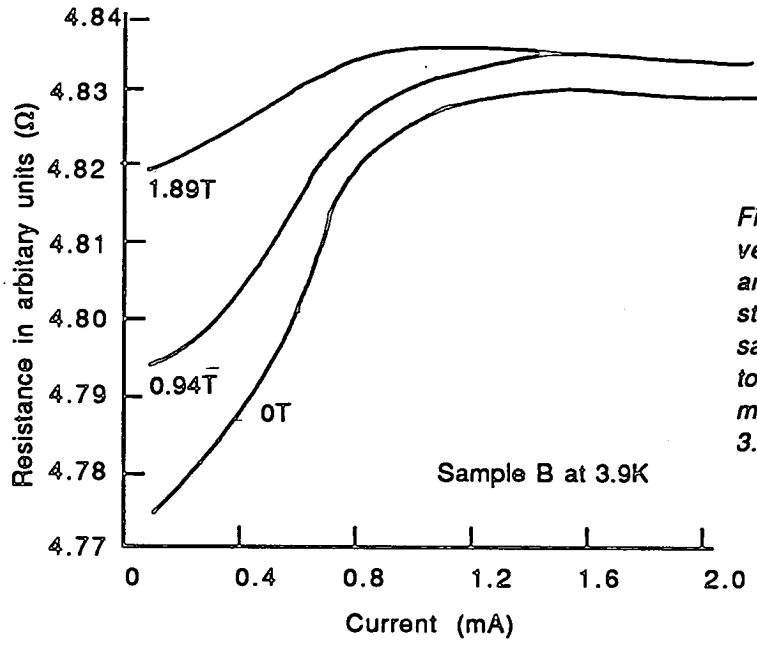

Fig.7.5 Resistance versus current and magnetic field strength for a sample with an Al top contact. Measurements made at 3.9K.

The form of the (dV/dI) curves close to zero bias was found to be similar for the Cr, Au and Fe samples. These are shown in fig.s. 7.6, 7.7 and 7.8 respectively.

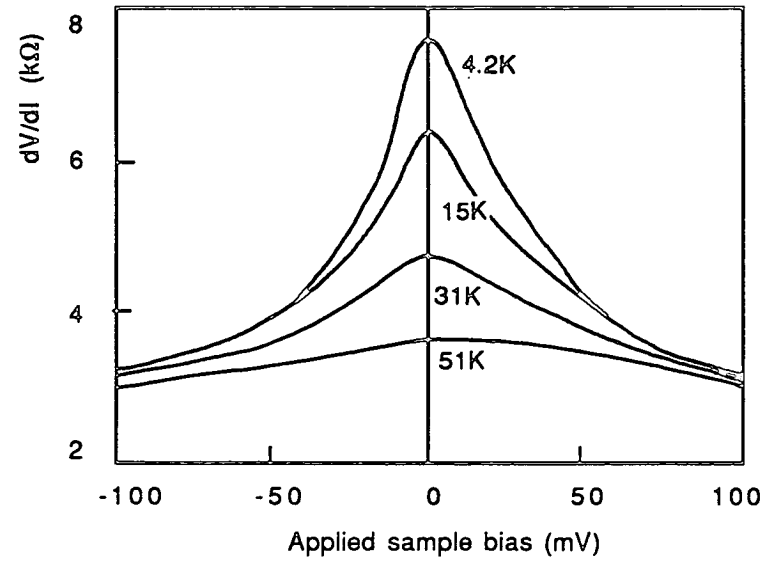

Fig.7.6 (dV/dI) versus bias and temperature for a sample with a Cr top contact.

They all show pronounced peaks centred about 0V at low temperatures, which gradu-

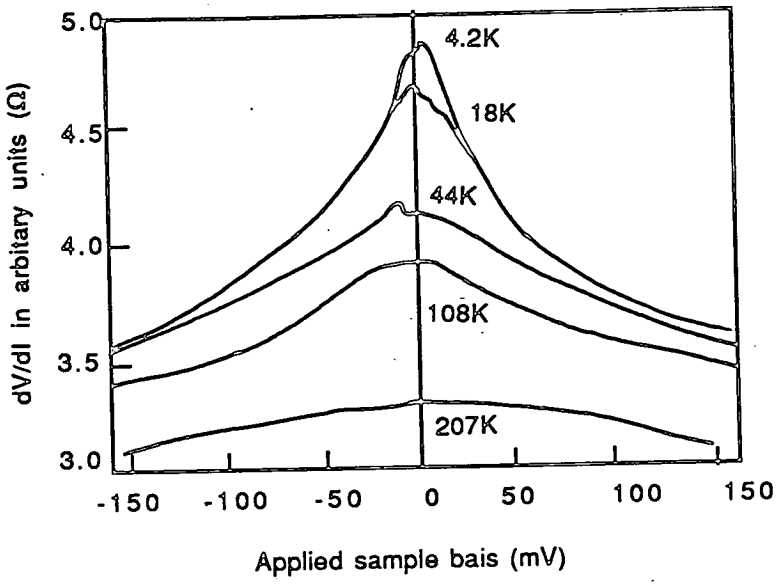

Fig 7.7 (dV/dI) versus bias and temperature for a sample with a gold top contact.

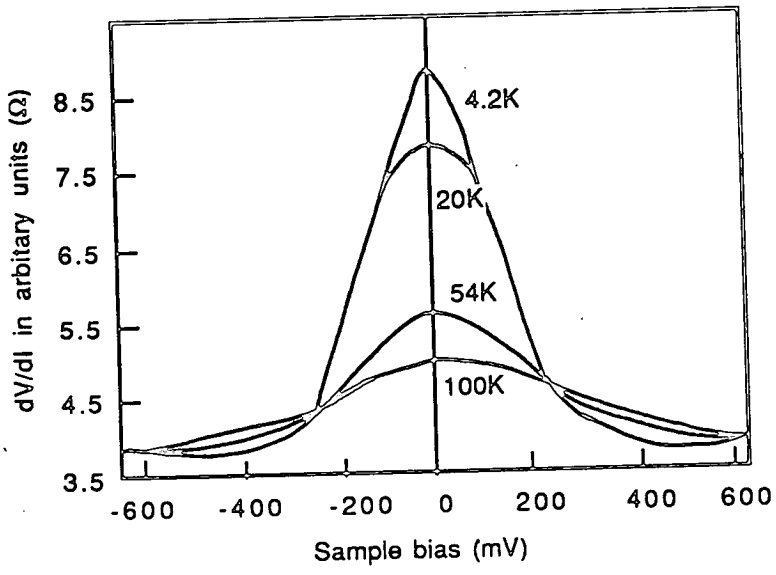

Fig.7.8 (dV/dI) versus sample bias and temperature for a sample with an Fe top contact.

ally decrease in height as the temperature is raised. The size of the peaks varied from sample to sample and in some represented a change of only one percent compared to the value at higher bias. An applied magnetic field of 0.2 Tesla did not have any observable effect on the Cr and Au samples, and only one of the Fe samples showed

very slight and inconsistent sensitivity to the presence of the magnetic field.

7.5. Discussion of results from Al top electrode samples

Measurements with liquid crystals have established that at room temperature conduction in the On state takes place along a filament.[1] There is no obvious reason why the same should not happen at lower temperatures. The TCR of the Al samples as deduced from fig.7.1 therefore tells us much about conduction within this filament. Any amorphous semiconductor, even heavily doped, would show a much larger increase in resistance than we see in these samples when cooled from room temperature to 4.2K . It is clear from this that there exists a conduction path between the two electrodes that is made of material other than unmodified a-Si:H, or in other words the filament must extend right through the device. Furthermore, conduction in the filament must be taking place at or close to the Fermi level of the filament material. Two processes seem to be available to account for the high conductivity of the sample at these temperatures: crystallisation of the a-Si:H and/or, the injection of metal from the electrodes into the a-Si:H.

Crystallisation of the Si can only explain the observed resistance at 4.2K if the Si making up the filament is heavily doped. Data from the literature [2] suggests that both n and p-type Si doped to impurity concentrations greater than $10^{18} cm^{-3}$ gives rise to resistivities at 4.2K of less than $10^{-1} \Omega cm$. Taking the filament diameter to be 0.5μm , its length 1μm and making use of this value of resistivity gives a filament resistance of 4kΩ - close to that measured experimentally. The i-type layer of our device clearly cannot give rise to crystalline material with resistivities as low as this. The n-type layer is prepared using a phosphine to silane ratio, (N_{PH3}/N_{SiH4}), of 3.10^{-3} which, making use of data from Spear and LeComber[3] is equivalent to an ionised dopant concentration in the a-Si:H film of about $7.10^{16} cm^{-3}$. This is somewhat lower than $10^{18} cm^{-3}$ and so the n-type a-Si:H when crystallised is likely to have a resistivty

greater than $10^{-1}\Omega cm$. The heavily doped p-type layer is prepared using a diborane to silane ratio, (N_{B2H6}/N_{SiH4}), of 10^{-2} which is expected to correspond to a dopant concentration in the film of $10^{18}-10^{19}cm^{-3}$. This material when crystallised would be expected to have a resistivity of $10^{-1}\Omega cm$ or less. To explain the low resistance of the device at 4.2K by crystallisation alone requires, therefore, that the i and n-type layers be penetrated by heavily doped p-type Si. Bearing in mind the high field strengths and energies associated with forming it is hard to rule this out.

The injection of metal from the electrodes into the a-Si:H can give rise to a number of effects. A continuous metal filament joining the two electrodes could be created. This has been reported as taking place in SiO memory devices (§2.4.2), however, the TCR of a metal filament should be positive, which is not what we observe. If the injected metal mixes intimately with the silicon a metal-Si alloy would be formed. The electrical properties of such materials, which were discussed in §4.8, can vary from semiconductor-like to metal-like depending on the composition of the alloy. It is quite possible that an Al-Si or Cr-Si alloy could have a TCR similar to that seen here.[4] At this stage it is difficult to decide whether metal injection , crystallisation of the a-Si:H or a combination of the two is responsible for the low temperature electrical properties of these devices; the following section provides further information.

The increases at low bias (<150mV) in the device resistance with increasing temperature, current and magnetic field strength, as shown in fig.s 7.3,7.4 and 7.5, can be most satisfactorily explained in terms of a normal to superconducting transition of part of the material along the conduction path. If this suggestion is correct then from fig.7.4 it appears that an upper limit for the transition temperature lies between 8 and 9K i.e. beyond this temperature all the superconducting material has become normal. This is considerably higher than the 1.5K transition temperature for Al. Chromium, which is used to make the bottom contacts does not superconduct in its

bulk form although it has been reported that thin films can do so. The Cr tracks that run the length of the sample piece did not, however, show any evidence of superconductivity even at 3.8K. To my knowledge the only report that can explain these observations is that by Meunier et al. [5] which describes the superconducting properties of Al-Si mixtures. Fig.7.9 taken from this paper shows how the superconducting transition temperature of these mixtures can be as high as 8.3K depending on their composition.

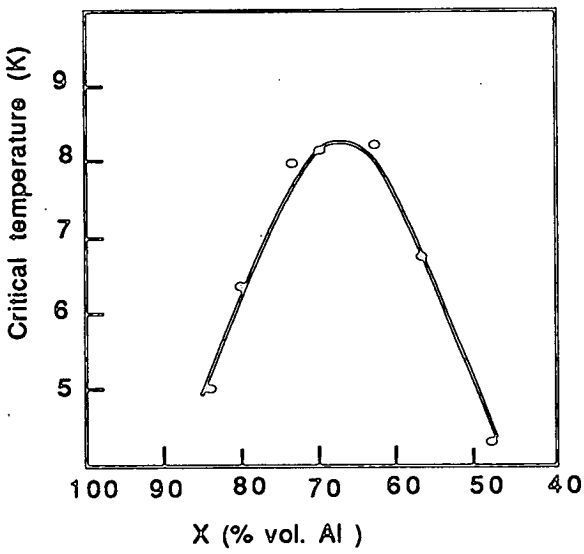

Fig. 7.9. Composition dependence of the superconducting transition temperature for a-Si implanted Al film. (After ref. 5).

It seems probable, then, that somewhere in the device there has been some intermixing of the Al from the top electrode and the a-Si:H layer. Fig.7.4 demonstrates that the transition in the devices occurs over a broad temperature range. It is likely, therefore, bearing in mind the data in fig.7.9, that the superconducting region in the devices contains Al-Si alloys of a range of compositions each with its own transition temperature, the lowest I have measured being 3.8K and the highest 8.2K. This implies a mixture with an Al composition varying between 50 and 90%.

The data of figs. 7.3 and 7.5 lend weight to the suggestion that a superconductor is present, as both show behaviour characteristic of these materials. The low to high

resistance transition caused by increasing the current through the device, as seen in fig.7.3, can be understood in terms of the quenching of the superconductor once a critical current is exceeded. The current driven transitions occur gradually with increasing current indicating either that the superconductor has an intermediate state (as in a type II superconductor)[6] and/or that different parts of the conduction path have different critical currents. The latter could occur in two ways: (1) If the cross-section of the conduction path was non-uniform it would cause fluctuations in the current density (as occurs at a constriction in a wire), or, (2) as suggested in the previous paragraph , if the superconducting material is inhomogeneous there will exist a range of critical currents each associated with a particular composition.

The data of fig.7.3 can also be explained in terms of Joule heating in normal material raising the temperature of adjacent superconducting material above its critical temperature and so driving it normal too. The overall amount of Joule heating will increase with device current and so more and more material will be driven normal. The data of fig.7.5 shows the quenching of the superconductivity by a magnetic field. The gradual nature of the transition implies that there is a range of critical field strengths, again lending weight to the notion of there being a range of compositions each with its own critical field strength.

There seems to be strong evidence, therefore, that the Al of the electrodes and the a-Si:H have mixed. Bearing in mind the many reports of the readiness of Al to migrate under high fields into c-Si [7,8,9] it seems most probable that the Al has migrated into the a-Si:H film rather than the other way round.

7.6. Discussion of results from Cr, Fe and Au top electrode samples

The TCR at 100mV for these samples has been found to be about $10^{-3}/K$. This leads one to similar conclusions about the post-formed conduction mechanism in these

samples to those arrived at in the discussion of the Al top electrode devices, namely a filament of modified material must join the two electrodes and that conduction in this material takes place in states close to the Fermi level.

Peaks in (dV/dI) similar to those shown in figs. 7.6, 7.7 and 7.8 have been reported by a number of workers.[10,11,12,13,14] The effect was explained in 1968 by Zeller and Giaever [14] who showed the resistance peaks to be a manifestation of a conduction mechanism in which transport of electrons involved activated tunnelling between small metal particles embedded in an insulating matrix. The structure of their devices is shown in fig.7.10 and the dynamic resistance obtained from these samples as a function of temperature and bias is shown in fig.7.11.

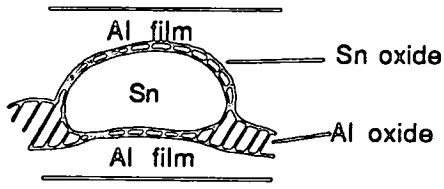

Fig.7.10 The tunnel junction used by Zeller and Giaever seen in cross-section. *(After ref.14)*

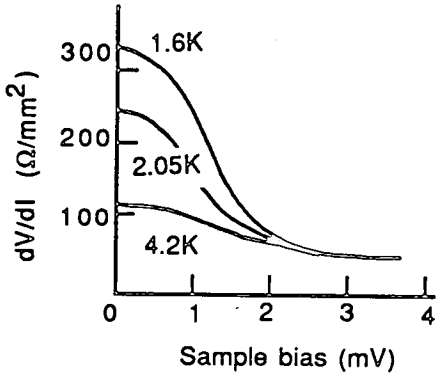

Fig.7.11 Dynamic resistance versus voltage and temperature from Zeller and Giaever's tunnel junction. The average particle size is 150Angstroms. (After ref14)

Zeller and Giaever argued that electrons tunnelling into the metal particles have a non-negligible activation energy. This energy exists because each metal particle has a capacitance with respect to the electrodes and neighbouring particles and in putting an extra electron on to the particle an energy equal to the increase in the electrostatic

energy of this capacitance has to be provided. (This is the same as doing work when a flat plate capacitor is charged up.) To put one electron on to a metal particle the energy required is $E = e^2/2C$ (Joules) where C is the capacitance of the particle. An electron making the tunnelling transition can obtain this energy thermally. At sufficiently low temperatures E becomes commensurate with kT and the rate of electron tunnelling and therefore the conductance of the device decreases with decreasing temperature. The electron can also get the required energy from the electric field, as demonstrated by fig.7.12. In moving along the direction of the field the electron gains an energy of $e\Delta V$ which, if the field strength is sufficiently strong, can exceed the activation energy E.

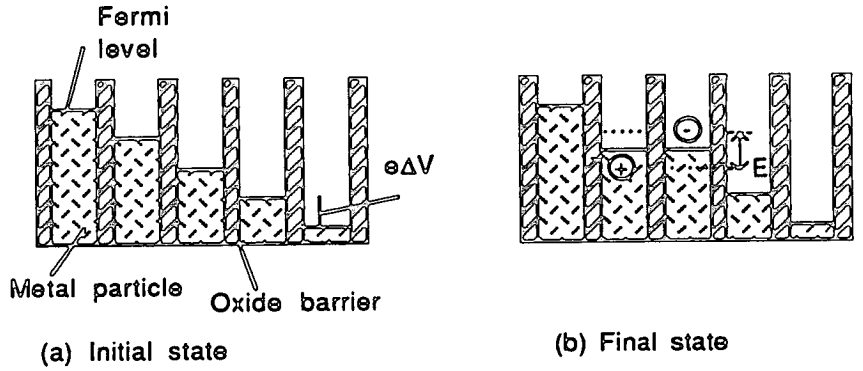

Fig.7.12 Schematic illustration of the effect of an electric field on the electronic energy levels in an idealised granular metal. The voltage drop between adjacent grains is ΔV. (a) In this initial state there are no free carriers present, (b) an electron tunnels along the direction of the field to a neighbouring metal island where it occupies the first permitted energy state of that particle. A hole is left at the particle from which the electron came. (After ref.14)

Conductance can, therefore, be both temperature and field dependent. Overall, as is seen clearly in fig.7.11 taken from Zeller and Giaever,[14] the device resistance is at its highest at low fields and temperatures but decreases as either field or temperature is increased. This closely resembles the observations made on the a-Si:H samples.

If this mechanism explains the observations of zero bias resistance peaks in a-Si:H

samples it implies that somewhere along the conduction path of the devices there is a region of material in which small metal islands are embedded in the insulating matrix of the a-Si:H. This would fit with the conclusion drawn from the general observations of the TCR of these devices, namely,that one way of accounting for the high level of conductivity at low temperatures is to imagine that metal from the electrodes has entered the a-Si:H film.

There is, however, a second way of relating the mechanism suggested by Zeller and Giaever to our devices and that is to take the 'metal islands' to be made not of metal but of particularly highly doped and, therefore conductive, silicon and the 'insulating matrix' to be made of less conductive silicon. Conduction would then take place by activated tunnelling between the islands of heavily doped silicon. In the a-Si:H devices this situation might arise if the doped n or p a-Si:H mixes with the i-layer. This type of structure has been hinted at as a possible cause of zero bias resistance peaks in heavily doped silicon diodes [11] but there appears to be no reports of direct observations of resistance peaks caused by such a mixture of differently doped silicon.

7.7. Summary

The electrical properties of p-n-i samples in the On state have been investigated down to 4.2K. The most important observation is that conduction remains only weakly thermally activated down to 4.2K. The samples with Al top contacts showed a TCR of $10^{-4}/K$ and the other samples, with Cr, Au and Fe top contacts, higher values of around $10^{-3}/K$. This implies that, firstly, in these devices the filament extends the whole way through the a-Si:H layer connecting the top and bottom contacts and, secondly, that the filament is made of material that has a high density of states at or near the Fermi level. This strongly suggests a filament made of crystallised and highly doped silicon or of a material comprising a mixture of metal and silicon.

The presence of a possible superconducting to normal transition in the Al samples and the zero bias resistance peaks of the Cr, Au and Fe samples all lend weight to the suggestion that metal has migrated in to the a-Si:H from the contacts. In the case of the Al samples it appears that somewhere along the filament there exists a Si/Al alloy that contains at least 50% Al. For the Cr, Au and Fe samples it is difficult to estimate the concentration of the metal in the material that is causing the zero bias resistance peak but it is clear that in certain regions at least these metals are not forming an intimate mixture with the silicon but are giving rise to a material that contains regions of high conductivity embedded in a less conductive material.

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Chapter 8

Silicon contact devices

8. Introduction

At the simplest level of enquiry the metal contacts of the a-Si:H switching devices can be regarded as nothing more than 'contacts', i.e. their sole function is a means of making a low resistance connection to the a-Si:H. If this were really the case then it would follow that the processes of forming and switching should be attributable entirely to properties of the a-Si:H layer. For example, the high current density during forming may give rise to sufficient temperature increase to crystallise part of the a-Si:H thereby creating the filament.

An alternative view could, however, attach more significance to the presence of the contact metal. Two possible roles seem to be particularly obvious; the first is that the metal to semiconductor contact creates an electronic environment at the interface conducive to forming and switching. The second is that the contacts provide a source of metal atoms which, during forming, mix with the a-Si:H to produce a new material which exhibits switching. In this chapter a series of experiments are described that set out to clarify the role of the contact by investigating the forming and switching characteristics of devices with contacts made not of metal but of silicon.

8.1. Experimental structures

Three alternative device structures have been considered, all of which have contacts to the a-Si:H layer made of highly conductive Si. The first of these is shown in fig.8.1. As can be seen, contacts to the n^+ a-Si:H layer are made through the crystalline Si substrate at the bottom and via the layer of micro-crystalline Si at the top. Both the crystalline and micro-crystalline Si is n-type and doped to a high conductivity to minimise contact resistances. External connections to the devices are made by placing probes directly onto the substrate and the micro-crystalline layer. Devices of this type will be refered to as 'all-Si'devices.

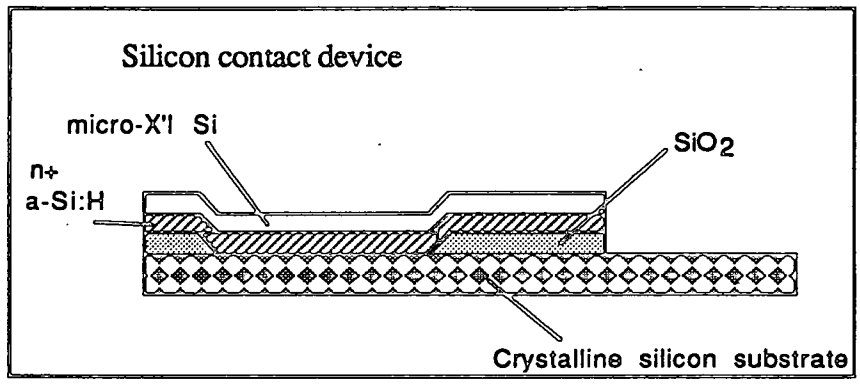

Fig.8.1 A 10micron diameter pore structure with a crystalline Si bottom contact and a microcrystalline Si top contact.

The second structure, shown in fig.8.2, is identical to the all-Si device except that there is a metal overlay on parts of the top micro-crystalline contact and the substrate. The metal does not, however, cover the pore area of the device and for this reason these devices will be refered to as 'uncovered' devices.

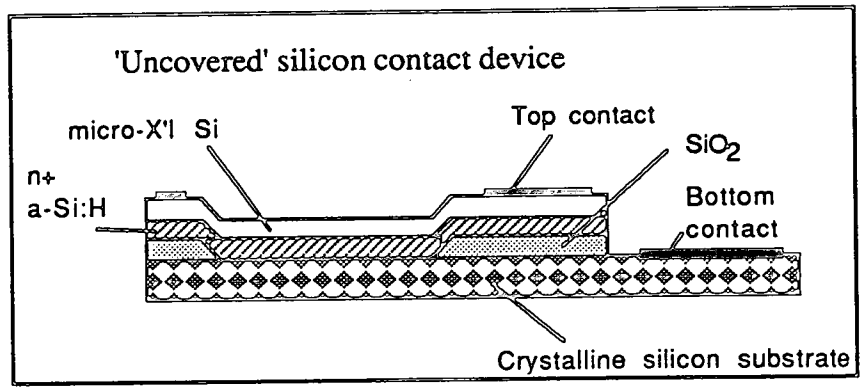

Fig.8.2 An 'uncovered' silicon contact device with a 10μm diameter pore. The metal contacts do not extend over the pore area.

The final device structure is shown in fig.8.3. In this, the 'covered' device, the metal overlays are identical to those in the uncovered device except that at the contact the metal extends over the pore area.

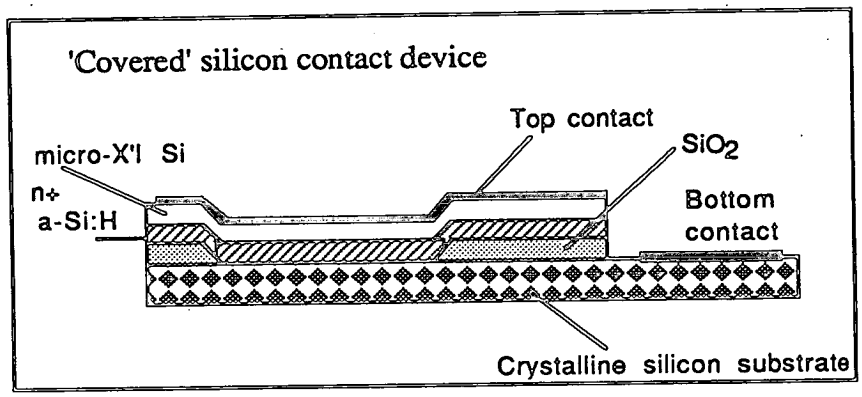

Fig.8.3 A 'covered' silicon contact device with a 10μm diameter pore. The top metal contact in these devices does extend over the pore.

The substrates used were p-type <111> crystalline silicon with an n-type implant at the surface to 12Ω/□. The thermal oxide was 350nm thick. The n^+-type amorphous and micro-crystalline layers were grown in a continual process using a phosphine concentration of 1000vppm. The metallisation layer was either Al (thermally evaporated, thickness 50nm) or NiCr (sputtered, thickness 300nm). For the purposes of future reference the devices are named as follows: the type of metal used is followed by the word 'uncovered' or 'covered', e.g. Al-uncovered.

If in normal a-Si:H memories the contacts serve no greater purpose than to act as electrical connections to the a-Si:H, then forming and switching should be seen in these three new device types provided the Si contacts make sufficiently low resistance substitutes for their metal conterparts. If, however, the metal contact plays a more involved part it might be expected that there would be differences between the performance of

the silicon contact devices of figs.8.1,8.2 and 8.3 and the conventional metal-a-Si:H-metal devices. By including the covered and uncovered design variations it is possible, by comparing the I-V characteristics of the three new device types, to establish some measure of the additional resistance introduced by replacing the metal contacts with silicon ones.

8.2. Experimental method

Attempts were made to form each of the sample types described above. The forming circuit of fig.5.2 § 5.3, was used. If a device was found to form successfully its switching properties were investigated in the usual way.

8.3. Results

The I-V characteristics of the unformed devices are shown in fig.8.4. The difference between the I-V characteristics of the uncovered and the covered devices, as shown by fig.8.5, was small over this voltage range indicating that the micro-crystalline layer was acting as a good substitute contact. The origins of the discontinuous changes in the resistance seen in all devices between 0.25V and 0.75V when the top contact was positively biased are not understood.

Table 8.1 summarises the forming and switching behaviour of the various types of devices.

The current oscillations mentioned for the Al-uncovered devices are shown in fig.8.6. These were attained by applying a voltage pulse of constant magnitude around 6-9V to the formed devices. Investigations showed that the frequency and magnitude of the oscillations depended on the resistive and reactive elements in the external circuit. This type of behaviour has been observed in the past in situations where a negative differential resistance (NDR) element is present somewhere in the circuit; the theoretical analysis of these effects is fairly well understood and the interested reader is

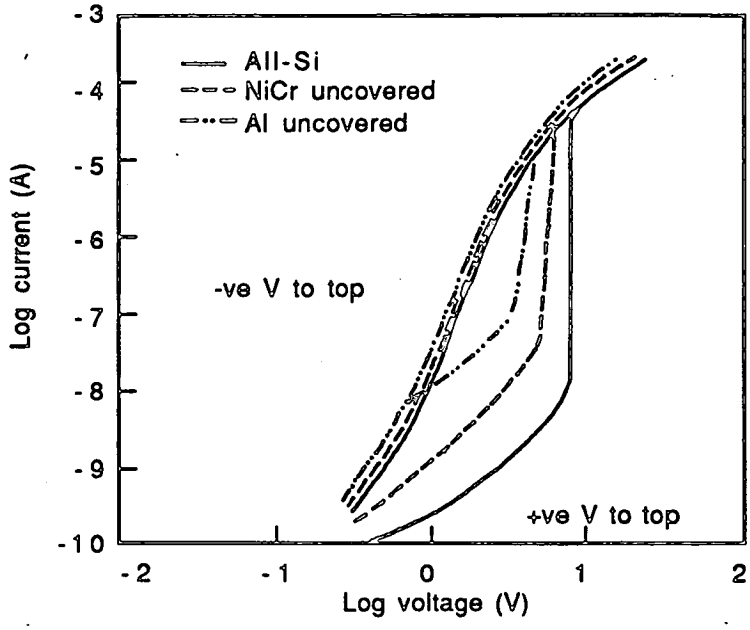

Fig.8.4 Current - voltage characteristics of 10micron diameter pore structures with a n+ a-Si:H layer a crystalline Si bottom contact and a microcrystalline top contact. The three sets of curves refer to variations on this general device type the details of which are described in the text.

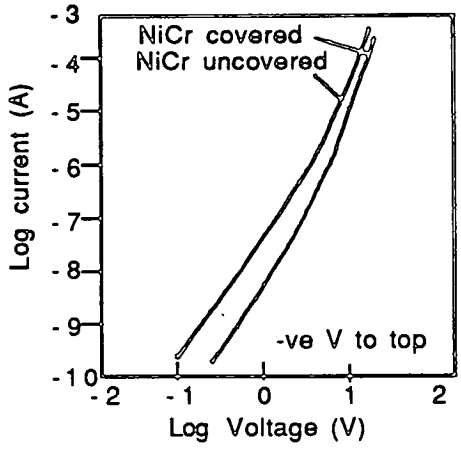

Fig.8.5 A comparison of the I-V characteristics of NiCr 'covered' and 'uncovered' devices. The similarity of the two curves suggests that the microcrystalline Si layer is not introducing a significant additional resistance as compared to the devices with metal overlays.

referred to the literature[1] for further details . It has been known for a long time that electrically formed Al-SiO-Al devices can give rise to N-type NDR [2] and it is commonly speculated that in these structures forming causes Al to diffuse into the bulk of

Device type	Forming		Comments	Switching
	Voltage	Current		
Aluminium uncovered	21V	2.5mA	Damage to the metal at the pore edge	Oscillations
Aluminium covered	15V	1.3mA	Damage to the metal at the pore centre	No
NiCr uncovered	30V	5.2mA	Filament grows horizontally	Slight
NiCr covered	14V	11mA	No damage seen	Slight
All Si	–	–	100V and 10mA formed only 2 out of 14 devices	None

Table 8.1 This summarises the results of the attempts to form and switch the devices with crystalline silicon bottom contacts and microcrystalline top contacts.

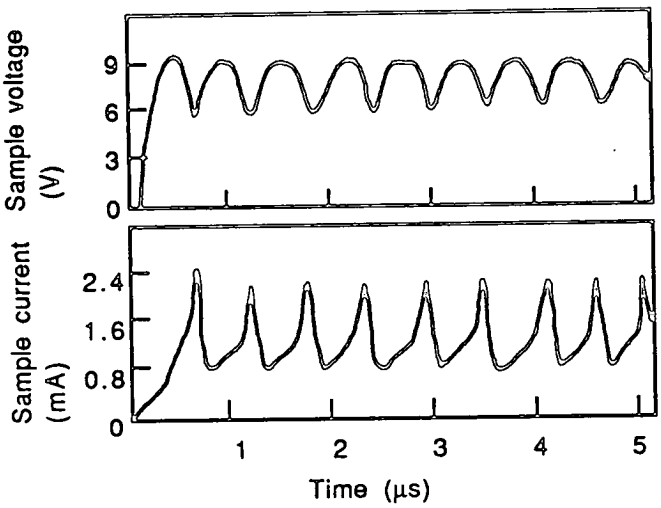

Fig.8.6 Oscillations in the sample voltage and current observed in formed Al uncovered devices i.e. pore structures with a crystalline silicon bottom contact, a microcrystalline top contact and an Al contact that does not cover the pore area.

the dielectric. Alternaitvely Al is known to migrate into Si under high field strengths to form spikes or filaments.[3,4] These filaments may in turn, as is common in filamentary conduction, give rise to S-type NDR. The origin of the negative differential resistance element in our case could, therefore, lie with the formation of an aluminium filament, possibly through the oxide, but as the surface damage to the aluminium is

always found at the point where the Al comes closest to the edge of the pore it seems likely that the Al is migrating downwards through the a-Si:H layer in the pore area.

The filament mentioned under the NiCr uncovered entry is shown in the electron micrograph of fig.8.7 and as can be seen it crosses the micro-crystalline silicon from the edge of the NiCr to the edge of the pore.

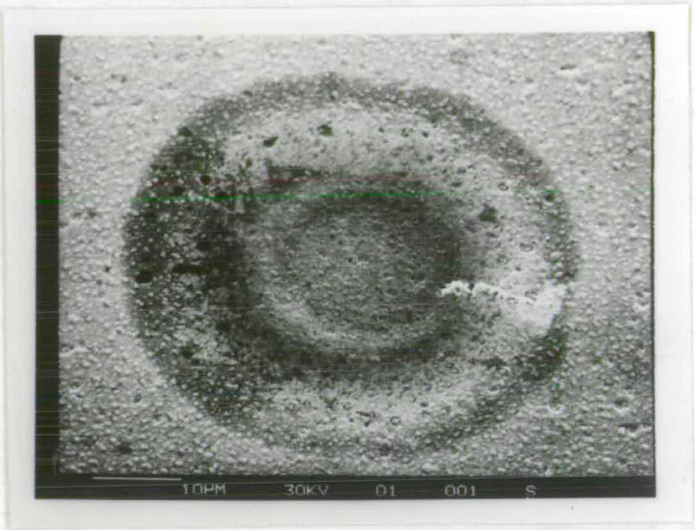

Fig.8.7 Electron-micrograph of a filament formed across the surface of the μ-crystalline top contact of a μ-X'l - a-Si:H - X'/ device.

Optically the filament appeared to be the same colour as the NiCr suggesting the metal had migrated across the surface. X-ray microprobe analysis, however, did not show a Ni or Cr signal for the filament but it is possible that the volume of the filament was too small to be detected by our equipment. The electron micrograph shows the filament to be a light region implying the material is charging up , i.e. is more insulating than the surrounding micro-crystalline Si. This might cast doubt over the suggestion that the filament contains NiCr as a Si/NiCr mixture would likely be more conductive. A report by Ishihara,5 however,which describes an investigation of the interaction between n-type a-Si:H and metal contacts at elevated temperatures, includes electron

micrographs of samples where metal has migrated across the surface of the a-Si:H giving rise to surface damage which appears light coloured in the same way to the features in fig.8.7. In conclusion it appears likely that the filament contains NiCr.

The All-Si devices showed virtually no tendency to form even though large voltages and currents were applied. Attempts to form them were also performed at elevated temperatures of up to 100°C but with no effect despite the increase in current.

8.4. Discussion

The first general observation to be made from these results is that the devices that include metal will form whilst the All-Si samples that contain no metal at all will not. The observation of damage to the metal in both covered and uncovered Al and NiCr devices and the voltage level at which forming takes place strongly suggests similar processes are occurring in these samples as occur in the conventional metal-a-Si:H-metal pore devices, namely, forming involves metal migration and filamentation. This is not especially surprising in the covered structure because of its close resemblance to the conventional device structure. In the uncovered Al and NiCr devices, however, the specific intention was to exclude the metal from any involvement in the forming process by keeping it apart from the active area of the device but this appears not to have been realised because of the apparent ease with which migration of the metal takes place. The filament of fig.8.7, which crosses at least 8μm of μ-crystalline Si, appears to be a particularly striking example of the ease with which metal migrates.

It is most interesting that the All-Si devices do not really form at all despite having experienced field strengths and current levels in excess of those used on the metallised devices. This strongly suggests that forming is not a process initiated by the a-Si:H itself by , for example, dielectric breakdown or internal heating, rather it is the readiness of the metal to migrate into the Si that initiates the process.

In addition to this, the absence of any switching in the All-Si devices suggests that forming is necessary to establish switching and as-prepared a-Si:H does not possess the required properties to switch.

8.5. Summary

Devices have been made in which the contacts to an n+ a-Si:H layer have been made of crystalline and micro-crystalline silicon. It has been found that in the absence of metal close to the pore area of the device the forming process does not take place. Furthermore there is no observation of switching in the unformed a-Si:H layer. Where metal is present in the device, even though it is away from the pore area, forming does take place. The presence of metal, therefore, seems to be essential for forming and it appears that during forming migration of the metal takes place giving rise to a metal rich filament which accounts for the permanent decrease in the resistance of the device.

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Chapter 9

Modelling temperature changes in the filament

9. Introduction

The majority of accounts found in the literature that try to explain memory switching in thin films make use of thermal switching mechanisms (see §2.4.2). This is particularly true when conduction in the device is filamentary as in these cases the high current densities in the filament during a switching pulse can give rise to temperature increases sufficient to melt the filament material. Despite the fact that the a-Si:H memory device possess a filament, no direct experimental evidence has been found for any temperature increases either during forming or switching. Partly for this reason the paper regarding these devices published in 1985 [1] largely dismissed thermal mechanisms for both forming and switching in their a-Si:H devices. It was also pointed out that the switching energy for the a-Si:H device of $<10^{-8}J$ was probably too small to cause temperature increases sufficient to justify considering a thermal mechanism. The measurement of the temperature changes in the filament is, however, exceedingly difficult both because of its small size and the short length of the voltage pulses used to operate the device. The 1985 paper based its conclusions about the temperature increases on visual observations made with thermochromatic liquid crystalls which were intended to highlight hot spots on the surface of the device. It is arguable, however, that this method is unlikely to give a realistic picture of the temperatures in the device, not least because any hot spot that does exist would last for, at the most, tens of μsec, which is too short for the human eye to register.

In an attempt to establish with more certainty the internal temperature increases in the filament I have carried out a numerical simulation of the heat generation and dissipation in the device. Contrary to the conclusions of the 1985 paper the results from this model suggest that during forming, and possibly during switching , temperature increases sufficient to cause structural alterations to the a-Si:H such as dehydrogenation and crystallisation, would occur.

The remaining sections of this chapter describe the model I have used to calculate the temperature increases, the results from these simulations and finally the possible meaning of these results in terms of forming and switching processes.

9.1. Modelling the temperature increases in the device

The model device , shown schematically in fig.9.1, is a block of electrically resistive material through which a filament of electrically conductive material passes.

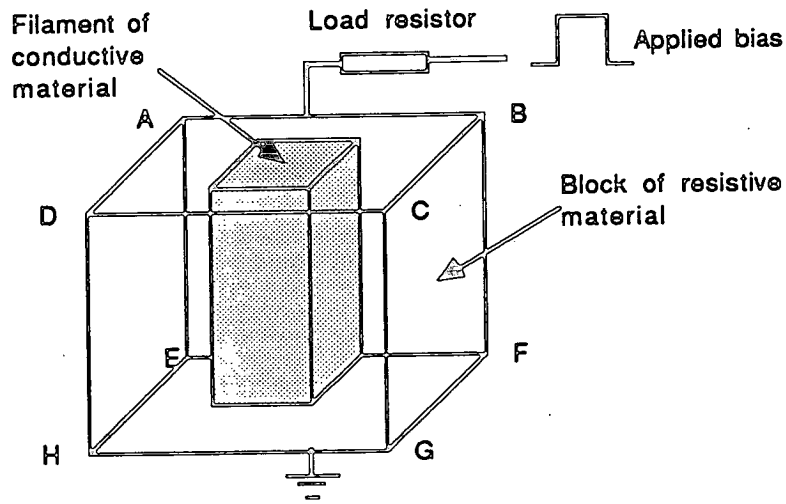


Fig.9.1 Schematic representation of the block of material used to represent the switching device. Surfaces ABCD and EFGH are the "metal" electrode surfaces through which all current enters and leaves.

The thickness of this block is varied between 1μm and 0.3μm and the dimensions of the sides between 1μm and 1.4μm. The filament can have any cross-section but always passes through the whole length of the device. A voltage is applied across the series combination of the device and the load resistor, and from calculations of the Joule heating caused by the current in the device and the heat loss across the external surfaces, the internal temperature increases are found. By including the load resistor it is possible to account for changes in the voltage across the device that result when the

device warms up and its resistance falls i.e. load-line effects.

9.1.1. Choosing the electrical resistivity of the model material

Deciding on a value for the resistivity of the model filament material requires some thought. It was pointed out earlier in §6.11 that the d.c. I-V characteristics of the memory states tend to converge at voltages similar to those used to switch the device. This means that at the switching voltage of 2-3V the resistances of devices in both the On and Off states are very close to each other. Observations of the device resistance during a switching pulse (i.e. no longer under d.c. but pulsed conditions of applied bias) shows that the resistance of the On and Off states are again roughly equal. This resistance lies between 2kΩ and 10kΩ. As both On and Off states have the same resistance at the switching voltage the heat dissipation in both will be much the same. For the purposes of calculating the heat generated in the devices we need not, therefore, distinguish between On and Off states. The resistivity of the filament material in the model device has been calculated by matching the overall resistance of the model filament to a value of 5kΩ which is a typical value for the device resistance during switching. The bulk resistivity has been taken to be that of p^+ a-Si:H i.e. $10^3 \Omega cm$.

9.1.2. Temperature coefficient of resistance

The resistivity of the filament material has been taken to have a linear dependence on temperature of the form $\rho = \rho_o(1-\alpha T)$ where the value of the TCR, α, has been taken to be $10^{-3}/K$, a value that is based on experimental observations made on real devices in the On state (e.g. see §7.4).

9.1.3. Electrical boundary conditions

The current enters at the top surface of the device and leaves at the bottom; the

four sides are regarded as perfect electrical insulators.

9.1.4. Thermal conductivity

The room temperature thermal conductivity of a-Si is 2W/m K^2 but at elevated temperatures it is expected that this value will increase. In the absence of data on a-Si I have used results for the temperature dependence of the thermal conductivity of another amorphous material, fused silica, which shows an increase of thermal conductivity of 30% in the temperature range 0°C to 400°C, to set the value for a-Si:H at 2.7W/m K.

9.1.5. Specific heat

The specific heat of the filament and the bulk has been taken to be identical, independent of temperature and equal to 700J/kg K.

9.1.6. Thermal boundary conditions

The thermal boundary conditions are: (1) The four vertical side are regarded as perfect heat sinks and maintained, for convenience, at 0 degrees. (2) Heat-loss from the top surface, (ABCD), is assumed to be negligible compared to that lost by conduction through the other surfaces. This surface , therefore, is regarded as being perfectly thermally insulating. Heat lost by radiation from the top surface will be many times less than the heat dissipated by conduction through the device and can therefore be ignored. Rather more heat may be lost by lateral conduction along the metal electrode. Detailed calculations show that for our devices, which are about 100 times wider than they are thick and which have metal electrodes thinner than than 0.1μm, the loss of heat through the top electrode is small.[3] (3)The bottom surface (EFGH) is alternately regarded as a perfect heat sink and a perfect thermal insulator. This apparently paradoxical arrangement allows an upper and lower limit of the temperature increases in

the device to be found but avoids the complication of accurately accounting for the conduction of heat away from the device through the glass substrate.

9.2. Using finite elements analysis

To translate the physical description of the device in to a set of workable mathematical equations, finite element analysis has been used. This numerical process is widely used and its implementation here is routine so no details of this aspect of the work are given.[4,5,6] Suffice it to say the block of material of fig.9.1 is subdivided into many smaller subvolumes, as illustrated schematically in fig.9.2a. The material of each subvolume is then taken as being lumped at a point, or 'node', at the centre of the subvolume, see fig.9.2b. The flow of heat and current are then considered as taking place along lines connecting each node with its neighbours, these lines being attributed with electrical or thermal resistances equivalent to the volume of material they represent, as shown in fig.9.2c. For this particular model 9000 nodes have been used, arranged on a cubic lattice.

The modelling programmes were written in C; a simplified flow diagram of the program is shown in appendix II.

9.3. Sources of inaccuracy in the model

Once the parameters and boundary conditions of the model have been set the numerical calculations are performed to an accuracy better than 1%. Two methods have been used to check the self consistency of the model. The first is to ensure that as time tends to infinity the internal temperature values reach stable values. The second is to sum all the heat generated within the device at any instant and compare it with a sum of all the heat leaving the device by conduction across the external surfaces. At all times whilst the bias is applied (Heat in) $\geq$ (Heat out) and if a steady state is reached during the voltage pulse (Heat in) = (Heat out).

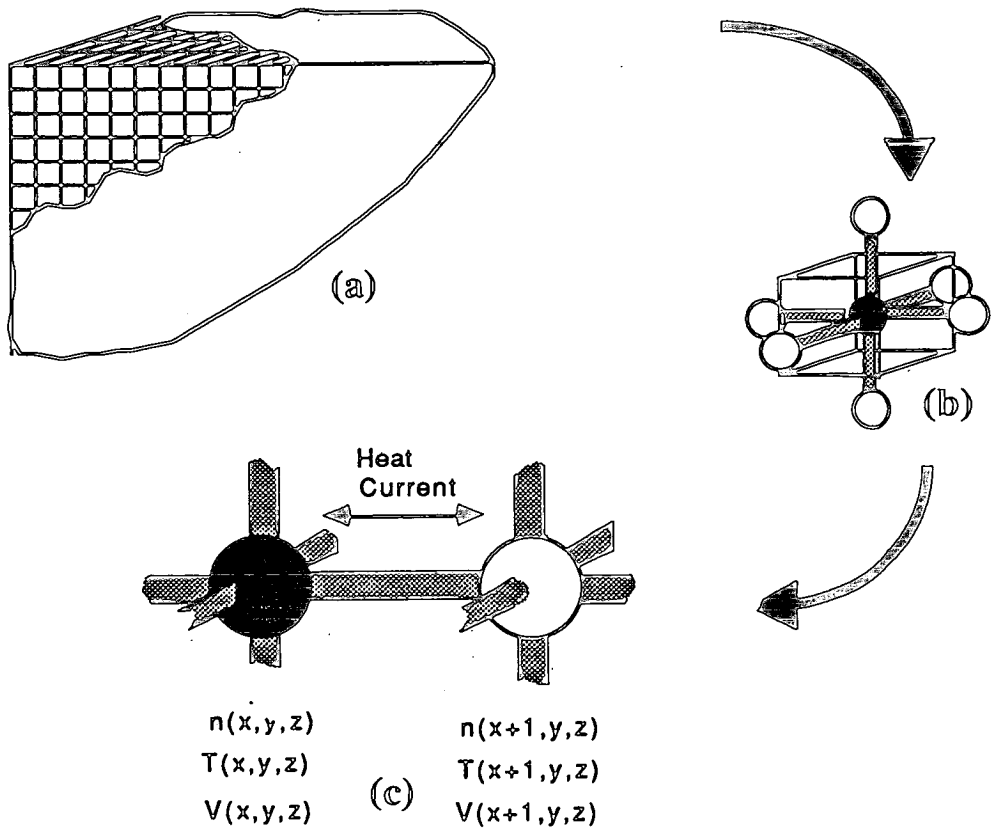


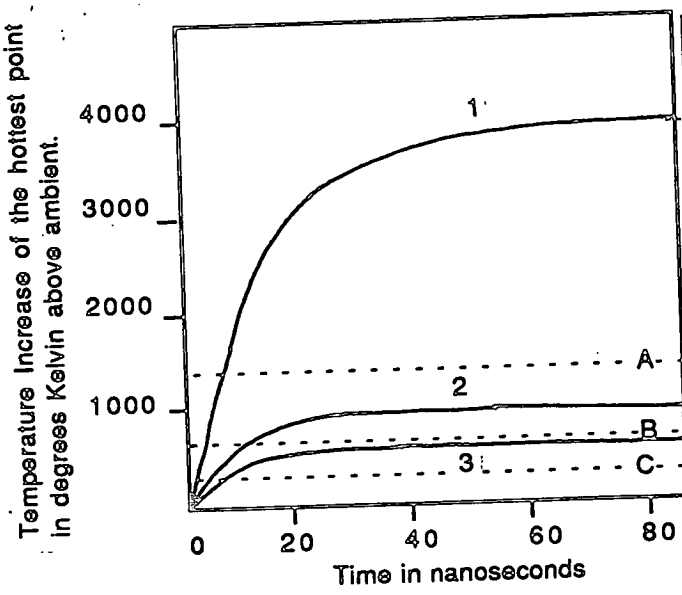
Fig.9.2 A schematic representation of the use of finite element analysis to model the properties of a body. Part of the block of material used to represent the a-Si:H is shown in part at the top (a). This is subdivided into thousands of smaller blocks. These in turn are replaced by a mesh of nodes and interconnecting rods (b). Each node is uniquely labelled , n(x,y,z) and its temperature T(x,y,z) and its electrical potential V(x,y,z) through out the simulation are recorded (c). The flow of heat and curent between nodes is calculated using the finite difference method.

The largest source of error will lie with the choice of the initial conditions. The difficulty in choosing the correct boundary conditions for the heat loss at the bottom contact is certainly one of the major sources of uncertainty and, as will be shown in the results section, can give rise to a variation in the results of 80%. The other principle area of uncertainty is the dimensions of the filament. From experimental observations it is possible to gain an upper limit on the filament diameter of 0.5μm [1] but it is entirely possible that filaments could be much smaller than this. For this reason a

number of filament sizes have been modelled. Furthermore nothing is known about how the cross section of the filament changes along its length; in the absence of this information it is assumed that the cross section is the same everywhere along the filament. This will give a conservative estimate of the temperature increases as it means the heat is dissipated in the largest volume of material Overall it would appear that this model is reliable only to within a factor ten.

9.4. Results

The results from the simulations are summarised in figs. 9.3 to 9.8. Fig.9.3 shows the temperature increase in degrees Kelvin above ambient for filaments of two different sizes under applied biases equivalent to those used during the forming of the device. The filament resistance has been taken to be 5kΩ , a value taken from experimental observations of the device resistance during the forming of both p-n-i and p+ devices. The temperature scale shows the temperature of the hottest point in the filament which, as the bottom contact has in this case been taken to be a perfect heat sink, is found immediately under the top contact in the centre of the filament. As can be seen the larger filament (curves 2 and 3) attains a lower final temperature than the smaller filament (curve 1). Both, however, have reached, or are close to, their steady state within 80ns. The size of the temperature increases are discussed in the next section. Fig.s 9.4 to 9.6 show the temperature increases expected during switching operations where the applied bias ranges between 2 and 5V. Again the filament has been taken to have a resistance of 5kΩ. These temperature values are substantially lower than those of fig.9.3 for the obvious reason that the current flowing thorough the filament is less. The graph of fig.9.7 shows the effect on the calculated temperature increases of the thermal properties of the bottom contact. As can be seen, by changing this contact from being a perfect heat sink to a perfect thermal insulator the calculated temperature increases by about 80%. The final result, shown in fig.9.8, shows the temperature as a function of position on a vertical plane cut through the middle of the filament.



Curve no	1	2	3
Filament area μm^2	0.3^2	1^2	1^2
Filament length, μm	0.3	1	1
Applied bias, V.	10	15	10

Fig.9.3 The predicted temperature increases in the filament occuring during forming for three different filament geometries. The three lines have been marked on assuming an ambient temperature of 30C and are; line A is the melting point of Si,1414C, line B marks the onset of crystallisation at 640C and line C marks the onset of dehydrogenation at 300C.

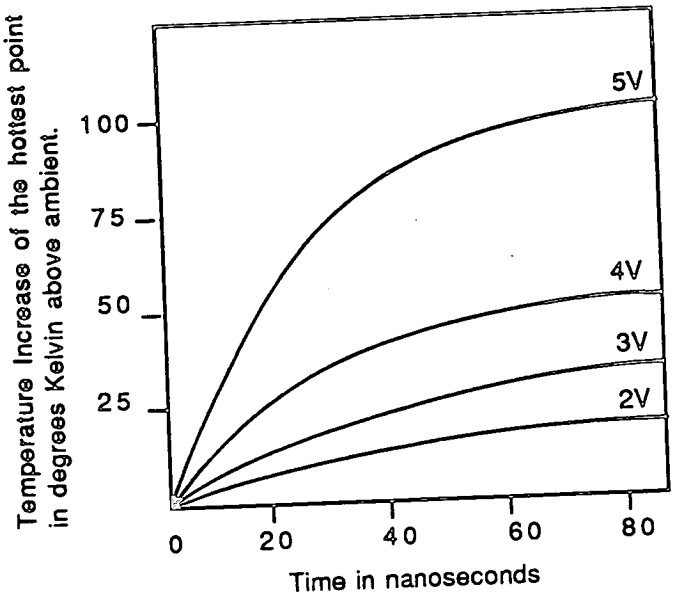


Fig.9.4 Temperature changes expected during switching in a LARGE filament, $1\mu m^2$ in a $1\mu m$ thick sample. The filament resistance is $5k\Omega$. The applied bias is marked on the curves.

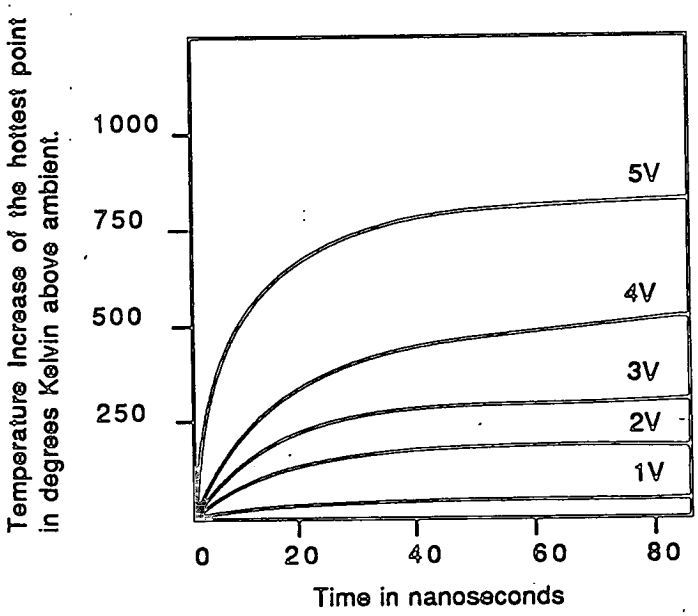


Fig.9.5 Temperature changes expected during switching in a MEDIUM filament, 0.3μm in a 0.3μm thick sample. The filament resistance is 5kΩ. The applied biases are marked on the curves.

9.5. Discussion

The model described here deals specifically with the estimation of temperature increases in filaments. Its application to the forming process is only valid, therefore, once we assume a filament has been created in the device. (The model does not tell us anything about the temperature changes in the device leading up to the filament's formation and can not therefore predict whether the filament is initiated by a localised increase in temperature.) The schematic current trace of fig.9.9 shows that at time T_f during the forming of a p-n-i device there is a sudden increase in the device current. As the conductive filament is a known product of forming it seems reasonable to assume that the current jump in fig.9.9 corresponds to the onset of filamentary conduction. Once this has happened, and for whatever reasons, the current flowing throughout the remainder of the forming pulse will be concentrated along the filament. This situation can be modelled and thus an estimate of the temperatures occurring in

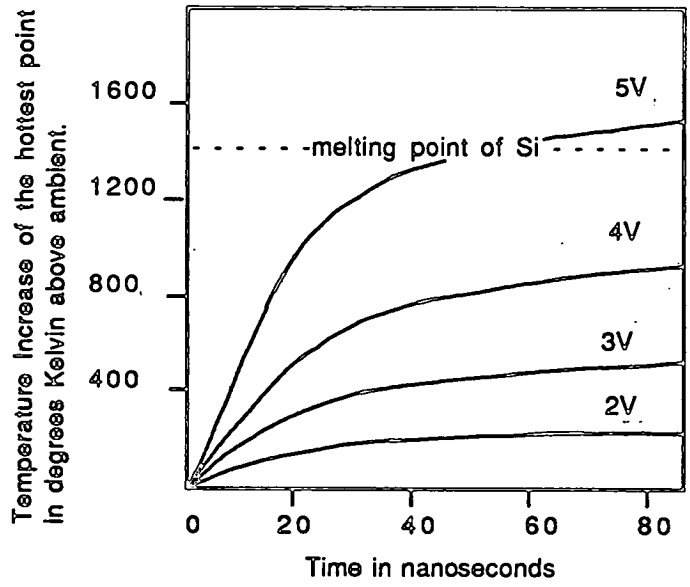


Fig.9.6 Temperature changes expected during switching in a SMALL filament, 0.15μm in a 0.3μm thick sample. The applied biases are marked on the curves. The filament resistance is 5kΩ. The melting point of silicon, 1414C, has been marked on assuming the ambient temperature is 30C.

the filament during forming can be arrived at. Forming pulses are typically 10 to 15V and at least 100ns long. Once the sudden current increase has taken place the device resistance at these biases is typically <5kΩ. The temperature increases occuring in the filament, as deduced by the model, depend strongly on the size of the filament and the thickness of the film. The data of fig.9.3 shows that for a filament cross-section of $1\mu m^2$ in a 1μm thick film the maximum temperature increase is likely to be 500K at an applied bias of 10V and 1125K at a bias of 15V. The data for the $(0.3)^2\mu m^2$ cross-section filament in a 0.3μm thick film, also shown in fig.9.3, shows that for this smaller filament the temperature increases are now thousands of degrees! Both of these sets of data have been calculated assuming the bottom contact is a perfect heat sink and so they may under estimate the actual temperature.

What does the data of fig.9.3 mean in terms of physical changes to the a-Si:H?. In §4.7 it was established that four distinct processes occur as a-Si:H is heated, namely,

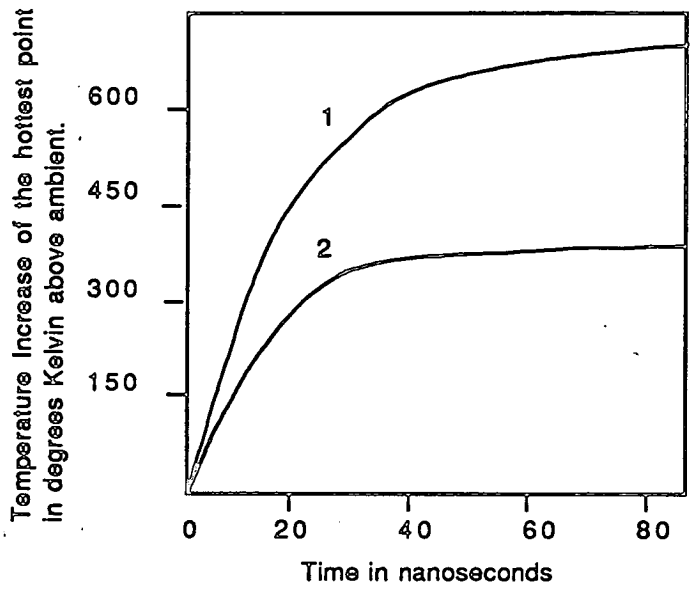


Fig.9.7 A demonstration of the effect on the expected temperature increases in the filament of the thermal properties of the bottom contact. Curve 1 is for a perfect heat sinking contact and curve 2 for a perfectly insulating contact.

defect annealing from 150°C to 450°C, dehydrogenation from 300°C to crystallisation, crystallisation from 640°C to 770°C and finally melting at 1414°C. For the large filament (curve 3 of fig.9.3) there is a sufficient increase in the filament temperature at a bias of 10V to initiate dehydrogenation. For the same filament at 15V (curve 2 of fig.9.3) the crystallisation temperature is exceeded. The temperature increases in the smaller filament (curve 1 of fig.9.3) exceed the melting point of Si even at 10V. It appears from the simulations, therefore, that the temperature increases occurring during the forming process are, at least in the hottest part of the filament, highly likely to cause some dehydrogenation and crystallisation of the a-Si:H and in films thinner than about 1μm it appears that a-Si:H would melt. The temperature map of the filament shown in fig.9.8 suggests that whilst the temperature close to the bottom contact and outwith the filament are considerably less than those elsewhere in the filament, the temperature increases described by fig.9.3 can be expected to prevail in a large part of

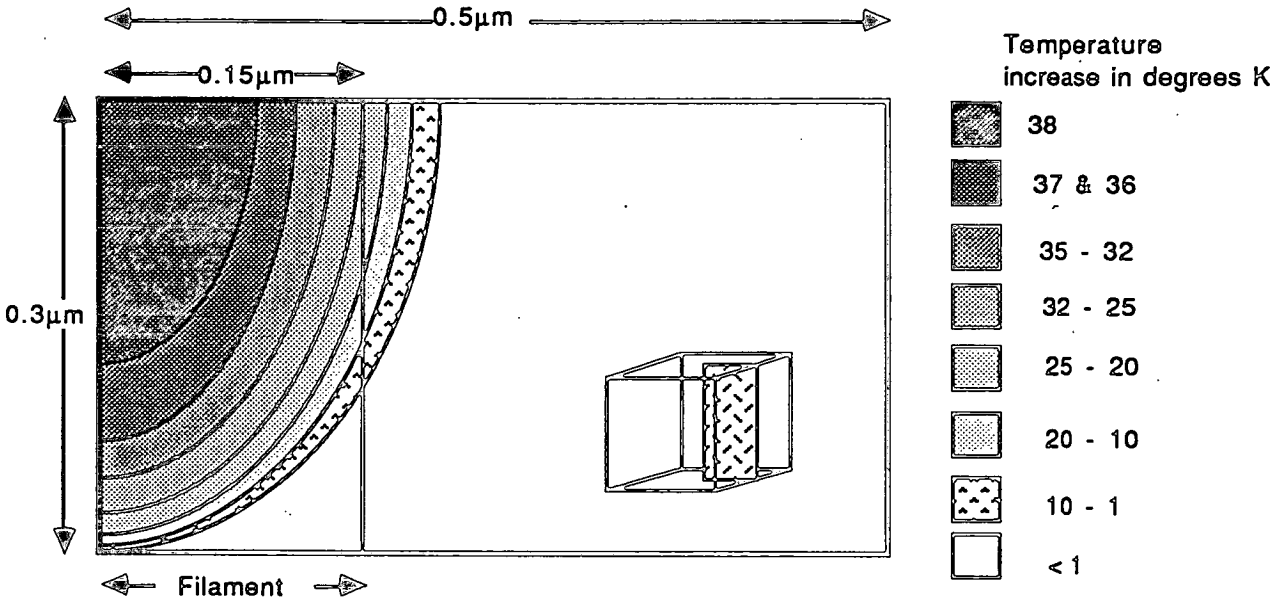


Fig.9.8 The spatial distribution of the temperature in a 0.3µm square filament penetrating 0.3µm thick sample with an applied bias of 1V. and a total filament resistance of 5kΩ. These values are after 10ns of the voltage pulse has elapsed. The inset shows the plane of the model device to which this data refers. The top contact is a perfect insulator and the bottom contact a perfect heat sink.

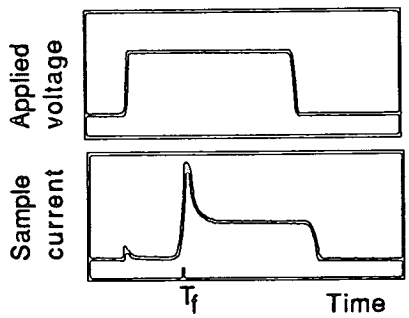


Fig.9.9 Typical current and voltage traces for the forming of a p-n-i sample. The transition to the high conducting state occurs at time Tf.

the upper half of the filament. The crystallisation and melting should, therefore, occur throughout a sizable fraction of the filament. If the Si melts it is probable that it will subsequently solidify in a microcrystalline form.

Considering now the temperature changes during the switching of the samples, one of the central questions to answer is whether the switching current will heat the

filament sufficiently to melt it? The voltages used to switch the devices range from 2V to 5V and their duration can be as short as 10ns. From the data presented here it appears that only the narrowest filament in the 0.3μm thick film (fig.9.6) exceeds the melting point of Si within 10ns and then only at biases of about 5V. Applying pulses for longer than 10ns would not greatly change this picture as, according to the model, the filament reaches about 60% of its steady state temperature within 10ns. Although melting of the filament in most cases is unlikely it is clear form fig.s 9.4 to 9.6, that temperatures of a few hundreds of degrees can be attained. These elevated temperatures may have an important part to play in enhancing atomic movement within the filament; hydrogen, for example, starts to become mobile in a-Si:H at 360°C [7] and may do the same in the modified material of the filament. The movement of ionic species under the influence of the electric field will also be encouraged by the temperature increases. This could include dopant ions from the a-Si:H and metal ions that have come from the electrodes and mixed with the thin film.

9.6. Summary

When attempting to identify mechanisms for both the forming and switching processes in the a-Si:H memory it is useful to have an estimate of the temperature increases arising in the filament as a result of Joule heating. Knowing this enables some judgement to be made about whether temperature induced structural alterations to the a-Si:H, such as dehydrogenation, crystallisation and melting, are likely to take place. In the absence of a satisfactory experimental means of measuring these filament temperatures I have made use of a series of numerical simulations of the conditions of heat generation and dissipation in the filament. The means by which these simulations have been performed has been described in this chapter. The model provides information on the temperature of the hypothetical filament as a function of time for a prescribed filament size, filament resistance and applied bias.

A number of interesting conclusions have been drawn from this work. (1). The simulations suggest that during forming the temperature of the filament almost certainly exceeds the dehydrogenation and crystallisation temperatures of the a-Si:H and may well exceed the melting point of Si. If it does melt it is probable that it will finally solidify in a microcrystalline form and so overall it appears highly likely that at least part of the filament is made of crystallised Si. (2). The filament temperatures expected during switching are substantially lower than those associated with forming. Temperature increases of a few hundreds of degrees seem to be feasible within 10-20ns. The melting of the filament appears to be unlikely although the estimates of the filament temperature are sufficiently close to the melting point of Si i.e. within a factor of less than 10, that it is hard to rule it out altogether.

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Chapter 10

Final discussion

10. Introduction

This final chapter draws together many of the results presented in chapters 6, 7, 8 and 9, and some by other workers, to discuss the overall picture that has emerged of the forming process and the nature of the filament. The implications these results have for speculations of switching mechanisms is also discussed.

10.1. Forming and the filament

One of the more enlightening discoveries in the course of the research into the a-Si:H memory has been the observation of switching in single layers of homogenous a-Si:H, such as p^+ and n^+-type. The structural simplicity of these devices compared to the earlier p-n-i devices has made a number of areas of the work much clearer, amongst them an understanding of the conduction processes in the pre-formed state and certain aspects of the forming process. In single layer p^+ samples, which have been the focus of the work reported in chapter 6, it seems reasonably certain that the generally low level of conductance of unformed samples arises from contact resistances which can probably be accounted for by Schottky barriers at the metal to a-Si:H interfaces but may, in addition, be due to oxide layers at the metal electrodes. Capacitance measurements suggest that the thickness of the Schottky barriers in these devices is of the order of 4 - 5nm at zero bias.

Forming p^+ samples causes a reduction in the device resistance of at least two orders of magnitude indicating that a drastic modification of the contact resistances has taken place. The observation of a conductive filament in the formed samples has lead to the suggestion that the increase in conductance is in part due to the bridging of the contact resistance by the conductive filament. As the I-V characteristics of the formed devices are largely symmetrical about zero volts, it is reasonable to conclude that both top and bottom contact resistances have been bridged. If the barrier widths at the con-

tacts are of the order of 4-5nm then the filament penetrating them must at least be of a comparable length.

In more general terms the fact that forming takes place at all in p^+ samples, or any other single layer structure such as n^+ or i-type, reveals an important result, namely that forming in a-Si:H memory devices is not a process that requires the presence of an a-Si:H to a-Si:H heterojunction, such as the p-n or n-i junction. Models that adopt charge trapping at these interfaces as a mechanism for increased sample conductance, such as those discussed by LeComber et al.[1] (regarding p-n-i devices), would not, therefore, seem to provide a complete picture of forming if indeed they are relevant at all. What is perhaps of most interest is that *despite* the differences between the various structures investigated there is a very large degree of similarity in their forming characteristics. In other words, the forming process does not appear to be particularly sensitive to the detailed structure of the a-Si:H layer.

A possible reason for this insensitivity has come from the experiments reported in chapter 8 that investigated the forming process in n^+ a-Si:H single layer samples with Si contacts. It was found that samples made entirely out of Si (with crystalline silicon as the bottom contact, micro-crystalline silicon as the top contact and no metal present anywhere in the device) did not form even under extreme biases of around 100V. Samples incorporating metal in the vicinity of the active area of the device (overlaying the top micro-crystalline contact) did form in the usual way however. It appears from this that subjecting a piece of a-Si to a typical forming voltage or current is not in itself sufficient to cause forming to take place. Forming is not, therefore, a process wholely associable with the properties of a-Si:H. Rather, it appears that the contact metal plays the central role in initiating forming, or more specifically it is the injection of metal into the a-Si:H layer to form the beginnings of a conductive filament that initiates forming. This suggestion is perhaps all the more plausible when viewed

in the light of the many reports of metal migration or "spiking" at metal:semiconductor interfaces subjected to conditions of high field and current.[2,3,4]

Further insight into the forming process has come from the low temperature conductivity measurements reported in chapter 7. These go some way toward substantiating the idea that forming causes the introduction of metal into the a-Si:H layer - the observation of superconductivity in samples with Al top electrodes indicates the presence of Al-Si mixtures and peaks in the zero bias resistance of samples with Cr, Au and Fe electrodes indicates conduction by activated tunnelling between metal islands embedded in the a-Si:H. In addition to providing information about the presence of metal in the a-Si:H the low temperature measurements have made it clear that, in the On-state at least, there must exist between the top and bottom contacts a continuous link of modified material that has a conductivity considerably higher and a temperature coefficient of resistance considerably lower than that possible for any type of unaltered a-Si:H. This is the only way the value of the sample conductance observed at low temperatures can be accounted for.

The results from the modelling of Joule heating in the device during the forming pulse have indicated that once the device resistance has undergone the transition from its virgin value to its post-formed value and if, as appears likely, this transition is associated with the onset of current filamentation, there is scope for temperature increases within the filament of at least hundreds of degrees possibly even exceeding 1000 degrees. This suggests that dehydrogenation and crystallisation are both probable in the filament material and melting is possible.

To summarise, the following useful points on forming and the filament have come from the work described in this thesis:

(i) Forming occurs in both homogeneous and heterogeneous samples. This indicates that forming is not a process that requires the presence of an a-Si:H to a-Si:H

heterojunction.

(ii) The initiation of forming appears to be related to the presence of metal electrodes suggesting that electromigration of metal may be a crucial early stage in the process.

(iii) Measurement of conductances and temperature coefficients of resistance (TCR's) around 4.2K strongly suggest that in low resistance samples at least, the filament extends continuously through the device. By estimating the filament dimensions an average resistivity of $10^{-1}\Omega cm$ for the filament material is arrived at and from experiment the TCR of this material is found to be between 10^{-3} to$10^{-4}/K$. These results suggest that the filament is either heavily doped crystalline Si or a metal:Si mixture.

(iv) Low temperature measurements show an anomalous zero bias resistance peak in samples with top contacts made of Cr, Fe and Au which is indicative of conduction by activated tunnelling possibly between small metal particles embedded in Si. At 4.2K devices with Al top contacts show evidence of superconductivity which can be related to the creation of an Al:Si mixture. In summmary, all samples so far looked at show some evidence for the inclusion of metal into the Si layer.

10.2. Switching mechanisms

10.2.1. Introduction

Before discussing switching mechanisms it is sensible to summarise what appear to be the most relevant observations of the switching. Drawing on work from this thesis and to a large extent on work from other workers the folllowing points arise:

(1) Switching is polarity dependent i.e. pulses of opposite voltage polarity are used to perform the Write and Erase operations.

(2) Switching speeds can be as fast as 10ns for both Erase and Write operations.

(3) The best devices can perform at least 10^6 operations before failure.

(4) The switching energy lies around 100pJ for both Erase and Write operations.

(5) Devices in a range of resistance states have been monitored at room temperature for periods of years with no signs of non-volatility.

(6) Devices retain their memory states when exposed to 5Mrad of γ radiation.

(7) Samples with homogenous layers (e.g. p^+,n^+) show similar switching characteristics (in terms of the polarity dependence, switching speed and switching voltages) to samples with heterogenous a-Si:H layers (e.g. p^+-n-i). The reliability of the switching does, however, appear to be related to the type of a-Si:H used although no clearly defined relationship has yet emerged.

(8) The use of different contact metals affects the switching characterisitics - Owen et al. pointed out the difference between the use of Al and transition metals [5] and more recently LeComber et al. reported subtler differences between Cr and V.[6]

(9) All samples have a conductive filament that appears to contain metal from contacts and the a-Si:H in the filament region may have undergone dehydrogenation and crystallisation.

(10) Simulations of the temperature increase in the filament during switching suggest that the filament is unlikely to melt although for reasons discussed in §9.6 this result is a little inconclusive.

10.2.2. Charge storage models

Electronic models for memory switching rely on the storage of charge to maintain a particular memory state. Adopting this type of approach to account for switching in a-Si:H devices outwardly appears rather attractive as it can accommodate a polarity dependence, the observed switching speed and the operational life-time of $>10^6$ cycles,

and would not necessarily be inconsistent with the presence of a filament. The difficulty with this approach lies, however, in identifying a trap in a-Si:H that has a release time comparable to the life-time of the memory. It is improbable that the tail or gap states of the a-Si:H could retain charge for long enough to account for the non-volatility of the devices. Metastable defects in a-Si:H, such as those reported by Staebler and Wronski [7] and others,[8] might offer more plusible trapping sites as they are often found to have sufficiently large release activation energies to persist at room temperature for indefinite periods of time. The use of any eletronic models, however, currently faces serious problems in accounting for insensitivity of the memory devices to prolonged exposure to high energy radiation. If charge were stored in the device it is expected that the radiation would cause its release and thus affect the resistance of at least some of the memory states. On the basis of present evidence, therefore, an electronic model seems unlikely.

10.2.3. Thermal models

The basic requirements of a purely thermal switching mechanism are that part of the device material melts during the switching operation and that this is accompanied by a quasi-permanent change in the phase or composition of part of the device material. As outlined in §2.5.2 such mechanisms are most often proposed when conduction is filamentary as it is in these cases that the current density is sufficient to cause the required Joule heating. Other relevant features characteristic of thermal mechanisms are; (a) effectively indefinite storage of memory states, (b) switching times that vary from a few ms to 10ns and, (c) operational life-times that are often greater than 10^6 cycles.

The a-Si:H memory certainly shows filamentary conduction and displays points (a)-(c). Furthermore, although earlier in point (9) above it was mentioned that the results of simulations did not suggest the melting point of Si is likely to be exceeded

during switching it should be remembered that, as discussed in §9.6, the predicted temperature increases are within one order of magnitude of the melting point of Si and the errors in the model may be of a similar magnitude. It is, therefore, not impossible that at least part of the filament could melt.

Despite all the evidence for a purely thermal model there is perhaps stronger evidence against it, the most prominent of which is the polarity dependence of the switching. As outlined in §2.5.2 in devices with a thermal switching mechanism the parameter that determines the final resistance of the memory is usually one of the following: the voltage pulse height, its width or the rise or fall time of the leading and trailing edges, but it is never just the direction of the current. In the a-Si:H device, however, it is possible to perform both Erase and Write operations with voltage pulses that are identical in every respect except for their polarity. Furthermore, as the Off-state I-V characteristics are non-linear, by 4-5V the Off-state conductance is commensurate with that of the On-state so the current passing through the device can also be the same for Write and Erase operations. In short a-Si:H devices can be successfully switched using pulses that are similar in both voltage and current level but of opposite polarity. There appears to be no simple reason, therfore, why the internal heating conditions should be different during Erase or Write operations and it is difficult to imagine what the mechanism might be. It may be possible, however, that the internal heating assists a field dependent process.

10.2.4. Alternative mechanisms

One process that may account for the polarity dependence of switching and the non-volatile nature of the memory states is that of electromigration. This occurs in conductors carrying high currents and manifests itself as a migration of the conductive material either with or against the direction of the current flow. The effect is usually observed at current densities in excess of $10^5 A/cm^2$ and is normally regarded as being a

rather slow process taking many hours to cause observable effects. Most studies of electromigration appear to have concerned themselves with metal tracks in integrated circuits where the migration of the metal can lead to the track's failure. In his discussion of electromigrations in Al tracks Sze[9] gives an equation describing the mean time to failure (MTF) of the track by the creation of voids,

$$MTF \propto J^{-2}\exp^{(\epsilon_E/kT)} \qquad (1)$$

where ϵ_E is an electromigration activation energy and J is the current density. This equation shows that the rate of electromigration, which is inversley proportional to the MTF, is proportional to J^2 and inversley proportional to the exponential of a migration activation energy. As electromigration takes place preferentially along low energy routes such as grain boundaries ϵ_E is generally less than the self-diffusion activation energy of the crystal; for polycrystalline Al Sze takes ϵ_E to be 0.5eV compared to 1.4eV for self diffusion in the bulk crystal.

During normal switching operations the current in the a-Si:H device is typically a few mA which, taking an upper limit for the filament diameter of 0.5μm, corresponds to a minimum current density in the filament of around $10^5 A/cm^2$. Bearing in mind the filament could be much smaller than this the current density might be closer to $10^6 A/cm^2$. At these current densities electromigration within the filament would appear to be quite possible. The origin of the switching mechanism may, therefore, lie with the reversible migration of material giving rise to a change in the filament resistance. What would appear to be clear is that if the switching occurs as rapidly as 10ns the electromigration distances are likely to be very small i.e. possibly only a few atomic spacings.

Identifying the migrating species is difficult. The filament comprises silicon, hydrogen, dopant ions (phosphorus or boron), and metal from the electrodes. Conceivably any of these could be the active species. The observation that the switching

characteristics are dependent on the type of metal used for the contacts might implicate the metal ions. It was shown earlier in chapter 7 that the inclusion of metal from the contacts into the filament is a probable means of accounting for the low resistance of the device particularly at low temperatures. The redistribution of this metal by electromigration could quite possibly cause large changes in the filament resistance. One mechanism by which this might happen has been outlined by Reynolds.[10] He points out that if, as shown in fig.10.1, the current in the filament is determined by tunnelling between two regions of highly conductive material such as metal rich Si, changes in the tunnelling distance by as little as 1-2nm can alter the tunnelling current by many orders of magnitude. The reversible 'opening' and 'closing' of such a gap by the electromigration of metal might then offer a suitably fast means of changing the device resistance by the 3 or 4 orders of magnitude that is observed. It is possible that the dependence of the switching characteristics on the electrode metal type could then be accounted for in terms of the different migration rates in Si of differet metal ions.

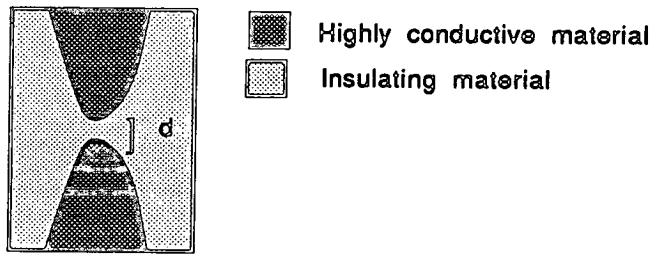

Fig.10.1 A schematic representation of a tunnelling gap of width d between two conductive 'fingers' in an insulating matrix. (After suggestions by Reynolds).

The electromigration of hydrogen could give rise to changes in the device conductance in a number of ways. LeComber et al. have already pointed out the possible significance of observations of changes in metal workfunctions at a-Si:H to metal interfaces caused by the incorporation of hydrogen into the metal. If conduction in the

filament were controlled by transport across metal:a-Si:H interfaces the reversible diffusion of hydrogen across these interfaces may cause substantial changes in the overall current level. This could be happening at the a-Si:H:electrode interfaces or within the filament at metal islands.

The hydrogen also plays a central role in determining the density of states, and therefore the conductivity, of the a-Si:H itself. It is perhaps possible that a field-activated re-ordering of the bonding between the Si and H is taking place. Hydrogen is also known to deactivate phosphorus acceptors in Si[11] and so there is the possibility, in n-type samples at least, that the effective doping level of the a-Si:H in the filament is being affected. The choice of hydrogen as the electomigratory species is a particularly attractive one because both the hydrogen molecule and the proton should be relatively mobile in the a-Si:H and perhaps offer the easiest means of accounting for the high switching speed.

Electromigration of the Si itself is also possible; a switching mechanism might involve the creation and closing of voids under a contact, for example.

10.3. Future work

To improve upon these rather loose speculations of switching mechanisms it is necessary to learn considerably more about the electromigration of hydrogen, dopants and metals in disordered Si. Perhaps the two most pertinent questions to be answered regarding electromigration and switching are, (1) can electromigration occur fast enough to account for the observed switching speed, and (2) under what conditions is it reversible? Having, as we do, some knowledge of the likely composition and structure of the filament material it should be possible to prepare similar material to that in the filament in bulk form. If switching can be achieved in bulk material then a range of structural and compositional analysis tools such as TEM and SIMS can be used to

study the effects of current densities of $10^5 A/cm^{-2}$ Maybe then some more concrete evidence for the switching mechanism will come to light.

Another avenue of investigation seemingly worth pursuing is that of preparing switching samples with planar structures. The advantage of a planar device over a sandwich devices is that the filament, and any structural changes occuring in the filament during switching, should be easier to observe from the surface with an electron microscope. From the observations of switching in sandwich structures it would appear that for good switching performance the a-Si:H film thickness should be greater than about 50nm but less than 1.5μm. Making a planar structure in the form of a gap cell should therefore have a gap spacing within this range, although the limitations of photolithography would probably restrict the gap cell thickness to greater than 1μm.

In addition to the two suggestions mentioned above to prepare new materials and device types two useful experiments could be carried out on existing devices; (1) the switching performance at very low temperatures i.e. less than 20K, should be investigated and (2) the effects of high energy radiation on the resistance of memory states of recent p^- samples should be looked at. Both of these experiments provide information about the switching mechanism. The first should establish with little doubt whether there is a necessary thermal component to the switching mechanism. The second should establish whether or not the switching mechanism in the p^+ samples involves charge storage. These two experiments should provide a reasonable footing on which to speculate further about the switching mechanism.

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Appendix 1

A technique for converting dynamic resistance, dV/dI, into static resistance, R.

Many low temperature investigations of the memory device made use of the measurement of dynamic resistance, dV/dI. As will be shown below, for a non-Ohmic conductor dV/dI is not always equatable to the static resistance of the device, R, and some numerical processing is required to obtain the latter from the former.

For a device with non-Ohmic I-V characteristics its resistance can be writen either as a function of current

$$R = R(I) \tag{1}$$

or as a function of applied voltage

$$R = R(V) \tag{2}$$

Using equ.(1) and Ohms law gives

$$V = IR(I) \tag{3}$$

Differentiating equ.(3) w.r.t current gives,

$$\frac{dV}{dI} = R(I) + \frac{IdR(I)}{dI} \tag{4}$$

As can be seen from equ.(4), dV/dI only equals $R(I)$ when the current is zero i.e. at zero bias.

In order to find R at any non-zero voltage or current the following manipulative sequence was carried out. The first step was to reciprocate dV/dI to give dI/dV. Integrating dI/dV over a particular voltage range (which was done numerically) then gives the current at that voltage i.e.

$$I = \int_{V=0}^{V=v} \frac{dI}{dV} dV \tag{5}$$

Knowing the current at a particular voltage enables the static resistance. R, to be found simply by using Ohms law.

Appendix 2

The flow diagram for the program used to simulate internal temperature increases in the memory device.

The flow diagram shows the basic features of the program previously discussed in chapter 9 that was used to simulate the temperature increase in the filament of memory devices during forming and switching. Further details of the model can be found in chapter 9.