Subthreshold Behaviour of Small Geometry MOSFETs

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Declaration

I declare that the contents of this thesis are my own work. Wherever another author has been quoted, this is stated and a reference is provided.

signed by

CAO, Xuezhou

Abstract

The subthreshold region becomes increasingly important in small geometry circuits as dimensions of MOSFETs continue to shrink in order to reduce cost and to obtain better performance. For short-channel or narrow-channel devices, their potential distribution becomes two-dimensional instead of one-dimensional as for a large device. Thus the one dimensional subthreshold model used for large devices is no longer accurate for small geometry devices. Two-dimensional models have to be developed. A two-dimensional analytical subthreshold and punchthrough model for short-channel MOSFETs with nonuniformly doped channel is presented. Analytical expressions for the subthreshold current and gate swing are given. Ion implantation has become a standard MOS process step to adjust threshold voltage and to prevent punchthrough. It has great impact on the subthreshold behaviour of MOSFETs. A detailed examination of how the channel profile affects the subthreshold behaviour has been carried out for large and small geometry devices. The effects of terminal voltages and geometry dependence of the subthreshold behaviour have been studied carefully. A semi-empirical subthreshold model suitable for circuit simulation is proposed based on the experimental observation and theoretical results.

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Chapter 1

Introduction

1.1 History of MOS Technology

The principle of MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) was first proposed by Lilienfeld in the 1920s and by Heil in the 1930s [1,2]. It was subsequently studied by Shockley and Pearson in the late 1940s [3]. The basic transistor physics was by then understood and although the new transistor structure that was proposed was very similar to today's devices it did not work because there was no technology to control surface states. In 1953, Brown [4] theoretically modelled the surface band bending of a semiconductor and gave experimental proofs of conduction in an n-type inversion channel across the surface of the p-type base layer of a Ge n-p-n bipolar transistor. Ian Ross was the first to describe the modern enhancement-mode MOSFET structure in a 1957 patent disclosure using Brown's observations [2].

The transistor technology and new device structures developed quickly in the 1960s. In 1960, Kahng and Atalla proposed and fabricated the first MOSFET using a thermally oxidized silicon surface[1]. Noyce invented the monolithic integrated circuit concept in 1960 and used the planar processing technique to fabricate the first monolithic silicon integrated circuits[2]. CMOS (Complementary MOS) was invented by Wanlass in 1963[5] and the first two commercial MOSFETs were announced in late 1964. Another important development was the silicon gate process reported by Kerwin, Klein and Sarace in 1963 [2]. This process provides self-alignment of the gate over the drain and source junctions. It is widely-used

today to produce micron and submicron feature sizes in silicon MOSFETs and BJTs (Bipolar Junction Transistors).

In the mid-60s, there were four important technology discoveries which still form the basis in today's silicon VLSI fabrication technology. In 1964, Snow *et al.* [6] identified sodium ion drift in thermally grown oxide as the principal cause of threshold voltage instability in the electrical characteristics of silicon MOSFETs. In the same year, Kerr and Young [2] discovered that the silicon dioxide film can be electrically stabilized to eliminate sodium ion drift by growing a phosphorus silicate glass (known as PSG) layer. In 1965, Pieter Balk suggested that hydrogen can anneal out surface states (interface traps at the oxide/silicon interface) by tying up the dangling silicon and oxygen bonds [2]. In the same year, Balk, Burkhardt and Gregor at IBM[7], Delord, Hoffman and Stringer at Reed College in Oregon[8], Miura at NEC Japan[9] independently discovered that the surface or interface state density is lower on the oxidized $\langle 100 \rangle$ silicon surface than on the $\langle 110 \rangle$ and $\langle 111 \rangle$ surfaces. In 1967, a one transistor dynamic memory cell for use in the random access memory (DRAM) was invented by Dennard [10]. The use of silicon nitride as a mask was reported by Sarace *et al.* in 1968 [11]. Although the ion implantation technique was proposed by Shockley in 1954[12] and the theoretical background for it, the LSS theory, was developed by Lindhard, Scharff and Schiött in 1963[13], it was not introduced into device manufacturing until late 60's. The first ion implanted self-aligned MOSFET was reported in 1966[14]. In 1969, Boron ions were implanted into the surface region of the channel thus providing a threshold voltage adjusting technique for MOSFETs[15]. In 1973, Dennard *et al.* developed the concept of scaling to achieve standard logic operations by using reduced-size transistors [16]. This led to increased packing density and reduced cost.

Bipolar transistors dominated the IC market in the early years. However, CMOS has eroded this bipolar dominance since 1970. Although bipolar technology has the advantage of higher speed over MOS, the latter has fewer fabrication steps, higher packing density, higher yield and thus lower costs so MOS technology is very attractive for digital circuits. The very low static power requirement of CMOS also allows high packing density circuits to be produced. For example, a DRAM chip

using CMOS has a considerably lower standby power dissipation compared to a BJT memory chip. Recently, the combination of bipolar and CMOS, i.e. BiCMOS, has nearly eliminated the advantage of the larger output driving capability of an all-bipolar circuit over a MOS circuit.

1.2 Small Geometry Effects in MOSFETs

Since the beginning of the integrated-circuit era, to reduce cost, the transistor packing density of ICs (Integrated-Circuits) has been increased steadily from small-scale integration (64-2K transistors) to today's VLSI (Very-Large-Scale Integration) (64K-4M active elements). The density of active devices on a chip has doubled about every two years for logic chips and quadrupled for memory chips. Meanwhile, the minimum feature length has been reduced by almost two orders of magnitude. The minimum dimension continues to shrink although recently the speed of decrease appears to have slowed down due to the difficulty of scaling at submicron levels. Fig. 1–1 summarises the development of IC technology [17]. Typical advanced IC products in 1987 had features in the 1.5-1.25μm size range [18] while the 0.7-0.8μm 4M-bit DRAM was just starting volume production and the 0.5-0.7μm 16M-bit DRAM chips were in the laboratory [19]. Experimental single transistors with linewidths as narrow as 0.1μm have been made successfully [17]. This advancement has been supported by several technology developments such as accurate process control, fine pattern photolithography, improved short-channel MOSFET structures and low-power circuits.

As channel length decreases, departures from ideal long-channel device behaviour, known as short-channel effects, may occur [20]. Those short-channel effects arise as a result of the two-dimensional potential distribution and high electric fields in the channel region. This two-dimensional potential results in lower punchthrough voltage, rising subthreshold current and higher subthreshold gate swing, reduction of the threshold voltage as channel length decreases and/or drain bias increases. As the electric field is high, the channel mobility becomes field-

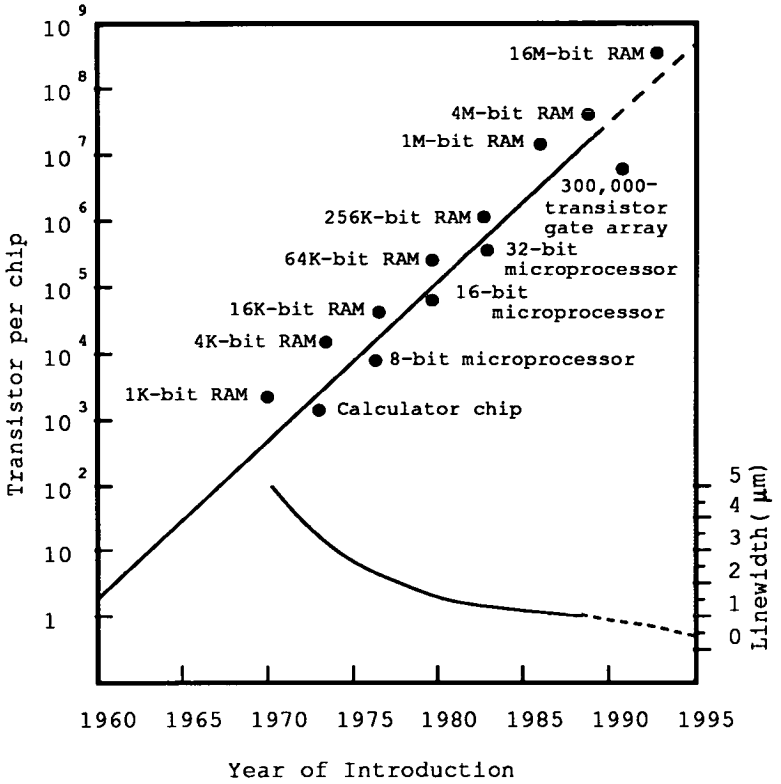


Figure 1–1: Development of IC Technology

dependent, and eventually velocity saturation occurs. When the field is increased further, carrier multiplication near the drain occurs, leading to substrate current and parasitic bipolar transistor action. High fields also cause hot-carrier injection into the oxide, leading to oxide charging and a subsequent threshold voltage shift and transconductance degradation.

One approach to avoid short-channel effects is to maintain the long-channel behaviour by simply scaling down all dimensions and voltages of the long-channel MOSFET so that the internal electric fields remain unchanged. All dimensions, i.e. oxide thickness, channel length, channel width and junction depth, are shrunk by a 'scaling factor' κ. The doping level increases by $\sqrt{\kappa}$ and all voltages are reduced by κ, leading to a reduction of the depletion layer width by about κ. Threshold voltage is also reduced approximately by κ. Therefore, the number of devices per unit area increases by a factor of κ^2, the delay time due to transit across the channel decreases by κ, the power dissipated per cell is reduced by κ^2. However, the subthreshold current and the subthreshold gate swing remain essentially the same [16]. Due to the non-ideal properties of semiconductor devices,

such as the non-scalable built-in voltage at a junction, a more generalized scaling rule was proposed. All line dimensions are scaled by λ, all voltages reduced by κ and impurity concentration is increased by λ^2/κ [21], with the result that the electric field is λ/κ of that before scaling, capacitances are reduced by λ, linear region current becomes λ/κ^2, power is λ/κ^3, power density is λ^3/κ^3, gate delay is κ/λ^2 and current density is λ^3/κ^2 of the appropriate values before scaling.

Unlike the short-channel effect which reduces the threshold voltage of MOSFETs and increases their subthreshold current, the narrow-channel effect is more complicated. For nonrecessed or semi-recessed (LOCOS) oxide isolation structures, the threshold voltage increases and the subthreshold current drops when the channel width decreases[22,23,24]. For a fully-recessed oxide isolation structure, the threshold voltage decreases and the subthreshold current increases with the channel width decreasing, called the inverse-narrow-channel effect[25].

1.3 Subthreshold Region

There are three operation regions for a MOSFET: the subthreshold or weak inversion region, the linear region and the saturation region. Before the gate voltage reaches the threshold voltage, the channel is weakly inverted and only a small diffusion current flows. This operation region is called the subthreshold or weak inversion region. In this region, the current flowing in the channel increases exponentially with the gate voltage. When the gate voltage increases above the threshold voltage, a strong inversion layer is formed beneath the gate oxide. The current in the channel increases linearly with the drain voltage and this is referred to as the linear region. As the drain voltage rises further the channel current saturates instead of increasing linearly with drain voltage. Thus the device operates in the saturation region.

The subthreshold region has not received as much attention as the other two regions due to its low current level. It was considered an 'OFF' region with zero drain current. But as feature sizes shrink and the supply voltage tends to drop,

the subthreshold behaviour can no longer be ignored. It has been demonstrated that there is a direct relationship between the reduction in the refresh time for a DRAM cell with the rise in the subthreshold current as the device dimensions are scaled down [26]. As mentioned in the last section, the subthreshold current can not be scaled down. A higher subthreshold gate swing and higher subthreshold punchthrough current for shorter MOSFETs makes the subthreshold leakage current one of dominant scaling limitations for MOSFETs [27].

As minimum feature sizes shrink below $1\mu m$, conditions increasingly favour a low supply voltage. Because a higher packing density also implies a higher internal electric field, lowering the supply voltage reduces internal electric fields. There are also other benefits: less power dissipation, less heating on the chip and thus more transistors in a given area. 4M-bit and 16M-bit DRAMs operating at 3.3V have been announced [18]. In 1990, the first 64M-bit DRAM on a single chip was announced with a 1.5V supply voltage [19]. A major beneficiary of the rising integration performance is battery-powered portable electric equipment of all kinds, such as laptop, notebook and palmtop computers. Low-voltage ICs can run directly from 1 to 3 nickel-cadmium batteries which are much lighter than their higher voltage counter parts and with lower power consumption, battery life is prolonged. Workstations today use 50MHz processors; 100MHz will be the norm and 500MHz or higher will be common by the end of the decade [28]. Higher speeds follow from smaller device geometries. Lowering the supply voltage reduces the threshold voltage which puts a greater restriction on the range of the subthreshold gate swing because devices have to turn off more quickly.

Although MOSFETs have dominated digital circuits, bipolar transistors still dominate analogue circuitry. However, the rapid increase in chip complexity has created a need to implement complete analogue-digital subsystems on the same integrated circuit using the same technology. For this reason, the implementation of analogue functions in MOS technology has become increasingly important [29]. Increasing interest has been shown in operating CMOS analogue circuits in the subthreshold region due to noise and gain improvement and the lower power consumption. For example, Vittoz and Fellrath designed a CMOS current reference

and an amplitude detector based on known bipolar circuits [30]. They believe that the well-controlled exponential transfer characteristics and excellent DC current source behaviour of both types of MOS transistors operating in weak inversion indicate that some circuit schemes used with bipolar technology can be implemented in CMOS. In addition, CMOS offers the advantage of the truly negligible gate current and of wide range of transfer characteristic slope. Tsividis and Ulmer designed a voltage reference for analogue-digital LSI CMOS. Part of the circuit operates in the weak inversion region for its low power consumption [31]. Degrauwe *et al.* designed two transconductance amplifiers for the better gain and noise performance when operating in weak inversion region [32]. To simulate analogue MOS circuits which operate in the subthreshold region, an accurate subthreshold model is necessary.

The one-dimensional model is no longer accurate since the potential distribution is two-dimensional for short-channel or narrow-channel MOSFETs and three dimensional for small geometry devices (short- and narrow-channel at the same time). Two- and three-dimensional numerical models have been developed. But numerical analysis is not a cost-effective method for circuit simulation and statistical modelling in process diagnosis due to its time and memory-consuming nature and convergence problems. Analytical techniques to characterize small geometry MOSFETs have been developed recently by solving the two-dimensional Poisson's equation with approximate boundary conditions. The accuracy of the analytical solution of the Poisson equation is strongly dependent on the choice of boundary conditions. An analytical two-dimensional subthreshold model for short-channel MOSFETs with ion implanted channel is presented in this thesis. More accurate boundary conditions at the source and drain ends are used. An analytical expression of the subthreshold gate swing is given and the bulk punchthrough current is considered. Ion implantation has became the standard MOS process step to adjust threshold voltage and to prevent punchthrough. It has significant impact on the subthreshold behaviour. A detailed study of how ion implantation affects the subthreshold behaviour of large and small devices has been carried out. A simple closed formula or compact model is needed for using in a circuit simulator or for

statistical modelling in process control. A semi-empirical model which accounts for the influence of substrate and drain bias and geometry dependence is proposed after the dependence of the subthreshold gate swing on the terminal voltages and geometries has been examined carefully.

Chapter 2

Subthreshold Models of MOSFETs

2.1 Introduction

Before going into detail about subthreshold models of MOSFETs, a brief introduction to the general electrical behaviour of MOSFETs and to their models is appropriate.

The basic structure of an n-channel MOSFET[1] is illustrated in Fig. 2–1 [20].

There are three operation regions for a MOSFET: the subthreshold or weak inversion region, the linear region and the saturation region. Before the gate voltage reaches the threshold voltage, the channel is weakly inverted and only a small diffusion current flows. This operation region is called the subthreshold or weak inversion region. In this region, the current flowing in the channel increases exponentially with the gate voltage. When the gate voltage increases above the threshold voltage, a strong inversion layer is formed beneath the gate oxide. The current in the channel increases linearly with the drain voltage and this is referred to as the linear region. As the drain voltage rises further the channel current saturates instead of increasing linearly with drain voltage. Thus the device operates in the saturation region. This is because when V_D reaches the Saturation Voltage V_{Dsat}, the surface potential at the drain end ceases to increase with V_D and saturates at a value ψ_{sat}. Fig. 2-2 illustrates the drain characteristic curve of a MOSFET, Fig. 2-3 shows the same characteristic on the semi-log scale to emphasize the subthreshold behaviour. Fig. 2-4 is the transfer or gate turn-on characteristic

[1] Only n-channel MOSFETs with a grounded source are analyzed in this thesis, unless otherwise stated.

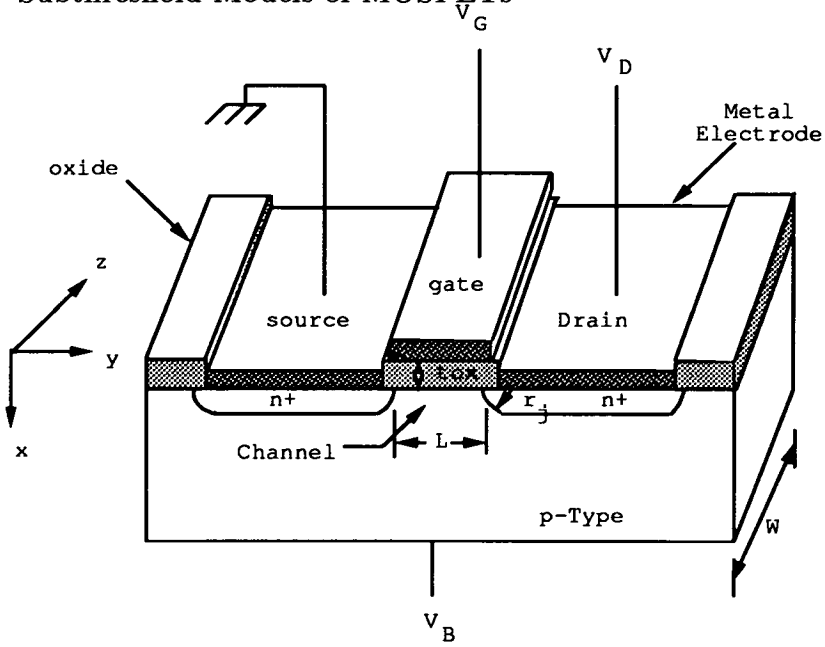


Figure 2–1: Basic structure of a MOSFET

curve. Fig. 2–5 presents it in the semi-log form to show the subthreshold characteristic more clearly. These figures show the three operation regions and their characteristics mentioned above.

With the development of VLSI, circuits have become more complex and it is not only costly but also time-consuming to fabricate a circuit in order to test a design. Therefore, circuit simulation has become an essential tool for circuit design engineers because it can give an initial representation of circuit performance more quickly and at much lower cost than by a purely experimental approach. Circuit simulation is also very important for process engineers to connect process parameters with the circuit performance in order to control process parameters and to improve the process.

MOSFETs are basic components of all MOS integrated circuits. For the purpose of circuit simulation, models which describe a single device are needed first. There are two levels of MOSFET model. One group consists of models which are suitable for circuit simulation, such as SPICE2 level 1 [33,34] and level 3 [35], those proposed by Wright [36] and by Oakley and Hocking(CASMOS) [37]. These models give a description of the relationship between the drain current and terminal voltages in an explicit closed-form formula. They require as input, a set of model parameters to give a unique description of a particular device. Models in

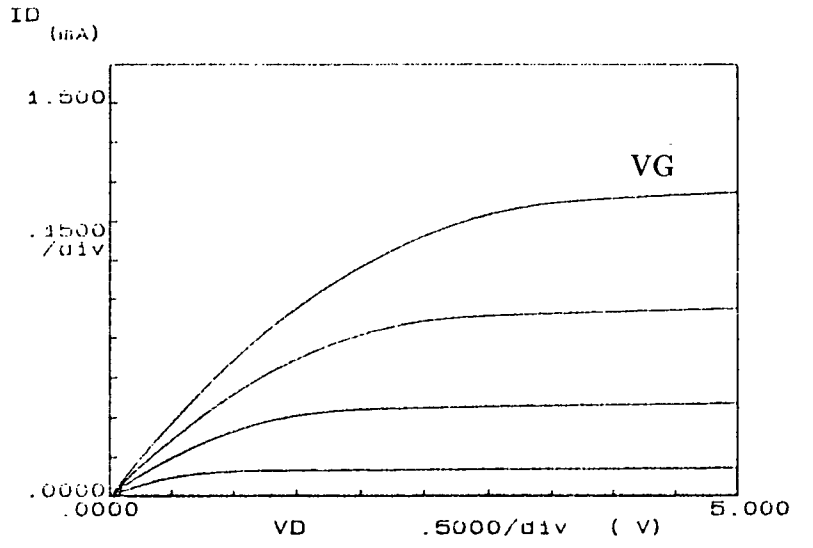


Figure 2–2: Drain characteristic of an n-channel MOSFET

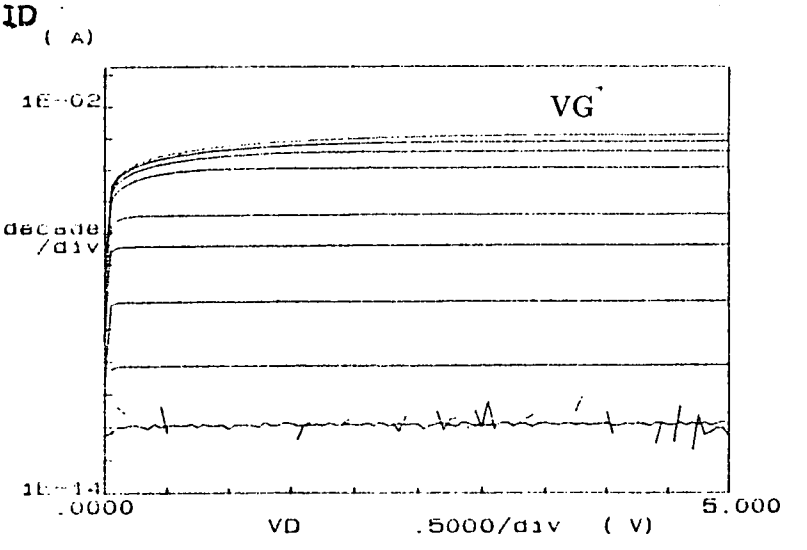


Figure 2–3: Drain characteristic of an n-channel MOSFET in semi-log scale

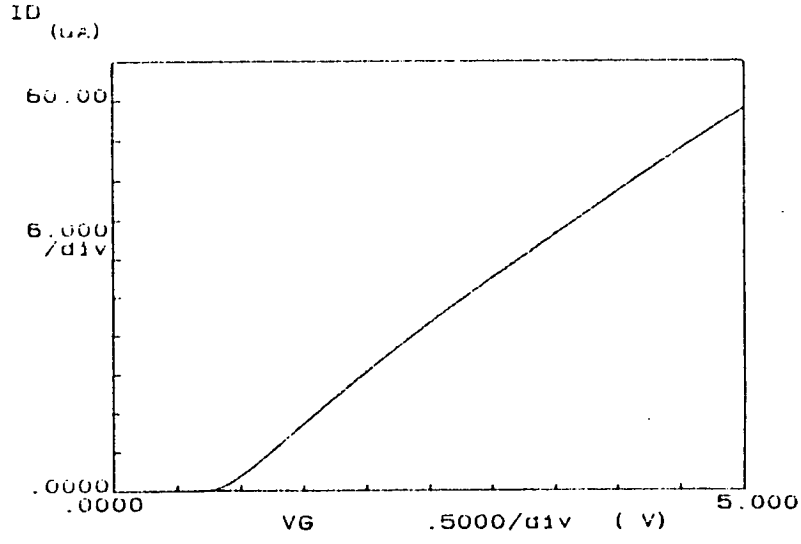


Figure 2–4: Transfer characteristics of an n-channel MOSFET

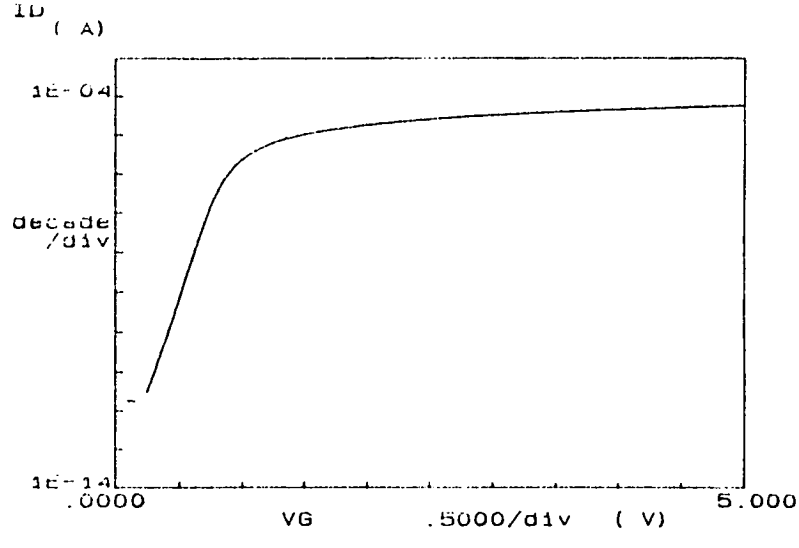


Figure 2–5: Transfer characteristic of an n-channel MOSFET in semi-log scale

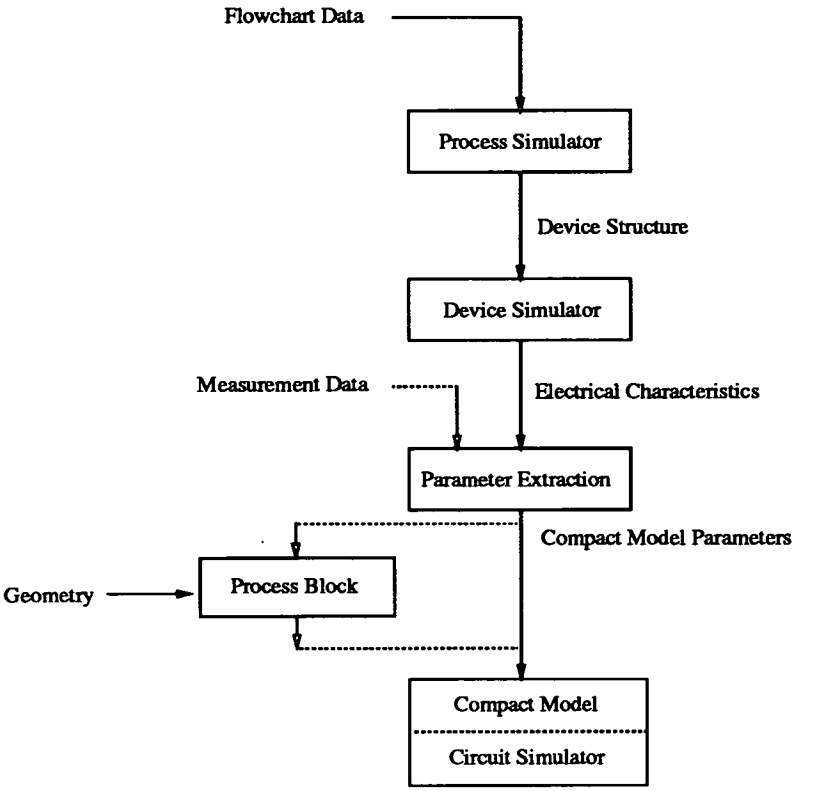


Figure 2–6: Schematic diagram of design and fabrication

this group have to be simple enough to enable their parameters to be extracted easily from characteristics of devices and to be easily modified to include second order effects. They will be discussed in more detail in Section 2.6.

Another group of models are based on the solution of Poisson's equation and current-continuity equations. There are two approaches being used to develop these models, namely the numerical technique and the analytical technique. They will be discussed in detail in Section 2.3 and Section 2.4 . These models only need the device structure (doping profile, oxide, channel length, p, n region etc.) to be specified and will generate electrical characteristics of MOSFETs. From the output of these models, the input parameters for device models for circuit simulation can be extracted.

Fig. 2–6 shows a flow chart of how the process, device and circuit simulators may be used interactively for design and fabrication of MOS integrated circuits [38].

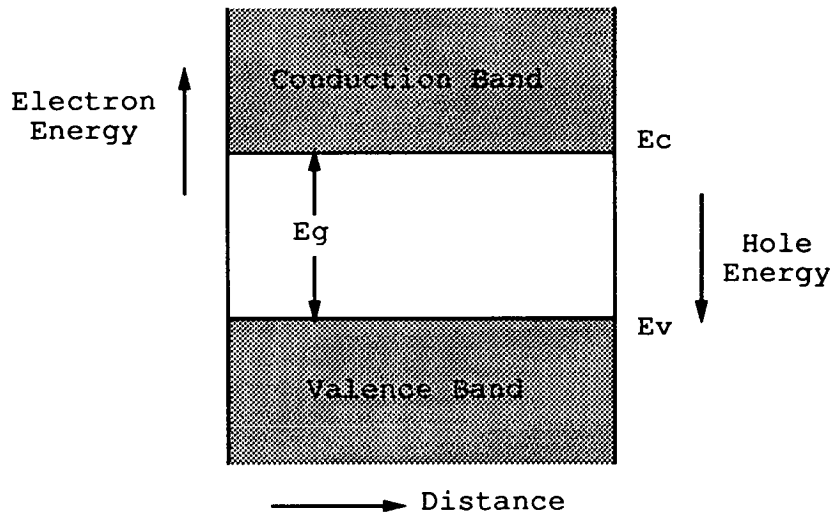


Figure 2–7: Simplified band diagram of a semiconductor

2.2 Basic Physics

2.2.1 Physics of Semiconductor Relevant to MOSFETs

To understand the operation of MOSFETs more easily and clearly, it is necessary to use the energy band diagram. A simplified band diagram of a semiconductor is shown in Fig. 2–7 [20]. For a semiconductor, there is a forbidden energy region in which no states are allowed to exist. Above and below the forbidden region, there are conduction bands and valence bands. The separation between E_c, the energy of the lowest conduction band, and E_v, the energy of the highest valence band, is called the bandgap, E_g. Electron energy increases when measured upwards; hole energy increases when measured downwards.

The Fermi level E_F is a very important parameter in the physics of semiconductors. It is defined as the chemical potential of electrons in a solid. If the Fermi level is not constant throughout the semiconductor, then electrons and holes will redistribute themselves until the Fermi level is constant throughout the semiconductor, i.e. thermal equilibrium is reached [39].

The Fermi level can be derived from following formula:

$$n = \int_{E_c}^{E_{top}} N(E)f(E)dE \tag{2.1}$$

where n is the electron density, $N(E)$ is the electron density of states.

$$f(E) = \frac{1}{1 + e^{\frac{E-E_F}{kT}}} \tag{2.2}$$

f is the Fermi-Dirac distribution function and represents the probability of an electron state with energy E being occupied by an electron. k is Boltzmann's constant, T is the absolute temperature. The meaning of Eq. (2.1) is that the sum of all probabilities of all energy levels being occupied by electrons in the semiconductor should equal to the sum of all electrons in the semiconductor. From Eq. (2.2), one can notice that the Fermi level is the energy level at which the probability of occupation of an energy state by an electron is exactly one-half.

The Fermi level of an intrinsic semiconductor, E_i, is very close to the middle of the bandgap. The conducting carriers of an intrinsic semiconductor can only be generated by exciting electrons from valence bands to conduction bands. When a semiconductor is doped with impurities, impurity energy levels are introduced into the forbidden region. For example, in phosphorus or arsenic doped silicon, a donor energy level is introduced into the forbidden region. Because the donor energy level is very near the bottom of the conduction band, the donor is almost totally ionized at room temperature. So, there are many more free electrons than free holes, hence the semiconductor is n-type. To preserve charge neutrality, the Fermi level has to adjust itself. In this example, the Fermi level, E_F, is moved above the intrinsic Fermi level, E_i. Schematic band diagrams for an intrinsic semiconductor, n-type and p-type semiconductors at thermal equilibrium are shown in Fig. 2–8 [20].

2.2.2 Physics of MOSFETs

Having discussed the energy band diagram of a semiconductor in Section 2.2.1, the energy band diagram of a MOSFET will be discussed in this section.

Fig. 2–9 [20] shows the energy band diagram of an ideal MOS structure with p-type semiconductor substrate. An ideal MOS structure means that the work

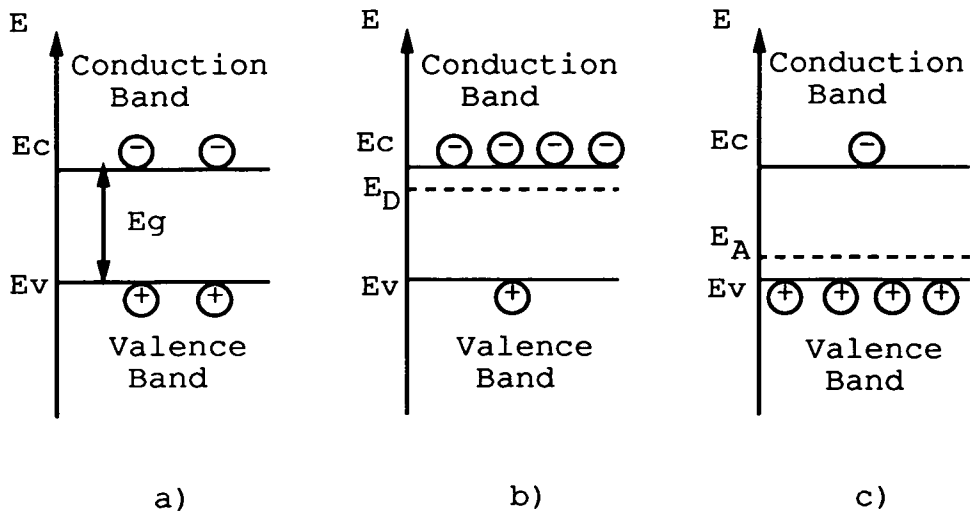


Figure 2–8: Schematic band diagram a) intrinsic, b) n-type, c) p-type semiconductors at thermal equilibrium

function difference between the gate material and the semiconductor, ϕ_{ms}, is zero and there are no charges existing in the oxide. For a real MOS structure, the work function difference, ϕ_{ms}, is not zero and there are charges present in the oxide but the difference does not affect the basic analysis of device operation. Since an n-channel MOSFET has a p-type substrate, a p-type semiconductor MOS structure is discussed here. For a p-type semiconductor MOS structure,

$$\phi_{ms} = \phi_m - \left(\chi + \frac{E_g}{2q} + \psi_B\right) \tag{2.3}$$

where ϕ_m is the work function of the gate material, χ is the semiconductor electron affinity, ψ_B is the difference between the Fermi level E_F and the intrinsic Fermi level E_i. q is the elementary charge. The flat band voltage V_{FB} is defined as

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \tag{2.4}$$

where

Q_{ox} is the charge density in the gate oxide, including oxide fixed charges, mobile ions and oxide trapped charges;

C_{ox} is the capacitance of the oxide layer, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$;

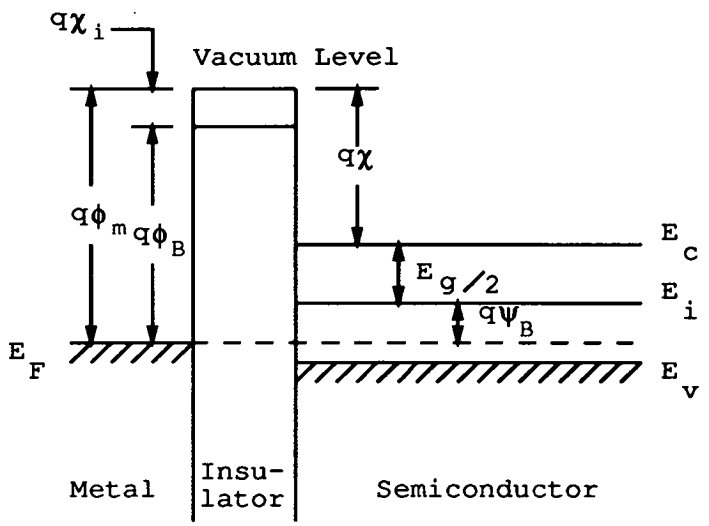


Figure 2–9: Band diagram of an ideal MOS structure with p-type semiconductor

ϵ_{ox} is the permittivity of oxide;

t_{ox} is the thickness of oxide.

Depending on the sign of V_{FB}, the energy bands of the semiconductor at the surface will bend upwards ($V_{FB} > 0$) or downwards ($V_{FB} < 0$). A p-type semiconductor with an n^+ polysilicon gate MOS structure may be used as an example. The work function difference, ϕ_{ms}, is about $-1V$. The exact value of ϕ_{ms} depends on the acceptor doping level which decides the Fermi level in the semiconductor. Neglecting oxide charges, the flat band voltage V_{FB} is equal to the work function difference ϕ_{ms}. Fig. 2–10 shows the energy band diagram of a p-type semiconductor with an n^+ polysilicon gate MOS structure without applying gate bias. If the gate voltage $V_G = V_{FB}$ applied, then the semiconductor energy band will be flat as shown in Fig. 2–9.

Fig. 2–11 [20] shows different energy band diagrams of a MOS structure under different gate bias conditions. Defining the surface potential ψ_s as surface band bending, then it is clearly shown in Fig. 2–11 that when $V_G - V_{FB} < 0$, $\psi_s < 0$, the semiconductor surface is in the condition of accumulation of holes. When $V_G - V_{FB} > 0$ but $0 < \psi_s < \psi_B$, the surface is in the depletion condition. When V_G increases and $\psi_B \leq \psi_s < 2\psi_B$, the surface is weakly inverted, since the electron

density at the surface begins to exceed the intrinsic electron density but is less than the hole density in the bulk. When V_G increases continually until $\psi_s \geq 2\psi_B$, strong inversion occurs and at that point the electron density at the surface begins to exceed the hole density in the bulk.

2.2.3 Basic Physics Equations

To understand electrical characteristics of MOSFETs, two equations are essential. They are Poisson's equation and current-continuity equations [20].

A two-dimensional Poisson's equation has the form:

$$\frac{\partial^2 \psi}{\partial x^2} + \frac{\partial^2 \psi}{\partial y^2} = -\frac{\rho}{\epsilon_{si}} \tag{2.5}$$

where $\psi(x, y)$ is the electrostatic potential, ρ is the charge density per unit volume.

Poisson's equation is derived from Gauss' Law and describes the relationship between the potential and the charge density. One can solve Poisson's equation with appropriate boundary conditions to obtain potential distributions for MOSFETs.

Current-continuity equations have the form:

$$\frac{\partial n}{\partial t} = G_n - U_n + \frac{1}{q}\nabla \cdot \mathbf{J}_n \tag{2.6}$$

$$\frac{\partial p}{\partial t} = G_p - U_p - \frac{1}{q}\nabla \cdot \mathbf{J}_p \tag{2.7}$$

where n and p are the electron and the hole density. G_n and G_p are the electron and the hole generation rate, caused by external influences. U_n and U_p are the electron recombination rate in p-type semiconductors and the hole recombination rate in n-type semiconductors. $\mathbf{J}_n$ and $\mathbf{J}_p$ are the electron and the hole current density, respectively.

The electron and the hole current density can be expressed by current-density equations.

$$\mathbf{J}_n = q\mu_n n\mathcal{E} + qD_n \nabla n \tag{2.8}$$

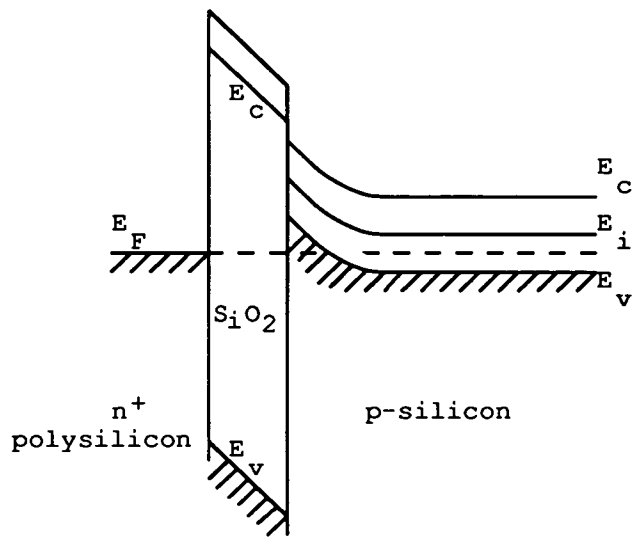


Figure 2–10: Energy band diagram of a p-type semiconductor with an n^+ polysilicon gate MOS structure

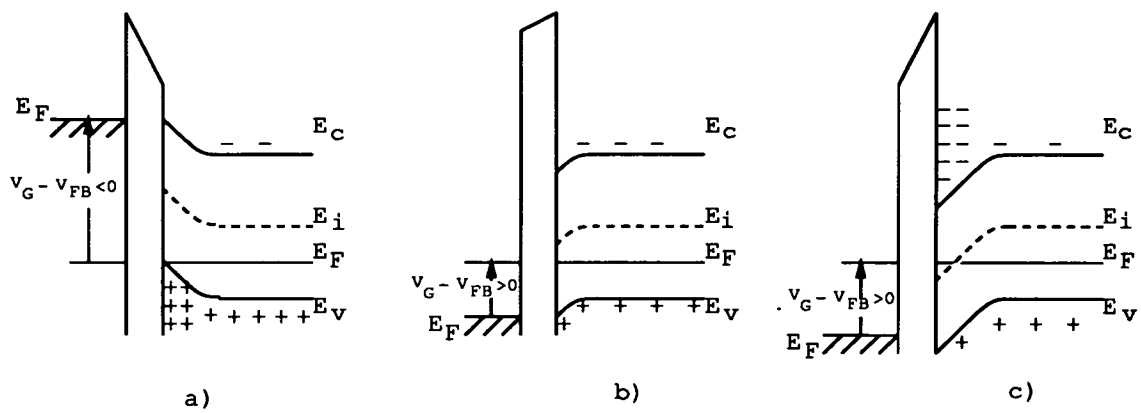


Figure 2–11: Energy band diagram for a p-type semiconductor MOS structure when $V_G - V_{FB} \neq 0$. a) accumulation, b) depletion, c) inversion.

$$\mathbf{J}_p = q\mu_p p\mathcal{E} - qD_p\nabla p \tag{2.9}$$

The first terms in the right hand side of Eq. (2.8) and (2.9) are drift components caused by the electrical field. The second terms are diffusion components caused by the carrier concentration gradient. μ_n and μ_p are the electron and hole mobility terms. D_n and D_p are the electron and hole diffusion constants for nondegenerate semiconductors. $\mathcal{E}$ is the electric field. The Einstein relationship gives $D_n = \frac{kT}{q}\mu_n$ and $D_p = \frac{kT}{q}\mu_p$.

Finally, the total current density is the sum of the electron and the hole current density, that is

$$\mathbf{J}_{cond} = \mathbf{J}_n + \mathbf{J}_p \tag{2.10}$$

2.3 Numerical Simulators

As mentioned in Section 2.1 , it is necessary to have device simulators which are based on descriptions of device structure, *eg.* the substrate doping profile, the channel length, the source and drain junction depth etc., and can produce accurate electrical characteristics of MOSFETs. There are a few numerical device simulators available, for example CANDE [40], PISCES [41], MINIMOS [42]. Although details of solution techniques vary in different simulators, the basic idea is the same, i.e. solving Poisson's equation and current-continuity equations simultaneously and by discretization. Since the same physics equations are valid in all operation regions, there is no need to treat them differently in different regions for a numerical simulator. The different behaviour in different operation regions will come out naturally from the solution of Poisson's equation and current-continuity equations. For example, for a long-channel MOSFET in the subthreshold region, the numerical solution will naturally reflect the facts that the surface potential is constant in most parts of the channel and the lateral field is near zero under the subthreshold bias condition. So the drift current is very small compared to the diffusion current. The exponential dependence of the drain current on the gate voltage comes out naturally because

1. the diffusion component dominance of the drain current,

2. the exponential dependence of the electron density on the surface potential,

3. the nearly linear dependence of the surface potential on the gate voltage.

In addition to the capability mentioned above, the simulator CANDE can calculate the drain current in the subthreshold region and the linear region analytically using a numerical solution of Poisson's equation without solving the current-continuity equations. This concept enables the development of analytical subthreshold models of short-channel MOSFETs. This will be discussed in Section 2.4.3 .

Since they are able to show distributions of the potential, electric field, carrier concentration and current density in the structure of a device, numerical device simulators can bring physical insight into device performance. They predict device performance reasonably accurately if one chooses carefully the coefficients of the solution technique, such as the size of the discretization mesh, etc. However, their disadvantages are that they are time-consuming and cannot connect process parameters with device's performance directly. As a compromise between time-efficiency, simplicity and accuracy, people develop analytical models which can show the relationship between process parameters and the device's performance, such as the drain current, subthreshold gate swing, transconductance etc. directly.

2.4 Analytical Models

Unlike numerical models which solve the same equations for all operation regions, analytical models use different techniques for different operation regions according to the dominant conducting mechanism. For example, in a subthreshold model, the effect of minority carriers on the electric field is ignored and only the diffusion current of minority carriers is considered to contribute to the drain current. Existing models for the subthreshold region are reviewed in the following subsections.

2.4.1 Models for Long-Channel MOSFETs with Uniform Substrate Doping

The drain current in the subthreshold region is first calculated by Guzev *et al.* [43] as a drift current due to the lateral field. Swanson and Meindl [44] treated the subthreshold drain current as a drift current, and applied it to a low voltage CMOS inverter. Although they had the right expression, the concept is wrong as pointed out by Overstraeten [45]. Stuart and Eccleston [46] noted that the subthreshold drain current is a diffusion current and that the drain current increases exponentially with the gate voltage. Then Barron [47] gave the first complete theoretical analysis of the subthreshold behaviour of a p-channel MOSFET. Since Barron's and many other subthreshold models for long-channel MOSFETs are based on the double integral model developed by Pao and Sah in the mid-1960's[48], it will be described first. Unless otherwise stated, an n-channel MOSFET with grounded source is analyzed in this thesis. For a p-channel MOSFET, the procedure of the analysis is the same, only the signs need to be changed. Fig. 2–1 shows the coordinate system used. The potential reference is chosen at the intrinsic Fermi level, see Fig. 2–12.

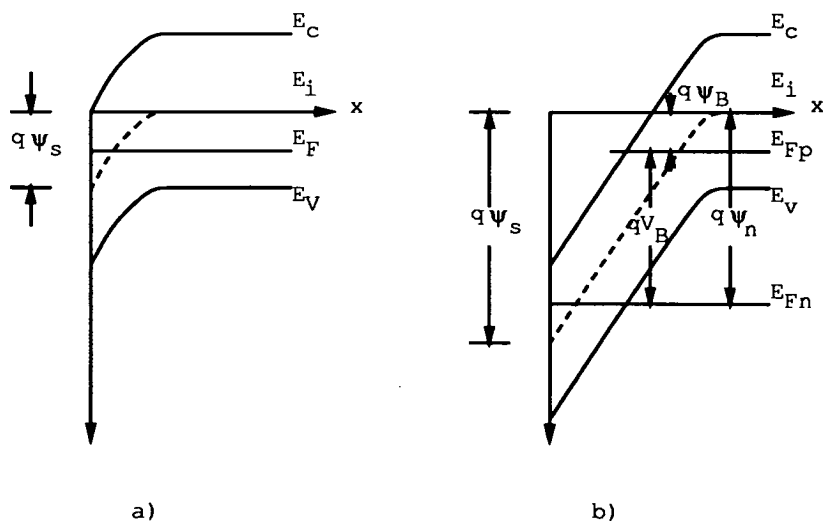


Figure 2–12: Energy band diagram of an inverted p region for a) the equilibrium case b) the nonequilibrium case at the channel.

The current density in the channel may be written as

$$\mathbf{J} = \mathbf{J}_n + \mathbf{J}_p \tag{2.11}$$

Because an n-channel device is considered here, $\mathbf{J}_p$ may be neglected. Hence

$$\mathbf{J} \approx \mathbf{J}_n = q\mu_n n\mathcal{E} + qD_n\nabla n \tag{2.12}$$

If the gradual channel approximation, i.e. $\mathcal{E}_y \ll \mathcal{E}_x$, is assumed, the Eq. (2.12) may be reduced to one dimension, that is

$$J(x,y) = q\mu_n n\mathcal{E}_y + qD_n\frac{\partial n}{\partial y} \tag{2.13}$$

where $\mathcal{E}_x$ is the transverse field, $\mathcal{E}_y$ is the longitudinal field. Making use of the Einstein relation $D_n = \frac{kT}{q}\mu_n$, then

$$J(x,y) = -qD_n n\frac{\partial \xi}{\partial y} \tag{2.14}$$

where ξ is the electron quasi-Fermi level measured from the bulk Fermi level and normalized to $\frac{kT}{q}$, i.e. $\xi = \frac{q}{kT}(\psi_n - \psi_B)$. ψ_n is the electron quasi-Fermi level, defined as $n = n_i \exp[\frac{q}{kT}(\psi - \psi_n)]$, n_i is the intrinsic carrier density.

The drain current may be written as

$$I_D = \int_0^{x_i} J(x,y)W dx = -\int_0^{x_i} qD_n n\frac{\partial \xi}{\partial y}W dx \tag{2.15}$$

where x_i denotes the point at which the intrinsic Fermi level intersects the electron quasi-Fermi level. W is the width of the channel. If an assumption $\frac{\partial \xi}{\partial x} = 0$ is made, i.e. no current flows in a direction normal to the interface, then

$$I_D = -D_n qW\frac{d\xi}{dy}\int_0^{x_i} n(x,y)dx \tag{2.16}$$

Integrating the drain current I_D from source to drain, since I_D is the same all along the channel, it becomes

$$I_D = -\frac{1}{L}\int_0^L D_n qW\frac{d\xi}{dy}\int_0^{x_i} n(x,y)dxdy \tag{2.17}$$

where L is the length of the channel. The electron density

$$n = n_i e^{u-u_n} = n_i e^{u-\xi-u_B},$$

where

u, u_B, u_n are the electrostatic potential, the equilibrium Fermi potential in the bulk, and the electron quasi-Fermi level respectively, all normalized to $\frac{kT}{q}$.

Substituting the expression for n into Eq. (2.17), one has

$$\begin{aligned} I_D &= -\frac{1}{L}\int_0^{\frac{qV_D}{kT}} D_n qW \int_0^{x_i} n_i e^{u-\xi-u_B} dx d\xi \\ &= -\frac{1}{L} qW n_i D_n \int_0^{\frac{qV_D}{kT}} \int_{u_s}^{0} e^{u-\xi-u_B} \frac{1}{\frac{du}{dx}} du d\xi \end{aligned} \tag{2.18}$$

where u_s is the surface potential, normalized to $\frac{kT}{q}$. The solution of Poisson's equation is presented in Appendix A. Substituting Eq. (A.9) into (2.18), assuming D_n is constant along the channel, i.e. μ_n is constant along the channel, yields

$$I_D = \frac{qW D_n n_i L_d}{L} \int_0^{\frac{qV_D}{kT}} \int_0^{u_s} \frac{e^{u-\xi-u_B}}{F(u,\xi,u_B)} du d\xi \tag{2.19}$$

To derive the relation between the gate voltage V_G and the surface potential ψ_s, making use of Gauss' Law

$$\begin{aligned} Q_s &= -\epsilon_{si}\mathcal{E}_s = \epsilon_{si}\left(\frac{d\psi}{dx}\right)_{x=0} = \frac{kT}{q}\epsilon_{si}\left(\frac{du}{dx}\right)_{x=0} \\ &= -\frac{kT}{q}\frac{\epsilon_{si}}{L_d} F(u_s,\xi,u_B) \end{aligned} \tag{2.20}$$

where

Q_s is the total charge induced in the semiconductor per unit area;

$\mathcal{E}_s$ is the surface transverse electrical field;

ϵ_{si} is the permittivity of silicon;

L_d is the intrinsic Debye length, $L_d = \left[\frac{\epsilon_{si}}{2qn_i\beta}\right]^{\frac{1}{2}}$. where $\beta = \frac{q}{kT}$.

Since from the charge conservation law, $Q_s = -C_{ox}(V_G - V_{FB} - \psi_s)$, then

$$\begin{aligned} V_G &= \psi_s + V_{FB} - \frac{Q_s}{C_{ox}} \\ &= \frac{kT}{q}u_s + V_{FB} + \frac{kT}{q}\frac{\epsilon_{si}}{C_{ox}L_d} F(u_s,\xi,u_B) \end{aligned} \tag{2.21}$$

The Pao-Sah double integral model agrees with experimental results very well. However, the calculation has to be done numerically. It is desirable to have a

simple closed-form current expression for the subthreshold region. Thus Barron [47] applied Pao-Sah theory to a p-type MOSFET in the subthreshold region. He assumed that there is no current component flow normal to the interface. This is true for channel areas which are far away from the drain depletion region. He considered that only ionized donors contribute to the electric field in the depletion region. He found out that the surface potential is constant through most of the channel in the subthreshold region. After using the above assumptions and mathematical approximations, finally, he derived a source current expression,

$$I_S = \frac{qWD_p n_i L_d e^{\frac{3u_B}{2}}}{L\sqrt{-(u_s+1)}} e^{-u_s}\left(1 - e^{\frac{qV_D}{kT}}\right) \tag{2.22}$$

and a gate voltage and surface potential relationship

$$u_s = u'_G + \frac{q}{kT}\frac{Q_{fs}}{C_{ox}} - B\left\{1 - \left[1 - \frac{2}{B}\left(u'_G - \frac{qQ_{fs}}{kTC_{ox}} + 1\right)\right]^{\frac{1}{2}}\right\} \tag{2.23}$$

where I_S is the source current. It should be equal to the drain current I_D if only the surface channel current has been considered. $u'_G = \frac{q}{kT}(V_G - V_{FB})$, Q_{fs} is the charges in fast states, $B = \frac{C_D^2 N_A}{2C_{ox}^2 n_i}$. The results from the model agree well with the experimental data of his p-channel devices.

Troutman and Chakravarti [49] and Masuhara *et al.* [50] applied the Pao-Sah double integral model in the subthreshold region and included the effect of the substrate bias. The latter demonstrated how important it is to consider the subthreshold current for a low supply voltage circuit by comparing the transfer characteristics of a static inverter with and without considering the subthreshold current.

Brews proposed a charge-sheet model for MOSFETs including the subthreshold region [51] based on previous work by Guerst [52], Loeb, Andrew and Love [53], Armstrong, Magowan and Ryan [54]. Those charge-sheet models treated the inversion layer as a conducting plane of zero thickness, thus the effect of minority carriers in the inversion layer on potential distribution can be ignored. The subthreshold current expression in Brews' charge sheet model is essentially the same as that of Barron's except that it is for nMOS devices and Q_{fs} is not considered.

Fichtner and Pötzl [55] considered a MOSFET operating in the subthreshold region as an npn bipolar transistor with homogeneous base doping because the drain current in the subthreshold region is dominated by the diffusion current. The drain current can be calculated in the same way as the collector current. i.e.

$$I_D = -qAD_n\frac{dn}{dy} = -qAD_n\frac{n(L)-n(0)}{L} \tag{2.24}$$

where A is the cross section of the current flow. $n(L)$ and $n(0)$ are the electron density at the drain and the source ends, respectively. Since

$$n(x) = n_i e^{\beta(\psi-\psi_n)} \tag{2.25}$$

where $\beta = \frac{q}{kT}$. The electron quasi-Fermi level

$$\psi_n(L) = \psi_B + V_D - V_B \tag{2.26}$$

$$\psi_n(0) = \psi_B - V_B \tag{2.27}$$

So,

$$n(L) = n_i e^{\beta(\psi_s - V_D + V_B - \psi_B)} \tag{2.28}$$

$$n(0) = n_i e^{\beta(\psi_s + V_B - \psi_B)} \tag{2.29}$$

Then

$$I_D = \frac{qWD_n t_{ch} n_i}{L}[e^{\beta(\psi_s - V_B - \psi_B)} - e^{\beta(\psi_s - V_D + V_B - \psi_B)}] \tag{2.30}$$

where t_{ch} is the effective channel thickness.

Because of the exponential dependence of electron density on potential ψ, t_{ch} may be considered as the distance where $\psi = \psi_s - \frac{kT}{q}$, i.e. $n(t_{ch}, y) = n(0, y)e^{-1}$.

Assuming that the transverse field $\mathcal{E}_x = -\frac{\partial\psi}{\partial x}$ is constant along x, then the surface electrical field is

$$\mathcal{E}_s = \frac{\psi - \psi_s}{t_{ch}} = \frac{kT}{q}\frac{1}{t_{ch}} \tag{2.31}$$

Therefore,

$$t_{ch} = \frac{kT}{q}\frac{1}{\mathcal{E}_s} = \frac{1}{\beta\mathcal{E}_s} \tag{2.32}$$

In order to know $\mathcal{E}_s$, Poisson's equation should be solved. Poisson's equation in the channel and the depletion region of an n-type device may be written as

$$\frac{\partial^2\psi}{\partial x^2} = \frac{q}{\epsilon_{si}}(n + N_A) \approx \frac{q}{\epsilon_{si}}N_A \tag{2.33}$$

In the subthreshold region, the semiconductor surface is weakly inverted. In comparison with ionized acceptors, electrons in the channel may be neglected.

$N_A \simeq p_{p0} = n_i e^{\beta\psi_B}$, so

$$\frac{d^2\psi}{dx^2} = \frac{qn_i}{\epsilon_{si}}e^{u_B} \tag{2.34}$$

Following the same procedure of solving the Poisson's equation as in the Pao-Sah model, one gets

$$\left(\frac{d\psi}{dx}\right)_{x=0} = -\left(\frac{2qn_i}{\beta\epsilon_{si}}\right)^{\frac{1}{2}}(u_s e^{u_B})^{\frac{1}{2}} \tag{2.35}$$

Because $\psi_B = \frac{kT}{q}\ln\frac{N_A}{n_i}$, so $e^{u_B} = \frac{N_A}{n_i}$.

$$\left(\frac{d\psi}{dx}\right)_{x=0} = -\left(\frac{2qn_i}{\beta\epsilon_{si}}\frac{N_A}{n_i}\right)^{\frac{1}{2}} u_s^{\frac{1}{2}} \tag{2.36}$$

If it is defined that the extrinsic Debye length $L_B = \left[\frac{\epsilon_{si}}{qN_A\beta}\right]^{\frac{1}{2}}$, then Eq. (2.36) can be rewritten as

$$\mathcal{E}_s = -\left(\frac{d\psi}{dx}\right)_{x=0} = \frac{\sqrt{2}}{\beta L_B}\sqrt{u_s} \tag{2.37}$$

Substituting Eq. (2.37) into (2.32)

$$t_{ch} = \frac{L_B}{\sqrt{2u_s}} \tag{2.38}$$

Substituting Eq. (2.38) into (2.30),

$$I_D = \frac{q\mu_n W L_B}{\sqrt{2}\beta L}\frac{n_i^2}{N_A}\frac{1}{\sqrt{\beta\psi_s}}e^{\beta\psi_s}\left(1 - e^{-\beta V_D}\right)e^{\beta V_B} \tag{2.39}$$

To relate ψ_s to V_G, using Gauss' Law and the charge conservation law, one has

$$Q_s = -C_{ox}(V_G - V_B - V_{FB} - \psi_s) = -\epsilon_{si}\mathcal{E}_s \tag{2.40}$$

Thus,

$$C_{ox}(V_G - V_B - V_{FB} - \psi_s) = \frac{\sqrt{2}\epsilon_{si}}{\beta L_B}\sqrt{\beta\psi_s} \tag{2.41}$$

Solving Eq. (2.41), one has

$$\psi_s = V_G - V_B - V_{FB} - \frac{a^2}{2\beta}\left\{\left[1 + \frac{4\beta}{a^2}(V_G - V_B - V_{FB})\right]^{\frac{1}{2}} - 1\right\} \tag{2.42}$$

where $a = \frac{\sqrt{2}\epsilon_{si}}{C_{ox}L_d}$.

From all the models mentioned above, it can be seen that the subthreshold drain current, I_D, of a long-channel MOSFET depends exponentially upon the gate voltage, V_G, but it is independent of the drain voltage, V_D, when the drain voltage is more than several $\frac{kT}{q}$.

The subthreshold gate swing is an important parameter for device design consideration. It estimates how much reduction of the gate voltage is needed to reduce the drain current by one decade, that is[56]

$$\begin{aligned} S &= \frac{dV_G}{d(\log_{10} I_D)} = \frac{kT}{q}(\ln 10)\frac{d(\beta V_G)}{d(\ln I_D)} \\ &= \frac{kT}{q}(\ln 10)\left[1 + \frac{C_D(\psi_s)}{C_{ox}}\right]\left[1 - \frac{2}{a^2}\left(\frac{C_D(\psi_s)}{C_{ox}}\right)^2\right]^{-1} \end{aligned} \tag{2.43}$$

where the differential capacitance of the semiconductor depletion layer[20]

$$C_D = \frac{\partial Q_s}{\partial \psi_s} = \frac{\epsilon_{si}}{\sqrt{2}L_B}\frac{1 - e^{-\beta\psi_s} + \frac{n_{p0}}{p_{p0}}(e^{\beta\psi_s} - 1)}{F(\beta\psi_s, n_{po}/p_{po})} \tag{2.44}$$

L_B is the extrinsic Debye length. $L_B = \left(\frac{\epsilon_{si}}{qN_A\beta}\right)^{\frac{1}{2}}$.

For a long channel device operating in the subthreshold region

$$C_D = \frac{\partial Q_B}{\partial \psi_s} = \frac{\epsilon_{si}}{w_d} \tag{2.45}$$

where Q_B is the charge per unit area within the depletion region.

$$Q_B = qN_A w_d = \sqrt{2\epsilon_{si}qN_A\psi_s} \tag{2.46}$$

w_d is the depletion region depth.

$$w_d = \sqrt{\frac{2\epsilon_{si}\psi_s}{qN_A}} \tag{2.47}$$

2.4.2 Models for Long-Channel MOSFETs with Nonuniform Substrate Doping

Subthreshold models for long-channel MOSFETs with uniform substrate doping have just been discussed in the last subsection. However, in practice MOSFETs have usually been ion implanted. A shallow ion implantation is used to shift the threshold voltage and a deeper one to prevent punchthrough in bulk. This results in a nonuniform distribution of the impurity in the substrate. Although the effect of the nonuniform doping profile on the threshold voltage has been discussed a lot [57,58,59,60], its effect on the subthreshold behaviour has not received as much attention as that on the threshold voltage. To present the subthreshold gate swing of a device with a nonuniformly doped substrate, Rideout *et al.* [61] used the expression of the subthreshold swing for a device with a uniform doping substrate and considered the effect of a step doping profile on the depletion depth in their formula. Brews [56] also developed a subthreshold model for nonuniform doping substrate MOSFETs in 1979. He derived an expression for subthreshold gate swing.

$$S = \frac{kT}{q}(\ln 10)\left(1 + \frac{C_D}{C_{ox}}\right)\left[1 - \frac{2}{a^2}\left(\frac{C_D}{C_{ox}}\right)^2 \frac{1}{1+\alpha}\right]^{-1} \tag{2.48}$$

where $a = \frac{\sqrt{2}\epsilon_{si}}{C_{ox}L_B}$ and

$$\alpha = \frac{\sqrt{2}}{a}\frac{C_D}{C_{ox}}\left[m_0 - L_B \frac{d\beta\psi_0}{dx}\,|_{x=w_d}\right] \tag{2.49}$$

$$m_0 = \frac{1}{L_B N_A}\int_0^{w_d}[N_A(x) - N_A]dx \tag{2.50}$$

$\psi_0(x)$ is the built-in potential due to the doping profile gradient itself.

We derived a subthreshold model for a MOSFET with nonuniformly doped substrate. It will be presented below. Two assumptions are used:

1. The surface potential along the entire channel is the same. Simulation results from the two-dimensional device simulator CANDE confirms that this assumption is correct along most of the channel. The only exceptions are the depletion regions at the source and the drain ends, which can be ignored for long-channel MOSFETs.

2. The drain current in the subthreshold region is dominated by the diffusion current. To maintain a constant current in the channel, the gradient of the carrier density per unit area in the channel must be the same all along the channel. That is, if the carrier density per unit area at the source is N_s, at the drain is N_d and the channel length is L, then the gradient is $\frac{N_s - N_d}{L}$.

By following the same idea as in Eq. (2.24), one has

$$I_D = WqD_n \frac{N_s - N_d}{L} \tag{2.51}$$

where W is the channel width. If one defines $n(x,0)$ as the electron density at the source end and $n(x,L)$ at the drain end, then

$$I_D = \frac{W}{L} q \frac{\mu_n}{\beta} \int_0^{w_d} [n(x,0) - n(x,L)] dx \tag{2.52}$$

where $\mu_n = \beta D_n$ is assumed constant in the channel. Appendix B shows how the depletion depth w_d may be calculated under these conditions. If one defines $n_s(0)$ and $n_s(L)$ as the surface electron density at the source and the drain respectively, according to the Boltzmann relationship, one has

$$n(x,0) = n_s(0) \exp\{-\beta[\psi_s - \psi(x)]\} \tag{2.53}$$

$$n(x,L) = n_s(L) \exp\{-\beta[\psi_s - \psi(x)]\} \tag{2.54}$$

So, Eq. (2.52) becomes

$$I_D = \frac{W}{L} q \frac{\mu_n}{\beta} [n_s(0) - n_s(L)] \int_0^{w_d} \exp\{-\beta[\psi_s - \psi(x)]\} dx \tag{2.55}$$

Now, we use an effective channel thickness t_{ch} to replace the integral term in Eq. (2.55). As pointed out by Greenfield and Dutton [40], for a surface current path, the effective channel thickness is

$$t_{ch} = \int_0^{w_d} \exp[-\beta(\psi_s - \psi)] dx \approx \frac{1}{\beta \mathcal{E}_s} \tag{2.56}$$

Substituting t_{ch} into Eq. (2.55), one has

$$I_D = \frac{W q \mu_n t_{ch}}{\beta L} [n_s(0) - n_s(L)] \tag{2.57}$$

where $n_s(0) = n_{p0}\exp[\beta(\psi_s + V_B)]$, $n_s(L) = n_{p0}\exp[\beta(\psi_s - V_D + V_B)]$, the electron density in bulk $n_{p0} = \frac{n_i^2}{N_A}$. So the subthreshold drain current

$$I_D = \frac{W}{L}\frac{q\mu_n n_{p0}}{\beta^2 \mathcal{E}_s}\exp(\beta\psi_s)[1 - \exp(-\beta V_D)]\exp(\beta V_B) \tag{2.58}$$

Now, the subthreshold gate swing S will be derived next. By definition,

$$S \equiv \frac{dV_G}{d\log_{10} I_D} = (\ln 10)\frac{dV_G}{d\ln I_D} \tag{2.59}$$

and

$$\frac{d\ln I_D}{dV_G} = \frac{d\ln I_D}{dw_d}\frac{dw_d}{dV_G} \tag{2.60}$$

From Eq. (2.58), one has

$$\frac{d\ln I_D}{dw_d} = \beta\frac{d\psi_s}{dw_d} - \frac{1}{\mathcal{E}_s}\frac{d\mathcal{E}_s}{dw_d} \tag{2.61}$$

From the relation $C_{ox}(V_G - V_{FB} - V_B - \psi_s) = \epsilon_{si}\mathcal{E}_s$, one has

$$\frac{dV_G}{dw_d} = \frac{\epsilon_{si}}{C_{ox}}\frac{d\mathcal{E}_s}{dw_d} + \frac{d\psi_s}{dw_d} \tag{2.62}$$

To obtain the expression for $\frac{d\psi_s}{dw_d}$ and $\frac{d\mathcal{E}_s}{dw_d}$, we have to solve the one-dimensional Poisson's equation in the channel and the depletion region.

$$\frac{d^2\psi}{dx^2} = \frac{q}{\epsilon_{si}}N(x) \tag{2.63}$$

Integrating Eq. (2.63) from x to w_d,

$$\frac{d\psi}{dx} = \left(\frac{d\psi}{dx}\right)_{x=w_d} - \frac{q}{\epsilon_{si}}\int_x^{w_d} dx_0 N(x_0) \tag{2.64}$$

Integrating Eq. (2.64) from x to w_d,

$$\psi(x) = \psi(w_d) - (w_d - x)\left(\frac{d\psi}{dx}\right)_{x=w_d} - \frac{q}{\epsilon_{si}}\int_x^{w_d} dx_1(x - x_1)N(x_1) \tag{2.65}$$

From Eq. (2.64) using boundary condition $\left(\frac{d\psi}{dx}\right)_{x=w_d} = 0$, one has

$$\mathcal{E}_s \equiv -\left(\frac{d\psi}{dx}\right)_{x=0} = \frac{q}{\epsilon_{si}}\int_0^{w_d} dx N(x) \tag{2.66}$$

Therefore,

$$\frac{d\mathcal{E}_s}{dw_d} = \frac{q}{\epsilon_{si}}N(w_d) \tag{2.67}$$

From Eq. (2.65), using boundary condition $\psi(w_d) = 0$ and $\left(\frac{d\psi}{dx}\right)_{x=w_d} = 0$, one has

$$\psi_s \equiv \psi(0) = \frac{q}{\epsilon_{si}} \int_0^{w_d} dx \cdot xN(x) \tag{2.68}$$

Thus,

$$\frac{d\psi_s}{dw_d} = \frac{q}{\epsilon_{si}} w_d N(w_d) \tag{2.69}$$

Substituting Eq. (2.69) and (2.67) into Eq. (2.61) and (2.62), then latter two into Eq. (2.60), one has

$$\frac{d\ln I_D}{dV_G} = \frac{\beta\frac{q}{\epsilon_{si}} w_d N(w_d) - \frac{1}{\mathcal{E}_s}\frac{q}{\epsilon_{si}} N(w_d)}{\frac{\epsilon_{si}}{C_{ox}}\frac{q}{\epsilon_{si}} N(w_d) + w_d \frac{q}{\epsilon_{si}} N(w_d)} = \frac{\beta w_d - \frac{1}{\mathcal{E}_s}}{\frac{\epsilon_{si}}{C_{ox}} + w_d} \tag{2.70}$$

Thus, the subthreshold gate swing

$$S = \left(\frac{\ln 10}{\beta}\right) \frac{1 + \frac{C_D}{C_{ox}}}{1 - \frac{t_{ch}}{w_d}} \tag{2.71}$$

where w_d, t_{ch} and C_D are all functions of the doping profile.

Since channel implantation shifts the threshold voltage of a device, comparing the subthreshold gate swing of devices with different channel implants at fixed values of gate bias makes no sense; they have to be compared at the same current level instead. Fig. 2–13 and 2–14 shows how the subthreshold gate swing varies with the implant energy with implant dose and substrate bias as parameters, respectively. The following parameters are used in the calculation: $t_{ox} = 350\mathring{A}$, $N_A = 7.5e15cm^{-3}$, $W/L = 10$, $V_D = 0.1V$, drain current $I_D = 1nA$. For Fig. 2–13, $V_B = 0$. For Fig. 2–14, the implantation dose was $8e11cm^{-2}$.

2.4.3 Models for Short-Channel MOSFETs

So far, the subthreshold behaviour of long-channel MOSFETs with uniform and nonuniform doping of the substrate has been discussed. As VLSI technology develops, the dimensions of MOSFETs decrease continually. Some undesirable phenomena arise as a result of the short channel length of a MOSFET. For example, the shift of the threshold voltage and the rising of the subthreshold current and gate swing. The channel of a MOSFET is considered short when the channel length is comparable with the source and the drain depletion depth. Brews *et al.*[62] proposed an empirical formula,

$$L_{min} = 0.4\left[r_j t_{ox}(W_S + W_D)^2\right]^{\frac{1}{3}} \tag{2.72}$$

where r_j is the junction depth. W_S and W_D are the source and drain depletion depth, respectively. Their expressions can be found in page 35.

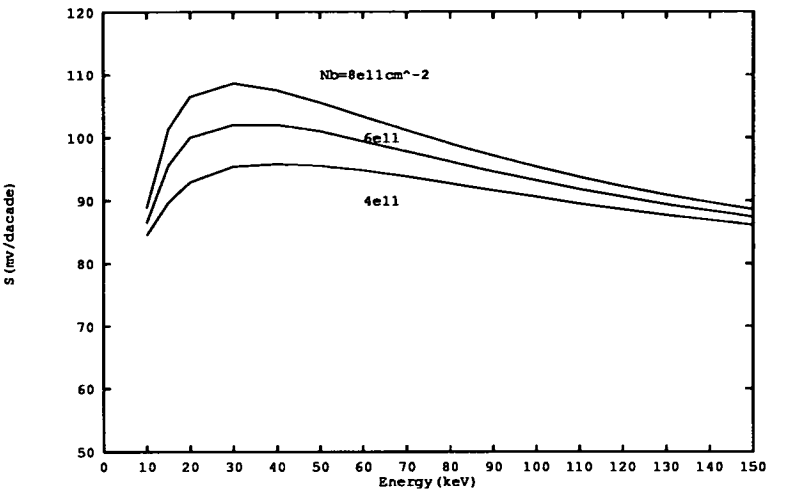


Figure 2–13: Subthreshold gate swing vs. implant energy with implant dose as parameter

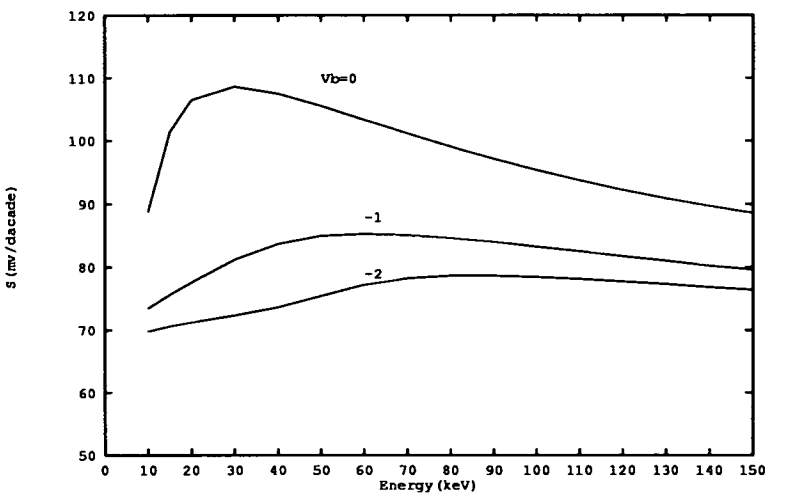


Figure 2–14: Subthreshold gate swing vs. implant energy with substrate bias as parameter

where L_{min} is the minimum channel length for which long-channel subthreshold behaviour can be observed. For short-channel MOSFETs, the subthreshold behaviour is quite different from that of their long-channel counterparts due to the two-dimensional potential distribution in the depletion region. So the one dimensional equations used for long-channel devices no longer hold and two-dimensional equations have to be adopted.

One of the early attempts to find a short-channel subthreshold model was made by Troutman and Fortino [63]. They gave a semi-empirical model based on the numerical result and concluded that the increase of the subthreshold drain current when the channel length decreases is due to drain-induced surface potential barrier lowering. That is

$$I_D = WL_B \frac{qDn_i}{L[2\beta(b\psi_B - 1 - V_B)]^{\frac{1}{2}}} \exp[\beta(b-1)\psi_B][1 - \exp(-\beta V_D)] \qquad (2.73)$$

where $b\psi_B \equiv \psi_s$, b is a band bending parameter. For a short-channel device,

$$b\psi_B = b_{LC}\psi_B + P_r + P_e V_D \qquad (2.74)$$

This is an empirical formula, where b_{LC} is the band bending parameter for a long-channel MOSFET. P_r and P_e are fitting parameters.

There are two groups of models of the threshold voltage and the subthreshold behaviour for short-channel MOSFETs, that is, charge sharing models and two-dimensional analytical models. Charge sharing models will be discussed first. To distinguish from the narrow-channel effect, a wide channel width is assumed.

Due to the two-dimensional potential distribution, the electric potential lines which terminate in charges in the depletion region not only originate from the gate, but also from the drain and the source. That is, the charges in the depletion region are controlled by the gate, the drain and the source in different degrees. See Fig. 2–15. Thus, the depletion region in a semiconductor can be divided into three areas [64,65].

(I) gate controlled region,

(II) source depletion region,

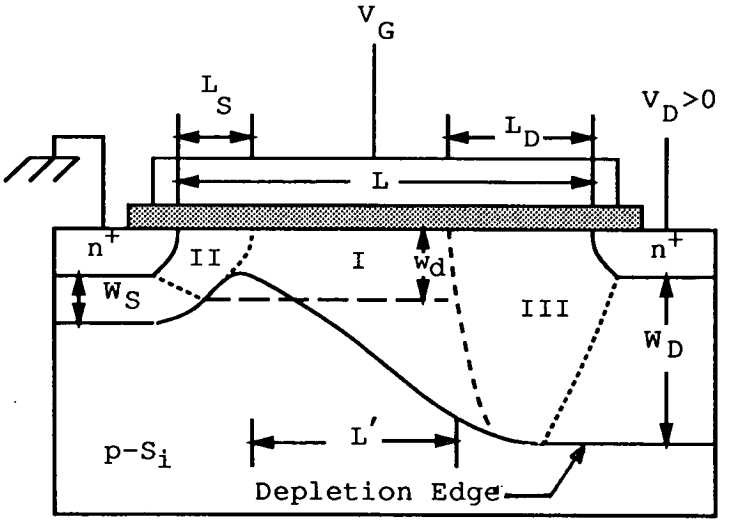


Figure 2–15: Charge sharing model

(III) drain depletion region.

The gate voltage, V_G, can only control charges in area (I). Using the charge conservation concept, one has

$$C_{ox}(V_G - V_{FB} - \psi_s) = Q_{BI} \tag{2.75}$$

where Q_{BI} is the charge density per unit area in area (I).

That is

$$C_{ox}(V_G - V_{FB} - \psi_s) = qN_A w_d \frac{1}{2}\left(1 + \frac{L - W_D - W_S}{L - L_S - L_D}\right) \tag{2.76}$$

where $W_D = \sqrt{\frac{2\epsilon_{si}}{qN_A}(V_D + V_{bi} - V_B)}$, $W_S = \sqrt{\frac{2\epsilon_{si}}{qN_A}(V_{bi} - V_B)}$,
$L_D = \sqrt{\frac{2\epsilon_{si}}{qN_A}(V_D + V_{bi} - \psi_s)}$, $L_S = \sqrt{\frac{2\epsilon_{si}}{qN_A}(V_{bi} - \psi_s)}$. V_{bi} is the built-in voltage of the junction.

The subthreshold current is given by [66]

$$I_D = \frac{q\mu_n L_B}{\sqrt{2}\beta} \frac{W}{L - L_S - L_D} \frac{n_i^2}{N_A} \frac{1}{\sqrt{\beta\psi_s}} e^{\beta\psi_s}(1 - e^{-\beta V_D})e^{\beta V_B} \tag{2.77}$$

From above expressions, one can find that when the channel length L decreases or the drain voltage V_D increases, the surface potential ψ_s increases. Thus the subthreshold current I_D increases as the channel length L decreases or the drain voltage V_D increases for a short-channel MOSFET.

Because the boundaries between regions (I), (II) and (III) in Fig. 2–15 is somewhat arbitrary, the accuracy of models of this kind is limited. To be more accurate, it is necessary to have two-dimensional analytical models which solve the two-dimensional Poisson's equation analytically to obtain the potential distribution in the depletion region, then use this distribution to calculate the drain current.

In 1979, Toyabe and Asia solved a quasi-two-dimensional Poisson's equation analytically for the surface potential of a short-channel MOSFET based on the results of a numerical analysis [67]. They assumed that the potential distribution normal to the oxide-semiconductor interface is $\psi(x) = a_0 + a_1 x + a_2 x^2 + a_3 x^3$ and the depletion depth w_d is constant along the channel. The effect of the source and drain junctions was not considered. The result is that the surface potential ψ_s has a minimum ψ_{smin} at y_{min} ($0 < y_{min} \leq L/2$). $\psi_s - \psi_{smin}$ is an exponential function of y (distance from source end) and the threshold voltage, V_T, also changes exponentially with the channel length L. That is

$$V_T = V_{FB} + \psi_{smin} + \gamma\sqrt{\psi_{smin} + V_B}\left(1 - \eta_0 e^{-\frac{L}{l_0}}\right) \tag{2.78}$$

where ψ_{smin} is the minimum surface potential when the gate voltage $V_G = V_T$. The body factor $\gamma = \frac{\sqrt{2\epsilon_{si} q N_A}}{C_{ox}}$.

$$\eta_0 = \frac{\epsilon_{ox}}{\epsilon_{si}} \frac{\sqrt{(V_D + V_{bi} - \psi_{smin})(V_{bi} - \psi_{smin})}}{\psi_{smin} + V_B} \left(\frac{w_d}{t_{ox}} + \frac{3}{2}\frac{\epsilon_{si}}{\epsilon_{ox}}\right) \tag{2.79}$$

and the characteristic length

$$l_0 = w_d \left(\frac{3}{2} + \frac{\epsilon_{ox}}{\epsilon_{si}}\frac{w_d}{t_{ox}}\right)^{-\frac{1}{2}} \tag{2.80}$$

Ratnakumar and Meindl [68], Poole and Kwong [69], Pfiester and Meindl [70] and Kendall and Boothroyd [71] solved the two dimensional Poisson's equation analytically. They converted Poisson's equation into the Laplace equation, then used the variable separation technique to solve the Laplace equation. Thus they all had expressions which are the sum of an infinite series for the potential distribution. That is

$$\psi(x, y) = \sum_{n=0}^{\infty} \frac{f(\gamma_n x)}{\sinh(\gamma_n L)} [C_n \sinh \gamma_n (L - y) + D_n \sinh \gamma_n y] + \psi_L \tag{2.81}$$

where γ_n is a set of eigenvalues which arises from solving the Laplace equation. The expressions of function $f(\gamma_n x)$ and coefficients C_n, D_n depend on boundary conditions. ψ_L is the solution of Poisson's equation for long-channel devices. They predicted the exponential dependence of ΔV_T, the shift of the threshold voltage, on the channel length L, instead of the $1/L$ dependence predicted by charge-sharing models[64,66,55].

Pimbley and Meindl [72] used the variational method to obtain an approximate solution of the two-dimensional Poisson's equation. Their potential distribution is an exponential function of y, that is

$$\begin{aligned}\psi(x,y) \approx\ & \psi_L(x) + [h(x,V_{bi}) - \psi_L(x)]\exp[-\Gamma(V_{bi} - V_B)y] \\ & +[h(x,V_{bi}+V_D) - \psi_L(x)]\exp[-\Gamma(V_{bi}+V_D-V_B)(L-y)] \quad (2.82)\end{aligned}$$

where $h(x,V_{bi}) = \psi(x,0)$, $h(x,V_{bi}+V_D) = \psi(x,L)$.

Among the above works, Ratnakumar and Meindl assumed infinite source and drain junction depth and a constant surface potential along the channel. Poole and Kwong used infinite source and drain junction depth as well, which overestimate the short-channel effect. Pfiester and Meindl and Pimbley and Meindl used a rectangular junction with finite depth, which still overestimates the short-channel effect. Kendall and Boothroyd in [71] considered implanted MOSFETs with parabolic boundary conditions at the source and drain ends.

Greenfield and Dutton [40] developed a technique to calculate the low-level drain current of a short-channel device as long as one knows the two-dimensional potential distribution in the depletion region. That is

$$I_D = -qD_nW\frac{t_{ch}}{L_{eff}}\frac{n_i^2}{N_A}\exp(\beta\psi_{smin})[1-\exp(-\beta V_D)] \quad (2.83)$$

where the effective channel thickness

$$t_{ch} = \int_0^{w_d}\exp[-\beta(\psi(x,y_{min}) - \psi_{smin})]dx \approx \frac{1}{\beta\mathcal{E}_s} \quad (2.84)$$

The effective channel length

$$L_{eff} = \int_0^{L}\exp[-\beta(\psi_s - \psi_{smin})]dy \quad (2.85)$$

From the above, one can conclude that the short-channel effect is caused by the drain-induced field penetrating into the area underneath the gate (1) to reduce the effective channel length (2) to raise the surface potential and thus reduce the potential barrier in the channel.

Poole and Kwong [73] used their solution [69] of Poisson's equation to calculate the subthreshold current in the same manner as mentioned above. They assumed infinite source and drain junction depths which overestimate the short-channel effect. Their model predicted that the subthreshold current I_D increases when the channel length L reduces or the drain voltage rises. This is in agreement with experimental results. It also predicted that the subthreshold gate swing S *decreases* when the channel length L reduces. This disagrees with experimental results. Lin and Wu [74] solved the two-dimensional Poisson's equation by using the Green's function method with a cylindrical source and drain junction. The subthreshold current is obtained using the same method as above. Although their model was supposed to include implanted devices, their boundary conditions at the source and drain ends were derived for uniformly doped devices only. Since the subthreshold gate swing is the most important parameter to describe the subthreshold behaviour, we derive it in Chapter 3 for short-channel MOSFETs.

2.4.4 Models for Narrow-Channel MOSFETs

Having discussed the subthreshold short-channel effect of MOSFETs, another small geometry effect, namely the narrow-channel effect, will be discussed in this subsection. The channel of a MOSFET is considered narrow if the channel width is comparable with the depletion depth. Unlike the short-channel effect, the narrow-channel effect is more complicated. For non-recessed or semi-recessed (LOCOS) oxide isolation structures, the threshold voltage increases and the subthreshold current drops but the subthreshold gate swing rises when the channel width decreases. However, for a fully recessed oxide isolation structure, the threshold voltage decreases and the subthreshold current increases as the channel width decreases; this is called the inverse-narrow-channel effect.

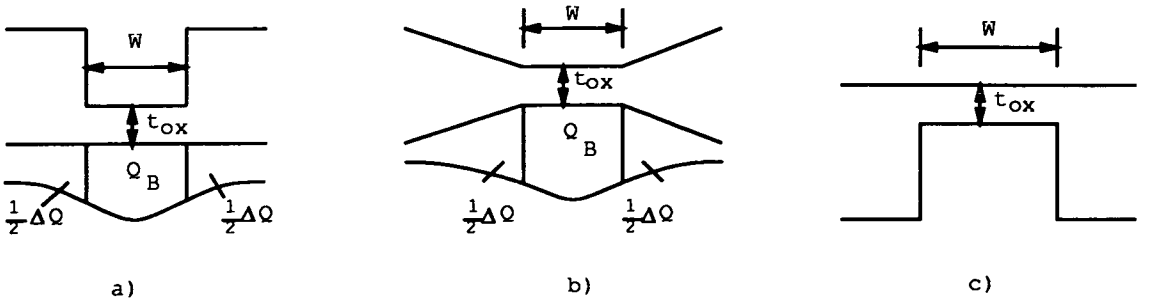


Figure 2–16: Width cross-section of MOSFETs: a) non-recessed b) semi-recessed c) fully-recessed oxide isolation structure

The narrow-channel effect of nonrecessed or semi-recessed oxide isolation structure will be discussed first. The narrow-channel threshold voltage increase has been analyzed by Jeppson for uniform oxide [75], Bandali and Lo for a semi-recessed tapered oxide (bird's beak) [22], Kotecha and De La Moneda *et al.* for a non-recessed tapered oxide [23], Merckel [76] and Akers [24] for a non-recessed stepped oxide, etc. They all developed their models by using the concept that extra charges, ΔQ, are induced under the field oxide because the fringe field induced by the gate bias extends into the isolation region. Fig. 2–16 shows the width cross-section of a narrow-channel device.

$$\Delta V_T = V_T - V_{T0} = \frac{\Delta Q}{C_{ox}} \tag{2.86}$$

It was predicted that the threshold voltage shift $\Delta V_T \propto \frac{1}{W}$. V_{T0} is the threshold voltage of a wide channel device. But the geometry division to calculate ΔQ is arbitrary, thus their accuracy is not very good.

Kroell and Ackermann [77], Noble and Cottrell [78], Ji and Sah [79,80] and Chung and Sah [81,82] etc. solved the two-dimensional Poisson's equation numerically. Numerical results show that potential is not constant along the channel width. The surface potential decreases towards the edge of the channel.

Chung and Sah calculated the threshold voltage and the subthreshold current of a narrow-channel device numerically. They proposed an empirical model for the

subthreshold slope based on their numerical result, that is

$$n = Ae - BW + C \tag{2.87}$$

where the three constants A, B, C are to be determined from three n values at three channel widths of numerical results. Although numerical models provide physical insight into the narrow-channel effect, they are not suitable for circuit simulation purposes.

Akers and Beguwala *et al.* developed an analytical expression of threshold voltage by geometry approximation for semi-recessed tapered oxide including effects of field oxide and field doping encroachment [83]. They have

$$V_T = V_{FB} + 2\psi_B + \frac{Q_B + 2Q_f}{C_{ox} + 2C_f} \tag{2.88}$$

where Q_f is the extra charge under one side of the field oxide, C_f is the field oxide capacitance of one side. In this section, Q_B is the charge due to ionized impurity in the depletion region and C_{ox} is the capacitance of the gate oxide, instead of charge per unit area and capacitance per unit area used elsewhere. Cheng and Lai [84] obtained the potential distribution for a non-recessed stepped oxide by solving the two-dimensional potential problem for the width cross section by means of Fourier transformation. V_T is taken as the gate voltage at which the surface potential under the middle of the gate equals $2\psi_B - V_B$. Li and Hong *et al.* [85] obtained an expression for threshold voltage for a semi-recessed stepped oxide structure by geometry approximation to obtain Q_f and solving Laplace's equation in the field oxide using conformal transformation. They apply Gauss's law directly, i.e.

$$Q_B + 2Q_f = \Psi_{gat} + 2\Psi_{sw} \tag{2.89}$$

where the gate electric flux $\Psi_{gat} = -C_{ox}(V_G - \psi_s)W$, Ψ_{sw} is the sidewall electric flux, which is determined from the potential distribution in the field oxide region. Their result predicts that the threshold voltage shift $\Delta V_T \propto \frac{1}{W}$.

Now, the fully recessed oxide structure should be considered. Shigyo, Konaka and Dang[86] used a three-dimensional numerical model to simulate the fully recessed oxide structure. Sugino and Akers [87] also used a numerical model to

obtain the subthreshold current for a fully-recessed oxide structure. They found that the surface potential goes up towards the channel edge. They compared the subthreshold current of non-recessed, semi-recessed and fully-recessed oxide structures. The result is that the non-recessed oxide has the smallest subthreshold current, the fully-recessed oxide has the worst subthreshold characterization and the semi-recessed oxide is in between.

Akers [25], Hong and Cheng[88], Li and Hong[85] and Chung and Li[89] etc. used a geometric approximation and conformal mapping methods to obtain the threshold voltage for a fully-recessed narrow-channel MOSFET. They either use Eq. (2.88), where C_f is obtained by conformal mapping, or they use Eq. (2.89). Hsueh and Sanchez[90] solved the two-dimensional Poisson's equation on the width cross-section. They used

$$V_T = V_{FB} + 2\psi_B + \frac{Q}{C_{ox}} \tag{2.90}$$

$$Q = \epsilon_{si}\mathcal{E}_s = -\epsilon_{si}\frac{\partial\psi}{\partial x}(0, \frac{W}{2}) \tag{2.91}$$

Their result shows that the narrow-channel effect of threshold voltage depends exponentially on the channel width.

It is obvious from above review that researchers are still concentrating on the narrow-channel effect of the threshold voltage. Except for their embodiment in numerical models, analytical subthreshold models have not been considered actively.

2.5 Models for Small Geometry MOSFETs

For a small geometry device with a short- and narrow-channel, consideration of either short-channel or narrow-channel effect is not enough. An expression which includes both of these effects and also their interactive coupling is needed. Wang [91] proposed a small geometry model which ignores the coupling between the short-channel and narrow-channel effect. He had

$$V_T = V_{T0} - \Delta V_{TL} + \Delta V_{TW} \tag{2.92}$$

where V_{T0} is the threshold voltage of a large device, ΔV_{TL} and ΔV_{TW} are threshold voltage shifts caused by short-channel effect and narrow-channel effect, respectively.

By using simple geometry approximation, Jeppson [75], Merckel [76] and Akers [92] etc. developed a small geometry model for threshold voltage. The models of Merckel and Akers have

$$V_T = V_{FB} + 2\psi_B + \gamma_M K(V_B + 2\psi_B)^{\frac{1}{2}} \tag{2.93}$$

where γ_M is a factor which takes into account the modification of the body effect, due to device dimensions.

$$\gamma_M = 1 + \alpha\frac{w_d}{W} + \frac{r_j}{L}\left(1 + \frac{3}{2}\alpha\frac{w_d}{W}\right)\left[1 - \left(1 + \frac{2w_d}{r_j}\right)^{\frac{1}{2}}\right] \tag{2.94}$$

where α is a fitting parameter.

Due to the arbitrary nature of the geometry approximation, those models above are not very accurate. However, because it is very difficult to solve the three-dimensional poisson equation analytically, an analytical model for small geometry MOSFETs does not exist yet.

2.6 Models for Circuit Simulation

A simple and compact model is necessary for efficient calculation in circuit simulations. As far as the subthreshold region is concerned, the SPICE2 level 1 model [33, 34] and the CASMOS model [37] assume that the drain current is zero. SPICE2 level 3 model [35] uses the parameter N_{sf} , surface state density, to describe the subthreshold slope, i.e.

$$I_D = I_0 \exp\left[\frac{\beta}{n}(V_G - V_{on})\right] \tag{2.95}$$

$$n = 1 + \frac{C_D}{C_{ox}} + \frac{qN_{sf}}{C_{ox}} \tag{2.96}$$

where n is the slope parameter. N_{sf}, I_0 and V_{on} are to be extracted from experimental data or device simulator results. However, for a real device fabricated by

present semiconductor technology, the surface state density is too low to affect the subthreshold gate swing significantly.

A subthreshold model proposed by Yang and Chatterjee [93] for SPICE has the following feature:

$$I_D = \frac{\sqrt{2}\mu_n \epsilon_{si} W}{\beta^2 L_B L} e^{\beta(V_B+\psi_s-2\psi_B)}(1 - e^{-\beta V_D}) \tag{2.97}$$

and

$$\psi_s = V_G - V_B - V_{FB} + \frac{\gamma_T^2}{2}\left\{1 - \left[1 + \frac{4}{\gamma_T^2}(V_G - V_{FB} - V_B)\right]^{\frac{1}{2}}\right\} \tag{2.98}$$

where γ_T is the effective body factor for a short-channel transistor.

$$\gamma_T = \gamma - \delta(\sqrt{2\psi_B + V_D - V_B} - \sqrt{2\psi_B}) \tag{2.99}$$

where δ is the drain effect term and represents the drain induced barrier lowering. It is clear from above equations that the effective body factor γ_T decreases as the drain voltage V_D increases. Thus surface potential ψ_s decreases as V_D increases. The result of this is that the drain current I_D decreases as V_D increases. This disagrees with experimental and theoretical results.

To include the narrow-width effect,

$$\gamma = \gamma_0 + \frac{\gamma_W}{W} \tag{2.100}$$

The subthreshold model of Grotjohn and Hoefflinger [94] for a long-channel MOSFET is

$$I_D = \frac{\mu W C_{ox}}{LA}\left(\frac{1}{\beta}\right)^2 \exp[A\beta(V_G - V_{T0})][1 - \exp(-\beta V_D)] \tag{2.101}$$

where

$$\frac{1}{A} = \frac{C_{ox} + C_D + C_{FS}}{C_{ox}} \tag{2.102}$$

C_{FS} is the fast surface state capacitance,

$$C_D = \frac{\gamma C_{ox}}{2\sqrt{\psi_s - V_B}} \tag{2.103}$$

The body factor

$$\gamma = \sqrt{\frac{2\epsilon_{si} q N_{eff}}{C_{ox}^2}} \tag{2.104}$$

where N_{eff} is the effective doping concentration. For a short-channel device,

$$I_D = \frac{I_0 L}{L - \Delta L_D} \tag{2.105}$$

$$\Delta L_D = K\sqrt{V_D + V_{bi}} - K\sqrt{V_{bi}} \tag{2.106}$$

The channel length modulation coefficient

$$K = \sqrt{\frac{2\epsilon_{si}}{qN_{eff}}} \tag{2.107}$$

$$I_0 = \mu \frac{W}{L}\frac{1}{A}C_{ox}\left(\frac{1}{\beta}\right)^2 \exp\{\beta[A(V_G - V_{T0}) + BV_D]\}[1 - \exp(-\beta V_D)] \tag{2.108}$$

The drain voltage dependence parameter

$$B = \begin{cases} \frac{\epsilon_{si} t_{ox}}{\eta \epsilon_{ox}}\left(\frac{1}{L} - \frac{1}{L^*}\right) & \text{for } L < L^* \\ 0 & \text{for } L > L^* \end{cases} \tag{2.109}$$

where L^* is the longest channel length with drain-induced barrier lowering present.

In Wright's model [36] (including the short-channel effect), the subthreshold current

$$I_D = \frac{2\mu_s C_{ox}}{(1 + F_B)}\left(\frac{W}{L}\right)\left(\frac{n}{\beta}\right)^2 \exp\left[\frac{\beta}{n}(V_G - V_T)\right] \tag{2.110}$$

and the subthreshold slope coefficient

$$n = s\left(1 + \frac{C_D}{C_{ox}}\right) \tag{2.111}$$

where s is an adjustable coefficient used to fit the value of n to measured characteristics. $F_B = \frac{\gamma}{4(\psi_s - V_B)^{1/2}}$. Later Wright proposed a model for MOSFETs with an implanted channel [95],

$$I_D = 2\mu_0 C_{ox}\frac{W}{L}\left(\frac{1}{\beta}\right)^2 m^2 \exp\left[\frac{\beta}{n}(V_G - V_T)\right][1 - \exp(-\beta V_D)] \tag{2.112}$$

m is a parameter used to adjust the magnitude of the subthreshold current. The subthreshold slope coefficient

$$n = 1 + \frac{C\varrho - \alpha_G(V_G - V_T) - \alpha_D V_D}{1 - \sigma V_B} \tag{2.113}$$

This is an empirical expression to include the effect of the nonuniformly doped channel. where ϱ, α_G, α_D and σ are empirical fitting parameters.

Klaassen proposed the following subthreshold model for MOSFETs in [96].

$$I_D = \frac{W}{L} I_0 \exp \frac{\beta(V_G - V_T)}{m} \tag{2.114}$$

where I_0 is a current constant. The slope factor

$$m = m_0 + \frac{1}{2}\gamma(1.5\psi_B - V_B)^{-\frac{1}{2}} \tag{2.115}$$

$$\gamma = \gamma_\infty - \frac{\gamma_L}{L} + \frac{\gamma_W}{W} \tag{2.116}$$

If considering the effect of the substrate bias V_B on the slope factor, one has [38]

$$I_D = \frac{I_0}{(1 - V_B/\psi_s)^{1/2}} \exp\left[\frac{\beta(V_G - V_T)}{M}\right] \tag{2.117}$$

$$M = 1 + \frac{m}{(\psi_s - V_B)^{1/2}} \tag{2.118}$$

Sheu *et al.* [97] proposed a semi-empirical model BSIM (Berkeley Short-channel IGFET Model for MOS transistor). They have

$$I_D = \mu_0 C_{ox} \frac{W}{L} \left(\frac{1}{\beta}\right)^2 e^{1.8} e^{\beta(V_G - V_T)/n}(1 - e^{-\beta V_D}) \tag{2.119}$$

The subthreshold slope coefficient

$$n = n_0 + n_A V_B + n_D V_D \tag{2.120}$$

and all size dependence parameters (P_i) (n_0, n_A, n_D here) subject to relationship

$$P_i = P_{0i} + \frac{P_{Li}}{L} + \frac{P_{Wi}}{W} \tag{2.121}$$

P_{0i} is P_i of a long- and wide- channel device. P_{Li} and P_{Wi} are fitting parameters.

Chung *et al.* [98] proposed a subthreshold model for small geometry MOSFETs. For short-channel devices,

$$I_D = \alpha \mu_n \frac{W}{L} C_{ox} \left(\frac{1}{\beta}\right)^2 e^{m(V_G - V_T)}(1 - e^{-\beta V_D}) \tag{2.122}$$

where α is an empirical parameter. m is the subthreshold slope. For a narrow-gate device,

$$I_D = \frac{\mu_n}{L} W'_{CE} C_{ox} \left(\frac{1}{\beta}\right)^2 e^{m(V_G - V_T)}(1 - e^{-\beta V_D}) \tag{2.123}$$

where W'_{CE} is the effective channel width.

Chung [99] proposed a model for narrow-channel devices.

$$I_D = I_0 \frac{W}{L} e^{m(V_G - V_{on})}(1 - e^{-\beta V_D}) \tag{2.124}$$

where $I_0 = \mu_0 \alpha C_{ox} \frac{1}{\beta^2}$, m is subthreshold slope, α is a fitting parameter.

$$m = m_0(AW^{-n} + B)(1 + \lambda\sqrt{-V_B}) \tag{2.125}$$

where m_0 is the subthreshold slope of a wide channel device at zero substrate bias. A, n and B are to be extracted from three m values at three channel width at zero substrate bias. λ is to be extracted from m vs. $\sqrt{-V_B}$ relation for a wide-channel device.

Several models above used the formula $n = 1 + \frac{C_D}{C_{ox}} = 1 + \frac{\gamma}{2}(\psi_s - V_B)^{-\frac{1}{2}}$ for the subthreshold slope coefficient. The body factor γ decreases when the channel length L decreases or the drain voltage V_D increases. If one uses the above formula, one will find the subthreshold slope coefficient n decreases when L decreases or V_D increases. This is against experimental observation.

A compact subthreshold model for circuit simulation will be proposed in Section 7.3. It is based on the theoretical results in Chapter 3 and experimental observation in Chapter 6 and 7.

Chapter 3

Two-dimensional Analytical Subthreshold and Punchthrough Model for Short-Channel MOSFETs

3.1 Introduction

As geometry sizes of MOSFETs shrink, the so-called short-channel effects give more cause for concern. One of the more serious small-geometry effects is the increase of subthreshold current and the subthreshold gate swing. As the channel length is reduced, the influence of the drain and source-induced lateral field becomes more profound, which results in potential barrier lowering. Consequently, it leads to a significant rise in subthreshold leakage or may even prevent the turn-off of a MOSFET. Since this current does not obey the scaling rules, it is one of the major limitations to scaling of MOSFETs.

In the literature about the subthreshold behaviour for short-channel MOSFETs, a satisfactory model does not yet exist. In Poole and Kwong's subthreshold current model [73] for short-channel MOSFETs with a uniformly doped channel, they assumed infinite source and drain junction depth which overestimates the short-channel effect. Their model predicted that the subthreshold gate swing S *decreases* when the channel length L reduces. This is against experimental re-

sults. Lin and Wu [74] solved the two-dimensional Poisson's equation by using the Green's function method with a cylindrical source and drain junction. Although their model was supposed to include implanted devices, their boundary conditions at the source and drain ends were derived for uniformly doped devices only. The subthreshold gate swing is a very important parameter for device design consideration. However, no analytical expression for the subthreshold gate swing for short-channel devices exists yet.

In Section 3.2, we present a two-dimensional analytical subthreshold model based on the analytical solution of Poisson's equation. Cylindrical source and drain junctions are used to derive the boundary conditions at the source and drain ends and the effect of the non-uniform doping profile on the boundary conditions has been taken into account. It gives an analytical expression for the subthreshold current and gate swing for a short-channel MOS device with an arbitrary doping profile.

Another short-channel effect is the higher punchthrough current for shorter-channel devices. Short-channel MOSFETs are affected by the drain-induced lateral field which leads to lowering of the potential barrier height at the surface and in the bulk of the semiconductor. This effect causes the punchthrough current and reduction of the punchthough voltage. It leads to a significant rise in subthreshold leakage or even prevents the turn-off of a MOSFET. Since punchthrough current does not obey the scaling rules, it is another major limitation to scaling of MOSFETs. Although a lot of work has been reported on punchthrough, there is not yet a satisfactory model.

There is some controversy about where punchthrough occurs first. In [100,101, 102,103,104,105], it was believed that punchthrough happened in the bulk. However, in [106,27], it was considered that punchthrough occurred at the surface. Based on a quasi-two-dimensional analysis and two-dimensional numerical simulation, Fu in [107] argued that the sign of the effective gate voltage, $V_G - V_{FB}$, decides whether punchthrough occurs in the surface or in the bulk for a subthreshold-biased MOS device. But her result was only obtained for a uniformly doped device. Due to the complexity of the problem, people rarely consider both the

surface and the bulk component of punchthrough together. They either only deal with surface punchthrough[73,72], or only consider bulk punchthrough[108]. Skotnicki et al.[109] gave an analytical model including both punchthrough components for a single-implanted device using a step profile approximation. An assumption of infinite depth of source and drain junctions was used. It also assumed that the saddle point (virtual cathode) in the bulk conducting path happens near $y = L/2$. This assumption indicates that this model is only valid under a small drain bias. A total of seven fitting parameters were needed.

In Section 3.3, we present a two-dimensional analytical punchthrough current model based on the analytical solution of Poisson's equation. It includes both surface and bulk components of the punchthrough current for a non-uniformly doped MOS device with an arbitrary doping profile and no fitting parameters are needed.

3.2 Subthreshold Model

3.2.1 Theory and Results

Solution of Two-Dimensional Poisson Equation

The rectangular region in which Poisson's equation is solved is indicated by the shadowed region in Fig. 3–1. The various geometric parameters and operating voltages are defined in it.

Solving the two-dimensional Poisson Equation with boundary conditions below

$$\frac{\partial \psi}{\partial x}(0,y) = -\frac{C_{ox}}{\epsilon_{si}}[V'_{GB} - \psi(0,y)] \tag{3.1}$$

$$\frac{\partial \psi}{\partial x}(w_d,y) = 0 \tag{3.2}$$

$$\psi(x,0) = \psi_S(x,0) \tag{3.3}$$

$$\psi(x,L) = \psi_D(x,L) \tag{3.4}$$

where

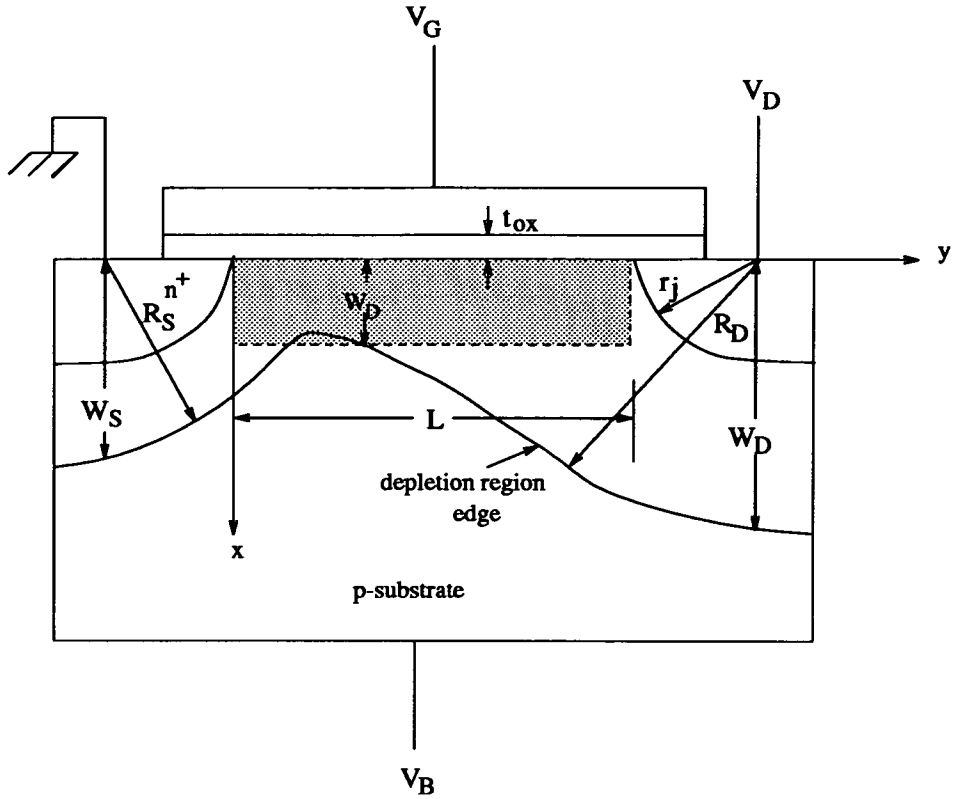


Figure 3–1: Schematic cross section of an nMOSFET

ψ is the electrostatic potential;

C_{ox} is the capacitance per unit area of the gate oxide layer, $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$;

ϵ_{si} and ϵ_{ox} are the permittivity of silicon and oxide, respectively;

$V'_{GB} = V_G - V_B - V_{FB}$;

w_d is the depletion region depth;

ψ_S and ψ_D are source and drain cylindrical junction induced potential respectively.

The solution is

$$\psi(x,y) = \psi_L(x) + V(x,y) \tag{3.5}$$

where

$$\psi_L(x) = V'_{GB} - \frac{q}{\epsilon_{si}}F(x) - \frac{q}{\epsilon_{si}}x[G(w_d) - G(x)] - \frac{q}{C_{ox}}G(w_d) \tag{3.6}$$

$$V(x,y) = \sum_{n=0}^{\infty} \frac{\cos k_n(w_d - x)}{u_n \sinh k_n L}[H_n \sinh k_n(L-y) + I_n \sinh k_n y] \tag{3.7}$$

$\psi_L(x)$ is a one-dimensional function, it has a similar form to the solution of Poisson's equation for a long-channel MOSFET. Actually, when the channel length $L \to \infty$, ψ_L becomes the same as the long-channel solution. $V(x,y)$ is the solution of Laplace equation, it represents the two-dimensional nature of the potential distribution. The detail of the solution is presented in Appendix C.

$N(x)$ is the doping profile;

$F(x) = \int_0^x x_1 N(x_1) dx_1$;

$G(x) = \int_0^x N(x_1) dx_1$.

and

$$k_n w_d = \arctan\left(\frac{C_{ox}}{\epsilon_{si} k_n}\right) + n\pi \ (n = 0, 1, 2, ...) \tag{3.8}$$

$$u_n = \frac{1}{2}\left(1 + \frac{\sin 2k_n w_d}{2k_n w_d}\right) \tag{3.9}$$

$$H_n = \frac{1}{w_d}\int_0^{w_d} V(x,0)\cos k_n(w_d - x)dx \tag{3.10}$$

$$I_n = \frac{1}{w_d}\int_0^{w_d} V(x,L)\cos k_n(w_d - x)dx \tag{3.11}$$

where $V(x,0) = \psi(x,0) - \psi_L(x)$, $V(L,x) = \psi(x,L) - \psi_L(x)$.

$$\psi_S(x,0) = \begin{cases} V_{bi} - V_B & x = 0 \\ V_{bi} - V_B - \frac{q}{\epsilon_{si}}\frac{r_j^2}{x_j^2}[\int_{x_j}^{x} x_0 N(x_0)\ln\frac{x_0}{x_j}dx_0 & \\ + \ln\frac{x_j}{x}\int_x^{x_S} x_0 N(x_0)dx_0] & 0 < x < W_S \\ 0 & x \geq W_S \end{cases} \tag{3.12}$$

$$\psi_D(x,L) = \begin{cases} V_{bi} + V_D - V_B & x = 0 \\ V_{bi} + V_D - V_B - \frac{q}{\epsilon_{si}}\frac{r_j^2}{x_j^2}[\int_{x_j}^{x} x_0 N(x_0)\ln\frac{x_0}{x_j}dx_0 & \\ + \ln\frac{x_j}{x}\int_x^{x_D} x_0 N(x_0)dx_0] & 0 < x < W_D \\ 0 & x \geq W_D \end{cases} \tag{3.13}$$

where $x_j = xr_j/\sqrt{x^2 + (r_j + y)^2}$, $x_S = xR_S/\sqrt{x^2 + (r_j + y)^2}$, $x_D = xR_D/\sqrt{x^2 + (r_j + y)^2}$. See Fig. 3–2 for reference.

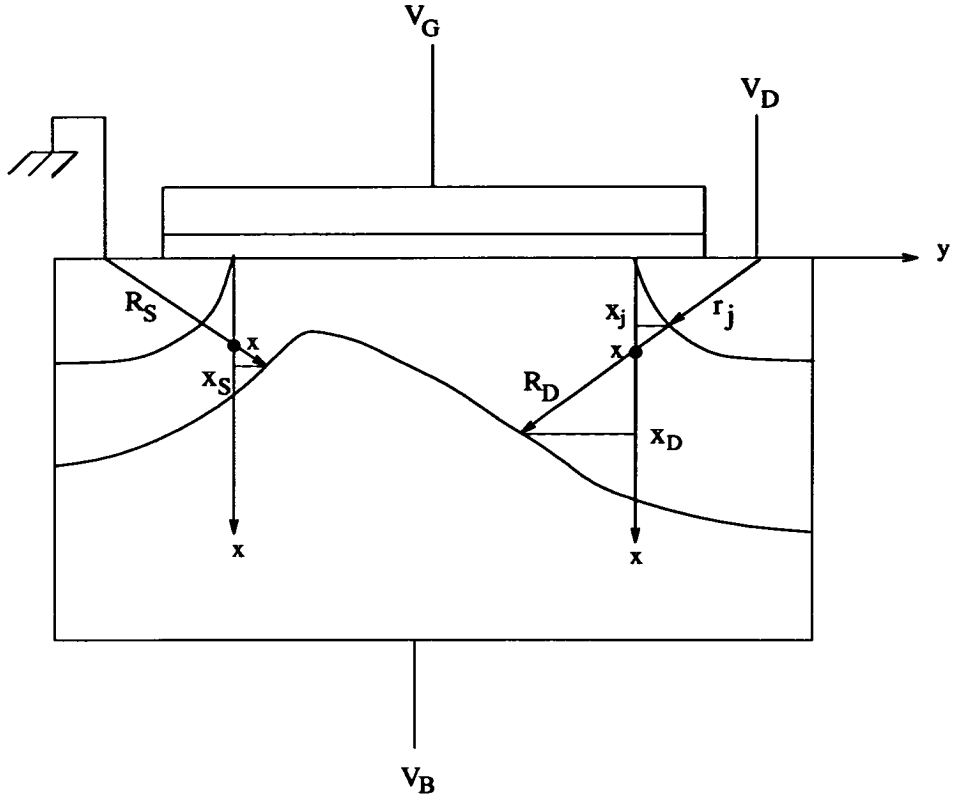


Figure 3–2: Schematic cross section of an nMOSFET

R_S, R_D satisfy

$$V_{bi} - V_B - \frac{q}{\epsilon_{si}} \frac{r_j^2}{x_j^2} \int_{x_j}^{x_S} x_0 N(x_0) \ln \frac{x_0}{x_j} dx_0 = 0 \tag{3.14}$$

$$V_{bi} + V_D - V_B - \frac{q}{\epsilon_{si}} \frac{r_j^2}{x_j^2} \int_{x_j}^{x_D} x_0 N(x_0) \ln \frac{x_0}{x_j} dx_0 = 0 \tag{3.15}$$

respectively. More details can be found in Appendix E.

The minimum potential along the surface, ψ_{smin} at $y = y_m$, is calculated using condition $\frac{\partial \psi}{\partial y}(0, y_m) = 0$. The depletion depth, w_d, is calculated by using condition $\psi(w_d, y_m) = \frac{1}{\beta} \ln \frac{N_A}{N(w_d)}$. For a short-channel device with a uniformly doped channel, its depletion depth may be written as

$$w_d = \sqrt{\frac{2\epsilon_{si}}{qN_A}[\psi_{smin} + V(w_d, y_m) - V(0, y_m)]} \tag{3.16}$$

Refer to Appendix B for more details. Since $V(w_d, y_m) - V(0, y_m) > 0$, it is obvious that w_d of a short-channel device is wider than that of a long-channel device with the same surface potential.

The subthreshold current[40]

$$I_D = qD_n \frac{Wt_{ch}}{L_{eff}} \left(\frac{n_i^2}{N_A} \right) \exp[\beta(\psi_{smin} + V_B)][1 - \exp(-\beta V_D)] \tag{3.17}$$

The effective channel thickness[40]

$$t_{ch} \approx \frac{1}{\beta \mathcal{E}_s} \tag{3.18}$$

The effective channel length

$$L_{eff} = \int_0^L \exp[-\beta(\psi_s - \psi_{smin})]dx \tag{3.19}$$

For a long-channel device, ψ_s is constant along the channel, thus $L_{eff} = L$.

For a short-channel device, ψ_s is not constant along the channel and it has a minimum ψ_{smin}, thus $L_{eff} < L$.

Poole and Kwong[73] only used the first term of the series in their potential expression to evaluate the effective channel length, which we found is inaccurate. To calculate the effective channel length for a very short-channel MOSFET, use a Taylor's expansion to the surface potential around the minimum point $\psi(0, y_m)$:

$$\begin{aligned} \psi(0,y) &= \psi_{smin} + \frac{\partial \psi}{\partial y}(0,y_m)(y-y_m) + \frac{\partial^2 \psi}{\partial y^2}(0,y_m)(y-y_m)^2 + \cdots \\ &= \psi_{smin} + \frac{\partial^2 \psi}{\partial y^2}(0,y_m)(y-y_m)^2 + \cdots \end{aligned} \tag{3.20}$$

and

$$\begin{aligned} L_{eff} &= \int_0^L \exp[-\beta(\psi(0,y) - \psi_{smin})]dy \\ &\approx \int_0^L \exp[-\beta \frac{\partial^2 \psi}{\partial y^2}(0,y_m)(y-y_m)^2]dy \\ &\approx \left(\frac{2\pi}{\beta \frac{\partial^2 \psi}{\partial y^2}(0,y_m)} \right)^{\frac{1}{2}} \end{aligned} \tag{3.21}$$

Eq. (3.21) is valid under condition that

$$\frac{\beta}{2} \frac{\partial^2 \psi}{\partial y^2}(0,y_m)(L-y_m)^2 > 1 \tag{3.22}$$

Otherwise, following approach is used[40].

$$L_{eff} = y_2 - y_1 \tag{3.23}$$

where y_1, y_2 satisfy $\psi(0,y_1) = \psi(0,y_2) = \psi_{smin} + \pi/4\beta$ and $y_1 < y_m < y_2$.

The subthreshold gate swing $S \equiv \frac{dV_G}{d(\log_{10} I_D)}$ is a very important parameter in describing the subthreshold behaviour. It indicates how much gate bias lowering is needed to reduce the current by one decade.

$$S = 1000\,(\ln 10)\frac{dV_G/dw_d}{d(\ln I_D)/dw_d}\ (\text{mV/decade}) \tag{3.24}$$

$$\begin{aligned}
\frac{d(\ln I_D)}{dw_d} &= \beta\frac{d\psi_{smin}}{dw_d} - \frac{1}{L_{eff}}\frac{dL_{eff}}{dw_d} - \frac{1}{\mathcal{E}_s}\frac{d\mathcal{E}_s}{dw_d} \\
&= \frac{q}{\epsilon_{si}}w_d N(w_d)\beta\left(1 - \frac{1}{\beta\mathcal{E}_s}\right) - \frac{1}{L_{eff}}\frac{dL_{eff}}{dw_d} \\
&\quad +\beta\left[\left(1 + \frac{1}{\beta\mathcal{E}_s}\frac{C_{ox}}{\epsilon_{si}}\right)\frac{d}{dw_d}V(0,y_m) - \frac{d}{dw_d}V(w_d,y_m)\right] \qquad (3.25) \\
\frac{dV_G}{dw_d} &= \frac{d\psi_{smin}}{dw_d} + \frac{\epsilon_{si}}{C_{ox}}\frac{d\mathcal{E}_s}{dw_d} \\
&= \frac{q}{\epsilon_{si}}w_d N(w_d) + \frac{q}{C_{ox}}N(w_d) - \frac{d}{dw_d}V(w_d,y_m) \qquad (3.26)
\end{aligned}$$

Therefore

$$S = 1000\left(\frac{\ln 10}{\beta}\right)\frac{1 + \frac{\epsilon_{si}}{w_d}\frac{1}{C_{ox}} - T_1}{1 - \frac{1}{\beta\mathcal{E}_s}\frac{1}{w_d} + T_2 - T_3} \tag{3.27}$$

where

$T_1 = \frac{1}{T}\frac{d}{dw_d}V(w_d,y_m)$,

$T_2 = \frac{1}{T}\left[\left(1 + \frac{1}{\beta\mathcal{E}_s}\frac{C_{ox}}{\epsilon_{si}}\right)\frac{d}{dw_d}V(0,y_m) - \frac{d}{dw_d}V(w_d,y_m)\right]$,

$T_3 = \frac{1}{T}\frac{1}{\beta L_{eff}}\frac{dL_{eff}}{dw_d}$,

$T = \frac{q}{\epsilon_{si}}w_d N(w_d)$.

Details about how to calculate S are presented in Appendix D.

When $L \to \infty$, $\frac{d}{dw_d}V(0,y_m) \to 0$, $\frac{d}{dw_d}V(w_d,y_m) \to 0$ and $\frac{1}{L_{eff}}\frac{dL_{eff}}{dw_d} \to 0$. So S reduces to its long-channel formula.

When the drain voltage V_D is small, we can assume that the potential minimum is near the middle of the channel, then using only the first term in the series $V(x,y_m)$ may be approximated as

$$V(x,y_m) = \frac{\cos k_0(w_d - x)}{u_0}(H_0 + I_0)\exp\left(-\frac{k_0 L}{2}\right) \tag{3.28}$$

Thus, $\frac{dV}{dw_d}(x, y_m) \propto \exp\left(-\frac{k_0 L}{2}\right)$. Compared with T_1, effects of T_2 and T_3 are second order. Thus $S - S_0 \propto \exp\left(-\frac{k_0 L}{2}\right)$. S_0 is the subthreshold gate swing for a long-channel device.

3.2.2 Verification and Discussion

A FORTRAN77 program has been written which is based on the above theory to calculate the subthreshold gate swing. Some of the results from this program are presented below.

When solving Poisson's equation, a constant depletion width $w_d = w_d(y_m)$ is assumed, which means that the ionized impurity outside $x = w_d(y_m)$ is ignored. Fig. 3–3 shows the potential along $x = w_d(y_m)$ for devices of different channel length. One can see that the potential along this line is not equal to the constant: $\frac{1}{\beta} \ln \frac{N_A}{N(w_d)}$. Fig. 3–4 shows the depletion width calculated at a normalized current level $\frac{I_D}{W/L} = 1nA$ by using condition $\psi(w_d, y) = \frac{1}{\beta} \ln \frac{N_A}{N(w_d(y))}$, for devices of different channel length. It is clearly shown that the depletion depth is not a constant throughout the channel. w_d is wider at the source/drain end than at the middle of the channel, in agreement with the results from a numerical simulator. Thus we conclude that the error caused by the constant depletion depth assumption is smaller than was originally expected. Fig. 3–4 also shows that the depletion depth for a shorter channel device is wider than that of a longer channel device.

Fig. 3–5 shows the calculated surface potential of devices with different channel length at the normalized current level $1nA$. The parameters used in the above calculations are $t_{ox} = 250\mathring{A}$, $N_A = 4e14cm^{-3}$, $r_j = 0.25\mu m$, shallow implantation dose $7e11cm^{-3}$, energy $50keV$, deep implantation dose $7e11cm^{-3}$, energy $140keV$, $V_D = 0.1V$, $V_B = 0$. It is shown that for a long channel device, a large portion of its surface potential is constant. However, this is not the case for a short-channel device. Instead, there is a minimum potential and this minimum point shifts towards the source end when the channel length reduces. It is also shown that to produce the same level of the normalized drain current, shorter device has a lower

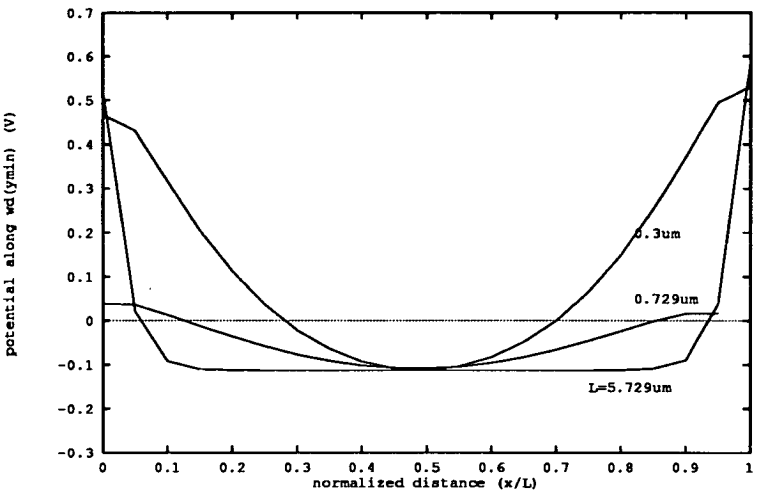


Figure 3–3: Calculated potential along $w_d(y_m)$ for different channel length The channel lengths $L = 0.729\mu m$ and $5.729\mu m$ correspond with the actual channel lengths of my experimental devices.

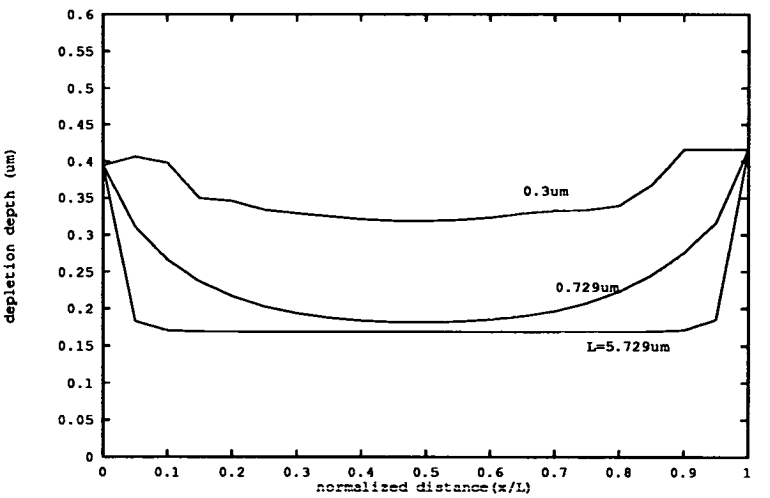


Figure 3–4: Calculated depletion width with different channel length

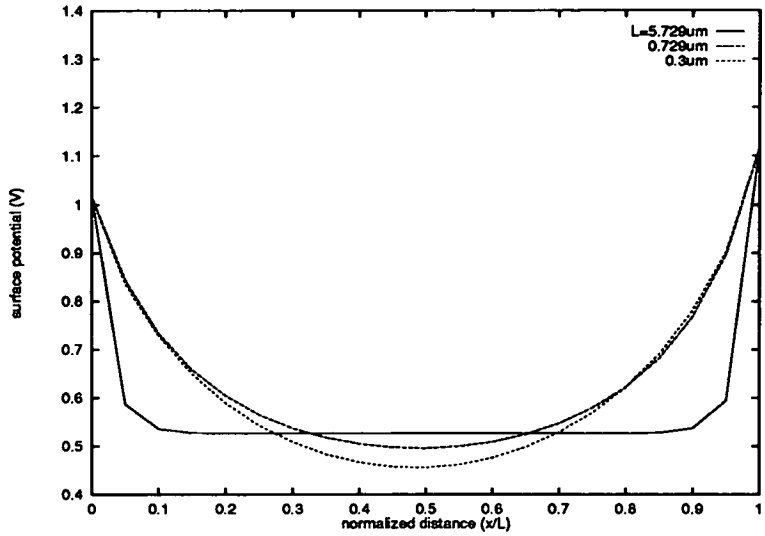


Figure 3–5: Calculated potential along channel surface with different channel length

surface potential. This can be attributed to the effect that L_{eff}/L is smaller for a shorter device. Those results are in agreement with that of a numeric simulator.

Fig. 3–6 compares the calculated surface potential by using cylindrical and rectangular source/drain junctions and the result of a numeric simulator PISCES. The channel length used is $0.729\mu m$. $I_D/(W/L) = 1nA$ is used for the cylindrical junction. Then the value of V_G which corresponds to this current level is calculated and used for the rectangular junction and in PISCES. The agreement between the results from the numeric simulator and our two-dimensional analytical model is satisfactory. It is obvious that using the rectangular source/drain junction results in a larger surface barrier lowering than using a cylindrical junction, thus results an overestimated short-channel effect.

The analytical model is compared to numeric simulator PISCES in Figs. 3–7 and 3–8. The parameters used in Fig. 3–7 are the same as in Figs. 3–3 to 3–6. In Fig. 3–8, the shallow implantation energy is $25keV$ and all other parameters are the same as previously used. It shows the subthreshold gate swing versus channel

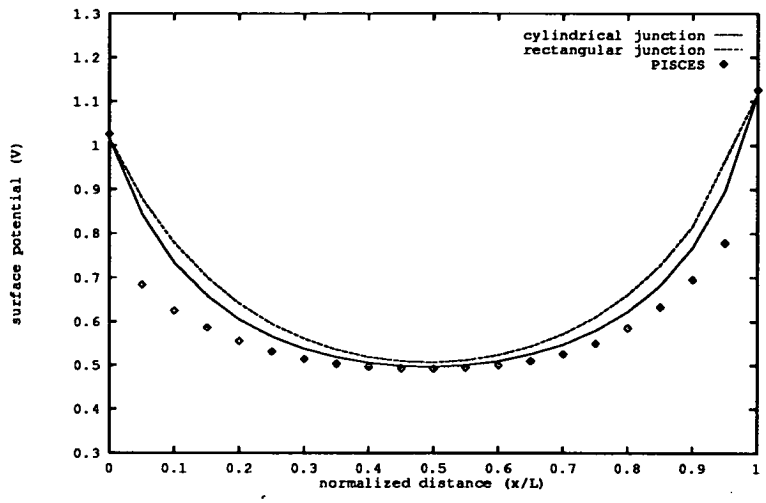


Figure 3–6: Calculated surface potential along the channel by using different models

length at substrate bias $V_B = 0$ to $-1V$. It is clear in Figs. 3–7 and 3–8 that as the channel length decreases, the subthreshold gate swing increases. And the subthreshold gate swing reduces as the substrate bias increases. The agreement between results of the analytical model and the numeric model is satisfactory.

In the analytical model, the doping profile described by a Gaussian distribution including annealing effect[110] is used. That is,

$$N(x) = N_A + \sum_{i=1}^{2}[R_i(A,x) + R_i(A,-x)] \tag{3.29}$$

where

$$R_i(A,x) = \frac{1}{2}\frac{D_{Ii}}{\sqrt{2\pi}\Delta R'_{pi}} \exp\left[-\frac{(x-A)^2}{2\Delta R'^2_{pi}}\right] \text{erfc}\left[-\frac{2DtA + x\Delta R^2_{pi}}{2\Delta R_{pi}\Delta R'_{pi}\sqrt{Dt}}\right] \tag{3.30}$$

$$A = R_{pi} - t_{ox}\frac{\Delta R_{pi}}{\Delta R_{oxi}} \tag{3.31}$$

$\Delta R'_{pi} = \sqrt{\Delta R^2_{pi} + 2Dt}$ and $Dt = \sum_j D_j t_j$. D_I is the implantation dose, R_p is the projected range, ΔR_p is the standard deviation of the projected range, $\Delta R'_p$ is the effective standard deviation after annealing, Dt is the product of diffusion coefficient and the annealing time.

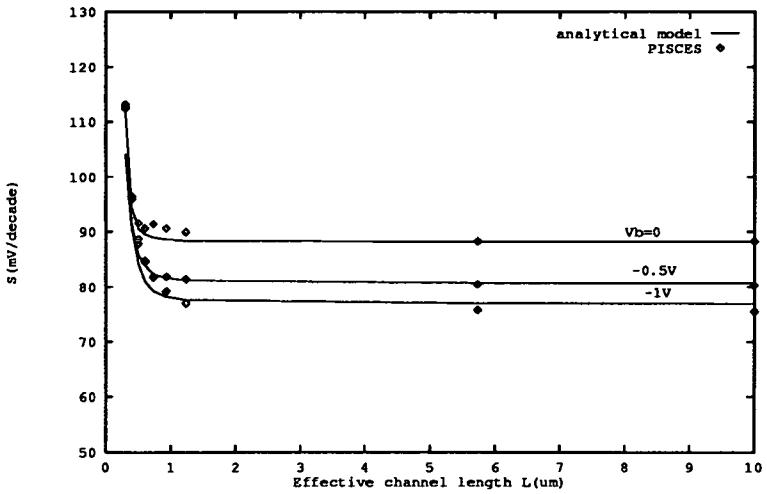


Figure 3–7: Subthreshold gate swing vs. channel length

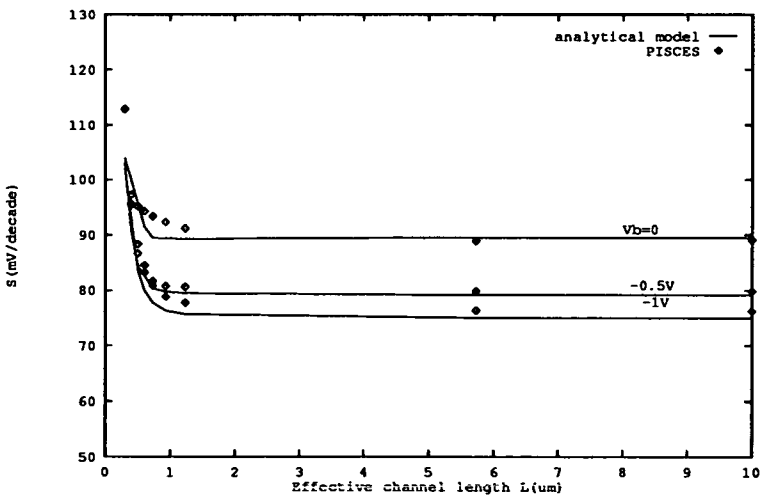


Figure 3–8: Subthreshold gate swing vs. channel length

Only the surface current path has been considered in this section so far. When the channel length of a device reduces or the drain bias rises, a bulk current path may arise. In this case, this bulk current component has to be included in the subthreshold current model. In the next section, this problem will be dealt with.

3.3 Punchthrough Model

3.3.1 Theory and Results

Solving the two-dimensional Poisson's Equation as in Section 3.2, but taking into account the bulk current accurately, one has to consider the situation under which drain and source induced field has reached to the other end of the channel. Thus the boundary conditions $\psi(x,0)$ and $\psi(x,L)$ used in Section 3.2 are no longer valid. Instead, the following $\psi(x,0)$ and $\psi(x,L)$ are to be used.

$$\psi(x,0) = \psi_S(x,0) + f(x)\psi_D(x,0) \tag{3.32}$$

$$\psi(x,L) = \psi_D(x,L) + f(x)\psi_S(x,L) \tag{3.33}$$

where $f(x)$ has to satisfy $f(0) = 0$ and $f(W_{S,D}) = 1$. $f(x) = \sin(\frac{\pi}{2}\frac{x}{W_{S,D}})$ is chosen here. The solution has the same form as in Section 3.2. That is

$$\psi(x,y) = \psi_L(x) + V(x,y) \tag{3.34}$$

$$\psi_L(x) = V'_{GB} - \frac{q}{\epsilon_{si}}F(x) - \frac{q}{\epsilon_{si}}x[G(w_d) - G(x)] - \frac{q}{C_{ox}}G(w_d) \tag{3.35}$$

$$V(x,y) = \sum_{n=0}^{\infty} \frac{\cos k_n(w_d - x)}{u_n \sinh k_n L}[H_n \sinh k_n(L-y) + I_n \sinh k_n y] \tag{3.36}$$

Surface Current

The condition for a surface conducting path to exist is that the transverse electrical field at the surface should fulfill the condition

$$\mathcal{E}_s = -\frac{\partial \psi}{\partial x}(0, y_m) > 0 \tag{3.37}$$

Using the boundary condition Eq. (3.1), one has

$$\frac{q}{\epsilon_{si}}G(w_d) - \frac{C_{ox}}{\epsilon_{si}}\sum_{n=0}^{\infty}\frac{\cos k_n w_d}{u_n \sinh k_n L}[H_n \sinh k_n(L-y_m) + I_n \sinh k_n y_m] > 0 \quad (3.38)$$

The surface current[40]

$$I_{DS} = qD_n\frac{Wt_{ch}}{L_{eff}}\left(\frac{n_i^2}{N_A}\right)\exp[\beta(\psi_{smin}+V_B)][1-\exp(-\beta V_D)] \quad (3.39)$$

H_n and I_n have the form of

$$H_n = \frac{\sin k_n w_d}{k_n w_d}[V_{bi} - (V_G - V_{FB}) - \frac{q}{C_{ox}}G(w_d)] + \Delta_h \quad (3.40)$$

$$I_n = \frac{\sin k_n w_d}{k_n w_d}[V_{bi} + V_D - (V_G - V_{FB}) - \frac{q}{C_{ox}}G(w_d)] + \Delta_i \quad (3.41)$$

Substituting Eq. (3.40) and (3.41) into (3.38), it is clear that either the decrease of $V_G - V_{FB}$ or increase of V_D may cause the surface conducting path shift into the bulk. The reduction of channel length L will cause the shift as well. The integral of the doping profile in the depletion region will also have an effect on the position of the conducting path. Thus whether the punchthrough path lies in the surface or in the bulk is decided by the value of $V_G - V_{FB}$, V_D, the channel length L and the integral of the doping profile in the depletion region etc. all together, not only by the sign of $V_G - V_{FB}$.

Bulk Current

For a MOSFET with a uniformly doped channel, when its drain bias rises or its gate bias drops until $\mathcal{E}_s < 0$, the conducting path shifts from the surface to the bulk. For a device with a nonuniformly doped channel, even if the surface path exists, there could be a bulk path existing at the same time, provided that there exists another potential peak in the bulk along the direction normal to the current path.

We calculate this bulk current at the saddle point (x_p,y_p)[40]. Let $\psi_{pm} = \psi(x_p, y_p)$, ψ_{pm} is the potential minimum in the direction along the current path and the potential maximum along direction normal to the current path. The point

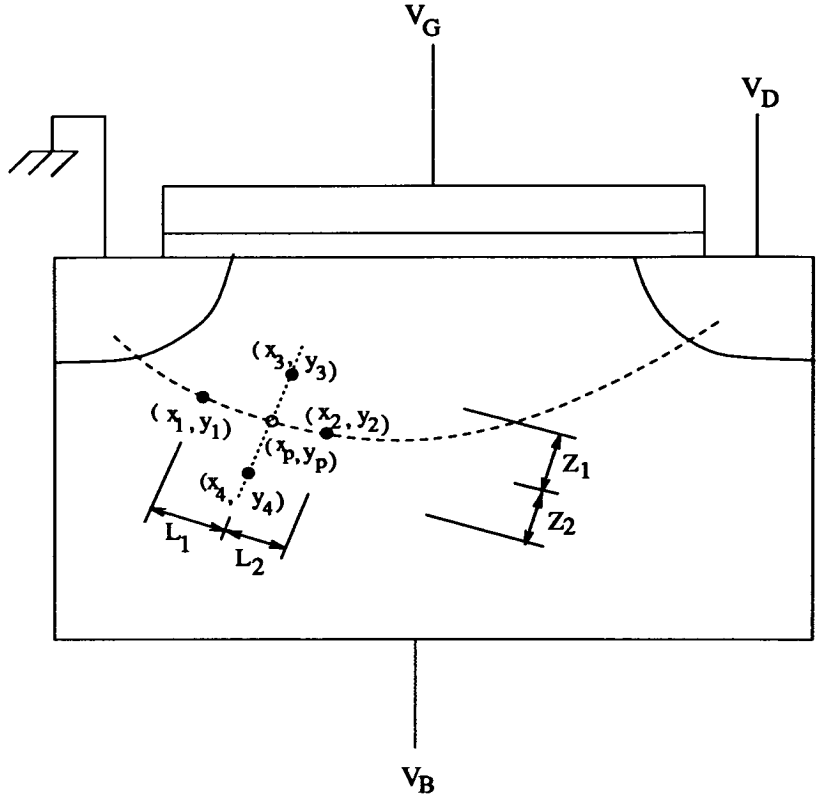


Figure 3–9: Schematic cross section of an nMOSFET

(x_p, y_p) can be found under conditions $\frac{\partial \psi}{\partial x}(x_p, y_p) = 0$ and $\frac{\partial \psi}{\partial y}(x_p, y_p) = 0$. The bulk current[40]

$$I_{DB} = qD_n \frac{Wt_{ch}}{L_{eff}} \left(\frac{n_i^2}{N_A}\right) \exp[\beta(\psi_{pm} + V_B)][1 - \exp(-\beta V_D)] \tag{3.42}$$

where $L_{eff} = L_2 + L_1$, $t_{ch} = Z_2 + Z_1$ and $\psi(x_1, y_1) = \psi(x_2, y_2) = \psi_{pm} + \frac{\pi}{4\beta}$, $\psi(x_3, y_3) = \psi(x_4, y_4) = \psi_{pm} - \frac{\pi}{4\beta}$. Refer to Fig. 3–9 for definitions of geometry terms. The total punchthrough current

$$I_D = I_{DS} + I_{DB} \tag{3.43}$$

3.3.2 Verification and Discussion

A FORTRAN77 program has been written based on the theory discussed above to calculate the punchthrough current under subthreshold bias condition, which includes both the surface and the bulk current. Some results from this programme are presented below.

Potential distribution along $y = y_m$ is compared between results of our analytical model and those of PISCES in Figs. 3–10 to 3–15. Parameters used in our

calculations are $t_{ox} = 250\mathring{A}$, $N_A = 4e14cm^{-3}$, $r_j = 0.25\mu m$, $L = 1.272\mu m$. In Figs. 3–10 to 3–13, a single implantation with implantation energy $25keV$, dose $7e11cm^{-2}$ is used. In Figs. 3–14 and 3–15, besides using above shallow implantation, a deep implantation of energy $140keV$ and dose $7e11cm^{-2}$ is used as well. It is clear for the single implantation case that as the drain bias increases, the potential barrier in the surface and in the bulk both are lowered, but comparing with the surface potential, the substantial barrier lowering happens in the bulk. The agreement between our analytical model and the numerical simulator is very good with zero substrate bias. There is discrepancy in the bulk when a negative substrate bias is applied. It is also clear comparing Figs. 3–10, 3–11 with Figs. 3–14 and 3–15 that the second implantation suppressed the bulk current sufficiently, thus the change of drain bias does not have much effect on the surface potential.

The subthreshold characteristics resulting from our analytical model and PISCES are compared in Figs. 3–16 to 3–21. In Figs. 3–16 and 3–17, the channel length of the MOSFET's is $0.772\mu m$. In Figs. 3–18 and 3–19, the channel length of the MOSFET is $1.272\mu m$. Other parameters for above two devices are the same as those used in Fig. 3–10. Parameters used in Figs. 3–20 and 3–21 are the same as those used in Fig. 3–14.

In Figs. 3–16, 3–18 and 3–20, the effect of drain bias V_D on the subthreshold characteristics has been compared for the calculated results of our model and those of PISCES. It is shown that the increase of V_D raises both the surface and the bulk punchthrough current which indicates that increasing V_D lowers the potential barrier at both surface and the bulk. As the channel length reduces, the influence of V_D becomes more profound. But a second ion implantation suppresses the influence of V_D successfully.

In Figs. 3–17, 3–19 and 3–21, the effect of the substrate bias V_B on the subthreshold characteristics has been compared between the calculated results of our model and those of PISCES. A strong suppression of the punchthrough current is observed when the substrate bias increases, especially that of a bulk component. For devices with second implantation, the influence of V_B is more profound.

From Figs. 3–16 to 3–21, it is observed that when gate bias V_G is smaller than a

certain value V_{Gp}, it loses its controls on the punchthrough current. This indicates that the bulk punchthrough current dominated at this state. It is clearly shown that the value of V_{Gp} is dependent on drain bias V_D, substrate bias V_B, channel length L and substrate doping profile.

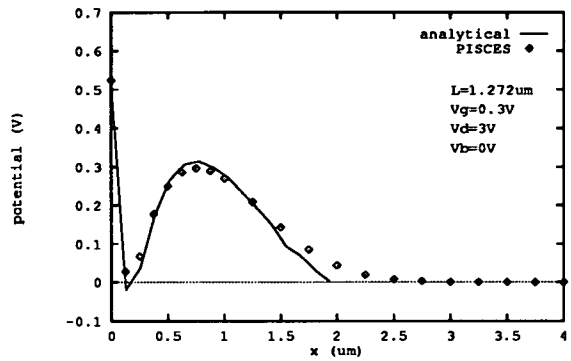


Figure 3–10: Potential distribution along $y = y_m$

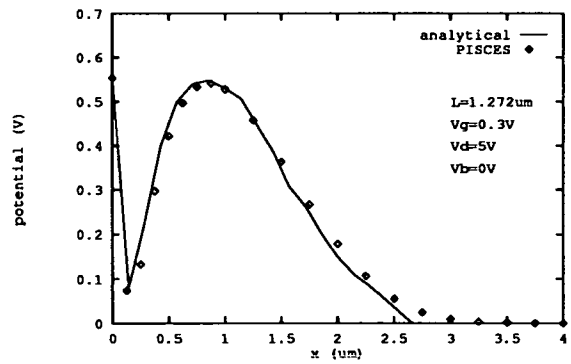


Figure 3–11: Potential distribution along $y = y_m$

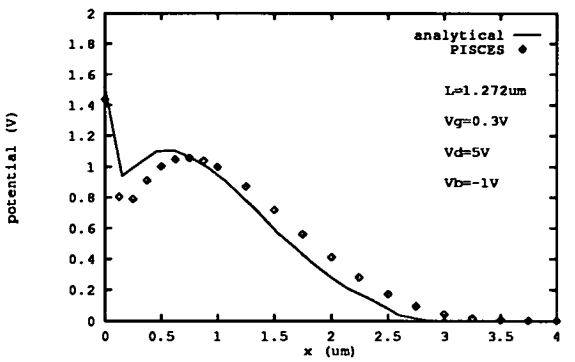


Figure 3–12: Potential distribution along $y = y_m$

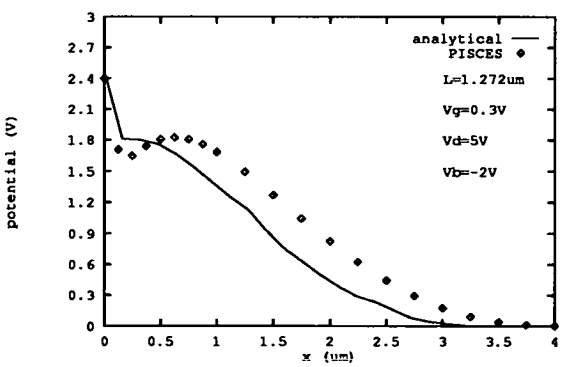


Figure 3–13: Potential distribution along $y = y_m$

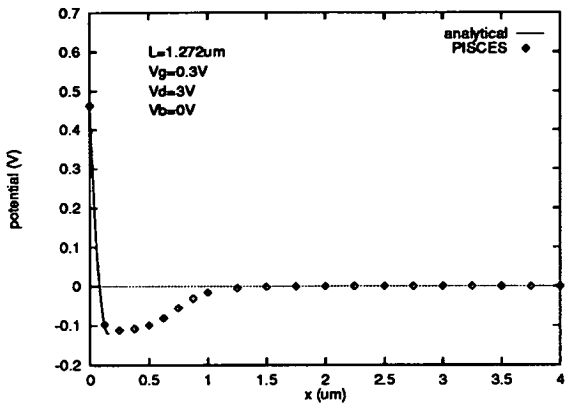


Figure 3–14: Potential distribution along $y = y_m$

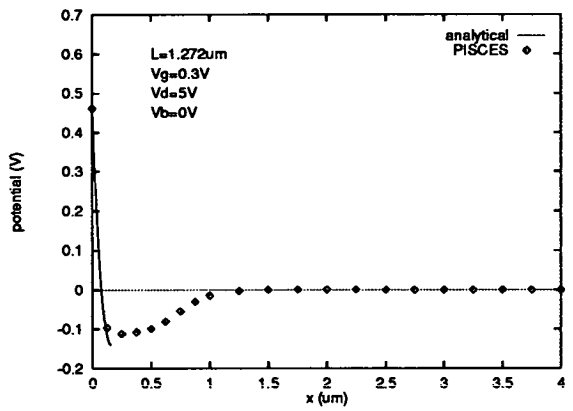


Figure 3–15: Potential distribution along $y = y_m$

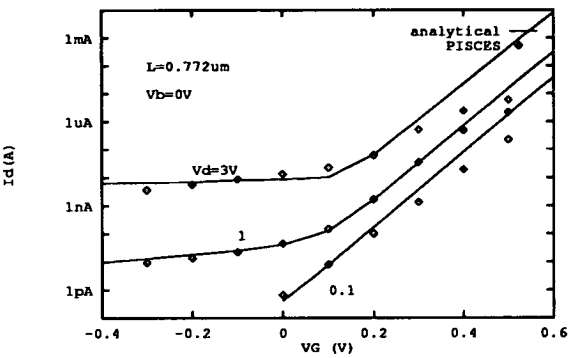


Figure 3–16: Gate characteristics

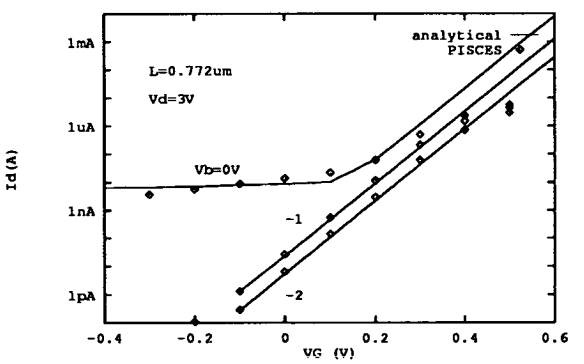


Figure 3–17: Gate characteristics

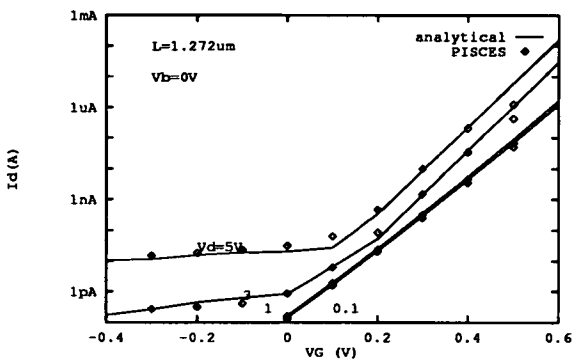


Figure 3–18: Gate characteristics

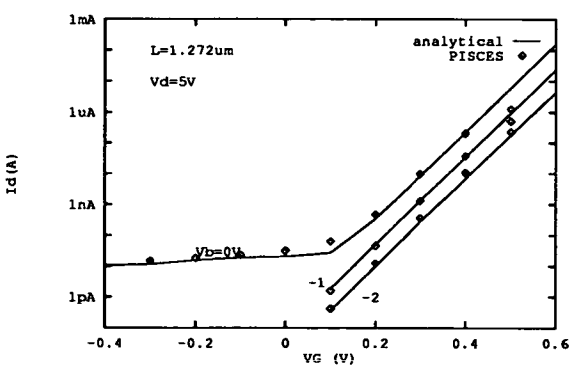


Figure 3–19: Gate characteristics

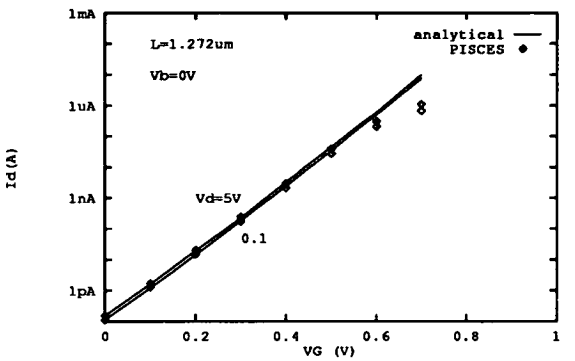


Figure 3–20: Gate characteristics

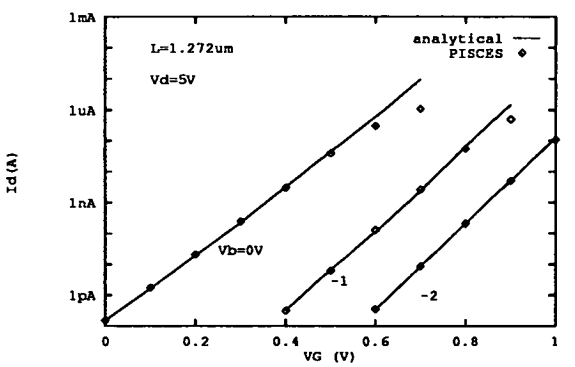


Figure 3–21: Gate characteristics

Chapter 4

Experimental Devices and Test Systems

Experimental devices have been made by using the EMF 1.5μm NMOS process. The main steps of the process are described below.

4.1 EMF 1.5μm nMOS Process

Throughout the process, positive photoresist is used, i.e. the areas of resist exposed to UV light remain in the development process.

The starting material is a 3-inch diameter wafer which is lightly doped p-type silicon with a $\langle 100 \rangle$ crystal orientation. The $\langle 100 \rangle$ orientation offers the lowest surface state density at the Si – SiO_2 interface. The low impurity doping results in a high resistivity of 14 – 20Ω·cm to ensure low source and drain parasitic capacitances.

The first step is the initial clean; that is, using acid to remove unwanted impurities from the surface of the wafer, such as organic materials and a surface layer of silicon dioxide.

A technique called LOCOS (LOCal Oxidation of Silicon) [111] is used to produce the field oxide to provide isolation between devices on the wafer. First, an initial oxide layer (thickness 350$\AA$) is grown over the entire wafer. Then, a layer

of thick silicon nitride about 1000Åthick is deposited. The first photomask defines the areas where devices will eventually be formed. All other areas of the silicon surface are isolation regions. After exposure and developing, only the active regions are covered by silicon nitride and resist. Boron is implanted into the field region (B_{11}^{+} at 70keV dose 8e12 atom/cm^2) to prevent any significant parasitic conduction path in the field region. The remaining photoresist can then be stripped away. A layer of field oxide about 6000$\mathring{A}$ thick is then grown in the isolation region. The silicon nitride which covers the active regions prevents any oxide growth and only a very thin layer of oxide grows on the nitride surface. Next, the silicon nitride and the initial oxide on the active region are all etched away. To ensure the quality of the silicon surface in the active region, a layer of sacrificial oxide is grown on it, then removed. The task of defining the active and the isolation regions has been done. Now, the wafer looks like in Fig. 4–1 and active devices can be made in the active region.

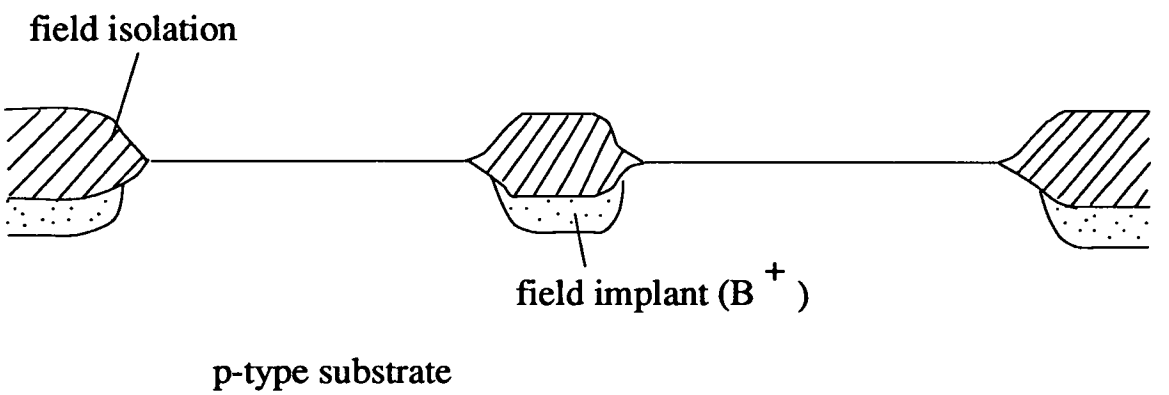


Figure 4–1: Diagram of wafer after the isolation (field) region and active region defined

A layer of thin (250$\mathring{A}$) and high quality oxide is grown as the gate oxide. Then on the active area, a shallow Boron implant (B_{11}^{+}) is performed to obtain the desired threshold voltage, followed by a deep Boron implant to prevent any punchthrough which may arise due to the lightly-doped substrate. To investigate

the influence of ion implantation on device electrical characteristics, a total of 15 different combinations of implant energy and dose is used. Their values are listed in Table 4.2.1.

Next, a layer of polysilicon is deposited over the whole wafer and doped with phosphorus to increase its conductivity. During the phosphorus deposition, a layer of phosphosilicate glass is formed on the surface so that has to be etched away. The surface of the polysilicon is oxidised to form a thin polyoxide layer to allow good adhesion of the subsequent photoresist layer. See Fig. 4–2.

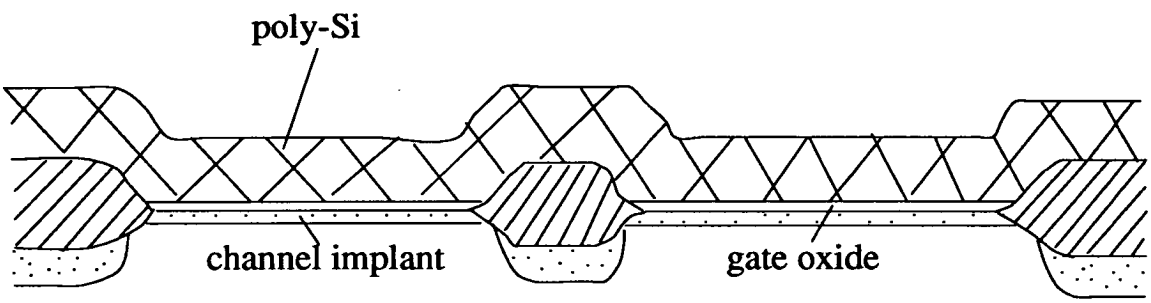


Figure 4–2: Diagram of wafer after gate formed

The second photomask is used to define the drain and source regions and the oxide and polysilicon are etched away. A heavy arsenic dose is implanted into the wafer to form the drain and source regions. An annealing step follows to repair the damage to the crystal structure caused by implantation. See Fig. 4–3.

A layer of pyrolytic oxide is deposited to insulate the polysilicon from metal interconnection layer. Next, a high temperature reflow step is employed to smooth the coverage of the pyro over the sharp edges of the polysilicon tracks. Then a wet oxidation step is used to leach phosphorus from the surface of the pyro to improve the adhesion of the photoresist in the next step.

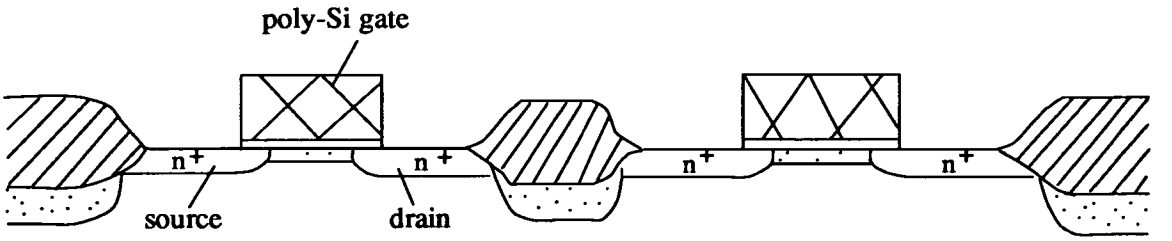


Figure 4–3: Diagram of wafer after source/drain formed

The third photomask is used to define contact windows where aluminum will make contact to the polysilicon and diffusion areas below. The oxide is etched out of the areas defined for contact windows.

Finally, a layer of aluminum is sputtered over the wafer and a fourth photomask is used to define the interconnection pattern. Unwanted aluminum is etched away and a low temperature anneal (sinter) is used to ensure a good ohmic contact between aluminum and silicon. See Fig. 4–4.

4.2 Ion Implantation

As mentioned in Chapter 2, ion implantation into the channel of a device is used to determine the threshold voltage of a MOSFET. To investigate how ion implantation affects the subthreshold operation of MOSFETs, a group of 15 wafers with different ion implantation energies and doses has been manufactured using the EMF 1.5μm nMOS process described above. The doses and energies used are listed in Table 4.2.1.

Wafers 1–6 have only one ion implantation. Among them, Wafers 1, 2 and 4 have the same implantation energy but different doses. Wafers 3–6 have the same

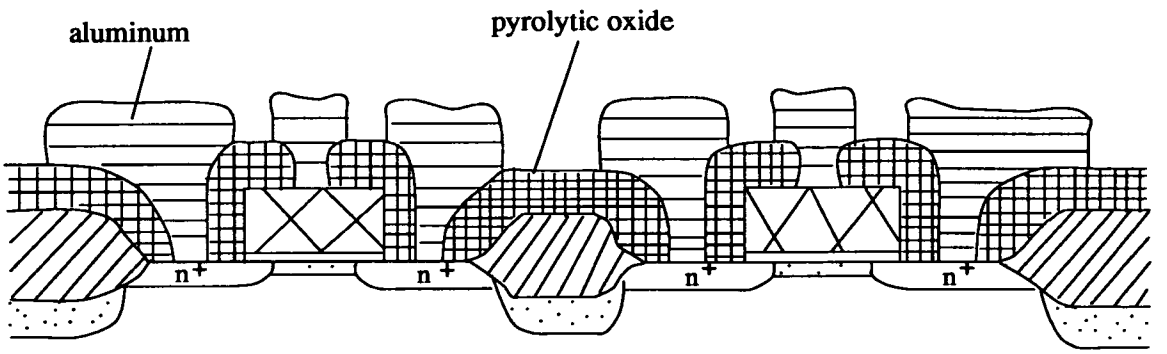


Figure 4–4: Diagram of wafer at the end of process

Table 4.2.1 Boron Implantation in Channel				
Wafer No.	$Dose_1(cm^{-2})$	$Energy_1$(keV)	$Dose_2(cm^{-2})$	$Energy_2$(keV)
1	2e11	25	–	–
2	5e11	25	–	–
3	7e11	10	–	–
4	7e11	25	–	–
5	7e11	50	–	–
6	7e11	100	–	–
7	3e11	25	7e11	140
8	5e11	25	7e11	140
9	7e11	10	7e11	140
10	7e11	15	7e11	140
11	7e11	25	7e11	140
12	7e11	50	7e11	140
13	7e11	25	5e11	140
14	7e11	25	7e11	100
15	7e11	25	7e11	200

implantation dose but different energies. Wafers 7–15 are double-implanted. Wafer 11 had the standard implants for the EMF 1.5μm nMOS process. Of four implant parameters: the shallow implantation dose and energy and the deep implantation dose and energy, only the shallow implantation doses were changed for Wafers 7, 8 and 11. Wafers 9–12 have different shallow implantation energies. The deep implantation energy for Wafers 11, 14 and 15 vary. Wafers 11 and 13 also have different deep implantation doses. By changing the ion implantation parameters for each subgroup of wafers, the effect of implantation parameters on subthreshold behaviour of MOSFETs can be studied and the results can provide a quick guide for device and process designers.

A two dimensional process simulator SUPRA (Stanford University PRocess Analysis program) [112] was used to predict the impurity profile at the end of the process in the channel of a MOSFET on each wafer. The SUPRA results for wafers 1 to 15 are shown in Figs. 4–5 to 4–19.

4.3 Geometry Arrangement

To investigate the geometry effect on MOSFETs, four devices with the same width and different length and four devices with the same length and different width from each wafer were used in the experiments. The device dimensions are listed in Table 4.3.1.

Note that the channel width and length indicated in the table are the mask width W_m and the mask length L_m of the channel. The effective width $W = W_m - 2\Delta W$, and the effective length $L = L_m - 2L_d$ are smaller than the mask width and the mask length. See Section 4.5.

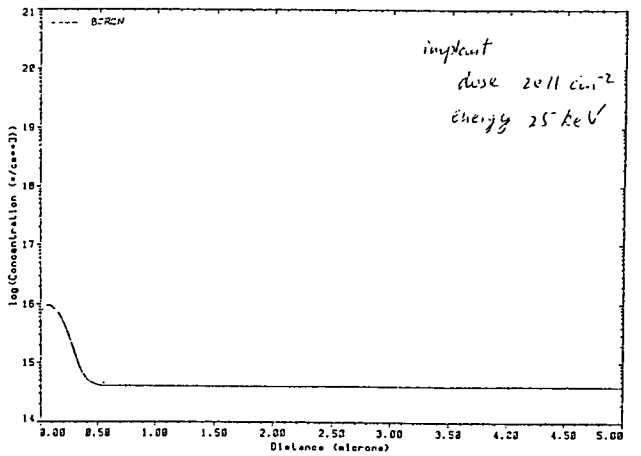


Figure 4–5: Boron profile in channel of MOSFET on wafer 1

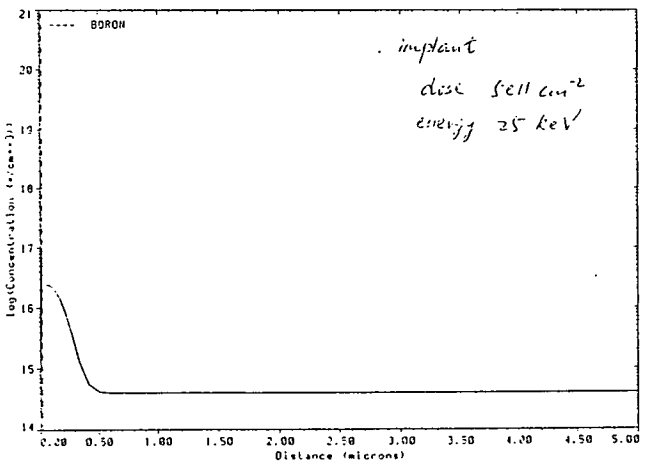


Figure 4–6: Boron profile in channel of MOSFET on wafer 2

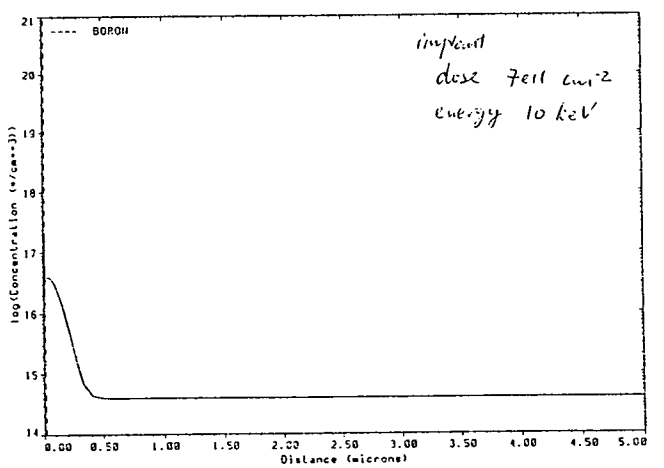


Figure 4–7: Boron profile in channel of MOSFET on wafer 3

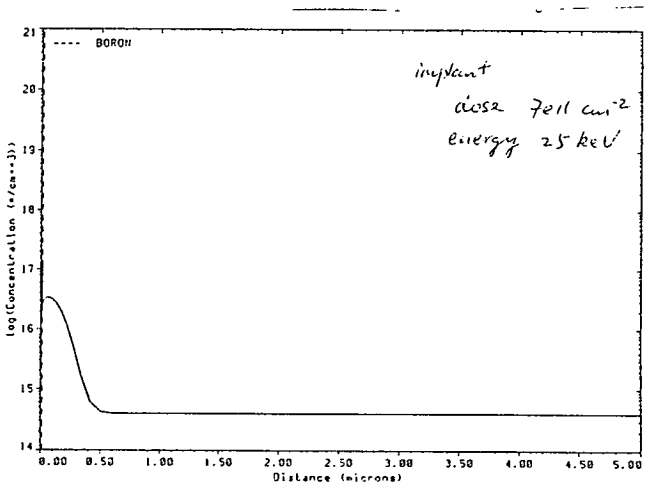


Figure 4–8: Boron profile in channel of MOSFET on wafer 4

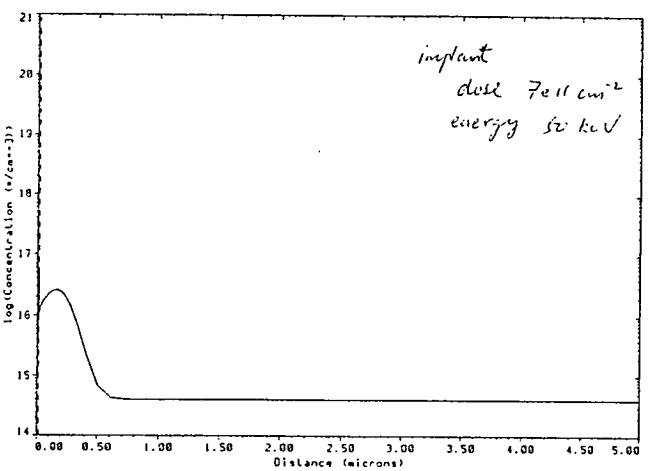


Figure 4–9: Boron profile in channel of MOSFET on wafer 5

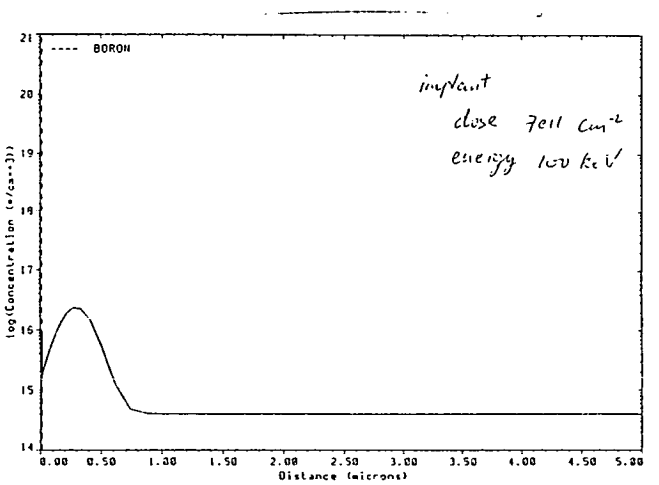


Figure 4–10: Boron profile in channel of MOSFET on wafer 6

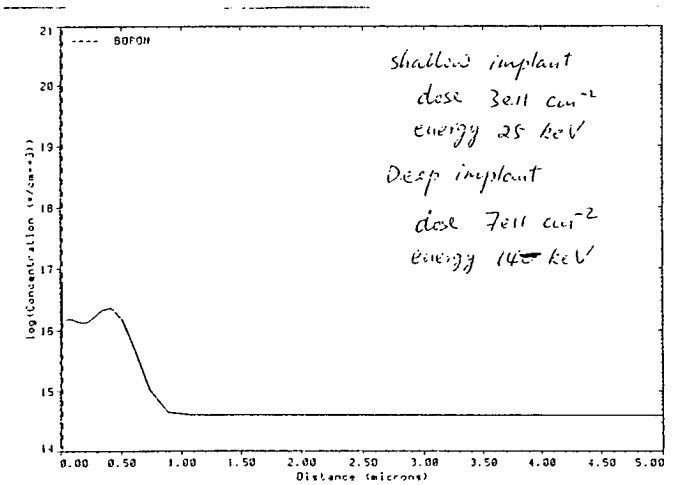


Figure 4–11: Boron profile in channel of MOSFET on wafer 7

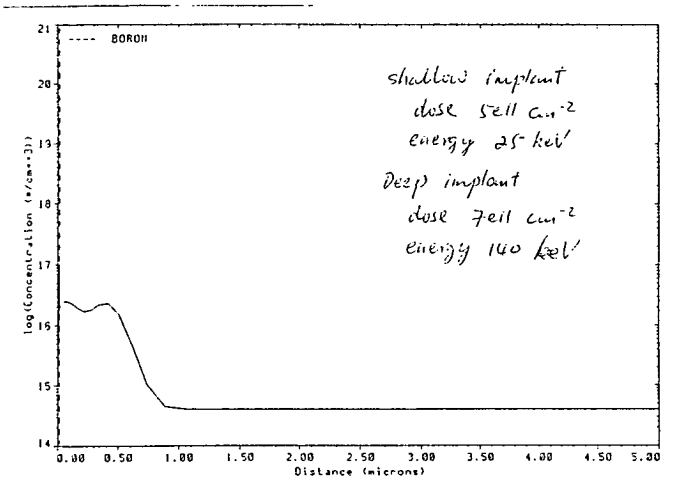


Figure 4–12: Boron profile in channel of MOSFET on wafer 8

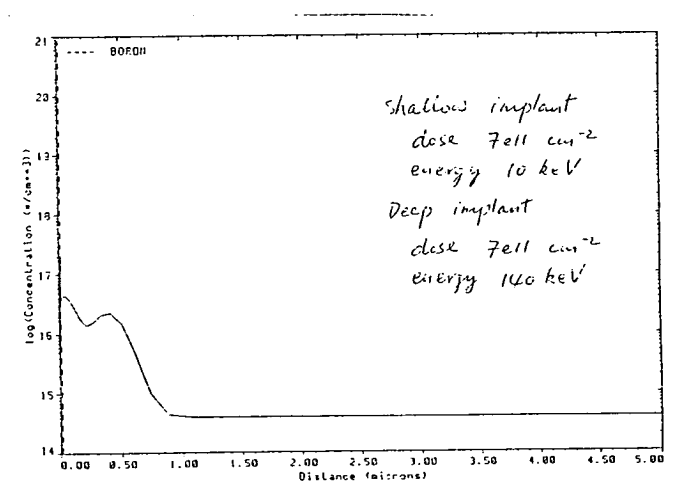


Figure 4–13: Boron profile in channel of MOSFET on wafer 9

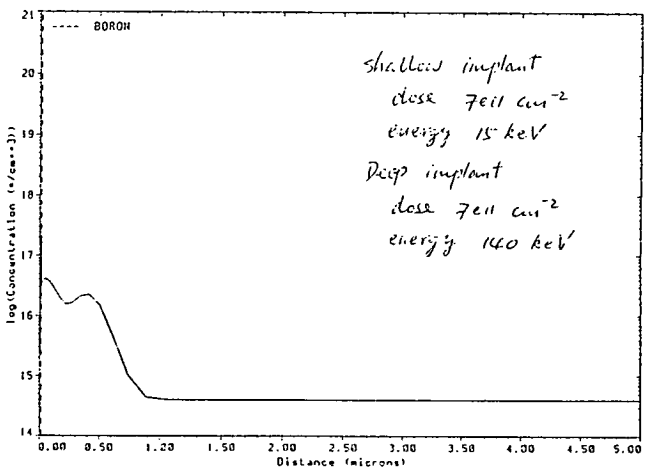


Figure 4–14: Boron profile in channel of MOSFET on wafer 10

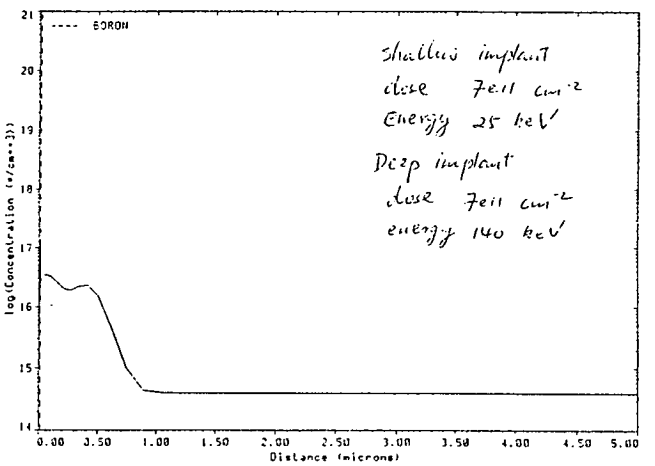


Figure 4–15: Boron profile in channel of MOSFET on wafer 11

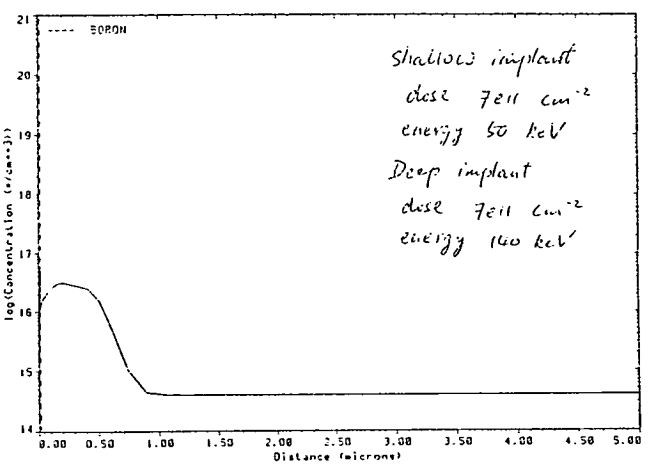


Figure 4–16: Boron profile in channel of MOSFET on wafer 12

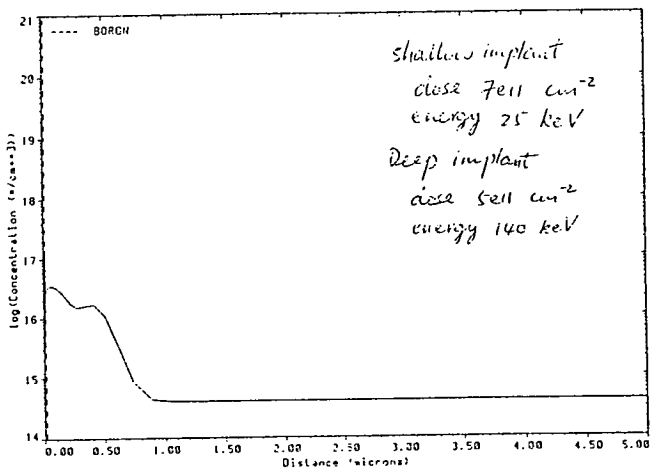


Figure 4–17: Boron profile in channel of MOSFET on wafer 13

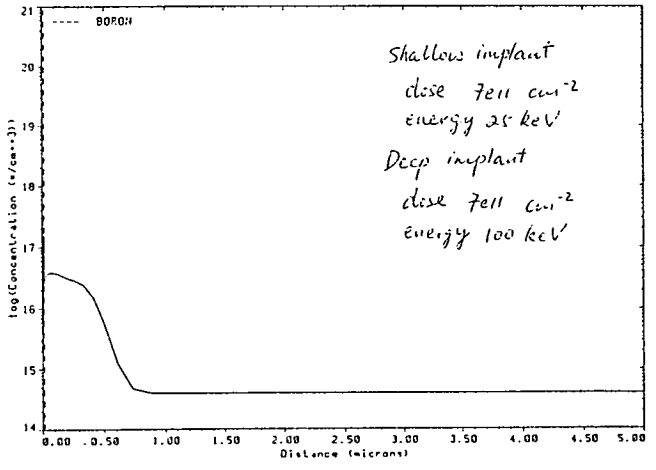


Figure 4–18: Boron profile in channel of MOSFET on wafer 14

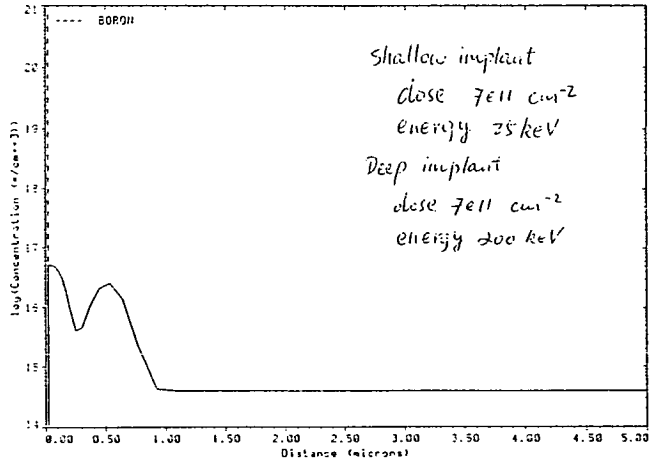


Figure 4–19: Boron profile in channel of MOSFET on wafer 15

Table 4.3.1 Geometry Arrangement		
Device	Channel Width(μm)	Channel Length(μm)
A	30	6
B	30	1.5
C	30	1.2
D	30	1.0
E	7	30
F	1.5	30
G	1.2	30
H	1.0	30

4.4 Measurement Instrumentation

An HP 4145B Semiconductor Parameter Analyzer was used to measure the current and an HP310 computer was used as a controller. The diagram of the measurement system is illustrated in Fig. 4–20. The software which controls the measurement system was written using HP Basic 5.0. The system is capable of measuring currents down to 1pA.

To minimize the noise level when measuring the subthreshold drain current, packaged chips were used in the experiments. For each sample, the gate voltage V_G was chosen so that its lower limit ensured the drain current was measured from 1pA. The upper limit was just above the threshold voltage V_T at

(a) 5 values of substrate bias V_B ranging from 0 to $-2V$ with an interval of $-0.5V$ and drain bias $V_D = 0.1V$.

(b) substrate bias $V_B = 0$ and drain bias V_D ranging from $0.1V$ to $2.6V$ with an interval of $0.25V$.

Figs. 4–21 to 4–24 show subthreshold characteristics of 4 devices from Wafer 11 with V_B as a parameter (Condition (a) above). Figs. 4–25 and 4–26 show subthreshold characteristics with V_D as a parameter (Condition (b) above).

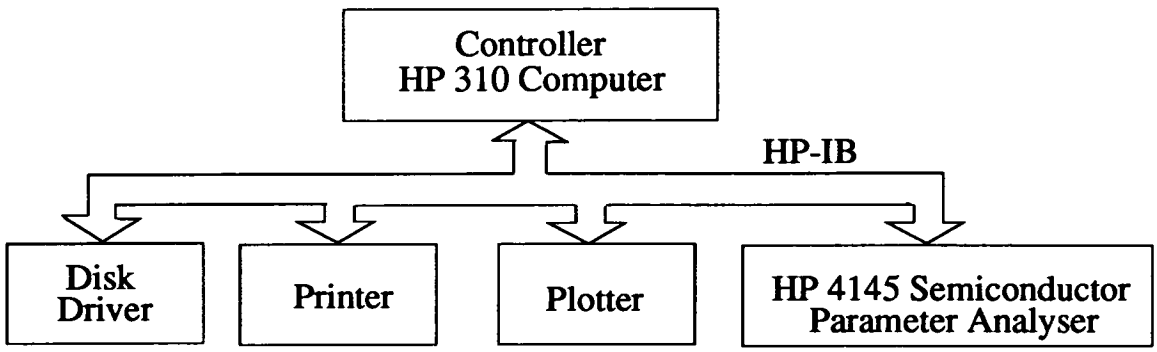


Figure 4–20: Instrument set up for measurement

4.5 Parameter Extraction

One of the best known circuit simulators is SPICE. It has models for MOSFETs at three different levels. Level 1 uses a very simple first order model which gives correspondingly approximate results. Level 2 uses a more sophisticated model which is derived from the physics of the device. Level 3 is more accurate and uses empirical factors to describe small geometry effects. Since small geometry effects are one of the main points of interest in our experiments, SPICE level 3 model was used.

Parameters for the SPICE level 3 model, (i.e. threshold voltage V_T, body factor γ, diffusion length L_d and width reduction ΔW) for each experimental device were extracted using a parameter extractor developed in the EMF, called PARAMEX.

The threshold voltage, V_T, also determines the range of gate voltage values in which a MOS device operates in the subthreshold region. To a first order, the equation for current in the linear region of operation is

$$I_D = Beta[V_G - V_T - \frac{V_D}{2}]V_D \tag{4.1}$$

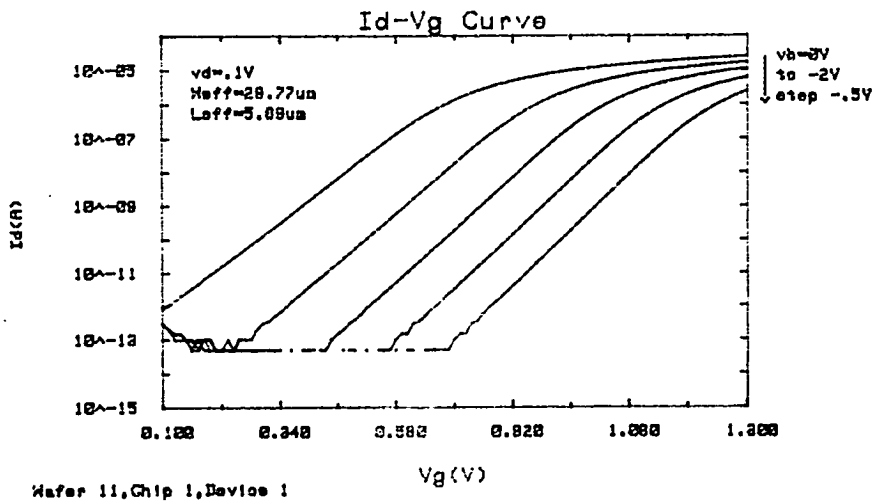


Figure 4–21: Subthreshold characteristic of Wafer 11 Device A

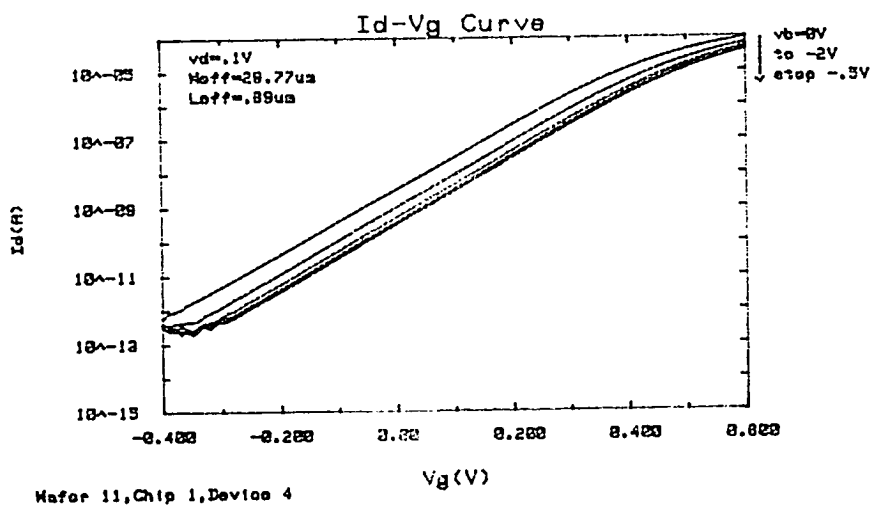


Figure 4–22: Subthreshold characteristic of Wafer 11 Device D

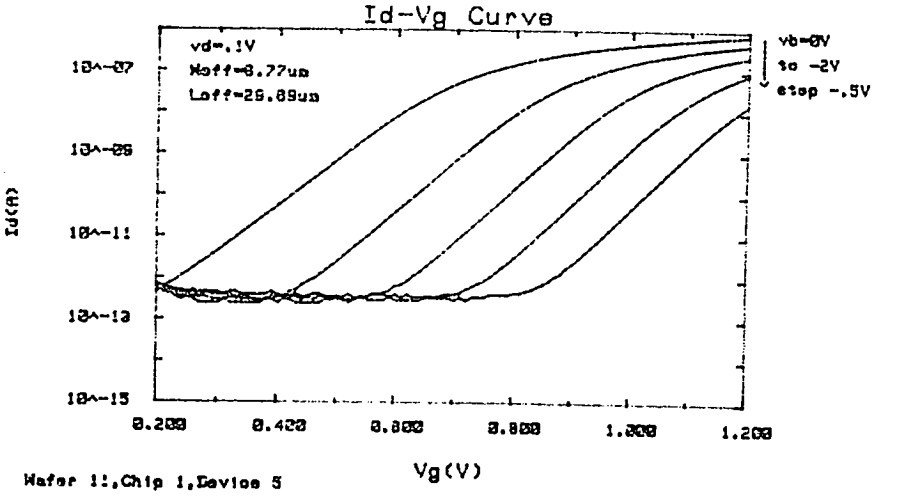


Figure 4–23: Subthreshold characteristic of Wafer 11 Device E

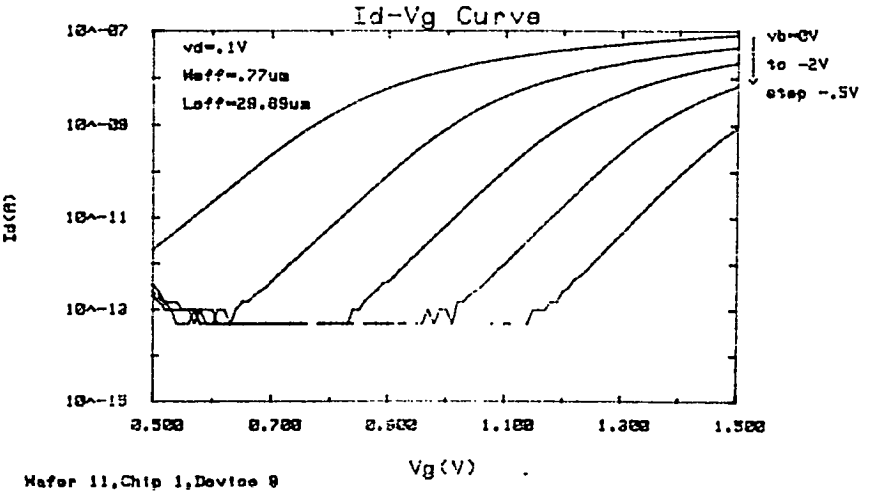


Figure 4–24: Subthreshold characteristic of Wafer 11 Device H

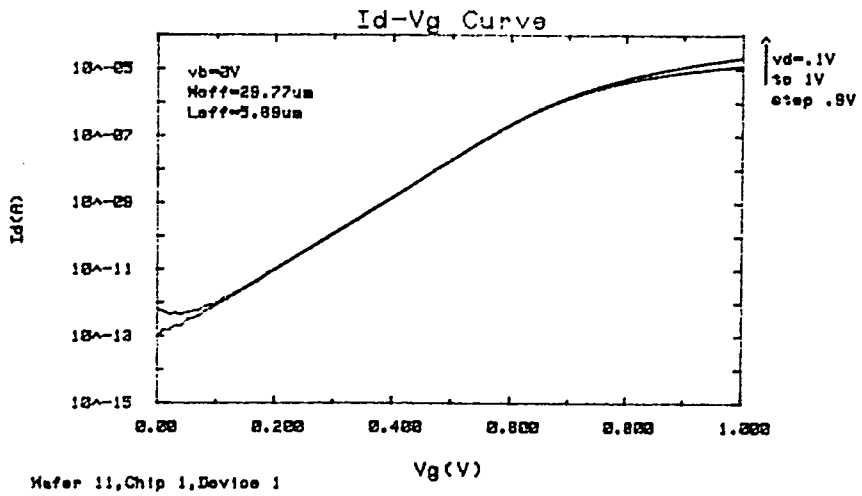


Figure 4–25: Subthreshold characteristic, V_D as parameters

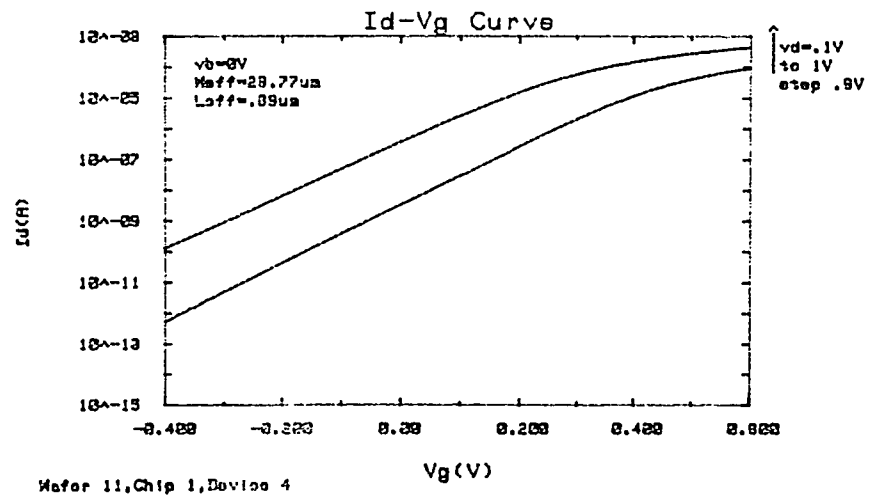


Figure 4–26: Subthreshold characteristic, V_D as parameters

where *Beta* denotes the gain of a MOSFET. Then

$$\frac{I_D}{Beta \cdot V_D} = V_G - V_T - \frac{V_D}{2} \tag{4.2}$$

On a V_G vs. I_D graph, the intercept on the V_G-axis i.e. when $I_D = 0$ is $V_T + \frac{V_D}{2}$. V_D is kept small at $0.1V$.

Since body factor $\gamma = \sqrt{2q\epsilon_{si}N_{eff}}/C_{ox}$, it can be used to calculate the average substrate doping level and thus to obtain the minimum surface potential in the channel. It will be used in Section 6.2.

$$V_T = V_{T0} - \gamma|2\psi_B|^{\frac{1}{2}} + \gamma|2\psi_B - V_B|^{\frac{1}{2}} \tag{4.3}$$

Plot V_G vs. I_D at several different substrate biases. V_T at each V_B is found, then plot V_T vs. $|2\psi_B - V_B|^{\frac{1}{2}}$. The slope is γ.

The diffusion length L_d is caused by lateral diffusion of the n^+ source and drain into areas under the gate. The actual channel L is given by

$$L = L_m - 2L_d \tag{4.4}$$

where L_m is the mask channel length. To find L_d, the gains of transistors of different channel length are found from their transfer characteristics. The drain voltage has to be kept low to ensure that the depletion region around the drain would not affect the measurement. The gate voltage should be large enough to bias the devices in the linear region but not higher. This enables the maximum *Beta* to be measured and so reduces the influence of parasitic source and drain contact resistances on the measurement. Biasing the devices in the linear region means that the *Beta* values can be found from

$$Beta = \frac{I_D}{(V_G - V_T - \frac{V_D}{2})V_D} \tag{4.5}$$

Beta can also be expressed as

$$Beta = \mu_{eff}C_{ox}\frac{W_m}{L_m - 2L_d} \tag{4.6}$$

That is

$$\frac{1}{Beta} = \frac{L_m}{\mu_{eff}C_{ox}W_m} - \frac{2L_d}{\mu_{eff}C_{ox}W_m} \tag{4.7}$$

If $\frac{1}{Beta}$ is plotted against L_m, then the intercept of the best fit straight line with the L_m axis is $2L_d$.

The width reduction ΔW is due to the bird's beak formed in the LOCOS isolation process. It reduces the mask width W_m to the actual width W.

$$W = W_m - 2\Delta W \tag{4.8}$$

The extraction of ΔW is similar to L_d, so the *Beta* values for various width devices have to be found from their transfer characteristics. The bias condition is the same as that for L_d extraction.

$$Beta = \mu_{eff} C_{ox} \frac{W_m - 2\Delta W}{L_m - 2L_d} \tag{4.9}$$

So,

$$Beta = \mu_{eff} C_{ox} \frac{W_m}{L_m - 2L_d} - \mu_{eff} C_{ox} \frac{2\Delta W}{L_m - 2L_d} \tag{4.10}$$

This shows that $2\Delta W$ is the intercept on the W_m axis when plotting *Beta* against W_m.

The procedure of extracting the subthreshold gate swing S from experimental data is as follows:

1. Measure the $I_D - V_G$ curve in the subthreshold region.

2. Chose a certain normalized drain current $I_0 = I_D/(W/L)$ from the subthreshold characteristic, such as $I_0 = 10^{-9}$A, that is $I_D = 10^{-9}(W/L)$A. Then chose three points from the measured data (I_{D-1}, V_{G-1}), (I_{D0}, V_{G0}) and (I_{D1}, V_{G1}), which satisfy $I_{D-1} < I_D(= I_0(W/L)) < I_{D0} < I_{D1}$ and $V_{G0} - V_{G-1} = V_{G1} - V_{G0}$.

3. Let $y = \lg I_0$;
   $x_{-1} = V_{G-1}$, $y_{-1} = \lg(I_{D-1}/(W/L))$;
   $x_0 = V_{G0}$, $y_0 = \lg(I_{D0}/(W/L))$;
   $x_1 = V_{G1}$, $y_1 = \lg(I_{D1}/(W/L))$. See Fig. 4–27.

4. Use inverse interpolation and differentiation of the three-point Stirling formula [113] to find x corresponding to y, i.e. the gate voltage V_G corresponding to the chosen current I_D and to compute the subthreshold slope $n = \frac{d \lg I_D}{dV_G}$ (decade/V) $= \frac{dy}{dx}$ at this chosen point (I_D, V_G). So the subthreshold gate swing $S = 1000 \cdot \frac{1}{n}$ (mV/decade).

The three-point Stirling formula is as follows:

$$y = y_0 + \frac{u}{2}(y_1 - y_{-1}) + \frac{u^2}{2}(y_1 - 2y_0 + y_{-1}) \tag{4.11}$$

where $y = f(x)$, $y_{-1} = f(x_{-1})$, $y_0 = f(x_0)$ and $y_1 = f(x_1)$. f is a unknown function. y is known. (x_{-1}, y_{-1}), (x_0, y_0) and (x_1, y_1) are three known points with equal interval $h = x_{n+1} - x_n$. They satisfy $y_{-1} < y < y_0 < y_1$. x is to be found.

$$x = x_0 + uh \tag{4.12}$$

From Eq. (4.11), u can be easily found by solving a quadratic equation. So x is found from Eq. (4.12).

The derivative $\frac{dy}{dx}$ can be derived as follows:

$$\frac{dy}{dx} = \frac{dy}{du}\frac{du}{dx} \tag{4.13}$$

From Eq. (4.12),

$$\frac{dy}{dx} = \frac{1}{h}\frac{dy}{du} \tag{4.14}$$

From Eq. (4.11),

$$\frac{dy}{dx} = \frac{1}{h}[\frac{1}{2}(y_1 - y_{-1}) + u(y_1 - 2y_0 + y_{-1})] \tag{4.15}$$

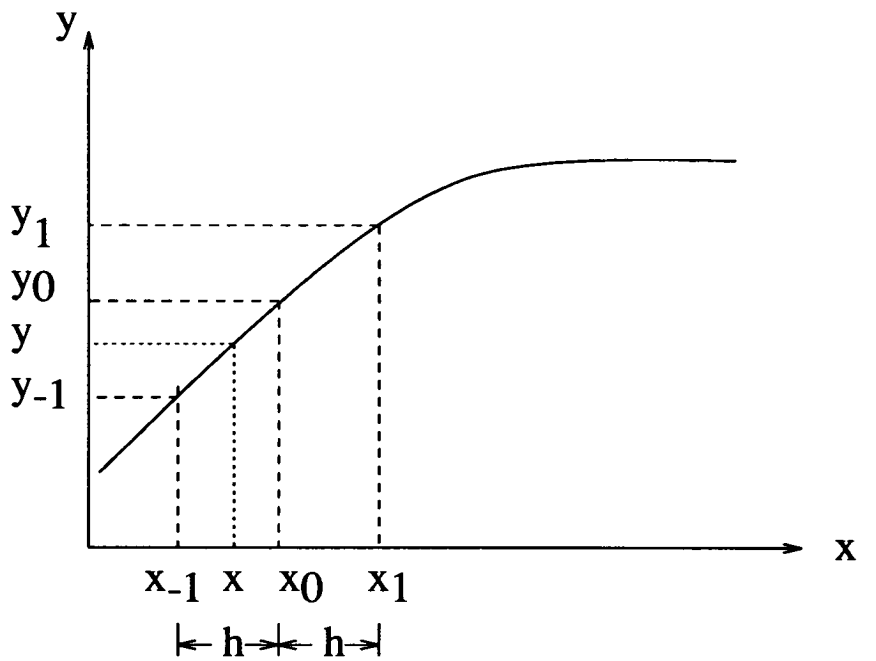


Figure 4–27: Diagram about extraction of S

Chapter 5

Ion Implantation and Subthreshold Behaviour

5.1 Ion Implantation and Subthreshold Behaviour of Long-Channel MOSFETs

It has been discussed in Chapter 2 that the channel ion implantation will affect the subthreshold gate swing S greatly. We will analyze its impact on long-channel MOSFETs first.

The values of the subthreshold gate swing S obtained from the subthreshold characteristics at normalized current level $I_0 \equiv I_D/(W/L) = 10^{-9}$A of Device A on each wafer are listed in Table 5.1.1.

From Table 5.1.1, it is clear that wafer group 1 consists of 3 wafers which have a single implant and have the same shallow implantation energy of 25keV. The subthreshold gate swing S increases substantially from 68.82 to $91.42mV/decade$ when the implantation dose increases from $2e11cm^{-2}$ to $7e11cm^{-2}$.

Wafer group 2 consists of 4 wafers which also have a single implant and have the same implantation dose of $7e11cm^{-2}$. When implantation energy increases from 10keV to 25keV, S increases from 80.99 to $91.42mV/decade$. Then S decreases while the energy increases.

Table 5.1.1 S and Ion Implantation

group of wafers	wafer No.	$Dose_1$ (cm^{-2})	$Energy_1$ (keV)	$Dose_2$ (cm^{-2})	$Energy_2$ (keV)	S (mV/decade)
	1	2e11				68.82
1	2	5e11	25	–	–	79.42
	4	7e11				91.42
	3		10			80.99
2	4	7e11	25	–	–	91.42
	5		50			85.39
	6		100			82.95
	7	3e11				83.82
3	8	5e11	25	7e11	140	86.46
	11	7e11				89.76
	9		10			86.52
4	10	7e11	15	7e11	140	88.39
	11		25			89.76
	12		50			88.36
	14				100	92.92
5	11	7e11	25	7e11	140	89.76
	15				200	87.42
6	13	7e11	25	5e11	140	89.60
	11			7e11		89.76

This can be explained by our theory in Section 2.4.2 (Eq.(2.71)). From Eq. (B.10), when the implant is very shallow, the edge of the depletion layer lies in the uniformly doped substrate. w_d thus S is determined by the implant dose, substrate doping and oxide thickness. Initially as the implant depth increases, w_d decreases thus S increases. However, once w_d is reduced to the point that it meets the edge of the implant depth, w_d reaches its minimum value thus S reaches its maximum. As the implant is made deeper, w_d begins to increase thus S decreases.

Wafer group 3 has 4 wafers which are double-implanted and have the same deep implantation dose of 7e11cm^{-2}, energy of 140keV and shallow implantation energy of 25keV. When their shallow implantation dose increases from 3e11cm^{-2} to 7e11cm^{-2}, S increases from 83.82 to 89.76$mV/decade$. Comparing with wafer group 1, one can conclude that deep implantation reduces the sensitivity of S to the shallow implantation dose but increases the value of S.

Wafer group 4 includes 4 wafers which are double-implanted and have the same deep implantation as in group 3 and the same shallow implantation dose of 7e11cm^{-2}. The dependency of S on the shallow implantation energy has the same tendency as in group 1 and comparing with group 2, the conclusion is also similar to the comparison between group 3 and group 1.

Wafer group 5 consists of 3 wafers which are double-implanted and have the same shallow implantation dose of 7e11cm^{-2}, energy of 25keV and deep implantation dose of 7e11cm^{-2}. When their deep implantation energy increases from 100keV to 200keV, S drops from 92.92 to 87.42$mV/decade$.

Wafer group 6 has 2 wafers which are double-implanted and they have the same shallow implantation as in group 5 and the deep implantation energy of 140keV. When their deep implantation dose increases from 5e11cm^{-2} to 7e11cm^{-2}, S only rises slightly from 89.60 to 89.76$mV/decade$.

From the above experimental results, one can conclude that shallow implantation has a bigger influence on the subthreshold behaviour of a MOSFET than deep implantation. Shallow implantation dose has a bigger influence on the subthreshold behaviour of a MOSFET than shallow implantation energy.

Now, we will compare the experimental results for subthreshold gate swing S with the theoretical results from the model presented in Section 2.4.2 For our theoretical calculation, we will use four different channel doping profile approximations and compare their results with the experimental results. The four doping profile approximations are:

1. Step doping profile approximation [114]. That is, the doping profile in the

double implanted channel of a MOSFET is

$$N(x) = \begin{cases} N_{AS} + N_A & x \leq w_S \\ N_{AB} + N_A & w_S < x \leq w_S + w_B \\ N_A & x > w_S + w_B \end{cases} \tag{5.1}$$

where N_A is the substrate concentration. $x = 0$ at the oxide–silicon interface. w_S and w_B are the width of the step doping profiles and have forms

$$w_S = R_{p1} - t_{ox}\frac{\Delta R_{p1}}{\Delta R_{pox1}} + 2\Delta R_{p1} \tag{5.2}$$

$$w_S + w_B = R_{p2} - t_{ox}\frac{\Delta R_{p2}}{\Delta R_{pox2}} + 2\Delta R_{p2} \tag{5.3}$$

where t_{ox} is the thickness of gate oxide. R_p and ΔR_p are the projected range and the projected standard deviation of Boron implanted into Silicon. ΔR_{pox} are the projected standard deviation of Boron implanted into Oxide. Subscripts 1 and 2 refer to parameters of shallow and deep implantation respectively. N_{AS} and N_{AB} are the average shallow and deep implanted concentration.

$$N_{AS} = \frac{1}{w_S}\int_0^{w_S} \frac{D_{I1}}{\sqrt{2\pi}\Delta R_{p1}} \exp\left\{-\left[\frac{x - R_{p1} + t_{ox}\frac{\Delta R_{p1}}{\Delta R_{pox1}}}{\sqrt{2}\Delta R_{p1}}\right]^2\right\} dx \tag{5.4}$$

$$N_{AB} = \frac{1}{w_B}\int_{w_S}^{w_S+w_B} \frac{D_{I2}}{\sqrt{2\pi}\Delta R_{p2}} \exp\left\{-\left[\frac{x - R_{p2} + t_{ox}\frac{\Delta R_{p2}}{\Delta R_{pox2}}}{\sqrt{2}\Delta R_{p2}}\right]^2\right\} dx \tag{5.5}$$

where D_I is the implantation dose. See Fig. 5–1.

2. Gaussian distribution [115,110]. That is,

$$N(x) = N_A + \sum_{i=1}^{2} \frac{D_{Ii}}{\sqrt{2\pi}\Delta R_{pi}} \exp\left\{-\left(\frac{x - R_{pi} + t_{ox}\frac{\Delta R_{pi}}{\Delta R_{poxi}}}{\sqrt{2}\Delta R_{pi}}\right)^2\right\} \tag{5.6}$$

3. Gaussian distribution including the annealing effect [110]. This annealing effect expression comes from the analytical solution of the diffusion equation assuming an extension of the semiconductor from $-\infty$ to $+\infty$. We only need replace ΔR_p in Eq. (5.6) by the effective projected standard deviation

$$\Delta R_p' = \sqrt{\Delta R_p^2 + 2Dt} \tag{5.7}$$

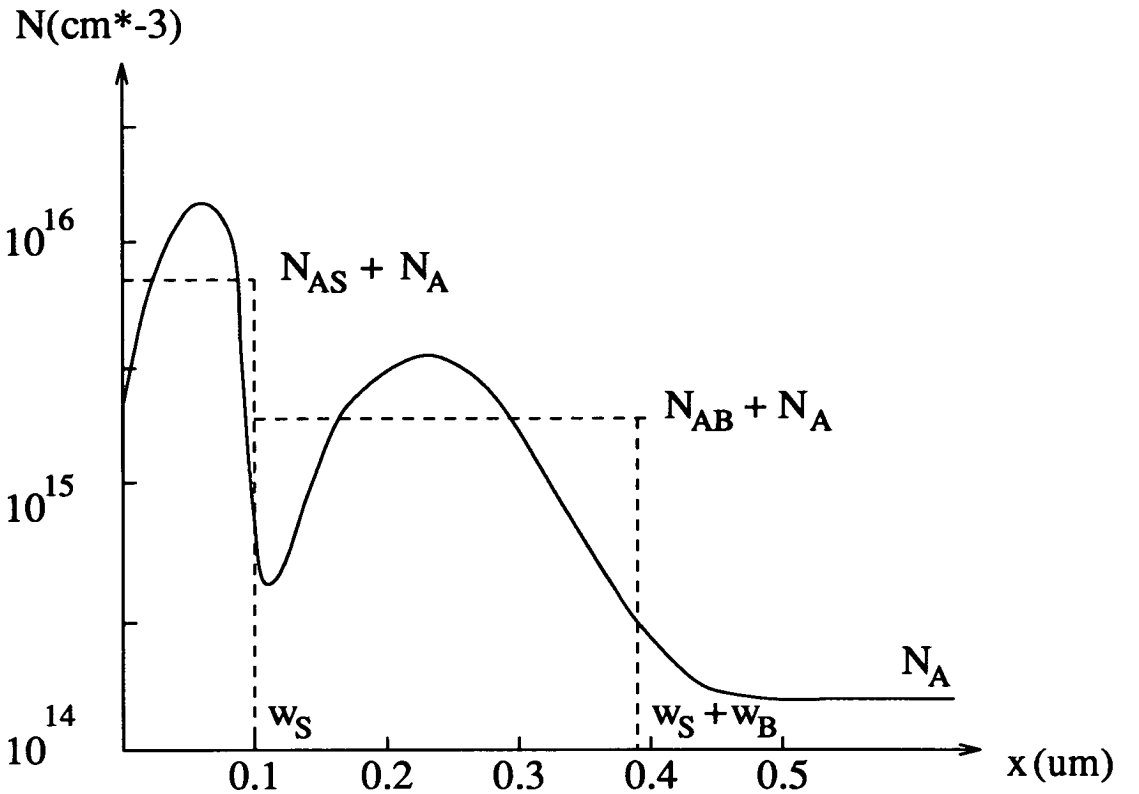


Figure 5–1: Step profile approximation

where Dt is the sum of the product of diffusion coefficient by diffusion time at all thermal diffusion steps, namely $Dt = \sum_i D_i t_i$.

4. Gaussian distribution after annealing. The distribution is the analytical solution of the diffusion equation considering the boundary condition as $[\frac{\partial N}{\partial x}]_{x=0} = 0$ [115,110]. We have

$$N(x) = N_A + \sum_{i=1}^{2}[R_i(A,x) + R_i(A,-x)] \tag{5.8}$$

where

$$R_i(A,x) = \frac{1}{2}\frac{D_{Ii}}{\sqrt{2\pi}\Delta R'_{pi}} \exp\left[-\frac{(x-A)^2}{2\Delta R'^2_{pi}}\right] \text{erfc}\left[-\frac{2DtA + x\Delta R^2_{pi}}{2\Delta R_{pi}\Delta R'_{pi}\sqrt{Dt}}\right] \tag{5.9}$$

$$A = R_{pi} - t_{ox}\frac{\Delta R_{pi}}{\Delta R_{oxi}} \tag{5.10}$$

The results from the theory by using above four approximations of the channel doping profile are compared with experimental results in Fig. 5–2.

The relative errors(%) between experimental and theoretical results are plotted in Fig. 5–3.

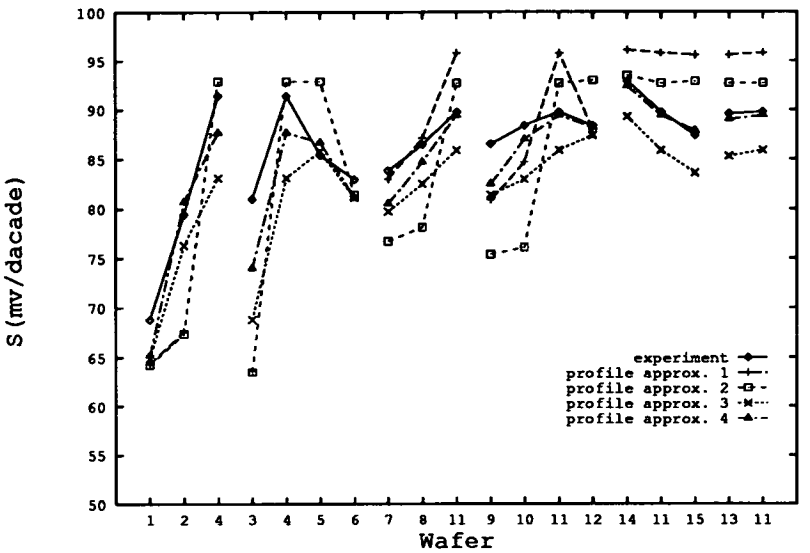


Figure 5–2: Compare S of experiment and theory

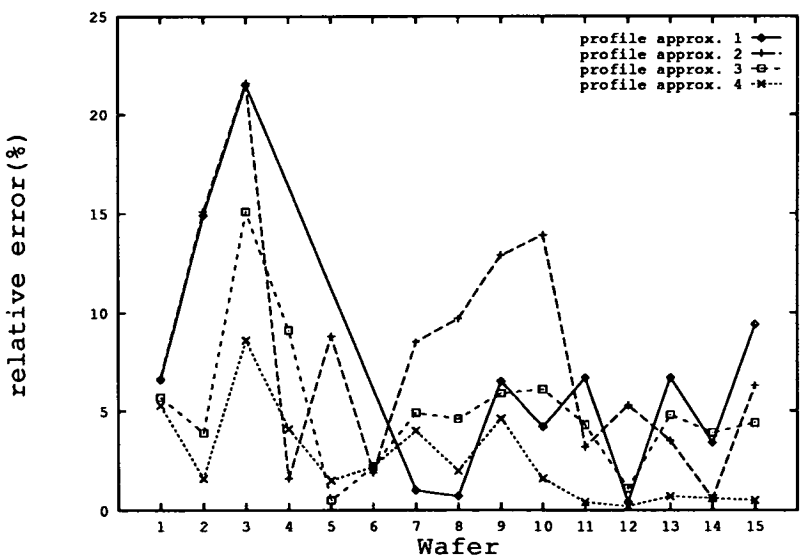


Figure 5–3: Relative error between experimental and theoretical results

It is clear from Fig. 5–3 that the theoretical results using the 4th channel profile approximation agree with the experimental results excellently. The average relative error by using approximations 1 to 4 is 6.8%, 8.0%, 5.1%, 2.5%, respectively. The maximum relative error by using approximations 1 to 4 is 21.5%, 21.6%, 15.1% and 8.6% respectively. Theoretical values of S using the step doping profile approximation for Wafers 4, 5, 6 are not available because difficulties in calculating depletion depth w_d arise from the discontinuity of doping profile $N(x)$ at w_S caused by this approximation (See Appendix B).

Since using the fourth channel profile approximation offers the best agreement with the experimental results, it has been used in our short-channel model in Chapter 3.

5.2 Ion Implantation and Subthreshold Behaviour of Short-Channel MOSFETs

Fig. 5–4 plots the subthreshold gate swing S for Devices A, B, C, D on each wafer. Changes of S against the implantation conditions for a short-channel transistor have the same trends as for a long-channel device. However, the implantation has the biggest impact on the subthreshold gate swing S of the shortest device, i.e. Device D.

5.3 Ion Implantation and Subthreshold Behaviour of Narrow-Channel MOSFETs

Fig. 5–5 plots the subthreshold gate swing S for Devices E, F, G, H on each wafer. Changes of S against the implantation for a narrow-channel transistor have the same trend as for a wide-channel device. The effect of implantation conditions on the subthreshold gate swing, S, of a wide-channel device is not obviously different from that of a narrow-channel device.

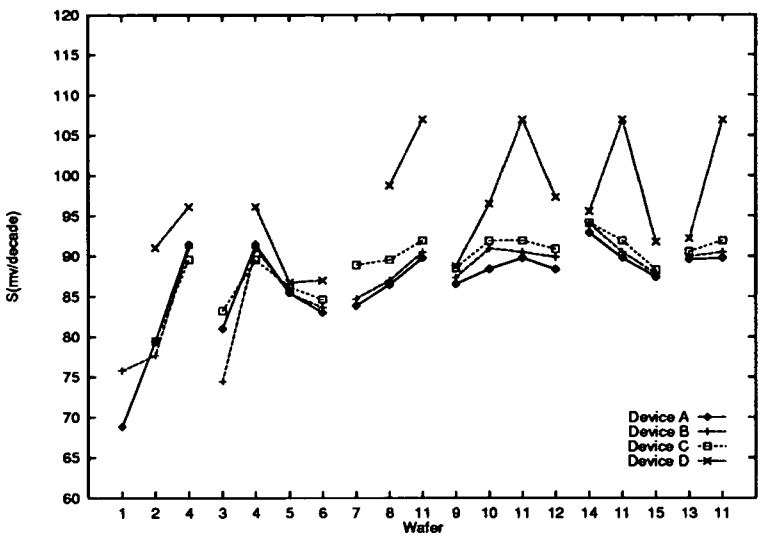


Figure 5–4: Experimental S for short-channel device on each wafer

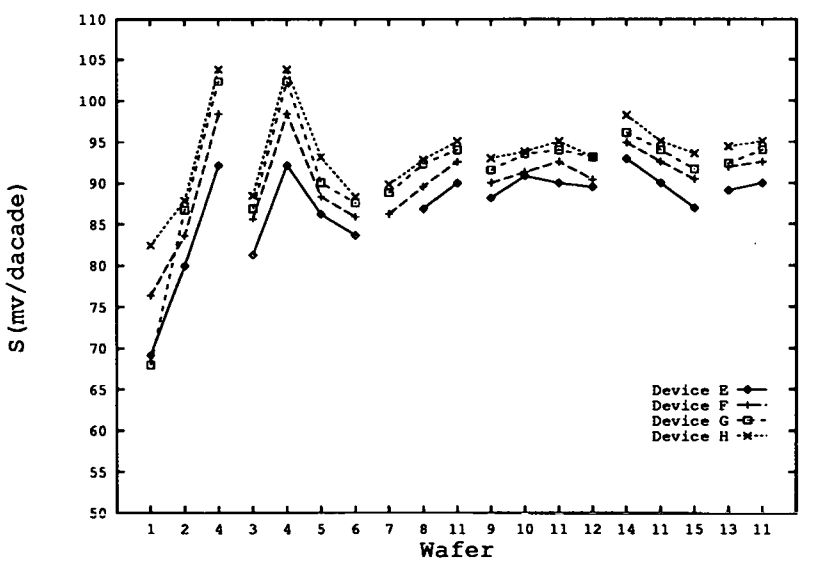


Figure 5–5: Experimental S for narrow-channel device on each wafer

5.4 Annealing Temperature, Time and Subthreshold Behaviour

Theoretical results in Section 5.1 show that the thermal annealing steps do have an effect on the subthreshold gate swing S, since they change the profile of the channel doping, especially that of an implant with high dose and low energy. The biggest percentage difference of S between considering the annealing affect or ignoring it is 19.7%. In this section, we concentrate on the effect of annealing temperature and time on S. Fig. 5–6 shows how the subthreshold gate swing S changes with the annealing time. Basically, the effect of the annealing time on S is not substantial. The change of the annealing time has a stronger influence on an implantation with low energy and high dose than on an implantation with a high energy and low dose. For implantation with 1) energy 25keV, dose 7e11cm^{-2}, 2) energy 50keV, dose 7e11cm^{-2}, 3) energy 50keV, dose 3e11cm^{-2}, 4) energy 140keV, dose 7e11cm^{-2}, when the annealing time changes from 10min to 200min, the changes in S are 3.7%, 2.9%, 3.3% and 0.4%, respectively.

Fig. 5–7 shows that for a certain ion implantation, the higher the annealing temperature, the smaller is the value of S. Any change in annealing temperature has a stronger influence on an implantation with low energy and high dose than on an implantation with high energy and low dose. For implantation with 1) energy 25keV, dose 7e11cm^{-2}, 2) energy 50keV, dose 7e11cm^{-2}, 3) energy 50keV, dose 5e11cm^{-2}, 4) energy 140keV, dose 7e11cm^{-2}, 5) energy 140keV, dose 5e11cm^{-2}, when the annealing temperature changes from 600°C to 1400°C, the changes in S are 28.0%, 27.9%, 25.4%, 13.0% and 12.7%, respectively.

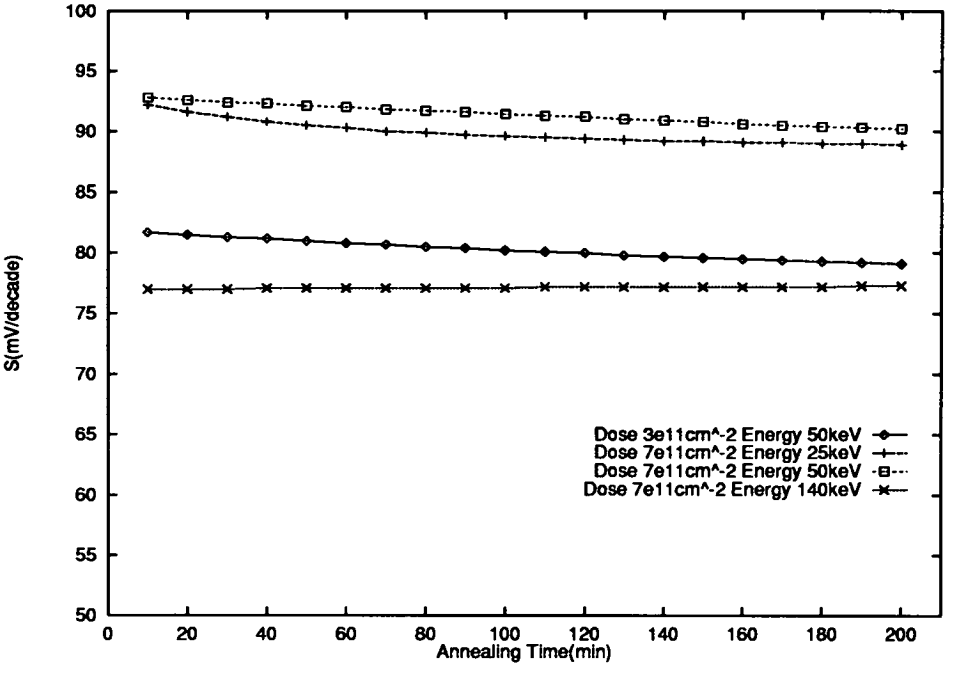


Figure 5–6: S vs annealing time at annealing temperature 900°C, $I_0 = 1\text{nA}$, $N_A = 4e14/cm^3$, $V_B = V_S = 0$, $V_D = 0.1\text{V}$

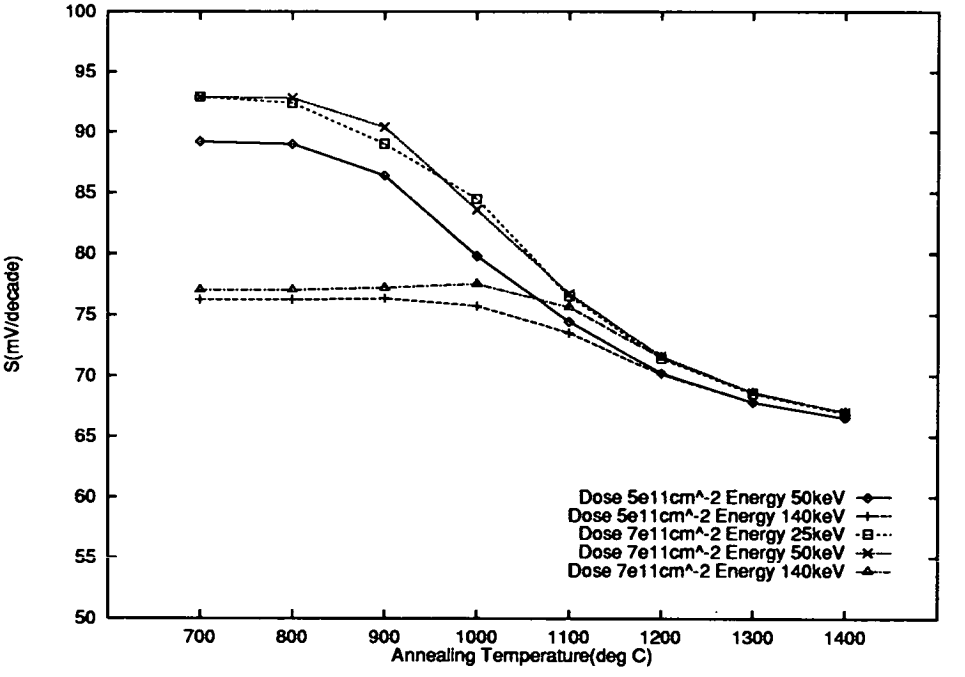


Figure 5–7: S vs annealing temperature at annealing time 180min

Chapter 6

Terminal Voltage and Subthreshold Behaviour

6.1 Gate Voltage V_G

Figs. 6–1 to 6–4[2] show the semi-logarithm plot of subthreshold $I_D - V_G$ characteristics with V_B as a parameter for our experimental devices. We have measured eight devices on each of the fifteen wafers. Although the measured values for each device are all different, they do look similar as graphics. To save space, the subthreshold characteristics of only four devices on wafer 11 are shown here as examples. It is clear that the subthreshold drain current I_D increases exponentially with gate voltage V_G. This agrees with the theoretical prediction (Eq. (2.58)).

However, the subthreshold gate swing S dose not remain a constant while V_G changes. Using the theory given in Section 2.4.2, we calculated the subthreshold gate swing S against the normalized drain current level I_0 of the long-channel device A on each wafer at $V_B = 0$ and $V_B = -2$V. It is clear that S decreases when V_G increases, i.e. I_0 increases. The change of S with V_G is smaller at a higher value of V_B than at a lower one. See Figs. 6–5 to 6–10.

For single-implant wafers, the percentage difference between S at $I_0 = 10^{-12}$A and S at $I_0 10^{-6}$A, ΔS, ranges from 6.7% to 24.3% when $V_B = 0$. When

[2] Figs. 6-1 to 6-4 are identical with Figs.4-21 to 4-24 and are being repeated for convenience.

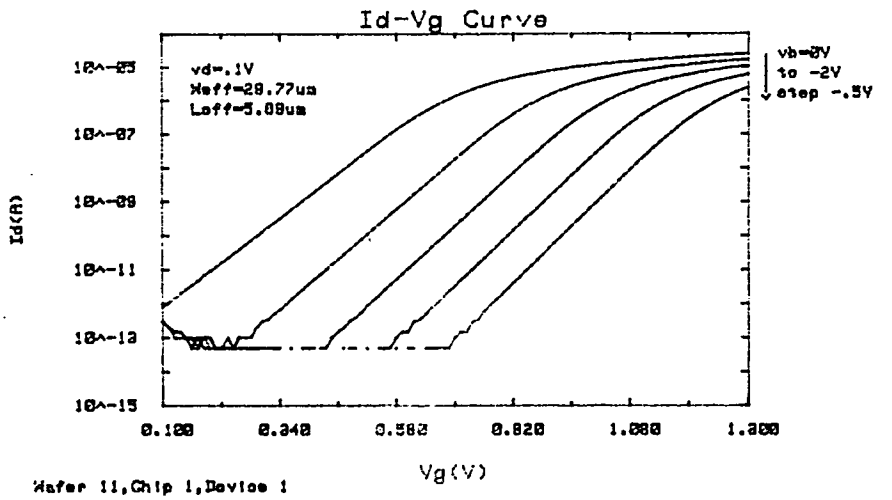


Figure 6–1: Subthreshold characteristic of Wafer 11 Device A

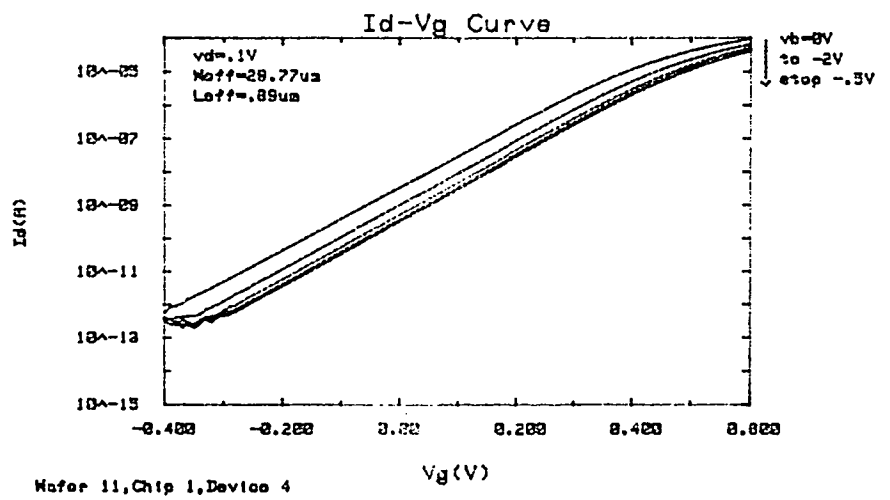


Figure 6–2: Subthreshold characteristic of Wafer 11 Device D

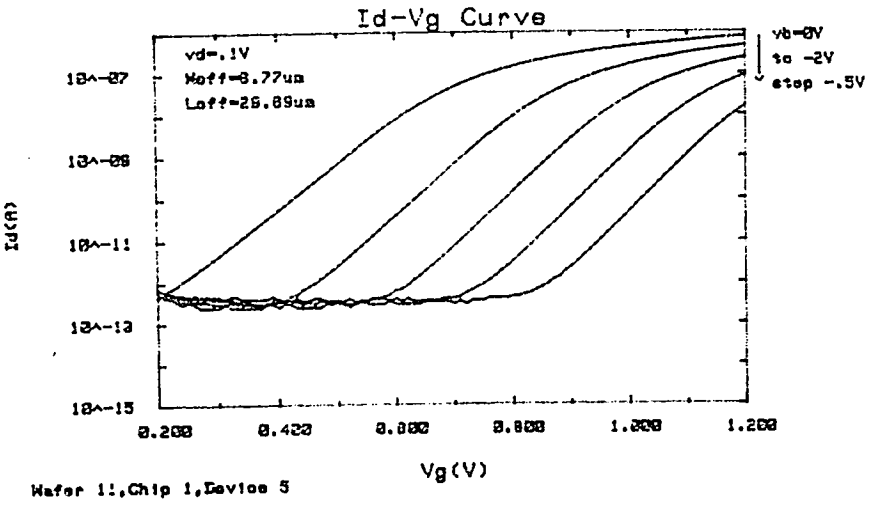


Figure 6–3: Subthreshold characteristic of Wafer 11 Device E

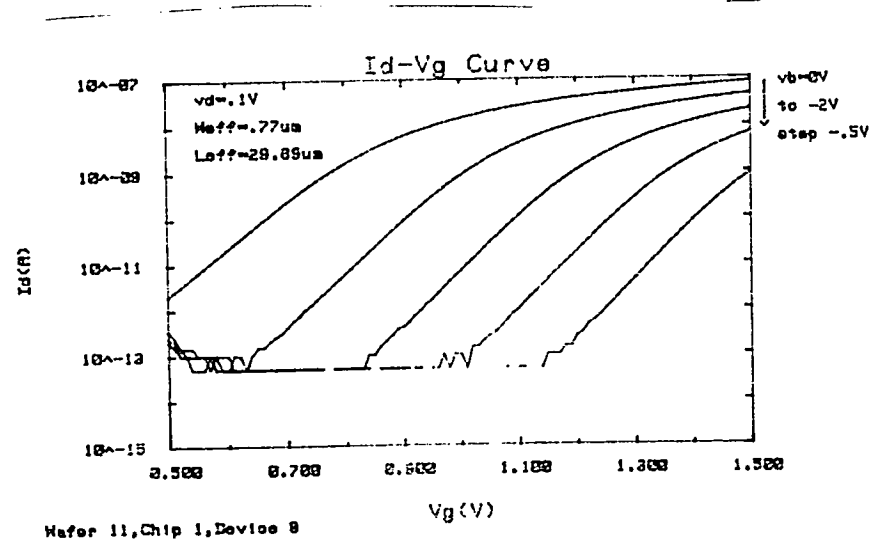


Figure 6–4: Subthreshold characteristic of Wafer 11 Device H

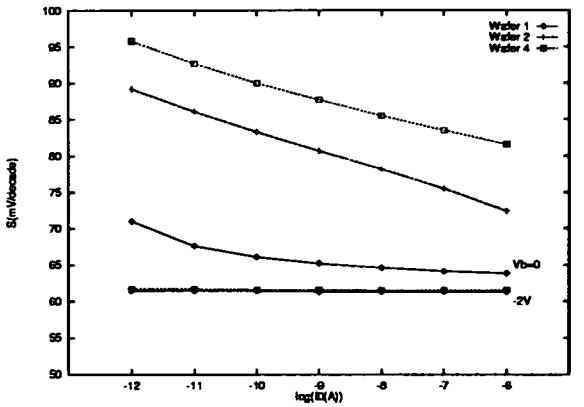


Figure 6–5: Theoretical S vs I_0 for wafer group 1

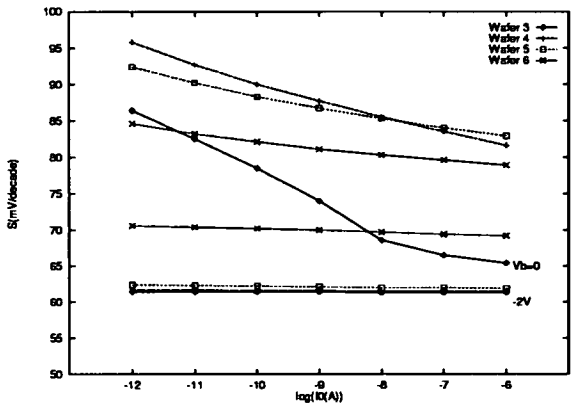


Figure 6–6: Theoretical S vs I_0 for wafer group 2

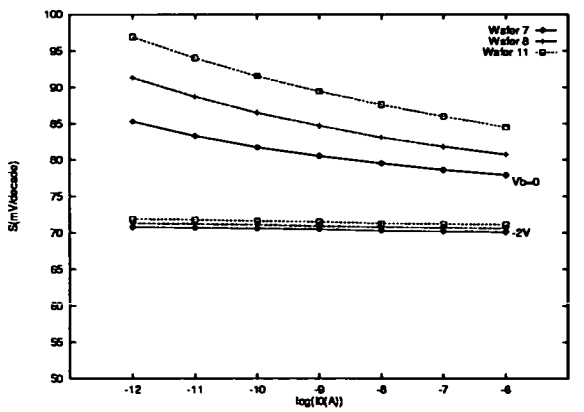


Figure 6–7: Theoretical S vs I_0 for wafer group 3

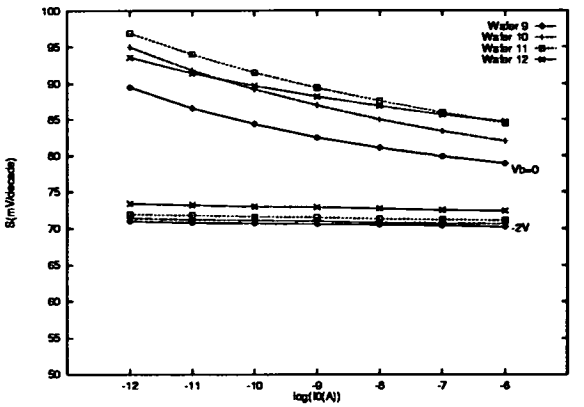


Figure 6–8: Theoretical S vs I_0 for wafer group 4

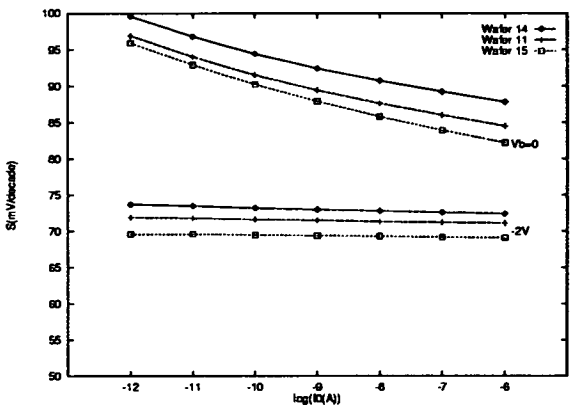


Figure 6–9: Theoretical S vs I_0 for wafer group 5

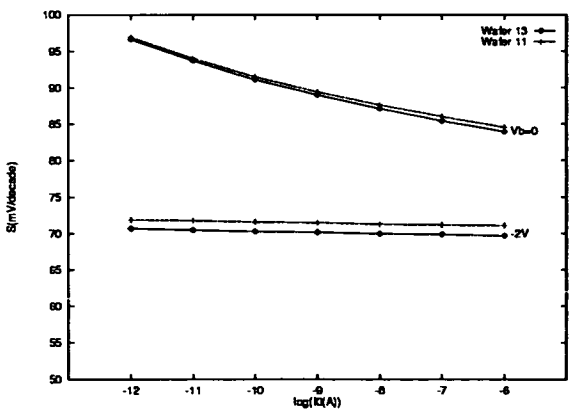


Figure 6–10: Theoretical S vs I_0 for wafer group 6

$V_B = -2$V it varies from 0.2% to 2.0%. For double implanted wafers, ΔS ranges from 8.7% to 14.3% when $V_B = 0$. When $V_B = -2$V it varies from 0.7% to 1.8%. See Fig. 6–11.

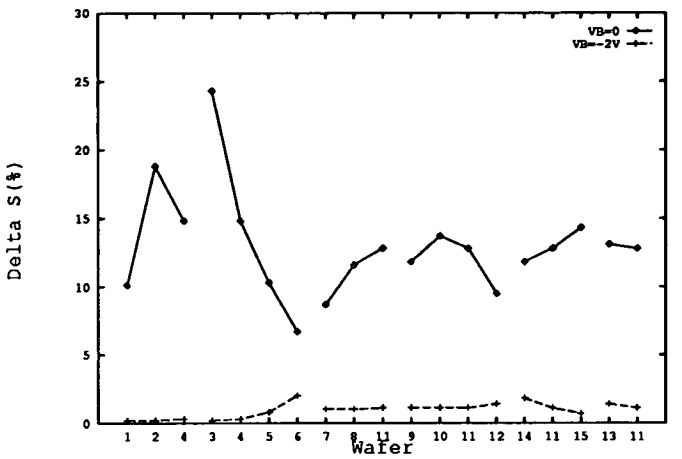


Figure 6–11: Theoretical ΔS for device A on each wafer

Fig. 6–12 shows experimental results of the relation between S and I_0 (i.e. V_G). Again, to save space, only results for wafer 11 are shown as an example. It is clear in Fig. 6–12 that for long-channel devices S decreases when V_G increases at $I_0 < 10^{-9}$A. Then after I_0 reaches 10^{-9}A, S increases with V_G. For short-channel devices, the increase in S begins at a lower current level. This is because when V_G approaches the threshold voltage V_T, the drain current I_D is no longer dominated by diffusion current. The drift current is then comparable with the diffusion current. So the drain current no longer increases exponentially with gate voltage V_G. It changes to a linear dependency on V_G gradually. Therefore ΔS is not as large as predicted in the subthreshold theory but it is within 10% for all our experiments. Thus, we can consider that S does not change with V_G in a device model for circuit simulation.

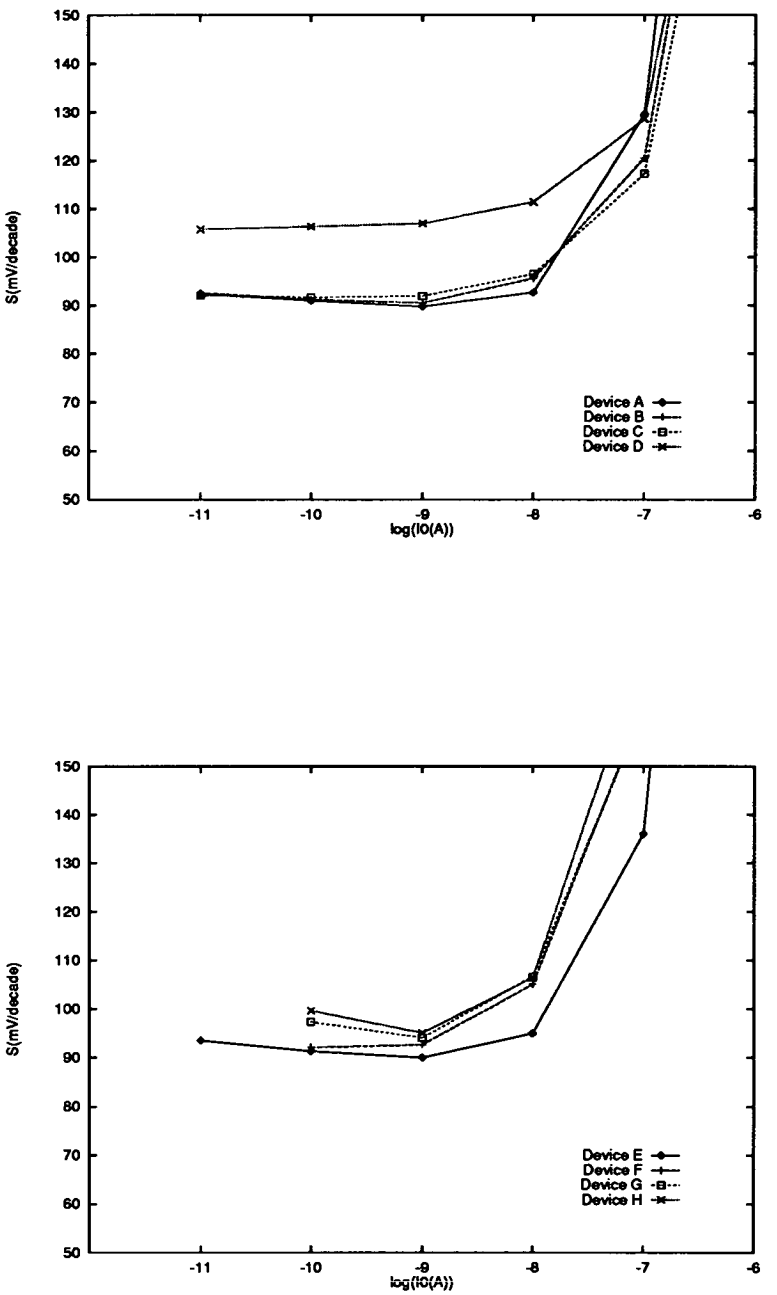


Figure 6–12: Experimental S vs I_0 of device A – H on wafer 11

6.2 Substrate Bias V_B

From Figs. 6–1 to 6–4, it is clear that the subthreshold drain current I_D decreases while the value of the substrate bias $|V_B|$ increases. This agrees with the theory(Eq. (2.58)). Furthermore, we also observe that the change in drain current (ΔI_D) for the same substrate bias change, ΔV_B, is smaller at a higher value of $|V_B|$ than at a lower one. ΔI_D at the same ΔV_B is smaller at a higher gate voltage V_G than at a smaller one. When the channel length L decreases, the influence of V_B on I_D decreases as well. All those phenomena can be explained as follows:

Using the same procedure of deriving S for long-channel device in Chapter 2, we have

$$\begin{aligned} \frac{d\ln I_D}{dV_B} &= \frac{d\ln_D}{dw_d}\frac{dw_d}{dV_B} \\ &= \frac{d}{dw_d}(\beta\psi_s - \ln\mathcal{E}_s + \beta V_B) \Big/ \frac{dV_B}{dw_d} \end{aligned} \tag{6.1}$$

From relation $C_{ox}(V_G - V_B - V_{FB} - \psi_s) = \epsilon_{si}\mathcal{E}_s$, one has

$$\frac{dV_B}{dw_d} = -\left(\frac{d\psi_s}{dw_d} + \frac{\epsilon_{si}}{C_{ox}}\frac{d\mathcal{E}_s}{dw_d}\right) \tag{6.2}$$

Finally,

$$\frac{d\ln I_D}{dV_B} = \frac{\beta\left(\frac{t_{ch}}{w_d} + \frac{C_D}{C_{ox}}\right)}{\left(1 + \frac{C_D}{C_{ox}}\right)} \tag{6.3}$$

Usually, $t_{ch} \ll w_d$, thus

$$\frac{d\ln I_D}{dV_B} \approx \frac{\beta}{\left(1 + \frac{C_{ox}}{C_D}\right)} \tag{6.4}$$

When the value of the substrate bias $|V_B|$ increases, the depletion width w_d increases, thus the capacitance of the semiconductor depletion layer C_D decreases. From above formula, $\frac{d\ln I_D}{dV_B}$ decreases. When the gate voltage V_G increases, the surface potential ψ_s increases, so w_d increases, thus $\frac{d\ln I_D}{dV_B}$ decreases. When the channel length L decreases, w_d increases thus $\frac{d\ln I_D}{dV_B}$ decreases.

We also notice that when the channel width, W, decreases, the influence of V_B on I_D does not have a noticeable change.

Fig. 6–13 illustrates experimental results of S vs V_B. Again, to save space, only result for wafer 11 is shown here as an example. The change of S (ΔS) for a small fixed substrate bias change, ΔV_B, is smaller at higher values of $|V_B|$ than at lower ones. When the channel length L decreases, the influence of V_B on S decreases as well. When the channel width W decreases, the influence of V_B on S does not have a noticeable change. The percentage changes of S between $V_B = 0$ and $V_B = -2$V at $I_0 = 10^{-9}$A for all experimental devices are plotted in Fig. 6–14.

In the SPICE level 3 MOS model, the effect of the substrate bias V_B on the subthreshold behaviour is not considered. If a MOSFET is always operated under the condition that the source is biased at the same potential as the substrate, then this assumption will not cause any problem. But in a VLSI circuit, the source of a MOSFET is not always at the same potential as the substrate. So the influence of the substrate bias V_B on the subthreshold behaviour has to be taken into account..

For a long-channel MOSFET, from Eq. (2.71)

$$S = \frac{1}{\beta}(\ln 10)\left(1 + \frac{C_D}{C_{ox}}\right) / \left(1 - \frac{t_{ch}}{w_d}\right) \quad . \tag{6.5}$$

where $C_D = \epsilon_{si}/w_d$, $C_{ox} = \epsilon_{ox}/t_{ox}$ and $t_{ch} \ll w_d$ normally. Thus

$$S \approx \frac{1}{\beta}(\ln 10)\left(1 + \frac{\epsilon_{si}}{C_{ox}}\frac{1}{w_d}\right) \tag{6.6}$$

To make things simple, let us use the depletion width of a device with uniformly doped long-channel as a first order approximation. That is

$$w_d = \sqrt{\frac{2\epsilon_{si}\psi_s}{qN_A}} \tag{6.7}$$

For a device with uniformly doped channel,

$$\psi_s = V_G - V_{FB} - V_B - \frac{a^2}{2\beta}\left\{\left[1 + \frac{4\beta}{a^2}(V_G - V_{FB} - V_B)\right]^{\frac{1}{2}} - 1\right\} \tag{6.8}$$

The last term in curly braces is negligible compared with the first three terms.

For a device with a nonuniformly doped channel, using the theory in Section 2.4.2, we calculated the surface potential ψ_s at different substrate bias V_B for

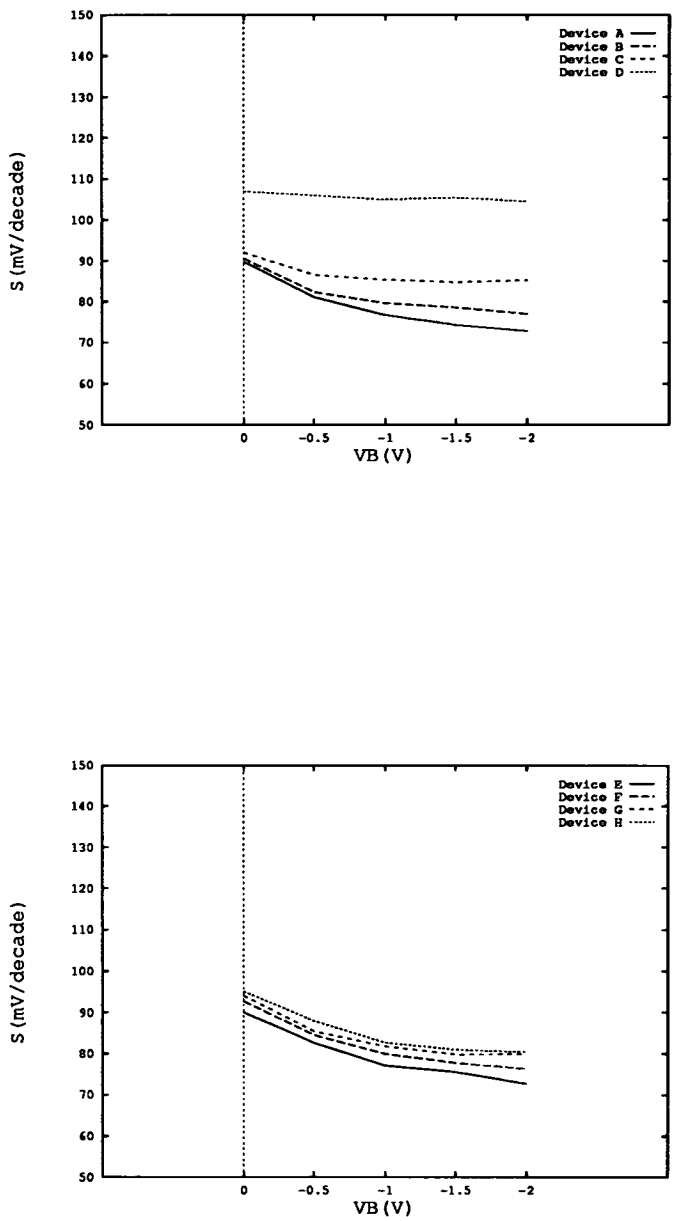


Figure 6–13: Experimental S vs V_B for device A – H on wafer 11

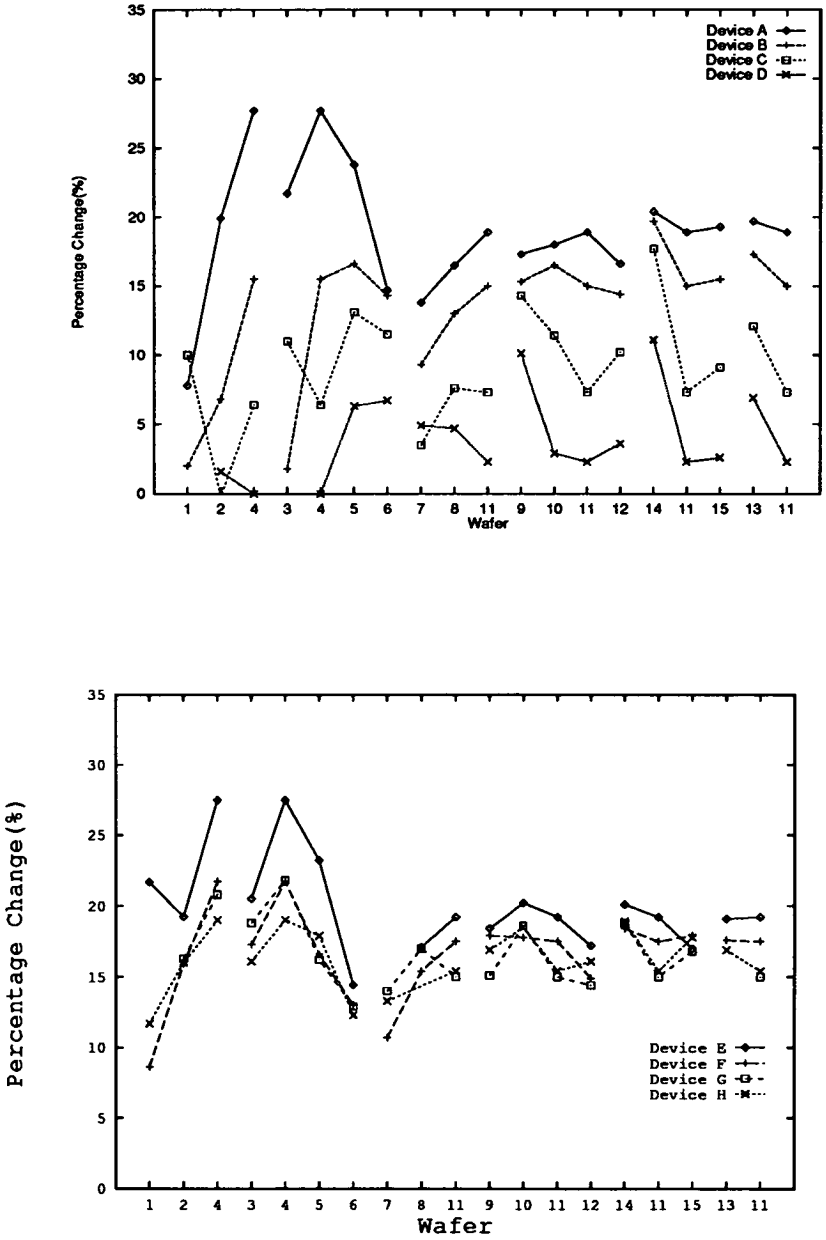


Figure 6–14: Percentage change of S at $V_B = 0$ and $V_B = -2$V

a long-channel device with 15 different implantations, identical with our 15 wafers. They can all be described excellently by

$$\psi_s = \psi_{s0} - V_B \tag{6.9}$$

where $\psi_{s0} \equiv \psi_{s(V_B=0)}$. So,

$$S = \frac{1}{\beta}(\ln 10)\left(1 + \frac{\epsilon_{si}}{C_{ox}}\sqrt{\frac{qN_A}{2\epsilon_{si}}}\frac{1}{\sqrt{\psi_{s0} - V_B}}\right) \tag{6.10}$$

Since the body factor

$$\gamma = \frac{\sqrt{2q\epsilon_{si}N_A}}{C_{ox}} \tag{6.11}$$

So

$$S = \frac{1}{\beta}(\ln 10)\left(1 + \frac{\gamma}{2}\frac{1}{\sqrt{\psi_{s0} - V_B}}\right) \tag{6.12}$$

when $V_B = 0$, let $S_0 \equiv S_{(V_B=0)}$

$$S_0 = \frac{1}{\beta}(\ln 10)\left(1 + \frac{\gamma}{2}\frac{1}{\sqrt{\psi_{s0}}}\right) \tag{6.13}$$

Thus,

$$S = S_0 + \frac{1}{\beta}(\ln 10)\frac{\gamma}{2}\left(\frac{1}{\sqrt{\psi_{s0} - V_B}} - \frac{1}{\sqrt{\psi_{s0}}}\right) \tag{6.14}$$

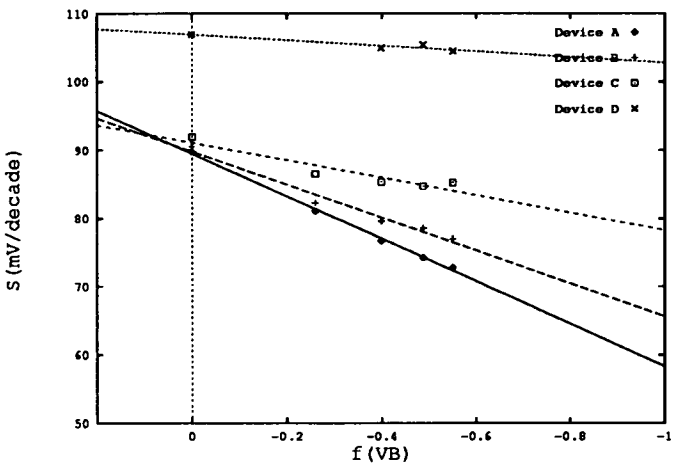
But for a non-uniformly doped MOSFET, calculation of the depletion depth w_d is much more complex and the coefficient $\frac{1}{\beta}(\ln 10)\frac{\gamma}{2}$ in Eq. (6.14) does not agree well with experimental results. Thus we propose a new parameter γ_s, the subthreshold body factor. That is

$$S = S_0 + \gamma_s\left(\frac{1}{\sqrt{\psi_{s0} - V_B}} - \frac{1}{\sqrt{\psi_{s0}}}\right) \tag{6.15}$$

Since S is not sensitive to V_G in reality, it does not matter at which V_G value we calculate S, as long as it is in the subthreshold region. Therefore, we choose $\psi_s = 1.5\psi_B$ in the middle of the subthreshold region. N_A can be calculated from γ because $\gamma = \sqrt{2q\epsilon_{si}N_A}/C_{ox}$ and $\psi_B = \frac{kT}{q}\ln(N_A/n_i)$.

Fig. 6–15 plotted S vs $1/\sqrt{1.5\psi_B - V_B} - 1/\sqrt{1.5\psi_B}$. The slope is γ_s. In Table 6.2.1, the values of γ_s for Device A, B, C, D, E, F, G, H on each wafer are listed.

From Table 6.2.1, the changing trend of γ_s against implantation is the same as that of the subthreshold gate swing S. That is the impact of V_B on S increases with



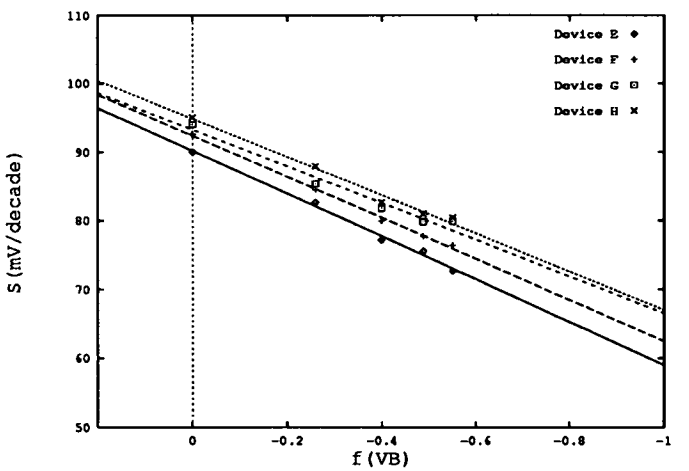


Figure 6–15: S vs $f(-V_B)$

Table 6.2.1 γ_s of Device A, B, C, D, E, F, G, H								
Wafer	A	B	C	D	E	F	G	H
1	7.55	2.00	13.24	–	11.74	8.75	11.11	12.44
2	26.24	8.44	1.05	2.34	25.56	22.09	23.61	22.94
3	24.57	1.88	16.37	62.01	23.53	20.06	19.96	19.57
4	47.28	24.69	9.91	0.03	46.80	38.48	39.15	36.61
5	36.09	27.33	20.64	9.85	35.47	27.01	26.39	29.30
6	20.66	20.26	12.80	10.19	21.00	19.31	19.64	18.68
7	20.37	13.87	8.13	9.86	–	17.90	21.43	21.24
8	24.81	19.96	11.43	7.73	26.21	25.16	27.48	27.47
9	26.07	23.67	22.34	15.71	27.74	26.88	23.55	28.10
10	28.23	27.17	18.13	4.42	32.64	28.65	30.29	30.90
11	31.16	24.18	12.78	4.07	31.16	29.91	26.74	27.81
12	27.08	23.39	15.56	6.84	28.00	25.09	26.47	27.07
13	31.94	28.54	20.89	11.16	30.80	29.78	29.74	29.59
14	35.21	34.40	30.57	20.77	34.46	32.32	33.68	34.90
15	30.47	24.65	14.75	4.83	26.99	29.05	27.57	29.51

implantation dose, and it increases with implantation energy when energy is small (< 25keV for our experimental devices). After it reaches its maximum, it declines when the energy increases. However, Wafers 1 and 3 are exceptions. Because they received the lightest implant dose and lowest implant energy respectively, they have the lowest average doping concentration in the depletion region. Thus punchthrough happens for their short-channel Devices C and D.

6.3 Drain Voltage V_D

Experimental results show that the drain voltage V_D does not affect the subthreshold drain current I_D and thus does not affect the subthreshold gate swing S for a long-channel MOSFET. This agrees with theory.

However, the picture is quite different for a short-channel device. It is clear from the experiment that the subthreshold current I_D increases exponentially with V_D because V_D lowers the potential barrier in the channel. See Figs. 4–25 and 4–26.

Experimental results suggest that for a short-channel device, the subthreshold gate swing S decreases slightly while V_D increases when V_D is small. When V_D increases to a certain value V_{DD}, S begins to increase with V_D. See Fig. 6–16. S does not vary linearly with V_D as suggested by some models in Section 2.6. Instead, we found that if ΔS denotes the change of S when V_D changes by a given amount, then when $V_D < V_{DD}$, S and ΔS decrease when V_D increases. When $V_D > V_{DD}$, S and ΔS increase with V_D. The explanation is that when $V_D < V_{DD}$ surface current dominates subthreshold drain current. w_d increases when V_D increases, thus S decreases from Eq.(3.27). However, when $V_D > V_{DD}$, bulk current begins to dominate subthreshold current. V_G begins to lose its control over drain current, thus S begins to increase.

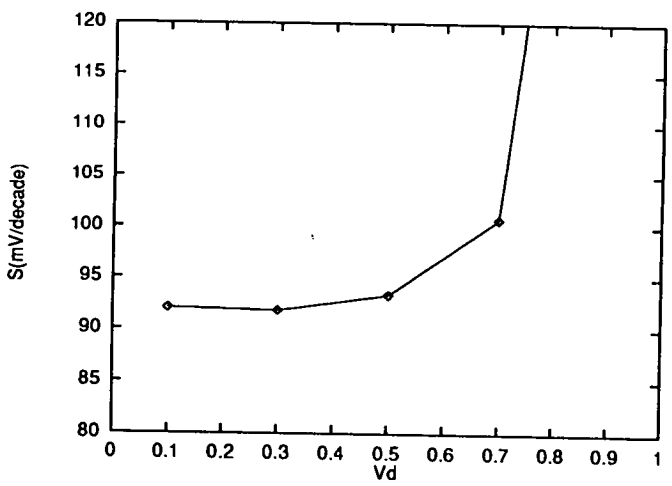


Figure 6–16: Experimental S vs V_D

Chapter 7

Geometry Size and Subthreshold Behaviour

7.1 Channel Length L

From Figs. 6–1 to 6–4, one can see that the subthreshold drain current I_D rises when the channel length L decreases. This agrees with the theoretical work presented in Section 2.4.3. The influence of V_B on I_D decreases with L. It is clear from Figs. 7–1 to 7–6 that S increases while L decreases.

Let us analyse the S–L relationship at $V_B = 0$ first. Define $S_0 \equiv S_{(V_B=0)}$ and $S_{L0} \equiv S_{(V_B=0)}$ of a long-channel MOSFET, assuming

$$S_0 = S_{L0} + \frac{s_c}{L^m} \tag{7.1}$$

Plotting $\ln(S_0 - S_{L0})$ against $\ln L$, then $m = -slope$. The values of m are listed in Table 7.1.1.

The values of m vary widely from 1.6 to 23.3. Thus we do not consider Eq. (7.1) with a fixed value of m to be a good description of the S–L relation.

From the above result, one can see that the dependency of S on L is very strong. The exponential dependence of S on L is most likely and this confirms the

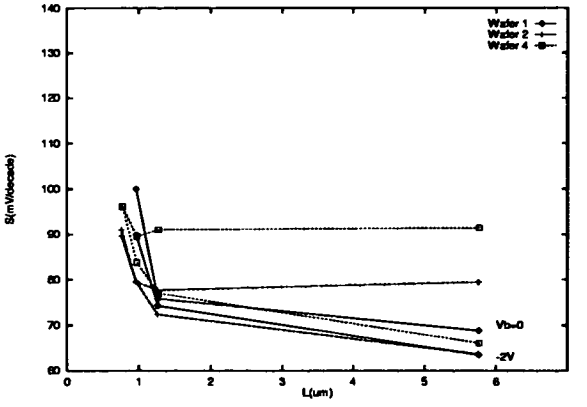


Figure 7–1: S vs. L at $V_B = 0$ and $V_B = -2$V for wafer group 1

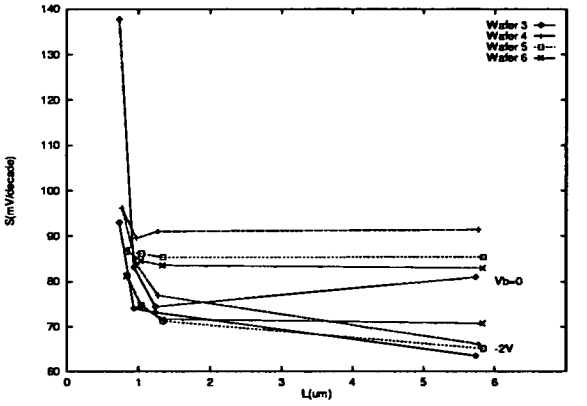


Figure 7–2: S vs. L at $V_B = 0$ and $V_B = -2$V for wafer group 2

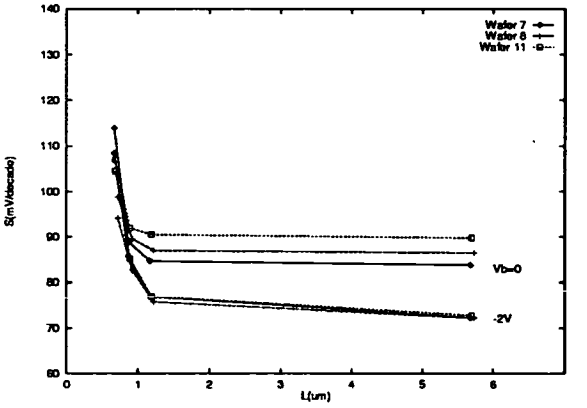


Figure 7–3: S vs. L at $V_B = 0$ and $V_B = -2$V for wafer group 3

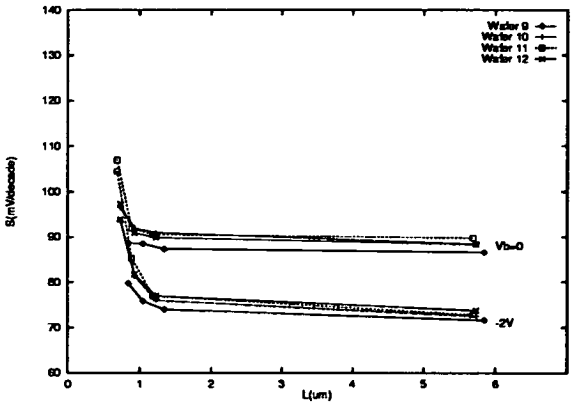


Figure 7–4: S vs. L at $V_B = 0$ and $V_B = -2$V for wafer group 4

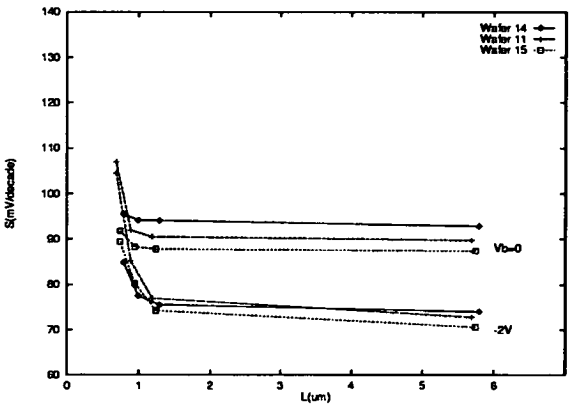


Figure 7–5: S vs. L at $V_B = 0$ and $V_B = -2$V for wafer group 5

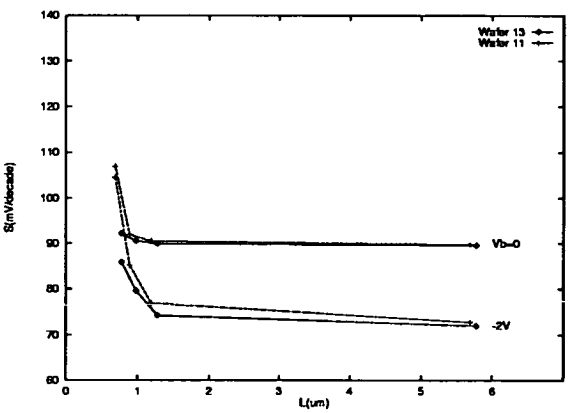


Figure 7–6: S vs. L at $V_B = 0$ and $V_B = -2$V for wafer group 6

Table 7.1.1 m in $S_0 = S_{L0} + s_c/L^m$					
Wafer	m	Wafer	m	Wafer	m
1	5.5	6	3.9	11	5.7
2	23.3	7	8.7	12	3.4
3	13.5	8	6.0	13	4.0
4	5.2	9	2.2	14	1.6
5	2.7	10	2.2	15	4.7

Table 7.1.2 s_l and d_l in $S_0 = S_{L0} + s_l \exp(-L/d_l)$					
Wafer	s_l	d_l	Wafer	s_l	d_l
1	3.8e3	0.20	9	13.7	0.49
2	1.1e10	0.04	10	35.3	0.45
3	8.8e6	0.06	11	800.4	0.17
4	282.5	0.19	12	86.9	0.29
5	15.4	0.34	13	50.9	0.26
6	80.3	0.27	14	7.48	0.65
7	2.8e3	0.14	15	114.6	0.21
8	1.1e3	0.16			

short-channel expression for S we derived in Section 3.2. We use

$$S_0 = S_{L0} + s_l e^{-\frac{L}{d_l}} \tag{7.2}$$

to describe the S–L relation. Plotting $\ln(S_0 - S_{L0})$ against L, we have $d_l = -1/slope$ and $s_l = e^{const}$. Values of s_l and d_l are listed in Table 7.1.2. d_l is a parameter which is an indicator of the depletion depth w_d. A bigger value of d_l indicates a bigger depletion depth w_d. Thus short-channel effects will happen at a longer channel length, i.e. the short-channel effect is more serious. The correlation coefficient between d_l and w_d is 0.44[3] which proves that the correlation between d_l and w_d is strong but one might expects an even stronger correlation between them. This may be explained by the variation in parameters across the wafers and bulk current exists in some short-channel devices.

From Table 6.2.1, it is obvious that γ_s decreases with L. Let $\gamma_{sL} \equiv \gamma_s$ for a long-channel device. Assuming

$$\gamma_s = \gamma_{sL} - \frac{g_c}{L^m} \tag{7.3}$$

[3]A value of 1 indicates perfect correlation, 0 indicates that there is no correlation.

Table 7.1.3 m in $\gamma_s = \gamma_{sL} + g_c/L^m$					
Wafer	m	Wafer	m	Wafer	m
1	–	6	7.1	11	2.5
2	0.6	7	0.8	12	3.3
3	–	8	2.4	13	3.7
4	1.5	9	3.1	14	5.9
5	2.4	10	6.0	15	2.9

Table 7.1.4 g_c and d_γ in $\gamma_s = \gamma_{sL} - g_c \exp(-L/d_\gamma)$					
Wafer	g_c	d_γ	Wafer	g_c	d_γ
1	–	–	9	93.7	0.36
2	41.4	1.58	10	2844.8	0.16
3	–	–	11	191.4	0.36
4	153.1	0.67	12	259.3	0.29
5	157.4	0.46	13	367.3	0.27
6	4476.6	0.15	14	1398.7	0.17
7	24.4	0.95	15	246.9	0.33
8	122.7	0.39			

$\ln(\gamma_{sL} - \gamma_s)$ can be plotted against $\ln L$, then $m = -slope$. Values of m are listed in Table 7.1.3.

m ranges from 0.6 to 7.1, so Eq. (7.3) with a fixed value of m is not a good description for γ_s–L relation.

The strong dependency of γ_s on L is also obvious. So, we use following expression to describe γ_s–L relation.

$$\gamma_s = \gamma_{sL} - g_c e^{-\frac{L}{d_\gamma}} \tag{7.4}$$

Plotting $\ln(\gamma_{sL} - \gamma_s)$ against L, we have $d_\gamma = -1/slope$ and $g_c = e^{const}$. Values of g_c and d_γ are listed in Table 7.1.4. The trend in the variation of d_γ against ion implantation is opposite to that of d_l.

Table 7.2.1 m in $S_0 = S_{W0} + s_w/W^m$					
Wafer	m	Wafer	m	Wafer	m
1	1.27	6	1.52	11	1.33
2	1.75	7	1.83	12	2.98
3	1.01	8	1.59	13	1.27
4	1.27	9	1.86	14	2.12
5	2.47	10	4.03	15	1.31

7.2 Channel Width W

In Figs. 7–7 to 7–12, we can see that S increases when the channel width W decreases. If we define $S_{W0} \equiv S_0$ of a wide-channel transistor, assuming

$$S_0 = S_{W0} + \frac{s_w}{W^m} \tag{7.5}$$

Plotting $\ln(S_0 - s_{W0})$ against $\ln W$ gives $m = -slope$. Values of m are listed in Table 7.2.1.

m ranges from 1.01 to 4.03. Compared with the results in the last section, one concludes that the dependence of S on the channel width W is not as strong as the dependence of S on the channel length L. However, the expression $S_0 = S_{W0} + s_w/W$ as suggested by some of the models described in Section 2.6 is not a good description of S–W relation. The dependence of S on W is stronger than $1/W$. Thus we decided that the exponential dependence of S on W is a better description for S–W relation. That is

$$S_0 = S_{W0} + s_w e^{-\frac{W}{d_w}} \tag{7.6}$$

Values of s_w and d_w are listed in Table 7.2.2. The correlation coefficient between d_w and w_d is 0.42, thus a similar conclusion is drawn as d_l.

From Table 6.2.1, γ_s does not have an obvious dependence on W and the changes in its value are not big when W changes. Thus we believe that γ_s is effectively independent of W.

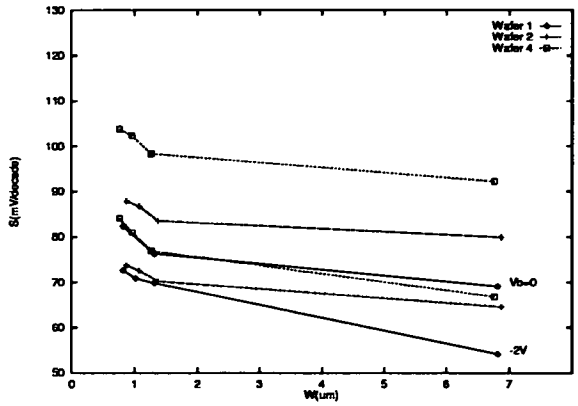


Figure 7–7: S vs. W at $V_B = 0$ and $V_B = -2$V for wafer group 1

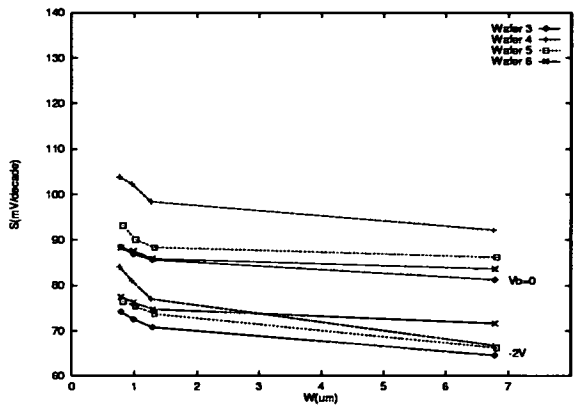


Figure 7–8: S vs. W at $V_B = 0$ and $V_B = -2$V for wafer group 2

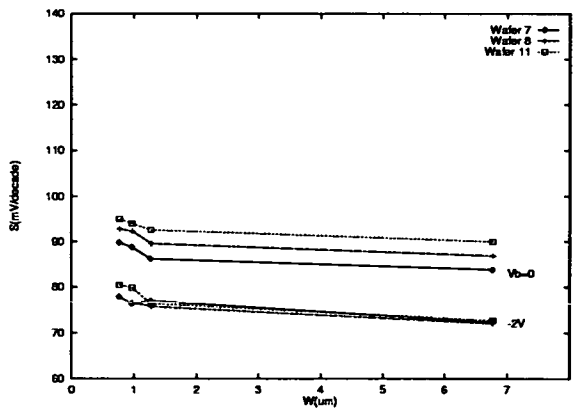


Figure 7–9: S vs. W at $V_B = 0$ and $V_B = -2$V for wafer group 3

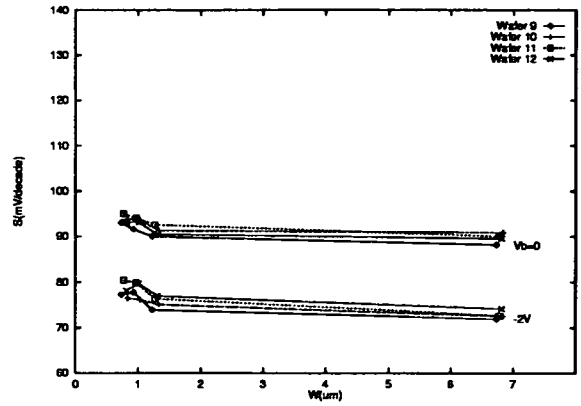


Figure 7–10: S vs. W at $V_B = 0$ and $V_B = -2$V for wafer group 4

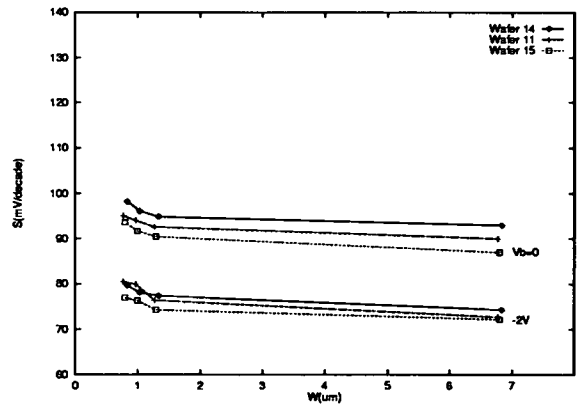


Figure 7–11: S vs. W at $V_B = 0$ and $V_B = -2$V for wafer group 5

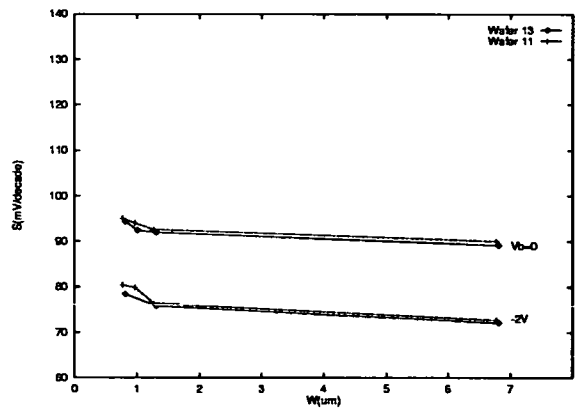


Figure 7–12: S vs. W at $V_B = 0$ and $V_B = -2$V for wafer group 6

Table 7.2.2 s_w and d_w in $S_0 = S_{W0} + s_w \exp(-W/d_w)$

Wafer	s_w	d_w	Wafer	s_w	d_w
1	35.40	0.83	9	20.18	0.51
2	34.17	0.63	10	95.86	0.26
3	15.29	1.02	11	14.26	0.75
4	32.74	0.77	12	48.99	0.34
5	44.49	0.43	13	12.63	0.85
6	16.07	0.66	14	25.95	0.51
7	26.66	0.54	15	17.53	0.79
8	22.85	0.62			

7.3 A Model for Circuit Simulation

Based on the theoretical and experimental results given in Chapter 3, 6 and 7, we propose a model which is suitable for circuit simulation.

$$I_D = \frac{I_0}{\sqrt{1.5\psi_B - V_B}} \exp \alpha_D \beta V_D \exp\left(\frac{V_G - V_T}{S}\right) \tag{7.7}$$

where I_0 is the current constant, α_D is the drain barrier lowering coefficient and S is the subthreshold gate swing. They are to be extracted from the subthreshold characteristics.

$$S = S_0 + s_l e^{-\frac{L}{d_l}} + s_w e^{-\frac{W}{d_w}} + \left(\gamma_{s0} - g_c e^{-\frac{L}{d_\gamma}}\right)\left(\frac{1}{\sqrt{1.5\psi_B - V_B}} - \frac{1}{\sqrt{1.5\psi_B}}\right) \tag{7.8}$$

where S_0 and γ_{s0} are the subthreshold gate swing S at zero substrate bias and the subthreshold body factor γ_s for a long and wide channel MOSFET, respectively.

Chapter 8

Conclusion and Discussion

A new two-dimensional analytical subthreshold model is derived. It gives analytical expressions for the subthreshold current and gate swing for a non-uniformly doped MOS device with an arbitary doping profile. It predicts that the subthreshold gate swing depends exponentially on the channel length. A two-dimensional analytical punchthrough model is also derived. It has included both the bulk and surface punchthrough current component. It shows that the position of the punchthrough current path is determined by the value of $V_G - V_{FB}$, V_D, channel length L and the integral of the doping profile in the depletion region.

Fifteen wafers with different ion implant dose and energy have been fabricated. Eight devices on each wafer with different geometry sizes have been measured for their subthreshold characteristics. The influence of ion implantation on subthreshold behaviour of MOSFETs has been examined. It is demonstrated that shallow implantation has a bigger influence on the subthreshold gate swing of a MOSFET than deep implantation. Shallow implant dose has a bigger influence on the subthreshold gate swing than shallow implant energy.

An examination of how terminal voltages and geometry sizes affect subthreshold behaviour has been carried out. It verifies the theoretical model derived earlier. It confirms that the subthreshold gate swing depends exponentially on the channel length. It also shows that the subthreshold gate swing depends exponentially on the channel width as well, though the dependency is not as strong as that on the

channel length. Based on above observation and theoretical model, a compact subthreshold model suitable for circuit simulation has been proposed.

Appendix A

Solution of One-Dimensional Poisson Equation

The one-dimensional Poisson's equation in the channel and the depletion region of a MOSFET may be expressed as

$$\frac{d^2\psi}{dx^2} = -\frac{\rho}{\epsilon_{si}} = -\frac{q}{\epsilon_{si}}(p - n + N_D - N_A) \tag{A.1}$$

where N_D and N_A are the density of donor and acceptor respectively. The hole density p and the electron density n can be expressed as follows

$$p = n_i e^{u_p - u} = n_i e^{u_B - u} \tag{A.2}$$

$$n = n_i e^{u - u_n} = n_i e^{u - \xi - u_B} \tag{A.3}$$

The charge neutral condition should be satisfied in the neutral bulk, so

$$p_{p0} - n_{p0} + N_D - N_A = 0 \tag{A.4}$$

Therefore

$$\begin{aligned} N_A - N_D &= p_{p0} - n_{p0} \\ &= n_i \left(e^{u_B} - e^{-u_B}\right) \end{aligned} \tag{A.5}$$

where u_p is the hole quasi-Fermi level, normalised to $\frac{kT}{q}$. p_{p0} and n_{p0} are the equilibrium density of holes and electrons in the bulk of semiconductor. Substituting Eq. (A.2), (A.3) and (A.5) into Eq. (A.1), one has

$$\frac{d^2u}{dx^2} = \frac{q^2}{kT}\frac{n_i}{\epsilon_{si}}\left(e^{u-\xi-u_B} - e^{u_B-u} + e^{u_B} - e^{-u_B}\right) \tag{A.6}$$

Integrating with respect to u at both sides of the Eq. (A.6), it can be written as

$$\int_0^{\frac{du}{dx}} \left(\frac{du}{dx}\right) d\left(\frac{du}{dx}\right) = \frac{1}{L_d^2} \int_0^u \left(e^{u-\xi-u_B} - e^{u_B-u} + e^{u_B} - e^{-u_B}\right) du \tag{A.7}$$

resulting

$$\left(\frac{du}{dx}\right)^2 = \frac{1}{L_d^2}[e^{u-\xi-u_B} + e^{u_B-u} + (u-1)e^{u_B} - (u+e^{-\xi})e^{-u_B}] \tag{A.8}$$

So,

$$\left(\frac{du}{dx}\right) = -\frac{1}{L_d} F(u, \xi, u_B) \tag{A.9}$$

where the intrinsic Debye length

$$L_d = \left(\frac{\epsilon_{si} kT}{2q^2 n_i}\right)^{\frac{1}{2}} \tag{A.10}$$

and

$$F(u, \xi, u_B) = [e^{u-\xi-u_B} + e^{u_B-u} + (u-1)e^{u_B} - (u+e^{-\xi})e^{-u_B}]^{\frac{1}{2}} \tag{A.11}$$

Appendix B

Depletion Depth w_d

From Eq. (2.71) and (3.27), it is clear that to obtain the subthreshold gate swing S, w_d is needed to be calculated first.

For a long-channel device, substituting Eq. (2.66) and (2.68) into relation $C_{ox}(V_G - V_B - V_{FB} - \psi_s) = \epsilon_{si}\mathcal{E}_s$, one finds that w_d satisfy

$$\frac{q}{\epsilon_{si}}\int_0^{w_d} dx \cdot xN(x) + \frac{q}{C_{ox}}\int_0^{w_d} dxN(x) - V'_{GB} = 0 \tag{B.1}$$

If the channel is uniformly doped, then it reduces to

$$w_d = \sqrt{\frac{2\epsilon_{si}\psi_s}{qN_A}} \tag{B.2}$$

where

$$\psi_s = V'_{GB} + \frac{qN_A\epsilon_{si}}{C_{ox}^2}\left[1 - \left(1 + \frac{2C_{ox}^2}{qN_A\epsilon_{si}}\right)^{\frac{1}{2}}\right] \tag{B.3}$$

For a long-channel device, to calculate w_d at a given current level, following approach is used. From Eq. (2.58), one has

$$\ln\left(\frac{I_D}{W/L}\right) = \ln\left\{\frac{q\mu_n n_{p0}}{\beta^2}[1 - \exp(-\beta V_D)]\right\} + \beta\psi_s + \beta V_B - \ln\mathcal{E}_s \tag{B.4}$$

If we define

$$I \equiv \frac{q\mu_n n_{p0}}{\beta^2}[1 - \exp(-\beta V_D)] \tag{B.5}$$

where $n_{p0} = \frac{n_i^2}{N_A}$. Then

$$\ln\frac{I_D/(W/L)}{I} = \beta\psi_s + \beta V_B - \ln\mathcal{E}_s \tag{B.6}$$

From Eq. (B.6) and (2.68),

$$\ln \frac{I_D/(W/L)}{I} - \beta \left[\psi(w_d) - w_d \left(\frac{d\psi}{dx} \right)_{x=w_d} + \frac{q}{\epsilon_{si}} \int_0^{w_d} dx \cdot xN(x) + V_B \right] + \ln \mathcal{E}_s = 0 \tag{B.7}$$

Using boundary conditions [116]

$$\psi(w_d) = \frac{1}{\beta} \ln \frac{N(w_d)}{N_A} \tag{B.8}$$

$$\left(\frac{d\psi}{dx} \right)_{x=w_d} = 0 \tag{B.9}$$

For a chosen $I_D/(W/L)$ at a certain constant level, we can use a numerical method to obtain w_d. The basic idea is that let

$$f(w_d) = \ln \frac{I_D/(W/L)}{I} - \beta \left[\psi(w_d) + V_B + \frac{q}{\epsilon_{si}} \int_0^{w_d} dx \cdot xN(x) \right] + \ln \mathcal{E}_s = 0 \tag{B.10}$$

Choose w_{d1} and w_{d2}, let $f(w_{d1}) < 0$ and $f(w_{d2}) > 0$. Because of the continuity of $f(w_d)$, a w_d between w_{d1} and w_{d2} can certainly be found to satisfy Eq. (B.10).

For a short-channel device, from Eq. (3.5) and (3.6), w_d must satisfy

$$\frac{q}{\epsilon_{si}} F(w_d) + \frac{q}{C_{ox}} G(w_d) - V(w_d, y_m) - V'_{GB} + \psi(w_d, y_m) = 0 \tag{B.11}$$

where $\psi(w_d, y_m) = \frac{1}{\beta} \ln \frac{N(w_d)}{N_A}$. For a device with an uniformly doped channel, from Eq. (D.7), one has

$$w_d = \sqrt{\frac{2\epsilon_{si}}{qN_A} [\psi_{smin} + V(w_d, y_m) - V(0, y_m)]} \tag{B.12}$$

Since $V(w_d, y_m) - V(0, y_m) > 0$, it is obvious that w_d of a short-chanel device is wider than that of a long-channel device with the same surface potential. To calculate w_d at a given current level for a short-channel device, let us define normalised drain current $I_{D0} = I_D/(W/L)$, coefficient $I_0 = qD_n(n_i^2/N_B)[1 - \exp(-\beta V_D)]$, from Eq. (3.17), we have

$$\ln \frac{I_{D0}}{I_0} = \ln \frac{t_{ch}}{L_{eff}} + \beta \psi_{smin} + \beta V_B \tag{B.13}$$

where t_{ch}, L_{eff} and ψ_{smin} are function of w_d. So w_d must satisfy

$$f(w_d) = \ln \frac{I_{D0}}{I_0} - \ln \frac{t_{ch}}{L_{eff}} + \beta \psi_{smin} + \beta V_B = 0 \tag{B.14}$$

This can be solved by method of iteration.

Step 1 giving a initial guess of V_G^0 and choosing w_{d1} and w_{d2},

Step 2 for a given V_G and w_d, one can obtain y_m, ψ_{smin}, L_{eff} and $\mathcal{E}_s$ thus t_{ch},

Step 3 using iteration method on (B.14) to obtain w_d^0,

Step 4 using w_d^0 and V_G^0, then y_m^0 and ψ_{smin}^0 can be obtained,

Step 5 V_G^1 can be determined from w_d^0, y_m^0 and ψ_{smin}^0,

Step 6 If $|V_G^1 - V_G^0| < \epsilon|V_G^0|$, then the iteration is over, w_d^0 obtained in Step 3 is the depletion depth we are looking for. where ϵ is a small number, say 0.001.

Step 7 Otherwise, let $V_G^0 = V_G^1$, repeat Step 1-6.

Appendix C

Solution of Two-Dimensional Poisson Equation

The two-dimensional Poisson's equation in the depletion region of a MOSFET may be expressed as

$$\frac{\partial^2\psi}{\partial x^2}+\frac{\partial^2\psi}{\partial y^2}=\frac{q}{\epsilon_{si}}N(x) \tag{C.1}$$

Let $\psi(x,y)=\psi_L(x)+V(x,y)$, where $\psi_L(x)$ is a one-dimensional function; $V(x,y)$ is the solution of Laplace equation, it represents the two-dimensional nature of the potential distribution. They satisfy following equations and boundary conditions.

$$\begin{array}{ll}
\frac{d^2\psi_L}{dx^2}=\frac{q}{\epsilon_{si}}N(x) & \frac{\partial^2 V}{\partial x^2}+\frac{\partial^2 V}{\partial y^2}=0 \\
\left(\frac{d\psi_L}{dx}\right)_{x=0}=-\frac{C_{ox}}{\epsilon_{si}}[V'_{GB}-\psi_L(0)] & \frac{\partial V}{\partial x}(0,y)=\frac{C_{ox}}{\epsilon_{si}}V(0,y) \\
\left(\frac{d\psi_L}{dx}\right)_{x=w_d}=0 & \frac{\partial V}{\partial x}(w_d,y)=0 \\
 & V(x,0)=\psi(x,0)-\psi_L(x) \\
 & V(x,L)=\psi(x,L)-\psi_L(x)
\end{array} \tag{C.2}$$

Solving one-dimensional Poisson's equation for ψ_L, one has

$$\psi_L(x)=V'_{GB}-\frac{q}{\epsilon_{si}}\int_0^x x_1N(x_1)dx_1-\frac{q}{\epsilon_{si}}x\int_x^{w_d}N(x_1)dx_1-\frac{q}{C_{ox}}\int_0^{w_d}N(x_1)dx_1 \tag{C.3}$$

It has a similar form to the solution of Poisson's equation for a long-channel MOSFET, thus the expression of ψ_L. Actually, when the channel length $L\rightarrow\infty$, ψ_L becomes the same as the long-channel solution.

Now we use variable separation technique to solve the two-dimensional Laplace equation. Let

$$V(x,y)=X(x)Y(y) \tag{C.4}$$

substitute it into Laplace equation, one has

$$X''Y + XY'' = 0 \tag{C.5}$$

rewritting it, one has

$$\frac{X''}{X} = -\frac{Y''}{Y} = \pm k^2 \tag{C.6}$$

Since $\frac{X''}{X}$ is a function of x, $-\frac{Y''}{Y}$ is a function of y, if these two term are equal, they have to equal a constant. This constant could be positive or negtive, for future convenience, a form of $\pm k^2$ is chosen. for $+k^2$, one has

$$\begin{cases} X'' - k^2 X = 0 \\ Y'' + k^2 Y = 0 \end{cases} \tag{C.7}$$

Its solution is

$$(I) \begin{cases} X = ae^{kx} + be^{-kx} \\ Y = c\cos ky + d\sin ky \end{cases} \tag{C.8}$$

for $-k^2$, one has

$$\begin{cases} X'' + k^2 X = 0 \\ Y'' - k^2 Y = 0 \end{cases} \tag{C.9}$$

Its solution is

$$(II) \begin{cases} X = A\cos kx + B\sin kx \\ Y = Ce^{ky} + De^{-ky} \end{cases} \tag{C.10}$$

Considering boundary conditions, one has

$$X'(0) = \frac{C_{ox}}{\epsilon_{si}} X(0) \tag{C.11}$$

$$X'(w_d) = 0 \tag{C.12}$$

$$XY(0) = V(x, 0) \tag{C.13}$$

$$XY(L) = V(x, L) \tag{C.14}$$

(I) cannot satisfy above boundary conditions. For (II), from boundary conditions (C.11) and (C.12), one has

$$k = \frac{C_{ox}}{\epsilon_{si}} \cot kw_d \tag{C.15}$$

that is

$$kw_d = \arctan\left(\frac{C_{ox}}{\epsilon_{si} k}\right) + n\pi (n = 0, 1, 2, ...) \tag{C.16}$$

since k is function of n, we redefind it as k_n,*i.e.* $k \equiv k_n$, and

$$B_n = \frac{1}{k_n}\frac{C_{ox}}{\epsilon_{si}}A_n \tag{C.17}$$

Substituting Eq. (C.17) into (C.10), one has

$$X_n = A_n \cos k_n x + \frac{1}{k_n}\frac{C_{ox}}{\epsilon_{si}}A_n \sin k_n x = A_n \frac{\cos k_n(w_d - x)}{\cos k_n w_d} \tag{C.18}$$

Since whatever value we chosen for A_n, (C.18) will satisfy boundary conditions (C.11) and (C.12), for simplification sake, $A_n = 1$ is chosen. X_nY_n $(n = 0, 1, 2, \ldots)$ are all solutions of (C.2), their sum is the full solution to (C.2). Thus

$$V(x, y) = \sum_{n=0}^{\infty} X_n Y_n \tag{C.19}$$

using boundary conditions (C.13) and (C.14), one has

$$V(x, 0) = \sum_{n=0}^{\infty} \frac{\cos k_n(w_d - x)}{\cos k_n w_d}(C_n + D_n) \tag{C.20}$$

$$V(x, L) = \sum_{n=0}^{\infty} \frac{\cos k_n(w_d - x)}{\cos k_n w_d}(C_n e^{k_n L} + D_n e^{-k_n L}) \tag{C.21}$$

since

$$\int_0^{w_d} \cos k_m(w_d - x) \cos k_n(w_d - x)dx = 0 \; m \neq n \tag{C.22}$$

$$\int_0^{w_d} \cos^2 k_n(w_d - x)dx = \frac{1}{2}w_d\left(1 + \frac{\sin 2k_n w_d}{2k_n w_d}\right) \tag{C.23}$$

let $u_n \equiv \frac{1}{2}\left(1 + \frac{\sin 2k_n w_d}{2k_n w_d}\right)$, one has

$$\frac{C_n + D_n}{\cos k_n w_d} = E_n \tag{C.24}$$

$$\frac{C_n e^{k_n L} + D_n e^{-k_n L}}{\cos k_n w_d} = F_n \tag{C.25}$$

where

$$E_n = \frac{1}{u_n w_d}\int_0^{w_d} V(x, 0) \cos k_n(w_d - x)dx \tag{C.26}$$

$$F_n = \frac{1}{u_n w_d}\int_0^{w_d} V(x, L) \cos k_n(w_d - x)dx \tag{C.27}$$

Thus, one has

$$C_n = \frac{F_n - E_n e^{-k_n L}}{2 \sinh k_n L} \cos k_n w_d \tag{C.28}$$

$$D_n = \frac{E_n e^{k_n L} - F_n}{2 \sinh k_n L} \cos k_n w_d \tag{C.29}$$

Therefore,

$$\begin{aligned} V(x,y) &= \sum_{n=0}^{\infty} \frac{\cos k_n(w_d - x)}{\cos k_n w_d} \left(C_n e^{k_n y} + D_n e^{-k_n y}\right) \\ &= \sum_{n=0}^{\infty} \frac{\cos k_n(w_d - x)}{u_n \sinh k_n L} [H_n \sinh k_n(L - y) + I_n \sinh k_n y] \end{aligned} \tag{C.30}$$

where

$$H_n = \frac{1}{w_d} \int_0^{w_d} V(x,0) \cos k_n(w_d - x) dx \tag{C.31}$$

$$I_n = \frac{1}{w_d} \int_0^{w_d} V(x,L) \cos k_n(w_d - x) dx \tag{C.32}$$

Appendix D

Subthreshold Gate Swing for Short-Channel MOSFETs

The subthreshold gate swing

$$S = 1000\,(\ln 10)\frac{dV_G/dw_d}{d(\ln I_D)/dw_d} \quad \text{mV/decade} \tag{D.1}$$

From Eq. (3.17),

$$\frac{d(\ln I_D)}{dw_d} = \beta\frac{d\psi_{smin}}{dw_d} - \frac{1}{L_{eff}}\frac{dL_{eff}}{dw_d} - \frac{1}{\mathcal{E}_s}\frac{d\mathcal{E}_s}{dw_d} \tag{D.2}$$

Since $\mathcal{E}_s(y) = -\frac{\partial\psi}{\partial x}(0,y)$, from Eq. (3.1),

$$V'_{GB} - \psi_{smin} = \frac{\epsilon_{si}}{C_{ox}}\mathcal{E}_s(y_m) \tag{D.3}$$

So, one has

$$\frac{dV_G}{dw_d} = \frac{d\psi_{smin}}{dw_d} + \frac{\epsilon_{si}}{C_{ox}}\frac{d\mathcal{E}_s}{dw_d} \tag{D.4}$$

Now, let us derive the expression for $\frac{d\psi_{smin}}{dw_d}$ first. From Eq. (3.5) and (3.6)

$$\psi_{smin} = \psi(0,y_m) = V'_{GB} - \frac{q}{C_{ox}}G(w_d) + V(0,y_m) \tag{D.5}$$

$$\psi(w_d,y_m) = V'_{GB} - \frac{q}{\epsilon_{si}}F(w_d) - \frac{q}{C_{ox}}G(w_d) + V(w_d,y_m) = \frac{1}{\beta}\ln\frac{N_A}{N(w_d)} \tag{D.6}$$

substrate Eq. (D.6) from (D.5), one has

$$\psi_{smin} = \frac{q}{\epsilon_{si}}F(w_d) + V(0,y_m) - V(w_d,y_m) + \psi(w_d,y_m) \tag{D.7}$$

So,

$$\frac{d\psi_{smin}}{dw_d} = \frac{q}{\epsilon_{si}} w_d N(w_d) + \frac{d}{dw_d} V(0, y_m) - \frac{d}{dw_d} V(w_d, y_m) \tag{D.8}$$

Next, we derive the expression for $\frac{d\mathcal{E}_s}{dw_d}$. Substituting Eq. (D.5) into (D.3), one has

$$\mathcal{E}_s = \frac{C_{ox}}{\epsilon_{si}}[V'_{GB} - \psi_{smin}] = \frac{q}{\epsilon_{si}} G(w_d) - \frac{C_{ox}}{\epsilon_{si}} V(0, y_m) \tag{D.9}$$

So,

$$\frac{d\mathcal{E}_s}{dw_d} = \frac{q}{\epsilon_{si}} N(w_d) - \frac{C_{ox}}{\epsilon_{si}} \frac{d}{dw_d} V(0, y_m) \tag{D.10}$$

Substituting Eq. (D.8) and (D.10) into (D.4), one has

$$\frac{dV_G}{dw_d} = \frac{q}{\epsilon_{si}} w_d N(w_d) + \frac{q}{C_{ox}} N(w_d) - \frac{d}{dw_d} V(w_d, y_m) \tag{D.11}$$

The expression of $\frac{d}{dw_d} V(0, y_m)$ and $\frac{d}{dw_d} V(w_d, y_m)$ are to be derived next. Let

$$\begin{aligned} A_n(x, y) &= \frac{\cos k_n(w_d - x)}{u_n \sinh k_n L}[H_n \sinh k_n(L - y) + I_n \sinh k_n y] \\ &= a_n(x)[H_n s_0(y) + I_n s_L(y)] \end{aligned} \tag{D.12}$$

where $a_n(x) = \cos k_n(w_d - x)/u_n$, $s_0(y) = \sinh k_n(L - y)/\sinh k_n L$, $s_L(y) = \sinh k_n y/\sinh k_n L$. Then

$$\frac{d}{dw_d} V(x_0, y_m) = \sum_{n=0}^{\infty} \frac{d}{dw_d} A_n(x_0, y_m) \ (x_0 = 0 \text{ or } w_d) \tag{D.13}$$

Let

$$\frac{d}{dw_d} A_n(x_0, y_m) = DV_1(x_0, y_m) + DV_2(x_0, y_m) + DV_3(x_0, y_m) \tag{D.14}$$

where

$$DV_1(x_0, y_m) = \frac{da_n(x_0)}{dw_d}[H_n s_0(y_m) + I_n s_L(y_m)] \tag{D.15}$$

$$DV_2(x_0, y_m) = a_n(x_0)[\frac{dH_n}{dw_d} s_0(y_m) + \frac{dI_n}{dw_d} s_L(y_m)] \tag{D.16}$$

$$DV_3(x_0, y_m) = a_n(x_0)[H_n \frac{ds_0(y_m)}{dw_d} + I_n \frac{ds_L(y_m)}{dw_d}] \tag{D.17}$$

To find the expression of DV_2, we have to find those for $\frac{dH_n}{dw_d}$ and $\frac{dI_n}{dw_d}$ first. From Eq. (3.10), one has

$$\frac{dH_n}{dw_d} = \frac{1}{w_d}\{-H_n + V(w_d, 0)$$

$$
\begin{aligned}
& - \int_0^{w_d} V(x,0) \sin k_n(w_d - x) \left(\frac{d(k_n w_d)}{dw_d} - \frac{dk_n}{dw_d} x \right) dx \\
& - \int_0^{w_d} \left[\frac{dV_G}{dw_d} - \frac{q}{\epsilon_{si}} x N(w_d) - \frac{q}{C_{ox}} N(w_d) \right] \cos k_n(w_d - x) dx \} \\
= \; & \frac{1}{w_d} \{ - H_n + V(w_d, 0) \\
& - \frac{d(k_n w_d)}{dw_d} \int_0^{w_d} V(x,0) \sin k_n(w_d - x) dx \\
& + \frac{dk_n}{dw_d} \int_0^{w_d} V(x,0) x \sin k_n(w_d - x) dx \\
& - \left[\frac{dV_G}{dw_d} - \frac{q}{C_{ox}} N(w_d) \right] \frac{\sin k_n w_d}{k_n} + \frac{q}{\epsilon_{si}} N(w_d) \frac{1 - \cos k_n w_d}{k_n^2} \} \\
= \; & \frac{1}{w_d} [-H_n + V(w_d, 0)] + DH1_0 + DH2_0 + DH3 \\
& - \frac{dV_G}{dw_d} \frac{\sin k_n w_d}{k_n w_d}
\end{aligned}
\tag{D.18}
$$

where

$$
DH1_0 = - \frac{1}{w_d} \frac{d(k_n w_d)}{dw_d} \int_0^{w_d} V(x,0) \sin k_n(w_d - x) dx \tag{D.19}
$$

$$
DH2_0 = \frac{1}{w_d} \frac{dk_n}{dw_d} \int_0^{w_d} V(x,0) x \sin k_n(w_d - x) dx \tag{D.20}
$$

$$
DH3 = \frac{q}{\epsilon_{si}} \frac{N(w_d)}{k_n w_d} \left[\frac{\epsilon_{si}}{C_{ox}} \sin k_n w_d + \frac{1 - \cos k_n w_d}{k_n} \right] \tag{D.21}
$$

Similarly,

$$
\begin{aligned}
\frac{dI_n}{dw_d} = \; & \frac{1}{w_d} [-I_n + V(w_d, L)] + DH1_L + DH2_L + DH3 \\
& - \frac{dV_G}{dw_d} \frac{\sin k_n w_d}{k_n w_d}
\end{aligned}
\tag{D.22}
$$

Replacing $V(x,0)$ in $DH1_0$ and $DH2_0$ with $V(x,L)$, one has $DH1_L$ and $DH2_L$. Thus,

$$
\begin{aligned}
DV_2 = \; & \frac{1}{w_d} \{ -V(x_0, y_m) + \sum_{n=0}^{\infty} a_n(x_0) [V(w_d, 0) s_0(y_m) + V(w_d, L) s_L(y_m)] \} \\
& + \sum_{n=0}^{\infty} a_n(x_0) [(DH1_0 + DH2_0 + DH3) s_0(y_m) \\
& + (DH1_L + DH2_L + DH3) s_L(y_m)] \\
& - \frac{1}{w_d} \frac{dV_G}{dw_d} \sum_{n=0}^{\infty} a_n(x_0) [s_0(y_m) + s_L(y_m)] \frac{\sin k_n w_d}{k_n} \\
= \; & DV_2' - \frac{1}{w_d} \frac{dV_G}{dw_d} \sum_{n=0}^{\infty} a_n(x_0) [s_0(y_m) + s_L(y_m)] \frac{\sin k_n w_d}{k_n}
\end{aligned}
\tag{D.23}
$$

Next, we derive the expression for DV_3, thus we deal with $\frac{ds_0}{dw_d}$ and $\frac{ds_L}{dw_d}$ first.

$$\begin{aligned}
\frac{ds_0}{dw_d} &= \frac{d}{dw_d}\left(\frac{\sinh k_n(L-y_m)}{\sinh k_n L}\right) \\
&= \frac{\cosh k_n(L-y_m)}{\sinh k_n L}\left[\frac{dk_n}{dw_d}(L-y_m) - k_n\frac{dy_m}{dw_d}\right] \\
&\quad -\frac{\cosh k_n L}{\sinh^2 k_n L}\sinh k_n(L-y_m)\frac{dk_n}{dw_d}L \\
&= c_0(y_m)\left[\frac{dk_n}{dw_d}(L-y_m) - k_n\frac{dy_m}{dw_d}\right] - s_0(y_m)\coth k_n L\frac{dk_n}{dw_d}L \qquad \text{(D.24)} \\
\frac{ds_L}{dw_d} &= \frac{d}{dw_d}\left(\frac{\sinh k_n y_m}{\sinh k_n L}\right) \\
&= \frac{\cosh k_n y_m}{\sinh k_n L}\left(\frac{dk_n}{dw_d}y_m + k_n\frac{dy_m}{dw_d}\right) - \frac{\cosh k_n L}{\sinh^2 k_n L}\sinh k_n y_m\frac{dk_n}{dw_d}L \\
&= c_L(y_m)\left(\frac{dk_n}{dw_d}y_m + k_n\frac{dy_m}{dw_d}\right) - s_L(y_m)\coth k_n L\frac{dk_n}{dw_d}L \qquad \text{(D.25)}
\end{aligned}$$

where $c_0(y) = \cosh k_n(L-y)/\sinh k_n L$, $c_L(y) = \cosh k_n y/\sinh k_n L$. Thus

$$\begin{aligned}
DV_3(x_0, y_m) &= \frac{dk_n}{dw_d}a_n(x_0)[H_n(L-y_m)c_0(y_m) + I_n y_m c_L(y_m)] \\
&\quad -L\frac{dk_n}{dw_d}\coth k_n L A_n \\
&\quad +\frac{dy_m}{dw_d}a_n k_n[-H_n c_0(y_m) + I_n c_L(y_m)] \qquad \text{(D.26)}
\end{aligned}$$

So,

$$\begin{aligned}
\frac{d}{dw_d}V(x_0, y_m) &= \sum_{n=0}^{\infty} DV_1(x_0, y_m) + \sum_{n=0}^{\infty} DV_2(x_0, y_m) + \sum_{n=0}^{\infty} DV_3(x_0, y_m) \\
&= \sum_{n=0}^{\infty} DV_1(x_0, y_m) + \sum_{n=0}^{\infty} DV_2'(x_0, y_m) + \sum_{n=0}^{\infty} DV_3(x_0, y_m) \\
&\quad -\frac{1}{w_d}\frac{dV_G}{dw_d}\sum_{n=0}^{\infty} a_n(x_0)(s_0 + s_L)\frac{\sin k_n w_d}{k_n} \qquad \text{(D.27)}
\end{aligned}$$

One has

$$\begin{aligned}
\sum_{n=0}^{\infty} DV_3 &= \sum_{n=0}^{\infty}\frac{dk_n}{dw_d}a_n[H_n(L-y_m)c_0(y_m) + I_n y_m c_L(y_m)] \\
&\quad -L\sum_{n=0}^{\infty} a_n\frac{dk_n}{dw_d}\coth k_n L[H_n s_0(y_m) + I_n s_L(y_m)] \\
&\quad +\frac{dy_m}{dw_d}\sum_{n=0}^{\infty} a_n k_n[-H_n c_0(y_m) + I_n c_L(y_m)] \qquad \text{(D.28)} \\
&= \sum_{n=0}^{\infty} DV_3' + \frac{dy_m}{dw_d}\frac{\partial V}{\partial y}(x_0, y_m)
\end{aligned}$$

$$\approx \sum_{n=0}^{\infty} DV_3' \tag{D.29}$$

$$\sum_{n=0}^{\infty} DV_3' = \sum_{n=0}^{\infty} \frac{dk_n}{dw_d} a_n [H_n(L-y_m)c_0(y_m) + I_n y_m c_L(y_m)] - L\sum_{n=0}^{\infty} a_n \frac{dk_n}{dw_d} \coth k_n L[H_n s_0 + I_n s_L] \tag{D.30}$$

Since the third sum in Eq. (D.28) is $\frac{\partial V}{\partial y}(x_0, y_m)$. By definition of y_m, $\frac{\partial V}{\partial y}(0, y_m) = 0$. Although $\frac{\partial V}{\partial y}(w_d, y_m)$ is not zero, but it is negligible thus $\frac{\partial V}{\partial y}(w_d, y_m) \approx 0$. Instituting Eq .(D.27) into (D.11), one has

$$\frac{dV_G}{dw_d} = \frac{\frac{q}{C_{ox}} N(w_d)\left(1 + \frac{C_{ox}}{\epsilon_{si}} w_d\right)}{1 - \frac{1}{w_d}\sum \frac{\sin k_n w_d}{k_n u_n}(s_0 + s_L)} - \frac{\sum DV_1(w_d, y_m) - \sum DV_2'(w_d, y_m) - \sum DV_3(w_d, y_m)}{1 - \frac{1}{w_d}\sum \frac{\sin k_n w_d}{k_n u_n}(s_0 + s_L)} \tag{D.31}$$

Now, we going to derive $\frac{dL_{eff}}{dw_d}$. For very short-channel MOSFETs which satisfy $\frac{\beta}{2}\frac{\partial^2 \psi}{\partial y^2}(0, y_m)(L - y_m)^2 > 1$, using Eq. (3.21) then

$$\frac{dL_{eff}}{dw_d} = -\frac{1}{2}\frac{L_{eff}}{\frac{\partial^2 \psi}{\partial y^2}(0, y_m)} \frac{d}{dw_d}\left(\frac{\partial^2 \psi}{\partial y^2}(0, y_m)\right) \tag{D.32}$$

$$\frac{d}{dw_d}\left(\frac{\partial^2 \psi}{\partial y^2}(0, y_m)\right) = \frac{d}{dw_d}\sum_{n=0}^{\infty} k_n^2 A_n(0, y_m) = \sum_{n=0}^{\infty} k_n^2 \frac{d}{dw_d} A_n(0, y_m) + \sum_{n=0}^{\infty} 2k_n \frac{dk_n}{dw_d} A_n(0, y_m) \tag{D.33}$$

Otherwise, from Eq. (3.23) one has

$$\frac{L_{eff}}{dw_d} = \frac{dy_2}{dw_d} - \frac{dy_1}{dw_d} \tag{D.34}$$

Since $\psi(0, y_1) - \psi_{smin} = \frac{\pi}{4\beta}$, then

$$\frac{d\psi_s(y_1)}{dw_d} - \frac{d\psi_{smin}}{dw_d} = 0 \tag{D.35}$$

$$\psi_s(y_1) = \psi_L(0) + V(0, y_1) = V_{GB}' - \frac{q}{C_{ox}} G(w_d) + V(0, y_1) \tag{D.36}$$

So,

$$\frac{d\psi_s(y_1)}{dw_d} = \frac{dV_G}{dw_d} - \frac{q}{C_{ox}} N(w_d) + \frac{dV}{dw_d}(0, y_1) \tag{D.37}$$

Deriving $\frac{dV}{dw_d}(0, y_1)$ is similar as we deriving $\frac{dV}{dw_d}(x_0, y_m)$, except that $\frac{\partial V}{\partial y_1}(0, y_1) \neq 0$. That is

$$\begin{aligned}\frac{d\psi_s(y_1)}{dw_d} &= \frac{dV_G}{dw_d} - \frac{q}{C_{ox}}N(w_d) + \sum_{n=0}^{\infty} DV_1(0, y_1) + \sum_{n=0}^{\infty} DV_2(0, y_1) \\ &\quad + \sum_{n=0}^{\infty} DV_3'(0, y_1) + \frac{dy_1}{dw_d}\frac{\partial V}{\partial y}(0, y_1) \end{aligned} \tag{D.38}$$

Substitute Eq. (D.11) into (D.38), then with Eq. (D.8) into (D.35), one has

$$\frac{dy_1}{dw_d} = \frac{1}{\frac{\partial \psi}{\partial y}(0, y_1)}\left[\frac{dV}{dw_d}(0, y_m) - \sum_{n=0}^{\infty} DV_1(0, y_1) - \sum_{n=0}^{\infty} DV_2(0, y_1) - \sum_{n=0}^{\infty} DV_3'(0, y_1)\right] \tag{D.39}$$

$\frac{dy_2}{dw_d}$ is obtained similarly. For a long-channel device, $\frac{1}{L_{eff}}\frac{dL_{eff}}{dw_d}$ can be neglected.

Substituting Eq (D.8) and (D.10) into (D.2), then together with (D.11) into (D.1), one has

$$S = 1000\left(\frac{\ln 10}{\beta}\right)\frac{1 + \frac{\epsilon_{si}}{w_d}\frac{1}{C_{ox}} - T_1}{1 - \frac{1}{\beta \mathcal{E}_s}\frac{1}{w_d} + T_2 - T_3} \text{ mV/decade} \tag{D.40}$$

where

$T_1 = \frac{1}{T}\frac{d}{dw_d}V(w_d, y_m)$;

$T_2 = \frac{1}{T}\left[\left(1 + \frac{1}{\beta \mathcal{E}_s}\frac{C_{ox}}{\epsilon_{si}}\right)\frac{d}{dw_d}V(0, y_m) - \frac{d}{dw_d}V(w_d, y_m)\right]$;

$T_3 = \frac{1}{T}\frac{1}{\beta L_{eff}}\frac{dL_{eff}}{dw_d}$;

$T = \frac{q}{\epsilon_{si}}w_d N(w_d)$.

Appendix E

Boundary Conditions at Source and Drain End for 2-D Poisson's Equation

Different boundary conditions at source and drain end for two-dimensional Poisson's equation have been used in literatures.

A rectangular source/drain junction with indefinite junction depth was used first, which gave

$$\psi_S(x,0) = V_{bi} - V_B \tag{E.1}$$

$$\psi_D(x,L) = V_{bi} - V_B + V_D \tag{E.2}$$

Another assumption was a rectangular source/drain junction with junction depth r_j, which gave

$$\psi_S = \begin{cases} V_{bi} - V_B & 0 \le x \le r_j \\ V_{bi} - V_B + \frac{q}{\epsilon_{si}} \left[r_j \int_{r_j}^{W_S} N(x)dx \right. & \\ \left. - \int_{r_j}^{x} x_1 N(x_1)dx_1 - x \int_{x}^{W_S} N(x_1)dx_1 \right] & r_j < x < W_S \\ 0 & x \ge W_S \end{cases} \tag{E.3}$$

$$\psi_D = \begin{cases} V_{bi} - V_B + V_D & 0 \le x \le r_j \\ V_{bi} - V_B + V_D + \frac{q}{\epsilon_{si}} \left[r_j \int_{r_j}^{W_D} N(x)dx \right. & \\ \left. - \int_{r_j}^{x} x_1 N(x_1)dx_1 - x \int_{x}^{W_D} N(x_1)dx_1 \right] & r_j < x < W_D \\ 0 & x \ge W_D \end{cases} \tag{E.4}$$

where W_S and W_D are depletion depth at source and drain end respectively, they satisfy

$$V_{bi} - V_B - \frac{q}{\epsilon_{si}}\left[\int_{r_j}^{W_S} xN(x)dx - r_j\int_{r_j}^{W_S} N(x)dx\right] = 0 \tag{E.5}$$

$$V_{bi} - V_B + V_D - \frac{q}{\epsilon_{si}}\left[\int_{r_j}^{W_D} xN(x)dx - r_j\int_{r_j}^{W_D} N(x)dx\right] = 0 \tag{E.6}$$

Solutions of two-dimensional Poisson's equation using boundary conditions derived from above two assumptions tend to over-estimate the short-channel effect. More accurate boundary conditions are derived from the cylindric junction assumption. That is

$$\psi_S = \begin{cases} V_{bi} - V_B & x = 0 \\ V_{bi} - V_B & \\ -\frac{q}{\epsilon_{si}}\frac{r_j^2}{x_j^2}\left[\int_{x_j}^{x} x_0 N(x_0)\ln\frac{x_0}{x_j}dx_0 + \ln\frac{x_j}{x}\int_{x}^{x_S} x_0 N(x_0)dx_0\right] & 0 < x < W_S \\ 0 & x \geq W_S \end{cases} \tag{E.7}$$

$$\psi_D = \begin{cases} V_{bi} + V_D - V_B & x = 0 \\ V_{bi} + V_D - V_B & \\ -\frac{q}{\epsilon_{si}}\frac{r_j^2}{x_j^2}\left[\int_{x_j}^{x} x_0 N(x_0)\ln\frac{x_0}{x_j}dx_0 + \ln\frac{x_j}{x}\int_{x}^{x_D} x_0 N(x_0)dx_0\right] & 0 < x < W_D \\ 0 & x \geq W_D \end{cases} \tag{E.8}$$

where $x_j = xr_j/\sqrt{x^2 + (r_j + y)^2}$, $x_S = xR_S/\sqrt{x^2 + (r_j + y)^2}$, $x_D = xR_D/\sqrt{x^2 + (r_j + y)^2}$. See Fig. 3–2 for reference. R_S, R_D satisfy

$$V_{bi} - V_B - \frac{q}{\epsilon_{si}}\frac{r_j^2}{x_j^2}\int_{x_j}^{x_S} x_0 N(x_0)\ln\frac{x_0}{x_j}dx_0 = 0 \tag{E.9}$$

$$V_{bi} + V_D - V_B - \frac{q}{\epsilon_{si}}\frac{r_j^2}{x_j^2}\int_{x_j}^{x_D} x_0 N(x_0)\ln\frac{x_0}{x_j}dx_0 = 0 \tag{E.10}$$

respectively.

The detail of solving Poisson's equation for the cylindric junction is as follows: Poisson's equation in a polar coordinate is

$$\frac{\partial^2\psi}{\partial r^2} + \frac{1}{r}\frac{\partial\psi}{\partial r} + \frac{1}{r^2}\frac{\partial^2\psi}{\partial\theta^2} = -\frac{\rho(r,\theta)}{\epsilon_{si}} \tag{E.11}$$

If the device is uniformly doped, then $\psi = \psi(r)$, $\frac{\partial^2\psi}{\partial\theta^2} = 0$. For a nonuniformly doped device, in most cases the impurity concentration dose not change dramatically along the direction normal to surface due to the annealing process following

the implantation. Thus we can neglect $\frac{\partial^2\psi}{\partial\theta^2}$. As a result, one has

$$\frac{1}{r}\frac{d}{dr}\left[r\frac{d\psi}{dr}\right] = \frac{q}{\epsilon_{si}}N(r\sin\theta) \tag{E.12}$$

Integrating twice with respect to r at both sides of the equations using boundary conditions $\left(\frac{d\psi}{dr}\right)_{R_s} = 0$ and $\psi(R_s) = 0$, resulting

$$\psi = -\frac{q}{\epsilon_{si}}\left[\ln r\int_r^{R_s} r_1 N(r_1\sin\theta)dr_1 - \int_r^{R_s} r_1\ln r_1 N(r_1\sin\theta)dr_1\right] \tag{E.13}$$

For source end junction, substituting

$$\psi(r_j) = -\frac{q}{\epsilon_{si}}\left[\ln r_j\int_{r_j}^{R_s} r_1 N(r_1\sin\theta)dr_1 - \int_{r_j}^{R_s} r_1\ln r_1 N(r_1\sin\theta)dr_1\right] = V_{bi} - V_B \tag{E.14}$$

from it, one has

$$\psi(r) = V_{bi} - V_B - \frac{q}{\epsilon_{si}}\left[\int_{r_j}^{r} r_1\ln\frac{r_1}{r_j}N(r_1\sin\theta)dr_1 + \ln\frac{r}{r_j}\int_r^{R_s} r_1 N(r_1\sin\theta)dr_1\right] \tag{E.15}$$

To express above formula in a x,y coordinate system, we change the integral along a line with given θ in a polar coordinate system to an integral along a line with given y in a x, y coordinate system. since $x = r\sin\theta$, $y = r\cos\theta$, thus $x = x$, $y = x\cot\theta$. Therefore $\dot{x} = \frac{dx}{dx} = 1$, $\dot{y} = \frac{dy}{dx} = \cot\theta$.

$$\begin{aligned}\int_{r_1}^{r_2} f(r,\theta)dr &= \int_{x_1}^{x_2} f(x,y)\sqrt{\dot{x}^2+\dot{y}^2}dx = \int_{x_1}^{x_2} f(x,y)\sqrt{1+\cot^2\theta}dx \\ &= \frac{1}{\sin\theta}\int_{x_1}^{x_2} f(x,y)dx\end{aligned} \tag{E.16}$$

Thus,

$$\begin{aligned}\psi(x,0) &= V_{bi} - V_B - \frac{q}{\epsilon_{si}}\frac{1}{\sin\theta}\left[\int_{x_j}^{x}\frac{x_0}{\sin\theta}\ln\frac{x_0}{x_j}N(x_0)dx_0 + \ln\frac{x}{x_j}\int_x^{x_S}\frac{x_0}{\sin\theta}N(x_0)dx_0\right] \\ &= V_{bi} - V_B - \frac{q}{\epsilon_{si}}\frac{r_j^2}{x_j^2}\left[\int_{x_j}^{x} x_0\ln\frac{x_0}{x_j}N(x_0)dx_0 + \ln\frac{x}{x_j}\int_x^{x_S} x_0 N(x_0)dx_0\right]\end{aligned} \tag{E.17}$$

where x_S satisfy

$$V_{bi} - V_B - \frac{q}{\epsilon_{si}}\frac{r_j^2}{x_j^2}\int_{x_j}^{x_S} x_0\ln\frac{x_0}{x_j}N(x_0)dx_0 = 0 \tag{E.18}$$

Glossary

$Beta$	the gain of a MOSFET	A/V^2
C_{ox}	capacitance of oxide layer per unit area	F/cm^2
C_D	capacitance of depletion layer per unit area	F/cm^2
D_n	electron diffusion constant	cm^2/s
D_p	hole diffusion constant	cm^2/s
$\mathcal{E}$	electric field	V/cm
$\mathcal{E}_s$	surface transverse electrical field	V/cm
$\mathcal{E}_x$	transverse field	V/cm
$\mathcal{E}_y$	longitudinal field	V/cm
E_F	Fermi level	eV
E_c	conducting band energy	eV
E_g	bandgap	eV
E_i	intrinsic Fermi level	eV
E_v	valence band energy	eV
I_D	drain to source current	A
I_{DS}	surface component of drain to source current	A
I_{DB}	bulk component of drain to source current	A
L	actual length of the channel	μm
L_B	extrinsic Debye length $L_B = \left[\frac{\epsilon_{si}}{qN_A\beta}\right]^{\frac{1}{2}}$	$\mathring{A}$
$L_d(inChapter2)$	Intrinsic Debye length $L_d = \left[\frac{\epsilon_{si}}{2qn_i\beta}\right]^{\frac{1}{2}}$	$\mathring{A}$
$L_d(InChapter4)$	diffusion length	μm
L_{eff}	effective channel length	μm
L_m	mask length of the channel	μm
N_A	substrate doping concentration	cm^{-3}

N_{eff}	effective substrate doping concentration	cm^{-3}
Q_{ox}	charge density in oxide	$Charges/cm^2$
Q_s	total charges induced in the semiconductor per unit area	$Charges/cm^2$
Q_B	charge density due to ionized impurity in the depletion region	$Charges/m^2$
R_p	projected range of ion implantation	μm
S	subthreshold gate swing	$mV/decade$
T	absolute temperature	K
V_B	substrate voltage	V
V_D	drain voltage	V
V_{FB}	flat band voltage	V
V_G	gate voltage	V
V_T	threshold voltage	V
V_{bi}	built-in voltage of the junction	V
W	actual width of the channel	μm
W_m	mask width of the channel	μm
k	Boltzmann constant	J/K
n	electron density	m^{-3}
n_i	intrinsic carrier density	m^{-3}
p	hole density	m^{-3}
q	electronic charge	C
r_j	source and drain junction depth	μm
t_{ch}	effective channel thickness	μm
t_{ox}	thickness of gate oxide	$\AA$
w_d	depletion region depth	μm
x	distance from oxide-semiconductor interface normal to the interface	μm
y	distance from source end along channel direction	μm
y_m	distance from source end at which surface potential is minimum	μm
ΔW	width reduction	μm
ΔR_p	projected standard deviation of ion implantation	μm
β	$\frac{q}{kT}$	$1/V$

γ	body factor	$\sqrt{V}$
ϵ_{ox}	permittivity of oxide	F/cm
ϵ_{si}	permittivity of silicon	F/cm
μ_n	electron mobility	$cm^2/V.s$
μ_p	hole mobility	$cm^2/V.s$
ξ	electron quasi-Fermi level measured from the bulk Fermi level and normalized to $\frac{kT}{q}$	
ρ	charge density per unit volume	m^{-3}
ϕ_m	work function of gate material	V
ϕ_{ms}	metal-semiconductor work function difference	V
χ	semiconductor electron affinity	V
ψ	electrostatic potential	V
ψ_B	potential difference between E_F and E_i	V
ψ_s	surface potential	V
ψ_{smin}	minimum surface potential along the channel	V

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