CMOS PROCESS SIMULATION

Thesis submitted by

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DECLARATION

I declare that all the work done in this Thesis is entirely my own except where otherwise indicated.

This Thesis is the result of a CASE project with Motorola Ltd., East Kilbride.

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Abstract

The fabrication of CMOS integrated circuits have now reached so high a level of complexity as to require, not only 1-D, but also 2-D computer simulation of process design, scaling and optimisation. A new 2-D simulator called EPIC (Edinburgh Program for Impurity Concentrations) has been developed to model complete fabrication processes in CMOS technology. The philosophy behind EPIC lies in a unique synergism of the well-established 1-D simulator SUPREM with new 2-D analytical and 2-D numerical process models.

The first simulation of both vertical and lateral effects in a p-well CMOS process is presented. The formation of source/drain regions in both NMOS and PMOS field-effect transistors is modelled in 2-D to allow prediction of effective channel length. EPIC is also used to examine narrow width transistors by simulating impurity redistribution during formation of the bird's beak region between the field and gate oxides. In addition, the first algorithm capable of modelling the capacitance of CMOS structures with non-uniform doping profiles is presented.

Publications by the author relevant to this work include:

A.G. Buttar and J.M. Robertson, "Computer Simulation - The Key to Flexibility in CMOS Technology", Proc of Technical Programme, Semiconductor '83 International, Birmingham, England, 27 - 29 Sept 1983.

A.G. Buttar, M.N. Kozicki and J.M. Robertson, "Temperature Modelling for Transient Annealing", in Proc. 8th Symposium on Solid State Device Technology, Canterbury, Kent, 13-16 Sept 1983, The Inst. of Phys. Studies.

A.G. Buttar and J.M. Robertson, "Control of Width Effects in Small Geometry CMOS Devices", in Proc. Simulation of Semiconductor Devices and Processes Conf. (ed. K. Board and D.R.J. Owen), Swansea, 9-12 July 1984, Pineridge Press, p 547.

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Implementation of the transient temperature model for electron beam annealing of silicon wafers would not have been possible without the help of Dr M.N. Kozicki.

Last, but not least, I would like to thank Mrs E. Paterson for the high quality of typing in this Thesis, and for showing no impatience with the large equations.

CHAPTER ONE : INTRODUCTION

It is the aim of this introduction to outline the importance and uses of modelling and simulation in Complementary Metal-Oxide-Semiconductor (CMOS) Integrated Circuit (IC) technology. The recent surge of interest in the general topic of simulation /1/ has been stimulated by rapid advances in computer technology which have allowed complex physical systems such as those encountered in fields of science and engineering, meteorology, geophysics, etc, to be considered without over-simplification of the model in order to make the solution procedure tractable. Although accurate physical models are important, the sophistication of mathematical analysis used to solve a problem is usually dictated by the level of computational ability available. Consequently, it is generally true that the more comprehensive the computer model is, the more computing power is required. It is interesting to note that integrated circuit simulation is in a unique position since this very activity aids in the development of faster computers which, in turn, offer a more comprehensive simulation capability.

While computer systems have been used to solve problems in academic subjects and fundamental research for several decades, it is only recently that the capabilities of such tools have been realised in both light and heavy manufacturing industries. The computer is now frequently used as a large 'database' in which to store vast amounts of information in a readily retrievable way. Data can be collected from the outside world, subsequently processed, and

then, either presented in tabular or graphical form, or transmitted to another system via a communications network. In particular, Computer-Aided-Manufacture (CAM) is now widely used in the IC manufacturing industry to alleviate administrative and inventorial tasks, and also increase production efficiency. Equally important is the role of computer simulation in the engineering of semiconductor products /2,3,4 /, and none more so than in the case of CMOS technology which has now advanced to such a level of complexity as to require Computer-Aided-Design (CAD) of both circuit layout and fabrication process. A review of techniques used to fabricate integrated circuits which make use of complementary n-channel and p-channel transistors is given in Chapter 2. Most manufacturers are either converting existing NMOS designs to CMOS, or designing in CMOS from the beginning, in order to take advantage of recent advances in CMOS technology. This progress in itself has provided the incentive to further enhance circuit design methodology. Simulation provides an aid in the design of a cost-effective CMOS process to satisfy an IC market which is continually asking for larger and faster chips. While NMOS will remain a mainstream technology, process simulation is a useful tool in the design of a modular process architecture in which NMOS wafers are manufactured as a subset of the CMOS process /5/.

The modelling and simulation of a semiconductor IC is summarised by the flowchart of figure 1.1. The simulation task is generally split into a hierarchy of three levels, which are applied sequentially in the research and development of an IC product. The

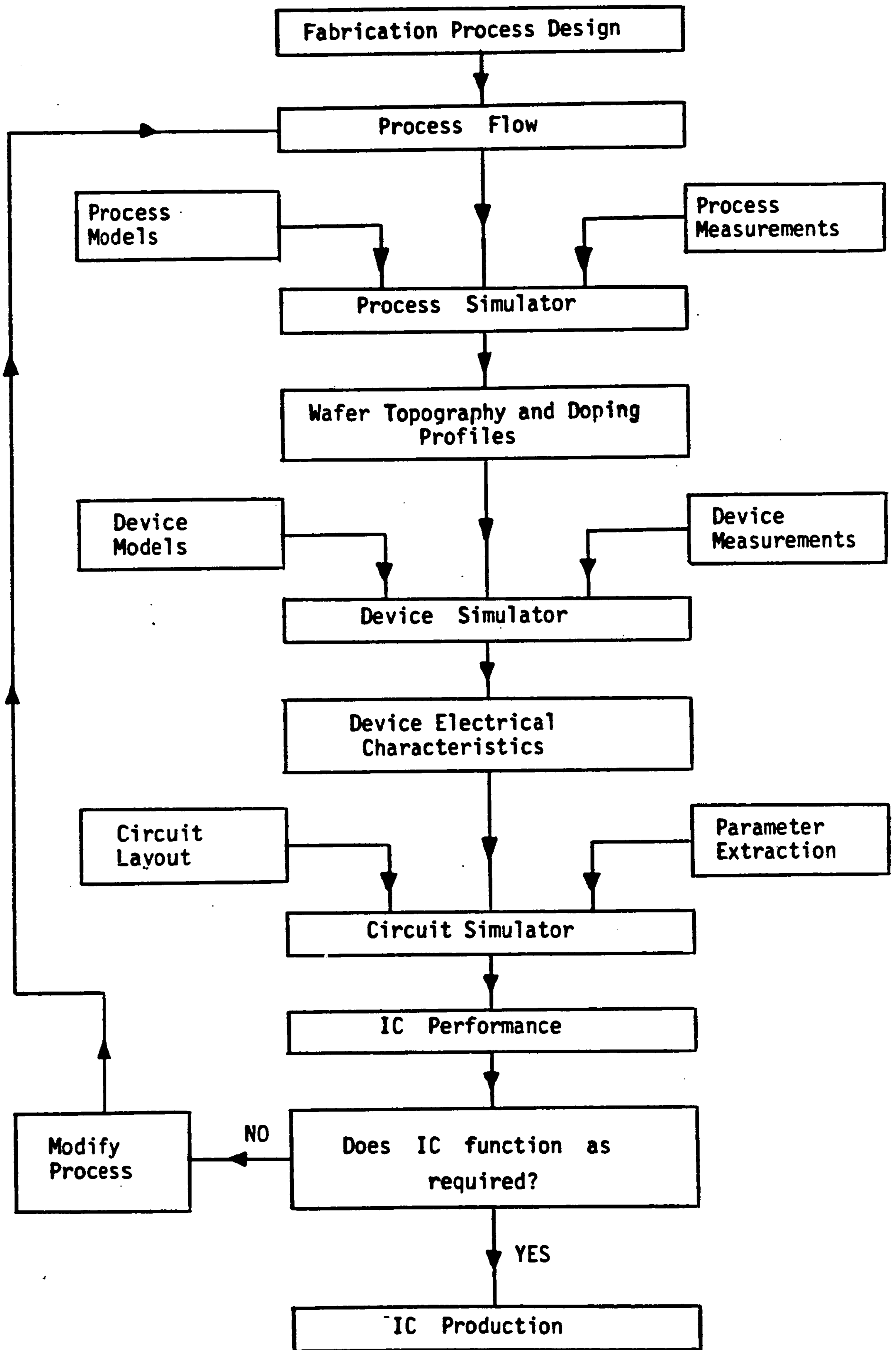


Figure 1.1 : IC Simulation Flowchart

individual roles of process, single device and circuit simulations are now clarified.

The simulation chain begins with a specification of the details of the fabrication process. Usually an existing process is modified, but, less frequently, a novel process must be designed. The process flow comprises a sequential list of all stages in the fabrication procedure. A process model is formulated for each type of process step, eg ion implantation. The process flow and relevant process measurements are passed as input to a process simulator. In general the output from a process simulation program consists of the dopant distributions in the silicon, and details of any other material layer present, for example, silicon dioxide, polysilicon, etc. This information is then fed to a device simulation program which has the capability of modelling the electrical response of basic circuit elements such as resistors, capacitors and MOS transistors. Often, additional parameters for the program are determined from electrical measurements of test structures which constitute part of a process control chip. While models for resistors and capacitors are straightforward, accurate MOS transistor models are relatively sophisticated /6,7/. Results of such simulations are simplified to semi-empirical forms suitable for incorporation in a CAD circuit simulation program /8/. It is important that an automated method exists for extracting parameters for use in such circuit simulations /9/.

In addition to modelling the devices which are designed ex-

plicitly as part of an IC layout, the magnitude of parasitic effects must be determined. Examples of unwanted effects include parasitic MOS transistor action between adjacent diffusion tracks, short and narrow channel effects at small geometries, interlayer capacitance, latch-up in CMOS circuits, threshold voltage shifts, etc. Such phenomena are sensitive functions of the impurity concentration profiles in the silicon. Simulations are required to investigate the operation of circuit designs both at a functional level, assuming a given time for each logic transition, and also at the transistor level, to ensure that 'rise' and 'fall' times of nodes are sufficiently fast for reliable circuit operation. From this general discussion of simulation, it is clear that accurate process modelling is essential for adequate circuit simulation.

While the present work is concerned with the application of computer simulation to CMOS processing technology, the drive to develop process simulators originally came from the requirement in bipolar technology to fabricate narrow transistor base regions reproducibly /10/. Demand for simulations of MOS processes grew in the 1970's, and the first general purpose simulator to be offered to both academic and commercial semiconductor houses was SUPREM (Stanford University Process Engineering Models) /11/. This program allows modelling of one-dimensional (1-D) impurity distributions in silicon and silicon-dioxide, and remains the most widely used process simulator in the semiconductor industry at the present time. Chapter 4 demonstrates how SUPREM (Version II) can be used to simulate a typical CMOS fabrication process.

The main limitation with SUPREM is that it can only simulate profiles in 1-dimension, and therefore it cannot realistically describe small geometry MOS structures. 2 or 3-dimensional programs have been written, but they are very slow and of limited accuracy. A more economical approach is therefore necessary. This has lead to EPIC (Edinburgh Program for Impurity Concentrations), and it is the major result of this research project. Its structure and capabilities are described in Appendix A and in the following chapters.

In a semiconductor factory, process monitoring is vitally important for maximisation of wafer yield and isolation of production problems. Capacitance-voltage (C-V) measurements of MOS capacitors on test wafers are routinely carried out to test for contamination of high temperature furnace tubes. Mobile metal ions alter the flat-band capacitance and therefore threshold voltage of MOS transistors /13/ and are potentially disastrous to MOS processes. Knowledge of the theoretical C-V curve is required to determine flat-band capacitance, defined by the shift between ideal and measured characteristics. A theory for C-V characteristics of non-uniform doping profiles in NMOS technology /14/ is generalised to accommodate CMOS structures in Chapter 5. A comparison of theoretical and measured results provide a check on the accuracy of the 1-D process model, and examples of the calculation of flat-band capacitance are presented.

Process modelling is undoubtedly the weakest link in the

simulation chain of figure 1.1, and lags behind current IC processes in production. Most simulation activity in the past has been concerned with only a few sequential process steps, for example, one ion implantation followed by one subsequent anneal step. The goal of process simulation must be to offer a predictive capability to model complete fabrication processes. However, with the advent of Large-Scale-Integration (LSI) followed by Very-Large-Scale-Integration (VLSI), the routine fabrication in production of devices with dimensions approaching one micron has given rise to a need for two-dimensional (2-D) and three-dimensional (3-D) process simulators. The lateral effects which could previously be ignored now have a dominating effect on device characteristics. The MOS transistor is intrinsically at least a two-dimensional (2-D) device, since a vertical electric field is used to control current flow in a lateral direction. Accurate transistor models, therefore require doping concentration profiles in more than one-dimension. 2-D analytical models for ion implantation and impurity redistribution due to diffusion are considered in Chapter 6.

Transient annealing of silicon using electron beam heating as a promising technique for VLSI technologies. A 3-D model for temperature distribution in a silicon wafer due to a scanning electron beam is presented in the same chapter since the diffusion of heat energy and the diffusion of impurity species at low concentration are described by the same differential equation i.e. Fick's law.

While analytical techniques are suitable for modelling the

diffusion of low concentration impurity profiles in non-oxidizing furnace ambients, a more sophisticated model is required to simulate the high concentration profiles in diffused source/drain regions of the wafer. Chapter 7 describes how such a model can be used to predict the effective channel length of both n-channel and p-channel MOS transistors.

A model for simultaneous diffusion and local oxidation of silicon (LOCOS) has been developed to simulate narrow channel effects in the MOS transistor. This complex moving boundary diffusion problem is dealt with in Chapter 8. A precise estimate of effective channel width is only possible through a combined use of 2-D process and device simulators. A non-planar device analysis is beyond the scope of this thesis, however it is shown that simulation results are consistent with MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) electrical data.

This brief thesis outline demonstrates many of the problems which are inherent in any description of process simulation: individual problems are difficult and must be treated in some depth, but there is also a complex interaction between process steps. Any successful software package must therefore be able to describe individual process steps, and also their aggregation into a complete process. The approach which has been used in this thesis is to describe the individual topics in the following chapters, and to give an overview of the program architecture of EPIC in Appendix A.

CHAPTER TWO : REVIEW OF CMOS TECHNOLOGY

Complementary Metal-Oxide-Semiconductor (CMOS) technology was first proposed by Sah and Wanlass /12/ in 1963 for circuit applications which require very low static power consumption. Figure 2.1 shows a static three-input NAND gate in which a p-channel MOS transistor complements each n-channel MOS transistor. A logic '1' is required at all three inputs to give an output of '0'. Because no dc path exists to ground, current is only consumed during switching.

CMOS circuits can be fabricated using either p-wells, n-wells or both n-wells and p-wells, i.e. twin wells. Early CMOS used a p-well as shown by figure 2.2 because boron was the only element available that would form deep but lightly doped tubs. Use of an n-type starting wafer was compatible with PMOS, the mainstream integrated MOS technology of that time. In this approach n-channel transistors are fabricated in the p-well and p-channel transistors in the n-substrate. A metal gate electrode is deposited and patterned after the source and drain regions have been diffused into the wafer. To allow for misregistration, which always occurs to some extent, a large safety margin is used to ensure that the metal overlaps with the diffusion regions. Only then can a complete channel form when the gate is appropriately biased. Metal gate CMOS parts are therefore slow due to a large 'Miller' feedback capacitance between the gate and source/drain regions.

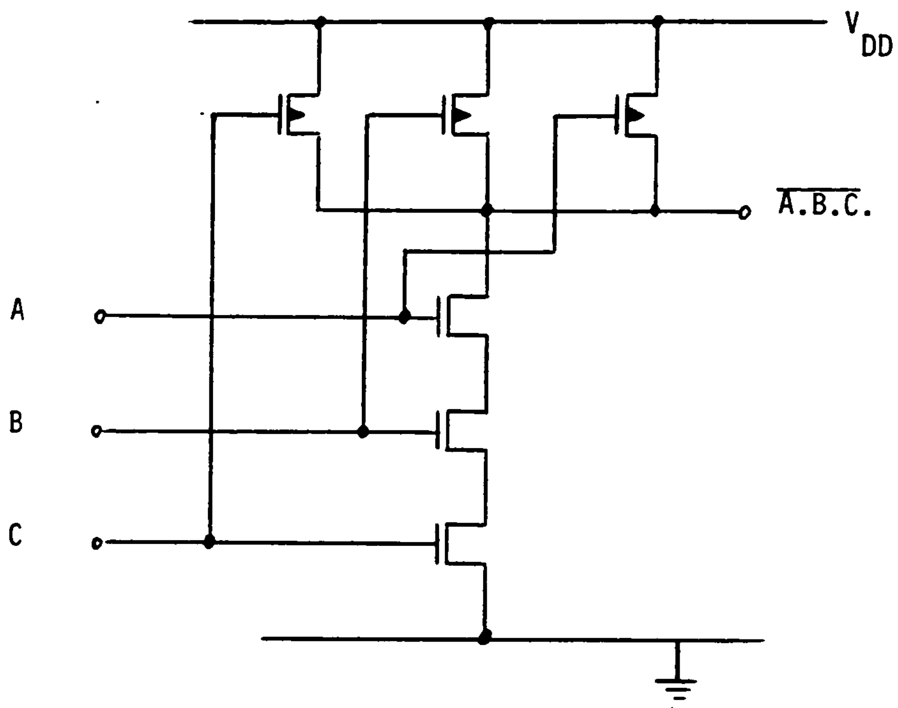


Figure 2.1 : Three-input CMOS NAND gate

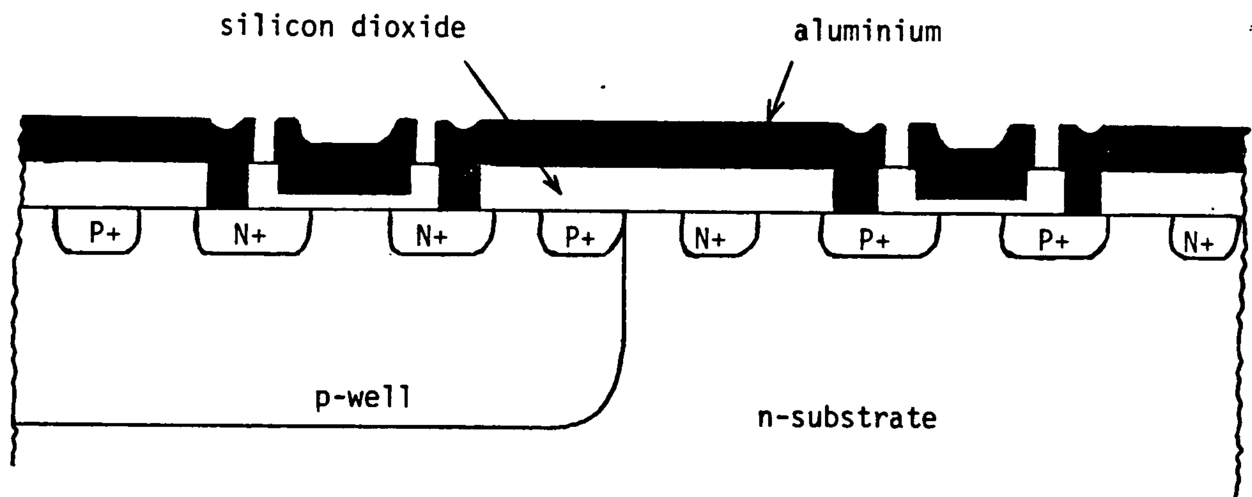


Figure 2.2. : P-well metal gate CMOS cross-section.

Throughout the 1960's and early 1970's, static CMOS circuit designs were wasteful of die area and consequently lagged behind PMOS and bipolar technologies. However, the advantage of very low power dissipation allowed CMOS to be used in specialised products such as calculators, wristwatches and other portable products. Renewed interest in CMOS was stimulated by more inspired design practices through the use of clocked circuitry /242/.

Subsequently, faster circuits were fabricated using a polycrystalline silicon or 'polysilicon' gate electrode which allows the diffused source and drain regions to be formed after polysilicon deposition and self-aligned to the gate edge as shall be shown in the description of a silicon-gate CMOS process to follow. RCA developed closed COS/MOS logic or 'C^2L CMOS' where the gate of the MOSFET completely surrounds the drain. This technology was used in a 1K static random access memory (RAM) /243/ and an 8-bit microprocessor /244/.

By the end of the 1970's, large NMOS circuits were dissipating up to 1 watt of power, which is dangerously close to the limit for normal plastic packaging. High temperatures lead to aluminium electromigration and other reliability problems. However, CMOS circuits were not subject to this problem and, in addition the p-channel transistor found uses as an active pull-up device in dynamic circuitry. The use of twin-wells allowed optimisation of each transistor type independently /246, 295/, and the flexibility of CMOS allowed other types of devices to be fabricated on the same wafer. Hitachi

for example used a buried-junction FET of JFET as part of a static RAM cell and the intrinsic n-p-n bipolar transistor of the p-well process to boost the current of output buffers /245/. Motorola announced a high speed CMOS logic family as a low power alternative to LSTTL /247/. Matsushita /128/ developed an n-well CMOS process which replaced all furnace doping steps by ion implantation technology. The speed, layout density and power dissipation of circuits could be optimised by designing some sections in NMOS and others in CMOS on the same die /248, 249/.

Since logic levels swing all the way between the supply rails, noise immunity is high and CMOS circuits find applications in harsh environments such as down drilling wells or inside engines /250/. A high demand for CMOS circuits and advancing fabrication equipment technology has helped to increase process yields and lower costs so that CMOS is now often preferred to NMOS /251-254/.

Latest circuits optimise speed and layout density by the use of CMOS domino logic /255/ which is demonstrated in figure 2.3. This dynamic technique requires only a single clock signal, and is particularly effective when the logic gates are complex. When the clock ϕ is low, nodes P1 and P2 are pre-charged to V_{DD}. The inputs are then applied, and when ϕ goes high, P1 and then P2 are conditionally discharged in a ripple or 'domino' fashion. Domino CMOS has been successfully used in the Arithmetic Logic Unit (ALU) of a single chip 32-bit microprocessor /256/ at AT & T Bell Laboratories. Care must be taken in pipe-lined data paths to avoid 'race condi-

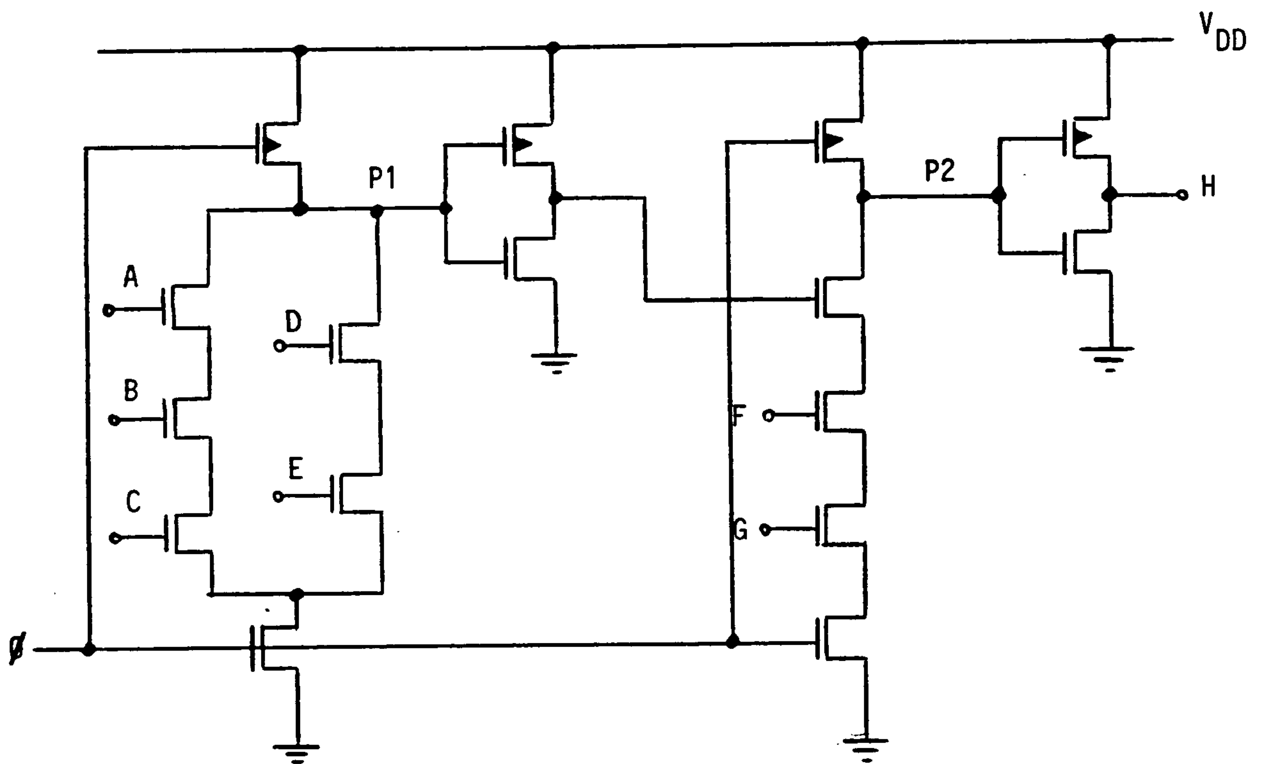


Figure 2.3 : CMOS Domino Logic

(A-G are inputs, H is the output and Ø is the clock)

tions' whereby false outputs appear momentarily before a valid logic level is attained. Instead of using n-channel devices for all logic blocks, p-logic and n-logic stages can be alternated to give race-free operation. Although discharge times are longer in the p-logic blocks, this arrangement offers a higher degree of logic flexibility and has been termed 'no race' or NORA CMOS /257/.

CMOS is also pervading the semiconductor memory market, and access times of static RAM circuits are reported to be as fast as NMOS versions /258/ and even bipolar ECL designs /259/, but with greatly reduced power consumption. N-well CMOS has been used in preference to p-well for both a dynamic RAM /260/ and a read-only memory (ROM) /261/. NMOS dynamic RAM's require a negative back bias or 'charge-pump' to sweep up injected carriers, however, this is not necessary in CMOS, and the use of ground potential in a p-substrate is more effective /283/.

Analogue or linear design in NMOS technology has been made difficult by the assymetric electrical characteristics of enhancement and depletion transistors. The complementary enhancement transistors of CMOS are much more suited to such applications and many analogue CMOS circuits bear a close resemblance to their bipolar equivalents /262/. Efficient CMOS operational amplifiers have been presented /263, 264/. Switched capacitor filters implemented in CMOS technology are finding applications in high frequency communication systems /265/ and in speech synthesis techniques /266/. The use of standard cells greatly reduces the time required to com-

plete a circuit design. Both analogue and digital functions can be designed as blocks and then inserted into a library for use in different systems /267/. Automatic routers are currently being developed to interconnect library cells by optimisation of data paths which are represented by vectors.

The gate array or uncommitted logic array (ULA) comprises a collection of functional blocks which are not linked by interconnects until the metallisation stage /298/. Although a high degree of redundancy is inherent in such semiconductor products, a fast turn-around time is possible and arrays of 20K gates have been reported /268/. In such temporarily uncommitted designs, the number of input and output signals ('fan-ins' and 'fan-outs') is not usually known. The difficulties encountered in designing ratioed NMOS circuits to deal with uncertainties in loading between stages are not nearly so critical in CMOS.

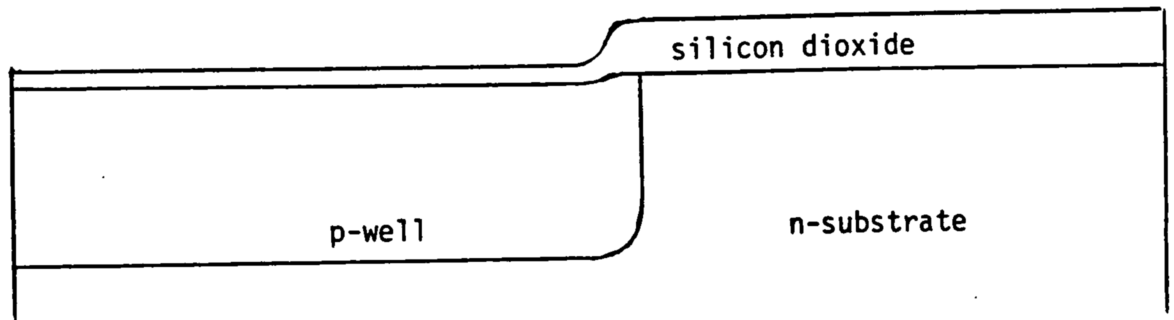
Since a high percentage of die area is occupied by interconnects, a much more dense circuit is possible with the use of multilevel interconnects /276/. One of the major problems currently being encountered by the semiconductor industry in the development of VLSI processes is the fabrication of reliable parts using double-level aluminium /269, 276, 289/. In the future CMOS wafer topography will move further away from the traditional isoplanar structure and progressively more three-dimensional, hence requiring a more sophisticated hierarchical design methodology /270/.

Process simulation is currently struggling to keep pace with rapidly advancing processing technology. The following 'industry standard' p-well CMOS process is chosen as the subject for the present modelling activity.

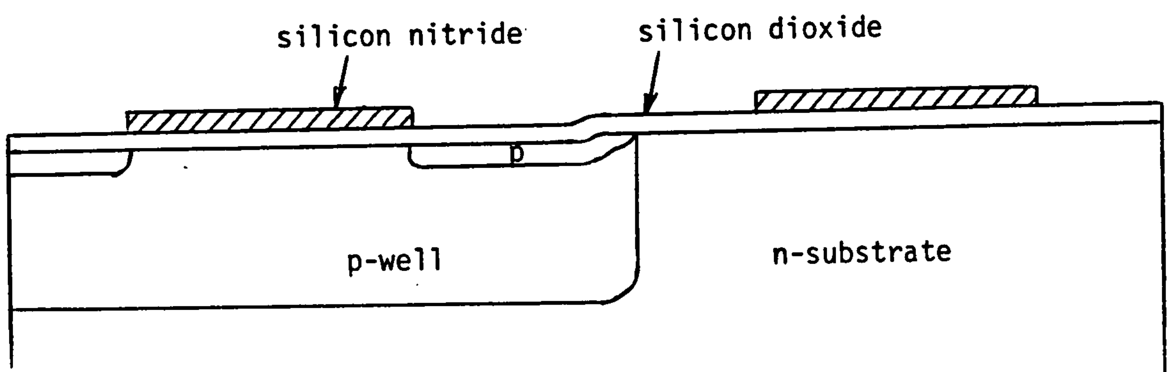
2.2 A TYPICAL CMOS PROCESS FLOW

Virtually all silicon for integrated circuit fabrication is prepared by the Czochralski growing technique /271/. This method allows simultaneous doping of the silicon, but as the silicon crystal grows, the melt becomes progressively enriched with impurities due to segregation effects between the liquid and solid phase. As a result of this, the dopant concentration in the crystal is non-uniform and when the material is sawn into slices, a variation in doping level is found not only from wafer to wafer, but also radially across each wafer. Since all starting wafers show a large tolerance in electrical resistivity, implantation of ions into high resistivity starting material is used to dope the silicon surface to a high degree of precision.

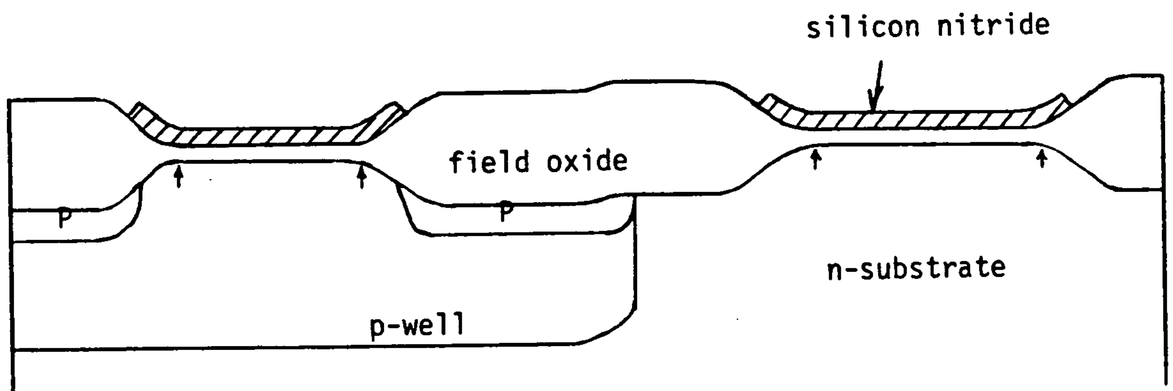
Figures 2.4(a-e) show several key stages in the fabrication of a silicon-gate p-well CMOS wafer. In the description to follow, details of photolithography /273/ are omitted for simplicity. Dopant concentration is fixed in the n-substrate by ion implantation of phosphorus ions ($^{31}P^{+}$) followed by a high temperature drive-in cycle in an oxidising ambient. After photoresist is deposited and patterned, the unprotected regions of oxide are etched in buffered hy-



(a) p-well formation

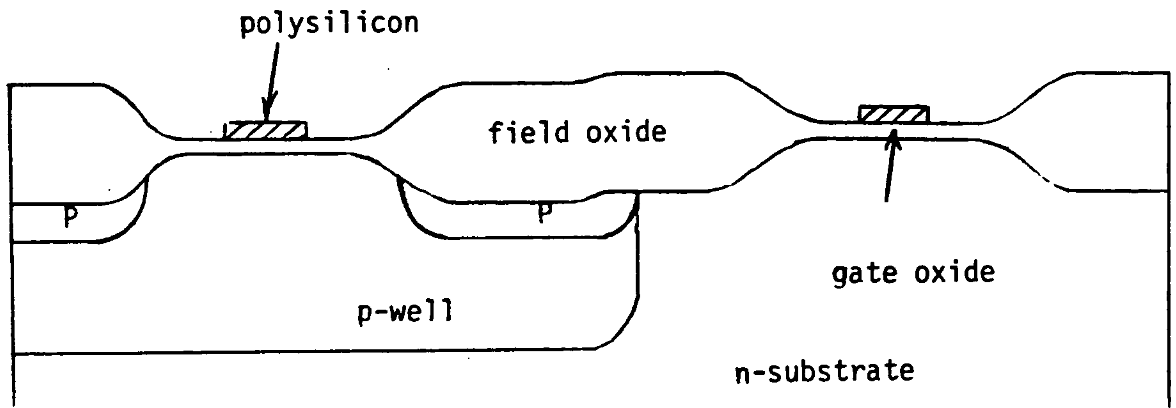


(b) definition of active transistor regions

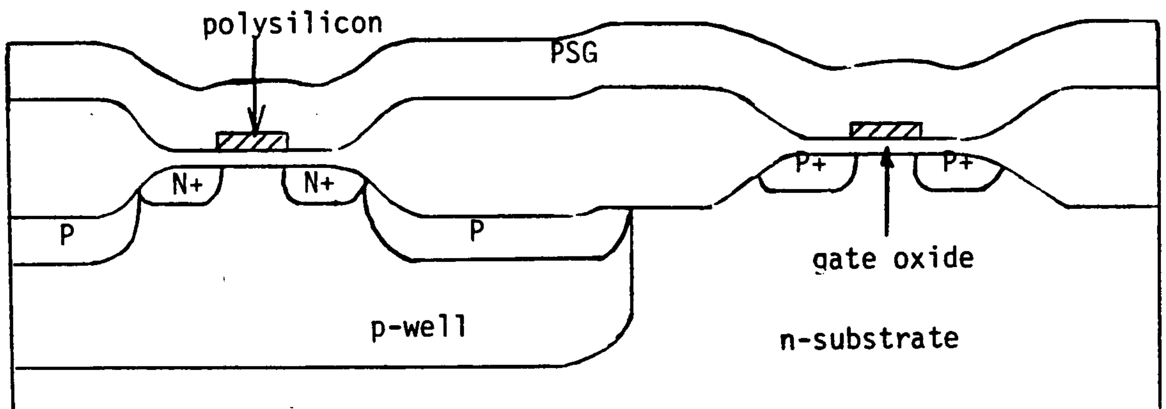


(c) field oxidation (arrows indicate position of silicon nitride formation).

Figure 2.4 : Key stages in a typical CMOS process.



(d) definition of polysilicon gates



(e) cross-section of finished wafer

Figure 2.4 (continued) : Key stages in a typical CMOS process

drofluoric (HF) acid to define the p-well regions. Boron ($^{11}B^+$) is then implanted and diffused into the wafer at high temperature to form net p-type tubs as shown by figure 2.4(a). An oxide step is necessary at this stage in the process in order that subsequent layer masks can be aligned to visible p-well boundaries. For this reason, photoresist alone cannot be used as a mask against p-well implantation. This oxide step is often omitted in cross-sectional views.

Next the oxide layer is stripped, and a fresh 'pad' oxide is grown on which to deposit a layer of silicon nitride (Si_3N_4) at low pressure using chemical vapour deposition LPCVD /197/. Photoresist is patterned to leave the active device regions covered. The nitride in the field regions is then etched in a plasma /272/ as shown in figure 2.4(b). The lateral extent of the etch is important because it influences the final effective channel width of the MOSFET.

With the n-substrate region covered with the photoresist, boron is implanted into the field regions while the n-channel active device regions are masked by the nitride layer as in figure 2.4(b). After a neutral ambient drive-in, the thick field oxide is grown using local oxidation of silicon (LOCOS) /274, 275/ in burnt hydrogen, with the addition of HCl gas to suppress the occurrence of oxidation-induced stacking faults and to getter sodium ion contamination /41, 42, 111, 116, 118/. Figure 2.4(c) shows the wafer topography after field oxidation, and the situation of the channel stop (CS) region of boron which suppresses parasitic n-channel MOSFET ac-

tion in the p-well field region.

An n-type field implant in the n-substrate region is not usually required since, contrary to the behaviour of boron, phosphorus tends to pile up at the surface of the silicon.

The stress induced during local oxidation causes the edges of the nitride layer to bend upwards like a 'bird's beak'. Next the oxynitride, nitride and pad oxide layers are removed and a dry oxidising ambient is used to grow the gate oxide. During field oxidation, silicon nitride forms at the Si - SiO_2 interface under the edge of the nitride mask /277/ as shown by the arrows in figure 2.4(c). At this place, growth of the gate oxide is impeded and inspection of the wafer through a high power optical microscope reveals a 'white ribbon' around the active regions. Such oxides exhibit low breakdown voltages and also give rise to poor subthreshold device characteristics. This problem is remedied by the use of a sacrificial gate oxide which is grown and then etched back before a second and final gate oxide layer is formed /278/.

No threshold adjust implant is required if the source/drain implant is used to dope the polysilicon. In this approach, the polysilicon is heavily doped n-type (N+) in the p-well regions and heavily p-type (P+) in the n-substrate regions /246/. Judicious choice of doping level in each region allows NMOS and PMOS threshold voltages in the ranges 0.6V to 1.0V and -0.6V to -1.0V respectively. However, polysilicon tracks which cross well boundaries must be

'boot-strapped' with metal to prevent the formation of rectifying p-n junctions.

Modern CMOS processes use LPCVD of polysilicon /280/ which is then blanket doped with phosphorus by either a high temperature furnace treatment or ion implantation to compensate the part of the boron source/drain implant which remains in the polysilicon. While the n-channel MOSFET remains unaltered, the work function in the p-channel transistor changes such that an extra surface implant is required to achieve a useful value of threshold voltage. If the concentration of phosphorus in the n-substrate region is reduced, the threshold voltage of the parasitic field MOS transistor becomes unacceptably low. Hence the n-substrate region is implanted with boron and the dose of this implant is typically high enough to invert the surface of the silicon to p-type. When this occurs, the p-channel MOSFET operates as a buried channel device /279/. To avoid the use of an extra masking stage, a non-selective threshold implant can be used provided the p-well concentration levels are reduced to compensate for the addition of more boron later in the process flow.

The polysilicon is patterned to define MOS transistor gates and interconnecting tracks as indicated in figure 2.4(d). A high degree of control in the lateral extent of the etch is necessary to ensure a low tolerance in the effective channel length of transistors /281/.

A further masking stage is required for each of the N+ and P+ source/drain implants. If P+ polysilicon is retained in the process, a thin layer of oxide is grown on the polysilicon to prevent counter doping of the gate electrode by the heavily phosphorus-doped phosphosilicate glass (PSG) which is deposited to isolate the polysilicon and aluminium layers.

A high temperature treatment follows to repair lattice damage and decrease sheet resistance in the source/drain regions and also to flow the PSG layer over the surface of the wafer. Contact cuts are etched through the oxide in preparation for aluminium deposition by electron-beam evaporation or sputtering /282/. A layer of silicon dioxide or silicon nitride is used to passivate and protect the finished wafer. Only the bonding pad areas remain open at the surface to allow connection of the integrated circuit to a suitable package. Figure 2.4(e) shows the final CMOS wafer cross-section, where contact cuts and metallisation have been omitted for simplicity.

Although MOS technologies have been traditionally referred to as 'iso-planar', the wafer topography and doping profiles are clearly 3-D in nature. Adequate representation of cross-sections such as that depicted in figure 2.4(e) necessitates multi-dimensional process modelling. Simulation of lateral effects in wafers is particularly attractive as an engineering tool since no method exists of experimentally profiling silicon in more than 1-D.

A variety of fabrication options are currently being investigated to extend CMOS technology through VLSI (Very Large Scale Integration) and into ULSI (Ultra Large Scale Integration) levels of complexity. Some form of simulation is necessary to aid in the development of these processes and so a short review of the current status of advanced CMOS is now presented in order to set a perspective for simulation effort in the future.

2.3 ADVANCED CMOS TECHNOLOGY

It is generally believed in the semiconductor industry that CMOS will be the dominant VLSI/ULSI technology /322/. However, as device geometries are shrunk to one micron and below, a variety of parasitic effects influence device operation.

It has been observed that α-particles from the atmosphere or the packaging material of the integrated circuit can corrupt data in dynamic RAM circuits /284/. A single α-particle incident on the silicon wafer generates several hundred thousand electron-hole pairs. If enough minority carriers (electrons in p-type silicon) diffuse into the depletion region of a storage capacitor then a logic '1' can be switched to a logic '0' which then constitutes an erroneous bit of information. If the memory cells are placed in a p-well, the electrons generated in the n-substrate are repelled by the built-in potential of the well-substrate p-n junction, and the occurrence of a soft error is less likely /285/.

Despite this advantage, the use of n-wells is now preferred for several reasons. N-well CMOS uses p-type starting material and so is compatible with NMOS. Carrier mobility is degraded by the presence of dopants of either type and is a function of the total (not net) impurity concentration. Current CMOS circuit designs often rely on the faster n-channel transistors to conditionally discharge output nodes, and such devices in a p-substrate offer a higher gain than those in a p-well.

One of the biggest problems to be overcome in the development of a VLSI CMOS process is the parasitic bipolar mechanism known as 'latch-up' /65-68/. With reference to figure 2.4(e), the vertical n-p-n and lateral p-n-p structures in the p-well CMOS process together make up a thyristor (p-n-p-n device) which, when appropriately biased by a noise spike, gives rise to a sustained current between the positive and negative terminals of the power supply. The latch-up current can only be terminated when the power is switched off, by which time the circuit is likely to be permanently damaged. Because the mobility of holes is less than that of electrons, the gain of the vertical p-n-p in an n-well process is less than the gain of the vertical n-p-n in a p-well process, and hence the n-well process is less susceptible to the occurrence of latch-up.

An increase in the well and substrate concentration levels reduces the risk of latch-up by decreasing the minority carrier lifetime in the parasitic bipolar transistor base regions. Howev-

er, a larger back-gate bias effect /13/ is induced in the active MOS transistors.

Other attempts to eliminate latch-up have included the diffusion of gold atoms into the wafer /286/ or the use of internal gettering /287/ to reduce minority carrier lifetime. The use of Schottky barriers in a CMOS process is also reported to solve latch-up problems /288/.

One of the most effective methods of decreasing the lateral resistance of the well is to use a heavily doped substrate on which a near-intrinsic epitaxial layer is grown. From then on, a normal process flow can be adopted. Both N+ substrates /290, 291, 294/ and P+ substrates /283, 292/ have been utilised, but fabrication costs are high and defect density is increased /296/. Figure 2.5 shows a twin-well CMOS process using N+ starting material. The transition region between the substrate and the epitaxial layer contains point defects which help to getter unwanted impurity atoms from the surface of the wafer.

While these processing techniques reduce the possibility of latch-up occurring, it is still necessary to take precautions at the design level. Input and output buffers for example should be completely surrounded by 'guard-rings' which are hardwired to the power supply to collect any minority carriers in the substrate /258/.

One technology which eliminates latch-up problems is silicon-

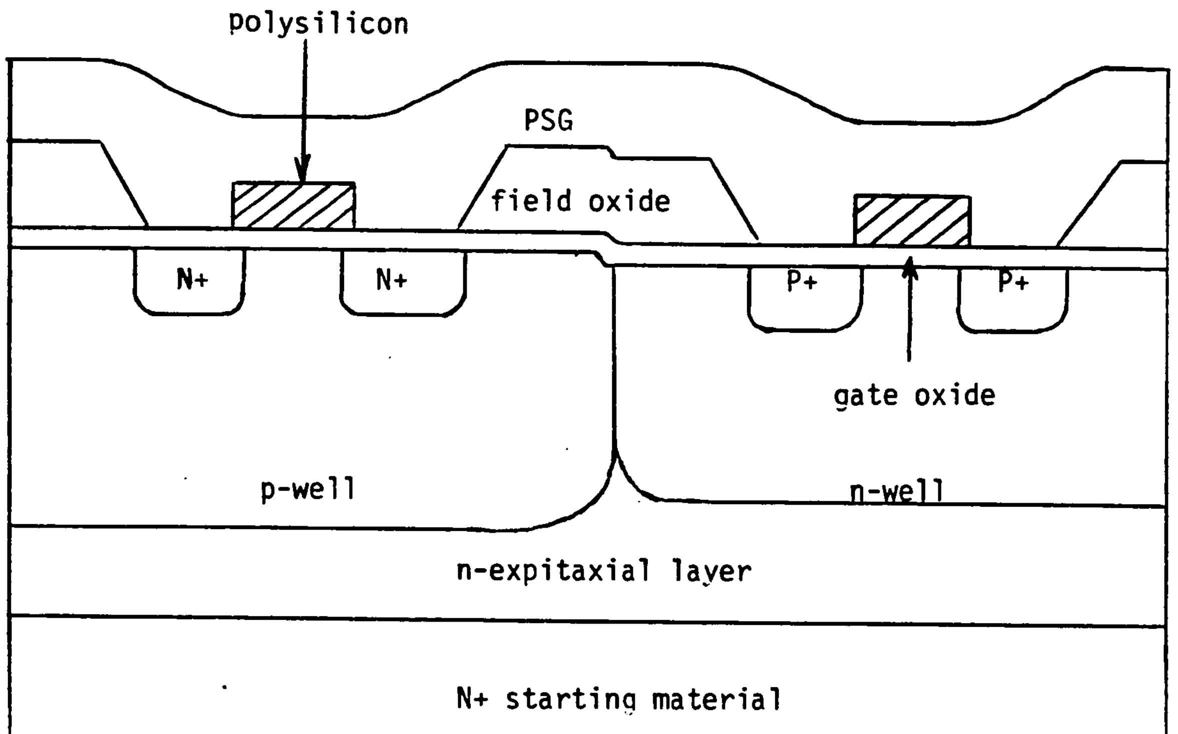


Figure 2.5 : Twin-well CMOS

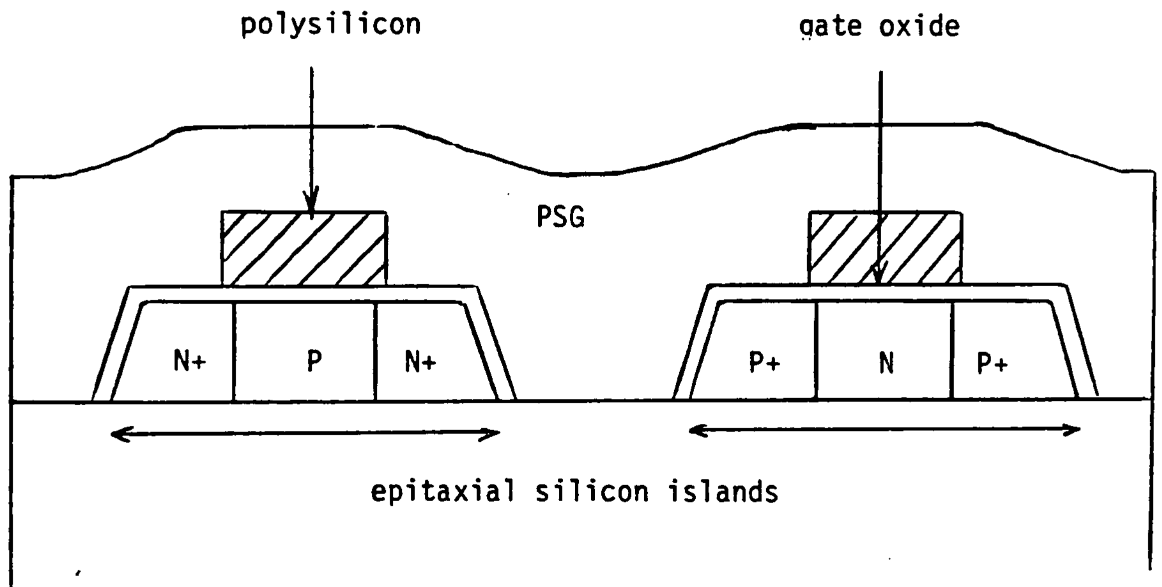


Figure 2.6 : Silicon-on-Sapphire (SOS) CMOS

on-sapphire (SOS) by using an insulating substrate material /297, 298/. An epitaxial layer of silicon is grown on the sapphire, and then selectively etched to form islands in which to form n-channel and p-channel MOSFET's as shown in figure 2.6. Field oxide is not required and the spacing between transistors is only determined by how well the epitaxial islands can be defined. Also no separation is necessary between the diffused N+ and P+ regions on the output node of an inverter hence allowing a high packing density of transistors. SOS circuits boast a low susceptibility to radiation and because the substrate is non-conducting, parasitic capacitances are low. Using similar design rules, SOS is about twice as fast as bulk CMOS in VLSI /300/. High performance applications justify the added processing cost and Toshiba manufacture a 16-bit microprocessor using SOS technology /301/.

Since the fabrication of CMOS/SOS wafers is made difficult by the difference in thermal expansion between sapphire (α - Al_2O_3) and silicon, there is great interest in obtaining an insulating substrate by other techniques. High dose oxygen implantation into silicon wafers followed by an anneal treatment gives a buried silicon dioxide layer with silicon at the surface /302/. Nitrogen can be implanted to form a silicon nitride layer in a similar fashion /303/. Alternatively, a one-micron thick layer of oxide can be grown on the surface of the wafer, and then a layer of polysilicon is deposited using LPCVD. The grained silicon structure is melted and grown into a single crystal by thermal radiation from halogen lamps /304/. Such silicon-on-insulator (SOI) techniques remain

research topics currently and are not yet feasible for the production environment.

As device geometries are shrunk to dimensions below 2 micron for VLSI, a variety of parasitic effects become important for device performance /306,309/, and these are collectively known as 'short and narrow channel effects'. The 2-D nature of device structures can no longer be ignored, and threshold voltage becomes a function of device size /305/.

While the transistors themselves exhibit higher switching speeds, the maximum operating frequency of VLSI circuits is limited by the resistance of diffused regions and polysilicon interconnects which contribute to large RC time delays. Refractory metal silicides can be fabricated on the surface of these doped areas in order to increase their conductivity /253/. Smaller contact openings and more shallow source/drain junction depths also increase the series resistance to transistors /306/. The transconductance of devices with gate oxide thicknesses below 100Å degrades since this dimension is comparable with the thickness of the inversion layer and a large portion of the applied gate-source voltage appears across the channel hence decreasing the effective gate capacitance /306/.

Use of the traditional 5V TTL-compatible power supply causes problems for VLSI MOS devices. As the transistor channel length is reduced, the drain depletion region extends to the source giving rise to unrestricted current flow despite a gate voltage correspond-

ing to the 'off' condition /7, 311/. N-channel devices already require a surface implant of boron to allow the use of an N+ polysilicon gate electrode. To suppress punch-through, an additional deep implant of boron is required to raise the p-type dopant concentration in the bulk while not contributing appreciably to the threshold voltage. A high lateral electric field gives rise to 'hot' carriers which are sufficiently energetic to create free electrons and holes /306/. Substrate currents can initiate parasitic bipolar mechanisms like latch-up. Another is 'snap-back' /299/ which is characterised by a state of negative differential resistance in the I_{DS} - V_{DS} relationship. Since the p-channel MOSFET operates as a buried-channel device, careful process design is necessary to ensure good sub-threshold characteristics /310/.

Despite the above-mentioned complications to basic transistor operation, a process which holds promise for advanced VLSI and ULSI levels of circuit complexity is retrograde well CMOS. Compared to conventional bulk CMOS, the main difference of this approach is that the p-well implant is performed after the active device regions have been formed. A high energy, typically 400 - 600 keV, is used to accelerate boron ions through the field oxide into the underlying silicon /293, 296/. Only a brief anneal is necessary instead of the customary long p-well drive-in step. A channel-stop (CS) region is formed in the p-well field area and boron suck-out due to oxidation is minimised. The net p-type doping concentration reaches its maximum value in the bulk of the transistor active region and suppresses drain-source punchthrough. This process has been ex-

tended to twin retrograde wells /294/, as shown in figure 2.7. Since the tubs form four distinct regions in the silicon, this technology is consequently referred to as 'quadruple well CMOS'.

Because changes in processing technology tend to be evolutionary rather than revolutionary due to the immense cost of introducing changes into a wafer production line, quadruple well CMOS has the potential to be the dominant VLSI/ULSI circuit technology. However, the advancement of this technique to a feasible production process is hampered by the lack of a commercially available ion implanter which is reliable and capable of the high acceleration voltages necessary to implant ions through the thick field oxide.

Even more dense circuit layouts are possible by increasing the level of integration in the vertical direction of the wafer. The use of triple-level polysilicon permits fabrication of very small dynamic RAM cells /312/. A further step towards three-dimensional (3-D) integration is taken by stacked CMOS (ST-CMOS) /313/. In this sophisticated process flow, p-channel transistors are created in a laser-recrystallised polysilicon layer and are placed directly above the n-channel devices.

Since the bird's beak transition region of conventional MOS technologies is wasteful of die area, several new isolation techniques have been proposed for advanced processes /50, 51, 314-317/. The most promising is 'deep-trench' isolation /318/ which has been used to reduce the separation between n-channel and p-channel

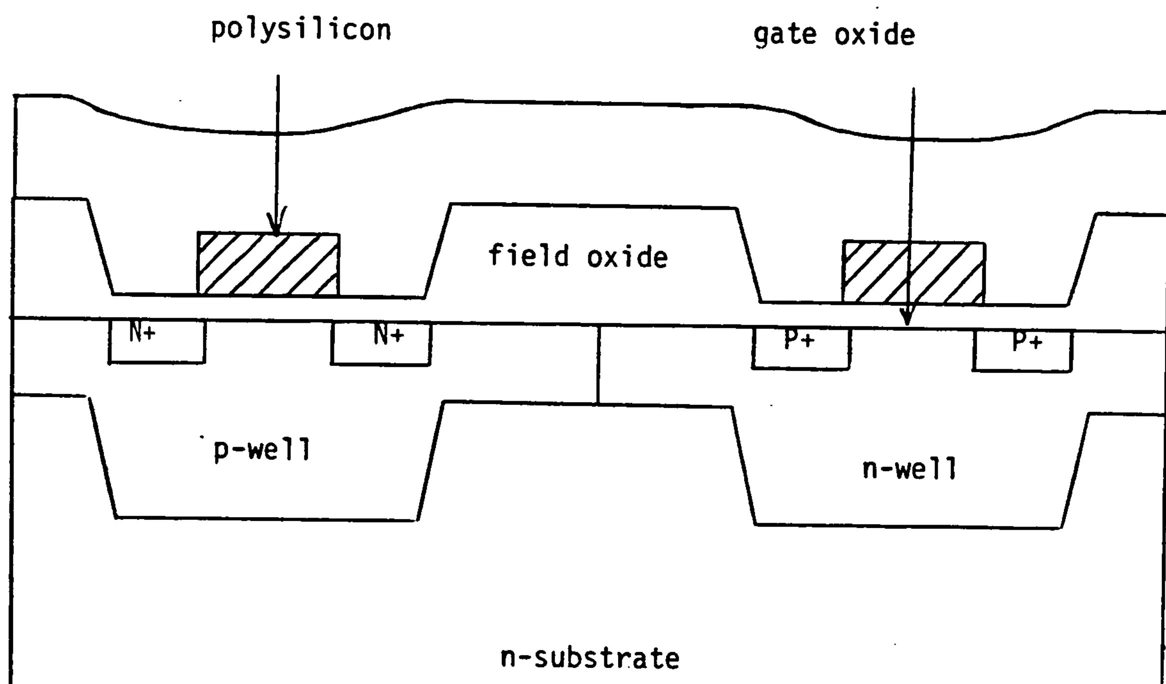


Figure 2.7 : Quadruple-well CMOS

transistors and also increase latch-up immunity. The deep trenches are created using reactive ion etching (RIE). The sidewalls are oxidised and then the pits are filled with polysilicon. The surface of the wafer must be planarised to avoid step coverage problems when the aluminium layer is deposited.

Powerful single-chip silicon systems can be realised by combining bipolar and MOS elements on the same die in a 'BIMOS' process. The feasibility of this approach has already been demonstrated in a dynamic RAM design /319/. Fairchild have developed a complex process which combines bipolar, CMOS and high voltage DMOS transistors /320/. Most of the large semiconductor manufacturers are engaged in research to fabricate BIMOS circuits, but since process details are proprietary, little published material has yet emerged.

It is clear from this review and discussion of CMOS technology that processing techniques are becoming more complex and consequently increased use of computer aids is now required. When used in conjunction with test chip data /321/, computer simulation provides an aid to understanding phenomena, and offers a valuable tool for CMOS process development in VLSI/ULSI.

CHAPTER THREE : REVIEW OF PROCESS SIMULATION ACTIVITY

A large amount of research work on individual process steps, such as ion implantation, diffusion, oxidation, etc., has been reported in the literature. The power of process simulation lies in the combination of models for each fabrication step to allow simulation of complete processes from beginning to end. Several man years of effort is involved in the development of such a simulation package. The realisation of such a project calls on a variety of disciplines including semiconductor physics, processing knowledge, computer programming and applied numerical analysis.

As well as being important for process development and understanding, simulation provides a convenient means of carrying out a process sensitivity analysis to determine those parameters which have a critical effect on device characteristics and thus require a high degree of control on the production line. A process variation analysis has been undertaken by Aoki et al /241/ with the program CASTAM. Herr et al /240/ have reported a statistical modelling approach to determine best and worst case device parameters for circuit design.

While simulation of impurity concentration profiles only is discussed in this thesis, modelling of wafer topography /233/ is becoming increasingly important for VLSI. The most advanced general purpose simulator for dealing with the process steps of lithography, deposition and etching is SAMPLE /231, 232/.

The 2-D models of this program have been applied to the projection printing of positive photoresist /234/ and negative photoresist /235/, and also to the electron-beam exposure of resist /236/. Plasma etching of material layers is a critical process step in MOS technologies. The width of a silicon nitride track defines the effective channel width of the MOS transistor, and the width of a polysilicon track defines the effective channel length, assuming all other offsets are fixed. A high degree of control in etching characteristics is necessary since any variations in nitride or polysilicon linewidths appear as a tolerance on the electrical characteristics of devices. Optimisation of etched profiles is possible using both vertical and lateral etch rate components /237/. Deposition models for electron-beam evaporation or sputtering of aluminium aid in the reduction of step coverage problems /238/.

Several process simulators which model impurity distributions in silicon have been reported in the literature and these are summarised in table 3.1. For comparison, the EPIC program produced in this project has also been included, although it is described more fully later. A 1-D process simulator allows modelling of the impurity profile in the vertical direction in the wafer, but if lateral effects are also important, for example in the length and width cross-sections of a small geometry MOS transistor, then a 2-D simulator is required.

The complexity of mathematical process models means analytical methods can only be applied to certain aspects of the process, and in general, accurate results are only possible by using a numerical method.

Process Simulator	D	References	Place of Origin	Num. Method*	Non-Un. Mesh	High Conc. Diff.	Diff. and Oxid.	Applications
SUPREM II	1	11,97	Stanford Univ.	FD	✓	✓	✓	used extensively
SUPREM III	1	181, 229	Stanford Univ.	FD	✓	✓	✓	N-well CMOS
ICECREM	1	81, 188	Munich Univ.	FD		✓	✓	used extensively
SUPRA	2	16, 202	Stanford Univ.	FD	✓	✓		NMOS
FEDSS	2	17, 230	IBM	FE	✓	✓		N-well CMOS
ROMANS II	2	20-22	Rockwell	SD		✓	✓	N-well CMOS
BICEPS	2	27-29	AT & T Bell Labs	FD		✓	✓	NMOS
LADIS	2	25,26, 180	Siemens	FD		✓	✓	NMOS, DIMOS
Taniguchi et al	2	19	Toshiba	FD		✓	✓	NMOS
RECIPE	2	198	Rensselaer Poly. Inst.	?				NMOS
EPIC	2	31	Edinburgh Univ.	FD	✓	✓	✓	P-well CMOS

* FD = Finite Difference; FE = Finite Element; SD = Semi-Discretisation

Table 3.1 : Review of 1-D and 2-D process simulators

method. Such numerical analyses fall into three categories: the finite difference (FD) method, the finite element (FE) method and the semi-discretisation (SD) method or method of lines.

Advantages are to be gained in the use of a non-uniform mesh where a fine grid is used to accommodate rapidly varying impurity profiles due to ion implantation or thermal oxidation at the surface of the wafer, and a coarse mesh in the bulk where impurity concentration gradients are not large. It is essential to adopt such an approach in the simulation of a bulk CMOS process which makes use of an n-well, p-well or both types of well, in order to reduce computation times.

High concentration ion implantation and diffusion models are required to model source/drain regions in MOS processes. The concentration dependence of the diffusivity gives rise to non-linear diffusion, which cannot be modelled analytically. The 1-D programs SUPREM II /11,97/, SUPREM III /181,229/ and ICECREM /81, 188/ solve for impurity diffusion in inert and oxidising furnace ambients. However, the diffusion coefficient of species in the oxide is very low, and during a non-oxidising (inert) anneal step in the fabrication process, the Si - SiO_2 interface can be approximated by a reflecting boundary. This approach is used by all the 2-D process simulators reviewed. All these programs use a well established numerical method, except in the case of RECIPE /198/ which uses an 'incremental solution method'. The mathematical basis of this work is suspect, and the authors do indeed confess that diffusion results

could be inaccurate by a factor of 2.

The simulation of impurity diffusion during thermal oxidation of the silicon wafer is a complex moving boundary problem. The 1-D programs of table 3.1 model simultaneous diffusion and oxidation without the use of any simplifying assumptions. Simulation of the transition region between the active and field regions commonly known as the 'bird's beak' requires a 2-D model. All attempts to solve this problem so far have been forced to neglect impurity diffusion in the oxide and to model segregation effects purely as an interfacial flux in the form of a boundary condition. In practical situations this is a good approximation, as shall be demonstrated in chapter 8. Instead of a 2-D numerical model, SUPRA /16, 202/ uses a semi-empirical model which can generate only approximate results in general situations, and therefore cannot be credited as a realistic diffusion/oxidation simulator. The model of Taniguchi et al /19/ assumes a bird's beak angle of precisely 45° which rarely occurs in practical MOS processes. FEDSS /17, 230/ models non-rectangular structures but completely neglects impurity segregation effects. An accurate and mathematically valid numerical treatment, however, is used by the programs ROMANS II /20-22/, BICEPS /27-29/ and LADIS /25, 26, 180/.

The 1-D programs SUPREM II and ICECREM are available to anyone from the authors for merely handling costs, and are consequently used extensively in the semiconductor industry. SUPREM III is capable of modelling multilayered structures, for example, polysilicon

and gate oxide in the cross-section through the active device region of the MOS transistor, and results have been presented for an n-well CMOS process /229/.

A 1-D process simulator called PROSIM II has recently been reported by Fair et al /239/. Although the program has been used to predict source/drain junction depths in CMOS, details of the process models have not yet been presented.

In the field of 2-D process simulation, SUPRA, BICEPS and the program of Taniguchi et al have been applied to NMOS technology, and in addition, LADIS allows simulation of DIMOS transistors /13/.

N-well CMOS processes have been simulated by FEDSS and ROMANS II and although no simulation results have yet been presented, ROMANS II is the only 2-D process simulator capable of modelling impurity profiles in silicon-on-sapphire (SOS) CMOS /22/.

From table 3.1, the most popular solution technique is the finite difference method. The alternative finite element method has attractions in that it can use a mesh structure which conforms to the physical boundaries of the device. However, the resultant matrix structure is less amenable to iterative solution. Finite difference methods have been much more widely used both for device and process simulation. It was therefore decided to use finite difference analyses for all the models developed in the course of this project.

The programs reviewed in table 3.1 provide a good starting

point but none of the 2-dimensional packages are yet sufficiently comprehensive to be generally usable. The main features which were considered in the definition of EPIC were:

* 2-D representation
* Use of analytical solutions where possible
* Numerical solution by finite difference methods
* Executable on a small VAX computer
* Modules to describe single process steps
* Linked modules for whole fabrication processes

The program architecture is described in Appendix A, and the single process step modules in the following chapters. By using this approach, it has been possible to devise a program which is unique in its scope of application, but which remains economical to use. This thesis and the previous work by Buttar et al /31/ comprise the first 1-D and 2-D simulation of of a complete p-well CMOS process, and the program may also be applied to n-well or twin-well CMOS structures.

Two features have contributed to the detailed efficiency of EPIC:

(i) use of SUPREM 1-D profiles to define initial mesh conditions for 2-D simulations.

(ii) use of a non-uniform mesh to give an economical representation of deep non-uniform dopant profiles.

Electron-beam annealing is a promising technique which holds promise for VLSI MOS technologies. A simple annealing model for use in the development of scanning electron-beam systems is presented in chapter 6.

CHAPTER FOUR : 1-D PROCESS SIMULATION

4.1 ION IMPLANTATION

Ion implantation is now the principal doping technique used in the fabrication of integrated circuits because it offers several advantages over furnace doping methods. A high degree of uniformity and reproducibility is possible by monitoring the ion beam current. Since the MOSFET is a surface-effect device, the silicon surface must be free of contaminants in order to ensure reliable device operation. Ion implantation can be performed through a passivating layer of silicon dioxide on the wafer surface. In addition, photoresist, silicon dioxide and silicon nitride can be used to mask regions of the silicon from the impinging beam. Implantation is carried out at low temperatures and so no impurity diffusion takes place. This is important in MOS technologies because VLSI devices require highly doped but shallow impurity profiles in source/drain regions to minimise short channel effects /69-71/. In addition source/drain regions can be self-aligned to polysilicon gates hence reducing parasitic gate/source and gate/drain capacitances. Short channel ($<2\mu m$) MOS transistors require a gate adjust implant to fix the threshold voltage and also a deeper implant to suppress drain-source punch-through /83,99/.

The theoretical background for ion implantation is due to

Lindhard, Scharff and Shiott /79/ and this work is known as the LSS theory. An amorphous target is assumed to provide both electronic and nuclear stopping of incident ions and the predicted profile takes the form of a symmetrical Gaussian distribution given by

$$N(x) = \frac{Q}{\sqrt{\frac{\pi}{2}}\ \Delta R_p \{1 + \mathrm{erf}(\frac{R_p}{\sqrt{2}\ \Delta R_p})\}} \exp\{-\frac{(x - R_p)^2}{2\Delta R_p^2}\} \qquad (4.1)$$

where x is distance into the silicon, Q is the implant dose, R_p is the projected range of the ion in silicon and ΔR_p the projected standard deviation or range straggle. The so-called error function is defined by

$$\mathrm{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^x \exp(-\gamma^2) d\gamma \qquad (4.2)$$

The LSS range statistics for R_p and ΔR_p have been computed as a function of implant energy by Gibbons et al /80/. While LSS theory considers amorphous targets, silicon wafers are single crystals, and a certain amount of ion channeling always occurs along major crystallographic directions /85/. Ions which find themselves channeled between adjacent lattice planes penetrate deeper into the silicon and give rise to a 'tail' on the Gaussian distribution. The effects of channeling can be reduced, but not eliminated, by both rotating and tilting the wafer prior to implantation, and also by using a passivating silicon dioxide layer to randomise the ion directions before they reach the silicon /92/.

If the assymetric nature of the distribution is not too

severe then a good fit to the experimental results is obtained by using the third moment ratio estimate or 'skewness' γ which characterises the degree of tilt of the profile. In this formulation two half-Gaussian profiles with different range straggles are joined at a common range /80,100/.

The best fit to experimental profiles is obtained by considering, in addition to the skewness γ, the kurtosis β which indicates flatness at the top of the profile. The four parameters $R_p, \Delta R_p, \gamma$ and β are incorporated into a Pearson distribution of type IV defined by /81,82,103/

$$f_p(x) = k_p \left[b_2(x-R_p)^2 + b_1(x-R_p) + b_0\right]^{\frac{1}{2b_2}} \cdot$$

$$\exp\left\{ - \frac{\frac{b_1}{b_2} + 2a}{\sqrt{4b_0b_2 - b_1^2}} \right\} \arctan\left\{ \frac{2b_2(x - R_p) + b_1}{\sqrt{4b_0b_2 - b_1^2}} \right\} \qquad (4.3)$$

where

$$b_1 = a = - \frac{\Delta R_p \, \gamma(\beta + 3)}{A} \qquad (4.4)$$

$$b_0 = -\frac{\Delta R_p^{\,2}(4\beta - 3\gamma^2)}{A} \tag{4.5}$$

$$b_2 = -\frac{(2\beta - 3\gamma - 6)}{A} \tag{4.6}$$

$$A = 10\beta - 12\gamma^2 - 18 \tag{4.7}$$

The constant k_p is determined from the normalisation integral

$$\int_0^\infty f_p\,(x)\,dx = 1 \tag{4.8}$$

and the complete ion distribution is given by

$$N(x) = Q\,f_p(x) \tag{4.9}$$

For a Pearson type IV distribution β must satisfy

$$\beta \geqslant \beta_{min} = \frac{48 + 39\gamma^2 + 6\,(\gamma^2 + 4)^{3/2}}{32 - \gamma^2} \tag{4.10}$$

Boron profiles in particular are well modelled using this distribution /81,82,92/.

The remainder of this section considers how ion implantation theory may be implemented in process simulation models.

SUPREM II uses joined half-Gaussian distributions for phosphorus and arsenic, and Pearson IV distributions for boron. EPIC uses Pearson IV distributions for all three elements. The values of kurtosis β are taken from ICECREM /81/ and are

$$\beta = \begin{cases} 1.5\ \beta_{min} & ;\ B,\ P \\ \beta_{min} & ;\ As \end{cases} \qquad (4.11)$$

Implantation of ions is rarely performed into bare silicon in MOS processes, but usually through a passivating layer such as silicon dioxide. The basic LSS theory cannot be applied to multilayered structures and only two general theories have been developed to model the range of ions and lattice damage in arbitrary solid targets.

The first method is to solve the Boltzmann Transport Equation /87/ to obtain the implanted profile in 1-D. No generalisation to more than one-dimension has yet been reported, so the method has only limited use in a VLSI process simulation program.

The second method relies on a Monte Carlo technique /88-90, 101,102/, which involves the modelling of each scattering event as a projectile collides with target atoms. Because each ion path must be simulated, the procedure must be repeated very many times in order to build up a statistically valid distribution, and so execution times of Monte Carlo programs are long.

Alternative methods, which are simpler to implement, replace masking layers by equivalent thicknesses of silicon to allow the use of LSS data. Sakurai et al /91/, Furukawa and Ishiwara /93/, and Ryssel and Hoffman /92/ use a density transformation based on the projected standard deviation. If the thickness of passivating layer is d_1 and the range straggle of the incident ion in this material is ΔR_{p1}, then the effective thickness of silicon d^* is given by

$$d^* = \frac{\Delta R_p}{\Delta R_{p_1}} d_1 \qquad (4.12)$$

EPIC uses a transformation based on the projected range, as used by Antoniadis and Dutton in SUPREM II /11, 97/ and Tielert /94/. If the projected range of the incident ion in the masking layer is R_{p1} then the equivalent thickness of silicon is given by

$$d^* = \frac{R_p}{R_{p_1}} d_1 \qquad (4.13)$$

The implantation of ions through multilayered structures gives rise to recoil or knock-on implantation of ions /95/. If the mass of the implanted ions is similar to the mass of the atoms comprising the masking layer, a large fraction of the energy of the primary projectiles can be transferred to the atoms of the masking layer which are themselves implanted into the silicon. Knock-on implantation of silicon and oxygen atoms has been observed to occur during high dose arsenic implantation through oxide into the source/drain regions of MOS devices. However, experimental results

show that the free-carrier mobility is not degraded in those regions /86/.

Sputtering of target atoms occurs for very high implant doses ($>10^{17}$ ions cm^{-2}) and low energies (<10 keV) /92/, but this effect is negligible in all practical situations in current MOS processes.

In order to test the accuracy of EPIC in one-dimension, simulation results are compared with Secondary Ion Mass Spectrometry (SIMS) data /96, 104/ for typical source/drain implants of CMOS technologies. In the present study, SIMS analysis was obtained commercially through Loughborough Consultants Ltd. EPIC uses the LSS statistics of Gibbons et al /80/ in all cases except for the data of range R_p and standard deviation ΔR_p for boron in silicon where the values used are those appearing in the program ICECREM /81/. Figure 4.1 shows a comparison of LSS data and empirically obtained ICECREM data for R_p and ΔR_p for a range of implant energies between 10 keV and 200 keV. Figure 4.2 shows SIMS experimental data for a high dose boron implant through an oxide of thickness 820Å.

Dopant concentration is plotted as a function of depth from the silicon surface, and the concentration of dopant in the oxide layer is not considered.

SUPREM II fits an exponential tail to the Pearson IV distri-

Figure 4.1 : Projected Range and Standard Deviation of Boron in Silicon

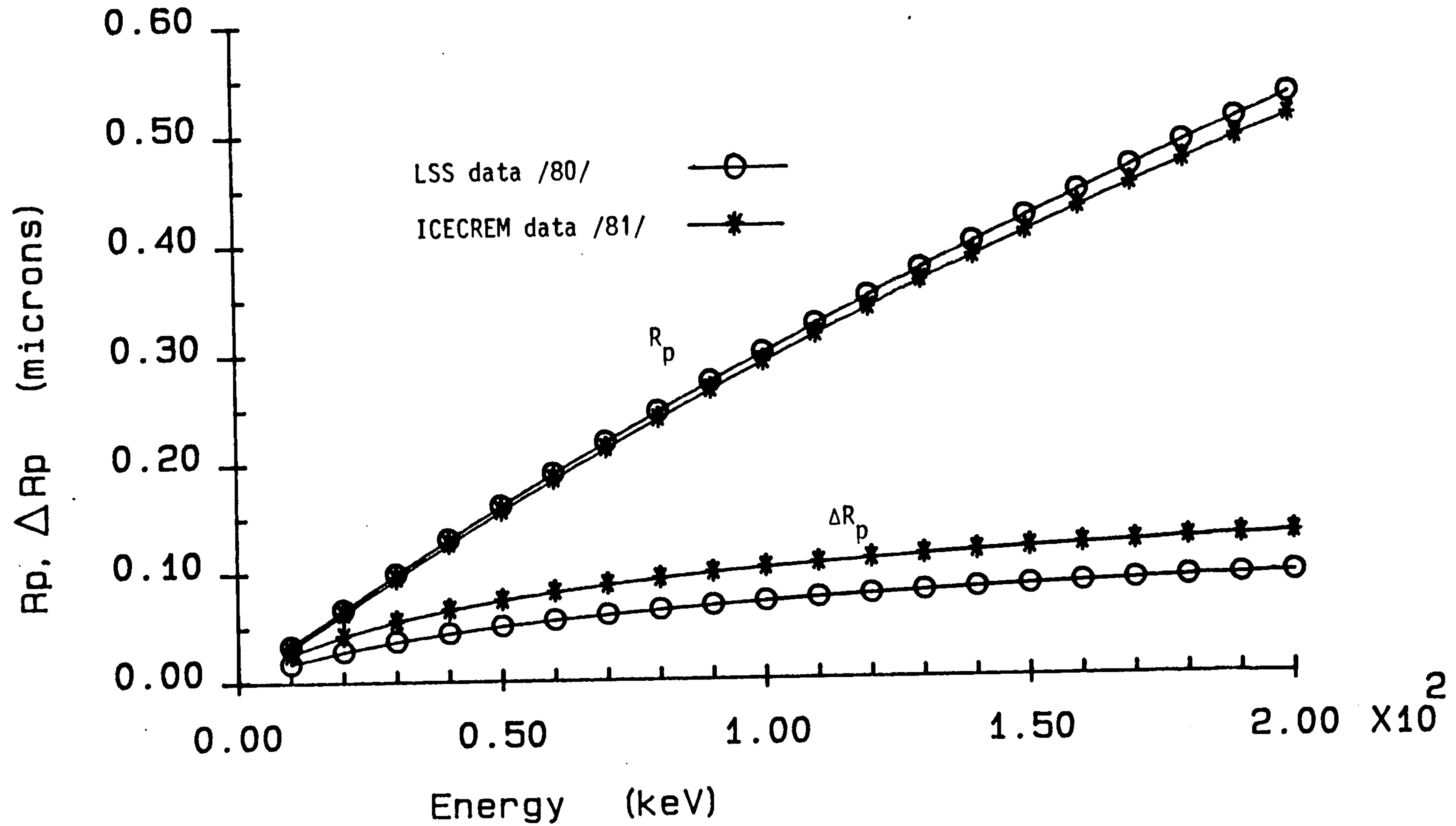
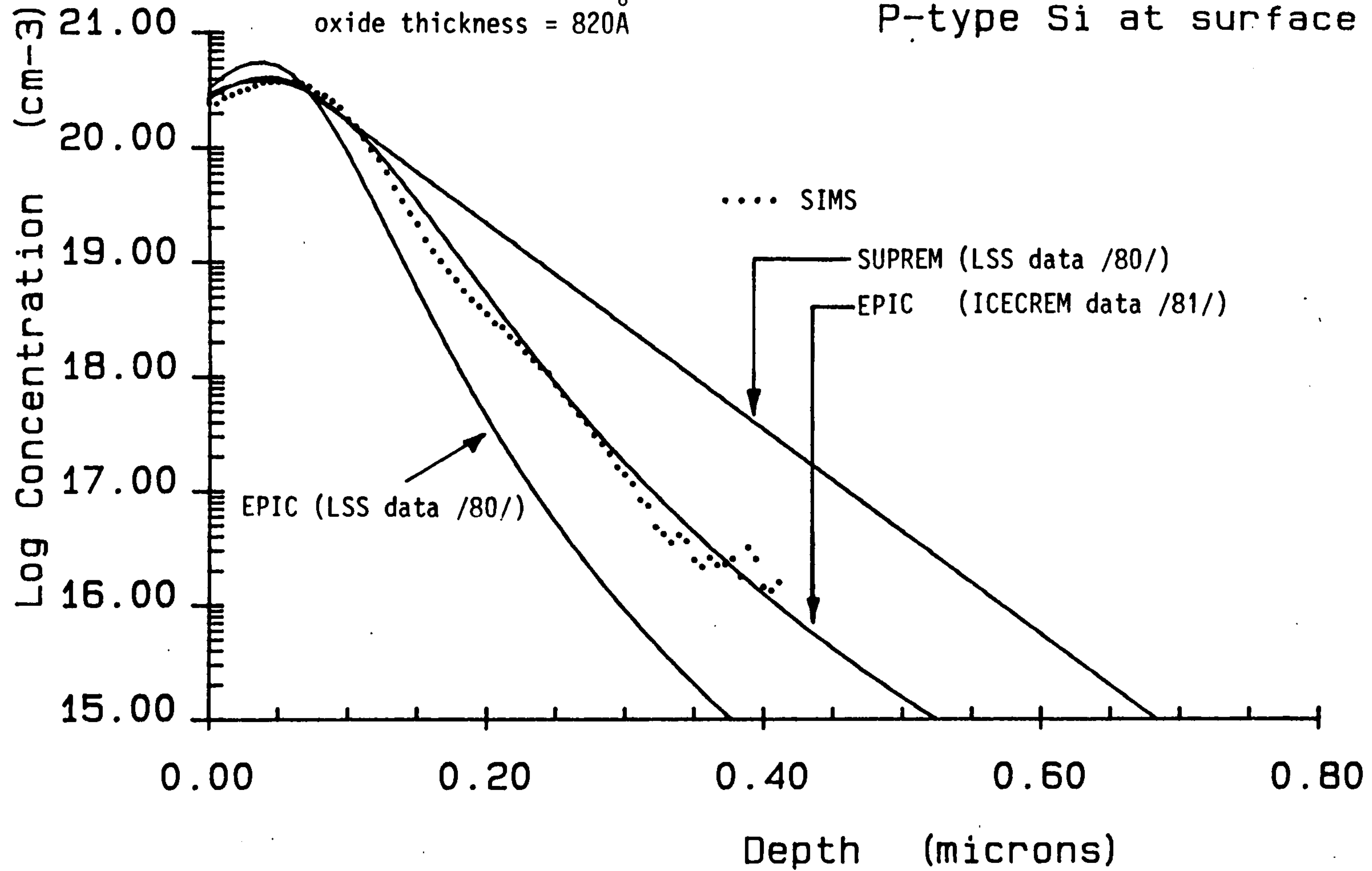


Figure 4.2 : BORON SOURCE/DRAIN IMPLANT



bution which overestimates the extent of ion channeling. Also shown are the simulation results of EPIC using both LSS data and ICECREM data, of which the latter clearly gives the best agreement with the SIMS data. The ICECREM data for boron is therefore also used in the 2-D implantation models in EPIC.

The SIMS results for a phosphorus implant are shown in figure 4.3. The use of joined half-Gaussian profiles in SUPREM underestimates both the surface concentration of phosphorus, and the extent of the distribution tail. EPIC, in contrast, overestimates the surface concentration and slightly overestimates the distribution tail. The top of the experimentally measured profile is much flatter than is expected from LSS statistics, and this discrepancy is attributable to the masking layer of oxide. Both SUPREM and EPIC assume that masking layers have no effect on the range straggle, however Monte Carlo calculations of phosphorus implanted at 150 keV through a 1500Å thick layer of SiO_2 predict a flatter peak region compared with LSS distributions /98/.

Figure 4.4 shows a comparison of SIMS results for an arsenic implant with the joined half-Gaussian profiles of SUPREM and the Pearson IV distribution of EPIC. Conversion of the masking oxide layer to an equivalent thickness of silicon using the LSS data of projected standard deviation in (4.12), or range in (4.13), does not adequately model the stopping power of SiO_2 for As implantation. In the present work, LSS statistics for an energy of 80 keV predict a

Figure 4.3 : PHOSPHORUS SOURCE/DRAIN IMPLANT

$1 \times 10^{16} cm^{-2}$ $^{31}P^{+}$ at 85 keV

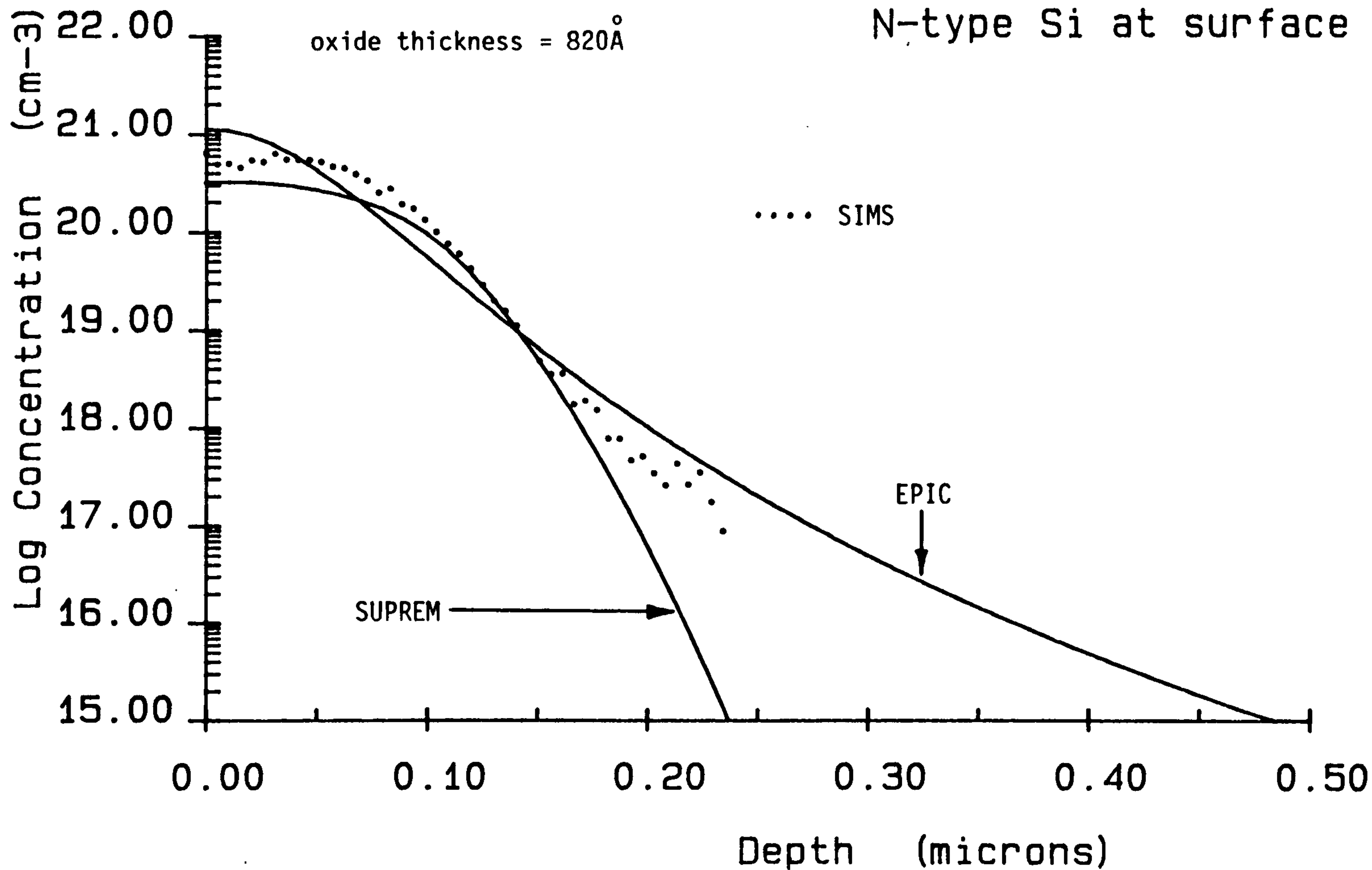


Figure 4.4 : ARSENIC SOURCE/DRAIN IMPLANT

1×10^{16} cm^{-2} $^{75}As^{+}$ at 80 keV

oxide thickness = 705Å

N-type Si at surface

Log Concentration (cm-3)

22.00
21.00
20.00
19.00
18.00
17.00
16.00
15.00

EPIC

SUPREM

0.00 0.05 0.10 0.15 0.20

Depth (microns)

greater stopping power than is experimentally observed. The same effect is evident in the work of Hirao et al /86/ who present SIMS results for 180 keV As implants, but do not consider any model for the stopping of As in SiO_2. Table 4.1 summarises the results using equations (4.12) and (4.13) for both energies.

As implant energy (keV)	d_1(Å)	d^*(Å) eq.(4.12)	d^*(Å) eq.(4.13)	d^*(Å) experimental
80	705	970	869	530
180	970	1318	1185	955

Table 4.1 : Comparison of modelled and experimental equivalent thicknesses of Si for As implanted at two different energies

The values of oxide thickness d_1 were measured using a Nanometrics film thickness computer. In each case, the calculated values of equivalent silicon thickness d^* overestimate the experimentally determined data.

All the As implants dealt with in this thesis are performed at 80 keV, and an empirical stopping power is used for SiO_2 where

$$d^* = 0.75\ d_1 \quad \text{(As only)} \qquad (4.14)$$

Use of this model gives excellent agreement between EPIC simulation

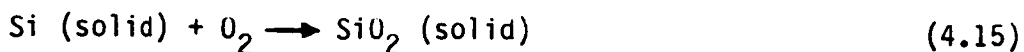
results and SIMS data as shown in figure 4.4, but its accuracy at energies other than 80 keV is uncertain.

4.2 THERMAL OXIDATION

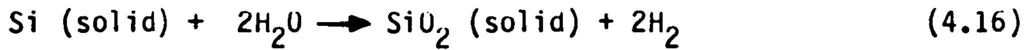
Modern integrated circuit technology relies heavily on thermal oxidation of silicon. In fabrication processes, many high temperature operations are carried out with an oxidising ambient in the furnace tube. MOS technologies require high quality oxides which must be formed in a controlled and repeatable manner. Silicon dioxide is used as a mask against ion implantation or diffusion, and also provides dielectric isolation between adjacent devices or between different conducting layers such as polysilicon and aluminium.

Several techniques are available to form silicon dioxide /107/, but the method most often used for processing steps in MOS technology is thermal oxidation because it offers good oxide film quality and low surface states at the $Si-SiO_2$ interface /112/.

Either dry oxygen or water vapour, usually produced by burning hydrogen in oxygen, can be used to form silicon dioxide through the reactions



$$Si\ (solid) + O_2 \longrightarrow SiO_2\ (solid) \qquad (4.15)$$



$$Si\ (solid) + 2H_2O \longrightarrow SiO_2\ (solid) + 2H_2 \qquad (4.16)$$

Reaction (4.15) is often referred to as 'dry' oxidation and (4.16) as 'wet' oxidation, and the rate of wet oxidation is substantially greater than that of dry oxidation /36,42,110,111/.

When oxidation occurs, the Si-SiO_2 interface moves into the silicon with an accompanying volume expansion. One unit of silicon dioxide is produced by α units of silicon where the constant α is 0.44. The Deal-Grove law /36/ for oxide growth in 1-D is given by

$$x_0^2 + Ax_0 = B(t + \tau) \qquad (4.17)$$

where x_0 is the oxide thickness, t is time, and, B and B/A are the parabolic and linear rate constants respectively. τ is a time corresponding to an initial oxide thickness x_i and is given by

$$\tau = \frac{(x_i^2 + Ax_i)}{B} \qquad (4.18)$$

This model is accurate for oxide thicknesses between 200Å and 20,000Å over a temperature range 700°C - 1300°C /105-107, 110, 111/. Wet oxide growth below 200Å is also well modelled by (4.17), but in the case of dry O_2 an accelerated rate is observed for the first 200Å of oxide growth.

The mechanisms of thin oxide growth in dry O_2 are as yet uncertain. The initial theory of Blanc /108/ gives good agreement with the data of Irene /109/ over the temperature range 780°C to 980°C. However the pressure dependence of the reaction rate is not consistent with the data of Van der Meulen and Ghez /113,114/. Hu /115/ presents a general model which reduces to the Deal-Grove law and the Blanc law as two special cases, but this theory has not been tested experimentally to any great extent.

Since the minimum gate oxide thickness considered in the present simulation activity is 500Å, the details of the thin oxide regime can be neglected and the simple Deal-Grove model is sufficiently accurate for engineering purposes. The SUPREM II model for thin oxide growth involves multiplication of the linear rate constant B/A by a factor of 10 during the first 200Å of oxide growth in dry O_2 /11,97/.

In most MOS processes, chlorine-containing gases are introduced into the oxidising ambient to improve both the oxide and underlying silicon properties. The addition of a few per cent HCl to a dry oxidising ambient results in a significantly greater oxidation rate /117/. Conversely, HCl gas decreases the oxidation rate of wet oxygen /118/, which is apparently due to the reduced H_2O vapour pressure. Similar results are observed with the addition of trichloroethene (TCE) /119/ to the furnace ambient, but as in the case of HCl, the mechanisms of the interface reaction are not fully

understood.

The oxidation reaction rate is very sensitive to the composition of the oxidising ambient and even trace amounts of H_2O, eg 20 ppm, result in an accelerated rate in dry O_2 /120/. Consequently in a practical situation, it is difficult to predict oxide thickness as a function of oxidising time, and for simulation purposes, oxide growth parameters must be fitted empirically.

High concentration levels of dopants enhance oxidation behaviour /121,122/, but the effect is not important for most processes because the highly doped source/drain regions of the wafer are not usually subjected to an oxidising anneal.

The field oxidation step of current bulk MOS processes in production requires a furnace treatment of many hours at a temperature of $900^{o}C$ to $950^{o}C$ to grow an oxide layer thickness of around one micron at atmospheric pressure. There is therefore great interest in using high pressure systems to accelerate oxide growth rates and decrease processing times of wafers /123-125/. High pressures allow the furnace temperature to be reduced so that redistribution of impurities in channel-stop regions between transistors can be minimized.

The use of polycrystalline silicon or 'polysilicon' as a gate material in MOS technologies is now standard practice. Thermal oxi-

dation of polysilicon layers is used to provide dielectric isolation for multilayer structures. The grain structure of polysilicon results in a non-uniform oxide layer thickness on the surface of the polysilicon, and because high doping levels are required for low sheet resistances, concentration-enhanced oxidation is observed /126/. The oxidation of polysilicon is therefore a complex process and no good simulation model exists at the present time.

4.3 DIFFUSION

4.3.1 General Discussion of Diffusion

High temperature diffusion of impurity species is fundamental to the formation of doped regions in silicon wafers. Impurity atoms can be introduced into silicon using the following methods /127/: diffusion from the vapour of a chemical source, diffusion from a doped oxide glass, and diffusion from an ion implanted layer. The anneal and drive-in of ion implanted profiles is the most important technique for doping the silicon substrate in modern MOS processes. It is advantageous to have a fully implanted CMOS process for VLSI /128/, but often a gaseous source is used to saturate the polysilicon layer with phosphorus. Knowledge of the doping profile in the polysilicon gate material is required for prediction of the threshold voltage of MOS transistors /129/.

The subject of solid state diffusion in single crystals is well studied in the literature. A detailed account of atomistic diffusion on a microscopic scale is given by several authors, eg Fair /42/, Rupprecht /130/, Antoniadis /131/ and Tsai /127/, and so only a brief description is necessary here.

It is believed that both vacancies and self-interstitials are intrinsic point defects in silicon. A vacancy is created when a silicon atom gains enough energy to migrate to a position between planes of lattice atoms in which case the atom is known as a 'self-interstitial'. Similarly, an impurity atom which does not occupy a substitutional site is known as an 'interstitial'. In the past, elements which diffuse interstitially have been known as 'fast' diffusers and those which diffuse substitutionally via vacancies have been referred to as 'slow' diffusers. Research now indicates that elements from Groups III and V in the periodic table can migrate using a combination of both vacancy and interstitial mechanisms /131, 132/. This microscopic study of diffusion phenomena is important for the formulation of macroscopic diffusions laws suitable for incorporation into a process simulation program.

The diffusion coefficient or diffusivity D for crystals in general is a second rank tensor, but since the silicon lattice is cubic, D reduces to a scalar and the diffusion process is isotropic /133/. At concentration levels below the intrinsic carrier concentration n_i, the diffusivity D is a constant and diffusion is

described by Fick's law. However, at high concentration levels D becomes concentration-dependent. In addition, a fraction of the total dopant concentration becomes inactive and unable to participate in the diffusion process. The complexity of high concentration diffusion rules out an analytical analysis and instead, a numerical treatment is used.

Thermal oxidation of silicon often occurs simultaneously with high temperature diffusion, and gives rise to a flux of impurity species across the moving $Si-SiO_2$ interface, caused by a difference in chemical potential across the boundary. Segregation effects for boron in particular have important implications for MOS processes.

Diffusion of impurity species in silicon dioxide is modelled in SUPREM, but not in EPIC. The diffusivities of B, P and As in SiO_2 are much less than the diffusivities of these elements in Si /153/, and in the case of As at concentrations above 5×10^{20} cm^{-3} no diffusion occurs in a dry N_2 ambient /154/. An accurate model for segregation effects at the $Si-SiO_2$ interface includes diffusion within the oxide, however, for most practical purposes migration of dopants in the oxide can be neglected. An investigation of the validity of this assumption is postponed until chapter 8.

The above-mentioned effects are included in general diffusion models implemented in SUPREM and EPIC as detailed below.

cients is used extensively in the field of process modelling, and is therefore used as far as possible in the present work. Figure 4.5 shows an Arrhenius plot of the temperature dependence of the intrinsic diffusivity D for boron and arsenic according to SUPREM /97/. Figure 4.6 shows the temperature dependence of the intrinsic diffusivity D of P according to both SUPREM /97/ and Hill /137/. The data of Hill is obtained using a best fit to measurements of several authors, and appears to give better simulation results than the default SUPREM data for processing steps involving P which are carried out at the high temperature of 1200°C. This intrinsic diffusion data is summarised in table 4.2.

Element	$D_o (cm^2 s^{-1})$	$E_A (eV)$
B/97/	0.555	3.4265
P/97/	3.85	3.66
P/137/	0.6	3.51
As/97/	24.0	4.08

Table 4.2 : Intrinsic diffusion data for B, P and As

Figure 4.5 : Temperature Dependence of Diffusion Coefficients for B and As

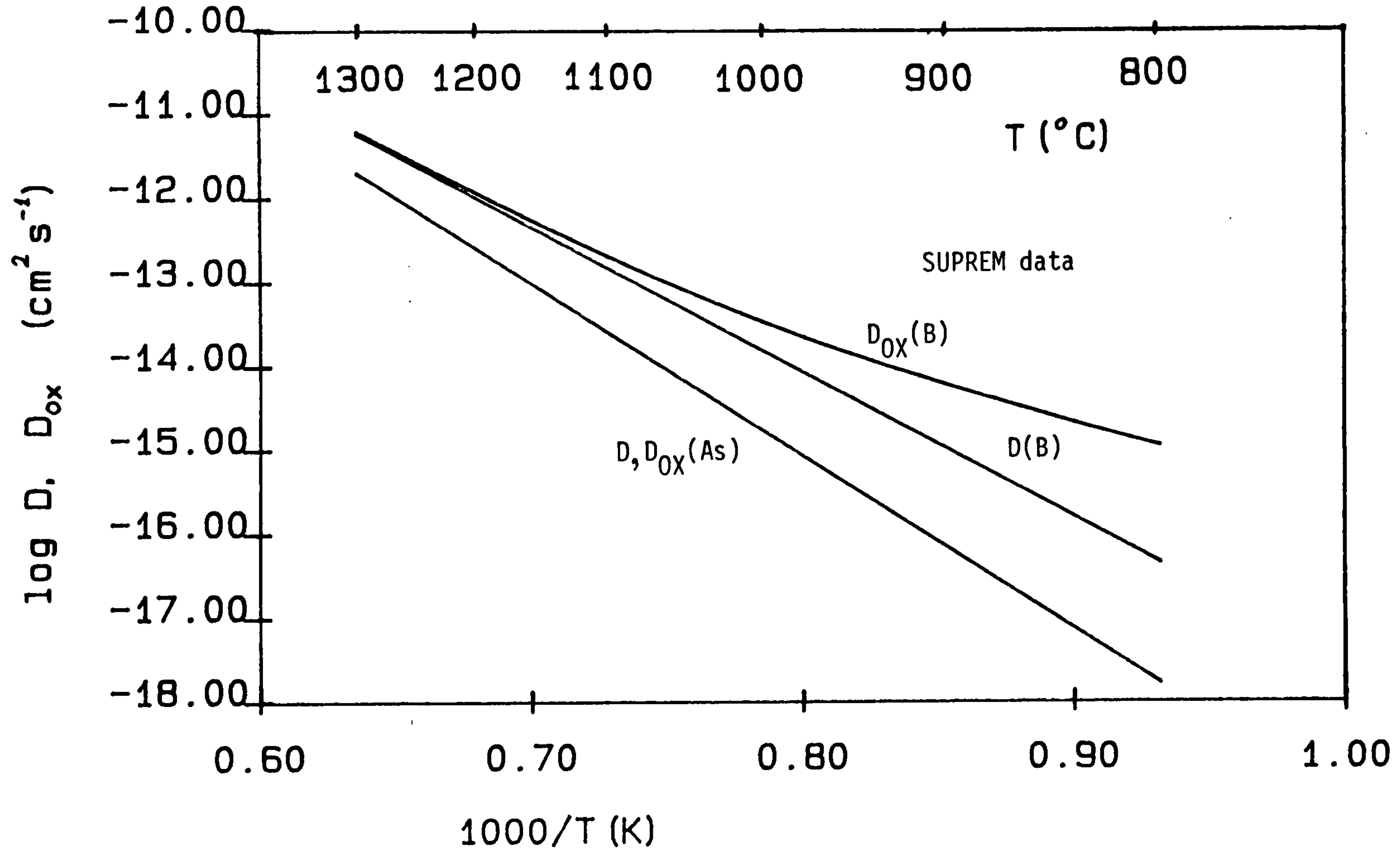
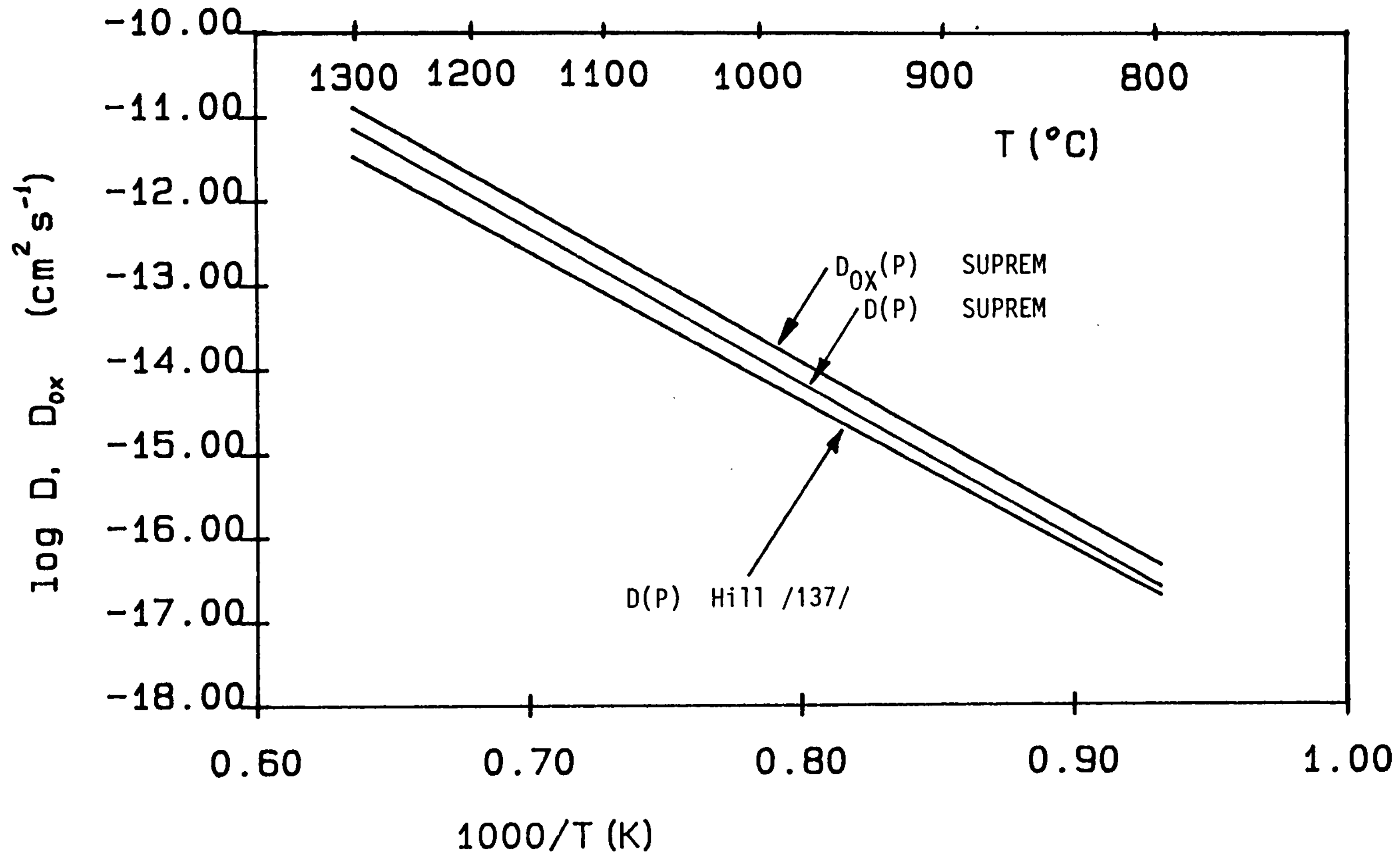


Figure 4.6 : Temperature Dependence of Diffusion Coefficient for P



4.3.3 Oxidation Enhanced Diffusion

Evidence of oxidation-enhanced diffusion (OED) of impurity species during thermal oxidation was first observed in high concentration profiles of boron /145/. This enhanced diffusion effect was subsequently found to bear a close relation to the formation of oxidation induced stacking faults /41/ which have a detrimental effect on MOS devices. Further research indicated that OED occurs for boron, phosphorus and arsenic /146-149, 152/, where boron is affected most, arsenic least and the behaviour of phosphorus lies between these extremes. The following explanation of these effects is due to Hu /41/.

Free silicon atoms are generated during thermal oxidation because of an incomplete chemical reaction at the Si-SiO_2 interface. Although the proportion of silicon atoms which do not participate in the reaction is only of the order of 1 in 10^3, these atoms may diffuse interstitially into the bulk of the silicon wafer. At non-planar regions of the Si - SiO_2 interface, such as at the bird's beak produced by LOCOS in MOS technologies, a regrowth process exists for excess self-interstitials which form stacking faults in the silicon. Non-equilibrium interstitial silicon atoms also increase the diffusion of boron which diffuses via a dual mechanism involving both interstitials and vacancies. Phosphorus is affected in the same way but to a lesser extent, and the migration of arsenic is only slightly influenced since this atom diffuses primarily by the

vacancy mechanism.

In a process simulation program, oxidation-enhanced diffusion can be modelled by adding a factor ΔD_{ox} to the intrinsic diffusivity D to obtain a modified diffusion coefficient D_{ox} where

$$D_{ox} = D + \Delta D_{ox} \tag{4.21}$$

Hill /137/ presents the model

$$\Delta D_{ox} = F \exp\left(-\frac{E_o}{k_B T}\right) \tag{4.22}$$

where the pre-exponential constant F and activation energy E_o are determined empirically. This is the model which is implemented in SUPREM and EPIC. Lin et al /135/ use the model

$$\Delta D_{ox} = F \left(\frac{dX_o}{dt}\right)^n \tag{4.23}$$

where F and n are empirically determined constants.

Taniguchi et al /147/ use a synthesis of these two models with the addition of an exponentially decaying term in distance which models the capture of self-interstitials by lattice vacancies in the bulk. In this formulation

$$\Delta D_{ox} = F \left(\frac{dX_o}{dt}\right)^n \exp\left(-\frac{x}{L_D}\right) \exp\left(-\frac{E_o}{k_B T}\right) \tag{4.24}$$

where L_D = 25 micron and represents the characteristic diffusion length of self-interstitials into the bulk.

Both (4.23) and (4.24) are functions of the oxide growth rate which in turn depends on the furnace ambient, temperature and pressure.

It has been observed that oxidation-enhanced diffusion of impurity species is not isotropic. Experiments have indicated that the vertical diffusion length of self-interstitials generated during oxidation is about 25 microns, but the lateral diffusion length is only 2 microns /151/. MOS transistors with channel widths of a few microns are now being fabricated in the production environment, but it is uncertain to what extent this lateral OED effect influences device characteristics. The 2-D analysis for silicon self-interstitials of Hamasaki /32/ predicts too large a lateral effect. This work is improved by Shin and Kim /75/ who have added an annihilation model for excess self-interstitials at the Si-SiO_2 interface to explain the experimental observations of Lin et al /151/. However a model to accommodate the moving non-planar Si-SiO_2 interface during formation of the bird's beak has not yet been formulated.

The OED parameters used by SUPREM and EPIC according to Hill's model through equations (4.21) and (4.22) are summarised in table 4.3 and are plotted in figures 4.5 and 4.6. This model considers simply the presence, and not the partial pressure of oxidis-

ing ambient in the furnace tube, and OED effects for arsenic are assumed to be negligible.

Element	F (cm^2s^{-1})	E_o (eV)
B	9.17×10^{-8}	1.69
P	3.08	3.66
As	0	4.08

Table 4.3 : OED data /97/ to be used in equation (4.22)

4.3.4 Segregation

During thermal oxidation, a redistribution of dopant species occurs on each side of the $Si-SiO_2$ interface until the chemical potential of the dopants are the same on each side of the interface /155, 156/. The equilibrium segregation coefficient k is defined by

$$k = \frac{N_{ox}}{N} \bigg| \quad Si - SiO_2 \text{ interface} \tag{4.25}$$

where N_{ox} and N are the impurity concentration levels on the oxide and silicon sides of the interface respectively. The redistribution arising from segregation effects depends on the diffusivities in the silicon and the oxide, and also the oxide growth rate /155/. It is very important to model segregation effects in MOS technology because device performance is sensitive to changes in impurity concentration at the silicon surface.

Boron tends to be sucked from the silicon surface during thermal oxidation, while phosphorus and arsenic pile up in the silicon. The segregation coefficient of boron is a function of crystal orientation /157/, ambient composition /158/, and temperature according to

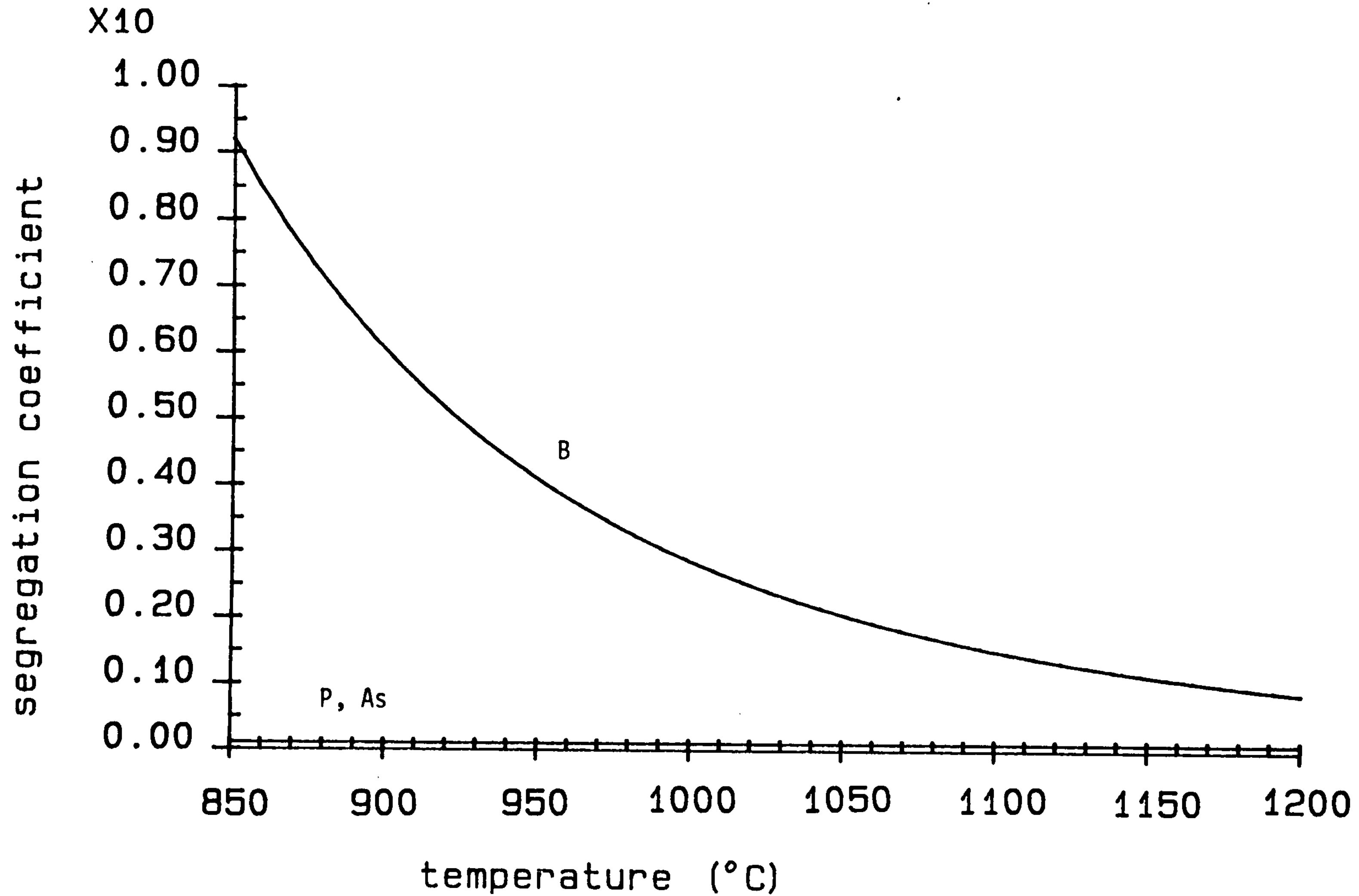
$$k = k_0 \exp(-\frac{E_k}{k_B T}) \tag{4.26}$$

Values of $k_0 = 4.52 \times 10^{-4}$ and $E_k = 0.96$ eV give good results for (100) silicon in either dry or wet oxidising conditions /11, 97/. For phosphorus and arsenic the segregation coefficient is assumed to be independent of temperature and takes a value of $k = 0.1$ /11,97/. Figure 4.7 indicates the temperature dependence of k for all three elements. This data for segregation is also implemented in EPIC.

Impurity redistribution during thermal oxidation coupled with the impurity flux due to segregation at the moving $Si\text{-}SiO_2$ interface is a complex problem to solve. Av-Ron et al /159/ describe an analytical treatment which allows simulation of the impurity redistribution occurring during the oxidation of a uniformly doped wafer. However, this method is not applicable in most practical situations in MOS technology since impurity profiles are non-uniform. Huang and Welliver /160/ approximate the one-dimensional profile after thermal oxidation by adding an empirical correction factor to the profile generated assuming inert drive-in conditions. Modifications of this work are detailed by Lee et al /162/, but the accuracy of this analysis is uncertain in general situations.

The only reliable way of modelling impurity diffusion and segregation is to use a numerical treatment. The work of Antoniadis et al /161/ forms the basis for SUPREM /11,97/ which uses the finite difference method. EPIC also uses the finite difference method but extends the simulation capability to two-dimensions.

Figure 4.7 : Segregation Coefficients for B, P and As



In order to ascertain the accuracy of the oxidation, diffusion and segregation models already described it is necessary to compare SUPREM simulation results with experimentally determined impurity profiles.

4.3.5 Measurement of Doping Profiles by the Deep Depletion C-V Method

The use of differential capacitance-voltage (C-V) measurements to determine impurity doping profiles in semiconductors is well established. This technique can be applied to a metallic Schottky barrier diode or an abrupt p-n junction where the impurity concentration is very high on one side of the junction and low on the other side /163-166/. The same analysis can also be used for the MOS capacitor /169/, in which case the experimentally measured profile provides a check on the accuracy of 1-D process models.

In the method, the MOS capacitor is biased into depletion and the depletion-layer approximation /168/ is assumed to hold. This is equivalent to the assumption of a vanishingly small Debye screening length at the depletion edge. In the notation to follow, capacitance is denoted C(V) to avoid confusion with chemical concentration of dopant C. By pulsing the silicon into depletion and taking a capacitance measurement in a total time less than the minority carrier generation time, no inversion region forms at the silicon surface. The doping concentration N at the depletion edge is given

by /169/

$$N(w) = 2 \left[q \, \varepsilon_s \left| \frac{d}{dV} \left\{ \frac{1}{C^2(V)} \right\} \right| \right]^{-1} \tag{4.27}$$

where the depletion layer width w is calculated from

$$w = \varepsilon_s \left\{ \frac{1}{C(V)} - \frac{1}{C_{ox}} \right\} \tag{4.28}$$

In these equations, V is bias voltage, q is the electronic charge and ε_s is the permittivity of silicon.

Expression (4.27) is only valid where the impurity profile does not vary appreciably over a distance of a few extrinsic Debye lengths /168/, where one extrinsic Debye length L_D is defined by

$$L_D = \sqrt{\frac{k_B T \varepsilon_s}{q^2 N}} \tag{4.29}$$

and T is absolute temperature.

Measurement of rapidly varying profiles characteristic of implanted ions /167/ requires a correction procedure to achieve accurate results /170, 172/.

The minority carrier lifetime is important for MOS dynamic

random-access memory technology since it affects cell refresh time /174/. This parameter can be measured simultaneously with the doping profile using a double sweep technique /173/. As in the present work, the top electrode of the capacitor is usually formed by deposition of aluminium or doped polysilicon, however this extra processing step is not required if a mercury probe is contacted directly with the capacitor dielectric /171/.

In the present work, capacitance readings are taken and subsequently processed numerically using the Hewlett-Packard 4061 Automatic Data Acquisition System. The silicon is repeatedly pulsed from a voltage V_{acc} in accumulation to a measurement voltage V, after which a 'settle-in' time ensures steady state conditions before the capacitance measurement is taken, as in figure 4.8. Differential capacitance methods are sensitive to noise and the doping profile is calculated from an average over five voltage scans. Figures 4.9-4.11 show experimental results for the active regions of three PMOS transistors each having a different level of n-type doping. Also shown are SUPREM simulation results using both the default SUPREM model and the model due to Hill for diffusion of phosphorus as shown in table 4.2. The doping level in the n-substrate region is predominantly due to the furnace conditions of the p-well drive-in step performed at 1200°C and lasting 725 mins. Use of Hill's diffusion data /137/ for phosphorus at this temperature results in good agreement between simulation results and the experimental profile at the surface of the silicon. The agreement is not so good into the silicon bulk, since the measurements are af-

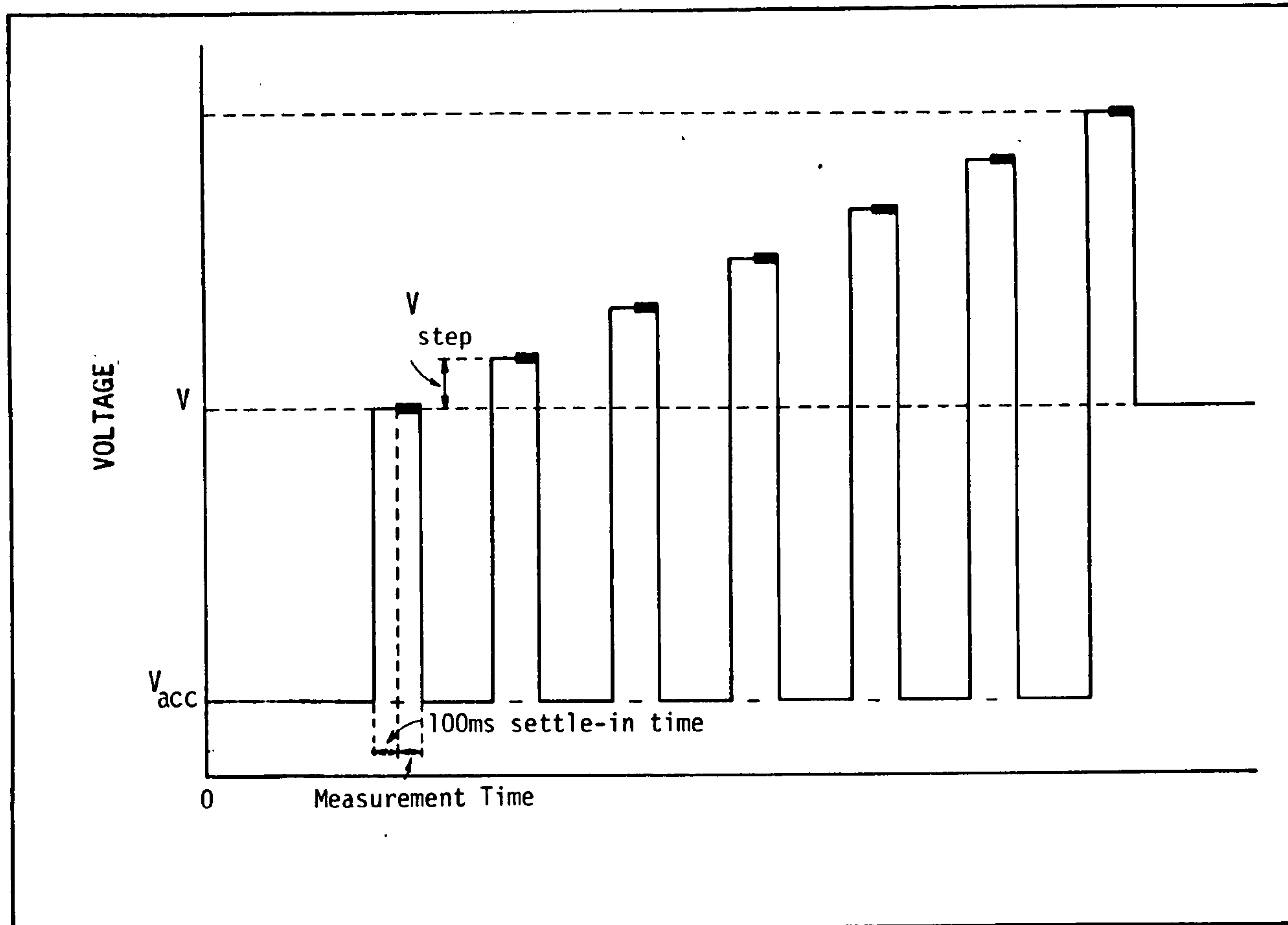


Figure 4.8 : Timing diagram for deep depletion C-V measurements.

Figure 4.9 :Comparison of SUPREM and Deep Depletion CV Results

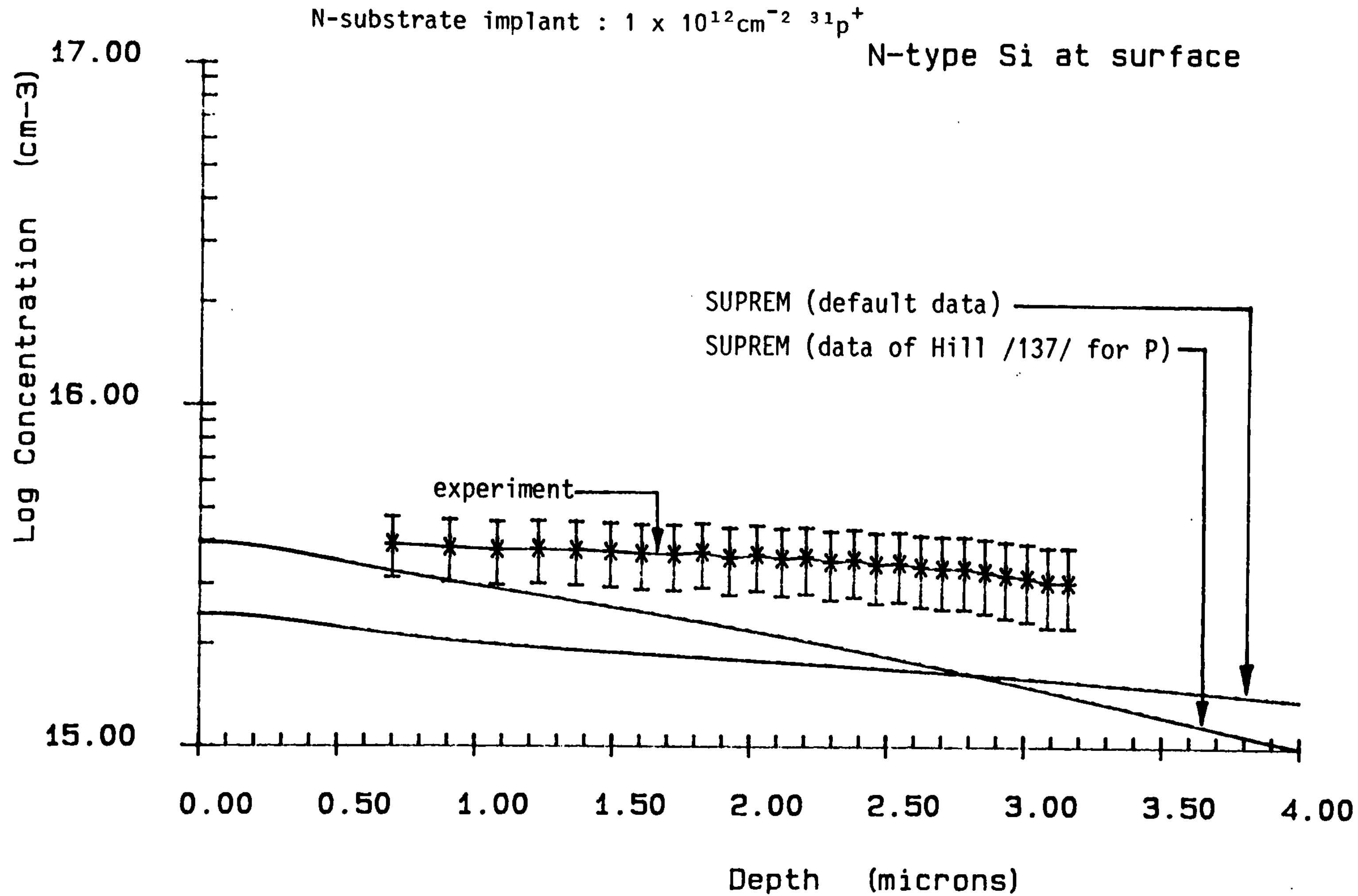


Figure 4.10 : **Comparison of SUPREM and Deep Depletion CV Results**

N-substrate implant : $2 \times 10^{12} cm^{-2}$ $^{31}P^{+}$

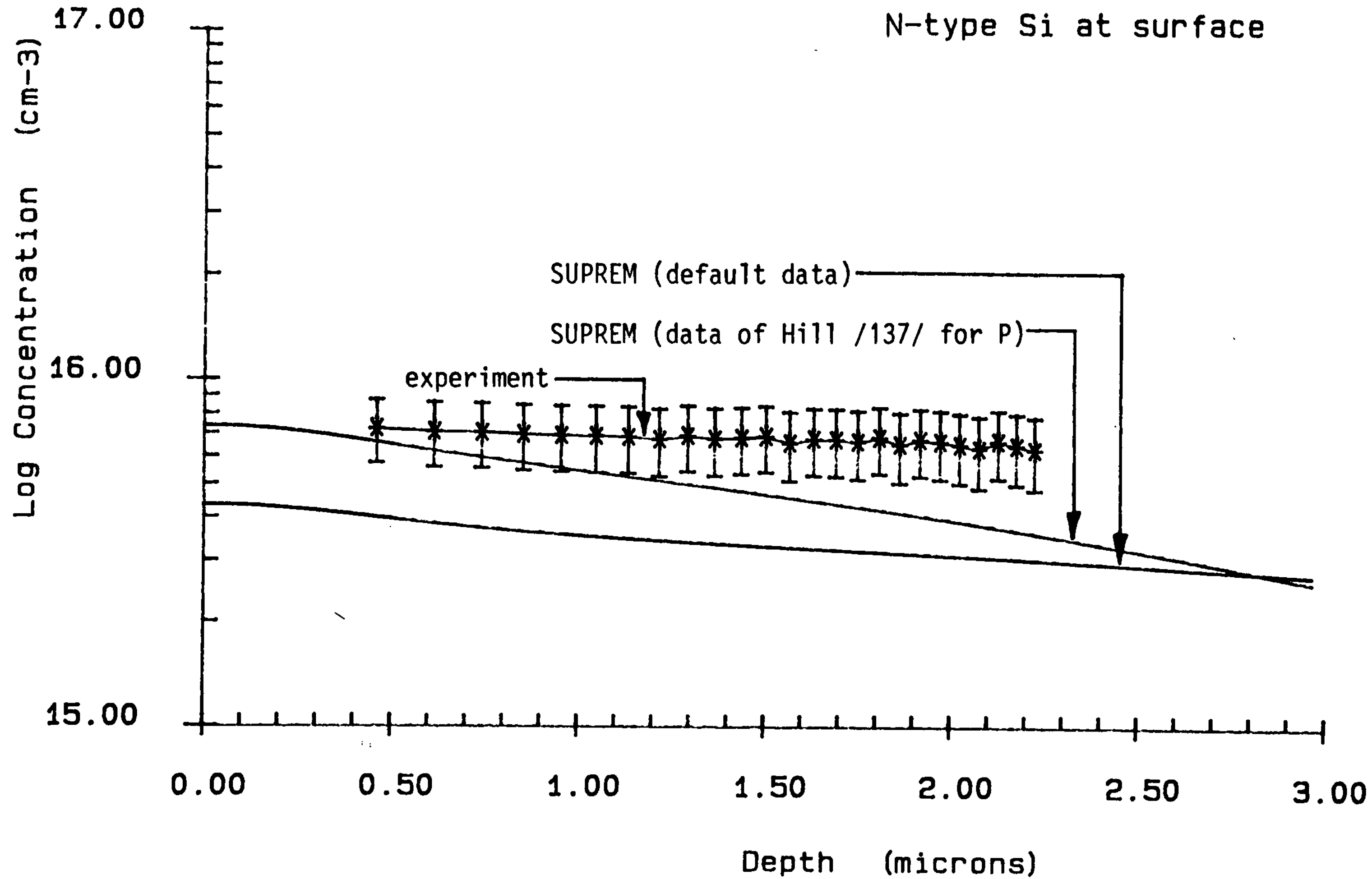
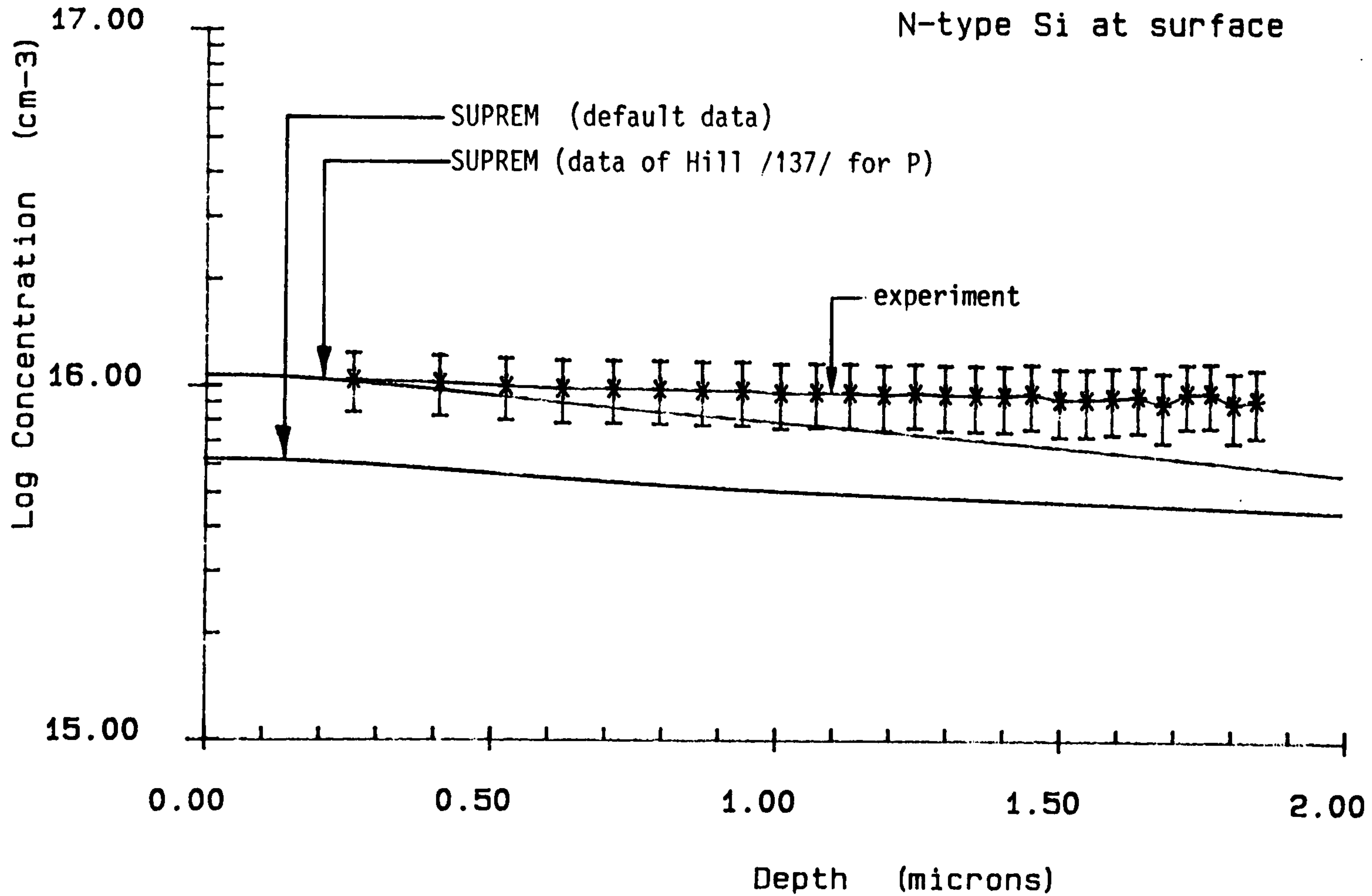


Figure 4.11 : **Comparison of SUPREM and Deep Depletion CV Results**

N-substrate implant : 3×10^{12} cm^{-2} $^{31}P^{+}$



fected by stray capacitances and MOS chip capacitances which are not part of the gate oxide region. Figures 4.12 and 4.13 show the corresponding results for the active regions of two NMOS transistors fabricated in wafers with a different level of p-well doping, but the same n-type phosphorus profile. Again, Hill's diffusion data for phosphorus appears to be more accurate than the data used by SUPREM, and is therefore used for diffusion at temperatures greater than or equal to 1200°C in all subsequent simulation examples.

4.3.6 High Concentration Diffusion

Fick's law of diffusion is only accurate for low impurity concentrations in silicon i.e. $n \ll n_i$. The high concentration levels typical of source/drain diffused regions in MOS wafers require a generalisation of this basic model. A non-uniform doping profile gives rise to an internal electric field which enhances ion diffusion /175/. An additional increase in diffusion is caused by interaction of impurity ions with interstitials and vacancies which can accept or lose electrons to become electrically charged /176/. The concentration of these point defects in a given charge state can be determined from statistical thermodynamics /130, 177/. A diffusivity for each charge state can be calculated, but for most practical purposes it is necessary to consider interaction of impurities with only neutral and singly-charged point defects /11,97/.

It can be shown /27/ that the transport equation for one im-

Figure 4.12 : **Comparison of SUPREM and Deep Depletion CV Results**

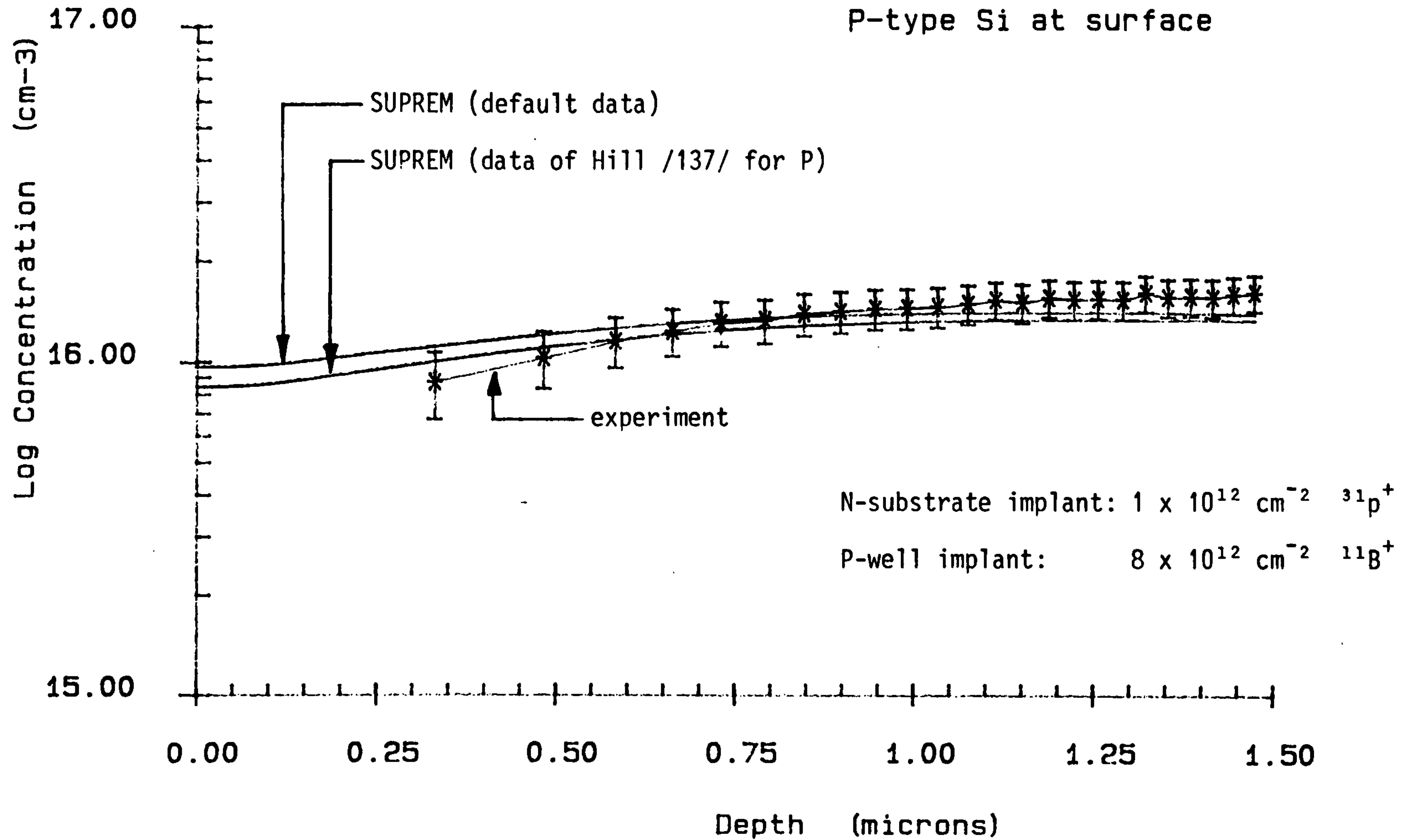
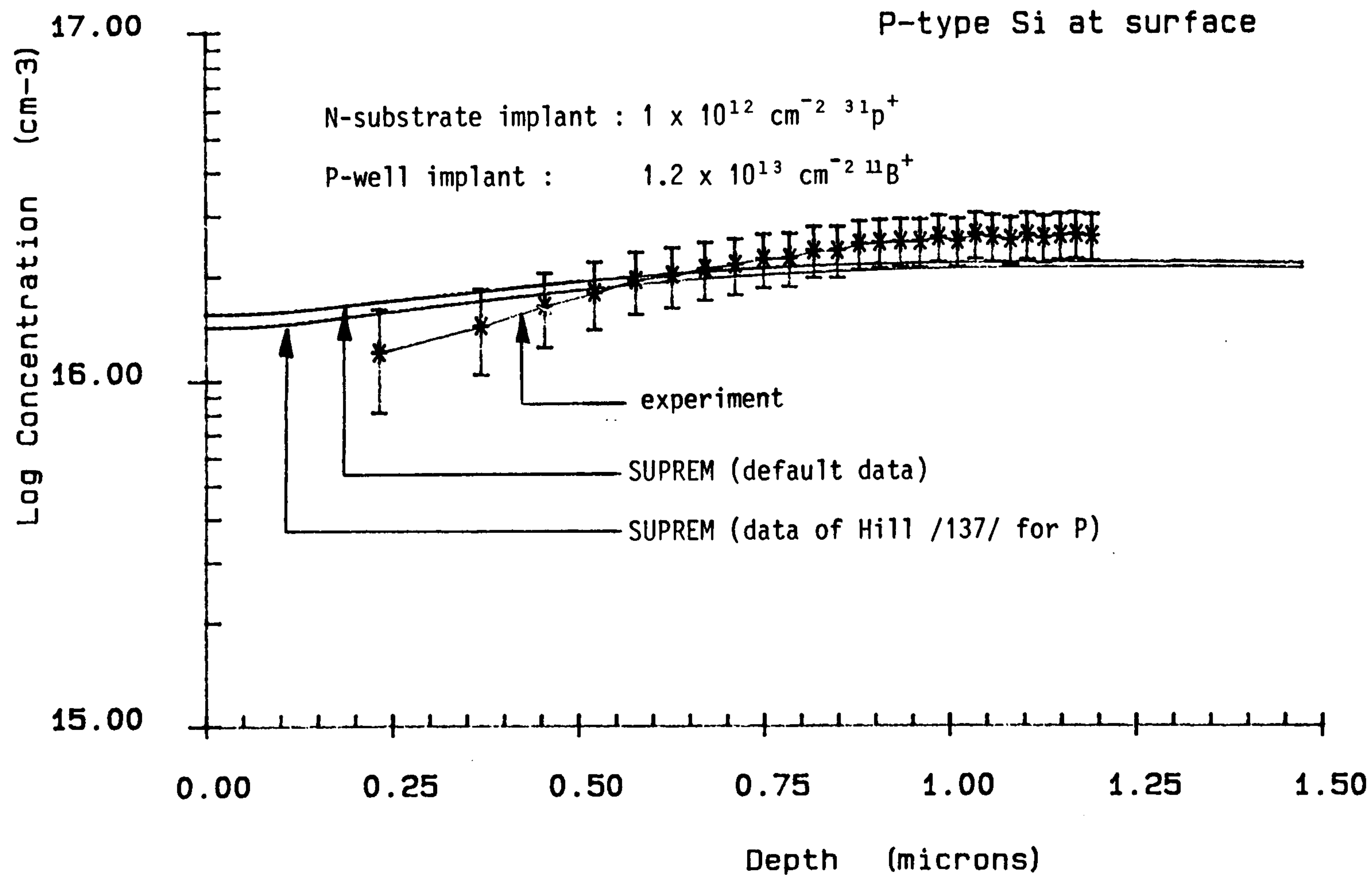


Figure 4.13 : **Comparison of SUPREM and Deep Depletion CV Results**



purity species can be written as

$$\frac{\partial C}{\partial t} = \nabla.(D^{*}\nabla N) \tag{4.30}$$

where the active or mobile impurity concentration N is some fraction of the total or chemical concentration C. The effective diffusion coefficient D^{*} is given by

$$D^{*} = h_V h_F D \tag{4.31}$$

where the point defect enhancement factor h_V is given by

$$h_V = \begin{cases} \dfrac{(1 + \delta \frac{n}{n_i})}{(1 + \delta)} & ; \quad \text{donors} \\[2ex] \dfrac{(1 + \delta \frac{n_i}{n})}{(1 + \delta)} & ; \quad \text{acceptors} \end{cases} \tag{4.32}$$

and the electric field enhancement factor h_F is given by

$$h_F = 1 + \frac{N}{2n_i} \{1 + (\frac{N}{2n_i})^2 \}^{-\frac{1}{2}} \tag{4.33}$$

The constant δ in (4.32) is the ratio of the diffusivity of impurities via singly-charged point defects to that via neutral point defects. This parameter is chosen empirically and is different for each element, as summarised in table 4.4.

Element	δ
B	3
P	1
As	100

Table 4.4 : Values of point defect enhancement parameter δ for B, P and As/11,97/.

Hu and Schmidt /178/ were the first to consider the coupled diffusion of two species, boron and arsenic, at high concentration levels in the fabrication of a bipolar transistor. Their assumption of quasi-neutrality everywhere in the wafer is not justified because of the existence of a p-n junction. A correct treatment of this problem should involve the simultaneous solution of a transport equation for each impurity species, and Poisson's equation for potential/179/. However, several authors /18, 29, 180, 181/ tacitly assume quasi-neutrality in coupled diffusion problems with apparently good agreement between simulation results and experiment. This erroneous idea is not implemented in EPIC or ROMANS II, the program of Maldonado et al /20-22/.

SUPREM II /8, 97/ uses the transport equation

$$\frac{\partial C}{\partial t} = \nabla^2 (D^* N) \tag{4.34}$$

which only reduces to (4.30) if the term ∇D^* is negligible. This form may not be accurate in certain cases but the revised version of the program SUPREM III /181/ is reported to use the correct equation (4.30).

Any model of high concentration diffusion requires an expression for the intrinsic carrier concentration n_i. SUPREM uses the expression of Morin and Maita /183/ given by

$$n_i^2 = np = CT^3 \exp(-\frac{E_G}{k_B T}) \tag{4.35}$$

where C is a constant and E_G is the minimum difference in energy between the conduction and valence bands in silicon. However theory and measurements have established that the bandgap and therefore intrinsic number are functions of temperature and high concentration levels /184/, but no reliable data is available for temperatures greater than 450^oC. Although optical absorption measurements suggest a value of E_G = 1.21 eV /184/, electrical measurements of semiconductor devices at room temperature (300K) suggest a value of E_G = 1.12 eV and $n_i = 1.45 \times 10^{10}$ cm^{-3} /13/. In EPIC, to be consistent with room temperature conditions, equation (4.35) is used with E_G = 1.12eV and $C = 5.10 \times 10^{31}$ cm^{-6} K^{-3}, at all temperatures and doping levels.

High concentration levels result in immobile clusters of dopants which do not participate in the diffusion process. Because the concentration gradient of mobile atoms is small, the field enhancement of diffusion is reduced. The details of the physical mechanisms responsible for inactive dopants are as yet uncertain, but it is believed that at high concentrations the dopant either precipitates or forms a compound with silicon /81/.

A simple model for immobile complexes assumes that all atoms are active up to a certain critical concentration value N_m, the solid solubility limit, beyond which all additional atoms form part of a cluster. Figures 4.14 and 4.15 show the temperature dependence of the solid solubility of B /182/, P /187/ and As /182/ as used by

Figure 4.14 : Solid Solubility of B

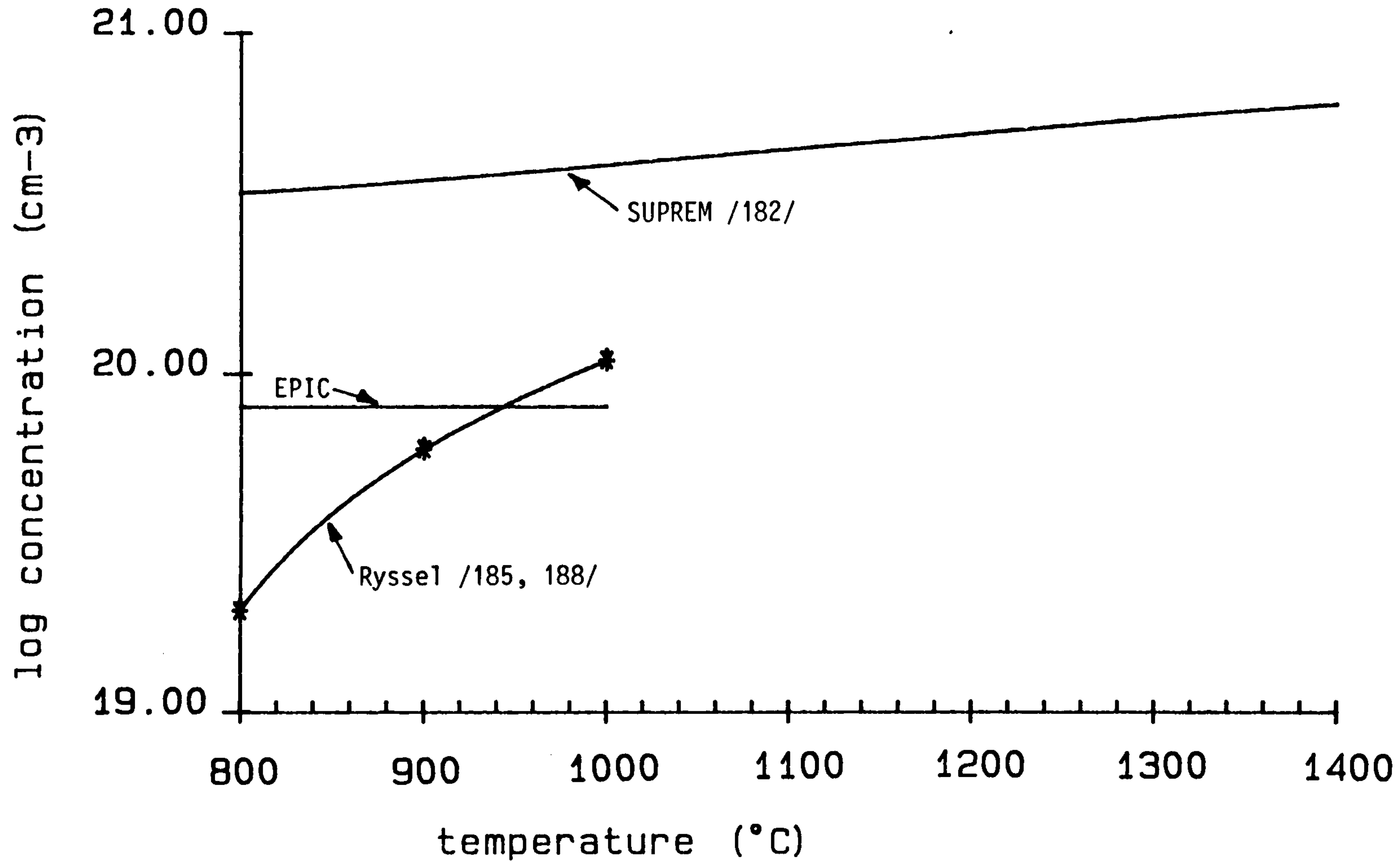


Figure 4.15 : Solid Solubility Limits of P and As

SUPREM model

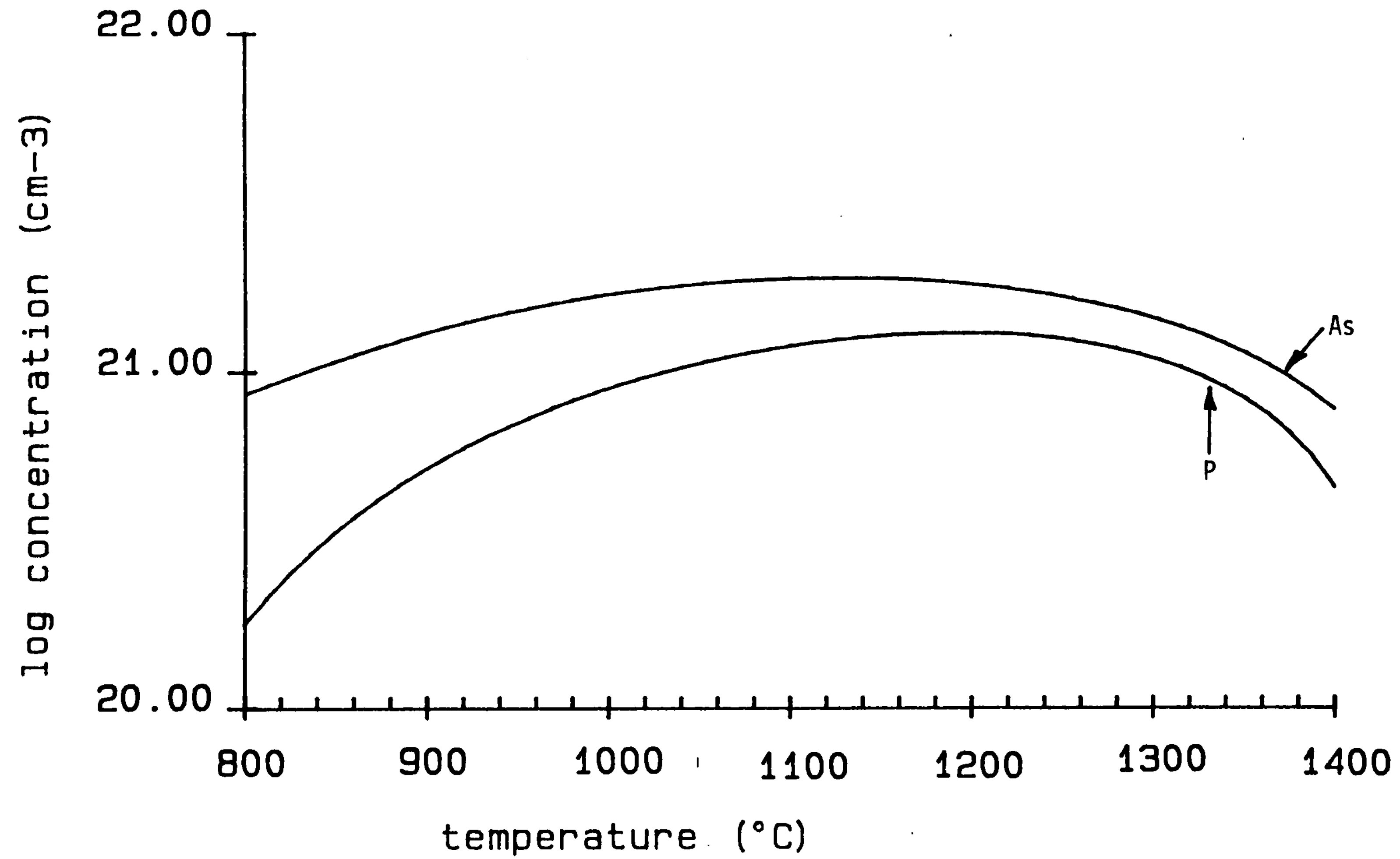
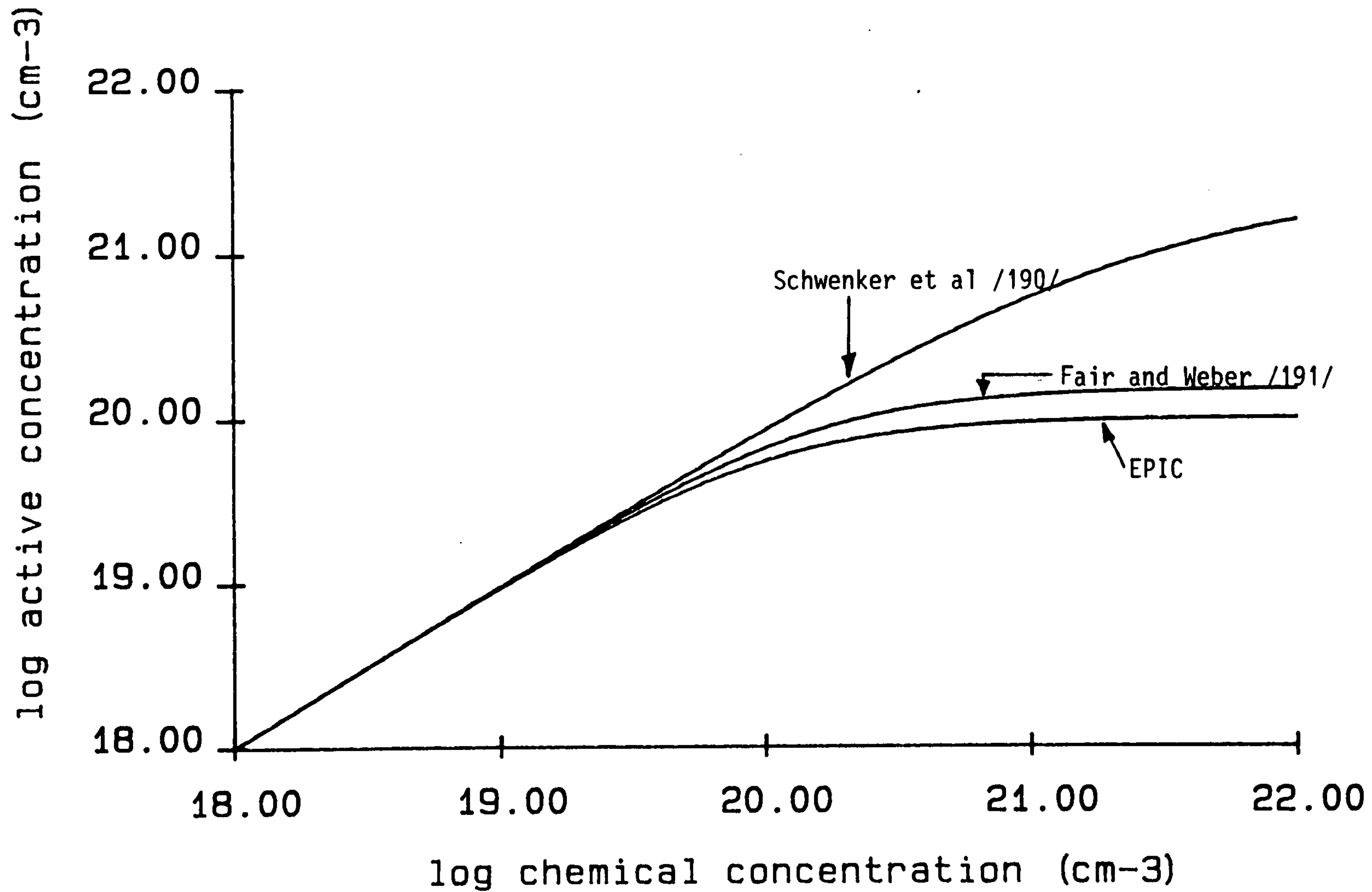


Figure 4.16 : Clustering Models for As at 1000°C



SUPREM. Research by Ryssel et al /185, 188/ indicates that the solubility limit for B is much lower than originally thought and figure 4.14 shows a quadratic polynomial fit to data presented for the temperatures of 800°C, 900°C and 1000°C.

As a test for the high concentration diffusion models, the implanted profiles of figures 4.2, 4.3 and 4.4 were subjected to a typical source/drain anneal treatment. After loading the furnace tube at 900°C, the wafers are ramped linearly with time to a temperature of 1000°C over a period of 14 mins. and then maintained at 1000°C for 30 mins. Figures 4.17, 4.18 and 4.19 show the SIMS data for each diffused implant. Figure 4.17 shows the simulation results of SUPREM and also those of EPIC using the solid solubility model of Ryssel et al. The immobile peak shown by the SIMS results is not predicted by either of these models, indicating that clustering effects must occur at lower concentration levels. A better fit to the experimental data is obtained by using in EPIC a solubility limit of 8×10^{19} cm^{-3} as shown in figure 4.14 and also multiplying the diffusion coefficient by a factor of 0.8. From figure 4.18, the inactive boron is modelled at least qualitatively, and the extent of the distribution tail should allow a reasonable estimation of source/drain junction depth in the PMOS transistor.

Diffusion of phosphorus in silicon is complex and not clearly understood /189/. The implementation of the phenomenological model due to Fair and Tsai /140/ in SUPREM is discussed in detail by An-

Figure 4.17 : BORON SOURCE/DRAIN IMPLANT ANNEALED

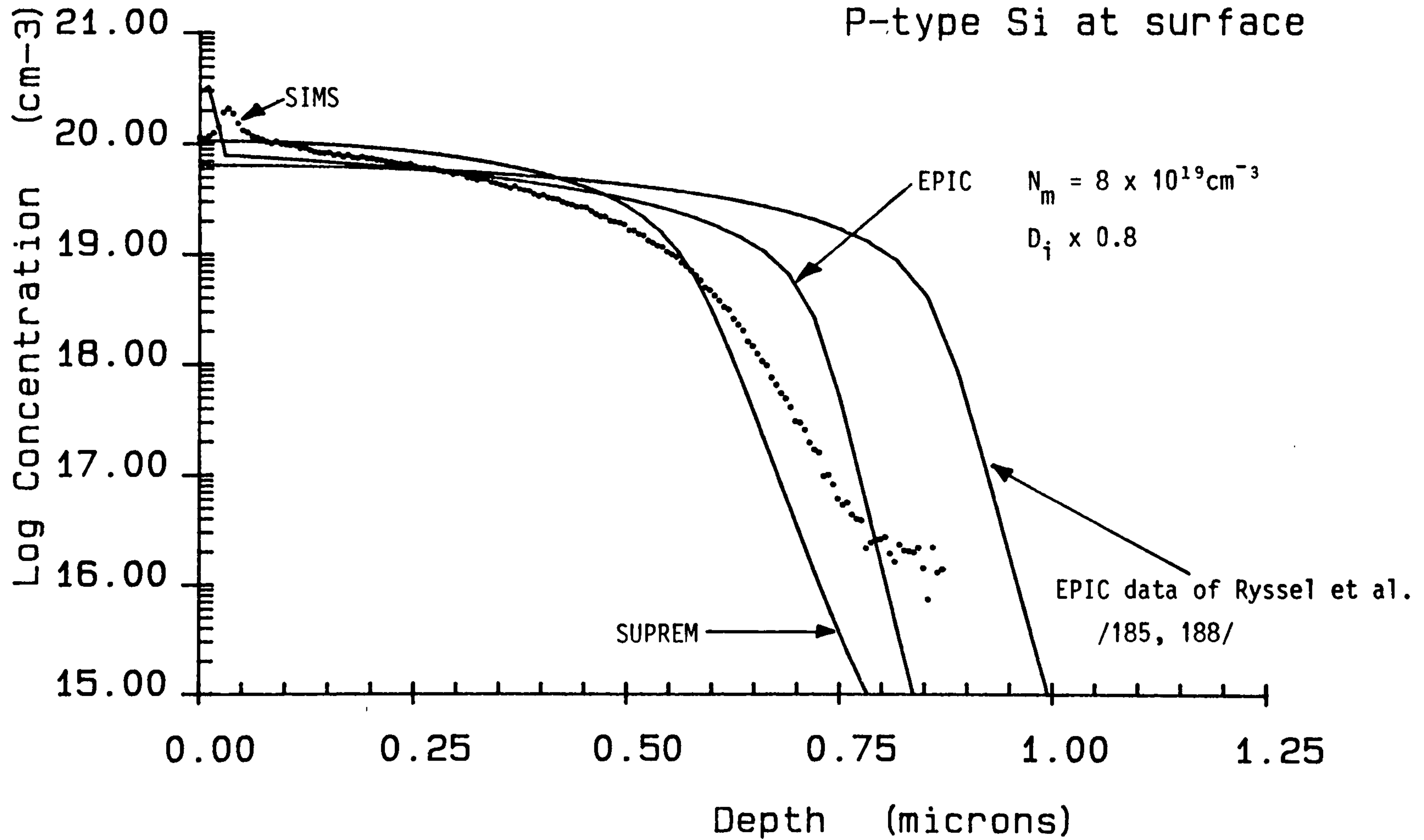


Figure 4.18 : PHOSPHORUS SOURCE/DRAIN IMPLANT ANNEALED

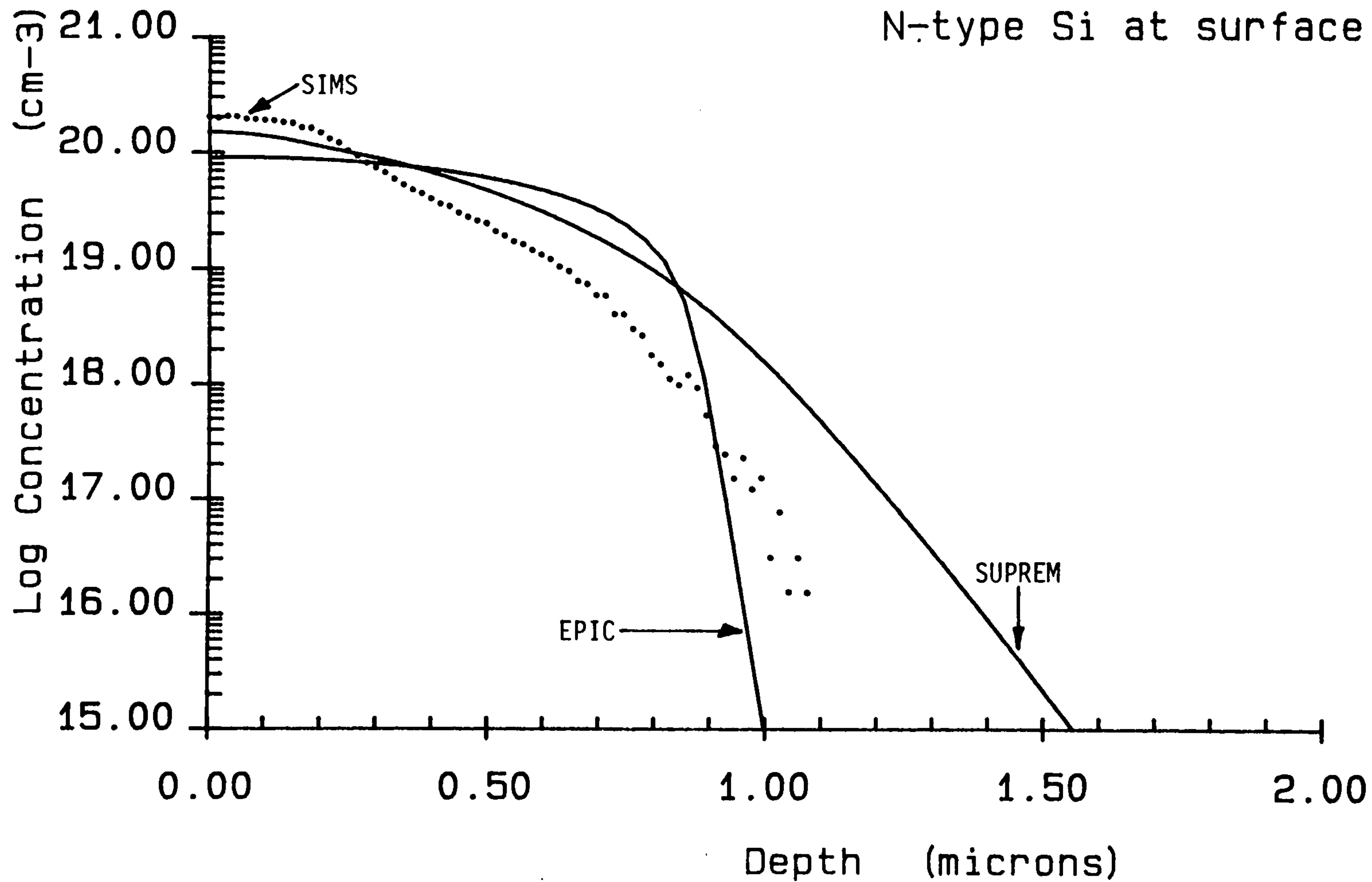
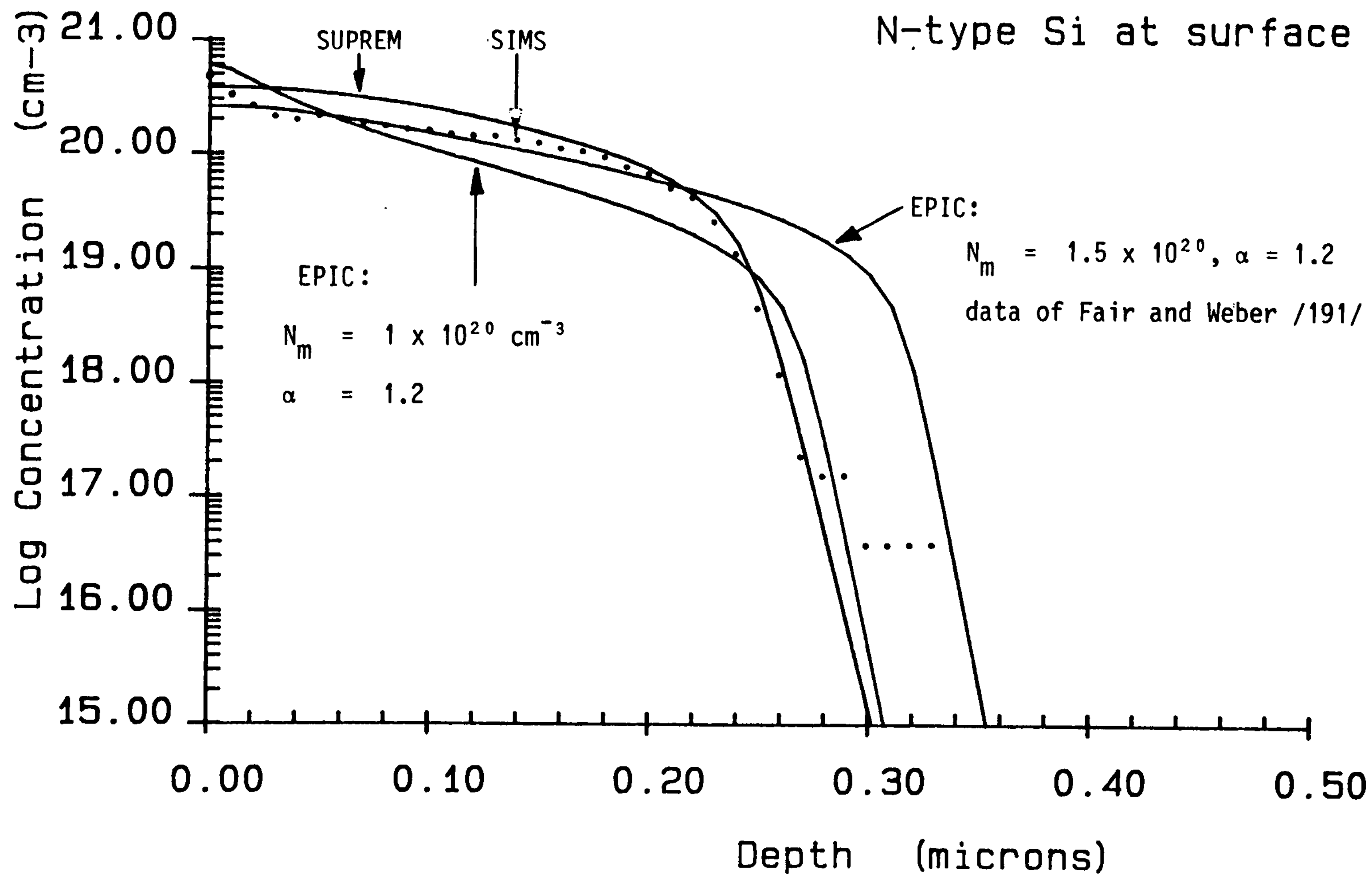


Figure 4.19 : ARSENIC SOURCE/DRAIN IMPLANT ANNEALED



toniadis and Dutton /11/ and so is not reiterated here. Figure 4.18 shows a comparison of SUPREM and EPIC simulation results with experimental data. Use of the more complicated diffusion model by SUPREM does not seem justified, and is therefore not implemented in EPIC. EPIC is likely to predict junction depths in phosphorus source/drain regions more accurately than SUPREM.

A more sophisticated model has been developed for the clustering of arsenic. For most practical processing situations, diffusion temperatures are greater than 900°C and anneal times are longer than 20 min, in which case dynamic clustering and declustering of dopants is not significant /185, 186/. At equilibrium, the total impurity concentration C is the sum of atoms on substitutional sites N and atoms in clusters to give

$$C = N + \bar{m} \; C^{*} \left(\frac{N}{C^{*}}\right)^{\bar{m}} \tag{4.36}$$

where $\bar{m}$ is the number of atoms in the cluster and C^{*} characterises the concentration value where significant clustering starts /81/. Equation (4.36) is sometimes written in the form

$$C = N + \bar{m} \; k_{eq} \, N^{\bar{m}} \tag{4.37}$$

where k_{eq}, the equilibrium clustering coefficient, is given by

$$k_{eq} = (C^{*})^{1-\bar{m}} \tag{4.38}$$

Since the clustering relation (4.37) is difficult to implement numerically, Tielert /94/ uses an empirical fit to this form through the expression

$$N = C \left[1 + \left(\frac{C}{N_m}\right)^{\alpha}\right]^{-\frac{1}{\alpha}} \tag{4.39}$$

where α is an empirically-determined parameter. Using this approach, figure 4.16 shows a fit to the data of Schwenker et al /190/ with $N_m = 2.5 \times 10^{21}$ cm^{-3} and $\alpha = 0.7$. Also shown is a fit to the data of Fair and Weber /191/ where $N_m = 1.5 \times 10^{20}$ cm^{-3} and $\alpha = 1.2$. Tielert claims that the results of Schwenker et al should be used for diffusion simulation in preference to the data of Fair and Weber since Schwenker et al quenched their wafers quickly enough after the furnace treatment for the state of clustering not to change.

It is clear from the SIMS results of figure 4.19 that an inactive portion of arsenic atoms exists at the silicon surface, and so clustering begins at a concentration level much lower than that claimed by Schwenker et al. Figure 4.19 shows EPIC simulation results using the data of Fair and Weber. Further reduction of the solubility limit to $N_m = 1 \times 10^{20}$ cm^{-3} gives a better fit to experiment, and is the value used for all simulations of arsenic in EPIC.

It has been suggested that arsenic clusters, despite being immobile at high temperature, are electrically charged /186, 192/,

in which case the free electron concentration is changed. Clusters are assumed to have zero net charge in EPIC.

The comparisons of experimental SIMS data with simulation results indicate that physical models for high concentration diffusion require to be refined, particularly for short anneal times. However, the models in EPIC give a reasonable estimate of the extent of the diffused profiles in the vertical direction in the wafer.

4.3.7 Diffusion in Polysilicon

The doping of polysilicon is important for MOS technologies since this material is used for the gate electrode. A high but uniform doping level is required in this layer to ensure a low sheet resistance and therefore low RC time delays in circuits. Dopant atoms are introduced into polysilicon by diffusion from a doped oxide source, from a chemical source or by ion implantation.

The diffusivity in a polysilicon film depends on the grain structure, which in turn depends on the deposition temperature, rate of deposition and thickness of film /193/. The diffusivity of impurities along grain boundaries is observed to be enhanced by a factor of about 100 compared to that in a single crystal. Arsenic and phosphorus segregate in grain boundaries while boron does not /194/. The furnace doping of polysilicon does not introduce any impurities

into the silicon of the substrate, and so can be treated as an inert anneal step by EPIC.

4.4 MATERIAL DEPOSITION AND ETCHING

Epitaxial growth is now becoming important for VLSI CMOS technology since this processing technique offers a means to guard against latch-up. Near-intrinsic silicon is grown on a heavily doped substrate, and thereafter process steps are similar to conventional bulk CMOS. Impurity redistribution occurring during epitaxial growth is modelled by SUPREM II /11,97/ and to an improved level in SUPREM III /181/.

Modelling of epitaxial growth is not required for the p-well CMOS process under study in this thesis, however this subject is discussed, for example, by Reif et al /195, 196/.

Other processing steps such as chemical vapour deposition (CVD) /197/ of phosphosilicate glass (PSG), silicon nitride and polysilicon, and deposition of aluminium using electron-beam evaporation or sputtering are all low temperature processes and give rise to no impurity distribution.

Material removal by wet chemical or plasma etching is also carried out at low temperature. Changes in boundary position caused

by etching are relatively easily accommodated by both 1-D and 2-D simulators.

4.5 1-D SUPREM SIMULATION OF A P-WELL CMOS PROCESS

Using the process models already described, the SUPREM simulation program can be used to generate the 1-D impurity profiles for each of the six important cross sections in the p-well CMOS process /5/ as shown by figure 4.20. These cross-sections are only representative of the true doping profile in regions where complete symmetry in the lateral direction can be assumed. Outwith these regions, a 2-D simulation effort is required to accommodate lateral variations in wafer structure. Figures 4.20 to 4.25 show the 1-D doping profiles in each region at the end of the CMOS process flow described in chapter 2, using the process parameters of table 4.5. The temperature ramps used in the furnace treatments are included in this simulation example, but these are omitted from table 4.5 for reasons of brevity. Details of photolithographic stages are also not included in the process flow.

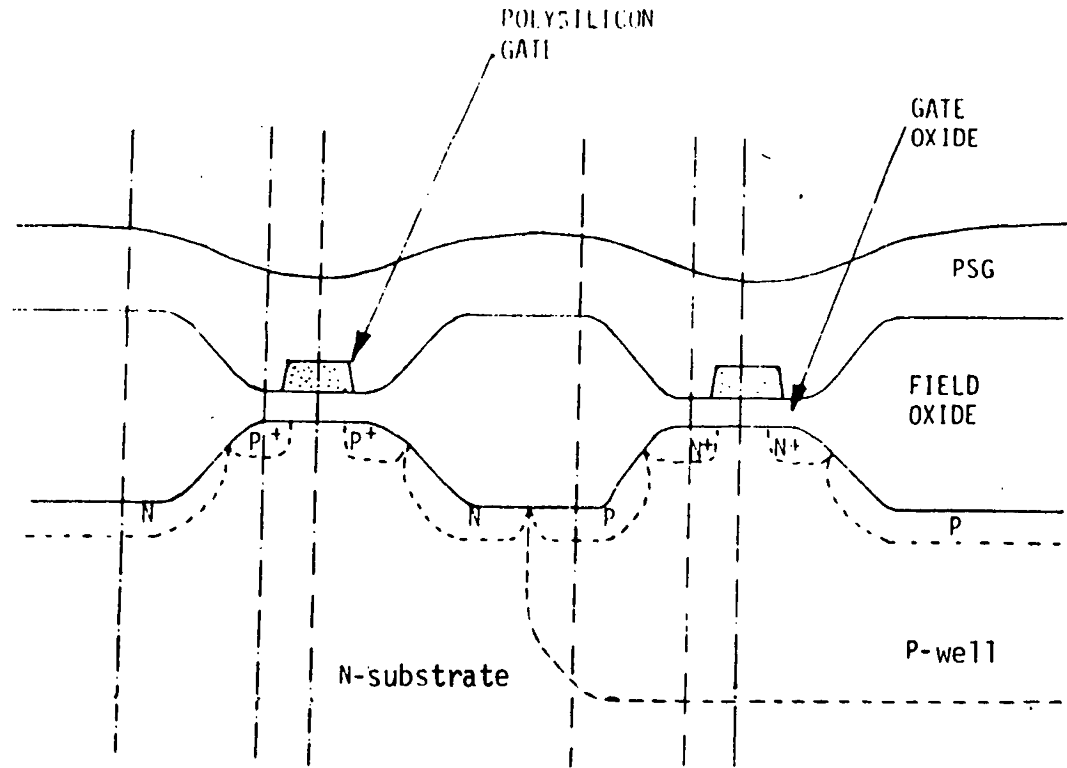


Figure 4.20 The Six Main Cross-Sections of a Bulk P-Well CMOS Process

(1) n-substrate implant 2.1×10^{12} cm^{-2} $^{31}P^{+}$ at 125 keV

(2) n-substrate drive-in 110 mins at 1000°C in wet O_2

(3) p-well implant 1.8×10^{13} cm^{-2} $^{11}B^{+}$ at 60 keV

(4) p-well drive-in 800 mins at 1200°C in dry O_2

(5) oxide strip, pad oxide growth, nitride deposition and etch

(6) p-well field implant 1.1×10^{13} cm^{-2} $^{11}B^{+}$ at 35 keV

(7) field implant drive-in 500 mins at 1025°C in dry O_2

(8) field oxidation (1.25μm) 1160 mins at 900°C in wet O_2

(9) nitroxide, nitride, oxide removal

(10) sacrifical gate oxide growth and removal

(11) gate oxidation (730Å) 24 mins at 1050°C in dry O_2

(12) gate oxide anneal 60 mins at 1050°C in N_2

(13) n-substrate threshold adjust implant 5×10^{15} cm^{-2} $^{11}B^{+}$ at 45 keV

(14) poly deposition and etch

(15) poly doping 85 mins at 900°C with $POCl_3$

(16) n-substrate source/drain implant 5×10^{15} cm^{-2} $^{11}B^{+}$ at 35 keV

(17) p-well source/drain implant 5×10^{15} cm^{-2} $^{31}P^{+}$ at 85 keV

(18) source/drain and PSG anneal 30 mins at 1000°C in N_2

Table 4.5 : CMOS process parameters for SUPREM simulation

Figure 4.21 : N-SUBSTRATE FIELD REGION

wafer c2#19

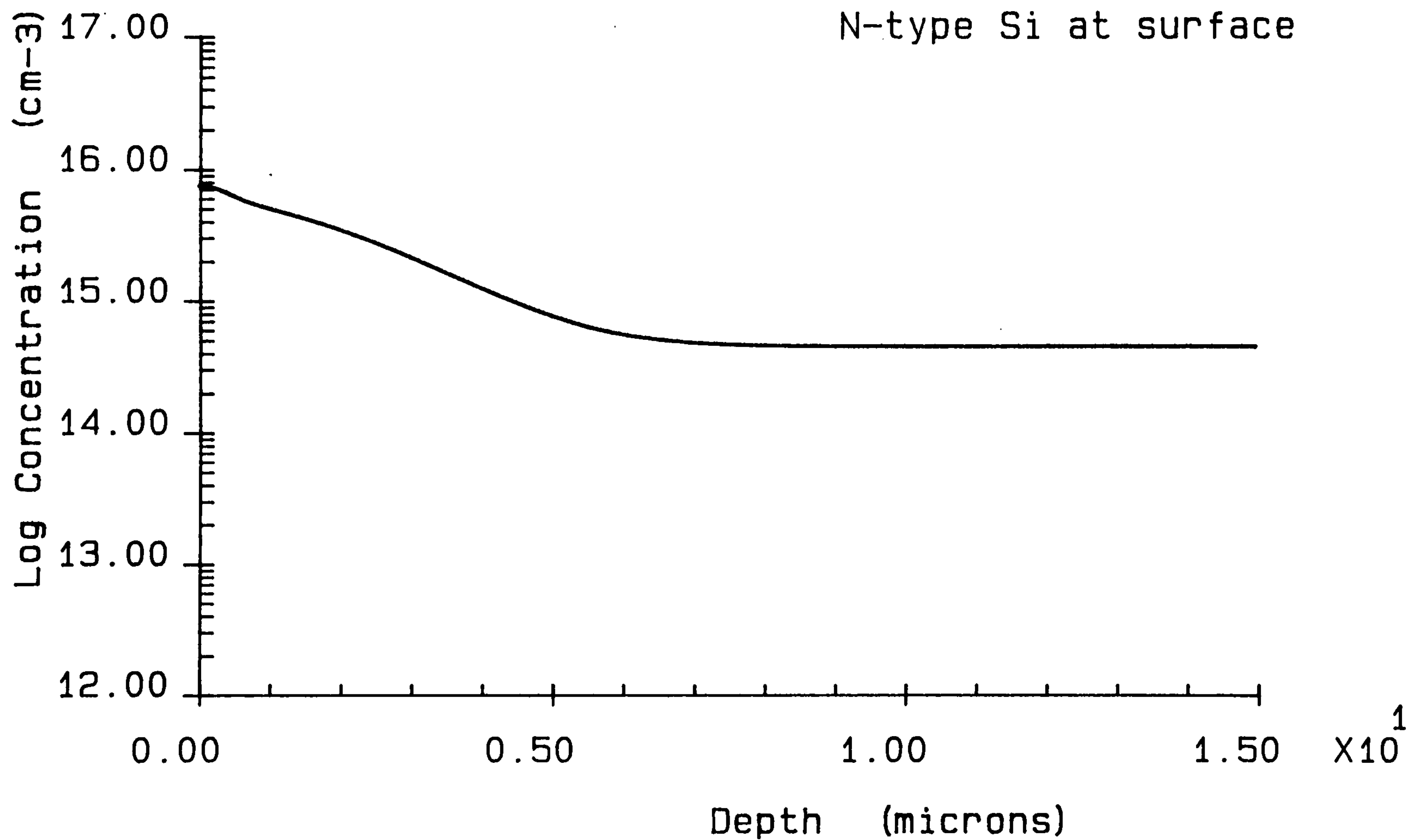


Figure 4.22 : N-SUBSTRATE SOURCE/DRAIN REGION

wafer c2#19

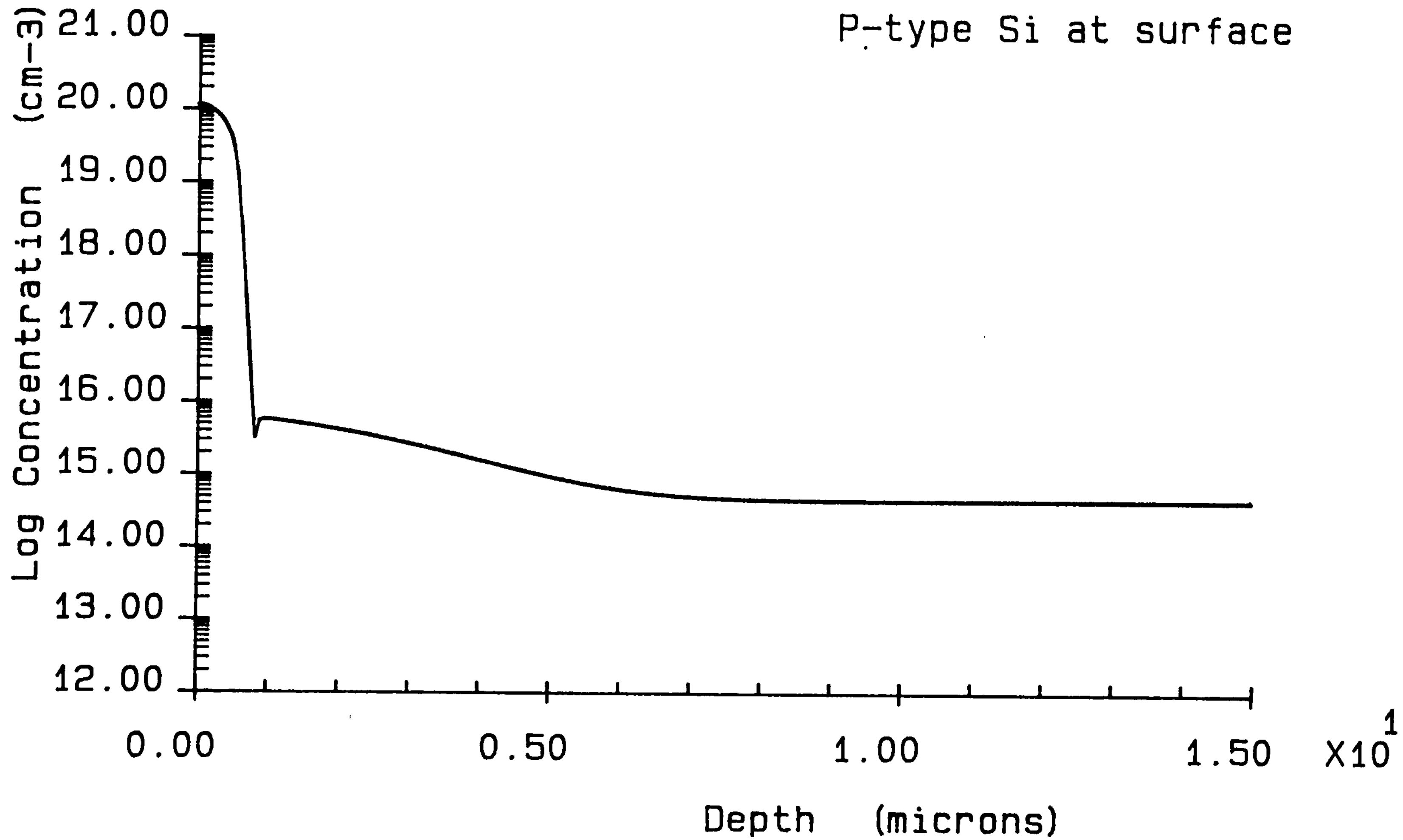


Figure 4.23 : N-SUBSTRATE ACTIVE REGION

wafer c2#19

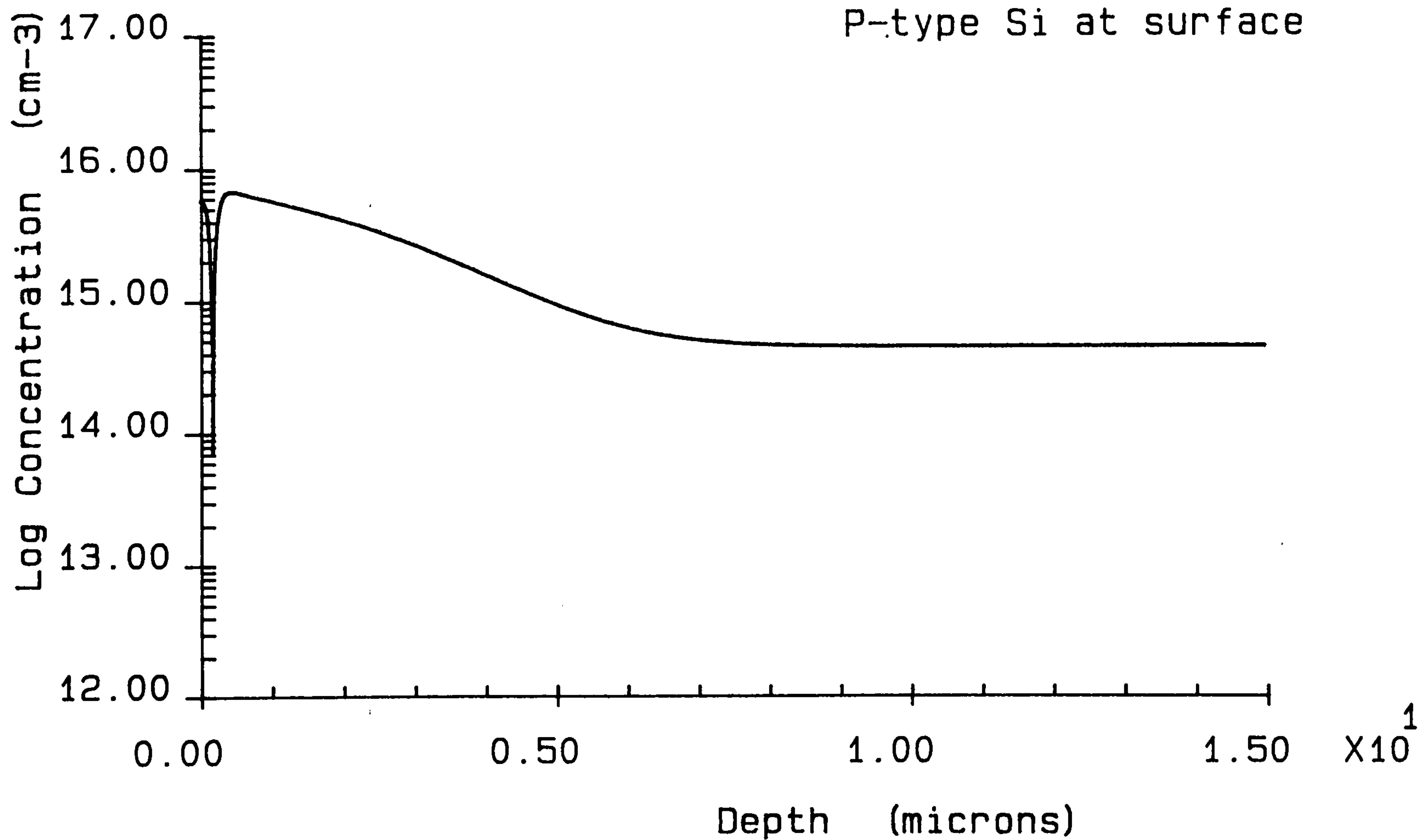


Figure 4.24 : P-WELL FIELD REGION

wafer c2#19

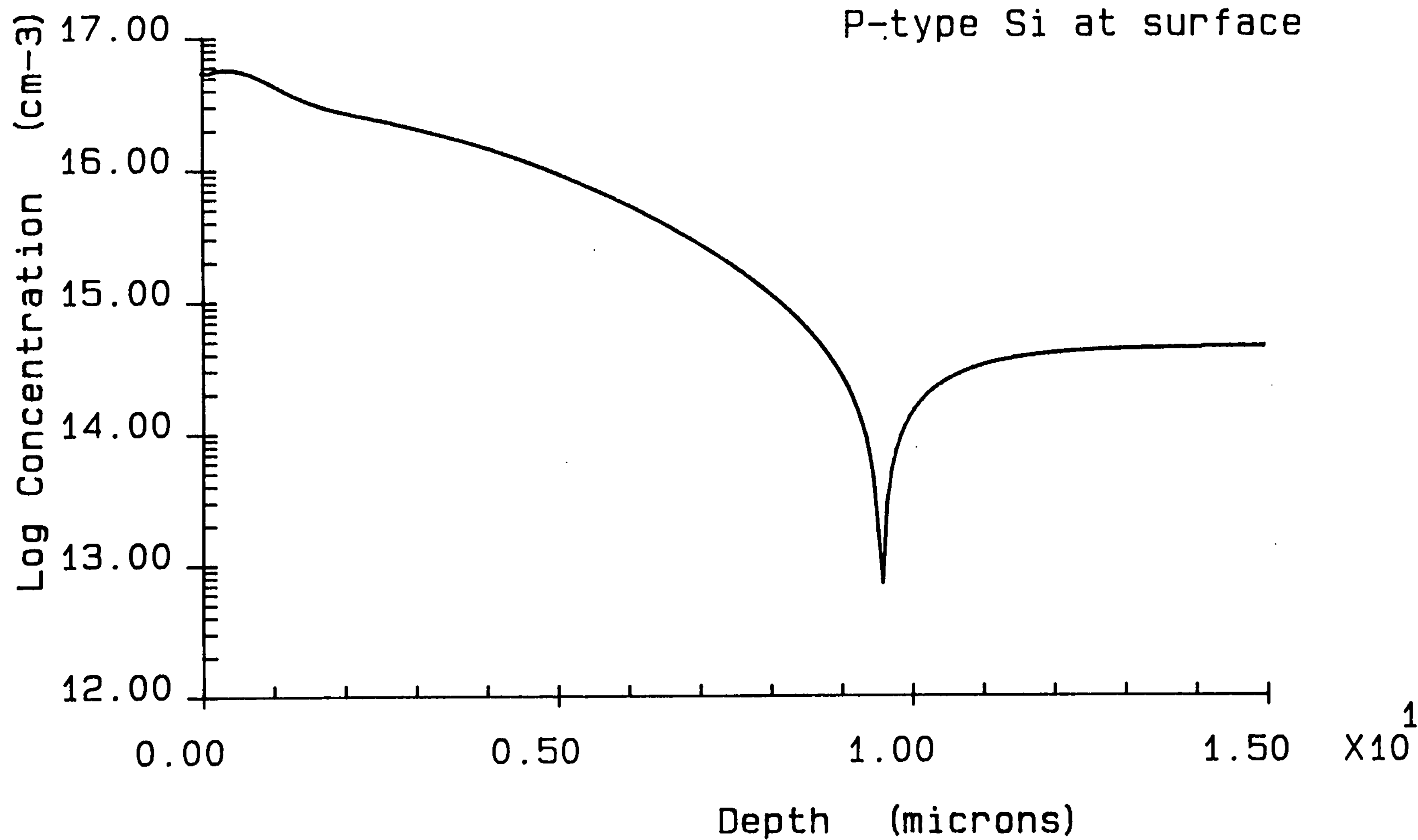


Figure 4.25 P-WELL SOURCE/DRAIN REGION

wafer c2#19

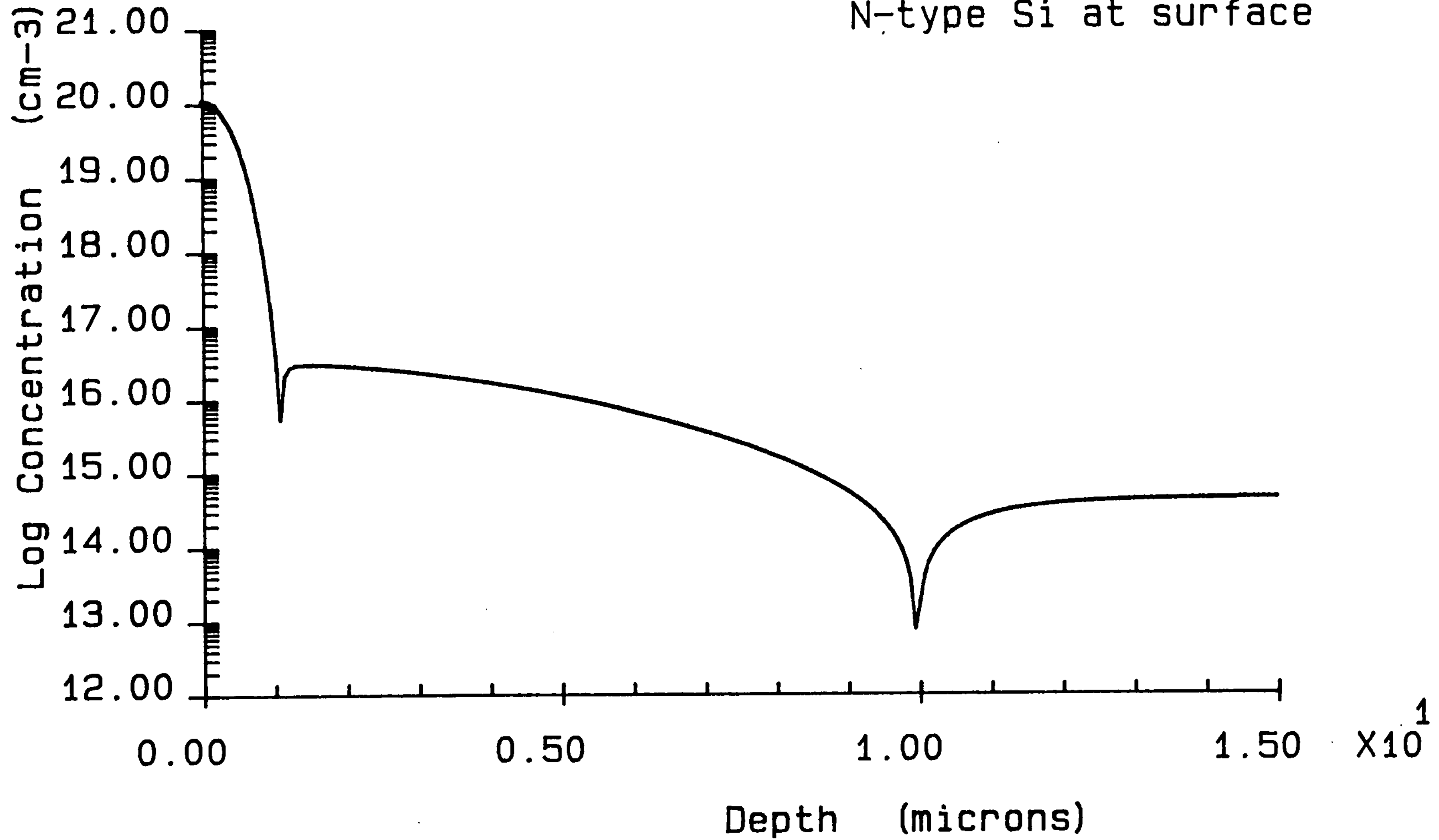
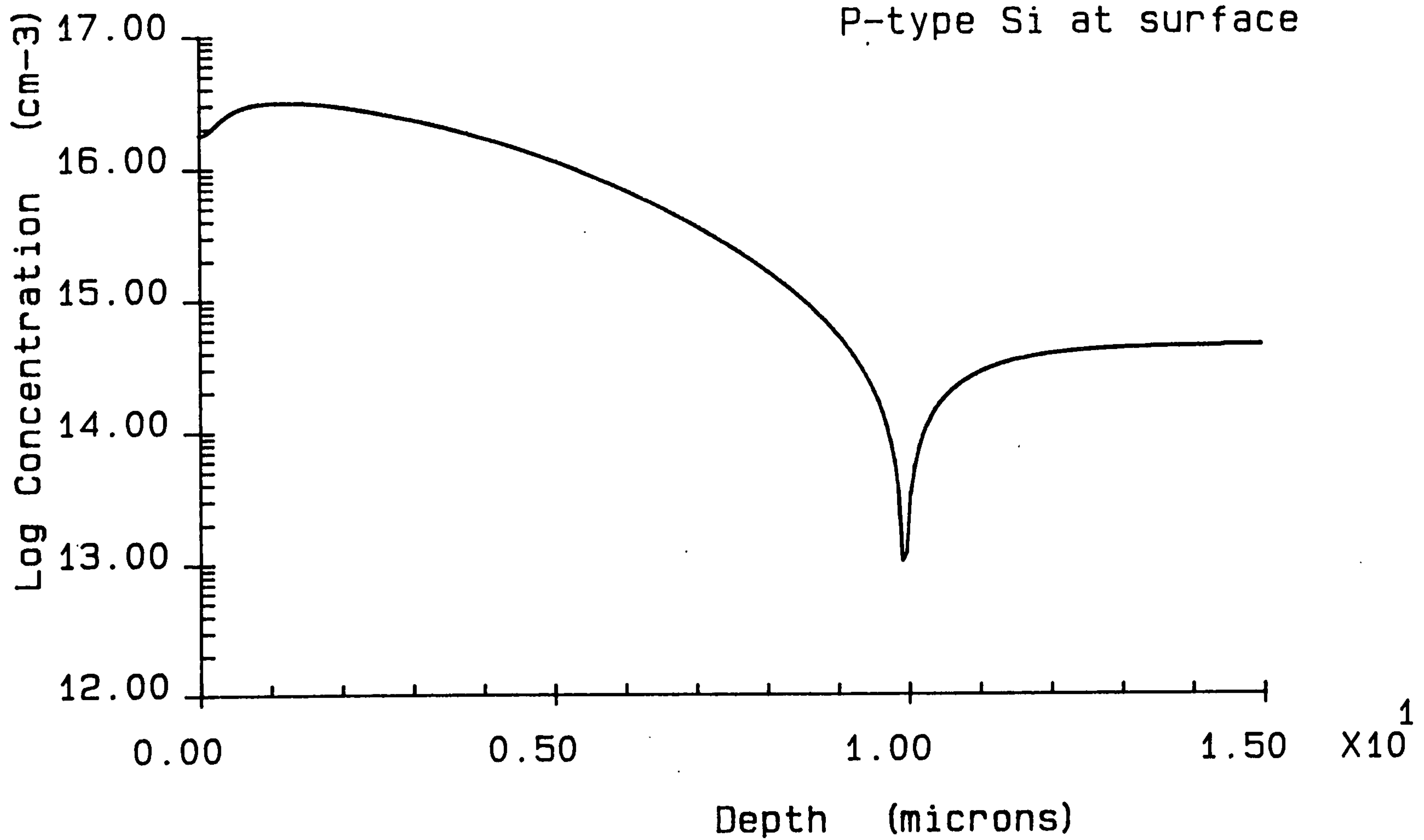


Figure 4.26 : P-WELL ACTIVE REGION

wafer c2#19



CHAPTER FIVE : MOS CAPACITANCE-VOLTAGE CHARACTERISTICS

5.1 USES AND TYPES OF C-V MEASUREMENTS

Capacitance-Voltage (C-V) measurements of MOS structures are routinely carried out on the semiconductor production line in order to monitor the fabrication process /217-219/. Contamination of furnace tubes and malfunction of ion implantation equipment can be diagnosed through inspection of C-V data. Since computer-aided manufacture (CAM) is now important for the semiconductor industry /4/, a computer controlled C-V characterisation system is required to store data for later examination and to maximise wafer throughput /220/.

Mobile metal ions such as Na^+ are potentially disastrous for MOS processes and such contamination can be detected in oxide layers by heating the wafer to a temperature of around 200°C /220/. An applied bias causes the metal ions to migrate at this temperature, and if a positive voltage is applied to the gate electrode with respect to the substrate, the ions collect at the silicon-silicon dioxide interface. Subsequent low or high frequency C-V measurements show the existence of such contaminants through a shift in the flat-band capacitance C_{FB}. A simulation of MOS capacitance is required to determine C_{FB} by a comparison of measured C-V data with the ideal C-V curve which neglects effects due to interface states and a non-zero work function difference between the gate material and the silicon substrate. The gate voltage at which the flat-band condition

occurs is known as the flat-band voltage V_{FB}, and any MOS transistor model requires this parameter for an accurate determination of threshold voltage V_T /6,7,13/.

The flatband voltages of n-channel and p-channel devices in a CMOS process are difficult to model from processing information since they depend on many factors including impurity concentration in the polysilicon gate, surface state density, oxide thickness, work function in the silicon bulk, and the impurity concentration at the surface of the source/drain regions where contacts to the aluminium are made /224/. Consequently it is probably more accurate to determine flat-band capacitance by electrical measurements for use in any device simulation.

Figure 5.1 shows an MOS capacitor structure, where the dielectric material on the wafer is usually silicon dioxide, and the gate electrode is typically composed of n-type or p-type heavily doped polysilicon, or aluminium.

C-V measurement techniques fall into three main categories: low frequency or quasi-static, high frequency and deep depletion. Deep depletion C-V measurements can be used to extract the 1-D doping profile at the surface of the silicon as already demonstrated in Chapter 4. Low frequency C-V measurements, where the minority carriers in inversion can follow the applied ac signal, must be carried out at frequencies lower than 10 Hz /227/, and metal shielding of the sample and connections is required to reduce noise levels /226/.

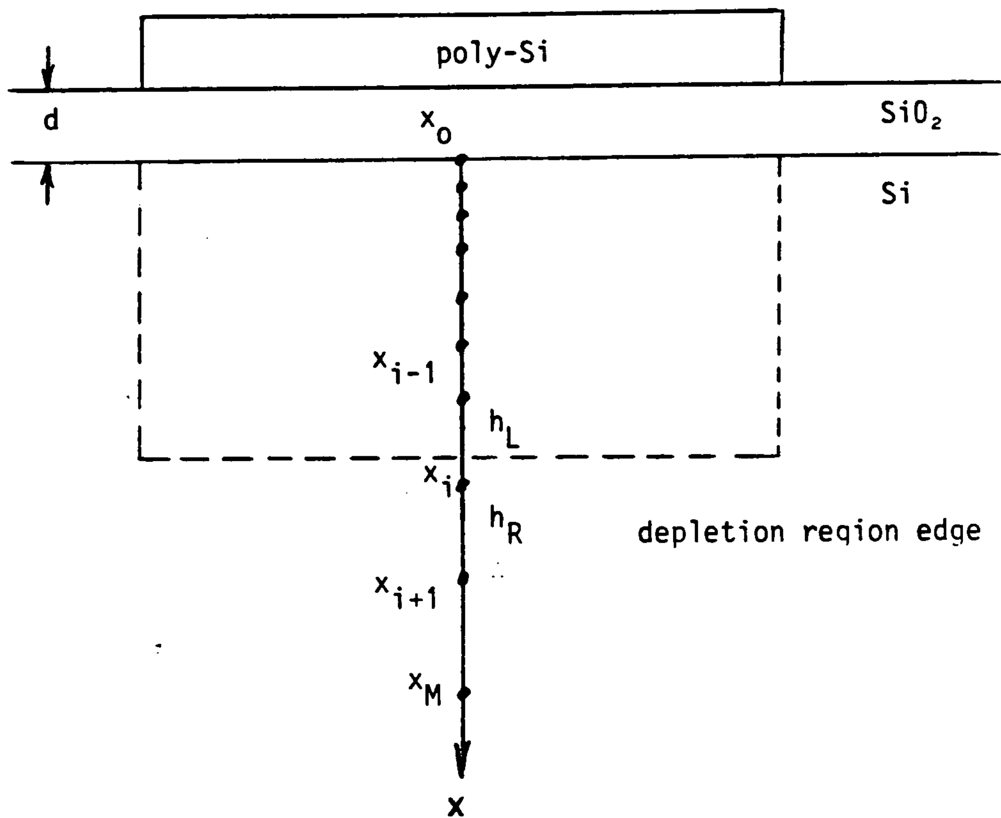


Figure 5.1 : MOS capacitor for C-V simulation

If a high frequency ac signal is used, the minority carriers in the inversion layer respond only slightly to the applied modulation and therefore contribute marginally to the capacitance of the silicon /216/. This type of C-V measurement is carried out most often, and a frequency of 1 MHz is usually chosen to minimise the effect of fast surface states at the Si - SiO_2 interface. While only ideal C-V characteristics are given theoretical consideration here, non-ideal effects are discussed in detail elsewhere /13, 226/.

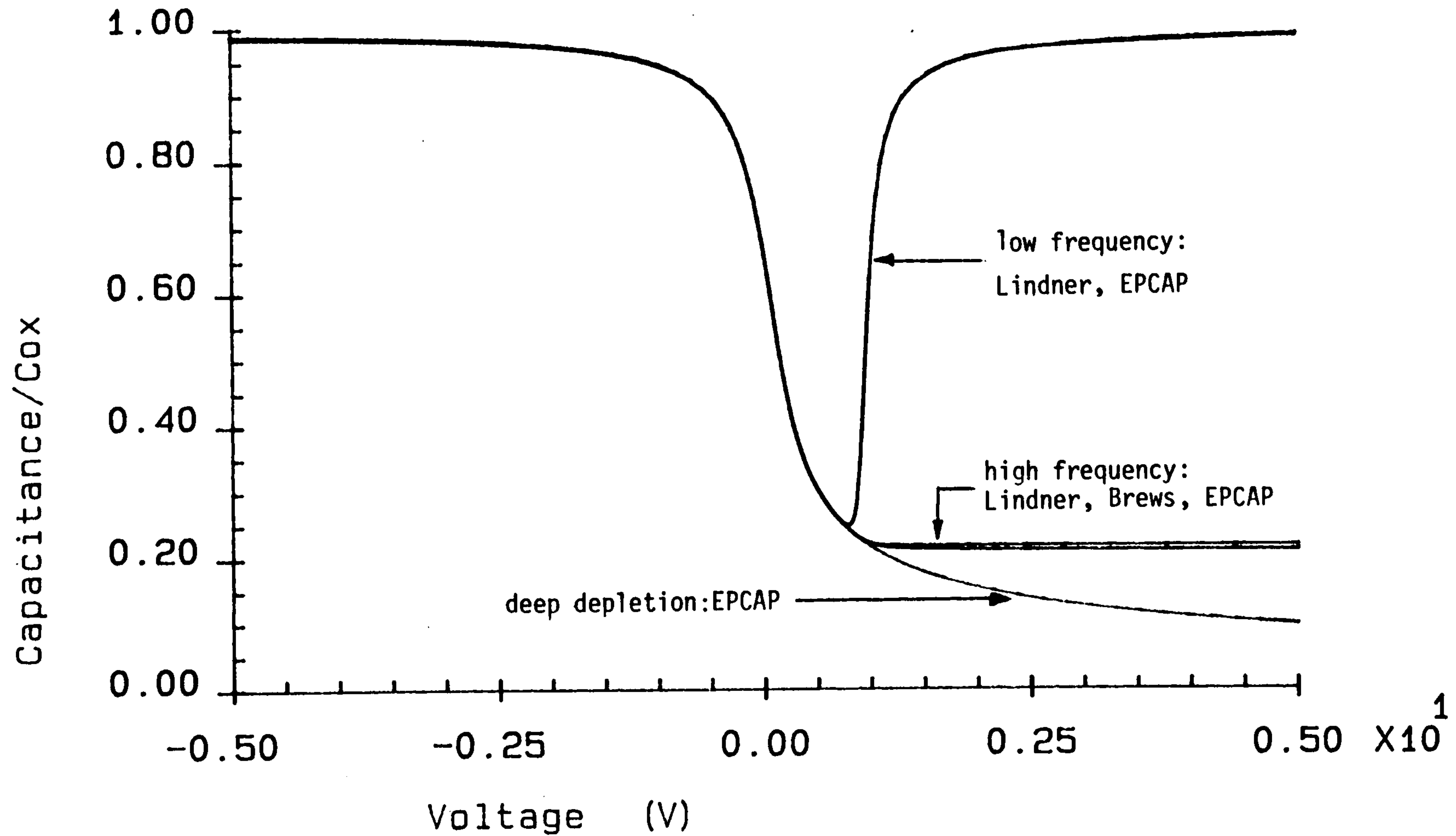
5.2 UNIFORM DOPING PROFILES

Lindner /214/ was the first to simulate MOS capacitance under both low and high frequency bias conditions for a uniformly doped semiconductor. Baccarani and Severi /215/ refined the high frequency model to accommodate minority carrier rearrangement in the inversion layer. Since this analysis involves the solution of an integro-differential equation, Brews /221/ has proposed a simplification to use for practical purposes where an empirical fit is used for the part of the high frequency curve in inversion. In the range of doping concentrations of practical interest, this formula is accurate to within 1.5% of the more complicated treatment of Baccarani and Severi.

Assuming a uniform p-type doping concentration of $N = 10^{15}$ cm^{-3}, a gate oxide thickness of d = 800Å and a flat-band voltage V_{FB} of 0V, figure 5.2 shows the ideal low frequency C-V curve according to Lindner /214/, and a comparison of the high frequency C-V

Figure 5.2 : **MOS Capacitance-Voltage Models**

$N = 10^{15}\ cm^{-3}$; $d = 800 Å$; $V_{FB} = 0V$



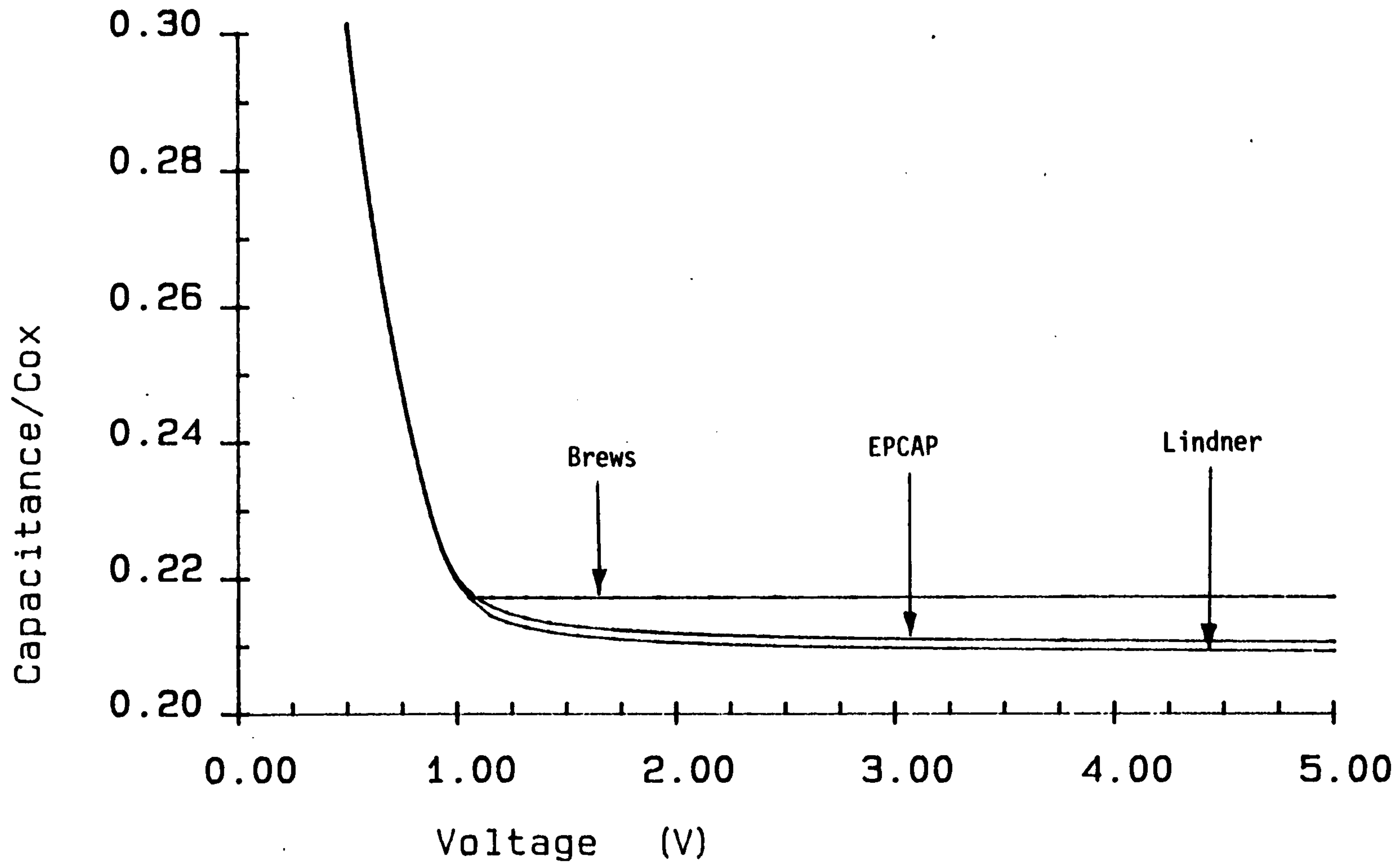
models due to Lindner /214/ and Brews /221/. The region of positive voltage is expanded in figure 5.3 to clarify the difference between the high frequency models, but the separation of the three curves in inversion is negligible for most practical purposes.

5.3 NON-UNIFORM DOPING PROFILES

In typical MOS processes, the impurity concentration at the surface of the silicon wafer is not constant and capacitance simulations of non-uniform doping profiles are required. Jaeger et al /223/ have proposed an elegant MOS capacitance algorithm for use in NMOS technology. These authors consider a temperature range of 50 - 350K, and also the energy dependence of interface state density. A generalisation of this method is necessary to allow simulation of CMOS structures, where the electric field in the vertical direction may never disappear as in the case of a p-well or n-well. A less restrictive boundary condition must be used at the point where the simulation mesh terminates in the silicon bulk. This modification is implemented in EPCAP (Edinburgh Program for Capacitance of MOS Structures), and the case considered by Jaeger et al /223/ is a special case of the algorithm now presented.

The total capacitance C(V) of the MOS structure is given by the series combination of the capacitance of the oxide C_{ox} and the space-charge capacitance of the silicon C_s through

Figure 5.3 : MOS HF Capacitance-Voltage Models



$$C(V) = \frac{C_{ox}C_s}{C_{ox} + C_s} \qquad (5.1)$$

where

$$C_{ox} = \frac{\varepsilon_s}{d} \qquad (5.2)$$

All capacitances are assumed to be for unit area, ε_s is the permittivity of silicon and d is the oxide thickness.

For convenience the quasi-static capacitance of the silicon will be derived first, and the cases of high frequency and deep depletion will be considered in retrospect as was done by Jaeger et al /223/. The differential capacitance of the silicon is defined by

$$C_s = \frac{\partial Q_s}{\partial \psi_s} \qquad (5.3)$$

where Q_s is the total silicon charge per unit area and ψ_s is the surface potential. Following Nicollian and Brews /226/, the term 'flat-band' is retained even although the energy bands are not flat by virtue of the non-uniform doping in the silicon. In this context a reference to 'flat-band' corresponds to the condition of zero charge density everywhere in the silicon region of interest.

As is usual in semiconductor device simulation activity, po-

tential ψ is defined as /7, 228/

$$\psi = \frac{E_F - E_i}{q} \tag{5.4}$$

where E_F is the Fermi energy, E_i is the intrinsic energy level and q is the modulus of the electronic charge.

The total charge in the silicon Q_s is given by

$$Q_s = \int_{x=0}^{\infty} \rho(x)\, dx \tag{5.5}$$

where ρ is the charge density. Substitution of (5.5) in (5.3) gives

$$C_s = \int_{x=0}^{\infty} \frac{\partial \rho}{\partial \psi} \frac{\partial \psi}{\partial \psi_s}\, dx \tag{5.6}$$

Steady-state conditions are described by Poisson's equation which is

$$\frac{\partial^2 \psi}{\partial x^2} = - \frac{\rho(x)}{\varepsilon_s} \tag{5.7}$$

where the charge density is

$$\rho(x) = q(p - n + N_D^{\ +} - N_A^{\ -}) \tag{5.8}$$

Here N_D^+ is the density of ionised donors, N_A^- is the density of ionised acceptors, and the electron concentration n and hole concentration p are given by

$$n = n_i \exp(\beta\psi) \tag{5.9}$$

$$p = n_i \exp(-\beta\psi) \tag{5.10}$$

The parameter β is defined by

$$\beta = \frac{q}{k_B T} \tag{5.11}$$

The approximation that all donors and acceptors are ionised is assumed, and the net concentration of either n-type or p-type silicon is represented by N. Equation (5.7) is an elliptic partial differential equation subject to boundary conditions

$$\psi = \psi_s \qquad ; \quad x = 0 \tag{5.12}$$

$$\psi = \begin{cases} \dfrac{k_B T}{q} \ln \dfrac{N}{n_i} & \text{, donors} \\ -\dfrac{k_B T}{q} \ln \dfrac{N}{n_i} & \text{, acceptors} \end{cases} \quad ; \quad x = x_M \qquad (5.13)$$

where, from figure 5.1, the bulk boundary at $x = x_M$ is chosen to be well outside the region of accumulation or depletion at the surface of the silicon.

Jaeger et al /223/ assume that electric field vanishes in the bulk through

$$\frac{\partial \psi}{\partial x} = 0 \qquad ; \qquad x = x_M \qquad (5.14)$$

However this is not true in CMOS structures by virtue of the built-in potential. The homogeneous Neumann-type boundary condition (5.14) corresponds to a special case of the Dirichlet boundary condition (5.13) when the concentration N is invariant in the region of $x = x_M$.

The finite difference method is used to solve for potential in Poisson's equation (5.7) /222/. Central differences are used to approximate the second order derivative term through

$$\frac{\partial^2 \psi}{\partial x^2} \cong \frac{2}{h_L(h_L + h_R)} \psi_{i-1} - \frac{2}{h_L h_R} \psi_i + \frac{2}{h_R(h_L + h_R)} \psi_{i+1} \qquad (5.15)$$

where $\psi_i = \psi(x_i)$ and the distances h_L and h_R relative to the i'th grid node are defined in figure 5.1. Boundary conditions (5.12) and (5.13) are discretised to

$$\psi_o = \psi_s \tag{5.16}$$

$$\psi_M = \begin{cases} \dfrac{k_B T}{q} \ln \dfrac{N(x_M)}{n_i}, & \text{donors} \\[2ex] -\dfrac{k_B T}{q} \ln \dfrac{N(x_M)}{n_i}, & \text{acceptors} \end{cases} \tag{5.17}$$

The discretised form of Poisson's equation is written in homogeneous form to give

$$f_i = \frac{2h_R}{h_L + h_R} \psi_{i-1} - 2\psi_i + \frac{2h_L}{(h_L + h_R)} \psi_{i+1}$$

$$+ \frac{qh_L h_R}{\varepsilon_s} [\pm N + n_i \{\exp(-\beta\psi_i) - \exp(\beta\psi_i)\}] = 0 \quad ,$$

$$\begin{matrix} + \text{ donors} \\ - \text{ acceptors} \end{matrix} \quad ; \quad i = 1\ (1)\ M - 1 \tag{5.18}$$

where a total of $(M + 1)$ grid points are used. Equation (5.18) can be written in vector form as

$$\underline{f}\ (\underline{\psi}) = 0 \tag{5.19}$$

where

$$\underline{f} = [f_1 \quad f_2 \quad \cdots\cdots\cdots \quad f_{M-1}]^T \tag{5.20}$$

$$\underline{\Psi} = [\psi_1 \quad \psi_2 \quad \cdots\cdots\cdots \quad \psi_{M-1}]^T \tag{5.21}$$

Equation (5.19) represents a non-linear system of (M - 1) unknowns, corresponding to the value of potential at each internal grid point. Linearisation is accomplished using Newton's method /78/ where a correction vector $\underline{\Delta\psi}$ is added to an initial guess for $\underline{\psi}$.

$$\underline{f}\,(\underline{\psi} + \underline{\Delta\psi}) = \underline{f}(\underline{\psi}) + \underset{\sim}{J}\,\underline{\Delta\psi} = 0 \tag{5.22}$$

Explicitly,

$$\begin{bmatrix} \frac{\partial f_1}{\partial \psi_1} & \frac{\partial f_1}{\partial \psi_2} & \cdots\cdots & \frac{\partial f_1}{\partial \psi_{M-1}} \\ \frac{\partial f_2}{\partial \psi_1} & \frac{\partial f_2}{\partial \psi_2} & \cdots\cdots & \frac{\partial f_2}{\partial \psi_{M-1}} \\ \vdots & \vdots & & \vdots \\ \frac{\partial f_{M-1}}{\partial \psi_1} & \frac{\partial f_{M-1}}{\partial \psi_2} & \cdots\cdots & \frac{\partial f_{M-1}}{\partial \psi_{M-1}} \end{bmatrix} \begin{bmatrix} \Delta\psi_1 \\ \Delta\psi_2 \\ \vdots \\ \Delta\psi_{M-1} \end{bmatrix} = - \begin{bmatrix} f_1 \\ f_2 \\ \vdots \\ f_{M-1} \end{bmatrix} \tag{5.23}$$

where the elements of the Jacobian matrix $\underset{\sim}{J}$ are obtained by analytical differentiation of (5.18) /223/.

Convergence is achieved through successive linearisation, and the (k+1)th approximation to the solution is obtained from the previous approximation, the kth, through

$$\underline{\psi}^{(k+1)} = \underline{\psi}^{(k)} + \underline{\Delta\psi}^{(k)} \tag{5.24}$$

where $\underline{\Delta\psi}^{(k)}$ is the solution of (5.23) at the kth iteration. The Jacobean matrix is sparse and tridiagonal in nature, so the matrix equation at each iteration can easily be solved using a direct technique /23/. In practice, only a few iterations are necessary for the solution to converge to a small limit. For Digital Equipment Corporation VAX machines, a tolerance limit of 10^{-6} V is suitable.

Once the steady-state potential solution has been obtained, the silicon capacitance C_S is determined by numerical integration of equation (5.6) using Simpson's rule /78/. The grid points used for the integration are chosen to be identical to those used in the finite difference discretisation. The integrand at the i'th node is given by

$$\left. \frac{\partial \rho}{\partial \psi} \frac{\partial \psi}{\partial \psi_s} \right|_i = \frac{\partial \rho}{\partial \psi} (x_i) \frac{\partial \psi_i}{\partial \psi_s} \tag{5.25}$$

Now $\partial\rho/\partial\psi$ is obtained by differentation of (5.8) analytically, however a first order perturbation approach is required to evaluate $\partial\psi_i/\partial\psi_s$ for each i. The surface potential ψ_s is perturbed by an infinitesimal amount $d\psi_s$, and the resulting change in potential at all other node points is represented by the unknown vector $\underline{d\psi}$. Equation (5.22) is essentially a first order Taylor expansion, which, in the limit $|\underline{\Delta\psi}| \to 0$, can be written in differential form as

$$\frac{\partial \underline{f}}{\partial \psi_s} + \underset{\sim}{J} \frac{\partial \underline{\psi}}{\partial \psi_s} = 0 \tag{5.26}$$

where

$$\frac{\partial \underline{f}}{\partial \psi_s} = \left[\frac{\partial f_1}{\partial \psi_s} \; \frac{\partial f_2}{\partial \psi_s} \; \cdots\cdots\cdots \; \frac{\partial f_{M-1}}{\partial \psi_s}\right]^T \tag{5.27}$$

and

$$\frac{\partial \underline{\psi}}{\partial \psi_s} = \left[\frac{\partial \psi_1}{\partial \psi_s} \; \frac{\partial \psi_2}{\partial \psi_s} \; \cdots\cdots\cdots \; \frac{\partial \psi_{M-1}}{\partial \psi_s}\right]^T \tag{5.28}$$

The components of the vector (5.28) are precisely those required for numerical integration in (5.25). The entries of the Jacobian matrix J are evaluated analytically as before, and the components of vector (5.27) are evaluated from the perturbed form of equation (5.18). Since f_1 is the only difference equation involving $\psi_0 = \psi_s$, the partial derivative of f_1 is the only non-zero component. In detail,

$$\frac{\partial f_i}{\partial \psi_s} = \begin{cases} \dfrac{2h_R}{(h_L + h_R)} & ; \quad i=1 \\ 0 & ; \quad i=2(1)M-1 \end{cases} \tag{5.29}$$

Following solution of the matrix equation (5.26), the silicon capacitance is evaluated from (5.6) and then substituted in (5.1) to give the total low frequency or quasi-static capacitance of the MOS structure.

To simulate high frequency C-V characteristics, Poisson's equation is solved as before, but for the calculation of capacitance the minority carriers are omitted from the charge density in (5.18). For pulsed or deep-depletion C-V simulation, it is necessary to remove the minority carrier terms from both Poisson's equation in the solution for potential and the subsequent calculation of capacitance /223/.

5.4 EPCAP SIMULATION RESULTS AND DETERMINATION OF FLATBAND VOLTAGE

The so-called 'flat-band' condition occurs when a state of zero charge density occurs in the silicon. Assuming quasi-neutrality, this corresponds to a surface potential $\psi_s = \psi_{FB}$ defined by

$$\psi_{FB} = \begin{cases} \dfrac{k_B T}{q} \ln \dfrac{N(x=0)}{n_i} & ; \text{ donors} \\[2ex] -\dfrac{k_B T}{q} \ln \dfrac{N(x=0)}{n_i} & ; \text{ acceptors} \end{cases} \tag{5.30}$$

While this assumption is directly applicable to all typical p-well CMOS impurity profiles, this is not possible in the n-substrate region by virtue of the p-type surface implant as shown in figure 4.23. When a p-n junction exists close to the silicon surface, the depletion region precludes use of the quasi-neutrality approximation.

It is well known in the semiconductor industry that implanted samples of silicon like this show a curious dip in the high frequency curve at the onset of inversion. This phenomenon provides an easy test on the production line to determine whether a wafer has

been implanted or not. Fang /225/ discusses this observation, and the effect of a surface implant on the threshold voltage of the PMOSFET. However, no capacitance model of such devices exists at the present time.

P-channel MOSFET's with threshold voltages in the range -1.0V to -0.5V can be fabricated as part of a p-well CMOS process with no threshold adjust implant provided that heavily p-type doped (P+) polysilicon is used for the gate material. For such a process, equation (5.30) can be applied to both the n-substrate and p-well regions.

Figure 5.4 shows the non-uniform n-type doping profile characteristic of the active region of a p-channel MOSFET with a P+ polysilicon gate and a gate oxide thickness of 840Å. A comparison of EPCAP simulation results for an ideal MOS capacitor with this doping profile in the silicon substrate and measured high frequency (1 MHz) data from the real capacitor is shown in figure 5.5. The measured and simulated values of minimum capacitance in the inversion region are reasonably consistent. The displacement of the graphs along the voltage axis corresponds to the flat-band voltage V_{FB} of the real MOS capacitor. This parameter should be measured at the flat-band capacitance C_{FB} as shown in the diagram. In this particular case C_{FB} = 32.2 nF cm^{-2} and V_{FB} = 1.0V. Also plotted are the simulation results for low frequency (quasi-static) and deep depletion cases.

Figure 5.4 : Impurity Doping Profile wafer c1#7

P+ poly-Si/ gate oxide/ n-substrate

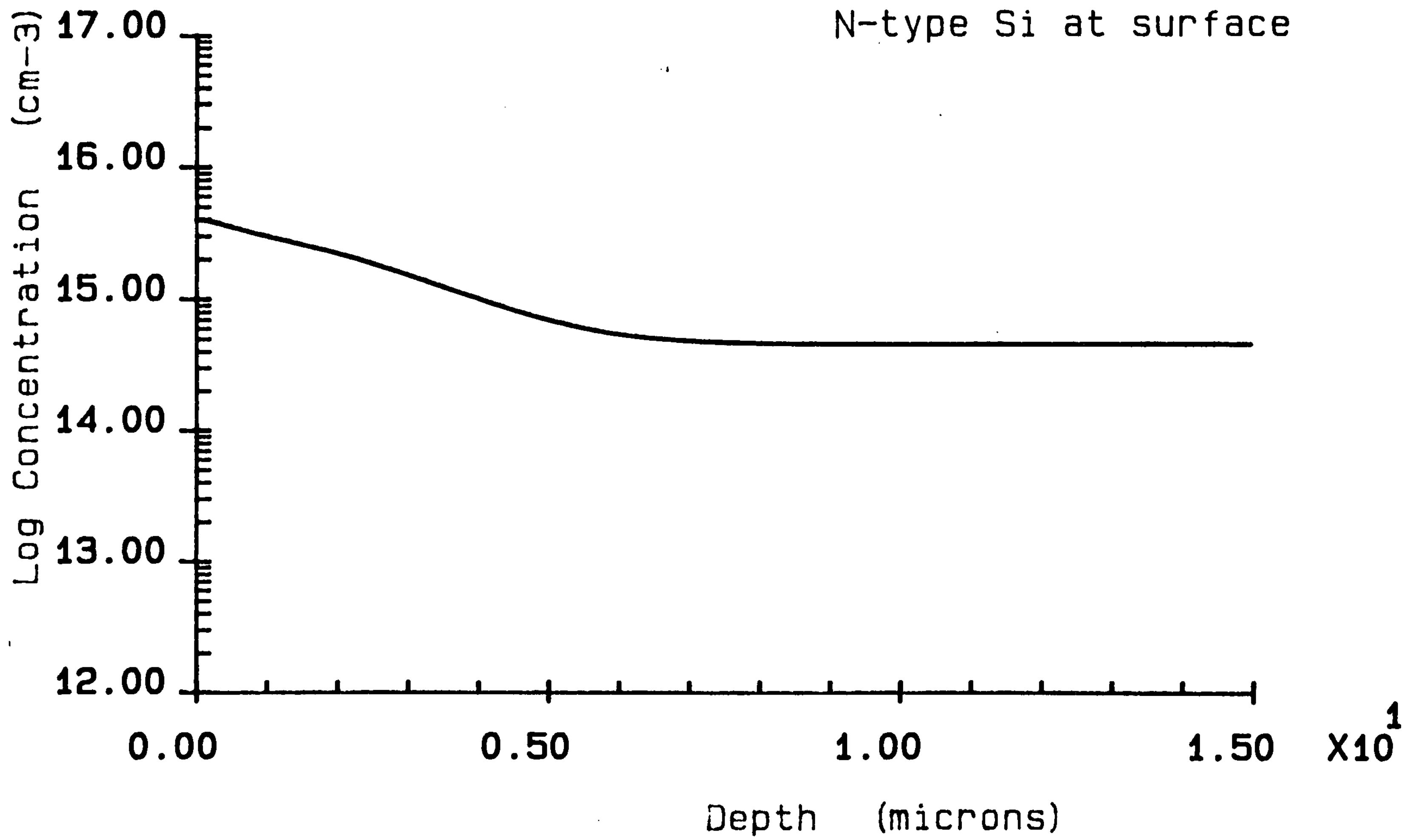


Figure 5.5 : C–V Characteristics wafer c1#7

n–substrate 840 Å gate oxide

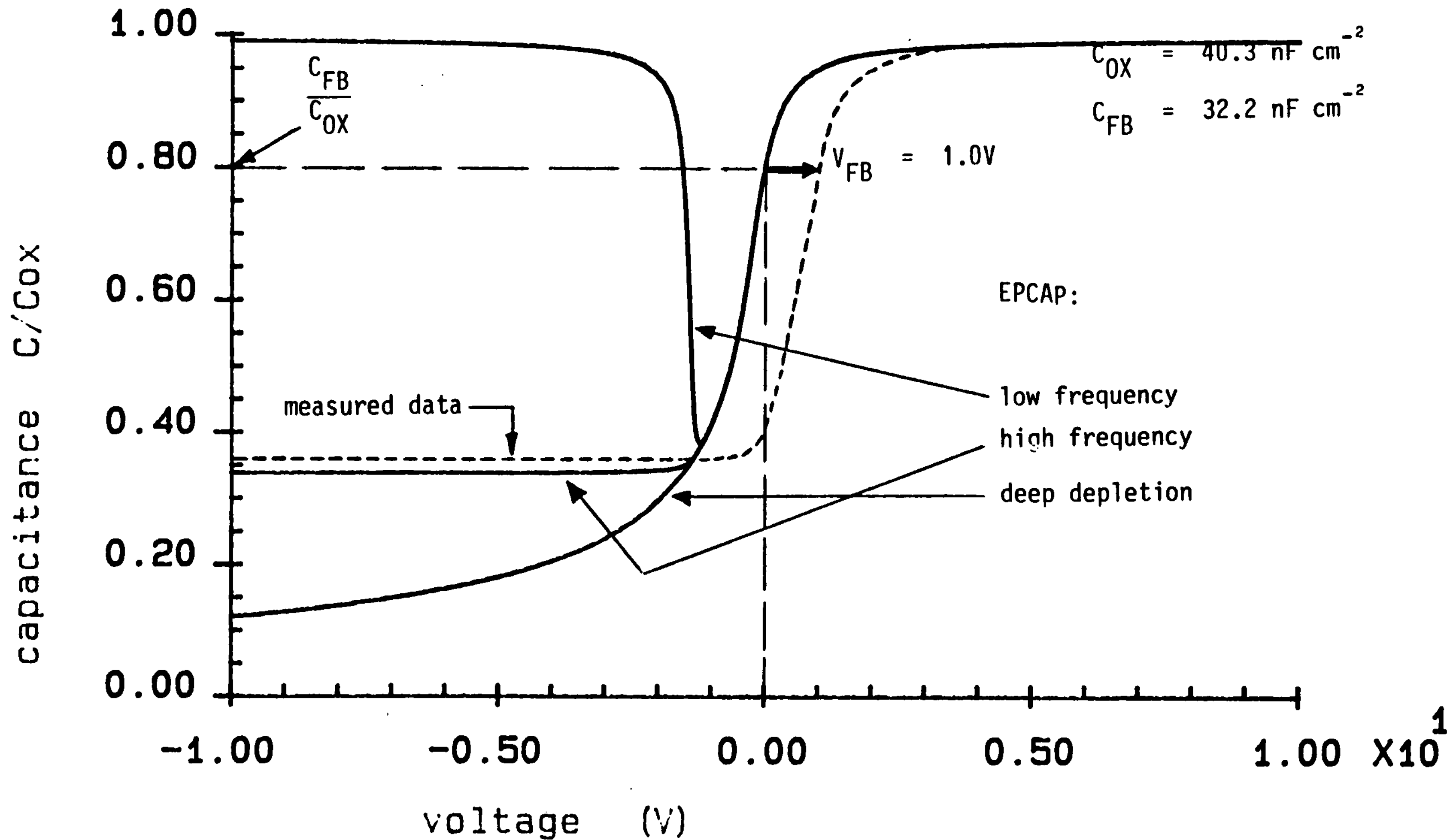


Figure 5.6 shows a typical p-well profile and the measured and simulated C-V characteristics are shown in figure 5.7. The agreement between the high frequency curves in the inversion region is very good, and it is found that C_{FB} = 35.6 nF cm^{-2} and V_{FB} = -1.5V.

The MOS capacitance simulations provide an additional check on the accuracy of the 1-D process simulations, and the method allows determination of flat-band capacitance for MOS device simulation purposes.

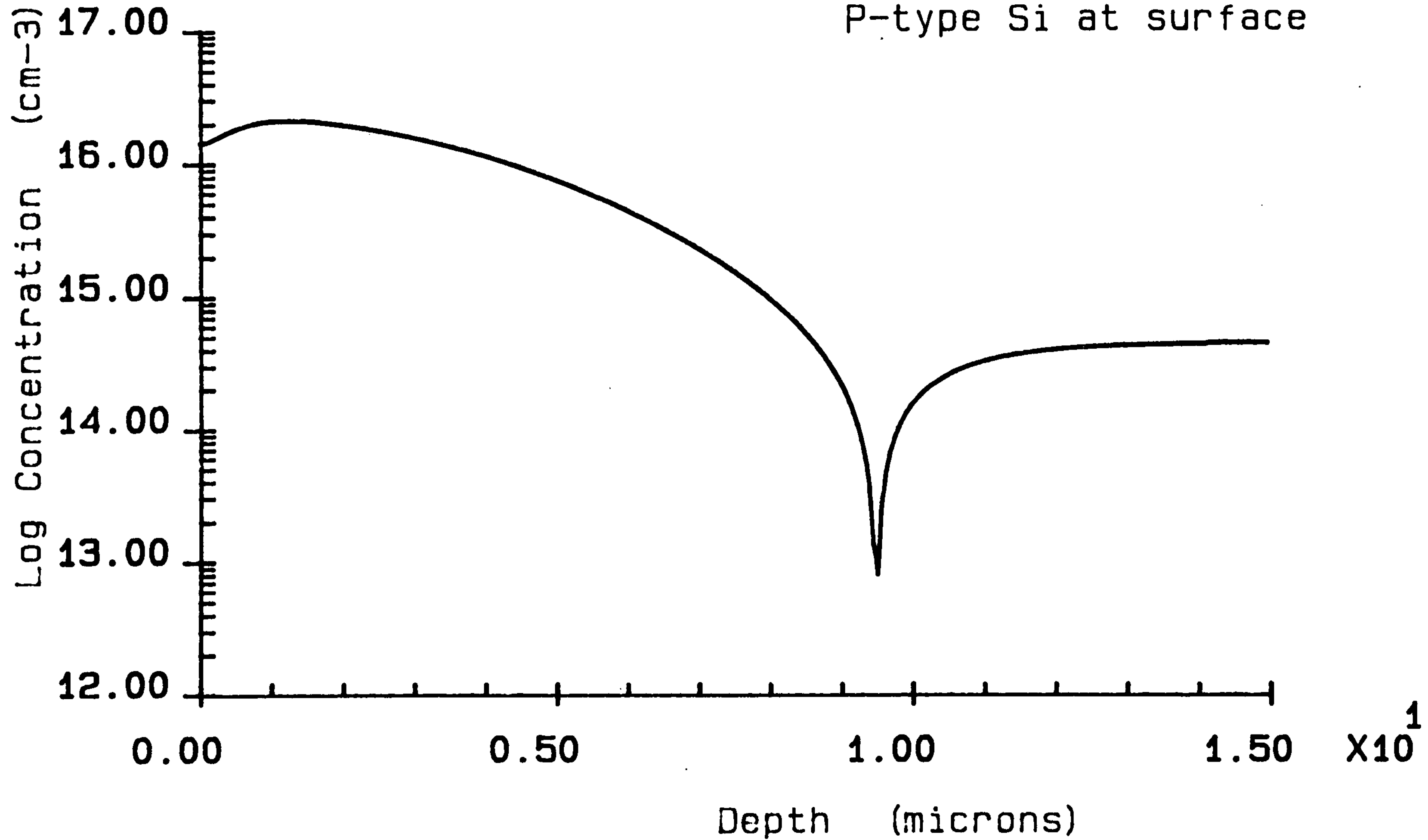
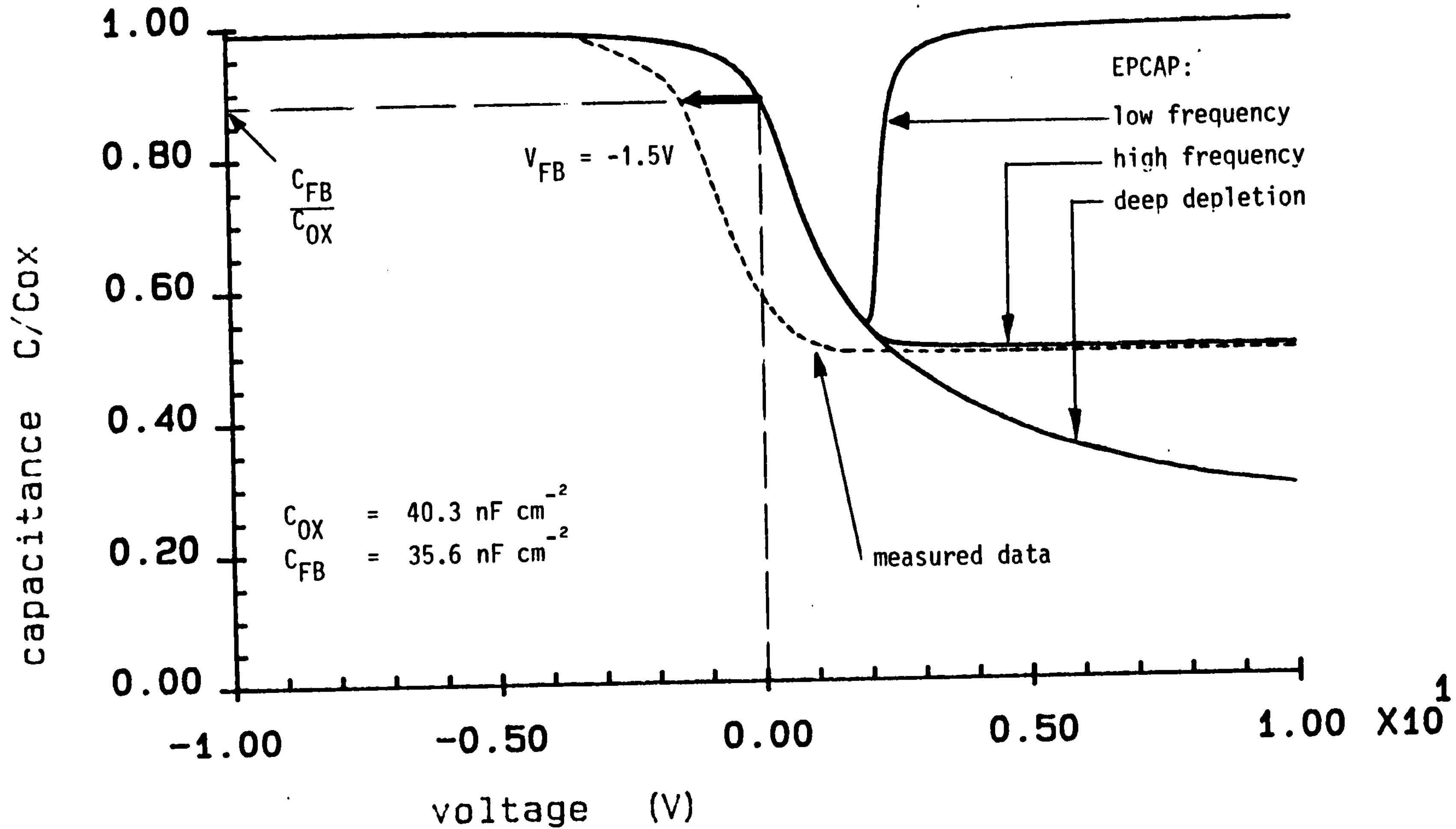


Figure 5.6 : Impurity Doping Profile wafer c1#7

Figure 5.7 : C–V Characteristics wafer c1#7

p–well 840 Å gate oxide



CHAPTER SIX : ANALYTICAL PROCESS MODELS

6.1 THE REDISTRIBUTION OF IMPURITIES NEAR MASK EDGES

6.1.1 Review of 2-D Analytical Process Models

Simulation of ion implantation of impurity species and subsequent redistribution due to diffusion at high temperatures is well established for the one-dimensional case /13,52/. While one-dimensional process models continue to be important for the vertical direction, the small size of MOS devices now fabricated means that lateral effects must also be considered. Two-dimensional (2-D) and three-dimensional (3-D) models are required to simulate VLSI processes. Analytical models are particularly useful because they allow impurity doping profiles to be specified in closed form for fast execution speeds in a computer program.

Analytical solution of the diffusion equation requires the assumption of a constant diffusivity D in order that well-established solution techniques /56/ can be used. Diffusion is independent of dopant concentration N provided $N < n_i$, where n_i is the intrinsic carrier concentration. The enhancement of diffusion at higher concentration levels due to the existence of defects and a local electric field has already been discussed in chapter 4. However, at very high concentration levels typical of source/drain re-

gions, impurity clustering reduces the local electric field, and so a simple-minded analytical treatment assuming no diffusion enhancement is found to be more accurate than is initially expected. In addition, approximate simulation results are useful before a full numerical treatment is undertaken to accommodate a concentration-dependent diffusivity as discussed in Chapter 7.

Kennedy and O'Brien /57/ consider the diffusion of impurities under mask edges during the fabrication of planar p-n junctions. They deal with two cases: in the first, a constant impurity atom concentration is maintained at the surface, and in the second, the total number of atoms involved in the diffusion process is fixed.

Modern MOS processes make full use of ion implantation and so require simulations of the redistribution of Gaussian implanted profiles. Krusius et al /58/ apply analytical models to diffused regions in a metal-semiconductor field effect transistor (MESFET). However, their method suffers from the disadvantage that a linearly varying mask edge must be approximated by a 'staircase' function, and contributions from many steps must be summed to obtain an adequate representation of the final profile.

The model presented here clarifies the work of Lee and Dutton /15/ but considers a more general masking layer structure. Figure 6.1 shows the geometry considered by these authors. Ion implantation is performed into bare silicon on the left side of the simulation area and the right side is masked by a material layer whose

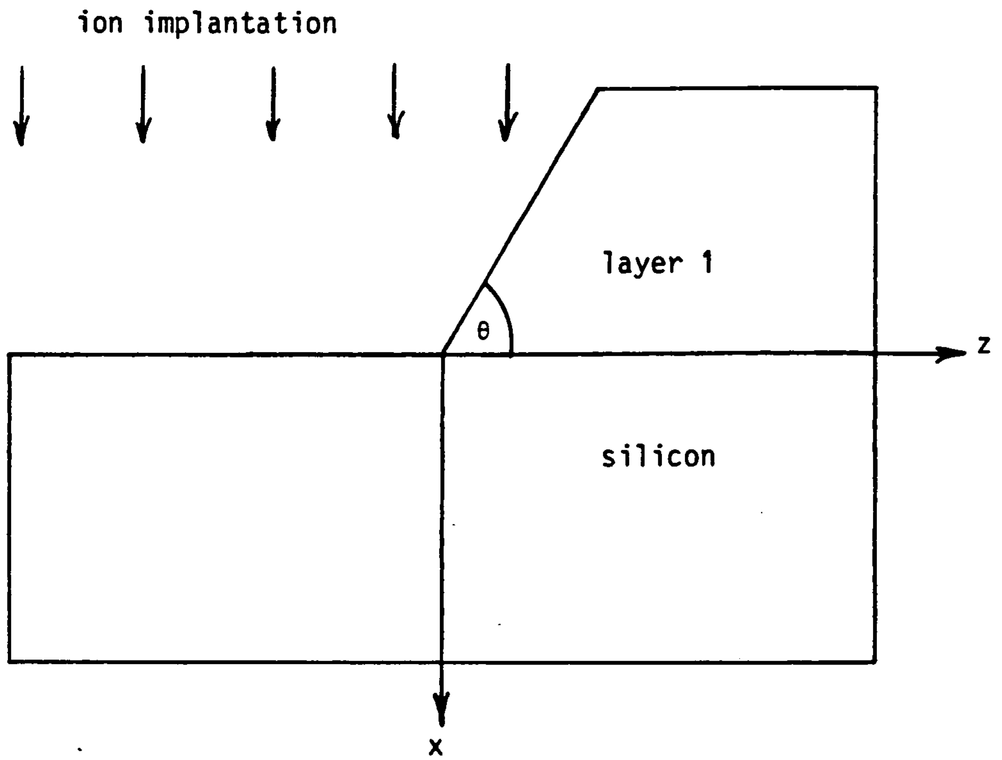


Figure 6.1 : Mask geometry considered by Lee and Dutton /15/.

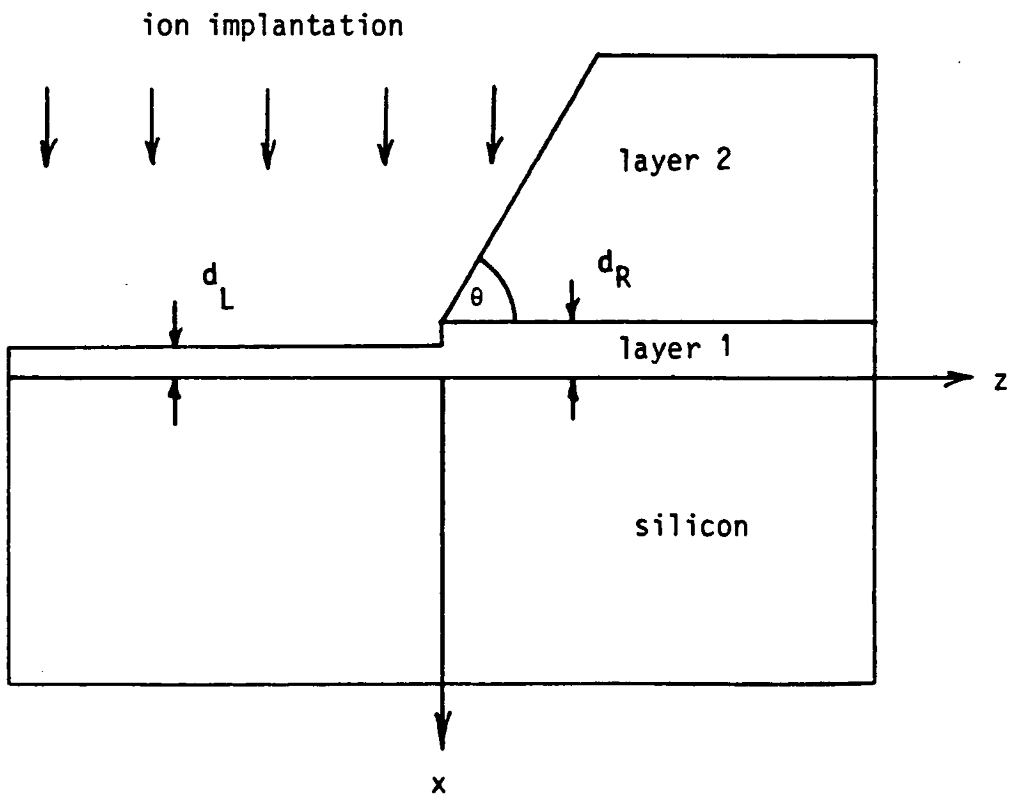


Figure 6.2 : Mask geometry considered by EPIC.

thickness is a linear function of the lateral distance z. The stopping power of the masking material is assumed to be the same as that for silicon. Figure 6.2 shows the structure accommodated by the new model implemented in EPIC. In a practical situation layers 1 and 2 could be silicon dioxide and silicon nitride respectively. This case arises at the field implantation step prior to field oxidation and is discussed in Chapter 8. In the example to follow, layer 1 is silicon dioxide and layer 2 is polysilicon which masks the active device region of the MOS transistor from the source/drain implant. The shape of the mask edge is important for VLSI devices since lateral extension of the dopant under the polysilicon gate influences the effective channel length of the MOS transistor. A different thickness of oxide is assumed on each half of the simulation area because when the material of layer 2 is etched to define the open regions, a small amount of layer 1 can be removed in the left half due to a non-infinite etch selectivity between the two materials. 'Over-etching' occurs because the etch time is usually extended to allow an adequate safety margin. Incomplete material removal in the open regions can have disastrous consequences for device operation.

6.1.2 Ion Implantation at a Non-Vertical Mask Edge

Following Furukawa et al /53/ the probability f that an ion impinging on a target at point (ξ,η,γ) will come to rest at a point

(x, y, z) is given by

$$f(x,y,z) = \frac{1}{(2\pi)^{3/2} \Delta R_p \Delta Y \Delta Z} \exp\left[-\frac{(x-\xi)^2}{2\Delta R_p^2} - \frac{(y-\eta)^2}{2\Delta Y^2} - \frac{(z-\gamma)^2}{2\Delta Z^2}\right] \quad (6.1)$$

where R_p is the projected range of the ion in silicon, ΔR_p is the projected standard deviation, and ΔY and ΔZ are the lateral standard deviations which are identical assuming isotropy. Furukawa et al /53/ assume a vertical mask edge, but Runge generalises the analysis to deal with arbitrarily shaped mask profiles /54/.

The oxide layer is converted to equivalent thicknesses of silicon in each side, d_L^* and d_R^* in the left and right halves respectively, according to

$$d_L^* = \frac{R_p}{R_{p1}} d_L \quad (6.2)$$

$$d_R^* = \frac{R_p}{R_{p1}} d_R \quad (6.3)$$

where R_{p1} is the projected range of the implanted ion in layer 1. Similarly the mask angle θ scales to an effective angle θ^* defined by

$$\alpha_m = \tan \theta^* = \frac{R_p}{R_{p2}} \tan \theta \quad (6.4)$$

where R_{p2} is the projected range in layer 2.

The surface of the effective layer of silicon d_m^* is therefore defined by

$$d_m^*(z) = \begin{cases} -d_L^* & ; \quad z < 0 \\ -d_R^* - \alpha_m z & ; \quad z \geqslant 0 \end{cases} \tag{6.5}$$

In the formulation due to Runge /54/ the implanted distribution at the point (x, y, z) is given by

$$I(x,y,z) = \frac{Q}{(2\pi)^{3/2}\,\Delta R_p\,\Delta Y \Delta Z} \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \delta(\xi - d_m^*(\gamma))$$

$$\cdot \exp\left[-\frac{(x-\xi-R_p)^2}{2\Delta R_p^2} - \frac{(y-\eta)^2}{2\Delta Y^2} - \frac{(z-\gamma)^2}{2\Delta Z^2}\right] d\xi\, d\eta\, d\gamma \tag{6.6}$$

where Q is the ion dose and δ is the Dirac delta function /55/. Equation (6.6) becomes

$$I(x,z) = \frac{I_{max}}{\sqrt{2\pi}\,\Delta Z} \int_{-\infty}^{\infty} \exp\left[-\frac{(x - d_m^*(\gamma) - R_p)^2}{2\Delta R_p^2} - \frac{(z-\gamma)^2}{2\,\Delta Z^2}\right] d\gamma \tag{6.7}$$

where

$$I_{max} = \frac{Q}{\sqrt{\frac{\pi}{2}}\,\Delta R_p\,\{1 + \mathrm{erf}\,(\frac{R_p}{\sqrt{2}\Delta R_p})\}} \tag{6.8}$$

which is the maximum concentration well to the left of the mask edge i.e. $z \ll 0$.

Evaluation of (6.7) gives the final implanted profile as

$$I(x,z) = I_L(x,z) + I_R(x,z) \tag{6.9}$$

where

$$I_L(x,z) = \frac{I_{max}}{2} \exp\left[-\frac{(x + d_L^* - R_p)^2}{2\,\Delta R_p^{\,2}}\right] \operatorname{erfc}\left[\frac{z}{\sqrt{2}\,\Delta Z}\right] \tag{6.10}$$

and

$$I_R(x,z) = \frac{\Delta R_p}{2\sqrt{D_o}} \exp\left[-\frac{(x + d_R^* + \alpha_m z - R_p)^2}{2D_o}\right] \cdot \left[1 + \operatorname{erf}\left[\frac{z\Delta R_p^{\,2} - \alpha_m(x + d_R^* - R_p)\Delta Z^2}{\Delta R_p\,\Delta Z\,\sqrt{2D_o}}\right]\right] \tag{6.11}$$

The constant D_o is given by

$$D_o = \Delta R_p^{\,2} + \alpha_m^{\,2}\,\Delta Z^2 \tag{6.12}$$

The reason for splitting the implanted distribution into two parts is that I_L corresponds to the ions due to a vertical mask edge and infinite mask thickness on the right side of the simulation domain, and I_R is the contribution due to the wedge-shaped part of the mask on the right side but with an infinite thickness of masking material in the left half. This becomes clear in the plots to follow.

Ion Implantation Parameters

element : boron

dose : $5 \times 10^{15} cm^{-3}$

energy : 70 keV

layer 1 material : silicon dioxide

$d_L = 200 Å$

$d_R = 300 Å$

layer 2 material : polysilicon

mask angle $\theta = 60°$

Diffusion Parameters

temperature $T = 1000°C$

diffusivity $D = 9.09 \times 10^{-5}$ μm^2 min^{-1}

time $t = 30$ mins

Table 6.1 : Ion Implantation and Diffusion Parameters

a	1×10^{13} cm^{-3}
b	1×10^{14} cm^{-3}
c	1×10^{15} cm^{-3}
d	1×10^{16} cm^{-3}
e	1×10^{17} cm^{-3}
f	1×10^{18} cm^{-3}
g	1×10^{19} cm^{-3}
h	2.5×10^{19} cm^{-3}
i	5×10^{19} cm^{-3}
j	7.5×10^{19} cm^{-3}
k	1×10^{20} cm^{-3}
l	1.25×10^{20} cm^{-3}
m	1.5×10^{20} cm^{-3}
n	1.75×10^{20} cm^{-3}
o	2×10^{20} cm^{-3}
p	2.25×10^{20} cm^{-3}
q	2.5×10^{20} cm^{-3}
r	2.75×10^{20} cm^{-3}
s	3×10^{20} cm^{-3}

Table 6.2 : Key to equidensity contour values for figures 6.3, 6.5, 6.7, 6.9, 6.11 and 6.13.

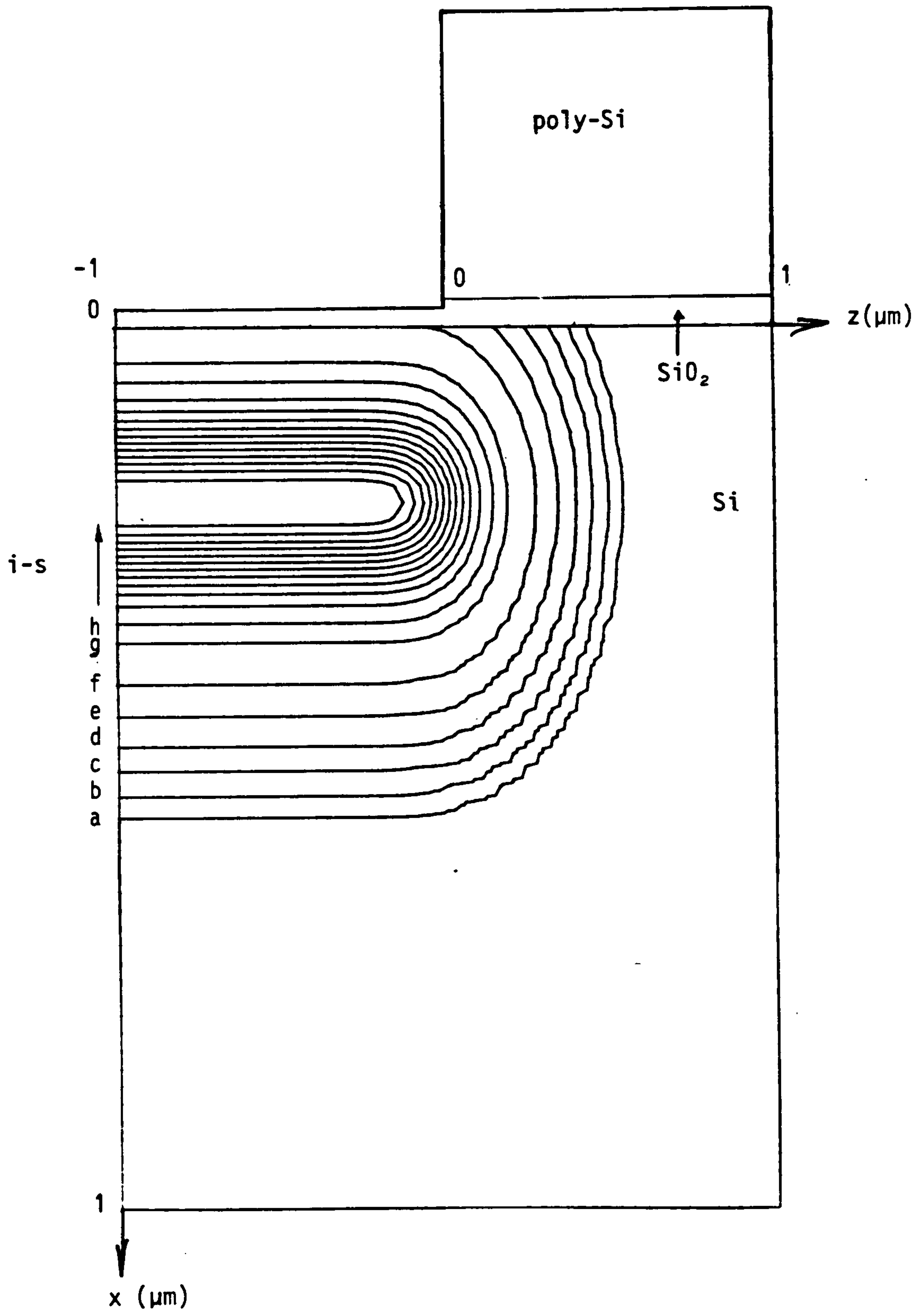


Figure 6.3 : Implanted profile $I_L(x,z)$ at vertical mask edge.

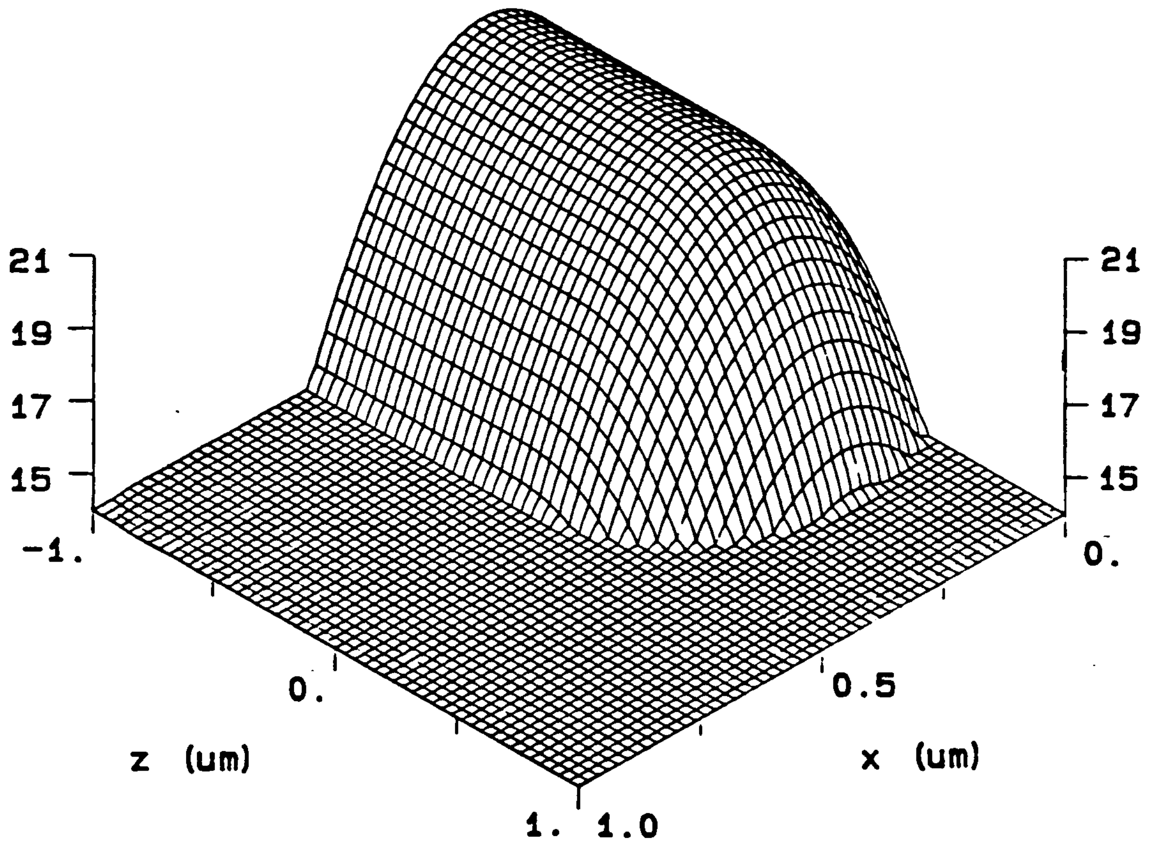


Figure 6.4 : Implanted profile $I_L(x,z)$ at vertical mask edge.

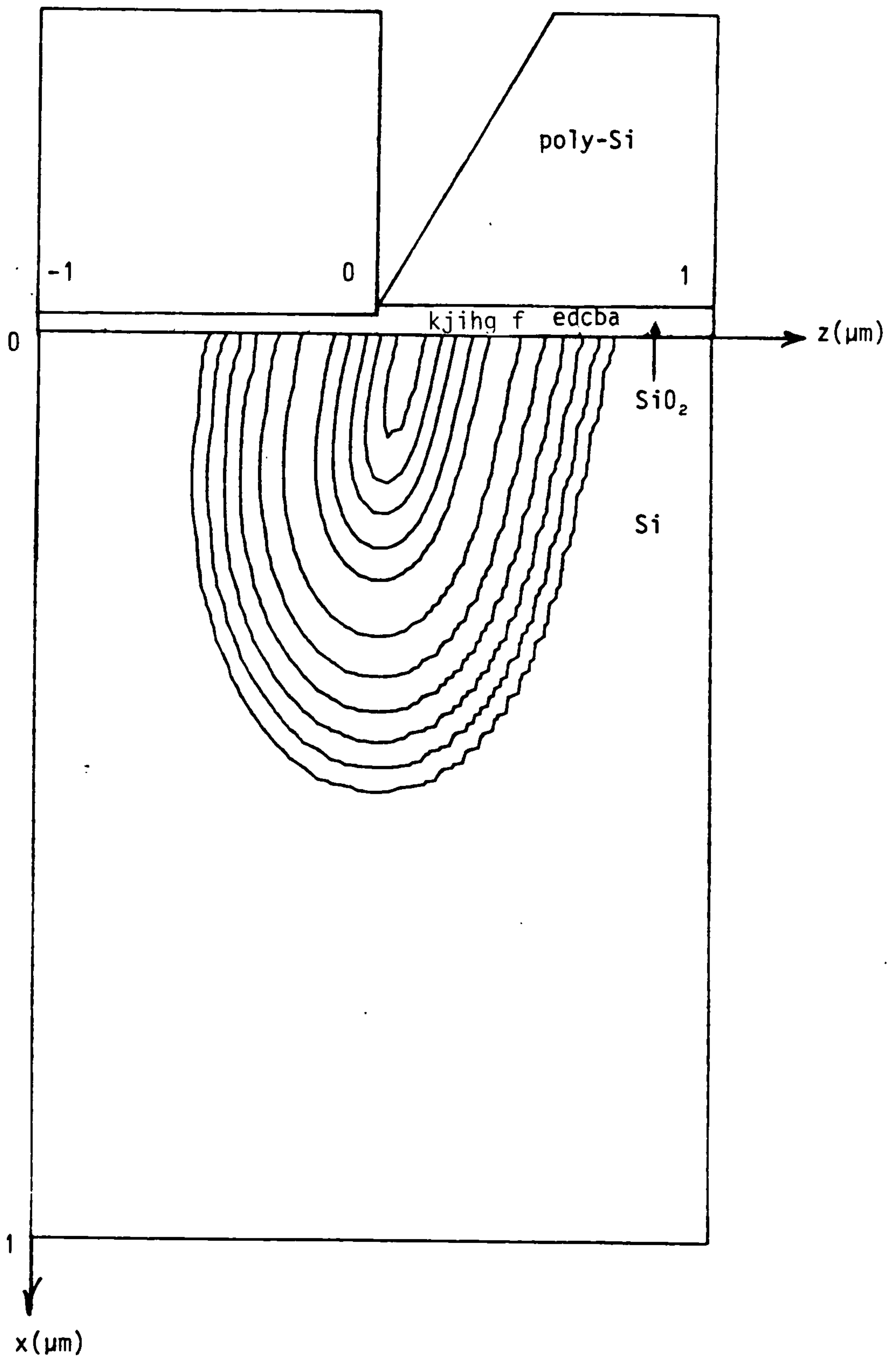


Figure 6.5 : Implanted profile $I_R(x,z)$ at wedge-shaped mask opening.

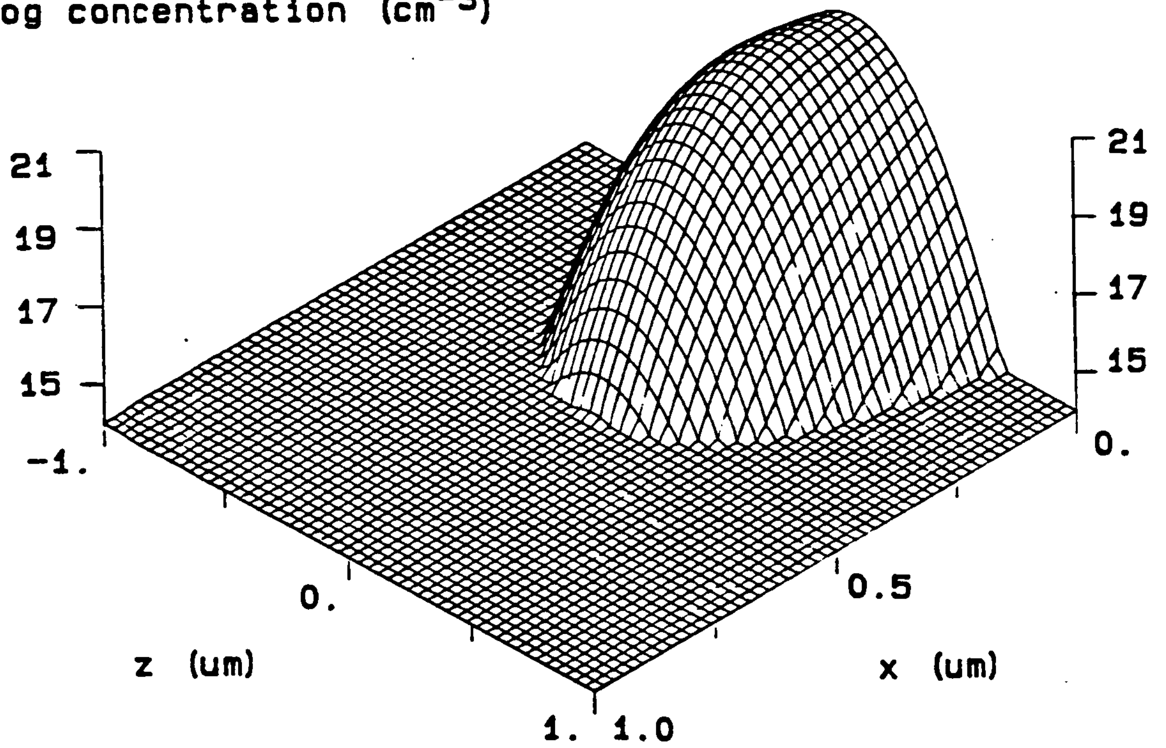


Figure 6.6: Implanted profile $I_R(x,z)$ at wedge-shaped mask opening.

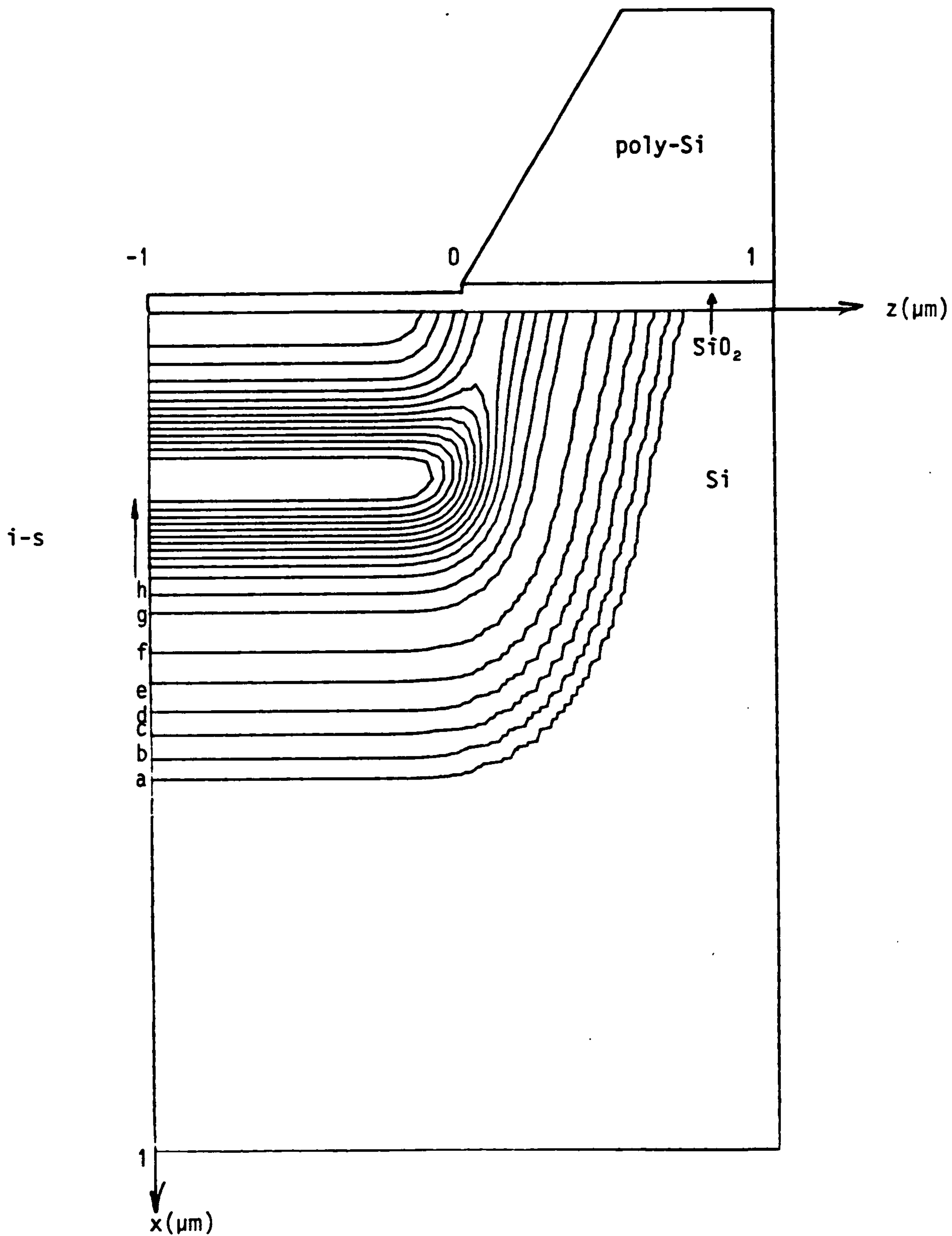


Figure 6.7 : Implanted profile I(x,z) at sloping mask edge.

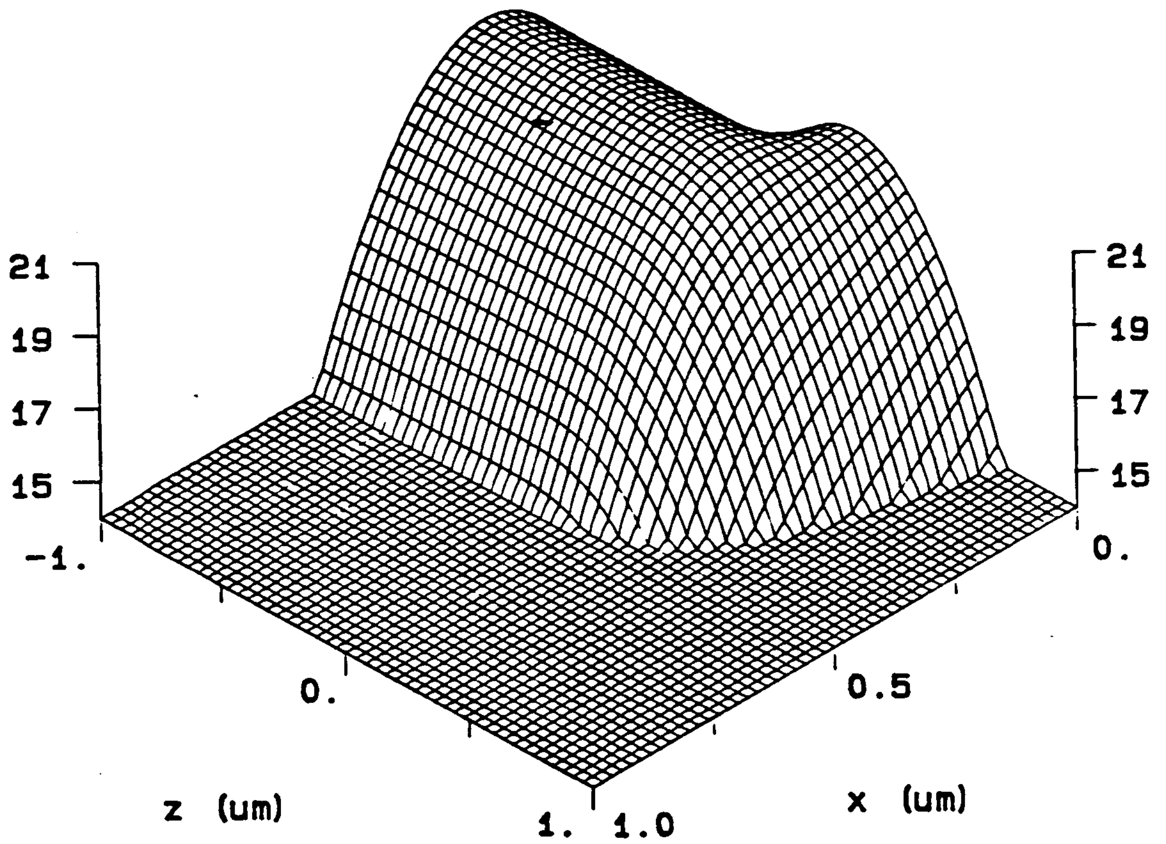


Figure 6.8 : Implanted profile I(x,z) at sloping mask edge.

An example of the effect of a sloping mask edge is now presented using the ion implantation parameters of table 6.1. Figure 6.3 shows a 2-D equidensity contour plot of the implanted profile I_L due to a vertical mask edge. The key to the contour values is shown in table 6.2. A surface plot of the same profile is shown in figure 6.4. The profile I_R due to the ions reaching the silicon through the wedge-shaped part of the mask is shown in figures 6.5 and 6.6. The total implanted profile I is given by the sum of the distributions in figures 6.3 and 6.5 and is shown in figures 6.7 and 6.8. On comparing figures 6.3 and 6.7, it is clear that the sloping mask edge allows the implanted ions to scatter further under the mask edge.

After the ions are implanted they are subjected to a high temperature anneal.

6.1.3 Diffusion Under a Non-Vertical Mask Edge

The redistribution of the implanted impurity profile due to diffusion at high temperature in a furnace tube is described by Fick's Law of diffusion in two dimensions i.e.

$$\frac{\partial N}{\partial t} = D\left(\frac{\partial^2 N}{\partial x^2} + \frac{\partial^2 N}{\partial z^2}\right) \qquad (6.13)$$

which is subject to a reflecting boundary at the silicon surface x = 0. The solution of (6.13) for a unit contribution of impurities at

the point (x',z') is

$$\Delta N = \frac{1}{4\pi Dt} [\exp \{- \frac{(x - x')^2}{4Dt}\} + \exp \{- \frac{(x + x')^2}{4Dt}\}] \cdot$$

$$\exp [- \frac{(z - z')^2}{4Dt}] \qquad (6.14)$$

which is the Green's function solution of this initial-boundary value problem. The implanted profile becomes the initial condition over which (6.14) is integrated to give the diffused profile N as

$$N(x,z,t) = \int_{x'=0}^{\infty} \int_{z'=-\infty}^{\infty} \Delta N \ (I_L + I_R) \, dx' \, dz' \qquad (6.15)$$

or

$$N(x,z,t) = N_L(x,z,t) + N_R(x,z,t) \qquad (6.16)$$

Hence N is composed of two components, N_L and N_R, which correspond to the independent diffusion of the implanted components I_L and I_R respectively. These are given by

$$N_L (x,z,t) = \frac{I_{max} \ \Delta R_p}{4 \sqrt{2Dt + \Delta R_p^2}} [\Omega(x,t) + \Omega(-x, t)].$$

$$\text{erfc} [\frac{z}{\sqrt{4Dt + 2\Delta Z^2}}] \qquad (6.17)$$

$$N_R(x,z,t) = \frac{I_{max}\,\Delta R_p}{4\sqrt{\pi D D_1 t}} \int_{x'=0}^{\infty} [\exp\{-\frac{(x-x')^2}{4Dt}\} + \exp\{-\frac{(x+x')^2}{4Dt}\}]$$

$$\cdot \exp\{-\frac{(\alpha_m z + x' + d_R^* - R_p)^2}{2D_1}\}\ \text{erfc}\{\frac{\alpha_m (x' + d_R^* - R_p)D_2 - zD_0}{\sqrt{2\,D_0 D_1 D_2}}\}\ dx'$$

(6.18)

where

$$\Omega(x,t) = \exp\{-\frac{(x + d_L^* - R_p)^2}{4Dt\,(1+r)}\} \quad [1 + \text{erf}\{\frac{R_p - d_L^* + r\,x}{\sqrt{2(1+r)}\,\Delta R_p}\}] \quad (6.19)$$

$$r = \frac{\Delta R_p^{\,2}}{2Dt} \quad (6.20)$$

$$D_1 = D_0 + 2\alpha_m^{\,2} Dt \quad (6.21)$$

$$D_2 = 2Dt + D_1 \frac{\Delta Z^2}{\Delta R_p^{\,2}} \quad (6.22)$$

In the paper due to Lee and Dutton /15/, equation 9 is incorrect and should be replaced by (6.18) above. The integral in equation (6.18) is evaluated using Simpson's rule /78/ in EPIC. An example of diffusion using this model is presented using the parameters of table 6.1. Figures 6.9 and 6.10 show a contour plot and surface plot of the profile N_L due to a vertical mask edge. Figures 6.11 and 6.12 show the profile N_R due to a wedge-shaped mask and figures 6.13 and 6.14 depict the final diffused profile N obtained by summing the distributions of figures 6.9 and 6.11. The lateral extension of the profile under the mask edge is greater in figure 6.13 for a sloping mask edge compared to figure 6.9 for a vertical mask edge. Because the shape of the mask influences the lateral distribution of

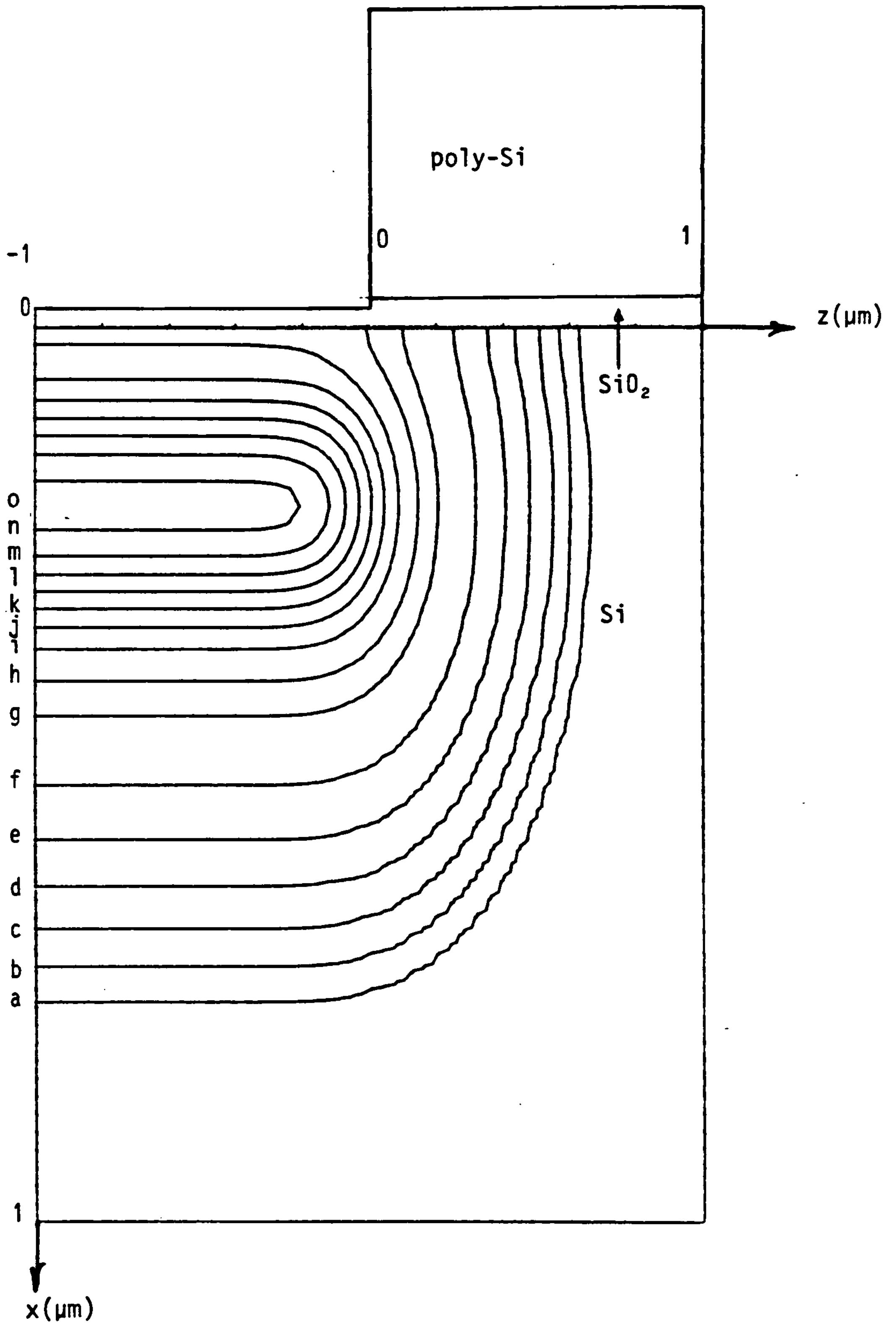


Figure 6.9 : Diffused profile $N_L(x,z)$ at vertical mask edge.

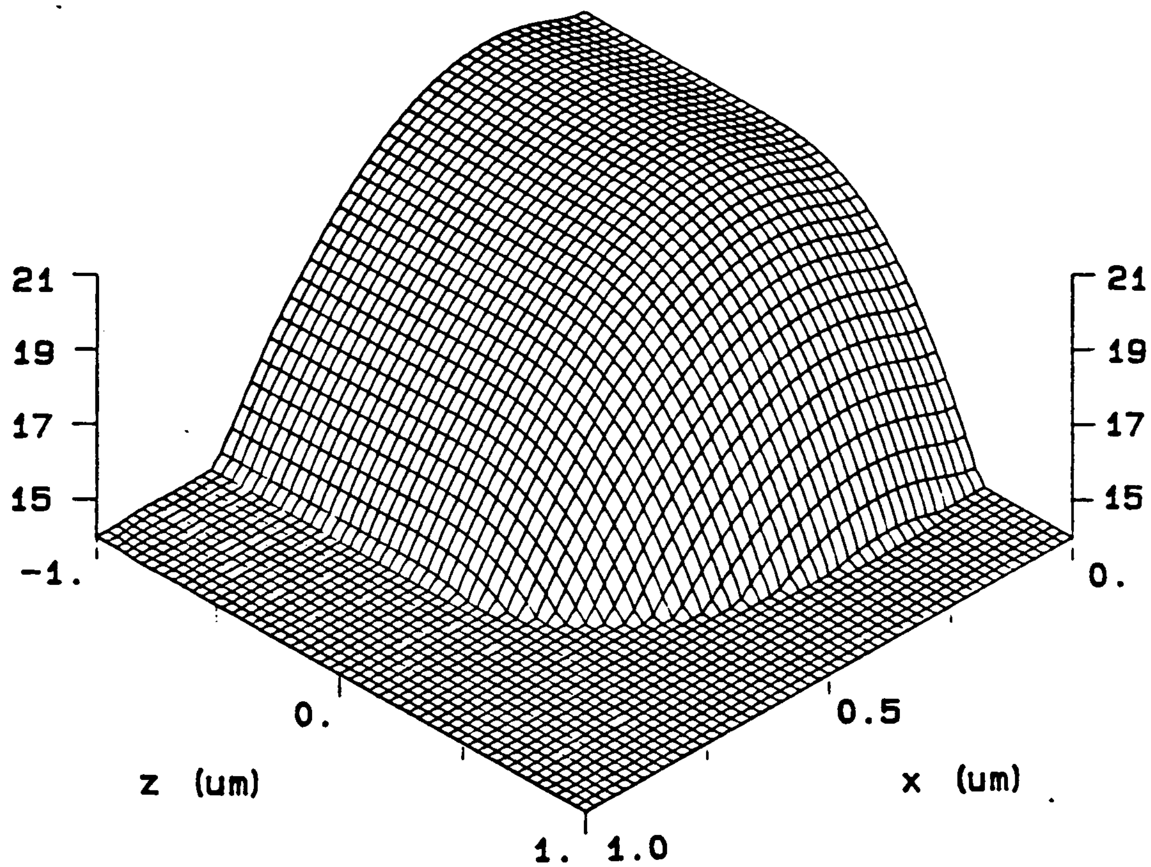


Figure 6.10 : Diffused profile $N_L(x,z)$ at vertical mask edge.

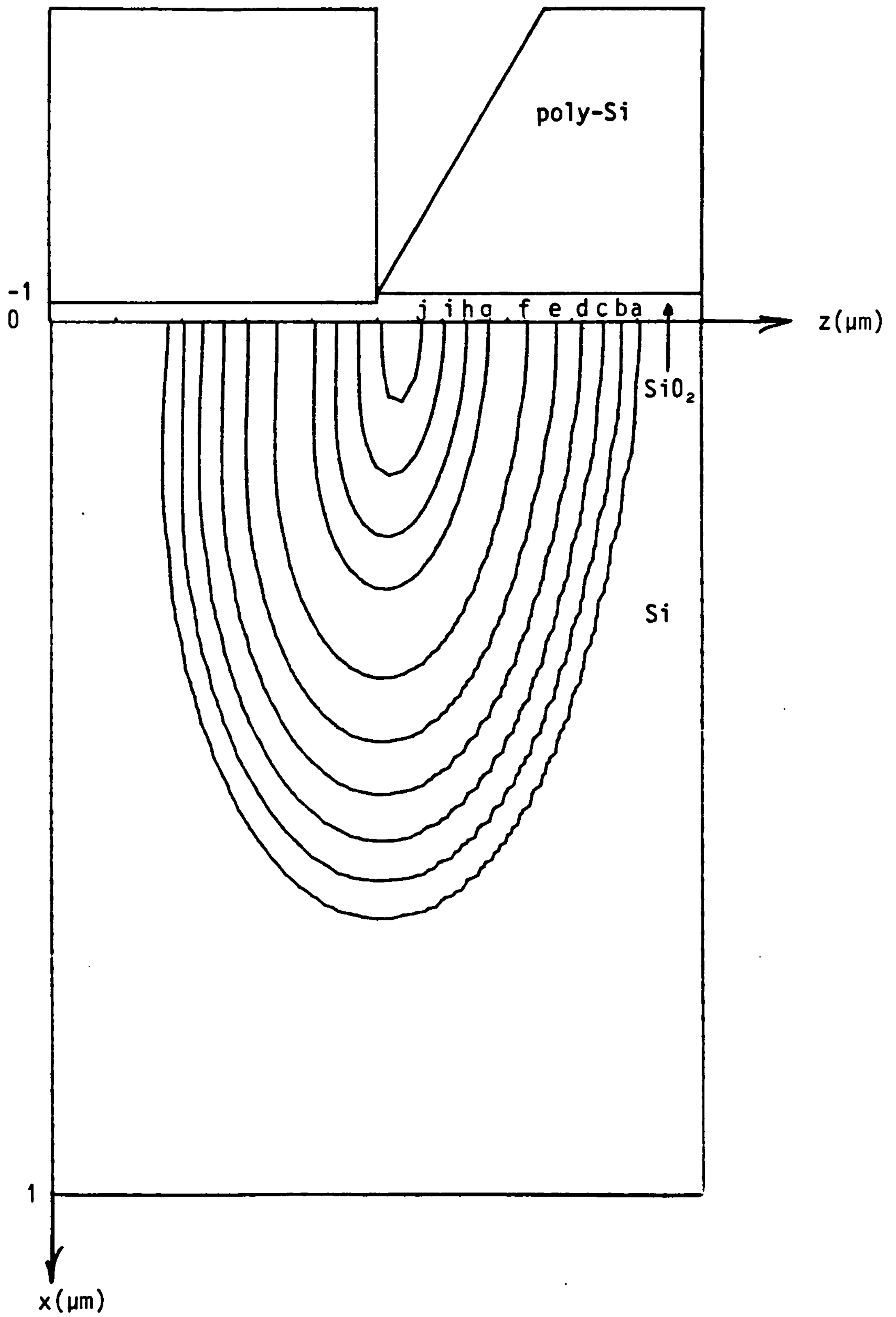


Figure 6.11 : Diffused profile $N_R(x,z)$ at wedge-shaped mask opening.

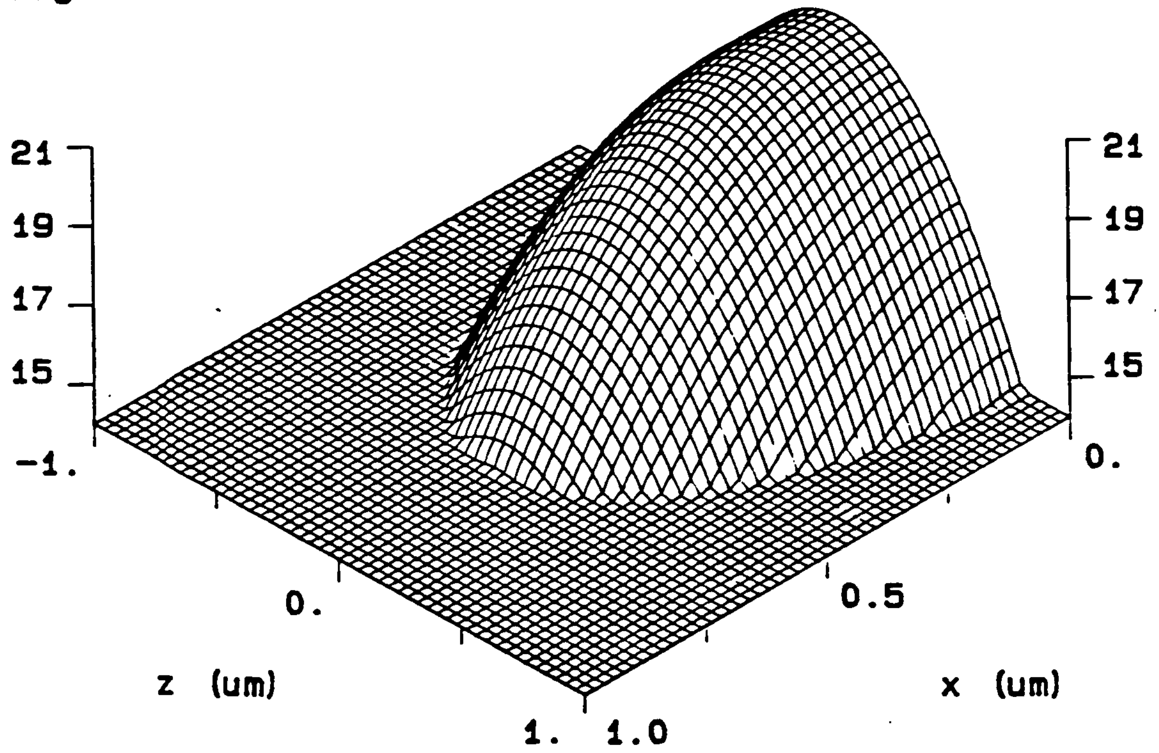


Figure 6.12 : Diffused profile $N_R(x,z)$ at wedge-shaped mask opening.

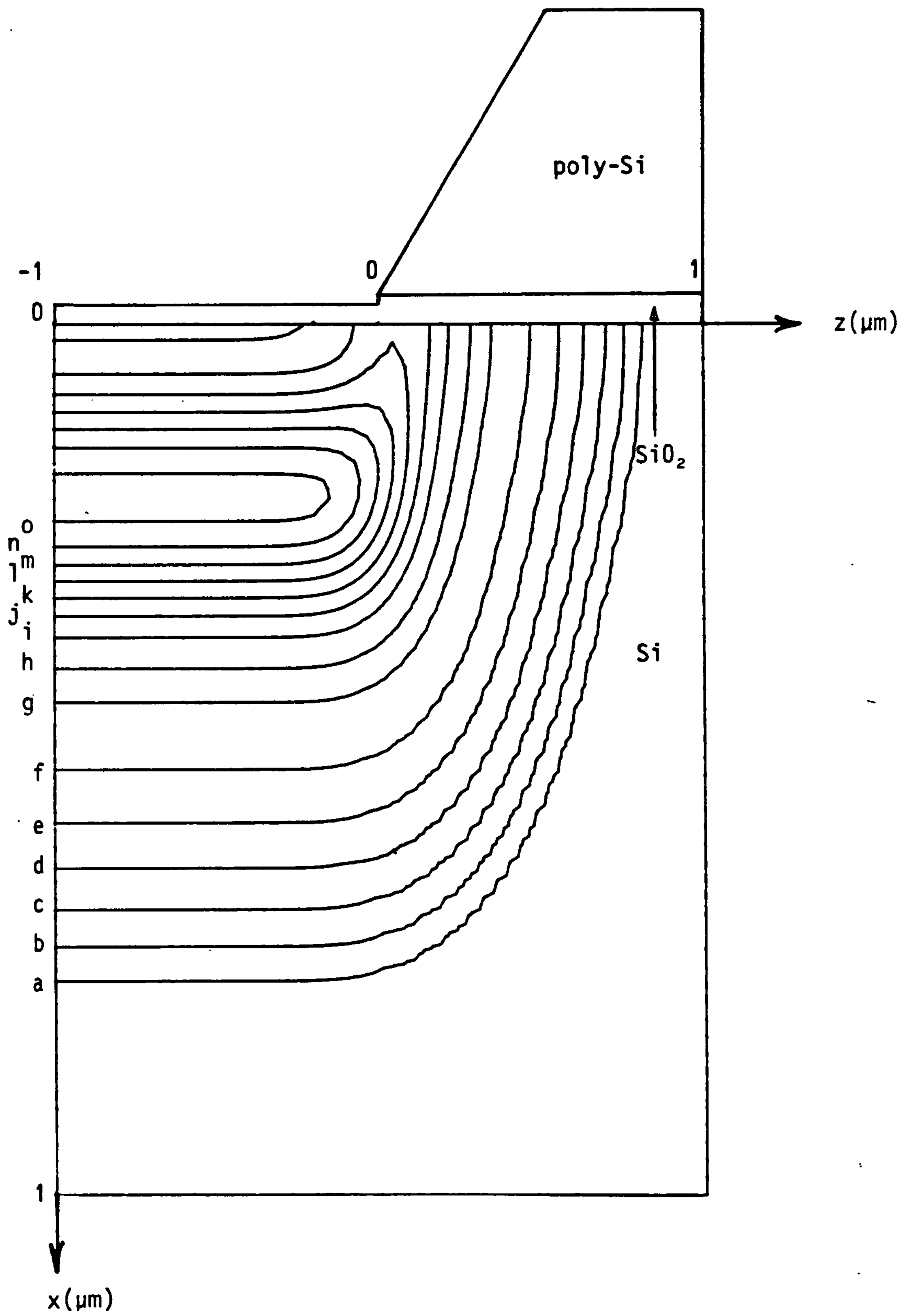


Figure 6.13 : Diffused profile N(x,z) at sloping mask edge.

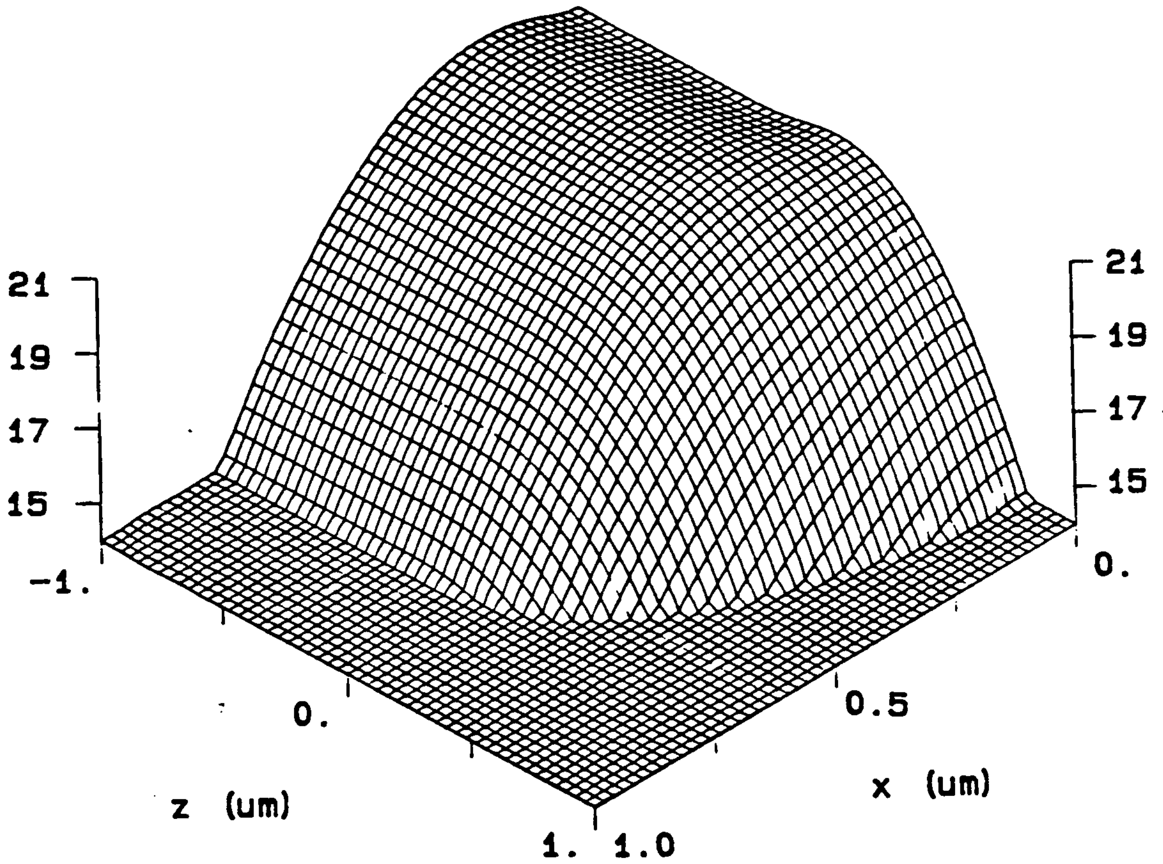


Figure 6.14 : Diffused profile N(x,z) at sloping mask edge.

dopants, a greater degree of control is required on photolithographic and etching stages in VLSI fabrication processes.

6.1.4 2-D Nature of a Diffused P-Well

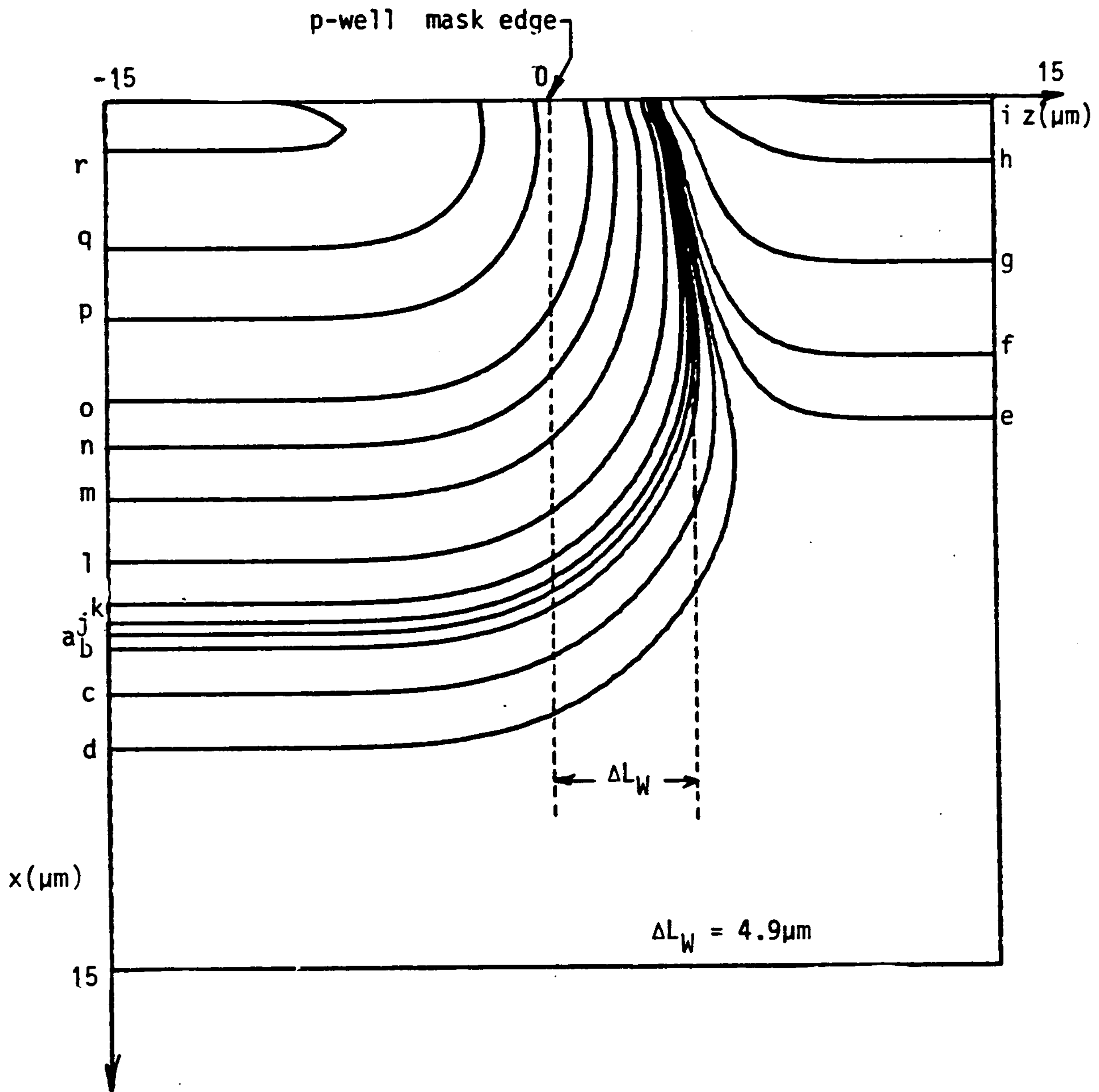
One aspect of present day bulk CMOS technology which is wasteful of wafer area is the lateral diffusion of the p-well. It is important to determine the offset ΔL_W between the mask edge and the final position of the p-n junction between the p-well and the n-substrate. Knowledge of ΔL_W aids estimation of important design rules for a CMOS process, for example, the minimum spacing between NMOS and PMOS transistors. Each transistor must be placed far enough away from the p-n junction to avoid a reduction in the modulus of the threshold voltage caused by the compensating effect of the boron and phosphorus dopants in this region of the wafer. In VLSI processes a larger minimum separation of NMOS and PMOS devices may be appropriate to avoid the parasitic bipolar action known as 'latch-up' /65-68/.

If the segregation effects of the boron at the surface of the silicon wafer are neglected, the analytical model of this chapter can be applied to determine the parameter ΔL_W. The n-substrate region is modelled using the SUPREM results of figure 4.21 since no variation of phosphorus concentration exists in the lateral directions. To this profile, EPIC adds the 2-D boron distribution constituting a p-well using the process parameters of Table 6.3.

implant	element : boron
	dose Q : 1.8×10^{13} cm^{-2}
	energy E : 60 keV
drive-in	temperature T : 1200°C
	time t : 725 mins
	ambient : inert

Table 6.3 : Process parameters for p-well formation

Subsequent process steps use short times and/or low temperatures compared to the p-well drive-in stage, and so give rise to a negligible amount of impurity redistribution in the bulk. Figures 6.15 and 6.16 show contour and surface representations of the net impurity profile. The parameter characteristic of the lateral extension of the p-well is found to be ΔL_W = 4.9 micron, and should be accounted for in the 'sizing' procedure prior to maskmaking. It is interesting to note from figure 6.15 that the lateral extension of the p-well in the bulk is greater than that at the silicon surface. This is caused by the increase in phosphorus concentration towards the surface of the wafer.



a	p-n junction
b	$1 \times 10^{14}\ cm^{-3}$(n)
c	$3 \times 10^{14}\ cm^{-3}$(n)
d	$4 \times 10^{14}\ cm^{-3}$(n)
e	$6 \times 10^{14}\ cm^{-3}$(n)
f	$9 \times 10^{14}\ cm^{-3}$(n)
g	$2 \times 10^{15}\ cm^{-3}$(n)
h	$4 \times 10^{15}\ cm^{-3}$(n)
i	$6 \times 10^{15}\ cm^{-3}$(n)
j	$1 \times 10^{14}\ cm^{-3}$ (p)
k	$3 \times 10^{14}\ cm^{-3}$ (p)
l	$1 \times 10^{15}\ cm^{-3}$ (p)
m	$3 \times 10^{15}\ cm^{-3}$ (p)
n	$6 \times 10^{15}\ cm^{-3}$ (p)
o	$1 \times 10^{16}\ cm^{-3}$ (p)
p	$2 \times 10^{16}\ cm^{-3}$ (p)
q	$3 \times 10^{16}\ cm^{-3}$ (p)
r	$4 \times 10^{16}\ cm^{-3}$ (p)

Figure 6.15 : 2-D simulation of p-well diffusion.

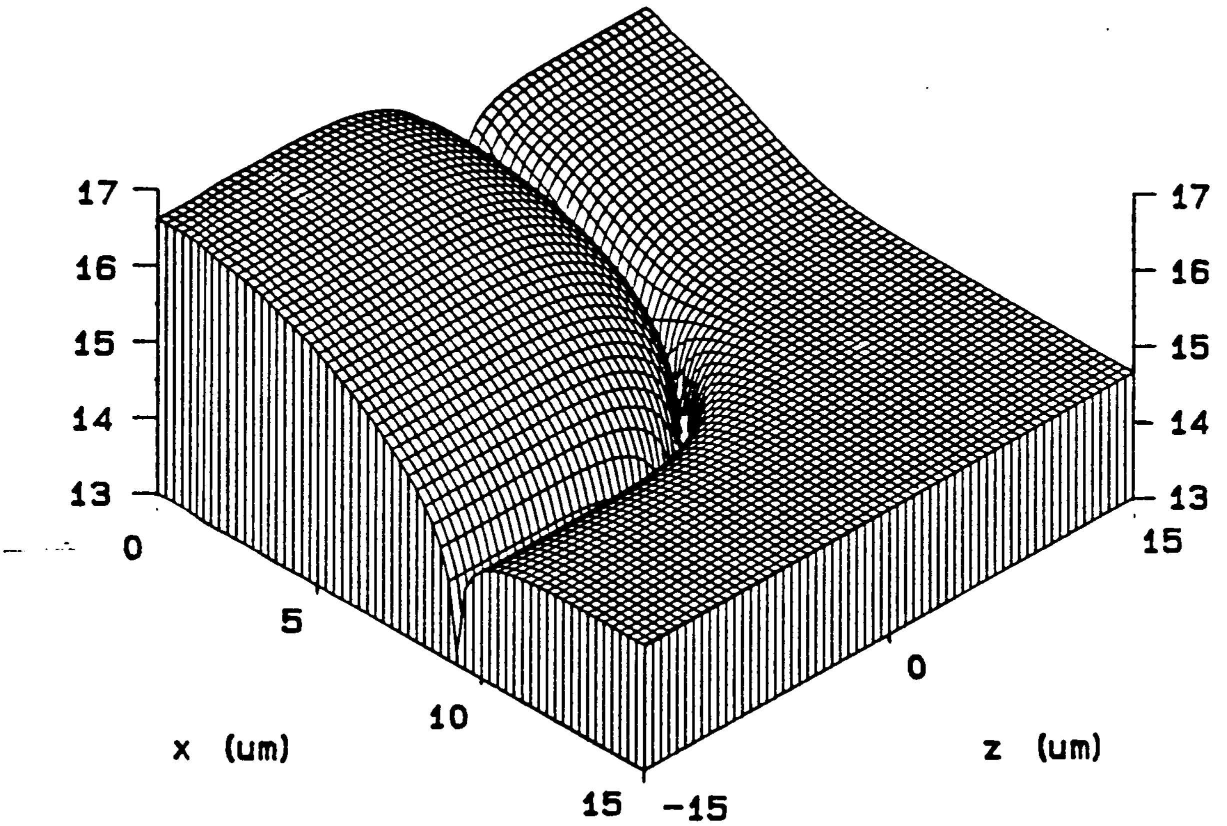


Figure 6.16 : 2-D simulation of p-well simulation

6.2 TEMPERATURE MODELLING FOR TRANSIENT ANNEALING

6.2.1 Uses of Transient Annealing in MOS Processing

Research activity into the transient annealing of silicon has increased markedly in recent years because heat sources such as lasers, electron beams and arc discharge lamps offer several advantages over conventional high temperature furnace treatments /60, 62/. The source/drain regions of MOS wafers receive high dose implants of the order of 10^{16} ions per cm^2. The implanted ions cause considerable lattice damage in the surface of the silicon wafer, and consequently some form of heat treatment is required to repair the disorder and activate the implanted species. Furnace annealing causes significant redistribution of impurity species at high temperature, as has already been discussed in Chapter 4. High p-n junction depths in MOS devices give rise to short channel effects /69-71/, and lateral diffusion under the polysilicon gate reduces the effective channel length and increases parasitic gate/drain and gate/source capacitance.

Transient annealing, however, offers reduced impurity redistribution after ion implantation, a high degree of impurity activation, and low contact resistances /73/. The fraction of dopants which can take up substitutional sites in the silicon lattice is not limited by the solid solubility limit occurring in conventional furnace operations /60, 62/. In addition electron beams can be used to recrystallise and improve conductivity of polycrystalline films /62,

77/ or form refractory metal silicides /72/. Since the properties of a semiconducting material are critically dependent on the temperature of the anneal, it is important to model heat transport and hence optimise annealing parameters as shown by Buttar et al /76/.

6.2.2 Review of Temperature Models for Electron-Beam Annealing

Energy is coupled from the electrons of the beam to the silicon lattice by way of either nuclear or electronic collisions /61/. Nuclear collisions are essentially elastic and merely change the direction of the electron. Electronic collisions are inelastic and gradually slow down the beam electrons due to the absorption of energy for both static excitations and secondary electrons. In addition, a proportion of the electrons are backscattered /61/. Monte Carlo studies of electron paths in the silicon indicate that energy equidensity surfaces form tear-drop shapes /64/. In a practical situation, beam energies must be kept below about 30 keV to avoid damage in material layers, eg. silicon dioxide, below the one to be annealed /73/. In this case, most of the beam energy is deposited within the first micron of silicon at the wafer surface /64/. Existing temperature models /63, 64/ assume that all the beam energy is deposited at the surface, and, since both the number and energy of backscattered electrons, and also radiation losses are difficult to model quantitatively /61/, all the energy impinging on the silicon is assumed to remain there. The thermal diffusivity of silicon is found to vary with temperature /59/, but is approximated by a

constant to simplify the analysis. In using these approximations, analytical temperature models provide an initial estimate for the annealing parameters, such as beam energy, radius, scan speed, etc. required to achieve a given temperature at the front surface of a bare silicon wafer.

Pittaway /63/ treats the case of a Gaussian electron beam scanning across a thin foil and a semi-infinite target. Neukermans and Superstein /64/ extend this model to include volume heating effects for a stationary Gaussian beam impinging on a silicon slice of finite thickness. Buttar et al /76/ extend the analysis to the case of a scanning electron beam as described below, and the model is used to determine scan pitch for a practical electron-beam annealing system /77/.

6.2.3 Temperature Model for a Scanning Electron-Beam

As in the case of impurity diffusion, heat transport is described by Fick's Law in the form

$$\frac{\partial T}{\partial t} = \alpha \nabla^2 T \qquad (6.23)$$

where T is temperature, t is time and α is the thermal diffusivity, taken to be 1.37×10^{-5} m^2 s^{-1} which is appropriate for a temperature of 1000^oC /59/.

The distribution of power E in a beam of total power E_0 and radius (standard deviation) s_0 as a function of radial distance s from the centre of the beam is given by

$$E(s) = F_0 \exp(-\frac{s^2}{s_0^2}) \qquad (6.24)$$

where

$$F_0 = \frac{E_0}{\pi s_0^2} \qquad (6.25)$$

Extending the work of Pittaway /63/ and Neukermans and Saperstein /64/, the temperature rise induced in the silicon by a scanning beam is

$$\Delta T(x,y,z;t_1, t_2) = \frac{F_0 s_0^2}{K} \left(\frac{\alpha}{\pi}\right)^{1/2} \int_{t=0}^{t_1} \frac{dt}{(t_2 - t)^{1/2} \{s_0^2 + 4\alpha(t_2 - t)\}} \cdot$$

$$\left[\exp\left\{-\frac{x^2}{4\alpha(t_2 - t)}\right\} + \exp\left\{-\frac{(x - 2d)^2}{4\alpha(t_2 - t)}\right\}\right] \exp\left\{-\frac{(y - vt_2)^2 + z^2}{s_0^2 + 4\alpha(t_2 - t)}\right\} ;$$

$$0 \leqslant x \leqslant d, \ -\infty \leqslant y \leqslant \infty, -\infty \leqslant z \leqslant \infty; \ t_1 \geqslant 0, \ t_2 \geqslant t_1 \qquad (6.26)$$

The co-ordinate system is defined in figure 6.17, where x, y and z refer to position in a wafer of thickness d and infinite extent in the y and z-directions. The beam heats the wafer from time t = 0 to $t = t_1$, and is scanned in the y-direction with speed v. The beam is turned off at $t = t_1$ and the silicon is allowed to cool until $t = t_2$. When no cooling occurs ie $t_2 = t_1$, the integral of (6.26) is

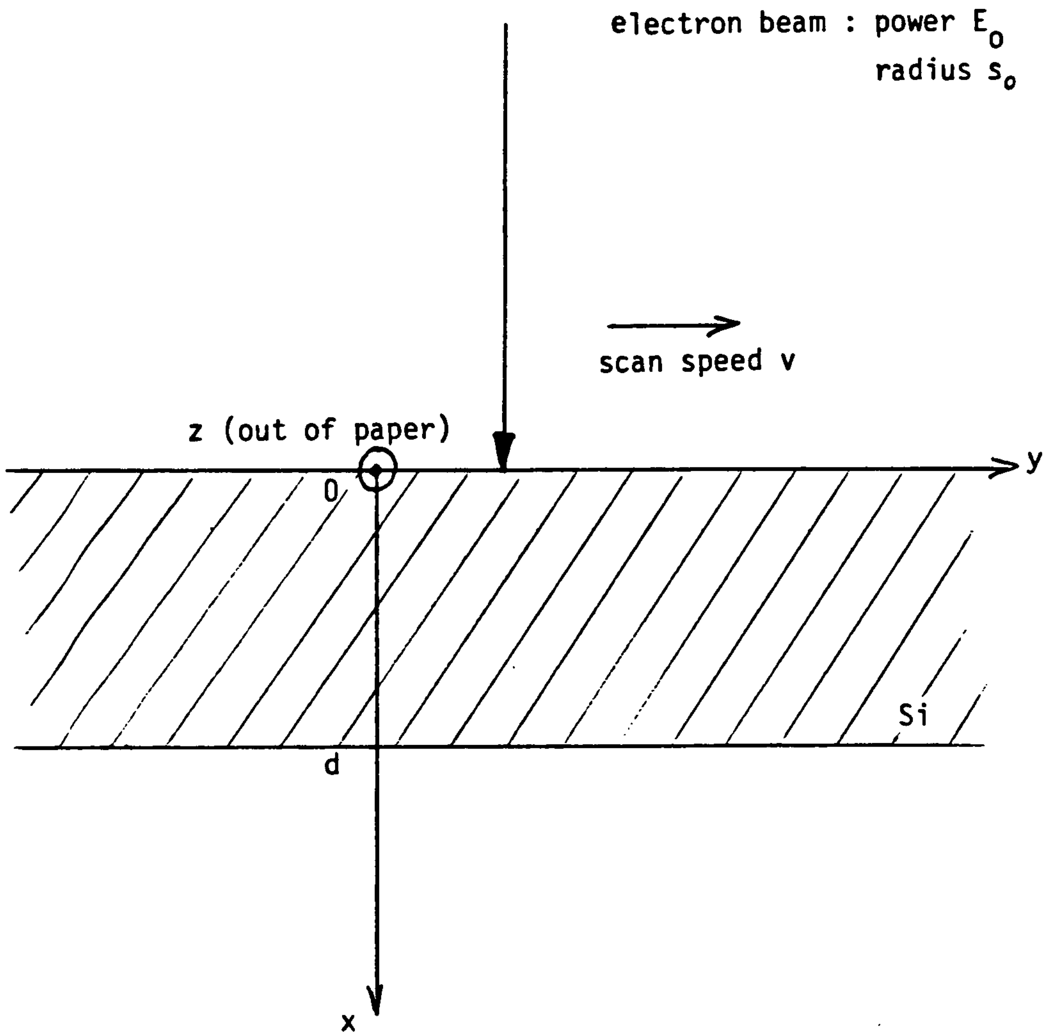


Figure 6.17 : Co-ordinate system for temperature modelling during electron-beam anneal.

'improper' /78/ and requires the change of variable

$$\gamma = (t_2 - t)^{1/2} \tag{6.27}$$

to allow the use of Simpson's rule on the result (6.28).

$$\Delta T(x,y,z;t_1, t) = \frac{2F_o s_o^2}{K} \left(\frac{\alpha}{\pi}\right)^{1/2} \int_{(t_2-t_1)^{1/2}}^{t_2^{1/2}} \frac{d\gamma}{(s_o^2 + 4\alpha\gamma^2)} \cdot$$

$$\left[\exp\left\{-\frac{x^2}{4\alpha\gamma^2}\right\} + \exp\left\{-\frac{(x-2d)^2}{4\alpha\gamma^2}\right\}\right] \exp\left[-\frac{\{y - v(t_2 - \gamma^2)\}^2 + z^2}{s_o^2 + 4\alpha\gamma^2}\right] ;$$

$$0 < x < d, \ -\infty < y \leq \infty, \ -\infty \leq z < \infty; \ t_1 \geq 0, \ t_2 \geq t_1 \tag{6.28}$$

This model neglects residual heating effects due to previous scans.

6.2.4 Application to Determine Scan Pitch

In a practical annealing system /77/, it is useful to know the approximate positions for the controls before the beam is applied to the sample.

Knowledge of the peak temperature and also the lateral extent of the temperature distribution at the silicon surface is required to ensure a uniform anneal in a raster scan system. A general model

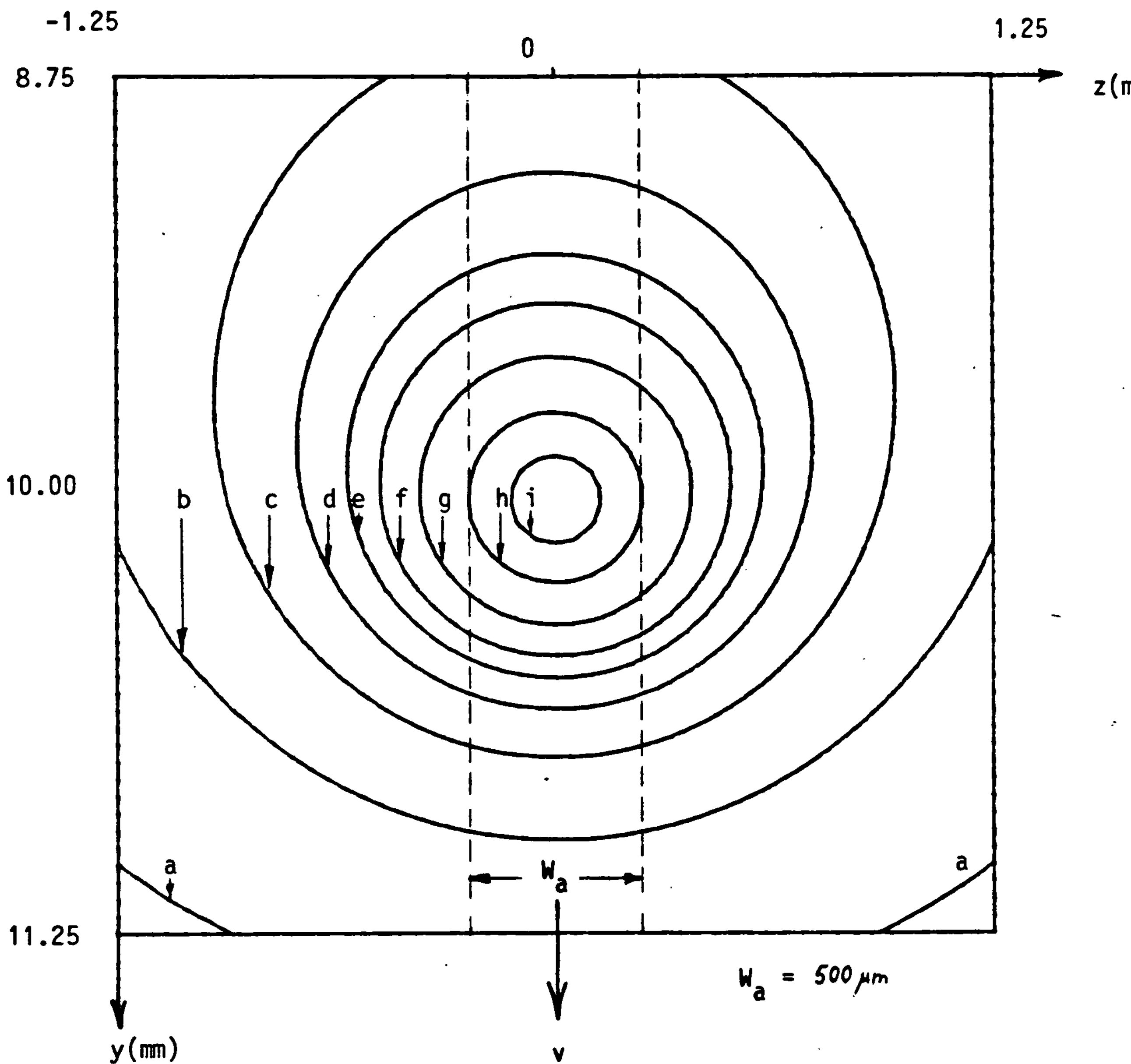
for activation of impurity species during a non-equilibrium transient heat treatment has never been formulated. A simple criterion is therefore adopted whereby all points in the silicon which attain a temperature of $1000^{o}C$ or greater are assumed to be annealed. As an example, table 6.4 shows a set of typical scanning electron-beam parameters /76/.

wafer thickness	$d = 500\ \mu m$
beam energy	$E_o = 23W$
beam radius	$s_o = 250\mu m$
scan speed	$v = 1\ cm\ s^{-1}$
chuck temperature	$T_c = 400^{o}C$

Table 6.4 Typical scanning electron-beam parameters.

The wafer is held on a heated chuck and is assumed to be at a uniform temperature T_c before the anneal begins. Figures 6.18 and 6.19 show contour and surface plots respectively of the temperature T at the surface of the wafer after time t = 1s, when steady state conditions have been reached with respect to the frame of reference of the beam. Using the anneal criterion defined above, a strip of width $W_a = 500\ \mu m$ is annealed. To ensure uniformity of the anneal, a scan pitch, or distance between adjacent scans, of less than W_a must be used.

The local heating effect at the beam centre relaxes quickly when the beam is turned off. Figures 6.20 and 6.21 show plots of



a	450°C	f	700°C
b	500°C	g	800°C
c	550°C	h	1000°C
d	600°C	i	1200°C
e	650°C		

Figure 6.18 : Temperature distribution at the surface of the wafer during a transient anneal.

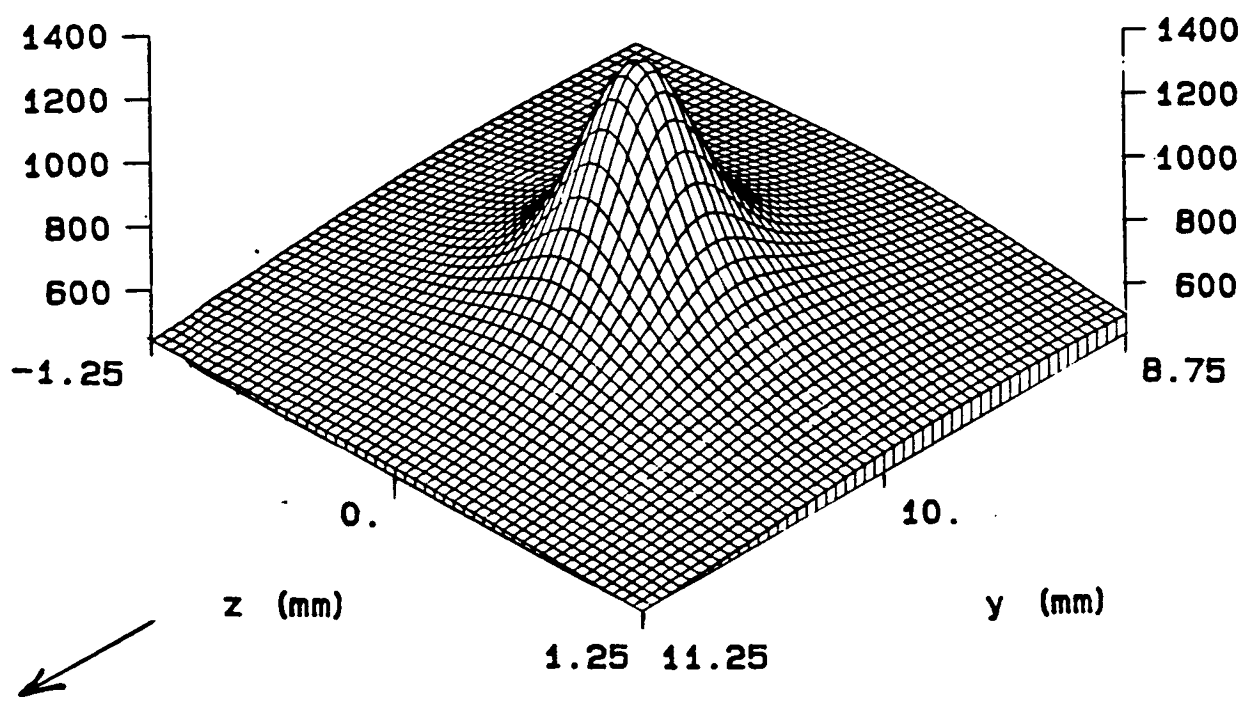
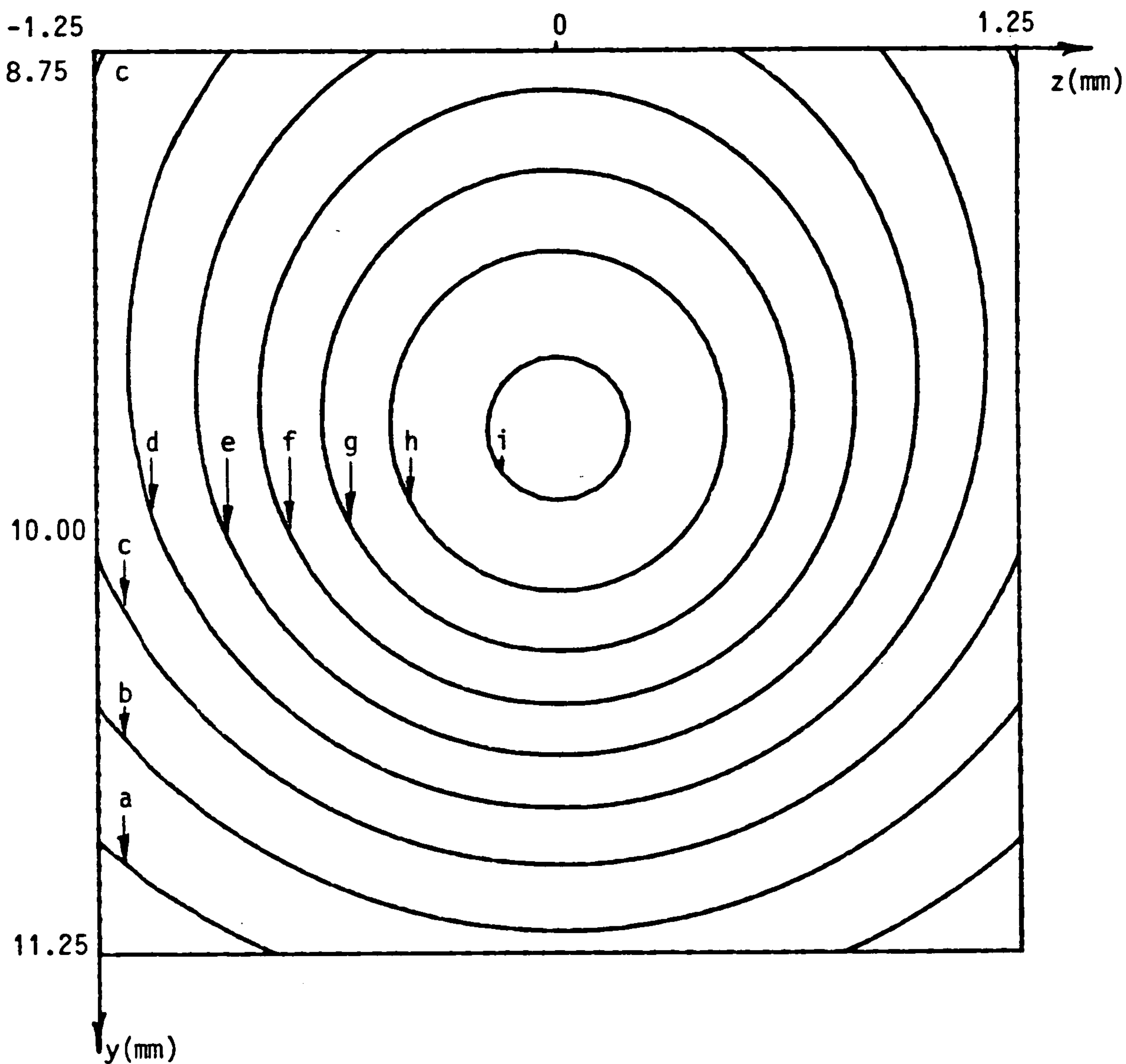


Figure 6.19 : Temperature distribution at the surface of the wafer during a transient anneal.



a	460°C	f	560°C
b	480°C	g	580°C
c	500°C	h	600°C
d	520°C	i	620°C
e	540°C		

Figure 6.20 : Temperature distribution at the surface of the wafer 10 ms after beam turned off

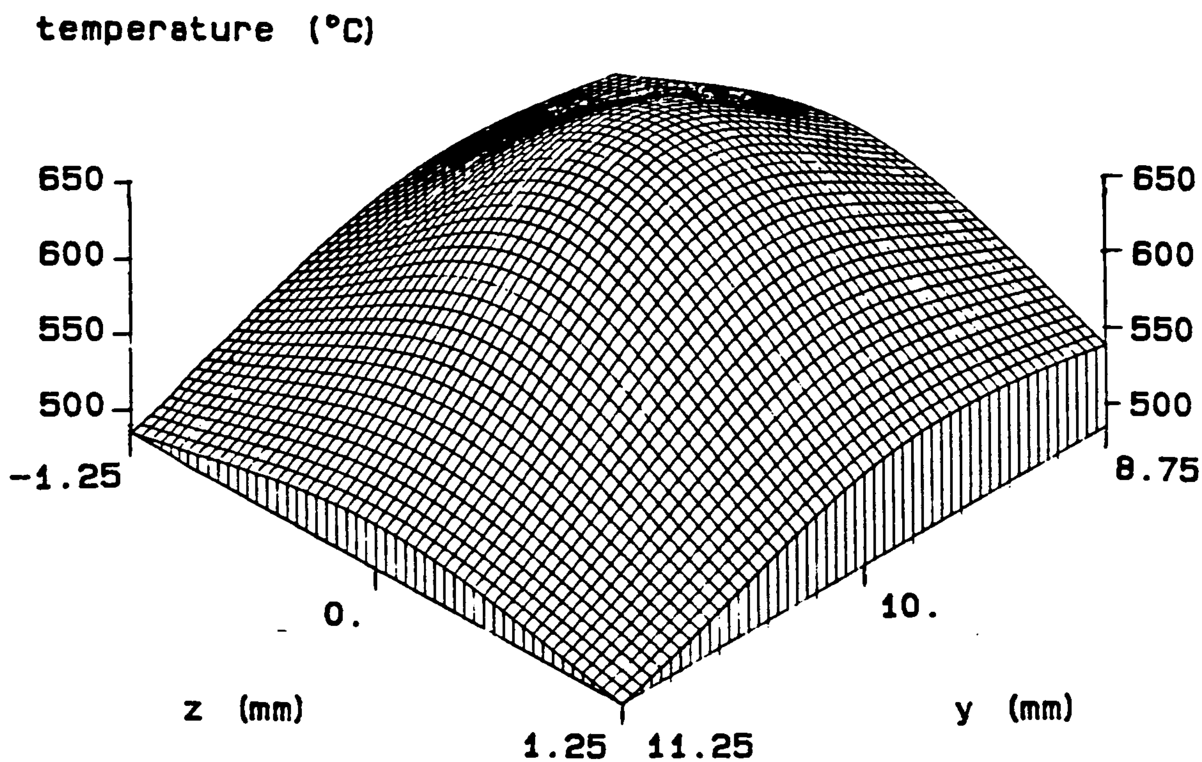


Figure 6.21 : Temperature distribution at the surface of the wafer 10 ms after beam turned off.

the temperature distribution at the wafer surface after a cooling time of 10 ms ie t_1 = 1s and t_2 = 1.01s. In this short time, the peak temperature drops by more than 600°C.

Despite the use of many simplifying approximations, this temperature model determines the 3-D temperature distribution in silicon at least qualitatively, and is a useful tool for the development of experimental electron-beam annealing systems /76,77/.

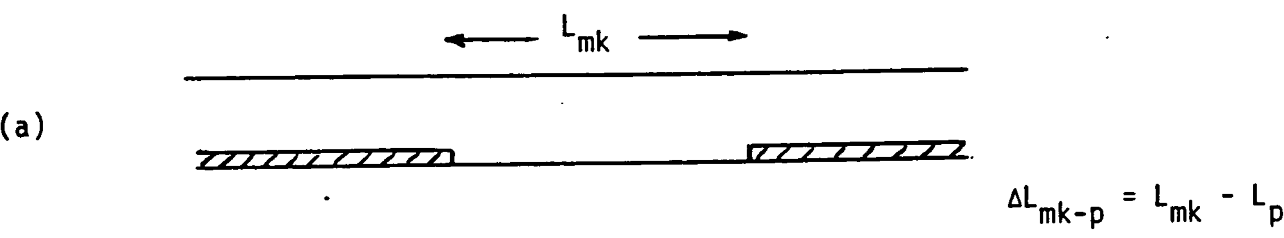
CHAPTER SEVEN : 2-D SIMULATION OF HIGH CONCENTRATION PROFILES

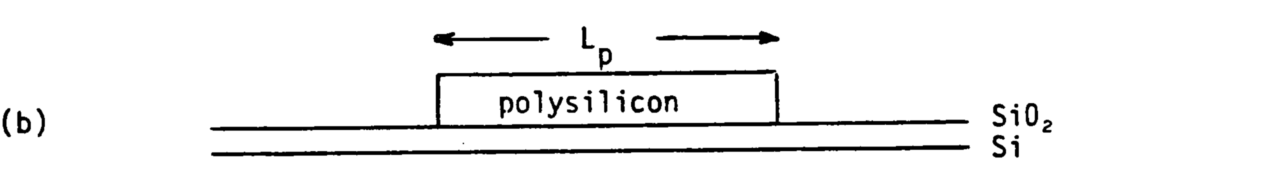
7.1 OFFSETS WHICH INFLUENCE EFFECTIVE CHANNEL LENGTH

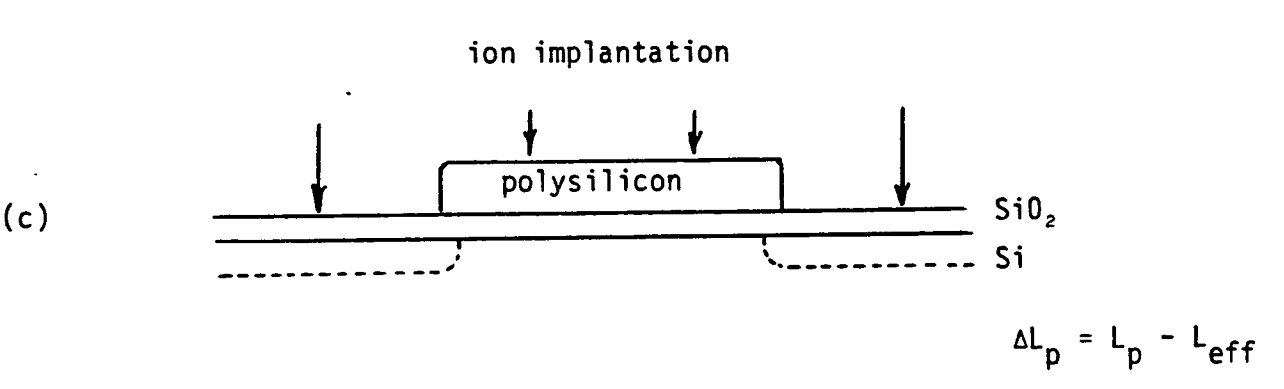
A photolithographic step is used to define the polysilicon layer after deposition and doping. A high degree of control is imperative for the patterning of polysilicon tracks, because, as well as providing an interconnect level on the wafer, this layer defines the channel length of the MOS transistor. However, the final effective channel length is offset from the mask dimension and must be compensated in a procedure known as 'sizing' before maskmaking. Figure 7.1 illustrates the cause of this offset in a practical situation. Photolithography and etching results in an offset ΔL_{mk} between the mask dimension and polysilicon track width. The source/drain implant is self-aligned to the polysilicon gate, although a small amount of lateral scattering occurs. When the source/drain regions and the phosphosilicate glass are annealed, the implanted regions diffuse both vertically and laterally in the silicon. The overall offset ΔL_{mk} between the mask dimension L_{mk} and the final effective channel length L_{eff} is given by

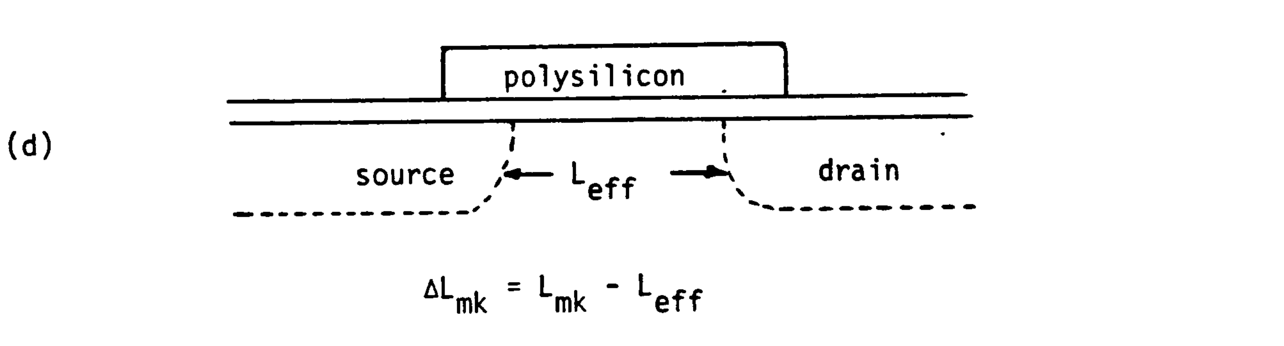
$$\Delta L_{mk} = L_{mk} - L_{eff} \qquad (7.1)$$

Alternatively, in terms of successive offsets









(a) mask
(b) polysilicon definition
(c) source/drain implantation
(d) implant anneal

Figure 7.1 : Process offsets which influence L_{eff}.

$$\Delta L_{mk} = \Delta L_{mk-p} + \Delta L_p \quad (7.2)$$

It is shown later that the offset ΔL_{mk} can be determined from electrical measurements of transistor characteristics, however in order to predict the magnitude of this offset, a 2-D process simulator capable of modelling high concentration profiles is required. Simulation results for the NMOS and PMOS transistors of a p-well CMOS process are presented below. The ion implantation model uses a Pearson IV distribution for the vertical profile of both source/drain implants and threshold adjust implants in the gate regions. While the threshold adjust implant is characterised by low concentrations and can therefore diffuse according to Fick's law, the source/drain regions are doped to high concentration levels and exhibit non-linear diffusion due to several effects as discussed in Chapter 4. From considerations of symmetry, it is only necessary to model impurity redistribution at one edge of the polysilicon gate.

7.2 CURRENT STATUS OF 2-D HIGH CONCENTRATION PROFILE MODELLING

In order to define the initial condition for a model of source/drain diffusion, a 2-D implanted ion profile must be generated. The analytical model of chapter 6 assumes a Gaussian profile in the vertical direction however in order to accurately predict the position of the source/drain junction depth it is necessary to model the channelling tail of the distribution. A Pearson IV profile is

used for the vertical direction into the wafer coupled with a Gaussian probability distribution in the lateral direction. Such implanted distributions can be generated in a simulation program relatively easily, however, subsequent redistribution of impurities at high concentration levels exhibits a high degree of non-linearity and only a fully numerical treatment can give accurate results.

The program RECIPE /198/ uses Pearson IV implanted profiles for boron and joined half-Gaussian profiles for arsenic and phosphorus as in SUPREM. Diffusion is modelled using what the authors describe as an 'incremental' technique, the mathematical details of which are not presented. This program has been used to determine the effective channel length of NMOS transistors, but the accuracy of this method appears to be suspect.

The finite element method offers the advantage of a non-uniform mesh and examples of high concentration diffusion have been shown for NMOS technology /199/ and n-well CMOS /17/.

The finite difference method has been used to simulate source/drain regions in NMOS /15,16,29/ and also coupled diffusion (using the incorrect assumption of local charge neutrality) in a DI-MOS transistor /26,180/.

The method of lines has been used in ROMANSII /20-22/ to simulate an n-well CMOS process, but only Gaussian distributions and not Pearson IV distributions are used for the vertical cross-section

of the implanted profile.

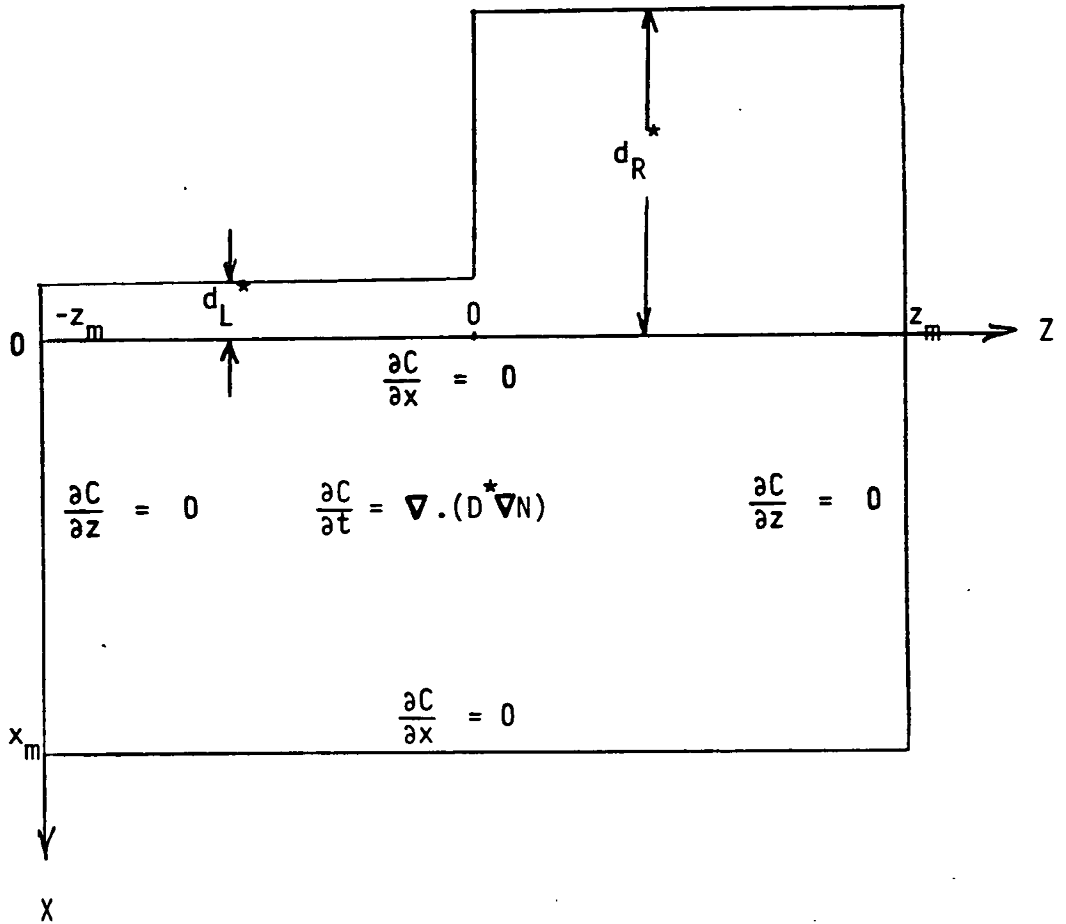
To date, 2-D simulation results of diffused source/drain regions in a p-well CMOS process have never been presented. The program EPIC boasts this capability and also allows determination of effective channel length in small geometry MOS transistors. In the following, simulation results are compared with electrical measurements of devices.

7.3 2-D ION IMPLANTATION USING THE PEARSON IV DISTRIBUTION

Runge's integral (6.6) for implanted profiles at an arbitrarily shaped mask edge can be generalised to include the Pearson IV distribution for the vertical direction through

$$N(x,z) = \frac{Q}{\sqrt{2\pi}\ \Delta Z} \int_{\infty}^{\infty} f_p(x - d_m^*(\gamma) - R_p) \exp[- \frac{(z - \gamma)^2}{2\ \Delta Z^2}] d\gamma \qquad (7.3)$$

If a wafer geometry with vertical mask edges similar to that of figure 7.2 is assumed, the masking materials on each side of the mask edge can be converted to equivalent thicknesses of silicon, d_L^* and d_R^*, according to the density transformation of equations (6.2) and (6.3). Equation (7.3) then reduces to



d_L^* and d_R^* are effective thicknesses of silicon

Figure 7.2 : Coordinate system, differential equation and boundary conditions for diffusion simulation.

$$N(x,z) = \frac{Q}{2}\left[f_p(x + d_L^* - R_p)\,\mathrm{erfc}\left(\frac{z}{\sqrt{2}\,\Delta Z}\right) + f_p(x + d_R^* - R_p)\left(1 + \mathrm{erf}\left(\frac{z}{\sqrt{2}\,\Delta Z}\right)\right)\right] \tag{7.4}$$

where the Pearson IV distribution f_p is defined by (4.3). This equation provides the initial condition for a general high concentration diffusion problem.

7.4 NUMERICAL MODELS FOR 2-D DIFFUSION

7.4.1 Diffusion of Threshold Adjust Implants

The low doses characteristic of threshold adjust implants allow the use of a constant diffusivity D in the general diffusion equation. The numerical solution of Fick's law, equation (6.13), subject to homogeneous Neumann type boundary conditions (7.5) - (7.8), is well studied in basic texts on numerical analysis /23, 24, 35, 200, 201/.

$$\frac{\partial N}{\partial x} = 0 \quad ; \quad x = 0 \tag{7.5}$$

$$\frac{\partial N}{\partial x} = 0 \quad ; \quad x = x_m \tag{7.6}$$

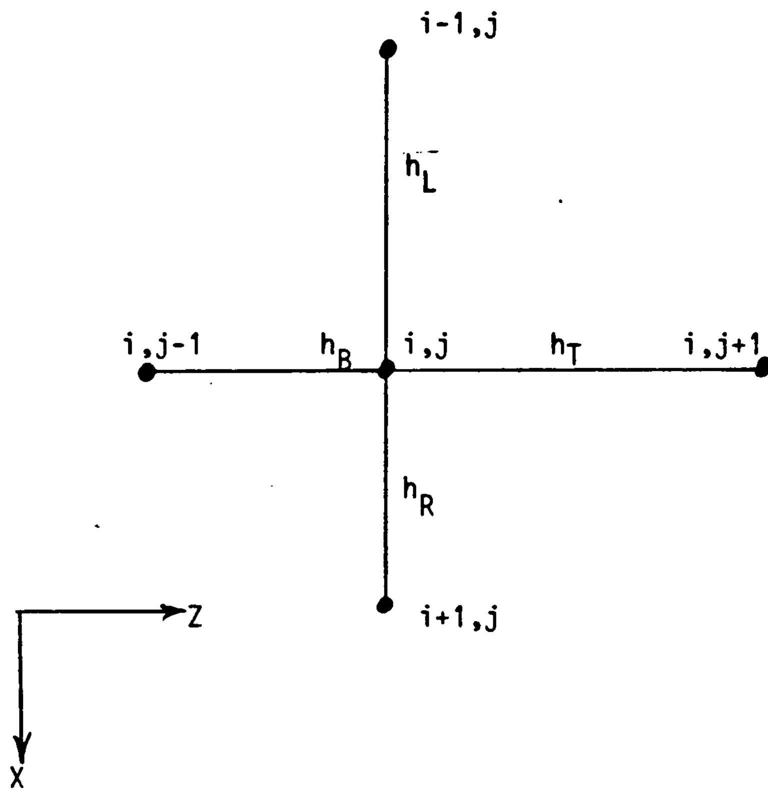
$$\frac{\partial N}{\partial z} = 0 \quad ; \quad z = -z_m \tag{7.7}$$

$$\frac{\partial N}{\partial z} = 0 \quad ; \quad z = z_m \tag{7.8}$$

The use of an explicit difference scheme to solve the parabolic diffusion equation requires utilisation of small time steps in order to ensure numerical stability /23, 35/. Larger time steps and shorter execution times are possible with the use of an implicit difference scheme, but these methods require solution of a matrix equation.

The Crank-Nicolson method /203/ is unconditionally stable for arbitrary choice of time step and has been used by Tielert /25, 26, 180/ in the program LADIS. A further speed advantage in the solution of 2-D diffusion problems can be gained by using the alternating-direction-implicit (ADI) method of Peaceman and Rachford /204/. Buonomo and C. Di Dello /207/ have already used this technique to solve problems of gaseous predeposition, where the impurity concentration on the surface of the silicon wafer is kept constant, and drive-in, where the initial distribution is characterised by an impulse and the integrated impurity concentration is invariant during the diffusion process. EPIC uses the ADI method to model the diffusion of 2-D ion implanted profiles, and in addition, allows the use of a non-uniform mesh.

Figure 7.3 defines the five-point finite difference star used for discretisation. In the ADI approach, an implicit discretisation approximation is used for the x direction and an explicit difference approximation for the z-direction during one time step. The procedure is alternated in the following time step so that the difference approximation is then explicit in x but implicit in z. The re-



$$h_L = x_i - x_{i-1}$$
$$h_R = x_{i+1} - x_i$$
$$h_B = z_j - z_{j-1}$$
$$h_T = z_{j+1} - z_j$$

Figure 7.3 : Five point finite difference star for discretisation

petitive use of either of these solution procedures on its own results in an uncontrollable growth of numerical errors. However, if the direction of implicitness is alternated for each step solution and the time step remains unchanged within a pair of time solutions, then the method is unconditionally stable for arbitrary size of time step /204/.

In order to advance from the nth to the (n+1)th time level, it is necessary to solve

$$\frac{N_{i,j,n+1} - N_{i,j,n}}{\delta t} =$$

$$D \left\{ \frac{1}{h_L(h_L + h_R)} N_{i-1,j,n+1} - \frac{1}{h_L h_R} N_{i,j,n+1} + \frac{1}{h_R(h_L + h_R)} N_{i+1,j,n+1} \right.$$

$$\left. + \frac{1}{h_B(h_B + h_T)} N_{i,j-1,n} - \frac{1}{h_B h_T} N_{i,j,n} + \frac{1}{h_T(h_B + h_T)} N_{i,j+1,n} \right\} ;$$

$$i = 0\ (1)\ M,\ j = 0\ (1)\ S \qquad (7.9a)$$

where δt is the time step.

Subsequently, the solution at the (n+2)th level is given by

$$\frac{N_{i,j,n+2} - N_{i,j,n+1}}{\delta t} =$$

$$D \{\frac{1}{h_L(h_L + h_R)} N_{i-1,j,n+1} - \frac{1}{h_L h_R} N_{i,j,n+1} + \frac{1}{h_R(h_L + h_R)} N_{i+1,j,n+1}$$

$$+ \frac{1}{h_B(h_B + h_T)} N_{i,j-1,n+2} - \frac{1}{h_B h_T} N_{i,j,n+2} + \frac{1}{h_T(h_B + h_T)} N_{i,j+1,n+2}\} ;$$

$$i = 0\ (1)\ M, \quad j = 0\ (1)\ S \qquad (7.9b)$$

Boundary conditions are represented by virtual nodes outside the simulation area and equations (7.5) - (7.8) are discretised using central differences to give (7.10) - (7.13) respectively.

$$N_{-1,j,n} = N_{1,j,n} \quad ; \quad j = 0\ (1)\ S \qquad (7.10)$$

$$N_{M+1,j,n} = N_{M-1,j,n} \quad ; \quad j = 0\ (1)\ S \qquad (7.11)$$

$$N_{i,-1,n} = N_{i,1,n} \quad ; \quad i = 0\ (1)\ M \qquad (7.12)$$

$$N_{i,S+1,n} = N_{i,S-1,n} \quad ; \quad i = 0\ (1)\ M \qquad (7.13)$$

In the discretised boundary conditions, the subscript n refers to a general time level and can therefore be replaced by (n+1), (n+2), etc.

Equation (7.9a) represents (S+1) independent linear systems

of equations where each system contains (M+1) unknowns. Similarly equation (7.9b) represents (M+1) independent linear systems of equations, where each system contains (S+1) unknowns. Each linear system can be written in matrix form and solved directly using the highly efficient 'tridiagonal algorithm' /23/.

7.4.2 Diffusion of Source/Drain Regions

High concentration diffusion is non-linear and requires a full 2-D numerical treatment in order to model both the vertical and lateral extent of dopant profiles. The diffusion equation (4.30) is written in its 2-D form assuming isotropy to give

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x} \left(D^* \frac{\partial N}{\partial x}\right) + \frac{\partial}{\partial z} \left(D^* \frac{\partial N}{\partial z}\right) \qquad (7.14)$$

where the effective diffusivity D^* is concentration dependent through (4.31). A distinction must be made between the active impurity concentration N and the total or chemical concentration C.

This second order partial differential equation is subject to initial condition (7.4) and boundary conditions (7.15) - (7.18).

$$\frac{\partial C}{\partial x} = 0 \quad ; \quad x = 0 \qquad (7.15)$$

$$\frac{\partial C}{\partial x} = 0 \quad ; \quad x = x_m \qquad (7.16)$$

$$\frac{\partial C}{\partial z} = 0 \quad ; \quad z = -z_m \tag{7.17}$$

$$\frac{\partial C}{\partial z} = 0 \quad ; \quad z = z_m \tag{7.18}$$

Several mathematical treatises on the ADI method /205, 206, 208/ suggest that this method should be applicable to the solution of (7.14). In practice this did not prove feasible, and consequently, in EPIC only low concentration diffusion problems are solved using the ADI method.

A difference scheme between two time levels can in general be written in the form

$$\frac{C_{i,j,n+1} - C_{i,j,n}}{\delta t} = \Gamma_{i,j,\bar{n}} \tag{7.19}$$

where the parameter $\bar{n}$ defines the time discretisation.

Boundary conditions (7.15) - (7.18) are discretised to

$$C_{-1,j,n} = C_{1,j,n} \quad ; \quad j = 0\ (1)\ S \tag{7.20}$$

$$C_{M+1,j,n} = C_{M-1,j,n} \quad ; \quad j = 0\ (1)\ S \tag{7.21}$$

$$C_{i,-1,n} = C_{i,1,n} \quad ; \quad i = 0\ (1)\ M \tag{7.22}$$

$$C_{i,S+1,n} = C_{i,S-1,n} \quad ; \quad i = 0\ (1)\ M \tag{7.23}$$

Using central differences with the star of figure 7.3, the spatial discretisation is given by

$$\Gamma_{i,j,\bar{n}} = \frac{1}{(h_L + h_R)}\left[\frac{(D^*_{i-1,j,\bar{n}} + D^*_{i,j,\bar{n}})(N_{i-1,j,\bar{n}} - N_{i,j,\bar{n}})}{h_L} + \frac{(D^*_{i,j,\bar{n}} + D^*_{i+1,j,\bar{n}})(N_{i+i,j,\bar{n}} - N_{i,j,\bar{n}})}{h_R} \right]$$

$$+ \frac{1}{(h_B + h_T)}\left[\frac{(D^*_{i,j-1,\bar{n}} + D^*_{i,j,\bar{n}})(N_{i,j-1,\bar{n}} - N_{i,j,\bar{n}})}{h_B} + \frac{(D^*_{i,j,\bar{n}} + D^*_{i,j+1,\bar{n}})(N_{i,j+1,\bar{n}} - N_{i,j,\bar{n}})}{h_T} \right] ;$$

$$i = 0\ (1)\ M,\ j = 0\ (1)\ S \qquad (7.24)$$

The time level $\bar{n}$ is given by a weighted average of conditions at the nth (known) and (n+1)th (unknown) time levels according to equations (7.25) and (7.26) (similar expressions hold at all adjacent nodes, however for brevity only the (i,j)th node is considered here).

$$N_{i,j,\bar{n}} = (1 - \theta)\, N_{i,j,n} + \theta\, N_{i,j,n+1} \quad ; \quad i = 0\ (1)\ M,\ j = 0\ (1)\ S \qquad (7.25)$$

$$D_{i,j,\bar{n}} = (1 - \theta)\, D^*(C_{i,j,n}) + \theta\, D^*(C_{i,j,n+1}) \quad ; \quad i = 0\,(1)\,M,\ j = 0\,(1)\,S \tag{7.26}$$

The parameter θ must be chosen such that $0 \leq \theta \leq 1$ and in practical situations, it assumes the value 0, 1/2 or 1. If $\theta = 0$, then $\bar{n} = n$ and the difference scheme is explicit. As already discussed, explicit methods are subject to numerical instability if δt is too large. A fully implicit method results if $\theta = 1$, which is equivalent to the statement $\bar{n} = n+1$. If $\theta = 1/2$ then $n = n+1/2$ and the spatial discretisation is an arithmetic average of conditions at the known and unknown time levels. This choice of θ gives second order accuracy in time step δt and also ensures numerical stability. This approach is known as the Crank-Nicolson method or Euler's method and is used by Tielert /25,26,180/ and Penumalli /27-29/ for discretisation on a uniform rectangular mesh. The analysis is extended to non-uniform rectangular grids in EPIC.

When the Crank-Nicolson method is applied, the discretised transport equation can be written in homogeneous form to give

$$\Gamma_{i,j,n+\frac{1}{2}} - \frac{C_{i,j,n+1} - C_{i,j,n}}{\delta t} = 0 \quad ; \quad i = 0\,(1)\,M,\ j = 0\,(1)\,S \tag{7.27}$$

Alternatively, and more concisely,

$$\underline{f}(\underline{C}) = 0 \tag{7.28}$$

where

$$\underline{f} = [f_0 \ f_1 \ f_2 \ \ldots\ldots\ldots \ f_Q]^T \tag{7.29}$$

is a non-linear vector function with Q = (M+1)(S+1) components, and

$$\underline{C} = [C_0 \ C_1 \ C_2 \ \ldots\ldots\ldots \ C_Q]^T \tag{7.30}$$

is a vector whose components comprise the concentration values at each of the Q mesh points in the simulation domain (for convenience only a single subscript is used to refer to a specific mesh point and the time level subscript n+1 is assumed).

Equation (7.24) is repeatedly linearised using Newton's method /78/ through

$$\underset{\sim}{J}(\underline{C})^{(k)} \ \underline{\Delta C}^{(k)} = \underline{f}(\underline{C}^{(k)}) \quad ; \ k = 1, 2, 3 \ldots. \tag{7.31}$$

where the correction vector $\underline{\Delta C}^{(k)}$ at iteration k is given by

$$\underline{\Delta C}^{(k)} = \underline{C}^{(k-1)} - \underline{C}^{(k)} \quad ; \ k = 1, 2, 3 \ldots. \tag{7.32}$$

The concentration values at time level n are used for the initial guess $C^{(o)}$ and the Jacobian matrix $\underset{\sim}{J}$ is defined by

$$\underset{\sim}{J}(\underline{C}) = \begin{bmatrix} \frac{\partial f_o}{\partial C_0} & \frac{\partial f_o}{\partial C_1} & \cdots\cdots & \frac{\partial f_o}{\partial C_Q} \\ \frac{\partial f_1}{\partial C_0} & \frac{\partial f_1}{\partial C_1} & \cdots\cdots & \frac{\partial f_1}{\partial C_Q} \\ \vdots & \vdots & & \vdots \\ \frac{\partial f_Q}{\partial C_0} & \frac{\partial f_Q}{\partial C_1} & \cdots\cdots & \frac{\partial f_Q}{\partial C_Q} \end{bmatrix} . \tag{7.33}$$

The entries of the Jacobean matrix are evaluated by analytical partial differentation of the components of $\underline{f}$ in equation (7.29). Fortunately most of the elements are zero and the matrix is said to be 'sparse'. Equation (7.31) defines a large sparse linear system which is solved iteratively using the successive over-relaxation (SOR) technique for diagonally dominant matrices /23,35/.

In a practical situation, only a few Newton iterations are required for convergence to a safe tolerance limit, but the use of two nested iteration levels in this solution procedure results in long execution times.

7.5 SIMULATION RESULTS FOR A P-WELL CMOS PROCESS

The 2-D ion implantation and diffusion models in EPIC can be used to simulate impurity redistribution at the polysilicon gate edge of both NMOS and PMOS transistors. Table 7.1 defines the p-

n-substrate implant	2.1×10^{12} cm^{-2} $^{31}P^{+}$ at 125 keV
p-well implant	1×10^{13} cm^{-2} $^{11}B^{+}$ at 60 keV
gate oxide growth	500Å
n-substrate gate adjust implant	6×10^{11} cm^{-2} $^{11}B^{+}$ at 45 keV
polysilicon doping	85 mins at 900°C
n-substrate source/drain implant	5×10^{15} cm^{-2} B^{+} at 35 keV
p-well source/drain implant either	1×10^{16} cm^{-2} $^{75}As^{+}$ at 80 keV
or	5×10^{15} cm^{-2} $^{31}P^{+}$ at 85 keV
PSG anneal	14 mins ramp 900 - 1000°C
	30 mins at 1000°C

Table 7.1 : CMOS process parameters for EPIC simulation

well CMOS parameters for the simulation examples to follow. Only the parameters different from those in table 4.5 are shown in order to avoid duplication.

SUPREM is used to simulate the p-well and n-substrate regions until after gate oxidation. EPIC is used to model subsequent process steps. Only the PMOS transistor receives a threshold adjust implant. A source/drain implant of boron is used for the PMOS transistor, and either phosphorus or arsenic is used for the source/drain regions of the NMOS transistor. The doping profile for each transistor is now considered.

Figure 7.4 shows an equidensity contour plot of the threshold adjust implant of boron which is carried out through the gate oxide. The same distribution is shown as a surface plot in figure 7.5. The diffusion of this implant during the polysilicon doping step is modelled by EPIC and added to the SUPREM results for the phosphorus of the n-substrate region. Figure 7.6 and 7.7 show the net concentration in the active device region of the PMOS transistor and also the existence of a p-n junction. The source/drain implant of boron is shown by figures 7.8 and 7.9. The polysilicon gate is thick enough to prevent most of the boron reaching the active device region. The boron of the source/drain implant is combined with the threshold adjust implant in the n-substrate and subjected to the final high temperature anneal in the process.

Figures 7.10 and 7.11 show the final net concentration in the

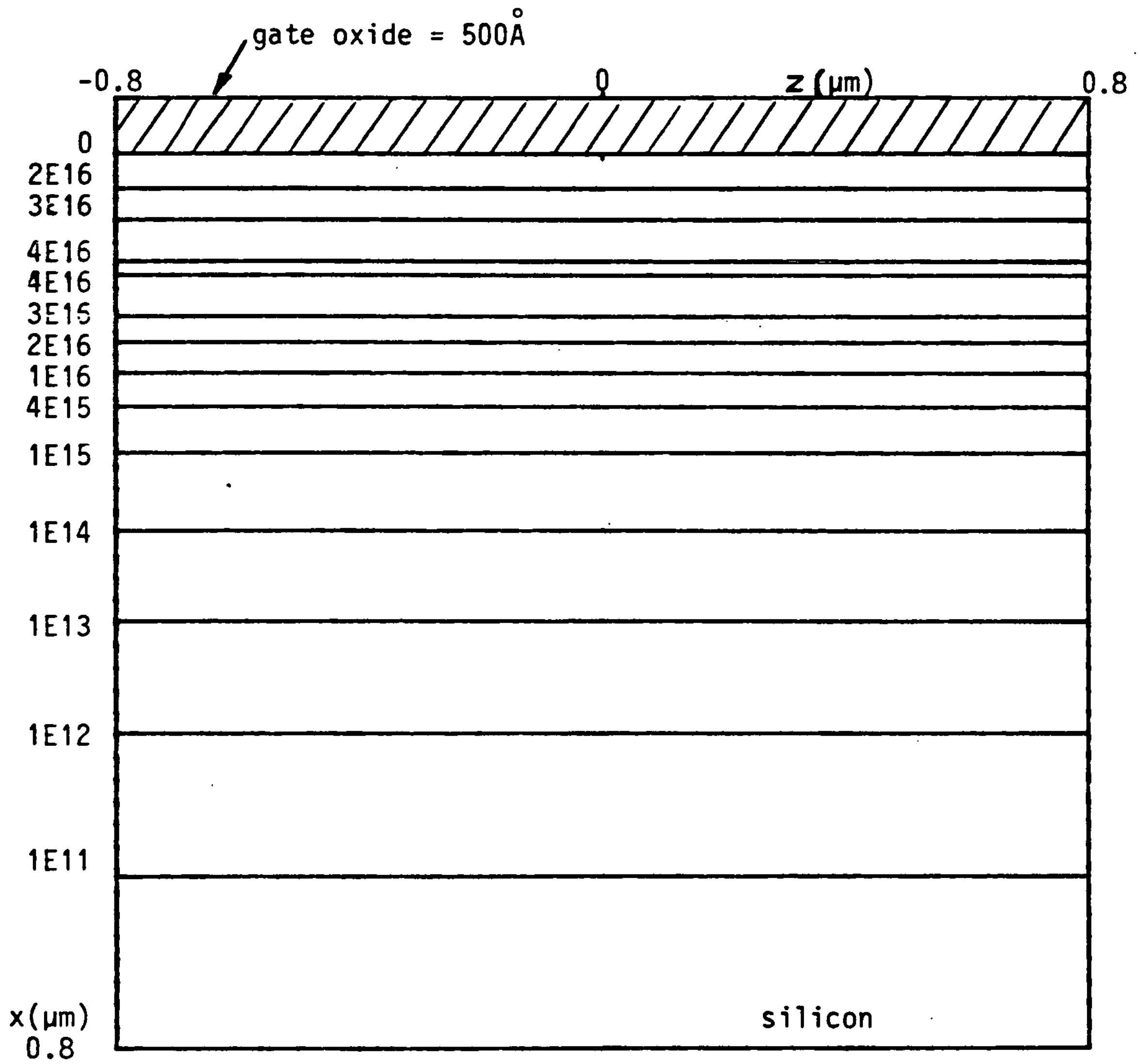


Figure 7.4 : Boron threshold adjust implant

6×10^{11} cm^{-2} $^{11}B^{+}$ at 45 keV

log concentration (cm^{-3})

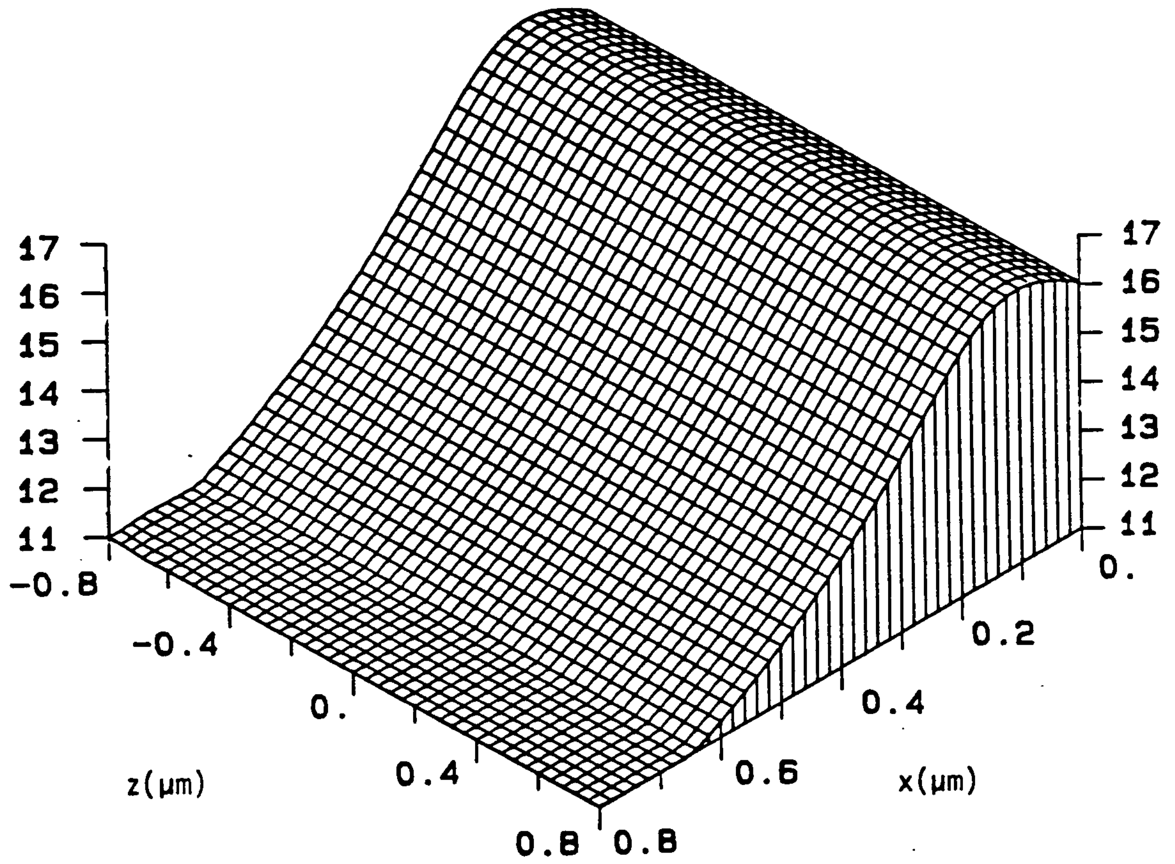


Figure 7.5 : Boron threshold adjust implant

6×10^{11} cm^{-2} $^{11}B^{+}$ at 45 keV.

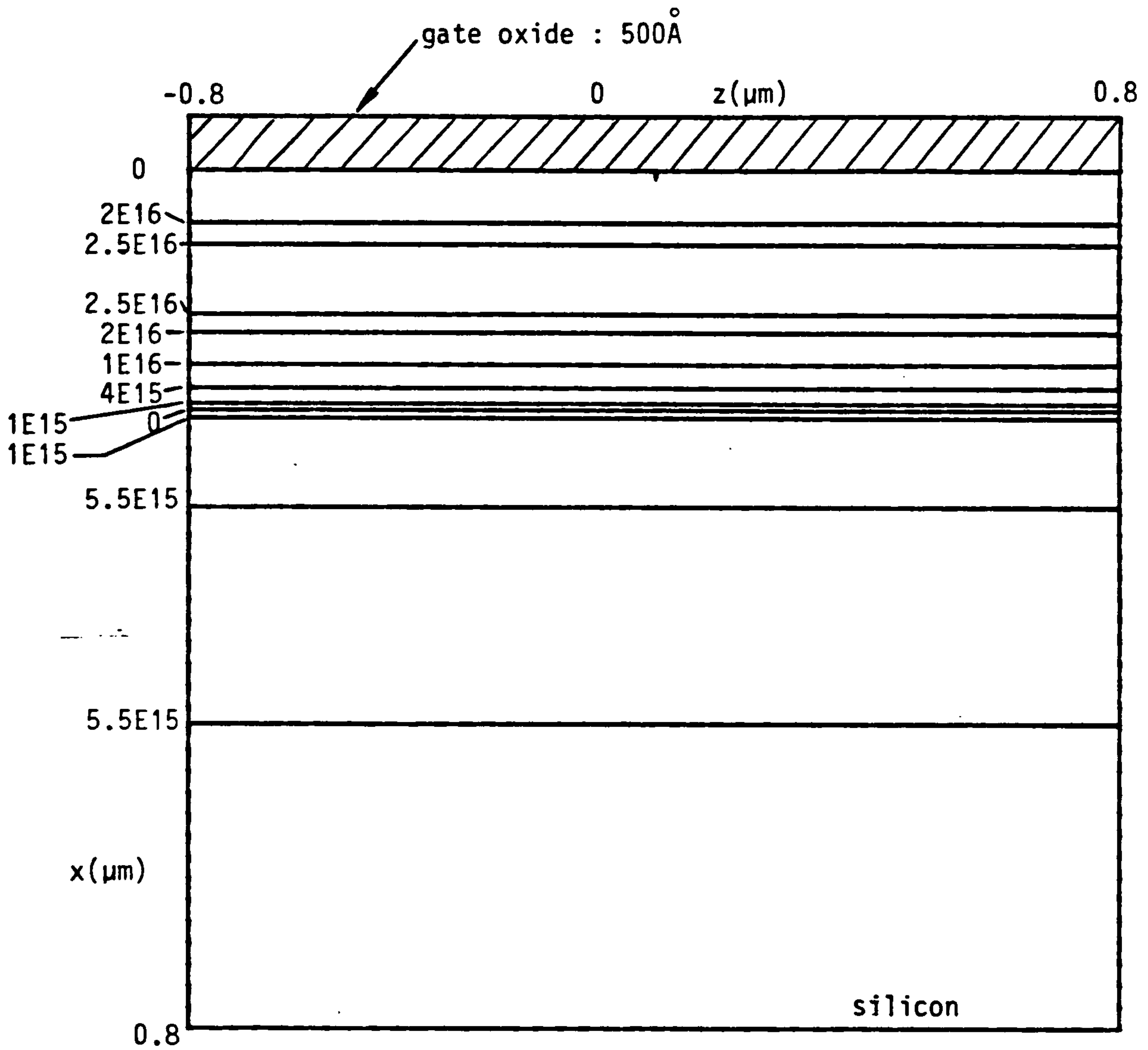


Figure 7.6 : Threshold adjust implant in the n-substrate after poly-silicon doping:85 mins at 900°C.

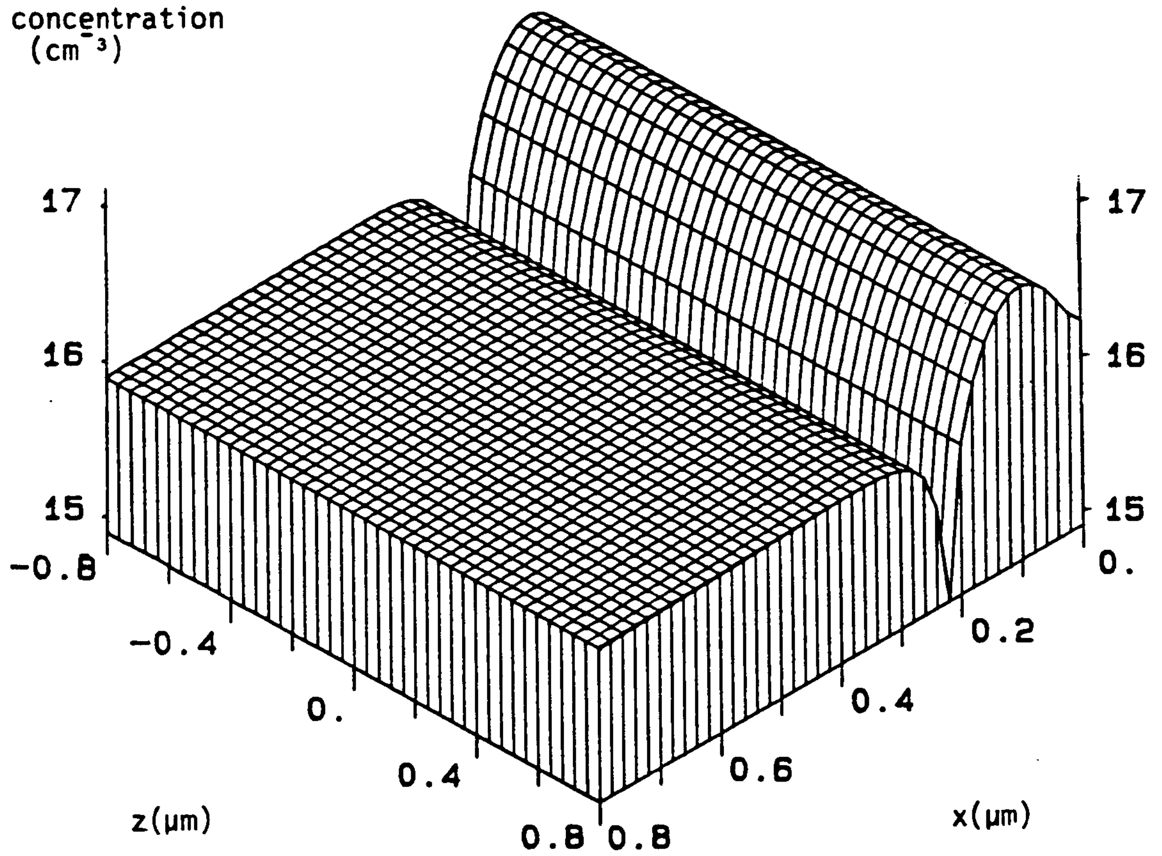


Figure 7.7 : Threshold adjust implant in the n-substrate
after polysilicon doping:85 mins at 900°C.

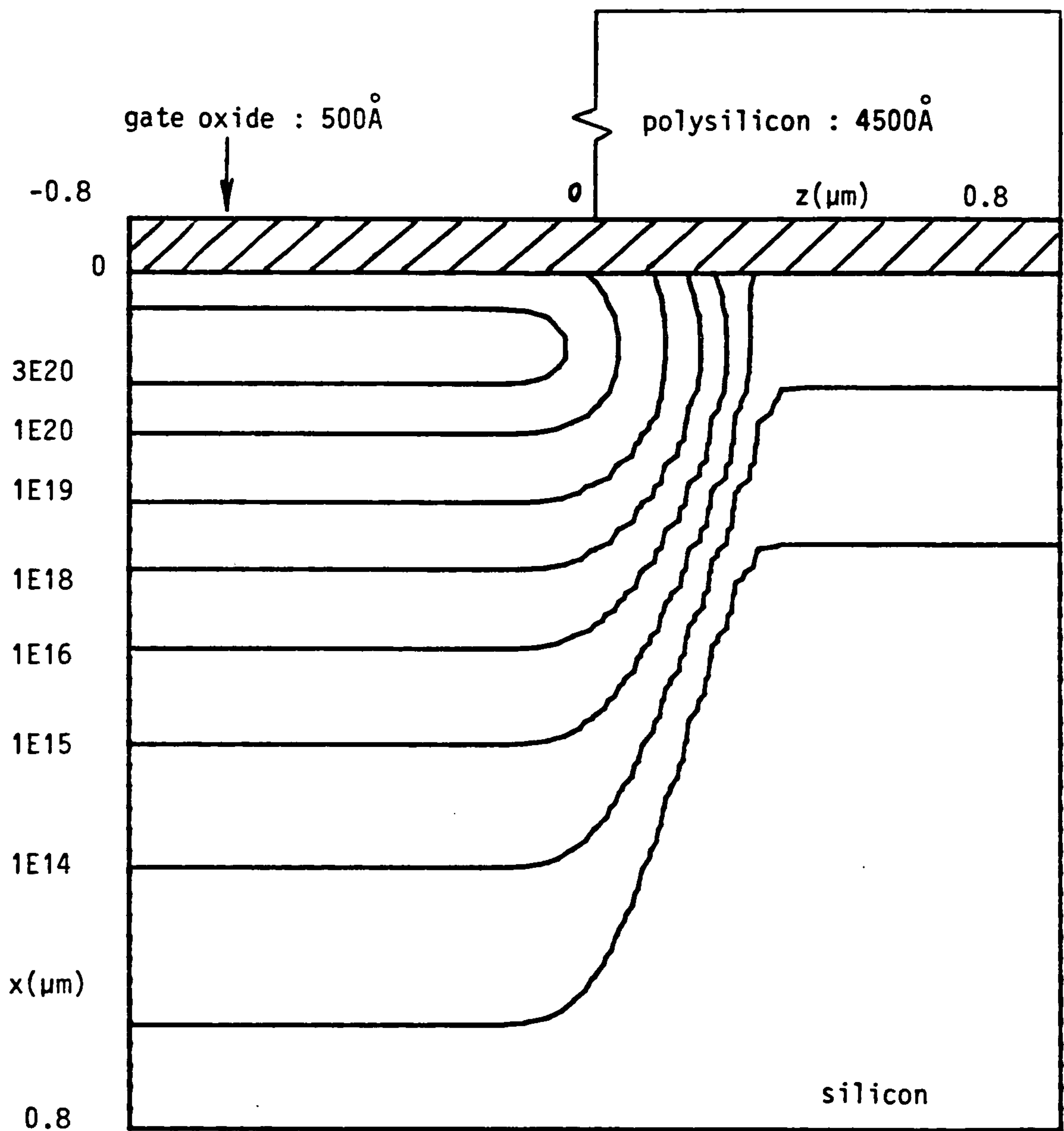


Figure 7.8 : Boron source/drain implant

5×10^{15} cm^{-2} $^{11}B^{+}$ at 35 keV

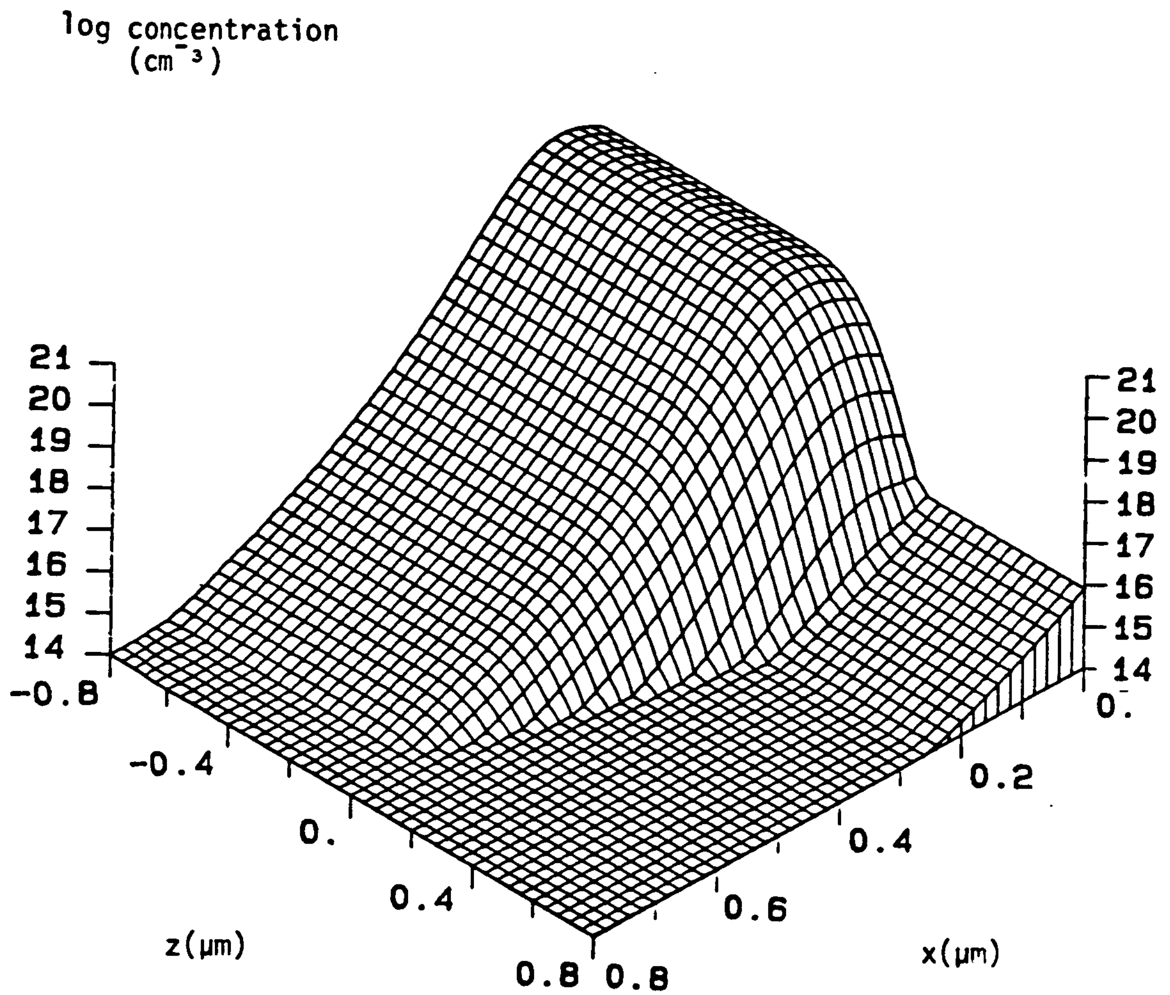


Figure 7.9 : Boron source/drain implant

5×10^{15} cm^{-2} $^{11}B^{+}$ at 35 keV

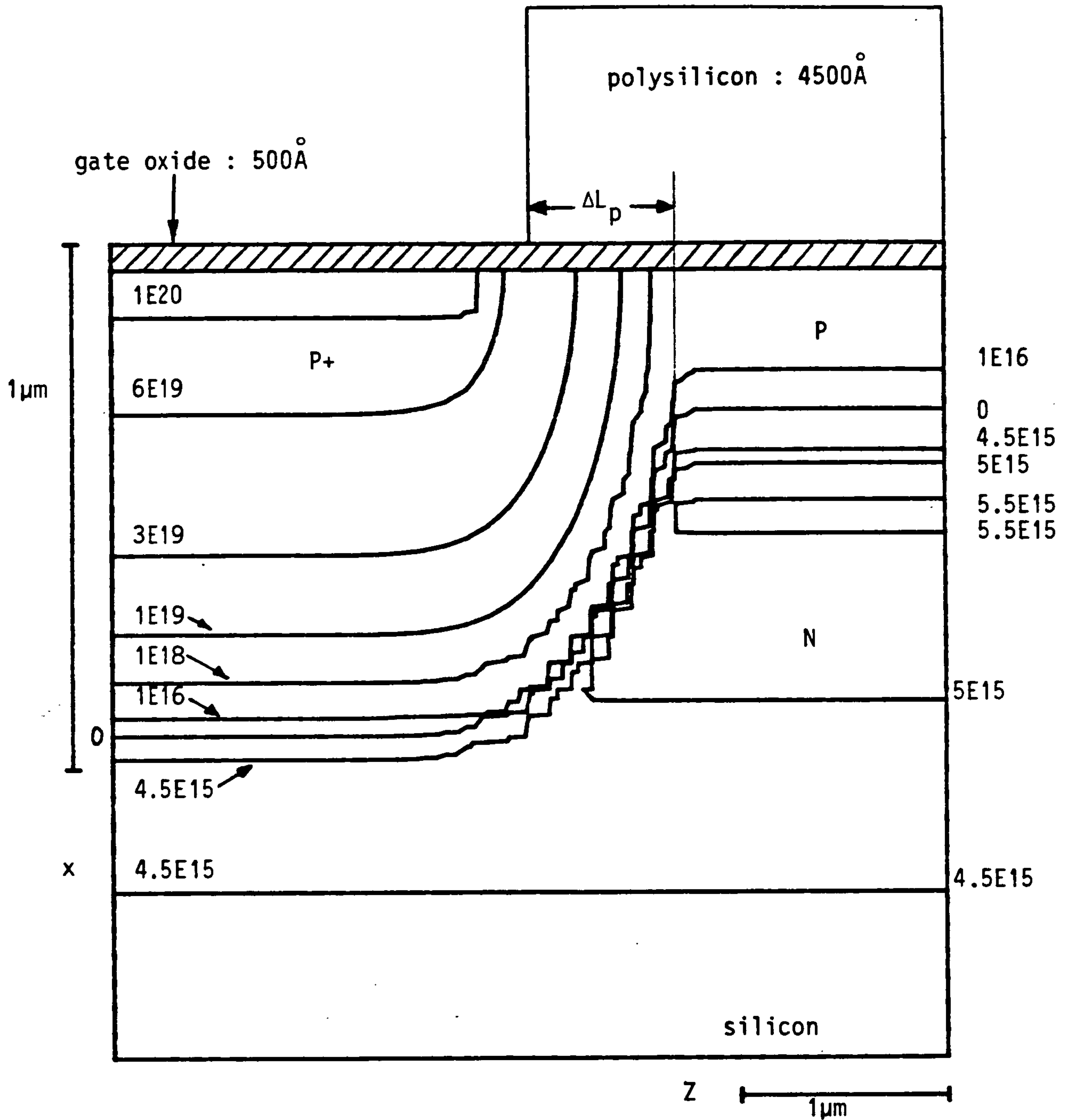


Figure 7.10 : Net profile of PMOSFET after PSG anneal

14 mins ramp 900 - 1000°C

30 mins at 1000°C

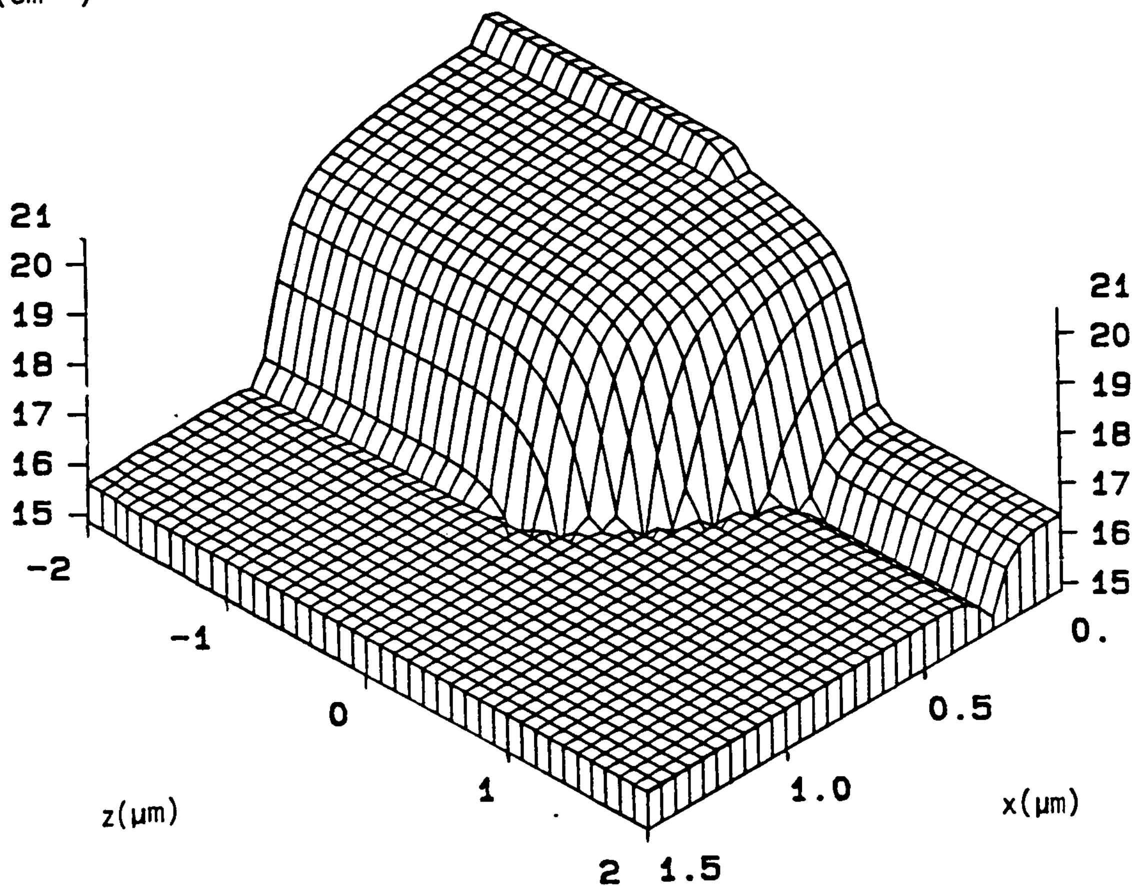


Figure 7.11 : Net profile of PMOSFET after PSG anneal

14 mins ramp 900 - 1000°C

30 mins at 1000°C

PMOS transistor. The p-n junction does not terminate at the silicon surface due to the existence of the net p-type layer under the polysilicon gate. The inactive boron at the surface of the source/drain region is clearly shown by figure 7.11. The contour plot of figure 7.10 allows an estimate of the lateral diffusion of the source/drain implant under the polysilicon gate. This offset of the profile from the polysilicon edge also appears at the other end of the transistor gate and, using the notation of figure 7.1

$$\Delta L_p = 1.40\ \mu m \qquad \text{(PMOS : B source/drain)} \qquad (7.34)$$

EPIC is also capable of simulating the doping profile in the NMOS transistor, which in contrast to the PMOS device, does not require a threshold adjust implant. Figures 7.12 and 7.13 show plots of the phosphorus source/drain implant.

As in the case of boron, a small proportion of the implanted phosphorus penetrates the polysilicon gate and underlying gate oxide to reach the active device region of the NMOS transistor. The use of phosphorus for the source/drain implant can result in a distribution of threshold voltages for NMOS transistors on the same silicon wafer /209/. This effect is caused by the random orientation of polysilicon grains in the gate electrode of small geometry devices. Whenever the 100 direction of a grain lines up with the direction of the implanted ions, an increased degree of channeling occurs and

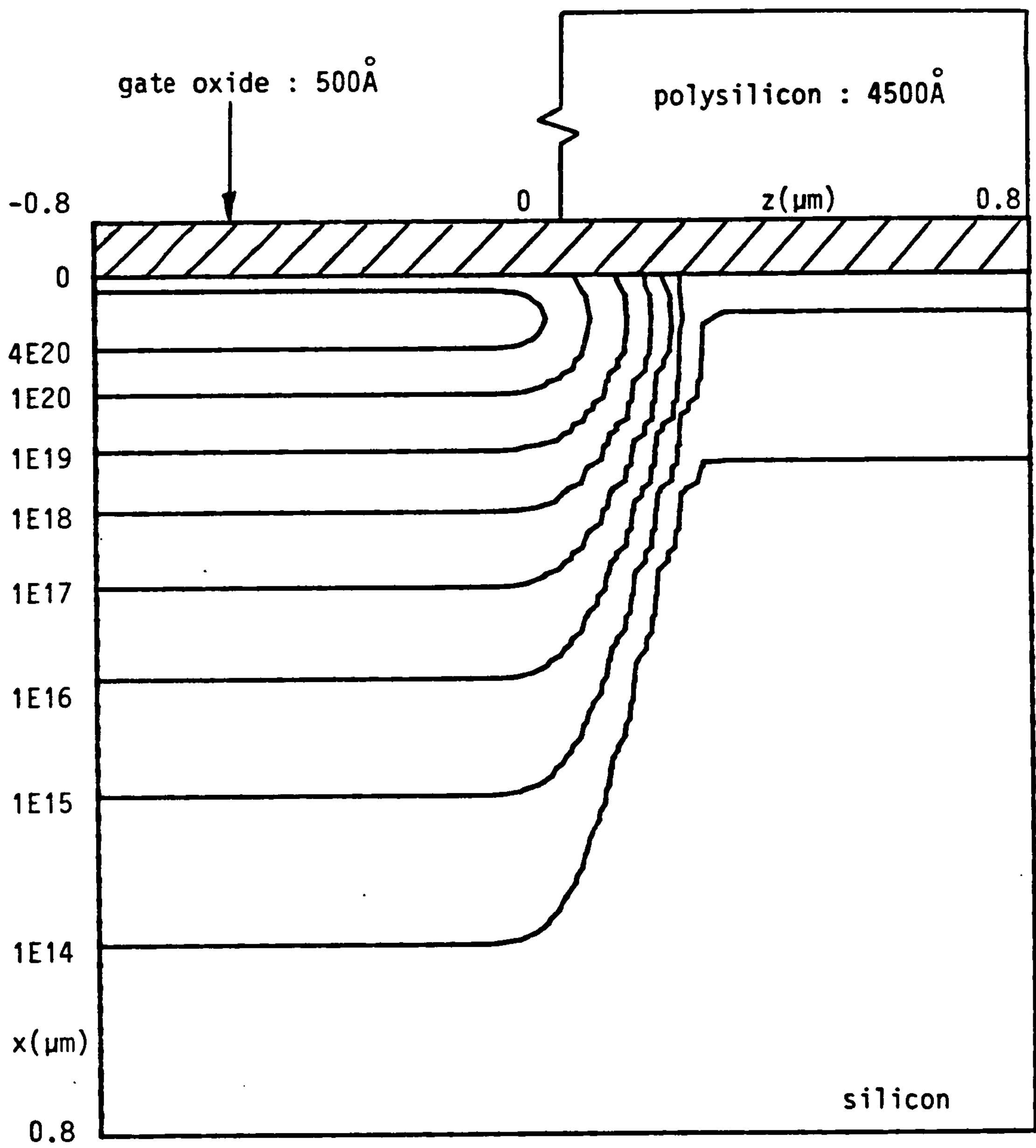


Figure 7.12 : Phosphorus source/drain implant

5×10^{15} cm^{-2} $^{31}P^{+}$ at 85 keV

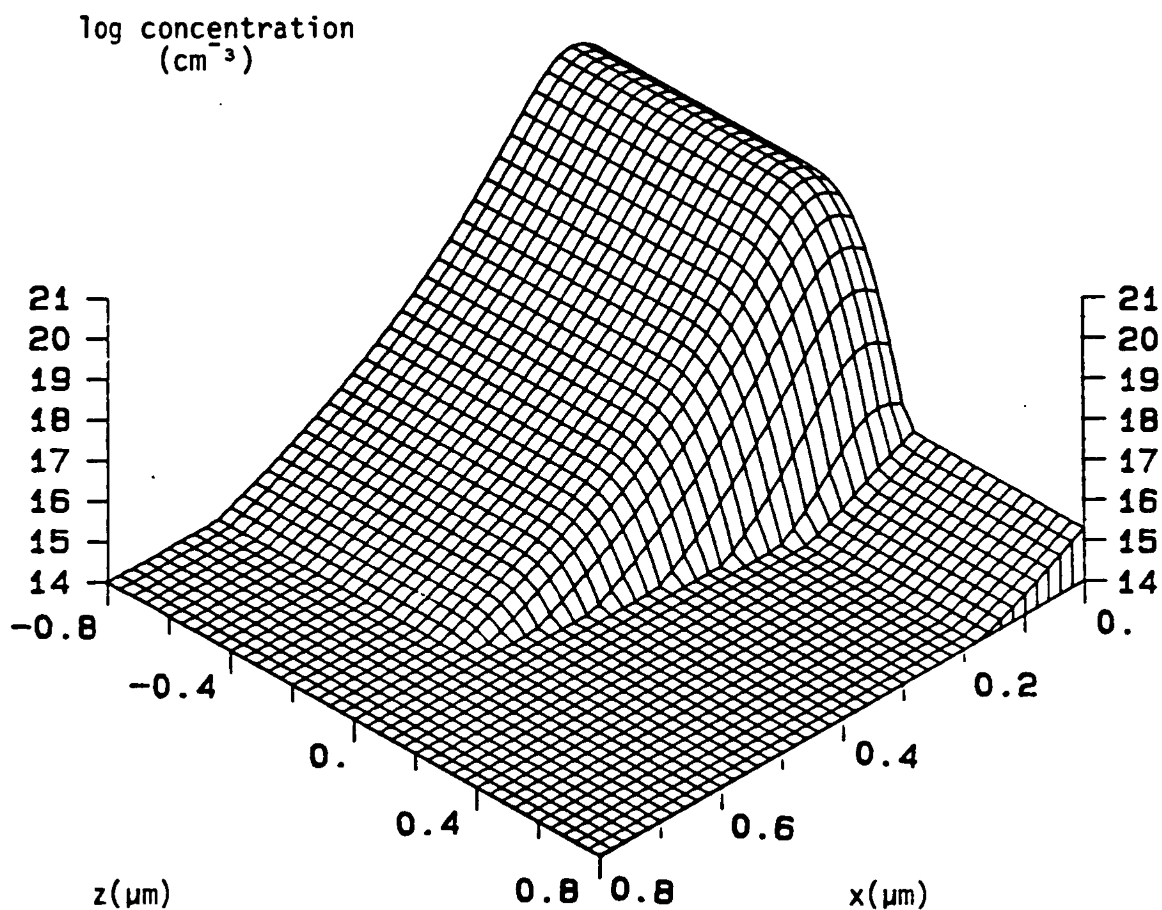


Figure 7.13: Phosphorus source/drain implant

5×10^{15} cm^{-2} $^{31}P^{+}$ at 85 keV

more phosphorus can penetrate through the gate into the silicon. This random effect is not modelled by EPIC.

After the PSG anneal, the phosphorus distribution is added to the SUPREM results for the p-well to give the final profile of the NMOS transistor as in figures 7.14 and 7.15.

The solid solubility of phosphorus is much higher than that of boron, and so no inactive dopant appears at the peak of the distribution. Instead, the enhanced diffusion in this region gives rise to a plateau near the silicon surface. From figure 7.14, the offset ΔL_p is found to be

$$\Delta L_p = 1.55\ \mu m \qquad \text{(NMOS : P source/drain)} \qquad (7.35)$$

The use of arsenic for source/drain regions in NMOS transistors is now preferred to phosphorus in order to reduce junction depths and minimise short channel effects /69-71/. Figure 7.16 shows the arsenic profile after source/drain implantation at the polysilicon mask edge. The fraction of ions penetrating the polysilicon gate into the active device region is negligible for the same polysilicon layer thickness as was assumed for the boron and phosphorus implants. The subsequent diffusion of the arsenic profile is simulated by EPIC and combined with the SUPREM results for the p-well to give the net profile of figures 7.18 and 7.19. The peak of

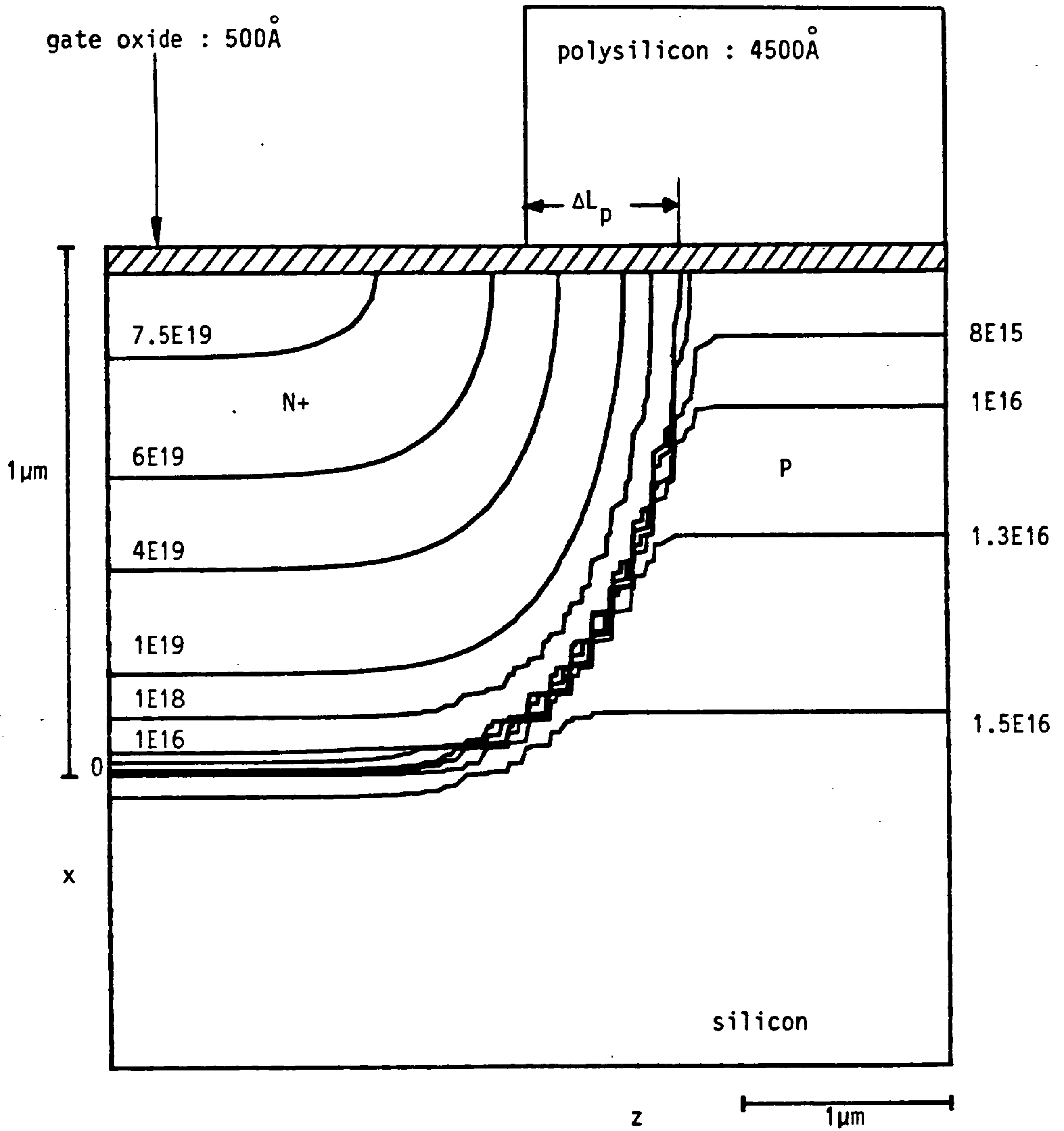


Figure 7.14: Net profile of NMOSFET (P source/drains) after PSG anneal

14 mins ramp 900 - 1000°C

30 mins at 1000°C

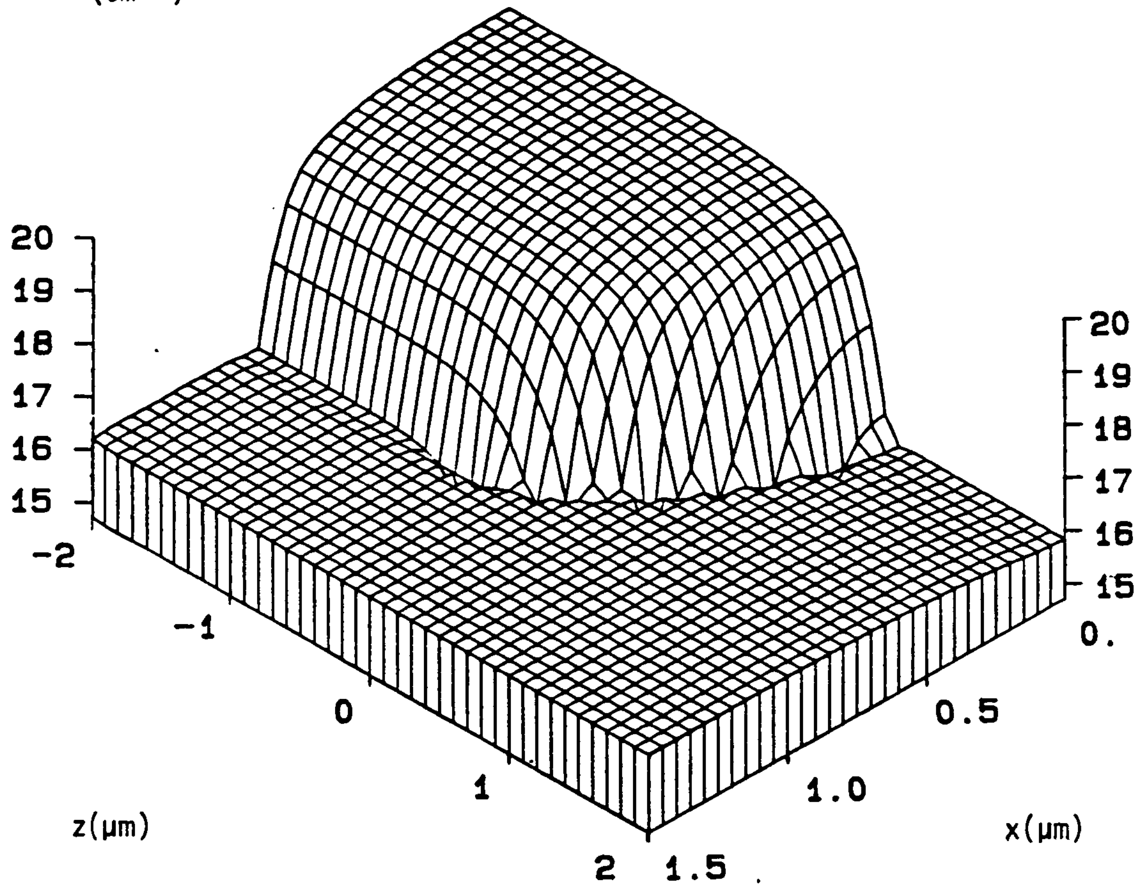


Figure 7.15 : Net profile of NMOSFET (P source/drains) after PSG anneal

14 mins ramp 900 - 1000°C

30 mins at 1000°C

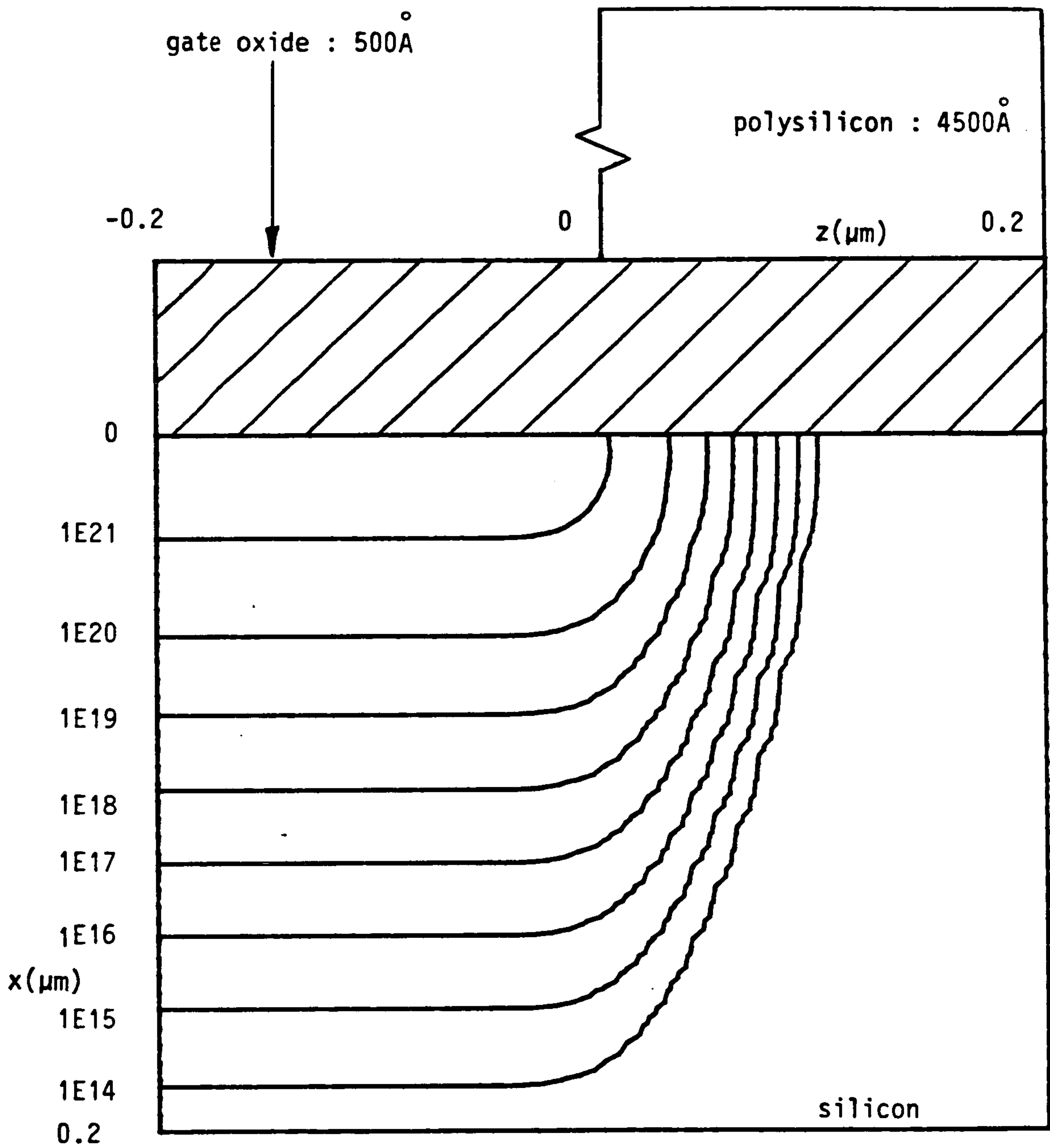


Figure 7.16 : Arsenic source/drain implant

1×10^{16} cm^{-2} $^{75}As^{+}$ at 80 keV

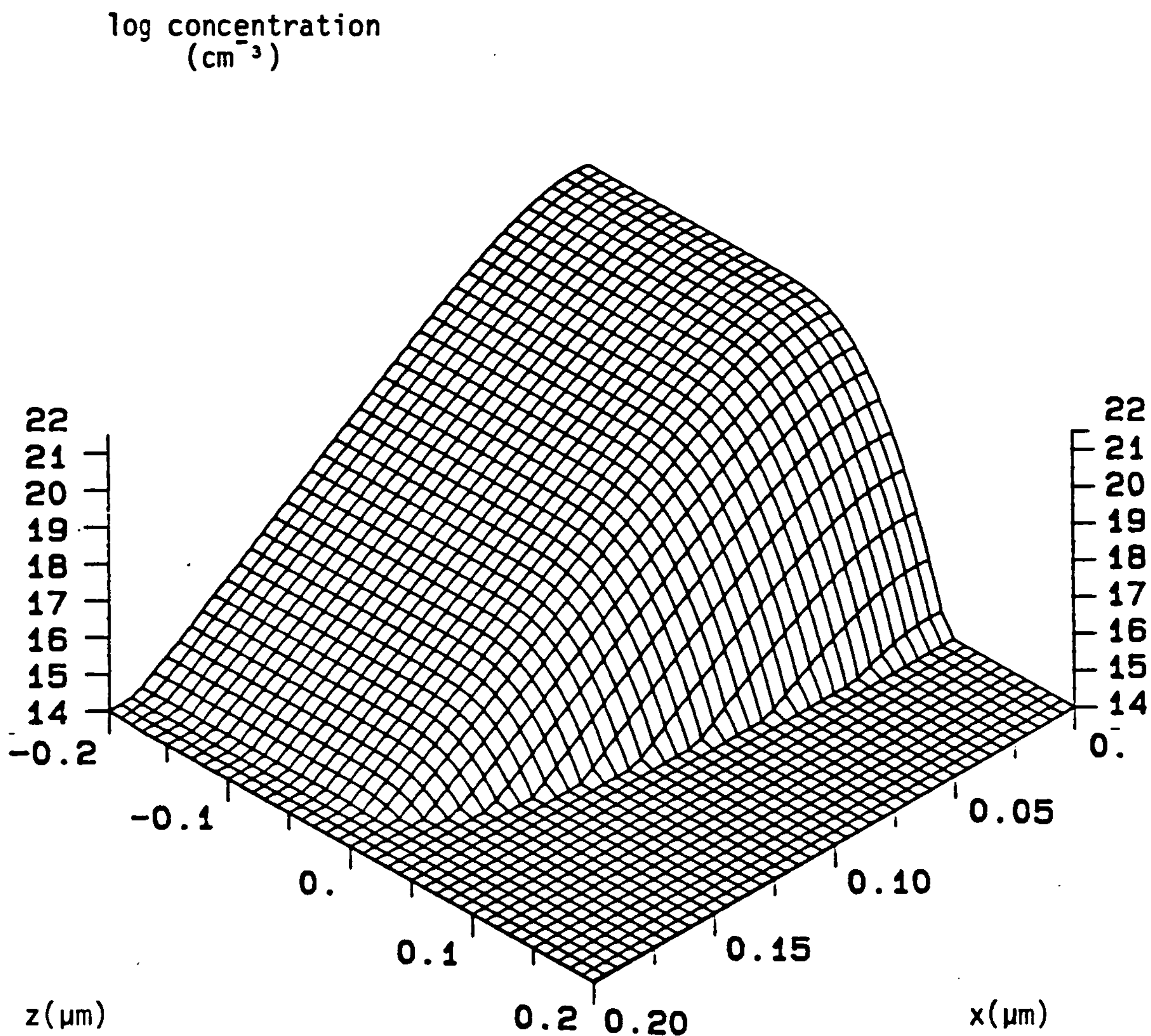


Figure 7.17 : Arsenic source/drain implant

1×10^{16} cm^{-2} $^{75}As^{+}$ at 80 keV

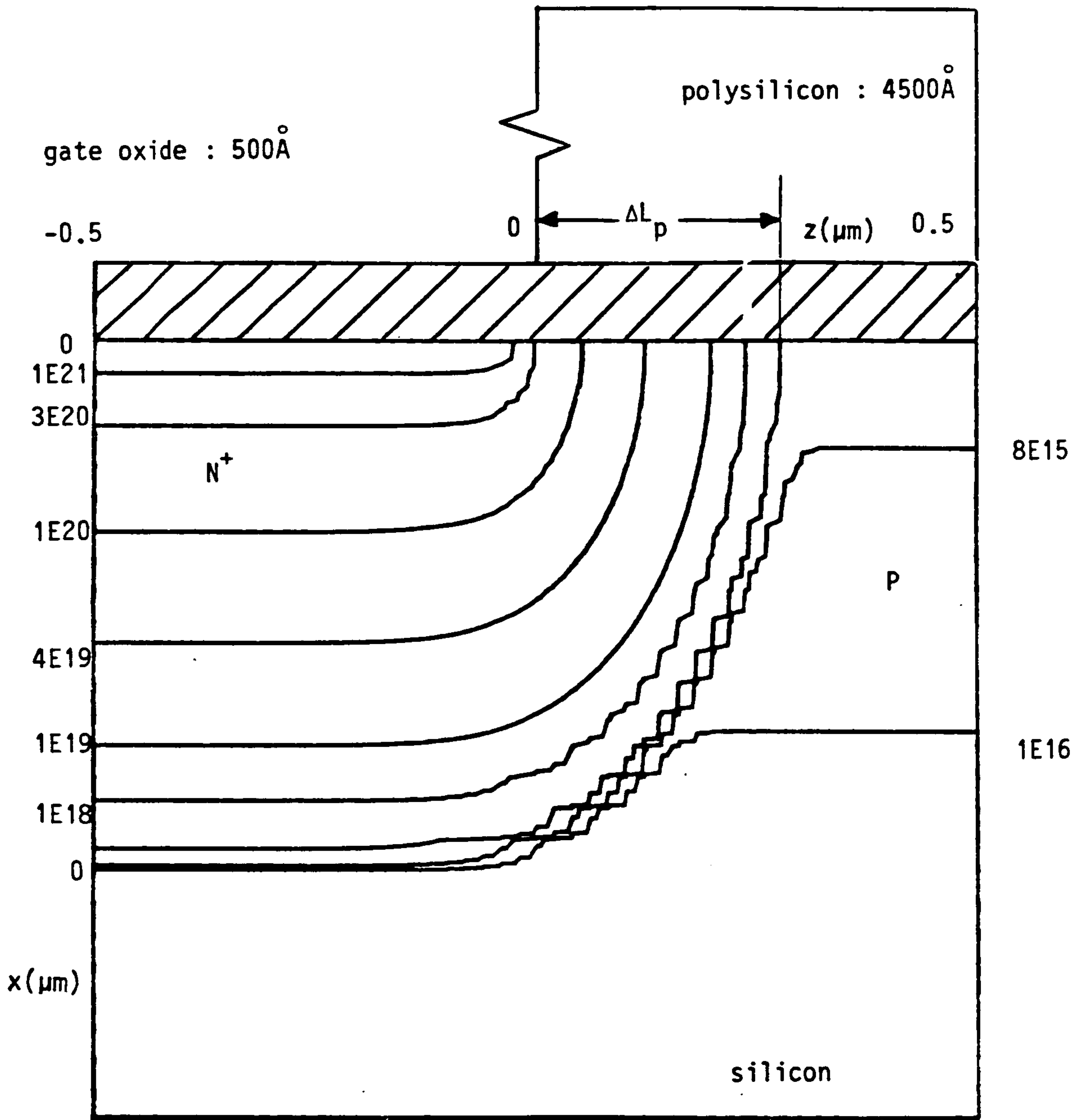


Figure 7.18 : Net profile of NMOSFET (As source/drains) after PSG anneal

14 mins ramp 900 - 1000°C

30 mins at 1000°C

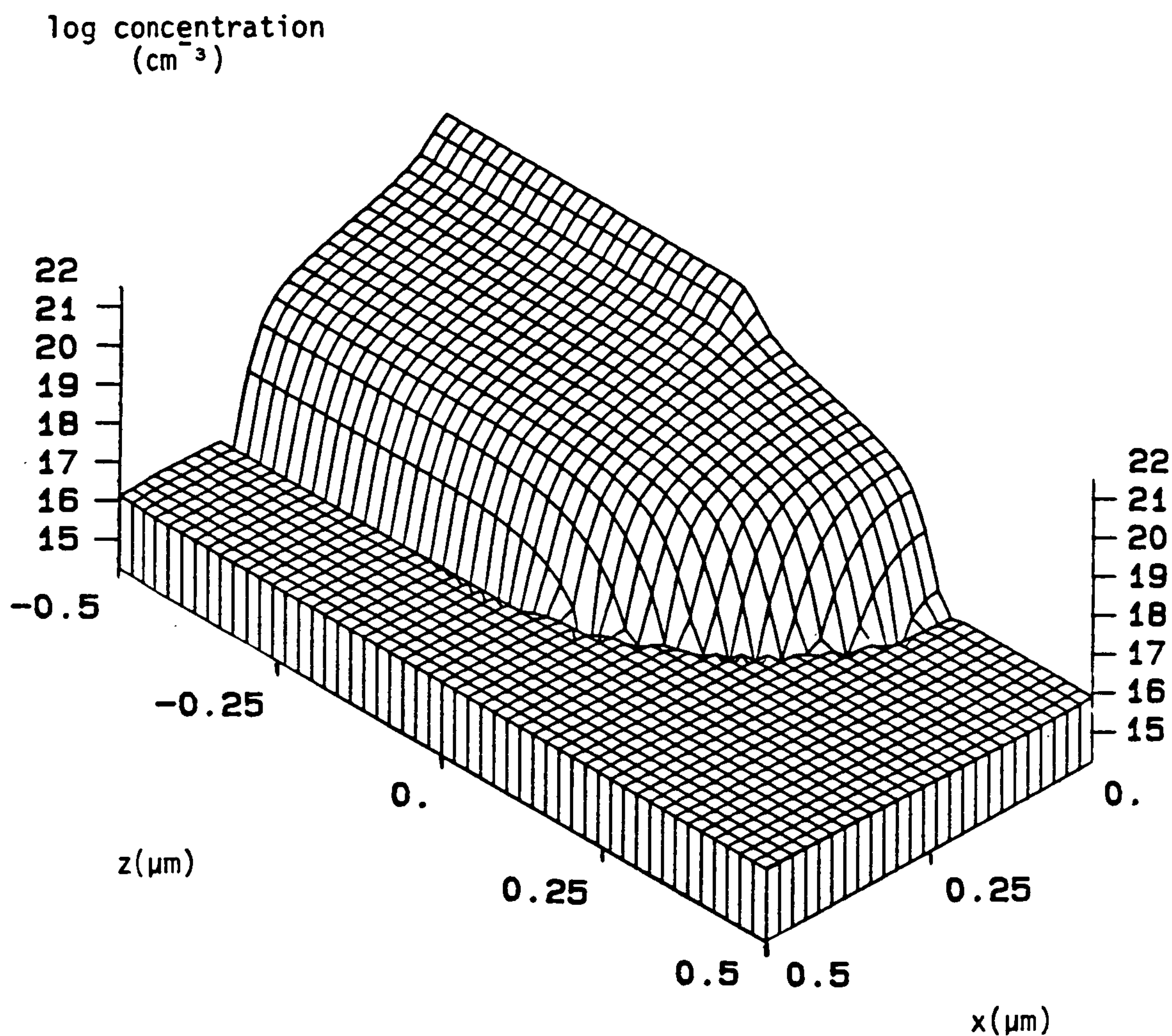


Figure 7.19 : Net profile of NMOSFET (As source/drains) after PSG anneal.

14 mins ramp 900 - 1000°C

30 mins at 1000°C

the distribution shows evidence of inactive arsenic, but the profile changes less abruptly in this region compared with the boron profile of figure 7.11. This difference is due to the fact that the transition from activity to inactivity, as the impurity concentration is increased, is less sudden in the case of arsenic compared to boron. From figure 7.18, the offset ΔL_p is found to be

$$\Delta L_p = 0.55\ \mu m \qquad \text{(NMOS : As source/drain)} \tag{7.36}$$

The values of ΔL_p for each type of MOS transistor are now compared with electrical measurements of devices.

7.6 MEASUREMENT OF EFFECTIVE CHANNEL LENGTH

Several methods of extracting MOSFET channel length from electrical measurements of such devices have been proposed /210-213/. The method of Takacs et al /44/ is easily incorporated into an automated parameter extraction algorithm, and is therefore the one chosen for measurements of effective channel length in this thesis.

The linear region of transistor operation is given by /13/

$$I_{DS} = \frac{W_{eff}}{L_{eff}} \mu C_{OX} (V_{GS} - V_T) V_{DS} \quad ; \quad V_{DS} \ll V_{GS} - V_T \tag{7.37}$$

where I_{DS} is drain-source current, V_{GS} is gate-source voltage, V_{DS}

is drain-source voltage, μ is mobility, W_{eff} is the effective channel width, L_{eff} is the effective channel length and C_{OX} is the oxide capacitance per unit area.

Using (7.1), (7.37) can be written

$$I_{DS} = \frac{B}{(L_{mk} - \Delta L_{mk})} \tag{7.38}$$

where the parameter B is given by

$$B = \mu C_{OX} W_{eff} (V_{GS} - V_T) V_{DS} \tag{7.39}$$

If the quantity B is a constant, then measurements of reciprocal drain source current I_{DS}^{-1} for a variety of transistors, each with a different length L_{mk}, but the same width W_{mk}, should give a straight line plot with intercept ΔL_{mk} on the L_{mk} axis. In practice, even if V_{GS} and V_{DS} are kept constant between measurements, the parameter B is found to vary because the threshold voltage V_T is a function of the transistor length at small geometries /43, 71/. Figure 7.20 shows how measurements of V_T for the transistors used in the simulation examples of this chapter depend on channel length. The modulus of threshold voltage $|V_T|$ decreases with decreasing channel length L_{mk}.

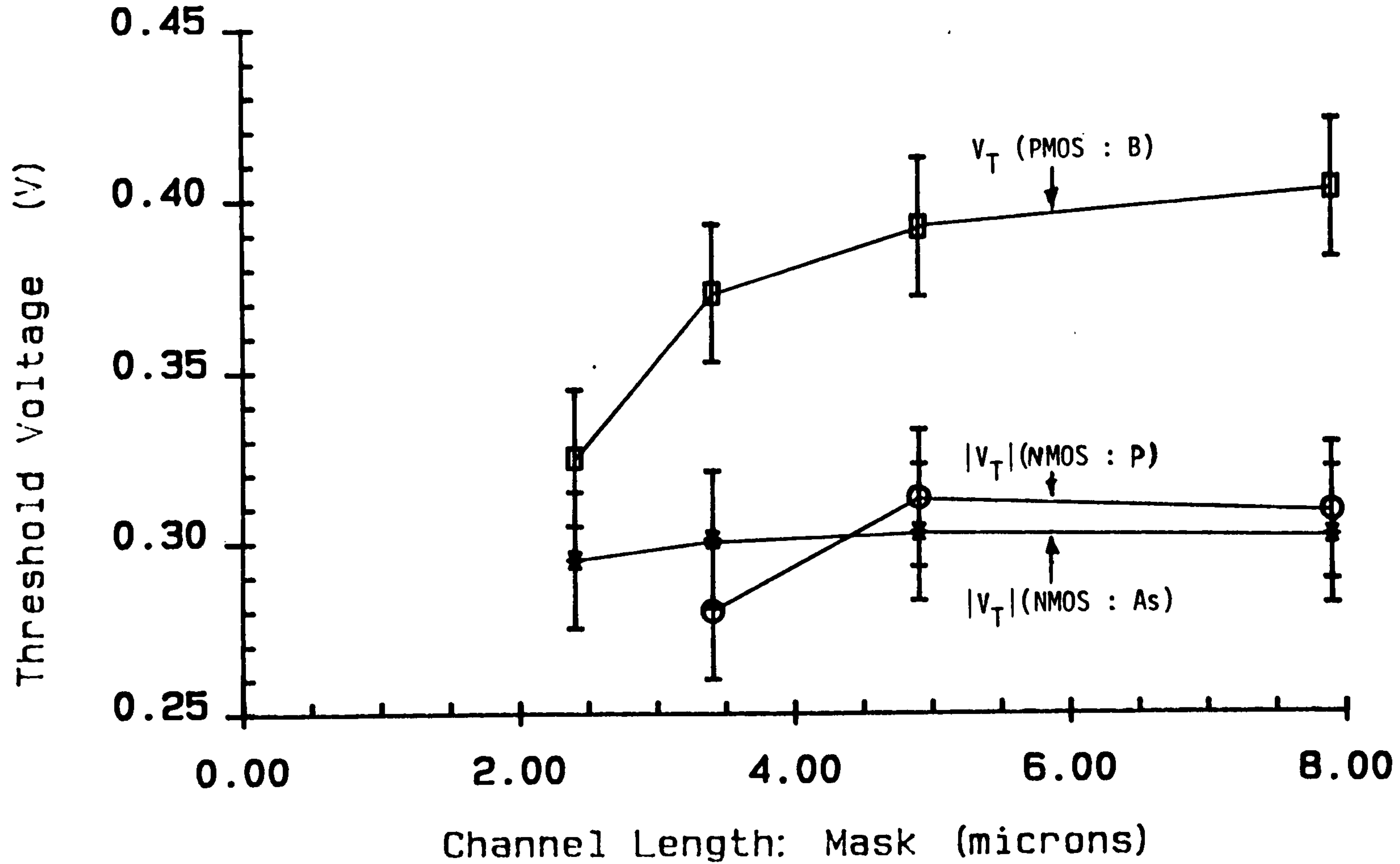


Figure 7.20

This difficulty is overcome by considering, instead of I_{DS}, the transconductance g_m defined by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \bigg|_{V_{DS}} \qquad (7.40)$$

It is well established that /13, 44/ the point of maximum transconductance $g_{m,max}$ scales with V_T, so that a plot of reciprocal peak transconductance $g_{m,max}{}^{-1}$ against mask dimension gives a straight line as shown in figure 7.21. A least squares fit to the data for each transistor type gives the offset ΔL_{mk} (measured) as summarised in table 7.2. The offset ΔL_{mk-p} was found to be negligible and so from (7.2)

$$\Delta L_{mk} = \Delta L_p \qquad (7.41)$$

which allows calculation of the simulated values of ΔL_{mk} in table 7.2.

Within experimental error, the simulated and measured values for ΔL_{mk} agree, in the case of the PMOS transistor and the NMOS transistor with arsenic source/drains. However this cannot be said for the NMOS transistor with phosphorus source/drains which is due to the inadequacy of the ion implantation and diffusion models for phosphorus. From the 1-D diffused profile of figure 4.18 it is clear that EPIC underestimates the extent of the tail of the distribution. The predicted values of vertical junction depth are too low

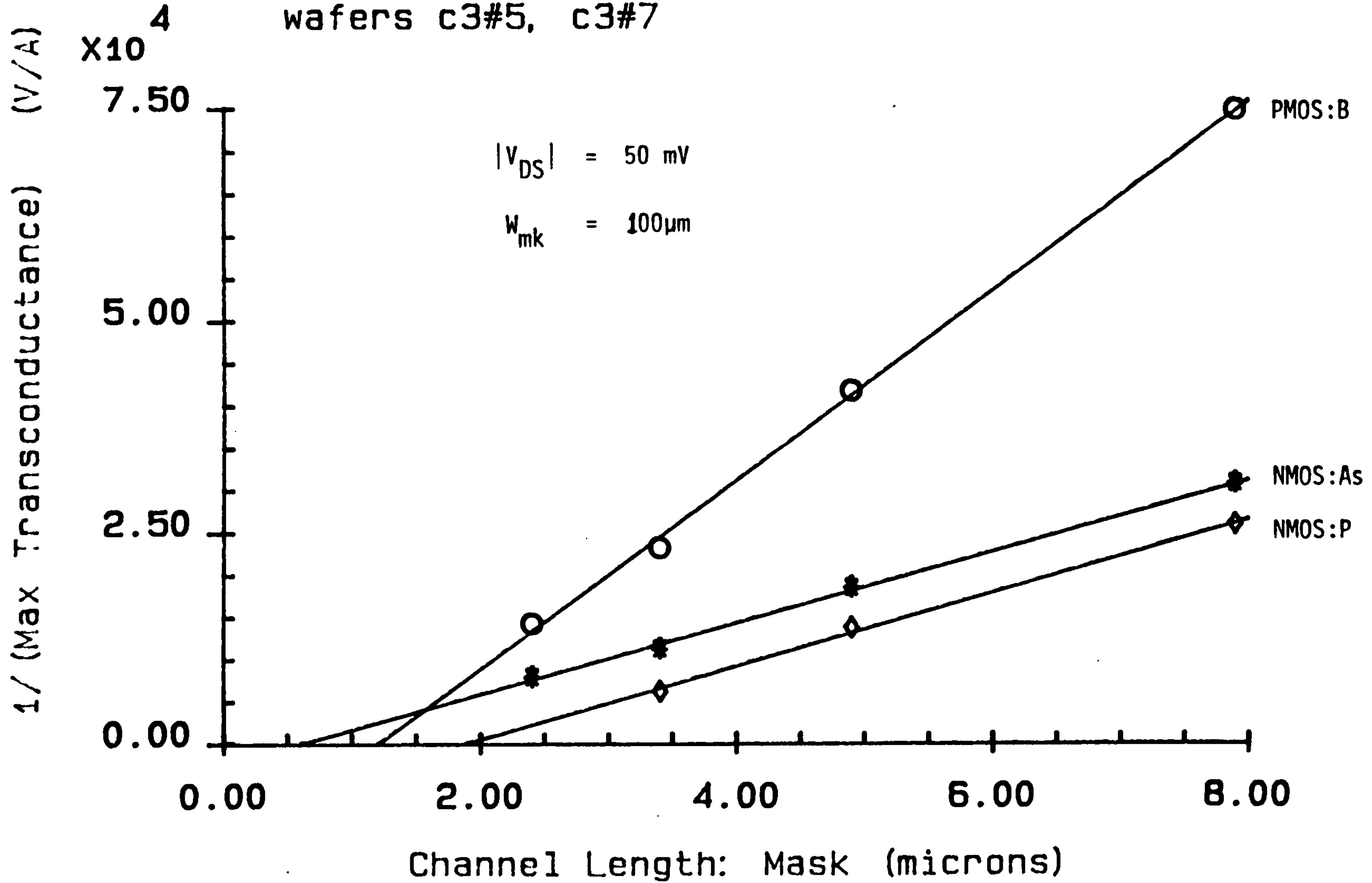


Figure 7.21

MOSFET	ΔL_{mk}(sim.) (μm)	ΔL_{mk}(meas.) (μm)
PMOS : B	1.40	1.20±0.2
NMOS : P	1.45	1.89±0.2
NMOS : As	0.55	0.60±0.2

Table 7.2 : Comparison of simulated and measured values of subdiffusion ΔL_{mk} in MOSFETs.

and, since diffusion is assumed to be isotropic, the simulated lateral junction position is also underestimated. While EPIC is capable of predicting the effective channel length due to subdiffusion of boron and arsenic, a more sophisticated model for phosphorus is required for simulation purposes.

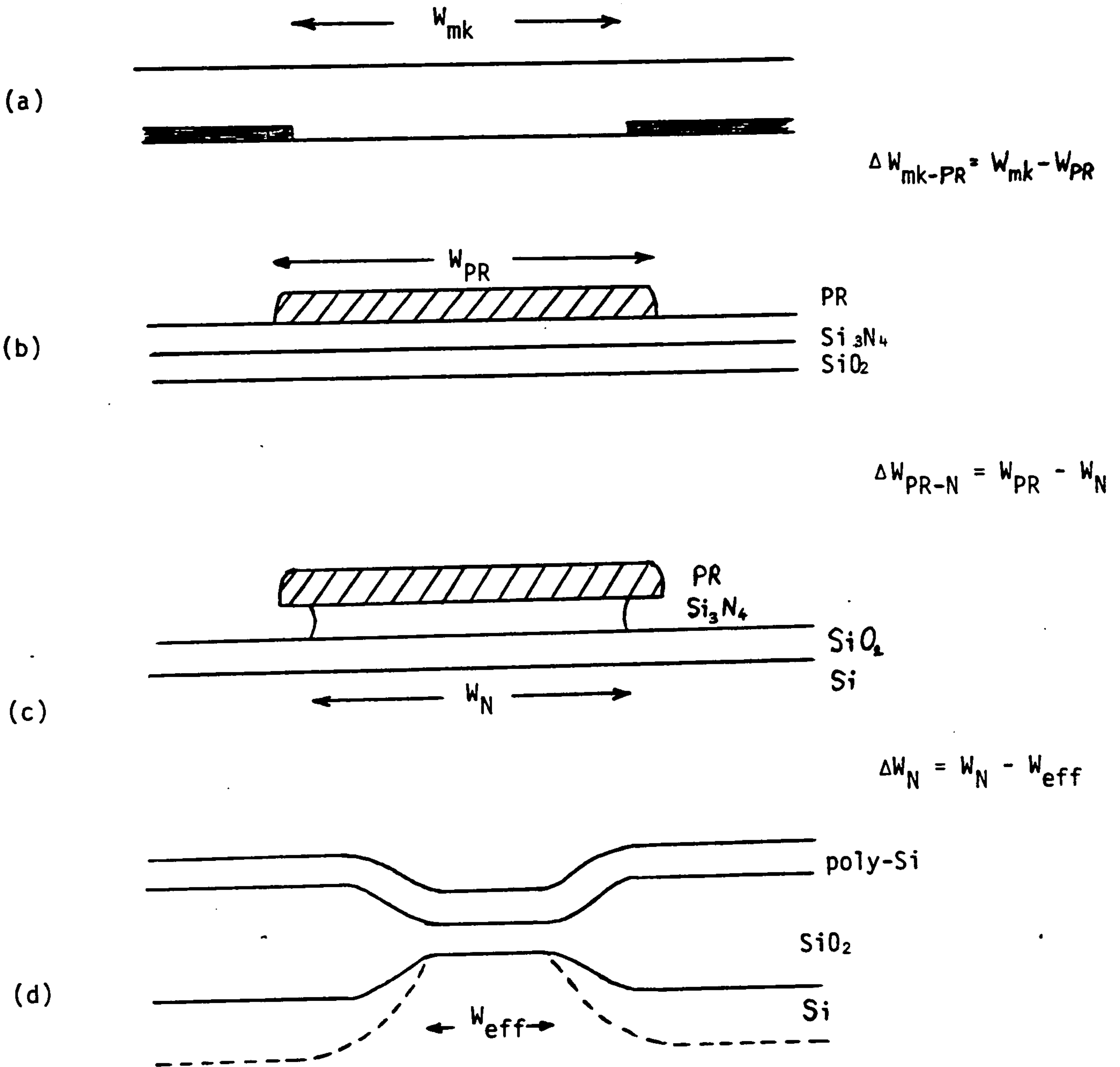
CHAPTER EIGHT : 2-D SIMULATION OF SIMULTANEOUS DIFFUSION AND OXIDATION

8.1 OFFSETS WHICH INFLUENCE EFFECTIVE CHANNEL WIDTH

While Chapter 7 deals with effective channel length L_{eff}, an equally important parameter for circuit design is the effective channel width W_{eff} which, like L_{eff}, directly affects drain-source current I_{DS} and transconductance g_m of the MOS transistor. In a practical situation the final effective channel width is not the same as the dimension defined by the chrome pattern on the mask by virtue of several offsets occurring throughout the process flow. Figure 8.1 shows the main process offsets which affect W_{eff}. ΔW_{mk-PR} represents the offset between the mask dimension and the photoresist dimension, and ΔW_{PR-N} the offset between the photoresist dimension and the patterned silicon nitride track width. Subsequent offsets due to thermal steps, most notably field oxidation, are represented collectively by ΔW_N. The aim of this chapter is to present simulation results for the impurity profile at the end of each process step after the nitride layer is defined. The effective width is therefore given by

$$W_{eff} = W_{mk} - \Delta W_{mk} \tag{8.1}$$

where ΔW_{mk} represents the net offset in MOS transistor width, and



(a) mask
(b) photoresist (PR) developed
(c) silicon nitride etched
(d) final MOSFET cross-section

Figure 8.1 : Process offsets which influence W_{eff}.

with reference to figure 8.1

$$\Delta W_{mk} = \Delta W_{mk-PR} + \Delta W_{PR-N} + \Delta W_{N} \quad (8.2)$$

All linear dimensions must be offset by the quantity ΔW_{mk} in the 'sizing' procedure carried out before maskmaking in order that the widths of transistors specified by the design engineer in a circuit are accurately reproduced on the silicon wafer. ΔW_{mk} can be determined from electrical measurements of MOS transistors. However, in order to predict this offset, a 2-D process simulation is required to model both field oxide growth and impurity redistribution during Local Oxidation of Silicon (LOCOS). The program EPIC is capable of modelling simultaneous diffusion and oxidation, and results are presented below for a p-well CMOS process /31/.

8.2 CURRENT STATUS OF 2-D SIMULTANEOUS DIFFUSION AND OXIDATION MODELLING

Simulation of width effects in MOS devices has been treated by several authors. While ion implantation steps can be simulated relatively easily, any model of the impurity redistribution which takes place during field oxidation is complicated by the moving silicon-silicon dioxide interface.

In the program SUPRA Lee and Dutton /15/ and Chin et al /16/ extend the 1-D profile generated by SUPREM in the field region to 2-D assuming that the lateral diffusion of the field implant is both

independent of impurity segregation at the silicon-oxide boundary and identical to that occurring during a non-oxidising anneal. The mathematical validity of this approach is highly questionable, and in addition, the thermal steps subsequent to field oxidation are totally ignored. Consequently simulation results obtained using this method can be expected to achieve only qualitative accuracy at best in practical situations. Nevertheless examples of NMOS process modelling have been presented /15,16/.

Salsburg and Hansen in FEDSS /17/ use the finite element method to model the diffusion of the boron channel-stop implant during oxidation. While the elements can be stretched to accommodate the moving non-rectangular geometry of the silicon as more oxide is formed, segregation effects of impurities across the oxide-silicon interface are completely neglected. This program has been used in the simulation of a proposed n-well CMOS process at IBM /17/. Although no simulator using finite elements to model impurity redistribution throughout a complete fabrication process has yet been reported, recent work /18/ holds promise for the future.

Taniguchi et al of Toshiba /19/ have used a finite difference method to model impurity redistribution during field oxidation. However, the analysis neglects a component of the impurity flux at the moving oxide-silicon interface, and only accommodates a bird's beak slope of precisely 45° in order to simplify the discretisation procedure. These approximations mean that this method has limited applications for general MOS processes using LOCOS isolation, but

the results generated have been fed to a device simulator to calculate diffused line capacitance.

The most productive method to date has been to apply a time-dependent co-ordinate transformation which maps the real diffusion-oxidation solution domain onto a new area which is both rectangular and stationary. The diffusion equation becomes more complicated on transformation, but is more amenable to solution using a discretisation procedure. Maldonado et al /20,22/ use the method of lines /23/ whereby all independent variables except one are discretised to give a system of ordinary differential equations in time which is solved using previously developed and efficient routines /24/. Results from the program ROMANS II have been presented for a 2 micron n-well CMOS process under development at Rockwell /21,22/.

Other authors using a grid transformation but with a full finite difference discretisation method have included Tielert /25,26/ in Siemens and Penumalli /27-29/ in AT&T Bell Laboratories using the programs LADIS and BICEPS respectively. Also, Seidl /30/ has used a multigrid method to solve the diffusion equation. Each of these authors has presented simulation results of width effects in NMOS technology.

The EPIC program has been used to present the first simulation results of lateral effects in both n-channel and p-channel MOS transistors of a p-well CMOS process /31/. The finite difference method is applied to a transformed system as described above. The

authors reviewed have used a uniform rectangular discretisation grid to model the redistribution of the channel-stop implant through the steps of either an NMOS or n-well CMOS fabrication process. This approach is not tractable in the case of a p-well CMOS process. In this case a non-uniform rectangular mesh must be used to accommodate not only the boron of the field implant, but also the extent of the p-well in the vertical direction as seen from figure 6.16. In addition all previous simulation activity has included the use of a concentration-dependent diffusion coefficient, which, for the low concentration values typical of both field and threshold tailoring implants, requires unnecessary calculation of both field-enhancement and vacancy-enhancement factors. It is therefore justified to assume a constant diffusivity D (including the effects of OED) to model width effects in MOS transistors. A more accurate treatment would involve first solving the diffusion equation for silicon self-interstitials generated during oxidation, then calculating a spatially dependent OED factor to use in the solution of dopant diffusion /26,32,75/.

8.3 A 2-D MODEL FOR DIFFUSION DURING OXIDATION

The physical models used for the diffusion and oxidation steps in EPIC are the same as those used by SUPREM II, but extended to 2-D assuming isotropy. Because doping levels are low, a constant diffusion coefficient D, accounting for OED is assumed. The partial differential equation (PDE) representing Fick's Law of Diffusion (8.3) must be solved subject to an initial condition given by

the doping profile at the end of the last process step, and boundary conditions (BC's) (8.4) - (8.7) where figure 8.2 defines the coordinate system used.

$$\frac{\partial N}{\partial t} = D \nabla^2 N \tag{8.3}$$

$$N\left(\frac{k}{\alpha} - 1\right) \dot{X}_n = D \frac{\partial N}{\partial n} \quad ; \quad x = X(y,t) \tag{8.4}$$

$$N = N_{sub} \quad ; \quad x = x_m + X(y,t) \tag{8.5}$$

$$\frac{\partial N}{\partial y} = 0 \quad ; \quad y = -y_m \tag{8.6}$$

$$\frac{\partial N}{\partial y} = 0 \quad ; \quad y = y_m \tag{8.7}$$

The segregation coefficient k, given by

$$k = \left.\frac{N_{ox}}{N}\right|_{x = X(y,t)} \tag{8.8}$$

relates the concentration of the impurity N on the silicon side of the moving interface $x = X(y,t)$ to that on the side of the oxide N_{ox}. α is the amount of silicon consumed to produce one unit of silicon dioxide, n denotes distance normal to the interface, $\dot{X}_n$ is the velocity of the interface in the normal direction, and N_{sub} is the concentration of the dopant in the starting material. The inhomogeneous Neumann boundary condition (8.4) quantifies the impurity flux normal to the moving silicon-dioxide interface. Seidl /33/ gives a lucid mathematical derivation of this equation which assumes that impurity diffusion in the oxide can be neglected. The validity of this simplification has not been tested in the literature, so,

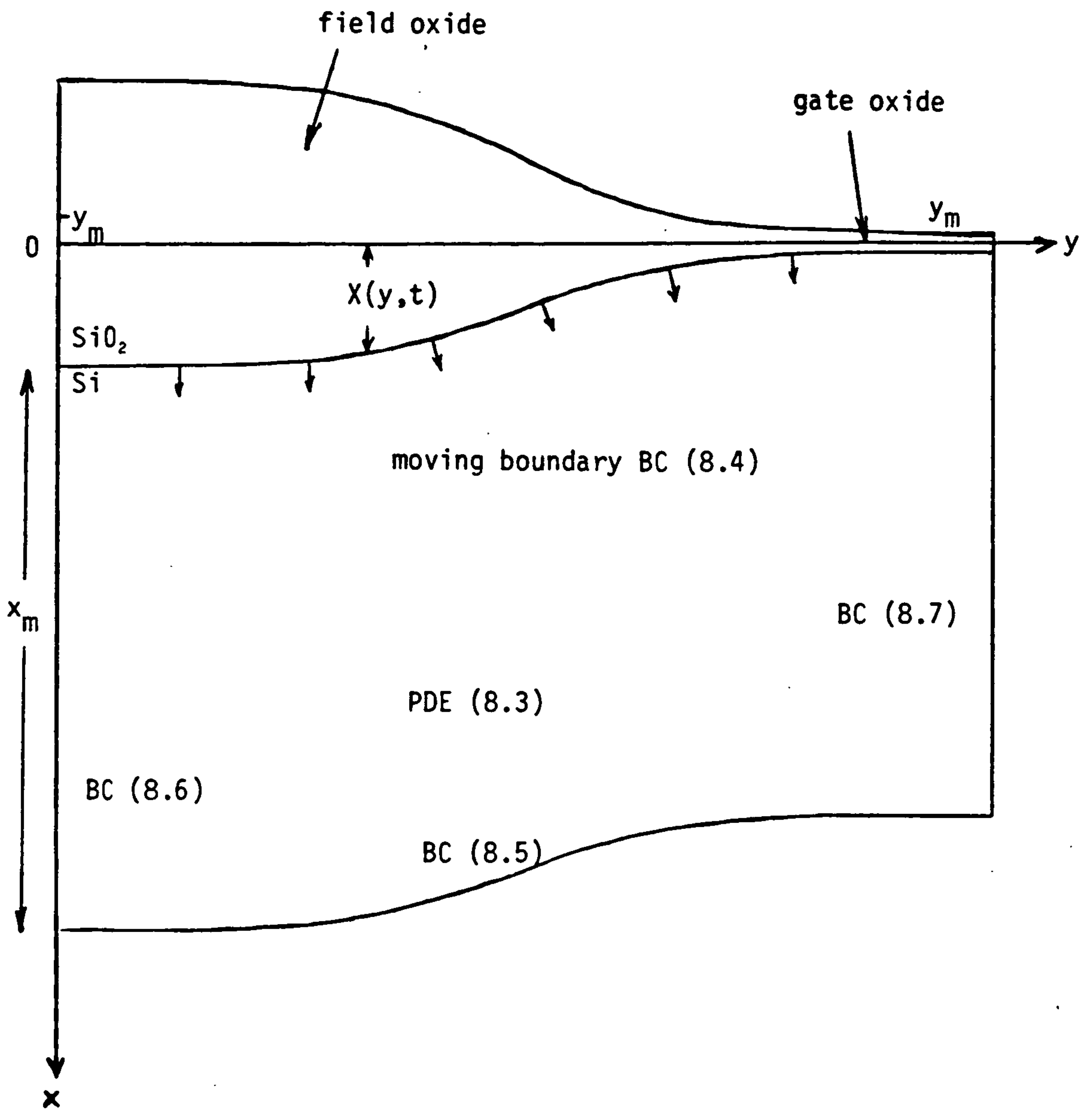


Figure 8.2 : 2-D simulation domain in (x,y) plane.

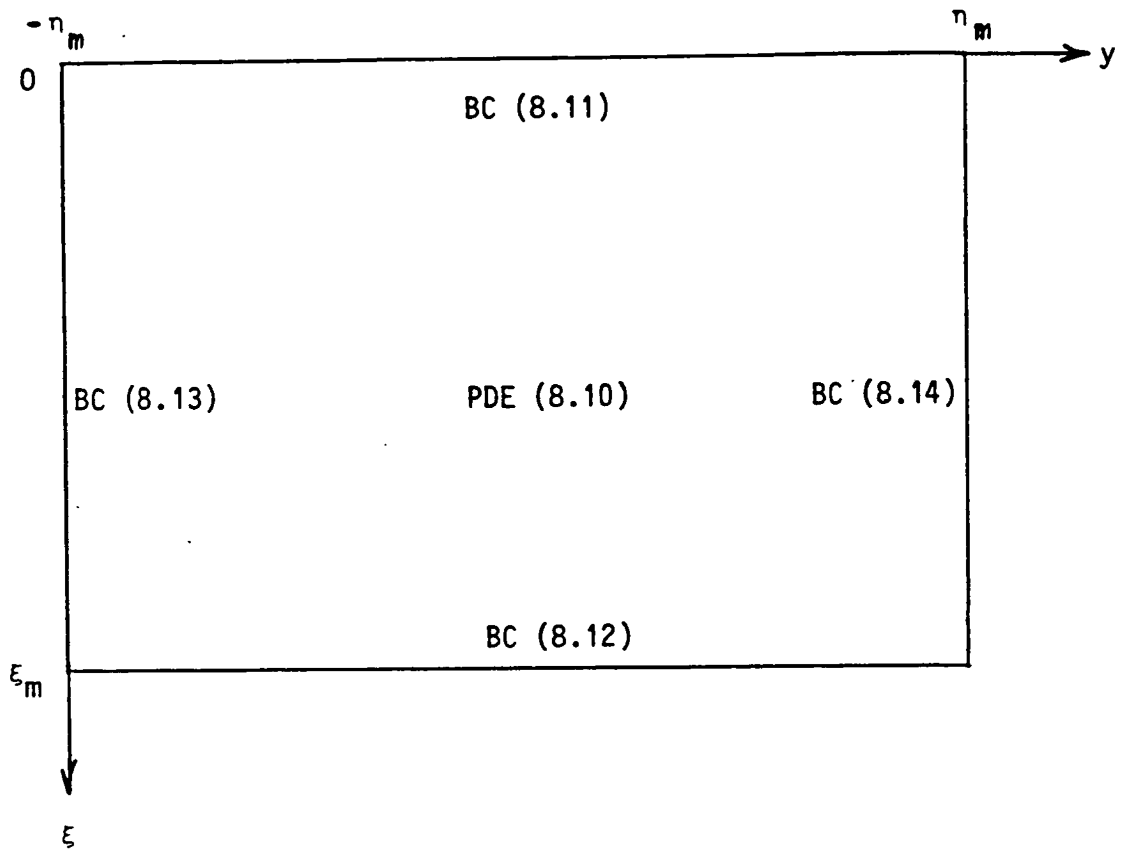


Figure 8.3 : 2-D transformed simulation domain in (ξ,η) plane.

as a preliminary check, the results of EPIC in 1-D are compared with the results of SUPREM below. The boundary condition (8.5) ensures that the doping level remains fixed in the bulk of the wafer and the value of N_{sub} is deduced from electrical resistivity measurements of the starting material /13/. Reflecting boundary conditions (8.6), (8.7) are assumed in the lateral directions.

A co-ordinate transformation /27/

$$\xi = x - X(y,t) \tag{8.9a}$$

$$\eta = y \tag{8.9b}$$

$$\tau = t \tag{8.9c}$$

is applied to map the real co-ordinate system (x,y,t) onto a new system (ξ,η,τ) in which the solution domain is now rectangular and time-invariant, as shown by figure 8.3. The transformed diffusion equation is given by /31/

$$\frac{\partial N}{\partial \tau} = (\dot{X} - DX'')\frac{\partial N}{\partial \xi} + D \{1 + (X')^2\} \frac{\partial^2 N}{\partial \xi^2}$$

$$+ D \frac{\partial^2 N}{\partial \eta^2} - 2X'D \frac{\partial^2 N}{\partial \xi \partial \eta} \tag{8.10}$$

and the corresponding boundary conditions are

$$N(\frac{k}{\alpha} - 1) \dot{X} = D[\frac{\partial N}{\partial \xi}\{1+(X')^2\} - X'\frac{\partial N}{\partial \eta}] \quad ; \xi = 0 \tag{8.11}$$

$$N = N_{sub} \quad ; \quad \xi = \xi_m \tag{8.12}$$

$$\frac{\partial N}{\partial \eta} = 0 \quad ; \quad \eta = -\eta_m \tag{8.13}$$

$$\frac{\partial N}{\partial \eta} = 0 \quad ; \quad \eta = \eta_m \tag{8.14}$$

where $\dot{X} = \frac{\partial X}{\partial \tau}$, $X' = \frac{\partial X}{\partial \eta}$ and $X'' = \frac{\partial^2 X}{\partial \eta^2}$.

Equations (8.10) - (8.14) constitute an initial-boundary value problem which is discretised using the finite difference method with a non-uniform mesh as shown in figure 8.4. Difference approximations to the partial derivatives are based on first order Taylor expansions applied to the nine point star of figure 8.5, which shows the (i,j)th node and its eight nearest neighbours. Nine points are required as opposed to the more usual five because of the existence of a second order mixed derivative term in (8.10). As in the high concentration diffusion model of Chapter 7, central differences are used for the diffusive terms.

Tielert /26/ has used central differences for the advective terms also, but in EPIC this approach was found to be inadequate. One-sided 'upwind' differences are imperative in order that numerical disturbances, which are bound to occur due to round-off errors, flow only in the direction of the advective velocity i.e. 'downstream'/31/. Roache refers to this condition as the 'transportative property' /34/ in his discussion of the vorticity transport equation of fluid dynamics. Gauss' divergence theorem can be used to prove that upwind differencing is in fact conservative /34/.

The full spatial discretisation at the (i, j)th node is given by /31/

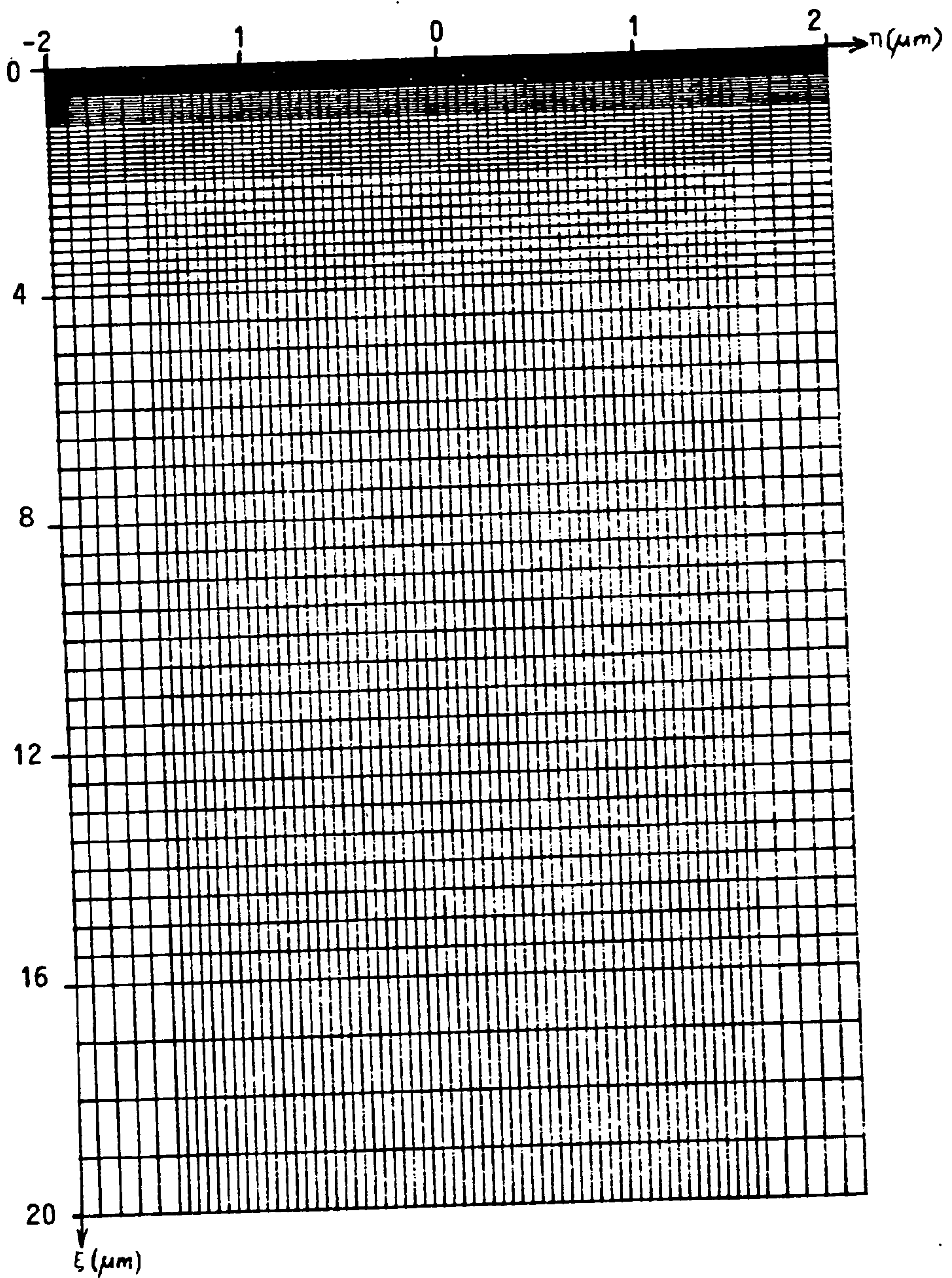
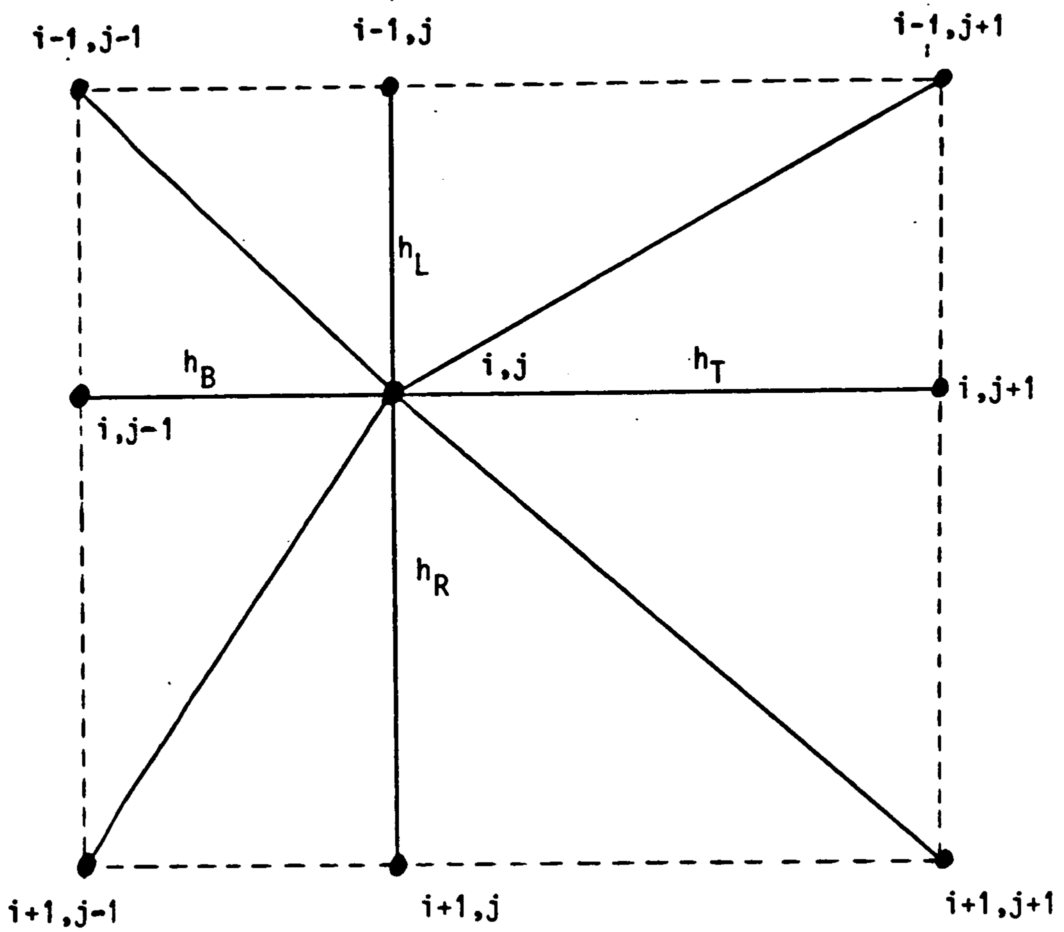
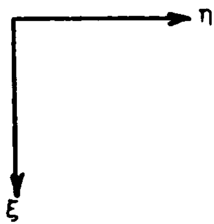


Figure 8.4 : Non-uniform grid for finite difference method.





$$h_L = \xi_i - \xi_{i-1}$$
$$h_R = \xi_{i+1} - \xi_i$$
$$h_B = \eta_i - \eta_{i-1}$$
$$h_T = \eta_{i+1} - \eta_i$$

Figure 8.5 : Nine-point finite difference star.

$$\Gamma_{i,j,n} =$$

$$(\dot{X}_{j,n} - DX_{j,n}{''}) \frac{N_{i+1,j,n} - N_{i,j,n}}{h_R}$$

$$+ 2D \{1 + (X'_{j,n})^2\} \{\frac{1}{h_L(h_L + h_R)} N_{i-1,j,n} - \frac{1}{h_L h_R} N_{i,j,n}$$

$$+ \frac{1}{h_R(h_L + h_R)} N_{i+1,j,n})\}$$

$$+ 2D \{ \frac{1}{h_B(h_B + h_T)} N_{i,j-1,n} - \frac{1}{h_B h_T} N_{i,j,n} + \frac{1}{h_T(h_B + h_T)} N_{i,j+1,n}\}$$

$$- \frac{2DX_{j,n}{'}}{(h_L + h_R)(h_B + h_T)} \{N_{i+1,j+1,n} - N_{i+1,j-1,n} + N_{i-1,j-1,n} - N_{i-1,j+1,n}\}$$

$$; \quad DX_{j,n}{''} - \dot{X}_{j,n} < 0 \quad ; \quad i = 0\ (1)M,\ j = 0\ (1)S. \qquad (8.15a)$$

$$\Gamma_{i,j,n} =$$

$$(\dot{X}_{j,n} - DX_{j,n}{''}) \frac{N_{i,j,n} - N_{i-1,j,n}}{h_L}$$

$$+ 2D \{1 + (X_{j,n}{'})^2\} \{\frac{1}{h_L(h_L + h_R)} N_{i-1,j,n} - \frac{1}{h_L h_R} N_{i,j,n}$$

$$+ \frac{1}{h_R(h_L + h_R)} N_{i+1,j,n}\}$$

$$+ 2D \{\frac{1}{h_B(h_B + h_T)} N_{i,j-1,n} - \frac{1}{h_B h_T} N_{i,j,n} + \frac{1}{h_T(h_B + h_T)} N_{i,j+1,n}\}$$

$$- \frac{2DX_{j,n}{'}}{(h_L + h_R)(h_B + h_T)} \{N_{i+1,j+1,n} - N_{i+1,j-1,n} + N_{i-1,j-1,n} - N_{i-1,j+1,n}\}$$

$$; \quad DX_{j,n}{''} - \dot{X}_{j,n} \geqslant 0 \quad ; \quad i = 0\ (1)M,\ j = 0\ (1)S. \qquad (8.15b)$$

where the subscript n refers to a specific time level. Equation (8.15a) uses a forward difference for the advective term while (8.15b) uses a backward difference. The Dirichlet type boundary condition (8.12) undergoes trivial discretisation to become (8.17). The Neumann type boundary conditions (8.11), (8.13), (8.14) are discretised to (8.16), (8.18), (8.19) respectively using virtual nodes outside the simulation area.

$$N_{-1,j,n} = N_{1,j,n} - \frac{(h_L + h_R)}{D\{1 + (X_{j,n}')^2\}} \{N_{o,j,n} (\frac{k}{\alpha} - 1) \dot{X}_{j,n}$$

$$+ DX_{j,n}' \frac{N_{o,j+1,n} - N_{o,j-1,n})}{(h_B + h_T)}\} ;j = 0(1)S \qquad (8.16)$$

$$N_{M,j,n} = N_{sub} \qquad ; \qquad j = 0(1)S \qquad (8.17)$$

$$N_{i,-1,n} = N_{i,1,n} \qquad ; \qquad i = 0(1)S \qquad (8.18)$$

$$N_{i,S+1,n} = N_{i,S-1,n} \qquad ; \qquad i = 0(1)S \qquad (8.19)$$

Initial attempts to extend the Crank-Nicolson method (used in chapter 7) to the simultaneous diffusion and oxidation problem proved to be only partially successful. A Gauss-Seidl iterative scheme /23,35/ was used to solve the resulting matrix equation, but convergence to the solution was found to be too slow for practical purposes. Over-relaxation of the residual did not result in accelerated convergence. Therefore, efficient use of the Crank-Nicolson method to solve this problem requires a more detailed study of techniques to solve large sparse linear systems. Instead an explicit difference scheme was used in EPIC for all diffusion simula-

tions in the transformed system /31/. The discretised transport equation becomes

$$\frac{N_{i,j,n+1} - N_{i,j,n}}{\delta t} = \Gamma_{i,j,n} \tag{8.20}$$

To avoid numerical instability, the time step δt must be limited to some critical value which is difficult to estimate from theoretical considerations, and best found by trial and error.

In order to test the accuracy of the diffusion-oxidation model, comparisons are made in 1-D with results generated by SUPREM. In the examples presented, EPIC assumes complete symmetry in the lateral direction in the wafer, ie no variation in oxide thickness or impurity concentration in the y-direction. In each case a silicon wafer with a uniform doping concentration of 10^{15} cm^{-3} is oxidised assuming the SUPREM default models for both diffusion and oxidation. While EPIC neglects diffusion of impurity species in the oxide, diffusion in both oxide and silicon is modelled by SUPREM.

Figures 8.6 and 8.7 show a comparison of results at a temperature of $900^{o}C$ for oxidation times of 20 mins and 3 hrs respectively. Boron is segregated into the oxide, depleting the region of silicon near the surface of the wafer. The depth axis is referenced to the oxide-silicon interface. The corresponding comparisons at the higher temperature of $1100^{o}C$ are shown in figures 8.8 and 8.9. The agreement between EPIC and SUPREM is clearly good at both diffusion temperatures. Boron can be adequately simulated at $900^{o}C$ using a minimum mesh spacing of about 0.01 micron at the silicon

FIGURE 8.6 : SUPREM-EPIC COMPARISON

Oxidation at 900°C for 20 mins

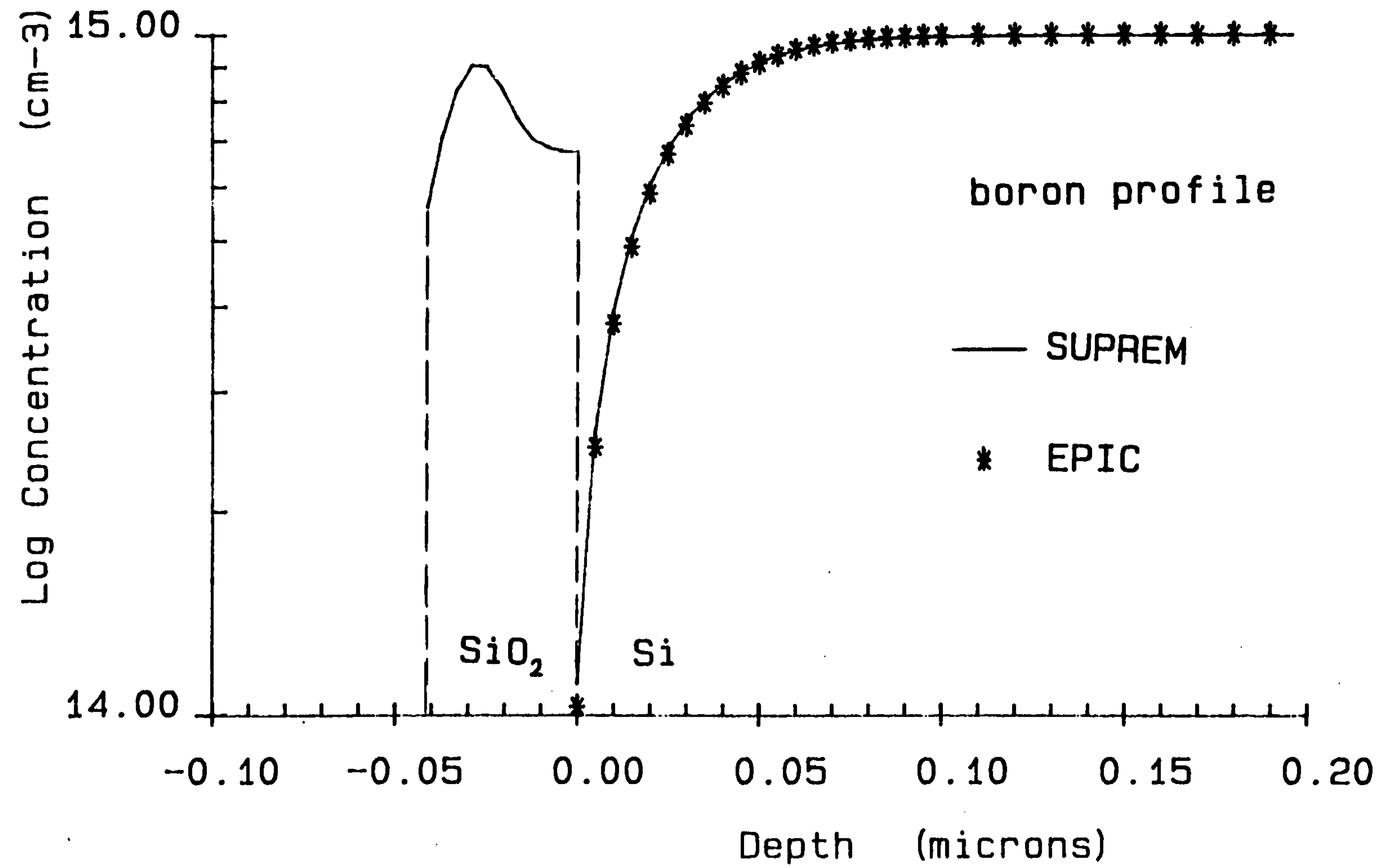


FIGURE 8.7 : SUPREM-EPIC COMPARISON

Oxidation at 900°C for 3 hours

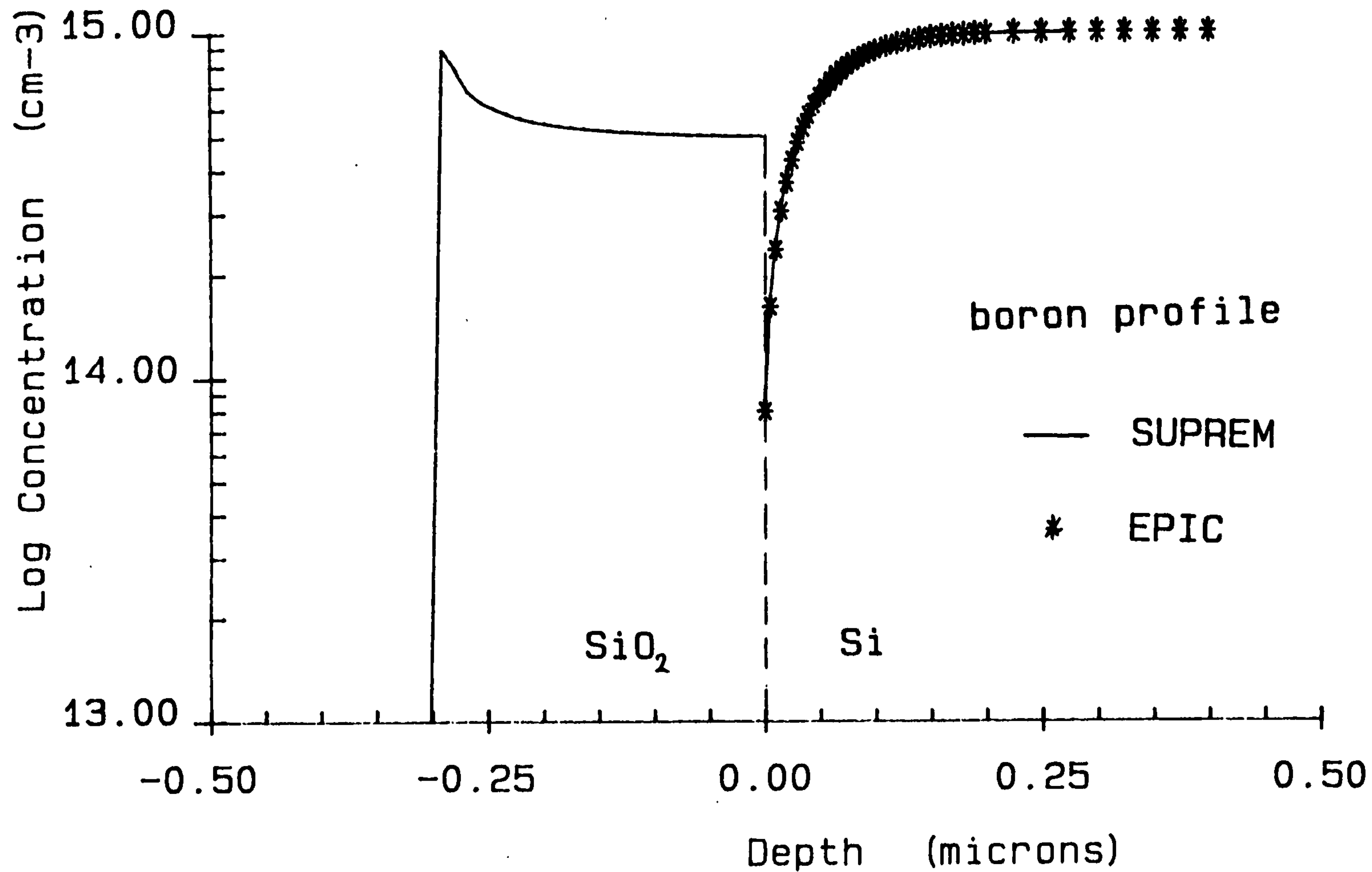


FIGURE 8.8 : SUPREM-EPIC COMPARISON

Oxidation at 1100°C for 20 mins

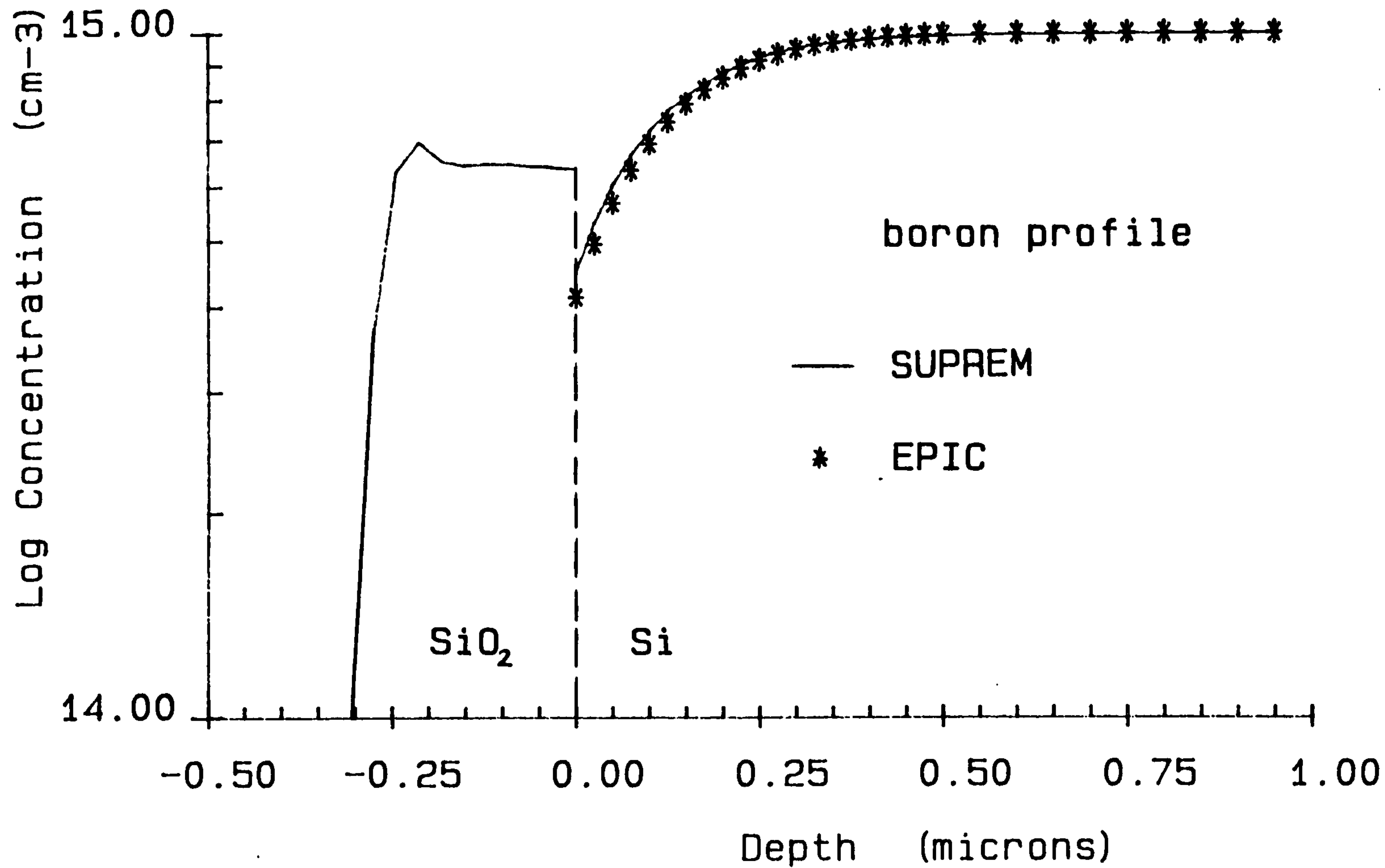


FIGURE 8.9 : SUPREM-EPIC COMPARISON

Oxidation at 1100°C for 3 hours

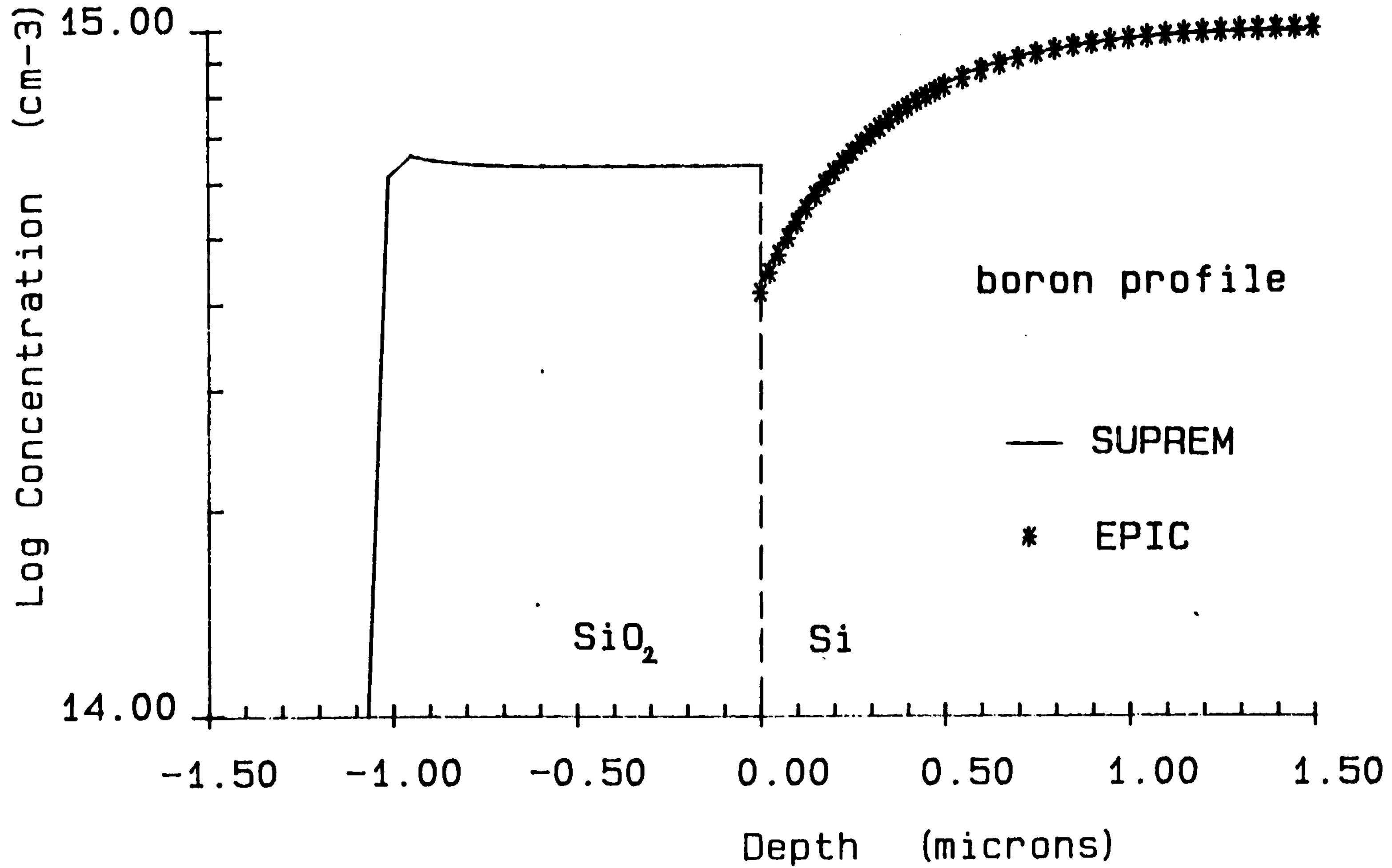


FIGURE 8.10 : SUPREM-EPIC COMPARISON

Oxidation at 900°C for 20 mins

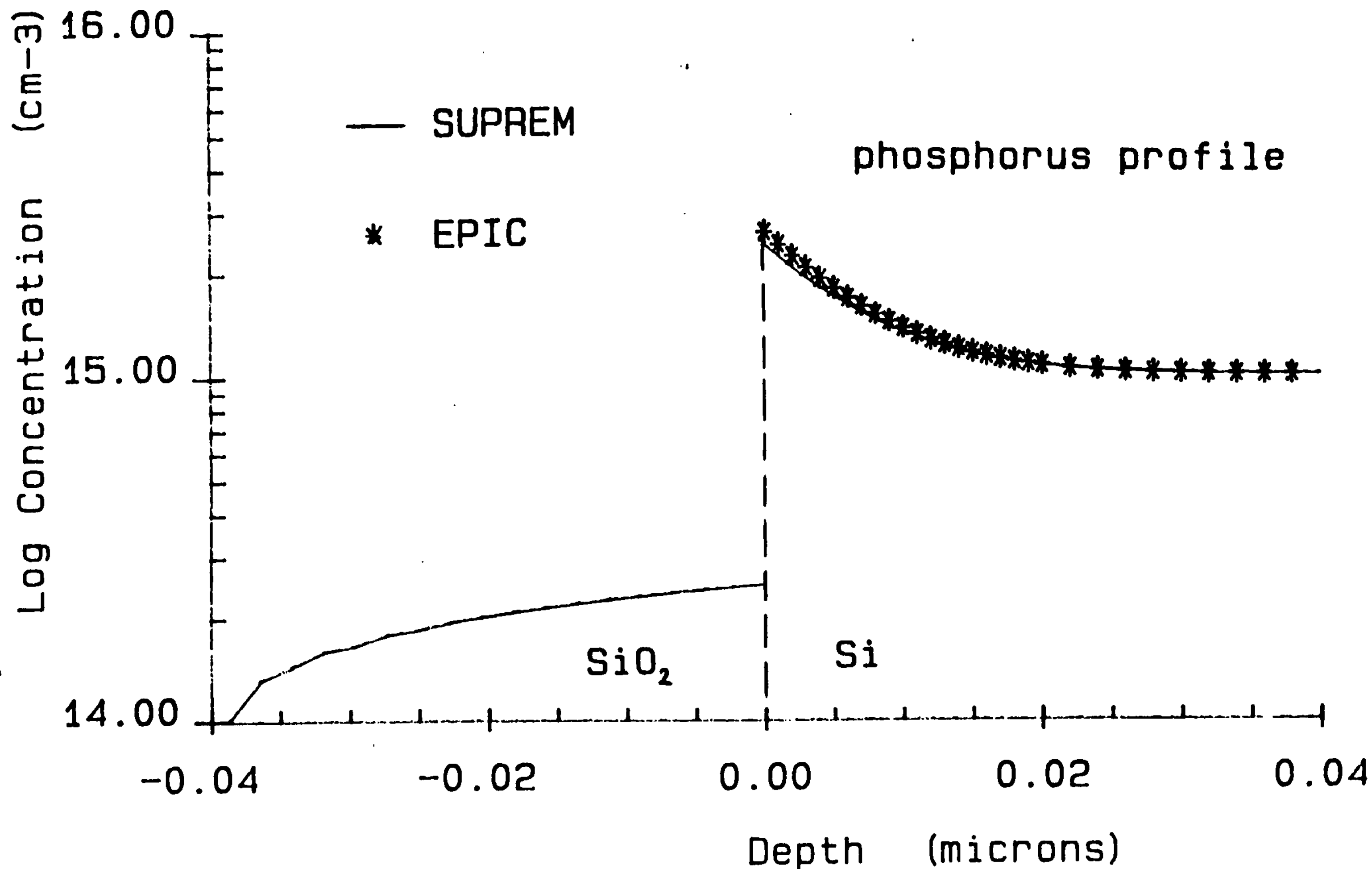
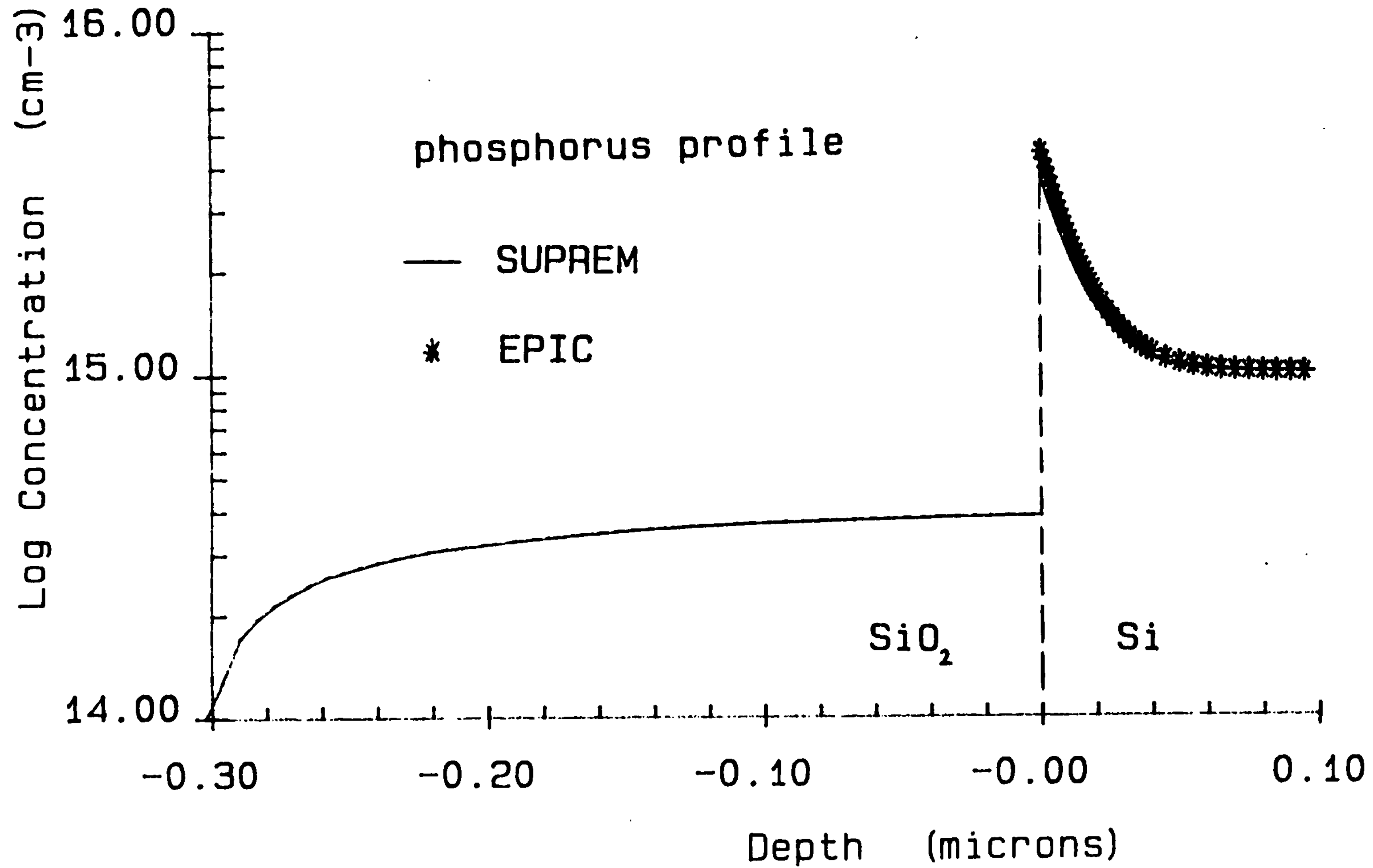


FIGURE 8.11 : SUPREM-EPIC COMPARISON

Oxidation at 900°C for 3 hours



surface. However, it is found that in the case of phosphorus which tends to pile up in the silicon during oxidation, a mesh spacing of the order of 0.001 micron or 10Å is required to properly accommodate the rapidly-varying impurity profile as shown by figures 8.10 and 8.11.

Although this comparison is only one-dimensional, the good agreement between the two simulators means that the EPIC model can be confidently used in its two-dimensional form, provided the discretisation mesh is sufficiently fine to accommodate the concentration gradients. Simulation results of width effects throughout a complete p-well CMOS process are now presented /31/.

8.4 SIMULATION RESULTS FOR A P-WELL CMOS PROCESS

Table 8.1 shows the process flow of the p-well CMOS process under consideration. Steps like source/drain implantation which do not influence the doping profile in this part of the wafer are omitted.

Taking advantage of symmetry in the y-direction, SUPREM is used to simulate the process in 1-D until after nitride layer deposition. Figure 8.12 shows the diffused p-well region in the n-substrate. The first two-dimensional process step consists of the boron field implant which is performed through the pad oxide layer of thickness X_p into the p-well field region, the active device region being partially masked by the patterned silicon nitride layer.

FIGURE 8.12 : SUPREM Results for P-well Formation

wafer c2#17

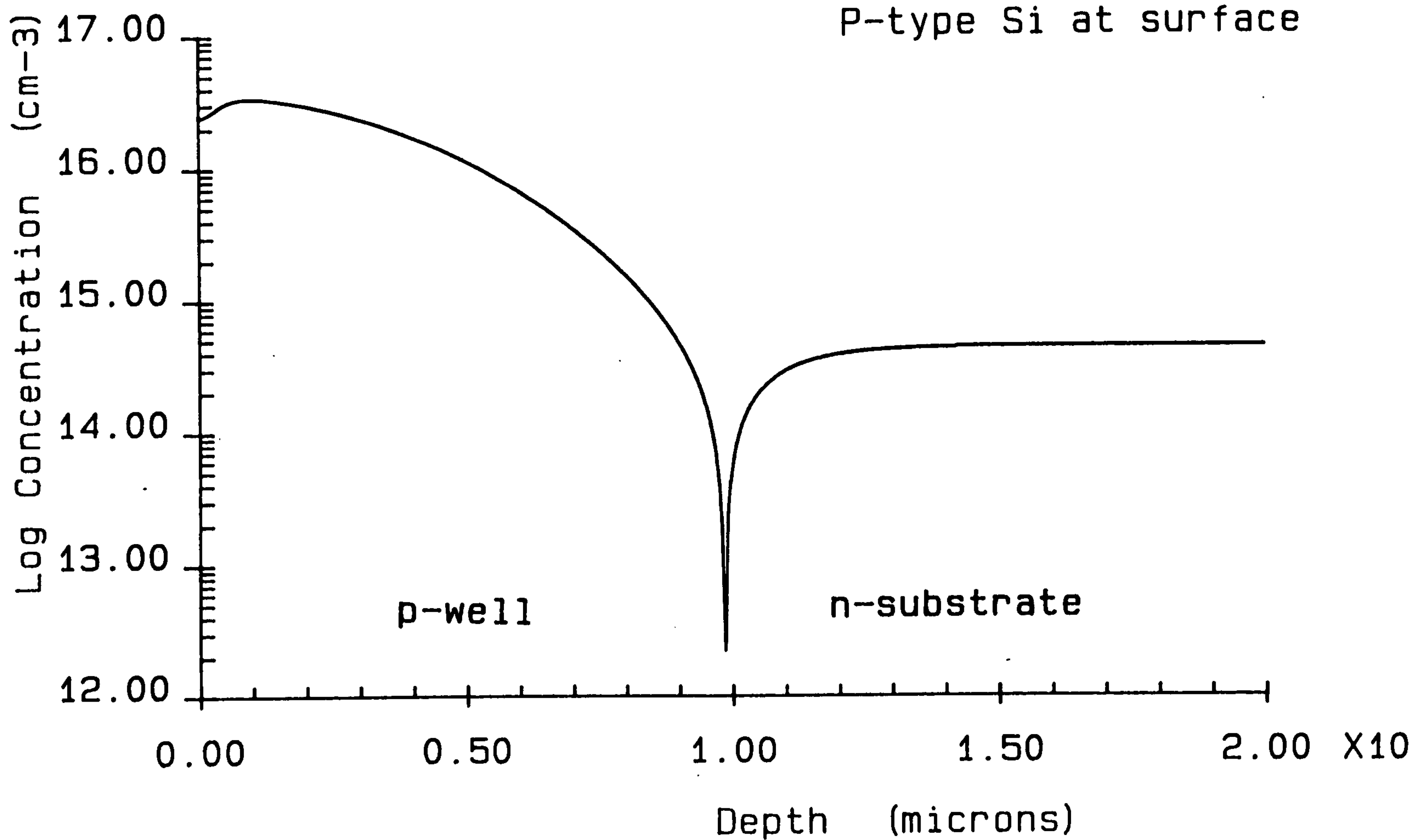


Figure 8.13 shows an equidensity plot of the boron concentration where the scale bars in both x and y directions indicate a distance of 1 micron. The diffusion of boron and phosphorus is assumed to be independent, and so only the boron in the p-well will be considered initially. In the plots to follow, only the surface portion of silicon is shown because the doping profiles in the bulk of the simulation area do not exhibit any lateral variation. Where the contour lines are straight lines, the profile is essentially one-dimensional and can therefore be adequately modelled by SUPREM.

The diffusion of the field or channel-stop implant during the inert drive-in step performed at $1025^{o}C$ for 500 mins is modelled using the analytical method of Chapter 6. Because the low concentration diffusion equation (8.3) is linear, the diffusion of the field implant can be modelled separately from the rest of the p-well which can be modelled by SUPREM because of the symmetry in the y-direction. The total profile is simply the sum of the two parts as shown by figure 8.14. A synthesis of solutions in this manner avoids a full 2-D numerical treatment at this point in the process, and hence reduces execution times /31/. As well as diffusing further into the bulk, the boron extends further under the masking nitride edge into the active device region.

An empirical fit is used to model the position of the interface $x = X_F(y,t)$ between the field oxide and silicon. Following Penumalli /27,28/ the functional form of (8.21) is used in EPIC.

$$X_F(y,t) = \frac{T_F(t)}{2} \quad \text{erfc} \left\{ \frac{\sqrt{2}y}{k_1 T_F(t)} \right\} \tag{8.21}$$

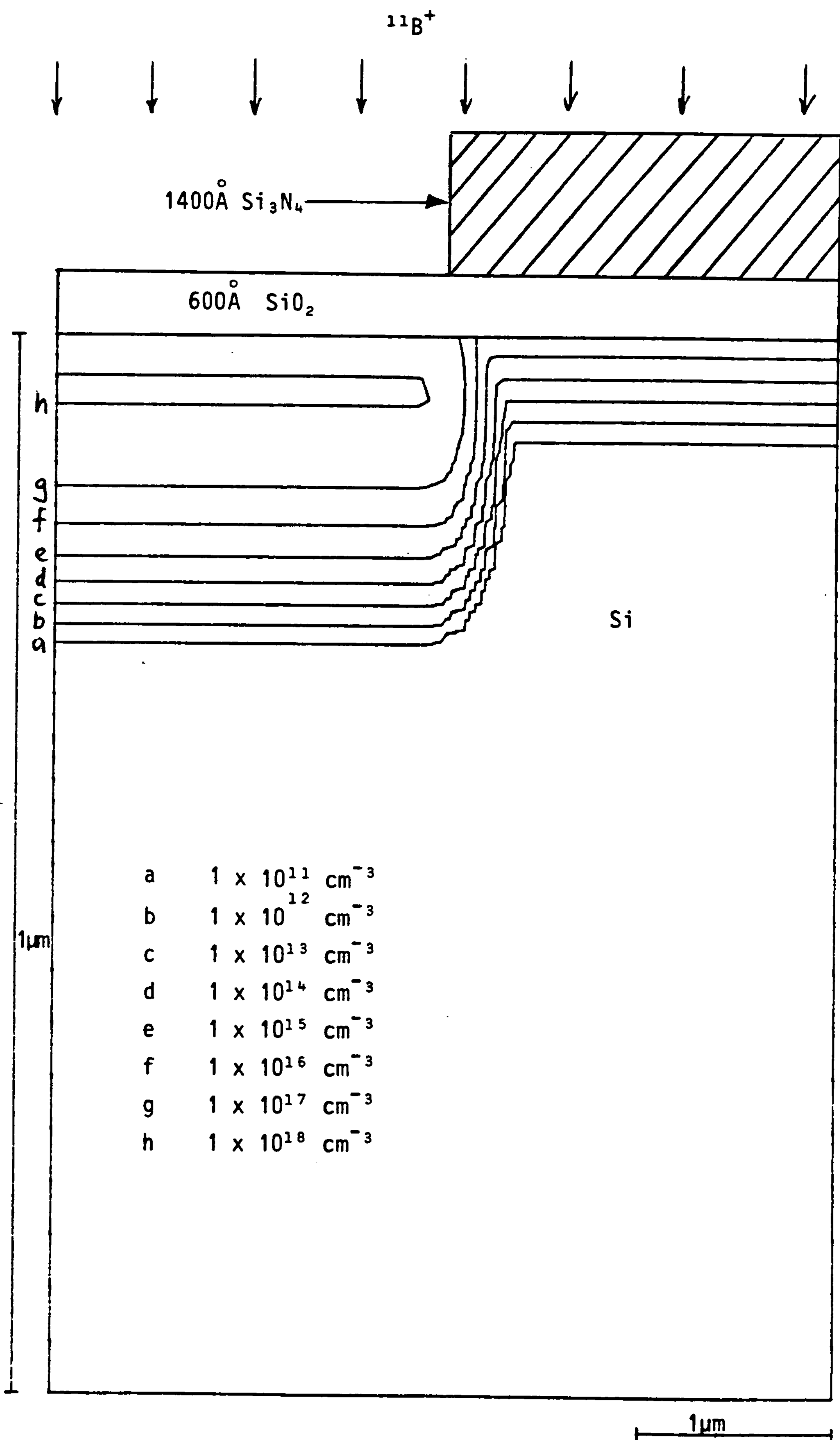


Figure 8.13 : Field implant into p-well
1.1×10^{13} cm^{-2} $^{11}B^{+}$ at 35 keV

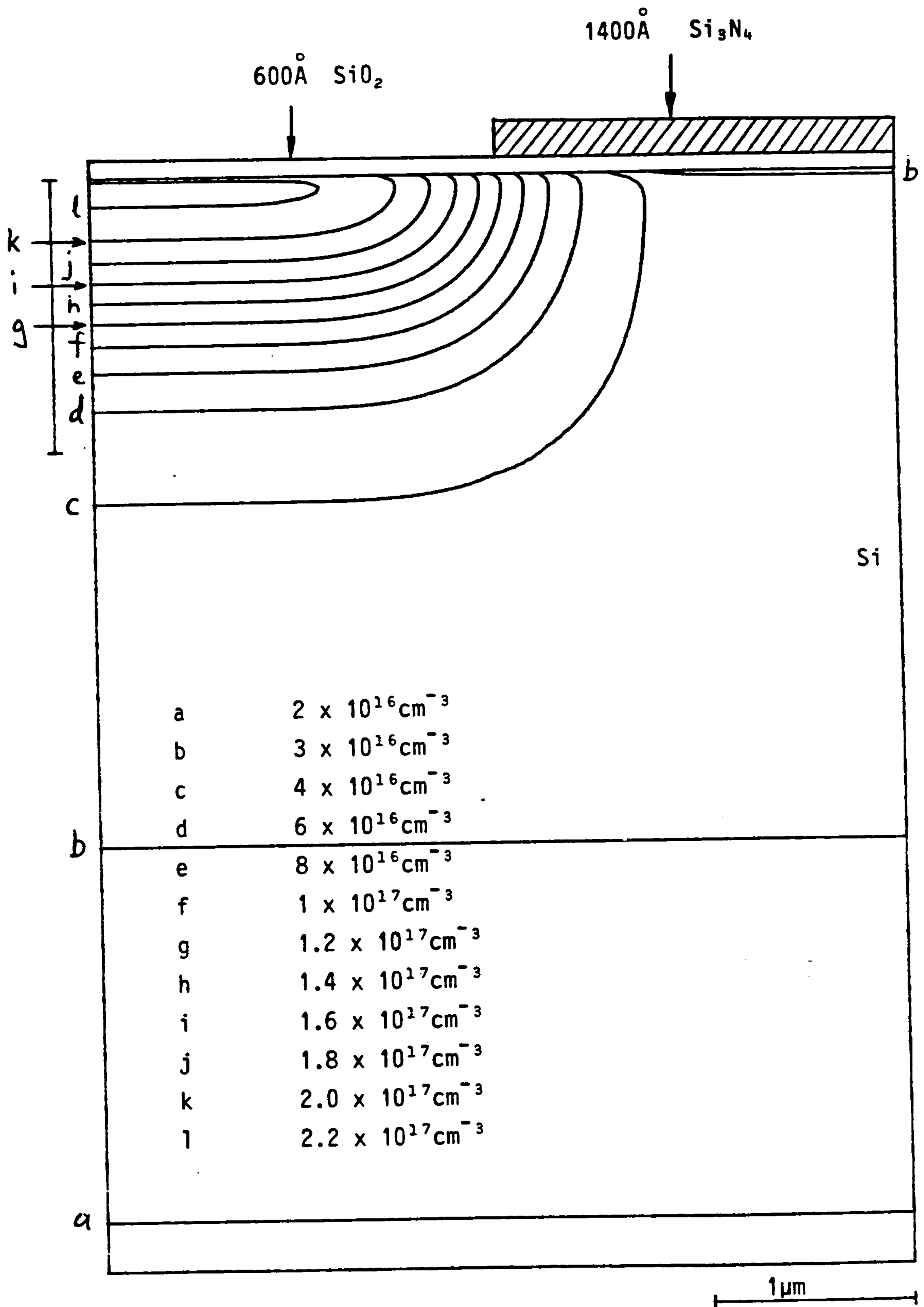


Figure 8.14 : Field implant in p-well after drive-in: 500 mins at 1025°C in N_2.

Here T_F is the maximum thickness of silicon consumed during field oxide growth and, using the Deal-Grove law /36/, is found to be

$$T_F(t) = \alpha \left[\frac{-A_{OF} + \sqrt{A_{OF}^2 + 4 B_{OF}t + 4 X_p^2 + 4 A_{OF}X_p}}{2} - X_p \right] \quad ; \quad 0 \leqslant t \leqslant t_F \tag{8.22}$$

where B_{OF}/A_{OF} and B_{OF} are the linear and parabolic rate constants and t_F is the total time for the field oxidation step. The top surface of the oxide layer is defined by $x = X_F'(y,t)$ where

$$X_F'(y,t) = -X_p - (\frac{1}{\alpha} - 1)X_F(y,t) \quad ; \quad 0 \leqslant t \leqslant t_F \tag{8.23}$$

The fitting parameter k_1 is a measure of the lateral extension of the bird's beak region and is best determined from a Scanning Electron-beam Microscope (SEM) study as shown in figure 8.15. In this particular case $k_1 = 2.3$, and the time evolution of the field oxide, beginning from the pad oxide and finishing with 1.25 micron at the thickest part, is shown in figure 8.16. Recently attempts have been made to model numerically field oxide growth as a result of a given pad oxide and nitride thickness by solving for pressure in the Navier-Stokes equation /37-39/.

However, this approach is not valid for temperatures below 950°C at which point silicon dioxide ceases to exhibit viscous flow /40/. In production MOS processes, the field oxidation step is usually carried out at or below a temperature of 950°C (with the addition of a chlorine-bearing gas to the furnace ambient) in order to

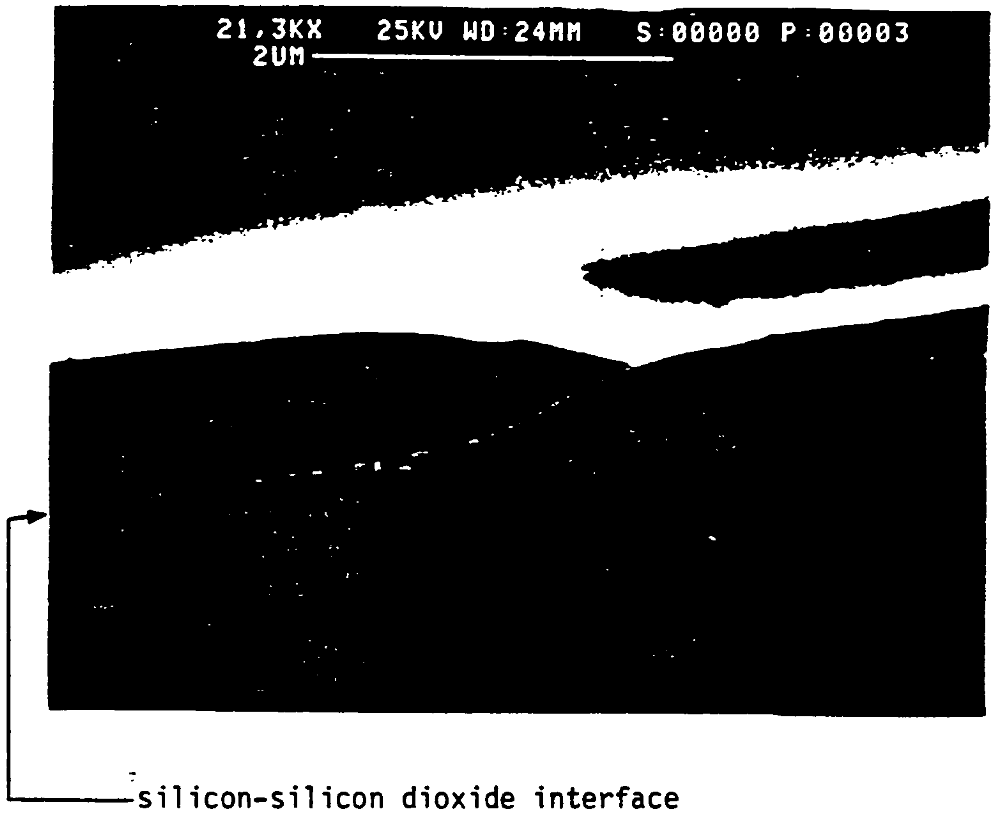
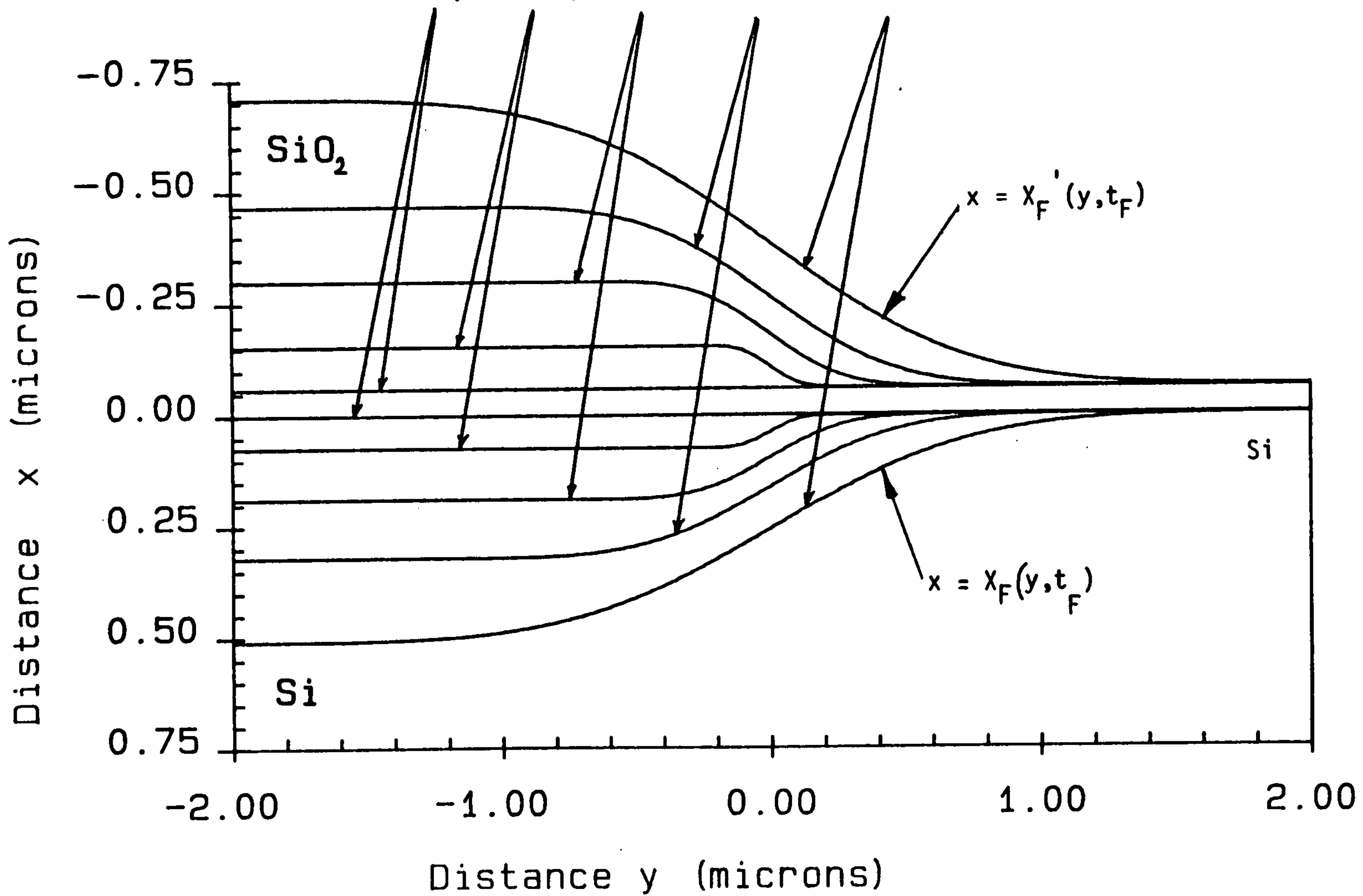


Figure 8.15 : SEM micrograph of bird's beak.

FIGURE 8.16 : Simulation of Field Oxide Growth

time= 0, 100, 300, 600, 1160 mins



suppress the occurence of oxidation-induced stacking faults /41,42/ which degrade die yield. The LOCOS step of the p-well CMOS process in the present study uses a temperature of $900^{o}C$ and so use of the Navier-Stokes equation is not valid.

The partial derivatives X' and X'' are evaluated by twice differentiating (8.20) and $\dot{X}$ is approximated by a finite difference between time levels.

Figure 8.17 shows the redistribution of boron after field oxidation. Because the segregation coefficient of boron is $k = 6$ at $900^{o}C$, the surface of the silicon is severely depleted of dopant after a time $t_F = 1160$ mins in the furnace tube, as is evident from the closely spaced contours characteristic of a steep concentration gradient. Indeed the sucking effect is so severe that even a portion of the active device region is depleted. As shall be shown by later plots, this effect has consequences for the dopant profile under the gate oxide of the n-channel MOS transistor even at the end of the fabrication process. The reason for using a field implant in the p-well region now becomes clear. Even although the surface concentration of boron is undesirably low at this stage in the process, enough of the field implant remains to fill the sucked out region by diffusion during subsequent high temperature cycles. The consequences of omitting the field implant from the process flow are shown by figure 8.18 where it is clear that the depleted region under the field oxide can only be filled slowly with diffusing boron atoms. The end results would be the occurrence of parasitic

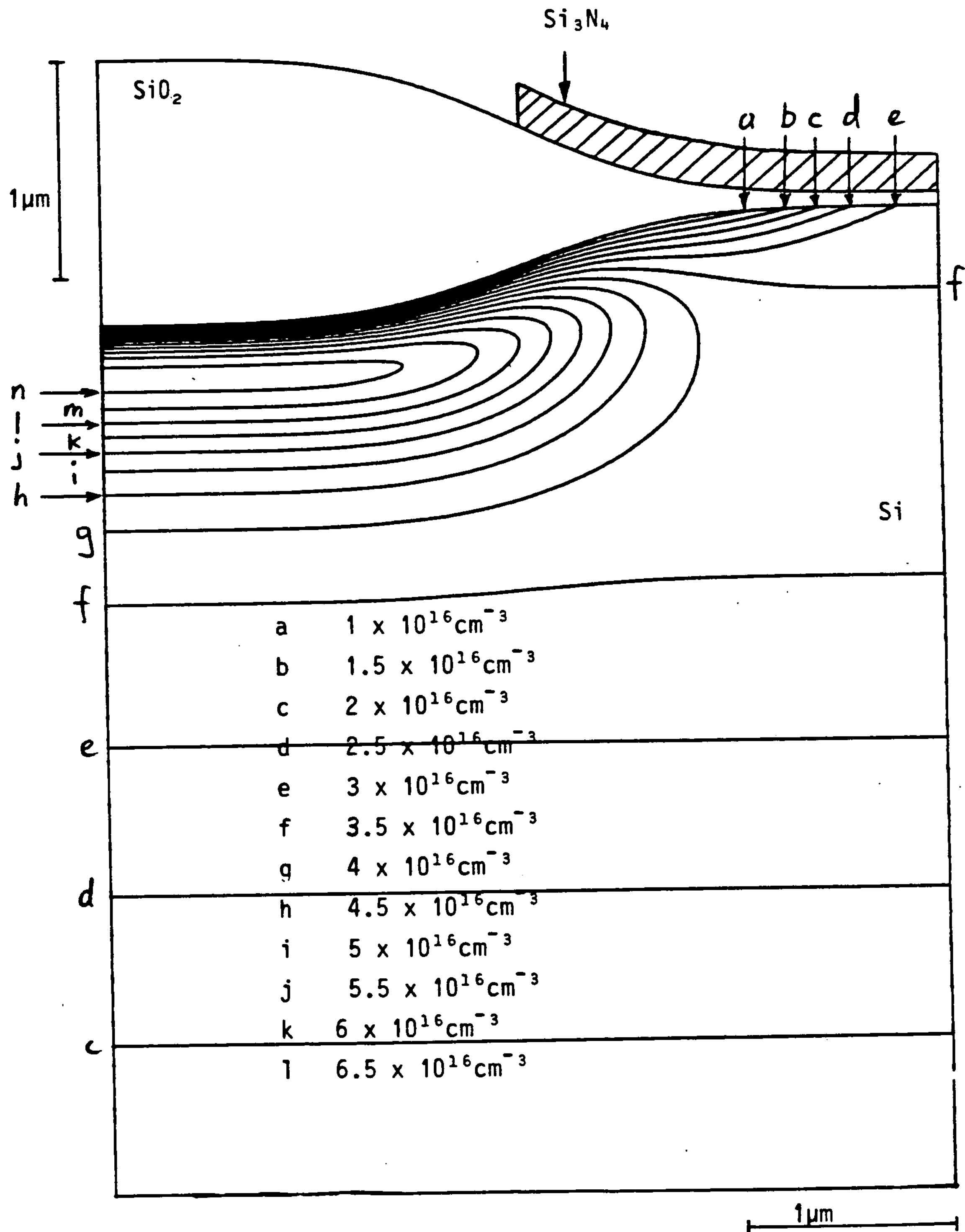


Figure 8.17 : Boron profile after field oxidation 1160 mins at 900°C in H_2O.

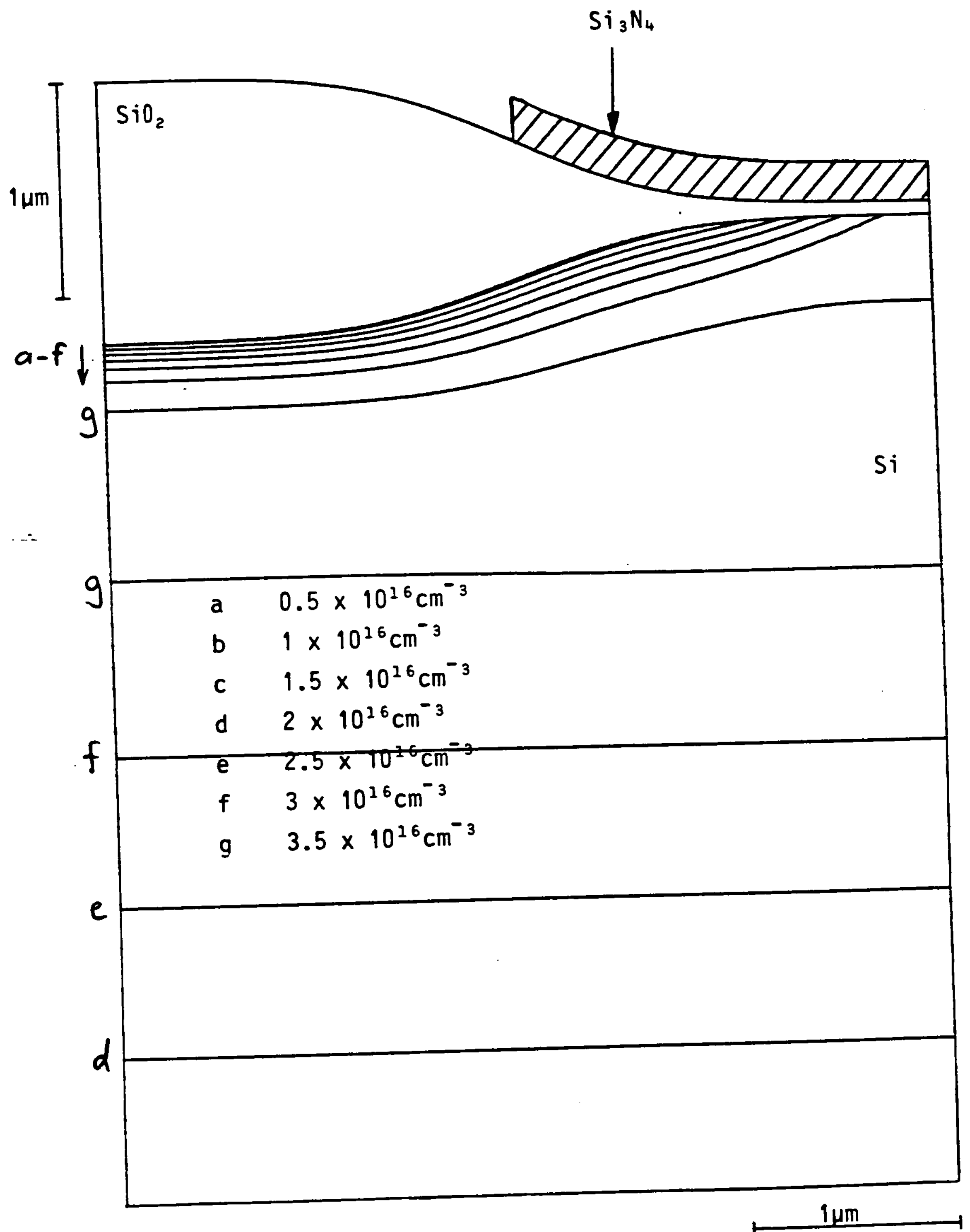


Figure 8.18 : Boron profile after field oxidation (no field implant performed).

transistor action between adjacent N+ diffused regions due to a low transistor threshold voltage in the field region.

Next the nitride and pad oxide layers are removed to leave bare silicon in the active region. Although the oxide-silicon interface is still described by $x = X_F(y,t_F)$, etching alters the position of the top oxide surface to $x = X_E'(y)$ where

$$X_E'(y) = -\left(\frac{1}{\alpha} - 1\right) X_F(y,t_F) \tag{8.24}$$

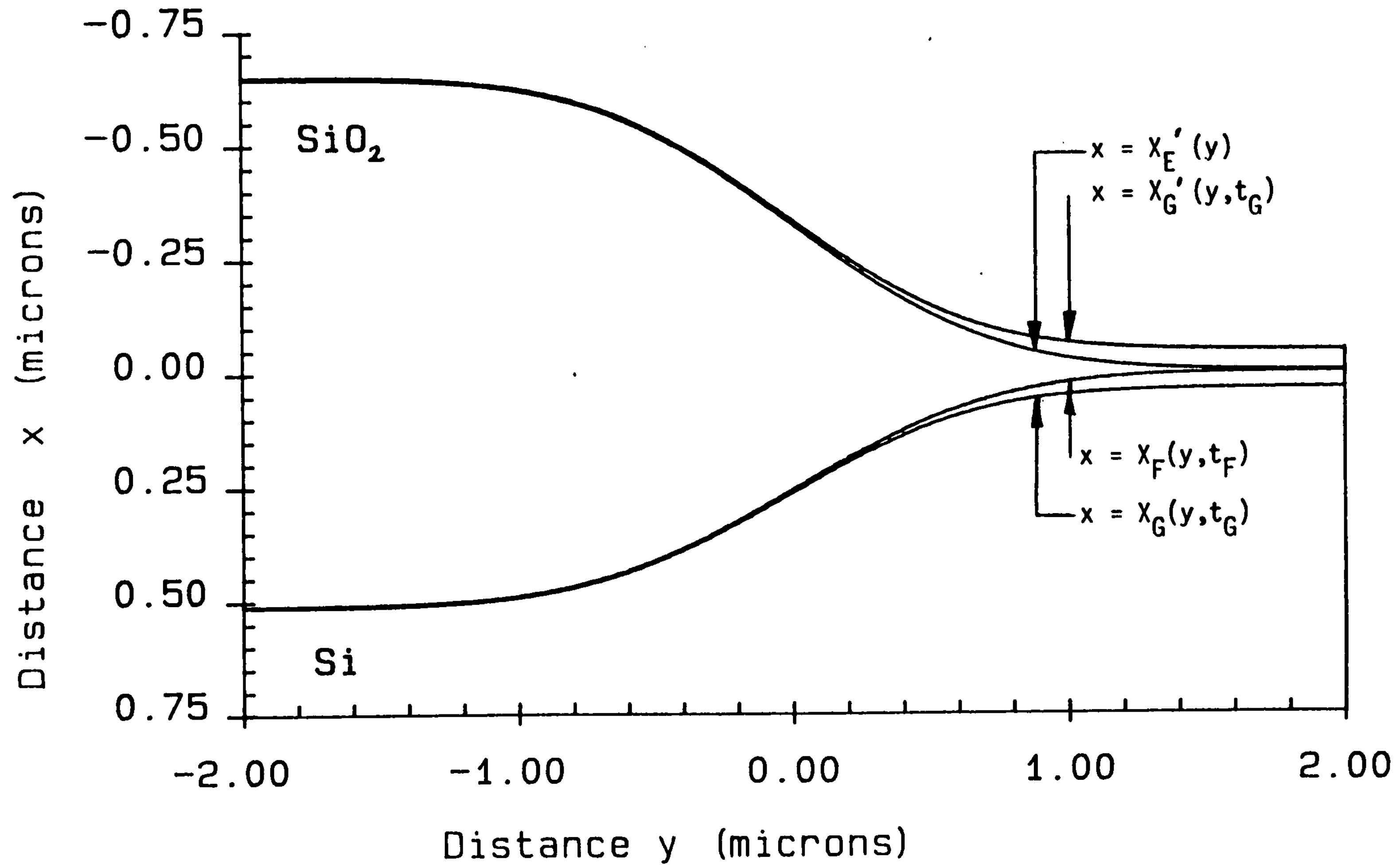
Plasma and wet chemical etching are carried out at low temperature and so give rise to no impurity redistribution. Gate oxidation is simulated using a quasi-2-D model whereby the increase in oxide thickness at a given point y in the lateral direction is dictated only by the initial thickness in the x-direction at that point. This approximation neglects any lateral oxidation effect, and is valid so long as the final gate oxide thickness is much less than the field oxide thickness, which is in fact the case in all current MOS processes. Thus, during gate oxidation, the position of the oxide-silicon interface is given by $x = X_G(y,t)$ where

$$X_G(y,t) = \frac{1}{2}\left\{-\alpha A_{OG} + \sqrt{\alpha^2 A_{OG}^2 + 4\alpha^2 B_{OG}\, t + 4X_F^2(y,t_F) + 4\alpha A_{OG} X_F(y,t_F)}\right\} \quad ; \; 0 \leqslant t \leqslant t_G \tag{8.25}$$

where A_{OG} and B_{OG} are the oxide growth parameters for this step and t_G is the total gate oxidation time. The top oxide surface is defined by $x = X_G'(y,t)$ where

$$X_G'(y,t) = \left(1 - \frac{1}{\alpha}\right) X_G(y,t) \quad ; \; 0 \leqslant t \leqslant t_G \tag{8.26}$$

FIGURE 8.19 : 800 Å Gate Oxide Growth



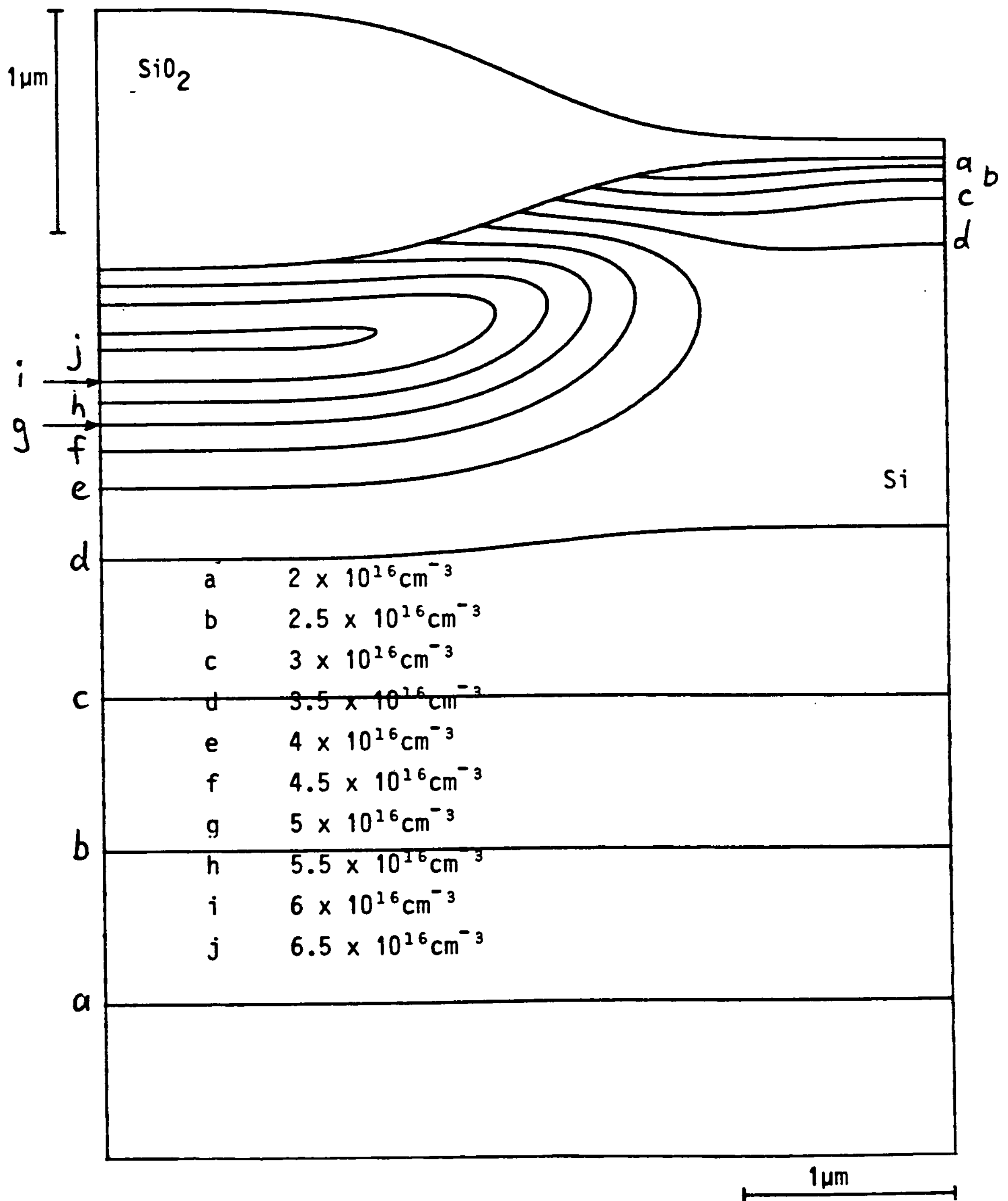


Figure 8.20 : Boron profile after gate oxidation: 32 mins at 1050°C in dry O_2.

The final oxide shape is shown in figure 8.19, and the resulting boron profile is shown in figure 8.20. While the boron of the field implant diffuses into the silicon surface region under the field oxide, more boron is removed from the active device region as gate oxidation proceeds. Next the gate oxide is annealed in a non-oxidising ambient to give the profile of figure 8.21, and this is followed by an anneal to activate the source/drain implant and flow the phosphosilicate glass (PSG) to give the final boron profile in the p-well as shown in figure 8.22.

In order to arrive at the net dopant concentration in the p-well, the phosphorus profile must be modelled also. However, as already discussed, a mesh spacing of the order of 10Å is required to model this impurity species accurately at the surface of the silicon. Such a fine mesh requires so small a time step to guarantee numerical stability of the explicit difference scheme that execution times prove to be prohibitively long. Instead of a numerical treatment, a semi-empirical model is used whereby the 1-D profile obtained from the active device region is simply extended across into the field region /31/ as shown in figure 8.23. Some idea of the accuracy of this approach can be obtained by comparing the 1-D cross-section at the left-hand side of this plot with the corresponding results of SUPREM from the field region of the wafer. The SUPREM and EPIC results are compared in figure 8.24 where it can be seen that this simplistic method of modelling phosphorus is accurate in the bulk and not more than 10% inaccurate near the silicon surface, which is good enough for all practical purposes. The boron of fig-

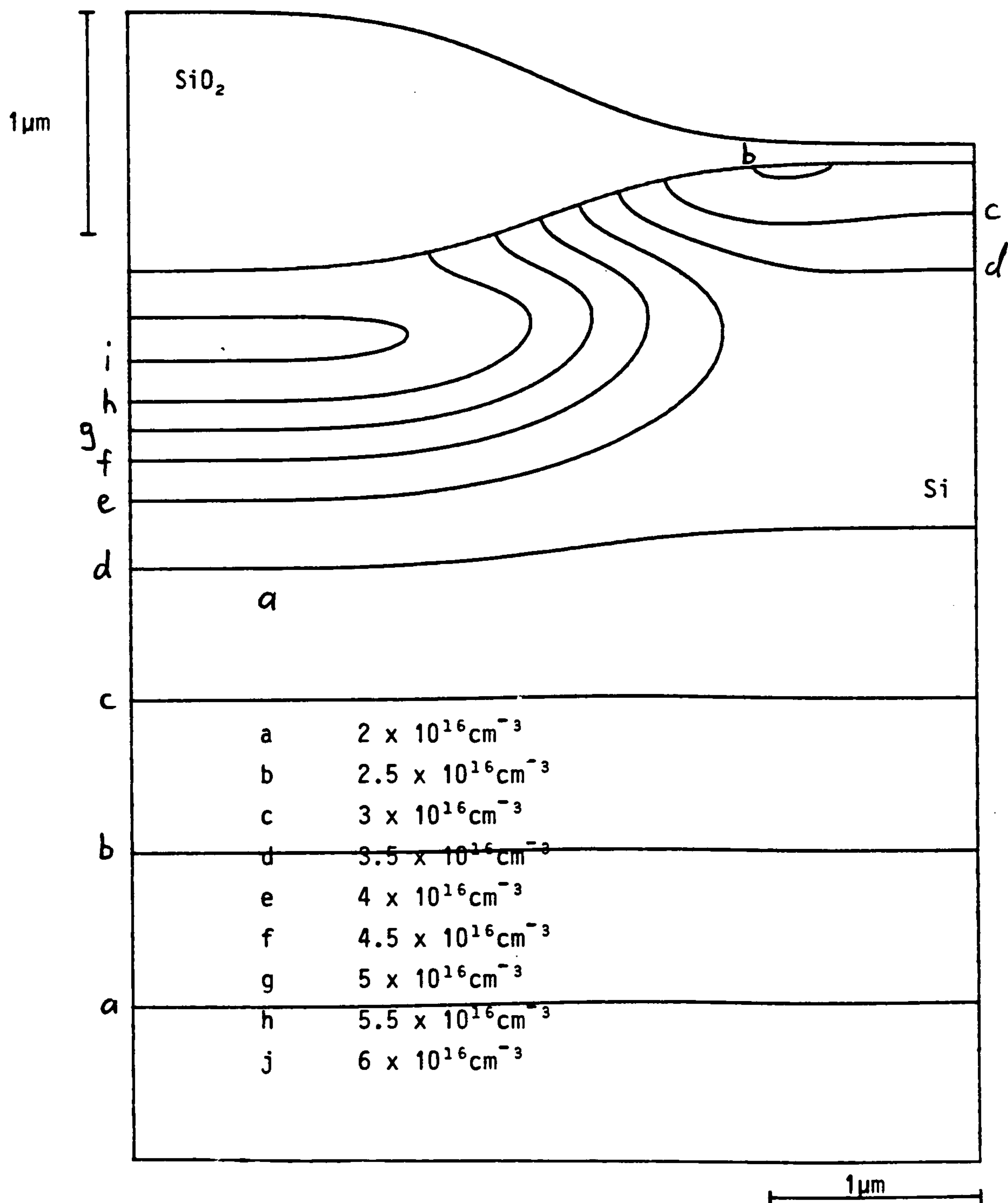


Figure 8.21 : Boron profile after gate oxide anneal: 60 mins at 1050°C in N_2.

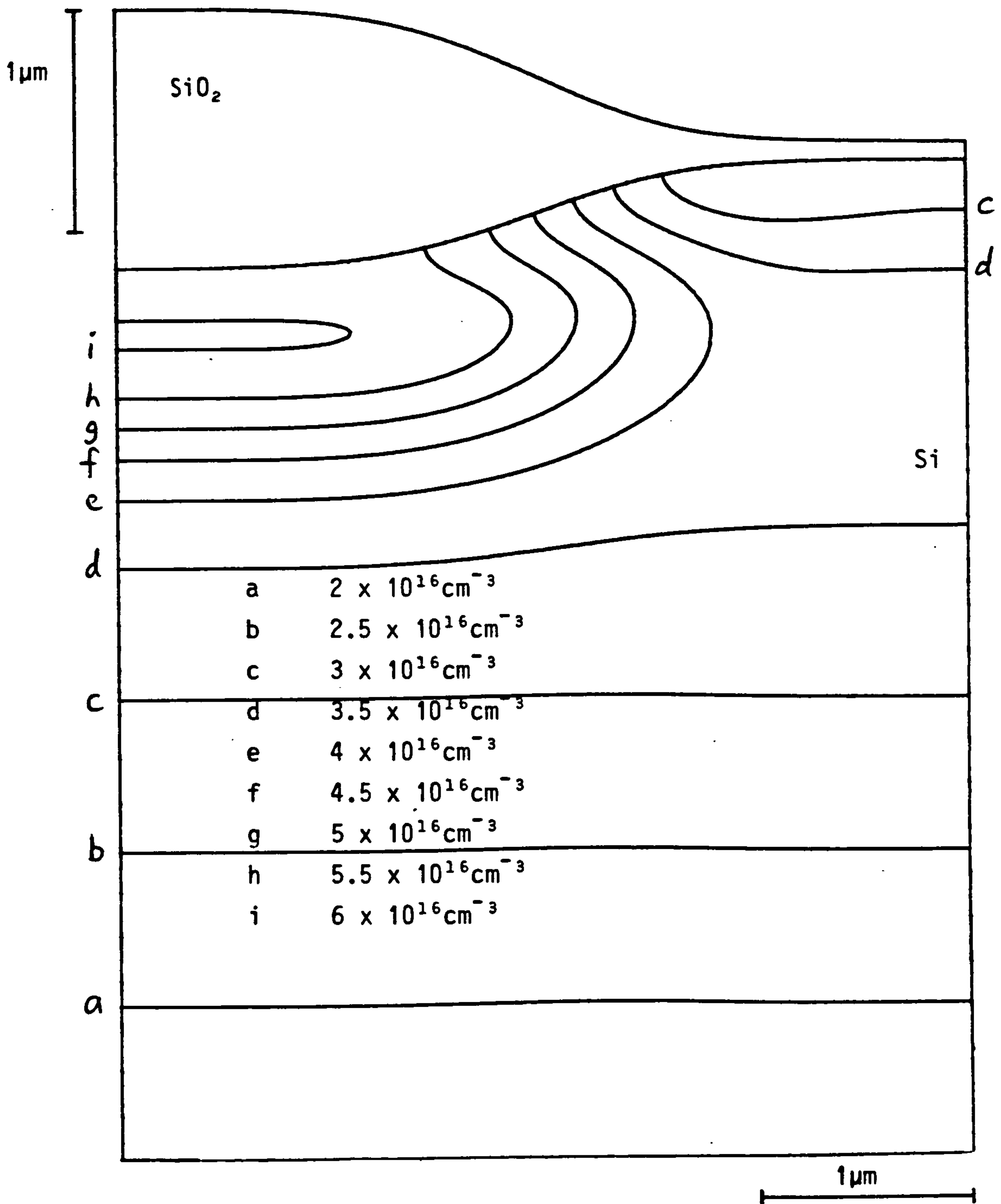


Figure 8.22 : Boron profile after PSG anneal: 30 mins at 1000°C in N_2.

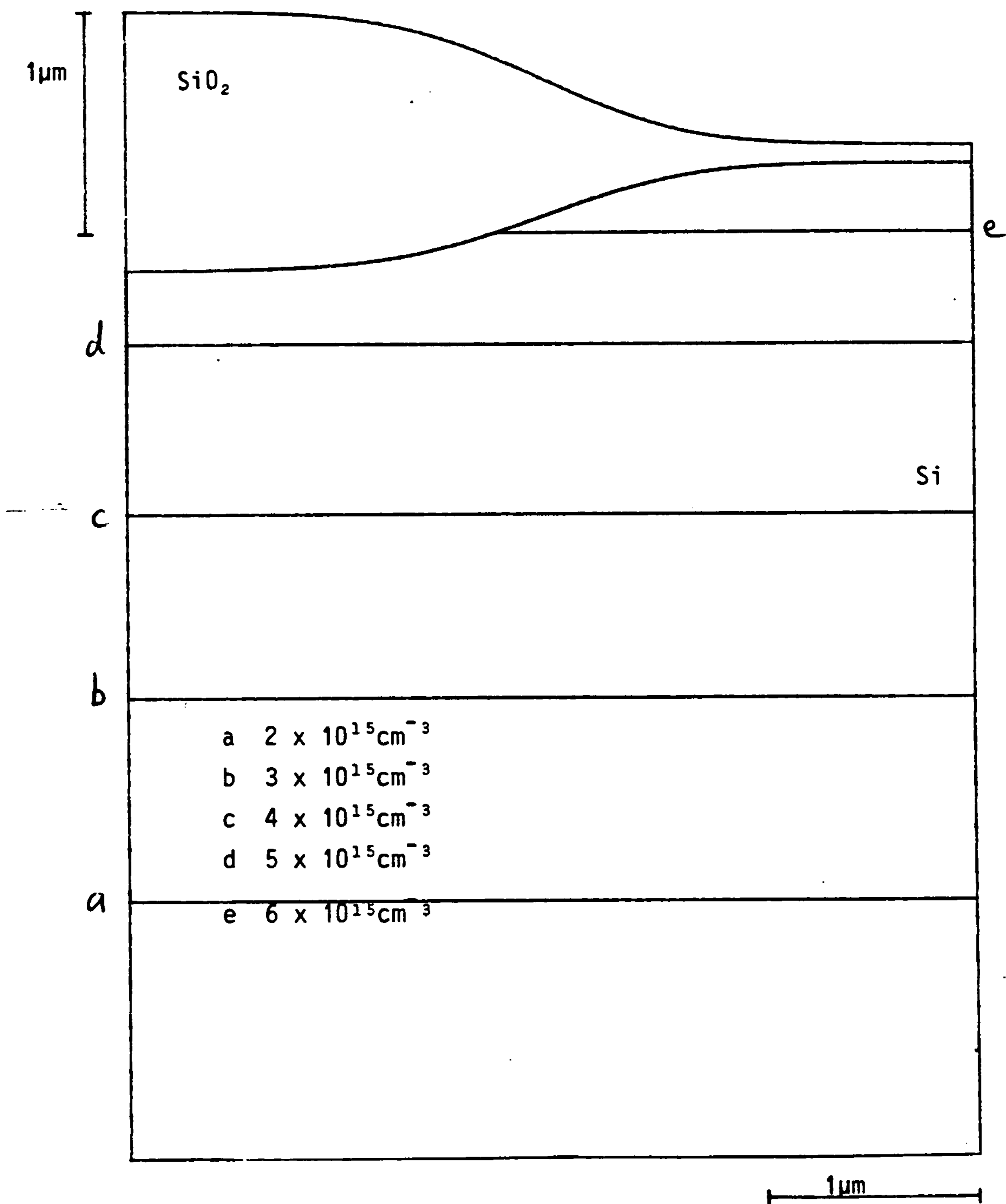
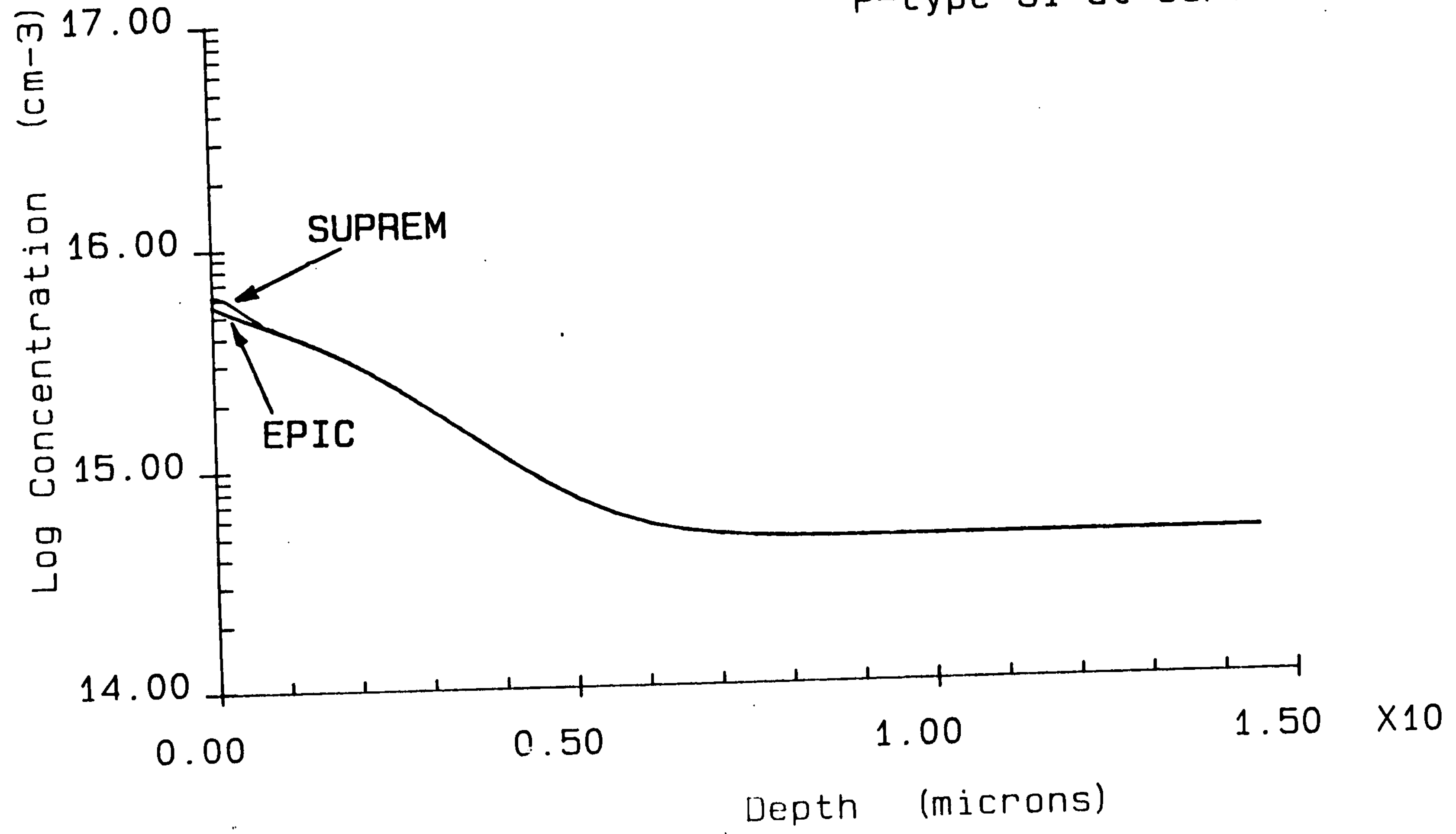


Figure 8.23 : Approximation to phosphorus profile after PSG anneal.

FIGURE 8.24 : SUPREM-EPIC Comparison

Phosphorus in p-well field region



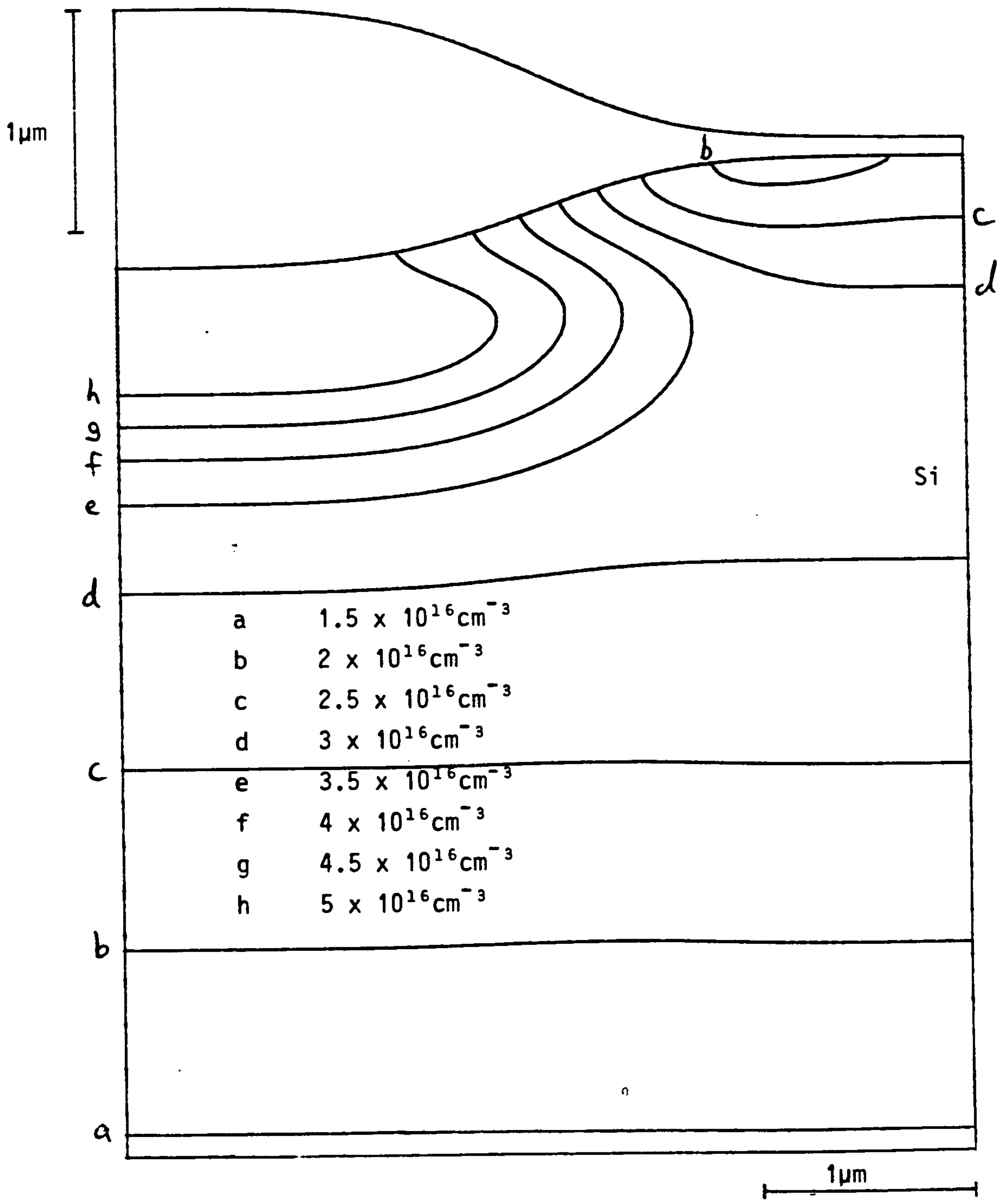


Figure 8.25 : Final net profile in p-well.

ure 8.22 is compensated with the phosphorus of figure 8.23, and the net acceptor profile for the n-channel MOS device is shown by figure 8.25. The most notable feature of this plot is the slight dip in the concentration values at the edge of the active device region, which is a consequence of the severe segregation behaviour of boron during the field oxidation step.

Now consider the profile of the p-channel MOS transistor in the n-substrate region. The threshold voltage V_T must be increased by a boron implant to allow use of heavily doped n-type polysilicon as a gate electrode. The accelerated ions impinge on both field and gate oxides as shown in figure 8.26. The resulting profile in the silicon is modelled using a similar approach to Chin et al /16/, where Runge's integral (6.6) is evaluated using a quadrature type of integration rule. The oxide layer is converted to an equivalent layer of silicon using the density transformation of (4.13).

The smooth top surface of the resulting effective silicon layer is approximated by a series of horizontal steps, one of which is shown in figure 8.26. The total implanted profile I(x,y) is obtained by summing the contributions from all sections to obtain

$$I(x,y) = \frac{I_{max}}{2} \sum_j \{ \operatorname{erf} \left(\frac{y - y_j + \delta y_j^-}{\sqrt{2}\,\Delta Y} \right) - \operatorname{erf} \left(\frac{y - y_j - \delta y_j^+}{\sqrt{2}\,\Delta Y} \right) \}$$

$$\cdot \exp \left[- \frac{\{ x - \frac{R_p}{R_{p1}} X_G'(y_j, t_G) + (\frac{R_p}{R_{p1}} - 1) X_G(y, t_G) - R_p \}^2}{2\,\Delta R_p^2} \right] \qquad (8.27)$$

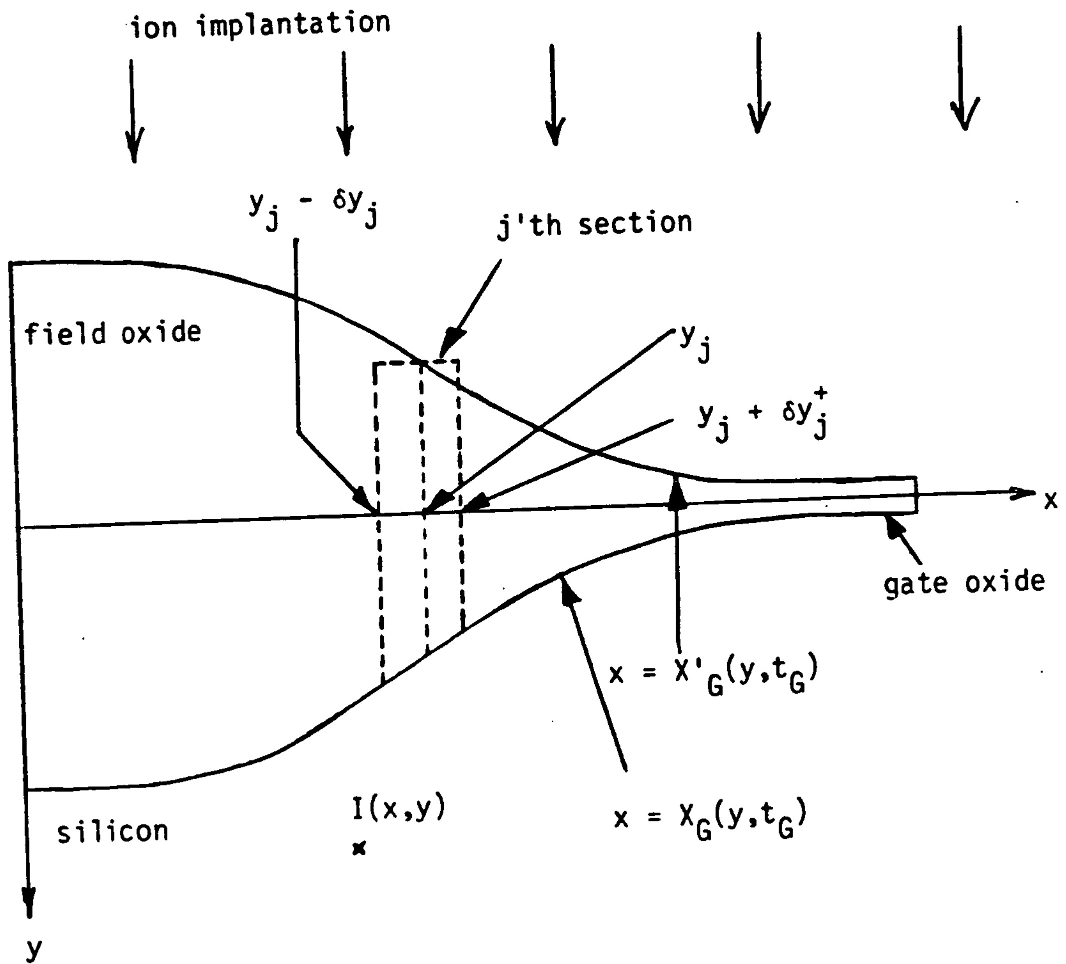


Figure 8.26 : Calculation of profile due to threshold adjust implant.

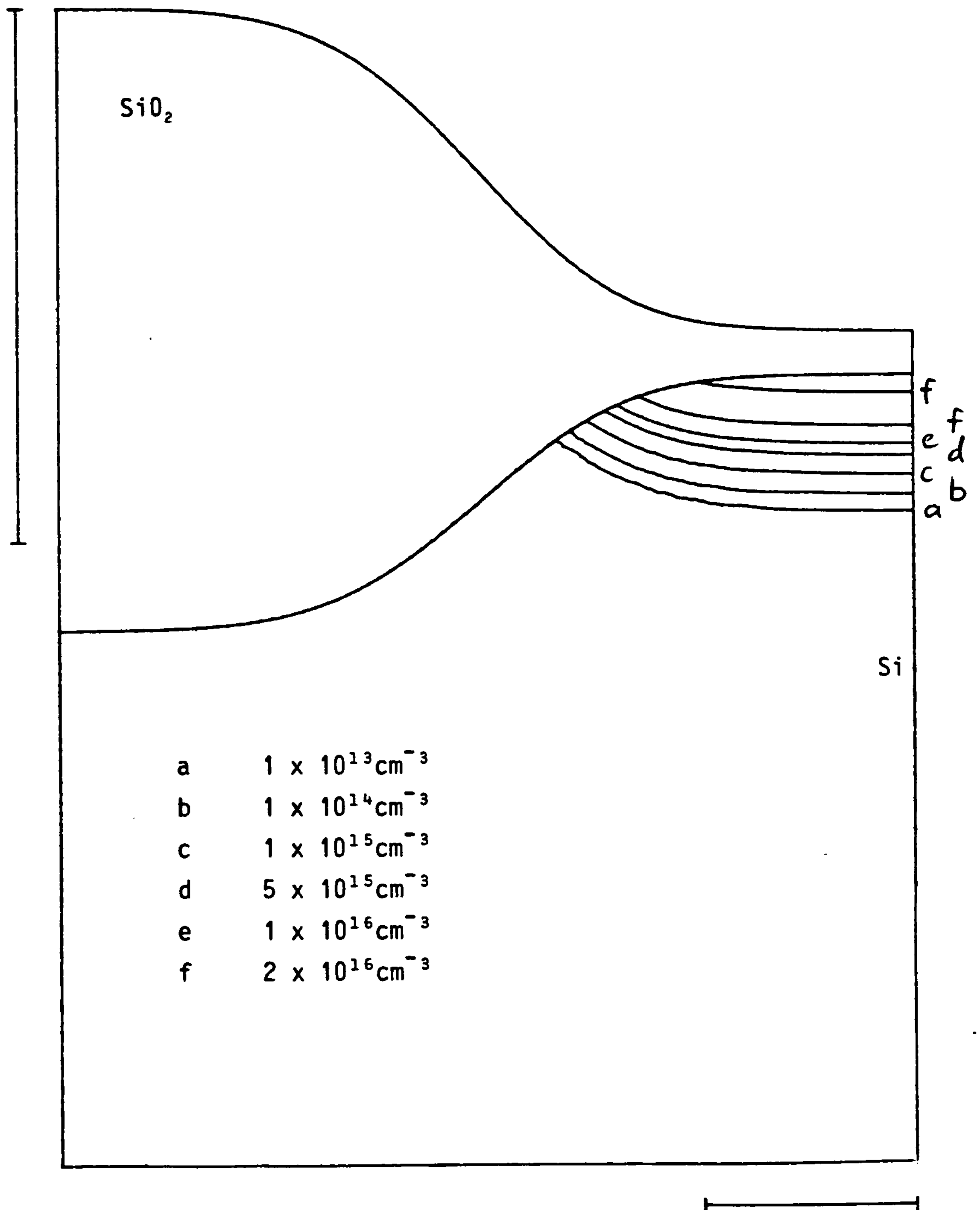


Figure 8.27 : Boron threshold adjust implant
3×10^{11} cm^{-2} $^{11}B^{+}$ at 45 keV

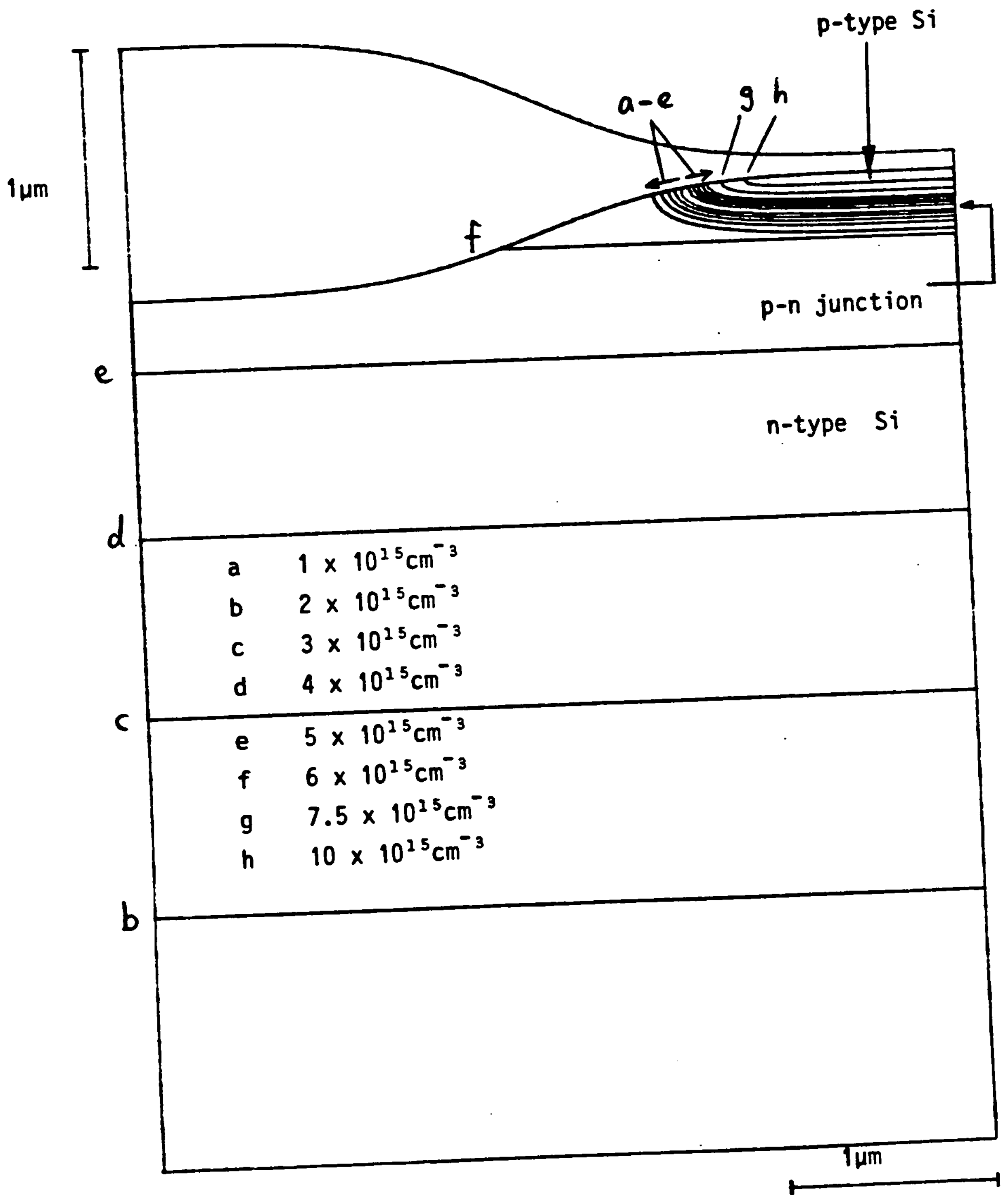


Figure 8.28 : Final net profile in n-substrate

where I_{max} is given by (6.8), R_{p1} is the projected range of the element in silicon dioxide and $(\delta y_j^- + \delta y_j^+)$ is the width of the j'th section. The summation must be extended outside the simulation domain by several R_p to account for those ions which are scattered into the area of interest. Maldonado /22/ uses sloping steps to approximate the top oxide surface, but the additional accuracy gained is only marginal for typical slowly varying oxide profiles used in MOS technologies at the present time.

Figure 8.27 shows a contour plot of the boron implant used to tailor the threshold voltage of the p-channel MOS transistor. The profile is subjected to the gate oxide anneal and PSG anneal at the end of the process, and is then combined with the phosphorus profile of figure 8.23 to give the net concentration of figure 8.28. The dose of the boron implant is high enough to invert the silicon type at the surface of the p-channel device as already seen in Chapter 4. Figures 8.25 and 8.28 represent the first simulation of n-channel and p-channel MOS transistors of a p-well CMOS process in the width direction /31/.

8.5 MEASUREMENT OF EFFECTIVE CHANNEL WIDTH

Determination of the effective channel width W_{eff} of both n-channel and p-channel MOS transistors is important for the design of CMOS integrated circuits. An accurate prediction of effective channel width using the 2-D impurity profiles presented in section 8.4 would require the use of a 2-D non-planar device simulator /6, 74/,

which is beyond the scope of this thesis. However it is shown that measurements of W_{eff} are consistent with the process simulation results already presented.

Most attempts to determine W_{eff} have been based on the linear regime of transistor operation where the drain-source current I_{DS} is given by /13/

$$I_{DS} = \frac{W_{eff}}{L_{eff}} \mu C_{ox} (V_{GS} - V_T) V_{DS} \quad ; \quad V_{DS} << V_{GS} - V_T \qquad (8.28)$$

Using (8.1) this becomes

$$I_{DS} = A (W_{mk} - \Delta W_{mk}) \qquad (8.29)$$

where the parameter A is given by

$$A = \frac{\mu C_{ox} (V_{GS} - V_T) V_{DS}}{L_{eff}} \qquad (8.30)$$

If the quantity A is a constant, then measurements of I_{DS} for a variety of transistors, each with a different width W_{mk}, but the same length, should give a straight line plot with intercept ΔW_{mk} on the W_{mk} axis. The channel mobility μ is effectively constant since it depends only weakly on channel width for low values of V_{DS} /43/. In practice, even if V_{GS} and V_{DS} are kept constant for each measurement, the parameter A is found to vary because the threshold voltage V_T is a function of the transistor width at small geometries /46,47/. Figure 8.29 shows how the modulus of V_T i.e. $|V_T|$ increases with decreasing channel width according to the mask for both NMOS

FIGURE 8.29 : Narrow Channel Effect on Vt

wafer c2#6

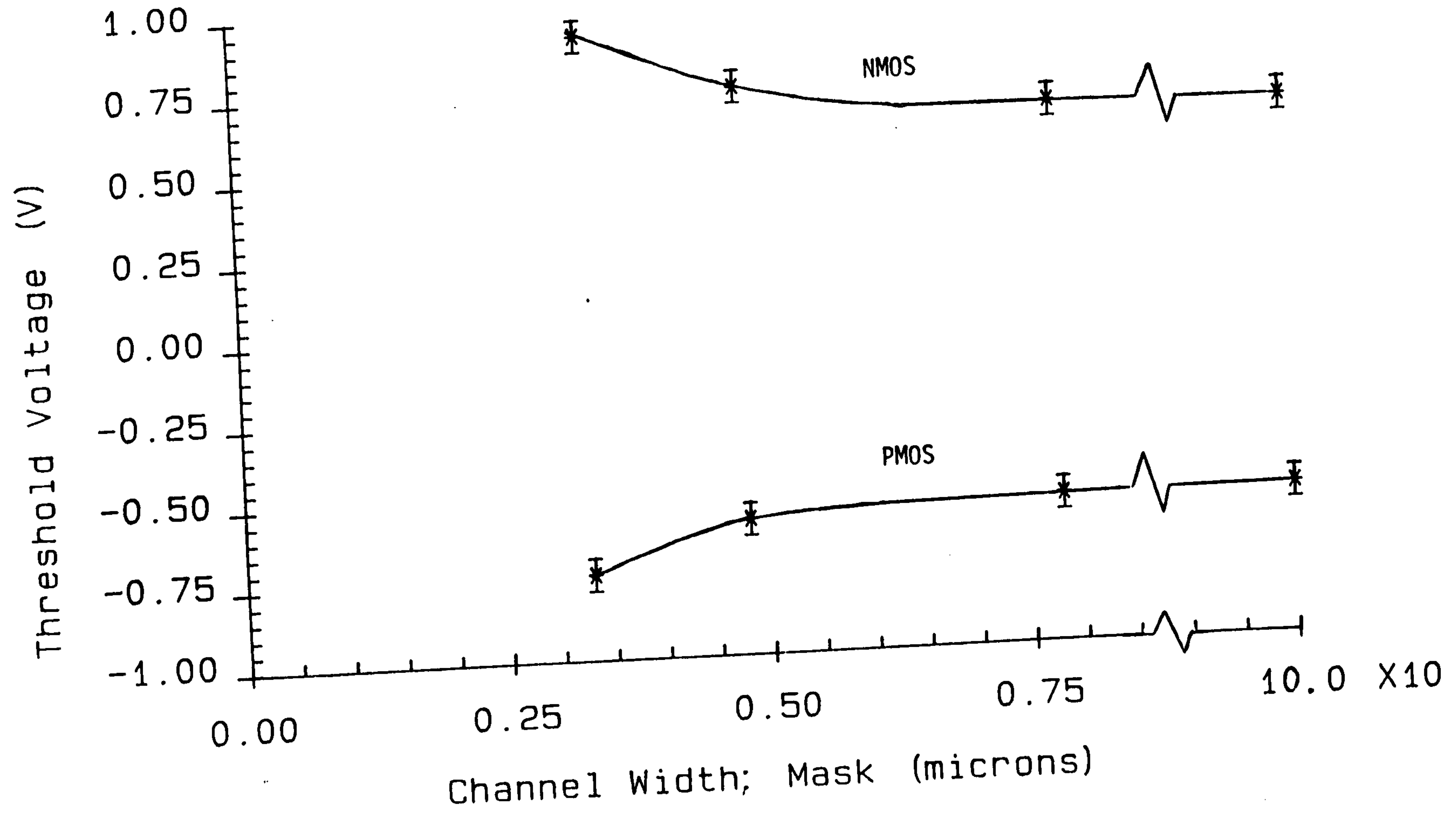
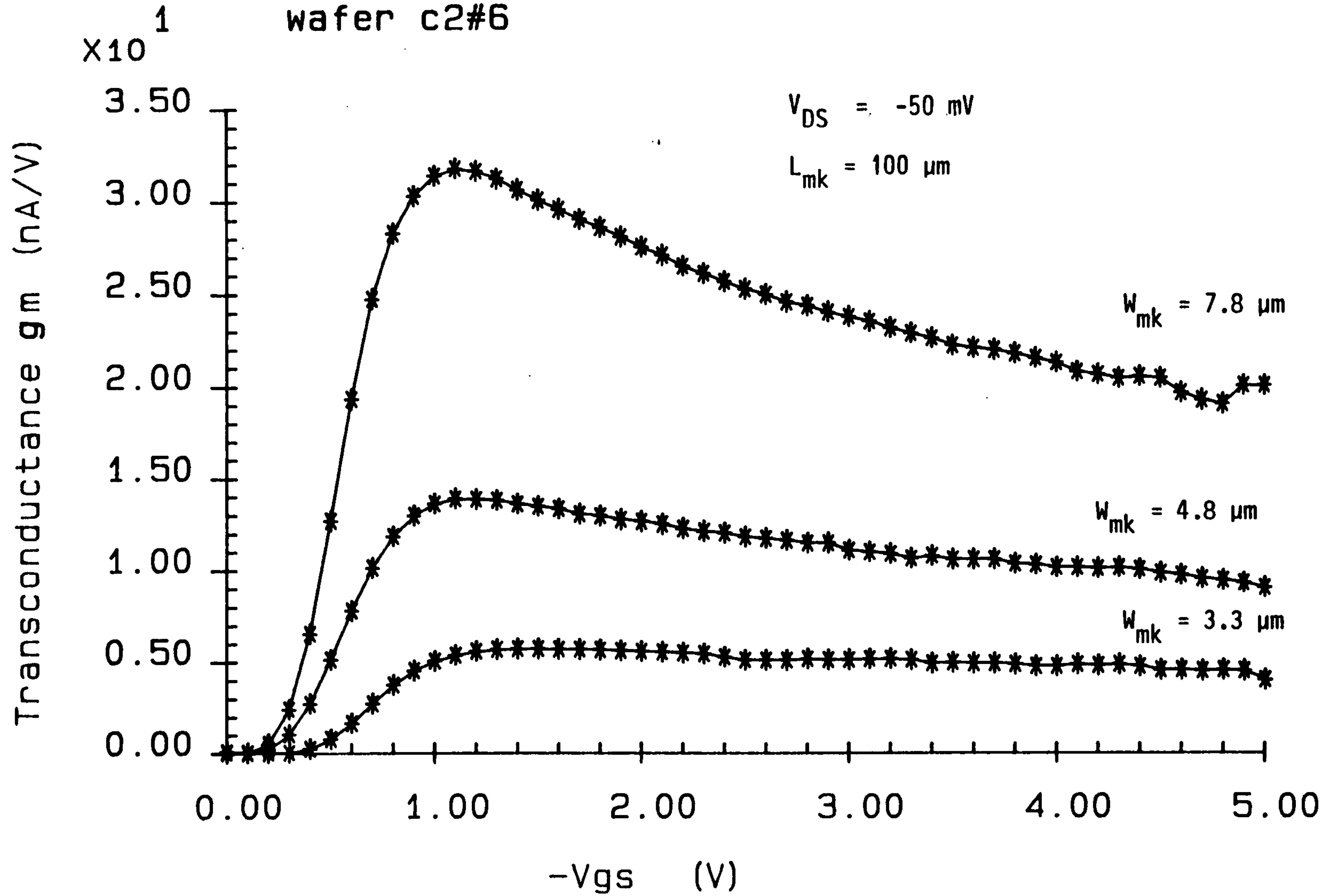


FIGURE 8.30 : PMOS Transistor gm-Vgs Measurements

wafer c2#6



and PMOS transistors which have large geometry threshold voltages of 0.6V and -0.6V respectively.

Despite the fact that V_T is not constant, ΔW_{mk} can be measured in either of the limiting cases of low V_{GS} /44/ or high V_{GS} /45/.

(a) Measurement of Width Offset for Low Gate-Source Voltage

This method of determining ΔW_{mk} is based on measurements of the transconductance g_m as a function of V_{GS} for each transistor as shown in figure 8.30 for the PMOS transistor. It is well established /13, 44/ that the point of maximum transconductance $g_{m,max}$ scales with V_T, so that a plot of this quantity against the mask dimension gives a straight line as shown in figure 8.31 for both NMOS and PMOS transistors. This procedure is repeated for a different set of NMOS and PMOS transistors which have large geometry threshold voltages of 1.0V and -1.0V respectively, as shown by figure 8.32. The least squares fit to determine ΔW_{mk}, is shown in figure 8.33. In each case it is found that

$$\Delta W_{mk} \text{ (low } |V_{GS}|) = (2.3 \pm 0.2)\ \mu m \qquad (8.31)$$

(b) Measurement of Width Offset for High Gate-Source Voltage

Variations in V_T between transistors of different widths can be reduced by taking measurements of I_{DS} at high V_{GS} ie $V_{GS} \gg V_T$

FIGURE 8.31 : MOST Effective Channel Width

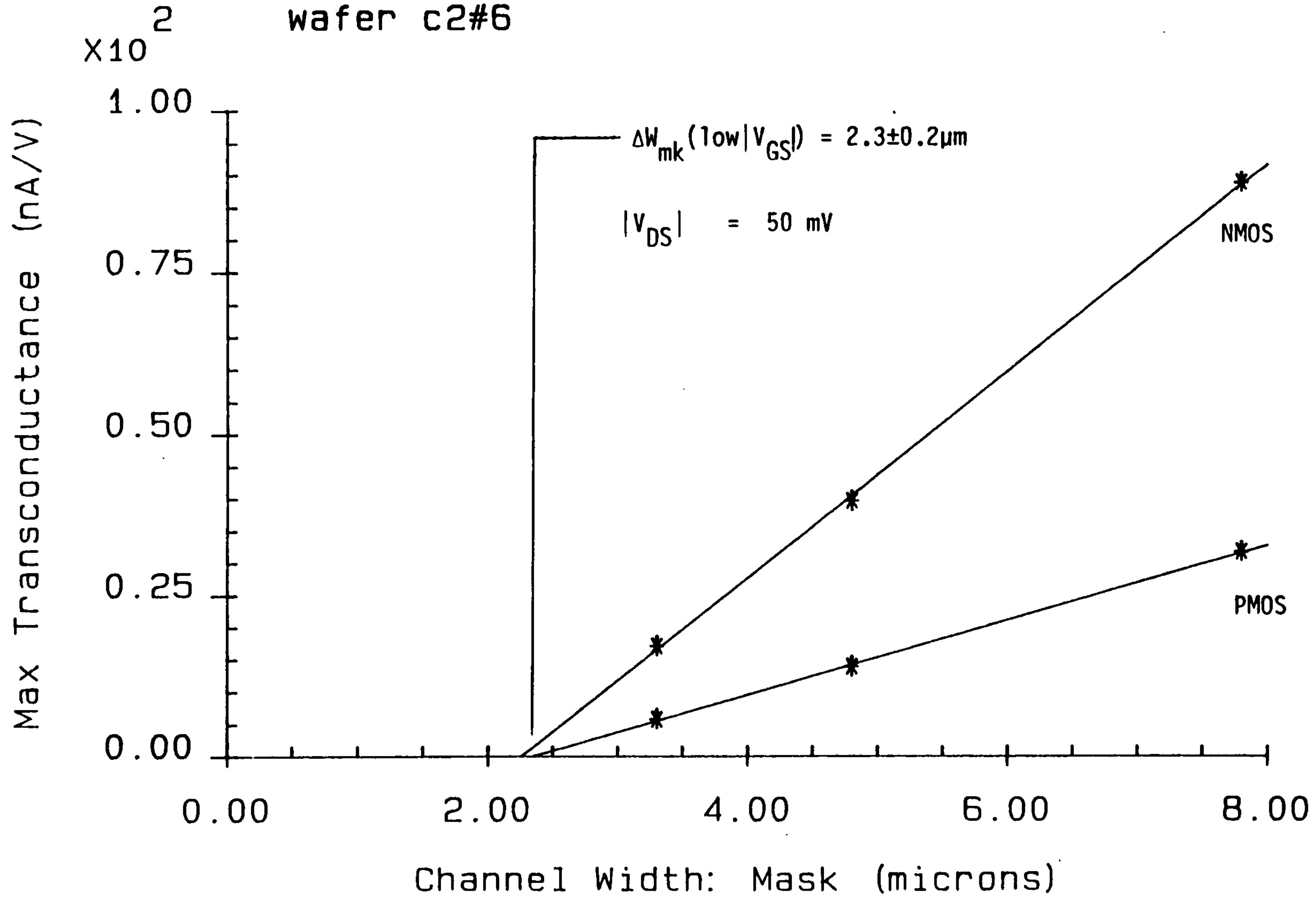


FIGURE 8.32 : Narrow Channel Effect on Vt

wafer c2#17 $|V_{DS}|$ = 50 mV

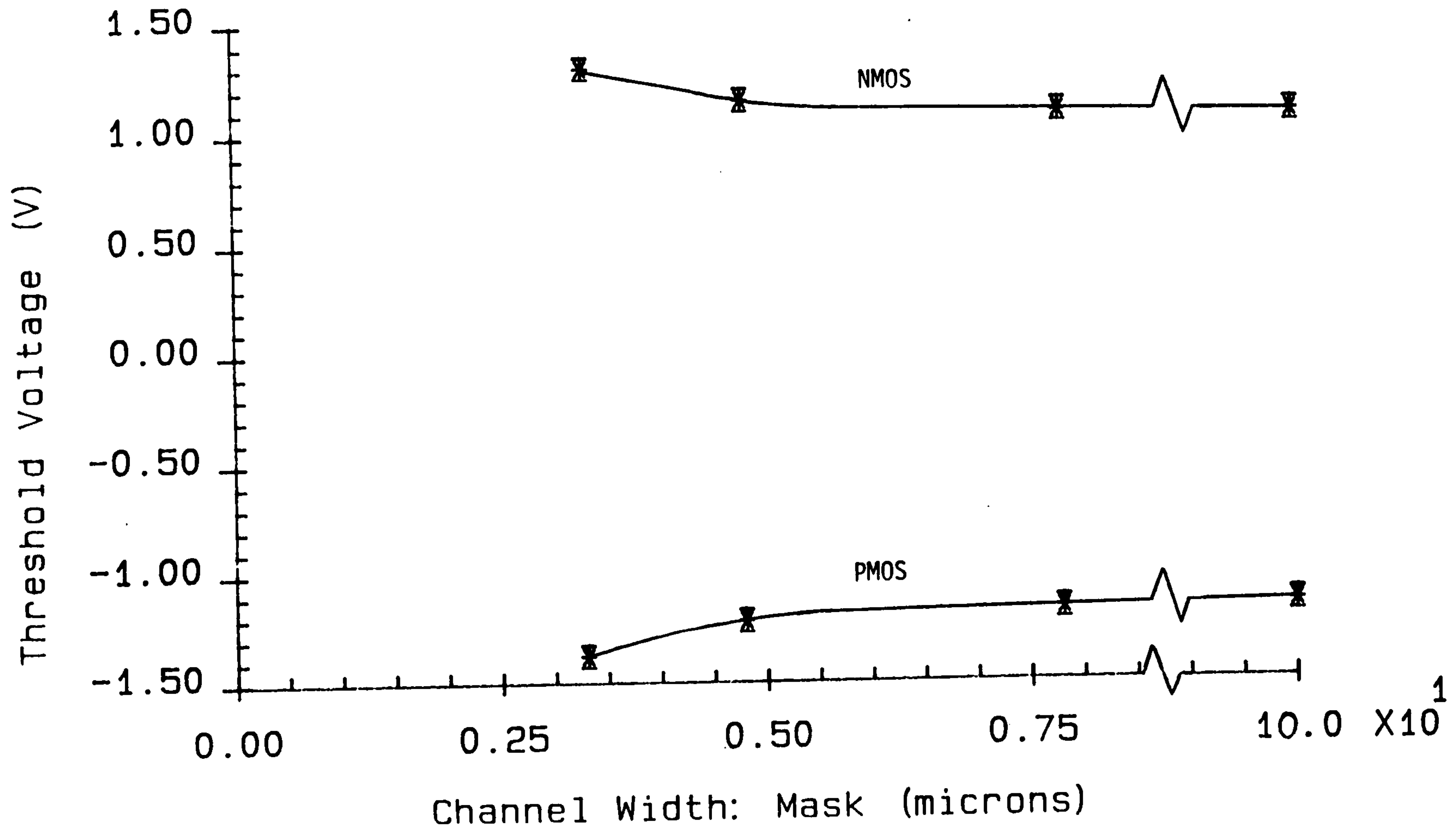


FIGURE 8.33 : MOST Effective Channel Width

wafer c2#17

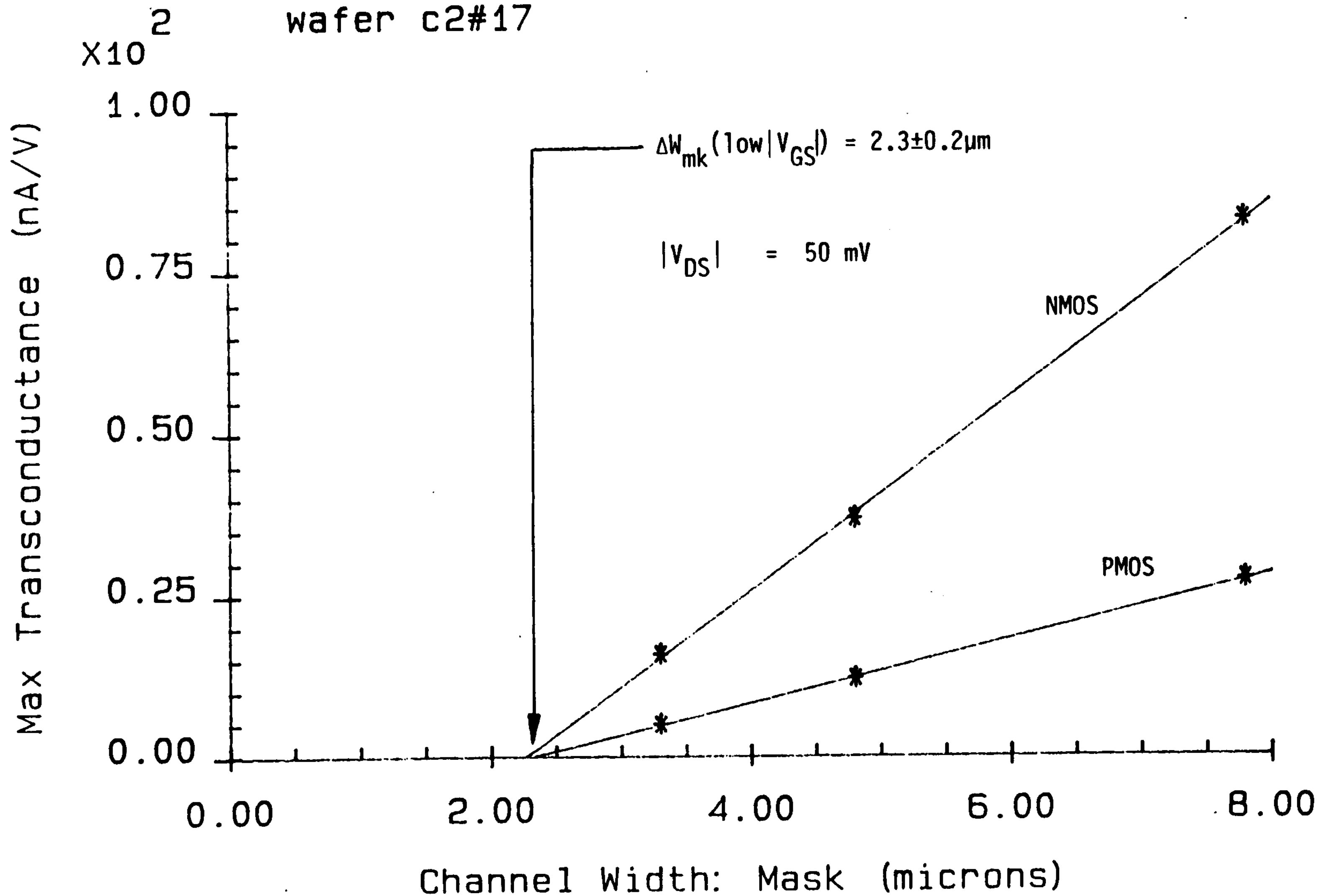


FIGURE 8.34 : MOST Effective Channel Width

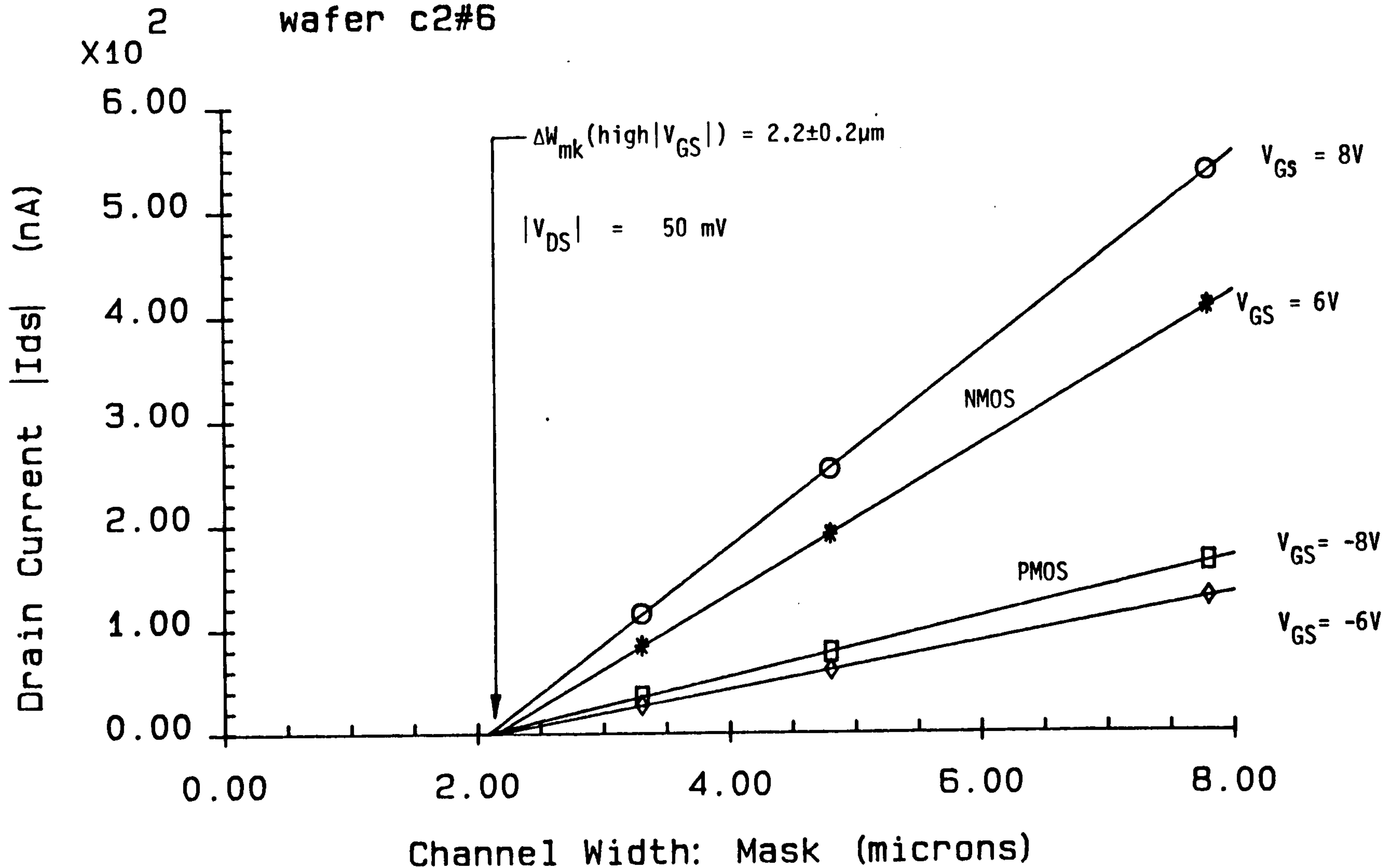
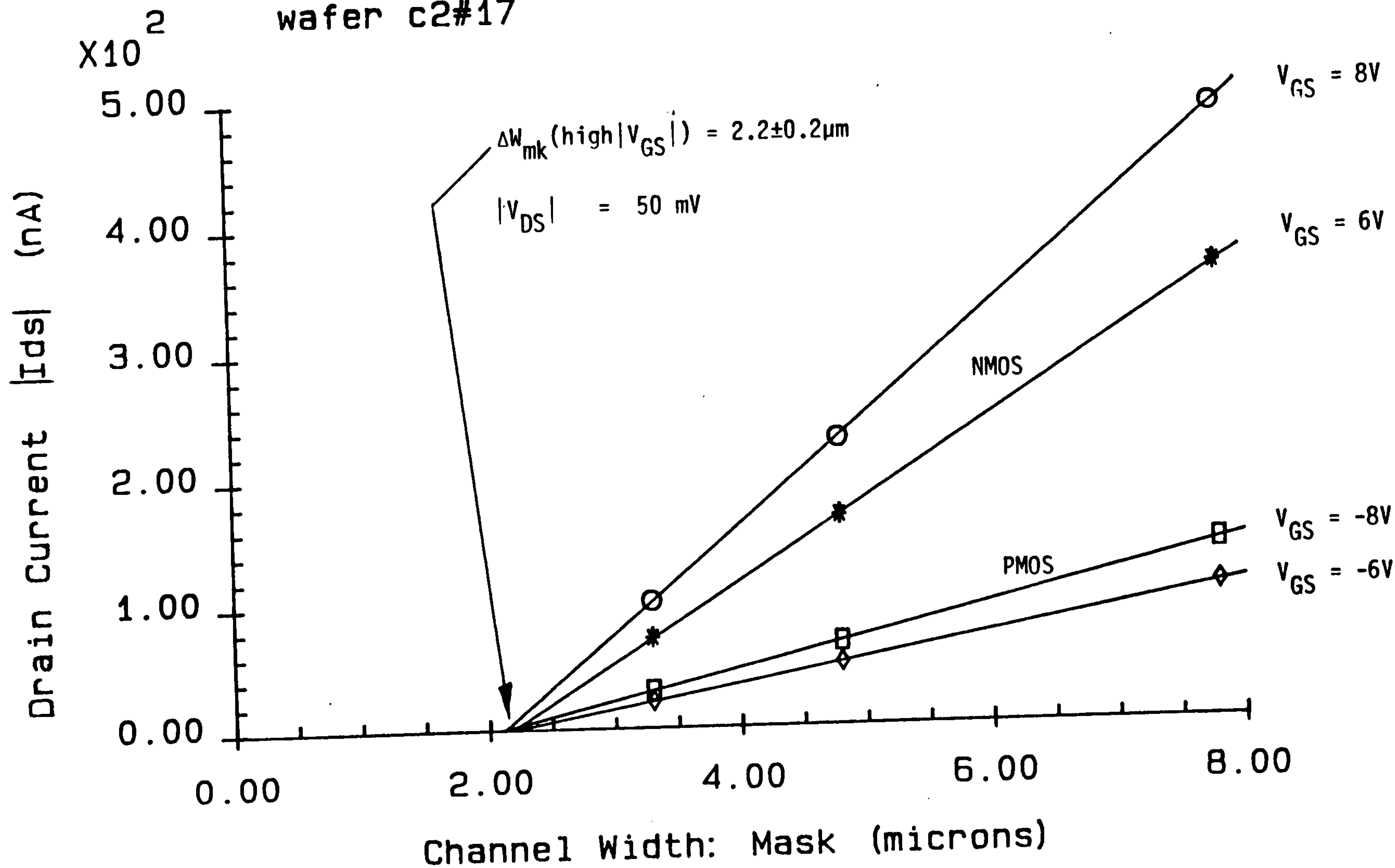


FIGURE 8.35 : MOST Effective Channel Width



/45/, in which case a plot of I_{DS} against W_{mk} for several different transistors gives a straight line plot with intercept ΔW_{mk}. This method is shown in figures 8.34 and 8.35 using the same CMOS wafers as in method (a) above. Two values of V_{GS} (V_{GS} = 6V and V_{GS} = 8V) are considered in order to test the consistency of this approach. In each case the result is

$$\Delta W_{mk} \text{ (high } |V_{GS}|\text{)} = (2.2 \pm 0.2)\ \mu m \qquad (8.32)$$

which is consistent with the result of method (a).

Since ΔW_{mk} is more or less the same for both wafers, the effective channel width is dominated by the shape of the bird's beak region, and it is clear that doping level in the channel region does not influence W_{eff} within experimental error.

The simulation results generated by EPIC are now shown to be consistent with this experimental data. From measurements of mask dimensions and patterned nitride tracks using both a Vickers image-splitting microscope and a Nanometrics Nanoline critical dimension computer, the offset between the mask dimension W_{mk} and the patterned nitride track width W_N is found to be

$$\Delta W_{mk-N} = \Delta W_{mk-PR} + \Delta W_{PR-N} = 0.2\mu m \qquad (8.33)$$

If W_{mk} = 4.2 micron, then W_N = 4.0 micron and W_{eff} = (1.9±0.2) micron. This value of effective channel width is indicated on figure

measured value of W_{eff} is shown with error bars

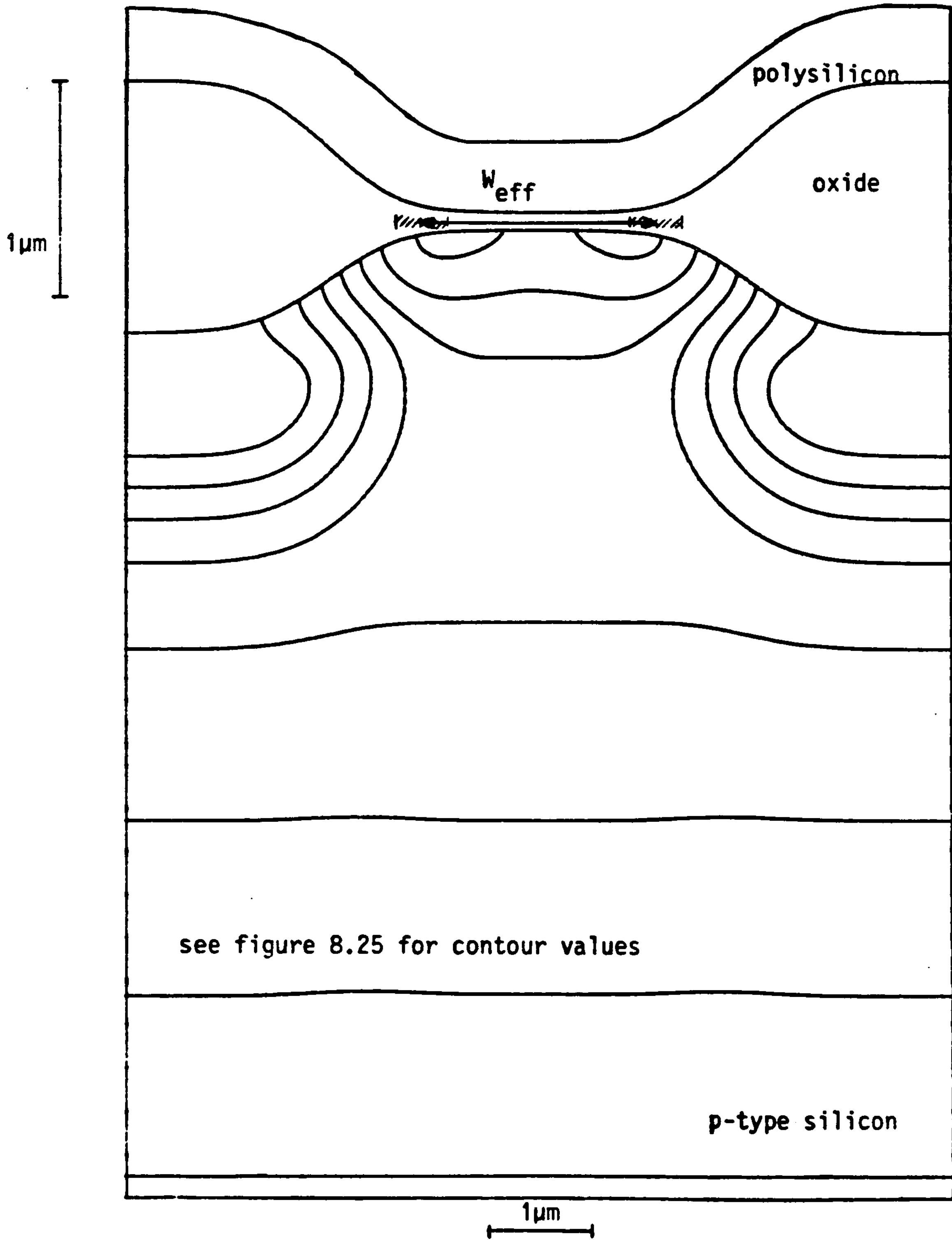


Figure 8.36 : Comparison of measured value of W_{eff} with simulation results for the NMOSFET.

measured value of W_{eff} is shown with error bars

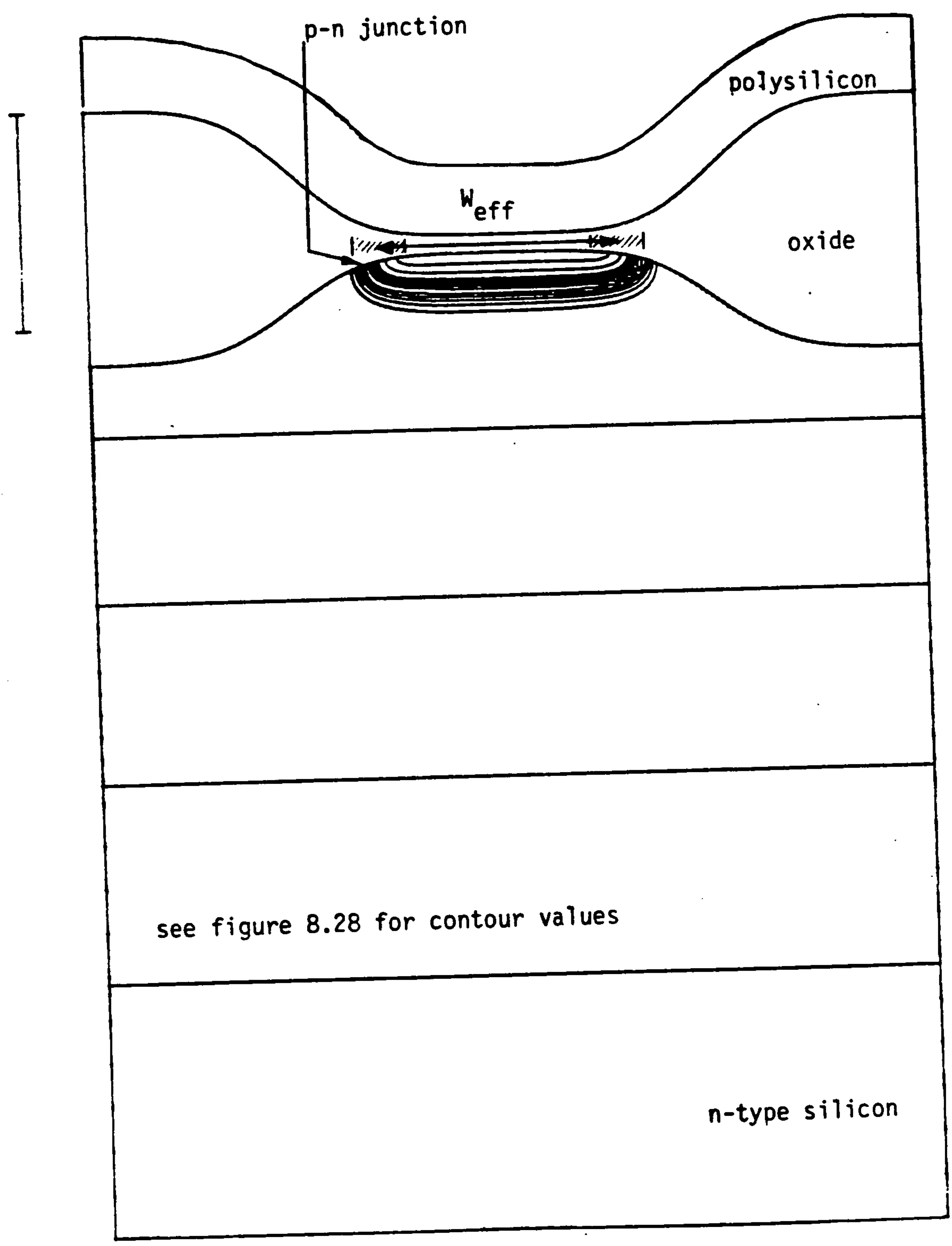


Figure 8.37 : Comparison of measured value of W_{eff} with simulation results for the PMOSFET.

8.36 where the plot of figure 8.25 has been reflected to show the full width of the NMOS transistor, and a polysilicon gate electrode has been added. Figure 8.37 shows the width profile of the PMOS transistor. The measured values of effective channel width are consistent with the extent of the gate oxide before it widens into field oxide /31/.

Such simulation results are useful in the estimation of certain design rules, for example, the minimum separation required to isolate adjacent transistors /48,49/. A conclusion of this study is that the boron channel-stop implant does not have an appreciable effect on the NMOS transistor channel width. Since the bird's beak of current MOS processes is wasteful of wafer area, there is great interest in using a more abruptly changing oxide profile to improve packing density of VLSI circuits /50,51/. The analysis outlined in this chapter could be used to optimise dopant distribution and determine effective channel width of transistors which use novel isolation techniques.

CHAPTER NINE : CONCLUSIONS

The importance of computer simulation in semiconductor process technology has been discussed. CMOS technology in particular has been reviewed since it is the subject of the present simulation effort and shall be increasingly important in future years. A comprehensive study of past and current process simulation activity has been presented. A thorough simulation of a p-well CMOS process has been chosen for this thesis.

The accuracy of the 1-D programme 'SUPREM' (Version II) has been evaluated and results are mostly consistent with deep-depletion C-V and SIMS measurements. A method for modelling C-V characteristics of MOS capacitors in CMOS wafers has been developed to accommodate non-uniform doping profiles generated by SUPREM. Furthermore, determination of flat-band voltage for both n-type and p-type doped silicon is possible using the program 'EPCAP'. However, the mathematical formalism must be extended to allow simulation of typical p-channel capacitors in modern CMOS processes, since the existence of a p-n junction near the silicon surface complicates the analysis. One possible solution is to extend the finite difference mesh to cover the oxide of the capacitor dielectric.

Since lateral effects in MOS processes are now important, a 2-D process simulator 'EPIC' has been developed in FORTRAN77 to run on a Digital Equipment Corporation VAX 11/750 computer system running under the UNIX operating system. This unique simulation pro-

gram combines both analytical and numerical models to allow modelling of complete fabrication processes. A non-uniform discretisation mesh offers efficient representation of deep wells of dopants. EPIC has been used to generate the first 2-D simulation results for a p-well CMOS process.

The SUPREM models have been retained wherever possible in EPIC. The ion implantation models were found to be accurate, although, particularly in the case of arsenic, more work is required for multilayer targets. The diffusion of dopants at low concentration levels is well modelled in both inert and oxidising ambients. However, physical models for high concentration diffusion require refinement in order that source/drain regions may be represented more accurately. A detailed simulation of oxide growth using furnace conditions alone has not been attempted in the present work, however such analyses become increasingly important as both gate and field oxide thicknesses are scaled for VLSI.

An approximate model for temperature during a transient anneal by an electron-beam has been developed using an analytical method to allow rapid computation of results. Possible extensions to this work include the use of a temperature-dependent thermal conductivity and specific heat capacity. A more sophisticated model for the beam energy coupling to the silicon is required. Such a general model would require the use of a finite difference or finite element method. Since annealing conditions are not known for situations where thermal equilibrium does not hold, transient annealing is not

modelled by EPIC. In addition to considering rapid annealing, it would also be useful to simulate the phase formation of novel materials such as refractory metal silicides.

No 2-D simulator has yet been reported that models both wafer topography during material deposition or etching, and doping level in the silicon. Such a simulator will be of prime importance in the future since is critically dependent on mask edge profile during ion implantation at small geometries. This also implies that simulation of photolithographic techniques is equally important.

Recent advances in technology provide motivation for an increased simulation effort. An extension of the present work would be to use EPIC to simulate a twin-well CMOS process. Process simulation can indicate how far existing processes can be scaled, as resolution limits improve. Simulations can aid optimisation as well doping levels, and determine how close to well boundaries transistors can be placed. The conventional LOCOS method of growing the field oxide will eventually be replaced by another isolation technique. Charge redistribution during oxide formation can have important implications for device operation. The development of trench isolation, for example could benefit from a general 2-D oxidation and diffusion simulation. While EPIC contains sophisticated numerical models for impurity redistribution, the program uses an implicit finite difference method on a non-uniform mesh for diffusion in a non-oxidising ambient only. An implicit method for problems of simultaneous oxidation and impurity diffusion would allow more effi-

cient computation of results. This approach requires the solution of a matrix equation for each time step, however larger time steps are possible without inducing numerical instability.

It is evident that processing technology is advancing more rapidly than the subject of process simulation. However, improved processing equipment offers a higher degree of control and hence, less statistical variation in wafer characteristics and so allows more effective research into basic physical and chemical mechanisms.

The step forward to 3-D simulation of processes is too demanding of current computer systems. The 2-D analytical method for modelling ion implantation and subsequent diffusion of impurities could be extended to simulate, for example, CMOS wells in 3-D. However, faster computers and an increased use of parallel processing for matrix operations will eventually allow a 3-D numerical treatment of general doping profiles. It is estimated that 3-D analyses of wafer topography and structure will become important for wafer dimensions below 0.5 micron.

The combined use of process and device simulators is becoming increasingly important to minimise process design time. Such tools allow tailoring of active transistor characteristics and also facilitate reduction of parasitic effects. A good example to which this philosophy can now be applied is the composite bipolar - MOS or 'BI-MOS' technology. It can therefore be concluded that process simulation has a significant role to play in the advancement of semiconductor technology.

APPENDIX A : EPIC Program Structure

EPIC is a 2-D process simulator written in the FORTRAN77 programming language. While the software has been developed on a Digital Equipment Corporation VAX 11/750 computer system running under the Berkeley UNIX operating system, it can be transferred, with only minor modifications, to other systems supporting a FORTRAN77 compiler. Program structure is summarised by figure A-1.

The process parameters are entered interactively and then the fabrication steps are simulated sequentially. The models used for each step are summarised below.

(i) Ion Implantation

- a Pearson IV profile is assumed for the vertical direction, except for the analytical model and implantation through a non-planar surface, which uses a Gaussian profile.
- a Gaussian distribution of ions is assumed for the lateral direction.

(ii) Diffusion

- an analytical method is used for the diffusion of Gaussian implanted profiles assuming a contant diffusivity D.

- the ADI method is used for diffusion of arbitrary initial profiles of low concentration.

- the implicit Crank-Nicolson method is used for high concentration profiles.

- an explicit finite difference method is used for the moving boundary problem of simultaneous diffusion and oxidation.

(iii) Oxidation

- the Deal-Grove model is used for oxide growth in the vertical direction.

- an empirical fit based on SEM measurements is used for the lateral variation.

(iv) Etching and Deposition

- a simple model based on experimental measurements is used to track the wafer surface during material removal and deposition.

- only low temperatures are used so no impurity redistribution takes place.

Photolithography is not simulated by EPIC, however the offsets

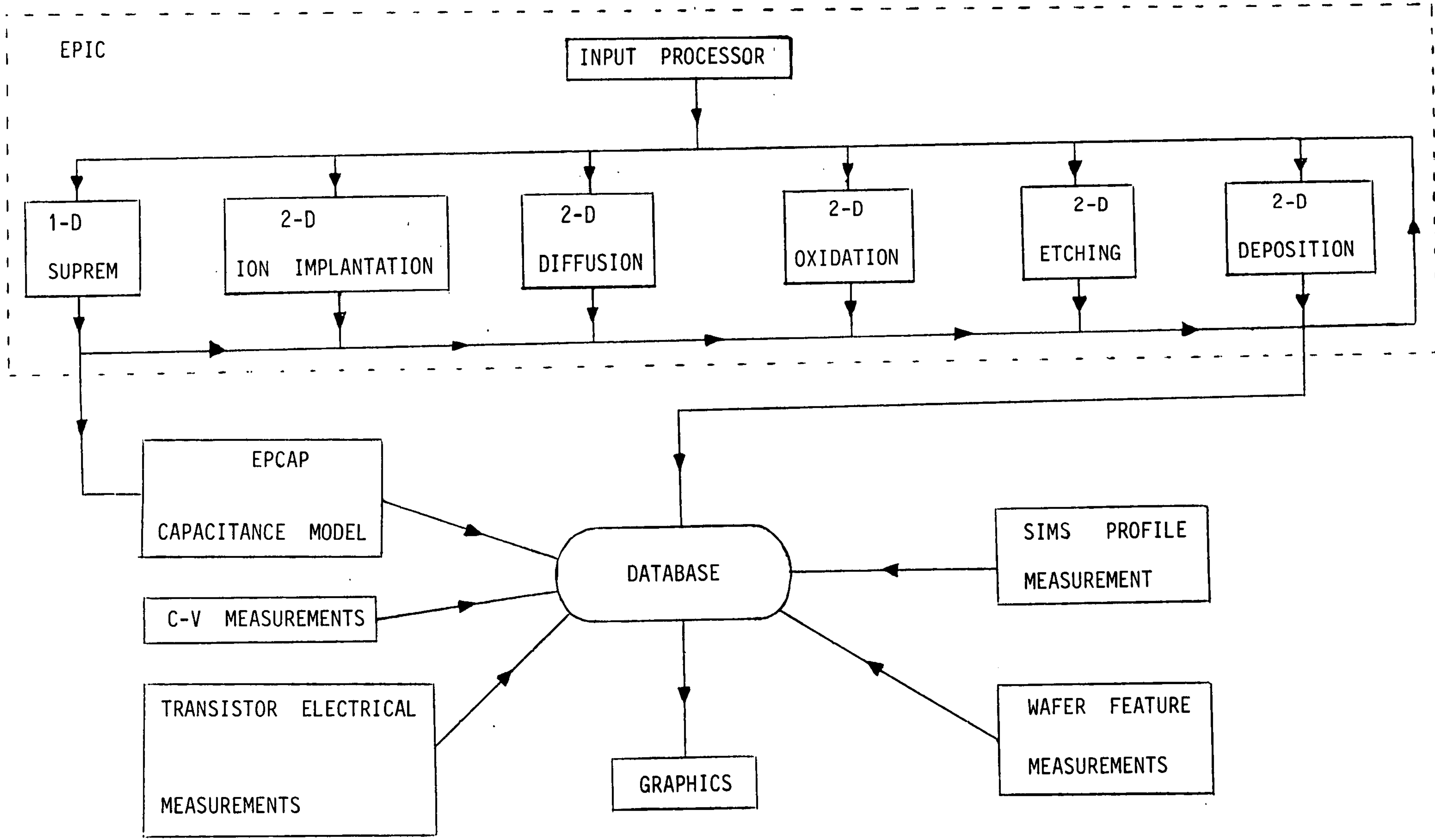


Figure A.1 : EPIC Program Structure and Experimental Data Acquisition.

occuring between the chrome mask and the wafer pattern are accounted for.

1-D simulation results generated by SUPREM can be added to the EPIC simulation grid using cubic spline interpolation and repeated througnout the 2-D array. In this way, SUPREM becomes a subset of the EPIC simulator. 1-D impurity profiles can also be fed to the program EPCAP for capacitance modelling.

Wafer measurements are carried out by a variety of experimental techniques as summarised in table A-1.

Simulation results and experimental measurements are stored in a central database and can be extracted for display on a graphics terminal or hardcopy plotter. 2-D distributions of impurities can be represented by contour plots or 3-D isometric views. Contour plots are useful for quantitative analysis of impurity profiles, but isometric views show minima and maxima in distributions more clearly.

Execution times of simulation runs depend on the number and complexity of process steps, and also on the number of grid points used. The analytical model for ion implantation and diffusion requires less than one minute of CPU time. However, the simulation of a complete fabrication process in 2-D requires several hours of CPU time. On the other hand, the fabrication of CMOS wafers normally takes at least three weeks and may disrupt production flow with

Measurements	System
1-D Impurity Profile	SIMS (Loughborough Consultants Ltd) Hewlett-Packard HP4061 deep depletion C-V
Film thickness	Nanometrics Film Thickness Computer Hewlett-Packard HP4061 high frequency C-V
Linewidth	Nanometrics Critical Dimension Computer Vickers Image Splitting Microscope
2-D Wafer Cross-Section	Cambridge Instruments SEM
MOSFET Electrical Data	Keithley S300 Parametric

TABLE A-1 : Measurement Systems for Wafer Analysis

non-standard process steps.

The integration of both process simulator and wafer measurement equipment as part of a Computer-Aided-Engineering (CAE) database system is important for production efficiency in VLSI.

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