Integration of Software Tools to Aid the Implementation of a DFM Strategy

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Abstract

With the increasing complexity and cost of semiconductor manufacturing there is a drive to maximise profits through higher quality production and reduced time to market. This has created a need for more efficient development tools to help reduce the demand placed on designers and development engineers.

This thesis reports on the design and operation of three software tools that have been developed to integrate commercial analysis packages into an existing TCAD framework. FASTT (FActory Simulation in Total TCAD) and CASTT (Cost AnalysiS in Total TCAD) automate the creation, simulation and extraction of results of factory and cost of ownership models respectively, whilst MASTT (MAnufacturing execution System in Total TCAD) ensures that up-to-date modelling data is readily available. Together they enable faster and simpler analysis of manufacturing issues than is the case with traditional model building techniques. This enhances the existing development tool set and for the first time allows manufacturing analysis to become a routine part of process development.

The thesis introduces the background associated with process development, the existing tool-set and the packages integrated by FASTT, CASTT and MASTT. Examples are used to illustrate the ease of use of the software tools and to highlight their potential. These include: the use of FASTT to identify potential production bottlenecks and capacity; identifying low cost production for a range of potential process options using CASTT; cycle time, throughput and cost of ownership analysis using both FASTT and CASTT to highlight the manufacturing differences of alternative dielectric process steps and finally, the role of MASTT during TCAD analysis to identify corrective processing after wafers have received an incorrect implant.

Declaration of originality

I hereby declare that the research recorded in this thesis and the thesis itself was composed and originated entirely by myself in the Department of Electronics and Electrical Engineering at The University of Edinburgh.

Vidar K. Nilsen

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Acronyms and Abbreviations

ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
CAM	Computer Aided Manufacturing
CASTT	Cost AnalysiS in Total TCAD
CIM	Computer Integrated Manufacturing
COO	Cost Of Ownership
CSV	Comma Separated Variable
DFM	Design For Manufacturability
DOE	Design Of Experiment
DRAM	Dynamic Random Access Memory
FASTT	FActory Simulation in Total TCAD
GUI	Graphical User Interface
IC	Integrated Circuit
MASTT	MAnufacturing execution System in Total TCAD
MES	Manufacturing Execution System
MOS	Metal On Silicon
MOSFET	Metal On Silicon Field Effect Transistor
MTBA	Mean Time Before Assists
MTBF	Mean Time Between Failures
MTTA	Mean Time To Assists
MTTR	Mean Time To Repair
MTTT	Mean Time To Test

ONO	Oxide Nitride Oxide
PM	Preventative Maintenance
PROD	Part, Procedure, Recipe, Operation and Document in PROMIS
RSM	Response Surface Methodology
TCAD	Technology Computer Aided Design
TWB	Taurus WorkBench (TMA WorkBench)
WIP	Work In Progress
VWF	Virtual Wafer Fab

Chapter 1
Introduction

In order to maximise efficiency within semiconductor production there is a benefit in incorporating the analysis of manufacturing issues within the development cycle for new or improved processes. The following chapter discusses the key issues of process development and outlines the role simulation tools can play within this field. The motivation and aims of this study are presented and a brief description of each of the following chapters is given.

1.1 Overview

> *"A well-designed product is far less costly to maintain throughout its product life. A dollar wisely invested in the design, development and pilot production phase can save thousands of dollars by avoiding poor performance in the field"* [1]

This is especially true within the field of IC manufacturing as designs and processes continue to become more complex and sophisticated. The drive to smaller device geometries required to meet this complexity and the associated increase in wafer size has continually reduced the production cost per unit function of an IC [2]. This has resulted in an increasingly financially important and expanding market that, despite recent fluctuations, shows little evidence of abating.

To ensure a competitive stance in this market place it is essential to ensure that the best use is made of available resources, especially given that today a new facility costs in the region of 1-2 billion US dollars [3]. This can be achieved in a number of ways, most notably through maximising manufacturing efficiency and by reducing production costs. To achieve this a Design For Manufacturability (DFM) strategy should be adopted.

1.2 DFM - Design For Manufacturability

Design for manufacturability is a philosophy that aims to improve the quality of products being produced. The key to DFM lies in continually considering the manufacture of the product, from the initial design and development stages through into its production. Identification of areas of the design or process that can be altered to improve the quality or yield of the product is critical to commercial success in manufacturing. There is little point in producing a sub-standard quality product that fails to routinely meet the required specification. For example, within IC manufacturing there may be a high degree of variability during processing which can severely effect device operation. However, if such variability is known about during the design stages, analysis can be performed in order to identify the design choice least susceptible to the variations. This thesis aims to extend this philosophy beyond the operation of the device being produced by considering the effect of these choices on the production environment to ensure cost effective production.

1.3 Process Development

The term *process development* conveys the following two meanings within the field of semiconductor manufacturing: On one hand there is the development of existing semiconductor processes and on the other the development of new processes and technologies. The similarity lies in the skills and tools required for either type and therefore the role of a development engineer within a IC manufacturing environment normally comprises of a combination of both. Regardless of which type is undertaken the minimum requirement is that of identifying a process which yields a correctly operating device within given specification limits. Ideally, this should also identify the optimum processing conditions in terms of performance, manufacturability and cost.

However, the rationale for process development is not so closely matched. For example, during the development of an existing process the costs incurred (engineers time, software costs, materials etc.) and any subsequent implementation of the revised process must be weighed up against the expected gain in order to assess whether or not the development is a

viable proposition.

In the case of a new process to produce new products the main issue is often in terms of time to market. This is due to the high rewards of attaining market share and being able to sell product at a higher level through lack of competition [4]. Any delay in time to market for a new or innovative product can have a significant impact on profit so the cost of development plays a less significant role than the time it takes to release the process to production.

Success for either scenario relies on the ability to accurately forecast the operation of the ICs, the effect on yield and the impact on the production line. Being able to forecast the impact of these issues quickly and accurately is the key to maximising the available resources and is the focus of a complete DFM strategy.

1.4 Manufacturing Issues and Process Development

The IC manufacturing industry can loosely be sub divided into two areas. High volume, mass market production associated with devices such as microprocessors, DRAM and voltage regulators. In contrast, a large segment of the IC market tends to comprise of lower volume ASIC (Application Specific IC) production [5], which use common processes to produce a variety of devices which may differ by as little as a single masking layer, resulting in numerous small production runs. Each has its own goals in terms of efficient production but both must try to maximise profit without unduly compromising product quality in order to remain competitive within their field. To achieve this manufacturing issues such as cycle time and production costs must be minimised whilst maximising the fab's throughput and ensuring the IC meets the required specification. However, the balance of these issues differs depending on the application. For example, a low volume manufacturer may place more of an emphasis on a low cycle time rather than on saving a few cents per wafer, whereas a high volume IC manufacturer may prefer to ensure a high throughput with a lower manufacturing cost rather than focusing on cycle time.

Despite the differences, one issue is common to all IC types of production: the ability to forecast manufacturing issues allows action to be taken before matters become a problem.

This can have significant repercussions in terms of the time to market of a product. Consider the situation when a process calls for the use of a piece of equipment which is already heavily utilised and can not cope with the proposed increase in capacity. If such situations can be accurately forecasted, using tools like factory simulation, it may be possible to either alter the process to eliminate or reduce the additional loading on this equipment type or to purchase and qualify additional equipment prior to the process being released to production. In either situation the problem can be addressed before it becomes a major manufacturing issue and therefore the potential exists to significantly reduce the time and cost of the development cycle.

1.5 Tools to Aid Process Development

A DFM framework (total TCAD) has been developed which enables the technological aspect of IC designs to be analysed and optimised using a combination of TCAD, DOE and RSM techniques [6]. This framework and its elements are described and discussed in chapter 2. However, in addition to this framework, there are a number of other tools available to engineers within process design and development. A large proportion of these cater for the analysis of the operation of the IC and the procedures involved in its development such as the extraction and modelling of the IC's physical parameters. As well as these there are also tools such as factory simulation and Cost Of Ownership (COO) models, which along with the Manufacturing Execution System (MES), enable the implications on the manufacturing environment to be assessed. It is these elements which must be incorporated into the framework to ensure that their usage becomes a common part of an overall DFM strategy within IC development. By doing this it will be possible for a more rounded analysis of design choices to be performed and potentially enable more efficient use of the existing resources.

Unfortunately, MES, TCAD and factory simulation software have been developed independently over the years. Although organisations like Sematech and SEMI have carried out some work into the development of a common data interchange format none exists and those in development such as the MDS (Modeling Data Standard) have not considered the

inclusion of TCAD. In order to bring all of the previously mentioned elements together within the total TCAD framework a method by which to transfer data between applications is essential.

1.6 Motivation and Aims of this Study

The practical implications of altering an existing process or introducing a new one are seldom considered during the development cycle. They are more commonly only evaluated once a design choice has been made. At this stage any possible ramifications to the manufacturing environment are then considered and production issues identified. However, after a process has been all but finalised any steps to alter its design at this point incur a significant increase in development time and cost. As such, it is unlikely that as long as it is still possible to manufacture the new or revised process that any further modifications would take place.

The common usage of TCAD simulation software for process development ensures that for many new and existing processes a complete technological history of the process is available. That is, a complete description of the chemical and physical effects on the wafer that occur during process flow, although for the most part, non-device relevant steps such as laser scribe and visual etch inspection are omitted. Given that TCAD information is already available within the existing framework it provides a starting point from which to incorporate the investigation of manufacturing issues into the framework.

Using the existing total TCAD framework as a basis for developments this thesis aims to incorporate a method of automating the analysis of manufacturing issues within the existing TCAD framework. Given the time it takes to collate the information required for each of the models this is essential if they are to ever be routinely used for process development. It is also important that the results of the manufacturing analysis are readily made available to the user in a familiar format, allowing them to be incorporated with the results of any TCAD analysis. By automated construction of factory simulation and COO models from information extracted from a facility's on-line MES (Manufacturing Execution System) it becomes possible to ensure that any manufacturing and cost analysis is performed using up-to-date information. This is also true of TCAD analysis when existing TCAD data is

stored on the MES and updated when any alterations to the process steps occur. In order to realise these aims three pieces of software have been developed as part of the work reported in this thesis:

- FASTT (FActory Simulation in Total TCAD)
- CASTT (Cost AnalysiS in Total TCAD)
- MASTT (MAnufacturing execution System in Total TCAD)

1.7 Thesis Plan

The following section outlines the content and focus of each of the remaining chapters within this thesis. Chapters 2 and 3 provide a background to the elements within the existing total TCAD framework and those incorporated for the first time because of the work reported in this thesis. Chapters 4-6 detail the rationale behind their integration, how it was achieved and the resultant benefits. Finally, Chapter 7 reviews the work undertaken, discusses the implications and suggests areas for potential development.

Chapter 2: The Existing Total TCAD Framework. The existing total TCAD framework and the elements incorporated within it are described. A general background of each element is given, with particular emphasis to their role in a DFM strategy for process development.

Chapter 3: Manufacturing Analysis Tools. The new elements which have been incorporated within the framework because of the work reported in this thesis are described. A general background of factory simulation, COO and MES is given, emphasising the features they bring to a DFM strategy.

Chapter 4: Incorporating Factory Simulation into Total TCAD. This chapter examines the main work reported in this thesis. The development of FASTT, a piece of software that enables the integration of factory simulation into the existing total TCAD framework, is outlined. The role of the individual elements integrated by FASTT are discussed and its operation is described together with examples of its potential uses. This allows manufacturing

issues such as cycle time and capacity issues to be analysed at a far earlier stage in the development cycle than is currently common place. More importantly, this can be performed with less input from the user than it would take to perform the analysis without the aid of FASTT.

Chapter 5: Incorporating Cost of Ownership Analysis into Total TCAD. This reports on the inclusion of a COO calculation within the framework in a similar way that the inclusion of factory simulation is detailed in chapter 3. Through CASTT the COO calculation enables a quick and simple method of generating the cost of each individual step within a process flow. This allows forecasting and comparison of actual manufacturing costs, again, at a much earlier stage in the development cycle than is currently common place.

Chapter 6: Automated Generation of Up-to-date TCAD Models. Two main issues are focused on in this chapter. During the development of FASTT and CASTT the need for supplemental processing information was identified. MASTT addresses this by automating the generation of extraction script to interrogate the factory MES to provide up-to-date manufacturing information required for factory and cost model generation. Additionally, because the MES holds the most current processing information, a methodology whereby the TCAD code itself can be stored within the MES is also presented. This ensures that the code is kept up-to-date with the current process, reducing the need to manually update and check the code before TCAD analysis is performed. As with the previous two chapters the potential benefit of using MASTT is also demonstrated with the aid of an example.

Chapter 7: Review, Discussion and Future Work. The work reported in this thesis is summarised and concluded. Suggestions for further work and improvements to the software are made.

Chapter 2
Total TCAD

This chapter provides a degree of background to the work carried out previously on developing the total TCAD framework. It is this framework which has provided the basic building blocks on which the work which will be reported in the following chapters is based. The existing total TCAD framework is introduced, its usage and importance are discussed and the main features of its individual elements described.

2.1 Introduction

The original total TCAD framework [6] is a set of software tools integrated to aid process design and development. This was made possible by a piece of software called Calphurnia [7] [8] [9] which combined TCAD simulation software with an experimental design and analysis package in order to automate the fitting of response surfaces to simulated data. The key to the framework is the ease by which data can be passed between the individual elements with minimal input from the user, reducing the time it takes to develop new or existing process flows. The relationship between these elements for one of the original systems is illustrated in figure 2.1.

Combining DOE (Design Of Experiments), TCAD and RSM (Response Surface Methodology) packages provides a system capable of driving TCAD analysis for process development. As such these three elements formed the basis of the original total TCAD framework. The DOE package enables experiments to be defined which can then be performed using TCAD process and device simulation software. The results of these simulations can then be analysed using techniques such as RSM and design choices made accordingly.

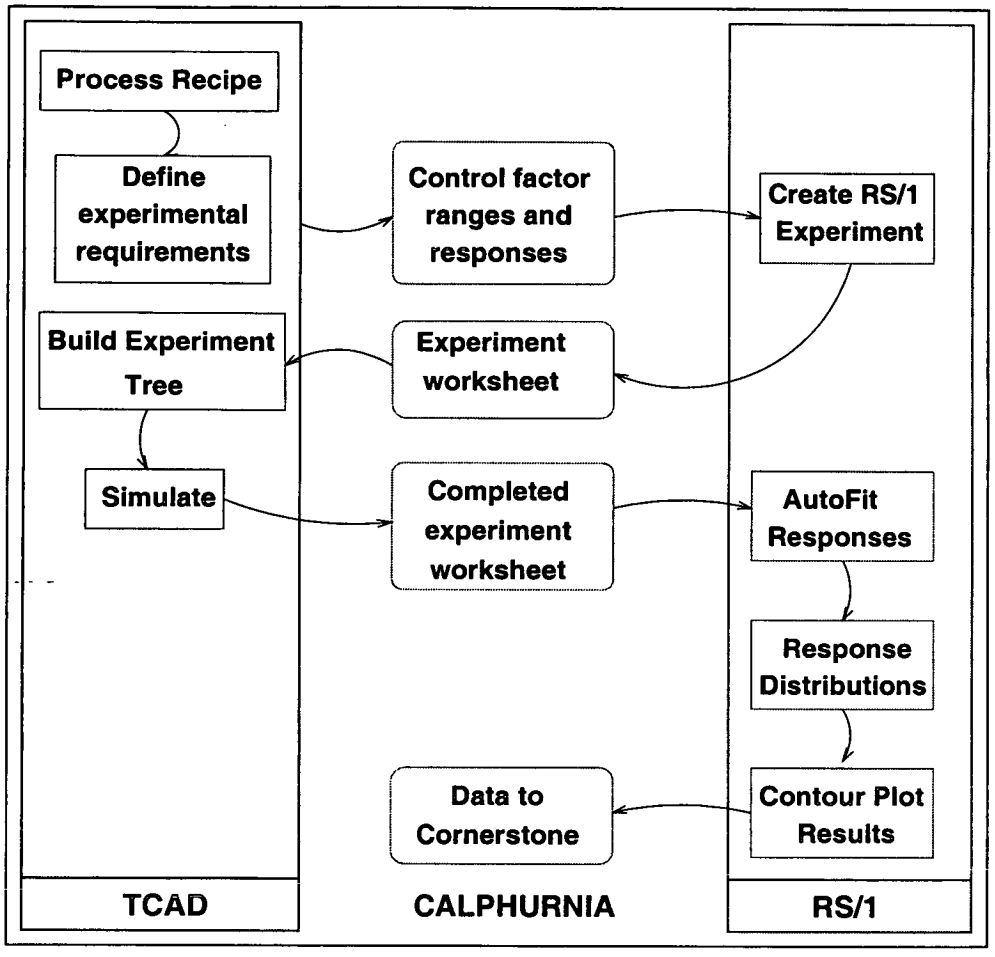


Figure 2.1: *The integration of TCAD, RS/1 and Cornerstone using Calphurnia in the original total TCAD DFM framework.*

The following sections provide an overview of individual elements within the original framework. Firstly, the core element of TCAD is discussed with particular reference to process and device simulation and virtual wafer fabs. The use of DOE and RSM techniques for defining and analysing TCAD experiments is then described. This is followed by a brief look at commercial TCAD frameworks that are the cornerstone of today's TCAD analysis.

2.2 TCAD - Technology Computer Aided Design

Simulation and modelling is widespread throughout engineering fields and semiconductor manufacturing is no exception. TCAD (Technology Computer Aided Design) is the area of computer simulation and modelling related to the design, development and manufacture of integrated circuits. In particular, TCAD software enables the simulation of semiconductor devices and circuits as well as the processes that are used to fabricate them. Thus TCAD has the potential to reduce not only trial fabrication costs but can be used to identify device or process designs that are the least susceptible to process variations [10]. The decreasing device dimensions and increasing complexity of IC designs and processes means TCAD is seen as a key tool in the design, development and manufacture of semiconductors [11].

Since the cost of processing 200mm experimental wafers can be in the thousands of dollars and takes several days [12] (more normally weeks) to process there is an obvious benefit in using simulation for as much development as possible. However, as with most simulations the accuracy is dependent upon the models used. In TCAD a significant effort is required to ensure that the models used are correctly calibrated [13]. This is further complicated when TCAD is used to examine leading edge geometries where there is little parameter or measurement data available from which to construct a model in the first place [14]. Despite this TCAD has been shown to be beneficial in analysing a number of situations and hence represents a useful analysis tool during process development [15] [16] [17].

Although there are many aspects of TCAD which can be discussed, this section concentrates on providing a brief overview of the development of TCAD as we know it today. Firstly a general background to both process and device simulation is given, which when combined formed the basis of TCAD. Their integration is discussed, as are the TCAD frameworks that have emerged from these initial systems to facilitate the use of a range of TCAD tools that are available today.

2.2.1 A History of Process Simulation

The continual development of processes to produce more complex devices has always pushed the need to better understand the effects of semiconductor processing. Process simulation is the area of TCAD concerned with the physical structure of a semiconductor wafer. At its most basic level, process simulation is a set of mathematical models used to model the action and interaction of individual process steps on a silicon substrate. From the heyday of bipolar technology in the 1960s through to the early days of MOS technology in the 1970s mathematical models were being developed for steps such as impurity diffusion, oxidation of silicon and ion implantation [18] [19].

However, many of these earlier models relied upon analytical equations which became inadequate as what were second order effects needed to be considered due to the increased complexity of the devices being produced. With the availability of increased computing power in the late 1970s, the development of more complex numerically based models became possible. This led to the development of general purpose process modelling software, enabling the simulation of a number of process steps within the same package [20].

The first generally available process simulation software was developed at Stanford University in 1977. SUPREM (Stanford University PRocess Engineering Models) [21] provided a means by which a whole process could be simulated. By transferring the outcome of a simulation of one process step to be the input of the next, the complete structure can be modelled within the same piece of code. This allows analysis of either the process as a whole or a subset of it, providing the user with a greater insight to the affect of each step on the final structure. Subsequent revisions of SUPREM [22] [23] [24] and other process simulators were developed to cater for the continually advancing technologies and geometries. In 1979 Stanford's SUPRA [25] was one of the first tools for 2-D analysis and was the fore runner to many others, most notably SUPREM IV [24]. More recently we have seen the advent of 3-D process simulators driven again by reduced feature size and enabled by advances in computing power [10].

2.2.2 A History of Device Simulation

Device modelling has been a feature of semiconductor development since the days of the first transistor in the 1940s. As with process simulation it has evolved, becoming increasingly more accurate with availability of increased computing power. Device simulators, or rather the algorithms and computer programs for calculating device models, have been available since the late 1970s. Tools such as CADDETT [26] which was developed in 1978 to model the avalanche breakdown in a MOSFET by simultaneously solving the Poisson and minority-carrier current continuity equations [27]. However, the situations simulated by CADETT could also be solved by using less detailed models in alternative tools such as SDVICE [28] and GEMINI [29], both 1980. These simulators provide good approximations to the more detailed CADETT calculation but do so faster (in the case of SDVICE by a factor of 10). This trade off of speed vs. accuracy is a common scenario in device simulation and one in which more control was made possible by through the use of 2-D device simulators such as PISCES [30] and MEDICI [31] through the use of user defined grids. This allows the user to specify the areas of most concern and solve for a greater number of nodes in those regions than in the rest of the device, giving greater control over limited resources.

In the 1980s further advances in computing power resulted in further development of 2-D device simulators and the introduction of 3-D simulators such as DAVINCI [32] to address the needs to model the 3-D effects of decreased device geometries. Advances in computing power have also made it possible the use CPU intensive techniques such as the Monte Carlo [33] method for solving Boltzmann's transport equations [27], which in 1990 would have taken 100s of hours of CPU time [20] using simulators such as DAMOCLES [34].

2.2.3 Tool Integration

For a number of years the development of early process and device simulators was independent. While some engineers were concerned with the physical and chemical effects of processing others remained more concerned with the manner in which the performance of a device could be modelled. However, if they were combined, such that device simulations were performed using a structure defined by the results of process simulation, the results

of the device analysis could be attributed to the actual processing steps used to create the device. The integration of these tools was the beginning of TCAD as we know it today.

Integration of process and device simulators is, as with all simulations, a matter of compromising accuracy for speed. For example, 1-D simulations of the gate and source or drain regions of an MOSFET can be used to approximate the device profile for simplified 2-D device simulation, thereby improving the speed by removing the need to perform 2-D process simulation. However, for more complex areas of the device better results may be obtained by using a full 2-D device simulator in conjunction with a 2-D process simulator. In such cases in the early-mid 1980s this more detailed analysis would only have been performed where necessary using simplified analysis [35] to reduce the time required. As 2-D process simulators developed and computing power improved, the need to perform 2-D device simulations based on 1-D process simulations decreased only to be replaced by 3-D device simulations based on 2-D process simulations. This is still very much the norm, although since the advent of 3-D process simulators in the last couple of years it is unlikely that it will be long before modelling both in 3-D will be common place.

In order to interface process and device simulators, a method by which to transfer and store profiles independently of particular applications was required. This is partly because of the numerous simulators that were available and partly because of the fundamental differences between process and device simulators. Accurate modelling of a process relies on focusing on the areas where there is a rapid change in dopant whereas device simulation needs to be focussed on the areas of carrier movement. As such, a grid designed for one is seldom the most suitable for the other so rather than transferring a grid an intermediate profile containing geometry and impurity details is used to transfer data between applications [36].

A number of intermediate formats and methods by which to transfer the data have been proposed, in particular: A PIF (Profile Interchange Format) based on a common file format was proposed in 1988 [37] and was extended in 1991, providing an object orientated approach [38] for the storage of profile data and a binary PIF format for use within an integrated TCAD environment [39]. In 1994 the SWR (Semiconductor Wafer Representation) [40] was proposed to meet the demands of the latest set of TCAD tools, also using an objected orientated approach to simplify data transfer between applications. It is

this type of work that has made the development of integrated TCAD frameworks possible.

2.3 The Virtual Wafer Fab

Increases in affordable computing power and the development of TCAD simulation tools and their associated models during the 1980s and early 1990s meant that the use of TCAD within the production environment became a more viable proposition. However, writing effective TCAD code, calibrating it and analysing experiments has largely been limited to specialist users. For TCAD software to become a standard tool for process and device development it needed to become more accessible to a wider audience. TCAD frameworks were developed to address this and deliver all the advantages of TCAD in an environment that the user could relate to.

There are many features which must be incorporated within the design of a virtual wafer fab. In particular, it should be intuitive in its operation, providing not only an easy to use interface but one that draws on the user's existing knowledge of the fab. It must also provide a high degree of flexibility in terms of the simulations it is able to perform by integrating all of the available TCAD packages. This integration is also required to aid efficient running of the simulations on the available resources and to reduce the data storage required by utilising common simulation results. Additionally, since techniques such as DOE and RSM (see following section) have emerged as key tools in TCAD analysis it is essential that methods for creating, reporting and analysing the results of experiments are also incorporated.

Early integrated systems, such as PRIDE [41], SIMPL-IPX [42] [43] developed at Stanford University and others [44] [45], utilised the PIFs discussed previously. By 1995 a number of systems, detailed in table 2.1, had been developed by both commercial companies and in academia.

Today Avant!'s Taurus WorkBench (TWB) [53] and Silvaco's Virtual Wafer Fab (VWF) [54] are perhaps the most widely used packages. Figure 2.2 shows a screen shot of TWB and figure 2.3 gives an overview of how the individual TCAD tools with the Silvaco suite are combined within the framework. These commercial suites are the latest versions of CAESAR

Company	TCAD framework system
Institute for Microelectronics, Vienna	VISTA [46] [47] [48]
ESPRIT project 2197	STORM [49]
OKI Electric Industry	UNISAS [50]
Technology Modeling Associates	CAESAR [51]
Silvaco International	MASTER [52]

Table 2.1: *TCAD framework systems circa 1995.*

(TWB) and MASTER (VWF) shown in table 2.1. Both use a graphical representation of the wafer flow that allows the order and choice of modules within the process flow and the information within them to be easily edited. They also enables users to simply transfer data to the appropriate simulator, other TCAD tool or piece of external software without having to manually alter the data.

2.3.1 Current TCAD Tools and Capabilities

The previous sections have considered both process and device simulation and described how over the years they were combined to form the basis of TCAD, as well as the development of virtual wafer fabs. However there are a large number of specialist simulation tools available from academia and commercial companies like Avant! and Silvaco. The current suite of TCAD tools available from market leaders Avant! and Silvaco are shown in table 2.2 and figure 2.3 illustrates how the Silvaco suite of tools are organised within their TCAD framework - VWF.

From table 2.2 it can been seen that, in addition to the range of process and device simulators tools for modelling lithography, topography and interconnect are also available. The progression of process and device simulation into 2-D and more recently 3-D analysis coupled with reduced feature size has meant that the physical structure of ICs becomes increasing important which has had a significant impact on the design and operation of devices [55]. This has led to the development of tools along with visualisation software to facilitate this type of analysis and parameter extraction software such as Aurora and UTMOST. These enable the engineer to derive device models for use within design tools

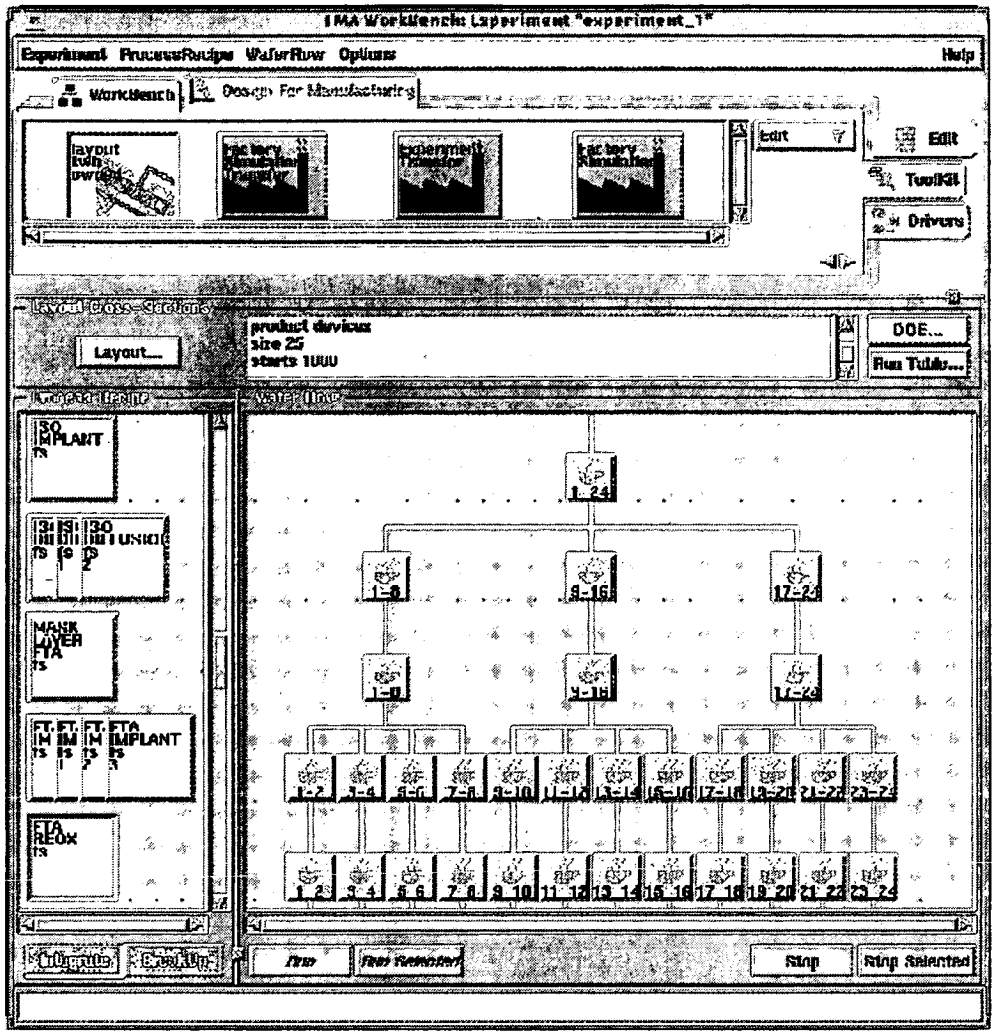


Figure 2.2: *Taraus WorkBench, virtual wafer fab screen shot.*

such as SPICE [56] and are also an essential element during TCAD calibration where the model must be adapted to match the parameters extracted from silicon. As previously discussed all of these tool are available in an integrated package using similar interfaces and a common database, removing many of the complexities of older TCAD packages which facilitates analysis [12].

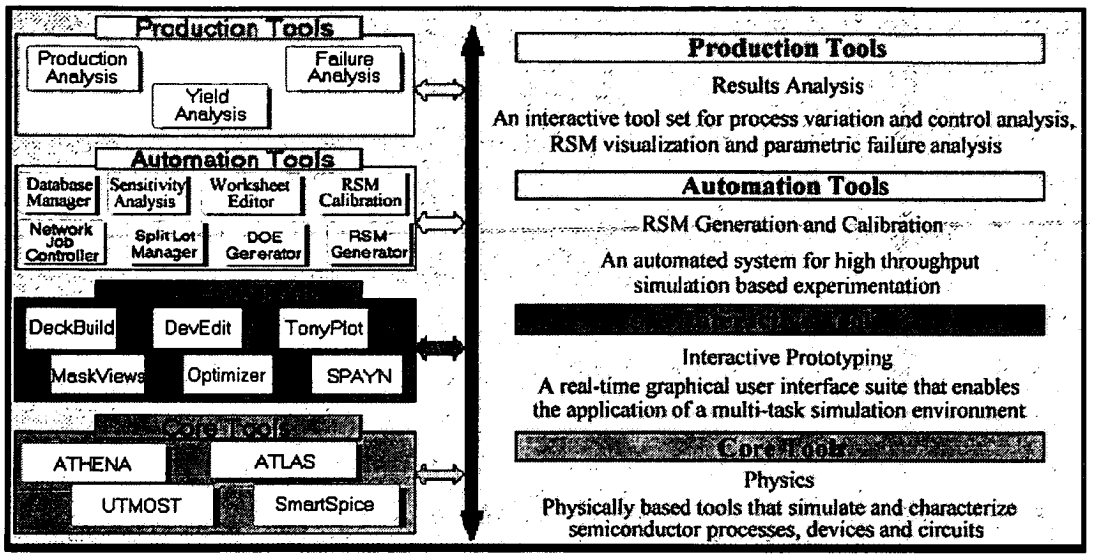


Figure 2.3: *General overview of Silvaco's Virtual Wafer Fab.*

2.4 Process Optimisation

The fabrication of a semiconductor device is a complex procedure involving many, often repeated, individual process steps. Within each of these steps there are numerous factors governing the outcome including the processing equipment which is prone to variation. Hence, attempting to optimise any process can be time consuming, especially as possible interactions between factors must be considered. In order to ensure successful optimisation and gain an understanding of any interactions occurring a structured approach is required. The use of DOE (Design of Experiments) [57] techniques together with RSM (Response Surface Methodology) [58] analysis is one such approach particularly suited for use during process development using TCAD [59] [60] and is discussed in the following sections.

2.4.1 Design Of Experiments

DOE techniques are essential in ensuring efficient experimentation when there are a number of inputs and outputs. This is because if more than one control factor is present there is not always an orthogonal relationship between individual factors and resultant responses. This means that altering one factor at a time and examining the resultant response is unlikely to

Silvaco Products	TCAD Tool Type	Avant! Products
Virtual Wafer Fab II	TCAD Framework	Taurus-WorkBench DFM WorkBench
SSuprem3	1-D Process Simulator	
SSuprem4	2-D Process Simulator	TSuprem4
Lava/Mesa	3-D Process Simulator	Taurus-Process
S-Pisces	2-D Device Simulator	Medici
Device3D	3-D Device Simulator	Davinci
Diamond	3-D Device Simulator	Taurus-Device
Optolith	2-D Lithography Simulator	
Nova	3-D Lithography Simulator	Taurus-Lithography
Elite	2-D Topography Simulator	
	3-D Topography Simulator	Taurus-Topography
Interconnect3D	3-D Interconnect Simulator	Raphael
TonyPlot	Structure Visualisation	Taurus-visual
UTMOST III	Parameter Extraction	Aurora

Table 2.2: *Current TCAD tools from Silvaco and Avant!.*

fully explain what is actually happening. If there are any interactions it would be necessary to test all possible combinations of factors to identify every possible response. This is not a viable proposition for most semiconductor processes because of the large number of control factors involved, typically in the region of 100s to 1000s. To address this issue a number of experimental designs have been developed over the years [61] [62] [63]. As part of the original total TCAD project and subsequent revisions to commercial TCAD software many of these designs have been incorporated into TWB and can be seen in the screen shot shown in 2.4.

The general procedure used to design an experiment which will allow generation of response surfaces comprises of several stages and has been well documented [64] [60] [65] [44]. The general methodology can be summarised as follows: Firstly, all the control factors and responses of interest must be identified. If there are more than four control factors then an initial screening should be performed to reduce the number [66]. The screening process eliminates some of the least important factors, allowing the interactions between the most influential factors to be examined in more detail. Once the control factors have been determined an experimental design must chosen. This is usually performed using a DOE

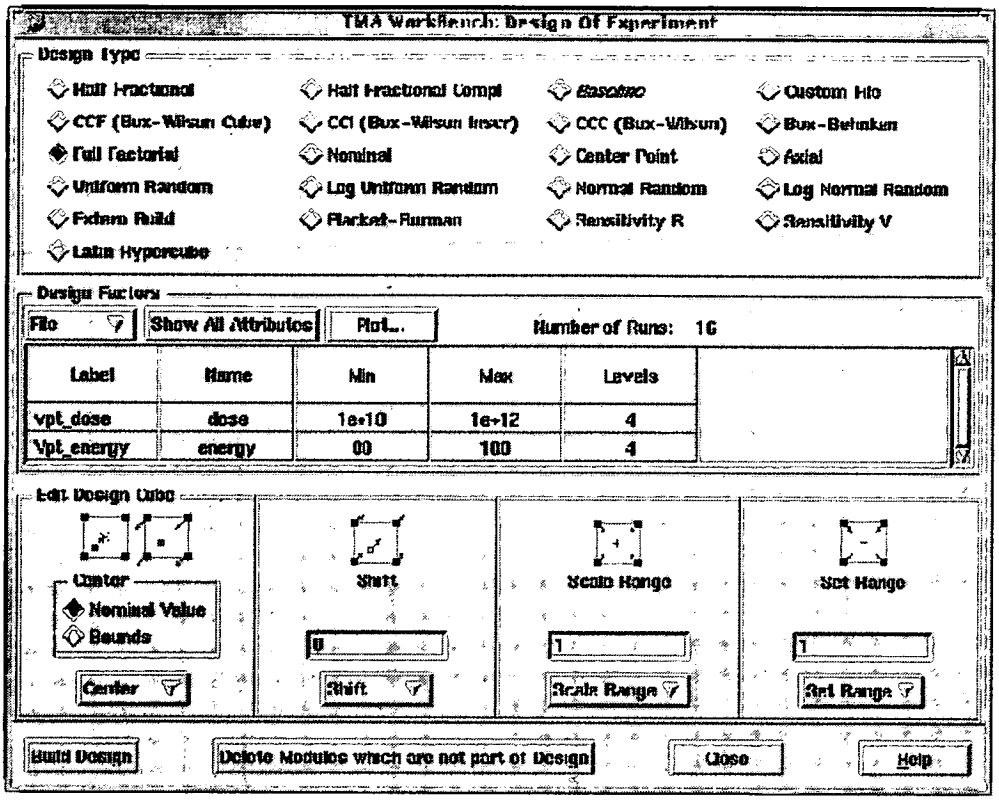


Figure 2.4: *TWB DOE screen shot.*

software package such as RS/1 [67], Calphurnia [7] [8] [9] or the DOE section of TWB [53]. These packages allow the user to select a design that best meets their requirements. The final choice of design depends on two main factors: the resources available to perform the experiments and the type of response that will be fitted to the simulation results. This is particularly important since, for example, the requirements for fitting a quadratic polynomial do not match those required for a cubic.

On completion of the experimental runs polynomial models, typically quadratic or cubic, are fitted to the results, again using appropriate software (e.g. RS/1, Calphurnia, TWB) to generate a model for each response. These models can then be used to predict the response for a combination of control factors other than those that were included within the designed experiment. The models rely on attempting fit the experimental results to low order polynomials, ensuring that a general trend is fitted which also takes into account a degree of experimental randomness with the results.

2.4.2 Contour Plots

Response surfaces plotted as contour plots provide a useful tool for interpreting the effect on a number of responses when two control factors are varied. For example, figure 2.5 shows a single contour for each of the responses, representing the specification limits for the transconductance (G_m), punch through voltage (V_{pt}), series resistance (R_{sd}) and peak electric field (E_{peak}). When the constraints of these responses are plotted together, as in figure 2.5, the combination of factor settings which meet given criteria can be easily identified.

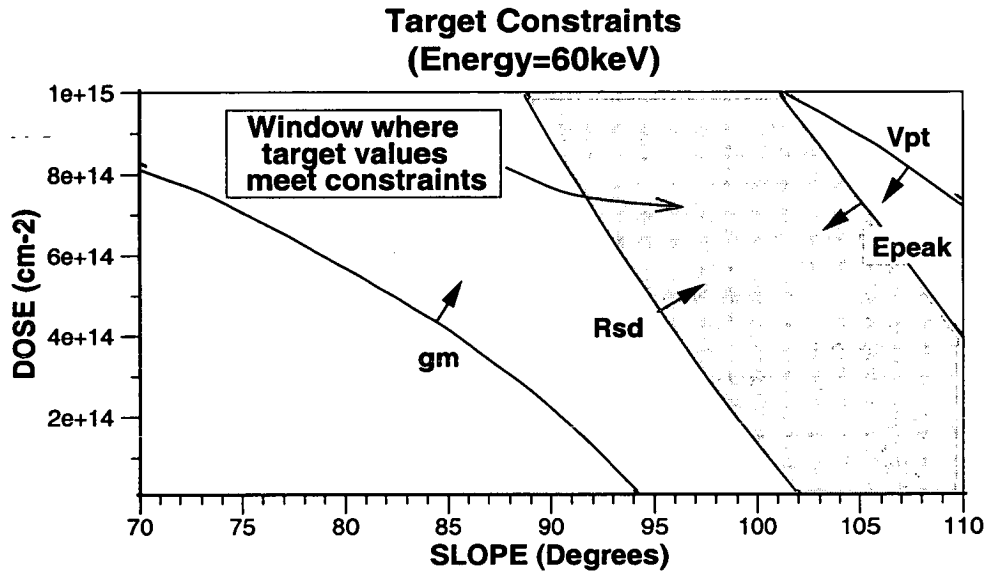


Figure 2.5: *Response surfaces plotted as a function of implant dose and side wall slope for a fixed implant energy, shaded area indicates where specifications are met [68].*

However, the contours in figure 2.5 represent the responses from the process target values, which do not take any process variation into account. Since there will be some degree of variation from the equipment settings not all combinations will guarantee that each constraint will be met. Therefore, further analysis must be carried out using the distribution of the input factors to identify the response distributions, rather than relying on a single *ideal* value. Figure 2.6 shows the contours for each response for the tails of the distribution of the process variation. It can be seen that all four have come closer together and in particular V_{pt} now affects the choice of factor combination. It should also be noted that the highlighted area that shows the solutions which are robust to the expected manufacturing variability during

processing is not in the centre of the previously identified area. This highlights the need to perform the additional analysis rather than using a factor combination from the original analysis. Once this type of analysis has been performed within the total TCAD framework the response models can be used to predict the response distributions resulting from control factor variability [69].

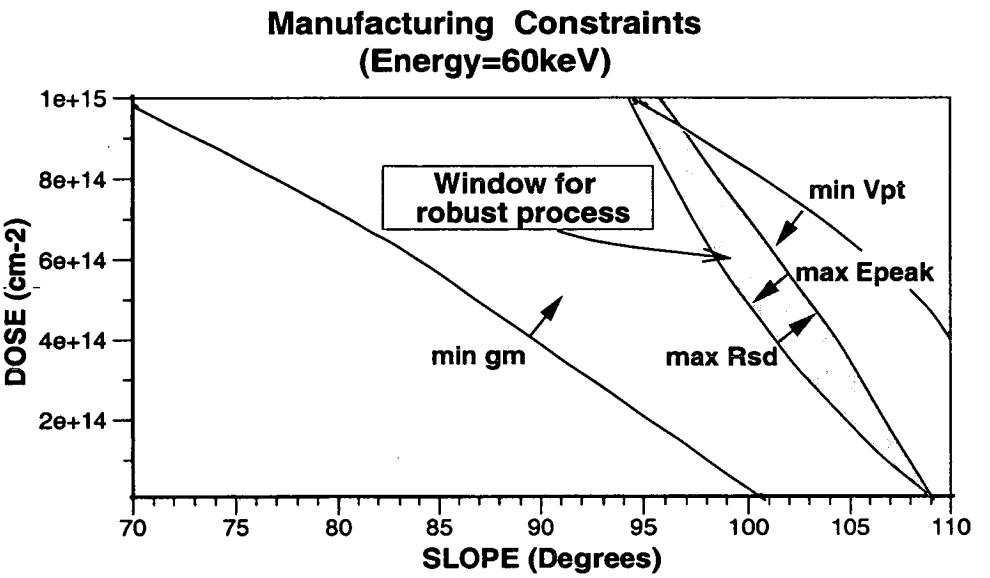


Figure 2.6: *Response surfaces plotted as a function of implant dose and side wall slope for a fixed implant energy, shaded areas indicates area where the process is robust to expected manufacturing variations [68].*

2.4.3 Response Distributions Analysis

The key to the accurate prediction of response distributions lies with the fit of the response model and the accuracy of the control factor distributions. Figure 2.7 indicates how a response distribution can be effected by the slope of a response. The gradient, or first derivative, influences the standard deviation, as shown in figure 2.7 (a) and the rate of change of the slope, or second derivative, the skewness as shown in figure 2.7 (b) [69]. Given a well fitted model and accurate distribution for each control factor it is possible to accurately predict the distribution of each response and hence identify a robust solution [68]. This is crucial in ensuring that accurate manufacturing distributions can be predicted.

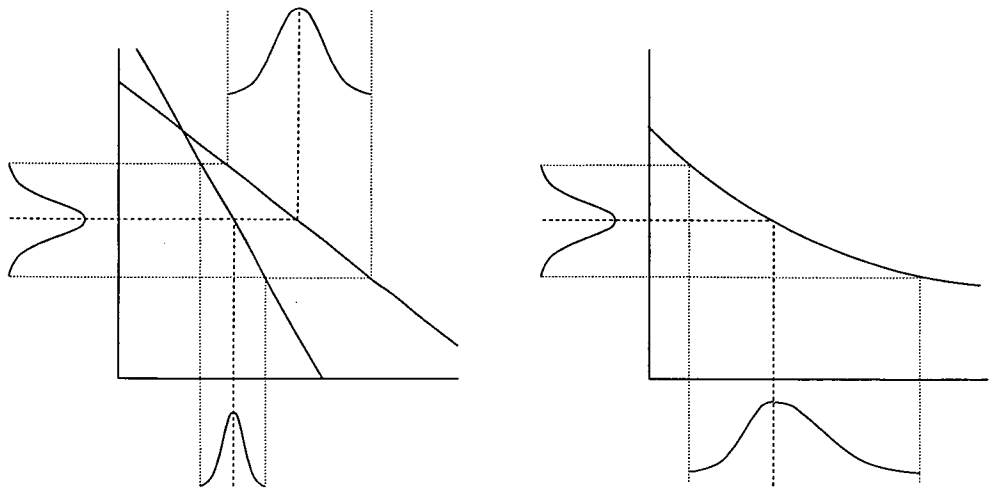


Figure 2.7: *Examples of how the slope affects (a) the standard deviation and (b) the skew of a distribution [69].*

2.4.4 Covariance Modelling

In contrast to standard experimental techniques, simulation results have no random error associated with them and so there is every justification in fitting a surface through all the data points. Fitting a covariance response to the results ensures that the resultant model passes through each data point. This is done by by initially fitting a low order polynomial model to the results and then *pulling* it to make it pass through each of the data points [70] [71] [72].

In order to demonstrate the effectiveness of fitting a covariance model in comparison to traditional polynomial models a known response can be examined. Figure 2.8 shows contour plots for the known response, together with quadratic, cubic and covariance models fitted to the 16 data points indicated by the * on the plots. The known response is given by:

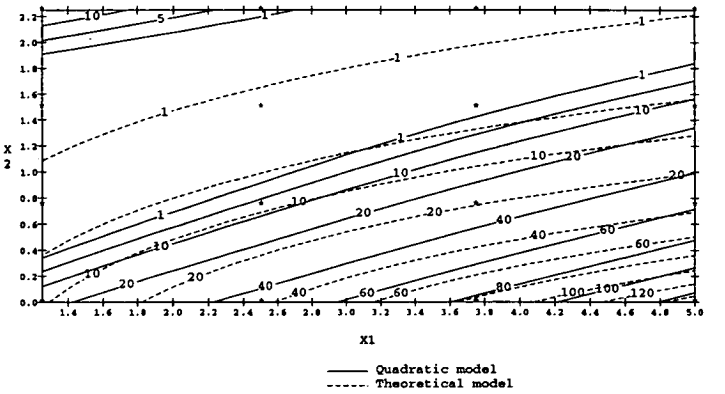
$$Y = \frac{15.0X1^2}{1.0+1.5\times10^{2.5X2}} \qquad (1)$$

The R^2_{adj} value of 0.985 for the cubic model would suggest that its fit is very good but even it is struggling to fit equation (1) in this region. However, it is clear that the covariance model provides a more accurate representation of the response than either of the polynomial models, particularly the region of low X1 and high X2. Thus, for simulated data the fitting of a

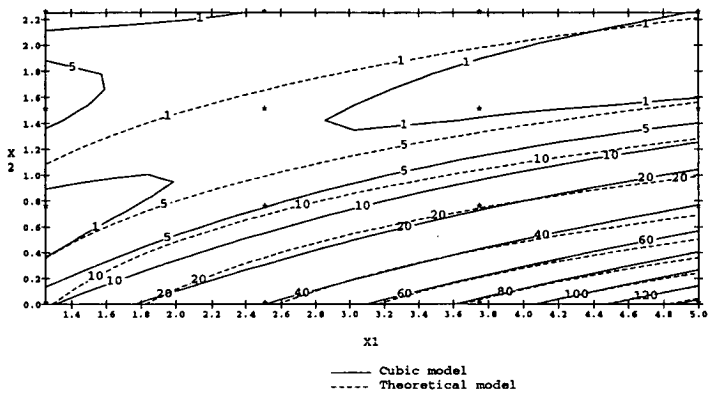
covariance model is a valid and potentially more accurate method than traditional polynomial models [69].

2.5 Summary

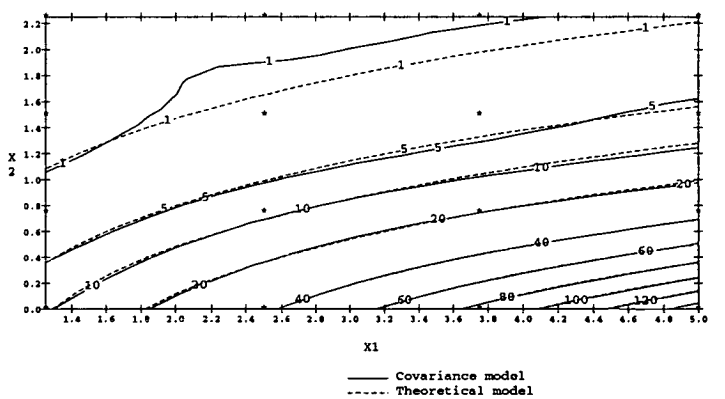
TCAD is an increasingly important tool for semiconductor design and development. When used correctly it has the potential to save significant time and money in identifying the most robust processes. When used in conjunction with DOE and RSM techniques the efficiency of TCAD analysis is further improved. Calphurnia and commercial TCAD frameworks which incorporate the elements of the original total TCAD framework make this integration possible and have ensured the success of TCAD within the industry. However, no attempt has been made to address the practical implications of any new processes or changes to those already in production. So just as TCAD provided the starting point for the original TCAD framework it also provides the starting point for the work presented within this thesis which reports on the integration of additional software tools to address the practical issues.



(a)



(b)



(c)

Figure 2.8: *Contour plots of responses (16 data points) for the actual response (equation 1) and, (a) quadratic model (R^2_{adj} = 0.880), (b) cubic model (R^2_{adj} = 0.985), (c) covariance model.*

Chapter 3
Manufacturing Analysis Tools

Chapter 2 introduced the original total TCAD framework and discussed the role of the tools incorporated within it. Despite its abilities it does not address the implications to the manufacturing environment that may result from a technological change to the process. It is these tools, whose integration into the framework are described in the following chapters, that are introduced and discussed here.

3.1 Introduction

In order to address manufacturing issues during process development, the original total TCAD framework has been expanded, as shown in figure 3.1. The incorporation of MES (Manufacturing Execution System), factory simulation and costings packages provides the additional elements required to assess the practical implications of any technological decision made using a combination of the TCAD, DOE and RSM elements. As before, TCAD remains at the heart of the framework, supplying the bulk of the data required for the factory and cost models with the additional data being drawn from the facility's MES or an alternative database of equipment details. When costing analysis of future processes is desired it is possible to extract much of the data which is normally held by the MES (when the process is in production) from the results of factory simulations. Additionally, as the MES database is the core information source for any fab it is a natural progression to add the storage of TCAD data files to its roles, thereby ensuring up-to-date TCAD data for analysis.

The following sections introduce IC production issues and the role factory simulation can play in optimising manufacturing efficiency. The use of an MES within a semiconductor facility is then discussed and finally costings are looked at with particular reference to COO (Cost Of Ownership) calculations.

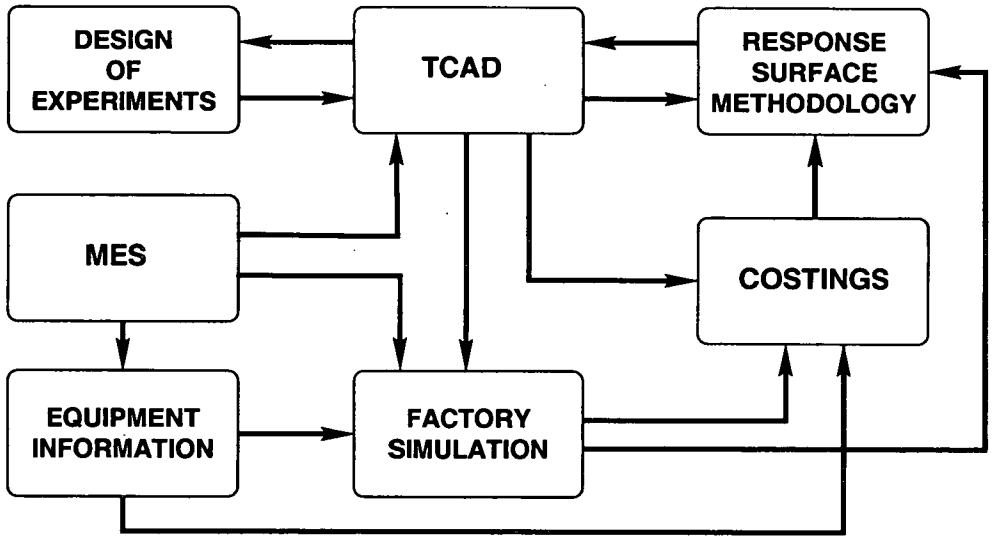


Figure 3.1: *Total TCAD component relationships, adapted from [73].*

3.1.1 IC Manufacturing Issues

Within a semiconductor production environment there are three key metrics used to gauge the performance of the fab: cycle time, throughput and WIP (Work In Progress) [74]. Cycle time, the time taken to process a wafer, has been shown to have a direct impact on both product cost and quality, hence its reduction is a target for the majority of semiconductor plants. However, the reduction of cycle time must be considered in conjunction with the throughput of the fab. That is the volume of production for a given time period and the inventory level (WIP) of the fab required to ensure efficient production. In a steady state system the relationship between these factors, as illustrated in figure 3.2 is given by Little's Law [75]:

$$WIP = throughput \times cycletime$$

However, IC manufacturing rarely exhibits a steady state on a day-to-day or even weekly basis. This can be a attributed to numerous factors including, equipment failure, poor scheduling or a lack of operators. Thus there is a more complex interaction between the WIP, cycle time and throughput than Little's Law suggests [77]. The following subsections provide a general background to some of the key production metrics in order to illustrate the issues that must be considered whilst attempting to maximise manufacturing efficiency.

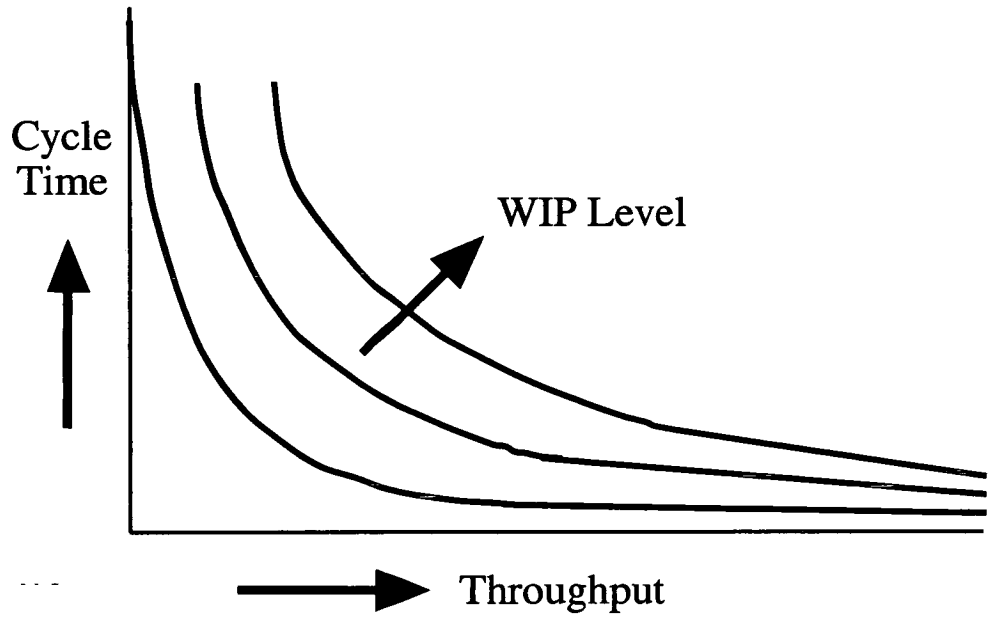


Figure 3.2: *Relationship between cycle time, throughput and WIP for various WIP levels [76].*

3.1.2 Cycle Time

Cycle time and its reduction is often seen as the key to improved manufacturing. This is not least because actual cycle times within the industry are often in the region of 6-8 weeks which is far in excess of those theoretically possible [78]. Shorter cycle times mean reduced delivery lead time and greater flexibility in meeting customer demands as well as improving the wafer yield as a result of lower exposure to contaminants within the cleanroom and a quicker response to variations detected at test [79]. Of these numerous advantages it has been shown that not only is the potential yield improvement as a result of the reduced time within the fab difficult to quantify [80] but that it is of lesser importance than the ability to improve the process through feedback from in line or end of line test results [81].

Assessment of the repercussions of cycle time reduction can not be accurately modelled by traditional static spreadsheets so other techniques must be used, such as the analytical queueing network models or through the use of factory simulation [82] [83].

3.1.3 Inventory, Queues and Bottlenecks

Inventory levels are an important issue within the semiconductor manufacturing industry. Although high inventory levels result in greater equipment utilisation, when this reaches around 80% the resultant cycle time has been shown to reach a level such that it has a negative impact on both the yield and throughput [84]. In addition, too high a level of inventory can also result in queues building up in front of equipment, hiding manufacturing problems [78]. This is further complicated by the desire for batch processing in much of the equipment to minimise set-up times and efficiently use equipment such as furnaces [85]. As well as using factory simulation for queueing analysis, dedicated software has also been developed [86] which requires less setup time than a full blown factory model.

On any production line there is normally at least one bottleneck, that is a piece or set of equipment that constrains the capacity of the line [87]. In order to maximise throughput it is essential that the bottleneck equipment is always fully utilised. In order to help achieve this alternative methodologies have been suggested and tools other than factory simulation [88] used to assess the potential impact [89]. Protective capacity within a production line is used to ensure a steady stream of work for the bottleneck equipment [90]. This technique relies upon the creation of a wafer inventory buffer that is used to absorb variations in the previous processing steps. Alternatively, the concept of a constant WIP level can also be used in an attempt to maintain throughput [91]. The WIP level of the production line is one of simplest methods by which to determine whether or not a facility is well balanced and operating within its capacity. Figure 3.3 illustrates how WIP varies over time for a range of wafer starts.

After an initial start up period, within a fab with no initial inventory, the WIP should stabilise and remain at constant level as a function of time for a given level of wafer starts. For a fab with no initial inventory this start up phase is indicated in area A in figure 3.3. A continually increasing WIP, as illustrated in plots B and C in figure 3.3, indicates that the line is being loaded in excess of the available capacity. Plot C in figure 3.3 shows the resultant WIP plot for a level of starts just beyond capacity. At the initial stages the WIP appears constant but as the time increases the WIP steadily rises. When the fab operates with a constant level of WIP, indicated by plots D-F in figure 3.3, the production line is balanced and is operating at or below capacity [93].

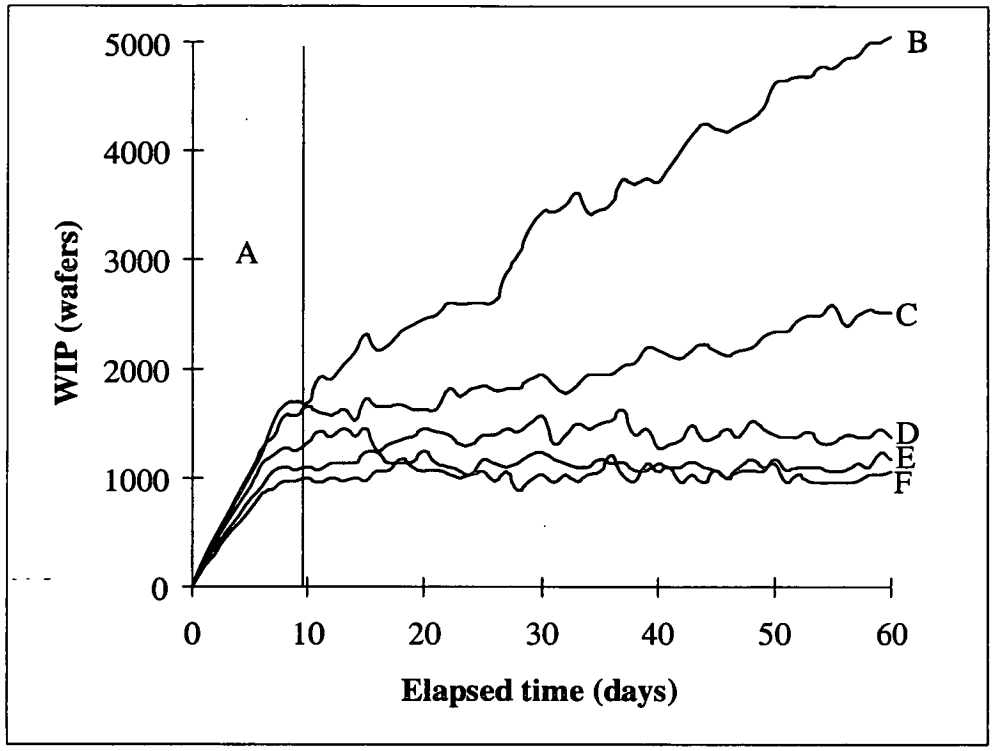


Figure 3.3: *WIP vs. elapsed time comparison for increasing number of wafer starts [92].*

3.2 Factory Simulation

The previous section has outlined some of the complexities involved with IC manufacturing. The relationships are such that they can not be easily interpreted through observation nor modelled well by a traditional static spreadsheet. Factory simulation software use dynamic stochastic models to give a more precise and realistic model of than was previously possible. Today's discrete event factory simulators are able to perform a number of stand alone tasks which include [94] [95]:

- identify production bottlenecks
- determine potential capacity
- provide equipment and personnel utilisation information
- cost production

These simulations also work in conjunction with other software to where the simulation using the fab model can be used to predict forthcoming events. Typically this centres around the generation of start schedules to ensure high resource utilisation with a minimum of late orders and reduced labour variability [96]. This is achieved by down-loading the current WIP and using the factory simulator to generate reports to predict line conditions at regular intervals allowing preventative action to take place if required [97]. Previously this type of analysis would have been performed using models written in dedicated simulation languages such as SIMAN [98] which required significantly more effort than building a model using in a modern simulation package. Other methods using a smaller data set than that required by a factory simulator can also be used which, although potentially faster, can only perform limited calculations [99].

Although there are a number of factory simulators are available those shown in table 3.1 are among the most popular and a comparison of them can be found in [100].

Company	Factory Simulator
Tyecin (Manugistics)	ManSim/X
Autosimulations	AutoSched
Systems Modelling Corp.	Wafer Fabrication Template
Wright, Williams and Kelly	Factory Explorer

Table 3.1: *Commercial Factory Simulation Tools [100].*

3.2.0.1 ManSim/X

Manugistics' ManSim/X [95] is a factory simulation package that has been specifically designed to meet the needs of the semiconductor industry. It models the whole production line as a system of queueing networks which change state at distinct points in time, allowing them to be modelled by discrete event simulation [101] [102]. This builds up into a very large detailed model comprising of not only the individual elements but also the process flows and options that they bring, such as rework routes. This level of detail is required to perform the wide ranging analysis that the simulators are capable of but is clearly not ideal because such models are costly and time consuming to build [103]. For this reason it is essential that an integrated package such as ManSim/X is used, enabling easy development of factory

models and access to the results in a simple to use format, thus catering for a wide user base. Figure 3.4 shows a screen-shot of the main ManSim/X run window. The WIP vs time plot that appears in this window allows the user to quickly assess line balance as described previously. Additional run windows allow the user to monitor equipment utilisation and the build up of queues as they occur during the simulation helping locate bottlenecks. Once the simulation is complete a reporting menu gives access to a range of all the production metrics in a series of set reports as well as allowing the generation of custom reports.

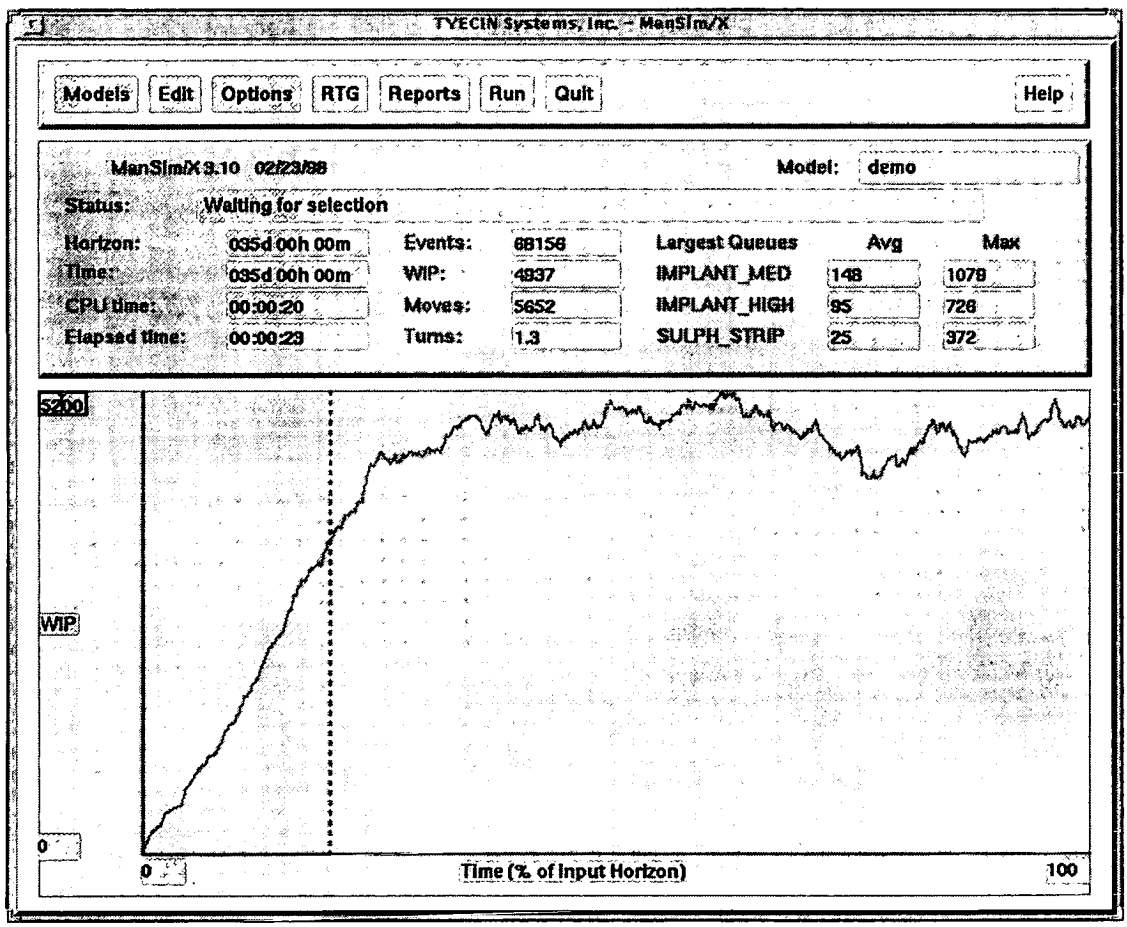


Figure 3.4: *Manugistics' ManSim/X factory simulator screen shot.*

3.2.1 Factory Simulation Summary

Factory simulation enables the potential efficiency of a facility to be easily assessed by investigating alternative operating conditions and, perhaps more importantly, provides a

clearer picture of what is actually occurring within the fab. The identification of bottlenecks and critical pieces of equipment is especially important when the product mix or level of starts within the fab changes, as is often the case with the introduction of a new or revised process. Removing bottlenecks through the addition of new equipment or altering other areas of production such as the product mix, start levels or the allocation of personnel enables the production line to be balanced. A balanced line with highly utilised equipment is a major element in helping maximise the production capabilities of the fab. Thus, identification of measures to balance the line before the introduction of a new process has the potential to increase productivity.

3.3 The Cost of Production

The importance of knowing the true cost of IC production should not be underestimated. Without this knowledge it is impossible to determine the level of profit for each IC, complicating decisions about the future of individual products. For example, should the start rate of one product be reduced to allow an increase in the start rate of another or is it more cost effective to shrink the die size to increase the volume produced? In order to fully answer this and other issues that continually arise in manufacturing environments it is essential that production costs can be clearly identified to ensure that profits can be maximised.

In order to evaluate the cost of wafer processing a number of factors must be considered. These include direct costs e.g. labour, materials and maintenance, capital investments in equipment, buildings, land etc. and indirect costs such as engineering support, engineering lots and indirect labour (e.g. administration and security staff) [87]. At a high level this is simple and is the sum of all the production costs divided by the number of wafers, die or ICs produced. This may be fine for the annual accounts but is of little use in determining how individual areas of production affect the cost of the IC or the cost of a particular product from within a mix. In order to break down the actual production costs requires a significant amount of detail. One method of doing this is through cost of ownership analysis.

3.3.1 Cost of Ownership

Cost of Ownership (COO) provides a measure of the real cost of performing a processing step for each equipment type within a facility. Perhaps its most significant feature is the inclusion of the fixed cost and depreciation of the equipment being used. This is important as it attributes the actual cost of the equipment within the cost of the ICs produced, something that can not be done when only the operating and material costs are considered.

COO has been defined by SEMI as the full cost of embedding, operating, and decommissioning, in a factory and laboratory environment, a system needed to accommodate a required volume [104]. It can also be defined by:

$$COO = \frac{CF+CR+CY}{L \times TPT \times Y \times U} \qquad (1)$$

Where:

- COO = Cost per good unit
- CF = Fixed Cost
- CR = Recurring Cost
- CY = Cost of Yield Loss
- L = Equipment Life
- TPT = Throughput Rate
- Y = Yield
- U = Utilisation

Thus, COO is the cost per correctly processed wafer passing through each given piece of equipment within the process flow. This is achieved by ensuring that the total costs are divided by the throughput and yield that together determine how many wafers are correctly processed. It also includes the life span of the equipment and its utilisation which ensure that the cost of the equipment is also attributed to the processed wafers. This basic COO model is available in more detailed formats, such as the Sematech COO model which is in the form

of a spreadsheet. The Sematech COO spreadsheet uses three pages of input data, partially loaded with industry standard defaults, to enable the calculation to take place. In addition to calculating the cost per good wafer out it also provides a range of results, such as annual costs breakdowns for each cost category. The Sematech COO model is further discussed in Chapter 5 where its use with CASTT is described.

3.4 MES - Manufacturing Execution System

Due to the complexity of semiconductor manufacturing modern fabs use an MES (Manufacturing Execution System) as an aid to improve manufacturing efficiency. In essence an MES aids the day-to-day running of the fab by monitoring the progress of wafers through the line, identifying equipment status and providing a means by which the information collected can be accessed. This section provides a brief history of the MES, discusses its role within IC manufacturing and takes a closer look at PROMIS [105], the MES used in MASTT to ensure that up-to-date simulation data is easily made available.

3.4.1 MES Background

CAM (Computer Aided Manufacturing) systems, the forbearer of the MES, began life in the early 1980s. They were developed in order to meet the rising needs of the industry to track the progress of wafers with an ever increasing number of processing steps. In order to improve manufacturing efficiency computer systems were developed to assist manual methods of production management which could no longer respond quickly enough to changes in the manufacturing environment [106].

The availability of sufficient computing power in the 1980s enabled the CAM system to become a reality. As with many software products in the IC industry there was the dilemma of whether to develop an in-house system or a use a commercial package. Despite the potential to model all of the fab and address the needs of its staff the major investment required to develop an in-house system made it a poor choice given the already available commercial packages in the the late '80s [107]. The preferred option was to use one of the available

commercial packages, see table 3.2, which despite only modelling 80% of the fab provided a low cost, well supported alternative [107].

Company	CAM Package
Cameo System	CAMEO
Consillium	COMETS
Promis Systems	PROMIS
Qronos Technology	Advantage

Table 3.2: *Commercial CAM systems circa 1987 [107].*

The fundamental roles of a semiconductor MES are lot tracking and equipment recipe managements [108]. The original CAM systems were developed around the core idea of lot tracking and data collection [109]. Direct control of equipment and automated recipe download based on the information contained within the CAM system were features that were incorporated during the mid 1980s. This was made possible by the development of equipment specific software but more importantly through SECS, the SEMI Equipment Communications Standard, which allows equipment to be incorporated into the CAM system [110]. In addition to these roles, there were a number of elements integrated within a CAM system at the end of the 1980s as illustrated in figure 3.5.

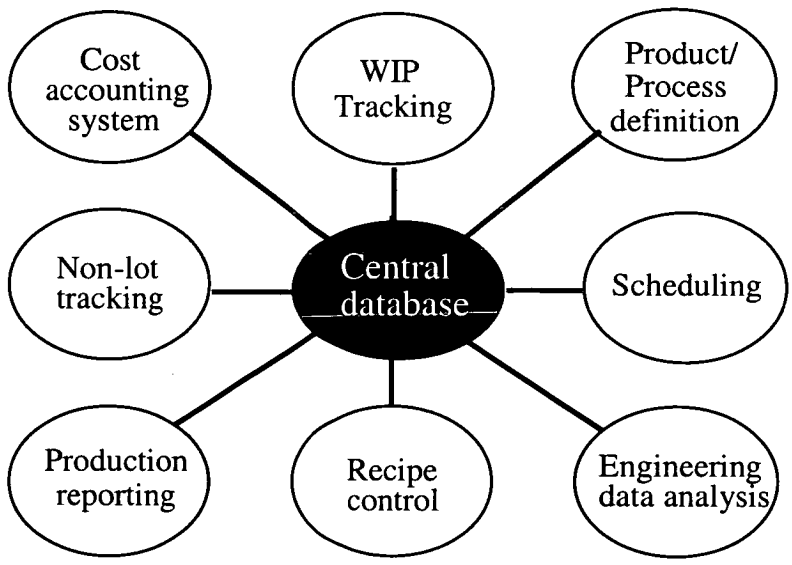


Figure 3.5: *Core elements of a CAM systems circa 1989 [111].*

Today's MESs, see table 3.3, have developed from original CAM systems to include higher level features and play an important role in linking the shop floor to business management systems such as ERP (Enterprise Resource Planning) [112]. This link is crucial in ensuring effective management and can be used to aid optimisation of a manufacturer's assets. Today's MES software can now be considered to have at least 11 functionalities, as defined by MESA (International Association of MES Vendors) [113]:

- resources allocation and status
- operations and detail scheduling
- dispatching of production units
- document control
- data collection and acquisition
- labour management
- quality management
- process management
- maintenance management
- product tracking and genealogy
- performance analysis and reporting

An MES stores production details for individual wafers, lots, processes and products together with most of the equipment information. This information is stored within a central database and can be accessed throughout the fab, ensuring that all users are using the same information. A variety of user interfaces are available to access or enter this data from simple text based terminals and bar code readers to graphical interfaces such as Motif and Windows, ensuring ease of access to the stored data.

Company	MES Package
Consillium	Workstream DFS
FASTech Integration	CELLworks
FASTech Integration	FACTORYworks
FASTech Integration	PCworks
Promis Systems	PROMIS
Promis Systems	PROMIS Encore!

Table 3.3: *Commercial MES circa 1996 [114].*

3.4.2 PROMIS

As shown in tables 3.2 and 3.3 Promis Systems have been involved within the CAM/MES software market for a number of years. Together with Consillium they are market leaders in the field and have produced systems with have met the criteria described above and in figure 3.5 since the beginning of the 1980s [115]. Today the focus lies with ensuring compatibility with Sematech's CIM Applications Framework which has been developed to promote the integration and use of MES and stand alone analysis tools [116] [117]. By introducing an MES into the total TCAD framework through MASTT it may be possible to further combine the existing TCAD and process development tools with other elements incorporated within the Sematech CIM framework in the future.

3.4.3 Promis Structure

A core feature of the Promis MES is the hierarchical structure, illustrated in figure 3.6, used to define the processing instructions - PRODs (Part, Procedure, Recipe, Operation and Document) [105]. Promis issues instructions either to operators or directly to equipment based on the information recorded within the PRODs by the process engineer. Additionally the PRODS are used to record the entire history of each lot including any measurement data or test results.

To summarise, a *part* is the object being produced and the instructions required to produce each part are given in a *primary procedure*, which is designated the same name as the *part*. The *primary procedure* consists of a series of *called procedures*, which are built up of a

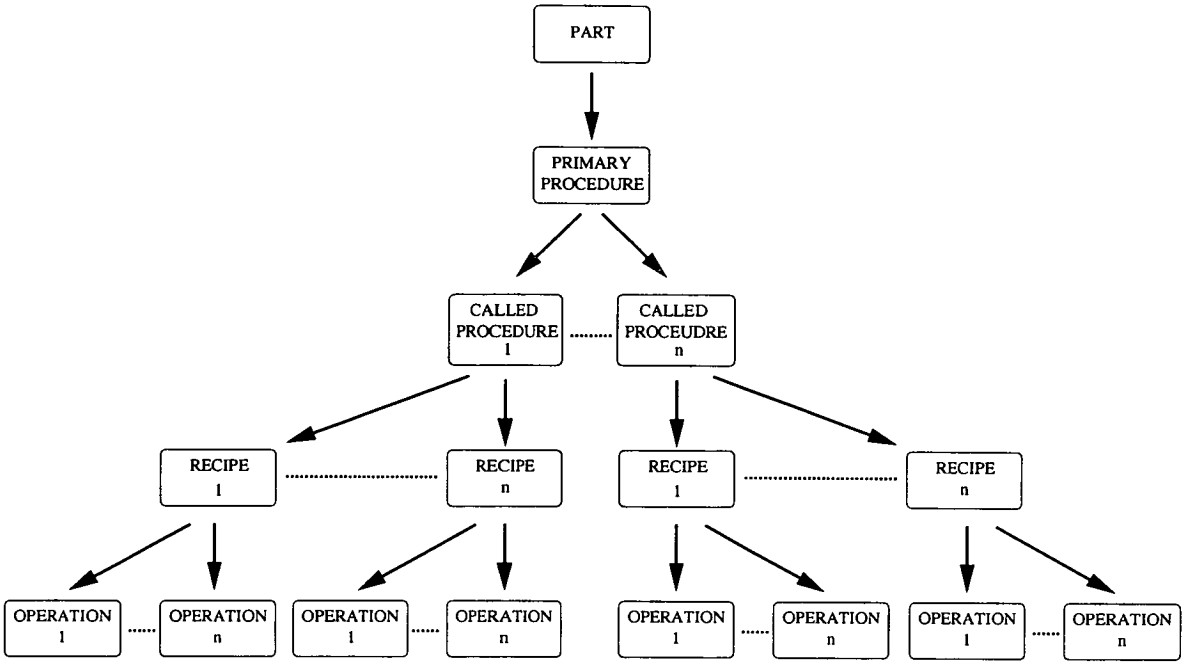


Figure 3.6: *Promis PRODs Hierarchical Structure.*

collection of *recipes*, which in turn are defined as a set of *operations*.

At any level of the PROD hierarchy a DOCU file (ASCII text) can be attached to provide further details about the process at that stage. Typically, these are either used to supply detailed operator instructions or on-line information for engineers. Finally, if desired, a *stage* can be defined within Promis. This is used to group a set of recipes or procedures into manageable sections, making reporting and analysis of line performance easier.

3.4.4 Promis Parameters and Scripts

Another important feature of Promis is how, within the PROD structure, parameters can be passed between the levels of hierarchy. Parameters may be used to transfer variables (e.g mask details, implant dose and energy, oxidation time) between PRODs. They follow a similar hierarchy to the PRODs themselves whereby any parameter defined at a higher level within the PROD hierarchy will overwrite any previous settings at a lower level. It should be noted that the DOCU files are not included within the parameter structure and hence any

parameter change will leave them unaffected.

Finally one of the most powerful facilities within Promis is the ability to create and run macros called scripts [118]. These can either be written directly or automatically created by recording key strokes. Scripts are essential for day-to-day use of Promis simplifying the generation of custom reports in addition to the standard reports within Promis [119]. Additionally Promis scripts can be run in a background mode from the VMS operating system without user interaction. It is this last feature that makes Promis ideal for inclusion within the new framework as it enables a hands-off approach to data retrieval from the MES database.

3.5 Summary

The three additional elements that have been incorporated within the total TCAD framework because of the work reported in the following chapters bring an extra dimension to the analysis previously possible. Factory simulation can be used to examine numerous production issues and along with COO calculations important financial and strategic issues can be forecast at a much earlier stage in process development. The MES is the key IC manufacturing system and its inclusion as the core data source within the framework utilises not only the information it contains but also its well defined procedural structure.

Chapter 4
Incorporating Factory Simulation into Total TCAD

The role factory simulation can play in examining manufacturing and production issues was discussed in the previous chapter. However, for it to form a part of an overall DFM strategy it must become integrated within the existing total TCAD framework. This chapter describes the design, development and implementation of a software tool called FASTT (FActory Simulation in Total TCAD). FASTT integrates commercial TCAD and factory simulation packages, for the first time incorporating a factory simulator into the total TCAD framework. FASTT facilitates the creation of factory simulation models from a TCAD data file, enabling the impact on manufacturing operations to be more readily considered at an earlier stage during the design and development process than is currently common place.

4.1 Introduction

The introduction of a new or improved process has the potential to significantly impact manufacturing issues such as cycle time, WIP, throughput and capacity. As such, it is prudent to consider the possible effect on factory performance as close to the start of any new process development as possible. Typically, the feasibility of introducing a new process into production is often only considered once significant effort has gone into the design and development of a process. This is partly because TCAD engineers are often far removed from those concerned with factory operation and that the generation of data required for factory simulation software is time consuming and tedious. This being the case there is an obvious reluctance for engineers involved in development to invest any significant effort into using factory simulation to examine the potential effect on the manufacturing environment.

The development of FASTT, which is described in this chapter, makes it possible to identify

potential problems earlier in the design cycle, enabling them to be taken into consideration during development. This was achieved by ensuring that the software enabled the automatic generation of factory simulation models largely from information already available within TCAD data files. As a result of this work, the gap between development and production has been bridged, making earlier consideration of manufacturing issues during process development viable.

4.2 Commercial Software Packages

A key feature of the total TCAD approach to DFM is the use, where possible, of existing commercially available software. This utilises the features available within fully supported packages and ensures an existing user base. As such, this was also an aim when considering the integration of factory simulation into the framework. Taurus Work Bench (TWB), Avant!'s virtual wafer fab and Manugistics' factory simulation package, ManSim/X, are among the leaders in their respective disciplines and provide the core elements which have been integrated. This section provides an overview of these packages with the emphasis on their integration through FASTT.

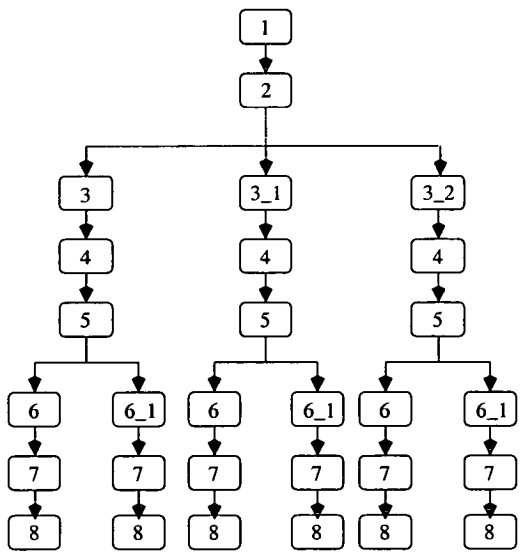
4.2.1 Processing Data Storage in TWB

TWB uses a single ASCII data file, the .vfl file, to store all the information required to define an experiment. This is the sole source of TCAD information for each experiment and provides the initial point from which experimental data can be extracted. The .vfl file records the last saved version of the experiment and contains the following information:

- the data stored in the TWB experiment annotation box.
- each of the available drivers/simulators, the code required to initiate them and the machines on which they can be run.
- each external tool, the code required to initiate them and the machines on which they can be run.

- each of the process modules available.
- additional information, e.g. DOE options and settings for the wafer flow.
- a list defining the wafer flow through the process modules.
- a list of the completed simulations of the wafer flows.

The key to exporting the processing details from the .vfl file was the identification of the section of the file that defines the wafer flows. The format of the list is shown in figure 4.1 together with a representation of the wafer flow it defines. The .vfl file contains the most recently saved wafer flow storing all the combination of process flows created within the TWB experiment. When this information is combined with the data from the individual process modules the two major components required to ensure that all the processing options can be extracted from the .vfl file are available.



TWB .vfl file wafer flow code

```
<module> ( ) 1:0 (2:0);
<module> ( ) 2:0 (3:0);
<module> ( ) 3:0 (4:0);
                ( ) 3_1:0 (4:0);
                ( ) 3_2:0 (4:0);
<module> ( ) 4:0 (5:0);
<module> ( ) 5:0 (6:0, 6_1:0);
<module> ( ) 6:0 (7:0);
                ( ) 6_1:0 (7:0);
<module> ( ) 7:0 (8:0);
<module> ( ) 8:0 ();
```

Figure 4.1: *Wafer flow representation and .vfl file code format.*

4.2.2 Model Creation in ManSim/X

Within ManSim/X the conventional method for creating a new factory model is through its GUI interface. This is a time consuming, laborious and error prone procedure that does not

lend itself well to the automated creation of factory models. It is however invaluable for assessing the success of any trial transfer, allowing the user to see what information has been imported, enabling the model to be refined and simulations performed.

ManSim/X uses a number of directories, containing ASCII files for each individual model, to store both factory models and the simulation outputs. Directly writing each of the 49 model files needed to create a new model was considered but rejected. Unfortunately, a number of fields are present in more than one model file and the ordering of the information is both complex and critical to the model's functionality. As the format of the files lies outwith the scope of this work and is subject to change with subsequent versions of the software it was felt that this approach was inappropriate.

Fortunately, ManSim/X also incorporates a utility, Model Builder, which allows the creation of a basic factory model from CSV (Comma Separated Variable) files. The templates for these files are supplied for use with spreadsheet software and are designed to provide a familiar interface for the user. Once the CSV files have been written, ManSim/X's Model Builder GUI (shown in figure 4.2) can be used to form the factory model within ManSim/X. Model Builder is simple to use, requiring the user only to name the model to be created and ensure that the CSV files are present in the correct directory. The ease of use and the forward compatibility of this approach made it the most appropriate method for use with FASTT.

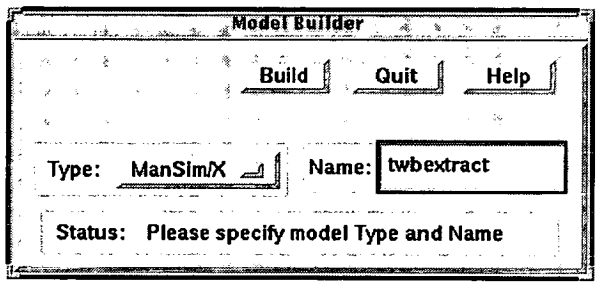


Figure 4.2: *Manugistics' ManSim/X's Model Builder utility GUI.*

4.3 FASTT - Factory Simulation in Total TCAD

This section outlines the procedure used to automate the creation of a factory simulation model within ManSim/X utilising the information available in the TWB .vfl file. During this stage of the development of FASTT it was necessary to identify:

- the information required by Model Builder
- the role of TWB in suppling this information
- sources for additional information
- the level of automation achievable

The following subsections discuss how these issues were solved, highlighting the design choices made and the features incorporated within FASTT to ensure its ease of use.

4.3.1 Relevant Data

The information required by Model Builder was of prime importance during identification of which data was available from the TWB .vfl file and which had to be obtained from elsewhere. Examples of the data fields required by Model Builder are shown in table 4.1, the full specification details are available in in appendix H of the ManSim/X User's Manual [95].

From table 4.1 it is clear that there is a mismatch between the data required by Model Builder and that available from the .vfl file. The PRODUCTS.CSV and STARTS.CSV files only require a few pieces of data that are not necessarily available within a .vfl file. This data can be made readily available through the use of TWB's annotation box shown in figure 4.3. This area of the experiment window allows details about the experiment to be recorded and provides the ideal location for such information. The product ID, process ID, lot size and level of weekly wafer starts are recorded here and the default values are used for the additional fields needed in the PRODUCTS.CSV and STARTS.CSV files.

The WIP.CSV file can be used to import lot specific details from a fab's MES to allow factory simulations to be performed using an existing set of start conditions. However, for most of

CSV file	Example Data Fields
PRODUCTS.CSV	Product, start rate, priority, lot size, process ID, product type.
STARTS.CSV	Product, week, no. of starts.
WIP.CSV	Lot, no. of wafers, operation, lot priority.
EQUIP.CSV	Area, work station, PM interval, PM duration, usage, equipment, MTTR, MTBF, capacity, setup time, maximum load time, load interval.
PFLOW.CSV	Process, work station, operation, yield, specifications, step description, step equip, time, capacity.

Table 4.1: *Data fields required by ManSim/X's Model Builder utility*

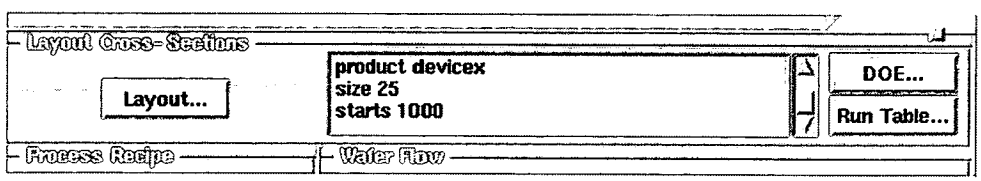


Figure 4.3: *TWB annotation box data format.*

the applications for which FASTT will be used a zero initial inventory will be assumed and analysis will begin after an initial ramp up time. Assuming no initial inventory is present for any model created removes the need to supply data for WIP.CSV. However, during day to day forecasting use it is common practice to download WIP data from a fab's MES [120] into the factory simulator, so if required a model using the current WIP status could be written to the WIP.CSV file.

The data required for the EQUIP.CSV file is not process specific, rather it is dependent upon the given production line and can therefore be omitted from consideration during the development of FASTT. As long as details like the MTTR and MTBF of the equipment remain constant the EQUIP.CSV file should not need to be altered once it has been generated for each facility. The file is effectively a database of the equipment set it that need only be modified when a piece of equipment is added or removed.

The PFLOW.CSV file is the basis of any factory model created using Model Builder and it is also the one which requires the greatest amount of additional information to that available within TWB. To achieve this it was decided to add the details to each of the individual process modules within TWB in the form of a comment, where each comment, as illustrated in figure 4.4 has the same structure:

comment FS *field data*

Where 'comment' is required to distinguish the line of code from those read by the TCAD simulator, 'FS' (case insensitive) is the string used by FASTT to identify appropriate comments '*field data*' combination within the code. Although in the initial stages this additional data had to be manually added to TWB it is automatically incorporated in this format when MASTT is used to build an up-to-date TWB TCAD data file as outlined in chapter 6.

The above discussion of data requirements assumes that Model Builder is to be used to create a model containing details of only those process flows within TWB. Clearly, there are many situations where this will not be the case and it would be desirable to consider processes from TWB with those already present in the facility. In such situations the appropriate

```
Comment FS  operation    1234
Comment FS  description ISO_IMP
Comment FS  time  60
Comment FS  wstat IMPLANT_HIGH
Comment FS  equipment    IMP_01
Comment FS  equipment    IMP_02
Comment FS  equipment    IMP_03
implant boron  dose=5e15 energy=90 rp.eff
```

Figure 4.4: *TCAD code for an implantation process step including factory simulation comments.*

files must be augmented with the additional information from the existing PFLOW.CSV, PRODUCTS.CSV and STARTS.CSV files. Unfortunately, the current version of ManSim/X does not allow the export of a factory model in any format. So if these files are not already available the data must be manually extracted from a set of the existing ManSim/X model files. This procedure is much simpler than writing directly to the model files since the order of the data is unrestricted and need only be performed once and only updated when a new process or product is added.

4.3.2 Extracting Factory Simulation Data from TWB

Once the Model Builder data requirements and the appropriate sources were identified a method of extracting the data from the TWB .vfl file had to be developed. To ensure FASTT could be easily adapted for use with other vendor's simulators an intermediate step was used rather than writing the extracted data directly to Model Builder format. This also allows the extraction code to be utilised by other applications such as CASTT which is described in the following chapter. This element of FASTT, written in C, extracts a full factorial of process modules available within TWB. This disregards any reduced experiment created using DOE techniques, the reasons for which are three fold:

- the time taken to perform factory simulation is a fraction of that required for TCAD simulations
- the proprietary definition of the experimental design types within TWB is undocumented and outwith the control of this work

- and most importantly it can not be assumed that methods such as DOE and response surface analysis, as described in chapter 2, can be directly applied to factory simulation results

For each processing split an intermediate single column text file is created, containing both the TWB annotation information and the processing details. Figure 4.5 shows the information extracted from the data file shown in figure 4.4 in this single column format.

```
operation
1234
description
ISO_IMP
time
60
wstat
IMPLANT_HIGH
equipment
IMP_01
equipment
IMP_02
equipment
IMP_03
```

Figure 4.5: *Single column factory simulation data extracted from the TCAD code for the implantation process step given in Figure 4.4.*

The data for the intermediate files was obtained by firstly extracting the information contained within the TWB annotation box: the product ID, the process ID, the number of wafers in a lot and the wafer start rate. Then the processing details from the TCAD code and finally the additional factory simulation comments that were added to each module. This was done for each of the full factorial of process flows as defined by the wafer flow section of code in the .vfl file, as described in section 4.2.1.

The first version of FASTT used the method illustrated in figure 4.6 (a) to traverse the wafer flow. Initially data is extracted from the modules to all of the output files at the same time, continuing until a branch is encountered. This method uses these branch points to initiate the extraction and allocate the information to the correct subset of the output files. At each branch the left most path is taken until the final extraction has been performed. The next path to the right is then taken until all of these paths from this branch point have been traversed.

On occasions where there is more than one level of branches, such as shown in figure 4.6 the same rules are applied and hence there is the potential to duplicate a large number of extractions from the same modules to each output file.

This issue was addressed and the extraction routine altered. The current method of traversing the flow is shown in figure 4.6 (b). It uses a similar approach whilst reducing the number of extractions required. When the first branch is encountered the number of branches at this point and the total number of splits are used to identify which of the output files the extracted details from each of the module choices are written to. Until the next branch is reached the data from the subsequent modules is written to all of the output files, as was the case before the first branch was reached. If another branch is encountered the procedure is repeated, treating each first level branch as if it were an individual tree.

A more efficient method of parsing the tree may be to consider that all modules output to all files with the exception of the modules at the branches as shown in figure 4.7. However, this would require a significant rewrite of the extraction software, due to its current use of nested loops. The potential benefit in terms of speed which may be gained by this extraction method is negated by the time taken to perform either the TCAD or factory simulations. This being the case it was felt that there was little to be gained by further developing the software in this manner.

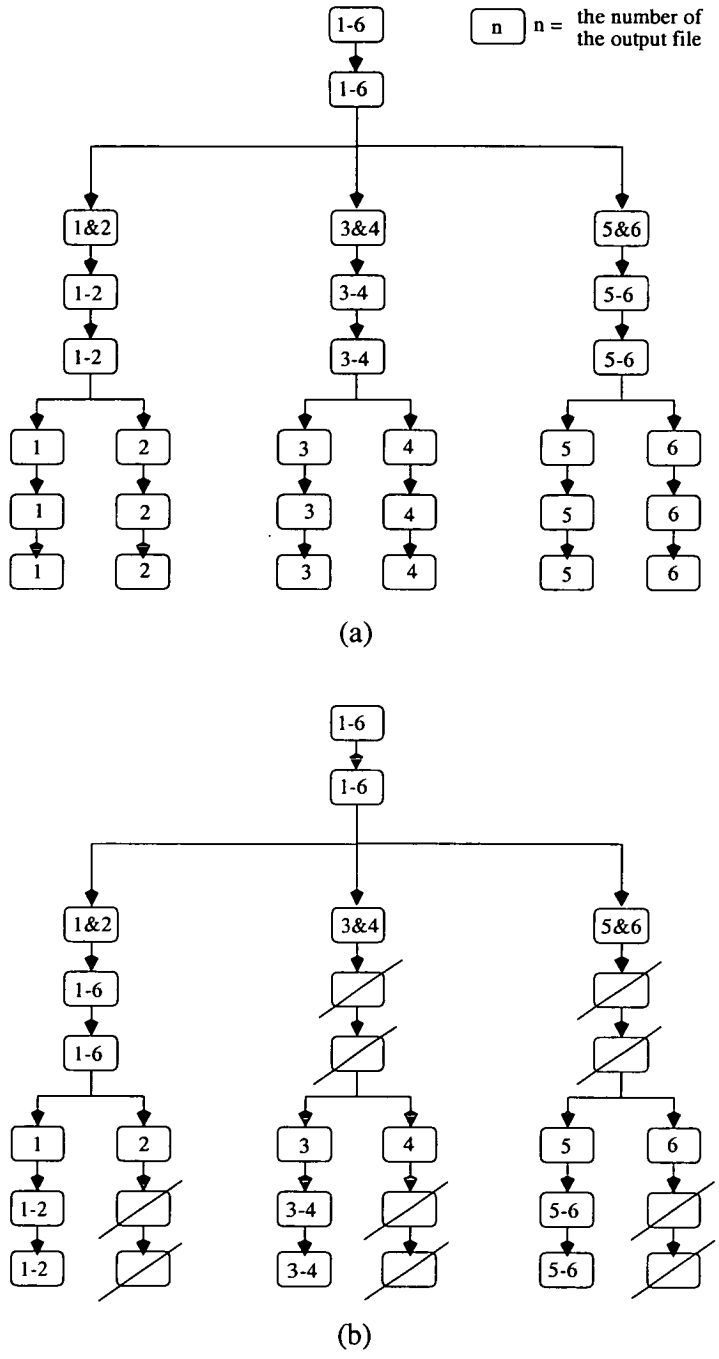


Figure 4.6: *Wafer flow extraction methods (a) original (b) current.*

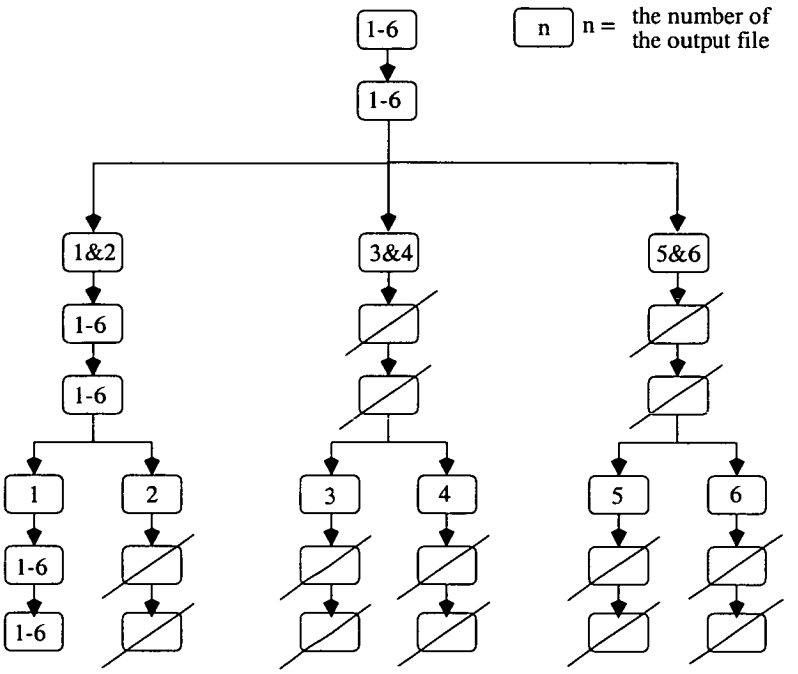


Figure 4.7: *Proposed wafer flow extraction method.*

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4.3.3 Constructing the ManSim/X Factory Model

Model Builder requires all five CSV files before a model can be successfully imported into ManSim/X. As discussed in section 4.3.1 and illustrated in figure 4.8 the EQUIP.CSV file is always available and the WIP.CSV file need not contain any data. The remaining three are constructed using information from the intermediate files. For each intermediate file the data list is searched through writing the appropriate data to the STARTS.CSV and PRODUCTS.CSV files, the remainder of the list is then parsed building up the data for the PFLOW.CSV file, the format of which is shown in figure 4.9 for the same data previously presented in figures 4.5 and 4.4. This is repeated for each process option until all of the flows have been written to the CSV file where each is denoted as an individual product using an individual process.

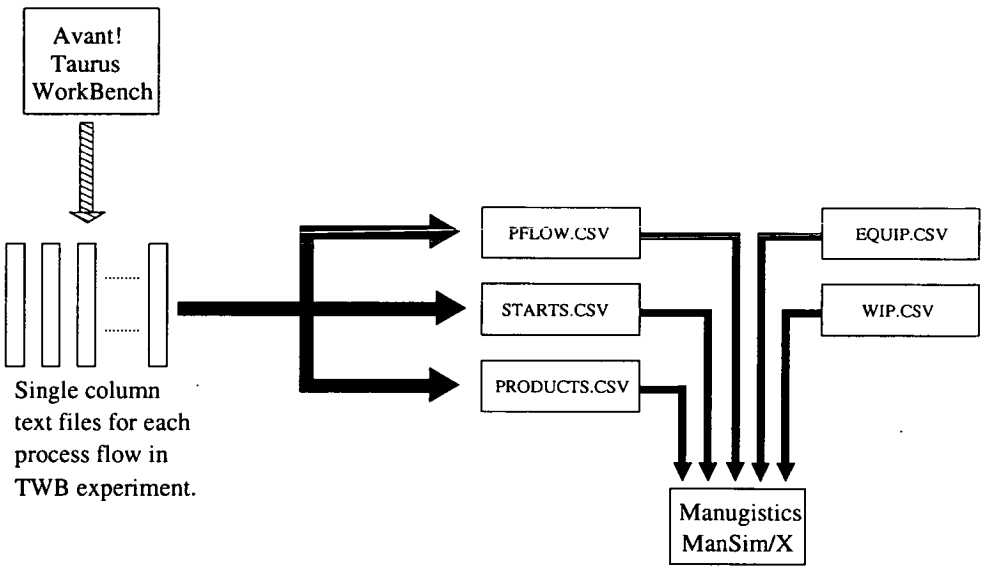

Figure 4.8: *Data transfer flow from Taraus WorkBench to ManSim/X.*

```
Process-1,IMPLANT_HIGH,60,,,1234,ISO_IMP,IMPLANT_HIGH,IMP_01,,,,
Process-1,,60,,,1234,ISO_IMP,IMPLANT_HIGH,IMP_02,,,,
Process-1,,60,,,1234,ISO_IMP,IMPLANT_HIGH,IMP_03,,,,
```

Figure 4.9: *The ManSim/X's PFLOW.CSV format, required for the process flow file for an implantation process step.*

4.4 Using FASTT and Factory Simulation

The previous sections of this chapter have outlined how FASTT can be used to automate factory model generation from a TCAD data file. However, although this has significantly reduced the time and skill level required to create a factory model it does not fully provide the functionality and ease of use that process developers require. This is because TCAD users are seldom also experienced factory simulation users. As such, it was felt that it was important to incorporate into FASTT a method by which factory simulations could be performed without the need for extensive additional training. So, in addition to creating the factory models FASTT has been designed to enable the automated running of the simulations. This feature provides basic factory simulation results with a minimal user input as well as providing a starting point from which experienced factory simulation users can perform more detailed analysis.

As described in section 4.3.2 FASTT extracts the full factorial set of process options, creating a single process with a single device for each within the factory model in ManSim/X and each of these alternatives must be simulated. To accomplish this an interactive UNIX shell script (Korn) was written to automate the running of the simulations. This is discussed in the following subsections, as is the collation of simulation results into a number of formats for further analysis using the statistical software incorporated within the total TCAD framework.

4.4.1 Running Automated Factory Simulations

Once a factory model has been imported into ManSim/X there are essentially three pieces of information required before a factory simulation can be performed: the length of the simulation in days, the percentage of simulation length that is deemed startup and is therefore omitted from the results and finally the start rates of the products/processes within the model. This is the case whether the simulations are to be performed using either the ManSim/X GUI or through the use of a background batch command. This latter method enables the simulations to be performed automatically. However, before the simulations can be performed the start rates must be considered.

Simulation of any given process through the fab at a start rate significantly below that of capacity is unlikely to highlight manufacturing issues. Additionally, the approximate capacity of a line is unknown until several simulations have been performed identifying the point at which the WIP begins to continually rise, as discussed in chapter 2. To remove the need to pre-determine start levels FASTT uses an initial wafer start level and a start rate increment to initiate the simulations. The default initial rate is that defined in the TWB annotation box, however, the program prompts the user to alter this as required, ensuring that the whole extraction process need not be repeated. Using the concept of a stable WIP, to ensure that that capacity has not been exceeded, simulations are performed at increasing start levels until the WIP gradient exceeds the value set in the initial settings as shown in figure 4.10. By using this approach all of the alternative process flows can be simulated from the initial level to beyond capacity, providing a range of results for further analysis.

```
Default settings are as follows to change enter the setting number.

      1. Mansim/X model name.....................twbextract
      2. Product start rate increment.............25
      3. Simulation length in days................60
      4. Simulation - percentage warmup time.......20
      5. Number of experiment wafers..............6
      6. Max allowable mean WIP increase/Day.......5
      7. Combine with existing fab model..........0

      0. Quit, use present values.

Enter option to change defaults, or 0 (zero) to finish editing:
```

Figure 4.10: *FASTT factory simulation control initial settings.*

The initial settings of FASTT's simulation controls shown in figure 4.10, allow the extracted model to be combined with an existing factory model. This requires model details of the existing factory that match the Model Builder PFLOW.CSV, STARTS.CSV and PRODUCTS.CSV files but without the header information. The extracted model is then combined with the additional data to give a model of the whole fab. As with the EQUIP.CSV file discussed in section 4.3.1 these files only require minimal alteration in line with products

or processes changes within the fab change.

The FASTT factory simulation control flow diagram in figure 4.11 shows how the WIP gradient is used to control the running of the simulations. Once a simulation is complete the WIP vs. time data is extracted for the period of the simulation after any initial warm up that is specified and a linear line fitted. The gradient of this line is used to decide if the starts should be incremented for that process option, based on the value set in the control settings. This has the advantage that the once the start level for the current process option has exceeded a realistic level the simulations continue with the next until each has been completed. This means that there is no need to pre-determine the maximum level of starts, allowing all of the simulations to be run without the need for manual intervention since the results of the simulations are also automatically extracted.

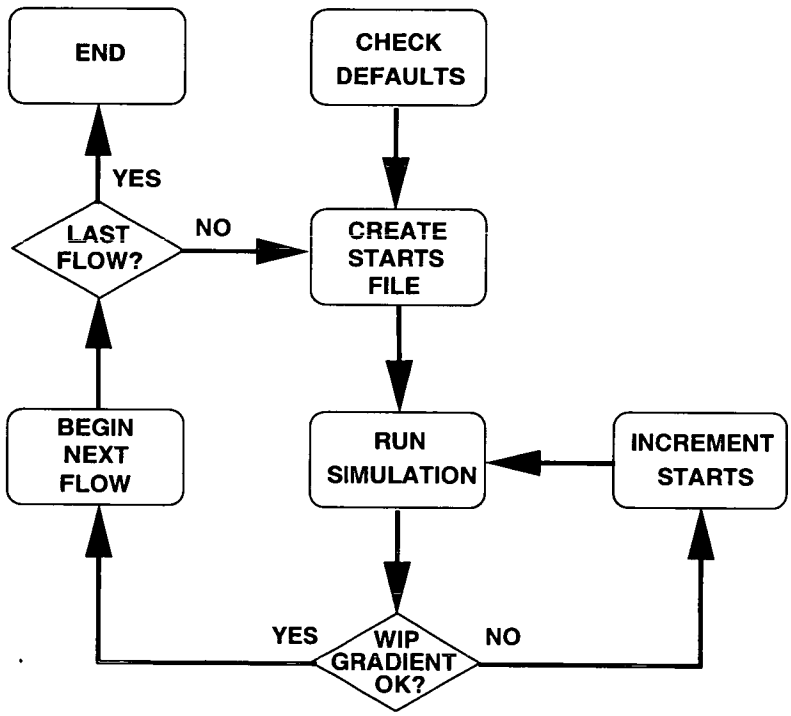

Figure 4.11: *FASTT factory simulation control operation flow diagram.*

4.4.2 Extracting Simulation Results

ManSim/X generates a large data set on the completion of a simulation. These results can be viewed within ManSim/X or directly from the report files. As with the input files these reports are stored as individual files within a set of directories denoted by the model name. These files are overwritten each time the model is simulated, keeping only the latest results. Therefore, it is necessary to store the results for future analysis because FASTT uses the same model each time.

However, in most circumstances only a small subset of the data is either relevant or desired. This means that a general set of results can be extracted by examining the more important result files. Thereby significantly reducing the volume of information that must be kept, although at the expense of potentially losing data that may be useful in further analysis.

FASTT automatically extracts and stores data for four key manufacturing metrics at the end of each simulation run:

- cycle time
- throughput
- WIP
- equipment utilisation

This information is combined into a single data set and is made available in tab and CSV delimited ASCII text files, a TWB spreadsheet version and a Calphurnia compatible version. Allowing the data to be analysed using general spreadsheet programs or using packages already within the total TCAD framework such as TWB, Calphurnia and RS/1 to Cornerstone via Calphurnia.

4.5 Applications of FASTT

Having described the implementation of FASTT this section gives examples of potential applications. Two possible scenarios are presented to demonstrate the use of the FASTT in creating factory models and using them to analyse manufacturing issues. Both examples utilise FASTT's WIP controlled experimental utility to automatically perform the simulations. Firstly, a comparison will be made between alternative versions of an existing process and secondly, the introduction of a new process to an existing fabrication facility will be evaluated. Although FASTT allows for the extraction and comparison of many alternative processes, relatively simple examples have been selected for the purpose of illustration.

4.5.1 Capacitor Dielectric Cost Comparison

Many potential process improvements are procedural, such as when and where wafers should undergo cleaning, while others are technological. Examples of the latter might be a diffusion recipe change, or a change of implant dose or energy. The options are vast and their implications on manufacturing are varied. For example, small changes, such as a 5% increase in implant dose, which may make a significant difference to the operation of the device, may only result in a marginal increase in actual processing time. Hence, this would be unlikely to have an impact on production, unless the implantation equipment was already fully loaded.

This example considers the case where there is a desire to improve the dielectric integrity of an MOS structure. The proposition is to substitute an oxide with a more robust ONO (Oxide, Nitride, Oxide) dielectric. As the proposed modification involves a number of process steps it is prudent to consider the implications on the manufacturing line before committing to full production. Thereby helping determine if the change is practicable or cost effective and if any investment in new equipment is required. In the following example, cycle time and throughput are used as metrics to determine the impact of the proposed process change.

The first step is to create the new ONO process flow within TWB by adapting the existing process. The next step is to use TCAD simulation to check that the required specifications are met. This results in two flows within TWB, the original process and the ONO process.

FASTT is used to import these flows into ManSim/X and to perform the simulations.

Figure 4.12 shows the throughput as a function of wafer starts for both processes. If the factory WIP is not increasing, then the wafer start rate will be equal to the throughput. It can be observed that the throughput of the ONO process is indistinguishable from that of the standard process until the facility approaches capacity, at approximately 1375 wafer starts per week, and that the trend becomes erratic due to bottlenecks. The proximity of the two plots means that little can be concluded from this metric alone.

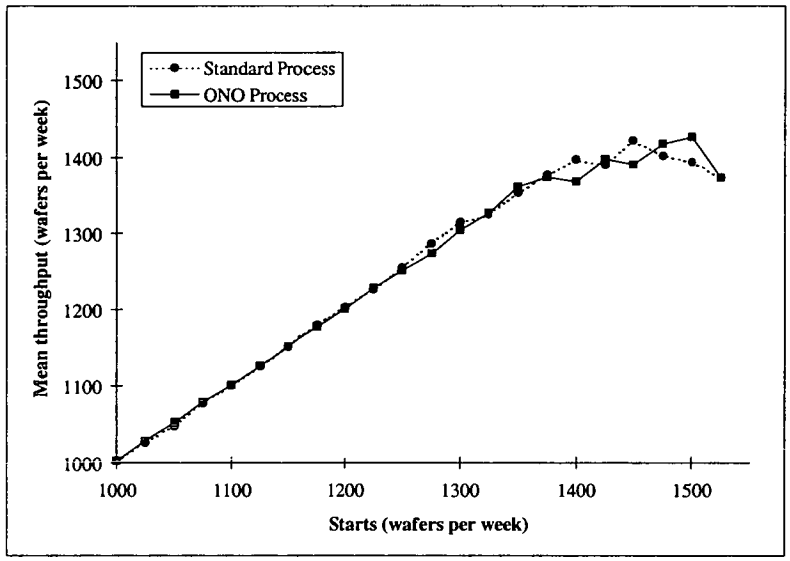

Figure 4.12: *Throughput vs. wafer starts for the standard and ONO processes.*

Figure 4.13 compares the cycle time of the two processes as a function of wafer starts. It can be observed that the mean cycle time for both processes remains roughly constant until line capacity is reached at approximately 1375 wafers per week. On closer inspection it can be seen that the mean cycle time actually rises gradually as the number of starts increases and that the ONO process has a mean cycle time approximately 10 hours longer than the standard process. When capacity is reached the cycle time for both processes starts to rise significantly. The dramatic increase in cycle time occurs as a result of bottlenecks forming within the fabrication facility.

It can be concluded that introducing the ONO process will increase the cycle time by approximately 10 hours regardless of the level of wafer starts and that there will be a

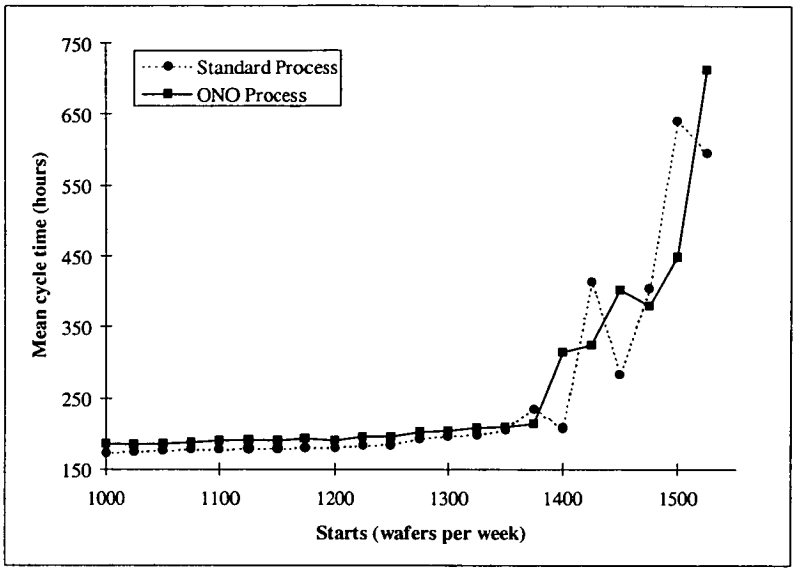

Figure 4.13: *Mean cycle time vs. wafer starts for the standard and ONO processes.*

negligible effect on the throughput when the line is below capacity.

4.5.2 Addition of a New Process

The ability to analyse the effect of introducing a new process into a fabrication line is essential for the early warning of potential issues resulting from a change of product mix. This situation is illustrated in the following example where the start rates of the other products within the fabrication facility have been set at arbitrary, but realistic levels. This models the situation when it is planned to introduce a new technology and capacity analysis is used to identify potential equipment bottlenecks.

This example demonstrates the effect that a given equipment set has on the fabrication facility's capacity. More importantly, it demonstrates how the automated link between TCAD and factory simulation can be used to provide timely identification of potential problems related to production. These can then be addressed early on in the design phase as part of the DFM process.

As before the process conditions are first determined using TCAD and this information then used to automatically create the data required by the factory simulation software. The factory

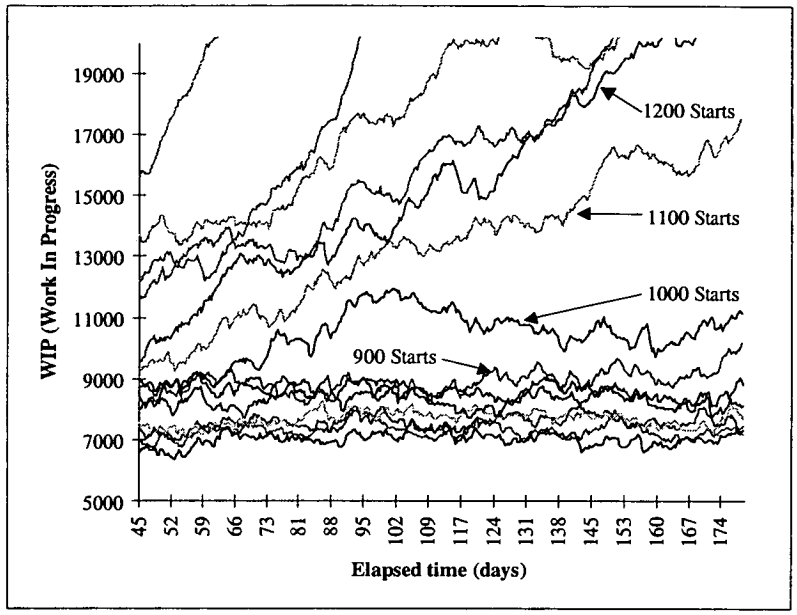

Figure 4.14: *Initial WIP vs. elapsed time for a range of wafer starts.*

simulations were run as in the first example, but in this case the factory is already loaded with WIP as would be the case when introducing a new process. Figure 4.14 shows the WIP for these initial simulations, for different start rates. From these results it can be deduced that a start rate of 900 wafers per week is possible without reaching the facility's capacity. However at 1000 wafers per week the WIP starts to increase indicating the capacity has been exceeded.

The mean equipment utilisation results for each simulation shown in Figure 4.14 are illustrated in Figure 4.15, highlighting the most heavily loaded items that are the most likely source of bottlenecks. Figure 4.16 clarifies the loading of the three most heavily used pieces of equipment for different numbers of wafers starts. The reduction of loading as the number of wafers starts increases indicates that other items of equipment are also becoming bottlenecks.

To investigate the possible benefits to factory performance extra equipment can be added to the model. In this example the two most heavily loaded work stations identified in Figure 4.16 were augmented with an extra item of equipment and the simulations were then re-run. Figure 4.17 shows the resulting WIP and it can be observed that a start rate of 1200 wafers per week is now possible with 1300 wafers per week exceeding capacity. Thus, the

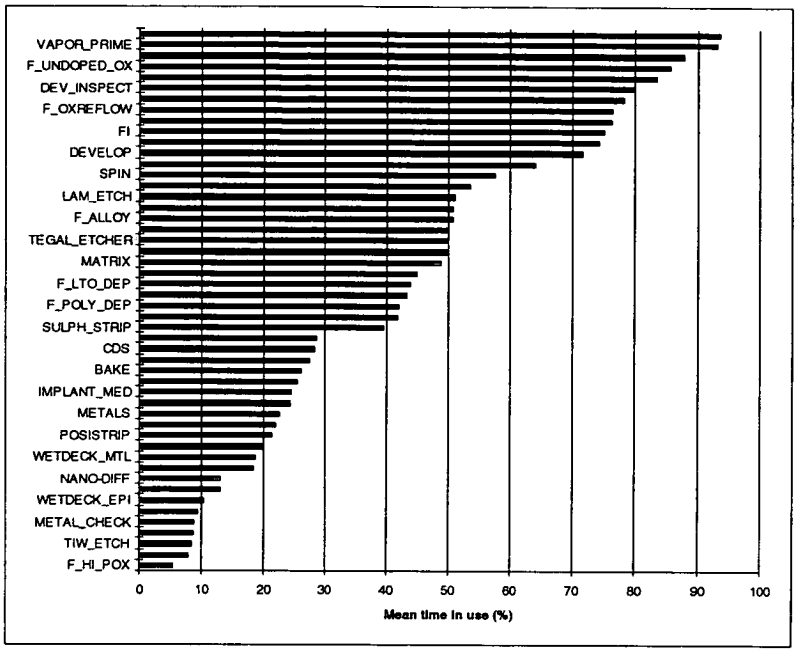

Figure 4.15: *Mean equipment utilisation figures for simulations shown in Figure 4.14*

addition of two pieces of equipment has increased the factory capacity for the new process by approximately a third.

4.6 Summary

Factory simulation and TCAD play important roles within an overall DFM strategy. Traditionally they are often seen and used as independent tools within the overall design of a process. However, integrating them within the total TCAD framework ensures that manufacturing issues need no longer only be considered once a process has been fully defined. The development of FASTT integrates TWB and ManSim/X, automating the creation and simulation of factory models based largely on information already available within the TCAD data file and presenting the results for analysis. This has the potential to reduce time to manufacture and hence the time to market of new or improved devices as well as enabling process development to take place without resulting in unforeseen manufacturing issues.

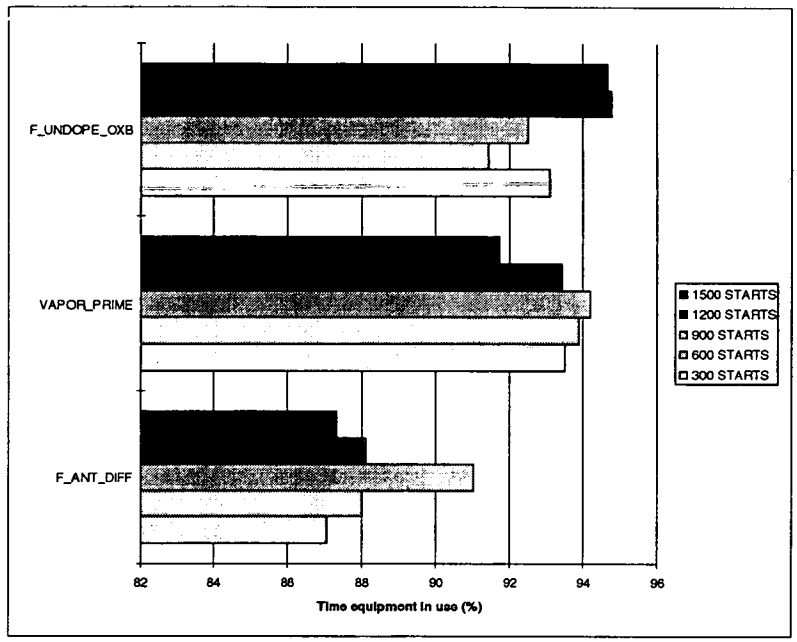

Figure 4.16: *Specific equipment utilisation figures for a subset of the simulations shown in Figure 4.14*

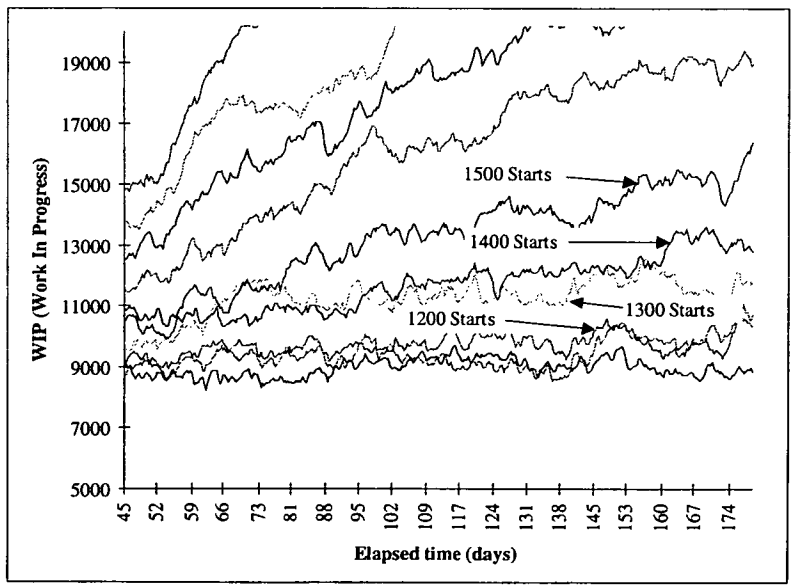

Figure 4.17: *Secondary WIP vs. elapsed time for a range of wafer starts.*

This chapter has outlined the design and operation of FASTT, a software tool that automates the creation and simulations of factory models, allowing the outcomes to be taken into account during process development. Two examples have been presented to indicate potential uses of FASTT. These have demonstrated the effect that changing the equipment set has upon potential process capacity and the impact that a minor alteration can have on manufacturing. The earlier these issues can be identified in the design cycle the better it is for the design team who can then either modify the process or use the increased lead time to implement changes to a fabrication facility.

Chapter 5
Incorporating Cost of Ownership Analysis into the Total TCAD Framework

The previous chapter introduced factory simulation into the total TCAD framework with FASTT, providing a means by which to assess the impact of process variations of manufacturing metrics such as cycle time, throughput and WIP. However, in order to measure the financial impact of any changes to a process flow using factory simulation, a more complex model than is usually available is required. Given that cost is a key issue in all areas of manufacturing it is essential for a complete framework that a method by which to forecast and compare the cost of production is incorporated. This chapter describes how this has been achieved through the development of a software tool called CASTT (Cost AnalysiS in Total TCAD). CASTT enables automated Cost of Ownership (COO) calculations to be performed, providing a quick and simple forecast of manufacturing costs within the total TCAD framework. This allows the potential implications of altering a process to be assessed during process development without significantly increasing the workload for the user.

5.1 Introduction

Although it is common practice to cost a process once the design has been finalised the detailed cost of processing a wafer is seldom considered during process development. By this point in the development cycle it is often too late to alter the design to minimise the production costs whilst still maintaining the quality and performance of the process. With manufacturing costs increasingly important this is an issue that should be addressed as early as possible during the development cycle in order to identify potential design changes which can be used to minimise unnecessary production costs. CASTT has been developed to meet this need by providing a method by which processing costs can be forecast and compared for alternative design options.

As with FASTT, the key to the success of this procedure lies with its automation. This ensures that the user should require limited additional training and need only to provide a minimal amount of additional input data in order to estimate the cost of manufacturing a wafer. To achieve this CASTT employs a similar method to that of FASTT. The core process flow information available from TWB, in conjunction with additional data, is used to determine the cost of each individual process step within the complete or a partial process flow.

5.2 Cost Of Ownership Model

As with all of the other elements incorporated within the total TCAD framework it is possible to utilise an existing package for the basis of our COO calculations. A generic COO model for semiconductor processing equipment is available from Sematech, comprising of 95 input data fields in 4 areas, some of which are shown in table 5.1.

Area	Example Data Fields
volume & throughput	MTTT, MTBF, MTTR, MTBA, MTTA, lot size, start rate, throughput, throughput yield, no. of systems per operator.
equipment	Initial costs, installation costs, floor space, training requirements.
production & running	Utility usage, supply/material costs, maintenance costs, personnel costs.
standard rates	Scheduled production, salary rates space rent rates, support/admin costs.

Table 5.1: *Data fields required by Sematech's COO calculation spreadsheet.*

Of these the minimum data fields required to perform a COO calculation are as follows:

- MTBF - Mean Time Before Failure
- MTBA - Mean Time Between Assists
- throughput at capacity per system

- start rate
- lot size
- throughput yield
- number of systems an operator can run

The Sematech COO spreadsheet gives a breakdown of annual costs for a number of areas over a five year period. It also produces a management summary of the results, an example of which is shown in figure 5.1. This provides a quick and simple way of assessing the cost issues of the process step and importantly provides a value for cost per good wafer out. This figure indicates the actual cost of successful wafer processing for each individual process step. So, when the COO is calculated for each step of a process it is this value that can be used to estimate the production cost of the complete process or any given subset.

5.3 CASTT - Cost AnalysiS in Total TCAD

This section describes the main aspects of the CASTT system, the cost of ownership calculation, the sources for the information required for the calculation and finally the general operation of the software. The use of CASTT to perform automated experiments is discussed in the following section.

5.3.1 Relevant Data and Sources

To provide the information for the COO calculations several data sources were required. The equipment details define the fixed costs for each process step, for example the initial purchase price, cost of shipping and installation. These are specific to individual pieces of equipment and can therefore be regarded as constants regardless of any changes to the process recipe. This is also the case for the standard rates and the data required in the production/running section, example values of which are also available from Sematech. In order to utilise this information within CASTT it is stored within a COO template model for each equipment type, as an ASCII version of the Sematech Excel spreadsheet.

MANAGEMENT SUMMARY		
		$/WAFER
PRODUCTION		
THROUGHPUT YIELD	99.95%	$0.13
DEFECT DENSITY (cm2)	0.01	
PROBE YIELD	98.22%	$9.05
COMPOSITE YIELD (Throughput Yield X Probe Yield)	98.17%	$9.18
* PRODUCTION UTILIZATION CAPABILITY	63.20%	
EQUIPMENT		
ORIGINAL CAPITAL COST PER SYSTEM	$3,400,000	$3.08
RAW THROUGHPUT (Throughput at Capacity)	57	
MAXIMUM WAFER STARTS PER WEEK PER SYSTEM	5992	
** EQUIPMENT UTILIZATION CAPABILITY	87.13%	
HEADCOUNT PER SHIFT		
DIRECT	0.9	$0.47
MAINTENANCE	0.3	$0.13
INDIRECT	0.5	$0.42
TOTAL	1.7	$1.02
TOP THREE COST DRIVERS		
SCRAP	39.49%	$9.18
CONSUMABLES	27.98%	$6.50
EQUIPMENT (Depr, Moves, Qual, Space, Train'g)	14.34%	$3.33
ALL OTHERS	18.19%	$4.23
COST PER GOOD WAFER OUT		**$23.25**

* PRODUCTION UTILIZATION CAPABILITY: The maximum production utilization for the given qualification requirements.
PUC = Equipment Utilization Capability - (scheduled process qual time)/ 168 hours as a %

** EQUIPMENT UTILIZATION CAPABLITY: The maximum utilization possible for the given equipment downtime characteristics.
EUC = 1 - (scheduled maintenance + unscheduled maintenance)/ 168 hours as a %.

Figure 5.1: *Sematech's COO spreadsheet management summary.*

However, the data within the volume/throughput section of the COO model are process dependent. Manufacturing information such as the required fields: MTBF, MTBA, throughput yield and the number of systems an operator can run are available from the MES or from the results of factory simulations. The 3 remaining required fields: lot size, throughput at capacity and the start rate are available from the information already present within a TWB data file which has been adapted for use with FASTT or one created by MASTT, see the following chapter. Lot size and start rate are stored in the TWB annotation box, see Chapter 4, and the throughput at capacity can be calculated given the processing time, the lot size and the number of batches that can be processed at any given time. In order to calculate this a single, fab dependent, file is used to store the number of batches that can

be processed at the same time for each piece of equipment. This file will rarely require alteration since the loading capacity of equipment seldom changes.

5.3.2 Extracting COO Data from TWB

The TWB extraction procedure that is used in FASTT is also used to generate single column text files for use with CASTT. However, the resultant single column files contain more information than is required for the COO calculation. Therefore, these files are then parsed to remove the extra data, leaving only the following:

- process ID
- product ID
- lot size
- start rate
- processing time for each step
- type of equipment for each step

By default the parsing program converts the data for every process steps. However, it can also be used to extract only part of the overall process flow. This is done by specifying the either the initial or final process step or both. These are defined by the operation number used with the TWB modules. This has obvious advantages in improving the speed of the cost calculation and ensuring that during process comparisons unnecessary operations can be easily omitted.

5.3.3 Cost Of Ownership Calculation

Although COO model templates are available from Sematech they are in a MS Excel spreadsheet format, making it easy to use but at the expense of requiring user interaction. However, this is inconvenient for integration within an automated framework so the

spreadsheet was translated into a C program for use in CASTT. This enables the calculation to be performed in a background mode, requiring only input and output files to be specified.

The input file is a single column text file that represents the column within the Sematech COO spreadsheet that contains the input data. A Perl script is used to convert the ASCII version of the spreadsheet into this single column text file. This procedure need only be done once for each piece of equipment, unless data such as the standard rates change. The data fields within the COO model which are extracted from the TWB data file will be overwritten when CASTT is used to calculate the COO so no data need be supplied for those fields.

Figure 5.2 illustrates the basic procedure used by CASTT to calculate the COO for a process flow. For each equipment type within the extracted process flow the basic COO template file is located, if none exists this process step is ignored. The extracted data from the TWB data file is overwritten onto this file to update the process dependent data and the resultant file used as the input to the COO C program. This then generates the cost per good wafer out for that process step which is added to the accumulative cost. The procedure is repeated until the cost of each process step has been identified.

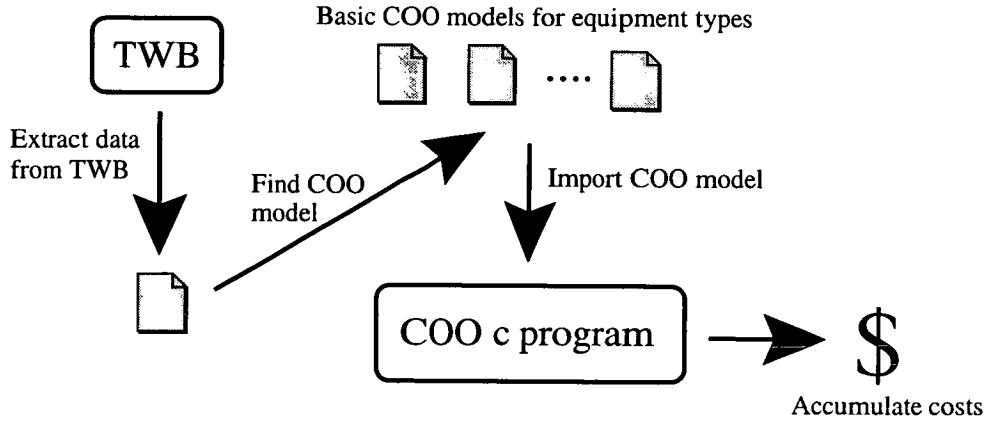

Figure 5.2: *COO calculation summary.*

5.4 Using CASTT

Whether CASTT is to be used to provide an overall process cost or to compare processing options it is unlikely that a single calculation will provide a clear picture of the costs

associated with IC production. For a single process flow it would be more useful to calculate the COO for a range of wafer starts than for a single start rate, thereby indicating the affect of scale of production on the cost. Likewise, by definition, a process comparison requires more than one set of costings, regardless of alternative wafer start rates. Therefore CASTT, as with FASTT, has been developed to automate the running of multiple calculations.

5.4.1 Performing Automated Calculations

CASTT uses a similar method to control the COO calculations as FASTT does when automating factory simulations. The control program uses the initial settings shown in figure 5.3 to provide the necessary arguments for the shell scripts and Perl programs it initiates. It can be seen from figure 5.3 that both an upper and lower limit of wafer starts must be specified. This is necessary because, unlike the WIP control within FASTT, there is no method by which to automatically identify either of the limits. However, this is a minor issue since in most cases COO calculations will be performed in conjunction with factory simulation analysis, which will identify realistic start rate limits. As previously mentioned, it is possible to calculate costings from a subset of the process flow. Selecting option 6 displays all of the possible operation numbers and descriptions of the modules within TWB, allowing the initial and/or final operation numbers to be easily set.

```
Default settings are as follows to change enter the setting number.

      1. Cost model name.........................twbcost
      2. Number of experiment wafers.............2
      3. Product start rate increment............50
      4. Minimum start rate .....................100
      5. Maximum start rate .....................1500
      6. Operation limits .......................none

      0. Quit, use present values.

Enter option to change defaults, or 0 (zero) to finish editing:
```

Figure 5.3: *CASTT COO calculation initial settings.*

After the initial settings have been defined the control script automates the running of the calculations. The method used to perform the calculations is illustrated in the flow diagram shown in figure 5.4. Essentially each process flow option is taken in turn and the COO

calculated for each of its individual steps. Each COO calculation is performed over the range of starts identified in the initial settings. During the analysis the cumulative COO for the process flow (or subset) is updated, providing an overall cost for each start rate for each process split on completion of the analysis.

5.4.2 Automated Result Collation

In keeping with FASTT the results of a COO experiment are automatically collated into a number of formats: tab and CSV delimited ASCII text files, a TWB spreadsheet version (figure 5.5), a Calphurnia compatible file(figure 5.6) and a Gnuplot generated postscript plot of the data as shown in figure 5.7. This combination ensures that the data can be quickly analysed without requiring significant input from the user. In particular it means that the results can be easily combined with other data, such as TCAD and factory simulations.

5.5 Applications of CASTT

The previous sections have outlined the design and implementation of CASTT, this section expands on this by demonstrating two potential uses. These examples demonstrate the benefits of using CASTT to provide costings information during process development. At its most basic CASTT can be used to calculate the manufacturing cost of a wafer undergoing complete or partial processing, enabling the forecasting the cost of a process during development. However, CASTT can also be used to compare alternative processing options. This aspect of CASTT is illustrated in the following examples. The first example uses CASTT to perform a cost comparison of capacitor dielectrics and the second considers a design choice between a number of equally valid technological solutions based on the cost of manufacture.

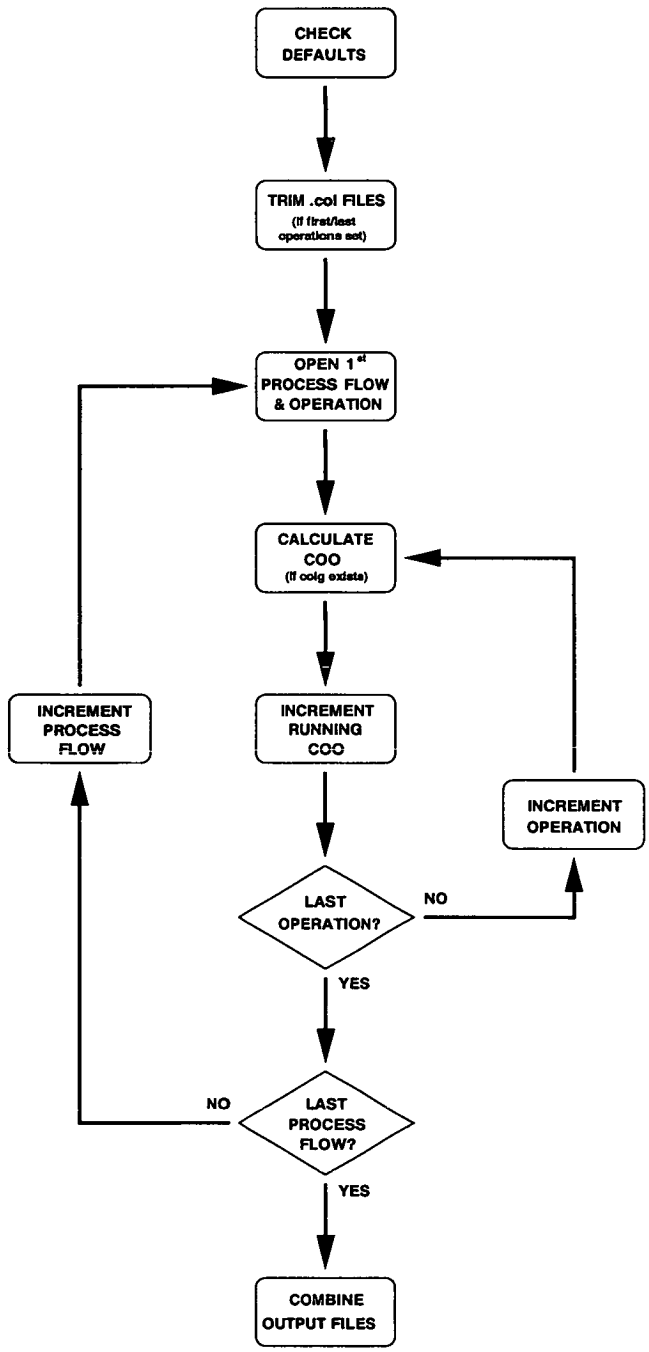

Figure 5.4: *CASTT COO calculation flow diagram.*

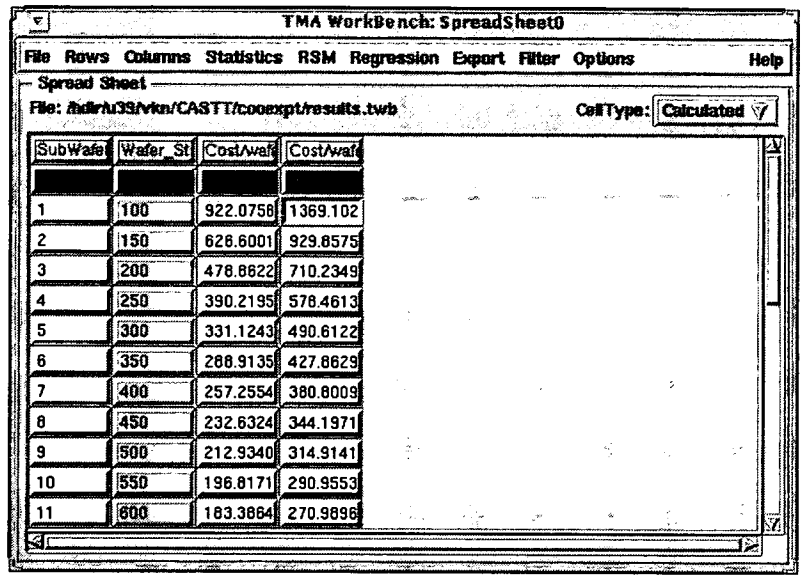

Figure 5.5: *Screen-shot showing COO data from two alternative process flows for a range of wafer starts imported into TMA spreadsheet.*

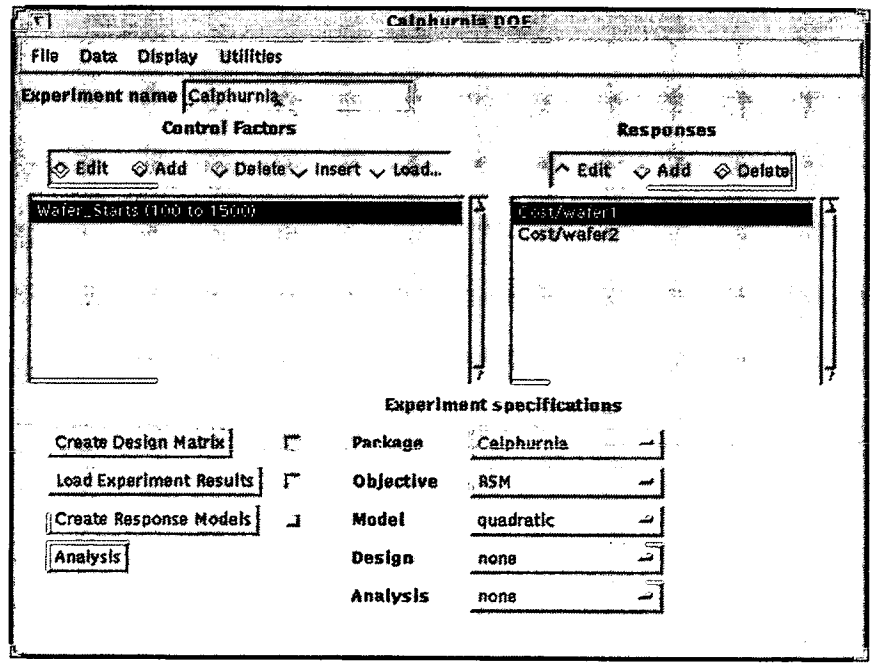

Figure 5.6: *Screen-shot showing COO data from two alternative process flows for a range of wafer starts imported into Calphurnia.*

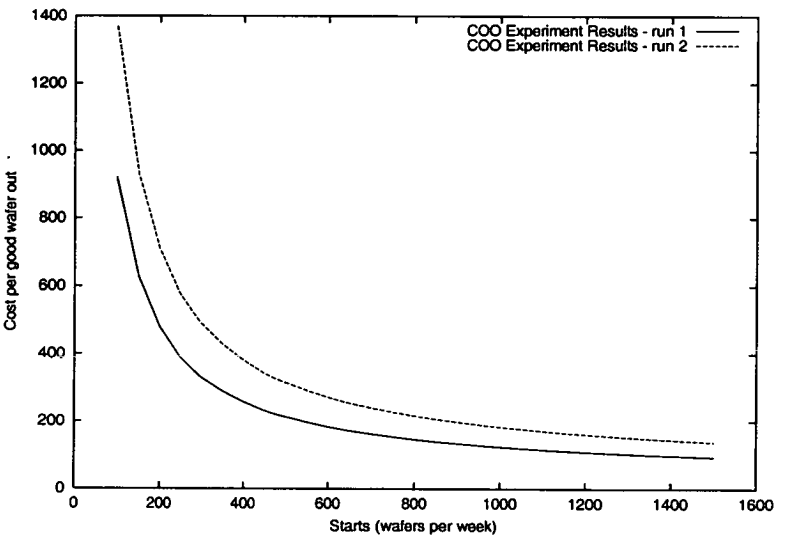

Figure 5.7: *Plot of the results of the COO calculations for two alternative process flows for a range of wafer starts, automatically generated using Gnuplot.*

5.5.1 Capacitor Dielectric Cost Comparison

This example further considers the scenario presented in the previous chapter; the comparison of a single oxide layer of dielectric and an ONO combination alternative. The previous example concluded that there would be a 10 hour increase in cycle time and little impact on throughput at start levels below 1375 wafers per week. By using CASTT we can compare the manufacturing costs for each alternative. This will provide more information regarding the choice, allowing the decision of whether or not the impact on manufacturing issues and cost can be justified in terms of the technological advantage of using the ONO process.

While the standard process uses a single oxide layer grown in a furnace, the ONO process uses a thinner thermal oxide with layers of nitride and oxide deposited on top. Clearly there are additional processing steps: pre-process cleans, layer thickness measurement and a photolithography stage which is likely to be required to remove the deposited nitride from the field oxide. However, to simplify the example only the diffusion and deposition steps will be considered. Since only these steps differ between the process flows only they need be compared using CASTT. This has the advantage of reducing the time it takes to perform the analysis as well as the time taken to ensure the validity of data the within the COO templates for the required processing steps. As previously mentioned, the operation numbers used to identify the process modules in question within TWB are used in CASTT to limit the cost analysis to these process steps only.

The results plotted in figures 5.7 and 5.8 show the increase of processing costs for the ONO dielectric relative to the cost of the standard process as a function of the weekly wafer starts. The downward trend of the cost increase as the start rate rises is due to the initial costs of the equipment being spread over a greater number of wafers. The decision of whether or not to implement the change will require the assessment of the benefit of the technological change to product yield and quality relative to the increased production cost for the expected number of wafer starts.

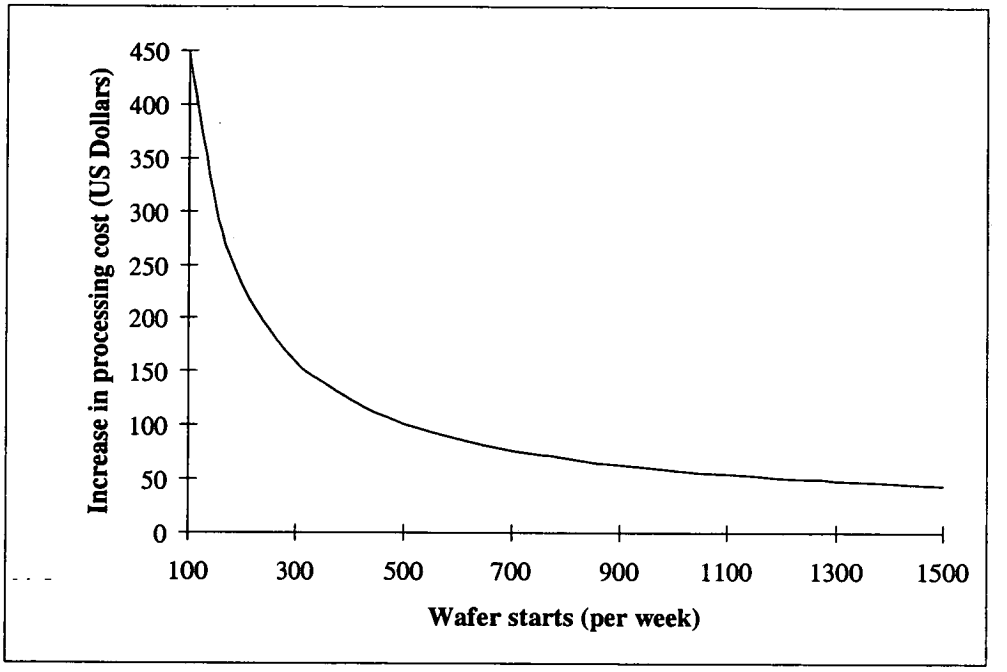

Figure 5.8: *Increase in cost per wafer using the ONO rather than the existing process vs. wafer starts.*

5.5.2 Alteration to an Existing Process

This example considers the optimisation of process steps used to form the base region of a bipolar device. For simplicity, only two control factors: the base implant dose and the drive time have been considered, along with two responses: the sheet resistance (R_s) and the junction depth (X_j). An experiment was designed using the DOE package in TWB and the alternative process flows simulated and models fitted.

Figure 5.9 shows the response surfaces for R_s and X_j as a function of base implant dose and base drive time. The shading highlights the areas that fall outwith the given response specifications ($130 < R_s < 150\ \Omega/\square$ and $3.9 < X_j < 4.1\ \mu$m). It can be seen that a number of potential solutions exist which meet the technical specification.

COO analysis can be used to provide another metric by which to evaluate the options. It is clear that the dose and drive time should be minimised, since the time taken to perform the implant is governed to some extent by the dose, as this will maximise the throughput of the equipment. However, it is not known which of the two factors will have the greater effect of

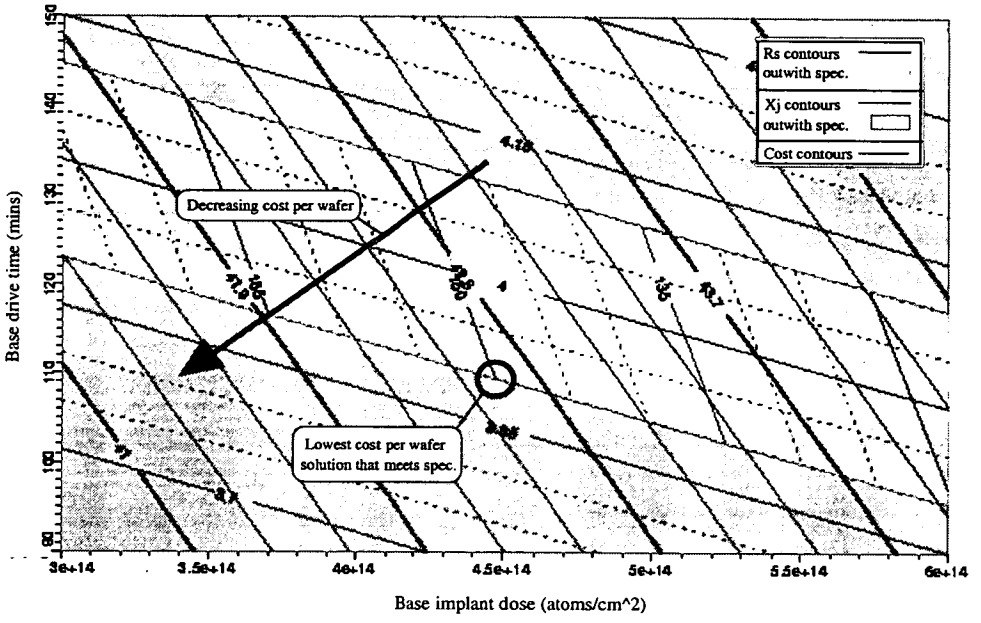

Figure 5.9: *Response surfaces for R_s, X_j and cost plotted as a function of base implant dose and base drive time, shading indicates areas outwith spec, the direction of decreasing cost is shown by the arrow and the point of the lowest cost solution is circled.*

the cost. CASTT can be used to identify the wafer costs of the individual process steps by using the comparison limits option (which allows the user to specify the beginning and end of the cost calculation). The costs can then be summed for each of process combinations used in the TCAD experiment and the response surface plotted as with R_s and X_j. The results of these calculations have also been plotted as a response surface in figure 5.9. The direction of decreasing wafer cost is indicated by the arrow and the point of the optimum solution (a dose of 4.47×10^{14} atoms/cm^2 and a drive time of 109.5 mins) circled.

5.6 Summary

The development of CASTT has enabled the integration of COO analysis into the total TCAD framework. This has made cost calculations a quick and simple procedure just as FASTT has done for manufacturing issues such as cycle time and throughput. It is now possible to consider economic issues at a much earlier stage in the development of a process than is

currently common place because of the significant reduction in the time it takes to perform the analysis. This has the benefit of making it possible to minimise production costs whilst still maintaining product quality and functionality.

This chapter has described the design, implementation and potential uses of CASTT. Examples of CASTT in use have furthered the process comparison introduced in the previous chapter by examining the increase in cost incurred as a result of changing from the standard oxide dielectric to the three stage ONO dielectric. The second example illustrated how COO analysis can be combined with the results of a TCAD DOE in an RSM to identify the most cost effective solution from a range of solutions which meet the technical specification. Together with the examples in the previous chapter, it can be seen that FASTT and CASTT provide a significant contribution towards assessing the practical implications of process development and a complete DFM strategy.

Chapter 6
Automated Generation of Up-to-date TCAD Models

The previous two chapters have described the development of FASTT and CASTT and shown the potential benefits to be gained by using them to examine the impact on manufacturing issues during process development. However, the one issue that still remains untouched within the total TCAD framework is how up-to-date the simulation data is. This is an important consideration during analysis with FASTT, CASTT or TCAD. This chapter introduces MASTT (MAnufacturing execution System in Total TCAD), the final piece of software reported within this thesis. It was developed to ensure that analysis within the total TCAD framework is performed using current data. This is achieved by integrating an MES into the total TCAD framework, enabling the TCAD data files to be stored and up-dated as part of the main fab database. This allows the current TCAD data files, which also contain the manufacturing data required by FASTT and CASTT, to be extracted. This improves access not only to a more detailed online documentation of the process but also means that TCAD, factory simulation and cost analysis can be more readily performed by engineers without requiring a full knowledge of the simulation software. Perhaps most importantly, this allows them to use TCAD as a day-to-day analysis tool with which they can simulate a specific lot to the end of line. Thereby, enhancing the understanding of the process and providing a tool to aid processing decision making.

6.1 Introduction

Over recent years TCAD has become a widely used tool within the field of process design and development. Unfortunately, it is too often the case that once a device is released to full production, subsequent modifications to the process mean that the development TCAD data

files may no longer provide an accurate reflection of the actual process flow. As a result, when TCAD would be beneficial to either help sustain or improve processes, accurate TCAD files for the process are simply not available. Therefore, the TCAD decks invariably require updating before representative simulations can be performed. This is an error prone and tedious procedure because the complete TCAD process flow must be thoroughly checked, typically taking a couple of days. As such, this seldom happens and the use of TCAD as an analysis tool for continued process development is therefore limited.

MASTT has been developed to address this issue and has two key aims, to enhance the operation of FASTT and CASTT by automating the inclusion of manufacturing data within the TCAD data file and to ensure that the data accurately represents the current processing conditions. Additionally, to encourage the use of MASTT it should only require minimal further training for TCAD or process engineers. This can be achieved by ensuring that the system is as automated as possible and where this is not possible provide adequate instructions for those steps. This also reduces the potential for data handling errors, ensuring the validity of the TCAD models created.

A method of integrating process simulation with a CAM system has already been investigated in 1989 [121] and published [111]. An interface was designed within the COMETS CAM system to enable 1-D process simulation of lots as they passed through the line. This provided a system which could be used to investigate the effect of future processing whilst aiding the understanding of the process. Unfortunately, this work was carried out before TCAD was more widely accepted within the industry and because of the need for what was then significant computational processing power, or perhaps the limitations of 1-D simulation the approach was never further developed. However, with the improvements in TCAD and the development of more extensive TCAD frameworks, such as TWB and VWF, this original work can now be updated and extended through MASTT. The integration of Promis within the total TCAD framework provides a more flexible system which benefits from the other elements within the framework whilst still providing the same basic forecasting ability.

6.2 MASTT - MAnufacturing execution System in Total TCAD

MASTT uses an MES, in this case Promis, to store sections of TCAD code that can be extracted to build a a complete TCAD process flow. The code is stored as text documents within the PROD hierarchy which was discussed in chapter 3. The following sections highlight the issues encountered during the development of MASTT and describe its operation and implementation.

6.2.1 TCAD Data Storage in Promis

To ensure that the data used for TCAD simulations is kept up-to-date a structure for its storage within Promis must be defined. By storing the data within Promis it is a simple matter to include the TCAD code within the sign off loop for any changes made by a process engineer since the standard Promis entries must also be edited. MASTT uses attached DOCU text files which, when combined, contain all of the information required for TCAD simulation of the process flow. These take the form of TCAD code but with those parameters defined elsewhere within the Promis process flow replaced by the parameter names. The DOCU files and the parameter information held within the Promis database for each lot provide all the information required to build a TCAD process flow within TWB. This approach also has the additional benefit of providing detailed on-line process information, in excess of what is commonly available.

The *recipe* level of the PROD hierarchy is particularly suited to TCAD data storage. It provides sufficient detail about individual process steps without incorporating the all of the equipment and wafer handling instructions outlined at the *operation* level. The *procedure* level is part specific, so any TCAD code stored at this level would need to be updated for every instance of a process step within each *procedure* that uses it rather than once at a *recipe* level. Additionally, PROMIS has a *stage* command available which is commonly used to group together parts of the process flow for reporting. This arbitrary level was chosen to allow to collate the data from groups of *recipes* into TWB modules, thereby allowing analysis

of the process flow in a format with which process engineers will already be familiar.

TCAD can be used to analyse a number of issues. The most basic of which allows an engineer to investigate whether or not processing specifications (e.g. oxide thickness and sheet resistivity) have been, or will be, met during processing. However, in most circumstances an engineer will be more concerned whether or not the device will meet the parametric test criteria. To simulate this the TCAD model must also incorporate device simulation code. In order to preserve a single data source for the TCAD model, this information should also be stored within the MES database. Obviously a *recipe* level document is inappropriate for this data, so any device simulation TCAD code is stored at the *PART* level.

6.2.2 Extracting Data from Promis

The extraction of the data from the Promis database is controlled by a UNIX shell script. The user is initially prompted for the lot ID, which once entered is used by a series of Perl programs to generate Promis extraction scripts and VMS executables. This ensures minimal contact with the database for unfamiliar users requiring them only to run the VMS executables and FTP the given files between systems as directed. Figure 6.1 shows an example of the UNIX script illustrating its ease of use.

MASTT generates two Promis extraction scripts, demoflow.scr and demoequip.scr, which are executed by running demoextract.com on the Promis VMS system. These extract the process flow and the equipment used to process the lot, generating their respective .tab files. The demoflow.tab file is then used to generate the Promis document extraction script, demodocext.scr and its VMS executable. Running demodocext.scr extracts the large number of small files which contain the sections of TCAD code, each of which must be transfered to the UNIX system and stored in the TCAD code directory. Once this has been done the TCAD process model can be created.

```
Enter LOT ID
demo

Promis and VMS scripts written for:

      LOT: demo

ftp these files to your VMS account:

    demoextract.com
    demoflow.scr
    demoequip.scr

and run demoextract.com (@demoextract)

ftp the output files back to your unix account:

    demoflow.tab
    demoequip.tab

Press return when completed.........


Promis and VMS scripts written for:
      LOT ID: demo

ftp these files to your VMS account:

    demoextractsecond.com
    demodocuext.scr

and run demoextractsecond.com (@demoextractsecond.com)

ftp the output files back to your unix account:

 i.e. the recipeidTCADOUT.txt files

Press return when completed.........


Extracting FS data from Promis extraction

Extracting equipment set information
Extracting parameter names and values
Updating TCAD data from extracted Parameters
Combining all information to create TCAD flow
TCAD flow: PARTNAME/EXTRACTED_TCAD_FLOW ready for import into TWB
```

Figure 6.1: *Example of the instructions to user generated by the MASTT control script.*

6.2.3 Forming the Process Model

The flow and equipment files extracted from Promis are used in conjunction with the TCAD template files from the recipe DOCU files to provide the inputs to a series of Perl programs. These programs combine to build a single TCAD flow file that can then be read into TWB. This is a 5 stage process which, once complete, develops the file structure illustrated in figure 6.2.

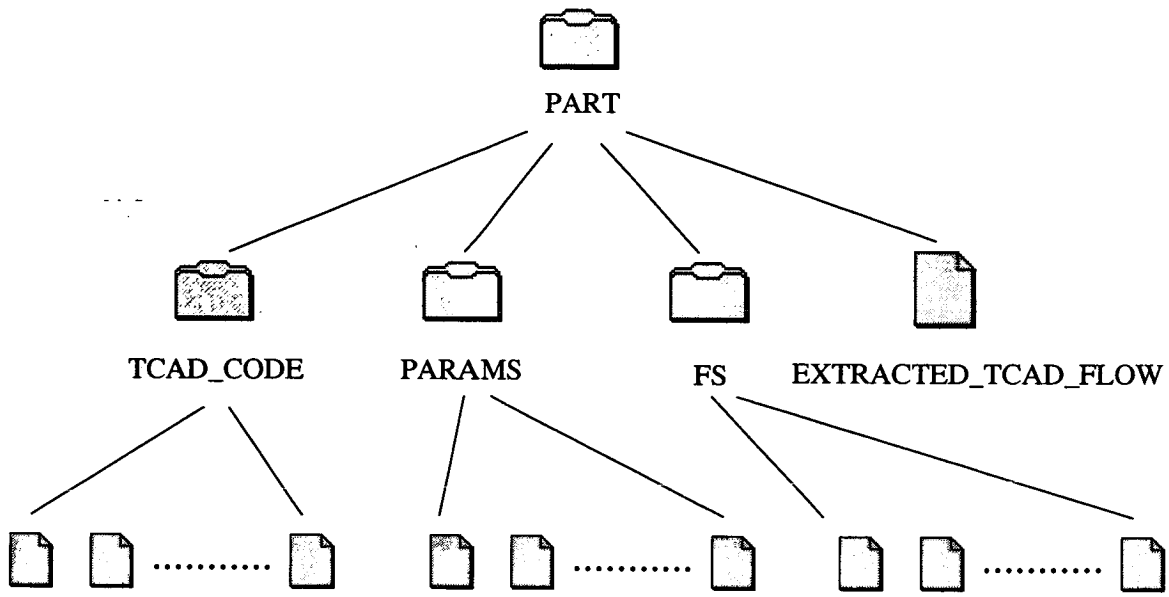

Figure 6.2: *File structure of the data extracted by MASTT from the Promis MES.*

Stage 1. The extracted process flow file is parsed. For each recipe the following information is extracted and written to a file in the FS (Factory Simulation) directory in the following format:

$step RECIPE_NAME_FS

comment fs operation RECIPE_NAME

comment fs time TIME_TAKEN_AT_RECIPE

comment fs wstat EQUIPMENT_GROUP_USED

Stage 2. The Equipment set options are then added to these files, by parsing the equipment set file, and hence the format becomes:

$step RECIPE_NAME_FS

comment fs operation RECIPE_NAME

comment fs time TIME_TAKEN_AT_RECIPE

comment fs wstat EQUIPMENT_GROUP_USED

comment fs equipment EQUIPMENT_NAME_1

comment fs equipment EQUIPMENT_NAME_2

Stage 3. The parameter names and values for each recipe are extracted from the process flow file. These are written to a file for each recipe in the PARAMS directory, for example:

$dose 1e14

$energy 100

$species phosph

$tilt 0

$rotation 45

Stage 4. For each recipe that a TCAD data template exists the corresponding parameter file is parsed and each of the parameter names in the TCAD data file are replaced by the extracted values, as illustrated below:

The original TCAD data template is:

```
implant $species dose=$dose energy=$energy tilt=$tilt rotation=$rotation
```

After replacement this becomes:

```
implant phosph dose=1e14 energy=100 tilt=0 rotation=45
```

Stage 5. The individual recipe files are then combined in the order of the process flow. Any TCAD data for the *recipe* is written first, followed by the processing equipment details. The final process flow is grouped by the Promis stage definitions, giving a single file containing not only the complete TCAD flow, but also information on the equipment upon which it can

be processed. Once all of the individual recipe stages have been added any device simulation TCAD data from the *part* level is then added to complete the TCAD deck.

6.2.4 Importing the Process Model into TWB

A feature of TWB is its ability to import TCAD code written for each of the particular TMA simulators into the virtual fab. In order to translate the code into a set of individual process blocks two commands, $module and $stage are used. This ensures that the TWB data file can be easily read and used. Unfortunately, regardless of the driver information contained within the TCAD template files the TWB conversion program always defaults to the 2-D process simulator TSUPREM-4. Hence, some manual editing of the created TWB experiment is required to ensure that the simulator driver is altered for some of the modules. This is particularly important for any device simulation steps and the initial module which usually requires an adapted TSUPREM-4 driver since no data needs to be imported into the simulator from a previous step as with the standard TSUPREM-4 driver.

6.3 Additional Applications of MASTT

Implementing MASTT within a manufacturing environment has many potential uses in addition to ensuring that the TCAD code is up-to-date and the ability to automate the sourcing of data for use with FASTT and CASTT. At the most basic level, the additional processing information introduced to the MES through the inclusion of the TCAD data provides a more detailed process flow description than is usually incorporated into an on-line system. As this can be accessed at any point within the facility, through an MES terminal, it provides a valuable hands-on resource for both aiding process understanding and training since the engineer can examine the details of the surrounding process steps. This has the added benefit of providing the process engineer with easy access to the TCAD data files enabling TCAD, factory simulation and costing analysis to be readily performed. However, one of the most important uses of automating the generation of up-to-date TCAD code is the ability to use it to forecast the processing of specific lots.

6.3.1 *Look Ahead & What If* Analysis

There are two main uses of TCAD simulation as an on-line analysis tool, *look ahead* and *what if* analysis [111]. *Look ahead* provides a facility whereby an engineer can use TCAD to simulate the effect of processing a lot to the end of line from any given point in the process. This is accomplished by extracting the partially completed process flow from the MES and combining this with previously extracted TCAD data for the same process. By simulating the lot to the end of processing and deriving the final device parameters it may be possible to indicate whether or not continued processing of the lot is worthwhile. This decision can then be based upon analysis rather than subjective assessment as is currently common practice within many fabs.

Through the use of *look ahead* it may be apparent that the lot will fail to meet the required specification if processing is continued until end of line. However, by providing the engineer with the processed TCAD steps it becomes possible to simulate the effect of altering the subsequent processing conditions. This makes it possible to analyse what measures, if any, can be taken to rectify the effects of earlier processing. Thereby allowing informed corrective action to be taken rather than merely relying upon an engineers previous experience.

Hence, the potential exists to significantly reduce production costs, in terms of the cost of processing wafers which are almost guaranteed to fail to meet specification and by enabling replacement wafers to be started at an earlier stage, or by saving mis-processed wafers through the use of what if analysis.

6.3.2 Example of *what if* analysis using MASTT

In order to demonstrate the potential of integrating TCAD and MES software through the MASST interface the following scenario has been created and a potential case of mis-processing considered.

The process uses a double implant stage to set the threshold and punch through voltages (V_{th} and V_{pt} respectively) during the formation of the nMOS devices. Firstly there is an implant of boron, dose = 7×10^{11} atoms cm^{-2}, energy = 25 keV, followed by another boron implant,

dose = 7×10^{11} atoms cm^{-2} , energy = 140 keV. However, the wafers are mis-processed, receiving a higher dose, 8×10^{11} atoms cm^{-2}, during the initial implant.

The first question that must be asked is if this will result in the wafers failing meet the parametric specifications? In order to answer this the information from the part processed wafers can be extracted from the MES and the TCAD model imported into TWB. A model for a completed batch of wafers must also be imported. The additional TCAD code required to simulate the mis-processed wafers to end of line is added from the completed wafer flow. The resultant parameters for both simulated flows are compared in table 6.1.

Device Parameter	Correctly processed	Mis-processed
Threshold voltage (V_{th})	0.4745 V	0.517 V
Punch through voltage (V_{pt})	10.697 V	10.660 V

Table 6.1: *Simulation parameters from correctly processed and mis-processed wafers.*

It is clear from the simulation results that the mis-processed wafers will fail to meet the parametric test specifications ($V_{pt} > 10V, 0.475 < V_{th} < 0.495V$). So if the wafers are to be saved subsequent process steps must be altered. This can be achieved either through the alteration of existing recipes or by the introduction of a new recipe. The former provides the simplest option in this scenario. An adjustment to the second implant will leave the wafers back on the standard process flow after the corrective action.

In this example, to counter the effect of the additional dopant at the surface of the silicon the second implant can be adjusted to either push the peak concentration further into the silicon or reduce its concentration so that it has less effect at the surface of the silicon. To determine the best combination of these possible solutions a DOE is performed using the built in experimental design features within TWB. The results from a 9 simulation CCF (Box - Wilson cube) design, in the form of a contour plot, are shown in figure 6.3.

A cubic model has been fitted to the simulation results giving a fit with R^2_{adj} figures of 0.99997 and 0.99993 for V_{pt} and V_{th} respectively. The shaded areas on the RSM represent the areas of V_{pt} and V_{th}, left and right respectively, which lie outwith specification. The final choice of the corrective implant dose and energy should be made once the response distributions have

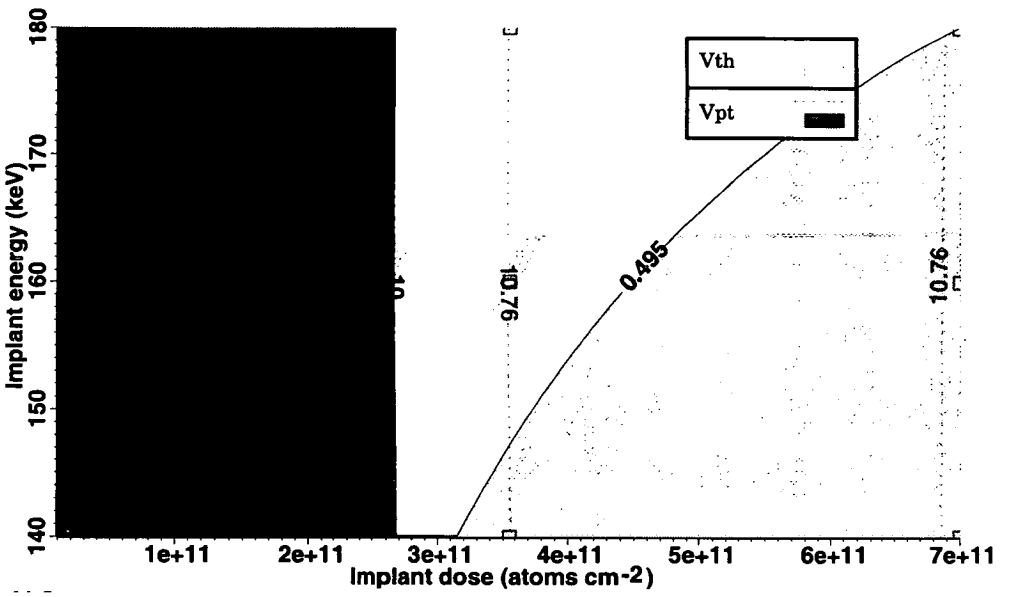

Figure 6.3: *RSM: Phosphorus implant corrective action.*

been considered to ensure that a robust combination is chosen, as discussed in chapter 2.

This example of how MASTT can be used to supply the TCAD code to enable *what if* analysis to be performed for a mis-processed lot indicates the power of using TCAD for day-to-day decision making on the production line. Before the development of MASTT such analysis would have taken days rather than hours rendering it too costly to be used on all but the most wide spread cases of mis-processing. By enabling access to the total TCAD framework and using the data held on the MES both the technological and practical aspects of altering the future processing of a lot can be quickly assessed. This has the potential to significantly save both time and money as the inherent value of a lot can be retained and the product may not need to be restarted saving days or even weeks on the final delivery time.

6.4 Summary

MASTT automates the sourcing of manufacturing details required by FASTT and CASTT and ensures the creation of up-to-date TCAD simulation files from data stored within the on-line MES database. This reduces the effort required to initiate accurate TCAD analysis

of day-to-day processing issues or continued process development once a process has been released to manufacture. The implementation of MASTT provides a means by which process engineers can access tools previously only used by designers and developers. This allows TCAD analysis to be easily performed within the production environment without the need for extensive TCAD training.

Chapter 7
Review, Discussion and Future Work

The previous chapters have discussed the elements within the original total TCAD framework and those which have been incorporated as a result of the work presented in this thesis. They have also described the development and implementation of the software tools required to achieve this. This final chapter aims to draw all of the elements of this thesis together by reviewing what has been accomplished, discussing its implications for semiconductor development and manufacturing and by considering possible future developments.

7.1 Review

This thesis has presented three new software tools: FASTT, CASTT and MASTT. Together with the original total TCAD framework these allow the process designer or developer to examine not only the technological aspects of a device or process during development but also the effect on the manufacturing environment. The resulting total TCAD framework is shown in figure 7.1 and this section summarises the main features of each tool.

7.1.1 FASTT

The development of FASTT forms the basis of the bulk of the thesis. It automatically generates a factory simulation model from the information contained within TWB and any supplemental manufacturing details which have been included manually or automatically via MASTT. The TWB data file is parsed to generate a factory model with products for each of the full factorial of process options within TWB. A UNIX control script can then be used to automate the running of factory simulations and the collation of the results for a range of wafer starts. This requires an initial start rate and an increment to be defined and uses the

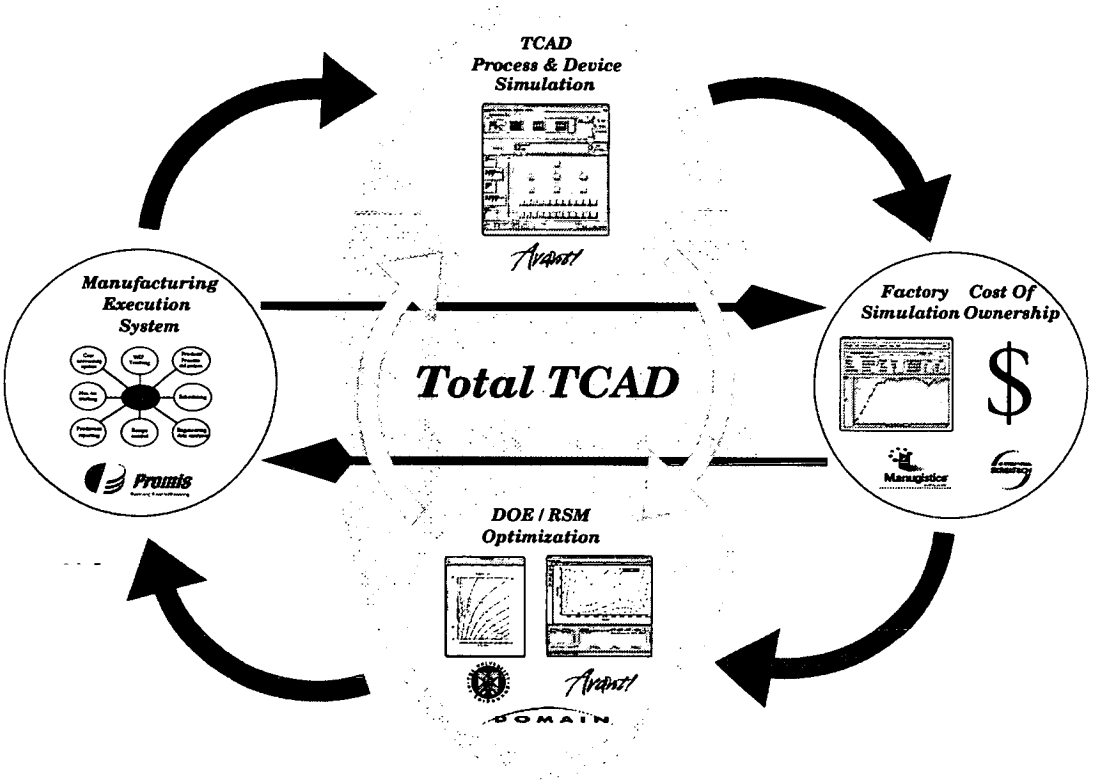

Figure 7.1: *The new total TCAD framework.*

WIP level to cease further simulations as this can be used to identify a start rate in excess of the facility's capacity. The collated results of the factory simulations, nominally: throughput, cycle time, WIP and equipment utilisation are made available in CSV and tab delimited files as well as in formats for reading into TWB spreadsheets and Calphurnia.

7.1.2 CASTT

CASTT provides the engineer with quick and efficient access to Sematech's COO calculation. As with FASTT the process flow is extracted from TWB this is then broken down to include only the information pertinent to the COO calculation. The COO for each step of the process is then calculated and summed. Alternatively, a subset of the process can be defined to reduce the number of calculations. Again, in keeping with FASTT an automated series of calculations can be performed over a range of wafer starts, although in this case the upper and

lower start rates must be identified. The results of the COO calculations are made available in CSV and tab delimited files and in a suitable format for importing into TWB spreadsheets and Calphurnia.

7.1.3 MASTT

MASTT has been developed to ensure that up-to-date data is used for TCAD, factory and COO analysis. A TCAD data storage methodology, using text documents, has been defined using the Promis MES. MASTT extracts the TCAD process flow from the MES database using the text documents and augments it with the manufacturing information that is required for use with FASTT and CASTT. The extraction process has two main stages, through which the user is guided by a UNIX script. Firstly, the lot ID is used to extract the Promis process flow and manufacturing information and secondly the text documents containing the TCAD data for each of recipes used within the process flow are extracted. This information is then collated by a series of programs to build up a TCAD process flow, which can then be imported into TWB.

7.2 Discussion

The original total TCAD framework enabled the implementation of DFM strategy capable of addressing the technical aspects of process and device development. The integration of TCAD with DOE and RSM tools has allowed engineers to determine the most suitable manufacturing conditions to maximise device yield. However, the existing total TCAD framework gives no consideration to the effect that the solutions will have on production. Manufacturing of semiconductors is a complex procedure which is predominantly carried out in high volume and one where financial success is largely governed by the time it takes a product to reach the market. It is these factors that have driven the work in this thesis, enabling the implementation of a DFM strategy that considers both the technical and practical aspects of process development.

FASTT, CASTT and MASTT allow engineers automated access to up-to-date simulation data

which can be used to identify manufacturing issues such as cost, cycle time, throughput and WIP. These are key issues in a production environment and taking them into account early in the design and development of process has the potential to save a significant amount of money without adversely affecting product quality. As importantly, the ability of FASTT to forecast issues such as equipment bottlenecks or insufficient capacity ensures that they can be identified well in advance of them impacting the time to market of the devices to be produced using a new or revised process.

Obviously, manufacturing issues could have been addressed during process development since the advent of the spreadsheet but this rarely occurred. It is only with the introduction of automated tools such as FASTT, CASTT and MASTT that this type of analysis becomes feasible as previously the time taken to manually collate and verify the data would have precluded it. The ease of use and its inclusion in an existing framework ensure that the work presented in this thesis can form the basis of a complete DFM strategy.

7.3 Future Work

After the development of any software it often becomes apparent that other algorithms or even other languages would have been a better choice in the first place. The software tools reported within this thesis are no exception. A great deal of the C code written could be replaced by Perl code and vice versa. This may result in more elegant code, by reducing the memory management needed with a C program or by utilising the string manipulations available within Perl. However, none of this would alter the ultimate function of the programs or have significant impact on their speed. Indeed, because of the relative speed of the TCAD and factory simulation tools involved within the framework in comparison to FASTT, CASTT or MASTT the operational speed of the software was never a major consideration. That said, there are two particular areas where the work could be furthered.

7.3.1 Alternative Commercial Software

Each of the three commercial packages integrated using FASTT, CASTT and MASTT: Avant!'s TWB, Manugistics' ManSim/X and Promis have at least one major competitor which holds significant market share. To this end it is clear that if all of the total TCAD tools are to be made available to a wide range of manufacturing facilities interfaces to each of these packages must be developed. Fortunately, each of the software tools has been designed to interface with the commercial packages through a flat file ASCII format. Therefore, as long as any alternative commercial package also allows the import or export of data in a flat file ASCII format then a straight forward format conversion can take place.

7.3.2 Graphical User Interface

All three tools make use of user interactive UNIX control scripts to prompt and guide the user. This is an efficient and simple method by which to demonstrate the effectiveness of the software. However, the development of a GUI can not be ignored. Although there is little academic benefit to be gained from the introduction of a GUI front end to the software it would be a step towards consolidating the new elements of total TCAD with the old. Adding further options to the Calphurnia GUI, which forms the basis of the user interface for the original framework, has potential but this could really only serve as a launch pad for GUI versions of the control scripts as it can already be used to collate simulation results. Hence, individual GUIs would need to be developed to replace the FASTT and CASTT experimental control scripts. The MASTT dialog would benefit little from a GUI unless ftp software was to also be included. Such a venture would only be worthwhile should the software be taken up on a larger scale than at present. Additionally further development in this direction would be rendered immaterial should the tools be commercialised by one of the industrial partners involved in the project, as was the case with the original total TCAD framework.

7.4 Summary

To conclude, the three software tools developed during the course of the work have transformed the original total TCAD framework from a set of process and device technology development tools into a DFM package capable of analysing and forecasting the impact of any technology on the manufacturing environment. Ever increasing device and process complexities mean that the practical implications of a design choice can not be ignored if companies are to maximise their production efficiency and reduce their time to market. By bringing access to factory simulation and cost analysis into the framework coupled with ensuring the availability of data files the potential now exists to design and develop IC processes and devices with manufacturability in mind.

Appendix A
Published Papers

The following are papers written by the author associated with this thesis which have either been published, submitted or are to be submitted for publication:

V.K. Nilsen, A.J. Walton, D Wilson; "Incorporation of TCAD within an MES to help Optimise Manufacturing Efficiency", International Symposium on Semiconductor Manufacturing, pp. 95-98, 7-9th Oct 1998. *See figures A.1 to A.4.*

V.K. Nilsen, A.J. Walton; "Integration of TCAD and Factory Simulation", PREP'99, Manchester, UK, pp. 395-398, Jan 5-7 1999.

V.K. Nilsen, A.J. Walton; "Integration of Factory Simulation with TCAD Process and Device Simulation within a Total TCAD approach to DFM", International Symposium on Microelectronic Manufacturing Technologies, SPIE, 3742, pp. 186-196, May 19-21 1999. *See figures A.5 to A.15.*

V.K. Nilsen, A.J. Walton; "Automated Cost of Ownership Analysis for Process Development", International Symposium on Microelectronic Manufacturing Technologies, SPIE, 3742, pp. 112-120, May 19-21 1999. *See figures A.16 to A.24.*

V.K. Nilsen, A.J. Walton, J. Donnelly, G. Horsburgh, R. Childs; "Implementation of a TCAD based System to Aid Process Transfer", International Workshop on Statistical Metrology, pp. 54-57, June 12, 1999. *See figures A.25 to A.28.*

V.K. Nilsen, A.J. Walton, "Accurate Prediction of IC Manufacturing Distributions using Improved Response Surface Fitting", Accepted for publication at the International Workshop on Statistical Metrology, 2000. *See figures A.29 to A.32.*

V.K. Nilsen, K.M. Findlater, A.J. Walton, J. Donnelly, G. Horsburgh, R. Childs, J. McGinty and M. Fallon, "A Methodology for Efficient Process Transfer Using TCAD", Under review

for publication in the IEEE Trans Semiconductor Manufacturing, 2000.

Incorporation of TCAD within a MES to help optimize manufacturing efficiency

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Abstract - This paper describes the integration of TCAD and MES software tools to help optimize manufacturing efficiency as an integral part of a DFM (Design for Manufacturability) strategy. Automated creation of up-to-date TCAD models facilitates accurate analysis of manufacturing issues and process or product development. The paper describes the design and operation of the MASTT (MAnufacturing execution System in Total TCAD) software which integrates two commercially available software packages - TWB and Promis. An example is used to illustrate its use in identifying corrective action for misprocessed wafers.

1. Introduction

Over recent years TCAD (Technology Computer Aided Design) has become a widely used tool within the field of process design and development. Unfortunately, it is too often the case that once a device is released to full production, subsequent modifications to the process mean that the development TCAD data files may no longer provide an accurate model.

As a result, when TCAD would be beneficial to either help sustain or improve processes, accurate TCAD data for the process is simply not available. Therefore, the TCAD code must always be updated before accurate simulations can be performed. This is an error prone and tedious procedure as the complete TCAD process flow must be thoroughly checked, typically taking a couple of days. As a result this is seldom done and the use of TCAD as an analysis tool for continued process development is therefore limited.

This paper presents the MASTT (MAnufacturing execution System in Total TCAD) software developed to bridge the gap between development and production. MASTT facilitates the analysis of any on-line process development, through the automated creation of TCAD process models directly from the MES (Manufacturing Execution System) database.

1.1 TCAD software

TCAD software enables engineers to simulate the effect of IC processes on the electrical characteristics of devices without the need to embark on expensive and time consuming wafer fabrication. In recent years it has been demonstrated that the time required to complete the TCAD analysis can be further reduced by employing Design Of Experiment (DOE) techniques [1,2]. This Total TCAD (T^2CAD) approach has the potential to reduce development or analysis time further by both reducing the number of simulations while at the same time enabling them to be performed in parallel [3].

TCAD frameworks are now available which utilise graphical user interfaces, enabling less experienced users to perform simulations and analysis of both processes and devices. These "virtual wafer fabs" such as TMA's WorkBench (TWB) [4] shown in figure 1 provide a graphical representation of the wafer flow, making operation intuitive to those familiar with processing.

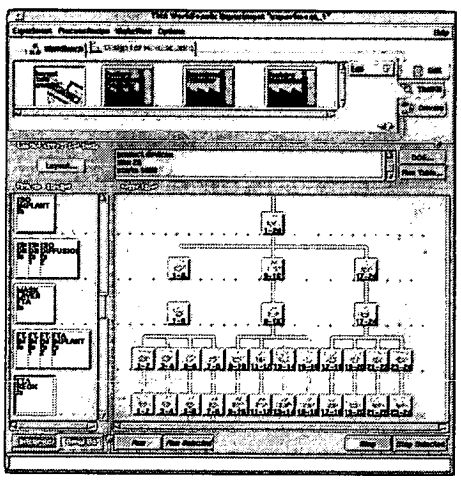

Figure 1. Alternative wafer flows for a number of process splits as presented in TWB

This makes it an ideal tool to use during the development of an existing process, or as analysis tool to aid the understanding of the process in general. It is also suited to investigating what may have happened to wafers during processing and can aid identification of corrective action in the event of misprocessing.

1.2 MES software

A MES [5] lies at the heart of production support for every modern fab. In essence, it aids the day-to-day running of the fab, monitoring processing and equipment and provides a means by which to access the information collected. The core elements of a MES are illustrated in figure 2.

MESs, such as Promis, are essential in today's competitive market place. They provide a utility which can be used not only to assess and improve production but one which can be utilised by external software tools which require the

Figure A.1: *Reprint of paper presented at ISSM 1999, page 1.*

information contained within the database. It is the ability to easily extract specific information for individual lots that makes it possible to encompass the MES database within a T²CAD environment.

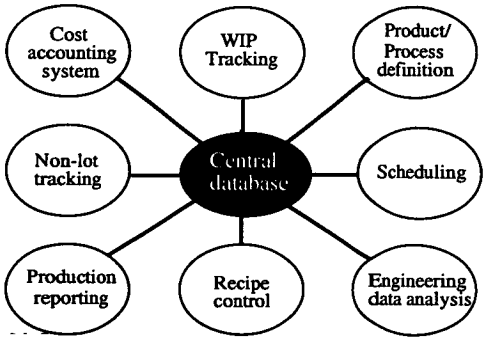

Figure 2. Core elements of a MES

2. Objectives

The key aim in the development of MASTT was to maximise ease of use. To encourage the use of MASTT it should only require minimal additional training for TCAD or process engineers. To achieve these goals the system must be as automated as possible and provide adequate instructions for those steps that can not be automated. This also reduces the potential for data handling errors, ensuring the validity of the TCAD models created.

T²CAD can be used to analyse many processing situations and as such a number of options must be catered for with MASTT. The most basic level of analysis is that of TCAD process simulation. This allows an engineer to investigate whether or not processing specifications (e.g. oxide thickness and sheet resistivity) have been, or will be, met during the processing.

However, in most circumstances an engineer will be more concerned as to whether or not the device will meet the parametric test criteria. In order to simulate this aspect the process model must be augmented by the addition of device modelling data. This must also be included within the TCAD simulation file. In order to preserve a single data source for the TCAD model, this information should also be stored within the MES database.

The MES database also contains information regarding the equipment used to process any given lot. Including this within the created TCAD model would have two significant benefits. Firstly it would provide a more detailed description of the processing conditions, providing a greater understanding of the practical issues involved in the processing. Secondly it would allow the creation of factory simulation models through the use of the FASTT (Factory Simulation in Total Tcad) software [7]. This would allow manufacturing issues such as costings, throughput and cycle time to be considered in any analysis when considering a process change. This becomes especially important if a proposed change to the process is to become permanent, as the implications to the whole facility must be considered due the potential impact upon other product lines.

3. Implementation

3.1 Storing TCAD data within Promis

The first stage in implementing the MASTT software is the inclusion of the TCAD template files within the Promis MES database. The TCAD template is stored as ASCII text files associated with the individual recipes that make up the process flow. Storing the TCAD template files at a recipe level ensures that any change to any part of a process will be up-dated in other processes that use the same recipe.

It is possible to incorporate parameters within a recipe as variables that are either entered by the operator or passed on from a previous processing step. If any of these parameters are relevant to the TCAD code they should be included within the stored TCAD template files. This allows modelling of the actual process settings used, by substitution of the actual values for the parameters when the TCAD process flow is formed.

3.2 Extraction of data from Promis

The extraction of the requisite data from the Promis database is controlled by a UNIX shell script, prompting the user to enter required information and indicating any necessary action. The user is prompted for the lot and Product ID. Once this information is received Promis scripts are automatically created to extract the required information from the data base. These are then run and the resultant files transferred back to the users account.

3.3 Forming the TCAD process flow

The lot dependent files extracted from Promis are used in conjunction with the extracted TCAD template to provide the inputs to a series of Perl programs. These combine the data to build a single TCAD flow file, which can then be imported into TWB. This is a 4 stage process:

Stage 1. The extracted process flow file is parsed. For each recipe the following information is extracted and written to a file in the FS (Factory Simulation) directory in the following format:

```
$step RECIPE_NAME_FS
comment fs operation RECIPE_NAME
comment fs time TIME_TAKEN_AT_RECIPE
comment fs wstat EQUIPMENT_GROUP_USED
comment fs equipment EQUIPMENT_NAME
```

Figure A.2: *Reprint of paper presented at ISSM 1999, page 2.*

Stage 2. The parameter names and values for each recipe are extracted from the process flow file. These are written to a file for each recipe in the PARAMS directory:

```
$dose 1e14
$energy 100
$species phosph
$tilt 0
$rotation 45
```

Stage 3. For each recipe that a TCAD data template exists the corresponding parameter file is parsed and the parameter names replaced by the extracted values, as illustrated below: TCAD data template:

```
implant $species dose=$dose energy=$energy
tilt=$tilt rotation=$rotation
```

after replacement this becomes:

```
implant phosph dose=1e14 energy=100 tilt=0
rotation=45
```

Stage 4. The individual recipe files are then combined in the order of the process flow. Any TCAD data for the recipe is written first, followed by the processing equipment details. The final process flow is grouped by the Promis stage definitions, giving a single file containing not only the complete TCAD flow, but also information on the equipment upon which it can be processed.

4. Applications

Implementing MASTT within a manufacturing environment has many potential uses. At the simplest level, the additional processing information required to enable creation of the TCAD models provides a detailed on-line process flow description. As this can be accessed at any point within the fab, through an MES terminal, it provides a valuable, "hands-on" resource for both aiding process understanding and training.

When MASTT is used to create a TCAD process model the possible analysis can be considered to fall into one of two categories, "Look ahead" or "What if".

4.1 "Look ahead"

"Look ahead" provides a facility whereby an engineer can use TCAD to simulate the effect of processing a lot to the end of line from any given point in the process. This is accomplished by extracting the partially completed process flow from the MES and combining this with previously extracted TCAD data for the same process.

By simulating the lot to the end of processing and deriving the final device parameters it may be possible to indicate whether or not continued processing of the lot is worthwhile. This decision can then be based upon analysis rather than subjective assessment as is currently common practice within many fabs.

Hence, the potential exists to significantly reduce production costs, considering not only the cost of processing wafers which are almost guaranteed to fail to meet specification but also allowing replacement wafers to be started at an earlier stage.

4.2 "What if"

Through the use of "look ahead" it may be apparent that the lot will fail to meet the required specification if processing is continued until end of line. However, by providing the engineer with the processed TCAD steps it becomes possible to simulate the effect of altering the subsequent processing conditions.

This makes it possible to analyse what, if any, measures can be taken to rectify the effects of earlier processing. This can be further enhanced by the use of experimental design practices, e.g DOE, RSM, such as those now incorporated within TWB. These techniques, which form the backbone of Total TCAD reduce the number of simulation runs required to perform the analysis and simplify interpretation of the results. This allows informed corrective action to be taken rather than relying upon an engineers previous experience which is too often the case.

5. Example

In order to demonstrate the potential of integrating TCAD and MES software through the MASST interface a given scenario has been created and a potential case of misprocessing considered.

The process uses a double implant stage to set the threshold and punch through voltages (V_{th} and V_{pt} respectively) during the formation of the nMOS devices. Firstly there is an implant of boron, dose = $7x10^{11}$ atoms/cm^2, energy = 25 keV, followed by another boron implant, dose = $7x10^{11}$ atoms cm^{-2}, energy = 140 keV. However, the wafers are misprocessed, receiving a higher dose, $8x10^{11}$, during the initial implant.

The first question that must be asked is whether or not this will result in the wafers failing meet the parametric specifications? In order to answer this the information form the part processed wafers is extracted from the MES and the TCAD model imported into TWB. A model for a completed batch of wafers is also imported. The additional TCAD code required to simulate the misprocessed wafers to end of line is added from the completed wafer flow. The resultant parameters for both simulated flows are compared in table 1.

Table 1. Simulation parameters from correctly processed and misprocessed wafers.

Device Parameter	Correctly processed	Mis-processed
Threshold voltage (V_{th})	0.4745 V	0.517 V
Punch through voltage (V_{pt})	10.697 V	10.660 V

Figure A.3: *Reprint of paper presented at ISSM 1999, page 3.*

It is clear from the simulation results that the misprocessed wafers will fail to meet the parametric test specifications (V_{pt} >10V, 0.475 < V_{th} < 0.495V). So if the wafers are to be saved subsequent process steps must be altered. This can be achieved either through the alteration of existing recipes or by the introduction of a new recipe. The former provides the simplest option in this scenario. An adjustment to the second implant will leave the wafers back on the standard process flow after the corrective action.

In this example, to counter the effect of the additional dopant at the surface of the silicon the second implant can be adjusted to either push the peak concentration further into the silicon or reduce its concentration so that it has a lesser effect at the surface of the silicon. To determine the best combination of these possible solutions a DOE is performed. This is done using the built in experimental design features within TWB. The results from a 9 simulation run CCF (Box - Wilson cube) DOE, in the form of an RSM, are shown in figure 3.

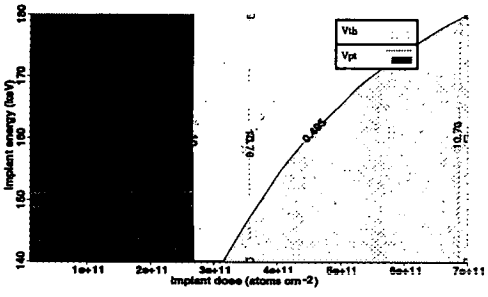

Figure 3. RSM: Phosphorus implant corrective action

A cubic model was fitted to the simulation results giving a fit with R-squared-adjusted figures of 0.99997 and 0.99993 for V_{pt} and V_{th} receptively. The shaded areas on the RSM represent the areas of V_{pt} and V_{th}, left and right receptively, which lie outwith specification. Hence, any combination of dose and energy settings in the remaining area will produce a device that will meet the parametric test specifications.

Two simulations have already been performed within this area during the DOE. Therefore, no more simulations are required to find a suitable corrective implant. Although the V_{th} is improved by using a 180 keV rather than the 160 keV implant it provides a solution closer to the original process flow and as such may be more desirable. Thus a potential corrective implant for this example is a boron implant of dose of $3.5x10^{11}$ atoms cm^{-2} at 160 keV. This gives a simulated V_{th} = 0.490 V and a V_{pt} = 10.760 V, suggesting that the wafers will pass parametric test.

The time taken to complete this type analysis is determined by the computational power available to the user. In this case the analysis was performed in approximately 12 hours, 80% of which was the time taken to perform the simulations.

6. Conclusion

This paper has discussed the roles of TCAD and MES within the semiconductor manufacturing environment. A method integrating the two through the use of the MASTT software has been presented. The MASTT interface facilitates the creation of up-to-date TCAD simulation files from data stored within the on-line MES database, this reduces the effort required to initiate analysis of day-to-day processing issues or continued process development once a process has been released to manufacture.

An example has been used to describe the role of the MASTT software within a Total TCAD framework. MASTT provides a means by which process engineers can access tools previously only used by designers and developers. This allows, as demonstrated, TCAD analysis to be easily performed within the production environment, without the need for extensive additional training.

7. Acknowledgments

The authors would like to acknowledge the contributions of the following organisations, without whom this research would not be possible: EPSRC (R/K98733) Avant! Corp., Promis Systems Corp., Manugistics Inc., Domain Solutions Corp., National Semiconductor UK, Motorola and Mitel Semiconductor.

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Figure A.4: *Reprint of paper presented at ISSM 1999, page 4.*

Integration of Factory Simulation with TCAD Process and Device Simulation within a Total TCAD approach to DFM

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ABSTRACT

This paper describes the integration of TCAD and factory simulation software tools to help facilitate their adoption as an integral part of a DFM (Design for Manufacturability) strategy. Automated exchange of data enables the impact on manufacturing operations to be more readily considered at an earlier stage during the process design procedure. The paper describes the design and operation of the FASTT (FActory Simulation in Total TCAD) software which integrates two commercially available simulation tools - TWB and ManSim/X. Two examples are used to illustrate its application within a DFM strategy.

Keywords: FASTT, Total TCAD, TCAD, Fcatory Simulation, DFM, ,

1. INTRODUCTION

The introduction of a new or improved process has the potential to significantly impact both cycle time and factory throughput. Hence, it is prudent to consider the possible effect on factory performance as close to the start of any new process development as possible. Typically, the feasibility of introducing a new process into a given fabrication facility is often only considered once significant effort has gone into the design and development of a process. This is partly because TCAD (Technology Computer Aided Design) engineers are often far removed from those concerned with factory operation. Additionally, the generation of data required for Factory Simulation (FS) software is time consuming and tedious. This being the case there is an obvious reluctance for engineers involved in technology developments to invest any significant effort into using FS to examine the effect a prototype process may have upon the manufacturing environment.

This paper gives a brief summary of both FS and TCAD and examines the issues involved in their integration. An implementation of the automated transfer of data between the two systems is described and some examples of its application are presented.

2. FACTORY SIMULATION

Factory simulation is an increasingly important element in manufacturing. Computer aided manufacturing (CAM) systems[1], such as Promis[2] and Workstream[3] have, for a number of years, provided the semiconductor industry with a means to both monitor and control the flow of product through a fabrication facility. However, they have little inherent predictive ability[4], although their integration with FS makes the investigation of what if scenarios possible.

In recent years, the increase in affordable computing power, together with the development of more powerful and easy to use FS software such as Manugistics' ManSim/X[5] has provided the capability to model the dynamic and stochastic nature of real life manufacturing. This provides a degree of precision previously unavailable with traditional static spreadsheet based systems, and has the has the ability to:

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Figure A.5: *Reprint of paper presented at SPIE 1999, page 1.*

- Identify production bottlenecks.
- Determine potential capacity.
- Provide equipment and personnel utilisation information.
- Cost production.

FS is one of the major tools available to help optimise the operation of a fabrication facility as it can identify potential changes to the existing production process that will help to meet manufacturing objectives. Given the investment required to keep pace with technology, this potential to optimise the production line operation is becoming increasingly important. Giving factory simulation software a more prominent role in the design equation can be considered an integral part of the DFM procedure. This is because it has the potential to save significant time and money by identifying potential bottlenecks and equipment investment issues well in advance of the introduction of new processes. These are important issues, especially in terms of reducing cycle time, which has a direct impact on both product cost and quality and hence is a target for the majority of semiconductor plants[4].

3. TCAD

The reduction in the time taken to develop the next generation process is an important goal in the introduction of a new technology. A key tool in achieving this objective is the use of TCAD software which enables engineers to simulate the effect of IC processes on the electrical characteristics of devices before embarking on expensive and time consuming wafer fabrication. In recent years it has been demonstrated that the time required to complete the TCAD analysis can be further reduced by employing Design Of Experiment (DOE) techniques[6,7,8]. This Total TCAD (T^2CAD) approach has the potential to reduce development time further by both reducing the number of simulations while at the same time enabling them to be performed in parallel[9].

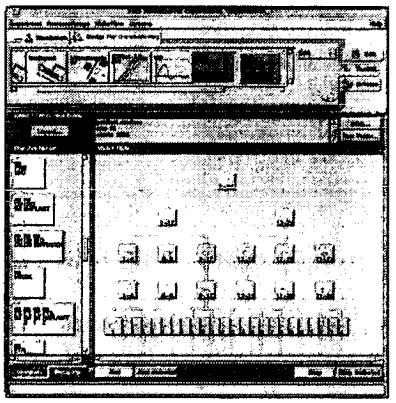

Figure 1: Alternative wafer flows for a number of process splits as presented in TWB

TCAD frameworks are now available which utilise GUIs, enabling less experienced users to take advantage of the capabilities of modern process and device simulators. These virtual wafer fabs such as Avant!'s WorkBench (TWB)[10] shown in figure 1 provide a graphical representation of the wafer flow. The information within each of the individual process modules can be easily edited as can the order and choice of modules within the process flow. This environment also enables users to easily select the appropriate simulator, as well as allowing the incorporation of external software tools, making them ideally suited to the integration of TCAD and FS. Examples of these external tools, including the FASTT software that has been incorporated into TWB as part of the work reported in this paper, are shown at the top of the TWB window (figure 1). If desired, these tools can be run by dragging a wafer from the process flow and dropping it over the tool icon.

Figure A.6: *Reprint of paper presented at SPIE 1999, page 2.*

4. INTEGRATING FACTORY SIMULATION AND TCAD

Several issues must be addressed in order to develop a data transfer method. They include, identification of the relevant data, the extraction of this data from TWB and the creation of a FS model within ManSim/X. These issues will now be examined and the approach used in the FASTT integration software described with the aid of examples.

4.1 RELEVANT DATA

The data contained within TCAD simulation files consists of process information together with items such as grid specifications and details of the mathematical models used to represent different processes. For integration purposes only the processing details and their sequence are relevant to a FS model. However, FS requires additional manufacturing information to be specified. This includes the equipment type, the actual pieces of equipment that are qualified for each process step and the time taken for each processing stage. Hence this information has been added to the TWB flow in the form of structured comments within the TCAD simulation data file, as shown in figure 2. Note that because timing information is already defined for diffusion and epitaxial processes within TCAD data files, this need not be included within the comment statements as required for other process steps.

```
Comment FS  operation     1234
Comment FS  description   ISO_IMP
Comment FS  time    60
Comment FS  wstat   IMPLANT_HIGH
Comment FS  equipment     IMP_01
Comment FS  equipment     IMP_02
Comment FS  equipment     IMP_03
implant boron  dose=5e15 energy=90 rp.eff
```

Figure 2: TCAD code for an implantation process step including FS comments.

4.2 EXTRACTING DATA FROM TWB

TWB uses an ASCII flat file format to store all the details of an experiment. In particular, this file includes the modules that define the process steps and the arrangement of these in terms of their order and any alternative process options. Additionally, alternative process splits may have been generated within a TWB experiment. Hence, each process flow must be considered individually with the arrangement of the modules determining the order in which the FS data is extracted from the TCAD files. For each process split the resulting output is written to single column text file and figure 3 gives an example of the information extracted from the data file presented in figure 2.

```
operation
1234
description
ISO_IMP
time
60
wstat
IMPLANT_HIGH
equipment
IMP_01
equipment
IMP_02
equipment
IMP_03
```

Figure 3: Single column FS data extracted from the TCAD code for the implantation process step given in Figure 2.

Figure A.7: *Reprint of paper presented at SPIE 1999, page 3.*

4.3 CONSTRUCTION THE MANSIM/X MODEL

Within ManSim/X the conventional method for creating a new FS model is through ManSim/X's GUI, which given the nature of many GUIs, can be a time consuming, laborious and error prone process[11]. Hence, this approach does not lend itself to the automation of the interface between TCAD and FS.

However, once data files of the format shown in figure 3 are available, one feasible method of transferring it into FS software is by writing directly to the model files. Unfortunately, with ManSim/X a number of fields are present in more than one file and the ordering of the information is both complex and critical to the model's functionality. As the format of these is subject to change with the release of new versions, it was decided that this approach was not suitable.

Fortunately, the FS software also includes a utility, ModelBuilder, that allows the construction of a basic model from ASCII files. These require information regarding the process flow, and products amongst other details and provide an ideal medium for transferring the relevant information from the TCAD files to ManSim/X. As an example, figure 4 shows an extract from the process flow file (PFLOW.CSV) for the process detailed in figures 2 and 3.

```
Process-1,IMPLANT_HIGH,60,,,1234,ISO_IMP,IMPLANT_HIGH,IMP_01,,,,
Process-1,,60,,,1234,ISO_IMP,IMPLANT_HIGH,IMP_02,,,,
Process-1,,60,,,1234,ISO_IMP,IMPLANT_HIGH,IMP_03,,,,
```

Figure 4: The ManSim/X's ModelBuilder file format required for the process flow file for an implantation process step.

4.4 TRANSFER SUMMARY

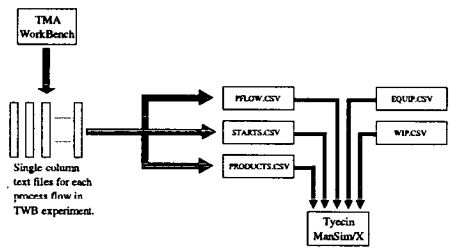

Figure 5: Data transfer flow from Avant! WorkBench to ManSim/X.

As previously discussed the procedure used to parse the TCAD file and extract the FS data is a two stage process. Firstly, a single column text file is created from the information extracted for each of the wafer flows present in the TWB process tree. Secondly, these files are translated, to create the required ManSim/X CSV files. This procedure is illustrated in figure 5.

The EQUIP.CSV file is determined by the facility's equipment set-up and hence independent from the extracted information. The WIP.CSV file is either left blank if modelling a zero initial inventory or extracted from the facility's CAM system. Once all five CSV files have been created the ModelBuilder utility can be used to create the model within ManSim/X. At this stage the CSV files can either be used directly or, if adding a new process to an existing fabrication facility, combined with other CSV files containing data from other processes. This along with multiple simulation runs may be simply controlled within a UNIX script environment.

Figure 6 shows the basic operation of the control script. The procedure relies upon a set of default settings: the ManSim/X model name, the start rate increment, the simulation length, the warm-up time, the number of process splits, and the maximum WIP increase. The final option is whether or not to combine the extracted model with an existing model. It is possible to define all of these factors prior to starting the simulations.

Figure A.8: *Reprint of paper presented at SPIE 1999, page 4.*

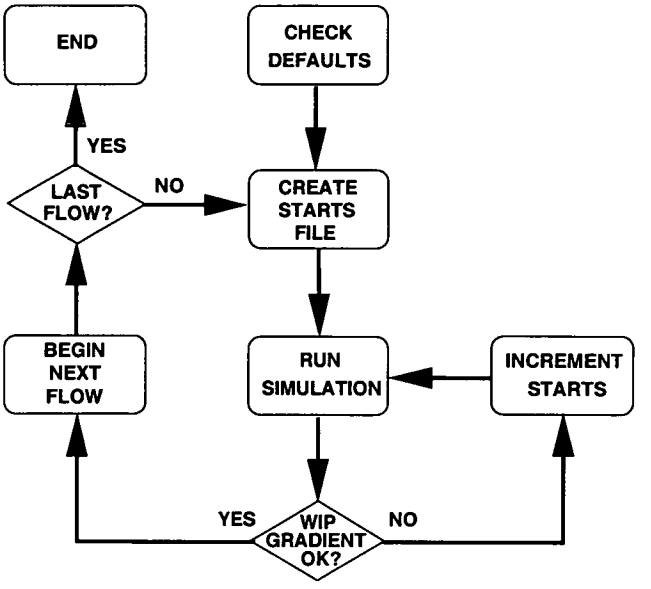

Figure 6: Simulation experiment shell script flow diagram.

The maximum WIP increase has a significant influence on the simulations run. By examining the resultant gradient of the WIP data an upper limit on it can be used to stop increasing the start levels and simulation of a particular model, and begin the simulation of the next model if applicable. This has the advantage that the once the starts have exceeded a realistic level the simulation process continues, without the need to pre-determine the maximum level of starts.

5. EXAMPLES OF THE APPLICATION OF FASTT

Two possible scenarios will be presented to demonstrate the automated transfer of information between the applications. Firstly, a comparison will be made between alternative versions of an existing process. Secondly, the introduction of a new process to an existing fabrication facility will be evaluated. Although FASTT allows for the extraction and comparison of many alternative processes, in this case relatively simple examples have been selected for the purpose of illustration.

A key requirement associated with efficient factory operation is that, after an initial start up period, the WIP (Work in Progress) should stabilise and remain at constant level as a function of time. For a line with no initial inventory this start up phase is indicated in area A in figure 7. This situation, where the factory operates with a constant level of WIP, only exists if the line is operating at or below capacity, as shown in the plots D-F in figure 7. A continually increasing WIP, as illustrated in plots B and C in figure 7, indicates that the line is being loaded in excess of the available capacity. In order to determine at what point capacity is reached it is necessary to increase the level of starts until capacity is exceeded, since it can not be determined from a constant WIP level whether the line is operating at or below capacity. Plot C in figure 7 shows the resultant WIP plot for a level of starts just beyond capacity. At the initial stages the WIP appears constant but as the simulation length increases the WIP begins to rise. It is this point that is often of most concern as, once the capacity of the factory has been exceeded, the manufacturing operation becomes less efficient.

Figure A.9: *Reprint of paper presented at SPIE 1999, page 5.*

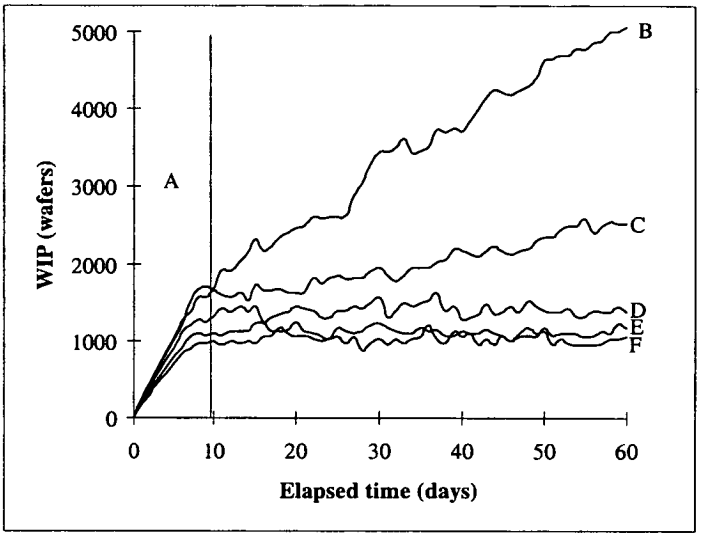

Figure 7: WIP vs. elapsed time comparison for increasing number of wafer starts.

5.1 ALTERATION TO AN EXISTING PROCESS

Many potential process improvements are procedural, such as when and where wafers should undergo cleaning, while others are technological. Examples of the latter might be a diffusion recipe change, or a change of implant dose or energy. The options are vast and their implications on manufacturing are varied. For example, small changes, such as an 5% increase in implant dose, which may make a significant difference to the operation of the device, may only result in a marginal increase in actual processing time. Hence, this would be unlikely to have an impact on production, unless the implantation equipment was already fully loaded.

This example considers the case where there is a desire to improve the dielectric integrity of an MOS structure. The proposition is to substitute an oxide with a more robust ONO (Oxide, Nitride, Oxide) dielectric. As the proposed modification involves a number of processing steps it is prudent to consider the implications on the manufacturing line before committing to full production. This will determine if the change is practicable or cost effective and if there will be a requirement for investment in new equipment. In the following example, cycle time and throughput will be used as metrics to determine the impact of the proposed process change.

The first step is to create the new ONO process flow within TWB by adapting the existing process. The next step is to use TCAD simulation to check that the required specifications are met. This results in two flows within TWB, the original process and the ONO process. As described in section 4, these TCAD data files must then be parsed to extract the information for the ManSim/X model. The control script can then used to set the initial starts, the start rate increment and the WIP gradient cut off level. After following the above procedure each process was then ramped up until capacity was exceeded.

Several output files are created during the simulation of the factory operation. Some contain information required by the controlling software to initiate the simulations and others record the results. In this example, files containing the cycle time and throughput data were automatically created and combined to produce a single output file for analysis.

Figure A.10: *Reprint of paper presented at SPIE 1999, page 6.*

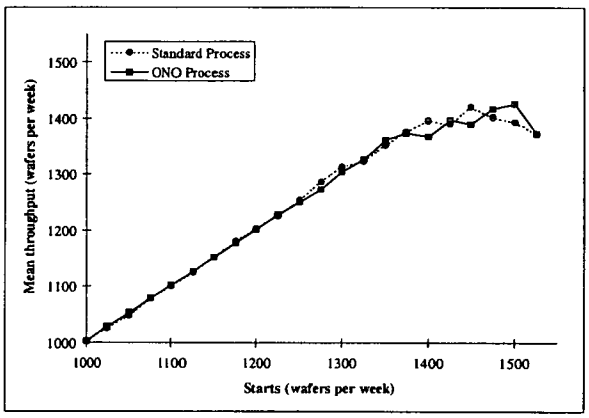

Figure 8: Throughput vs. wafer starts for the standard and ONO processes.

Figure 8 shows the throughput as a function of wafer starts for both processes. If the factory WIP is not increasing, then the wafer starts will be equal to the throughput. It can be observed that the throughput of the ONO process is indistinguishable from that of the standard process until the facility approaches capacity at approximately 1375 wafer starts per week and the trend becomes erratic due to bottlenecks occurring. As such, the proximity of the plots dictates that there is little that can be concluded from this metric alone.

Figure 9 compares the cycle time of the two processes as a function of wafer starts. It can be observed that the mean cycle time for both processes remains roughly constant until line capacity is reached at approximately 1375 wafers per week. On closer inspection it can be seen that the mean cycle time actually rises gradually as the number of starts increases and that the ONO process has a mean cycle time approximately 10 hours greater than the standard process. When capacity is reached the cycle time for both processes starts to rise significantly. The dramatic increase in cycle time occurs as a result of bottlenecks forming within the fabrication facility.

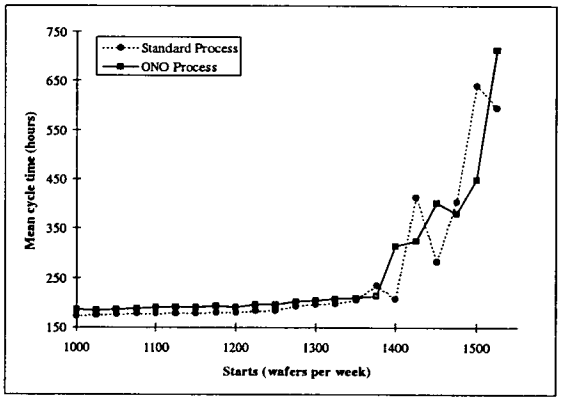

Figure 9: Mean cycle time vs. wafer starts for the standard and ONO processes.

Figure A.11: *Reprint of paper presented at SPIE 1999, page 7.*

It can be concluded that if the ONO process is to be introduced, the cycle time will increase by approximately 10 hours independent of the level of wafer starts and there will be a negligible effect on the throughput, assuming that the line is not operating beyond capacity.

5.2 ADDITION OF A NEW PROCESS

The ability to analyse the effect of introducing a new process into a fabrication line is essential for the identification of potential issues resulting from a change of product mix. This situation is illustrated in the following example where the start rates of the other products within the fabrication facility have been set at arbitrary, but realistic levels. This models the situation when it is planned to introduce a new technology and capacity analysis will be used to aid the selection of the specific site and also identify potential equipment bottlenecks.

This example demonstrates the effect that a given equipment set has on the fabrication facility's capacity. More importantly it demonstrates how the automated link between TCAD and FS can be used to provide early identification of potential problems related to production. These can then be addressed in a timely manner as part of the DFM process.

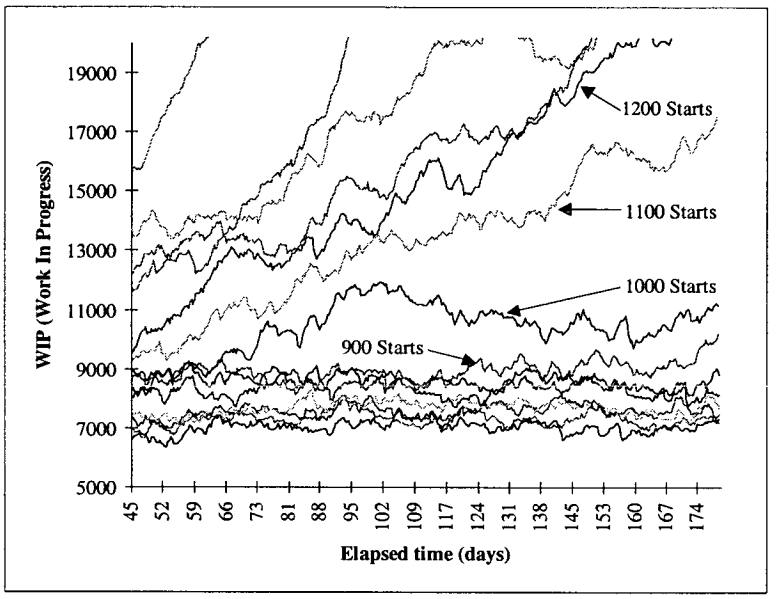

Figure 10: Initial WIP vs. elapsed time for a range of wafer starts.

As before the process conditions are first determined using TCAD and this data then used to automatically create the data required by the FS software. The factory simulations were then run as in the first example, but in this case the factory is already loaded with WIP to model the introduction of a new process. Figure 10 shows the WIP for these initial simulations, for different start rates. From these results it can be deduced that a start rate of 900 wafers per week is possible without reaching the facility's capacity. However at 1000 wafers per week the WIP starts to increase indicating the capacity has been exceeded.

Figure A.12: *Reprint of paper presented at SPIE 1999, page 8.*

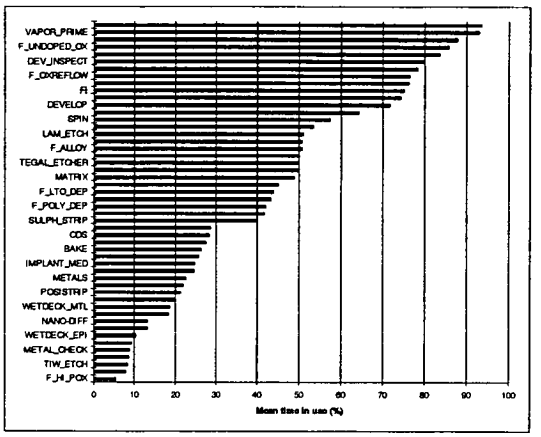

Figure 11: Mean equipment utilisation figures for simulations shown in figure 10.

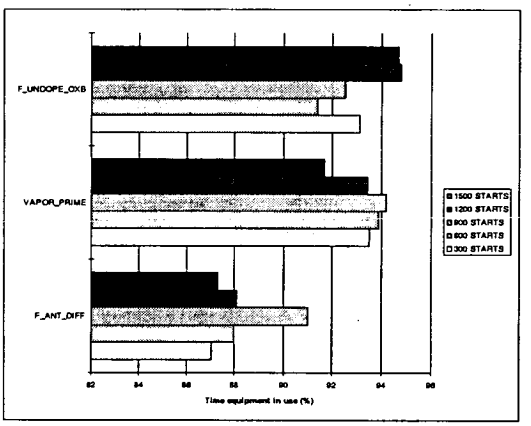

Figure 12: Specific equipment utilisation figures for a subset of the simulations shown in figure 10.

The mean equipment utilisation results for each simulation shown in figure 10 are illustrated in figure 11, highlighting the most heavily loaded items that are the most likely source of bottlenecks. Figure 12 clarifies the loading of the three most heavily used pieces of equipment for different numbers of wafers starts. The reduction of loading as the number of wafers starts increases indicates that other items of equipment are also becoming bottlenecks.

To investigate the possible benefits, an extra piece of equipment was added to the model for each of the two most heavily loaded work stations identified in figure 12. The simulations were then re-run and figure 13 shows the resulting WIP. It can be observed that a start rate of 1200 wafers per week is now possible with 1300 wafers per week exceeding capacity. Thus, the addition of two pieces of equipment has increased the factory capacity for the new process by approximately a third.

Figure A.13: *Reprint of paper presented at SPIE 1999, page 9.*

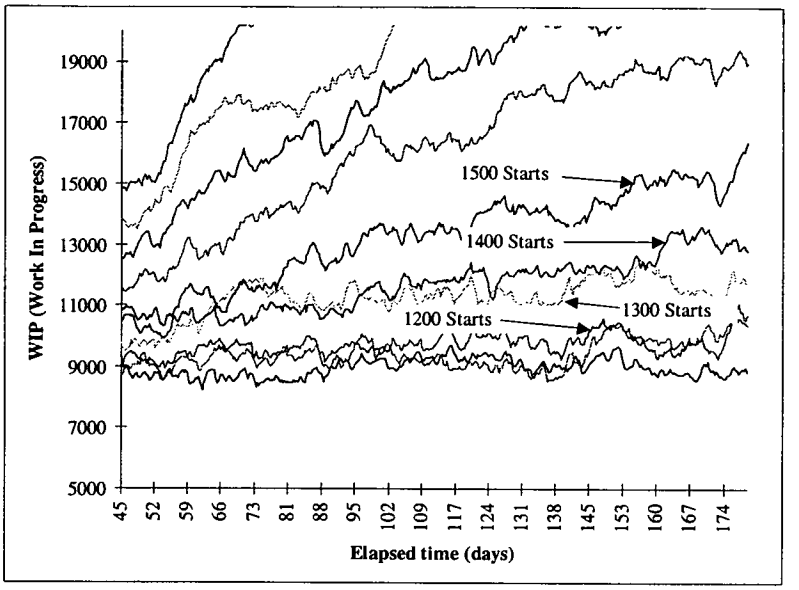

Figure 13: Secondary WIP vs. elapsed time for a range of wafer starts.

6. CONCLUSIONS

Factory simulation and TCAD play important roles within a DFM strategy. Traditionally they are often seen and used as independent tools within the overall design of a process. However, there are many benefits to be gained by integrating the two, ensuring that FS is no longer need only be considered once a process has been fully defined at the TCAD stage. By providing an automated data transfer between the utilities the gap between design and manufacturing can be bridged allowing easier analysis of manufacturing issues at a significantly earlier stage in process design. This has the potential to reduce time to manufacture and hence to market of new or improved devices enabling process development to take place without resulting in unforeseen manufacturing issues.

This paper has discussed the roles of FS, TCAD and their integration within a DFM strategy and a method of integrating FS and TCAD software to achieve this has been presented. The FASTT interface software extracts the relevant data from the TCAD files and builds the process model within the FS software. This allows factory simulations to be run and the outcomes to be taken into account during future process revisions. Two examples have been used to describe the operation of the software and indicate possible uses within a DFM strategy. These have demonstrated the effect that changing the equipment set has upon potential process capacity and the impact that a minor alteration to an existing process has on key metrics. The earlier these issues can be identified in the design cycle the better it is for the design team who can then either modify the process or use the increased lead time to implement changes to a fabrication facility.

7. ACKNOWLEDGEMENTS

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Figure A.14: *Reprint of paper presented at SPIE 1999, page 10.*

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Figure A.15: *Reprint of paper presented at SPIE 1999, page 11.*

Automated Cost of Ownership Analysis for Process Development

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Abstract

This paper describes how costings analysis can be incorporated into a framework for process development. It describes how Cost of Ownership (COO) can be calculated from the information stored within existing process development tools through the use of CASTT (Cost AnalysiS in Total TCAD). It provides a method by which manufacturing costs can be forecast and alternative processing options can be compared. The existing elements of Total TCAD framework are described, an outline of the CASTT software is then given and examples are used to illustrate its potential.

Keywords: CASTT, Total TCAD, TCAD, COO, costings, ownership, RSM, DFM.

1. INTRODUCTION

The cost of manufacturing a wafer is seldom considered by the technology development team during the development of a new process. However, with manufacturing costs becoming increasingly important in today's competitive market it is an issue that should be addressed. It is common place to cost a process once a design has been finalised but this is too late to be used to reduce manufacturing costs through design choices. Adoption of a method by which costs can be compared for alternative process options allows costings to be routinely considered during the development process.

As part of an overall DFM (Design For Manufacturability) strategy this paper presents CASTT, a software application which incorporates costings analysis into a Total TCAD framework. This paper describes the current T^{2}CAD framework[1] and its individual elements and CASTT's inclusion into this framework will be outlined and its operation and potential uses illustrated by examples.

2. T^{2}CAD - TOTAL TCAD

The Total TCAD (T^{2}CAD) framework integrates TCAD software tools into a structured environment as illustrated in figure 1. This reduces the time it takes to perform TCAD analysis on existing process flows and enables the forecasting of manufacturing issues during process development. The addition of costings details to this suite of software tools adds another dimension to the information available during process development thereby strengthening T^{2}CAD's role in a DFM strategy.

The following sections provide an overview of the elements currently incorporated into T^{2}CAD. Firstly the core element of TCAD is discussed with particular reference to virtual wafer fab frameworks. Design of experiment (DOE) and response surface methodology (RSM) techniques are then discussed as they provide the basis for defining and analysing TCAD experiments. Together these elements provide a system capable of driving TCAD analysis for process development. However, in order to address manufacturing issue during process development, Total TCAD has been expanded through the inclusion of manufacturing execution systems (MES) and factory simulation (FS). Incorporating MES software into the framework ensures TCAD analysis work can be carried out on up-to-date TCAD files through the use of the MASTT software[2]. The creation factory simulation models using FASTT[3] enables issues such as cycle time and throughput to be considered during process development. These two elements provide much of the information

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Figure A.16: *Reprint of paper presented at SPIE 1999, page 1.*

required to include of cost of ownership analysis into the T²CAD framework, adding another dimension to the development process.

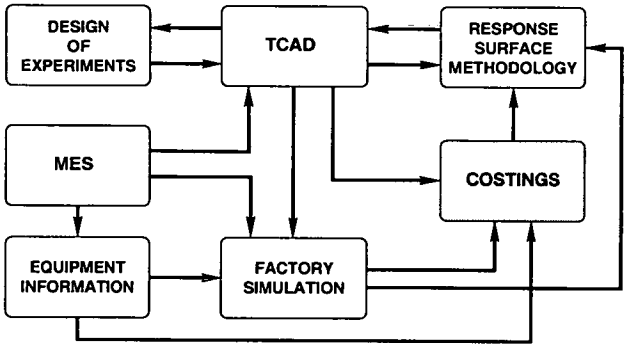

Figure 1: Total TCAD component relationships

2.1 TCAD - TECHNOLOGY COMPUTER AIDED DESIGN

TCAD (Technology Computer Aided Design) is the term given to the area of computer simulation and modelling related to the design, development and manufacture of integrated circuits. In particular, TCAD enables the simulation of semiconductor devices as well as the processes which are used to fabricate them. As the complexity of IC designs and processes increases so does the benefit of using TCAD for their development. The high cost of running experimental wafers (both in time as well as materials) has ensured that both hardware and software costs required for TCAD can be justified. However, using TCAD still takes a considerable time, not only in developing the simulation data files but also in their calibration.

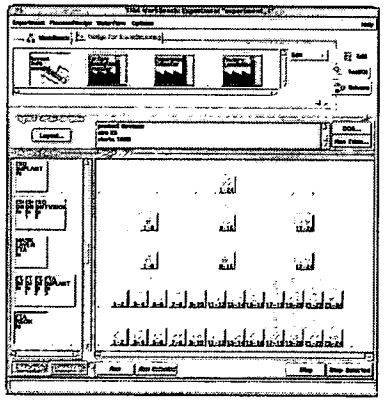

Figure 2: Alternative wafer flows for a number of process splits as presented in TWB

Figure A.17: *Reprint of paper presented at SPIE 1999, page 2.*

Virtual wafer fabs[4], such as Avant!'s TWB (Taurus Work Bench)[5] shown in figure 2, are designed to be more intuitive in their operation than conventional TCAD software. They provide an easy to use interface which draws on the user's existing processing knowledge. They also offer a high degree of flexibility by integrating all of the available TCAD packages as well as making Design of Experiment techniques readily available. These frameworks aid the efficient running of the simulations on the available resources and reduces the data storage required through the use of common simulation results. As such, it is this integrated system that forms the cornerstone of the Total TCAD framework.

2.2 DOE AND RSM- DESIGN OF EXPERIMENTS AND RESPONSE SURFACE METHODOLOGY

The fabrication of a semiconductor device is a complex procedure involving many, often repeated, individual process steps. Within each of these steps there are numerous factors governing the outcome including the processing equipment which is prone to variation. Hence, attempting to optimise any given process step can be time consuming especially as possible interactions between factors must be considered. In order to ensure successful optimisation and gain an understanding of any interactions occurring a structured approach is required. Design of Experiments (DOE)[6] methodology together with RSM (Response Surface Methodology)[7] is one such approach and is particularly suited to TCAD.

DOE techniques are required because if more than one control factor is present there is not always a direct relationship between individual factors and any observed responses. This means that altering one factor at a time and examining a given response is unlikely to fully explain what is actually happening. If interactions are present it would be necessary to test all possible combinations of factors. This is not a viable proposition for all semiconductor processes, simply because of the large number of control factors involved.

The general procedure used to identify response surface models to a process has several stages: All the control factors and responses of interest must be identified. If there are more than four control factors then an initial screening must be performed to reduce the number. The screening process eliminates some of the least important factors, allowing the interactions between the most influential factors to be examined in more detail. Once the control factors of interest have been determined an experiment to fit response surfaces must be designed. This is usually performed using a DOE software package (e.g. RS/1[8], Calphurnia[9], TWB[5]), allowing the user to select the design that most meets their requirements, usually in terms of the number of runs required. The experiment is then performed (simulated) using TCAD. On completion of the simulations polynomial models are fitted to the results, using appropriate software (e.g. RS/1[8], Calphurnia[10], TWB[5]),

After the appropriate model has been fitted the response surfaces can be examined. RSM contour plots provide a useful tool for interpreting the effect on a number of responses when two or more control factors are varied. Figures 3 and 4 illustrate this type of analysis by highlighting the combinations of factor settings which meet given criteria. Figures 3 and 4 show a single contour for each of the responses, representing the specification limits (gamma (Gm), punch through voltage (Vpt), sheet resistance (Rsd) and peak electric field (Epeak)). In figure 3 the contours represent the responses from the process target values, the responses to the factors without any process variation taken into account. Figure 4 shows the response surfaces including process variation. This is obtained by including the distribution of the equipment settings within the model. This gives a robust solution to the problem, i.e. one that is independent of the variations in processing. It is this structured approach to identifying response surfaces that has resulted in the inclusion of DOE and RSM features within today's virtual wafer fabs.

2.3 MES - Manufacturing Execution System

A MES (Manufacturing Execution System)[11] lies at the heart of most modern large scale production facilities and are an essential aid to improve manufacturing efficiency. In particular, the complexity of semiconductor manufacturing means that the use of an MES is a key element to ensure the successful operation of the fab. In essence an MES aids the day-to-day running of the fab, monitoring the progress of wafers through the fab, equipment status and providing a means by which the information collected can be accessed. There are a number of MES such as Promis[12] which have been developed to meet the requirements of the semiconductor industry[13] and their core elements are illustrated in figure 5

Figure A.18: *Reprint of paper presented at SPIE 1999, page 3.*

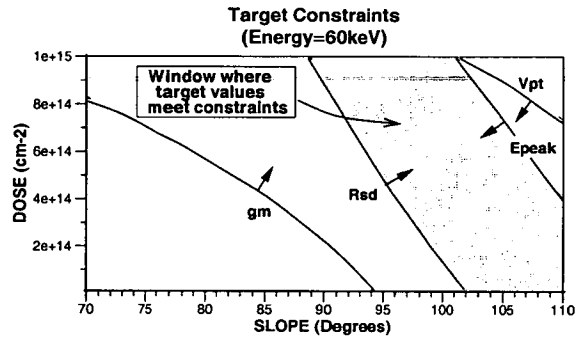

Figure 3: Response surfaces plotted as a function of implant dose and side wall slope for a fixed implant energy, shaded are indicates area where specifications are met

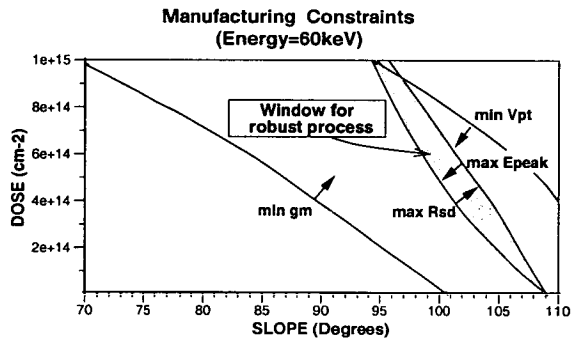

Figure 4: Response surfaces plotted as a function of implant dose and side wall slope for a fixed implant energy, shaded areas indicates area where the process is robust to expected manufacturing variations.

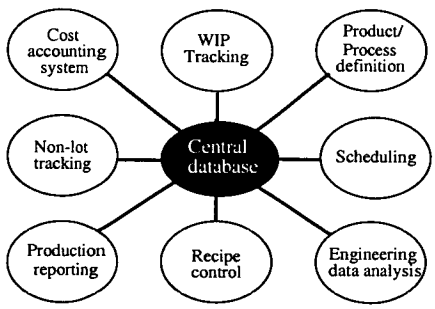

Figure 5: Core elements of a semiconductor MES

Figure A.19: *Reprint of paper presented at SPIE 1999, page 4.*

The information contained within the database is of prime importance when the MES is considered with the other elements of T²CAD. The database contains the information needed to define the processes, products and most of the equipment information. A variety of user interfaces are available to access or enter this data: simple terminals, bar code readers and more recently graphical interfaces through Motif and Windows.

It is this accessibility to the stored data that enables an MES be used to ensure that up-to-date TCAD process flows are always available for analysis. Since the MES is used to control wafer processing, the MES records any process changes. By storing the TCAD data on the MES and ensuring that it is updated when any process step is changed a system such as MASTT can be used to automatically create a TCAD process flow from the latest information. This system can also be used to provide additional information from the MES not usually incorporated into a TCAD process flow, such as the equipment details, which can be used to create factory simulation models and provide much of the information required for costings analysis.

2.4 FS - FACTORY SIMULATION

FS (Factory simulation) is an increasingly important element in manufacturing and particularly so in the semiconductor industry. Although an MES provides the essential elements required to run a fab they can not be used predict forthcoming events[14], however, FS provides this capability. FS software such as Manugistics' ManSim/X[15] which perform dynamic and stochastic modelling of semiconductor manufacturing provides a degree of precision previously unavailable with traditional static spreadsheet based systems. They have the ability to:

- Identify production bottlenecks
- Determine potential capacity
- Provide equipment and personnel utilisation information
- Cost production

Given the investment required to keep pace with technology, this potential to optimise the production line operation is becoming increasingly important. Incorporating factory simulation into the Total TCAD framework ensures that these issue can be considered at a much earlier stage than was previously possible. This has the potential to save significant resources by identifying potential bottlenecks and equipment investment issues well in advance of the introduction of new processes. These are important issues, especially in terms of reducing cycle time, which has a direct impact on both product cost and quality and hence is a target for the majority of semiconductor plants[14]. The analysis of manufacturing issues also plays an important role in addressing costing issues as FS results for processes not yet in production can be used to identify information required for cost of ownership calculations. For example, potential throughput of the fab must be identified to ensure that costs are not based an unrealistic number of wafer starts.

3. INTEGRATING COST OF OWNERSHIP ANALYSIS AND TCAD

This section describes the main aspects of the CASTT system, the cost of ownership calculation, the sources for the information required by the calculation and finally the general operation of the software.

3.1 COST OF OWNERSHIP CALCULATION

COO model templates are available from Sematech as a spreadsheet. This format provides an easy to use interface and allows the generation of a number of reports. However, this is not a convenient format for incorporation into the T²CAD framework as it requires manual intervention. To this end the Sematech spreadsheet has been translated into a c program, to enable the model to be integrated with the other systems.

Figure A.20: *Reprint of paper presented at SPIE 1999, page 5.*

3.2 DATA SOURCES

In order to provide the information for the COO calculations several data sources are required. Much of the data defines the fixed costs of the equipment used, for example the initial purchase price, cost of shipping and installation. Clearly these details are specific to individual pieces of equipment and as such are unavailable from any data sources within the total TCAD framework. This data is used to form the basic COO model. Manufacturing information such as MTBF (Mean Time Before Failure) which must be added to the basic model is available from the MES or factory simulation models. This leaves one key element to complete the COO model, the throughput of the equipment at full capacity. For much equipment (e.g. inspection and measurement equipment) this will remain unaffected as a result of changes to the process. However, for many of the process steps simulated using TCAD a change in the processing conditions has the potential to alter the throughput and hence the COO model. CASTT utilises this and uses it to complete the COO model.

3.3 CALCULATING COO

The data contained within TCAD simulation file is extracted to provide a single ASCII text file for each process option present. This file contains the:

- lot size
- number of starts per week
- order of the process steps
- processing time taken for each step
- type of equipment used for each step

For each process step in turn the lot size, starts and processing time are used to augment the information within the basic COO model and the COO calculation performed. This is repeated for each step and the overall cost of the wafer for the process returned. In order to reduce the analysis time for process comparisons, the process step identifier, the operation number can be used to define the first and/or last process step to be included in the calculation. The calculation procedure is summarised in figure 6.

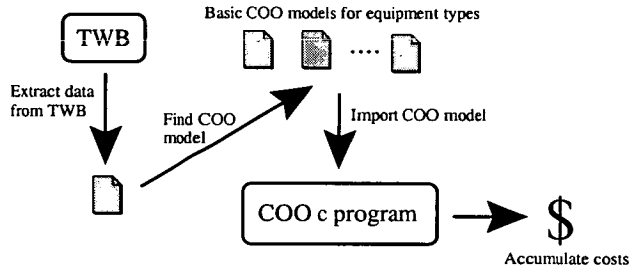

Figure 6: COO calculation summary

4. EXAMPLES OF THE APPLICATION OF CASTT

CASTT's basic operation returns a wafer cost for a given process flow, assuming that all of the COO models for the individual processing steps are available. Enabling the forecasting the cost of a process at an earlier stage during the development than is currently common place. However, CASTT can also be used to compare alternative processing options. Two simple examples of CASTT being used in this role are presented, to illustrate the potential of the system.

Figure A.21: *Reprint of paper presented at SPIE 1999, page 6.*

4.1 EXAMPLE 1

The first example considers the optimisation of process steps used to form the base region of a bipolar process. For simplicity only two control factors, the base implant dose and the drive time, and two responses, the sheet resistance (R_s) and the junction depth (X_j) have been considered using DOE techniques with TCAD. Figure 7 shows the response surfaces for R_s and X_j as a function of base implant dose and base drive time. The shading highlights the areas that fall outwith the given response specifications ($130 < R_s < 150\ \Omega/\square$ and $3.9 < X_j < 4.1\ \mu m$). From this it is clear that a number of potential solutions exist.

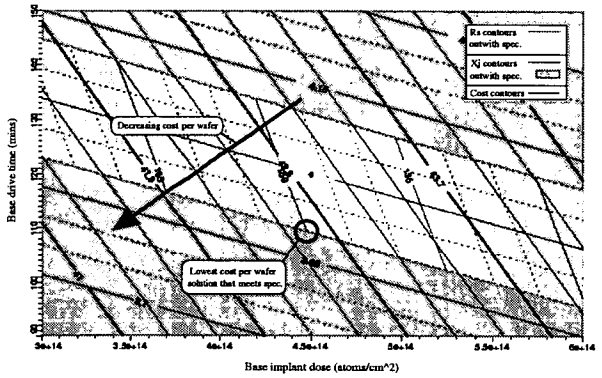

Figure 7: Response surfaces for R_s, X_j and cost plotted as a function of base implant dose and base drive time, shading indicates areas outwith spec, the direction of decreasing cost is shown by the arrow and t he point of the lowest cost solution is circled.

Cost analysis can be used to provide another metric by which to evaluate the options. It is clear that the dose and drive time should be minimised, since the time taken to perform the implant is governed to some extent by the dose, as this will maximise the throughput of the equipment. However, it is not known which of the two factors will have the greater effect of the cost. CASTT can be used to identify the wafer costs of the individual process steps by using the comparison limits option (which allows the user to specify the beginning and end of the cost calculation). The costs can then be summed for each of process combinations used in the TCAD experiment and the response surface plotted as with R_s and X_j. The results of these calculations are also plotted as a response surface in figure 7, with the direction of decreasing wafer cost indicated by the arrow and the point of the optimum solution (a dose of 4.47×10^{14} atoms/cm^2 and a drive time of 109.5 mins) circled.

4.2 EXAMPLE 2

In this example CASTT is used to compare two alternative processes to form a capacitor dielectric[3]. The existing process uses a grown oxide and the proposed an ONO (oxide Nitride Oxide). The ONO process has three stages: a grown oxide layer, a deposited nitride layer and finally a deposited oxide layer. The processes must be compared in terms of cost to determine whether or not the change (which has been identified in order to increase yield and reliability) can be justified.

In order to reduce the time of the calculation the comparison limits within CASTT are used,. The process details are extracted from TWB and the costs calculated using CASTT. The. The results shown in figure 8 show the increase in processing costs for the same range of start levels that were used during the throughput and cycle time analysis (which highlighted a maximum capacity of the process of around 1400 wafer starts per week).

Figure A.22: *Reprint of paper presented at SPIE 1999, page 7.*

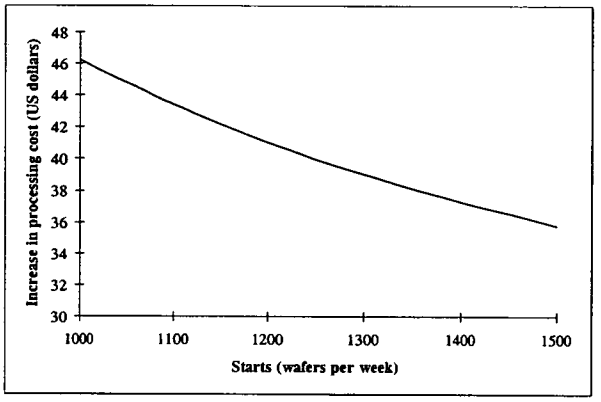

Figure 8: Increase in cost per wafer using the ONO rather than the existing process vs. wafer starts.

The downward trend of the cost increase as the start rate rises is due to the initial costs of the equipment being spread over a greater number of wafers. The of whether or not to implement the change will require the assessment of the benefit of the technological change to product yield and quality relative to the increased production cost for the given number of starts.

5. CONCLUSION

The use of Total TCAD as part of an overall DFM strategy is essential for identifying robust design and examining manufacturing issues prior to their implementation. This paper has given an overview of the existing elements of the Total TCAD framework and described how the CASTT software has been used to incorporate COO analysis into it. Incorporating COO analysis into the framework makes it possible to consider economic issues at a much earlier stage in the development of a process than was previously common place. CASTT makes cost calculations a quick and simple procedure, which with minimal effect provides the development team costings information throughout the development of a new process. The operation of CASTT has been outlined and its potential for use in process comparison demonstrated with the aid of examples.

6. ACKNOWLEDGEMENTS

The authors would like to acknowledge the contributions of the following organisations, without whom this research would not be possible: EPSRC (R/K98733) Avant! Corp., Promis Systems Corp., Manugistics Inc., Domain Solutions Corp., National Semiconductor UK, Motorola and Mitel Semiconductor.

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Figure A.24: *Reprint of paper presented at SPIE 1999, page 9.*

IMPLEMENTATION OF A TCAD BASED SYSTEM TO AID PROCESS TRANSFER

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ABSTRACT

This paper describes a methodology for using TCAD as an aid to process transfer. The methodology is based on the use of a semi-automated system developed to reduce the effort required by the user in developing the TCAD code, thereby reducing the time taken to implement a process transfer. The issues involved in process transfer are considered, as is the role that TCAD can play in the procedure. The operation of the system is outlined and an example of its application is used to indicate its potential.

INTRODUCTION

The time taken to transfer a process from one equipment set to another is one of the most important issues in maintaining a competitive position within today's market place. In recent years Technology Computer Aided Design (TCAD) has emerged as a key tool in reducing the development time of new processes and devices. TCAD is also one of a number of tools that can help reduce both the time and effort required to transfer a process. However, using TCAD to model semiconductor processing requires a significant investment in the generation of the simulation code. This paper aims to address this issue by providing a methodology for using TCAD for process transfer through the use of a semi-automated-system.

This paper gives a brief outline of process transfer issues and the role that TCAD can play in the procedure. The methodology of developing an automated system to aid this role is described together with its design. Implementation is discussed and an example used to illustrate its potential.

PROCESS TRANSFER

The key concept in process transfer is reproducing an existing process on a new equipment set. It is important that each new process step has the same effect on the wafer as the step it replaces. For example, oxide thickness should be the same, as should the doping profiles within the wafer.

In order to achieve this the process developer must consider a number of issues. These include the characterisation of the existing process, e.g. techniques such as SIMS (Secondary Ion Mass Spectroscopy) and SRP (Spreading Resistance Profiles), and the constraints placed on the new process by the new equipment set e.g. any enforced differences between thermal processing steps during the ramp up/down stages. Additionally, with wafer size changes, non-thermal processing conditions must also be examined, to ensure the reproducibility of process steps such as implant and lithography.

This paper concentrates on the issues involved in thermal processing. In particular, providing alternative furnace operations when an existing temperature-time profile can not be directly matched.

THE ROLE OF TCAD IN PROCESS TRANSFER

TCAD is capable of simulating the effect of thermal processing which must often be modified when processes are transferred. In practical terms this means all of those process steps that involve, diffusion, deposition and epitaxial growth. This is a consequence of the potential for differences in equipment settings, such as the initial processing temperatures and ramp up/down rates illustrated in figure 1.

Figure 1 shows two furnace temperature-time profiles. The existing process is indicted by a dashed line and the new one by the solid line. In this scenario, the differences between the profiles means that for the same overall diffusion to occur the soak time for the new process must be adjusted.

In order to find a new soak time to act as a start point for a process transfer the differences between the ramp rates must be calculated. This can then be translated into an equivalent time at the soak temperature and the new soak time derived. This start point can then be used to

Figure A.25: *Reprint of paper presented at IWSM 1999, page 1.*

process confirmation wafers. SIMS and SRP techniques can then be used to compare the wafers from the new process with wafers processed under the existing conditions and the soak time adjusted accordingly. This

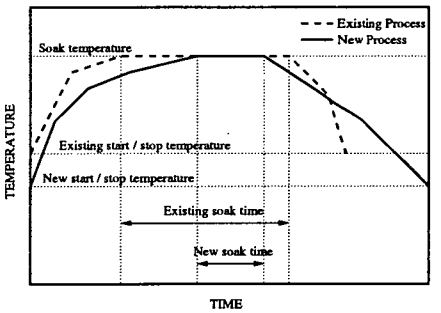

Figure 1: Furnace temperature profiles.

procedure continues until a suitable match is identified.

However, this same approach can be taken using TCAD to simulate the doping profiles and optimise the soak time to match the profile of the two processes. This is a much faster and more robust method of arriving at a first estimate. The advantage to be gained by this approach is magnified as the number of process changes increase.

IMPLEMENTATION

An overview of the general operation of the system that has been developed is shown in figure 2. The key to the system lies within the process flow file. This is an ASCII text file which contains a list of all the existing individual process step file names in the order in which processing occurs. This file allows any unwanted process steps to be commented out, allowing different 1-D process cross-sections to be easily selected. It is also used to identify the process steps which are being replaced, i.e. those that require optimisation to match an equivalent step in the existing process.

For each process step highlighted for replacement the control software will either use a replacement TCAD input file (.new files in figure 2) or if no new file is available sample code is provided for editing.

The control software creates two TSUPREM-4 [1] (1-D or 2-D process simulator) input files, one for the existing process and one for the new one. For each step selected for optimisation the existing process TCAD file is augmented with instructions to extract the doping profiles after the completion of that process step. These profiles are used by TSUPREM-4 to optimise any selected TCAD parameter such that the doping profiles match. In order to assess the success of the optimisation process the doping profiles for both the existing and new process are automatically plotted after each step in question and at the end of the complete process.

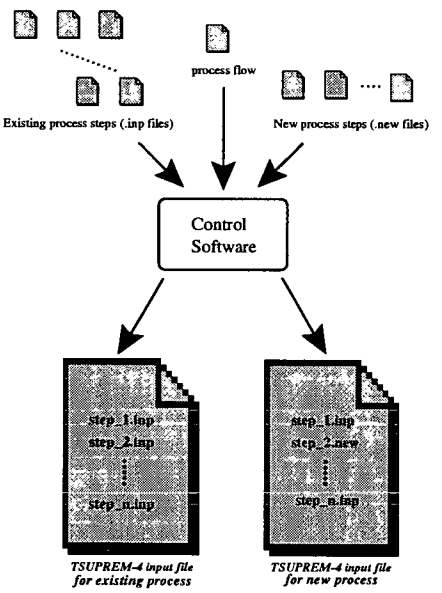

Figure 2: General overview of process transfer software.

EXAMPLE

Using automated TCAD optimization to match 200mm and 150mm wafer process steps.

This example considers the implications on the process steps used to form the p and n-wells of a CMOS process when the wafer size is increased from 150 to 200mm. Due to the change in wafer size and the subsequent difference in furnace profile new well drive process conditions must be identified. The circumstances are similar to those previously described and illustrated in figure 1. The start and finish temperature is reduced and slower ramp rates must be used to ensure an even rise in temperature over the wafer surface. This example will

Figure A.26: *Reprint of paper presented at IWSM 1999, page 2.*

show the methodology used to find the soak time required to result in a comparable process.

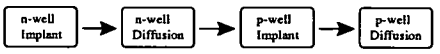

Figure 3: Process flow, for 150 to 200mm transfer.

Figure 3 illustrates the order of processing, the wafer passes through both the n and p-well drive stages and is implanted as defined by the appropriate masks. Both the p and n-well regions must be considered separately as they receive only one implant. The problem can be split into two 1-D simulations, one in each of the wells. Given that the ramp up and down rates are fixed, the soak time for the 200mm p-well drive that mirrors the 150mm process must be determined. Similar analysis can then be performed for the n-well region. This procedure has four stages:

1. Simulate the 150mm n-well drive, the p-well implant and the 150mm p-well drive. This provides doping profiles for the boron within the p-well region.

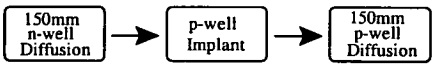

Figure 4: Stage 1 process flow, existing p-well region.

2. Simulate the 150mm n-well drive and the p-well implant. Then use the optimise routine in TSUPREM-4 to find the p-well soak time by comparing the current doping profile with that obtained from the p-well drive in stage 1. TSUPREM-4 uses a sum of squares optimiser and uses a single RMS error, calculated by combining the errors from all doping profile locations, to determine the fit of the solution. When this RMS error is less than the set tolerance (in this case 0.01) the optimisation step is complete and the final values are returned. This gives the 200mm p-well drive process step.

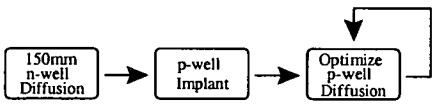

Figure 5: Stage 2 process flow, optimisation loop for new p-well region.

3. Simulate the n-well implant, the 150mm n-well drive and the 150mm p-well drive. This provides the doping profile for the phosphorus within the n-well region after the drive.

Figure 6: Stage 3 process flow, existing n-well region.

4. Next, the n-well implant is simulated and the optimise routine in TSUPREM-4 used to determine the new n-well soak time. This is done by comparing the current doping profile with that obtained from the n-well drive in stage 3, resulting in the 200mm n-well drive process step.

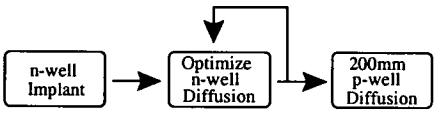

Figure 7: Stage 4 process flow, optimisation loop for new n-well region.

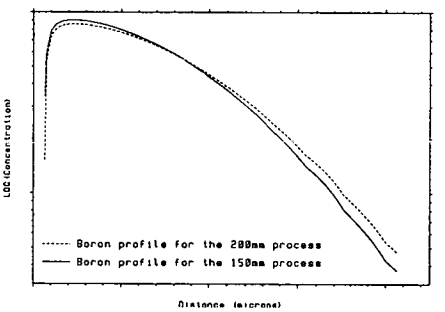

Figure 8: Comparison of existing 150mm wafer size process flow and the new 200mm wafer size process flow, for the boron doping in the p-well region.

Figure A.27: *Reprint of paper presented at IWSM 1999, page 3.*

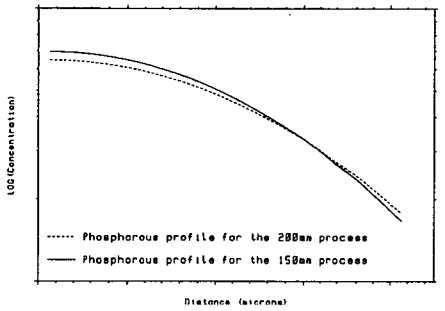

Figure 9: Comparison of existing 150mm wafer size process flow and the new 200mm wafer size process flow, for the phosphorus doping in the n-well region.

The results of this analysis are shown in figures 8 and 9, for the p and n-well regions respectively. It should be noted that the scales have been removed to obscure the exact details of the profile. The plots show the doping profiles after completion of the drive stages for both the existing 150mm process and the 200mm process as optimised by TSUPREM-4. While the two profiles for the p-well and n-well are not identical the TSUPREM-4 optimiser has managed to synthesise a process soak time that provides a good starting point for the process transfer.

CONCLUSION

This paper has discussed the role of TCAD within the context of process transfer. A semi-automated system and methodology for the use of TCAD in process transfer have been presented and an example has been used to illustrate its use in a real life situation.

The system uses a simple process flow to build TSUPREM-4 input files for both the existing process and the new process. Running the existing simulation process provides the information for the simulator to fit the new process to match the existing one. The main benefits of the system lies in its data management and the reduction in time it takes to write the TCAD code. By removing much of the need for manual editing and automatically creating the output files needed for the optimization routines the effort required by the user is greatly reduced. In particular the system widens the TCAD user base by making it possible for the less specialised users to perform tasks that would previously have required more detailed knowledge.

ACKNOWLEDGMENTS

The authors would like to acknowledge the contributions of the following organisations, without whom this research would not be possible: NEC Semiconductors (UK) Limited, EPSRC (R/K98733) Avant! Corp., Promis Systems Corp., Manugistics Inc., Domain Solutions Corp., National Semiconductor UK, Motorola and Mitel Semiconductor.

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Figure A.28: *Reprint of paper presented at IWSM 1999, page 4.*

Accurate Prediction of IC Manufacturing Distributions using Improved Response Surface Fitting

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Abstract - This paper presents an improved method of fitting response surfaces which enables manufacturing distributions to be more accurately predicted. Response surfaces and distributions are compared for covariance and polynomial models for both a known response and for actual simulation data and the improvements highlighted.

I. Introduction

The key to the accurate prediction of response distributions lies in the fit of the response model. The purpose of this paper is to demonstrate that covariance based response models can provide a significant improvement over traditional polynomial models when used to predict response distributions.

II. Covariance Based Models

Experimental design and response surface methodology [1] techniques are common place in process and device simulation. However, in contrast to standard experimental techniques, simulation results have no random error associated with them and so there is every justification in fitting a surface through all the data points. The covariance [2] method ensures that the resultant model passes through each data point by initially fitting a polynomial and then pulling the model to pass through each of the data points.

III. Response Distributions

Figure 1 indicates how a response distribution can be affected by the slope of a response. The gradient, or first derivative, influences the standard deviation, as shown in figure 1 (a) and the rate of change of the slope, or second derivative, the skewness as shown in figure 1 (b). This means that the fit of a response model is crucial in ensuring that accurate manufacturing distributions can be predicted.

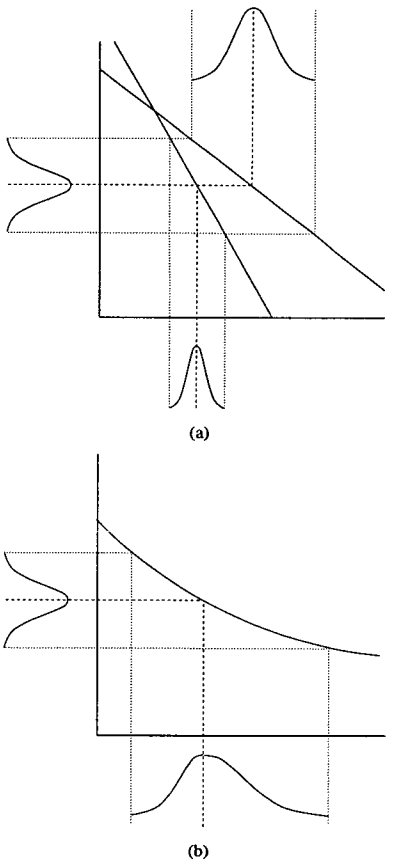


Figure 1. Effect of the slope on (a) the standard deviation and (b) the skew of a distribution

Figure A.29: *Reprint of paper submitted to IWSM 2000, page 1.*

IV. Response models comparison

In order to demonstrate the effectiveness of covariance modelling for predicting distributions, both covariance and polynomial models have been fitted to a hypothetical process. The response of the process is given by:

$$Y = (15.0\ X1^2) / (1.0 + 1.5e^{2.5X2}) \qquad (1)$$

The power of this approach is that the exact response surface can be generated for comparison.

A full factorial experiment was designed and 16 values calculated. Both quadratic and cubic models were fitted to the data points in addition to the covariance model. Figure 2 shows contour plots for the actual response, together with the quadratic, cubic and covariance fits.

It is clear that the covariance model provides a more accurate representation of the response than either of the polynomial models, particularly the region of low X1 and high X2. From table 1 it can be observed that the R^2-adj. value (0.985) of the cubic model is very good but even it is struggling to fit equation (1) in this region.

The fitted models can be used to generate response distributions to simulate variability in the control factors. Figure 3 compares the response distributions for the four models examined in figure 2 when X1 = 3.125 and X2 = 1.125, and with both factors having a standard deviation of 2%. These results are summarised in table 1.

Table 1. Fit for the four response models shown in figure 2 at the 16 data points and the distribution parameters associated with figure 3.

Model	R^2-adj.	Mean	St. Dev.	Skewness
Actual	1	5.650	0.379	0.195
Covariance	1	5.245	0.385	0.194
Cubic	0.985	2.559	0.336	0.376
Quadratic	0.880	2.560	1.015	0.112

The results shown in figure 3 and table 1 indicate that a covariance fit offers a definite improvement over the polynomial models. The excellent agreement of the covariance model with the actual distribution indicates that there are significant advantages using the covariance fit for both the prediction of response surfaces and their associated distributions.

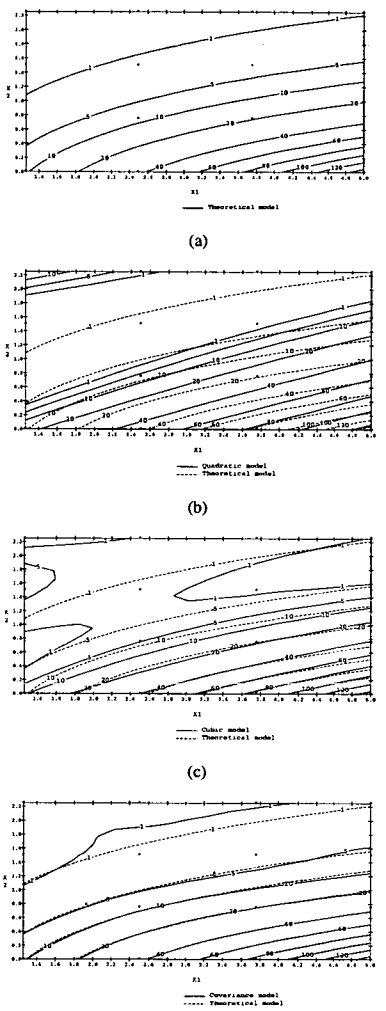
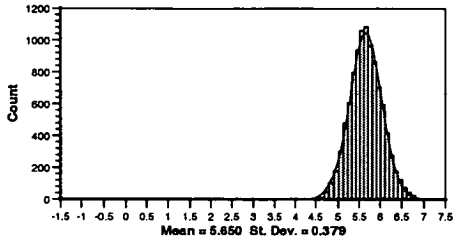
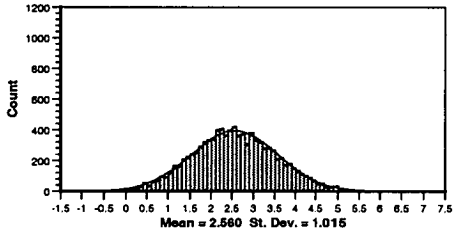


Figure 2. Contour plots of responses (16 data points) for (a) actual response (equation (1)), (b) quadratic model, (c) cubic model, (d) covariance model.

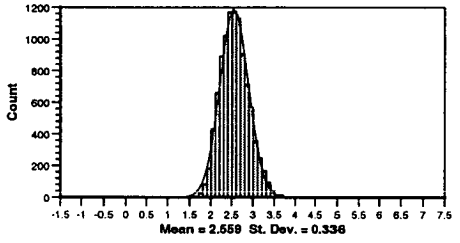
Figure A.30: *Reprint of paper submitted to IWSM 2000, page 2.*



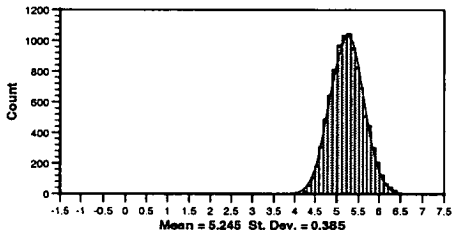
(a)



(b)



(c)



(d)

Figure 3. Response distributions for X1 = 3.125, X2 = 1.125 (2% St. Dev., sample size = 10000) for (a) theoretical response (equation 1), (b) quadratic model, (c) cubic model and (d) covariance model.

V. Response Models Comparison using Simulated Data

Finally we demonstrate the application of the technique on some IC related simulation data. This example considers a 3 factor full factorial experiment with 4 responses, R_{SD}, G_m, V_{PT} and E_{PEAK}. The 27 simulations were performed and quadratic and covariance models fitted. Table 2 gives the quadratic R^2-adj. values (Note: by definition R^2-adj. = 1 for all covariance models). Figure 4 shows contour plots of both models for each response and in each case it is clear that there is a significant difference between them.

Table 2. Comparison of the fit and distribution parameters for the covariance and quadratic response models fitted using 27 simulated data points.

Responses	Mean		St. Dev.		Skewness		R^2-adj.
	Cov	Quad	Cov	Quad	Cov	Quad	Quad
V_{PT} (V)	19.51	18.37	0.217	0.227	-0.036	0.043	0.983
E_{PEAK} (MeV)	327.0	322.0	6304	4288	0.273	0.217	0.997
G_m (mhos)	6.506	6.684	0.108	0.106	0.252	0.058	0.995
R_{SD} (ohms)	972.7	1009	40.58	44.00	0.100	0.107	0.989

This is further emphasised when the distributions are generated. The key factors of the distributions are summarised in table 2 and the response distributions for E_{PEAK} illustrated in figure 5.

From figure 5 it can be observed that the mean value of the distributions are close but there is a significant difference in the predicted standard deviation. The previous comparison suggests that the covariance model should be the one of choice for all the responses.

VI. Conclusions

Covariance fitting of response models has been demonstrated to provide a significant improvement over traditional polynomial fitting methods. This paper shows for the first time the improvement that covariance modelling can have on the prediction of response distributions.

VII. Acknowledgments

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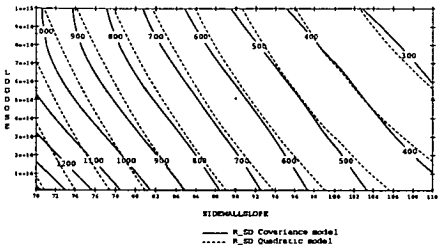
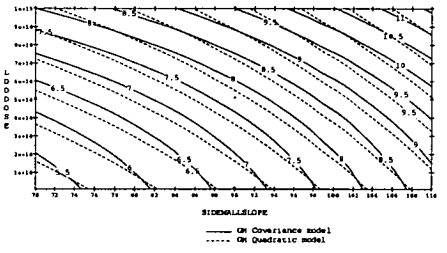
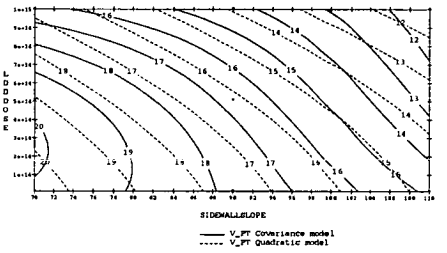
Figure A.31: *Reprint of paper submitted to IWSM 2000, page 3.*



(a)



(b)



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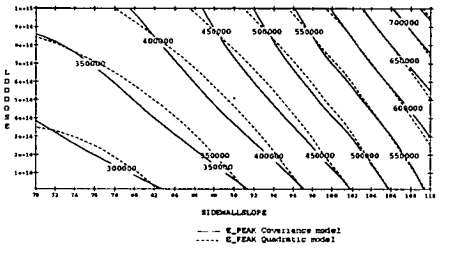
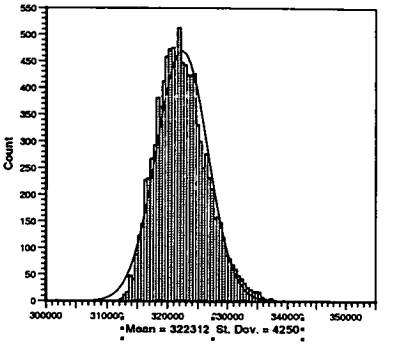
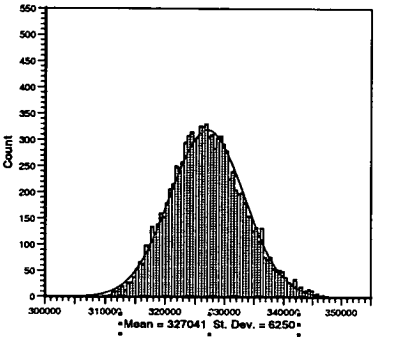


(d)

Figure 4. Comparison of contour plots of quadratic and covariance models fitted to 27 simulation data points, (a) R_{SD}, (b) G_m, (c) V_{PT}, (d) E_{PEAK}.



(a)



(b)

Figure 5. E_{PEAK} Response distributions (side wall slope = 75, LDD Dose = 5e14, LDD Energy = 30 keV, (2% St. Dev, sample size = 10000, bin size = 500), (a) quadratic model, (b) covariance model.

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