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High efficiency wide-band line drivers in low voltage CMOS using Class-D techniques

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Abstract

In this thesis, the applicability of Class-D amplifiers to integrated wide-band communication line driver applications is studied. While Class-D techniques can address some of the efficiency limitations of linear amplifier structures and have shown promising results in low frequency applications, the low frequency techniques and knowledge need further development in order to improve their practicality for wide band systems.

New structures and techniques to extend the application of Class-D to wide-band communication systems, in particular the HomePlug AV wire-line communication standard, will be proposed. Additionally, the digital processing requirements of these wide-band systems drives rapid movement towards nanometer technology nodes and presents new challenges which will be addressed, and new opportunities which will be exploited, for wide-band integrated Class-D line drivers.

There are three main contributions of this research. First, a model of Class-D efficiency degradation mechanisms is created, which allows the impact of high-level design choices such as supply voltage, process technology and operating frequency to be assessed. The outcome of this section is a strategy for pushing the high efficiency of Class-D to wide band communication applications, with switching frequencies up to many hundreds of Megahertz.

A second part of this research considers the design of efficient, fast and high power Class-D output stages, as these are the major efficiency and bandwidth bottleneck in wide-band applications. A novel NMOS-only totem pole output stage with a fast, integrated drive structure will be proposed.

In a third section, a complete wide-band Class-D line driver is designed in a $0.13\mu m$ digital CMOS process. The line driver is systematically designed using a rigorous development methodology and the aims are to maximise the achievable signal bandwidth while minimising power dissipation. Novel circuits and circuit structures are proposed as part of this section and the resulting fabricated Class-D line driver test chip shows an efficiency of 15% while driving a 30MHz wide signal with an MTPR of 22dB, at 33mW injected power.

Acknowledgements

This work would not have been possible without help from a large number of people. I would like to thank Dr. Robert Henderson, my supervisor, for his support, guidance and suggestions of areas to explore. I am very grateful to Dr. Keith Findlater from Broadcom Europe, for his unwavering support for me finishing this project; both on a personal level and in terms of the considerable flexibility he allowed me to find time to work on this. I am also extremely grateful to Bob Stevenson, from the Broadcom Europe Layout team, who provided significant assistance with the layout of the test chip and build of the test board.

I would like to thank Jed Hurwitz for giving me the opportunity to learn about IC design; my former research group colleagues, Dr Seyed Danesh and Dr Steve Collins for our relaxed, insightful discussions; and the current and former members of the Broadcom Edinburgh, and formerly Gigle Networks, analogue design teams from whom I have learnt much and who are all great people to work with.

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Finally, for my wife Ming Yuan Cao; I am and always will be grateful for your support and companionship, I could not have done this without your help. This Thesis is as much a product of your efforts as it is of mine.

Declaration of Originality

I declare that this thesis was composed by myself and except for where specified in the text, that the work was originated and completed by myself. The work has not been submitted for any other degree or professional qualification except as specified.

Steven Maughan

Contents

Chapter 1

Introduction

Recent years have seen a rapid growth in the use of high data rate,"broadband" Internet connections to the home. In March 2001, less than 0.1% of UK Internet connections used a broadband system[1], but by the end of 2008, broadband connections accounted for 95.1% of home Internet connections[2].

The growth of broadband connections spurred the development of data intensive applications such as streaming audio and video. Broadband also makes it practical for multiple users to use a single Internet connection simultaneously. However, similar to the "last mile" problem known in broadband access networks[1], there is a "last 10 meter" problem – the final communication link between the broadband terminating equipment inside the customer premises, and the multitude of devices which want to use it.

The solution focused on here re-uses the existing mains wiring system to create a *powerline network*. This transmits/receives data using the in-home mains wiring network as a communications channel. However, the mains network is a noisy environment and it is hard to achieve high data-rates. Complex modulation schemes such as OFDM have been found to perform well in noisy environments, but problematic time domain properties of the modulated signal result in low efficiency of the final stage of the powerline communication transmitter, the line driver. Line drivers are power amplifiers tailored for driving wired communication channels and in order to meet the linearity and bandwidth requirements of the OFDM modulation scheme, designers have been forced to use line driver structures which are inherently inefficient.

As home networking becomes commoditised (and driven down in cost), manufacturers aim to reduce the cost of their parts in order to maintain profit margins. There is a

[1]The "last mile" is the approximate distance between a company's telecommunications exchange, and the terminating equipment within a customers premises.

desire to integrate analogue functions, like the line driver, on the same die as digital functionality usually implemented in a low voltage CMOS process. This can lead to significant cost savings, but the use of low voltage digital technologies to implement demanding analogue structures significantly exacerbates analogue block implementation challenges.

Switching output stages known as Class-D have been shown to be highly efficient and linear in low frequency audio applications. Due to their switching nature, they also seem well matched to digital CMOS implementation. However, extending their bandwidth while maintaining linearity and efficiency soon encounters circuit and implementation difficulties, and the low digital CMOS supply voltages, limit the power that the Class-D can develop.

1.1 Problem Statement

The aim of this work is to develop a Class-D line driver architecture for in-home powerline communication applications, with two main aims:

- Improve the Class-D trade-off of efficiency-linearity-bandwidth through the development of novel circuit and system structures.
- Integrate the line driver in a low voltage digital CMOS process, while injecting sufficient power for full-home powerline network coverage.

1.2 Contributions of Thesis

The focus of this work is improving the efficiency of line drivers for use in modern wide band communication systems through the use of Class D amplifier structures. This has resulted in three new developments. The first is a new power modelling toolkit, which allows rapid exploration of the efficiency implications of different Class-D structures under different operating conditions – process technology, operating frequency, load configuration and supply configuration.

The second new development is a Class-D output stage which is suitable for high frequency operation while exhibiting lower parasitic losses than conventional structures[3].

The final contribution is a wide band Class-D structure implemented in a 0.13μm CMOS process which achieves a bandwidth more than 50% greater than any other reported Class-D structure.

During the course of this work, the following publications were produced:

1. "A 90nm CMOS Dual-Channel Powerline Communication AFE for HomePlug AV with a Gb Extension", in Proceedings of the International Solid State Circuits Conference, 2008. This paper was produced by Gigle Networks and describes a Powerline AFE to which a very-low dropout, charge pump regulator was contributed.
2. "NMOS-only Class-D Output Stages based on Charge Pump Architectures" in Proceedings of the IEEE International Symposium on Circuits and Systems, 2009.
3. "A wide band CMOS Class-D line driver for wireline communication" in Proceedings of the 53rd IEEE International Midwest Symposium on Circuits and Systems, 2010.
4. "Transformer driver circuit with IC protection circuitry", US Patent US9001534 B2.

1.3 Organisation

Chapter 2 will outline the historical development of in-home data networks, and the development of the HomePlug AV standard. Basic metrics for the system will be established. A review of the available architectures will be given, including comparisons with other similar systems. Established solutions to the problem will be presented and the performance of the different architectures will be compared.

Chapter 3 will present some theoretical comparisons of the performance limits of the two main amplifier structures, and will suggest directions in which research should go.

Chapter 4 will discuss a new technique for driving NMOS-only output stages in Class-D applications at high frequency whilst minimising gate drive losses.

In Chapter 5, Class-D theory, design principles and modelling methodologies will be presented and in Chapter 6 these design methodologies will be used to create a high efficiency wide-band line-driver. Measurement results from a fabricated chip will be presented in Chapter 7.

Chapter 8 will summarise the work and present suggestions for future work.

Chapter 2

Background

Communication is a cornerstone of a successful society[4]. In previous centuries, communication involved media such as stone, papyrus or paper and while all are effective for storing and – aside from stone, perhaps – transmitting basic information, they have a range of monetary, time and distribution costs which limit the amount of information that can be transmitted economically. This in turn limits the services that can be provided over the communication medium.

With the emergence of electronic communication systems, the cost of communication has dropped to a point where it can be considered for most purposes as a near-zero cost resource. This has been driven by the development of the MOS transistor[5] and lithographic processes[6] which enable the precise and consistent production of immensely complicated digital electronic machines (integrated circuits), while requiring negligible[1] volume, mass, power and cost. Semiconductor-based digital information processing allows vast quantities of information to be managed at extremely low cost and at very high speed, allowing commoditising of complex information processing and communication tasks.

As electronic communication systems such as telephony, television, computer data networks and mobile communication devices have evolved, they have converged around the Internet Protocol[7] as a transport protocol. Protocol standardisation allows interoperability between different classes of devices and has enabled a rapid increase in products and services which leverage communication, ranging from business and personal communication such as electronic mail, to entertainment services such as video streaming, to just-in-time supply chain management, and much more.

In recent years, these communication services have moved into the home, through rapid

[1] Compared to mechanical or valve-based technologies.

uptake[1][2] of high-speed "broadband" Internet access technologies such as Digital Subscriber Line (DSL)[8]. In parallel, the digital home has arisen, consisting of electronic information hot-spots: personal computers, smart phones, televisions, digital video recorders, home media centres, digital cameras and Internet access devices such as modems or routers. Initially operating in isolation, there is now a desire to connect these (and other) devices to allow communication between them, creating the digital *networked* home.

The digital networked home is a challenging communications environment. Entertainment media has rapidly embraced digital storage and transmission technologies, and this has led to a convergence of entertainment access devices, such as televisions with Internet access and personal computers with catch-up television[9]. This has opened the way for data agility: content distributed across devices in the home, but accessible by any device in the home. The data-rate demands of these systems can be very high and existing technologies may struggle to meet them, especially in situations where multiple streams are viewed simultaneously.

High Definition video streaming is one example of a growing and demanding use for the home communication network. Streams are typically encoded at between 10-20Mbit/s[10], but the dominant home networking technologies – wireless systems based on the IEEE 802.11 standard – have a practical maximum rate in ideal conditions of around 24Mbit/s[11] – only just capable of transferring a single high-quality HD video stream, assuming short range and favourable channel conditions. The data-agile networked home would have its potential severely constrained if it were built on existing communications technologies – multiple interaction devices could exist, but only one could be used at a time.

2.1 In-home networking

In-home networking became popular with the emergence of broadband internet access which could support data rates sufficient for multiple simultaneous users. While in-home networking has long been possible using technologies such as wired Ethernet[12], the requirement of costly retrofitting of network infrastructure such as cabling, switches and hubs in homes which rarely have network infrastructure installed, severely limited its uptake. Between 1999 and 2003, the emergence of the wireless Ethernet standards IEEE 802.11a/b/g [13][14][15], made home networking cheap, easy to install and practical by avoiding the need for cabling infrastructure and this kick-started the in-home networking market.

The maximum throughput rates of these standards – 5Mbit/s for 802.11b and 24Mbit/s

for 802.11a/g[11][16][17] – are sufficient for first generation text, voice and low-quality video. However, as broadband internet data rates have risen in response to higher quality audio and video applications, these technologies are becoming bottlenecks to the development of the digital networked home.

The latest revision of the 802.11 wireless ethernet standards, released in 2009, is 802.11n[18] which raises throughput rates to 100Mbit/s[19]. However, wireless networks are to some extent a victim of their own success. As wireless signals are not confined to the walls of a single house, wireless systems tend to be designed for small cell sizes in order to maximise global capacity by minimising interference with neighbouring cells, while being just large enough to ensure coverage of the average house. For a particular house, this causes either reduced coverage throughout the house (areas of poor or no reception), or interference with neighbouring channels – in both cases the result can be lower than expected data rates.

A number of new technologies aim to exceed the data rates of wireless networks by re-using existing in-home cabling, specifically phone line[20], co-axial[21] and powerline[22] cabling. By reusing existing cabling, these technologies provide a channel which can be exclusively used by a single dwelling, free from interference from neighbouring units and with far fewer radio spectrum restrictions than wireless have – allowing for wider bandwidth, higher rate communication links.

While extensive phone line and co-axial installations are common in some geographic regions – such as North America or Japan – they are less common in others, such as Europe. In contrast, powerline networks are common in all geographic regions and, unlike phone line or co-axial networks which are typically limited to a single access point in each room, it is common for powerline installations to have a multiplicity of access points per room. Additionally, a significant advantage of powerline compared to co-axial or phone line networking is that most devices need to be connected to the powerline network anyway, in order to receive electrical power.

For these reasons, powerline has become a prominent candidate for implementing the digital networked home. It should be noted, however, that powerline networking is only partially a competitor to wireless home networking technologies as the two have different strengths. While powerline networking can offer a dedicated, high-rate communication channel with coverage throughout a dwelling's electrical network, wireless networking provides a medium-rate communication channel with user mobility, within a short range of an access point. An interesting implementation of the digital networked home appears to be a combination of the two technologies. However, this thesis will focus on the implementation of powerline networks.

2.2 Powerline communication

Communication over power lines has been around since electricity networks became commonplace. However, the term *powerline communication* (PLC) covers three different usage scenarios. The first scenario is long-distance transmission of data – typically signalling and network control – over high-voltage electricity transmission lines at data rates of a few hundred bits per second. A second scenario involves communication over a neighbourhood power distribution network and aims to provide low data rate control information for systems such as street lighting, or to provide automated meter readings from household electricity meters, with data rates around a few kilo-bits per second. Recently, the technology has also been proposed[23] and trialled as a method of providing home internet access at rates around a few mega-bits per second, although the market share of technology is low compared to technologies such as Digital Subscriber Line (DSL) and coaxial cable.

Finally, PLC can also involve the use of the in-home mains network to provide data communications at each power socket throughout a home. Communication beyond the home is is limited by attenuation through the electricity meter, thus distinctly separating distribution and in-home networks. In this scenario, data rates typically range from 85Mbit/s to 1Gbit/s and the intended usage is in-home data networking, including high data-rate entertainment applications such as digital video transmission.

This work will focus on the in-home PLC scenario.

2.2.1 Channel characteristics

To appreciate the development of in-home powerline networking, it is useful to consider the channel characteristics of an in-home powerline network.

Powerline networks were designed for low cost, high power and low frequency electricity distribution and are not well suited for use in low power, high frequency communication systems. The main problems faced are variable line impedance, noise and attenuation of the signal, which vary across time, frequency, from house to house and from country to country. As electrical appliances on the mains network are connected and disconnected, or change power/operating states, they alter the impedance, noise and attenuation seen from other points on the network and this variation also takes places across frequency[24]. Furthermore, unlike other wired communication channels such as co-axial cable or ethernet cable, powerline is an unshielded untwisted medium and so is especially prone to radio interference, in addition to noise generated by other appliances on the powerline network.

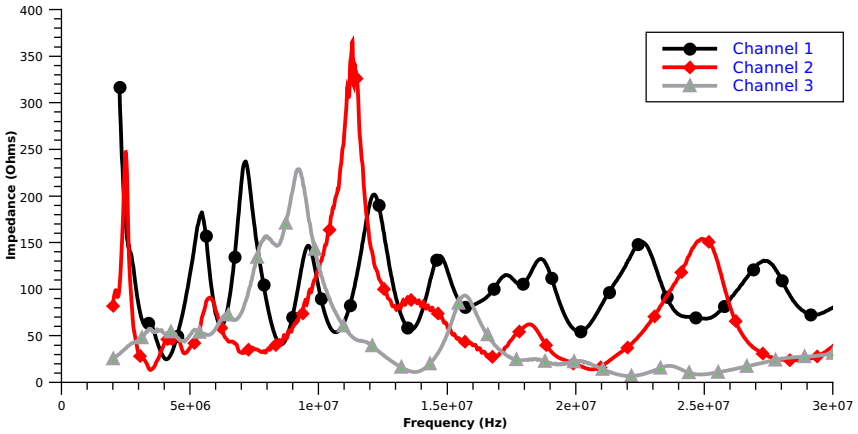

Figure 2.1: Impedance of the powerline versus frequency as seen from three sockets in three separate powerline networks. Impedance varies significantly with frequency, and varies between socket. Measurement data provided by Gigle Networks.

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Figures 2.1 and 2.2 show selected impedance and attenuation versus frequency measurements from different mains networks which are illustrative of the variability typically encountered on a powerline network. The peaks and notches present in both graphs are a result of the tree structure of a powerline network, which has branches of various lengths and with different termination impedances at the end of each branch. As transmitted signals propagate along many paths in parallel, impedance mismatches cause reflections which can cancel out the transmitted signal at a frequencies related to the length of the branches[25].

While there is significant impedance variability across and between channels, measurement data provided by Gigle Networks shows that average impedance computed over hundreds of channels is approximately 100 Ohms, and this matches results in other publications[26].

2.2.2 Regulation

As powerline networks connect to every mains powered device in a home, there are many possibilities for unwanted and unexpected interference between devices. To reduce the risks and consequences of interference, the use of powerline networks are regulated by regional bodies such as the Federal Communications Commission (FCC) in the United States and Ofcom in the UK. These bodies take guidance from International Telecommunication Union (ITU) standards and so regulations are similar between different geographic regions.

Within the powerline regulatory framework, PLC is classed as an “unintentional radia-

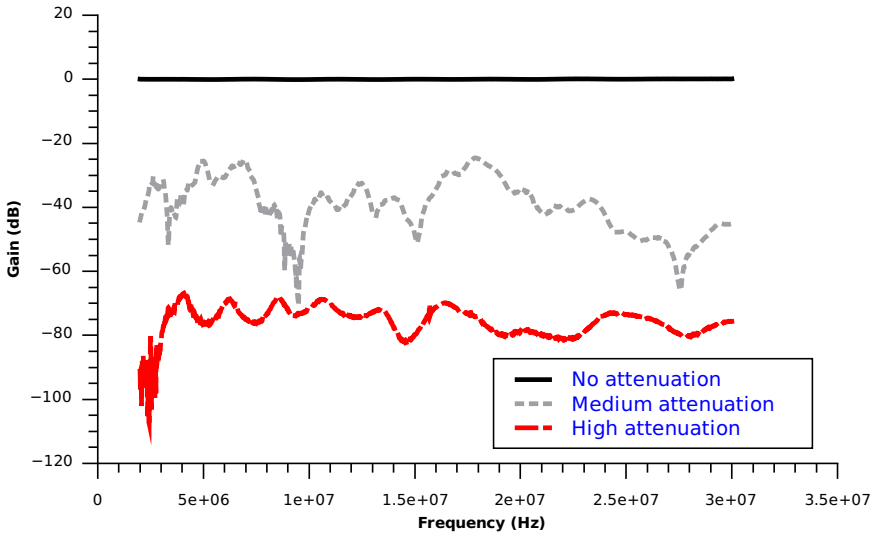

Figure 2.2: Attenuation between a transmitter and a receiver on a powerline network for a selection of powerline channels showing high, medium and low attenuation profiles. Line attenuation varies across frequency, and different points on the network experience vastly different attenuation profiles. Measurement data provided by Gigle Networks.

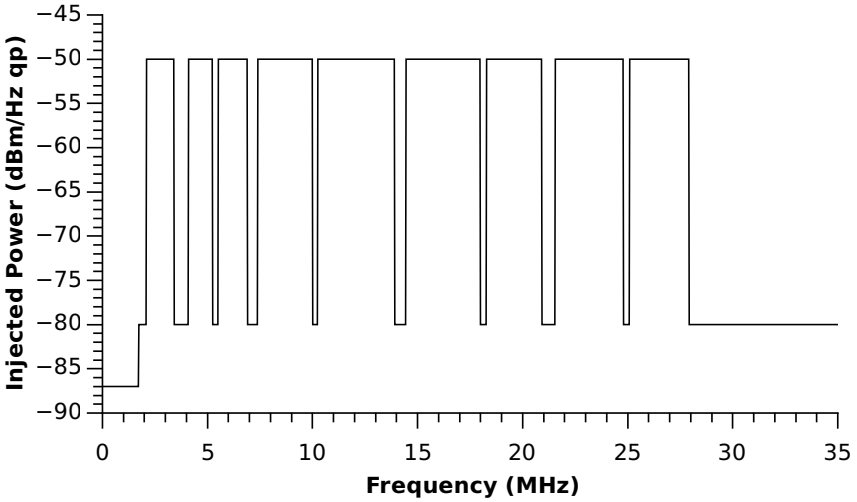

Figure 2.3: North American EMC limits for powerline communications in the 0-35MHz band. The limits are specified in dBm/Hz quasi-peak while driving a specific test setup with a 100Ω differential load.

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tor", whereby it can be used to transmit and receive data over power lines but it must adhere to requirements designed for devices which are *not intended to be transmitters*. The relevant specifications come in the form of an Electromagnetic Compatibility (EMC) spectrum which shows the maximum power that can be injected at each frequency on a powerline network. The EMC spectrum for North America in Figure 2.3 shows a maximum injected power of -50dBm/Hz quasi-peak in a number of bands each of

which is a few megahertz wide, separated by bands with a maximum injected power of -80dBm/Hz quasi-peak. At very low frequency, the injected limit is -87dBm/Hz quasi-peak and above 30MHz, the limit is -80dBm/Hz quasi-peak up to 88MHz, after which the level drops to very low levels. The -80dBm/Hz "notches" are in place to ensure powerline devices do not interfere with amateur radio equipment which operates in the radio bands corresponding to the notches.

2.2.3 History and development

In-home powerline communication uses are known dating back to the 1940's, with the Pye Talkbox, an intercom system using analogue modulation over in-home mains network. Digital communication systems operating over the mains network are known of from the 1980's, where 9.6kbit/s data networks are created over mains wiring[27], although there was little standardisation of the modulation, protocols or frequencies. In order to cope with the variable channel characteristics, these systems used narrowband analogue or digital modulation schemes such that the band could be approximated as flat over a narrow enough band. A small number of carriers generated using analogue circuitry operated in the 110kHz–140kHz band, which was in part due to regulatory constraints which existed at the time, and in part due to the slightly favourable impedance and attenuation characteristics which made low-rate data communication practical.

The maximum data rate of a channel is given by the well known Shannon-Hartley theorem[28][29], which relates the power of a communication signal P, the noise level in a channel N, and the bandwidth of the channel W, to the channel capacity C given in bits per second. The relationship is given in Equation (2.1).

$$\mathrm{C} = \mathrm{W} \log_2 \frac{\mathrm{P} + \mathrm{N}}{\mathrm{N}} \tag{2.1}$$

As discussed previously, regulatory constraints limit the maximum carrier power and the frequency bands which can be used in PLC networks. Channel noise is also out of the control of the powerline communication designer – time and frequency variable noise will be present and a reliable communication system must be able to cope with it.

As signal power P and channel noise N are both parameters determined externally, the only option left to increase the channel capacity is the signal bandwidth parameter, W. While it is possible to modulate a high frequency carrier with a wide band information signal such as in Figure 2.4(a), variations of the channel impedance, noise and attenuation across signal bandwidth causes inter-symbol interference, resulting in poor bit error rates. While this can be mitigated to some extent by channel equalisation, where the

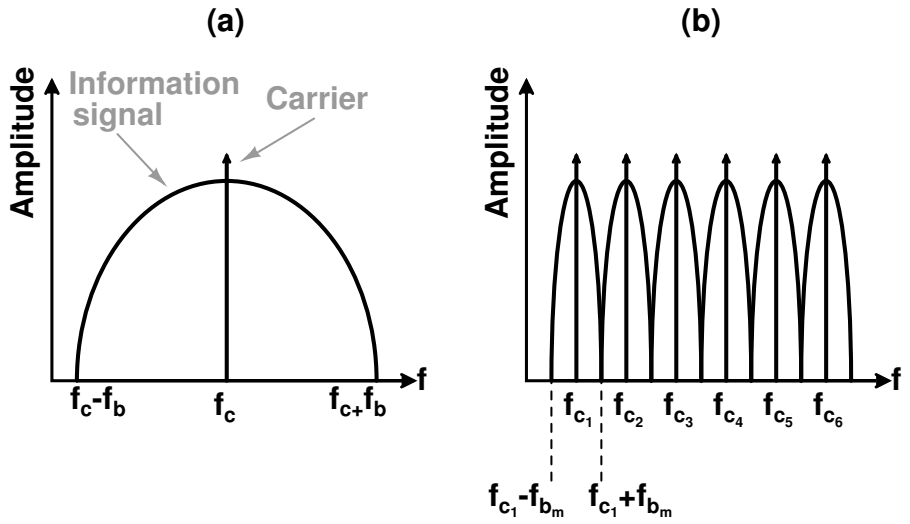

Figure 2.4: Spectra of (a) a single carrier signal modulated by a signal with bandwidth $2f_b$ and (b) a multi-carrier signal with six carrier each with bandwidth $2f_{b_m}$.

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characteristics of the channel are estimated and an inverse channel model is computed, the complex equalisation hardware required to equalise wide-band channels with widely varying characteristics – such as in powerline networks – makes them uneconomical. Additionally, the spectrum allocated by regulatory bodies which is available for use by PLC systems is not of consistent power as shown earlier in Figure 2.3 and so a single wide-band carrier is therefore not possible and instead, multiple medium-band carriers would be required.

Embracing the requirement of multiple medium-band carriers, a more robust and economical approach is to divide a wide-band channel into many narrowband channels and use multiple carriers, one per narrowband channel, with a bandwidth less than the narrowband channel spacing. Such an approach is illustrated in Figure 2.4(b) and is termed Orthogonal Frequency Division Multiplexing (OFDM) or alternately, Discrete Multi-Tone (DMT)[2]. Multi-carrier approaches ensure that over a narrow enough band, each individual channel has an approximately flat frequency response (both attenuation and impedance) so avoids inter-symbol interference[30]. Additionally, frequencies which are notched in a region's EMC spectrum and have a lower maximum injected power can either be reduced in power or, more commonly, not used for transmitting information.

A number of additional techniques can be used with the basic DMT approach. While narrowband carriers ameliorate the problems of inter-symbol interference, different carriers still have different attenuations and see different powers, as well as having different noise levels, depending on their frequency. Therefore, the amount of information

[2]The term Discrete Multi-Tone (DMT) is also used, more commonly in a baseband context while the term OFDM is more commonly used in RF applications.

transmitted per carrier can be optimised on a per-carrier basis according to the power, noise and attenuation at that specific frequency. Furthermore, as the noise, attenuation and impedance varies over time, the powerline communication system can dynamically adjust the information-carrying capacity of each carrier in order to the maximise the total capacity of all narrowband carriers at each point in time. In this way, DMT approaches enable near-Shannon channel capacity to be achieved on poor-quality, highly time and frequency variable channels.

However, there is a problem with the DMT approach. The use of narrowband carriers and wide overall signal bandwidths means hundreds or thousands of carriers are required. Modulating and demodulating data on so many carriers, in addition to managing optimum information loading on those thousands of carriers creates extremely high digital processing requirements. It is only recent improvements in DSP and the increased availability of cheap, fast digital technologies that has made computationally intensive modulation schemes such as DMT practical.

2.2.4 Standardisation

The DMT approach to powerline communication is a common choice among PLC manufacturers but the complexity of the approach leaves open many decisions on how the system should be implemented, how carriers should be modulated, what the width and frequency of each carrier should be, how the system responds to changing channel conditions and many other details.

Over time, a number of manufacturer consortia emerged, each with their own “standard” which was incompatible with other consortiums’ standards, but most of which used the same basic multi-carrier techniques. The consortium which developed the largest market share was the HomePlug Powerline Alliance, often shortened to just “HomePlug”.

The first HomePlug standard, HomePlug 1.0, was released in the year 2000 and used phase modulated DMT carriers in the -50dBm/Hz parts of the EMC spectrum between 2MHz and 30MHz to achieve a maximum channel rate of 14Mbit per second. Later, in an effort to improve speeds, some manufacturers[31] developed extensions to the HomePlug 1.0 specification which increased the bit loading per carrier in order to achieve speeds up to 85Mbit/s, while maintaining backward compatibility with HomePlug 1.0 devices.

With demand for higher data-rates being pushed by the growth of high-speed internet access and in particular digital media distribution, the HomePlug consortium began developing a new standard, which would be capable of providing the performance

required for the digital networked home. In 2005 the standard was released and is called HomePlug AV. Approximately 1000 narrowband carriers are used with further increased bit loading per carrier and turbo coding, to achieve channel rates of up to 200Mbit/s. Similar to other PLC standards, HomePlug AV achieves bidirectional communication using time-division duplexing such that only a single transmitter operates on a powerline network at any one time.

The HomePlug AV specification provides a number of implementation challenges which are representative of problems in state-of-the-art areas of communication system development, and so will be used as a reference point for this work.

It should be mentioned that the standardisation of powerline communications has continued since the release of HomePlug AV, with increasing collaboration between the manufacturer consortia and with participation from international standardisation bodies such as the IEEE and the ITU. The latest standards such as HomePlug AV2 from the HomePlug consortium and G.hn from the ITU expand the system bandwidth even further and achieve even higher data rates.

2.3 System architecture

As the motivation for, and development of, powerline networks has been discussed, the architecture of a PLC system will now be presented.

Very generally, a powerline communication system provides a point-to-point, unidirectional communication channel between a transmitter and a receiver and an individual powerline transceiver will contain a both a transmitter and receiver component, which time-share the powerline channel.

Due to the high complexity of the DMT modulation scheme, the only practical method method of modulating thousands of carriers in parallel is to use digital modulation and demodulation using Fourier and Inverse-Fourier transforms. To bridge the interface between the digital modulator and the analogue communication line, an Analogue Front End (AFE) is also required.

Figure 2.5 shows a schematic of an integrated powerline transceiver, although multi-chip solutions are also possible. Data to be transmitted is sent to a digital processing circuit, which performs operations such as error coding, interleaving and modulation. Subsequently, digitally modulated data is converted to an analogue form using a Digital to Analogue Converter (DAC) and finally can be driven off-chip and onto a powerline network using a power amplifier to drive the low channel impedance.

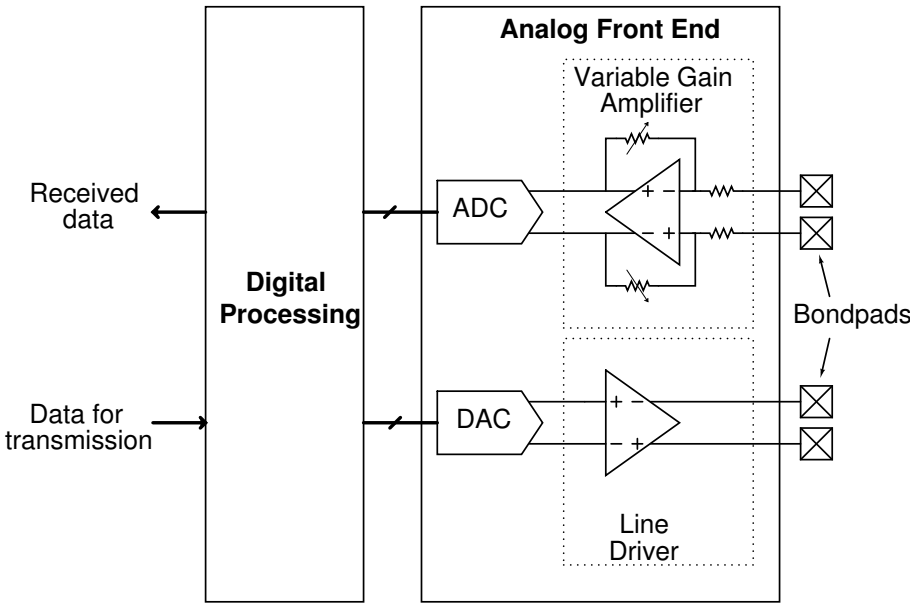

Figure 2.5: Architecture of a powerline communication system, showing a receive path (top) and a transmit path (bottom). Due to the time-multiplex nature of the system, the digital processing circuitry may be shared between both paths.

Similarly, received data are amplified by a variable gain amplifier and then converted to digital using an Analogue to Digital Converter (ADC), after which they can be digitally demodulated, de-interleaved and de-coded. The transmit path and receive path are time-multiplexed such that when transmitting, the receive path is disabled and ideally high impedance and similarly when receiving, the transmit path is disabled and high impedance.

It should be noted that the digital processing unit performs a number of other tasks such as medium access control, channel estimation, synchronisation and channel capacity optimisation, but these tasks are beyond the scope of this thesis and will not be discussed further.

The final link between the edge of a PLC transceiver and the powerline, the off-chip powerline interface circuit, is shown in Figure 2.6. A step-up transformer with ratio n:p is required when the peak line voltage requirement is greater than the supply voltage of the PLC circuit and in order to prevent unwanted DC current flows which would cause saturation of the transformer, DC blocking caps C_{DC} are also required. In order to limit reflections while transmitting, termination resistors R_{TERM} can also be added in series with the line driver outputs.

In the receive path, a p:m transformer is used to couple a signal received from the powerline into the receive path, where the ratio p:m is optimised to maximise receiver signal-to-noise ratio. To remove out-of-band noise prior to Analogue-to-Digital

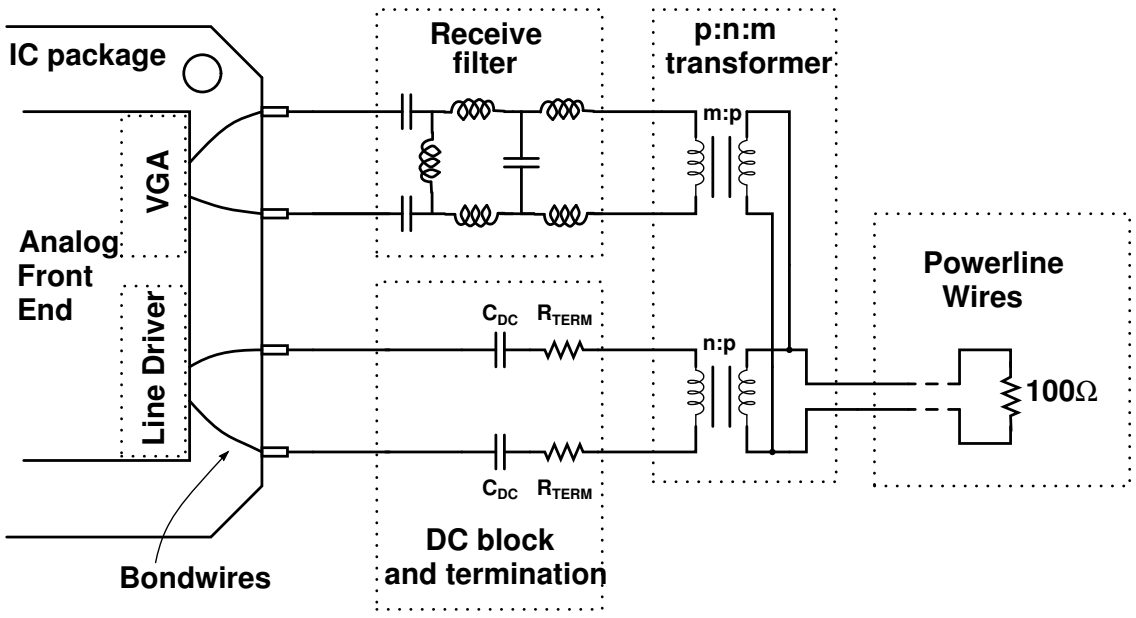

Figure 2.6: External circuitry required to connect powerline communication IC to powerline wiring. The powerline wiring is shown with a nominal characteristic impedance of 100Ω.

conversion, a bandpass receive filter is used.

2.4 OFDM symbol generation

The motivation for using OFDM has been established so now the method by which the OFDM time domain signal is generated from digital data will be discussed. In HomePlug AV applications, the OFDM time domain signal is referred[22] to as a "symbol", and this terminology will be used from here on.

Digital input data are represented by a series of binary 1's and 0's and will be mapped to a complex phasor in the frequency domain. To illustrate this, a constellation diagram showing all possible phasor endpoints is given in Figure 2.7. Input data is segmented into blocks of length $log_2(M)$, where M is the number of OFDM constellation points. For an example QAM-16 system, $M = 16$ and so each block would be four bits long. The first two of these four bits could be used to choose a real axis value in the constellation diagram, according to a mapping table. Table 2.1 shows an example mapping table. The same mapping table can also used for the second of two of the four data bits, to choose an imaginary axis value in the constellation diagram. Thus digital input bits can be mapped to a complex phasor with a particular real and imaginary value. As an example, the bit sequence 01110000 would be broken into two segments, which can be mapped using Table 2.1 to vectors $v_1{=}1 + 3j$ and $v_2{=}-1 - j$, as shown in Figure

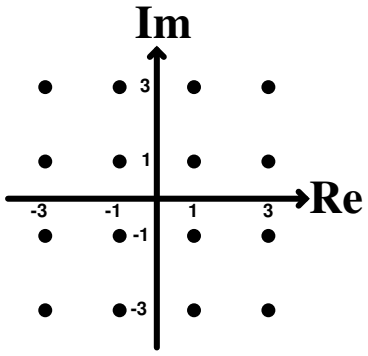

Figure 2.7: Constellation diagram showing all possible complex phase endpoints for a QAM-16 system. The constellation has been normalised such that the shortest phasor magnitude will have a value of $|\sqrt{2}|$.

Bit pair	Amplitude
01	1
11	3
00	-1
10	-3

Table 2.1: Mapping table showing example of relationship between data bits and real/imaginary amplitude values for a QAM-16 vector.

2.8. The complex phasors are then be mapped to specific carrier frequencies. Vector v_1 may be mapped to a frequency f, while vector v_2 could be mapped to a frequency $2f$. This operation is usually performed digitally in the frequency domain and for a straight forward linear mapping of vector v_n to carrier $n \times f$, means that complex phasor v_1 would be the first element in an inverse Fourier transform input sequence while complex phasor v_2 would be the second element in the inverse Fourier transform input sequence.

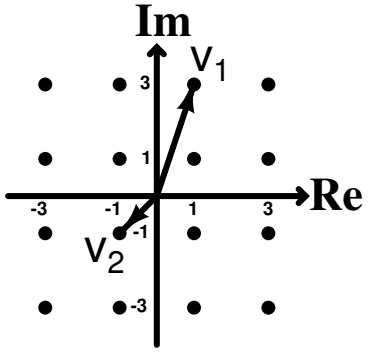

Figure 2.8: Vector mapping. Data bits 0111 are mapped to vector v_1, while data bits 0010 are mapped to vector v_2.

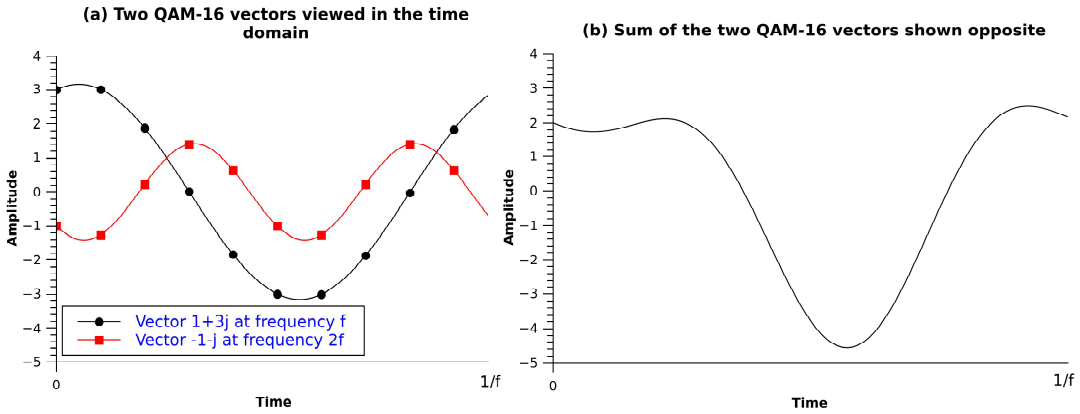

Figure 2.9: (a) Two complex phasors are mapped to two carrier frequencies, modulating their amplitude and phase. (b) The summation of the two modulated carriers results in the complete OFDM symbol.

The output of the inverse Fourier transform is the time domain OFDM symbol which will be transmitted.

Using the same example as above, the two-vector symbol would correspond to two time-domain sine waves at frequencies f and $2f$, with amplitudes and phases described by the corresponding complex phasor, as shown in Figure 2.9(a). The resulting time-domain symbol is shown in Figure 2.9(b). In a practical OFDM system the QAM level M can be chosen separately for each carrier in order to optimise the number of bits loaded at each frequency. As shown previously in Figure 2.2, carriers at some frequencies may suffer from more attenuation than at other frequencies. At a receiver, which is assumed to have a flat noise profile across the signal band, attenuated carriers will have lower available SNR than non-attenuated carriers, so those lower SNR carriers will be allocated a lower QAM level M than high SNR carriers would be allocated. This allows the bit loading per carrier to be adjusted according to the SNR available at each carrier. Note that dynamic bit loading per carrier is not common in most OFDM systems due to the overhead involved in continually measuring the channel SNR, but this is done in powerline OFDM implementations.

2.4.0.1 OFDM characteristics

In a multiple-carrier OFDM system, where there are hundreds or thousands or carriers, the time domain signal consists of a sum of many carriers which are phase and amplitude modulated according to the input data. Depending on the input data, it is possible for many of the carriers to align in phase and so the instantaneous value of the sum waveform can reach a peak. It is also possible for many of the carriers to align such

that the instantaneous value of the sum waveform at some point in time is zero. Most of the time, however, some of the carriers align in phase and most do not, so the sum signal which must be transmitted has a relatively small value. Figure 2.9(b) shows a two-carrier OFDM symbol and it should be noted that after normalising the signal, it spends more of its time at lower magnitudes than the two single carriers shown in Figure 2.9(a) do. Generally, greater numbers of carriers result in a lower root-mean-square signal value.

Representing a series of symbol amplitude values by the variable s, an important OFDM metric, Crest Factor (CF), can be defined as in Equation (2.2). It can also be expressed in decibel form, as in Equation 2.3.

$$\mathrm{CF} = \frac{\max(|\mathrm{s}|)}{\mathrm{rms}(s)} \tag{2.2}$$

$$\mathrm{CF_{dB}} = 20\log_{10}(\mathrm{CF}) \tag{2.3}$$

Practical OFDM systems have hundreds or thousands of carriers and as the number of carriers increases, so too does the CF. Figure 2.10 shows the CF of a number of randomly generated OFDM symbols. The number of carriers in each symbol is set to a particular value between 1 and 8191 and 50 symbols are generated for each number of carriers, in order to give a sample of the possible CFs. While a single carrier system can only have the crest factor of a sine wave which equals $\sqrt{2}$, as the number of carriers increases, range of possible CFs also increases, as does the median CF value.

In the case of HomePlug AV, which uses 920 carriers, the mean crest factor value is 3.5, although the CF of a specific symbol can vary widely. Figure 2.11 shows the distribution of CF for 100,000 randomly generated symbols, and in rare cases, the CF can almost double the mean value. High CFs can cause implementation problems – which will be discussed shortly, in Section 2.5 – so practical systems limit the allowable phasor combinations in a single symbol to prevent too many carriers aligning in phase and causing large peaks. Another technique often used is to digitally clip the output of the IFFT such that signals with a CF greater than some value are hard clipped to reduce the CF. While this introduces errors into the transmitted information, the errors can often be corrected by error correction systems and anyway, the probability of very high peaks occurring is low.

The result of these CF limiting techniques is that for HomePlug AV, the CF limit is commonly around 4. It is useful to be aware of what a HomePlug AV signal looks like in the time and frequency domains as these views will be used in subsequent analysis and measurement. Figure 2.12 shows a 920 carrier symbol with each carrier using QAM-4

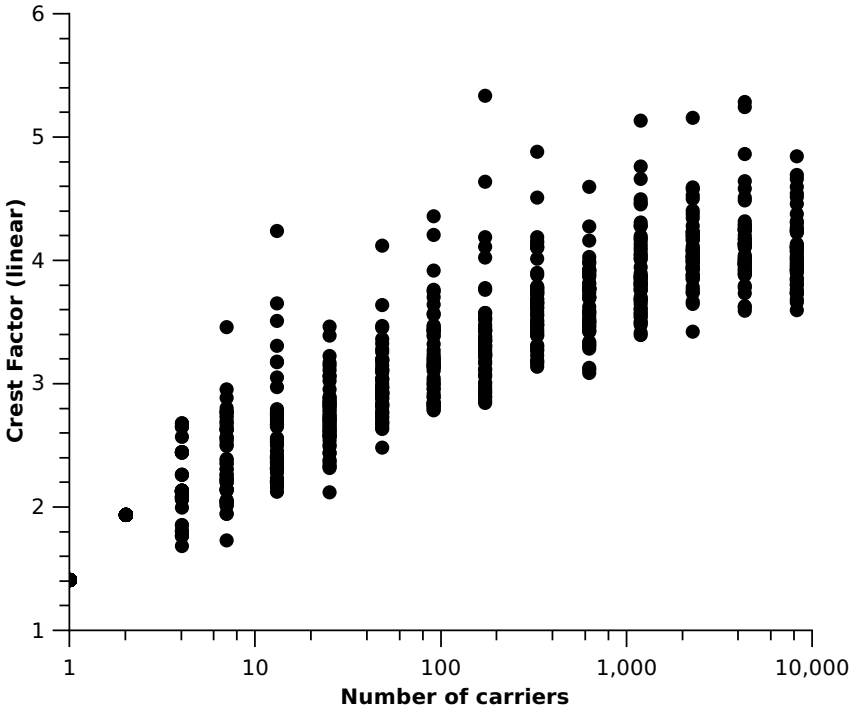

Figure 2.10: Scatter plot of OFDM Crest Factors for fifty randomly generated QAM-4 symbols, repeated for a selection of OFDM signal carriers.

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modulation, in the time domain. Figure 2.13 shows an FFT magnitude plot of the same symbol. A frequency domain plot in particular is a very common way of viewing the output of DMT systems.

2.5 Implementation challenges

Given a specification for a system such as HomePlug AV, one of the first implementation decisions to be made is which semiconductor technology (or technologies) should be used. The decision is driven by two factors: financial cost and technological feasibility. Economic considerations include the cost per die in a given technology and the revenue per part, and the expected market size. For PLC, these factors point towards fine-scale CMOS as appropriate technology and also suggest a single-technology, single-chip solution as this minimises cost.

In terms of technological feasibility, the use of digital-processing-intensive DMT modulation mean that PLC systems require considerable digital processing and computational capabilities, especially given the high data-rates involved. The large number of digital transistors required to implement this digital functionality will consume significant die

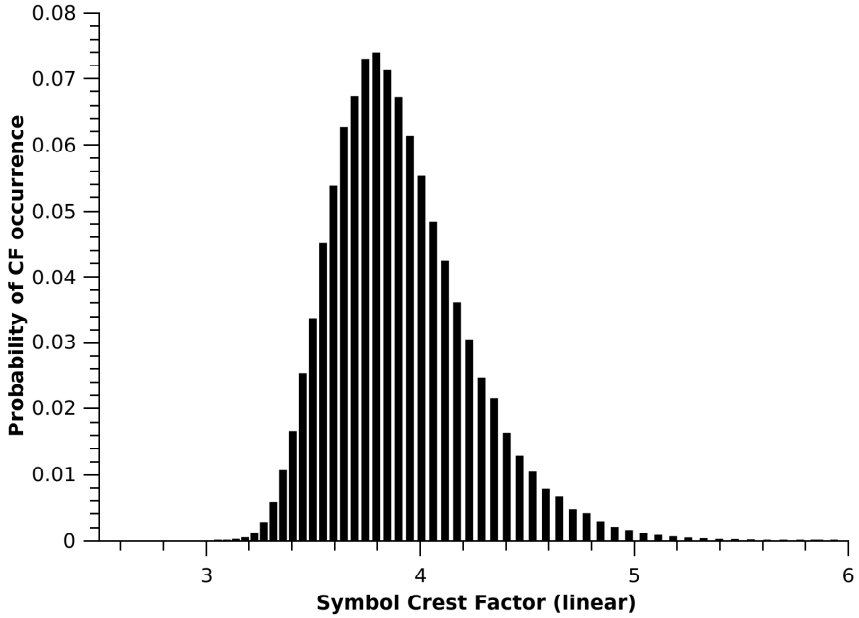

Figure 2.11: Histogram of CF of 920 carrier OFDM using QAM-4 modulation, repeated to randomly generate 100,000 symbols.

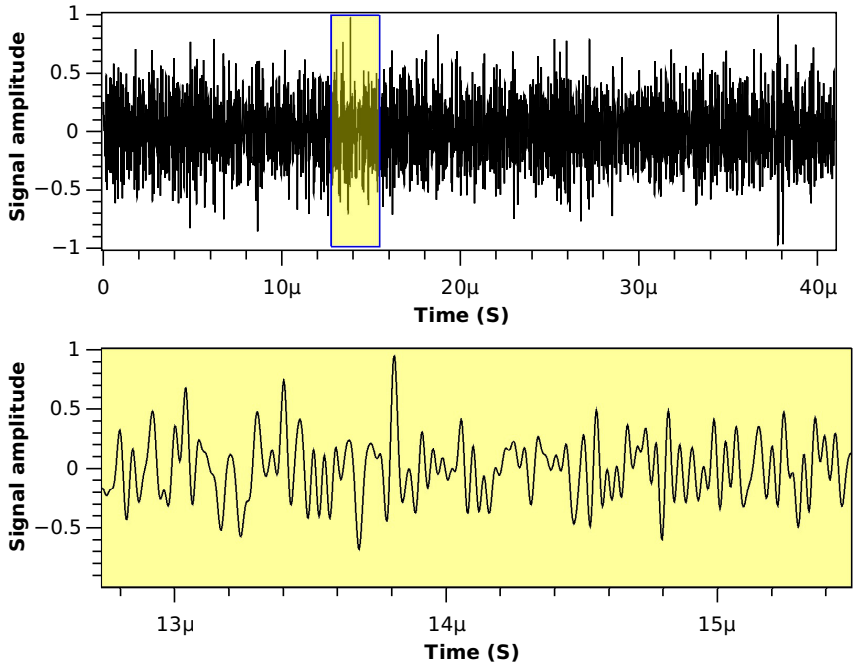

Figure 2.12: Time-domain representation of a real HomePlug AV symbol. The symbol shows large peaks where many carriers align in phase at a particular point in time. A second plot shows an enlarged part of the signal. Symbol data provided by Gigle Networks.

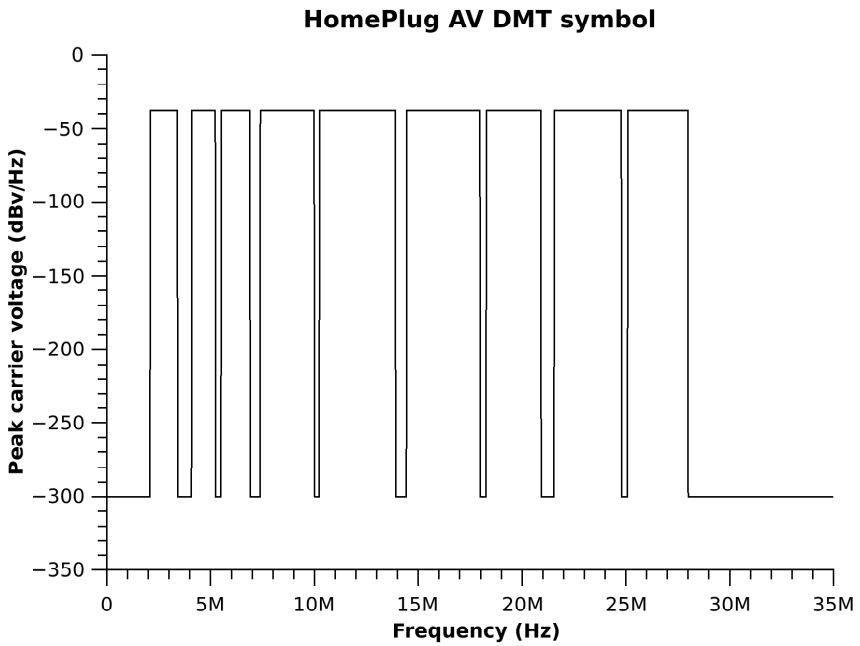

Figure 2.13: Frequency-domain magnitude representation of a HomePlug AV symbol, generated by performing an FFT on the time domain signal of Figure 2.12. The QAM-4 carriers are visible at approximately -39dBV/Hz, while all other values are -300dBV/Hz, which is the noise floor of the FFT implementation. The symbol is compatible with the EMC mask illustrated in Figure 2.3

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area, so to reduce production costs, it is desirable to use the finest resolution process possible. CMOS is the technology of choice for implementation of digital circuits and is used by state-of-the-art commercial PLC designs in 90nm[32] and 65nm[33] production processes.

Together, PLC standards such as HomePlug AV and modern high density, low cost digital CMOS manufacturing processes are capable of meeting the promise of the data-agile digital networked home. There are, however, many implementation challenges to be met in implementing a real PLC communication system. One challenge, that will be investigated here, involves the final stage in the transmit path, the power amplifier which drives the time domain OFDM signal onto the variable/low impedance powerline. This amplifier is usually referred to as a *line driver*.

The near-Shannon and adaptive operation benefits of OFDM modulation do not come for free; as discussed, the resulting time domain signal has a high CF and the linearity required of line driver is moderate; approximately 40dB. In addition, the line driver must be wide bandwidth and inject high power of the order of 30-100mW. This causes an efficiency problem for conventional line drivers where, as derived in Section 2.7, the line driver efficiency is often inversely proportional to the CF of the signal. With a high

CF and high injected power, efficiency is low and power consumption is high.

It is useful to briefly consider why efficiency is a concern here – after all, the HomePlug AV device is connected to the mains power network, so it has access to essentially unlimited power. However, low efficiency results in a large amount of power being dissipated as heat. Up to some level of dissipation, this can be dealt with by package conduction and convection, which allows for the cheapest and smallest end-product. However, beyond some level, heat-sinking and/or fans must be used to improve convective heat transfer to the external environment. This increases the cost and size of the overall networking solution, and could make it quite unattractive for an embedded consumer mass-market product. Additionally, fans increase the costs to the product developer who must very carefully design their units to ensure sufficient cooling.

Another motivation for improving efficiency relates to the cost of the power supply. Low efficiency and high power supply requirements mean that a larger power supply is required. This is typically manifested in a HomePlug AV system by physically larger capacitors and inductors which have higher component costs and require more PCB area.

Efficiency is also becoming increasingly important from a legislative point of view with regulations such as [34] which mandates standby power consumption of less than 0.5 Watt for consumer electronic devices. A typical use of a HomePlug AV transceiver would be embedded inside a consumer electronic device such as a television or home audio system. In both cases the 0.5 Watt power budget must be shared between many other components in addition to the HomePlug AV transceiver, all of which may be operating while the device is in standby. Low line driver efficiency can cause integration challenges for device manufacturers when attempting to meet these regulations.

Finally, it should be noted that line drivers are typically a significant power consumer in integrated communication systems[35]. It is thus reasonable that any work to reduce total system power consumption and heat dissipation should focus on improving the known low efficiency of the line driver.

The efficiency problems above increase the cost and complexity of the final HomePlug AV product, and decrease its marketability. There is considerable commercial interest in improving the efficiency of integrated wide band OFDM line drivers.

2.6 Metrics

The 2005 HomePlug AV (HPAV) specification provides the basis for this work. It defines the modulation and error coding systems which must be used in an HPAV system, and also the transmitter electrical specifications. The main metrics for line drivers which emerge from these specifications, and which will now be defined, are Missing Tone Power Ratio (MTPR)[3] and Injected power. Line driver efficiency will also be considered, and some information on intermodulation distortion will be given.

2.6.1 Third-order Intermodulation distortion

In many systems, the linearity and noise performance of the system is assessed using dynamic metrics such as SNR and SINAD. While these metrics are used in communication systems, it is more common to use multi tone metrics as, with single tone testing, any harmonics often fall out-of-band and so may not directly limit affect the performance of the system. Instead, a two-tone test signal, with tones at closely spaced frequencies f_1 and f_2, can be injected at the system input and the effect on the output spectrum is measured. Assuming a differential system, second order intermodulation components will be cancelled and so the next largest third-order intermodulation components are dominant. These fall at frequencies $2f_1 \pm f_2$ and $2f_2 \pm f_1$, where $2f_1 - f_2$ and $2f_2 - f_1$ are immediately adjacent to the input tones f_1 and f_2, so fall in band and are the dominant distortion mechanism. The ratio of the power of the tones $f_{1,2}$ to the third order intermodulation distortion components is given the name IM3.

2.6.2 Missing Tone Power Ratio

In a HPAV system, where hundreds or thousands of tones are transmitted simultaneously, intermodulation and harmonic distortion components are both created. However, multiple distortion/intermodulation components can fall at the same frequency and add, increasing the distortion at that frequency. In addition, noise will also be present. The total integrated distortion plus noise level will define the effective channel capacity as per Equation (2.1).

In order to see the cumulative effect of the distortion and noise components, OFDM carriers can be removed from the input signal, with carriers which are disabled being called “notched” carriers, or just “notches”. The power of a transmitted carrier can now

[3]Interchangeably referred to as Multi-Tone Power Ratio, although the description Missing Tone Power Ratio is more accurate.

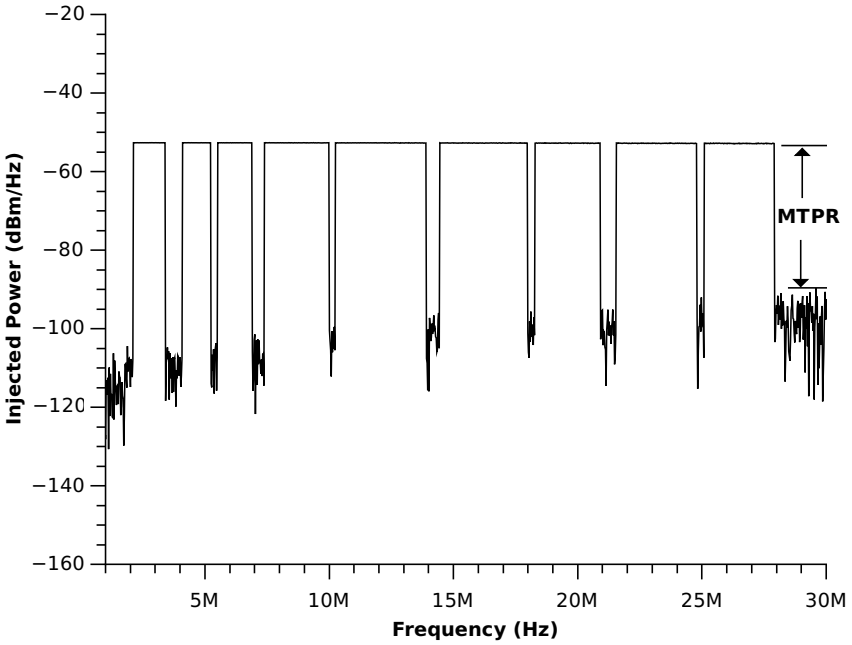

Figure 2.14: Output spectrum of a line driver, transmitting a HomePlug AV symbol. The ratio between the transmitted carrier power and the spectrum power where no signal is transmitted – in a "notch" – defines the Missing Tone Power Ratio. Here, the drawn MTPR is approximately 40dB and the worst-case MTPR occurring at the band edge at 28MHz, is approximately 35dB.

be compared to the power measured at the notch frequency and the ratio, expressed in dB, is called the Missing Tone Power Ratio (MTPR).

While the available literature[36, 37, 38] on MTPR measurement is clear on this aspect of MTPR measure, it is less clear on how to interpret the MTPR metric when there are many notched carriers. In this case, there will be one MTPR value for each notched carrier, but it is common to summarise all the MTPR results into one MTPR value for the signal. Some methods of doing this include taking the worst case MTPR value and using that as the MTPR value of the system, or to use an average of some or all of the individual MTPR values[36]. An example of a worst-case MTPR measurement is shown in Figure 2.14.

During the course of this work, and in conjunction with the Powerline design teams at Broadcom Europe, a number of additional MTPR metrics have been developed, by comparing MTPR values of signals to the results of a full vector decoding of the symbol – the reverse of the process described in Section 2.4 – and error vector magnitude calculation[39]. The basis of these metrics is to measure all of the notched carriers within the signal band and then report the MTPR value at a certain percentile. The most commonly used percentiles are the 50^{th} percentile, written as "pc50", and the 90^{th} percentile, written as "pc90".

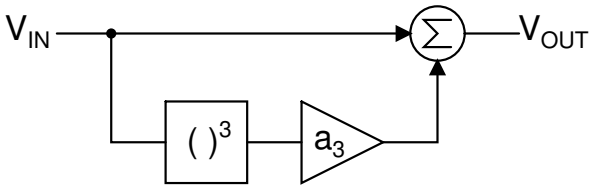

Figure 2.15: Model of a system with third order distortion. Coefficient a_3 is the third order distortion coefficient.

The pc50 metric is a particularly useful metric as it is found to be an accurate predictor of the EVM performance of a system. A real system will be transmitting a stream of data which, due to the coding and randomizing applied to the data before Digital-to-Analog conversion, will look like a random datastream. This results in randomly modulated carriers and so the intermodulation products are also randomly placed and vary from symbol-to-symbol – and hence the MTPR of a particular notch can vary from symbol-to-symbol. Due to the random nature of the intermodulated tones which determine the MTPR in each notch, the central limit theorem states that the MTPR values will have a normal distribution. The centre value of this distribution is the median value – or pc50 – of the MTPR across all notches.

Note that for HomePlug AV, where the emissions mask of Figure 2.3 already specifies bands of missing tones, suitable notched carriers already exist for MTPR measurement.

2.6.3 Relationship between MTPR and IM3

As discussed above in Section 2.6.1, the distortion components in a communication system are dominated by IM3, so the MTPR is related to the IM3 figure. However, in a multi-tone system such as HPAV where there are hundreds or thousands of carriers, multiple intermodulation components can land in the same notch frequency and add. There is no simple analytic relation between a particular MTPR value and an IM3 value, however it is possible to define an empirical relationship.

A general system with third order distortion can be modelled as shown in Figure 2.15, where an input signal V_{IN} is cubed, multiplied by a distortion coefficient a_3, and added to the original V_{IN} value. The output signal V_{OUT} then contains third order harmonic and intermodulation distortion components. A DMT signal with randomized transmission vectors can then be applied to the model and its pc50 MTPR measured. The MTPR will vary from symbol-to-symbol, so this is repeated a number of times and an average MTPR is taken. A sinewave with the same RMS amplitude as the DMT signal can then also be applied to the model and its IM3 measured. Finally, the whole process is repeated for a range of values of a_3. By comparing the MTPR and IM3 for each value of

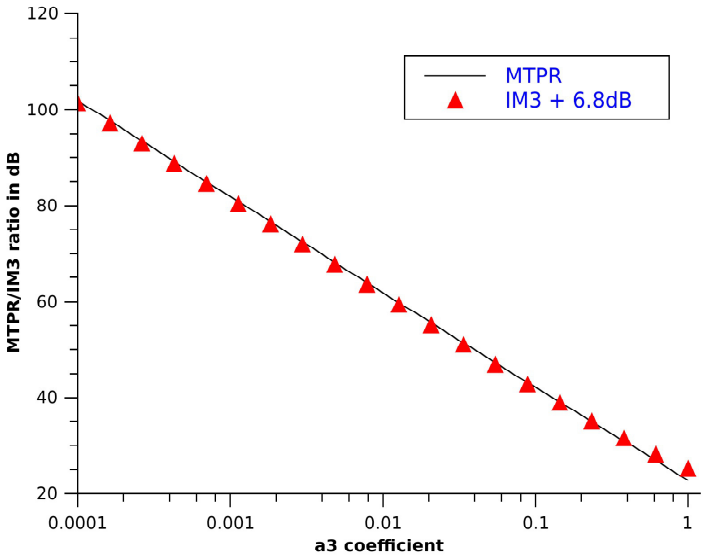

Figure 2.16: Relationship between MTPR and IM3. The graph shows a good match between the MTPR and IM3+6.8.

a_3, the following relationship, Equation 2.4, is observed. The raw data from the model is shown in Figure 2.16.

$$\text{MTPR} = \text{IM3} + 6.8\text{dB} \tag{2.4}$$

2.6.4 Injected power

In HomePlug AV, the power the line driver injects is limited by the EMC spectrum shown in Figure 2.3, using *dBm/Hz quasi-peak*. Line drivers inject a certain amount of power measured in Watts, so it is necessary to be able to convert from dBm/Hz quasi-peak to Watts. While dBm/Hz is a well known metric – the power relative to 1 mW in a 1 Hz bandwidth, specified in decibels – the quasi-peak metric is less common.

The quasi-peak value of a signal is measured by a quasi-peak detector, which uses a signal peak detector followed by a filter with programmable maximum rise rates and fall rates. The quasi-peak number is hard to measure in simulation as the time constants used mean that it integrates signal peaks over multiple symbols and also over multiple transmission cycles, so is dependent on transmission duty cycles and network activity. In order to simplify analogue circuit design, Gigle Networks have experimentally determined a quasi-peak-to-RMS conversion factor of -6dB. Thus, for an EMC limit of -50dBm/Hz quasi-peak, an RMS value of -56dBm/Hz should be used

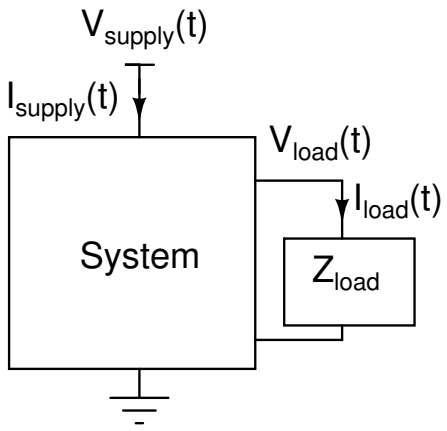

Figure 2.17: Black-box representation of a generic system with supply and load voltage and currents.

to ensure that the final end product operating normally as part of an active powerline transmission network will be close to, but not exceeding, the EMC limit.

Given the RMS power per Hertz, total power over the signal band can be calculated. For the 2-28MHz HPAV band, which includes 4MHz of notches at -86dBm/Hz which are not normally used for signal transmission, the power in Watts that is transferred into the powerline network – the "injected power" – is given by Equation (2.5).

$$\mathrm{P_{injected}} = 10^{\left(\frac{\mathrm{P_{dBm/Hz}}}{10}\right)} \times \mathrm{Bandwidth} \tag{2.5}$$

$$= 55mW \tag{2.6}$$

The injected power can also be related to a line driver peak voltage swing if the CF of the signal is known. The relationship is given by:

$$\mathrm{V_{swing\_peak}} = \mathrm{CF} \times \sqrt{\mathrm{P_{RMS}\,R_{load}}} \tag{2.7}$$

2.6.5 Efficiency

Efficiency is a measure of the power a system must dissipate in order to transfer power into a load. It is given as a percentage which specifies the ratio of power dissipated in the load, to the total power the system requires in order to achieve this, including the load power. For the general system shown in Figure 2.17, there are two terminals one

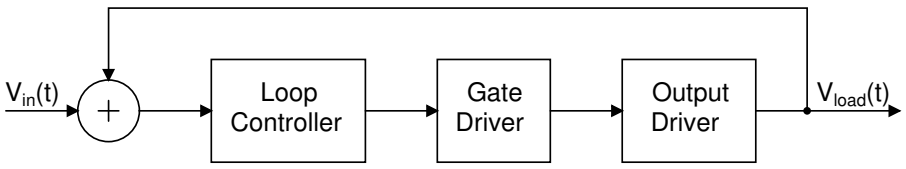

Figure 2.18: Common structure of a closed loop electronic line driver. The Loop Controller implementation varies; it could be a simple amplifier or a more complex modulator, depending on the intended operating principles of the line driver.

for a connection to a supply and a second for a connection to a load. The power taken from the supply, $\mathrm{P_{supply}}$ and the power transferred to the load $\mathrm{P_{load}}$ can then be used to calculate system efficiency over a measurement period T:

$$\mathrm{P_{supply}} = \frac{1}{T}\int_0^T \mathrm{I_{supply}}(t)\mathrm{V_{supply}}(t)\,\mathrm{d}t \tag{2.8}$$

$$\mathrm{P_{load}} = \frac{1}{T}\int_0^T \mathrm{I_{load}}(t)\mathrm{V_{load}}(t)\,\mathrm{d}t \tag{2.9}$$

$$\text{Efficiency} = \frac{\mathrm{P_{load}}}{\mathrm{P_{supply}}} \times 100\% \tag{2.10}$$

2.7 Amplifier classes

While much research has gone into power amplifiers over many decades, modern OFDM line drivers have only emerged into the mainstream around the year 2000, along with the development of the networked home and the falling costs of, and increased performance from, powerful digital CMOS processes. As such, while there are many possible amplifier implementations, not all are well suited to OFDM systems. This section will review the common amplifier types and will establish the fundamental efficiency limits. As amplifier efficiency usually depends on the signal being driven, as will be discussed below, it is necessary to define the signal which will be used in the efficiency analysis. Two signals have been chosen, a sine wave and a HomePlug AV DMT signal. Sine wave efficiency analysis, using output signals of the form $\mathrm{V_{DD}}\sin(t)$, is commonly used as the simple analytic expression for a sine wave permits straight forward mathematical manipulation in order to determine efficiency. Sine wave analysis also provides insight into why a particular type of amplifier is or is not efficient. The concepts developed during sine wave analysis can then be used to numerically compute the efficiency of a particular DMT signal, in this case the one presented earlier in Figures 2.12 and 2.13. One final piece of information which will be needed is the CF of the two signals. For the sine wave, it is $\sqrt{2}$, while for the DMT signal it is taken as 4.

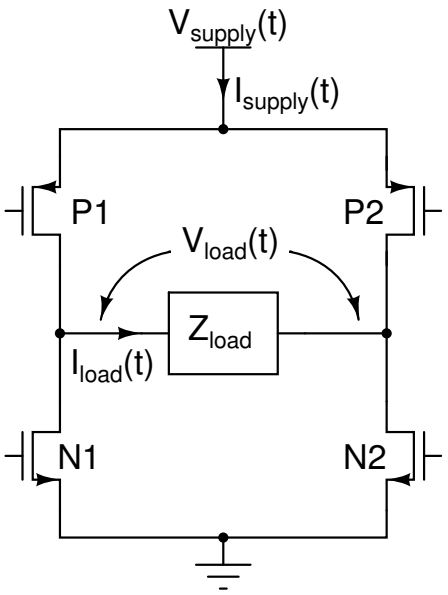

Figure 2.19: General differential output stage in an H-bridge configuration with differentially connected load impedance.

Figure 2.18 shows the general structure of a closed loop line driver. There is an input signal $V_{in}(t)$ and a feedback control loop which tries to force the amplifier output, $V_{load}(t)$, to be equal to the input signal. An Output Driver provides current to a load and a Gate Driver determines how the Output Driver should be controlled in order to achieve the output voltage defined by the Loop Controller, while trading off linearity, noise, power consumption and circuit simplicity, among other metrics. From the many different methods of driving the output driver, a number of fundamentally distinct general classes of Loop Controller and Gate Driver can be identified, and letters are used to describe an amplifier which belongs to a certain class, such as Class-A, Class-B or Class-H. Note that other amplifier implementations are possible but do not significantly affect the efficiency analysis.

In line drivers, the Output Driver is usually implemented based on the schematic of Figure 2.19, which implements a differential output stage. This is normal for line drivers in low voltage technologies as for a given supply voltage, this can achieve twice the signal swing across the load impedance, and so four times the injected power, versus a single ended output stage.

Devices P1 and P2 are shown as P-MOSFET devices and devices N1 and N2 are shown as N-MOSFET devices as these are common implementations, but it should be noted that other arrangements and device types are possible without affecting the validity of the analysis. Further, to simplify the analysis it will be assumed that all devices can act as ideal voltage-controlled current sources, where the output current depends on the gate voltage but not on the drain voltage. The aim here is to establish

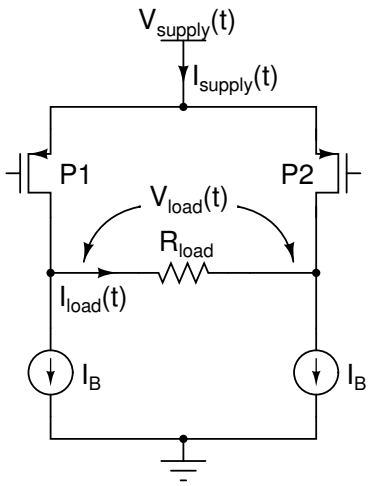

Figure 2.20: Class-A output stage schematic.

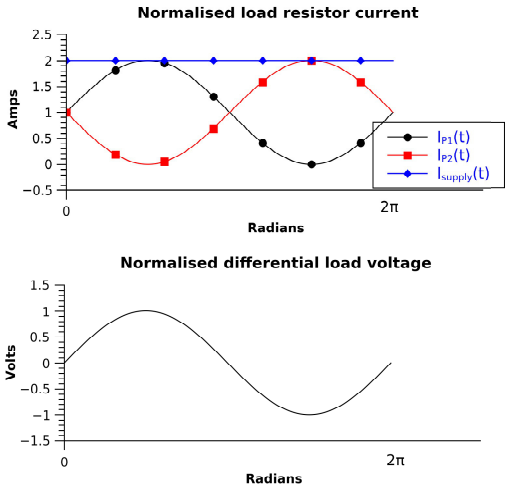

Figure 2.21: Class-A output stage current and voltage waveforms.

the fundamental efficiency limits of the architecture, not the efficiency limits of a particular implementation with a particular device type which has a particular minimum drain-source voltage requirement.

Finally, the notation to be used must be clarified. $\mathrm{V}_x(\mathrm{t})$ refers to a time varying voltage on node x, while V_x is the average of voltage x over some measurement period and finally $\mathrm{V}_{x_{\mathrm{RMS}}}$ is the RMS value of voltage x over the measurement period. The same notation is used for current signals of the form $\mathrm{I}_x(\mathrm{t})$, I_x and $\mathrm{I}_{x_{\mathrm{RMS}}}$.

2.7.1 Class-A

Figure 2.20 shows a Class-A H-bridge output stage with resistive load $\mathrm{R}_{\mathrm{load}}$. Transistors P1 and P2 vary the current from the supply that reaches the terminals of $\mathrm{R}_{\mathrm{load}}$, subject to the criteria enforced by the current sources that the total current from the supply is always $2\mathrm{I}_{\mathrm{B}}$, as shown in Figure 2.21.

To determine the efficiency of the amplifier, Equation 2.10 can be used if $\mathrm{P}_{\mathrm{load}}$ and $\mathrm{P}_{\mathrm{supply}}$ are known. Assuming the gates of P1 and P2 are modulated so that the differential output, $\mathrm{V}_{\mathrm{load}}$, is a sine wave with peak voltage V_{DD} as in Equation 2.11.

$$\mathrm{V}_{\mathrm{load}}(t) = \mathrm{V}_{\mathrm{DD}} \sin(t) \tag{2.11}$$

Using the definition of Crest Factor from Equation 2.2, $\mathrm{V}_{\mathrm{load}_{\mathrm{RMS}}}$ can be calculated.

$$\mathrm{V}_{\mathrm{load}_{\mathrm{RMS}}} = \frac{\mathrm{V}_{\mathrm{DD}}}{\mathrm{CF}} \tag{2.12}$$

Now P_{load} can be determined:

$$P_{load} = \frac{V^2_{load_{RMS}}}{R_{load}} = \frac{{V_{DD}}^2}{CF^2\, R_{load}} \tag{2.13}$$

From inspection of Figure 2.21, it can be seen that the total current from the positive supply is determined by the two current sources, so I_{supply}=$2I_B$. The minimum value of I_B which allows a full scale sine wave to be driven into the load is $I_B = \frac{V_{DD}}{R_{load}}$. Also, the supply voltage is a fixed DC voltage, so $P_{supply} = I_{supply}V_{supply}$. Therefore, the efficiency of a Class-A output stage can be derived as in Equation 2.14.

$$\text{Efficiency}_A = \frac{P_{load}}{P_{supply}} = \frac{{V_{DD}}^2}{CF^2 R_{load}} \frac{1}{2I_B V_{DD}} = \frac{{V_{DD}}^2}{CF^2 R_{load}} \frac{R_{load}}{2{V_{DD}}^2} = \frac{1}{2CF^2} \tag{2.14}$$

Substituting in the CF of sine wave and DMT signals, the efficiencies for the two types of signal can be found.

$$\text{Efficiency}_{A_{sine}} = 25\% \tag{2.15}$$

$$\text{Efficiency}_{A_{DMT}} = 3.125\% \tag{2.16}$$

Due to the low efficiency, Class A biasing is normally only used where efficiency is not a concern. However, it is very linear with a simple biasing scheme and for these reasons is used widely for amplifiers which drive small loads.

2.7.2 Class-B

Unlike Class-A biasing, the Class-B biasing shown in Figure 2.22 uses no quiescent current. Instead, P1 and P2 force current into the terminals of R_{load} while N1 and N2 pull current out of the terminals of R_{load}. With appropriate gate control on P1 and N2 while P2 and N1 are off, a current can be directed through R_{load}. The opposite current can be achieved with corresponding gate control of P2 and N1 while P1 and N2 are off.

The efficiency calculation starts with Equation 2.10. The power dissipated in R_{load} is still described as in Equation 2.13. The power from the supply can be written in terms of average values:

$$P_{supply} = I_{supply}V_{supply} \tag{2.17}$$

The supply is a DC voltage source so V_{supply}=V_{DD}. The supply current will be a rectified version of $I_{load}(t)$ and can be expressed in terms of the average voltage across the load, as in Equation 2.18. The average of the rectified load voltage is written as

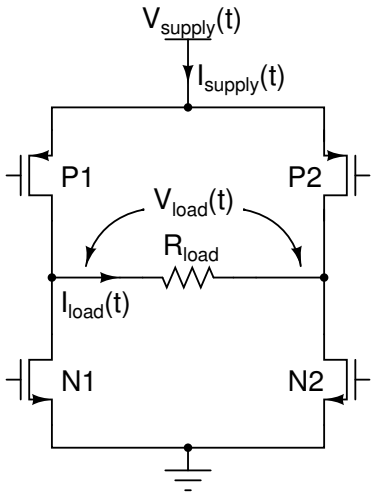

Figure 2.22: Class-B output stage schematic.

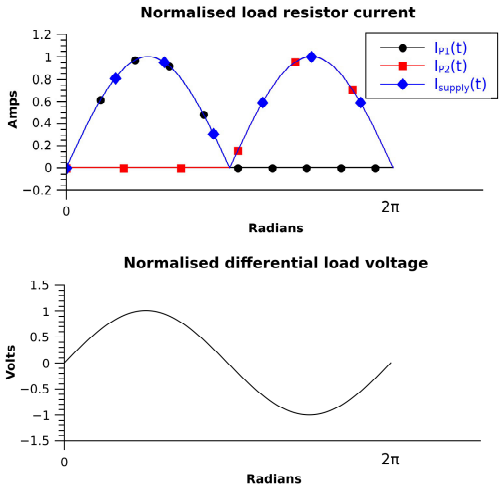

Figure 2.23: Class-B output stage current and voltage waveforms.

$V_{load_{rect}}$.

$$I_{supply} = \frac{1}{T}\int_0^T |I_{load}(t)|\,dt = \frac{1}{R_{load}}\frac{1}{T}\int_0^T |V_{load}(t)|\,dt = \frac{1}{R_{load}} V_{load_{rect}} \tag{2.18}$$

The efficiency of Class-B can then be determined using Equation 2.13 for P_{load} and Equation 2.17 for P_{supply}. The equation has been simplified by normalising the rectified load voltage by the supply voltage using using the following substitution.

$$V_{load_{rectnorm}} = \frac{V_{load_{rect}}}{V_{DD}} \tag{2.19}$$

Class-B efficiency is then given by

$$Efficiency_B = \frac{P_{load}}{P_{supply}} = \frac{{V_{DD}}^2}{CF^2\, R_{load}} \frac{R_{load}}{V_{load_{rectnorm}}\, {V_{DD}}^2} = \frac{1}{CF^2\, V_{load_{rectnorm}}} \tag{2.20}$$

For a sine wave $V_{load_{rectnorm}}$ can be determined analytically and has value $\frac{2}{\pi}$. For DMT signals there is no simple analytical solution, but the average rectified value can easily be computed numerically for a given waveform. For the DMT signal here, the normalised rectified load voltage is 0.2. The final efficiency result is given below.

$$Efficiency_{B_{sine}} = 78.5\% \tag{2.21}$$

$$Efficiency_{B_{DMT}} = 31.1\% \tag{2.22}$$

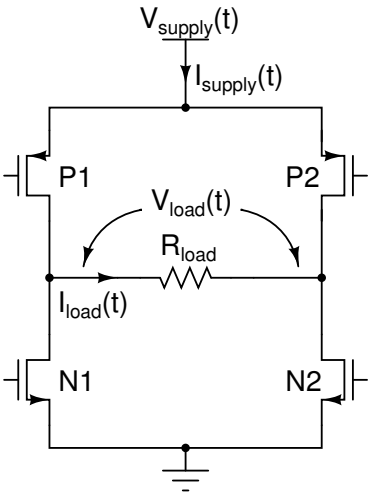

Figure 2.24: Class-AB output stage schematic.

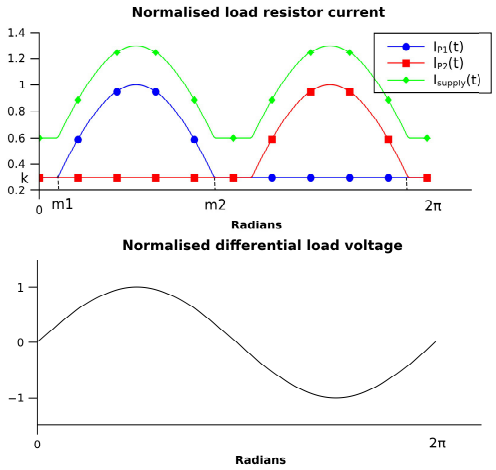

Figure 2.25: Class-AB output stage normalised current and voltage waveforms shown over one cycle of a sine wave output signal. The quiescent level I_Q is denoted with the letter k. X-axis values m1 and m2 are integration limits.

2.7.3 Class-AB

While Class-B offers a significant efficiency improvement over Class A, it does so at the cost of increased crossover distortion. Crossover distortion is increased distortion at the point when the output signal crosses the x-axis and the load current carrying devices swap from P1 and N2 to P2 and N1, or vice-versa and is caused mainly by gate channel charging and discharging when the devices turn on or off, and also to a lesser extent by imperfect transitions from one set of output devices to another set of output devices due to gate drive asymmetry or device mismatch. To reduce the distortion level, the output devices can be biased with a small quiescent current, I_Q, so that one device is always on, and both are not off for zero signal. This scheme is illustrated in Figure 2.25. When the load current is less than I_Q, the output stage acts as a Class-A and when the load current is larger than I_Q, the output stage acts as a Class-B. To simplify the analysis, it is assumed that the quiescent current never drops below the level defined by I_Q, although it can in certain implementations.

The schematic of a Class-AB output stage shown in Figure 2.24 is identical to that of the Class-B shown in Figure 2.22, the difference between the two is how the gates of P1, P2, N1 and N2 are driven in order to maintain a minimum current rather than allowing the current to fall to zero.

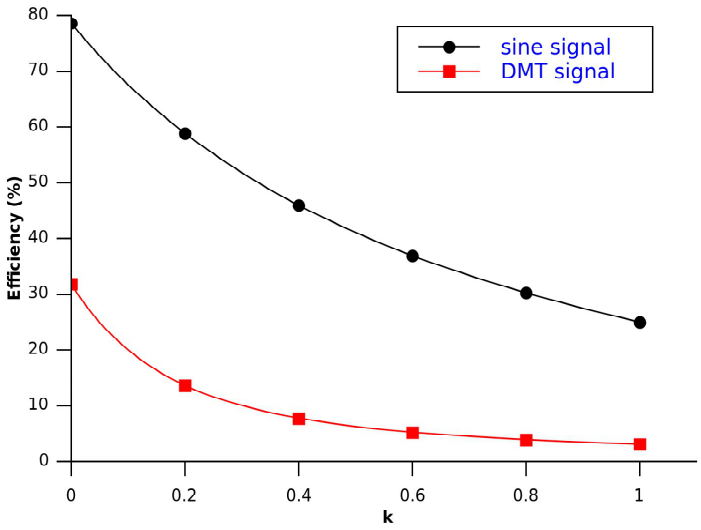

Figure 2.26: Efficiency of a Class-AB amplifier as a function of k.

The efficiency can be determined using Equations 2.10, 2.13 and 2.17 as shown in Equation 2.23.

$$\text{Efficiency}_{\text{AB}} = \frac{{\text{V}_{\text{DD}}}^2}{\text{CF}^2\,\text{R}_{\text{load}}}\frac{1}{\text{I}_{\text{supply}}\,\text{V}_{\text{DD}}} \tag{2.23}$$

For a sine wave, I_{supply} can be computed analytically by integrating the three separate regions of $\text{I}_{\text{P1}}(t)$ depicted in Figure 2.25; $0 \rightarrow \text{m1}$, $\text{m1} \rightarrow \text{m2}$ and $\text{m2} \rightarrow 2\pi$. After summing and dividing by 2π to find the average current then multiplying by 2 to account for the supply current flowing through I_{P2}, which is symmetric with the load current of I_{P1} about π, an expression for I_{supply} can be obtained, Equation 2.24. It is also useful to define a variable $\text{k} = \frac{\text{I}_{\text{Q}}}{\text{I}_{\text{load}_{\text{max}}}}$, where $\text{I}_{\text{load}_{\text{max}}}$ is the peak value of the load current.

$$\text{I}_{\text{supply}} = \frac{\text{V}_{\text{DD}}}{\text{R}_{\text{load}}}\frac{1}{\pi}(-\cos(\pi - \sin^{-1}(\text{k})) + \cos(\sin^{-1}(\text{k})) + 2\text{k}\sin^{-1}(\text{k}) + \text{k}\pi) \tag{2.24}$$

Thus, efficiency of the AB stage for a sine wave output signals is:

$$\text{Efficiency}_{\text{AB}} = \frac{1}{\text{CF}^2}\frac{\pi}{(-\cos(\pi - \sin^{-1}(\text{k})) + \cos(\sin^{-1}(\text{k})) + 2\text{k}\sin^{-1}(\text{k}) + \text{k}\pi)} \tag{2.25}$$

Equation 2.25 has been evaluated over the range of k in Figure 2.26. Equation 2.23 has also been evaluated numerically for DMT signals over the range of k, and the results also plotted in Figure 2.26. As expected, the efficiency curves converge on the efficiency results for Class-A output stages when k=1, and on the results for Class-B output stages when k=0.

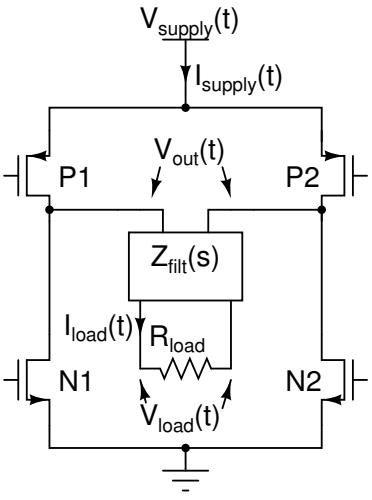

Figure 2.27: Class-D output stage schematic.

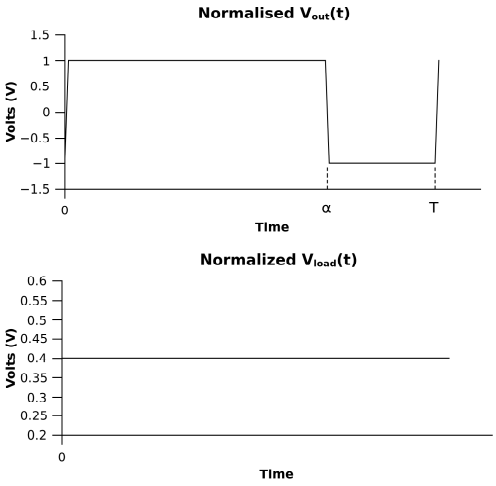

Figure 2.28: Class-D amplifier normalized voltage waveforms.

It is common to use Class AB amplifiers with k $\approx$ 0.1. In this situation there is a significant efficiency benefit versus Class-A while having much better distortion performance than Class-B. As such, Class AB biasing is used widely for power amplifiers which need good linearity and good efficiency.

2.7.4 Class-D

The amplifier classes discussed so far all work by creating an output voltage which is linearly proportional to an input voltage. An alternative is to encode the input voltage information in the edge-positions of a high frequency pulse-width modulated rail-to-rail square wave, such that the low frequency part of the square wave contains the frequency content of the input signal, while the high frequency part of the square wave contains high frequency switching components. The transistors in the output stage, shown in Figure 2.27, all operate as switches. To obtain a positive voltage at $\mathrm{V_{out}}(t)$, P1/N2 are turned on and P2/N1 are turned off, and for a negative $\mathrm{V_{out}}(t)$, the switch states are inverted. If a lossless inductor-capacitor (LC) filter, shown as a $\mathrm{Z_{filt}}(s)$ block, is then connected to the output stage to remove the high-frequency square wave harmonics, only the low-frequency amplifier input signal will remain at $\mathrm{V_{load}}(t)$. The efficiency of Class-D can now be analysed. Unlike the analyses above, the focus here will be on DC signals but will conclude by determining the implications for non-DC signals.

Assuming filter $\mathrm{Z_{filt}}(s)$ completely removes the high frequency harmonics of the pulse-width modulated square wave, the only signal left at $\mathrm{V_{load}}(t)$ would be the low frequency input signal. Note that incomplete removal of high frequency switching harmonics – due to finite filter roll-off – complicates the analysis but does not alter the final result.

A DC modulator input signal will be assumed, which after normalisation results in the waveforms shown in Figure 2.28. $V_{out}(t)$ can be related to the average load voltage V_{load} using the duty cycle variables α and T shown in Figure 2.28, as in Equation 2.26.

$$V_{load} = \left(\frac{2\alpha}{T} - 1\right) V_{DD} \tag{2.26}$$

As $Z_{filt}(s)$ is assumed to remove all high frequency switching energy, I_{load} must also flow through P1 and N2 when $V_{out}(t)$ is high and P2 and N1 when $V_{out}(t)$ is low. In this example, the implication is that when $V_{out}(t)$ is negative, current I_{load} flows *in to the supply*. This is the critical point in Class-D efficiency analysis. This behaviour is made possible by the inductive elements inside $Z_{filt}(s)$ as they will oppose fast current changes so over for a short period, much less than the filter time constant, they will continue to force I_{load} after the polarity of $V_{out}(t)$ reverses, even if that means I_{load} must be forced back into the supply.

Using Equations 2.17, 2.26 and Figure 2.28, and assuming the maximum value of V_{load} is V_{DD}, P_{supply} and P_{load} can now be determined.

$$\begin{aligned}
P_{supply} &= I_{supply} V_{supply} && (2.27)\\
&= \frac{1}{T}\int_0^T I_{supply}(t)\, V_{DD}\, dt && (2.28)\\
&= \frac{V_{DD}}{T}\left(\int_0^{\alpha} I_{load}\, dt + \int_{\alpha}^{T} -I_{load}\, dt\right) && (2.29)\\
&= V_{DD}\, I_{load}\left(\frac{2\alpha}{T} - 1\right) && (2.30)\\
P_{load} &= I_{load}\, V_{load} && (2.31)\\
&= V_{DD}\, I_{load}\left(\frac{2\alpha}{T} - 1\right) && (2.32)
\end{aligned}$$

The efficiency of Class-D can now be found using Equations 2.10, 2.30 and 2.32.

$$\text{Efficiency}_D = 100\% \tag{2.33}$$

As this efficiency result has no dependency on signal level, it is applicable to both the sine wave and DMT signals used above.

2.7.5 Class G

The amplifier classes above have all taken output current from a single supply, V_{DD}. If an additional supply is available with a value $V_{DD_{LOW}} = mV_{DD}$ where m is a real value

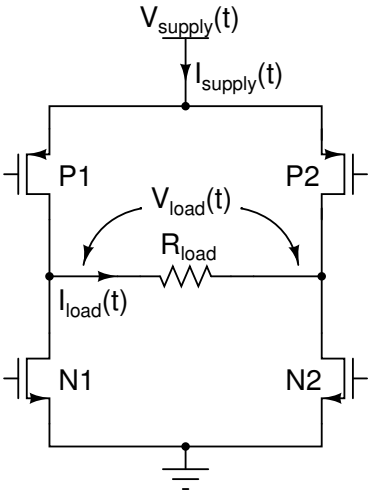

Figure 2.29: Class-G output stage schematic.

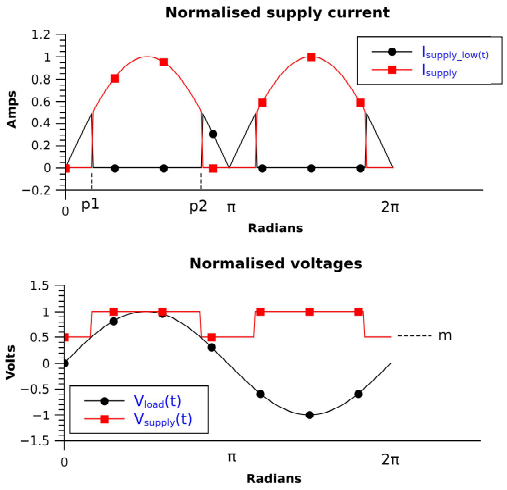

Figure 2.30: Class-G amplifier normalised supply/load voltages and supply current waveforms. When the signal exceeds m, $V_{supply}(t)$ rises to its maximum value.

between 0 and 1, then the Class A, AB and B architectures can be used in conjunction with a supply switching scheme. For output signal values below mV_{DD}, current is taken from the mV_{DD} supply while for output signals values above m V_{DD}, current is taken from the V_{DD} supply.

Figure 2.29 shows the structure of a Class G amplifier – it is almost identical to a Class B amplifier structure, with the one difference being that here, $V_{supply}(t)$ is load-dependent. As this section aims to determine efficiency limits of different structures, this analysis will proceed assuming the Class G supply scheme is used in conjunction with Class B amplifier output device biasing as this is the most efficient of the non-switching biasing schemes discussed. The corresponding waveforms for a Class B biased Class G supply scheme are shown in Figure 2.30.

The general form of the Class G efficiency equation is given in Equation 2.34, using Equations 2.10 and 2.13.

$$\text{Efficiency}_G = \frac{{V_{DD}}^2}{CF^2\, R_{load}} \frac{1}{I_{supply}\, V_{DD} + I_{supply\_low}\, m\, V_{DD}} \tag{2.34}$$

I_{supply} is the average current taken from the V_{DD} supply and I_{supply_low} is the average current taken from the $V_{DD_{LOW}}$ supply. For a sine wave output signal where $I_{load}(t) = \frac{V_{DD}}{R_{load}} \sin(t)$, these can be found using the integrals in Equations 2.35 and 2.36 with the

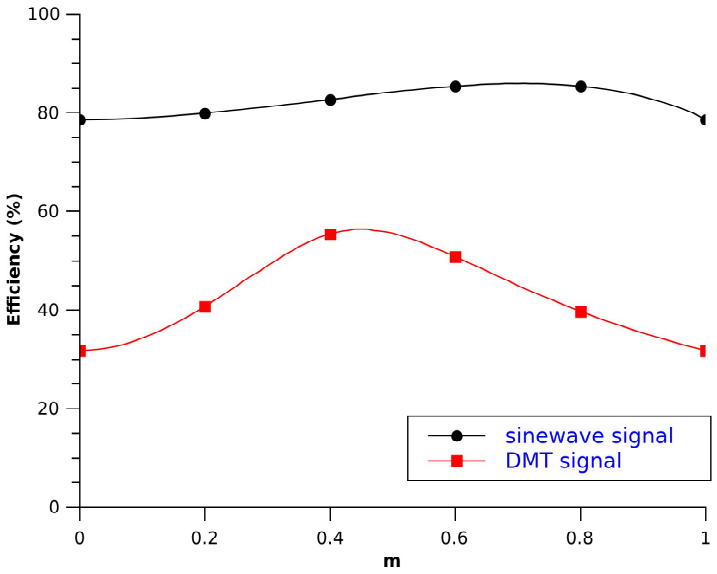

Figure 2.31: Efficiency of a Class G amplifier as a function of m.

limits p1= $\sin^{-1}(\mathrm{m})$ and p2= $\pi - \sin^{-1}(\mathrm{m})$.

$$\mathrm{I}_{\mathrm{supply}} = \frac{1}{\pi}\int_{p1}^{p2} \mathrm{I}_{\mathrm{load}}(t)\,\mathrm{d}t \tag{2.35}$$

$$\mathrm{I}_{\mathrm{supply\_low}} = \frac{2}{\pi}\int_{0}^{p1} \mathrm{I}_{\mathrm{load}}(t)\,\mathrm{d}t \tag{2.36}$$

By inserting Equations 2.35 and 2.36 into Equation 2.34, the efficiency of Class G with Class B biasing can be found for a sine wave output signal. Using numerical integration of the DMT waveform, the efficiency for the reference DMT signal can also be found. The results are plotted in Figure 2.31 over the range of possible values for m. It is observed that Glass G significantly improves the efficiency of the output stage when driving DMT signals, versus Class AB.

Note that Class G can also involve more than two supply levels but the additional efficiency improvement reduces as the number of supplies increase. There is also the issue of where all of the supplies would come from - if they are down-regulated from a higher supply, the regulators will need to be highly efficient to gain any system-level efficiency benefit from Class-G.

2.7.6 Class H

Class H uses the same structure as Class G, as shown in Figure 2.32, and the biasing is similar to Class G in that it varies the output stage supply as a function of the amplifier

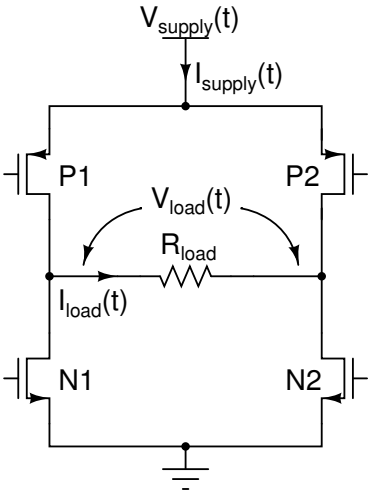

Figure 2.32: Class-H output stage schematic.

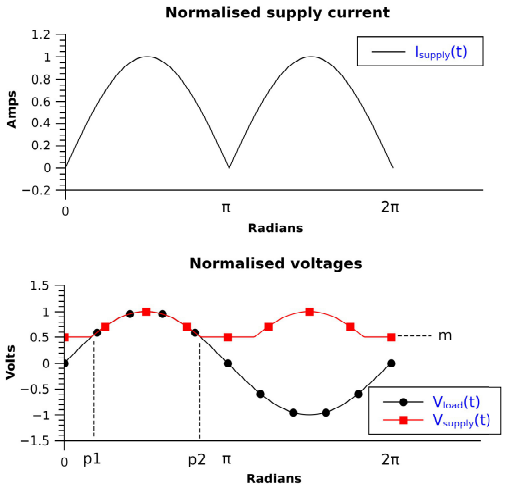

Figure 2.33: Class-H amplifier normalised supply/load voltages and supply current waveforms. When the absolute value of output voltage exceeds m, $V_{supply}(t)$ starts tracking the output voltage.

input signal. However, rather than stepping the output stage supply voltage between discrete levels as in Class G, Class H systems make the output stage supply rail track the output signal when the output signal is above some level, as in Figure 2.33. In the subsequent discussion, as in the Class-G discussion, Class-B biasing of the output devices is assumed.

The power from the supply can be computed by expanding Equation 2.17 and solving for the waveforms in Figure 2.33, using p1=$\sin^{-1}(m)$ and p2=$\pi - \sin^{-1}(m)$.

$$P_{supply} = \frac{1}{2\pi}\int_0^{2\pi} I_{supply}(t)V_{supply}(t)\,dt \tag{2.37}$$

$$= \frac{1}{R_{load}\pi}\int_{p1}^{p2} {V_{load}}^2(t)\,dt + \frac{2}{R_{load}\pi}\int_0^{p1} V_{load}(t)\,m\,V_{DD}\,dt \tag{2.38}$$

$$\tag{2.39}$$

Equation 2.38 can be solved for a sine wave load signal of the form $V_{load}(t) = V_{DD}\sin(t)$, and with Equations 2.10 and 2.13, the Efficiency of a sine wave can be calculated as in Equation 2.40.

$$\text{Efficiency}_{A_{sine}} = \frac{\pi}{CF^2}\,\frac{1}{\left[\frac{t}{2} - \frac{\sin(2t)}{4}\right]_{p1}^{p2} + \left[-2\cos(t)\right]_0^{p1}} \tag{2.40}$$

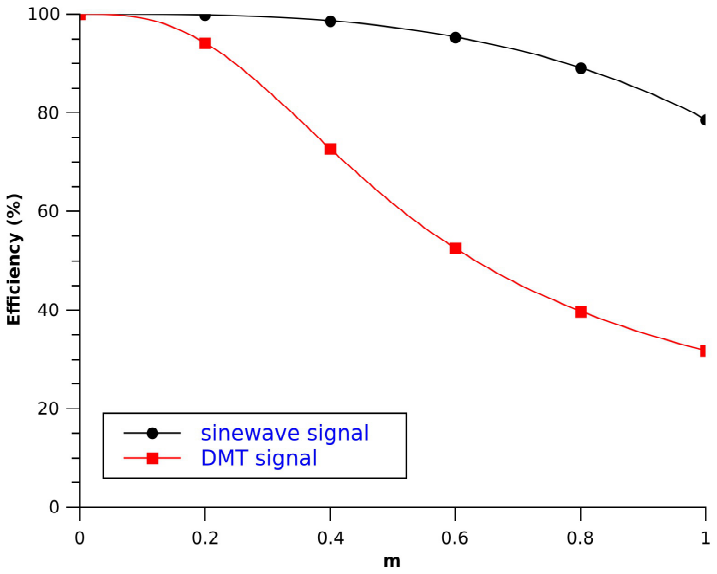

Figure 2.34: Efficiency of a Class H amplifier as a function of m.

The efficiency plots of Class H are shown in Figure 2.34, for the sine wave and reference DMT signal. While Class H can achieve very high efficiency with low values of m, low values of m correspond to a supply voltage which tracks the desired output signal over most of the signal period. The regulator which produces this supply will need to be very efficient and have a wide bandwidth in order to follow the signal – but this is just pushing the efficiency problem from the output stage into the supply, it is not solving the output stage efficiency problem. For higher values of m and with signals with a high CF – so that signal peaks are relatively rare – it is possible to temporarily bootstrap the Class-B supply just to accommodate signal peaks. This supply bootstrapping will only work for a short period until the bootstrap capacitors have discharged, after which the Class H supply will collapse. However, the efficiency can be improved modestly versus the basic Class B efficiency if the conditions above, high CF and high m, are met.

2.7.7 Other classes

A number of other amplifier classes exist, however these are either not relevant to this work or they build on the classes above and so will not be covered separately here. Classes C, E and F are similar to Class B in terms of schematic structure, but they are intended for single carrier systems and work by clipping parts of the signal in order to ensure that the output devices are only conducting for parts of the signal when the voltage across the output devices is small. This increases the CF of the signal by turning off the output stage when the output signal value is low, and so improves efficiency. The distortion that is introduced by clipping the signal can be filtered or controlled

using a resonant LC structure, tuned to the single carrier frequency.

Other classes of amplifier such as Class K involve using multiple amplifiers in parallel – such as a Class D output stage in parallel with a Class AB output stage, where the Class D provides most of the signal current with a high efficiency and the Class AB cancels any distortion added by the Class D. The efficiency limit of these structure is very much determined by the specific implementation, but will build on the results above.

2.8 Literature survey

2.8.1 Overview

The main amplifier classes have been described in Section 2.7 from a theoretical perspective. Now a survey of relevant published power amplifiers will be given, and relevant literature is found in three main areas. Portable audio is the first; systems must process audio signals which have high crest factors around 5, but a desire to maximise battery life means that power dissipation in the amplifier must be minimised. Wireless communication systems – the second area – are emerging which use modulation schemes such OFDM. Again, a high crest factor is present and, especially in portable wireless applications, power dissipation must be minimised.

The third area, and the one around which this project is based, is wireline communication systems using DMT modulation. Of notable relevance are DSL central-office line drivers, which process DMT signals. The limit on how many DSL lines can be terminated in a single office is determined by the power and thermal requirements of the DSL Analogue Front End (AFE). In order to maximise the number of lines served by a single DSL exchange, the power dissipation of the line driver should be minimised as the line driver often accounts for more than 60% of total system power dissipation[40].

Additional literature of relevance exists relating to ISDN, Ethernet and analogue video line drivers. However, the above three areas cover the state-of-art in the field and they are representative of the techniques in use.

2.8.1.1 Class A/B/AB/G/H

Class AB designs typically show efficiencies from 5-15%[41, 42, 43], although this is heavily influenced by the crest-factor of the signal being driven so results from different

applications can not easily be compared. To overcome the CF problem, Class-G or Class-H structures are used[44, 45, 46], and these can improve efficiencies to approximately 20%.

Class-H structures are also very well known from wireless power amplifier systems where they have a long history in polar modulation and envelope tracking/elimination and restoration systems, for example [47, 48, 49].

Various implementations of class H systems are possible and the specific implementation determines whether the technique will be called class H or polar modulation. A switching amplifier is usually used to generate a modulated supply rail for the output stage. Use of a linear output stage eg. [50] will then result in the system being called class H whereas use of an RF style output stage will result in the system being termed polar modulation or similar.

2.8.1.2 Class D

Class D wireline drivers are a relatively unexplored area, although the techniques used are well understood from audio, where class D is commonly used and actively researched. However, the design of switching class D line drivers includes additional challenges compared to audio, most significantly the wider bandwidth of communication systems compared to audio bands, but also the requirements of line termination and duplex signalling[51].

Switching class D line drivers generally have some form of modulator followed by a class D output stage and modulation techniques of interest include: synchronous sigma-delta (SD)[52], asynchronous/self-oscillating sigma-delta (SO-SD)[53, 54] and pulse width modulation[55].

Synchronous sigma-delta modulators quantize the input signal in time and amplitude, so introduce harmonics of the input signal to the output spectrum. In audio applications, where SD modulators are widely used, the narrow audio bandwidth allows the use of high oversampling ratios without approaching the physical technology limitations which become apparent when switching at high frequency. However, attempting to use an audio SD modulator architecture in a communications application, requires increasing the bandwidth – hence sample rate – by a factor of around 1500[4]. The resulting sample rate is too high for current CMOS processes, so modifications must be made to the basic sigma-delta architecture to reduce the required oversampling ratio.

[4] Assuming a 30MHz communication channel bandwidth versus a 20kHz audio bandwidth.

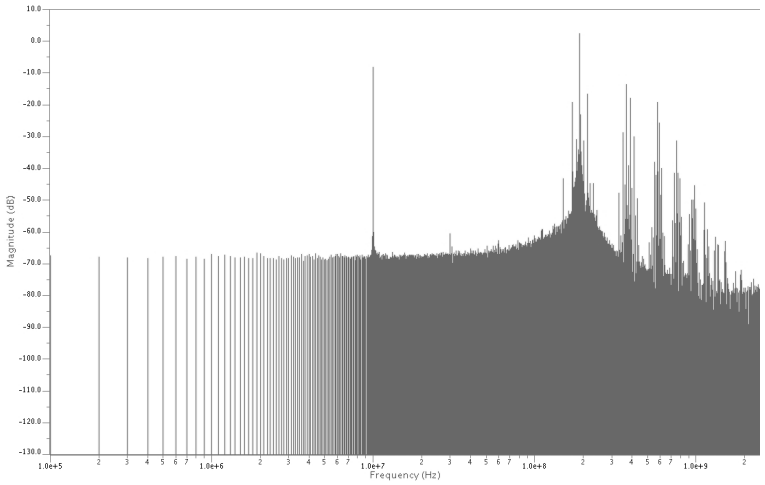

Figure 2.35: Self-oscillating modulator output spectrum with 10MHz sinusoid input signal.

Asynchronous/self-oscillating modulators, a type of hysteresis modulator[56], are well-known in control engineering but have not been widely used in communication or audio applications until relatively recently. They are similar to single-bit synchronous sigma-delta modulators, but the (usually single-bit) quantizer clock is removed. The resulting system will exhibit a high frequency oscillation known as a *limit cycle*. The oscillation frequency is determined by the loop phase response which, in turn, is usually determined by the amount of comparator hysteresis, loop delay and the integrator bandwidth.

A modulation technique which takes advantage of this limit cycle is continuous duty-cycle modulation[54], where amplitude information is converted into time information in the form of discrete-amplitude but continuously varying pulse widths. The signal can then be amplified using a high-efficiency class D output stage.

Forcing the external input of a single-bit self-oscillating modulator which is experiencing a limit cycle oscillation will modulate the input signal onto the limit cycle, in a process involving the limit cycle dithering the input signal[53]. In the frequency domain, shown in Figure 2.35, the modulator output will consist of the forcing signal at low frequency and the limit cycle, modulated by the forcing signal, at high frequency. Harmonics of the input signal, and the limit cycle, are also visible, although all high frequency out-of-band content can be removed by filtering.

The advantage of self-oscillating modulators over their synchronous counterparts is that they add no quantization noise to the output signal as the system is continuous time and not quantized, so much lower oversampling ratios are required for a given linearity.

The asynchronous/self-oscillating sigma-delta modulating technique has been used in

audio power amplifiers[57] where it achieves 90% power efficiency, and in an ADSL line driver[58] where it has achieved 47% power efficiency although line termination is not included in this efficiency figure. It has also been proposed for use in wireless UMTS systems[59] and as a modulator for 8MHz VDSL systems, using a 140MHz limit cycle frequency[60]. However, difficulty in analysing the modulators, a lack of a mature design procedure, and circuit challenges mean that the use of self-oscillating modulators for communication-bandwidth applications is a relatively untested area, compared to other linear and switching approaches mentioned earlier.

2.8.1.3 Combined

Combined line drivers usually involve decomposing a high-efficiency, high-linearity problem into a high-efficiency problem to be solved by a non-linear switching amplifier, with a low-efficiency linear amplifier linearising the output of the non-linear amplifier. These systems are sometimes referred to as class K although a class H modulation scheme can be considered a combined approach if a switching amplifier is used to generate a modulated supply rail for a linear class AB output stage in feedback. Alternately, a switching stage can be used to generate a rough waveform and a linear amplifier in feedback is used to correct the difference between the input signal and the switching amplifier's output[61][62]. The difference between these two methodologies is that the former is a series approach to combining while the latter is a parallel approach to combining. The techniques used in combined systems have been covered separately in the preceding sections so will not be discussed further.

An audio amplifier implementing a class K architecture has been presented in [63] and achieves 90% efficiency.

2.8.1.4 Other

Various other techniques exist which attempt to solve the same problems of high power-efficiency, high crest factor and high linearity that line driver designers attempt to solve. However, these other techniques focus on system-level solutions to problems and not on the design of the line driver itself.

One technique[64] combines multiple small power amplifiers using L-C combining networks or transformers, as this reduces the power lost in impedance transformation networks. It also allows power control by switching on or off some number of the small power amplifiers to alter the overall output power. It also suggests the possibility of operating multiple high-efficiency, low-bandwidth amplifiers in parallel for a high-

efficiency, high-bandwidth output signal.

2.8.1.5 Summary

Conventional linear line drivers are fundamentally limited in the maximum possible efficiency that they can achieve. The result of low efficiency, especially with high crest-factor signals, is excessive power dissipation in the line driver output stage, which can cause the thermal and current density problems for the entire communication system.

Non-linear switching line drivers and power amplifiers show higher efficiencies, so much less excessive power dissipation, but they involve bandwidth or linearity compromises.

Low bandwidth, class D line drivers with sigma-delta modulation are commonly used in audio, but at higher bandwidths, commercial line drivers use linear class AB or G output stages. However, various groups are researching the feasibility of self-oscillating sigma-delta modulation, as the low oversampling ratio required for this modulation scheme makes it attractive for high-bandwidth signal use. One author[36] has extensively investigated self-oscillating line drivers and has developed an 8MHz DMT line driver for ADSL which achieves 47% efficiency.

2.8.2 Reported performance

HomePlug AV is a relatively new standard and as such, the number of published line driver architectures is very small. However, there are other established areas which share similar performance or functional aspects with HomePlug AV line drivers. Digital Subscriber Line (DSL) technologies are most similar, also being wide band OFDM communication systems. Audio power amplifiers share a lot of architectural similarities with some classes of line drivers, and the same is true for Power controllers (regulators etc.), although with much lower frequency and higher power requirements than HPAV.

A selection of papers will now be reviewed to understand the structures, efficiencies and directions that power amplifier research is taking. The review will consider the different classes from the point of view of their applicability to PLC line drivers.

2.8.2.1 DSL

DSL is a widely used telecommunications technology for providing the last-mile data connection between a telephone company's exchange and a customer's premises. It shares many similarities with the HomePlug AV standard: use of OFDM modulation and the resulting high CF problems this creates for the line driver, as well as moderate communication bandwidths around 1-2MHz. DSL systems are usually multi-chip solutions, due to the difficulty of implementing the line driver in the digital CMOS process and as a result, often use high-voltage Bipolar[46], BiCMOS/DMOS[41, 45, 65] or high-voltage CMOS[66, 67] processes. Class-AB based designs in particular benefit from higher voltage supplies as their output devices require some minimum voltage drop typically of the order of 0.4V in order keep the output devices operating in their saturation region. If the output devices are powered from a low voltage such as 3.3V, this voltage drop – doubled, because a voltage drop is required for both the pull-up and also the pull-down output devices – is a significant proportion of the supply voltage. The maximum swing is now $3.3\text{V} - 0.8\text{V}$, and so the maximum injected power is reduced by $((3.3 - 0.8)/3.3)^2$ versus what could be achieved if no voltage drop were required. Class-D[68, 58, 62] designs do not operate in saturation and so for the same 3.3V supply voltage, can achieve a higher injected power.

Table 2.2 summarises the performance and architecture of a number of published DSL line drivers. Research interest has been driven by improving efficiency and this has been achieved by experimenting with alternate driver architectures. The original Class-AB stage reports efficiencies around 5%[41, 69], which was increased with the introduction of Class-G/H techniques to around 16%[40, 45, 46]. Recent Class-D structures have reported even higher efficiencies from 19% to 53%[68, 66, 58]. While the Class-D structures report good efficiency, the trade-off is reduced linearity, typically around 52dB[66] MTPR compared to around 70dB[40] MTPR for Class-AB/G/H based designs.

A number of other works have investigated combinations of line driver output stages such as an AB stage in parallel with a Class-D stage[62], high voltage[70] and multi-level[67] Class-D, and active termination[71, 40] which aims to minimise the losses associated with line termination resistors in series with the line driver outputs.

Considering the above, the structure that has had most success at achieving high efficiency in low-voltage processes is the Class-D and this suggests it is worthy of further investigation for use in wide-band, integrated HomePlug AV line drivers. One caveat is that the bandwidth of the reported DSL structures is a factor of ten lower than that required by HomePlug AV.

Reference	Author	Year	Technology	Supply	Efficiency	Bandwidth	Injected Power	Linearity	Architecture
[69]	Sands	1999	0.35μm CMOS	+3.3V, +5V	3.15%	1.1MHz	12.6mW	52dB SFDR	Class-AB with off-chip bipolar output devices
[41]	Weinberger	2002	0.6μm BiCMOS	+12V	6.3%	1.1MHz	20mW	75dB SFDR	Class-AB line driver fully integrated in AFE
[62]	Shorb	2002	0.35μm CMOS	+3.3V	8.5%	1.1MHz	110mW	unknown	Class-AB in parallel with multi-level Class-D
[71]	Sabouri	2002	26V Bipolar	±12V	14.8%	1.1MHz	110mW	75dB MTPR	Class-AB with active termination
[46]	Pierdomenico	2002	Bipolar	±4V, ±8V	16%	1.1MHz	110mW	69dB MTPR	Switched Class-G
[58]	Piessens	2002	0.35μm CMOS	+3.3V	53%	1.1MHz	100mW	56dB MTPR	Self-oscillating Class-D
[58]	Piessens	2002	0.35μm CMOS	+3.3V	20%	8.5MHz	5.5mW	>40dB MTPR	Self-oscillating Class-D
[45]	Maclean	2003	0.7μm BiCMOS	+5V, +16V	16%	1.1MHz	100mW	69dB MTPR	Switched Class-G
[40]	Bicakci	2003	0.25μm CMOS with 2.5/5V devices	+6V	16%	1.1MHz	110mW	72dB MTPR	Supply pumping Class-G, active termination and digital calibration.
[65]	Vecchi	2003	0.8μm BCD	±5V, ±12V	14.2%	1.1MHz	100mW	41dB MTPR	Parallel low and high voltage AB amplifiers
[72]	Mehrmanesh	2004	0.25μm CMOS	+2.5V	12.7%	1.1MHz	7mW*	77dB THD	Class-AB with gain-boosted output devices
[70]	De Gezelle	2005	0.7μm 100V CMOS	+50V	13.1%	1.1MHz	100mW	40dB MTPR	High-voltage Class-D
[68]	Serneels	2007	0.13μm CMOS	+1.2V, +5.5V	42%	2.2MHz	100mW	58dB MTPR	Stacked self-oscillating Class-D
[67]	Doutreloigne	2009	0.35μm CMOS with 50V devices	+3.3V, ±25V	unknown	unknown	unknown	unknown	Multi-level Class-D
[66]	Gierkink	2009	0.35μm CMOS with 10V devices	+3.3V, +10V	19%	2.2MHz	100mW	52dB MTPR	PWM Class-D with three levels
[73]	Cesura	2009	0.15μm CMOS with 3.3V and 5V devices	+3.3, +7V	3.9%	30MHz	28mW	69 MTPR	Class-AB with cascoded output stage

2.8.2.2 Audio

Audio power amplifier share a number of similarities with OFDM line drivers. Audio signals have a high CF of typically 10dB or greater[74] and applications such as portable, battery powered music players require long battery life and so high efficiency. As the audio power amplifier consumes a significant percentage of total system power – similar to HomePlug AV line drivers in HPAV systems – there is significant demand to achieve high audio power amplifier efficiency. Additionally, like HPAV systems, some portable audio applications require implementation in low-voltage digital CMOS and so it is useful to briefly investigate the subject area given some of the similarities to HPAV. One important difference between Audio and Communications applications is that audio typically has a very narrow bandwidth of around 20kHz and so has substantially different design trade-offs than HPAV systems do.

The narrow bandwidth provides plenty of scope for oversampling to very high levels, while still only requiring a switching frequency in the hundreds of kilo-hertz to the low tens of mega-hertz. The moderate switching frequency means that high order, multiple-integrator loops can be made. High order loops contain multiple poles and zeros which define the loop transfer function, but the circuit components used to implement the loop, such as operational amplifiers, transconductance stages and output drivers may introduce additional poles and zeros. If these circuit-level poles/zeros are near in frequency to the poles/zeros which define the loop transfer function, they will alter the loop transfer function and can degrade the performance of the high order loop, or cause instability. To prevent this, the circuit-level poles/zeros must be pushed far beyond the switching frequency, which costs current. Additionally, transmitter systems often include the large, high power output driver within the feedback loop. The phase shift introduced by the delay of the output driver is proportionally much less significant when the switching frequency is low, than when the switching frequency is high, and so low-frequency audio drivers are simpler to stabilize. Finally, the output power in audio applications is usually greater than 1W and the switching frequency is on the order of hundreds of kilohertz and so the current required to push a circuit pole is less than in wide bandwidth applications due to the lower switching frequency, and is also a low proportion of the load current as the load power is higher than what is typically found in communication applications.

For these reasons, audio amplifier research has been the pioneer of Class-D and many of the techniques in Class-D DMT line drivers have evolved from Audio approaches. One early work[50] involved two self-oscillating Class-D amplifiers used to create a positive and a negative supply which tracks an audio signal. The two supplies are used to power a Class-A or Class-B output stage which linearises the output of the Class-D stages. This would now be called a Class-H approach.

Much of the audio research can be split along two lines; stationary/vehicular applications and portable applications. Stationary/vehicular amplifiers are characterised by high output powers greater than 5W and to achieve this, high voltage output stages using bipolar or DMOS devices in a Bipolar+CMOS+DMOS (BCD-MOS) process are often used[75, 76, 77]. These structures use CMOS-implemented PWM modulators or low-order sigma-delta modulators to achieve linearities below 0.05% THD and achieve efficiencies of around 90% at maximum DC output power. In contrast, portable applications usually require operation from lithium-ion batteries with supply voltages around 3.6V. To minimise cost, integration of the audio power amplifier with the digital audio decoding logic is required, and to reduce final implementation costs, it is desirable to use three-level PWM modulation to reduce switching energy, such that the circuit can operate without an off-chip LC filter. The resulting[78, 79] efficiencies are approximately 80% at maximum output power and PWM structures predominate.

While Class-D structures are popular and in widespread use, Class-AB structures can still provide competitive efficiencies[74] as audio crest factors can reach up-to 20, so the RMS power of the signal is very low. At low powers, and so low output voltage swings, the switching losses of Class-D can exceed the quiescent current of Class-AB, such that the Class-AB becomes more efficient than Class-D.

Approaches such as Class-K (Class-AB in parallel with Class-D) have also been attempted for audio[63, 80] although they have not achieved significant performance improvements compared to AB-only or D-only structures and so their extra complexity has prevented their widespread use.

Summaries of the performance of a selection of audio power amplifiers are given in Table 2.3.

Reference	Author	Year	Class	Technology	Efficiency	Supply	Bandwidth	Output Power	Linearity	Architecture
[50]	Kashiwagi	1985	H	Discrete devices	57%	unknown	20kHz	100W	0.005% THD	Self-oscillating Class-D generates signal-dependent supply for Class A/B
[75]	Ballan	1995	D	2μm CMOS	80%	+5V, +12V	15kHz	5.7W	56dB SNR	Second order sigma-delta with H.V. output
[63]	Jung	1998	K	unknown	90%	+22V	20kHz	50W	0.005% THD	Parallel Class-D and Class-AB
[78]	Forejt	2005	D	90nm CMOS	75%	2.7V–5.4V	20kHz	700mW	0.03% THD	First-order PWM with 3-level output
[76]	Berkhout	2003	D	BCD-MOS	90%	+12V, +60V	20kHz	100W	1% THD	Second-order PWM with H.V. output
[81]	Morrow	2004	D	0.6μm BCDMOS	89%	+5V, +20V	20kHz	20W	0.01% THD	Third-order PWM with H.V. output
[79]	Muggler	2004	D	1.2μm BiCMOS	86%	2.5V–6.5V	20kHz	2.5W	0.04% THD	First-order PWM with 4-state output
[80]	van der Zee	1999	K	BCD-MOS	85%*	+18V	22kHz	30W	0.02% THD	Parallel Class-D and Class-AB
[77]	Gaalaas	2005	D	0.6μm BCD-MOS	88%**	+5V, +5V–+20V	20kHz	40W	0.001% THD	7^{th} order sigma-delta with H.V. output stage
[74]	Becker	2005	AB	90nm CMOS	70%	+2.75V-5.5V	20kHz	1W	0.001% THD	Class-AB with thick-oxide transistors

Table 2.3: Performance of Audio Power Amplifiers. Efficiency is measured at the maximum DC output power except where specified. *Efficiency measured with a 1kHz sine wave input. **Efficiency measured at 5W output power. H.V. == High Voltage.

2.9 Conclusion

PLC is an emerging in-home networking technology that uses complex digital modulation with hundreds or thousands of carriers to make maximum use of the time and frequency SNR available in the mains wiring system. The market environment, modulation scheme and the communication line itself combine to place significant demands on the line driver: low-voltage CMOS implementation, wide bandwidth and high power.

Much of the relevant literature focuses on DSL based systems which have lower bandwidths but comparable injected power to PLC. The most popular commercial line driver classes are Class-AB/G, as these can achieve the linearity required by DSL systems while improving efficiency over Class-AB approaches. However, the power dissipation in state-of-art AB/G structures is still high and so the line driver dominates system power consumption.

The success of the Class-D architecture at achieving high efficiency has motivated research into Class-D based line drivers and there has been some success reported. However, these Class-D DSL line drivers have a bandwidth that is typically a factor of 10 lower than that required for PLC.

In the subsequent chapters, this work will investigate the feasibility of wider bandwidth Class-D structures and will develop new circuits required to achieve low-voltage CMOS implementation of an efficient, wide bandwidth and high-power PLC line driver.

Chapter 3

Modelling

3.1 Introduction

To develop the idea of using a Class-D structure as a line driver for wide band communication systems, an initial exploration of the design space must be performed to understand what performance Class-D can achieve over a wide bandwidth. While it is possible to do this using transistor level simulations of various architectures, this would require significant design and simulation time and so would reduce the design area that could be explored given a finite amount of time. This suggests that a fast, simplified model of the Class-D structure is required in order to allow rapid design space exploration. Frequency domain models, or simplified behavioural models are often used in similar works [82][53], but these models are primarily linearity models aimed at exploring the linearity performance of a design and they do not consider the power flows in the structure beyond high-level model parameters such as injected power and supply voltage. Important metrics such as power efficiency and power consumption are left for transistor-level simulations, making the efficiency performance a matter of pot luck, to some extent.

In this work, a power dissipation model of the Class-D amplifier has been developed which considers the losses incurred in practical Class-D systems which have parasitic resistances and capacitance, but does not consider other performance aspects such as linearity or time domain behaviour. While linearity is an important parameter in Class-D systems, it is better dealt with using traditional Class-D linearity modelling techniques. Additionally, the linearity requirements of communication systems, and HomePlug AV in particular, is modest; on the order of 40dB MTPR. Although the wide bandwidth does pose additional challenges, it is expected that with appropriate choices of modulator architecture and switching frequency, sufficient linearity for wide band

communication applications can be achieved.

Hence, this chapter is concerned with understanding the high level problems and opportunities involved in Class-D communication line drivers. It is less concerned with the physical realisability of some of the design choices that will be examined; the work will drive the development of the new structures required to achieve new levels of performance.

3.2 Model development

There are three parts of the power dissipation model:

1. Compute the basic parameters of the system.
2. Calculate the losses due to the on-resistance of the Class-D output stage.
3. Calculate the switching losses due to parasitic gate and drain capacitance of the Class-D output stage.

The other major loss mechanism in Class-D output stages is shoot-through current which occurs if the pull-up and pull-down output devices are both turned on during an output transition, resulting in a large spike of current flowing from positive to negative supplies. However, shoot-through can be avoided using a non-overlap circuit which prevents both output devices being on simultaneously using either a fixed delay as in [83], or using a calibration routine which senses the shoot-through current and alters the non-overlap time to minimise shoot-through current as in [84]. It is assumed that a practical Class-D design will use appropriate shoot-through control and so shoot-through loss is not significant and will not be modelled.

The three parts of the power dissipation model will now be covered in order.

3.2.1 Parameter calculation

The power dissipation model for on resistance losses is shown in Figure 3.1. This is derived from the Class-D output stage structure shown previously in Figure 2.27 and represents a Class-D H-bridge driver in either high or low states. The output stage transistors which are conducting current are shown as resistors R_{ON} and the output stage transistors which are not conducting are not required by the model; it is assumed that either one or the other of the H-bridge switch pairs will be conducting, but not both at the same time. The model also includes a transformer with N_p and N_s primary

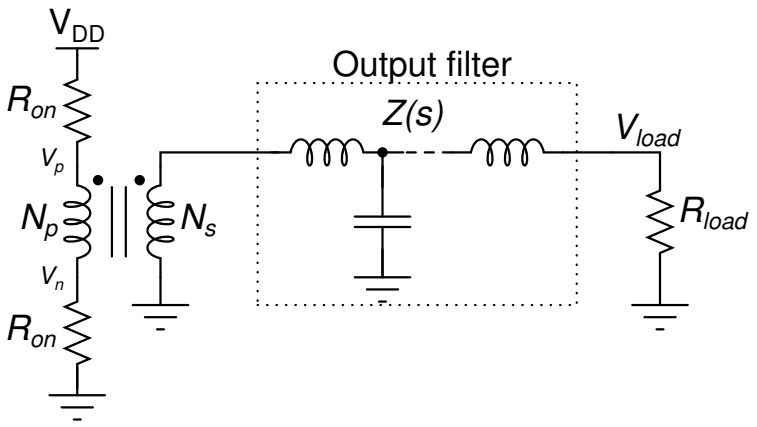

Figure 3.1: Model used to compute power dissipation in a Class-D output stage.

and second turns, respectively; a complex loop filter $Z(s)$; and a load resistor $\mathrm{R_{load}}$. The transformer is required in a practical powerline line driver to provide isolation between the high voltages on the powerline and the relatively low voltages from the line driver, but the ability to choose the turns ratio provides an additional degree of freedom in the design of the line driver. For example, using a N_p:N_s ratio of 1:n rather than 1:1 will increase the voltage swing of $\mathrm{V_{load}}$ by a factor of n, at the cost of reducing the effective load resistance seen by the line driver by a factor of n^2. In low voltage CMOS line drivers, this step-up ratio n is a critical design parameter which is required to meet the required injected power.

The filter $Z(s)$ is required to prevent high frequency switching components from reaching the load resistance, $\mathrm{R_{load}}$. In order to maximise efficiency and power transfer, the filter is singly terminated; the load impedance is finite and determined by the impedance of the powerline, and the source impedance is minimised and from the perspective of the filter, can be considered as almost zero Ohms.

From this model, the amount of power dissipated in $\mathrm{R_{ON}}$ can be calculated. It is not a simple equation because in a Class-D, power can flow back and forth across $\mathrm{R_{ON}}$ on each switching cycle, and power dissipated depends on the characteristics of $Z(s)$ and on the frequency components present in the system.

The model is parameterised by the desired power P_l that is injected into the powerline, as this is usually the system specification that a power amplifier designer is concerned with, and the $\mathrm{R_{ON}}$ of the Class-D stage output devices. Before computing losses in the system, the maximum value of $\mathrm{R_{load}}$ that can support the desired value of P_l must be calculated.

In Figure 3.1, the load power can be written as in Equation 3.1 and the RMS load

voltage $V_{load_{RMS}}$ can be written in terms of V_{max}, which represents the peak value of the load voltage, as in Equation 3.2. In turn, V_{max} can be expressed in terms of $\mathrm{V_{DD}}$ and transformer parameters N_p and N_s, as in Equation 3.3.

$$P_l = \frac{V_{load_{RMS}}^2}{\mathrm{R_{load}}} \tag{3.1}$$

$$V_{load_{RMS}} = \frac{V_{max}}{\mathrm{CF}} \tag{3.2}$$

$$V_{max} = \mathrm{V_{DD}} \frac{N_s}{N_p} \frac{\mathrm{R_{load}}}{\mathrm{R_{load}} + 2\mathrm{R_{ON}}} \tag{3.3}$$

Equation 3.3 can be substituted into Equation 3.2, and the result inserted into Equation 3.1. With some manipulation, a quadratic in terms of $\mathrm{R_{load}}$, Equation 3.4, is obtained.

$$\left(P_l\,\mathrm{CF}^2\right)\mathrm{R_{load}}^2 + \left(P_l\,\mathrm{CF}^2\,4\,\mathrm{R_{ON}} - \mathrm{V_{DD}}^2\left(\frac{N_s}{N_p}\right)\right)\mathrm{R_{load}} + \left(P_l\,\mathrm{CF}^2\,4\,\mathrm{R_{ON}}\right) = 0 \tag{3.4}$$

This quadratic can be solved to find two values of $\mathrm{R_{load}}$ which will result in the desired power being injected by the Class-D with output resistance $\mathrm{R_{ON}}$. If values of $\mathrm{R_{load}}$ are complex or negative, then it is not possible to design a line driver for the specified P_l with the specified $\mathrm{R_{ON}}$. If there are two real solutions then the larger of the two is taken, as this will minimise the power consumption of the driver.

Equation 3.3 can be evaluated with the calculated $\mathrm{R_{load}}$ and now the on-resistance losses can be found.

3.2.2 On-resistance losses

A frequency domain representation of the power model is shown in Figure 3.2. The transformer has been removed and $\mathrm{R_{ON}}$ has been transformed into an equivalent on-resistance as seen from the secondary side of the transformer, R_{on_sec}, as given by Equation 3.5.

$$R_{on\_sec} = \mathrm{R_{ON}}\left(\frac{N_p}{N_s}\right)^2 \tag{3.5}$$

The Class-D driver is now represented by a voltage source matrix $\mathbf{V_{in}}$, which contains the the magnitude and frequency information of the Class-D output signal. There are two contributors to $\mathbf{V_{in}}$, the signal to be driven into the load $\mathbf{V_{sig}}$ and the Class-D switching components $\mathbf{V_{sw}}$.

A DMT signal like the one shown previously in Figure 2.13 consists of n individual carriers with amplitudes a_i and frequencies f_i. It is represented in the power model as

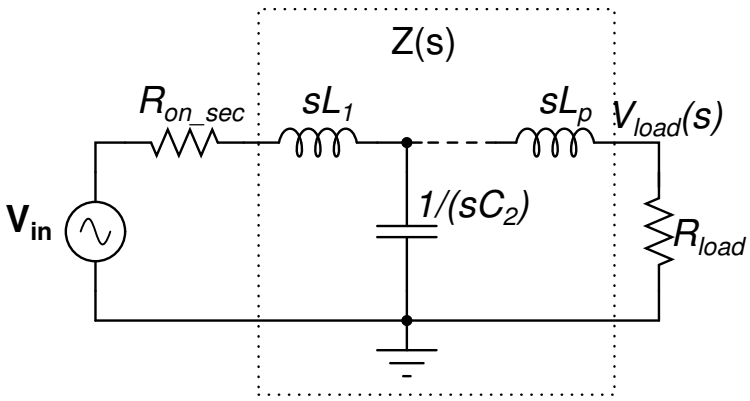

Figure 3.2: Frequency domain model of the Class-D output stage and load.

a row of frequencies and a row of amplitudes, as in Equation 3.6.

$$\mathbf{V_{sig}} = \begin{bmatrix} f_1 & f_2 & \cdots & f_n \\ a_1 & a_2 & \cdots & a_n \end{bmatrix} \tag{3.6}$$

A similar approach is used to define $\mathbf{V_{sw}}$. It is assumed that in the frequency domain the Class-D switching components are approximately represented by the switching components of an un-modulated square wave at frequency f_{sw}. They occur at odd harmonics of f_{sw} and have an RMS amplitude b_j given by Equation 3.7, where j is the j^{th} harmonic and in principle continues to infinity. However, for the purposes of modelling, the maximum value of j was chosen to be 1001, which is computationally practical whilst being a sufficiently close approximation to infinity that there is only a negligible difference in the results when further increasing j.

$$b_j = \frac{\sqrt{2}\,\mathrm{V_{DD}}}{\pi\, j} \tag{3.7}$$

The switching components of the Class-D switching frequency are thus represented in the power model as in Equation 3.8.

$$\mathbf{V_{sw}} = \begin{bmatrix} f_{sw} & 3f_{sw} & \cdots & 1001f_{sw} \\ b_1 & b_3 & \cdots & b_{1001} \end{bmatrix} \tag{3.8}$$

The frequency domain representation of the Class-D output signal is thus given by combining the above matrices, as in Equation 3.9.

$$\mathbf{V_{in}} = \begin{bmatrix} f_1 & f_2 & \cdots & f_n & f_{sw} & 3f_{sw} & \cdots & 1001f_{sw} \\ a_1 & a_2 & \cdots & a_n & b_1 & b_3 & \cdots & b_{1001} \end{bmatrix} \tag{3.9}$$

Regarding the use of this square wave approximation for the Class-D switching compo-

nents; other spectrum characteristics have been tested using the same basic approach as is described here, including a real Class-D spectrum as described by Equation 5.18, but these more accurate spectrum characteristics did not provide a significant improvement to the accuracy of the model.

An s-domain frequency vector is now created from the top row of $\mathbf{V_{in}}$.

$$\mathbf{s} = j\,2\,\pi \begin{bmatrix} f_1 & f_2 & \cdots & f_n & f_{sw} & 3f_{sw} & \cdots & 1001f_{sw} \end{bmatrix} \tag{3.10}$$

The output filter can now be modelled. The filter is modelled single-ended so the equivalent single ended load resistance must be used.

$$R_{load\_se} = \frac{\mathrm{R_{load}}}{2} \tag{3.11}$$

As discussed above, $Z(s)$ is singly terminated and so given a load resistance R_{load_se} and assuming R_{on_sec} is close to zero Ohms so can be approximated for the filter design as a zero Ohm source resistance, normalized component values $L_{1,n}$, $C_{2,n}$, $\cdots$, $L_{p,n}$, $\cdots$ for the output filter can be obtained from references such as [85] and from filter design software, or component values can be derived through hand analysis for simple filters. Once normalized component values are available, the impedance looking in to the filter from R_{on_sec} can be calculated. First, the normalized component values are scaled for the desired load impedance and cut-off frequency F_c using Equations 3.12 and 3.13.

$$C_x = \frac{C_{x,n}\,F_c}{R_{load\_se}} \tag{3.12}$$

$$L_x = L_{x,n}\,F_c\,R_{load\_se} \tag{3.13}$$

Now, the impedance seen from R_{on_sec}, looking towards the load, can be calculated for each frequency $\mathbf{s}$. For the example filter shown in Figure 3.2, it is given by Equation 3.14.

$$\mathbf{Z_{in}} = \mathbf{s}L_1 + \left(\frac{1}{\mathbf{s}C_2} \parallel (\cdots \parallel (\mathbf{s}L_p + R_{load\_se})) \right) \tag{3.14}$$

Finally, the current flowing from $\mathbf{V_{in}}$ at each frequency can be calculated by performing the following division element-wise.

$$\mathbf{I_{in}} = \frac{\mathbf{V_{in}}}{\mathbf{Z_{in}} + R_{on\_sec}} \tag{3.15}$$

The power dissipated in R_{on_sec} is then given by Equation 3.16, where $I_{in,k}$ represents the k^{th} element of the current flow vector $\mathbf{I_{in}}$. The factor of 2 is because in an H-bridge the output current always flows through two devices, the pull-up device and the pull-down

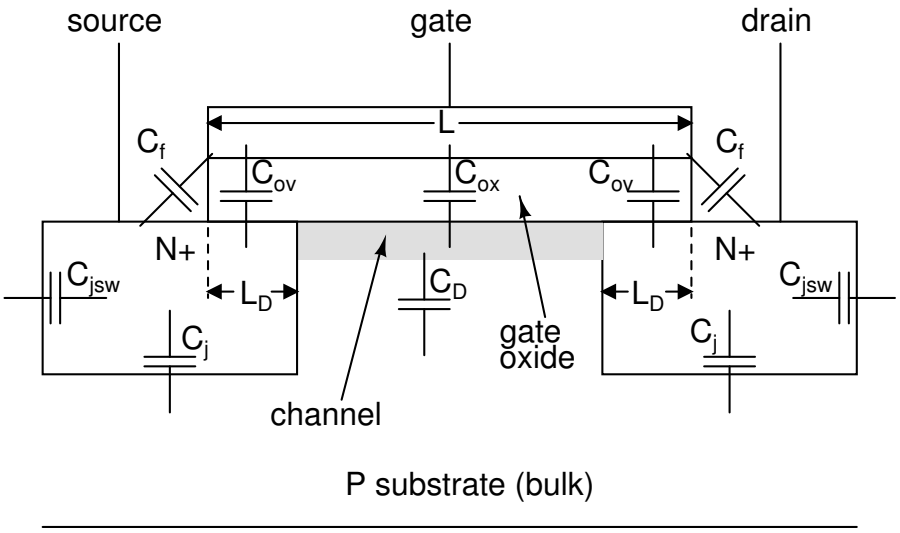

Figure 3.3: Cross-section of an NMOS transistor showing relevant physical capacitances when it is turned on.

device. The absolute operator is needed because current flow can be complex but real-valued resistors only act on the absolute value of the current.

$$P_{\mathrm{R_{ON}}} = 2 \sum_{k=1} |I_{in,k}^2 \, R_{on\_sec}| \tag{3.16}$$

3.2.3 Switching losses

The other loss mechanism in Class-D, which is not included in the model above, is parasitic capacitance charging loss. Before discussing and quantifying this loss mechanism, the MOSFET device capacitances will be reviewed more generally.

3.2.3.1 MOSFET device capacitances

The following discussion is condensed from a number of other sources[86, 87, 88]; these should be consulted for further detail.

Figure 3.3 shows a cross-section of an NMOS transistor, including its physical capacitances. $\mathrm{C_{ox}}$ is the capacitance per unit area between the gate and the channel as given by Equation 3.17.

$$\mathrm{C_{ox}} = \frac{\varepsilon_{\mathrm{ox}}}{\mathrm{t_{ox}}} \tag{3.17}$$

Here, $\varepsilon_{\mathrm{ox}}$ is the permittivity of the oxide and $\mathrm{t_{ox}}$ is the oxide thickness. Capacitances $\mathrm{C_{ov}}$ are the gate-source and gate-drain overlap capacitances and $\mathrm{C_f}$ models the gate-source

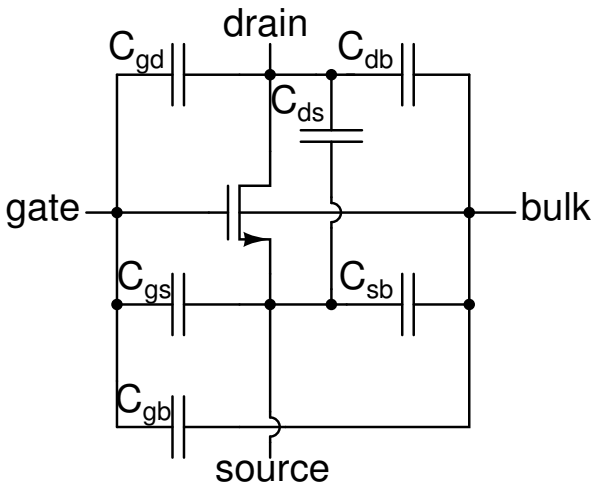

Figure 3.4: NMOS transistor with all possible inter-terminal capacitances.

and gate-drain fringing capacitances. C_j is the depletion capacitance per unit area between the bottom of the source/drain regions and the bulk, and C_{jsw} is the sidewall capacitance per unit width and length, between the source/drain regions and the bulk. C_D is the capacitance per unit area between the channel and the bulk.

The physical capacitances of Figure 3.3 can be modelled as a set of capacitors connected across all possible pairs of transistor terminals, as shown in Figure 3.4. For example, C_{gs} is the effective capacitance between the gate and source and may be made up of C_{ox}, C_{ov} and C_f, depending on the operating region. Unless specified otherwise, it is assumed that all capacitors have the same capacitance value regardless of the terminal it is measured from – so C_{gs} will equal C_{sg}.

Off capacitance

When the transistor is off, there is no channel beneath the gate and C_{ox} and C_D appear in series between gate and bulk. C_D typically[5] has a value of $\frac{C_{ox}}{5}$ and so C_{gb} is approximately given by Equation 3.19.

$$C_{gb,off} = \frac{1}{\frac{1}{W\,L\,C_{ox}} + \frac{1}{W\,L\,C_D}} \tag{3.18}$$

$$= \frac{W\,L\,C_{ox}}{6} \tag{3.19}$$

The gate-drain and gate-source capacitances $C_{gd,off}$ and $C_{gs,off}$, Equation 3.20, are made up of overlap capacitance C_{ov} and fringing capacitance C_f. C_{ov} is physically modelled by Equation 3.21, where L_{ov} is the length of overlap between the gate and the drain, but this parameter is hard to measure and so manufacturing foundries will instead measure and make available parameters C_{gdo} and C_{gso}, which represent the capacitance per unit

width due to gate-drain and gate-source overlap, as in Equation 3.22.

$$C_{gd,off} = C_{gs,off} = C_{ov} + C_f \tag{3.20}$$

$$C_{ov} = W\, L_{ov}\, C_{ox} \tag{3.21}$$

$$= W\, C_{gdo/gso} \tag{3.22}$$

C_f is another measured parameter although in some popular models[89], the computed value given in Equation 3.23 can be used.

$$C_f = 2\, W \frac{\varepsilon_{ox}}{\pi} \log\left(1 + \frac{4 \times 10^{-7}}{t_{ox}}\right) \tag{3.23}$$

The capacitances C_{db} and C_{sb} are the p-n junction capacitances between the doped drain/source and the bulk. They depend on the junction bias voltage, as can be seen in Equation 3.24, where ψ_0 is the built-in potential of the p-n junction at zero bias[87].

$$C_{sb/db} = \frac{1}{\sqrt{1 + \frac{|V_{sb/db}|}{\psi_0}}} \left(WLC_j + 2\,(W + L)\, C_{jsw}\right) \tag{3.24}$$

Parameter C_j represents the capacitance per unit area between the bottom of the drain/-source region and the bulk, while C_{jsw} represents the capacitance per unit distance between the sidewalls of the drain/source region and the bulk. Both parameters are usually measured by the process foundry and included in device models and documentation, although there is a simple analytical expression for C_j[87] as shown in Equation 3.25, where N_A and N_D are the doping densities of the p and n type materials, respectively, q is the charge of an electron, and ε_{si} is the permittivity of silicon.

$$C_j = \sqrt{\frac{q\varepsilon_{si} N_A N_D}{2\,(N_A + N_D)}} \tag{3.25}$$

The only capacitor that has not been covered is C_{ds}, but this is usually taken to be zero in all regions of operation as it is much smaller than the other capacitances.

The total gate capacitance $C_{gg,off}$ and drain capacitance $C_{dd,off}$ for a MOSFET which is turned off are thus given by Equations 3.26 and 3.28.

$$C_{gg,off} = C_{gb,off} + C_{gs,off} + C_{gd,off} \tag{3.26}$$

$$= \frac{WLC_{ox}}{6} + W\,(C_{gso} + C_{gdo}) + 2C_f \tag{3.27}$$

$$C_{dd,off} = C_{gd,off} + C_{db} \tag{3.28}$$
$$= WC_{gdo} + C_f + C_{db} \tag{3.29}$$

Linear region capacitance

For linear region operation of the transistor, a channel is present which has roughly constant charge density across the transistor length. The gate-oxide capacitance WLC_{ox} is modelled by including half its value in C_{gs} and the other half in C_{gd}, as in Equation 3.30.

$$C_{gs,lin} = C_{gd,lin} = \frac{WLC_{ox}}{2} + C_{ov} + C_f \tag{3.30}$$

The gate-bulk capacitance C_{gb} is approximately zero in this region as the channel shields the bulk from changes in the gate, and C_{sb}/C_{db} have the same value as in Equation 3.24.

The total gate capacitance $C_{gg,lin}$ is given by Equation 3.32.

$$C_{gg,lin} = C_{gs,lin} + C_{gd,lin} \tag{3.31}$$
$$= WLC_{ox} + W\left(C_{gdo} + C_{gso}\right) + 2C_f \tag{3.32}$$

The capacitance seen at the drain includes terms C_{gd} and C_{db}, but less obviously also includes C_{gs}. This can be explained by recalling that C_{gs} includes half of the gate oxide capacitance and assuming the MOSFET is switched from off to linear, the full gate oxide capacitance must be charged – both the C_{gd} component and the term $\frac{WLC_{ox}}{2}$ from C_{gs}. The total drain capacitance is thus given by Equation 3.34.

$$C_{dd,lin} = C_{gd,lin} + C_{gs,lin} + C_{db} + \frac{WLC_{ox}}{2} \tag{3.33}$$
$$= WLC_{ox} + WC_{gdo} + C_f + C_{db} \tag{3.34}$$

Saturation region capacitance

For operation in the saturation region, the voltage changes on the drain have little effect on the charge in the channel and C_{gd} is given by 3.20. The effect of gate-oxide capacitance is then lumped entirely into the gate-source capacitor. As the channel pinches off in saturation, the channel charge must be integrated across the channel and is found[87] to be $\frac{2WLC_{ox}}{3}$. $C_{gs,sat}$ is then given by Equation 3.35.

$$C_{gs,sat} = \frac{2WLC_{ox}}{3} + C_{ov} + C_f \tag{3.35}$$

When the transistor is in saturation, there is a negative gain between the gate and the drain; a conditions which result in Miller multiplication of capacitances between gate and drain. Denoting the miller gain as A_m, the gate-drain capacitance in saturation becomes:

$$C_{gd,sat} = A_m \left(C_{ov} + C_f\right) \tag{3.36}$$

Note that in this case, this capacitance seen from the drain side does not experience a miller multiplication so in this instance, C_{gd} does not equal C_{dg}. Instead, C_{dg} is given by Equation 3.37.

$$C_{dg,sat} = C_{ov} + C_f \tag{3.37}$$

Other capacitances have the same values as in the off region and the total gate and drain capacitances are given by Equations 3.39 and 3.40.

$$C_{gg,sat} = C_{gs,sat} + C_{gd,sat} \tag{3.38}$$

$$= \frac{2WLC_{ox}}{3} + W\left(C_{gso} + A_m C_{gdo}\right) + 2C_f \tag{3.39}$$

$$C_{dd,sat} = C_{dg,sat} + C_{db} \tag{3.40}$$

$$= WC_{gdo} + C_f + C_{db} \tag{3.41}$$

3.2.3.2 Capacitor charging loss

The switches which will implement the two R_{ON} resistors shown in Figure 3.1 are assumed here to be a PMOS device and an NMOS device. Their gate and drain capacitances will be charged and discharged each switching cycle and so must be included in the power model. In order to understand which specific capacitances should be accounted for when computing parasitic capacitance charging loss, Figure 3.5 describes the behaviour of the output stage for a low-to-high under the assumption that the input signal transition is much faster than, or takes place before, the output signal transition. This assumption is valid for most practical Class-D drivers, and particularly for high frequency Class-D drivers where the filter current usually opposes the output transition – and so the drain transition does not begin until the gate transition is almost complete.

Before the transition, the NMOS device is initially in the linear region and at the end of the transition, will be turned off. Similarly, the PMOS device will be off before the transition but during the transition, will initially turn on in its saturation region, before moving into its linear region when $|V_{ds}|$ falls below $|V_{gs} - V_t|$. From Figure 3.5(a), it can be observed that the PMOS gate transition occurs mainly when the device is in its saturation region, while it operates in its linear region for the majority of the drain transition.

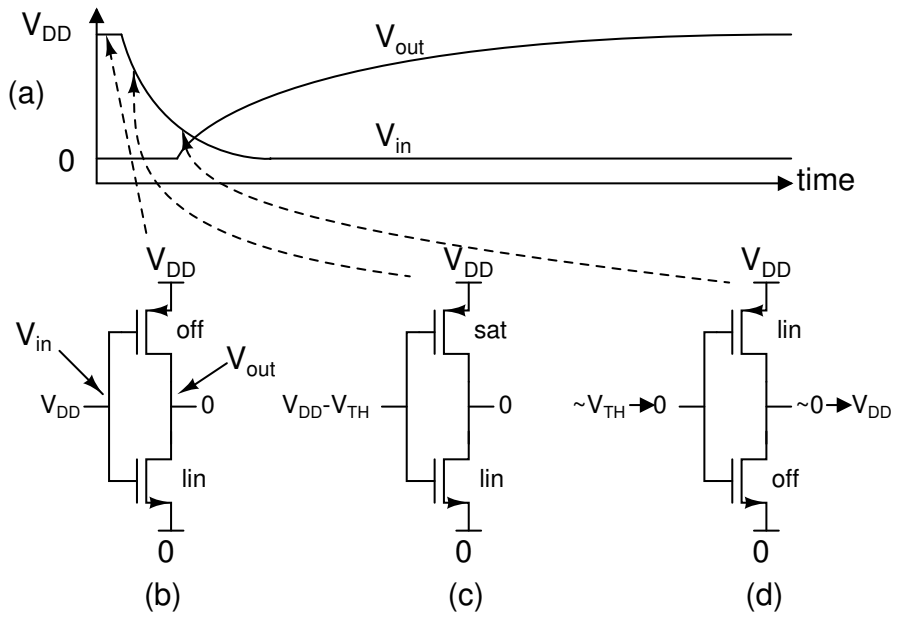

Figure 3.5: P/N totem pole and device operation regions during a transition from high input to low input. (a) assumed input/output waveform timing, (b) initial conditions of the output stage, (c) PMOS begins turning on and operates in saturation initially. The NMOS is also still on so sinks the current injected by the PMOS. (d) PMOS begins to overcome drive strength of NMOS and the V_{out} starts to rise. Soon after, the PMOS moves into the linear region and the NMOS turns off.

Denoting PMOS and NMOS capacitances with a p and n suffix respectively, and by inspection of Figure 3.5, the total charge required to drive the NMOS and PMOS gates for a falling input edge is given by Equation 3.42. By analogy for the rising input edge, the total charge required for a complete switching cycle (one falling and one rising edge) is given by Equation 3.43.

$$Q_{g,falling} = (C_{gg,lin_{NMOS}} V_{DD}) + (C_{gg,off_{PMOS}} V_{th} + C_{gg,sat_{PMOS}} (V_{DD} - V_{th})) \quad (3.42)$$

$$Q_{gg,total} = Q_{gg,falling} + Q_{gg,rising} \quad (3.43)$$

Similarly, the charge required to drive the drain capacitances for rising and falling output edges is given by Equations 3.44 and 3.45.

$$Q_{d,rising} = (C_{dd_n,off} V_{DD}) + \left(C_{dd_p,lin} V_{DD}\right) \quad (3.44)$$

$$Q_{d,falling} = \left(C_{dd_p,off} V_{DD}\right) + (C_{dd_n,lin} V_{DD}) \quad (3.45)$$

3.2.3.3 Capacitive loss simulation

The analytical model of MOS capacitance described above is intentionally simple as it helps develop insight into the capacitive loss mechanisms inside a transistor. However, the model has its limits - the equations are first order approximations, ignoring higher order effects, and more fundamentally, it does not correctly model the transition from one MOSFET operating region to another. For accurate capacitive loss data, simulations of the full BSIM4 transistor model must be used.

A simulation test bench was created with minimum length, unit width output devices. The NMOS output device uses a width of 1μm and length of 0.34μm , while the PMOS output device uses a width of 3μm and length of 0.34μm . The difference in width is due to the NMOS and PMOS device having different drive strengths $\mu_n \mathrm{C_{ox}}$ and $\mu_p \mathrm{C_{ox}}$, respectively, and the ratio $\frac{\mathrm{W_p}}{\mathrm{W_n}}$ was chosen to obtain identical on-resistance from both devices. By simulating a switching cycle (successive positive and negative input transitions) and measuring the charge taken from the supply over this period, a coefficient $\mathrm{C_{g_{unit}}}$ can be calculated as in Equation 3.46, which represents the effective capacitance per unit unit area that must be charged over one period of the input signal. This equation computes the charge transferred into the gates of the PMOS and NMOS devices over a switching cycle, and divides by the total PMOS and NMOS area to get a normalised effective capacitance per unit area, for a certain PMOS:NMOS width ratio $\frac{\mathrm{W_p}}{\mathrm{W_n}}$. The result of evaluating this equation on simulation results from the chosen process is given in Equation 3.47.

$$\mathrm{C_{g_{unit}}} = \frac{1}{\mathrm{W_pL_p + W_nL_n}} \left(\frac{1}{\mathrm{V}} \int_0^{\frac{1}{f_{sw}}} I_{\mathrm{supply}}(t) \mathrm{d}t \right) \tag{3.46}$$

$$\approx 5\,\mathrm{fF}/\mu\mathrm{m}^2 \tag{3.47}$$

Similarly, the effective drain capacitance per 1 μm width of a minimum length device can be calculated from the charge taken from the positive supply over a switching cycle, and is given in Equation 3.48.

$$\mathrm{C_{d_{unit}}} = 4.47\mathrm{fF}/\mu\mathrm{m}^2 \tag{3.48}$$

The total gate and drain charging powers for a Class-D H-bridge are given by Equations 3.49 and 3.50. The factor of 2 accounts for both sides of the H-bridge in a differential

system.

$$\mathrm{P_{gate}} = 2\left(1 + \frac{\mathrm{W_p}}{\mathrm{W_n}}\right)\mathrm{C_{g_{unit}}}\,{\mathrm{V_{DD}}}^2 f_{sw} \tag{3.49}$$

$$\mathrm{P_{drain}} = 2\left(1 + \frac{\mathrm{W_p}}{\mathrm{W_n}}\right)\mathrm{C_{d_{unit}}}\,{\mathrm{V_{DD}}}^2 f_{sw} \tag{3.50}$$

3.2.4 Model summary

Total power dissipation for the Class-D can be calculated by summing Equations 3.16 3.49, 3.50 and as load power P_l is also known, the efficiency can be calculated.

The model is built in a modular fashion and each of the components can be swapped out and replaced with an alternate implementation. For example, a library of filter types have been implemented, parasitic series resistance in the LC filter can be included with a $\mathrm{R_{ESR}}$ parameter and alternate devices and architectures – such as power combining[90] of a segmented output driver – can be explored.

3.3 Model verification

While the gate/drain charging equations above are well known, the process used to estimate power dissipated in the output devices on-resistance is less well known. A model of a system is only useful if it can predict performance of the real system to a known degree of accuracy, so an ideal schematic implementation of a Class-D system with LC filter and resistive load has been created in the Cadence Spectre tool, with the aim of verifying the on-resistance power dissipation model results. The modulator, a

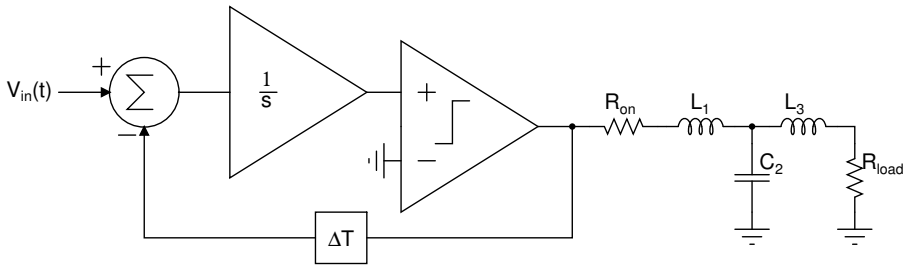

Figure 3.6: Reference schematic against which the on-resistance power dissipation model was compared.

first order Class-D from [36], is shown in Figure 3.6. The integrator and comparator are both ideal, mathematical implementations and the Class-D switching frequency can be set by choosing ideal delay $\Delta T = 1/(4f_{sw})$. The input signal $\mathrm{V_{in}}(t)$ is a 30MHz DMT

signal as described in Figure 2.13.

The power dissipation model is compared to this numerical reference design to establish how accurately the model matches the simulations as the main parameters that affect losses in the output stage – mean switching frequency, output stage on resistance, and input signal amplitude – are varied.

The reference point for model verification is an input signal peak-to-peak amplitude of 3.3V, a mean switching frequency set to 100MHz and an on-resistance set to 1Ω. These three parameters were varied across their expected useful range – based on some knowledge of the required injected power and minimum and maximum oversampling requirements – and the error between the power dissipation in the Cadence Spectre numerical simulations and the Class-D power model were calculated as a percentage error. A 30MHz 3rd order singly terminated Chebyshev Type I LC output filter with 0.1dB ripple was used for all simulations. The filter is implemented with normalized components such that as the computed R_{load} value changes, the filter components are scaled for this new R_{load}. Provided that R_{load} is always much greater than R_{ON}, the filter transfer function does not change as R_{load} or R_{ON} vary – this condition is found to be valid across the useful range of Class-D injected powers.

Figure 3.7 shows the power dissipation error between the Spectre simulations and the Class-D power model, in the resistive load, R_l and in the on-resistance R_{ON}, as the mean switching frequency is varied. The R_{ON} dissipation is accurate to within 2%, but the R_l dissipation shows more variation. LC filter attenuation is significantly lower closer to its cutoff frequency, so the modulator-dependent switching harmonic power is attenuated less and the load power in harmonics neglected by the model become significant, leading to model error of the R_l dissipation of up to 13%. However, this is only an error in the computation of injected power, and the R_{ON} dissipation, which is the main parameter of interest, does not suffer from the same frequency dependent error as it sits before the LC filter.

In Figure 3.8, the effect on model error of varying the input signal peak-to-peak amplitude – and thus signal range and distribution – is examined. The R_{ON} dissipation is generally slightly overestimated but is still within useful limits – from -1% to +4%. The variation in the R_l dissipation error is due to the operation of the self-oscillating modulator, which will oscillate at lower frequencies for larger input signals. As such, larger input signals correspond to lower switching frequencies, and the errors due to the 5-harmonic assumption discussed above become apparent.

Finally, Figure 3.9 examines the effect of altering the on-resistance R_{ON} of the output devices, on model error. While there is little impact on the R_l dissipation error, there is a slight variation of the R_{ON} dissipation error across a range of on resistances, however

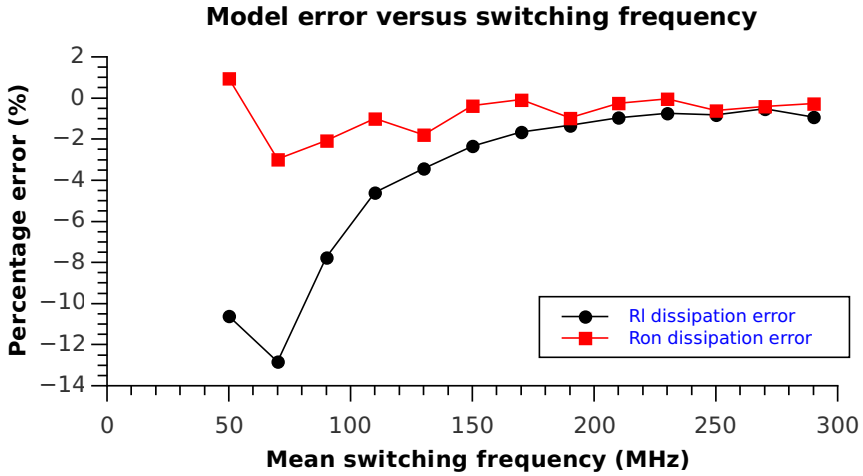

Figure 3.7: Class-D power model error across a range of mean switching frequencies.

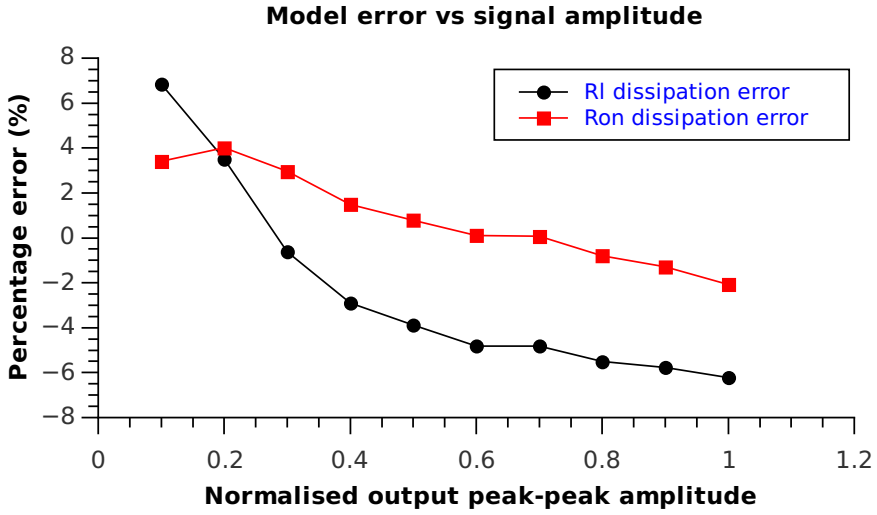

Figure 3.8: Class-D power model error across a range of input signal amplitudes.

the error is still less than $\pm$ 2%.

With the basic Class-D power model operation and accuracy now established, the metrics and usage required to apply the model to communication system power modelling can be considered. This allows freedom from doing slow transistor-level design, implementation and simulations, and allows rapid exploration of the design space.

3.4 Model metrics and usage

To begin exploring the Class-D efficiency design space, a metric is needed. Efficiency on its own does not provide a sufficient basis for comparison as it has no physical relation

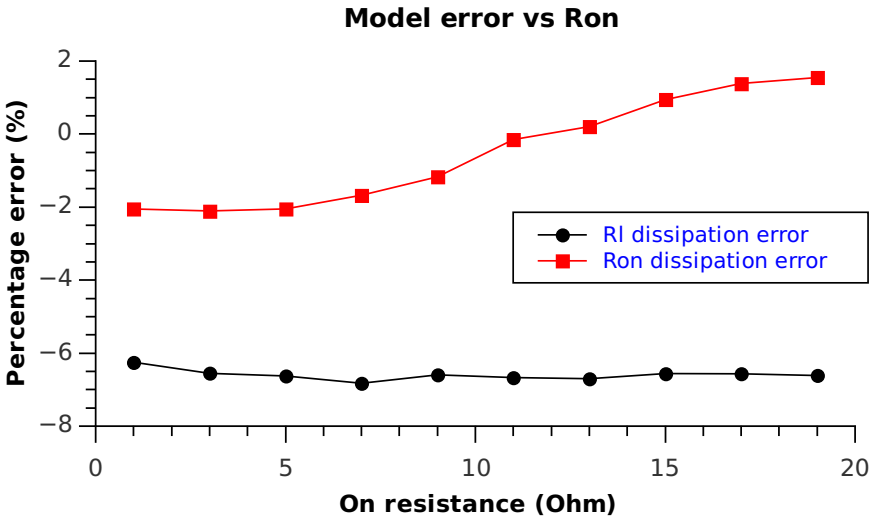

Figure 3.9: Class-D power model error across a range of output stage on-resistances.

to a specific driver – for example, a physically large output driver operating at low frequency may achieve the same efficiency as physically small output drivers operating at high frequency, as one suffers from high R_{ON} losses while the other suffers from high parasitic capacitance losses. However, these drivers are applicable to very different application areas. The most obvious physical quantity to use as a reference point is the width of the NMOS output device, which can be related to the PMOS output device size by multiplying by P/N transconductance ratio $\frac{\mu_p}{\mu_n}$, but this only ties an efficiency to a device size and does not provide much high level insight into the application-level capabilities of a specific design. Instead, a more useful reference parameter is the RMS power injected into a specified load – so the main metric used to compare different Class-D designs will be the efficiency at a given output power.

Determining the efficiency at a given power level is a cumbersome task as all of the system parameters – switching frequency, on-resistance, load resistance, transformer ratios – interact and there is no unique solution. Instead, there are many solutions with a range of efficiencies. It is useful to constrain the problem and then solve it iteratively.

First, a desired injected power is specified, and a range of values to explore is selected, for example, on-resistances between 0.1Ω and 5Ω, in steps of 0.1Ω. The efficiency of each injected power/on-resistance combination can be calculated using the method described in Section 3.2, and the power/on-resistance combination with the highest efficiency is considered to be the optimised design.

3.5 Design exploration

Given an accurate model of power dissipation mechanisms in Class-D output stages, it is now possible to examine the influence of system-level choices on the achievable efficiency of a Class-D output stage. The main variables to consider are:

- Technology – $\mu_n C_{ox}$ and $\mu_p C_{ox}$ values
- Mean switching frequency of the output stage
- Supply voltage
- Filter topology

In addition to these basic system parameters, there are a number of model parameters which must be specified. The model parameters given in Table 3.1 define the default model parameters that will be used in the subsequent design space exploration, are are based on those of a minimum length output device.

3.5.1 Technology

The choice of technology in single-chip communication systems is, as discussed previously, mainly determined by digital processing and cost requirements. One of the significant parameter changes in digital processes is the increase of technology transconductance parameter $\mu_n C_{ox}$. Understanding how this affects the performance of Class-D gives a quick measure of the suitability of digital CMOS processes for implementing wide band communication systems.

Figure 3.10 shows the efficiency-vs-injected power performance for the model with parameters as in Table 3.1, as NMOS transconductance parameter $\mu_n C_{ox}$ is varied. Four $\mu_n C_{ox}$ values are examined, $100\mu A/V^2$, $200\mu A/V^2$, $400\mu A/V^2$ and $800\mu A/V^2$, which are representative of the transconductances per unit area that might be available between the $0.35\mu m$ and 90nm technology nodes.

Three main regions of operation are visible in the graph. At low injected power below -70dBm/Hz, efficiency is dominated by the static power consumption of the modulator and losses in the output stage are negligible. In this region, there is little difference with different $\mu_n C_{ox}$ values and given the low injected power, it is questionable whether Class-D is even an appropriate architecture: greater efficiencies could be achieved with a simple Class-A output stage.

In the centre region, between -65dBm/Hz and -56dBm/Hz, the Class-D achieves good

Table 3.1: Default parameters used in Class-D power dissipation model for a typical 0.13μm CMOS process.

Parameter	Value	Description
L	0.34 μm	Minimum NMOS Length
$\mu_n C_{ox}$	200 $\mu A/V^2$	NMOS transconductance
$\frac{\mu_n}{\mu_p}$	0.33	Ratio of PMOS transconductance to NMOS transconductance
V_{TH}	0.5 V	NMOS Threshold voltage
C_{ox}	4.9 fF/μm^2	Gate capacitance per 1μm^2
C_{dp}	2.39 fF	Effective PMOS drain capacitance per μm width assuming minimum length device
C_{dn}	1.67 fF	NMOS drain capacitance per μm width assuming minimum length device
R_{on}	0.7	Output device on resistance
f_{switch}	150 MHz	Class-D switching frequency
	Chebyshev, 0.1dB ripple, singly terminated	LC filter type
	3	LC filter order
f_c	30 MHz	Filter cutoff frequency
Ns	1	Number of secondary transformer windings
Np	1	Number of primary transformer windings
R_{par}	0.5	Parasitic routing & bond wire resistance
	P/N totem pole	Output stage architecture
BW	22.148 MHz	Communication signal bandwidth
CF_{dB}	12.06 dB	Communication signal Crest Factor
P_{ldBmHz}	-53 dBm/Hz	Desired RMS injected power.
V_{DD}	3.3 V	Output stage supply voltage
P_{static}	4 mW	Static power consumption of modulator

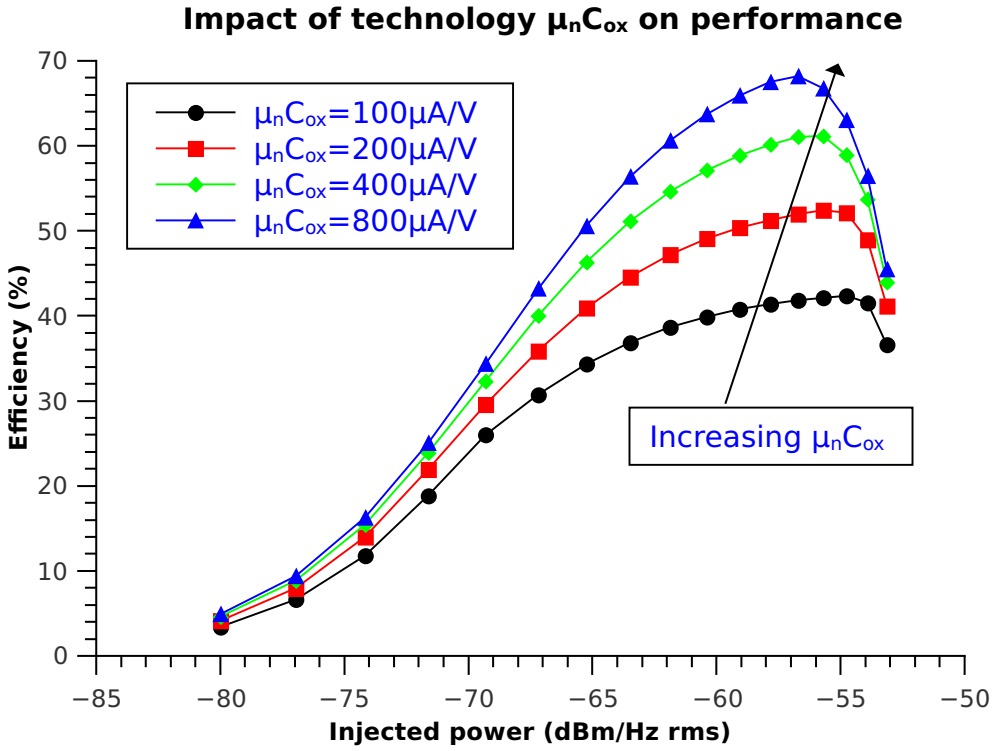

Figure 3.10: Effect of varying technology $\mu_n C_{ox}$ parameter on Class-D performance.

efficiency. The modulator losses become increasingly less significant and overall losses become dominated by on-resistance and gate-charging. Each doubling of $\mu_n C_{ox}$ gives a roughly constant increase in efficiency – or conversely, the efficiency increase follows $\log_2(\mu_n C_{ox})$. The mechanism behind this is that increasing $\mu_n C_{ox}$ allows a smaller device width to be used for a given R_{on}, which reduces gate-charging losses.

A final region of operation exists at high power, above -56dBm/Hz. In this region, the output Class-D resistance – the sum of the transistor on-resistance plus the parasitic routing/bond wire resistance – reaches a minimum, determined by the parasitic routing/bond wire resistance. As such, as injected power increases, it is becomes harder to reach the optimum efficiency point – which would require a lower source resistance – and as a result, the efficiency begins to drop. As the injected power increases, the R_{on} losses begin to dominate system power consumption and the effect of gate capacitance – and so transconductance parameter $\mu_n C_{ox}$ – becomes of decreasing significance, and the efficiencies converge.

To illustrate this behaviour, the main power consumption mechanisms are illustrated in Figure 3.11 for the $\mu_n C_{ox}$ =200μA /V^2 transconductance setting. At -56dBm/Hz, the capacitance-related parasitic power consumption ceases to increase, as increases in device size no longer reduce total on-resistance as the total on-resistance is dominated by

the parasitic routing and bond wire resistance. As a result, the on-resistance losses, and so the total parasitic losses, increase rapidly, growing much quicker than the injected power does, hence the efficiency reduces.

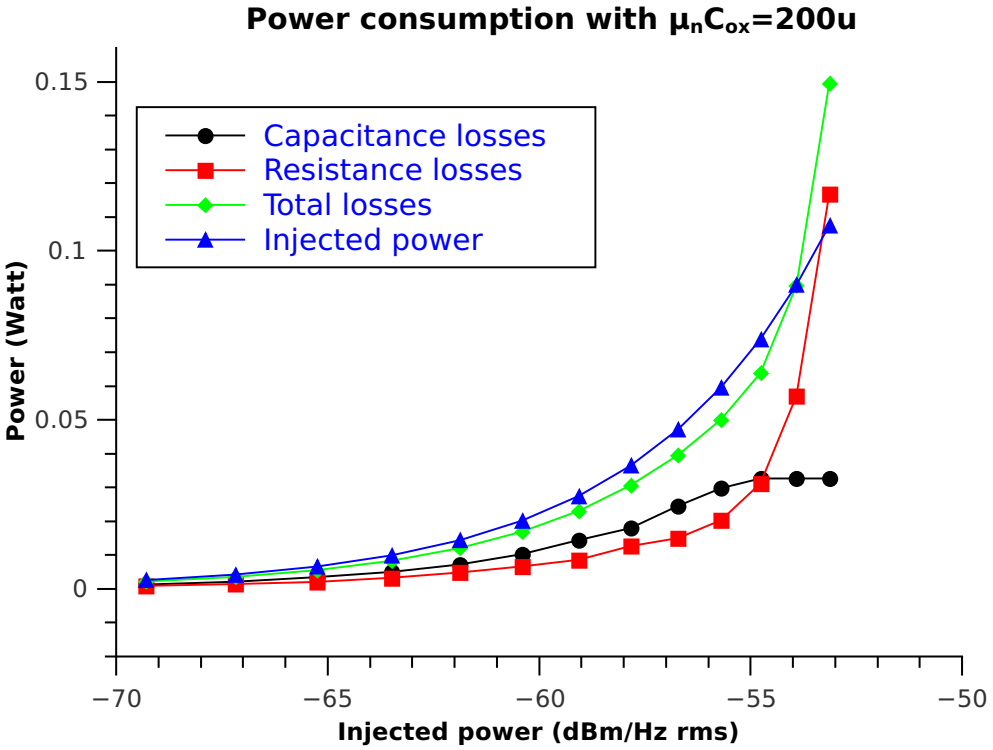

Figure 3.11: Main power consumption mechanisms in the Class-D output stage assuming, using a $\mu_n C_{ox}$ =200μm technology.

At an injected power of -53dBm/Hz, the efficiencies of different technologies have almost converged. This point is the point of maximum injected power for that structure and is determined by the parasitic routing/bond wire losses R_{par}.

In summary, at reasonable injected powers which are not too high and not too low for a particular driver configuration, the impact of increasing technology transconductance parameter $\mu_n C_{ox}$ is significantly beneficial to the efficiency of Class-D output stages operating in the hundreds-of-megahertz region. This is an important validation of the initial concept of using digital CMOS processes to implement wide bandwidth Class-D communication systems. In a practical sense, the implication here is that where possible, the transistors with the highest possible $\mu_n C_{ox}$ values should be used for the output stage.

3.5.2 Voltage

Another important parameter when considering the suitability of low voltage digital CMOS for Class-D is the supply voltage, which usually decreases as the minimum device geometry decreases. It is useful to understand the impact of supply voltage on the Class-D output stage, as it will define the performance that a low voltage output stage can achieve and will suggest directions which should be taken to maximise the usability of low voltage Class-D output stages.

Figure 3.12 shows Class-D efficiency vs injected power performance for the default model configuration, with a range of supply voltages which may be available in a wireline communication system.

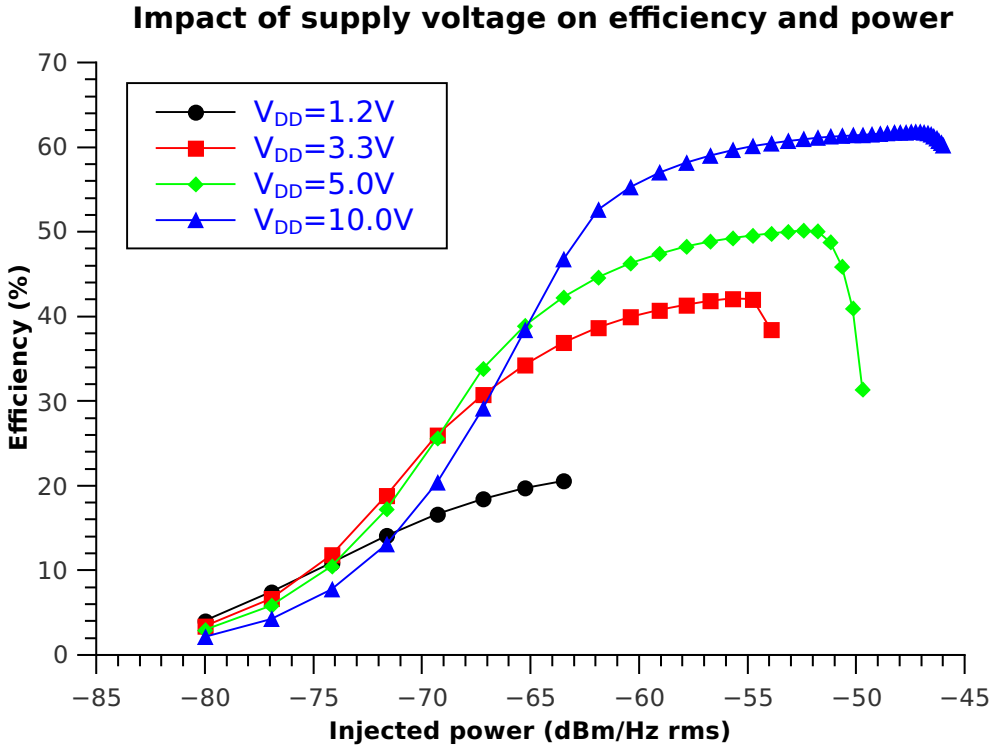

Figure 3.12: Class-D performance across a range of voltages that might be available on-chip or off-chip to a circuit in a digital CMOS process.

The power-efficiency curves for three supply voltages – 1.2V, 3.3V, 5.0V and 10.0V – are shown. The basic three-region shape described in Section 3.5.1 is evident. The effect of increased supply voltage is easily visible. At low power, where efficiency is dominated by the fixed static power consumption of the modulator, efficiencies are similar, with slightly lower losses/higher efficiency for the low supply voltages. However, in the centre region of the graph, higher voltages have a distinct efficiency advantage. Caution should be taken when considering the efficiency figures however, as in a practical

situation, higher voltage structures usually involve physically larger structures which have increased parasitic capacitance and lower $\mu_n C_{ox}$ /$\mu_p C_{ox}$. This would increase parasitic capacitance losses and so would reduce the practically achievable efficiency of the higher supply structures. It is also important to note that the higher voltage supplies will allow a lower transformer ratio for a desired output swing, which reduces parasitic winding resistance and so transformer loss.

Despite these practical concerns, the graph is still useful in determining potential directions for efficiency improvement, separate from the implementation details of a particular device.

The other significant impact of higher supply voltages is the increase in maximum injected power, which can be understood by considering the power limit mechanism discussed previously. As the maximum injected power is given by:

$$P_{max} = \frac{V_{DD}{}^2}{R_{par} + R_{on_{min}} + R_{load}} \tag{3.51}$$

Due to this, an increase of supply voltage will give a squared increase in the maximum injected power. Thus, while the efficiency benefits of increased supply voltage need further consideration before they can be assessed, the increase in injected power is a useful relationship to keep in mind.

3.5.3 Voltage and technology

The previous two sections have considered voltage and technology in isolation, as the two do not necessarily need to have a direct relationship. However, if the design space is constrained to simple two-transistor P/N output stages then there is certainly a relationship between technology transconductance parameters $\mu_n C_{ox}$ and $\mu_p C_{ox}$, and supply voltage, in low-voltage digital CMOS processes.

Using approximations from [91] given in Equation block 3.52 to define C_{ox} and $\mu_n C_{ox}$ values, as well as some assumed V_{TH} values, three example transistors, representative of the voltage and transconductance range available in modern CMOS processes, are defined in Table 3.2.

$$\begin{aligned} \varepsilon_{ox} &= 0.34 \times 10^{-12} \\ t_{ox} &= \frac{L_{min}}{50} \\ C_{ox} &= \frac{\varepsilon_{ox}}{100 * t_{ox}} \\ \mu_n C_{ox} &= 240 * C_{ox} \\ \mu_p C_{ox} &= \tfrac{1}{3}\mu_n C_{ox} \end{aligned} \tag{3.52}$$

L_{min} (μm)	$\mu_n C_{ox}$ (μA /V^2)	C_{ox} (fF/μm^2)	V_{DD} (V)	V_{TH} (V)
0.12	680	28	1.2	0.25
0.34	240	10	3.3	0.45
0.5	163	6.8	5	0.7

Table 3.2: Example parameters for three typical transistors.

As technology moves towards finer scales, $\mu_n C_{ox}$ tends to increase and V_{DD} tends to decrease, increasing or decreasing efficiency when considered individually. For simple output stages where both effects are coupled in opposing directions, the results from the Class-D power model are shown in Figure 3.13. This is modelled with a 1:1 transformer ratio and a load impedance/filter which is scaled appropriately for each supply voltage, but in practice would entail changing the transformer ratio to scale the line impedance as seen by the line, appropriately.

To a first order, the effects roughly cancel each other out and the efficiency variation across the central operating region of all technologies is less than efficiency variation observed while sweeping parameters individually. Looking in more detail at the Figure, there are noticeable peak-efficiency points for different injected powers and this suggest that for simple P/N output stages, the optimum technology depends on the desired injected power. Also, the practical impact of using a higher voltage supply – that is, lower $\mu_n C_{ox}$ and so higher losses – result in a decreased efficiency, although the peak injected power available in the higher voltage processes may make the efficiency degradation an acceptable trade-off. Generally, this graph shows that for most devices available in low-voltage digital CMOS, there is promise for the use of Class-D as all can achieve competitive efficiencies, and that structures that can maximise $\mu_n C_{ox}$ and V_{DD} while minimising C_{ox} and V_{TH} could achieve very good efficiency vs injected power figures of merit.

3.5.4 Frequency

While the majority of effort so far has focused on the power efficiency and capabilities of the Class-D stage, it misses an important practical parameter: linearity. For Class-D structures, linearity is heavily influenced by the switching frequency – a higher switching frequency generally results in higher linearity, at least until switching non-idealities become significant – and so it is important to determine the magnitude of the impact of switching frequency on power efficiency, as this will determine what modulation methods would be appropriate.

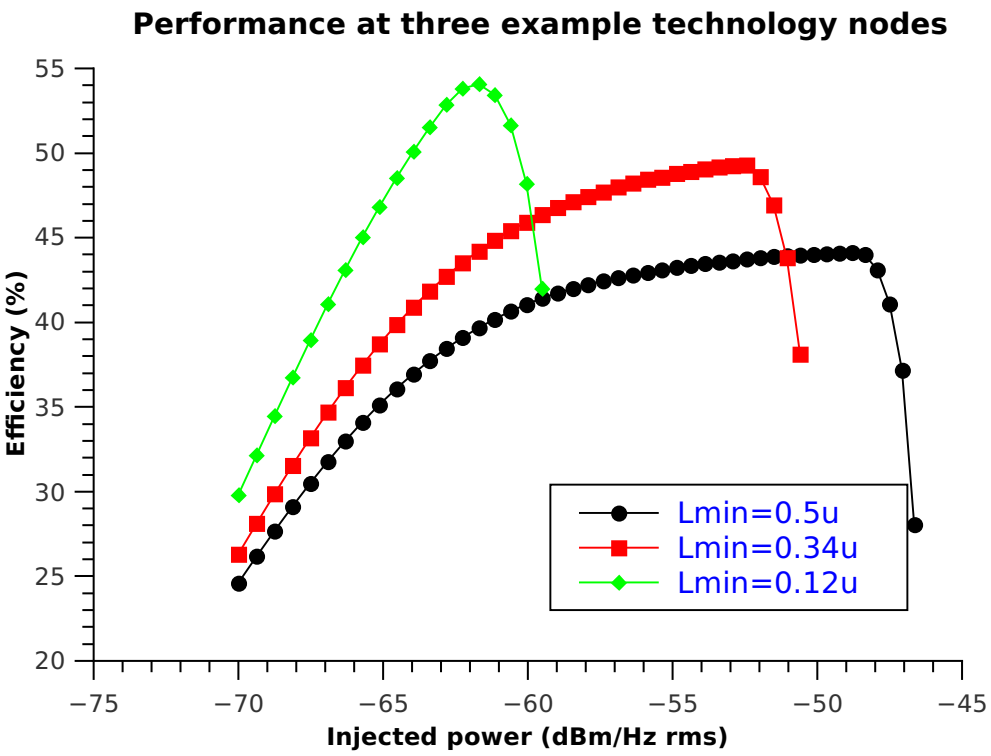

Figure 3.13: Class-D performance of a P/N totem pole at three technology nodes, approximately representative of 0.5μm, 0.34μm and 0.12μm technology nodes.

Figure 3.14 shows the power modelling results for the default model configuration with four switching frequencies: 100MHz, 200MHz, 400MHz and 800MHz. With an understanding of the dynamic loss mechanisms, it is unsurprising that increased switching frequency results in poorer efficiency. However, it is interesting to note that in the third, power-roll-off region of the graph, at certain power levels, higher frequency structures can be marginally more efficient than lower frequency structures. For example, at -54dBm/Hz, a structure at 200MHz can be slightly more efficient than a structure operating at 100MHz. This can be explained by the power consumption graph in Figure 3.11 which shows that capacitance related losses become constant in the power-roll-off region, while the parasitic resistance related losses increase. The parasitic resistance losses are dependent on frequency, but the switching-frequency related current flowing through R_{ON} is lower due to greater filter attenuation. As the switching frequency is increased further to 400MHz, this behaviour is no longer visible, however, as the rate of roll-off towards maximum injected power is too steep, and at 800MHz the efficiency-vs-power curve rolls off abruptly.

The conclusion from this Figure is that switching frequencies in the low hundreds of megahertz are the limit if efficiencies higher than with conventional Class-AB structures are desired.

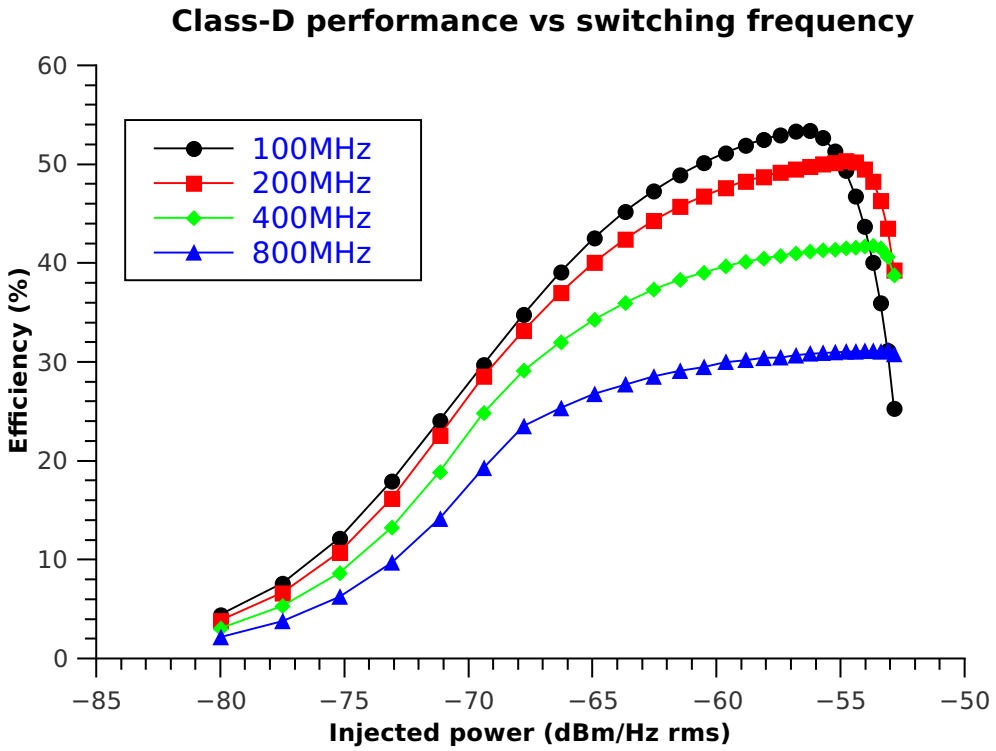

Figure 3.14: Class-D performance is modelled across a range of operating frequencies – 100MHz, 200MHz, 400MHz and 800MHz.

3.5.5 Filter

The energy storage capability of the LC filter provides the basis for efficient operation in Class-D amplifiers, so the impact of filter parameters on Class-D performance must be understood. The main parameters which are investigated are the filter order and filter type. While cut-off frequency is a major filter parameter, the effect of this follows on from the results of the other two parameters, so is not considered separately.

There are two complementary realisations for a given passive filter design, the "π" structure shown in Figure 3.15(a) and the "T" structure shown in Figure 3.15(b). It is important to choose the correct filter type for a Class-D system.

In a voltage-mode Class-D system, the output voltage should be determined according to the modulator – so that a two level output can be achieved with near-ideal zero-voltage switching operation – while the output current should primarily be determined by the low frequency input signal. As such, the output filter must be able to force a low-frequency current independent of the modulator voltage. The T-network has these properties due to its inductive input. To a first-order, the voltage of the V_{IN} connected terminal of inductor L4 is determined by the Class-D modulator while the other terminal

is approximately at a fixed voltage determined by capacitor C5. Hence the first inductor will integrate the voltage waveform and deliver a lower frequency current. If a π-based filter were used instead, voltage-mode Class-D would be extremely inefficient as the input capacitor would appear as a large parasitic output capacitance which has significant losses. This can also be considered in terms of the filters out-of-band impedance; the T-network has a high out-of-band impedance and so high frequency energy does not result in significant current flows, while the π network has a low out-of-band impedance and so high frequency energy is shorted to ground. All filters used from here on will be T-network structures.

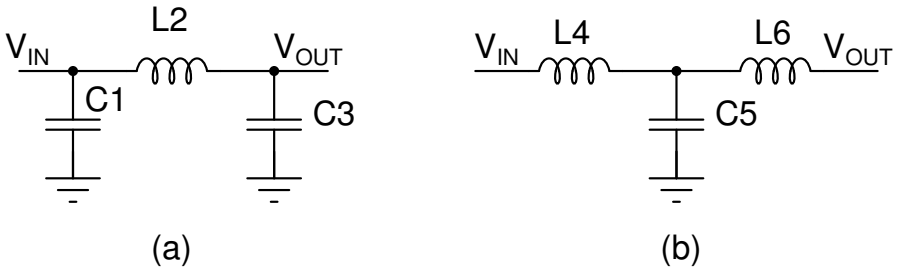

Figure 3.15: Alternate LC filter realisations: (a) "π" and (b) "T".

3.5.5.1 Order

To understand the effects of filter order on efficiency, the order of a Chebyshev type I filter was varied and for each order, an optimized Class-D design was generated using the Class-D power model, and the efficiency was calculated. The Chebyshev type I was chosen as it is appropriate for this application - it has a sharp roll-off near the transition so is good for low frequency Class-D, which has a switching frequency not far above the cut-off frequency.

All of the implemented Chebyshev type I filters have a 30MHz cut-off frequency, 0.1dB ripple and are singly terminated with the R_{load} and R_{ON} calculated by the model. Filters suffer from parasitic losses due to the series resistances of the filter components and so to represent this in the power dissipation model, the series parasitic resistance parameter R_{par} – which also includes routing and bond wire resistances – is increased by 0.1Ω for each additional component, from a starting point of 0.3Ω for no output filter.

Figure 3.16 shows the result of applying these filters to the default Class-D power dissipation model. The first order filter provides little attenuation of the switching harmonics, so in the time domain, a large switching ripple is present in the filter output signal. As the filter drives a resistive load, this in turn determines the current that flows in the Class-D output stage. The large switching ripple translates into a large switching

current flowing between the supplies and the LC filter, which results in high R_{ON} and R_{par} losses and so low efficiency.

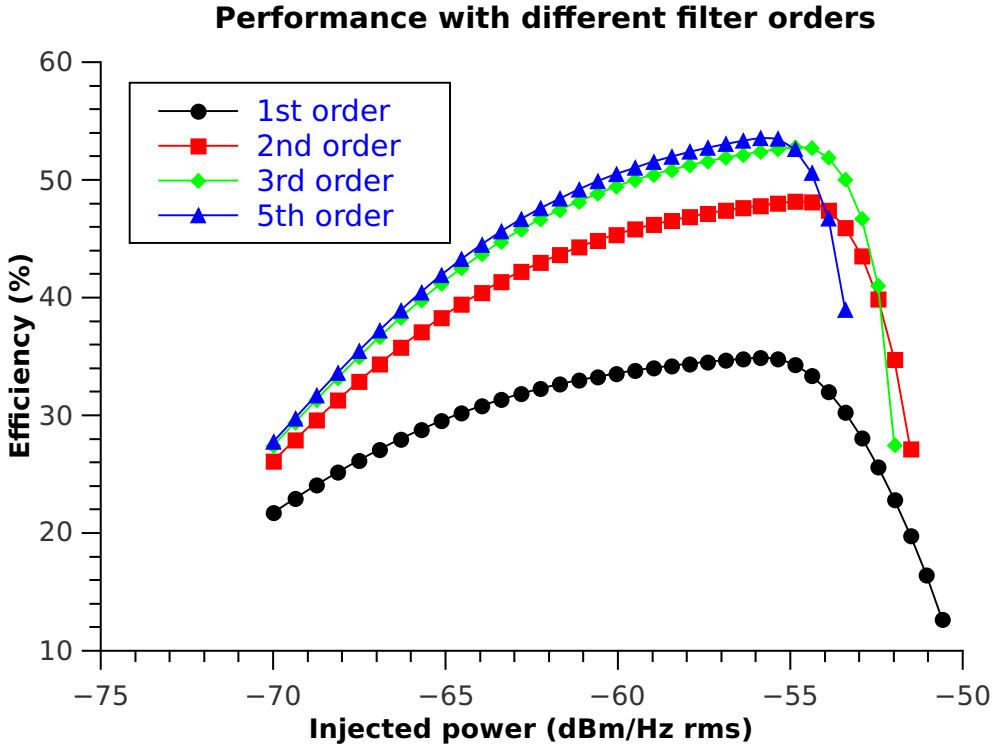

Figure 3.16: Class-D performance with various orders of Chebyshev Type I filter, all with 30MHz cut-off frequency and 0.1dB ripple, is examined.

Higher order filters reduce the amplitude of this switching current and give corresponding increases in efficiency, but there is little efficiency benefit to using orders higher than three as the efficiency improvement becomes negligible for higher orders. However, the increased component count and corresponding increased parasitic series resistance losses of higher order filters decreases the maximum-power point, where the high current levels mean significant voltage is dropped across the filter's parasitic resistances, reducing power that can be delivered to the load. As such, the filter order should be minimised to maximise efficiency, although other application-level requirements – such as the out-of-band emissions requirements in HPAV – may require a higher order filter, which is non-optimal in terms of efficiency.

3.6 Conclusion

This chapter has presented a power model which can quickly estimate the parasitic power dissipation of a Class-D output stage to an accuracy of 7% over a wide range of

operating and load conditions. The model can estimate the efficiency of hundreds of Class-D output stages per minute, so allows a rapid exploration of the Class-D design space without having to resort to slow transistor level simulations.

Using the model, some important key Class-D parameters have been investigated. The effect of transistor transconductance on efficiency was evaluated and while higher transconductance can significantly increase efficiency at medium output power around -60dBm/Hz, at high output powers above -55dBm/Hz the efficiency benefits of higher transconductance collapse. This occurs as the efficiency of the output stage becomes dominated by the supply voltage, the parasitic output resistance and the low load resistance.

Increasing the supply voltage improves efficiency by increasing the required load resistance, with the parasitic output resistance proportionally smaller. A higher supply also significantly increases the maximum injected power and suggests that high voltage structures are required for injected power levels greater than -55dBm/Hz.

Practical transistors usually combine both of the above effects such that as transconductance increases, voltage decreases, and the effect is that supply voltage becomes the primary design parameter. The minimum supply voltage which can achieve the required injected power should be used to achieve maximum efficiency.

The efficiency implications of switching large power transistors at hundreds of Megahertz have also been investigated and, while Class-D falls short of the ideal 100% efficiency, switching frequencies up to 200MHz should be achievable after which efficiency begins to degrade rapidly as switching frequency increases.

Finally, the reason Class-D is an efficient amplification scheme is due to the energy storage properties of its output filter and in particular its output inductor. Attention should be paid to the filter order used, a minimum of second order is suggested with third order being preferable as otherwise the Class-D output stage wastes effort over-charging the filter, then discharging the excess to ground. Higher order filters do not improve efficiency and with practical components which exhibit losses, are likely to reduce the achievable efficiency, although they may be required for EMC compliance. The filter characteristic has only a small impact on Class-D efficiency, so the filter characteristic should be first optimised to meet system requirements, with orders above three only being used if system requirements such as out-of-band emissions cannot be met with a lower order filter.

Chapter 4

NMOS-only output stages

4.1 Introduction

Output stages delivering Watt-levels of power are common in audio applications. At these high power levels, the output stage dominates system power consumption and so modest improvements in output stage efficiency can result in significant improvements of overall system power consumption and thermal dissipation. Audio exists in a demanding performance space; the human ear has a dynamic range of approximately 130dB and this means that ideally any distortion components generated by the power amplifier would have to be below -130dB relative to the fundamental. In order to achieve high linearities, audio power amplifiers often use highly linear Class-A output stages, although Class-AB output stages are more common as the power and thermal dissipation in Class-A stages delivering Watt-levels of power was prohibitively high.

With the advent of digital CMOS combining high speed operation and low cost digital signal processing, Class-D has emerged as a viable solution for highly linear audio power amplifiers. This is achieved using high orders of oversampling and noise shaping, which moves noise from low, in-band frequencies to high, out-of-band frequencies where it can be removed by linear filtering.

In communication systems, the high frequencies of operation mean that the switching frequencies can be considerably higher than those used in audio applications. However, the linearity requirements are lower. It is desirable to see whether the Class-D techniques developed for Audio power amplifiers can be used to improve the efficiency of communication line drivers.

The Class-D principle considers movement of charge from a supply at one voltage to

a load at another voltage, by taking advantage of the energy storage properties of ideally lossless passive components, specifically inductors and capacitors. However, practical Class-D implementations suffer from parasitic power dissipation in the form of on-resistance of the output switches, switch gate capacitance which must be charged and discharged each clock cycle, and shoot-through currents, as discussed in detail in Section 3.2.

The use of Class-D in high-frequency wide-band communication systems requires very high switching frequencies and if Class-D is to be practical, the gate charging losses must be reduced as they scale with frequency and can quickly come to dominate the system power consumption.

This chapter will present novel N/N totem pole class-D output stages based on charge pump architectures [92]. These structures provide gate area and switching loss reductions over existing circuits and are particularly suited to high-frequency operation with low supply voltages. Charge pump techniques allow improved gate drive over existing N/N totem pole circuits which obviate the need for large PMOS transistors in P/N stages (typically 3 times larger than the NMOS driver). The overall approximately 45% saving in gate capacitance reduces parasitic losses and lowers gate drive requirements on pre-buffering stages, which can also be made smaller and lower power. These techniques are also compatible with non-overlap driver sizings or circuits. Finally, all gate-oxide reliability criteria are respected during operation of the circuits.

4.2 Background

4.2.1 Charge pump structures

Charge pumps are switching structures which use charge storage in capacitors to generate DC voltages or switching signals, at voltages which may be outside of the range of the charge pump supply voltage.

Traditional charge pump structures such as the Dickson[93] charge pump are based on diode/capacitor circuits. Figure 4.1 shows one implementation, consisting of diode D1 and a pump capacitor C_p. Also included in the implementation is an output network consisting of a charge storage capacitor C_s and output diode D2. Starting with the assumption that the chargepump has reached a steady state, at the start of a cycle, diodes D1 and D2 will both initially be forward biased, with a forward voltage drop V_D, until V_{TOP} rises to $3.3 - V_D$ and V_P rises to $3.3 - 2V_D$, at which point current stops flowing through the diodes. The first pump phase begins with V_{CLK} rising to

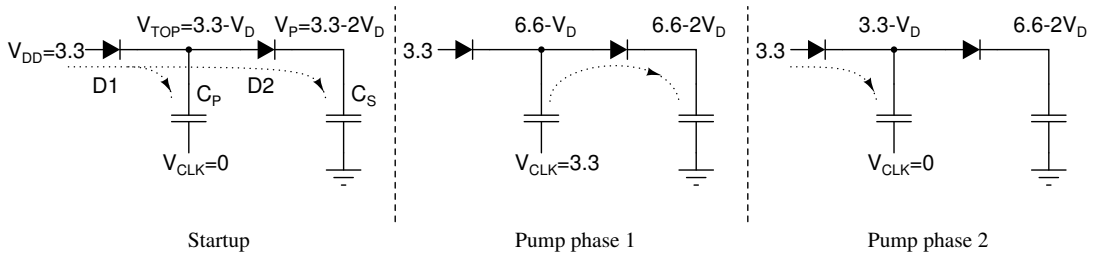

Figure 4.1: Dickson charge pump showing three phases of operation for a 3.3V single supply system. Dotted lines indicate the flow of charge during each phase. Voltages are the steady-state voltages at the end of each phase.

3.3V, forcing V_{TOP} to rise to $6.6 - V_D$ and reverse biasing D1 but strongly forward biasing D2. Charge on pump capacitor C_p can now flow on to storage capacitor C_s until it rises to $6.6 - 2V_D$ and D1 is only just forward biased. The charge pump now returns to phase 1 and the process repeats. At all times, the voltage across the diodes is kept to less than the supply voltage, so avoiding pushing the diodes outside their safe (voltage) operating region. In this structure, it is assumed that the capacitors can tolerate the high voltages present. In CMOS technologies where diodes are not readily available, the above structure can be adapted by replacing diodes with diode-connected transistors, with their gates connected to their drains, which changes the diode drop V_D to a gate-threshold voltage drop V_{th}.

The main drawback of this structure is that in low voltage CMOS implementations, V_{th} is typically around 0.5V and can become a significant proportion of the supply voltage, reducing the maximum pump voltage that can be generated. The problem stems from the diode drop preventing the pump capacitor from charging to V_{DD} and instead, only reaching $V_{DD} - V_{th}$. To eliminate this V_{th} loss, [94] proposed a cross-coupled NMOS configuration. Two instances of transistors and pump capacitors are used, but rather than diode connecting the two transistors, their gates are cross-coupled to the other transistor's drain, as shown in Figure 4.2. The pump capacitors are then driven by out-of-phase clocks. As shown in Figure 4.3 for a $V_{DD} = 3.3V$ system, the capacitor top nodes A and B undergo a number of start-up cycles until normal operation commences at t=15ns, until a voltage $2V_{DD}$ on node B set the V_{gs} of transistor MA to 3.3V, allowing node A to charge to 3.3V in the minimum time. When V_{CLK} and V_{CLKB} change phases at 20ns, the structure changes phase. Node A is pumped up to $2V_{DD}$ by a rising V_{CLK}, which fully turns on transistor MB, allowing it to charge node B to 3.3V. Additionally, the voltage doubler achieves this while keeping all of the transistor junctions within their recommended maximum-voltage operation region. As supply voltages in modern CMOS have decreased, the voltage and reliability benefits have become increasingly important.

State of art charge pumps, in particular those in low voltage technologies, are commonly

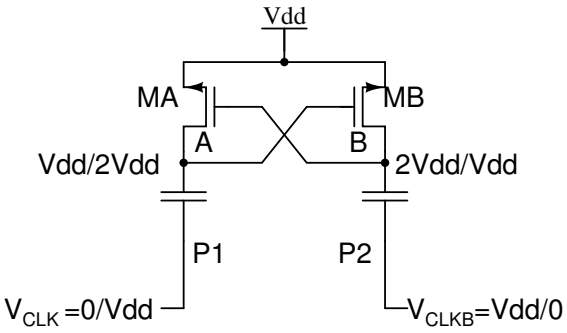

Figure 4.2: Positive voltage doubler circuit. A smoothing capacitor to create a stable $2V_{DD}$ rail is not required in this application.

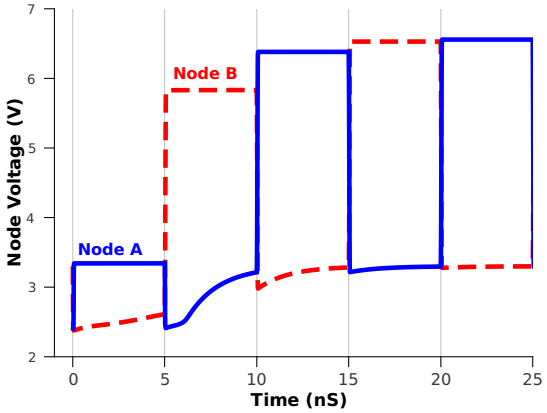

Figure 4.3: Voltage doubler start-up and operation of pump nodes A and B.

based on the voltage doubler structure with a charge storage output stage[92]. However, the voltage doubler structure has also found application in other areas, in particular, the bootstrapping of switches. In [95] the voltage doubler is used to provide a 0-6.6V swing on the gate of a switching implemented using a 5V device operated from a 3.3V supply, although this implementation does not consider gate-oxide reliability. In [96], the structure is improved to respect gate-oxide reliability in a bootstrapped switch application.

4.2.2 Class-D totem poles

4.2.2.1 P/N structures

The conventional P/N totem pole Class-D output stage is shown in Figure 4.4. To achieve equal pull-up and pull-down drive strengths, the pull-up PMOS transistor M_P must be significantly larger than the pull-down NMOS transistor M_N, due to the lower mobility of PMOS charge carriers than NMOS charge carriers. The PMOS is thus typically three times wider than the NMOS device, incurring three times the gate charge

losses of the NMOS. Additionally, this structure requires a separate non-overlap circuit to prevent shoot-through. In order to prevent shoot-through currents, M_P and M_N

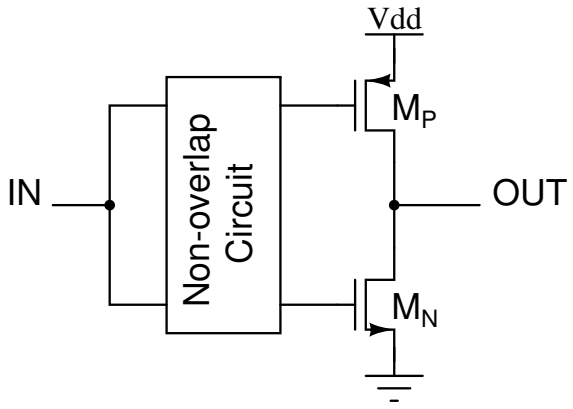

Figure 4.4: P/N totem pole output stage.

must be prevented from switching on at the same time. The traditional method of achieving this is to use a non-overlap clock circuit such as Figure 4.5, which separate the edges of the clock so that there is a period when both devices are off. Reducing the parasitic losses of the Class-D structure must start by reducing the losses due to the PMOS device, as this dominates overall output stage losses. A first step is to replace the pull-up PMOS switch with a pull-up NMOS switch, which halves the total output stage gate area which must be driven, and is termed a N/N totem-pole arrangement.

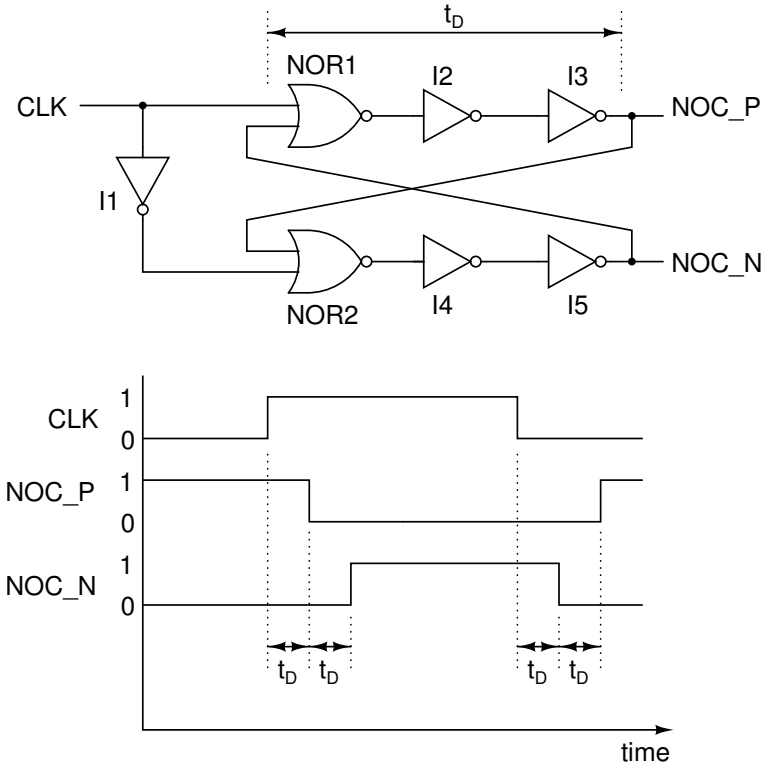

Figure 4.5: Non-overlap circuit and timing of input/output nodes.

However, this requires that the gate of the pull-up NMOS device must be driven beyond the positive supply rail, which is problematic for single-supply systems.

4.2.2.2 N/N structures

An established N/N totem pole arrangement for audio applications, which operates from a single output supply was presented in [97]. A diode-based Dickson charge pump is used to create a temporary high supply voltage to drive the pull-up NMOS device, as shown in Figure 4.6. However, the implementation of pull-up control signal, in_{high} is problematic, as the voltage in_{high} required to keep transistor M_H switched on rises up as the Class-D output voltage V_{out} rises. A multi-stage level-shifter structure operating from the V_{PUMP} supply is used, but this introduces significant complexity and delay to the operation of the output stage. While this delay is acceptable in low frequency audio applications, it becomes a limiting factor in high frequency communication systems. A second problem with above N/N totem pole solution is the use of a Dickson charge

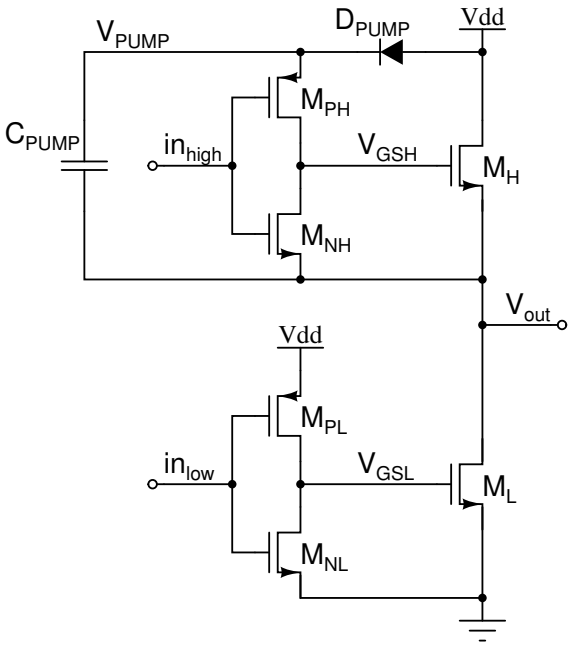

Figure 4.6: High voltage N/N totem pole Class-D driver [97].

pump. The structure was designed for a very high voltage, 72V, technology, and so the ratio of the diode forward voltage V_D to the gate-source voltage V_{GS} is low. However, in low-voltage implementations, this ratio becomes much larger and as a result, the gate-drive of the pull-up NMOS is reduced, which reduces some of the benefits of using a pull-up NMOS rather than a pull-up PMOS[98]. To compensate for the reduced V_{GS}, the size of the pull-up NMOS device must be increased, which is contrary to the original motivation for using an NMOS pull-up device.

As Class-D drivers are pushed to higher frequencies in lower voltage technologies, the benefits of using an N/N totem pole configuration increase, but the drawbacks of using high-voltage drivers in low voltage processes become more severe. Two new N/N totem pole drivers will now be presented, both of which address the problems in creating efficient high frequency, medium power Class-D output stages.

4.3 Proposed output stages

To address the problems of implementing high-frequency Class-D drivers in low-voltage CMOS processes, two new output stages have been developed, building on the the developments seen in low voltage, high-frequency charge pumps.

4.3.1 Class-AD/BD driver

A new N/N totem-pole output driver which addresses some of the limitations of the established N/N totem pole arrangement, has been developed. The new structure is a half-bridge output, so in a full-bridge configuration, is compatible with both AD and BD Class-D driver timings, and so is termed an *AD/BD Driver*. It is shown in Figure 4.7.

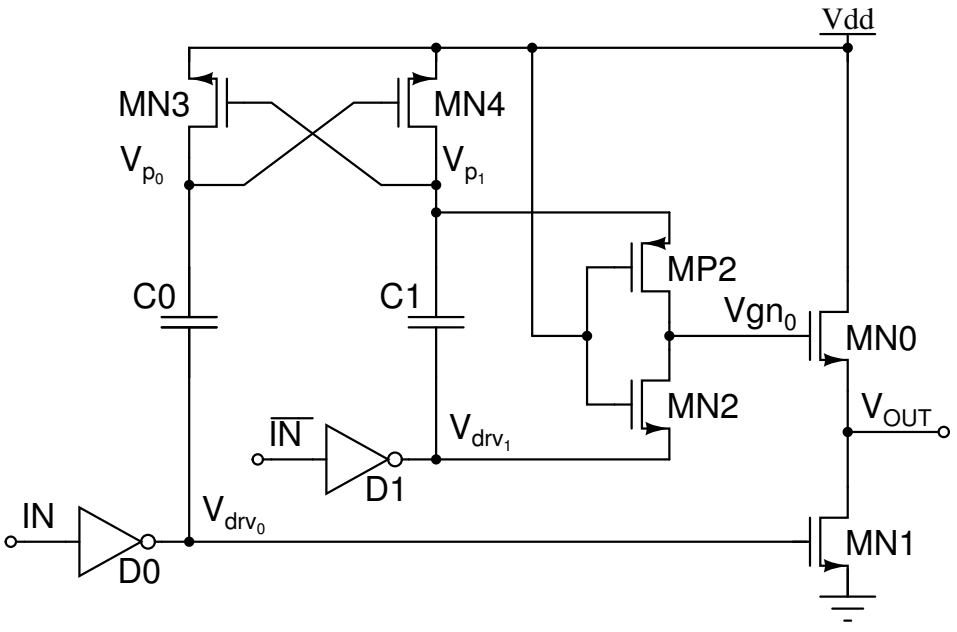

Figure 4.7: Charge pumped N/N totem pole output stage.

An N/N totem pole output stage arrangement, transistors $MN0/1$, is used. For V_{OUT}

to go low, $V_{GS_{MN1}}$ should be equal to the supply voltage V_{DD} and $V_{GS_{MN0}}$ should be $0V$, both of which can be generated by inverters with low and high inputs, respectively. For V_{out} to go high, however, $V_{GS_{MN1}}$ should be $0V$ and $V_{GS_{MN0}}$ should be driven to $2V_{DD}$.

The voltage doubler provides the basis for an N/N totem pole drive circuit, producing the high, $2V_{DD}$ voltage required to switch pull-up device $MN0$ fully on. In order to complete the circuit, it is emphasised that while the maximum swing across any two transistor terminals in the voltage doubler or the output stage is V_{DD}, the swing on node V_{gn_0} is from 0V to $2V_{DD}$, and no single node in the voltage doubler can provide this swing. The solution presented here notes that the pump capacitors $C0$ and $C1$ always maintain a charge of V_{DD}*C across them, and so can be used as a temporary supply rail. A P/N inverter structure can be connected across capacitor $C1$ but the inverter input is connected to the V_{DD} supply rail. A conventional inverter keeps the supply terminals apart by V_{DD} and the gate voltage is switched from 0 to V_{DD}. Here, the supply terminals are kept apart by V_{DD}, but are switched from 0 to V_{DD}, while the gate voltage is kept constant. When pump terminal V_{drv1} is low, MN2 will be on and MP2 will be off, and V_{gn0} is pulled to 0V. When pump terminal V_{drv1} is high, MN2 will be off and MP2 will be on, pulling V_{gn0} up to $2V_{DD}$ as V_{drv1} rises to V_{DD}.

To a first order, operation of the circuit is as follows. Initial conditions are $IN = 0$, $I\bar{N} = V_{DD}$, $Vdrv0 = V_{DD}$, $Vdrv1 = 0$, $Vp0 = 2V_{DD}$, $Vp1 = V_{DD}$, $Vgn0 = 0$ and $V_{out} = 0$. Transistors MN3, MP2 and MN0 are off while MN4, MN2 and MN1 are on. IN and $I\bar{N}$ are generated by a non-overlap circuit. A low-to-high output transition begins with IN rising, causing $Vdrv0$ to fall, turning MN1 off and preventing shoot-through current in the output stage, and turning MN4 off so setting the voltage doubler in a charge-storage state. $I\bar{N}$ will then fall, allowing $Vdrv1$ to rise, pumping $Vp1$ up to $2V_{DD}$. This turns MN3 on, charging Vp0 to V_{DD}, and turns MN2 off and MP2 on, charging $Vgn0$ to $2V_{DD}$. A high-to-low output transition follows a similar principle.

The two halves of the voltage doubler have different drive requirements. The MN4/C1 half must be sized to drive the large gate-capacitance of MN0, whereas the MN3/C0 half only needs to drive the much smaller parasitic capacitances at node Vp0. As Vgn0 is charged from pump capacitor C1, the ratio of C1 to the parasitic (gate) capacitance at node Vgn0 determines how close $V_{GS_{MN0}}$ can come to V_{DD}. A lower ratio means that the V_{GS} of MN0 will be lower that the V_{GS} of MN1 and so to match the on-resistance of pull-down device MN1, a larger device MN0 will be needed – which means that the gate capacitance and switching losses of MN0 will be increased. However, choosing C1 too large means a larger MN4 is needed, increasing the sizing requirements of MN3 and C0. More importantly, in order that the ΔV_{OD} can reach a reasonable fraction of the supply, C1 must be much larger than $C_{GS_{MN0}}$. The implications of this are that C1 can

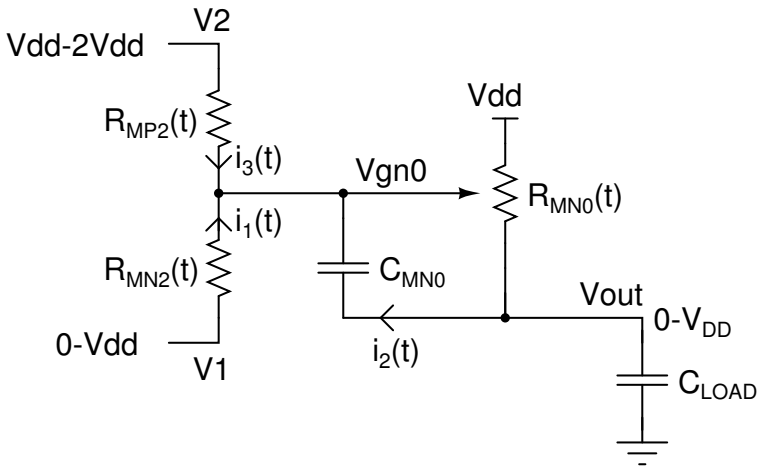

Figure 4.8: Simplified circuit around the $Vgn0$ node showing dynamic currents.

be quite large – 5-15 times the size of MN0 – and so choosing C1 too large comes with a significant area penalty.

This structure meets the static voltage requirements of a N/N totem pole drive circuit, but correct dynamic operation – that is, preventing any two transistor terminals experiencing a voltage difference greater than the supply voltage – requires careful sizing of the inverter $MP2/MN2$ as a race condition exists between the rise and fall of V_{out} and V_{gn0}. This will now be discussed for a rising edge at V_{out}, but the same principle applies to a falling edge at V_{out}, with appropriate modifications to the following description.

A simplified, resistor-capacitor representation of the on-resistances of switches MP2, MN2, MN0, the gate capacitance of MN0, and the load capacitance Cload, is shown in Figure 4.8. If V_{gn0} reaches $2\mathrm{V_{DD}}$ before V_{out} reaches $\mathrm{V_{DD}}$, the gate-source voltage of MN0 could be above the safe operating voltage of the device, resulting in reduced device lifetime or device destruction. During a low-to-high output transition, R_{MP2} is initially high impedance and R_{MN2} is low impedance, so V_{gn0} will charge from $V1$ through R_{MN2}. When V_{gn0} reaches the threshold voltage of MN0, V_{out} will start rising. This will cause a transient current i_2 to flow through the parasitic capacitance C_{MN0}, effectively increasing the rise of V_{gn0}. At some point, MP2 will turn on, allowing i_3 to contribute to charging V_{gn0}. At some point, i_1 will change direction as both MP2 and MN2 are on and Vgn0 is greater than voltage V1. This shoot-through current will temporarily delay the rise of Vgn0, but then the contribution from i_1 will fall to zero as Vgn0 exceeds V1, and charging of Vgn0 will continue from i_2 and i_3.

As the on-resistances $R_{MP2}(t)$, $R_{MN2}(t)$ and $R_{MN0}(t)$ are time-dependent and non-linear due to changes of operation regions, analytic solutions are not the most useful tool to find a solution. Instead, numerical simulations can be used to size MN2 and

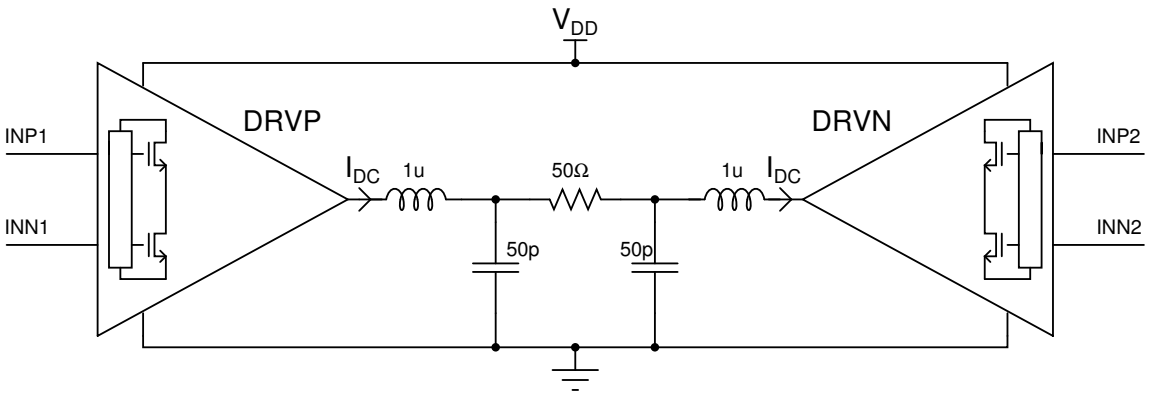

Figure 4.9: Class-AD/BD simulation setup.

MP2 such that the contributions of i_1 and i_3 do not unnecessarily delay the rise of Vgn0, but prevent over-voltage conditions occurring across the gate-source junction of MN0.

4.3.2 Simulations

The Class-AD/BD output stage was designed for a 50Ohm load and a 3Ω on resistance in a 0.13μm CMOS process with a single +3.3V supply, in a full-bridge configuration. Note that only transistors used are those with a thick oxide and a minimum length used is 0.34μm , the transistor properties are similar to that from a 0.35μm process.

As Class-D must be operated with an output filter, the simplest representative LC filter possible was used - a second order LC filters were used between the output point of the output stage and the resistive load, as shown in Figure 4.9. While Section 3.5.5.1 suggests an order of three is more appropriate to maximise efficiency, this work pre-dates the power modelling analysis and a second order filter was used instead. However, the filter is common to all structures examined in this section and so the following discussions are still valid.

The DRVP and DRVN blocks represents the circuit shown in Figure 4.7. The short term modulation of the signal is such that there is a DC current i_{DC} flowing from driver DRVP to DRVN. The following simulation show the operation of DRVP, with the the steady-state operation of DRVP involving current flowing out of the output stage. This is achieved by setting the duty cycle of the Class-D input signal to 90%.

Figure 4.10 shows the internal nodes as the output undergoes negative and positive transitions. With reference to Figure 4.7, drivers D0 and D1 are sized so that the gate-source voltages of MN0 and MN1, given by Vgs(MN0)=Vgn0-Vout and Vgs(MN1)=Vdrv0, have low crossing points in order to reduce shoot-through current, and this can be seen by their low crossing point and by the absence of shoot-through spikes in the drain

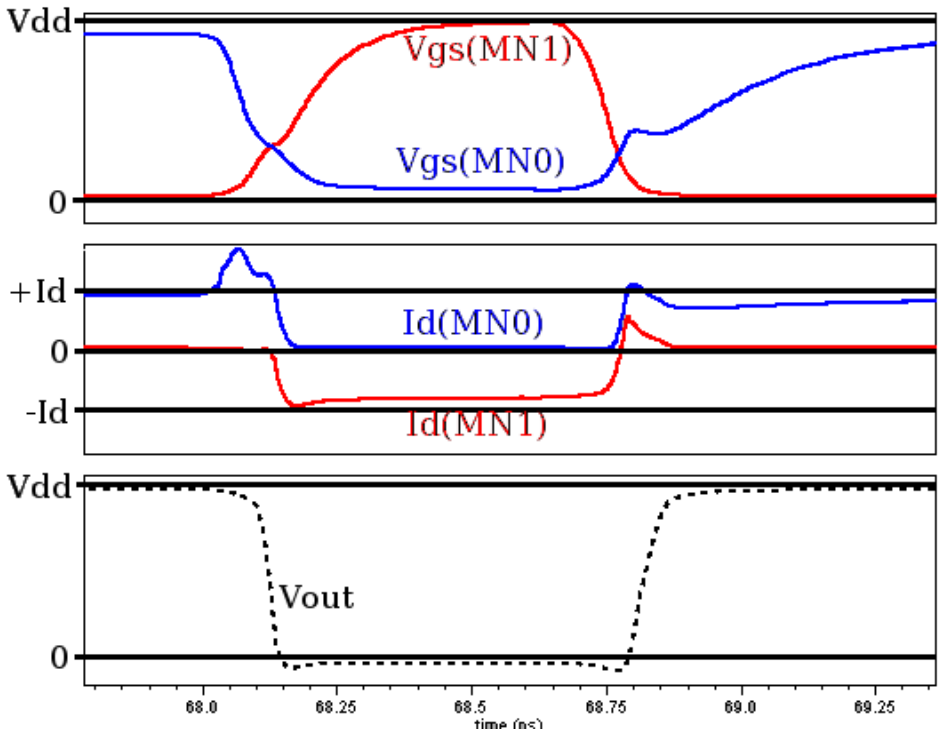

Figure 4.10: Timing diagram illustrating node waveforms while the output undergoes high-low and low-high transitions.

current waveforms of MN0 and MN1, denoted Id(MN0) and Id(MN1) respectively. As current is flowing out of the output stage due to the inductive load, the falling V_{out} transition is assisted by the output current, and so the transition will occur quickly as soon as Vgs(MN1) crosses Vgs(MN0). V_{out} will then continue falling to below the 0V supply until $V_{out} = -I_{out} * R_{ON}$. The rising edge of V_{out} is impeded by the output current and so a delayed transition takes place. Vgs(MN0) and Vgs(MN1) complete their output transitions, but the pulldown NMOS device continues to provide the output current until the MOSFET channel charge in the pull-down device is cleared, after which point V_{out} will transition high quickly. The effect of the fast negative and positive output edges can be seen on Vgs(MN0) and Vgs(MN1), as the fast output edges force an AC current through the gate-drain capacitance of output devices MN1 and MN0, stalling the gate-source switching waveforms while the output transitions.

Figure 4.11 verifies gate-oxide reliability criteria by examining all the junctions in the circuit which experience voltages greater than V_{DD}, except for the voltage doubler which is covered in Figure 4.3. With reference to Figure 4.7, devices MP2 and MN2 experience voltages greater than V_{DD}, but as the devices are referenced to Vdrv1 which also generates the $2V_{DD}$ signal, these devices are inherently safe from experiencing over-voltages, as shown at the top of Figure 4.11. The pull-up device MN0 can potentially be more problematic, but with appropriate device sizing, it is able to maintain safe voltages at all points of positive and negative transitions, as shown at the bottom of

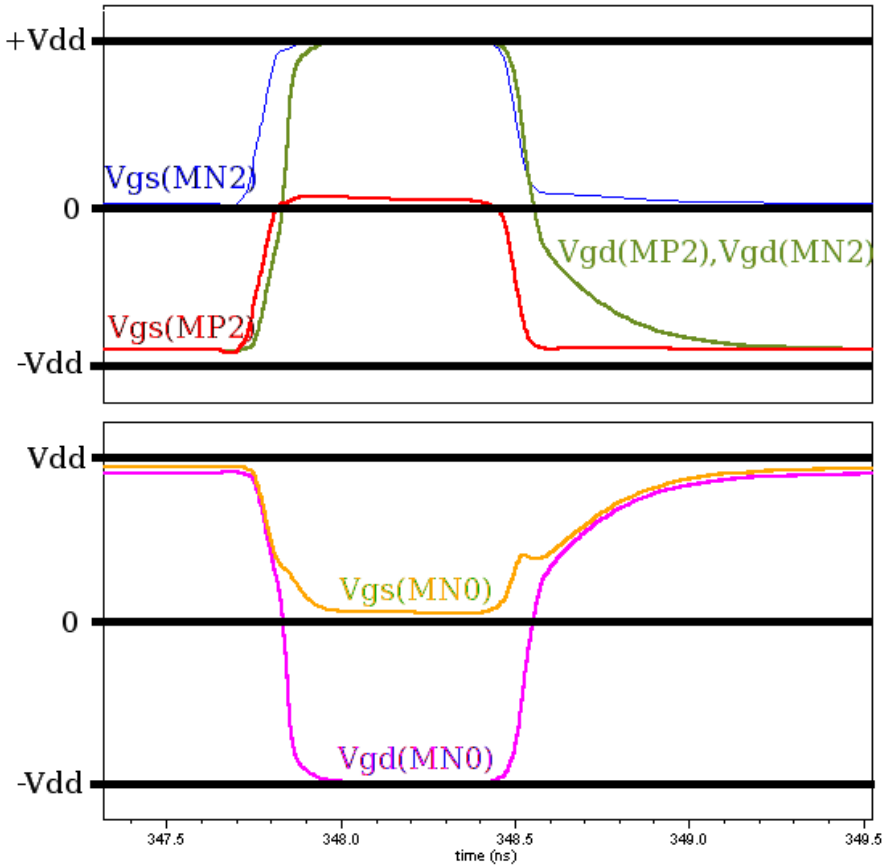

Figure 4.11: Class-AD/BD Driver gate-oxide reliability.

Table 4.1: Transistor sizes for the Class-AD/BD Output stage, R_{on}=3Ω.

Device	MN0	MN1	MP2	MN2	MN3	MN4	C0	C1
W (μm)	571.2	489.6	40	40	60	6	25.6	460.8
L (μm)	0.34	0.34	0.34	0.34	0.34	0.34	5	5

figure 4.11. Chosen device sizes are shown in Table 4.1. The input drivers D0 D1 are P/N inverters, with sizings as in Table 4.2.

4.4 Class-AD driver

For situations where the ability to independently drive both sides of an H-bridge, is not required (for example, in AD modulation), a simpler N/N totem pole output stage has been developed. As such, it is termed a Class-AD driver and is shown in Figure 4.12.

Table 4.2: Class-AD/BD driver output stage, P/N pre-driver sizings

Device	D0(PMOS)	D0(NMOS)	D1(PMOS)	D1(NMOS)
W (μm)	180	180	80	100
L (μm)	0.34	0.34	0.34	0.34

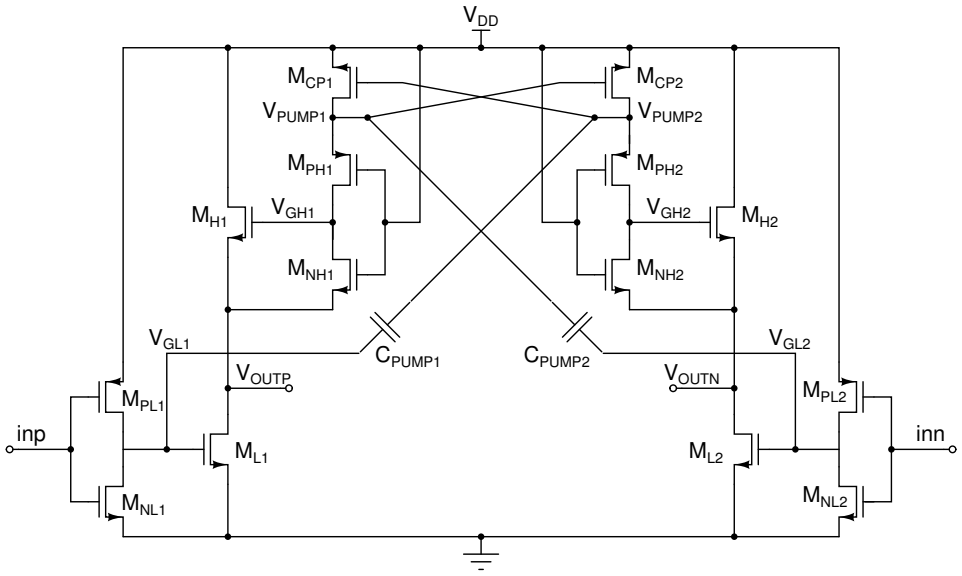

Figure 4.12: Cross-pumped NMOS-only Class-D output in H-bridge configuration.

The circuit is made of a N/N totem pole output stage ($M_{H1/2}$ and $M_{L1/2}$), charge pumped voltage doubler ($M_{CP1/2}$ and $C_{PUMP1/2}$), and high-side and low-side drivers $M_{PH1/2}$, $M_{NH1/2}$ and M_{PL1}, $M_{NL1/2}$, respectively.

The voltage doubler structure is used to drive node $V_{PUMP1/2}$ to $2V_{DD}$ without violating gate-oxide reliability conditions, but the structure is split across the two sides of a Full H-Bridge output structure, and pump capacitor drive signals are "cross-coupled" with appropriate nodes on the opposite half of the H-bridge, which should be driven by a complementary input. This reduces the component count in the output stage and saves a small amount of area.

The AD driver shown also removes one of the control signals from each side of the H-Bridge. The result is that only two control signals, *inp* and *inn*, are required, which should be 180 degrees out-of-phase from each other.

The removal of one complementary control signal on each side of the H-bridge means that the cross-coupled NMOS devices in the voltage doubler dictate pump node timings and so there are only two pump node states. A non-overlap circuit requires four pump node

Table 4.3: Component sizes for the Class-AD Output stage, for R_{on}=3Ω.

Device	M_{PL1}	M_{NL1}	M_{H1}	M_{L1}	M_{CP1}	M_{PH1}	M_{NH1}	C_{PUMP1}
W (μm)	48	64	550	500	64	96	32	150
L (μm)	0.34	0.34	0.34	0.34	0.34	0.34	0.34	15

states. As such, shoot-through current cannot be eliminated using a non-overlap clock generator, so must be addressed with another technique. In this circuit, non-overlapping pre-driver timings are used. MPL1/2, MNL1/2, MPH1/2 and MNH1/2 are sized such that the crossover point of Vgs_{ML1} and Vgs_{ML2} is close to the threshold voltages of MH1 and ML1.

The operation of the output stage is described with the aid of Figure 4.13, assuming all start-up transients have died out. The Class-D input signals inn and inp are buffered by inverters $M_{P/N\ L1}$ and $M_{P/N\ L2}$ causing V_{GL1} to start rising and V_{GL2} to start falling. Nodes V_{GL1} and V_{GL2} transition from 0V to 3.3V and from 3.3V to 0V, respectively, and directly control the gate of the output pull-down devices $M_{L1/2}$. The same nodes are also the input nodes of the voltage doubler made of $M_{CP1/2}$ and $C_{PUMP1/2}$, so also cause pump nodes V_{PUMP2} and V_{PUMP1} to transition from 3.3V to 6.6V, and 6.6V to 3.3V, respectively. On the left-hand side of the driver, the fall of V_{PUMP1} will cause V_{GH1} to fall and turn off pull-up device V_{H1}, allowing M_{L1} to pull V_{OUTP} to 0V. Similarly, on the right hand side of the driver, the initial fall of V_{GL2} will turn off pull-down device M_{L2} and the rise of V_{PUMP2} will switch on M_{PH2}, raising V_{GH2} to 6.6V, allowing pull-up device M_{H2} to pull V_{OUTN} to 3.3V.

The design considerations of the Class-AD driver are very similar to those for the Class-AD/BD driver, so will not be discussed separately here. Component sizes for the left-hand side of the output stage are given in Table 4.3 – transistors on the right hand side have the same sizes as their counterparts on the left hand side.

4.5 Performance

The goal of this work is to improve efficiency of high-frequency Class-D output stage structures and so in order to quantify the improvement, all four output structures discussed in the preceding section have been design and simulated: a conventional P/N output driver (PN), a diode-pumped N/N driver based on [97] (NN), a new charge pumped low voltage N/N driver (AD/BD) and a new cross pumped low voltage N/N driver (AD). All of the output stages have been designed for a 100MHz operating

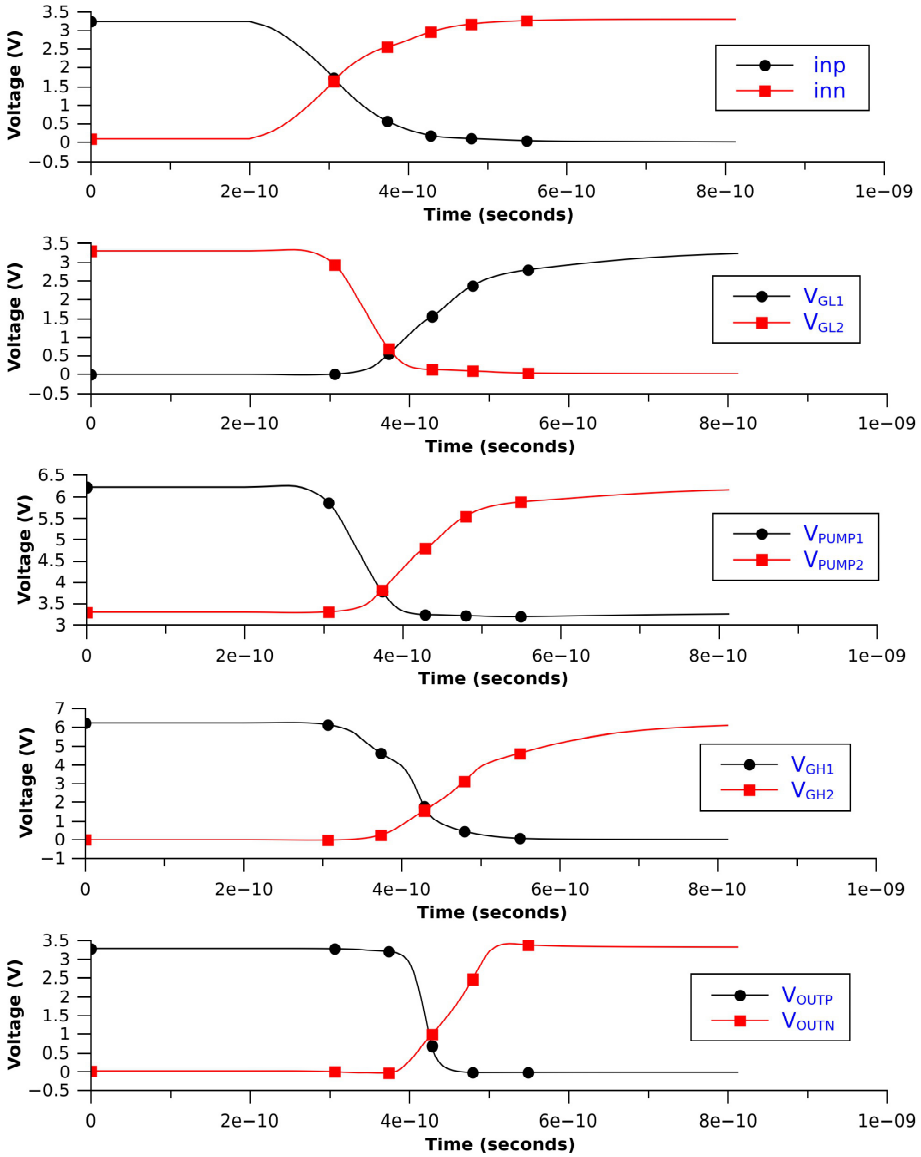

Figure 4.13: Voltage waveforms for the Class-AD N/N totem pole driver of Figure 4.12.

frequency and a 3Ω output impedance, with a L=1μH, C=50pF low pass filter between the output stage and the differential 50Ohm load.

Table 4.4 shows the area and efficiency performance of the compared output structures. The three main loss mechanisms are R_{on} losses, shoot-through losses and gate charging losses. Shoot-through losses are eliminated by using non-overlapping driver sizing techniques, and so the losses are determined by the on-resistance losses – which are identical for all of the output driver structures due to their identical on-resistance – and gate-charging losses. The N/N totem pole drivers achieve higher efficiency than the P/N driver due to their reduced gate area. As the dynamic losses are a function of frequency, Figure 4.14 shows the effect of frequency on overall output stage losses. At low frequency, the losses of all of the drivers converge, as dynamic losses become

Table 4.4: Performance comparison of this work* and other works.

	PN	NN [97]	AD/BD*	AD*
Driver on-resistance (Ω)	3	3	3	3
Pre-driver gate area (μm^2)	280	150	190	200
Output device gate area (μm^2)	690	380	330	330
Switched gate area (μm^2)	970	530	520	530
Diode/capacitor gate area (μm^2)	0	1725	1620	1500
Total gate area (μm^2)	970	2255	2140	2030
Efficiency at 100MHz (%)	79.2	82.6	83.4	82.8

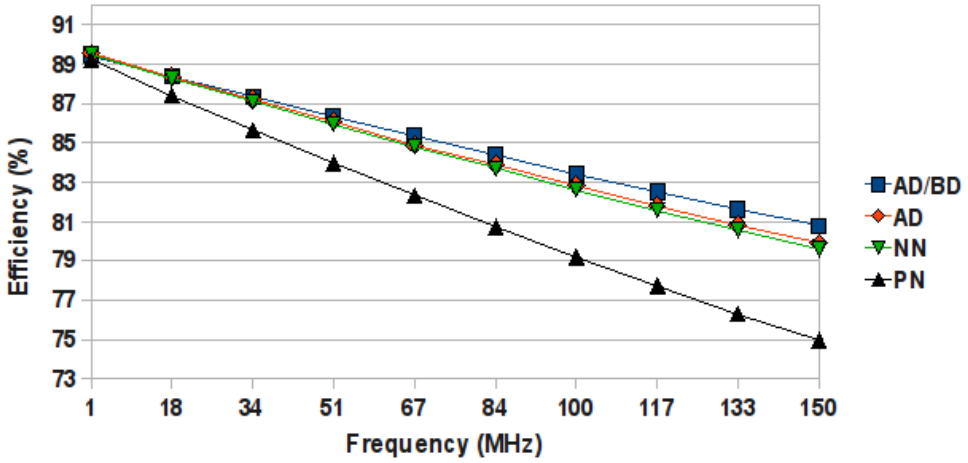

Figure 4.14: Simulated H-bridge efficiency variation with switching frequency.

negligible. At 100MHz, the AD/BD driver achieves an efficiency five percent higher than the P/N driver, which gives a noticeable improvement in power dissipation due to the high power consumed by the output stage. At even higher frequencies, these differences become even more significant.

It is observed that the total gate area of each of the N/N drivers is greater than that of the PN driver, due to the area overhead of the MOS capacitors and diodes. However, as the switched gate area that is charged for each input edge is significantly less in the N/N drivers than in the P/N driver, lower gate charging losses and so higher efficiencies are achieved for the N/N drivers, as is seen in the table.

A second aspect of the output stages is the distribution of area between the different output stages, and this is important when considering layout area requirements for an output stage. CMOS devices which connect to the outside world via package pins must be protected from ESD events. ESD protection structures which fit inside the bond

pads cannot be used for power pins such as supply rails or high power (line driver) outputs, so instead ESD layout rules must be used for any device which connects to a package pin. These layout rules typically include requirements such as spacing of devices, frequent substrate contacts and significantly extended gate-drain spacings. The impact of this is that in order to lay-out devices to ESD rules, $1\mu m^2$ of gate requires approximately $14\mu m^2$ of silicon area. In comparison, the layout area requirements of internal transistors is typically $4\mu m^2$ of silicon per $1\mu m^2$ of gate, and for MOS capacitors can be as low as $1.2\mu m^2$ of silicon per $1\mu m^2$ of gate.

The PN structure above is heavily made up of output devices, and so has a significant area penalty in layout due to ESD rules. The NN structure removes some of this output device area and replaces it with diodes and capacitors. While externally connected diodes also suffer from high silicon-gate area ratios, capacitors do not. The AD/BD and AD structures move the majority of output stage gate area into internal capacitors, which have low silicon-area costs per unit gate area, as they do not need to comply with ESD layout rules. The effect of this is an estimated 10% layout area saving when using the AD/BD or AD output stages compared to a conventional AD output stage.

4.6 Conclusion

In order to improve the efficiency of very high frequency Class-D output stages, two new N/N totem pole structures with an integrated bootstrapped pull-up device supply has been presented. The new structures do not require any external level shifters and so are able to achieve very small switching delays, allowing high frequency operation, with a targeted operating range between 100MHz and 150MHz. Charge-pump techniques are used to ensure maximum allowable gate-drive for the pull-up device, whilst respecting voltage-reliability constraints. Diode-losses incurred with Dixon-style bootstrap structures, which become significant in low voltage implementations, are avoided. By replacing I/O device gate area with MOS capacitance, the overall layout area is reduced as the latter does not require layout to ESD design rules.

The structure was verified using simulations in a 0.13μm process, using 3.3V I/O transistors to implement the Class-D output stage and can achieve an efficiency improvement of 7% over a comparable P/N totem pole structure, while reducing pre-driver power consumption and reducing switching delay.

Finally, it should be noted that the non-overlap mechanisms in the presented structures rely on matching the timing of the pull-up path to the timing of the pull-down path. As the process corner and device matching varies, the timing which minimises shoot-through current and minimises crossover distortion – when both pull-up and pull-down devices are

off – also varies. While it is possible to prevent shoot-through by designing for a worst-case corner, this results in excessive crossover distortion for the typical case. A better solution, suggested as further work, would include a calibration circuit to periodically alter the timing of the pull-up and pull-down paths to minimise shoot-through without significantly increasing crossover distortion.

Chapter 5

Wide band Class-D design

5.1 Introduction

The use of wide-bandwidth OFDM causes two problems for a communication system line driver. The high CF results in poor efficiency, typically 5%[99][100] for linear amplifiers such as those based on Class-AB[101] structures and while the efficiency problems can to some extent be ameliorated through the use of Class-G/H approaches, reported efficiencies are still low, around 17%[40][46]. Furthermore, the wide bandwidth, multi-tone nature of the OFDM signal prevents the use of efficient single-carrier resonant amplifier structures, such as Classes C/E/F[102]. Of the main amplifier classes, the remaining class is the Class-D[36][60][81] amplifier, which has demonstrated high efficiency at low frequencies – in particular, audio applications – but whose structure and circuit implementations have not been optimised for very wide bandwidth applications.

An important, practical consideration for wide band communication line drivers is their cost. It is usually cheaper to integrate all digital and analogue functionality on a single die, rather than having separate digital and analogue die. Additionally, OFDM in particular requires extensive digital signal processing hardware, but more generally the digitisation of the entire communication chain, except for the analogue front end, means that inevitably it is desirable for the analogue front end, including line driver, to be integrated in a digital CMOS process.

The goal of this chapter is to provide the necessary information to support the design of a Class-D line driver for the HomePlug AV standard in a UMC 0.13 μm digital CMOS process. It will cover relevant background material on the main Class-D structures and will, through justified reasoning, reduce these down to a single architecture, of which the theoretical performance limitations will be investigated in detail. An appropriate

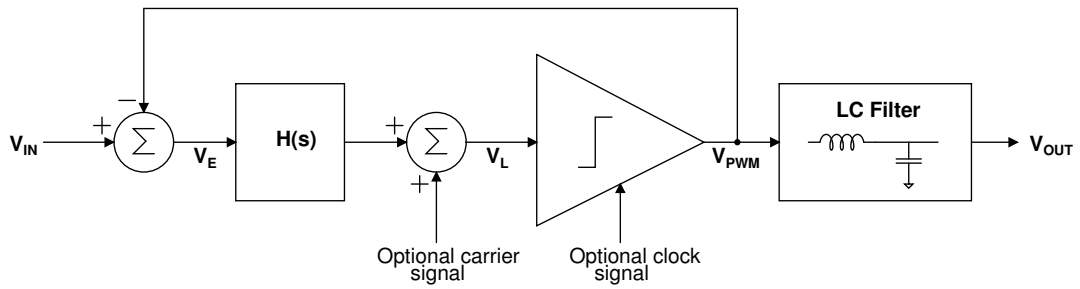

Figure 5.1: General structure applicable to the major types of Class-D system: Synchronous, PWM and Self-oscillating.

system-level design methodology will be described and, finally, a systematic method of taking the chosen architecture from concept to block-level realisation will be described.

This chapter will intentionally not focus on specific application or implementation details, or the parameterization of the blocks, as these will be discussed in detail in Chapter 6.

5.2 Background

5.2.1 Class-D architectures

The general structure of a Class-D line driver is shown in Figure 5.1. From left-to-right, it consists of a differencing block to compute the error between the comparator output V_{PWM} and the system input V_{IN}, a Loop Filter with transfer function H(s) which provides gain at low frequency and stabilizes the loop at high frequency, a comparator which computes the sign of the loop filter output V_L, and an LC output filter which removes high frequency switching energy from the comparator output V_{PWM}, leaving only low frequency content at output V_{OUT}. In some architectures, a carrier signal can also be summed with the loop filter input to synchronize the Class-D switching frequency; in other architectures the comparator is clocked.

As discussed very generally in Section 2.8.1.2, there are three main types of implementation of the structure above.

1. Synchronous/Sigma Delta modulators
2. PWM modulators
3. Self-oscillating modulators

Synchronous modulators, commonly called Sigma Delta modulators, are well described

in [52]. Briefly, they clock the comparator such that it samples the loop filter output and then outputs a level depending on whether the loop filter is above or below a threshold, at each clock edge. This is a sampling and quantizing operation and so introduces significant quantization noise. The quantization noise can be reduced by increasing the sampling (comparator clock) frequency, which is called "Oversampling". High oversampling ratios are used, typically on the order of 30-100, to spread the quantization noise over a much wider bandwidth than the signal bandwidth[52]. This improves the quantization noise level by 3dB for each doubling of sampling frequency.

In PWM modulators, the comparator is un-clocked and a triangular carrier signal is injected at the loop filter output. In self-oscillating modulators, the comparator is un-clocked and no additional carrier is injected – instead, the system will oscillate at a frequency where the loop phase shift is 180°. Although both architectures are topologically very similar to Sigma Delta modulators, they differ in that while the Sigma Delta can be considered as coarsely quantizing the input signal and then using an extremely high OSR to lower the in-band quantization noise, PWM and self-oscillating modulators instead map their input signal amplitude into the time domain using the edge positions of V_{PWM}. This mapping is performed in continuous time; it is not quantized. These schemes therefore do not introduce any quantization noise and so can accurately represent an input signal with a low oversampling ratio. Typical OSR's are in the range 3-30.

The wide signal bandwidth of the target application, combined with the high OSR requirements of Sigma Delta modulators, mean that a Class-D driver driven by a Sigma Delta modulator will operate at a very high frequency – certainly significantly higher than a PWM or self-oscillating modulator. It would therefore suffer from high switching losses, as was discussed in Section 3.5.4, and so the Synchronous Sigma Delta with clocked comparator is unsuitable for wide band Class-D, and so will not be considered further.

5.2.2 Loop gain and stability

While PWM and self-oscillating modulators both work on the same principle, they have different loop bandwidth and stability limits. Assuming $H(s)=1/s$, and representing the small signal comparator gain by the term N_A, it is known from [103] and [104] that the loop gain at frequency f for PWM is given by Equation 5.1 and for self-oscillating

modulators by Equation 5.2, where f_{pwm} is the switching frequency of the modulator.

$$H(f)\,N_{Apwm} = \frac{2}{\pi}\,\frac{f_{pwm}}{f} \tag{5.1}$$

$$H(f)\,N_{Aso} = \frac{1}{\pi}\,\frac{f_{pwm}}{f} \tag{5.2}$$

For equivalent PWM and self-oscillating loops, the self-oscillating loop will have twice the loop gain of the PWM loop. Additionally, it is known from [103] and [97] that PWM loops will become unstable if the loop gain at the signal frequency is less than unity, whereas self-oscillating loop are do not share this constraint.

For these reasons, in applications such as wide band line drivers where the oversampling ratio must be very low due to the desire to minimise switching frequency while achieving a wide bandwidth, self-oscillating modulators are superior as they can achieve a certain amount of loop gain with half the switching frequency as the equivalent PWM system and without the risk of instability.

5.2.3 Distortion in Class-D

Until now it was assumed that both PWM and self-oscillating modulation perform a perfectly linear amplitude-to-time conversion, however this is not the case; most implementations do create harmonic distortion as part of the modulation process.

In addition to harmonic distortion, all PWM/self-oscillating modulators create switching energy at multiples of the switching frequency. The switching frequency mixes with the input signal frequency components and gives rise to intermodulation products around the switching frequency and multiples of the switching frequency. This is not distortion in the classical sense because it does not appear at an integer multiple of the input frequency, but for the purposes of this discussion it will still be treated as a form of distortion.

A final form of distortion comes from component non-idealities such as finite rise/fall times of the output square wave, or finite bandwidth of internal amplifiers. These can affect both the harmonic distortion levels and the switching component levels.

To understand the modulation distortion mechanisms of self-oscillating loops, it is useful to start by examining the distortion mechanisms of PWM modulators. Modulator distortion in both PWM and self-oscillating architectures shares a common cause, but there is one PWM configuration which does not produce modulation distortion and so it is useful to examine this, in order to compare it to a PWM configuration which does produce modulation distortion.

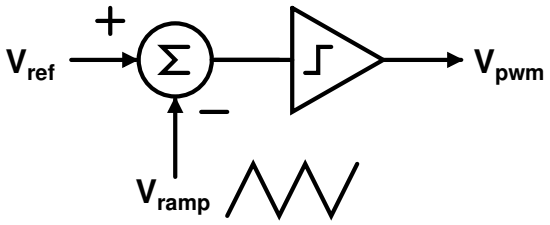

Figure 5.2: Open-loop PWM generating structure.

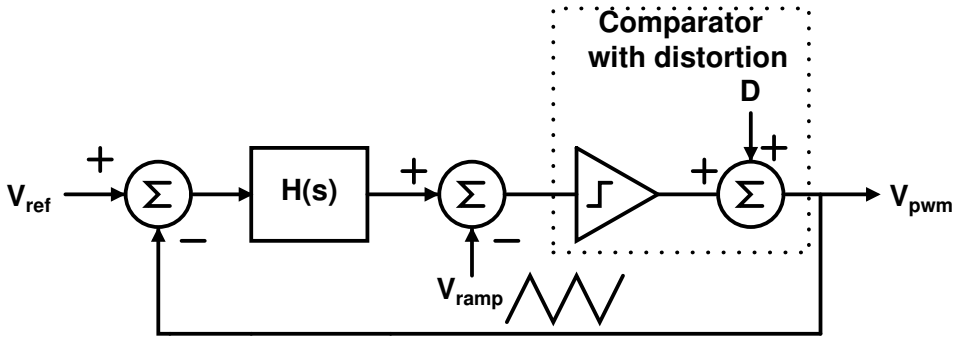

Figure 5.3: Closed-loop PWM generating structure. The open-loop PWM generator is embedded in a negative feedback loop. The term d represents distortion being added at the output of the comparator due to non-ideal comparator implementation.

Ideal open-loop PWM as shown in Figure 5.2 compares an input V_{ref} against a perfect triangle signal V_{ramp} using an ideal comparator with a Class-D output stage. The transition points of V_{pwm} will be exactly linearly proportional to the input signal amplitude, so a perfect amplitude to time conversion is obtained and no in-band harmonic distortion is created[55]. Note that the scheme does still produce intermodulation components between the input signal and the switching frequency which repeat at $mf_{switch} \pm nf_{in}$, where $n \in 1, 2, 3, ...$ and $m \in 1, 3, 5, ...$ These components decay in amplitude as n and m increase and provided that there is sufficient frequency separation between the signal band and the switching frequency, these components will have decayed below the noise floor once they are in-band and so can be ignored. Ideal open-loop PWM is thus considered distortion-free.

Unfortunately, in practise, open-loop PWM suffers from non-idealities such as finite rise/fall times of the V_{pwm} signal and assuming some supply impedance, the comparator supply voltage (and so the PWM output voltage) become dependent on the signal V_{ref} leading to harmonic distortion. Further, the structure has no power supply rejection, so any noise on the comparator supply will appear directly at V_{pwm}. These problems can severely limit the performance of open loop PWM system.

To overcome the practical implementation problems in open-loop PWM, it is common to embed the open-loop PWM modulator in a negative feedback loop as in Figure 5.3.

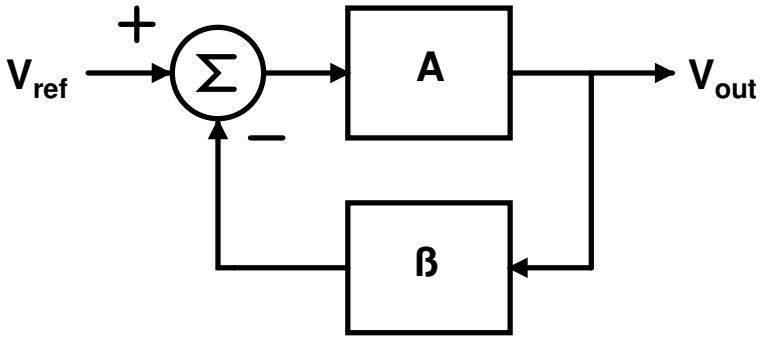

Figure 5.4: General model of a loop which can oscillate. Variables A and β can be fixed values or frequency dependent terms. V_{ref} is an optional external input which can be used to force the oscillation state such that the low frequency content of V_{OUT} is proportional to V_{ref}.

Techniques based on linear system analysis can then be used to show that any distortion or noise present at the comparator output, lumped into the term D, is attenuated at low frequencies by the loop gain. Note that the comparator is a non-linear element and so conventional linear analysis can not show this directly, but using the Describing Function method[105], an equivalent low frequency linear gain N_A can be determined for the comparator and then the linear system analysis can proceed as normal. If $H(s) = 1/(s/\tau)$, then the approximate linear output equation is:

$$\mathrm{V_{out}} = \mathrm{D}\,\frac{s}{s+\tau\,\mathrm{N_A}} + \mathrm{V_{ref}}\,\frac{\tau\,\mathrm{N_A}}{s+\tau\,\mathrm{N_A}} \tag{5.3}$$

It is straight forward to see that at frequencies below τN_A, the loop attenuates any distortion injected by D. However, while this analysis is instructive, it misses an important point: when open loop PWM is embedded in a feedback loop, the PWM modulation process is no longer inherently distortion free. This is explained in [106] as being due to the "ripple signal", which is the comparator output signal filtered by H(s) as it appears at the comparator input. The ripple signal is not a linear ramp; it contains intermodulation sidebands at $f_{switch} \pm nf_{in}, n \in 0, 1, 2...$ as in open-loop PWM and when they are fed back to the comparator input, they intermodulate with the carrier signal and the ripple sidebands are down-converted into the signal band. This is often called "aliasing error" and results in harmonic distortion.

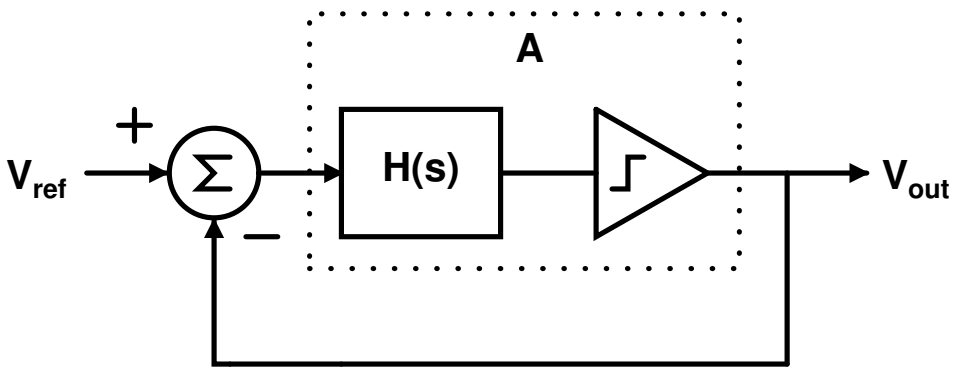

Figure 5.5: General model of a self-oscillating loop which corresponds to the structure of the basic negative feedback loop in Figure 5.4.

5.3 Self-oscillator theory

5.3.1 Oscillation frequency

Feedback loops such as in Figure 5.4 can maintain a stable oscillation, called a limit cycle, if the Barkhausen criterion given by Equations 5.4 and 5.5 is met. Self-oscillating Class-D amplifiers use this structure but often set $\beta = 1$ and replace block A with a loop filter and comparator as in Figure 5.5.

$$\angle \beta \mathrm{A} = 2\pi \mathrm{n}, \mathrm{n} \in 0, 1, 2, ... \tag{5.4}$$

$$\mid \beta \mathrm{A} \mid = 1 \tag{5.5}$$

The self-oscillating frequency of a particular loop will depend on the implementation details of the loop filter H(s) and the comparator, and involve different ways of introducing the required phase shift in the loop. The magnitude criterion is met automatically as if the oscillation signal is too large the gain of the comparator will reduce as the comparator output levels are fixed, regardless of the comparator input amplitude. There are three main methods of achieving a particular oscillation frequency:

1. Phase-based loops such as [36] use a loop filter with order three or greater, where the filter poles are chosen so that the loop filter phase response crosses -180° at the desired oscillation frequency. For a loop filter consisting of n identical poles with time constants τ_p, the self-oscillation frequency is given by Equation 5.6[36].

$$\mathrm{f}_{\mathrm{so}_{\mathrm{phase}}} = \frac{\tan(\frac{\pi}{n})}{\tau_p} \tag{5.6}$$

2. Hysteresis based loops such as [107] use a comparator which has a hysteresis window. The hysteresis window is measured in units of Volts and the integrator time-constant

τ_{int} is measured in Volts per second. Together, the result is similar to a time delay through the comparator which contributes a frequency-dependent phase shift. Assuming an ideal integrator loop filter, the resulting oscillation frequency is given below[108], where M is the modulation index defined by $M = 2D - 1$, D is the duty cycle ratio of the output pulse signal, V_{hyst} is the height of the hysteresis window and $t_{d_{hyst}}$ accounts for any parasitic time delay in the comparator.

$$f_{so_{hyst}} = \frac{1}{4} \frac{(1 - M^2)}{\tau_{int} V_{hyst} + \frac{1}{2} t_{d_{hyst}} (1 + M^2)} \tag{5.7}$$

Note that in hysteretic loops, $t_{d_{hyst}}$ is usually assumed to be small, and the self-oscillation frequency is determined mainly by V_{hyst} and τ_{int}. In this case, Equation 5.7 simplifies to Equation 5.8.

$$f_{so_{hyst}} = \frac{1}{4} \frac{1 - M^2}{\tau_{int} V_{hyst}} \tag{5.8}$$

3. Delay-based loops such as [109] use a comparator which has a fixed delay element in series with its input or output, providing a time delay of t_d. The delay corresponds to a linear phase shift with frequency and with the common first-order integrator loop filter, will oscillate at a frequency given by Equation 5.9[108].

$$f_{so_{delay}} = \frac{1 - M^2}{4 t_{d_{delay}}} \tag{5.9}$$

For low frequency audio applications, the hysteretic self-oscillating loop is most common as it has higher loop gain than the delay loop[103] and has better inherent distortion characteristics than the phase based loop[108]. However, for wide band Class-D, the required self-oscillation frequency is much higher than in audio applications and so the required self-oscillation period drops. The phase shift contribution from the comparator's parasitic delay then becomes non-negligible, or even comparable to the phase shift due to the hysteresis window. The hysteretic loop gain then drops to that of a delay based loop.

Given that the loop gain of the hysteretic and delay-based loops will then be comparable in a wide band system, it is useful to consider the relationship between $t_{d_{delay}}$ and $t_{d_{hyst}}$ for a particular desired oscillation frequency. Equations 5.7 and 5.9 can be equated and solved for $t_{d_{delay}}$, and the result is given in Equation 5.10

$$t_{d_{delay}} = t_{d_{hyst}} + \frac{2 V_{hyst} \tau_{int}}{1 + M^2} \tag{5.10}$$

This shows how the phase shift of the hysteresis window contributes to time delay (or phase shift) in the overall loop; the factor $\frac{2 V_{hyst} \tau_{int}}{1+M^2}$ can be considered as an additional

time delay. More significantly, it also shows that if the delay is fixed for both architectures, for example a parasitic delay at the output of the comparator due to the need for a buffer chain to drive large output devices, then $t_{d_{delay}} = t_{d_{hyst}}$ and so the delay-based loop will be able to operate at a higher frequency than the hysteretic loop as it avoids the term $\frac{2V_{hyst}\tau_{int}}{1+M^2}$.

Fundamentally, there is a trade-off between improved loop gain in a hysteretic loop and improved switching frequency in a delay loop and as the hysteretic loop is pushed to higher frequency, it converges towards being a delay based loop, assuming some fixed minimum delay in the system. The only benefit of using comparator hysteresis would be to address a circuit level implementation issue such as noise at the comparator decision point causing glitches in the comparator output. At the high frequencies being considered here, it is not sensible to consider any further the hysteretic loop as a self-oscillation architecture.

Similarly, pure phase loops are unrealistic at wide bandwidth, as Equation 5.6 contains no reference to parasitic comparator delay. Instead, the following general equation can be derived using the general structure in Figure 5.5 and the Barkhausen phase criteria in Equation 5.4, which combines and generalises the equations for the delay and phase based loops and can be solved with a particular loop filter $H(s)$ to find the oscillation frequency of any phase and delay based system.

$$\angle H(j2\pi f_{so}) - 2\pi f_{so} t_d = -\pi \tag{5.11}$$

For the common case of $H(s) = 1/s$, $\angle H(j2\pi f_{so}) = \frac{\pi}{2}$ and Equation 5.11 can be rearranged to find the required t_d for a desired oscillation frequency f_{so}, as in Equation 5.12.

$$t_d = \frac{1}{4f_{so}} \tag{5.12}$$

In summary, at high self-oscillation frequencies where the comparator parasitic delay reaches the same order of magnitude as the self-oscillation period, the three architectures converge into one - a phase-delay self-oscillating loop.

5.3.2 Distortion analysis

A formal analysis of distortion in self-oscillating loops with sine wave input signals has been presented in [53]. For completeness, the method will be summarised here.

As briefly discussed above, linear analysis of loops containing an element with a non-linear input-output transfer function – such as a comparator – can be performed by replacing

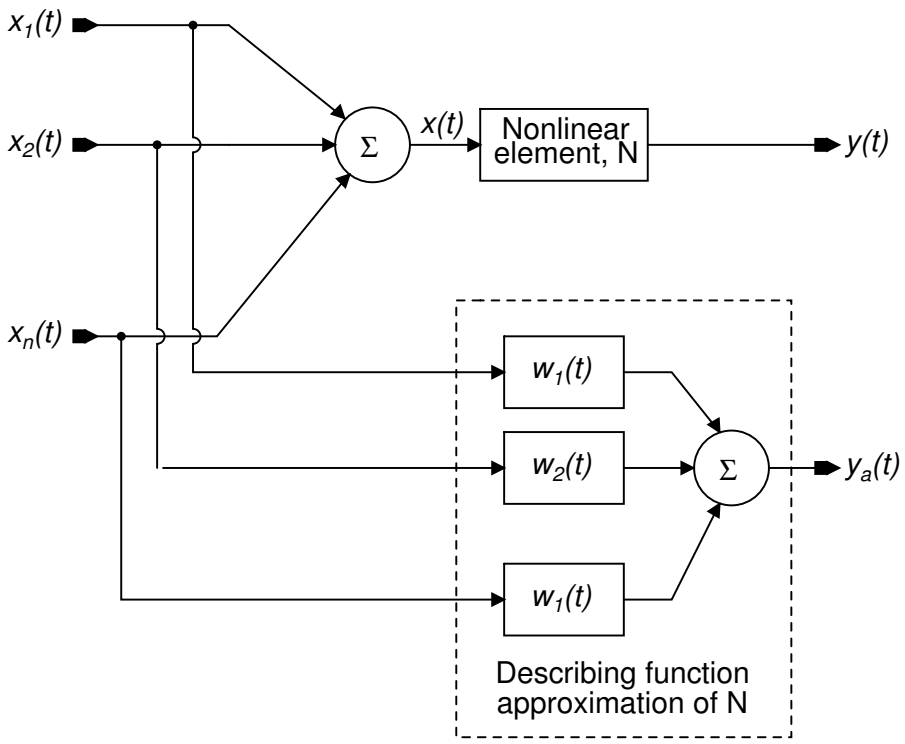

Figure 5.6: Describing function approximation for a nonlinear element. Based on [110].

the non-linear element by its Describing Function, which is described in detail in [110].

As shown in Figure 5.6, the Describing Function method splits the nonlinear element input $x(t)$ into components $x_i(t)$ according to their type, such as a sine wave at a frequency, a DC offset or a random signal. Weighting functions w_i are then chosen to minimise the mean squared error between $y(t)$ and $y_a(t)$ and will be a function the signal components $x_i(t)$ in the system. After taking the Fourier transform of the system, the describing function is obtained; it is the scaling function which relates the amplitude and phase of a frequency component at the input of a nonlinear element, to the amplitude and phase of the same frequency component at the output of the nonlinear element. It is written as $N(A)$, which would be a describing function that depends on one input signal A. In order to use linear analysis techniques on a loop containing a nonlinear element such as Figure 5.5, the describing function would replace the nonlinear element.

Tables of describing functions for common types of non-linearity are given in [110]. For distortion calculation of a self-oscillating modulator, the most useful describing function is the two-sine-wave-input describing function (TSIDF), which is used when there are two significant sine wave components present at the input of the non-linear element. In this case, those two components are the self-oscillating frequency component and the input sine wave. The describing function tables include an entry for an ideal relay, which is a good approximation of a comparator, and the TSIDF for this is given in

Equation 5.13.

$$N_B(A,B) = \frac{V_{\mathrm{DD}}}{\pi\, B}\left(\frac{B}{A}\right)\, {}_2F_1\left(\frac{1}{2},\frac{1}{2};2;\left(\frac{B}{A}\right)^2\right) \tag{5.13}$$

In this equation, $N_B(A,B)$ is the describing function for the comparator input component B as a function of signals A and B, where A is the amplitude of the self-oscillating frequency component at the comparator input and B is the amplitude of the error signal frequency component at the comparator input. ${}_2F_1$ denotes the 2-1 hypergeometric series.

The hypergeometric series can be expanded out to the first two terms as in Equation 5.14 in order to determine the harmonic distortion generated by the comparator.

$$N_B(A,B) = \frac{V_{\mathrm{DD}}}{\pi\, A} + \frac{V_{\mathrm{DD}}\, B^2}{8\pi A^3} + O\left(\frac{B^4}{A^4}\right) \tag{5.14}$$

The second term in this equation shows that an input sine wave B will be multiplied by B^2, so will generate third-order distortion according to Equation 5.15.

$$\sin(t) \times \sin^2(t) = \sin^3(t) = \frac{3}{4}\sin(t) - \frac{1}{4}\sin(3t) \tag{5.15}$$

To compute the level of third harmonic distortion, A and B must be determined. The limit cycle amplitude A will be significantly larger than B, the amplitude of the input signal under feedback, and so initially B can be neglected and the single sinusoid describing function $N(A) = \frac{2\mathrm{V_{DD}}}{\pi\,\mathrm{A}}$ can be used to replace the comparator in Figure 5.5. The value of A can then be solved using Barkhausen equations. First, the self-oscillation frequency is computed by solving Equation 5.4, and then resulting frequency can be substituted into the solution of 5.5 which is then solved for A.

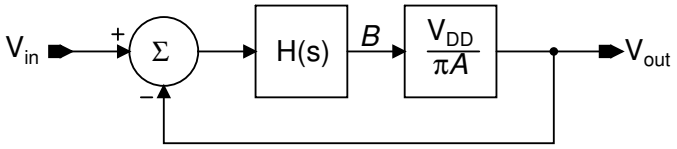

Figure 5.7: Structure used to calculate B, the amplitude of the input signal under feedback at the input to the comparator.

To calculate B, the comparator in Figure 5.5 can be approximated by the first term of Equation 5.14, as shown in Figure 5.7. The distortion term is usually much smaller than the B, which allows the second term of Equation 5.14 to be neglected. Solving the loop for B results in Equation 5.16, where $\mathrm{V_{in}}$ is the input sine wave amplitude.

$$B = \frac{\mathrm{H}(s)\,\mathrm{V_{in}}}{1 + \dfrac{\mathrm{H}(s)\,\mathrm{V_{DD}}}{\pi\, A}} \tag{5.16}$$

The distortion described by Equations 5.14 and 5.15 can modelled as shown in Figure 5.8.

Care should be taken with this model – it is only applicable for signals at three times the frequency of V_{in}. As the distortion is injected at the output of a loop in feedback, it will be attenuated by the loop gain. The describing function of the comparator for the third order distortion term must be updated to be that for a three-sinusoid describing function (limit cycle, input signal and third harmonic) and in this case the comparator describing function has an additional factor of $\frac{1}{2}$ versus the comparator TSIDF in Figure 5.7. Solving this loop for $V_{out_{\omega_{in}}}$ gives the amount of third harmonic distortion seen at the system output, as shown in Equation 5.17.

Figure 5.9 compares this harmonic distortion model to a simulated results, for an ideal comparator with third order self-oscillating loop. The loop is created with an ideal comparator and three repeated poles in feedback between the comparator output and the comparator's negative input, to ensure sufficient phase shift for the loop to oscillate. This result shows a good match at small input signal levels, but at higher input signal levels the model results begin to diverge from simulation results, due to additional switching energy being injected into the loop filter as a result of a large input signal amplitude – which causes the self-oscillating frequency to shift down in frequency towards the signal band, violating the approximation of the describing function analysis that the self-oscillating waveform is fully filtered out.

$$V_{out_{3\omega_{in}}} = \frac{B^3 V_{DD}}{32\,\pi\,A^3\left(1+\frac{V_{DD}}{2\,\pi\,A}H(s)\right)} \tag{5.17}$$

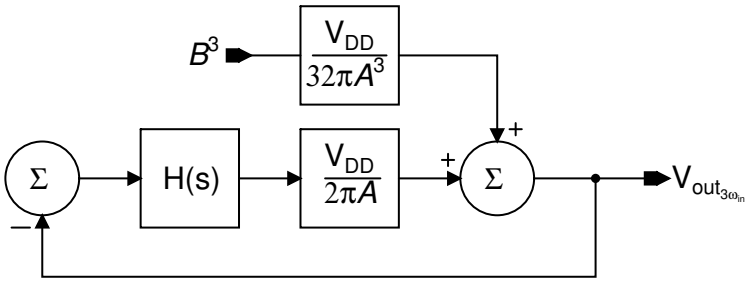

Figure 5.8: Structure used to calculate the amount of distortion that appears at the output, when the loop is in feedback.

5.3.3 Oscillation intermodulation

It is well known[55] that PWM systems produce Bessel-weighted intermodulation products between the PWM carrier frequency and the input frequency. Self-oscillating modulators produce similar intermodulation products between the self-oscillating fre-

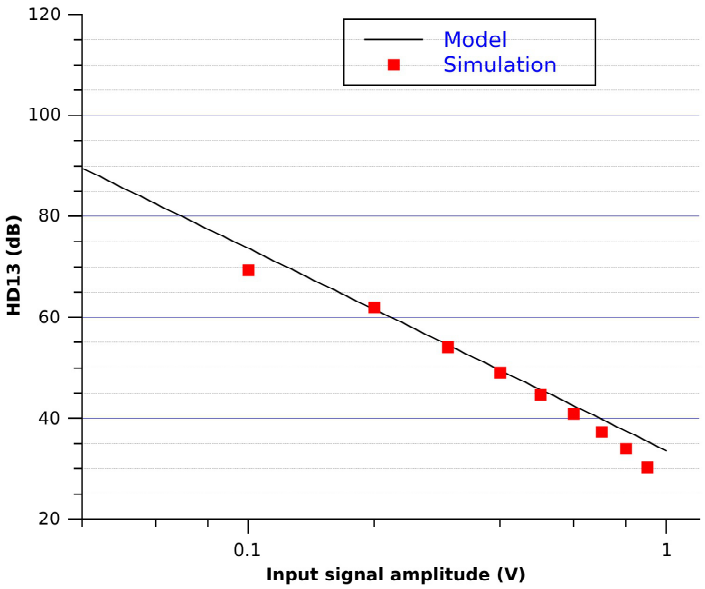

Figure 5.9: Performance of model described by Equation 5.17 versus simulation results, for a third order self-oscillating loop at 17MHz.

quency ω_{osc} and input signal frequency ω_{in} and an expression for them is given in [53]. It is repeated here (Equations 5.18–5.21) for convenience.

$$s_i(t) = \frac{\mathrm{V_{DD}}}{i\pi} \sum_{l=-\infty}^{\infty} \frac{1-(-1)^{i+l}}{2} B(i,l) \cos\left(\omega(i,l) + i\frac{\pi}{2}\right) \tag{5.18}$$

In this equation,

$$\omega\,(i,l) = i\,\omega_c + l\,\omega_{in} \tag{5.19}$$

$$B(i,l) = \sum_{p=-\infty}^{\infty} J_p\left(i\,\frac{\omega_{osc}B^2}{4\omega_{in}{\mathrm{V_{DD}}}^2}\right) J_{(l-2p)}\left(i\frac{B\pi}{2\mathrm{V_{DD}}}\right) \tag{5.20}$$

and

$$\omega_c = \left(1 - \frac{B^2}{2\,{\mathrm{V_{DD}}}^2}\right)\omega_{osc} \tag{5.21}$$

In the above, J_n is the Bessel function of the first kind, $\omega(i,l)$ computes the frequency of spectral component l in band i, and $B(i,l)$ represents the amplitude weighting factor of spectral component l in band i.

5.3.4 Distortion in practical DMT systems

The harmonic and intermodulation distortion mechanism of an ideal self-oscillating modulator with a single sine wave input are well understood from both intuitive and analytical points of view. However, the harmonic distortion analysis does not extend

directly to multi-carrier systems because the comparator is a non-linear element; with reference to Figure 5.6, superposition does not hold, as described in Equation 5.22 for a DMT system with W carriers.

$$(x_1(t) + x_2(t) + \ldots + x_W(t))\,\mathrm{NL} \neq x_1(t)\mathrm{NL} + x_2(t)\mathrm{NL} + \ldots + x_W(t)\mathrm{NL} \qquad (5.22)$$

Other describing functions for the ideal relay are known, such as one for a sinusoid plus random Gaussian-distributed signal[105], which would seem to be a good match for a self-oscillating system with Gaussian distributed input signal, although this has not been investigated here.

In wide band multi-carrier systems which aim to minimise the self-oscillation frequency – such as Class-D line drivers, for efficiency optimisation – the intermodulation distortion between the carrier frequency components and the input frequency components becomes more significant than harmonic distortion of the modulation process. Intermodulation distortion for a DMT signal is hard to analyse analytically as it will depend on many different carriers with randomly assigned phases, and so is entirely signal dependent. Further, the introduction of physical effects associated with real implementations – such as finite rise/fall times of the comparator output signal and $\mathrm{d}i/\mathrm{d}t$ voltage transients (discussed in Section 6.6.1) alter the energy in the intermodulation components, and this is also hard to analyse analytically.

As a result, the design of wide-band self-oscillating amplifiers must rely on system and circuit level modelling techniques, such as time domain simulation of idealised prototype architectures; the use of simplified circuit models in languages such as Verilog-A; and mixed-mode simulations of behavioural blocks with transistor levels implementations of critical components such as the output driver. These techniques will be presented next.

5.4 Circuit modelling

The lack of suitable analytical methods to quantify multi-tone performance in self-oscillating Class-D means numerical design approaches are required. The two main methods for doing this[111] are system simulation, such as Matlab or Simulink; and mixed-mode simulation, such as Cadence Virtuoso/Spectre which allow co-simulation of mathematical representations of blocks written in languages such as Verilog-A, with circuit-level implementations of other critical blocks. The former provides greater capabilities for exploring the design space of the system, particularly as it has powerful in-built methods for computing and manipulating filter responses, but the latter allows prototype transistor level implementations of critical blocks to be simulated with

mathematical models of the remaining loop components, early on in the design. Self-oscillating Class-D drivers are well-known for their sensitivity to design implementation, producing switching frequencies on silicon which do not match the expected design performance[36, 70], so during system modelling, it is necessary to include critical blocks at the transistor level. For wide-band self-oscillating Class-D, the implementation of the output driver and buffer chain significantly limits the maximum switching frequency of the loop, which in turn impacts the following:

- Inherent gain of the loop (Equation 5.2) and its tolerance to implementation imperfections
- Harmonic distortion of the loop via limit cycle attenuation provided by the loop filter (Equation 5.17),
- Level of intermodulation distortion (Equation 5.18),
- Power consumption (Figure 3.14)
- The practicality of design implementation (Section 6.6.1).

For these reasons, the Class-D driver must be included in the system model at transistor level from the start.

A Cadence Virtuoso implementation of the general self-oscillating Class-D loop shown in Figure 5.5 is thus a suitable starting point for the modelling. The loop filter is initially implemented as a Verilog-A s-domain transfer function, which can be parameterized with desired loop filter coefficients. As the design progresses towards a particular implementation, Verilog-A models can be created for each of the sub-blocks and non-idealities such as finite gain or bandwidth can be added to the sub-block models as required. Once the circuit implementations of the loop filter components are complete, their Verilog-A implementations can still be used to debug complete system performance issues. Further, once layout is completed, individual blocks can be extracted and verified on a block-by-block basis.

The comparator is initially implemented as two sub-blocks, a Verilog-A comparator model and a prototype transistor level buffer and driver, which can quickly be designed using the process in Section 6.5.1. This allows the buffer delay and output stage non-idealities to be accurately represented in numerical simulations from the start of the design process. Bondwire models are also included from the start, as are PCB parasitics, to ensure that design decisions made early on are not based on assumptions which turn out to be incorrect as the design progresses and more attention is paid to interfacing with external components.

The lumping of the comparator plus all output driver circuitry into one top-level block is specifically arranged, as it allows all the non-linear elements to be switched out and

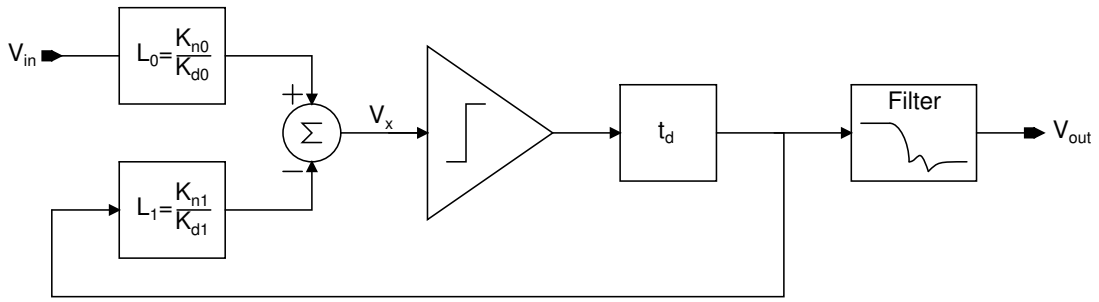

Figure 5.10: Matlab/Simulink time-domain model of the self-oscillating Class-D line driver.

replaced by a linear comparator model with an equivalent low frequency gain. This is useful for quickly estimating the frequency domain characteristics of the loop.

While this methodology is sufficient for designing a Class-D modulator, it is not well suited to quickly exploring loop filter architectures. For this, a Matlab/Simulink model has been created which has a main purpose of exploring different filter characteristics. For characteristics that are of interest, their coefficients are inserted into the Cadence Virtuoso loop filter model to gain a detailed understanding of the performance of that filter in a realistic loop. The method by which a characteristic is determined to be of interest or not will be described in Section 6.4.

5.5 Loop filter modelling

To explore the design space and derive the design of the loop filter, a Matlab/Simulink time domain model of the amplifier was created and is shown in Figure 5.10. This is similar to the general model shown earlier in Figure 5.5 but with two refinements:

- The loop filter H(s) has been split into two, a transfer function block L_0 in series with the input signal and a transfer function L_1 in series with the feedback signal. The two new transfer functions are placed before the summing junction. They are equivalent to H(s) if L_0=L_1. The transfer functions are defined in terms of numerator and denominator coefficients which for L_0 are denoted K_{n0} and K_{d0}, and for L_1 are denoted K_{n1} and K_{d1}. The variables $K_{n0/n1}$ and $K_{d0/d1}$ are vectors which store the polynomial coefficients of the numerator and denominator transfer functions.
- The comparator propagation delay and the delay involved in driving the large Class-D output stage are lumped into a delay block with delay t_d.

The input signal and comparator output signal are both assumed to vary between ±1V and the comparator is implemented as an ideal relay. This comparator implementation

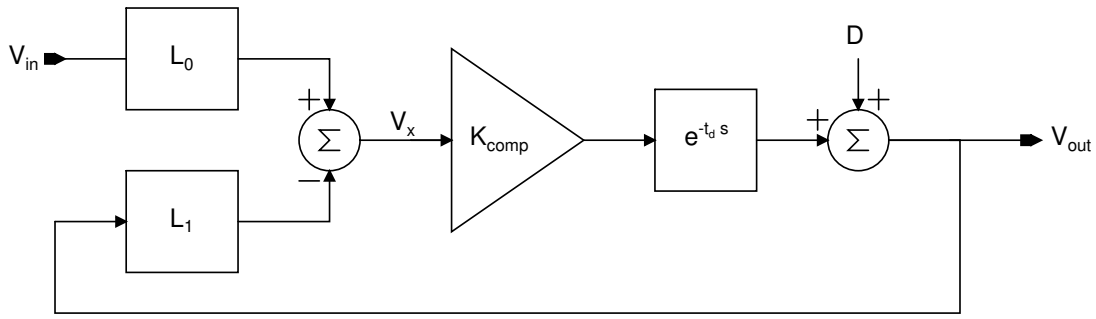

Figure 5.11: Low frequency linearized s-domain model of the self-oscillating Class-D line driver.

will be revisited and enhanced in Section 6.5.3.

For loop analysis, a low frequency linear model of the time domain model is used and is shown in Figure 5.11. This looks at the steady-state operation of the loop as an average over one period of the switching frequency. The comparator is replaced by a linear gain $\mathrm{K_{comp}}$[104] which is related to the first order term of the describing function gain in Equation 5.14. The describing function model of the comparator represents the comparator as a gain dependent on the signals in the system, but for first order circuit modelling, it is useful to represent the comparator gain in terms of the parameters in the model shown in Figure 5.11. This is despite the limitations discussed above about the accuracy of the describing function comparator model when used with DMT input signals; and so numerical verification is still required.

5.5.0.1 Comparator gain

The linearized comparator gain is determined by solving the loop gain equation:

$$|\mathrm{L_1\,K_{comp}}| = 1 \tag{5.23}$$

Note that the delay block t_d does not alter the magnitude of the signal. Assuming the loop gain has a first-order characteristic at the frequency of self-oscillation, then:

$$\mathrm{K_{comp}} = \left|\frac{1}{\mathrm{L_1}}\right| = \left|\frac{s}{\omega_0}\right| \tag{5.24}$$

This should be evaluated at the switching frequency $s = j2\pi\mathrm{f_{sw}}$, where $\mathrm{f_{sw}} = \frac{1}{4t_d}$ (from Equation 5.6), giving the following expression for $\mathrm{K_{comp}}$.

$$\mathrm{K_{comp}} = \frac{\pi}{2}\,\frac{1}{\mathrm{t_d}\,\omega_0} \tag{5.25}$$

Note an important property of this result; the comparator gain is inversely proportional to the loop filter unity gain frequency. This intuitively makes sense as the comparator only detects whether its input is above or below a threshold, it does not care about the scaling of its input signal.

5.5.1 Linearized loop analysis

From the linear model in Figure 5.11, the output V_{out} can be written as in Equation 5.27.

$$V_{out} = \frac{D}{1 + K_{comp} L_1} + \frac{V_{in} K_{comp} L_0}{1 + K_{comp} L_1} \tag{5.26}$$

$$= NTF \times D \; + \; STF \times V_{in} \tag{5.27}$$

Here, NTF and STF are the Noise and Signal Transfer Functions[52], respectively. Note that the overall loop gains are determined by transfer functions $L_{0/1}$ and comparator gain K_{comp}. It is useful to define two new variables, $L_{0/1}{}'$ in Equations 5.28 and 5.29 which give the comparator-scaled gains.

$$L_1{}' = K_{comp} L_1 \tag{5.28}$$

$$L_0{}' = K_{comp} L_0 \tag{5.29}$$

Now the NTF and STF can be written as in Equations 5.30 and 5.31.

$$NTF = \frac{1}{1 + L_1{}'} \tag{5.30}$$

$$STF = \frac{L_0{}'}{1 + L_1{}'} \tag{5.31}$$

$$= L_0{}' NTF \tag{5.32}$$

Finally, expressions for $L_0{}'$ and $L_1{}'$ can also obtained for a desired NTF and STF, as in Equations 5.33 and 5.34.

$$L_1{}' = \frac{1}{NTF} - 1 \tag{5.33}$$

$$L_0{}' = \frac{STF}{NTF} \tag{5.34}$$

Note that usually $L_0{}'$ and $L_1{}'$ share the same denominator, although their numerators can differ. This is because they are usually implemented in the same physical structure and the pole-defining components are common to both the $L_0{}'$ and $L_1{}'$ signal paths.

Listing 5.1: Computing zeros, poles and gain for a prototype NTF

```
order = 2; % order of the filter
rs = 10;  % minimum stopband ripple in dB
fc = 30e6; % stopband edge frequency in Hz

[zn,pn,kn] = cheby2(order, rs, fc, 'high', 's')
```

5.5.2 Loop design methodology

There are five parameters in the linear model of Figure 5.11; L_0, L_1, K_{comp}, t_d and distortion D. In high frequency loops, the lower limit of t_d is determined by the comparator and Class-D driver propagation delays, although t_d can be increased if required with a delay cell. However, the propagation delay is not considered as a main design variable. K_{comp} is a function of L_0, L_1 and t_d and distortion term D is determined by the choice of modulation scheme, switching frequency and driver implementation. Thus the two remaining variables, L_0 and L_1 are the principle design variables with which to define loop performance, once other higher level implementation decisions (injected power, supply voltage, switching frequency) are fixed.

The loop design methodology begins by choosing a desired NTF. This should have a high pass characteristic as the purpose of the NTF is to attenuate distortion generated by the modulator which is present within the signal band. A Matlab example of a method to do this is given in Listing 5.1 for a Chebyshev type II characteristic, but similar functions are available for other filter types.

Once an NTF is chosen, the feedback transfer function L_1 can be calculated using Equations 5.34 and 5.29.

Assuming the STF and NTF share the same poles, an un-scaled prototype of L_0 can be created as in Equation 5.35, where L_{1d} is the denominator of L_1.

$$L_{0_{unscaled}} = \frac{1}{L_{1d}} \tag{5.35}$$

The scaling factor T required to give a low frequency signal gain of 1 is given by evaluating Equation 5.36 at 1 Hz;

$$T = \frac{1 + L_1'}{K_{comp}\, L_{0_{unscaled}}} \tag{5.36}$$

The scaled L_0' is given by $T \times L_{0_{unscaled}}$.

The Matlab code used to implement the above steps is given in Listing 5.2. Note that

Listing 5.2: Determining loop filter transfer functions

```
function [Kn0, Kn1, Kd, NTF, STF, L1 ] = sopa_compute_coefficients(zn, pn,
    kn, Kcomp);
s = tf('s');
NTF = zpk(zn, pn, kn);
L1 = (1/Kcomp) * (1/NTF - 1);

[l1_num, den] = tfdata(L1);
Kn1 = cell2mat(l1_num);
Kd = cell2mat(den);

L0_den = tf(1, den);
unscaled_L0 = Kn1(end)*L0_den;
T = evalfr((1+Kcomp*L1)/(Kcomp*unscaled_L0), 2*pi*1);
L0 = T*unscaled_L0;

l0_num = tfdata(L0);
Kn0 = cell2mat(l0_num);

STF = Kcomp*L0 / (1+Kcomp*L1);
endfunction
```

the input parameters zn, pn and kn are the output parameters of Listing 5.1. The loop filter numerator and denominator coefficients K_{n0}, K_{n1} and K_d can be inserted into the Matlab/Simulink model in Figure 5.10 and the performance of that NTF can be characterised.

5.5.3 Loop filter synthesis

Once the loop filter transfer functions L_1 and L_0 have been decided, it must be mapped to a physical structure for circuit realisation. The systematic method of doing this will now be described.

A general second order loop filter structure which can implement any input and feedback transfer function pair L_0 and L_1, as defined in Figure 5.11, is shown in Figure 5.12. Other loop filter orders can be determined by analogy. Using superposition, the L_1 transfer function can be calculated while V_{in} is set to zero, as shown in Equation 5.37, and vice-versa for the L_0 transfer function, as in Equation 5.38.

$$L_1 = \frac{a_3\, s^2 + a_2\, s + a_1}{s^2 + g_2\, s + g_1} \tag{5.37}$$

$$L_0 = \frac{b_3\, s^2 + b_2\, s + b_1}{s^2 + g_2\, s + g_1} \tag{5.38}$$

It is observed that the integrators plus feedback paths consisting of g_1 and g_2 coefficients

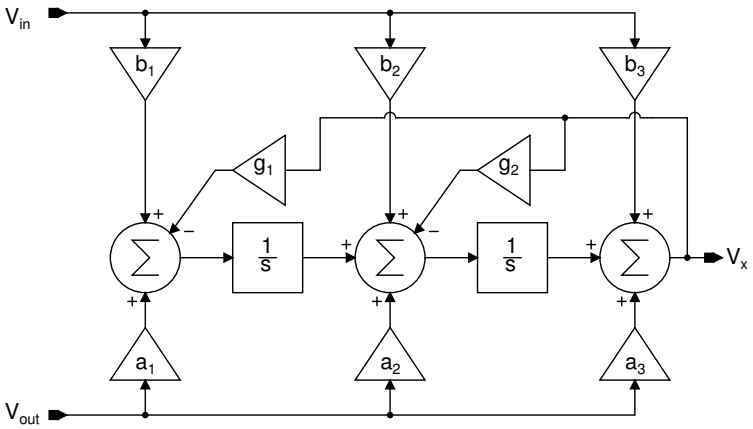

Figure 5.12: Structure of a general purpose loop filter which can implement any L_0 and L_1.

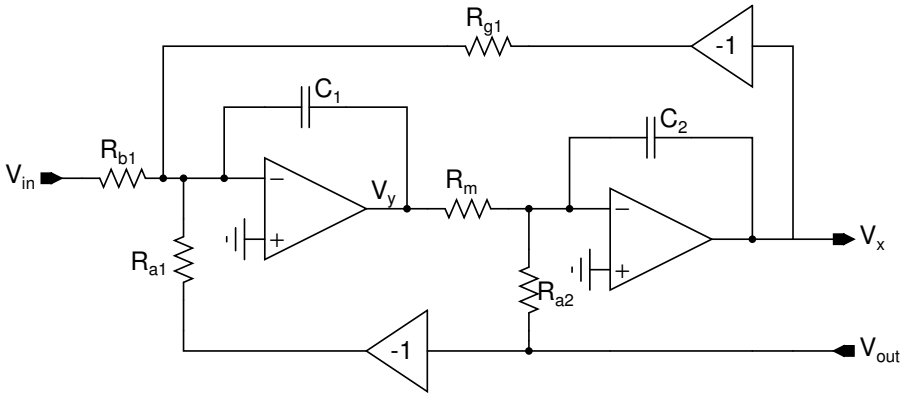

Figure 5.13: Prototype circuit structure to implement the structure shown in Figure 5.12.

implement the denominators of both L_1 and L_0 transfer functions. The numerators of L_1 and L_0 are defined by the integrators and either the a_n or b_n forward paths.

5.5.4 Circuit structure

While there are a wide variety of circuits which can implement a desired structure, such as the example shown in Figure 5.12, a simple and straight forward implementation has been chosen to illustrate the method.

With reference to the general transfer functions shown in Equations 5.37 and 5.38, it will be assumed that in the desired transfer function $b_2 = b_3 = g_2 = 0$. The corresponding elements can be removed from the diagram. Now by considering the summing junctions in Figure 5.12 as current summing nodes, an initial circuit realization can be developed, as shown in Figure 5.13, and analyzed to give circuit output Equation 5.39.

Listing 5.3: Calculation of circuit component values

```
function [ Ra1, Rm, C1, C2, Ra2, Rg, Rb ] = sopa_compute_2nd_order_RCs(Kn0,
    Kn1, Kd);

a1 = Kn1(3);
a2 = Kn1(2);
b1 = Kn0(3);
g = Kd(3);

Ra1 = 25e3;
Rm = 25e3;
C1 = 300e-15;

C2 = 1/(a1*C1*Ra1*Rm);
Ra2 = 1/(C2*a2);
Rg = 1/(g*C1*C2*Rm);
Rb = 1/(b1*C1*C2*Rm);
```

$$V_x = \frac{\left(\frac{1}{R_{b1}C_1C_2R_m}\right)V_{in}}{s^2 + \frac{1}{C_1C_2R_{g1}R_m}} - \frac{\left(\frac{s}{C_2R_{a2}} + \frac{1}{R_{a1}C_1C_2R_m}\right)V_{out}}{s^2 + \frac{1}{C_1C_2R_{g1}R_m}} \tag{5.39}$$

By comparing the coefficients of Equation 5.39 to Equations 5.37 and 5.38, circuit component equations can be obtained. As there are seven components in the circuit schematic (Figure 5.13) which map to five coefficients (Figure 5.12), there are multiple solutions to the circuit equations, which gives some degree of freedom. Resistors R_{a1}, R_m and C_1 were chosen as fixed variables, as they determine the noise and current consumption of the system, and the remaining component values are computed. A Matlab program listing to do this is shown in Listing 5.3.

5.5.5 Coefficient scaling

Until now, the voltage and current swing limits of practical systems have not been discussed. With a circuit realization such as Figure 5.13, it is expected that practical op-amps would have an output swing range which falls within their supply rails, but the loop filter design methodology so far has not accounted for this. The swings at integrator outputs V_x and V_y will be a function of V_{in}, V_{out} and the component values, and it may be greater than what the practical integrator can achieve.

Coefficient scaling can be used. If the swing at node V_y in Figure 5.13 is larger than the supply rails by a factor k, it can be brought within the supply rail range by increasing C1 by a factor k and, to compensate for the effect this would have on the current flowing

through R_m, R_m can also be reduced by a factor k. The overall loop transfer function has not changed, but the swing at the output of the first integrator has been reduced. A similar procedure can be followed to adjust the swing at the output of the second integrator, at node V_x, by altering components C_2, R_{g1} and R_{a2}. Note that node V_x also drives a comparator and so this would see a reduced swing, but the comparator is insensitive to the scaling of its input signal; only the sign matters. This does increase the sensitivity of the design to comparator offset and noise, but there are still a number of high gain integrator stages preceding the comparator and so this effect is usually negligible.

Note that the integrator output must be prevented from clipping because it feeds back via the g_1/g_2 coefficients to other nodes in the loop filter and any clipping at this point will inject additional error into the loop. However, large swings which would saturate the supply may not be a problem for the comparator itself depending on the comparator implementation, as the comparator only needs accurate detection of the crossing point of its input signals and provided that it can recover from any saturation of its inputs sufficiently quickly, its inputs can be allowed to saturate. One technique that can then be used here is to insert a preamplifier between the loop filter output and the comparator input to scale the loop filter output signal back up, reducing sensitivity of the system to comparator noise and offset, then using a comparator which is tolerant to input signal saturation.

Coefficient scaling is usually performed using numerical simulations of a chosen amplifier; this is the approach used here, and it fits in well with the circuit modelling strategy discussed in Section 5.4.

5.6 Conclusion

There are three main Class-D architectures; Sigma-Delta, PWM and self-oscillating. With reasoned discussions, self-oscillating architectures have been identified as being the most suitable for wide-band Class-D line drivers. The main published self-oscillator architectures have been reviewed with the conclusion that at high frequency, they converge into a single phase-delay architecture, and mechanisms and equations which define the frequency of oscillation in these loops have been presented. The fundamental distortion mechanisms in self-oscillating loops have been discussed from intuitive and analytical points of view but limitations of the published analyses in predicting the distortion components, in the presence of a multicarrier input signal, has been identified. The resulting numerically based design methodology has been discussed in detail and the systematic method of moving from a high level design conceptual implementation

to a circuit-block level implementation has been presented. There is now sufficient information and methodology to carry out the design of a Class-D line driver.

Chapter 6

Circuit Implementation

6.1 Introduction

The design and implementation of a self-oscillating Class-D line driver targeting the HomePlug AV standard will be presented in this chapter. In order to prove the applicability to modern fine-scale technology nodes from 40 nm and below, a cost effective 130 nm digital CMOS process from UMC has been chosen for the implementation, as it includes features common to lower geometry processes such as high g_m, low V_T, 1.2V devices and also lower g_m, higher V_T, 3.3V devices; deep N well regions; and metal-metal finger capacitors.

The design methodology, theory and techniques presented in Chapter 5 will be used throughout this chapter.

This chapter will start by defining the high level specifications that the line driver should aim for. Then the main system level parameters – oscillation frequency and loop filter coefficients – will be determined, and the transistor level design process and outcome for each of the circuit blocks in the system will be described. Chip fabrication, bonding and related design issues will be detailed and then finally, the test and measurement setup will be described.

6.2 System Specifications

System specifications for bandwidth and injected power are constrained by the relevant EMC standards, as described in Section 2.2.2. These place an upper limit on the

Table 6.1: Line driver specifications

Parameter	Value
Minimum signal frequency	2 MHz
Maximum signal frequency	28MHz
Injected power	<56mW
Line impedance	100Ω
MTPR	30dB

injected power per carrier of -50dBm/Hz quasi-peak (or -56dBm/Hz average), and on the maximum signal transmission band of approximately 2–28MHz. Assuming a flat distribution of power across the carriers in a 26 MHz bandwidth, and allowing for 4MHz of notches, this corresponds to a maximum injected power of 56 mW when using the nominal line impedance of 100 Ω.

A further constraint imposed by this EMC limit is on the distortion and noise of the line driver. With reference to the EMC graph shown in Figure 2.3, the power in the notches, where no signal is transmitted, must be less than -80 dBm/Hz quasi-peak, whereas the signal power can be -50dBm/Hz quasi-peak. The difference between the two numbers determines the minimum MTPR of the line driver, which is 30dB.

These specifications are summarised in Table 6.1

While system specifications are mandatory, they provide room for flexibility. A particular design will have trade-offs in terms of its linearity, injected power, efficiency, area, robustness and design complexity, among other criteria and it may, for example, be beneficial to reduce the injected power that a design targets if that allows integration in a lower voltage, cheaper process. It is therefore useful to have design goals; aspects of the design to target for improvement. In this design, the primary design goal is improving efficiency, subject to meeting other design specifications, and this will guide many of the architectural design trade-offs.

6.3 Application design

Before examining the internal architecture and circuit level details of the line driver, the application environment for the line driver should be reviewed. From this, initial design decisions are made concerning the specific application mentioned here - self-oscillating

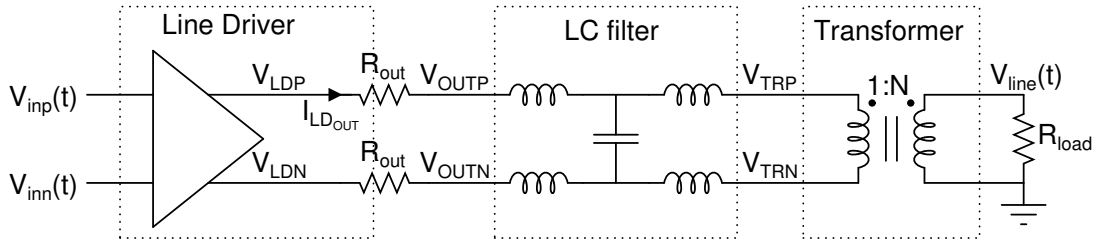

Figure 6.1: Powerline transmit path showing relevant system components. R_{out} is the line driver output resistance. Also shown is an output LC filter and a transformer with 1:N ratio which couples the line driver output signal onto the powerline. R_{load} represents the powerline impedance and is shown between a node $V_{line}(t)$ and ground. This model simplifies analysis although in practice, $V_{line}(t)$ and ground would be replaced by a pair of powerline cables.

Class-D, in a low voltage process, with high injected power requirements.

The system level circuit shown in Figure 2.6 has been redrawn in Figure 6.1 with an increased focus on relevant sections of the transmit path. The line driver is shown with a differential input, differential output configuration. A differential input is a reasonable assumption for applications involving a highly integrated AFE, as there will be many other frequencies present in the system which could couple in to the line driver through the routing of the input signal. Using a differential input stage and matched differential input routing means that any interferers should couple to both inputs equally and so will be rejected by the differential line driver.

The line driver differential output can also be justified. If the line driver outputs $V_{OUTP/N}$ swing between 0V and V_{DD}, then for a symmetrical signal a single ended output stage can drive a maximum power of:

$$P_{max\_se} = \frac{(0.5\,V_{DD})^2}{R_{load}} \tag{6.1}$$

A differential output stage which can swing differentially between $\pm V_{DD}$ can drive a maximum power which is four times that of a single ended line driver with the same supply voltage, as in Equation 6.2. For an application targeting high injected power, a differential output is a sensible choice.

$$P_{max\_diff} = \frac{{V_{DD}}^2}{R_{load}} = 4\,P_{max\_se} \tag{6.2}$$

Now that the structure is known, the voltage swing at the load can be calculated. To inject 56mW into a typical powerline impedance of 100Ω, the peak-peak signal swing on the powerline network is:

$$V_{line_{pp}} = 2\,CF\,\sqrt{56mW\,R_{load}} = 18.9V \tag{6.3}$$

Table 6.2: Required line driver supply and internal swings for a range of transformer ratios, at 56mW injected power.

N	Transformer loss (dB)	V_{TRP} and V_{TRN} (V peak-peak)	Filter loss (dB)	V_{OUTP} and V_{OUTN} (V peak-peak)	R_{out} (Ω)	V_{LDP} and V_{LDN} (V peak-peak)	I_{LDout} (mA peak)
1	0.5	10.1	1	11.3	0.2	11.3	95
2	0.6	5.1	1	5.7	0.2	5.8	189
3	0.8	3.5	1	3.9	0.2	4.0	284
4	1	2.7	1	3.0	0.2	3.2	378

Considering the components in Figure 6.1 – R_{out}, the LC filter and the transformer – as a chain of voltage dividers, the voltage swing at each node can be calculated starting from the load and working towards the line driver, ultimately determining a minimum supply voltage for the line driver. Practical LC filter and transformers exhibit some signal transmission loss and this must be factored in. Estimated values for these losses have been proposed, based on values from datasheets of commercially available parts[112] and from measurements.

These calculations depend on R_{out} and the transformer ratio N, and are constrained by a number of factors:

- The maximum supply voltage in the UMC 0.13μm process of 3.3V.
- Transformer loss increases with N, so N should be minimized.
- Line driver output current increases with N. High currents are particularly problematic for Class-D drivers due to the fast switching edges, as described in Section 6.6.1, and so this should be minimized.
- Output stage losses depend on device size and as in Figure 3.11, losses associated with device capacitance are significant at the target injected power. There is a tradeoff with R_{on} losses here as assuming a minimum length transistor is used, the only way to reduce capacitance is to reduce transistor width – which increases R_{on} losses.

A spreadsheet similar to Table 6.2 allows rapid exploration of the circuit parameters, where the voltages and currents on this spreadsheet are those that are shown in Figure 6.1. Initially, R_{out} is set to 0 and the minimum N, which results in a swing $V_{LDP/N}$ which is less than the 3.3V limit, is determined. R_{out} is then increased to the largest value that can be accommodated with a 3.3V supply, with some margin. The transformer losses are estimated based on measurements and datasheets of available Coilcraft PWB and TTWB parts.

The chosen circuit parameters are thus N=4 and R_{out}=0.2. Using this information, a suitable output driver can now developed as described in Section 6.5.1, however a number of system level design issues must be discussed first.

6.4 System design

The basic configuration of the line driver has been established from application level design (Section 6.3), and now the high level system design issues should be addressed. There are two main aspects; the self-oscillating frequency; and the loop filter transfer function.

6.4.1 Self-oscillating frequency

The choice of self-oscillating frequency is determined by many factors, as discussed in Section 5.4. Higher frequencies may improve the modulator's fundamental linearity but they increase the power dissipation in the Class-D output stage and place more demanding specifications, such as edge transition time, on the output driver.

Instead, the problem was reversed, first identifying what self-oscillating frequency was achievable, and then determining with numerical simulations what performance could be achieved with a variety of loop filter architectures, at that self-oscillating frequency. This requires an output driver to be implemented at transistor level (Section 6.5.1) and a suitable test bench which accurately models relevant parasitics (Section 5.4) to be constructed. From pre-layout simulations, the delay of the buffer was measured at 1.9 ns, and to account for the propagation delay of the comparator block itself, an additional estimated 0.2 ns was added to this time. Using Equation 5.12, this limits the oscillation frequency to 119 MHz, assuming an ideal first order loop filter. Adding some margin, a target frequency of 100MHz has been chosen as the basis for in-depth loop filter design exploration.

6.4.2 Loop filter

Loop filter design begins by choosing a desired NTF, then computing the L_0 and L_1 filters which implement this NTF, as discussed in Section 5.5, and finally examining the effect of the filter performance on oscillation frequency and modulator linearity using small signal and numerical analyses.

There are a variety of filter structures that are commonly used as prototypes for the NTF,

Table 6.3: Characteristics of major filter types.

	Butterworth	Chebyshev type 1	Chebyshev type 2	Bessel	Elliptic
Roll-off	Slow	Fast	Very fast	Very slow	Fastest
Ripple	No	Yes (in pass band)	Yes (in stop band)	No	Yes (pass band and stop band)
Group delay	Quite linear	Ripple (in pass band)	Ripple (in stop band)	Flat in band	Ripple (pass band and stop band)
Component sensitivity	Small	Medium	Medium	Small	Large

and their main characteristics are shown in Table 6.3. The high-pass form of the filter is used as it is desirable to attenuate distortion and noise which are present at low frequency in the signal band, which is the stop band of the filter. For the Class-D self-oscillating amplifier, faster roll-off corresponds to greater in-band (stop-band) attenuation of noise and distortion, so this should be maximised. Ripple is tolerated in both the filter pass and stop bands of the NTF, and allowing ripple in the stop band can improve the rate of stop band roll off, around the cut-off frequency of the filter. Group delay is not important in this application as it will be calibrated out by the channel estimation algorithm referred to in Section 2.3. Finally, component sensitivity is somewhat of a concern in terms of achieving reliable performance across process variation. While in a commercial application, this problem can be significantly reduced as a concern by using a process/voltage/temperature measurement circuit and an algorithm to trim component values between transmissions, this capability will not be implemented here.

To give some direction for the loop filter characteristic required, numerical simulations of the system with a simple 1/s loop filter are useful. Figure 6.2 shows the spectrum envelope of the intermodulation tones around the limit cycle frequency. These tones determine the noise floor within the DMT signal band, particularly in the upper half of the signal band. As the intermodulation tones decrease in amplitude as they approach DC, less loop gain is needed in the lower frequency sections of the signal band than in the higher frequency sections.

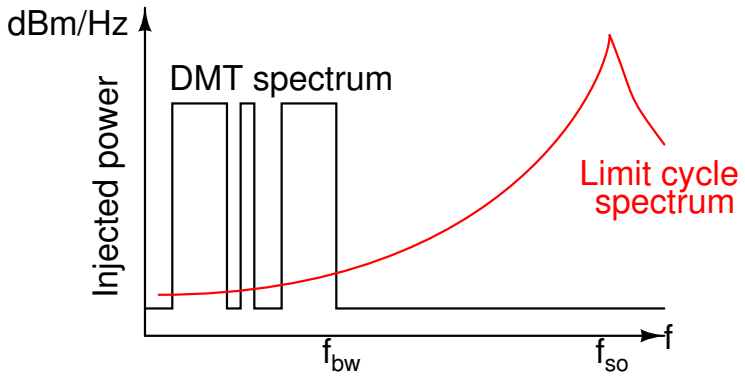

Figure 6.2: Bessel weighted intermodulation tones resulting from a DMT input signal.

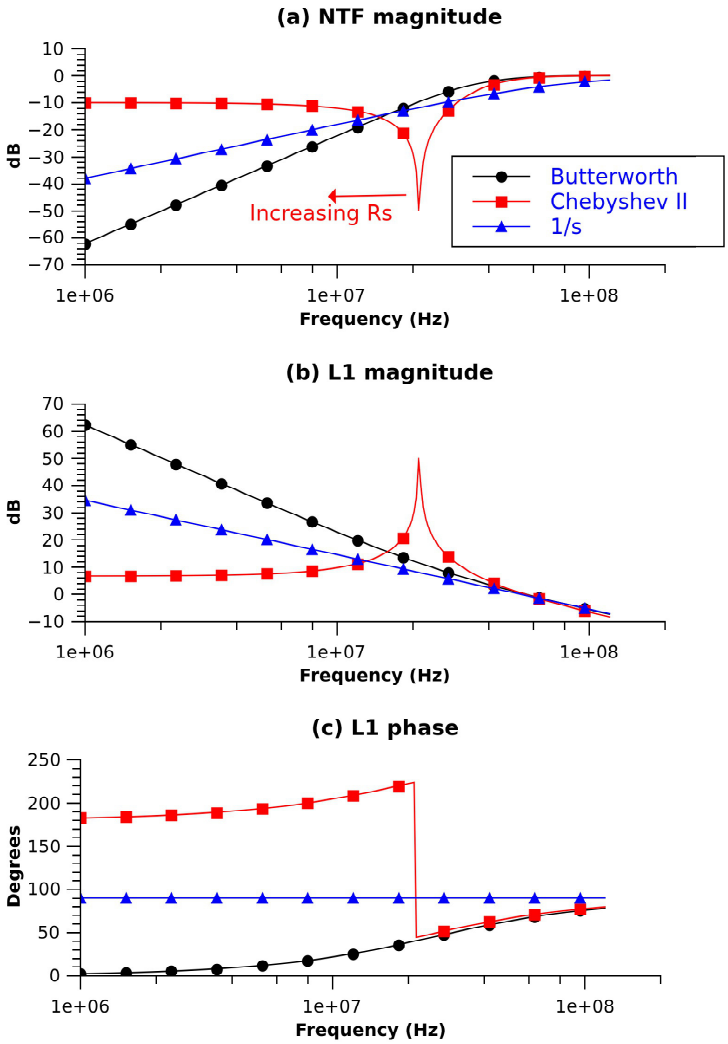

Figure 6.3: Comparison of the two main types of second order noise transfer function investigated, Chebyshev Type II and Butterworth, compared with a simple integrator. Variable R_s represents the stopband ripple.

The loop filter will be implemented using active components and so the filter order must be minimized as for an active integrator, each additional order adds at least one additional non-dominant pole due to the active circuitry. As discussed in Section 5.3.1, the oscillation frequency of a phase/delay self-oscillating loop is reduced due to the accumulated phase shift resulting from all of the non-dominant poles in the loop. To achieve a high self-oscillation frequency, the number of non-dominant poles (and so integrator stages) should be minimized, and the remaining non-dominant poles should be pushed to high frequency – although this costs current consumption.

The simplest loop filter is a first order integrator and the next simplest are the second order filters. These are used as the starting point for investigating a suitable loop filter. The first order integrator has no degrees of freedom although it can be scaled. However, for second order loop filters, the relative positions of the poles and zero can be altered

to create transfer functions with different properties. Two filter topologies can be taken as representing the main types of second order filter; Butterworth, representing flat response, slow roll-off filters and Chebyshev type 2, representing filters with stop band ripple and fast roll off. The NTF and L_1 magnitude and phase plots for second order Butterworth and Chebyshev type 2 responses are shown in Figure 6.3, along with the responses for a simple first order $\frac{\omega 0}{s}$ integrator.

All responses have been normalized for a 55 MHz unity gain frequency as in Figure 6.3(b), but as per Equation 5.25, this is an arbitrary choice; the important parameter is how much gain the filter can achieve relative to its unity-gain frequency.

The Butterworth filter is not a sensible choice - it only outperforms the simpler 1/s filter at low frequencies but from Figure 6.2, it is desirable to have high NTF attenuation at high frequencies.

The Chebyshev type 2 provides very low gain at low frequency, due to the low value of the Chebyshev stop band ripple parameter R_s. However, at low frequencies the MTPR will be determined by the harmonic distortion level, and this is low enough to easily meet the 30dB MTPR specification. At higher frequencies where intermodulation distortion becomes a problem, the Chebyshev type 2 provides more stop band attenuation. Note that the stop band ripple parameter R_s sets the near-DC attenuation of the NTF and also the position of the NTF zero. Increasing R_s shifts the zero to lower frequencies, increasing the NTF attenuation at low frequencies but reducing the attenuation in the upper half of the band.

Based on this above discussion and on numerical investigation of the different filter types, a high-pass Chebyshev type 2 filter was chosen with R_s=10 dB as the NTF. Based on simulations of the model in Section 5.4, this can achieve a MTPR (pc50) of 40dB.

While the discussion above focuses on the standard Butterworth and Chebyshev NTF's, the properties of these filters – maximally flat magnitude and minimized error between idealized and actual filter characteristic, respectively – may not be optimum for this application and perhaps some other arrangement of poles and zeros would be appropriate. To investigate this, a monte-carlo analysis was performed on the chosen Chebyshev type 2 NTF. A prototype second order loop filter was creating using the procedure in Listings 5.2 and 5.3 and then the real/imaginary parts of the poles and zero were independently varied by $\pm 50\%$ at 3σ around their prototype values. The resulting filters were normalized to have a 55MHz unity gain frequency and then key parameter were measured: inband gain, gain at 30MHz and phase shift at the estimated oscillation frequency of 100MHz. These results were analyzed but the performance of the varied NTFs was not significantly different than the performance of the prototype Chebyshev

NTF. While some monte-carlo iterations may improve loop filter phase shift performance, they degrade NTF attenuation at 30MHz, for example.

With an NTF now defined, the loop filter L_1 can be computed using Equation 5.34, as in Equation 6.4.

$$L_1 = \frac{A_0\ (s + z1)}{s^2 + p1} \tag{6.4}$$

Using Listings 5.1 and 5.2, values for the parameters are: $A_0 = 1.84e8$, $z1 = 1.39e8$ and $p1 = 1.78e16$. This filter has a single zero on the real axis and a pair of complex conjugate poles on the imaginary axis. The complex conjugate poles become the NTF zero at frequency $\sqrt{p1}/(2\pi)$. One final modification made to this filter was to reduce the high frequency phase shift by inserting an additional zero as otherwise the loop filter phase shift can begin to impact upon the oscillation frequency. This is particularly a concern after the integrator circuit implementation when additional high frequency non-dominant poles will be present in the L_1 transfer function. With the additional zero, the L_1 transfer function becomes:

$$L_1 = \frac{A_0\ (s + z1)\ (s + z2)}{s^2 + p1} \tag{6.5}$$

Filter parameters are $A_0 = 0.15$, $z_1 = 1.39e8$, $z_2 = 1.26e9$ and $p1 = 1.78e16$. The effect of the zero on the NTF is negligible within the signal band and only contributes to a marginal increase in noise at higher frequencies, but these frequencies will be removed by the external LC filter. There is a significant phase improvement at high frequency from the L_1 filter, as expected. The magnitude and phase plots of L_1 and the NTF are shown in Figure 6.4, both with the additional zero and without the additional zero.

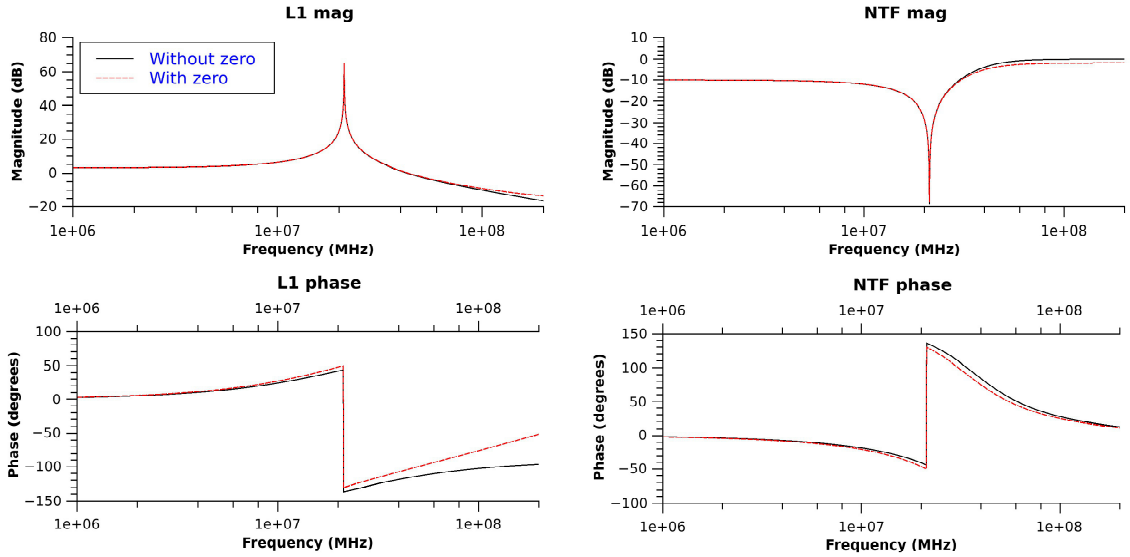

Figure 6.4: Magnitude/phase plots of the chosen L_1 and NTF, with and without the additional zero for phase shift improvement.

6.5 Circuit design

The system level design of the circuit has now been completed. Using the methodology described in Sections 5.5.2 – 5.5.5, a loop filter structure can be synthesized from the chosen L_1 transfer function as described in Section 6.4.2. Design of the circuit blocks can now proceed. To give an overall perspective of the following sections, a full-system diagram is shown in Figure 6.5. Each of the major sub-blocks – Loop filter, Comparator, Non-overlap generator and Output driver – will be covered below.

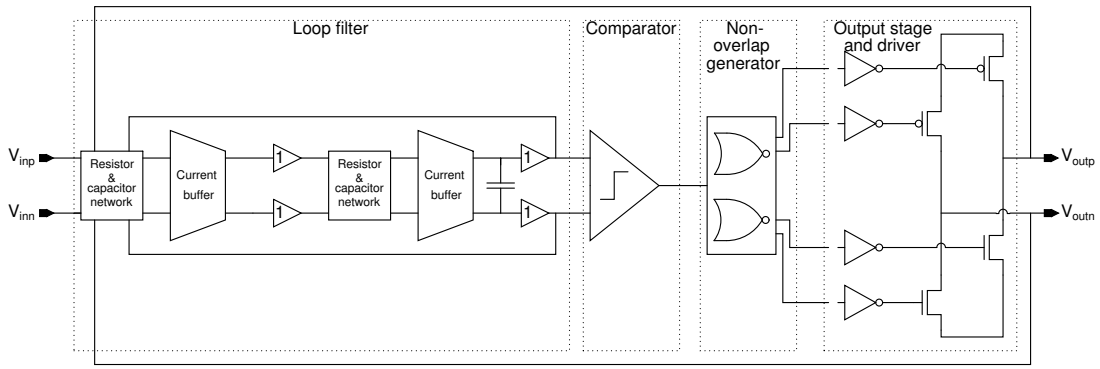

Figure 6.5: Top-level block diagram for the implemented Class-D line driver.

6.5.1 Output stage and driver

Once R_{out} is determined during the Application design phase, the output stage can be designed. Using minimum length devices and the $\mu_n C_{ox}$ parameters for PMOS/NMOS devices in the UMC 0.13μm process operating in the linear region, the required transistor widths for a P/N totem pole can be determined using MOSFET Equation 6.6, which is valid for low drain-source voltage. Transistor length L has been chosen as minimum width to minimise device area and reduce gate charging losses. The final sizes are shown in Table 6.4.

$$W \approx \frac{L}{R_{on}\, KP\, (V_{gs} - V_t)} \tag{6.6}$$

Table 6.4: P/N totem pole device sizes.

	PMOS	NMOS
width (μm)	18432	6144
length (μm)	0.34	0.34

The large output drivers have separate gate controls for PMOS and NMOS output devices to allow the implementation of a circuit to control shoot-through current. They need to be driven from unit inverters at the output of the analogue control circuitry and a tapered buffer consisting of a chain of scaled inverters will be used to do this. A scaling factor between inverter stages which optimizes the power × delay product of the buffer chain is derived in [113] as $e^1 \approx 2.72$. This has been approximately confirmed with simulations of buffer chains – each with the same unit input inverter and the same load capacitance at the end of the chain – in the UMC 0.13μm process as shown in Figure 6.6. Note that this means that for different scaling factors, the number of stages in the buffer chain changes too. The power and delay values are approximately flat for scaling factors between 2.5 – 4.5 and so a scaling factor of 4 was chosen as this simplifies the physical implementation/layout of the transistors. With this scaling factor and the output device sizes from Table 6.4, the full output stage and driver can be designed and is shown in Figure 6.7.

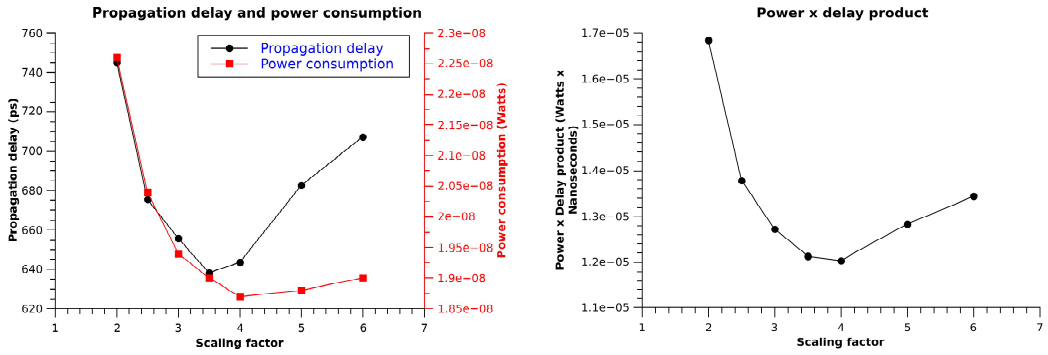

Figure 6.6: Power consumption and delay simulation results from tapered buffers with a range of buffer scaling factors.

To simplify the layout task, the driver is broken into four basic types of cell, a unit inverter N_UNIT, larger inverters BIG_BUFF_P and BIG_BUFF_N and a unit of output devices DRIVER. All instances of each type are the same size. These types are arrayed up as indicated by the repetition factor at the bottom right of each block. For example, there are 16 DRIVER cells inside a BUFF_DRIVER cell, then 24 BUFF_DRIVER cells are placed to make the full driver. All width and length dimensions shown are in μm, all NMOS source terminals connect to ground and all PMOS source terminals connect to the 3.3V supply. One N_UNIT labelled "DUMMY" is used to match the loads seen by the first stage N_UNIT buffers for the differently sized buffer chains in the PDRV and NDRV path.

A highly repetitive layout structure is used which allows for matched routing from the PDRV and NDRV inputs, to all of the PMOS and NMOS output devices. The completed layout is shown in Figure 6.8.

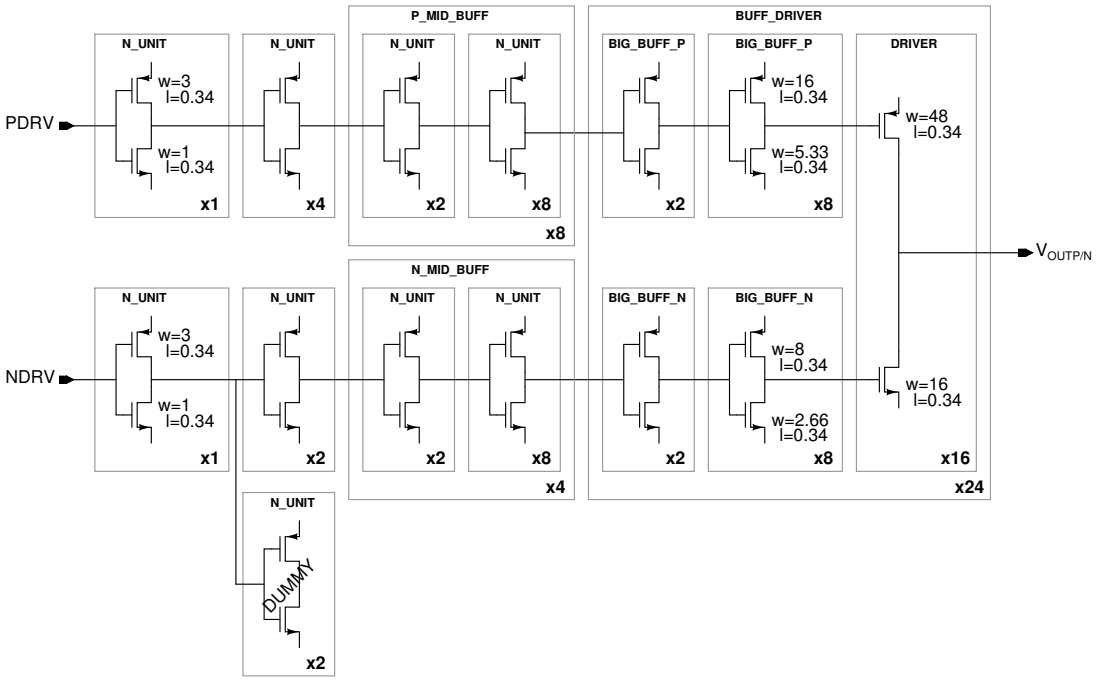

Figure 6.7: Output driver and buffer schematic for one half of the H-bridge.

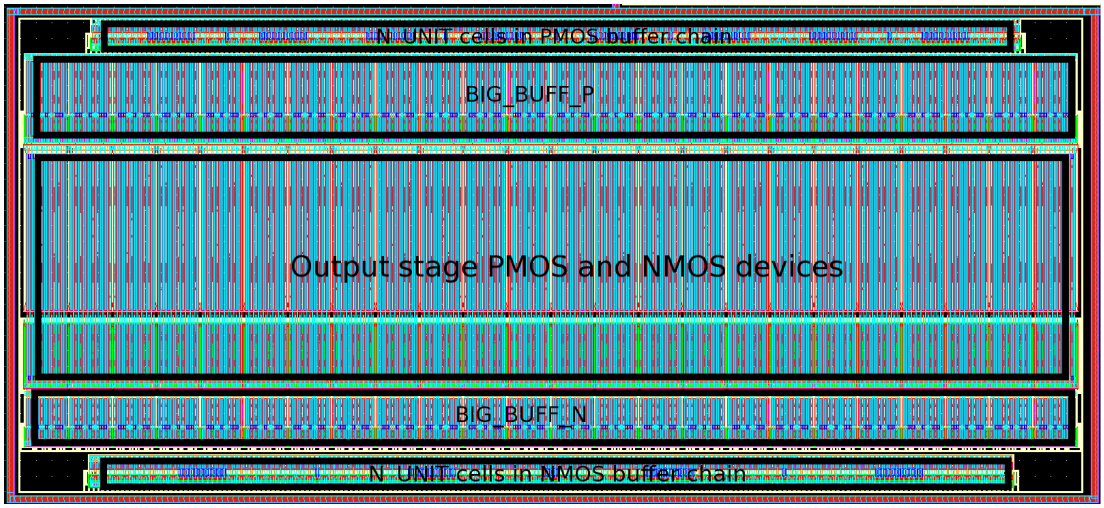

Figure 6.8: Output driver and buffer layout plot for one half of the H-bridge. The main sections of the layout are highlighted and labelled.

To help maintain a stable supply for the buffer chain, each cell in the tapered buffering network includes MOS capacitor decoupling with area comparable to that of the buffer itself. The output stage supply is also decoupled to the output stage ground connection – unused area was filled with ≈1 nF of decoupling capacitance. This capacitance helps reduce the voltage overshoot due to the $\mathrm{d}i/\mathrm{d}t$ current during output stage transitions, as will be discussed in more detail in Section 6.6.1.

Using post-layout extractions of the output stage and tapered buffer, which included both parasitic resistance and parasitic capacitance, the delay through the buffer was

simulated and found to be 1.4ns. The post-layout extractions also highlighted an issue in layout; an additional 0.4Ω of routing resistance was found in the output driver layout and due to time constraints, this could not be improved.

6.5.2 Non-overlapping gate control and loop delay

The non-overlap circuit creates non-overlapping gate drive signals for the tapered buffer, based on the comparator output COMP and on the inverse of the comparator output, COMPB. It is required in order to prevent both PMOS and NMOS output devices turning on at the same time. There are two non-overlapping circuits in the design, one for each H-bridge, where the inputs of the two are swapped. The non-overlap schematic is shown

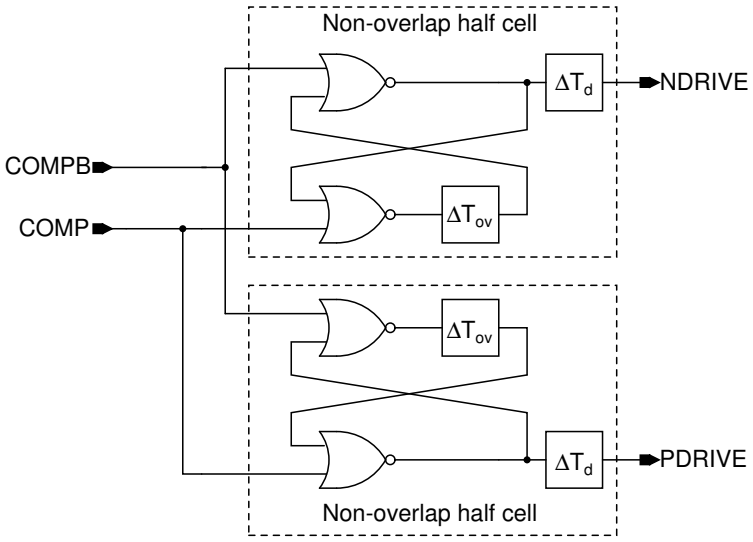

Figure 6.9: Non-overlap clock generator circuit and delay control.

in Figure 6.9 and is made from two half cells. Each half cell is similar to the conventional non-overlap circuit[114], except that the non-overlap delay ΔT_{ov} is only inserted in series with one of the NOR gate outputs rather than in both. Assuming the NOR gate and inverter have zero delay, the conventional non-overlap circuit has a minimum propagation delay of ΔT_{ov}, while the presented circuit has a minimum propagation delay of zero. This is advantageous in high-frequency self-oscillating amplifiers, where the gate driver propagation delay is an important performance determinant. Additionally, it allows ΔT_{ov} to be chosen without impacting the gate driver propagation delay.

The switching frequency of the phase-delay self-oscillating loop is strongly influenced by parasitic effects such as non-dominant comparator and loop filter poles, and by parasitic capacitance and resistance affecting propagation time through the gate drive circuitry. It is necessary to have some external method of controlling the switching frequency otherwise it is hard to guarantee a desired level of performance once the circuit has

been fabricated. Programmable delay cells have been implemented and are shown as ΔT_d in Figure 6.9, are used to insert a delay into the NDRIVE and PDRIVE signal paths. These are identical to the delay cells used to define the non-overlap time.

In a real application, the self-oscillating frequency could be measured at start-up and appropriate adjustment made to ΔT_d until the desired self-oscillating frequency is obtained, as is commonly done in Phase Locked Loops[115, 116]. However, for this design, circuitry was not implemented to automatically calibrate the delay. With fabricated silicon, the frequency can be manually trimmed by connecting the amplifier inputs to common mode, observing the oscillation frequency with an oscilloscope, and adjusting the delay cell trim setting appropriately. For simulation of this design, a Verilog-A module has been written to automatically calibrate the value of ΔT_d whenever a "stabilize" control signal is high. Calibration is performed when the inputs have been shorted to common-mode, so that the self-oscillating frequency is not affected by input signal variations, as described by Equation 5.9. The module listing is shown in Appendix A.

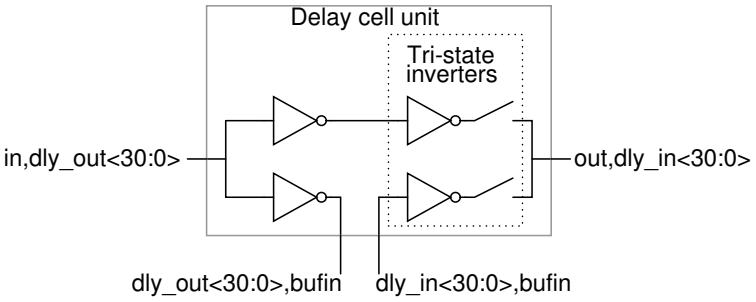

Figure 6.10: Programmable delay cell.

Finally, the delay cell itself is shown in Figure 6.10. It uses a delay unit cell which provides two paths, a fast path (top) and a slow path (bottom) and then nests multiple instances of these cells. The output inverters in the delay cell are tri-stateable and so either the fast or slow path can be chosen at each level of hierarchy.

6.5.3 Comparator

Specifications for the comparator were derived using the Matlab system model described in Section 5.5. The comparator circuit is modelled as in Figure 6.11, which results in the transfer function given in Equation 6.7

$$\frac{V_{out}}{V_{in}} = \frac{g_m R}{1 + sRC} \tag{6.7}$$

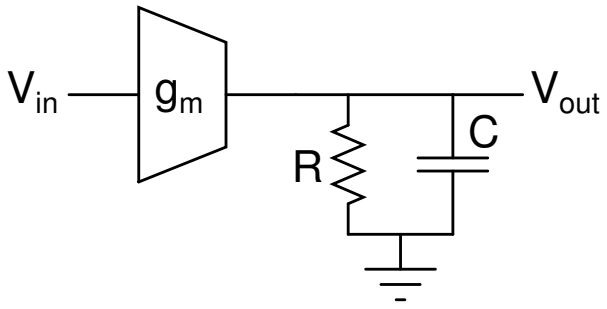

Figure 6.11: Comparator circuit model

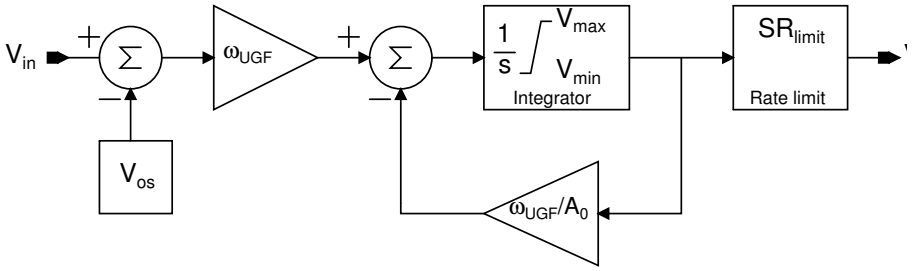

Figure 6.12: Matlab model of a comparator.

Matlab/Simulink does not include resistor or capacitor elements[1], so to implement this circuit model in Matlab/Simulink, it must be converted to a generic signal flow model. Equation 6.7 can be multiplied out and rearranged into the form of Equation 6.8, using the substitutions A_0=g_mR and ω_p=$\frac{1}{RC}$.

$$V_{out} = \frac{1}{s}\left(A_0\,\omega_p\,V_{in} - \omega_p\,V_{out}\right) \tag{6.8}$$

This can then be written in terms of integrator unity gain frequency ω_{ugf}, as $\omega_{ugf} = A_0\omega_p$. This gives Equation 6.9, which by inspection can be seen to be identical to the implemented Simulink comparator model shown in Figure 6.12, except for the addition of offset V_{os} and slew-rate limiting in the Simulink comparator model, which are not included in this equation.

$$V_{out} = \frac{1}{s}\left(\omega_{ugf}\,V_{in} - \frac{\omega_{ugf}}{A_0}V_{out}\right) \tag{6.9}$$

Thus, a single-pole amplifier with parameterisable DC gain A_0, unity gain frequency ω_{ugf}, maximum slew rate SR_{max}, output voltage limits V_{max} and V_{min}, and offset V_{os} was created and is shown in Figure 6.12. The system model was simulated to determine comparator values which would limit degradation of system performance (oscillation frequency and linearity) to acceptable values. The resulting comparator parameters

[1] Additional Simulink toolboxes do exist which provide analogue circuit components including resistors and capacitors, but these are not always available.

are shown in Table 6.5. An important result from the modelling was that the most important property of the comparator was its propagation delay t_p, which is influenced by the architecture, slew rate and bandwidth.

Table 6.5: Comparator specifications

Parameter	Target value
V_{max}	3.3 V
V_{min}	0 V
DC gain	30dB
ω_{ugf}	3 GHz
SR_{limit}	16.5e9 V/s
V_{os}	50 mV

At the circuit level, the comparator must drive the non-overlapping clock generator, which has approximately 50fF of input capacitance. Due to considerable physical separation between the non-overlapping clock generator and the comparator, there is approximately 350fF of additional parasitic capacitance at the comparator output for a total comparator load capacitance (C_{load}) of 400fF.

The load capacitance requirement and the high slew rate specification result in a high slewing current requirement of:

$$I_{slew} = SR_{limit} \times C_{load} = 6.6\,\text{mA}. \tag{6.10}$$

This high slew current requirement suggests that a push-pull output stage should be used. If this is considered along with the requirement for low propagation delay, then a suitable architecture for the comparator can be identified: the single pole open loop symmetrical comparator with push-pull output stage, which is know[117] for good slewing characteristics and low propagation delay. There is a choice of whether to use the NMOS-input version of the circuit or the PMOS-input version. While the NMOS-input has higher g_m and so higher gain-bandwidth product, it includes two slow PMOS mirror poles and a NMOS mirror pole. The PMOS-input version has two NMOS mirror poles and one PMOS mirror pole, and the NMOS mirror poles are likely to be higher frequency than the PMOS mirror poles, so is likely to be faster.

The choice of input device is also influenced by the output level of the preceding stage. As will be discussed in Section 6.5.4.8, a simple source-follower buffer is used at the loop filter output, to drive the comparator inputs, and the output level of this buffer will

have an impact on whether a PMOS or NMOS comparator input stage is practical. The NMOS source follower suggests a PMOS input stage would be most appropriate, but with adjustment to the loop filter output common-mode voltage, either input topology can be supported.

As an existing NMOS-input symmetrical comparator was available from previous work, this was re-used here, although a PMOS-input symmetrical comparator may have been more appropriate due to the improved non-dominant poles. While it is a reuse of an existing block, the comparator design will still be discussed below.

The comparator schematic shown in Figure 6.13 also includes an additional logic buffer stage, M_{p5} and M_{n5}, to isolate the comparator from parasitic routing capacitance that may be present at the comparator output, but will not be understood accurately until late in the design process.

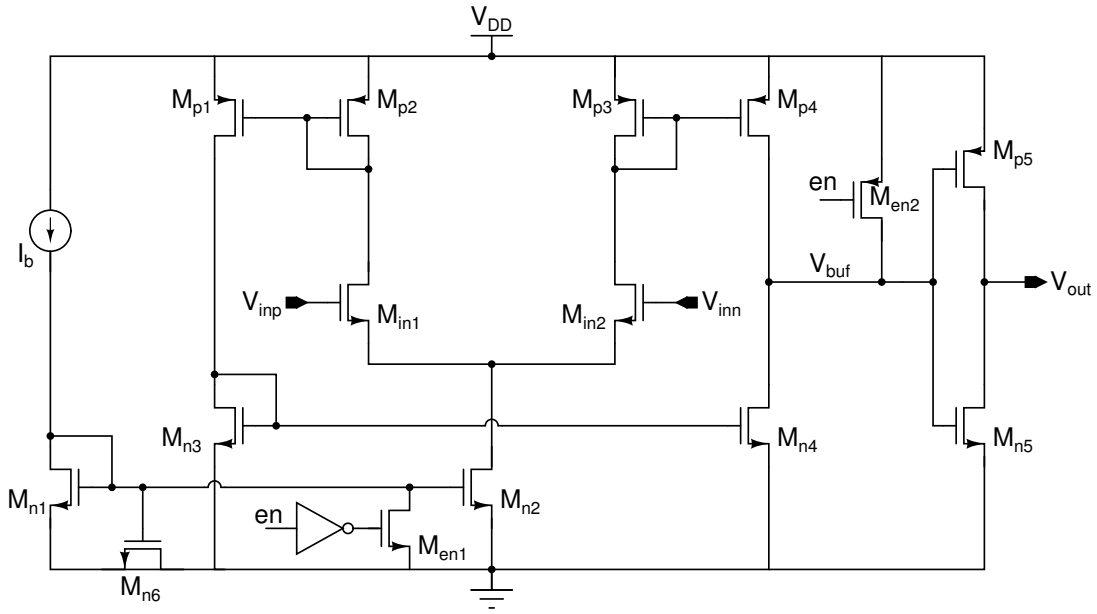

Figure 6.13: Schematic of an open loop symmetrical comparator with push-pull output stage and additional output buffer.

Transistor design starts from the output and works backwards. The node V_{buf} will be a rail-to-rail output, so M_{p5} and M_{n5} will operate in their linear regions, and the time constant of V_{out}, τ_{OUT}, will be defined by the transistor on resistance R_{on} and C_{load}. A 10% – 90% rise takes $2.2\tau_{OUT}$, so the required widths of M_{p5} and M_{n5} can be found by substituting Equation 6.11 into Equation 6.6.

$$R_{on} = \frac{V_{DD}}{SR_{limit}} \frac{1}{2.2\, C_{load}} \tag{6.11}$$

An additional factor of $\frac{1}{2}$ has been applied to the result of Equation 6.11 to give some margin, and the resulting widths of M_{p5} and M_{n5} are shown in Table 6.6. These devices

are set to minimum length to minimise capacitive loading on the main part of the comparator.

Table 6.6: Comparator device sizes

Device	$M_{in1/2}$	M_{n1}	M_{n2}	$M_{p1/2/3}$	M_{p4}	M_{n3}	M_{n4}	M_{p5}	M_{n5}
Width (μm)	32	8	128	16	64	8	32	24	12
Length (μm)	0.34	1	1	0.3	0.3	0.34	0.34	0.3	0.34

The effective capacitance seen at the input V_{buf} of the logic buffer must be considered next. Section 3.2.3.1 describes in detail the gate capacitance seen as the input of a CMOS logic buffer changes from supply to ground, and should be consulted for further detail. In summary, the device driving the output transition – PMOS, for the example case of a low-to-high output transition – will operate primarily in saturation, while the device that is opposing the transition – NMOS, for this example – will operate primarily in its linear region. There is only a small miller multiplication of the gate-drain capacitance of the PMOS as the impedance at the buffer output is low due to the NMOS in its linear region, and the equations of Section 3.2.3.1 predict an effective gate capacitance of 50fF.

An additional 50fF of parasitic capacitance is assumed due to the drain capacitance of M_{p4}/M_{n4} and parasitic routing capacitance on V_{buf}, so to achieve a GBW of 3GHz, the g_m of the voltage-current transconductors $M_{n1/2}$ must be set as in Equation 6.12.

$$g_m = \text{GBW} \times 2\pi C_{load} \tag{6.12}$$

With C_{load} = 100fF, the required g_m from input devices $M_{in1/2}$ is 1.9 mS. This assumes a first-order response from the amplifier but it is likely that non-dominant poles will be present in the structure around the unity gain frequency and so to compensate, the target gm has been set at 3 mS.

From Equation 6.13, the drain current can be found. The choice of $V_{gs}-V_t$ is a trade-off between offset and current consumption so is set to 0.25 for a compromise between the two. The required value of I_d is thus 375 μA, and has been rounded up to 400 μA.

$$I_D = \frac{g_m (V_{gs} - V_t)}{2} \tag{6.13}$$

The transistor widths can be calculated using Equation 6.14, which uses MOSFET saturation parameter K. Transistor length L was chosen as minimum length to minimise capacitance on the internal mirror nodes and prevent non-dominant poles from impacting

performance significantly. The results widths are shown in Table 6.6.

$$W = \frac{2\,L\,I_D}{K\,(V_{gs} - V_t)^2} \tag{6.14}$$

Active mirror devices M_{p2}, M_{p1}; M_{p3},M_{p4}; and M_{n3},M_{n4} were initially sized with 1:1 ratios, with $(V_{gs} - V_t)$=0.5V and with minimum length in order to minimise parasitic capacitance. However, node V_{buf} was found to be slew limited. Increasing the mirror ratio of M_{p3},M_{p4} and M_{n3},M_{n4} to 1:4 removed the slew limit while keeping the GBW roughly the same. It would be expected that a 1:4 mirror ratio would increase the g_m (and hence GBW) at node V_{buf} by a factor of four, but the extra parasitic capacitance due to increased sizing of M_{p4} and M_{n4} negated any GBW increase.

The biasing mirror, $M_{n1/2}$ was sized for a moderate $(V_{gs} - V_t)$=0.3 based on the swing requirements at the drain of M_{n2}, and uses a long length to improve output resistance. M_{n6} is a MOS capacitor which decouples the bias node, and enable devices $M_{en1/2}$ pull the bias node and comparator output low and high, respectively, when an enable signal is low.

Finally, the offset should be calculated to check that it is not excessive. There are two significant contributors to the offset, the input device V_t mismatch, and the switching level of the logic buffer M_{p5} and M_{n6}.

Assuming mismatch proportionality constant A_{VT}=8 mVμm for a 0.13μm process, as given in [91], the estimated 3σ offset V_{os}' due to input device mismatch is given by Equation 6.15.

$$V_{os}' = \frac{3\,A_{VT}}{\sqrt{W\,L}} \tag{6.15}$$

$$\approx 7\text{mV} \tag{6.16}$$

The logic buffer has a threshold voltage which varies over process corner, as shown in Table 6.7, where threshold voltage range (maximum minus minimum) is 121mV. This range should be divided by the gain of the first stage, which is measured as 34dB, to give an input offset due to logic buffer threshold voltage process variation, of 2.4mV.

The total input referred offset is thus the sum of the two numbers above - they do not add in quadrature as the threshold voltage variation is a systematic effect on a particular die. The total comparator input offset is thus 9.4mV, which meets the target V_{os}.

The comparator layout is shown in Figure 6.14. The main parts are the comparator

Table 6.7: Comparator logic buffer switching threshold vs corner, schematic simulation results. TT is typical NMOS, typical PMOS. FS is fast NMOS, slow PMOS, and the other corners can be determined by analogy.

Temperature	TT	FF	SS	SF	FS
-40 C	1.496	1.487	1.506	1.545	1.449
90 C	1.507	1.489	1.523	1.559	1.456
125 C	1.517	1.498	1.534	1.570	1.465

core (left) and the bias block (right). The sections of the comparator core are, from top-to-bottom: input devices, PMOS active mirrors, NMOS active mirrors, device M_{p5} and finally device M_{n5}. The signal flow is top-to-bottom; the comparator inputs come in at the top and the output is at the bottom.

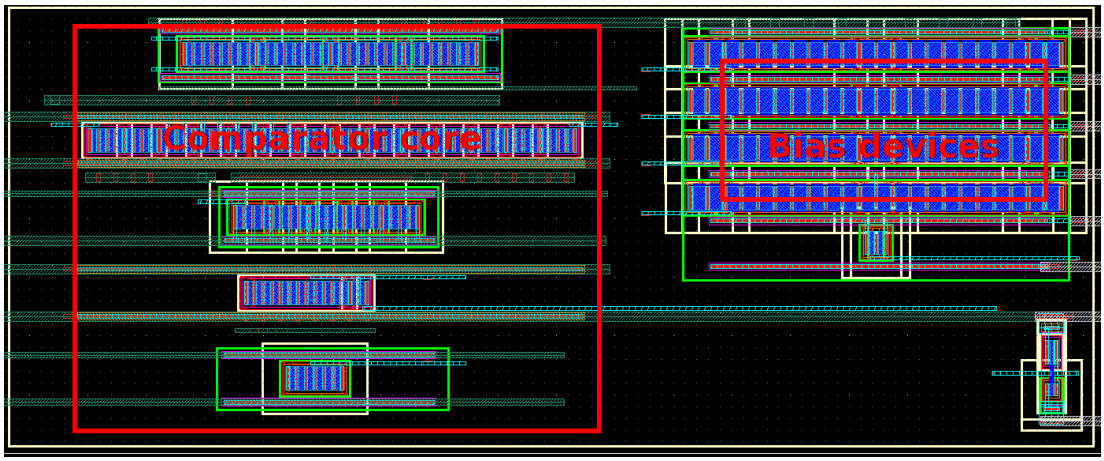

Figure 6.14: Layout of the open loop symmetrical comparator. A more compact layout is possible but there was no area constraint on this test chip and so additional area was used to accelerate the layout process.

6.5.4 Loop filter

A second order loop filter transfer function has been determined in 6.4.2. Using the loop filter synthesis procedure described in Sections 5.5.3 – 5.5.5, a differential loop filter was created, as shown in Figure 6.15. With reference to this figure, the integrators are implemented using current buffers – shown as an isosceles trapezium with the text "I->I" – whos inputs act as a virtual ground, holding a fixed input voltage and sinking or sourcing current as required. A resistor, for example R_b, is connected between an integrator voltage input such as V_{inp} and the current buffer virtual ground, and the voltage between V_{inp} and the virtual ground node will linearly be converted to a current

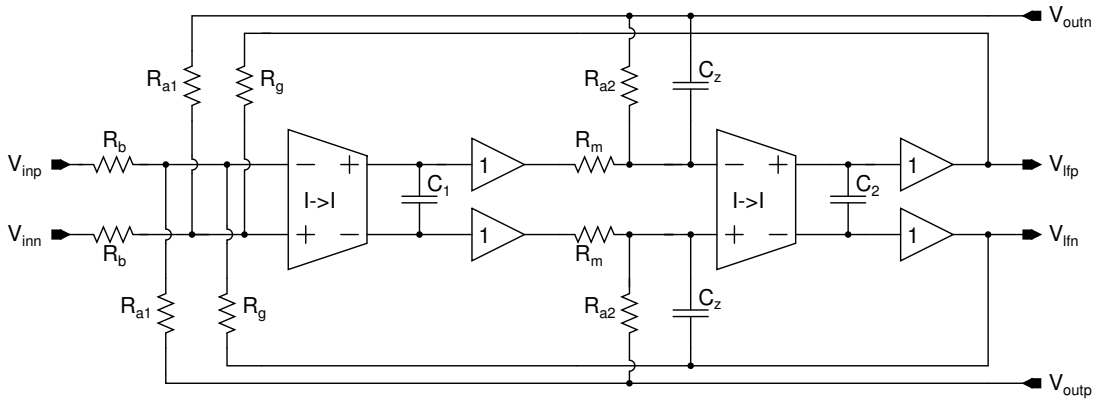

Figure 6.15: Circuit which implements a second order Chebyshev type 2 loop filter. Cells marked "I->I" are current buffers which mirror an input current to the output.

buffer input current, which is then injected by the current buffer on to an integration capacitor.

To put this in context, the current buffer based integrator will be compared to the more common Op-amp integrator and g_m-C integrator. The main metrics for active filters are:

- Linearity/distortion performance
- Swing of input signal, related to linearity - smaller input swings are more linear.
- Bandwidth
- Variation of the integrator time constant τ over process/temperature changes. This is important because integrator stages are often combined to make higher order filters. If the time constant of each stage varies, the higher order loop filter response may change.
- Ease of tunability, to correct for process or temperature variations.

A summary of how the different integrator structures compare against these metrics is given in Table 6.8.

Due to the wide bandwidth in this application, the g_m-C or Current buffer structures are most appropriate. However, as the current buffer input is a virtual ground and the input signal is a current rather than a voltage, it can tolerate a large input (current) swing, which relaxes the noise requirements as the input signal can be larger, and it can also achieve higher linearity than the g_m-C structure.

The current buffer integrator will be discussed further in Section 6.5.4.1. Note that buffers are required after the integrators as the structure can not drive resistive loads.

Table 6.8: Comparison of integrator structures.

Metric	Op-amp RC	g_m-C	Current buffer
Linearity	High: linear V-I conversion using resistor and in a high gain, closed-loop configuration to reduce nonlinearity.	Low: Relies on linearity of degenerated MOS-input devices, and open-loop.	Medium: Linear V-I conversion using resistor, but open-loop.
Swing	High: input resistor does V-I conversion, amplifier does not see large voltage swing.	Low: Input swing seen directly on transistor gates	High: input resistor does V-I conversion, current buffer does not see large voltage swing.
Bandwidth	Low: Loop gain decreases at high frequency due to low frequency op-amp pole	High: open-loop	High: open-loop
Variation	High: depends on R and C, both of which vary	Medium: depends on C, and C ratios match well on a die so in a high order filter, the C variation may cancel	High: depends on R and C variation.
Tunability	Low: Requires cumbersome R and C trimming banks, which can introduce distortion.	High: Can be varied by adjusting the g_m	High: Can be varied by adjusting the current-buffer gain.

Component values are derived from Equation 6.5 using the method in Section 5.5.4, although there are more unknowns than there are equations and so the components R_{a1}, C_1 and R_m can be chosen based on design constraints, before computing the values of R_b, R_g, R_{a2} and C_2 required to give the desired L_1 and L_0 transfer functions.

The choice of R_{a1} and R_b set the low frequency STF gain; from Equations 5.27 and 5.31, at DC the STF is given by:

$$\mathrm{STF} = \frac{R_{a1}}{R_b} \frac{A_{DC}}{1 + A_{DC}} \tag{6.17}$$

Where A_{DC} is the DC gain of L_1. This is approximately equal to the magnitude of the Chebyshev stop band ripple parameter R_s, and so for a desired $|\mathrm{STF}| = 1$, Equation 6.17 can be reversed to find an approximate value of:

$$R_b \approx 0.75 R_{a1} \tag{6.18}$$

The input and feedback resistor's thermal noise will be the dominant noise contributors in the circuit as they are present before the first integrator, which will attenuate subsequent noise sources. The noise requirements are determined by the target MTPR. As above, an MTPR of 40dB was typically seen in numerical, noise-free simulations with a Verilog-A loop filter and schematic output stage. Circuit noise should be chosen to not impact this MTPR performance.

A noise level 12dB below the distortion level was chosen. For a 40dB MTPR and a maximum injected power of -56 dBm/Hz, as per Section 2.3, circuit noise should be below $p_{n_{\mathrm{dBm/Hz}}} = -108$ dBm/Hz. This is a noise power on the powerline, it must be converted to a voltage per $\sqrt{\mathrm{Hz}}$, v_n, at the line driver output using Equation 6.19

$$v_n = \frac{1}{N}\sqrt{\frac{10^{\left(\frac{p_{n_{\mathrm{dBm/Hz}}}}{10}\right)}}{\mathrm{R_{load}}1000}} \tag{6.19}$$

In this equation, N is the transformer ratio, $\mathrm{R_{load}}$ is the line driver load resistance and 1000 is a factor to convert from milli-Watt to Watt. v_n will include the noise from both sides of the differential system – $2 \times \mathrm{R_b}$ and $2 \times \mathrm{R_{a1}}$ – and also from other noise contributors such as the input devices of the current buffer. Half of the v_n noise budget is allocated to the resistors, and using Equation 6.18, and noise Equation 6.20, $\mathrm{R_{a1}}$ can be determined.

$$v_{n_{\mathrm{R_{a1}}}} = \sqrt{4\,\mathrm{k\,T}\,(2 \times (1 + 0.75))} \tag{6.20}$$

For a worst case situation (T=125C), $\mathrm{R_{a1}}$ should be set less than 320 kΩ. This is a very relaxed specification and may even cause problems post-layout; any parasitic capacitance on the order of $1/\left(\mathrm{R_{a1}}\,2\pi 30e6\right) \approx 15f\mathrm{F}$ will add extra in-band poles to $\mathrm{L_1}$, affecting loop gain. $\mathrm{R_{a1}}$ was thus chosen as 25 kΩ, which comfortably meets the specification and allows moderate values of layout parasitics without affecting the NTF.

$\mathrm{R_{a1}}$ is now determined, but $\mathrm{R_m}$ and $\mathrm{C_1}$ must still be chosen. One constraint is that a single integrator cell was designed and then used twice in the design; once for the first integrator and once for the second integrator. This is not optimum from a current consumption perspective as the second integrator can tolerate higher noise and so can consume lower current, but it considerably reduces the design, layout and verification time.

A spreadsheet is useful to calculate the remaining component values for a range of $\mathrm{R_m}$ and $\mathrm{C_1}$ values, accounting for coefficient scaling. The maximum swings at each point in the circuit, the current buffer input voltage and the resistor values define the peak currents that can flow in to and out from each current buffer. Using this information, values of $\mathrm{R_m}$ and $\mathrm{C_1}$ were chosen which minimised the current required in both current buffer cells. The final values, after coefficient scaling, were $\mathrm{R_m}$=12.5kΩ and $\mathrm{C_1}$=600fF. The peak current flowing in and out of the current buffer is 350uA.

Finally, the zero $\mathrm{C_z}$ which short-circuits the first integrator at high frequency was set to give a zero frequency of $\mathrm{f_z}$=120MHz, using Equation 6.21.

$$\mathrm{C_z} = \frac{1}{2\,\pi\,\mathrm{f_z R_{a2}}} \tag{6.21}$$

In addition to improving the phase shift around the self-oscillation frequency, this L_1 zero moves the NTF poles off the imaginary axis, resulting in a lessening of the depth of the stop band notch. It is still more than 30dB deep and more than sufficient for this application.

All remaining component values can now be calculated, and are shown in Table 6.9.

Table 6.9: Component values for the circuit shown in Figure 6.15.

Ra1 (kΩ)	Ra2 (kΩ)	Rb (kΩ)	Rm (kΩ)	Rg (kΩ)	C1 (fF)	C2 (fF)	Cz (fF)
25	26	12.5	17	12.5	300	300	50

6.5.4.1 Differential current buffer

The top-level structure of the current buffer is shown in Figure 6.16. It is a pair of single-ended current buffers in a pseudo-differential configurations. A Common-mode Feedback (CMFB) block creates a stable output common-mode voltage. A half-cell layout strategy was used to improve symmetry of the layout. Every device within Figure 6.17 has been halved in size from its original designed value, and then two instances of the half-sized block are placed adjacent to each other.

The current buffer cells have a low impedance input, so for example, when one terminal of a resistor is connected to the current buffer and a voltage is applied to the other terminal of the resistor, the resistor will perform a voltage to current conversion and that current will flow through the current buffer and then be forced onto the integration capacitor.

6.5.4.2 Single-ended current buffer cell

The differential current buffer is made from two single ended current buffer cells shown in Figure 6.17. The input I_{in} is connected to the source terminal of common-gate device M_1, the gate of which is biased at a DC voltage V_{ref}. This device acts as a source follower, holding the voltage at node V_{in} fixed at V_{ref}-V_t-$Vdsat_{M1}$, and so ensures the input is low impedance. The core of the cell is comprised of transistors M_{in}, M_{sf}, M_{nm2} and M_{nm1}, which implement a new type of super source follower structure. An input current I_{in} flowing into node V_{in} will generate a large voltage change on high impedance node V_x which will, via M_4, raise V_y correspondingly. Node V_y will adjust the current

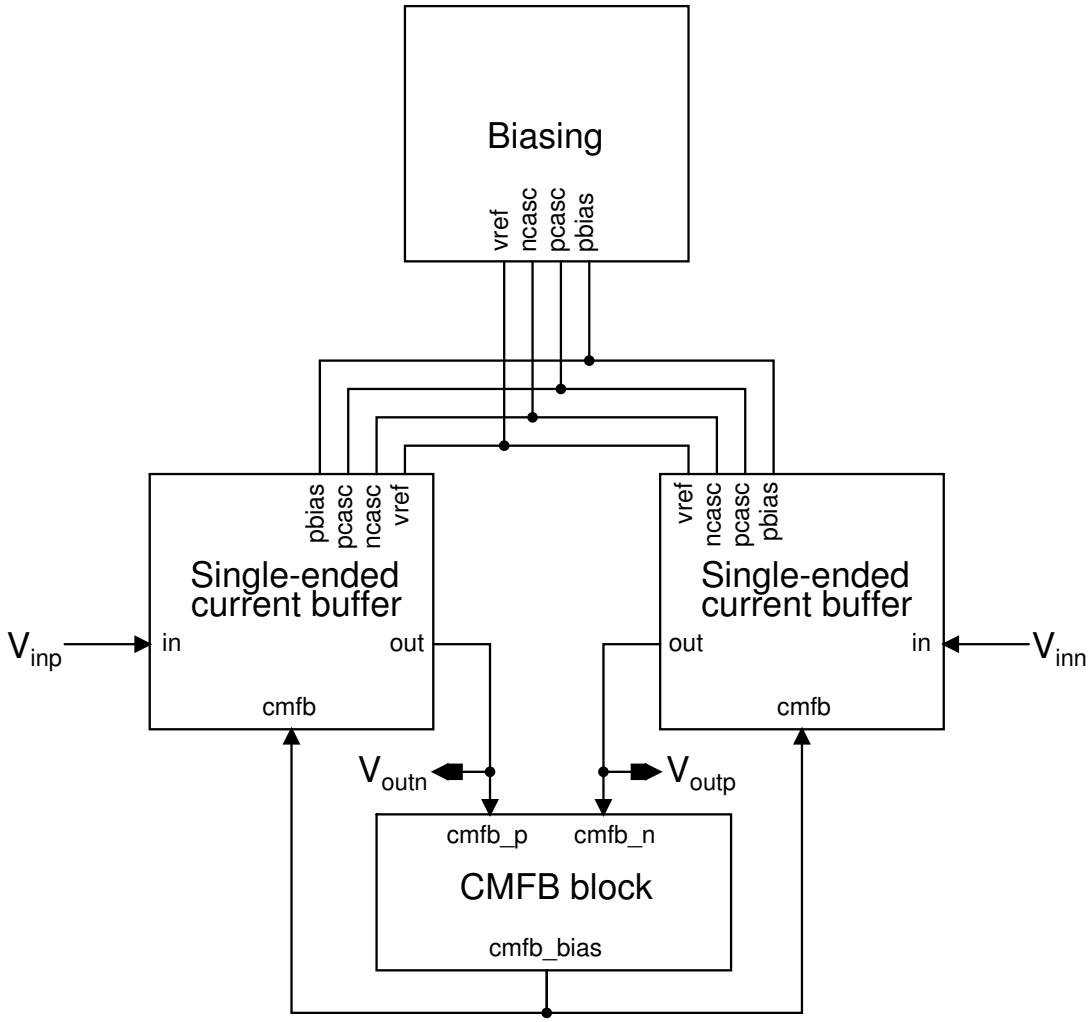

Figure 6.16: Top level half-structure of the current buffer. The entire half-structure is repeated twice.

through M_2 until the additional current through M_2 matches the current I_{in}. This current is also mirrored to the output via M_7. In this way, the impedance at V_{in} is lowered by the gain of the loop, which keeps V_{in} fixed over a very wide input current range, ensuring a high linearity. The use of a NMOS-only signal path also means that the structure can achieve very wide bandwidth due to the higher g_m per unit area of NMOS devices versus PMOS devices.

An additional feature, which is not taken advantage of here, is that the virtual ground input means the structure can be used with input voltage swings beyond the supply rail of the chip, as the only component which will see the high voltage is the resistor which performs the transconductance operation, and these can tolerate very high voltages.

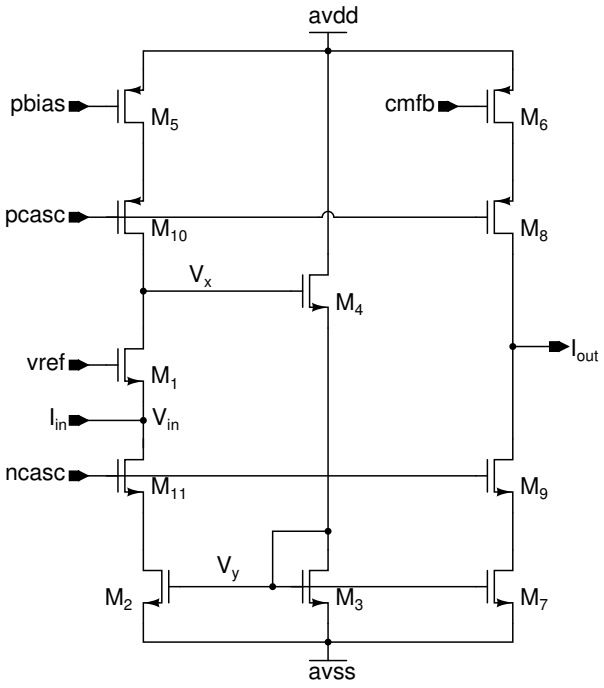

Figure 6.17: Schematic of the single ended current buffer cell.

6.5.4.3 Input impedance analysis

To confirm the operation of the loop, a small signal analysis of the input impedance will be carried out. The small signal model for this is shown in Figure 6.18. Only the super-source follower loop is shown, and cascode devices have been removed for clarity. Terms r_x represent the small signal drain-source resistance of transistor x, according to the transistor numbering in Figure 6.17.

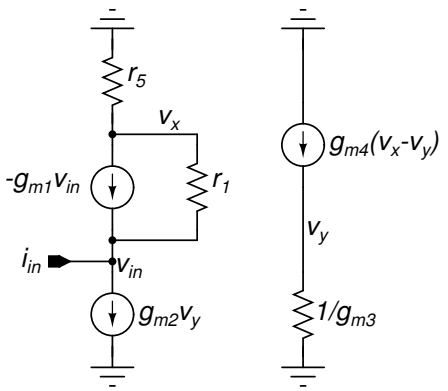

Figure 6.18: Small signal model of current buffer for input impedance analysis.

Using Kirchoff's Current Law, the nodal Equations 6.22, 6.23 and 6.24 can be written for nodes v_y, v_x and v_{in}, respectively. Note that the substitution $g_x = 1/r_x$ is used to

improve clarity.

$$i_{in} = v_x \left(\left(\frac{g_{m2}\, g_{m4}}{g_{m4} + g_{m3}} \right) + g_1 \right) + g_{m1}\, v_{in} \tag{6.22}$$

$$v_x = v_{in} \frac{g_{m1} + g_1}{g_5 + g_1} \tag{6.23}$$

$$v_y = \frac{g_{m4}}{g_{m4} + g_{m3}} v_x \tag{6.24}$$

Using the assumptions that $g_{m2} = g_{m3} = g_{m4}$ and $\{g_{m1}, g_{m2}\} > g_1$, and solving the equations above for i_{in} results in the following expression, Equation 6.25.

$$i_{in} = v_{in} \left(\frac{g_{m1}\, g_{m2}}{2\ (g_5 + g_1)} \right) \tag{6.25}$$

This can be solved for input impedance r_{in} as in Equation 6.26, where the substitution above is reversed; $r_x = 1/g_x$.

$$r_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{g_{m1} \left(\frac{g_{m2}\ (r_5 // r_1)}{2} \right)} \tag{6.26}$$

This shows an reduction of input impedance by a factor $g_{m2}\,(r_5 // r_1)\,/2$ versus the conventional[118] source follower, and confirms the operation of the structure.

6.5.4.4 Pole analysis

To gain some design insight, a small-signal analysis of the loop is required to determine the position of poles in the structure, and the stability properties of the loop. A enhanced small signal model which includes frequency-dependent components is shown in Figure 6.19. Capacitors c_x, c_y and c_{in} represent the lumped parasitic capacitance on each of the respective nodes. To find the closed loop pole positions, the loop must be broken. This is done by breaking the v_y node between the output of mirror device M_3 and the gate of mirror device M_2, as shown in the diagram.

The loop equations can now be written using Kirchoff's Current Law and solved to find v_y / v'_y, giving Equation 6.27.

$$\frac{v_y}{v'_y} = \frac{-g_{m1}\, g_{m2}\, g_{m4}}{(g_{in}\, g_1 + g_5\,(g_{in} + g_{m1}))\,(g_{m3} + g_{m4})} \times \frac{1}{\left(s^2 \left(\frac{c_x\, c_{in}}{g_{in}\, g_1 + g_5 (g_{in} + g_{m1})} \right) + s \left(\frac{c_x (g_{in} + g_{m1}) + c_{in} (g_1 + g_5)}{g_{in}\, g_1 + g_5 (g_{in} + g_{m1})} \right) + 1 \right) \left(s \left(\frac{c_y}{g_{m3} + g_{m4}} \right) + 1 \right)} \tag{6.27}$$

With normal component sizes, the second order term consists of two real poles, ω_{p1} and

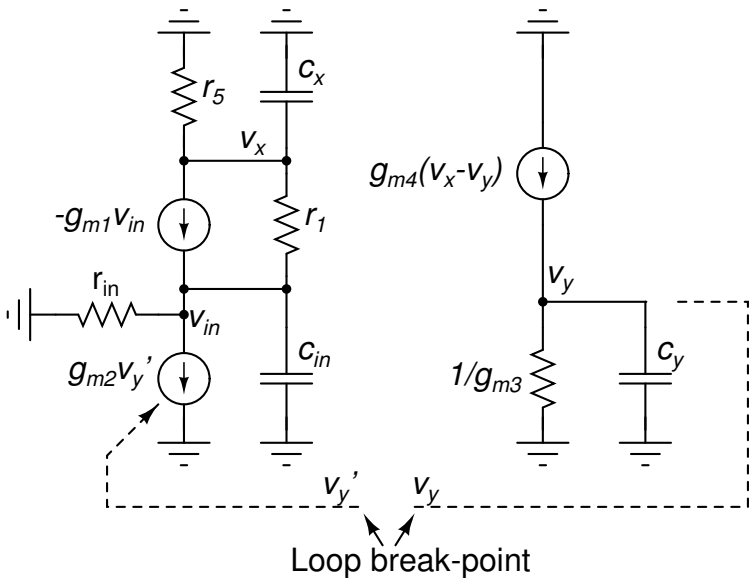

Figure 6.19: Small signal model of current buffer for stability/pole analysis.

ω_{p2}, which are widely spaced in frequency ($\omega_{p1} \ll \omega_{p2}$). We can then write:

$$\left(\frac{s}{\omega_{p1}} + 1\right)\left(\frac{s}{\omega_{p2}} + 1\right) \approx \frac{s^2}{\omega_{p1}\,\omega_{p2}} + \frac{s}{\omega_{p1}} + 1 \tag{6.28}$$

Comparing coefficients of s against the second-order term in Equation 6.27, expressions for the two poles can be obtained.

$$\omega_{p1} = \frac{g_{in}\,g_1 + g_5\,(g_{in} + g_{m1})}{c_x\,(g_{in} + g_{m1}) + c_{in}\,(g_1 + g_5)} \tag{6.29}$$

$$\omega_{p2} = \frac{c_x\,(g_{in} + g_{m1}) + c_{in}\,(g_1 + g_5)}{c_x\,c_{in}} \tag{6.30}$$

Assuming $g_{m1} \gg g_1 \gg g_5$ for ω_{p1}, $g_{m1} \gg (g_{in} + g_5 + g_1)$ for ω_{p2}, and that $c_x \approx c_{in}$, these equations simplify to Equations 6.31 and 6.32. There is an additional first order term in Equation 6.27 which gives rise to a pole ω_{p3} as shown in Equation 6.33.

$$\omega_{p1} \approx \frac{g_{in}\,g_1}{c_x\,g_{m1}} \tag{6.31}$$

$$\omega_{p2} \approx \frac{g_{m1}}{c_{in}} \tag{6.32}$$

$$\omega_{p3} \approx \frac{g_{m3} + g_{m4}}{c_y} \tag{6.33}$$

Usually, ω_{p1} is at a low frequency and will be the dominant pole of the system. ω_{p2} and ω_{p3} are closely spaced poles at very high frequency.

For typical component values ($g_{m1} \gg g_{in}$ and $g_1 \gg g_5$), the DC gain A_0 can be simplified

to Equation 6.34.

$$\mathrm{A}_0 = \frac{g_{m1}\, g_{m2}}{2\, g_{in}\, g_1} \tag{6.34}$$

One final useful equation is the unity-gain frequency of the buffer. This can be found using Equations 6.34 and 6.31 and is given in Equation 6.35.

$$\mathrm{UGF} = \frac{g_{m2}}{2\, c_x} \tag{6.35}$$

To verify the analysis, a transistor level current buffer was design and simulated. The results of a stability analysis of the buffer loop were compared with the transfer function in Equation 6.36, where the DC gain and poles are defined as in Equations 6.31–6.34. The bode plots, shown in Figure 6.20 show a good match between theory and schematic.

$$\mathrm{H}(s) = \frac{\mathrm{A}_0}{(\frac{s}{\omega_{p1}} + 1)\,(\frac{s}{\omega_{p2}} + 1)\,(\frac{s}{\omega_{p3}} + 1)} \tag{6.36}$$

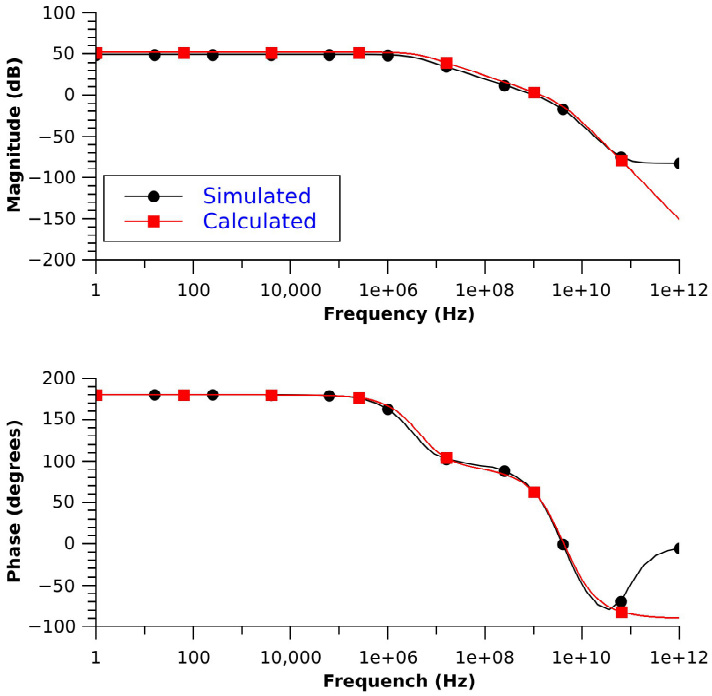

Figure 6.20: Bode plots of the current buffer loop, showing transistor-level simulation results versus approximate design equations.

6.5.4.5 Current buffer design

Using a Verilog-A model of the current buffer cell and the circuit modelling methodology described in Section 5.4, specifications were determined for the current buffers by sweeping parameter values and examining the resulting L_1 bode plot. As A_0 and the unity gain frequency of the current buffers decrease, the L_1 starts being impacted by the buffers, and this is seen first in the L_1 stop band pole moving to lower frequencies. For a minimal impact on L_1, the current buffer A_0 should be $>$ 40dB, with a unity gain frequency of greater than 500 MHz. However, the current swing requirement of the current buffers is also relevant. During the loop filter design (Section 6.5.4) a maximum sink/source current for the current buffer inputs of 350uA was determined. With PMOS bias currents in the input and output branches of 400uA, and with devices sized to ensure the circuit is DC biased correctly, values of A_0 and UGF are obtained which exceed the required values – as shown in Figure 6.20.

Final design values for the current buffer are given in Table 6.10. Note that these values are for the layout half cell as described in Section 6.5.4.1; the cell is used twice in parallel to make the full single-ended current buffer.

Table 6.10: Component values for the circuit shown in Figure 6.17.

	M1	M2/3/7	M4	M5/6	M8/10	M9/11
Length (μm)	30	13	8	120	40	6.8
Width (μm)	0.5	0.5	0.5	1	0.34	0.34

6.5.4.6 CMFB

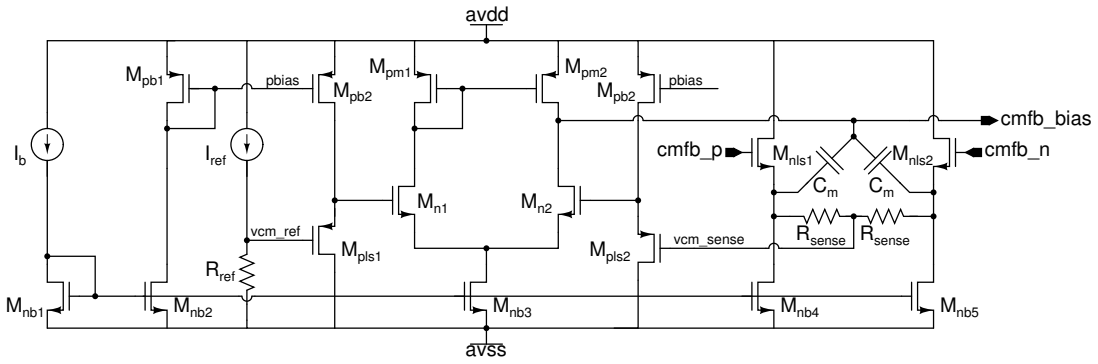

Figure 6.21: Common Mode Feedback circuit, used to set the output common-mode level of the integrator.

A common-mode feedback (CMFB) circuit is required to set the output common-mode

voltage of the current buffers. The integrator outputs connect to the cmfb_p and cmfb_n pins on the CMFB circuit shown in Figure 6.21. The output signal is buffered and then applied to common-mode sense resistor R_{sense}. The sensed voltage is used as an input to an amplifier, which compares the sensed level against an desired level. The output, cmfb_bias, drives one half of the two parallel current buffer layout cells.

The CMFB UGF was set at 35MHz as this was sufficient in circuit model simulations. In order to stabilise the CMFB loop, Miller compensation capacitors C_m are used.

6.5.4.7 Biasing

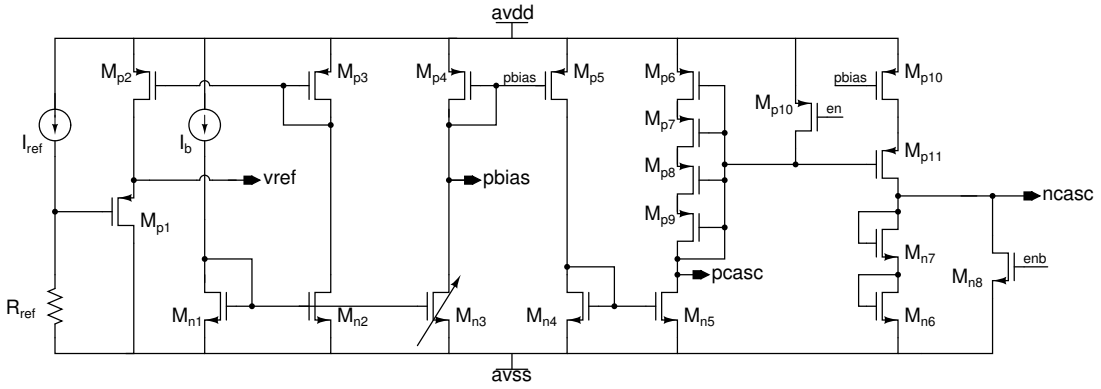

Figure 6.22: Bias circuitry used by other Integrator blocks.

For completeness, the bias structure used to generate all voltages in the remainder of the integrator is shown in Figure 6.22. I_{ref} is 100uA and is generated by applying a bandgap voltage to an on-chip polysilicon resistor made of 1kΩ units, and mirroring out the current that flows. R_{ref} is 16.5kΩ and is made up of the same unit resistor cells as used to generate the reference current, so any resistor process or temperature variation is cancelled out and a stable 1.65V reference voltage is created.

Similarly, the current I_b is a 25μA bias current which is generated by applying a bandgap voltage to an off-chip 1% accurate resistor and again mirroring out the current. This ensures that the bias currents used are well controlled and do not vary with process or supply voltage changes.

6.5.4.8 Buffer

The use of a gm-C integrator which must drive a resistive load means buffers must be used at the output of the integrator. A simple source-follower was used with -3dB point of at least 1GHz in order to minimise the degradation of overall performance. To reduce distortion, the body effect on the source-follower device was eliminated by connecting

the bulk and source terminals. This has a bandwidth penalty as the source terminal – which is source follower output – sees the bulk-to-well capacitance and so requires additional current to meet the bandwidth specification.

6.5.4.9 Layout

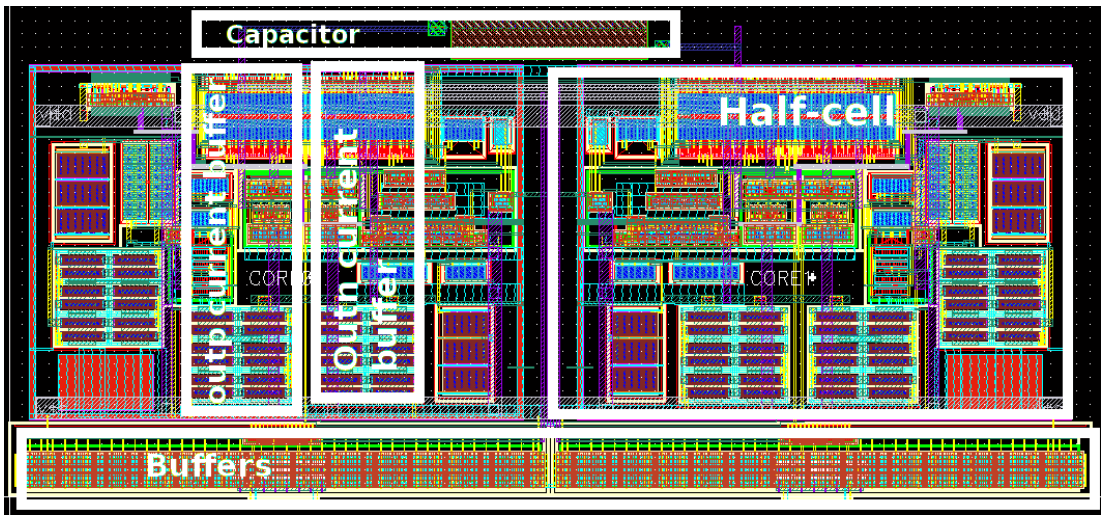

Figure 6.23: Layout for an Integrator, including integration capacitor and output buffers.

The layout for the completed integrator is shown in Figure 6.23. The same integrator was used for the both the first and second integrators required for the loop filter. The two half-cells are visible, one on the left and the other (highlighted) on the right. This strategy ensures a symmetrical layout to reduce the impact of temperature and process gradients across the chip.

6.6 Other design issues

6.6.1 di/dt Limit

Figure 6.24 shows the Class-D output stage. For simplicity, the output filter and load impedance have been replaced by a current source, which is an accurate approximation over a period of time which is comparable to the rise/fall times of the Class-D output stage. L_{vdd} and L_{vss} are parasitic inductors associated with bondwires and package parasitics.

When V_{OUT}=V_{OUTP}−V_{OUTN} is high, current flows through L_{vdd}, M_{P1}, the load model, M_{N2} and L_{vss} as shown by the red line of Figure 6.24. When the output changes state, M_{P1}/M_{N2} turn off and M_{P2}/M_{N1} turn on. The load current source will keep current

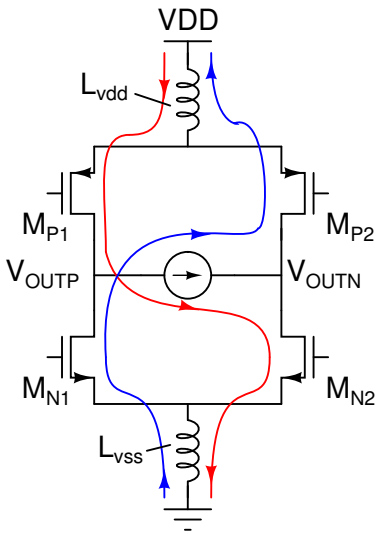

Figure 6.24: Current flow on two phases of a Class-D output stage. The current paths for the two differential output states ($\pm V_{DD}$) are shown in red and blue.

flowing in the same direction regardless of switch state, so by the end of the transition, the current flow will be as shown by the blue line in Figure 6.24. During this transition period, the current flow through L_{vdd} and L_{vss} must reverse and so a voltage V_{ind} will develop across the bondwire inductors according to Equation 6.37.

$$V_{ind} = L\frac{di}{dt} \tag{6.37}$$

To avoid over-stress on 3.3V transistors, V_{ind} should be kept below 0.33V. By rearranging Equation 6.37 in terms of L, using i=2 $\times$ 378mA from Table 6.2 for a 1:4 transformer, and estimating the transition time of the output stage to be 0.5 ns, a maximum supply inductance value of L_{max}=0.2nH is found.

This supply inductance is achievable when using flip chip packages but these are not cost effective for low volume prototyping. The alternative, wire-bond packages, have typical inductance per bondwire of approximately 2nH. Therefore, 20 pins (10 for V_{DD} and 10 for ground) would be needed to ensure devices do not see over-voltage stress. This was not possible on the fabricated test chip as it would result in more pads than there is area for, so only 6 V_{DD} and 6 ground bondwires/bondpads were implemented. To ameliorate gate oxide reliability concerns, unused area around the output stage was filled with decoupling capacitance between V_{DD} and ground – approximately 1nF in total – as this provides a charge reservoir which limits the excursions of the supply voltages due to high di/dt currents.

6.6.2 Biasing

For the biasing of the chip, a Bandgap circuit and Voltage Controlled Current Source (VCCS) taken from a library of available cells[2] was used. The bandgap provides a temperature stable 1.2V reference voltage, which is used in two places:

- The voltage is applied to an off-chip 1%-tolerance 12 KΩ resistor. The current flowing out to the external resistor is mirrored in units of 25 μA, and these units are used to provide bias currents used in the above schematics.
- The voltage is applied to an internal 12 $K\Omega$ resistor made up of a unit 1 KΩ poly-silicon resistor. The current flowing to this internal resistor is mirrored in units of 25 μA and these units are used for all the reference currents in the above schematics. Blocks that use a reference current to generate a voltage do so using stacks of the same 1 KΩ unit resistor, in order to provide a process and temperature stable voltage.

6.6.3 Digital control

A serial control interface taken from a library of available cells[3] was used to allow control of non-overlap delays, programmable loop delays, trimming of various currents and enabling of the different blocks. It is implemented as a chain of D-type flip flops, which is a serial-in, parallel-out shift register. The shift register uses 1.2V logic cells, so a 1.2V to 3.3V levelshifter has been created to translate the interfaces logic levels into those that can be used by the 3.3V line driver.

6.6.4 Supply/substrate strategy

The 0.13 μm UMC process used here includes a deep N-well (DNW) layer with which it is possible to create a P-well within which NMOS devices can be placed. This isolates the NMOS device from the substrate. All NMOS devices in the design were placed within DNW and PMOS devices are already built within their own N-well. This means that different parts of the design can be placed on different supply/ground domains. The different domains used are:

- Analogue supply domain; used for the loop filter, comparator, bandgap and VCCS

[2]The author would like to thank Steven Collins, who did the design and layout of this block, for allowing its use on this test chip.

[3]The author would like to thank Seyed Danesh, who did the design and layout of this block, for allowing its use on this test chip.

- Non-overlap generator supply domain; used for non-overlap circuit and programmable delay chains.
- Output stage supply domain; used for the the output stage and tapered buffer.
- Substrate; used by the serial control interface and by all substrate taps in the design. This provides a low impedance supply connection which is distributed around the chip to provide an additional layer of isolation between the other supply domains.

The separate domains all have separate bondpads and package pins so that they can be individually decoupled, before being star connected at a common point on the test PCB.

6.6.5 External LC filter

Based on full-system simulation, it was determined that a high-order external filter was needed in order to sufficiently attenuate the Bessel-weighted switching components around the carrier frequency. A 7^{th} order Elliptic low pass filter for zero ohm input impedance and infinite load impedance was implemented based on the method and filter prototypes in [85]. It has a upper pass band corner of 30MHz, a lower stop band corner of 53MHz and a stop band attenuation of 60dB and is designed for a load impedance of 10 Ω. The filter schematic is shown in Figure 6.25.

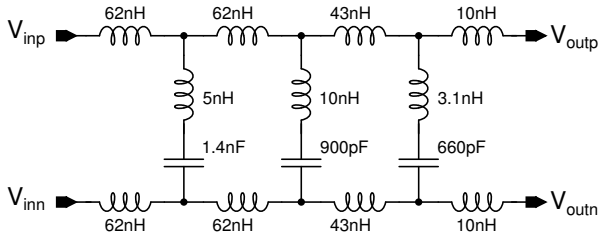

Figure 6.25: Elliptic filter used on test PCB.

6.7 Line driver simulation

Pre-layout and post-layout simulations have been performed on the implemented self-oscillating Class-D line driver. Some selected simulation results will be presented.

Transistor-level simulation of a high frequency self-oscillating switching amplifier is a time consuming task. As signal information is encoded in pulse transition times, the simulator must be set to use very small time steps in order to accurately represent the

pulse transition times, on the order of 10 picoseconds. A HomePlug AV DMT symbol lasts for 41 μs and with such a small time step, will take a very long time to simulate.

Rather than simulating real HomePlug AV symbols, the approach taken here is to generate a short version of the HomePlug AV symbol with a larger carrier spacing but with the same signal bandwidth, so fewer carriers. The generated DMT short signal has a 390 kHz carrier spacing with up to 76 carriers in the 0–30 MHz band, including notched carriers. The period of this short symbol is 2.56 μs, so requires only one sixteenth of the simulation time that the real HPAV symbol does. Comparisons of line driver linearity using the real HomePlug AV symbol and the short symbol show that the short symbol produces a MTPR result that is worse than the real symbol by approximately 0–5dB.

6.7.1 Pre-layout simulation

Pre-layout simulation of the design was carried out as the design progressed. Initial simulations early in the design phase were primarily of Verilog-A functional models but as the design processed, they were replaced by circuit level models as appropriate.

Figure 6.26 shows an AC simulation of the loop filter, showing the typical loop filter transfer function as well as the variation of the loop filter due to resistor and capacitor process variation. In the typical case, the graph matches reasonably well with the chosen L_1 transfer function as shown earlier in Figure 6.4, although the zero frequency has shifted slightly from the 22MHz design goal to 18MHz. This slightly worsens the attenuation of limit cycle intermodulation tones which appear at the upper edge of the band but the measured impact on MTPR is negligible.

As discussed in Section 6.5.4, the resistor and capacitor process variation can be compensated for by adjusting the current buffer gain, which in this implementation means adding programmability to the device M2 or M7 of the current buffer cell shown in Figure 6.17. Unfortunately, due to time constraints, this programmability was not included in this implementation.

Figure 6.27 shows a short MTPR signal injecting 22mW with a worst-case MTPR of 24dB. Unfortunately, various circuit-level imperfections degraded performance particularly at the upper edge of the band so the injected power was reduced to compensate. This will be discussed further in the Post-layout simulation section, next.

The NTF zero is visible at approximately 18MHz, as discussed above, and this is due to parasitic poles introduced into the L_1 loop by the integrator and source follower buffers. The heavily attenuated self-oscillation frequency fundamental component can be seen

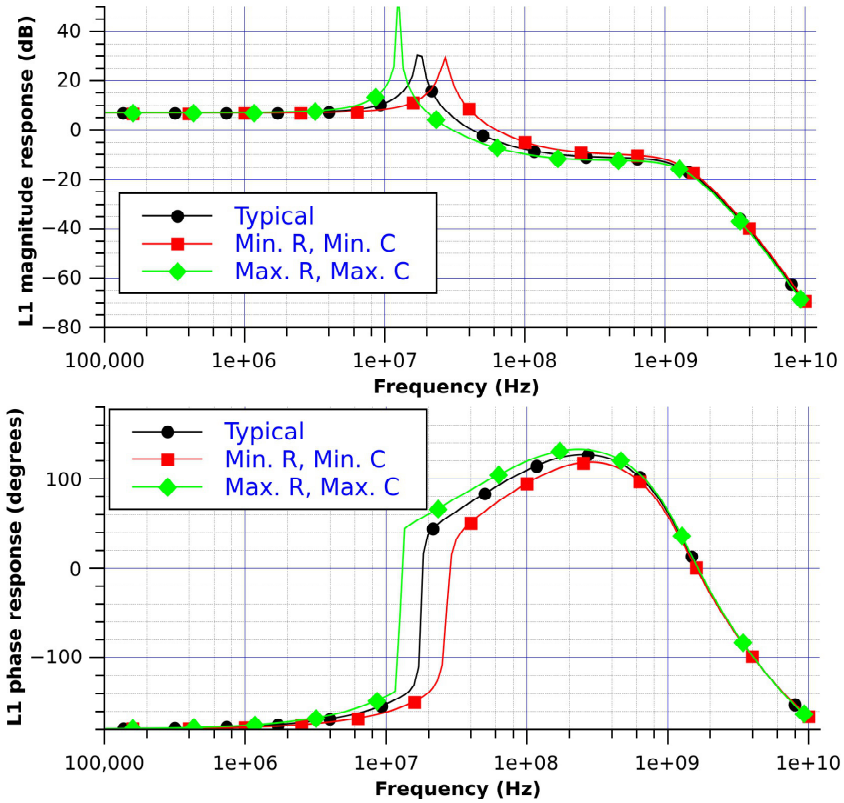

Figure 6.26: Pre-layout AC simulation of the L_1 loop filter, with minimum, typical and maximum values of resistors and capacitors.

at around 115MHz.

The self-oscillating frequency is an important design parameter, yet it is not precisely set - it depends on process, temperature and supply voltage. To quantify the effect, pre-layout schematic simulations were used. The Verilog-A module discussed in Section 6.5.2, which adjusts the programmable delay cell to achieve a desired oscillation frequency is disabled for these tests. Then, the frequency of oscillation in the typical case was measured; typical values for resistors and capacitors in the process, an 3.3V supply voltage and a 90° Celcius operating temperature. In this case, the self-oscillation frequency is measured as 111MHz.

Next, each parameter was varied throughout its expected range; resistors and capacitors include process models which can vary chosen to set the values to a minimum or to a maximum. The supply voltage can vary, in a commercial application, by ±10%, and the design temperature range is -40° Celcius to 125° Celcius. The results are shown in Table 6.11. It is observed that temperature and resistor changes primarily dominate the variation in self-oscillation frequency.

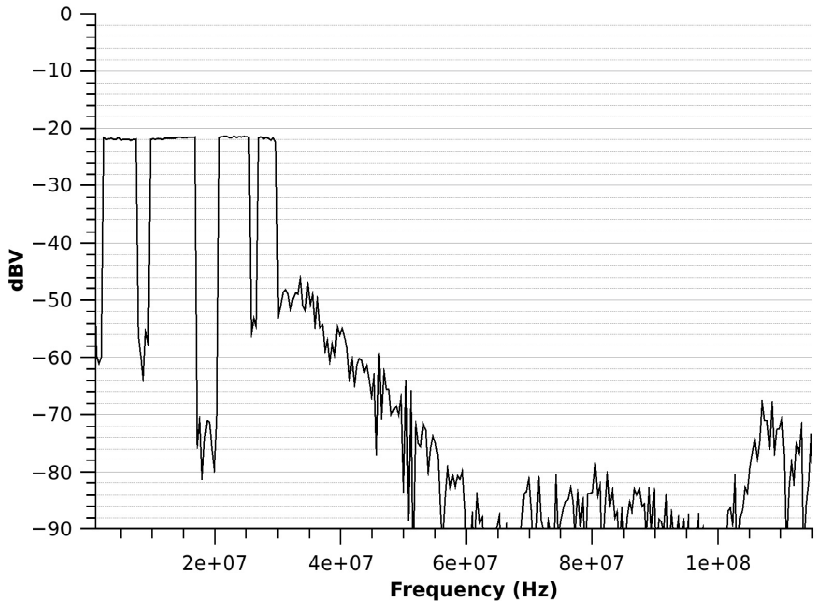

Figure 6.27: Pre-layout simulation of line driver transmitting a short MTPR symbol, injecting 22mW into a load.

Table 6.11: Impact of process/temperature/supply variations on self-oscillation frequency.

	Resistor		Capacitor		Supply		Temperature	
	Min.	Max.	Min.	Max.	2.97V	3.63V	-40°C	125°C
Frequency (MHz)	90	122	110	111	105	116	150	100
Variation (%)	-19	+10	-1	0	-5	+5	35	-10

6.7.2 Post-layout simulation

Post-layout simulation was carried out by extracting the device parasitics, parasitic routing resistance, and parasitic capacitance, from the full chip layout and then simulating it. While a small number of full-chip extracted simulations were performed, the simulation runtime was approximately one month for an extracted simulation of the full line driver with a short MTPR symbol, using the multi-threaded Cadence Spectre/APS simulator on a high-performance multi-CPU machine, and so for the majority of extracted simulations, an accurate but faster simulation methodology is required.

6.7.2.1 Extracted-model simulation strategy

There are two factors which affect simulation performance:

1. The number of time points the simulator needs to solve.
2. The number of nodes in the design that must be solved.

To improve simulation performance, either fewer time points must be solved, or the number of nodes/components that must be solved at each time point must be reduced.

The number of simulator time points is usually a function of the error tolerances in the simulator, which determines the accuracy of the final simulated MTPR result, but regardless, the options for altering the number of time steps the simulator takes is limited. More significantly, the impact of the number of time points on simulation run time is usually linear, while the impact of the number of nodes on simulation run time is exponential. For all of these reasons, to reduce simulation run time significantly, particularly when simulating extracted layout which contains many nodes, the number of nodes in a design must be minimized, but this must be done without removing nodes which significantly affect the simulation accuracy. To give some context to the problem, the line driver developed here contains 950k nodes when extracted (including parasitic capacitance and resistance), but the corresponding schematic contains only 1700 nodes.

In the extracted-model simulation methodology used here, the design is broken into a number of functional blocks:

- Loop filter
- Comparator
- Non-overlap circuit
- Output driver and tapered buffer

Each functional block is extracted twice, once including MOSFET parameters and parasitic capacitance – which is described as "C+CC extraction" – and a second time where the parasitic resistance is also included – and is called a "R+C+CC extraction". Parasitic resistance fragments nets in a design at each wire junction in the circuit layout, and is the main reason behind the increase in number of nets in an extracted design.

Each functional block is then simulated with both the C+CC and R+C+CC extracted views, and the performance and simulation run time impact of each extracted view is compared to the schematic. The performance comparison metric depends on the block - the loop filter is compared in terms of its AC performance, while the comparator,

non-overlap circuit and output driver are all compared using their output signal in a transient simulation including rise/fall times, DC level at beginning/end of a signal transition, and delay.

If the R+C+CC views give similar performance to C+CC views, it is ignored and the C+CC view is used to create an extracted model, else the R+C+CC view is used to create an extracted model.

An "extracted model" is a copy of the drawn (not extracted) schematic, but with modifications to reduce simulation time and to better match the output of the extracted view when the extracted and extracted-model views are simulated with the same input. Additionally, unless the effect of input/output loading is not significant, the input loading and output drive capability is kept the same as in the schematic so that schematics or extracted models can be switched in for a particular cell without introducing errors due to improper loading.

6.7.2.2 Extracted model development

While the development of the extracted model is necessary in order to improve simulation performance, it serves a dual purpose as it identifies the discrepancies – and in some cases, the causes of differences – between the designed schematic and what has been implemented after layout.

The final extracted model modifications used are:

- Loop filter: Simulation time is similar across schematic, C+CC and R+C+CC views so no extracted model was created and either the schematic or extracted views were used as appropriate.
- Comparator: Insert parasitic output capacitance of 200fF and add an ideal delay to the comparator inputs of 75ps to match the C+CC extracted view.
- Non-overlap circuit: Insert delay to increase minimum non-overlap time from 100ps to 430ps. Remove the programmable delay blocks used after the non-overlap circuit and replace with an input schematic inverter, ideal delay block with 430ps delay, and an output schematic inverter. The input and output schematic inverters match the first and last cells inside the programmable delay block. Result matches the C+CC extracted view.
- Output driver: The tapered buffer was removed apart from the first stage and was replaced by an ideal buffer with output resistance determined from the R+C+CC simulation. The ideal buffer drives the real output devices but the hierarchy is flattened, and series resistance of 0.4Ω is inserted into both the pull-up and

pull-down output paths. This0.4 Ω is split into 0.2Ω attached to the drain of the output device and another 0.2Ω attached to the source of the output device. The final output driver extracted model is shown in Figure 6.28.

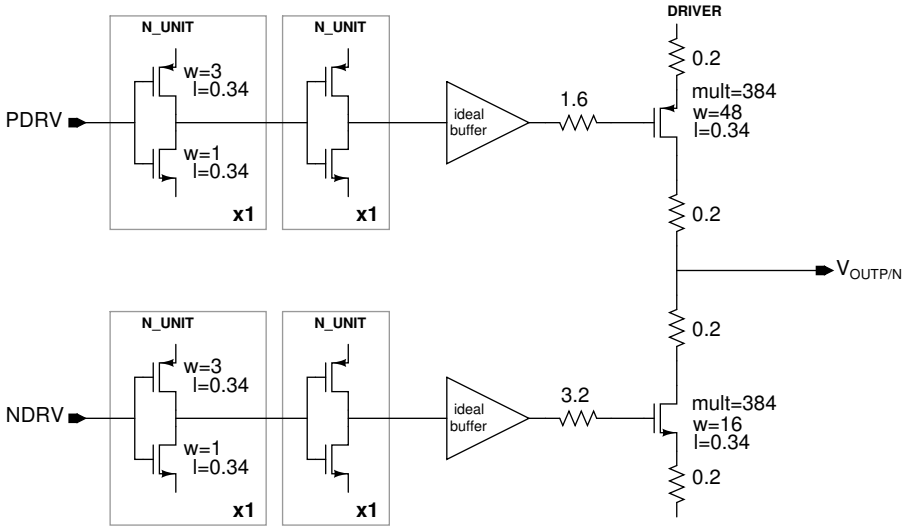

Figure 6.28: Extracted model of the output driver. This should be compared to the original output driver schematic in Figure 6.7.

By going through this process, a number of layout parasitic effects have been identified:

- Comparator load capacitance is 200fF larger than expected.
- Non-overlap circuit delay is 330ps longer than the 100ps delay which is needed for the extracted model to match the schematic.
- Output driver contains significant parasitic resistance which is not seen in a C+CC extracted view. This additional resistance, approximately 0.4Ω in both pull-up and pull-down paths, is twice the designed 0.2Ω value, and so the total resistance of the output driver (including output device on-resistance) is three times the value required to inject maximum power.

Unfortunately, there was insufficient time before manufacture of the this design to address these issues. Their impact will be quantified in the following sections.

6.7.2.3 Accuracy of extracted model

While the following section will present a more in-depth study of simulation results and areas of degradation, it is appropriate to include two data points here to illustrate the accuracy of the extracted model. Table 6.12 compares the number of components, number of time points, simulation time, and linearity performance. Simulation time is the CPU time required for the Cadence Spectre/APS simulation to simulate the netlist,

but as this is a multi-threaded simulator, it can parallelise work across multiple CPU's in order to reduce the elapsed simulation time, between starting the simulation and the results becoming available.

Table 6.12: Comparison of results from R+C+CC extracted simulation versus results from extracted model simulation.

Parameter	R+C+CC	Extracted model
Nodes in circuit	950,000	1800
Transistors in circuit	30,000	11,000
Capacitors in circuit	550,000	1024
Resistors in circuit	1,200,000	41
Simulator timesteps	600,000	400,000
Simulation time	105 days	25 minutes
Elapsed simulation time	35 days	9 minutes
MTPR (0-20MHz)	30dB	30dB
MTPR (30-35MHz)	14dB	16dB

The linearity is given using two metrics, the worst-case MTPR within the 0-20MHz band and the worst-case MTPR within the 30-35MHz band. These metrics were chosen as they provide a quick way of comparing the relative performance of particular simulation while providing the ability to distinguish between the two main distortion mechanisms; in-band intermodulation distortion, which is dominant at lower frequencies; and intrusion of limitcycle intermodulation harmonics into the signal band, which dominants at the upper edge of the band, at approximately 30MHz.

The MTPR results in Table 6.12 show that the extracted model closely matches the performance of the R+C+CC model, with a significant simulation time reduction.

6.7.3 Toplevel simulation

As discussed above, a simulation of the post-layout R+C+CC line driver was performed. The output spectrum as measured across the load resistor is shown in Figure 6.29. The power dissipated in the load was measured as 32mW, the degradation versus the ideal 56mW being due to the parasitic resistance in series with the output driver.

While the low frequency MTPR at less than 10MHz reaches approximately 40dB, the MTPR in the band 0-20MHz is 30dB and in 30-35MHz region, the MTPR is only 14dB.

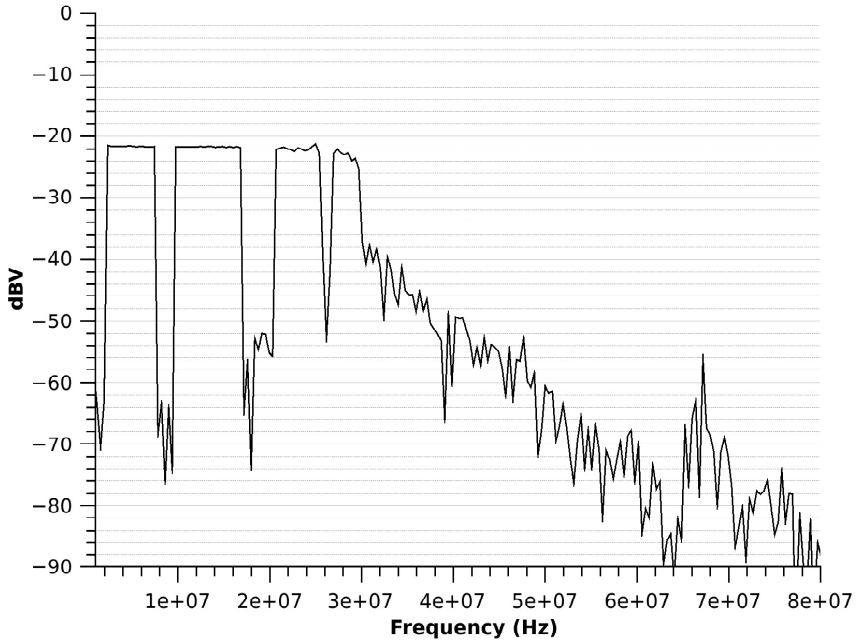

Figure 6.29: Post-layout simulation of short DMT symbol.

To identify the cause of the problem, it is useful to idealise various parts of the circuit and examine the degradations due to the non-idealities discussed in Section 6.7.2.2, one at a time.

To begin, a best-case simulation testbench was created, where the loop filter and comparator were replaced by ideal mathematical models implemented in the Verilog-A language, and the non-overlap circuit and output driver were implemented using their schematic views. In this case, the MTPR was 46dB/41dB – where the first figure refers to the 0-20MHz performance and the second figure refers to the 30-35MHz performance – and the self-oscillation frequency was 100MHz.

From this reference circuit, three independent trials were made, to investigate the impact of layout imperfections in the switched-circuitry in the loop: the comparator, non-overlap circuit, programmable delay block and output driver. The trials were:

1. Replace the non-overlap circuit was replaced with its extracted model – which has a minimum non-overlap delay time of 430ps versus 100ps for the schematic. The line driver MTPR decreased to 45dB/37dB and self-oscillation frequency dropped to 98MHz.
2. Replace the delay block after the non-overlap circuit with its extracted model – which has an input-output delay of 430ps versus the 100ps for the schematic. The MTPR decreased to 42dB/28dB and the self-oscillating frequency drops to 89MHz.
3. Replace the output driver with its extracted model, which has an additional 0.4Ω

of output resistance. The MTPR decreased to 39dB/35dB and the self-oscillation frequency stayed at 100MHz.

4. Replace the comparator with its extracted model, which has additional output capacitance and delay. The MTPR and limit cycle frequency change was negligible.

A final simulation was performed with extracted-model implementations for all of: non-overlap circuit; delay block; output driver; comparator. The measured MTPR was 39dB/23dB and the limit cycle frequency was 90MHz. If the distortion contributions from the independent trials above are assumed to be uncorrelated, then they can be added in quadrature to estimate their combined effect analytically, and then compared to the simulated value. This analytical computation of the combined impact of the independent trials above results in an MTPR of 37dB/27dB which, while not a perfect match for the full extracted-model simulation, is close. This suggests that the 0-20MHz linearity is limited to 37dB approximately equally by the layout imperfections of the non-overlap circuit, delay cell, and output driver. Also, the 30-35MHz MTPR is limited mainly by the delay cell layout, and in particular by the effect of the additional delay on the self-oscillating frequency of the loop.

Next, the effect of the loop filter was examined. Starting from the reference circuit above, the loop filter was changed to use a schematic implementation rather than Verilog-A. In this case, the MTPR drops to 32dB/26dB and the limit cycle frequency increases slightly to 105MHz. If the other blocks in the line driver (non-overlap, delay-block, output driver, comparator) are implemented using extracted-model views, the top level linedriver MTPR is 30dB/16dB and the self-oscillating frequency is 91MHz. This closely matches the performance of the toplevel R+C+CC simulation.

The MTPR degradation ovserved when using a schematic loop filter implementation was found to be caused by the addition of capacitor C_z in the loop filter, as shown in Figure 6.15, which introduces a zero in the L_1 transfer function. This zero was inserted late in the design in order to compensate for higher than expected phase shift in the L_1 loop due to integrator non-dominant poles and parasitic delay-block delay, both of which lower the self-oscillation frequency. While the AC impact of this zero on the NTF and STF is negligible within the signal band, the short rise/fall times seen at the output of the line driver, on the order of 300ps, mean that a current of 550uA should flow through the capacitor at each input edge. This uses C_z=50fF as defined in Table 6.9, an output driver voltage change ΔV_{out}=3.3V, and Equation 6.38.

$$I_{C_z} = \frac{C_z \, \Delta V_{out}}{t_{rise/fall}} \tag{6.38}$$

C_z is connected to the input of the second integrator in the loop filter, but as this

has an input bias current of 400uA, the second integrator is being overloaded by the transient current spikes after each switching edge. To confirm this, the loop filter current buffers were first replaced with ideal current buffers and performance improved to 36dB/23dB – matching the performance above for an ideal Verilog-A loop filter with extracted-model implementation of the non-overlap cell, delay cell, output driver and comparator. However, adding an output current limit to the ideal current buffers reduces the performance to 27dB/15dB.

This is an unfortunate flaw in the design and while it was discovered prior to IC fabrication, there was insufficient time to make any changes.

So far, only the pre-layout loop filter schematic has been considered. Figure 6.30 shows the L_1 transfer function measured in an AC simulation of the loop filter R+C+CC extraction. By comparison to the pre-layout results in Figure 6.26, it is observed that the NTF zero (L_1 peak) has dropped to 12MHz. It is notable that this does not significantly affect the linearity – toplevel R+C+CC results are similar to those with a schematic loop filter with other blocks using extracted-model implementations. However, it does affect the self-oscillating frequency, which drops to 67MHz in the R+C+CC toplevel extracted simulation, versus 91dB with the schematic loop filter.

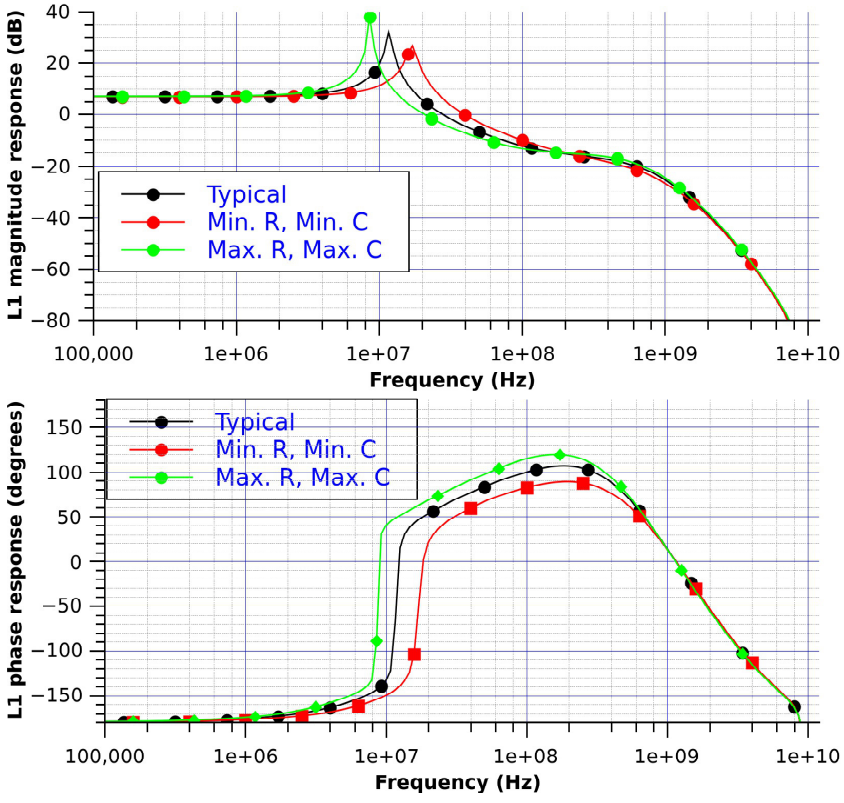

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Figure 6.30: Post-layout AC simulation of the L_1 loop filter, with minimum, typical and maximum values of resistors and capacitors.

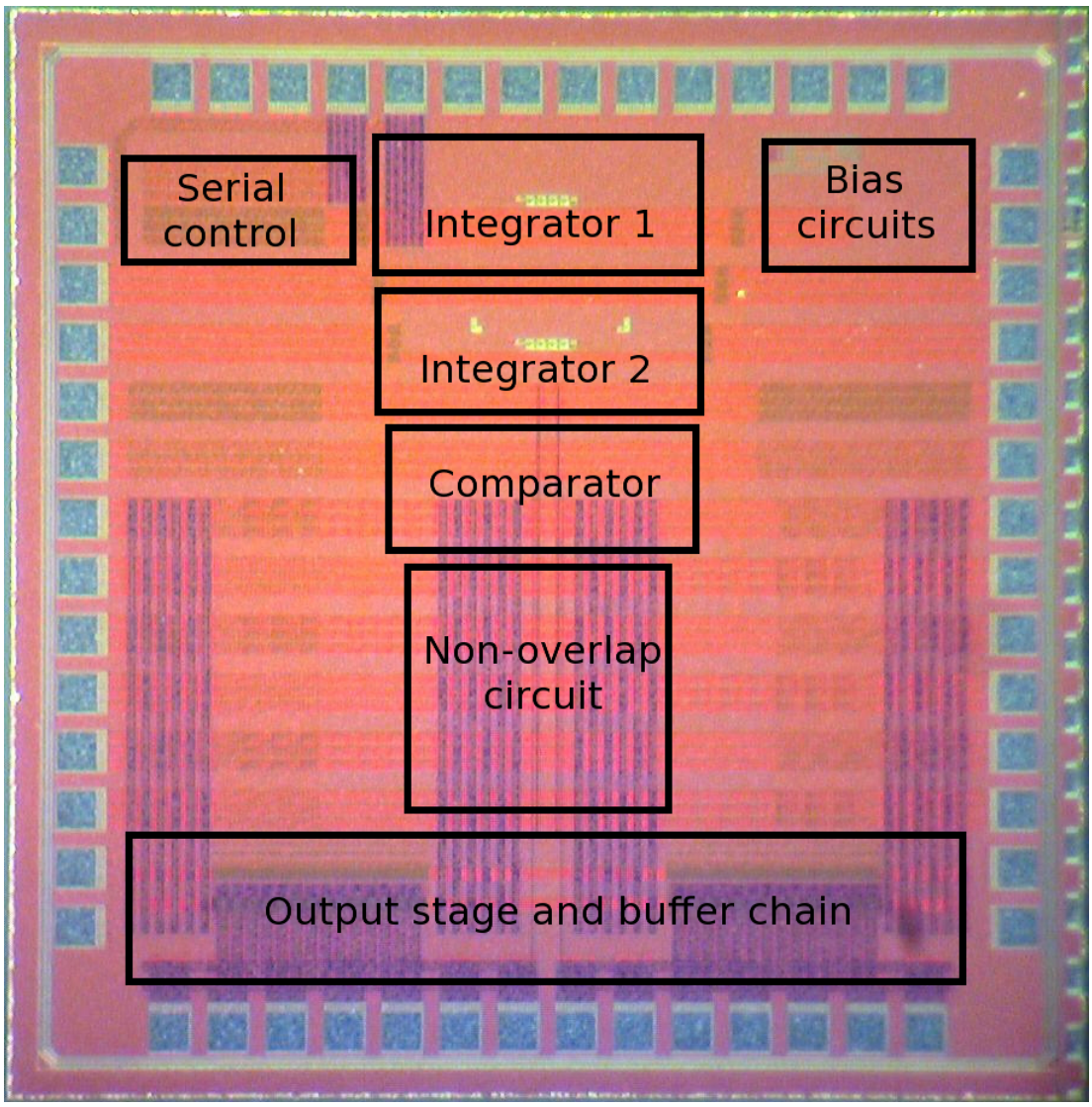

Figure 6.31: Micro-photograph of the manufactured line driver test chip.

6.8 Fabrication and Packaging

The design was fabricated in a 0.13μm CMOS process from UMC, through Europractice. The completed chip micro-photograph is shown in Figure 6.31. The die measures 1.5 mm $\times$ 1.5 mm. Due to the large number of metal layers (8) in this process, it is not possible to see transistor detail at the bottom of the metal stack and so the position of circuit elements has been annotated in the figure.

The top two metal layers, Metal 8 (running vertically) and Metal 7 (running horizontally) are visible in the figure. These are thick metal layers with high current capacity, and are used extensively around the output stage in order to provide enough metal routing to minimise routing resistance and to comply with maximum current density design rules.

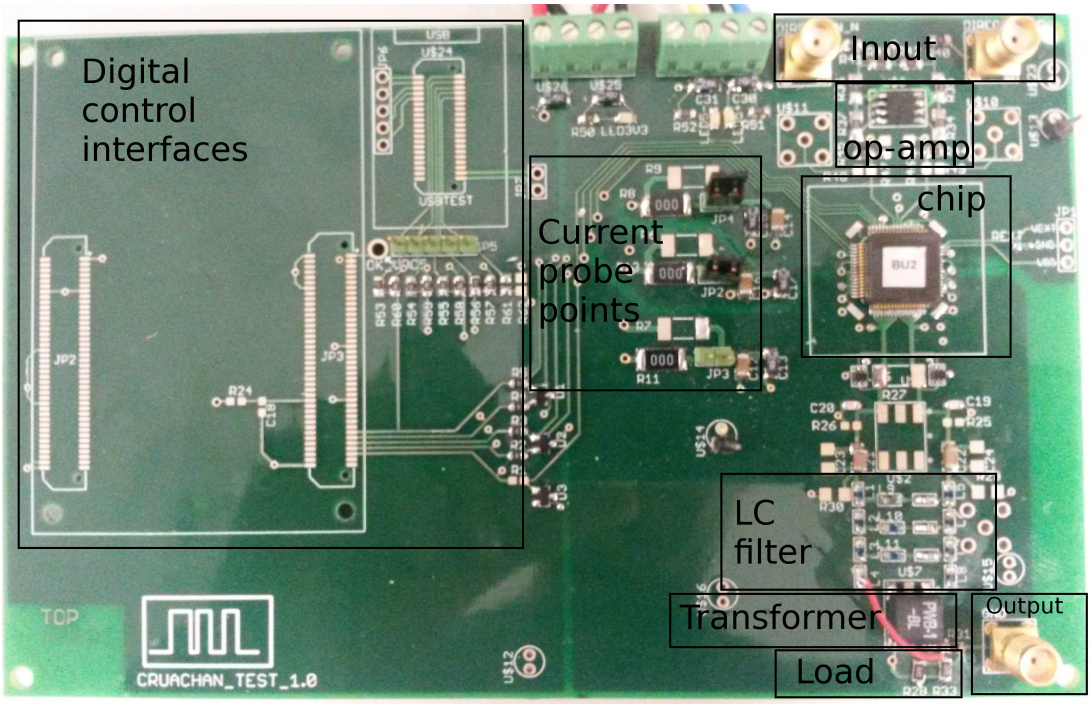

Figure 6.32: PCB used for testing the chip.

The die was attached to a 64-pin ceramic quad flat pack package and bonded using 25 μm (diameter) gold bondwires.

6.9 Measurement setup

6.9.1 Hardware

A Printed Circuit Board (PCB) was created to interface the manufactured chip with the various inputs and outputs required to power it and test it. The test board, shown in Figure 6.32, is a four layer FR4 PCB. Layer 1, the top layer, is used for signal routing; layer 2 is for supply routing; layer 3 is a ground plane and layer 4 is for signal routing and for adding decoupling capacitors close to the chip supply pins. The transformer used on the board is a Coilcraft PWB-1-BL, which has a 1:1 ratio. This was used instead of a 1:4 ratio transformer discussed in Section 6.3 as the available 1:4 transformer suffered from roll-off of up-to 5dB across the band due to transformer parasitics. It is expected that in a commercial application, a custom wound transformer with improved high frequency performance could be obtained. However, for this work, a 1:1 transformer was used instead and the load impedance was reduced by a factor 4^2.

Various items of external hardware are required to drive/measure the chip. The DMT

input signal is generated by an Agilent M8190 Arbitrary Waveform Generator (AWG), which provides a highly linear differential output signal with a 0V – 0.7V maximum swing when connected to a 50Ω load. The AWG outputs are connected to the SMA headers on the PCB labelled "Input", and these connect to an Analog Devices AD8138 high speed, wide bandwidth op-amp. This op-amp is configured to terminate the AWG inputs by presenting a 50Ω input impedance, while giving a signal gain of 4.4 in order to provide up-to a 3.08V input swing for the line driver test chip. This large swing would be lossy if the line driver was implemented as a discrete chip, due to the need to drive the large pad capacitances, but in the application here where the line driver is integrated on the same die as the DSP and DAC, the interface between DAC and line driver is internal to the chip, it is much more practical to support a large swing.

Time domain measurements are performed using an Agilent Infinium DSA90604A Digital Signal Analyzer (DSA), which is connected with a high-impedance single-ended probe to the output of the transformer.

Frequency domain measurements are performed using a Agilent MXA N9020A Spectrum Analyzer. It has a 50Ω input which is attached to the "Output" SMA on the PCB. Note that this impedance appears in parallel with the load impedance on the board. This has been accounted for when determining the actual load impedance that the line driver test chip must drive.

Current measurements are performed using an Agilent 34410A Digital Multimeter (DMM), either in series with the PCB power cables, or using one of the supply current measurement points which are in series with the three main supply domains; analogue supply, non-overlap generator supply and output stage supply.

Finally, digital control of the line driver test chip is provided by a custom-built USB-serial device based on a FTDI-2232D[119] chip.

6.9.2 Software

6.9.2.1 General

A Python-based automated measurement suite has been developed to assist with performance characterisation. This consists of the following components:

- DMT symbol generation
- Programming interface for driving the test chip digital interface, using the FTDI-2232D in bit-bang mode

- Automated MTPR measurement using the Spectrum Analyzer

Python libraries to remotely control the Spectrum Analyzer, DSA, DMM and AWG from Python scripts were made available by Broadcom Europe.

This software environment allows a test to be defined in a test script which can configure the line driver test chip and perform all measurements automatically.

6.9.2.2 MTPR measurement

The Automated MTPR measurement code has been designed to work with a signal with non-constant amplitude across the band. The variable frequency response of a powerline means that the injected power may vary with frequency, so it is important to be able to cope with these in MTPR measurement. Even when performing measurements while driving carefully controlled load impedances, non-ideal effects such as transformer or filter roll-off mean that the power of each carrier is unlikely to be the same.

To accurately compute MTPR, each notched carrier is considered independently. The power at the notched carrier frequency is measured, and then the power of the 10 nearest used carriers above and below the notched carrier are also measured. The linear carrier power is averaged and the ratio between the average carrier power and the notch power is used to define the MTPR for that notched carrier. The worst-case, pc90 and pc50 values, as described in Section 2.6.2, can now be obtained.

All measurements use a spectrum analyzer resolution bandwidth of 300Hz.

6.10 Conclusion

The requirements that the HomePlug AV standard places on the line driver have been analyzed and line driver specifications have been determined, and application-level design decisions discussed. The basic Class-D self-oscillating structure was presented in Chapter 5, and this chapter takes the basic structure then investigates the implications of different loop filter transfer functions. Once a suitable loop filter transfer function exists, the circuit level design and layout of the line driver is presented, starting from the line driver output devices and working backwards towards the loop filter and then covering all the required supporting circuitry.

A new wide-band integrator structure is presented and compared to more conventional integrators, highlighting the wide bandwidth and good linearity in the presence of a

large input signal, of the new structure. A detailed analysis of the small-signal operation of the integrator structure is presented, and simple design equations are derived.

Simulation results are presented from both before after layout – that is, without and with the parasitic resistors and capacitors that are present in the physical circuit structure. The methodology used to achieve time-efficient simulation of a complex non-linear block while accounting for the effects of layout parasitics is discussed and during this process, the performance limitations present in the schematic design and in the physical layout are established. The bench hardware and software measurement setup is then presented.

While preparing for design fabrication, a number of additional parasitic resistances and capacitances were identified which degrade the performance of the overall line driver. Additionally, a flaw in the implementation of the loop filter was discovered which degrades performance further. Unfortunately there was not sufficient time to correct these issues before the design was fabricated. Although these issues make it unlikely that the implemented line driver will achieve the highest power and widest bandwidth permitted by the HPAV standard, lower powers and narrower bandwidths can be used to prove whether the line driver is fundamentally more efficient that other approaches.

Chapter 7

Results

7.1 Introduction

Previous chapters have established the motivation behind using Class-D for wide band line drivers, and have provided design theory and detailed discussion of the process by which a prototype Class-D line driver was created, fabricated and how it can be tested. The goal of this chapter is to first present and discuss details of a measured waveform, to understand the performance degradations and how they relate to simulated results. Next, measurement results from the chip in a number of power/bandwidth configurations are presented, as there are different linearity and efficiency trade-offs in the different configurations. Afterwards, the performance of the chip will be summarised and compared with what other line driver architectures have achieved. Finally, conclusions will be drawn regarding the suitability and effectiveness of the prototype architecture for the intended application.

7.2 Initial results

Figure 7.1 shows a typical output from the line driver. This signal is measured by the Spectrum Analyzer connected to the Output SMA measurement point on the test PCB. The signal swing is 680 mV_{RMS} as measured using the Digital Signal Analyzer and a single ended probe connected across the load resistor on the PCB. The load is 13.3Ω so the power injected into the load is 33mW.

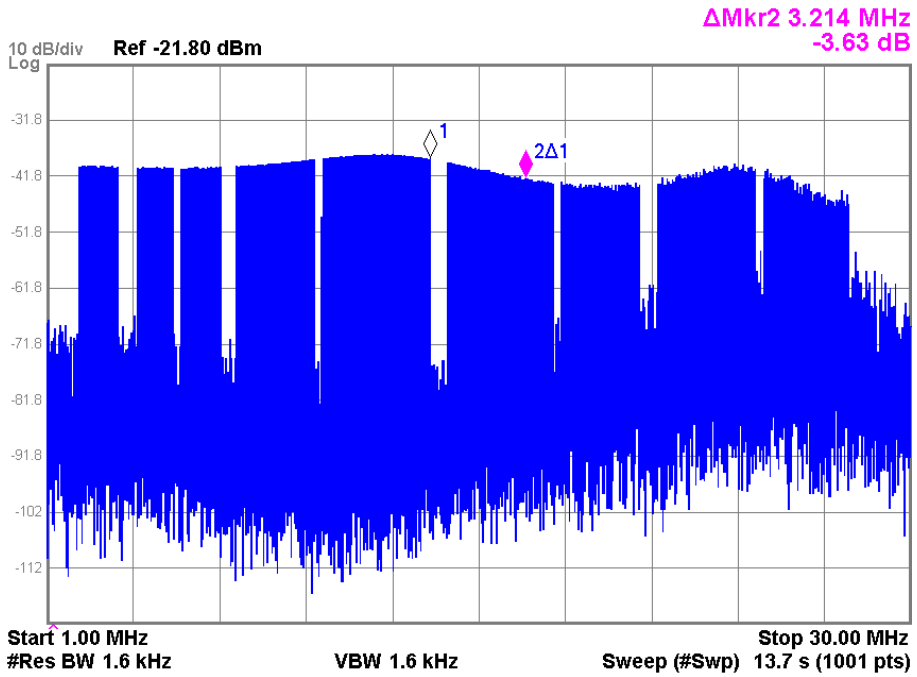

Figure 7.1: Output HPAV test signal.

7.2.1 Oscillation frequency

The oscillation frequency is 57MHz. This is far off the designed value of 100MHz, and lower even than the 67MHz value obtained from post-layout simulations including layout parasitics, suggesting that the test chip used comes from a slow lot or that there is some effect not modelled by the simulation test bench or by the extraction tool which accounts for this difference.

7.2.2 Linearity

The spectrum shown in Figure 7.1 shows a ripple of up to 5dB across the signal band. This is due to the LC output filter and requires careful matching of the load impedance to the filter impedance, and fine tuning of filter component values to account for parasitic inductances, capacitances and resistances on the PCB to eliminate. Some initial work was carried out to improve the ripple but there was insufficient time to further debug the issue. It does not significantly affect the measurements as both signal and distortion experience the ripple and it is the ratio of the two – which is independent of the ripple – which is of most interest in terms of MTPR.

Using the MTPR analysis script, the following MTPR values are obtained:

- pc50: 32.4 dB

- pc90: 22 dB
- worst case: 10.9dB

This MTPR result show that at least half of the carriers have a reasonable (above 30dB) SNR, but there are a bottom 10 percent which are very bad, below 22dB.

This result is similar to the extracted simulation result shown in Figure 6.29, and a combination of saturation of the second integrator at each of the Class-D output edges, and also the additional parasitic delay introduced by the delay cell. Section 6.7.3.

related to the reduced self-oscillating frequency causing modulation tones to fall into the upper half of the signal band, as per Equation 5.18. To improve performance, the frequency separation between the oscillation frequency and the signal band should be increased, as described in Equation 5.20.

7.2.3 Power consumption

The total power supply consumption of the test board is 88mA while the chip is transmitting, but with the line driver powered down, the test board still consumes 18mA. This 18mA is mainly due to devices on the test PCB, but also includes 2.5mA consumed by the on-chip bandgap, which is always on. This 18mA is calibrated out of all measurements in order to get a fair power estimate of the line driver itself. As such, the power consumption of the line driver is 88mA - 18mA = 70mA, from a 3.3V supply. The efficiency is thus 35mW/231mW, or 15%.

The supply current consumption of the three separate supply domains can be measured separately in order to coarsely determine which blocks are consuming the current. The result of this is:

- Analogue supply: 13.8mA, used for all analogue circuitry in the test chip (loop filter, buffers, comparator, biasing, references). This includes 2.5mA for the bandgap and should not be included when determining line driver efficiency.
- Non-overlap clock generator supply: 2.6mA
- Output stage and driver supply: 54mA. This supplies the output buffers and output stage, which includes the load current.

The load current is approximately 11mA, so the output buffers and output stage consume 43mA quiescent current. The efficiency for a given load current can thus be estimated

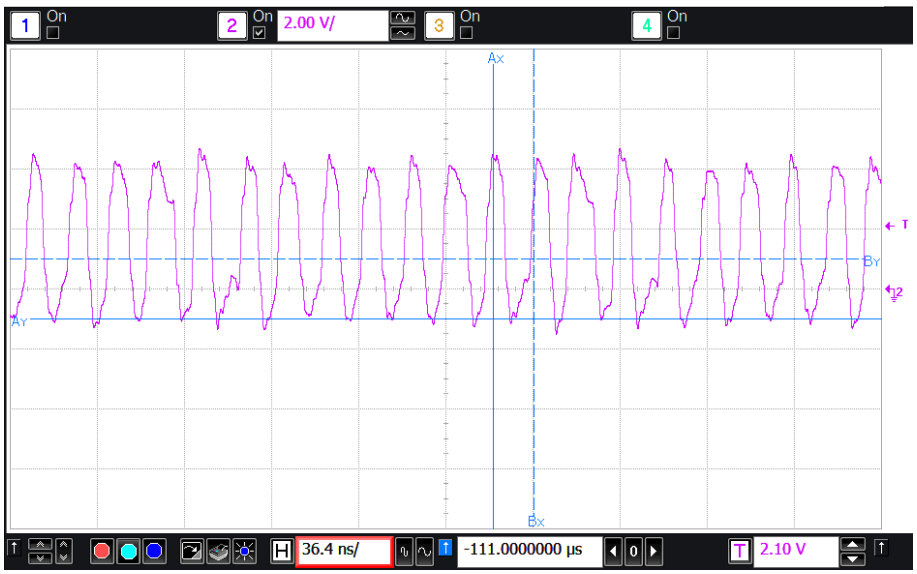

Figure 7.2: Positive output of line driver test chip at pin of package, prior to LC filter, while line driver is driving a DMT signal.

with Equation 7.1. This has been confirmed with measurements.

$$\text{Efficiency}_{(\text{estimate})} = \frac{\text{I}_{\text{load}}}{I_{\text{load}} + 57\text{mA}} \tag{7.1}$$

7.2.4 Time domain characteristics

The unfiltered PWM output of the chip while driving a DMT signal can be seen by probing the chip output pin with the Digital Signal Analyzer, and this trace is shown in Figure 7.2. The waveform is far from the ideal square pulse wave and there are three obvious degradations from the ideal.

- The rise/fall time of the pulse edges is approximately 500ps. This corresponds well with the post-layout simulations (400ps) and is one of the smaller contributors to the waveform nonideality.
- The high and low periods of the pulse waveform can be seen to be ramping up or down. This is normal operation for a Class-D amplifier, as discussed in Section 5.18. After the Class-D output stage changes state from positive to negative, or vice-versa, the LC filter will start integrating the negative input and so will reduce its input current. The current forced by the LC filter flows through the output resistance of the Class-D driver and so generates a voltage $\text{V}_{\text{on}}=\text{I}_{\text{load}}\text{R}_{\text{out}}$ at the line driver output. As the LC filter current changes, so does this voltage V_{on}. Note that the additional 0.4Ω parasitic resistance present in the output stage, discussed in Section 6.5.1, significantly increases the size of this ripple.

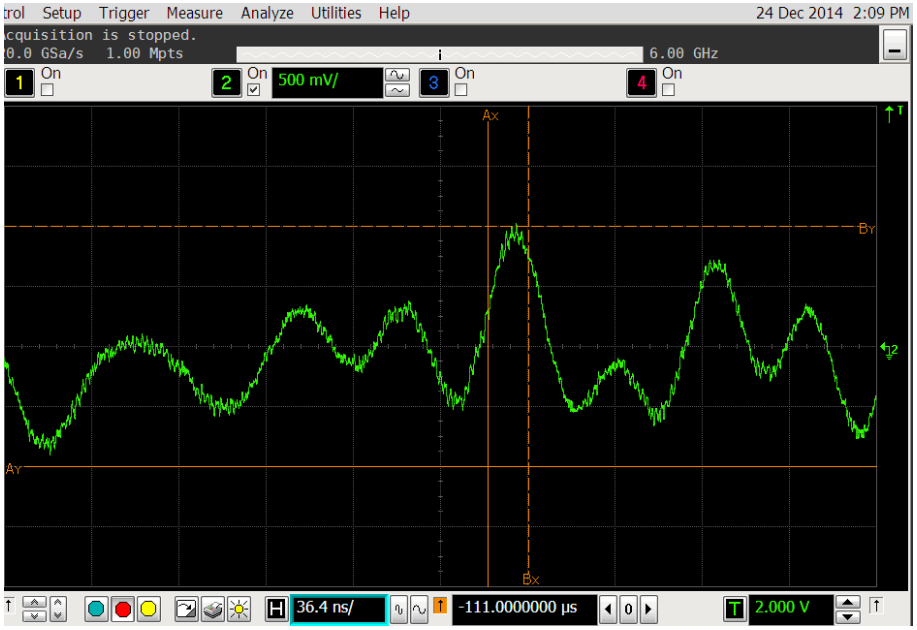

Figure 7.3: Output of the line driver test chip after the Elliptic output filter.

- Bondwire ringing, due to the L-C network created by the bondwire inductance and the on-chip/on-PCB parasitic capacitance occurs after the output stage completes each rise/fall transition.

These are the three most obvious errors in the output pulse signal. They alter the output harmonic content around the self-oscillating frequency such that it is no longer accurately described by Equation 5.18, although the equation is still useful as a guide.

The filtered PWM output is shown in Figure 7.3. This is a close up of the DMT signal and is similar to what is shown in the enlarged section of Figure 2.12. The time-domain impact of the raised intermodulation harmonics is visible as a time-domain noise added to the DMT signal.

7.3 Design characterisation

It is useful to understand how the line driver performs with slightly different configurations of swing and signal bandwidth. If there is, for example, a large linearity improvement with a -1dB signal change, this might be an overall benefit for system SNR.

An automated measurement script was written to measure the Class-D line driver performance over a range of output swings and signal bandwidths. The swings were varied from 7.5dB below full-scale to full-scale, while the signal bandwidth was varied in

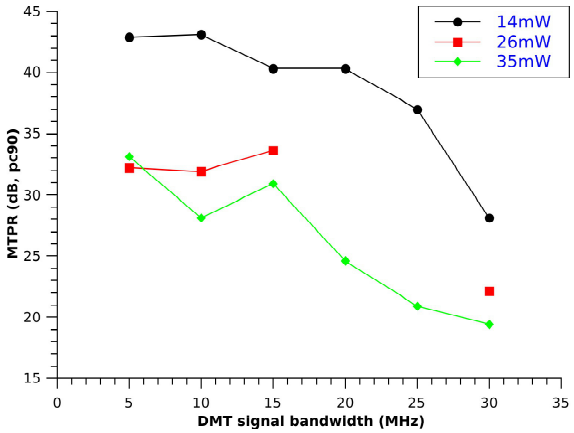

Figure 7.4: MTPR (pc90) versus DMT signal bandwidth, three levels of injected power; low (14mW); medium (26mW); and high (35mW). The data for two points on the 26mW line are not available due to a problem with the automated measurement interface on the spectrum analyzer, so those points are left blank in the graph.

steps of 5MHz up to 30MHz. Varying the signal bandwidth entails generating new test data for the line driver input, which use carriers only going up to a specified frequency. Note that the load resistor and LC filter are kept constant for this test.

The power supply current, RMS and peak-peak output swings, and the MTPR values (pc50, pc90, pc97 and worst-case) are measured for each swing and bandwidth combination. The MTPR is measured up the to maximum signal carrier plus 10 carriers. From this information, the line driver efficiency can be calculated.

The raw characterisation result tables are included in Appendix B.

A plot of the line driver performance for a range of signal bandwidths and selected powers (swing) is shown in Figure 7.4. In all cases, reducing signal bandwidth from 30MHz to 15MHz gives a large improvement in MTPR but further reducing the signal bandwidth does not further improve the MTPR. This “knee” suggests two distortion mechanisms are present in the system, one limiting below 15MHz and another limiting above 15MHz. The low frequency limit is likely to be related to third harmonic distortion from the modulation scheme and from component non-idealities, while the high frequency limit is, from Figure 7.1, likely to be due to modulation components falling in band. If the self-oscillating frequency were to be increased, it is expected that the knee on the curves would also move up in frequency.

The same Figure 7.4 also shows the linearity improvements that come with reducing the signal amplitude/injected power. In Figure 7.5, the impact of reducing swing on efficiency can be seen. As described in Equation 7.1 above, line driver quiescent power consumption is roughly flat and so efficiency varies proportionally to the injected power.

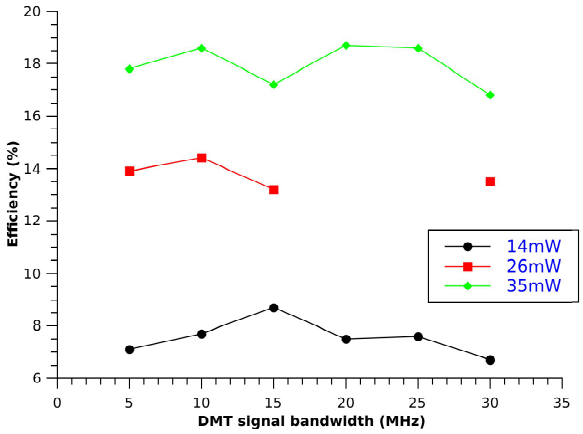

Figure 7.5: Efficiency versus DMT signal bandwidth, three levels of injected power; low (14mW); medium (26mW); and high (35mW). As per Figure 7.4, the data for two points on the 26mW line are not available due to a problem with the automated measurement interface on the spectrum analyzer, so those points are left blank in the graph.

7.4 Performance comparison

The line driver developed in the previous two chapters will now be compared with similar works published in the last fifteen years, which represent the state-of-art.

Figures 7.6 and Figure 7.7 compare the performance of the line driver presented here, against a number of the references referred to in Section 2.2, according to their efficiency, linearity and bandwidth. Black dots with a square brackets refer to a particular publication, while the black dot labelled "This work" refers to the performance presented here for the 30MHz HomePlug AV application. The line driver presented here was measured with various other signal bandwidth and injected power combinations, and a selection of these data points – from Appendix B – are included as black dots with two numbers in brackets to their side. These numbers represent a signal bandwidth (in MegaHertz) and an injected power. Including all of the data points from Appendix B clutters the graph, so instead the remaining data points are shown as red "plus" symbols with no bandwidth/power annotated. The overall performance space – the approximate extent of the red "plus" symbols – is shaded red.

Figure 7.6 shows the linearity of the line drivers as a function of line driver signal bandwidth. There is an obvious divide between line drivers based on linear techniques (Classes AB/G/H) and those using non-linear Class-D techniques, with the former achieving higher linearities than the latter. Within the linear classes, the widest bandwidth structure uses a Class AB architecture whereas those based on G/H structures are much lower bandwidth. This is in part due to the increased complexity of managing

supply rail switching/modulation at higher frequencies, and so wide bandwidth line drivers generally favour the simplest possible structure.

The Class-D line drivers show a considerable range of bandwidths and linearities, however there are some trends. The structures around 1MHz/40dB uses zeroth or first order modulators and low oversampling ratios, which result in relatively low linearities. Wider bandwidth structures around 2.2MHz-8MHz achieve linearities around 55dB by using higher order loops, higher oversampling ratios or alternate modulation structures. These advanced techniques are possible due to the modest signal bandwidths which allow lower switching frequencies for a given oversampling ratio than a wider bandwidth structure can achieve. The new Class-D structure uses a very low oversampling ratio in conjunction with a loop filter which aims to extend the usable signal bandwidth.

While linearity is important to meet the system requirements of a particular application, the motivation to use Class-D structures is to take advantage of their high efficiency. The efficiency of recently published line drivers is shown in Figure 7.7, versus the line driver bandwidth. The graph divides into three sections according to the amplifier Class, in accordance with the theoretical efficiency of the different classes, with Class-AB structures the least efficient around 5-10%, Class-G/H structures achieving 15-17%, and Class-D structures achieving from 20-42% efficiency. There is a trend among the Class-D line drivers where as the line driver bandwidth increases, the efficiency decreases.

The new line driver presented here exceeds the bandwidth of other published Class-D line drivers by a factor of 3 and is 3 times as efficient as a similar 30MHz Class-AB line driver.

7.5 Conclusion

A wide band Class-D line driver based on a second order self-oscillating modulator has been implemented and measured. It is wider bandwidth than other reported Class-D line drivers, capable of up-to 30MHz. The line driver also achieves higher efficiency than other 30MHz Class-AB/G/H line drivers, in the region of 10% – 20% depending on the injected power.

Linearity, particularly at wide bandwidths and high power, is degraded by layout parasitic components and a schematic flaw. The performance of the line driver could be improved substantially with a number of relatively minor adjustments to the design, which will be covered in Section 8.3 (Further Work).

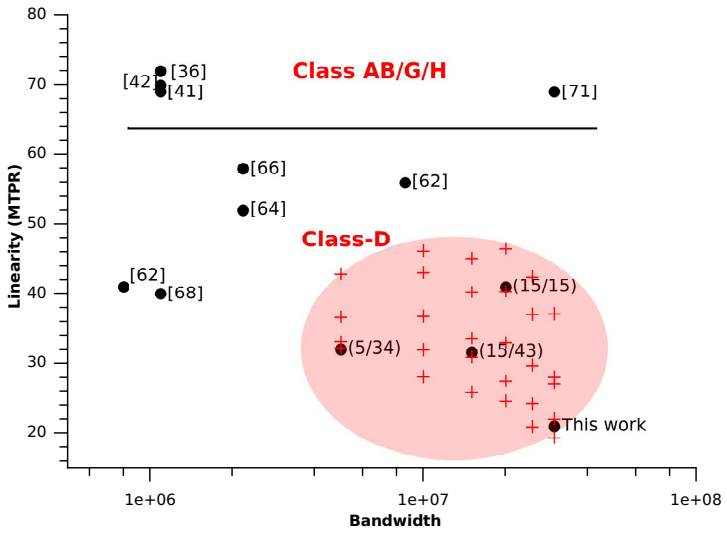

Figure 7.6: Bandwidth versus linearity of recently published line drivers and this work (black dots). Red crosses show the performance of this work at other signal bandwidth and injected power combinations.

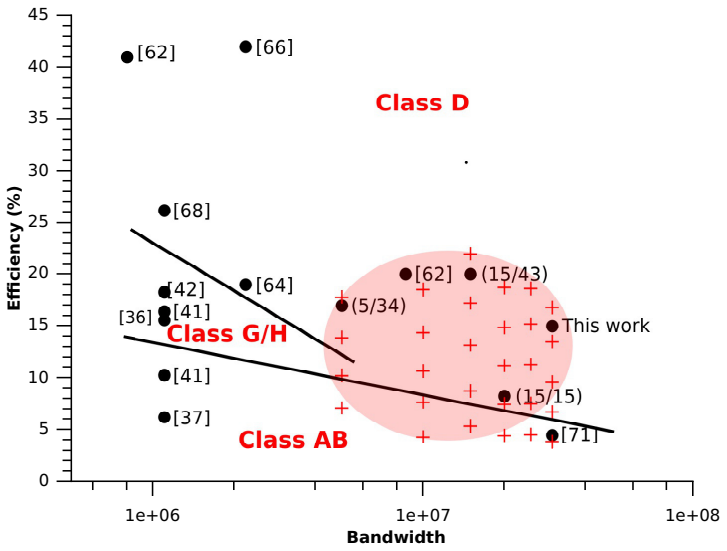

Figure 7.7: Bandwidth versus efficiency of recently published line drivers and this work (black dots). Red crosses show the performance of this work at other signal bandwidth and injected power combinations. The graph is divided into three areas according to the Class of line driver used: AB, AB+G/H and D.

Chapter 8

Conclusion

8.1 Summary

Line drivers sit in an uncomfortable position between digital communication systems, real-world poor-quality communication cables, and commercial technology decisions. The digital communication system is optimised for maximising spectral efficiency, but one of its greatest drawbacks, high CF, is delegated by the digital designer as a problem for the line driver designer to solve.

Similarly, real world cables have highly variable impedances and to design for a worst case line means the line driver must drive a low impedance load with a corresponding high injected power. Again, this problem is delegated by the system designer as a problem for the line driver designer to solve. Finally, the system designer also desires low-voltage digital CMOS implementations with high efficiency. It is not easy to meet all the requirements.

Previous line driver solutions involve significant compromises in some way – they are either wide band with low efficiency (Class-AB structures), or medium band but with high efficiency (Class-D structures). As communication systems have increased in bandwidth, the only choice is to use Class-AB structures and accept the poor efficiency.

The aim of this work was to improve the poor efficiency of wide-band line drivers by improving the bandwidth of Class-D structures, while injecting high power and maintaining compatibility with modern, nanometer level digital CMOS processes.

Along the path to the solution, a power modelling toolkit has been developed which allows quick examination of the system-level trade-offs between technology, voltage,

frequency and efficiency, of Class-D output stages. This model shows that Class-D can maintain competitive efficiencies at high switching frequencies, and allows Class-D output stage efficiency trade-offs to be evaluated quickly and accurately without lengthy numerical simulations.

Building on this work, a N/N totem pole output stage was proposed to replace the conventional P/N totem pole output stage. The N/N totem pole uses a fast totem-pole driver to pump the gate of the high-side NMOS device above the supply at frequencies around 150MHz. As well as exceeding the efficiency of the common P/N totem pole structure by 7%, the new output stage operates at considerably higher frequencies than other N/N totem pole drivers and is implemented in a low-voltage process CMOS process. Finally, the output stage also occupies approximately 10% less die area than other reported N/N totem pole structures by replacing output transistor area which must be laid out to ESD rules, with pump capacitors which do not need to observe ESD rules.

The design of a wide band Class-D amplifier then begins in earnest. Relevant theory is reviewed and a design flow for Class-D design is presented. A new Class-D line driver is then designed in a 0.13μm CMOS process from UMC. It aims to achieve a signal bandwidth of 30MHz by using novel, very wide bandwidth circuit components to push non-dominant poles to very high frequencies. Although wide bandwidth and high efficiency are achieved, the implementation suffers from a slow gate driver circuit which limits the switching frequency and so the usable signal bandwidth. Note that due to time constraints, the N/N totem pole was not implemented in the Class-D line driver, instead a conventional P/N totem pole was used.

8.2 Critical Analysis

During the course of this work, a number of issues and caveats arose and these will now be discussed.

8.2.1 Power modelling

The power model presented in Chapter 3 can accurately model simple output stage losses and provides a fast way of exploring the Class-D design space by considering just the Class-D output stage. However, it is in some ways oversimplified as it does not consider how the output stage will be driven.

Losses from the output driver are not included in the model as they are, to a large

extent, determined by the implementation of the driver circuit. Due to the large size of the output devices and, in particular for N/N totem pole structure which requires non-trivial driver circuits, the losses of the output driver can become comparable to those of the output stage itself.

While it is possible in principle to model complex output stages including driver in the power model, doing so is non-trivial and impractical in the early stages of design, so while the model is useful for pointing out directions, it should be kept in mind that the efficiencies and injected powers it reports may have significant deviation from a final circuit design.

8.2.2 N/N totem pole variability

The N/N totem pole structures presented in Chapter 4 achieve efficient operation while driving high power at very high frequencies. One aspect to be aware of is that the transitions from low-to-high and high-to-low are sensitive to the timing of the two input signals and to process variations. If these signals are not correctly time-aligned and the circuit is operating in a slow-P/fast-N or fast-P/slow-N process corners, cross-over distortion can result or worse, increased power consumption due to shoot-through of the output devices.

Preventing output-device shoot-through requires aggressive sizing of the pre-driver transistors such that additional distortion and parasitic power dissipation occur.

8.2.3 Implementation challenges

The implemented chip does give tantalising hints that state-of-art efficiency in wide-band applications is possible from Class-D amplifiers, however the self-oscillating topology used here is extremely sensitive to design parasitics, which becomes increasingly problematic as the design progresses and the layout of different blocks becomes complete. By this point, however, it may be too late to change much in the design.

8.2.4 Wider bandwidths

New powerline communication standards such as G.hn[120] have emerged during the course of this work. This increases the signal bandwidth further, up to approximately 80MHz, corresponding to an approximately three times increase in the required switching frequency. This will present a major problem for the Class-D line driver. Aside from

getting a self-oscillating architecture to oscillate predictably and reliably at around 300MHz – where small parasitics will have an even more significant effect than they do at 100MHz – getting large switching currents on and off the chip will become a major challenge due to extremely high $\mathrm{d}i/\mathrm{d}t$ voltages associated with parasitic package inductance.

More generally, the quiescent power dissipation of a Class-D driver is determined by the size of the driver and frequency of operation according to $P = CV^2 f_{\text{switch}}$, where gate area C is determined by the peak power that must be driven. Increasing bandwidth for a fixed peak load power means a corresponding increase in f_{switch} and so an almost linear decrease in efficiency. A Class-D line driver for G.hn might be possible, but it would be no more efficient than a Class-AB structure.

8.2.5 Class-D operation

It is common for reports on Class-D to claim theoretical efficiencies of 100%. Practical implementations quickly encounter static and dynamic loss mechanisms related to non-idealities of the Class-D output devices which detract from this 100% figure. Especially in systems handling high power with very high switching frequencies, these parasitic losses become very significant and the Class-D is no longer a particularly efficient structure.

It could be said that from a certain point-of-view, Class-AB and Class-D systems both suffer from the same efficiency problem: neither of them address the high CF of the signal. Class-AB inefficiency comes from the voltage drop over the output devices which are sized to drive a large voltage. Due to the large CF, there is a large RMS voltage drop across the output devices so they dissipate the majority of supply power in the output devices rather than transferring it to the load.

Similarly, Class-D systems are sized to driver a certain voltage swing, but because of the high signal CF, they spend most of their time at low modulation indexes, where they deliver only small amounts of energy to the load. The ratio of energy transferred to the load, to the energy used to drive the Class-D output stage is thus a low number.

From this perspective, Class-D approaches do not address the fundamental source of inefficiency – crest factor – in modern communication line drivers. To properly address the problem, a line driver would need to do less work when injecting less signal power.

8.3 Further Work

Immediate further work should involve addressing the layout and schematic performance degradations. For a comparatively small amount of work, it is expected that a significantly improved design can be achieved – on the order of 35dB MTPR at 56mW injected power and 30MHz bandwidth. This requires the following items to be completed.

- Re-layout the non-overlap circuit and programmable delay block to reduce capacitance. It may be beneficial to replace the structure with a faster 0.9V implementation and then use a high speed levelshifter to convert back to 3.3V logic levels.
- Identify the cause of additional parasitic resistance in the output driver then improve metal routing to reduce it.
- Either increase the bias current of the current buffer cells so that they can better tolerate the fast current spikes coming through the "zero" capacitor, or alternately, remove the "zero" capacitors and increase bandwidth of the current buffers and reduce the delay of the non-overlap circuit/delay block.

In addition, in order to prepare the part for production, the following issues must be addressed:

- An R/C calibration circuit is needed to compensate for process variations in resistor and capacitor values which alter the loop filter transfer function.
- A self-oscillating frequency control loop is needed to automatically drive the delay-block programmability control, such that the self-oscillating frequency is well defined and not excessively sensitive to parasitics and supply/temperature changes.

Longer term and more generally, a number of areas for further work have been identified.

- The analysis of self-oscillating loop distortion uses describing function techniques for sine wave input signals. Real line drivers use Gaussian-distributed signals which requires a different distortion model for the loop than the one used in the sine wave case. An analysis of distortion for the Gaussian signal case would be a useful addition to the Class-D amplifier design literature.
- A model, either empirical or analytical, covering the impact of output stage non-idealities as discussed in Section 7.2.4 would assist with determining final chip performance at the very start of a design.
- The loop filter in this design was not current optimized and a redesign could reduce its current consumption. As the loop filter and comparator consume almost one

quarter of total line driver quiescent current, any improvements here will make a noticeable difference to overall efficiency.

- The transconductor topology can tolerate large voltage inputs which are higher frequency than the supply. This can be taken advantage of by implementing the signal path using the very high g_m 1.2V devices available in the UMC 0.13 μm process, allowing a very wide bandwidth loop filter and a low propagation delay tapered buffer to be implemented. This should improve the self-oscillating frequency and the linearity of the line driver.

- Class-D is quite efficient but high linearity is hard at wide bandwidth. A self-oscillating Class-D amplifier could be used as the supply generator for a Class-AB amplifier – a Class-H structure – in order to combine the efficiency of a Class-D with the linearity of a Class-AB.

- A low bandwidth self-oscillating Class-D amplifier could be used in parallel with a Class-AB, where the self-oscillating Class-D provides only the low frequency current and the Class-AB provides the high frequency current and linearizes the Class-D. This is similar to [80].

- The self-oscillating frequency is a critical design parameter in self-oscillating loops and the number of variables it depends on should be minimized. A comparator can be made to oscillate by placing it in negative feedback with a third order loop filter in the feedback path, as in Figure 8.1[36]. This could be extended by embedding the oscillating comparator structure inside a Class-D loop as in Figure 8.2, with the aim of making the self-oscillating frequency independent of the properties of $H(s)$ and the output driver. Care would need to be taken to ensure the outer loop does not start to oscillate, however.

- In conventional Class G amplifiers, the supply rail of a Class-AB is pumped or switched in order to minimise losses in the Class-AB stage. A similar approach could be used in Class-D to reduce quiescent power consumption, which depends on the supply voltage squared.

- An output transformer with multiple input windings[90] could be used to segment the Class-D output driver into multiple units. At low powers, most units can be disabled to reduce the quiescent power consumption.

- Rather than worrying about the design parasitics which result in a particular oscillation frequency, it may be advantageous overall to use an open loop PWM architecture. This is extremely simple and can have a very well defined switching frequency. Distortion and noise at the output are not suppressed by loop gain but potentially some of this can be removed using digital predistortion of the input signal, possibly in conjunction with a feedback ADC or calibration loop which measures the Class-D output signal and applies some correction to the input signal.

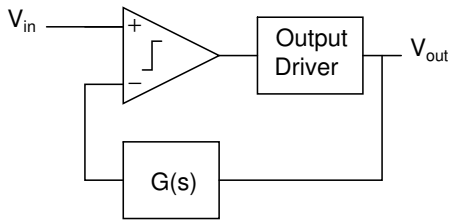

Figure 8.1: Comparator that self-oscillates, used as a Class-D power amplifier[36].

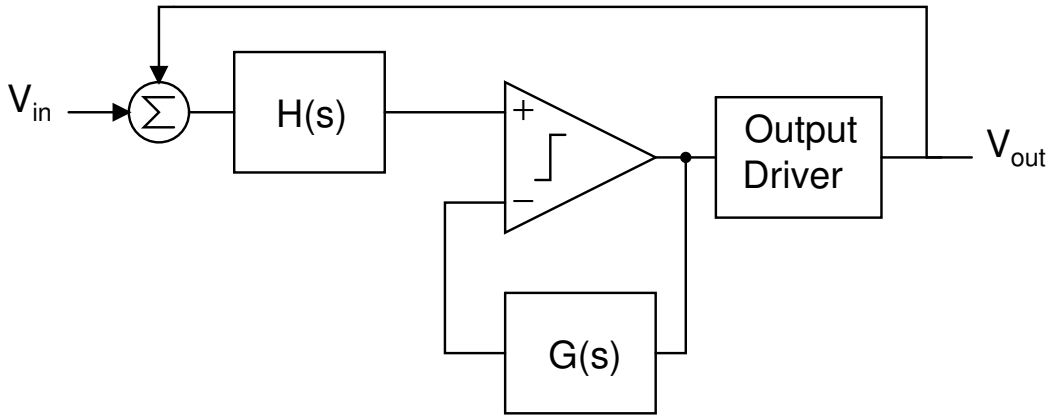

Figure 8.2: Oscillating comparator embedded in a Class-D loop. Neither the loop filter or the output stage are in the comparator's oscillating loop.

8.3.1 High-power, low-I/O voltage Class-D

In very modern technology nodes such as 28nm and below, it is common for the I/O device supply voltage to start decreasing below 3.3V – 1.8V or 1.5V are typical. This makes implementing structures capable of injecting sufficient power much more difficult. While stacking was discussed earlier as a method of using a series stack of low voltage devices to safely operate from a high voltage supply, it requires a slow and complex level shifter to drive it.

An alternate structure was developed during this work which potentially allows above-supply voltages in the output stage, while reducing the complexity of, or eliminating entirely, the level shifter. The structure is shown in Figure 8.3, where it places the conventional pull-up devices – shown as PMOS devices in the figure, but can also be implemented using NMOS devices – with a passive pull-up structure, a centre tapped transformer. This structure is often used in DC-DC converters[121].

In operation, the circuit behaves as follows. In a first state, INP is high and INN is low. Transistor MP will be a low impedance path to ground, while MN will be high impedance. Transformer winding C will effectively by open-circuited and non-operational, while windings A and B will operate as a conventional transformer. As the windings A and B are out-of-phase, voltage V_{DD} will appear inverted at output, ie. $V_{OUT} - V_{DD}$, causing

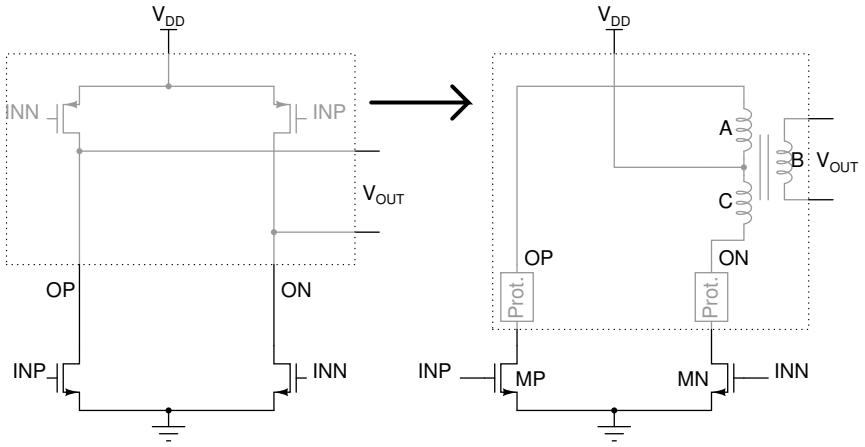

Figure 8.3: Conversion of a conventional Class-D structure to a High voltage structure.

current to begin flowing in the load. This load current is reflected across windings B and A and will flow through MP to ground. In a second state, INP is low and INN is high. MP will be high impedance and MN will be low impedance. Now, transformer winding A is open-circuited and so windings C and B operate as a transformer. Windings C and B are in-phase, so the output V_{OUT} is approximately equal to V_{DD} and now the load current will flow through MN.

It should be noted that while the winding connected to a high-impedance point is open-circuited, the electromotive force of the transformer will cause a voltage equal in phase but opposite in magnitude to develop across the open-circuited winding. For example, while OP is at 0V, ON will be forced to $2V_{DD}$. It follows that a protection structure will always be necessary, as a voltage twice the supply voltage will be present on either node OP or on node ON. A number of protection schemes are possible and Figure 8.4 briefly describes four such structures[74].

One key advantage of this centre-tapped transformer structure is that the drive device in the output stage can be a low-voltage, high-g_m core device. No output stage pre-driver is then required and the output stage should be able to switch very quickly, directly driven by the tapered buffer. This would allow high self-oscillating frequencies and so even wider bandwidths as required by newer PLC standards, while taking full advantage of the very high g_m available in the 28nm and below process nodes.

8.4 Final remarks

Class-D structures can be pushed to wide bandwidths while maintaining their efficiency benefits versus other amplifier classes, but the design is very parasitic sensitive and high linearities are hard to achieve. Revisions to test chips can be made to overcome

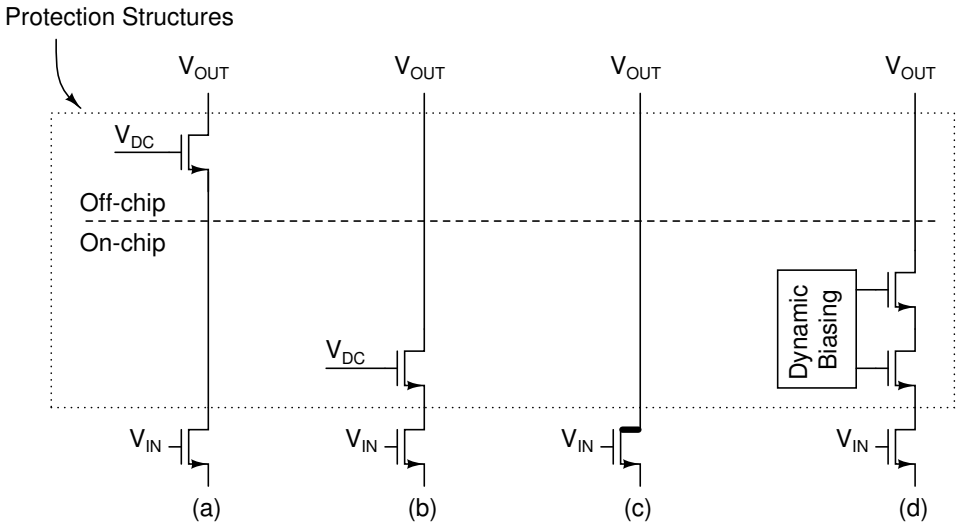

Figure 8.4: High-voltage-tolerant protection structures. (a) Off-chip cascode protection. (b) On-chip cascode protection. (c). High-voltage tolerant LDMOS, DEMOS or Drift-MOS devices. (d) On-chip dynamically biased cascode.

implementation shortcomings, and further work can always be done to attempt to squeeze out a little more linearity or to chip away at the power consumption of the basic Class-D design. However, in high power applications with wide bandwidth – where the power required to drive the output devices is much more than the signal power – Class-D is not a fundamentally efficient structure.

There is more scope for development if the basic Class-D output stage is used in conjunction with system level techniques – such as segmented output stages, combined AB+D stages in series or in parallel, open-loop modulation with digital compensation – to fundamentally address the crest factor problem.

Appendix A

Self-oscillating frequency calibration code

This Verilog-A block, called the "Cycle Stabilizer", will determine the delay that must be inserted into the loop to achieve a particular self-oscillating frequency. For simulation purposes, it is inserted between the loop filter output and the comparator input, but this is equivalent to applying the delay in the ΔT_d programmable delay cell inside the non-overlap generator. at the beginning of simulation, the line driver inputs are both set to the common mode input voltage, the "stabilize" signal is set high and the Cycle Stabilizer will continually measure and adjust the switching frequency until it matches the desired frequency, or the minimum/maximum delay limit is reached.

Listing A.1: Verilog-A implementation of automatic delay calibration algorithm

```
// VerilogA for PLC_CLASSD, y_cycle_stabilizer, veriloga_200MHz_zero

`include "constants.vams"
`include "disciplines.vams"

module y_cycle_stabilizer(intocm, stabilize, sensep, sensen, outp, outn);
    input sensep, sensen, stabilize;
    output outp, outn, intocm;

    parameter real fset = 100e6;
    parameter real tdmax = 5e-9;
    parameter real tstep = 50e-12;

    electrical sensep, sensen, outp, outn, intocm, stabilize;
```

```
real rising_time, period, td, step, delta;

integer do_stabilize;

analog begin
    @(initial_step) begin
        rising_time = 0;
        td = 1e-9;
        do_stabilize = 0;
    end

    @(cross(V(stabilize)-0.5, +1, 25p)) begin
        $display("Starting loop stabilization.");
        do_stabilize = 1;
    end

    @(cross(V(stabilize)-0.5, -1, 25p)) begin
        if ((do_stabilize == 1) && (period > 0)) begin
            // we have been running loop stabilization
            $display("===== LOOP STABILIZATION ENDING =====");
            $display("    Inserted loop delay: %.2f ns", td*1e9);
            $display("    Loop frequency:    %.2f MHz", 1/(1e6*period));
        end
        do_stabilize = 0;
    end

    @(cross(V(sensep, sensen), 1, 25p)) begin
        if(do_stabilize == 1) begin
            if (rising_time > 0) begin
                period = $abstime - rising_time;
                delta = period - (1/fset);
                if (delta > 10*tstep) begin
                    step = 5*tstep;
                end else begin
                    step = tstep;
                end

                $display("Frequency %f (step %f ps, td: %.2f ns)",
                    1/(period), step*1e12, td*1e9);

                if (period > (1/fset)) begin
                    if (td <= step) begin
                        td = 0.0;
                        $display("WARNING: Cycle stabilizer hit minimum
                            delay.");
                        do_stabilize = 0;
```

```
                    end else begin
                        td = td - step;
                    end
                end else begin
                    if (td + step > tdmax) begin
                        $display("WARNING: Cycle stabilizer hit maximum
                            delay.");
                        td = tdmax;
                        do_stabilize = 0;
                    end else begin
                        td = td + step;
                    end
                end
            end

            rising_time = $abstime;
        end else begin// if (do_stabilize == 1) begin
            rising_time = 0;
        end
    end

    if (analysis("tran")) begin
        V(outp) <+ absdelay(V(sensep), td, tdmax);
        V(outn) <+ absdelay(V(sensen), td, tdmax);
        V(intocm) <+ transition(1.0*do_stabilize, tstep, 1e-9);
    end else begin
        V(outp) <+ V(sensep);
        V(outn) <+ V(sensen);
        V(intocm) <+ 0.0;
    end
  end
endmodule
```

Appendix B

Test chip characterisation data

Table B.1 contains characterisation data for the line driver with a 13.3Ω load. Table B.2 contains characterisation data for the line driver with an 8.3Ω load.

Table fields are:

- BW: This is the signal bandwidth. For each bandwidth possibility, a DMT signal has been generated between 2MHz and BW. All the signals are normalized so that they contain the same integrated power, so signals with a smaller bandwidth will have more power per Hertz.
- AWG swing: This is the peak-to-peak swing provided by the arbitrary waveform generator, with a maximum of 0.7Vpp. The op-amp on the text board applies a gain of 4.4, so with a 0.7Vpp input signal, the signal at the input of the line driver test chip will be 3.08Vpp. The line driver operates in unity gain so the output should be ±3.08Vpp on the positive and negative line driver outputs. After the differential-to-single-ended conversion by the output transformer, the maximum signal swing would be 6.16Vpp single ended.
- Power supply current: This is the raw power supply current value, before the PCB and Bandgap current are removed.
- Vload (rms): RMS load voltage, as measured by a oscilloscope.
- Vload (p-p): Peak-to-peak load voltage, as measured by an oscilloscope.
- CF: Calculated CF to sanity check the signal swings.
- Psupply (mW): Calculated line driver power consumption. This subtracts the current consumption for the PCB and Bandgap before multiplying by the nominal 3.3V supply voltage, 3.3V.
- Pload (mW): Power computed in the load, using the Vload(rms) measurement above and the known load resistor value.

To aid interpretation of the tables, the MTPR and Efficiency results have been colour coded. For Efficiency fields, green means Efficiency $> 15\%$ while orange means Efficiency $> 10\%$ but $< 15\%$.

For MTPR, green means MTPR $>$ 30dB, orange means 27 dB $<$ MTPR $<$ 30dB while red means MTPR $<$ 20dB.

BW	AWG swing	Power supply current (mA)	Vload (rms)	Vload (p-p)	CF	Psupply (mW)	Pload (mW)	Efficiency (%)	MTPR results pc50	pc90	pc97	wc
5	0.4	6.94E-02	0.40	3.1	3.9	172.9	12.3	7.1	48.5	42.9	38.7	38.7
5	0.5	7.16E-02	0.49	4.1	4.2	180.1	18.4	10.2	41.1	36.6	32.6	32.6
5	0.6	7.42E-02	0.58	4.9	4.2	188.6	26.2	13.9	36.3	32.2	28.3	28.0
5	0.7	7.71E-02	0.68	5.9	4.4	198.5	35.4	17.8	37.7	33.1	28.7	27.6
10	0.3	6.79E-02	0.31	2.4	4.0	167.9	7.2	4.3	52.8	46.2	45.0	44.8
10	0.4	6.98E-02	0.42	3.2	3.8	174.3	13.5	7.7	46.8	43.1	41.7	41.2
10	0.5	7.23E-02	0.50	4.1	4.1	182.4	19.5	10.7	40.0	36.8	35.9	34.5
10	0.6	7.52E-02	0.60	5.1	4.3	192.1	27.6	14.4	37.0	31.9	30.9	28.6
10	0.7	7.86E-02	0.70	5.1	3.6	203.3	37.7	18.6	32.3	28.1	26.5	25.2
15	0.3	6.88E-02	0.35	2.6	3.8	171.1	9.2	5.4	55.1	45.1	42.3	41.3
15	0.4	7.15E-02	0.45	3.8	4.2	180.0	15.7	8.7	47.0	40.3	37.9	36.3
15	0.5	7.49E-02	0.57	4.7	4.1	191.2	25.2	13.2	39.9	33.6	32.6	31.5
15	0.6	7.90E-02	0.68	5.7	4.2	204.7	35.3	17.2	35.1	30.9	27.2	26.6
15	0.7	8.35E-02	0.79	6.1	3.9	219.4	48.3	22.0	31.9	25.9	23.9	22.4
20	0.3	6.84E-02	0.31	2.3	3.8	169.7	7.5	4.4	53.0	46.5	42.8	40.9
20	0.4	7.08E-02	0.42	3.2	3.8	177.5	13.3	7.5	46.0	40.3	37.7	27.4
20	0.5	7.38E-02	0.52	3.9	3.8	187.3	21.0	11.2	38.8	32.9	30.9	27.3
20	0.6	7.72E-02	0.62	4.6	3.7	198.8	29.6	14.9	33.5	27.5	25.4	21.2
20	0.7	8.12E-02	0.72	5.3	3.7	212.0	39.7	18.7	29.5	24.6	22.3	20.0
25	0.3	6.87E-02	0.32	2.5	3.9	170.5	7.7	4.5	50.6	42.5	38.9	32.1
25	0.4	7.12E-02	0.42	3.1	3.6	178.9	13.6	7.6	44.0	37.0	32.8	29.9
25	0.5	7.44E-02	0.53	3.9	3.7	189.3	21.4	11.3	36.2	29.8	25.0	16.8
25	0.6	7.80E-02	0.63	4.8	3.8	201.3	30.6	15.2	30.9	24.2	19.7	14.2
25	0.7	8.21E-02	0.72	5.5	3.8	214.9	40.0	18.6	26.7	20.9	19.9	13.0
30	0.3	6.83E-02	0.29	2.3	4.0	169.3	6.5	3.8	49.7	37.2	33.1	27.1
30	0.4	7.06E-02	0.39	3.2	4.0	177.0	11.9	6.7	42.2	28.1	23.5	17.1
30	0.5	7.35E-02	0.48	3.9	4.0	186.5	17.9	9.6	37.1	27.2	22.5	19.5
30	0.6	7.69E-02	0.59	4.5	3.8	197.8	26.8	13.5	32.5	22.1	19.3	10.2
30	0.7	8.08E-02	0.68	5.1	3.8	210.6	35.4	16.8	27.2	19.4	16.0	10.2

Table B.1: Line driver characterisation results, R_{load}=13Ω.

The last line in the Table is the closest to the original HomePlug AV specification; 30MHz signal bandwidth and an injected power of 35mW which is 2dB below the 56mW limit. However, even at this reduced injected power the test chip is unable to meet the 30dB notch depth specification with the worst case MTPR value. Also, the poor performance of the pc90 and pc97 metrics indicate that it is the problem is not confined to a very small number of notches, but that are a lot of other notches which also have poor notch depth. If the problem was only with a small number of notches then those particular notches might improve on a subsequent symbol transmission and so the MTPR degradation will average out over multiple symbols. This is discussed in

Off-current 1.70E-002

BW	AWG in	Power supply current (mA)	Vload (rms)	Vload (p-p)	CF	Psupply (mW)	Pload (mW)	Efficiency (%)	MTPR results pc50	pc90	pc97	wc
5	0.4	0.07	310	2.5	4.1	173.8	11.6	6.7	47.5	43.0	38.8	38.8
5	0.5	0.07	390	3.2	4.1	181.6	18.3	10.1	41.0	36.8	32.9	32.4
5	0.6	0.07	466	3.9	4.2	190.8	26.2	13.7	36.2	32.3	28.3	27.7
5	0.7	0.08	531	4.5	4.2	201.4	34.0	16.9	36.9	31.7	28.8	28.1
10	0.3	0.07	224	1.7	3.8	166.1	6.0	3.6	55.1	48.8	46.3	45.1
10	0.4	0.07	300	2.3	3.8	171.4	10.8	6.3	47.4	43.7	42.0	41.6
10	0.5	0.07	362	2.9	4.1	178.0	15.8	8.9	41.0	37.4	36.7	34.6
10	0.6	0.07	431	3.6	4.2	186.0	22.4	12.0	37.6	32.8	31.8	31.2
10	0.7	0.08	501	3.5	3.5	195.1	30.2	15.5	32.3	28.4	26.4	24.9
15	0.3	0.07	270	2.2	4.1	170.4	8.8	5.2	55.2	46.6	44.5	42.8
15	0.4	0.07	351	2.9	4.1	179.0	14.8	8.3	47.1	41.4	38.4	36.2
15	0.5	0.07	440	3.5	4.0	189.9	23.3	12.3	40.2	34.3	33.1	30.7
15	0.6	0.08	520	4.0	3.8	202.8	32.6	16.1	34.8	28.7	27.3	26.5
15	0.7	0.08	600	4.5	3.8	217.0	43.4	20.0	31.6	26.3	24.6	23.4
20	0.3	0.07	245	1.9	3.9	169.7	7.2	4.3	53.2	45.8	42.5	40.4
20	0.4	0.07	325	2.4	3.7	177.5	12.7	7.2	46.0	39.2	36.0	30.8
20	0.5	0.07	404	3.0	3.7	187.4	19.7	10.5	38.9	32.6	30.3	27.8
20	0.6	0.08	481	3.4	3.6	199.0	27.9	14.0	33.9	28.1	26.0	19.8
20	0.7	0.08	550	4.0	3.6	212.0	36.4	17.2	30.1	23.8	22.2	18.2
25	0.3	0.07	240	1.9	4.0	170.3	6.9	4.1	50.3	40.4	35.3	24.0
25	0.4	0.07	329	2.4	3.6	178.4	13.0	7.3	44.6	32.3	27.1	25.1
25	0.5	0.07	405	3.0	3.7	188.6	19.8	10.5	36.3	26.6	24.5	19.9
25	0.6	0.08	475	3.5	3.7	200.5	27.2	13.6	31.7	22.9	19.6	15.0
25	0.7	0.08	554	4.1	3.7	213.8	37.0	17.3	26.7	21.3	18.6	11.4
30	0.3	0.07	228	1.9	4.2	169.3	6.3	3.7	50.7	37.6	33.6	28.4
30	0.4	0.07	300	2.6	4.3	176.9	10.8	6.1	42.4	28.4	24.3	15.5
30	0.5	0.07	380	3.0	3.9	186.4	17.4	9.3	37.3	27.5	22.7	19.2
30	0.6	0.08	450	3.7	4.1	197.6	24.4	12.3	33.7	25.5	19.2	16.5
30	0.7	0.08	520	4.1	3.9	210.6	32.6	15.5	27.2	21.0	17.5	12.5

Table B.2: Line driver characterisation results, R_{load}=8Ω.

Section 2.6.4.

Glossary

ADC Analogue to Digital Converter.

ADSL Asymmetric Digital Subscriber Line.

AFE Analogue Front End.

AWG Arbitrary Waveform Generator.

CF Crest Factor.

CMFB Common-mode Feedback.

CMOS Complimentary Metal Oxide Silicon.

DAC Digital to Analogue Converter.

DC Direct current.

DMM Digital Multi-Meter.

DMOS Drift-MOS.

DMT Discrete Multi-Tone.

DNW Deep N-well.

DSA Digital Signal Analyzer.

DSL Digital Subscriber Line.

DSP Digital Signal Processing.

EMC Electromagnetic Compatibility.

ESD Electrostatic Discharge.

FCC Federal Communications Commission.

FFT Fast Fourier Transform.

GBW Gain Bandwidth product.

HPAV HomePlug AV.

IM3 Third-order Intermodulation distortion.

ISDN Integrated Services Digital Network.

ITU International Telecommunication Union.

LC Inductor-Capacitor. A type of filter..

MTPR Missing Tone Power Ratio. The ratio between the power of a carrier and the power of noise/distortion level, measured at a specific frequency..

NTF Noise Transfer Function.

OFDM Orthogonal Frequency Division Multiplexing.

OSR Oversampling Ratio. The ratio between the switching frequency of a converter or Class-D amplifier, and the maximum signal frequency..

PCB Printed Circuit Board.

PLC Powerline communication.

PWM Pulse Width Modulation, a method of encoding amplitude information in the time domain.

QAM Quadrature Amplitude Modulation, where information is encoded into the magnitue or phase of a sinusoid carrier..

RF Radio Frequency.

RMS Root Mean Square.

SD Sigma-Delta.

SINAD Signal-to-Noise-and-Distortion ratio.

SNR Signal-to-Noise Ratio.

SO-SD Self-oscillating sigma-delta.

STF Signal Transfer Function.

THD Total Harmonic Distortion.

TSIDF Two-sine-wave-input describing function.

UGF Unity gain frequency.

UMTS Universal Mobile Telecommunications System (UMTS), a cellular telephone communications system.

VCCS Voltage Controlled Current Source, a block for generating current outputs from a voltage input..

VDSL Very-high bit-rate Digital Subscriber Line, a high speed telecommunications technology.

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NMOS-only Class-D Output Stages based on Charge Pump Architectures

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***Abstract*— An NMOS only Class-D output driver which uses charge pump techniques in a low voltage CMOS technology is presented. Compared to conventional Class-D output stages, the given implementation shows a gate area reduction of 45%, resulting in efficiency improvements. The circuit has been simulated in a $0.13\mu m$ process and is implemented using 3.3V I/O devices. The structure does not violate any gate-oxide reliability rules.**

I. Introduction

Class-D output stages are commonly used eg. [1] in low frequency audio applications due to their high efficiency at transferring charge from a supply to a load. When used in conjunction with a lossless LC filter, high linearity and high efficiency can be achieved simultaneously. The conventional Class-D H-bridge output structure shown in Fig. 1 consists of a P/N totem pole configuration with LC filter and resistive load, with the output transistors either off chip or on chip. Also shown are chains of pre-drivers, required to provide drive for the large gate capacitance of the output transistors. The input signals to the pre-drivers can either be out-of-phase, referred to as AD modulation, or in-phase, referred to as BD modulation.

In theory, Class-D drivers can be 100% efficient but the on-resistance, gate charging and shoot-through losses [2] of the output transistors decreases the practically achievable efficiency. The remainder of this paper will focus on the design of a single ended half of the full H-bridge output stage unless otherwise specified.

The main design challenges in Class-D are minimizing shoot-through, dead-time, parasitic losses and gate area. For a shared pre-driver circuit and a P/N totem pole configuration, shoot-through will always occur. To reduce shoot-through, the pre-drivers must be split into separate pull-up and pull-down pre-drivers. Then non-overlap techniques such as non-overlap circuits or non-overlap pre-driving sizing can be used to minimize or eliminate the time when both output devices are on, reducing or eliminating the shoot-through current. However, if both output devices are off for any time, the output will distort as it is not being driven. The longer the non-overlap time, the greater the distortion. Thus there is a trade-off between minimizing shoot-through and minimizing distortion, which is described in [3].

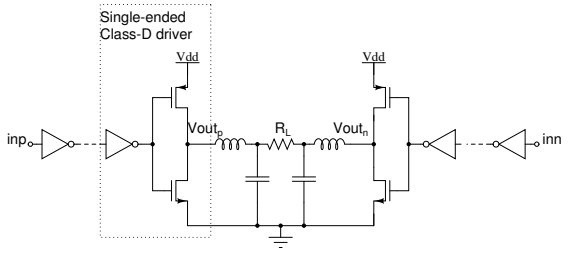

Fig. 1. Conventional P/N totem pole Class-D output in H-Bridge configuration.

The Class-D gate-charging losses are proportional to the gate area and the on-resistance losses are inversely proportional to the gate area. For a specified on-resistance in a given driver architecture, the gate area is fixed and so both parasitic losses are fixed. However, by exploring alternate driver architectures, it is possible to reduce the dynamic parasitic losses.

In this paper we present novel N/N totem pole class-D output stages based on charge pump architectures [4]. These structures provide gate area and switching loss reductions over existing circuits and are particularly suited to high-frequency operation with low supply voltages. Charge pump techniques allow improved gate drive over existing N/N totem pole circuits which obviate the need for large PMOS transistors in P/N stages (typically 3 times larger than the NMOS driver). The overall approximately 45% saving in gate capacitance reduces parasitic losses and lowers gate drive requirements on pre-buffering stages, which can also be made smaller and lower power. These techniques are also compatible with non-overlap driver sizings or circuits. Finally, all gate-oxide reliability criteria are respected during operation of the circuits.

In Section II, we will present a review of existing Class-D output stages. In Section III we will describe the main components and operation of our output driver. Section IV will present simulated results of the reduced shoot-through timing, gate-oxide reliability verification and circuit operation. Performance comparisons with other published Class-D driver circuits are given in Section V.

II. Class-D Output Stages

In the conventional P/N totem pole Class-D output stage shown in Fig. 1, equal pull-up and pull-down drive strengths require the PMOS transistor to be significantly larger than the NMOS transistor, resulting in a large total gate capacitance and so large gate charging losses. The structure also requires separately driven gates to reduce shoot-through losses.

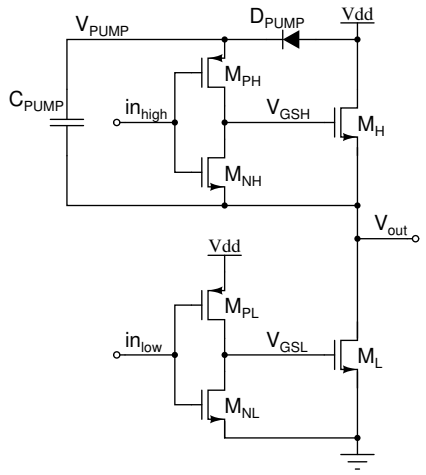

Fig. 2. High voltage N/N totem pole Class-D driver [5].

In integrated audio applications of Class-D, the output stage transistors (particularly the PMOS) dominate overall chip efficiency losses and so power savings are obtainable by optimization of this circuit. One method of reducing gate area is to replace the pull-up PMOS with a pull-up NMOS, which is known as an N/N totem pole. The N/N totem pole configuration requires that the gate of the pull-up device must exceed the positive supply rail. In high voltage processes, an established technique to achieve this is to use a Dickson charge pump where the pump capacitor is driven by the output of the Class-D stage [5], as shown in Fig. 2. It is emphasized that in_{high} is a level-shifted input referenced to $Vout$, while in_{low} can be driven directly as it is referenced to $0V$.

In high voltage processes, the diode drop introduced into the gate voltage of M_H is small in comparison to the supply voltage, however for low voltage applications this diode drop can be a significant fraction of the supply voltage. It has been reported in [6] that this decrease of gate drive reduces some of the benefits of using a pull-up NMOS rather than a pull-up PMOS. Additionally, the implementation of the level-shifted in_{high} signal involves extra complexity.

As Class-D drivers are pushed to higher frequencies in lower voltage technologies, the benefits of using an N/N totem pole configuration increase, but the drawbacks of using high-voltage drivers in low voltage processes become more severe.

III. Circuit Overview

Two circuits will be presented. The first circuit is a single ended driver for use in single-ended or H-Bridge configurations, with AD or BD modulation. The second circuit is a differential driver and can only be used with AD modulation.

A. Class-AD/BD Driver

The proposed Class-AD/BD output driver shown in Fig. 3 consists of an NMOS only Class-D output stage $MN0/1$ driven by a charge pump $MN3/4$ and $C0/1$ [7], and an inverter $MP2/MN2$.

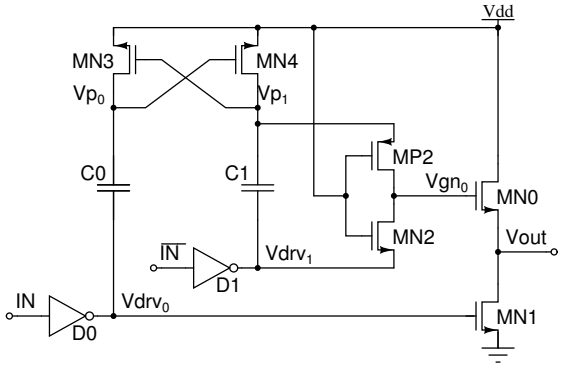

Fig. 3. Charge pumped N/N totem pole output stage.

The charge pump is unbalanced; the $MN4$, $C1$ pair must drive the large gate capacitance of output device $MN0$, while the $MN3$, $C0$ pair only need to drive the small parasitic capacitance on node Vp_0 – so can be significantly smaller than the former first pair.

The gate of output device $MN1$ requires a $0 - Vdd$ drive which is out-of-phase from IN. This is implemented by driving $MN1$ directly with the output of inverter $D0$. However, output device $MN0$ requires a $0 - 2Vdd$ drive on $Vgn0$ which is out-of-phase with $\overline{IN}$. The $MN4/C1$ half of the charge pump drives Vp_1 up to $2Vdd$ when $\overline{IN}$ is low. When $\overline{IN}$ is high, $Vdrv_1$ will be at $0V$, so the correct voltages to drive $MN0$ exist on $Vdrv_1$ and Vp_1 on alternating phases of $\overline{IN}$. To choose which voltage should be driven onto the gate of $MN0$, the source-driven inverter $MP2 - MN2$ is used. Conventional inverters connect either the PMOS source terminal or the NMOS source terminal to the common drain output depending on the gate voltage. Here, the gate voltage is fixed at Vdd and the PMOS and NMOS source terminals are driven between $Vdd/2Vdd$ and $0/Vdd$, respectively. The result is that Vgn_0 will be driven to $0V$ when $\overline{IN}$ is high, and to $2Vdd$ when $\overline{IN}$ is low.

As the gate of $MN0$ is charged from the pump capacitor $C1$, the voltage on pump node V_{p1} – and hence on Vgn_0 – will drop when charge is transferred to the gate of $MN0$. $C1$ is sized ten times larger than the gate capacitance of $MN0$ in order to limit the drop in gate voltage to one tenth of $2Vdd$. To equalize the output drive strengths, $MN0$ must be sized 10 percent larger than $MN1$.

Compared to [5], the proposed driver does not require a level shifted gate control signal and it does not suffer from a gate drive diode drop, which is a significant advantage in low voltage processes.

B. Class-AD driver

The proposed Class-AD driver is shown in Fig. 4. It is similar to [5] and to the above Class-AD/BD driver. Compared to the Class-AD/BD driver, the smaller half of the charge pump is removed and instead the appropriate signals are cross-coupled to a second Class-AD driver, which is driven with a complementary input. The result is a simplified circuit with

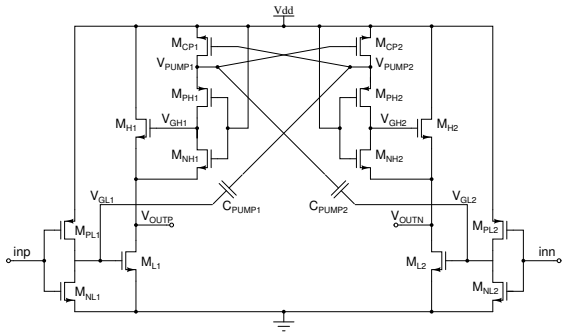

Fig. 4. Cross-pumped NMOS-only Class-D output in H-bridge configuration.

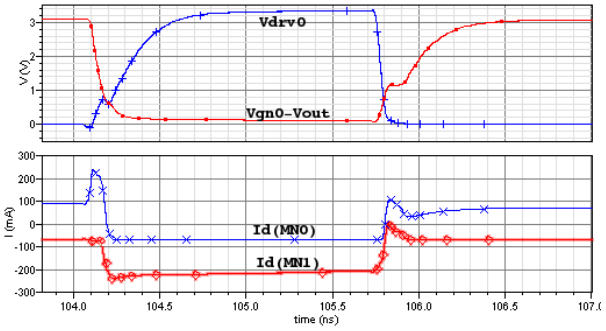

Fig. 5. Timing diagram showing pre-driver outputs and drain currents for $MN0/1$.

only a single input on each side of the H-bridge. The operating principles of the circuit very closely follow those described for the Class-AD/BD driver, so will not be elaborated on. However, the elimination of the separate pull-up control signal introduces some shoot-through, requiring aggressive driver sizing in order to limit the shoot-through current at the expense of increased power dissipation in the pre-driver circuit.

IV. Simulations

The proposed circuits have been designed and simulated in a $0.13\mu m$ CMOS process, operating from a single $+3.3V$ supply, and are based on an output driver on-resistance of 3Ω and a modulation depth of 0.9. Operation of the reduced shoot-through pre-driver sizing is demonstrated, followed by a simulation of output transitions, and finally the gate-oxide reliability conditions are verified. All discussions are based on the Class-AD/BD driver shown in Fig. 3.

A. Reduced Shoot-through

To reduce shoot-through, the pre-driver dimensions have been designed such that the crossing point of $Vdrv_0$ and $Vgs_{MN_0} = Vgn_0 - Vout$ is close to the threshold voltage of the output devices. This ensures that only one of the output devices can be fully on at any point in time, so shoot-through is significantly reduced.

A timing diagram demonstrating reduced shoot-through drive signals and drain currents is shown in Fig. 5. The reduced shoot-through driver sizings mean that $Vdrv_0$ and $Vdrv_1$ are

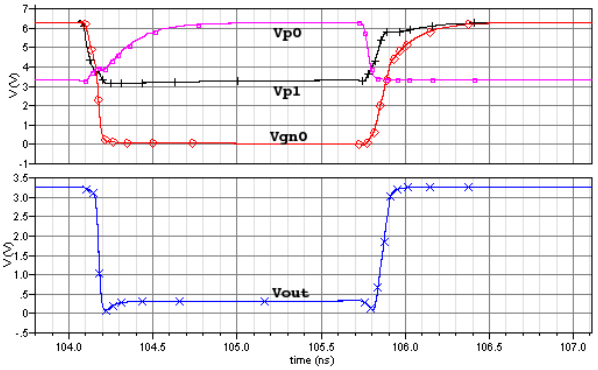

Fig. 6. Timing diagram illustrating node waveforms while the output undergoes high-low and low-high transitions.

not symmetric. For falling/rising $IN/\overline{IN}$, $Vdrv_1$ drops first followed by $Vdrv_0$ rising, while for rising/falling $IN/\overline{IN}$, $Vdrv_0$ drops first followed by $Vdrv_1$ rising.

B. Output transition

The operation of the output driver circuit as it creates output edges is now discussed and is illustrated in Fig. 6. Initially, $Vdrv_0 = 0$, $Vdrv_1 = Vdd$ and $Vp_1 = 2Vdd$. MN3 will be turned on, charging Vp_0 to Vdd. $MN2$ will be off and $MP2$ will be on as $Vgsp_2 = -Vdd$ and $Vgsn_2 = 0$, so Vgn_0 will be charged to $2Vdd$. Therefore, output device MN0 is on and MN1 is off, so $Vout = Vdd$.

A negative output transition begins with $Vdrv_1$ falling, pulling Vp_1 towards Vdd. $MN3$ and $MP2$ turn off, and $MN2$ turns on. Vgn_0 begins discharging through D1. At the same time, $Vdrv_0$ is slowly rising. $Vdrv_0$ crosses the threshold voltage of $MN1$ just as Vgn_0 negatively crosses the threshold voltage of $MN0$, and in doing so begins to pull $Vout$ low. $Vdrv_0$ keeps rising and pushes Vp_0 up, turning on MN4 and charging Vp_1 to Vdd. The transition is now complete and $Vout$ is at $0V$. The positive output transition follows a similar process, but uses complementary signals and devices.

C. Gate-Oxide Reliability

Transistors $MP2$, $MN2$ and $MN0$ are the only devices which experience voltage swings greater than $\pm Vdd$. Charge pump devices $MN3/4$ do not, in operation, encounter voltage swings greater than $\pm Vdd$ so will not be discussed here. The multiplexer $MP2/MN2$ and output device $MN0$ all experience voltages from $0V$ to $2Vdd$. The gates of $MP2/MN2$ are connected to Vdd and this ensures that their gate-source/drain voltages can never exceed $\pm Vdd$. Finally, while the gate-source voltage of $MN0$ equals $Vdd/0V$ in high/low output states, $MN0$ must be sized to be able to pull $Vout$ up quickly enough to avoid any output edge transients which could violate gate-oxide voltage requirements. Appropriate sizing is used in this paper.

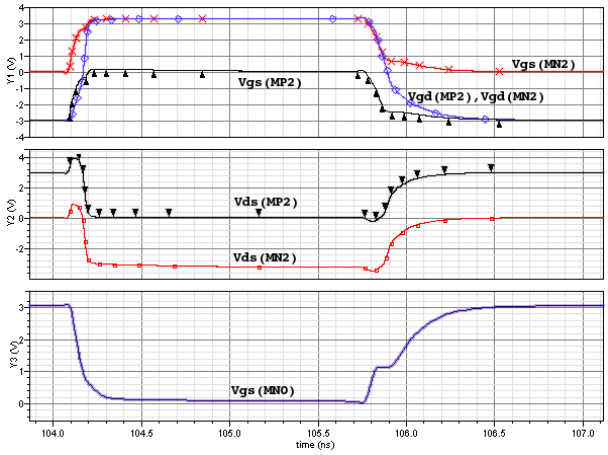

Fig. 7. All gate-source, gate-drain and drain-source voltages across devices which experience a voltage swing greater than Vdd are shown here.

V. Performance Comparison

The four structures discussed in this paper are the conventional P/N driver (PN), a diode pumped N/N driver based on [5] (NN), a new charge pumped low voltage N/N driver (AD/BD) and a new cross pumped low voltage N/N driver (AD). To provide a comparison, the PN and NN drivers have also been designed and simulated for the same specifications and for the same performance as the new AD/BD and AD drivers. The area of a single-ended half of an H-bridge, is shown in Table I, along with the efficiency of a full H-bridge. Switched gate area is the sum of pre-driver gate area and output device gate area, and the load resistance is 50Ω.

It is observed that the total gate area of each of the N/N drivers is greater than that of the PN driver, due to the area overhead of the MOS capacitors and diodes. However, as the switched gate area that is charged for each input edge is significantly less in the N/N drivers than in the P/N driver, lower gate charging losses and so higher efficiencies are achieved for the N/N drivers, as is seen in the table.

Aggressive device sizing to reduce shoot-through in the AD driver enlarges its pre-driver gate area compared to the AD/BD stage, but does not fully eliminate shoot-through, hence it suffers from poorer efficiency than the AD/BD driver. The NN and AD/BD drivers show only small differences in terms of area and efficiency, although in both cases the AD/BD driver displays slightly better performance. In even lower voltage technologies, these difference will become more significant.

Gate charging losses and hence efficiency depend on the switching frequency of the four output stages, as shown in Figure 8. At low frequency, efficiencies converge as loss mechanisms are dominated by on-resistance, which is identical for all output stages. At high frequencies the efficiencies diverge along with the switched gate area in Table I.

VI. Conclusion

The use of N/N totem pole Class-D output drivers in low voltage technology is shown to be feasible and implementable without violating any gate-oxide reliability rules or requiring additional circuitry such as level shifters. Simulation results have shown that the new N/N drivers can achieve higher efficiency than P/N drivers, and are more suited to low voltage processes than other published N/N drivers.

TABLE I

Performance comparison of this work* and other works.

	PN	NN [5]	AD/BD*	AD*
Driver on-resistance (Ω)	3	3	3	3
Pre-driver gate area (μm^2)	280	150	190	200
Output device gate area (μm^2)	690	380	330	330
Switched gate area (μm^2)	970	530	520	530
Diode/capacitor gate area (μm^2)	0	1725	1620	1500
Total gate area (μm^2)	970	2255	2140	2030
Efficiency at 100MHz (%)	79.2	82.6	83.4	82.8

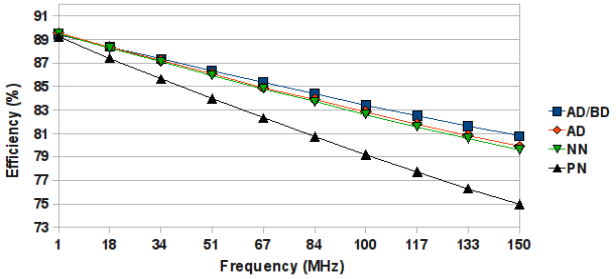

Fig. 8. Simulated H-bridge efficiency variation with switching frequency.

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A Wide Band CMOS Class-D Line Driver for Wireline Communication

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***Abstract*— A wide band Class-D line driver for wireline communications is presented in a low voltage CMOS technology. The new driver improves switching frequencies by a factor of six compared to other works. To reach wide bandwidths, a new NMOS only output stage and a new transconductor are developed. Simulated results of the complete line driver implemented in 0.13μm CMOS, with a 30MHz HomePlug AV input signal and 160MHz switching frequency, show an efficiency of 22.8% with 111mW injected power.**

I. Introduction

Wireline communication systems such as HomePlug AV [1] or VDSL2 use wide communication bandwidths of up to 30MHz. The use of OFDM modulation results in a high peak to average signal value, so traditional Class-AB line drivers are inherently inefficient. An alternate structure, the Class-D driver, has no theoretical inefficiency and in practice is limited only by parasitic losses. While the Class-D driver is well known in audio applications [2] where it is optimized for low frequency operation, the use of Class-D for communication systems introduces different challenges.

To achieve sufficient linearity from a Class-D output, oversampling must be used. In communications systems, the required oversampling ratio (OSR) is typically around 3-8, but in wireline communication applications, this increases the switching frequency by a factor of 6-15 above previous results from similar ADSL communications systems [3]. The use of fine-scale, low voltage, high-g_m digital processes is necessary as they are inherently faster than older and higher voltage processes. Additionally, wireline communication systems are moving towards single chip solutions [4], so a line driver implementation in the same digital CMOS process as the digital core is highly desirable.

However, line drivers are fundamentally high power devices, but the low supply voltage of high speed digital processes coupled with parasitic supply and output resistances and transformer losses, limits the power that can be injected. A high voltage supply is thus required in order to achieve the required injected power at an acceptable efficiency.

One technique used to address this problem is to split the Class-D core supply voltage and output supply voltages. Shown in Figure 1, the Class-D line driver structure is configured as a self-oscillating amplifier with separate low voltage core supply V_{DDL} and high voltage output driver supply V_{DDH}, and a half-bridge output. The Output Driver

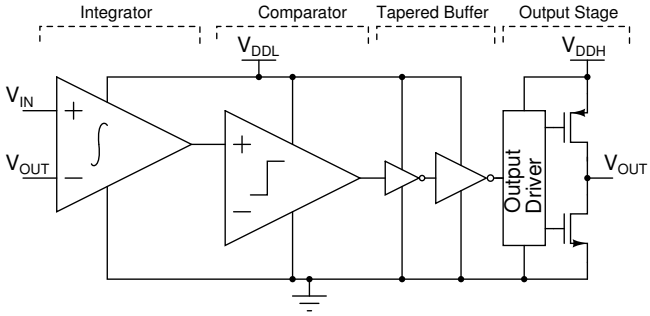

Fig. 1. Conventional P/N totem pole Class-D in single ended configuration.

translates a low voltage switching signal into a high voltage signal appropriate for the output stage. Although shown with a P/N totem pole output stage, other variants are possible such as the stacked output stage [5]. The stacked output stage is desirable from a cost point of view as it is implemented entirely with low voltage digital devices, but unfortunately its complexity makes it too slow for wide band systems. Thus, simpler and faster high-voltage tolerant output stages such as [6] are more appropriate in this application.

A problem introduced when splitting the output and core supply voltages is the implementation of the feedback path and wide bandwidth integrator. The most common structure, shown in Figure 2, uses a closed loop op-amp with input resistor to convert voltage into current which is integrated on a capacitor. However the implementation of the op-amp is challenging at very high frequencies. A higher frequency approach, shown in Figure 2b, uses a linearized transconductor and integration capacitor, but is difficult to maintain linearity over a wide input swing with conventional transistor-input transconductors, and split supply operation requires additional circuitry, such as a potential divider, to limit the input voltage swing.

In this paper, we present a new self-oscillating Class-D line driver for 30MHz HomePlug AV signals. The line driver core is implemented with 1.2V devices, but 3.3V I/O devices are used for the output stage. In order to maximize loop switching frequency and to minimize switching losses, the output stage is implemented with only NMOS devices, approximately halving the driven gate area compared to a P/N totem pole, and so reducing the power consumption of the tapered buffer and output driver. Further, in order to address the frequency and

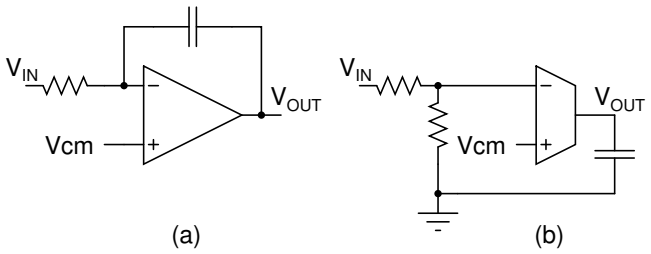

Fig. 2. Common feedback-integrator structures for high-to-low supply translation.

linearity compromise of conventional feedback and integrator structures, a new current-mode structure is proposed which uses a NMOS-only signal path to achieve wide bandwidth and a large input range.

In Section II we present the theoretical motivation for the work and examine the main requirements for realizing wide bandwidth Class-D systems. In Section III we will present two circuits which make high frequency Class-D practical. Section IV will present simulated results from the new line driver structure. Comparisons with other published communications line drivers will be given in Section V.

II. Background

The self-oscillating line driver architecture shown in Figure 1 oscillates at the frequency where the phase shift around the loop reaches 180 degrees. The two main contributions to loop phase shift are the integrator phase shift, $\phi(f)$, and the phase shift that results from the delay through the comparator, tapered buffer chain, output driver and output stage, t_d.

The self-oscillating frequency is typically much greater than the integrators dominant pole position, so assuming a non-dominant pole at frequency f_{nd}, the overall integrator phase shift can be written as:

$$\phi(f) \simeq 90 + \frac{180}{\pi}\left(\tan^{-1}\left(\frac{f}{f_{nd}}\right)\right) \quad (1)$$

Similarly, the phase shift due to delay t_d can be written as:

$$\Phi(f) = 360\,(t_d \times f) \quad (2)$$

The phase shift as a function of frequency for both equations has been plotted in Figure 3, for a range of t_d and f_{nd} values. The phase contribution of f_{nd} has been plotted as $180 - \phi(f)$ in order to aid graphical interpretation. For particular values of f_{nd} and t_d, the loop will oscillate at the frequency where $\phi(f) = \Phi(f)$.

In order to achieve high switching frequencies greater than 100MHz, t_d must be reduced. Efficiency trade-offs for a 50Ω load determine the output stage sizing and, in turn, the sizing and number of stages of the output driver and tapered buffer. Collectively these determine t_d. To decrease t_d while maintaining the same output stage impedance, output devices with a higher g_m per unit area are required, presenting a smaller load to the tapered buffer chain and allowing for a shorter, faster structure.

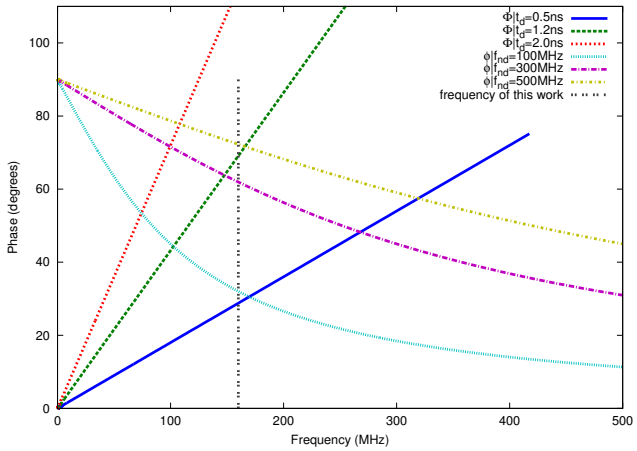

Fig. 3. Delay t_d and integrator non-dominant pole f_{nd} loop phase shift contributions as a function of frequency. Self-oscillation occurs at the intersection of Φf and ϕf. The frequency of this work is shown by a vertical line at 160MHz.

However, there is a limit to the availability of higher g_m devices, and as t_d reaches its minimum for a given process, driver architecture and load size, the intersection of $\phi(f)$ and $\Phi(f)$ becomes determined by f_{nd}. In order to practically achieve high switching frequencies greater than 100MHz with an estimated minimum $t_d = 1ns$, an wide band integrator with a non-dominant pole above 300MHz is required.

III. Circuit Overview

A. High-voltage output stage and driver

A high-voltage output stage using 3.3V I/O devices has been implemented, and is shown in Figure 4. In order to minimize gate capacitance and delay, an N/N totem pole replaces the conventional P/N totem pole, halving gate capacitance. The pull-up device requires a gate voltage twice the high supply, so to drive the output devices, a development of [7] is used, with modifications to accept low, 1.2V, input signals.

The output stage is a full-bridge driver with positive ($M_{H1/L1}$) and negative ($M_{H2/L2}$) outputs. Transistors $M_{LV1/2}$ and $M_{IN1/2}$ implement a 1.2V-3.3V level shifter, with $M_{PR1/2}$ preventing the drains of the input devices from experiences voltages greater than 1.2V. $M_{CP1/2}$ and $C_{PUMP1/2}$ implement a charge pump. Finally, $M_{PH1/NH1}$ and $M_{PH2/NH2}$ implement multiplexers, selecting either the pumped capacitor top-plate or the low output voltage to be applied to the pull-up output device. The pull-down output device requires only a 0-3.3V gate drive so can be driven directly from by the level shifter output.

B. Wide-band, wide-input-range transconductor

For implementing wide band transconductors, the open loop configuration shown in Figure 2b is the dominant topology. In order to improve their linearity, super-linear source follower techniques, which increase the effective g_m of the input devices, have been proposed [8].

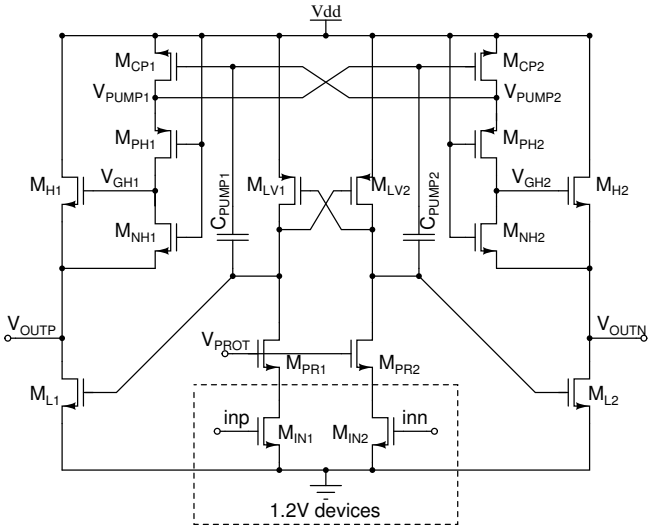

Fig. 4. 3.3V N/N totem-pole output stage with driver circuit and 1.2V input. Unless otherwise specified, transistors are 3.3V I/O devices.

A development of this approach, shown in Figure 5, uses an all-NMOS boosting loop ($M_{N4,N1C,N1A}$) to linearize an NMOS source follower (M_{N3}), with PMOS devices ($M_{P1A/B}$,$M_{P2A/B}$) used only for DC biasing. The use of only NMOS devices in the signal path allows for for higher frequency operation than mixed NMOS-PMOS loops. Additionally, rather than using the source follower to buffer the input voltage on to a resistor for V-I conversion, the approach presented here fixes the gate of the source follower at a bias voltage, V_{REF}. This also fixes the gm-boosted, low impedance source follower output node V_X, which provides a suitable point for connecting one terminal of a V-I conversion resistor R_{IN}, the other terminal of which is driven directly by the transconductor input V_{IN}. The g_m boosting loop also provides a suitable NMOS mirror point to mirror the current I_{IN} from the boosting loop to the output, through M_{N1C}-M_{N1B}.

A pseudo-differential implementation of this structure is used, consisting of a transconductor stage for each input and a common mode output feedback loop through M_{P1B}.

IV. Simulations

A complete line driver, a fully differential version of the structure shown in Figure 1, has been implemented in a 0.13 μm CMOS process from UMC with eight metal layers. The high supply is 3.3V and the low supply is 1.2V. The new N/N totem pole output stage and driver are used, as is the new wide-band, large input range integrator. Figure 6 shows the simulation configuration. A fifth order Chebyshev LC filter is used at the line driver output, to remove output switching energy and to ensure compliance with HomePlug AV EMC requirements. Bondwires and pad/pin capacitances are modeled with a pi-network. In order to decrease bondwire inductance, four parallel bondwires are used for all 3.3V pins.

In order to achieve a target injected power of -53dBm/Hz RMS while maximizing efficiency, modeling determined the optimum load resistance to be 3.125Ω. Thus, a 1:4 step up transformer is also required in order to transform the 50Ω line impedance to 3.125Ω.

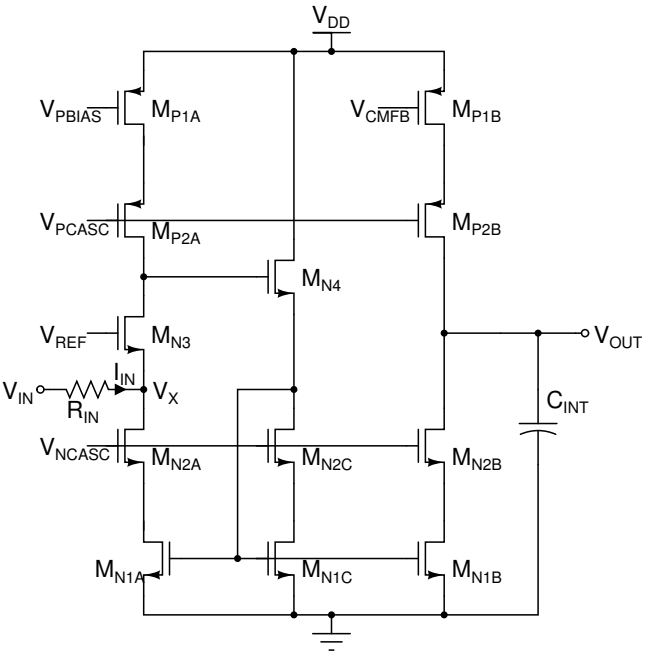

Fig. 5. Wide-band, wide-input-range transconductor

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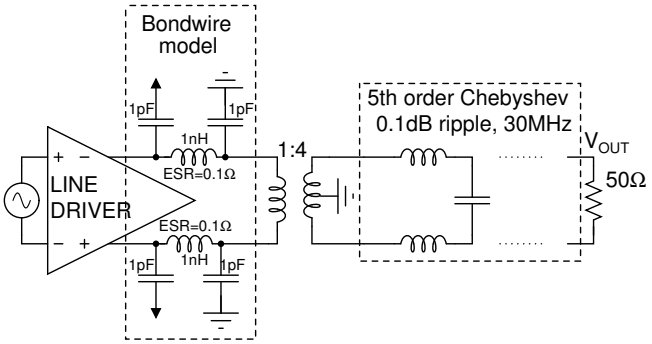

Fig. 6. Simulation configuration.

The differential input signal applied to the line driver input is a QAM-modulated 917 carrier OFDM signal between 2MHz and 30MHz, with EMC-compliance notches.

V. Performance

Simulation of the line line driver finds that the comparator, tapered buffer and output stage have a delay of 1.2ns, and the integrator non-dominant pole is at 524MHz. The resulting self-oscillating frequency is 160MHz.

Figure 7 shows the Missing Tone Power Ratio (MTPR) plot of the line driver output, measured across the 50Ω line model load. The plot shows an injected power of -53dBm/Hz RMS, with a worst case MTPR of 31dB over the 2-30MHz signal band. The power consumption from the 1.2V supply is 4.6mW,

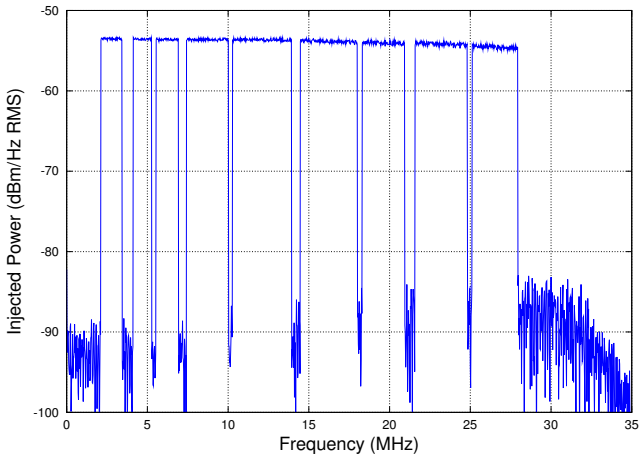

Fig. 7. MTPR of line driver output with 30MHz 7th order Chebyshev low pass filter and HomePlug AV input.

TABLE I

PERFORMANCE COMPARISON OF THIS AND OTHER WORKS.

	This work	[3]	[5]	[9]
Supply voltage (V)	+1.2,+3.3	3.3	1.2,5.5	± 25
Technology (μm)	0.13	0.35	0.13	0.7
Injected Power (mW)	111	100	100	100
Bandwidth (MHz)	30	8.5	2.2	1.1
Fswitch (MHz)	160	19	25	4.7
Efficiency (%)	22.8	47	42	40
Linearity (MTPR, dB)	31	56	58	40

and from the 3.3V supply is 482.2mW. This gives an efficiency of 22.8%.

A comparison of the new line driver with a selection of existing state-of-art line drivers is given in Table I. The other line drivers all target DSL applications, which share a number of similarities with HomePlug AV.

While all the line drivers examined inject a similar power, the bandwidth of the new line driver reported here is greater than the next widest bandwidth driver by a factor of three. A different linearity-switching frequency optimization versus the other works means the switching frequency in this application is six times higher than the next highest frequency loop. This has implications for the efficiency, as Class-D losses are mainly due to charging/discharging of parasitic capacitances in the output stage and tapered buffer, and so are strongly dependent on switching frequency. Given the considerably higher switching frequency, an efficiency significantly lower than that reported for DSL drivers would be expected, but the low voltage tapered buffers and NMOS only output stage ameliorate the efficiency degradation and the new line driver reports an efficiency of 22.8%. The linearity of the new driver is below that of the other drivers, due to the lower OSR and loop order. In [3], three integrator stages are used and in [5], a higher OSR is used. While both techniques improve linearity, both techniques are also impractical for high frequency loops. The switching frequency of [9] is much lower than here, so switching non-idealities are proportionally less, improving the achieved linearity. However, wide band systems typically require lower linearity than narrow band systems - 30dB MTPR in HomePlug AV versus 55dB ADSL - and the linearity reported here is sufficient for the intended application.

VI. CONCLUSION

The use of Class-D line drivers for wide band wireline communication systems has been shown to be feasible in low-voltage CMOS processes, and capable of achieving high efficiency and high output power. To achieve this, high-speed NMOS-only circuits are vital, as is appropriate segmentation of supply voltages through the system, using a low voltage supply for the high speed analog processing, and a high voltage supply for a high power output. Simulation results of the new line driver have reported efficiencies comparable to other published drivers, despite a significantly wider bandwidth and higher switching frequency.

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