A Novel Test Structure to Monitor Electromigration

M.RAVINDRA

Ph.D. Thesis

Edinburgh Microfabrication Facility
Department of Electrical Engineering
University of Edinburgh
Edinburgh

1992

Abstract

Electromigration continues to be one of the important failure mechanisms limiting the attainment of higher levels of reliability in sub-micron geometry VLSI circuits. Successful management of electromigration in future requires adoption of effective statistical process control techniques, in addition to the traditional quality control tests and inspections. The aim of this project was to develop a test structure and test methodology to monitor electromigration for metallisation process control.

Based on analysis and some preliminary measurements on chequerboards, a new test structure and methodology was proposed to monitor electromigration. 'Chequerboards' are dense patterns of clear and opaque squares of metal film over silicon.

As part of this study, an electromigration test chip was designed. It consists of two designs: The design EU9101 mainly contains chequerboards while EU9102 contains conventional and other electromigration test structures for comparative assessment. The chip design, fabrication and measurement details including the instrumentation aspects are also given in the thesis.

One of the key process parameters, namely, linewidth is chosen to demonstrate the sensitivity of the proposed methodology to monitor electromigration. Possible applications of the new structure in electromigration measurements, other than process monitoring are also discussed. The thesis also contains a review of the electromigration measurement techniques, some measurements using the conventional test structure and a detailed discussion on the limits of conventional tests.

DECLARATION

I declare that the thesis has been composed by myself and that, except where stated otherwise, the work presented is my own.

M.RAVINDRA

To my parents.

Acknowledgements

I am very grateful to my supervisor, Professor John M.Robertson, for his very valuable guidance throughout the research work, his help and advice during my stay in Scotland and above all for providing a very good training in scientific analysis and reporting.

I thank my second supervisor, Dr.Les Haworth for his useful comments on the many reports written during the initial stages of the project and also for his help and advice. I would like to express my deep gratitude to Dr. Robert J.Holwill for critically reviewing the thesis and offering many useful suggestions. I am also grateful to Mr.Alan M.Gundlach for the advice on fabrication matters and, to Messers Alec Ruthven, Mike Fairgrieve, Brian Neilson, Dave Hope and J.D.M. Fraser for their technical and general help. I would like to thank Dr.A.J.Walton, Mr.W.Gammie, Mr.Z.Chen and all the EMF staff for their assistance and also I thank my friends Raymond Bienek, Anthony Chester, Nicos Porfiris, Robin Smith, Godfrey Gaston, John Thom, Robbie Hannah and Stewart Robertson for their co-operation and support.

I am very grateful to my parent organisation, the Indian Space Research Organisation for sanctioning the necessary leave and to the commonwealth commission in the U.K. for awarding the scholarship. Finally, I would like to thank all my family members for the continued encouragement throughout my research work. I thank my wife for typing the thesis and providing the necessary moral support.

Chapter 1

Introduction

The quality and reliability requirements of present day integrated circuits(ICs) is increasing inexorably. The demand for higher speed, low power consumption and lower cost per gate has been the driving force to go for higher and higher levels of integration, development of new materials and processes and innovative designs. So far the tremendous advance in IC manufacturing techniques has not only offered improved performance and low cost, but improved reliability as well [1]. This improvement in reliability has not often been achieved easily. New technologies and processes have presented new challenges and failure mechanisms. So, new solutions have to be evolved to combat these problems [2]. The same trend is expected for future generation VLSI circuits.

1.1 Technology Trends

1.1.1 Level of Integration

Since 1965, IC complexity has advanced from Small-Scale Integration (SSI) through Medium-Scale Integration (MSI) and Large-Scale Integration (LSI) and to Very-Large Scale Integration (VLSI) which has 10^5 or more components per chip. Figure 1–1 shows the remarkable growth achieved in DRAM (Dynamic Random Access Memory) packing density over the past few years and the expected trend [3]. The

packing density roughly quadruples every 3 years ("Moore's law"), and at this rate 1024 MDRAM (M for megabits) should be available by the year 2001. Of course no exponential growth can continue indefinitely. Limits may be imposed by physics, manufacturability, cost, performance and reliability. One objective of this thesis is to analyse one aspect of reliability measurement and specification.

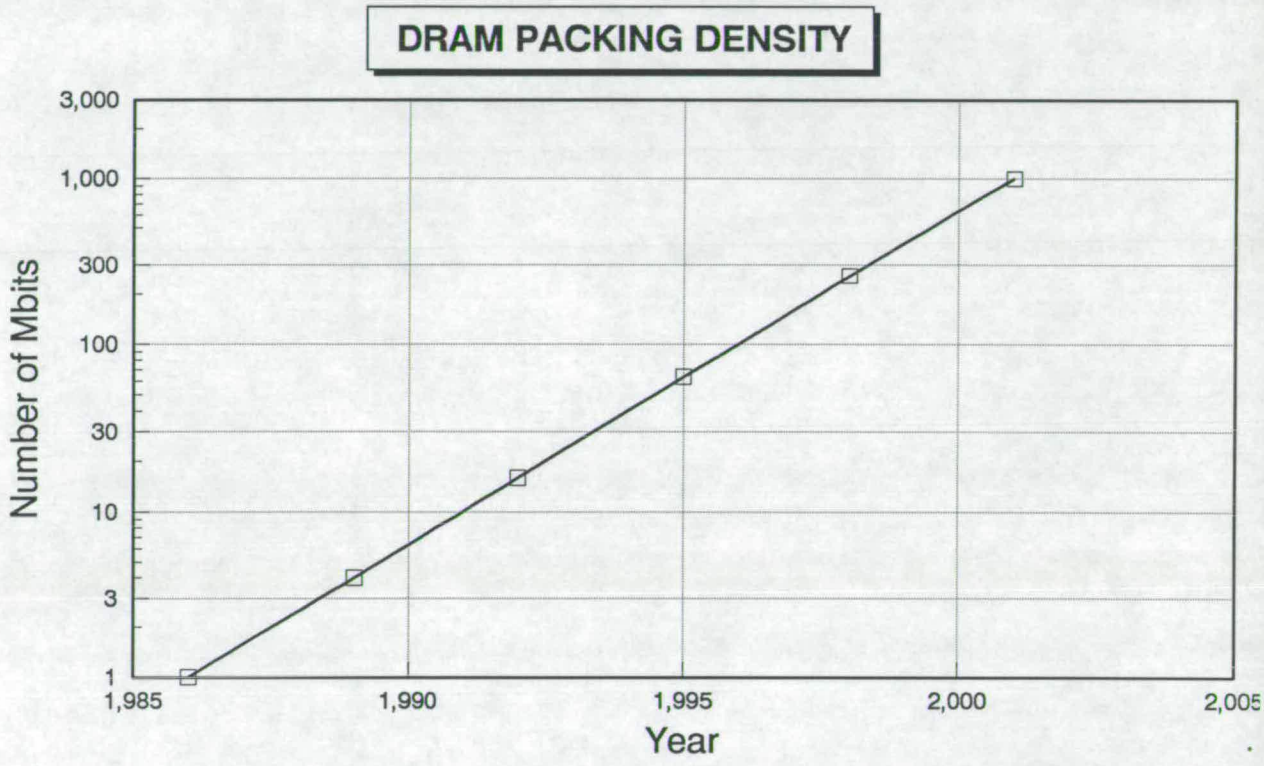


Figure 1–1: Trends in level of integration

1.1.2 Minimum Linewidth

The most important factor in achieving very high component density is the continued reduction of the minimum linewidth as shown in Figure 1–2 [4]. At this rate, the minimum linewidth is planned to shrink to about 0.2 μm in the year 2000.

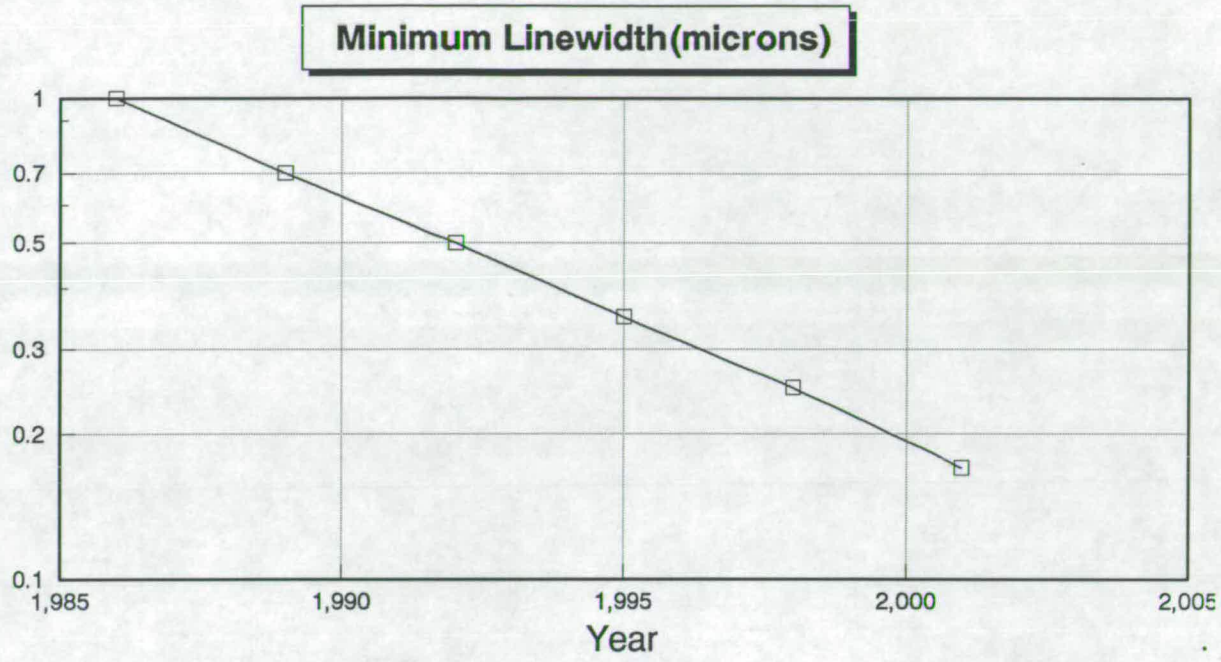


Figure 1–2: Trends in minimum linewidth

1.1.3 Reliability Levels

In spite of the ever-increasing complexity, the reliability of ICs is continually increasing. This is reflected in the decreasing failure -rate[1] goal of a manufacturer achieved over the years, as shown in Figure 1–3 [5]. 1 FIT corresponds to 1 failure in 10^9 device-hours of operation. The failure rate indicated here is that in the 'working life' period. This ('working life' period) is defined in the next section.

Although manufacturers may all have slightly different failure rate goals, customers will have a tendency to drive all the manufacturers to match the failure rate goals of the few most aggressive manufacturers. Therefore, all failure rate goals should tend to converge, but continue to decrease. Like Moore's Law for chip

[1] ratio of number of ICs failing per unit time to number surviving at any instant of time

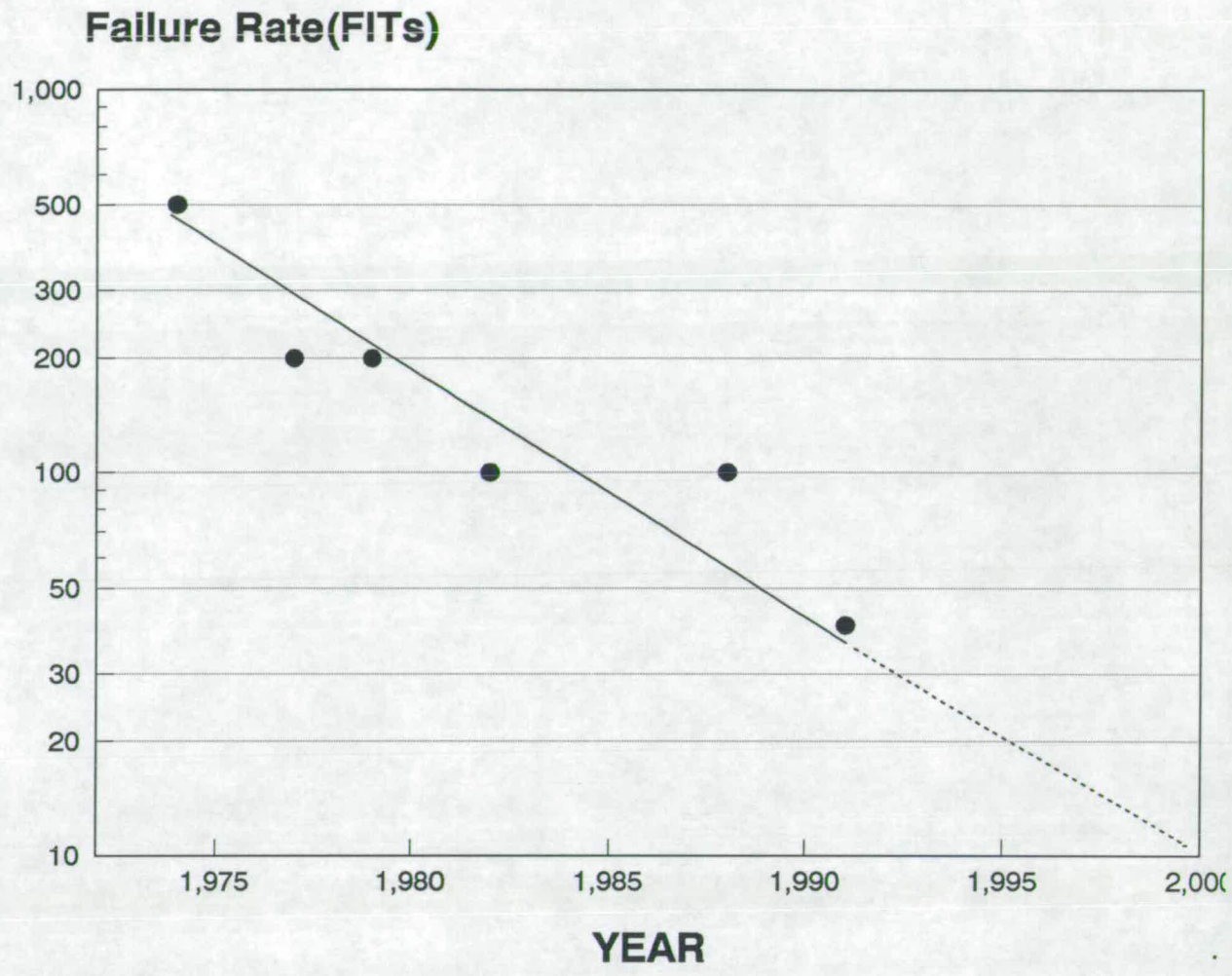


Figure 1–3: Failure rate goal of a manufacturer versus time

densities, it appears that these market forces have also established an empirical law that govern the reliability performance.

Based on the projection in Figure 1–3, VLSI circuits failure rate goals at the turn of the century should be approximately 10 FITs.

1.1.4 Reliability Improvement Approaches

The 'bathtub' curve

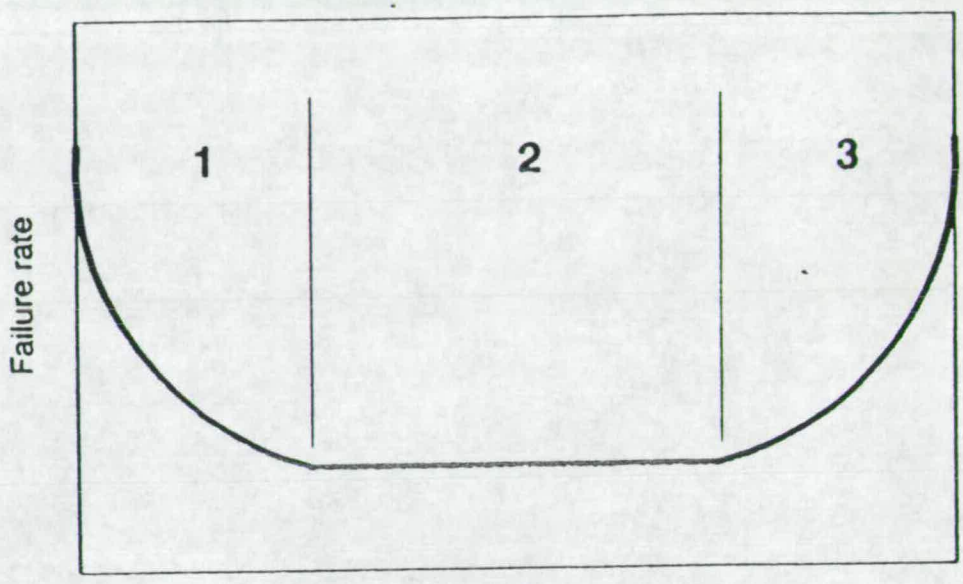
The conventional representation of the variation of failure rate of mechanical components with time is shown in Figure 1–4. This is commonly known as the 'bathtub' curve. However, for IC performance failure can be more realistically represented by 4 regions as shown in Figure 1–5 [6] :

Region 1:

The failures in this region are caused by quality-related defects ("killer defects"), workmanship problems etc. Examples of such defects are oxide pinholes, photoresist or etching defects resulting in near-opens or shorts, weak die bonds, weak wire bonds, partially cracked packages. These defects cause yield losses that occur during the initial device testing period.

Region 2:

The failures in this region are caused by parametric degradations. Components which marginally meet the upper and lower parameter specifications (for example, threshold voltage) may fail during this period. For semiconductor components 'screening' tests are carried out to weed out such 'weak' devices. Examples of such generally used screening tests are, high temperature storage, 'burn-in', thermal cycling, centrifugal spinning, package leakage tests (hermeticity). Ideally the test time and temperature should be selected based on the specific failure mechanisms for a given technology and process and the corresponding activation energy. In practice, the general test conditions specified in military standards are used [7] since they represent a general catch - all standard. For example a typical high temperature storage test at 150°C for 24 hours; 'burn-in' for 168 hours etc.



Conventional representation of the variation of failure rate with time

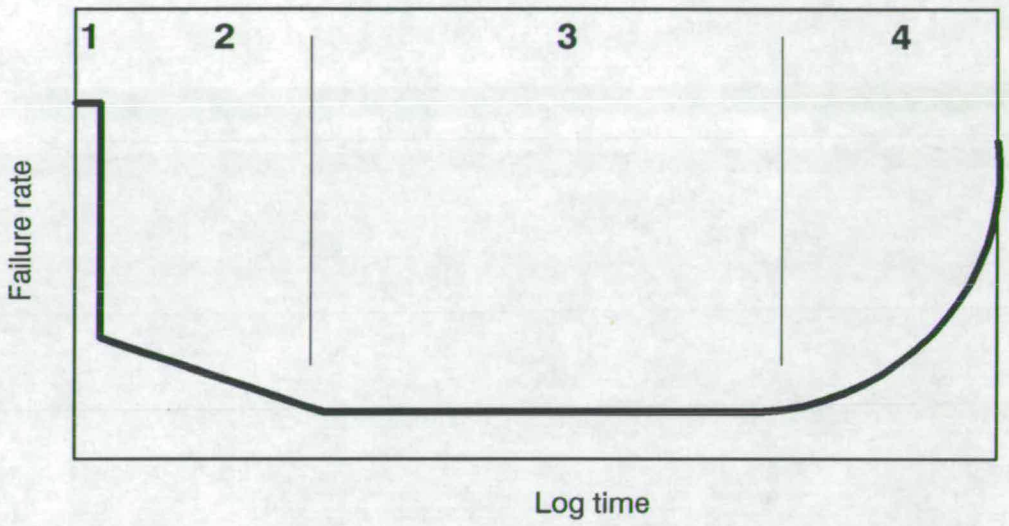
3 Regions

1 Failures controlled by manufacturing

2 Mature life phase; design limits

3 Wear-out phase

Figure 1–4: The 'bathtub' curve



1 Yield due to killer defects

2 Early life parametric failures

3 User-induced failure

4 Wear-out mechanisms

Figure 1–5: The 'IC bathtub' curve

Region 3:

This is the region in which failure rate remains roughly constant. This is also known as the 'useful-life' or 'working-life' period. Failures in this region are caused by 'screening-escapes'.

One typical distribution of failures in this region is given in Figure 1–6.

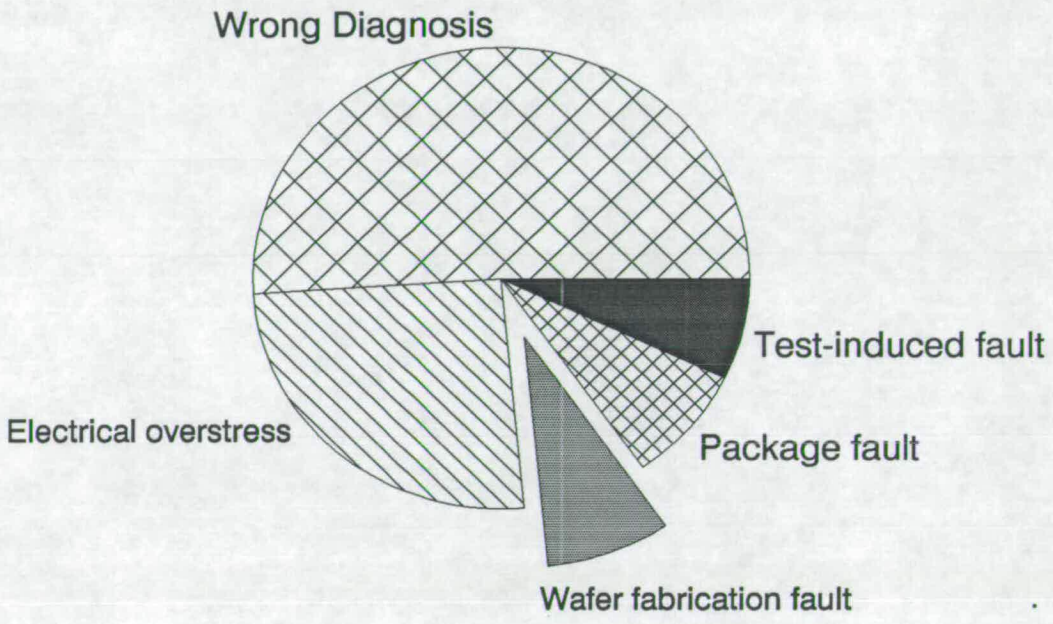


Figure 1–6: Distribution of in-service failures

These data are from a manufacturer's product reliability report [8]. From this figure it is clear that a large percentage of failures are due to wrong diagnostics or misuse of the device and a very small percentage of failures can be attributed to intrinsic degradation processes. This implies that the inherent reliability of the present generation of ICs is quite high, in spite of the ever-increasing complexity. However, this does not mean that the future generation VLSI circuits can easily meet the projected reliability specifications shown in Figure 1-3.

Region 4:

This is the region in which failure rate increases with time. This is also known as the 'wear-out' region. Electromigration - the subject of this thesis - is a good

example for a failure mechanism in this region. The failure rate due to 'wear-out' is expected to be very low during the 'useful-life' period of a component. However, improper design, materials, process and/or test conditions can cause wear-out failures during the typical 'useful-life' period.

The mathematical details of the common distribution functions (Log-normal, Weibull etc.) used to represent these regions are given in Appendix C.

Traditional versus present trends

Traditionally, screening tests have been used to improve the reliability levels of ICs. For example, consider the general reliability level classification used by US military standards such as class S (high reliability components for critical space applications) or class B (for less critical airborne or ground applications). These are mainly specified in terms of the screening test specifications. For example, 168 hours burn-in for class B, 240 hours burn-in for class S etc. However, failures caused by manufacturing variations and occurring during actual field use can not always be eliminated by screening. Such failures are noticed even after high-reliability screening tests. The whole methodology of end- of-line screening to achieve high reliability is now being questioned.

The trend now is to 'design-in' and 'build-in' reliability and to depend less and less on screening tests. Designing-in and building-in reliability includes use of conservative design rules, quality assurance of the materials, and statistical process control. Efforts are underway to modernise the procedure for qualification of military high reliability microcircuits based on inline process monitoring of every wafer [9].

Device or circuit parameters	Constant electric field scaling	Constant voltage scaling
Device dimensions	$1/\alpha$	$1/\alpha$
Gate density	α^2	α^2
Supply voltage	$1/\alpha$	1
Current	$1/\alpha$	α
Power/gate	$1/\alpha^2$	α
Power density	1	α^3
Current density	α	α^3
Electric field	1	α

Table 1–1: The effects of scaling on electic field and current density

1.2 Scaling Trends and Wear-out Problems with VLSI circuits

The shrinking in device geometries to achieve high packing densities is based on the so-called 'scaling rules' devised to preserve the operating characteristics. The scaling procedures and effects of these on electric field and current density in MOS devices are summarised in Table 1-1.

From Table 1-1 it is clear that current density increases by a factor of α for constant field scaling and as α^3 for constant voltage scaling. There is an increase in electric field by a factor of α for constant voltage scaling and no increase in electric field for constant field scaling (apparent from the name). This implies that the electric field dependent wear-out mechanisms such as time-dependent dielectric breakdown (TDDB) and hot-electron effects and current density dependent wear-out mechanism– electromigration– are likely to be the most important wear-out failure mechanisms in the future complex VLSI circuits [10,11].

If the power supply voltage is scaled down as indicated in Table 1-1 for constant field scaling, then TDDB and the hot-electron effects should not worsen with

scaling. However the trend is to scale down power supply voltage more slowly than device dimensions at some expense of power dissipation. The main reasons for this compromise are:

1. Non-standard supply voltages impose serious end-use compatibility problems

2. Reduced supply voltages imply reduced threshold voltages and therefore even tighter control over implant conditions.

Additionally the reduction in supply voltage is limited by built-in junction voltages which can not be scaled. Hence TDDB and hot-electron effects may still continue as dielectric wear-out problems of future complex VLSI circuits.

Both constant field scaling and constant voltage scaling result in increased susceptibility to electromigration. This is because of the increased current density in the case of constant field scaling and the drastic increase by a factor α^3 in current density and power density, in the case of constant voltage scaling. Power density leads to temperature rise in the chip and hence more rapid electromigration failure.

Gardner [12] has worked out the impact of the above 'scaling-rules' on median time to failure (this is denoted by MTF and represents the time for 50% failures to occur) due to electromigration in MOS devices using the well known Black's equation. The results of his analysis are shown in Figure 1–7. It is clear from this figure that as geometries shrink (i.e, scale factor increases) electromigration poses a serious threat to IC reliability. The problem is much more severe because, in addition to the obvious current density increase due to scaling, current crowding effects at steps and vias cause further reduction in the median time to failure.

The technological solutions offered to increase the MTF are to use multilayered structures where aluminium-alloy films are alternated with refractory-metal/alloy films such as titanium, tungsten etc. However the microstructural, metallurgical and chemical interactions between the layers is quite complex. Firstly, the exact mechanism responsible for MTF increase is not yet clear. For example, in the case

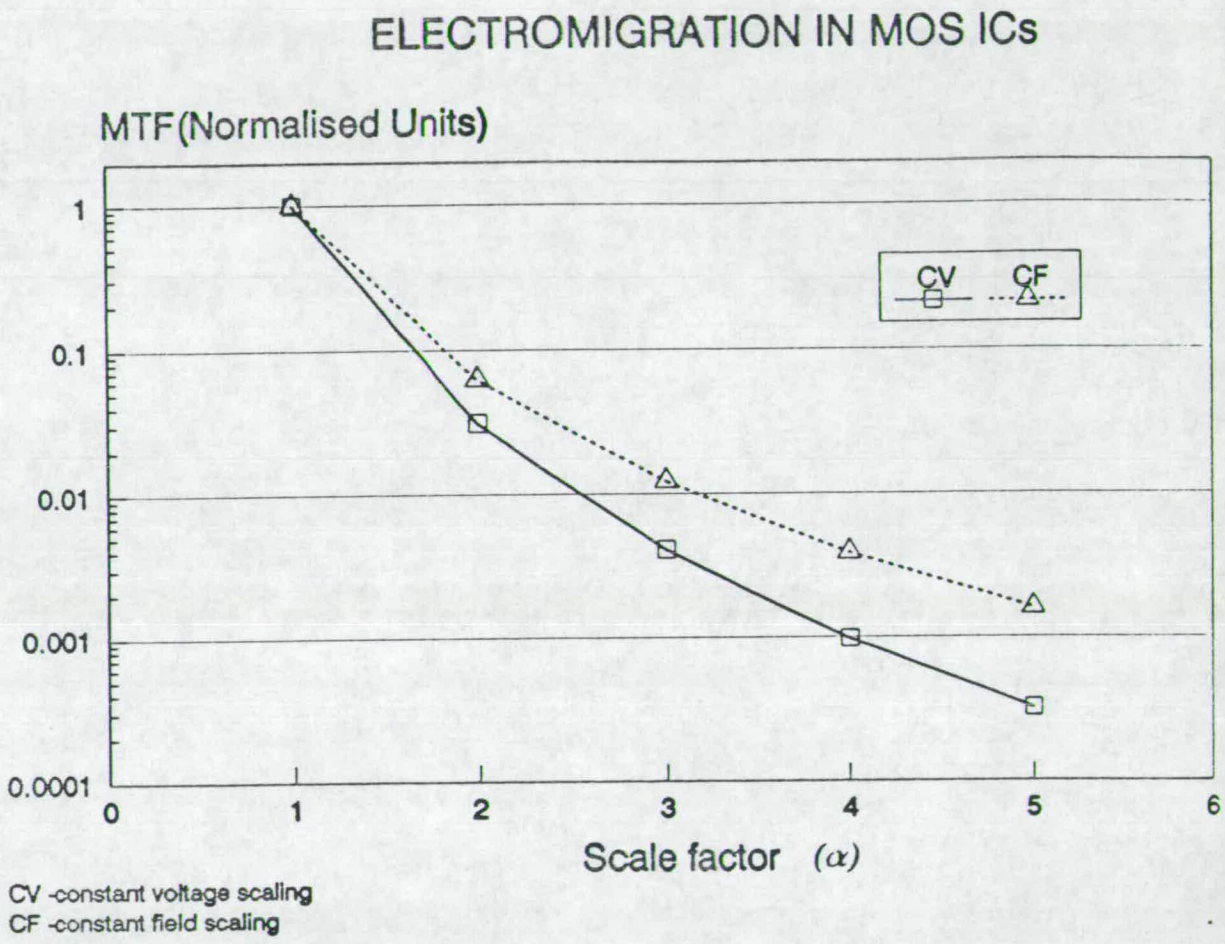


Figure 1–7: Effects of scaling on electromigration MTF in MOS devices

of titanium and aluminium multilayers the MTF increase may be due to the formation of the chemical compound $TiAl_3$ and/or microstructural changes following the heat treatment of the layers [13]. Secondly, some new problems (for example, increased whisker growth with TiW and TiN films) arise with these layers. Therefore, new solutions have to be found. Hence single layer aluminium-alloy films are not obsolete. Even though aluminium-copper films are more resistant to electromigration, these have dry etch, corrosion and Schottky contact problems [14]. In summary, aluminium-silicon alloys are likely to continue as the interconnect material for some time to come [15].

1.3 Electromigration Monitoring Requirements

Electromigration has traditionally been measured through MTF tests and post mortem failure analysis, but these will be of limited use in future. This is mainly because such techniques can not be used to ensure the required electromigration resistance of the metallisation on every wafer in a lot and also because of cost and time considerations since typical test times may range from weeks to months.

A more fundamental approach to improved reliability would be by monitoring the quality of the materials and strictly controlling the process variables to target specifications. Although this sounds attractive and is very much in line with the best manufacturing practice for improved quality and reliability, it is not yet feasible because electromigration is affected by a large number of material and process parameters and the interactions between these is not always obvious. Figure 1–8 is a ' fishbone-diagram' showing the major material and process parameters affecting electromigration performance. Each of these may depend on a number of other parameters. For example, effective width on exposure control, photoresist thickness, and photoresist thickness on spin rate etc. It should be borne in mind that this is a simplified representation of the various factors affecting electromigration; the interdependence of many factors is not shown and in many cases it is not completely understood. For example, the presence of refractory metal layer over

aluminium may modify the grain structure during heat treatment, in addition to other mechanisms in increasing the MTF.

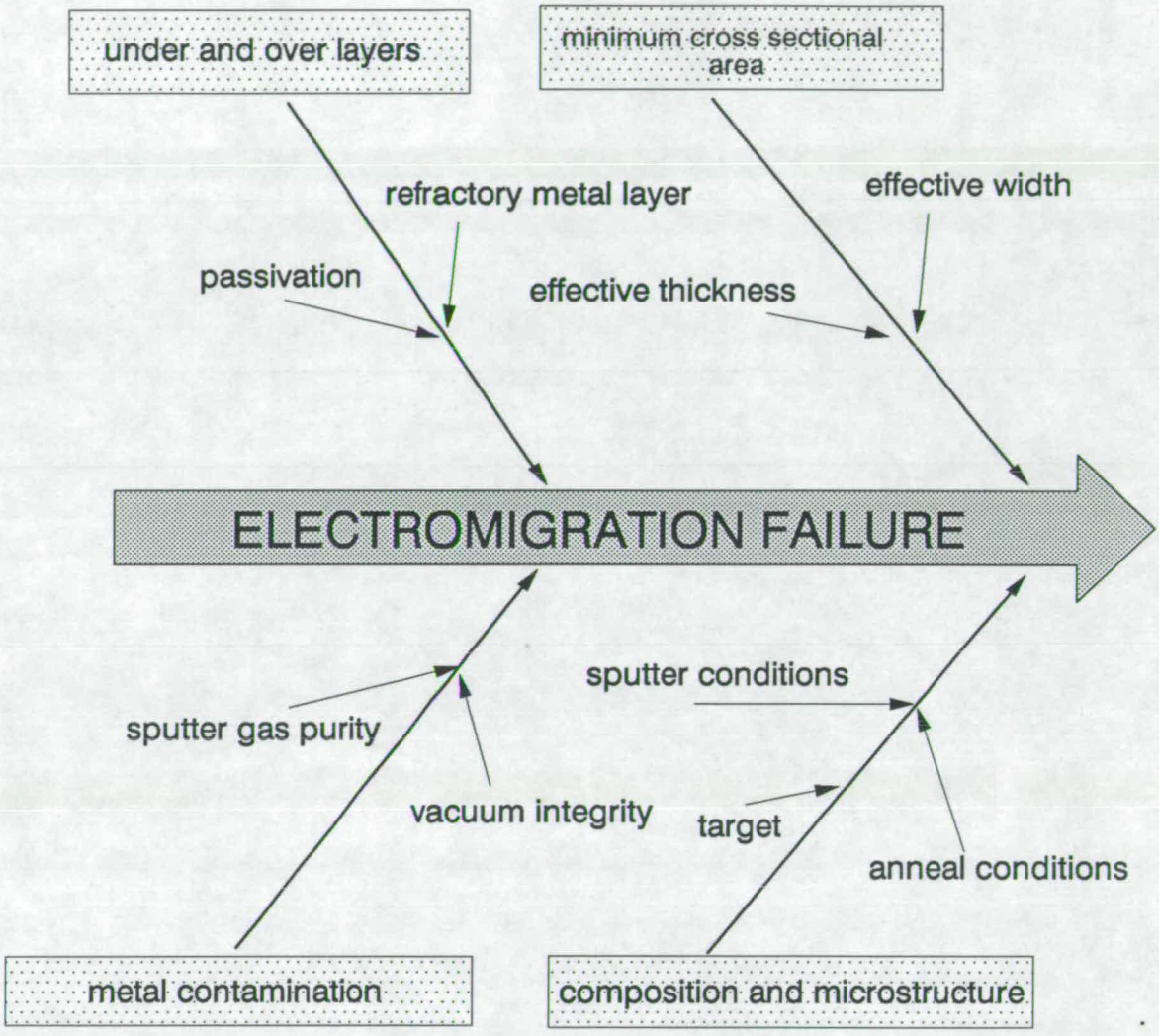


Figure 1–8: Material and process parameters affecting electromigration

1.4 Aim of the Project

There is a strong need to develop a reliable process control test structure and test methodology to monitor electromigration for the reasons given in the previous section.

The main aim of the project was to develop a test structure and technique keeping in mind the following requirements: it should meet the compatibility requirements of a process monitor chip, sensitive to various factors that affect electromigration lifetime and should be usable to characterize 'sub-micron' metallisation geometries of the future complex VLSI circuits. By compatibility requirements it is meant that it should be possible to produce the new test structures with other test devices and to obtain test results quickly, preferably without using a hot chuck.

An additional objective of the project was to use the new test structure to develop statistical techniques to estimate the MTF of small segments of conductor in which current crowding effects are significant. The future VLSI circuits are most likely to contain a large number of such small segments such as bends, vias etc. and hence it is very likely that the circuits will be analysed for any loss of reliability inherent in the design.

Bibliography

[1] F.Fantini. Reliability problems with VLSI. *Microelectronics and Reliability*, 24(2):275–296, 1984.

[2] P.Brambilla et al. CMOS reliability: a useful case history to revise extrapolation effectiveness, length and slope of the learning curve. *Microelectronics and Reliability*, 21(2):191–201, 1981.

[3] J.M.Robertson. Private communications.

[4] S.Asai. Reliability and yield in MOS VLSI. *IMEC(Belgium) summer course*, 1989.

[5] D.L.Crook. Evolution of reliability engineering. *Reliability Physics, IEEE Annual Proceedings*, pages 2–7, 1990.

[6] J.Moltoft. Behind the 'bathtub' curve – a new model and its consequences. *Microelectronics and Reliability*, 23:489–500, 1983.

[7] Military standard: Test methods and procedures for microelectronics: MIL-STD-883D . US Department of Defense, Washington, 1988.

[8] SIGNETICS INC. Product reliability report: R363, 1975.

[9] E.B.Hakim. Advancement in complex microcircuit qualification. *Solid State Technology*, (5) :98–100, 1989.

[10] M.Davis and F.Hass. Inline wafer-level reliability monitors. *Solid State Technology*, (5) :107–110, 1989.

[11] P.Weiss. Study, design and test of semiconductor test structures for reliability evaluation of ICs. ESTEC Report, 1986.

[12] Donald .S.Gardner, James D.Meindl, and Krishna C .Saraswat. Interconnect and electromigration scaling theory. *IEEE Transactions on Electron Devices*, ED-34(3) :633–643, 1987.

[13] Hoang H. Hoang. Effects of annealing temperature on electromigration performance of multilayer metallisation system. *Reliability Physics, IEEE Annual Proceedings*, pages 173–178, 1988.

[14] N. P. Armstrong et al. Electromigration alternatives to aluminium-copper. *IEEE VLSI Multilevel Interconnection Conference*, pages 460–468, June 1988.

[15] Dipankar Pramanik and Arjun N. Saxena. Aluminum metallisation for ULSI. *Solid State Technology*, (3) :73–79, 1990.

Chapter 2

Electromigration and Metallisation Reliability

2.1 Background

Reliability studies on microeletronic circuits sponsored by US Air Force in the mid-1960s led to the identification of electromigration in thin metal films as one of the primary failure mechanisms limiting the reliability of film interconnections used in microelectronic devices [1]. This discovery fostered a period of intense activity in the study of electromigration phenomena in thin films which continues to this day [2,3,4]. While the majority of the work on bulk materials was concentrated on the electron-ion interactions and interaction of mobile defects and charge carriers [5], most of the studies on thin films were aimed at the rather practical aspect of conductor line failures in ICs. These studies were carried out on thin films prepared by evaporating metal layers onto insulating substrates and at moderate temperatures of about half the melting point of the metal.

With the rapid advancement in microelectronic materials and processing, new technological solutions were found to improve the electromigration resistance. These include microstructure modifications by various processing techniques (for example, increasing the grain size by using higher substrate temperatures[6]), alloying with other elements like copper [6] and formation of multilayer metallisation systems [7]. These new solutions brought new problems as well; for example, the excess copper forms a compound $CuAl_2$ which is responsible for galvanic corrosion and degradation of Schottky contacts. It also causes dry etch problems. Thus,

addition of copper even though it improves the MTF of the conductor, brings new problems. Similarly multilayered sandwiches of aluminium-alloys with refractory metals/alloys, are prone to new problems because of the complex metallurgical, chemical and microstructural interactions between the layers [8]. For example, the mechanism causing whisker growth with titanium and tungsten multilayer structures is not yet fully understood. Hence aluminium-silicon alloy continues to be used as the most common inteconnect material and will probably continue for some time to come [9]. This means that electromigration continues to be an important wear-out problem.

Historically, the theory of electromigration was developed for bulk metals. However, the same approach can be used for thin films provided some appropriate modifications are made, for example, replacing the lattice diffusion coefficient by grain boundary diffusion coefficient. Hence the theory of electromigration in bulk metals is given first.

2.2 Theory of Electromigration

2.2.1 Bulk Metals

Electromigration is the term applied to the transport of mass in metals when stressed at high current densities. In other words it is the phenomenon of 'current induced atom flux'. The development of electromigration theory has evolved around two components of the driving force causing momentum transfer to the ions of the crystal : electrostatic and 'electron wind'. Early developments of the theory includes the semi-classical model by Fiks [10] in 1959, and by Huntington and Grone [11] in 1961, and the quantum mechanical model by Basvieaux and Friedel [12] in 1962. However the model proposed by Huntington and Grone is still commonly used and hence the salient features of this model are given.

Huntington and Grone [11] made light transverse scratches on the surface of gold wires and then used them as markers to observe motion of gold atoms when

the current density was about $10^4 A/cm^2$. The experiments were carried out at high temperatures, (850°C−1000°C) for periods of several days. They developed a theory to explain the observed current-induced mass transport and its dependence on current density and temperature.

The following expression for the net atomic flux J in a lattice due to current density j was obtained :

$$J = \left(\frac{ND}{kT}\right) Z^* e \rho j \tag{2.1}$$

where,

N = density of ions

D = $D_o exp(-E_a/kT)$= self-diffusion coefficient

E_a = activation energy

k = Boltzmann constant

ρ = resistivity

T= absolute temperature

Z^*e = effective charge on the migrating ion

In the above equation 2.1 the effective charge Z^*e is defined and given by:

$$F \equiv Z^* eE \tag{2.2}$$

where E is the electric field and F is the total force acting on the migrating ion. The total force F consists of two components: electrostatic force ZeE (Z is the valency) and the 'wind force'. The direction of these two forces are opposite to each other. For example, for a positively charged ion, electrostatic force acts in the direction of the electric field, while 'wind force' acts in the direction of electron flow. The magnitude and sign of Z^* indicate the relative strength of the two forces. For instance, in gold the measured value of Z^* is about -7 [13] and since the the valency is 1 this implies that the wind force is about 8 times larger than the electrostatic force.

2.2.2 Thin Films

Electromigration studies in thin films are usually carried out at moderately low temperatures compared to the melting point of the metal, for example, less than 250°C for aluminium and the mass transport is mainly controlled by grain boundary diffusion; mass transport by lattice diffusion is negligibly small. A detailed theoretical discussion of electromigration in thin films is not yet attempted by researchers because of the complexity arising due to the grain boundaries [14].

In the absence of a rigorous theory, the atomic flux expression derived for bulk metals is modified to [15]:

$$J_b = (\frac{\delta}{S})(\frac{N_b D_b}{kT}) Z_b^* e \rho j \qquad (2.3)$$

where, $J_b$is the atomic flux along grain boundaries, N_b is the local density of ions in the grain boundaries, δ is the effective width of the boundaries, S is the average grain size, D_b is grain boundary diffusion coefficient and Z_b^*e is the effective charge. It may be noted that Z_b^* and N_b may not be the same as these parameters in the lattice. Also, migrating impurity atoms often segregate to the boundaries which may modify the value of N_b and Z_b^*.

Expression 2.3 is based on the assumption that in all the grain boundaries mass transport proceeds with the same charactrerstics. However, in a film all grain boundaries are not alike. Typically the grain distribution is lognormal and the grain boundaries are oriented at random. Hence, the grain boundary parameters in equation 2.3 are always considered as suitable averages. These limitations should be borne in mind while using the above expression.

Electromigration causes mass transport along a thin film conductor, but such a displacement alone can not create a discontinuity in the film. For a discontinuity to occur there must be an imbalance in the electromigration flux at some point along the conductor path which is usuually referred to as 'flux divergence'. Flux divergence will occur whenever there are changes in Z_b^* and D_b.

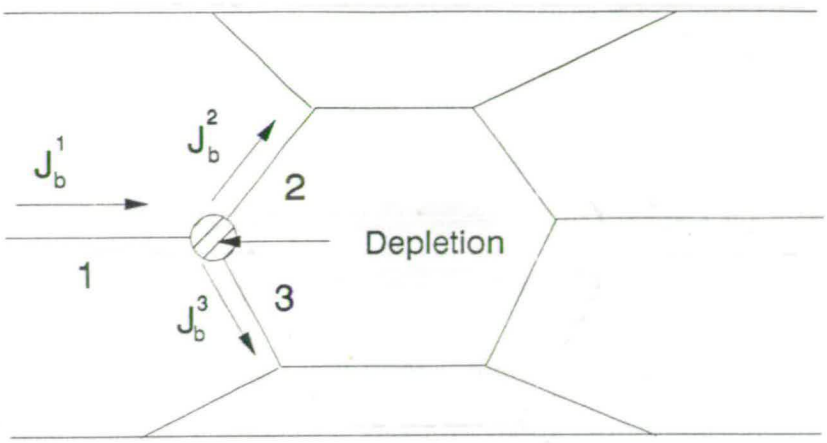


Figure 2-1: Mass transport at a triple point

A typical site in a thin film at which flux divergence occurs is schematically shown in Figure 2-1. This is known as a 'grain boundary triple point'— the junction of three grains. Here the electromigration-induced mass flux along the boundaries 1, 2, 3 represented as J_b^1, J_b^2, J_b^3 respectively are such that,

$$J_b^2 + J_b^3 > J_b^1$$

Under these circumstances, mass depletion will occur at the triple point and hence void formation. These voids grow in size and coalesce to form larger voids. A crack may then develop that eventually leads to discontinuity in the conductor path i.e. an open circuit.

2.3 Factors Affecting Electromigration in Thin films

Several material and process related factors have been reported to affect electromigration resistance. For instance, composition of the metal, anneal procedures, film deposition conditions, metal line geometry, contamination, passivation layer thickness, grain structure etc. [16,17,18,19,20]. This was shown in Figure 1-7 in the form of a simplified 'fishbone-diagram'.

These are now discussed further with reference to the commonly used aluminium-alloy metallisation.

2.3.1 Composition of Metal

Significant improvements in MTF can be achieved by the addition of small quantities of metals like copper, silicon, titanium etc [16,17]. Addition of copper (up to 4% copper in Al-Si metallisation) increases the MTF by a factor of 70 to 100 [18]. The exact mechanism is not yet well established. Two reasons have been given; one is a reduction in grain boundary diffusivity (copper atoms segregate at the grain boundaries and so retard the electromigration-induced aluminium ion flux, the other is grain structure modification when the added copper helps to form 'bamboo' structures as shown in Figure 2-2 which may also be an important factor contributing to improvement in lifetime. Dry etch and other problems with copper, whisker growth with titanium, etc. have to be considered if these alloys are used instead of the common aluminium-silicon [8].

2.3.2 Linewidth

A number of experimental studies on the linewidth dependence of electromigration lifetime have been reported [21,22,19]. Figure 2–3 shows one typical example [22].

In general it has been noticed that MTF decreases with linewidth up to a 'critical width' below which the lifetime either levels off or increases.

The improvement of MTF for linewidths smaller than the median grain size is usually explained in terms of the 'bamboo' grain structure in such fine lines [19]. These are further confirmed by computer simulations, taking microstructural aspects into consideration. For example, simulations by Harrison [23] on aluminium-copper metallisation is shown in Figure 2–4. The three curves correspond to median grain sizes of 3 μm (curve A), 2 μm (curve B) and 1 μm (curve C). The standard deviation of the failure distribution also shows a similar behaviour. It follows from these simulations and the experimentally observed results that 'critical width' is a sensitive function of the metallisation process parameters such as, substrate temperature during deposition, anneal conditions etc. because these are the factors that affect grain size in the films [20].

Even though MTF may increase below the critical width, electromigration still continues as a major problem in sub-micron geometry ICs. This is because,

1. Current density increases with scaling and this will decrease MTF (it may be noted that Figure 2-3 is for a given current density).

2. Metallisation process parameters such as linewidth, sputter parametrs etc. may have to be monitored and controlled to take advantage of the increased MTF below the critical width. In general, statistical process control measures are becoming necessary to preserve process uniformity over a wafer and from wafer to wafer in a batch which is discussed in chapter 4.

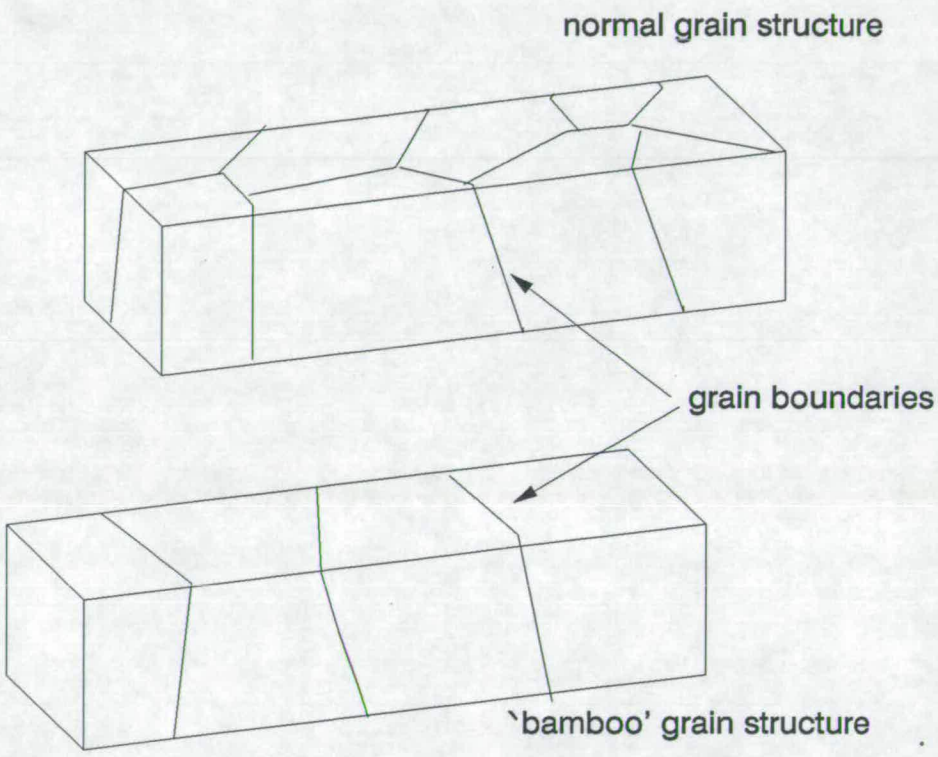


Figure 2–2: Sketches of the normal grain structure and 'bamboo' structure

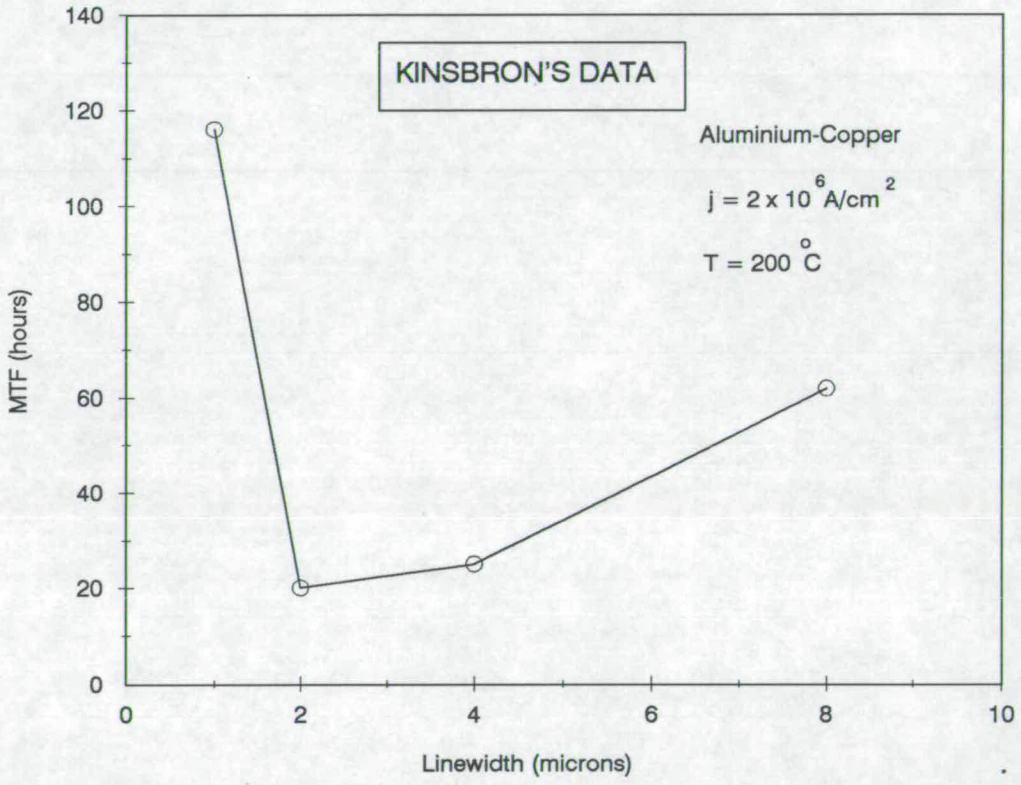


Figure 2–3: Experimentally measured MTF versus linewidth

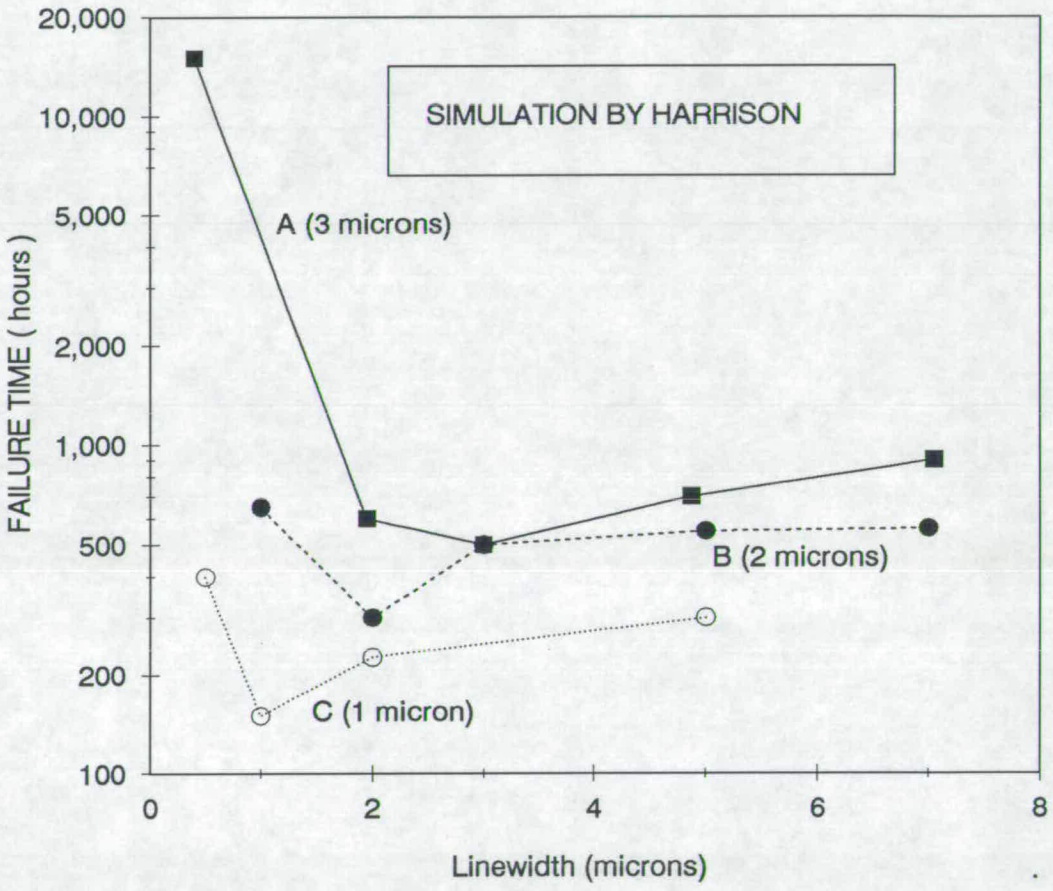


Figure 2–4: Simulated MTF versus linewidth

2.3.3 Linelength

The MTF has been reported to first decrease and then become independent of the length for all practical purposes [24]. This is thought to be due to the higher probability of finding more defects in a longer metal line. However, if we are considering electromigration-induced failures caused by grain boundary defects then there should be no linelength dependence of electromigration lifetime. This is because there is an abundance of these defects in lines of any length.

2.3.4 Microstructure

Detailed investigations of electromigration in fine line aluminium by Vaidya and others [19] has shown that there is a strong correlation between microstructure and electromigration lifetime. MTF is shown to be proportional to an empirical microstructural quantity η, given by [19]

$$\eta = \frac{S}{\sigma^2}\log(I_{111}/I_{200})^3 \tag{2.4}$$

where S is the grain size, σ is the standard deviation in grain size distribution and I_{111} and I_{200} represent the intensity of X-ray diffraction peaks for (111) and (200) respectively.

A large number of process and material-related factors could cause variations in the microstructural parameter:

- Sputter deposition bias
- Deposition temperature
- Post-deposition annealing
- Addition of alloying elements
- Cleanliness of the vacuum during deposition

Thus metal lines having identical geometry and metal composition may have different lifetimes depending on the deposition and anneal conditions.

2.3.5 Under and Over Layers

Passivation

The technique of covering thin film conductors with an insulating dielectric layer has been found to be beneficial with respect to electromigration failure times. In the earliest implementation, aluminium conductors were covered with a layer of fused glass [25]. Subsequently, improvements in electromigration by orders of magnitude were reported for aluminium films covered with a layer of aluminium oxide obtained by anodisation [26]. The mechanism for the improvement is not well understood. It is believed that the passivation layer inhibits the hillock growth and defers the void formation. [18].

Refractory metal layers

Multilayer sandwiches of aluminium-alloys with refractory metals/alloys, have also been reported to significantly increase the MTF. However, the complex metallurgical, chemical and microstructural interactions between the layers responsible for this improvement is not yet fully understood [8]. For example, in the case of aluminium and titanium films the improvement in MTF has been observed only in the films where the intermetallic compound $TiAl_3$ is formed. The presence of this compound which represents an electrically continuous layer is believed to block the propagation of the voids across the film. Additionally, new problems arise with these structures. For example, whisker growth with titanium and tungsten etc. However, research efforts are expected to continue to combat these deficiencies.

2.3.6 Other Factors

Many other factors have been reported to affect the electromigration resistance of thin films. These include, mechanical stress arising due to the difference in ther-

mal expansion coefficient between the metal and the insulator,reverse mass transport('back flow') due to concentration and pressure gradients because of hillock formation [27] and the presence of hydrogen and other gaseous ambients during thin film deposition and anneal [28]. However, in general it is quite difficult to estimate the relative contribution to mass transport due to these factors and special experimental techniques have had to be developed to separate out the contribution to mass transport from these factors. For example, drift velocity measurements using aluminium-silicon segments over titanium-nitride films to study reverse mass transport [27].

2.4 Failure Models

The industrial requirement is to predict the electromigration-induced failure time when operating at the specified maximum current density and chip temperature for a given material, deposition process and track layout.

A satisfactory and complete model for failure should be able to predict the observed relations between the lifetimes of thin film conductors and such parameters as material, current density, test temperature, linewidth etc. For example, lifetime increases as the linewidth increases (when the linewidth is significantly larger than the grain size) and it is inversely proportional to the square of the current density when j is about $1 \times 10^6 A/cm^2$.

Many failure models have been proposed [29,30]. However, the semi-empirical model proposed in 1969 by J.R.Black [25] has been very widely used in estimating the MTF of conductor lines so it is now discussed in detail.

2.4.1 Black's Equation for MTF

A metal ion which has been thermally activated and is at a saddle point (lifted out of its potential well and essentially free of the metal lattice) is acted on by two forces as shown in Figure 2–5 :

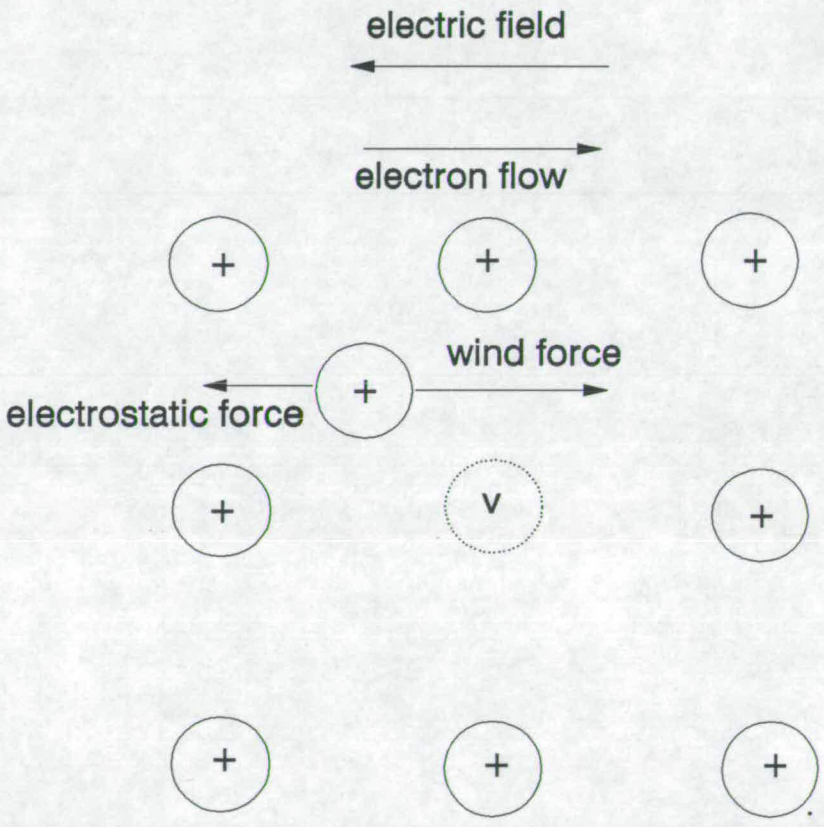


Figure 2–5: Forces acting on an ion at its saddle point

1. The electric field applied to the conductor— this will exert a force on the activated positive ion in a direction opposite to electron flow.

2. The rate of momentum exchange between the conducting electrons colliding with activated metal ions—this will exert a force on the metal ion in the direction of electron flow.

Because of shielding electrons, the force on the ion due to the electric field is quite small. The predominating force is due to the 'electron wind'. As a result, the thermally activated metal ions travel towards the positive side of the conductor. This can also be viewed as vacancies moving towards the negative side. The vacancies condense to form voids while the ions condense to form hillocks.

After being accelerated and colliding with ions elastically, the electrons impart all of their momentum to the ions. The rate of mass transport by momentum transfer between electrons and thermally activated ions is directly proportional to:

- Electron momentum
- The number of electrons/second/cm^2 available for striking the activated ions
- Effective target cross section
- Activated ion density

Electron Momentum

The additional momentum picked up by an electron in an electric field E, in a distance of its mean free path Λ is given by

$$P = eE\tau = e\rho j\tau = e\rho j(\frac{\Lambda}{v}) \tag{2.5}$$

where v is the average velocity, τ is the mean free time between collisions, e is the charge on the electron, ρ is the volume resistivity and j the current density. The

average velocity v is determined mainly by thermal velocity v_T and is perturbed only slightly by the drift velocity v_d

Number of electrons.

The number of electrons per second per unit cross sectional area, N, is related to current density (j) by

$$N = j/e \tag{2.6}$$

Activated Ion Density (Θ).

One may consider the number of activated ions per cubic centimeter in the metal to follow the Arrhenius equation as a function of temperature. Hence we get:

$$\Theta = F_1 \exp\left(-\frac{E_a}{kT}\right) \tag{2.7}$$

Where E_a is the activation energy in electron volts, F1 is a constant, and other symbols as defined earlier.

The MTF is considered to be inversely proportional to the rate of mass transport, and directly proportional to the film cross sectional area. That is,

$$MTF = \frac{F_2 wt}{R} \tag{2.8}$$

where F_2 is a constant and R is the rate of mass transport given by

$$R = (e\rho j)\left(\frac{\Lambda}{v}\right)\left(\frac{j}{e}\right)\left(F_1 \exp\left(-\frac{E_a}{kT}\right)\right) \tag{2.9}$$

This gives

$$MTF = \frac{A}{j^2}\exp\left(\frac{E_a}{kT}\right) \tag{2.10}$$

where the constant A depends on: film geometry (w and t), the electron mean free path(Λ), average velocity (v), the volume resistivity of the metal and F_2/F_1.

Using this model and the experimental results on aluminium films, Black obtained an activation energy in the range 0.48 eV to 1.2 eV. He attributed this wide differnce to the different mass transport processes, namely, grain boundary diffusion and lattice diffusion having different activation energies.

The drawback of Black's equation is that it does not satisfactorily explain the observed variation in MTF with grain boundary parameters such as median grain size, grain orientation etc. In addition, the finer details of mass transport in terms of grain structure of thin films are not dealt with in the model. Also, the linewidth dependence as in equation 2.8 (MTF $\propto$ wt) is valid for wide metallisation lines for which the linewidth is larger than the median grain size. The increase in MTF at widths smaller than critical width (discussed in section 2.3.2) is not explainable using Black's equation.

Subsequent to Black's model a number of failure models have been proposed, mainly based on computer simulations of microstructure of thin films. These include the earlier attempts by Attardo et al (1971) [31] and more recent models by Huntington et al (1991) [32] continue to account for a large number of empirical results collected over the years. These simulations have some succcess in explaining the microstructural dependence of electromigration, but use complex models. For example, in the model used by Huntington et al [32] a grain boundary network is first established by laying down a random array of points in two dimensions and then constructing the perpendicular bisectors of lines joining nearby points. The planes so constructed form the grain boundaries. Having generated the above network many details have to be carefully worked out. This includes, the determination of the orientation of the individual grains, optimisation of the network to meet the minimum surface energy requirements etc. However, a simple failure model incorporating microstructural and temperature factors is not yet available. Hence, despite its drawbacks, Black's equation is very widely used in IC metallisation failure time predictions.

However, based on subsequent studies, Black's equation is usually modified to:

$$\mathrm{MTF} = \frac{\mathrm{f(w)\ tA'}}{\mathrm{j^x}} \exp\left(\frac{\mathrm{E_a}}{\mathrm{kT}}\right) \tag{2.11}$$

where ,

x=1 for $j \leq 1 \times 10^5 A/cm^2$

x=2 for $j \geq 1 \times 10^6 A/cm^2$

f(w)= w for wide lines with w $\gg$ grain size and the functional relation is to be empirically obtained for widhs near critical width.

2.5 VLSI circuit Reliability Simulation Models

2.5.1 Motivation for Reliability Simulation

In designing a complex circuit, designers make a large number of circuit simulations, design changes and optimisations and can predict the circuit's performance reasonably accurately before committing it to silicon. It would be unthinkable to bypass the circuit simulation and optimisation and rely entirely on the testing of finished ICs to discover errors or to find out if the performance of the circuit meets specifications. Yet,this is basically the way IC reliability is treated today [33].

At the present time, reliability assurance relies mainly on failure detection, which occurs only at the end of a lengthy product development and qualification process. This practice poses serious problems for future complex VLSI circuits. Reliability failure, if detected during testing, or worse during field application, will be prohibitively costly both from time and cost points of view to fix the problem by process or design changes.

It is highly desirable to predict the circuit reliability at the circuit design stage. A schematic diagram of this methodology is shown in Figure 2–6 [33]. Several reliability simulators analogous to process simulators which contain separate models for diffusion, implantation, oxidation etc. have been reported in the literature to model electromigration, hot-electron degradation etc. [34,35]. In these simulators, a set of parameters relevant to circuit reliability is identified for each failure

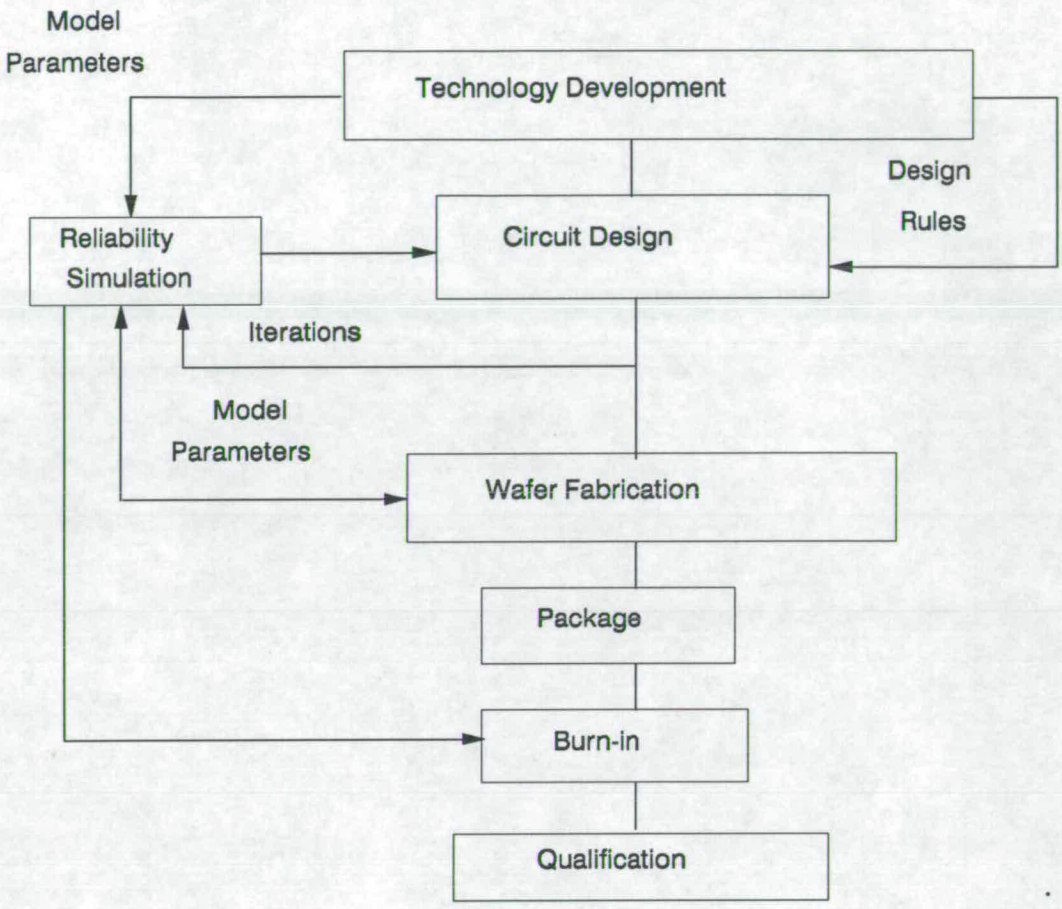


Figure 2–6: A methodology of reliability assurance

mechanism. Computer programs are developed to predict circuit failure rate from these parameters .

The above methodology is still in its early stages and not well established. Development of simple methods of extracting these parameters for a given process or technology involving accelerated stress tests on test structures is one of the important research areas.

2.5.2 Reliability Simulators for Electromigration

Many of the VLSI circuit electromigration reliability simulators use the series model to express the failure [36,37]. That is, the failure rate of any one of the

segments (bends, vias etc.) in the IC causes IC failure and that the total failure rate is the sum of the individual failure rates:

$$\lambda = n_l\lambda_l + n_b\lambda_b + n_v\lambda_v + ... \tag{2.12}$$

Where λ is the failure rate of the IC,

n_l = number of linear segments

λ_l = failure rate of linear segment

n_b = number of bends

λ_b = failure rate of bend

n_v = number of vias

λ_v = failure rate of via

It should be noted that in the absence of any technique to directly obtain the failure rate λ_l of a small linear segment, (generally of median grain size), it is a general practice to use the MTF of a lengthy line and estimate λ_l by applying statistical techniques [38]. Estimations of λ_b and λ_v are complicated because of current crowding effects. If we use the usual current density dependence (MTF $\propto 1/j^2$) and inceased current density values due to current crowding, the calculated failure rate of VLSI circuits may come down to unrealistic values; on the other hand ignoring these effects overestimates the reliability. Quite often the latter approach is adopted [38] and λ_b and λ_v are usually estimated based on the expected changes in cross sectional area at a via or a bend. This is one important area where further research is needed.

A statistical methodology has been suggested in this thesis to estimate the MTF of small segments using the new test structures.

Bibliography

[1] A.Blech and H.Sello. Rome Air Development Center, New York, Technical Report : TR-66-31, 1965.

[2] J. R. Black. Electromigration — a brief survey and some recent results. *IEEE Transactions on Electron Devices*, ED-16(4) :338–347, 1969.

[3] M. J. Attardo and R. Rosenberg. Electromigration damage in aluminium film conductors. *J. Applied Physics*, 41(6):2381–2386, 1970.

[4] A. Bobbio and O. Saracco. Electromigration failure in aluminium thin films under constant and reversed DC powering. *IEEE Transactions on Reliability (USA)*, R23:194–202, January 1974.

[5] R.S.Sorbello. *Electro and Thermo-Transport in Metals and alloys*, chapter 1. AIME, New York, 1977.

[6] S. S. Iyer and C. Y. Wong. Grain growth study in aluminium films and electromigration implications. *J.Applied Physics*, 57(10) :4594–4598, 1985.

[7] Hoang H.Hoang and J.Michael .McDavid. Electromigration in multilayer metallisation systems. *Solid State Technology*, (10):121–126, 1987.

[8] N. P. Armstrong et al. Electromigration alternatives to aluminium-copper. *IEEE VLSI Multilevel Interconnect Conference*, pages 460–468, 1988.

[9] Dipankar Pramanik and Arjun N. Saxena. Aluminum metallisation for ULSI. *Solid State Technology*, (3):73–79, 1990.

[10] V.B.Fiks. On the mechanism of the mobility of ions in metals. *Soviet Physics -Solid State*, (1):14, 1959.

[11] H. B. Huntington and A. R. Grone. Current-induced marker motion in gold wires. *J.Phys.Chem.Solids*, 20 (1 and 2):76–87, 1961.

[12] C.Bosvieux and J.Friedel. *J.Phys.Chem.Solids*, (23) :123, 1962.

[13] C.Herzig and D.Cardis. Matter transport in pure gold, induced by high direct current densities. *Applied Physics*, (5) :317, 1975.

[14] T.Kwok and P.S.Ho. *Diffusion Phenomena in Thin Films and Microelectronic Materials*, chapter 7, page 424. Noyes Publications, USA, 1988.

[15] F.M.d'Heurle and P.S.Ho. Electromigration in thin films. In *Thin Films: Interdiffusion and Reactions*, chapter 8. Wiley-Interscience, New York, 1978.

[16] K. V. Reddy, F. Beniere, and D. Kostopoulos. Electromigration and diffusion of copper in aluminium thin films. *J.Applied Physics*, 50(4) :2782–2786, 1979.

[17] P. B. Ghate. Electromigration induced failures in VLSI interconnects. *Reliability Physics, IEEE Annual Proceedings*, pages 292–299, 1982.

[18] F.Fantini. Metallisation and electromigration. *Interuniversity Microelectronics Centre (Belgium), summer course*, 1989.

[19] S. Vaidya, D. B. Fraser, and A. K. Sinha. Electromigration resistance of fine line aluminium for VLSI applications. *Reliability Physics, IEEE Annual Proceedings*, pages 165–170, 1980.

[20] Dr.Hendel. Electromigration resistance improved through sputtering control. *Microelectronic Manufacturing and Testing*, pages 25–26, November 1990.

[21] P.J.Dulnaik. Effect of integrated metallisation linewidth on the distribution of electromigration lifetime. *Applied Physics Letters*, 54(13) :1229–1231, 1989.

[22] E. Kinsbron. A model for the width dependence of electromigration lifetimes in aluminium thin-film stripes. *Applied Physics Letters*, 36(12) :968–970, 1980.

[23] J.W.Harrison. A simulation model for electromigration in fine-line metallisation of integrated circuits due to repetitive pulsed currents. *IEEE Transactions on Electron Devices*, 35(12) :2170 –2179, 1988.

[24] B.N.Agarwala, M.J.Attardo, and A.P.Ingraham. Dependence of electromigration-induced failure time on length and width of aluminium thin film conductors. *J.Applied Physics*, 41(10) :3954–3960, 1970.

[25] J. R. Black. Electromigration failure modes in aluminium metallisation for semiconductor devices. *Proceedings of the IEEE (USA)*, 57(9) :1587–1594, 1969.

[26] A.J.Learn. Effect of structure and processing on electromigration -induced failure in anodized aluminium. *J.Applied Physics*, 44 :1254, 1973.

[27] I. A. Blech and C. Herring. Stress generation by electromigration. *Applied Physics Lettesrs*, 29(3) :131–133, 1976.

[28] R.W.Pasco, L.E.Felton, and J.A.Scwarz. The effects of hydrogen ambients on electromigration in aluminium-2% copper thin film conductors. *Solid State Electronics*, 26(11) :1053–1063, 1983.

[29] R.A.Sigsbee. Failure model for electromigration. *Reliability Physics, IEEE Annual Proceedings*, page 301, 1973.

[30] J. M. Schoen. Monte Carlo calculations of structure_induced electromigration failure. *J. Applied Physics*, 51(1) :513–521, 1980.

[31] M. J. Attardo, R.Rutledge, and R.C.Jack. Statistical metallurgical model for electromigration failure in aluminium thin-film conductors. *J. Applied Physics*, 42(11) :4343–4349, 1971.

[32] H.B.Huntington. A computer simulation of stripe deterioration through electromigration. *J. Applied Physics*, 70(3) :1359–1368, 1991.

[33] Chenming Hu. IC reliability simulation. *IEEE J.Solid - State Circuits*, 27(3) :241–246, 1992.

[34] F.Najm et al. Probabilistic simulation for reliability analysis of CMOS VLSI circuits. *IEEE Transactions on Computer-Aided Design*, 9(4) :439–450, 1990.

[35] B.J.Sheu et al. An integrated circuit simulator-RELY. *IEEE J.Solid-State circuits*, 24:473–477, April 1990.

[36] P.M.Lee et al. *BERT-Circuit Aging Simulator.* Electronics Research Laboratory of University of California report, January 1990.

[37] D.F.Frost, K.F.Poole, and D.A.Haeussler. RELIANT: a reliability analysis tool for VLSI interconnects. *IEEE custom integrated circuits conference, pages 27.8.1–27.8.4*, 1988.

[38] D. F. Frost and K. F. Poole. A method for predicting VLSI device reliability using series models for failure mechanisms. *IEEE Transactions on Reliability*, R-36(2) :234–242, 1987.

Chapter 3

Review of Measurement Techniques

3.1 Introduction

Electromigration in thin films has many interesting features both from theoretical and technological points of view. The former include the nature of the 'wind force' at the grain boundaries, while the latter concerns mainly the more practical aspect of failure time predictions of IC metallisation. Accordingly the following two types of measurement techniques have evolved to meet these requirements:

1.Electron microprobe techniques, drift velocity measurements and mass transport measurements to measure the electromigration parameters of fundamental interest such as the effective charge (Z_b^*) and diffusion coefficient (D_b) at the grain boundary. Details of these measurement techniques can be found in a review article [1].

2. Conductor lifetime measurements (usually referred to as MTF measurements or lifetests), resistometry, fast tests, mass transport measurements and noise tests [2].

We are interested in type 2 measurements because these give parameters useful in assessing the IC metallisation reliability. Therefore these are discussed here. However, the noise measurements are not discussed here because the theory and analysis of these tests are yet to be developed and also the instrumentation requirements are quite complicated.

In the initial stages of this project some measurements were carried out using some of these techniques, in order to derive the constants in Black's equation for

the EMF process and the results are also included here. In all of these measurements, accelerated testing are used to cut down the test times. Hence the various aspects of accelerated testing and acceleration factors are discussed first.

3.2 Accelerated Testing

Accelerated testing techniques involve stressing a part in an environment more severe than standard operation conditions. The stress conditions are selected under the assumption that factors controlling the degradation are the same failure mechanisms as those that predominate in typical operating conditions for the part. The observed behaviour of the part under these conditions is then related to its performance at actual operating conditions using a degradation model.

The major reason for using accelerated testing is to cut down the test times involved. The failure rate expected of the present day VLSI circuits under normal operating conditions is very low- of the order of 100 FITs. This corresponds to stressing 100 parts for approximately 11 years or equivalently 10,000 parts for approximately 1000 hours to observe one failure. In future the situation will be much more demanding; to monitor 100 parts for one failure in 114 years of operation under normal operating conditions. Obviously the test times and the number of test parts required make it extremely difficult to carry out reliability testing of a design in a time scale short enough that the design has not become obsolete before being produced. Also the usage of ASICs in military/aerospace applications means the number of samples actually needed may be far below that required for reliability testing. Using higher current densities and temperatures, one could shorten test times, for example: the MTF of 20 years at an operating temperature of 25° C and current density of $1 \times 10^5 A/cm^2$ will be reduced to almost a few days at $1 \times 10^6 A/cm^2$ at 150°C for Al-1%Si metallisation [3]. However, one should be cautious in using high temperatures. At temperatures $\geq$ 250°C lattice diffusion may become predominant and it will be inappropriate to extrapolate these failure

rates to normal operating conditions where grain boundary diffusion dominates [4].

3.3 MTF Measurement [5-9]

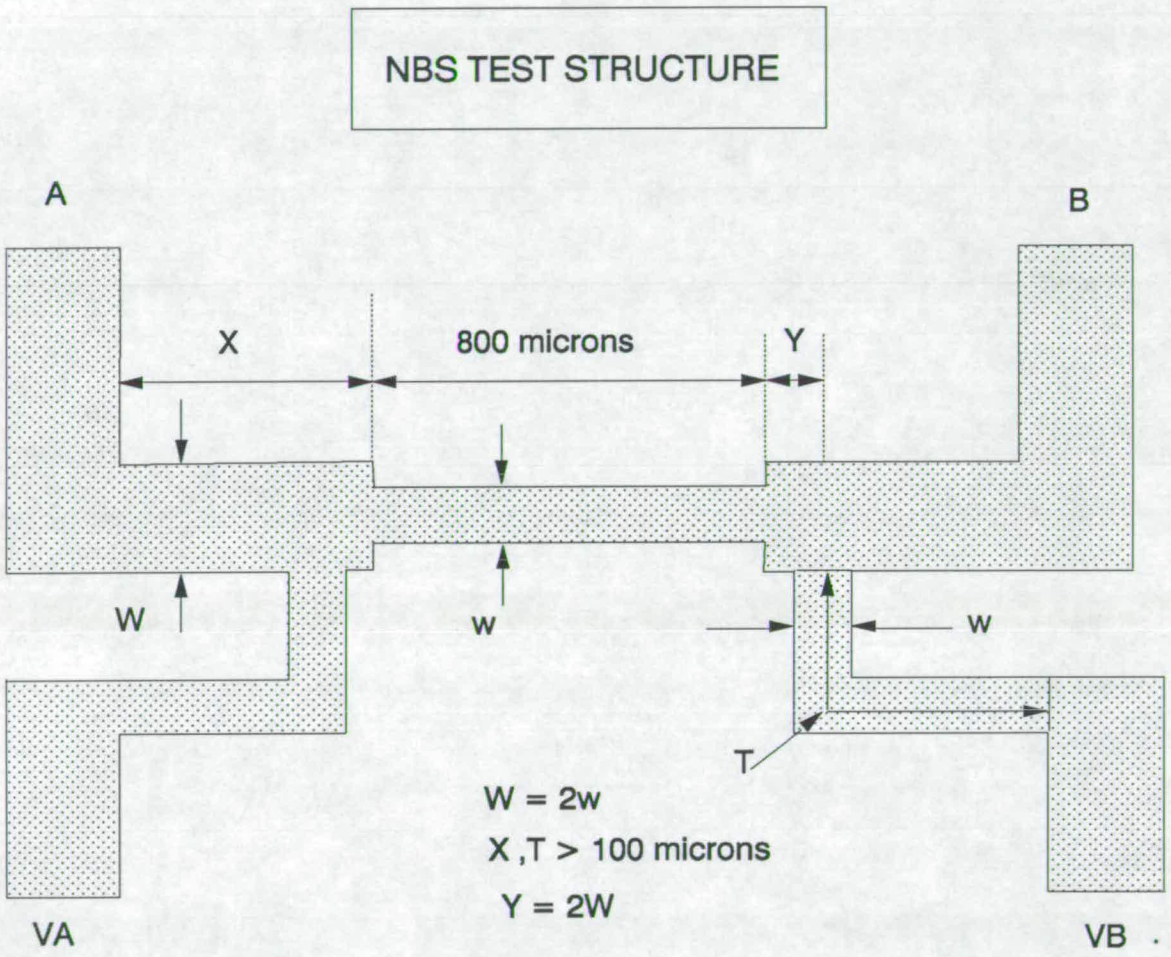
This measurement records the time at which 50% of a large number of nominally identical specimens fail when subjected to constant current density at a given temperature. This is the most commonly used method for evaluating electromigration resistance [1]. The advantages of this method are its simplicity and well defined failure mode("open"). We have a good empirical database and experience and also the availability of standard test procedures and methods for reliability estimations [10-12]. Hence MTF measurement has been described as a ' a corner stone of metallisation reliability testing' [13] and MTF values are the most sought-after electromigration parameters.

However, the main practical disadvantage is the fact that it requires a large number of samples to be tested at elevated temperatures usually in a burn-in chamber for test times that may range from weeks to months. There are some fundamental limitations of MTF measurements and these are discussed in detail in chapter 4.

3.3.1 MTF Measurements on EMF Metallisation

These measurements were done to derive the constants in Black's equation. The standard NBS [14] test structure commonly used for MTF tests was used which is shown in Figure 3–1. The process and other details are summarised in Table 3–1, the dimensions shown are the measured values (averages).

Ideally the number of samples used for electromigration MTF measurements should be as large as possible. However, test setup, cost and time factors forbid the use of a large number of samples and some compromises have to be made. A literature survey indicated that majority of experiments have been carried out with a sample size between 10 and 20. So the minimum acceptable sample size of 10



A, B: pads for passing the stress current
VA, VB: pads for monitoring the voltage-drop

Figure 3–1: Test structure used for MTF measurements

Wafer	P-type, 3 inch dia.,	
Insulator	Material	SiO_2
	Process	wet oxidation
	Thickness	$5600\mathring{A}$
Metallisation	Material	Al-1%Si
	Deposition	sputtering
	Thickness	$1.0\mu m$
Anneal	435^oC, 10 min. N_2/H_2	
Etch	Dry	
Structure dimensions	Width	$6.20\mu m$
	Length	$800\mu m$

Table 3–1: Test structure and process details

was chosen. The samples were mounted in DIP packages and powered individually (current density of $1 \times 10^6 A/cm^2$) and a HP computer was used to monitor the failure times. For stress experiments conducted at 150°C, printed circuit boards made from epoxy glass were used. But to conduct stress experiments at 175°C , these PCBs were not suitable and special jigs were fabricated using holes drilled in metal boards and high temperature IC sockets, turrets, solder and wires were used.

All the test samples were visually inspected for any defects using optical microscopes. Only defect free samples were used. The resistances of all the samples were measured at various temperatures inside the oven and the temperature coefficient of resistance was obtained. Using this, the temperature rise in all the samples when subjected to a current density stress of $1 \times 10^6 \mathrm{A/cm^2}$ was obtained. This was found to be approximately 3°C.

3.3.2 Test Results and Discussion

The time to failure data obtained is shown in Figure 3–2.

The activation energy is obtained using Black's equation as follows:

$$\begin{aligned}
\mathrm{MTF_1} &= \frac{\mathrm{A}}{\mathrm{j^2}}\exp\left(\frac{\mathrm{E_a}}{\mathrm{kT_1}}\right) \\
\mathrm{MTF_2} &= \frac{\mathrm{A}}{\mathrm{j^2}}\exp\left(\frac{\mathrm{E_a}}{\mathrm{kT_2}}\right) \\
\frac{\mathrm{MTF_1}}{\mathrm{MTF_2}} &= \exp\frac{\mathrm{E_a}}{\mathrm{k}}\left(\frac{1}{\mathrm{T_1}} - \frac{1}{\mathrm{T_2}}\right) \\
\mathrm{E_a} &= \mathrm{k}\ln\left(\frac{\mathrm{MTF_1}}{\mathrm{MTF_2}}\right) / \left(\frac{1}{\mathrm{T_1}} - \frac{1}{\mathrm{T_2}}\right)
\end{aligned}$$

where

$$\mathrm{T_1} = 150 + 3 + 273 = 426\mathrm{K} \tag{3.1}$$

$$\mathrm{T_2} = 175 + 3 + 273 = 451\mathrm{K} \tag{3.2}$$

$$\mathrm{MTF_1} = 30.5\mathrm{hours} \tag{3.3}$$

$$\mathrm{MTF_2} = 9\mathrm{hours} \tag{3.4}$$

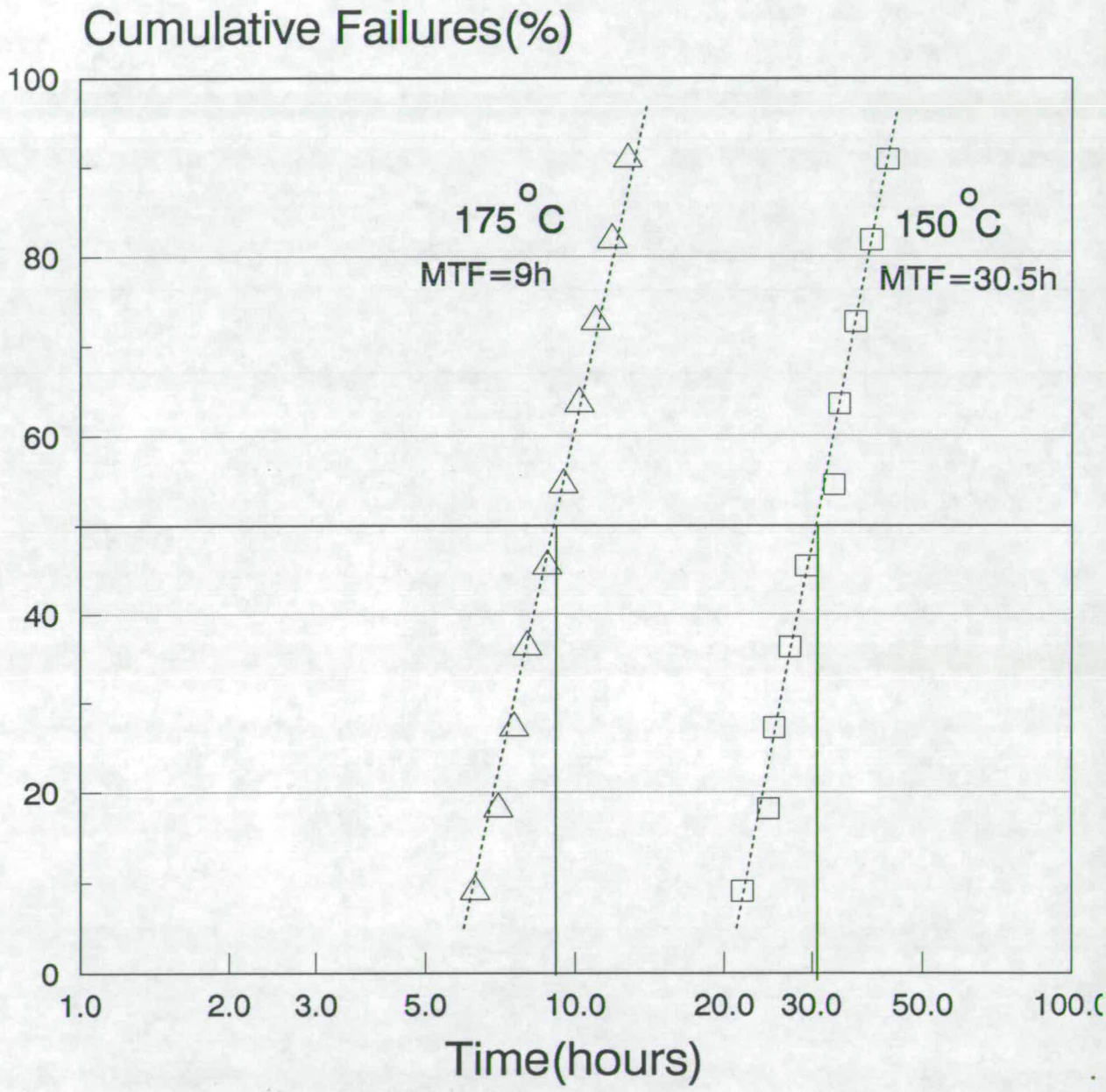


Figure 3–2: failure time distribution

substituting the above values in the expression above, we get

$$E_a \simeq 0.8eV \tag{3.5}$$

$$\mathrm{A} \simeq 10.4 \times 10^3 [hours][amperes/cm^2]^2 \tag{3.6}$$

Most values of E_a for aluminium films lie in the range of 0.6 ± 0.2 eV [12]. This spread is due to the fact that in addition to the mass transport due to grain boundary diffusion, other parallel mass transport mechanisms with different activation energies coexist.

Mass transport mechanism	$E_a(eV)$
Lattice diffusion	1.4
Grain boundary diffusion	0.4-0.5
Grain boundary to bulk	0.63
Defects to bulk diffusion	0.62
Surface diffusion	0.28

Table 3–2: Mass transport mechanisms in thin aluminium films

These are summarised in Table 3–2. Hence the activation energy of 0.8 eV may be considered as an appropriate average .

The reliability specifications are commonly given in terms of FITs and hence, the MTF data is translated into failure rate versus time curves as shown in Figure 3–3. This prediction is for a 3μm width line and under the following operating conditions: normal operating current density $1 \times 10^5 \mathrm{A/cm^2}$ and normal operating temperature 40°C. Also, the commonly used value of x=1 for this current density was used in Black's equation (see section 2.4.1).

The failure rate as a function of time is calculated using the probability density function and cumulative distribution function of the lognormal distribution described in Appendix C. The expression for the failure rate is given below.

$$\lambda(\mathrm{t}) = \frac{\exp[-\frac{(\ln \mathrm{t}-\mu)^2}{2\sigma^2}]}{\mathrm{t} \int_{\mathrm{t}}^{\infty} \frac{1}{\mathrm{t}} \exp[-\frac{(\ln \mathrm{t}-\mu)^2}{2\sigma^2}]} \, \mathrm{dt} \tag{3.7}$$

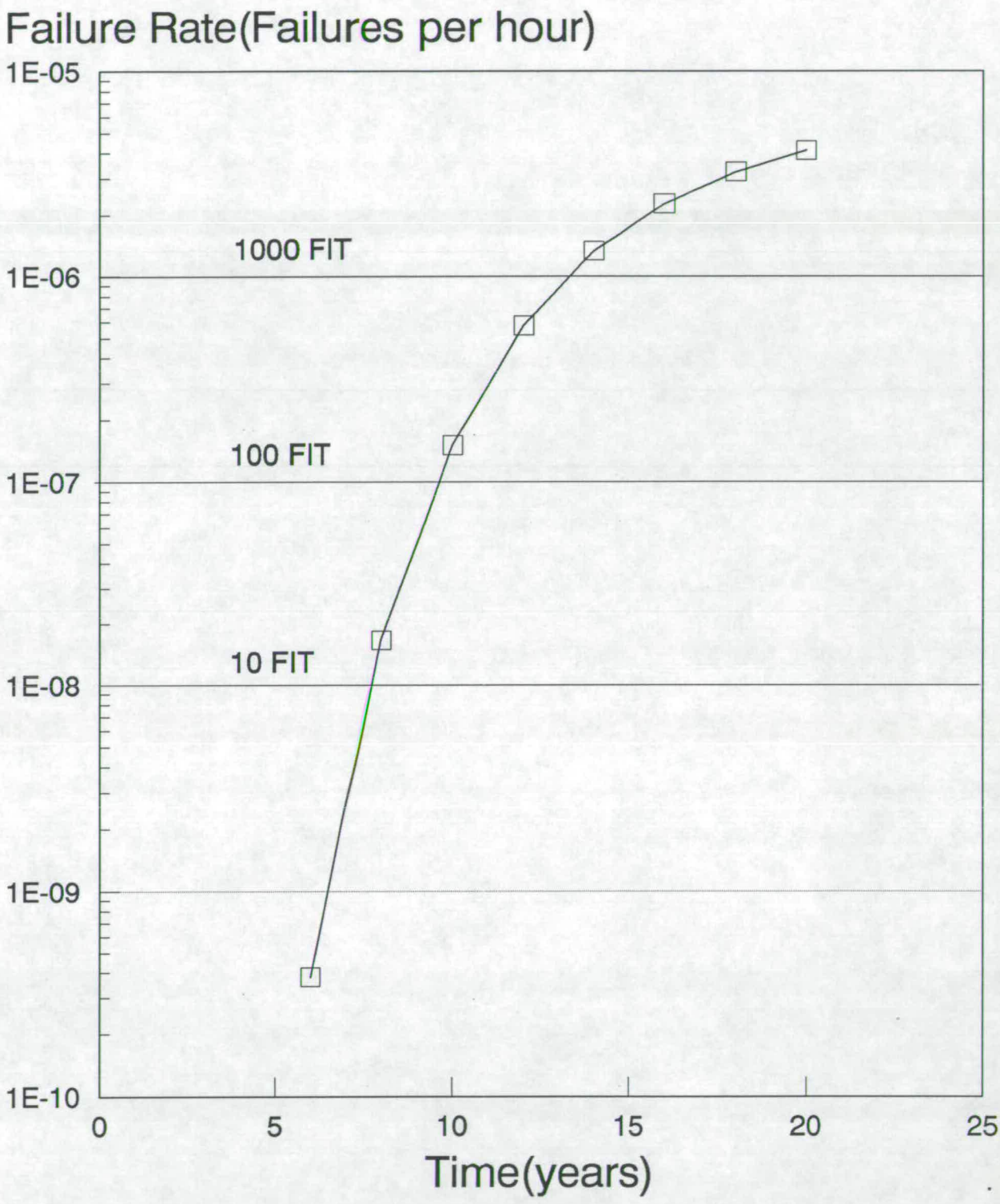


Figure 3–3: Estimated failure rate versus time of EMF metallisation under normal operating conditions

where,

λ (t) = failure rate as a function of time

t = time

$\mu = \ln(MTF)$

$\sigma = \ln[MTF/t_{16}]$

t_{16} = time for 16% cumulative failures

Figure 3–3 shows that when the linewidth is $\leq 3\mu$m it may become increasingly difficult to meet the future reliability requirements. The failure rate may far exceed (by a factor of about 500) the minimum acceptable limit of 10 FITs for 20 years.

There are many ways to meet the reliability demands of high reliability device users. One method is to reduce the operating current density. This is not a real option because it puts stringent constraints on the circuit designer. The second way is the technological solution; addition of copper to the aluminium-silicon alloy film or multilayer metallisation systems with refractory metals which give order of magnitude improvement in MTF and hence a significant reduction in failure rate to meet or exceed the requirement for 10 FITs for 20 years. However, this may bring in other technological process problems as discussed in chapter 2 (section 2.3.5). The most attractive solution is to increase the MTF by grain structure modifications such as 'bamboo' structures. This means the process should be well controlled and should be continuously monitored to ensure that all the wafers meet the target reliability specifications. There are some fundamental limitations with MTF measurement as a process control monitor and these are discussed in chapter 4.

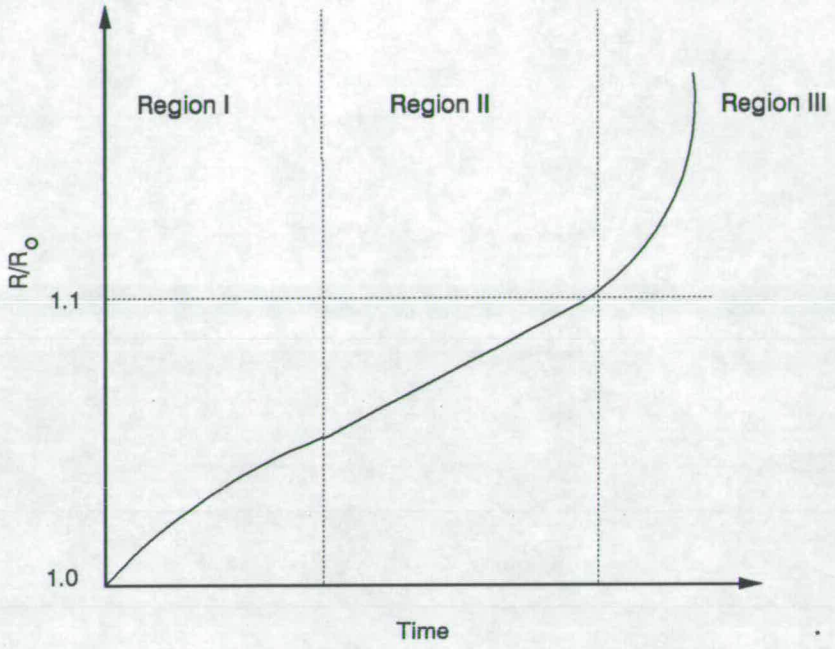


Figure 3–4: Schematic representation of resistance change with time of a metallisation line during electromigration stress experiments

3.4 Resistometry [15-24]

This method measures the fractional change in resistance ($\frac{R}{R_o}$) with time caused by material accumulation and depletion as a result of electromigration. The technique has the advantage of being simple and resistance changes can be measured accurately. The resistance change with time during electromigration stress experiments usually looks like 3–4. It consists of three regions:

Region I: joule heating
Region II: mass transport due to electromigration
Region III: catastrophic failure processes

In region I the temperature of the metallisation increases due to self-heating. The thermal stabilization time depends on various thermal time constants. For example, thermal time constant of the metallisation/oxide; oxide/substrate; substrate/chuck etc.

In region II the resistance increases gradually due to mass transport. Typically a near linear resistance increase has been reported by many researchers. Electromigration parameters like activation energy, the pre-exponential constant in Black's equation, and estimation of MTF are usually obtained by analysing this region.

In region III resistance increases rapidly and within a short time the structure fails ("opens"). The mechanisms leading to the ultimate failure of the line are quite complex, involving increase in current density, temperature and void growth. The exact point on the resistance versus time curve at which these catastrophic failure processes take over is not yet resolved, typically it is taken as that corresponding to 5-10% increase in resistance.

Figure 3–4 shows a smooth resistance versus time curve, but this may not be the case in practice and multiple spikes may occur to further complicate the analysis. This problem is discussed in section 3.4.2.

While the time to failure is determined by the failure time of a worst site along the stripe length, all the grain boundaries at which electromigration is taking place contribute to the resistance change and hence the rate of resistance change is considered to be an appropriate average over the entire stripe. These measurements are carried out before the catastrophic failure processes occur and an understanding of the mechanisms of solid state transport is only possible through measurements carried out in the earlier stages of electromigration damage.

Resistometry has been used to obtain many important electromigration parameters like activation energy, effects of material/processing on the pre-exponential constant in the MTF equation, and also MTF.

3.4.1 Resistometry Types

Resistometric measurements have been carried out under three types of stress conditions:

1. High ambient temperature but negligible initial joule heating— This is the simplest of the three types. Samples are subjected to constant current density stress at high temperatures. Current density values are such that the temperature rise is usually small (5 to10°C). Using a minor alteration of this technique, activation energies have been obtained using a single sample by suddenly changing the ambient temperature, but keeping the same current density and noting the ratio of rate of change of resistance.

2. Temperature Ramp — This technique is known as temperature ramp analysis of resistance to characterize electromigration [TRACE] [25]. Instead of keeping the ambient temperature constant, it is ramped up with a known rate. Now the resistance increase is due to increase of temperature as well as electromigration. This may be expressed as:

$$\begin{aligned} R(t) &= R_{TEMP(t)} + R_{EM(t)} \\ TEMP(t) &= T_0 + \beta t \end{aligned}$$

where β is the heating rate and T_o is the initial temperature.

By knowing the temperature ramp rate and subtracting $R_{TEMP(t)}$ one obtains the rate of resistance change due to electromigration. Black's equation is modified as:

$$\frac{1}{R_o}\frac{dR_{EM}}{dt} = \frac{C}{j^2}\exp(-\frac{E_a}{kT}) \tag{3.8}$$

Where R_o is the resistance at room temperature and C is a constant determined by TRACE experiments in the initial stages (5-10 % increase in resistance). It may be noted that TRACE assumes a linear increase in R_{EM} with time. Both activation energy and pre-exponential constant C can be determined by the TRACE experiments carried out on a single sample in few hours time. Using this technique, the effects of composition and structure on electromigration time to failure at a given failure criteria such as 10 % increase in resistance have also been studied [26].

The TRACE experimental set-up is very complicated. Usually TRACE experiments have been carried out on packaged parts by ramping the temperature of a furnace at a known rate. However, the TRACE methodology is very risky because it is assumed that the ramp rate must be carefully maintained.

3. Resistometry Without External Heating:

In order to accelerate the failure rate to cut down test times, resistometry techniques using high current densities which cause self-heating have been used to compare the lifetimes of conductors and to obtain activation energies [27]. The main disadvantage of this technique compared to low current densities is that the temperature rise due to joule heating as a function of time has to be known. In the past, thermocouples placed adjacent to the tracks have been used for this purpose. But, that procedure is clearly inaccurate and gives poor reproducibility.

3.4.2 Problems with resistometry

The major problem in using resistometry is the erratic resistance versus time curves, characterised by multiple spiking and sudden increases, unless efficient heat conducting paths are provided for electromigration structures. A typical example is shown in Figure 3–5 [28]. The explanations provided for this graph and similar graphs obtained by others are summarised in Figure 3–6.

The above explanations are supported by computer simulation of the thermal and electrical environment in the vicinity of a void [15]. Experimental evidence has also been provided by TEM studies [19].

In those cases where very smooth resistance versus time curves are reported:

1. Time resolutions are not fine enough to record the spikes. For example, only a few points collected over a period of hundreds of hours at selected intervals.

2. Only the average value of resistance within a time interval is shown.

In summary, resistometry is very promising from the point of view of process monitoring for electromigration because any process deviation causing an unac-

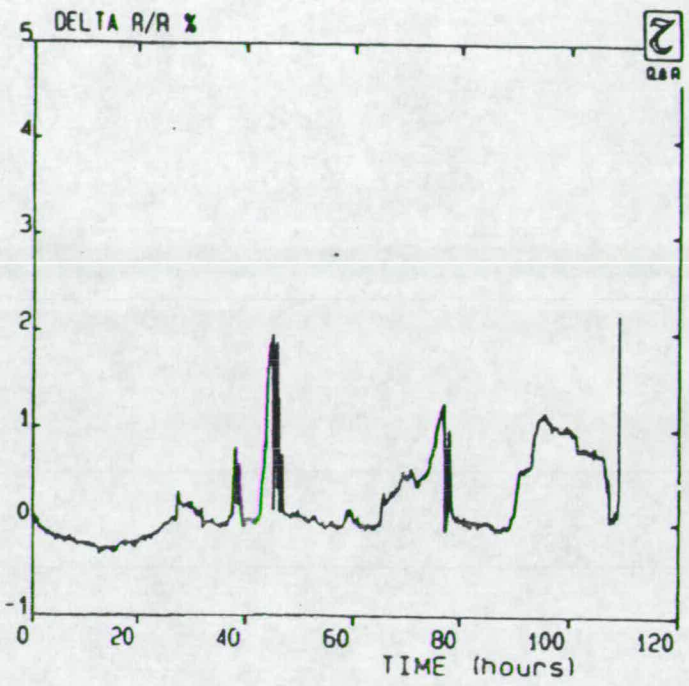


Figure 3–5: Resistance versus time curve showing multiple spiking

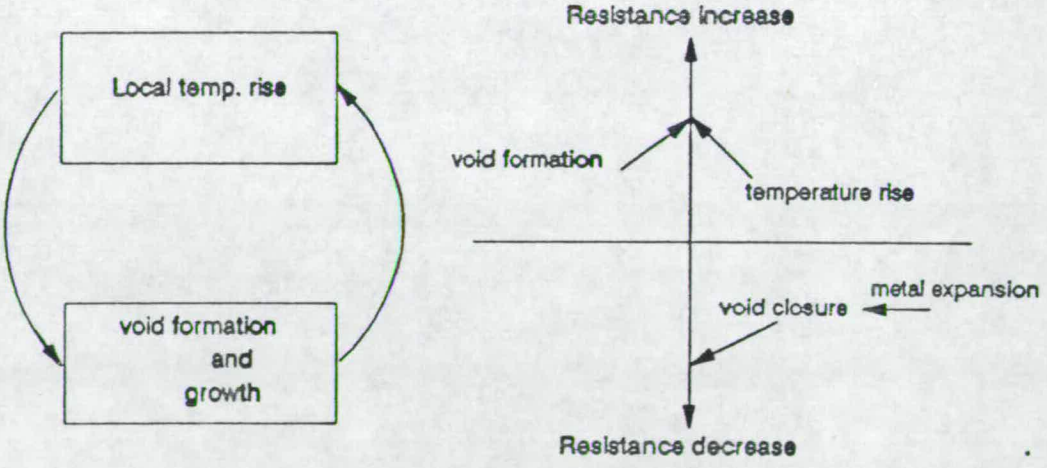


Figure 3–6: Factors causing multiple spiking and sudden increase and decrease in resistance

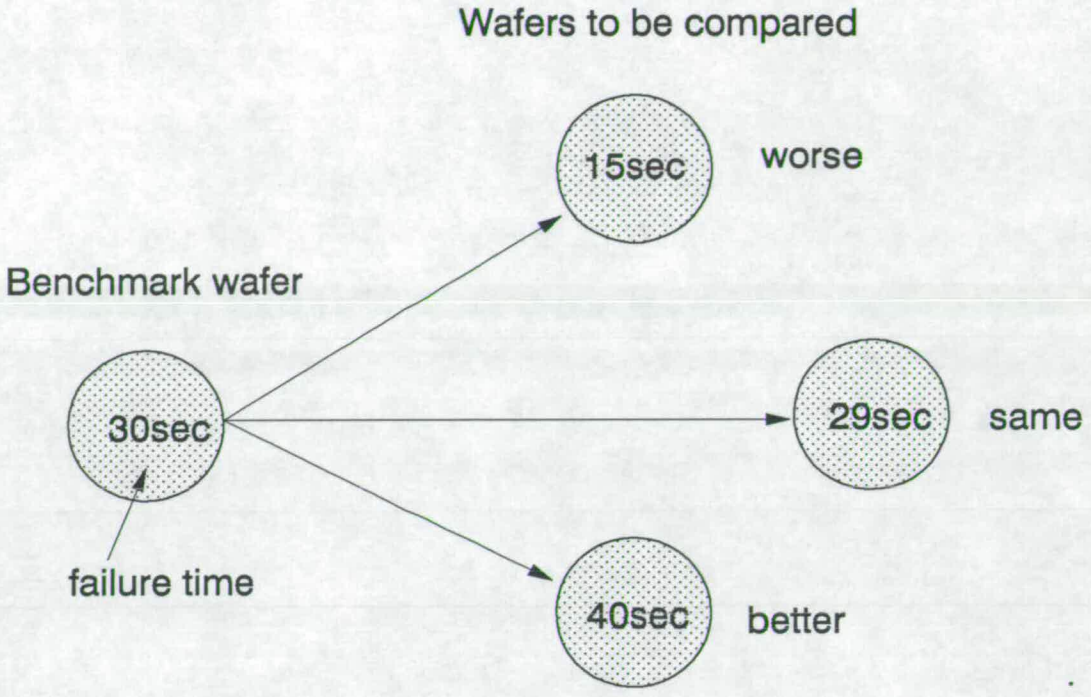


Figure 3–7: SWEAT method for monitoring electromigration

ceptable overall change in width, thickness, median grain-size etc. would change the average mass transport integrated over the entire line and this would be reflected in the resistance measurements. However, the spiking problem is the major drawback of this technique.

3.5 Fast Tests [4, 29-32]

Many tests have been developed recently as process control monitors of metallisation reliability, usually referred to as 'fast tests' [29, 30]. All these tests use high current densities and temperatures to shorten the test time to few tens of seconds. One typical example is **S**tandard **W**afer-level **E**lectromigration **A**cceleration **T**est (SWEAT) [29]. The principle behind this test is to provide a stress (current and temperature) equivalent to 20 years of normal operating conditions, within a very short time of few seconds and to compare the actual failure time against a calibrated reference value. This is schematically shown in Figure 3–7. Before starting the test, the value of the pre-exponential constant in Black's equation,

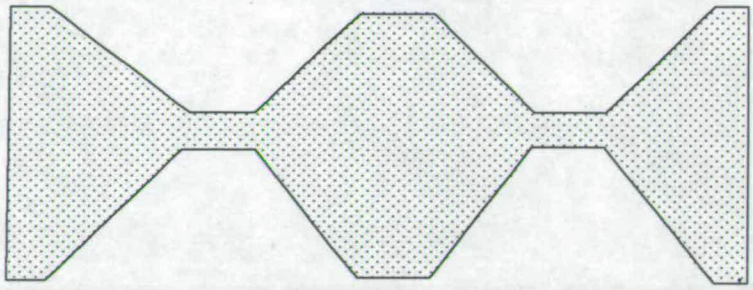


Figure 3–8: SWEAT structure unit

temperature coefficient of resistance of metallisation, activation energy etc. are needed. These are used to estimate factors like temperature rise and equivalent stress time.

The test structure consists of alternate wide and narrow segments as shown in Figure 3–8. Electromigration damage is mainly confined to the narrow regions and thus is localised because of high current density. Another characteristic feature is that the wide segments act as heat sinks. In conventional long tracks where the heat dissipation from the electromigration region (may include the entire metal length) is mainly through the oxide-silicon-chuck sandwhich, such highly accelerated tests produce irreproducible results [13].

The actual test system consists of computer controlled instruments used to ramp up the power and continuously monitor the current and temperature of test line and estimate the 'equivalent stress time' the line receives in 30 milliseconds time intervals, typically. Usually the testing is continued till the line fails and the cumulative value of this (equivalent stress time) is compared with the target value. The principle is illustrated in Figure 3–7. For temperature estimations, the metal line is used as its own temperature monitor. Equivalent stress time at any instant of time is estimated using Black's equation.

SWEAT testing may work but it is risky to use it for routine process monitoring. This is because it is assumed that thermal equilibrium is established rapidly across the structure. But this depends on the different thermal time constants for the metal-oxide-silicon-chuck sandwhich and the implications of this are not

clear. Some typical values of the thermal time constants are given in Appendix E. Inaccurate temperature estimations in SWEAT tests are also due to the fact that temperature is not independently monitored during the course of stress testing but the test line is used as its own temperature monitor. Also, test line temperatures may reach 250°C in a very short time and when this happens lattice diffusion becomes significant and hence these results are not accurate in estimating the equivalent stress under normal operating conditions where grain boundary diffusion dominates.

In spite of the above deficiencies, fast tests are becoming popular in the industry and in the military/aerospace VLSI circuit qualification programmes [33]. However, at present many of the IC manufacturers are running classical tests also to 'satisfy the customers' because the validity of these fast tests is yet to be established Nevertheless, efforts are continuing to make these tests more acceptable.

3.6 Mass Transport Measurement [34-36]

This type of experiment measures directly the net amount of mass transport caused by electromigration. It may be recalled that electromigration may result in mass accumulation or depletion depending on the flux divergence at a triple point. This mass transport is usually manifested by formations of hillocks and voids. The aim of the experiment is to measure the total volume of the voids and/ or hillocks as a function of time. Usually a transmission electron microscope (TEM) is used for this purpose. However, there are obvious limitations of this method to evaluate metallisation reliability for routine process monitoring. For example, access to specialised instruments and sample preparation difficulties. Also, because TEM requires suspended films, accurate temperature measurements present a problem due to the existence of large thermal gradients.

Bibliography

[1] F.M.d'Heurle and P.S.Ho. Electromigration in thin films. In *Thin Films: Interdiffusion and Reactions*, chapter 8. Wiley-Interscience, New York, 1978.

[2] Junko Komori and J Mitsuhashi. A fast testing of electomigration immunity using noise measurement technique. *Proceedings, IEEE International Conference on Microelectronic Test Structures*, 4 (1) :257–261, 1991.

[3] M.Ravindra. Rapid wafer level evaluation of metallisation reliability. study-report, EMF, University of Edinburgh, 1989.

[4] R. E. Jones and L. D. Smith. Wafer level isothermal joule heated electromigration test structures (WIJET). *J. Applied Physics*, 61(9) :4670–4678, 1987.

[5] J. R. Black. Electromigration — a brief survey and some recent results. *IEEE Transactions on Electron Devices*, ED-16(4) :338–347, 1969.

[6] M. J. Attardo and R. Rosenberg. Electomigration damage in aluminium film conductors. *J. Applied Physics*, 41(6) :2381–2386, 1970.

[7] S. P. Sim. Procurement specification requirements for protection against electromigration failures in aluminium metalliisation. *Microelectronics and Reliability*, 19(3):207–218, 1979.

[8] A.J.Learn. Effect of structure and processing on electromigration -induced failure in anodized aluminium. *J.Applied Physics*, 44(3) :1251, 1973.

[9] P. M. Smith, J. R. Lloyd, and G. S. Prokop. Lot-to-lot variations in electromigration performance for thin film microcircuits. *J. Vaccum Science&Technology A*, 2(2–part 1) :220–224, 1984.

[10] D. F. Frost and K. F. Poole. A method for predicting VLSI device reliability using series models for failure mechanisms. *IEEE Transactions on Reliability*, R-36(2) :234–242, 1987.

[11] D.F.Frost, K.F.Poole, and D.A.Haeussler. RELIANT: a reliability analysis tool for VLSI inerconnects. *IEEE custom integrated circuits conference*, pages 27.8.1–27.8.4, 1988.

[12] P. B. Ghate. Electromigration induced failures in VLSI interconnects. *Reliability Physics, IEEE Annual Proceedings*, pages 292–299, 1982.

[13] Bryan Root. Metallisation reliability. Sienna Technologies Inc. catalogue, 1991.

[14] Harry A. Schafft, Tammy C. Staton, and John Mandel. Reproducibility of electromigration measurements. *IEEE Transactions on Elecron Devices*, ED-34(3) :673–681, 1987.

[15] D.J.Lacombe and E.Parks. *Reliability Physics, IEEE Annual Proceedings*, pages 74–80, 1985.

[16] J. R. Lloyd. Study of electromigration induced resistance and resistance decay in aluminium thin film conductors. *Reliability Physics, IEEE Annual Proceedings*, pages 161–168, 1987.

[17] Y. Z. Lu and Y. C. Cheng. Measurement technique of electromigration. *Microelectronics and Reliability*, 23(6):1103–1118, 1983.

[18] R. W. Pasco and J. A. Schwarz. The application of a dynamic technique to the study of electromigration kinetics. *Reliability Physics, IEEE Annual Proceedings*, pages 10–23, 1983.

[19] R. Rosenburg and L. Berenbaum. Resistance monitoring and effects of nonadhesion during electromigration in aluminium films. *Applied Physics Letters*, 12(5) :201–204, 1968.

[20] A. Bobbio and O. Saracco. Electromigration failure in aluminium thin films under constant and reversed DC powering. *IEEE Transactions on Reliability(USA)*, R23:194–202, 1974.

[21] R. E. Hummel, R. T. Dehoff, and H. J. Geier. Activation energy for electrotransport in thin aluminium films by resistance measurements. *J.Phys.Chem.Solids*, 37:73–80, 1976.

[22] K. P. Rodbell, M. V. Rodriguez, and P. J. Ficalora. The kinetics of electromigration. *J. Applied Physics*, 61(8–part1) :2844–2848, 1987.

[23] L. Bacci, C. Caprie, and G. Desanti. Electromigration control: the accelerated BEM test. In *ESSDERC'87*, pages 373–376.

[24] F. Fischer and J. Fellinger. Failure analysis of thin-film conductors stressed with high current density by application of Matthiessen's rule. In *Reliability Physics, IEEE Annual Proceedings*, pages 250–256, 1977.

[25] R. W. Pasco and J. A. Schwarz. Temperature ramp resistance analysis to characterize electromigration. *Solid State Electronics (GB)*, 26(5) :445–452, 1983.

[26] L. F. Felton, J. A. Schwarz, R. W. Pasco, and D. H. Norbury. Effects of composition and structure on electromigration kinetics in aluminium-alloy thin films. *J.Applied Physics*, 58(2) :723–727, 1985.

[27] K.Sato et al. Combined resistance and temperature change measurement for the study of electromigration. *Vacuum*, 41(4–6) :1229–1230, 1990.

[28] G. Specchiulli, F. Fantini, and G. Desanti. Electromigration in narrow aluminium-silicon stripes for VLSI: Comparison between MTF and resistom-

rtric methods for life predictions. *Solid State Devices Proceedings*, pages 369–372, 1987.

[29] B. J. Root and T. Turner. Wafer level electromigration tests for production monitoring. *Reliability Physics, IEEE Annual Proceedings*, pages 100–107, 1985.

[30] C. C. Hong and D. L. Crook. BEM- a new technique for monitoring metallisation reliability at wafer level. *Reliability Physics, IEEE Annual Proceedings*, pages 108–114, 1985.

[31] Marshall Davis and Fred Hass. Inline wafer level reliability monitors. *Solid State Technology*, pages 107–110, May 1989.

[32] M. Kemalkhan and L. Schmidt. Understanding electromogration: a simple new life profile technique. *Semiconductor International*, (11):102–106, 1989.

[33] V.Tyree. Wafer level reliability testing and control. *Interuniversity Microelectronics Center (Belgium), summer course*, 1989.

[34] I.A.Blech and E.S.Meieran. Electromigration in thin aluminium films. *J. Applied Physics*, 40(2):485–491, 1969.

[35] J.Weiss. Quantitative measurements of the mass distribution in thin films during electrotransport experiments. *Thin Solid Films*, 13:169, 1979.

[36] L.Berenbaum. Electromigration damage of grain-boundary triple points in aluminium thin films. *J. Applied Physics*, 42:880, 1971.

Chapter 4

Limits of Conventional Tests

4.1 Introduction

It was outlined in chapter 1 that statistical process control measures are becoming necessary to achieve higher levels of quality and reliability. It was also pointed out that a large number of interacting factors affect electromigration and hence the problem cannot be solved by just monitoring all the process variables. Nevertheless, manufacturing priorities are to reduce process variations and to keep process parameters closer to target specifications. This is usually stated as aiming for a process capability, $C_p \geq 2$. This term is briefly explained in section 4.2. By these process control measures, an improvement in yield and an overall improvement in quality and reliability [1] have been demonstrated. Thus, process controls leading to increased C_p may be expected to result in more reliable metallisation since that result is contained in overall failure rates. However, the conventional electromigration MTF tests may fail to meet our expectations of a direct causal link to process capability data. This is mainly because MTF is essentially determined by the failure times of the weak-spots in the lines under test rather than the average values represented by C_p values. Also, the sample size determines the accuracy of the measurements. Section 4.4 discusses these issues in detail.

There are many metallisation process parameters for which it is becoming necessary to adopt the process control measures. However, one parameter, namely linewidth is discussed in detail in section 4.3 because it is one of the critical process parameters affecting electromigration MTF and it is also very important from

yield considerations. To preserve device yield it is essential to maintain the target linewidth specifications not only over the entire wafer, but for all wafers in a batch and from batch to batch [2]. The present trend in linewidth measurement is to move away from the conventional spot-checks, and to get an average value over an area of a wafer [2, pages:199-200].

4.2 Process Capability

Two yardsticks, C_p and C_{pk}, have become standard terminologies in the area of statistical quality control in recent years [3]. The usual definitions and the formulae are given in Figure 4-1. USL and LSL stand for upper specification limit and lower specification limit respectively.

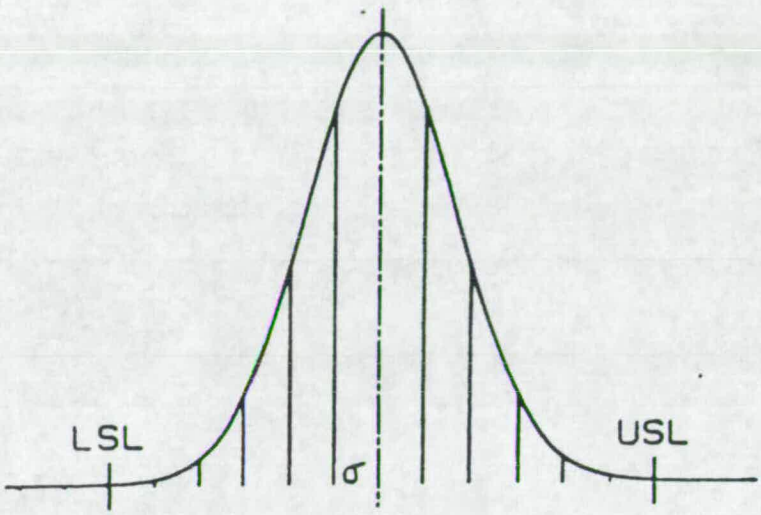
C_p does not take into account any noncentering of the process relative to the specification limits of a parameter. Such noncentering reduces the margin of safety and this is taken into account in the parameter C_{pk}. For example, when the process mean and the target value coincide, k is reduced to zero making C_p and C_{pk} equal. If, however, the process mean is skewed toward one end or the other of a specification limit the value of k increases, causing a decrease in C_{pk}. Thus C_{pk} is a measure of both spread and noncentering. Generally for critical parameters the aim is to attain $C_p \geq 2.0$ and $C_{pk} \geq 1.5$) [4]. Within the semiconductor industry, these statistical control procedures are being more widely introduced for control of all physical dimensions, layer thicknesses, etc.[5].

4.3 Linewidth Control

4.3.1 Factors affecting linewidth control

There are a large number of photolithographic and etch process parameters which control the minimum feature size achievable and variation in linewidth from sample to sample [6,7,8,9].

CAPABILITY INDEX



$$C_p = \frac{USL - LSL}{6\sigma}$$

$$C_{pk} = C_p(1-k)$$

$$k = \left| \frac{\text{target value} - \text{process mean}}{\text{specification width}/2} \right|$$

Figure 4–1: Definitions and formulas for C_p and C_{pk}

Variation can be due to:

1. The quality of the optical system producing the image.

2. Variations in exposure.

3. Resist–image–substrate interactions.

4. Etch variations.

Some of the above in turn depend on a number of other parameters. For example, resist–image–substrate interactions include a wide variety of process parameters like resist type, spinner rotational velocity, bake time and temperature, reflectivity of the substrate, etc. Non-uniform etching may be caused by the plasma machine configuration, composition of the plasma, etc. In the case of wet etch— concentration of the chemicals, temperature and time.

A functional relationship derived by Einspruch [10] based on a simplified model connects the fractional change in line-width to photolithography parameters as follows:

$$\frac{\Delta W}{W} = \frac{1}{2M}\left[\left(\frac{\Delta E}{E}\right)^2 + \left(\frac{\Delta P}{P}\right)^2\right]^{1/2} \tag{4.1}$$

where M stands for the modulation transfer function of the imaging system . The first term ($\frac{\Delta E}{E}$) in the bracket is the fractional change in exposure (expressed in terms of radiation intensity multiplied by time duration). The second term ($\frac{\Delta P}{P}$) is the fractional change in the 'threshold exposure' of the resist. The 'threshold exposure ' includes the effects of the development process, resist thickness, spectral composition of the radiation and optical properties of the underlying substrate. In short, this term represents non-uniformities in resist processing.

The above equation despite its simplifying assumptions helps to approximately estimate the relative contribution of the various parameters. For example, equation 4.1 clearly shows that large image modulation transfer function (M) is the

most important factor in achieving good linewidth control. Increasing M can reduce the effect of non- uniformities in exposure and process variations. To achieve ±10% linewidth control at 60% modulation with a non-uniformity of exposure of ±10% leaves around ±6% allowable variation for the rest of the process.

The equation contains a subtle relationship between focus and linewidth control as a result of M in the denominator. When the optical system becomes defocused, M decreases causing more linewidth variations.

4.3.2 Linewidth Measurements

Linewidth measurements for process monitoring purposes have traditionally been based on optical or SEM inspection or electrical measurements of test structures on process control chips [11]. In the latter case, linewidth data are taken by measuring the resistance of bridge resistors of known length and then calculating the linewidths based on the sheet resistance, as determined from the adjacent van der Pauw structures [12]. Such systems usually produce linewidth uniformity maps of wafers. But electrical probing techniques are restricted to conducting layers, and can not measure photoresist. Optical techniques can measure resist but they have some dependency on the exact measurement location on the wafer, small bumps, scratches etc. An integrated measurement over a localized area would give a more accurate picture of linewidth dimensions at each site. But it can easily result in a measurement routine that is too slow for production purposes. There is a need for a non-destructive fast scan system for monitoring linewidth uniformity across wafers for routine process monitoring and this was the motivation behind one of the PhD projects at the EMF [2]. This research [2] led to the development of a new test structure – chequerboard test structure– to measure linewidth uniformity for process control [2, pages, 199-230]. In essence, the technique involves a simple optical measurement of a large area test pattern consisting of an array of alternate clear and opaque squares. Using an aluminium chequerboard over the entire surface of a glass wafer the sensitivity of the technique has been demonstrated [2, page,237]. Using white light in transmission through a glass wafer, variation

of only 5% in linewidth across the wafer becomes visible to the naked eye. Also it reveals details such as non-uniformities in photoresist spinning. Since the chequerboard test structure is also relevant from electromigration point of view also, it is briefly described in chapter 5.

A sample linewidth contour map and focus exposure curves for the EMF process are shown in Figure 4–2 and Figure 4–3 [2, pages, 110-111]. The plots are generated from the commonly used Prometrix Lithomap LM20 system for linewidth process monitoring. This is an electrical probing system and hence can be expected to yield an integrated measurement over the entire area of a track. The linewidth contour map in Figure 4–2 shows variations in linewidth across the wafer for nominal exposure and focus conditions. Referring to equation 4.1, under nominal exposure conditions, $\left(\frac{\Delta E}{E}\right)$ is small because the exposure is nearly constant, but $\left(\frac{\Delta P}{P}\right)$ varies depending upon the process variations across the wafer and hence the variations in linewidth shown in the linewidth contour map are mainly due to process variations. The focus exposure curves in Figure 4–3 show variations in linewidth when exposure and M, the modulation transfer function in equation 4.1 are varied.

In summary, Figures 4–2 and 4–3 indicate that in order to reduce linewidth variations, uniformity in other process parameters such as photoresist processing, exposure etc. should be carefully maintained.

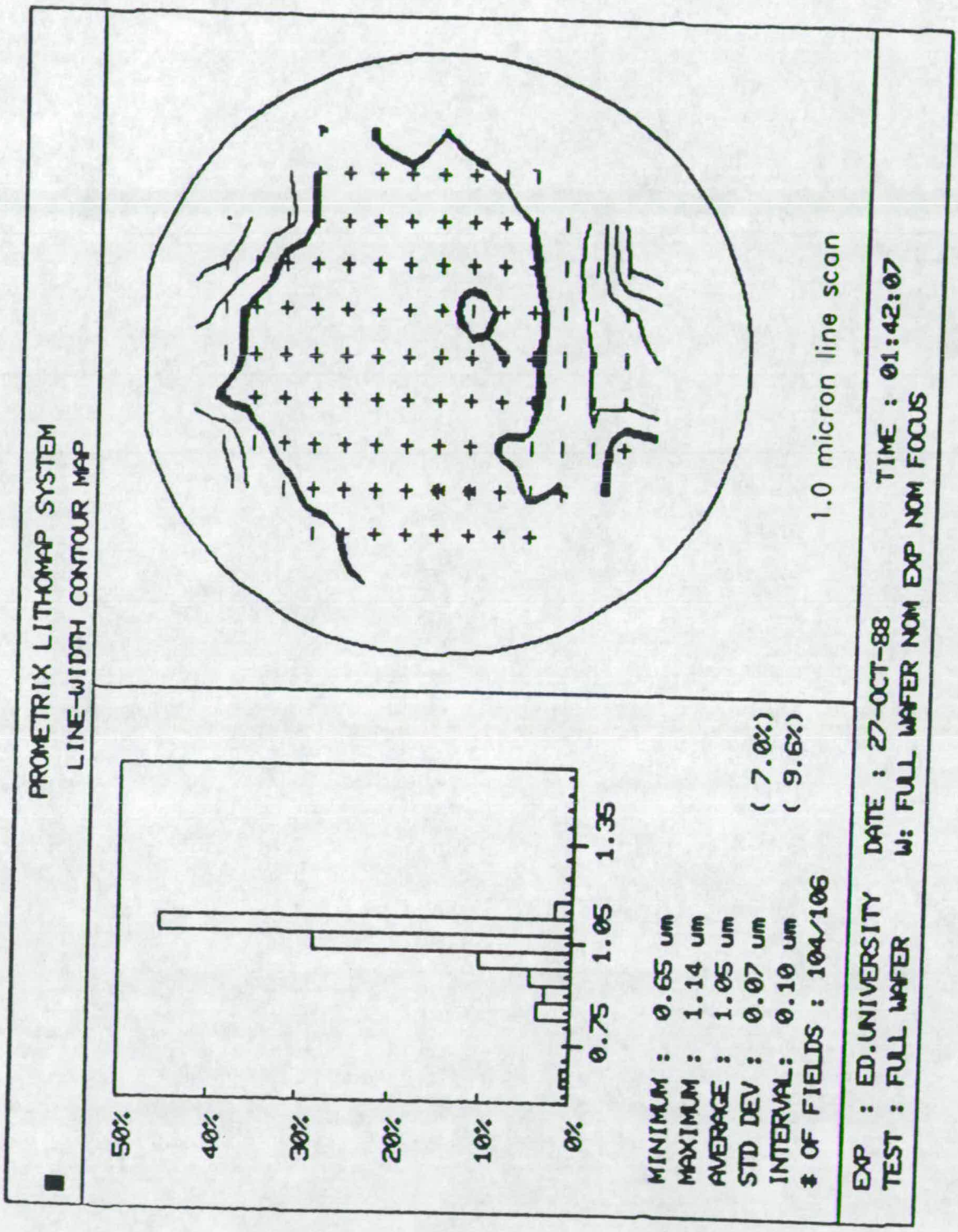


Figure 4–2: Linewidth contour map

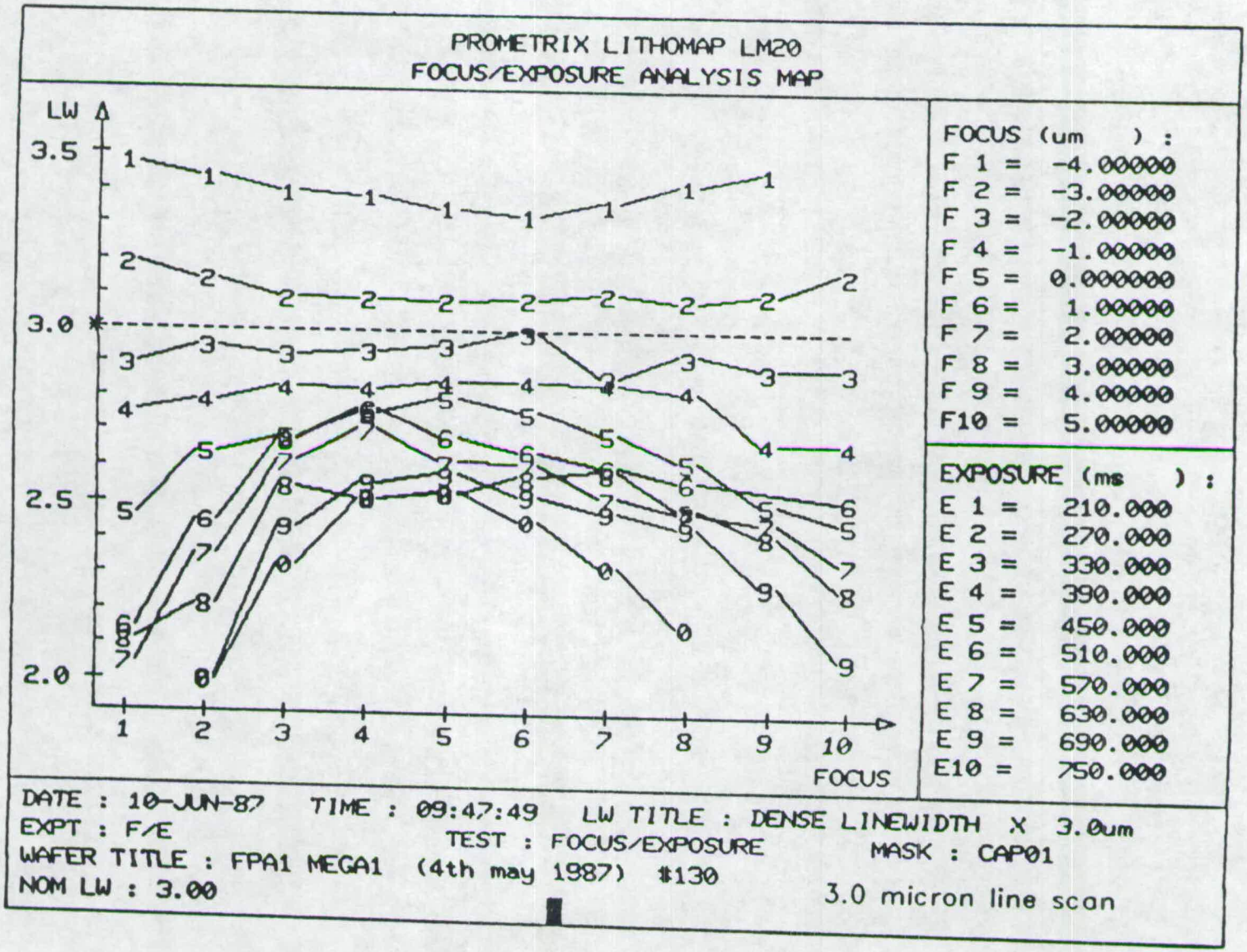


Figure 4-3: Focus/exposure curves

4.4 Conventional MTF tests and metallisation process monitoring

Conventional MTF tests are popularly used for metallisation quality and reliability evaluations because they have a very good empirical base, i.e. they 'work well' and have been widely accepted by the microelectronics industry, despite the fact that they take prolonged test times. It is natural to expect that the metallisation process control measures such as linewidth control should result in an overall improvement in quality and reliability of IC metallisation. However, a closer look indicates the following disadvantage and limitation if we want to use them for routine metallisation process monitoring in general, and linewidth control in particular.

4.4.1 Sample Size

Sample size plays an important role in determining the accuracy of the electromigration lifetime measurements. This is evident from the Figure 4–4 based on the mathematics of failure distributions [13]. In this figure, t_{50} is the MTF of the samples, t_{50_a} is the population MTF , s is the standard deviation of the failure distribution and n is the sample size. By population MTF we mean the MTF obtained when a very large number of samples are used (theoretically, when $n \rightarrow \infty$) . When n=400 the sample MTF is close to the population MTF with an error of about $\pm$ 10%. But, as the sample size is decreased below 400, the sample MTF deviates more and more from the population MTF, depending on the standard deviation. For example, when s=0.6 and n =10, $\frac{t_{50}}{t_{50_a}}$ can be expected to be within the range [0.5 to 1.5] with 90% confidence. That is, there may be an error of about $\pm$ 50 % in the sample MTF. However, although theory demands a large number of samples for an accurate analysis, cost and time considerations are usually prohibitive. In practice, a sample size of around 10 is generally chosen.

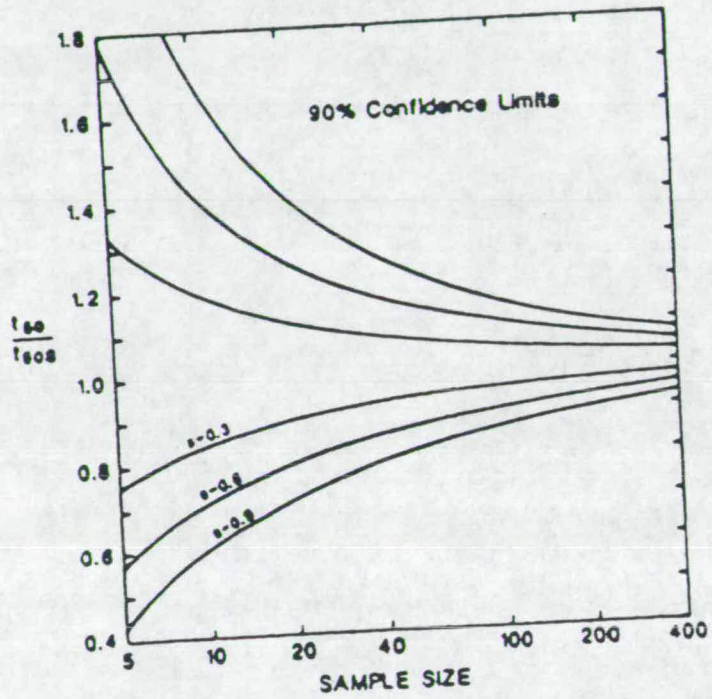


Figure 4–4: Ninety-percent confidence limits for t_{50} divided by t_{50_s} versus sample size for three sample estimates of sigma

In resistometry, it may be recalled that small sample sizes may not produce large errors because MTF extraction is based on average mass transport over the entire line and any metallisation line contains a large number of electromigration damage sites.

4.4.2 MTF and Process Capability

The process control measures to improve the process capability, C_{pk}, usually make the distributions narrower and decrease k. In the case of linewidth control, this means aiming for smaller linewidth variations across a wafer and from wafer to wafer in a batch and from batch to batch. Also the mean linewidth has to be kept closer to the specified linewidth so that k remains small. In practical terms this demands the maintenance of uniformity in photoresist processing, etch control etc. across a wafer. The emerging technique using chequerboards is promising for measuring these parameters over an area of the wafer. However, the MTF measurements may not be linked to C_{pk} because the failure time is determined by the weak-spot in a metallisation line and not to the average mass transport over the entire line.

When small number of samples are used, as is the common practice, the problems are much more serious.

Apart from the errors that may result because of the small sample size, irreproducible results may also be obtained if the samples are not properly screened. This is because, gross defects such as localized overetched areas, scratches etc., may determine the failure time of the entire line. However, in the experiments where a small number of samples are used (as in the case of this project – reported in chapter 3) the samples are usually visually inspected and only good devices are taken for stress experiments. But, even screening may not solve the problem completely, because some of the defects may go undetected even under high reliability military/aerospace quality control inspections such as MIL-STD-883D [14, 15,16].

In summary, it is difficult to estimate the population MTF from conventional MTF measurements because of sample size and other considerations and also difficult to link conventional MTF results to C_{pk}. However, in contrast to the conventional MTF measurements, it may be recalled that in resistometry, resistance increase due to electromigration is monitored. The mass transport along the entire line due to electromigration contributes to resistance change and hence the extracted MTF can be expected to be better linked to C_{pk}.

4.5 Chapter Conclusions

1. There are many critical process parameters which affect electromigration. Linewidth is one of the most important parameters for the present submicron geometry VLSI circuits. It is also very important from yield considerations.

2. Figures 4–2 and 4–3 show that there are many factors which cause linewidth variations across a wafer. The latest trend in statistical quality control strategy is to reduce these variations, in addition to the traditional approach, namely, inspections and screening tests on the end-products. New techniques which give an integrated measurement over an area of a wafer are becoming necessary to maintain linewidth uniformity. One new technique uses a novel test structures namely, a chequerboard for demonsration of linewidth control. This structure appears to be useful from the electromigration point of view also.

3. Routine process monitoring for critical parameters that affect electromigration using conventional MTF tests is difficult because of sample size and other considerations.

4. Conceptually, resistometry appears to be better suited for the above purpose (process monitoring) than conventional MTF tests.

Bibliography

[1] E.A.Amerasekera and D.S.Campbell. *Failure Mechanisms in Semiconductor Devices*, chapter 10, pages 135–142. John Wiley & Sons, 1987.

[2] Iona Binnie. *Critical dimension control: influencing factors and measurement.* PhD thesis, University of Edinburgh, 1991.

[3] Keki.R.Bhote. *World Class Quality.* AMA Membership Publications Division, New York, 1988.

[4] J.M.Robertson. Product performance and optimisation. A course for Motorola, East Kilbride, 1992.

[5] M.Aceves, J.A.Hernandez, and R.Murphy. Applying statistics to find the causes of variability in aluminium evaporation: a case study. *IEEE Transaction on Semiconductor Manufacturing*, 5(2):165–167, 1992.

[6] D.S.Perloff. VLSI process monitoring: current practice/future trends. *Microelectronics Measurement Technology Seminar*, pages 300–305, 1979.

[7] J.H.McCoy, W.Lee, and G.L.Varnell. Optical lithography requirements in the early 1990s. *Solid State Technology*, 3:87–92, 1989.

[8] A.S.Oberai. Lithography- challenges of the future. *Solid State Technology*, 9:123–128, 1987.

[9] R.L.Rieger and J.A.Schoeffel. Managing lithography errors. *Solid State Technology*, 4 :151–155, 1989.

[10] N.G.Einspruch, editor. *VLSI Electronics: Microstructure Science*, volume 1, chapter 2. Academic Press, 1981.

[11] N.N.Kundu, K.I.Arshak, and B.Lane. A new test structure for misregistration evaluation. *Proceedings of Microcircuit Engineering*, pages 687–691, 1989.

[12] N.N.Kundu, K.I.Arshak, and B.Lane. Plasma etch characterization using electrical linewidth measuring techniques. *Integrated Circuit Metrology, Inspection and Process Control*, pages 687–691, 1989.

[13] H.Schafft and J.A.Lechner. Statistics for electromigration testing. *Relability Physics, IEEE Annual proceedings*, pages 192–201, 1988.

[14] Military Standard : Test methods and procedures for microelectronics: MIL-STD-883D. US Department of Defense, Washington, 1988.

[15] R.T.Howard. Package reliability–how to define and measure it. *IEEE Transactions on components, hybrids and manufacturing technology*, 5:454–462, 1982.

[16] C.M.Ryerson. Reliability testing and screening: a general review paper. *Microelectronics and Reliability*, 17:367–377, 1978.

Chapter 5

Some Studies on Chequerboards

5.1 Background

Patterns of squares as shown in Figure 5–1 are routinely used in the EMF (Edinburgh Microfabrication Facility) to optimise development and etching conditions [1,2]. They are commonly added to a mask or reticle to provide a rapid visual indication that the layer has been correctly exposed/developed/etched. The principle is: if under-development/etching has occurred, the squares overlap at the corners and conversely, with over-development/etching the squares become isolated from each other. Only when the process is correct, will the squares just contact at their respective corners. These three cases are shown in Figure 5–2.

Figure 5–2 does not show the finer details at the corners. In reality rounding off (Figure5–3) at the corners occur depending on the resolution and modulation transfer function of the optical exposure system.

The optical characteristics of chequerboard test patterns have been shown to give an excellent visual representation of the effect of severe lithographic factors that determine linewidth uniformity and the inadequacy of using spot checks of critical dimensions to monitor the process [1]. Aluminium chequerboards on the surface of glass wafers were used to show the deviations in linewidth in terms of an area change on the chequerboard. Electrical resistance of chequerboard structures are also being studied to monitor the under/over-etch[3].

When this project started, a large number of micrographs and experimental database from earlier projects were available. From these it was clear that chequer-

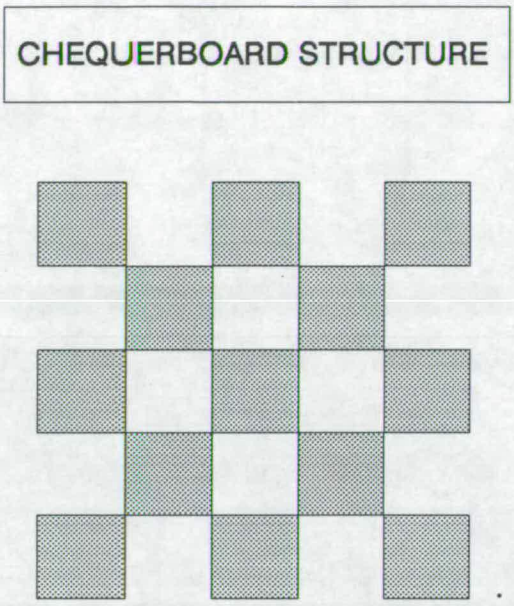


Figure 5–1: chequerboard structure for rapid visual monitoring of linewidth

board structures could be used to generate a large number of nominally identical micron to sub-micron width segments distributed over an area. There are some striking features of these structures from the electromigration point of view:

- Localisation of electromigration damage sites to the overlap regions because of higher current density due to smaller cross sectional area.
- Possibility to include a large number ($\sim$ 1000) of nominally identical segments in one structure to extract mass transport data which can be considered to be very close to the 'effective' average value.
- The chequerboard structures may provide efficient heat dissipation from the overlap regions through the large metal squares and this may yield spike-free resistance versus time curves.
- Sub-micron to deep sub-micron width segments could be fabricated using the standard optical lithography techniques.

The first step was to study the current density distribution in the overlap segments. PISCES-2B [4] software was used to do this and the results are given in section

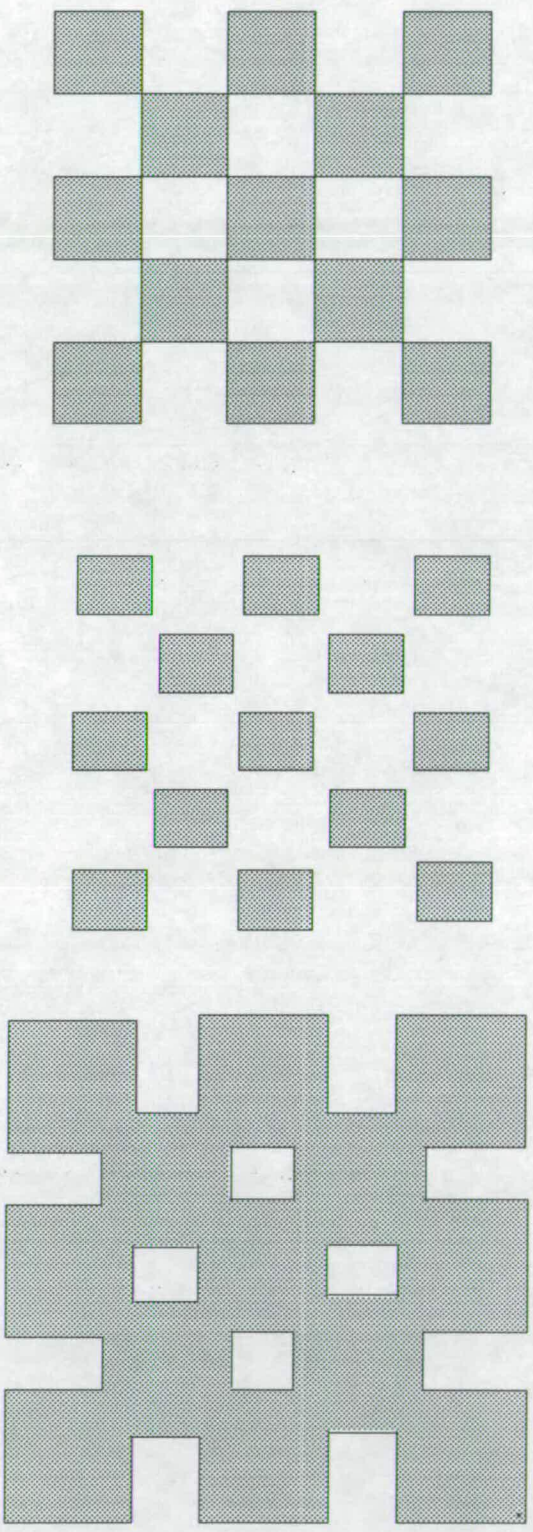


Figure 5–2: Correct-etch (Top), over-etch (Middle), under-etch (Bottom)

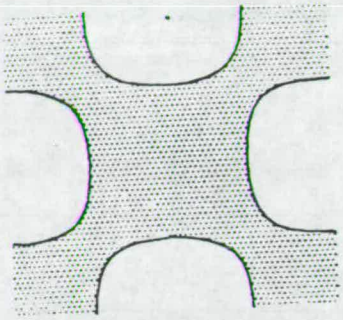


Figure 5–3: Rounding off at the corners

5.2. The heat-sinking aspects are discussed in section 5.3. It was also thought appropriate to do some preliminary integrity tests with these structures before designing the structure for electromigration studies. This was because the structures are radically different from those normally used for electromigration studies. The results of some of these experiments are given in section 5.4. This is followed by the proposed electro- migration failure model for chequerboard structures.

5.2 Current-density Simulations of Chequerboard Structures

Figure 5–4 shows a sample plot of the current flowlines for a 6μm chequerboard with an overlap of 0.2μm. The plots were derived from simulations with PISCES-2B for a current of 25 mA. They show the current peaking in the centre of the segments as expected.

A current density vector plot for one of the overlap segments is shown in Figure 5–5. In this figure the length of the arrow is proportional to the current density at the given point. It is apparent from this figure that the current density at the corners is much higher than at the centre. This is due to the current crowding effects at the corners. The arrows are more closely spaced in the centre of Figure 5–5 because of the close grid spacing used in this region during simulation. In these simulations only 90^o corners for the metal pattern were used. The effect of the rounding off that occurs at the corners can be shown by replacing the 90^o corners with a typical curvature geometry.

The graph of Figure 5–6 shows the variation of current density along the line AB from one corner to the other, when curvature effects are considered. The segment with the minimum time to failure in a chequerboard can be expected to be the one having the highest current density at the corners and also having the largest value of microstructural parameter η in the vicinity of the corner. A failure leading to the discontinuity ('open') may propagate from one of these sites.

5.3 Heat Dissipation in Chequerboards

The large metal squares of the chequerboards are expected to provide an efficient heat dissipation path for the temperature increase caused by Joule heating. Before a steady state temperature is established across the chequerboard, we can expect the temperature to be maximum at the overlap regions. The thermal stabilization time is determined by various thermal time constants and this aspect is discussed in Appendix E. Also, some of the general concepts such as thermal resistance, thermal capacity etc. are defined and discussed in Appendix E. An approximate estimation of the efficiency of chequerboards compared to the conventional long tracks in dissipating the Joule heat is given below.

Consider an unit element of a chequerboard structure as shown in Figure 5–7 (a). Mainly there are two components of the heat flow as shown in Figure 5–7 (b): one is the conduction through the metal pads A and B and the other

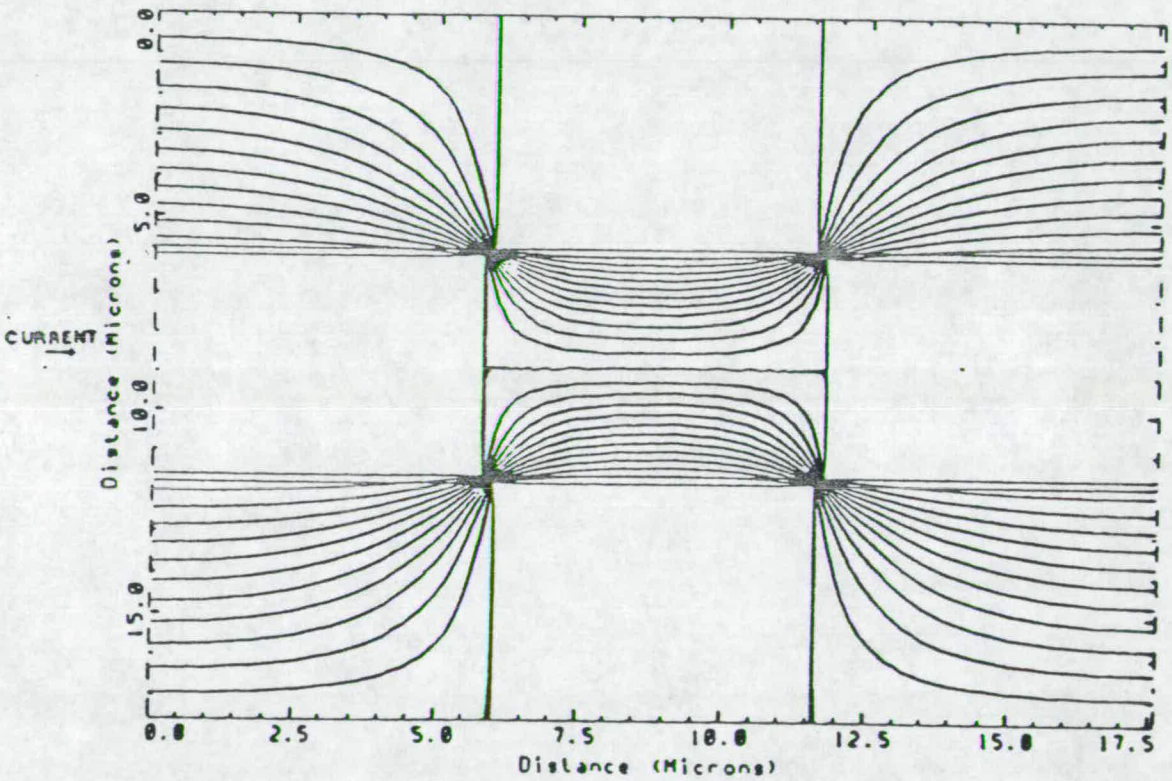


Figure 5–4: Current flowlines

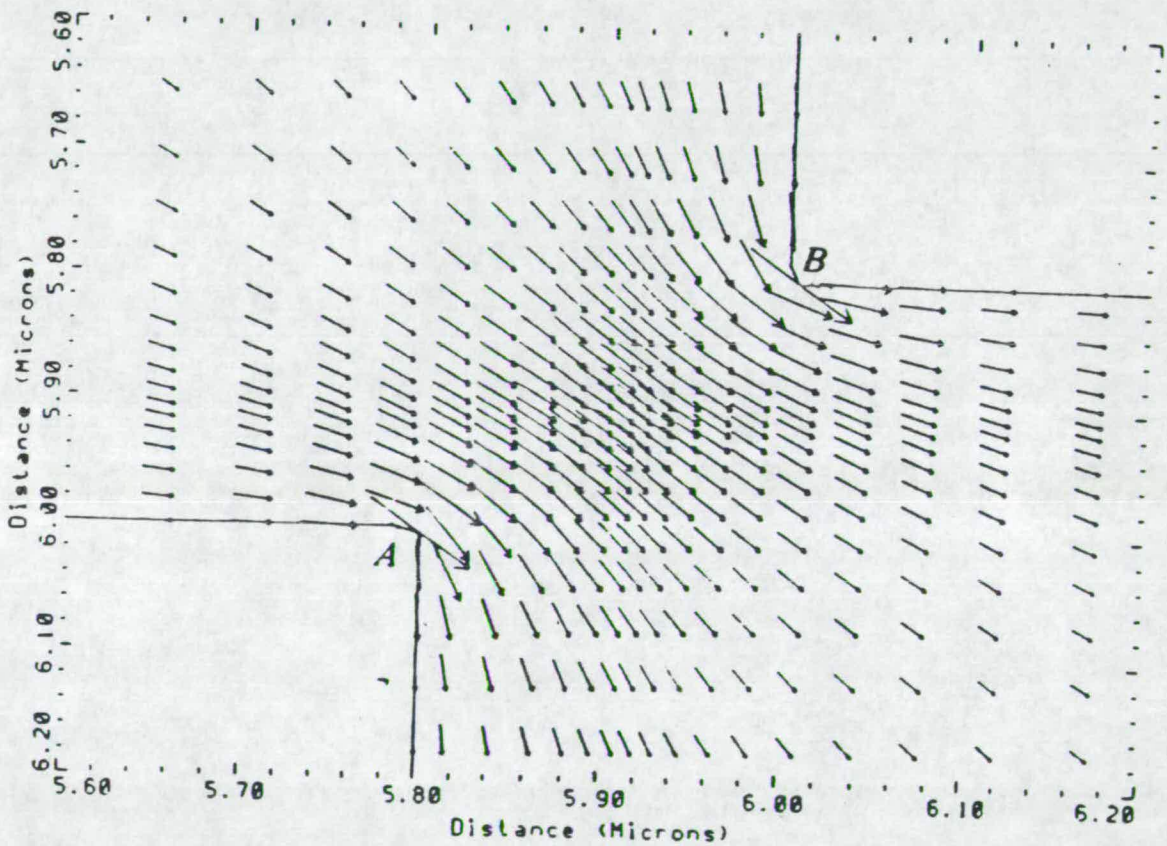


Figure 5–5: Current density vector plot

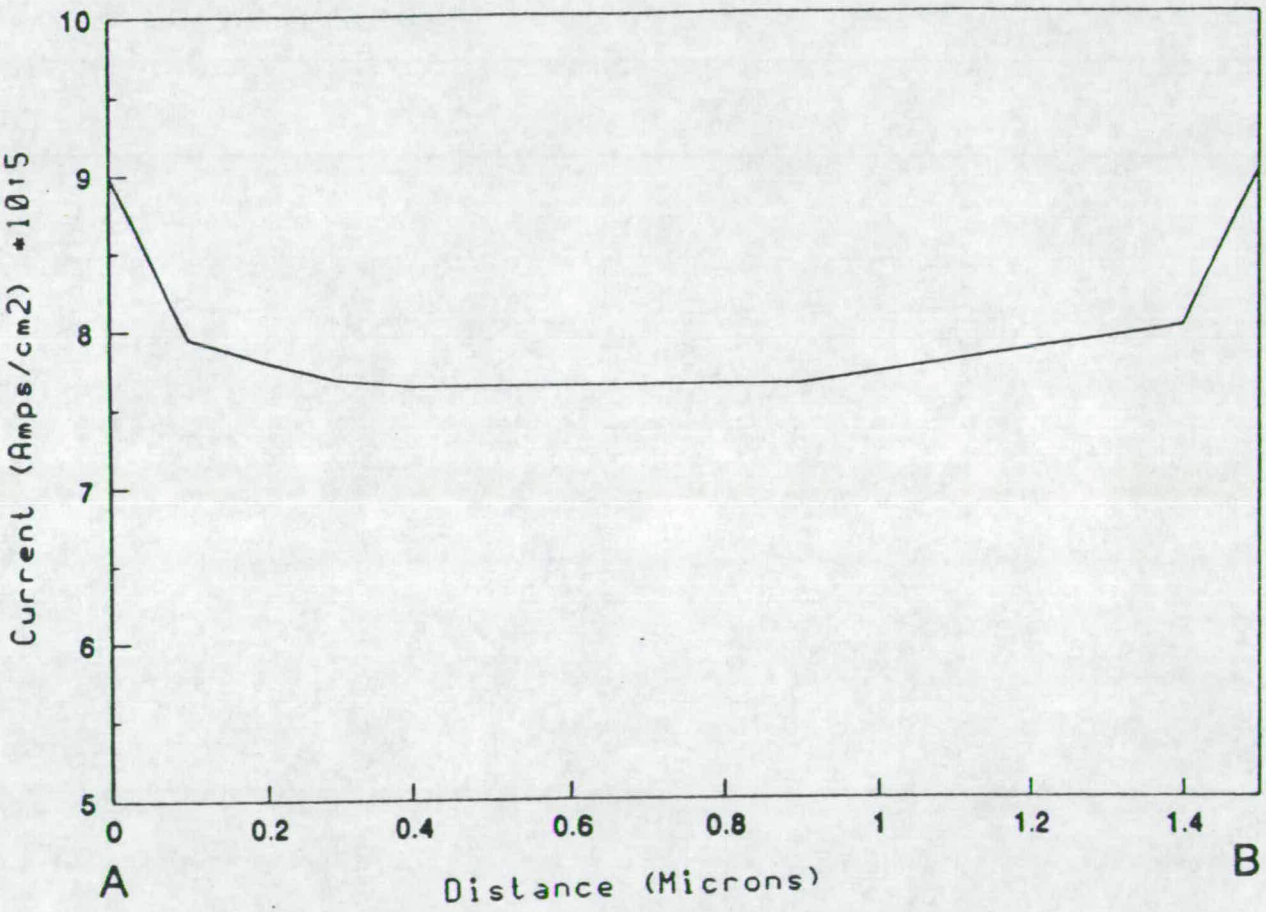


Figure 5–6: Current crowding effects

is the conduction through the oxide-wafer-chuck sandwich and into the outside environment.

The thermal resistance for the heat conduction towards the metal pads A and B can be expressed as:

$$R_m = \frac{L}{K_m w t_m} \tag{5.1}$$

where,

R_m = thermal resistance for heat conduction across the metal

K_m = thermal conductivity of the metal

t_m = metal thickness

the width w and length L of the metal as defined in Figure 5–7(a). Similarly, the thermal resistance for the conduction heat flow through the oxide-wafer-chuck sandwich (R_o) may be approximately expressed as:

$$R_o = \frac{t_o}{K_o w L} \tag{5.2}$$

where,

t_o = oxide thickness

K_o = thermal conductivity of the oxide

It may be noted that in the equation 5.2 a linear approximation to the decrease of R_o with $(\frac{t_o}{w})$ has been assumed. But, in reality non-linearities may occur due to the heat flow through the metallisation edges depending on w and t_o. However, for the calculations shown here, this is a reasonable approximation because while discussing the results later we are considering the orders of magnitude only.

Now, the ratio $(\frac{R_o}{R_m})$ is used as a figure of merit to compare the effectiveness of the heat dissipation through the large metal squares. That is, the higher the ratio the higher is the effectiveness. (Note that the figure of merit is $(\frac{R_o}{R_m})$ and not $(\frac{R_m}{R_o})$). The length L is varied from 1 μm to 1000 μm, the latter length is the typical length of a conventional electromigration test structure. Using the following values for the material constants and the oxide and metal thickness:

$K_m = 2.38 W/cm^{\circ}C$

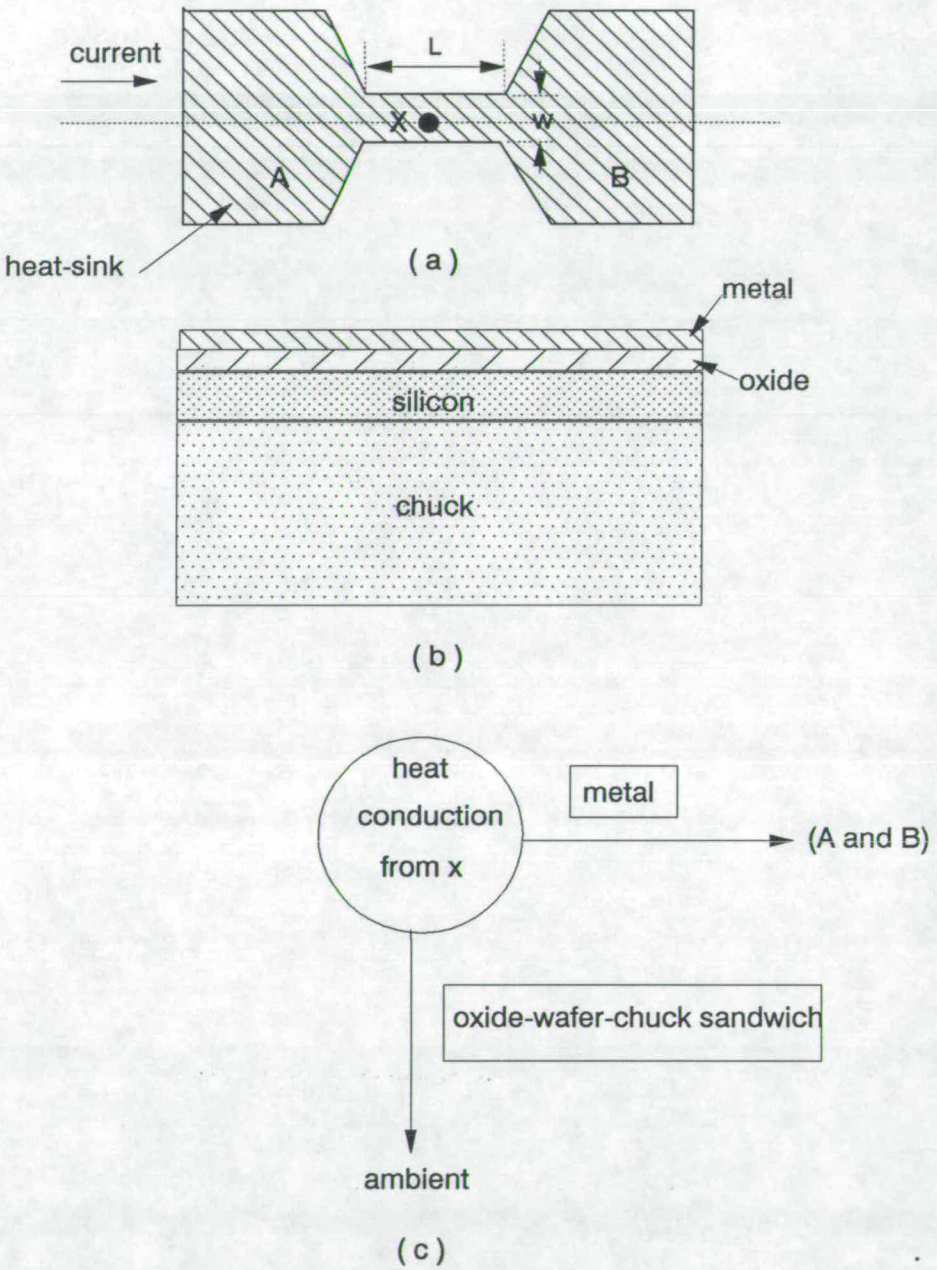


Figure 5–7: Heat conduction from the overlap region of a chequerboard

L (μm)	$(\frac{R_o}{R_m})$
1	248
10	248×10^{-2}
100	248×10^{-4}
1000	248×10^{-6}

Table 5–1: Relative heat conduction (metal versus oxide) values

$K_o = 0.0096 W/cm°C$

$t_m = 1\mu m$

$t_o = 1\mu m$

the values of $(\frac{R_o}{R_m})$ for different L values are calculated and the results are given in table 5–1. From table 5–1 it is clear that the chequerboards where L is typically around $1\mu m$ provide efficient heat dissipation paths through the large metal pads unlike the conventional long tracks. For example, when $L = 1\mu m$ the heat conducted away by the pads A and B from the centre of the overlap region is about 248 times that conducted away by the oxide. Thus the metal pads A and B act as heat-sinks conducting away the Joule-heat generated in the overlap region.

The fact that the thermal conductivity of aluminium is $\simeq 248$ times that of the oxide will be used to put forth the argument that in chequerboard structures significant heat is conducted away by the squares from the segments. In classical structures where length is $\simeq 1000\ \mu m$ heat conduction through oxide is significant.

5.4 Thermal Measurements

Before using chequerboard structures to study electromigration, it was thought appropriate to study the integrity of the structures at high currents and temperatures. The structures are radically different from the conventional test layouts and this may lead to new problems, for example, a chequerboard contains a large number of high current density segments so the definition of uniformity is very d-

ifferent from the usual long track case. Temperature coefficient of resistance is one of the important parameters required in any electromigration study to estimate the temperature rise due to Joule heating. Hence, resistance versus temperature behaviour of these structures was also studied to confirm that the typical thermal behaviour of these films was linear in the temperature range of interest: 25−200°C.

5.4.1 Temperature Coefficient of Resistance Measurements

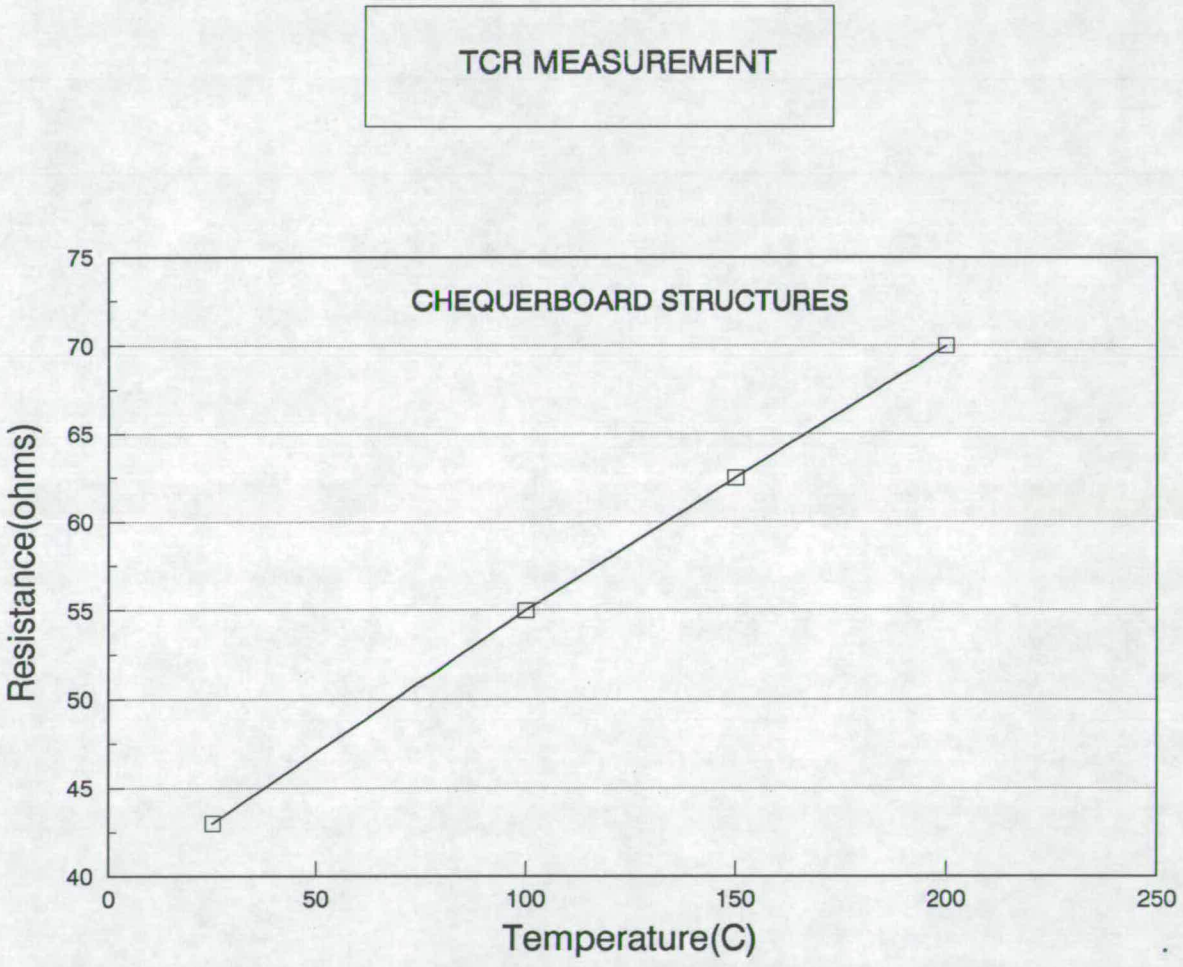


Figure 5–8: TCR measurements

The measurements were carried out using the chequerboard structures from one of the previous projects. It should be noted that these structures did not contain the commonly used four-probe arrangements for accurate resistance mea-

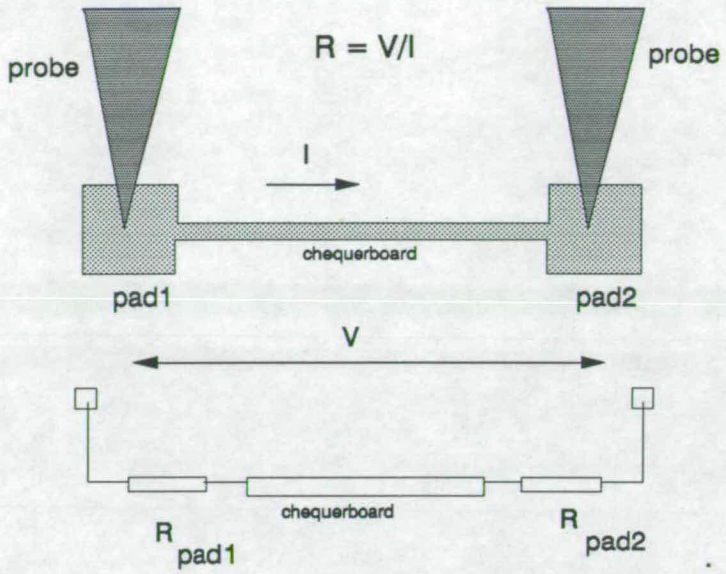


Figure 5–9: Two-probe resistance measurements

surements and were quite long ($\simeq 1cm$) giving resistances typically in the range of 40-50 ohms. The results are shown in Figure 5–8. The TCR value obtained from the graph (0.36 %/°C) contains an error due to the contact resistance between the tungsten probes and aluminium bond pads. This adds R_{pad1} and R_{pad2} in series with chequerboard structures as shown in Figure 5–9. These two resistance components may not remain constant from one measurement to the next, depending upon the contact pressure, probe placement, thermo-emf depending on the temperature etc. Nevertheless, these measurements showed the general linearity of resistance versus temperature. It may be noted that the published TCR value for aluminium-silicon films is ($\sim$ 0.39 % /°C).

5.4.2 Integrity Tests

The resistance of the chequerboard test structures was monitored at higher currents causing significant (greater than about $5°C$ and up to about 30°C) joule heating to test the integrity of these structures. The results are shown in Figure 5–10. The following observations can be made from the graph:

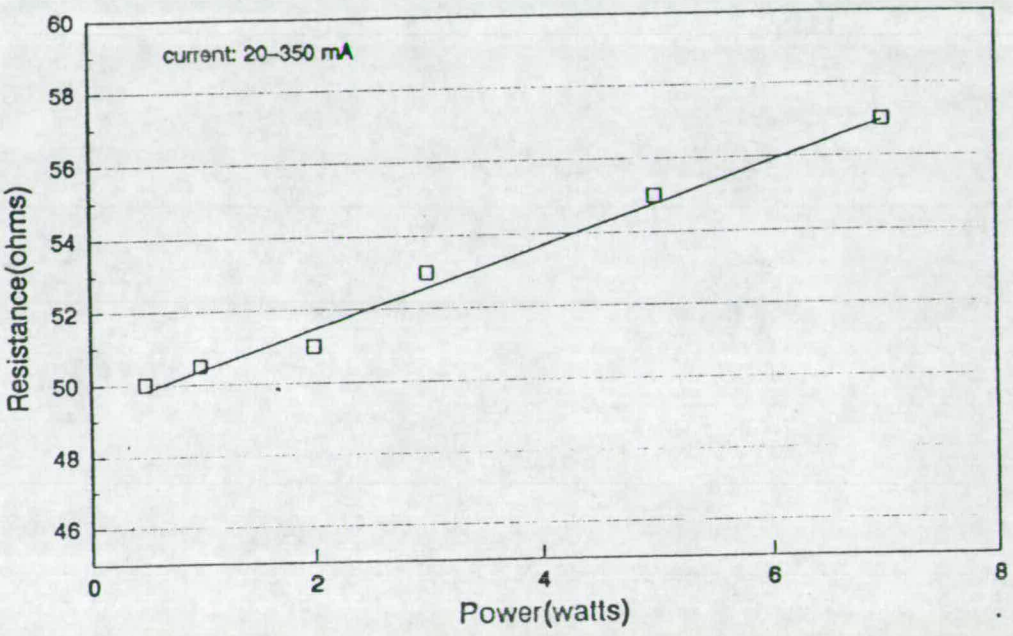


Figure 5–10: Integrity Tests

The resistance increases from about 50 ohms at low power levels ($\simeq$ 20 mA) to 57 ohms at $\simeq$ 350 mA. Using the TCR value of 0.36 % /°C this indicates a temperature rise of about 39°C. Many structures were tested at much higher currents till failure and similar graphs were obtained.

In summary, these measurements showed that there are no 'integrity' problems with these structures for electromigration studies involving high current densities and temperatures.

5.5 Electromigration Model for Chequerboard Structures

The above measurements and studies clearly indicated the general suitability of chequerboards for electromigration monitoring. In addition, resistometry appeared to be the most appropriate choice for the following reasons:

- We are mainly interested in estimating an average lifetime value from a process monitor structure so that it can be used as a check to verify process control. Resistometry techniques have a general advantage over other electromigration techniques in that these measure the average mass transport occurring over the entire stripe as opposed to 'weak spots' in the structure.

- Because of the heat-sinking effects of the chequerboard structure we can expect spike-free resistance versus time curves.

Hence, it was natural to use electromigration models which describe the resistance behaviour due to electromigration.

There have been many theoretical models that describe the nucleation of voids and their and growth during electromigration in thin films. [7,8,9,10]. But, these models do not explain the observed increase in resistance in terms of growth rate of voids. However, the model by Rodbell, Rodriguez and Ficalora [11] explains the resistance increase in thin films caused by void nucleation and growth due to electromigration. This model has been shown to represent the resistance versus time data of lengthy metallisation stripes [11]. This model is referred to as the RRF model in this thesis.

According to the RRF model, resistance increase due to electromigration in straight line structures is considered to be due to the creation and subsequent coalescence of voids. This is an important analysis of electromigration and it should be considered in some detail. So the details of this model are given first, followed by a discussion on its applicability to chequerboards.

RRF Model

Let,

N = nucleation rate of voids

G = growth rate of voids

τ = incubation time for nucleation

V = total volume of the system

V_{void} = total volume of voids

f_v = volume fraction of voids = V_{void}/V

t = time

Then, The equation governing $f_v(t)$ is shown to be given by:

$$\ln \frac{1}{1 - f_v} = \frac{4\pi G^3}{3} \int_0^t N(t - \tau)^3 \, d\tau \tag{5.3}$$

a general solution for f_v is [11]:

$$f_v = 1 - \exp[-(m\, t^n)] \tag{5.4}$$

where, m is proportional to G^3N and n is a constant.

The above formula in the RRF model is based on the model developed by Johnson, Mehl and Avrami [12,13] in connection with the nucleation and growth of solid-phase particle precipitation in a saturated solid-solution matrix. The nucleation and growth depends on the local super-saturation of the solute element before precipitation can occur. Precipitation generally begins at grain boundaries. In the case of electromigration a super-saturation of vacancies must occur before

a void nucleates. In this sense, vacancies are considered analogous to the precipitates. This analogy has been experimentally verified for the case of vacancy precipitation during diffusion in metallic systems [14]. In the general solution represented by equation 5.4 there are no restrictions on n but through experiments, certain values of n have been given definite physical significance and is discussed at the end of this section.

Resistance versus Time

At constant temperature,

$$R(t) = \rho L/A(t) \tag{5.5}$$

where, R(t) is the resistance as a function of time, ρ is the resistivity , L is the length and A(t) is the effective cross-sectional area as a function of time.

The volume fraction of voids f_v can be expressed as the area fraction (considering cylindrical voids) as:

$$f_v = \frac{A_{voids}}{A} \tag{5.6}$$

where,

$A_{voids} = \sum_{i=1}^{n}$cross-sectional area of voids
A = total cross-sectional area
i = number of voids per unit cross-section

Noting that,

$$A = A_{voids} + A(t) \tag{5.7}$$

From equations 5.6 and 5.7,

$$A(t) = A(1 - f_v) \tag{5.8}$$

Substituting for f_v from equation 5.4,

$$A(t) = A\,[\exp(-\,m\,t^n)] \tag{5.9}$$

From equations 5.9 and 5.5,

$$R(t) = \frac{\rho L}{A} \exp[m\,t^n] \tag{5.10}$$

or

$$R(t) = R_1 \exp[m\,t^n] \tag{5.11}$$

where, R_1 is the initial resistance.

Significance of m and n

It has been shown that

$$m \propto G^3 N$$

where G is the growth rate of voids and N is the nucleation rate of voids. In the case of electromigration, it is reasonable to assume that the activation energy can be calculated from the temperature dependence of m [11]. In a precipitation process the value of n distinguishes various mechanisms such as increasing, decreasing or constant nucleation rate (among others) with n varying from 1 to 4 [15]. The same significance of n can be applied to electromigration induced voids. For example; n=1 for an initial high void growth rate with void nucleation occurring at grain boundaries. This is further confirmed by the activation energy measurements by Rodbell et al[11] for aluminium and silver.

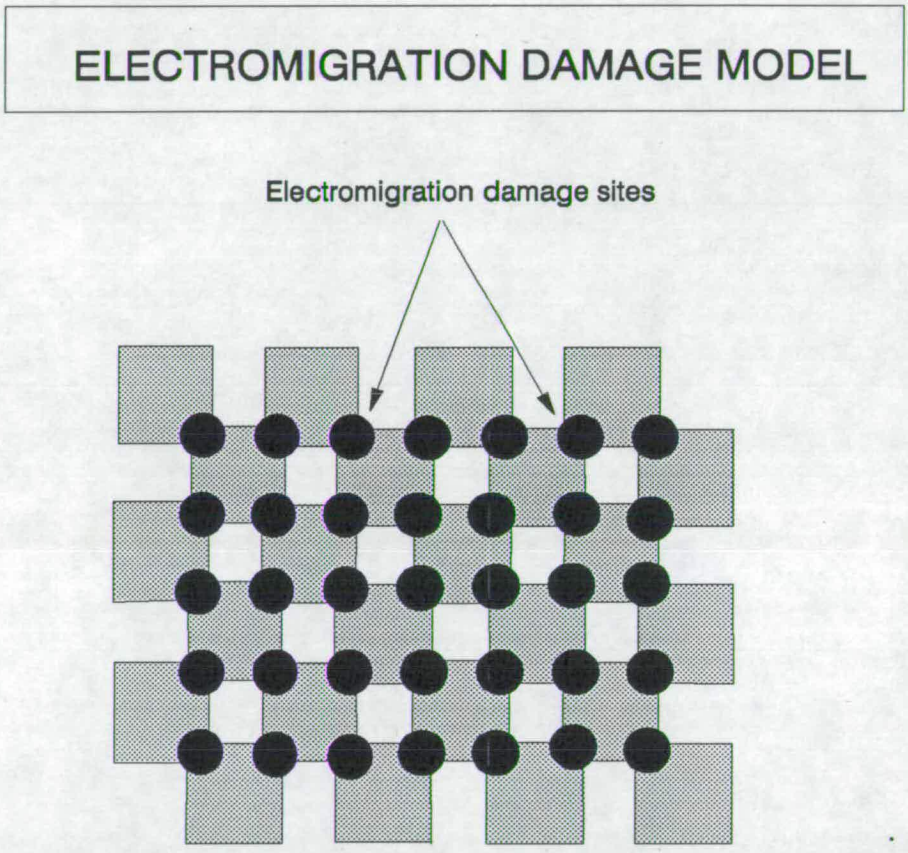


Figure 5–11: Electromigration damage model

5.6 RRF Model and Chequerboard Structures

In a chequerboard structure the void nucleation and growth sites are localised as shown schematically in Figure5–11. Hence it is reasonable to consider that A(t), the effective cross sectional area as a function of time, is proportional to the effective thinning rate of the overlap areas. However, it should be noted that now the parameters m and n characterize the void nucleation and growth processes occuring at the overlap regions. Equation 5.9 now describes the resistance increse of a chequerboard due to electromigration.

In order to estimate the MTF of a chequerboard in terms of the parameters m and n, the failure criteria have to be fixed. Failure is taken as the time taken for the resistance to increase by 10%. This is a reasonable approximation in view of the fact that in region III of the resistance versus time curve, the time differential between this point and the open circuit failure is negligibly small (refer to Figure 3-4). It should also be noted that the calculated failure time is an average time. This is because the resistance increase is due to the void volume summed over the entire chequerboard. For the case of grain-boundary nucleation (n=1), the above failure criteria yield,

$$\mathrm{m\,t} = \ln \mathrm{R/R_1} \tag{5.12}$$

since R/R_1 =1.1 when R increases by 10%. This gives,

$$\mathrm{MTF} = 0.09531/\mathrm{m} \tag{5.13}$$

For n=2 and 3, MTF is given by $0.30872/\sqrt{m}$ and $0.0.45678/m^{1/3}$ respectively.

5.6.1 Extraction of Parameters m and n

In principle, extraction of m and n should follow the following three steps:

1. Monitor resistance as a function of time.

2. Identify the constant temperature region.

3. Use function fitting software to extract m and n.

However, there are many experimental aspects to be given due attention. When high currents are used to cause Joule heating to reduce test times, we have to consider the temperature changes that occur over the lifetime of the sample as discussed previously. The model presupposes that the temperature is constant and hence the beginning and the end of region II of the resistance versus time (Figure 3-4) in which the temperature remains nearly constant should be determined experimentally by some means. Some trial experimentations may also be needed to determine thermal stabilization time. Using very high stress levels (currents and temperatures) may cause the breakdown to occur much before the typical stabilization time and thus produce erroneous results.

5.7 Chapter Conclusions

1. The success of chequerboards to assess linewidth control has been demonstrated in an earlier PhD project and they offer the possibility to produce micron/sub-micron dimensions close to and even below the typical minimum linewidth specifications. This capability has to be further confirmed by experiments and measurements when the linewidth approaches the resolution limits of the optical system. Chapter 6 describes how this is planned to be carried out.

2. The current density simulations show the higher current density in the overlap regions of a chequerboard, as expected.

3. Sample thermal calculations indicate that the large metal squares of a chequerboard may provide efficient heat conduction from the overlap regions. In this regard, it is necessary to monitor the resistance and temperature throughout the electromigration test period. The temperature monitoring methodology is discussed in chapter 6.

4. Preliminary measurements on chequerboards indicate that there are no integrity problems with these structures for electromigration experiments. TCR of metal films and the temperature rise caused by Joule heating can be obtained from the resistance measurements on chequerboards.

5. It has been proposed to use the RRF model to describe the electromigration damage in chequerboards. The validity of this model has to be established through experiments.

Bibliography

[1] Iona Binnie. *Critical dimension control: influencing factors and measurement.* PhD thesis, University of Edinburgh, 1991.

[2] A.F.Ward and J.T.M.Stevenson. Simple test reticle for rapid evaluation of VLSI photolithography processes. EMF report.

[3] Linda Strefford. NMOS test structures. Master's thesis, University of Edinburgh, 1989.

[4] PISCES-2B: Two-dimensional device analysis program. TMA modelling associates, Inc., CA.

[5] Harry A Schafft et al. Thermal conductivity measurements of thin-film silicon dioxide. *IEEE, International conference on Microelectronic Test Structures*, 2(1):121–125, 1989.

[6] Harry A Schafft and Tammy C.Grant. Electromigration and the current density dependence. *Reliability Physics, IEEE Annual Proceedings*, pages 93–99, 1985.

[7] M.Rosenberg and M.Ohring. Void formation and growth during electromigration in thin films. *J.Applied Physics*, 42(13):5671–5679, 1971.

[8] H.Suhl and P.A.Turner. Nucleation of voids and their growth during electromigration. *J.Applied Physics*, 44(11):4891–4895, 1973.

[9] J.R.Lloyd and R.H.Koch. Electromigration-induced vacancy behaviour in unpassivated thin films. Research note, Digital Equipment Corporation, MA, 1991.

[10] M.J.Attardo and R.Rosenberg. Electromigration damage in aluminium film conductors. *J.Applied Physics*, 41(6):2381–2386, 1970.

[11] K.P.Rodbell, M.V.Rodriguez, and P.J.Ficalora. The kinetics of electromigration. *J.Applied Physics*, 61(8):2844–2848, 1987.

[12] W.A.Johnson and R.F.Mehl. *Transactions of American Institute of Mining(Metall.)Engineers*, 135:416, 1939.

[13] M.Avrami. *J.Chem.Phys.*, 8:212, 1940.

[14] R.Resnick and L.Seigle. *J.Metals*, 1:87, 1957.

[15] J.W.Christian. *Theory of Transformations in Metals and Alloys.* Pergamon, Oxford, England, 1975.

Chapter 6

Chip Layout and Fabrication

6.1 Introduction

The main aim of this chapter is to give an overall view of the layout that was chosen for the test chip that formed the core experimental vehicle for this project. Several test structures with a range of dimensions were designed. They each had different objectives but all were produced by the same fabrication process. Some useful tips to generate chequerboard structures are given, along with a brief note about the mask design software. The purpose of the different types of test structures are discussed under the broad category of conventional test structures, chequerboard test structures and other test structures. Each structure in the chip belongs to one of these types and they are summarised in Tables 5-1 and 5-2 and are denoted by 'con.', 'cbd.' and 'other' respectively in these tables. Even though the main aim of the project was to use chequerboards as a process monitor, chequerboards are likely to be used for statistical modelling of the electromigration failure times. This is mainly because of the ease with which a large number of nominally identical electromigration damage sites can be incorporated in a single die and in a single structure. Keeping this in mind, chequerboards with a wide range of rows and columns were also included for further work. The structure by structure details of the number of rows and columns are also summarised in Tables 6-1 and 6-2.

There are invariably differences between the designed or target dimensions and actual dimension on the wafer depending upon the calibration methods and process control. Results comparing the target values and actual values obtained are also included in this chapter. The process run-sheet is given in Appendix A.

6.2 Chip Layout

6.2.1 Chip Design

The mask layout for the chequerboard chip consisted of two designs EU9101 and EU9102 and was done using the PRINCESS[1] CAD software system run on a VAX station 2000. EU9101 predominantly contains chequerboard structures while EU9102 contains in addition standard test structures recommended by the National Bureau of Standards (NBS) to be used with straight line metallisations [1]. Figure 6–1 shows how the two designs are placed on a 1cm×1cm chip. The actual chip plots are placed in the pocket attached to the inside back cover of this thesis.

All the structures are contained in 2x20 probe-pad arrays. Each pad is 120 μm × 120μm size and has a separation of 120 μm. This makes it suitable to probe test these structures with a standard probe card used for other routine structures in the EMF [2].

One notable feature of the the chequerboard chip design is the large number of squares and their arrangement in the form of an array. The layout task was eased by the graphics editor command ADD ARRAY to create an array of cells.

By defining a cell as shown in Figure 6–2 and using the following edit commands, chequerboards with required square size, overlap and rows × columns can be easily designed.

NUMBER_X—number of copies in X-direction
NUMBER_Y—number of copies in Y-direction
DELTA_X—column spacing
DELTA_Y—row spacing

---

[1]Trademark of Silvar-Lisco software systems

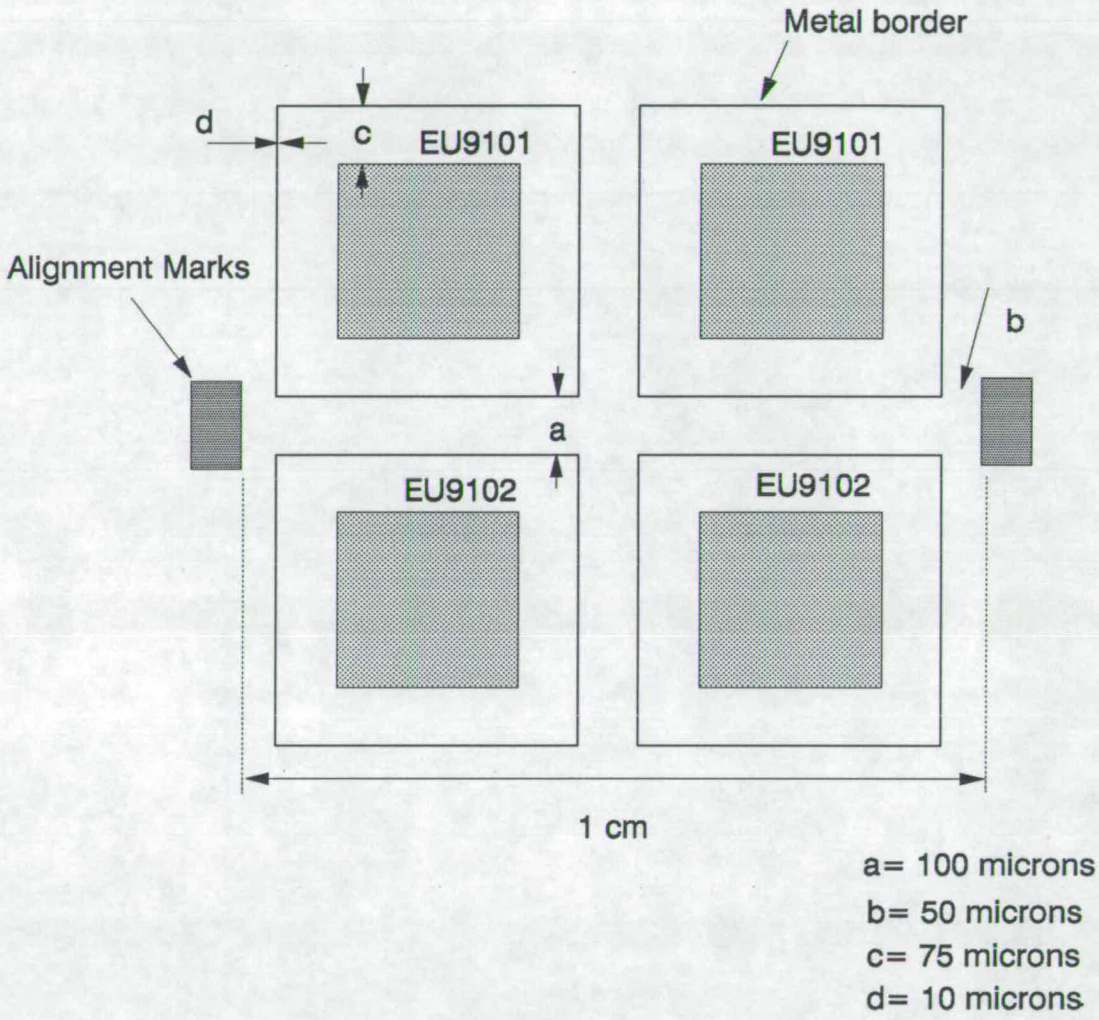


Figure 6–1: Geometric details of the chip

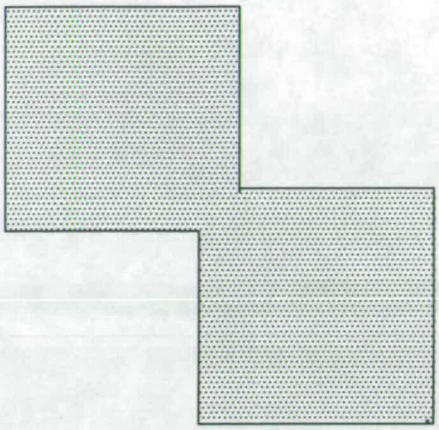


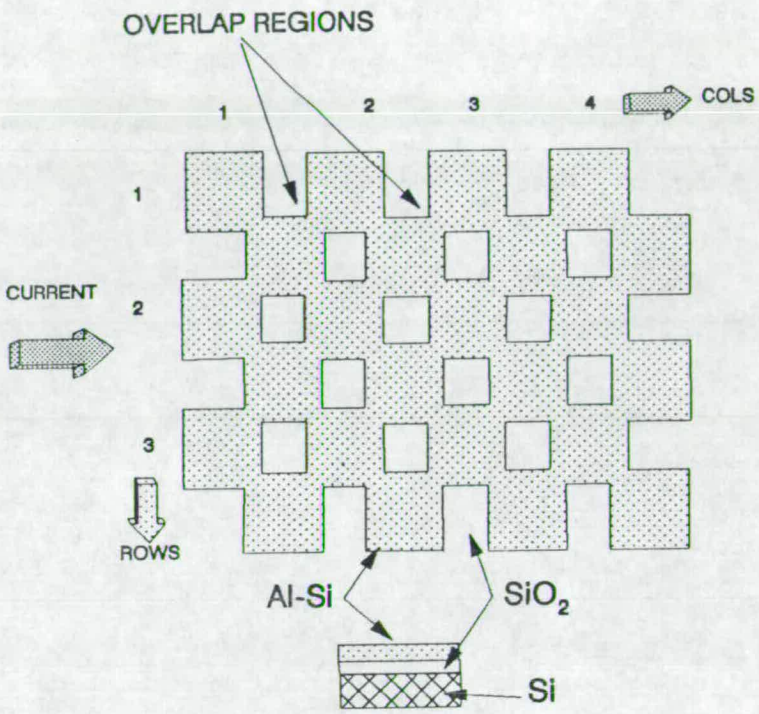
Figure 6–2: Cell used in the design of chequerboard arrays

Another problem of having such a large number of squares is that using an optical pattern generator for mask making is too slow and it is necessary to use an electron beam pattern generator to produce the mask. The graphic database file was sent to Rutherford Apleton Lab for conversion from HPGL to GDSII and finally to Compugraphics Company to get the electron beam mask.

6.2.2 Test Structure Types and Their Purpose

Conventional Test Structures

These structures are meant for classical electromigration tests (MTF tests) and are denoted by 'con.' in the tables 6-1 and 6-2. Typically the tracks are 800 μm or more in length. The structures NB1, NB2, NB3 and NB4 in EU9102 are based on the U.S.National Bureau of Standards test structure [1]. This structure has been shown in Figure 3-1 of chapter 3. The dimension details are summarised in Tables 5-1 and 5-2. Structures A1 to A6 in EU9101 are similar to the above test structures except for the fact that they do not exactly conform to the strict geometric details of the standard test structures but nevertheless can be generally used in all MTF measurements. All the structures in row H of chip EU9102 are also long conventional structures but have a number of bends. They were intended to be used for general studies such as the reduction in lifetime caused by bends.



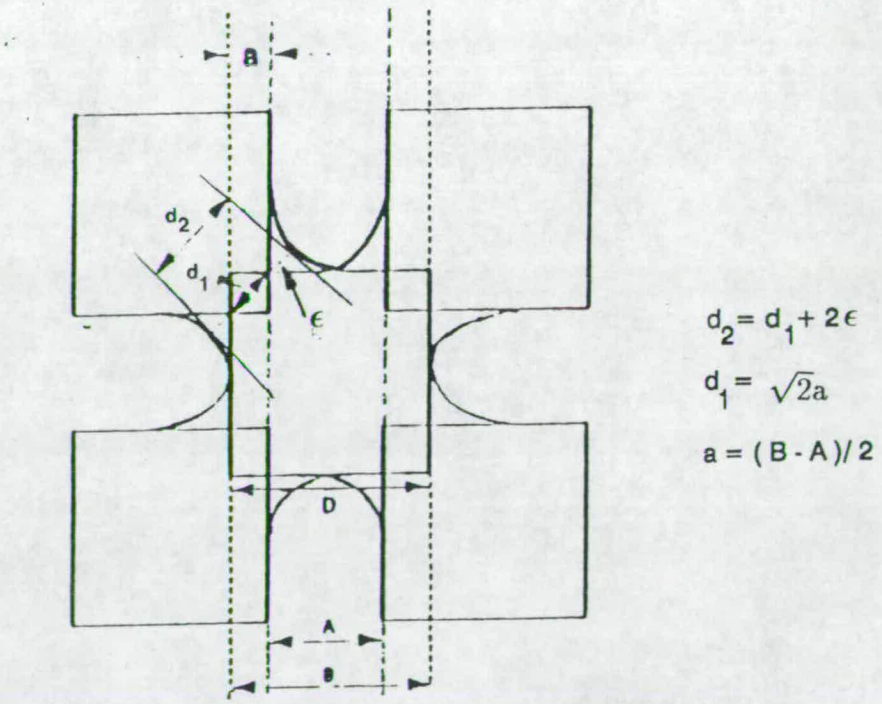


Figure 6–3: Symbols and terms used to define the chequerboard geometry

Structure	Location	Type	D(μm)	a(μm)	columns	rows	width(μm)
A1	row A	con.					10
A2	row A	con.					6
A3	row A	con.					4
A4	row A	con.					3
A5	row A	con.					2
A6	row A	con.					1
B1	row B	cbd.	2	0.2	100	1	
B2	row B	cbd.	2	0.4	100	1	
B3	row B	cbd.	2	0.6	100	1	
B4	row B	cbd.	2	0.8	100	1	
B5	row B	cbd.	4	0.2	100	1	
B6	row B	cbd.	4	0.6	100	1	
B7	row B	cbd.	4	1.0	100	1	
B8	row B	cbd.	4	1.4	100	1	
C1	row CI	cbd.	6	0.2	80	4	
C1S	row CI	cbd.	6	0.2	80	1	
C2	row CI	cbd.	6	0.6	80	4	
C2S	row CI	cbd.	6	0.6	80	1	
C3	row CI	cbd.	6	1	80	4	
C3S	row CI	cbd.	6	1	80	1	
C4	row CII	cbd.	6	0.2	80	8	
C5	row CII	cbd.	6	0.6	80	8	
C6	row CII	cbd.	6	1.0	80	8	
D1	row D	cbd.	2	0.2	300	4	
D2	row D	cbd.	2	0.4	300	4	
D3	row D	cbd.	2	0.6	300	4	

Table 6–1: Test structures in EU9101

Structure	Location	Type	D(μm)	a(μm)	columns	rows	width(μm)
D4	row D	cbd.	2	0.2	300	8	
D5	row D	cbd.	2	0.4	300	8	
D6	row D	cbd.	2	0.6	300	8	
E1	row E	cbd.	6	1-2	80	4	
E2	row E	cbd.	4	1-1.8	80	4	
F1	row F	cbd.	6	0.2-1.8	40	4	
F2	row F	cbd.	4	0.2-1.8	40	4	
G1	row G	cbd.	4	0.2	100	4	
G2	row G	cbd.	4	0.6	100	8	
G3U	row G	cbd.	4	1.0	100	4	
G3L	row G	cbd.	4	1.0	100	8	
G4U	row G	cbd.	4	1.4	100	8	
G4L	row G	cbd.	4	1.4	100	4	
H	row H	cbd.	4	-1.8 to +1.8	20	4	
I1	row I	cbd.	6	0	100	4	
I2	row I	cbd.	4	0	100	4	
I3	row I	cbd.	2	0	100	4	
I4	row I	cbd.	6	0	100	1	
I5	row I	cbd.	4	0	100	1	
I6	row I	cbd.	2	0	100	1	

Table 6–2: Test structures in EU9101(continued from the previous page)

Structure	Location	Type	Design details and remarks
A1,A2	row A	other	100 μm length segments in series
GC	row A	other	width=10 μm,length=200 μm(Van der Pauw)
NB4	row A	con.	width=6 μm, length=800 μm (NBS)
10U	row B	cbd.	D=10 μm,a=1 μm,rows=4
ST-3	row C	other	narrow region width=2 μm(SWEAT)
ST-4	row C	other	narrow region width=1 μm (SWEAT)
ST-1	row D	other	narrow region width=6 μm (SWEAT)
ST-2	row D	other	narrow region width=4 μm (SWEAT)
E1	row E	other	6 μm wide, 100 μm length segments
E2	row E	other	4 μm wide, 100 μm length segments
4U	row F	cbd.	D=4 μm,a=0.2 μm, > 1000 segments
2U	row F	cbd.	D=2 μm,a=0.2 μm, > 1000 segments
6U	row G	cbd.	D=6 μm,a=0.2 μm, > 1000 segments
H1 to H6	row H	other	lengthy lines with bends
NB1	row I	con.	width=10 μm, length=800 μm(NBS)
NB2	row I	con.	width=5 μm, length=800 μm(NBS)
NB3	row I	cbd.	width=2.5 μm, length=800 μm(NBS)
J1	row J	other	same as structure H in EU9101
J2	row J	cbd.	D=4 μm,a=0.2 μm,rows=8

Table 6–3: Test structures in EU9102

It may be recalled that the NBS test structures are based on an inter-laboratory electromigration experiment conducted by U.S. National Bureau of Standards using 3 μm width aluminium-silicon metallisation lines [1] to recommend methods to standardise MTF measurements. The important design consideration behind the NBS structures is the optimisation of the dimensions and placement of voltage taps so that the temperature profile of the lengthy line is not altered in a significant way.

Chequerboard Structures

These are denoted by 'cbd.' in the tables6–1 and 6-2. Basically two categories of chequerboard structures were designed, first one to be used for routine characterisation for electromigration and the second mainly intended for extracting critical width data. The design features of these are discussed below.

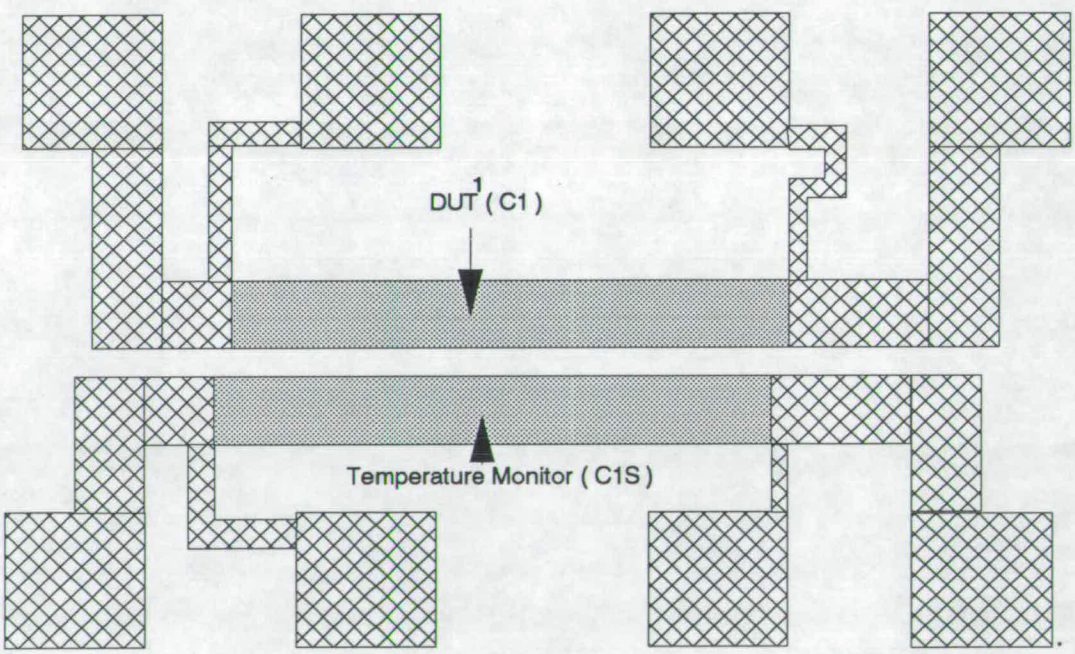


Figure 6–4: Structures C1 and C1S

Structures in rows CI and CII of EU9101 belong to the first category. One typical structure is shown in Figure 6–4. To extract electromigration parameters m and n from resistance versus time data it is essential to monitor the temperature

[1] Device Under Test

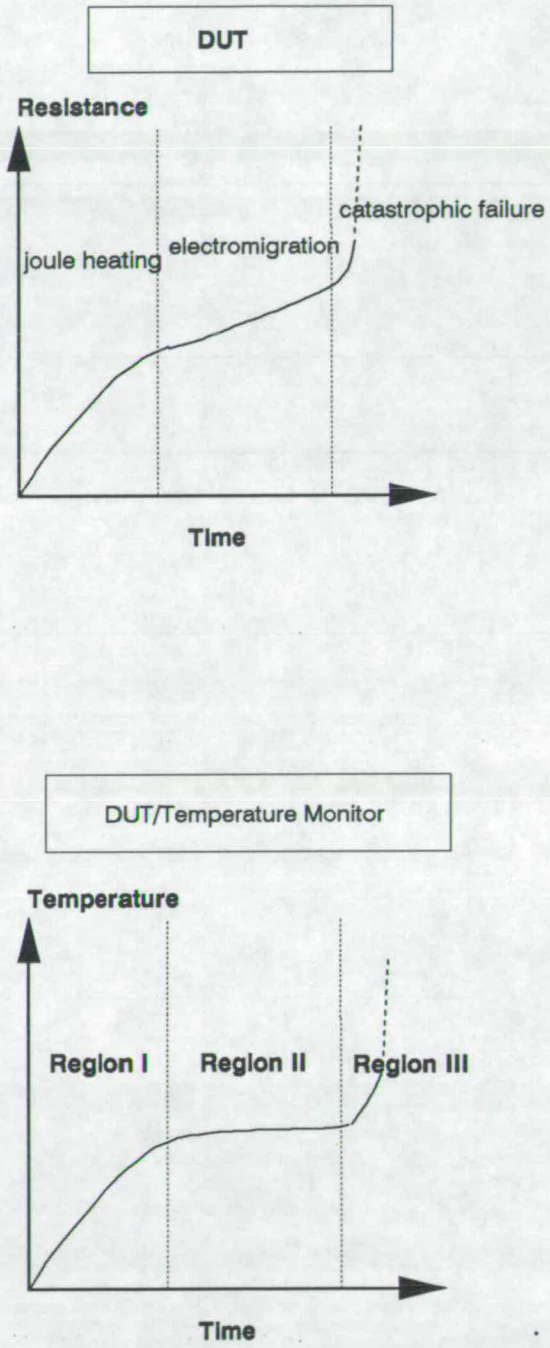


Figure 6–5: Temperature rise in the monitor

profile of the DUT. Adjacent chequerboard structure C1S is intended to be used for this purpose. The temperature of C1S is expected to closely follow that of the DUT. The temperature increase in DUT/C1S during electromigration experiments is expected to consists of three regions I, II, III as shown in the bottom Figure 6–5.

These three regions correspond to the three failure/physical processes taking place in the DUT during electromigration experiments shown in the top [2] Figure 6–5. That is, region I → joule heating, region II → electromigration, region III → catastrophic failure processes.

It may be noted that the temperature of C1S is measured by monitoring its resistance and using its temperature coefficient of resistance to estimate the temperature. Hence low current which does not cause significant joule heating and electromigration should be used for C1S.

Structures E1, E2, F1, F2, of EU9101 belong to the second category. An outline diagram of the structure F1 is shown in Figure 6–6. Structure E1 is same as that of F1 but has an overlap width increasing from 1.0 μm to 2.0 μm in step of 0.2 μm. Structures E2 and F2 are for the smaller square size of 4 μm. In these structures, chequerboards with increasing overlap width are all connected in series to enable the resistance versus time characteristics of all series-connected chequerboards to be monitored simultaneously. In reality the voltage tap outputs of these chequerboards are not measured in parallel but through a multiplexing scheme. However, the time interval between any two successive measurements is typically 30 second which is large compared to the multiplexing time of interval of 100 milliseconds.

These structures are intended to be used for critical width determination because the electromigration parameters m and n can be measured for the range of widths at once. These structures are intended to be tested using low currents which do not cause significant temperature rise (i.e., less than about 2°C). Ex-

---

[2] reproduced from Figure 3-4

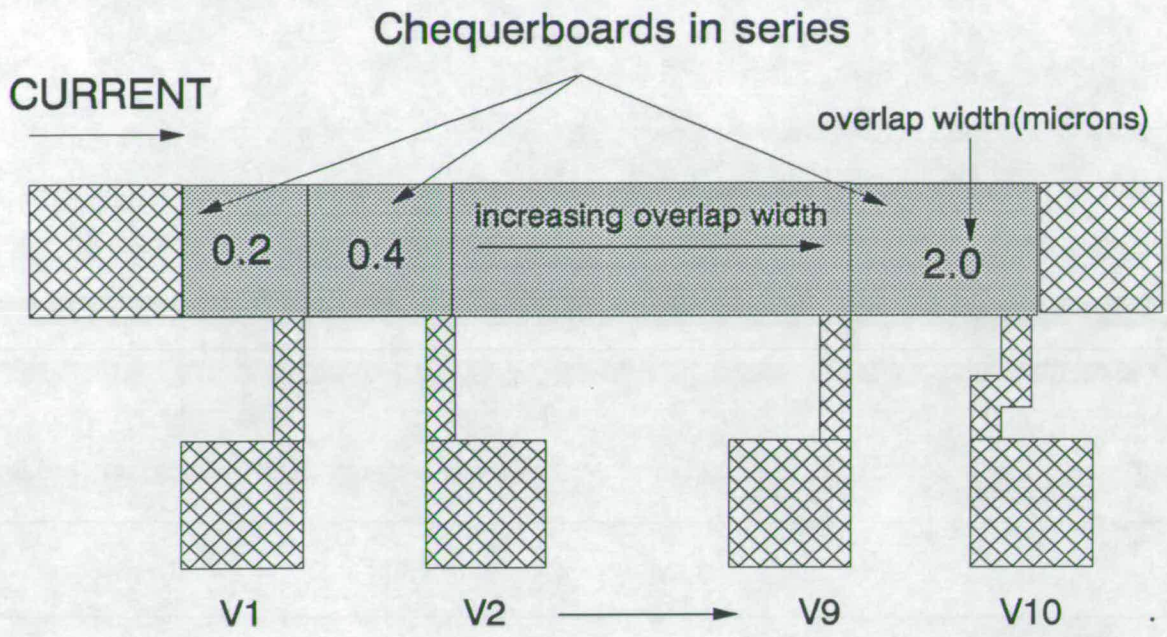


Figure 6–6: Serially connected chequerboards

ternal heat source either a hot chuck for wafer level tests or an oven for packaged devices is necessary to shorten test times.

Other Structures

Many other structures are included on the chip because of their general importance. For example, SWEAT structures, chequerboard structures for etch monitoring etc. The dimensional details and location of these structures on the chip are summarised in Tables 6-1 and 6-2. These structures are denoted by 'other' in tables 5-1 and 5-2. SWEAT structures were included because of their importance in electromigration (discussed in chapter 3) evaluation while the other structures are included from their general importance in metallisation process monitoring. Rapid visual monitoring of under/over etch may be done using structure J1 of EU9102.

6.3 Fabrication

6.3.1 Starting Material

The starting material is 3 inch diameter p-type silicon wafer of resistivity 14-20 ohm-cm and having (100) crystallographic orientation.

6.3.2 Oxidation

The process details of the oxidation process are given in step II of the process run-sheet in Appendix A.

6.3.3 Aluminium Sputtering

All the oxidised wafers were coated with aluminium- 1% silicon using a Balzers sputterer. Target thickness was around 0.6 μm. Process details are given in step III of the process run-sheet.

6.3.4 Photolithography

All the wafers except numbers 5 and 10 went through the normal exposure/development process (steps IV and V of the process run-sheet). Wafers 5 and 10 were subjected to an exposure matrix, that is, exposure time was increased in steps of 20 ms from one die to the next, starting at 600 ms and ending at 1340 ms for the final die as shown in figure 6–7. Higher exposure time has the same result as overetching and this is useful to extend the segment widths into the deep sub-micron region.

It may be noted that for routine electromigration characterisation it is sufficient usually to evaluate for the minimum linewidth for a given technology and use the normal exposure to realise this linewidth. Hence in general it may not be necessary to process the wafers using the exposure matrix for routine process monitoring.

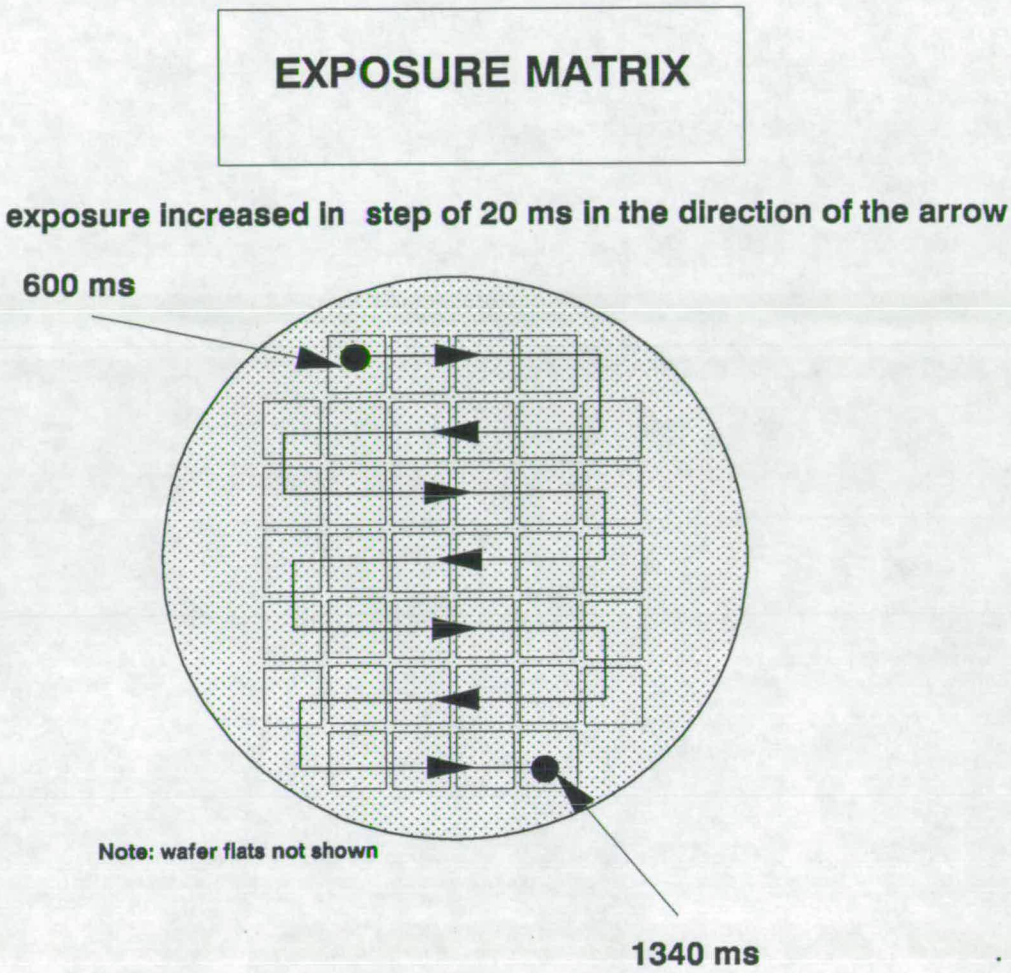


Figure 6–7: Exposure time variations across the wafers 5 and 10

6.3.5 Reactive Ion Etching (RIE) and Anneal

The standard RIE process of the EMF was used to etch the metal. The samples were annealed for 5 minutes nitrogen, 10 minutes in nitrogen/hydrogen and 5 minute in nitrogen at 435°C. The process details are given in the process run-sheet.

6.4 Dimensional Measurements

6.4.1 Pattern Dimension Measurements on the Mask

The electron beam mask was visually examined under an optical microscope for any visual defects. Pattern dimensions were measured using a Vickers shearing microscope. The visual examination did not show any defects such as pinholes, scratches etc . However, there was an offset of 0.2 μm between the designed dimension and the pattern dimension on the mask. This is evident from Figure 6–8.

6.4.2 Oxide Thickness

The target thickness was 500 Å. The thickness measurements were carried out using ellipsometer. Figure 6–9 is a two dimensional contour map showing the thickness variations across the oxide film. Excellent uniformity of the oxide thickness is quite evident from the figure.

6.4.3 Pattern Dimension Measurements on the Wafer

Linewidth measurements

Linewidth measurements were carried out using a Cambridge S100 scanning electron microscope. The results of measurements on 10, 6, 4, and 1 μm lines within a central die in wafer 6 are shown in Figure 6–10

Chequerboard structures

From electromigration point of view the important dimensions in a chequerboard are d_2 , d_1 , a and ϵ. These symbols are described in Figure 6–3. d_2 was measured by placing the SEM cursors as shown in Figure 6–3. d_1 was measured

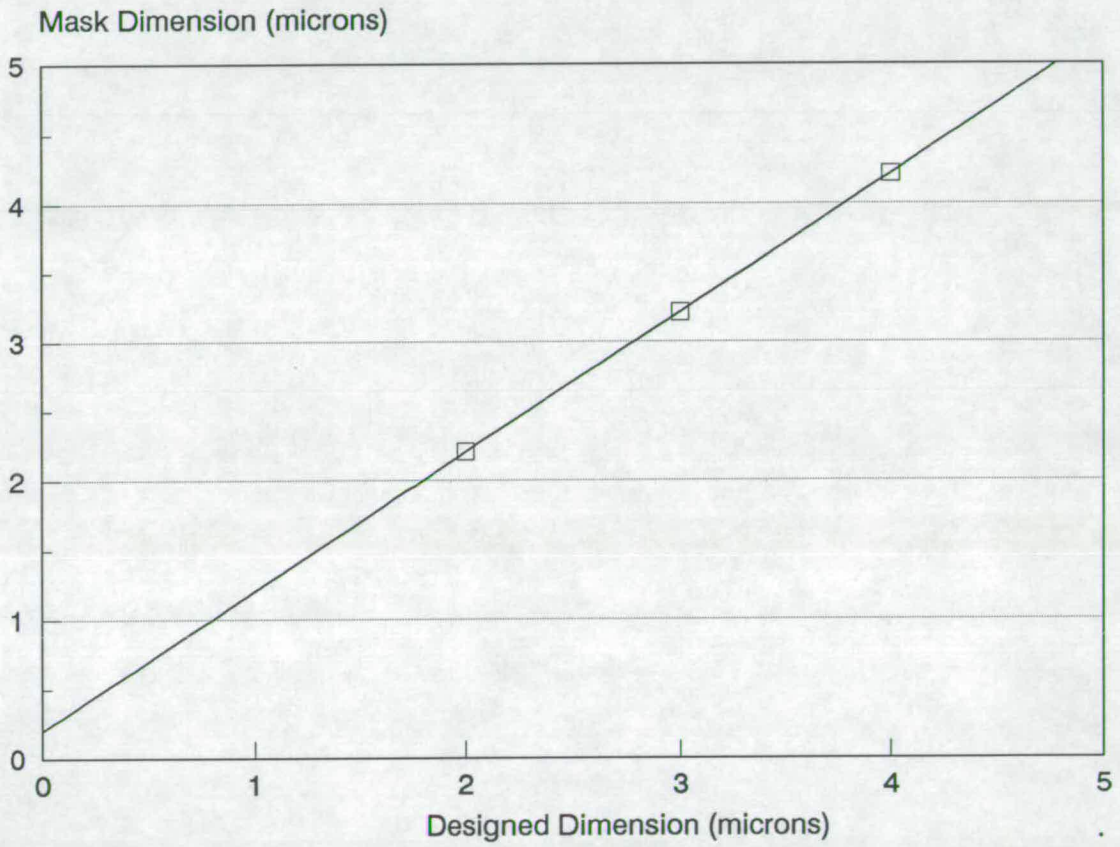


Figure 6–8: Pattern dimension measurements on the mask

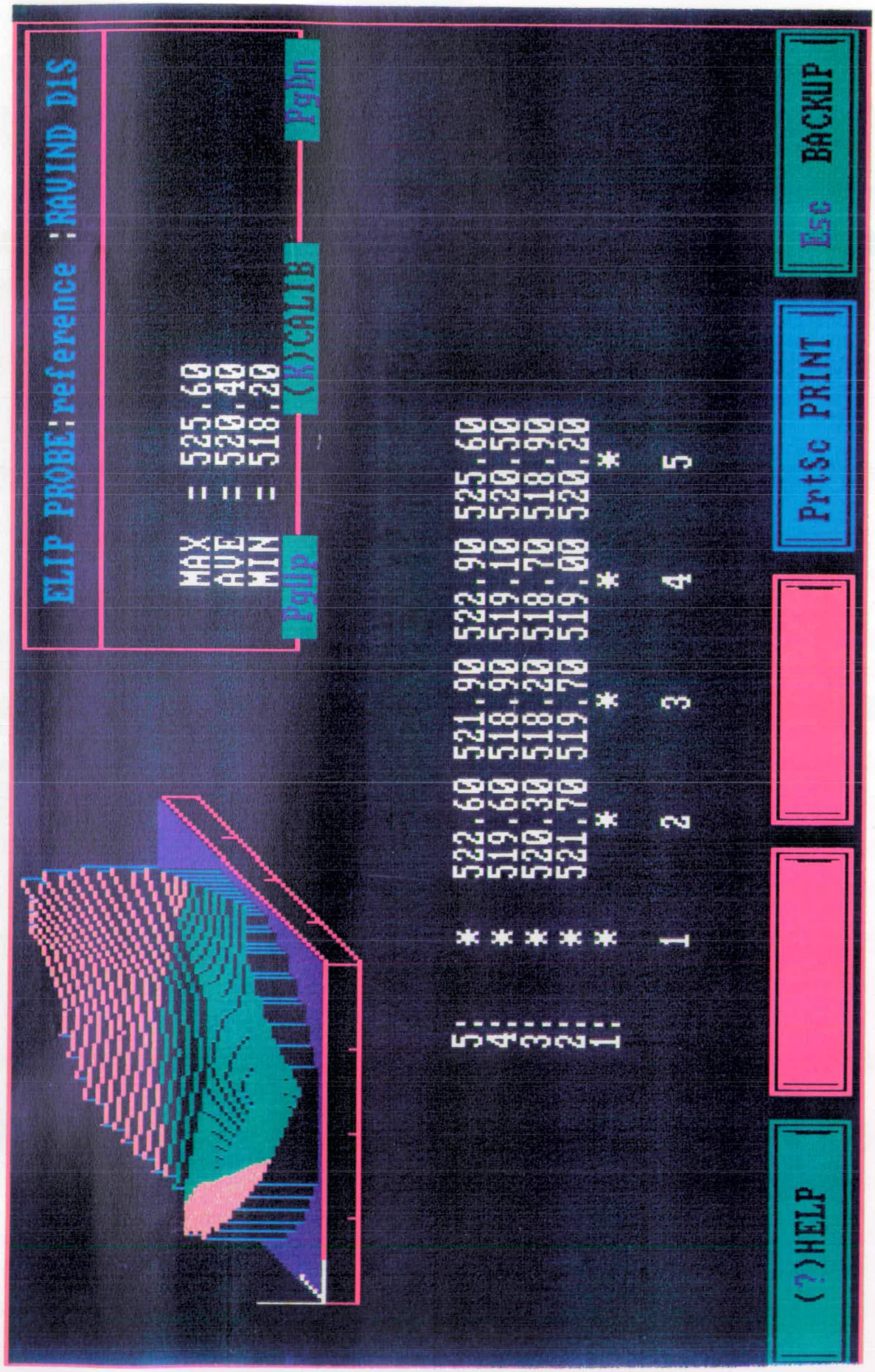


Figure 6–9: Scanning Ellispometer 2-D Wafer Map

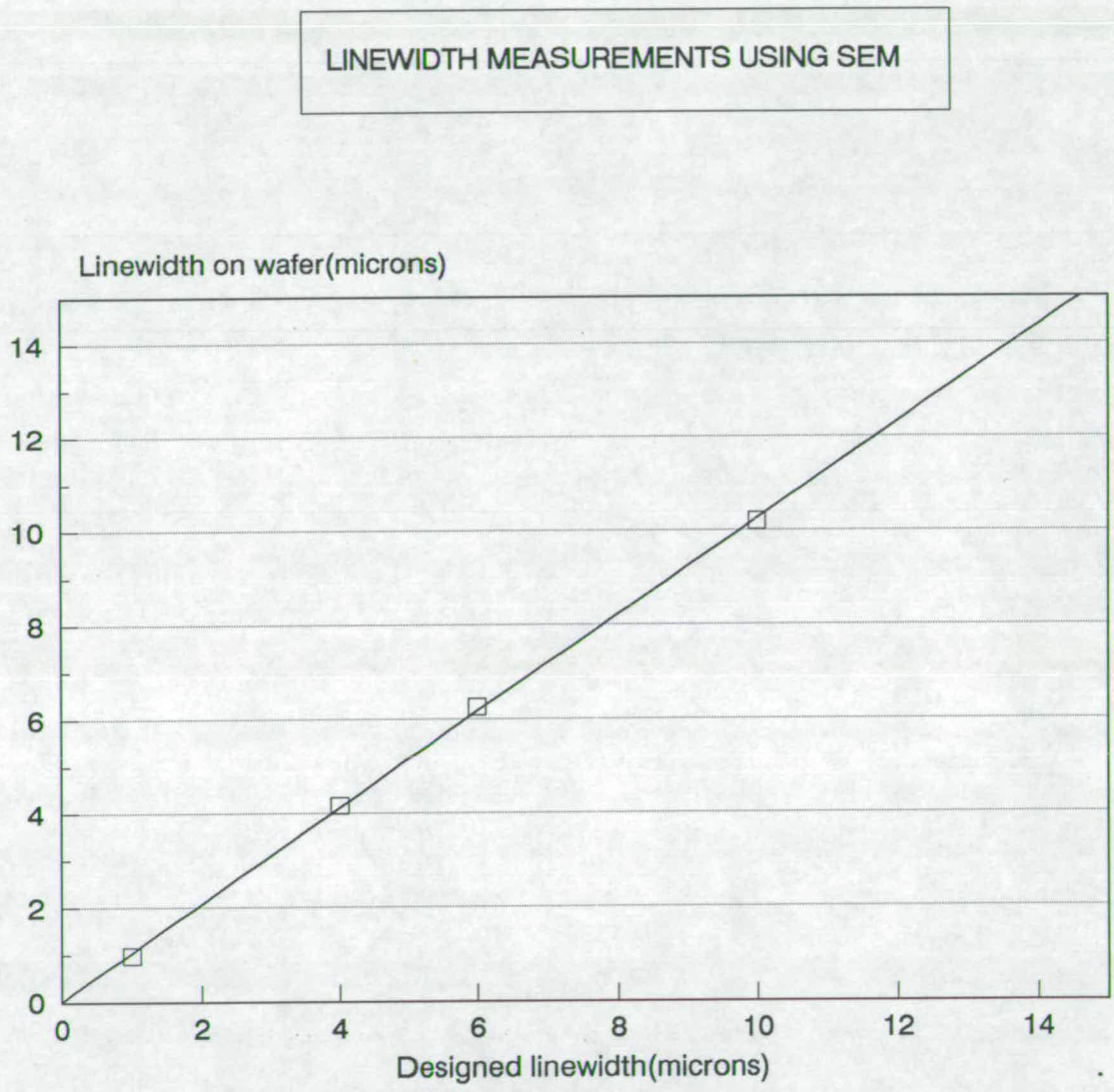
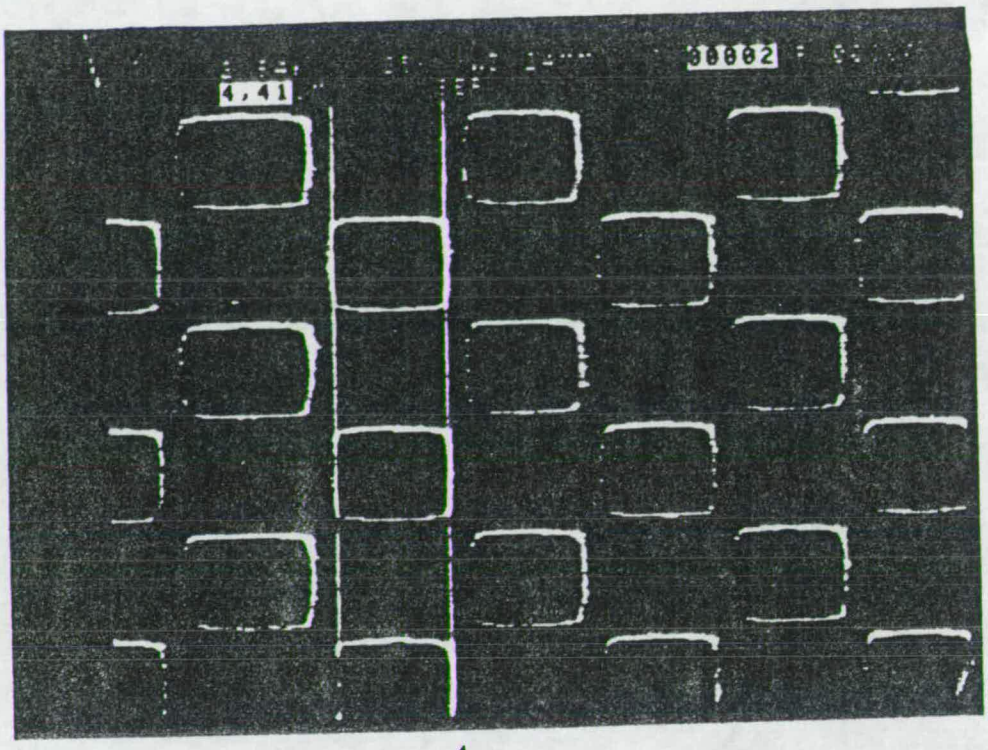
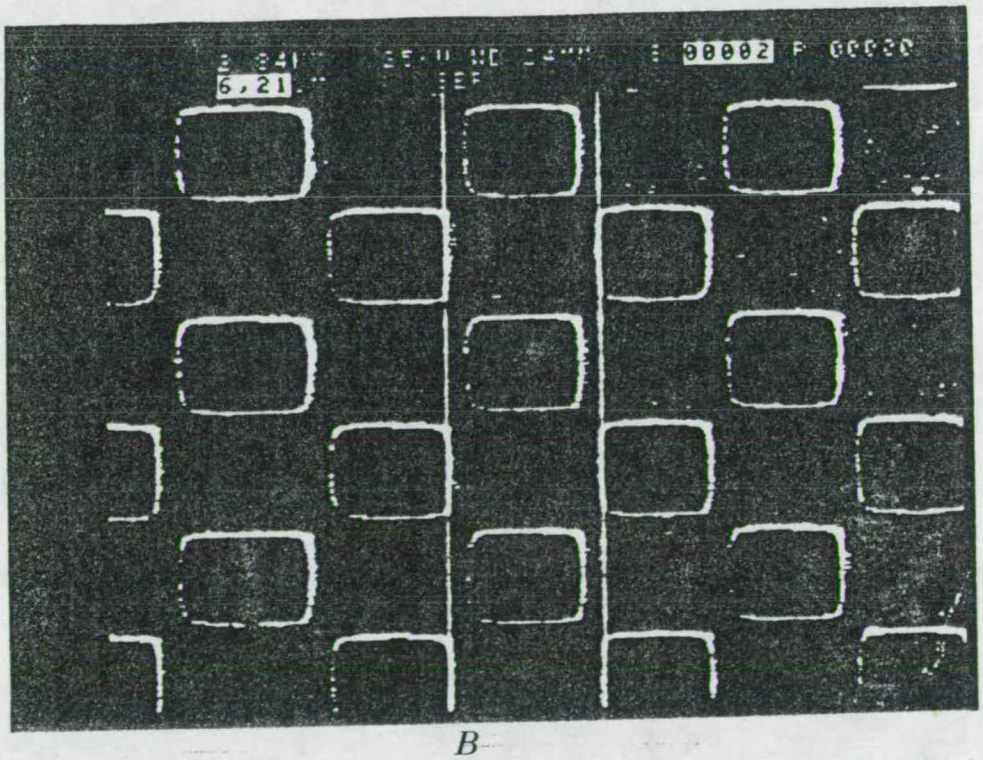


Figure 6–10: Linewidth measurements using SEM



A



B

Figure 6–11: SEM micrographs showing the dimensions A(Top) and B(Bottom) on a chequerboard

by measuring A and B and noting that $d_1 = \sqrt{2}a$ where $a = \frac{B-A}{2}$.

SEM micrographs showing the measurement of the dimensions A and B are given in Figure 6–11. From these micrographs we can calculate the overlap(a) as follows:

$A = 4.41\ \mu m$

$B = 6.21\ \mu m$

Therefore,

$a = \frac{B-A}{2} = 0.4\ \mu m.$

ϵ is the additional component due to the 'rounding off' at the corners. It depends on the modulation transfer function and the resolution of the lens (ϵ_{optics}) and also on the over/under etching caused by exposure/develop/etch processes ($\epsilon_{process}$). It may be represented as:

$$\epsilon = \epsilon_{optics} \pm \epsilon_{process} \tag{6.1}$$

also,

$$d_2 = d_1 + 2\epsilon \tag{6.2}$$

If we plot $(d_2 - d_1)$ versus d_1 for the segments within a die, the above equations indicate that we should get a line nearly parallel to the d_1 axis because the segment-to-segment variations in ϵ_{optics} and $\epsilon_{process}$ within a die can be considered to be negligible. In other words ϵ is expected to be nearly constant within a die. Hence it was expected that as overlap (a) is increased in steps of 0.2 μm in the serial chequerboard structures, d_2 and d_1 would increase, but $(d_2 - d_1)$ will be very nearly constant. Constancy of ϵ would also enable us to obtain the value of d_2 for all the overlap widths in a serial chequerboard quite easily. This simplifies the measurements, especially when we note the fact that measurements of hundreds of segments using SEM is quite tedious.

The main intentions of these measurements can be summarised as:

- To verify the expected normal distribution of segment widths in a chequerboard structure.

- To verify the constancy of ϵ within a die.

A sample histogram is given in Figure 6–12. The segment width distribution shown in the histogram was normalised using the method described in Appendix C and the result is shown in Figure 6–13, the resulting linear plots in all the cases gave further proof that the distributions were indeed normal. The average and standard deviation values obtained in each case are summarised in Table 5-3. Constancy of ϵ is evident from Figure 6–14

Segment label	Number of observations	overlap(a) (microns)	Mean d_2 (microns)	σ of d_2 (microns)	Mean d_1 (microns)	$(d_2 - d_1)$ (microns)
A	112	0.3	1.11	0.041	0.43	0.68
B	101	0.51	1.41	0.038	0.72	0.69
C	101	0.73	1.71	0.039	1.04	0.67
D	75	0.95	2.03	0.034	1.34	0.69

Table 6–4: Summary of the chequerboard segment width measurements

6.4.4 Metallisation Thickness

The thickness across the wafer was measured using a Dektak surface profiler. The measurements were repeated at many locations within a die and an average value was obtained for each die. Finally these measurements were repeated across the wafer and typical results are shown in Figure 6–15. The variations in metallisation thickness shown in Figure 6–15 are quite typical of any well maintained IC fabrication facility.

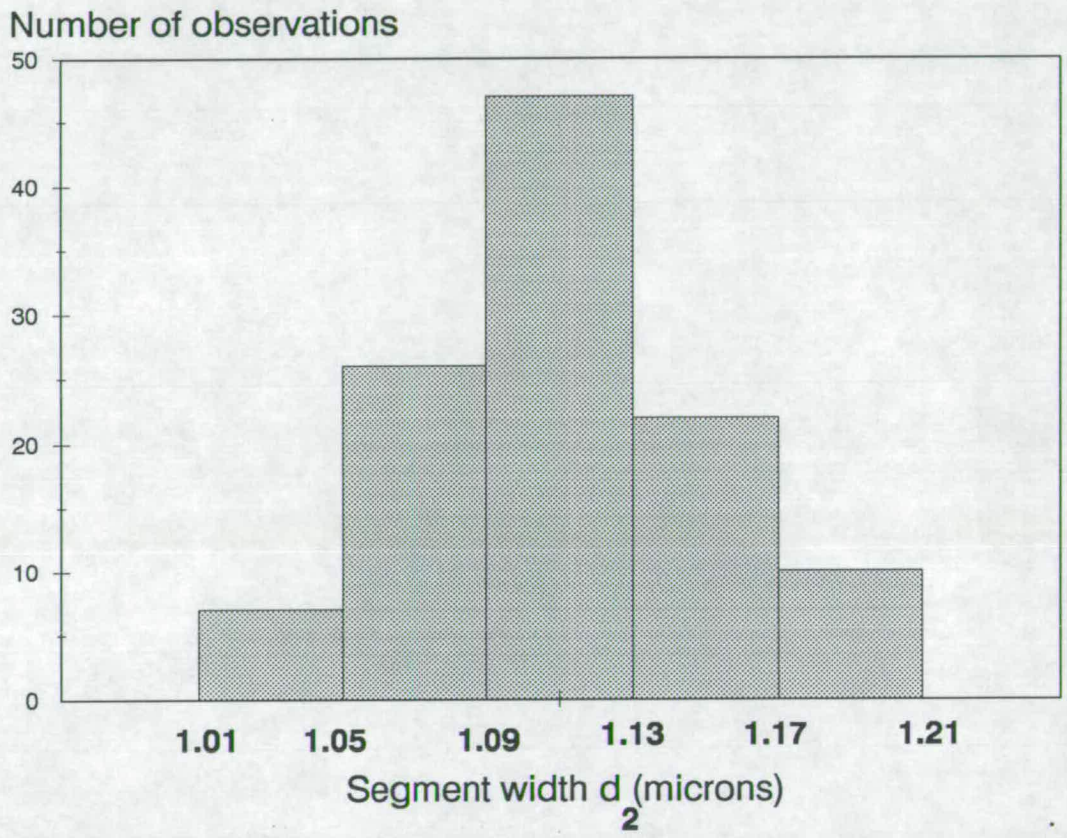


Figure 6–12: Segment width distribution

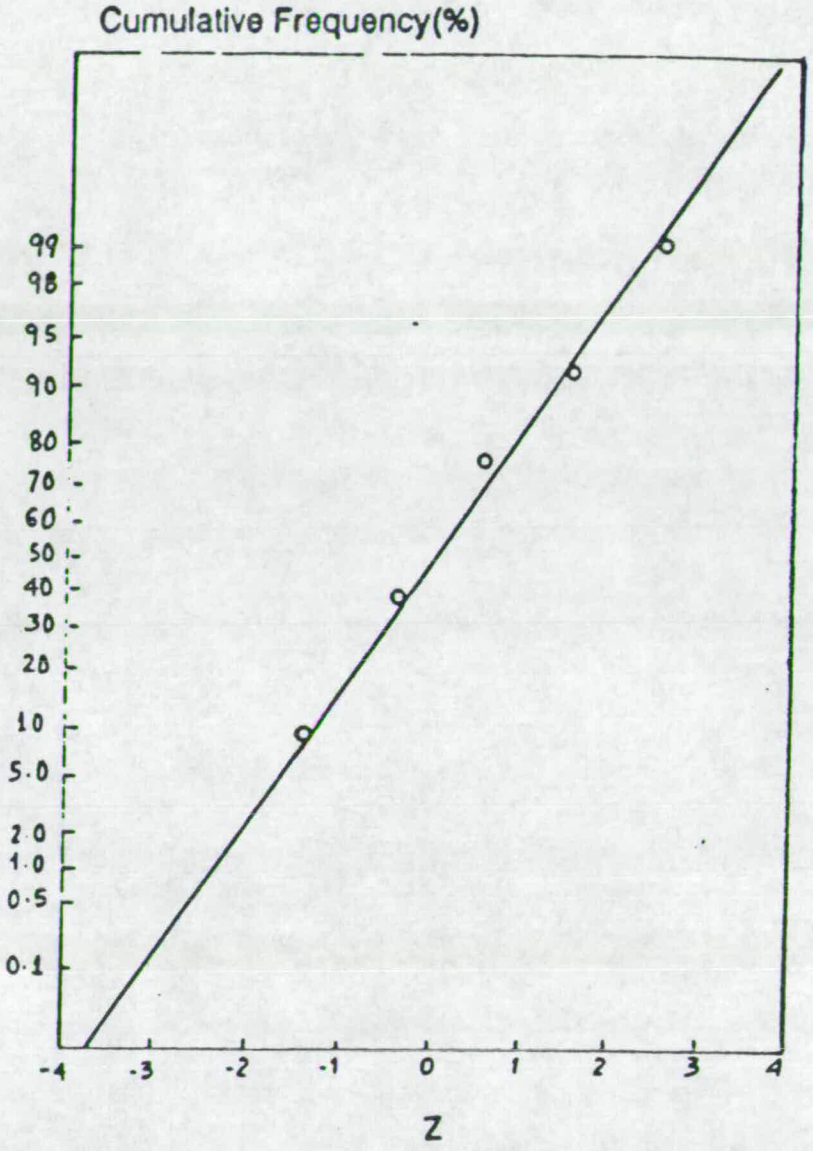


Figure 6–13: Linear plot of cumulative distribution function on normal probability paper

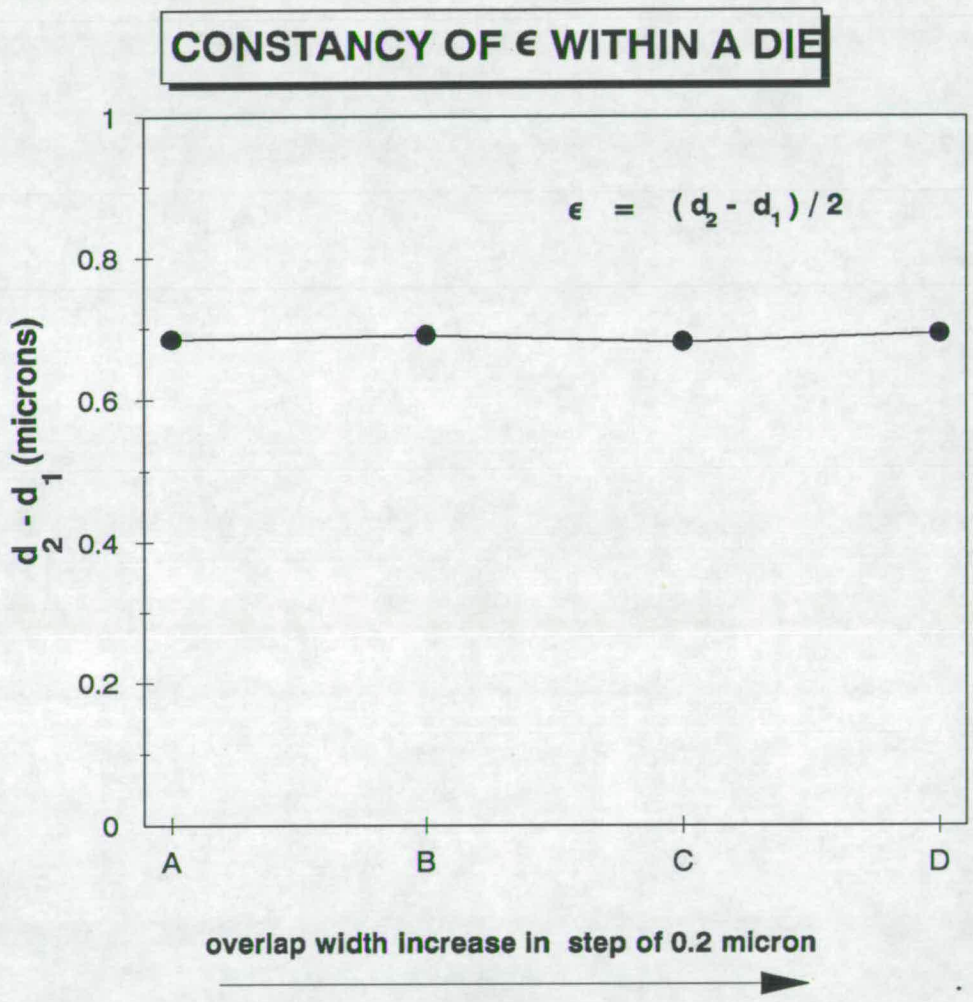


Figure 6–14: Constancy of ϵ within a die

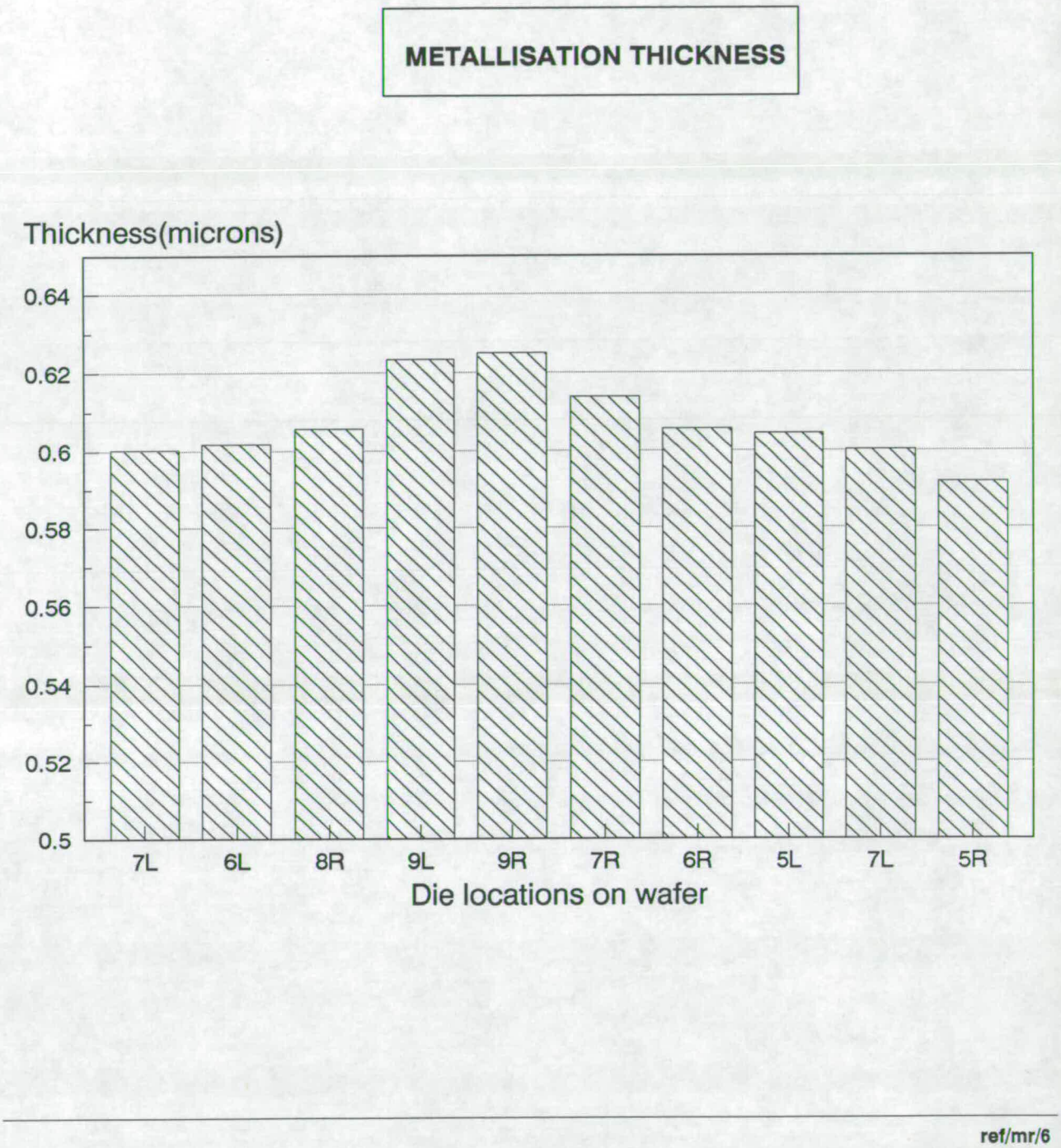


Figure 6–15: thickness measurements across wafer 6

Bibliography

[1] Harry A. Schafft et al. Reproducibility of electromigration measurements. *IEEE Transactions on Elecron Devices*, ED-34(3) :673–681, 1987.

[2] W.R.Gammie. The 5 micron EMF test strip. Technical report, Edinburgh Microfabrication Facility, 1987.

Chapter 7

Electromigration Measurements and Test Results

7.1 Introduction

In this chapter all the electromigration and related measurements carried out using chequerboard structures are given and the results are analysed within the overall context of this PhD project aims.

The measurements include:

1. General measurements such as resistance, temperature coefficient of resistance (TCR) etc.

2. Thermal measurements.

3. Monitoring for spikes in resistance-time curves.

4. Resistometry measurements.

5. Fast tests.

As the resistometry technique was intended to be used extensively, it was considered appropriate to measure the resistance of chequerboard structures and the die-to-die variations across a wafer. The chip contains various geometry structures and resistances of nearly all the structures in one die were measured to test the integrity of these structures and to verify some of the general expectations. For

example, resistance of structure C1 is expected to be higher than that of C2 because of the smaller overlap width(a) of C1. It may be recalled that C1 and C2 are chequerboard structures meant for resistometry experiments and the dimension details are given in Table 6-1. Die-to-die variations of resistance of a number of structures were also measured. However, the results of chequerboard structure 10U are typical and hence are shown as a reference in Figure 7–3. Besides, this structure covers the largest area of the die and hence is expected to yield a better process average. TCR measurements are important in estimating the temperature rise in the metallisation due to Joule heating. Thermal measurements include measurements such as thermal stabilization time and the significance of this is discussed in section 7.3.3.

The resistometry technique can be applied only if there are no spikes in resistance versus time curves. This was verified by stress testing a chequerboard structure for long test times (tens of hours) and monitoring the resistance for spikes. The test results are given in section 7.4.

The resistometry details have been discussed in chapter 3. Both options, namely, resistometry with self-heating and resistometry with external heating were carried out and the test results are given in section 7.5. The measurements were carried out using a microcomputer and the instrumentation details are also provided in this section, but the program listing is given in Appendix B.

Some fast tests were carried out to check whether very rapid monitoring of electromigration can be carried out using the chequerboard structures and the results are given in section 7.6.

Finally, in section 7.7 the results are analysed. Activation energy is one of the important parameters of general interest and hence it is extracted from resistometry measurements and the results are given in section 7.7.2. It may be recalled that the main aim of the project was to use chequerboard as a process monitor structure. Hence, one of the process parameters, namely, average linewidth is considered and the results are analysed to check the sensitivity of the methodology for this parameter. Specifically, the interest was to determine the critical width. The results are given in section 7.7.3. It may be recalled that an additional objec-

tive of the project was to estimate the MTF of a single segment from an array of chequerboard segments and the proposed method is described in section 7.7.4.

7.2 Instrumentation

A block diagram of the measurement system is shown in Figure 7–1. A notable feature of the instrumentation is the measurement of voltages at various bond pads of the chequerboard structure in a multiplexed way using the HP 3495A multichannel scanner. It consists of 2 'Duo-decade- options' [1] each of which is a 20-to-1 multiplexer allowing 20 signals to be monitored by one measurement system. This is schematically shown in Figure 7–2. The various instruments such as power supply sources, DMM etc. and their HP-IB address schemes are provided in the HP BASIC program listing in Appendix B. The resistance values are obtained from the scanned voltage data.

7.3 Measurements

7.3.1 Resistance Measurements

The resistance of various chequerboard structures summarised in Table 6-1 and Table 6-2 of chapter 6 were measured to verify the integrity of these structures and the values are tabulated in Table 7–1. All the structures listed in this table belong to the same die. These measurements indicated that in general the resistance values of the chequerboard structures were as expected.

For example,

$$R_{B1} > R_{B2} > R_{B3} > R_{B4}$$

$$R_{B5} > R_{B6} > R_{B7} > R_{B8}$$

$$R_{C1} > R_{C2} > R_{C3}$$

$$R_{C4} > R_{C5} > R_{C6}$$

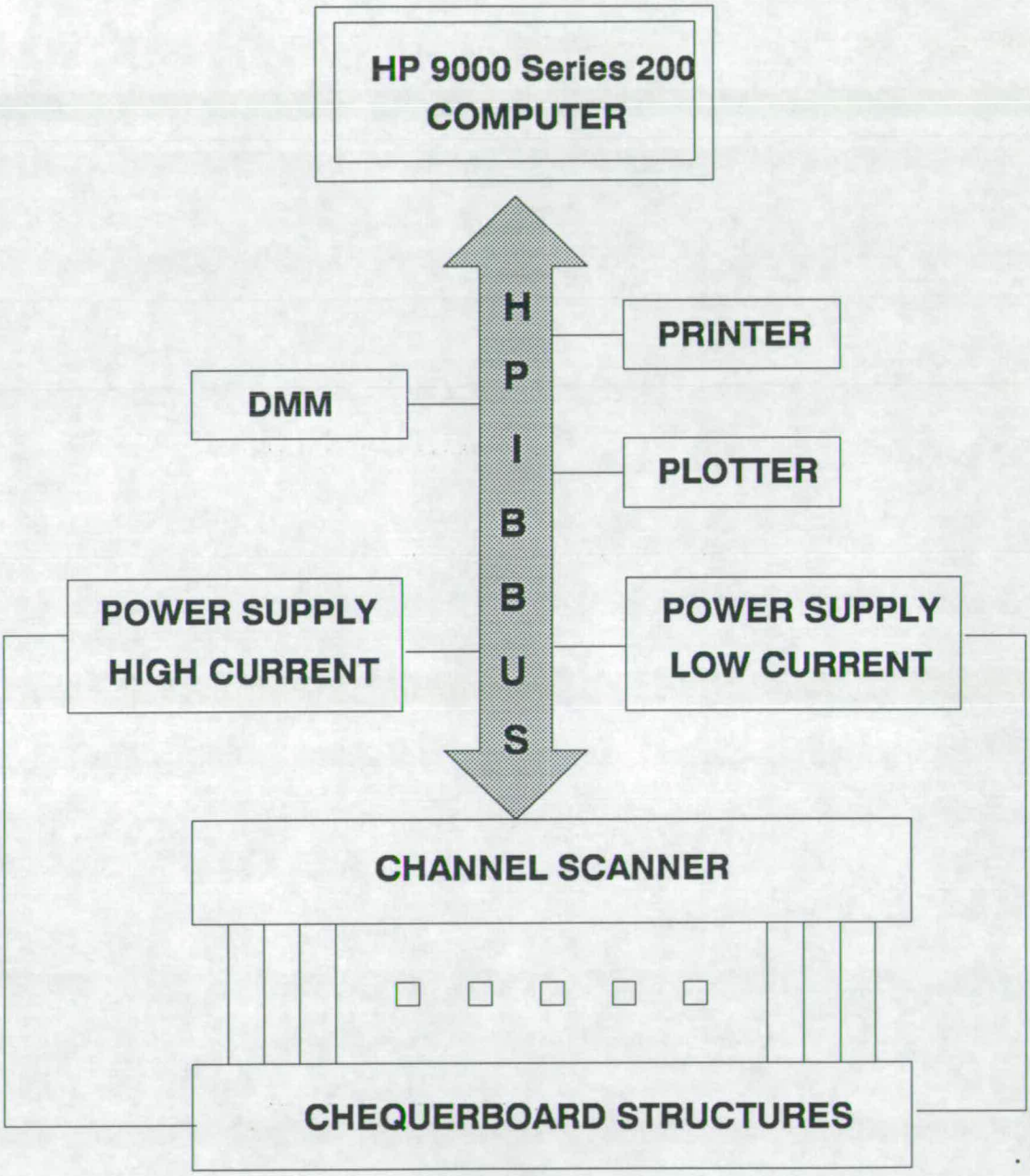


Figure 7–1: Block diagram of the measurement system

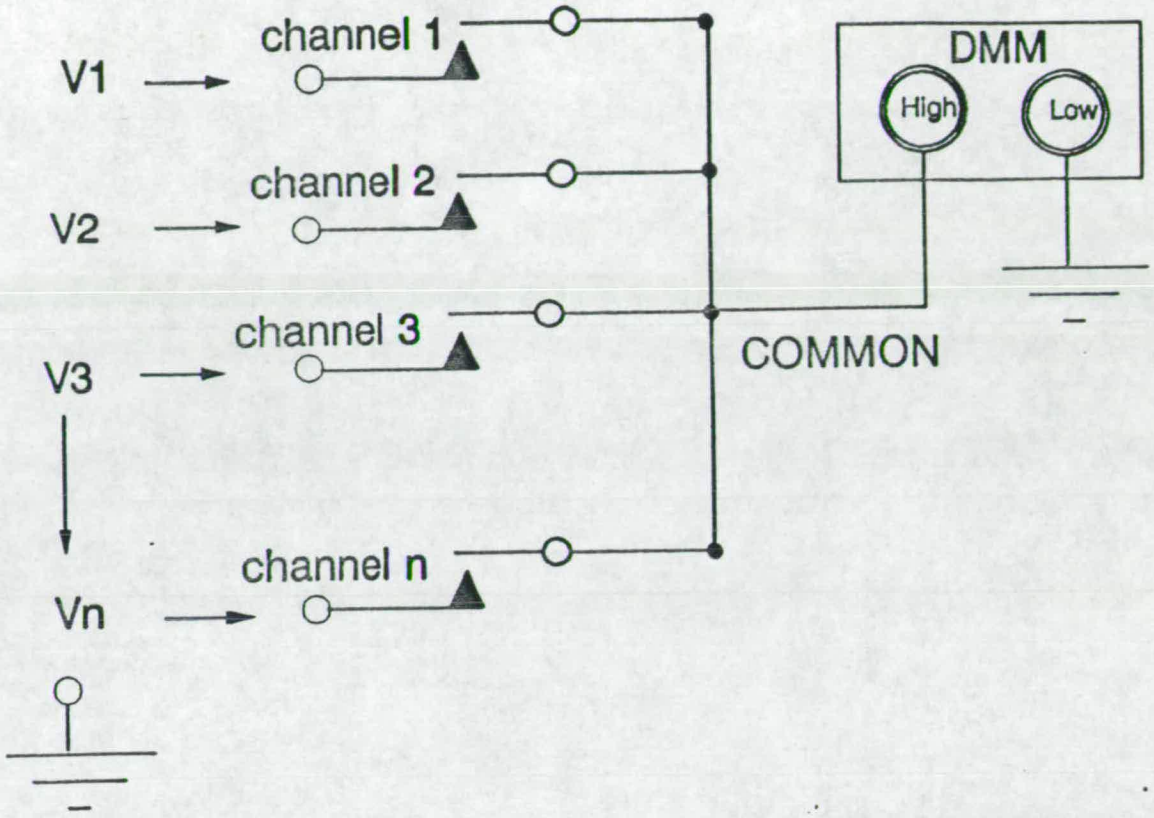


Figure 7–2: A schematic representation of the multichannel scanner

where, R_X stands for resistance of structure X.

Variation in metallisation cross sectional area (width × thickness) over the wafer due to process variations such as etch, exposure, etc. means one can expect die-to-die variations in resistance for any given chequerboard structure. One typical result showing the resistance variations across wafer 6 using structure 10U is given in Figure 7–3. The spread in resistance of $\pm$ 10 to 15 %[1] from the average value was quite typical and considering the typical linewidth variations ($\pm$10%) and thickness variations ($\pm$ 3%) over a wafer, is quite reasonable. We can notice the higher values of the resistance in die at the edge of the wafer than those at the centre and these variations were quite typical for any wafer.

[1] edge values are rejected

Structure	Resistance(ohms)	Structure	Resistance(ohms)
A1	9.33	C6	2.27
A2	13.66	D1	19.5
A3	22.4	D2	13.8
A4	32.5	D3	8.74
A5	54.7	D4	9.26
B1	38.6	D5	6.56
B2	28.0	D6	3.96
B3	20.9	E1	17.63
B4	9.1	E2	18.7
B5	63.1	F1	23.0
B6	40.1	F2	16.6
B7	29.5	G1	8.67
B8	19.6	G2	5.99
C1	7.4	G3L	1.97
C1S	48.0	G4U	3.01
C2	5.7	G4L	1.42
C3	4.68	I1	11.16
C3S	29.8	I2	10.7
C4	3.45	I3	9.64
C5	2.69	I4	7.58
I5	6.88	I6	5.91

Table 7–1: Test structures and their resistance

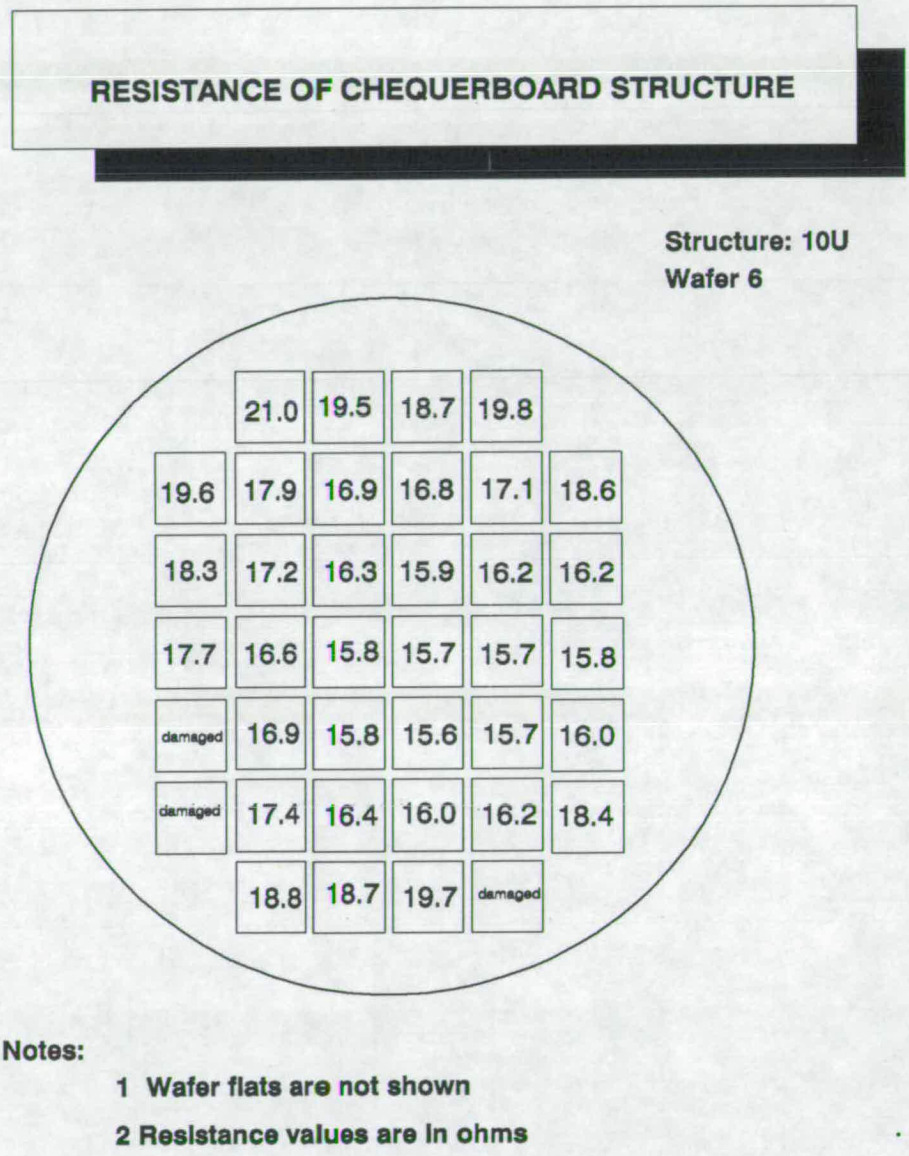


Figure 7–3: Resistance variations of the chequerboard structure 10U across wafer 6

7.3.2 TCR Measurements

The temperature coefficient of resistance measurements were carried out using chequerboard structure F1 as described in chapter 3. The sample resistance versus temperature curves are shown in Figure 7–4. The curves A to E correspond to the successive serial chequerboards in F1. The TCR values calculated from these curves are tabulated in Table 7–2. These measurements clearly showed that the the resistance versus temperature curves were linear as expected and average TCR is 0.33%/°C.

Chequerboard	TCR(%/ °C)
A	0.32
B	0.39
C	0.27
D	0.32
E	0.36

Table 7–2: TCR of chequerboards

7.3.3 Thermal Measurements

Temperature Tracking

In chapter 6 it was described that the chequerboard structure C1 is the DUT (device under test) and the structure C1S is the corresponding temperature monitor (Figure 6-4). That is, the temperature of the DUT during electromigration experiments would be monitored by monitoring the temperature of the adjacent structure C1S. Some measurements were carried out to determine the effectiveness of the structure C1S in tracking the temperature profile of the DUT. The results are shown in Figure 7–5. These measurements were done by using a current of 500 mA through C1 in die 5L of wafer 8 (There are two EU9101 patterns in each die and L denotes the left one).

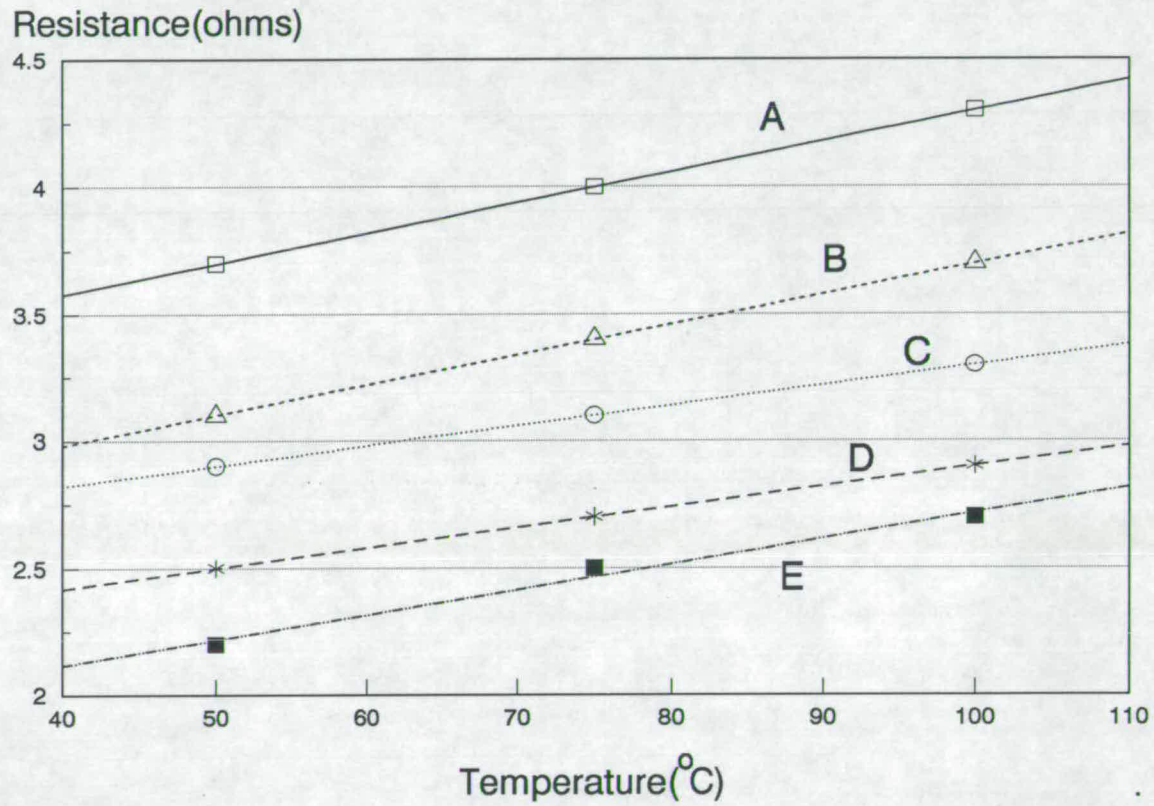


Figure 7–4: Temperature coefficient of resistance measurements

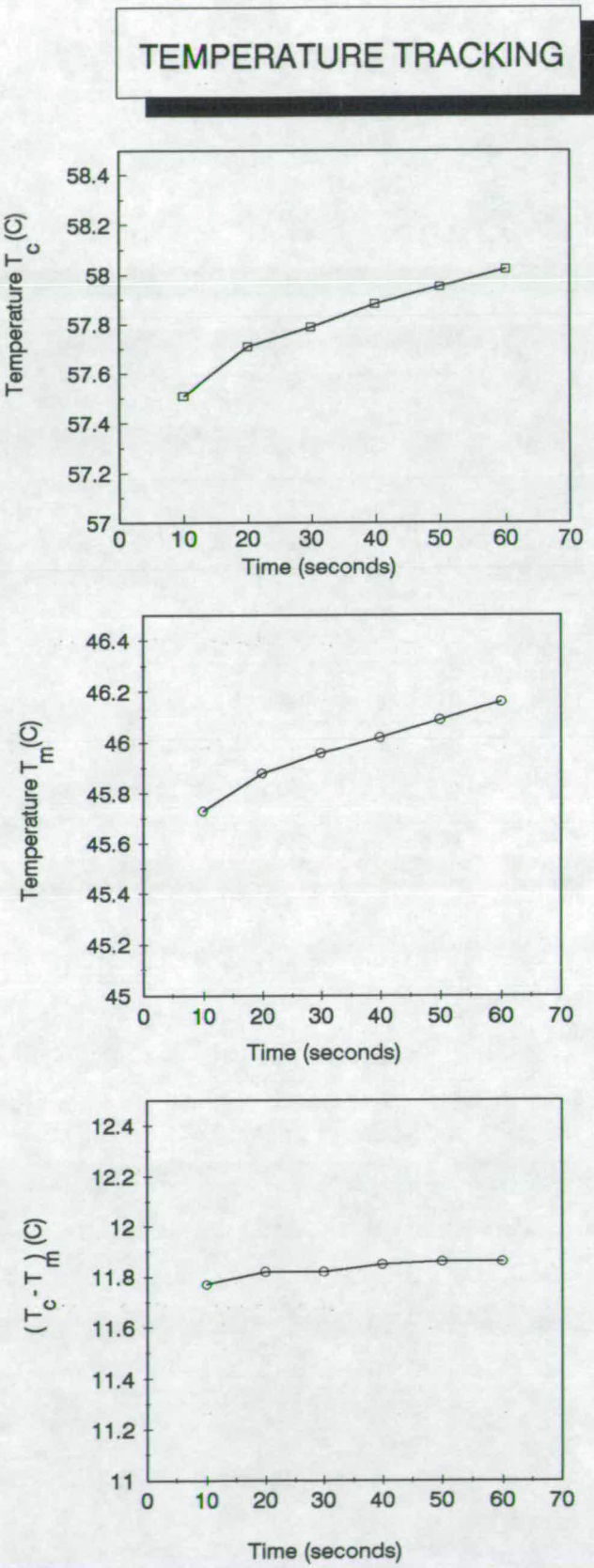


Figure 7–5: Temperature increase in the chequerboard under test C1 and the monitor C1S

The top figure in Figure 7–5 shows the temperature increase in the chequerboard structure C1 during the initial Joule heating period (T_c). The temperature rise was calculated using the increase in resistance from the ambient value and the TCR of the chequerboard. That is, structure C1 is used as its own temperature monitor.

In general,

$$\triangle R = \triangle R_{electromigration} + \triangle R_{temperature} \tag{7.1}$$

where the left side of the above equation represents the total increase in resistance of C1, $\triangle R_{electromigration}$ is the electromigration component of the resistance increase, and $\triangle R_{temperature}$ is the temperature component of the resistance increase. The following approximation was made,

$$\triangle R = \triangle R_{temperature} \tag{7.2}$$

The above approximation in equation 7.2 is reasonable because the resistance increase due to electromigration is expected to be negligible in the short duration test (about 60 seconds). This is based on rough estimations and the experimental observations that the structure typically takes more than few hours to break down as a result of electromigration with a stress current of 500 mA.

The middle figure in Figure 7–5 shows the temperature of the monitor structure C1S (T_m). The temperature estimations were made as usual using the resistance and TCR of C1S. It may be noted that low current was used to measure the resistance of C1S and hence the Joule heating and electromigration in C1S due to the test current is negligible. In other words the resistance increase in C1S with time may be considered to be mainly due to increase in temperature of C1. The bottom figure in Figure 7–5 shows the difference between T_c and T_m and is nearly constant as expected. The close 'temperature tracking' is evident from these figures and the result indicates the good thermal coupling provided by the silicon substrate.

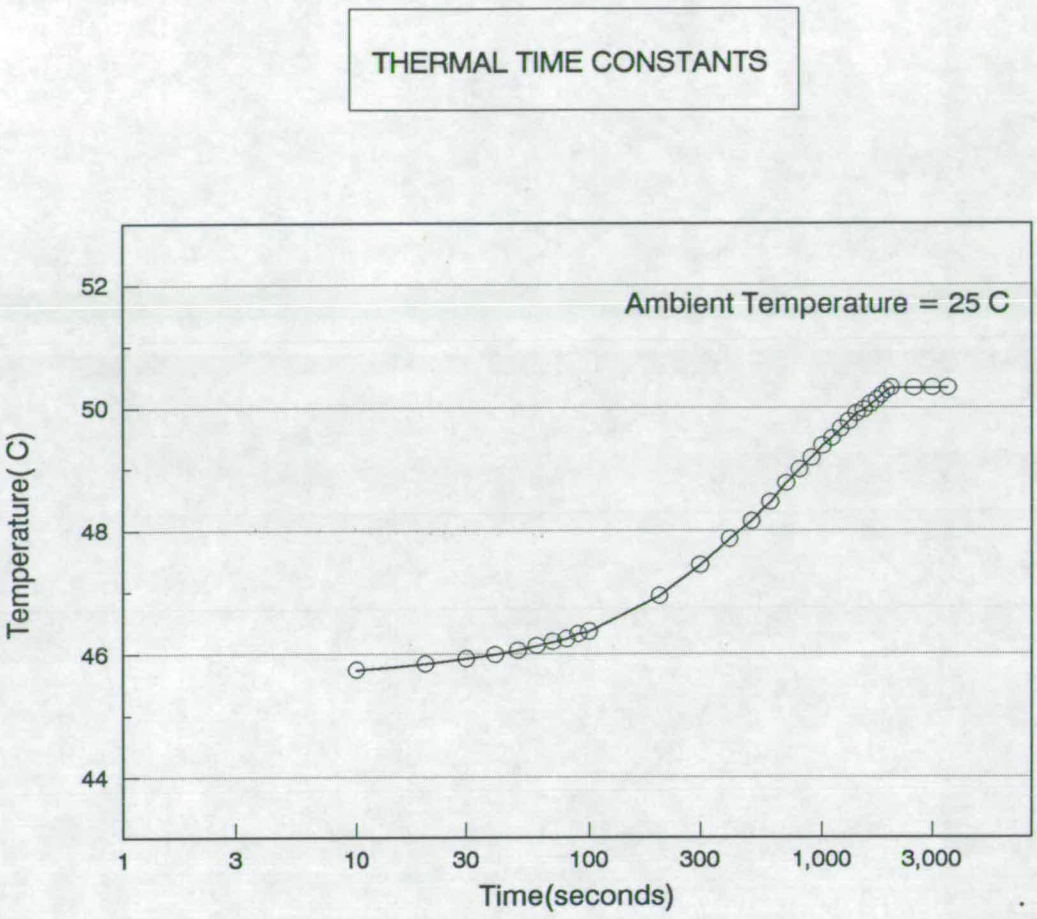


Figure 7–6: Temperature rise versus time in the monitor structure C1S

Thermal Stabilization Time

The temperature of a chequerboard subjected to a stress test increases rapidly in the beginning but nearly levels off after some time and the time required for this is defined as the the thermal stabilization time. The thermal stabilization time depends on the thermal time constants of the various interfaces: metal to oxide, oxide to silicon, substrate to chuck and chuck to outside environment. Typical values of these are given in Appendix E.

A sample result using structure C1 of EU9101 in the die 5R of wafer 8 (There are two EU9101 patterns in each die and R denotes the right one) is given in Figure 7–6. A current of 500 mA was forced through C1 and resistance of C1S was monitored continuously. During monitoring of C1S only low current was used

to measure the voltage drop across C1S. The temperature was monitored every 5 seconds and there were more than 700 data points available, but only sample typical values have been shown. For example, up to 100 seconds there are 20 data points but only 10 have been shown.

The structure C1S attains 45°C much before 10 seconds. That is, the temperature increases from 25°C to about 45°C rapidly and this is not shown in the figure. Similar results were obtained using other die. In Appendix E the procedure used to determine the thermal stabilization time is given. It is typically in the range of 10 to 15 minutes. These measurements clearly show that using too short test times ($\sim$ few seconds) may result in erroneous conclusions about Joule heating.

7.4 Monitoring Resistance-Spikes

One of the major problems in using resistometry technique for electromigration monitoring is the occurrence of random spikes [2]. This was reviewed as a general issue in chapter 3. The chequerboard structures were expected to yield spike-free resistance versus time curves because of the good heat dissipation from the electromigration damage sites (see section 5.3). In order to verify this prediction, the resistances of chequerboards subjected to electromigration experiments were monitored through an oscilloscope at regular intervals and also the resistance values were continuously stored in an hard disc by the microcomputer for about 1000 minutes. Figure 7–7 shows a typical plot generated from the stored data.

The measurements shown in Figure 7–7 were done using a packaged device at 125°C and a current of 100 mA. Structure F1 of EU9101 was used because more than one chequerboard could be stressed at once. The three lines A, B, C correspond to the three serial chequerboards in the same structure. The measurements showed the integrity of these structures for electromigration stresses being applied for a long time and the absence of spikes. A number of spike-free resistance

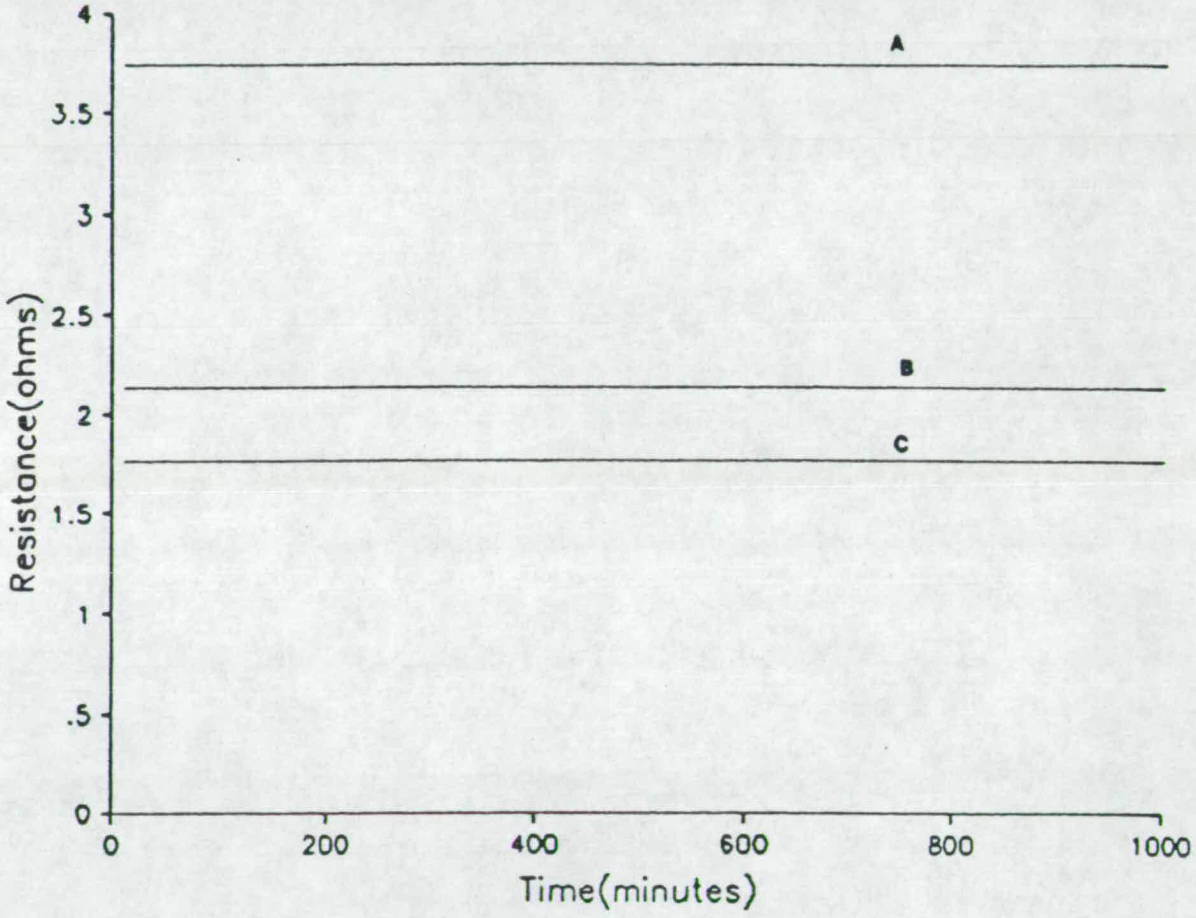


Figure 7–7: Resistance monitored for a long stress period to verify the non-ocuurence of spikes

versus time curves were obtained as part of the resistometry measurements and some of these are shown elsewhere in the thesis.

7.5 Resistometry Measurements

7.5.1 Resistometry with Self-Heating

It may be recalled that in this technique external heating is not necessary and metallisation failure can be accelerates by using high currents to cause a temperature rise in the metallisation. Structures in row CI of EU9101 are suitable for these measurements since the temperature profile in the chequerboard under test can be obtained as described in chapter 6 (see section 6.2.2).

A number of experiments were carried out with the following aims:

1. To study the general nature of resistance-time curves of chequerboards.

2. To use the resistometry technique to monitor the effect of one of the parameters on electromigration, namely, average segment width.

The measurements indicated that in general the resistance versus time curve looks as shown in Figure 7–8. This particular curve was obtained using the structure C1 in the wafer 8 and a current of 700 mA. It is clear that the resistance increases gradually and then shoots up just before the failure. The temperature profile of the structure during its life period and as recorded by the temperature monitor is shown in Figure 7–9.

These figures confirmed the general expectation of three characteristic regions of the resistance versus time curve. Another striking feature was the sudden increase in the resistance after about 8 to 10 % near-linear increase in resistance.

The visual examination of the failed chequerboards revealed that these structures fail in a characteristic 'chain-like' fashion. A few typical optical micrographs

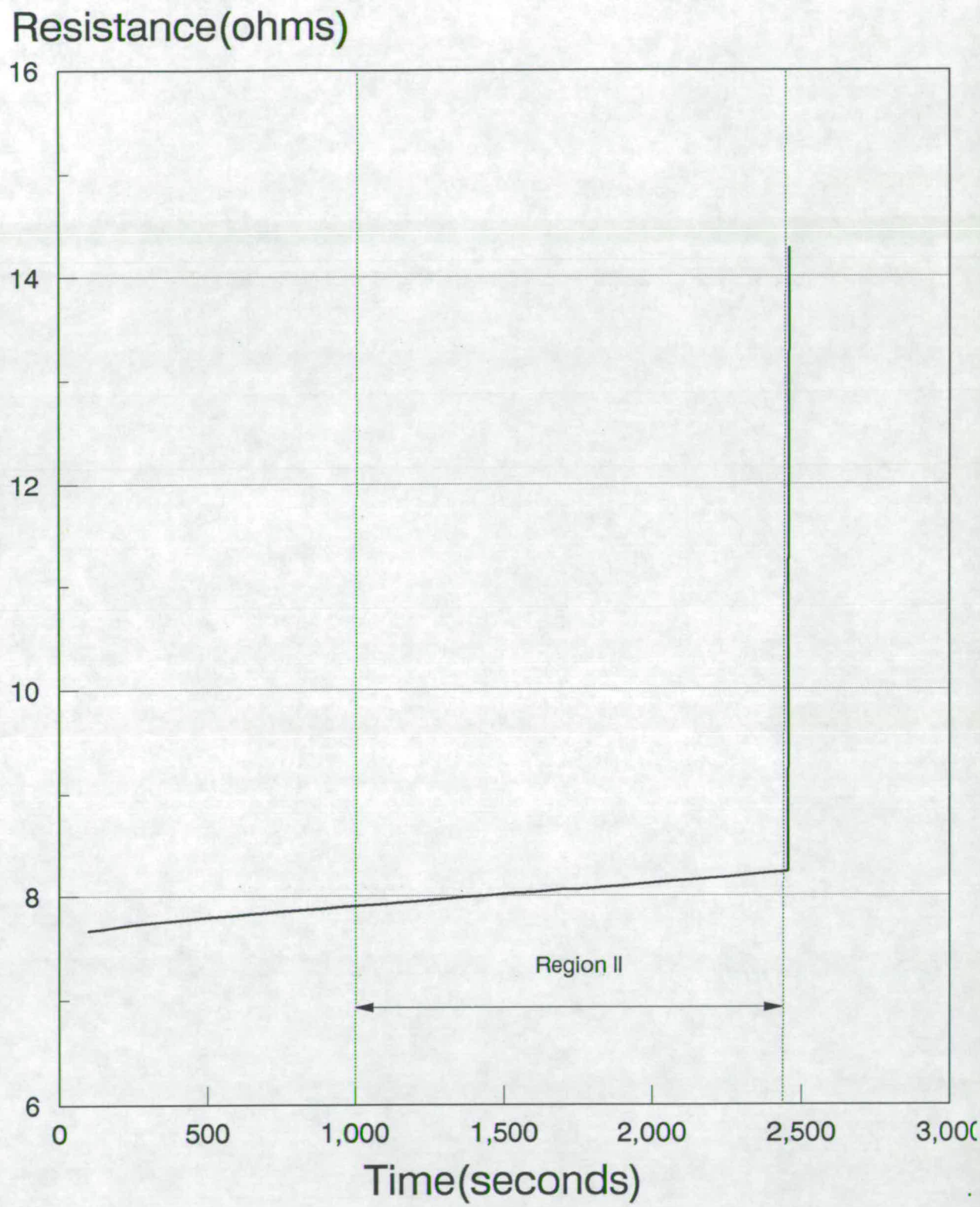


Figure 7–8: Typical resistance-time curve

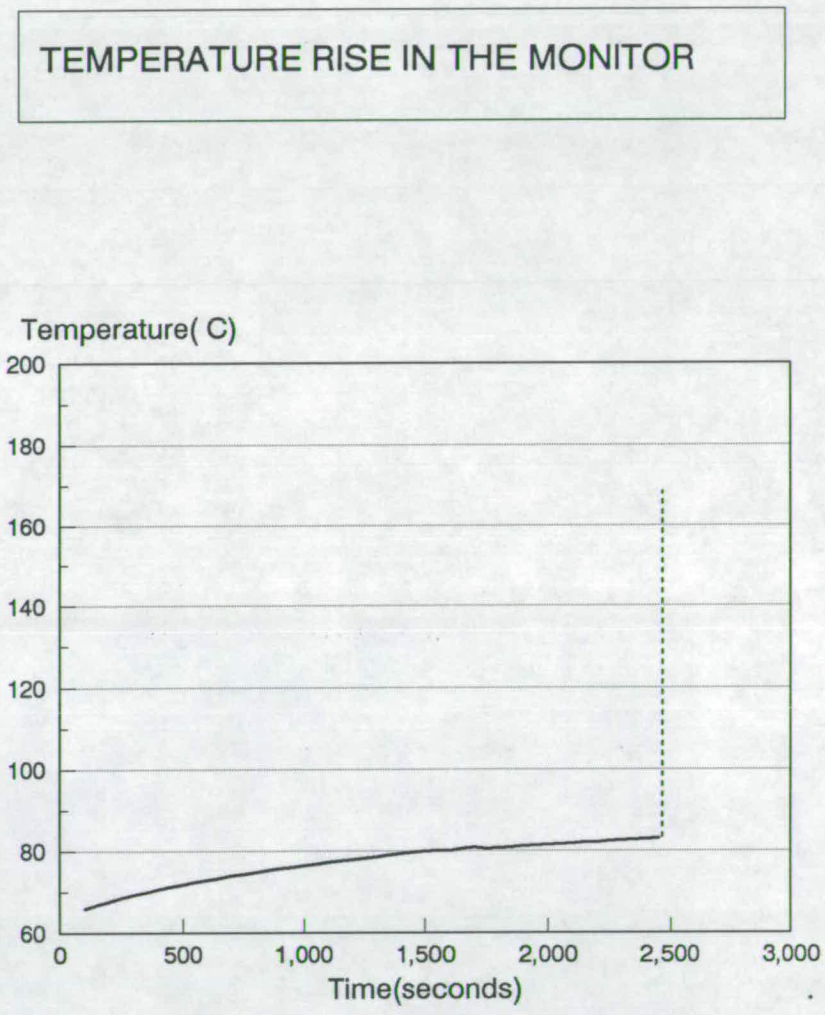


Figure 7–9: Temperature profile recorded by the monitor structure

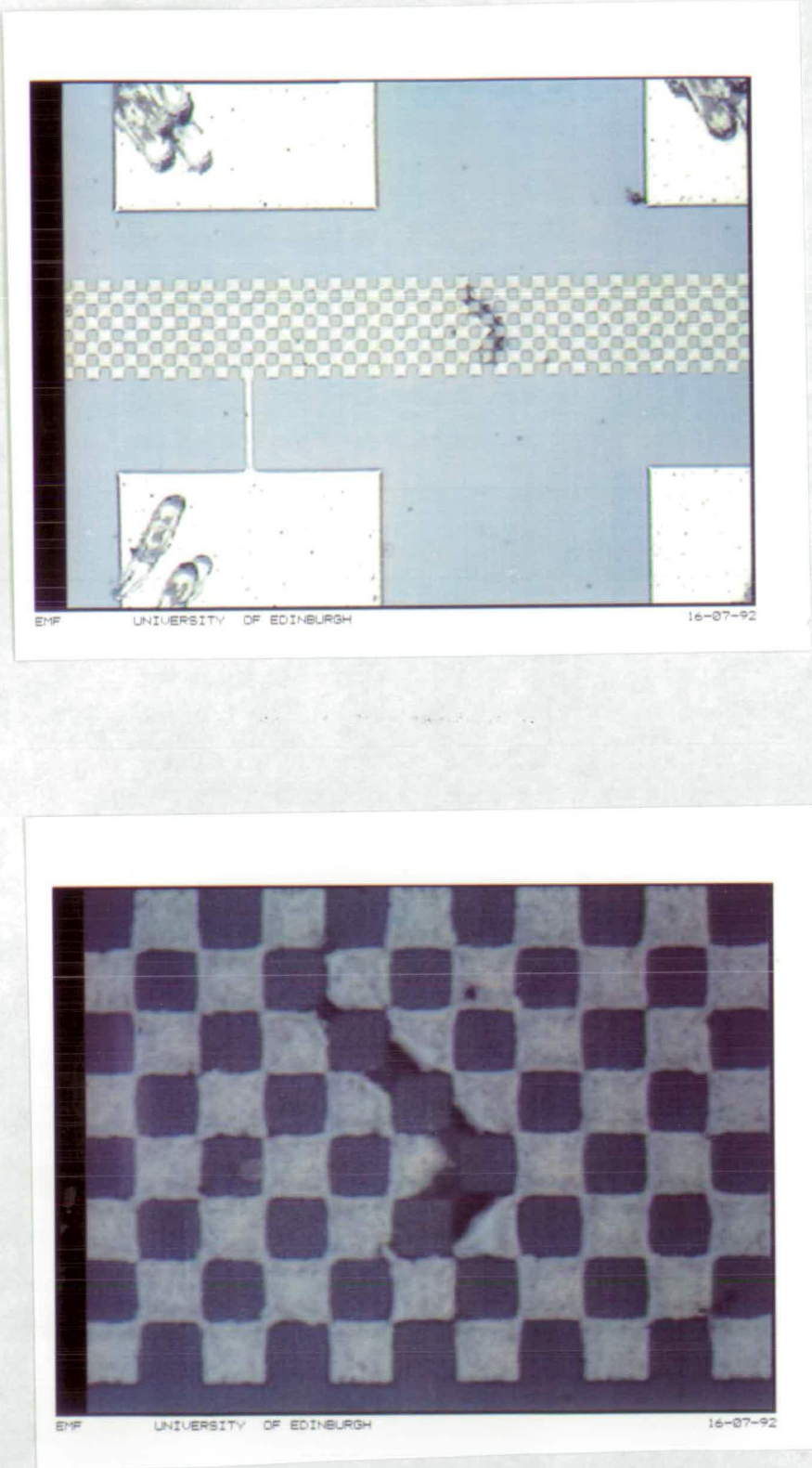


Figure 7–10: Optical micrographs showing chain-like failure in chequerboards

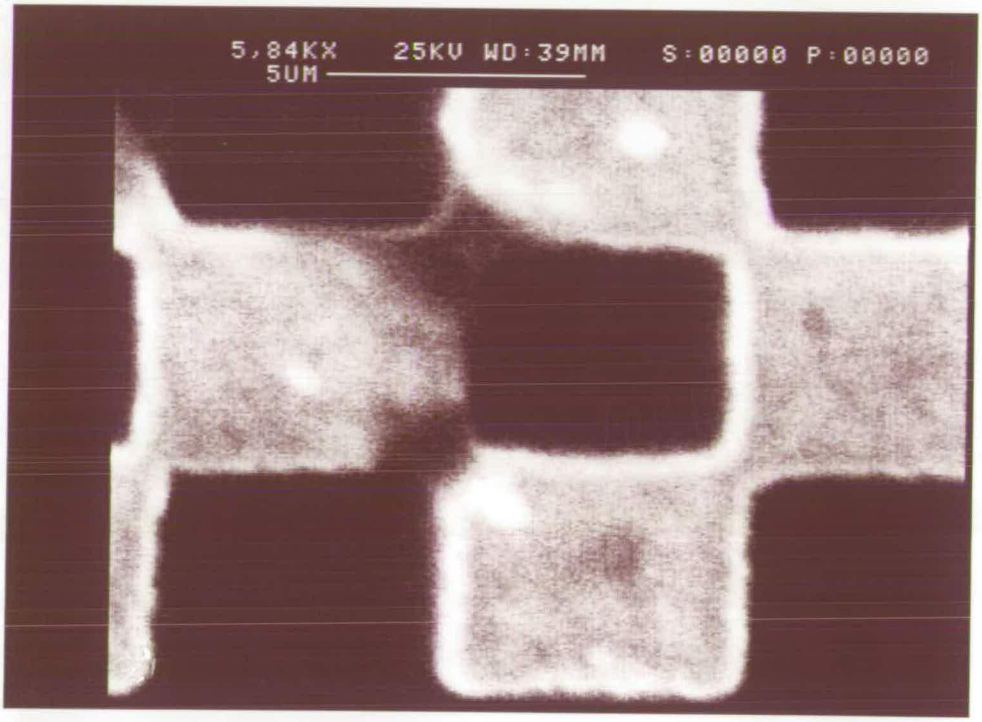


Figure 7–11: SEM micrographs showing the magnified view of chequerboard failure sites

are shown in Figure 7–10 while a typical scanning electron micrograph of adjacent overlap regions is shown in Figure 7–11.

The chain reaction failures may be explained by the increase in current density in all the parallel segments when one of the segments fails.

Extraction of Parameters m and n

Having studied the general nature of resistance versus time curves of chequer-boards, the next step was to study the region II in detail. That is, to analyse the near-linear region of the resistance versus time curve to extract the parameters m and n. It may be recalled that m and n are defined by:

$$R = R_o \exp(mt^n) \tag{7.3}$$

where R_o is the resistance at time $t = 0$ and R is the resistance at time t. The time $t = 0$ is counted from the time the temperature stabilization has occurred. The resistance versus time curve in the region II obtained for structure C1 (die 7 wafer 8) is shown in Figure 7–12. 700 mA current was used.

The following values for m and n are obtained from the measured resistance versus time data by curve fitting :

$$m \simeq 3.8 \times 10^{-5} s^{-n}$$
$$n \simeq 0.9$$

The curve obtained by substituting these values of m and n in the equation 7.3 is also shown in the Figure 7–12. The close agreement between the measured values (dotted line) and the values obtained by using the above values of m and n in the resistometry equation is quite obvious. Similar near-linear resistance curves were obtained for other structures in row CI of EU9101 and the values of m extracted are tabulated in Table 7–3. (n is nearly equal to 1 in all these cases).

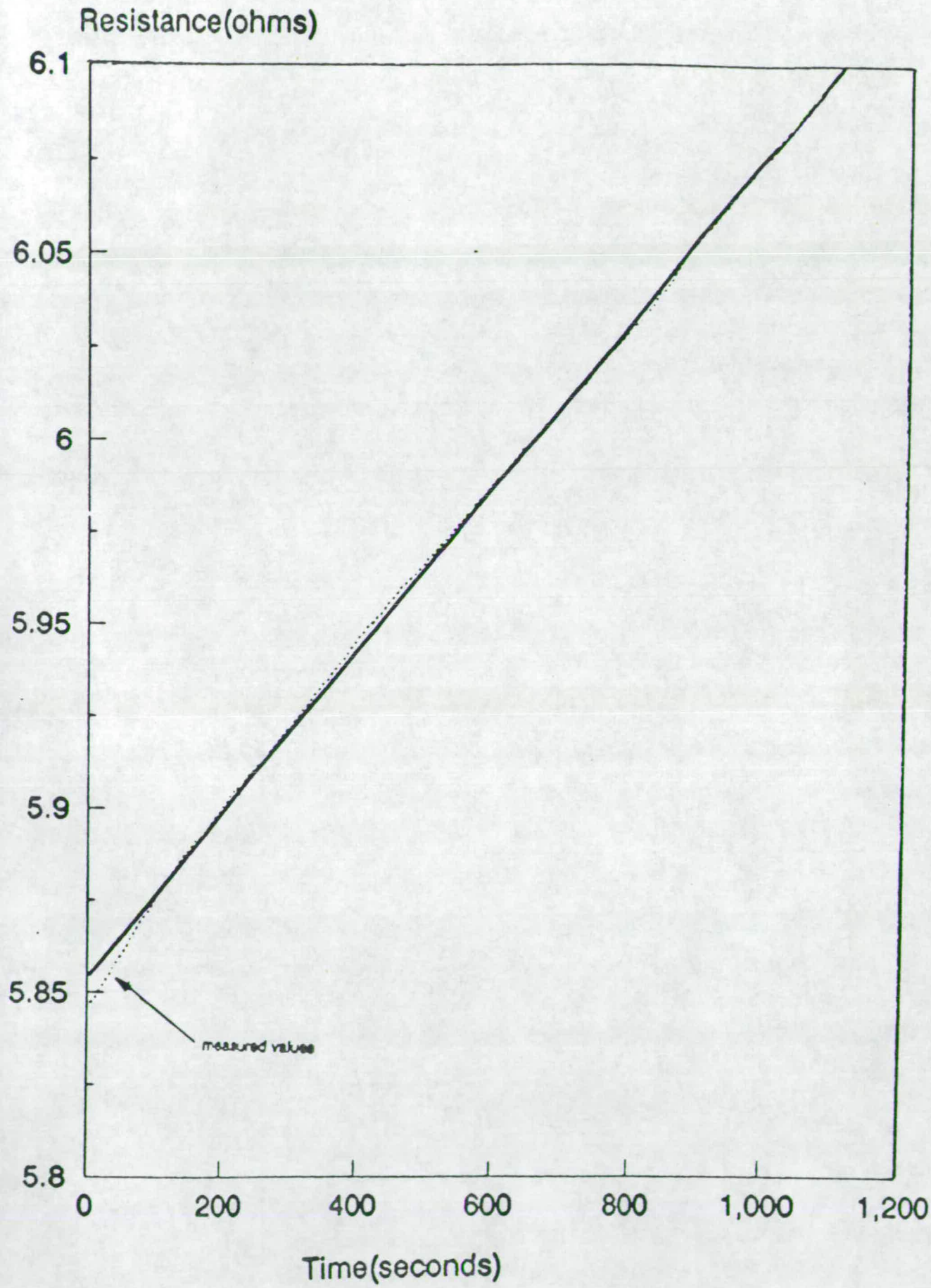


Figure 7–12: Resistance versus time curve in the region II

Die Number	Structure	m ($\times 10^{-6} s^{-1}$)
13L	C1	35.0
13L	C2	17.4
13L	C3	5.0
12R	C1	38.0
12R	C2	20.0
12R	C3	5.6
14R	C1	38.5
14R	C2	16.0
14R	C3	4.5
8R	C1	38.0
8R	C2	17.4
8R	C3	4.2

Table 7–3: The values of m extracted from the measured resistance data and using the resistometry equation

Normalisation of m and MTF Estimation

The values of m listed in the table 7–3 are those obtained using a current of 700 mA through the structures C1, C2 and C3 of EU9101. Since these samples have different overlap widths (a) and hence different segment widths (d_2), the current density in the segments will be different. The temperature rise may also be different depending on the electrical and thermal resistance. The parameter m is a measure of the average mass transport and hence is expected to vary depending upon the values of the current density and temperature. If we wish to compare the values of m of structures C1, C2 and C3, normalisation is required to illustrate the equivalent values of m for identical stress conditions.

The normalisation of m was carried out using the following equations based on the Black's equation:

$$m_{cnd1} \propto j_{cnd1}^2 \exp(-E_a/kT_1) \tag{7.4}$$

$$m_{cnd2} \propto j_{cnd2}^2 \exp(-E_a/kT_2) \tag{7.5}$$

$$m_{cnd2} = m_{cnd1}\left[\left(\frac{j_{cnd2}}{j_{cnd1}}\right)^2 \exp\frac{E_a}{k}\left(\frac{1}{T_1}-\frac{1}{T_2}\right)\right] \tag{7.6}$$

where, m_{cnd1} and m_{cnd2} are the values of m at stress conditions 1 and 2 respectively having current density values of j_{cnd1} and j_{cnd2} and temperatures T_1 and T_2 respectively. E_a is the activation energy. The structures C1, C2 and C3 on the same die were compared and normalisation was carried out using the stress conditions of structure C3 as a reference. The temperatures T_1 and T_2 were estimated from the temperature monitor structures and the results are shown in Table 7–4.

The average current density was calculated using the average segment width d_2. For example, if $d_2 = 1\mu$m, thickness = 0.61 μm and the current through the segment is 10 mA then,

$$j = \frac{10\text{mA}}{1\mu\text{m} \times 0.61\mu\text{m}} = 1.64 \times 10^6 \text{A/cm}^2$$

Die Number	Structure	normalised m ($\times 10^{-6} s^{-1}$)
13L	C1	116.1
13L	C2	103.2
13L	C3	5.0
12R	C1	121.3
12R	C2	102.2
12R	C3	5.6
14R	C1	120.1
14R	C2	83.7
14R	C3	4.5
8R	C1	123.7
8R	C2	108.7
8R	C3	4.2

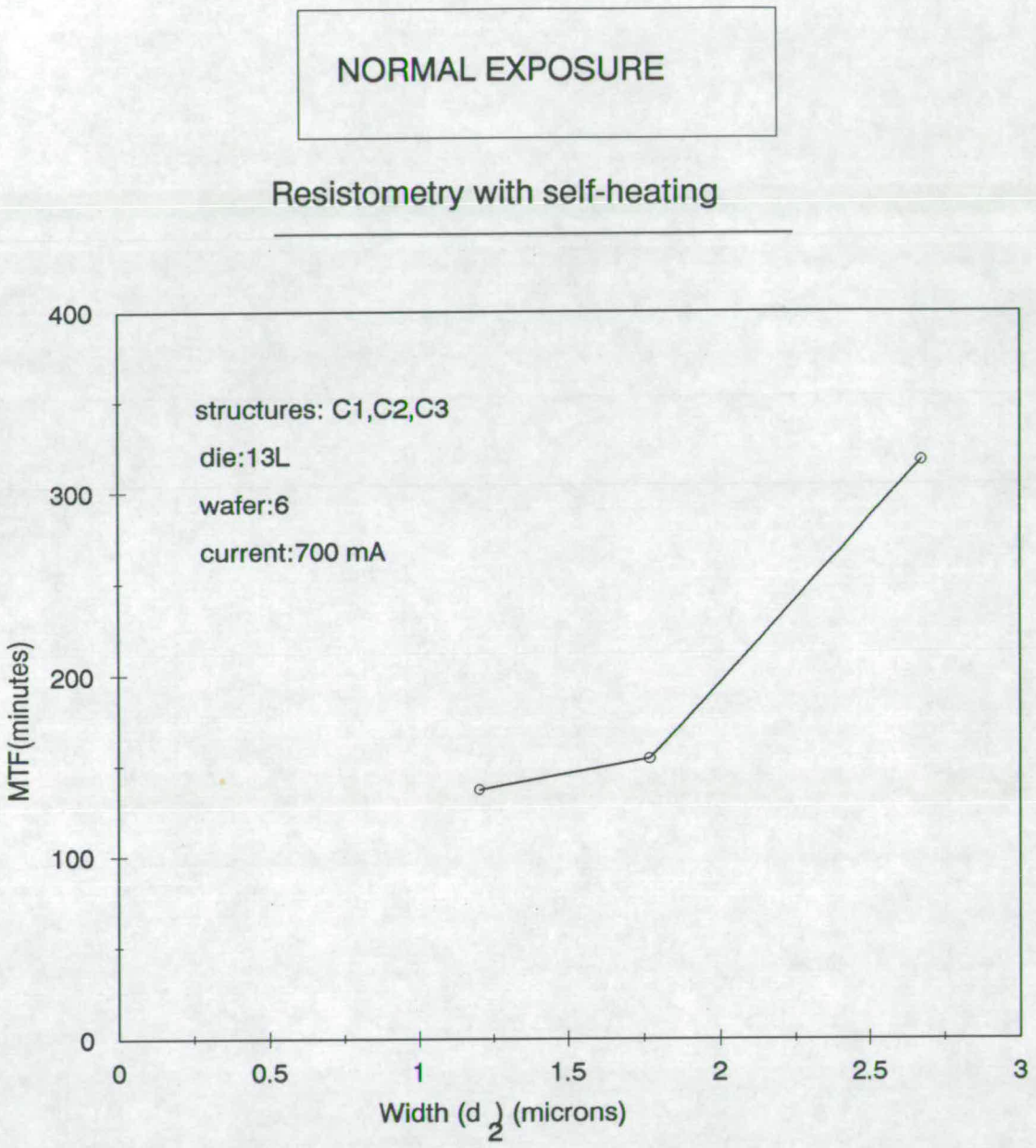
Table 7–4: Normalised values of m

The main reasons for using the average current density and not the current density at the corners are:

- If we are monitoring the failure times of 'weak-spots', current density at the corners may be important. But, in resistometry it is the average mass transport rate that is measured and not the mass transport rate at any specific site. Even in the case of classical tests which essentially measure the failure time of the 'weak-spots', only average current density values are considered [3]. The justification for this is based on empirical results [4,5]. In other words, it means that the MTF does not decrease as suggested by Black's equation, that is, (MTF $\not\propto j^2_{corner}$)

- The reason why the MTF does not decrease as one would expect from the higher current densities at the corners is expected to be due to the complex nature of the geometry and microstructural defects at the corners and is not attempted in this thesis.

MTF estimations were done using the method described in chapter 4 and using the average current density. Typical results are shown in Figure 7–13. This is for the die 13L shown in the table 7–4. A similar MTF decrease with width was noticed for the other die listed in the table.



Note:

1. 10% increase in resistance considered a failure

2. Stress conditions normalised wrt C1

Figure 7–13: MTF versus d_2 segment width

7.5.1.1 Measurements on Wafer across which Exposure was Varied

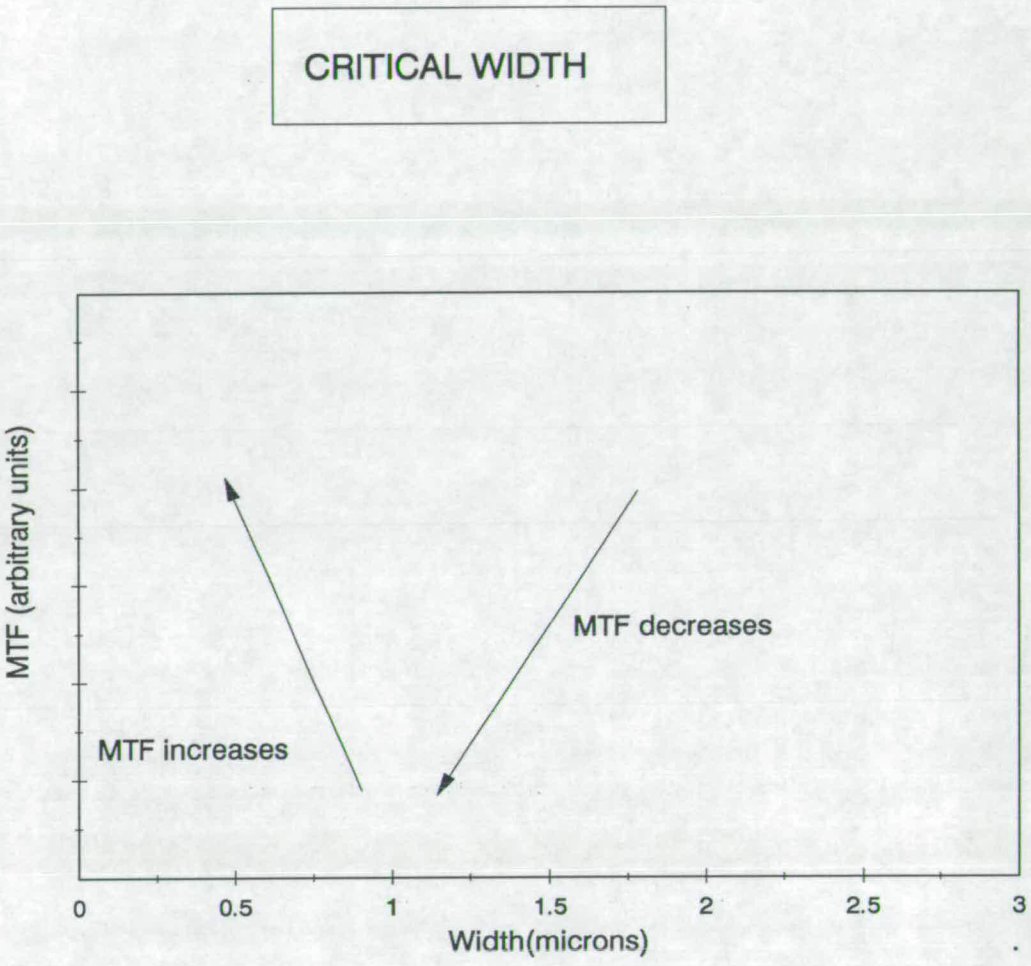


Figure 7–14: MTF versus segment width

The above methodology of extraction of the parameters m and n, normalization and MTF estimation was repeated for wafer 5 which had gone through the exposure matrix as described in chapter 6. The main purpose of this methodology can be described through Figure 7–14. The aim was to observe the increase in MTF with decrease in segment width in the sub-micron region. It may be recalled that the exposure time was increased in step of 20 ms starting from die 1 and was expected to have the same effect as overetching and hence we can expect the average width to decrease from die 1 to die 38. The d_2 reduction was further confirmed by visual examination (segment width d_2 has been defined in Figure 6-3). For example, the optical micrographs A (lower exposure) and B (higher ex-

posure) given in Figure 7–15 show the effect on d_2 caused by increased exposure. Further, resistance is expected to increase as the exposure time is increased and the results shown in the Figure 7–16 confirm this. The average segment width was obtained using the scanning electron microscope, the results of dimensional and resistometry measurements are summarised in table 7–5 while the corresponding variation of MTF with d_2 segment width is shown in Figure 7–17

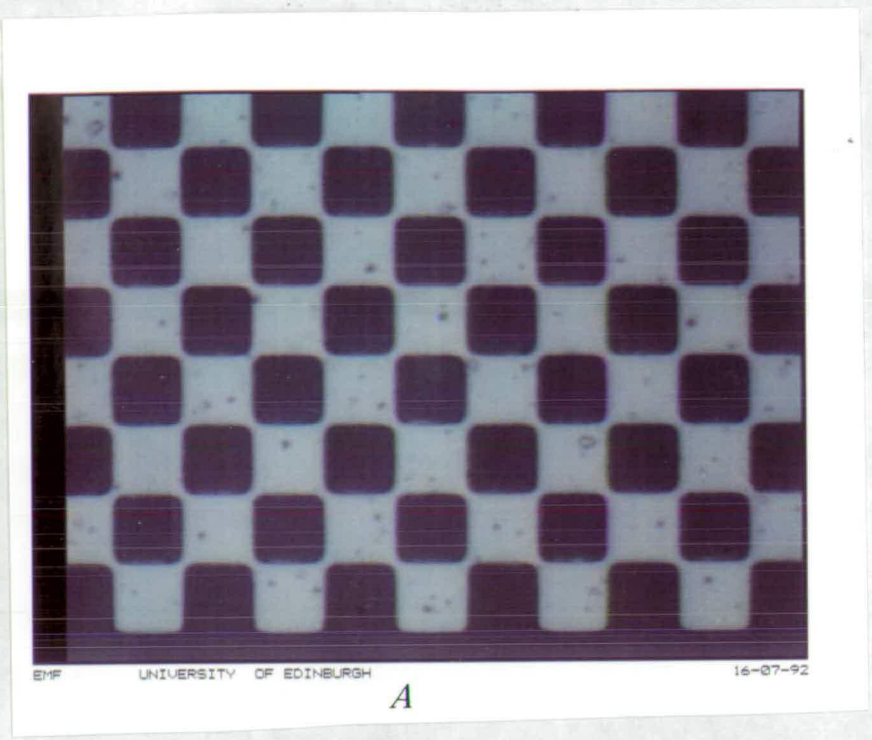
Die Number	d_2 (μm)	measured m ($\times 10^{-6} s^{-1}$))	normalised m ($\times 10^{-6} s^{-1}$)
13L	1.10	10.0	10.0
19L	0.90	1.88	0.65
25L	0.64	3.02	0.26

Table 7–5: Dimensional and resistometry measurements on wafer 5 across which the exposure was varied

7.5.2 Resistometry with External Heating

Generally resistometric measurements are carried out on packaged devices using external heating in an oven [6] and test times may be in the range of few tens of hours to few days. Longer test times are usually required because low currents which do not cause significant Joule heating (less than about 2 to 3 °C) are used. In spite of the long test times, this is the most commonly used resistometry technique to study electromigration and hence it was thought appropriate to use this with chequerboards. However, it may be recalled that this is not intended as a routine process monitor test because of the long test times but it may be used to determine the critical width.

Structure F1 of EU9101 was used for this experiment. It may be recalled that this is a serially connected chequerboard in which the designed overlap (a) increases from 0.2 μm to 2 μm in steps of 0.2 μm. But, because of the offset-error of 0.2 μm introduced during mask making the actual overlap width increases from 0.4 μm to 2.4 μm. The d_2 segment widths were measured using the SEM



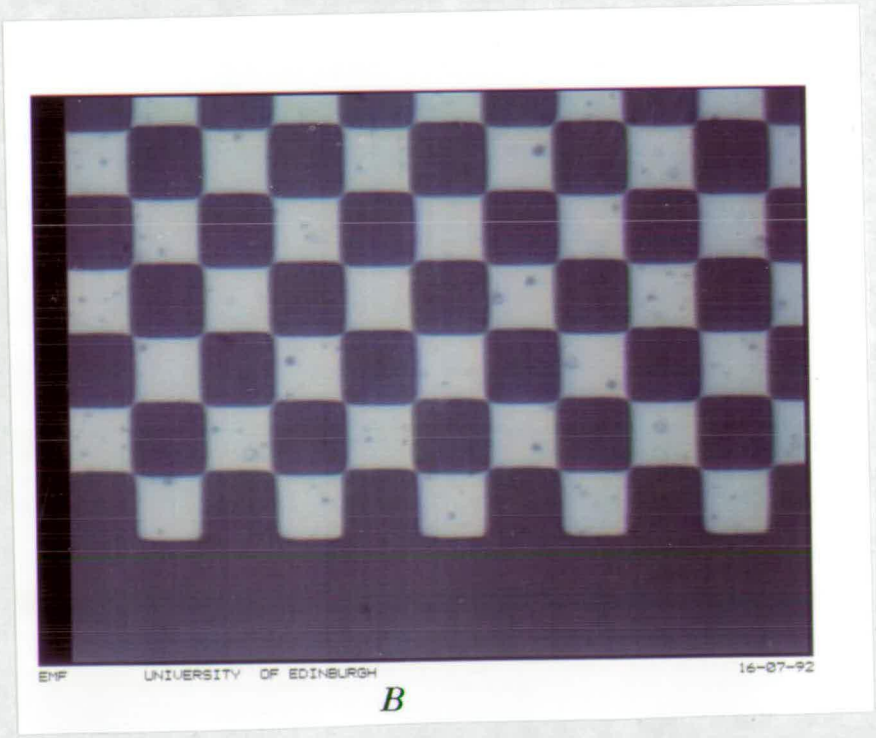


Figure 7–15: The reduction in segment width d_2 caused by increased exposure

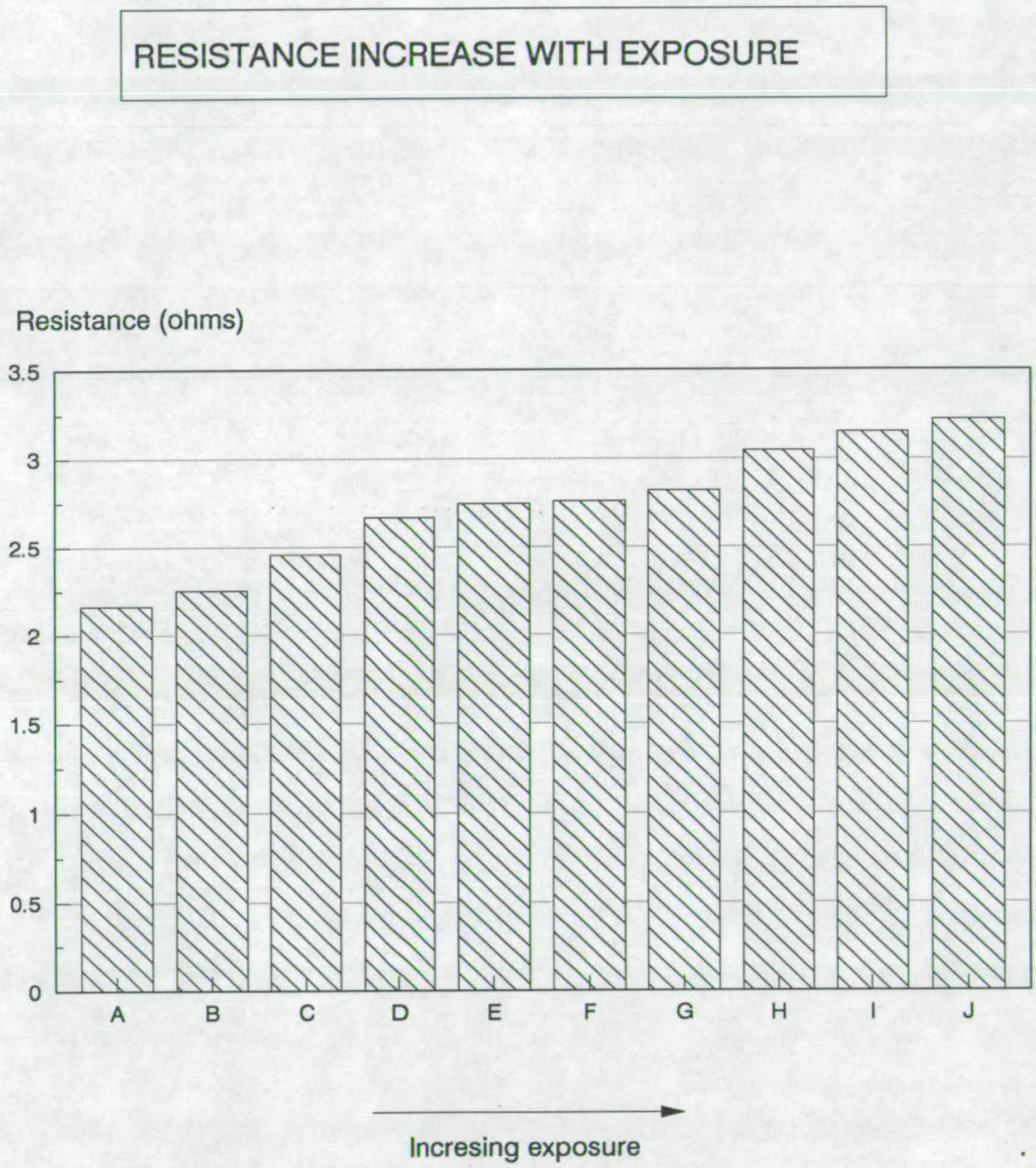


Figure 7–16: Resistance increase across wafer 5

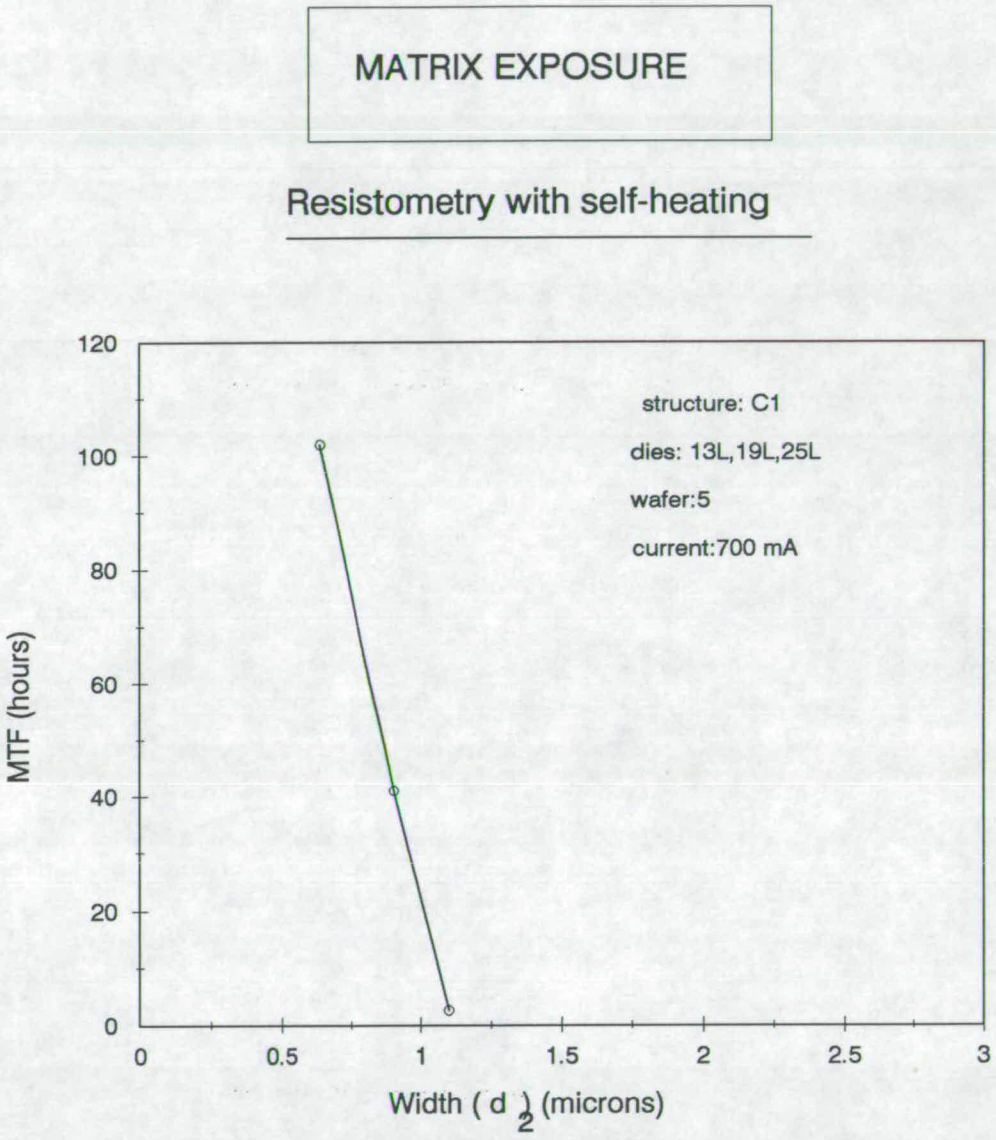


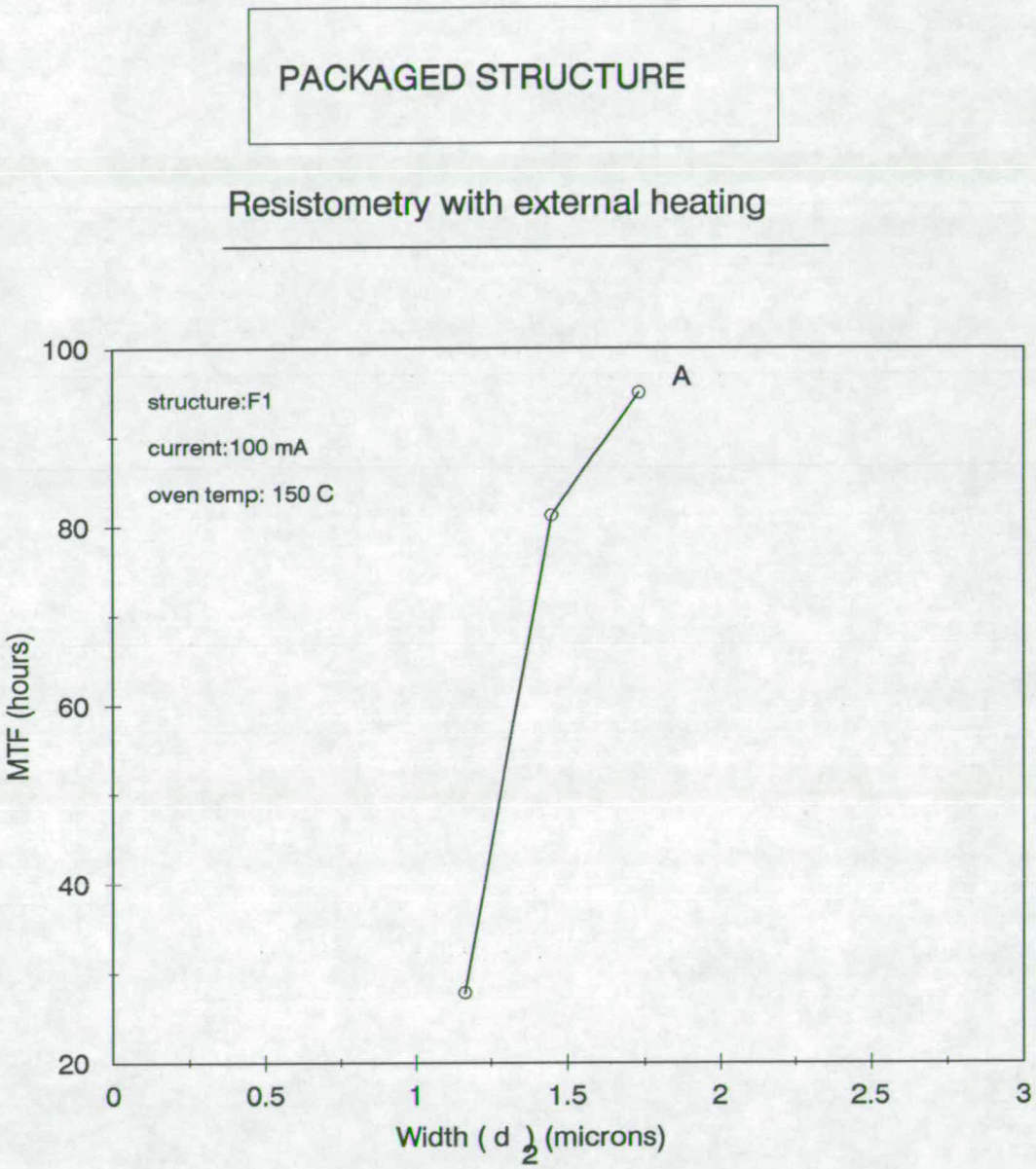
Figure 7–17: MTF versus d_2 segment width

as described earlier. The values are given in table 7–6. The structure was wire bonded and packaged in a DIP (dual-inline-package).

The package was heated in an oven and resistances were measured at 50 °C, 100 °C, 125 °C and 150 °C to determine the TCR ($\sim 0.34\%/^{o}C$). Using this value of TCR the temperature rise due to Joule heating for a current of 100 mA was found to be about 3 °C. The resistometry experiments were carried out at 150 °C and 100 mA. The resistance versus time of the three successive chequerboards (a=0.4, 0.6 and 0.8 μm respectively) were monitored. The parameters m and n were extracted and the values of m were normalised as usual. The parameter n was nearly equal to 1 for all the three chequerboards. The values of m are shown in table 7–6. The normalised values of m shown in table 7–6 are with respect to the stress (current and temperature) conditions of the 0.8 μm overlap width chequerboard. All the samples were stressed till they failed ('open-circuit') and whenever a failure occured, the failures were analysed and the experiments were continued by shorting the appropriate package pins. All the chequerboards showed the usual chain-reaction failures. The MTF vales were derived from the normalised values of m as usual. The MTF versus d_2 segment width variation is shown in Figure 7–18.

Overlap(a)(μm)	d_2(μm)	measured m ($10^{-7}s^{-1}$))	normalised m ($10^{-7}s^{-1}$)
0.4	1.17	24.5	9.5
0.6	1.45	5.1	3.3
0.8	1.73	2.8	2.8

Table 7–6: Measurements for packaged structure



Note:

1. 10% increase in resistance considered a failure
2. Stress conditions normalised wrt the chequerboard A .

Figure 7–18: MTF versus d_2 segment width

7.6 Fast Tests

Can we use resistometry techniques to monitor electromigration by ramping the power quickly to cause catastrophic failure processes within a few tens of seconds ? This was motivated by the SWEAT [7] tests. Chequerboard structures C1, C2, C3 and F1 of EU9101 were subjected to rapid electromigration experiments. The expected break-down time due to electromigration was within a few tens of seconds. These experiments produced inconsistent results. For example, the electromigration damage sites were not localised to overlap regions only but included the large metal squares and the chequerboard end-pads also. Optical examination of the failed chequerboards indicated a complete destruction of the sample as shown in Figure 7–19 unlike the characteristic chain-reaction failures. The results are briefly discussed in section 8.2 on suggestions for further work.

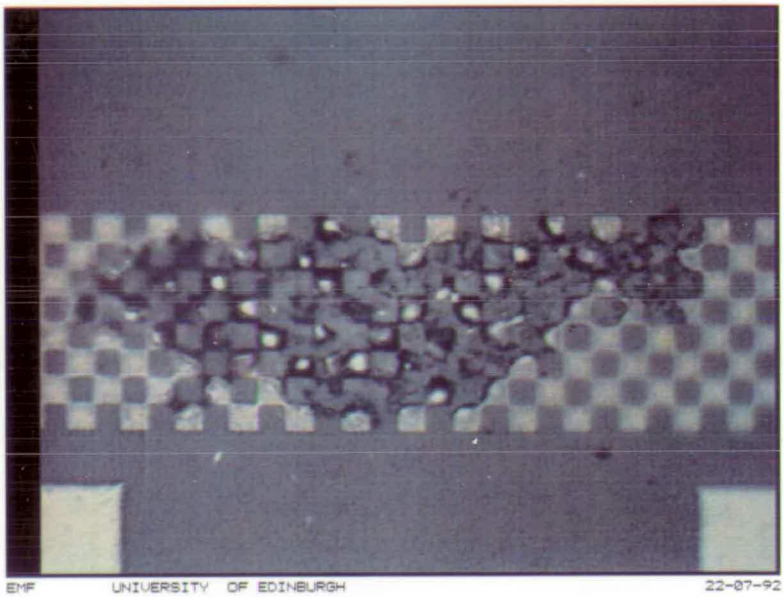


Figure 7–19: A typical optical micrograph of fast-test failure

7.7 Analysis of Test Results

7.7.1 Determination of Activation Energy

Using Black's equation and the MTF expression based on resistometry, we get:

$$m = C' \exp(-E_a/kT) \tag{7.7}$$

where E_a is the activation energy, k is Boltzmann constant, T is the temperature and C′ is a constant. Taking logarithms on both sides of the equation 7.7 we get:

$$\ln m = \ln C' - \frac{E_a}{kT} = C'' - \frac{E_a}{kT} \tag{7.8}$$

where $C'' = \ln C'$, is a constant. From equation 7.8, a plot of $\ln m$ versus $1/T$ should yield a straight line with slope E_a/k.

A typical plot is given in Figure 7–20.

The activation energy is given by

$$\begin{aligned} E_a &= slope \times k \\ &= (6045 \pm 2100) \times (8.617 \times 10^{-5} \text{ eV K}^{-1}) \\ &\simeq 0.5 \pm 0.2 \text{ eV} \end{aligned}$$

The activation energy so obtained is believed to be an effective average value of the various mass transport mechanisms having different activation energies [8, 9,10]. For example, around 0.5 eV for grain boundary diffusion and around 1.2 eV for bulk diffusion. It may be noted that in general the activation energy for aluminium-silicon thin films is reported to be in the range 0.4 to 0.8 eV [11] and using conventional MTF measurements a value of 0.8 eV was obtained (chapter 3).

7.7.2 MTF Variations with Width

It may be recalled that in general the MTF is expected to decrease with a decrease in track width to the critical width. Below that point it is expected to either

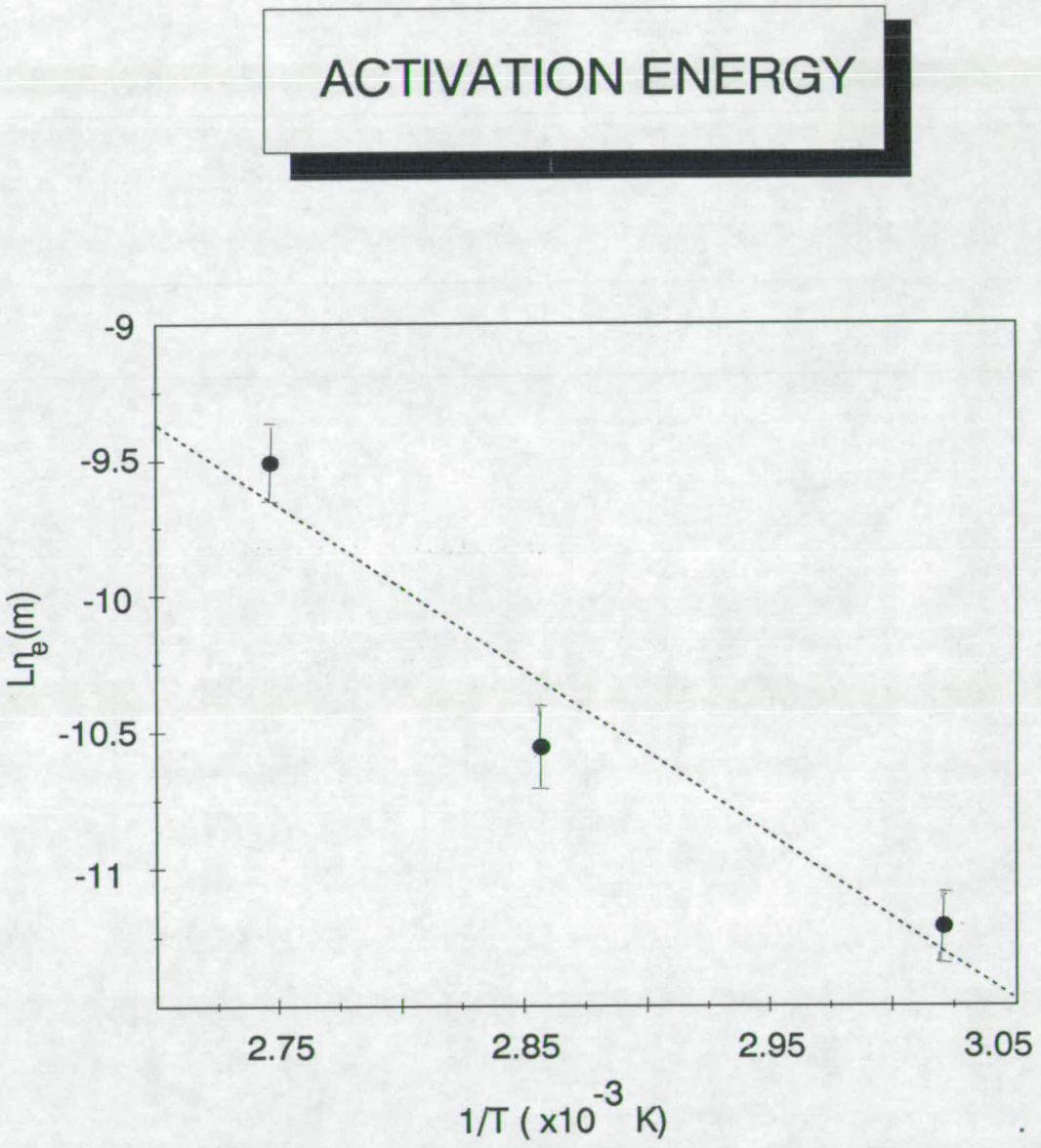


Figure 7–20: Parameter m versus 1/T to determine activation energy

level off or increase. At about the critical width the grain structure may be approximated to a 'bamboo' structure (Figure 2-2).

The designed overlap width in a chequerboard (dimension (a) in Figure 6-3) was in the range of 0.2 μm to 2.0 μm. But because of the offset-error in the mask dimensions the achieved range was 0.4 μm to 2.4 μm and hence with normal exposure we could provide a segment width d_2 greater than about 1 μm. This is because,

$$d_2 \simeq \sqrt{2}a + 0.6\mu m$$

as shown earlier and for $a = 0.4$ μm , $d_2 \simeq 1.17$ μm. Therefore, to get the complete picture of how the MTF varies with width, both the normal exposure (see Figure 7–13) and the matrix exposure (see Figure 7–17) results are necessary.

It follows from these figures that the critical width is around 1 μm. The median grain size is expected to be typically about 1 μm and hence [12] the critical width meets the general expectations. The microstructural confirmations such as confirming 'bamboo' structure through TEM studies could not be carried out because of sample preparation problems. However, new techniques are now available which do not require any specialised sample preparation. This new technique is briefly described in the section on suggestions for further work in chapter 8.

7.7.3 MTF of a Single Segment

The estimation of MTF of a single segment may be made by considering the chequerboard as a series-parallel structure formed by the overlap regions as shown in Figure 7–21. The statistical methods quite commonly used in the analysis of electromigration of series-parallel elements [13,14] may also be here. The definitions and mathematical details of the statistical distributions (for example, probability density function and cumulative distribution function of the lognormal distribution) are discussed in Appendix C.

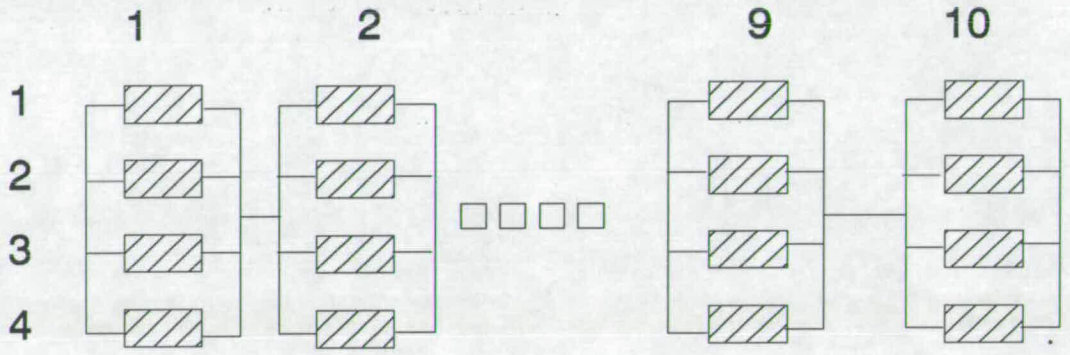


Figure 7–21: Series-Parallel representation of a chequerboard with n_s=10 and n_p=4

Let,

n_s = number of serial elements

n_p = number of parallel elements

t_{50sp} = MTF of the chequerboard (series-parallel system)

$\mu_0 = \ln t_{50}$

t_{50} = MTF of a single element

σ_0 = sigma of the element failure time distribution

Then it can be shown that (the mathematical details are given in Appendix D)

$$\ln t_{50sp} = \mu_0 + \sigma_0 \phi \tag{7.9}$$

where,

$$\frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\phi} \exp(-z^2/2)\, dz = \left[1 - (1/2)^{1/n_s}\right]^{1/n_p} \tag{7.10}$$

Given the values of n_s and n_p ϕ can be obtained from statistical tables and hence t_{50sp} can be calculated.

As an example, the MTF results obtained for chequerboards for the packaged structure (see Figure 7–18) are used to estimate the single segment MTF. Since $n_s = 39$ and $n_p = 7$ for these chequerboards, the right hand side of equation 7.10 simplifies to:

$$\left[1 - (1/2)^{1/n_s}\right]^{1/n_p} \simeq 0.5616$$

Now, using statistical tables to get the value of ϕ satisfying the equation:

$$\frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\phi} \exp(-z^2/2)\, dz = 0.5616$$

we get,

$\phi \simeq 0.16$

We require the value of σ_0. We can use the value 0.278 obtained from the conventional MTF measurements as on approximation. However, it should be noted that this approximation is valid for linewidths greater than the critical width. In the calculations shown here we are considering the chequerboards with d_2 greater than about 1 μm and hence the approximation is valid. Rearranging equation 7.9, MTF of single element can be expressed as:

$$\text{MTF single element} = \exp[\ln t_{50sp} - \sigma_0 \phi] \tag{7.11}$$

The results of the above calculations are given in table 7–7

$d_2(\mu m)$	t_{50sp} (hours)	MTF of single segment(hours)
1.17	28	27
1.45	81	78
1.73	95	91

Table 7–7: Estimation of MTF of a single segment

Table 7–7 indicates that in this particular case ($n_s = 39$ and $n_p = 7$) the MTF of the system t_{50sp} (i.e. chequerboard) is slightly higher than that of the corresponding single element MTF.

Bibliography

[1] Programming and service manual. hp model 3495A Scanner. page 3-1.

[2] G. Specchiulli, F. Fantini, and G. Desanti. Electromigration in narrow aluminium-silicon stripes for VLSI:comparison between MTF and resistometric methods for life predictions. In *Solid State Devices Proceedings*, pages 369–372, September 1987.

[3] D. F. Frost and K. F. Poole. A method for predicting VLSI device reliability using series models for failure mechanisms. *IEEE Transactions on Reliability*, R-36(2) :234–242, 1987.

[4] F.Jeuland et al. Geometry-induced electromigration degradations in aluminium-silicon narrow interconnects. *IEEE VMIC conference*, pages 399–401, 1991.

[5] L. F. Felton, J. A. Schwarz, R. W. Pasco, and D. H. Norbury. Effects of composition and structure on electromigration kinetics in aluminium-alloy thin films. *J.Applied Physics*, 58(2) :723–727, 1985.

[6] Y. Z. Lu and Y. C. Cheng. Measurement technique of electromigration. *Microelectroncs and Reliability*, 23(6) :1103–1118, 1983.

[7] B. J. Root and T. Turner. Wafer level electromigration tests for production monitoring. *Reliability Physics, IEEE Annual Proceedings*, pages 100–107, 1985.

[8] J. R. Black. Electromigration — a brief survey and some recent results. *IEEE Transactions on Electron Devices*, ED-16:338–347, 1969.

[9] M. J. Attardo and R. Rosenberg. Electomigration damage in aluminium film conductors. *J. Applied Physics*, 41(6) :2381–2386, 1970.

[10] A. J. Learn. Evolution and current status of aluminium metallisation. *J. Electrochemical Society(USA)*, 123(6) :894–906, 1976.

[11] P. B. Ghate. Electromigration induced failures in VLSI interconnects. *Reliability Physics, IEEE Annual Proceedings*, pages 292–299, 1982.

[12] Private communications.

[13] L. P. Murray, L. C. Rathbun, and E. D. Wolf. New technique and analysis of accelerated electromigration life testing in multilevel metallisations. *Applied Physics Letters*, 53(15) :1414–1416, 1988.

[14] J. Cho and C. V. Thompson. Grain size dependence of electromigration induced failures in narrow interconnect. *Applied Physics Letters*, 54(25):2577–2579, June 1989.

Chapter 8

Conclusions

8.1 General Remarks

The main objective of the project was to develop a process control test structure and technique to monitor electromigration. The development of a process monitor structure is a challenging task. Although electromigration in thin films has been studied extensively over the past two decades, we have to work under the constraint of a lack of a rigorous theory. It is unlike the situation in bulk metals. Electromigration in thin films is complex because it is strongly influenced by grain structure in thin films and an all-embracing theory has yet to be developed. That is why even today Black's semi-empirical model is commonly used. Electromigration in thin films is also complicated because a large number of material, process and design factors affect electromigration and the interaction amongst them is not always clear. Chapter 2 discusses these issues in detail.

Chapter 3 and 4 highlight electromigration measurement difficulties from a process control point of view. The conventional MTF test has been described as a 'corner stone' in metallisation reliability testing. However, from a process control point of view, 'sample-size' and 'weak-spots' in tracks pose major problems. We may have to use around 400 samples to get an MTF value which is close to the process average. However, experiments carried out with as few as 10 samples showed that it is possible to get consistent results. It should be noted that these samples were invariably screened for any visual defects. However, no experiments were carried out using large sample size, because of project time and cost considerations. Based on this limited experimental work it may be concluded that a

sample size of around 10 seems to work provided the samples are carefully chosen, but it is risky and the risk factor is not easily quantifiable. The measurements also showed that there is a need to maintain uniformity in process parameters to achieve the reliability goal of 10 FITs.

In summary, the studies and measurements described in chapters 2–4 clearly indicated that a new test structure and methodology are required for process monitoring. It should meet the following requirements:

1. The possibility to include the test structure with other process control test structures in a scribe channel or a drop-in die on a wafer. This will enable electromigration experiments to be carried out as part of routine quality assurance tests on all wafers, unlike the conventional package-level tests.

2. Use of resistometry because the mass transport over the entire track caused by electromigration contributes to resistance change. Hence it can be expected that the results obtained from resistometry are better linked to the statistical index, namely, the process capability (C_p).

3. Demonstration of the sensitivity of the methodology to the average linewidth over an area of a wafer.

4. Fast test capability; unlike conventional tests where typical test times may vary from weeks to months.

Chapter 5 describes how and why chequerboards are considered appropriate to monitor electromigration. The success of chequerboards to assess linewidth control has been demonstrated in an earlier PhD project and they offer the possibility to produce micron/sub-micron dimensions close to and even below the typical minimum linewidth specifications. This capability has been further confirmed in this project. Pattern dimension measurements given in chapter 6 and the micrographs of chapter 7 (Figure 7-15) clearly indicate that by using chequerboards we can generate a large number of sub-micron width segments distributed over an area. A small degree of broadening occurs at the corners depending on the quality of

the imaging system and etching. It may be recalled that this is expressed in terms of the quantity ϵ ($\epsilon = 1/2$(segment width on a wafer - segment width on the mask)). The ϵ value of around 0.35 μm derived from chequerboards is nearly constant within a die. This is expected to be a function of the quality of the imaging system because the etch conditions can be considered to be nearly uniform within a die. Thus, this work has shown another interesting possibility: chequerboards can be used for stepper characterization experiments.

From an electromigration point of view the notable features of chequerboards are:

1. The localisation of electromigration damage sites to the overlap areas because of higher current density.

2. In chequerboards, in addition to the heat dissipated by the oxide-wafer-chuck sandwich, a significant quantity of heat is conducted away from the overlap regions by the larger metal squares. It may be recalled that in conventional long tracks the Joule heat generated near the centre of the track has to be dissipated mainly through the oxide-wafer-chuck sandwich.

Current density simulation using PISCES software confirms item (1) above, while item (2) has been confirmed by thermal tracking measurements described in chapter 6 and close monitoring of resistance versus time for a number of chequerboards stressed at high currents and temperatures (chapter 7).

Chapter 6 discusses the chip layout, fabrication and dimensional measurements in detail. Monitoring the temperature profile of a chequerboard during electromigration experiments is one important requirement. Another chequerboard adjacent to the device under test (DUT) is used to monitor the temperature profile. It has been shown later in chapter 7 that this technique works well and the thermal tracking is excellent.

An unintended linewidth offset of 0.2 μm was introduced during mask-making. This meant that the minimum segment width could be greater than 1 μm under normal exposure/etch conditions. Hence it was considered appropriate to use an

effective overetching technique to produce sub-micron geometry segments. Micrographs in Figure 7-15 along with dimensional and resistance measurements show that over-exposure causes a systematic decrease in segment width as expected. Other dimensions such as oxide thickness and metallisation thickness have also been measured as part of general integrity tests and the variations reported in chapter 6 are quite typical of any well maintained IC fabrication facility.

The electromigration measurements and test results given in chapter 7 indicate that chequerboards can be used to monitor electromigration for metallisation process control. The overall performance of chequerboards to monitor electromigration are now summarised.

Chequerboard test structures having a segment width nearly equal to the minimum specified linewidth may easily be included with other process control test structures in scribe channels or in drop-in die on wafers. This is possible because all the chequerboards have been designed to conform to a standard probe pad layout requirements with a pad spacing of 120μm. It may be recalled that resistometry with self-heating was used for routine process monitoring because it does not require external heating to increase temperature to accelerate the failure process. The extracted parameter m from the resistance versus time curve can be used to monitor the average electromigration performance.

The activation energy of 0.5 eV derived from chequerboard methodology is typical of the value published in the literature for electromigration in aluminium-silicon alloy films (0.4—0.8 eV).

A key process parameter, namely, linewidth has been chosen to demonstrate the sensitivity of the proposed methodology to monitor electromigration. Even though only one parameter was chosen, the measurements and tests consumed a major portion of this work. The salient features of this task involved:

- A detailed study of the various factors affecting linewidth control

- Extensive SEM measurements using chequerboard segments to derive the

small degree of broadening that occurs at the corners due to the resolution limits of the optical system.

- Generation of sub-micron geometry segments using an effective overetching technique.

- Resistometry with self-heating and the more common method of package level tests.

Based on the above studies the critical width was determined, thus demonstrating the sensitivity of chequerboards to average linewidth.

As regards the fast test time capability, although the typical stress levels (current and temperature) used in the present work correspond to a breakdown time of about an hour, it is to be noted that the acceleration factor is still very high (calculated and shown below) compared to the general specification of about 20 years lifetime under normal operating conditions. It may be noted that the breakdown time chosen is about 5 to 6 times the typical thermal stabilization time. When breakdown time is 1 hour,

$$\text{Acceleration Factor} = \frac{20\text{years}}{1\text{hour}} = 175200$$

Further study is required to use higher acceleration factors and this aspect is discussed in the next section on suggestions for further work.

8.2 Suggestions for Further Work

One important limitation which has become clear by fast tests is the need to study the thermal aspects of chequerboards before thermal equilibrium is established. When the stress (current and temperature) conditions are such that the breakdown times are about few seconds, inconsistent results have been obtained. In this short duration, when test durations are significantly smaller than the thermal stabilization time, temperature may vary significantly across the chequerboard.

Thus even when same current is used, failure times may vary considerably from sample to sample depending upon the 'thermal signature' of the chequerboard. The approximation of a uniform temperature across the entire chequerboard may not be valid. Computer simulations of thermal profile and temperature rise as a function of time in chequerboards may deepen our understanding in this area. This is expected to be an interesting subject for another PhD. The thesis cited in reference [1] may provide some useful hints as to how to analyse this complicated problem.

As chequerboards provide a new insight into electromigration measurements which correlate to average process parameters, it is obvious that one can use this methodology to study the effect of all the major parameters affecting electromigration which are described in chapter 2. No doubt, this will generate a great deal of information and further enhance our understanding of electromigration. Of special interest will be the study of the effects of the microstructure on MTF. This interesting area had to be left out in the present work because of sample preparation difficulties with TEM. However, new techniques such as focussed ion beam microscopy are now available and they do not need any specialised sample preparation [2]. This technique can be used to determine grain size distribution in aluminium films at any point on a die or wafer relatively easily and hence is being used for metallisation process control [2]. In this technique the sample surface is imaged with ion beam generated secondary electrons in a manner analogous to the operation of an SEM.

It may be recalled that an additional objective of the project was to make some statistical estimations of the MTF of small segments. Sample calculation has been carried out and is generally in agreement with similar estimations that have been reported. However, the electromigration test chip contains a number of chequerboards with a wide range of rows and columns and further statistical analysis should improve our understanding in the emerging area of circuit level reliability estimation. For example, study of the variation of chequerboard MTF with n_s and n_p, the number of serial and parallel elements respectively.

In summary, a starting point for a radically new way of thinking in test struc-

ture design and test methodology to monitor electromigration has been shown. Further experimental and theoretical work is needed to deepen the understanding of the issues introduced here.

Bibliography

[1] J.C.Rouais. *Role des heterogeneities locales de temperature dans la rupture des couches minces d'or par electromigration.* PhD thesis, Institut National des Sciences Appliquees, Lyon, 1976.

[2] Dipankar Pramanik and Jay Glanville. Aluminium film analysis with the focused ion beam microscopy. *Solid State Technology*, (5):77–80, 1990.

Appendix A

Process Run-Sheet

EDINBURGH MICROFABRICATION FACILITY

ELECTROMIGRATION EXPERIMENT

BATCH NUMBER: 91034 START DATE: 30 MAY 1991

DEVICE IDENTIFICATION: **EU 9101, EU9102**

MASK SET:SERCB 247

MASKING SEQUENCE: 1

MASK REV.LETTERS: A

STARTING MATERIAL: 14-20 ohm-cm(100) p-type,3inch diameter

STEP 1 FURNACE 9 WOXHCL11 10minutes

Start date: Start Time Initials

Furnace 1950°C,idling on oxygen

Preset gas flows as follows:

Nitrogen 20% (1.5 litres/minute)

Oxygen 20% (1.5 litres/minute)

HCI 15% (0.15 litres/minute)

Hydrogen 10% (1.7 litres/minute)

Load wafers into furnace with Oxygen only flowing:

5 minutes Oxygen + HCl

10 minutes Oxygen +HCl + Hydrogen

5minutes Oxygen

Measure oxide thickness:

Finish date: Finish time: Initials

STEP II. SPUTTERING

Start Date: Start time Initials:

Load wafers on palettes and load into Balzers BAS 450 coater.

Pump system to 5×10^{-6} Torr better with Meissner trap.

Close shutter.

Throttle pump and admit argon at 2×10^{-3} Torr.

Set integrator at 3500. Range 3.

Run up Aluminium/Silicon target to 6KW.

Open shutter until integrator times out.

Warm up Meissner and chamber.

Vent system and remove wafers.

Finish date: Finish time: Initials.

STEP III PHOTO(POSITIVE RESIST)

NOTE: Wafers 5 and 10 EXPOSURE RUN 600 milliseconds to 1360 milliseconds in 20 milliseconds steps

Start date: Start time: Initials:

HMDS vapour box prime for 30 minutes

Spin HPR 204 at 4500 rpm for 30 seconds

Hotplate bake at 105°C for 60 seconds

Align and expose.

Inspect for proper development

Measure resist image: microns

Hot plate bake at 130°C for 60 minutes

Inspect for proper baking

Finish date: Finish time: Initials:

STEP IV. ALUMINIUM RIE ETCH

Start date: Start time: Initials

RIE etch to in CC14(10cc/min) pressure 40×10^{-3}Torr

Power 750 Watt for 2 minutes + 500 Watt to clear

Finish Date: Finish Time: Initials:

STEP V. RESIST STRIP

Start date: Start time: Initials

Oxygen plasma ash 30 minutes

Immerse in Fuming Nitric Acid for 10 minutes

Wash and spin dry

Inspect for removal of resist

Measure etched image: microns

Finish date: Finish time: Initials

STEP VI. FURNACE(ANNEAL)

430°C, idling on Nitrogen

preset gas flows as follows:

Nitrogen 50 (2.0 litres/minute)

Nitrogen/40

Finish date: Finish time: Initials

5 minutes Nitrogen

10 minutes Nitrogen/Hydrogen

5 minutes Nitrogen

Finish date: Finish time: Initials

Appendix B

HP-BASIC Program Listing

```
10    ! XXXXXXXXXXXXXXXXXXXXXXXXX
20    !XXXXXXXXXXXXXXXXXXXXXXXXXX
30    ! COMPUTERISED TEST SET FOR
40    ! MONITORING ELECTROMIGRATION
60    ! M.RAVINDRA  1991
70    !XXXXXXXXXXXXXXXXXXXXXXXXXX
80    PRINT TABXY(22,8);"XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX"
90    PRINT TABXY(25,10);"  ELECTROMIGRATION TESTS "
100   PRINT TABXY(22,12);"XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX"
110   WAIT 1
120   CLEAR SCREEN
130   INPUT "WAIT TIME",W
140   !.............................
150   COM INTEGER Istart,W
160   COM /Name/ File1$[10],File2$[10],@Way1,@Way2
170   Istart=0
180   CLEAR SCREEN
190   PRINT TABXY(17,2);"SELECT CHOICE FROM MENU USING SOFTKEYS"
200   PRINT TABXY(24,4);"1: TCR"
210   PRINT TABXY(24,7);"2: BREAK DOWN"
220   PRINT TABXY(24,10);"3: EMT"
230   PRINT TABXY(24,13);"4: QUIT"
240   !
250   ON KEY 1 LABEL "TCR" CALL Tcr
260   ON KEY 2 LABEL "BRD(N/A)" CALL Nu
270   ON KEY 3 LABEL "EMT" CALL Emi
280   ON KEY 4 LABEL "QUIT" GOTO 294
281   ON KEY 5 LABEL "NU" CALL Nu
282   ON KEY 6 LABEL "NU" CALL Nu
283   ON KEY 7 LABEL "NU" CALL Nu
284   ON KEY 8 LABEL "NU" CALL Nu
285   GOTO 285
294    CLEAR SCREEN
304    END
320   !XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
330   SUB Emi
340    COM INTEGER Istart,W
350    CALL Createfile(150)
360    !HP6633 SETTINGS TO  FORCE
370    !REQUIRED CURRENT DENSITY
380    INPUT "ENTER VSET",Vset
390    C$="VSET"
400    P$=VAL$(Vset)
410    Q$=C$&" "&P$
420    OUTPUT 705;Q$
430    OUTPUT 705;"VOUT?"
440    ENTER 705;Vout
450    PRINT Vout
460    INPUT "ENTER ISET",Iset
470    C1$="ISET"
480    P1$=VAL$(Iset)
490    Q1$=C1$&" "&P1$
500    OUTPUT 705;Q1$
510    OUTPUT 705;"IOUT?"
520    ENTER 705;Iout
530    PRINT Iout
540    CLEAR SCREEN
```

```
550     REPEAT
560               CALL Measure
570               WAIT W
580       UNTIL Iout<.00001
590       SUBEND
600     !XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
610     SUB Measure
620     COM INTEGER Istart,W
630     COM /Name/ File1$,File2$,@Way1,@Way2
640     DIM V1@(500),V11(500),V3(500) ! 500 READINGS FOR 250s
650     DIM V4(500),V5(500),V6(500) ! MORE THAN 4HRS TESTING
660     DIM V7(500),V8(500),V9(500),V100(500)
670     !HP SCANNER + DMM USED TO MONITOR VOLTAGES
680     I=Istart
690     OUTPUT 709;"DCL" !OPEN ALL CHANNELS UNCONDITIONALLY
700     OUTPUT 709;"1@E" !CLOSE CHANNEL 1@
710     OUTPUT 722;"F1  R7" ! DC VOLTS, AUTO RANGE
711     WAIT .1
720     ENTER 722;V1@(I)
730     WAIT .1
740     OUTPUT 709;"C" !OPEN ALL CHANNELS
750     OUTPUT 709;"@1E"
760     OUTPUT 722;"F1  R7"
761     WAIT .1
770     ENTER 722;V11(I)
780     OUTPUT 709;"C"
800     OUTPUT 709;"11E" ! CLOSE CH. 11
810     OUTPUT 722;"F1  R7"
811     WAIT .1
820     ENTER 722;V3(I)
840     OUTPUT 709;"C"
850     OUTPUT 709;"@3E"
860     OUTPUT 722;"F1  R7"
861     WAIT .1
870     ENTER 722;V4(I)
890     OUTPUT 709;"C"
900     OUTPUT 709;"@4E"
910     OUTPUT 722;"F1  R7"
920     ENTER 722;V5(I)
930     WAIT .1
940     OUTPUT 709;"C"
950     OUTPUT 709;"@5E"
960     OUTPUT 722;"F1  R7"
961     WAIT .1
970     ENTER 722;V6(I)
990     OUTPUT 709;"C"
1000    OUTPUT 709;"@6E"
1010    OUTPUT 722;"F1  R7"
1011    WAIT .1
1020    ENTER 722;V7(I)
1040    OUTPUT 709;"C"
1050    OUTPUT 709;"@7E"
1060    OUTPUT 722;"F1  R7"
1061    WAIT .1
```

```
1070   ENTER 722;V8(I)
1090   OUTPUT 705;"C"
1100   OUTPUT 705;"05E"
1110   OUTPUT 722;"F1  R7"
1111   WAIT .1
1120   ENTER 722;V9(I)
1140   OUTPUT 705;"C"
1150   OUTPUT 705;"05E"
1160   OUTPUT 722;"F1  R7"
1161   WAIT .1
1170   ENTER 722;V100(I)
1180   !
1200   DIM A$[90]
1210   OUTPUT A$ USING "#,XXX,DDDD,SDD.6D,SDD.6D,SDD.6D,SDD.6D,SDD.6D";I,V10(I),
V11(I),V3(I),V4(I),V5(I)
1220   OUTPUT @Way1;A$
1230   PRINT A$
1240   DIM B$[90]
1250   OUTPUT B$ USING "#,XXX,DDDD,SDD.6D,SDD.6D,SDD.6D,SDD.6D,SDD.6D";I,V6(I),V
7(I),V8(I),V9(I),V100(I)
1251   PRINT B$
1260   OUTPUT @Way2;B$
1270   Istart=Istart+1
1280   SUBEND
1290   !XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
1300   SUB Breakdown
1310   SUBEND
1320   SUB Createfile(Block)
1330   COM /Name/ File1$,File2$,@Way1,@Way2
1340   PRINT "FILENAME IN THE FORMAT WN_DNX_UU"
1350   PRINT "EX: 06_15L_01"
1360   INPUT File$
1370   File1$=File$&"A"
1380   File2$=File$&"B"
1390   CREATE ASCII File1$,Block
1400   CREATE ASCII File2$,Block
1410   ASSIGN @Way1 TO File1$
1420   ASSIGN @Way2 TO File2$
1430   SUBEND
1440   !XXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
1450   SUB Ter
1460   F=0
1470   COM /Tergroup/ Ter$[10],@Path
1480   INPUT "ENTER VSET",Vset
1490   C2$="VSET"
1500   P2$=VAL$(Vset)
1510   Q2$=C2$&" "&P2$
1520   OUTPUT 705;Q2$
1530   INPUT "ENTER ISET",Iset
1540   C3$="ISET"
1550   P3$=VAL$(Iset)
1560   Q3$=C3$&" "&P3$
1570   OUTPUT 705;Q3$
1580   OUTPUT 705;"IOUT?"
```

```
1590   ENTER 705;Tout
1600   INPUT "TEMPERATURE?",Temp
1610   !..............
1620   CALL Tcrfile(20)
1630   !.............
1640   DIM V10(10),V11(10),V3(10),V4(10),V5(10)
1650   DIM V6(10),V7(10),V8(10),V9(10),V100(10)
1660   OUTPUT 705;"DCL"
1670   OUTPUT 705;"10E"
1680   OUTPUT 722;"F1   R7"
1681   WAIT 1
1690   ENTER 722;V10(P)
1691   PRINT V10(P)
1710   OUTPUT 705;"C"
1720   OUTPUT 705;"01E"
1730   OUTPUT 722;"F1   R7"
1731   WAIT .1
1740   ENTER 722;V11(P)
1741   PRINT V11(P)
1760   OUTPUT 705;"C"
1770   OUTPUT 705;"11E"
1780   OUTPUT 722;"F1   R7"
1781   WAIT .1
1790   ENTER 722;V3(P)
1791   PRINT V3(P)
1810   OUTPUT 705;"C"
1820   OUTPUT 705;"03E"
1830   OUTPUT 722;"F1   R7"
1831   WAIT .1
1840   ENTER 722;V4(P)
1860   OUTPUT 705;"C"
1870   OUTPUT 705;"04E"
1880   OUTPUT 722;"F1   R7"
1881   WAIT .1
1890   ENTER 722;V5(P)
1910   OUTPUT 705;"C"
1920   OUTPUT 705;"05E"
1930   OUTPUT 722;"F1   R7"
1931   WAIT .1
1940   ENTER 722;V6(P)
1950   OUTPUT 705;"C"
1960   OUTPUT 705;"06E"
1970   OUTPUT 722;"F1   R7"
1971   WAIT .1
1980   ENTER 722;V7(P)
2000   OUTPUT 705;"C"
2010   OUTPUT 705;"07E"
2020   OUTPUT 722;"F1   R7"
2021   WAIT .1
2030   ENTER 722;V8(P)
2050   OUTPUT 705;"C"
2060   OUTPUT 705;"08E"
2070   OUTPUT 722;"F1   R7"
2071   WAIT .1
2080   ENTER 722;V9(P)
2100   OUTPUT 705;"C"
2110   OUTPUT 705;"09E"
2120   OUTPUT 722;"F1   R7"
2121   WAIT .1
```

```
130   ENTER 722;V100(*)
150   !.........................
160   DIM Title1$[50]
170   DIM Title2$[50]
180   DIM Title3$[50]
190   DIM N1$[80]
200   DIM N2$[80]
210   DIM N3$[80]
220   CLEAR SCREEN
230   Title1$="DEVICE ID  "&Ter$
240   Title2$="TEMPERATURE(C)  "&VAL$(Temp)
250   Title3$="CURRENT(A):  "&VAL$(Iout)
260   OUTPUT N1$ USING "#,10X, 30A";Title1$
270   OUTPUT N2$ USING "#,10X, 30A";Title2$
280   OUTPUT N3$ USING "#,10X, 30A";Title3$
290   PRINT N1$
300   PRINT N2$
310   PRINT N3$
320   DIM M1$[80],M2$[80],M3$[80],M4$[80],M5$[80]
330   DIM M6$[80],M7$[80],M8$[80],M9$[80],M10$[80]
340   OUTPUT M1$ USING "#,DD,SDD.6D,SDD.6D,SDD.6D";1,V10(P),V10(P)-V11(P),(V10(
)-V11(P))/Iout
350   OUTPUT M2$ USING "#,DD,SDD.6D,SDD.6D,SDD.6D";2,V11(P),V11(P)-V3(P),(V11(P
-V3(P))/Iout
360   OUTPUT M3$ USING "#,DD,SDD.6D,SDD.6D,SDD.6D";3,V3(P),V3(P)-V4(P),(V3(P)-V
(P))/Iout
370   OUTPUT M4$ USING "#,DD,SDD.6D,SDD.6D,SDD.6D";4,V4(P),V4(P)-V5(P),(V4(P)-V
(P))/Iout"
380   OUTPUT M5$ USING "#,DD,SDD.6D,SDD.6D,SDD.6D";5,V5(P),V5(P)-V6(P),(V5(P)-V
(P))/Iout
390   OUTPUT M6$ USING "#,DD,SDD.6D,SDD.6D,SDD.6D";6,V6(P),V6(P)-V7(P),(V6(P)-V
(P))/Iout
400   OUTPUT M7$ USING "#,DD,SDD.6D,SDD.6D,SDD.6D";7,V7(P),V7(P)-V8(P),(V7(P)-V
(P))/Iout
410   OUTPUT M8$ USING "#,DD,SDD.6D,SDD.6D,SDD.6D";8,V8(P),V8(P)-V9(P),(V8(P)-V
(P))/Iout
420   OUTPUT M9$ USING "#,DD,SDD.6D,SDD.6D,SDD.6D";9,V9(P),V9(P)-V100(P),(V9(P)
-V100(P))/Iout
430   PRINT M1$
440   PRINT M2$
450   PRINT M3$
460   PRINT M4$
470   PRINT M5$
480   PRINT M6$
490   PRINT M7$
500   PRINT M8$
510   PRINT M9$
530   OUTPUT @Path1;N1$
540   OUTPUT @Path1;N2$
550   OUTPUT @Path1;N3$
560   OUTPUT @Path1;" "
570   OUTPUT @Path1;M1$
580   OUTPUT @Path1;M2$
590   OUTPUT @Path1;M3$
600   OUTPUT @Path1;M4$
610   OUTPUT @Path1;M5$
620   OUTPUT @Path1;M6$
630   OUTPUT @Path1;M7$
640   OUTPUT @Path1;M8$
```

```
2650   OUTPUT @Path;M$$
2660   SUBEND
2670   !XXXXXXXXXXXXXXX
2680   SUB Terfile(Block)
2690   COM /Tergroup/ Ter$,@Path
2700   PRINT "INPUT FILENAME"
2710   PRINT "ID FORMAT: @@18L100"
2720   INPUT Ter$
2730   CREATE ASCII Ter$,Block
2740   ASSIGN @Path TO Ter$
2750   SUBEND
2760   !XXXXXXXXXXXX
2770   SUB Nu
2780   BEEP
2800   SUBEND
```

Appendix C

Mathematics of Failure Distributions

The term reliability has many popular connotation. However, from mathematical point of view, it is usually defined as : "Probability that an item will perform a required function under stated conditions for a stated period of time." The required function includes definition of failure which may vary from application to application. However, failures could be broadly classified into degradation failures and catastrophic failures as explained in chapter 1. The stated conditions in the definition comprise of the total physical environment, including the mechanical, thermal, and electrical conditions of expected use. For example, burn-in at 150°C ; centrifugal spinning at 20,000g etc. The stated period of time is the time during which satisfactory operation is required. This includes the concept of lifetime. This will vary depending upon the usage of the system. In some cases, the time can be relatively short, as in the case of an emergency beacon transmitter or an air- craft or the component has to perform throughout the target mission life as in the case of a satellite. The next sections present the basic reliability concepts in terms of mathematical functions. For further details refer to references [1,2,3, 4].

C.1 Quantifying Reliability

C.1.1 Cumulative Distribution Function

Assume that a device is operating at time t=0. The probability that the device will fail at or before time t is given by the function F(t). This is a cumulative distribution function (CDF) with the properties

$$F(t) = 0 \qquad t < 0 \tag{C.1}$$

$$0 \leq F(t) \leq F(t') \qquad 0 \leq t \leq t' \tag{C.2}$$

$$F(t) \to 1 \qquad t \to \infty \tag{C.3}$$

F(t)=percentage of failures at time t

C.1.2 Reliability Function

The reliability function R(t) is the probability that the device will survive to time t without failure. The function is related to F(t), and is given by

$$R(t) = 1 - F(t) \tag{C.4}$$

R(t)=percentage of good devices at time t

C.1.3 Probability Density Function

The derivative of F(t) with respect to time is known as the probability density function (PDF) and is represented by f(t).
i.e,

$$f(t) = \frac{d}{dt}F(t) \tag{C.5}$$

or

$$F(t) = \int_0^t f(x)dx \tag{C.6}$$

From the above equations it follows that,

$$\begin{aligned} R(t) &= 1 - F(t) && \text{(C.7)} \\ &= \int_0^\infty f(x)dx - \int_0^t f(x)dx && \text{(C.8)} \\ &= \int_t^\infty f(x)dx && \text{(C.9)} \end{aligned}$$

and

$$f(t) = -\frac{d}{dt}R(t) \tag{C.10}$$

C.1.4 Failure rate

The instantaneous failure rate $\lambda(t)$, defined as the ratio of (fraction of failures in a time period (t, t+ δ t) of those units that were good at the beginning of this period) to (the time interval δ t),
can be expressed in terms of f(t), F(t) and R(t) as shown below:

$$\lambda(t) = \lim_{\delta t \to 0} \frac{F(t+\delta t) - F(t)}{R(t) \times \delta t} \tag{C.11}$$

$$= \lim_{\delta t \to 0} \frac{1}{\delta t} \frac{R(t) - R(t+\delta t)}{R(t)} \tag{C.12}$$

$$= \frac{-1}{R(t)} \frac{d}{dt} R(t) \tag{C.13}$$

$$= \frac{f(t)}{R(t)} \tag{C.14}$$

$$= \frac{f(t)}{1 - F(t)} \tag{C.15}$$

C.2 Common Distribution Functions

C.2.1 Exponential Distribution Function

The exponential distribution is characterized by a constant failure rate over the lifetime of the device. This function is useful in representing a device in its working-life or useful-life period. The exponential distribution is characterized by the following functions

$$\lambda(t) = \lambda_0 = constant \tag{C.16}$$

$$R(t) = exp(-\lambda_0 t) \tag{C.17}$$

$$F(t) = 1 - exp(-\lambda_0 t) \tag{C.18}$$

$$f(t) = \lambda_0 exp(-\lambda_0 t) \tag{C.19}$$

Some of these functions are shown in Figure C–1

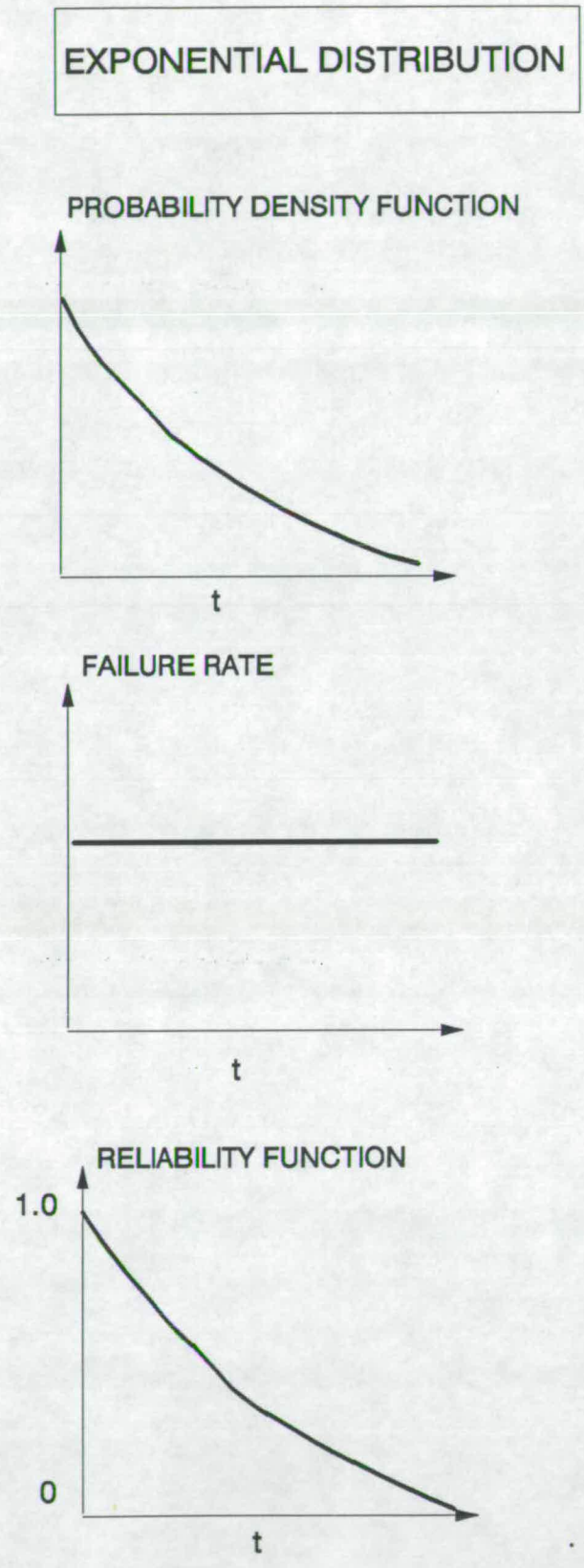


Figure C–1: Probability density function, failure rate and reliabilty function of exponential distribution

C.2.2 Normal Distribution Function

The PDF, CDF and λ(T) are given by

$$\text{PDF} = \text{f(t)} = \frac{\exp\left[\frac{-(\text{t}-\mu)^2}{2\sigma^2}\right]}{\sigma\sqrt{2\pi}} \tag{C.20}$$

$$\text{CDF} = \text{F(t)} = \frac{1}{\sigma\sqrt{2\pi}} \int_0^{\text{t}} \exp\left[-\frac{(\text{t}-\mu)^2}{2\sigma^2}\right] \text{dt} \tag{C.21}$$

$$\lambda(\text{t}) = \frac{\text{f(t)}}{1-\text{F(t)}} = \frac{\exp\left[\frac{-(\text{t}-\mu)^2}{2\sigma^2}\right]}{\int_{\text{t}}^{\infty} \exp\left[-\frac{(\text{t}-\mu)^2}{2\sigma^2}\right] \text{dt}} \tag{C.22}$$

where μ is the mean or median of the normal distribution. It may be noted that for normal distribution mean and median coincide.

Some of these functions are shown in Figure C–2

Normalization of normal distribution

It may be noted that if we consider t to represent a general normal variable in which case negative t is also meaningful, The CDF can be expressed as:

$$F(t) = \frac{1}{\sigma\sqrt{2\pi}} \int_{-\infty}^{t} exp\left[-\frac{(t-\mu)^2}{2\sigma^2}\right] dt \tag{C.23}$$

Normal curves can be normalized to yield linear plots of the CDF using the following substitution :

$$\text{z} = \frac{\text{t}-\mu}{\sigma}$$

The CDF F(t) can be expressed in terms of the function ϕ(z) given by:

$$F(t) = \phi(z) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{z} exp(-z^2/2) dz \tag{C.24}$$

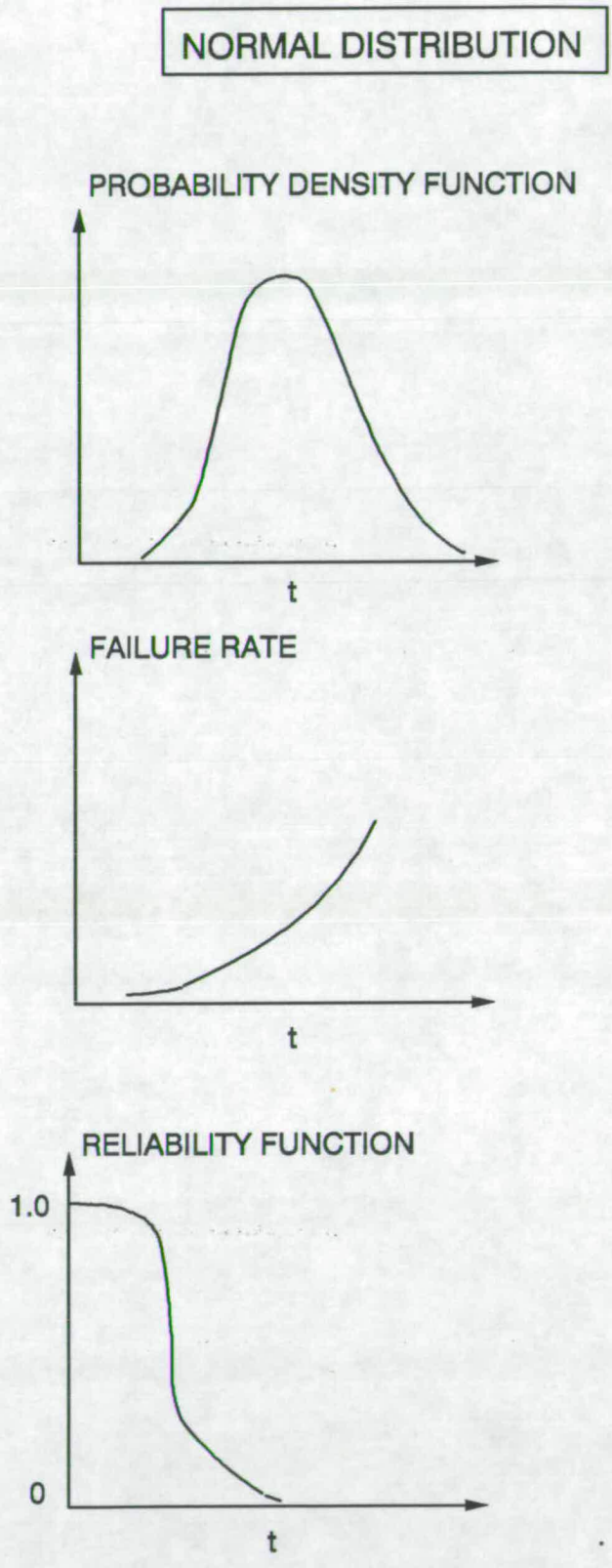


Figure C–2: Probability density function, failure rate and reliability function of normal distribution

$\phi(z)$ cannot be expressed analytically. But it is generally tabulated in statistical tables, and can be evaluated by approximated expressions.

The equation,

$$z = (\frac{1}{\sigma})(t - \mu)$$

gives a straight line with slope $\frac{1}{\sigma}$ and intercept μ. Plots of z versus t and $\phi(z)$ versus t are shown in Figure C–3

C.2.3 Lognormal Distribution

The PDF, CDF and $\lambda(t)$ are given by:

$$\text{PDF} = f(t) = \frac{\exp\left[\frac{-(\ln t - \ln t_{50})^2}{2\sigma^2}\right]}{\sigma t\sqrt{2\pi}} \tag{C.25}$$

$$\text{CDF} = F(t) = \frac{1}{\sigma\sqrt{2\pi}} \int_0^t \frac{1}{t} \exp\left[-\frac{(\ln t - \ln t_{50})^2}{2\sigma^2}\right] dt \tag{C.26}$$

$$\lambda(t) = \frac{\exp\left[\frac{-(\ln t - \ln t_{50})^2}{2\sigma^2}\right]}{t \int_t^\infty \frac{1}{t} \exp\left[-\frac{(\ln t - \ln t_{50})^2}{2\sigma^2}\right] dt} \tag{C.27}$$

where t_{50} is the median time to failure. Some of these functions are shown in Figure C–4

The lognormal distribution may represent the early life, the useful life or the wear out period of a device. It can be used to represent the increasing and decreasing failure rates as opposed to just increasing failure rate of a normal distribution.

Normalization of lognormal distribution

Linear plots can be obtained by the substitution,

$$z = \frac{\ln t - \mu}{\sigma}$$

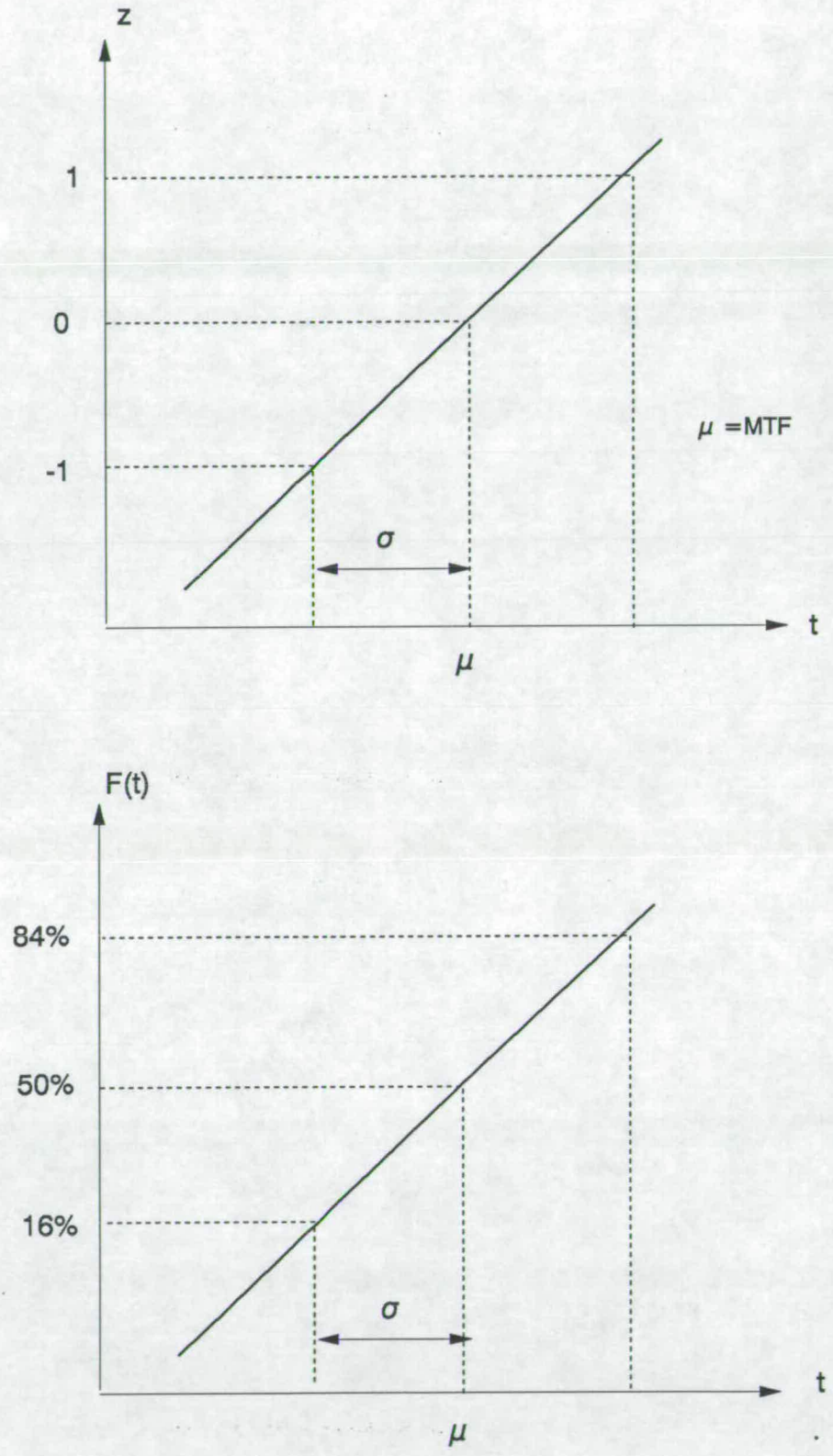


Figure C–3: Normalized variable and CDF versus time of the normalized normal distribution

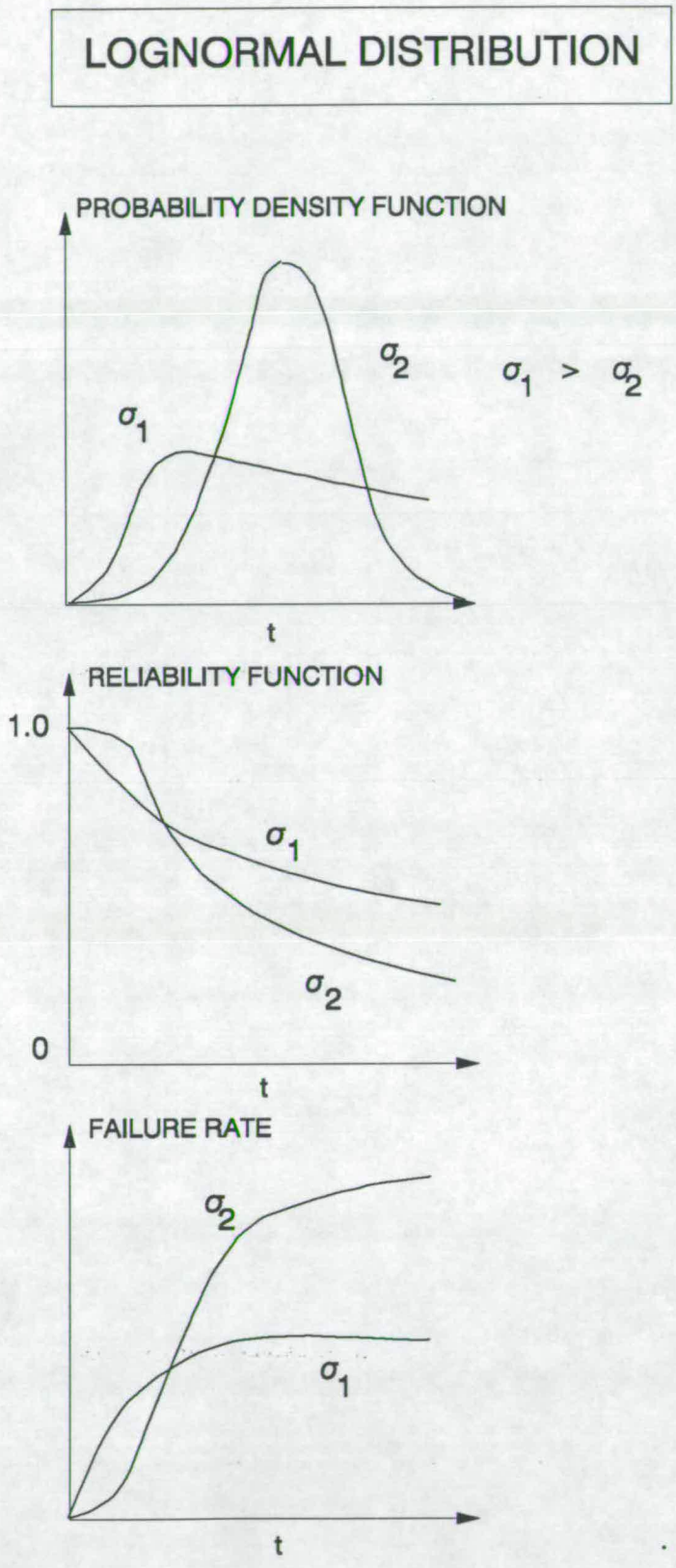


Figure C–4: Probability density function, failure rate and reliability function of lognormal distribution

Now F(t) can be expressed as

$$F(t) = F_z(z) = \frac{1}{\sqrt{2\pi}} \int_{\infty}^{z} \exp(-z^2/2)dz$$

The plots of z and F(t) versus $\ln t$ are shown in Figure C–5

C.2.4 Weibull distribution

The Weibull distribution function is characterized by the following functions:

$$f(t) = \frac{b}{a} t^{b-1} exp(-\frac{1}{a} t^b) \quad \text{(C.28)}$$

$$F(t) = 1 - exp(-\frac{1}{a} t^b) \quad \text{(C.29)}$$

$$R(t) = exp(-\frac{1}{a} t^b) \quad \text{(C.30)}$$

$$\lambda(t) = \frac{b}{a} t^{b-1} \quad \text{(C.31)}$$

Figure C–6 shows the plot of some of these functions. In some applications of the Weibull distribution function, the time t is replaced by t_γ where γ corresponds to some portion of the life of the device that has been used up (for example, burn-in). When b=1, Weibull reduces to the exponential distribution function. If $b < 1$, the failure rate decreases with time and if $b > 1$, the failure rate increases with time, representing the early life and wear-out regions respectively.

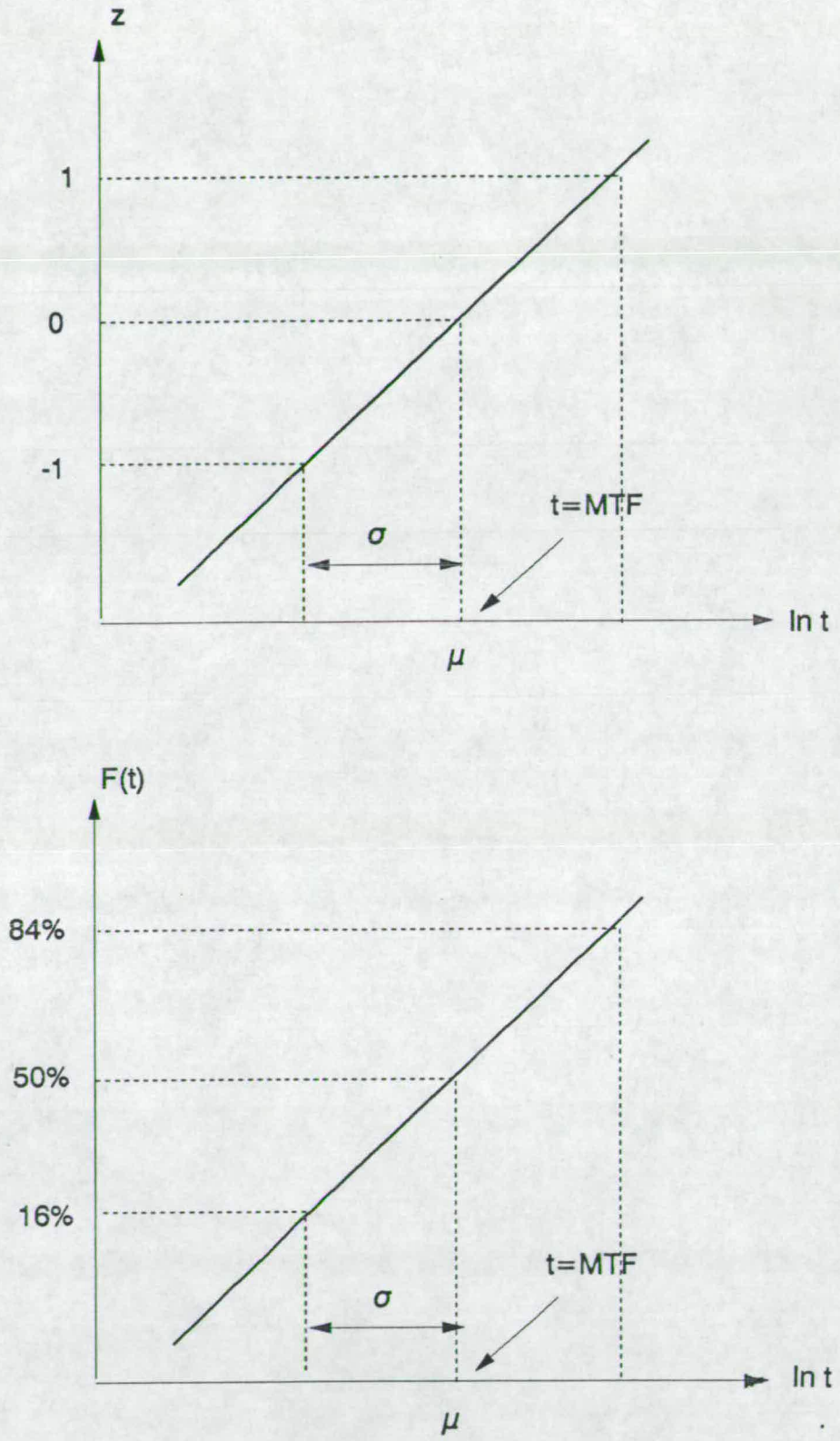


Figure C–5: Normalized variable and CDF of the normalized lognormal distribution

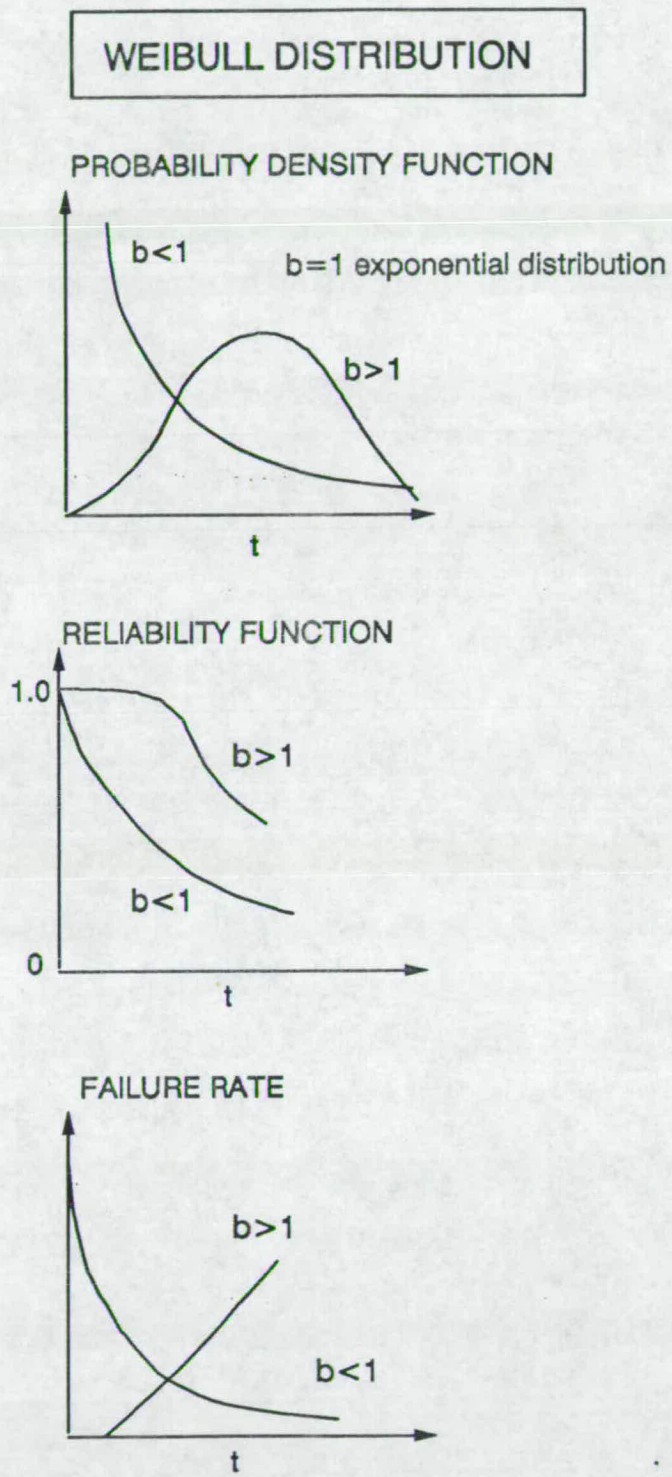


Figure C–6: Probability density function, failure rate and reliability function of Weibull distribution

Appendix D

Electromigration MTF Estimations for Series-Parallel Elements

In this appendix the equation used in estimating MTF of a single element (equation 7.9, chapter 7) is derived. The concepts and methodology described here are taken from the references [5,6,7].

Let, n_s and n_p represent the number of serial and parallel elements of a test structure subjected to electromigration stress experiments. The PDF, CDF etc. of the elements are denoted by the same notations as used prevoiusly in appendix A, section A.2.3 to describe lognormal distribution and are reproduced below for easy reference. Lognormal distribution has been used because it is the commonly used distribution to describe electromigration failures.

$f(t)$ = Probability density function (PDF)
$F(t)$ = Cumulative distribution function (CDF)
t_{50} = MTF
$\mu_0 = \ln t_{50}$
σ_0 = standard deviation of the lognormal distribution

The CDF of the series-parallel system, $G(t)$, is given by [6],

$$G(t) = 1 - [1 - F(t)^{n_p}]^{n_s} \tag{D.1}$$

Let, t_{50sp} = MTF of the series-parallel system, Then by definition of MTF,

$$G(t_{50sp}) = \frac{1}{2} \tag{D.2}$$

or

$$\int_0^{t_{50sp}} g_{sp}(t) = \frac{1}{2} \tag{D.3}$$

where $g_{sp}(t)$ is the PDF of the series-parallel system. Equation D.3 follows from equation B.2 by noting that PDF is the derivative of CDF.

From equations D.1, D.2, D.3 and noting that $F(0) = 0$, we get,

$$1 - [1 - F(t)^{n_p}]^{n_s} \Big|_{\text{at } t=t_{50sp}} \textbf{ minus } 1 - [1 - F(t)^{n_p}]^{n_s} \Big|_{\text{at } t=0} = \frac{1}{2} \tag{D.4}$$

i.e,

$$1 - [1 - F(t_{50sp})^{n_p}]^{n_s} = \frac{1}{2} \tag{D.5}$$

i.e,

$$1 - F(t_{50sp})^{n_p} = \left(\frac{1}{2}\right)^{\frac{1}{n_s}} \tag{D.6}$$

i.e,

$$F(t_{50sp}) = \left[1 - \left(\frac{1}{2}\right)^{\frac{1}{n_s}}\right]^{\frac{1}{n_p}} \tag{D.7}$$

by defining the normalized variable ϕ with the equation:

$$\phi = \frac{\ln t_{50sp} - \mu_0}{\sigma_0} \tag{D.8}$$

the CDF at $t = t_{50sp}$ in equation D.7 can be expressed as (see section A.2.3 of appendix A),

$$F(t_{50sp}) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\phi} \exp(-z^2/2)dz \tag{D.9}$$

where z is a dummy variable. Equation D.8 may be rearranged to get,

$$\ln t_{50sp} = \mu_0 + \sigma_0 \phi \tag{D.10}$$

Appendix E

Thermal Time Constants

E.1 Thermal Resistance and Thermal Capacity

In the steady state, the rate of heat transfer by conduction in the monodimensional case can be expressed as:

$$q = kA\frac{\triangle T}{\triangle x} = \frac{\triangle T}{R_{th}} \tag{E.1}$$

where,

q = rate of heat transfer

R_{th} = thermal resistance

k = thermal conductivity of the material

A = area of cross section

$\triangle T$ = temperature difference between two points distant $\triangle x$.

However, it may be noted that for ICs the thermal resistance is usually expressed as:

$$R_{th} = \frac{\triangle T_j}{P}$$

Where,

$$\triangle T_j = T_A + T_j$$

Where, T_A is the ambient temperature, T_j is the junction temperature and P is the applied power. For a ceramic 16 pin DIP packaged IC the thermal resistance is typically in the range 110 –140 °C/W.

The thermal capacity C_{th} is defined and given by,

$$C_{th} = \frac{\triangle h}{\triangle T} = \frac{ms \triangle T}{\triangle T} = ms \tag{E.2}$$

where, $\triangle h$ is the amount of heat required to rise the temperature of m grams of a substance through $\triangle T$ and s is the specific heat.

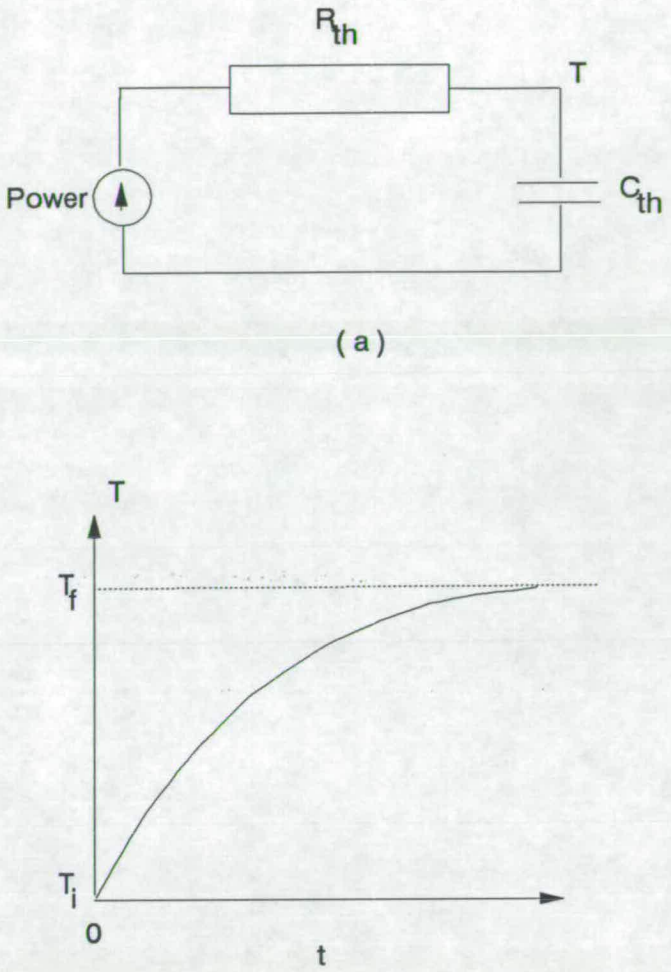


Figure E–1: Thermal equivalent circuit (a) and the thermal response for a pulse (b)

E.2 Thermal Time Constant

Let R_{th} and C_{th} be the thermal resistance and thermal capacity respectively of a system whose thermal equivalent circuit is shown in Figure E–1 (a). Figure E–1 (b) shows the expected temperature rise as a function of time when a heat pulse is applied. The temperature rise can be mathematically expressed as:

$$T = T_i + (T_f - T_i)[1 - \exp(-t/\tau)] \tag{E.3}$$

where, $\tau = R_{th}C_{th}$ is the thermal time constant and, $T = T_i$ at $t = 0$ and $T \rightarrow T_f$ as $t \rightarrow \infty$.

E.3 Equivalent Thermal Circuit for the Metal-Oxide-Silicon-Chuck Sandwich

It may be recalled that the chequerboard test structures are fabricated by sputter depositing aluminium-silicon on an oxidised silicon wafer. Also, the electromigration experiments are carried out by probe-testing the wafers whilst held by a vacuum-chuck.

A simplified model which can be used to describe the dynamic response of the above system to heat energy is shown in Figure E–2 [8]. In the electromigration experiments using chequerboards, the source of this heat energy is the Joule heating caused by the current applied to the DUT (device under test).

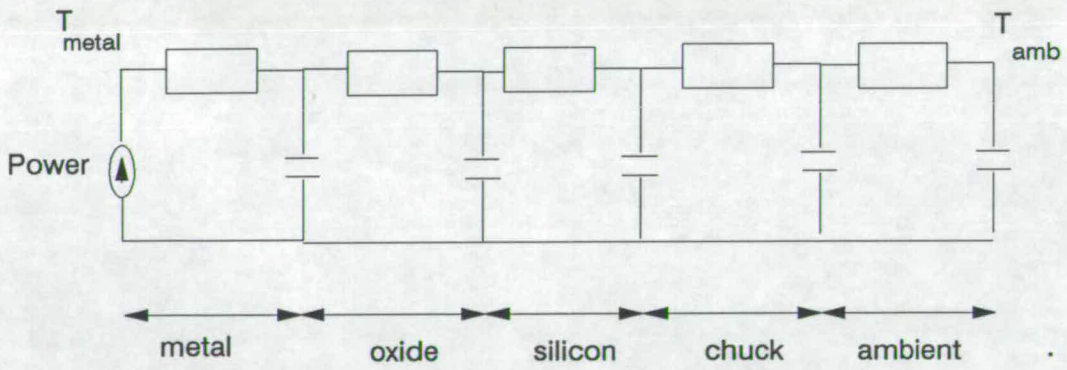


Figure E–2: A simplified thermal model for the metal-oxide-silicon-chuck sandwich

Some calculations and typical values of the different thermal time constants are shown below. The following estimations are expected to indicate the order of magnitude of the various thermal time constants involved in the electromigration experiments using chequerboards. In the example shown below, we consider a $6\mu m \times 6\mu m$ aluminium film of thickness $1\mu m$ deposited over an $1\ \mu m$ thick silicon

dioxide.

Using the following material constants for aluminium:

$\rho = 2.7$ g/cc

s = 0.9 J/g °C

k = 2.38 J/cm °C sec

we get,

$R_{th} = \frac{thickness}{kA} \simeq 116$ °C/W

C_{th} = m s = (volume × density)(specific heat) $\simeq 10^{-10}$ J/°C

Therefore,

$\tau_{metal} = R_{th}C_{th} \sim 10^{-8}$ seconds.

Similarly, using the following material constants for silicon dioxide:

$\rho = 2.2$ g/cc

s = 1.0 J/g °C

k = 0.0096 J/cm °C sec

we get,

$\tau_{oxide} \sim 10^{-7}$ seconds.

Some typical values of the thermal time constants for the heat flow from silicon wafer to the outside environment through the chuck are summarised in table E–1. These values are taken from reference [8].

In the electromigration experiment described in section ? the temperature of the chequerboard rises from 25°C to 50 °C. The rise from 25°C to about 40 °C is rapid and is expected to be of the order of few microseconds to fraction of a millisecond determined by the metal-oxide thermal time constants. However, the chuck-ambient time constant is the longest and was empirically found to be greater than about 5 minutes. Hence the time at which the slope becomes nearly

Thermal time constant	Order of magnitude
$\tau_{silicon}$	milliseconds
τ_{chuck}	seconds
$\tau_{ambient}$	few hundred seconds

Table E–1: Some typical values of the silicon wafer to ambient thermal time constants

zero after a minimum period of 300 seconds from the start of the electromigration experiments has been considered the thermal stabilization time.

Bibliography

[1] S.M.Sze. *VLSI Technology*, chapter 14. McGraw-Hill Book Company, 1988.

[2] Edward B.Hakim. *Microelectronic Reliability*, volume 1, chapter 1. Artech House, London, 1989.

[3] G.Groeseneken. Basic reliability and yield definitions and mathematics. *IMEC (Belgium) summer course - part I*, pages 1–65, 1989.

[4] W.W.Hines and D.C.Montgomery. *Probability and statistics in engineering and management science.* Wiley, New York, 1972.

[5] L. P. Murray, L. C. Rathbun, and E. D. Wolf. New technique and analysis of accelerated electromigration life testing in multilevel metallisations. *Applied Physics Letters*, 53(15) :1414–1416, 1988.

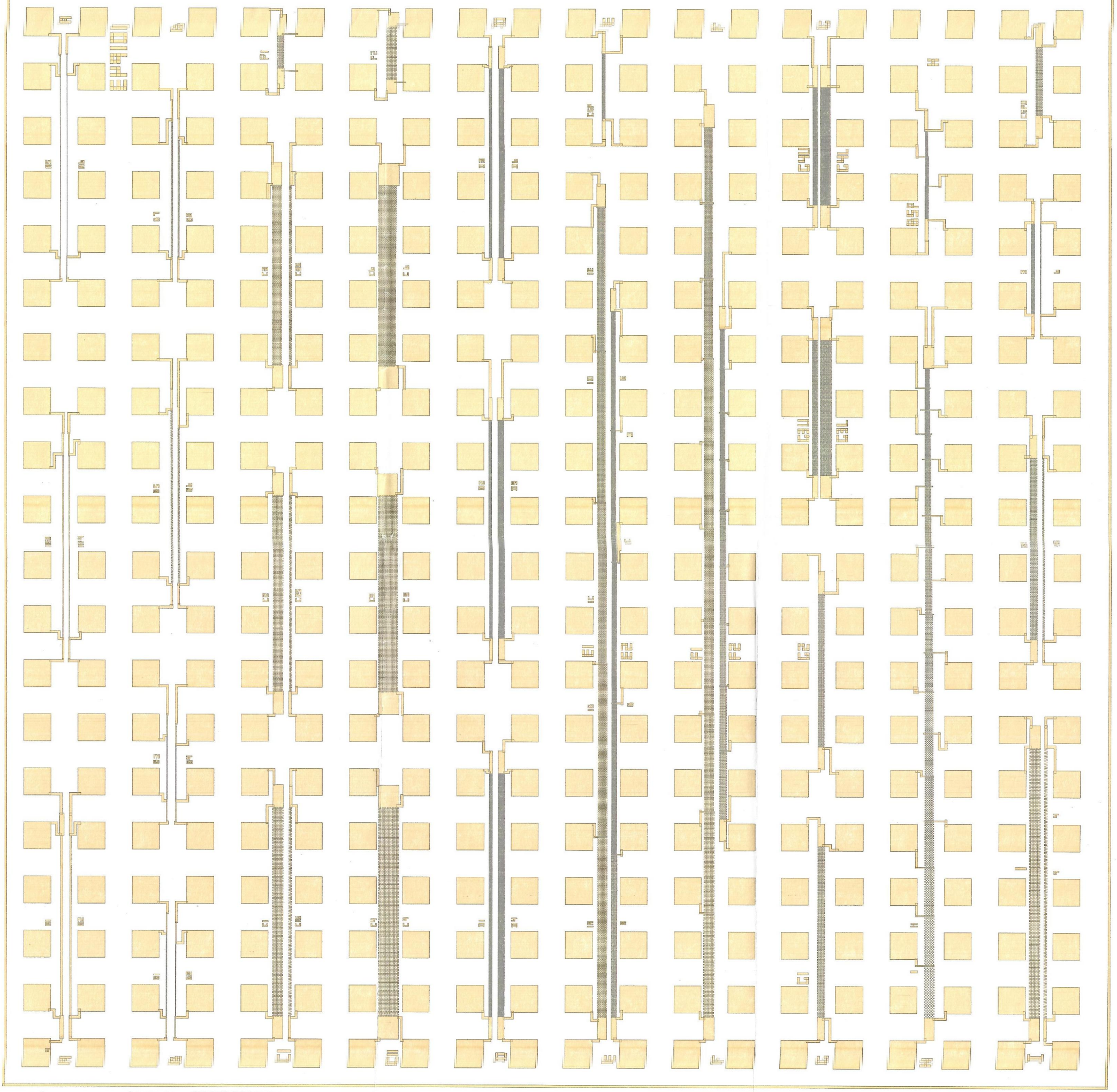
[6] J. Cho and C. V. Thompson. Grain size dependence of electromigration induced failures in narrow interconnect. *Applied Physics Letters*, 54(25):2577–2579, 1989.

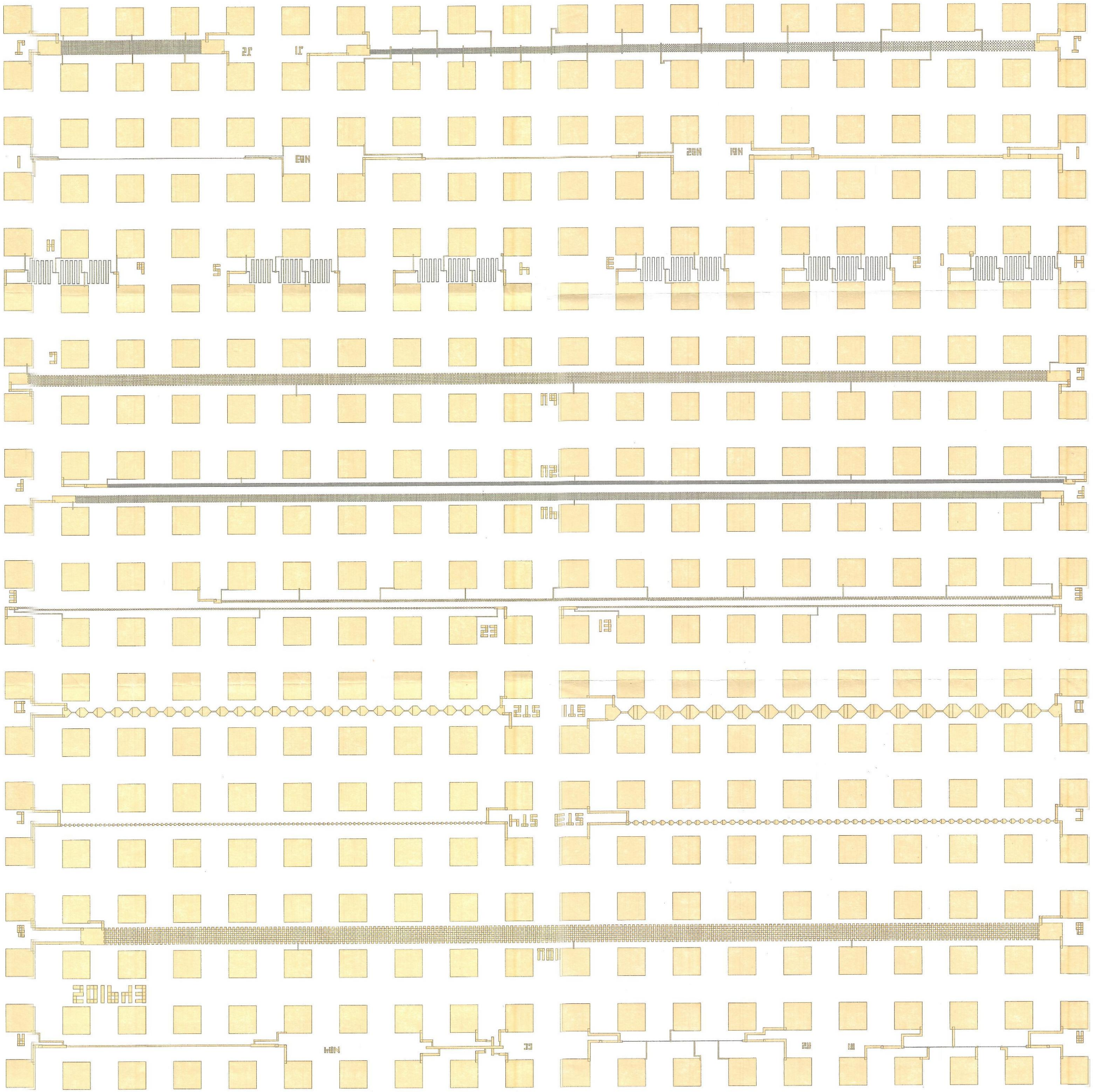
[7] B.N.Agarwala et al. Dependence of electromigration-induced failure time on length and width of aluminium thin-film conductors. *J. Applied Physics*, 41(10):3954–3960, 1970.

[8] Emiliano Pollino. *Microelectronic Reliability*, volume 2, chapter 10. Artech House, MA, 1989.

Appendix F

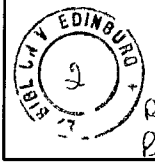
Chip Layout





ELECTROMIGRATION TEST STRUCTURES

EU 9102



RAVINDRA M
PhD 1993

— M RAVINDRA EMF

M RAVINDRA
PhD Student EMF
Dept of Electrical Engineering
University of Edinburgh

ELECTROMIGRATION TEST STRUCTURES

EU 9101

— M RAVINDRA EMF