Ferroelectric Liquid Crystal Spatial Light Modulators: Devices and Applications

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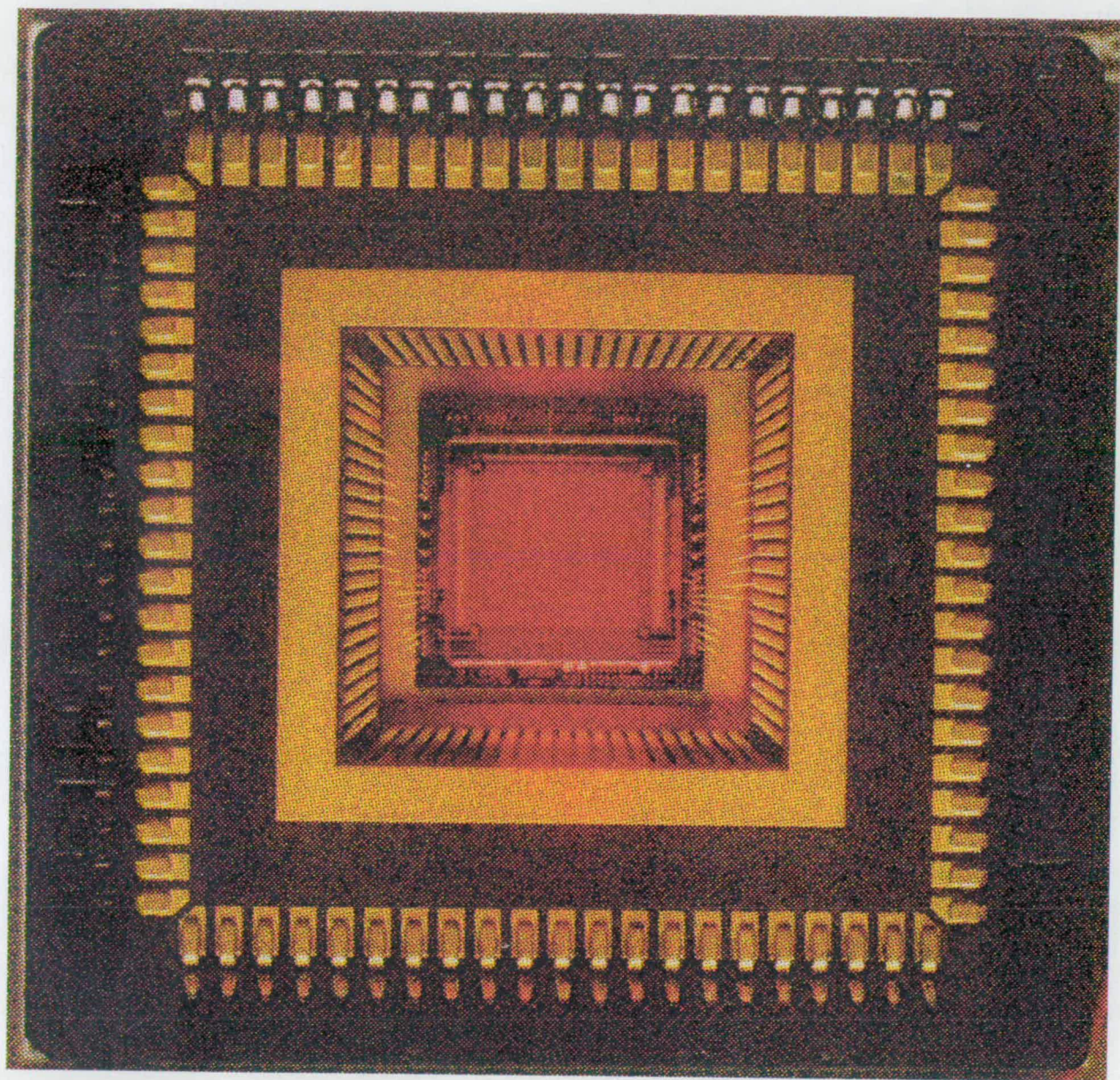
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A packaged 176^2 spatial light modulator

Acknowledgements

Declaration

I declare that the composition of this thesis, and all of the work described within it, was carried out by me, except where otherwise acknowledged.

Abstract

The inherent parallelism in optics allows very powerful information processing. An electronically addressed spatial light modulator is a device which can perform the function of converting information from the electronic domain to the optical domain. A review of optical system requirements and potential spatial light modulator technologies identified the combination of Ferroelectric Liquid Crystal and Very-Large-Scale-Integration circuitry as a very powerful generic technology. The circuitry allows high levels of addressing functionality and low power requirements in the modulation permit high density arrays. The investigation of the interaction of the two parent technologies to form useful modulator devices is the basis of this study.

Ferroelectric liquid crystals were identified as allowing fast switching and good light modulating characteristics. Optimisation of device structures for high optical performance was investigated, particularly cell construction, liquid crystal alignment and cell appraisal techniques. Various liquid crystal configurations were studied chiefly the Surface-Stabilised structure, but also the Soft-mode Electroclinic effect, the Distorted Helix, and Twisted Smectic. The Surface-Stabilised device structure was identified as being the most applicable for use with silicon backplanes and its fabrication parameters were optimised for good performance.

Spatial light modulators were constructed and their performance evaluated. The performance of the devices constructed initially did not approach that obtained in the preliminary liquid crystal studies. Post-processing improvements to the silicon backplane, particularly planarisation, allowed tremendous improvement.

Spatial light modulators were used in real-time optical systems, and their performance gauged. A novel non-coherently illuminated system, which allowed the determination of the Hadamard transform of input images, was constructed and evaluated. Investigation into the use of the devices in an optical Fourier transforming environment were also performed. Simple grating patterns displayed on the devices allowed measurement of the phase modulating diffraction properties. Adaptive computer generated holograms with applications in optical computing were also investigated.

The conclusions of this research were that this technology has great potential for realising many important optical processing architectures, and means of further enhancement of the existing technology are suggested.

Contents

Chapter 1

Introduction: Spatial Light Modulators

'I tried to remember my thesis', Umberto Eco, 1988.

Electrons are suited particularly for switching circuits because they generally interact 'strongly' with matter. Where 'weak' interaction is required, for example in long range communication systems, optics has been employed successfully [1, 2, 3]. As electronic systems reach the fundamental limits of integration and connectivity, other solutions for processing systems will be required. Optics is a very promising candidate for use in conjunction with electronics to improve processing power. Fibre optic communication is already established widely, offering advantages of low losses, very low cross-talk and immunity to electrical interference. But optical fibres, like electrical wires, are still essentially one-dimensional. Free-space optical systems offer two or three dimensions of processing space. Thus, free-space optics has the capability to increase interconnectivity, which is a significant trend, particularly in parallel computing systems. It should be remembered that electronics will generally out-perform optics only over very short distances. Electronics does not scale-up very easily, generally losing processing speed with size. Optics becomes competitive for highly parallel interconnected systems.

A key component for optoelectronic systems is the Spatial Light Modulator (SLM). Such a device has the function of spatially 'imprinting' information onto an optical wavefront. This 'imprinting' can be in the form of modulation of the amplitude, intensity, phase, polarisation and/or wavelength of the optical wavefront. SLMs can essentially be divided into two generic types, the Optically Addressed Spatial Light Modulator (OASLM) and

"read" image

"write" image

output image

(a)

Electronic inputs

SLM

"read" image

output image

(b)
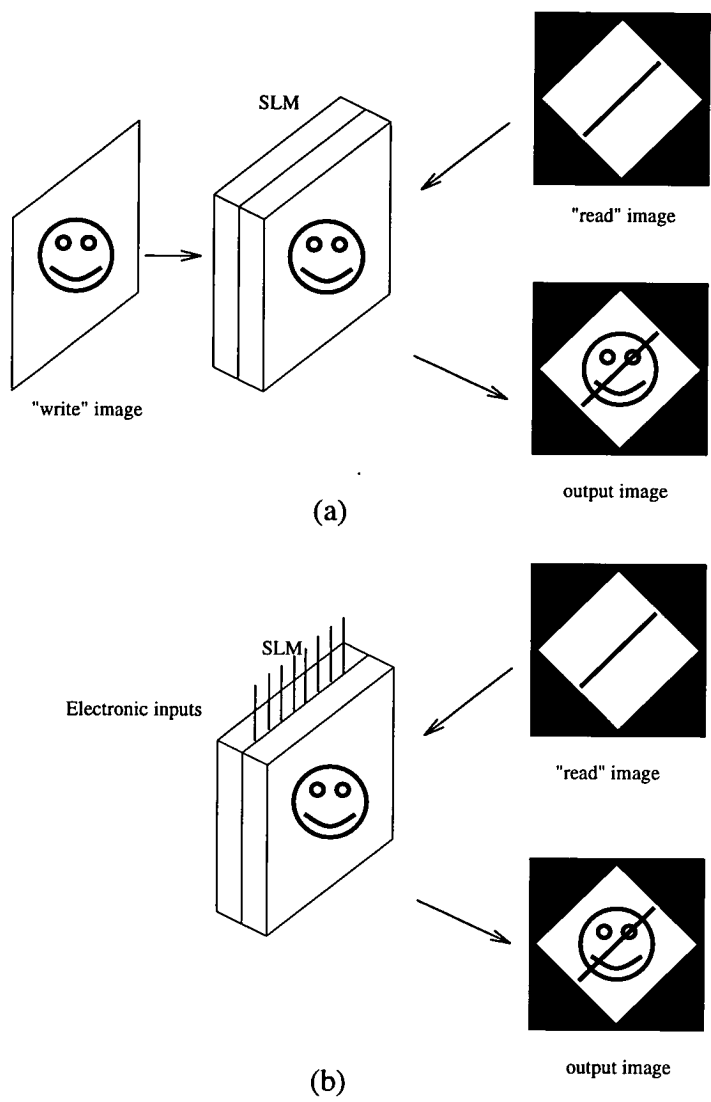
Figure 1.1: Schematic showing an (a) optically addressed spatial light modulator, and an (b) electrically addressed spatial light modulator

the Electronically Addressed Spatial Light Modulator (EASLM), see figure 1.1. The output modulation produced by an OASLM is derived from input optical information. The output modulation produced by an EASLM is derived from input electronic data. The main concern of this study shall be into EASLM devices and their application.

Generally, an EASLM device takes electronic data and represents this data in an optical form by modulating an incident beam of light. The oldest form of SLM is the

photographic transparency, but this can not be updated in real-time. A Liquid Crystal (LC) display is a widely available example of an SLM as it can modulate light which is either reflected or generated by a back light. The Cathode Ray Tube (CRT) is an emissive device and therefore not an SLM. These two examples can give an insight into the advantages of SLMs over emissive devices. In general, SLMs have much lower power requirements than emissive techniques because the device does not need to generate the photons but merely modulate externally generated light. The other main advantage is cascadability: an emissive device cannot be cascaded directly with another one, whereas SLMs can be used to modulate light already modulated by other SLMs. This is a very desirable feature, see figure 1.2. These differences become apparent when one compares LC displays and CRT displays. LC displays tend to be very small, light in weight and can be driven with low voltages at low power. Although a more mature technology, CRT displays are bulky, require high voltages and have high power requirements. It should be noted, that for this reason, there is enormous research into LC displays to replace CRT displays.

Although the LC display is an SLM device, it is not generally suited to high performance optical processing applications. In their current form, LC displays suffer from a number of severe limitations for optical processing systems. These include the relatively primitive electronic addressing of the modulation elements, the relatively bulky size, the low optical quality acceptable for many applications and the relatively slow switching speed of the optical modulation elements. Although widely available commercially and quite mature technologically, much more specialised devices are required for advanced information processing systems. EASLM devices must therefore meet certain criteria if they are to become a viable option in processing systems. These criteria can only be made apparent when one examines the requirements of optoelectronic systems. Therefore, a limited selection of optoelectronic systems will be discussed with a view to determining the required characteristics of EASLM devices. Current EASLM device technology will be reviewed. Ferroelectric Liquid Crystal (FLC) over Very Large Scale Integration (VLSI) silicon backplane SLMs will then be introduced and their particular advantages discussed. The aims of this study will then be presented with regard to the discussion concerning optoelectronic systems and the EASLM devices required.
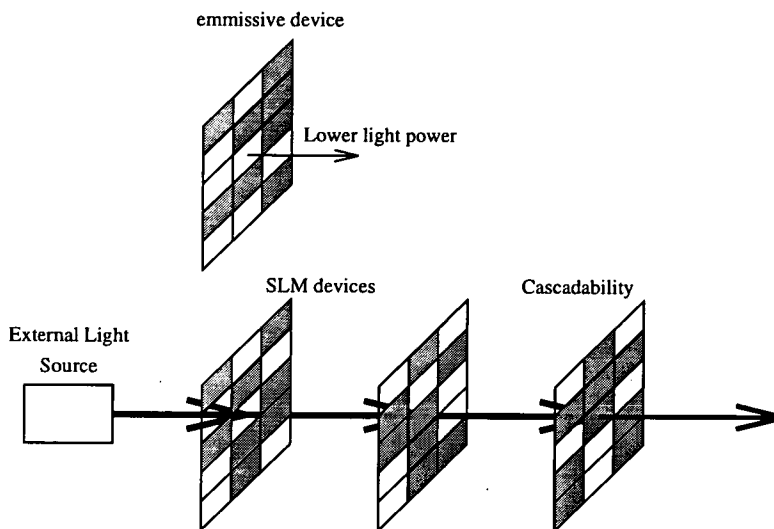
Figure 1.2: Comparison of emissive and light modulating devices

1.1 Optoelectronic Systems

A brief review of optoelectronic systems which require SLMs will be examined. Five of the more important application areas are discussed.

1.1.1 Coherent Optical Processing

If an object at the first focal plane of a thin lens is illuminated with coherent light, the Fourier transform of the object is obtained at the second focal plane [3, 4]. The Fourier transform is a very useful frequency representation of information. Filtering operations on the transform can allow a variety of image processing operations to be performed such as frequency filtering, matched filtering, pattern recognition, image restoration, image compression and feature extraction. An inverse transform operation can be effectively performed by a second lens. This makes the coherent optical processing system extremely powerful and versatile for image processing. This is the classic 6f system (see figure 1.3), first fully appreciated by Vander Lugt in 1966 [4]. Originally, both the object and Fourier plane filter were photographic transparencies, but more powerful systems can be constructed in which EASLMs act as real-time updatable objects and filters. The
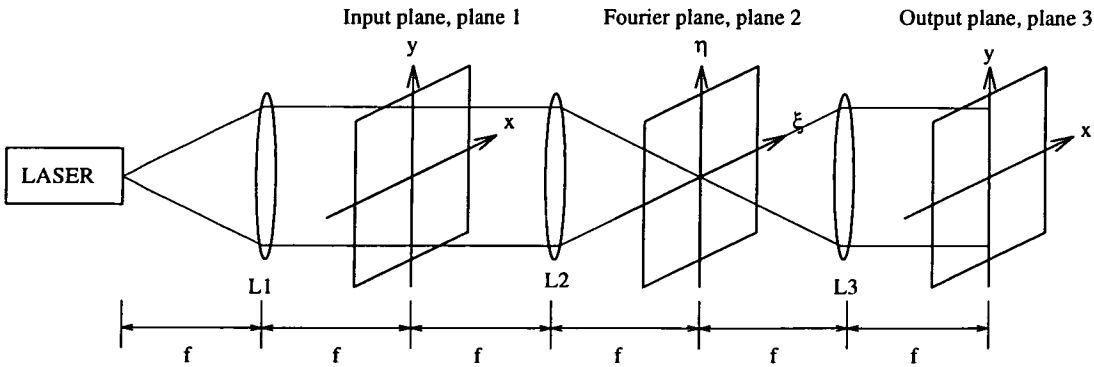
Figure 1.3: The coherent optical processor

modulation imposed by the EASLMs can be either amplitude or phase (or a combination of both) in nature. A high optical quality and large Space-BandWidth Product (SBWP) (or a high number of modulating elements) are the most critical factors. Coherent light illumination requires a high optical phase flatness and uniformity to retain accuracy in the transforms [5]. A high SBWP is required to exploit fully the highly parallel information processing capabilities of the optics. The main information bottle-neck of such a system is in the time to update the information on the SLM. High speed and high quality EASLMs are the key components in coherent optical processing systems.

1.1.2 Free-Space Digital Optical Computing

Digital Optics is a generic term for technology relating to digital logic, data transport and information storage using optical techniques [6, 7]. Digital optical computing is analogous to digital electronic computing. The inherent parallelism of optics is the main advantage of optical systems. Instead of electrical wires carrying the digital information, optical 'beams' may be employed, giving greater interconnectivity and lower crosstalk [8, 9]. In general, such optical systems are not wholly optical, but involve some form of electronic interaction at the optical logic gates. The gates have an optical input and an optical output and usually some form of electronic interaction to perform the logic function. Various system demonstrators have been built, for example using Multiple-Quantum Well (MQW) Self Electro-optic Devices (SEEDs) acting as optical logic gates [10]. EASLM devices are employed for a number of functions in such systems. They can

be used to transfer electronic information into the system, either input data or to change the interconnectivity. Optical modulators used for the optical switching must have a very high optical switching speed if they are to be useful. If used for optical interconnectivity, they must be quickly addressable and offer high contrast ratios and low losses [11].

The term **smart** pixel denotes a pixel with optical input and output incorporating some electronic functionality [12]. This functionality can take many forms from simple thresholding to more complicated programmable inter-pixel interconnectivity. Programmability of the pixel can be arranged under electronic or optical control. An SLM device consisting of such **smart** pixels is essentially an optical/electronic hybrid, exploiting the advantages of both optics and electronics. The **smart** pixel need not be an isolated element in an array and inter-pixel communication can increase the computational power considerably.

1.1.3   Optical Neural Networks

Neural networks have been established as an important complement to conventional computing techniques [13, 14]. The essential difference is that neural networks exploit highly reconfigurable interconnected systems with learning. They are an attempt to mimic some of the characteristics of biological neural systems. Simple thresholding neurons may be interconnected to form a network. Each neuron sums the input from many other neurons, compares this value to a threshold and 'fires' if the sum exceeds the threshold. The output from each neuron is distributed to other neurons in the network by a weighted interconnect (figure 1.4). The functionality of the network is determined by the interconnection weights and the network learns by modifying the interconnection weights. The network may be trained with sets of target input and corresponding output patterns allowing the network to build its own internal representation of the classification problem. The network is then able to process new input patterns using the knowledge learnt in the training phase. The human brain requires some 10^{10} neurons, each interconnected to some 10^4 others to perform its complicated recognition processes. This level of interconnection is very difficult to achieve in electronic systems. However, this large scale, dense and non-interacting channel network may be implemented by exploiting free-space optical interconnection. The use of SLMs in optical neural network systems is

Weighted Interconnect   Neuron

Neuron

Functionality

Sum Signals + Threshold
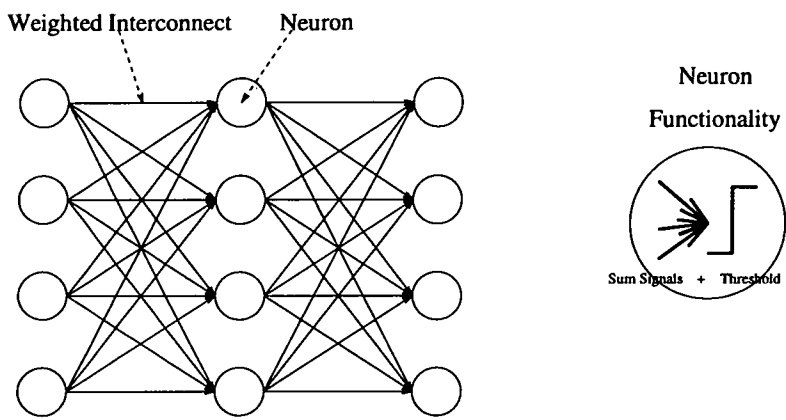
Figure 1.4: Schematic of a Neural Network

somewhat similar to their use in digital optical computing, allowing electronic-to-optical data conversion and adaptive interconnection, except that in neural networks the signals tend to be analogue (introducing fuzziness) [15]. The SLMs can be used either in the neuron plane as **smart** pixel devices, requiring the functionality of optical-to-electrical summation, thresholding and output, or as interconnection weighting elements.

1.1.4   Displays

Arguably the most obvious commercial application of SLMs is in high quality displays, such as in helmet mounted display systems. The general requirements of such devices include a large number of pixels, a high reflectivity or transmission, a good contrast ratio and the ability to produce grey levels [16]. With large numbers of pixels, fast addressing times are crucial. Therefore with large arrays, intelligent devices utilising data compression algorithms will be required. For holographic displays, phase modulation capabilities and phase uniformity are important criteria. The main display device in current use is the CRT, but it is reaching the limits of design.

1.1.5   Telecommunication Switching and Routing

Fibre bundles are used to carry information as optics is very good at the transfer of information. To route this information from one fibre to another, the optical signal is often converted to an electronic one, routed electronically and then converted back to an optical signal. It would be more efficient and indeed much faster, if the signal was kept optical while being routed. In a similar way, optical fibre amplifiers are much more desirable than electronic amplifiers in fibre systems [17].

The optical cross-bar is a means of achieving a communication routing where the information remains optical. N input channels require N^2 SLM 'shutters' to fully connect to N output channels. Optical information from one input channel is 'fanned out' with diffractive or refractive optics to N SLM 'shutters' which either allows (**ON**) or disallows (**OFF**) the optical information to be routed to any of the N output 'channels'. High speed pulsed data rates (GHz) can be routed by the comparatively slow optical 'shutters', as the 'shutter' acts as a transparent switch. The main criteria is a high contrast ratio, as low contrast limits the number of channels routable due to cross-talk [18].

1.2   Spatial Light Modulator Requirements

Figure 1.5 summarises the most important SLM specifications required by the optical system applications discussed. Although differing in their particular requirements, such systems do show a general need for a certain generic type of device. The device is used to convert electronic information into optical information for input, control, connectivity, adaptive or optimisation functionality in the optoelectronic system. The characteristics of this generic device should be:

- Versatile in the selection of the operating optical wavelengths (UV-IR).

- Very fast switching optical modulation elements (picosecond).

- Relatively high level of addressing complexity for high speed of information update ($> 10^6$ pixel elements).

SLM SPEC SYSTEM	Contrast Ratio (ratio of ON to OFF pixels)	Switching Speeds	High optical throughput (efficiency)	High optical quality (flatness, uniformity)	Large number of pixels (SBWP)	Compact and low power requirements
Coherent Optical Processing				✓	✓	
Digital Optical Computing		✓	✓			
Optical Neural Networks	✓		✓			
Displays and Projection Systems					✓	✓
Telecoms switching and routing	✓		✓			

Figure 1.5: The more important SLM specification requirements for optical systems

- Very good optical quality for high efficiency and minimisation of phase errors (Flatness or uniformity better than $\lambda/16$)

- A very compact size (less than $1cm \times 1cm \times 1cm$).

- The opportunity for large-volume production.

- Very low power requirements ($< 1W/cm^2$).

- Robust in nature.

Research into the field of SLMs has resulted in a wide variety of technologies. A short review of the more important and promising technologies is presented in the next section.

1.3   Current Spatial Light Modulator Technologies

A number of EASLMs are being developed currently. The devices discussed initially will employ light modulation schemes not related to LC technology. In general, these modulation technologies are not easily compatible with VLSI silicon processes. Hybrid SLM devices involve an interfacing of the VLSI silicon backplane addressing circuit substrate with the light modulating substrate. This is not a trivial undertaking and a variety of techniques are being investigated such as solder bump and lift-off processes [19]. Most of the modulating devices to be discussed use a simple line addressing of the modulation elements.

1.3.1   Multiple Quantum Well Devices

MQW technology would seem to be the most active area of research for light modulation. MQWs are based on III-V epitaxy and processing technology [10]. Layers of material are constructed, usually on GaAs substrates, to obtain MQW stacks. When fields are applied to the stack, mechanisms such as the Quantum Confined Stark Effect (QCSE) can allow absorption of certain wavelengths of light. Therefore, amplitude light modulation is achieved by varying the electroabsorption. Figure 1.6 gives an example of a typical MQW structure, showing a number of thin doped layers upon a GaAs substrate. MQWs can also be constructed to be birefringence modulators which can rotate incident polarised light [20]. SEEDs are a subset of MQW devices and are a combination of MQW modulators, photodetectors and possibly other circuitry [21]. The MQW devices are sometimes enhanced by being constructed as Fabry-Perot cavities. This has resulted in very high contrast being attainable [22]. The main advantage of the MQW is the fast switching speeds, as high as picoseconds. This is arguably the highest switching available for light modulation, although very high powers, both optical and electrical, are required to use these devices practically. Devices have been quoted recently as having contrast ratios of $> 100 : 1$ and switching speeds of the order of 10 picoseconds [23].
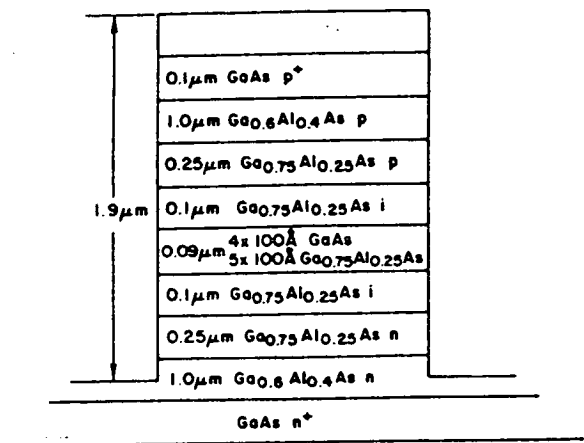
Figure 1.6: A typical Multiple Quantum Well structure

1.3.2 Magneto-Optic Devices

The Magneto-Optic modulator is a solid state device which is electronically addressed and transmissive in operation [5]. The Faraday effect is used to rotate incident polarised light. The device is fabricated from a magneto-optic substrate (e.g. Gallium Garnate). Pixels are etched and the magnetic domains are aligned perpendicular to the film surface, parallel to an external field. Orthogonal current drive lines are deposited on both sides of the film. Loops at the intersection of the address lines are used to create a magnetic field at the pixel corner. The field at the corner induces a propagation of the magnetic domain wall to the other corner of the pixel. Creation of the domain in the pixel is bistable. This domain causes a different rotation of the polarisation of incident light than in an oppositely aligned pixel domain. A reversed current in the loop will revert the pixel to the original domain.

Contrast ratios of 60,000:1 are projected for the device although this is a trade-off with pixel transmission which would be very low. Arrays of up to 256 × 256 have been fabricated. These have exhibited a low switching power, with 22 volt operation, optical flatness $\frac{\lambda}{4}$ and pixel switching times of $10^{-9}s$ [24]. The main switching limit is in the heat

from Ohmic loss in the addressing wires. Parallel addressing is impractical due to the limiting effects of thermal and magnetic stress. However, these devices are commercially available to a certain extent. In practice, the devices are slow, have a poor contrast, low optical quality and require to be cooled. Scaling the device up to larger array sizes will be problematic due to the heat and magnetic damage constraints. The overall size and weight of the device can be considered prohibitive.

1.3.3 Deformable Mirror Devices

The Deformable Mirror Device (DMD) consists of micromechanical arrays of electronically addressable mirror elements [25, 15]. In general, incident light is modulated either by a change of direction or phase by the mechanical movement of a mirror element. Three main types of devices have so far been developed, the elastomer, the membrane and the cantilever. In the elastomer device, a metallised elastomer is electrically addressed by underlying circuitry. Electrostatic forces due to the the addressing cause the elastomer thickness to deform. Membrane devices have a metallised polymer membrane stretched over a spacer grid above the addressing circuitry. When the membrane is addressed, it deforms into the air gap between the membrane and underlying circuitry. The cantilever (or torsion beam) device (shown in figure 1.7) has a mirrored cantilever and hinge above addressing circuitry. Electronic addressing of underlying circuitry causes the beam to be electrostatically attracted to the electrode. The membrane device has been attempted at Edinburgh University for a phase modulating SLM with varying degrees of success [26]. Although these devices operate mechanically, response times have been quoted as fast as $10\mu S$. These devices are of particular interest as they can be produced through monolithic fabrication processes and are therefore applicable to low voltage, high density silicon address circuitry. Current pixel sizes are quoted at $25\mu m$, with arrays of 128×128 cantilever pixels and has a frame rate of 4kHz [25]. The devices modulate light either by deflection or changing the optical path length (phase modulation). Contrast ratio measurements of 10:1 are quoted for devices configured to give an amplitude modulation. Texas Instruments are planning $1,000 \times 1,000$ arrays using existing CMOS technology and improved fabrication techniques. They are also hoping to increase the speed by improved switching techniques. The main draw backs of such devices currently are the low yields, low robustness (the mirrors are easily broken), response-time dependent on
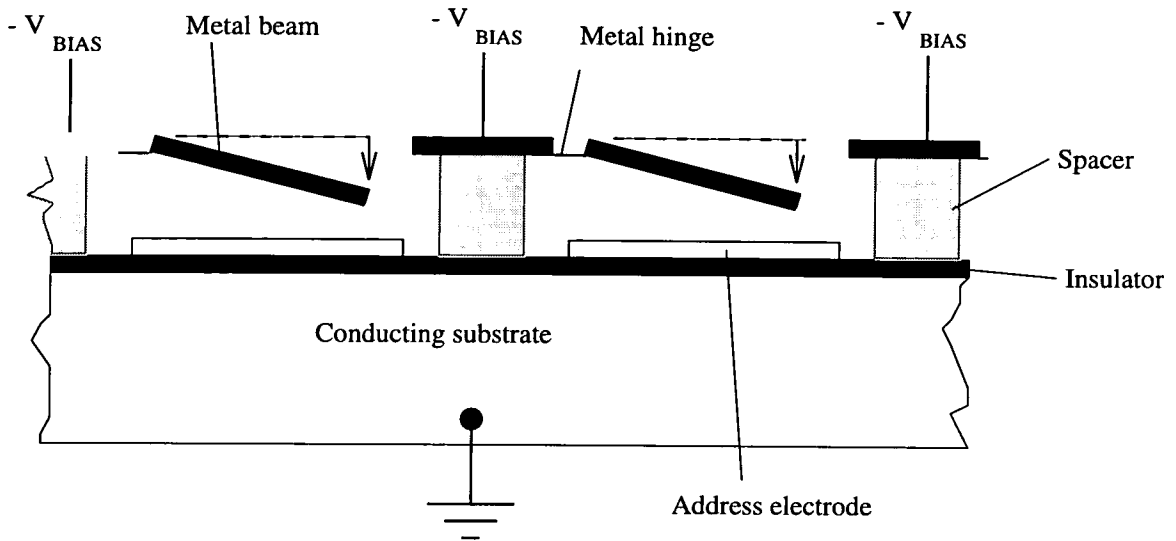
Figure 1.7: The cantilever Deformable Mirror device

atmospheric conditions and, as far as we know, not commercially available.

1.3.4   Electro-Optic Crystal Devices

Various crystals have useful electro-optic properties. Crystals such as PLZT (Lead-
nthanum-Zirconium-Titanate) and LiNbO$_3$ exhibit Pockels Effect [27, 28]. This is a linear
longitudinal electro-optic effect where birefringence is induced proportional to an applied
electric field [29]. This allows the modulation of amplitude or phase appropriate to
the arrangement of polarisers. The produced birefringence is usually independent of
the depth as it is field dependent. One of the main drawbacks of such materials is
the relatively high fields required for useful effects, typically hundreds of volts. Device
fabrication is also traditionally difficult as thin mono-domain layers of the crystal material
must be grown on a modulation element substrate. Some devices have nevertheless been
produced. A 12 × 12 element PLZT device was fabricated on high voltage nMOS silicon
circuitry. Amplitude modulation showing a contrast of 35:1 has been demonstrated with
a switching time of $10\mu S$ [19].

1.3.5   New Light Modulating Materials

Many new and interesting materials for optical modulation are currently being developed. Electro-optic polymers are one such group of new materials [30, 31, 32]. Electro-optic polymers are being investigated to supersede electro-optic crystals and LCs. They consist of two primary components: a nonlinear moiety with a large hyperpolarisability (guest) and a polymer (host) system. The mechanical, structural, and passive optical properties are determined by the host polymer and the electro-optic properties determined by the guest. The materials are spin-coatable into high quality, multilayer films, and can be patterned and metallised. So far, these materials have found most application in planar optical wave-guide devices as switches, directional couplers and Fabry-Perot etalons. Their use in free-space optics is as yet undetermined. Another interesting area of research is into bio-electro-optic devices. Bioengineering can produce living material such as bacteria which can modulate light. As an example, a genetic mutation of the common bacteria Rhosdopsm, can be grown to produce an electro-optic film [33]. Two absorption states at different wavelengths allow the film to be used as an OASLM. The photosensitivity is found to be over 10,000 lp/mm and the switching speed is quoted as a few pico-seconds. Certainly, such novel approaches to electro-optic materials would seem to indicate a very promising future.

1.3.6   Liquid Crystal Light Modulator Technologies

Liquid Crystal (LC) materials have the advantage of requiring low voltages and power to exhibit large electro-optic effects (chapter 2 will discuss these in more detail). Large arrays of matrix-addressed pixels have been fabricated for commercial display purposes. A matrix-addressed pixel is the simple crossing of two orthogonal transparent conducting electrodes. The voltage across a line of pixels can thus be altered to modulate the phase, polarisation or amplitude of an optical wavefront. But, this results in a low frame rate as only one line at a time is switched before progressing to addressing the next. Thin-film transistor technology has been employed to improve this type of device. A single transistor can be employed at the pixel to store the addressing voltage. These devices tend to be very large for optical system applications, have a low optical quality and although widely commercially available suffer from yield problems. Most thin-film tran-

sistor and matrix addressed LC devices use nematic LC modulation structures, although some have been reported with Ferroelectric Liquid Crystal (FLC) [34]. Other techniques for electronically addressed LC modulation include Electron-Beam Addressing [35]. This is essentially a CRT used to write voltages onto an electrode mirror, on top of which is fabricated an LC modulator. This device is commercially available but very bulky, and requires high voltages and power.

1.4 Modulator Addressing

Most of the modulator technologies show a basic limitation. This limitation is the limited complexity and functionality of the electronic addressing. If devices are to be scaled up to large arrays and still retain fast frame rates then the bottle-neck in EASLM devices is the electronic addressing of the modulation elements. Therefore for fast SLMs, a higher level of addressing circuitry than simple conducting electrodes or single transistors is crucial. The hierarchy of modulator addressing circuitry is thus:

- Direct element addressing.

- Matrix addressing.

- Single Transistor Active Addressing.

- Multiple Transistor Active Addressing.

- Smart pixel addressing.

This higher pixel functionality could include memory, intrapixel processing, interpixel communication, data decoding, data compression, shift register addressing or even on-pixel optical input. The placing of LCs onto silicon integrated circuitry would seem an obvious step toward investigating such device requirements. Backplanes with similar functionalities will be needed for the other modulation technologies.

1.5 VLSI Silicon Backplane Liquid Crystal Spatial Light Modulators

LCs are a very attractive SLM technology due to the low power requirements and the low voltage switching. Complex addressing is required for the modulators if high frame rates are required on large arrays. The most obvious mature technology for the design of such addressing circuitry is Very Large Scale Integration (VLSI) silicon. The device structure of LCs on top of VLSI circuitry is shown in figure 1.8. The placing of LCs on wafer scale silicon integrated circuitry was first attempted by Hughes Aircraft Company, Toshiba Corporation, Suwa Seikosha and STC Technology in the early 1980's. These consisted of simple Dynamic Random Access Memory (DRAM) pixels for display purposes and the approach was abandoned in favour of thin-film technologies (section 1.4) for transmissive displays. LC devices for use in optical correlator systems on single chip VLSI circuits were pioneered by the University of Edinburgh in 1986 [36, 37, 38]. These devices were much smaller so as to be compatible with compact optical system resolutions. The original device was a 16 × 16 Static Random Access Memory (SRAM) device designed by I.Underwood and R.M.Sillitto [36]. The device had the relatively slow guest-host nematic LC structure fabricated on top of the modulation mirrors. An interferogram of the pixel mirror is shown in figure 1.9. This device has been successfully used in optical correlator systems [39, 40]. Only recently have FLCs been employed on such VLSI SLM devices. Much of the research effort in these devices has been concerned with the design of the VLSI backplane, particularly **smart** pixel structures. Although FLC technology and VLSI technology are advancing independently, there is very little work being carried out to improve their compatibility. Much of this effort is being carried out at the University of Edinburgh.

1.5.1 Currently Designed VLSI Backplanes

Table 1.1 (courtesy of I.Underwood) shows a table listing of all the currently designed VLSI backplanes before 1993 for LC SLM purposes as far as the author is aware [36, 39, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52]. It should be noted that there is a particular trend towards more complicated pixel designs. One would expect that this trend should
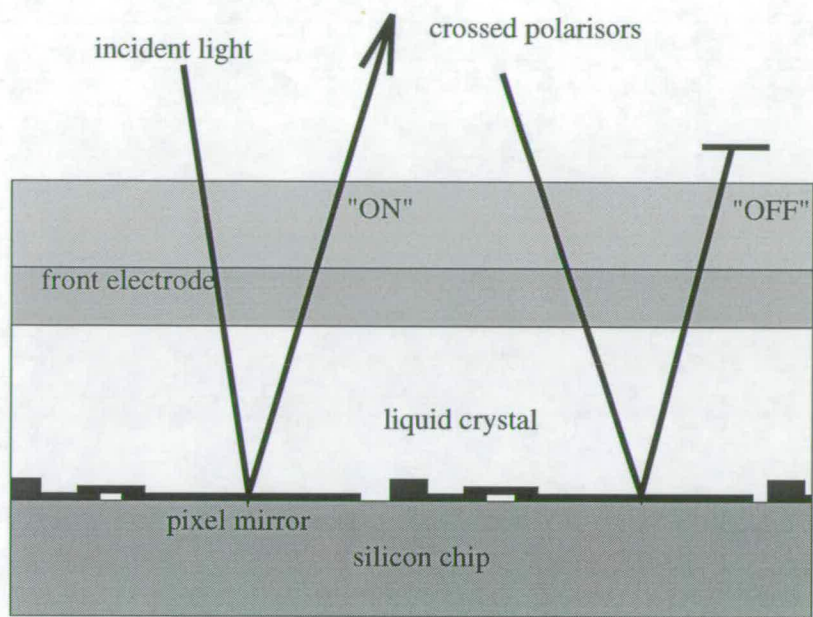
Figure 1.8: A schematic of a VLSI silicon Liquid Crystal SLM
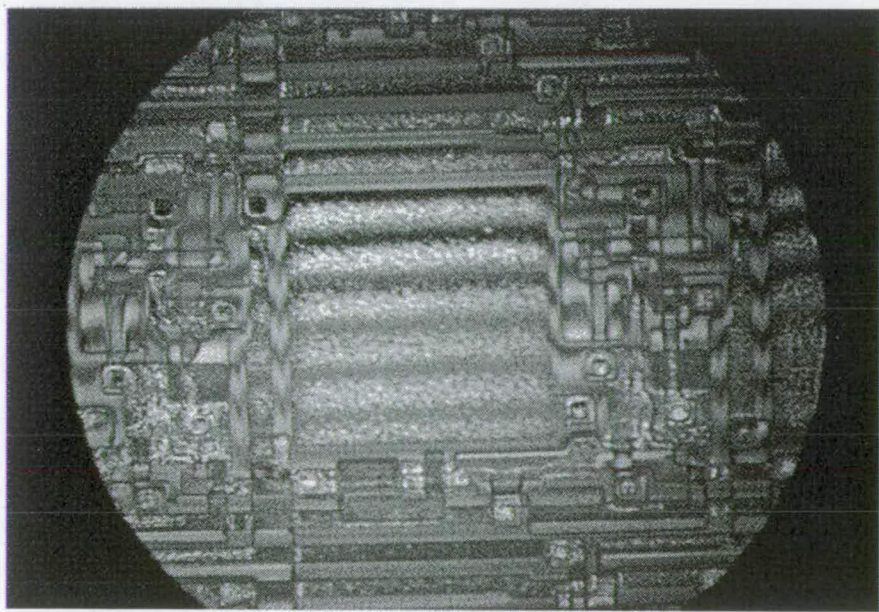
Figure 1.9: An interferogram of the original SLM pixel

Date	Group	array	pixel style
1981	STC Tech.	40 × 40	DRAM
1986	Univ. of Edinburgh	16 × 16	SRAM-XNOR
1988	Univ. of Edinburgh	50 × 50	SRAM-XNOR
1988	Univ. of Edinburgh	40 × 40	SRAM-XNOR
1989	Univ. of Edinburgh	128 × 128	SRAM-XNOR
1989	Univ. of Edinburgh STC	176 × 176	DRAM
1989	Univ. of Edinburgh STC	176 × 176	DRAM
1990	Georgia Tech Displaytech	64 × 64	SRAM 8 transistors
1990	Univ. of Colorado	64 × 64	DRAM 4 transistors
1991	Lockheed	12 × 12	DRAM
1992	Univ. of Colorado BNS	128 × 128	DRAM
1992	Univ. of Colorado	64 × 64	DRAM High voltage (2 trans.)
1993	Univ. of Edinburgh	256 × 256	SRAM-XOR

Table 1.1: Silicon backplanes for LC SLMs

continue with more intelligent arrays being designed. The essential similarity between all of the modulator pixels is that a voltage is held on an aluminium modulation mirror either using a DRAM or SRAM pixel memory. Some of the devices have shift register addressing of the pixel lines which allows easier interfacing with electronic hardware. In general, the earlier devices developed at the University of Edinburgh were used to drive nematic LC structures. FLC devices have been constructed on devices in the University of Colorado with a certain degree of success. This work tends to concentrate on the VLSI design of the backplane, and the important issues concerning the development of the backplanes towards usable system devices have not yet been fully investigated.
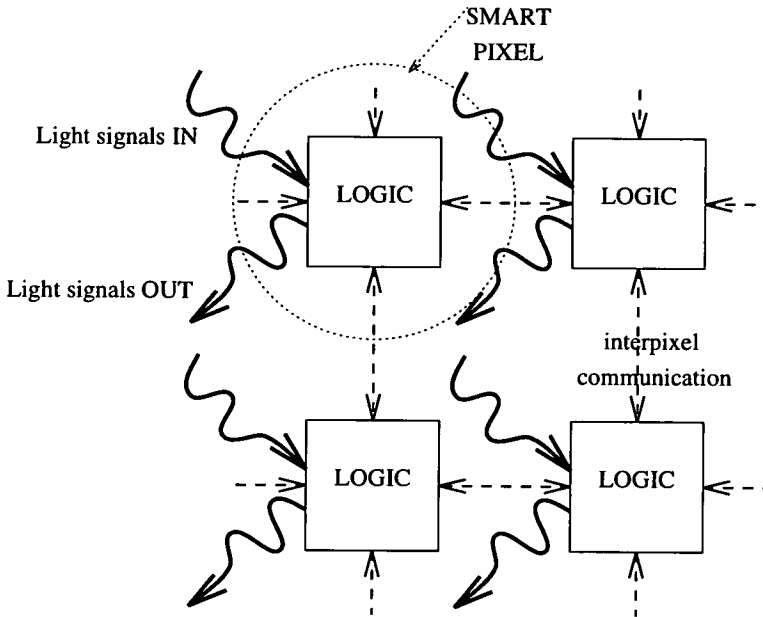
Figure 1.10: Schematic of a Smart Pixel

1.5.2 Smart Spatial Light modulator Devices

Smart SLMs refer to devices which include the following generic attributes:[50, 12]

- **Memory:** Storage of data at a pixel, either in the electronic circuit or the modulation material.

- **Optical Input:** Input of optically coded information by photodetection integrated into the electronic circuitry at either the pixel level or device level.

- **Optical Output:** Output of optically coded information by electro-optic modulator.

- **Intrapixel Processing:** Local processing functionality at the pixel such as amplification, arithmetic or logical operation, thresholding, comparison, differentiation or integration on stored and/or input data.

- **Interpixel Communication:** Information exchange between pixels either at a local or global level.

A schematic of a smart pixel is shown in figure 1.10. These attributes are available readily from FLC/VLSI technology. Smart pixel SLMs have been designed through the **Smart and Advanced Spatial Light Modulators (SASLM)** program in the U.K. [12, 53] and in the University of Colorado [44]. These devices have been designed for a variety of optoelectronic system applications. These include, neural networks, cellular logic, image processing, and optical computing.

1.5.3 Advantages and Limitations

FLC/VLSI SLM technology is potentially very attractive. It addresses two of the important criteria for SLMs in realistic optical systems: low power requirement for the available performance characteristics and a potentially high level of complexity in the addressing of the modulators. These would appear to be its most obvious advantages. Although other modulation technologies have potentially better performance (e.g. picosecond switching), this performance is not as readily accessible for practical SLM devices. The main limitations of FLC/VLSI SLMs are in the individual technologies of FLC devices and VLSI silicon backplanes themselves. Practical FLC devices have fundamental limits on their modulation characteristics [54]. FLC/VLSI SLM characteristics will only asymptotically reach these practical limits through further research. VLSI backplane modulator design is in itself a very active area of research, being pushed by advances in silicon fabrication and design technologies. No one in the field of FLC/VLSI SLMs is under any illusions that newer materials will not become available in the future that will supersede FLCs in performance and application. The important point to be made is that FLC/VLSI SLMs allow the capabilities of optical systems to be assessed now, no matter what electro-optic material is used on future VLSI SLM devices. Performance can only be improved and one must look optimistically to future developments.

1.6 The Aims of the Project

The aims of this study are twofold: firstly, to develop techniques to produce high quality FLC modulator structures directly applicable to currently available and future VLSI

silicon SLM backplanes; secondly, to assess the performance of such FLC/VLSI SLM devices in novel system applications. The following sections describe the aims in more detail.

1.6.1 Ferroelectric Liquid Crystal Cell Development

Issues concerning FLC modulators will be addressed in chapter 2 with a view to developing cell fabrication techniques in chapter 3. The large topic of FLC materials and device structures will be reviewed to gain an insight into the subject and establish a starting point. A number of important FLC topics will be discussed and some examined experimentally. This will allow techniques to be developed to produce and appraise FLC test cells. In chapter 4, the techniques will then be developed to meet the specific requirements of VLSI backplane SLM devices and different modulation methods will be investigated and appraised. The most suitable techniques will be applied to SLM backplane devices for use in optical systems in chapter 5.

1.6.2 Novel Spatial Light Modulator System Applications

The performance of the developed SLM devices will be analysed in chapters 6 and 7. Examples of the main system applications of the SLM devices will be investigated in both simulation and using the SLM devices themselves in optical systems. Two particular novel optical system demonstrators will be developed: An noncoherent image Hadamard transform system and a computer generated hologram (CGH) display for holographic interconnection and routing applications. The implications of performance in these optical systems will provide information regarding which FLC structures and techniques are most applicable.

1.6.3 The Structure of the Thesis

The thesis is structured in a manner to try to keep it focused on device development and experimental verification. Some salient topics which may detract from the arguement have been placed in the appendices. The information and experimentation described in the appendices are significant, however the thesis can be viewed as whole without them.

1.7 Summary

A need exists for high performance SLM devices for the many useful optical processing system applications. The current state of SLM device technology has been discussed, showing that the generic technology of FLC/VLSI is very attractive. The development of this technology and its appraisal in optical system applications is the goal of this study.

Chapter 2

Ferroelectric Liquid Crystals

'He who would foresee what has to be should reflect on what has been',
Niccolo Machiavelli, The Discourses.

LC light modulation is an enormous interdisciplinary subject, embracing chemistry and physics [55, 56]. For the purposes of this study only certain key features of particular importance to silicon VLSI backplane SLM devices will be addressed. Commercially available LC modulators appeared in the early 1970s as single element addressed nematic displays. Although a very mature LC technology, nematic LCs are slow switching and have low contrast. From the early 1980s FLC materials were investigated, exhibiting much higher switching speeds and promising very high contrasts with the advantages of low power and voltage requirements [57, 58]. Nematic devices have switching speeds of the order of milliseconds, but FLC materials have switching speeds of the order of microseconds. These modulators are incorporated readily onto VLSI backplane SLMs [59]. In the development of FLC devices, initially it was generally held that FLC technology was just a straight forward progression from nematic technology. This could not have been further from the truth as was discovered in subsequent research work. FLC devices are inherently more complicated than nematics and this will be reflected in the discussions in this chapter. The practical differences between FLC devices and nematics include [60]:

- The FLC cell is much thinner than the nematic (microns instead of 10's of microns).

- The FLC structure is much more sensitive to surface treatment on the bounding electrodes.

- The nematic device tends to compensate for differences in cell thickness to a first order approximation.

- The light modulation techniques are essentially varied and different.

- The FLC cell is inherently more difficult to fill due to the higher viscosity of the material.

The speed advantage of FLC device structures is due to its inherent spontaneous polarisation [54]. Nematic devices do not exhibit this property and so a dipole must be induced [59]. From a relaxed **OFF** state a nematic molecule is reorientated to an **ON** by an external field. The field induces a dipole moment which interacts with the field to allow the reorientation. To return to the **OFF** state the field is removed, allowing the molecules to slowly relax by elastic processes. In the FLC devices, different reorientation states are reached by being externally driven into both the **ON** and **OFF** states due to the inherent spontaneous polarisation. The emphasis of this study concerns the implications of the marriage of FLC technology and VLSI backplane technology and overcoming the inherent difficulties. To this end, a discussion of FLC background is a necessary introduction to the complexities of device implementation.

2.1 Liquid Crystals: General

The term liquid crystal is applied to fluids which have a certain degree of ordering in the arrangement of their molecules [55, 56]. Anisotropic behaviour in the various physical properties of liquid crystals can be caused by this ordering. These mechanical, electrical, magnetic and optical properties have been exploited for numerous applications [61]. This usefulness of liquid crystals has been the reason for their enormous interest. The electro-optic effects of liquid crystals will be of primary concern in this study. The basis of this electro-optic behaviour is due to some external electrical signal reorientating the preferred orientation of the molecules and thus altering certain optical properties. The study of the electro-optic properties of liquid crystal has essentially a two stage history. Firstly,
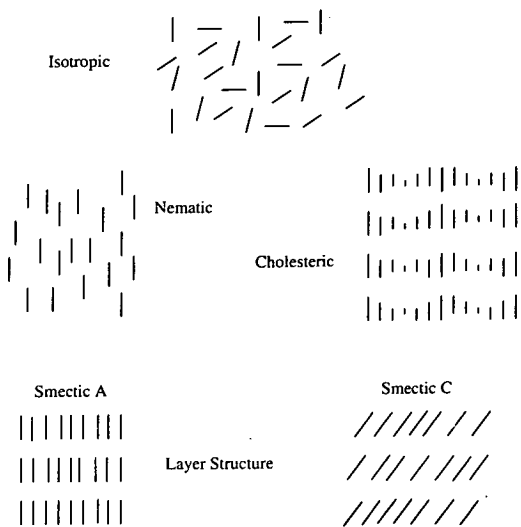
Figure 2.1: Liquid Crystal Mesophases

before the early 1970s, small scale research was employed on these novel materials. Then, once the prospect of their application to displays was realised, a tremendous interest was engendered which persists to the present day.

Liquid crystal mesophases are thermodynamically stable states of mesogenic compounds. They occur in the melting process between the solid state and the liquid state. The solid state can be described as a long-range positional ordering of the molecules in three-dimensions. The liquid state is a complete disorganised arrangement of the molecules. Therefore, the mesophases of liquid crystals are somewhere between these two extreme cases. This results in the physical properties and structures being intermediary. The mesophases of rod-like molecules are of most interest. These can be divided into three general categories, nematics, cholesterics and smectics [62]. Nematics have no positional ordering (see figure 2.1), but the molecular axis does have a preferential direction and the long axes of the molecules are approximately parallel. Cholesterics are characterised by the direction of the long molecular axes in the molecules forming a helix from layer-to-layer. Smectics are identified by short-range positional ordering and long-range orientational ordering. This results in a characteristic layer structure called smectic layers. The smectic state itself is further divided into classes which differ in the the nature of the positional ordering and the molecular tilt. Some of these classes exhibit a temperature dependent tilt angle with respect to the smectic layers. If these molecules are designed
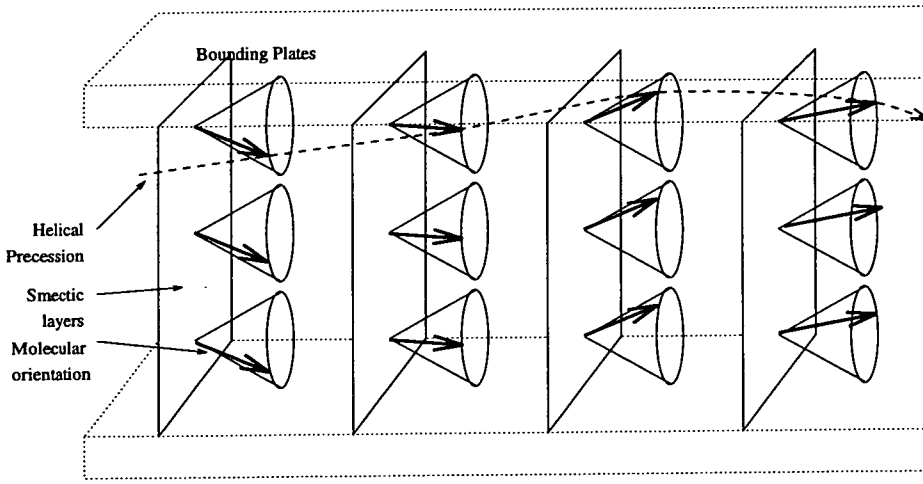
Figure 2.2: The Smectic C* structure.

to be chiral as well, from symmetry arguments it can be deduced that the the material will exhibit a local non-zero spontaneous polarisation and will therefore be ferroelectric. Many smectic phases have been studied. Two of the most interesting are the smectic A (SmA) phase and the smectic C (SmC) phase. When exhibiting chirality, these phases are denoted by a *. For example, the chiral smectic C phase is abbreviated to SmC*. When the smectic layers are parallel, this structure is commonly called the 'bookshelf' or 'bookstack' structure.

2.2 Ferroelectric Liquid Crystals

Ferroelectricity in liquid crystals was first demonstrated by Meyer in 1975 [63]. Some dielectrics, termed polar materials, exhibit a non-zero and permanent value of electric polarisation, known as spontaneous polarisation (P_s). This polarisation exists in the absence of an external applied field or stress. If the direction of the spontaneous polarisation can be changed by the application of an external applied field they are termed ferroelectric. The materials have an analogy with ferromagnetic materials, having corresponding properties. FLC material thus exhibits hysteresis loops, domains and Curie-Weiss behaviour near their phase transition temperatures. The implication of the chirality is the introduction of a macroscopic helix. Due to smectic layer-to-layer interaction, the tilt ordering of the chiral molecules (and therefore the spontaneous polarisation) precesses in
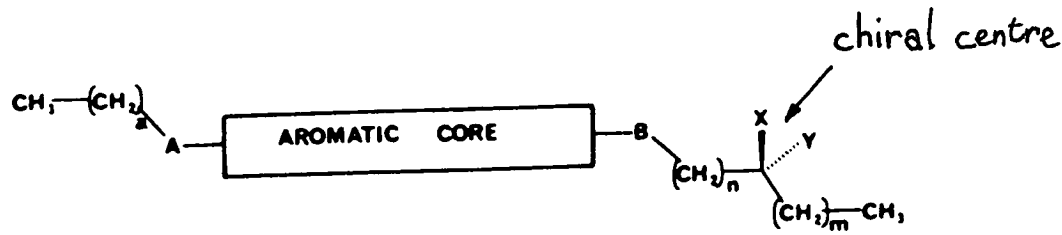
Figure 2.3: A typical FLC molecule, A is O, B is COO

a helical fashion (figure 2.2). This is a lowest energy configuration for the bulk material. For useful ferroelectric properties in device applications, the helix must in general be suppressed. Otherwise the average dipole and the average spontaneous polarisation is macroscopically zero.

2.3 Material Considerations

It is worth-while to consider for a moment the material design which has been employed to generate useful molecules for FLC properties [62]. The chiral molecules need to pack into layers with their long-axis tilted at useful temperatures. Exhaustive research has resulted in some general rules for the kinds of molecules which are useful. In general these molecules consist of a rigid aromatic core and two flexible terminal alkyl chains. On one of these alkyl chains there is a chiral centre. To induce the dipole, certain atoms are attached to this chiral centre. This dipole causes the spontaneous polarisation perpendicular to the long-axes direction. The chiral centre plays a very important part in the resulting physical properties, affecting the spontaneous polarisation, helical pitch length, helical twist sense and the phase transition sequences and temperatures. For most practical purposes, mixtures of FLC materials are used to obtain improved performance [54]. An example of a FLC molecule is shown in figure 2.3.

Unfortunately, the complexity of the interactions in mixtures has not allowed the result of the mixing process to be fully understood. One of the most common mixtures for optimised properties involves mixing an achiral smectic C host with a small amount of chiral

dopant. It is generally held that for good FLC alignment, the phase-transition sequence $I - N - S_A - S_C$ is most useful. I represents the isotropic phase (essentially a liquid), N the nematic phase and SmA/SmC the smectic phases. Material exhibiting transitions of $I - N - S_C$ have also been designed. The design of FLC matérials and mixtures is still relatively a 'black-art' as there is not a sufficiently thorough theoretical description of FLCs. An example of phase transitions for the FLC mixture SCE13 (Merck-BDH) is given below:

$$I^{105^\circ} - N^{85^\circ} - S_A^{65^\circ} - S_C^{5^\circ} - solid$$

Material purity is a very important issue. Ionic impurities are of particular concern. Ionic charges lower the resistivity of the FLC material, causing charge leakage [64]. Arguably, their most damaging effect is when they build up at the FLC/bounding plate interface [65]. If sufficient charge build-up occurs, any switching ability in the FLC material is lost due to the opposing field created (depolarisation field). This means that long term application of d.c. voltages will be detrimental to the performance of FLC devices. As completely pure and uncontaminated samples of FLC material are extremely difficult to obtain and ions can be introduced by the bounding plates, d.c. balancing must be applied to retain longevity of the device i.e. the overall voltage across the material, integrated over time, must be zero. The practical implication is that any +ve voltage/time pulse applied to the device must be complemented with an equal -ve voltage/time pulse. This has major consequences for practical FLC device addressing techniques.

2.4 Theoretical Models

There are numerous theoretical approaches one can take toward FLCs [66]. Three of the most useful to gain insight are a thermodynamic approach, studies of the molecular switching dynamics and comparisons with the ferroelectric capacitor. Thermodynamic models can explain the structure of the various phases and the spontaneous polarisation. Molecular dynamical models describe the electrical and optical switching characteristics. Useful models of ferroelectric capacitors exist which can be used to examine some of the

electrical properties of FLC devices. The theoretical models are discussed in more detail in appendix A. None of these models has been fully completed [54]. It is hoped that some form of unification of these approaches can be found. But perhaps a description of FLC devices considering surface, electric field, elastic and viscous effects will result in a too complicated model to be readily useful for device design.

2.5 FLC Alignment

Some confusion may arise with the term FLC alignment. It describes two closely related concepts. Firstly, what the actual observed alignment of the liquid crystal molecules is and secondly, how that alignment is achieved. The discussion here concerns the latter meaning i.e. what techniques can be applied so as to (hopefully) arrange the liquid crystal molecules into a useful device structure. Such techniques consist predominantly of anisotropic surface treatments to change the boundary conditions at the bounding electrodes in the device [67, 68]. The specific boundary conditions at this interfacial layer causes structures and orientation in the bulk LC. (It is well known that in nematic LCs, alignment techniques can be used to obtain structures such as the twisted nematic device. Different directions of the prefered LC director orientation at each bounding plate causes the director profile to twist in a helix from one plate to another in the bulk material.)

2.5.1 Alignment Techniques

In FLC devices, there are essentially two reasons for the use of alignment techniques. The first is similar to that required in the nematic devices i.e. to specify a preferential director orientation for parallel smectic planes. The second, is to suppress the helix obtained in the FLC bulk and obtain only two bistable director orientations in a Surface-Stabilised FLC (SSFLC) device (section 2.6). Simplified, the boundary conditions can be characterised by two parameters, the average angle of the molecules to the plane of the surface (Θ_o) and the anchoring energy (W_s). Using the angle one can distinguish two ideal molecular surface orientations, planar ($\Theta_o = 0$) and homeotropic ($\Theta_o = \frac{\pi}{2}$).

In most practical cases the molecules are tilted ($0 < \Theta_o < \frac{\pi}{2}$) but for simplicity may be considered either planar (homogeneous) or homeotropic. For the anchoring energy, two idealised regimes can be considered, strong anchoring ($W_s \rightarrow \infty$) and weak anchoring typically of order $W_s < 10 Jm^{-2}$. For the purposes of this study only planar alignment will be considered. Originally the shearing of the bounding plates or magnetic fields were used to align the molecules [69]. But these techniques are not very practical for VLSI backplane SLMs. More practical methods to achieve alignment of the molecules are to apply anisotropic treatment to the bounding plates in the device. Techniques for anisotropic surface treatment include [61, 70]:

- Mechanical rubbing of nylon, PVA or some other electrode coating in one direction. The rubbing creates a microrelief structure in the electrode coating in the form of ridges and troughs and/or preferred dipole direction in the electrode coating.

- Oblique evaporation of metals or oxides which results in a variety of useful surface micro-profiles which give preferred orientations, surface pretilts and energies.

- Polishing of the electrode surface in one direction to obtain a microrelief structure.

- Etched periodic structures using photolithographic techniques.

- Langmuir-Blodgett films allow homeotropic alignment through molecular interaction between the LC molecules and the film molecules.

These alignment methods cause either a preferred orientation due to the minimising of the LC elastic energy when in contact with the surface or alignment by dipole interaction [67]. One can idealise that the molecules prefer to 'fit in' at the surface [71]. This surface interaction is transferred to the bulk material. The shape and scale of the surface structures can be examined to estimate the surface energy which is transferred to the LC. In general, the smaller the scale of the structures, the greater the surface energy [68]. This can be thought of as due to a greater surface area being in contact with the LC material. Rubbing techniques tend to result in relatively large structures and are therefore generally considered to generate weak surface anchoring. Oblique evaporation causes much finer structures and results in strong surface anchoring [70].

2.5.2   The conductivity of the alignment layers

The conductivity of the alignment layers is an important parameter [72, 64, 65]. Appendix A describes how a high spontaneous polarisation would give fast switching speeds. However, recent studies indicate that FLCs with high spontaneous polarisation do not exhibit bistability. This has been due to the build up of ionic charges at the FLC/alignment layer interface, causing a depolarisation field (section 2.3). This depolarisation field results in a rapid relaxation of the bistability when the external field is removed. The injection of +ve and -ve charges into the FLC material from the alignment layer can provide a mechanism to neutralise this depolarisation field. This can be achieved by using thin and/or conducting alignment layers. This provides a further consideration in the selection of alignment layers. However, conducting alignment layers covering all of the modulation elements will cause charge leakage between each element (cross-talk), which should be avoided [73].

2.5.3   A.C. field stabilisation

Careful selection of the alignment layers can allow stable switched states. If this is not achieved, the molecular direction can relax to some unspecified state when driving voltages are removed. This can result in a reduction of the optical contrast in the cell [74]. Poor surface alignment stabilisation can be compensated for with a.c. field stabilisation. The applied field must be above the relaxation frequencies of the FLC so as not to excite any mode oscillations in the dipole [75]. The high frequency a.c. field is applied after d.c. switching pulses, this makes the switched states more stable and the relaxed switched state angles are very similar to the driven state angles. The reason for improved device performance caused by the application of high frequency a.c. fields is due to a complex interaction with the biaxiality of the FLC molecules in the bulk [76]. Typically, waveforms of 100kHz and 50V pk-pk have been applied to attain this stabilisation improvement in thin cells[75].

2.6   The Surface-Stabilised FLC Device

The SSFLC structure has been of considerable interest for optical modulator devices due to its increase in speed and contrast compared to nematics. The device structure was first demonstrated by Clarke and Lagerwall in 1980 [69]. The smectic C class of structure is identified by the molecular tilt from layer to layer, resulting in no rotational symmetry. The SSFLC device uses the smectic C* phase with a thin cell and surface alignment to suppress the formation of the helix. Originally a simple bookshelf structure was expected in the smectic C* phase, as in the Smectic A phase. The bookshelf structure has uniform smectic layers perpendicular to the bounding plates. The observed structures can be much more complex with such phenomena as tilted smectic layers, chevrons and splayed chevrons depending on both the bulk properties and surface anchoring. The reality is further complicated by the presence of other kinds of defects. SSFLC is a special case where the spontaneous polarisation can only point in two directions. The structure can be achieved by applying external boundary conditions on the FLC intermolecular interactions, producing a more ordered structure than would normally be expected. The various LC alignment techniques can be used to obtain the condition. Clarke and Lagerwall originally used a shearing force on the bounding plates to unwind the helix. In a similar manner LC alignment techniques and a sufficiently 'thin' cell can allow enough energy to be transferred to the bulk to allow only two degenerate states to be energetically favourable (figure 2.4), resulting in the bistable nature of SSFLC switching [77]. The alignment layers in the SSFLC device is therefore crucial and careful selection of alignment techniques is required for optimum performance. Subsequent work by Clark and Lagerwall has demonstrated that much more complicated SSFLC device structures are possible. For example the director profile need not be spatially uniform, the smectic layers need not be normal to the bounding plates and molecular surface interaction need not be parallel to the surface plates. By employing, alone or in combination, non-planar or polar boundary conditions, boundaries with multiple physical states, intrinsic spontaneous splay distortions of the polarisation orientation field, combined ferroelectric and dielectric torques and layers tilted with respect to the boundary plates, one can obtain ferroelectric smectic structures with monostable, bistable or multistable states. Such complications have serious consequences for the generation of unwelcome defects in the simple SSFLC structure.
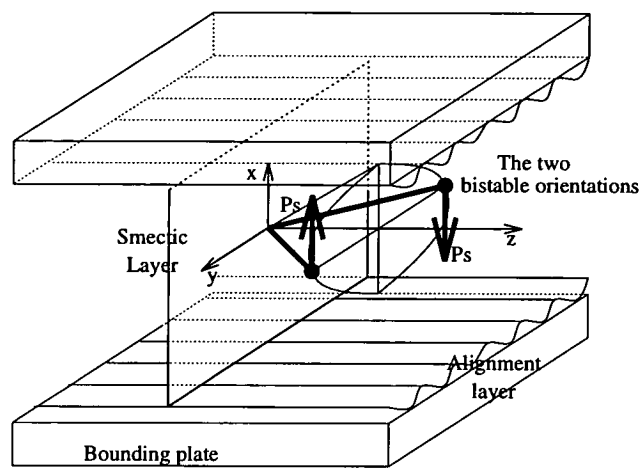
Figure 2.4: The SSFLC device structure

2.7 SSFLC optical modulation

The SSFLC device structure results in the reduction of the degeneracy of the director direction to two bistable states where the polarisation is nearly perpendicular to the plates. Positive and negative voltage pulses can switch the orientation between these two states [34]. The director can thus be switched through twice its director tilt cone angle θ parallel to the boundary plates. The cone angle is temperature dependent (Appendix A). Due to the optical anisotropy of the FLC molecule, birefringence is obtained. The axis of the birefringence can be switched between two orientations seperated by the angle 2θ [78].

2.7.1 Amplitude Modulation

In this simplified representation, the SSFLC device has two bistable orientations of the optical axis of its birefringence. By careful selection of FLC material, different optical tilt cone angles can be obtained. A switchable **ON/OFF** half-wave plate can be obtained by selecting a FLC material with 22.5° cone angle. Therefore, the optical axis can be switched by 45°. An amplitude modulator can be obtained by configuring the polarisation vector of the incident with the axis of one of the switched states. An analyser (crossed polariser) at the output will block the light output from the device. By switching the

OFF STATE   ON STATE (Half-wave plate)
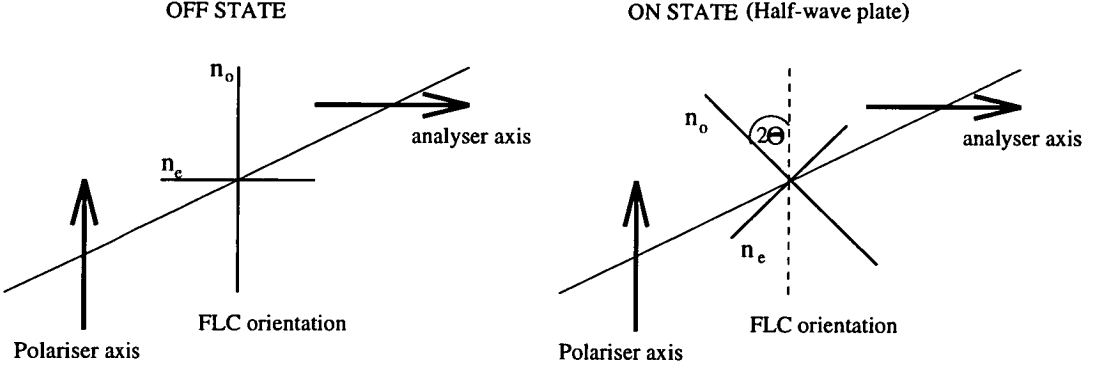
Figure 2.5: Optical intensity modulation with the SSFLC device, θ is the FLC cone angle, n_o, n_e are the ordinary and extraordinary refractive indices

modulator to its other state, the FLC acts as half-wave plate and the polarised light is rotated by 90° and is not blocked by the crossed polariser (figure 2.5). Thus the birefringent FLC material can act as a switchable uniaxial medium. The transmission of this device between crossed polarisers is given by [11]:

$$I = I_o sin^2(4\varphi) sin^2(\frac{\Delta n d\pi}{\lambda})$$

(2.1)

where I is the output intensity, I_o is the input intensity, φ is the angle of the alignment with the first polariser, Δn is the birefringence, d is the thickness of the FLC material and λ is the wavelength of light. The smectic C* material is weakly biaxial but for most purposes can be considered uniaxial.

The contrast ratio, the ratio of light intensity between the two switched states, is theoretically infinite. Practically, the contrast ratio is dependent on cell/polariser quality. Therefore, it is limited by director alignment uniformity, LC defects and ultimately polariser/analyser efficiency.

2.7.2   Phase Modulation

There are two methods of phase modulation with the SSFLC device. The first has one optical axis parallel to the polarisation vector of the incident light. When the molecule rotates, the incident light passes through the medium with a different refractive index

ZERO PHASE DIFFERENCE   PI PHASE DIFFERENCE

n_o n_o

Θ Θ

analyser axis   analyser axis

n_e n_e

FLC orientation   FLC orientation

Polariser axis   Polariser axis
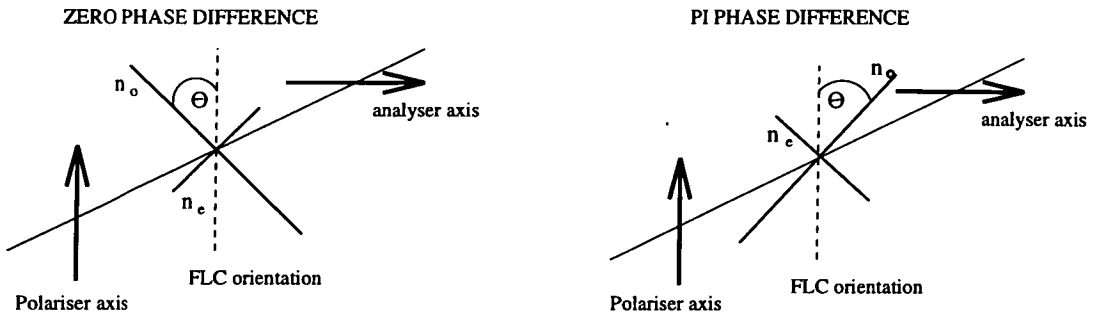
Figure 2.6: The second technique for phase modulation in the SSFLC device

dependent on the rotation angle [59]. The phase difference is dependent on the angle and the birefringence. In the second method, the incident direction of polarisation is configured to be between the two directions defined by the FLCs switchable optical axis [59, 79]. The propagation of light through the liquid crystal produces elliptically polarised light from the incident linear polarisation, the sense of the polarisation depending on which side of the optical axis the incident light falls. The state of elliptical polarisation depends on the angle between the optical axis of the molecule and the incident polarised light (figure 2.6). If the angle is 45° then the result is linearly polarised light but in opposite directions in each of the switched states. The two states of elliptically polarised light then pass through a second polarised, orthogonal to the first, which reduces the elliptical polarisation (general case) to linear polarisation states exhibiting a relative 0 or π phase difference. This is illustrated in figure 2.6. For 100% transmittance in each switched state, a FLC material switching through an angle of 90° (cone angle 45°), and a delay due to Δn, d and lambda resulting in π is required. No analyser is needed in this situation.

2.8 Ferroelectric Liquid Crystal Defects

Defects in FLC devices, particularly in the SSFLC structure, cause deviations from ideal operation characteristics. A defect is a perturbation of molecular direction in a portion of the FLC structure. In general, this is caused by elastic forces due to inhomogenieties in surface alignment or by molecular reorientation at phase transitions.

2.8.1   Tilted Layers

Usually the smectic layers in a thin SSFLC device are tilted with respect to the boundary plate normal, [80] due to some pretilt of the surface molecules associated with the particular boundary conditions. As a result, the director is not parallel to the boundary plate, and only a projection of the director is effective in switching and optical modulation. This has consequences in reducing the optical throughput of the device as full half-wave plate switching in not achieved [81].

2.8.2   The Chevron Defect

The most common defect found in SSFLC Smectic C* devices is the chevron defect [82, 83], caused by a shrinking of the smectic layers on cooling to the Smectic C* phase, from the Smectic A phase, while anchored to the bounding plates [84]. Normally one would expect a bookshelf or quasi-bookshelf structure in the smectic layers, but in this case, zig-zag defects can be observed in the SSFLC cells when viewed under polarising microscope [85]. These defects consist of narrow domain walls running in a zig-zag manner nearly normal to the smectic layers and broad walls running parallel. The walls separate regions of uniform but different optical contrast, suggesting that the smectic layers are not normal to the bounding plates and have a tilt angle. In fact, the smectic layers themselves are distorted. This defect was first fully explained and studied by Clark with high resolution x-ray scattering [83]. The local smectic layer structures were probed to show that a chevron kink had formed [86]. The molecules make an abrupt reorientation at a planar interface parallel to the bounding plates [87]. At the upper and lower portions of the cell the layer tilt is in the opposite direction. As this chevron kink can be in one of two directions, the domains are regions of similar direction chevron structure. The zig-zag defects are the transition areas (domain walls) between the two directions of kink. Where the transition is from smectic layer to layer the domain wall is thin, but where the transition is along the same smectic layer, the domain wall can be much thicker due to the twisting of the smectic layer. The formation of the chevron kink is just below the SmA-SmC phase transition temperature due to the reduction of the layer spacing at the phase transition temperature. The various orientations of the chevron kink and the resulting domain walls are shown in figure 2.7. The 'thin' domain
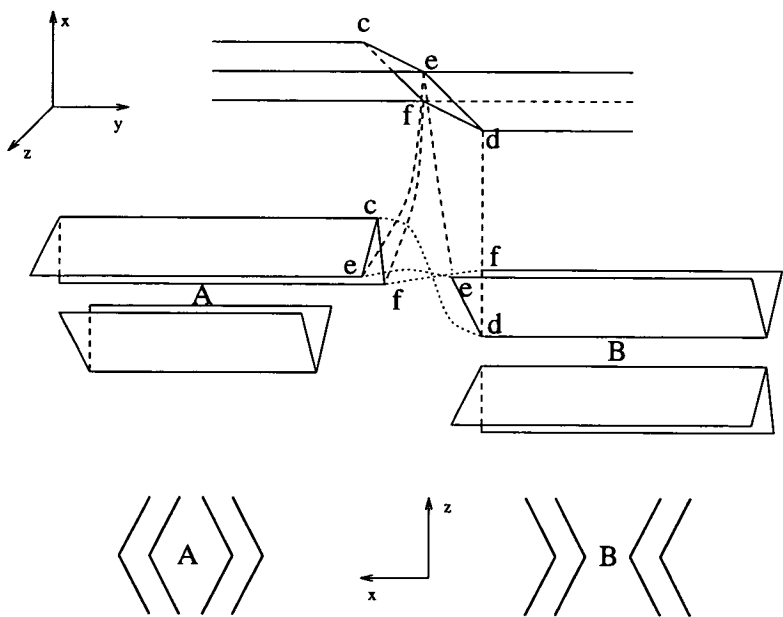
Figure 2.7: The origin of the chevron defect

walls are at **A** and **B**, and the thicker domain walls at the **c,d,e,f** locations. The two types of walls and two potential orientation of each, result in nonsymmetric shaped domains such as the **Bear Paw** and **Teardrop**, shown in figure 2.8. Needle defects usually result from rapid change in chevron kink direction. The optical modulation in each domain have different extinction angles due to the different projection angle which the molecular directors make with the bounding plates [88]. This results in four possible switched states to be observable in the cell, two for each domain. Under white polarised light illumination, these regions have slightly different colours, and exhibit the defect features shown in figure 2.8. Macroscopic contrast measurements are thus very low in such a condition, typically $< 10 : 1$.

Due to the interaction energy and increase in degeneracy, the switched states in the chevron structure are not generally wholly bistable, and one state in each domain is usually preferred when the driving voltage is removed [89]. The consequences of the chevron defect are very undesirable: reducing the contrast considerably, no or little bistability is evident and the relaxed state of each domain is indeterminate. Two methods have been found to minimise or remove the effect of the chevron defect. Antiparallel small angle deposition alignment (section 3.3.3) at the bounding plates induces a pretilt at the surface which in the bulk suppresses the formation of the chevron kink, but results in a
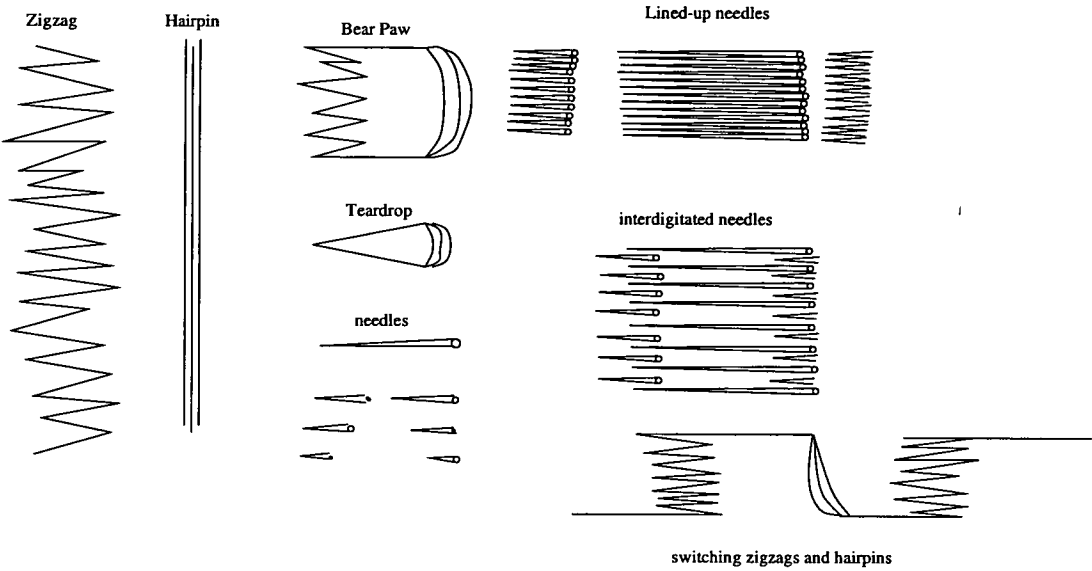
Figure 2.8: The various consequences of the chevron defect

tilted bookshelf structure and a slight reduction in contrast and modulation efficiency. The most common technique involves the application of low frequency a.c. treatment fields which induce the surface anchoring to rearrange slightly and reduce the chevron kink to a bookshelf structure (section 3.4) [90, 89, 91, 92].

2.8.3   Striped texture

Striped texture is observable in the chevron defect structure due to long narrow regions of different domains [93, 94]. In some cases the stripes can cover the whole of the sample. As well as the stripes, the other chevron domain defects are usually apparent. With a.c field treatment, the chevron kink is reduced and eventually removed resulting in the chevron domains disappearing, but the striped texture usually remains faintly. This can be visualised in figure 2.9, where as the chevron kink with striped texture is reduced through field treatment, the memory of the stripe is retained as an undulation of the smectic layers along each layer. This is probably the resulting bookshelf structure obtained on the realignment of the surface anchoring. Perhaps, the structure results from nonparallel alignment of the alignment layers on the two bounding plates. Any deviation from complete parallel orientation would allow a slightly different preferred
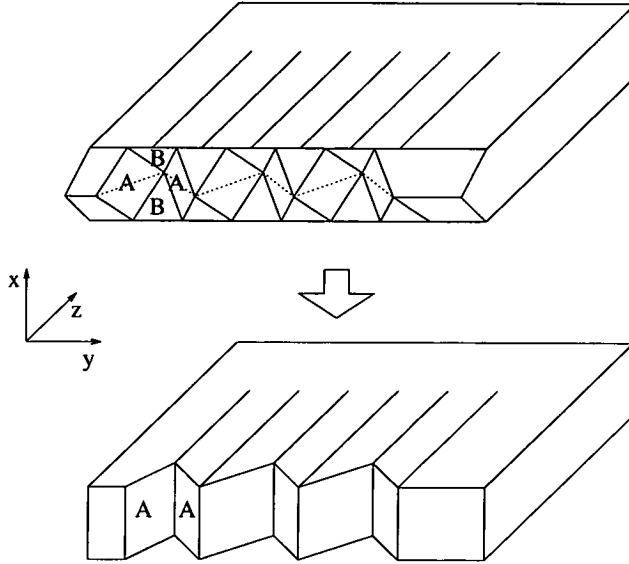
Figure 2.9: The origin of the striped texture

director orientation direction at each bounding plate. It is the author's opinion that completely parallel alignment of the top and bottom plates is practically impossible to obtain and some deviation will always be present. The striped texture can be difficult to observe, suggesting that the undulation is very slight. The contrast of the striped texture in the bookshelf structure is typically $> 100 : 1$. Observation of the contrast in each individual stripe by microspot shows the contrast to be $> 10,000 : 1$ [93]. Therefore, the faint striped texture tends to limit the contrast of bistable, bookshelf structures constructed using surface aligning techniques. It is not known if any techniques can be used to alleviate this situation.

2.9   Grey levels

An important requirement for some applications is that the optical modulation is analogue in nature. The idealised SSFLC device is inherently bistable, but some techniques have been employed to produce grey levels from binary switching [54]. In general, this has involved some time or spatial integration of binary switched pixel elements. Multipixel elements have been fabricated with unequal elements. By switching a portion

of the multipixel a spatially integratable grey level capability is attainable. For large arrays of grey level multipixels, an even larger area of addressable elements is required. The number and shape of the subpixels defines the number of grey levels available. An alternative approach uses time-multiplexing. With the persistence of human visual processing or through integration at detection, a number of sub-frames can be coded to allow grey level frames by dithering. If a pulsed light source is employed in the system the number of sub-frames can be reduced for a given number of grey levels. Generation of grey levels by coding both the sub-frames spatially and the light source pulse width has been demonstrated by Burns [95].

Both of these approaches reduce the performance of the SLM device by either reducing the resulting resolution or the frame-rate. A more interesting, although relatively ignored technique, involves charge metering and isolation on the modulation pixel [96]. This can be used in a pre-latching mode, where not enough charge is delivered to the FLC material to allow latching into a bistable state, or in a texture method, where the growth and change of multidomain defect structures in the device is exploited. At present these techniques do not result in reproducible grey level values as the surface energies which play a crucial role and the switching mechanisms are not fully understood. To implement such analogue switching on VLSI silicon certain problems need to be overcome. As with all FLC devices, charge balance must be maintained across the material. Analogue voltage addressing circuits retaining this charge balance must be designed. The temperature dependence of the cone angle will certainly be a problem for applications where grey levels must be accurately defined.

2.10   Distorted Helix FLC Device

Interest in the so-called Distorted Helix Effect (DHE) in FLCs has been due to its proposed application as a fast analogue switching device [97]. As was described in section 2.6, the SSFLC device configuration is ideally bistable and thus unable to supply directly analogue grey levels. This is not strictly true as was discussed in the previous section. The physical device structure of the DHE is generated when the cell boundary conditions are such as to allow the formation of the bookshelf structure (i.e. parallel smectic planes

NO Field   smectic layers   Field Applied
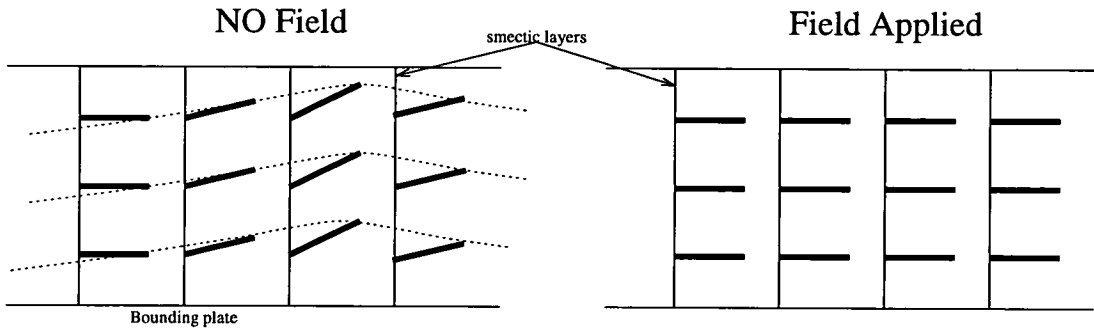
Bounding plate

Figure 2.10: The structure of the Distorted Helix Effect device

perpendicular to the cell bounding plates), yet not to inhibit the helical precession of the director from smectic layer to layer. The strong boundary interactions in the SSFLC device specifically suppress this helix to produce only two degenerate states. [In general, these boundary conditions are not useful to achieve the DHE device structure.] The required director structure for DHE has been obtained with short-pitch FLC mixtures using weak surface interaction. This has resulted in a FLC cell where the helix pitch is smaller than the wavelength of light and an apparent birefringence, averaged over the helix, is observed. The application of external applied field distorts (unwinds) the helix and thus changes the birefringence (figure 2.10). This change is manifested in a rotation of the ellipsoid of refractive index and a change of value of Δn, causing both an amplitude and phase modulation. At a certain critical field, the helix becomes completely unwound and the device shows SSFLC behaviour i.e. quasi-bistability no analogue response. The best device results noted from the literature are a contrast ratio of 40:1 (for an irreproducible sheared cell) and a switching speed of $2\mu S$ (achieving a 15 percent change in transmission) for 6 Volt pulses [97].

2.11   Soft-Mode Electroclinic FLC Device

The smectic A class of structure is identified by the rod-like molecules having long-axes orthogonal to the smectic layers with rotational symmetry around the normal to the layer. The electroclinic effect is a field-induced molecular tilt found in chiral orthogonal smectic phases [98]. The tilt is a soft mode of the Smectic A* phase [99, 100]. The effect can be found weakly in a variety of smectic phases but material has been designed to
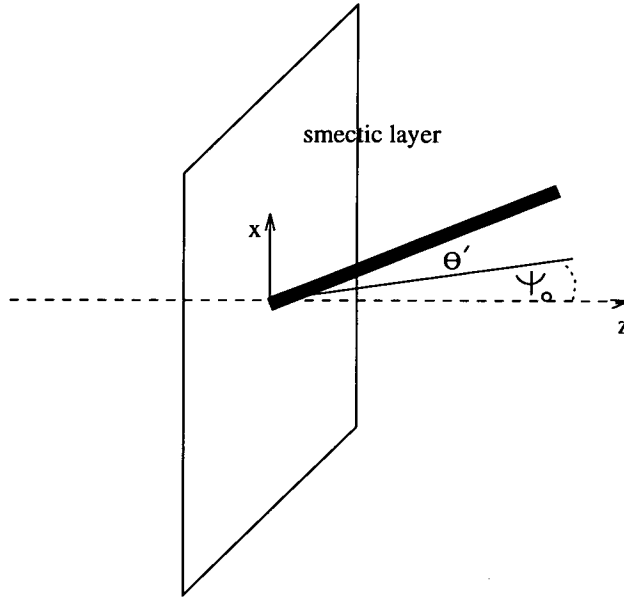
Figure 2.11: The structure of the Soft-mode Electroclinic Effect device

exhibit large induced tilt angles [101]. The induced molecular tilt θ is a linear function of the field E, but the response time is independent. These points are particularly true well away from the transition temperatures. The effect has no memory or bistability and has application as a analogue modulator device. The electroclinic effect was first proposed by Garoff and Meyer [98]. Originally suggested as a pretransitional effect near to the phase transition A*-C*, it has proven to be useful far from the transition. There is no critical slowing as in SSFLC devices, where as the switched state is reached there is less interaction with the field, and so the response can be made faster than any other LC electro-optic effect so far discovered. The molecules are structured in the bookshelf geometry, in a thin cell. An electroclinic device has a number of attractive electro-optic characteristics. There is a reduced temperature dependence compared to other FLC devices. At a constant response time, the field can be used to control the tilt angle, giving a continuous analogue response. This is because the response time is independent of both the field and the induced tilt. As no surface stabilisation is involved, the cell gap is not so critical as in the SSFLC device. The response time is given by:

$$\tau = \frac{\gamma}{\alpha(T - T_c)} \tag{2.2}$$

where γ is the viscosity coefficient for the θ motion, α is a constant, T is the temperature and T_c the phase transition temperature. Therefore the response is dependent on both

temperature and (tilt) viscosity [99]. The value of the response time is generally in the submicrosecond range and has been quoted as $50nS$ [101]. Linearity of the electroclinic effect is lost at high fields and near the phase transition temperature T_c.

The ideal case for electroclinic optical modulation is a uniform cell consisting of a chiral Smectic A FLC in a bookshelf geometry. With crossed polarisers orientated parallel/perpendicular to the smectic layer normal, the intensity of light through the cell is:

$$I = I_o sin^2 2\psi sin^2 \frac{\delta}{2} \tag{2.3}$$

with $\psi = \psi_o + \theta'$, where δ is the optical phase difference and θ' is the projection of the induced molecular tilt on the normal to the smectic layer (z-axis). The angle ψ is angle between the projection of the director and the transmission direction of the polariser (on x-axis in figure 2.11). By correct selection of the parameters the condition for a half-wave plate can be achieved, as in the SSFLC case. The intensity modulation transmission can therefore be described by:

$$I = I_o sin^2(\psi_o + \theta(E)) \tag{2.4}$$

The major drawback with linear soft-mode modulation is the poor contrast attained with currently available materials. This is due to the relatively low tilt angle available. e.g. a tilt of 5° gives only a contrast ratio of 2:1, but for a high throughput of light . For very low throughput ($< 10\%$), very high contrasts can be achieved at the expense of efficiency. Values as high as 2000 : 1[101] have been measured for low levels of transmitted light. The contrast can be enhanced by increasing the angular swing with higher voltages and leaving the linear domain. The material then acts more like a SmC* device and mixed soft-mode and cone switching (SSFLC) is observed. This can increase the contrast to what would be expected for a SmC* device i.e. only dependent by the cell/polariser quality, the homogeneity of the director alignment and the number of defects present. In this arrangement, values of 50:1 have been quoted in the literature [101]. Therefore, it is unlikely that with current materials it is possible to induce the tilt angle much further than 10°, except near the phase transition temperature where the response is slow and strongly temperature dependent. Some useful techniques using multiple cells to reduce this problem are described in the literature [102]. Unfortunately such techniques are not easily applicable to VLSI silicon backplane SLMs.
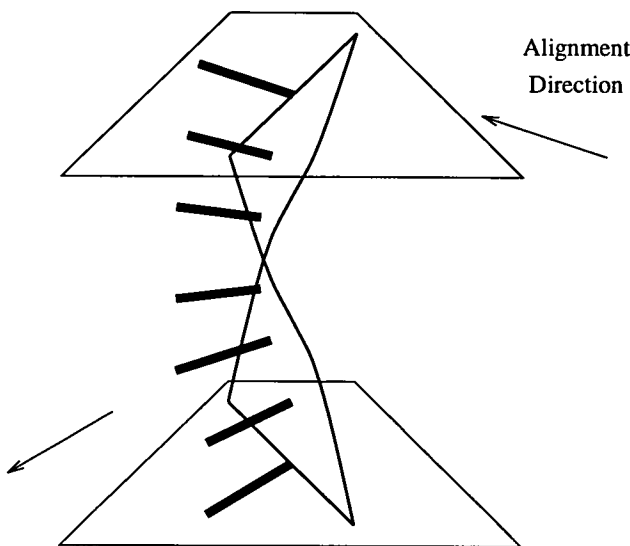
Figure 2.12: The structure of the Twisted Smectic Device

2.12 Twisted Smectic Structure Modulation

This effect was first described by Patel[103] and has had comparatively little written about it. In a twisted nematic device structure polarised light is 'wave-guided' through the twisted structure [104]. Light modulation is attained by destroying the wave-guiding effect when the cell is placed between crossed polarisers, to cause extinction. A similar structure can be produced in smectic liquid crystal phases. By making the anisotropic boundary conditions at the electrodes orthogonal, the molecules will twist by 90° from one bounding plate to the other (figure 2.12). The molecules are co-planar at the bounding plates but deviate from this plane in the bulk and are constrained to the surface of a cone. The polarisation direction is constrained to lie in the plane of the smectic layer and be normal to the director, so the polarisation P rotates by 180° going from one surface to the other. With the application of an external field this rotation of the polarisation can be destroyed in the bulk and no wave-guiding occurs. With low fields (typically $< 1V/\mu m$) applied, an incomplete destruction of the wave-guiding is observed which can allow analogue switching. Contrast ratios of 25 : 1 with $2V$ pulses and similar switching times to SSFLC devices have been reported [103].

2.13 Summary

This chapter has served as an introduction to the wide subject of FLCs. Some of the theoretical models were discussed with a view to giving some useful insight into the practical issues concerning FLC devices. Some of the possible device structures, their use and potential as modulators were described. The background to the SSFLC device would seem to be the most mature. Other analogue and potentially faster FLC devices were introduced and they certainly warrant some further investigation. For high contrast binary switching, the SSFLC structure would seem most suitable for digital logic SLM backplanes. If faster switching is required then the soft-mode device should be useful, but at a cost of much lower contrast ratio. The soft-mode or the DHE device could be applied to analogue SLM backplanes, although at present none have so far been designed. The background to FLC devices has been discussed, and it has been shown to be a wide and highly complicated topic. But what can be practically achieved within the bounds of this study? Table 2.1 describes a selection of SSFLC devices from the literature. The table demonstrates the wide variety of techiniques and results obtained from device development. In general, the alignment quality seems to be under most investigation and post-filling electrical treatment commonly applied. This table serves as a useful introduction to the next chapter, where the fabrication of FLC devices will now be introduced. This review of FLC topics suggests the following:

- FLC devices have an inherently higher performance than nematic LCs.

- However FLC devices have a different mode of operation and potentially greater influence from defects.

- The SSFLC device structure has been identified as having great potential for binary modulating SLMs.

- The expected performance and potential problems associated with this device structure were identified.

- Three other FLC device structures were studied, although in the literature they appear to be less developed than the SSFLC.

- The preliminary investigation will allow device fabrication to proceed with a firm understanding of the basic concepts and experience from other researchers.

Year	LC type	Cell Spacing	Alignment	Cell treatment	Performance
1988	CS-1011 (Chisso)	$1.4 - 2.4\mu m$	60° evap. Y_2O_3 or Al_2O_3, 200nm	d.c. or 100Hz, 10^7V/m while cooling	$250\mu s$ switching,[105] bistable
1989	CS-1011 (Chisso)	$2\mu m$	prerubbed polyimide	none	$C.R > 40:1$ [16] defect free
1989	SCE4 (BDH)	$3\mu m$	rubbed nylon	$10 - 50$ Hz, 20 V	defects removed [89]
1989	MOPOP	$2\mu m$	85° and 75° SiO, 50nm	none	few defects [106]
1991	CS-1024 (Chisso)	$1.7 - 1.8\mu m$	85°, 30nm SiO	100 Hz, 30V	C.R. 50:1, [107] bistable
1991	ZLI3654 (Merck)	$1 - 3\mu m$	$60° - 85°$, 10-100nm SiO	100 Hz, 10V/ μm	Good alignment [70] bistable
1991	ZLI-3654 (Merck)	$5 - 20\mu m$	Rubbed Polymer	100V, 1kHz, 2hrs ($^+_-5$ d.c.)	x-ray shows [86] no chevron

Table 2.1: A selection of SSFLC devices

Chapter 3

FLC Cell Fabrication

The subject of FLC modulator devices has been introduced in the previous chapter. To investigate further the possibilities of the application of FLCs to SLMs, one must consider the fabrication of useful modulation structures. This chapter will make a systematic investigation into the fabrication and appraisal of simple FLC test cells. The aim of the study is to attain a level of confidence in construction of cells before proceeding to full SLM devices on VLSI backplanes. Many of the fabrication options are discussed in appendix B. Appendix B should be regarded as a 'Users Guide' when one is familiar with the concepts. The literature abounds with descriptions of FLC cell investigations but very little detail on fabrication can be extorted. This is mainly due to the sensitive commercial nature of the technology. This study has therefore been built upon previous experience in the Applied Optics Group, at the University of Edinburgh, concerning Nematic LC cell fabrication [108, 104].

Techniques for the appraisal of FLC devices will be developed. Studies of possible alignments layers, the resulting liquid crystal alignment, cell treatments, optical measurement and electrical measurement will be detailed. This preliminary work will assess the various options in device structure and select structures suitable for more detailed examination in the following chapter.
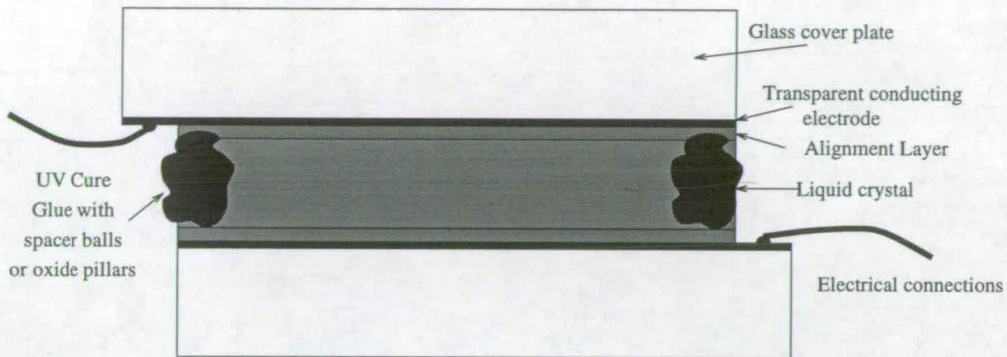
Figure 3.1: Schematic of a Ferroelectric liquid crystal test cell

3.1   Ferroelectric Liquid Crystal Cell Fabrication Techniques

The idealised FLC test cell is shown in figure 3.1. For transparent cells, two glass substrates are separated by a suitable spacing technique. On each glass substrate a transparent conducting electrode is deposited to allow electrical connection to the FLC material. On top of the electrode an anisotropic alignment structure is required to give the boundary conditions for the FLC material. FLC fills the gap between the two glass substrates. Each element in this idealised test cell has a number of options. With regard to FLC/VLSI SLMs, particular attention must be paid to the suitablity of such techniques.

3.1.1   Fabrication Environment

A clean room or clean space is required for successful cell fabrication. A sketch of the Applied Optics clean room is shown in figure 3.2. Airborn particulates and surface contaminants are all detrimental. Dust particles can be of the order of $10\mu m$ in size which is not conducive to the production of thin cells. Any surface contamination will adversely affect surface deposition adhesion and also disturb FLC alignment. All FLC cell fabrication was therefore performed in the Applied Optics clean room. Other precautions included the use of the ionising filtered nitrogen gun and substrates were kept 'wet' before
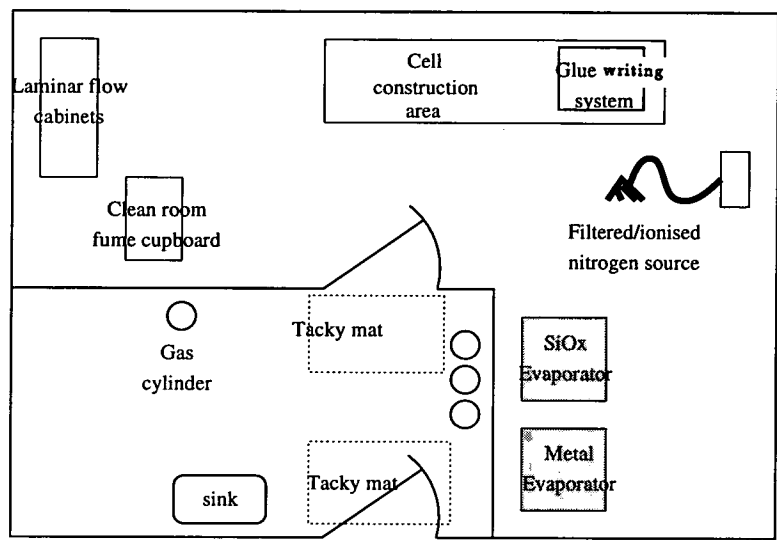
Figure 3.2: Elements of the clean environment

use. As a general rule, substrates were not left for any extended period exposed to the air. Any such exposure, such as during mechanical cell construction, was performed in the cleanest regions of the room, just in front of the laminar flow cabinets. Much effort has been employed to improve the quality of the clean room environment.

3.1.2 Cleaning

The cleaning of substrates is of critical importance to fabrication. As most of the substates employed in the investigations have come from external sources, it has been found necessary to have a standardised cleaning technique. Appendix C summarises the cleaning options. These can essentially be partitioned into two groups, organic based cleaning and inorganic based cleaning. Organic based techniques tend to be more 'substrate friendly' and have therefore been the most generally applied. Organic solvents subsequently blown from the substrate with the ionised filtered nitrogen gun have been found to be the most suitable. The substrate progresses through steps of ultrasonic cleaning in the solvents before the final solvent is blown off with the nitrogen gun. It is important that at no intermediate step is the substrate allowed to 'dry', as this will result in material deposition. The test for a clean substrate is that deionised water should form a sheet over the substrate and not form droplets. Inorganic oxidising liquids such as acids

can be used for destructively removing surface contamination, but care must be taken that the substrate is not unduly damaged.

3.1.3 Glass Options

Initial fabrication studies were performed using glass microscope slides which were coated with an Indium Tin Oxide (ITO) transparent conducting electrode in-house by the Physics Department Techniques Lab (E.Davidson). A number of problems were encountered with these samples. Perhaps the most important was the low quality of the deposited ITO layer. This is hardly surprising as ITO is a very sensitive material to deposit as a thin film. Also, the glass slides tended to be too flexible causing very non-uniform cell gaps. It was therefore deemed necessary to seek high quality ITO coated glass from external sources. Two types of optical flat glass, coated with high quality ITO, were acquired. A thick variety ($6mm$) and a thin variety ($1.1mm$) seemed most suitable. For the thin glass, the optical transmission ($\lambda = 633nm$) was measured at $85^{+}_{-}2\%$ and the resistivity measured at $30^{+}_{-}3ohms/cm$. For the thick glass, the optical transmission ($\lambda = 633nm$) was measured at $82^{+}_{-}2\%$ and the resistivity measured at $90^{+}_{-}3ohms/cm$. The thicker glass was diced into cubes for ease of initial SLM fabrication. The thinner glass has been the most useful, allowing easier optical access to devices, but with a slight increase in fabrication complexity.

3.1.4 Spacer Layers

In Nematic LC cell construction strips of polythene sheeting ($10\mu m$ thick) were employed previously as the spacer material. For FLC cells, the spacer material must be in the range $1\mu m$ to $3\mu m$. Two types of spacer material having this characteristic were investigated. These were SiO_x spacer layers and polymer micro balls or rods. SiO_x was evaporated onto the substrate to form spacing structures. An aluminium mask or some lithographic techniques were employed for the formation of pillars on the substrate. The depth of the pillars was controlled by the crystal monitor in the evaporator. These structures were investigated by Scanning Electron Microscope (SEM) (J.Findlay, Dept. of Botany) and by Tally-step measurement (A.O'Hara). Figure 3.3 shows an SEM picture of a $2\mu m$
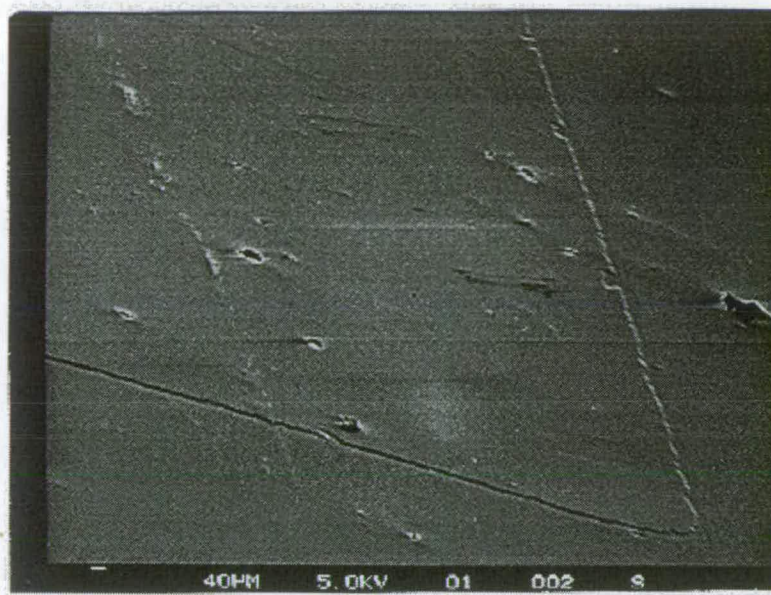
Figure 3.3: Typical SEM of early SiO_x pillars

oxide pillar. As the pillars do not have to be very accurately sized or positioned, the aluminium mask fabrication technique is by far the simplest and any photolithographic steps can be avoided. The crystal monitor in the evaporator is not very accurately calibrated, but tally-step measurements have been used for calibration as only certain pillar heights are required. The alternate technique used in the fabrication of FLC cells is the use of polymer spacer balls or rods. The main disadvantage of this techniques is the limited availability of suitable sizes for required cell thickness. After considerable effort, $1.7\mu m$ spacer rods and $3\mu m$ spacer balls [109] were acquired for investigation. As these particles constitute a health risk and possible contamination of the clean room, extreme care was required in their use. Two possible methods of deposition onto the substrate were considered. The first was spinning the spacers onto the substrate, but this led to possibility of spacers remaining in the active area of the cell and so causing defects. The second and much more appropriate was the mixing of the spacers into the glue used for sealing the cell. This has the requirement that the glue must go between the two cell substrates reasonably uniformly and not merely around the outside.
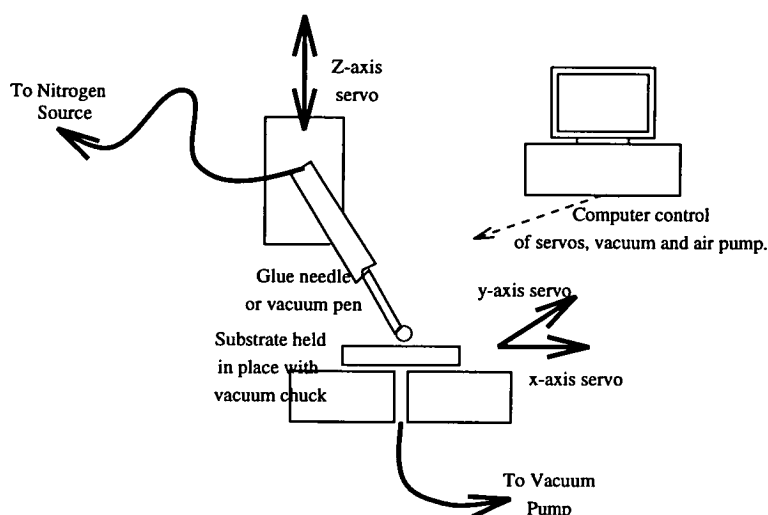
Figure 3.4: The glue writing and cell construction system

3.1.5 Photolithography

Various photolithographic techniques were investigated in initial fabrication studies. In eventual cell construction, they were deemed unnecessary. Both the ITO layer and spacer layers can be patterned if required. Etching techniques must be employed for the patterning of external ITO films, but lift-off techniques have successfully been used with in-house ITO fabrication of patterned electrodes [110].

3.1.6 Mechanical Construction

A glue writing and substrate positioning station was designed by M.W.G. Snook to facilitate this proceedure (figure 3.4). Initial studies were performed using a hand-held glue dispenser and a simple air evacuated bag to allow a vacuum packing technique to give uniform pressure across the substrates as the glue dried. This was found to be inadequate for the production of uniform cells. The two main reasons were that too much glue was deposited and that the vacuum bag did not give a uniform pressure. It was discovered that the application of a simple point of pressure on the top substrate was sufficient to produce good cell uniformity. A more accurate means of glue deposition was required. The glue writing station allows the accurate computer-controlled x-y-z positioning of the

($100\mu m$) dispensing needle and controlled deposition using a computer-controlled pump. Within a $1\mu m$ cell, $0.5mm^2$ dots of glue are possible and the accurate writing of lines of glue attainable. The top substrate can be accurately positioned by a vacuum pen on the x-y-z stage while under observation through the microscope. Alternatively, substrate holding jigs have been constructed is the Physics department workshop, which accurately position one substrate over another. The glue can then be cured while the cell thickness is being held uniform under a vacuum bag or with a point pressure probe. UV curing glue has been found to be the most useful type of glue as it can be cured in seconds and selectively with a UV source. Norland 68 UV cure glue has a high viscocity and has been used successfully in this procedure.

3.1.7 Vacuum Filling

Nematic LCs have a low viscocity at room temperature, so they flow easily into test cells by capillary action. FLCs are very viscous in the smectic phases and must be heated up to the isotropic phase to allow them to fill the cell. It is also advantageous to fill cells under vacuum conditions to out-gas the LC material and prevent the formation of air bubbles in the cell. Therefore, a hot plate with a temperature sensor was used in a vacuum chamber to fill FLC test cells. Figure 3.5 shows the apparatus for filling the FLC test cells. A small amount of FLC material is placed at an open edge of the test cell. This cell is placed on the hot plate in the vacuum chamber. The pressure in the vacuum chamber is reduced and the temperature of the hot plate raised to just beyond the materials particular isotropic phase transition temperature of the material for an initial out-gassing. This temperature is usually higher than $110^{\circ}C$ so aiding the removal of any moisture. The FLC material will 'froth-up' during this procedure and eventually fill the cell by capillary action in the isotropic phase. When the material has been left for a sufficiently long time, as a final aid to filling, the pressure is rapidly brought up to atmospheric pressure from 10^{-6} Torr. The cell is then left to slowly cool to room temperature (≈ 1 hour) to allow the formation of good structures at the various phase transitions. This technique has resulted in successful filling of cells. It is usually prudent **carefully** to remove the excess LC material from the outside of the cell with acetone (try to avoid acetone entering the cell and contaminating the FLC).

$($
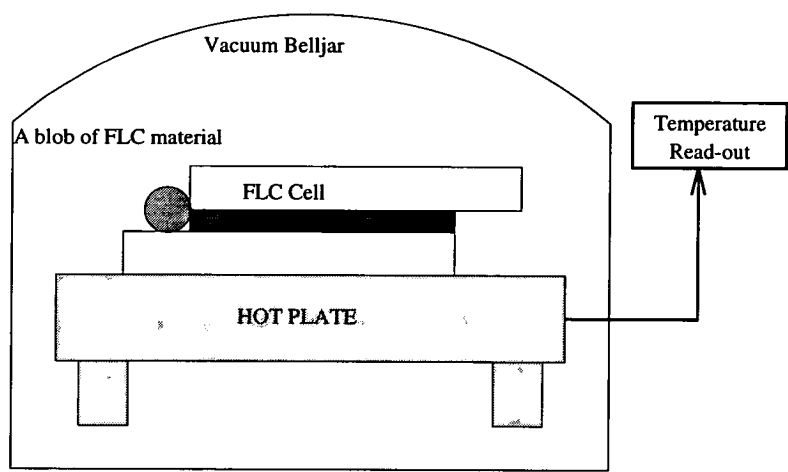
Figure 3.5: The apparatus for filling the FLC cells

3.1.8 FLC Mixtures

A number of different FLC mixtures have been used in the study. The majority were supplied by Merck-BDH [111], but also some from F.Hoffmann-La Roche [112] and Co. Ltd and Chisso [109]. The reasons for the use of each particular FLC mixture will be discussed in the relevant sections.

3.2 Cell Construction

Using the techniques discussed in section 3.1, FLC test cells can be constructed. The cells should be of a uniform thickness to avoid splay distortions and allow good alignment. The thickness of the cell should be such as to allow optimum optical modulation. The cells should readily allow optical access and electrical contact to the electrodes. Most importantly, they should reflect the constraints imposed upon construction of devices of VLSI backplane SLMs.

The techniques for the construction of two types of test cell were developed in detail. The simplest and most useful for preliminary study was the transmissive cell. A slightly more complicated cell is the reflective variety, but this does allow a more realistic appraisal of what is achievable in a VLSI based SLM.
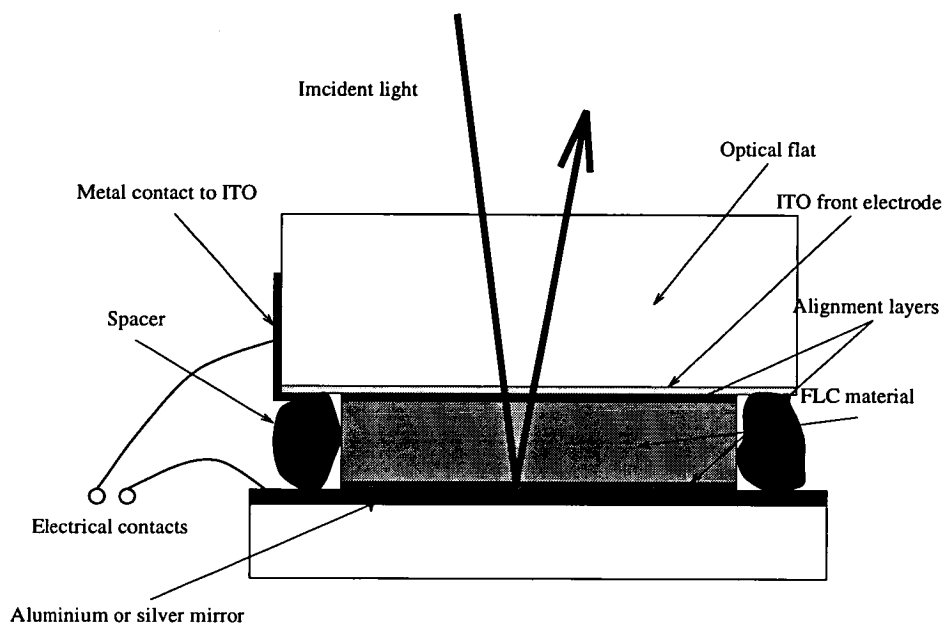
Figure 3.6: The structure of a reflective test cell

3.2.1 Transmissive Cells

The structure of the transmissive cell is shown in figure 3.1. It consists of two identical glass substrates separated by a spacer material. Identical alignment treatment can be expected on both of the transparent conducting electrodes. Electrical contact is achieved by a slight displacement of the two substrates. The majority of FLC investigation was performed with this test cell structure. The main advantage is that the substrates are identical, avoiding any extra processing step, so symmetric boundary conditions apply before any alignment treatments are applied. The optical system for investigation of this cell structure is much simpler. The only drawback of this structure is that cells thinner than $1.5\mu m$ will not optically modulate light in a satisfactory manner due to the wavelength/depth dependence (equation 2.1). For preliminary FLC investigation it was decided that the transmissive device would allow a potentially more useful means of cell development.

3.2.2 Reflective Cells

By depositing a reflective metal coating (aluminium or gold) onto one of the substrates, a reflective device structure can be fabricated. This more closely mimics the reflective nature of VLSI backplane SLMs, but adds an extra variable into the process (figure 3.6). A reflective cell further complicates cell investigation due to the double pass of incident light in and out of the cell which would perhaps cause complicating effects due to poor optical alignment. Nevertheless, the reflective cell proved a useful tool in assessing SLM performance during the transition from test cell to SLM device.

3.3 Alignment Layers

This is arguably the most sensitive portion of the FLC cell fabrication. Chapter 2 described how important the alignment layers are in the generation of high quality FLC device structures. Section 2.5 gave a summary of the different types of alignment layers possible in FLC cells. Rubbed polymer techniques are very popular, but would seem to be not very controllable and possibly detrimental to VLSI silicon backplane circuitry. Ideally any alignment layer technique would be part of a post-process in the wafer fabrication, and be repeatable on the top cover glass. Obliquely evaporated dielectrics are the most accessible techniques, as only one processing step is required; a single evaporation. Photolithographic etched structure would seem to be the most controllable alignment techniques, although somewhat more involved. Obliquely evaporated films were investigated in more detail.

Surface alignment layers cause the LC molecules to orientate their molecular axis to minimise the free energy near the bounding plane. In general, the elastic strain energy is the most important interaction affecting the molecular alignment of LC molecules. The dimensions and topography of the microstructures allow an estimation of the elastic strain energy. In general, it is usual to apply the same alignment treatment to both bounding plates, resulting in symmetric boundary conditions. In section 2.6, we suggested that much more complicated structures may result if asymmetric boundary conditions are employed, perhaps when alignment treatments are applied to only one of the boundary

plates. This is usually carried out due to necessity and not design. For example, rubbed polymer techniques have been applied to SLM backplane devices, but only on the cover glass electrode [45]. This was to avoid damage to the circuitry on the SLM backplane during any rubbing proceedure. As the consequences of asymmetric boundary conditions are potentially complicating, they will only be briefly discussed in chapter 4.

3.3.1   Rubbed Polymer Films

To achieve rubbed polymer alignment layers on a substrate two tasks must be addressed. Firstly, the deposition of the polymer layer and secondly, a reproducible rubbing technique must be applied. Reproducibility of both of these tasks was found to be problematic. To deposit a polymer, experimentation was performed using Poly-Vinyl-Alcohol (PVA). The PVA was suspended in distilled water ($2.5gl^{-1}$) to allow a thin layer to be deposited on evaporation. Two techniques were tried to distribute uniformly a thin layer of PVA on the substrate, spinning and blowing. In the spinning technique a small drop of the PVA/water suspension was dropped onto the substrate while the substrate was spinning at high speed on the spinner. In the blowing technique, the substrate was dipped into the PVA/water suspension and then unidirectionally blow-off with the ionising nitrogen gun. As the water blew off, a small deposit of PVA was left due to some evaporation. Both of these techniques results in PVA with varying thickness.

To achieve the rubbing, lens or cleanroom tissue, was manually rubbed across the substrate with 'light' pressure and at approximately $2cms^{-1}$. Rubbing procedures could have a detrimental effect on VLSI backplanes, perhaps causing damage. On inspection of the substrate, various structures and slightly different coloured regions could be observed. This suggests that the techniques described above were less than satisfactory in achieving a uniform alignment layer. The layers were coated in gold and observed by SEM. Unfortunately, no groove structure was evident from this study and little structure could be seen. Therefore, although this technique is used for mass production of LC displays, the preliminary investigation described above casts doubt on the reproducibility and suitability for SLM devices.

Medium Angle Deposition: LC molecules perpendicular to evaporation direction

(a)

Small Angle Deposition: LC molecules orthogonal to MAD alignment

(b)
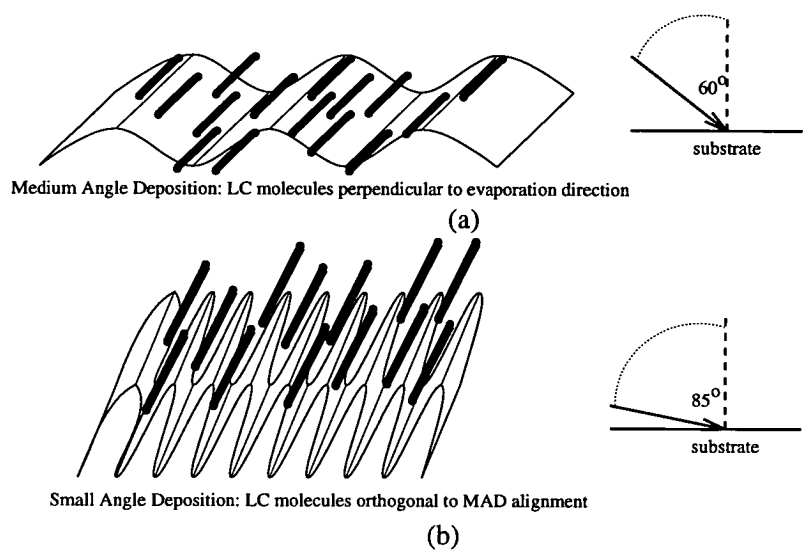
Figure 3.7: Schematics of MAD and SAD alignment layer structures

3.3.2 SiOx Films

This investigation was carried out in conjunction with Y. Rouxel. Two main types of obliquely evaporated SiO_x films were investigated. These are known as Small Angle Deposition (SAD) (deposition direction-to-substrate angle $\approx 85°$) and Medium Angle Deposition (MAD) (deposition direction-to-substrate angle $\approx 60°$). Figures 3.7 (a) and (b) ideally describe these two regimes of oblique evaporation. Samples with various thicknesses and evaporation angles were investigated. Figure 3.8 shows the apparatus in the evaporator used to deposit the films. The substrates were held above the SiO_x 'boat' at the required angle. The pressure in the chamber was reduced to at least 10^{-5} Torr before evaporation commenced. The molybdenum alloy boat, containing the oxide, was heated to achieve an evaporation rate of 0.1nm/sec. In practice, it was found to be very difficult to remain within a 50% of this value. Fine adjustment of the current supply was needed to retain this rate. The evaporation depth was measured on the quartz crystal monitor. The thickness is measured in the direction of the evaporation i.e. the vertical direction. Since the deposition is onto an oblique substrate, the actual material thickness is approximately $\cos \Phi \times$ **measured thickness** where Φ is the angle between the substrate normal and the evaporation direction. All thickness quoted for the alignment layers are those directly measured by the crystal monitor. The deposition of material is assumed to be uniform, although this is not strictly true. In reality, this
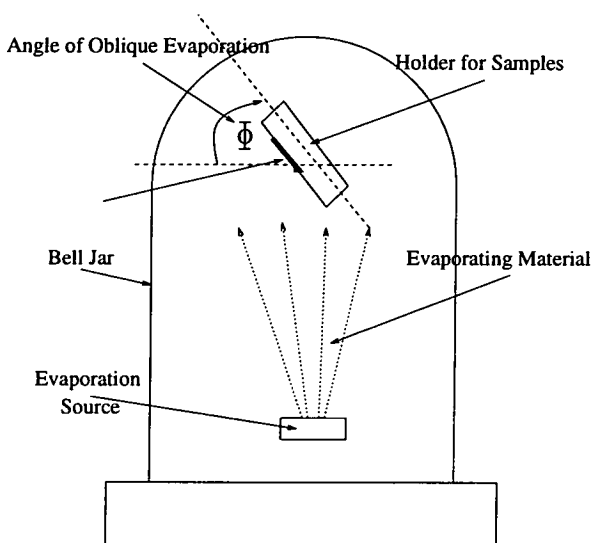
Figure 3.8: The apparatus for producing obliquely evaporated alignment layers

will depend on the distance the substrate is from the source and the dimensions of the oxide boat. If the source was assumed to be a point source then the evaporation would be produced in a conical direction, so depending on the distance the substate is from the source normal, the different the angle of incidence of the material would be arriving at the substrate. This variation is manifest as slightly varying colours in SiO_x films produced on reasonably large substrates ($> 60mm$). It is estimated for sufficiently small substrates and for close to the normal, that the effects of these variations will be negligible. The main concern for the evaporation proceedure is probably the difficulties in maintaining a uniform deposition rate. A Scanning Electron Microscope (SEM), operated by J.Findlay in the Department of Botany, was used to assess these alignment layers. Small alignment layer samples on pieces of glass slide were coated with a thin layer ($1nm$) of gold to allow electrical contact in the SEM, as the SiO_x films have high resistance. It was hoped that the thin layer of gold would not be detrimental to the investigation. MAD alignment layers resulted in a 'corrugated iron' like morphology and the SAD alignment layer were expected to result in tilted pillar like structures [70]. A typical SEM of a MAD structure is shown in figure 3.9. The deposition angle was 60° and the thickness measured as 100nm. The ridge pitch averages at about 0.4μm. and evaporation direction is 1 **top to bottom** Note the large particulates of SiO_x as large as 0.5μm. These are undesirable, but can be reduced by 'baffling' the SiO_x boat. The ridge structure is very randomly distributed, but this may be desirable in allowing the FLC alignment a greater degree
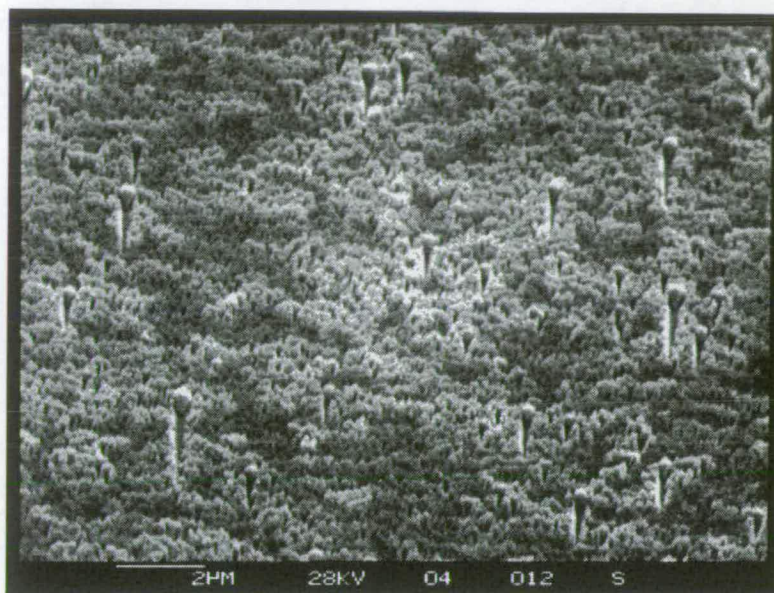
Figure 3.9: An SEM of MAD alignment layers (evaporation direction is top-to-bottom

of freedom, and perhaps to settle into a lower (and possibly more desirable) energy configuration. Figure 3.10 shows another MAD evaporation (the evaporation thickness $60nm$). The evaporation direction is top right to bottom left. This shows more clearly a ridge structure with a ridge pitch of approximately $0.2\mu m^{+}_{-}0.5$. A typical SEM of a SAD structure is shown in figure 3.11. The deposition angle was $85°$ and the thickness measured at $60nm$. The small bumps are much finer than the MAD ridge structures $< 100nm$ and more randomly distributed in the plane, tending to form short micro 'pillars'.

3.3.3 SAD and MAD alignment layer discussion

MAD alignment results in an undulating 'corrugated iron' topography of the alignment layers. This alignment structure will certainly line up the smectic layers parallel with the direction of evaporation and due to a small amount of asymmetry, akin to the asymmetry in ripples on sand, may cause a reduction in the molecular direction degeneracy to achieve a uniform director orientation. The SAD alignment structure of tilted columns will
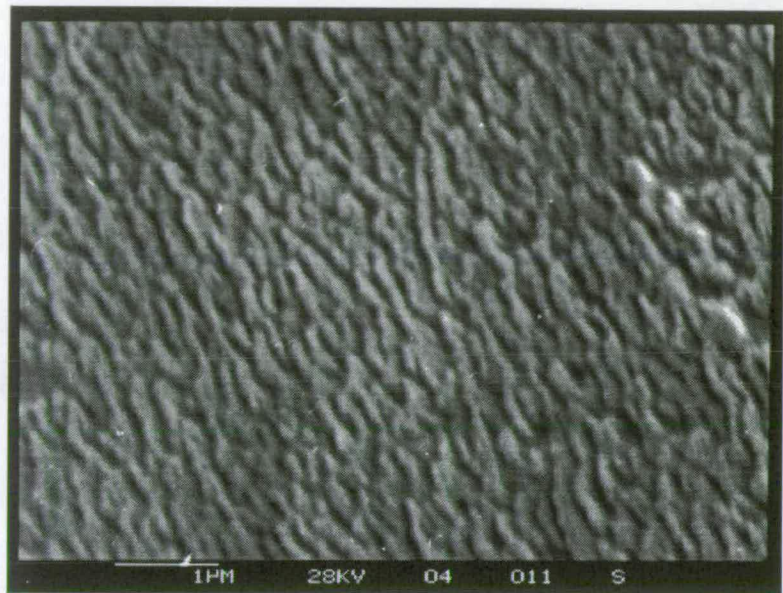
Figure 3.10: Another SEM of MAD alignment layers (evaporation is left-to-right)
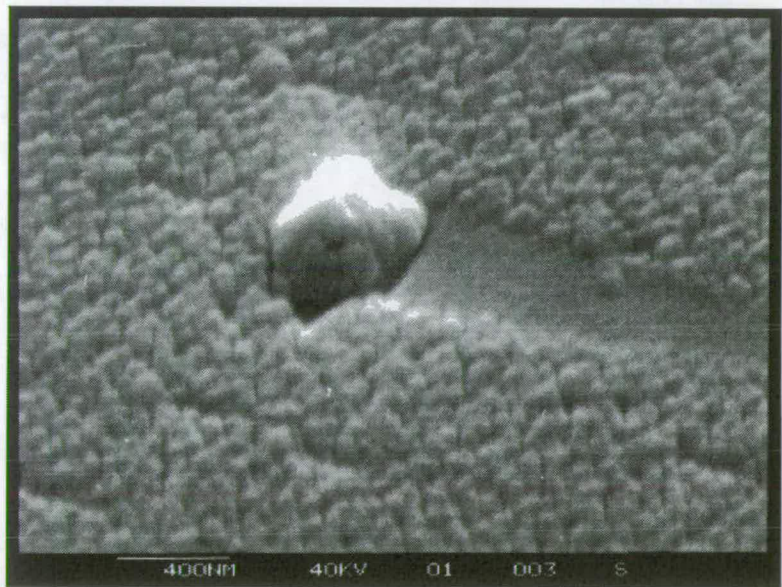
Figure 3.11: An SEM of SAD alignment layers (evaporation direction is left-to-right)

probably cause a pretilt of the molecules at the surface depending on the tilting of the columns. This should induce a uniform orientation of the molecules within the smectic layer in the direction of the column tilt, and only weakly affect the smectic layers. In the SAD alignment structure, parallel or antiparallel orientation of the bounding plates should cause different effects as the tilt angles of the FLC molecules would be 180° different near each surface. Therefore, it would seem that to achieve highly aligned and uniform FLC molecular structures a combination of both the SAD and MAD structures should be applied [89]. The directions of evaporation of the two structures should be orthogonal. It is desirable that the MAD structure should be applied first, as the SAD structure will have little opportunity to mask the topology of the MAD structure.

3.3.4   Etched Substrates

Work on etched substrates was carried out in conjunction with B.MacDonald and A.S. Stevens. The work was performed with a view to aligning nematic LCs, although the same principles can be applied to FLCs: the alignment requirements are different and the energy supplied to the bulk material is required to be larger in the FLC case. Gratings were fabricated using two techniques: photoresist gratings on silicon substrates and etching gratings on glass substrates using a dry plasma etch. As with the evaporated SiO_x alignment layers, the ability to physically align LCs was predicted using SEM measurements to calculate the estimated elastic strain energy for LC molecules near the gratings. Due to limitation in the photolithographic processes, relatively large grating pitches were fabricated (pitch $\approx 2 - 4\mu m$, depth $< 0.5.\mu m$). Although section 3.3.3 suggests that a simple periodic grating structure may not be all that is required for FLC alignment, this preliminary investigation allows the principles behind etched alignment layers to be investigated. With the photolithographic equipment available, only large grating structures could be fabricated. This means that the techniques may not really be applicable to thin cell FLC devices. The induced energies may be suitable for nematic LC but are perhaps too low for FLC materials. Access to sub-optical wavelength photolithographic techniques would allow much more suitable structures.

3.3.5 Alignment Layer Discussion

Three types of alignment layer techniques have been considered. Of the three, obliquely evaporated SiO_x films would seem to be the most suitable for further FLC development. The rubbed polymer technique, although suitable for large volume nematic LC displays, does not seem to be easily reproducible for the more sensitive alignment requirements of the FLC device. Etched alignment layers offer a great potential for fabrication as part of standard microelectronic proceedures. The etched alignment technique requires a much more thorough investigation, which is outwith the scope of this study. For the following FLC studies, obliquely evaporated SiO_x films will be the predominant technique applied.

3.4 Post-Filling Treatment of FLC Cells

Section 2.8 described FLC defects, particularly the chevron defect. On cooling into the liquid crystal phases, it is hoped that a uniform monocrystal structure grows, without any defects. This is a rather optimistic hope due to poor alignment layer quality or nonuniform thermal cooling of the cell. To assist the uniform alignment of the cell it is possible to aid the growth of monocrystal cells by the application of electrical or magnetic fields which induce preferential alignment of molecules in the bulk materials. To avoid ionic drift and the build-up of surface charges the fields should be a.c. . Alternatively, after the sample has cooled, it is still possible to reorientate the molecules with post-filling electrical treatment. A high voltage, low frequency, a.c. waveform is usually applied to a disfunctional cell, which can remove the chevron defect, reduce the striped texture defect and induce fully bistable operation. Voltage treatment techniques are discussed by Patel et al [89, 105, 86, 92, 91].

3.5 Cell Appraisal Techniques

There are a variety of techniques for analysis of various FLC device parameters. The ones of most concern in this study will be those which determine the optical modulation

characteristics. FLC material parameters such as the spontaneous polarisation and re-fractive indices, given in the manufacturers data sheets, will be assumed to be accurate. The principle area of investigation is when the material is constructed into a useful device structure, although the parameters will play an important role. The techniques apply to all types of FLC device structure, but this preliminary study has been limited to the SSFLC structure.

3.5.1 Electrical characteristics

In appendix A, some of the theoretical models of FLCs are introduced. The ferroelec-tric capacitor model can allow useful measurements into static and dynamic switching electrical characteristics of FLC devices. The techniques are particularly useful in the modeling of FLCs in circuit simulation for silicon backplane design. Two of the most interesting methods of electrical measurement on FLC devices are examining the $E - P$ (electric field-polarisation) ferroelectric hysteresis curves and measurement of the po-larisation reversal currents. Both of the techniques give an insight into the dynamical switching with regard to the polarisation. Equation A.7 shows that P is proportional to the integration of the current. The circuit used to examine this was developed by Sawyer and Tower [54] and is shown in figure 3.12.

The capacitor at the top is the ferroelectric capacitor (FLC cell), while at the bottom a linear capacitor is used to integrate the charge flowing through the circuit proportional to v_y.

$$v_y = \frac{1}{C} \int i \, dt \qquad (3.5)$$

Typically the linear capacitor has a capacitance much larger than the ferroelectric ca-pacitor, so that v_x fairly accurately represents the voltage applied to the ferroelectric material. From equation 3.5, the voltage v_y is proportional to the polarisation state of the ferroelectric material. When a sine wave is applied to the circuit and v_x and v_y are measured on the x-y inputs of an oscilloscope, the ferroelectric hysteresis curve can be measured. As an example, a $3\mu m$ thick FLC cell was filled with SCE13 (Merck-BDH). The active area of the cell was $7.8^{+}_{-}0.1 \times 5.6^{+}_{-}0.1 mm^2$. The capacitance of the linear ca-pacitor was $1\mu F(^{+}_{-}10\%)$ and the v_x, v_y voltages were measured on a storage oscilloscope. A $10Hz$ sine wave was applied to the circuit and the resulting   trace was obtained
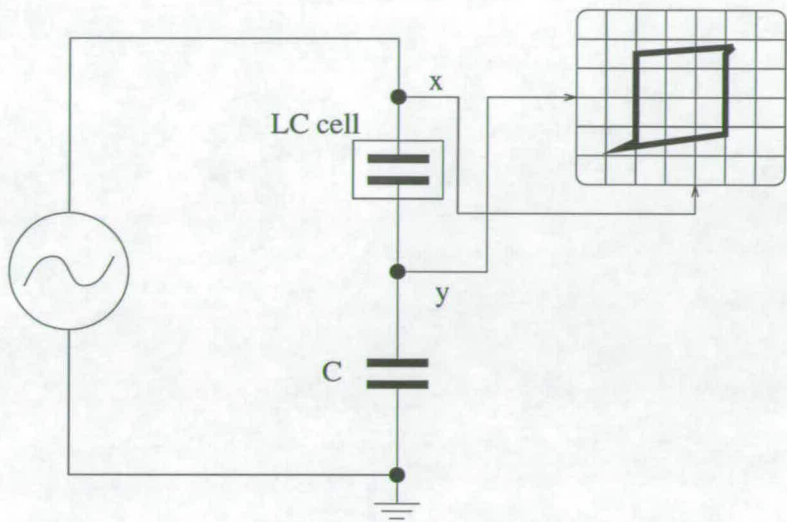
Figure 3.12: Sawyer-Tower circuit for the measurement of ferroelectric hysteresis curve.
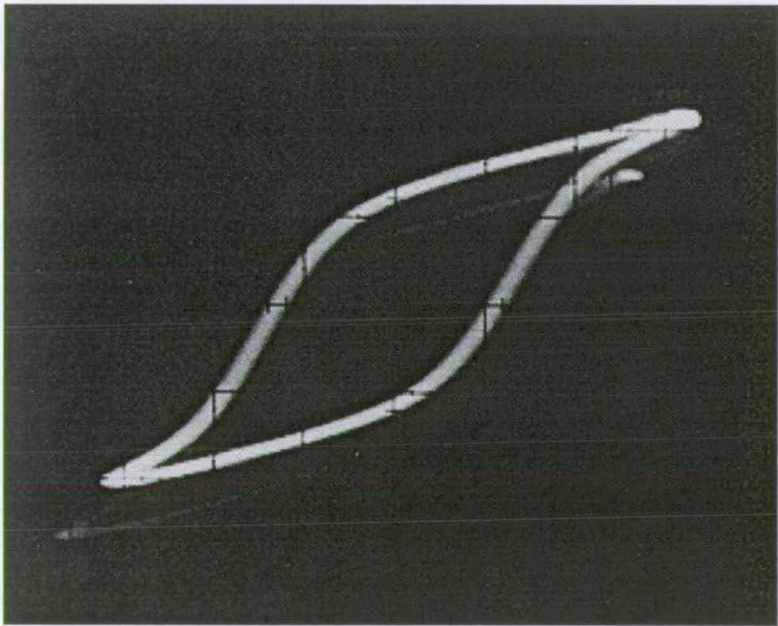
Figure 3.13: An example of a hysteresis curve
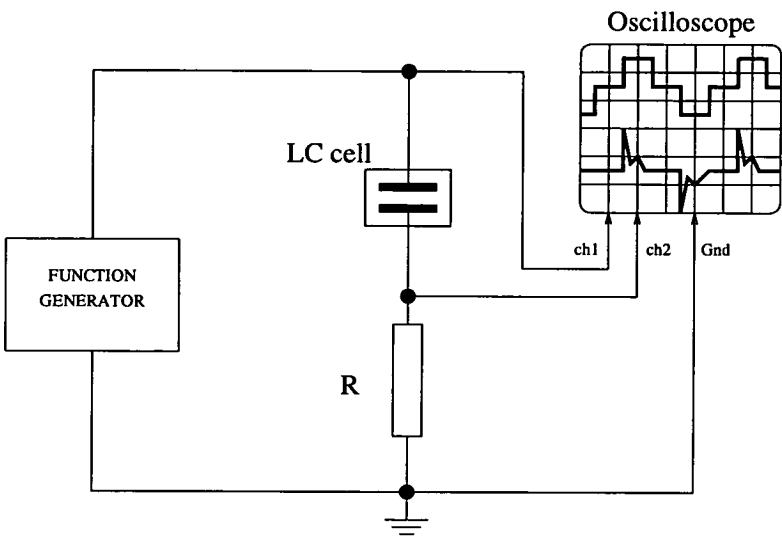
Figure 3.14: The circuit for measuring polarisation reversal currents

on the oscilloscope.The scale on the x-axis is $2V/div$ and on the y-axis $10mV/div$. Figure 3.13 shows the resulting trace. The polarisation can be measured directly on the y-axis. The spontaneous polarisation is obtained from the crossover point on the y-axis. The voltage at this point is 10^+_-2mV. Substituting these values into equations A.7 and 3.5, the value of $23^+_-5nCcm^{-2}$, is obtained for the spontaneous polarisation. A value of $27.8nCcm^{-2}$ is quoted in the data sheet for SCE13 at room temperature. More accurate measurements can be obtained by the addition of a compensating circuit to allow for the phase shift in the current response and a high impedance current amplifier to reduce the effects of the measurement apparatus. This high value of P_s is the main reason for the selection of SCE13 in following experiments.

The polarisation reversal current can also be measured. Instead of examining the polarisation current as a function of applied field, the transient current due to the reversal of the applied field can be measured. Figure 3.14 shows the simple circuit used to measure this current. A voltage step is applied to the series resistor and the FLC cell. The current through the circuit can be obtained by measuring the voltage across the series resistor. The area under the current peak gives the charge supplied to the cell to reverse the polarisation i.e. twice the P_s.

$$2P_s = \frac{1}{A} \int i \, dt \tag{3.6}$$

where i is the current and A is the cell area. The current curve has three components, the
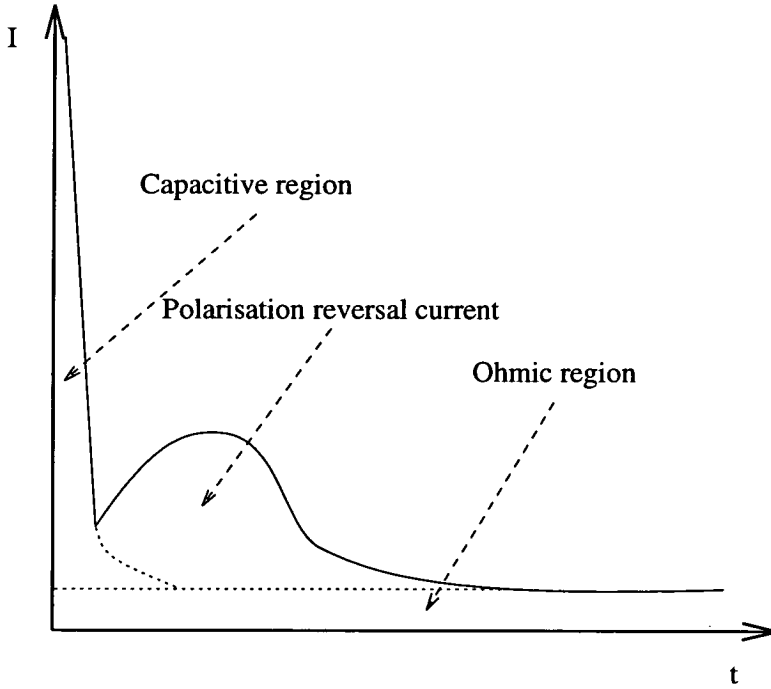
Figure 3.15: The polarisation reversal current schematic

capacitive current, the polarisation reversal current and ohmic and ionic current (figure 3.15). The capacitive current is the very high initial peak with with a rapid exponential decay. The second, broad peak is the current from the polarisation reversal. Any ohmic or ionic current contributions result in the current curve to being shifted up the y-axis [54].

The cell used in the hysteresis experiment was connected in series with a 2.2 KΩ resistor to obtain the current response to a voltage step of $10V$. The area under the current curve is obtained from the oscilliscope trace shown in figure 3.16. The area under the second peak was measured as $6^{+}_{-}1 \times 10^{-9}C$. When substituted into equation 3.13, this gives a value for the P_s as $30^{+}_{-}5nCcm^{-2}$ (cell area is $\approx \frac{1}{2}cm^2$). This current peak is well separated from any capacitive current and the conductive current can be subtracted. The driving circuit will contribute some effect but the polarisation is large in comparison to the effects of internal impedences. This is a useful empirical model to employ in the circuit simulation of SLM pixels. The average value of P_s obtained by these methods is $27^{+}_{-}4nCcm^{-2}$ in good agreement with the published value of $27.8nCcm^{-2}$.
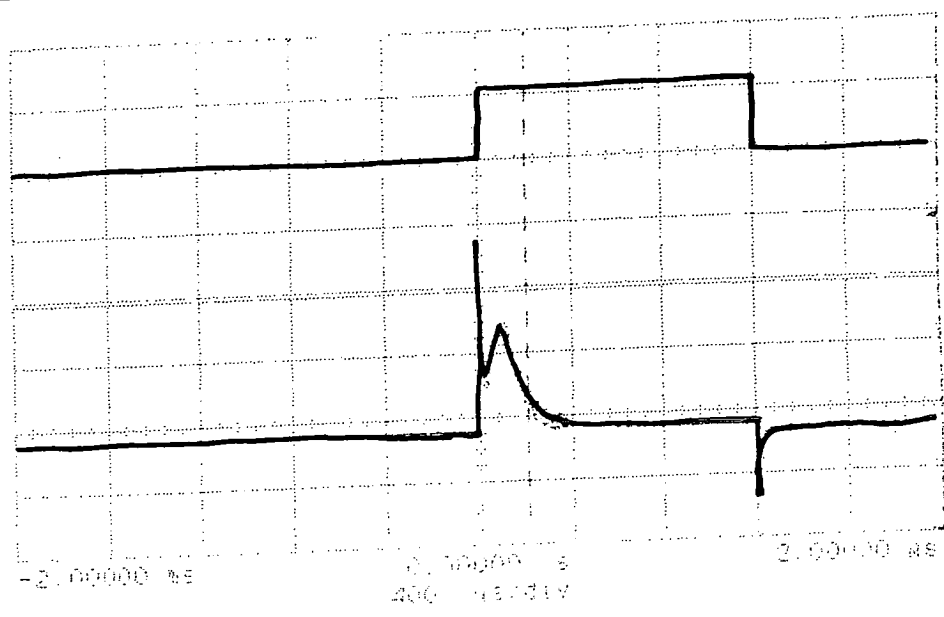
Figure 3.16: Measurement of polarisation reversal current

3.5.2 Polarisation Colours

As FLC material is birefringent, this can be observed as one would investigate uniaxial crystals through polarising microscopy. When viewed in white light between crossed polarisers, a colour change is observed due to the wavelength, depth and angle dependence on the birefringence which rotates the polarisation. Therefore, different wavelengths of light are attenuated by differing amounts causing a colour change from white. By holding two of these three variables constant, analysis of the colour can give an indication of the third variable. In crystallography, it is usual to measure the birefringence of a crystal by reference to a polarisation chart which plots the birefringence on a chart showing polarisation colour and material depth. As the birefringence is quoted in the FLC data sheets, this is a useful technique for analysing cell depth and director orientation. In an FLC device with a uniform director orientation, such as the ideal SSFLC, any wedge in the cell will be observable through a variation in colour.

In the polarisation chart, the regime of interest for thin cell FLC devices does not really give an accurate measure of cell depth, but will allow depth variations down to 50% accuracies, i.e. depth variations rather than particular depths can be more easily analysed. Any depth variation will affect unduly the device contrast uniformity (and probably the switching time and voltage across the cell). Different director directions
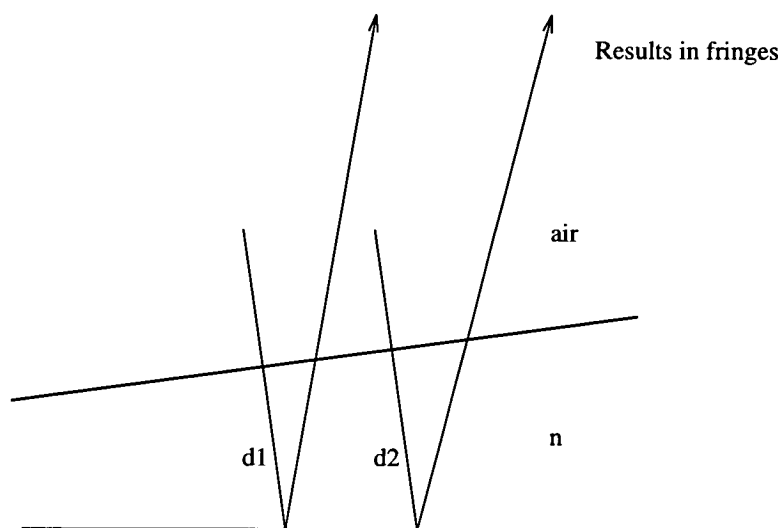
Figure 3.17: The origin of interference fringes in a wedged material

show up as different colours due to the differing angle to the polarisation direction. This is exemplified dramatically on observation of a non-surface-stabilised FLC device where the helical structure causes colour variation across the cell. The helical pitch can be measured from the colour repetition.

3.5.3 Interferometry

Interferometric techniques can be useful for investigating variations of depth in cells, filled or otherwise. Such techniques rely on low efficiencies of transmission or reflection in the cells for observable contrast in the interference fringes. If one places two glass plates together and observes them at a near incident angle under a light source, interference fringes are visible. These fringes show the variation in the air gap between the two plates. This allows a potentially useful technique for the appraisal of the flatness and uniformity of the test cells, before filling with LC. This technique is only application to variations in the air gap and does not give some absolute value of separation. To avoid splay distortions in the LC it is arguably more useful to know the level of cell gap variation than the actual cell gap depth. This will become more apparent when packaging of the silicon chip in SLM device fabrication must be contended with. Consider a wedge of material with refractive index n shown in figure 3.17. Two paths through the material

for parallel light are shown (d_1 and d_2). For constructive interference the path difference must be a multiple of λ the wavelength of light. As the light passes through the material twice, the optical path length is $2nd$ i.e.

$$2nd_1 = m\lambda \tag{3.7}$$

$$2nd_2 = (m+1)\lambda \tag{3.8}$$

where m is an integer. Therefore, between two fringes of equal wavelength, the difference in depth in the material is equation 3.7 subtracted from equation 3.8:

$$\Delta d = \frac{\lambda}{2n} \tag{3.9}$$

As an example, if two red ($\lambda \simeq 600nm$) fringes are observable across a test cell with an air gap ($n \simeq 1$), the variation of cell depth between them is therefore $\sim 300nm$.

D.J.Potter constructed an interferometer for observing the phase flatness of nematic SLMs [40]. An early 176^2 backplane SLM was placed in this system to examine the interference fringes obtained. Figure 3.18 shows the result of illumination under HeNe $\lambda = 633nm$. The cell was filled with LC, so the refractive index was averaged as 1.6. Due to the birefringence of the LC a more accurate measurement could be made if the polarisation direction of the incident light was specified. The circular fringes show a variation of $\sim 1.5\mu m$ on the cell depth of $3\mu m$, a very large variation.

A   simpler technique for observing the fringes is under white light. As the light is polychromatic, different colours of fringes, from blue to red can be observed. This allows the identification of which direction the variation is progressing due to the colour variation (blue shows thinner than red). A glass cell or SLM can simply be held nearly obliquely under white light and the fringes can be observed. This simple technique will be applied to the test cell and SLM developments in the following chapters. Cell depth variations will be identified through this method. This is a very practical method for simple application during cell and SLM fabrication.

3.5.4   Domains and Defects in SSFLC

Section 2.8 described some of the defects structures which could be observed in the thin SSFLC cells. In this section some examples of the expected defects will be presented.
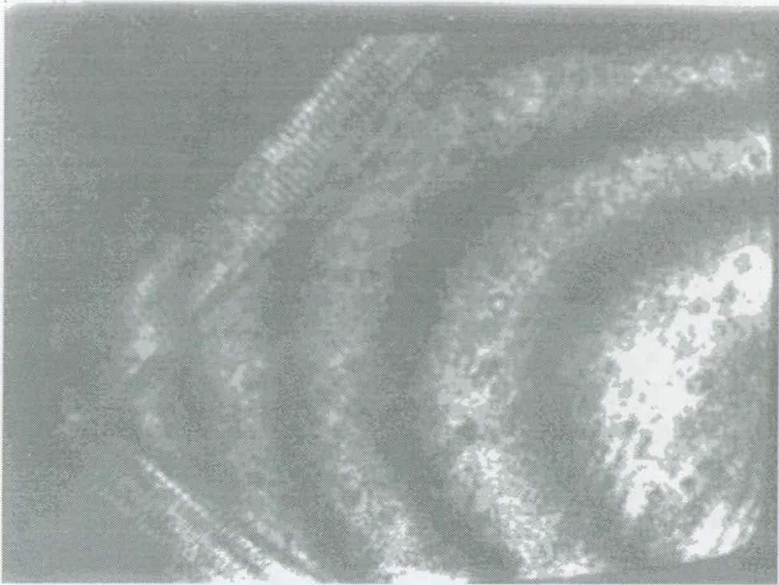
Figure 3.18: Monochromatic interference fringes in an SLM device
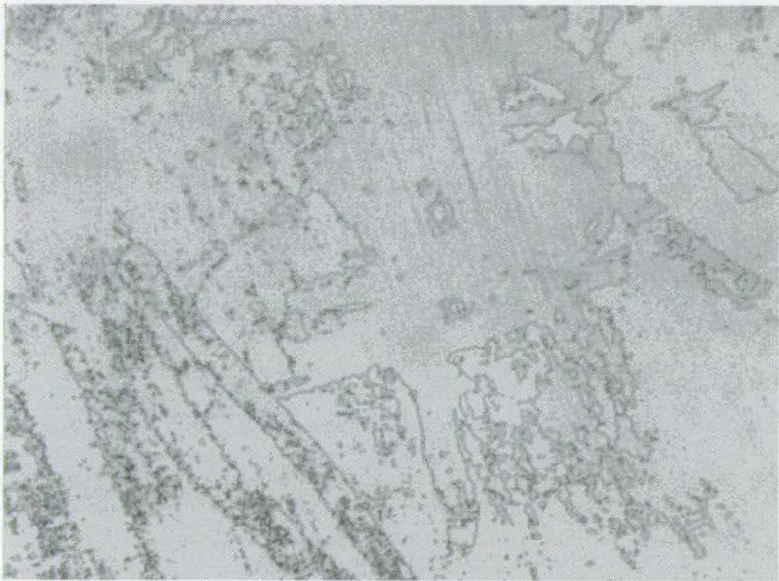
Figure 3.19: Observation of domain walls between different FLC orientations

The defects were examined under polarising microscope, with white light illumination. A comparison should be made between figures 3.19 to 3.25, showing examples of defect structures observable on SSFLC test cells, and figure 2.8, schematically identifying the generic types.
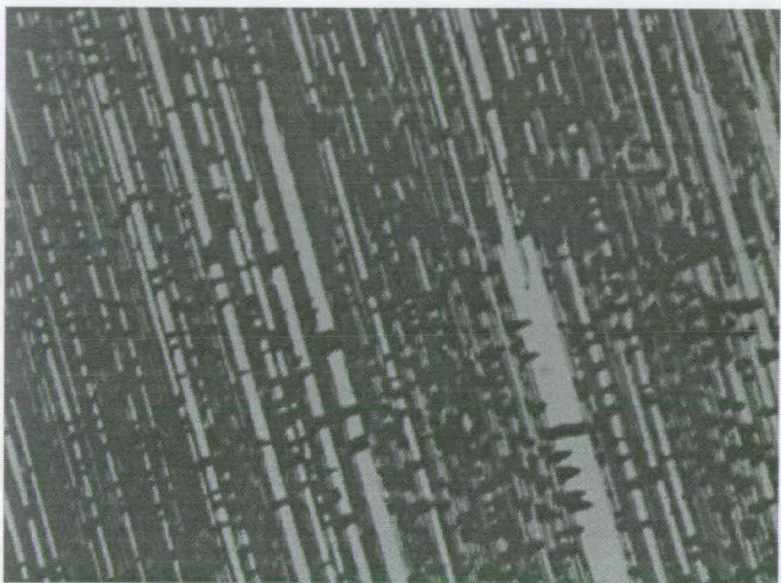
Figure 3.20: Stripe and Bear Paw defects
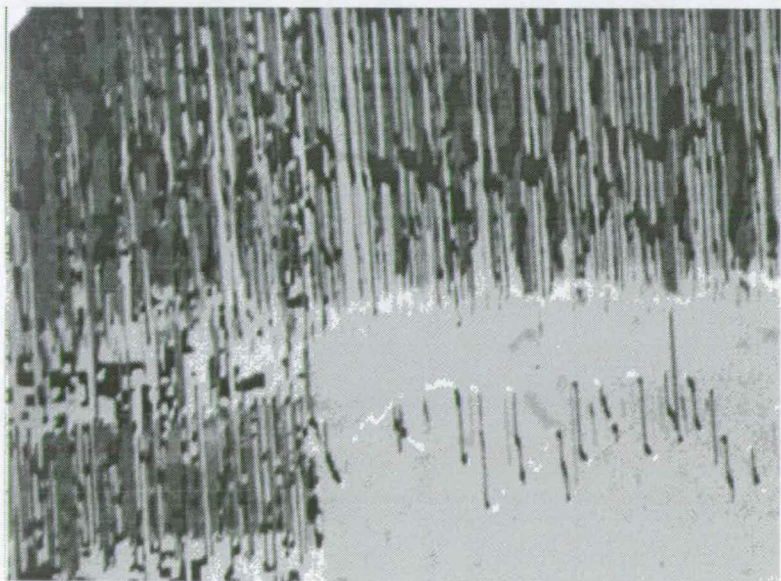
Figure 3.21: Stripes and zig-zags
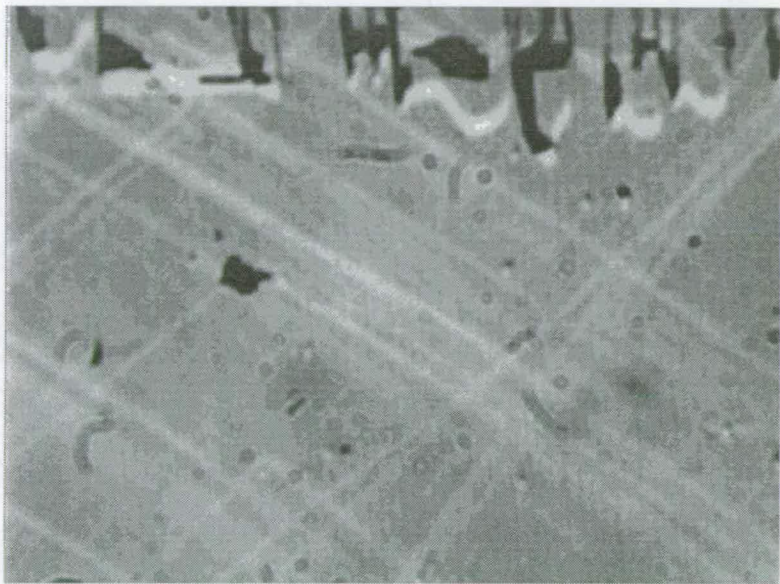
Figure 3.22: Close-up of zig-zag defects
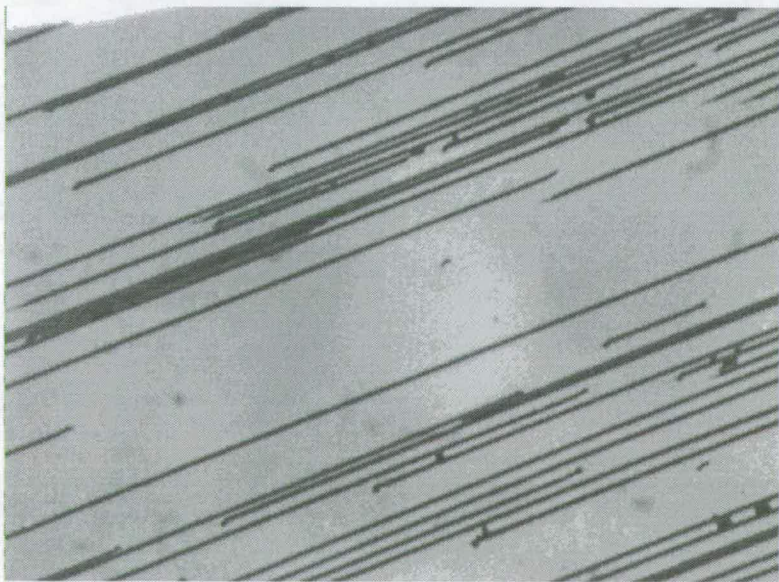
Figure 3.23: Isolated needle defects
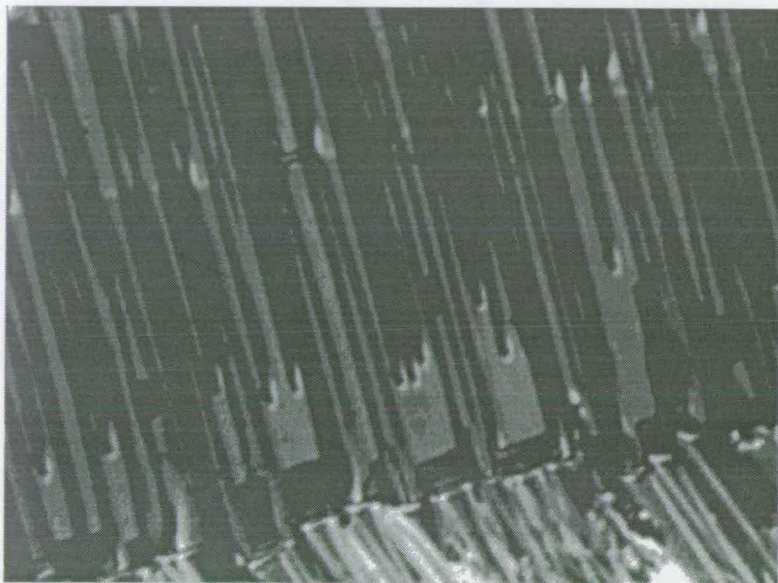
Figure 3.24: Close up of needle defects
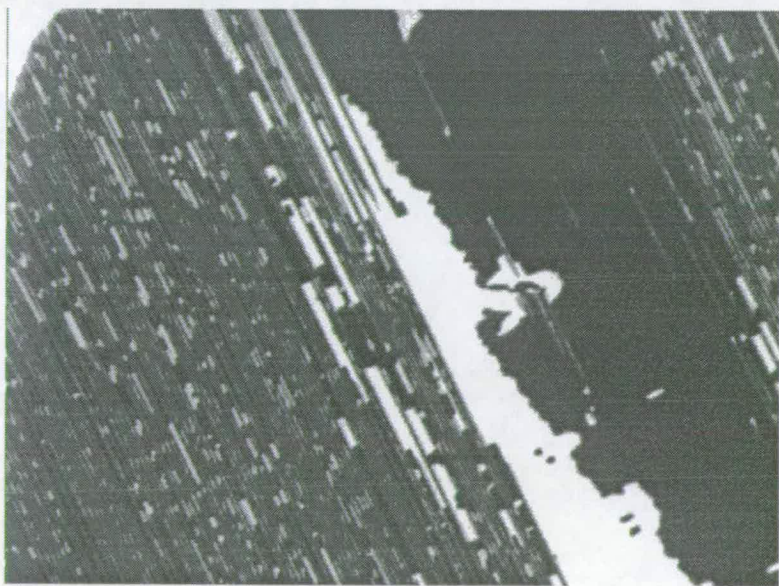
Figure 3.25: A mixture of non-chevron and chevron regions

Figure 3.19 shows two domain regions orientated to have the same transmission to show the domain wall as the dark lines. There is also a faint striped texture observable. Figure 3.20 shows a mixture of stripes, 'bear paw' and 'tear drop' defect structures. The stripe direction corresponds to the alignment direction. Figure 3.21 shows denser stripes and a region with a zig-zag defect line. Figure 3.22 is a close-up of the zig-zag. Note that as it zigs and zags, the domain wall changes from black to white and then back. There is also a faint background pattern. Figure 3.23 shows isolated needle defects which is different from figure 3.21. Figure 3.24 shows the close-up detail of needle defects which have a pitch of $\approx 3\mu m$. Figure 3.25 shows how complicated things can become with both chevron stripe defects and a region with only two orientations being produced.

3.5.5 Optical Measurements

An optical system was developed to allow investigations of the SSFLC test cells (figure 3.26). The system is for examining transmissive cells at one particular wavelength. A collimated HeNe laser source ($\lambda = 633nm$) passes first through a polariser, then the LC cell, and then through a second polariser (analyser). The polarisers and the LC cell can be rotated. The resulting light is then collected on a photodetector, either a photodiode/integral amplifier, or a photodetector for a light meter. Before any electrical connections are made to the SSFLC cell, very useful measurements can be made. These include light losses through the cell, with or without polarisers and potential contrast ratios.

Typical measurements on a chevron structure test cell follow:

- With no polarisers, light level measured at $5.10^{+}_{-}0.02\mu W$, when SSFLC cell is introduced the level is reduced to $3.55^{+}_{-}0.02\mu W$: i.e. light transmission of cell is 70%. The loss is due to the missmatch of the layers of different refractive index, absorption in the ITO, scatter from any LC domain walls, and a lack of antireflection coating on the glass.

- With two polarisers and no SSFLC cell, one can observe the maximum and minimum throughput, to assess the quality of the polarisers. Minimum $= 0.25^{+}_{-}0.2nW$
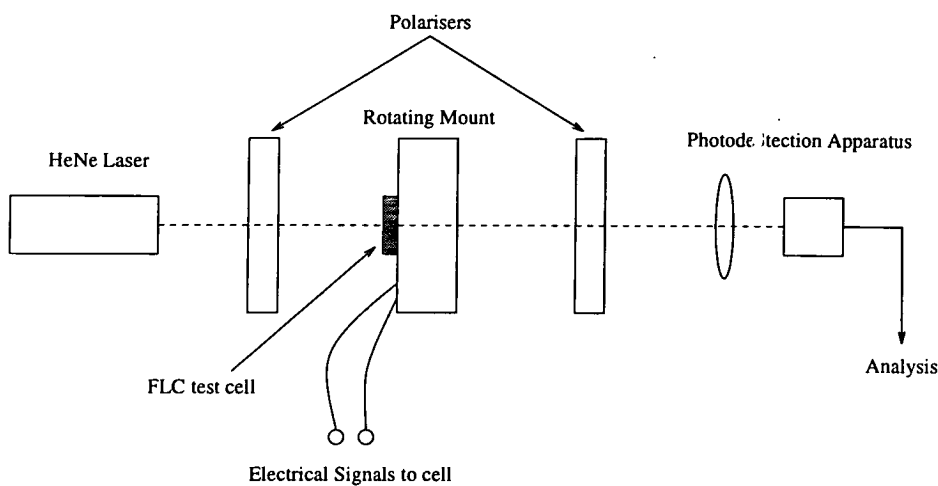
Figure 3.26: The optical system used for cell investigation

and maximum $= 380^{+}_{-}5nW$, which gives the maximum possible contrast ratio (the ratio of light transmitted **ON**, to light transmitted **OFF**) to be $1500:1$.

- Crossed polarisers (1st at $0°$, 2nd at $90°$), with no cell throughput is $6.4^{+}_{-}0.2nW$. With cell for maximum throughput, angle is $48.5^{+}_{-}1°$ and light level is $264.4^{+}_{-}1nW$. Therefore, in this configuration the transmission efficiency is 4%. With cell configured for minimum throughput, angle is $6.5^{+}_{-}1°$ and light level is $23.3^{+}_{-}0.5nW$. Therefore the static contrast ratio is $11^{+}_{-}1:1$.

- Parallel aligned polarisers (both at $0°$). With no cell, throughput is $745^{+}_{-}2nW$, with cell the maximum transmission is $557^{+}_{-}2nW$ at angle $-0.2^{+}_{-}1°$ (therefore transmission efficiency is 75%), the minimum transmission is $146^{+}_{-}1nW$ at $43.1^{+}_{-}1°$. Therefore the static contrast ratio in this configuration is $4^{+}_{-}0.5:1$.

The crossed and parallel orientations of the polariser seem to alter the measured gross static characteristics of the SSFLC cell. In a parallel configuration, the light throughput is is very high (in fact the polarisers improve the efficiency, but only after loss at the first polariser), but the contrast is low. The opposite situation occurs with crossed polariser orientation. This is understandable, considering the test cell in question was in the chevron structure and had many defects. If the cell was **ideal**, then the performance of both orientations would be similar, unlike the more complex situation.

3.5.6 Switching speeds and contrast ratios

To investigate the dynamic characteristics of the SSFLC cells, one must allow electrical signals to be applied to the SSFLC test cell and comparisons made with the optical response. So in addition to the optical system used in section 3.5.5, some electrical apparatus was added. This equipment is shown in figure 3.27. A bipolar pulse generator delivered specified pulses to the SSFLC test cell. All positive pulses were followed by an equal area negative pulse to retain the d.c. balance and avoid electrochemical degradation. Both the driving pulses and the resulting electronic signals from the light detection (photodiode/integral amp.) were displayed on a digital storage oscilliscope. This allows observation of the dynamic characteristics of the SSFLC performance and the ability to examine the maximum (**ON**) and minimum (**OFF**) **switched** states for one particular cell and polariser orientation. Examination of the switched states allows estimation of the switching speeds and contrast ratios, in a working environment. This is most useful for predicting the behaviour of SLM devices constructed with similar SSFLC structures.

Figure 3.28 shows the definition of switching time. The switching time is defined as the time of switching from 10% to 90% transmission. The dynamic contrast ratio is defined as the ratio of the switched maximum transmission (**ON**), to the switched minimum transmission (**OFF**). Figures 3.29 to 3.32 give some examples of typical SSFLC cell measurements. Figure 3.29 shows a measurement of the switching speed. The top trace shows the driving voltage and the bottom trace shows the optical response. In this case there is a $60^{+}_{-}10\mu S$ delay and then a $120^{+}_{-}10\mu S$ rise-time from 10% to 90% transmission for a $10V$ pulse. In this example the switching time would be quoted as $120^{+}_{-}10\mu S$, although this ignores the initial delay. Figure 3.30 shows non-bistable switching, where, after the driving voltage is removed, the orientation relaxes back to a previous state. In this case, the relaxed state is the same state as the negatively driven state, as no change is evident on the application of a negative pulse. The cell measured in figure 3.30 was in the chevron structure, exhibiting non-bistable switching, a low contrast ($10^{+}_{-}0.5 : 1$) and a low measured effective cone angle of $30^{+}2^{o}$, due to the molecular tilt (section 2.8). Figure 3.31 demonstrates the depolarisation field effect, described in section 2.5.2. As can be observed in the bottom trace, after initial reorientation, the FLC molecules relax slightly due to the depolarisation field, to reduce the switching angle, and ultimately to reduce the bistability of the SSFLC cell.
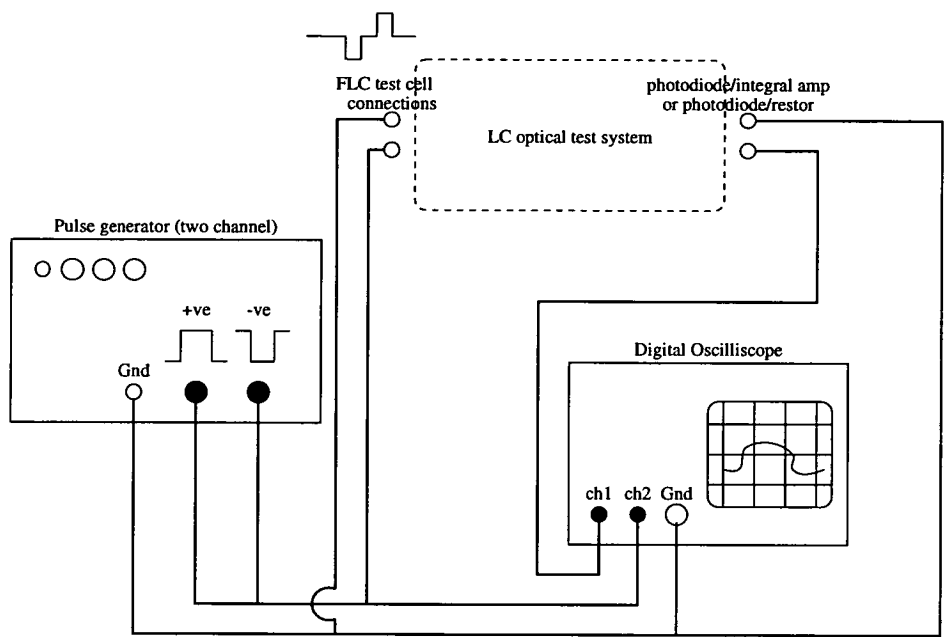
Figure 3.27: The circuit diagram used for cell investigation
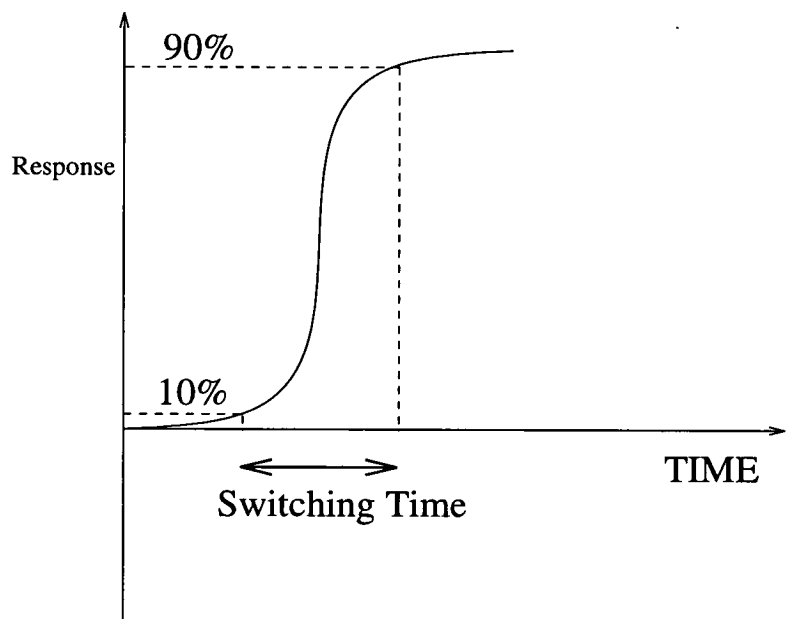
Figure 3.28: Measurement definitions
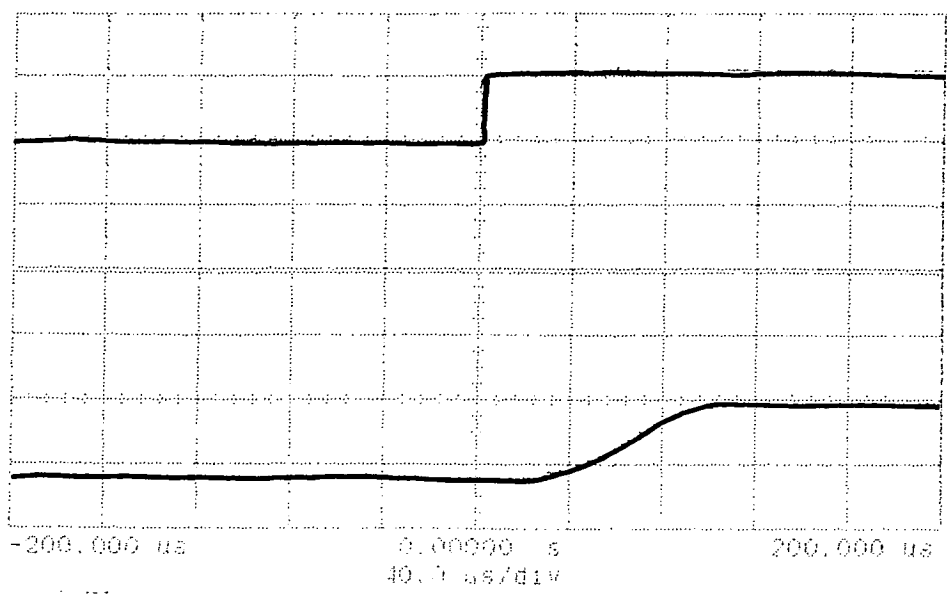
Figure 3.29: A typical switching speed measurement
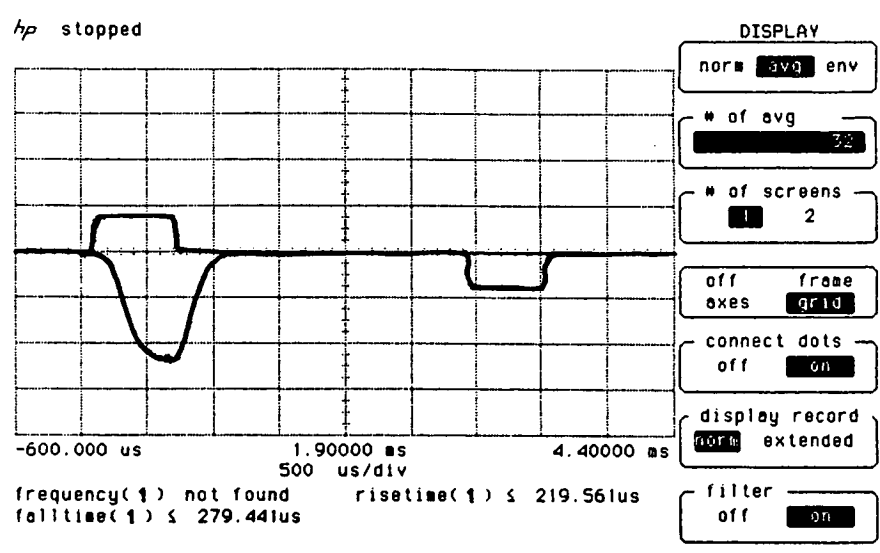
Figure 3.30: Non-bistable switching
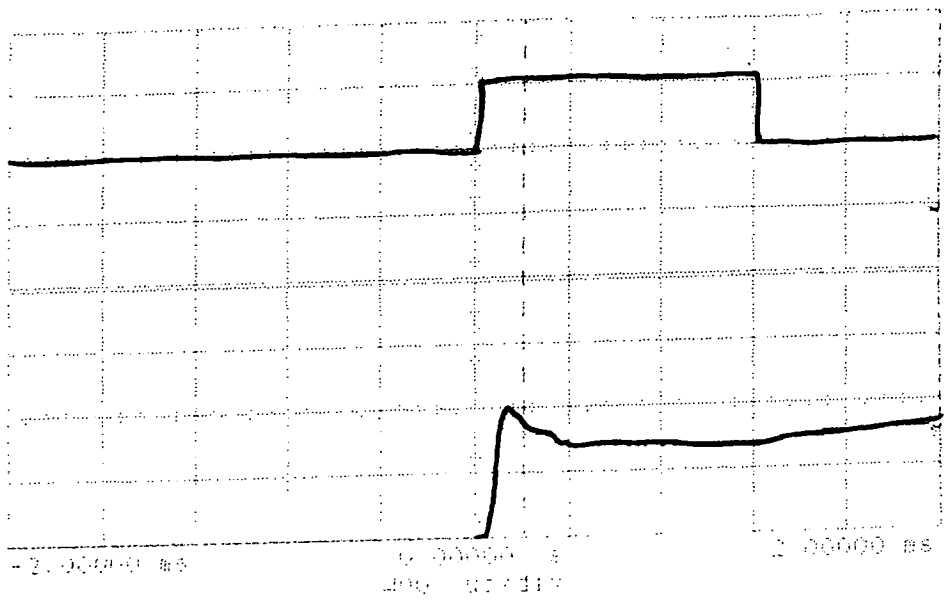
Figure 3.31: The depolarisation field effect

3.5.7   A.C. Treatment fields

Section 3.4 described how the chevron structure could be removed by the application of low frequency treatment fields. Low frequency pulses of up to ± 40 volts were applied to chevron structure SSFLC test cells. In general, the expected result of the removal of the chevron structure, and the generation of the bookshelf structure would be a bistable operation, increased contrast ratio (due to the reduction of the defects) and higher effective cone angle (towards $45°$). Figure 3.19 shows the domain combination, obtained after the removal of the chevron structure in the cell used in section 3.5.6. A very faint stripe can also be observed (section 2.8.1). The contrast has been increased from $10^{+}0.5 : 1$ to $100^{+}_{-}1 : 1$ and the effective cone angle is increased from $30^{+}_{-}2°$ to $43.5^{+}_{-}1°$. Figure 3.32 shows the bistable switching characteristics. If the separation between the two pulses is $\approx 1s$, the same characteristic results. The cell appears to be bistable over tens of seconds (observed qualitatively on a light box with polarisers). Optical throughput was measured as $30^{+}_{-}3\%$ for optimum contrast and $70^{+}_{-}4\%$ for optimum throughput. On occasion, the electrical treatment can cause cells to short circuit. This means that the cell will be unusable. This shorting is probably due to the high field carbonising any particulates or even the FLC material at very thin parts of the cell, and so making that region conductive.
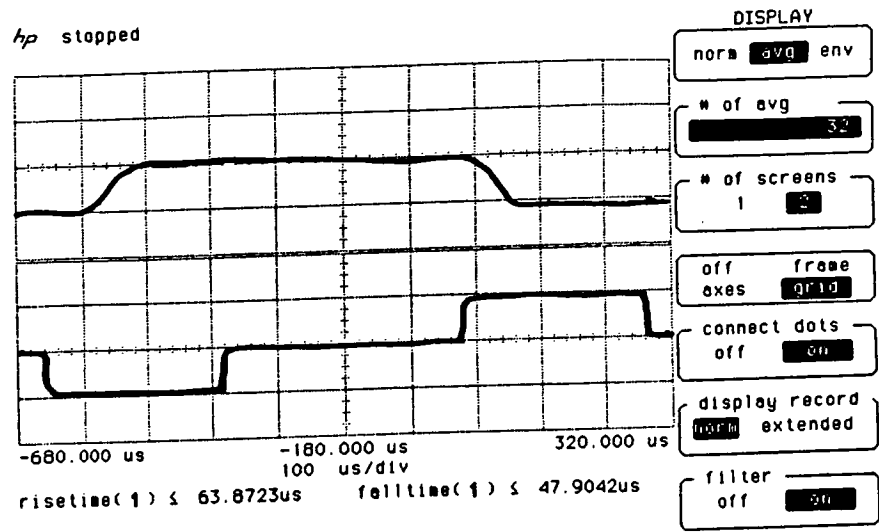
Figure 3.32: Switching characteristics after treatment

3.6 Discussion

Many of the ideas behind the fabrication and evaluation of FLC device structures have been introduced in this chapter. Many of the device fabrication issues have been discussed, with some of the more applicable techniques taken further and used for cell development. The cell fabrication techniques include:

- Use of thin commercially coated ITO glass.

- SiO_x alignment layers.

- Spacer balls in glue for cell construction.

- A transmissive cell structure.

- Vacuum filling at high temperature.

Various appraisal techniques have been examined. Potentially the most useful for SLM development are:

- The examination of white light fringes to assess cell uniformity/flatness.

- Examination of FLC defects to assess alignment quality.

- Dynamic electrical and optical measurement of device parameters for comparative studies.

- Appraised *in situ* and therefore special instruments not appropriate in many cases.

One is now is a position to make more detailed investigations into FLC device performance, particularly the SSFLC structure, but also the Distorted Helix Effect, the Soft-mode Electroclinic Effect and the Twisted Smectic devices. This will be addressed in the next chapter.

Chapter 4

Further FLC Investigations

Many of the techniques available for fabrication and appraisal of FLC devices, were
introduced in chapter 3. In this chapter some of the more interesting and applicable
techniques for FLC device structures are investigated. As an introduction, an example
of the assembly and assessment of a single type of SSFLC test cell will be presented
in detail to examine reproducibility. Some of the various fabrication variables will then
be examined to give an indication of suitable SSFLC structures for SLM construction.
Preliminary investigations into some of the other FLC device structures will also be
discussed. This allows a comparison of the various device structures producable by the
author. This gives an insight into the projected performance of these structures when
applied to VLSI backplane SLMs.

4.1   A Specific SSFLC Cell Development Example

To examine reproducibility in the fabrication of test cells, one particular combination of
test cell parameters was used to construct four test cells. Due to the degree of difficulty
in fabricating these devices, the experiment was limited to 4 cells, as this was considered
the minimum for a useful investigation. These test cells could be compared to assess if
the resulting performances were similar.

4.1.1 Cell Fabrication

SCE13 (Merck-BDH), an FLC material with a high spontaneous polarisation, and hence fast switching time, was selected. Due to the limited range of spacers rods (Nippon Glass) an intermediary cell thickness of $1.7\mu m$ was selected. A MAD alignment structure was decided upon, obtained by $60°$ oblique evaporation of SiO_x to a depth of $100nm$.

Eight $8mm^2$ ITO coated glass samples were cut from the Hoya†glass plates (section 3.1.3, protected with photoresist). The samples were cleaned with an organic solvent cleaning technique (section 3.1.2). The alignment layers were evaporated as described above (section 3.3.2). Four cells were constructed using a UV cure glue (Norland 68) and spacer rod mixture with a vacuum packing proceedure during curing. The cells were examined for white light fringes to assess the cell flatness. The cells were filled with liquid crystal as described in section 3.1. They were then examined under white light and crossed polarisers to assess the cell uniformity from polarisation colours. The cells were given a heat treatment in an oven and cooled from $145°C$ to room temperature at $\approx 0.1°$ per minute. Electrical contacts were applied with thin wire and conducting glue, and the cells were glued to a small plate to allow mounting on a rotational mount. A resistance meter was used to check the cells for short circuits. The devices were assessed for switching time and contrast ratio. A square wave of frequency 10Hz, voltage $40 - 60$ V pk-pk was applied until the cells showed signs of bistability i.e. retained one or other state when the waveform was removed. The devices were re-assessed for switching time and contrast ratio.

4.1.2 Test Cell Summaries

Figure 4.1, tabulates the results for the four test cells at each stage. Reference to the figures 4.2 to 4.4 are made in the table. Figure 4.2 shows the defect patterns in cell 1, just after it has been filled and allowed to cool. Figure 4.3, shows the same cell after some electrical treatment, but not yet exhibiting bistablity. Figure 4.4, shows cell 3 after electrical treatment. The cell is bistable, but the two domains follow the defects observed before treatment. This suggests, that although the electrical treatment can flatten the chevron kink and result in a bookshelf structure, the treatment will not compensate for

† page 173
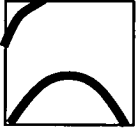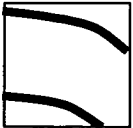
	CELL 1	CELL 2	CELL 3	CELL 4
Fringe pattern on construction ↑ alignment direction				
colour variation	uniform white	uniform white	yellow to pink	uniform yellow
Voltage at which bistability was obtained	40V pk-pk	18V pk-pk	40V pk-pk	18V pk-pk
Final (max) contrast ratio error 10 percent	100:1	40:1	120:1	10:1
Switching Speed (10V) Error 10 percent	120uS	100uS	120uS	140uS
Defects	Needle/stripe defects perpendicular to alignment small domains crossing stripes. (figure 4.2) After bistable, two large domains formed, still with fine stripe texture. (figure 4.3)	Needles/stripe defects Also large domain in centre. After bistable, many domains with the large domain much more dominant.	Needle/stripes plus perpendicular bands and a very prominent messy background "scribble". Bands and scribble become zig-zags as treatment progresses. When bistable, the domains follow the scribble pattern (figure 4.4).	Needle/stripes plus rough lines. Zig-zags form as treatment progresses. Bistable defects follow the rough lines.

Figure 4.1: Results for the four test cells.
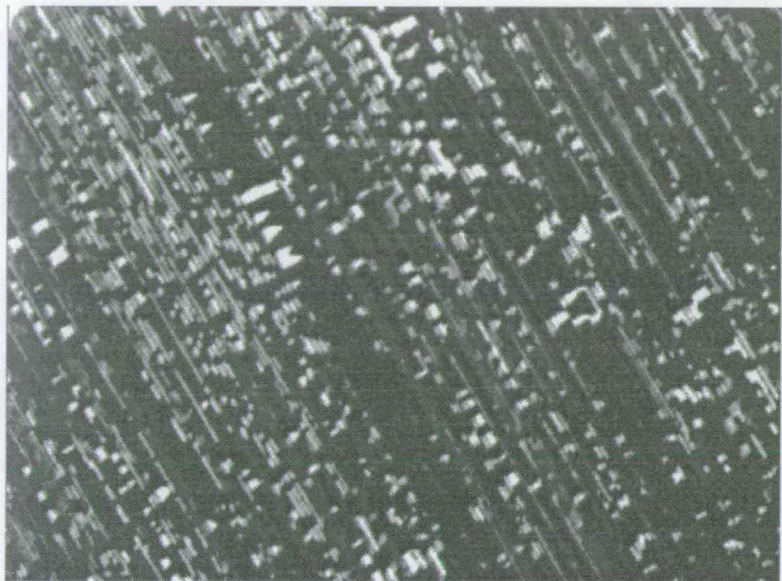
Figure 4.2: Initial stripe pattern on cell 1.
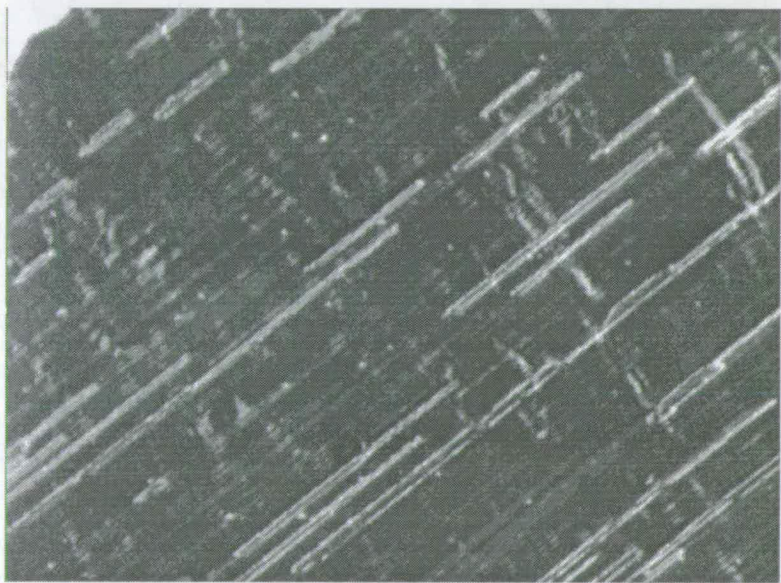
Figure 4.3: The stripe pattern is reduced as treatment ensues (rotated $\approx 90°$ compared to figure 4.2)

inhomogeneities or errors in the alignment layers.

Figure 4.4: Domain structure in bistable cell 3.

4.1.3   Discussion on the four test cells

As can be seen in the table (figure 4.1), the cells produced do not follow completely identical lives. Nevertheless, certain general characteristics are discernible from the results. The characteristics the cells all share are:

- The uniformity of thickness of the cells is good to an order of $0.5\mu m$, and appear reasonably uniform (colour) when filled with FLC.

- The uniform colour should allow a uniform contrast across the cell (to the naked eye $\approx 10\%$).

- The cells are readily made bistable at voltages between 30V and 60V pk-pk.

- Initially the cells have needle like defects with some zig-zags.

- These defects get fainter as the cell is electrically treated.

- When bistable the cells have two domains with different director directions.

- These domains seem to follow initial defect structure apparent on first filling.

- In one of these domain regions the contrast is > 100 : 1.

- The overall device will have a contrast dependent on the distribution of the two domains.

- These domains still retain a faint striped texture.

The FLC structure in the cells changes from chevron to bookshelf through the electrical treatment, but it is difficult to assess from these results a more precise description of these structures, i.e. their asymmetry, tilt angles or general molecular orientation. It would seem from the data that the main immediate area for investigation would be to repeatably obtain monodomain samples. In the two domains the smectic layers line up with the alignment layers but with the molecular directors (in either of their switched states) pointing in opposite directions i.e. one domain pointing left from the direction of evaporation and alignment layer and in the other domain right. This was discussed in section 3.3, with regard to SAD and MAD alignment structures. Either a more asymmetric MAD structure is required (perhaps through different evaporation conditions), a SAD structure is required or a combination of the two (MAD/SAD). The next section hopes to gain a fuller insight into these parameters although the limited reproducibility of cell fabrication casts doubt on the potential for detailed results.

4.2   Full Factorial Analysis on SSFLC Cells

The work so far has shown that there are numerous options for the physical design of the SSFLC device cell. The choice of FLC material is largely dependent on the availability from the suppliers. A material with a high spontaneous polarisation is an obvious candidate due to the advantages of fast switching times. For half-wave plate amplitude modulation a cone angle of 22.5° is required. SCE13 (Merck-BDH) is the most obvious material choice currently available for SLM requirements. But the selection of the device characteristics remains unsolved. In chapter 2, the most sensitive area determining device performance would seem to be the energy transferred to the bulk FLC. The main controllable parameters which influence this are the alignment layers and the thickness of the cell. An attempt was made to investigate these parameters in a controlled

set of experiments using a Full Factorial Experimental Design Technique [113]. These experiments were only partially successful, as will now be discussed.

4.2.1 Full Factorial Experimental Design

The main objective of this Full Factorial technique is, after having pinpointed the most important device variables, to separate and quantify the main and interaction effects of these variables [113]. This should result in an optimum set of device parameters for certain desired performance characteristics. Full factorials are used to investigate four or fewer variables. The main advantage of this proceedure is that the chosen variables are tested with all levels of every other variable. Therefore, all possible combinations of factors and levels are tested, allowing all complex interaction effects, second order, third order etc. to be investigated. Second order interaction has two variables interacting with one another and third order has three variables interacting to produce the result. With three factors, each with two levels, there are 2^3 or eight combinations, therefore, eight experiments are required. But to reduce the residual error inherent in all experimentation, these eight experiments should be repeated, making a total of sixteen. The sequence of experiments should not be performed in a methodical, predictable manner, but should be randomised. This allows any parameters, such as the temperature variation, to be allowed an equal opportunity to effect all the experiments. A Full Factorial Analysis includes the following steps:

1. Select the factors to be investigated, based on previous experiments and/or judgement.

2. Determine two levels for each factor, i.e. high value/low value.

3. Draw up a matrix showing the combinations by which each factor is tested with each level of every other factor.

4. Randomise the sequence of experiments.

5. Run an experiment with each combination in the sequence indicated by the random ordering.

6. Record the outcome of each experiment.

7. Repeat steps 4 to 6 with a new random ordering.

8. We are now in a position to examine in detail any complex interaction between the variables.

As has been previously discussed, the alignment layer and the cell thickness would seem the most obvious candidates for investigation. Three variables were selected each with two levels: Alignment layer angle, MAD and SAD; Alignment layer thickness, thin (10nm) and thick (100nm); and cell thicknesses, $2\mu m$ and $3\mu m$.

4.2.2 Failure of the Full Factorial Analysis

With three variables, 2×8 test cells were constructed for each experiment run. The full set of experiments were twice repeated fully. The FLC alignment quality, defects, switching time, contrast ratio and bistability were the specific cell characteristics under investigation. It had been assumed naively that it would relatively straight forward to distinguish which variables resulted in the best and worst results for each test cell. In general, within experimental errors, it became very difficult to distinguish between the various performance characteristics for each test cell and if differences occurred, they were not repeated on the second full experimental run. This meant that any detailed experimental conclusions could not be made. The Full Factorial Analysis was essentially inconclusive. Only certain general statements and impressions can be made regarding the results of the experiments. Probably two of the main factors for the failure of this set of experiments is the irreproducibility of the SiO_x evaporation which is very difficult to control accurately and guarantee reproducible rate, angle and depth. The construction of the cells is still not fully satisfactory, resulting usually in non-flat cells (at least $0.5\mu m$). Varying and nonuniform cell thickness is most likely to mask any subtle effects due to the various experimental variables. Therefore, using these cells, only the most general statements can be made concerning the effects of some of the experimental variables. With the recent acquisition by the Applied Optics Group of a new evaporation system, allowing much improved and more controllable deposition and with more recent improvements to the FLC cell construction techniques for test cells, a Full Factorial

Analysis should be attempted once more. The fruits of such an improved investigation should yield very interesting results.

4.3 Qualitative SSFLC Device Results

Test cells from the Full Factorial Analysis and additional cells with specific characteristics were used for a more general investigation of SSFLC device behaviour. Summaries of the results are discussed here. The qualitative conclusions of the study are:

- Thin cells gave the fastest switching times, typically $80\mu S$.

- Most uniform FLC alignment in chevron structure was obtained from MAD alignment.

- Most uniform FLC alignment in bookshelf structure was obtained from SAD alignment.

- Cell thickness (fringes) was more uniform for thin alignment layers.

- MAD alignment required lower treatment voltages to achieve bistability

- The contrast ratios, on average, were all macroscopically similar, with chevron structure $\approx 10 : 1$ and bistable bookshelf $\approx 100 : 1$

Some of these observations can perhaps be explained from discussions in previous chapters. The most obvious is that the switching time depends on the cell thickness. A thin cell will result in a higher electric field across the FLC material, for a constant voltage, and so aid the switching mechanisms (higher V/m).

4.4 Soft-Mode Electroclinic Device Investigations

Only limited experiments could be attempted to investigate the Soft-mode Electroclinic effect. This was mainly due to the lack of suitable temperature control of the test cells

in the optical test system.

4.4.1 Fabrication Description

The Soft-mode Electroclinic effect requires no Surface-Stabilisation (section 2.5 and 2.10), therefore only a thin $30nm$, $60°$ (MAD) SiO_x alignment technique was employed. It was hoped that the thin alignment layer would only contribute enough energy to give a preferential director orientation. The cells were $3\mu m$ thick and fabricated as described in section (3.1). The cells were filled with 764E (Merck-BDH). On observation of the polarisation colour in the cell, the cells were comparable in quality to SSFLC cells.

4.4.2 Experimental Measurements

A very crude method was employed to gain some insight into the device characteristics. A glass thermometer was placed in contact with the test cell in the optical test system. The test cells were heated up using a heat shrink gun. With carefull use, the temperature could be regulated to $\pm 5°$, which was adequate for this preliminary study.

Cell investigation apparatus was as described in section 3.5. At room temperature (20°C) the switching time for a 12V pulse was measured as $40 \pm 5\mu S.$, but the contrast was relatively low at $2 \pm 0.2 : 1$. This corresponds to a small deflection of the director as described in section 2.10. The cell was then carefully heated up. As it approached approximately $60°$, the switching time decreased to $10 \pm 3\mu S$ but the contrast reduced so as to be unmeasurable within experimental error bounds i.e. below the noise level.

4.4.3 Discussion on the Soft-Mode Electroclinic Device

These experiments, give some preliminary indictions as to the nature of the device characteristics. It was deemed that the experimental apparatus fell short of that required for a deeper study of cell performance. However, some successfully working cells were

fabricated and found to operate reasonably well. More detailed studies of this effect are required, perhaps using Peltier cells to allow more accurate temperature control.

4.5 Distorted Helix Effect Device Investigations

Section 2.9 described how the DHE requires very low surface energy and FLC material with a very short helical pitch. Various FLC test cells were fabricated to examine the conditions favourable for the DHE. A decision was made to limit the experiment to varying the bounding plate surface treatment. The thickness of the cell would also have a bearing on the effect of boundary conditions in the bulk, but this was held constant to allow the use of standard fabrication proceedures. Four surface treatments were examined, in order of increasing surface energy (section 3.3):

- No surface treatment

- Rubbed ITO

- Rubbed PVA (spun-on)

- Obliquely evaporated SiO_x, 60°, 30nm

The cells were fabricated as in section 3.1 to give a thickness of $3\mu m$. The DHE FLC material used in the experiments was FLC8823 (F.Hoffmann-La Roche and Co. Ltd.). Only the rubbed PVA technique resulted in a satisfactory device for experimentation. The weaker surface treatments did not give sufficient energy to the bulk FLC to attain good alignment of the smectic planes and a milky texture of microdomains resulted in the cells. For the obliquely evaporated SiO_x technique an SSFLC device structure resulted. This was to be expected due to its relatively strong surface anchoring energy. Thus for thin cells of the order of $3\mu m$ thick, a rubbed PVA (or nylon) surface treatment technique gives sufficient energy to attain a bookshelf structure but not so much as to generate a SSFLC structure with this particular DHE FLC material.
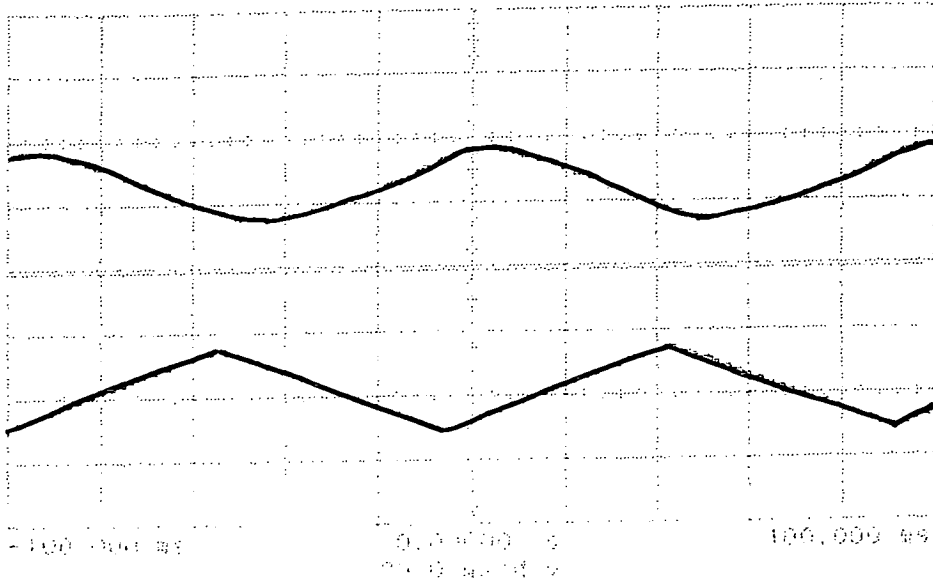
Figure 4.5: Analogue modulation with the DHE device

4.5.1 Quantitative Results

Having decided upon a repeatable fabrication technique for the DHE, electro-optic mea-
surements were performed with the aid of G.Springer. The optical and electrical mea-
surement apparatus was as described in section 3.5. The electrical signals were bipolar
to retain zero d.c. voltage balance and so avoid electro-chemical degradation. Triangular
waveforms were used to examine the analogue switching capacity of the device and the
critical field for the unwinding of the helix. Pulses were employed to measure the switch-
ing time and contrast ratio. The cell and crossed-polariser orientations were adjusted for
the optimum results in each case. Optical throughput was measured at $8^{+}_{-}1\%$ and the
losses are mainly due to scattering effects and the LC domains. Figure 4.5 shows typical
analogue switching (top waveform) for a bipolar triangular signal of 3 volts pk-pk and
a period of $100mS$ (bottom waveform). The onset of complete unwinding of the helix
was observed with the flattening of the optical modulation at nearly 6 volts amplitude.
Bipolar pulses have shown a full switching contrast ratio of 12 : 1 and a switching time of
$1mS$. The relatively low contrast ratio seems to be due to the large amount of scattering
of light by the device so adding to the background and the non-ideal alignment of the
director. The scattering effect is probably inherent in the device due to the comparable
dimensions of the helix and the wavelength of light. Any defects in the required director
orientation alignment could be improved by heat and electrical treatment as with the

SSFLC devices. The relatively slow speed is for full switching, but for switching up or down a few grey levels, a much faster response would be obtained. The analogue switching itself is not completely linear and asymmetric switching has been noticed. Also, the future level depends somewhat on the current state, so some hysteresis has been evident. The distortion of the helix also depends on the operating temperature but no detailed study of this has as yet been undertaken.

4.5.2 DHE Conclusions

The DHE is undoubtedly a highly interesting device structure and appears promising for the realisation of fast analogue optical modulation. This study has shown that such devices are achievable, although at present require some development. One of the main problems would seem to be the scattering effects, although F.Hoffmann-La Roche are apparently examining this problem [97]. **Repeatable** grey-level response with the DHE is probably not completely attainable with the materials currently available. If only a relative analogue response and not an absolute response is required (i.e. slightly more or less light and not a precise quantity), and the scattering effects can be tolerated, then the DHE device described above could be a very useful low voltage analogue modulator.

4.6 Twisted Smectic Layer Device Effect

Section 2.11 described how a twisted smectic layer structure could perhaps be produced by orientating the top and bottom alignment layers in a cell orthogonally.

4.6.1 Fabrication Description

A number of cells were fabricated with orthogonally orientated alignment layers. The alignment layers were $60nm$ thick and evaporated at $60°$ degrees (MAD). This should cause a relatively high anchoring energy to align the smectic layer with the alignment
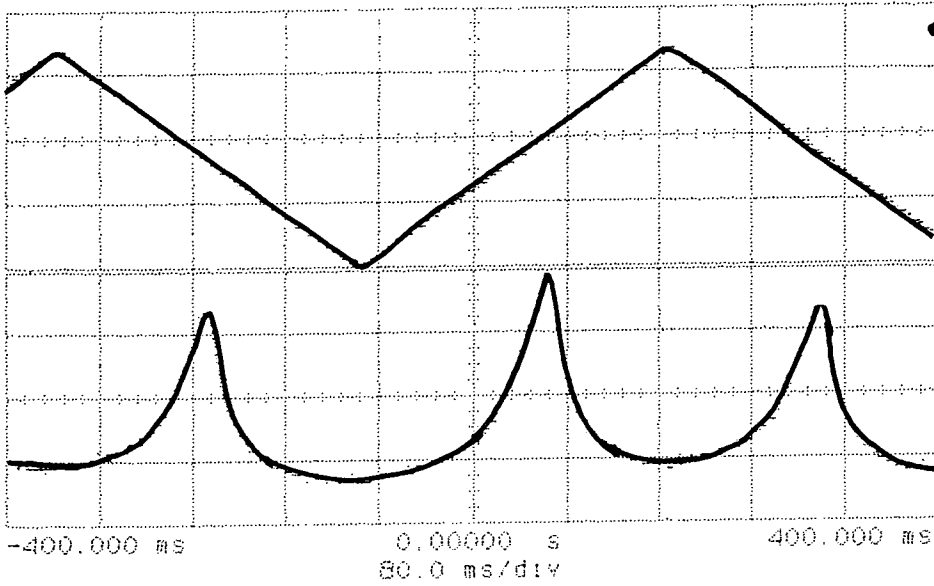
Figure 4.6: Analogue switching of the Twisted Smectic device.

direction at each bounding plate (section 3.3). $3\mu m$ thick cells were then constructed as described in section 3.2 and the cells were filled with SCE13 FLC material.

4.6.2 Experimental Measurements

When suitably orientated with crossed polarisers, the test cells rotated the light sufficiently for $10^{\pm}1\%$ intensity transmission. Application of voltage pulses destroyed the waveguiding effect, and reduced the light transmission. In this manner a contrast ratio of $20^{\pm}1 : 1$ with voltage pulses of 10 volts was measured. The switching time (time to destroy the wave-guiding effect) was measured at $400\mu S$ and the relaxation time (time for the twist in the layers to reform) was measured at $2mS$. The non-linear behaviour of the analogue switching is demonstrated in figure 4.6. This shows the response of the cell to a triangular waveform, which does not follow the driving voltage very well. Figure 4.7 shows a graph of the optical output against voltage for $20mS$ pulses. This graph also shows some non-linearity and the effect saturates (i.e. wave-guide is completely removed) at 1.5 volts.
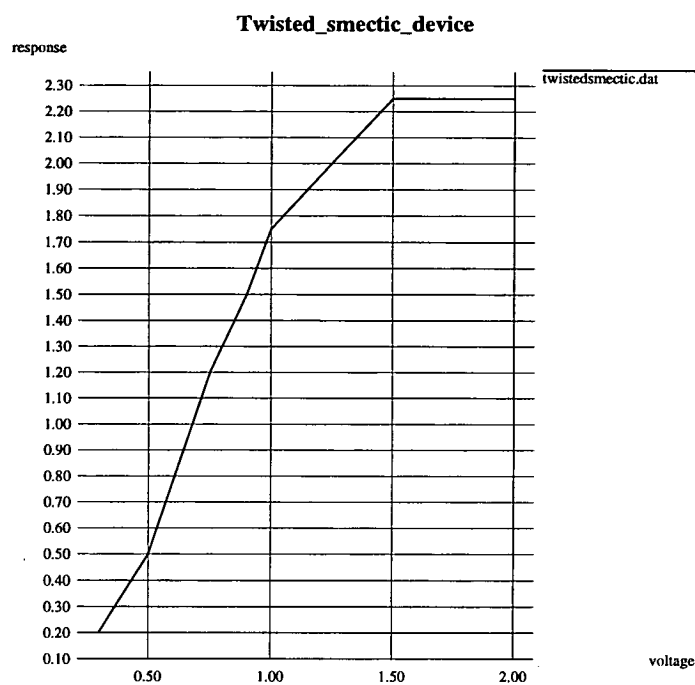
Figure 4.7: A graph of voltage versus optical output.

4.6.3 Discussion on the Twisted Smectic device

This study on the Twisted Smectic device has been very brief. Working devices have been investigated, but no attempt has yet been made to optimise the effect. In a similar way to the DHE, only low driving voltages are required for a moderately good response. The analogue response is very non-linear, but still usable. With further experimentation, device performance could be improved, but again, this must be left to future researchers.

4.7 Discussion

The achievements so far allow for useful SLMs to be constructed from FLC device structures. A summary of the device characteristics discovered in this chapter is shown in table 4.1. The most important device structure was found to be the SSFLC, although a number of the other types of device have been examined. The other types, particularly the DHE and Twisted Smectic, seem particularly suited for low voltage analogue

FLC structure	modulation mode	voltage range	contrast	switching
SSFLC	binary, amplitude or phase	$\approx 2 - 60$ volts	100 : 1	$\approx 100\mu S$
DHE	analogue, amplitude **and** phase	$0 - 6$ volts	12 : 1	1mS
Twisted smectic	analogue, amplitude **and** phase	$0 - 1.5$ volts	20 : 1	$400\mu S, 2mS$
Soft-mode device	analogue, amplitude or phase	$0 - 60$ volts	2 : 1	$10\mu S$

Table 4.1: Summary of FLC devices investigated in chapter 4

modulators. The main conclusions of this chapter are:

- The SSFLC is the most mature device structure.

- The SSFLC has the most suitable characteristics for use in LC over silicon SLMs, i.e. binary switching, high contrast, fast switching.

- Typical operating device characteristics include: contrast 100 : 1, switching time $100\mu S$ at 10 volts, optical throughput of 70%.

- Uniformity is the most critical parameter at present.

- DHE obtained by rubbed PVA alignment, showed low contrast (10:1), and analogue response was obtained at low voltage.

- Soft-mode Electroclinic showed fast switching time (temperature dependent) but a very low contrast (2:1).

- Twisted Smectic structure had a moderate contrast (20:1) and a very asymmetric analogue response.

The SLM development in the next chapter will therefore utilise the SSFLC device structure.

Chapter 5

Spatial Light Modulator Development

In the previous chapters, the issues involved in FLC fabrication have been considered and the resulting device characteristics have been studied. It is now prudent to turn one's attention to the development of SLM devices. The particular emphasis will be on the development of two VLSI backplane devices, the 16^2 and the 176^2. The goal of this work is to produce suitably working devices for evaluation and to make devices available for system application work.

Technical help for this work includes assistance from A.Garrie for the running of the clean room, **A.Ruthven** for dicing the chips and glass, and bonding the chips. Also, D.C.Burns for help in electrical testing of the 16^2 chips, and the construction of the interface and software for the 16^2 devices is acknowledged.

5.1   Ferroelectric Liquid Crystal Cell

We concluded in chapter 4 that the the SSFLC device is the most developed and suitable device structure for binary state modulator pixels. The study showed that thin SiO_x alignment layers would be the most suitable option for VLSI silicon devices, being the most reproducible at this stage and causing no detrimental effects. The specifications of alignment layers were chosen to be the mean of the various values investigated in chapter

4, as the cell performance is highly dependent on substrate quality, cell thicknesses and uniformity. Many of the test cell experiments in chapter 4 should be repeated for SLM fabrication, but due to the limited number of expensive backplanes, this was (and is) not possible. Therefore, a single MAD evaporation of 60°, thickness $60nm$, was selected to produce relatively well aligned devices. It should be stressed that at this stage, it was important that **working** devices were fabricated and made available for system experimentation.

Only with a large number of VLSI backplanes available will a complete study of FLC cell fabrication on VLSI backplanes be achieved. Now that the important parameters have been identified in chapters 3 and 4, this should be not too difficult an undertaking.

5.2 Backplane Considerations

A VLSI backplane is considerably different from a simple glass substrate for the fabrication of FLC devices. This will now be discussed.

5.2.1 Pixel Mirrors

The modulator pads on a VLSI backplane are aluminium electrodes. Typically, they are fabricated through standard VLSI processing techniques for optimum electronic performance and with little regard for the optical implications. This results in a rough granular mirror, with low reflectivity. With the mirror consisting of aluminium, this results in a different substrate material (also a rough topograghy due to the grains) onto which the alignment layers are deposited. This will produce different cell boundary conditions, compared with the ITO electrode. The mirrors have a finite dimension compared to test cell electrodes (which can be assumed to be infinite in extent by comparison). This will result in boundary constraints around the edge of the mirror, and perhaps noticable effects across the mirror area.
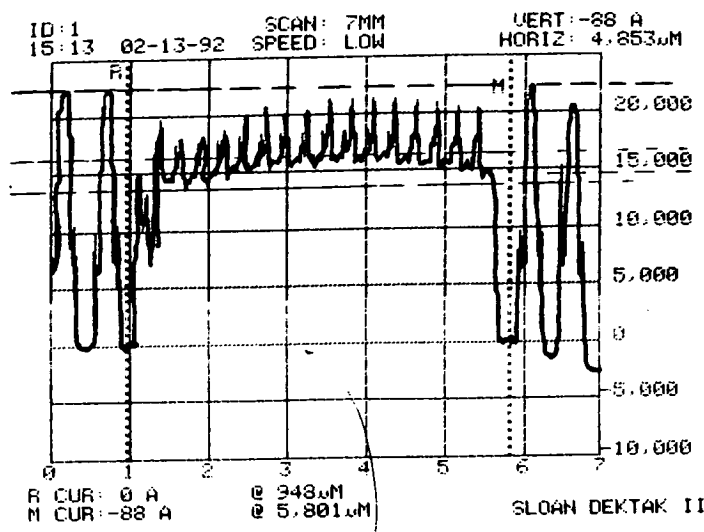
Figure 5.1: A surface profile across the 16^2 backplane.

5.2.2 SLM Circuitry

In general, at each pixel mirror, there is at least one storage transistor circuit and running between the pixel, there are at least row and column address lines, and potentially clock and other control lines. This means that the flat area of the pixel has usually a < 50% flat fill factor. One may simply allow the pixel mirror to cover all of the circuitry and address lines with a top level metal. Unfortunately, the mirror then has multiple heights due to the circuit topography. This variation will be of the order of a micron, potentially the thickness of the cell, and so does not permit the fabrication of LC with a uniform cell thicknesses over the whole pixel. In general, it has usually been found best to allow the pixel mirror to cover only a flat area of the silicon. This important point will be discussed more fully in section 5.7, with regard to planarisation. Figure 5.1 shows a typical tally step scan across the 16^2 SLM devices. The circuitry features around each pixel are of the order of $0.5\mu m$.

Around the pixel array, there may also be data shift registers or data decoders, which transfer the data and control signals, input to the device, to the pixel elements. Bonding pads are to be found, usually at the periphery of the chip. These are required to allow gold bonding wire connections to the chip package (and ultimately external devices) to be made. The position of the bonding pads limits the extent of the cover glass, and is a

significant constraint.

5.2.3 Reflection Mode

For visible wavelengths, silicon is opaque. Therefore, SLMs based on LC over VLSI silicon must operate in a reflection mode. The main consequence of this is a somewhat more complicated optical set-up for their use. In general, beam splitters are employed. Although, if one required compact optical systems, reflection mode devices do facilitate simple bending of the optical beams with potentially fewer components.

As discussed in section 3.2, the main practical device implication of reflective operation is in the selection of the FLC cell depth. For SSFLC material with $\Delta n = 0.15$, $\lambda = 633nm$, equation 2.8 gives a reflective cell depth of $1\mu m$ or $3\mu m$ for a switchable half-wave plate. This takes account of the double pass through the FLC material on reflection. The double pass will also mean that any non-uniformities and defects will cause twice as much disruption as one would expect from a transmissive device.

5.2.4 The Problem with DRAM

A simple DRAM pixel consists of a transistor gate connected to the row address line, with the transistor source connected to the column address line and the transistor drain connected to the pixel mirror. To place charge on the mirror, the row line is addressed to allow the gate to open and allow charge from the column line to flow onto the mirror. This means that the row addressing time must be such as to allow enough charge to flow onto the pixel mirror which is effectively a capacitor. This charge must be enough, to produce the voltage required for SSFLC switching and latching. The charge required for switching of the SSFLC is $2P_sA$, where P_s is the spontaneous polarisation and A is the area of the mirror. In general the line addressing time is much shorter than the switching time of the FLC. For faster switching FLC materials a higher P_s can be designed. But, this high P_s will require a longer line addressing time to achieve adequate charge transfer for switching. The consequence of this is that there is a trade-off between P_s and line addressing time to achieve fast frame rates. For large arrays, a fast line time is desirable

for high frame rate. A slower switching FLC material (i.e. lower P_s) material would be more appropriate to achieve this desired frame rate. The above discussion does not apply to SRAM pixels as the charge to the mirror pixel is supplied from the power lines and not the addressing lines.

DRAM also suffers from photo-induced charge leakage. Incident light on the circuitry can induce charge carriers in the silicon. In DRAM the data is stored on a capacitor, which can more rapidly discharge due to the generation of these charge carriers. SRAM is not susceptible to this problem as the charge is continually drawn from the power supply lines.

5.3 16^2 SLM Device Construction and Evaluation

This section deals with the fabrication and evaluation of a specific SLM device, the 16^2 SLM.

5.3.1   The 16^2 SLM

The 16^2 SLM backplane used was a redesign of the original nMOS SRAM device designed by I.Underwood [36, 37, 114]. The backplane was fabricated using a $6\mu m$ nMOS p-well process, at the Edinburgh Microfabrication Facility (EMF) at the University of Edinburgh. The backplane consists of an array of 16^2 pixel elements each incorporating an SRAM memory latch connected to an aluminium mirror element via an exclusive OR gate. This circuit allows data to be stored at the pixel on a latch, which defines whether the FLC element is to be **ON** or **OFF**. The actual signals to the FLC element are obtained from the output of the exclusive OR gate, which by means of a comparison with a global clock (related to the front electrode signal), either switches the FLC **ON** (positive pulse across FLC), switches the FLC **OFF** (negative pulse across FLC), or performs **NO CHANGE** (no voltage drop across the FLC). By various combinations of these signals (i.e. various drive schemes) one can obtain full d.c. voltage balance across the FLC material and display patterns. If the FLC is not bistable (**non-fully bistable**),
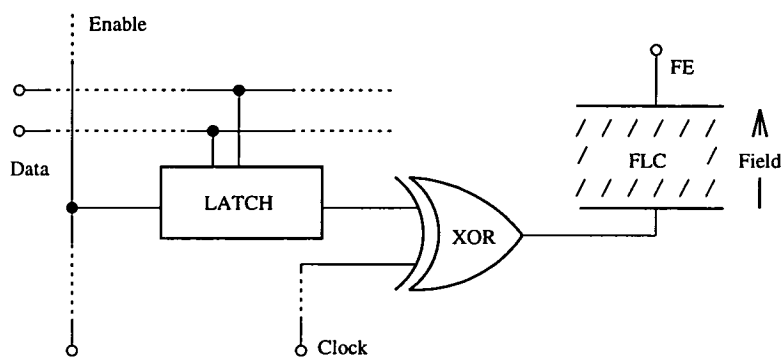
Figure 5.2: A schematic of the pixel circuit on the 16^2 SLM.

this full d.c. balance can be achieved at the expense of having the pattern only available for 50% of the time, the other 50% of the time there is no pattern. Figure 5.2 shows the schematic for this pixel circuitry.

The pixels are on a $200\mu m$ pitch with mirror area $110\mu m \times 110\mu m$. Figure 5.3 shows an interferogram of the SLM backplane. A special feature of this SLM design is the incorporation of polysilicon/metal structures around the pixel array to act as FLC cell spacers. The device can be driven at voltages up to $13V$. The device is interfaced to a PC IO card with a custom buffer circuit. The PC software for driving the SLM and the interface were designed by D.C.Burns. The device can be addressed at up to a 10kHz frame rate [114].

Only a limited set of tests could be performed on the backplane to assess whether it was electrically functioning. The most useful was measuring the current required by the device to check for electrical shorts (a fatal flaw). Electrical probing of the wafers was performed in collaboration with D.C.Burns. Only a limited number of wafers were available for use. Of these, only half of them showed any signs of electrical functioning. Devices on the more promising wafers were individually tested to select likely fully working devices. The resulting yield of working devices was very low and varied considerably from wafer to wafer, so only a handful of backplanes were available for FLC cell fabrication. Many of the disfunctional backplanes were used for cell fabrication practice.
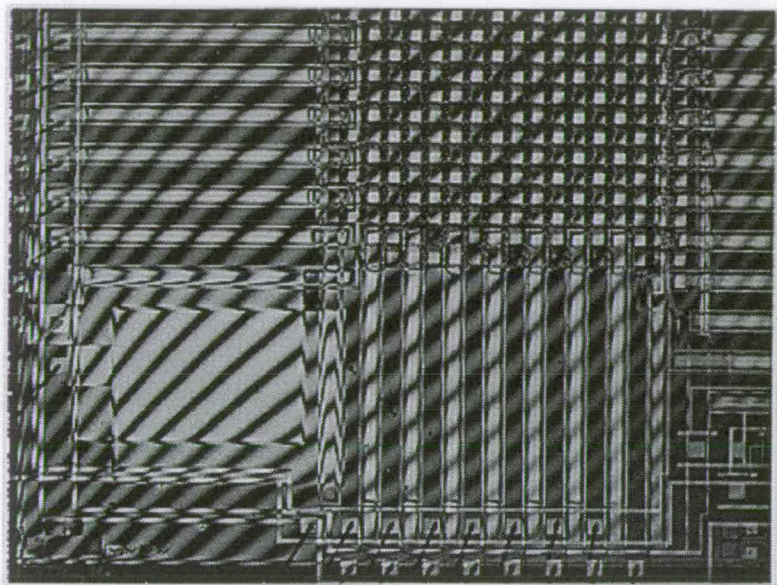
Figure 5.3: An interferogram of a 16^2 backplane (I.Underwood), at the top right is the pixel array, the top left and bottom right shows the poly/metal spacers and the bottom left shows the large metal FE pad.
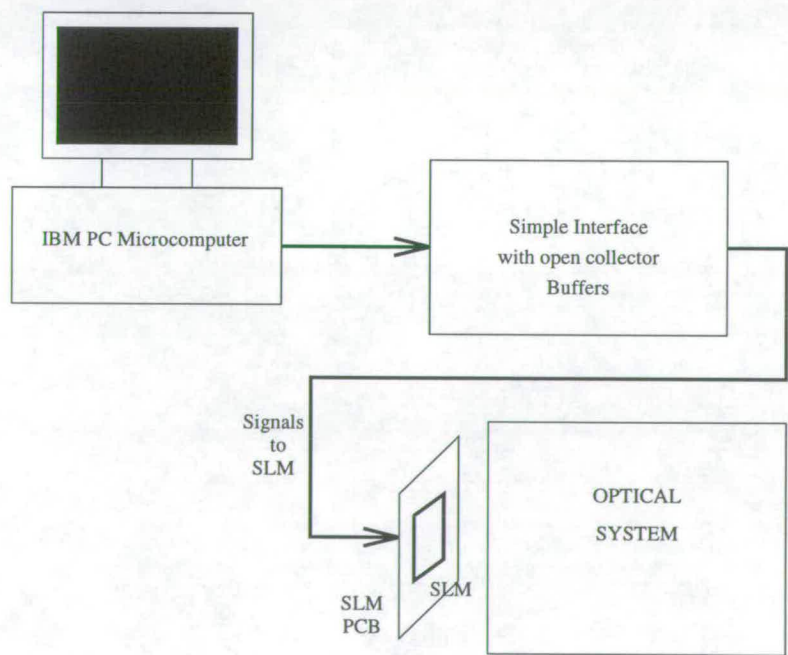
Figure 5.4: The 16^2 system.

5.3.2   Cell Construction on the 16^2 Backplane

A particular cell fabrication technique was experimentally chosen for the 16^2 device. The chip size is $10mm \times 10mm$ and the pixel area is $3.2mm \times 3.2mm$ so there are no tight constraints on the glass size or exact positioning required. Tally-step measurements on the circuit topology proved that the polysilicon/metal spacer structures designed around the array were the highest parts of the backplane at $1^+_-0.1\mu m$ above the pixel mirrors. This would allow the cover glass to be placed ontop of the chip without any need for added spacer layers. The first chips obtained were already packaged in chip carriers and bonded. This meant that care had to be taken not to damage the fine gold bonding wires around the edge of the chip. These features influenced greatly the cell construction proceedures used.

After bonding, the chips were observed to require cleaning, and the organic cleaning proceedure was used delicately with minimal use of the ultrasonic bath. The ITO coated optical flat glass (thickness 6mm) was used due to its ease in handling. An aluminium contact was evaporated around one side and over $0.5mm$ of the ITO front electrode defined by a metal mask. MAD alignment layers were deposited on both the front electrode and the chip backplane (section 3.3.2). Three fine dots of glue (no spacer balls) were written onto the backplane over three of the spacer areas and the glass block was positioned with the vacuum pen (section 3.1.6). Vacuum packing for the curing of the glue was found to damage the bonding wires, so a simple point contact was applied to the top of the cube as the glue was cured with UV light. The devices were then filled with SCE9 or SCE13 FLC as described in section (3.1.7).

5.3.3   Device Evaluation

After cell fabrication, on observation under polarising microscope, it was discovered that most of the devices had one or a few 'dead lines' of pixels or dead individual pixels. Only two devices were observed to have a fully working array of 16^2 pixels. Unfortunately, there were problems with the device cell thickness so although switching could be observed, the defects were such as to preclude completely satisfactory operation. Figure 5.5 shows one of the devices which has a flatter and more uniform cell thickness and had good liquid
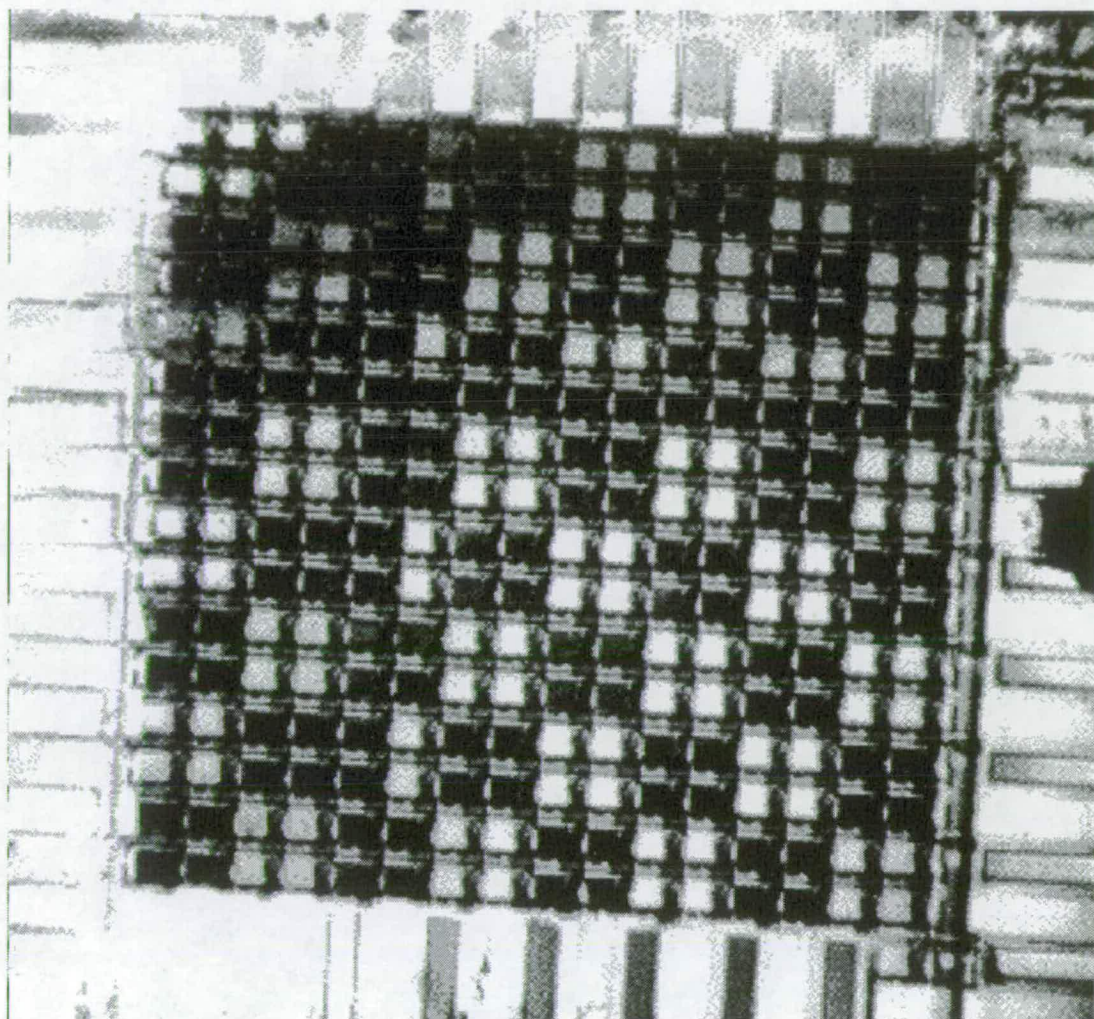
Figure 5.5: A 16^2 SLM displaying a checker pattern.

crystal alignment. Unfortunately, this device has two dead lines and only a useful area of 10×10 pixels. Device contrast was measured by imaging a portion of the SLM onto a photodetector and switching the pixels all **ON** and then all **OFF**. This was measured at $8^{+}_{-}1 : 1$. This value of contrast ratio includes the effects of the pixel circuitry around the mirror. Figure 5.6 shows a close up of an **ON** and an **OFF** pixel. The actual contrast on the mirror was much higher at $60^{+}_{-}5 : 1$. The switching speed was measured in a manner similar to the techniques described in section 3.5.6. The value obtained only refers to the rise-time from 10% to 90% in optical FLC switching. There was an additional time due to electrical delays. The risetime observed was $60^{+}_{-}10\mu S$. This is fast in comparison with typical test cell investigations. The reasons for the increase in speed are probably due
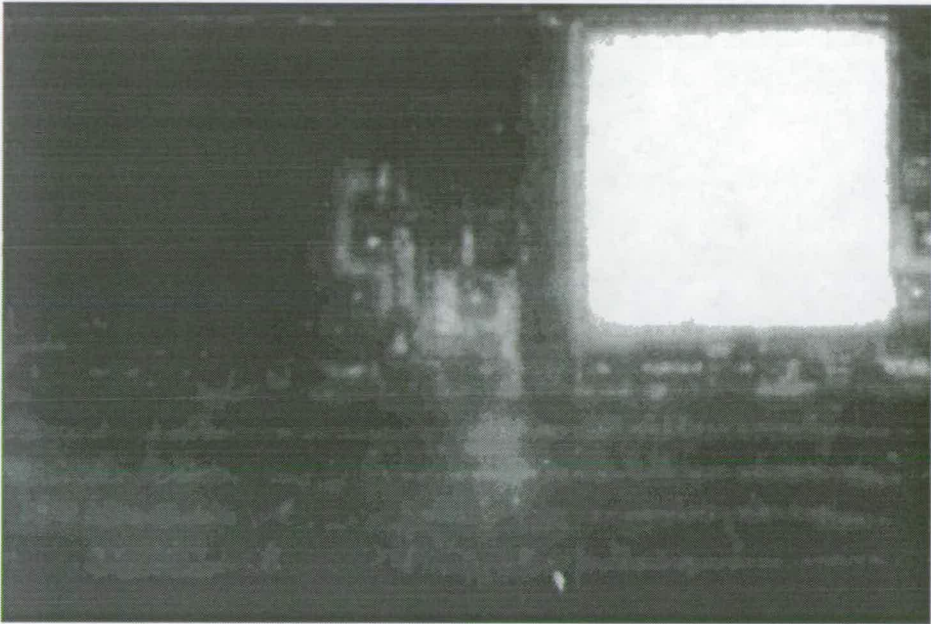
Figure 5.6: A pixel **ON** and a pixel **OFF** on the 16^2

to the thinner cell and hence higher electric field, and the slightly elevated temperature due to the power dissipation in the nMOS backplane. Optical throughput for the device was a maximum of $10^{+}_{-}2\%$, but $3^{+}_{-}0.5\%$ for maximum contrast (section 3.5.5).

The devices could not be made completely uniform and typical fringe patterns are sketched in figure 5.7. This resulted in polarisation colour variations of yellow to blue (i.e. approx. 1 to 2 μm variations at best). In some of the more extreme examples, this resulted in serious reduction and indeed reversal of contrast.

5.3.4 Structured Illumination

The problem of the low fill factor on FLC/VLSI backplanes can be addressed in a novel manner for certain system applications. Structured light can be employed to reflect only from the mirror areas and not the surrounding circuitry. This has been successfully implemented by Collings [115] using an SLM device fabricated by the author. A Dammann grating fan-out element was used to illuminate a 7×7 section of the SLM with 7×7 beamlets. This resulted in a contrast ratio of $\approx 100 : 1$, increased from $\approx 10 : 1$. This
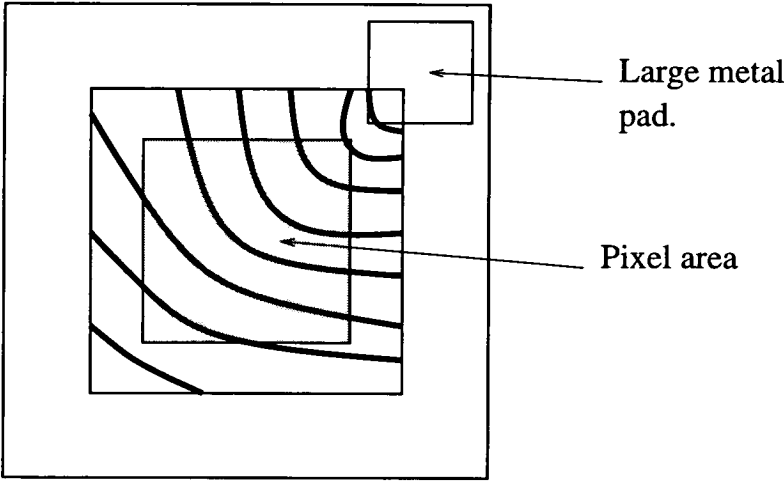
Figure 5.7: Typical fringe patterns on the 16^2

technique is particularly attractive for use with **smart** SLM devices which have modulator elements and detector elements adjacent to one another. Light beams can be targeted at either the modulators or detectors avoiding any interaction.

5.3.5 16^2 Device Discussion

The main device problem was the low yield on the electrical circuits. Only two fully working backplanes with all pixels operational were fabricated. Unfortunately, these devices had very poor liquid crystal alignment due to non-uniform cell thickness. No 16^2 SLM devices could be fabricated to produce as uniform a cell thickness as in a test cell. All seemed to have a considerable bow to a greater or less degree in the same direction (figure 5.7). The source of this bow was partly due to a curvature in the silicon, but also due to metal hillocks formed in the silicon fabrication process. This will be discussed in section 5.6.1. The final layer metal is **sintered** at high temperature causing stresses in the layers dependent on the size of the metal area. The 16^2 has a large metal contact pad at one corner of the device and as this has the largest metal area, produced the largest hillock structures. This caused the nonuniform cell thickness.

It is unfortunate that the electrical yield was so low with the 16^2 device. This resulted in a not too satisfactory investigation. However, as shall be seen in chapter 6, fabricated

devices did allow useful systems work. At present, the 16^2 device is being redesigned to allow commercial fabrication. This should result in a good supply of fully working back-planes for future research. The 16^2 device is a useful workhorse for device development.

5.4 176^2 SLM Device Construction and Evaluation

This section examines the construction and evaluation of the 176^2 SLM device. This device was designed through a JOERS research project HPSLM [116]. Originally it was fabricated using a $3\mu m$ CMOS process at the Edinburgh Microfabrication Facility (EMF), but is now fabricated at Austrian Micro Systems (AMS). It consists of an array of 176×176 DRAM memory cells, with full access shift register addressing circuitry around the pixel array. The pixel pitch is $30\mu m$, the array area is $5.28 \times 5.28mm$ and the mirror size is $22 \times 15.5\mu m$ i.e. fill-factor $\approx 30\%$.

5.4.1   Address times

Polysilicon gate access lines are a major impediment to fast operation due to their high RC time constant causing slow rise times. A pixel row is addressed in $1.6\mu s$, with the P_s of the LC chosen such that there is enough charge deposited on the modulator mirror to switch the LC. This limitation would be alleviated if additional metal access lines were incorporated into the design.

5.4.2   D.C. Balance

In order to avoid chemical degradation, the LC must not be exposed to a long term net d.c. voltage (section 2.3). To maintain this d.c. balance, after an image has been written to the SLM, the inverse data is then displayed. A frame is loaded, the liquid crystal is allowed to settle and then the image can be viewed. The image is blanked (SET) and then an inverse pattern is loaded and the front electrode signal is reversed, followed by a further blanking (RESET). This rather complex driving scheme retains d.c. balance

while allowing the full supply voltage to be applied to the LC for switching. To observe the pattern on the SLM, pulsed light must be synchronised with the positive frame. This makes testing of the device require a fully operational interface, imaging optics and pulsed light source.

5.4.3 Interface and Software

The electronic driving equipment for the device is shown in figure 5.8. A custom interface was designed by A.O.Al-Chalabi and G.Bradford. The interface is operated by an Archimedes 440 computer fitted with a 16-bit Input/Output Podule (Intelligent Interfaces) and an 8-bit User Port. The 16-bit Podule allows data transfer to and from the the computer and interface memories. The 8-bit User Port provides the control signals to the interface. The interface stores pattern data for 8 frames and presents them sequentially to the SLM as rapidly as possible. The data transferred to the interface from the computer can be returned to the computer for diagnostic purposes. The interface consists of memory address counter and static RAM memory. Output to the SLM device is performed through open-collector buffers to increase the voltage to $\sim 10V$ (8V used). 16-bit data words are presented to the SLM device column shift registers which are clocked along 11 times to the fill them (controlled by three clock signals). This data is stored on the appropriate pixel element by selection through a rolling logic '0' which is clocked down the row shift registers (controlled by two clock signals). Logic '1' values on the gates of all other rows isolates the non-addressed pixels so that any data previously written remains unchanged. The interface supplies column and row shift register SET and RESET signals, and the front electrode signal. A sync pulse for the strobed light source required for viewing is also available.

The software to control the interface and manipulate the picture data is written in ARM Assembly Programming language [117]. All control signals to the SLM can ultimately be varied by changing the software. This allows the frame rate, LC settling times, viewing time and any additional delays to be defined and optimised by the user. Much time was spent learning the assembly language and altering the software for suitable SLM driving parameters.
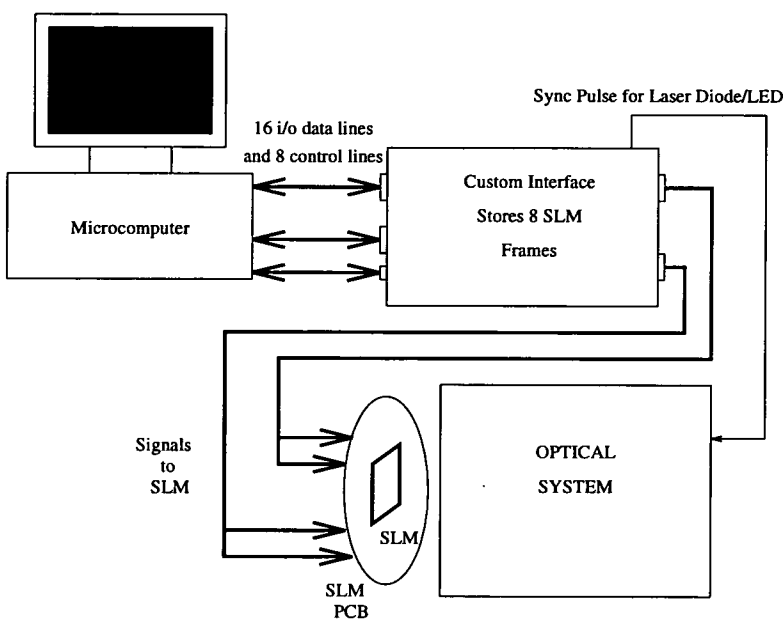
Figure 5.8: The 176^2 System

5.4.4 Cell Construction on the 176^2 Backplane

An alternative technique for constructing cells on this device was followed. From experience with the 16^2 device, it was believed that when the chip was glued into the chip package , serious bowing of the chip resulted due to thermal stresses. It was therefore decided to construct the FLC cell and fill the cell before gluing the chip into the chip package and bonding. To allow access of the bonding equipment to the chip bonding pads, thin glass had to be used. A compromise was reached in allowing enough of an overlap of the cover glass beyond the pixel array to allow successful gluing (i.e. no glue on the array) and in allowing the bonding equipment access to the bonding pads. Concern about the effects of hillocks suggested that instead of the $1\mu m$ thick FLC layer, a $3\mu m$ thick layer should be constructed. $1\mu m$ and $3\mu m$ thicknesses of SSFLC have similar light modulating properties (section 3.2). Differences include the lower electric field across the cell for a particular voltage and less surface energy transfer into the bulk (which has a larger volume) which would perhaps affect the LC alignment. The positioning of the cover glass on the 176^2 was much more crucial than for the 16^2 due to the

Hole to allow pressure
onto Cover Glass

Holes to allow UV curing of glue

SLM
Cover Glass

Dot of Glue
with spacer
balls

PTFE
SLM JIG

SLM
Backplane

Hole to allow chip to be removed
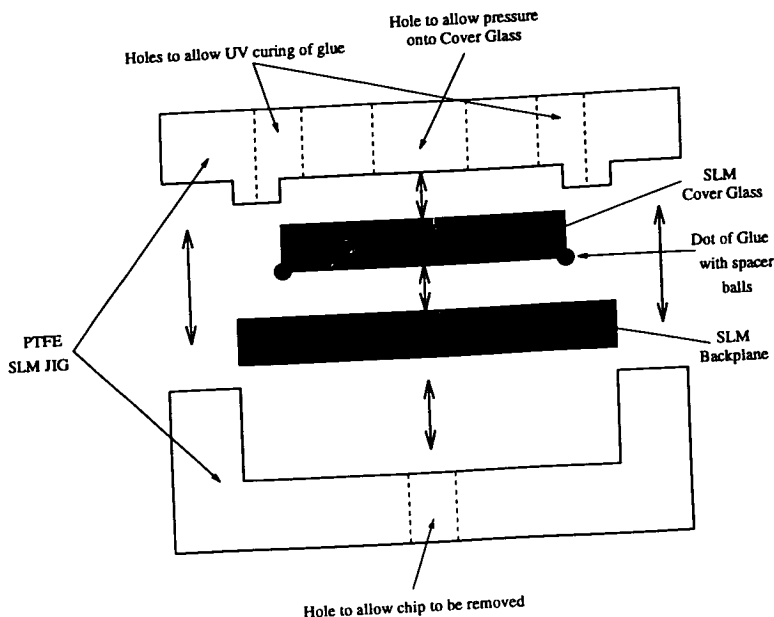
Figure 5.9: 176^2 device construction jigging.
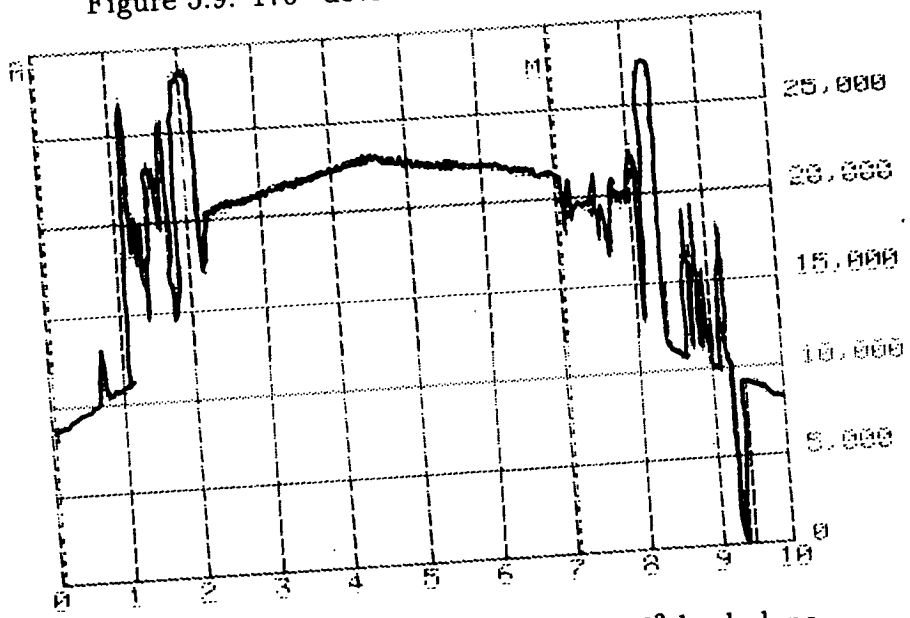
Figure 5.10: A surface profile across the 176^2 backplane.

smaller distance between the array and the bonding pads.

A positioning jig was designed for the 176^2 device construction. The jig consists of 2 Poly-tetra-floro-ethylene (PTFE) components (figure 5.9), machined in the Physics Dept. Mechanical Workshop. The lower component holds the 176^2 chip and the top component
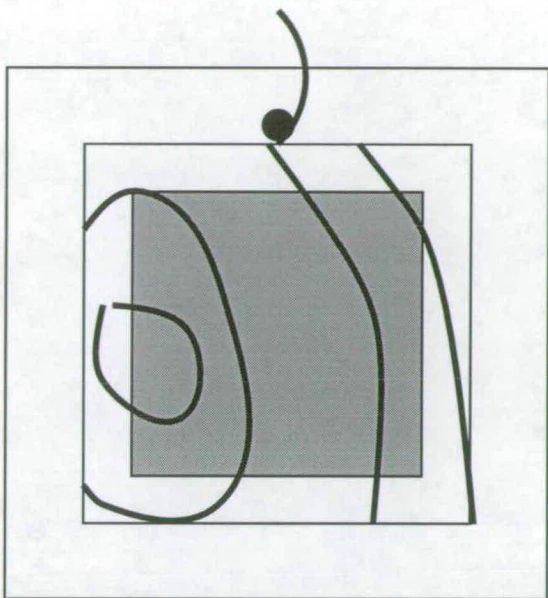
Figure 5.11: Typical fringe patterns on the 176^2.
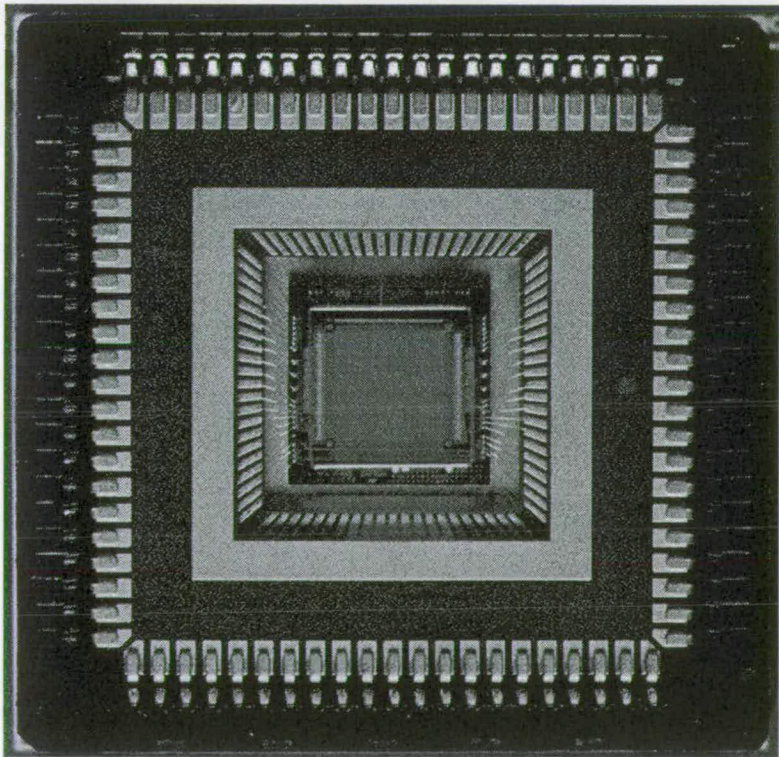
Figure 5.12: The constructed and packaged SLM.
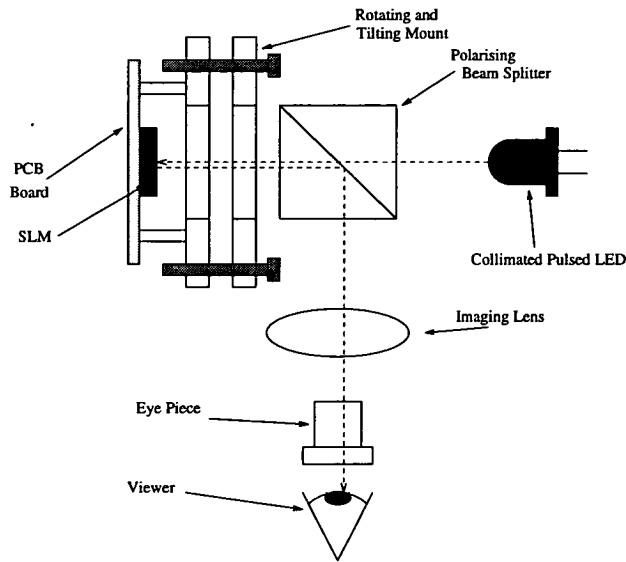
Figure 5.13: A noncoherent viewing system for the 176^2 SLM.

holds the cover glass. When the two components are carefully brought together, the cover glass is centrally located ontop of the chip. A hole in the top component allows a point pressure contact to be applied to the glass for uniform pressure while curing the glue. Four holes at the position of the corners of the glass allowed for UV curing of the glue dots (with $3\mu m$ spacer balls) applied to the corners of the cover glass.

Figure 5.10 shows a tally-step measurement across a 176^2 chip. This shows the circuitry features and a bow in the chip. When diced up, the chips seem to bow slightly, which results in a repeatable fringe pattern after fabrication. A typical fringe pattern observed is shown in figure 5.11. One or two fringes are reproducably obtained over the active area ($\approx 0.5 - 1\mu m$ variation). This is more uniform than the 16^2 device and this results in an almost uniform FLC polarisation colour of yellow. The fully packaged and bonded SLM is shown in figure 5.12, in a 84 d-type chip package (pga packages were also used).

5.4.5   Device Evaluation

For assessment of the fabricated devices, an optical system, incorporating a pulsable, high power LED was constructed in Spindlar and Hoyer optical components (figure 5.13). The
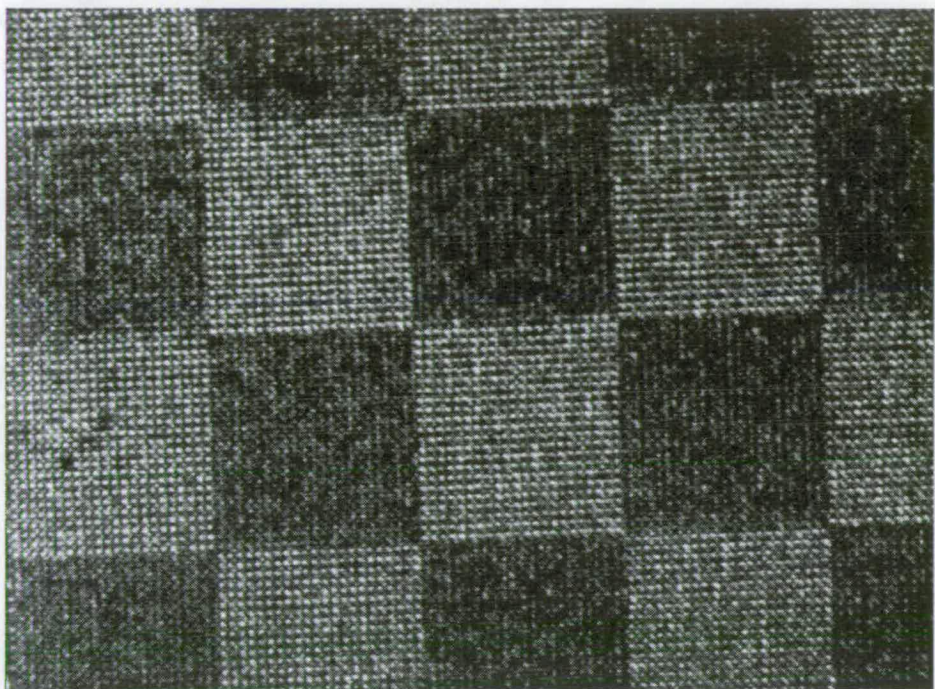
Figure 5.14: A checker pattern on the 176^2 SLM (unplanarised)

PCB board holding the SLM is attached to the optical bench via a rotating and tiltable mount, fabricated by the mechanical workshop. The pulsed LED illuminated the SLM through a polarising beam splitter to polarise the light. Reflected light passed back out through the polarising beam splitter, which acted like an analyser. The light was then imaged onto an eyepiece, a CCD camera or a photodetector (section 3.5.7). Contrast ratios were measured over the whole pixel array at $2^+_-0.5 : 1$ for low light levels, but this reduced to unmeasurable (in terms of errors) at high light levels. This reduction is due to charge leakage on the DRAM capacitor due to photo-induced effects. This will be discussed more in section 5.6.2. The FLC rise-time was measured at $120^+_-5\mu S$. Optical throughput was measured at $5^+_-1\%$, so the device has large losses.

Attempts were made to produce the bookshelf FLC structure, with high voltage a.c. fields on the front electrode, with the pixel elements held at $0V$ (section 3.5.7). This proved unsuccessful and the FLC was damaged. This will be discussed further in section 5.6.2. Figure 5.14 shows a checker pattern displayed on a fully working 176^2 device, with 8 volt power supply and a 500 Hz frame rate.

5.4.6 176^2 device discussion

The 176^2 SLM suffers from similar problems to the 16^2 SLM, except that it does not have the large metal pad in one corner. The 176^2 SLM has a DRAM structure and therefore has some of the drawbacks discussed in section 5.2.4. The fabrication constraints are much more limiting than for the 16^2 SLM, with more accurate positionings required. These have been overcome. The main points to be addressed involve the mirror quality, which reduces the FLC alignment and device efficiency. This will be discussed in section 5.6.

5.5 Miscellaneous SLM Devices

5.5.1 256^2 SLM

A 256 × 256 pixel SRAM EASLM designed by D.C.Burns became available very late in this study. This device has a similar pixel circuit to the 16^2 SLM. As the device is SRAM, switching of the FLC is more satisfactory, photo-induced charge leakage is less of a problem and interfacing is somewhat simpler. Data can be clocked onto this SLM at $25MHz$ so frame rates are potentially fast. The pixels are on a $40\mu m$ pitch and have a 24% fill factor. The pixel array is 10.24 × $10.24mm^2$ which is approximately four times the area of the 176^2 SLM.

Preliminary experiments give a contrast ratio of 10:1 over the pixel mirror, and an FLC switching rise-time of $100\mu s$, under coherent illumination. Figure 5.15 shows a close up of a pattern displayed on the 256^2 SLM. As a short experiment to show the advantage of SRAM devices over DRAM devices, with regard to photo-induced charge leakage, the 256^2 SLM was illuminated by a 250 Watt street light (for projection onto the wall). There was no obvious degradation to the image compared to illumination with a low power $5mW$ laser. More quantitative results are to be obtained. The SRAM-XOR pixels are robust under high read-beam intensities so do not need to be continually refreshed. Inclusion of the XOR gate, as in the 16^2 SLM, permits the FLC layer to be
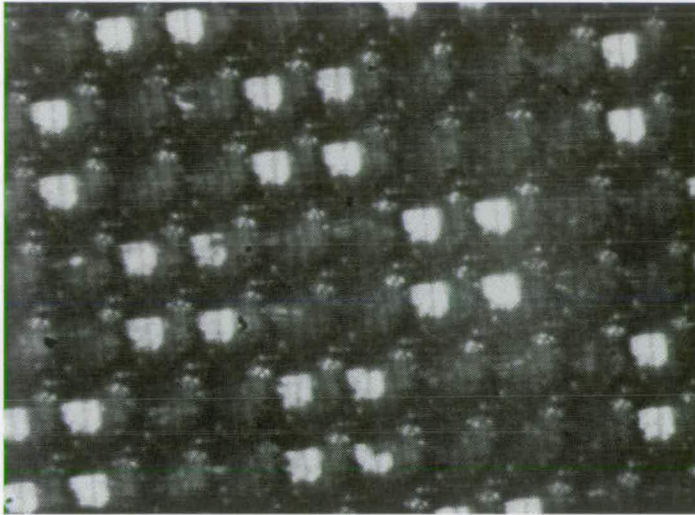
Figure 5.15: A close-up of the 256^2 SLM

charge balanced without the use of a pattern/inverse pattern drive scheme. The SLM is capable of running at a 5kHz fully d.c. balanced frame rate.

5.5.2   SASLM1 Smart SLM

The SASLM1 chip is a test device designed by M.W.G.Snook and fabricated on the SASLM [53] project.   The device consists of a number of circuits for examining the concept of the smart pixel (section 1.5.2). As well as a number of individual test pixels, three small arrays of pixels are present (two 8×8 neuron pixel arrays and an 8×4 cellular logic array). These were electrically investigated by L.B.Chua [118]. As a preliminary optical test, electrical and optical signals were used to switch the output mirrors on the smart pixels to drive a fabricated FLC modulator **ON** and **OFF**. This is shown in figures 5.16 and 5.17. The pixel contrast was measured at $\approx 5 : 1$ As can be seen, the mirrors are very small in comparison to the pixel dimensions. Structured illumination should be used in optically accessing these devices.
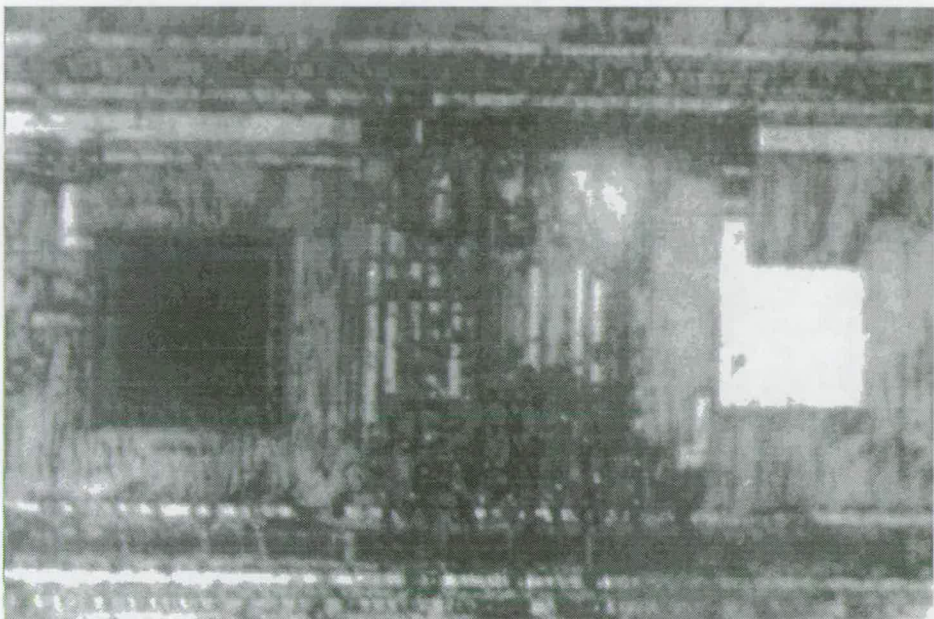
Figure 5.16: Smart pixel output **ON**
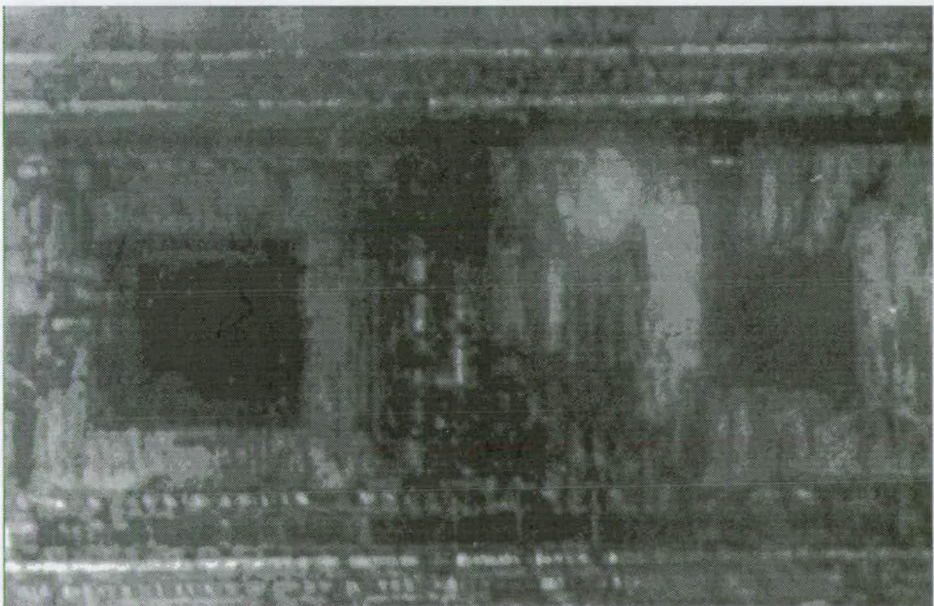
Figure 5.17: Smart pixel output **OFF**

5.6   Improvements in Device Morphology

The standard VLSI backplanes have a number of drawbacks when used for FLC SLM devices. Those concerned with the modulation mirrors are the most crucial. In general, VLSI processes take no consideration of the requirements of optical devices. Various post-processing steps must be applied to produce high quality SLMs. With regard to the modulation mirrors, there are a number of problems:

- **Low fill factors:** Due to the surrounding circuitry and addressing lines the flat area of the modulation mirror is limited in size. In both the 16^2 and in the 176^2 device it is $\approx 30\%$.

- **Poor mirror quality:** Following metal deposition, the Si wafers must be sintered to produce good ohmic contacts. The sintering operation involves the wafer being inserted into a high temperature furnace. During the heating and cooling phases of operation, stresses are induced in the films. To relieve the stresses the Al film distorts forming hillocks and depressions on the mirrors.

- **Device flatness:** Although the Si wafers are flat enough for photolithographic processes, they are not necessarily flat enough to give uniform FLC cell thickness or phase flatness (typically $1\mu m$ over 10 mm).

As the geometries of VLSI processes are reduced and multi-layer processes are introduced, these problems are currently being encountered in silicon manufacture. All of these problems are being addressed with specific regard to FLC/VLSI SLMs through the SCIOS program [119] at the University of Edinburgh by A.O'Hara. A number of different approaches were investigated. These culminated in a planarisation technique where layers of dielectric on the wafer were chemically-mechanically polished flat before a final layer of metal was deposited, hiding the addressing circuitry beneath. This will result in optically flat SLMs with high quality mirrors and high fill-factors.

5.6.1 Metal Protection

As a preliminary step, metal protection was employed to reduce the hillocks and depressions. A layer of dielectric acting as a restraining layer, is deposited to suppress hillock and depression formation during sintering. This proceedure allows high electrical performance in the Al contacts without reducing the optical quality of the mirrors. Improving the mirror quality on VLSI backplane SLMs improves the reflectivity of the device. But, perhaps more importantly, good mirror quality is crucial to enable highly aligned FLC structures. The alignment of FLC molecules is highly dependent on the bounding surface morphology (section 2.5). Irregular hillocks and depressions will locally alter the sensitive boundary conditions required of the SSFLC device structure. They will disturb the formation of parallel smectic planes, vary the surface molecular tilt angle and randomly induce all manner of defects from the device ideal. Ideally, the surface energy should be uniform across the bounding plates of the FLC device. If large enough, any perturbation from this uniformity will unduly affect the molecular alignment in the bulk FLC material. Therefore, mirror quality will directly determine the defect structure and may undermine any post-filling FLC cell treatment techniques. It is unlikely that such treatment can compensate for large fluctuations in the surface energy caused by poor mirror quality.

For FLC devices, improvements to the mirror quality would seem to be most important. Such improvements are a major route towards increases in contrast ratio, device uniformity and modulation efficiency as well as the reflectivity. Defect free FLC structures should be obtainable when high quality mirrors can be constructed on VLSI silicon backplane SLM devices. This improvement is demonstrated by a comparison of FLC devices fabricated on a unprotected metal standard VLSI process and those fabricated on a protected metal process. The protected metal process results in a reduction of hillock and depression formation although some of these undesirable features can still be observed.

To examine this, SSFLC cells were constructed on two SLM devices from the same VLSI process (supplied by A.O'Hara). The SLM backplane used was the 16^2 test-bed device. The wafers were processed at the Edinburgh Microfabrication Facility (EMF), so allowing the post-processing metal protection proceedure performed by A.O'Hara. One device originated from a wafer which used the standard, unprotected metal process. The other,
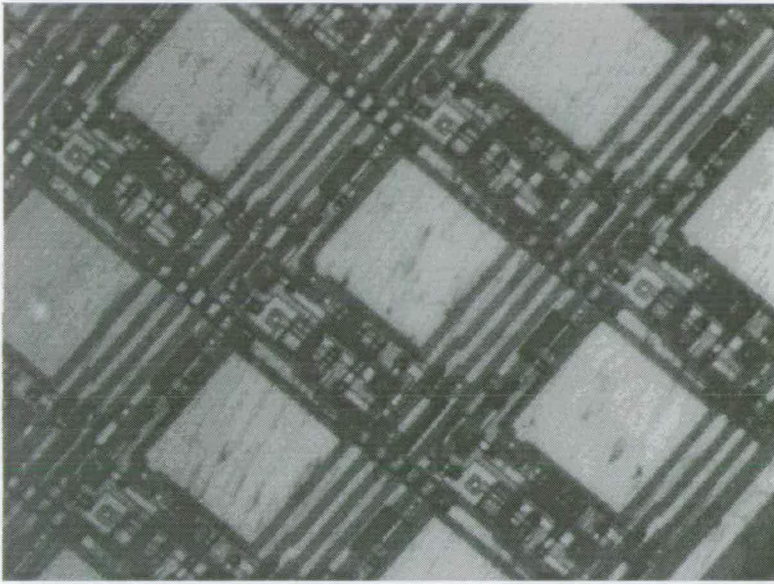
Figure 5.18: Non metal protected mirrors

from a wafer fabricated with an extra metal protection processing step. Both protected metal and unprotected metal devices were constructed under the same conditions as in section 5.3.2. Therefore, these devices allowed comparisons to be made to show any improvement to the FLC characteristics. Figure 5.18 shows the unprotected metal device illuminated with polarised light and observed through crossed polarisers. Figure 5.19 shows the protected metal. On observation of the unprotected metal device one can observe a lower reflectivity and apparently no defect structure. There are defects however, but they are so numerous and fine due to the poor metal quality that it appears uniform. This is not a desirable feature as they will still adversely affect performance and be difficult to remove. In the metal protected sample, defects are large and clearly visible. This is actually encouraging as such distinct defects are observed in plain FLC test cells in section 3.4. Therefore the alignment of the FLC in the metal protected device is clearly approaching the quality of that attainable in high quality surface test cells. The optical throughput of the device has increased from 10% to 15%. The high performance of FLC structures observable in test cells should be more obtainable by improved metal quality VLSI backplane SLMs.
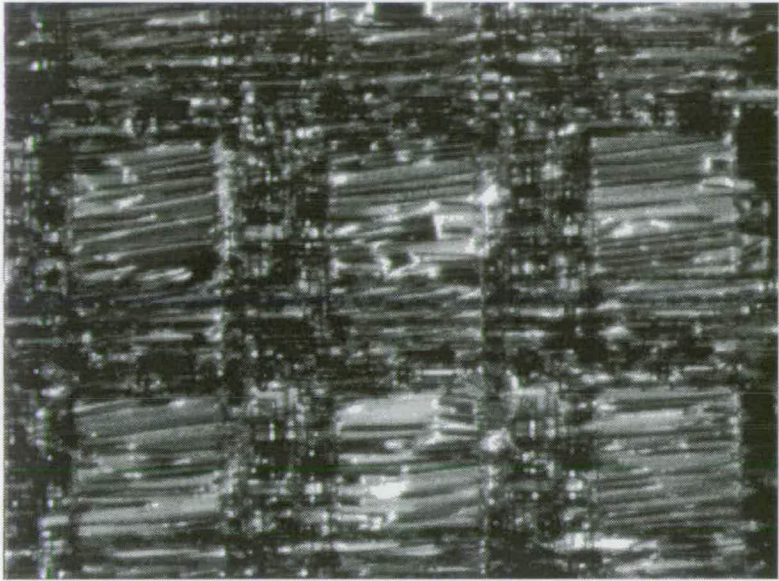
Figure 5.19: Metal protected mirrors (device rotated 45° compared to figure 5.18 to fully show the defects)

5.6.2 Cell Uniformity Problems

Uniformity of the SSFLC cell thickness is also an important parameter concerning good alignment of the FLC molecules. For example, if a cell is constructed as a wedge then different energies will be transferred to the bulk of the FLC material so imposing differing conditions on the structure. If configured as a switchable half-wave plate, variations in material depth will also alter the tuned wavelength for modulation (section 2.7). Optical flats are used for the SLM device cover glass and therefore are negligibly deformed. Deformation of the VLSI silicon wafer has been noted (section 5.4). This deformation has not been so large as to affect the lithographic processes involved in the processing, but has been shown to influence FLC alignment and wavelength tuning for half-wave plate modulators. Figure 5.1 showed typical variation across a device of approximately $0.5 \mu m$. This will unduly influence device performance. Two solutions are currently being investigated to reduce this problem. The first is mechanically constraining the tendancy for deformation at the cell fabrication stage. It is unknown if the stresses generated in such a process will cause mechanical instabilities over a period of time. Such constraining techniques are currently applied during the polishing stage of post-processing, but the chip reverts to its original deformation after this is completed. A much simpler approach

may be to use thicker silicon wafers in the VLSI process. Thicker wafers should have much less tendancy to be deformed and should be more mechanically stable at elevated temperatures.

5.6.3 Planarisation

A more satisfactory technique for improving SLMs is planarisation. A chemical-mechanical polishing post-process was developed by A.O'Hara [120]. The technique is described in appendix C. The resulting planarisation for a 176^2 wafer is shown in figure 5.20. The fill factor has been increased to $\approx 80\%$ and the surface variations were found to be $< 10nm$ r.m.s. (A.O'Hara).

To assess the improvement to device performance attainable through planarisation, planarised and non-planarised 176^2 SLMs were compared. The devices were constructed under the same experimental conditions. A planarised and a non-planarised device were fabricated with a similar FLC structure as described in section 5.4.4. These devices were then evaluated to investigate device parameters. Examination of the FLC alignment quality and domains under a polarising microscope show that the planarised device allows much better alignment with much larger domains. Figures 5.21, 5.22, 5.23 and 5.24 compare the unplanarised device and the planarised device, orientated for an **ON** and an **OFF** state. The defects are more characteristic of high quality FLC test cells before treatment. The FLC is in the characteristic chevron structure which exhibits different coloured domains and zig-zag defects. This results in low contrast and non-bistable switching. [FLC devices can be treated with a combination of high a.c. electric fields and slow cooling to remove the chevron defect and achieve the ideal bookshelf structure.] Both devices were examined to assess the optical losses. The devices were illuminated with a HeNe laser ($\lambda = 633nm$), rotated between crossed polarisers and optical throughput and extinction measured. The maximum throughput for the non-planaried device was $5^+_-0.5\%$ and for the planarised device $30^+_-3\%$. The losses in the non-planarised device are much more limiting for optical systems. Although the planarised device has a much improved optical efficiency, the FLC defects still apparent in the device cause optical losses.
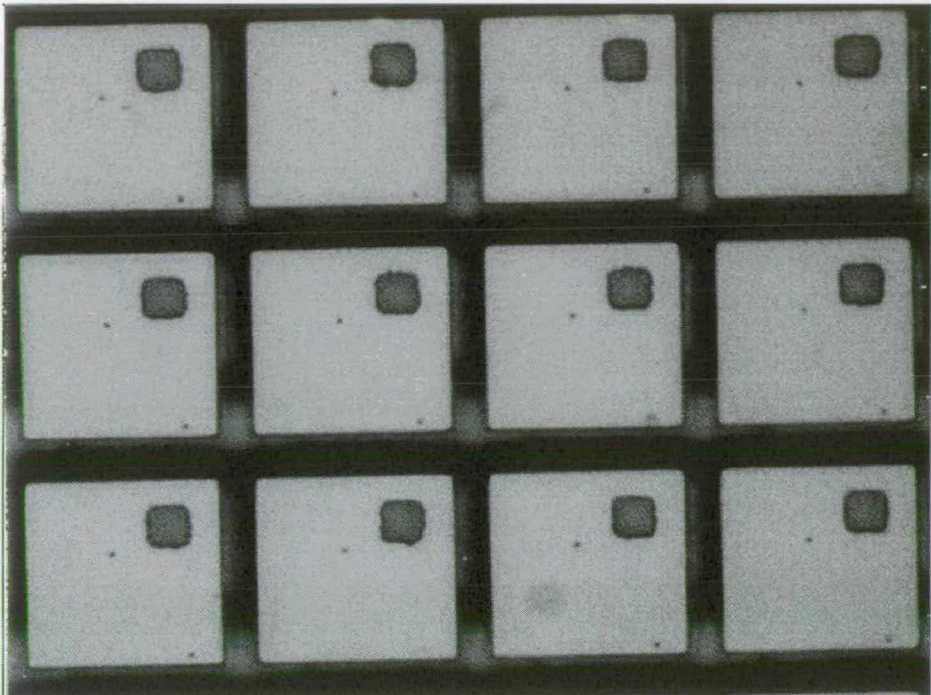
Figure 5.20: Planarised mirrors on the bare 176^2 backplane
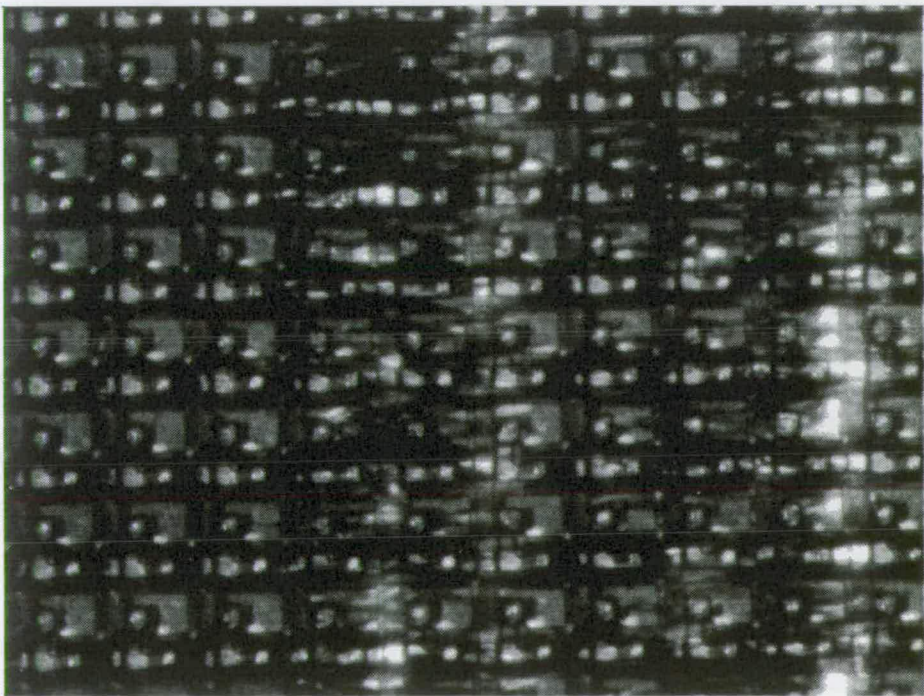
Figure 5.21: Liquid crystal on nonplanarised device **OFF**
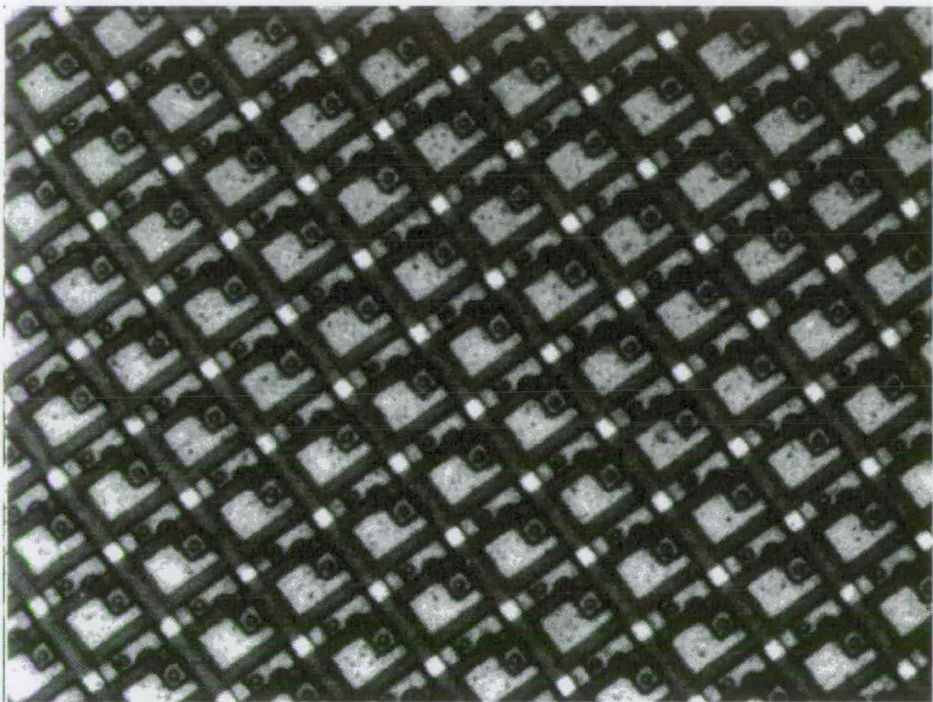
Figure 5.22: Liquid crystal on nonplanarised device **ON**
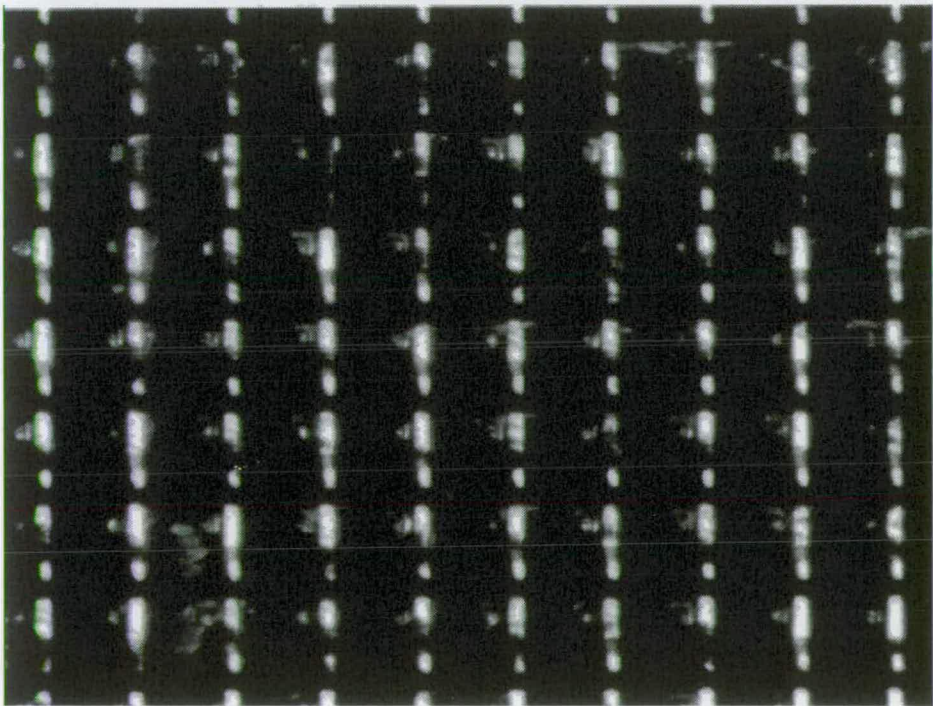
Figure 5.23: Liquid crystal on planarised device **OFF**
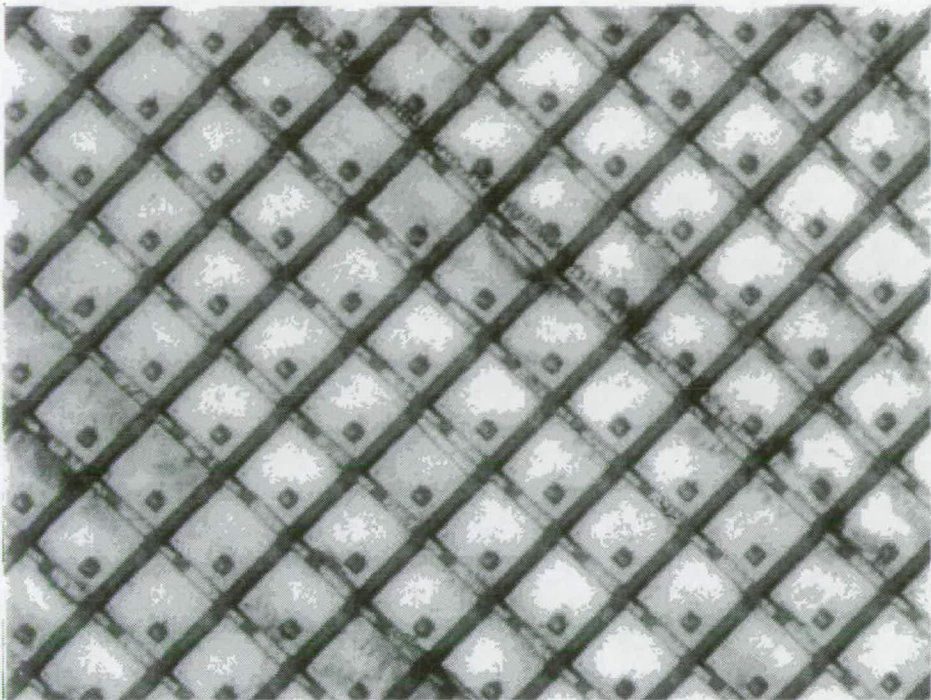
Figure 5.24: Liquid crystal on planarised device **ON**

The devices were shown to work, so the planarisation post-processing proceedure does not appear to cause electrical damage. Figure 5.25 shows a test pattern displayed on a planarised SLM backplane. The main immediate improvements expected were an increase in optical throughput, an increase in contrast ratio, improvements to the FLC alignment, less effect from photo-induced charge leakage and improved diffraction efficiency when used as a diffraction grating or hologram.

The contrast of the planarised device (before any post-filling treatment) is $10^{+}_{-}2 : 1$. The FLC is still in the chevron structure. This contrast ratio is similar to the contrast on the nonplanar device mirrors, but is applicable over a much larger area (figure 5.26). The circuit structure and low fill-factor in the non-planarised device reduced its *effective* contrast ratio down to less than 2 : 1, effectively uniform across the device. It is expected, that with electrical treatment voltages the chevron structure will be removed to obtain a tilted-quasi-bookshelf structure with its characteristic $\approx 100 : 1$ contrast ratio. So far this has not been attempted due to the risk of damage to the limited number of devices available for experimentation.
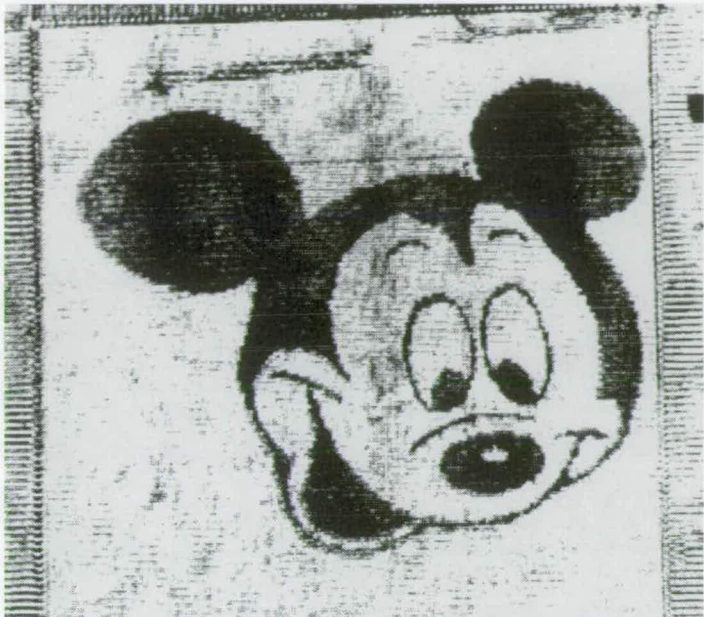
Figure 5.25: A coherently illuminated image displayed on the planarised 176^2
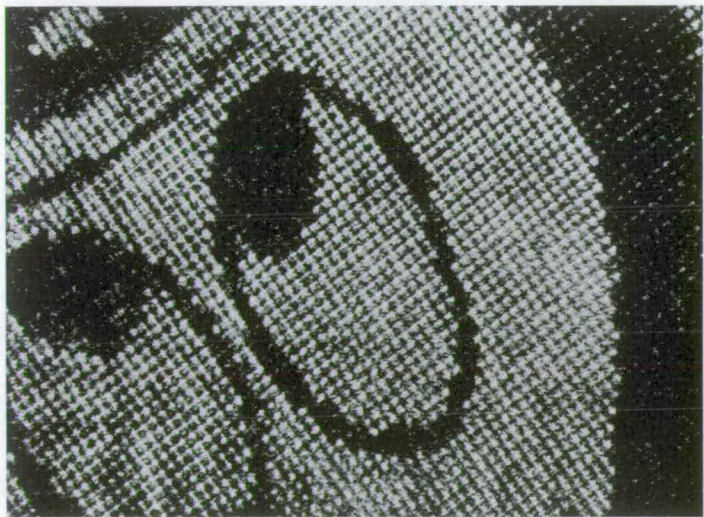
Figure 5.26: A closer view of the planarised pixels

	Test cell	16^2 SLM	176^2 SLM	256^2 SLM
No. of pixels	1	256	30976	65536
Pixel pitch	/	$200\mu m$	$30\mu m$	$40\mu m$
Pixel type	passive	SRAM	DRAM	SRAM
Process	none	$6\mu m$ nMOS	$3\mu m$ CMOS	$1.2\mu m$ CMOS
Active area	$\approx 6 \times 6mm^2$	$3 \times 3mm^2$	$5.5 \times 5.5mm^2$	$10 \times 10mm^2$
Drive voltage	typ. 10V	max. 13V	max. 8V	max. 5.5V
Frame rate	/	> 10 KHz	1KHz	5KHz
Cell thickness	$1.7\mu m/3\mu m$	$1\mu m$	$3\mu m$	$3\mu m$
Bistable	yes	yes?	no	no
Switching speed	$80\mu S$	$60\mu S$	$120\mu S$	$100\mu S$
Contrast ratio[1]	10:1[2]/100:1[3]	8:1	2:1/10:1[4]	2:1
Throughput	30%/70%	10%/15%[5]	5%/30%[6]	7%
Uniformity	$\approx 0.25\mu m$	$0.5\mu m$	$0.5\mu m$	$1\mu m$
Fab yield	70%	10%	30%	20%

Table 5.1: Table of SLM performance

[1]Over whole pixel.

[2]Chevron.

[3]Bookshelf.

[4]Planarised.

[5]Metal protected.

[6]Planarised.

5.7 Device Comparisons

Table 5.1 compares the various SLM devices and test cells. The most useful comparisons are between each device and the test cell parameters.

5.8 Discussion

In this chapter we have demonstrated how the SSLFC device investigations in chapters 3 and 4, have allowed the fabrication and appraisal of working VLSI backplane SLMs. The performance of the SLMs falls short of that obtained with the FLC test cells. This is mainly due to the properties of the VLSI chips, which are not optimised for optical use. The fabrication of FLC structures has allowed investigation into techniques for improving the optical characteristics of the backplanes which are necessary for useful devices. This is arguably the most crucial aspect of this study. Also, devices have been made available for use in the system demonstrators to be investigated in the following chapters. The main points of this chapter have been:

- FLC fabrication techniques were developed further to allow SLMs to be constructed.

- 16^2 SRAM and 176^2 DRAM devices were successfully constructed and shown to operate electrically and optically.

- The mirror quality was identified as a considerable problem for SLMs.

- Evaluation of post-processing techniques showed that planarisation allowed tremendous improvement.

- The device performance is currently at the level of FLC test cells in the chevron defect structure.

- Post-filling treatment should be performed when enough devices become available.

Chapter 6

Incoherent Illumination System Application

'It is clear that no significant discovery or inventing can take place without the will of finding.', J.Hadamard, 1945.

To assess the performance of the SLMs we have developed in system applications, some novel optical systems have been developed. A matrix transform system can allow the usefullness of the SLMs to be gauged in non-coherent illumination optical processing systems. Non-coherent processing systems have been relatively neglected since the development of high-power coherent laser sources. One might consider the non-coherent system as quite limiting compared to the coherent system. The coherent processor is a powerful system as it allows the manipulation of amplitude (and hence phase) of light. Non-coherent processor can only manipulate light intensity [121]. For non-coherent processors, the SLM performs the function of an adaptive mask, where each modulating element either allows light intensity to pass or not. Thus, simple two-dimensional matrix algebra operations can be performed, as light passing through two cascaded masks can be viewed as multiplication and imaging of two arrays superimposed on one another can be viewed as summation (intensities always add). Incoherent systems are less prone to noise, as optical path redundancy is inherent [121]. The systems can have less critical alignment, be more robust, and use lower quality (i.e. cost) components.

6.1 Matrix Transforms

Matrix transforms form a class of useful image representations for various procedures in image processing [122]. An input scene may be decomposed onto a basis formed by the elements of the matrix transform and thus be represented by a series of coefficients. Useful manipulations of the coefficient representation may then be performed and the resulting, processed, output image reconstructed.

Transformation of real world scenes requires optical-to-electronic data conversion followed by computationally intensive two-dimensional matrix handling, if the processing is to be carried out in an all electronic architecture. Optical systems utilising SLMs have been shown to be very useful in performing simple matrix algebra operations [18]. A logical progression is to use similar SLM optical systems to perform image transform calculations with optical multiplication and summation in real-time.

The binary nature of light modulation in the developed SLMs is suitable for the display of the binary Hadamard transform basis functions, which multiply input images optically. The high frame rate of the SLMs allow very fast calculation of the Hadamard transform coefficients. Each coefficient is obtained from the optical summation of the result of the multiplication of the input image and a transform basis function (displayed on the SLM). The resolution of the image processed is equivalent to the number of SLM pixels. Such an optical SLM system may have significant speed advantages over conventional optical-to-electronic information conversion and processing system. The high speed optical decomposition of the input scene to its Hadamard coefficient representation allows the manipulation and processing of the image information which may then be presented to electronic systems in a serial, high-dynamic range and high signal-to-noise ratio format. Where the system output is required to be an optical signal for transmission, image processing and compression may be performed in an all optical architecture.

Appendix D develops some image processing and compression algorithms using the Hadamard transform decomposition. Optical Hadamard transform processing shows the potential for implementing the processing algorithms presented in real-time optical SLM systems.

6.2   Image Representation in Orthogonal Basis

Most analysis models for image processing systems assume linear operation. As these linear assumptions are well known they will not be described here [122]. Image processing can be regarded as an analysis using large scale matrix manipulations. This will be discussed specifically with regard to vector outer products. The Fourier transform is a well-known example of a matrix image transform. It decomposes images in terms of complex exponentials as basis functions. Instead of complex exponentials one may represent an image with cosines, square waves or wavelets. In what follows we assume that an image matrix [G] has dimensions $N \times N$ (square matrix for simplicity). A general separable linear transformation of an image matrix [G] may be written in the form:

$$[a] = [U]^t[G][V] \tag{6.10}$$

where [a] is termed the unitary transform domain of the image, [U] and [V] are unitary operators, and the superscript t denotes the matrix transpose. Due to the unitary nature of [U] and [V], the inverse transform may be written in the form:

$$[G] = [U][a][V]^t \tag{6.11}$$

The matrix [G] can be represented in another way as

$$[G] = \sum_{i=1}^{N} \sum_{j=1}^{N} a_{ij} \mathbf{u_i v_j^t} \tag{6.12}$$

where u and v are the vectors made up from the columns of [U] and [V] respectively and a_{ij} is the value at the ith row and j^{th} column of [a]. A sum over all the combinations of outer products, weighed appropriately by the a_{ij} regenerates the original image [G]. Thus the image [G] is decomposed into a sum of N^2 matrices each weighed by the appropriate coefficient a_{ij}. The set of outer products form bases images, which can be used to generate for example Fourier, Walsh, Haar, Hadamard, Karhunen-Loéve and even identity expansions, and to reconstruct the original image [G] from these expansions. The specific transforms are represented by different matrices [U] and [V]. The set of orthogonal bases functions can be selected to match the particular hardware characteristics and implementation.

6.3   The Hadamard Transform

The Hadamard transform has been of particular importance in electronic implementa-
tions due to the relative simplicity of the computations required to calculate it [123, 124].
The Hadamard matrix which is used for [U] and [V], is composed of -1's or +1's. There-
fore only the arithmetic operations of addition and subtraction are required to perform
the Hadamard transform and no multiplication is necessary. The consequence of this, in
an optical transform system, is that the basis functions obtained from the outer product
expansions of [U] and [V] (both of which are the Hadamard matrix) have bipolar binary
values. A Hadamard matrix $[H_{N,N}]$ is a symmetric $N \times N$ matrix whose elements are
the real numbers +1 and -1. The rows and columns of a Hadamard matrix are mutually
orthogonal. The Hadamard matrix of order 2 is:

$$\begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$$

To recursively obtain high orders of the Hadamard matrix one would substitute the
$[H_{N,N}]$ matrix into the following relationship for $[H_{2N,2N}]$:

$$[H_{2N,2N}] = \begin{bmatrix} [H_{N,N}] & [H_{N,N}] \\ [H_{N,N}] & -[H_{N,N}] \end{bmatrix}$$

This is known as the Kronecker product [125]. The order of the Hadamard matrix
need not be a power of two, but the Hadamard matrices generated by this method are
sufficient for our purposes. Figure 6.1 shows a Hadamard matrix of order 8. The figure
also demonstrates **sequency** in one dimension. The outer product expansion of the rows
of this matrix generates the set of the binary basis functions.

The 64 binary basis functions for the matrix of order 8 are shown in figure 6.2. The
figure shows the frequency or **sequency** nature of the Hadamard transform. The d.c.
term is at the top right and functions of increasing **sequency** are found moving left
and down in the figure. This representation of images can be a highly desirable format.
Applications possible with such representations include image compression, frequency
filtering, pattern recognition and novelty detection (appendix D).

The Hadamard transform does not have the shift invariance property on transformation

```
1 1 1 1 1 1 1 1
1 1 1 1 - - - -
1 1 - - - - 1 1
1 1 - - 1 1 - -
1 - - 1 1 - - 1
1 - - 1 - 1 1 -
1 - 1 - - 1 - 1
1 - 1 - 1 - 1 -
```
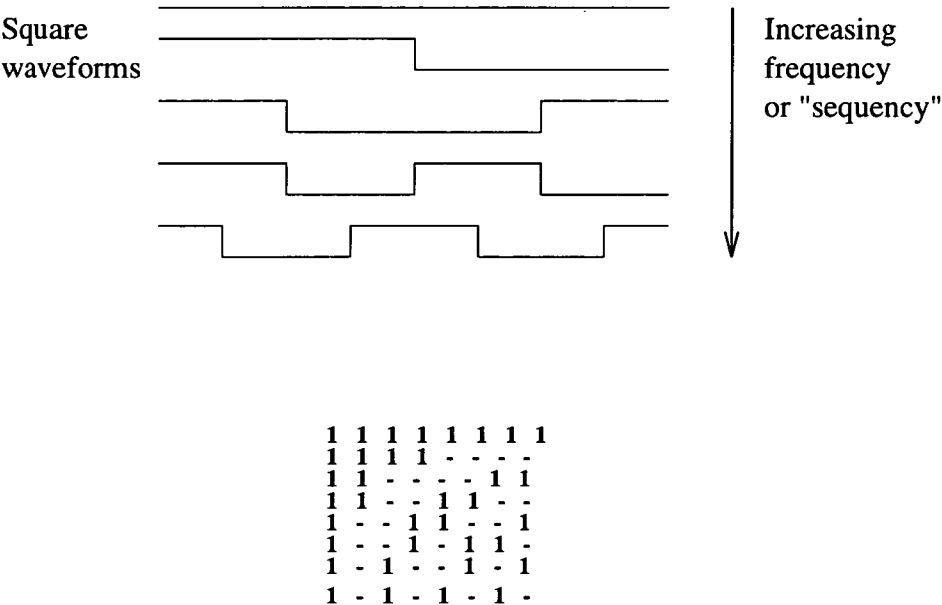
Figure 6.1: The 'sequency' of the Hadamard transform and the Hadamard matrix of order 8.
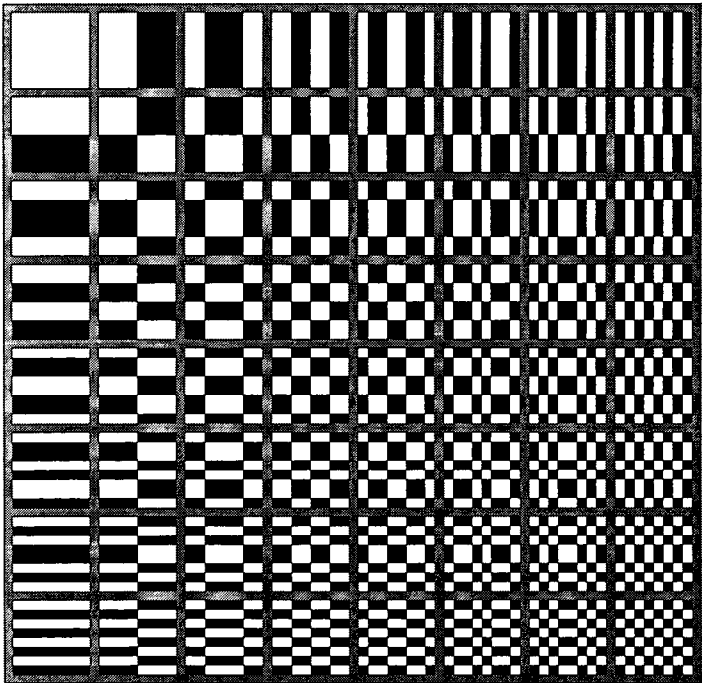
Figure 6.2: The complete set of basis functions for an 8 × 8 Hadamard transform.

which the Fourier transform possesses. Therefore, matched spatial filtering and corre-
lation are not possible in the conventional sense. It is important to emphasis at this
point that optical systems performing the Fourier transform use the Fraunhofer diffrac-
tion property of a lens to perform the transform. Unfortunately such a system requires
coherent light illumination and the phase of the transform would be lost on capture by a
CCD camera. Noncoherently illuminated systems offer much higher noise immunity due
to their inherent redundancy [121]. An optical implementation of the Hadamard trans-
form will use the multiplication of light from an image with a basis function mask and
then optical summation to obtain a single transform coefficient, given by the intensity.
This is essentially a time-multiplexed matrix-matrix transform configuration.

6.4   The Optical Implementation

Optical systems have previously been designed around the two-dimensional Hadamard
transform, but as far as the author is aware, have been limited to using mechanical
moving masks and sliding slits to generate the basis functions [126]. High performance
electronically addressed SLMs are ideal devices to display the individual basis images
required for direct transformation and inverse transformation through optical multipli-
cation and summation [127, 128]. A particular transform coefficient may be determined
by pixel-wise multiplication of the l, k^{th} input image element of matrix $[G]$ with the
corresponding l, k^{th} binary element of the outer product expansion matrix $(u_i v_j^t)$, as dis-
played on an SLM pixel. Summation over the two-dimensional array is then performed
by a lens which gathers the non-coherent light to a single photodetector with a high
dynamic range to determine the value of the coefficient a_{ij}. An analogue input scene
may therefore be decomposed into a series of transform coefficients which are obtained
by repeated optical multiplication with binary basis patterns displayed sequentially on
the SLM and by summation of the optical signal at the photo-detector. An advantage of
this frequency representation technique is the acceptance of an input image directly from
a scene illuminated by incoherent light. Figure 6.2 showed the set of 64 basis images
for an 8 × 8 implementation of the Hadamard transform. The individual patterns are
displayed sequentially on the SLM. An example of an 8 × 8 Hadamard transform basis
function for the coefficient a_{77}, displayed on an SLM, is shown in figures 6.3. This is a
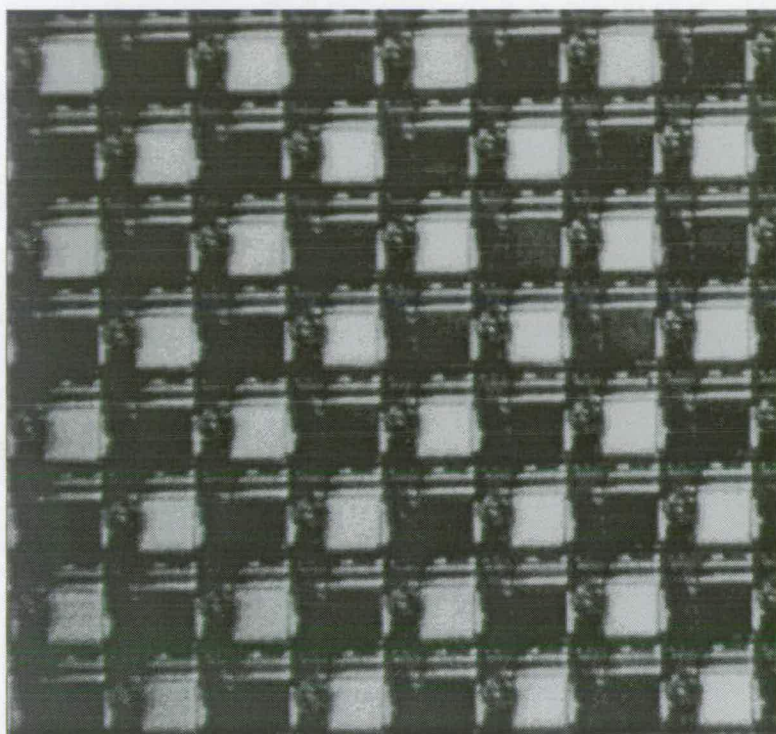
Figure 6.3: A Hadamard transform basis function

16^2 SLM device developed in section 5.3.

The Hadamard transform requires bipolar arithmetic as the basis functions are coded with +1(white) and -1(black) weights. Incoherently illuminated optical systems deal only with positive valued parameters. One way of overcoming this mismatch and retaining good signal-to-noise ratio is by implementing a two channel system: firstly calculating the positive contribution and then subtracting electronically the the negative contribution, for each basis function in turn. This time-multiplexed implementation of the transform is sensitive to uniformity variations across the device, but inherently insensitive to the mean device contrast, as the background is subtracted out at the detector. Positive-only versions of Hadamard bases images (called S-matrices) are available [122] and would be useful for all optical decomposition and reconstruction, but at the cost of a reduced signal-to-noise ratio. A polarisation encoding of the bipolar arithmetic would certainly seem an interesting alternative approach for a system implementation.

The compact optical system for implementation of the Hadamard transform is shown in
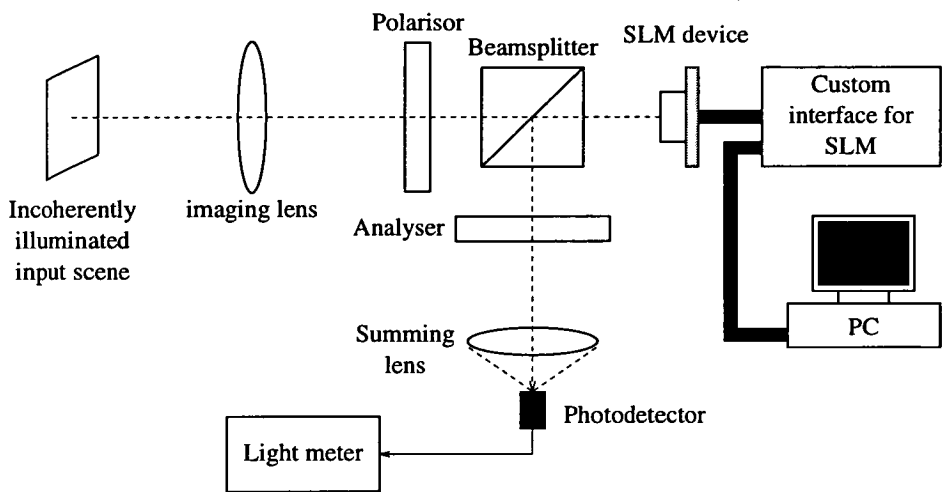
Figure 6.4: The optical system for Hadamard transform implementation

figure 6.4. An 8×8 test pattern (size $1.5mm \times 1.5mm$), shown in figure 6.5, was imaged onto an 8×8 section of the SLM device with an f=80mm lens (magnification $= 1$). The 64 positive and 64 negative basis functions for an 8×8 Hadamard transform were individually displayed on the SLM. The light reflected from the SLM (figure 6.6) was summed, via a lens (f=80mm), onto a photodetector, where the signal from the negative elements of the basis function was subtracted from the signal from the positive elements of the basis function to measure the value for the Hadamard transform coefficient. The resultant set of Hadamard transform coefficients measured in this way for the input test pattern is given in table 6.1 and shown in figure 6.7. As can be seen in the figure and from the table, the d.c. component has the largest value as expected because this technique analyses only input image intensity. This set of 64 coefficient values was input to a computer and an inverse transformation performed by digital computation. The reconstructed image is shown in figure 6.8.

The experimental measurement error on the coefficients was about ten percent in this simple system due to large instabilities in the light source. The effects of this error can be observed as noise in the reconstruction. If this data was thresholded the original input image would be accurately represented. Steps to improve the accuracy include reducing the insertion losses in the SLM, increasing the sensitivity of the detector as well as improving the stability of the incoherent illumination source or at least compensating for the variations [129]. An improved system may be a useful technique for generating

38	1.0	-4.0	-0.2	-3.8	0.1	-9.0	0.1
3.9	0.1	8.1	-0.2	0.5	0.2	-4.2	0.1
4.0	0.0	7.8	0.1	8.1	0.2	3.9	0.0
0.1	0.1	4.0	0.0	-4.1	-0.2	7.9	-0.1
3.8	-0.1	8.1	-0.2	-7.9	0.0	4.3	0.0
-8.8	0.0	-3.9	0.1	4.0	-0.2	0.0	0.0
0.2	0.2	4.0	0.2	4.0	0.1	0.1	-0.2
-11.7	0.3	8.2	-0.1	0.0	0.2	-3.7	0.0

Table 6.1: The measured Hadamard transform coefficients (10% error)
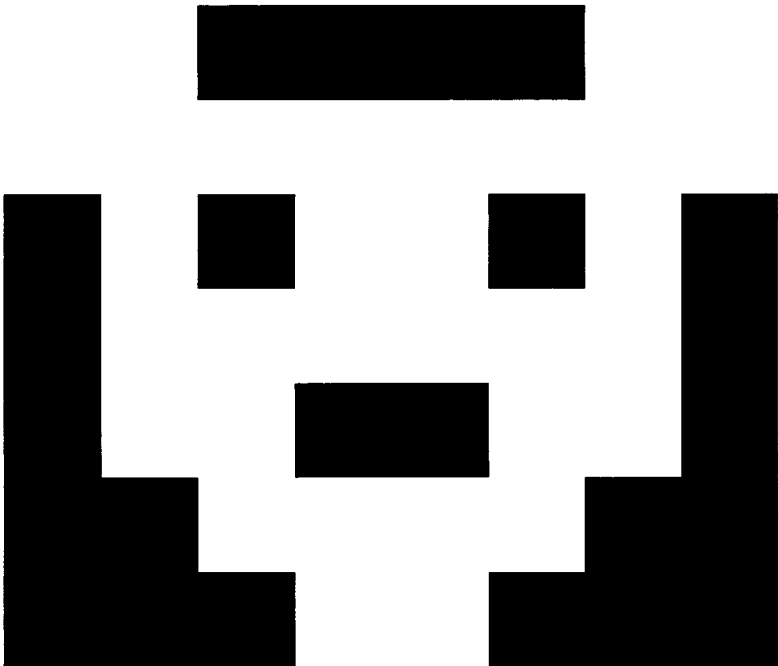
Figure 6.5: The input 8 × 8 test pattern.
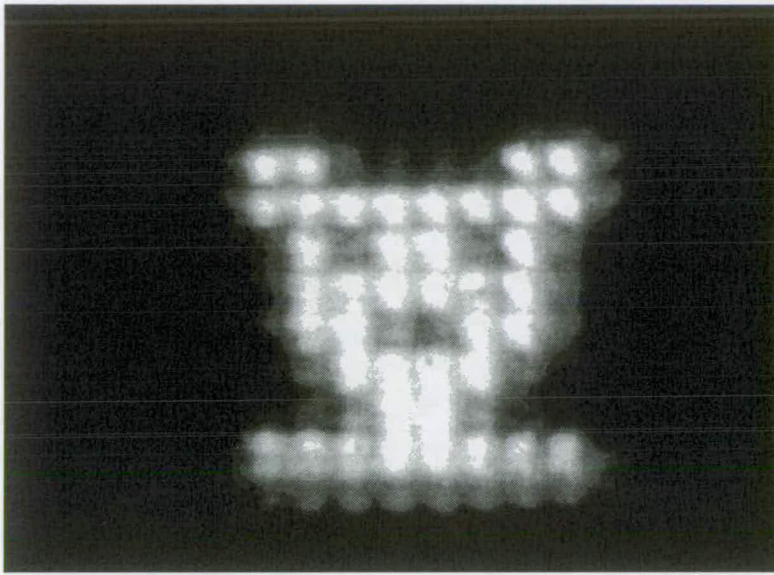
Figure 6.6: The test pattern reflected from the SLM (all pixels **ON**).

frequency information of input images for electronic processing systems. A wholly optical implementation which inputs an optical image, transforms it to a serial format, and then inverse transforms to generate a filtered or processed image is shown in figure 6.9. The forward transform is obtained as described above. If the inverse transform is required to be performed and the output is required to be an optical image, this can be generated by a similar optical system. As in equation 6.11, the serial coefficient values can be multiplied by their respective basis function and the summation of the equation components can by generated by optical integration. Such a technique may have application in short distance optic fibre coded image transfer. Figure 6.10 shows the optical/electronic hybrid system studied in this chapter and the all-optical system.

6.5 Future Work

The most obvious development of this work would to be to use an SLM with more pixels for a higher resolution transform. Other than the 176^2 SLM device available at present, larger array devices are at a stage near completion. With larger array transformation systems the main bottle neck would be the electronic addressing of the pixel array to write
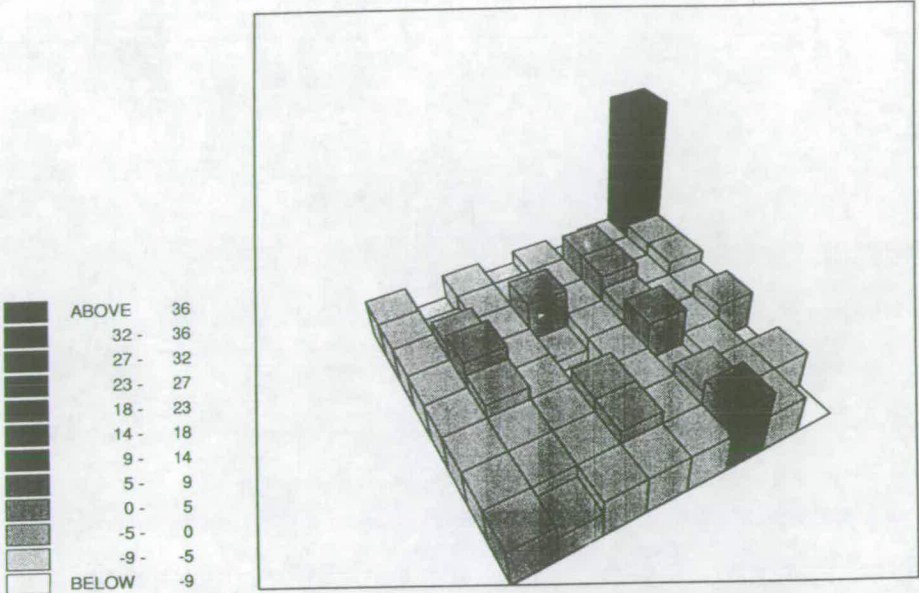
Figure 6.7: The optically measured Hadamard transform coefficients of the test pattern.
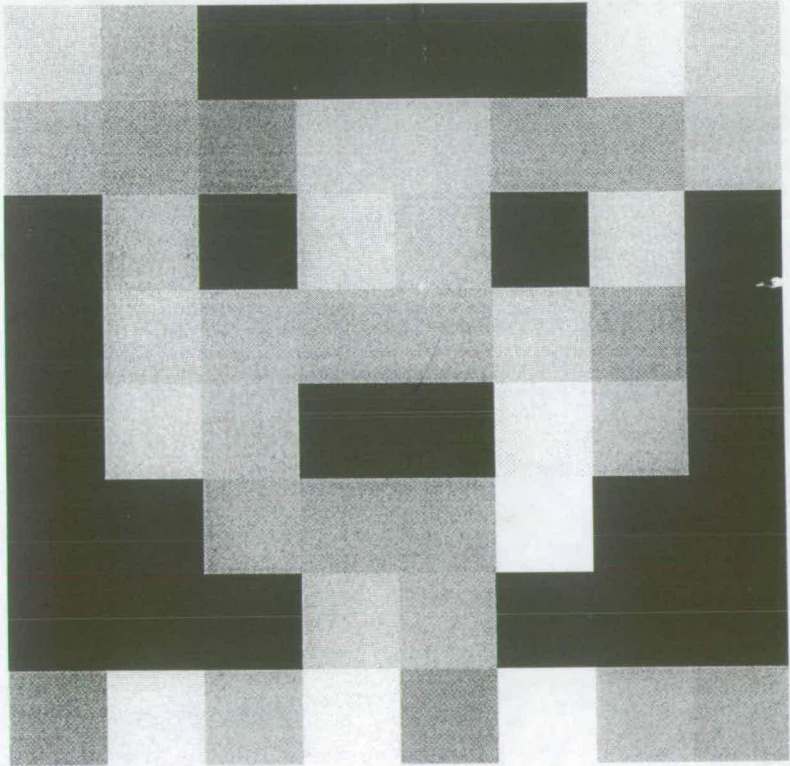
Figure 6.8: The electronic reconstruction of the test pattern from the optically measured Hadamard transform.

OPTICAL/ELECTRONIC HYBRID IMPLEMENTATION

photodetector

Electronic system for processing and inverse transformation

input scene   SLM mask   summing lens

ALL OPTICAL IMPLEMENTATION

optical channel

HADAMARD
TRANSFORM
DOMAIN

input scene   SLM mask   summing lens

optical inverse transform
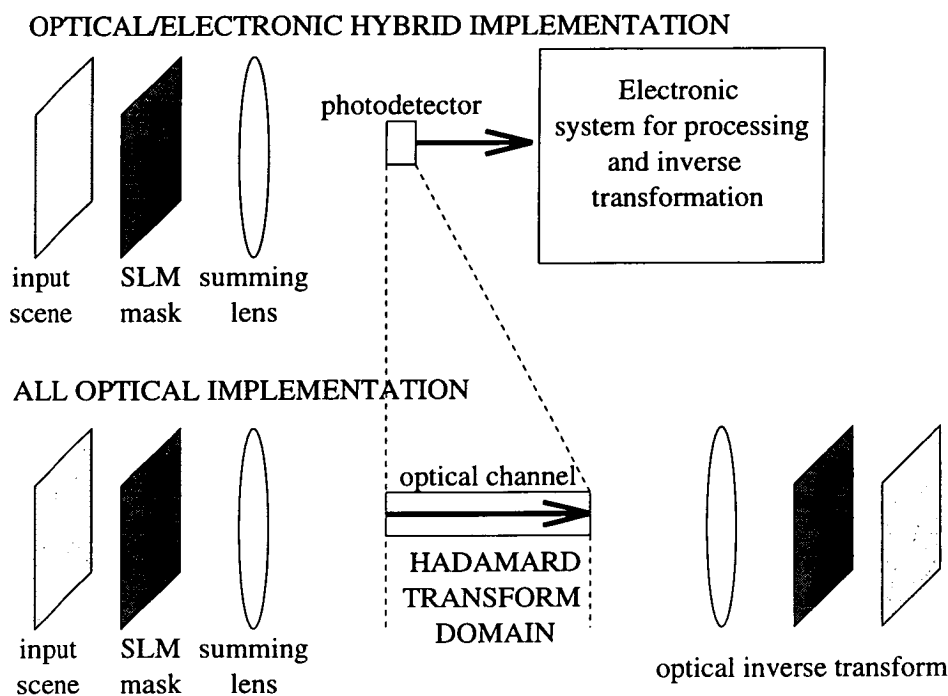
Figure 6.9: The two optical implementations of matrix transforms

the next basis function. At present this task is performed by relatively slow interfacing electronics. With the design of a dedicated VLSI backplane device for the Hadamard transform, the basis functions could be generated on-chip either through the use of cyclic vectors [125] in clocked shift registers for addressing the array or state machines in the shift registers or pixels. Thus, only power supplies and a clock signal need be applied to the device to display the required set of basis functions on the array. This would allow very fast operation of the SLM at frame rates approaching the optimum for the VLSI process used.

Other binary transforms should be investigated. The Haar transform seems particularly of interest as it is a wavelet transform with binary basis functions. It would be very interesting to compare and contrast the image processing capabilities of the Hadamard and Haar transforms. A more general approach to matrix transformations can be taken. The bases functions themselves could be optimised to perform specific functions. The optimisation could take the form of perhaps simulated annealing, to obtain the desired basis functions for certain transformation characteristics. In general, this would allow the specification of a transfer function. Sets of basis functions with properties (for example a

reduced number) for a certain application could be designed. Also, the basis functions on the forward transform could be different than those on the inverse transform. As an example one could envisage a simple recognition example. Basis functions could be 'trained' to distinguish between the letter A and the letter B input to the system. After transformation and inverse transformation a 'spot' at the top left at the output could indicate an A input and a 'spot' on the bottom right could indicate a B input. Such an optimisation of basis functions by adaptive learning is certainly a form of associative memory. It may even be possible to implement some forms of neural network in such a system.

6.6 Discussion on the Hadamard Transform

The use of high performance SLM devices for optical decomposition of images in terms of binary basis function may be a very useful technique for certain optical processing applications. A preliminary SLM system has shown this concept to be viable. Improved systems will allow the processing of 'useful' images for a variety of purposes. It is hoped that applications to which wholly electronic systems are not well suited, may benefit greatly from this work. Examples of applications such as frequency filtering of images have been considered and are presented in appendix D. Filtering operations can be extended to encompass more generalised transformation operations, and such operations may be adaptively implemented on the optical systems described.

High performance SLM devices are crucial for optical implementation of binary basis function decomposition. With on-chip basis function generation and new high-speed switching FLC material [127, 128] such implementations should be possible in excess of T.V. frames rates. Thus a highly useful compliment to current systems may be possible.

The main points of this chapter are:

- Matrix transforms are identified as potentially powerful techniques for image processing using non-coherently illuminated system application.

- The Hadamard transform is particularly suited to implementation by high frame rate binary SLMs.

- A 16^2 SLM, developed in chapter 5 has been used to demonstrate optical calculation of the Hadamard transform coefficients.

- This preliminary investigation suggests that further work with higher resolution SLMs should be performed.

Chapter 7

Coherently Illuminated System Applications

'Mehr licht!', the last words of J.W.Von Joethe, 1832.

In this chapter we discuss the performance of SLMs under coherent illumination. The main reasons for wanting to illuminate SLMs with coherent light are that high power laser sources can be employed and that the Fourier transforming properties of optical systems can be exploited [3, 2,   , 131]. In a Fourier optical processing system, one can employ phase modulation. This has the advantage of increasing the optical throughput and increasing the modulation efficiency. This will be discussed in the following sections.

7.1   Fourier Transforms of SLMs

Before assessing how an SLM operates as a phase modulator in a Fourier optical system, some points concerning the Fourier transform properties of the device should be discussed [1]. Appendix E discusses these points through analytical and simulation experimentation. As has been described, a simple lens can act as a Fourier transforming element (section 1.1.1) [3]. If coherently illuminated, the Fourier transform of an input object at the first focal plane of the lens, is obtained at the second focal plane. This is a very powerful processing operation. The actual Fourier transform is never actually observable at this plane, as on observation the amplitudes are squared to form intensities, and all
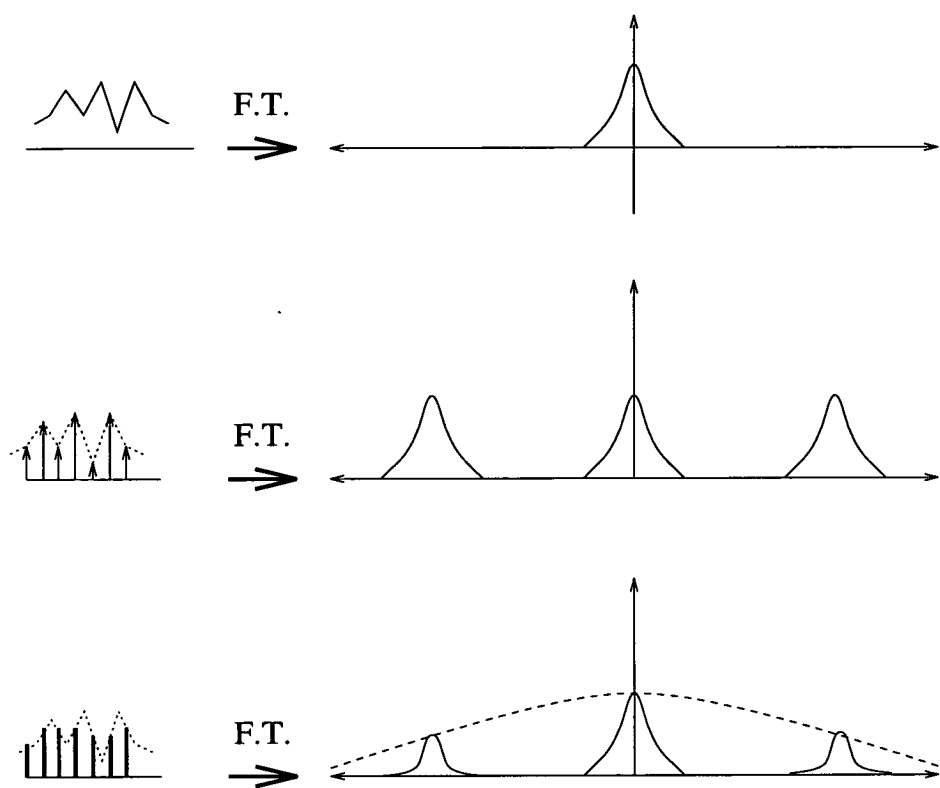
Figure 7.1: Fourier transform of discrete data.

phase information is lost. As in all coherent processors, the complex amplitudes can be manipulated extensively before observation.

In appendix E we discuss the implications of using a pixellated SLM in a simple Fourier transforming scenario. To summarise, a finite pixel size has important consequences for the resulting diffraction pattern resulting from the Fourier transformation of an SLM. This situation is depicted in figure 7.1, where the transform of continuous and discrete information is represented. Regular sampling data results in replications of the transform in the Fourier plane, and a loss of power into higher orders. With a finite pixel size, the intensity of the replicated orders are reduced. With a 100% fill factor (continuous data), all of the energy is in the central order (assuming an infinite data set).

7.2 SLMs as adaptive phase elements

Coding information in terms of phase modulation is a widely utilised technique [132]. The phase modulating capabilities of FLC devices were discussed in section 2.1 and simulated with simple gratings on an SLM device in appendix E. More elaborate phase patterns can be produced on SLMs for a variety of applications [133, 134, 135]. Two of the more obvious include Computer Generated Holograms (CGH) and efficient inputs and/or filters for optical processing systems[110, 26].

In appendix E we identified the pixel fill-factor as an important parameter in the Fourier transform of the SLM. The fill-factor determines the proportion of light energy routed to useful places in the Fourier plane. Light energy is diffracted into higher order replications due to the sampling and also remains in the d.c. term due to the reflectivity of non-modulating regions. Any detail smaller than the pixel dimension such as circuitry, defects and bumps on the mirror surface will diffract from the replications into other orders. This can contribute to noise in the zeroth order.

7.2.1 Optical System Considerations

The optical system (figure 7.2) designed for investigating the properties of the 176^2 SLM as an adaptive phase element consists of a collimated laser diode source ($\lambda = 670nm$, a X10 microscope objective, a $10\mu m$ pin-hole on an x-y-z positioner and a collimating lens f=140mm all configured to give a plane parallel wavefront), an input polariser, a non-polarising beam splitting cube, the SLM on a tilting, rotatable mount, an analyser, Fourier transforming lens (f=140mm) and a means of observation or measurement at the Fourier plane (CCD camera, ground glass screen, or x-y positionable pin-hole and light meter).

The dimensions of the SLM aperture, the wavelength of light and the Fourier transform focal length give an indication of the smallest discernable detail observable in the Fourier plane through the relation $u = \frac{\lambda f}{x}$ where f is the focal length of the lens, λ is the wavelength of light, x is the dimensions of the SLM aperture and u is the feature size
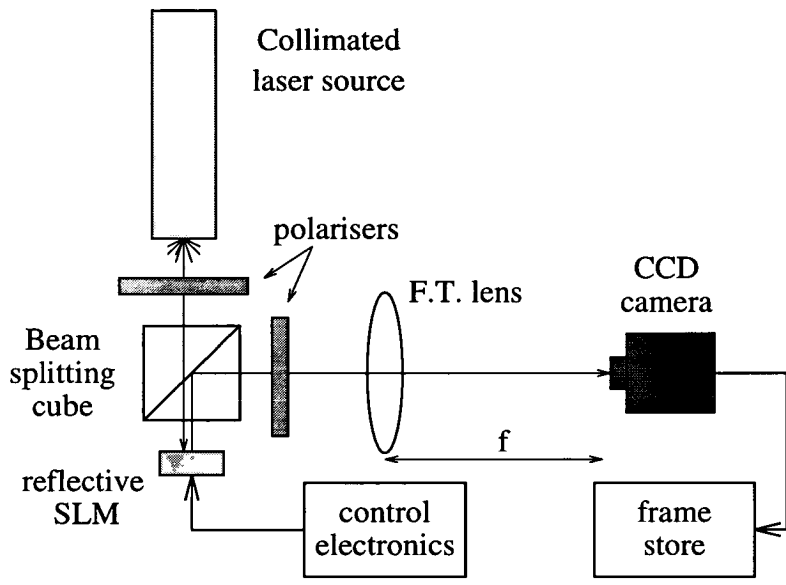
Figure 7.2: The optical system used in the CGH experiments.

(resolution) in the Fourier plane [1](appendix E). This relationship can also give the spacing between the replicated diffracted orders if x is regarded as the SLM pixel pitch and u is regarded as the spacing between the replications. For the 176^2 SLM in this system the aperture is $5.28mm$, the pixel pitch is $30\mu m$, $\lambda = 670nm$ and $f = 140mm$. This gives the smallest discernable detail in the Fourier plane of order $20\mu m$ and the replication separation as $\approx 3mm$. These values were calculated to fit well with the CCD camera [110]. The data frame obtained from the CCD camera is 512×512 pixels with 8-bit values, allowing a linear 256 level accuracy on intensity or peak height measurement.

7.2.2 Spot measurement and figure of merit definitions

Before discussing optical SLM diffraction experiments, some definitions must be clarified.

- **Spot** intensity **measurement**

  Diffraction patterns can be recorded by CCD camera. To compare the intensity of diffraction peaks obtained, the Full Width at Half Maximum (FWHM) is measured, and squared, and multiplied by the height of the peak. This approximates

the volume under a Gaussian, and allows direct comparison between peaks of different intensity: the higher the intensity, the higher and wider the peak.

- **Efficiency**

  This is a comparison of light intensity in the diffracted peaks of interest in the zeroth diffraction order and the total light incident onto the SLM i.e. **light in peaks/total incident light**. This takes into account the losses in the SLM modulation, polarisers, optics, scattered high frequencies, replicated orders due to pixellation and d.c. peak. The d.c. term can be due to non-ideal modulation, phase nonuniformities, FLC missalignment, hologram reproduction inaccuracies, and theoretical limitations. The measurement is performed by use of a light meter examining the laser output directly and the light intensity of a peak in the Fourier plane incident through a pin-hole.

- **Reflected Diffraction Efficiency (RDE)**

  This is a comparison of the light intensity in the diffracted peaks of interest in the zeroth diffraction order and the total light in the Fourier plane i.e. **light in peaks/total light in Fourier plane**. The gives a figure of merit for the diffraction including the d.c. term, higher order diffraction terms and general noise. The measurement is performed by use of a light meter collating all of the light at the Fourier plane and the light from a peak in this plane incident through a pin-hole.

- **Zeroth Order Diffraction Efficiency (ZODE)**

  This is a direct comparison of the light intensity in the diffracted peaks of interest in the zeroth diffraction order and the light in the d.c. spot i.e. **light in diffracted peaks/d.c. peak + light in diffracted peaks**. This ignores the replications and gives a figure of merit only in the zeroth order. The measurement is made from FWHM on CCD camera data.

The figures of merit can give useful comparison between different SLM devices. Comparison with static holograms would normally use the RDE, but the overall efficiency gives a greater insight into the SLM performance as it would be observed in an optical system. The ZODE is the easiest measurement to perform, only requiring CCD camera data. The overall efficiency and the RDE require a pin-hole to be accurately manouvered in the Fourier plane and measurement from a light meter. As the 176^2 SLM has

some difficulty working well under high light intensity, the accurate interpretation of measurements using this techniques are problematic.

7.2.3 A comparison of fill-factors with the 176^2 SLM

Comparisons have been made between a planarised and a non-planarised device, when used as phase gratings and holograms in Fourier optic systems. The main improvement to such systems from planarised devices is due to the higher phase-flat fill-factor. This increases greatly the diffraction efficiency of phase modulation. This has been demonstrated through calculation and simulation (appendix E), but more importantly, this will be presented, in optical SLM experiments.

A simple one-dimensional grating pattern, with a pitch of 8 pixels, was displayed on planarised and non-planarised 176^2 SLMs. With coherent illumination (continuous, 670nm), a simple lens (f=140mm) gives the Fourier transform when SLM-to-lens and lens-to-viewing plane distances are the focal length of the lens. The resulting diffraction patterns are shown for the non-planarised SLM in figure 7.3, and planarised SLM in figure 7.4. The differences are considerable. The diffraction peaks in the non-planarised case are barely visible compared to the d.c., but are much larger than the d.c. for the planarised case. The ZODE gives $4.5^+_-0.5\%$ for the non-planarised device and $75.5^+_-0.5\%$ for the planarised device. This will tremendously improve any signal-to-noise ratio at detection in the Fourier plane. The value is still relatively low due to the laser source not being pulsed. This results in the SET and RESET time slots in the SLM addressing (which blank the pattern) to contribute to the d.c. peak.

7.2.4 Efficiency measurements on the planarised 176^2

Efficiency measurements were performed on the planarised 176^2. The difficulties in this measurement necessitated higher light intensities than employed in the previous section. Therefore a higher power laser source was employed (10 mW, $\lambda = 633$ nm). This results in any photo-induced charge leakage adding to the effects of the SET and RESET time
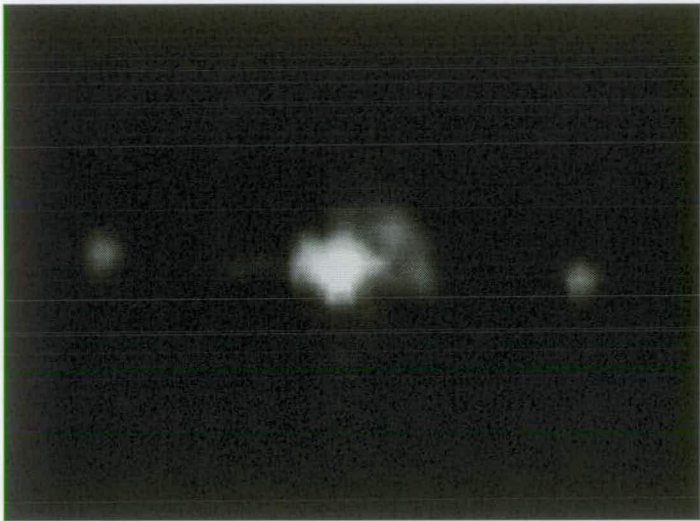
Figure 7.3: The diffraction pattern obtained from an unplanarised SLM
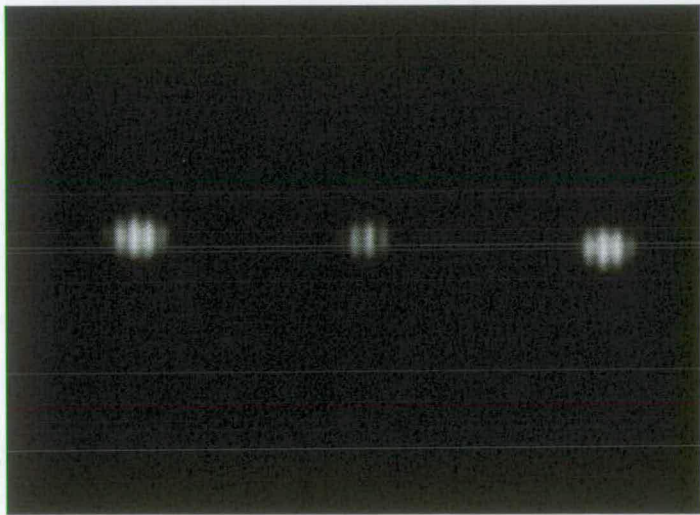
Figure 7.4: The diffraction pattern obtained from the planarised SLM

slots in the SLM addressing which all contribute to the d.c. term. As before, a one-dimensional grating pattern was displayed on the SLM. A $100\mu m$ pinhole was used to isolate a single diffracted peak in the zeroth order for measurement on the light meter. The optical system components were optimised to achieve a minimum d.c. spot intensity and rather than a high optical throughput. It was thought that a high signal-to-noise was most desirable for useful application, and therefore minimising the d.c. peak would be the most important parameter. Therefore, these measurement represent the SLM device operating in 'worst case scenario' as far as throughput conditions are concerned. The measurements are as follows:

- Light intensity from laser source: $10^+_-1\mu W/cm^2$

- Total light intensity at Fourier plane: $60^+_-2nW/cm^2$

- Light intensity in d.c. peak: $20^+_-2nW/cm^2$

- Light intensity in diffracted peak: $10^+_-2nW/cm^2$

As can be seen from the measured values, the RDE has a value of 33% and an overall system efficiency of 0.2% (light from laser/light in peaks). The lower RDE value can be attributed mainly due to the SET and RESET addressing and photo-induced charge leakage contributing to the d.c. (and its replications) as can be seen from the much lower ZODE (in this case 50%). The overall efficiency is very low and can be attributed to the high optical losses in the components and particularly the FLC material, which is in a chevron structure (section 2.8.2). The polarisers were orientated to reduce the light incident onto the SLM from the laser, which is included in the measurement.

7.3 Computer Generated Holograms

CGHs are very useful components in 2-D optical information processing systems. These holograms are created by computer simulation by a variety of optimisation techniques. The phase information is usually plotted out and transferred to a photolithographic mask to allow the fabrication of the hologram in a suitable phase material. For example,

photoresist on a glass substrate is patterned by the photolith mask and the exposed glass is etched to the required depth. In most cases the holograms are binary, although with suitable masks and multiple processing, multilayer holograms can be produced. Binary holograms have a maximum theoretical diffraction efficiency of 81% [136]. This efficiency is increased as the more levels are introduced. An analogue phase hologram, known as a blazed surface relief, has a theoretical efficiency of 100 percent [137].

7.3.1 CGH Applications

CGHs have a number of interesting applications. They are very useful as array generators for optical interconnection, where one optical beam is 'fanned out' to produce multiple beams to certain destinations [133]. This can be considered to be like optical 'wiring', where the hologram allows potentially lossless routing. Three dimensional stereoscopic display is another application under investigation [135]. The production of a display hologram where the object does not necessarily exist is of particular interest. The uses of such techniques include the representation of models to demonstrate building designs or molecule design. Various views of the object are coded into the hologram, which when viewed suggests a full 3-d image. Holograms can also be used to generate lenses (diffractive optical components) or be used for beam shaping [138].

7.3.2 Binary CGH Design

There are a variety of techniques for calculating binary CGHs. Most are based on the Fourier hologram. The optical wave passing through the phase pattern is altered and this is Fourier transformed with a lens to create an intensity distribution in the Fourier plane. The best two phase states for a binary hologram differ by 0 and π. In computer simulation, the hologram pixels are changed between the values 0 or π by some optimization technique until the required (or close to required) pattern is obtained on Fourier transform. Numerous techniques for the optimization of the hologram pixels are employed. Most of these are based on simulated annealing, but with a variety of ways of calculating the cost functions [139].

7.3.3 SLMs as phase holograms

FLC/VLSI SLMs are limited to producing binary phase patterns. Several parameters are used to determine the information coding ability of CGHs and these apply also to SLMs [18].

- **Fill factor:** Ideally the controllable pixels should cover the the entire surface of the SLM as this maximises the efficiency. With improved planarisation techniques the fill factor should be increased to > 95 percent. With the 176^2 SLM backplane the fill factor is $\approx 30\%$, and increased to $\approx 80\%$ through planarisation.

- **Phase Modulation:** The controllable pixels in the SLM should alter the phase by exactly 0 or π for optimum efficiency. This condition is impossible to attain exactly in fixed binary holograms due to fabrication limitations, but is attainable in FLC devices (see section 2.7.2).

- **Pixel pitch** The pixel pitch should be as small as possible to give a maximum number of line pairs/mm as this determines the separation of the diffractive orders and maximises the angle of diffraction so allowing more compact systems.

- **Space BandWidth Product (SBWP):** This is the number of binary pixels across the hologram. A large SBWP is required to encode a large amount of information. The 176^2 SLM device has a very small SBWP compared to fixed CGH recording techniques.

The main limiting factor with CGHs on current SLM devices is the low SBWP. Only with much larger arrays will this be improved. Techniques such as encoding a replicated pattern from an EASLM onto an OASLM device has been employed to improve the SBWP by O'Brien [18, 140] with a certain amount of success. The main advantage of using SLMs for display of CGH is that they are adaptive and the hologram can be altered or indeed calculated in real-time. This is a highly attractive feature for many applicationsoutweighing many of the disadvantages.
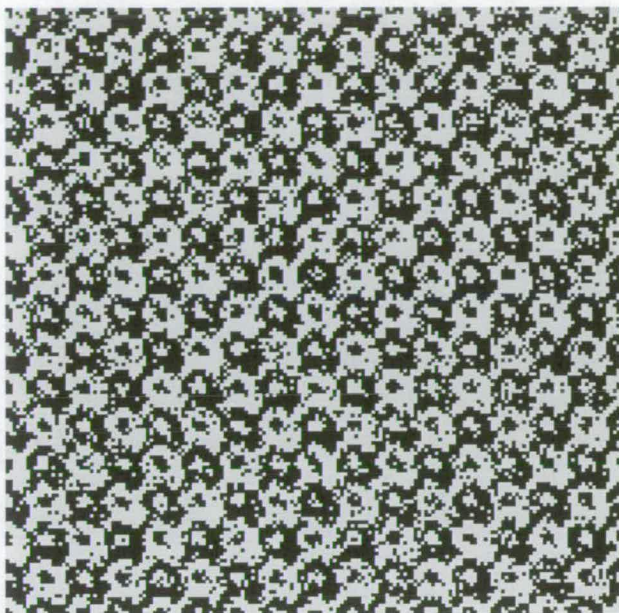
Figure 7.5: An example of a computer generated hologram

7.3.4 CGHs on SLMs Simulations

The effect of different pixel fill-factors through simulation is presented in appendix E.

7.3.5 Real-time display of CGHs on SLMs

Some of the other SLM devices described in section 1.3 have been used to demonstrate phase modulation [79, 141]. CGHs were designed to perform the function of an array generator and allow the SLM device to be used as an adaptive fan-out element. The phase hologram was designed using simulated annealing optimisation techniques by S.Samus [139]. The hologram pixels are flipped between the values 0 or π to effectively reduce an error function specifying the difference between the desired target Fourier plane reconstruction and the reconstruction achieved by the current state of the hologram. To ensure that the final hologram has the lowest error possible, changes that increase the error may be accepted. Accepting these energy increasing steps is governed by a statistical probability that reduces over time so allowing the algorithm to converge.
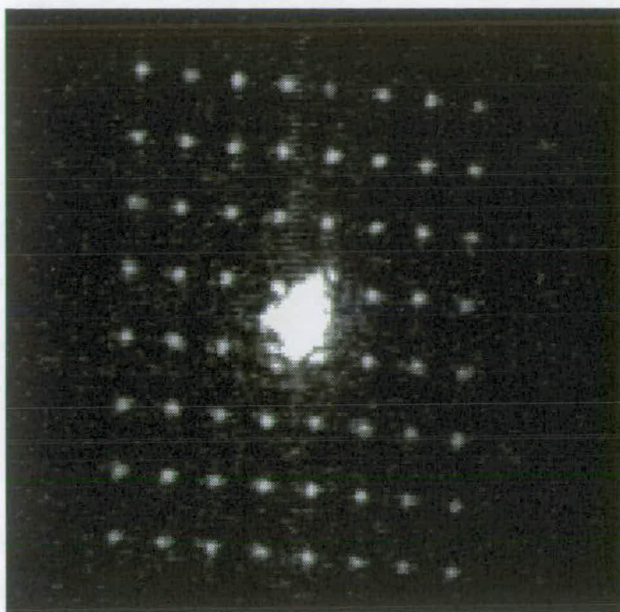
Figure 7.6: An 8 by 8 holographic fanout element produced from the unplanarised 176^2, note the enormous d.c. spot.

A CGH was designed to generate an 8×8 array of spots. The ZODE is 5% when simulated with a 25% fill factor at the 176^2 elements. The ZODE measurement allows a more direct comparison between simulation and optical experimentation. Figure 7.5 shows a calculated phase pattern which was subsequently displayed on an unplanarised 176^2 SLM. The resulting Fourier transform obtained at the CCD camera is shown in figure 7.6. The d.c. term is very large and is saturating the response of the CCD camera. The ZODE for this hologram is $2.5^+_-0.5\%$ and the peaks vary in intensity by as much as 30%. Figure 7.7 shows the result of the same CGH pattern displayed on the planarised 176^2. The ZODE in this case is $94^+_-3\%$, but the variation in the individual peak intensity is large due to the 'roll-off' induced by the pixel function transform. Figure 7.8 shows an example of a more general CGH spot pattern produced from the SLM.
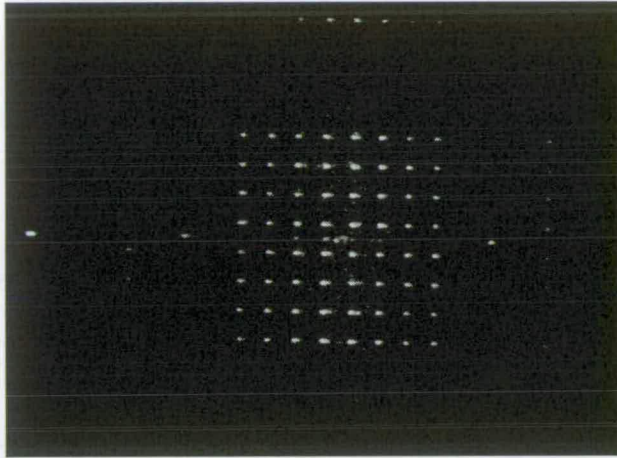
Figure 7.7: The 8 by 8 fanout displayed on the planarised 176^2.

7.3.6 Re-evaluation of the ZODE for the planarised 176^2 SLM

To improve the fanout patterns produced by the display of CGHs on the planarised 176^2 device, a pulsed laser source was employed to examine the narrow time slot, just after instant when the CGH was written to the SLM. This would remove the effects of the SET/RESET slots and minimise the effects of photo-induced charge leakage. Due to the limiting accuracy of the CCD camera (256 levels), one can employ a fanout CGH to split the diffracted light into a larger number of peaks, to improve the accuracy of the measurements. This was performed with a 4×4 fanout. The resulting CCD camera data is shown in figure 7.9 and 7.10. The level in each diffracted peak was 250^+_-5 and in the d.c. term 25^+_-5. This gives a value for the ZODE of $\approx 99\%$. This is a considerable improvement and shows that the device would be highly useful in Fourier optical processing systems as most of the light is modulated and the signal-to-noise level would be very high.

7.3.7 Discussion on CGHs on SLMs

The optical results from the grating and CGH experiments show that the evaluated experimental diffraction efficiency is lower than that expected from simulation and an-
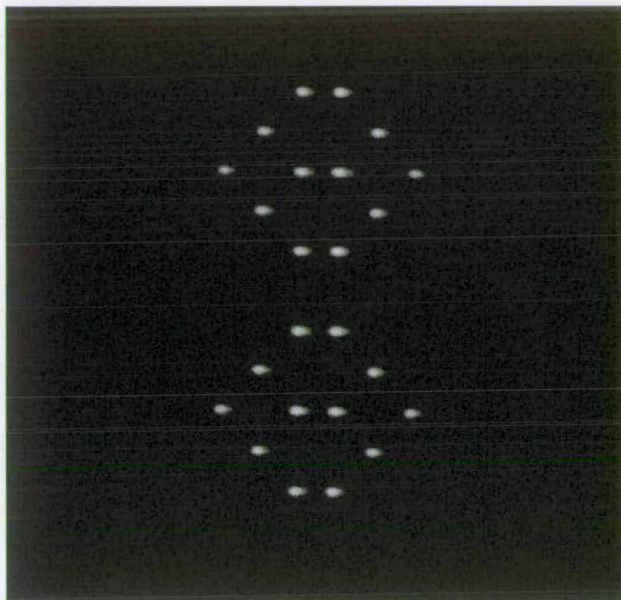
Figure 7.8: A custom fanout displayed on the planarised 176^2.

alytical studies in appendix E. The large spread of diffracted light around the on-axis d.c. spot indicates some of the difficulties present in using unplanarised SLM devices for reflective phase holograms. The light in the d.c. spot is obviously very high due to the low fill-factor and will swamp low frequency information. In planarised devices the main limiting factor will be liquid crystal defects. These will cause poor modulation, losses in optical throughput, diffraction noise effects in the Fourier plane and general scattering of the coherent light. The CGH should be designed with the pixel fill-factor taken into account as the design could be more fully optimised. This could reduce the 'roll-off' effect evident in figure 7.7.

7.4 Discussion

Planarisation techniques may be used to overcome the problems associated with the VLSI fabricated circuitry and mirrors, and the additional effect of liquid crystal defects. The main concern must be the low overall efficiency. This can only be improved through further work on the planarisation and the liquid crystal alignment. Also, particular regard must be made to the refractive index matching of the various interfaces and
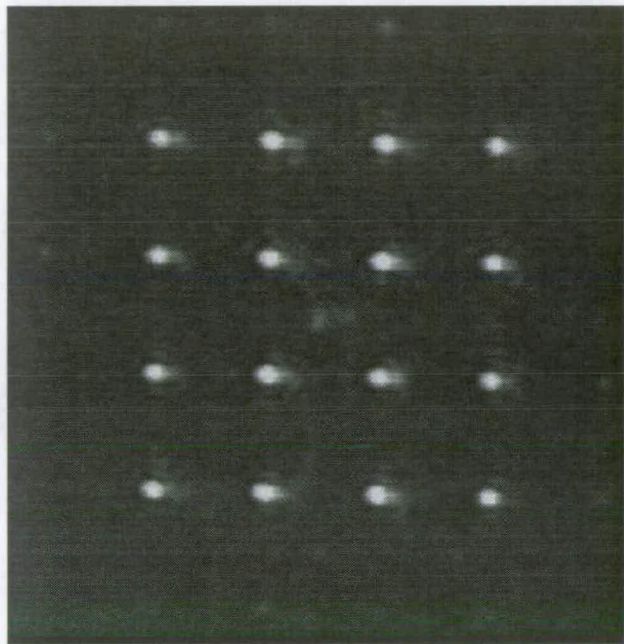
Figure 7.9: A 4 by 4 fanout displayed on the planarised 176^2.
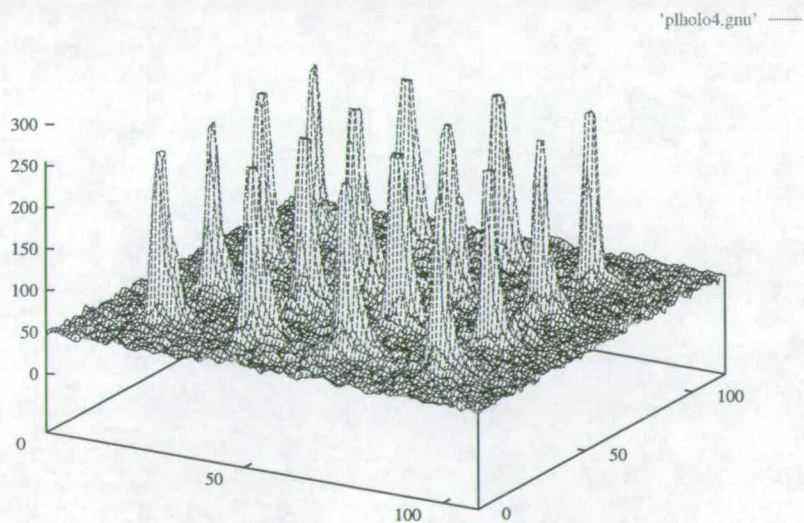
Figure 7.10: CCD camera data obtained from 4 by 4 fanout CGH displayed on the planarised 176^2.

anti-reflection coatings (MgE$_2$) should be employed.

The present 176^2 SLM device has a small space bandwidth product (SBWP), the number of pixels forming the hologram, compared to fixed CGH fabrication techniques. A higher SBWP allows the encoding of more information, an increase in the efficiency in the resulting Fourier transform i.e. more power in the zeroth order and a much improved signal-to-noise level. Techniques may be employed to improve the SBWP such as encoding a replicated pattern from an electronically addressed SLM onto an optically addressed SLM device. Another system consideration is that the pixel size should be as small as possible to give the maximum number of line pairs/mm. This determines the separation of the diffractive orders and maximises the angle of diffraction that may be achieved. This SLM technology will gain from all the improvements in CMOS silicon processing as smaller circuit geometries become practical, and larger array FLC/VLSI SLM devices are currently being designed.

As well as CGH applications, an adaptive phase modulating element is required for Joint Transform Correlation (JTC) applications. The JTC is a particular Fourier optics processing system. The theoretical background to the the JTC is discussed in appendix F, and describes simulation work showing how binary SLMs can be employed in practical systems. This suggests that FLC/VLSI SLMs would be useful to achieve such systems.

This chapter has shown that:

- SLMs have a great potential for performing the function of adaptive phase elements in Fourier optic systems.

- The SLM pixel fill-factor was identified as an important parameter in the performance in such systems.

- The effect of increasing the fill-factor on the 176^2 SLM was demonstrated.

- In general, a high phase-flat fill-factor is crucial for high performance devices.

- CGHs were demonstrated with the 176^2 SLM, showing a good performance.

- The overall efficiency of the SLMs are as yet very low due to losses in the FLC defects.

- The diffraction efficiency is very high.

- CGH design should take into account the particular device design parameters, particularly the fill-factor and pixel mirror shape.

- At present, with any use of the device in a real system, certain trade-offs must be made with regard to the overall efficiency and the diffraction efficiency.

Chapter 8

Conclusions

'and much study is the weariness of the flesh', Ecclesiastes 12:12.

8.1   Ferroelectric Liquid Crystal Devices

This study has concentrated on the implications of constructing FLC structures on VLSI silicon backplane SLMs. We have reviewed and discussed the idealised device performance which was promised by optimistic research in the 1980's. The reality of the situation was shown to be much more complicated in chapters 2 and 3. In chapters 3 and 4 we have assessed and improved the performance of existing FLC techniques. The FLC device fabrication techniques which we have developed, provide a route towards high quality test cells. Device performance characteristics have been obtained for the SSFLC device, the DHE device, the Soft-mode Electroclinic device and the Twisted Smectic device. From these studies, the SSFLC device was considered to be the most suitable structure for fabrication onto binary switching VLSI backplane SLM devices. The reasons for its selection include the binary nature of the switching, its bistability and high contrast ratio. Although its switching speed is somewhat slower, the other characteristics compensate for this deficiency, particularly in large array modulators, where the electrical addressing is the main limiting factor. The successful development of the in-house fabrication techniques for these device structures is an important achievement. Only through this development, could this study have been accomplished. The other de-

vice structures have important implications for fast switching analogue modulation, but their application in SLM devices would require the design of analogue VLSI backplane modulator arrays. The main conclusions are therefore:

- The subject of FLCs is extremely wide and it was found impossible to cover all of the many aspects.

- Very useful empirical studies were performed with simple glass test cells to assess the optical performance of FLCs.

- The SSFLC device structure was identified as extremely powerful and of greatest applicability to VLSI backplane SLMs at present.

- Fabrication techniques were developed for practical SSFLC devices which yielded results and consistent quality.

- Preliminary investigations of alternative FLC device structures were carried out. These novel LC structures have great potential for particular applications, and warrant further study.

8.2   VLSI Silicon Backplane Devices

Although no VLSI backplanes were designed in the course of this study, the critical step of fabrication of backplanes into full SLM devices was performed successfully. This has resulted in reproducable techniques for the construction of SLM devices. The two main VLSI backplanes under investigation were the 16^2 and 176^2 arrays, both designed at the University of Edinburgh. These allowed the important appraisal of the fabrication techniques and resulting modulation performance, with regard to the SLM backplane characteristics. This is the most complete study of the backplane and FLC interaction as far as the author is aware. The main points include:

- The design of modulator circuits in VLSI silicon is an extremely powerful technology.

- Fabrication techniques to produce SLM devices were developed. These could easily be applied to commercial production.

8.3   Compatability of the Two Technologies

Fabrication of SLM devices and their comparison with the glass test cells showed the compatability of the devices. Through this study, it has been shown that standard VLSI fabrication techniques are not wholly sufficient for obtaining high quality FLC modulator devices. This has been a very important conclusion for the future development of such devices. Further post-processing techniques as performed by A.O'Hara are required to allow the FLC device parameters to approach that obtained in test cells. This work is continuing. Nevertheless SLM devices have been successfully constructed for use in optical systems. The crucial points include:

- The problems associated with FLC/VLSI SLMs were investigated and addressed. Of particular importance is the quality of the metal pixel mirrors.

- Techniques for resolving these difficulties were examined, particularly planarisation, and routes towards high quality devices followed.

- 16^2 and 176^2 SLM devices were made available for system demonstrators.

8.4   System Applications

Two novel system applications have been successfully demonstrated using the devices developed. As well as being very interesting system demonstrators, they have confirmed the conclusions concerning the performance characteristics of the SLMs in real application. As far as the author is aware, these systems have not been demonstrated with this type of SLM device, indeed the Hadamard system has not been demonstrated with an SLM before. Both noncoherently illuminated and coherently illuminated systems have been studied. Perhaps the most important general consequence of the system work has

been to show which device parameters are the most limiting. This is highly illuminating for optimising the backplane and FLC characteristics for future devices. The main conclusions from the systems work include:

- Two novel optical systems were developed to allow the demonstration of the SLMs.

- The Hadamard transform system requires high resolution, fast frame rate SLMs for practical application.

- The pixel fill-factor was identified as an important parameter when SLMs are used in Fourier transform systems.

- Increasing the fill-factor through planarisation resulted in great improvement to the performance.

- FLC/VLSI SLMs have great potential in Fourier transform systems.

- The mirror quality and FLC alignment are major factors in determining the overall device efficiency in a system environment.

8.5 Final Summary

This study is really a 'snap-shot' of a much wider endeavour. It was particularly difficult to decide at which point to start and at which point to conclude the work. The study started essentially at the beginning, with FLC device development, but by-passing the need to design VLSI backplanes. However, the work concluded by only preliminary demonstration of the developed devices in optical systems. This work is ongoing. The greater importance of this research has only recently been revealed, as the international optical community seemingly turns away from GaAs circuit technology, with its high power requirements and low yields, towards silicon based modulator technology for smart optical processing arrays. GaAs will of course still remain a highly important technology for fabricating lasers, detectors and small arrays of modulators. This study has demonstrated the many advantages and great potential of FLC/VLSI silicon modulator arrays which will be required for future advanced optical processing systems.

Chapter 9

Publication List

1.GOURLAY J., McOWAN P., VASS D.G., UNDERWOOD I. and WORBOYS M.:
**Hadamard Transforms with Ferroelectric Liquid Crystal-over-Silicon Spatial
Light Modulators**, Spatial Light Modulators and Applications Technical Digest, (Optical Society of America, Washington, D.C., 1993), Vol. 6, pp. 100-103, (1993).

2.GOURLAY J., McOWAN P., VASS D.G., UNDERWOOD I. and WORBOYS M.:
Optical Engineering Aspects of Ferroelectric Liquid Crystal-over-Silicon Spatial Light Modulators The Institute of Physics (U.K.) Proc. Conf. Appl. Opt. and
Opto-electronic, Leeds, U.K., (1992).

3.STEVENS A., GOURLAY J., VASS D.G.,: Patent Applied For.

4.GOURLAY J., McOWAN P., VASS D.G., UNDERWOOD I. and WORBOYS M.:
Time-multiplexed optical Hadamard image transforms with ferroelectric liquid crystal-over-silicon light modulators Opt. Lett. 18, 20, Oct.15, (1993).

5.GOURLAY J. and VASS D.G.: **A high phase-flat fill-factor reflective ferroelectric liquid crystal spatial light modulation for real-time adaptive phase modulation** accepted for CLEO/Europe-EQEC Conference, Amsterdam, 28th Aug -
2nd Sept 1994.

6.GOURLAY J., SAMUS S., McOWAN P., VASS D.G., UNDERWOOD I. and WOR-BOYS M.: **Real-time binary phase holograms on a reflective ferroelectric liquid crystal spatial light modulator.** Accepted for Applied Optics.

7.GOURLAY J., McOWAN P. and VASS D.G.: **Hadamard transform image processing and its optical implementation with ferroelectric spatial light modulators** submitted to the International Journal of Optoelectronics

8.HEDDLE S., GOURLAY J., SAMUS S. and VASS D.G.: **Optical interconnect using pixellated spatial light modulators** accepted for Optical Computing 94 Conference to be held at Heriot Watt, Edinburgh.

9.UNDERWOOD I., VASS D.G., O'HARA A., BURNS D.C., McOWAN P.W. and GOURLAY J.: **Improving the performance of liquid-crystal -over-silicon spatial light modulators: Issues and achievements** Appl. Opt. **33**, No.14, 14th May (1994)

10.COLLINGS N., GOURLAY J. and VASS D.G.: **The use of structured illumination with pixellated SLMs** submitted to Applied Optics.

11.UNDERWOOD I., O'HARA A., BURNS D.C., GOURLAY J. and VASS D.G.: **Ferroelectric liquid crystal over silicon spatial light modulators for optical computing** accepted for the Optical Computing 94 Conference to be held at Heriot Watt, Edinburgh.

An SLM demonstration system showing the 176^2 device performing reconfigurable holographic interconnection and a poster have been presented at the JFIT conference, Heriot Watt University, March 94, and the 176^2 SLM demonstration plus a 256^2 SLM shown at Optical Computing 94 conference, Heriot Watt University, August 94.

Appendix A

Theoretical Models of FLCs

There are numerous theoretical approaches one can take toward FLCs. Three of the most useful to gain insight are a thermodynamic approach, studies of the molecular switching dynamics and comparisons with the ferroelectric capacitor. Thermodynamic models can explain the structure of the various phases and the spontaneous polarisation. Molecular dynamical models describe the electrical and optical switching characteristics. Useful models of ferroelectric capacitors exist which can be used to examine some of the electrical properties of FLC devices.

A.1   Thermodynamic models

Models can be obtained by considering Landau theory and symmetry arguments.[54] One can consider the LC material as a continuous deformable medium, obeying the laws of elasticity. The general theory for nematics is essentially complete. At present there is is no general theory for smectics due their much more complicated structure. The elastic theory for LCs relies on complicated expressions for the elastic energy density of the medium under small deformations. The phenomenological Landau free energy expansion for FLCs reflects the symmetry properties of the medium. As the spontaneous polarisation does not cause the paraelectric-ferroelectric transition, it has not been found to be very useful as an order parameter. A very useful theoretical treatment can be found in [62]. The goal of these models is to describe all aspects of the phase transitions, for example, the specific heat. At its simplest level, the tilt vector of the long axes can be a useful parameter. Unfortunately, the contributions from the helical structure and coupling terms between the tilt and the spontaneous polarisation makes things very complicated. By minimising the Landau free energy expansion with respect to introduced parameters, it is

possible to obtain the temperature dependence of these parameters. As a simple example one can consider the optical tilt angle   just below the SmA-SmC* transition.[62] The theoretical temperature dependance of optical tilt angle for this second order phase transition takes the form:

$$\theta(T) = \theta_o(T_c - T)^B \tag{A.1}$$

where $\theta(T)$ is the tilt angle at temperature T, T_c is the phase transition temperature, θ_o and B are constant and T is temperature. Equations such as this have been experimentally verified. Symmetry arguments can explain the source of ferroelectric behaviour. In the tilted smectic phases, molecules have a local monoclinic environment which has the following symmetry elements: a centre of inversion; mirror plane ; two-fold axis of rotation. If these molecules are designed to be optically active, the symmetry elements are reduced to a single polar C_2 axis, parallel to the layer planes and normal to the plane that contains the tilt axis of the molecules.[54] The P_s in the bulk is therefore assumed to be generated through a coupling of lateral components of the dipoles of individual molecules with the chiral centre. Only the time averaged projection of the dipole moments along the polar C_2 axis is effective in producing the macroscopic spontaneous polarisation. Current theoretical research is further enhancing the models of FLC to better represent the results from experimental representation.

A.2   Dynamical switching models

The switching mechanisms and states can be investigated by giving the rod-like molecules equations of motion [54, 142]. Much effort is being employed to describe the optical and electrical characteristics in terms of the director profile. The non-fully solved models derive this director orientation from molecule and energy related parameters of material and boundary conditions. The LC molecule simply rotates around its axis to minimise the interaction energy. This interaction energy is given by $-\mathbf{P}.\mathbf{E}$ where $\mathbf{P}$ is the polarisation and $\mathbf{E}$ is the applied external electric field. This relation is minimal when the electric field and the polarisation are aligned parallel. This can be used to obtain simple switching models for the molecules such as:

$$\gamma\frac{d\varphi}{dt} = PEsin\varphi \tag{A.2}$$

where γ is the rotational viscosity and φ is the angle of the molecular director with the bounding plates. One can derive from this the switching time of the FLC device in the high field, low surface energy limit:

$$\tau_s = \frac{\gamma}{PE} \tag{A.3}$$

Therefore the switching time is proportional to the viscosity and inversely proportional to the spontaneous polarisation. This gives a useful guide to the selection of material parameters. The
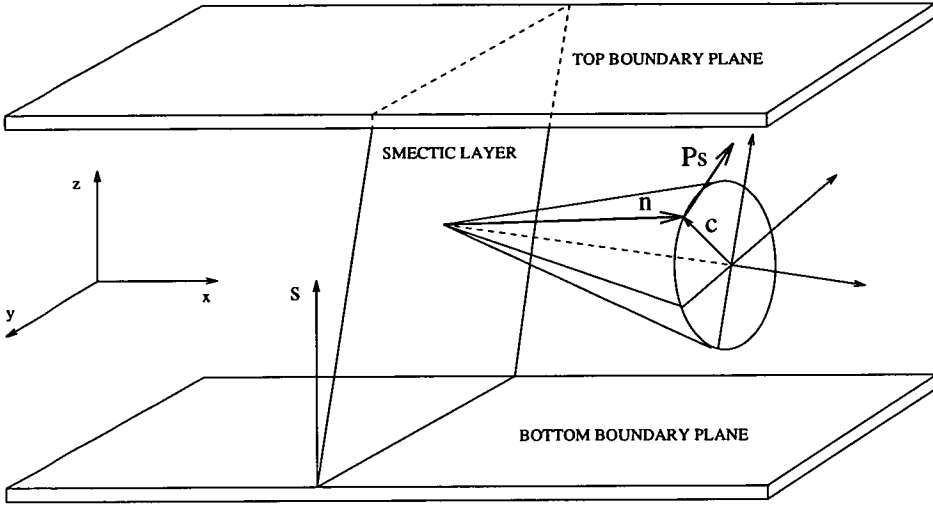
Figure A.1: The dynamical switching model

latching time, which is the time for the molecule to latch into a specified state, is proportional
to the switching time. The latching can be represented by:

$$E\tau_m = k\frac{\gamma}{P_s}$$
(A.4)

Where E is the applied electric field, τ_m the latching time, k is a constant depending on the
latching properties (surface and initial states) and P_s is the spontaneous polarisation. This can
be restated that the voltage multiplied by the latching time is a constant A. This means that
a certain driving pulse area is required to achieve latching. This critical pulse area A has been
experimentally verified [34]. For pulses below area A some switching is obtained but no memory
latching is observed [142]. This shows that some grey level switching capacity is available in
bistable ferroelectric devices. Such simple models are very useful but are complicated by elastic
boundary effects, dielectric torques, conductivity, tilt angles and distortion of the smectic layers.
The switching speed of the molecule is highly dependent on the P_s. From these arguments a
higher switching speed will be obtained by producing high P_s material.

A.3   The Ferroelectric Capacitor

There is a good analogy between ferromagnetic behaviour and ferroelectric behaviour [54]. Fer-
roelectric material is characterised by a spontaneous electric polarisation which can be removed
or reorientated by the application of external electric fields. At low fields the ferroelectric do-
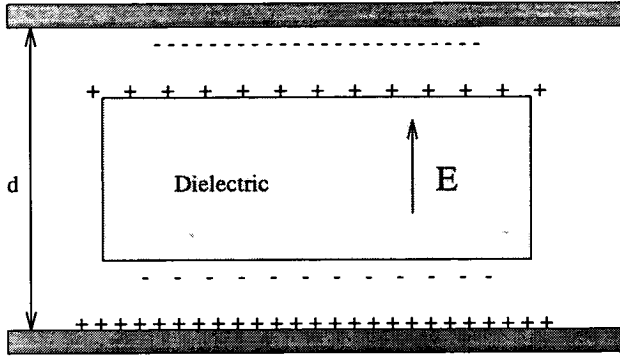
Figure A.2: The ferroelectric capacitor model

mains are relatively unaffected. But at large fields, the domains grow to favour orientation with the applied field. This saturates when saturation polarisation is reached. When the external field is removed most domains retain the reorientation. Therefore, there is hysteresis in the behaviour of the polarisation to an external field. As the polarisation is proportional to charge, the 'apparent' capacitance of the ferroelectric material can be electrically altered [143]. The displacement current through a ferroelectric capacitor has essentially two parts. Firstly, a linear component which is due to the charging of the electrodes to a sufficient voltage for the domains to begin to reorientate. Secondly, a nonlinear term due to the reorientation of the molecules to the external field. Therefore, there is an observed difference in the current between a switching and a non-switching domain. This interpretation of the current response in FLC material in terms of a ferroelectric capacitor model is an active field of research. But, there are many complicating factors in such investigations. These include the dielectric anisotropy, surface effects, non-uniform director structures and electrical conductivity (usually caused by ionic impurities). From the basic dielectric relations, investigation into FLC characteristics can be investigated.

$$\mathbf{D} = \epsilon_o \mathbf{E} + \mathbf{P} \qquad (A.5)$$

Where $\mathbf{D}$ is the electric displacement vector, $\mathbf{E}$ is the electric field vector ϵ_o is the permittivity of free space and $\mathbf{P}$ is the polarisation vector. The electric field vector is a measure of the local field due to all charges, both free and bound. The electric displacement vector is only a measure of free charges. The polarisation vector measures the polarisation charges and can have several contributions such as the dielectric polarisation for induced dipole moments, from bulk charges moving in the field and injected surface charges at the electrodes [54]. In a simplified ferroelectric capacitor, the polarisation P is proportional to the electric field E.

$$\mathbf{P} = \chi \epsilon_o \mathbf{E} \qquad (A.6)$$

where χ is the dielectric susceptibility. When a large field is applied, all domains orientate favourably with the field direction. When these processes have ceased the material has reached

the saturation polarisation which can be assumed for simplicity to be the spontaneous polarisation P_s. This is certainly true of large P_s ferroelectric liquid crystal materials. Since the polarisation is proportional to charge:

$$P = \frac{Q}{A} = \frac{1}{A} \int i \, dt \tag{A.7}$$

where A is the area of the material, Q is the charge and i is the current. Thus, by integrating the current, one can measure the polarisation.

Difficulties in experimental verification of such relations are due to the simultaneous presence of both the strong non-linear dielectric and ferroelectric polarisation responses. A review of these experimental investigations can be found in [54]. Numerous theoretical techniques can be employed to investigate the properties of FLC devices. None of these models have been fully completed [54].

It is hoped that some form of unification of these approaches can be found. But perhaps a description of FLC devices considering surface, electric field, elastic and viscous effects will result in a too complicated model to be truly useful.

Appendix B

Cell Fabrication Details

This is a discussion of the current fabrication techniques used for FLC device construction. Most of the proceedures are performed in the Clean Room (2314) in the AppliedOpticsGroup, Department of Physics, University of Edinburgh. All applicable options will be presented as well as preferred proceedure. Thepreferredproceedure is presented first in each section.

B.1 ITO Coated Glass

Indium-Tin Oxide is a transparent conducting thin film which is deposited on glass substrates to provide an electrode for the FLC device. The glass substrates are used for either both bounding plates in an FLC test cell or as the top cover glass for VLSI backplane SLM devices. The glass should have the property of being optically flat and of high quality. The ITO should have the property of being of a high quality, uniform, inert, strong, with a good transmission and low resistance. The ITO is usually coated with photoresist for protection during dicing to obtain required sizes.

- Hoya[†]supplied ITO coated optical flats with thickness 1.1 mm. This glass has provided the best ITO quality used so far and the relative thinness of the glass produces SLM devices which allow closer positioning of optics.

- Optical flats of a higher flatness were obtained, but the glass was much thicker (6mm), producing cubes when diced-up. The ITO quality is also poorer than that supplied by

† Hoya Europe B.V., Bilton House, 54/ 58 Uxbridge Road, London W5 2ST.

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Hoya. Although these cubes are easier to handle in the fabrication steps, the Hoya glass is to be prefered.

- Facilities exist in the Physics Department Techniques Laboratory for the deposition of ITO films on substrates. This facility is not in use continually and although great care is taken, lower quality films are produced. The resistivity tends to be higher, the transmission is lower and the films are not as robust as those obtained commercially. Nevertheless, this ITO has been used successfully in nematic LC device fabrication. This facility is most useful for patterned LC electrodes.

B.2   Substrate Cleaning

This is perhaps the most crucial step in FLC device fabrication and no corners must be cut. As much as possible these proceedures must be performed in the clean room. Only when certain chemical substances used are considered unfit to use in the clean room does this not apply. Whenever possible, cleaned substrates should be kept 'wet', i.e. stored in a solvent or deionised water, until they are required. Any substrate left out in air, even in the clean room, should be considered contaminated. Ideally, the subtrates used in SLM device construction should be clean from their initial fabrication. Do not assume this. Treat all incoming substrates as contaminated. The easiest technique for the removal of the final solvent or deionised water from the substrate for use is the ionised/filtered nitrogen gun. The liquid should be blown forcefully from the substrate without being allowed to evaporate or splash back. For large substrates this is not so easy and high speed rotation on the spinner should produce the same result. If glass is clean, deionised water should remain 'sheeted' over the entire surface. All beakers, tweezers and containers should be thoroughly cleaned. Floroware beakers, tweezers and containers are recommended for clean room use. The fume cupboards must be used for all solvents or otherwise dangerous substances. **Great care must be applied when using dangerous substances to avoid accidental spillage, bodily contact or fire.**

- One cleaning method involves only the use of organic solvents. The first stage involves the use of 1.1.1-trichloroethane (tric) which has been phased out of use in the E.E.C. due to the damage it causes to the environment. A substitute is currently being sought.

  1. The sample is placed in a beaker of tric and given ultrasonic treatment in the ultrasonic bath for a few minutes.

  2. The sample is then transfered to a beaker containing electronic grade acetone and the ultrasonic treatment is repeated.

3. The sample is then transfered to a beaker containing electronic grade isopropyl alchohol (IPA) and the ultrasonic treatment is repeated.

4. The sample is finally transfered to beaker or vial of IPA for storage.

5. The solvent is blown off with the ionised/filtered nitrogen source or spinner for use.

6. The substrate is examined under the microscope for any remaining contamination. If any remains, the sample is either discarded or taken through the process again from step 1.

- A number of useful cleaning techniques using a variety of inorganic substances are applicable. The techniques usually involve dipping the substrates in the inorganic and then rinsing and storing in deionised water. The inorganics are used to destroy organic contaminants on the substrate. Useful **substances** include Fuming Nitric Acid, Hydrogen Peroxide and mixtures of Concentrated Sulphuric and Nitric Acids. In general, these substances do not affect silicon circuitry if used for short periods. The effect on ITO films is unknown at present. Another option is 'etching' the substrate (glass) with Hydrofluoric acid.

- There are commercially available cleaning agents, but they seem to involve the chemicals named above in nice packaging. Decon 90 is a popular variety.

A number of other options are open for substrate cleaning. Distilling apparatus can be used to wash substrates in solvent vapour. Cleaning acrylic polymers can be used to paint onto the substrate, allowed to dry and then peeled from the surface, cleaning in the process. In the authors personal experience the polymer technique is notsatisfactoryand may indeed damage delicate surfaces. In the evaporator, under moderate pressure, a plasma source can allow ion bombardment onto substrates for molecular level cleaning.

B.3   Contacts to ITO

It is usual to make a metal contact from the ITO, around to the side of the glass to allow electrical connection to be made for the front electrode in SLM devcies. Aluminiumwas used due to the ease of depostion, although other metals can be used. Most of the ITO is masked with photoresist or an aluminium plate mask, exposing areas on the ITO and edge of the glass to be coated. The substrate is then placed in the evaporator at an angle to allow the evaporating aluminium access to both the ITO and edge of the glass. Aluminium wire is placed on the filament, where a low tension current can heat it under vacuum. The evaporator is taken to a

low pressure and then approximately 60 nm of aluminium is evaporated for a good contact. After cell construction electrical connection can then be made to the aluminium at the side of the glass by either bonding wire, conducting glue or conducting paint.

B.4   Alignment Layers

As has previously been discussed, the alignment layers are of utmost imporance to the alignment of the FLC molecules. A number of alignment layer options have already been discussed. The techniques for applying these will be discussed at length.

- **Oblique evaporation of oxide:** This is probably the most useful technique for VLSI silicon backplane SLM devices. It is probably the most repeatable option and will cause no damage to the silicon circuitry. The cleaned substrates are placed in the evaporator at an angle to the SiO_x source. The evaporation angle has been discussed (section 3.3.2). The chamber is evacuated and ion bombardment cleaning can be applied. At 10^{-5} Torr the source is slowly heated to obtain approximately 0.1 nm per second on the monitor. The oxide is deposited to the required height and then left for a short period to cool. As the surface is so delicate it is advisable to use the substrates in the next processing step immediately.

- **Rubbed polymers:** This is a not so repeatable technique for FLC alignment layer formation. The polymer, suspended in a solvent, is spun onto the substrate and the solvent is allowed to evaporate. The substrate is then baked to solidify the polymer. The substrate is unidirectionally rubbed with a lens tissue to obtain the microrelief structure. This can be improved by the application of a roller system to give a more repeatable rubbing.

- **Etched structures:** Alignment layers can be etched into material deposited on the surface or into the substrate features themselves. This would normally involve producing a photolithographic mask of the required relief structure. Photoresist would be spun onto the substrate and exposed through the mask. The patterned photoresist can then be used as the alignment layer or to allow etching of the substrate beneath, before removal. This is really part of SLM backplane post-processing techniques, but can equally apply to the generation of reproducable and quantifiable aligning structures.

B.5   Spacer Layers

Spacer layers are required to separate either the bounding plates of a test cell, or the front electrode from the VLSI silicon backplane mirrors. For reflecting FLC devices a separation of either $1\mu m$ or $3\mu m$ is required. For transmissive test cells it is not necessarily so important as long as the bounding plates are separated by more than $2\mu m$.

Polymer spacer balls or rods can be applied to one of the substrates. It is not desirable to have these over the active area of the device as they affect the FLC alignment. Usually, they can be suspended in the glue which is used to hold the two substrates together. Spinning techniques can be used to place the balls or rods at the edge of the substrate, but they are harmful if allowed into the atmosphere. $3\mu m$ spacer balls and $1.7\mu m$ rods are available for fabricating FLC devices. There are $9\mu m$ balls available if nematic devices are required.

With an appropriate mask, SiO_x pillars can be evaporated onto a substrate in a similar manner to the alignment layers. The evaporation takes considerably longer and the pillars do not seem to be very robust at thicknesses over $1\mu m$.

There are other methods to achieve the spacing between the two electrodes in FLC devcies. One such method uses the circuit structures on the silicon chip backplane. In the design of the device, isolated structures can be designed around the edge of the array to be $1\mu m$ above the modulation mirrors. Photoresist pillars can also be fabricated on the glass structures by photolithographic processes. An alternative technique has been suggested where accurate blocks of adhesive are deposited by screen printing processes and used as the spacer layer. Some 'older' methods for producing the correct spacing have involved mechanically squeezing a 'blob' of FLC material until it was the required depth.

B.6   Mechanical Construction of the Cell

This involves the construction of all the components of the the test cell or SLM device. The glue writing system, designed by M.W.G.Snook, has proved invaluable in this operation.

For SLM devices, the position of the glass on the SLM backplane is crucial. Small dots ($< 1mm^2$) of the UV curing glue is written with the glue gun onto the very corners of the glass. The glass is placed in one half of the jig and the SLM backplane in the other. The two halfs of the jig are

brought together, which positions the glass onto the backplane. Point pressure is applied to the glass while UV light is shone upon the glue to cure it. This technique makes most use of the glue writing system. One substrate is held on the platform by a vacuum and glue written as required. The other substrate is then positioned on top of the first with the positioning apparatus on the glue system. A clean plastic sheet is then placed over the substrates and the air evacuated. The vacuum produced, causes the sheet to give a uniform pressure onto the substrates while the glue is cured with UV light.

B.7   FLC Filling

FLC material at room temperature, looks like a very viscous paste. It is therefore necessary to heat the material until it becomes an isotropic liquid for it to flow into any cells. To out-gas the material and cell, and to help the filling process, it has been found necessary to fill the cell under a high vacuum. Therefore a hot-plate system is used inside a vacuum chamber to meet these requirements. Different FLC materials have differing isotropic phase transitions, but most will have have attained the liquid state by $120^\circ C$. The proceedure is as follows:

1. A small amount of FLC material is placed at an open edge of the cell with a thoroughly cleaned implement.

2. The cell is placed on the hot plate.

3. The evacuation of the chamber is started and the plate is allowed to heat up to allow the FLC to out-gas. The FLC should start foaming up.

4. At $120^\circ C$ the current is switched off and pressure allowed to drop in the chamber. The FLC is left for an hour to out-gas.

5. The plate is then reheated to 120° and allowed to stabilise for a few minutes.

6. The chamber is then rapidly brought to atmospheric pressure to aid complete filling of the cell by the isotropic FLC through capillary action.

7. The cell is then left to slowly cool to room temperature before removal.

8. Excess FLC material is then removed from the outside of the cell and the hot plate with acetone.

For nematic LCs no heating is required as the cell fills by capillary action as the LC has low viscocity, but the out-gassing procedure is advisable.

B.8 Storage of FLCs and Sundry Comments

The FLC material should avoid any contamination or moisture, as they will unduly affect the cells obtained. The FLC material should be kept in sealed containers in the dehumidifier, in the clean room. All apparatus, evaporators, equipment etc., should be cleaned after use. This should minimise any contamination in future cell fabrication. Glue needles and FLC implements should be discarded after use. The physiological effects of skin contact with FLC material is unknown at present. All exposure should be avoided and the safety guidelines followed.

Appendix C

Planarisation Proceedure

The planarisation of the 176^2 SLM was performed by A.O'Hara and is described in detail here. The arguments for the use of planarisation when fabricating SLMs are compelling, and much progress has been made towards realising planarisation as a practical post processing step. The planarisation process is an additional procedure carried out on completed wafers supplied by AMS. Since this is an experimental proceedure, the design of top level metal and the vias is simple and conservative to make the processing as robust as possible to complement the high yield of the AMS wafers. The sequence of processing steps which constitute the planarisation procedure is predominantly composed of standard MOS processes. The planarisation procedure is described in detail below (A.O'Hara):

- At the first stage an initial thick layer ($\sim 4\mu$m) of SiO_2 is deposited using Electron Cyclotron Resonance Plasma Enhanced Chemical Vapour Deposition (ECR-PECVD) by an Oxford Plasma Technology system. ECR systems are primarily employed in etching techniques and as yet is still not a standard MOS processing method for deposition. The ECR system deposits the SiO_2 at low temperature, therefore hillocks which could cause shorts between the interlevel metals are not produced during this procedure.

- Chemical-Mechanical Polishing(CMP) is another non-standard MOS process but is now being used in the fabrication of leading edge technology devices. It has been used to planarise the wafers following trench isolation and trench capacitor filling early in the microfabrication sequence. It is now being applied to the planarisation of interlevel dielectrics in multi-level metallisation schemes. Following SiO_2 deposition the variation of the surface topography of the chip is $\sim 1.5\mu$m. We have used a Logitech PS2000 polishing system to reduce the local surface variation to less than $60nm$ onto which the metal can

be deposited producing high quality mirrors.

- The photolithography stage entails the deposition of photoresist, exposure, and development. At Edinburgh the photolithography equipment is set up to deal with 3" wafers and cannot be easily adapted for 4". To overcome this problem work was carried out to cut the wafer from 4" to 3". Although successful, this procedure was deemed to be too fragile a process for long term inclusion into the fabrication sequences and also too wasteful on chips on the wafer, removing approximately half. The primary system is the Optimetrix stepper which requires the removal of alignment pins necessary for automatic loading and alignment. Now the 4" wafers must be loaded by hand with the reduced precision on global alignment that this incurs. This problem will need to be overcome to optimise the structure of the multi-level metal scheme.

- Via holes are etched in the SiO_2 to provide the connection between metal layers and is performed in a Plasmatherm etcher which can accommodate 4" wafers.

- The top level aluminium/silicon alloy is deposited in a Balzers sputter deposition system. The jigs supplied with the system are designed to house 3" wafers therefore the 4" wafers require to be clamped into position.

- Another photolith stage and a final metal etch.

The planarisation procedure described above has been successfully applied to working electrically addressed SLMs ensuring high optical quality mirrors. For the 176^2 SLM, the pixel mirror fill factor has been considerably increased from $\approx 30\%$ to $\approx 80\%$ and the mirror flatness reduced to $< 10nm$.

Appendix D

Hadamard Transform Simulation

In chapter 6 we discussed how the the Hadamard transform could be implemented successfully using optical techniques. But what useful procedures can the transform be applied to? This is a short simulation study of some of the potential applications of the Hadamard transform.

D.1 Simulation of the Hadamard Transform

Simulation of the Hadamard transform can readily be performed on digital computer. A useful investigation would examine relatively large image arrays, sizes such as 256×256 or 512×512. Unfortunately such calculations of the Hadamard transform are computationally intensive. It was therefore deemed necessary to employ a Connection Machine for the swift calculation of the transform. This computational calculation of the transform has allowed a preliminary investigation into its image processing capabilities. This work is ongoing but sufficiently mature to indicate the potential usefulness of the Hadamard transform. Image compression has been studied extensively [123], but more general image processing operations are also possible.

D.2 Simulation Experiments

The route to calculating the transform was different to that employed in the optical implementation. The unitary operators $[U]$ and $[V]$, ($[U]$ and $[V]$ are the same for the Hadamard transform) for the image array of interest, were calculted in the iterative manner described in 6.1.3. These allow the transform to be calculated by two matrix multiplications. On the Connection Machine, a parallel matrix multiplcation routine was
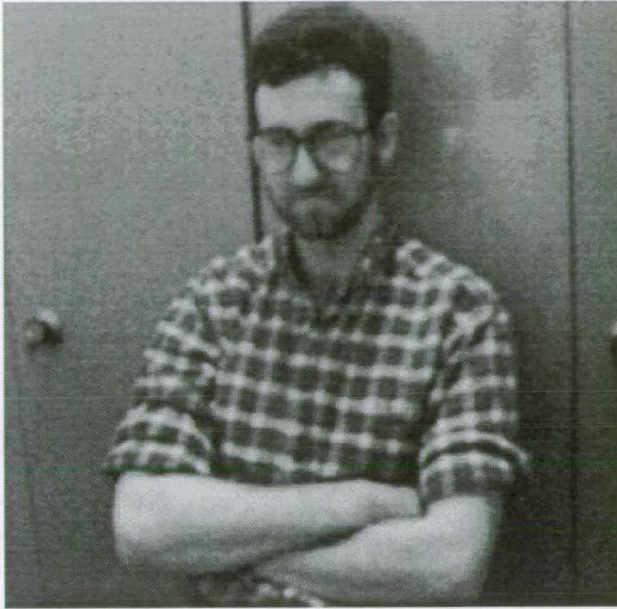
Figure D.1: The input test pattern 'steve'.

employed to perform these calculations, with floating point accuracy, on 256×256 8-bit test images. The resulting transform coefficients were then procesed to achieve the desired function and then inverse transformed by a similar method. The processed images were then converted to an 8-bit representation for visual examination. Transform and inverse transform usually took an average of 10 seconds to perform on the Connection Machine, but over 30 hours on a Sun workstation (Sparc 2). Figure D.1 shows the input test pattern used in the experiments. It includes human face information and regular patterning (the shirt), to give variety of information types.

D.3   Simulation Results

By selection of certain of the Hadamard transform coeffiecients it is possible to perform frequency filtering such as edge-enhancement, bandpass-filtering or generalised spectrum analysing. Frequency based pattern recognition and feature extraction are also possible. An example of edge-enhancement through a high-pass filter was performed on the test image. The lowest 50 percent of the Hadamard transform frequency coefficients were discarded by a filtering operation in the transform plane and the result on inverse transformation is shown in figure D.2. This has resulted in a differentiation operation being performed on the test image and a very useful representation for further image processing.

Figure D.2: The high pass filtering resulting in edge-enhancement.

To give an indication of image compression, the transform coefficients were thresholded around their average value (ignoring the d.c. component) to values +1 and -1. This reduced the 256×256 8-bit input data to a 256×256 1-bit representation i.e. compression to $\approx 11\%$. The reconstuction on inverse transformation of this particularly crude technique is shown in figure D.3. Much more information is retained than simply thresholding the original image. Much better approaches to compression include an ordering of the coefficients, in terms of their importance to the reconstruction, and then neglecting the least significant. Other more novel techniques for processing the transform coefficients have also been suggested [123].

Figure D.4 shows the filtering out of all of the diagonal transform coefficients. Such techniques can be applied to identify horizontal and vertical lines, a useful operation for low level vision tasks. Another potential use of the Hadamard transform implementation is in encryptology. If the Hadamard transform coefficients are reordered then the information is effectively encrypted, unless one were to know the correct ordering. To illustrate this, the picture of the Mona Lisa in figure D.5, was used to re-order the Hadamard transform coefficients. The value z of the nth pixel was used to swap the nth Hadamard transform coefficient of the test image with the $(n + z)^{th}$. Therefore, the Mona Lisa was used as an encryption key for the reordering of the coefficients. With the key image, the coefficients can be returned to their original ordering i.e. decrypted. Figure D.6 shows the test image encrpyted with figure D.5 used as the key. Reconstruction of an encrypted image takes the same time as reconstruction of a non-encrypted image. This is because only the order

Figure D.3: reducing the frequency information to only one bit

Figure D.4: The result of retaining merely the horizontal and vertical frequency components.
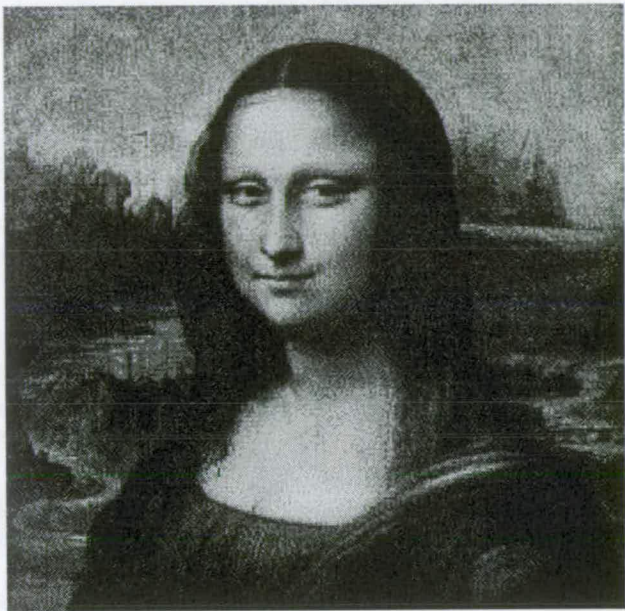
Figure D.5: The image used to encript the transform coefficients.
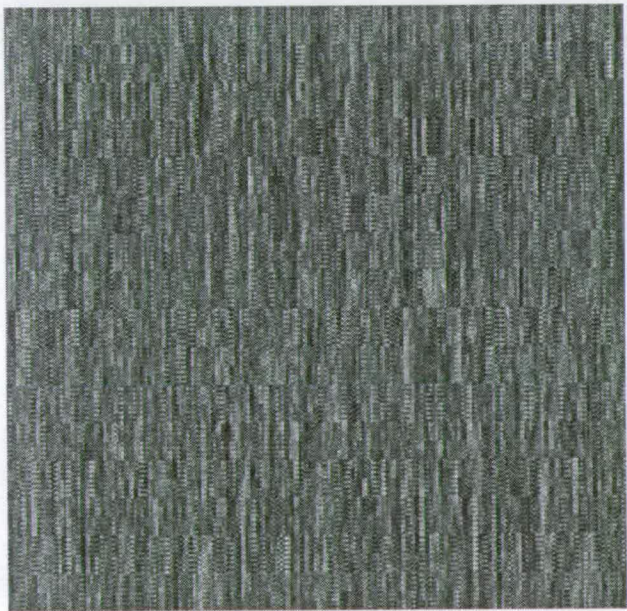
Figure D.6: The resulting encripted image.

of the basis function operations is different.

This short discussion has hopefully given a flavour of the useful applications of implementations of the Hadamard transform.

D.4 Comparisons of Images

The Signal-to-Noise (SNR) ratio is a numerical value assigned to data to give an indication of the extent of corruption by noise. This is only usefully defined for the case of image independent additive noise. In image compression situations the level of corruption of the data may be related to the original image. This means that the SNR is not a useful measure of the effects of image compression. The normalised correlation gives a more useful measure of the similarity (or dissimilarity) of images. The normalised correlation r is defined as:

$$r = \frac{<(fg- <f><g>)>}{[<|f-<f>|^2 ><|g-<g>|^2 >]^{\frac{1}{2}}}$$ (D.1)

where f is the original image and g is the corrupted image and $<>$ denotes a normalised summation. This relation can be used to compare images which have been compressed by various techniques and gives a quality value for useful comparison. Further simulation work should use this comparison to fully investigate potential Hadamard transform applications.

D.5 Summary

These preliminary studies and simulation results have shown that the Hadamard transform is an extremely useful image procesing tool. Further investigation into fast optical implementation of the transform and other related potential transforms has been justified.

Appendix E

Fourier Transforms of SLMs

As has been described (section 1.1.1), a simple lens can act as a Fourier transforming element [3]. If coherently illuminated, the Fourier transform of an input object at the first focal plane of the lens, is obtained at the second focal plane. This is a very powerful processing operation. The actual Fourier transform is never actually observable at this plane, as on observation the amplitudes are squared to form intensities, and all phase information is lost. The amplitudes can be manipulated before observation as in a coherent optical processor (section 1.1.1). Consider an idealised SLM device (no modulation). We have an array of $N \times N$ pixels, seperated by distance d with a rectangular mirror size a,b and described by the function $p(x, y)$. Figure E.1 illustrates the Fourier transform of the device without resorting to the mathematics details. The situation before a pattern is displayed on the SLM is represented at the top of the figure, where the SLM can be described by a square aperture function, multiplied by an infinite two dimensional array of delta functions, convolved with the pixel function. Due to the seperable nature of the Fourier transform, each function can be transformed individually, only the recombination of them is different. Multiplication becomes convolution in the Fourier plane and convolution becomes multiplication in the Fourier plane. In general, small functions become large in the Fourier plane and large funtions become small. The Fourier transform of the square aperture has a sinc function nature, which is convolved with the transform of the delta functions which is just another set of delta functions with a different spacing. All of this is multiplied by the transform of the pixel function which is a sinc function in nature. A number of important points concerning the Fourier plane information can be gleaned from this rather qualitative arguement:

- **Resolution:** The size of the aperture in the input plane decides the maximum spatial frequencies distinguishable in the Fourier plane. They are given by $w_o = \frac{Nd}{\lambda f}$ where λ is the wavelength of light and f is the focal length of the lens used for the transform.

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Infinite array of deltas   Aperture Fn.   Pattern on SLM   Pixel Fn p(x,y)
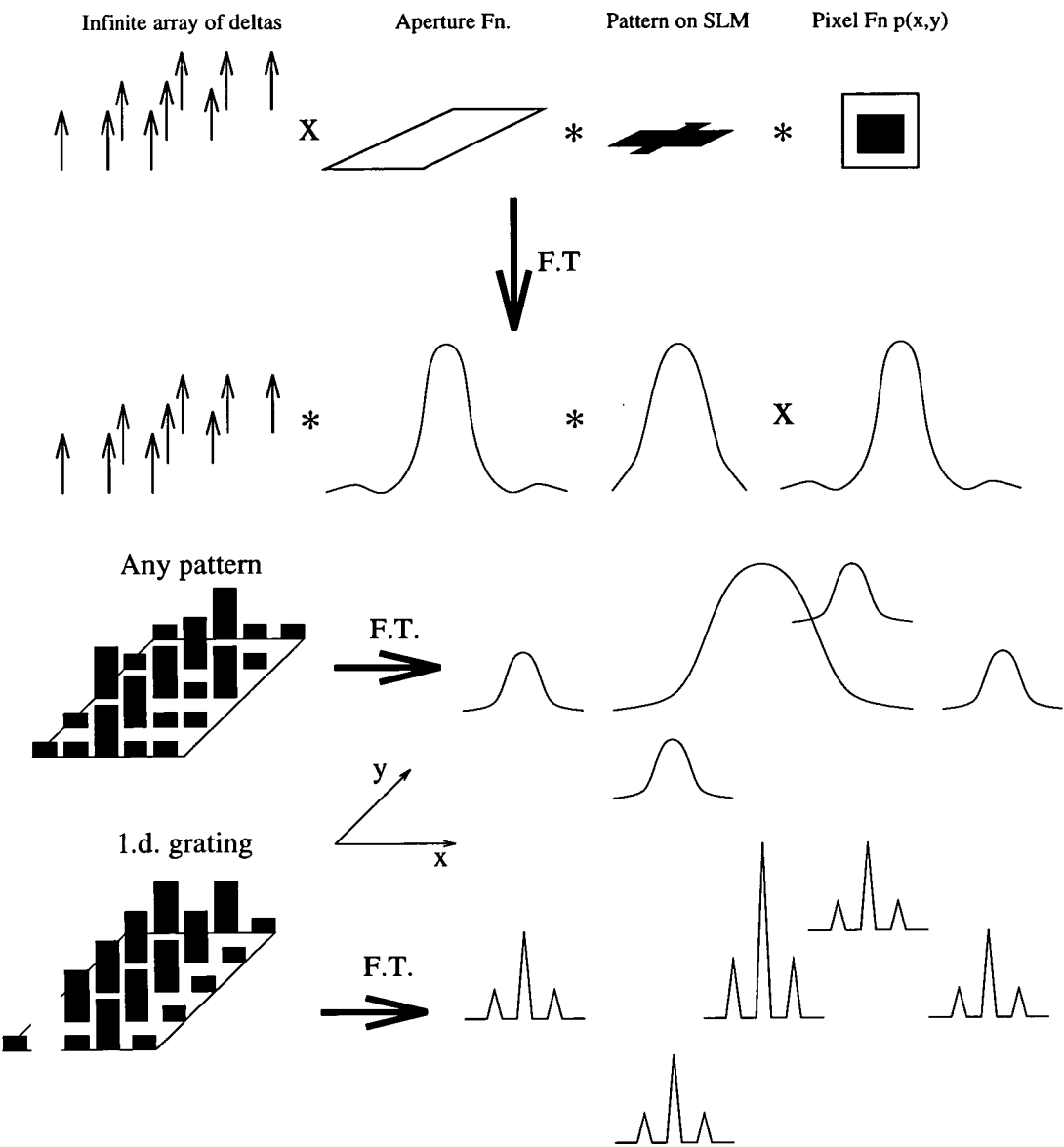
Figure E.1: The Fourier transform of a pixellated SLM.
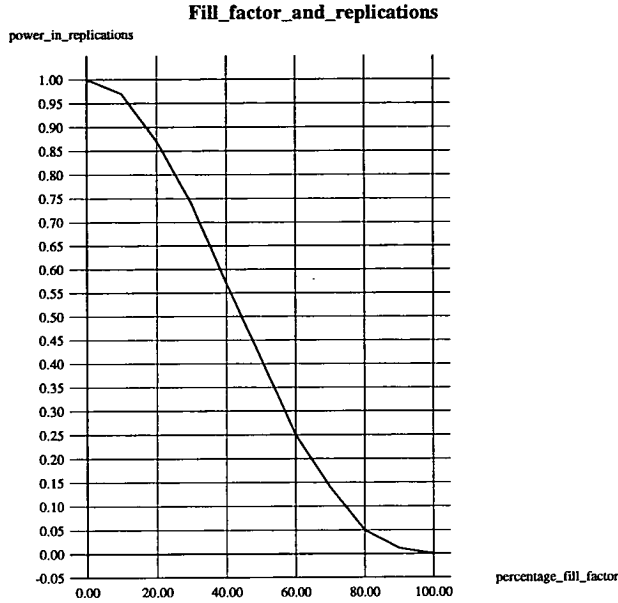
Figure E.2: Power in the first replicated order

- **Replication:** Due to the pixellated nature of the SLM an infinite number of replicated orders are produced, this results from the transform of the delta functions. The replications are scaled by the transform of the pixel function. As the pixel fill factor approaches 100% i.e. $a, b \rightarrow d$, the replications reduce to zero. But, with a finite fill factor i.e. $a, b < d$ the replications are scaled by the pixel function transform. For a rectangular pixel function this scaling take the form of a multiplication with the function $\frac{\sin(\pi a x)}{\pi a x} \frac{\sin(\pi b x)}{\pi b x}$. The replications are at positions $x_n = \frac{m}{d}, y_n = \frac{n}{d}$, for $m, n = 0, \pm 1, \pm 2, \ldots$.

- **Noise:** Any detail smaller than the pixel dimension d such as circuitry, defects and bumps on the mirror surface will diffract from the replications into other orders. This can cause noise in the zeroth order.

E.1 Analytical Calculations on the 176^2 SLM

The discussion above allows some preliminary calculations to be performed, before simulation and experiment, to assess the potential characteristics of the transform of the device [1]. The results of these describe the operation of the device before we add in phase or amplitude modulation in simulation. They also allow the dimensions of the various parameters to be calculated with regard to real optical systems. This is a very useful initial step before moving to optical
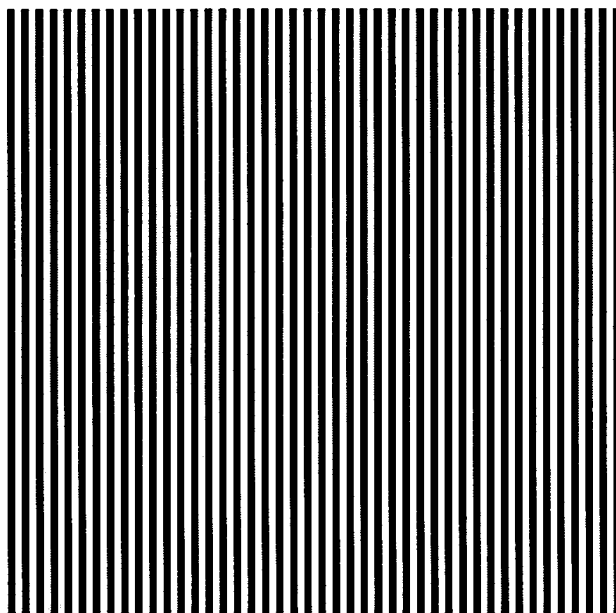
Figure E.3: The grating pattern.

experiments. For example, the resolution of the resulting Fourier transform pattern can be obtained from the SLM aperture size, the lens focal length and the wavelength of laser used. This allows the matching of any viewing CCD camera pixel pitch to system parameters (section 7.2).

Due to the pixellated nature of the SLM an infinite number of replicated orders are produced. These replications are scaled by the transform of the pixel function. As the pixel fill factor approaches 100%, the replications reduce to zero. Figure E.2 shows a graph of pixel fill factor against the analytically calculated power in the first order replication (the scaling due to the pixel function). Any detail smaller than the pixel dimension such as circuitry, defects and bumps on the mirror surface will diffract from the replications into other orders. This can cause noise in the zeroth order.

E.2   Simulation

To assess the potential improvement for CGH interconnects through increasing the fill factor, some simulations have been performed on the 176^2 SLM. Unplanarised, the 176^2 has a fill factor of $\approx 30\%$. When planarised, the fill factor is increased to $\approx 80\%$. The improvement due to this application as an adaptive phase element, in a Fourier transforming system, can be examined by

Figure E.4: The grating padded with zeros.

simulation. As in section 7.2, a simple one-dimensional grating pattern is useful for this purpose. Figure E.3 shows a one-dimensional grating pattern, with a 2 pixel period, for the 176^2. Each SLM pixel is represented by 4 simulation pixel values. Therefore 25%, 50%, 75% and 100% fill factors can be approximated. A 100% fill factor 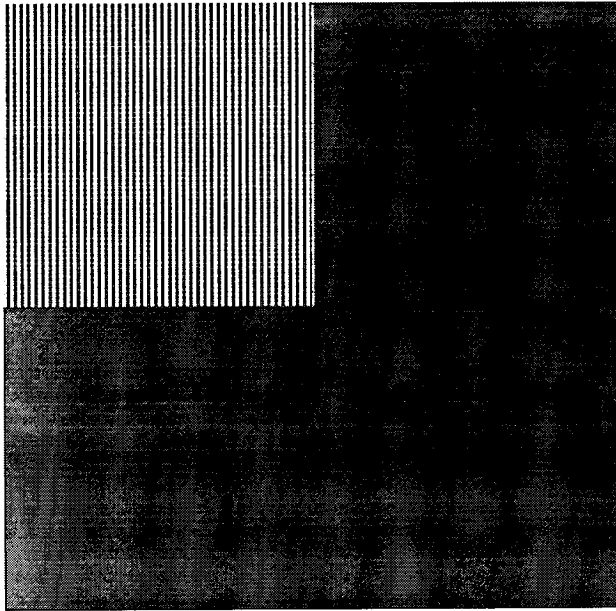is depicted in figure E.3. A standard technique in digital processing is to pad the data to be transformed with zeros. This results in a higher resolution in the Fourier domain i.e. spikes become more like sinc functions than merely single pixel columns. This is shown is figure E.4, where the data to be transformed has been increased fourfold, with zeros. The data depicted in the figure can have a complex number representation, so for the padding (grey area) the value is zero, for the zero phase modulation (black area) the value is +1, and for π phase modulation (white area) the value is -1. The Fourier transform experiments were performed using a C program written by the author which utilises routines written by W.J.Hossack.

Figure E.5 shows the central diffracted pattern obtained after Fourier transformation and squaring of a set of data. The data is squared to obtain an intensity distribution, as would be observed by the eye or a camera. In this example, this is the result of a simulation of a binary phase 176^2 pixellated device with a 25% fill factor. The d.c. term (central peak) is very prominant in this case. The replications have not been included for ease of presentation. As a figure of merit, the diffracted peaks were compared to the d.c. peak. The intensity of the peaks was measured from the Full Width at Half Maximum (FWHM), and the zeroth order (ignoring replication) diffraction efficiency (section 7.2, ZODE) was defined as **intensity in the diffracted**

'grate1ftcrop.gnu' ——
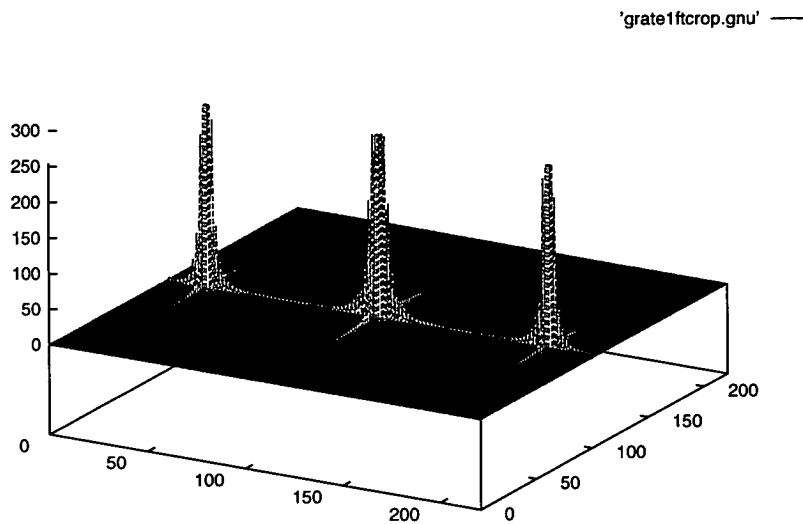
Figure E.5: A simulation of the central diffraction pattern.
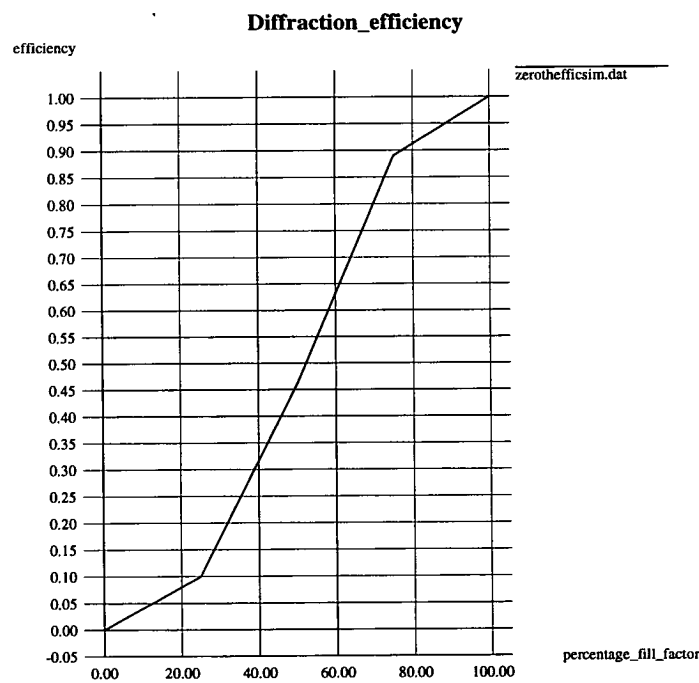
Figure E.6: Diffraction efficiency in zeroth order.

'j8na2ftcrop.gnu' ——
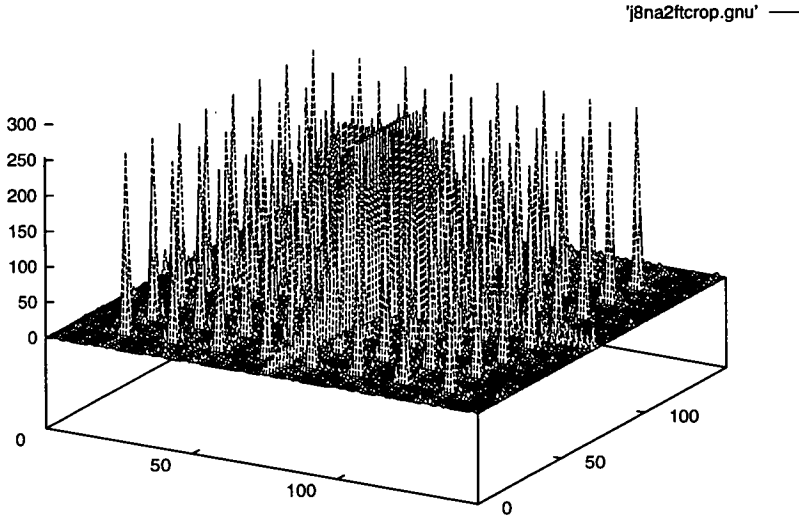
Figure E.7: The resulting hologram pattern.

peaks/intensity in all of the peaks in the zeroth order. A graph of these values for the simulated fill factors is shown in figure E.6. As one might expect, at 0% fill factor, the efficiency is zero, and at 100%, the effieciency is 100% (i.e. no d.c. peak).

E.3 CGHs on SLMs simulations

CGH display on the 176^2 SLM can also be examined through similar simulation. Figure 7.5, shows the CGH pattern used in section 7.3 which results in an 8 × 8 fanout array on transformation. This was simulated as a 176^2 binary phase pattern with 25% fill factor (zero padding was included). The resulting observable Fourier transform is shown in figure E.7. The zeroth order diffraction efficiency measured in in this case was 5% and the peaks varied by as much as $\approx 10\%$. This can be compared to the measured optical values in section 7.3.

E.4 Summary

This has been a short introduction to the more relevant simulation work for this study. This has allowed an investigation into the effect of pixellation, and comparisons between simulation and optical experimental results. The figures of merit for the simulation work give an upper limit to that expected from the real experiments. This is strong evidence that factors other than merely the pixel fill-factor have an important role in determining the resulting Fourier transform characterisitics obtained when using FLC/SLMs. The most obvious conclusion from all of this work is that that a high pixel fill factor is crucial if such devices are to be used successfully as phase elements in real systems. A large d.c. term and significant replications result in a reduction in efficiency and lower signal-to-noise.

Appendix F

Joint Transform Correlation

Coherent optical processing was introduced in section 1.1.1. . Joint Transform Correlation (JTC) is one technique which can be applied for pattern recognition processing [144]. Figure F.1 shows the operation of the JTC. An input scene and a reference pattern are Fourier transformed and thetransformis squared. The squaring of the transform produces the power spectrum of the input and reference patterns. When inverse transformed, correlation peaks are produced. These correlation terms correspond to the autocorrelation of the input and the reference on-axis, and two crosscorrelation terms off-axis representing the level of correlation between the input scene and reference. The height of the peak gives a value of similarity and the peak location gives an indication of position.

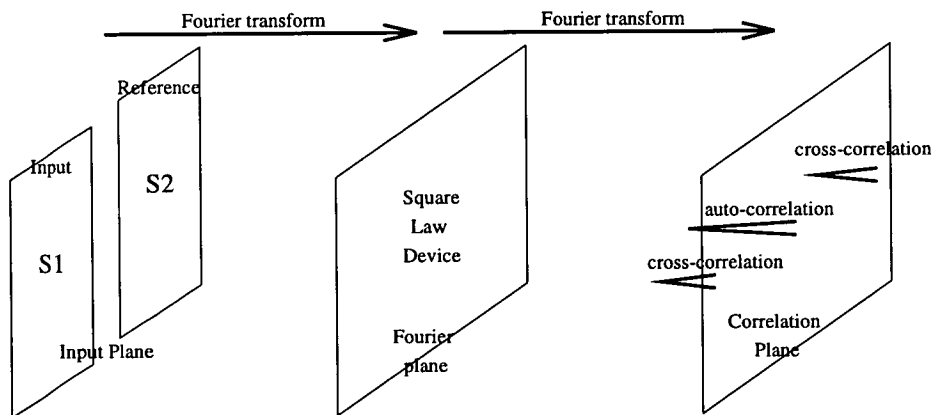Joint Transform Correlation (JTC) Techniques were widely described by Javidi [145], although

Figure F.1: Joint transform correlation.

the original concept was proposed by Weaver and Goodman in 1966 [144]. The JTC differs from the more common Matched Spatial Filter (MSF) technique in that both the reference and the target scene are presented at the input plane. This overcomes some of the limitations of the MSF. The JTC is very alignment insensitive, it does not necessarily require a complex reference and is easily implemented with SLM devices. The main draw-backs of the technique are that it is not very scale, rotational or intensity invariant, and that clutter can cause serious problems. Therefore, although more robust than the MSF, the JTC is not so versatile, but is still a useful technique for certain simple recognition applications.

F.1 Theoretical Background

Assume an input plane $t(x, y)$, split into two halves $s_1(x + x_o, y)$ and $s_2(x - x_o, y)$:

$$t(x, y) = s_1(x + x_o, y) + s_2(x - x_o, y) \tag{F.1}$$

s_1 represents the input scene and s_2 represents the reference pattern. If the Fourier Transform (FT) is taken of $t(x, y)$, as the FT is commutative this can be expressed:

$$F[t(x, y)] = F[s_1(x + x_o, y)] + F[s_2(x - x_o, y)] \tag{F.2}$$

If $F[t(x, y)]$ is $T(u, v)$ and the shift theorem gives $F[s(x + k, y)]$ as $S(u, v)e^{ikw}$:

$$T(u, v) = S_1 e^{ix_o w} + S_2 e^{-ix_o w} \tag{F.3}$$

This is the representation of $t(x, y)$ in the Fourier plane. The exponential terms are phase shifts. If some square law device is employed at this plane to square the FT:

$$\mid T(u, v) \mid^2 = \mid S_1 \mid^2 + \mid S_2 \mid^2 + S_1 S_2^* + S_1^* S_2 \tag{F.4}$$

The inverse FT of the function is taken to obtain:

$$F^{-1}[\mid T(u, v) \mid^2] = R_{11}(x', y') + R_{22}(x', y') + R_{12}(x' - 2x_o, y') + R_{21}(x' + 2x_o, y') \tag{F.5}$$

where $R_{i,j}(x', y') = \int \int_{-\infty}^{+\infty} s_i(x' - x, y' - y)s_j(x', y')dx'dy'$ and $i, j = 1, 2$, which is the correlation integral. Therefore after this procedure in equation F.5, in the correlation plane one can observe two on-axis auto-correlation functions and two cross-correlation functions between the input scene and reference at $^+_- 2x_o$. Movement of the object results in a change in position of the cross-correlation peaks.

When phase patterns are used at the input plane and for power spectrum representation, a more efficient and more discriminating correlation results [145]. Thus, phase modulating SLMs can be used to efficiently implement the JTC in optical systems.
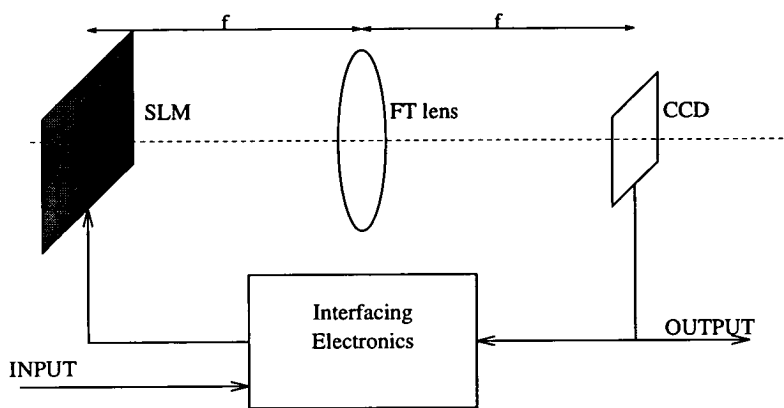
Figure F.2: A simple one lens JTC system.

F.2 JTC in optical systems

There are two main optical system configurations for performing JTC with SLMs. The first uses an SLM at the input plane to display the input scene and reference pattern. This is Fourier transformed with a lens to an OASLM which squares the amplitude signal to give an intensity distribution and thus the power spectrum. The power spectrum is transfered to the light modulating element for effective inverse transform by another lens. The correlation peaks are then available for detection at the Fourier plane of the second lens [145]. The second implementation requires only a single EASLM, a Fourier transforming lens and a CCD detector camera [146] (figure F.2). The input scene and reference are displayed initially on the EASLM and the power spectrum is obtained from the CCD detector. The power spectrum is then displayed on the EASLM for inverse transformation and the correlation peaks are generated at the CCD detector. Thus, the forward and reverse transformations are time-multiplexed through the same components, resulting in a very compact system. The main trade-off for this compactness is that the system performs the corrleation slower, dependent on the update time for the SLM and the acquisition time for the CCD camera. There is also the consideration of the peak detection required. The JTC is still a potentially powerful system and requires an EASLM device. The FLC/VLSI SLM would seem an obvious candidate.

F.3 JTC Simulations

Although time has not permitted optical experimentation with SLM devices, some simulation work has been performed. To give an indication of this, an example is presented here to more
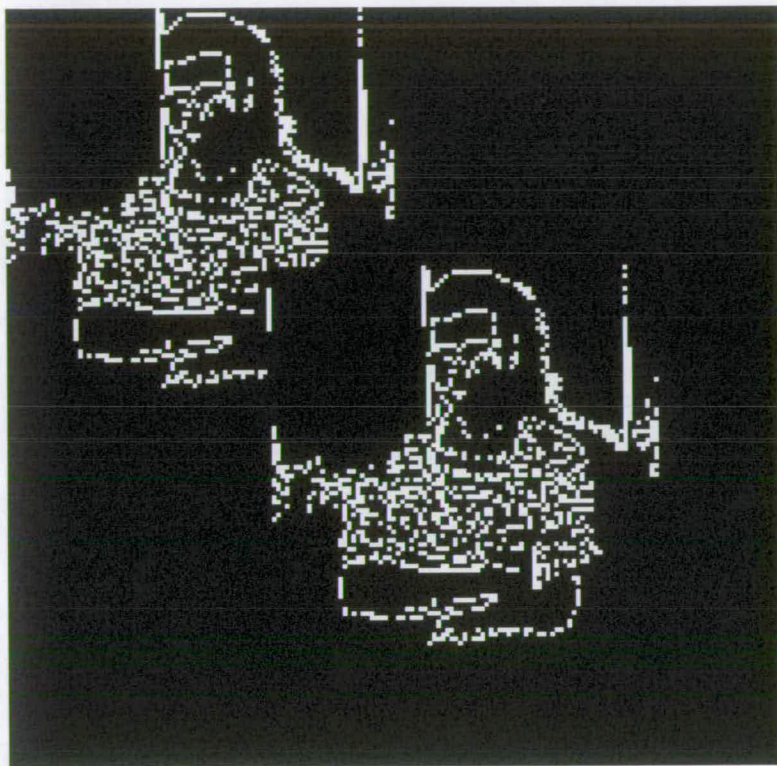
Figure F.3: A test input scene for JTC simulation.

fully illustrate the JTC. Figure F.3 shows an input test pattern to demonstrate correlation. The image on the left may be regarded as an input scene, and that on the right as a reference pattern. The patterns have been edge-enhanced and binarised, and then represented as a 176^2 binary phase (0 and π) information, with a 100% fill factor. This information was digitally Fourier transformed (see appendix E) and the data squared. Neglecting the d.c. term, the Fourier transform data was thresholded about the average to give 176^2 binary information for inverse transform. After inverse transformation, the data depicted in figure F.4 resulted. This shows a large central peak (autocorrelation) and two cross correlation peaks. Figures of merit for such results include the peak-to-noise ratio.

F.4   JTC Conclusions

Phase modulating SLM devices have a variety of important applications in information processing systems. Although the SLM characteristics currently available are somewhat limiting, some very useful applications can be demonstrated. This introduction to JTC has shown the viability

'jtcout_gnu' ——
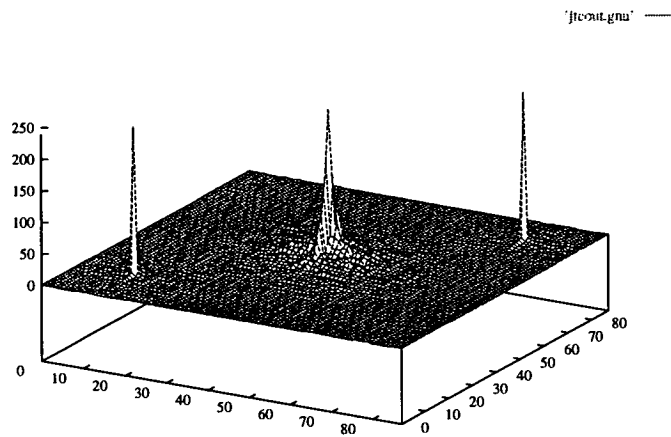
Figure F.4: The JTC of the test input scene.

of utilising SLM devices in optical implementation. In particular, binary phase SLMs look very promising.

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Time-multiplexed optical Hadamard image transforms with ferroelectric-liquid-crystal-over-silicon spatial light modulators

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The Hadamard transform is an example of a matrix transform that allows images to be represented in terms of orthogonal basis functions with binary-valued matrix elements. Such basis functions can be displayed on binary amplitude modulating ferroelectric-liquid-crystal-over-silicon spatial light modulators, permitting novel, real-time, and high-speed implementation of the transform on incoherently illuminated input scenes. An example of an optical Hadamard transform performed in real time by using a spatial light modulator is described. To show the validity of this optical decomposition, we electronically reconstruct the transformation data for comparison with the original input scene.

Image processing can often be reduced to the manipulation of large two-dimensional matrices according to the rules of linear matrix algebra.[1] In general, the unitary transform $[a]$ of matrix $[G]$ may be written as $[a] = [U]^t[G][V]$, where $[U]$ and $[V]$ are unitary operators and the superscript t denotes the transpose matrix. The inverse transform may be written in the form $[G] = [U][a][V]^t$. This can be expanded as $[G] = \sum_{i=1}^{N} \sum_{j=1}^{N} a_{ij} \mathbf{u}_i \mathbf{v}_j^t$, where $\mathbf{u}_i$ and $\mathbf{v}_j$ are the vectors made up from the i, jth columns of $[U]$ and $[V]$, respectively, and a_{ij} is the value at the ith row and the jth column of $[a]$. The outer product $\mathbf{u}_i \mathbf{v}_j^t$ may be interpreted as an image basis function so that a sum over all the combinations of outer products, weighted appropriately by the a_{ij}, reconstructs the original image $[G]$. The set of outer products that form the image basis functions can be chosen to perform a variety of transformations.[1] The Hadamard transform, the Walsh transform, and the Haar transform have binary basis functions containing 1's and −1's (additionally 0's for the Haar transform), which are particularly suited for implementation by fast-switching ferroelectric-liquid-crystal-over-silicon (FLCOS) spatial light modulators (SLM's),[2] configured as binary amplitude modulating arrays.[2] Serial electronic systems can be used to perform the simple calculations for matrix transforms, but, as the system scales up, the data manipulations become more cumbersome for serial electronics. The inherent global parallelism of optical systems can overcome such problems in the calculation of matrix image transforms. This is the main reason for investigation into optical solutions to such computational problems.

Optical systems have previously been designed around the two-dimensional Hadamard transform but, as far as we are aware, have been limited to the use of mechanical moving masks and sliding slits to generate the basis functions.[3] High-performance electronically addressed SLM's are ideal devices to display the individual basis images required for direct transformation and inverse transformation through optical multiplication and summation. A particular transform coefficient may be determined by pixelwise multiplication of the l, kth input image element of matrix $[G]$ with the corresponding l, kth binary element of the outer product expansion matrix $(\mathbf{u}_i \mathbf{v}_j^t)$, as displayed on a SLM pixel. Summation over the two-dimensional array is then performed by a lens that gathers the noncoherent light to a single photodetector with a high dynamic range to determine the value of the coefficient a_{ij}. An analog input scene may therefore be decomposed into a series of transform coefficients that are obtained by repeated optical multiplication with binary basis patterns displayed sequentially on the SLM and by electronic summation at the photodetector. An advantage of this highly useful frequency representation technique is the acceptance of an input image directly from a scene illuminated by incoherent light.

Figure 1 shows the set of 64 basis images for an 8 × 8 implementation of the Hadamard transform (white areas +1, black areas −1). The individual patterns are displayed sequentially on the SLM. Functions of increasing frequency (or, more correctly, sequency) are obtained by moving left and down in Fig. 1. The
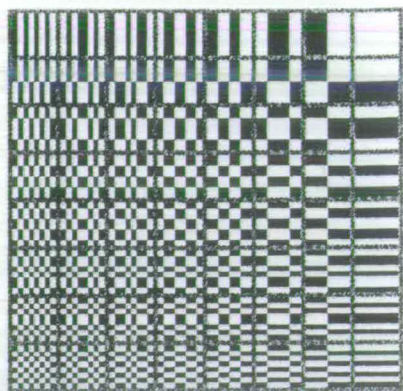
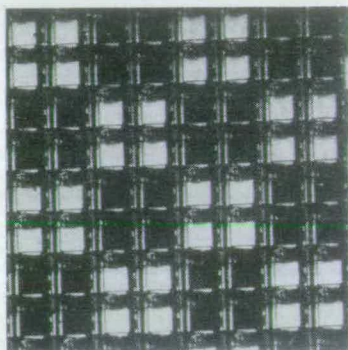Fig. 1. Hadamard transform basis functions for individual display on the SLM.

Fig. 2. Typical Hadamard transform basis function displayed on a FLCOS SLM.

Hadamard transform requires bipolar arithmetic as the basis functions are coded with +1 (white) and −1 (black) weights. Incoherently illuminated optical systems deal only with positive-valued parameters. One way of overcoming this mismatch and retaining good signal-to-noise ratio is by implementing a two-channel system: first by calculating the positive contribution and then by subtracting electronically the negative contribution, for each basis function in turn. This time-multiplexed implementation of the transform is sensitive to uniformity variations across the device but inherently insensitive to the mean device contrast as the background is subtracted out at the detector. Uniformity variations will be the limiting factor on the accuracy of the coefficients measured at the detector. This will become more important with scaled-up systems. An interesting analysis of how errors in the basis function representation on the mask correspond to coefficient accuracy in the detection plane can be found in Harwit and Sloane.[3] Positive-only versions of Hadamard basis images (called S matrices) are available,[3] which can be thought of as adding a dc bias to the functions. This would be useful for all-optical decomposition and reconstruction, but at the cost of a reduced signal-to-noise ratio. Such a loss of signal-to-noise ratio is particularly evident if low-contrast-ratio SLM devices are used to display the basis functions, which would be undesirable in the system implementation that we now describe.

The reflective SLM device used in the experiments is a FLCOS device with a static random-addressed memory backplane.[4] Such electronically addressed SLM devices have ferroelectric-liquid-crystal modulating material aligned on aluminum mirrors that are integrated into the specially designed microcircuits on the single-crystal silicon backplane.[5,6] The SLM exhibits a contrast ratio of 8:1 and a switching speed of 50 μs when operated with a 12-V power supply.[7] An example of an 8×8 Hadamard transform basis function for the coefficient a_{33}, displayed on the FLCOS SLM, is shown in Fig. 2.

The compact optical system for implementation of the Hadamard transform is shown in Fig. 3. An 8×8 test pattern, shown in Fig. 4(a), was imaged onto an 8×8 section of the FLCOS SLM device. An image of this test pattern reflected from the SLM devices configured with all pixels on is shown in Fig. 4(b), which shows the pixelation of the pattern and structure in the modulation elements. The 64 positive and 64 negative basis functions for an 8×8
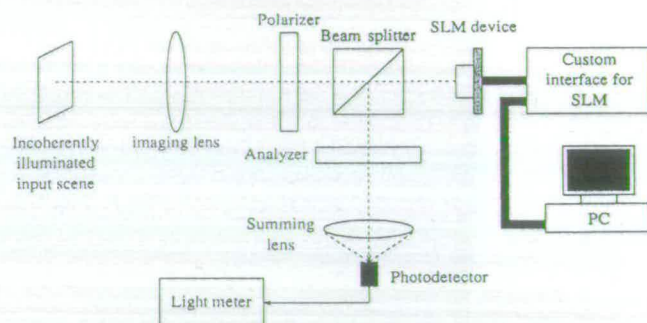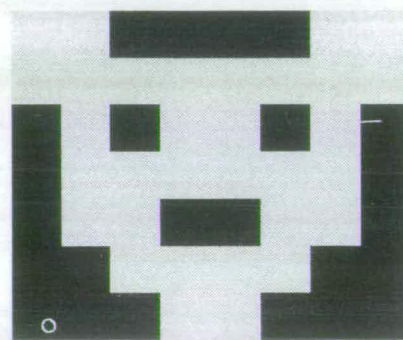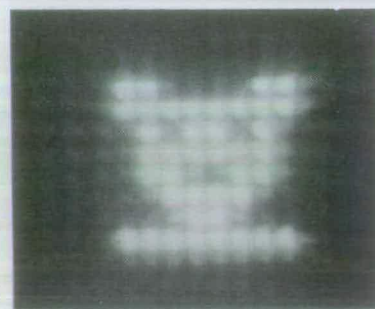

Fig. 3. Optical system used in the Hadamard transform experiments. PC, personal computer.

(a)

(b)

Fig. 4. (a) 8×8 input test pattern, (b) the 8×8 test pattern on reflection from the SLM device.
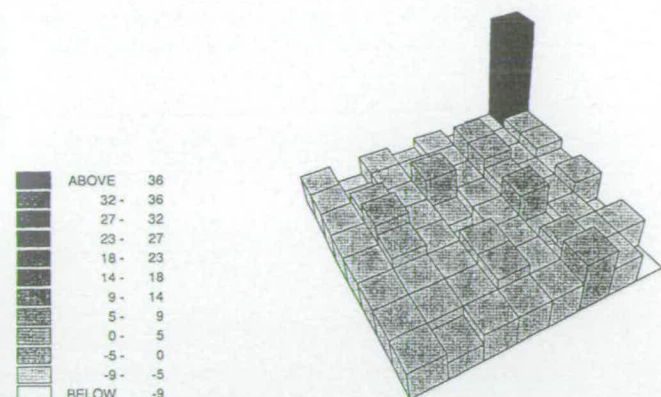
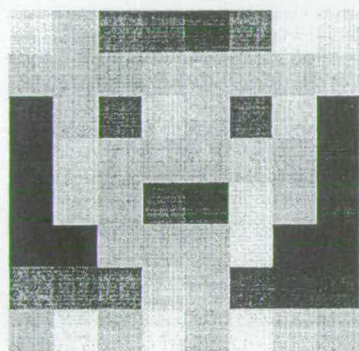Fig. 5. Optically measured Hadamard transform coefficients (a_{ij}) of the test pattern.

Fig. 6. Electronic reconstruction of the input pattern from the optical Hadamard transform coefficients.

Hadamard transform were individually displayed on the SLM. The light reflected from the SLM was focused, by a lens, onto a large photodetector, where the signal for the negative basis function was subtracted from the signal for the positive basis function to give a measured value for the Hadamard transform coefficient. The resultant set of Hadamard transform coefficients measured in this way for the input test pattern is shown in Fig. 5. As expected, the dc component has the largest value because this technique analyzes only input image intensity. This set of 64 coefficient values was input to a computer, and an inverse transformation was performed by digital computation. The reconstructed image is shown in Fig. 6 for comparison with Fig. 4(a). The experimental measurement error on the coefficients was approximately 10% in this simple system as a result of large instabilities in the light source. The effects

of this error can be observed as noise in the reconstruction. Steps to improve the accuracy include reducing the insertion losses in the SLM, increasing the sensitivity of the detector, and improving the stability of the incoherent illumination source or at least compensating for the variations.

An implementation of the Hadamard transform with an FLCOS SLM has been described that is suitable for applications in optical-to-electronic information conversion. An optimized system can bring the advantages of fast implementation and good signal-to-noise ratio to provide a useful selective frequency representation of real images while retaining a large dynamic range. Further studies are aimed at investigating higher-resolution transforms on larger-array SLM's and examining how the characteristics of available and future devices determine the accuracy of the transform coefficients. With submicrosecond liquid-crystal switching times[5] and generation of the basis functions on chip within a specially designed FLCOS SLM backplane device, high-resolution Hadamard transformation will be possible in excess of TV frame rates. Such dedicated systems would also be attractive for those all-optical communication applications in which high noise tolerance and data compression are required. Such techniques are not limited to the Hadamard transform, and other binary transform representations are possible.

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Improving the performance of liquid-crystal-over-silicon spatial light modulators: issues and achievements

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The performance of liquid-crystal-over-silicon spatial light modulators has advanced rapidly in recent years. Most progress has centered around new device designs with increased bandwidth. In this paper we report on a number of techniques to improve the optical quality; these have applications in both current and future devices.

Key words: Spatial light modulators, optical quality, ferroelectric liquid crystal, mirror morphology, gray scale, planarization.

1. Introduction

The hybrid technology of liquid-crystal-over-silicon has proved successful within the wider field of spatial light modulators (SLM's). The primary attractions are, first, that both component technologies have a high degree of inherent compatibility, and second, that the industries built around the component technologies, i.e., the Si and the liquid-crystal (LC) industries are each progressing rapidly so that the performance capability of SLM's has increased and can be expected to continue to increase significantly purely as a consequence of improvements in the component technologies. The latter is illustrated clearly by the progress over the past ten or so years in Si, from large-scale integration to very-large-scale integration (VLSI) and beyond, and in LC's, from nematic and related materials to the much faster switching smectic materials and in particular the surface-stabilized ferroelectric liquid-crystal (SSFLC) effect.[1] The attendant progression in SLM capabilities is shown in Table 1.

In addition to the SLM performance gains derived from the mainstream of the two component technolo-

gies, further performance gains are derived from SLM-specific (added-value) research such as custom SLM-specific VLSI (circuit and layout) design. This includes dynamic random-access memory (DRAM) and static random-access memory (SRAM) pixels as well as smart pixels that incorporate local processing or photodetectors. The development of custom SLM-specific VLSI fabrication methods, SLM-specific FLC materials, Si backplane packaging for SLM's, and FLC cell fabrication techniques that are compatible with the Si backplanes permits the enhancement of functionality, performance, and quality.

Most current SLM designs are based on Si backplanes of ~ 1- to 3-μm complementary metal-oxide semiconductors coupled with SSFLC's. We henceforth refer to the technology as ferroelectric liquid crystal over very-large-scale integration, FLC/VLSI. The Si backplanes are generally digital in nature and thus match the inherently binary nature of the SSFLC. The current status of SLM technology is examplified by the 176 × 176 DRAM device shown in Fig. 1.

In judging the performance of FLC/VLSI SLM's, particularly the functionally simple SLM's based on SRAM and DRAM, two main issues merit individual inspection: bandwidth and optical quality. The literature indicates that most progress has been made in the former by increasing the pixel count, the frame rate, or both. In this paper we report on a number of issues that have a direct impact on the latter.

We consider the following topics. In Section 2 we look at recent progress in customizing the fabrication of the Si backplane. The benefits include a high-

Table 1. Examples from the Literature that Show the Development of FLC/VLSI Devices

Year	Group/Reference	Backplane Technology	Liquid Crystal	Resolution ($n \times n$)	Frame Rate (Hz)	Pixel Circuit
1986	Univ. of Edinburgh[2]	6-μm nMOS[a]	Guest host	16	5	SRAM[c]
1988	Univ. of Edinburgh[3]	1.5-μm nMOS	Twisted nematic	50	60	SRAM
1989	Univ. of Edinburgh[4]	3-μm CMOS[b]	FLC	176	1 K	DRAM[d]
	STC Technology					
	GEC-Marconi					
	Research Centre					
1990	Displaytech[5]	3-μm CMOS	FLC	64	8 K	SRAM
1992	Univ. of Colorado[6]	2-μm CMOS	FLC	128	5 K	DRAM
	Boulder Nonlinear					
	Systems					

[a] nMOS, n-type metal-oxide semiconductor.
[b] CMOS, complementary metal-oxide semiconductor.
[c] SRAM, static random-access memory.
[d] DRAM, dynamic random-access memory.

quality optical finish that aids the alignment of the FLC layer and permits flat pixel mirrors coupled with a high fill factor. In Section 3 we examine a method of producing gray scale by temporal multiplexing on a binary device, thus enhancing its application potential. In electronical addressing of the device, the charge (or dc) balancing condition is maintained to extend the lifetime of the liquid crystal. Finally, in Section 4 we look at the potential of the above described techniques to promote further improvements.

2. Custom Silicon Fabrication

A. Procedure

The poor optical quality of the metal that forms the mirrors on the Si backplanes is due primarily to the electronically necessary sinter procedure during the metallization stage of microfabrication. Following the metal-deposition, photolithography, and metal-etch stages of fabrication, the wafers must be sintered to produce good ohmic contacts and improved adhesion of the Al film to the underlying SiO_2.[7] A typical example of this procedure involves the wafers being inserted into a furnace at 435 °C for 20 min in the presence of a forming gas ($40\%H_2/60\%N_2$). During the heating and cooling phases of the operation, stresses are induced in the films, and to relieve these stresses, the Al film distorts, which results in hillocks and depressions being formed.[8,9] The optical efficiency of the mirror is therefore substantially reduced because these irregularities scatter the light incident upon the mirror surface.

To protect the Al film during the sinter procedure, we applied a low-temperature SiO_2 coating to the wafer by using electron cyclotron resonance plasma-enhanced chemical-vapor deposition.

In the course of the anneal operation, the SiO_2 film acts as a constraining layer and, when the anneal is complete, the SiO_2 is removed. Initial work was carried out on test structures[10]; this technique has now been incorporated into the fabrication procedure of two batches of SLM wafers, both fabricated at the Edinburgh Microfabrication Facility (EMF). This additional procedure permits high electrical performance to be achieved without a reduction in the optical quality of the mirrors. An example of the improvement on mirror quality when the sinter protection layer is used is shown in Fig. 2.

Increasing the pixel mirror fill factor requires multilevel metallization in which the mirror is deposited as the last metal layer on top of the underlying circuitry. Further, this structure eliminates spurious switching of the LC layer that is due to electrical signals on exposed interconnect lines and partially protects the underlying circuitry from incident light that would otherwise lead to increased leakage currents in the circuit. In order to provide a flat surface onto which the mirror can be deposited, the intermediate dielectric must be planarized. Various planarization techniques are used in the semiconductor industry; however, the only method capable of producing the standard of optical flatness necessary here is chemical-mechanical polishing[11] (CMP). Although it is only recently that CMP has been used at this stage in the processing sequence it is already being used in the manufacture of leading-edge technology chips.[12,13] We have applied this technique to enhance our SLM's by adding it as a backend step on fully fabricated wafers. Studies have been carried out on electrically inactive 176×176 SLM backplane wafers in which the finished wafer is coated with ~ 4 μm of electron cyclotron resonance plasma-enhanced chemical-vapor deposited SiO_2 and is then polished to produce an optically flat surface. Metal is then deposited to produce high-quality mirrors. Figure 3(a) shows an area of a 176×176 SLM that is then coated with Al to enable the surface flatness to be measured by the use of interferometry [Fig. 3(b)]. We have demonstrated that, by using this technique, we can obtain the surface flatness on the intermediate dielectric that is essential for the fabrication of high-quality mirrors. The main difficulty associated with CMP is maintaining the uniformity of the polishing rate across the wafer.[10] Experimentation has allowed us to improve the control of the polishing
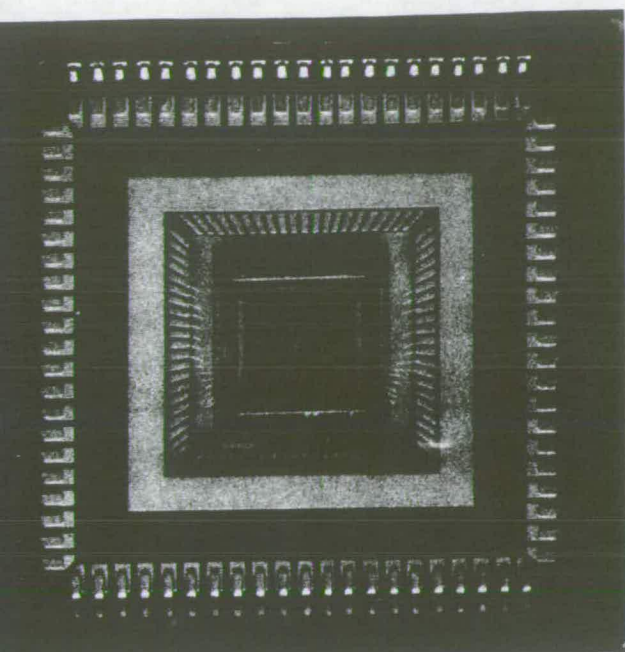
(a)

(b)

Fig. 1. 176 × 176 DRAM SLM (a) device, (b) displayed image (courtesy of GEC-Marconi). The backplane of this device is untreated.

ate to a point where we are now, for the first time, incorporating CMP into the fabrication sequence of fully operational wafers.

The improvements to the Al mirror surface quality have implications beyond improving the mirror efficiency. Previously, unevenness of the Al surface has had an adverse effect on LC alignment. By improving the mirror surface, the LC alignment has been enhanced (see Subsection 2.B). Our initial experience with cell fabricated by the use of backplanes produced with the hillock suppression technique sug-

(a)
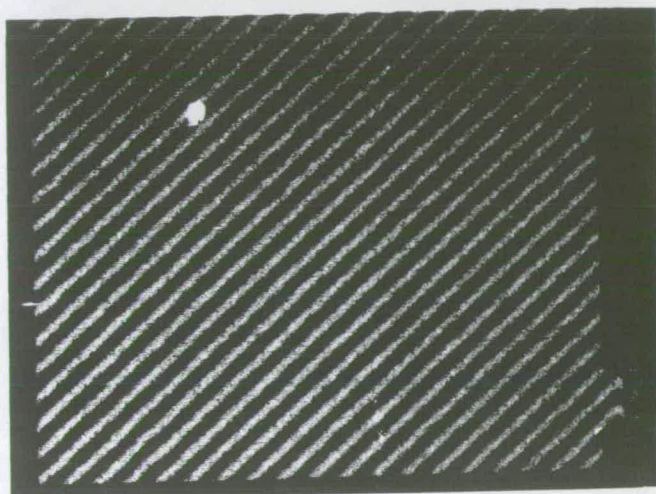
(b)

Fig. 2. Interferograms of pixel mirrors fabricated by the use of (a) standard procedure, (b) metal protection technique.

gests that LC layer thickness uniformity is greatly enhanced. We propose that this arises because the presence of hillocks causes tilting of the cover glass and a consequence wedging of the LC layer. Further investigation is required before reaching a firm conclusion.

B. Mirror Morphology

Good mirror quality is crucial to enable highly aligned FLC structures. The alignment of FLC molecules is highly dependent on the bounding surface morphology. Irregular hillocks and depressions locally alter the sensitive boundary conditions required of the SSFLC device structure. They disturb the formation of parallel smectic planes, introduce variations in surface molecular tilt angle, and randomly induce all manner of defects from the device ideal.[14] The boundary conditions for the formation of the SSFLC device structure are generally obtained by anisotropic treatment of the bounding plates. Surface energy is transferred to the bulk FLC medium by elastic forces. The surface treatment usually takes the form of the
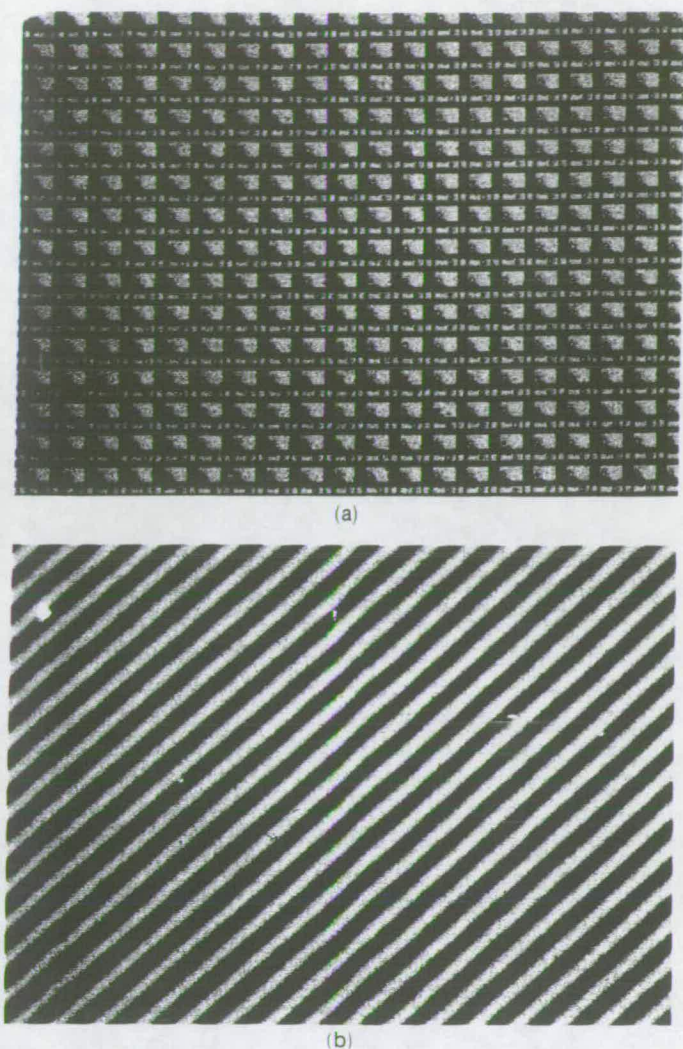
(a)

(b)

Fig. 3. Effect of CMP technique for backplane planarization: (a) Part of 176 × 176 SLM backplane with an area of ~ 600 μm × 450 μm, (b) interferogram of part of a polished wafer following metallization. Magnification is the same as (a).

creation of microrelief structures. A common technique for the generation of such structures is oblique evaporation of thin films such as SiO_x that can generate a variety of anisotropic surface structures such as ridges and tilted columns.[15] This surface energy should be uniform across the bounding plates of the FLC device. If large enough, any perturbation from this uniformity affects the molecular alignment in the bulk FLC material. Therefore mirror quality directly determines the defect structure. It is unlikely that surface treatments can compensate for large fluctuations in the surface energy caused by poor mirror quality.

Defect-free FLC structures should be obtainable when high-quality mirrors can be constructed on VLSI Si backplane SLM devices. Such improvements are significant steps toward increases in contrast ratio, device uniformity, modulation efficiency, and reflectivity. This improvement is demonstrated by a comparison of FLC devices fabricated on a standard (unprotected metal) VLSI process and those

Fig. 4. SEM picture of alignment structure produced by oblique SiO_x evaporation.

fabricated on a protected metal process, as described above. The protected metal process results in a reduction of hillock and depression formation, although some of these undesirable features can still be observed. It was expected that such an improvement to the mirror quality would result in more favorable surface conditions to attain good FLC alignment. This has been observed experimentally. SSFLC cells were constructed on two SLM devices from the same VLSI process. The SLM backplane used was a 16 × 16 test-bed device.[2,16] The wafers were processed at the EMF. One device originated from a wafer that used the standard, unprotected metal process. The other originated from a wafer fabricated with the extra metal protection processing step described at the beginning of Subsection 2.A. The SSFLC device alignment layers were obliquely evaporated with SiO_x to a thickness of 50 nm on both the SLM chip and the front cover glass with an indium tin oxide transparent–conducting electrode. The SiO_x was obliquely evaporated at an angle of 30° to the substrate. This is commonly referred to as medium-angle deposition.[15] This alignment layer technique results in a ridge structure with a period of ~ 100 nm running perpendicular to the direction of evaporation, which has been observed by a scanning electron microscope (SEM) and is shown in Fig. 4. This structure gives relatively strong surface anchoring of the FLC molecules. A zig-zag defect structure is usually observed in FLC test cells, suggesting the presence of the chevron defect. Small-angle deposition has been shown to give improved alignment with FLC devices.[15] But oblique evaporation of SiO_x at ~ 5° will have major shadowing problems because of the topography of the surrounding circuitry. Only fully planarized SLM backplanes would permit problem-free oblique evaporation at small angles on pixel mirrors. Alternatively the small-angle deposition technique could be applied to only the front cover glass electrode, and this would result in asymmetric boundary conditions on the FLC device. A study into such asymmetric alignment layers would be of considerable interest.
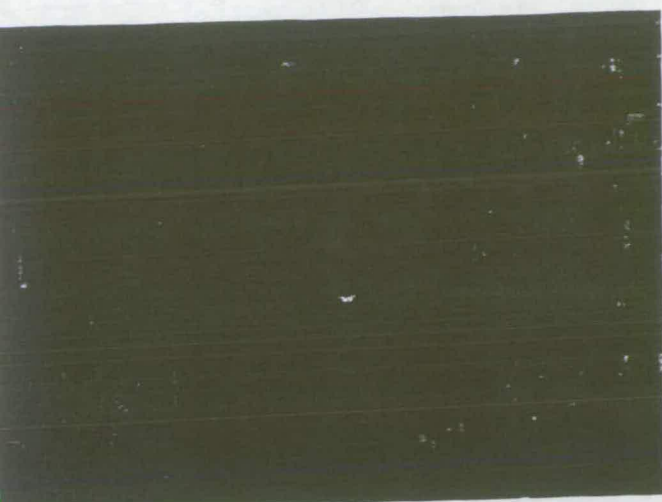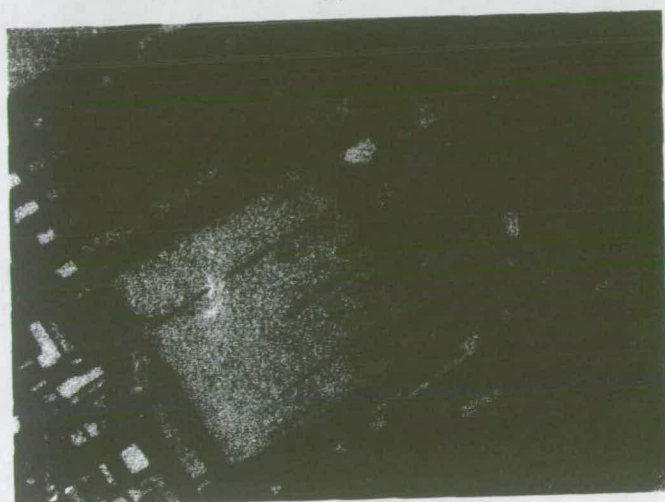
Fig. 5.   LC structure on pixel (a) untreated, OFF; (b) untreated, ON; (c) treated, OFF; (d) treated, ON.

An FLC cell was constructed on the SLM chip with a 1-μm cell gap between the mirrors and the conducting front electrode. The device is therefore optimized to operate in reflection as a switchable half-wave plate with smectic C* FLC material exhibiting a 22.5° cone angle for light with a wavelength of approximately 633 nm (He–Ne). The device was filled with SCE13 FLC material (Merck–British Drug House) under vacuum at an elevated temperature of 120 °C. Both protected metal and unprotected metal devices were constructed under the same conditions. Therefore these devices permitted comparisons to be made to show any improvement to the FLC characteristics. Figures 5(a) and 5(b) show the unprotected metal device illuminated with polarized light and observed through cross polarizers, respectively. Figures 5(c) and 5(d) show the protected metal device under similar circumstances. On the unprotected metal device one observes a lower reflectivity and apparently no domain structure. There are domains, however, but they are so numerous and fine (because of the poor metal quality) that they appear uniform. This is not a desirable feature as they will

still adversely affect performance and be difficult to remove. In the metal protected sample, domains are large and clearly visible. This is actually encouraging as such distinct domains are observed in glass-on-glass FLC test cells. Therefore the alignment of the FLC in the metal protected device is clearly approaching the level attainable in high surface quality test cells. We conclude that the high performance of FLC structures observable in test cells should be possible through improved metal quality VLSI backplane SLM's.

3.   Temporal Multiplexed Gray Levels

Gray-level SLM's have many potential uses, including display applications and as adaptive weight planes in optoelectronic neural networks. As described in the introduction, most current FLC/VLSI SLM's operate in a binary mode. However, the microsecond switching times of the FLC and the high addressing speeds of Si backplanes permit temporal multiplexing to be used as a means of real-time gray-level generation.
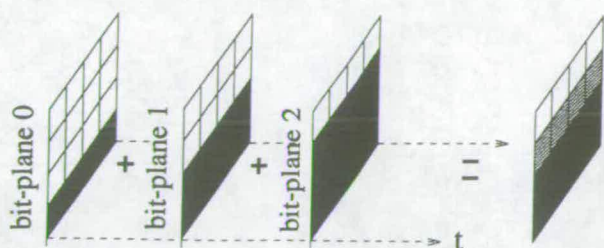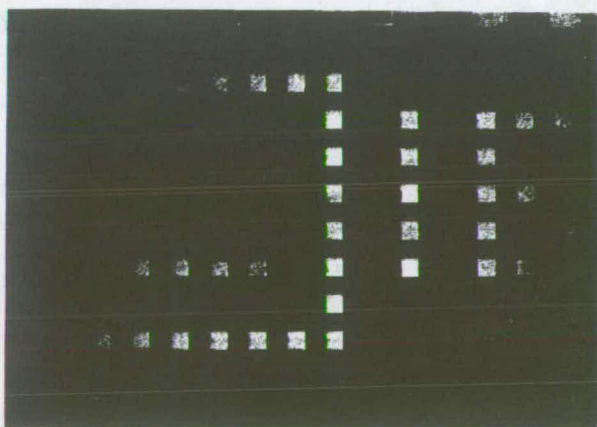
Fig. 6. Four-gray-level image obtained by the use of a linear encoding algorithm.

Temporal multiplexing involves splitting each gray-level image into a number of time-sequential subframes. Each subframe has an associated bit-plane that is generated by an approximate encoding algorithm. These bit-planes are then sequentially scanned into the SLM to produce the desired gray-level image.

A simple linear encoding algorithm has been used to create the bit-planes. Figure 6 shows how a four-gray-level image is built up. For the 16 gray levels illustrated in Fig. 7, 15 subframes were required. Each subframe lasts 500 μs, resulting in a frame rate of ~133 Hz.

The linear encoding algorithm above is satisfactory for generating a small number of gray levels; however, each extra gray level requires an extra subframe. The frame rate is inversely proportional to the number of gray levels. A more efficient binary weighted encoding algorithm with a pulsed light source, as illustrated in Fig. 8 is now being investigated. In this case, n subframes can generate 2^n gray levels. So, for example, 256 gray levels can be generated at 125 Hz when a 1-ms subframe duration is used.
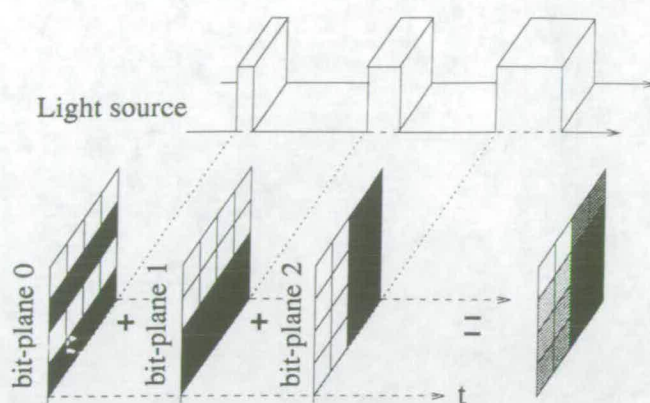

Fig. 8. Eight-gray level image obtained by the use of a binary encoding algorithm and a pulsed light source.

A. Advantages of Surface-Stabilized Ferroelectric Liquid Crystals for Producing Gray Scale

There are, in principle, several advantages to producing gray scale as described above:

(1) The fast switching speed of the FLC should eliminate the problems of shadowing and ghosting of a fast moving pattern that are associated with slow switching nematic-LC displays.

(2) In contrast to the gray levels produced by applying *analog* electrical signals to nematic LC's, there should be no phase variations associated with the gray levels produced by temporal multiplexing in which the applied electrical signal is *digital*. This makes the proposed scheme particularly suitable for use in coherent optical systems.

B. Direct-Current Balancing

It is widely accepted that to prevent chemical degradation of the FLC layer, the electric field across it should be properly dc balanced. In DRAM-type devices, this has been achieved by scanning in a bit-plane; then, after the FLC is allowed to settle and the read beam is pulsed, the exact inverse of the bit-plane is scanned in with the front electrode signal toggled.[4] The resulting image duty cycle was less than 5%.

The functionality of some SRAM-type pixels, such as those on the 16×16 SLM, is enhanced by the inclusion an XNOR gate.[2] The inputs to the XNOR are the pixel latch and a global clock signal. One can achieve dc balancing simply by continually toggling both the global clock and the front electrode. The resulting image duty cycle is 50%. A further advantage over the DRAM pixel is the availability of an effectively unlimited amount of charge to switch the FLC. This is discussed elsewhere.[6]

4. Conclusions and Future Developments

In this paper we began by identifying that improving the optical performance of FLC/VLSI SLM's is a critical issue if their success is to be continued.

We have demonstrated several techniques that, when applied to the Si backplane, boost the optical quality of finished devices. Custom sintering of the

3	2	1	0
7	6	5	4
11	10	9	8
15	14	13	12

Fig. 7. Photo showing 16 linearly encoded temporal multiplexed gray levels. The key shows the gray level present in the central square of 4 × 4 pixels.

metal layer has facilitated much improved FLC alignment and a consequent increase in optical contrast and uniformity. CMP has allowed the planarization of electrically inactive Si backplanes to optical flatness. This makes possible, for what is, to our knowledge, the first time, pixels that exhibit both optical flatness and a high fill factor. This research will continue with the application of the techniques to fully operational Si wafers, thereby permitting the improvements to be translated into fully working FLC/VLSI devices.

We have demonstrated a means of producing gray scale on an inherently binary device by means of temporal multiplexing. The drive scheme for the device maintains the dc balance condition that is essential for device longevity. The next steps here are to apply a binary weighting scheme to the subframes to permit the production of 2^n gray levels from n subframes and to prove by experiment the hypotheses made in Subsection 3.A, namely, that such a system eliminates shadowing and ghosting and that the gray levels produced are phase free.

The techniques described are applicable to all FLC/VLSI backplanes and will be used to enhance the performance of the next generation of SLM's based on backplanes, recently designed at The University of Edinburgh and currently in fabrication, which include a 256×256 SRAM backplane and a 512×512 DRAM backplane.

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