THE UNIVERSITY *of* EDINBURGH

Autonomous Smart Antenna Systems for Future Mobile Devices

Wei Zhou

A thesis submitted for the
Degree of Doctor of Philosophy
The University of Edinburgh
2014

DECLARATION

I hereby declare that this thesis has been composed by myself and that except where stated, the work contained is my own. I also declare that the work contained in this thesis has not been submitted for any other degree or professional qualification except as specified.

_____

Wei Zhou

August 2014

Edinburgh, UK

ACKNOWLEDGEMENTS

First of all, I wish to express my greatest gratitude to my supervisor, Professor Tughrul Arslan for his invaluable support, constant encouragement and incisive guidance throughout this study.

I wish also like to extend my appreciation to my second supervisor Dr. Khaled Benkrid, for his useful comments and suggestions in this research. I would like to thank Dr. Brian W. Flynn, Dr. Ahmed O. El-Rayis, Dr. Nakul Haridas, Dr. Ahmet T. Erdogan, and Mrs. Susan Kivlin for their support and help during my PhD study.

To the members of the System Level Integration Group (SLIG) and Advanced Smart Antenna Technologies (ASAT) research group, I owe sincere and earnest thankfulness for the unforgettable and unique experience of my life.

I would also like to thank all my colleagues in the Sofant Technologies for their friendship and support.

I am extremely grateful to my family and my girl friend, Miss Dixiao Shen, for their understanding, patience and support during the research and the preparation of this thesis.

ABSTRACT

Along with the current trend of wireless technology innovation, wideband, compact size, low-profile, lightweight and multiple functional antenna and array designs are becoming more attractive in many applications. Conventional wireless systems utilise omni-directional or sectored antenna systems. The disadvantage of such antenna systems is that the electromagnetic energy, required by a particular user located in a certain direction, is radiated unnecessarily in every direction within the entire cell, hence causing interference to other users in the system. In order to limit this source of interference and direct the energy to the desired user, smart antenna systems have been investigated and developed. This thesis presents the design, simulation, fabrication and full implementation of a novel smart antenna system for future mobile applications.

The design and characterisation of a novel antenna structure and four-element liner array geometry for smart antenna systems are proposed in the first stage of this study. Firstly, a miniaturised microstrip-fed planar monopole antenna with Archimedean spiral slots to cover WiFi/Bluetooth and LTE mobile applications has been demonstrated. The fundamental structure of the proposed antenna element is a circular patch, which operates in high frequency range, for the purpose of miniaturising the circuit dimension. In order to achieve a multi-band performance, Archimedean spiral slots, acting as resonance paths, have been etched on the circular patch antenna. Different shapes of Archimedean spiral slots have been investigated and compared. The miniaturised and optimised antenna achieves a bandwidth of 2.2GHz to 2.9GHz covering WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) mobile standards. Then a four-element linear antenna array geometry utilising the planar monopole elements with Archimedean spiral slots has been described. All the relevant parameters have been studied and evaluated. Different phase shifts are excited for the array elements, and the main beam scanning range has been simulated and analysed.

The second stage of the study presents several feeding network structures, which control the amplitude and phase excitations of the smart antenna elements. Research begins with the basic Wilkinson power divider configuration. Then this thesis presents a compact feeding network for circular antenna array, reconfigurable feeding networks for tuning the operating frequency and polarisations, a feeding network on high resistivity silicon (HRS), and an ultra-wideband (UWB) feeding network covering from 0.5GHz to 10GHz. The UWB feeding network is used to establish the smart antenna array system.

Different topologies of phase shifters are discussed in the third stage, including ferrite phase shifters and planar phase shifters using switched delay line and loaded transmission line

technologies. Diodes, FETs, MMIC and MEMS are integrated into different configurations. Based on the comparison, a low loss and high accurate Hittite MMIC analogue phase shifter has been selected and fully evaluated for this implementation. For the purpose of impedance matching and field matching, compact and ultra wideband CPW-to-Microstrip transitions are utilised between the phase shifters, feeding network and antenna elements. Finally, the fully integrated smart antenna array achieves a 10dB reflection coefficient from 2.25GHz to 2.8GHz, which covers WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) mobile applications. By appropriately controlling the voltage on the phase shifters, the main beam of the antenna array is steered ±50° and ±52°, for 2.45GHz and 2.6GHz, respectively. Furthermore, the smart antenna array demonstrates a gain of 8.5dBi with 40° 3dB bandwidth in broadside direction, and has more than 10dB side lobe level suppression across the scan.

The final stage of the study investigates hardware and software automatic control systems for the smart antenna array. Two microcontrollers PIC18F4550 and LPC1768 are utilised to build the control PCBs. Using the graphical user interfaces provided in this thesis, it is able to configure the beam steering of the smart antenna array, which allows the user to analyse and optimise the signal strength of the received WiFi signals around the mobile device.

The design strategies proposed in this thesis contribute to the realisation of adaptable and autonomous smart phone systems.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ACRONYMS AND ABBREVIATIONS

1D	=	1 Dimensional
2D	=	2 Dimensional
3D	=	3Dimensional
3G	=	Third Generation
4G	=	Fourth Generation
ACPS	=	Asymmetric Coplanar Stripline
ADC	=	Analogue to Digital Converter
ADS	=	Advanced Design System
AF	=	Array Factor
AM	=	Amplitude Modulation
BE	=	Beam Efficiency
BST	=	Barium Strontium Titanate
CBCPW	=	Conductor Backed Coplanar Waveguide
CLK	=	Clock Frequency
CP	=	Circular Polarisation
CPW	=	Coplanar Waveguide
CPU	=	Central Processing Unit
CS	=	Chip Select
CTR	=	Centre-Tapped Resistors
DAC	=	Digital to Analogue Converter
DC	=	Direct Current
DGFET	=	Dual Gate FET
DMA	=	Dynamic Memory Allocation
EM	=	Electromagnetic
EMI	=	Electromagnetic Interference
ESD	=	Electrostatic Discharge
FDTD	=	Finite Difference Time Domain
FET	=	Field-Effect Transistor
FGC	=	Finite Ground Coplanar
FM	=	Frequency Modulated
GaAs	=	Gallium Arsenide
GGG	=	Gadolinium Gallium Garnet
GPIO	=	General Purpose Input / Output
GPS	=	Global Positioning System

GSM	=	Global System for Mobile Communications
GUI	=	Graphical User Interface
HPBW	=	Half Power Beam Width
HSPLL	=	High Speed Crystal/Resonator with Phase Locked Loop
HRS	=	High Resistivity Silicon
IC	=	Integrated Circuit
ICSP	=	In Circuit Serial Programming
IMD	=	Intermodulation
ISP	=	In System Programming
LHCP	=	Left-Hand Circularly Polarised
LTE	=	Long-Term Evolution
MCLR	=	Master Clear Reset
MEMS	=	Miroelectromechannical Systems
MIC	=	Microwave Integrated Circuit
MIMO	=	Multiple Input Multiple Output
MMIC	=	Monolithic Microwave Integrated Circuit
MOSFET	=	Metal Oxide Semiconductor Field Effect Transistor
MSB	=	Most Significant Bit
NPN	=	A Bipolar Transistor with a Layer of P-Doped between Two N-Doped Layers
PC	=	Personal Computer
PCB	=	Printed Circuit Board
PEC	=	Perfect Electric Conductor
PLL	=	Phase Locked Loop
PNP	=	A Bipolar Transistor with a Layer of N-Doped between Two P-Doped Layers
QFN	=	Quad Flat No Leads
QFP	=	Quad Flat Package
RF	=	Radio Frequency
RFI	=	Radio Frequency Interference
RFID	=	Radio Frequency Identification
RHCP	=	Right-Hand Circularly Polarised
RSSI	=	Received Signal Strength Indicator
SCK	=	Serial Clock
SDI	=	Serial Data In
SDO	=	Serial Data Out
SLL	=	Sidelobe Level
SMA	=	SubMiniature version A

SMC	=	Scottish Microelectronics Centre
SMD	=	Surface Mount Device
SNoI	=	Signal Not of Interests
SNR	=	Signal to Noise Ratio
SOLT	=	Short-Open-Load-Through
SoI	=	Signal of Interests
SPI	=	Serial Peripheral Interface
SSID	=	Service Set Identity
UART	=	Universal Asynchronous Receiver/Transmitter
USB	=	Universal Serial Bus
UWB	=	Ultra Wideband
VNA	=	Vector Network Analyser
VSWR	=	Voltage Standing Wave Ratio
WiFi	=	Wireless Fidelity
YIG	=	Yttrium Iron Garnet

Chapter 1: Introduction

1.1 Research Motivation

The adoption of smart antenna techniques in communication systems demonstrates significant impacts on the efficient use of the spectrum, the optimisation of service quality, the minimisation of the network configurations, and realisation of transparent operation across multi-technology wireless networks. Furthermore, smart antennas have been identified to support several benefits include antenna gain, increased directivity, and a host of capabilities enabled with arrayed antennas and signal processing techniques including beam forming, null steering, spatial processing, diversity, and multiple input multiple output (MIMO) [1-4]. Smart antenna system utilises adaptive beam forming algorithm in a dynamic environment continuously adjusting the weight of antenna arrays for generating a beam to track desired users automatically, and placing nulls in other directions to minimise the interferences [5].

Smart antennas consist of two approaches: switched beam system and adaptive system [6]. A switched beam antenna, as illustrated in Figure 1.1(a), has a finite number of predefined radiation patterns and the appropriate beam pattern is selected based on the system requirement. Although the spatial dimension of the antenna is exploited, sometimes the main beam cannot point to the signal of interest (SoI) accurately, as shown in Figure 1.1(b).

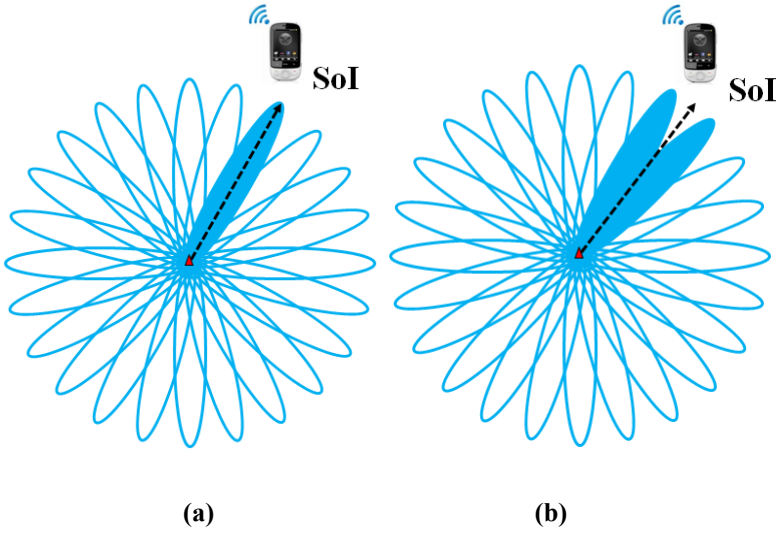


Figure 1.1: (a) Predefined Switched Beam Antenna (b) Low Resolution of the Main Beam

Comparatively, in the adaptive antenna system, the beam pattern is configured by adjusting the excitation of the individual antenna elements, which provides beam orientation in any directions in response to its signal environment, as depicted in Figure 1.2(a). Moreover, these excitations could be manipulated in order to suppress the radiation in the direction of signals not of interest (SNoI), as shown in Figure 1.2(b). With this adaptive beamforming, the smart antenna is able to maximise the spatial usability.

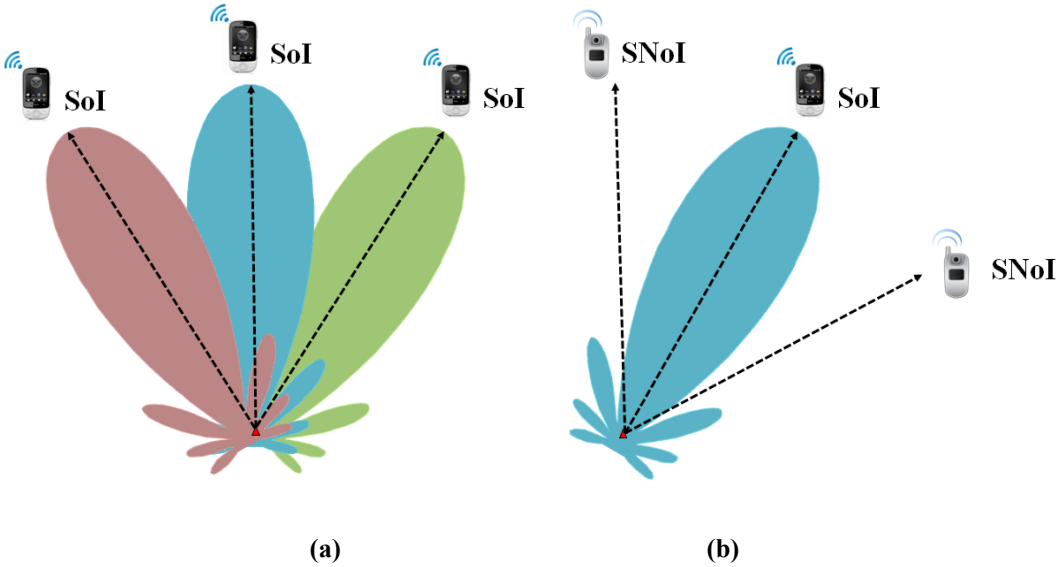


Figure 1.2: Adaptive Antenna (a) Arbitrary Steering (b) Adaptive Beamforming

Smart antenna systems are composed of reconfigurable antennas, control networks to provide beamforming functionality, and software for signal processing. Lots of successful implementations have revealed the capability of smart antenna technology on performance enhancement in terms of range, radio coverage, data rate, capacity, and flexibility. Pattern

reconfigurable antenna elements and weighted thinned synthesis technology has been presented in [7], a four-element phased array antenna using carbon nanotube thin-file transistors on a flexible Kapton polyimide substrates is demonstrated in [8], a electronically steerable parasitic array radiator antenna array is investigated in [9], a printed dipole phased array antenna using microstrip-fed coplanar stripline tee junctions has been shown in [10] and a reconfigurable RF MEMS phased array antenna within a liquid crystal polymer system-on-package has been presented in [11].

However, most of the designs have complicated structures and multilayer configurations. Moreover, not much of the works have been reported at WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) frequencies. For commercial applications, smart antenna systems with compact size, simple structure, low profile, reduced power consumption, wide scanning range, high gain and automatic control is required, which are the motivations of this research [12].

1.2 Research Investigations

The components in a complete smart antenna system include the antenna element, the array geometry, the feeding network, the phase shifter and the control unit. In order to achieve the autonomous smart antenna system, several challenges related to the components have to be addressed.

1.2.1 Design Challenges

1.2.1.1 Antenna Design

The microstrip antenna has become one of the most popular candidates for highly directive antenna applications due to its characterisations of light weight, low profile, easy fabrication, low cost and easy integration with other circuit components [13]. Several microstrip antennas have been developed to achieve multiple operating frequencies, reconfigurable polarisations, ultra wideband (UWB) performance or reconfigurable radiation patterns [14-16]. The greatest challenge associated with microstrip antenna design is to miniaturise the circuit dimension while maintaining certain antenna characteristics. In addition, the developed antenna structure should be able to easily integrate with feeding networks and phase shifters, in order to provide adaptive performance.

This research investigates the design of a planar monopole antenna with multiple operating frequency bands for mobile applications. Archimedean spiral slots are etched on a circular patch antenna for miniaturisation. The aim is to develop an antenna covering

2.45GHz/2.6GHz, in compact dimension, with suitable gain (3dB) and efficiency (70%), providing proper radiation patterns (omni-directional) and utilising a microstrip feed.

1.2.1.2 Array Geometry

Radiation pattern of an antenna array depends on the antenna arrangements, spacing between the elements, excitation phase of individual antenna and characterisations of the single element.

The theoretical separation between two adjacent elements is 0.5 λ, in order to avoid high coupling between neighbouring elements in an antenna array. Antennas that are separated less than 0.5λ will generate high coupling level and this consequently will distort the radiation pattern of the antenna array. Relatively, when the separations are more than 0.5λ, the tendency for grating lobes to occur is high and the gain is decreased. Due to the radiation power is transferred from the main beam to other lobes, grating lobes also reduce the peak directivity of the array [17-19].

Furthermore, in real smart antenna array implementations, the number of elements is limited. This also produces several design challenges, which include reduced angular scanning resolution, limited scanning range and high side lobe levels [20, 21].

The linear array geometry consisting of four elements is investigated in this research. The target is to develop an antenna array demonstrating low coupling (-10dB) and wide angle (±50º) scanning ability. Wide scan coverage is necessary in wireless communication system, since the transmission link is not always within the boresight of an antenna. Utilising the microstrip antenna, different inter-element spacing are investigated and compared. The gain, directivity, radiation patterns and mutual coupling are evaluated and analysed. Beam scanning range is estimated based on antenna gain, angular widths (3dB) and side lobe levels. Finally, the excitations of the antenna array will be configured by the feeding network to achieve adaptive beam scanning.

1.2.1.3 Feeding Network Structure

Another important configuration in the smart antenna array is the feeding network, which controls the amplitude and phase excitations of the antenna elements. The conventional T-junction power divider is lossless, but suffers from the issue of not being matched at all ports, and there is no isolation between the output ports. The resistance divider is able to match all the ports, however, the power loss is relative high and still no isolation is achieved. The conventional Wilkinson power divider is lossless and provides high isolation between outputs, but only operates at a certain frequency.

This research investigates reconfigurable and UWB feeding networks for smart antenna applications. Different feeding network geometries are developed, including feeding network on high resistivity silicon (HRS) and Aluminium wafers, circular feeding networks, reconfigurable feeding structure for multiple frequencies and dual circular polarisations, and also UWB feeding geometry. The main challenge is to achieve suitable S-Parameters for the required applications with compact circuit dimension and miniaturised power loss. Furthermore, suitable resistors are important in these geometries to produce high isolation (-10dB). Finally, the proposed feeding network should be able to easily integrate with the antenna elements.

1.2.1.4 Phase Shifter Implementation

In the proposed smart antenna system, phase shifters are used to provide required phase excitations. Various phase shifter structures are analysed and compared, which includes ferrite phase shifter, switched delay line phase shifter and loaded transmission line phase shifter. PIN diodes, FETs, MMIC and MEMS are employed as control elements in different configurations. The phase shifter should provide high and accurate phase excitations with low loss and suitable S-Parameters. Moreover, the control voltage cannot be too high due to low power mobile applications.

Based on the above design challenges, several phase shifter techniques are evaluated and a MMIC device has been fully characterised for the proposed smart antenna implementation.

Moreover, UWB CPW-to-Microstrip transitions are required between the antenna array, feeding network and phase shifters, for the purpose of providing suitable field matching and impedance matching. The aim is to develop miniaturised UWB transitions between CPW and microstrip transmission lines with minimum loss.

1.2.1.5 Hardware Control

Hardware control system is developed to configure the MMIC phase shifters and establish the communication between antenna array and mobile device. Control units are required to send suitable voltages to the smart antenna array and rotate the main beam direction. Basic algorithms are required to achieve the beam steering. The aim is to design compact processing units with accurate control ability and minimum power consumptions.

This research demonstrates two separate hardware control systems based on two microprocessors PIC18F4550 and LPC1768, respectively. After schematic design and layout analysis, both of the structures are fabricated on multilayer PCBs. In the developed smart array system, a USB WiFi adapter is running as a communication module between the

antenna array and mobile device. Basic algorithms are programmed into the processing units to achieve the adaptive beamforming.

1.2.1.6 Software Control

The software control program implemented in a mobile device contributes to the intelligence of a smart antenna array. The signals induced on each antenna element are processed and analysed, so as to adjust the array radiation characteristic in order to adapt to the environment.

Based on the developed hardware control units, several graphical user interfaces are investigated to automatically configure the smart antenna main beam direction. Current software program is using Windows. However, the algorithms can be easily transferred into Android and IOS systems. The attractive feature is the ability to locate the desired signal and perform the adaptive beamforming. The desired signal is calculated based on the received signal strength at different locations. Beamforming algorithms are used to optimise the complex excitations of the array elements.

Figure 1.3 summarises the area and challenges to be addressed in the thesis.

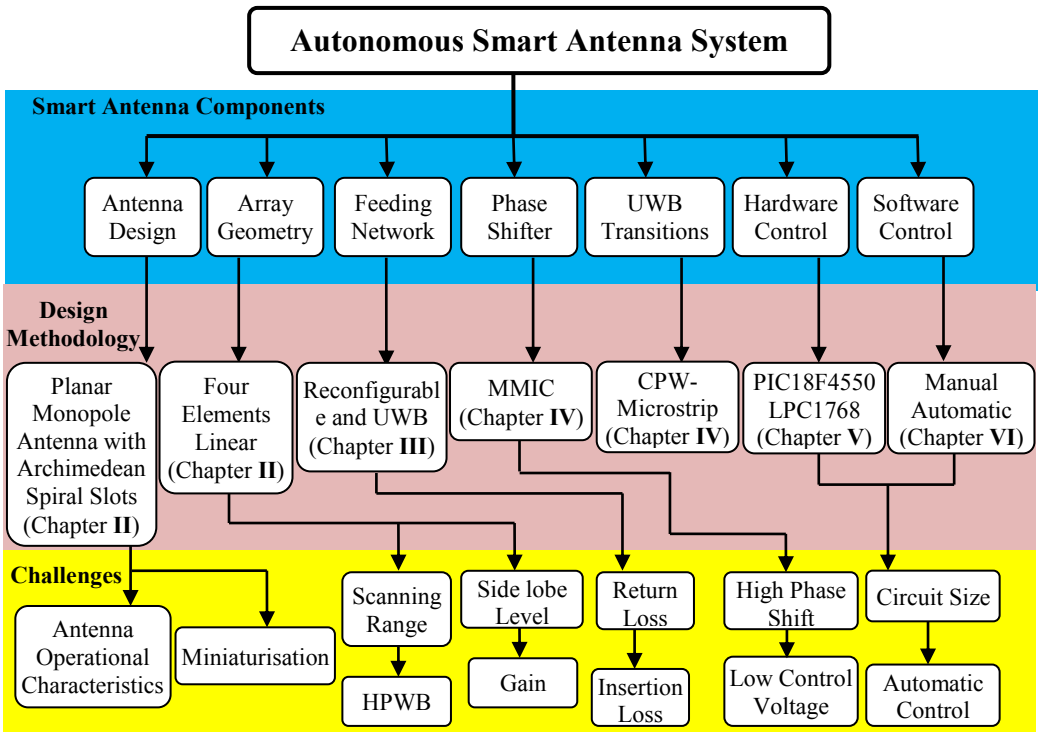


Figure 1.3: Overview of the Research Structure

1.2.2 Research Objectives

The main objectives of this research are:

1. Design a miniaturised multiband microstrip antenna for smart antenna system

2. Develop a wide scanning range adaptive array antenna

3. Produce reconfigurable and UWB feeding network for wireless communication system

4. Evaluate phase shifter techniques and select suitable device for smart antenna array

5. Smart Antenna full implementation and characterisation

6. Develop intelligent hardware and software control systems for realising smart antenna.

1.3 Overview of Thesis

This thesis is divided into seven chapters. In this chapter, the requirement and general structure of the autonomous smart antenna systems for mobile applications have been outlined.

Chapter 2 proposed a novel miniaturised planar monopole antenna. In order to achieve a multiband performance, Archimedean spiral slots, acting as resonance paths, have been etched on the circular patch antenna. Key parameters of the antenna structure are varied to understand their effects on the antenna characterisations. The optimised antenna demonstrates a bandwidth of 2.2GHz to 2.9GHz covering WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) mobile standards. Moreover, this chapter presents the design of a phased antenna array with wide scan coverage (±52º) for wireless communication systems. Various configurations and different separations between elements are analysed in order to achieve proper radiation patterns. Using suitable amplitude and phase excitations, the scanning range of the array is simulated and estimated.

Chapter 3 explores different feeding network structures for the smart antenna arrays. Based on the conventional Wilkinson power divider, firstly, a more compact structure has been proposed using high resistivity silicon (HRS) and Aluminium wafers. Then a feeding network for circular antenna array is demonstrated. Subsequently, two reconfigurable feeding networks to adjust the operating frequencies and circular polarisation directions are discussed. Finally, a UWB feeding network is developed and described for the smart antenna application.

In Chapter 4, several phase shifter techniques are studied, analysed and compared. A low loss (-3dB) and high accurate MMIC analogue phase shifter has been selected and fully

evaluated. This chapter also discusses the design and optimisation of UWB CPW-to-Microstrip transitions for field matching and impedance matching. Furthermore, the complete smart antenna array has been integrated and characterised. The scanning range, gain, side lobe levels are discussed and summarised.

Chapter 5 provides the smart antenna hardware control for mobile applications. Two control units are developed using microprocessor PIC18F4550 and LPC1768. The functions of key components in the circuit are discussed, including microchips, digital potentiometers, voltage boosters, oscillators and USB modules. The schematic design is transferred into PCB layout and finally fabricated and tested. Both of the integrated PCBs are able to configure the phase shifters and so to control the smart antenna array beam steering.

Chapter 6 presents the software control system for the smart antenna array. Several preliminary graphical user interfaces are developed to manually and automatically configure the smart antenna. In this implementation, a laptop running Windows system is used to display WiFi information at different beam directions. It is able to achieve the automatic beam steering and basic adaptive beamforming.

Chapter 7 concludes the research investigations and suggests future work.

Figure 1.4 illustrates the block diagram of the developed autonomous smart antenna system.

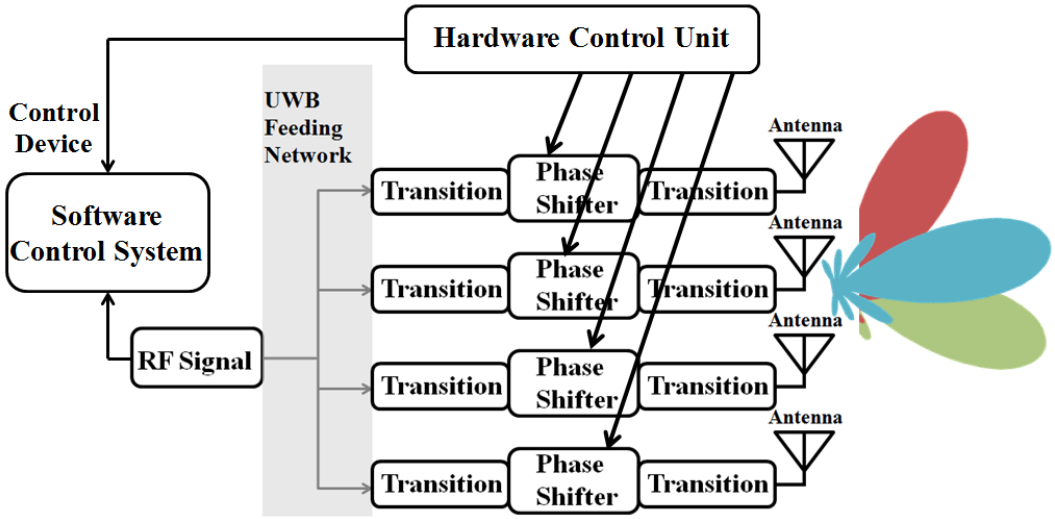


Figure 1.4: Block Diagram of the Autonomous Smart Antenna System

1.4 Key Contributions of the Thesis

The thesis contains number of novelties, which are including:

i. Miniaturised and multiband microstrip antenna for WiFi/Bluetooth and LET applications

ii. Adaptive array geometry with wide scanning range

iii. Reconfigurable and UWB feeding network for microwave applications

iv. Phase shifter technology accurate evaluation and comparison

v. UWB CPW-to-Microstrip transitions for RF circuits

vi. Compact hardware control units for smart antenna

vii. Software program to achieve adaptive beamforming

1.5 Publications Arising from This Research

In the course of this research, the following journals and conference papers have been published and submitted:

1. Wei Zhou; Noordin, Nurul; Haridas, Nakul; El-Rayis, Ahmed; Erdogan, Ahmet; Arslan, Tughrul, "A WiFi/4G compact feeding network for an 8-element circular antenna array," 2011 Loughborough Antennas and Propagation Conference (LAPC),vol., no., pp.1,4, 14-15 Nov. 2011

2. Yan Chiew Wong; **Wei Zhou**; El-Rayis, Ahmed; Haridas, Nakul; Erdogan, Ahmet; Arslan, Tughrul, "Practical design strategy for two-phase step up DC-DC Fibonacci Switched-Capacitor converter," 2011 20th European Conference on Circuit Theory and Design (ECCTD), vol., no., pp.817,820, 29-31 Aug. 2011

3. Wei Zhou; Arslan, Tughrul; Benkrid, Khaled "Low Power Autonomous Smart Antenna System for Future Mobile Devices," University of Edinburgh Postgraduate Student Poster Conference, 23 Apr. 2012

4.Noordin, Nurul; **Wei Zhou**; El-Rayis, Ahmed; Haridas, Nakul; Erdogan, Ahmet; Arslan, Tughrul, "Single-feed polarization reconfigurable patch antenna," 2012 IEEE Antennas and Propagation Society International Symposium (APSURSI), vol., no., pp.1,2, 8-14 July 2012

5.Wei Zhou; Haridas, Nakul; El-Rayis, Ahmed; Erdogan, Ahmet; Benkrid, Khaled; Arslan, Tughrul, "Enhanced Wilkinson divider on Si substrate for energy efficient microwave applications," 2012 Loughborough Antennas and Propagation Conference (LAPC), vol., no., pp.1,4, 12-13 Nov. 2012

6.Wei Zhou; Arslan, Tughrul; Benkrid, Khaled; El-Rayis, Ahmed; Haridas, Nakul, "Reconfigurable feeding network for GSM/GPS/3G/WiFi and global LTE applications," 2013 IEEE International Symposium on Circuits and Systems (ISCAS), vol., no., pp.958,961, 19-23 May 2013

7.Wei, Zhou; Arslan, Tughrul; Flynn, Brian, "A reconfigurable feed network for a dual circularly polarised antenna array," 2013 IEEE 24th International Symposium on Personal Indoor and Mobile Radio Communications (PIMRC), vol., no., pp.430,434, 8-11 Sept. 2013

8.Wei, Zhou; Arslan, Tughrul, "A bidirectional planar monopole antenna array for WiFi/Bluetooth and LTE mobile applications," 2013 Loughborough Antennas and Propagation Conference (LAPC), vol., no., pp.190,193, 11-12 Nov. 2013

9.Wei, Zhou; Arslan, Tughrul, "Planar monopole antenna with Archimedean spiral slot for WiFi/Bluetooth and LTE applications," 2013 Loughborough Antennas and Propagation Conference (LAPC), vol., no., pp.186, 189, 11-12 Nov. 2013

10.Wei, Zhou; Arslan, Tughrul, "Smart antenna array for WiFi/Bluetooth and LTE applications," IEEE Transactions on Antennas and Propagation (Journal Submitted, Under Review)

Chapter 2: Novel Antenna Design for Smart Antenna Array

2.1 Introduction

This chapter discusses the design, simulation, optimisation, fabrication and characterisation of a novel antenna structure and four-element liner array geometry for smart antenna systems. The radiation pattern of an adaptive array antenna is dependent on the individual radiation pattern of the array element and also the configuration of the array.

Firstly, this chapter presents a novel miniaturised microstrip-fed planar monopole antenna with Archimedean spiral slots to cover WiFi/Bluetooth and LTE mobile applications. The fundamental structure of the proposed antenna element is a circular patch, which operates in high frequency range, for the purpose of miniaturising the circuit dimension. In order to achieve a multiband performance, Archimedean spiral slots, acting as resonance paths, have been etched on the circular patch antenna. Analysis of the current distributions on the antenna design reveals that at low frequencies, the additional of the slots create new circular current paths, which generate a wideband low frequency response. Different shapes of Archimedean spiral slots have been investigated and compared. The miniaturised and optimised antenna achieves a bandwidth of 2.2GHz to 2.9GHz covering WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) mobile standards. The proposed antenna exhibits low return loss, large gain, high efficiency and stable omni-directional radiation pattern across all the relevant bands.

An array of omni-directional antennas will generate a radiation pattern with narrow main beam. A directional antenna array is suited to systems with limited power and involving data communication with known locations. The second part of this chapter describes a four-element linear antenna array geometry utilising the planar monopole elements with

Archimedean spiral slots. All of the relevant parameters have been studied and evaluated. Different phase shifts are excited for the array elements, and the main beam scanning range has been simulated and analysed.

This chapter is divided into six sections. The antenna theory and individual antenna design are presented in Section 2.2 and Section 2.3, respectively. The proposed antenna structure is modelled in CST Microwave Studio. Section 2.4 discusses the design principles of an antenna array. Section 2.5 presents the array geometry and analyses all of the key parameters in a smart antenna system. Finally, Section 2.6 summaries the chapter.

2.2 Antenna Theory

2.2.1 Antenna Introduction

An antenna is a device for radiating or receiving radio waves. It is an essential transitional structure between guiding device (transmission line) and free-space. The guiding device takes the form of a waveguide or a coaxial line, for the purpose of transporting electromagnetic energy from the transmitting source to the antenna, or from the antenna to the receiver. Then we have a transmitting antenna in the former case and a receiving antenna in the later one. Radiation pattern is utilised to describe the electromagnetic radiation distribution of an antenna, and it is achieved by controlling the current flow on the antenna. Figure 2.1 shows the antenna operating as a transition device. There are various types of antenna configurations, as illustrated in Figure 2.2, which include wire antennas, log-periodic antennas, travelling wave antennas, aperture antennas, reflector antennas, and microstrip antennas [22].

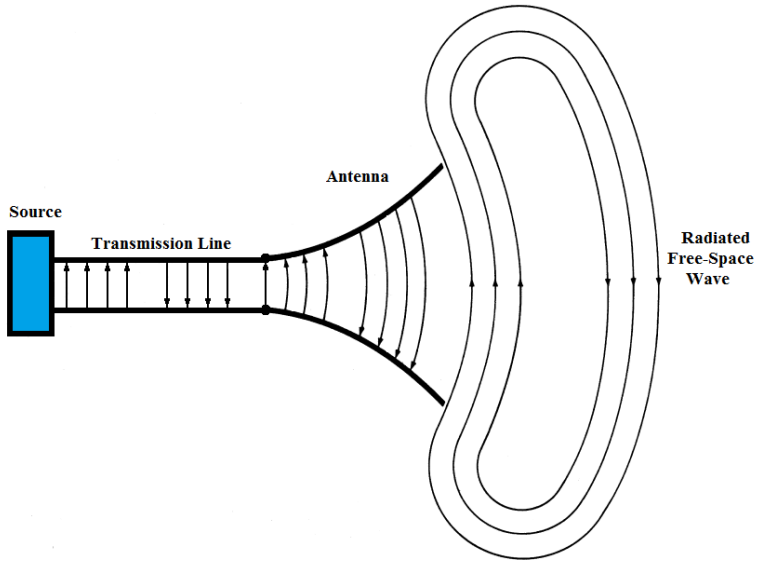
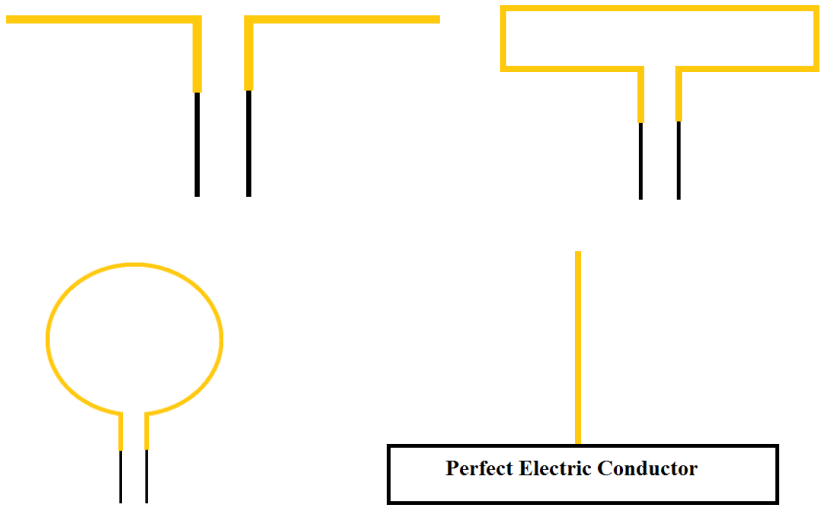
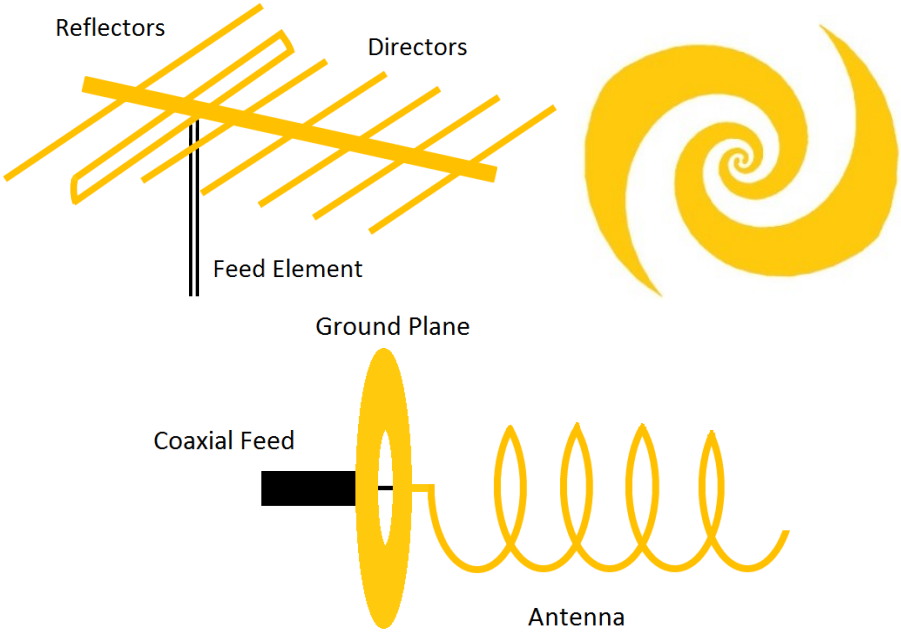


Figure 2.1: Antenna Operates as a Transition Device [22]

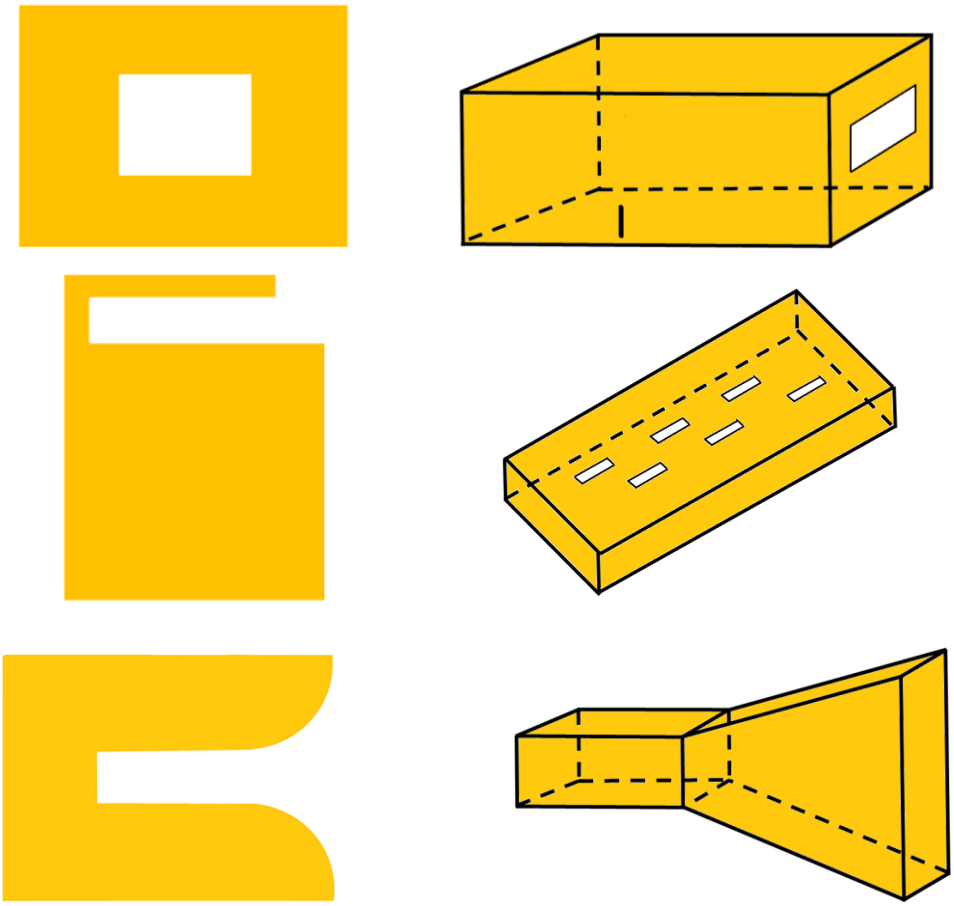


(a) Wire Antenna Configurations: Dipole Antenna, Folded Dipole Antenna, Circular Loop Antenna and Monopole Antenna

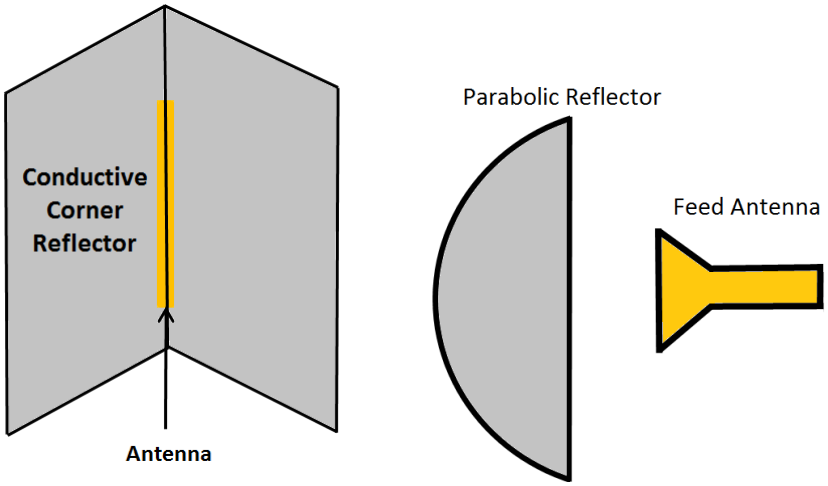
(b) Log-Periodic Antennas: Log Periodic Tooth Antenna



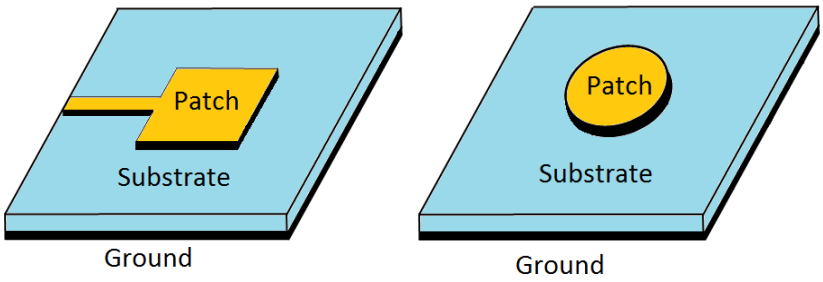
(c) Travelling Wave Antennas: Yagi-Uda Antenna, Spiral Antenna and Helical Antenna



(d) Aperture Antennas: Slot Antenna, Cavity-Backed Slot Antenna, Inverted-F Antenna, Slotted Waveguide Antenna, Vivaldi Antenna and Horn Antenna



(e) Reflector Antennas: Corner Reflector Antenna and Parabolic Reflector Antenna



(f) Microstrip Antennas: Rectangular Patch Antenna and Circular Patch Antenna

Figure 2.2: Antenna Types: (a) Wire Antennas, (b) Log-Periodic Antennas, (c) Travelling Wave Antennas, (d) Aperture Antennas, (e) Reflector Antennas, and (f) Microstrip Antennas

2.2.2 Antenna Properties

The transmission-line Thevenin equivalent circuit of a transmitting antenna is presented in Figure 2.3 [22].

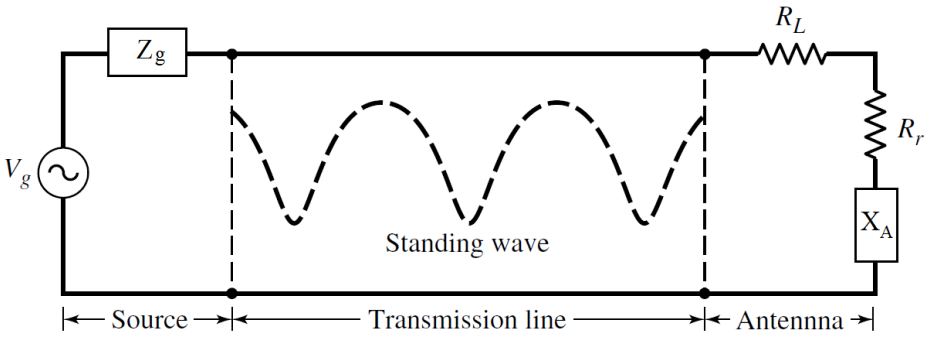


Figure 2.3: Transmission-Line Thevenin Equivalent of a Transmitting Antenna [22]

An ideal signal generator is used as the source and the transmission line is represented by a line with characteristic impedance of Z_C. The impedance of antenna, Z_A is given by the following equations:

$$Z_A = R_A + jX_A \tag{2.1}$$

$$R_A = R_L + R_r \tag{2.2}$$

Where, R_A refers to the antenna resistance. R_L is the loss resistance, which includes the conduction loss and dielectric loss. R_r stands for the radiation resistance and X_A is the antenna reactance.

By matching the antenna impedance Z_A and the transmission line characteristic impedance Z_C, the standing wave is decreased, and the energy storage capacity of the transmission line is

minimised [22]. As a result, the maximum power is delivered from the source to the antenna. This condition is calculated by conjugate matching:

$$R_g = R_A = R_L + R_r \tag{2.3}$$

$$X_g = -X_A \tag{2.4}$$

Where, R_g is the source resistance, R_A presents the antenna resistance, X_g describes the source reactance, and X_A is the antenna reactance.

Practically, the power reflected by the antenna, as shown above, is represented using S-Parameters. S-Parameters show the relationship between input power and output power for electrical systems. S_{11} is defined as reflection coefficient, which describes the reflected power from the antenna.

2.2.3 Antenna Fundamental Parameters

2.2.3.1 Radiation Pattern

The radiation properties of an antenna as a function of space coordinates can be mathematically or graphically represented by its radiation pattern [23]. Radiation properties include radiation intensity, power flux density, field strength, phase, directivity and polarisation. Generally, there are three types of antenna radiation patterns: isotropic, directional and omni-directional. Isotropic radiation pattern is created when a theoretical lossless antenna has equal radiation in all directions. Antenna with uniform radiation is in an ideal case, and it is not physically realisable. However, the isotropic radiation is often utilised as a reference to analysis the directive properties of actual antennas [22] . An antenna which radiates or receives more electromagnetic waves in some directions than in others is defined as a directional antenna. Various portions of a directional radiation pattern are represented by lobes, which may be classified into main lobe, minor lobe, side lobe, and back lobe (as shown in Figure 2.4). The lobe containing the strongest radiation intensity is defined as the main lobe (also called major lobe), while the rest are side lobes. Beam width of the main lobe is calculated using the angular separation between the half-power (3dB) points, also known as the half-power beamwidth (HPBW). A minor lobe is any lobe except the main lobe. A back lobe refers to a minor lobe which occupies the opposite direction of the main lobe. Minor lobes show radiations in undesired directions, and they will be minimised in the design procedure. Normally, side lobes are the largest minor lobes. Side lobe level (or side lobe ratio) are used to express the ratio of the power density between the side lobe and main lobe. Low side lobe level is very important requirement in smart antenna array designs. Finally, an

omni-directional radiation patten is a special type of a directional pattern, which generates a non-directional pattern in a given plane and a directional pattern in any orthogonal plane [22].

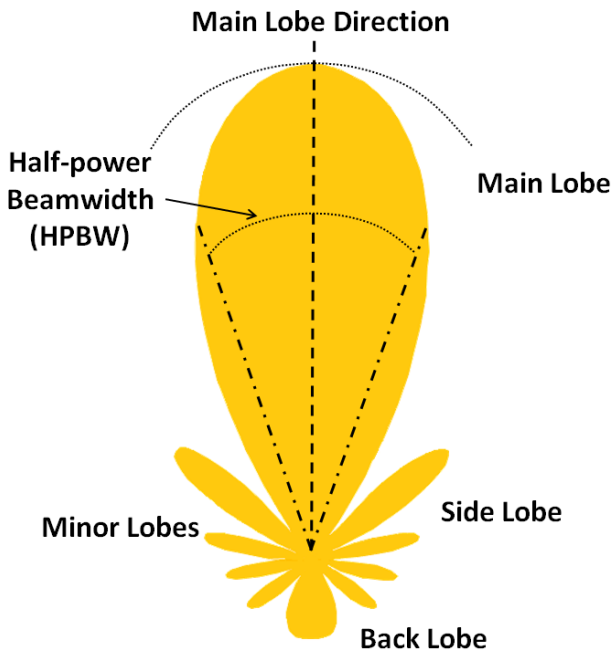


Figure 2.4: Directional Radiation Pattern

2.2.3.2 Field Regions

The antenna radiation area is divided into three regions: (a) reactive near-field region, (b) radiating near-field (Fresnel) region and (c) far-field (Fraunhofer) region, as presented in Figure 2.5. There are different preferences among the three regions. Reactive near-field region is the area immediately surrounding the antenna, and the distance is determined by $R_1 < 0.62\sqrt{D^3/\lambda}$, where D is the largest antenna dimension and λ stands for the wavelength. Radiating near-field (Fresnel) region is the portion between the reactive near-field region and the far-field region, wherein the angular field distribution is according to the distance from the antenna. The inner boundary is the space $R \geq 0.62\sqrt{D^3/\lambda}$ and the outer boundary is the distance $R < 2D^2/\lambda$. Far-field (Fraunhofer) region is the antenna radiation space where the angular field distribution is completely independent of the radial distance from the antenna. The distance is estimated by $R_2 \geq 2D^2/\lambda$.

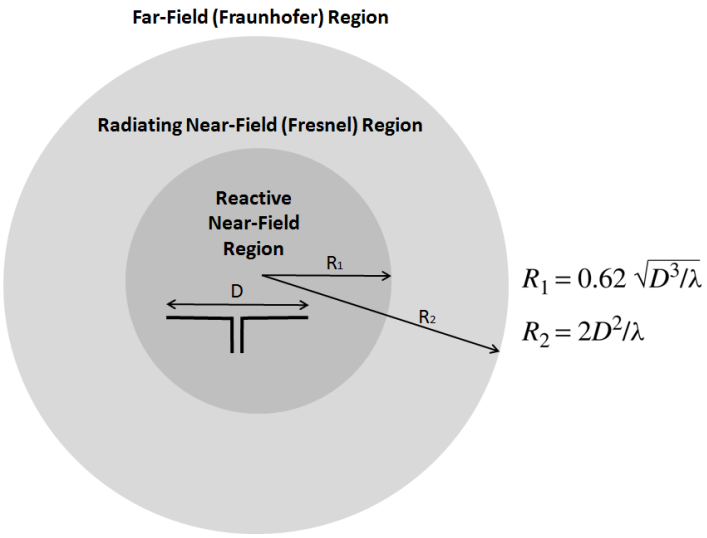


Figure 2.5: Antenna Radiation Field Regions [22]

2.2.3.3 Radiation Power Density

The average power radiated by an antenna in a particular direction is defined as the radiation power density, P_r (Watts/m^2). It is estimated using the time averaging Poynting vector. The following equation describes the relationship between power density and field intensities.

$$P_r(r,\theta,\phi) = \frac{1}{2}[E \times H^*] = \frac{1}{2\eta}|\overline{E}(r,\theta,\phi)|^2 \quad (2.5)$$

Where, E represents the electric field intensity, H refers to the magnetic field intensity, and η is the intrinsic impedance.

2.2.3.4 Radiation Intensity

Antenna radiation power per unit solid angle is defined as the radiation intensity, U (Watts/unit solid angle), as expressed in Equation (2.6).

$$U = r^2 P_r \quad (2.6)$$

Where, r is the distance to the antenna, and P_r stands for the radiation power density.

The total power radiated by an antenna, P_{rad}, is obtained by integrating the radiation intensity over the entire solid angle of 4π, as given in Equation (2.7).

$$P_{rad} = \oiint_{\Omega} U d\Omega = \int_0^{2\pi}\int_0^{\pi} U sin\theta d\theta d\phi \quad (2.7)$$

Where, dΩ is the element of solid angle, and $d\Omega = sin\theta d\theta d\phi$.

2.2.3.5 Directivity

The antenna directivity is the ratio of a particular direction's radiation intensity, to the average radiation intensity over all directions. The average radiation intensity is estimated using the total power radiated divided by 4π. The directivity of a non-isotropic antenna is the ratio of its radiation intensity in a specified direction over that of an isotropic antenna, as expressed in Equation (2.8).

$$D = \frac{U}{U_0} = \frac{4\pi U}{P_{rad}} \tag{2.8}$$

Where, P_{rad} is the total radiated power. When the direction is not clarified, the antenna directivity means the direction of maximum radiation intensity.

$$D_{max} = \frac{U_{max}}{U_0} = \frac{4\pi U_{max}}{P_{rad}} \tag{2.9}$$

2.2.3.6 Gain

Gain of an antenna is the ratio of radiation intensity in a specified direction, to the radiation intensity from an isotropic radiator with the same power feed to it. Isotropical radiated power equals to the antenna input power divided by 4π [23]. Compared to the antenna directivity, the antenna gain parameter also takes into account the antenna efficiency and directional capabilities. The following equation (2.10) describes the gain calculation [22] .

$$Gain = 4\pi \frac{Radiation\ Intensity}{Total\ Input\ Power} = 4\pi \frac{U(\theta,\phi)}{P_{in}} \tag{2.10}$$

Equation 2.11 describes the relationship between antenna radiation gain and directivity.

$$G(\theta, \phi) = e_{cd} D(\theta, \phi) \tag{2.11}$$

Where, e_{cd} stands for the radiation efficiency and it will be described in the following section.

2.2.3.7 Antenna Efficiency

The total antenna efficiency e_0 is utilised to describe losses at the input terminals and within the antenna structure. The losses are generally caused by two mechanisms: reflections because of the mismatch between the antenna and transmission line; conduction and dielectric losses (I^2R). Figure 2.6 illustrates the antenna terminals and losses.

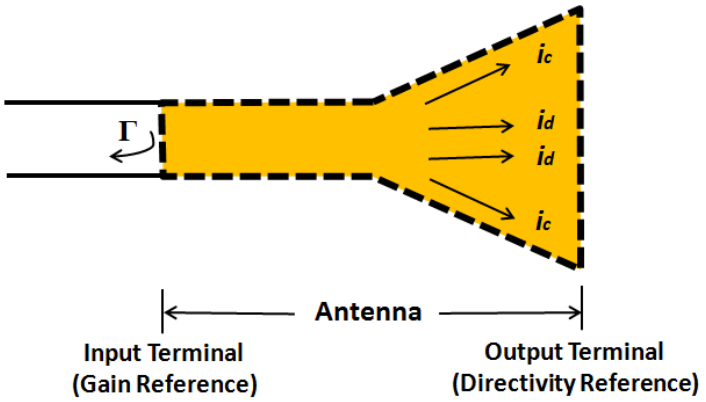


Figure 2.6: Antenna Terminals and Losses

The total efficiency e_0 is achieved using Equation 2.12.

$$e_0 = e_r e_c e_d \tag{2.12}$$

Where, e_r is the reflection (mismatch) efficiency, and $e_r = (1 - |\Gamma|^2)$. Γ stands for the voltage reflection coefficient at the antenna input terminals, and $\Gamma = (Z_A - Z_C)/(Z_A + Z_C)$, where Z_A is the antenna input impedance, and Z_C shows the characteristic impedance of transmission line.e_c represents the conduction efficiency. e_d describes the dielectric efficiency.

$$VSWR = Voltage\ Standing\ Wave\ Ratio = \frac{1+|\Gamma|}{1-|\Gamma|} \tag{2.13}$$

e_{cd} is defined as the antenna radiation efficiency.

$$e_{cd} = e_c e_d = \frac{P_{rad}}{P_{in}} \tag{2.14}$$

Where, P_{rad} is the total radiated power and P_{in} is the total input power to the antenna.

2.2.3.8 Beam Efficiency

Another parameter is used to describe the transmitting and receiving antenna performance: beam efficiency (BE). It is the ratio of power transmitted (received) within cone angle θ_1, to the power transmitted (received) by the antenna, as expressed in the following formula:

$$BE = \frac{\int_0^{2\pi}\int_0^{\theta_1} U(\theta,\phi) Sin\theta d\theta d\phi}{\int_0^{2\pi}\int_0^{\pi} U(\theta,\phi) Sin\theta d\theta d\phi} \tag{2.15}$$

2.2.3.9 Polarisation

Antenna polarisation describes the instantaneous electric field orientation of the propagated electromagnetic wave, as presented in Figure 2.7. It is a far-field characteristic of electromagnetic waves radiated by all practical antennas. In general, polarisations can be categorised into linear, circular, or elliptical. In linear polarised mode, the electric field vector is always directed along a line, as illustrated in Figure 2.7. If the antenna radiates an electromagnetic wave in a corkscrew pattern and performs a complete revolution in each wavelength, this radiation is defined as circularly polarisation. The figure of the electric field is traced either in a clockwise (Right-Hand Circularly Polarised, RHCP), or counter-clockwise (Left-Hand Circularly Polarised, LHCP) sense. When the electric field traces is an ellipse, the radiation is classified as elliptical polarisation. Linearly and circularly polarised antenna patterns are special cases of elliptical polarisation, and they can be achieved when the ellipse becomes a straight line or a circle, respectively.

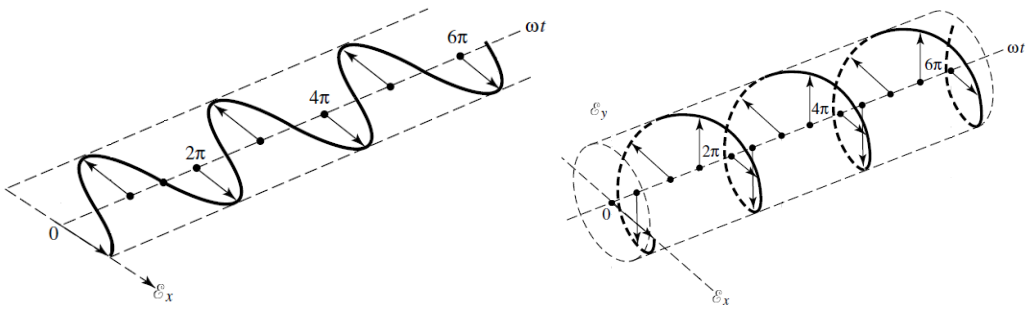


Figure 2.7: Linear Polarisation and Circular Polarisation

2.3 Novel Planar Monopole Antenna Design with Archimedean Spiral Slots

2.3.1 Introduction

With the rapid development of wireless technology innovation, compact size, low-profile, lightweight, wideband, and multiple functional antenna designs are becoming more attractive in many microwave applications. Planar monopole antenna structures have been investigated in order to fulfil these requirements. The monopole antennas demonstrate many advantages, including simple fabrication, low cost, wide impedance bandwidth, omni-directional radiation properties, and transmitting and receiving wideband signals without significant distortions [24, 25] . Numerous monopole antennas have been investigated employing various ground plane sizes and monopole radiating elements of different shapes, including squares, rectangles, trapezoids, circles and ellipses [26-28].

There are two main approaches in the literature to achieve multiband planar monopole antennas. In the first method, an antenna element is designed to cover a wide bandwidth. The low frequency limitation will increase the size of the antenna. Some notches are introduced into the antenna in order to create the multiband behaviour, as presented in [29]. An ultra wideband printed monopole antenna with a modified ground plane has been studied. By adding a pair of L-shaped slots in the ground plane, additional resonances are excited and hence the bandwidth is increased up to 130% (in Figure 2.8). By properly adjusting the dimensions of the capacitive-coupled elements, the lower-edge frequency of the band can also be decreased. Because the additional capacitive loads change the equivalent circuit model of the antenna and also generate more current flow in the lower frequency bands. The resonant frequency bandwidth is even wider.

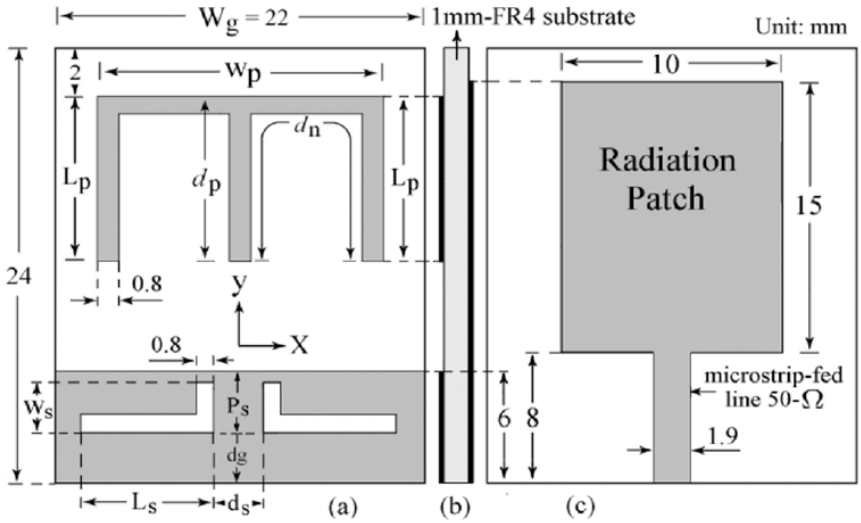


Figure 2.8: UWB Printed Monopole Antenna with a Pair of L-Shaped Slots [29]

With the second technique, a compact antenna can be designed to cover high frequencies. The lower frequency bands are created by adding extra resonant elements to the main antenna structure [30]. Figure 2.9 illustrates an antenna configuration integrating Bluetooth and UWB frequencies. The main rhombus radiating patch has been designed to cover UWB frequency (3.1GHz-10.6GHz). Additional arms have been added for the lower Bluetooth (2.45GHz) application. The combined structure is able to operate both in high UWB and low Bluetooth bands. Spirals are able to slow down the wave travelling within the antenna structure and hence they have been widely used in the second technology, and also for the purpose of furthermore miniaturisation [31].

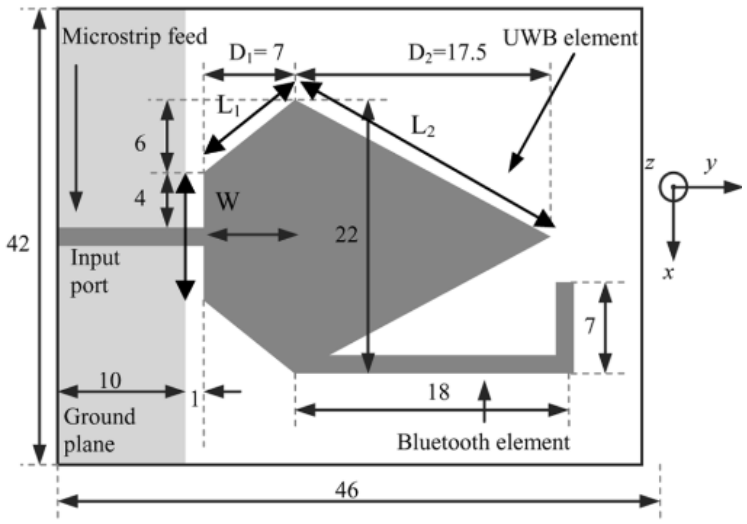


Figure 2.9: Microstrip-Fed Integrated Bluetooth/UWB Antenna [30]

The Archimedean two-wire spiral antenna is a traditional configuration which belongs to the family of frequency independent antennas. They are capable of operating over multiband frequencies while maintaining stable radiation patterns [32]. The conventional Archimedean spiral antennas utilising a perfect electric conducting (PEC) ground plane placed at a distance of λ/4 below the antenna, to generate a unidirectional beam (as presented in Figure 2.10). This technique introduces a fixed physical length between the ground plane and the antenna in terms of λ, and therefore seriously limiting the frequency independent characteristics [33, 34]. Moreover, the Archimedean spiral antennas have relatively complex feeding structure and unfixed phase centre, as a result, significant distortion will occur when transmitting and receiving wideband signals [35].

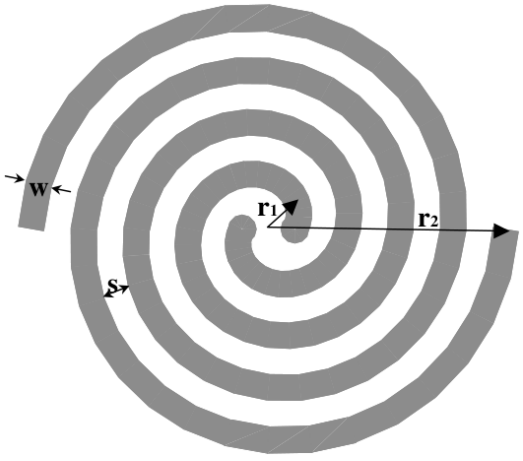


Figure 2.10: Conventional Archimedean Spiral Antenna Structure

In this section, the monopole and Archimedean spiral technologies are combined. Several Archimedean spiral shaped slots are etched on a circular patch antenna, and using microstrip-fed in order to achieve miniaturised dimensions, multiband operating frequencies, high efficiency, large gain and stable radiation patterns. Five different kinds of Archimedean spiral slot shapes have been investigated and compared. Full-wave simulations were carried out using finite-difference time-domain (FDTD) method based software, namely CST Microwave Studio. Moreover, the simulations were validated through a real fabrication with the measured results agreeing with simulated results.

2.3.2 Antenna Structure Design

Radiating patches of printed antennas have a variety of forms, including square, rectangular, triangular, circular and elliptical. It has been investigated that circular configuration achieve smaller dimensions related with the operating frequency. Furthermore, the only control variable for the structure is the patch radius, which makes the circular or disk antennas are easy to be calculated and designed. The proposed antenna structure is based on a circular patch, and the geometry is depicted in Figure 2.11. Since the substrate height h is very small (typically h<0.05λ), the radius of the patch is calculated based on circular TM_{11} mode resonance, and using Equations 2.16 and 2.17 [22].

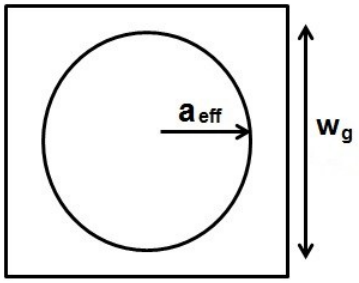


Figure 2.11: Geometry of the Fundamental Antenna

$$(f_r)_{mn0} = \frac{1}{2\pi\sqrt{\mu\varepsilon}}\left(\frac{x'_{mn}}{a}\right) = \frac{1.8412}{2\pi a\sqrt{\mu\varepsilon}} \tag{2.16}$$

$$x'_{mn} = 2\pi a\sqrt{\frac{\varepsilon_\gamma}{\lambda_0}} \tag{2.17}$$

Where x'_{mn} represents zero of the derivative of the Bessel function which determines the order of resonant frequency, f_{mn}. The value of x'_{11} is 1.8412 for TM_{11} mode analysis. The circular patch effective radius, a_{eff}, which including fringing effects, to replace the actual radius a, is referred to Equation (2.18)

$$a_{eff} = a\left\{1 + \frac{2h}{\pi a \varepsilon_\gamma}\left[ln\left(\frac{\pi a}{2h}\right) + 1.7726\right]\right\}^{1/2} \tag{2.18}$$

Therefore, the resonant frequency for the TM_{11} mode has been modified by using Equation (2.18) and expressed as:

$$(f_{rc})_{110} = \frac{1.8412 v_0}{2\pi a_e \sqrt{\varepsilon_r}} \tag{2.19}$$

Where, v_0 is the speed of light in free-space.

The substrate size, w_g is optimised in order to minimise the fringing effect and, simultaneously, to achieve the best reflection coefficient.

The feeding technique for the proposed antenna structure is a microstrip line. This feeding method has advantages over others, like testing point (coaxial connector) and coplanar feed, because it creates an easy approach to integrate with a printed circuit board. Furthermore, it can be utilised separately from the main circuit using a coaxial connector [15, 36].

The microstrip dimensions are calculated using the formulas in (2.20) to (2.22) [37].

$$\frac{W}{d} = \begin{Bmatrix} {8e^A}/{e^{2A} - 2}, \frac{W}{d} \leq 2 \\ \frac{2}{\pi}\left\{B - 1 - ln(2B-1) + \frac{\varepsilon_\gamma - 1}{2\varepsilon_\gamma}\left[ln(B-1) + 0.39 - \frac{0.61}{\varepsilon_\gamma}\right]\right\}, \frac{W}{d} > 2 \end{Bmatrix} \tag{2.20}$$

Where:

$$A = \frac{Z_0}{60}\sqrt{\frac{\varepsilon_\gamma + 1}{2}} + \frac{\varepsilon_\gamma - 1}{\varepsilon_\gamma + 1}\left(0.23 + \frac{0.11}{\varepsilon_\gamma}\right) \tag{2.21}$$

$$B = \frac{377\pi}{2Z_0\sqrt{\varepsilon_\gamma}} \tag{2.22}$$

Since the dielectric substrate thickness is very thin compared with the wavelength ($h << \lambda$), a quasi-TEM mode has been used for the microstrip line analysis. The characteristic impedance Z_0 (50Ω) can be rewritten here in Equations (2.23) and (2.24).

$$Z_0 = \frac{60}{\sqrt{\varepsilon_e}} ln\left(\frac{8h}{w_m} + \frac{w_m}{4h}\right) \tag{2.23}$$

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_e}\left[{w_m}/{h} + 1.393 + 0.667\, ln\left({w_m}/{h} + 1.444\right)\right]} \tag{2.24}$$

Where, w_m represents width of the transmission line, and h is the thickness of the substrate. ε_e presents the effective dielectric constant which is given by:

$$\varepsilon_e = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2\times\sqrt{1+12h/w_m}} \quad (2.25)$$

Where, ε_r shows the dielectric constant of the substrate. In the implementation, copper track with a conductivity of 5.89×10^7 has been etched on an FR4 printed circuit board (with a thickness h=1.6mm, and relative dielectric constant ε_r=4.55). The resonant frequency for the base circular patch is 3GHz in order to miniaturise the antenna dimension. From calculation, radius of the circular should be around 16mm. The substrate dimension w_g is near 38mm. The width of the feed line w_m is 3mm and length of the feed line is around 5mm. The base antenna structure has been further optimised in CST Microwave Studio, for the purpose of achieving a suitable reflection coefficient.

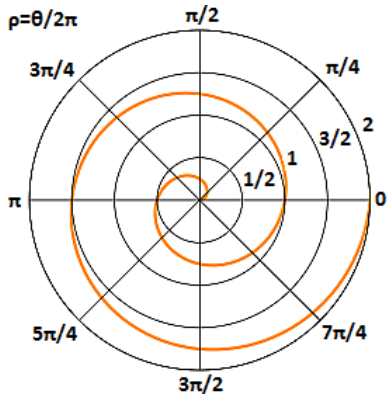


Figure 2.12: Archimedean Spiral Represented on a Polar Graph

Archimedean spiral slots are etched on the microstrip patch antenna, in order to increase circular current paths, which generate a wideband low frequency response. Figure 2.12 demonstrates the Archimedean spiral represented on a polar graph. The Archimedean spiral curve is defined by the polar equation $r=\alpha\theta$, with $\theta\geq 0$. The system of parametric equations corresponding to the polar graph is $x=\alpha\theta\cos(\theta)$ and $y=\alpha\theta\sin(\theta)$, where α represents any real number denoting the growth rate of the spiral. Figure 2.13 depicts the proposed antenna structure.

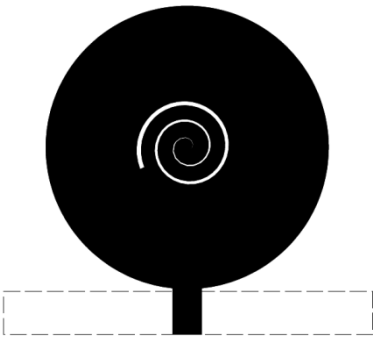


Figure 2.13: Geometry of the Proposed Antenna

In a Cartesian coordinate system, the Archimedean spiral slots are generated using the following formulas.

$$X = t \times 10 \times cos\,(^{t}/_{10} - 1) \times 360 \quad (2.26)$$

$$Y = t \times 10 \times sin\,(^{t}/_{10} - 1) \times 360 \quad (2.27)$$

$$Z=0 \quad (2.28)$$

Where, t is a variable representing the distance between the circular patch centre and the Archimedean spiral slots. By varying the value of t, different geometries of Archimedean spiral slots could be obtained. The planar monopole antennas with Archimedean spiral slots have been designed, calculated, simulated and optimised using finite-difference time-domain (FDTD) method based software, Advanced Design System (ADS) and CST Microwave Studio, for full-wave analysis.

2.3.3 Equivalent Circuit of the Antenna Structure

A simplified lumped element circuit model of the planar monopole antenna with Archimedean spiral slots has been derived. This model was achieved by studying the scattering parameter (S_{11}) of the antenna structure and simulating the antenna in an EM simulator. By obtaining the S-Parameter, the general structure of the circuit model has been transformed to imply the characteristics of the antenna.

The equivalent circuit of the base circular patch antenna is illustrated in Figure 2.14, where the patch cavity is modelled as a parallel RLC circuit, while the probe inductance is represented by a series inductor.

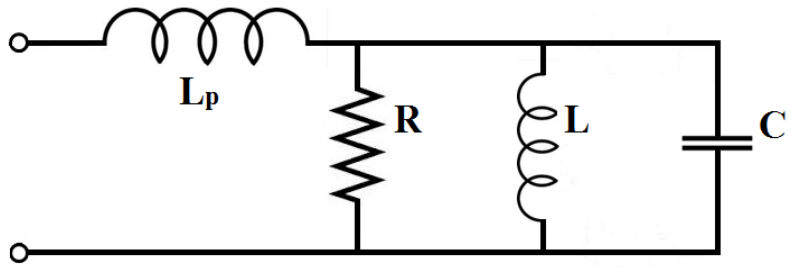


Figure 2.14: Equivalent Circuit of the Patch Antenna

When a notch is incorporated into the patch antenna, the resonance features change. The equivalent circuit for an Archimedean spiral slot in Figure 2.13 is modelled as a parallel LC circuit (L_s and C_s) [38].

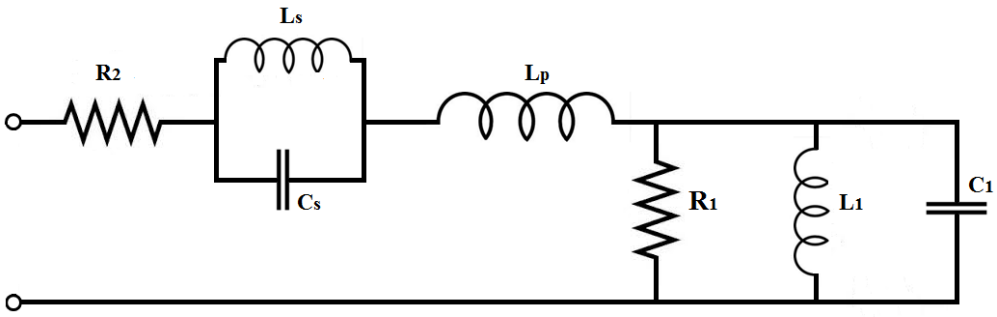


Figure 2.15: Equivalent Circuit of the Planar Monopole Antenna with Archimedean Spiral Slots

Figure 2.15 illustrates the equivalent circuit of the proposed planar monopole antenna with Archimedean spiral slots. The component values and reflection coefficient can be calculated using the following equations. Moreover, for the calculation of input impedance, the circuit model has been simplified using Equation 2.30 and 2.31.

$$\Gamma = \frac{Z_0 - Z_{in}}{Z_0 + Z_{in}} \tag{2.29}$$

$$Z_{in} = R_2 + \frac{\left({}^{1}/_{j\omega C_s}\right) j\omega L_s}{\left({}^{1}/_{j\omega C_s}\right) + j\omega L_s} + j\omega L_p + \frac{R_1\left({}^{1}/_{j\omega C_1}\right) j\omega L_1}{R_1\left({}^{1}/_{j\omega C_1}\right) + \left({}^{1}/_{j\omega C_1}\right) j\omega L_1 + R_1 j\omega L_1} \tag{2.30}$$

From the above equations and assuming Z_{in} is 50Ω, all of the resistance, inductance and capacitance could be calculated. Finally, in the equivalent circuit, R_1=50Ω, L_1=2nH, C_1=0.9pF, R_2=50 Ω, L_p=0.5nH, L_s=1.2nH and C_s=6.4pF. The circuit model has been built and simulated in Advanced Design System. Figure 2.16 shows the equivalent circuit diagram.

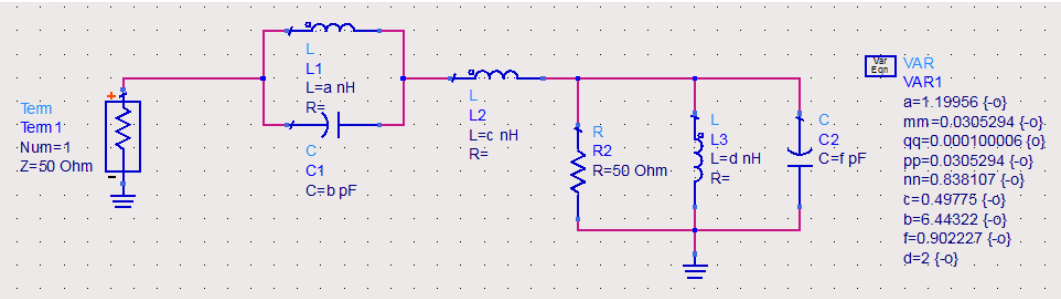


Figure 2.16: Equivalent Circuit of the Planar Monopole Antenna with Archimedean Spiral Slots in ADS

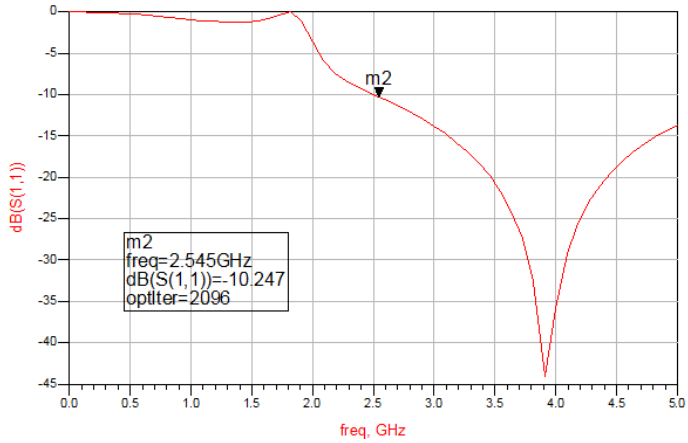


Figure 2.17: Simulation Results of the Antenna Equivalent Circuit in ADS

Figure 2.17 presents the simulation results for the antenna equivalent circuit in ADS. By varying the values of C_s and L_s, the Archimedean spiral slots dimensions are changed, which generates difference resonate frequency performance. The equivalent circuit in Figure 2.16 is based on the antenna model in Figure 2.18 (t=0~0.5mm). Similar antenna structure has also been modelled in CST Microwave Studio, for full wave analysis. Figure 2.19 (CST Model) shows the similar simulation results as in Figure 2.17 (Equivalent Circuit), which guarantees the component values in the equivalent circuit are all suitable.

2.3.4 Simulation and Experimental Results

Based on the above design procedures, five monopole antennas with Archimedean spiral slots are developed and simulated in CST Microwave Studio. Furthermore simulations for circular patch radius, transmission line length, Archimedean spiral slots shapes and substrate dimensions are made in order to optimise the reflection coefficient and radiation patterns.

For the finalised antenna geometry, the radius of the circular patch is 15mm and the dimension of the substrate is 35mm ×35mm. By controlling the value of t in formulas (2.26) to (2.28), there is a variation of the Archimedean spiral slot shapes, generating different antenna performance. The planar monopole antennas are implemented on a single FR4 substrate with the relative dielectric constant ε_γ=4.55, loss tangent $\delta = 0.025$ and the thickness of 1.6mm.

In Figure 2.18, the range of the parameter t is from 0 to 0.5mm, leading a small Archimedean spiral slots with number of turn, N=3. Figure 2.21 presents the monopole antenna with longer spiral slots, utilising parameter t increasing to 1mm, which raises the turn number N=5. When the range of t is between 0 and 1.3mm, the Archimedean spiral slots are the longest for the circular patch, and its structure is depicted in Figure 2.24. Figure 2.19, Figure 2.22 and Figure 2.25 illustrate the simulated surface current distributions and reflection

coefficients for the proposed antenna structures. Figure 2.20, Figure 2.23 and Figure 2.26 present the H-Plane and E-Plane antenna radiation patterns, which correspond to x-z (Phi=0°) and y-z planes (Phi=90°), for t=0~0.5mm, t=0~1mm and t=0~1.3mm, at 2.45GHz and 2.6GHz, respectively.

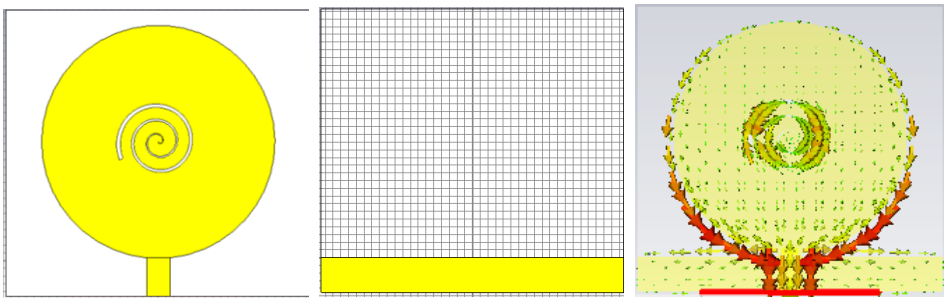


Figure 2.18: Planar Monopole Antenna with Archimedean Spiral Slots (t = 0~0.5mm), Front View, Back View, and its Corresponding Surface Current Distribution

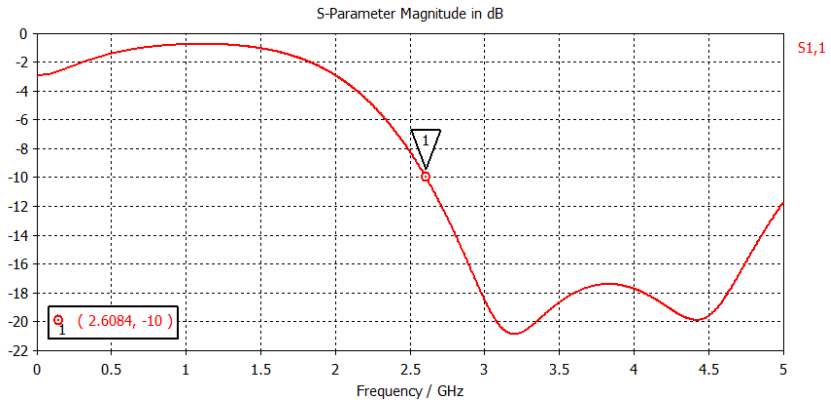


Figure 2.19: Simulated Reflection Coefficient of the Planar Monopole Antenna with Archimedean Spiral Slots (t = 0~0.5mm)

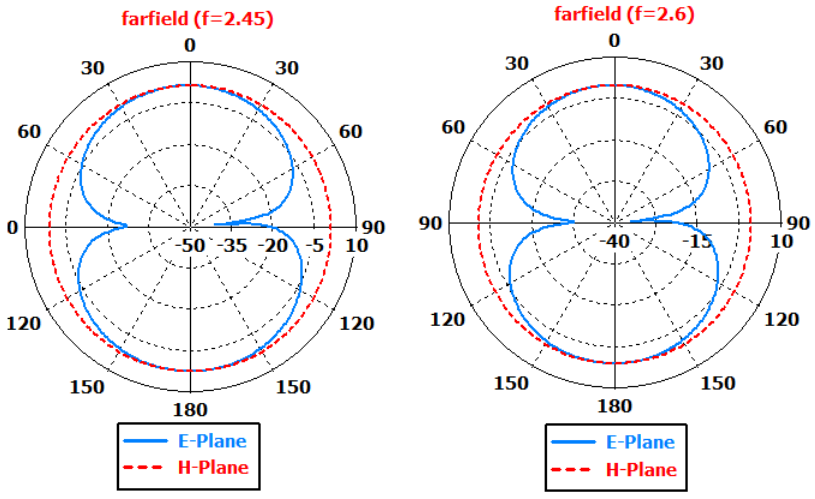


Figure 2.20: Simulated Radiation Pattern of the Planar Monopole Antenna with Archimedean Spiral Slots (t = 0~0.5mm), at 2.45GHz and 2.6GHz, in E-Plane and H-Plane

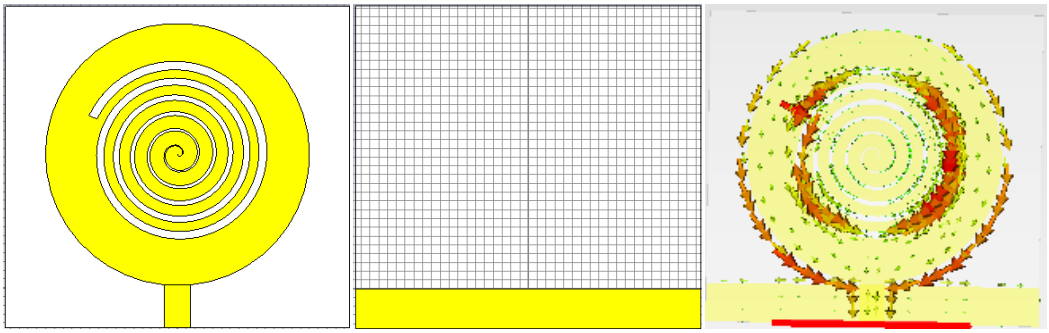


Figure 2.21: Planar Monopole Antenna with Archimedean Spiral Slots (t = 0~1mm), Front View, Back View, and its Corresponding Surface Current Distribution

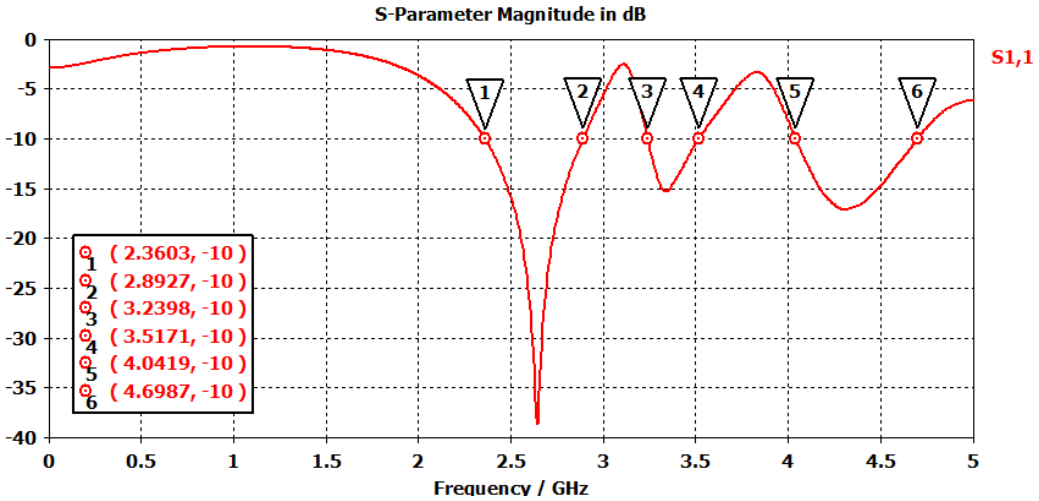


Figure 2.22: Simulated Reflection Coefficient of the Planar Monopole Antenna with Archimedean Spiral Slots (t = 0~1mm)

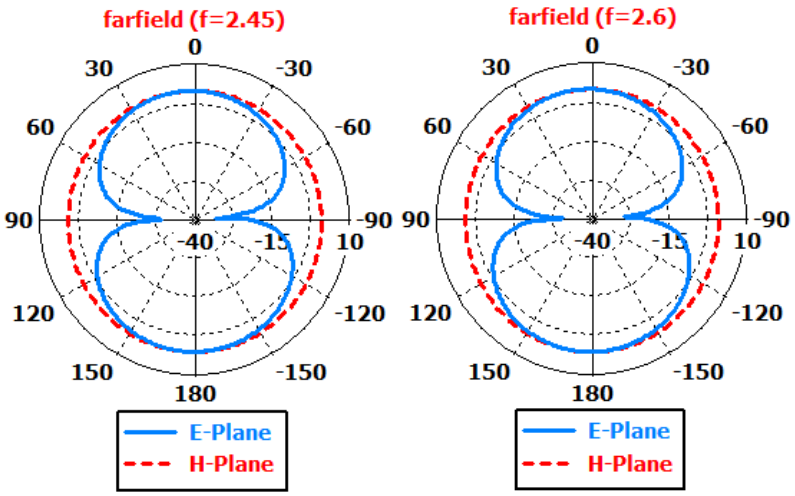


Figure 2.23: Simulated Radiation Pattern of the Planar Monopole Antenna with Archimedean Spiral Slots (t = 0~1mm), at 2.45GHz and 2.6GHz, in E-Plane and H-Plane

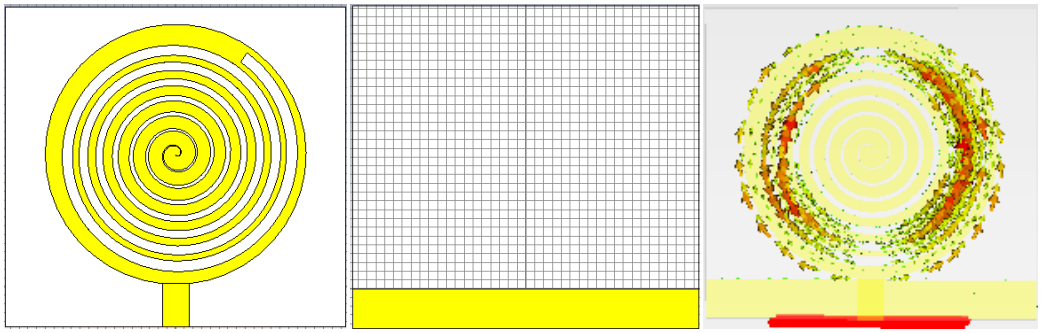


Figure 2.24: Planar Monopole Antenna with Archimedean Spiral Slots (t = 0~1.3mm), Front View, Back View, and its Corresponding Surface Current Distribution

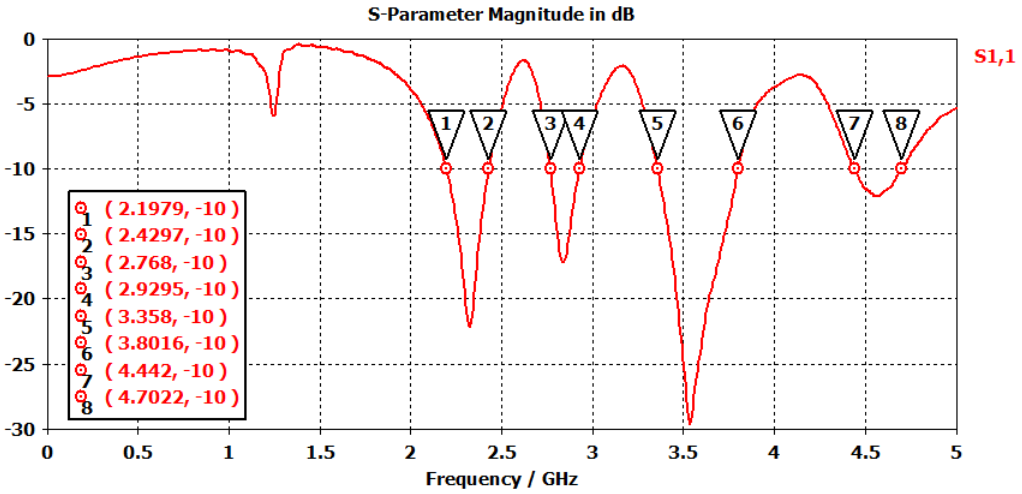


Figure 2.25: Simulated Reflection Coefficient of the Planar Monopole Antenna with Archimedean Spiral Slots (t = 0~1.3mm)

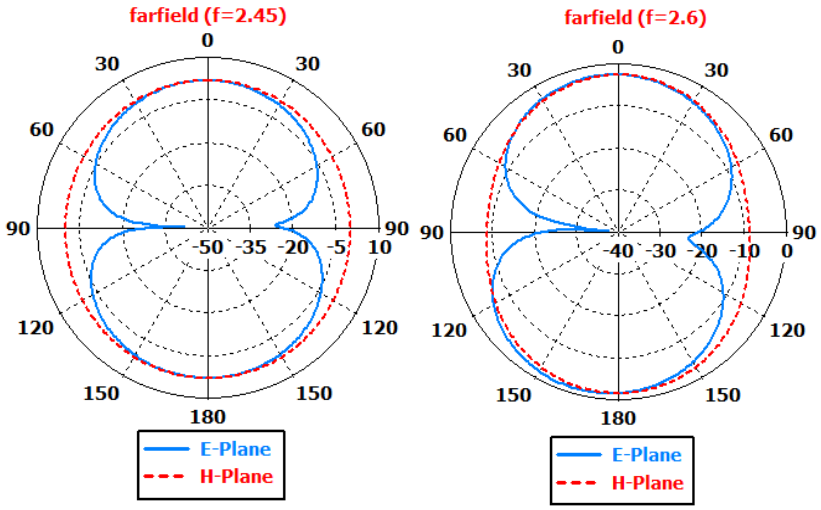


Figure 2.26: Simulated Radiation Pattern of the Planar Monopole Antenna with Archimedean Spiral Slots (t = 0~1.3mm), at 2.45GHz and 2.6GHz, in E-Plane and H-Plane

By applying Archimedean spiral slots to the circular patch antenna, the resonant frequency is shifted to lower band. Multiband and wideband antenna performance have been obtained. When the parameter t is from 0 to 0.5mm (as shown in Figure 2.19), the resonant frequency is from 2.6GHz to 5GHz. Figure 2.22 demonstrates a wideband performance from 2.36GHz to 2.89 GHz if the parameter t is varying from 0 to 1mm. In Figure 2.25, the antenna presents a multiband frequency performance, covering 2.19GHz to 2.43GHz, 2.76GHz to 2.92GHz, 3.35GHz to 3.8GHz and 4.44GHz to 4.7GHz.

Another important design parameter is the positions of Archimedean spiral slots. The variations of reflection coefficients with the positions of Archimedean spiral slots are shown in Figure 2.27 to Figure 2.32. By changing the range of parameter t, the Archimedean spiral slots could be created either in the centre or near the circular edge. The curves demonstrate that, the reflection coefficient improves as the Archimedean spiral slots start further from the centre, and that the resonant frequency also increases. It is also noted that the bandwidth decreases with the larger distance of Archimedean spiral slots.

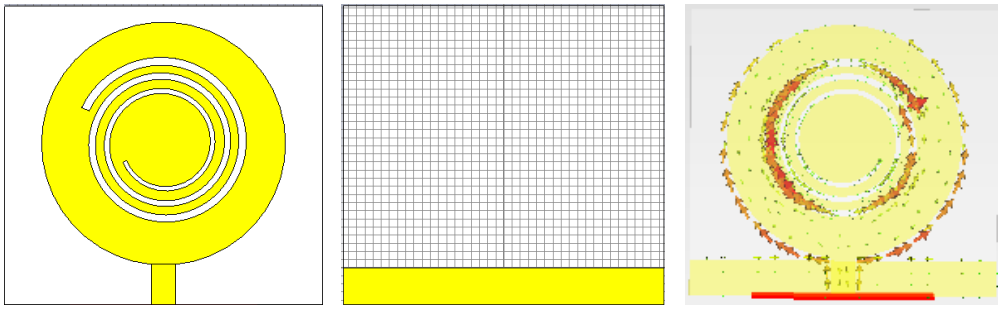


Figure 2.27: Planar Monopole Antenna with Archimedean Spiral Slots (t = 0.5~1mm), Front View, Back View, and its Corresponding Surface Current Distribution

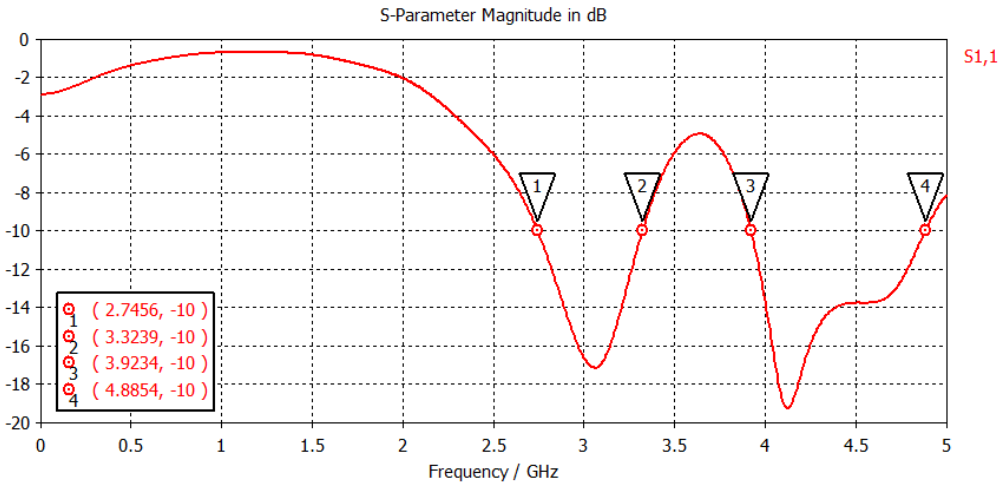


Figure 2.28: Simulated Reflection Coefficient of the Planar Monopole Antenna with Archimedean Spiral Slots (t = 0.5~1mm)

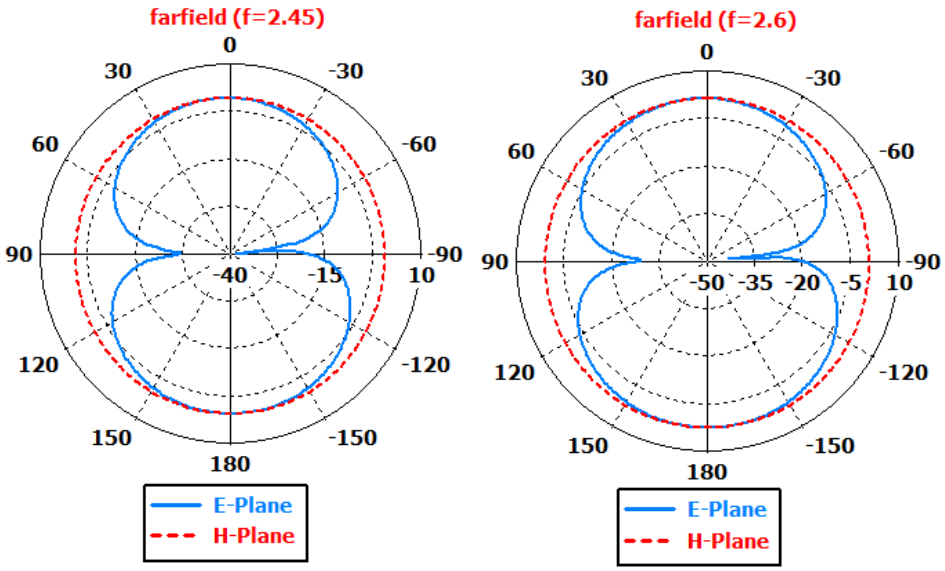


Figure 2.29: Simulated Radiation Pattern of the Planar Monopole Antenna with Archimedean Spiral Slots (t = 0.5~1mm), at 2.45GHz and 2.6GHz, in E-Plane and H-Plane

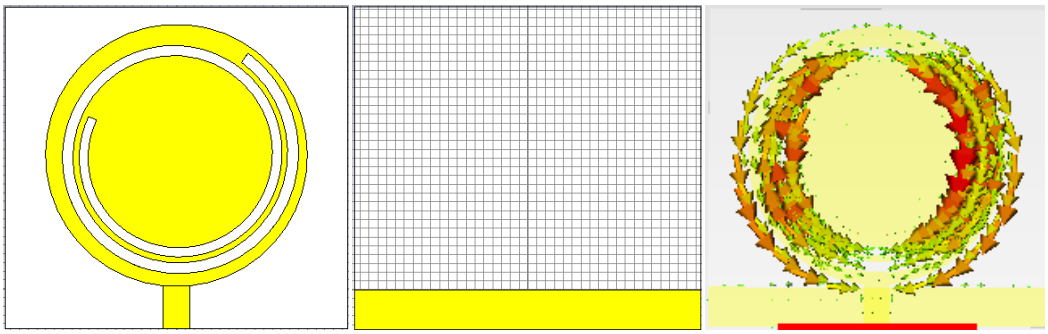


Figure 2.30: Planar Monopole Antenna with Archimedean Spiral Slots (t = 1~1.3mm), Front View, Back View, and its Corresponding Surface Current Distribution

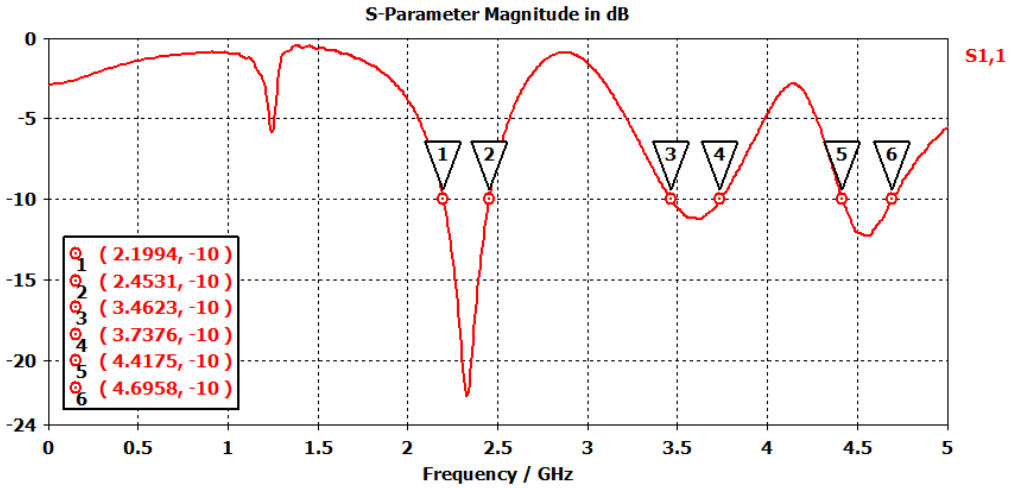


Figure 2.31: Simulated Reflection Coefficient of the Planar Monopole Antenna with Archimedean Spiral Slots (t = 1~1.3mm)

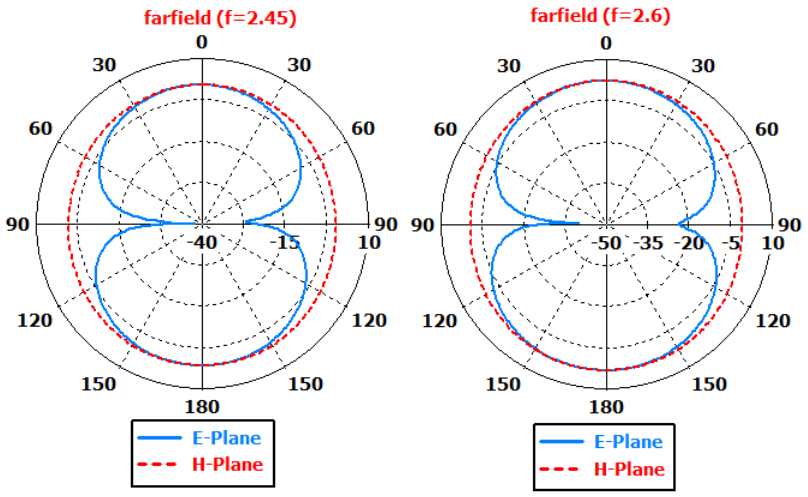


Figure 2.32: Simulated Radiation Pattern of the Planar Monopole Antenna with Archimedean Spiral Slots (t = 1~1.3mm), at 2.45GHz and 2.6GHz, in E-Plane and H-Plane

Table 2.1 compares the simulated radiation efficiency, total efficiency and gain corresponding to the value of parameter t, which determines the dimensions and positions of the Archimedean spiral slots.

Table 2.1: Simulated Efficiency and Gain

	2.45GHz			2.6GHz		
	Rad. Effic	**Tot. Effic**	**Gain**	**Rad. Effic**	**Tot. Effic**	**Gain**
T=0~0.5	89%	73%	2.55dB	90%	81%	2.63dB
T=0~1	91%	87%	2.77dB	92%	91%	2.93dB
T=0~1.3	84%	72%	2.58dB	83%	78%	2.97dB
T=0.5~1	81%	74%	2.47dB	80%	71%	2.53dB
T=1~1.3	88%	79%	2.38dB	83%	49%	2.68dB

From Table 2.1, it is clear that when the range of t is from 0 to 1mm, the antenna geometry demonstrates the best radiation performance. Combining the results from Figure 2.18 to Figure 2.32, t=0~1mm is leading a best Archimedean spiral slot on the circular monopole patch. This antenna configuration has been fabricated (as shown in Figure 2.33) and subsequently characterised with an HP8753C vector network analyser (VNA). The dimension of the realised implementation is 35mm × 35mm.

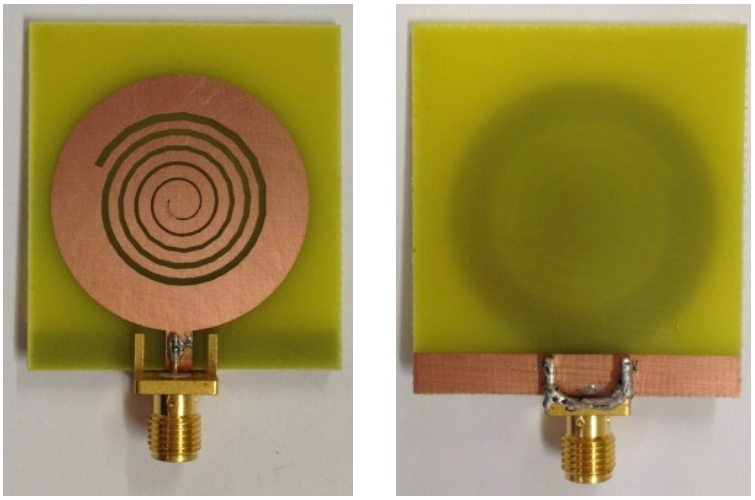


Figure 2.33: Photo of the Fabricated Antenna Designs, Front View and Back View

Figure 2.34: HP8753C Vector Network Analyser

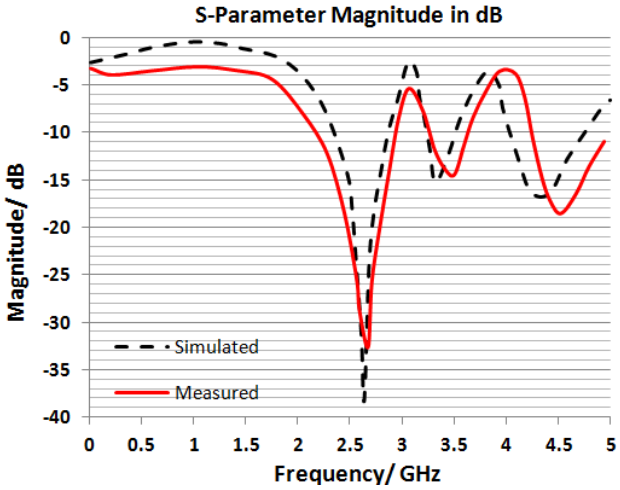


Figure 2.35: Simulated and Measured Reflection Coefficient of the Proposed Antenna

A schematic of the radiation pattern measurement setup is presented in Figure 2.36, which demonstrates the source Yagi antenna and the integrated smart antenna array are connected to Port 1 and Port 2 of the network analyser, respectively. A computer controlled positioner has been used to generate the azimuth and elevation for the antenna measurement. DC power supplies are utilised to provide suitable control voltage to the analogue phase shifters (later for the array measurements). Data acquisition interface sends the control signal to the position controller to rotate by specific step angle after programmed time interval and acquires the data from the network analyser for each step. The measurements were carried out in an anechoic chamber having walls that are covered with RF absorbers, as shown in Figure 2.37. Figure 2.38 illustrates the photo of the real measurement setup.

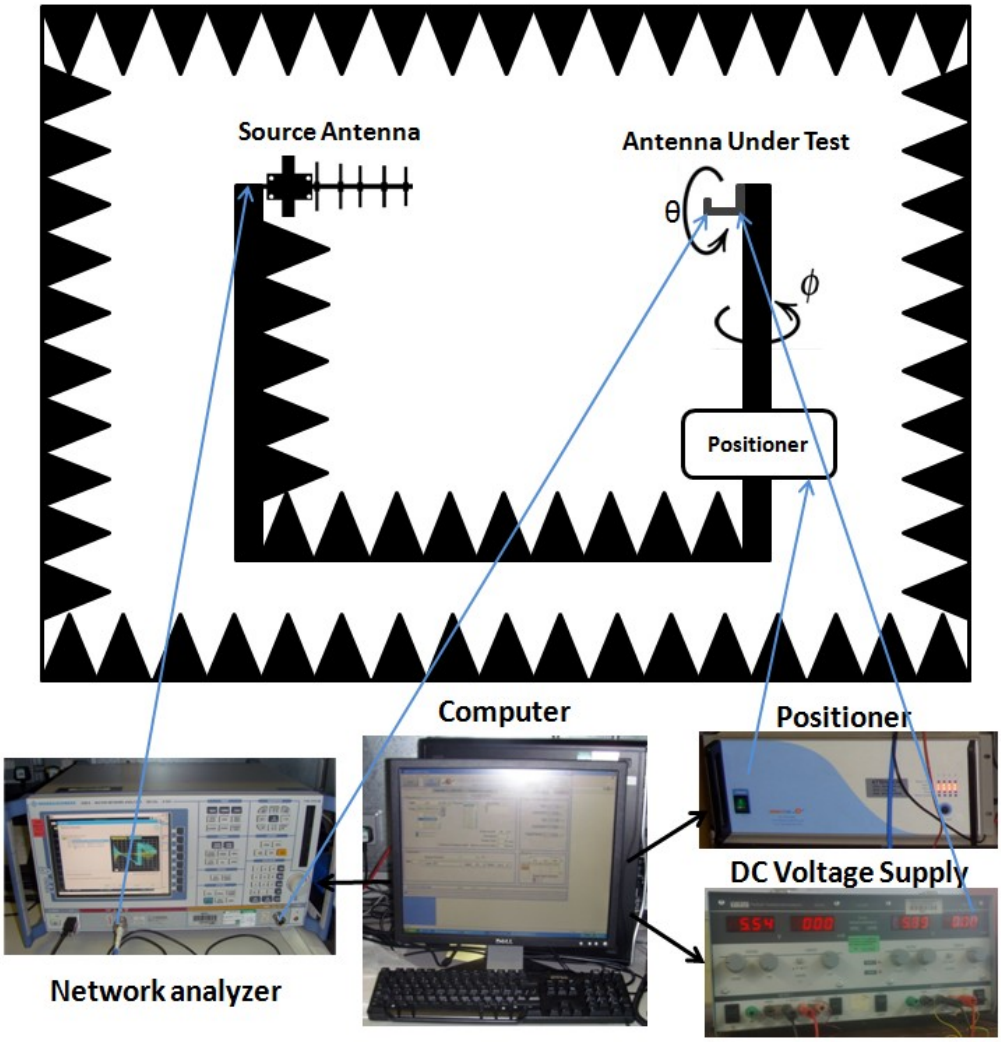
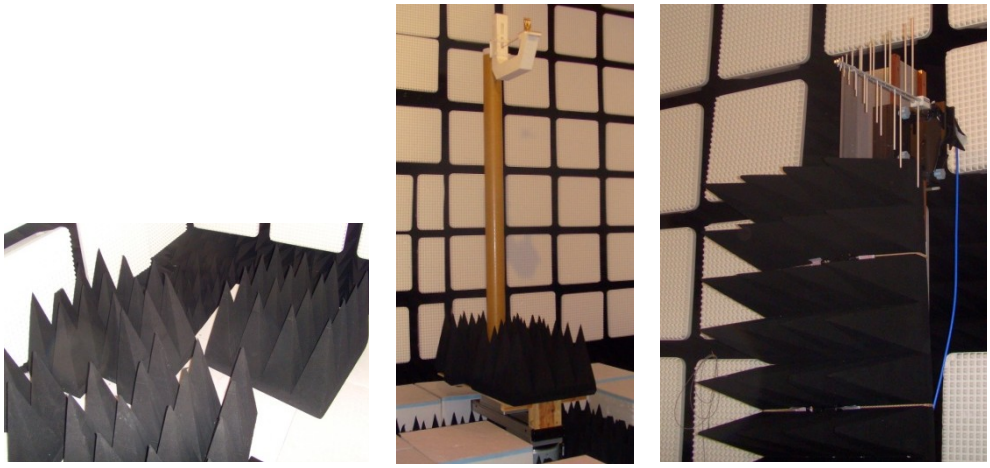


Figure 2.36: Radiation Pattern Measurement Setup



(a) **(b)** **(c)**

Figure 2.37: (a) RF Absorbers (b) Antenna under Test (c) Source Yagi Antenna

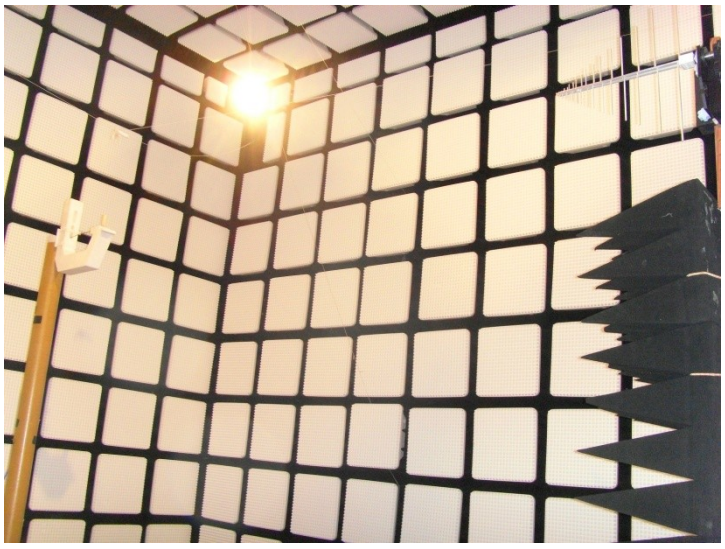


Figure 2.38: Photo of the Radiation Pattern Measurement Setup

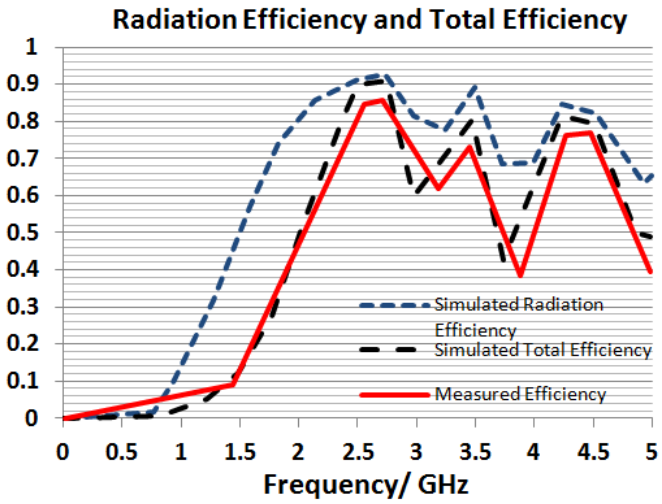


Figure 2.39: Simulated Radiation Efficiency, Simulated Total Efficiency and Measured Efficiency of the Proposed Antenna Structure

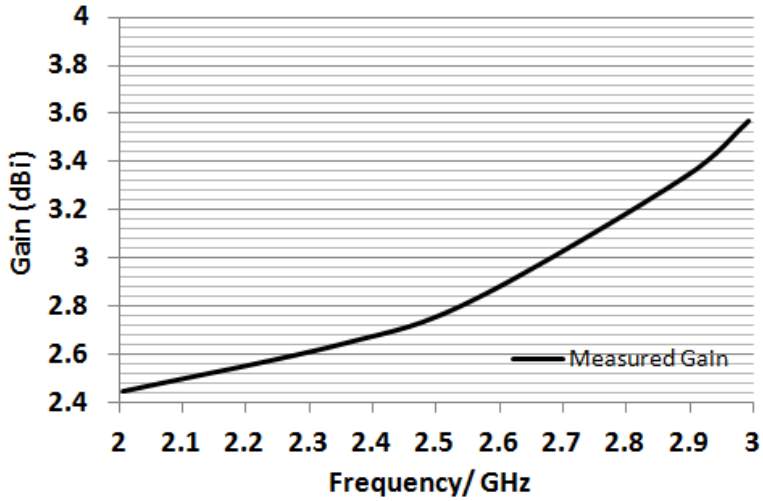


Figure 2.40: Measured Gain of the Proposed Antenna Structure

Figure 2.35, Figure 2.39 and Figure 2.40 demonstrate the simulated and measured reflection coefficient, radiation efficiency, total efficiency and gain, respectively. It is clear that a good consistency between the simulated and measured results, which verifies the design procedure. The proposed planar monopole antenna with Archimedean spiral slots configuration covers from 2.18GHz to 2.92GHz frequency band, which covers the WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) standards. Figure 2.39 depicts the measured efficiency are 79% and 87% for 2.45GHz and 2.6GHz, respectively. Figure 2.40 illustrates the measured gains are 2.72dBi at 2.45GHz and 2.88dBi for 2.6GHz.

2.4 Antenna Array Theory

2.4.1 Antenna Array Introduction

In the previous section, the characteristics of the single planar monopole antenna design with Archimedean spiral slots was discussed and analysed. Usually the radiation pattern of a single antenna element is relatively wide, and each element only provides low values of directivity and gain. In many commercial applications, it is required to design antennas with very directive characteristics and high gains (10dB), in order to meet the demands of long distance communication. This can only be achieved by increasing the electrical dimensions of the antenna. Enlarging the size of single antenna elements often demonstrates more directive characteristics. Another method to enlarge the electrical dimensions of the antenna, without necessarily increasing the size of the individual element, is to form an assembly of radiating elements in a geometrical and electrical configuration. This new antenna structure, formed by multi-elements, is referred to as an array [22]. In most cases, the array elements are identical. It is not necessary, but it is simpler, convenient, and more practical.

The individual elements in an antenna array could be of any forms (wires, microstrip, apertures, etc.). The vector addition of the fields radiated by the individual elements determines the total field of the antenna array, assuming that the current in each antenna is the same as that of the isolated antenna, neglecting coupling. This is in the ideal case and the performance depends on the separation between the elements. In order to obtain directive radiation patterns, the fields from the elements in the array should interfere constructively in the desired directions, and interfere destructively in the remaining space. There are five aspects controlling the shape and overall radiation pattern of the antenna array.

1. Geometrical construction of the antenna array (linear, rectangular, circular, rectangular, spherical)

2. Relative displacement between the antenna elements

3. Amplitude excitation of the individual antenna

4. Phase excitation of the individual antenna

5. Radiation pattern of the individual antenna

2.4.2 Antenna Array Fundamental Parameters

2.4.2.1 Array Factor

An array of identical antenna elements, with same magnitude and various progressive phases is referred to as a uniform antenna array. Its characteristic could be mathematically described by its array factor (AF). If the actual antennas are not isotropic sources, the total radiation field could be formed by multiplying the field of a single element by the array factor of the isotropic. This method applies for arrays of identical elements.

The array factor is given by Equation (2.31) [39].

$$AF = \sum_{n=1}^{N} w_n e^{j\psi_n} \tag{2.31}$$

Where, N is the number of elements, ψ_n stands for the difference in phase excitation between the elements and w_n demonstrates the complex weight of the n^{th} element.

By applying a phase shift δ_n to ψ_n, the main beam of the antenna array is steered to (θ_s, ϕ_s), as shown in Equation 2.32.

$$AF = \sum_{n=1}^{N} w_n e^{j(\psi_n + \delta_n)} \tag{2.32}$$

An antenna array distributed in 3D space is demonstrated in Figure 2.41 and its array factor could be described in Equation 2.33 to 2.35.

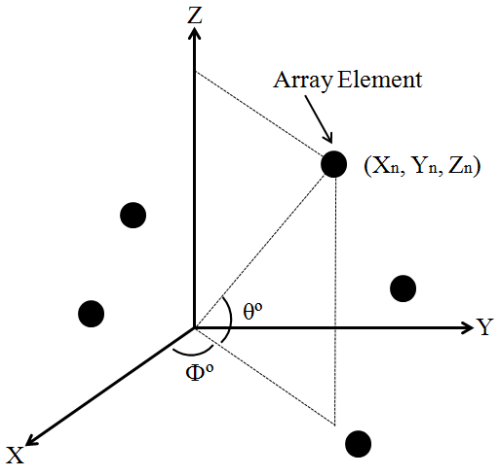


Figure 2.41: Arbitrary Antenna Array Geometry

$$AF = \sum_{n=1}^{N} w_n e^{jk[x_n(u-u_s)+y_n(v-v_s)+z_n cos\theta]} \tag{2.33}$$

$$u = sin\theta cos\phi,\ u_s = sin\,\theta_s cos\phi_s \tag{2.34}$$

$$v = sin\theta sin\phi,\ v_s = sin\theta_s sin\phi_s \tag{2.35}$$

Where, N shows the number of elements in the array, (x_n, y_n, z_n) represents the position of the n^{th} element, w_n stands for the array weight and (θ_s, ϕ_s) is the steering angle for elevation and azimuth, respectively, as depicted in Figure 2.41.

2.4.2.2 Radiation Pattern

The far-field radiation pattern of an antenna array is the total product of a single element radiation pattern, as described in Equation (2.36) [39].

$$AP(\theta,\emptyset) = \sum_{n=1}^{N} EP_n(\theta,\emptyset) w_n e^{jk[x_n(u-u_s)+y_n(v-v_s)+z_n cos\theta]} \quad (2.36)$$

Where $EP_n(\theta,\phi)$ is the radiation pattern of a single element, N shows the number of elements in the array, (x_n, y_n, z_n) represents the position of the n^{th} element, w_n stands for the array weight and (θ_s, ϕ_s) is the steering angle for elevation and azimuth, respectively.

2.4.2.3 Directivity

The directivity of an antenna array is determined by Equation (2.37) [46].

$$D = \frac{4\pi|EP(\theta,\emptyset)AF(\theta,\emptyset)|^2}{\int_0^{2\pi}\int_0^{\pi}|EP(\theta,\emptyset)AF(\theta,\emptyset)|^2 sin\theta\delta\theta\delta\emptyset} \quad (2.37)$$

Where, $EP(\theta,\phi)$ is the radiation pattern of a single element and $AF(\theta,\phi)$ is the array factor.

2.5 Array Geometry for Smart Antenna System

2.5.1 Antenna Array Structure

Radiation pattern of an antenna array depends on the antenna arrangements, spacing between the elements, excitation phase of individual antenna and characterisations of the single element. Utilising the analysis obtained from the individual antenna design, a four-element linear planar antenna array with uniform spacing is conceived (as illustrated in Figure 2.42).

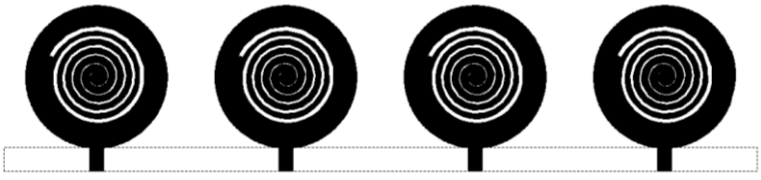


Figure 2.42: Four-Element Linear Planar Antenna Array

The separation between the adjacent planar monopole antennas relates to the inter-element (centre to centre) spacing. The wide inter-element spacing will limit the maximum scanning

range of the antenna array, because of the emergence of grating lobe. The separation also affects the reflection coefficient of the whole antenna array. The linear antenna array is designed to have 10dB gain and angular width less than 40° so that the beam steering characteristics could be demonstrated with reasonable phase shift. The inter-element spacing is defined using the following equation [22].

$$\theta_m = 2\left[\frac{\pi}{2} - \cos^{-1}\left(\frac{\lambda}{Nd}\right)\right] \tag{2.38}$$

Where, θ_m represents the first null beamwidth, λ stands for the free space wavelength and d is the separation between array elements. The array factor of an N-element array is simplified as:

$$AF_N = 20\log\left[{\sin N\psi/2}/{N\psi/2}\right] \tag{2.39}$$

Where $\psi=kd\cos\theta+\beta$, θ decides the maximum radiation direction of the antenna array. Phase difference ($\Delta\Phi=\beta d\sin\varphi_0$) applied to the consecutive antenna array elements depends on the beam scan angle (φ_0). Radiation pattern of the antenna array is obtained by multiplying the radiation pattern characteristics of the antenna with the array factor.

2.5.2 Antenna Array Simulation and Experimental Results

From calculation, the inter-element spacing should be around 35mm. In order to further optimise the reflection coefficient, radiation efficiency and gain, five inter-element spacing values: 32mm, 36mm, 40mm, 45mm and 50mm, have been simulated and compared, as shown from Figure 2.43 to Figure 2.47.

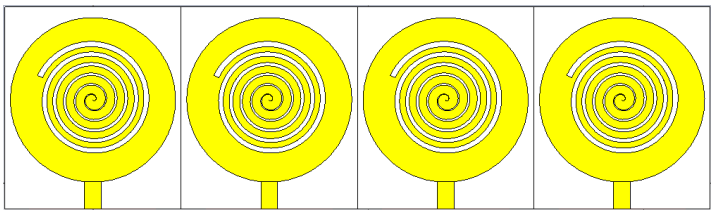


Figure 2.43: Antenna Array with Inter-Element Spacing S=32mm

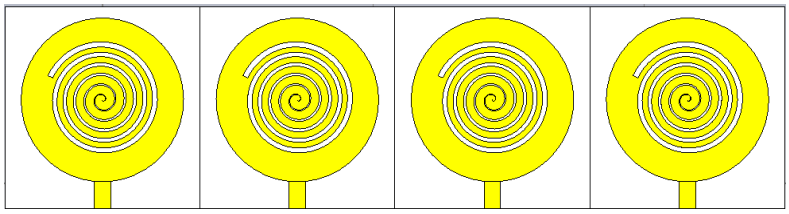


Figure 2.44: Antenna Array with Inter-Element Spacing S=36mm

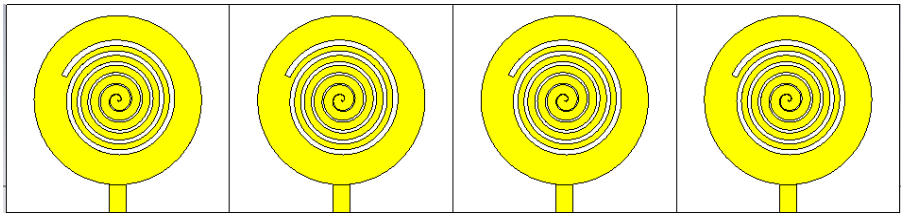


Figure 2.45: Antenna Array with Inter-Element Spacing S=40mm

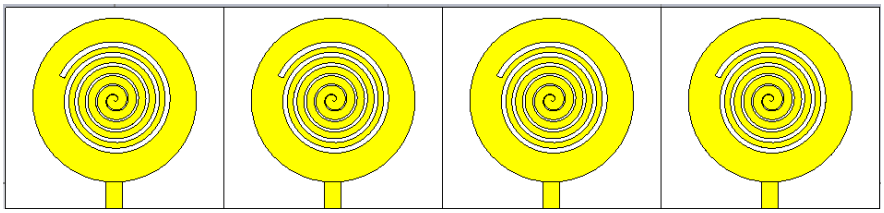


Figure 2.46: Antenna Array with Inter-Element Spacing S=45mm

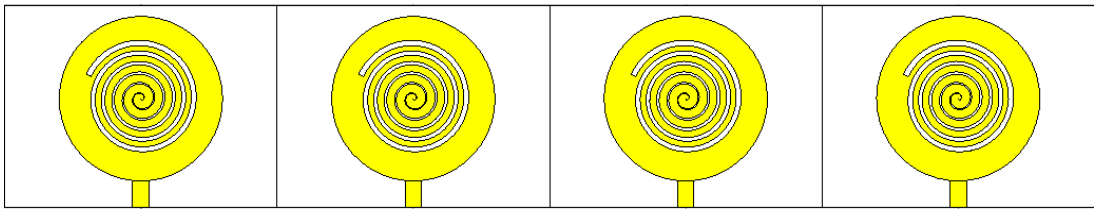


Figure 2.47: Antenna Array with Inter-Element Spacing S=50mm

Figure 2.48 illustrates the simulated reflection coefficients corresponding to the inter-element spacing (S). Table 2.2 summarises the simulated radiation efficiency, total efficiency and gain for the five antenna arrays.

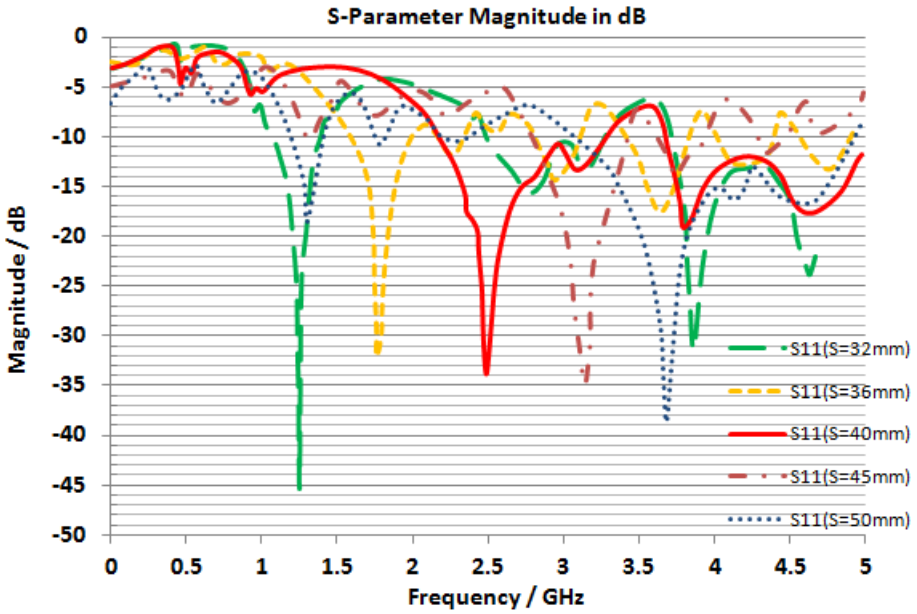


Figure 2.48: Simulated Reflection Coefficient (S_{11}) Corresponds to Inter-Element Spacing (S)

Table 2.2: Simulated Efficiency and Gain

	2.45GHz			2.6GHz		
	Rad. Effic.	**Tot. Effic.**	**Gain**	**Rad. Effic.**	**Tot. Effic.**	**Gain**
S=32mm	86%	67%	8.7dB	87%	78%	8.9dB
S=36mm	88%	73%	9.1dB	89%	80%	9.3dB
S=40mm	90%	75%	9.9dB	91%	84%	10.3dB
S=45mm	89%	74%	9.8dB	90%	83%	10.2dB
S=50mm	90%	74%	9.9dB	91%	82%	10.3dB

From Figure 2.48 and Table 2.2, it is significant to note that when the inter-element spacing is 40mm, the planar monopole antenna array achieves best reflection coefficient, highest efficiency and suitable radiation performance. The mutual coupling of the proposed antenna array is demonstrated in Figure 2.49.

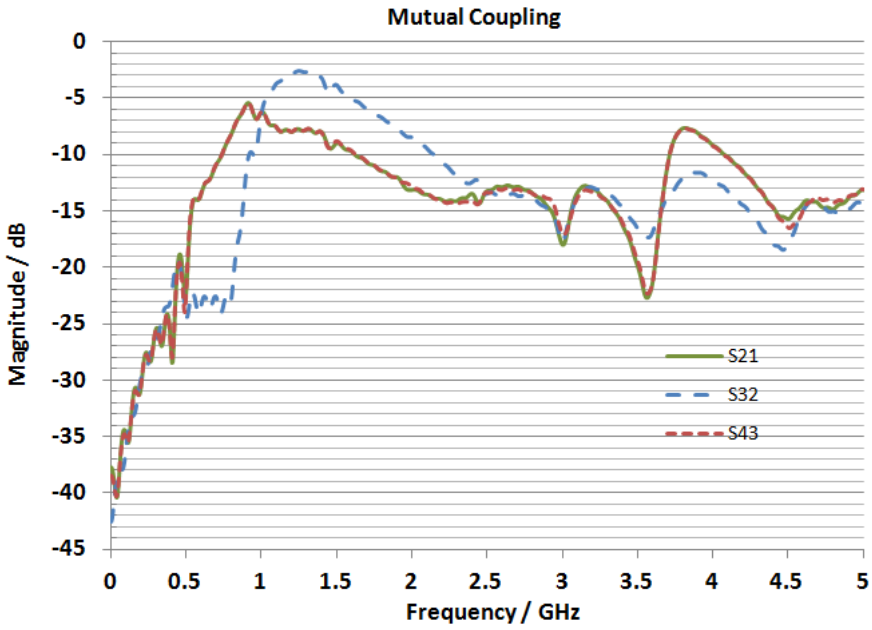


Figure 2.49: Simulated Mutual Coupling of the Proposed Antenna Array

Figure 2.50 presents the simulated radiation pattern of the four-element linear planar monopole antenna array with inter-element spacing s=40mm, in H-Plane and E-Plane, at 2.45GHz and 2.6GHz, respectively.

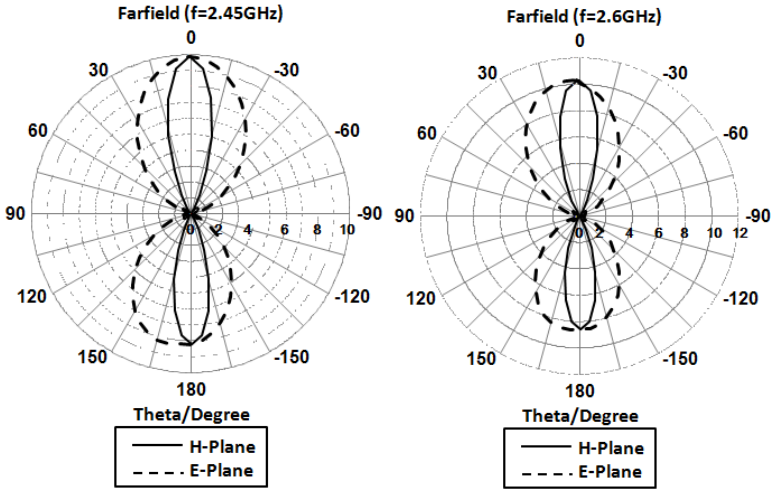


Figure 2.50: Simulated Radiation Pattern of the Proposed Four-Element Linear Planar Antenna Array at 2.45GHz and 2.6GHz in H-Plane and E-Plane

In both planes, the side lobe levels are down by at least 10dB from the main lobe magnitude. The angular widths (3dB) in the E-plane are approximately 81º and 80º at 2.45GHz and 2.6GHz, respectively. In the H-plane, the 3dB beamwidths are 31º and 30º at 2.45GHz and 2.6GHz, respectively.

This four-element linear antenna array configuration has been fabricated (as presented in Figure 2.51) and subsequently characterised with an HP8753C vector network analyser (VNA). Since the antenna array is a four ports circuit and the VNA is a two port system, while in the measurement, the empty two ports of the antenna array were terminated with 50 ohm terminators. The final inter-element spacing is 40mm, and the dimension of the realised implementation is 36mm × 155mm.

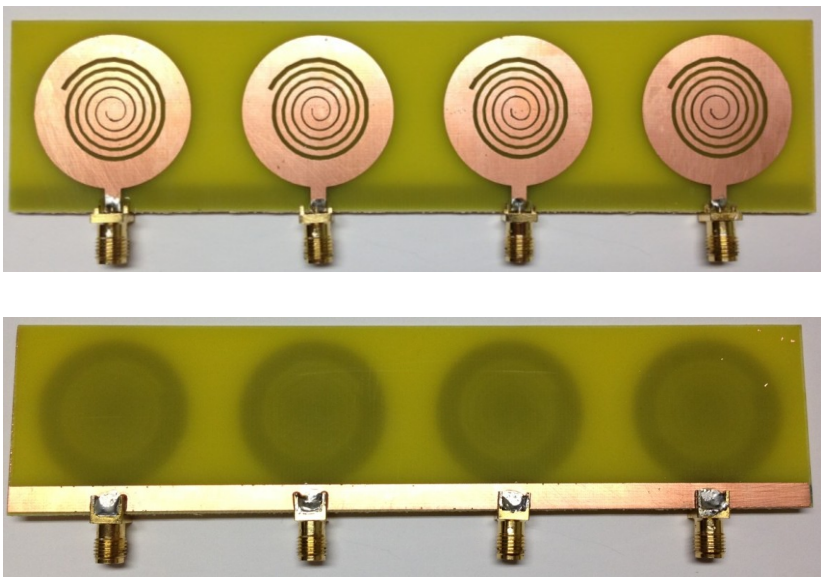


Figure 2.51: Photo of the Fabricated Antenna Array, Front View and Back View

Figure 2.52 and Figure 2.53 depict the measured reflection coefficient and mutual coupling of the proposed four-element linear antenna array.

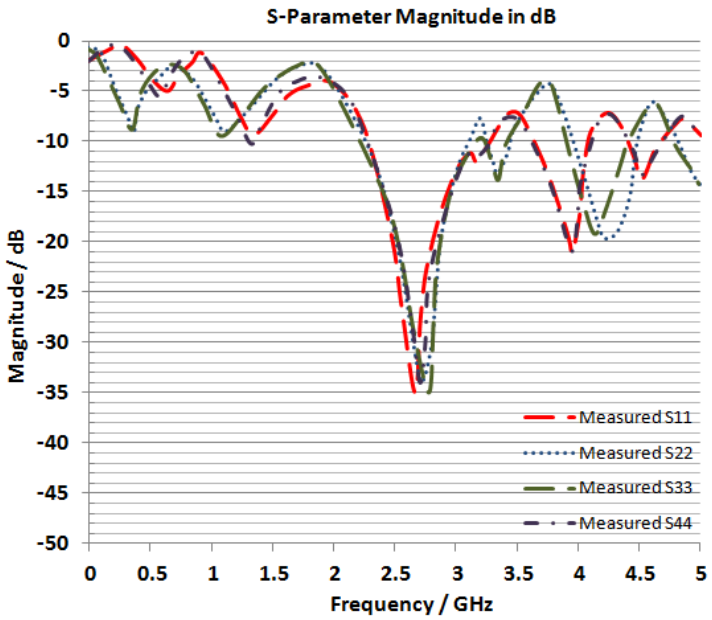


Figure 2.52: Measured Reflection Coefficient of the Proposed Antenna Array

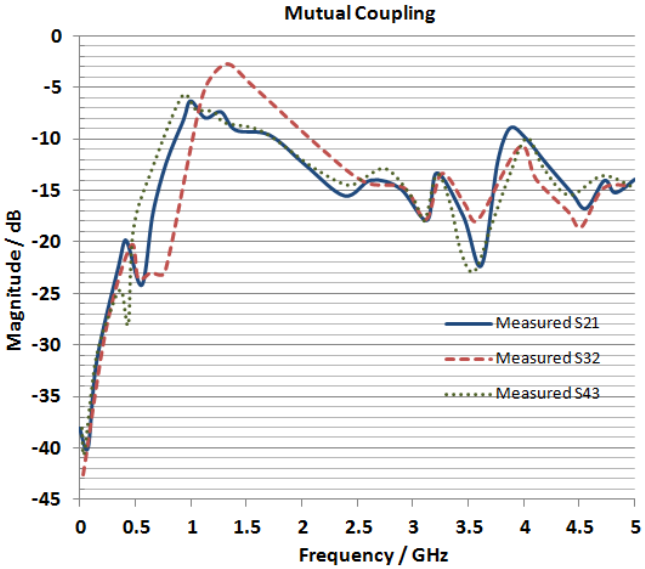


Figure 2.53: Measured Mutual Coupling of the Proposed Antenna Array

Figure 2.52 and Figure 2.53 reveal a good consistency between the simulated and measured reflection coefficients, which validates the antenna array configuration. The proposed antenna array achieves a 10 dB reflection coefficient from 2.2GHz to 2.9GHz with low mutual coupling (-10dB), which could cover WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) mobile applications. Gain, efficiency and radiation pattern measurements of the whole smart antenna array will be summarised in Chapter 4.

2.5.3 Antenna Array with Simulated Phase Excitation

The four-element linear antenna array has been excited by different phase degrees using CST Microwave Studio, in order to clarify the main beam scanning angles. The phase excitation of each antenna corresponding to the steering angle is tabulated in Table 2.3.

Table 2.3: Phase Excitation of the Antenna

Phase Excitation (Degree)				Main Beam Direction (θ°)
Antenna_1	Antenna_2	Antenna_3	Antenna_4	
0	0	0	0	0
0	30	60	90	10
0	55	110	165	20
0	85	170	255	30
0	105	210	315	40
0	130	260	30	50
0	145	290	75	60
0	155	310	105	70
0	165	330	135	80
0	175	350	165	85

The main beam scanning ranges are ±86° and ±88° for 2.45GHz and 2.6GHz, respectively. However, as the scanning reaches ±55° and ±57°, grating lobes start to appear in the linear antenna array. Grating lobes are not desired in adaptive antennas as they expose the system to noise and interference signals coming far from the direction of the required signal. Furthermore, the grating lobes also cause the array to radiate in undesired directions. Figure 2.54 and Figure 2.55 demonstrate the simulated gain vs. theta in the H-Plane, for scanning angles of -50°, -40°, -30°, -20°, -10°, 0°, +10°, +20°, +30°, +40° and +50°, at 2.45GHz and 2.6GHz, respectively. At 0°, the gains are 9.9dB and 10.3dB for 2.45GHz and 2.6GHz. The main beam could rotate ±50° without emergence of grating lobes. Scanning angles corresponding to the angular width and side lobe levels (SLL) are presented in Figure 2.56 and Figure 2.57.

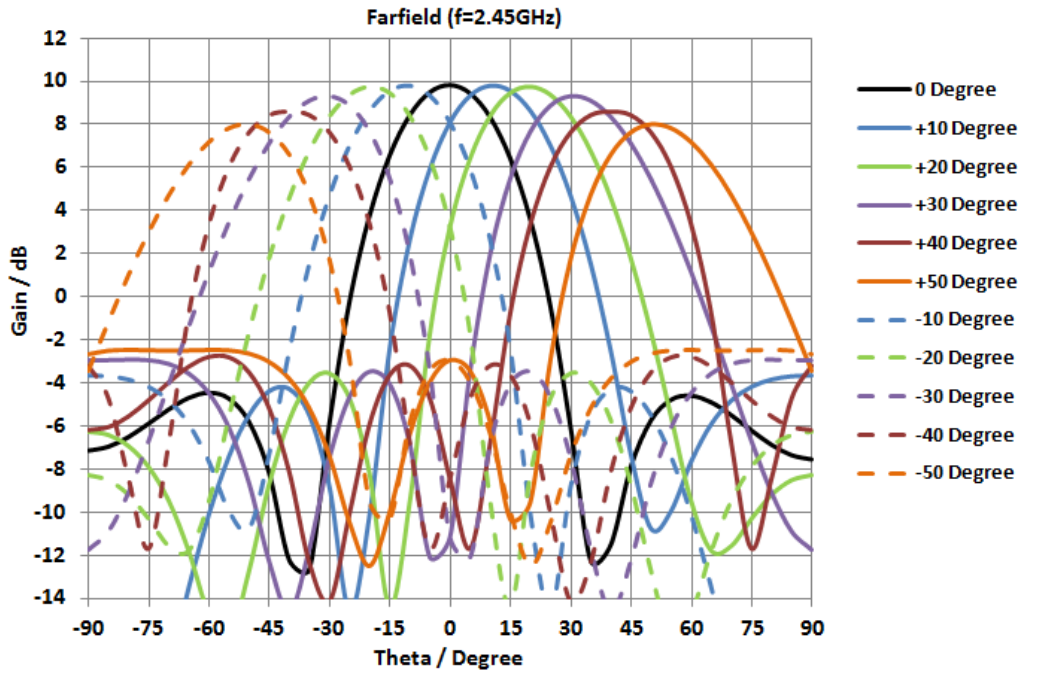


Figure 2.54: Simulated Gain vs. Theta in the H-Plane for Different Scanning Angles, at 2.45GHz

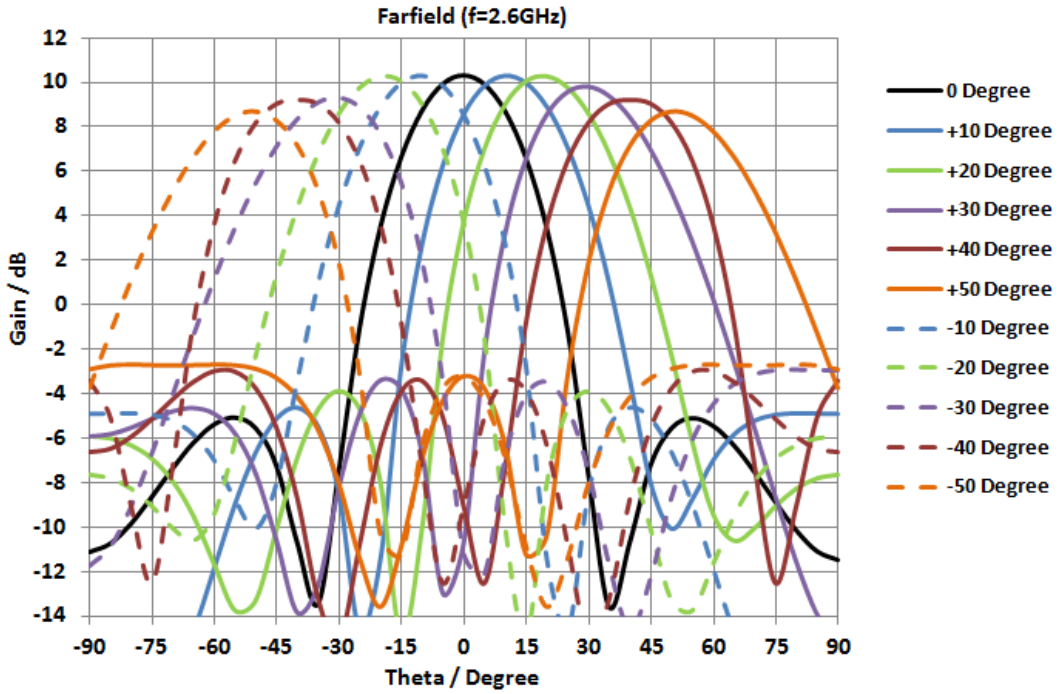


Figure 2.55: Simulated Gain vs. Theta in the H-Plane for Different Scanning Angles, at 2.6GHz

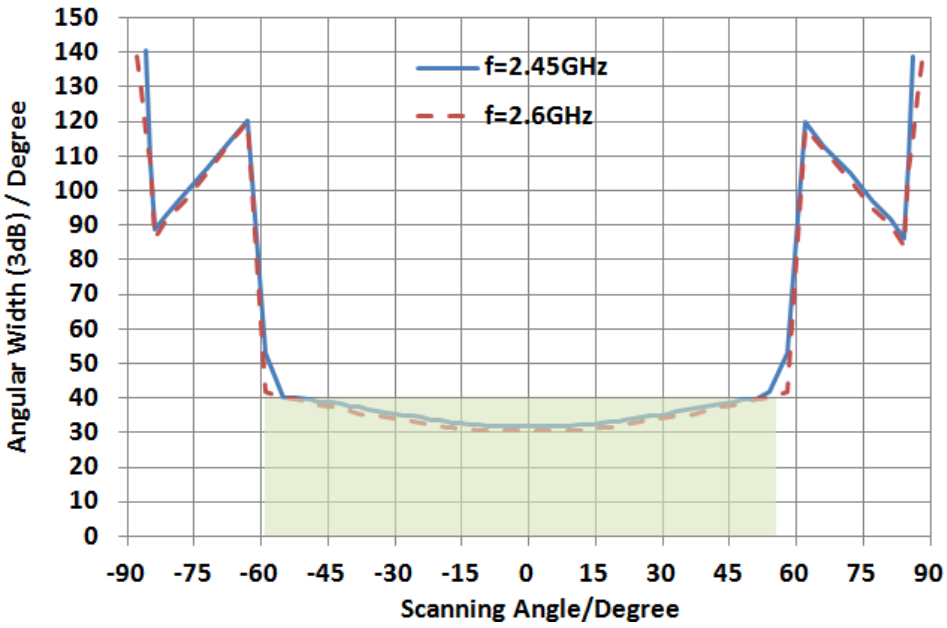


Figure 2.56: Full Wave Simulation Results of Angular Width (3dB)

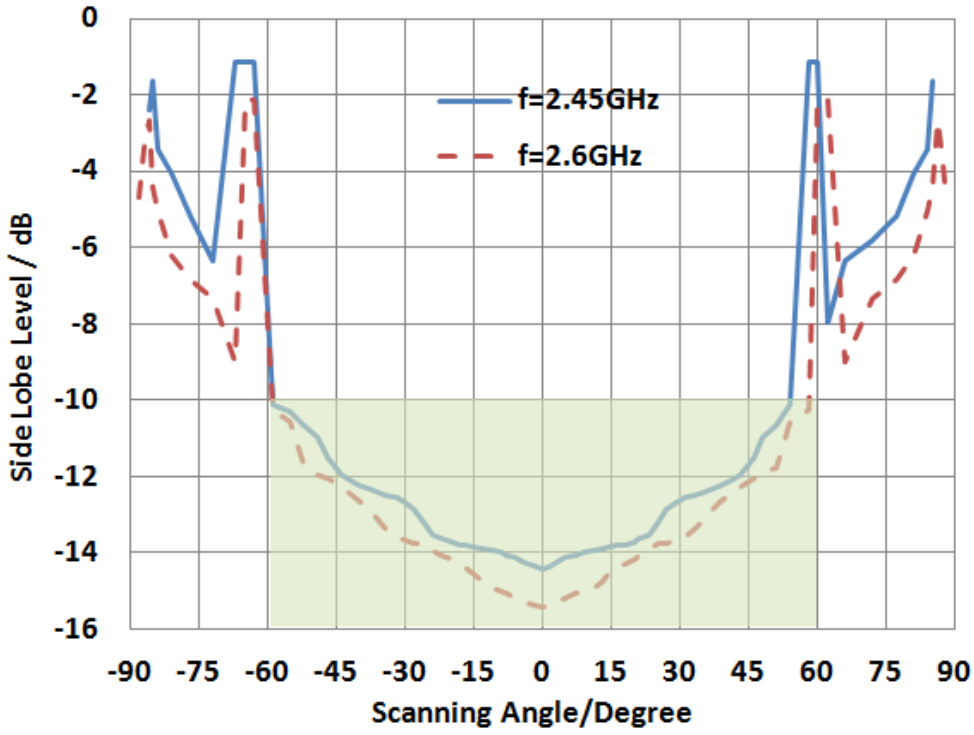


Figure 2.57: Full Wave Simulation Results of Side Lobe Level

The four-element linear antenna array was designed to achieve 10dB gain and angular width less than 40°. The 3dB bandwidth reaches -57° to +55° for 2.45GHz, and -59° to +57° at 2.6GHz. The SLL increases with the scanning range, which covers -59° to +54° and -59° to +58°, for 2.45GHz and 2.6GHz, respectively. Combing all of the simulation results from

Table 2.3, Figure 2.54 to Figure 2.56, the main beam of the four-element linear antenna array is able to steer from -57° to +54° for 2.45GHz, and -59° to +57° at 2.6GHz.

2.6 Summary

In this chapter, firstly, a novel compact planar monopole antenna configuration with Archimedean spiral slots for WiFi/Bluetooth and LTE frequency bands has been presented. The effects of varying slots dimensions and positions on the monopole antenna performance have also been studied. It is illustrated when the value of Archimedean spiral slot key parameter t is from 0 to 1mm, the presented structure obtains low reflection coefficient (-19dB, -30dB), high efficiency (79%, 87%), large gain (2.72dBi, 2.88dBi) and omni-directional radiation patterns for 2.45GHz and 2.6GHz, respectively. This antenna structure has application to multi-functional wireless communication systems.

Secondly, a four-element linear planar monopole antenna array utilising the unit antenna has been designed, simulated, optimised and characterised. Different inter-element spacing values are investigated and compared. When the spacing is 40mm, the array geometry archive low reflection coefficient (-17dB, -29dB), suitable mutual coupling (-15dB, -14dB), large efficiency (75%, 84%), high gain (9.9dB, 10.3dB) and directional radiation patterns for 2.45GHz and 2.6GHz, respectively. The antenna array is implemented and fabricated on an FR4 substrate. Reflection coefficient and mutual coupling measurement results closely correlate with those obtained during design simulations. The array will be integrated into a smart antenna system, and the radiation properties will be measured together with the feeding network and phase shifters.

Lastly, the four-element linear antenna array has been excited by progressive phase shifts using CST Microwave Studio, in order to demonstrate the main beam scanning angles. By analysing the radiation gain, angular width (3dB) and side lobe level, beam steering from 57° to +54° for 2.45GHz, and -59° to +57° at 2.6GHz in H-plane with the gain fluctuation less than 3dB, narrow half power beamwidth (40°) and low side lobe level (-10dB) have been achieved.

In summary, the investigations of single antenna design and array geometry are shown in Figure 2.58 and Figure 2.59.

In the next chapter, UWB feeding network for the linear antenna array will be discussed. Chapter 4 will focus on using high accurate analogue shifters to achieve real phase excitations. Moreover, full system fabrication and characterisation will also be presented in Chapter 4.

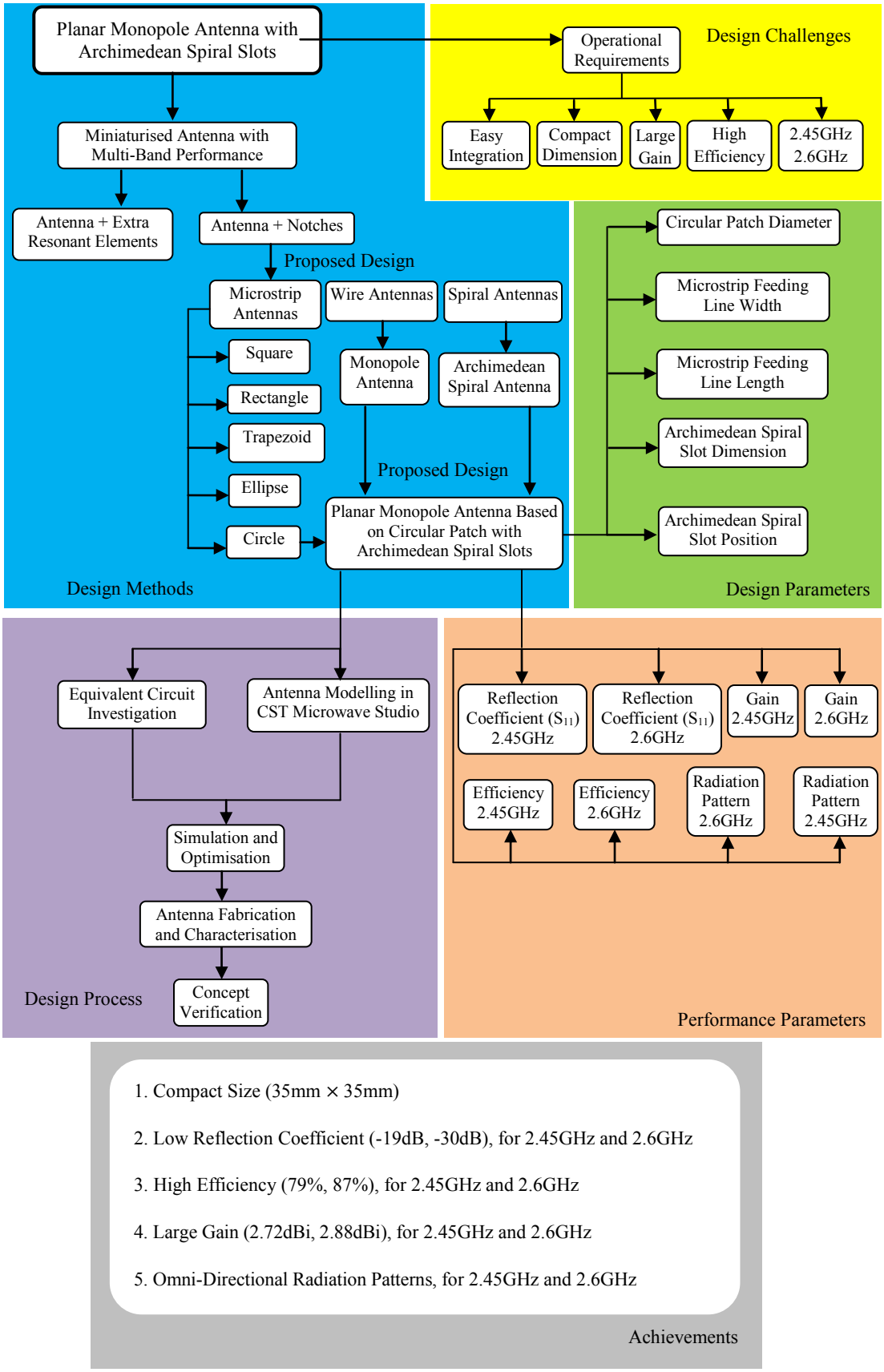


Figure 2.58: Investigation of Planar Monopole Antenna with Archimedean Spiral Slots

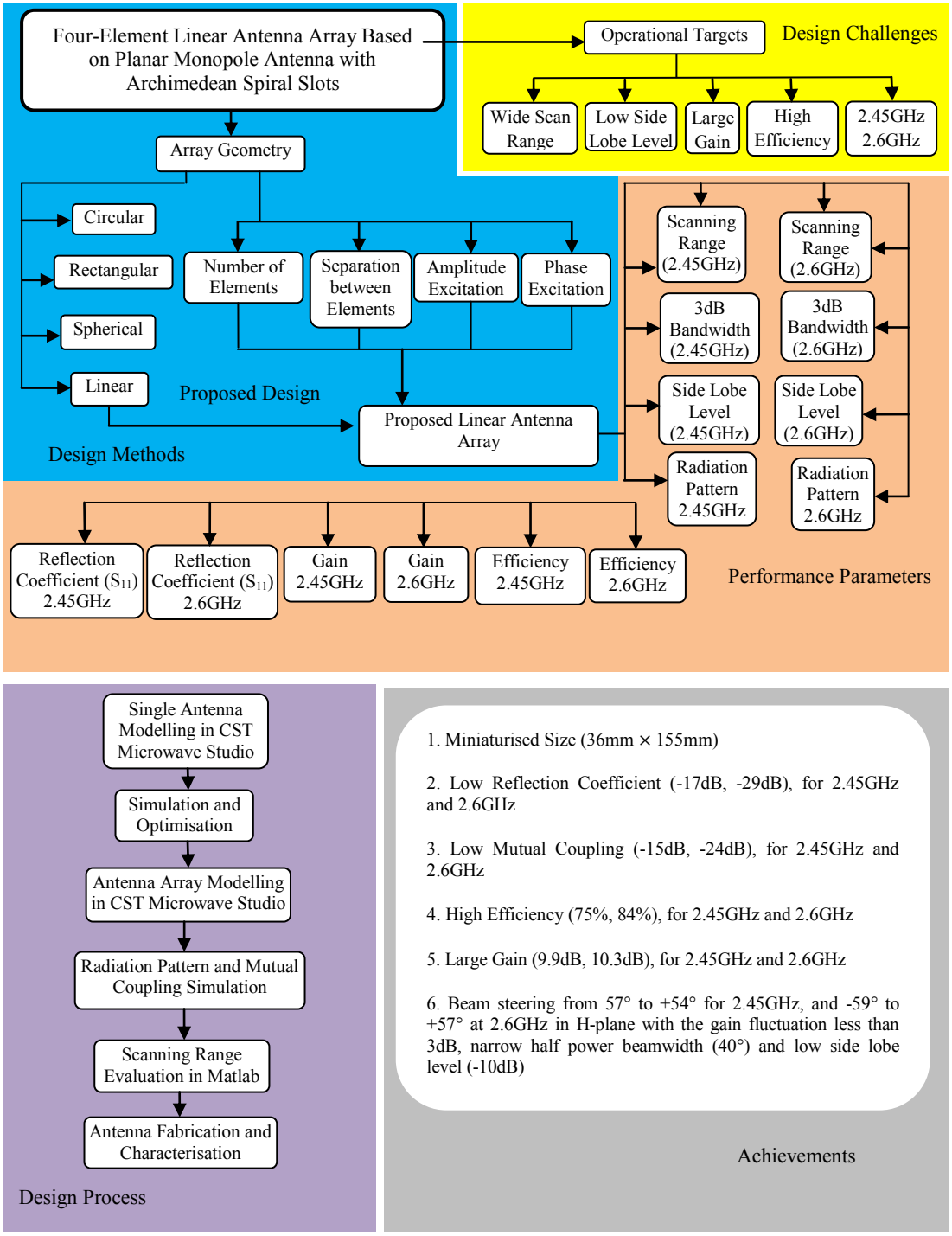


Figure 2.59: Investigation of Four-Element Linear Antenna Array

Chapter 3: Reconfigurable and Ultra-Wideband Feeding Network for Smart Antenna Array

3.1 Introduction

Another important element in a smart antenna array is the feeding network, which controls the amplitude and phase excitations of the antennas. This chapter concentrates on the design, simulation, optimisation and characterisation of various feeding network geometries.

The conventional T-junction power divider is lossless, but suffers from the issue of not being matched at all ports. Moreover, there is no isolation between the output ports. The resistance divider is able to match all the ports, however, the power loss is relative high and still no isolation is achieved. The Wilkinson power divider has been widely used in microwave communication systems, because it shows useful property of being lossless when the output ports are matched, and only the reflected power is dissipated.

The fundamental Wilkinson power divider and its equivalent circuit has been analysed, designed and simulated, targeting at 2.45GHz. Modifications and improvements have been made to the basic structure, in order to obtain multiband and reconfiguration performance. The divide circuit is designed in Agilent Advanced Design System, and later imported to CST Microwave Studio for full wave simulations.

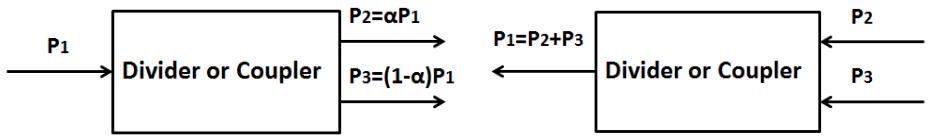
This chapter is divided into seven sections. Section 3.2 describes the introduction, theory and analysis of the fundamental Wilkinson power divider. Based on the standard structure, Section 3.3 investigates implementing the feeding network on high resistivity silicon (HRS) and Aluminium wafers. Section 3.4 presents a compact feeding network for circular antenna array. Reconfigurable feeding network for dual circular polarised antenna array is discussed

in Section 3.5, and reconfigurable feeding network for tuning the operating frequency is shown in Section 3.6. Section 3.7 presents an ultra-wideband (UWB) feeding network for smart antenna array. Finally, Section 3.8 summaries the chapter.

3.2 Fundamental Wilkinson Power Divider Design

3.2.1 Introduction

Power dividers are passive components in microwave communication systems, using for power division or power combination, as depicted in Figure 3.1 [37].



(a) **(b)**

Figure 3.1: (a) Power Division (b) Power Combination [37]

In power division, an input RF signal is distributed into two (or more) individual signals with less power. The divider could be a three-port circuit (as shown in Figure 3.1), with or without loss, and also would be a four-port geometry. Three-port structure may take the form of T-junctions, while four-port networks take the form of directional couplers and hybrids [37]. Power dividers can achieve both of equal (3dB) and unequal power divisions, depending on the system requirements. Directional couplers are usually designed for arbitrary power distribution, and hybrid junctions have equal power splitting. Moreover, hybrid junctions demonstrate either a 180º (Magic-T) or a 90º (Quadrature) phase shift between the output ports.

A wide variety of power dividers and couplers have been investigated and characterised, which include E-Plane waveguide T-junction, H-Plane waveguide T- junction, multi-hole directional coupler, Magic-T coupler, the Bethe hole coupler and the Schwinger coupler. Furthermore, there are many other couplers and dividers utilising coaxial probe, stripline and microstrip technologies, such as branch line hybrid, coupled line coupler and Wilkinson power divider.

3.2.2 T-Junction Power Divider Structure

T-junction is the simplest configuration of power divider, which is a three-port network and can be used for power splitting and combining. The T-junction is able to be implemented

in any type of transmission lines. Figure 3.2 illustrates some T-junctions in waveguide and microstrip structures.

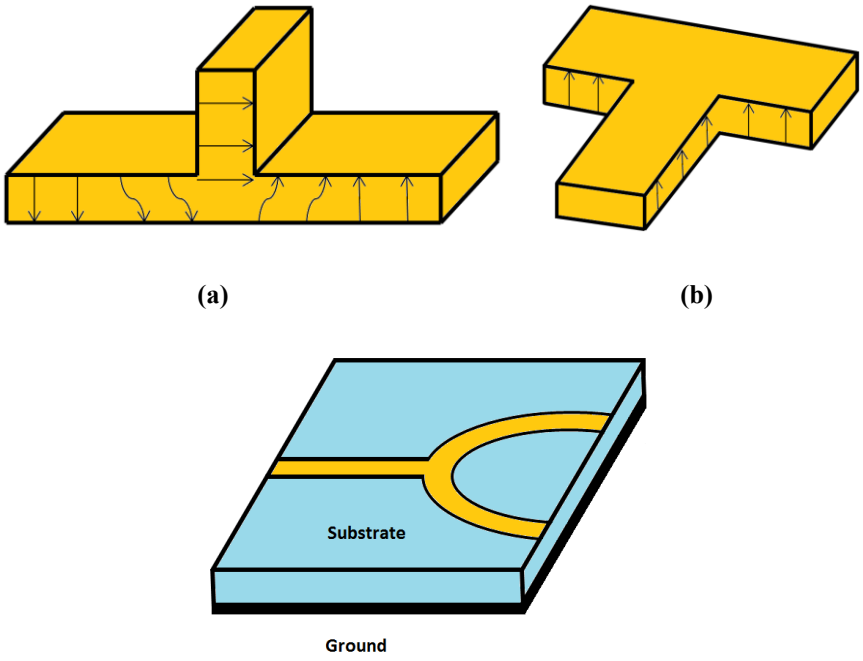


Figure 3.2: Various T-Junction Power Dividers: (a) E-Plane Waveguide (b) H-Plane Waveguide (c) Microstrip T-Junction

The scattering matrix of an arbitrary three-port network has nine elements:

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{3.1}$$

When the network is passive and contains no anisotropic materials, the power divider should be reciprocal and the [S] matrix must be symmetric ($S_{ij}=S_{ji}$). The ideal case is to construct a junction with lossless and matched at all ports. However, it is impossible to build such a three-port lossless reciprocal network with all ports matched.

If all ports are matched, then $S_{11}=S_{22}=S_{33}=0$, and if the network is reciprocal, the [S] matrix is simplified to

$$[S] = \begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{12} & 0 & S_{23} \\ S_{13} & S_{23} & 0 \end{bmatrix} \tag{3.2}$$

If the three-port network is also lossless, then the energy conservation requires the [S] matrix should be unitary, which generates the following conditions:

$$|S_{12}|^2 + |S_{13}|^2 = 1 \tag{3.3}$$

$$|S_{12}|^2 + |S_{23}|^2 = 1 \tag{3.4}$$

$$|S_{13}|^2 + |S_{23}|^2 = 1 \tag{3.5}$$

$$S_{13}^* S_{23} = 0 \tag{3.6}$$

$$S_{23}^* S_{12} = 0 \tag{3.7}$$

$$S_{12}^* S_{13} = 0 \tag{3.8}$$

Equations (3.6) to (3.8) demonstrate at least two of the three parameters (S_{12}, S_{13}, and S_{23}) should be zero. However, this condition will always be inconsistent with one of the Equations (3.3) to (3.5), which means a three-port network cannot be lossless, reciprocal and matched at all ports [37].

Lossless T-junction is able to be implemented, and the transmission line model is presented in Figure 3.3. As discussed before, such configuration cannot be matched simultaneously at all ports.

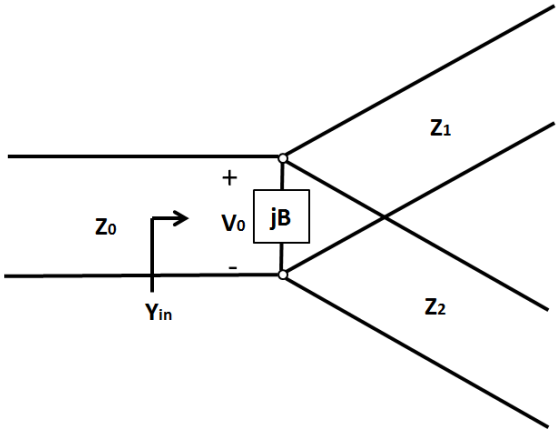


Figure 3.3: Transmission Line Model of a Lossless T-Junction [37]

There are fringing fields and higher order modes associated with the T-junction. The stored energy can be represented by a lumped susceptance, B. For the T-junction power divider, in order to match the input characteristic impedance Z_0, the following equation can be satisfied.

$$Y_{in} = jB + \frac{1}{Z_1} + \frac{1}{Z_2} = \frac{1}{Z_0} \tag{3.9}$$

If the transmission lines are lossless (or with low loss), then the characteristic impedances are real. In that condition, B=0, and Equation (3.9) is reduced to

$$\frac{1}{Z_1}+\frac{1}{Z_2}=\frac{1}{Z_0} \tag{3.10}$$

In reality, if B is not negligible, some reactive tuning elements will be utilised into the divider configuration, in order to cancel the susceptance, at least over a narrow frequency band.

The output line impedance Z_1 and Z_2 can be calculated to generate various power division ratios. For a 50Ω input transmission line, a 3dB (equal split) power divider can be designed by using two of 100Ω output lines. If necessary, λ/4 transformers could be used to bring the output line impedances back to the desired values. When the output lines are matched, then the input line will also be matched, however, there will be no isolation between the output ports.

Alternatively, a three-port network can be realised with lossless and reciprocal, if only two of its ports are matched. If Port 1 and Port 2 are matched, then the [S] matrix could be defined as

$$[\mathrm{S}]=\begin{bmatrix} 0 & S_{12} & S_{13} \\ S_{21} & 0 & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \tag{3.11}$$

In order to be lossless, the following unitarity conditions should be achieved:

$$|S_{12}|^2+|S_{13}|^2=1 \tag{3.12}$$

$$|S_{12}|^2+|S_{23}|^2=1 \tag{3.13}$$

$$|S_{13}|^2+|S_{23}|^2+|S_{33}|^2=1 \tag{3.14}$$

$$S_{13}^* S_{23}=0 \tag{3.15}$$

$$S_{12}^* S_{13}+S_{23}^* S_{33}=0 \tag{3.16}$$

$$S_{23}^* S_{12}+S_{33}^* S_{13}=0 \tag{3.17}$$

Equations (3.12) and (3.13) present that $|S_{13}|=|S_{23}|$, so Equation (3.15) generates that $S_{13}=S_{23}=0$. Then, $|S_{12}|=|S_{33}|=1$. The [S] matrix and signal flow diagram for this kind of three-port network are illustrated in Figure 3.4. Actually, the network consists of two individual elements, one a matched two-port line and the other a totally mismatched one-port [37].

$$[\mathrm{S}]=\begin{bmatrix} 0 & e^{j\theta} & 0 \\ e^{j\theta} & 0 & 0 \\ 0 & 0 & e^{j\varphi} \end{bmatrix} \tag{3.18}$$

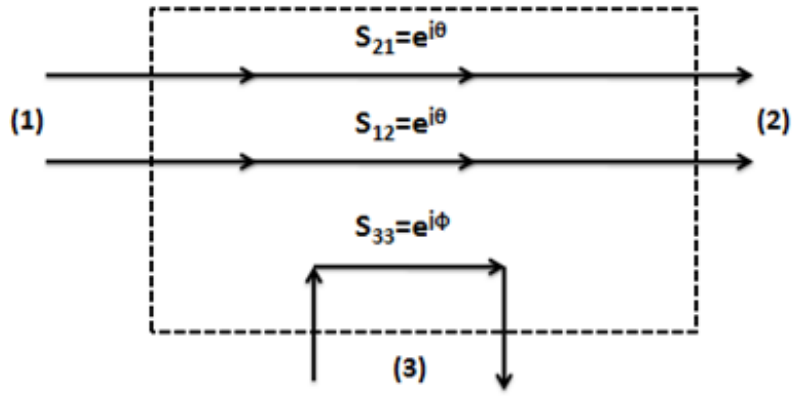


Figure 3.4: A Reciprocal, Lossless Three-Port Network Matched at Port 1 and 2 [37]

Finally, if the thee-port network is allowed to be lossy, it is able to be reciprocal and matched at all ports. This is the case of the resistive power divider, which will be discussed in the following section.

3.2.3 Resistive Power Divider Configuration

If a three-port network contains lossy components, its output ports can be all matched, although there is still no isolation between the output ports. Figure 3.5 illustrates a power divider structure using lump-element resistors.

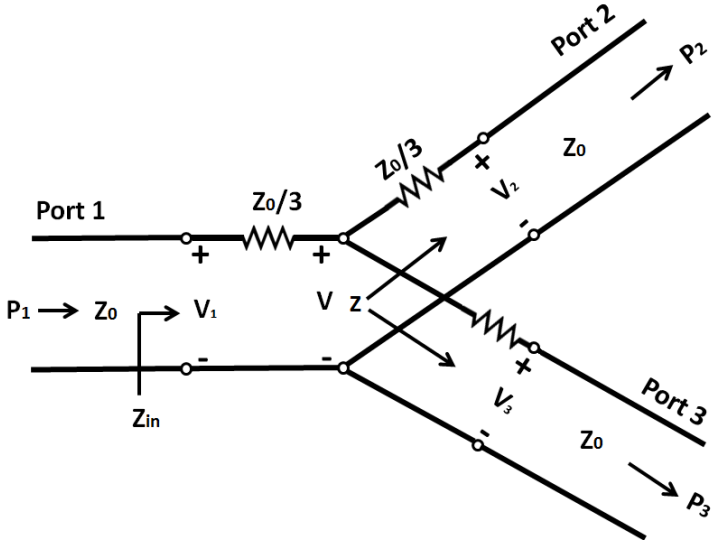


Figure 3.5: Equal-Split Three-Port Resistive Power Divider [37]

The resistive power divider can be calculated using standard circuit theory. All of the ports are terminated with the characteristic impedance Z_0. The impedance of $Z_0/3$ resistor together with the output line is defined by Equation (3.19).

$$Z = \frac{Z_0}{3} + Z_0 = \frac{4Z_0}{3} \tag{3.19}$$

The input impedance of the divider is

$$Z_{in} = \frac{Z_0}{3} + \frac{2Z_0}{3} = Z_0 \tag{3.20}$$

Equation (3.20) demonstrates that the input is matched to the feeding line. Since the resistive power divider is symmetric, all of the ports are matched.

$$S_{11} = S_{22} = S_{33} = 0 \tag{3.21}$$

If the voltage at port 1 is V_1, then the voltage at the centre of the junction is

$$V = V_1 \frac{2Z_0/3}{Z_0/3+2Z_0/3} = \frac{2}{3}V_1 \tag{3.22}$$

And the output voltages are calculated by

$$V_2 = V_3 = V\frac{Z_0}{Z_0+Z_0/3} = \frac{3}{4}V = \frac{1}{2}V_1 \tag{3.23}$$

Thus, S_{21}=S_{31}=S_{23}=1/2, refers -6dB below the input power. The resistive power divider is reciprocal, so the [S] matrix is symmetric, which could be simplified to

$$[S] = \frac{1}{2}\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix} \tag{3.24}$$

The power delivered into the resistive divider is

$$P_m = \frac{1}{2}\frac{V_1^2}{Z_0} \tag{3.25}$$

And the output powers are

$$P_2 = P_3 = \frac{1}{2}\frac{(1/2V_1)^2}{Z_0} = \frac{1}{8}\frac{V_1^2}{Z_0} = \frac{1}{4}P_m \tag{3.26}$$

Equation (3.26) illustrates that half of the power is dissipated in the resistors.

3.2.4 Wilkinson Power Divider Introduction

The T-junction power divider is lossless, but suffers from the issue of not being matched at all ports. Moreover, there is no isolation between output ports. The resistive divider can match the ports, but it is lossy and also without isolation. The Wilkinson power divider is an improved three-port network, which is lossless when the output ports are matched, with high isolation and only reflected power is dissipated.

The Wilkinson power divider can be designed to provide arbitrary power division. In this section, equal-split (3dB) structures will be presented, in order to construct the suitable feeding network for the smart antenna array system.

Various Wilkinson power dividers have been investigated and characterised. They differed in dimensions, fabrication materials, application of extra circuit components and integration methods.

With the development of microwave communication, the performance of Wilkinson power divider has been improved in many directions. In [40], an uniplanar MMIC Wilkinson power divider utilising ACPS series stubs has been presented. They use short-circuit series stubs in the signal conductor of an asymmetric coplanar stripline (ACPS) transmission line as a circuit element, in order to achieve a significant size reduction of a MMIC Wilkinson divider. The stubs are able to shorten the $\lambda/4$ transmission lines by approximately 35%. [41] proposes a method to increase the operating frequency range of a Wilkinson power divider. The broadband micro-coaxial Wilkinson divider operates from 2 to 22 GHz, demonstrating an 11: 1 bandwidth. The divider circuits are fabricated on silicon wafer with PolyStrata technology and implemented with 650μm×400 μm air-supported micro-coaxial lines. In [42], another 3dB Wilkinson power divider on low resistivity silicon substrate with a polyimide interface layer has been demonstrated. The design utilises finite ground coplanar (FGC) line technology, and operates at a centre frequency of 15 GHz. Low insertion loss, high return loss and suitable isolation are obtained. Moreover, many researchers add extra circuit elements into the Wilkinson power divider to enhance the performance. Since the quarter wave length lines have a significant dimension, causing a high MMIC fabrication cost, a lumped elements Wilkinson divider has been developed [43], which replaces the transmission lines with lumped capacitors and inductors. However, a lumped inductor with low loss and high self-resonant frequency is difficult to achieve, especially at a very high frequencies (f>10GHz). An improved lumped-distributed Wilkinson divider [44] is able to solve this problem. The structure removes the inductor and adds another two capacitors. One is between the output ports in series with the isolation resistor, and the other is in parallel with the input signal. By adjusting the capacitor values, it is possible to generate suitable RF performance and reduce the circuit dimension. Furthermore, Wilkinson power dividers can be designed to supply phase shifts to the antennas [45, 46].

3.2.5 Wilkinson Power Divider Equivalent Circuit Analysis

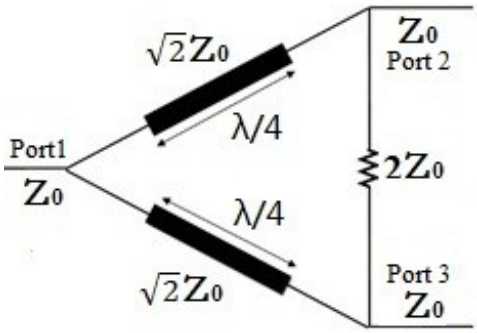


Figure 3.6: Wilkinson Power Divider Equivalent Transmission Line Circuit

Figure 3.6 depicts the equivalent transmission line circuit of Wilkinson power divider. For simplicity, all impedances can be normalised to the characteristic impedance Z_0, and the circuit is redrawn in Figure 3.7, with voltage generators at the output ports.

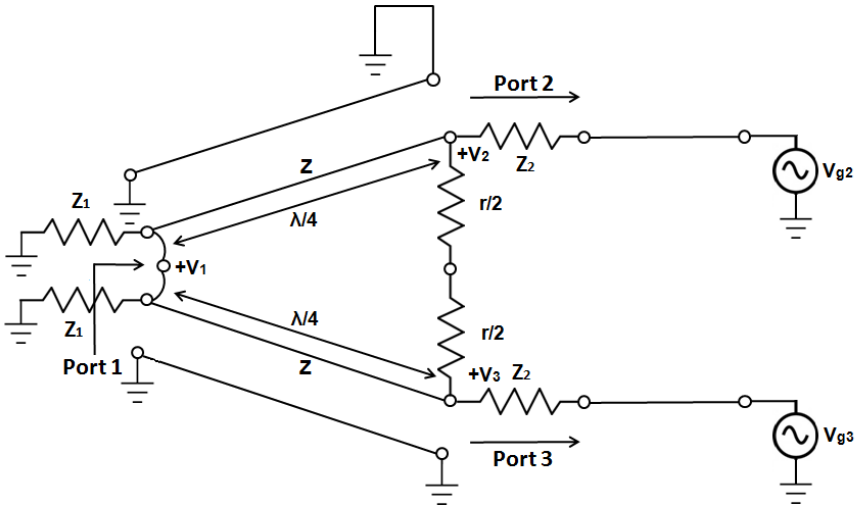


Figure 3.7: Wilkinson Power Divider in Normalised and Symmetric Form [37]

The three-port network is symmetric across the middle plane. The two source resistors Z_1 are combined in parallel to generate a resistor of normalised value. Z_2 presents the impedance of a matched source. The λ/4 transmission line shows a normalised characteristic impedance Z, and the lumped resistor has a normalised value of r. As shown in Figure 3.6, for a 3dB (equal-splitting) Wilkinson power divider, $Z = \sqrt{2}Z_0$, $r = 2Z_0$.

Even-Odd mode analysis has been used to design the Wilkinson power divider. For even mode, $V_{g2} = V_{g3} = 2V$, and in odd mode, $V_{g2} = -V_{g3} = 2V$. By superposition of the two modes, an excitation of $V_{g2} = 4V$ and $V_{g3} = 0$ could be obtained, which can be used to define the S-Parameters of the network [37].

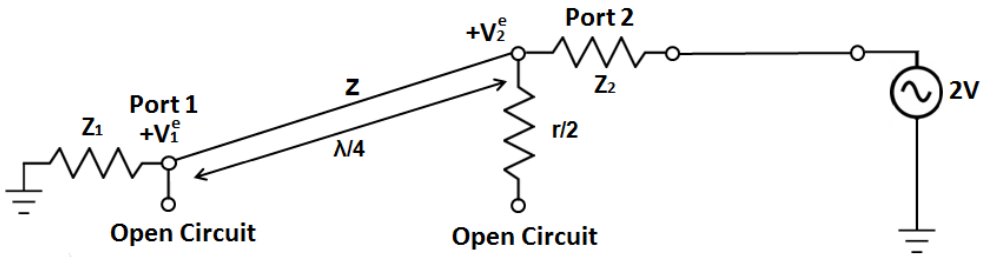


Figure 3.8: Bisection of the Circuit for Even Mode Excitation [37]

Even Mode: In the even mode excitation, $V_{g2} = V_{g3}$ =2V, $V_2^e = V_3^e$, and there is no current flow through the r/2 resistors or the short circuit between the inputs of the two transmission lines at Port 1. Then the equivalent circuit in Figure 3.7 can be simplified into bisection in Figure 3.8 with open circuits. Looking into Port 2, the impedance is

$$Z_{in}^e = \frac{Z^2}{2} \tag{3.27}$$

The transmission line works as a λ/4 transformer. If $Z = \sqrt{2}Z_0$, Port 2 will be matched for even mode excitation, and then, $V_2^e = V$, $Z_{in}^e = Z$. The r/2 resistor is superfluous in the even mode. If x=0 at Port 1 and x=- λ/4 at Port 2, the voltage on the transmission line can be written as:

$$V(x) = V^+(e^{-j\beta x} + \Gamma e^{j\beta x}) \tag{3.28}$$

$$V_2^e = V\left(-\lambda/4\right) = jV^+(1-\Gamma) = V \tag{3.29}$$

$$V_1^e = V(0) = V^+(1+\Gamma) = jV\frac{\Gamma+1}{\Gamma-1} \tag{3.30}$$

The reflection coefficient Γ is that seen at Port 1, looking to the resistor of normalised value $2Z_0$, so

$$\Gamma = \frac{2-\sqrt{2}}{2+\sqrt{2}} \tag{3.31}$$

Thus

$$V_1^e = -jV\sqrt{2} \tag{3.32}$$

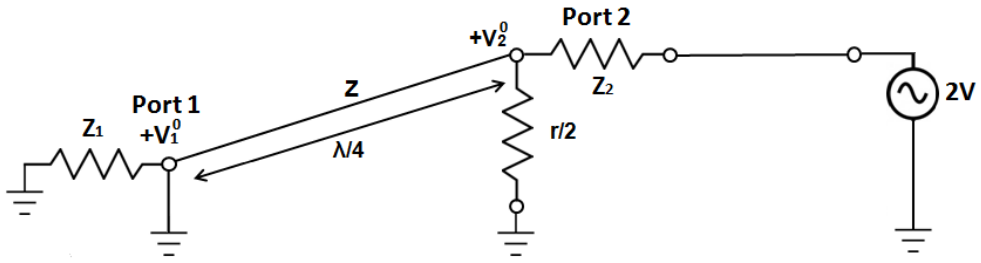
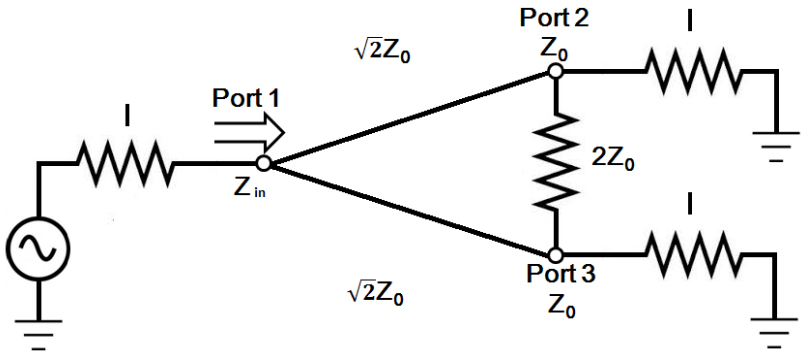


Figure 3.9: Bisection of the Circuit for Odd Mode Excitation [37]

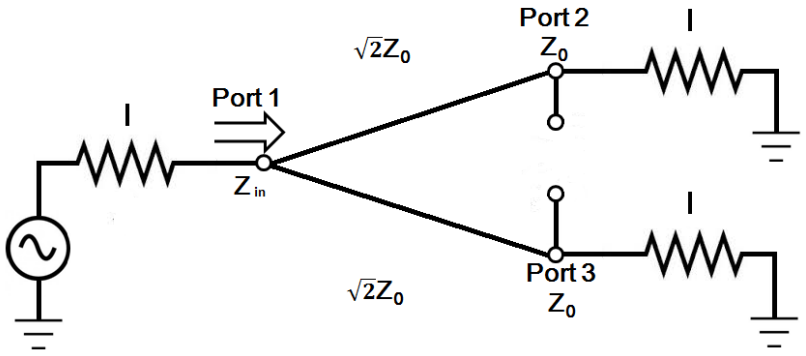
Odd Mode: In the odd mode excitation, V_{g2} = -V_{g3} =2V, $V_2^o = V_3^o$, and there is a voltage null along the middle of the equivalent circuit in Figure 3.7. The bisection circuit is illustrated in Figure 3.9, by grounding the network at two points on its middle plane. Looking into Port 2, there is an impedance of r/2. The paralleled transmission line is λ/4 long and shorted at Port 1, and it seems an open circuit at Port 2. So Port 2 will be matched in the odd mode excitation if r=2Z_0. Thus $V_2^o = V$ and $V_1^o = 0$, which means all of the power is transmitted to the r/2 resistors, none is going to Port 1.

Figure 3.10(a) shows an equivalent circuit of Wilkinson power divider when Port 2 and Port 3 are terminated in matched loads. It is similar to an even mode excitation, since V_2=V_3. There is no current flow through the resistor of 2Z_0, and it could be removed. The simplified circuit is demonstrated in Figure 3.10(b). The paralleled two λ/4 transformers are terminated in normalised loads, and the impedance is calculated by:

$$Z_{in} = \frac{1}{2}(\sqrt{2Z_0})^2 = Z_0 \tag{3.33}$$



(a)



(b)

Figure 3.10: (a). Terminated Wilkinson Power Divider (b).Bisection Wilkinson Power Divider [37]

Finally, the S-Parameters can be summarised

$$S_{11}= 0\ (Z_{in}= Z_0 \text{ at Port 1}) \tag{3.34}$$

$$S_{22} = S_{33}= 0 \text{ (Ports 2 and Port 3 are matched for even mode and odd mode)} \tag{3.35}$$

$$S_{12}=S_{21}= (V_1^e+V_1^0)/(V_2^e + V_2^0) =-j/\sqrt{2} \text{ (Symmetry due to reciprocity)} \tag{3.36}$$

$$S_{13} = S_{31}=-j/\sqrt{2} \text{ (Symmetry of Ports 2 and Port 3)} \tag{3.37}$$

$$S_{23} = S_{32}= 0 \text{ (Due to short or open at bisection)} \tag{3.38}$$

It can be seen from the above equations, all ports are matched when the divider is terminated with matched loads. When the network is driven at Port 1 and the outputs are matched, no power is dissipated in the resistor. So the Wilkinson power divider is lossless when the output ports are matched, only reflected power at Port 2 and Port 3 are lost by the resistor. Because $S_{23} = S_{32}= 0$, there is a high isolation between Port 2 and Port 3.

3.2.6 Wilkinson Power Divider Design

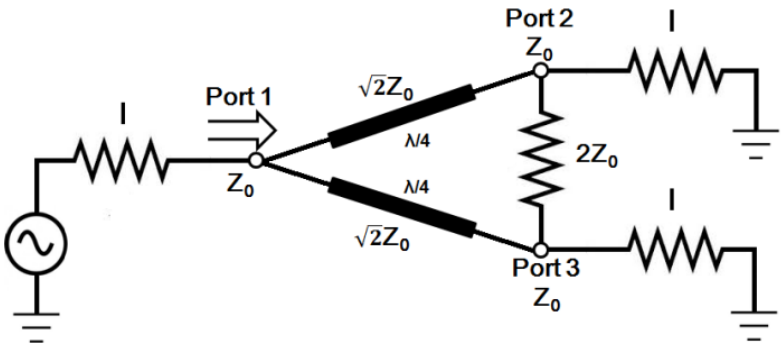


Figure 3.11: Structure of the Wilkinson Power Divider [47]

The Wilkinson power divider is one of the essential components in various wireless communication systems and it has been widely utilised for power division and combination for antenna feeding networks. In the conventional Wilkinson power divider structure, as shown in Figure 3.11, two lengths of λ/4 transmission lines with $\sqrt{2}Z_0$ impedance and a characteristic impedance of $2Z_0$ are placed between the output ports, for the purpose of providing return loss (-10dB) , insertion loss (-3.2dB), correct impedance matching (50Ω) and high isolation (-10dB).

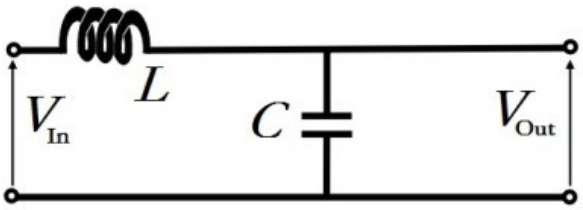


Figure 3.12: Equivalent Lumped Component Circuit of Lossless Transmission Line [48]

Figure 3.12 depicts the schematic representation of the elementary component of a lossless transmission line. Resistive effects have been neglected and there is no Joule effect loss because only reactive elements are presented. Since the dielectric substrate thickness is very thin compared to the wavelength (h<<λ), a quasi-TEM mode has been used for the circuit analysis [37]. The characteristic impedance Z_0 (50Ω) can be rewritten in Equation (3.39) and (3.40).

$$Z_0 = \frac{60}{\sqrt{\varepsilon_e}} \ln\left(\frac{8h}{w_m} + \frac{w_m}{4h}\right) \tag{3.39}$$

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_e}\left[{}^{w_m}/_{h} + 1.393 + 0.667 \ln\left({}^{w_m}/_{h} + 1.444\right)\right]} \tag{3.40}$$

Where, w_m shows the width of the transmission line and h represents the thickness of the substrate. ε_e demonstrates the effective dielectric constant of the substrate, which is given by:

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2 \times \sqrt{1 + 12h/w_m}} \tag{3.41}$$

Where, ε_r stands for the dielectric constant of the substrate. By using the equations (3.39) to (3.41), the most important parameter, port width of the Wilkinson power divider is able to be determined. Then, the full structure can be completed by utilising the following equations.

$$\beta = \frac{2\pi}{\lambda} = \frac{2\pi f}{v_p} = \frac{\omega}{v_p} = \frac{\omega\sqrt{\varepsilon_r \mu_r}}{c} = \omega\sqrt{\varepsilon_0 \mu_0} = \omega\sqrt{\varepsilon\mu} = \omega\sqrt{L \times C} \tag{3.42}$$

$$v_\rho = \frac{1}{\sqrt{\varepsilon_0 \varepsilon_r \mu_0 \mu_r}} = \frac{1}{\sqrt{\varepsilon\mu}} \tag{3.43}$$

$$z_o = \sqrt{\frac{L}{C}} \tag{3.44}$$

$$\lambda = \frac{v_p}{f} = \frac{c}{f\sqrt{\varepsilon_r \mu_r}} \tag{3.45}$$

Where, L and C illustrate the equivalent inductor and capacitor for the lossless transmission line, respectively. β stands for the wave propagation constant, v_p represents the phase velocity and ω demonstrates the angular frequency.

In this chapter, the Wilkinson power divider with two materials have been implemented and characterised. Firstly, silicon substrate and aluminium transmission lines are used to construct the power divider. The silicon substrate thickness is 380 um. The relative dielectric constant and relative permeability are 11.9 and 1, respectively. The aluminium conductor thickness is 6um and its conductivity is 3.5×10^7. Using the equations from (3.39) to (3.45), the width of the input and output ports are 0.278mm, in order to match the line impedance at 50 Ω. Secondly, copper transmission lines with a conductivity of 5.89×10^7 was etched on an FR4 printed circuit board (with a thickness h=1.6mm and relative dielectric constant, ε_r=4.55). The operating frequency is 2.45GHz, targeting WiFi applications. By calculation, the width of the input and output ports are 3.09mm.

Based on the above design procedures, several individual Wilkinson power dividers have been designed, calculated and simulated using electromagnetic simulators, Agilent Advanced Design System (ADS) and CST Microwave Studio. The following S-Parameters have been observed and optimised.

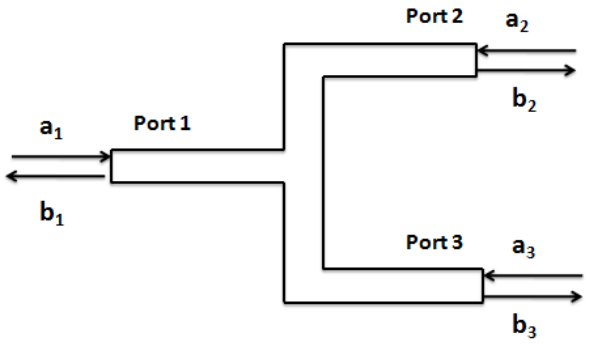


Figure 3.13: S-Parameter Relationships

S_{11}= 20 $\log_{10}$ ($\frac{b_1}{a_1}$), which represents the reflection coefficient at the input port.

S_{22}= 20 $\log_{10}$ ($\frac{b_2}{a_2}$), which demonstrates the reflection coefficient at the output port.

S_{21}= 20 $\log_{10}$ ($\frac{b_2}{a_1}$), which shows the forward gain between the input and output.

$S_{23}= 20 \log_{10}(\frac{b_2}{b_3})$, which illustrates the isolation coefficient between the two output ports

S_{11} is related to the return loss and S_{21} could be used to determine the insertion loss.

Return loss is the negative of the magnitude of the reflection coefficient in dB. Since power is proportional to the square of the voltage, return loss is given by:

$$\text{Return Loss} = -20\log_{10}|S_{11}| \tag{3.46}$$

Insertion loss is defined as

$$\text{Insertion Loss} = -20\log_{10}|S_{21}| \tag{3.47}$$

Based on the fundamental Wilkinson power divider, multiband and reconfigurable feeding networks for smart antenna arrays have been constructed.

3.3 Enhanced Wilkinson Divider on Si Substrate for Energy Efficient Microwave Applications

3.3.1 Introduction

The Wilkinson Power Divider is one of the essential components in radio frequency design field, used mainly for power division or combination in different microwave applications such as balanced amplifiers, mixers, and feeding networks of antenna arrays. Presently works have demonstrated that the performance of the conventional Wilkinson power divider can be improved by utilising different technologies. There are two approaches in the literature to increase the operating bandwidth of the divider. The first approach uses resonators [49], planar artificial transmission lines [50], coupled lines [51], and lumped elements [52], in order to achieve a multi-frequency Wilkinson power divider. The other approach utilising multi-layered structure [53], multi-section λ/4 lines [46, 54], and composite right-left-handed transmission lines [55], to generate an ultra wideband (UWB) Wilkinson divider. Meanwhile, there are lots of efforts to miniaturise the power dividers dimensions [56-58]. However, most of the geometries are based on FR4 substrate, which limits the miniaturisation and performance.

This section presents the design, simulation, fabrication, and experimental results of an enhanced 1:2 Wilkinson Power Divider fabricated on high resistivity Silicon (HRS) and aluminium wafer. Designed and simulated in Agilent Advanced Design System, this structure exceeds the characteristics of many Wilkinson dividers presented recently in the literature. The enhanced design provides suitable S-parameters and with significantly size reduction, by using Silicon substrate and optimising the transmission line segments from λ/4 to λ/8,

targeting compact portable devices. At the desired frequency (2.4GHz), the reflection coefficients at input and output ports are smaller than -42dB, compared to -30dB for previous designs on FR4 substrate. For the insertion loss and isolation coefficient, the enhanced design also demonstrates better performance results. Fabrication and measurement results closely correlate with those obtained during simulations. The presented configuration is particularly suited to energy efficient microwave systems [59].

3.3.2 Enhanced Wilkinson Power Divider Geometry

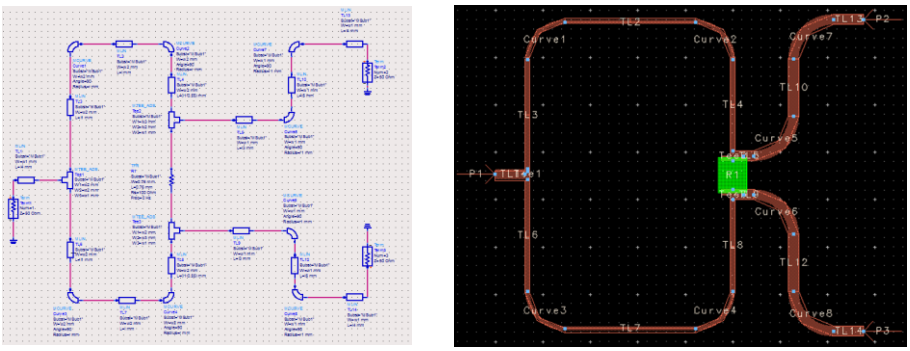


Figure 3.14: Enhanced Wilkinson Power Divider (a) Schematic (b) Layout [59]

Figure 3.14 illustrates the configuration of the enhanced Wilkinson power divider. The structure is designed to cover 2.4GHz, applying for WiFi and Bluetooth standards. For material properties, the silicon substrate thickness is 380 um, the relative dielectric constant is 11.9 and the resistivity is (ρ>25000S/m). The aluminium conductor thickness is 6um and its conductivity is 3.5×10^{7}. The design utilises a 100Ω smallest thin-film centre-tapped resistor (CTR, 0.76mm x 0.76mm) from VISHAY to provide perfect isolation [60], as illustrated in Figure 3.15. The CTR series is a centre-tapped chip resistor providing excellent stability with 250mW power levels. Moreover, the CTR's six bonding pads allow the user to increase layout flexibility [60]. VISHAY CTR chip resistor chips are mainly used in RF circuits where ratio matching, high power and tracking between two resistors is critical. A simulated model of this resistor is placed between the output ports (green block in Figure 3.14(b)).

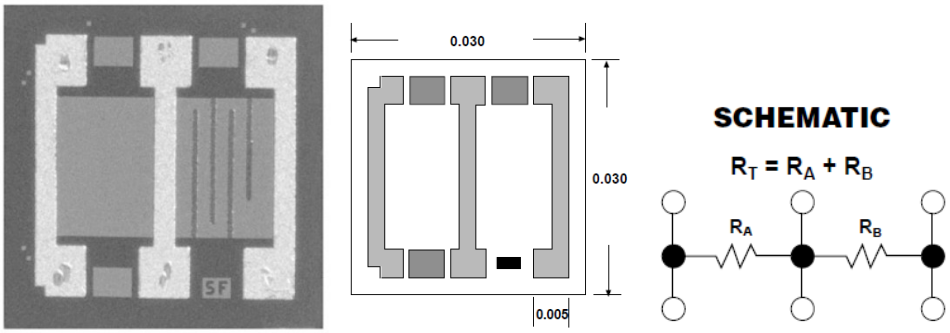
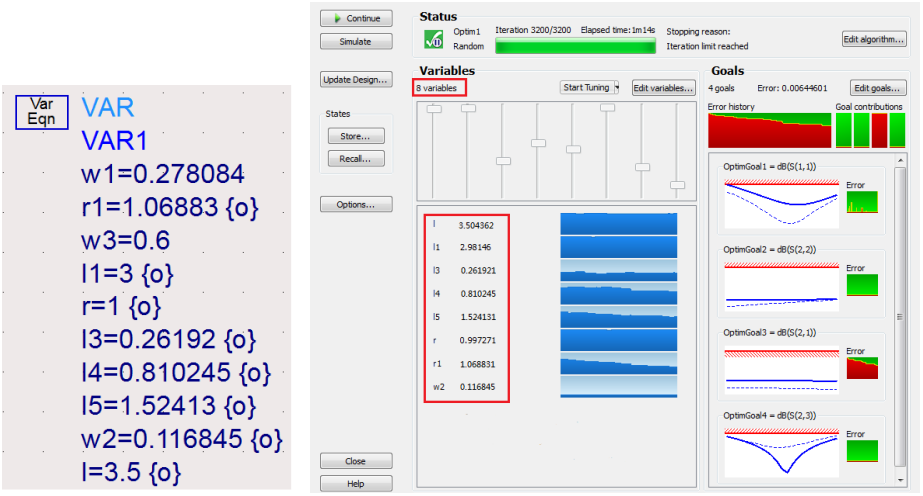


Figure 3.15: Thin Film, Centre-Tapped Resistors (CTR)



(a) **(b)**

Figure 3.16: (a) Wilkinson Power Divider Design Parameters (b) Optimisation Results

By using the equations in Section 3.2, the design parameters of the Wilkinson power divider have been calculated, as showed in Figure 3.16(a). In ADS, S_{11}, S_{21}, S_{22} and S_{23} are defined as optimisation targets. Length of the λ/4 transmission lines and size of the output ports are variables which have been optimised, in order to miniaturise the circuit dimension and achieve suitable S-parameters (as illustrated in Figure 3.16(b)). By using the high relative dielectric constant and high resistivity silicon substrate, much better S-Parameters are achieved compared to those dividers fabricated on FR4. Figure 3.17 illustrates the optimised configuration.

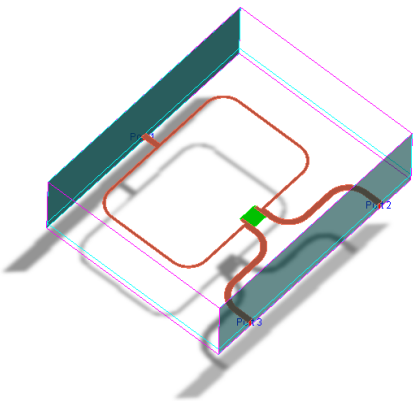


Figure 3.17: 3D View of the Optimised Enhanced Wilkinson Power Divider

Figure 3.18 to Figure 3.21 demonstrate the simulated S_{11}, S_{22}, S_{21} and S_{23} results of the proposed enhanced Wilkinson power divider. The reflection coefficients at input and output ports are all smaller than -35dB at 2.4GHz. The insertion loss between Port 2 and Port 1 is

3.2dB, which showing the divider is splitting power equally. Figure 3.21 depicts that good isolation (-39dB) has been obtained between the output ports at the centre frequency.

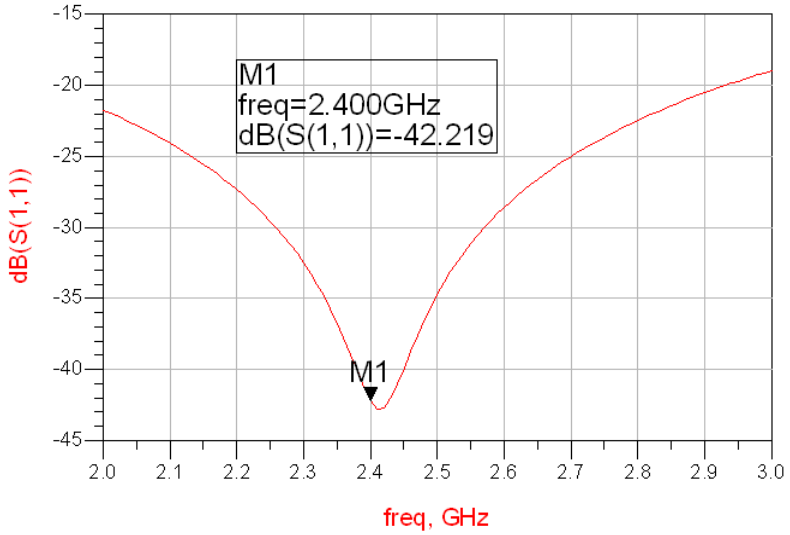


Figure 3.18: Simulated Reflection Coefficient (S_{11}) at the Input Port is -42.219dB at 2.4GHz

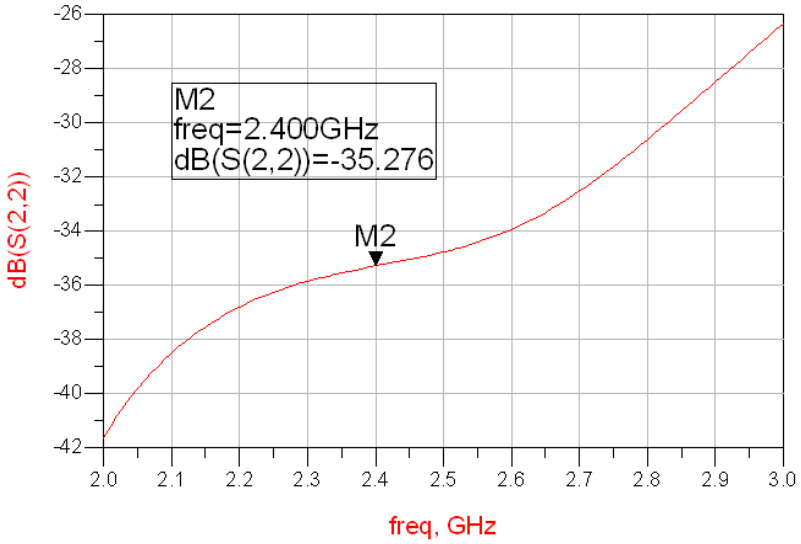


Figure 3.19: Simulated Reflection Coefficient (S_{22}) at the Output Port is -35.276dB at 2.4GHz

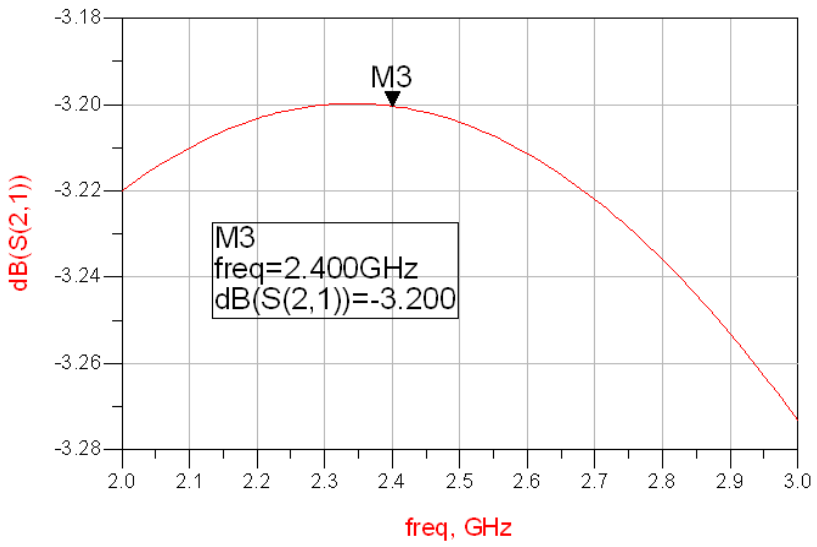


Figure 3.20: Simulated Insertion Loss between Port 2 and Port 1 is 3.2dB at 2.4GHz

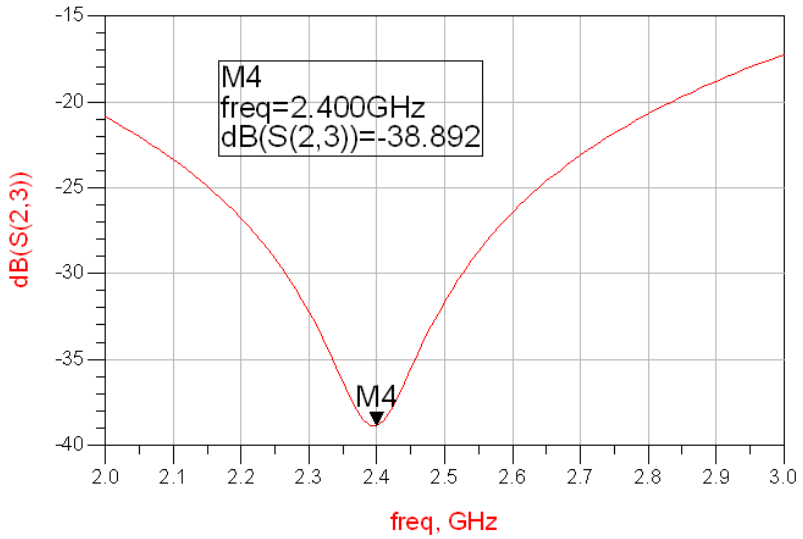


Figure 3.21: A Good Isolation (S_{23}) is Achieved (-38.892dB) Between Output Ports

Dimension of the enhanced Wilkinson power divider is 9.9mm × 8.64mm. Accordingly, the occupied space of the proposed geometry is only 35% of that of the conventional Wilkinson power [61]. The proposed configuration is constructed on high resistivity Silicon (HRS) wafers (ρ>25000S/m), which are utilised to overcome some disadvantages of traditional microwave circuits, such as the high loss of lumped elements, transmission lines, filters and antennas [62-64]. Compared to another Wilkinson power divider fabricated on low resistivity Si substrate with a polyimide interface layer [65], the proposed implementation is demonstrating much better S_{11} performance (-42dB versus -20dB).

3.3.3 Enhanced Wilkinson Power Divider Fabrication and Characterisation

The enhanced Wilkinson power divider has been fabricated on high resistivity silicon wafer, in the Scottish Microelectronics Centre (SMC). Figure 3.22 demonstrates the wafer layout. The original wafer is shown in Figure 3.23(a), and the components after dicing are presented in Figure 3.23(b).

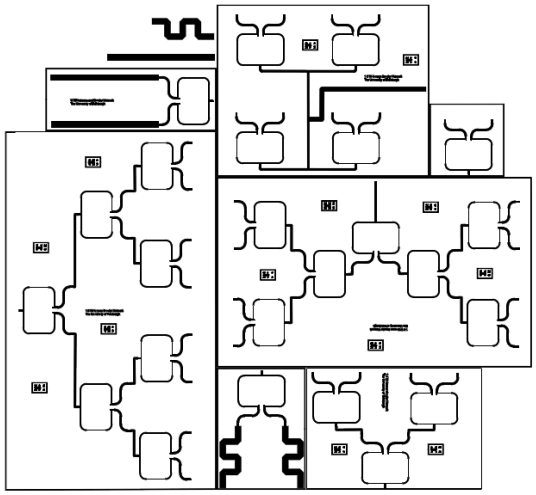
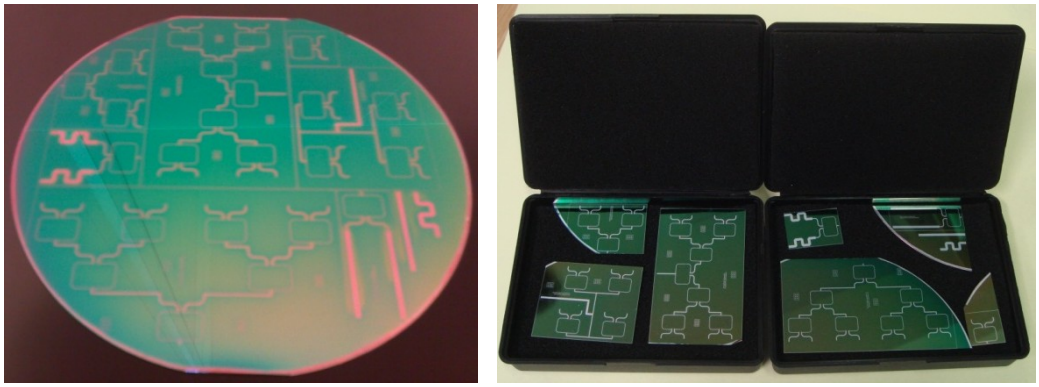


Figure 3.22: Silicon Wafer Layout



(a) **(b)**

Figure 3.23: (a) Original Wafer (b) Test Components after Dicing

The divider has been subsequently characterised with an HP8753C vector network analyser (VNA), controlled by a PC, a Bausch & Lomb microscope and an RF probe station (illustrated in Figure 3.24 and Figure 3.25). Calibration was done with Short-Open-Load-Through (SLOT) using an impedance standard substrate.

Figure 3.24: Vector Network Analyser, PC, Microscope and RF Probe Station

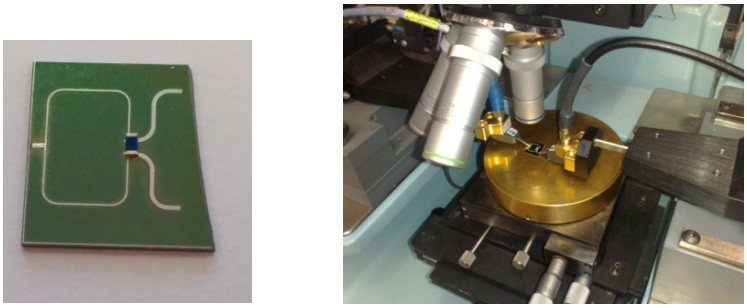


Figure 3.25: The Fabricated Divider and RF Probes Measurement

Since the Wilkinson power divider is a three port network and the VNA is a two port system, the third port of the divider was terminated with a specially built microprobe that incorporates a 50 termination.

Figure 3.26 demonstrates the measured S_{11} of the enhanced Wilkinson power divider, which is -42.637dB at the desired frequency (2.4GHz).

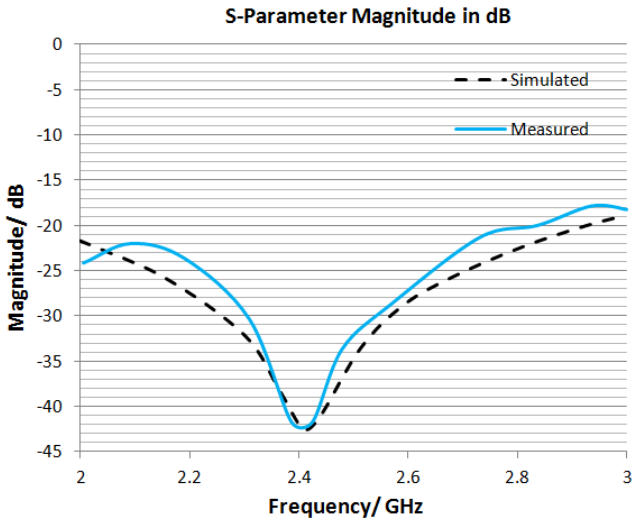


Figure 3.26: Measured S_{11} of the Enhanced Wilkinson Power Divider: S_{11} is -41.637dB at 2.4GHz

Table 3.1 compares the simulated and measured S-Parameters of the enhanced silicon based Wilkinson power divider.

Table 3.1: S-Parameters of the Enhanced Wilkinson Power Divider

	S_{11}(dB)	S_{22}(dB)	S_{21}(dB)	S_{23}(dB)
Simulation	-42.21	-35.27	-3.21	-38.89
Measurement	-42.63	-32.32	-3.29	-35.17

From Table 3.1, it is clear that a good consistency between the simulated and measured S-Parameters. At the centre frequency (2.4GHz), the reflection coefficient (S_{11}) of the proposed divider was simulated and measured to be smaller than -40dB. The insertion loss between the input and output ports was simulated and measured to be around 3.2dB (showing equal-splitting). Similarly, the isolation coefficient (S_{23}) between the output ports was measured to be smaller than -35dB. There is a slight discrepancy at the resonance frequency, which could be attributed to either fabrication errors or a small deviation of the silicon dielectric constant from 11.9. The only disadvantage of the proposed structure is the cost of silicon substrate. The developed feeding networks can be applied to industrial, scientific, SIMO communication and energy efficient microwave systems.

3.4 A WiFi/LTE Compact Feeding Network for an 8-Element Circular Antenna Array

3.4.1 Introduction

A Wilkinson power divider is a fundamental element in microwave systems such as the feeding network of an antenna array. Currently, most researches in this area focus on multiple operating frequencies [49, 51], broadband operating frequency ranges [66, 67] and unequalled power deviation [68-70]. However, majority of these structures are aimed at linear antenna arrays.

An antenna array which combines several individual antenna elements in certain electrical and geometrical configurations can satisfy the gain and highly directive radiation pattern required by long distance communication systems [71, 72]. By applying different algorithms and methods, classical linear arrays can be designed to generate a radiation pattern to match the desired pattern as closely as possible [73, 74]. Furthermore, interests in the development of antenna arrays with other geometrical shapes have been steadily on the rise. For example,

circular antenna arrays have various applications in radar, sensor and commercial satellite communication systems [75, 76].

This section demonstrates a novel one-to-eight compact feeding network based on Wilkinson power dividers for a circular antenna array. The network is composed of four 1:2 conventional Wilkinson power dividers. The outputs are revolved at 45° in order to satisfy the circular geometry on an FR4 substrate. Antenna elements are connected at the opposite side of the substrate through eight feeding pins. Furthermore, dimension of the feeding network has been optimised and miniaturised targeting compact portable devices. The proposed structure is applied to WiFi and LTE/LTE frequency bands. Designed and examined with the CST Microwave Studio, this feeding network provides high return loss (10dB), suitable insertion loss (9.6dB) and high isolation (-10dB) parameters for the designated frequency ranges. Fabrication and measurement results closely correlate with simulation results. The configuration can be used in SIMO and MIMO communication systems [77].

3.4.2 Individual Modified Wilkinson Power Divider Geometry

The schematic of fundamental Wilkinson power divider is illustrated in Section 3.2.6. In this design, the resonant frequencies are tuned for 2.45GHz and 2.6GHz, targeting WiFi and LTE/4G frequency bands. For FR4 substrate and copper transmission lines, the following parameters are utilised: substrate thickness = 1.6mm, relative permeability of FR4 = 1, relative dielectric constant of FR4 = 4.3, conductor thickness = 35um, and conductor conductivity = 5.89×10^7. The width of the input port and output ports are set to 3.059mm in order to match the line impedance at 50Ω. The design has been calculated using the methods in Section 3.2 6, and then simulated and optimised for the S-Parameter performance.

Figure 3.27 presents the structure of the single Wilkinson power divider. The design was simulated and verified with CST Microwave Studio. An RF resistor is placed between the output ports to provide high isolation (-10dB). According to discrete component manufacturer, VISHAY, the smallest thin-film, centre-tapped resistor (CTR) is 0.76mm x 0.76mm. A model of this resistor has been made and placed in the middle of the two output ports.

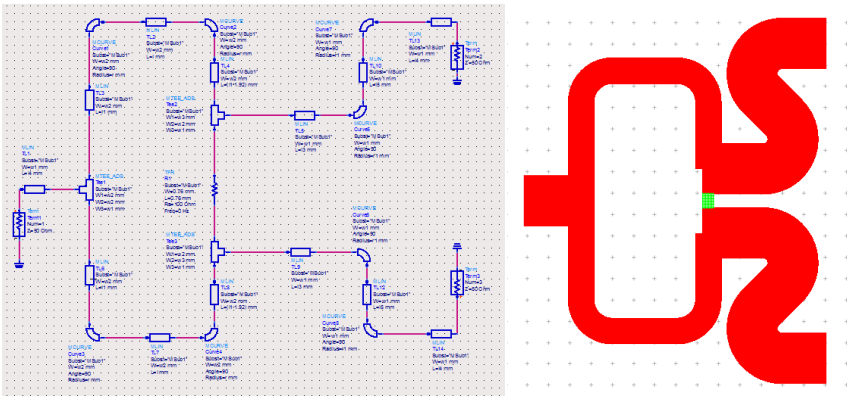
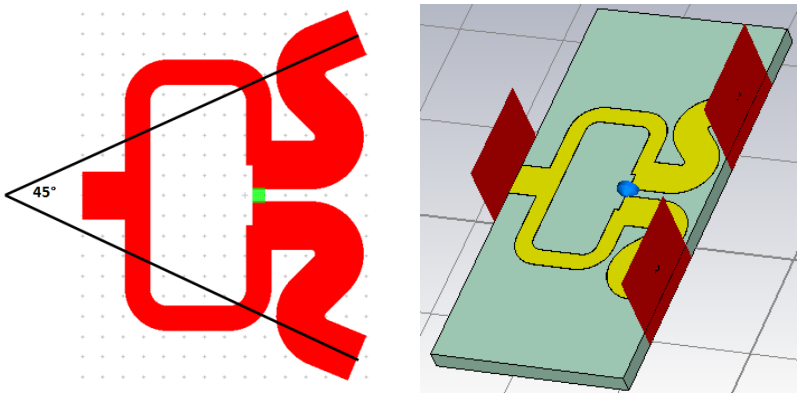


Figure 3.27: Individual Wilkinson Power Divider

For an 8-element circular antenna array, the separation angle between output ports is 360/8=45°. Figure 3.28(a) plots the modified Wilkinson power divider whose outputs have been rotated in order to obtain 45° angle. The lengths of the output transmission lines are made long enough in order to satisfy the requirements for circular feeding network. Figure 3.28(b) depicts the optimised structure of the modified Wilkinson power divider. The target frequencies are 2.45GHz and 2.6GHz.



(a) **(b)**

Figure 3.28: (a) Modified Wilkinson Power Divider (b) Optimised Structure Based on the Modified Wilkinson Power Divider

Figure 3.29 presents the simulated S_{11} for the optimised and modified Wilkinson power divider. The reflection coefficient at Port 1 (S_{11}) is -14.905dB and -15.348dB for 2.45GHz and 2.6GHz, respectively.

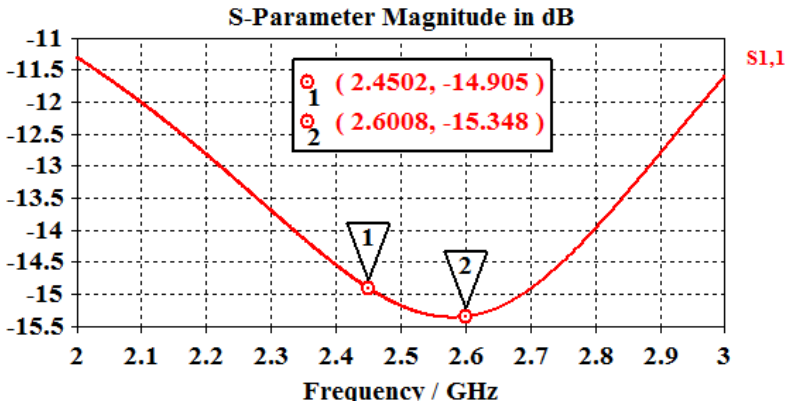


Figure 3.29: Simulated Reflection Coefficient (S_{11}) of the Proposed Optimised Wilkinson Power Divider

Table 3.2 summarises all simulated S-Parameters of the optimised Wilkinson power divider at 2.45GHz and 2.6GHz. It is clear from simulation results that the return loss, insertion loss and isolations are all adequate for the required frequency ranges. The dimension of this optimised layout is 21mm × 18mm. The total size can be miniaturised further to meet different requirements.

Table 3.2: Simulated S-Parameters of the Optimised Wilkinson Power Divider

	S_{11}(dB)	S_{22}(dB)	S_{21}(dB)	S_{23}(dB)
2.45 GHz	-14.9	-14.3	-3.2	-21
2.6 GHz	-15.3	-14.6	-3.2	-23

3.4.3 Feeding Network Configuration

Four of the optimised Wilkinson power dividers have been connected in order to create a circular feeding network, as illustrated in Figure 3.30. The sections of the feeding network are revolved at an angle of 45° with respect to output waveguides of the power divider. The radius of the presented circular feeding network is 25mm.

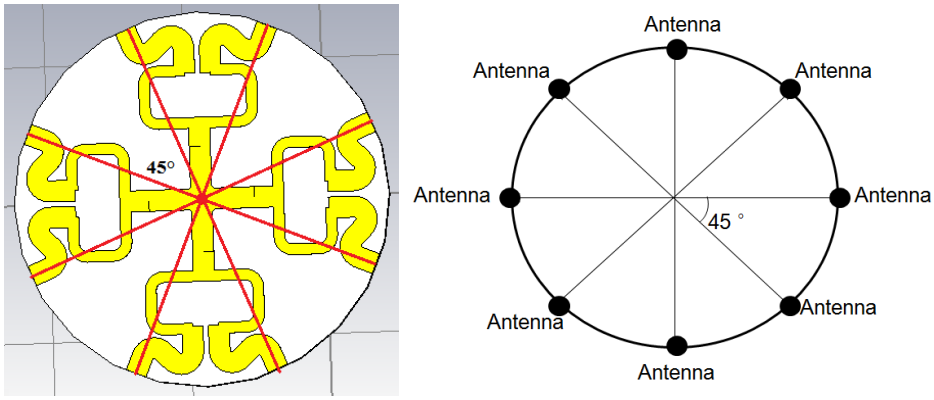


Figure 3.30: Structure of the Circular Feeding Network

In order to achieve suitable reflection coefficient at the power input port (S_{11}), a meandered structure was used, as shown in Figure 3.31.

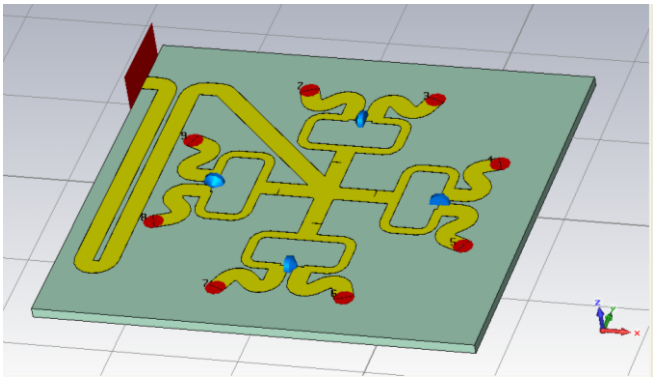


Figure 3.31: Geometry of the Circular Feeding Network with Meandered Input

This circular feeding network has been fabricated using the same dimensions from the simulation environment. Figure 3.32 demonstrates a photo of the fabricated circular feeding network.

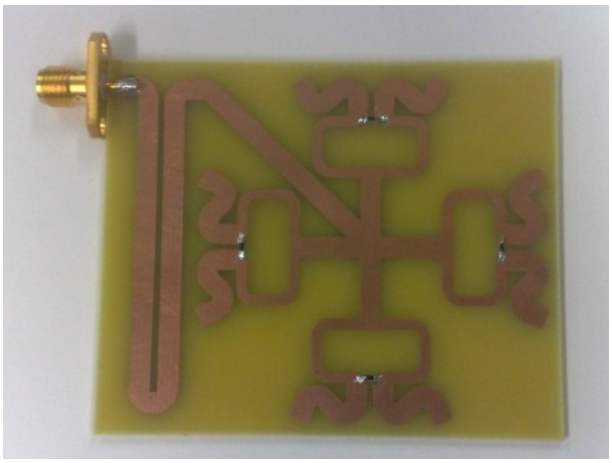


Figure 3.32: Photo of the Fabricated Prototype of the Circular Feeding Network

S-Parameter measurements were conducted using an HP8753C network analyser. Figure 3.33 and Figure 3.34 show the simulated and measured reflection coefficient S_{11} respectively of the circular one-to-eight feeding network.

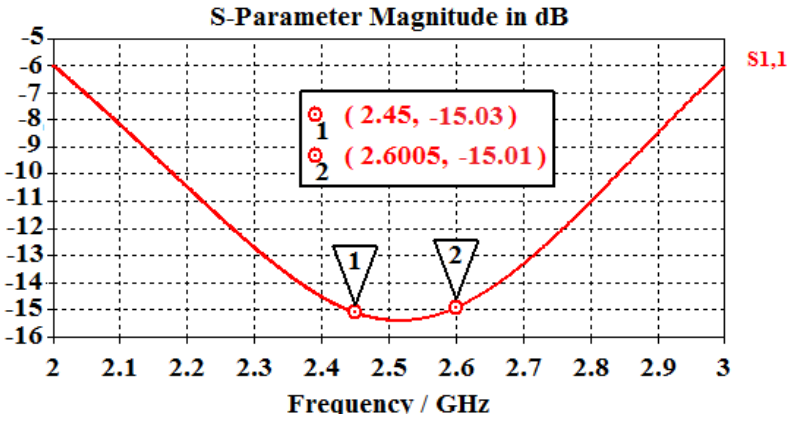


Figure 3.33: Simulated S_{11}: S_{11} is -15.03dB and -15.01dB at 2.45GHz and 2.6GHz

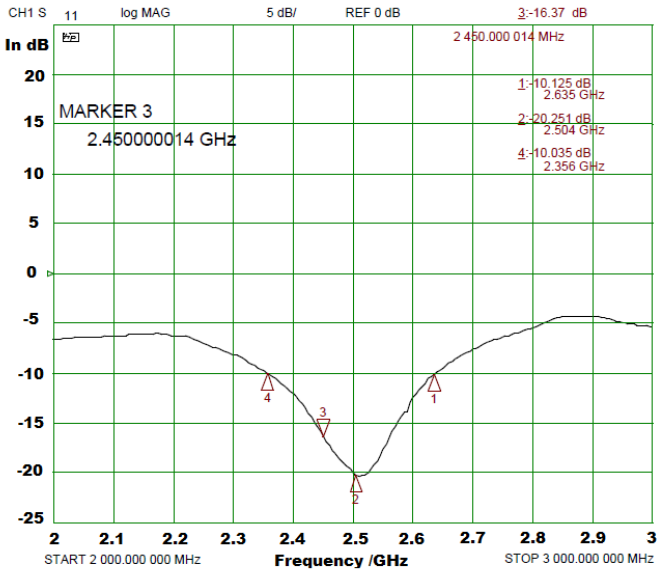


Figure 3.34: Measured S_{11} Parameter: S_{11} is -16.37dB and -12.34dB at 2.45GHz and 2.6GHz

Table 3.3 compares the simulated and measured S-Parameters of the circular feeding network at 2.45GHz and 2.6GHz. Clearly the results reveal a good correlation between simulation and measurement. The reflection coefficients (S_{11}, S_{22}, S_{33},...S_{99}) are all under -10dB. Theoretically, for an eight port feeding network, the forward gains (S_{21}, S_{31},...S_{91}) should be around -9.6dB [37]. The measured gains are around -10.2dB, which are strongly deteriorated by high FR4 substrate losses. High isolation coefficients (-10dB) between adjacent ports (S_{23}, S_{34},...S_{89}) have been achieved.

Table 3.3: Simulated and Measured S-Parameters for Circular Feeding Network

	2.45GHz Simulated	2.45GHz Measured	2.6GHz Simulated	2.6GHz Measured
S_{11}	-15 dB	-16.4 dB	-15 dB	-12.3 dB
S_{22}	-13 dB	-14 dB	-14 dB	-12 dB
S_{33}	-13 dB	-12 dB	-14 dB	-12 dB
S_{44}	-12 dB	-13 dB	-13 dB	-11 dB
S_{55}	-13 dB	-12 dB	-13 dB	-11 dB
S_{66}	-12 dB	-13 dB	-12 dB	-10 dB
S_{77}	-13 dB	-12 dB	-14 dB	-11 dB
S_{88}	-13 dB	-13 dB	-14 dB	-12 dB
S_{99}	-12 dB	-13 dB	-13 dB	-11dB
S_{21}	-9.6 dB	-9.9 dB	-9.7dB	-9.9 dB
S_{31}	-9.7 dB	-10.1 dB	-9.8dB	-10.3 dB
S_{41}	-9.8 dB	-10.3 dB	-10.1dB	-10.4 dB
S_{51}	-9.9 dB	-10.2 dB	-9.9 dB	-10.3 dB
S_{61}	-9.9 dB	-10.3 dB	-10dB	-10.4 dB
S_{71}	-10 dB	-10.4 dB	-10.1dB	-10.5 dB
S_{81}	-9.8 dB	-10.1 dB	-9.9 dB	-10.4 dB
S_{91}	-9.9 dB	-10.3 dB	-9.9 dB	-10.3dB
S_{23}	-15 dB	-18 dB	-16 dB	-15 dB
S_{34}	-14 dB	-19 dB	-15 dB	-14 dB
S_{45}	-14 dB	-18 dB	-15 dB	-14dB
S_{56}	-13 dB	-17 dB	-14 dB	-13 dB
S_{67}	-15 dB	-20 dB	-15 dB	-14 dB
S_{78}	-12 dB	-15 dB	-13 dB	-15 dB
S_{89}	-14 dB	-18 dB	-14 dB	-16 dB

The design, simulation and measurement results of a novel one-to-eight compact circular feeding network have been described. The proposed configuration consists of four 1:2 optimised Wilkinson power dividers with outputs revolving at an angle of 45° to suit circular antenna arrays. The structure presents suitable S-Parameters and occupies a small size of 25mm radius circle (area of 1986mm^2). At the desired frequencies 2.45GHz and 2.6GHz, the circular feeding network provides low reflection coefficient (-16.4dB, -12.3dB), suitable forward gain (-10.2dB, -10.2dB) and high isolation coefficient (-14dB, -15dB). A good correlation between simulation and measurement has been obtained.

3.5 A Reconfigurable Feeding Network for a Dual Circularly Polarised Antenna Array

3.5.1 Introduction

The continuous miniaturisation of transceivers for mobile communications leads to an increasing demand for low profile, lightweight, compact, multiband and multi-function antennas. Reconfigurable mobile terminals have been developed which can fulfil these requirements but these require a single reconfigurable antenna element that is effective for the multiple systems. In a reconfigurable antenna, characteristics such as the operating frequency, bandwidth and radiation pattern could be modified in order to achieve different targets [78-80].

An important property of electromagnetic wave propagation is the polarisation of the electric field (E), which is determined by the orientation of the E vector as it varies in time [81]. When the electromagnetic wave travels in free space, it propagates as a transverse wave, and the polarisation is perpendicular to the wave's direction of travel. In this case, if the electric field is oriented in a single direction, it defines as linear polarisation (horizontal or vertical). Otherwise, if the electric field rotates as the electromagnetic wave travels, it is defined as circular polarisation or elliptical polarisation [82]. Depending on the direction of electric field rotation (clockwise or counter-clockwise), left-hand circular polarisation (LHCP) and right-hand circular polarisation (RHCP) could be excited, respectively. Television broadcasting utilises linear polarisation and it is generally horizontally polarised. Several cellular operators use dual linear polarised propagation with the purpose of reducing the multipath interference, which otherwise produces fading. Nevertheless, for most of the point-to-point communication systems, such as radio frequency identification (RFID), satellite, navigation and mobile devices, it is preferable to operate with circular polarisation. The use of circular polarisation (CP) removes the need to continuously align the two antennas, maximises received power and also avoids the need of complex tracking systems.

There are many methods to obtain CP, including feeding ring slot antenna with a strip line hybrid coupler [83], adding a fan-shaped patch for an annular-ring antenna [84], cutting slot in a patch antenna [85], or applying mono-strip in the printed slot element to excite two near-degenerate orthogonal resonant modes of equal amplitude and 90º phase difference [86]. CP antenna arrays, which combine individual antenna elements are able to achieve the directivity and gain requirements for long distance communication [77]. In [87], four circularly polarised antennas are excited by a standard T-junction power divider. In [88] and [89], four standard patch antennas are fed in phase quadrature to generate 90º phase difference for generating CP.

Moreover, [90] demonstrates an elliptical CP dielectric resonator antenna array using sequential feeding networks. However, all of these structures can only achieve single direction CP. Dual circularly polarised antenna arrays are presented in [91] and [92], but they have either complex multilayer structures or complicated switching arrangements.

This section describes a novel miniaturised reconfigurable, switchable feeding network for a four elements dual circularly polarised antenna array. The four feeds are in phase quadrature to generate a phase shift of 90º between each neighbouring antenna element, producing a circularly polarised pattern. The feeding network consists of three optimised Wilkinson power dividers which can be individually reconfigured in length using PIN diodes switches. By controlling the bias voltages on these PIN diodes, the 90º phase increment can be allocated in either clockwise or counter-clockwise directions. Two orthogonal patterns with left-hand circular polarisation (LHCP) and right-hand circular polarisation (RHCP) are obtained. The operating frequency is 2.45GHz, targeting WiFi/Bluetooth applications. Full-wave simulations were carried out using Agilent Advanced Design System (ADS). With carefully miniaturisation and optimisation, the feeding network achieves a high return loss (10dB), equal power splitting, suitable insertion loss (3.2dB), high isolation (-10dB) and accurate phase difference. Fabrication and measurement results closely correlate with those obtained from simulations. The reconfigurable feeding network is particularly useful for diversity reception to combat channel fading in indoor wireless LAN applications [47].

3.5.2 Individual Wilkinson Power Divider Architecture

The Wilkinson power divider is one of the essential components in various radio frequency circuits and it has been widely used for power division and combination for antenna feeding networks. For the conventional Wilkinson power divider configuration, as discussed in Section 3.2.6, two lengths of λ/4 transmission lines with $\sqrt{2}Z_0$ impedance and a characteristic impedance of $2Z_0$ are utilised between the output ports, for the purpose of providing low insertion loss, accurate impedance matching and perfect isolation. When Port 2 and Port 3 are matched, the Wilkinson divider is a lossless network and only reflected power is dissipated [37].

In this implementation, copper transmission lines with a conductivity of 5.89×10^7 were etched on an FR4 printed circuit board (with a thickness h=1.6mm and relative dielectric constant, εr=4.55). The operating frequency is designed at 2.45GHz, targeting WiFi/Bluetooth applications.

Two individual Wilkinson power dividers (as shown in Figure 3.35 and Figure 3.36) have been designed, calculated, simulated and optimised using an electromagnetic simulator, namely Agilent Advanced Design System (ADS), for full-wave analysis.

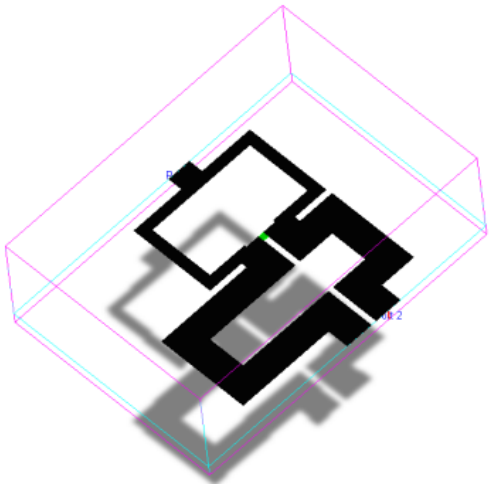


Figure 3.35: Wilkinson Power Divider with 90º Phase Shift

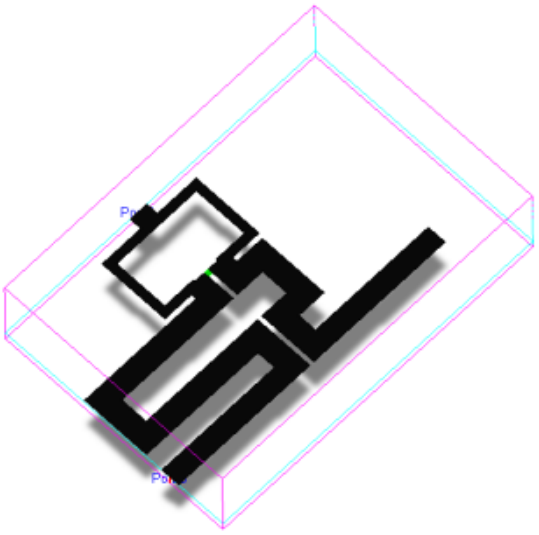


Figure 3.36: Wilkinson Power Divider with 180º Phase Shift

In Figure 3.35, the length of Port 3 is λ/4 longer than Port 2, which provides a 90º phase difference between the two outputs. Similarly, Figure 3.36 shows a Wilkinson power divider with λ/2 length difference, in order to produce a 180º phase shift. The simulation results of the two initial Wilkinson power divider geometries are plotted in Figure 3.37 to Figure 3.40.

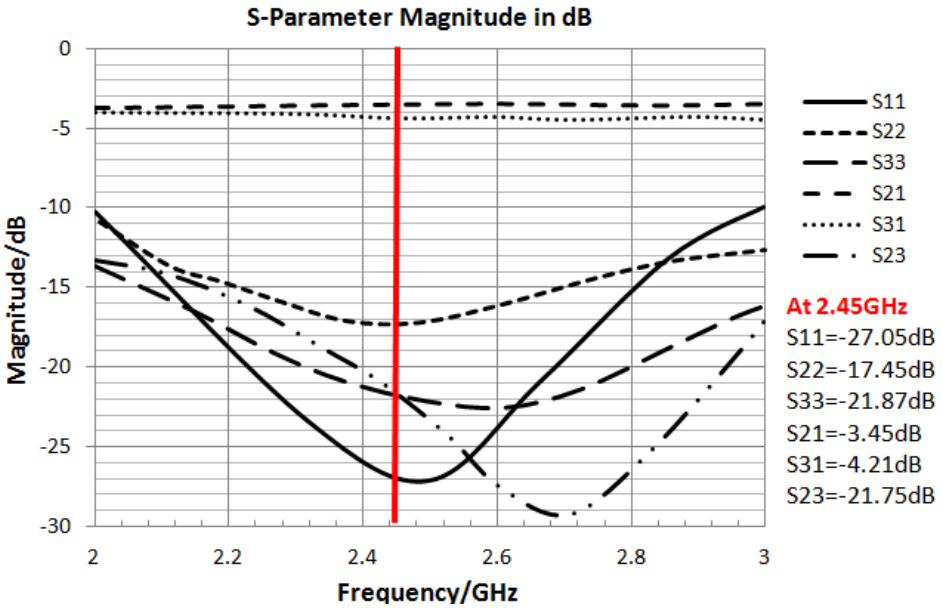


Figure 3.37: Simulated S-Parameters (Magnitude) of Wilkinson Power Divider with 90º Phase Shift

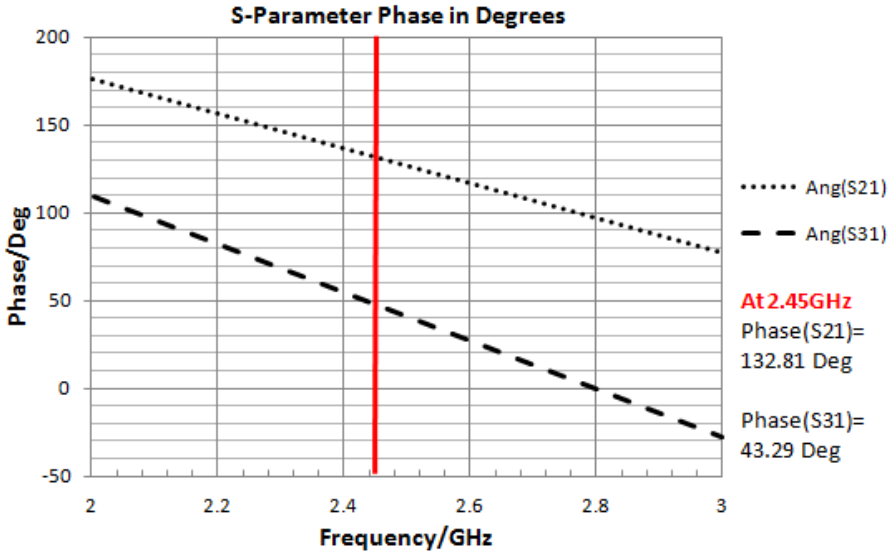


Figure 3.38: Simulated S-Parameters (Phase) of Wilkinson Power Divider with 90º Phase Shift

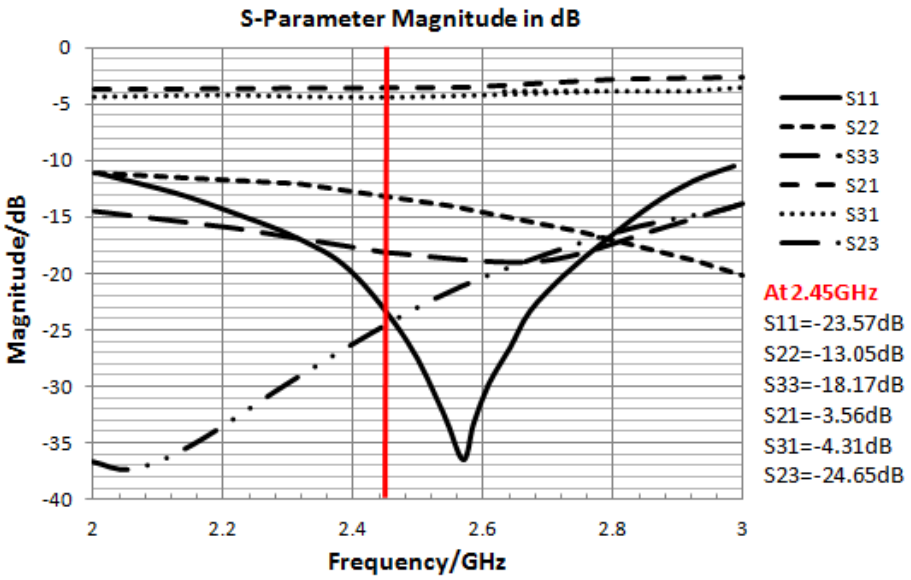


Figure 3.39: Simulated S-Parameters (Magnitude) of Wilkinson Power Divider with 180º Phase Shift

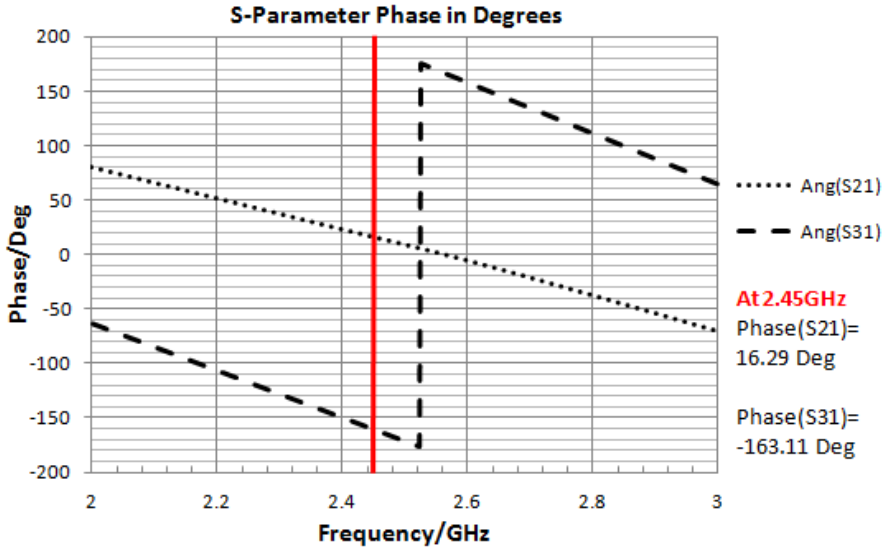


Figure 3.40: Simulated S-Parameters (Phase) of Wilkinson Power Divider with 180º Phase Shift

The two Wilkinson dividers share an identical configuration of transmission lines, same isolation resistor ($2Z_0$=100Ω, SMD0603 from VISHAY [60]) and the identical design structure. By varying the length difference between two output transmission lines, the proposed geometries could produce 90º and 180º phase shift, respectively.

Figure 3.37 illustrates all of the simulated S-Parameters in magnitude for the 90º phase shift Wilkinson power divider. At 2.45GHz, it provides low reflection coefficient (-27.05dB), suitable forward gains (3.45dB and 4.21dB) and high isolation (-24.65dB). S_{31}(-4.21dB) is

greater than S_{21}(-3.45dB), due to the additional λ/4 transmission line, which not only produces the 90º phase difference, but also increases the power loss at Port3. Figure 3.38 demonstrates the simulated phase of the S-Parameters. At 2.45GHz, S_{21} is 132.81º and S_{31} is 43.29º. A phase difference of 89.52º has been successfully generated. Figure 3.39 and Figure 3.40 depict correct S-Parameters and 179.4º (16.29º + 163.11º) phase difference for the second Wilkinson power divider architecture. It is clear from the simulation results that the two Wilkinson dividers are adequate for both of the required phase shifts. Furthermore, dimensions of the circuits have been miniaturised in order to be implemented for compact portable devices (26mm×29mm and 32mm×52mm, respectively).

3.5.3 Design of the Reconfigurable Feeding Network

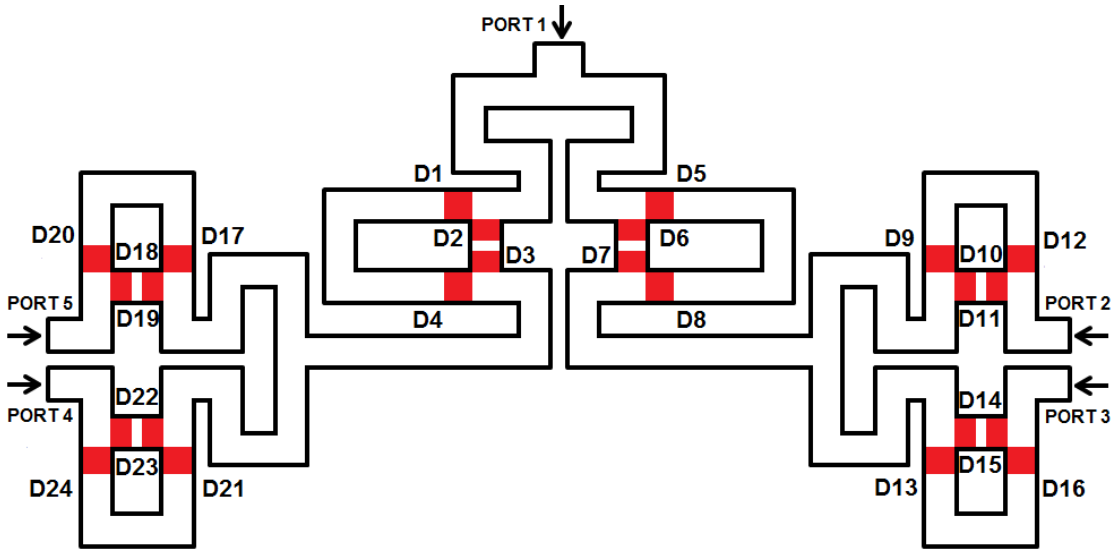


Figure 3.41: Schematic of the Reconfigurable Feeding Network

Based on the above design procedure, three individual Wilkinson power dividers in Section 3.5.2 and 24 PIN diodes are combined in order to produce the reconfigurable feeding network for dual circular polarisations. The schematic and geometry of the feeding network are illustrated in Figure 3.41. Furthermore simulations of transmission lines, PIN diodes locations and signal port dimensions have been made in order to optimise the S-Parameters. Figure 3.42 shows the final structure.

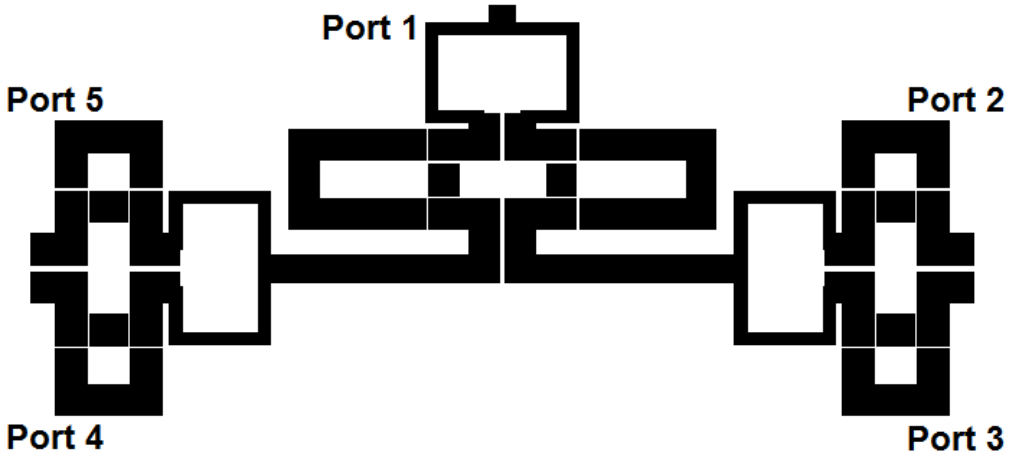


Figure 3.42: Configuration of the Proposed Feeding Network

PIN diodes are widely used in microwave circuits because they have attractive properties, such as low power handling, low insertion loss, good isolation and low fabrication cost [78] [93]. There are 24 PIN diodes integrated into the feeding network to construct the reconfigurable circular polarisation. By controlling the bias voltages on the PIN diodes (represented by small red blocks in Figure 3.41), the feeding network may convert between two states and hence switch its circular polarisation (as presented in Figure 3.43 and Figure 3.44).

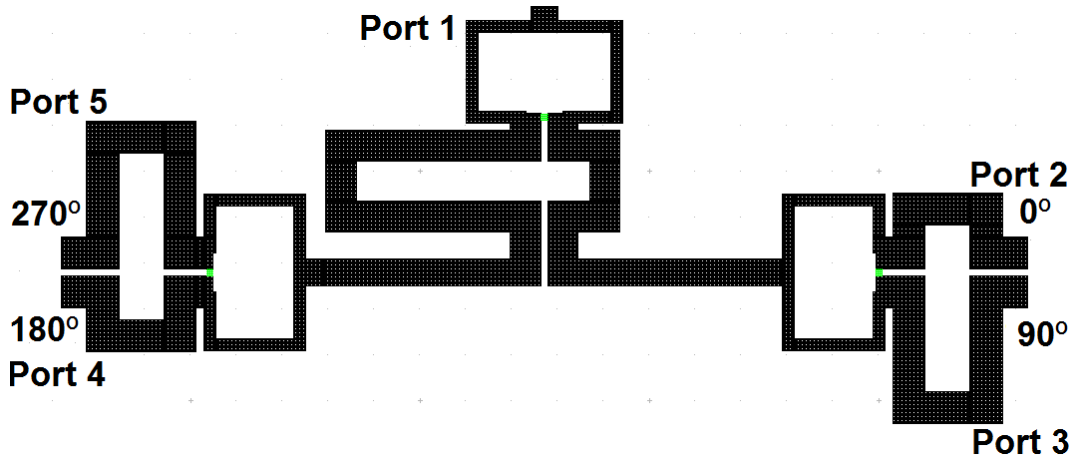


Figure 3.43: Circuit Configuration for Left-Hand Circular Polarisation (LHCP)

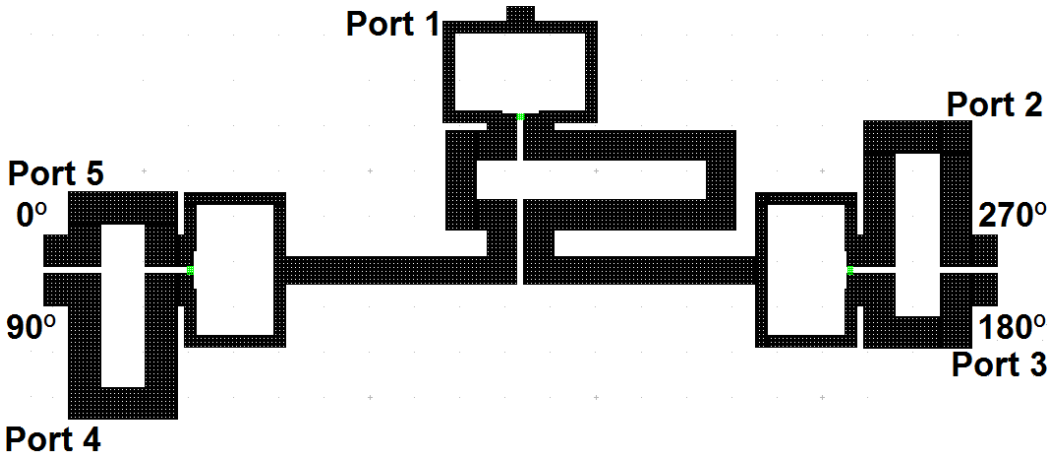


Figure 3.44: Circuit Configuration for Right-Hand Circular Polarisation (RHCP)

When the PIN diodes D_1, D_4, D_6, D_7 D_{10}, D_{11}, D_{13}, D_{16} D_{17}, D_{20}, D_{22} and D_{23} are in the ON-state (forward bias) and others are in the OFF-state (reverse bias), the proposed configuration transfers to the circuit diagram illustrated in Figure 3.43. There is a λ/4 length increment from Port 2 to Port 5, which creates 90º, 180º and 270º phase shift between Port 2, Port 3, Port 4 and Port 5. When this feeding network is connected to a four elements antenna array, the antenna elements will be fed in quadrature. The 90º phase delay is in clockwise direction and a left-hand circular polarisation (LHCP) will be excited. Similarly, when diodes D_2, D_3, D_5, D_8 D_9, D_{12}, D_{14}, D_{15} D_{18}, D_{19}, D_{21} and D_{24} are supplied with forward bias voltages, the structure reduces to the circuit as plotted in Figure 3.44. From Port 2 to Port 5, there is a λ/4 length decrement. The 90º phase delay is in the opposite direction compared with the geometry in Figure 3.43 (counter-clockwise), which converts the antenna array with a right-hand circular polarisation (RHCP). These bias voltages are configured by an ARM microprocessor (LPC1768) and the control circuit has been implemented and fabricated. Detailed hardware implementation will be discussed in Chapter 5.

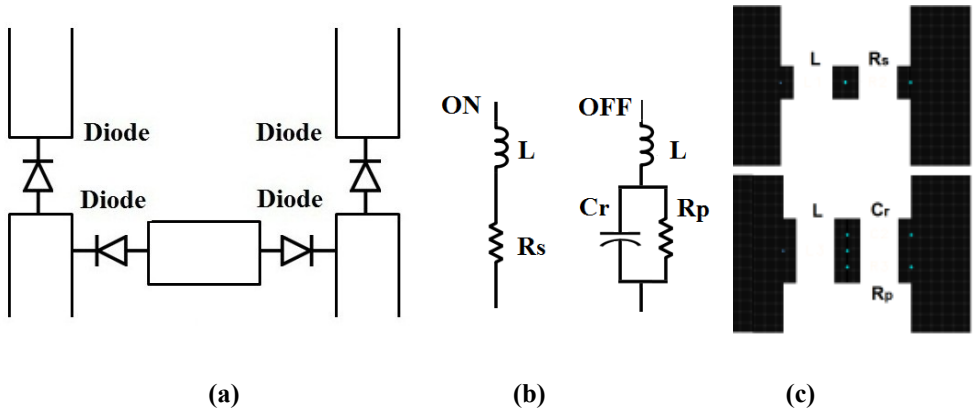


Figure 3.45: (a) PIN diodes Arrangement (b) Equivalent RLC Circuit of PIN Diode (c) PIN Diode Simulation Model in Agilent ADS

In Agilent ADS simulation environment, the packaged PIN diodes are modelled based on its equivalent RLC circuit (in Figure 3.45). Diodes of HSMP-389D (AVAGO) [94] with a dimension of 1.2mm× 2mm are applied as switches, which guarantee low insertion loss (0.36dB) and high isolation (25dB). The resistance, inductance and capacitance values for the equivalent RLC circuit model are according to the PIN diode datasheet. At the ON-state, the PIN diode is represented by a resistor (R_s=4.5Ω) and an inductor (L=2nH), while for the OFF-state, the diode can be replaced by a capacitor (C_r=0.2pF) and an inductor (L=2nH). R_p is the net dissipative resistance in the reverse bias and is neglectable for this RF circuit. The simulated S-Parameters are summarised in Table 3.4. Figure 3.46 and Figure 3.47 depict the simulated S-Parameters in phase format for the proposed reconfigurable feeding network.

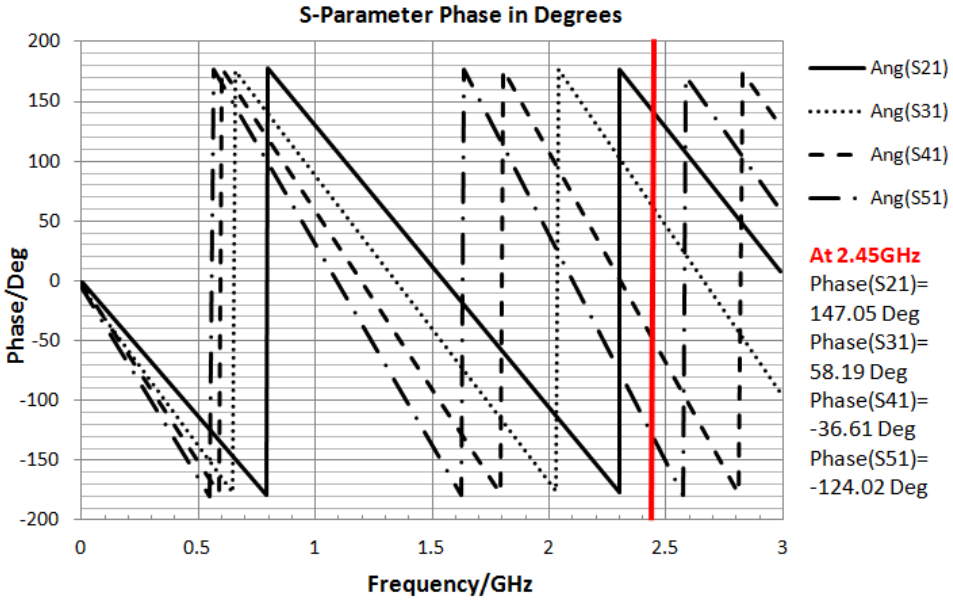


Figure 3.46: Simulated S-Parameter (Phase) of LHCP

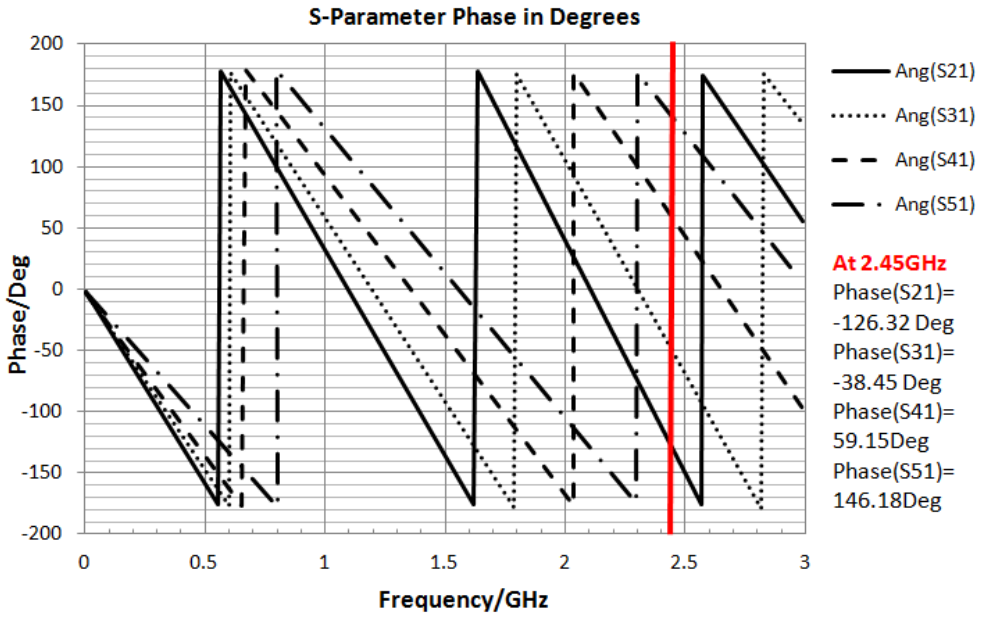


Figure 3.47: Simulated S-Parameter (Phase) of RHCP

3.5.4 Circuit Fabrication and Characterisation

The reconfigurable feeding network has been fabricated (as shown in Figure 3.48) and subsequently characterised with an HP8753C vector network analyser (VNA). The dimension of the realised implementation is 45mm×105mm.

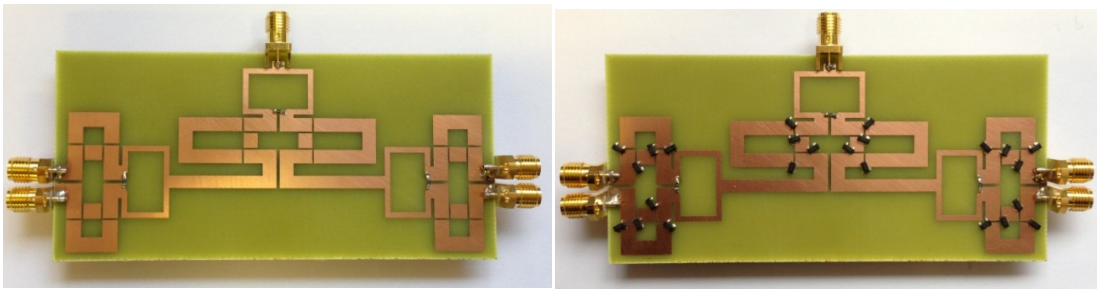


Figure 3.48: Photo of the Fabricated Structure (with and without PIN Diodes)

Table 3.4 compares the simulated and measured S-Parameters of the proposed reconfigurable feeding network.

Table 3.4: Simulated and Measured S-Parameters

	Simulation (LHCP)	Measurement (LHCP)	Simulation (RHCP)	Measurement (RHCP)
S_{11}(Magnitude)	-18.22dB	-20.56dB	-19.24dB	-21.15dB
S_{22}(Magnitude)	-11.47dB	-12.21dB	-22.98dB	-19.12dB
S_{33}(Magnitude)	-15.52dB	-13.87dB	-12.63dB	-15.31dB
S_{44}(Magnitude)	-12.81dB	-16.65dB	-15.54dB	-10.33dB
S_{55}(Magnitude)	-23.16dB	-20.13dB	-10.91dB	-9.31dB

S_{21}(Magnitude)	-7.48dB	-8.26dB	-8.38dB	-8.58dB
S_{31}(Magnitude)	-8.14dB	-8.57dB	-7.82dB	-8.12dB
S_{41}(Magnitude)	-7.81dB	-8.32dB	-8.16dB	-8.32dB
S_{51}(Magnitude)	-8.39dB	-8.62dB	-7.47dB	-8.34dB
S_{23}(Magnitude)	-14.61dB	-12.31dB	-17.28dB	-20.33dB
S_{34}(Magnitude)	-24.66dB	-26.11dB	-24.73dB	-19.56dB
S_{45}(Magnitude)	-17.51dB	-12.31dB	-14.54dB	-12.45dB
S_{21}(Phase)	147.05º	131.16º	-126.32º	-140.23º
S_{31}(Phase)	58.19º	43.28º	-38.45º	-58.98º
S_{41}(Phase)	-36.61º	-59.15º	59.15º	41.03º
S_{51}(Phase)	-124.02º	-133.13º	146.18º	122.75º

Finally, Figure 3.49 and Figure 3.50 demonstrate the simulated and measured phase difference for LHCP and RHCP, respectively.

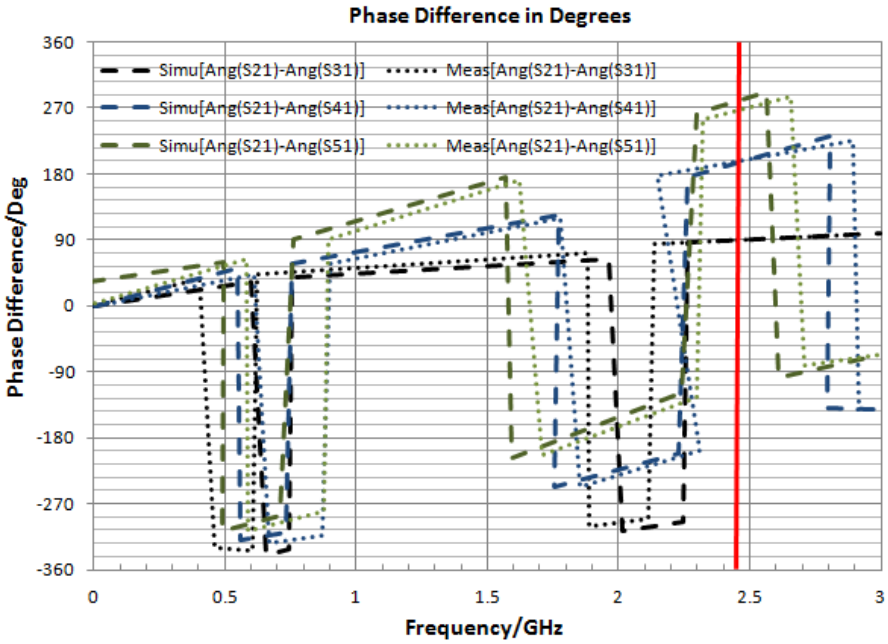


Figure 3.49: Simulated and Measured Phase Difference for LHCP

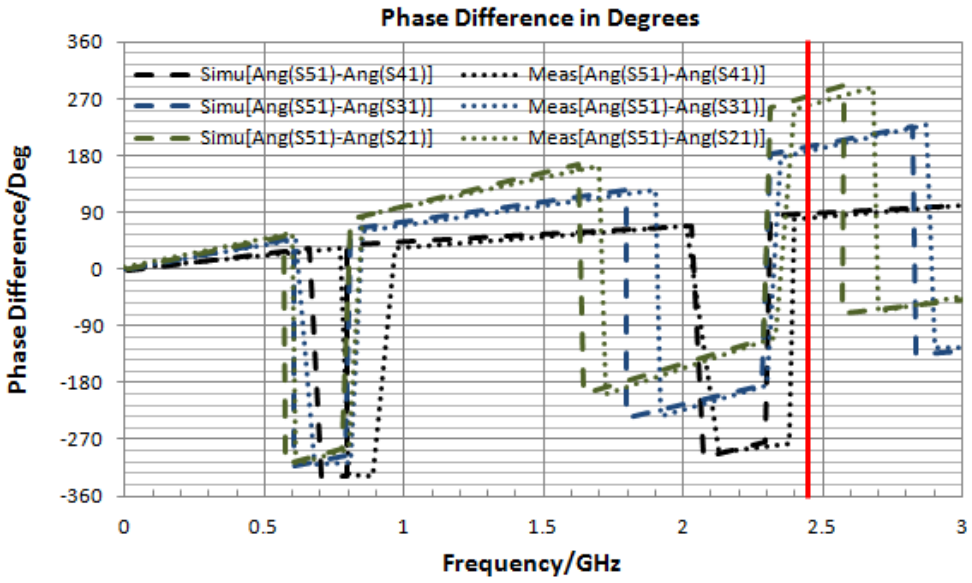


Figure 3.50: Simulated and Measured Phase Difference for RHCP

Table 3.4 and Figure 3.49 to Figure 3.50 reveal a good consistency between the simulation and measurement. At 2.45 GHz, all of the S-Parameters meet the requirements. Phase differences of 88º, 190º, 264º and 262º, 181º, 81º have been obtained for LHCP and RHCP, respectively. There is a slight difference of the insertion loss, which is due to the high loss of the lump components, PIN diodes in this circuit. Further work will apply MEMS devices integrated into the configuration to replace the PIN diodes. The proposed geometry could be applied to a four elements antenna array with dual circular polarisations.

3.6 Reconfigurable Feeding Network for GSM/GPS/3G/WiFi and Global LTE Applications

3.6.1 Introduction

With the rapid development in wireless communication systems, there are many growing demands for mobile design requirements, which include lightweight, compact size, multiband and multiple functionalities. Reconfigurable mobile terminals become the trend in order to satisfy these targets and various reconfigurable antennas have been investigated and demonstrated in practice. Reconfigurable antennas commonly adapt their properties to obtain selectivity in operating frequency, bandwidth and radiation polarizations [78-80]. However, these communication systems such as phased array antennas and smart antennas cannot be fully accomplished without the aid of advanced feeding networks [95-97].

The Wilkinson power divider is one of the indispensable components in various radio frequency circuits and it has been widely utilised for power division and combination in

antenna feeding networks [89, 91, 97]. The conventional Wilkinson divider applies two λ/4 transmission lines and only operates at a certain frequency [37]. A literature review demonstrates that both multiband and wideband Wilkinson dividers could be successfully developed [51, 55]. Nevertheless, these configurations have relatively limited abilities in miniaturising circuit dimensions and can only achieve a maximum of three operating frequency bands.

This section discusses a novel miniaturised switchable and reconfigurable feeding network covering GSM, GPS, 3G, WiFi and global LET standards. The feeding network is composed of four conventional Wilkinson power dividers which could be individually reconfigured in length using PIN diodes switches. By controlling the bias voltages on these PIN diodes, the operating frequency of the proposed geometry can be converted between four different bands: 600MHz-900MHz, 1.2GHz-1.6GHz, 1.8GHz-2.2GHz and 2.4GHz-2.6GHz. The first frequency band (600MHz-900MHz) is used to cover LTE US (700MHz), LTE UK (800MHz) and GSM (850MHz, 900MHz). The second band (1.2GHz-1.6GHz) targets GPS L1 (1.575GHz) and GPS L2 (1.227GHz). Different GSM (1800MHz, 1900MHz) and 3G standards (UMTS, W-CDMA, TD-SCDMA and CDMA2000) are located in the third frequency band (1.8GHz-2.2GHz). The last band (2.4GHz-2.6GHz) is applied to satisfy the applications of WiFi (2.45GHz) and LTE Europe (2.6GHz). The miniaturised and optimised feeding network exhibits good performance of S-Parameters in each band, which includes high return loss (10dB), suitable insertion loss (3.2dB), equal power splitting, and high isolation (-10dB). Full-wave simulations were carried out using CST Microwave Studio. Within the simulation environment, three types of PIN diode models were constructed and investigated in order to improve accuracy. The feeding network is implemented on an FR4 substrate. Fabrication and measurement results closely correlate with those achieved during design simulations. The reconfigurable feeding network could be particularly applied to commercial multiband communication systems [48].

3.6.2 Initial Wilkinson Power Divider Structure

Based on the design procedure discussed in Section 3.2.6, four Wilkinson power dividers (as shown in Figure 3.51 to Figure 3.54) have been designed, simulated and optimised using an electromagnetic simulator, namely CST Microwave Studio (CST), for full-wave analysis. In this implementation, copper transmission lines with a conductivity of 5.89×10^7 were etched on a FR4 printed circuit board (with a thickness h=1.6mm and relative dielectric constant, εr=4.55) [98].

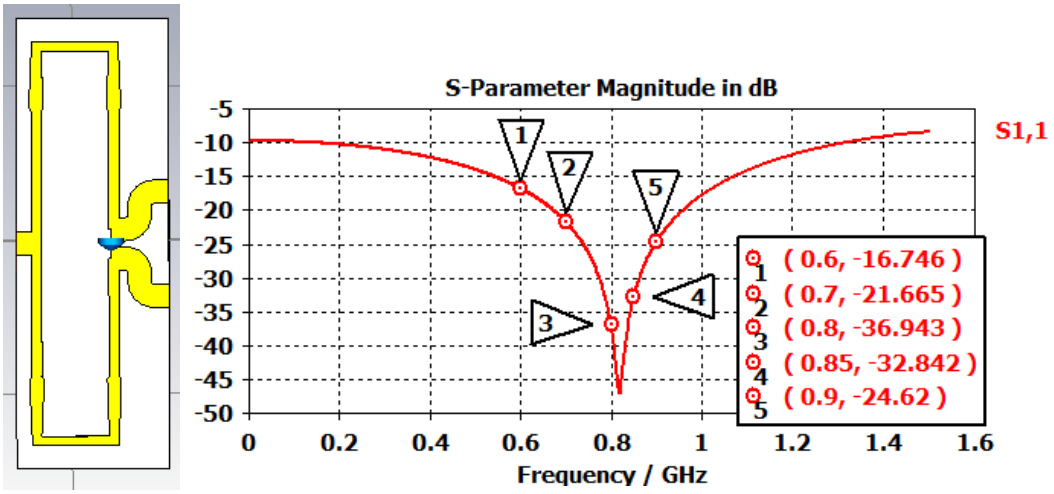


Figure 3.51: Wilkinson Divider with Frequency Band 600MHz-900MHz

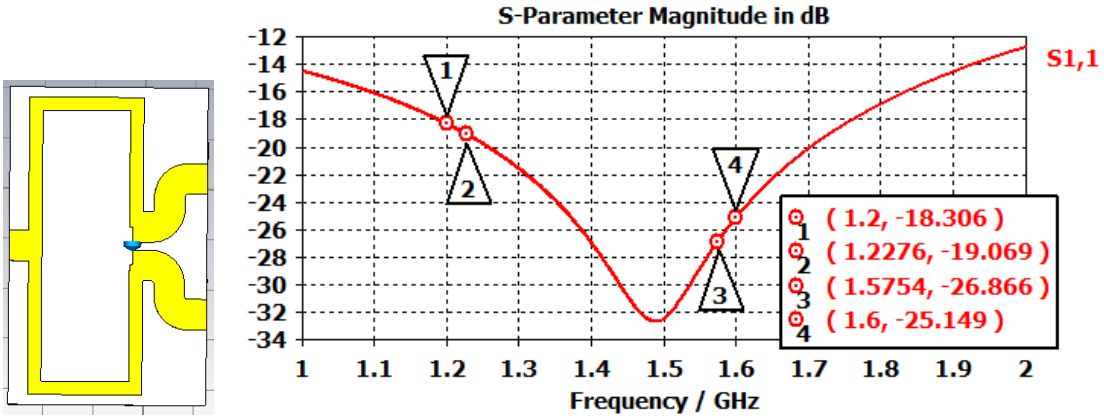


Figure 3.52: Wilkinson Divider with Frequency Band 1.2GHz-1.6GHz

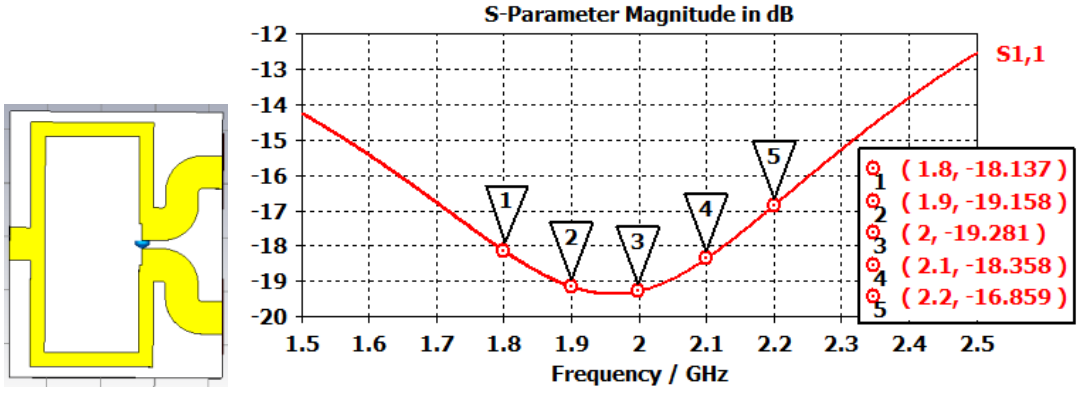


Figure 3.53: Wilkinson Divider with Frequency Band 1.8GHz-2.2GHz

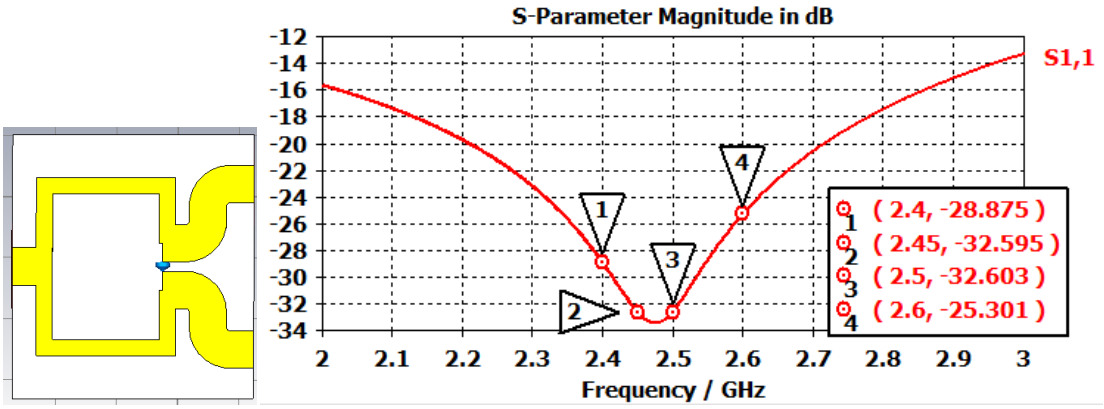


Figure 3.54: Wilkinson Divider with Frequency Band 2.4GHz-2.6GHz

These initial Wilkinson power dividers share an identical configuration of transmission lines, same characteristic impedance ($2Z_0$=100Ω, SMD0603 from VISHAY [60]) and the similar design structure. By only varying the quarter-wavelength, different operating frequency bands are achieved.

Figure 3.51 to Figure 3.54 demonstrate the simulated reflection coefficients (S_{11}) of the four initial Wilkinson power dividers for different operating frequency bands. The first architecture (in Figure 3.51) illustrates 600MHz to 900MHz bandwidth, which is applied for LTE US (700MHz), LTE UK (800MHz) and GSM (850MHz, 900MHz). The resonant frequency in Figure 3.52 is adjusted to operate from 1.2GHz to1.6GHz, targeting at GPS L1 (1.575GHz) and GPS L2 (1.227GHz). 3G applications (UMTS, W-CDMA, TD-SCDMA and CDMA2000) are covered by the configuration in Figure 3.53 and the last circuit (in Figure 3.54) is used for WiFi (2.45GHz) and LTE Europe (2.6GHz) standards. It is clear from the simulation results that the reflection coefficients (S_{11}) are adequate for each required frequency range. Furthermore, dimensions of these circuits have been miniaturised targeting compact portable devices (52.5mm × 19.6mm, 29.6mm × 19.6mm, 22.7mm × 19.6mm and 16.5mm×19.6mm, respectively).

3.6.3 Design of the Reconfigurable Feeding Network

Based on the above design procedure, four initial Wilkinson power dividers in Section 3.6.2 and 24 PIN diodes are combined in order to construct the reconfigurable feeding network. Its schematic and geometry are shown in Figure 3.55 and Figure 3.56. In radio frequency circuit, length of transmission lines, dimensions of microstrip ports and the locations of PIN diodes strongly influence the S-Parameters and operating frequencies. Furthermore simulations were carried out to optimise the circuit parameters and develop the feeding network. Figure 3.57 illustrates the final layout.

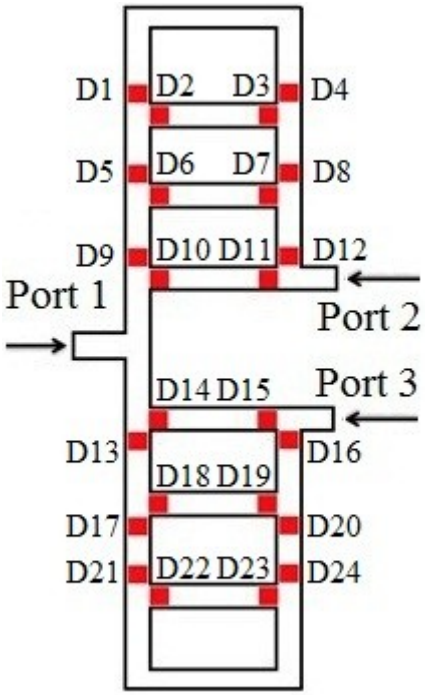


Figure 3.55: Schematic of the Reconfigurable Feeding Network

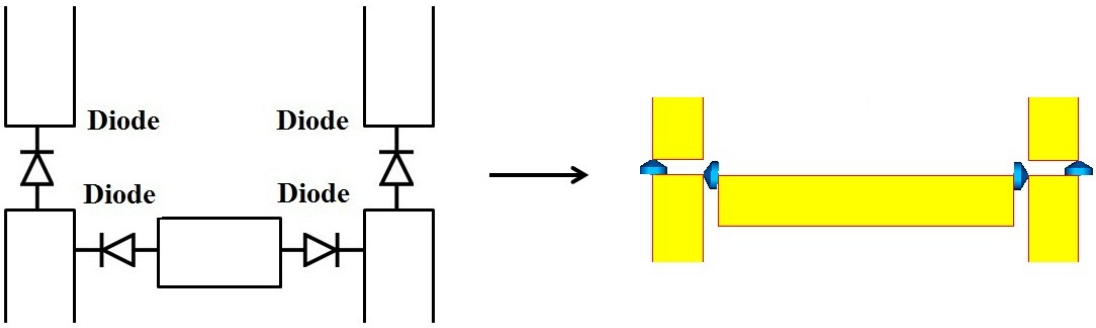


Figure 3.56: PIN Diodes Arrangement

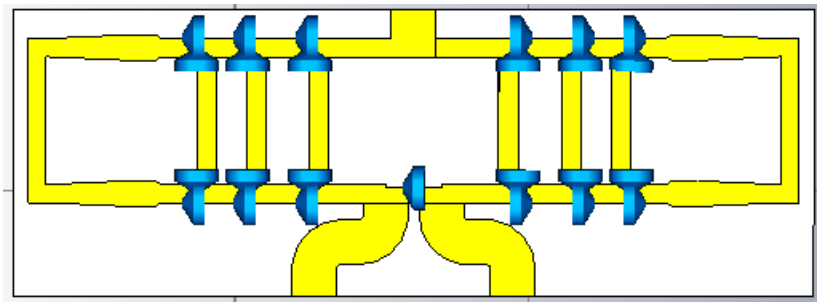


Figure 3.57: Configuration of the Proposed Design in CST Microwave Studio

By controlling the bias voltages on the PIN diodes (represented by small red blocks in Figure 3.55), the feeding network may convert between four states and hence switch its operating frequencies. When diodes D_{10}, D_{11}, D_{14}, D_{15} are in the ON-state (forward bias) and

others are in the OFF-state (reverse bias), the proposed structure reduces to the circuit presented in Figure 3.54, which targets at 2.4GHz-2.6GHz. Similarly, when diodes D_6, D_7, D_9, D_{12}, D_{13}, D_{16}, D_{18} and D_{19} are on, the operating frequency is from 1.8GHz to 2.2GHz as the design converts to the circuit illustrated in Figure 3.53. For the case when only diodes D_2, D_3, D_5, D_8, D_9, D_{12}, D_{13}, D_{16}, D_{17}, D_{20}, D_{22} and D_{23} are in the ON-state, the feeding network covers 1.2GHz-1.6GHz as the design changes to the circuit plotted in Figure 3.52. Finally, when diodes D_1, D_4, D_5, D_8, D_9, D_{12}, D_{13}, D_{16}, D_{17}, D_{20}, D_{21} and D_{24} are supplied with forward bias voltages, the design applies for 600MHz-900MHz as it reduces to the circuit demonstrated in Figure 3.51. These bias voltages are configured by an ARM microprocessor (LPC1768) and the control circuit will be discussed in Chapter 5.

The PIN diode (as depicted in Figure 3.58) is composed of an intrinsic semiconductor layer sandwiched between heavily doped P and N type regions. In reality, the intrinsic layer also becomes very weakly doped P-type or N-type silicon. The PIN diodes are widely utilised as switches when operated between forward and reverse DC bias states for tuning the microwave signals. When a forward DC bias is applied to the PIN diode, free charges from P and N regions flood the I-region, which converts the diode into a conducting medium. The diode behaves virtually like a short circuit, and allows easy flow of any RF signals superimposed on it. To the contrary, when a reverse DC bias is applied, the I-region is completely depleted of charge carriers, making the diode behave essentially like an open circuit.

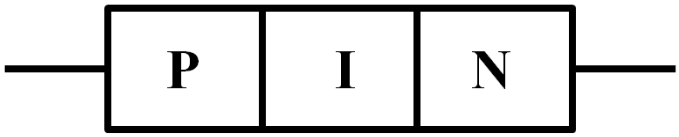


Figure 3.58: Schematic of a PIN Diode

There are generally three methods to construct the simulation model of PIN diode in microwave systems. Firstly, presenting and absenting air gap and perfect electrical conductor (PEC) strip is used to characterise the PIN diode [80, 99]. The second approach is to represent the diode by a microstrip or a metal strip [93, 100]. The third and most popular way is to utilise the equivalent RLC circuit of a packaged PIN diode [101]. This section applies all of the above methodologies to investigate the influence of the PIN diode on the feeding networks.

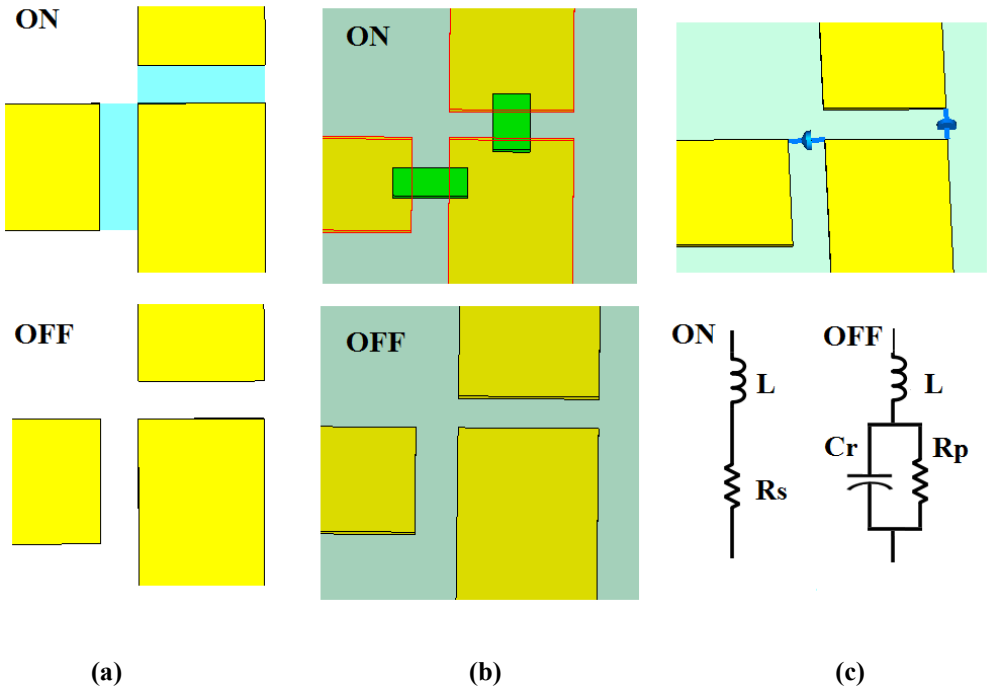


Figure 3.59: (a) PEC PIN Diode Model (b) Metal Strip PIN Diode Model (c) Equivalent RLC Circuit of PIN Diode

Figure 3.59 demonstrates the configurations of PIN diodes models in CST Microwave Studio. In Figure 3.59(a), a PEC pad is utilised to represent an open (or short) of the transmission lines. Figure 3.59(b) illustrates the connection or disconnection of PIN diodes simulated in the absence or presence of a metal pad with the area of 0.4mm×0.6mm. Several previous experiments have shown the validity of this simplification for RF device designs. Moreover, the equivalent RLC circuit of the PIN diode is sketched in Figure 3.59(c). Diodes of HSMP-389D (AVAGO) with a dimension of 1.2mm× 2mm are used as switches, which guarantee a high isolation of -25dB and low insertion loss (0.36dB). The equivalent RLC circuit models that include the parasitic packaging effects could be extracted from the PIN diode datasheet [94]. For the ON-state, the diode is represented by an inductor (L=2nH) and a resistor (Rs=4.5Ω), while in the OFF-state, the diode is replaced by an inductor (L=2nH) and a capacitor (C_r=0.2pF). R_p is the net dissipative resistance in the reverse bias and is not important for this application [101]. The simulated reflection coefficients (S_{11}) simulation results are presented Figure 3.61 to Figure 3.64.

3.6.4 Circuit Fabrication and Measurements

The proposed reconfigurable feeding network has been fabricated (as shown in Figure 3.60) and subsequently characterised with an HP8753C vector network analyser (VNA). Short-

Open-Load-Through (SLOT) calibration was done in order to improve measurement accuracy. The size of the realised implementation is 50mm× 19mm.

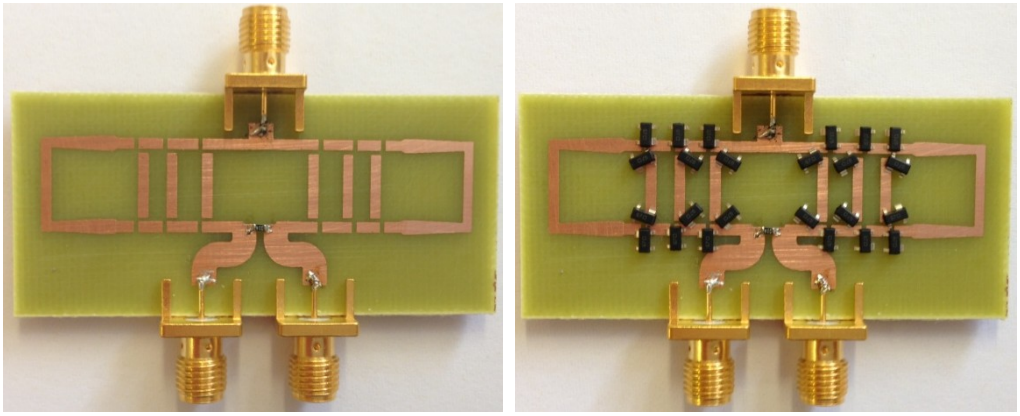


Figure 3.60: Photo of the Fabricated Configuration (With and Without PIN Diodes)

The presented reconfigurable feeding network is a three port microwave device and the VNA is a two port system. The third port of the circuit was terminated with a standard 50Ω terminator. Figure 3.61 to Figure 3.64 summarise the simulated and measured reflection coefficients (S_{11}). Table 3.5 compares the simulated and measured forward gain (S_{21}).

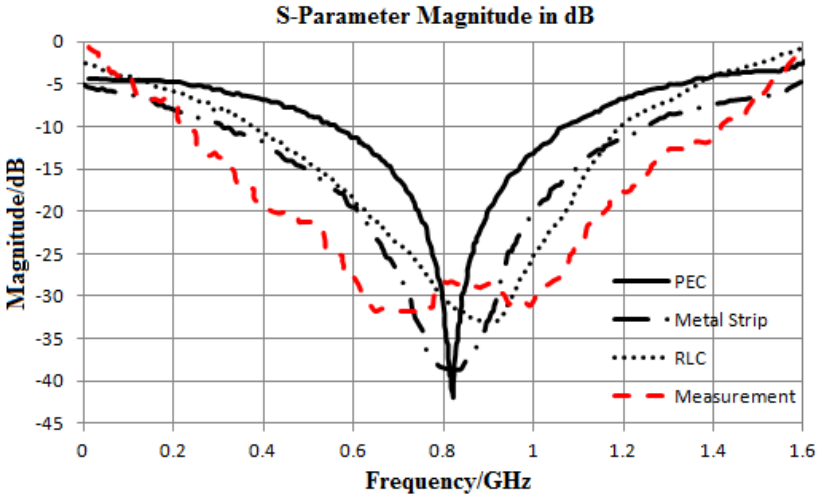


Figure 3.61: Simulated and Measured Reflection Coefficients (S_{11}) for 600MHz-900MHz

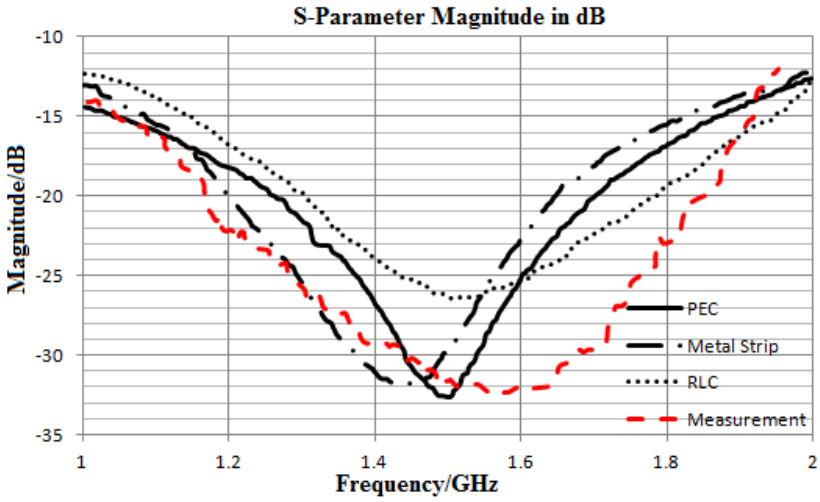


Figure 3.62: Simulated and Measured Reflection Coefficients (S_{11}) for 1.2GHz-1.6GHz

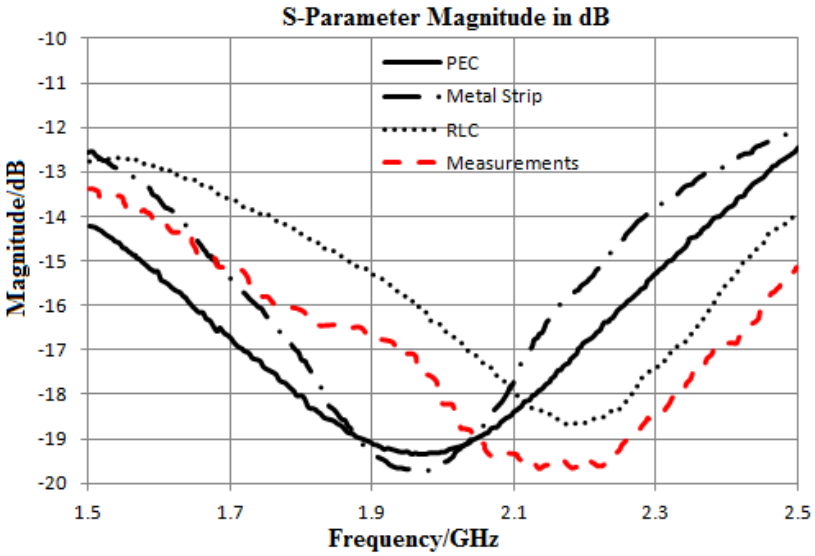


Figure 3.63: Simulated and Measured Reflection Coefficients (S_{11}) for 1.8GHz-2.2GHz

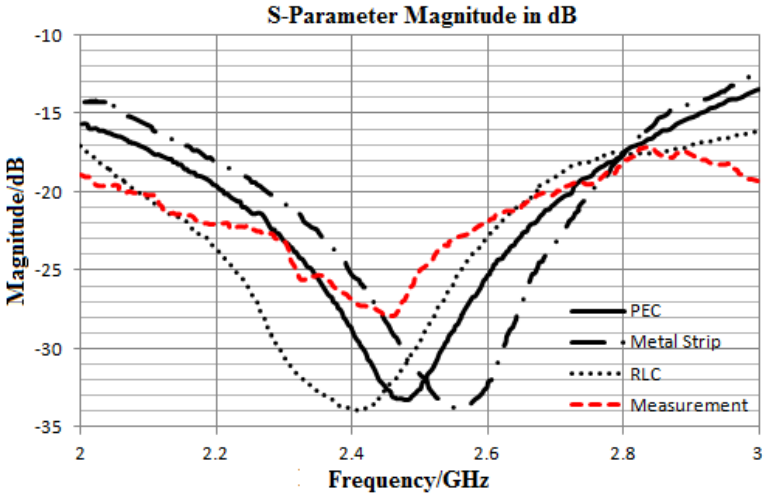


Figure 3.64: Simulated and Measured Reflection Coefficients (S_{11}) for 2.4GHz-2.6GHz

Table 3.5: Simulated and Measured Forward Gain (S_{21})

Frequency	PEC	Metal	RLC	Measurement
700 MHz	-3.22dB	-3.37dB	-3.81dB	-3.95dB
800 MHz	-3.12dB	-3.41dB	-3.85dB	-4.15dB
850 MHz	-3.25dB	-3.35dB	-3.91dB	-4.21dB
900 MHz	-3.15dB	-3.34dB	-3.79dB	-4.16dB
1.227 GHz	-3.21dB	-3.41dB	-3.96dB	-3.98dB
1.575 GHz	-3.19dB	-3.39dB	-4.02dB	-4.05dB
1.8 GHz	-3.15dB	-3.43dB	-3.89dB	-4.25dB
1.9 GHz	-3.22dB	-3.45dB	-3.98dB	-4.21dB
2.0 GHz	-3.21dB	-3.47dB	-4.05dB	-4.11dB
2.1 GHz	-3.19dB	-3.53dB	-3.89dB	-4.15dB
2.45GHz	-3.2dB	-3.45dB	-3.78dB	-4.11dB
2.6 GHz	-3.17dB	-3.34dB	-3.97dB	-4.15dB

Figure 3.61 to Figure 3.64 and Table 3.5 reveal a good consistency between the simulated and measured results. At the desired frequencies, all of the S_{11} (reflection coefficients) are lower than -15dB (most under -20dB). There is a slight difference for insertion loss. It is due to the high loss of the lump components, PIN diodes in this circuit. Further research will focus on using MEMS devices integrated into the configuration to replace these diodes.

3.7 UWB Feeding Network for Smart Antenna Arrays

3.7.1 Introduction

The Wilkinson power divider is one of the indispensable components in various microwave communication systems and it has been widely used for power division and combination for antenna feeding networks [37, 102, 103]. A literature review illustrates that both wideband and multiband Wilkinson dividers could be successfully developed [55, 104, 105]. Whereas, these structures have relatively limited abilities in miniaturising circuit dimensions and perform inefficiently in low frequency bands. In this section, an improved and miniaturised UWB Wilkinson power divider is developed in order to provide the UWB feeding network.

3.7.2 Single UWB Wilkinson Power Divider Structure

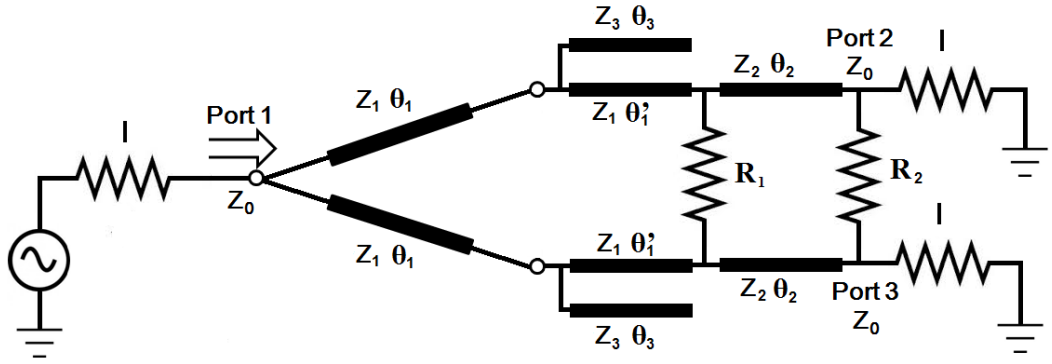


Figure 3.65: Structure of the UWB Wilkinson Power Divider

Structure of the UWB Wilkinson power divider is presented in Figure 3.65. The characteristic impedance Z_0 of Port 1, Port 2 and Port 3 are 50Ω, for standard applications. The fundamental geometry of the proposed design is a two-section Wilkinson power divider, with high frequency response. From Young's transformer tables [106], Z_1 and Z_2 could be calculated according to the terminating bandwidth ratio f_2/f_1. The input admittance and reflection coefficient are determined by means of elementary transmission line theory [107].

$$Y_{in,o} = 2G_2 + Y_2 \frac{Y_2+(2G_1+Y_1 s)s}{2G_1+(Y_1+Y_2)s} \tag{3.48}$$

$$\rho_o = \frac{1-Y_{in,o}}{1+Y_{in,o}} \tag{3.49}$$

Where $s=-j\cot\theta_1$. In order to achieve $\rho_o = 0$ at φ_1 and φ_2, Equation (3.48) and (3.49) yield that

$$\varphi_1 = 90° \left[1 - \frac{1}{\sqrt{2}}\left(\frac{f_2/f_1-1}{f_1/f_2+1}\right)\right] \tag{3.50}$$

$$R_1 = \frac{2Z_1Z_2}{\sqrt{(Z_1+Z_2)(Z_1-Z_2\cot^2\varphi_1)}} \tag{3.51}$$

$$R_2 = \frac{2R_1(Z_1+Z_2)}{R_1(Z_1+Z_2)-2Z_1} \tag{3.52}$$

Compared with the conventional Wilkinson power divider, the λ/4 transmission lines have been separated into two sections, with same impedance Z_1 but different electrical length θ_1 and θ_1'. Moreover, two open stubs are connected to the both branches, with impedance Z_3 and length θ_3 for impedance matching. By adjusting the length and width of the stubs, a reflection zero could be introduced into the lower and higher frequencies, so the bandwidth is even wider. The electrical length θ_1' compensates the impedance mismatch caused by the stubs

between the original λ/4 transmission lines, and also guarantees all of the input and output ports are matched to 50Ω.

Since the dielectric substrate thickness is very thin compared with the wavelength (h<<λ), a quasi-TEM mode has been utilised for the circuit design. The characteristic impedance Z_0 (50Ω) could be rewritten here in Equation (3.53) and (3.54).

$$Z_0 = \frac{60}{\sqrt{\varepsilon_e}} \ln\left(\frac{8h}{w_m} + \frac{w_m}{4h}\right) \tag{3.53}$$

$$Z_0 = \frac{120\pi}{\sqrt{\varepsilon_e}\left[{}^{w_m}/_{h} + 1.393 + 0.667 \ln\left({}^{w_m}/_{h} + 1.444\right)\right]} \tag{3.54}$$

Where, w_m stands for the width of the transmission line and h represents the thickness of the substrate. ε_e shows the effective dielectric constant which is given by:

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2 \times \sqrt{1 + 12h/w_m}} \tag{3.55}$$

Where, ε_r illustrates the dielectric constant of the substrate. In order to cover WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) applications, the centre frequency for the fundamental two-section Wilkinson power divider was set at 4.5GHz with the bandwidth ratio of 2, so the terminating frequencies are 3GHz and 6GHz, respectively.

By optimising dimensions of the open stubs, the two-section Wilkinson power divider is able to cover wider frequency ranges. In this implementation, copper transmissions with a conductivity of 5.89×10^7 was etched on an FR4 printed circuit board (with a thickness h=1.6mm and relative dielectric constant, ε_r=4.55). All of the transmission line dimensions have been calculated using the formulas (3.48-3.55). Finally, the UWB divider configuration has been optimised in order to achieve the following scattering matrix:

$$[S] = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} \Longrightarrow [S] = \frac{-1}{\sqrt{2}} \begin{bmatrix} 0 & j & j \\ j & 0 & 0 \\ j & 0 & 0 \end{bmatrix} \tag{3.56}$$

$$S_{11} = S_{22} = S_{33} = 0 \tag{3.57}$$

$$S_{23} = S_{32} = 0 \tag{3.58}$$

$$S_{12} = S_{21} = S_{13} = S_{31} = (V_1^e + V_1^0)/(V_2^e + V_2^0) = -j/\sqrt{2} \tag{3.59}$$

The UWB Wilkinson power divider (in Figure 3.67) has been designed, calculated, simulated and optimised using Advanced Design System (ADS) and CST Microwave Studio (CST), for full-wave analysis.

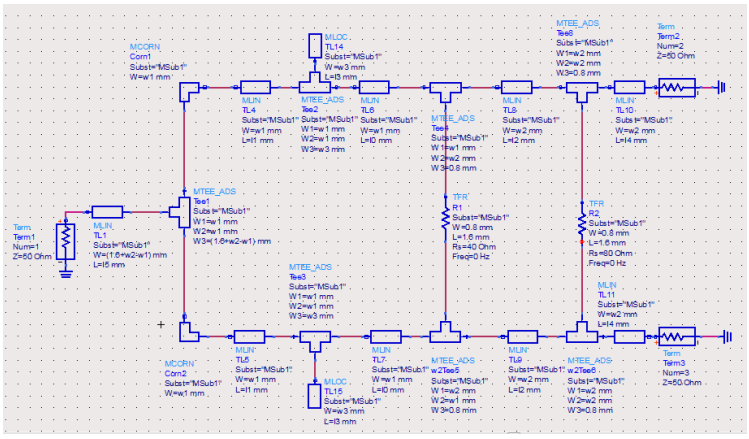


Figure 3.66: Schematic of the UWB Wilkinson Power Divider

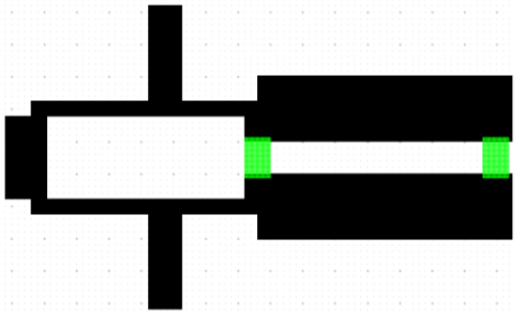


Figure 3.67: Configuration of the UWB Wilkinson Power Divider

Figure 3.68 illustrates the simulated S-Parameters of the proposed UWB Wilkinson power divider. It reveals that from 0 to 9GHz, the presented configuration demonstrates high return loss (greater than 10dB), suitable insertion loss (3.2dB=50%) and high isolation (larger than 10dB). There are two makers showing the S-Parameters for 2.45GHz and 2.6GHz respectively, which are the operating frequencies of the smart antenna developed in Chapter 2.

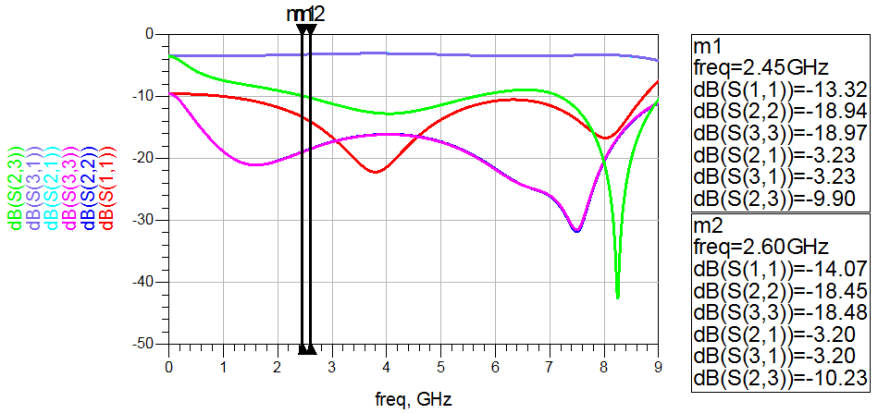


Figure 3.68: Simulated S-Parameters (Magnitude) of the UWB Wilkinson Power Divider

The proposed UWB Wilkinson power divider has been fabricated (as illustrated in Figure 3.69) and subsequently characterised with an HP8753C vector network analyser (VNA). Short-Open-Load-Through (SLOT) calibration was done in order to improve measurement accuracy. Figure 3.70 presents all of the measured S-Parameters.

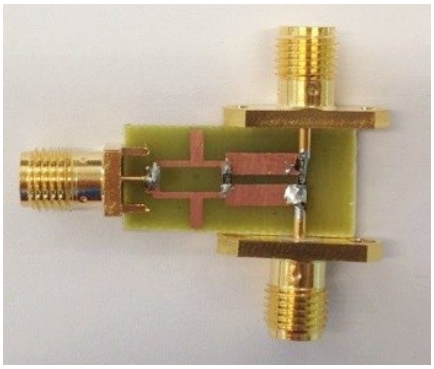


Figure 3.69: Photo of the Fabricated UWB Wilkinson Power Divider

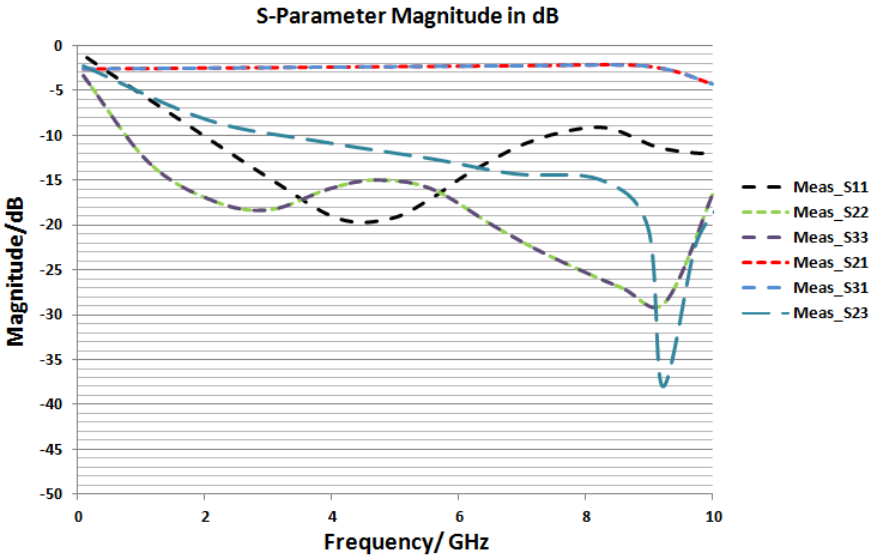


Figure 3.70: Measured S-Parameters (Magnitude) of the Fabricated UWB Wilkinson Power Divider

It is evident from the simulation and measurement results that the improved UWB Wilkinson power divider almost covers from 0.5GHz to 10GHz, which is adequate for both of WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz). The reflection coefficient S_{11} exhibits a matched behaviour because the reflected waves caused by the mismatched elements are cancelled by the open stubs and the isolation resistance (R_1=40Ω and R_2=80Ω) between the output ports. The divider also obtains suitable insertion loss and high isolation. Furthermore, dimension of the circuit has been miniaturised in order to be implemented for compact

portable devices (9.5mm × 15mm). Finally, this UWB Wilkinson power divider will be modified and applied into the smart antenna array systems presented in this thesis.

3.7.3 Modified UWB Wilkinson Power Divider Configuration

For the UWB Wilkinson power divider, separation between the two output ports is 3mm. It is difficult to connect antenna elements to the divider due to the limited spacing. This section describes several modified UWB Wilkinson power dividers with various output separations.

Figure 3.71 presents the schematic of the modified UWB Wilkinson power divider. Compared to the configuration in Figure 3.66, two additional transmission lines are added before the output ports. By varying the length of the two transmission lines, difference output separations could be achieved.

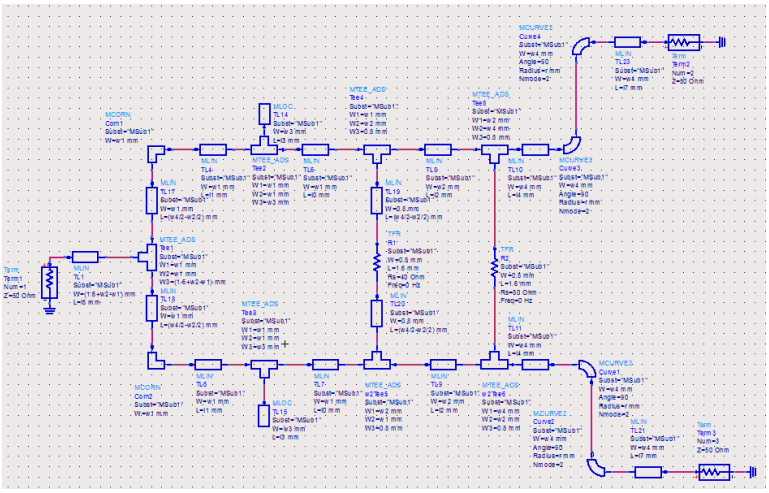


Figure 3.71: Schematic of the Modified UWB Wilkinson Power Divider

Five modified UWB Wilkinson power dividers have been calculated, simulated, and optimised in Agilent Advanced Design System (ADS). The structures are presented in Figure 3.72, Figure 3.75, Figure 3.78, Figure 3.81, Figure 3.84 and Figure 3.87, for the separations of 12mm, 16mm, 20mm, 36mm, 40mm and 45mm, respectively. The simulated S-Parameters are shown in Figure 3.73, Figure 3.76, Figure 3.79, Figure 3.82, Figure 3.85 and Figure 3.88. All of the modified UWB Wilkinson dividers have been fabricated and fully characterised. Figure 3.74, Figure 3.77, Figure 3.80, Figure 3.83, Figure 3.86 and Figure 3.89 summarise the measured S-Parameters.

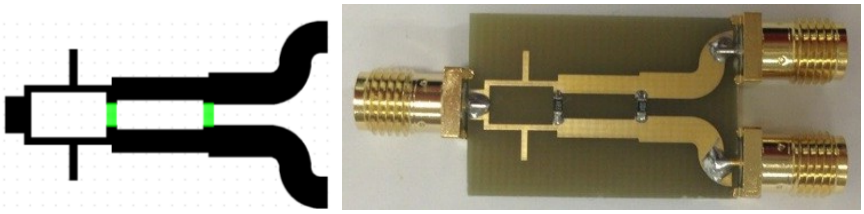


Figure 3.72: Modified UWB Wilkinson Power Divider with Separation of 12mm

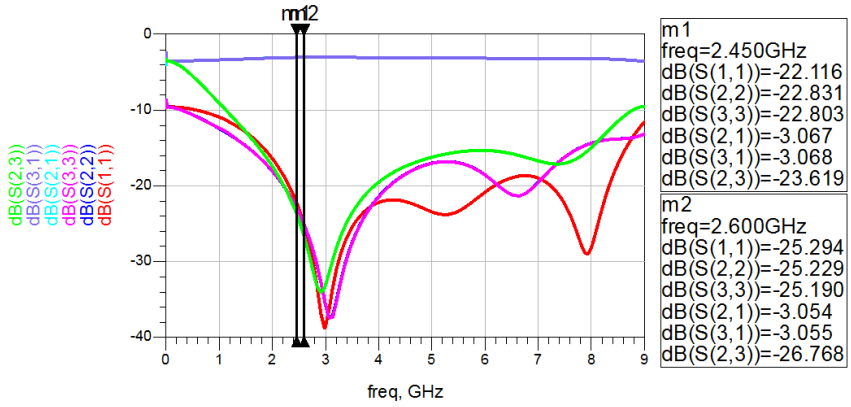


Figure 3.73: Simulated S-Parameters (Magnitude) of Modified UWB Wilkinson Power Divider with Separation of 12mm

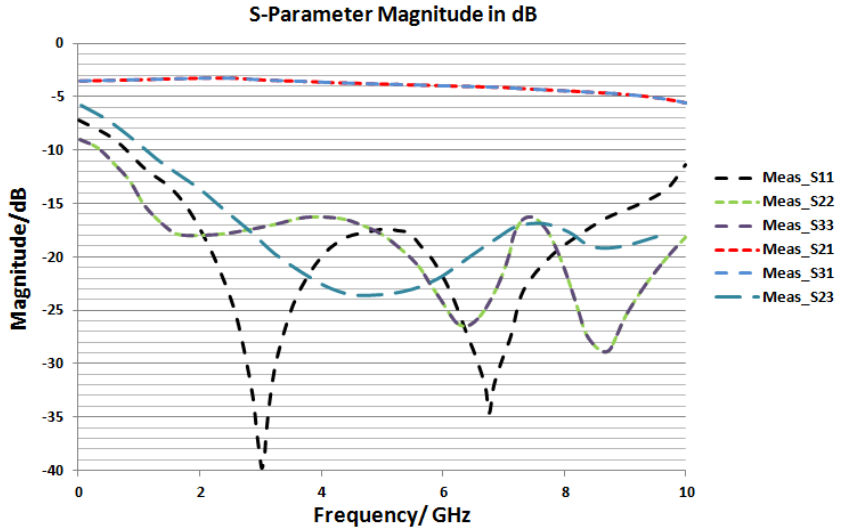


Figure 3.74: Measured S-Parameters (Magnitude) of Modified UWB Wilkinson Power Divider with Separation of 12mm

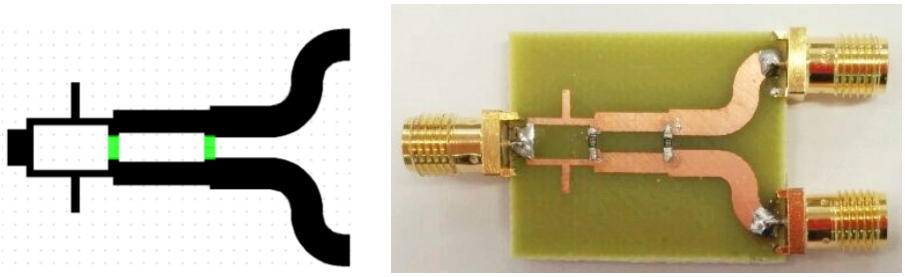


Figure 3.75: Modified UWB Wilkinson Power Divider with Separation of 16mm

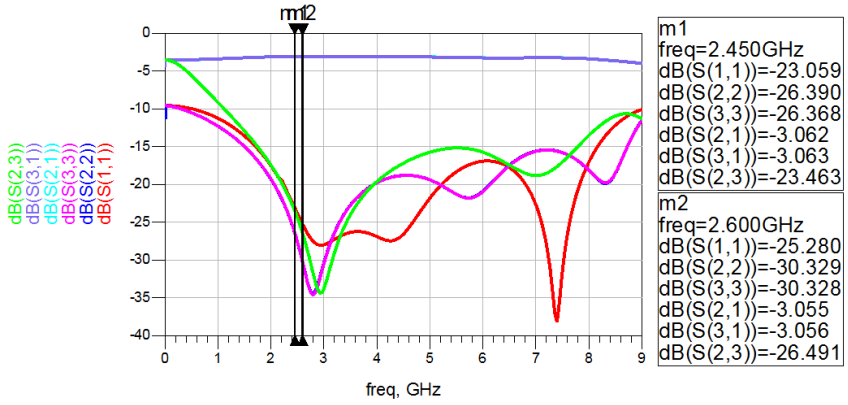


Figure 3.76: Simulated S-Parameters (Magnitude) of Modified UWB Wilkinson Power Divider with Separation of 16mm

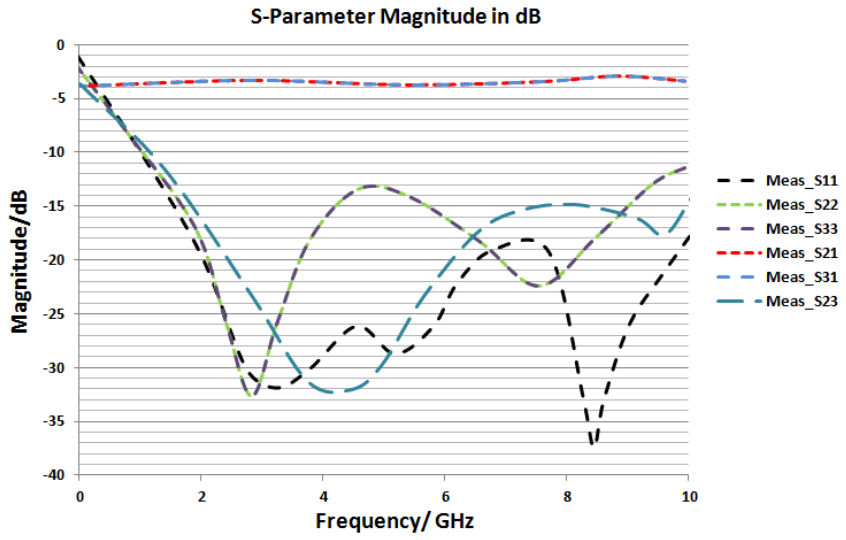


Figure 3.77: Measured S-Parameters (Magnitude) of Modified UWB Wilkinson Power Divider with Separation of 16mm

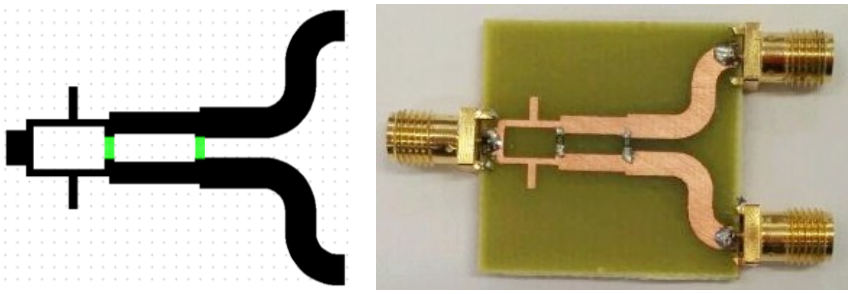


Figure 3.78: Modified UWB Wilkinson Power Divider with Separation of 20mm

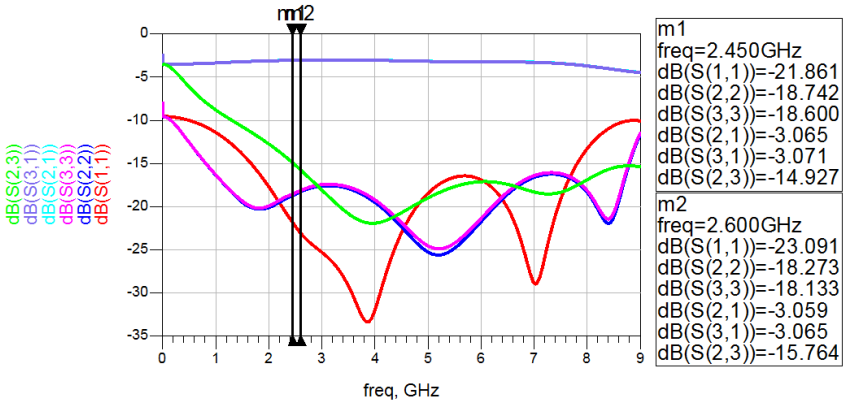


Figure 3.79: Simulated S-Parameters (Magnitude) of Modified UWB Wilkinson Power Divider with Separation of 20mm

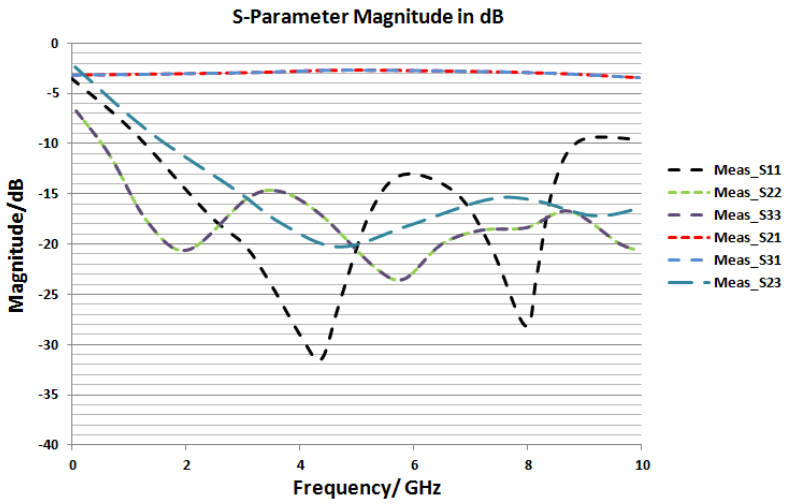


Figure 3.80: Measured S-Parameters (Magnitude) of Modified UWB Wilkinson Power Divider with Separation of 20mm

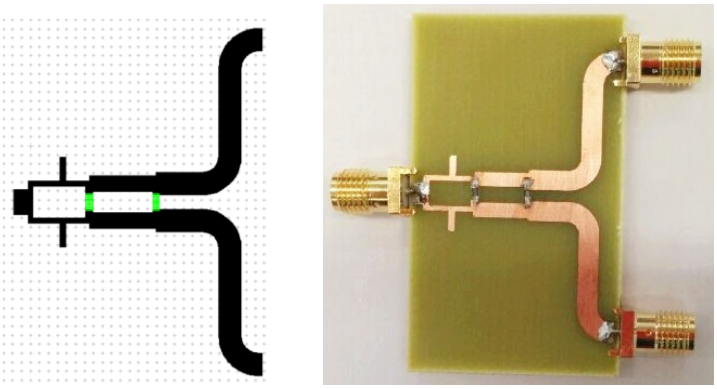


Figure 3.81: Modified UWB Wilkinson Power Divider with Separation of 36mm

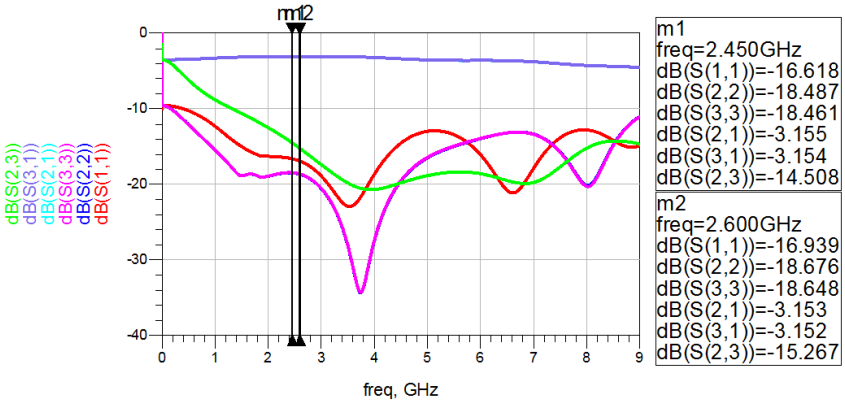


Figure 3.82: Simulated S-Parameters (Magnitude) of Modified UWB Wilkinson Power Divider with Separation of 36mm

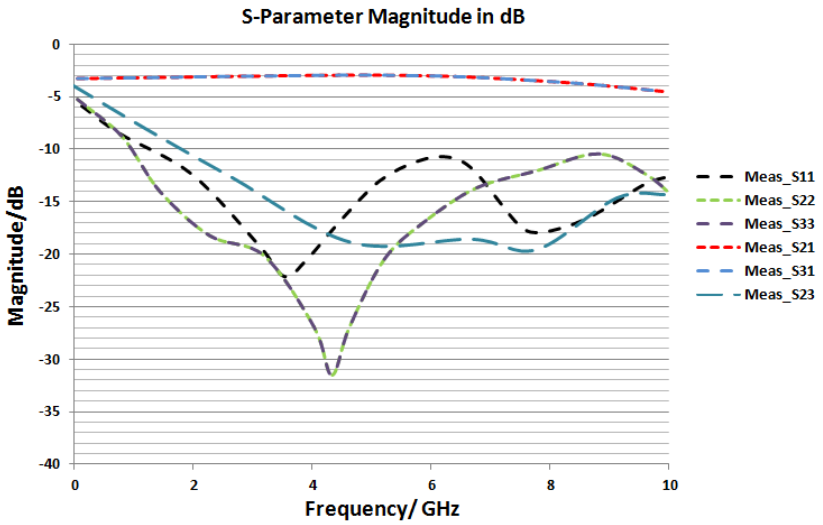


Figure 3.83: Measured S-Parameters (Magnitude) of Modified UWB Wilkinson Power Divider with Separation of 36mm

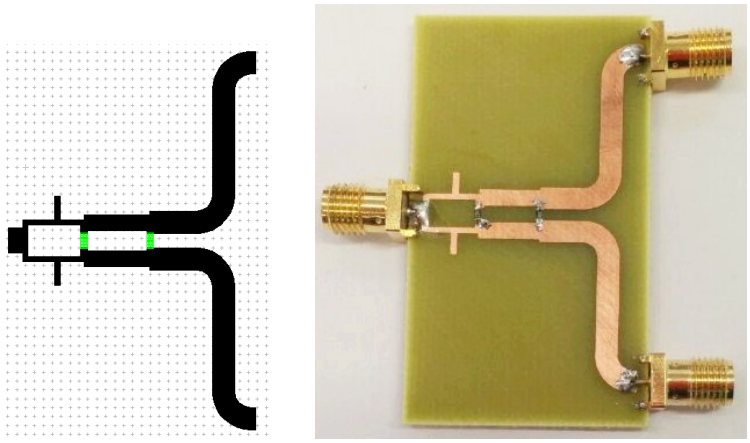


Figure 3.84: Modified UWB Wilkinson Power Divider with Separation of 40mm

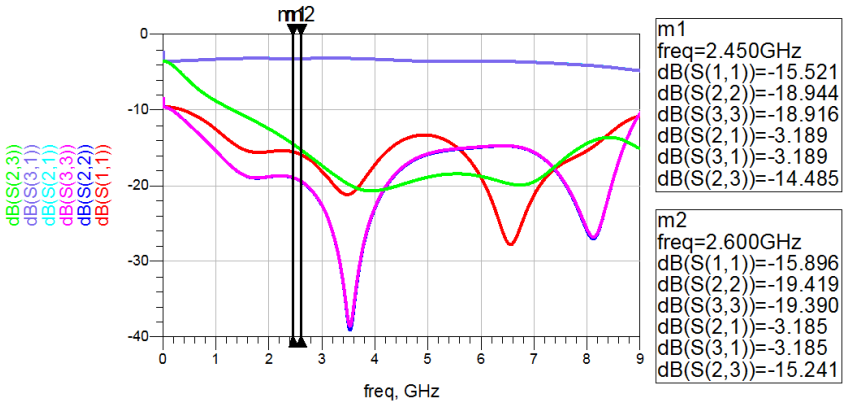


Figure 3.85: Simulated S-Parameters (Magnitude) of Modified UWB Wilkinson Power Divider with Separation of 40mm

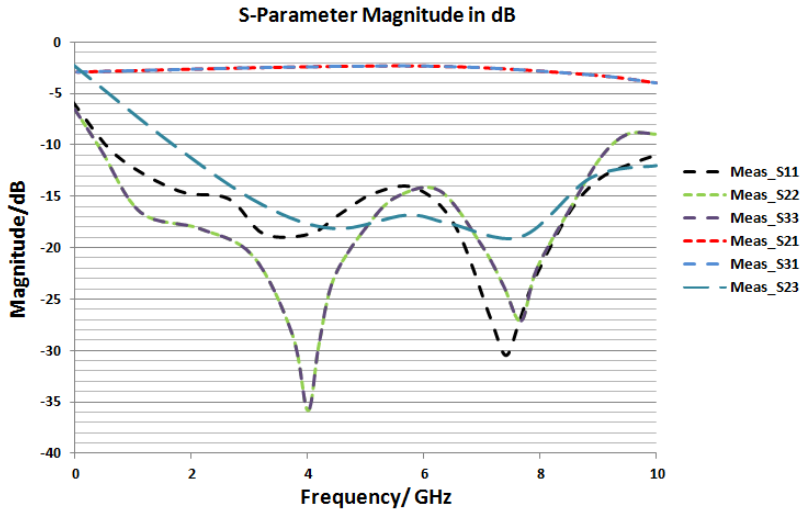


Figure 3.86: Measured S-Parameters (Magnitude) of Modified UWB Wilkinson Power Divider with Separation of 40mm

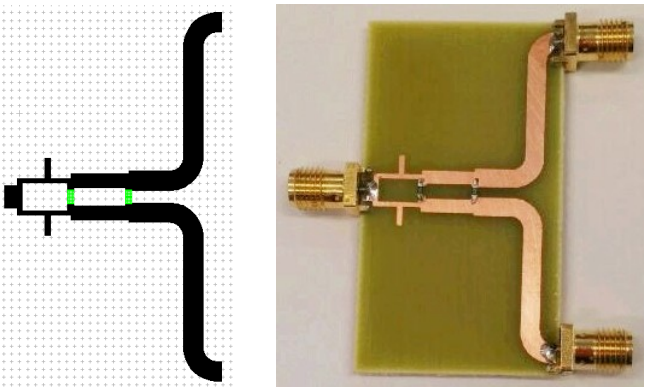


Figure 3.87: Modified UWB Wilkinson Power Divider with Separation of 45mm

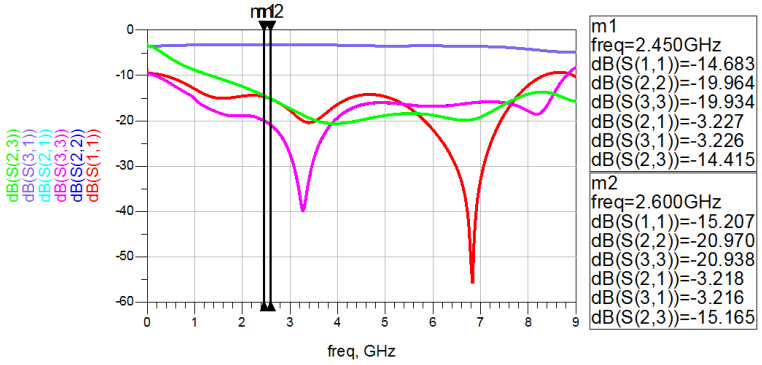


Figure 3.88: Simulated S-Parameters (Magnitude) of Modified UWB Wilkinson Power Divider with Separation of 45mm

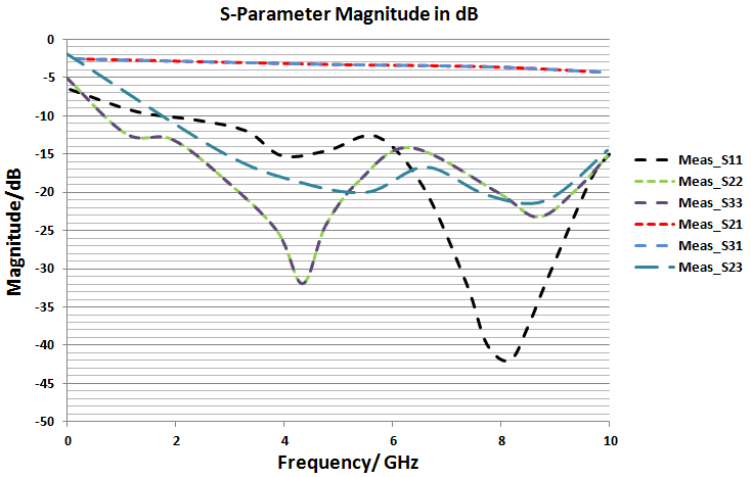


Figure 3.89: Measured S-Parameters (Magnitude) of Modified UWB Wilkinson Power Divider with Separation of 45mm

Figure 3.73 to Figure 3.89 reveal a good consistency between the simulations and measurements of UWB Wilkinson power dividers with various separations. From 0.5 to 10GHz, the UWB configurations demonstrate high return loss (10dB), suitable insertion loss (3.2dB) and high isolation (-10dB). The RF performances at 2.45GHz and 2.6GHz have been

recorded for smart antenna applications. Furthermore, the individual UWB Wilkinson dividers are combined to construct 1:4 UWB feeding networks. Based on UWB Wilkinson divider with separation of 12mm, three types of 1:4 networks have been conceived and simulated. Figure 3.90, Figure 3.92 and Figure 3.94 illustrate the optimised structures. The simulated S-Parameters are shown in Figure 3.91, Figure 3.93 and Figure 3.95, respectively. Finally, a 1:8 UWB feeding network has been designed, simulated and optimised (as presented in Figure 3.96 and Figure 3.97).

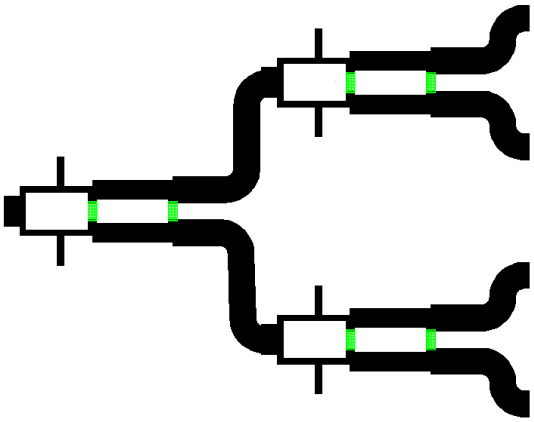


Figure 3.90: 1:4 UWB Feeding Network (Type I) with Separations of 12mm

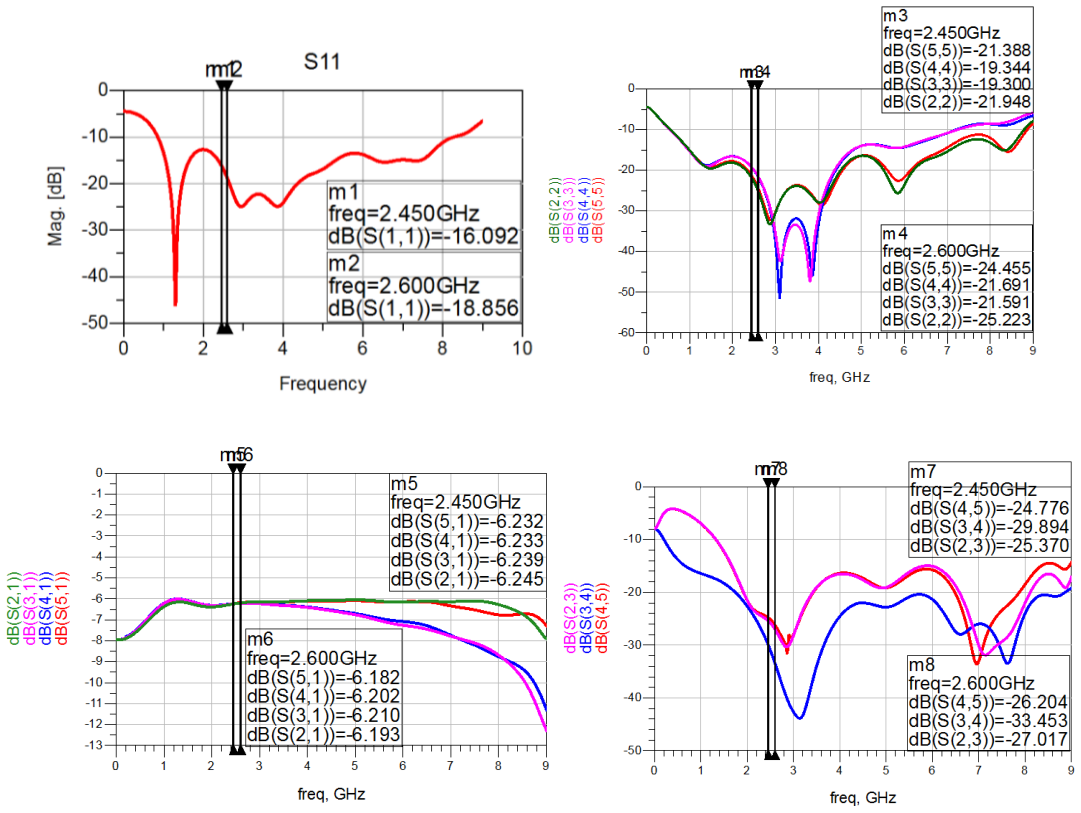


Figure 3.91: Simulated S-Parameters of 1:4 UWB Feeding Network (Type I) with Separations of 12mm

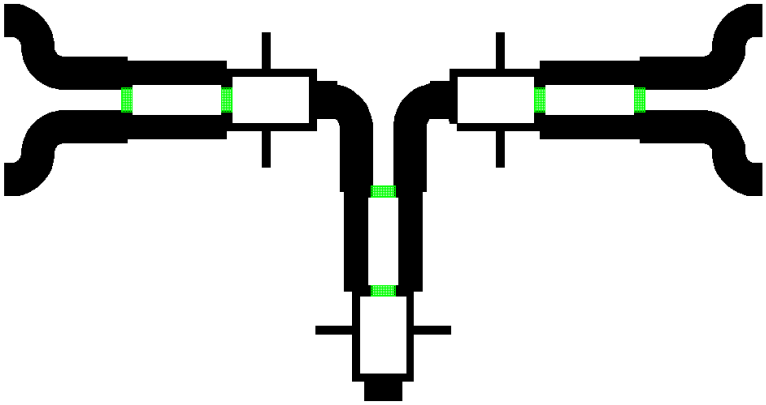


Figure 3.92: 1:4 UWB Feeding Network (Type II) with Separations of 12mm

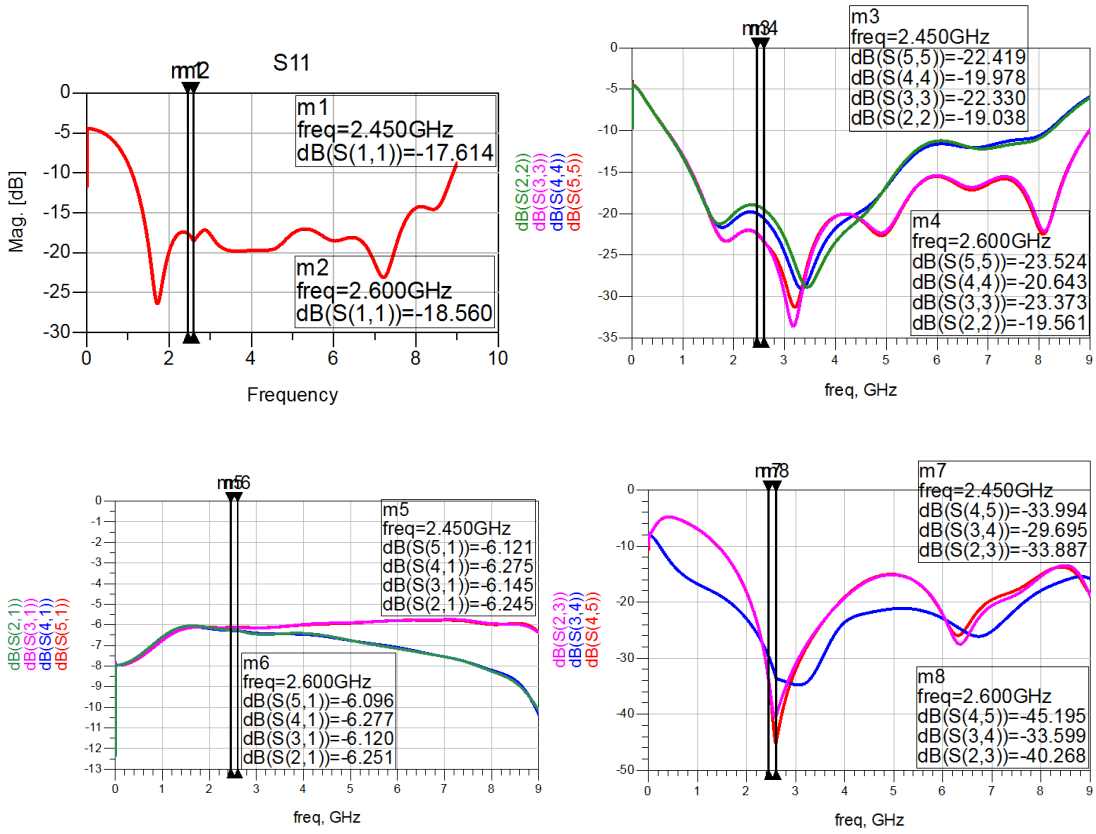


Figure 3.93: Simulated S-Parameters of 1:4 UWB Feeding Network (Type II) with Separations of 12mm

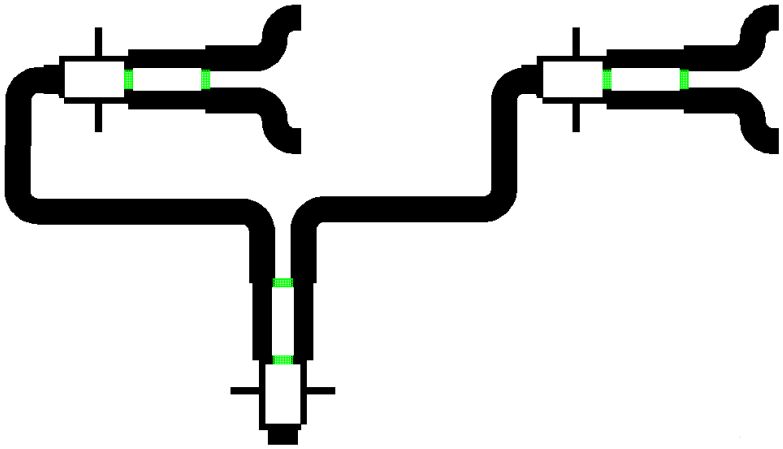


Figure 3.94: 1:4 UWB Feeding Network (Type III) with Separations of 12mm

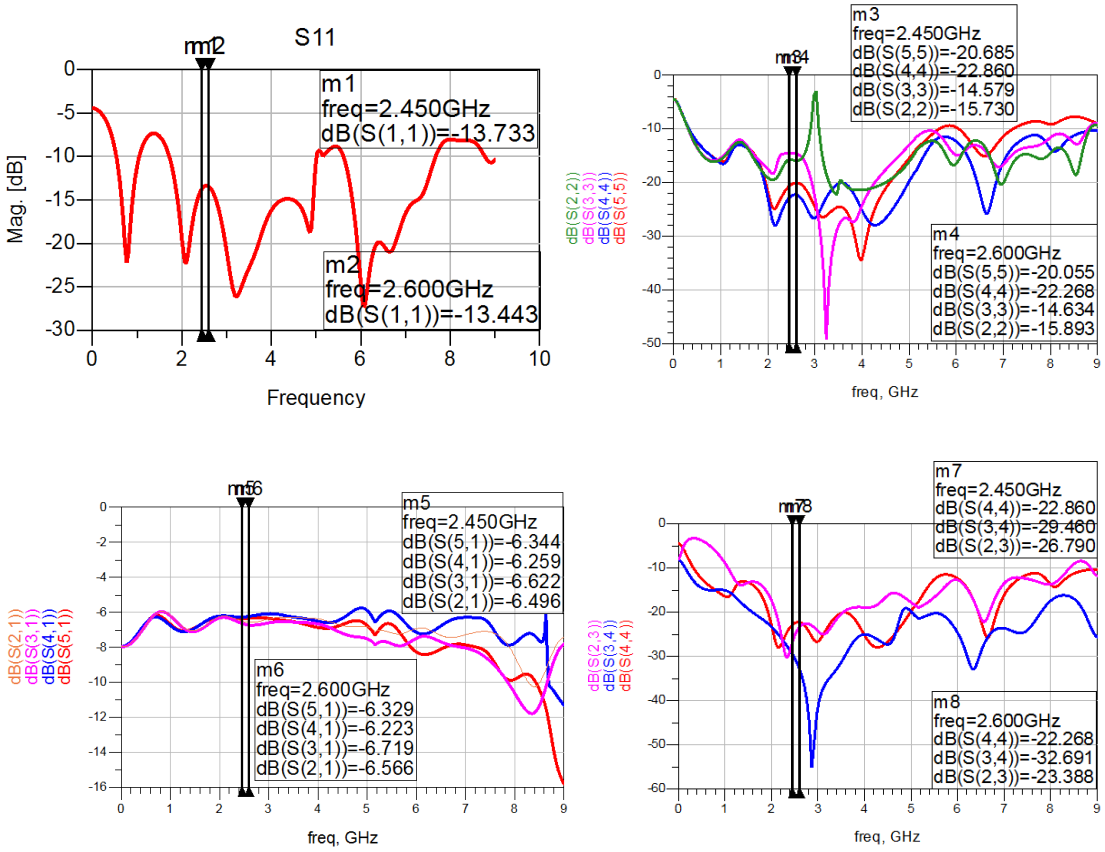


Figure 3.95: Simulated S-Parameters of 1:4 UWB Feeding Network (Type III) with Separations of 12mm

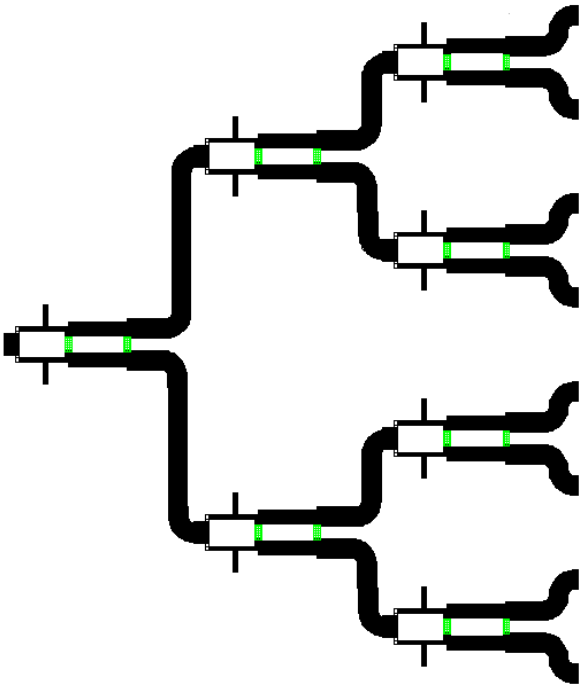
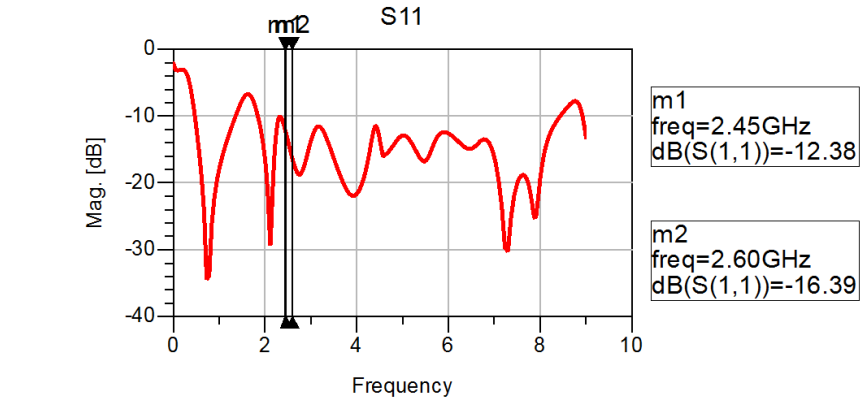
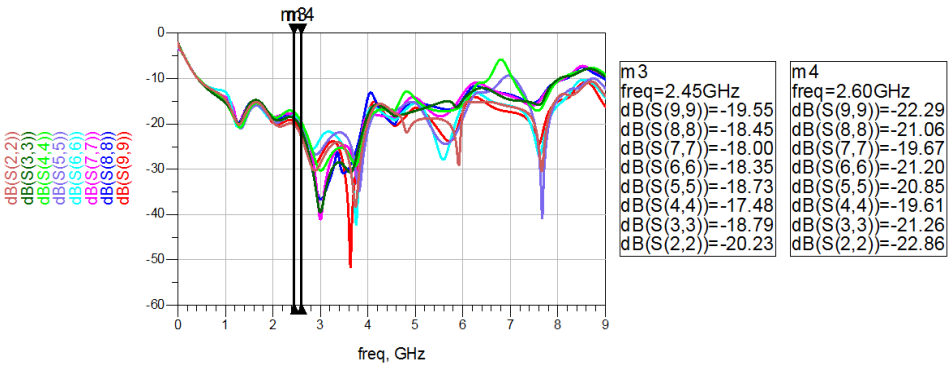


Figure 3.96: 1:8 UWB Feeding Network with Separations of 12mm





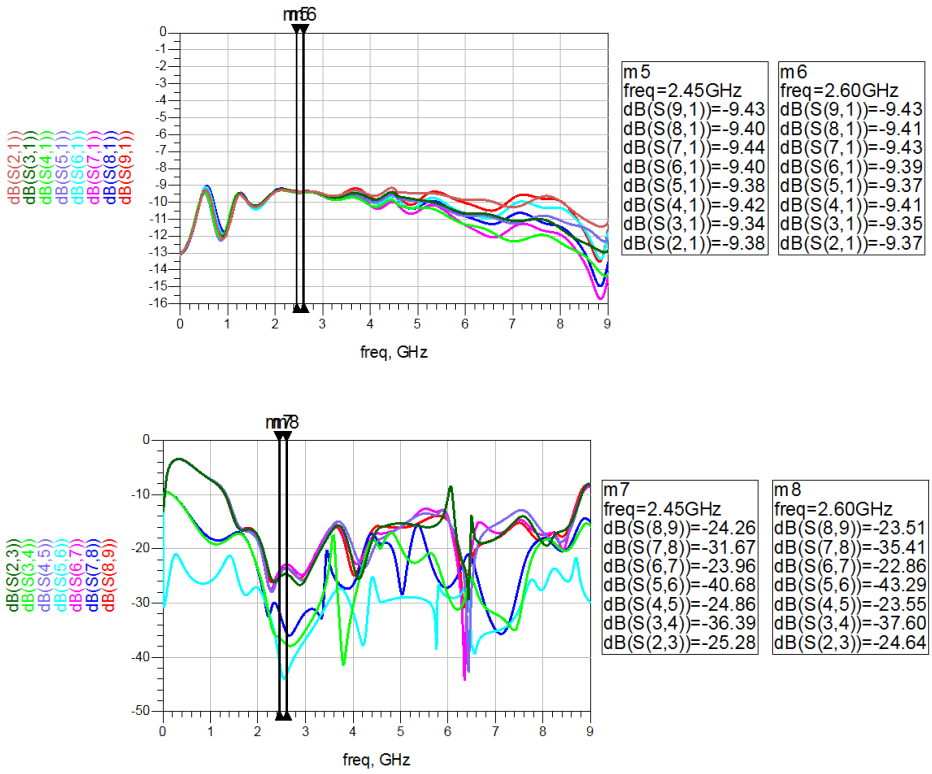


Figure 3.97: Simulated S-Parameters of 1:8 UWB Feeding Network with Separations of 12mm

The results clearly demonstrate that UWB Wilkinson power divider can satisfy all design requirements. Even when expanded to 1:4 and 1:8 feeding networks, it is possible to generate acceptable S-parameters through optimising the width and the length of the traces between these dividers and the locations of each divider. The proposed dividers can be used to construct different feeding network geometries, in order to satisfy the antenna array specifications.

(a) **(b)** **(c)**

Figure 3.98: Other UWB Wilkinson Power Divider Geometries

Moreover, other UWB Wilkinson power divider configurations have been investigated. In Figure 3.98(a), the open stubs are replaced by two fan-shape stubs, which can provide more accurate impedance matching. In Figure 3.98(b), two inductors are used instead of the open stubs. In Figure 3.98(c), additional sections are included into the structure with the purpose of even increasing the operating frequency. However, in these investigated designs, the return loss and insertion loss are worse than the original structure.

3.7.4 UWB Wilkinson Power Divider Third Order Intermodulation Distortion Measurements

Two-tone third order intermodulation (IMD) is a common problem in RF applications. When two (or more) RF signals are present in a communication system, strong harmonic components are often generated. In cases where two RF signals are present, the two signals (F_1 and F_2) mix with each other's second harmonic ($2F_1$ and $2F_2$), which creates distortion products evenly spaced about the fundamentals ($2F_1–F_2$ and $2F_2–F_1$). Components such as amplifiers, filters and power dividers will generate third order intermodulation distortion products. These distortion products degrade the RF performance of many communication systems, such as FM and AM transceivers and smart antenna systems. For instance, signals transmitted with excessive third order IMD will interfere with other transmissions. Receivers must also be distortion-free, especially in the pre-amplifier stages, to prevent crosstalk between adjacent channels.

This section concentrates on the two-tone third order intermodulation distortion measurement of an UWB Wilkinson power divider. Figure 3.99 illustrates the measurement setup. Two signal generators (HP83732A and HPE4400A) are connected with two attenuators, working at F_1 (-9dBm) and F_2 (-10dBm), and generating a two-tone IMD driven through the UWB Wilkinson power divider. A HP8566B spectrum analyser has been used to display the measured signal (also in dBm), in order to analysis linearity of the device.

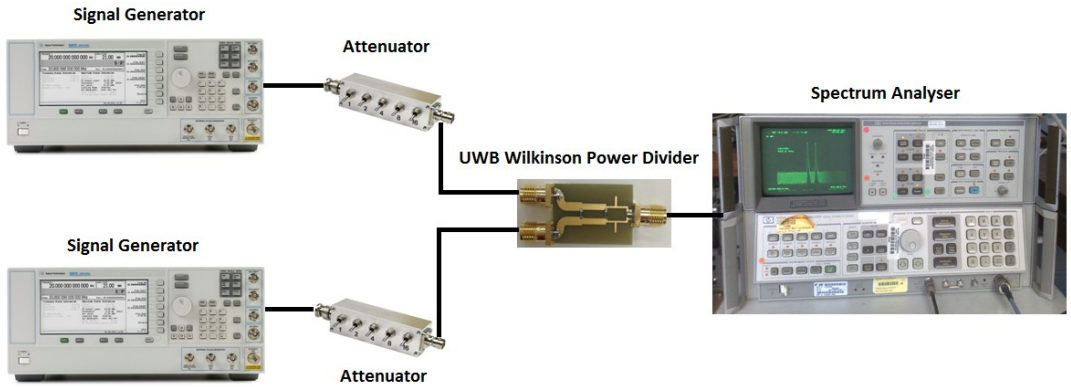


Figure 3.99: Intermodulation Distortion Measurement Setup

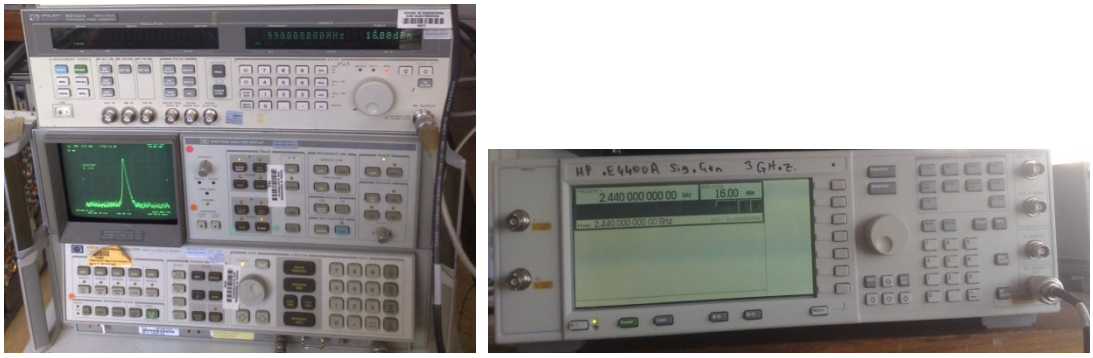


Figure 3.100: Signal Generators (HP83732A and HPE4400A) and Spectrum Analyser HP8566B

Figure 3.101: Attenuator and UWB Power Divider under Test

Various F_1 and F_2 frequencies were tested, including (1000MHz,990MHz), (1550MHz,1540MHz), (2000MHz,1990MHz), (2450MHz,2440MHz) and (3000MHz,990MHz). Due to the frequency limitation of signal generators, the maximum testing frequency can only reach 3000MHz. Harmonic distortions ($2F_1$ and $2F_2$) were recorded. The third order intermodulation frequencies ($2F_1$-F_2 and $2F_2$-F_1) are summarised in Table 3.6. Compared to the fundamental carrier frequencies, the measured results have been converted into dBc. For this third order intermodulation distortion measurement, the UWB Wilkinson power divider with separation of 12mm was under test.

Table 3.6: Third Order Intermodulation Distortion Measurements of UWB Wilkinson Power Divider

IIP3	F_1 (Carrier Frequency)	F_2	$2F_1+F_2$	$2F_1-F_2$	$2F_2+F_1$	$2F_2-F_1$	F_1+F_2	F_1-F_2
Frequency (MHz)	1000	990	2990	1010	2980	980	1990	10
dBm	-9	-10.1	-46.3	-80	-46.3	-81	-45	-32.3
dBc			-37.3	-71	-37.3	-72	-36	-23.3
Frequency (MHz)	1550	1540	4640	1560	4630	1530	3090	10
dBm	-9	-10	-47	-80	-47	-78	-36.9	-33.4
dBc			-38	-71	-38	-69	-27.9	-24.4
Frequency (MHz)	2000	1990	5990	2010	5980	1980	3990	10
dBm	-9	-10.1	-62	-78	-62	-79	-44.3	-31.4
dBc			-53	-69	-53	-70	-35.3	-22.4
Frequency (MHz)	2450	2440	7340	2460	7330	2430	4890	10
dBm	-9	-10	-77	-78.3	-76	-74	-48.6	-29.3
dBc			-68	-69.3	-67	-65	-39.6	-20.3
Frequency (MHz)	3000	2990	8990	3010	8980	2980	5990	10
dBm	-9	-10.1	-80	-90	-85	-90	-50	-33.3
dBc			-71	-81	-76	-81	-41	-24.3

It is significant to note that the UWB Wilkinson power divider demonstrates excellent linearity. The third order intermodulation frequencies ($2F_1$-F_2 and $2F_2$-F_1) are around -80dBm or -71dBc and -79dBm or -70dBc from the fundamental carrier frequencies.

3.7.5 1:4 UWB Feeding Network for Smart Antenna Array

Based on the above design procedure, three modified UWB Wilkinson power dividers have been combined in order to construct a 1:4 UWB feeding network for the smart antenna array. The separations between outputs are 40mm, according to the requirement of the four-element linear planar antenna array discussed in Chapter 2. The schematic and geometry of the UWB feeding network are plotted in Figure 3.102. Furthermore simulations for transmission lines and port dimensions have been carried out in order to optimise the S-Parameters. Figure 3.103 demonstrates the final structure and the fabricated layout.

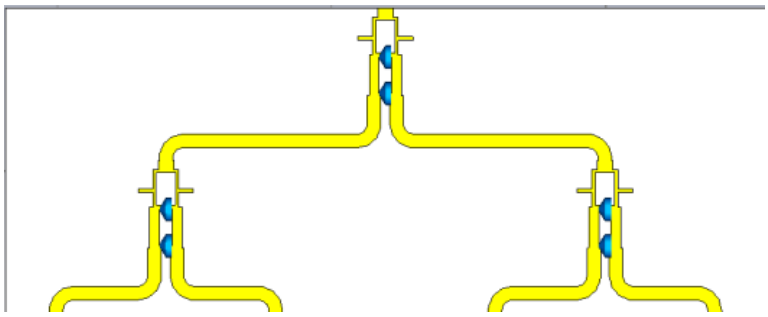


Figure 3.102: Configuration of the UWB Feeding Network for Smart Antenna Array

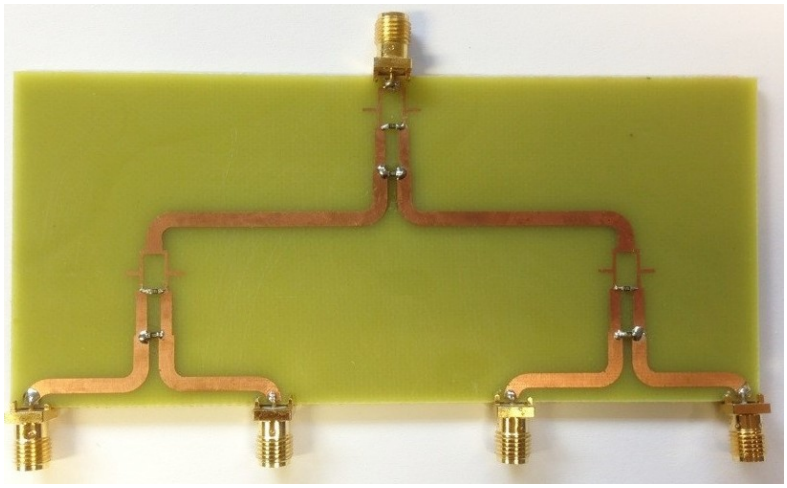


Figure 3.103: Photo of the Fabricated UWB Feeding Network for Smart Antenna Array

Table 3.7 compares the simulated and measured S-Parameters of the proposed UWB feeding network for smart antenna array. 2.45GHz (WiFi/Bluetooth) and 2.6GHz (LTE) are the required frequencies.

Table 3.7: Simulated and Measured S-Parameters of UWB Feeding Network for Smart Antenna Array

S-Parameters	2.45GHz		2.6GHz	
	Simulation	**Measurement**	**Simulation**	**Measurement**
S_{11}(Magnitude)	-15.71dB	-18.54dB	-16.81dB	-20.13dB
S_{22}(Magnitude)	-14.71dB	-15.64dB	-15.69dB	-17.45dB
S_{33}(Magnitude)	-16.45dB	-17.44dB	-15.97dB	-16.33dB
S_{44}(Magnitude)	-15.99dB	-18.45dB	-16.34dB	-17.43dB
S_{55}(Magnitude)	-16.12dB	-16.55dB	-16.98dB	-17.23dB
S_{21}(Magnitude)	-6.79dB	-6.91dB	-6.89dB	-7.12dB
S_{31}(Magnitude)	-6.78dB	-7.11dB	-6.85dB	-7.09dB
S_{41}(Magnitude)	-6.81dB	-7.13dB	-6.85dB	-7.15dB
S_{51}(Magnitude)	-6.76dB	-7.09dB	-6.89dB	-7.13dB
S_{23}(Magnitude)	-25.34dB	-27.98dB	-26.45dB	-28.15dB
S_{34}(Magnitude)	-37.13dB	-39.22dB	-39.47dB	-40.66dB
S_{45}(Magnitude)	-26.99dB	-27.23dB	-27.25dB	-29.02dB

A good agreement between simulation and measurement results is achieved in Table 3.7, verifying all of the suitable S-Parameters of the proposed 1:4 UWB feeding network for smart antenna array.

3.8 Summary

In this chapter, several Wilkinson power divider structures have been investigated and developed in order to construct a suitable feeding network for the smart antenna array system.

Firstly, the elementary T-Junction and resistance three port networks were explained and discussed. Because they are not matched at all ports and have power losses, the operating principles of fundamental Wilkinson power divider is presented, including Even-Odd modes and equivalent circuit analysis. Then, the conventional Wilkinson power divider has been modified and optimised for compact reconfigurable and UWB mobile applications

In Section 3.3, a novel miniaturised silicon-based Wilkinson power divider was analysed, designed, simulated and implemented down to fabrication stage. Based on both simulation and measurement results, it has been demonstrated that the circuit size could be reduced by 65% without significantly increasing the insertion loss or decreasing the bandwidth. At the desired frequency (2.4GHz), the proposed novel silicon-based Wilkinson divider can provide low reflection coefficient (-42dB), suitable forward gain (-3.2dB) and high isolation (-38dB). The developed feeding networks can be applied to industrial, scientific, SIMO communication and energy efficient microwave systems.

In Section 3.4, the design, simulation and measurement results of a novel one-to-eight compact feeding networks for circular antenna array have been presented. The proposed structure consists of four 2-way conventional Wilkinson power dividers with outputs revolving at an angle of 45° to suit circular antenna array geometry. The design has suitable S-Parameters and occupies a size of 25mm radius circle (area of 1986mm^2). At the desired frequencies 2.45GHz and 2.6GHz, the feeding network achieves low reflection coefficient (-16.4dB, -12.3dB), acceptable forward gain (-10.2dB, -10.2dB) and great isolation coefficient (-14dB, -15dB). A good correlation between simulated and measured results is obtained.

Section 3.5 discusses a novel reconfigurable feeding network which enables electronic switching of circular polarisation direction in an antenna array. This is achieved through the digital control of PIN diodes in the feeding network. The lengths of the transmission lines are various, leading to different phase shifts between output ports. Integrated with any four antenna elements, the feeding network is able to switch the polarisation between LHCP and RHCP. The performance of this reconfigurable feeding network has been verified both simulation and experiment. Both simulation and measurement results demonstrate that high return loss (10dB), suitable insertion loss (8dB) and good isolation (-12dB) can be obtained. Phase errors of ± 9º are achieved for required output ports. This feeding network could be applied to multi-function wireless communication systems.

Then, a novel reconfigurable feeding network which allows for the electronic switching among four frequency bands is illustrated in Section 3.6. This is also achieved through the digital control of the bias voltages of PIN diodes. The length of the quarter-wavelength transmission lines can thus be changed, resulting in a change in operating frequency. The feeding network is targeted at four frequency bands: 600MHz-900MHz, 1.2GHz-1.6GHz, 1.8GHz-2.2GHz and 2.4GHz-2.6GHz, in order to cover GSM, GPS, 3G, WiFi and LET applications in different countries. Performance of the synthesised reconfigurable feeding network has been both numerically verified and experimentally tested. Both simulation and measurement results show that high return loss (20dB) and good insertion loss (3.8dB) are obtained. The developed feeding network can be hence applied to multiband wireless communication systems. Moreover, this work forms an important step towards realizing a truly global mobile phone.

Finally, a novel miniaturised UWB Wilkinson power divider has been designed, calculated, analysed, simulated, fabricated and characterised. Dimension of the proposed UWB power divider configuration is only 9.5mm×15mm and the design demonstrates high return loss (10dB), low insertion loss (3.2dB) and high isolation (10dB) through 0.5GHz to 10GHz, generating an ultra wide band performance. The simulations were validated through a real implementation with the measured testing results agreeing with simulated results. Based on the UWB Wilkinson power divider structure, several UWB dividers with different output separations were successfully developed, which include 12mm, 16mm, 20mm, 36mm, 40mm and 45mm. These modified geometries could satisfy different antenna array inter-spacing. Furthermore, third order intermodulation distortion measurements for the proposed UWB devices were carried out, in order to confirm the linearity. Eventually, 1:4 and 1:8 UWB feeding networks based on the UWB Wilkinson power divider are discussed. A linear 1:4 UWB feeding network with separations of 40mm is developed and characterised for the smart antenna array. Suitable S-Parameters are obtained.

In a conclusion, the investigation of feeding network for smart antenna array discussed in this thesis is illustrated in Figure 3.104

The UWB feeding network developed in this chapter is able to control the magnitude of the antenna radiation. In the next chapter, various phase shifter technologies will be discussed and compared. An integrated UWB feeding network with high accurate analogue phase shifters for the complete smart antenna array will be presented and analysed.

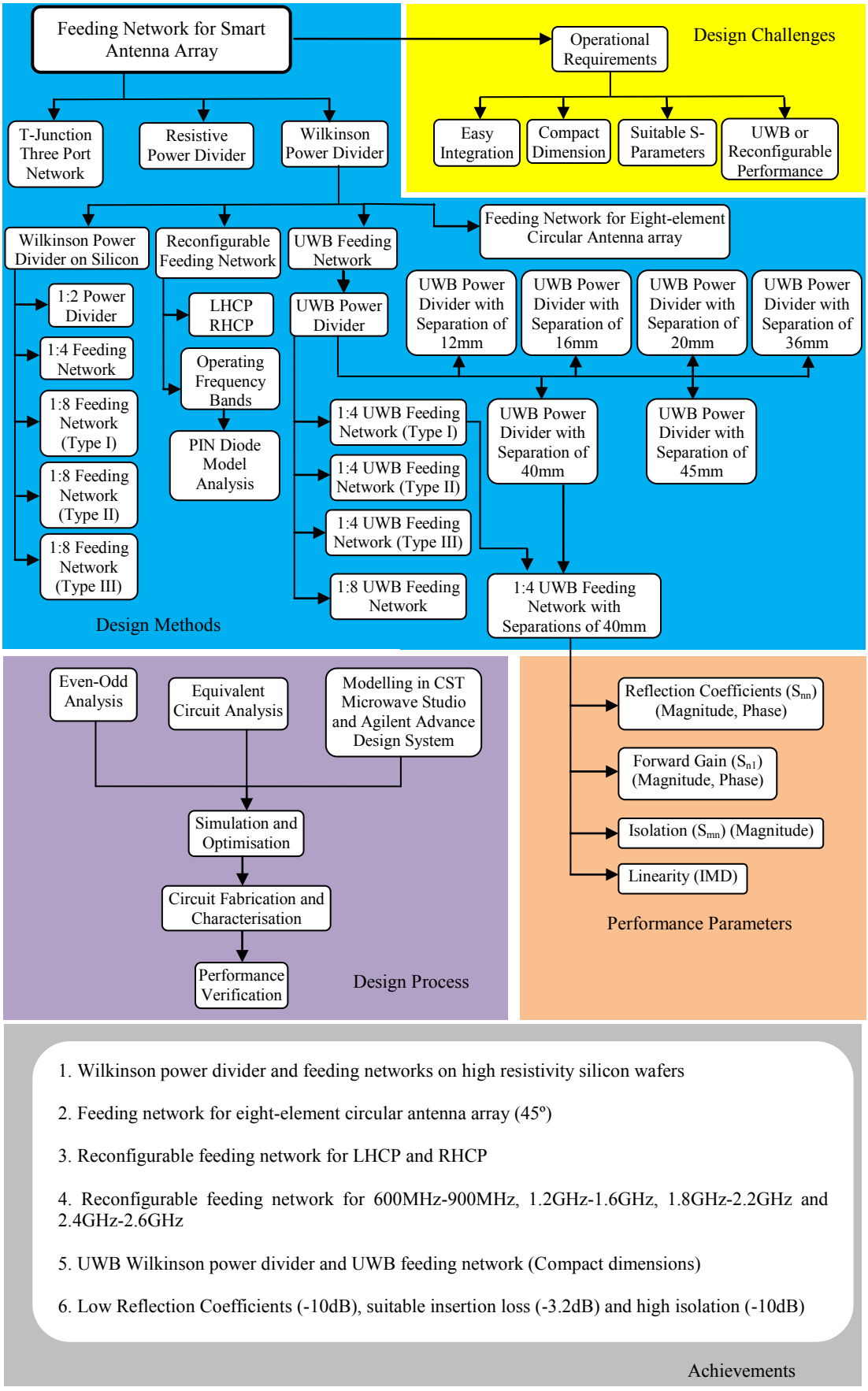


Figure 3.104: The Investigation of Feeding Network for Smart Antenna Array

Chapter 4: Smart Antenna Array Implementation

4.1 Introduction

In the smart antenna array systems, phase shifters are used to generate the required phase excitations for the antenna elements for main beam steering. Using the antenna analysis from Chapter 2 and UWB feeding network designed in Chapter 3, this chapter presents a complete smart antenna array and its full characterisation.

Research investigation begins with different topologies of phase shifters developed in the past and the associated practical considerations, which includes diodes, FETs, MMIC, and MEMS technologies. For comparisons, a low loss and high accurate analogue phase shifter from Hittite Microwave Corporation has been selected and fully evaluated. For impedance matching, compact and ultra wideband CPW-to-Microstrip transitions are utilised between the phase shifters, feeding network and antenna elements. All components in the smart antenna array are fabricated and characterised separately. Finally, this chapter proposes a complete smart antenna array based on microstrip structures, in order to simplify the configuration and reduce the energy loss.

Figure 4.1 presents the system layout. The individual element in the array is a planar monopole antenna with Archimedean spiral slots, covering multiband frequencies, with suitable S-Parameters and proper radiation patterns. The feeding network consists of three ultra wideband (UWB) Wilkinson power dividers which provide high return loss, equal power splitting, low insertion loss and ultra wide band performance. High accuracy and low loss analogue phase shifters and ultra wide band CPW-to-Microstrip transitions have also been integrated into the smart antenna systems. All of the components are designed, simulated,

fabricated and characterised individually before establishing the whole system, in order to confirm the RF performance. Furthermore, the capability of the proposed fully implemented smart antenna has been experimentally verified by measurements of the manufactured array.

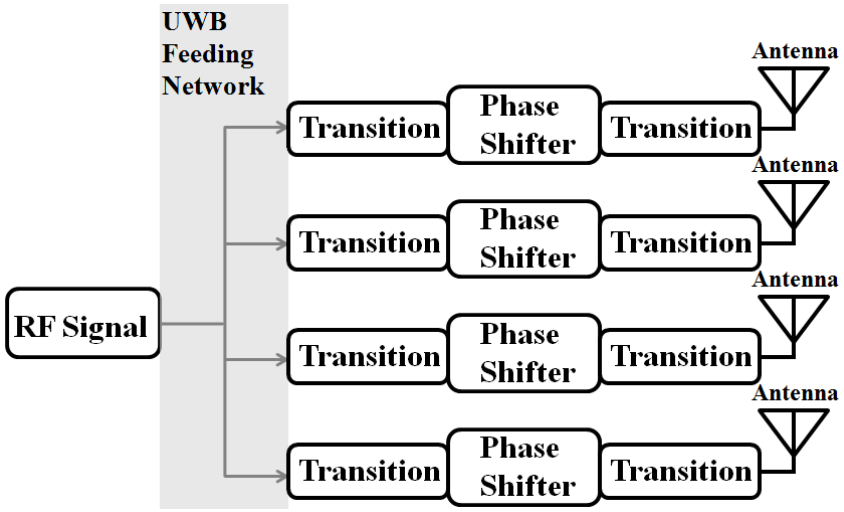


Figure 4.1: Smart Antenna Array System Layout

This chapter is mainly divided into five sections. Section 4.1 provides an overview of phase shifters and existing approaches for their implementations. Section 4.2 discusses the evaluation methods and performance of the Hittite analogue phase shifter. UWB CPW-to-Microstrip transition structures are shown in Section 4.3 and Section 4.4 presents the complete smart antenna array characterisation. Finally, Section 4.5 summaries this chapter.

4.2 Phase Shifter Introduction

Phase shifters are essential components in realising a phased array antenna system. During the last six decades, the design approaches and fabrication processes have gone through significant changes. In this section, some of the successful implementations to realise microwave phase shifters are reviewed and compared.

The earliest forms of phase shifters were all mechanical. Rotary vane adjustable waveguide phase changer was first proposed by Fox in 1947 [60] and the helical line phase changer for linear antenna array beam steering is developed by Stark in 1957 [108]. Prior to the development of electronically variable phase shifters, all the phased array antennas were implemented with mechanical phase shifters. Mechanical phase shifters are simple and inexpensive for fabrication. Hence they have been widely utilised in applications that do not require fast changing of phase shifts [109].

Electrical phase shifters could be made of: ferrite materials, Semiconductor/MMIC, and MEMS based fabrication approaches [110]. In these structures, there are no moving components and phase shift is achieved by applying a bias field. The following sub-sections explain some of these configurations.

4.2.1 Ferrite Phase Shifter

In 1957, the first electronically variable ferrite phase shifter was reported by Reggia and Spencer [111]. Currently, most of the ferrite phase shifters are realised in waveguide geometry, and only quite a few designs are in strip line, microstrip line and coaxial line configurations. Figure 4.2 presents the structure of a ferrite phase shifter. By varying the DC bias voltage, the magnetic field of the device is changed, which influences the permeability of the ferrite material. Because phase constant is a function of permeability, finally, the DC bias can control the phase shifts of the ferrite devices. Moreover, shape and geometry of the ferrite material will also affect the performance of the phase shifter [112].

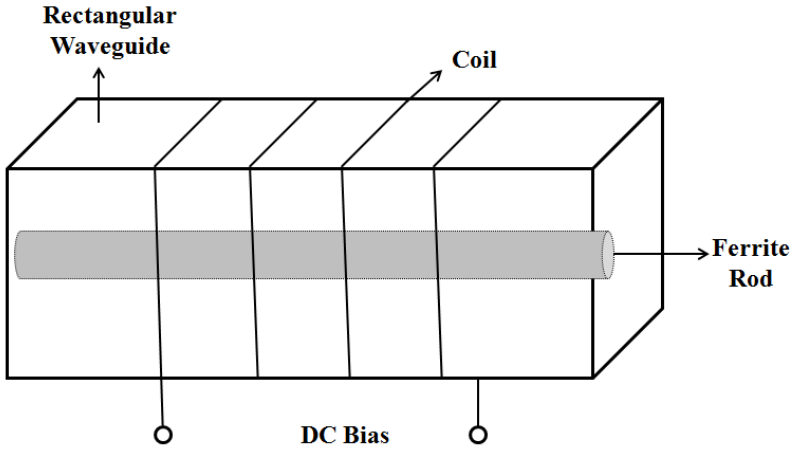


Figure 4.2: Ferrite Rod in Rectangular Waveguide

Planar ferrite phase shifters using microstrip transmission lines are presented in [113, 114] and ferrite tunable device is demonstrated in [115]. In [113], phase shifter is implemented using microstrip transmission lines on Yttrium Iron Garnet/Gadolinium Gallium Garnet (YIG/GGG) substrate, which is operated on magnetic field ($H_0\mu_0$) of 0.057T for numerical analysis. Similarly, in [114], a tunable device utilising symmetrically coupled microstrip transmission lines on a obliquely magnetised YIG substrate with magnetic field ($H_0\mu_0$) of 0.1T has been discussed. In [115], a phase shifter is achieved by placing a YIG bar on top of a microstrip transmission line. This configuration requires a very high magnetic field of 5.6kA/m, which is applied externally. An electromagnet was used for external magnetic field in order to characterise the device (as illustrated in Figure 4.3).

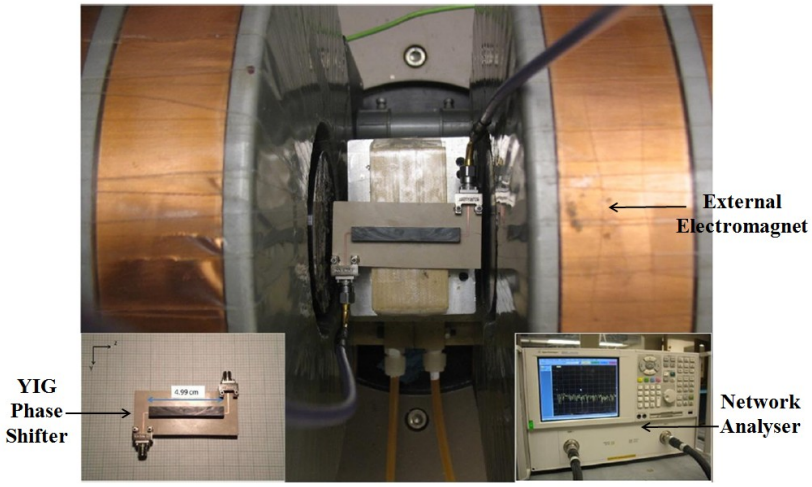


Figure 4.3: YIG Phase Shifter Measurement Setup [115]

The ferrite phase shifters have many advantages such as low losses and high power handling. However, dimensions of the devices are always huge, also they are heavy, temperature sensitive, high DC power consumptions, and expensive to fabricate [112,116, 117].

4.2.2 Planar Phase Shifter

Ferrite phase shifters are suited primarily for coaxial cables and non-planar waveguides, but not popular with planar transmission lines such as strip lines, microstrip lines, and coplanar waveguides. Planar transmission lines are highly preferred for miniaturising devices with low cost and simplifying the integration with antenna arrays. Some planar ferrite phase shifters have been discussed in Section 4.2.1, but the external set up is bulky. Therefore, electrical phase shifters are more attractive due to low cost and compactness. This section will concentrate on phase shifters using PIN diodes, field effect transistors and electro-mechanical structures. These designs could be configured as either switched delay lines or loaded transmission lines.

4.2.2.1 Switched Delay Line Phase Shifter

The switched line phase shifter is actually a time-delay circuit in which phase shift is achieved by varying the transmission line sections with different electrical lengths.

A schematic of the switched delay line phase shifter is depicted in Figure 4.4. There are four switches in the circuit to control the phase shifts. When the switches SW_1 and SW_3 are closed, while SW_2 and SW_4 are open, the RF signal is travelling through transmission line l_1. When the switching states are reversed, RF signal transmission is through the upper length $l_1+\Delta l/2+\Delta l/2= l_1+\Delta l$. The phase shift $\Delta\varphi$ between the two switching states is $\beta(\Delta l)$, where β

represents the propagation constant of the transmission line. PIN diodes and transistors are widely used as switching elements in switched delay line semiconductor phase shifters implementations [118].

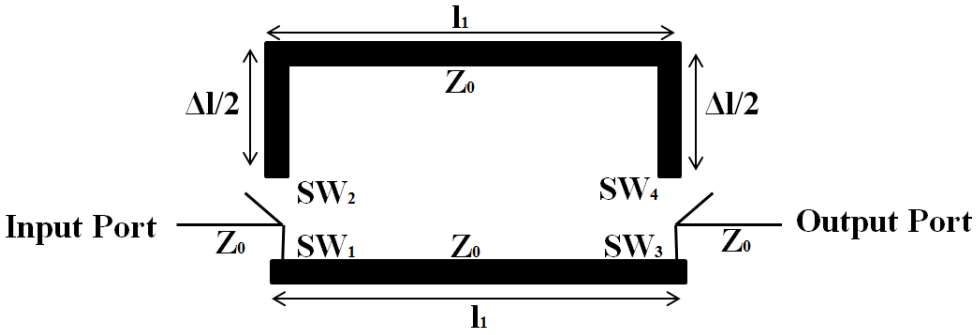


Figure 4.4: Basic Schematic of Switched Delay Line Phase Shifter

In Figure 4.4, basic switched delay line phase shifter is constructed on microstrip transmission lines with characteristic impedance of Z_0 [110]. Propagation constant of the transmission lines could be determined using the Equations (4.1) to (4.5) [37]:

The effective dielectric constant of microstrip transmission line is calculated by:

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2 \times \sqrt{1 + 12h/w}} \tag{4.1}$$

Where, ε_r represents the dielectric constant of the substrate, h is the substrate thickness and w stands for the signal conductor width. Then the propagation constant is given by:

$$\beta = \frac{2\pi}{\lambda} \tag{4.2}$$

$$\lambda = \frac{v}{f} \tag{4.3}$$

$$v = \frac{c}{\sqrt{\varepsilon_e}} \tag{4.4}$$

From Equations (4.2) to (4.4), propagation constant β can be expressed as:

$$\beta = \frac{\omega}{c}\sqrt{\varepsilon_e} \tag{4.5}$$

In some practical designs, multiple stages of the switching sections can be integrated in order to build reconfigurable phase shifters (as discussed in Chapter 3, Section 3.6). Another example of the reconfigurable geometry is illustrated in Figure 4.5, which shows three stages. Each stage generates a different electrical length of Δl. These values are typically selected so that the circuit is able to provide 360° phase shift by suitably controlling the switching circuit.

Each stage requires a bit (0/1) of the control circuit, therefore this configuration (shown in Figure 4.5) is defined as a 3-Bit phase shifter. Switching elements utilised in these phase shifters can be Pin diodes, FETs, and MEMS switches with appropriate biasing networks and DC blocking arrangements.

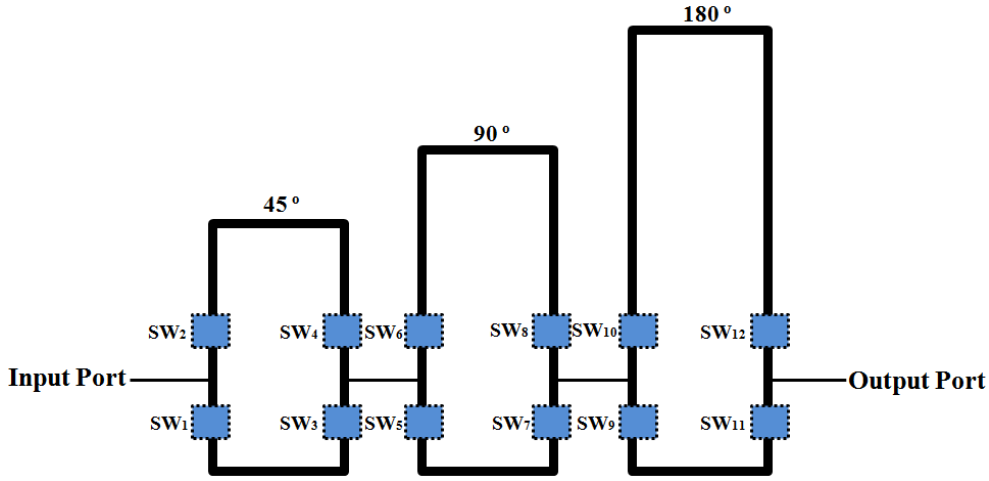


Figure 4.5: 3-Bit Switched Delay Line Phase Shifter

4.2.2.1.1 PIN Diodes Switched Delay Line Phase Shifter

Figure 4.6 demonstrates a typical circuit layout of a series-diode switched delay line phase shifter using microstrip transmission lines. When diodes D_1 and D_3 are supplied with forward bias and D_2 and D_4 are reverse biased, RF signal travels through l_1. While D_2 and D_4 are forward biased and D_1 and D_3 are reverse biased, RF signal follows the transmission line of l_2.

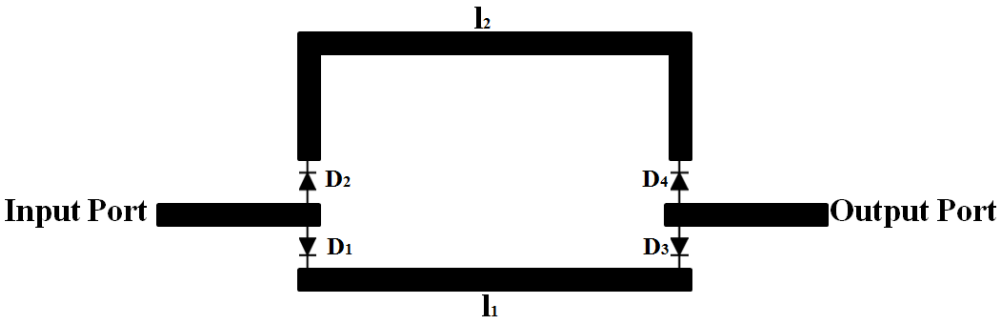


Figure 4.6: Series Diode Switched Line Phase Shifter

4.2.2.1.2 FETs Switched Delay Line Phase Shifter

MESFETs can also be used to implement switched delay line phase shifters. Compared to the P-I-N diode, the GaAs MESFET provides many advantages such as ultra fast switching and minimum DC power consumption. Moreover, dual gate FET (DGFET) is preferred over the single gate FET due to its much higher on-off switching ratio. Figure 4.7 demonstrates the

schematic of a phase shifter using DGFET [110]. It is assumed that two FETs have the same transfer phase and gain. At the input port, a Wilkinson power divider splits the signal equally and feeds the in-phase outputs to first gates (G_{1B} and G_{1A}) of the two FETs. Then the second gates G_{2B} and G_{2A} are applied with control voltages. The two DGFETs are operated in a complementary manner, which means when FET B in on state, FET A is in pinched off state, and vice versa. Thus switching between the two transistors, signal is allowed to pass through alternate transmission line paths (Path B or Path A). Due to Δl, the relative phase delay between two paths generates the differential phase shift. Finally, another Wilkinson power combiner recombines the two output paths into a single terminal. In this configuration, there is a 3dB power loss in each of the power diver and combiner. Assuming the mismatch and other circuit losses are negligible, if G is the gain of the DGFET, the overall gain of the phase shifter is (G-6) dB.

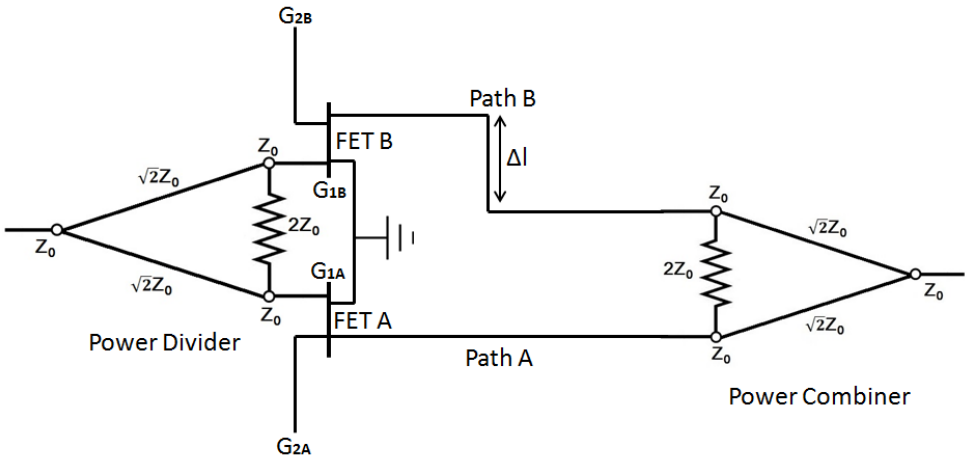


Figure 4.7: Schematic of Dual Gate FET (DGFET) Phase Shifter [110]

4.2.2.1.3 MMIC Phase Shifter

The semiconductor phase shifter is based upon microwave integrated circuit (MIC). In hybrid MIC, all of the passive components are deposited on the low loss dielectric substrate surface. Discrete semiconductor devices are either soldered or bonded onto the passive circuits. For the monolithic microwave integrated circuit (MMIC) technique, the entire circuit consisting of active devices, passive circuit elements, and interconnections are formed on or within a semi-conducting, semi-insulating substrate. The main advantages of MMIC over the hybrid MIC are its light weight, small dimensions, improved reliability, reproducibility through elimination of wire bonding, and its ability to incorporate multifunctional performance on the single chip. Elimination of wire bonding and embedding of active devices within the semi-conducting substrate reduces the undesired parasitics and also improves the

bandwidth performance. The MMIC circuit diagram is illustrated in Figure 4.8 [119], which is comprised of FETs, resistors, capacitors and inductors. Figure 4.9 demonstrates the photograph of MMIC. All of the components are fabricated on a single substrate of GaAs [119].

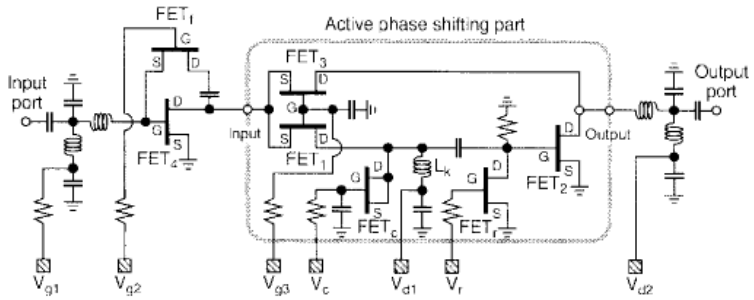


Figure 4.8: MMIC Circuit Configuration [119]

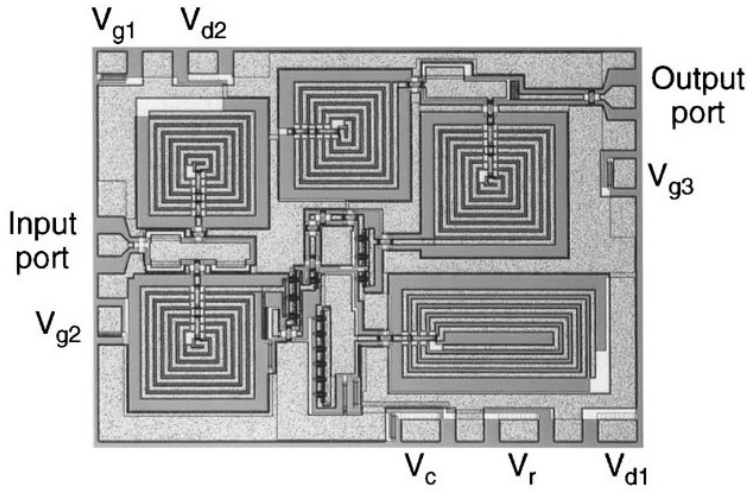


Figure 4.9: Photo of the Fabricated MMIC [119]

4.2.2.1.4 MEMS Phase Shifter

Microelectromechanical Systems (MEMS) is a novel technology and is being considered as a promising method for RF circuits because of high RF performance, low DC power consumption and high linearity compared to semiconductors. MEMS phase shifters are also configured into two directions: switched delay line MEMS phase shifter and varactor loaded transmission line MEMS phase shifter. MEMS phase shifters are implemented using MEMS switches.

RF MEMS switch is realised with air bridges as presented in Figure 4.10. The structure is made of air bridges anchored at one or more points and a bottom electrode under the bridge which is covered with thin dielectric materials. Air bridges are electrostatically actuated to

achieve the switching or varactor actions. Hence this device can replace the PIN diodes and semiconductor phase shifters presented previously. Bias voltage is supplied between the air bridge and the bottom electrode for electrostatic actuation. When the air bridge touches the bottom dielectric, the MEMS operates as a switch and while the air bridge is actuated below pull-in voltage, the device is used as a varactor. Pull-in voltage is the bias voltage at which the air bridge snaps on the dielectric layer.

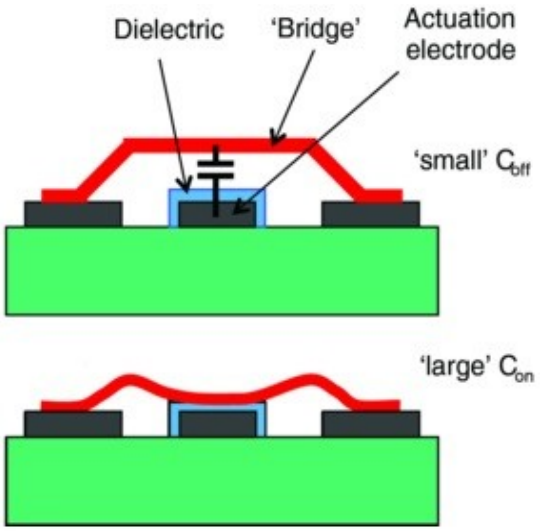


Figure 4.10: RF MEMS Switch, ON and OFF State

MEMS switched delay line phase shifter is implemented by applying MEMS switches in the Figure 4.10. Operating principles of MEMS switched delay line phase shifter is similar to the semiconductor phase shifter. Figure 4.11 demonstrates an 4-bit switched delay line MEMS phase shifter [112].

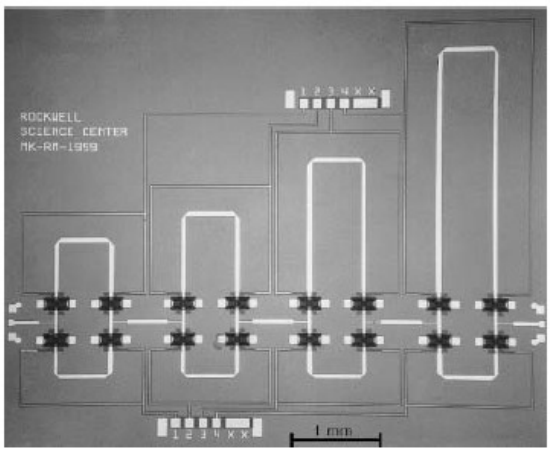


Figure 4.11: 4-Bit RF MEMS Switched Delay Line Phase Shifter [112]

4.2.2.2 Loaded Transmission Line Phase Shifter

In a loaded transmission line phase shifter, a transmission line is reactively loaded to control the phase shift of the output signal. There are two methods to obtain phase shifters utilising loaded transmission lines: lumped and distributed. The conventional circuit of the lumped approach incorporates two identical capacitances C_1 at the ends of a transmission line with length of 2l, and a variable capacitance C_2 located at the middle of the line, as presented in Figure 4.12. The end capacitances C_1 will control the phase shift, whereas the middle C_2 is adjusted to provide a suitable input matching [110].

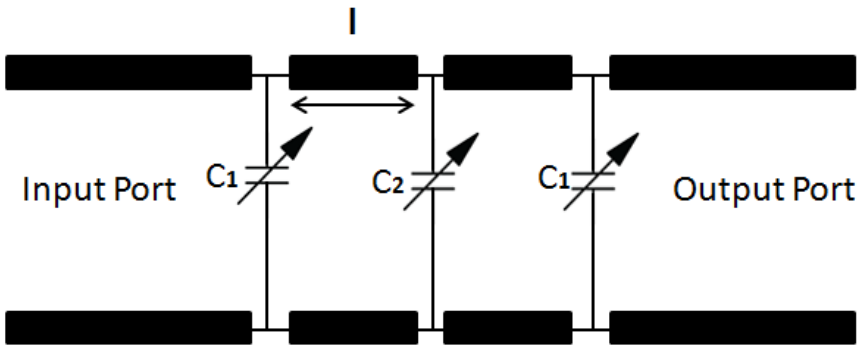


Figure 4.12: Loaded Transmission Line Phase Shifter with Shunt Varactors

Varactors loaded transmission line phase shifter use voltage-controlled varactors shunted at intervals across the transmission line. The capacitance of the varactor is a function of control voltage as expressed below:

$$C(V)=\varepsilon_0 A/d(V) \qquad (4.6)$$

For the distributed approach, the transmission lines are periodically loaded with variable capacitors, as illustrated in Figure 4.13.

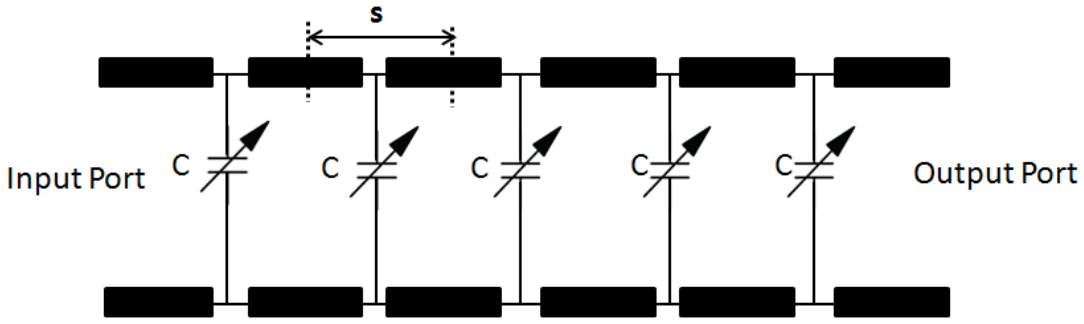


Figure 4.13: Distributed MEMS Transmission Line Phase Shifter

The separation "s" between these capacitors is too small that the modified telegraphic equation could be used to explain the propagation performance of the loaded transmission lines. Assuming the transmission lines are lossless:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{4.7}$$

$$v = \frac{1}{\sqrt{LC}} = \frac{c}{\sqrt{\varepsilon_{eff}}} \tag{4.8}$$

Where Z_0 is the characteristic impedance of the transmission line, L and C are the inductance and capacitance of transmission line, respectively. Using the Equation (4.7) and (4.8), the following formulas can be obtained:

$$C = \frac{\sqrt{\varepsilon_{eff}}}{Z_0 c} \tag{4.9}$$

$$L = cZ_0^2 \tag{4.10}$$

Where, $$C = C_t + \frac{C_{bo}}{s} \tag{4.11}$$

C_t is the distributed capacitance of the transmission line, while C_{b0} is the variable capacitance [120]. C_{b0} can be modified by various approaches such as tunable metal-insulator-metal (MIM) capacitors, inter-digital capacitors, varactors, and building bridges above the transmission line. The Propagation phase constant (β) is calculated by:

$$\beta = \frac{\omega}{v} \tag{4.12}$$

The capacitance C is controlled by the appropriate bias, which will change the phase of propagation, and so generating an effective 'φ' phase shift.

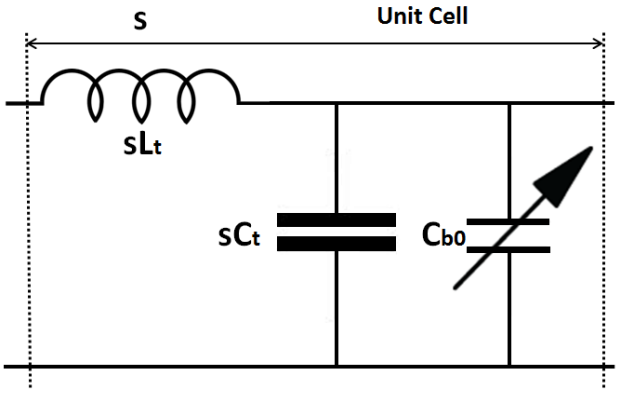


Figure 4.14: Lumped-Element Periodically Loaded Transmission Line Model [120]

4.2.2.2.1 Diode Distributed Transmission Line Phase Shifter

PIN diodes and Schottky diodes could be utilised as voltage variable capacitors. Schottky diodes are preferred in high frequency and low loss applications [112]. In [121], a phase shifter implemented using GaAs Schottky diode has been presented, as demonstrated in Figure 4.15. In this configuration, a transmission line is periodically loaded with Schottky varactor diodes. By controlling the DC bias, the varactor capacitance across the diode is changed, which varies the phase velocity and generates the phase shift.

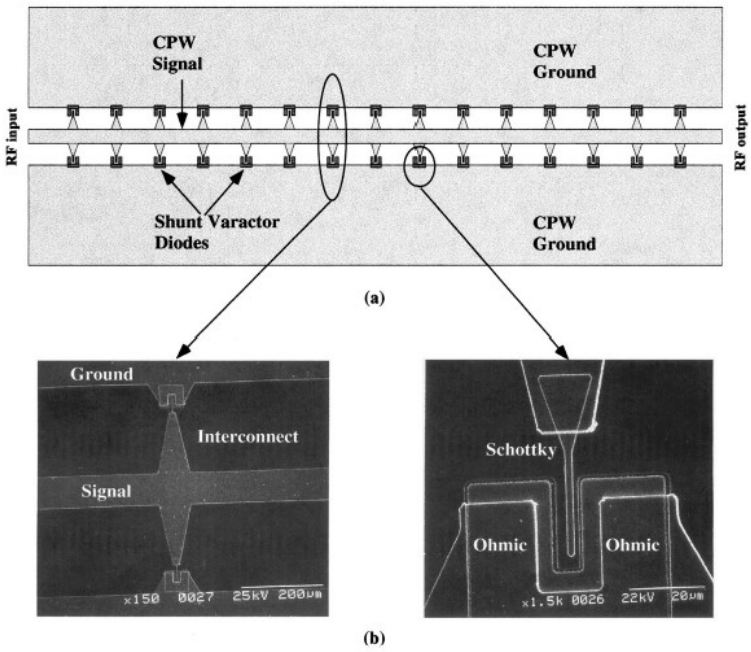


Figure 4.15: (a) Schematic of the Schottky Diode Varactor Loaded CPW Transmission Line (b) SEM Photographs of the Fabricated Phase Shifter [121]

4.2.2.2.2 Barium Strontium Titanate Distributed Transmission Line Phase Shifter

Barium strontium titanate (BST) is a nonlinear ferroelectric material and its permittivity is a function of the DC bias. BST Distributed transmission line phase shifter could be implemented either with parallel plate capacitors or inter-digital capacitors. Figure 4.16 presents the phase shifter implemented with BST tunable parallel plate capacitors periodically loaded on the transmission line [122]. Figure 4.17 illustrates the phase shifter implemented with inter-digital capacitors [123]. By changing the capacitance value of the loading BST capacitors, the phase velocity and phase shift can be controlled.

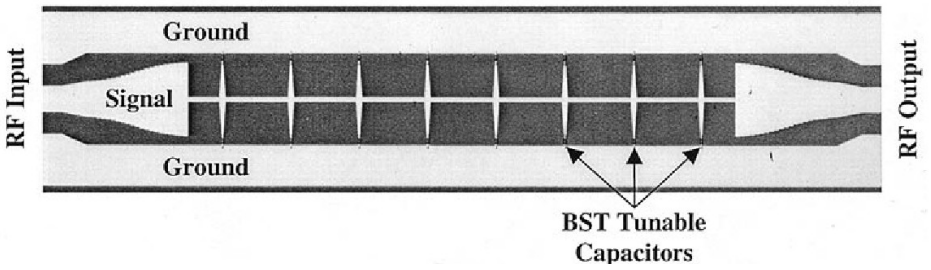


Figure 4.16: Fabricated Distributed Transmission Line Phase Shifter Using BST Parallel Plate Capacitor [122]

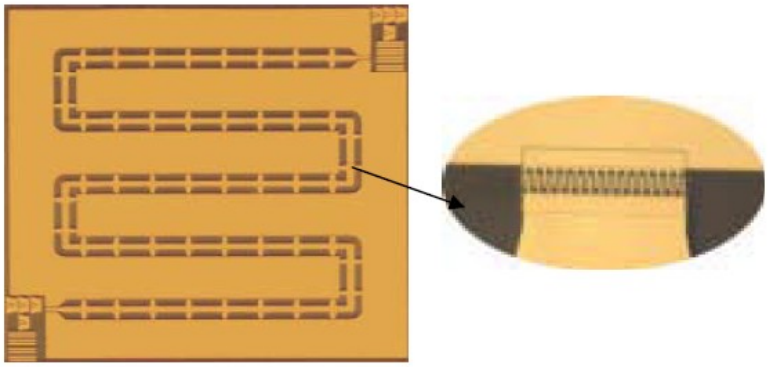


Figure 4.17: Fabricated Distributed Transmission Line Phase Shifter Using BST Inter-Digital Capacitor [123]

4.2.2.2.3 Distributed MEMS Transmission Line Phase Shifter

Distributed MEMS transmission line phase shifters are implemented with periodic distributed MEMS varactors on the transmission line, as illustrated in Figure 4.18 [112].

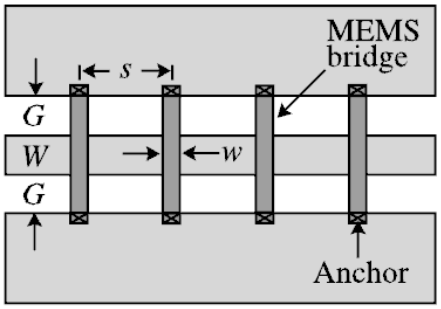
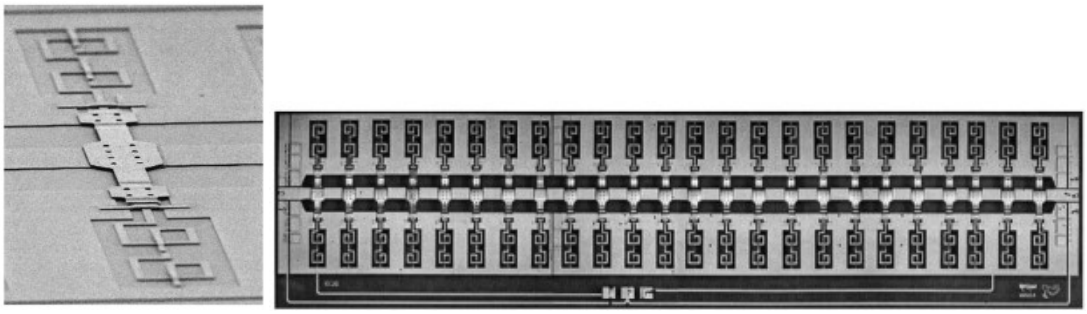


Figure 4.18: Distributed MEMS Transmission Line Phase Shifter [112]

Distributed MEMS transmission line phase shifters are mainly configured on CPW transmission lines due to ease in mounting the shunt MEMS bridges, because the signal and ground tracks are on the same plane of the substrate. Each MEMS varactor has the configuration similar to the MEMS switch structure presented in Figure 4.10, but is not

actuated by snapping down. By applying a bias voltage to the MEMS varactors, proper phase shift will be achieved.

Distributed MEMS transmission line phase shifters are usually fabricated using micro-machining. Distributed MEMS transmission line phase shifters on quartz and silicon substrates are demonstrated in [124] and [125], respectively (as illustrated in Figure 4.19 and Figure 4.20).



(a) **(b)**

Figure 4.19: (a) Photograph of the Unit Cell of a Phase Shifter with MEMS Bridge (b) Photograph of the Fabricated MEMS Phase Shifter, on Quartz Substrate [124]

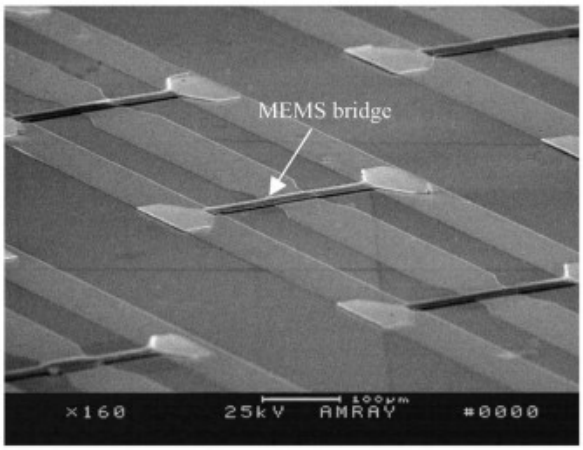


Figure 4.20: SEM Photograph of the Fabricated Phase Shifter on Silicon Substrate

The actuation voltage of MEMS varactor is higher than the bias voltage for semiconductor devices. Different technologies can be used to reduce the actuation voltage, such as changing the beam configurations to cantilever, longer fixed-fixed geometry and meandered structure. The cantilever can realise the air bridges, but its fabrication reliability is low, as it is only fixed on one end. The both ends are fixed at the fixed-fixed beam structure. Meandered beam configuration is able to even decrease the actuation voltage of the fixed-fixed beam design, as presented in Figure 4.21 [126].

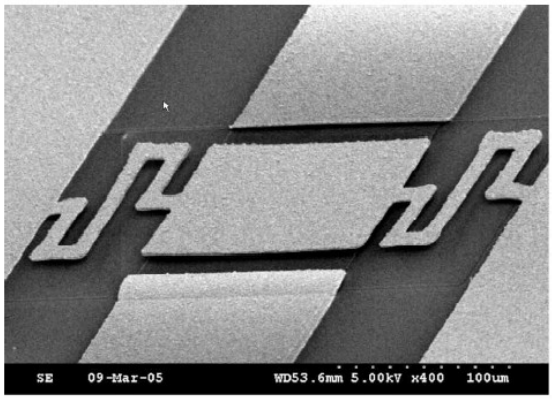


Figure 4.21: SEM Photograph of the Fabricated MEMS Device with Meander-Hinge Switches [126]

Distributed MEMS transmission line phase shifters are operated under the pull-in voltage. Pull-in phenomenon appears around 2/3rd of the total air gap. The tuning ratio for fixed-fixed beam phase shifter is around 1.5. There are several researches to increase the tuning ratio, such as in [116], a two-levelled bridge structure is being used.

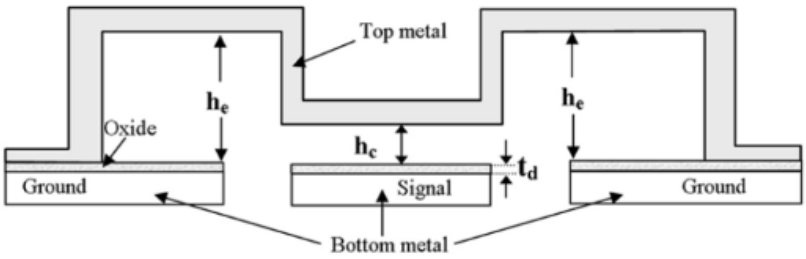


Figure 4.22: High Tuning Two-Levelled Bridge Capacitor Profile [116]

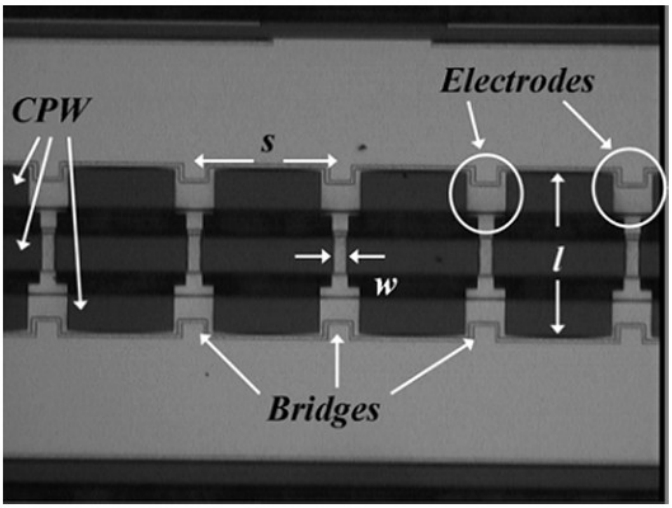


Figure 4.23: Photograph of the Fabricated Phase Shifter [116]

Based on the above phase shifter researches, a high accuracy and low loss analogue phase shifter from Hittite Microwave Corporation has been chosen and fully evaluated for the smart antenna array system. Detailed description and the fully characterisations will be presented in the following section.

4.3 Hittite Analogue Phase Shifter Evaluation

4.3.1 Hittite Analogue Phase Shifter Description

In the smart antenna array, analogue phase shifter HMC928LP5E, which is from Hittite Microwave Corporation [127], has been utilised between the 1:4 UWB feeding network and the planar monopole antennas, in order to provide suitable phase excitations. The high accuracy HMC928LP5E is a monolithic microwave integrated circuit (MMIC) analogue phase shifter which is controlled via an analogue voltage from 0 to 13V, providing a continuously variable phase shift of 0° to 450° from 2 to 4GHz with extremely consistent low insertion loss and proper return loss. The HMC928LP5E phase shifter is monotonic with respect to control voltage and features a typical low phase error of ±5 degrees over the wide bandwidth. The analogue phase shifter is useful for EW receiver, military radar, satellite communication and beamforming modules. The HMC928LP5E is housed in a RoHS compliant 5x5 mm QFN leadless package. Figure 4.24 shows the functional diagram of the HMC928LP5E MMIC analogue phase shifter.

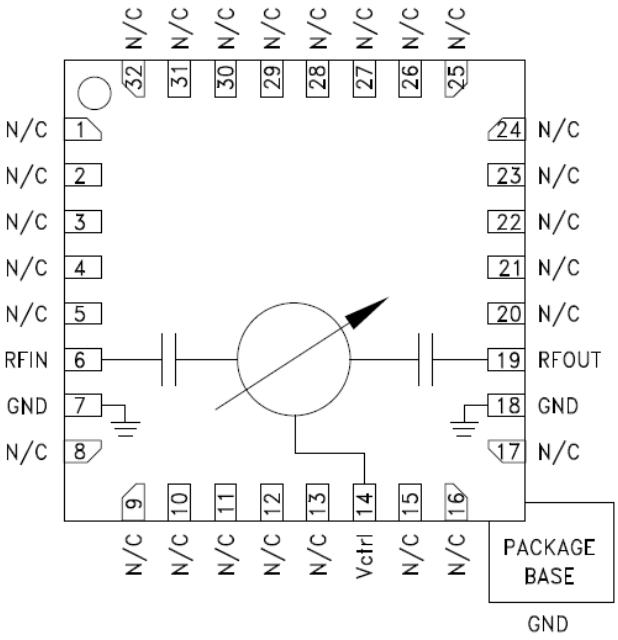


Figure 4.24: HMC928LP5E MMIC Analogue Phase Shifter Functional Diagram [127]

In the HMC928LP5E analogue phase shifter package, Pin 6 and Pin 19 are the input and output of the RF signal. Both of the RF ports have been DC blocked, which confirms the DC voltage will not affect the RF performance, as illustrated in Figure 4.25(a). Pin 7 and Pin 8 are the ground connections of the chip. Backside of the package has exposed metal ground slug that also should be connected to the RF ground thru a short path. Vias under the device have been utilised. Pin 14 is the voltage control. Application of a voltage between 0 and 13 volts causes the transmission phase to change. The DC equivalent circuit is a series connected diode and resistor, as shown in Figure 4.25(d) [127].

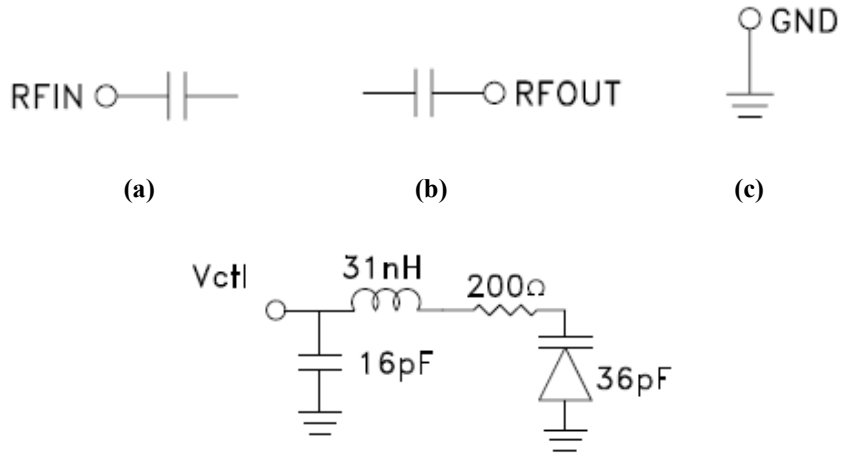


Figure 4.25: Interface Schematic of the Pins of HMC928LP5E MMIC Analogue Phase Shifter (a).RFIN (b).RFOUT (c).GND (d).Control Voltage

Figure 4.26 and Figure 4.27 demonstrates the measured return loss of the HMC928LP5E analogue phase shifter at the input and output, respectively. It is clear that the phase shifter generates suitable return loss across 1.5GHz to 4.5GHz.

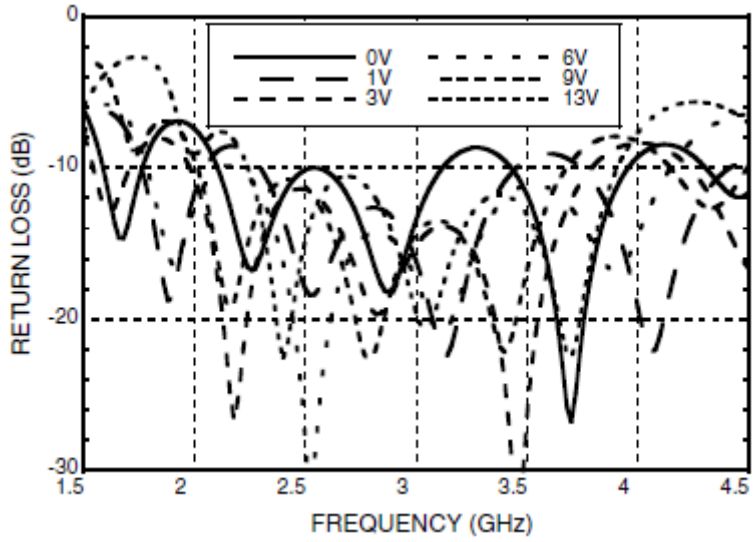


Figure 4.26: Input Return Loss of the HMC928LP5E MMIC Analogue Phase Shifter, for Vctl=0-13V [127]

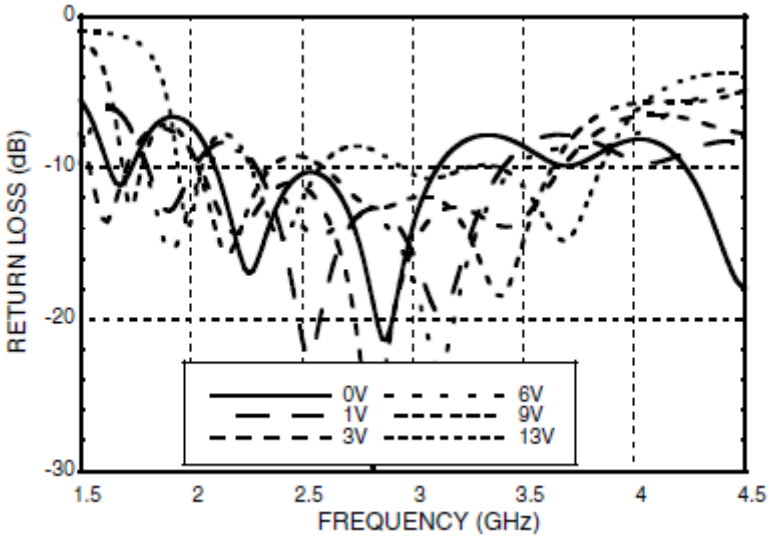


Figure 4.27: Output Return Loss of the HMC928LP5E MMIC Analogue Phase Shifter, for Vctl=0-13V [127]

The measured insertion loss of the phase shifter is presented in Figure 4.28. From 2GHz to 4GHz, the insertion loss is between 3 to 4 dB. Figure 4.29 illustrates the measured phase shift vs. operating frequency at various control voltages.

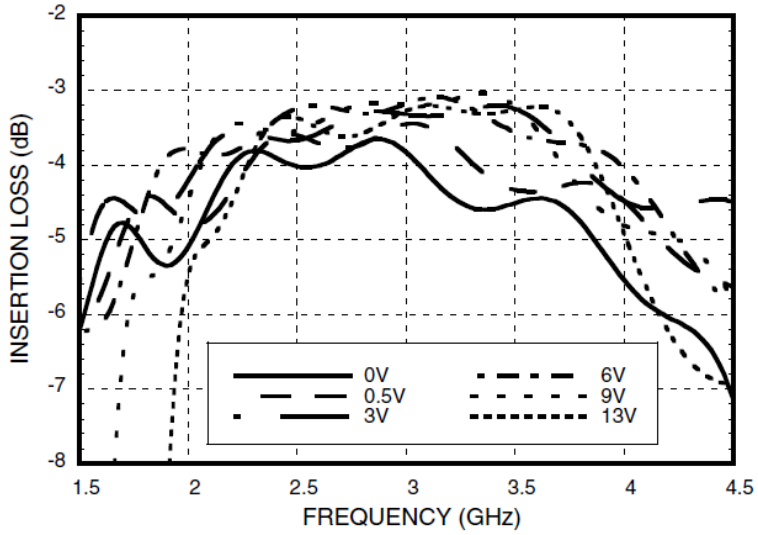


Figure 4.28: Insertion Loss of the HMC928LP5E MMIC Analogue Phase Shifter, for Vctl=0-13V [127]

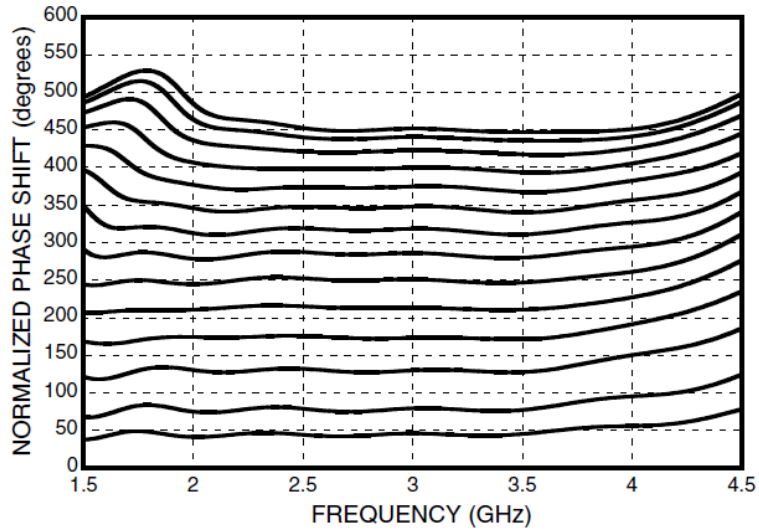


Figure 4.29: Phase Shift vs. Frequency, for Vctl = 0-13V [127]

4.3.2 Hittite Analogue Phase Shifter Characterisation

The manufacture provides an evaluation PCB design in order to test the HMC928LP5E MMIC Analogue Phase Shifter, as shown in Figure 4.30.

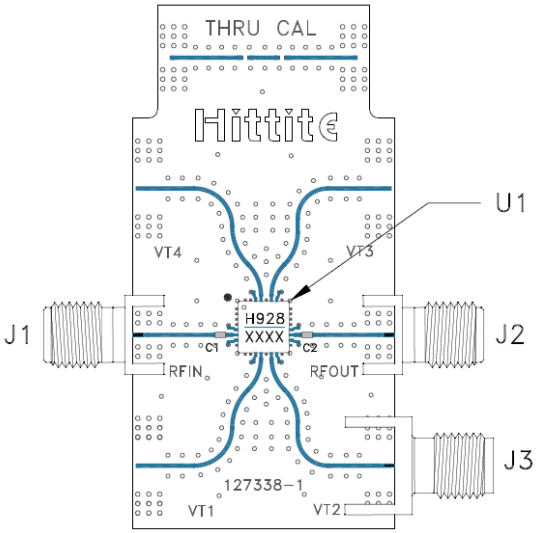
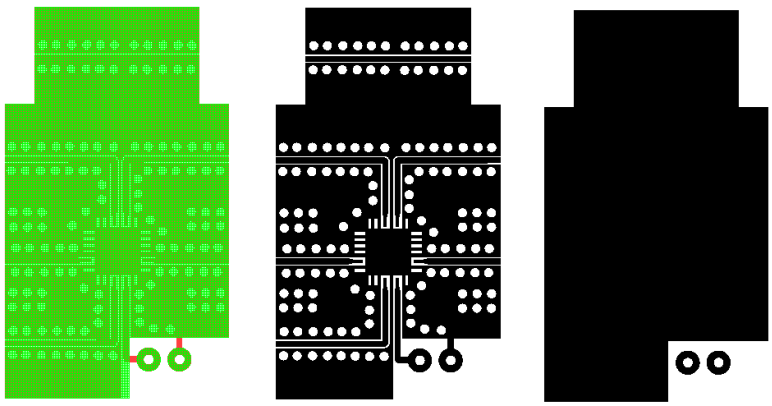


Figure 4.30: HMC928LP5E MMIC Analogue Phase Shifter Evaluation PCB [127]

Where, J1 to J3 are PCB mounted SMA connectors and U1 is the HMC928LP5E MMIC analogue phase shifter. The evaluation board in this application should use RF circuit design techniques. The signal transmission lines are 50 ohm impedance while the package ground leads and exposed paddle are connected directly to the ground plane. A sufficient number of via holes are applied in order to connect the top and bottom ground planes. Based on the design guide, an evaluation PCB using copper and FR4 substrate has been design, simulated, fabricated and characterised.



(a) **(b)** **(c)**

Figure 4.31: (a) Standard Evaluation PCB for HMC928LP5E MMIC Analogue Phase Shifter (b) Top Layer (c) Bottom Layer

In this implementation, copper transmission lines with a conductivity of 5.89×10^7 was etched on an FR4 printed circuit board (with a thickness h=1.6mm and relative dielectric constant, ε_r=4.55). All of the transmission line dimensions have been calculated using the formulas provided in Chapter 3. Finally, the evaluation board configuration has been optimised to achieve suitable S-Parameters. The input and output impedance of the transmission lines are calculated, in order to obtain the 50 ohm impedance matching.

This standard evaluation board has been fabricated and fully tested with a phase shifter. Figure 4.32 presents the manufactured and assembled layout. Dimension of the implemented layout is 18.5mm × 32mm.

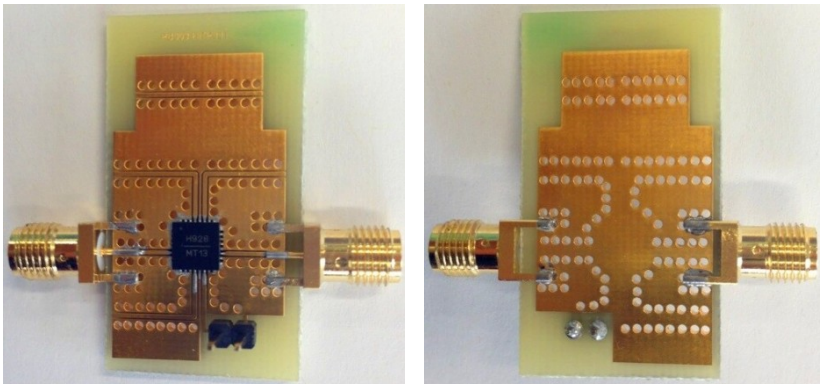


Figure 4.32: Photo of the Fabricated Standard Evaluation PCB for HMC928LP5E MMIC Analogue Phase Shifter: Front View and Back View

The proposed standard evaluation PCB has been subsequently characterised with an HP8753C vector network analyser (VNA). Short-Open-Load-Through (SLOT) calibration was done in order to improve measurement accuracy. Two digital power supplies are used to generate the DC control voltage to the analogue phase shifters, as shown in Figure 4.33. Table 4.1 and Table 4.2 summarise the measured S-Parameters in magnitude and phase format for 2.45GHz and 2.6GHz, respectively.

Figure 4.33: Digital Power Supply to Control the Analogue Phase Shifter

Table 4.1: Measured S-Parameters of the Standard Phase Shifter Evaluation PCB at 2.45GHz

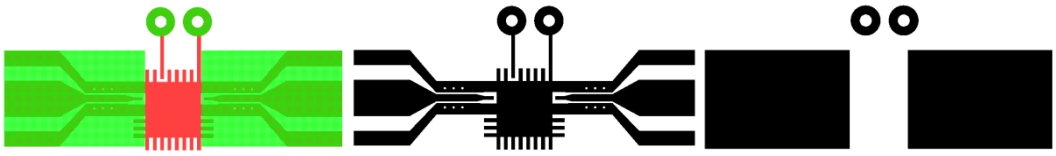
	Control Voltage: 0V	**Control Voltage: 3.16V**	**Control Voltage:7.93V**
S_{11}(Magnitude)	-12.43dB	-13.91dB	-15.12dB
S_{11}(Phase)	151.26°	162°	137.73°
S_{21}(Magnitude)	-3.38dB	-3.21dB	-3.10dB
S_{21}(Phase)	-91.1°	88.86°	-91.55°
S_{22}(Magnitude)	-13.45dB	-13.56dB	-15.01dB
S_{22}(Phase)	130.64°	122.89°	161.81°

Table 4.2: Measured S-Parameters of the Standard Phase Shifter Evaluation PCB at 2.6GHz

	Control Voltage: 0V	**Control Voltage: 3.12V**	**Control Voltage:7.89V**
S_{11}(Magnitude)	-13.42dB	-14.87dB	-15.01dB
S_{11}(Phase)	122.21°	137.31°	103.15°
S_{21}(Magnitude)	-3.36dB	-3.25dB	-3.12dB
S_{21}(Phase)	-118.51°	61.4°	-118.53°
S_{22}(Magnitude)	-14.21dB	-15.02dB	-15.12dB
S_{22}(Phase)	105.26°	100.27°	130.11°

It is evident from the measurement results that analogue phase shifter is adequate for both of WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) applications. The reflection coefficients S_{11} are smaller than -10dB and the insertion losses are around 3dB, similar performance as in the datasheet. The higher control voltage will generate high return loss and low insertion loss. The presented structure can achieve 180° phase shift at 3.16V and 3.12V, 360° phase shift at 7.93V and 7.89V, for 2.45GHz and 2.6GHz, respectively.

The HMC928LP5E MMIC analogue phase shifter will be applied in the smart antenna array developed in Chapter 2 and Chapter 3. In order to fully test the device, an improved and simplified evaluation PCB has been designed, to simulate the phase shifter performance in an antenna array, as illustrated in Figure 4.34.



(a) **(b)** **(c)**

Figure 4.34: (a) Modified Evaluation PCB for HMC928LP5E MMIC Analogue Phase Shifter (b) Top Layer (c) Bottom Layer

Compared to the standard evaluation PCB structure, the layout has been simplified and miniaturised. The calibration part has been removed and the phase shifter is directly connected to two SMA connectors. Two voltage control pins are near the chip and a significant number of vias are used in order to combine the top and bottom ground planes. Later the UWB feeding network and antenna elements will be placed at two sides of the analogue phase shifter. There is a slot cut on the backside of the evaluation PCB, for the purpose of placing the voltage control line. This modified evaluation PCB has exactly the same configuration as later in the smart antenna array, so it is able to fully estimate the phase shift and RF performance. The proposed structure has also been fabricated and measured, as shown in Figure 4.35. Dimension of the implemented layout is 9.5mm × 23mm. Table 4.3 and Table 4.4 present the measured S-Parameters in magnitude and phase format for 2.45GHz and 2.6GHz, respectively.

Figure 4.35: Photo of the Fabricated Modified Evaluation PCB for HMC928LP5E MMIC Analogue Phase Shifter: Top View and Back View

Table 4.3: Measured S-Parameters of the Modified Phase Shifter Evaluation PCB at 2.45GHz

	Control Voltage: 0V	**Control Voltage: 3.64V**	**Control Voltage:8.22V**
S_{11}(Magnitude)	-12.82dB	-14.14dB	-15.02dB
S_{11}(Phase)	112.27°	162°	160.15°
S_{21}(Magnitude)	-3.32dB	-3.21dB	-3.17dB
S_{21}(Phase)	-107.52°	72.48°	-107.13°
S_{22}(Magnitude)	-12.98dB	-14.98dB	-15.13dB
S_{22}(Phase)	114.03°	151.61°	152.22°

Table 4.4: Measured S-Parameters of the Modified Phase Shifter Evaluation PCB at 2.6GHz

	Control Voltage: 0V	**Control Voltage: 3.59V**	**Control Voltage:8.11V**
S_{11}(Magnitude)	-13.01dB	-14.45dB	-15.06dB
S_{11}(Phase)	89.12°	132.13°	130.56°
S_{21}(Magnitude)	-3.28dB	-3.18dB	-3.11dB
S_{21}(Phase)	-121.51°	58.49°	-121.49°
S_{22}(Magnitude)	-13.43dB	-14.78dB	-15.65dB
S_{22}(Phase)	90.12°	123.22°	121.03°

It is clear that the modified evaluation PCB demonstrates suitable S-Parameters and phase shift for both of WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) standards. This HMC928LP5E analogue phase shifter obtains 180° phase shift at 3.64V and 3.59V, 360° phase shift at 8.22V and 8.11V, with high return loss (10dB) and low insertion loss (3dB), at 2.45GHz and 2.6GHz, respectively. The proposed analogue phase shifter is adequate for the smart antenna array implementation.

4.4 UWB CPW-to-Microstrip Transition Structure

The phase shifter is developed for RF applications and the manufacturer recommends connecting the device utilising coplanar waveguide (CPW), for the purpose of 50Ω impedance matching [127].

The UWB feeding network and monopole antennas are both microstrip structures. In order to connect the phase shifter, two UWB CPW-to-Microstrip transitions have been developed, which obtain smooth field transformation and impedance matching.

4.4.1 Field Matching

In a microstrip configuration, the electric field lines are mainly vertical as terminating perpendicularly at the ground of the substrate, as illustrated in Figure 4.36(a). In a CPW, the electric field lines are generally horizontal and concentrated between the signal track and two ground strips, as depicted in Figure 4.36(b). In order to gradually match the field distributions between the microstrip and CPW, a conductor backed coplanar waveguide (CBCPW) has been intervened (as shown in Figure 4.36(c)). Furthermore, a ground-shaped conductor backed coplanar waveguide structure has also been developed, where the electric field lines change to those of the CPW as the signal propagates along the transition (as illustrated in Figure 4.36(d)) [128]. The proposed UWB Microstrip-to-CPW transitions are based on the CBCPW geometry.

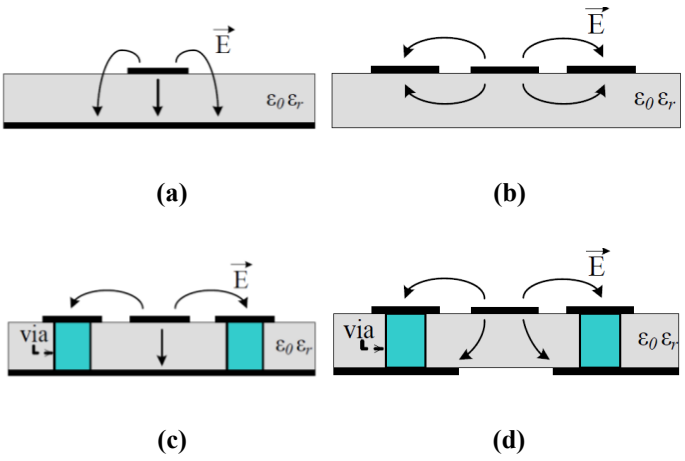
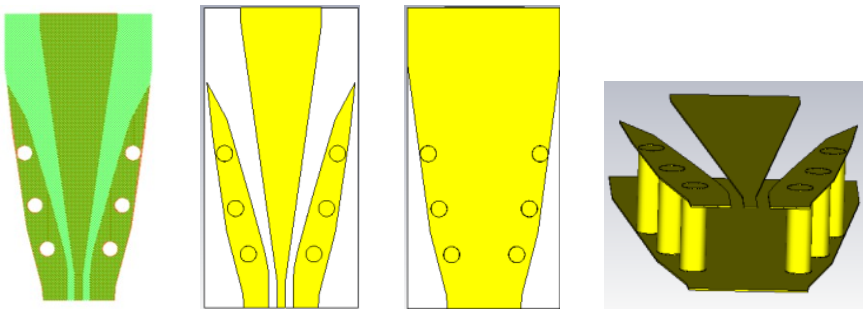


Figure 4.36: Electric Field Lines at Each Cross-Section along the Transitions [128]

4.4.2 Impedance Matching

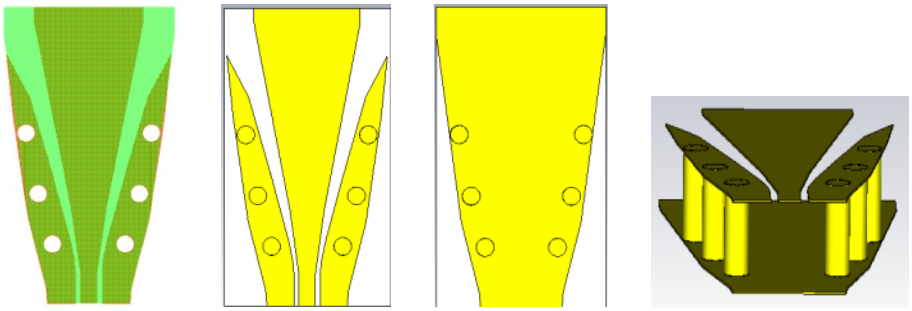
Because the characteristic impedance of a CPW with actual fabrication limitations or with the required signal-to-ground separations could be different from that of the microstrip structure, the transition should be able to match the impedance differences between the two transmission lines. As for the antenna array copper tracks were etched on 1.6mm FR4 printed circuit board material. Because of its relatively low dielectric constant (εr=4.55), the actual characteristic impedance of the CPW is usually greater than that of the microstrip line. As the ground gap of the transition becomes narrower, the capacitance of the transmission line is greater, and so the transition impedance becomes lower, finally reaching to that of microstrip. The impedance calculation was performed by utilising CST Microwave Studio.

For the purpose of optimally matching the impedances between two transmission lines, a Klopfenstein taper [37] has been applied. The Klopfenstein taper length is miniaturised to reduce the mismatch at the lowest operating frequency. With the transition length of 7.3mm and the maximum reflection coefficient Γ_m for the taper should be around 0.02. If better impedance matching is needed at lower frequencies, the length of the transition should be extended. The tapered transition shape is synthesised with the desired impedance variation, and the implemented layouts are demonstrated in Figure 4.37 and Figure 4.38. Since the width of the UWB feed network and the feed of the monopole antenna are slight different, two kinds of UWB transition configurations are required. Figure 4.37 presents the transition between the feeding network and phase shifter (Transition I), while Figure 4.38 shows the transition structure between the phase shifter and monopole antenna (Transition II).



(a) **(b)** **(c)** **(d)**

Figure 4.37: (a) Proposed UWB Transition between the Feeding Network and Phase Shifter (Transition I) (b) Top Layer (c) Bottom Layer (d) Side View



(a) **(b)** **(c)** **(d)**

Figure 4.38: (a) Proposed UWB Transition between Phase Shifter and Monopole Antenna (Transition II) (b) Top Layer (c) Bottom Layer (d) Side View

To prevent radiation from the grounded CPW into substrate modes, it is required to add via holes at a distance less than λ_{eff}, where λ_{eff} stands for the effective wavelength of the odd transmission line mode [129]. In this implementation, via holes are placed at both transition wings for the purpose of providing the ground continuity. In the proposed transition, three via holes are placed at each transition wing to achieve good performances up to 9GHz. Both of the UWB transition configurations have been designed, simulated and optimised in CST Microwave Studio. Figure 4.39 and Figure 4.40 present the simulated S-Parameters, which confirm the designs are suitable for WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) applications.

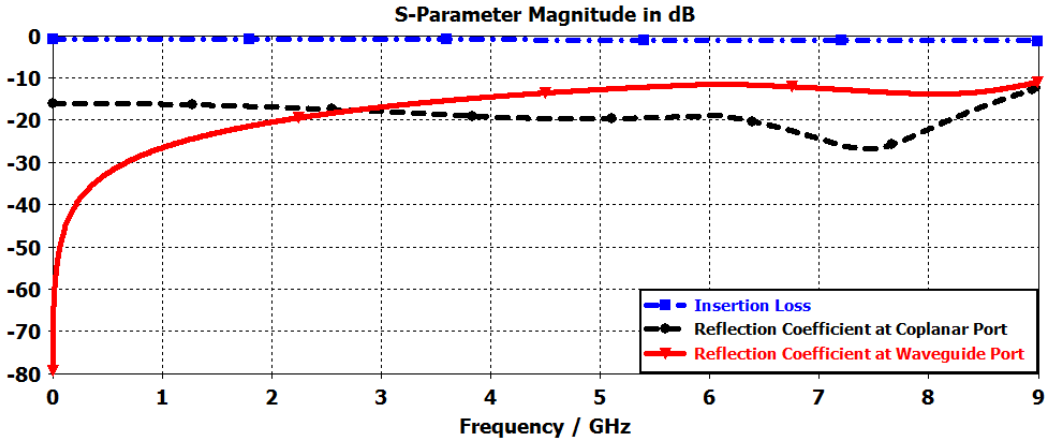


Figure 4.39: Simulated S-Parameters (Magnitude) of the Proposed UWB Transition between the Feeding Network and Phase Shifter (Transition I)

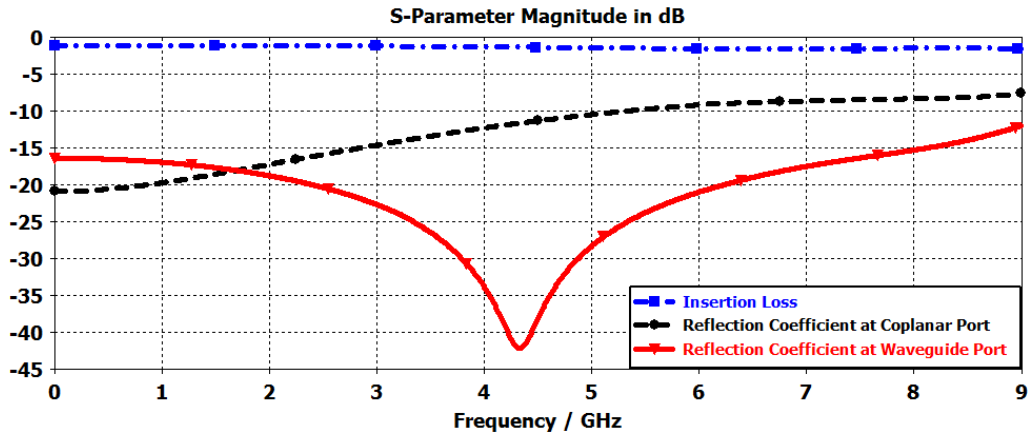
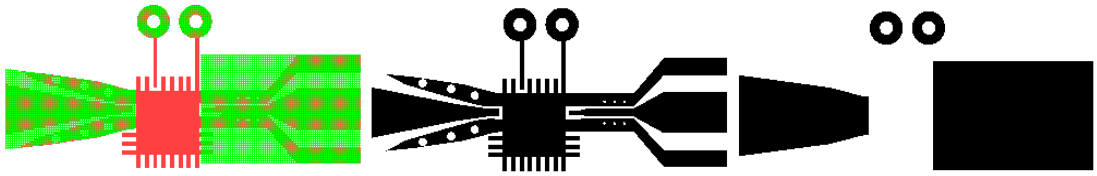


Figure 4.40: Simulated S-Parameters (Magnitude) of the Proposed UWB Transition between the Phase Shifter and Monopole Antenna (Transition II)

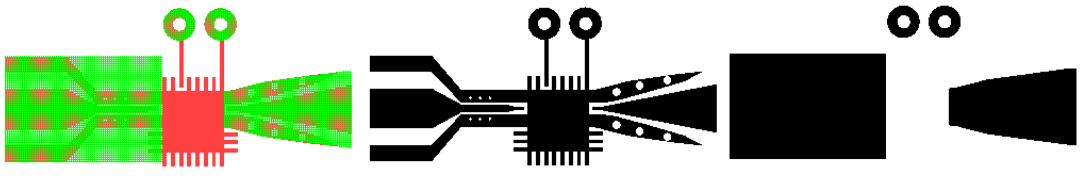
4.4.3 UWB CPW-to-Microstrip Transition Characterisation

There are two transition designs for the smart antenna array: Transition I between the feeding network and phase shifter and Transition II between the phase shifter and monopole antenna. The two configurations have been fabricated and evaluated separately. Figure 4.41 and Figure 4.42 present the evaluation board structures to test the Transition I and Transition II, respectively. In the evaluation PCB design, the phase shifter is placed in the middle, only one transition is connected and the other side is using standard CPW transmission line.



(a) **(b)** **(c)**

Figure 4.41: (a) Geometry of the Evaluation PCB for Testing the Transition between the Feeding Network and Phase Shifter (Transition I) (b) Top Layer (c) Bottom Layer



(a) **(b)** **(c)**

Figure 4.42: (a) Geometry of the Evaluation PCB for Testing the Transition between the Phase Shifter and Monopole Antenna (Transition II) (b) Top Layer (c) Bottom Layer

The two evaluation PCBs have been fabricated, assembled and fully characterised with an HP8753C vector network analyser (VNA) (as illustrated in Figure 4.43 and Figure 4.44). Table 4.5 and Table 4.6 demonstrate the measured S-Parameters in magnitude and phase at 2.45GHz and 2.6GHz for Transition I. Table 4.7 and Table 4.8 show the measured S-Parameters for Transition II.

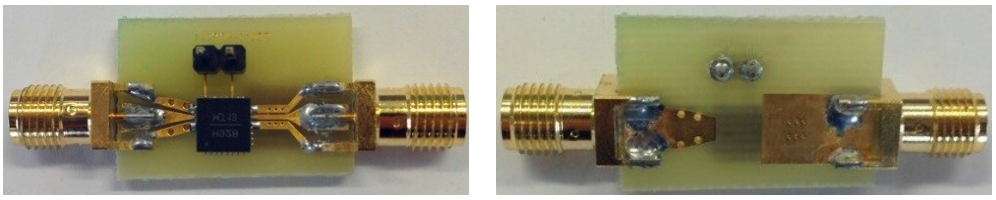


Figure 4.43: Photo of the Fabricated Evaluation PCB for Testing the Transition between the Feeding Network and Phase Shifter (Transition I): Top View and Back View

Table 4.5: Measured S-Parameters of the Fabricated Evaluation PCB for Testing the Transition between the Feeding Network and Phase Shifter at 2.45GHz

	Control Voltage: 0V	**Control Voltage: 3.39V**	**Control Voltage:7.96V**
S_{11}(Magnitude)	-12.68dB	-13.03dB	-14.06dB
S_{11}(Phase)	138.31°	145.27°	178.12°
S_{21}(Magnitude)	-3.32dB	-3.22dB	-3.17dB
S_{21}(Phase)	-95.35°	84.65°	-95.49°
S_{22}(Magnitude)	-12.78dB	-13.18dB	-14.11dB
S_{22}(Phase)	134.87°	135.32°	160.59°

Table 4.6: Measured S-Parameters of the Fabricated Evaluation PCB for Testing the Transition between the Feeding Network and Phase Shifter at 2.6GHz

	Control Voltage: 0V	**Control Voltage: 3.31V**	**Control Voltage:7.88V**
S_{11}(Magnitude)	-12.88dB	-13.45dB	-14.24dB
S_{11}(Phase)	105.18°	112.18°	153.77°
S_{21}(Magnitude)	-3.25dB	-3.15dB	-3.11dB
S_{21}(Phase)	-113.32°	66.68°	-113.49°
S_{22}(Magnitude)	-13.43dB	-13.78dB	-15.05dB
S_{22}(Phase)	100.12°	105.25°	147.03°

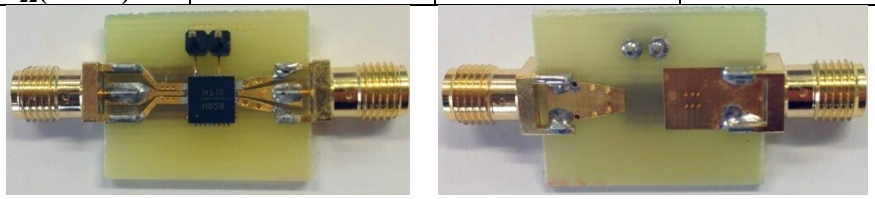


Figure 4.44: Photo of the Fabricated Evaluation PCB for Testing the Transition between the Phase Shifter and Monopole Antenna (Transition II): Top View and Bottom View

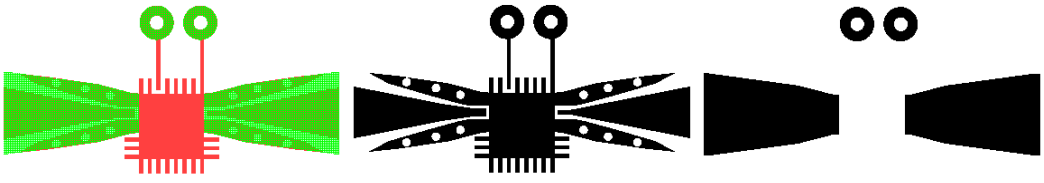
Table 4.7: Measured S-Parameters of the Fabricated Evaluation PCB for Testing the Transition between the Phase Shifter and Monopole Antenna at 2.45GHz

	Control Voltage: 0V	**Control Voltage: 3.22V**	**Control Voltage:7.93V**
S_{11}(Magnitude)	-12.64dB	-13.06dB	-14.26dB
S_{11}(Phase)	118.59°	125.91°	167.02°
S_{21}(Magnitude)	-3.36dB	-3.19dB	-3.15dB
S_{21}(Phase)	-94.78°	85.22°	-94.79°
S_{22}(Magnitude)	-12.78dB	-13.05dB	-14.16dB
S_{22}(Phase)	113.41°	129.61°	169.22°

Table 4.8: Measured S-Parameters of the Fabricated Evaluation PCB for Testing the Transition between the Phase Shifter and Monopole Antenna at 2.6GHz

	Control Voltage: 0V	**Control Voltage: 3.18V**	**Control Voltage:7.88V**
S_{11}(Magnitude)	-13.21dB	-14.05dB	-14.46dB
S_{11}(Phase)	90.17°	105.77°	141.06°
S_{21}(Magnitude)	-3.29dB	-3.15dB	-3.11dB
S_{21}(Phase)	-112.11°	67.89°	-112.19°
S_{22}(Magnitude)	-13.23dB	-14.18dB	-15.05dB
S_{22}(Phase)	88.14°	101.23°	137.03°

It is clear from the measurement results that the both transition structures achieve good S-Parameters and accurate 180º and 360º phase shifts for 2.45GHz and 2.6GHz, respectively. Finally an analogue phase shifter has been connected between the two UWB CPW-to-microstrip transitions. The design and fabricated layout are presented in Figure 4.45 and Figure 4.46.



(a) **(b)** **(c)**

Figure 4.45: (a) Geometry of the Evaluation PCB for Testing the Two Transitions (b) Top Layer (c) Bottom Layer

Figure 4.46: Photo of the Fabricated Evaluation PCB for Testing the Two Transitions: Top View and Bottom View

The measured results of the phase shifter integrated with the two UWB transitions at 2.45GHz and 2.6GHz are summarised in Table 4.9 and Table 4.10, respectively.

Table 4.9: Measured S-Parameters of the Fabricated Evaluation PCB for Testing the Two Transitions at 2.45GHz

	Control Voltage: 0V	**Control Voltage: 3.01V**	**Control Voltage:7.73V**
S_{11}(Magnitude)	-14.78dB	-15.11dB	-16.01dB
S_{11}(Phase)	142.09°	144.23°	173.47°
S_{21}(Magnitude)	-3.18dB	-3.15dB	-3.12dB
S_{21}(Phase)	-87.16°	92.84°	-87.16°
S_{22}(Magnitude)	-14.12dB	-14.98dB	-15.01dB
S_{22}(Phase)	138.21°	141.02°	166.45°

Table 4.10: Measured S-Parameters of the Fabricated Evaluation PCB for Testing the Two Transitions at 2.6GHz

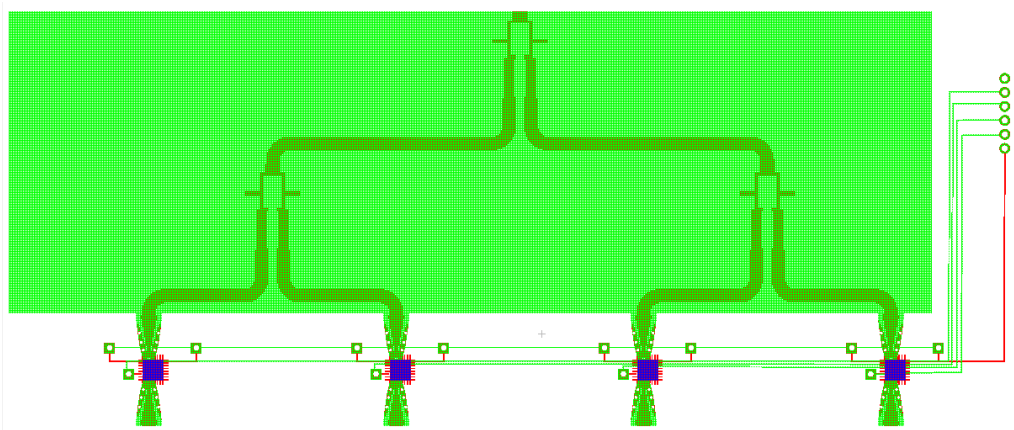
	Control Voltage: 0V	**Control Voltage: 2.98V**	**Control Voltage:7.98V**
S_{11}(Magnitude)	-15.22dB	-15.67dB	-15.98dB
S_{11}(Phase)	111.65°	117.34°	155.65°
S_{21}(Magnitude)	-3.06dB	-2.98dB	-2.90dB
S_{21}(Phase)	-115.43°	64.57°	-115.43°
S_{22}(Magnitude)	-17.34dB	-17.98dB	-18.87dB
S_{22}(Phase)	105.56°	113.54°	149.76°

It is significant to note that the integrated structure achieves suitable reflection coefficients. From the manufacture datasheet [127], the insertion loss of the phase shifter is around 3dB, and the measurements demonstrate a good agreement. The proposed configuration is able to generate 180° phase shift at 3.01V and 2.98V, 360° phase shift at 7.73V and 7.98V, for 2.45GHz and 2.6GHz, respectively.

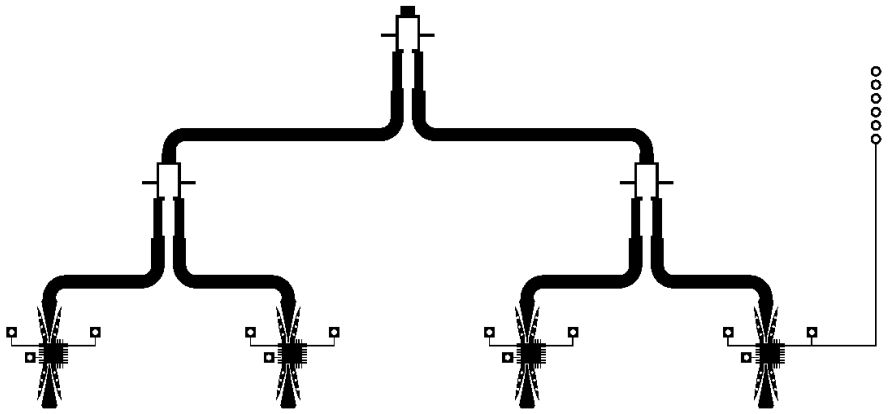
4.5 Smart Antenna Array Implementation

4.5.1 Adaptive 1:4 UWB Feeding Network Integration

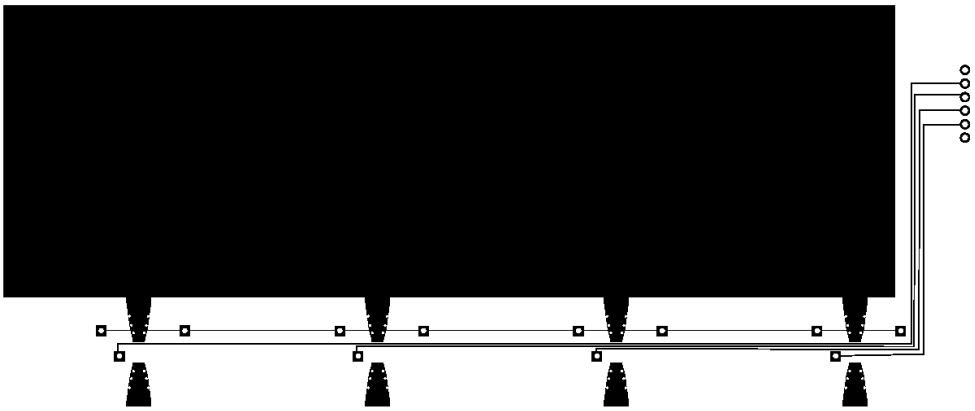
Based on the above analysis, the phase shifters and UWB transitions have been combined with the UWB feeding network. Figure 4.47 presents the fully integrated layout and Figure 4.48 illustrates the fabricated design. The measurement results are demonstrated in Table 4.11 and Table 4.12.



(a)

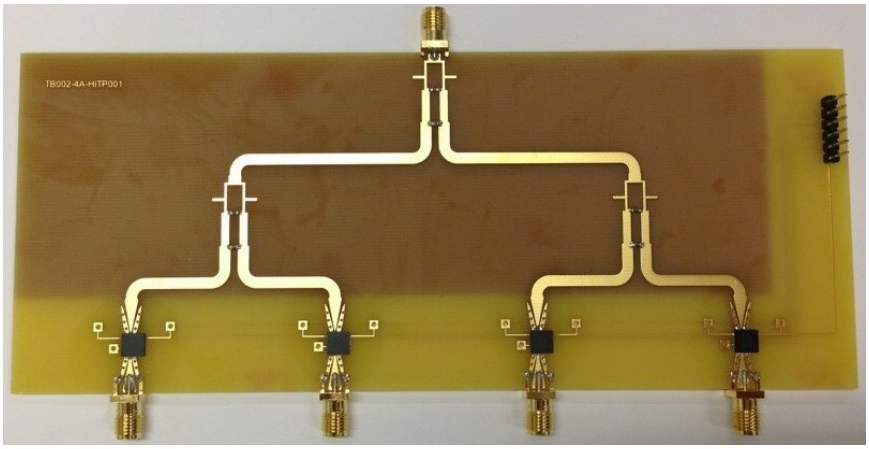


(b)



(c)

Figure 4.47: (a) Geometry of Adaptive 1:4 UWB Feeding Network (b) Top Layer (c) Bottom Layer



(a)

(b)

Figure 4.48: Photo of the Fabricated 1:4 Adaptive UWB Feeding Network: (a) Top View (b) Bottom View

Table 4.11: Measured S-Parameters of the Fabricated 1:4 Adaptive UWB Feeding Network at 2.45GHz

	Control Voltage: 0V	**Control Voltage: 2.79V**	**Control Voltage:7.79V**
S_{11}(Magnitude)	-17.63dB	-17.69dB	-17.72dB
S_{22}(Magnitude)	-16.54dB	-16.57dB	-16.61dB
S_{33}(Magnitude)	-17.14dB	-17.22dB	-17.26dB
S_{44}(Magnitude)	-17.26dB	-17.27dB	-17.32dB
S_{55}(Magnitude)	-17.02dB	-17.23dB	-17.33dB
S_{21} (Magnitude)	-9.52dB	-9.49dB	-9.41dB
S_{21} (Phase)	9.64°	-170.32°	9.72°
S_{31} (Magnitude)	-9.58dB	-9.52dB	-9.49dB
S_{31} (Phase)	10.98°	-167.45°	10.46°
S_{41} (Magnitude)	-9.76dB	-9.65dB	-9.51dB
S_{41} (Phase)	9.59°	-172.63°	9.96°
S_{51} (Magnitude)	-9.57dB	-9.51dB	-9.47dB
S_{51} (Phase)	11.92°	-169.73°	10.74°
S_{23}(Magnitude)	-25.11dB	-25.22dB	-25.32dB
S_{34}(Magnitude)	-28.35dB	-29.01dB	-29.23dB
S_{45}(Magnitude)	-26.22dB	-26.54dB	-26.99dB

Table 4.12: Measured S-Parameters of the Fabricated 1:4 Adaptive UWB Feeding Network at 2.6GHz

	Control Voltage: 0V	**Control Voltage: 2.85V**	**Control Voltage:7.91V**
S_{11}(Magnitude)	-18.23dB	-18.45dB	-18.98dB
S_{22}(Magnitude)	-17.05dB	-17.13dB	-17.35dB
S_{33}(Magnitude)	-17.13dB	-17.42dB	-17.61dB
S_{44}(Magnitude)	-16.98dB	-17.02dB	-17.23dB
S_{55}(Magnitude)	-17.02dB	-17.24dB	-17.56dB
S_{21} (Magnitude)	-9.42dB	-9.41dB	-9.41dB
S_{21} (Phase)	41.34°	-138.65°	41.36°
S_{31} (Magnitude)	-9.49dB	-9.46dB	-9.42dB
S_{31} (Phase)	43.23°	-137.32°	44.73°
S_{41} (Magnitude)	-9.52dB	-9.46dB	-9.44dB
S_{41} (Phase)	42.45°	-138.17°	43.57°
S_{51} (Magnitude)	-9.48dB	-9.46dB	-9.42dB
S_{51} (Phase)	41.52°	-140.73°	42.84°
S_{23}(Magnitude)	-27.15dB	-27.34dB	-27.55dB
S_{34}(Magnitude)	-30.16dB	-30.45dB	-30.81dB
S_{45}(Magnitude)	-28.12dB	-28.56dB	-28.77dB

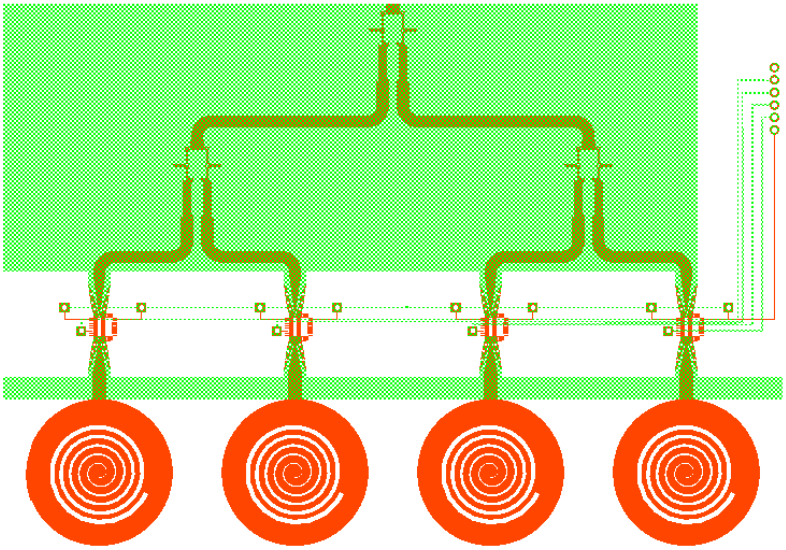
The measured reflection coefficients are similar to the results as in Table 3.7. S_{n1} (Magnitude and Phase) are the only differences, and the measured results have been summarised in the above tables. Based on calculation, the theoretical insertion loss is 6.4dB

for a four ports network. There is another 3dB loss caused by the phase shifter. The measured -9.5dB reveals a good consistency to the calculated -9.4dB. Furthermore, it is clear from the tables that the adaptive 1:4 UWB feeding network demonstrates 180° phase shift at 2.79V and 2.85V, 360° phase shift at 7.79V and 7.91V, for 2.45GHz and 2.6GHz, respectively. The proposed integrated feeding network provides good S-Parameters and generates accurate phase shifts, which is suitable for the smart antenna array implementation.

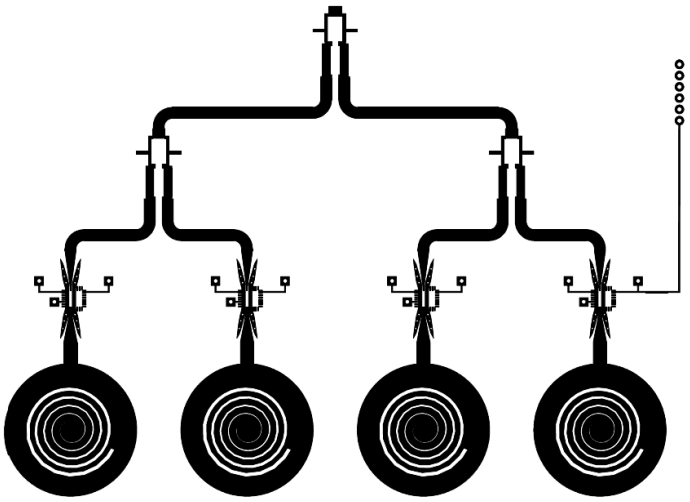
4.5.2 Smart Antenna Array Integration and Characterisation

Based on the above design procedure, the four-element linear antenna array, UWB feeding network, analogue phase shifters and UWB transitions are assembled, in order to establish a complete smart antenna system (as illustrated in Figure 4.49).

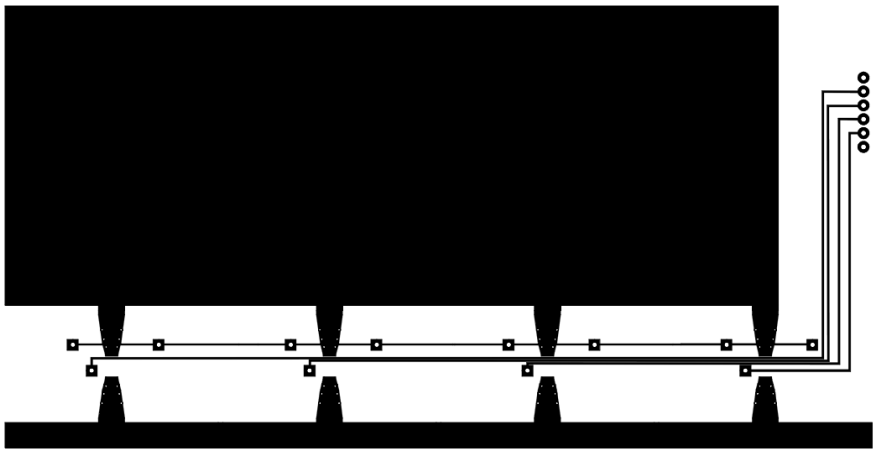
For the finalised smart antenna array system, the radius of the monopole antenna is 15mm and inter-element spacing is 40mm. The physical dimension of the manufactured circuit is 110mm × 155mm. DC bias voltages have been supplied to the analogue phase shifters. Figure 4.51 depicts the measured reflection coefficients of the proposed smart antenna array with different DC bias voltages.



(a)

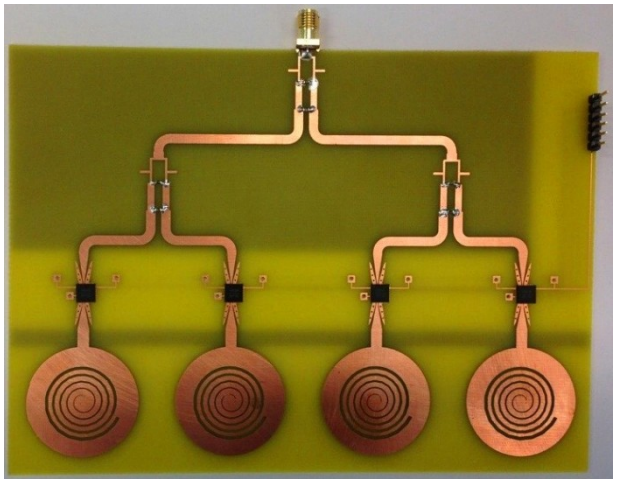


(b)

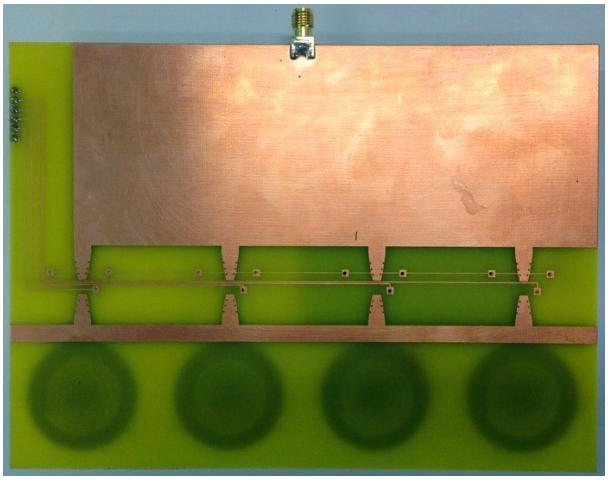


(c)

Figure 4.49: (a) Geometry of the Fully Integrated Smart Antenna Array (b) Top Layer (c) Bottom Layer



(a)



(b)

Figure 4.50: Photo of the Fabricated Smart Antenna Array (a) Top View (b) Bottom View

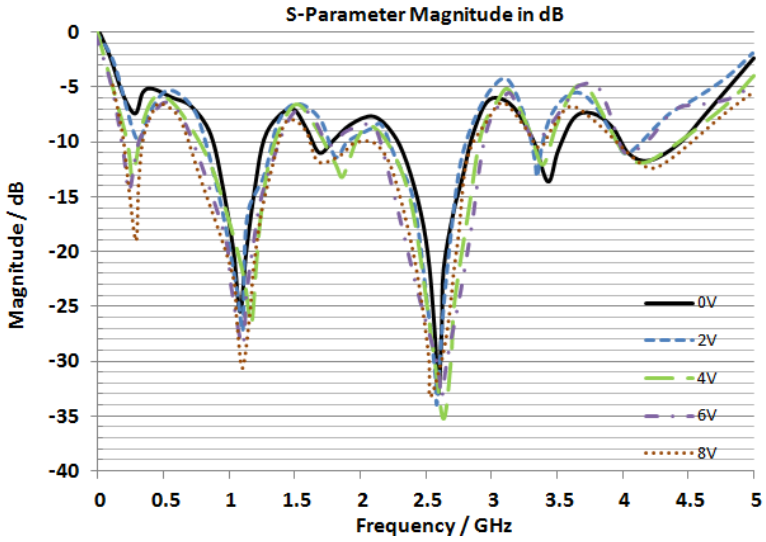


Figure 4.51: Measured Reflection Coefficient of the Proposed Smart Antenna Array with DC Bias 0V, 2V, 4V, 6V and 8V

The proposed smart antenna structure operates from 2.25GHz to 2.8GHz frequency band, covering the WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) standards. After applying the DC bias voltages to the phase shifters, the operating frequency range is even wider. This smart antenna array obtains suitable reflection coefficients.

The radiation pattern measurements were carried out in an anechoic chamber having walls that are covered with RF absorbers, as shown in Figure 2.36 (Chapter 2).

The main beam steering is performed in H-Plane and all of the H-Plane measurement results have been analysed. The measured gain is illustrated in Figure 4.52 and Figure 4.53, for 2.45GHz and 2.6GHz, respectively.

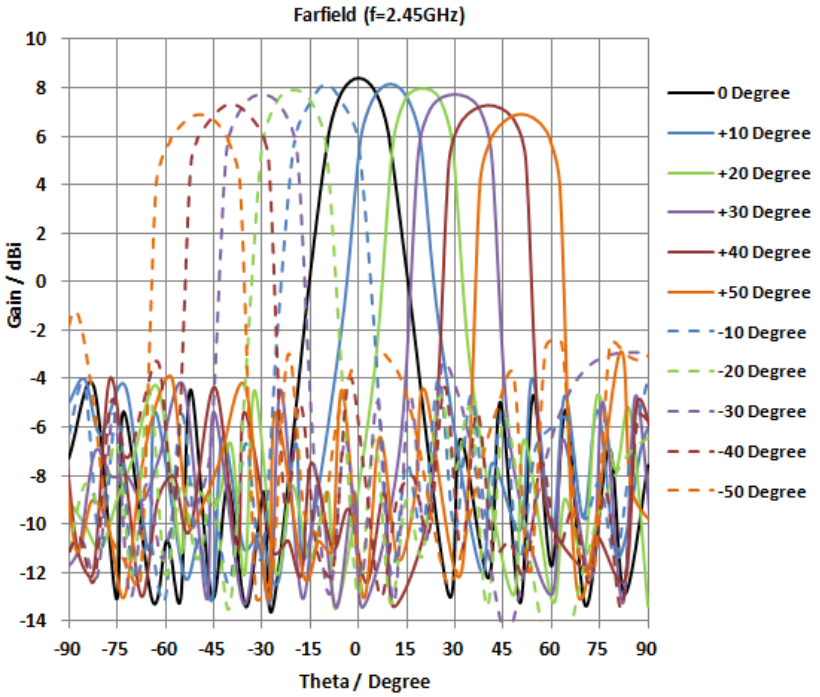


Figure 4.52: Measured Gain vs. Theta in the H-Plane for Different Scanning Angles, at 2.45GHz

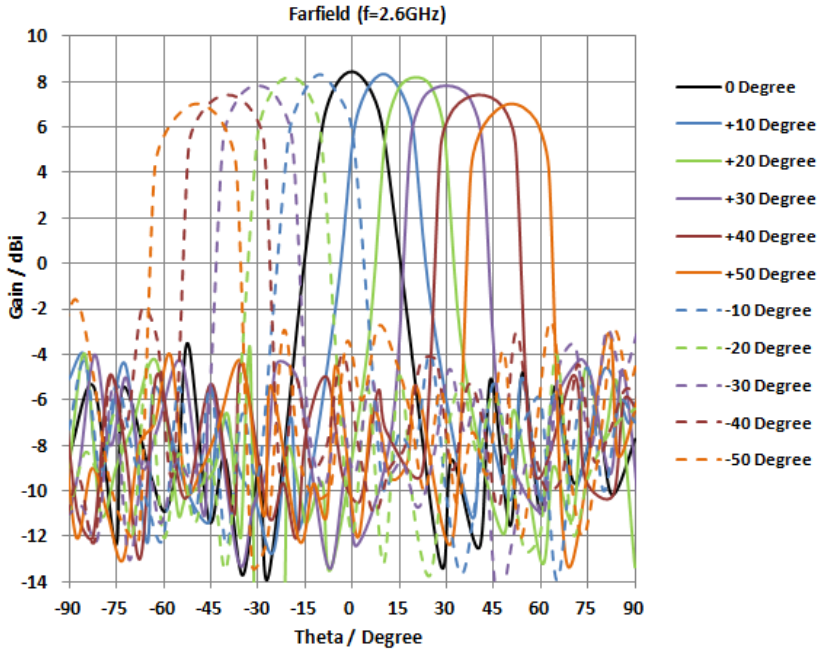


Figure 4.53: Measured Gain vs. Theta in the H-Plane for Different Scanning Angles, at 2.6GHz

Compared to the simulation results (discussed in Chapter 2), the measured gain is reduced by 2.5dB, which is caused by the loss of analogue phase shifters, feeding network and UWB transitions. At 2.45GHz, the smart antenna array is able to steer from -50° to +50°. For 2.6GHz, the scanning range reaches ±52°, while maintaining low side lobes. The smart antenna array demonstrates a gain of 8.5dBi with 40° 3dB bandwidth in broadside direction,

and has more than 10dB side lobe level suppression across the scan. Further work will use MEMS devices integrated into the design to replace the analogue phase shifters. By digitally controlling the DC bias voltages, this smart antenna array could be implemented into mobile devices for reconfigurable applications.

4.6 Summary

This chapter addressed the smart antenna array full integration and characterisation. The antenna array design has been described in Chapter 2 and the UWB feeding network structure was discussed in Chapter 3. This chapter firstly shows all of the different phase shifter developments, which include ferrite phase shifter and planar phase shifter. The planar phase shifter is divided into two sections: switched delay line phase shifter and loaded transmission line phase shifters. Both of the two structures could be implemented using PIN diodes, FETs, MMIC and MEMS devices. All of the phase shifter configurations have been reviewed and studied. Based on the comparison, a high accuracy and low loss MMIC analogue phase shifter from Hittite has been chosen for the smart antenna array implementation. Several evaluation boards were designed and fabricated to test the analogue phase shifter. From the measurement result, the phase shifter achieves suitable S-Parameters and phase shift for both of WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) standards. This HMC928LP5E analogue phase shifter obtains 180° phase shift at 3.64V and 3.59V, 360° phase shift at 8.22V and 8.11V, with return loss of 10dB and insertion loss of 3dB, at 2.45GHz and 2.6GHz, respectively, which confirms that the analogue phase shifter is adequate for the smart antenna array application.

Then two UWB transitions have been designed, simulated, fabricated and characterised between the UWB feeding network, phase shifters and the monopole antennas. The two transitions are able to transfer the RF signal from CPW to microstrip and achieve smooth field transformation and impedance matching. The proposed structure shows return loss of 10dB and suitable insertion loss of 0.2dB from 0.5GHz to 9GHz.

Finally, a novel smart antenna array integrating planar monopole antennas, UWB feeding network, analogue phase shifters and UWB transitions is proposed and fully evaluated. The dimension of the individual antenna element is 35mm×35mm and the design demonstrates high return loss (19dB, 30dB), high efficiency (79%, 87%) and large gain (2.72dBi, 2.88dBi) at 2.45GHz and 2.6GHz, respectively. A four-element planar antenna array combining the unit antenna has been designed, simulated and characterised. By appropriately controlling the analogue phase shifters and adjusting the excitations of the elements, beam steering for ±50° and ±52° in H-plane with the gain fluctuation less than 3dB and low side lobe level at 2.45GHz and 2.6GHz are achieved. Both simulated and measured results verified the validity of the array configuration. Due to its advantages of compact size, simple structure, accurate control, easy fabrication and low power consumption, the proposed smart antenna array has applications to multiband and multifunctional wireless communication systems.

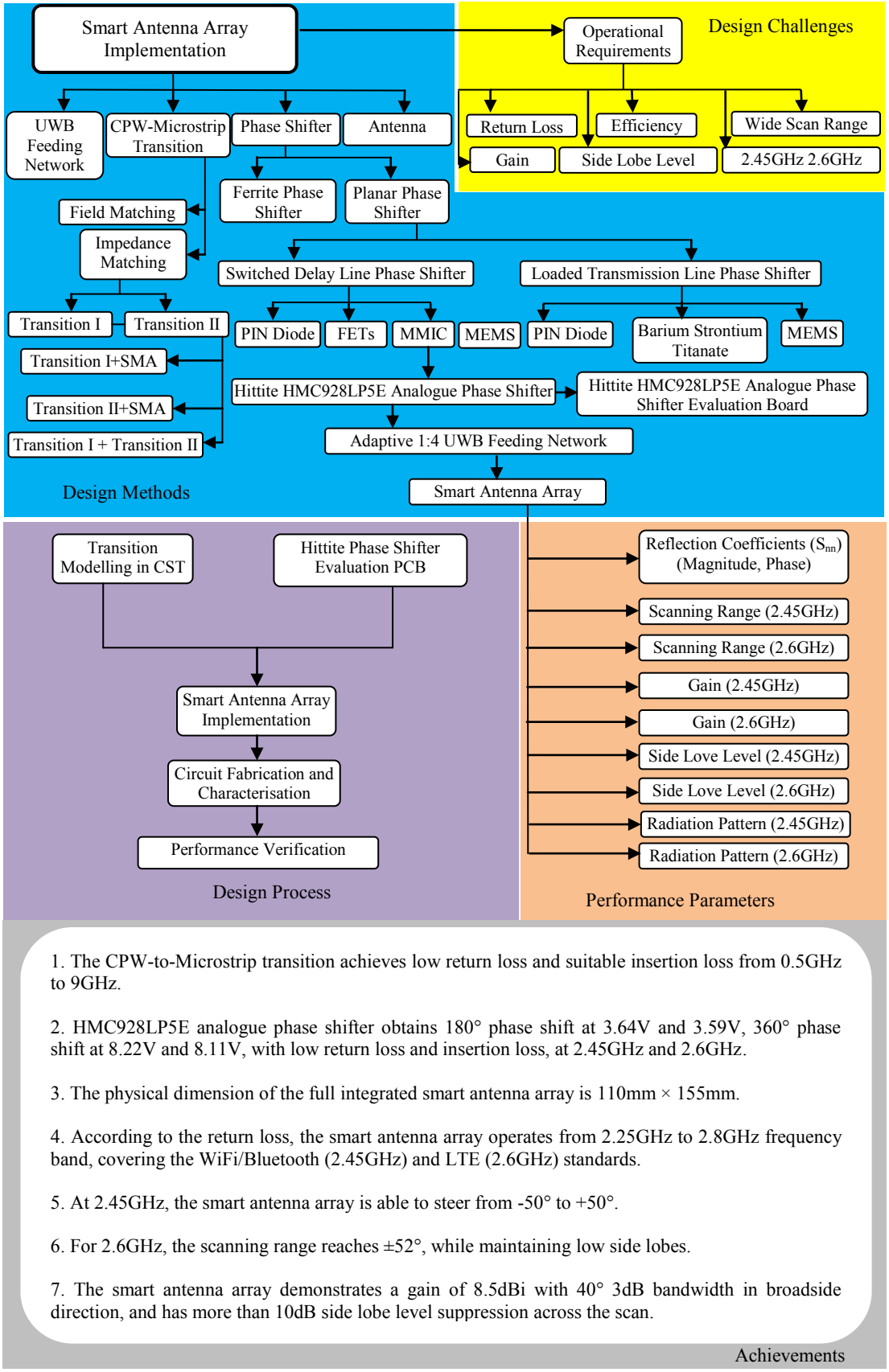


Figure 4.54: The Investigation of Smart Antenna Array Full Implementation

Chapter 5: Hardware Control Systems for Smart Antenna

5.1 Introduction

In the previous chapter, the fully integrated smart antenna array has been characterised and analysed. By appropriately controlling the analogue phase shifters and adjusting the excitations of the elements, beam steering is achieved for the required frequency bands. However, the control voltage was generated by an external DC power supply, as presented in Figure 4.33, which is large, heavy and difficult to achieve the automatic control. This chapter demonstrates the design, fabrication and evaluation of hardware systems in order to digitally control the smart antenna array. The smart antenna system is developed for mobile applications, so the hardware control section should be miniaturised, light weight, low power consumption and able to be integrated into smart phones or tablets.

The smart antenna array is controlled by software installed on the mobile devices. The controlling system includes software package installed on the mobile terminal and a USB interface board hosting a microprocessor. The USB interface board sends a set of controlling commands to the antenna array and transfer WiFi signal into the USB WiFi adapter. The smart antenna is made adaptive by digitally tuning the analogue phase shifters to support the beam steering. Finally, the software installed on the mobile terminal will indicate the WiFi signal information at different main beam directions.

Two USB interface boards are presented in this chapter, by utilising different microcontrollers, PIC18F4550 and LPC1768, respectively. Voltage booster of NJM2360 increases the power from 3.3V to 30V, and several digital potentiometers will generate the variable output voltages. By supplying these output voltage levels to the analogue phase

shifters, the smart antenna array can be reconfigured. Figure 5.1 shows the system layout of the hardware implementation for the smart antenna array system.

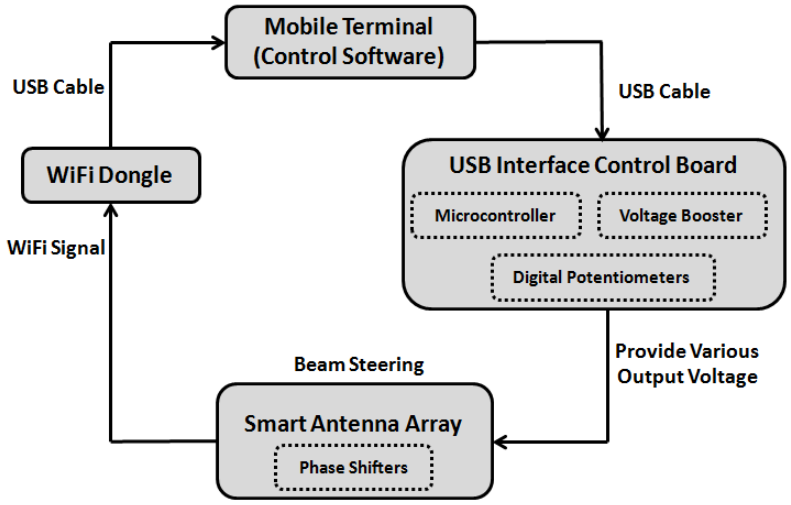


Figure 5.1: System Block Diagram of the Smart Antenna Array System

This chapter is mainly divided into five sections. Section 5.1 describes an overview of the hardware implementation. Section 5.2 focuses on key component characterisations in the control system. Two control PCB design, fabrication and evaluation using microcontroller PIC18F4550 and LPC1768 are discussed in Section 5.3 and Section 5.4, respectively. Section 5.5 presents the WiFi adapter applied in the hardware control system. Finally, the summary is addressed in Section 5.6.

5.2 Key Components Characterisations

In the USB interface control board, there are several key components and their characterisations determine the circuit design.

5.2.1 Microcontroller PIC18F4550

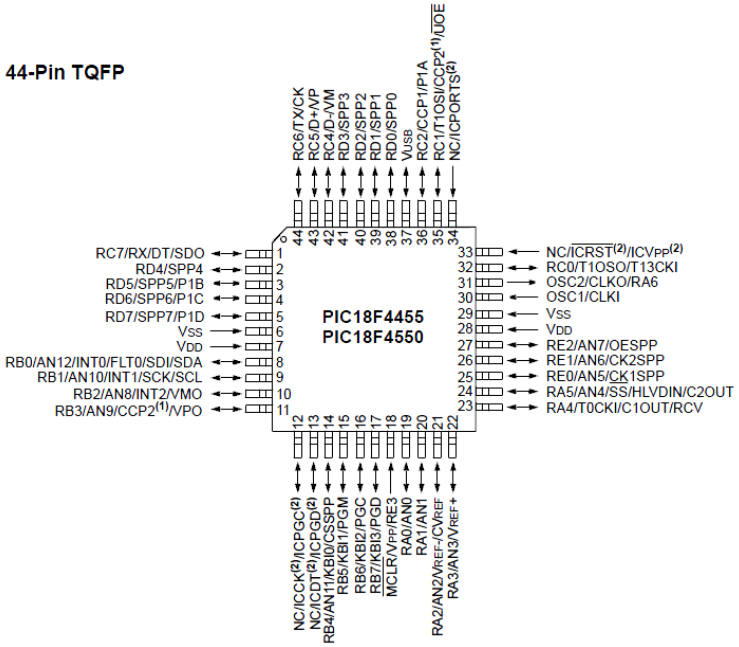


Figure 5.2: PIC18F4550 PIN Diagram [130]

PIC18F4550 from Microchip Technology Inc is one of the microcontrollers applied in the smart antenna array hardware control system. It is a 44-pin high performance USB microchip with nano watt technology [130].

The PIC18F550 microcontroller incorporates a fully featured universal serial bus communications module which is compliant with the USB Specification Revision 2.0. Low speed and full speed communications are both supported by this USB module for all data transfer types. Furthermore, the microcontroller contains an on-chip transceiver and a 3.3V regulator, and also supports the application of external transceivers and voltage regulators.

In the hardware control system, the microcontroller PIC18F4550 establishes the communication between mobile terminals and the PCB board. Oscillator of the microchip decides the data transfer speed and is the "heartbeat" of the digital circuit. The operation of oscillator in PIC18F4550 device is controlled by two configuration registers and two control registers. CONFIG1L and CONFIG1H are the configuration registers, which determine the oscillator mode and USB prescaler/ postscaler options. As configuration bits, they are set when the microchip is programmed and remain that configuration until the microchip is reprogrammed. For the control registers, the OSCCON register selects the active clock mode, which is primarily applied in controlling clock switching in power-managed modes. The OSCTUNE register is utilised to trim the INTRC frequency source and also choose the low frequency clock source for several special features. The PIC18F4550 microchip is able to

operate in twelve distinct oscillator modes. HSPLL (High-Speed Crystal/Resonator with Phase Locked Loop Enabled) is the ideal oscillator mode for the smart antenna array hardware control board. In this configuration, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins in order to generate oscillation. Figure 5.3 demonstrates the pin connections.

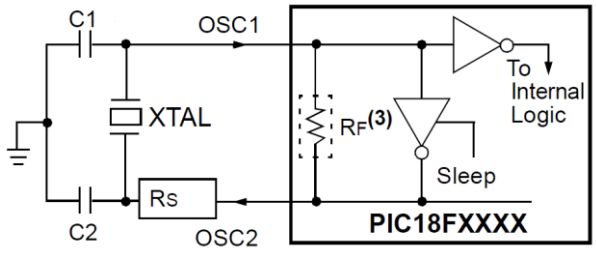


Figure 5.3: Oscillator Pin Connections [130]

Various capacitor values have been evaluated in order to produce acceptable oscillator operation. Higher capacitance will increase the stability of oscillator, but also increases the start-up time. In the PIC18F4550 USB interface control board, the crystal of 20MHz has been used, which requires the capacitance (C_1 and C_2) around 20pF. After testing the oscillator performance over the expected V_{DD} (5V) and temperature range for the application, 22pF for C_1 and C_2 have been selected. In the circuit presented in Figure 5.3, the series resistor Rs is used to avoid overdriving crystals with low drive level specification. The operating frequency of this microchip is 20MHz, which is already very high and Rs is not necessary for this design. Typically, the resistor in parallel with the crystal (R_F) is 1MΩ.

The phase locked loop (PLL) is enabled in HSPLL oscillator mode. It produces a fixed 96 MHz reference clock from a fixed 4 MHz input. Then, the output could be divided and applied for both USB and microcontroller core clock. In this implementation, the PLL frequency is used for the Bootloader program in order to control the microchip, which will be discussed in Chapter 6 software design section.

Before programming the microchip, it is required to reset the device. The reset command will control the master clear reset ($\overline{\text{MCLR}}$) pin and the circuit diagram is displayed in Figure 5.4. The $\overline{\text{MCLR}}$ pin provides a method for triggering an external reset for the microcontroller. A reset is achieved by holding the pin low. There is a noise filter in the $\overline{\text{MCLR}}$ reset path which detects and ignores small pulses. The diode D helps discharge the capacitor quickly when V_{DD} power is down. Normally, the resistor R is smaller than 40 kΩ to make sure the device's electrical specification will not be violated by the voltage drop across R.

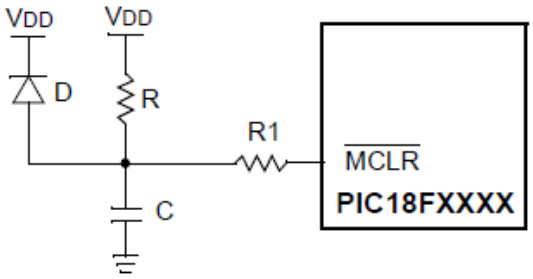


Figure 5.4: External Power Reset Circuit [130]

From Figure 5.2, it is noted that there are more than 30 Input / Output (I/O) ports on the microchip. Depending on the device selected and features enabled, up to five ports are available for each series (RA, RB, RC and RD). Moreover, some of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. Each I/O port has three kinds of registers: TRIS register (data direction register), PORT register (reads the levels on the pins of the device) and LAT register (output latch). For instance, in the RA series, PORTA is an 8-bit wide, bidirectional port and TRISA is the corresponding data direction register. When TRISA bit = 1, the PORTA pin becomes an input, which means the corresponding output driver is in a high impedance mode. When TRISA bit = 0, PORTA pin changes into an output, and the contents of the output latch will be transferred to the selected pin. The PORTA register reading illustrates the status of the pin and its writing value will finally go to the port latch (LATA). More descriptions of the three registers will be presented in Chapter 6.

There is a real serial peripheral interface (SPI) port on the PIC18F4550 microcontroller. The SPI mode allows 8 bits data to be transmitted synchronously and received simultaneously. To establish the communication, three pins will be utilised: serial clock (SCK), serial data in (SDI) and serial data out (SDO). However, in the hardware system, sixteen digital potentiometers will be connected to the microchip and there is only one real SPI mode in the chip, which is not enough to control all of the devices. For the purpose of configuring the potentiometers individually and make full use I/O ports, virtual SPI communications are applied. In the smart antenna array hardware control system implementation, sixteen I/O ports control the digital potentiometers. Another two I/O pins generate virtual clock (CLK) and chip select ($\overline{CS}$) in order to simulate the SPI communication method.

A Bootloader code is required to configure the PIC18F4550 microchip and an ICSP programmer is used to burn the code into the microcontroller. ICSP programming utilises the

PGD and PGC ports on the microchip and two pull-up resistors are connected to V_{DD}. Finally, several LEDs are linked to the PIC18F4550 chip to indicate the communication status.

5.2.2 Microcontroller LPC1768

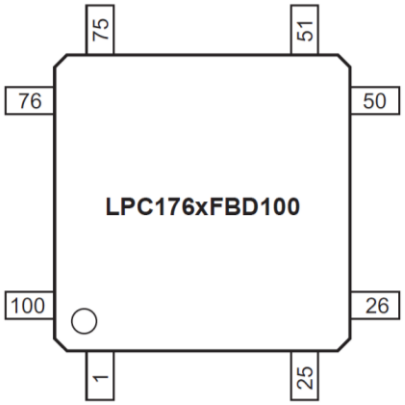


Figure 5.5: LPC1768 PIN Configuration [131]

The LPC1768 is an ARM Cortex-M3 based microcontroller for embedded applications featuring a high level of integration and low power consumptions. The ARM Cortex-M3 is a next generation core that offers system enhancements such as enhanced debug features and a higher level of support block integration. The operating CPU frequency of LPC1768 is up to 100MHz. The ARM Cortex-M3 CPU incorporates a three-stage pipeline and applies a Harvard architecture with separate local instruction and data buses as well as a third bus for peripherals. This microcontroller also includes an internal prefetch unit that provides speculative branching.

The peripheral complements in LPC1768 includes a flash memory (up to 512 kB), data memory (up to 64kB), USB Device/Host/OTG interface, UARTs, eight-channel general purpose DMA controller, SPI interface, I^2C-bus interfaces, Ethernet MAC, eight-channel 12-bit ADC, 10-bit DAC, motor control PWM, timers, ultra-low power Real-Time Clock (RTC) and up to 70 general purpose I/O outputs. The device is in LQFP100 package and the pin configuration is displayed in Figure 5.5.

The LPC1768 includes three independent oscillators. These are the main oscillator, RTC oscillator and the IRC oscillator. Each oscillator could be utilised for several purposes as required in particular applications.

Following reset, the LPC1768 operates from the internal RC oscillator until switched by software. This allows the microcontroller to operate without any external crystal and Bootloader code to work at a known frequency. In the smart antenna hardware design, the oscillator is driven by a clock in slave mode. A capacitor C_i = 100 pF is placed between the

clock and oscillator. To limit the input voltage to the specified range, an additional capacitor to ground C_g is applied which attenuates the input voltage by a factor $C_i/(C_i+C_g)$. Figure 5.6 presents the circuit diagram of the oscillator.

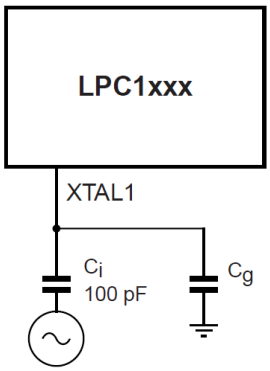


Figure 5.6: Oscillator Circuit Diagram [131]

Device pins that are not connected to a specific peripheral function are controlled by the general purpose input/output (GPIO) registers. These pins can be dynamically configured as inputs or outputs. Separate registers allow writing or clearing any number of outputs simultaneously. Similar to the PIC18F4550 microcontroller, several GPIO pins are used in order to simulate the SPI communication. Detailed descriptions will be addressed in Section 5.3.

The LPC1768 microcontroller will be controlled by USB connection. In the chip, the universal serial bus (USB) is a four-wire bus that allows communication between a host and several peripherals. The host controller allocates the USB bandwidth to attached devices through a token-based protocol. The bus supports hot plugging and dynamic configuration of the devices. All of the transactions are initiated by the host controller, which is the mobile terminal in the hardware design. The USB connection for the LPC1768 microchip is demonstrated in Figure 5.7.

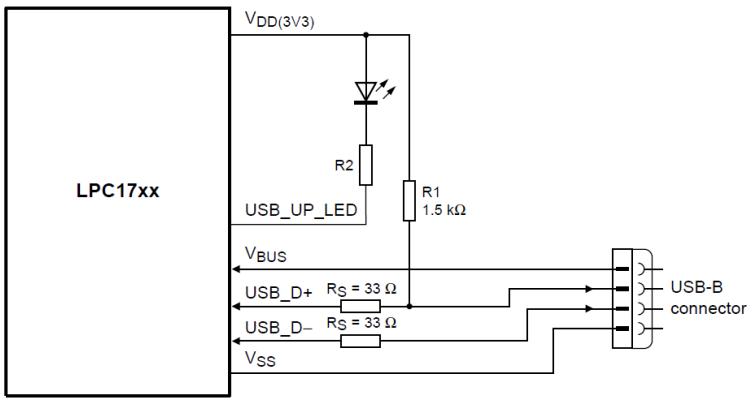
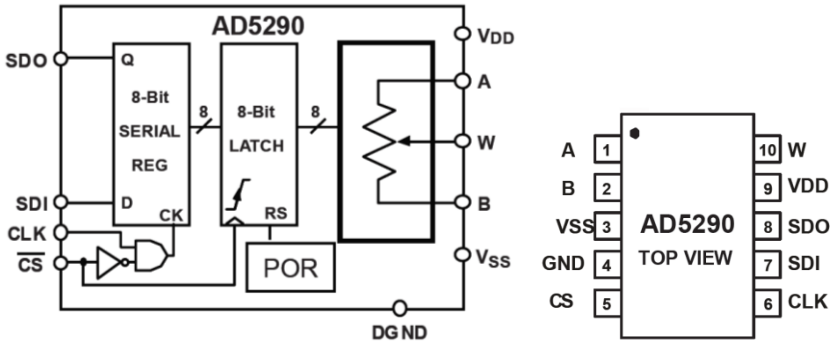


Figure 5.7: LPC1768 USB Connection [131]

5.2.3 Digital Potentiometer AD5290

In the hardware control system, compact +30V/±15V 256-position digital potentiometer AD5290 from Analog Device is used for providing control voltages to the phase shifters, as displayed in Figure 5.8.



(a) **(b)**

Figure 5.8: (a) AD5290 Functional Block Diagram (b) AD5290 PIN Configuration [132]

AD5290 is a low cost, high voltage, high performance, and compact digital potentiometer. It has been widely utilised for the applications such as programmable voltage supply, high voltage DAC, audio volume control and programmable gain and offset adjustment.

AD5290 performs the same electronic adjustment function as variable resistors, mechanical potentiometers and trimmers, with solid state reliability, enhanced resolution and superior temperature stability. Since the device is digital control instead of manually, it shows layout flexibility and allows closed-loop dynamic controllability. In the hardware implementation, AD5290 with 100 kΩ maximum resistor and MSOP-10 package is selected.

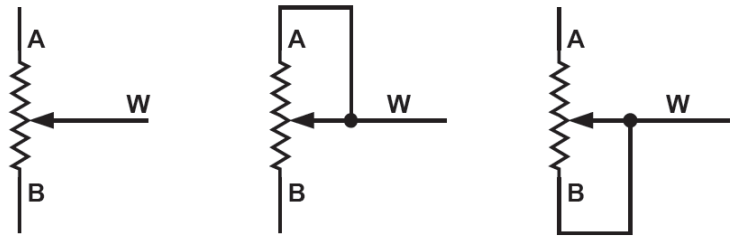


Figure 5.9: Rheostat Mode Configuration [132]

When only the W-B or W-A terminals are used as variable resistors, the floating terminal is opened or shorted by W. This operation is defined as rheostat mode, as illustrated in Figure 5.9. The resistance between terminal A and B is 100 kΩ with ±30% tolerance and it provides 256 tap points accessed by the wiper terminal (W). The 256 possible positions are selected by an 8-bit data decoded in the RDAC latch. The 8-bit data is controlled by SPI interface.

Equation 5.1 presents the programmable output resistance between the terminal W and A.

$$R_{WA}(D) = \frac{256-D}{256} \times R_{AB} + 3 \times R_W \quad (5.1)$$

Where, D represents the decimal equivalent of the binary code loaded to the 8-bit RDAC register from 0 to 255. R_{AB} is the maximum resistance, 100kΩ in this application. R_W shows the wiper resistance caused by the internal switch. R_W is a function of V_{DD} and temperature. Compared to the temperature coefficient of R_{AB} which is only 35 ppm/°C, the temperature coefficient for the wiper resistance is significantly higher because the wiper resistance doubles from 25°C to 125°C. However, in this application, the room temperature remains the same and R_W stays at 150Ω. Contrary to R_{AB} which is 100kΩ, R_W is small enough to be neglected.

Terminal A and W generate the output resistance of AD5290 in the hardware system. R_{WA} starts at the maximum value and starts to reduce when the latch data increases.

Based on the rheostat mode, the digital potentiometer easily provides a voltage divider at W-B and W-A proportional to the input voltages at terminal A to B (as shown in Figure 5.10).

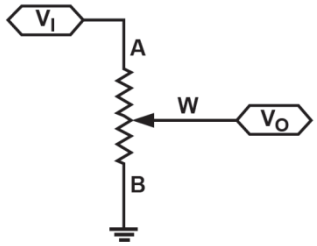


Figure 5.10: Voltage Divider Mode Circuit Diagram [132]

$$V_W(D) = \frac{D}{256} \times V_A + \frac{256-D}{256} \times V_B \quad (5.2)$$

Connecting A to 30 V and B to ground produces an output voltage at W. The output voltage (V_0) is defined by the position of potentiometer divider and the value is decoded from the 8-bit RDAC register. For instance, if the 8-bit data is 11010011(binary), the decimal value of D is 211, resistance R_{WA} from Equation 5.1 is 17.58kΩ and the output voltage at W (V_W) is 24.73V.

Compare to the rheostat mode, this voltage divider mode is dependent mainly on the ratio of the internal resistors R_{WA} and R_{WB} and not the absolute values. Therefore, it demonstrates an obviously reduce of the temperature drift, which makes the device more accurate.

AD5290 is communicating with SPI, which contains a three-wire digital interface: $\overline{CS}$, CLK, and SDI (as presented in Figure 5.11). In order to avoid clocking incorrect data into the serial input register, the positive edge sensitive CLK input needs clean transitions. When the chip select pin $\overline{CS}$ is low, the clock loads data into the serial register on each positive clock edge and the MSB of the 8-bit serial is loaded first. The data hold and setup times in Figure 5.11 determine the valid timing requirements. After eight clock cycles, the 8-bit serial input data register transfers the words into internal RDAC register and the $\overline{CS}$ line changes to logic high. Extra MSB bits are ignored. The detailed timing diagram is discussed in Chapter 6.

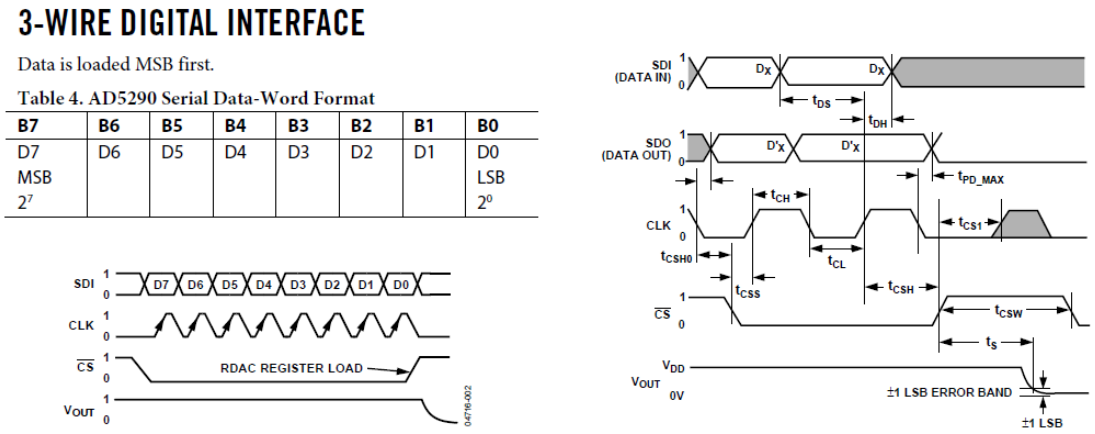


Figure 5.11: AD5290 Timing Diagram [132]

Furthermore, since SDO shifts out the SDI content in the previous frame, AD5290 could be connected as daisy-chaining multiple devices.

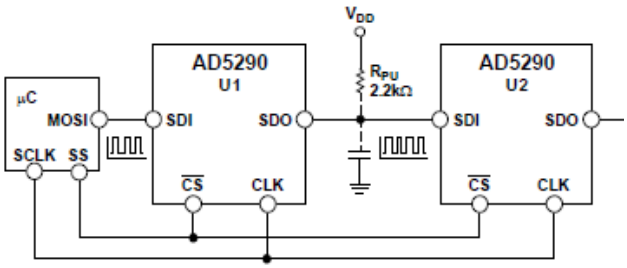


Figure 5.12: AD5290 Daisy-Chain Operation [132]

In Figure 5.12, two AD5290 devices are daisy-chained, and a total of 16 bits of data is needed for each operation. The first set of 8 bits transfer into U2, and the second set of 8 bits go to U1. This communication method can simplify the design structure, but the whole system will break down if any of the potentiometer is damaged. For the system stability, this daisy-chain connection is not applied in the hardware implementation. The sixteen digital potentiometers are connected and controlled in parallel.

5.2.4 Voltage Booster NJM2360

The control board is powered with the USB port which supplies 5V DC voltage and the digital potentiometer requires 30V power supply. A voltage booster NJM2360 that increases the DC voltage from 5V to 30V is included in the hardware design.

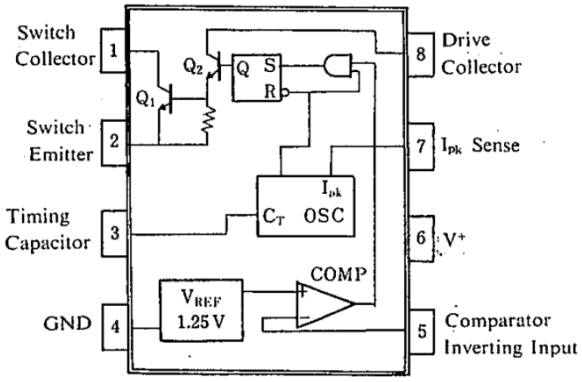


Figure 5.13: NJM2360 Block Diagram [133]

NJM2360 is a DC-DC converter control IC which is designed to be incorporated in Step-Down, Step-Up and inverting applications with a minimum number of external components. The operating voltage is from 2.5V to 40V and the output voltage varies between 1.25V to 40V.

In the hardware implementation, a Step-Up converter is being used, as displayed in Figure 5.14.

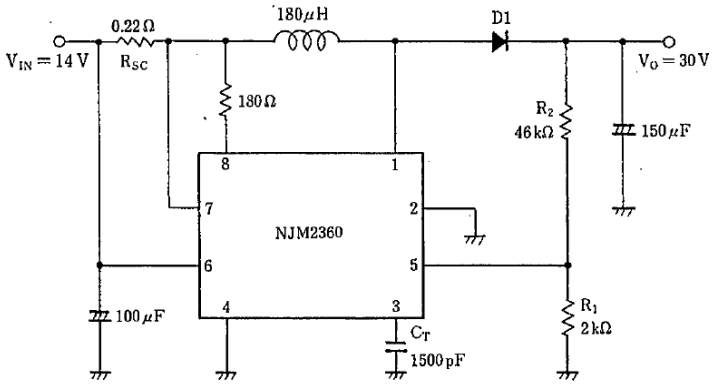


Figure 5.14: Voltage Booster Step-Up Circuit

By applying 30V to the digital potentiometers, the output voltages are varied between 0V to 30V, which can provide suitable control voltages to the phase shifters.

5.2.5 USB to UART Interface FT232RL

A USB to UART interface FT232RL device is used for microcontroller LPC1768 to achieve the real-time control.

The FT232RL is a USB to serial UART interface with optional clock generator output, and new FTDI security dongle feature. Moreover, synchronous and asynchronous bit bang interface modes are available. USB to serial designs using the FT232RL have been further simplified by fully integrating the external EEPROM, clock circuit and USB resistors onto the device. Figure 5.15 shows the FT232RL pin configuration.

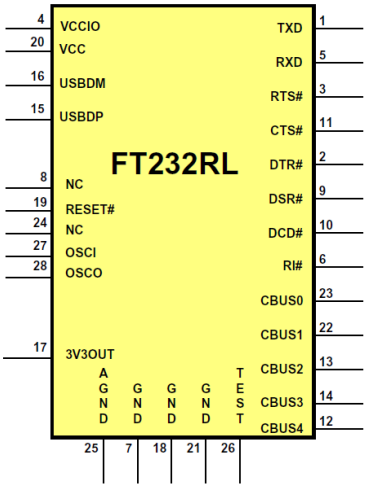


Figure 5.15: FT232RL Pin Configuration [134]

The FT232RL translates USB into UART interface and connects to the microcontroller LPC1768. Using this method, the LPC1768 can communicate through USB connection to mobile terminals and generate a real-time control. The circuit diagram is illustrated in Figure 5.16.

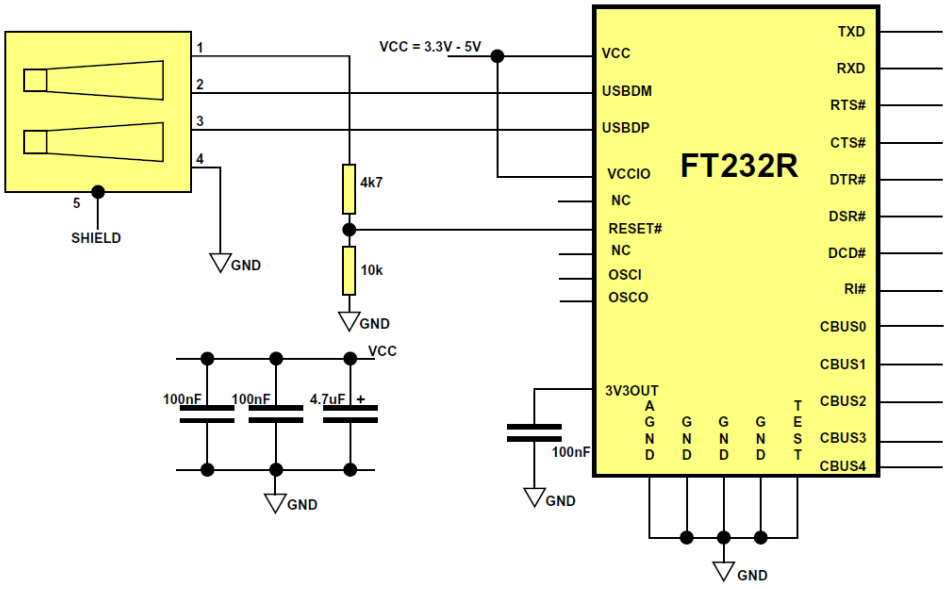


Figure 5.16: FT232RL to USB Configuration [134]

In this implementation, the USB bus power is utilised to control the RESET Pin of the FT232R device. When the USB host is powered up, the internal 1.5kΩ resistor on USBDP is pulled up to 3.3V, thus identifying the device as a full speed device to USB. When the USB host power is off, RESET will be low and the device is held in reset. As RESET is low, the internal 1.5kΩ resistor will not be pulled up to 3.3V, so no current will be forced down USBDP via the 1.5kΩ resistor when the host is powered down.

FT232RL is in a USB self powered configuration. A USB self powered device obtains power from its own power supply and does not draw current from the USB bus.

Using the key components described in this section, two separate control PCBs using PIC18F4550 and LPC1768 microcontrollers for the smart antenna array system have been designed, tested, fabricated and evaluated.

5.3 Control PCB Implementation Using PIC18F4550

5.3.1 Circuit Diagram

The complete circuit is composed of microcontroller, voltage booster, digital potentiometers, USB module and testing elements. The circuit and board design are built and analysed in a PCB design tool, namely KiCad.

Figure 5.17 demonstrates the microcontroller circuit diagram.

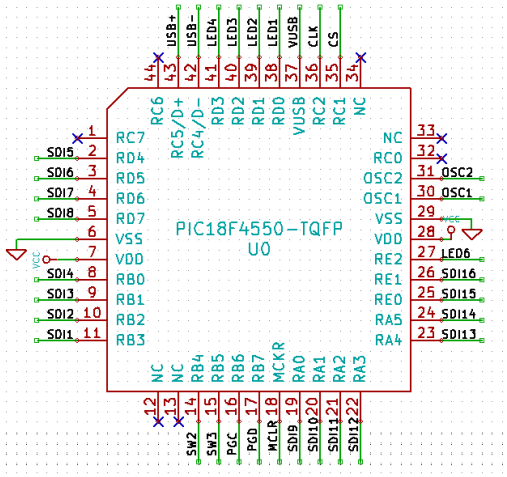


Figure 5.17: Microcontroller 18F4550 Circuit Diagram

In this microcontroller schematic, PIN2, PIN3, PIN4, PIN5, PIN8, PIN9, PIN10, PIN11, PIN19, PIN20, PIN21, PIN22, PIN23, PIN24, PIN25 and PIN26 are used to generate SDI signals to the sixteen digital potentiometers. These pins send 8-bit data to control the output voltages. PIN14 and PIN15 are followed by two switches to test the microchip. PIN16 and PIN17 are utilised for ICSP programming. There is a pull-up resistor linked to PIN18 in order to reset the device. PIN30 and PIN31 are driven by a crystal oscillator. PIN35 and PIN36 provide $\overline{CS}$ and CLK signals to the potentiometers. PIN38, PIN39, PIN40 and PIN41 are connected with LEDs to show the connection status. PIN27 also controls a LED to run the Bootloader and Hello World program to initialise the microcontroller. PIN42 and PIN43 are used for the USB module. Power supply goes into the device through PIN7 and PIN28.

The digital potentiometer circuit diagram is illustrated in Figure 5.18.

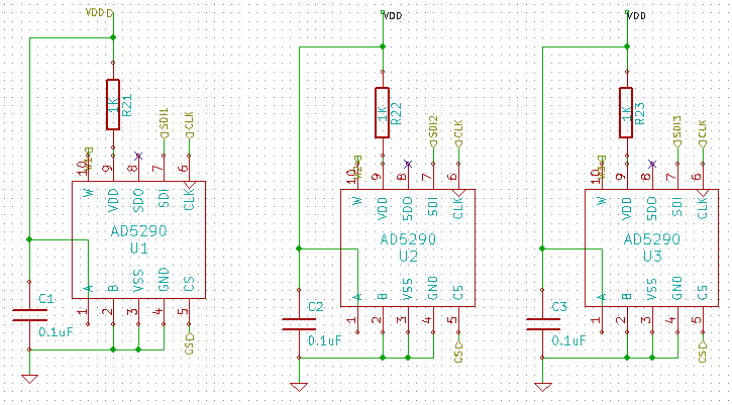


Figure 5.18: Digital Potentiometer AD5290 Circuit Diagram

In order to achieve 30V maximum output voltage, PIN1 (Terminal A) is connected to V_{DD} and PIN2 (Terminal B) is combined to ground. Therefore, the output voltage at PIN10 (Terminal W) varies from 0V to 30V with 255 possible positions. The 8-bit data comes from

PIN7 (SDI). $\overline{CS}$ and CLK control signals go to PIN5 and PIN6, respectively. There is a resistor of 1kΩ placed between PIN9 and V_{DD} with the function of protecting the potentiometer when the supply voltage increases suddenly. Finally, a decouple capacitor is added between V_{DD} and ground.

Figure 5.19 shows the voltage booster NJM2360 circuit diagram.

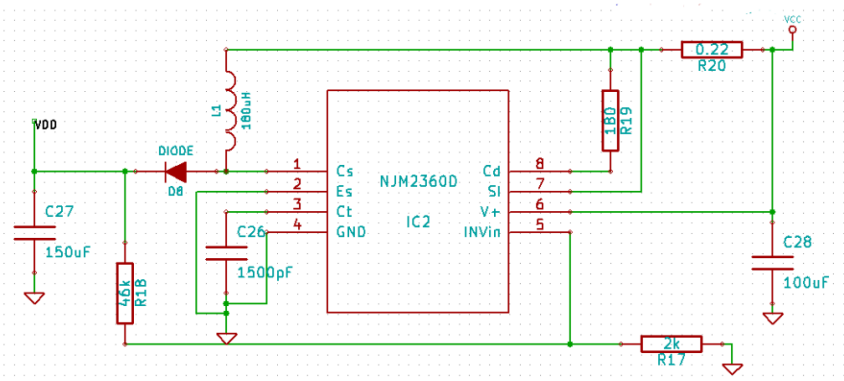


Figure 5.19: Voltage Booster NJM2360 Circuit Diagram

In this schematic, the input voltage at Vcc is 5V and the output voltage is 30V.

The USB connection is shown in Figure 5.20. There is a ferrite bead between Vcc and V_{USB} with the purpose of reducing electromagnetic interference (EMI) and radio frequency interference (RFI).

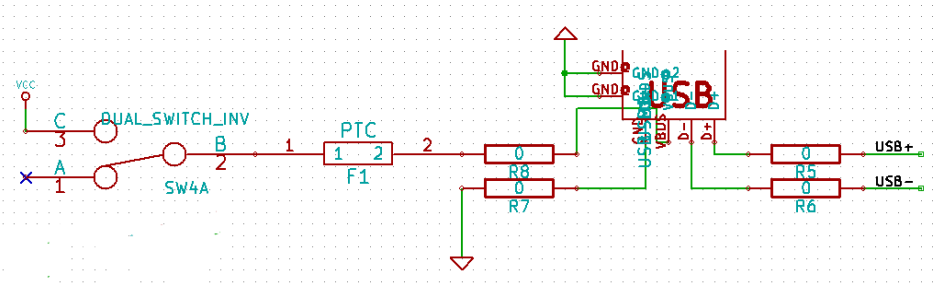
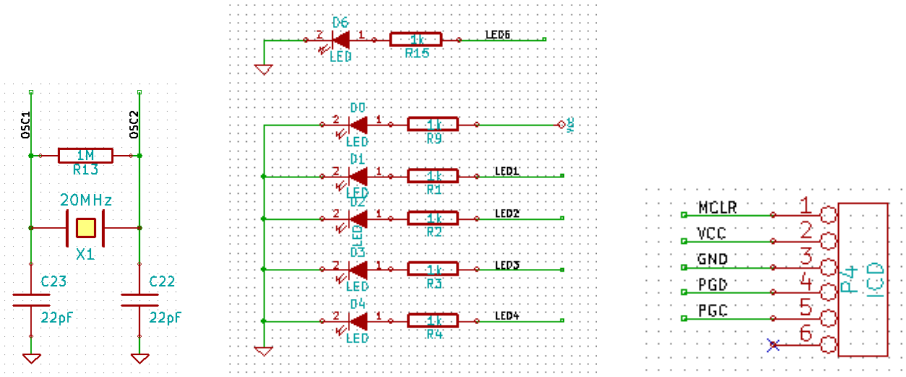


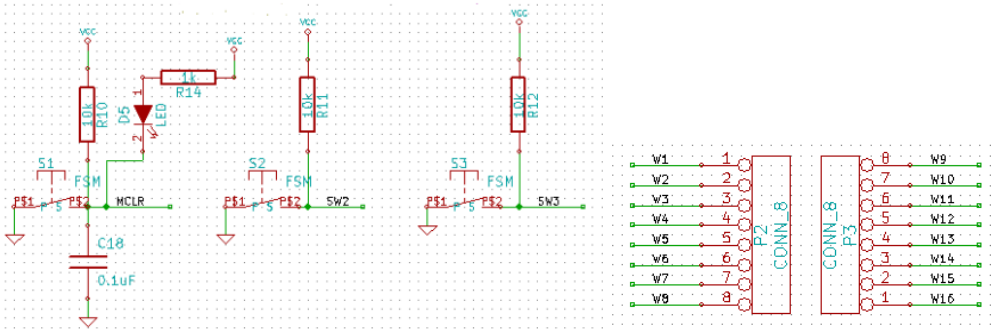
Figure 5.20: USB Module Circuit Diagram

There are several other and testing components on the PCB. Figure 5.21(a) demonstrates the crystal oscillator to the microcontroller. LED D_0 in Figure 5.21(b) illustrates the power supply. LED D_1 D_2, D_3 and D_4 are connected to some specified I/O ports of the microchip to indicate the USB connection statue. LED D_6 is applied for a Hello World program to initialise the device. Figure 5.21(c) shows a 6-Pin connection for ICSP programming. The first switch in Figure 5.22(a) is connected to MCLR of PIC18F4550 to reset the device. The other two are for running the Bootloader code. Figure 5.22(c) presents the output voltage pins.



(a) **(b)** **(c)**

Figure 5.21: (a) Crysital Oscillator (b) Testing LEDs (c) 6-Pin ICSP Connector



(a) **(b)**

Figure 5.22: (a) Reset Switches (b) Output Voltage Pins

The complete circuit diagram of the smart antenna hardware control board design using PIC18F4550 microcontroller is displayed in Figure 5.23.

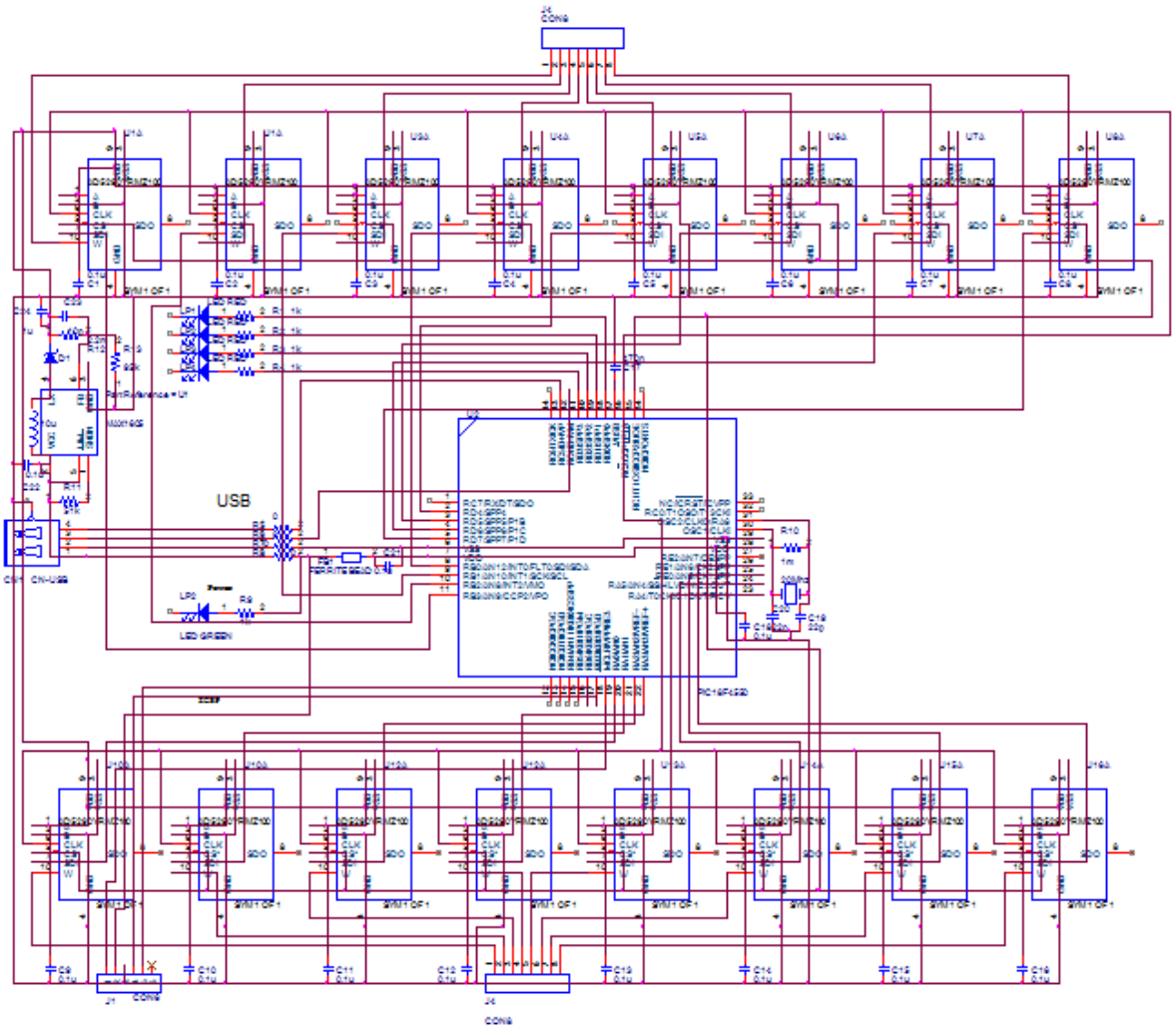


Figure 5.23: Schematic of Control PCB Using PIC18F4550

5.3.2 Breadboard Testing

The design circuits have been constructed on a breadboard for prototyping of electronics. Figure 5.24 presents the breadboard testing.

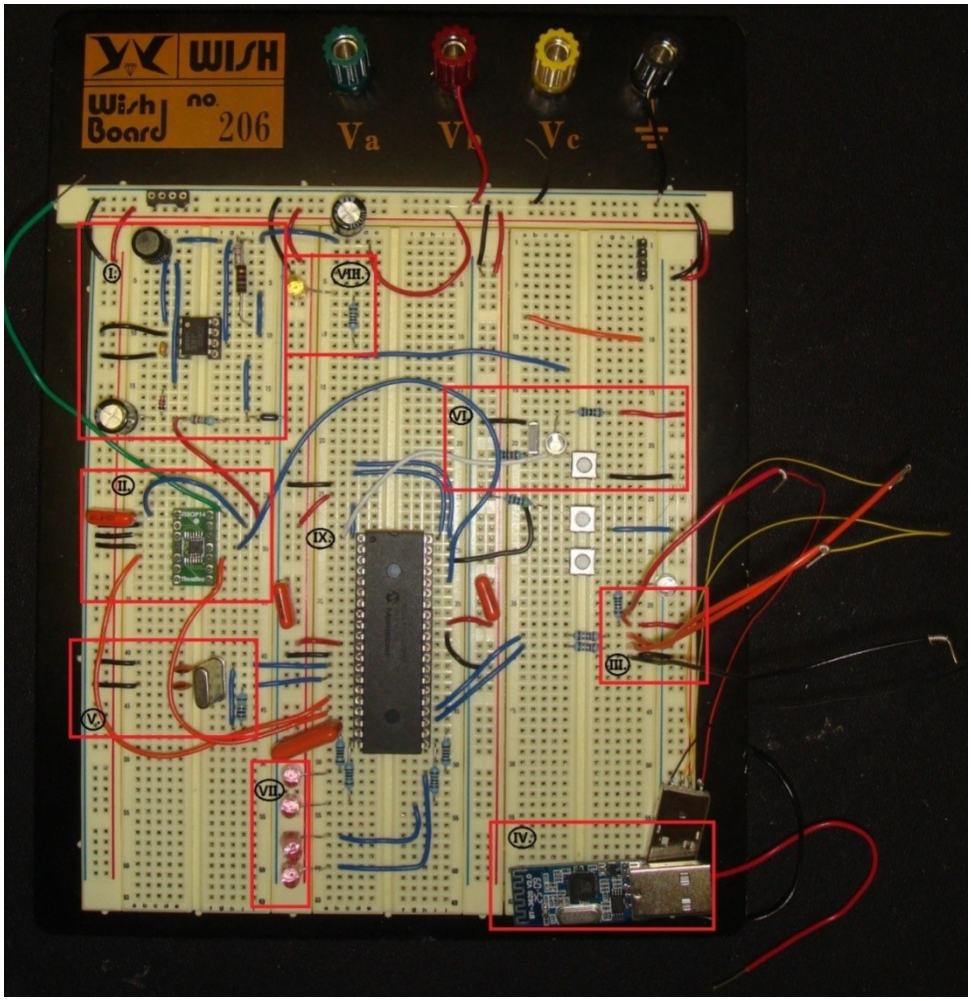


Figure 5.24: Breadboard Testing of Control Board Using PIC18F4550

On the prototype board, a PIC18F4550 microcontroller in TQFP40 package is used to test the circuit design. The whole control system is divided into several sections.

Section I shows the voltage booster, which increases the input voltage from 5V to 30V for digital potentiometers.

Section II is the digital potentiometer circuit. On the breadboard, only one digital potentiometer is being tested. A small socket for AD5290 is used to put the surface mount device (SMD) onto the prototype board. The green wire is the Terminal W of the device, which shows the variable output voltage.

Section III and **Section IV** are connecting the USB module. The red wire is V_{USB}, two orange wires are D+ and D-, and the ground is in black.

Section V demonstrates a crystal oscillator with a frequency of 20MHz. Both of the loading capacitors are 22pF, which have been calculated from Section 5.2.1.

Section VI illustrates a switch with a pull-up resistor for the purpose of resetting the microchip.

In **Section VII**, there are four LEDs with important functions. A Bootloader code is required to be burnt into the microcontroller PIC18F4550 in order to communicate with mobile terminal through USB connection. The four LEDs are showing the communication status. Bootloader program sets the suitable configuration bits of the microcontroller and initialises the whole control system. After programming the Bootloader into PIC18F4550, the mobile terminal treats the control board as a normal USB device and installs a firmware. After that, the first LED is on, showing the initialisation has been done correctly. Then, it is required to press the reset switch in Section VI to wake up the microcontroller. LED2 and LED3 will start to blink and show the microchip is waiting for commands. The blinking frequency is determined by the crystal oscillator. If any configuration bit in the microchip goes wrong, LED3 and LED4 will start to blink. The configuration bit is very important in the hardware implementation, because it decides the memory location, switches on/off the watch-dog, and selects the oscillator types. None of the LEDs will be lighted when the communication is totally wrong, which means it is necessary to reload the Bootloader.

Section VIII displays a yellow LED to run a Hello World program. Based on the Bootloader program, it is possible to write user's control code into this PIC18F4550. In the microchip, the Bootloader program occupies the memory from 0x00 to 0xFF. The new program starts from 0x100 in the memory in order not to disturb the configuration bits used by Bootloader. In this method, the new codes are regarded as part of the Bootloader, which increases the system stability. When the yellow LED blinks at the frequency of 1Hz, it means the configuration bits are suitable for the design and all of the components have been connected correctly. Then the microcontroller PIC18F4550 is able to control the digital potentiometers.

Several decoupling capacitors are placed in **Section IX** near the power supply.

5.3.3 PCB Fabrication

The breadboard testing confirms the design structure, and the circuit has been established on a compact PCB. The PCB geometry is constructed in KiCad, which is an open source integrated package for schematic circuit capture and PCB layout.

The complete design schematic is shown in Figure 5.23. For the PCB layout, the microcontroller PIC18F4550 is in 44Pin TQFP, digital potentiometer AD5290 is in MSOP10 and DMP8 package is for voltage booster NJM2360. All of the inductors, capacitors and

resistors are in SMD0805 dimensions and Mini USB B type is used for the USB connector. The PCB size has been miniaturised. In the design, the minimum tracks width is 0.008 mils, the minimum vias diameter is 0.035 mils, the minimum micro vias diameter is 0.02 mils and the clearance for the net class is 5.0 mils. The signal tracks are 0.013 mils and 0.017 mils are for the power supply. The PCB structure has two metal layers, with the front layer placing all of the components and the back one is a common ground. Control lines are added on both of the layers. Figure 5.25 demonstrates the final PCB design.

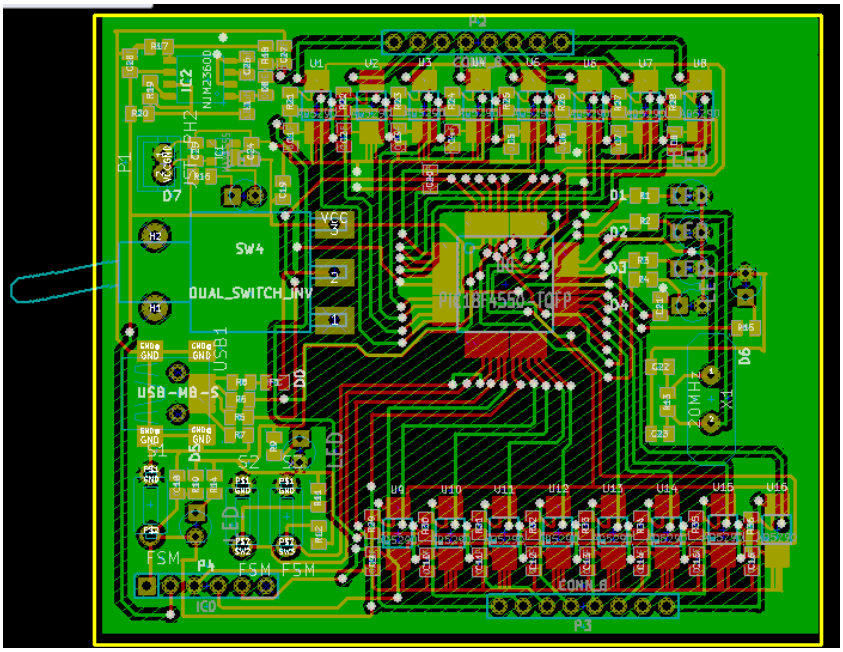


Figure 5.25: PCB Design Using Microcontroller PIC18F4550

The front copper layer and back copper layer are presented in Figure 5.26 and Figure 5.27, respectively. Figure 5.28 illustrates the silk screen showing all of the components.

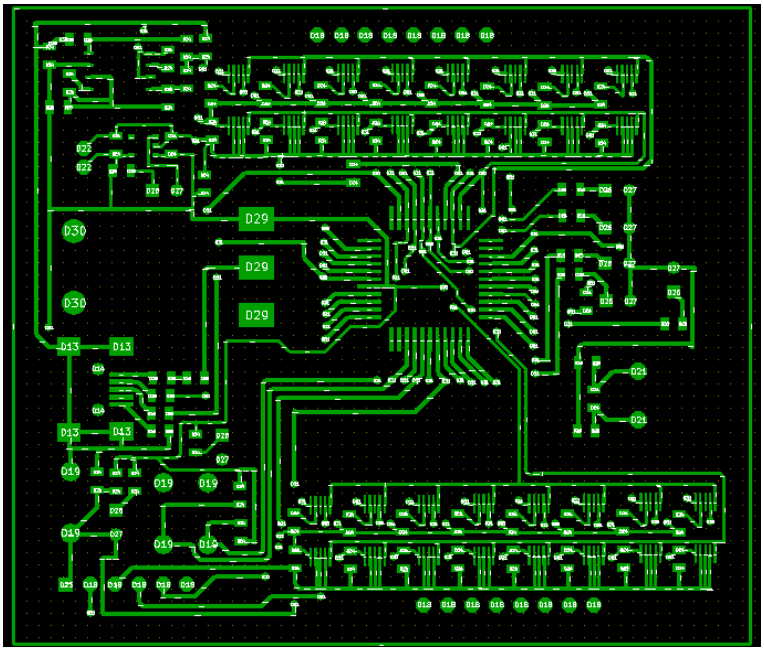


Figure 5.26: Front Layer of PCB Design Using Microcontroller PIC18F4550

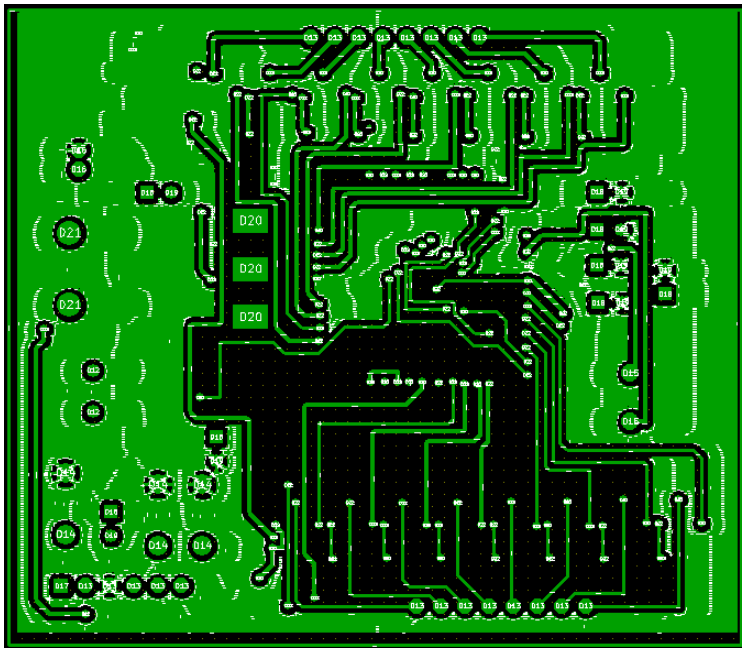


Figure 5.27: Back Layer of PCB Design Using Microcontroller PIC18F4550

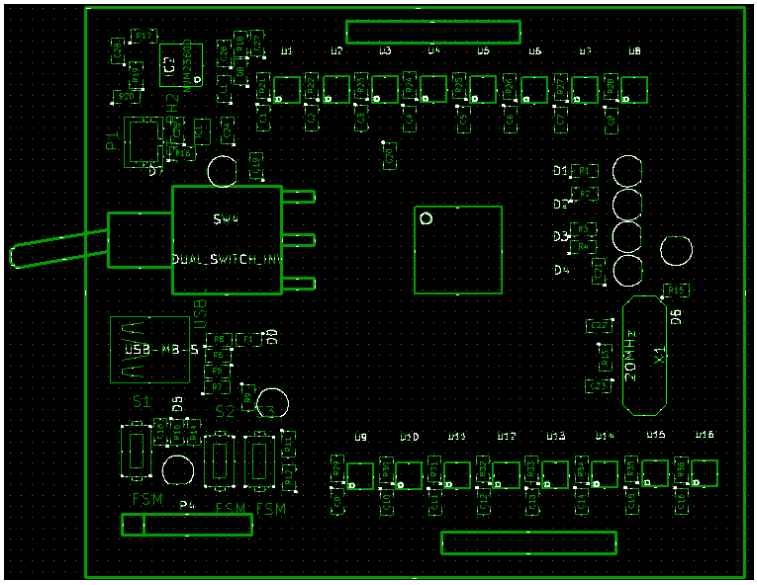


Figure 5.28: Silk Document of PCB Design Using Microcontroller PIC18F4550

3D view of the PCB design is shown in Figure 5.29.

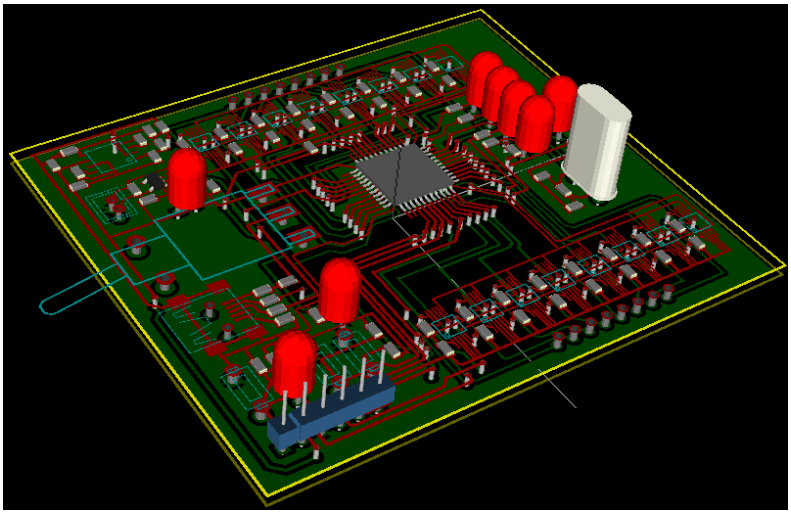
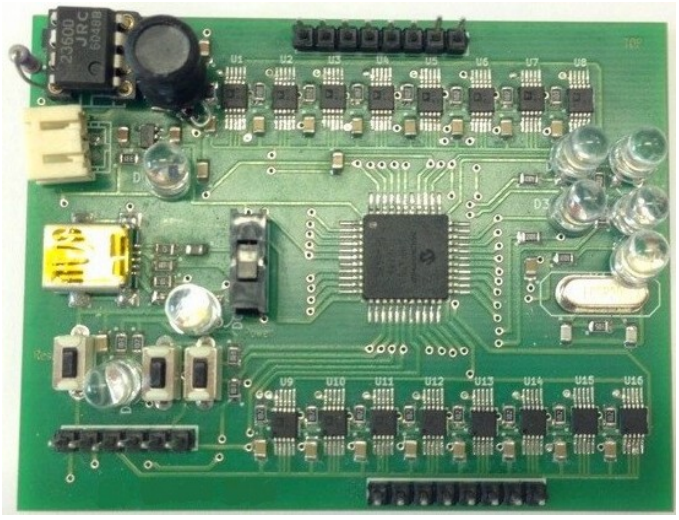
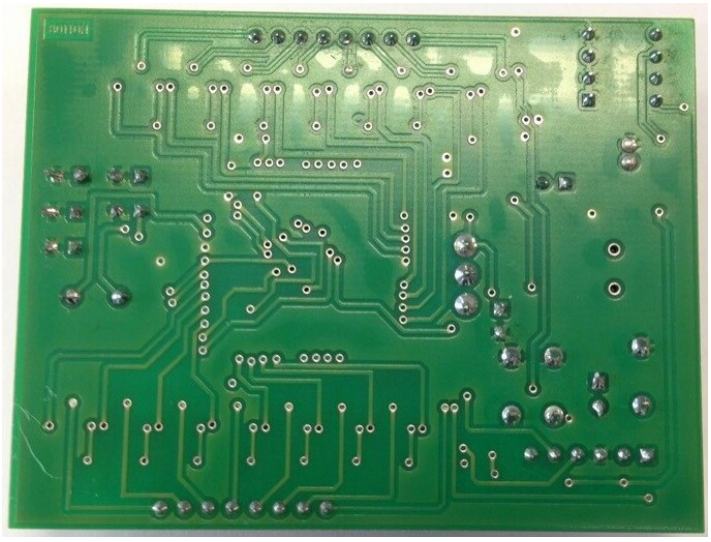


Figure 5.29: 3D View of the PCB Design Using Microcontroller PIC18F4550

The PCB design has been manufactured by Multi Circuit Board Ltd in Germany [135] and assembled by a technician in the University of Edinburgh. The fabricated layout is demonstrated in Figure 5.30. Dimensions of the final layout are 57mm×74 mm.



(a)



(b)

Figure 5.30: Fabricated PCB Design Using Microcontroller PIC18F4550 (a) Front View (b) Back View

5.3.4 PCB Evaluation

Devices in the PIC184550 family incorporate a fully featured universal serial bus communication module that is compliant with the USB Specification Revision 2.0. A Bootloader is needed to setup the configuration bits and initialise the microchip. There are eight source files and thirteen header files required in the Bootloader code and a BootModified.18f4550_g.lkr has been added into the Linker Script. To configure this smart antenna array application, some modifications have been made in io_cfg.h and main.c to map pin ID and pin functions. Some key settings are listed as follows.

```
#include <P18f4550.h>                    // Include the 18f4550 head file
#pragma config PLLDIV   = 5              // 20 MHz crystal on PICDEM FS USB board
#pragma config CPUDIV   = OSC1_PLL2      // OSC1/OSC2 Src:/1, 96MHz PLL Src:/2
#pragma config USBDIV   = 2              //Clock source from 96MHz PLL/2
#pragma config FOSC     = HSPLL_HS       //HS oscillator, PLL enabled, HS used by USB
#pragma config BORV     = 3
#pragma config VREGEN   = ON             //USB Voltage Regulator
#pragma config WDTPS    = 32768
#pragma config ICPRT    = OFF            // Dedicated In-Circuit Debug/Programming
#pragma config XINST    = OFF            // Extended Instruction Set
#pragma config WRTB     = OFF            // Boot Block Write Protection
……
```

The Bootloader code has been compiled using MPLAB (a compiler provided by Microchip) and translated into a hexadecimal document.

There are two available ICSP programmer can be used to copy the Bootloader code into microcontroller PIC18F4550, as shown in Figure 5.31 and Figure 5.32.

Figure 5.31: PICSTART Plus Programmer [136]

PICSTART Plus (as illustrated in Figure 5.31) is a development programmer from Microchip. It connects through serial RS232 port to PC and is operated by Microchip's integrated development environment (IDE) software, namely MPLAB IDE. This programmer supports most of the DIP packaged microcontroller products available from Microchip.

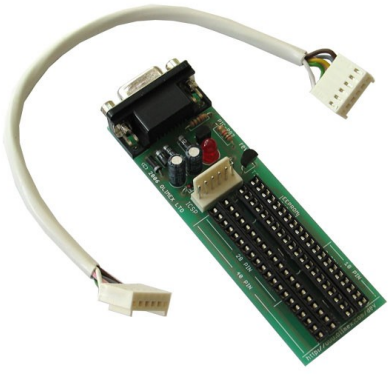


Figure 5.32: PIC-PG2 Programmer

PIC-PG2 (as shown in Figure 5.32) is a programmer based on JDM design which takes all necessary signals and power supply from RS232 serial port. It supports 8Pin, 18Pin, 28Pin and 40pin PIC microcontrollers which allow serial programming and I^2C EEPROM memories. The programmer utilises ICSP cable for direct connection to PIC prototype boards.

The PICSTART Plus programmer is used for the breadboard testing, and PIC-PG2 is applied for the PCB initialisation.

After the microchip initialisation and firmware installation, a software program can be used to control the Bootloader and PIC18F4550 microcontroller, as demonstrated in Figure 5.33.

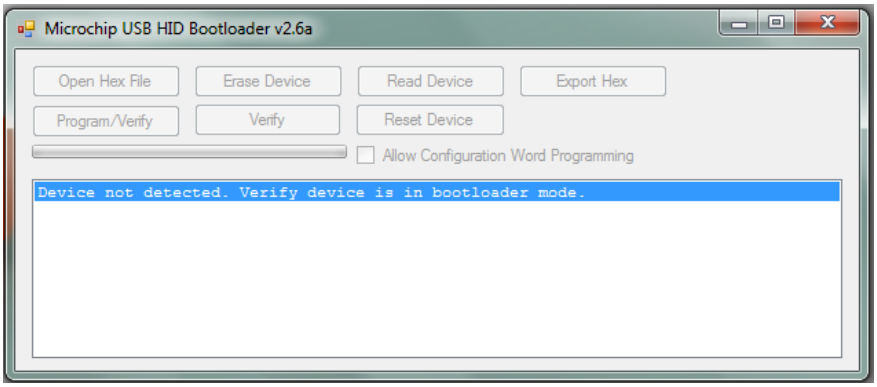


Figure 5.33: Bootloader Program Interface

The PCB using microcontroller PIC18F4550 has been evaluated by a laptop. The laptop sends commands to PIC18F4550 through USB connections, and the microchip control the digital potentiometers to generate different output voltages. By controlling the switching speed, the PCB is able to provide stable DC voltage (from 0V to 30V, as shown in Figure 5.34) and square wave signal with low switching frequency (as illustrated in Figure 5.35). It is clear to note that, this PCB structure is able to configure the phase shifters and finally control the smart antenna array system.

Figure 5.34: Stable DC Output Voltage from PCB Design Using Microcontroller PIC18F4550

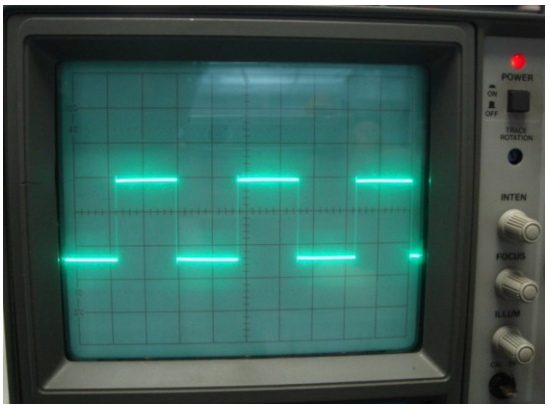


Figure 5.35: Square Wave Output Signal from PCB Design Using Microcontroller PIC18F4550

5.4 Control PCB Implementation Using LPC1768

The microcontroller PIC18F4550 cannot perform real time control, which means every new command to the microchip needs to go through the Bootloader program again and reset the device. In order to achieve the real time control, a PCB design using LPC1768 has been implemented.

5.4.1 Circuit Diagram

Similar to the PIC18F4550 control board, this circuit consists of microcontroller, voltage booster, digital potentiometers, USB module and testing components. The circuit and layout are constructed in a PCB design tool, namely DesignSpark PCB.

Figure 5.36 shows the microcontroller circuit diagram.

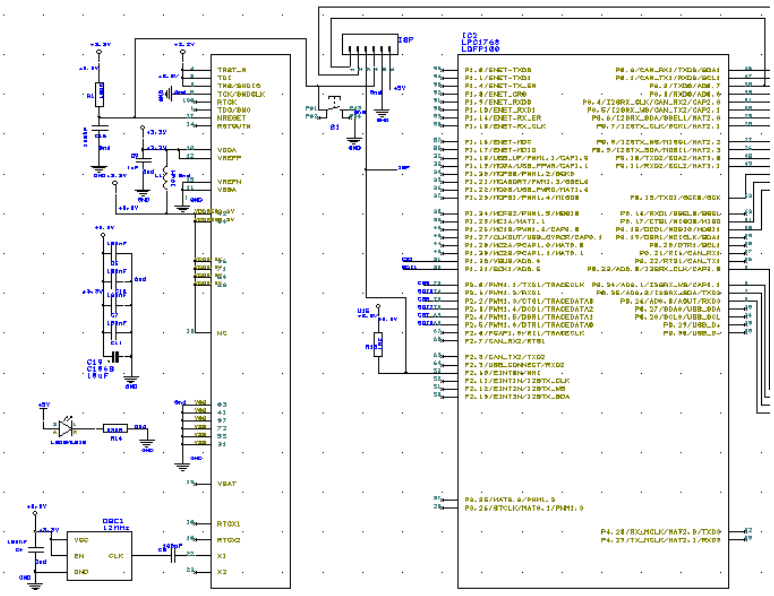


Figure 5.36: Microcontroller LPC1768 Circuit Diagram

There are 100 pins on the microcontroller LPC1768 and only 40 pins are used in this application. In this schematic, digital outputs PIN6, PIN7, PIN8, PIN20, PIN21, PIN46, PIN47, PIN48, PIN49, PIN60, PIN61, PIN62, PIN68, PIN69, PIN70, and PIN73 to PIN81 provide SDI signals to control twelve digital potentiometers. PIN9 generates the common CLK signal. A crystal oscillator of 12MHz is connected to the microchip PIN22 to provide external clock oscillation. PIN8 and PIN9 link to FT232RL device for USB communication. PIN17, PIN53, PIN98 and PIN99 are for ISP programmer to initialise LPC1768. Several pull-up resistors and coupling capacitors are applied to protect the microcontroller. The main power supply goes into PIN10.

Figure 5.37 and Figure 5.38 present the digital potentiometer AD5290 and voltage booster NJM2360 circuit diagram, respectively, which are similar to the PIC18F4550 control board.

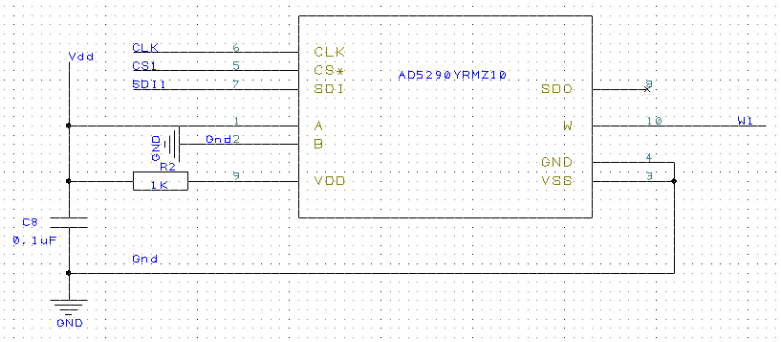


Figure 5.37: Digital Potentiometer AD5290 Circuit Diagram

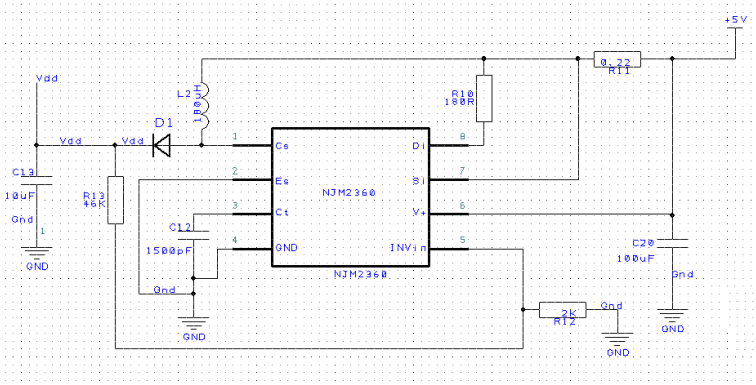


Figure 5.38: Voltage Booster NJM2360 Circuit Diagram

A FT232RL device is connected to the microcontroller in order to establish a real time control between the microchip and mobile terminal. The circuit diagram for FT232RL is shown in Figure 5.39.

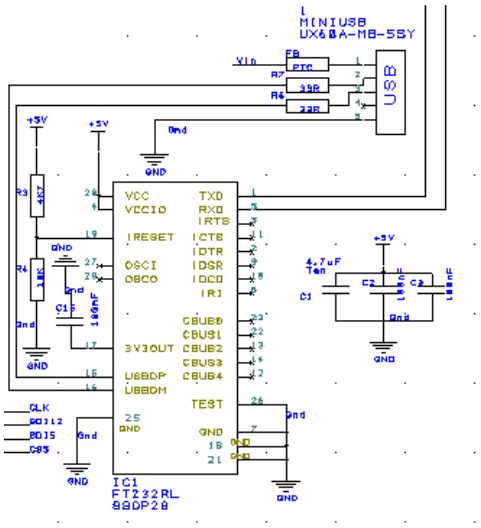


Figure 5.39: FT232RL Circuit Diagram

Furthermore, there are a number of ferrite bead and capacitors in the design to decrease EMI and RFI. The complete circuit diagram is demonstrated in Figure 5.40.

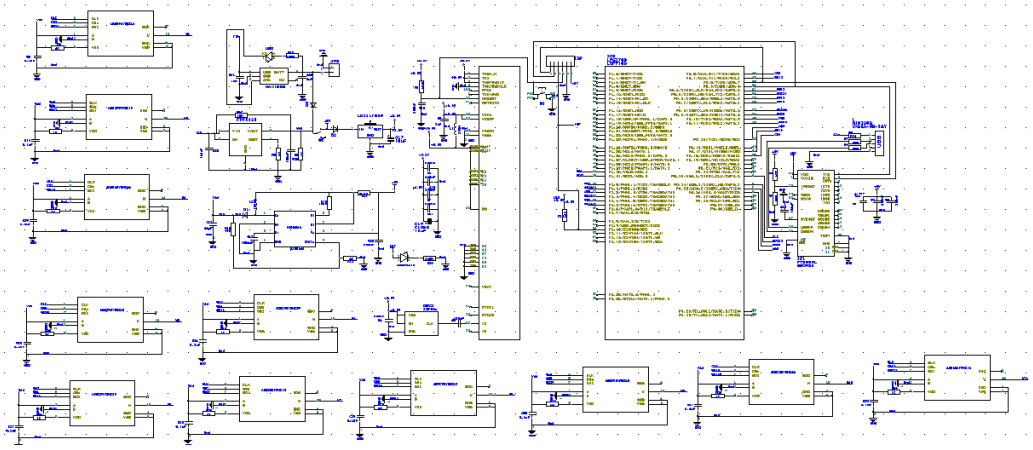
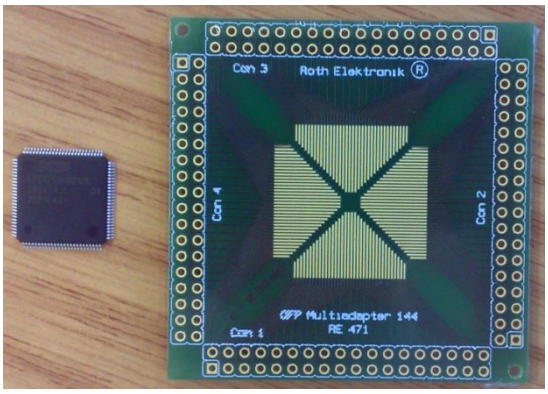


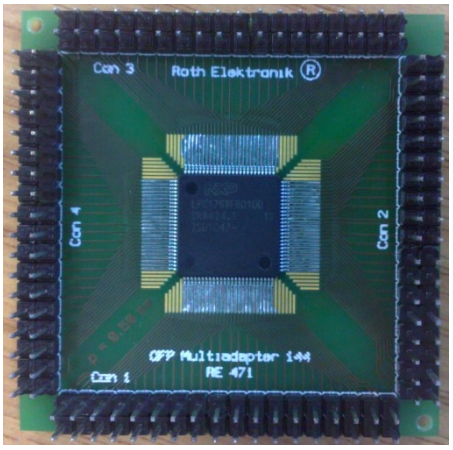
Figure 5.40: Schematic of Control PCB Using LPC1768

5.4.2 Breadboard Testing

Based on the schematic in Figure 5.40, the design was built on prototype boards. Since the microcontroller LPC1768 is only in LQFP100 SMD package and an adapter was used to connect the microchip onto the breadboard, as illustrated in Figure 5.41. The structure in Figure 5.42 is too complicated and the space is not enough to evaluate all of the circuit designs. Another prototype board was utilised to characterise the digital potentiometers and voltage booster, while the original board is only for testing the microcontroller LPC1768 and FT232RL USB module.



(a)



(b)

Figure 5.41: LPC1768 Microcontroller and Adapter

Figure 5.42 and Figure 5.43 display the two separate breadboards to test the microcontroller LPC1768.

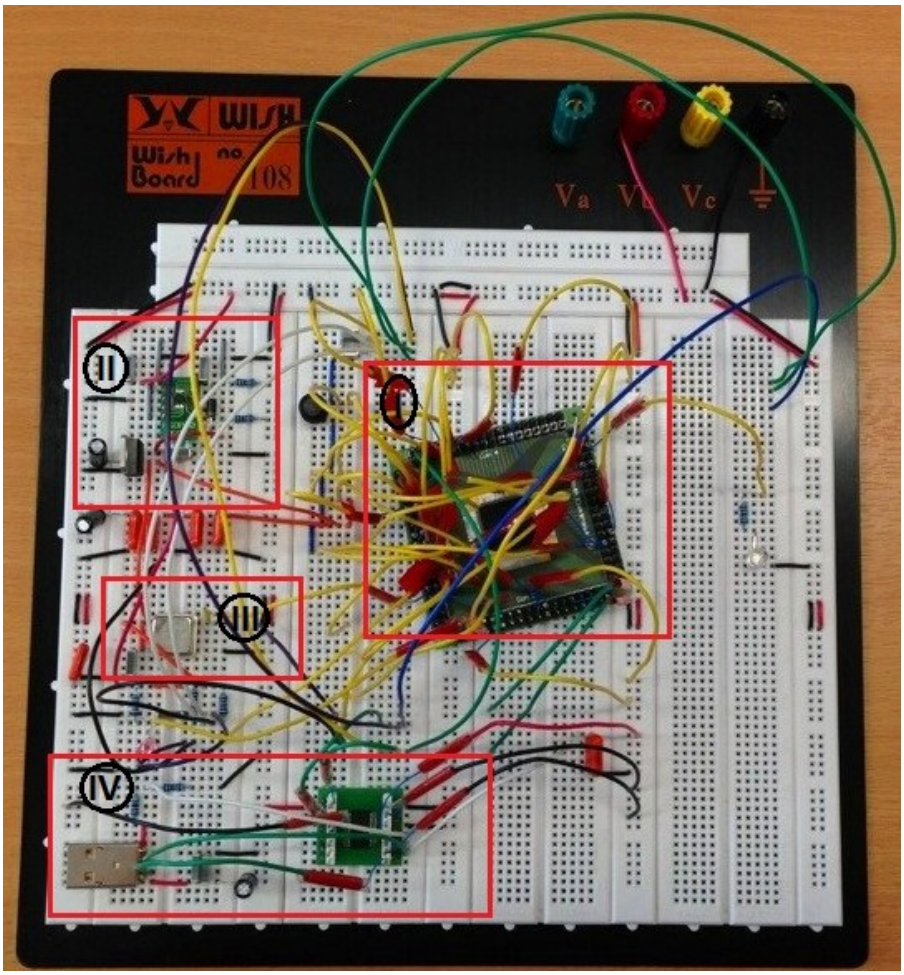


Figure 5.42: Breadboard_I to Test Control Board Using LPC1768

On the Breadboard_I, as shown in Figure 5.42, the microcontroller LPC1768 is placed on an adapter and some jumper wires are connecting the chip to the prototype board. In Section II, some voltage regulators transfer the 5V USB voltage to 3.3V, supplying the microchip, and also protecting the power circuit. Section III demonstrates the oscillator part of LPC1768, with the frequency of 12MHz. The FT232RL USB to UART interface control chip also stands on an adapter and the design circuit has been tested in Section IV. Finally, the Breadboard_I is able to establish the USB communication between the microcontroller LPC1768 and a laptop, which confirms both of the microchip and USB module are working properly.

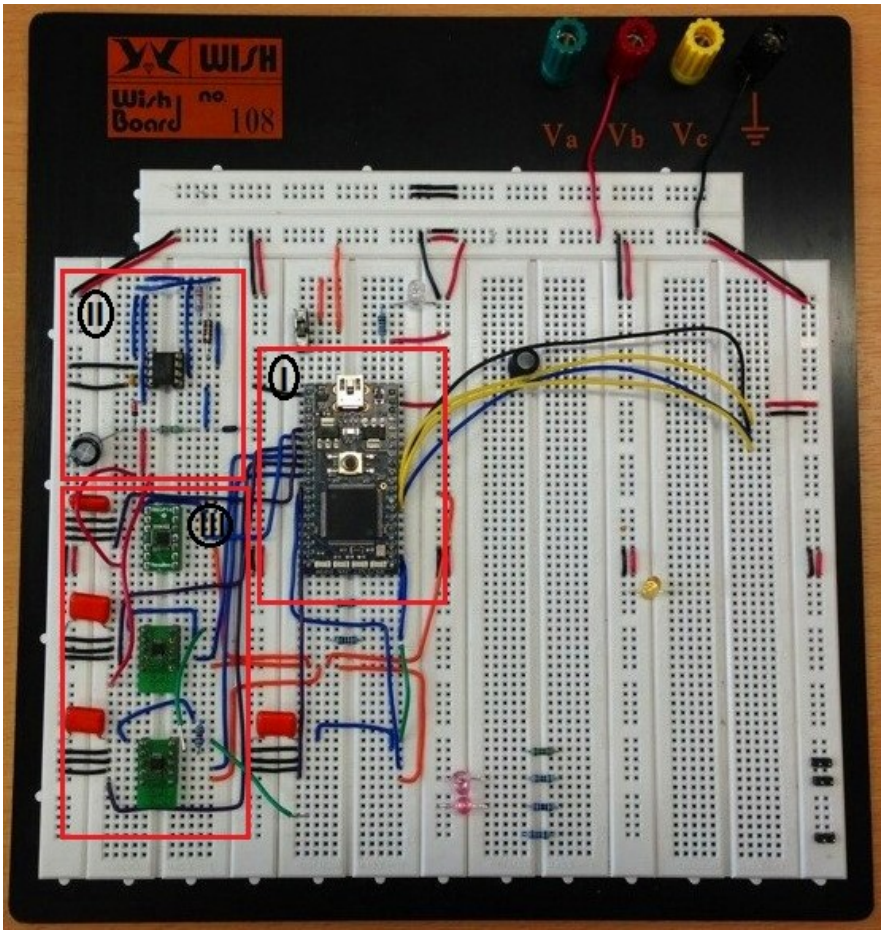


Figure 5.43: Breadboard_II to Test Control Board Using LPC1768

Breadboard_II evaluates the control loop between microcontroller LPC1768 and digital potentiometers. In this implementation, an mbed LPC1768 evaluation kit has been used instead of the microchip. The kit includes LPC1768 chip and also an USB module, which allows evaluation of the high level integration and low power consumptions. The evaluation kit is able to provide the same functions as Breadboard_I. Furthermore, the kit could be used as an ISP programmer to initialise the LPC1768 microchip. In Section II, a voltage booster circuit which increases the voltage from 5V to 30V has been characterised. Digital

potentiometers geometries are shown in Section III. Several decoupling capacitors are placed near the power supply. Finally, the mbed LPC1768 evaluation kit is able to control the digital potentiometers to generate different output voltages.

5.4.3 PCB Fabrication

After breadboard testing, the circuit design is translated in to PCB structure. The PCB geometry is constructed in DesignSparkPCB, which is also an open source integrated package for schematic circuit capture and PCB layout.

This PCB is using four metal layers structure, as presented in Figure 5.44. The top and back layers are for signal tracks and two middle layers are occupied with separate power supply and ground. The multiple layers PCB geometry demonstrates many advantages, including dimension miniaturisation, easy component arrangement, stability, reduced EMI and RFI, and also less complexity.

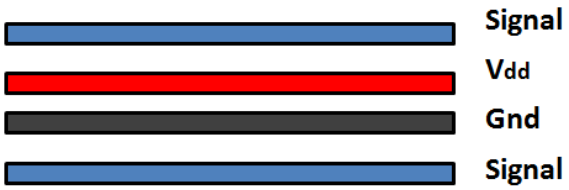


Figure 5.44: Four Layers PCB Structure

Furthermore, from the manufacture, several additional gold and nickel layers are implemented to protect copper layers. The copper layers are used as PCB structures (as shown in Figure 5.44) and 0.5mm FR4 are isolating the metal layers. Figure 5.45 illustrates the detailed design layers.

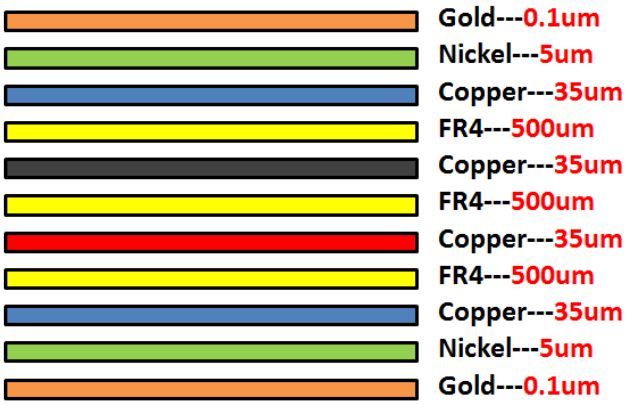


Figure 5.45: Detailed Multi-Layer PCB

There are four design layers in the PCB implementation. All of the components are placed on the top layer, including LQFP100 microcontroller LPC1768, MSOP10 digital potentiometer AD5290, DMP8 voltage booster NJM2360, SSOP28 USB interface FT232RL and several passive components. The second power layer is divided into several sections to arrange different voltage levels, as presented in Figure 5.47, including 3.3V, 5V and 30V. The third layer is a common ground and the bottom layer is occupied by some signal lines. The four layers are connected by vias. In this control board implementation, the track dimensions and pad size are both 0.15mm, for the purpose of miniaturisation. Figure 5.46 and Figure 5.47 display the final PCB layout, with the dimensions of 42mm×92mm.

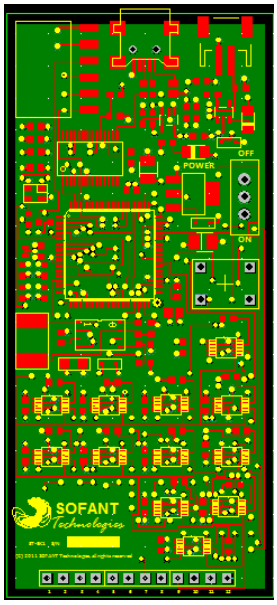
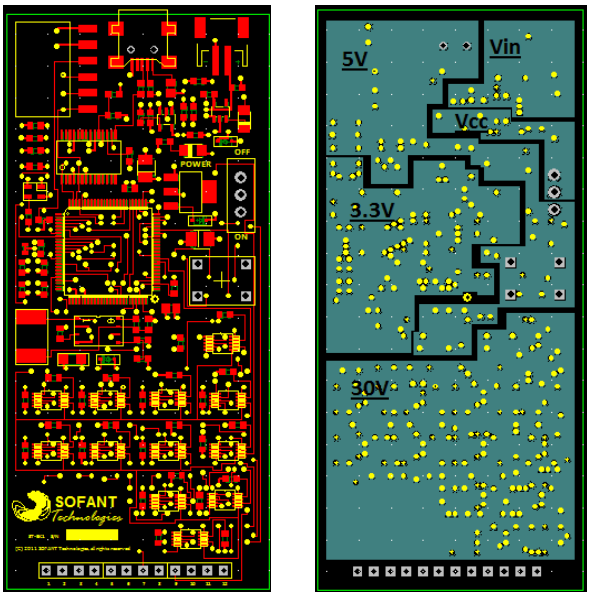
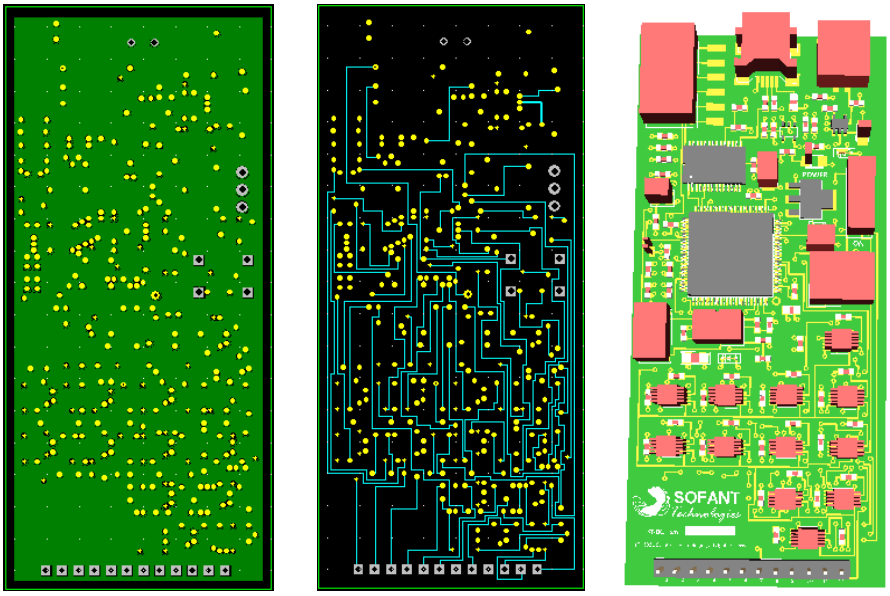


Figure 5.46: PCB Design Using Microcontroller LPC1768



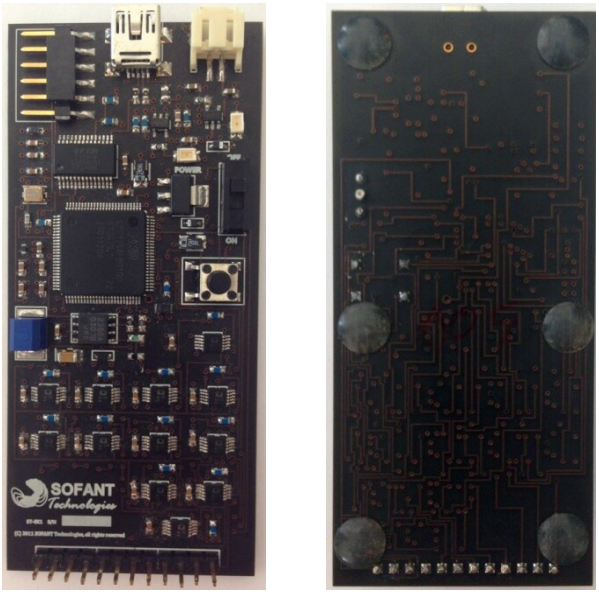
(a) **(b)**



(c) **(d)** **(e)**

Figure 5.47: PCB Layout Using Microcontroller LPC1768 (a) Top Copper Layer (b) Power Layer (c) Ground Layer (d) Bottom Copper Layer (e) 3D View

After carefully design rule check, the PCB structure has also been manufactured by Multi Circuit Board Ltd in Germany [135] and assembled by the technician in the University of Edinburgh. The fabricate layout is presented in Figure 5.48.



(a) **(b)**

Figure 5.48: Fabricated PCB Design Using Microcontroller LPC1768 (a) Top View (b) Bottom View

5.4.4 PCB Evaluation

Similar to the microcontroller PIC18F4550, it is also necessary to initialise the microchip LPC1768 before testing. An mbed LPC1768 evaluation kit is used as an ISP programmer to run the Bootloader code, as displayed in Figure 5.49.

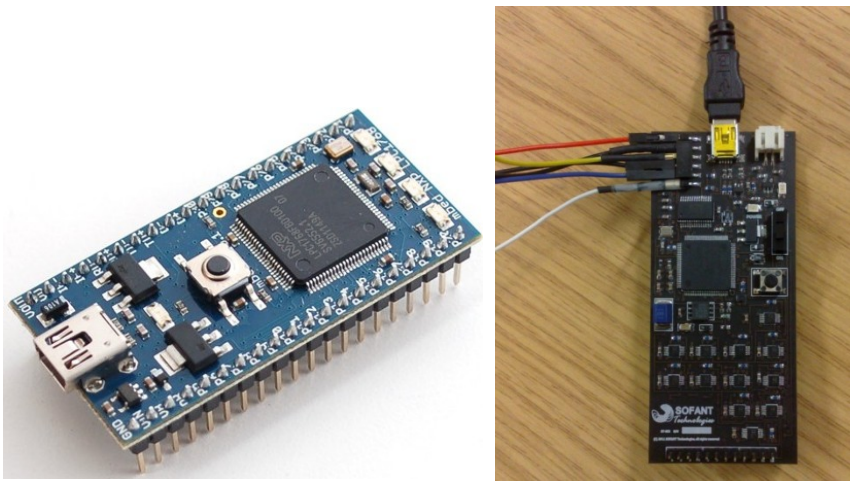


Figure 5.49: Mbed LPC1768 Evaluation Kit and the PCB Under Programmed

To bridge control the pins, and bridge the Bootloader serial port to PC, the mbed LPC1768 evaluation kit is utilised as a serial pass through and to drive the ISP and nReset pins. It can be referred as an mbed ISP. To initialise the microcontroller LPC1768, firstly the nReset pin is set low to reset the device. Then the ISP pin (P0.14) is also set low, to indicate the ISP is intended. By pulling high the nReset, the LPC1768 comes out of reset and samples the ISP pin. If the ISP is low, the Bootloader starts to run. Finally, the Bootloader communicates over a serial connection on UART0: TXD0 = P0.2 = Pin 98, RXD0 = P0.3 = Pin 99. A software Flash Magic is applied to burn the Bootloader into LPC1768 and reads the microchip signature. After this synchronisation, a complete control program is transformed into the microchip and the PCB design is able to control the digital potentiometers in real time.

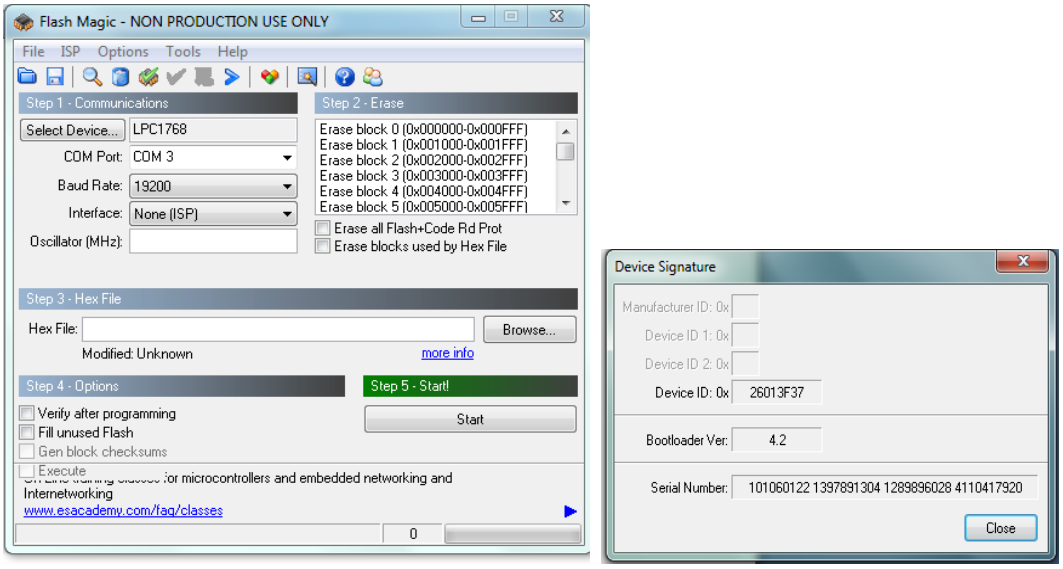


Figure 5.50: Flash Magic to Initialise Microcontroller LPC1768

Different output voltages from 0V to 30V are obtained from the digital potentiometers, which can fully control the phase shifters on smart antenna array to achieve main beam steering. Figure 5.51 demonstrates several stable DC voltages and a square wave output signal is displayed in Figure 5.52.

(a) **(b)** **(c)** **(d)**

Figure 5.51: Stable DC Output Voltage from PCB Design Using Microcontroller LPC1768 (a)0.626V (b)6.56V (c)11.67V (d)29.7V

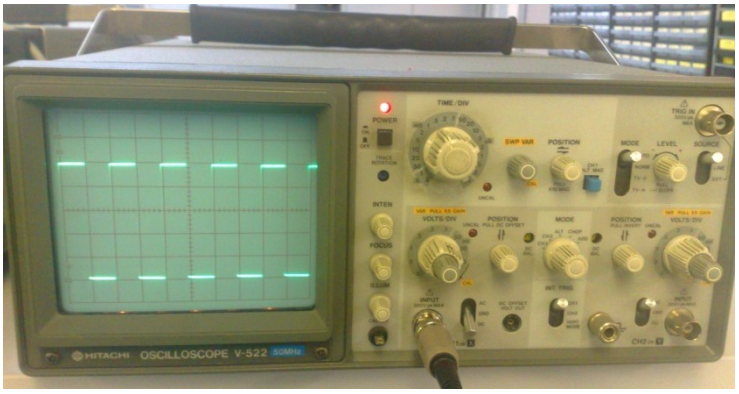


Figure 5.52: Square Wave Output Signal from PCB Design Using Microcontroller LPC1768

5.5 EDUP WiFi Adapter

In the smart antenna hardware control system, an EDUP wireless USB adapter with SMA connector (as shown in Figure 5.53) is used to transfer the WiFi signal into the control terminal. In the current implementation, a laptop is utilised as the control device, since the Window system is more stable to test the whole system. However, both of the two control boards descried in the previous sections are compatible with Android and IOS system.

Figure 5.53: EDUP Wireless USB Adapter with SMA Connector

For the original EDUP wireless USB adapter, it easily connects USB equipment to wireless network for internet or file sharing with minimum power consumption (less than 350mA). It is a compact design and supports Windows 98SE /ME /2000 /XP /Vista/7/8 systems.

In this hardware implementation, the original antenna is replaced by the smart antenna array using SMA connectors. The control PCB provides variable DC voltages to the phase shifters, generating the beam steering. The WiFi signal collected by the WiFi adapter will be transferred into the control terminal, which is a laptop in the current design. Figure 5.54

demonstrates the complete smart antenna system hardware implementation. Some basic algorithms have been included into the control software program to configure the smart antenna array. More descriptions about the software will be discussed in Chapter 6.

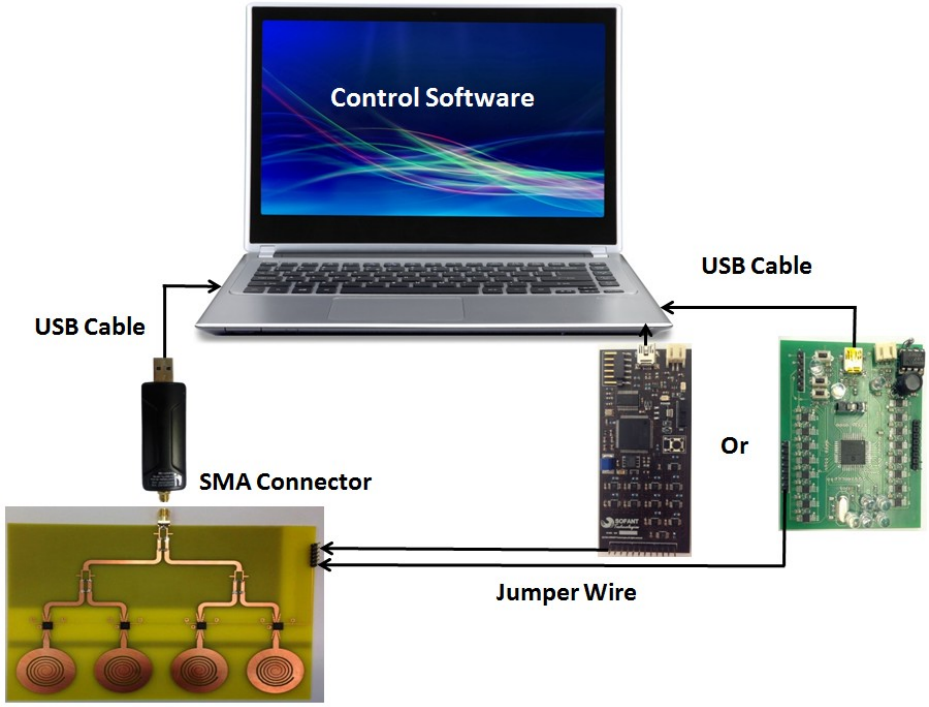


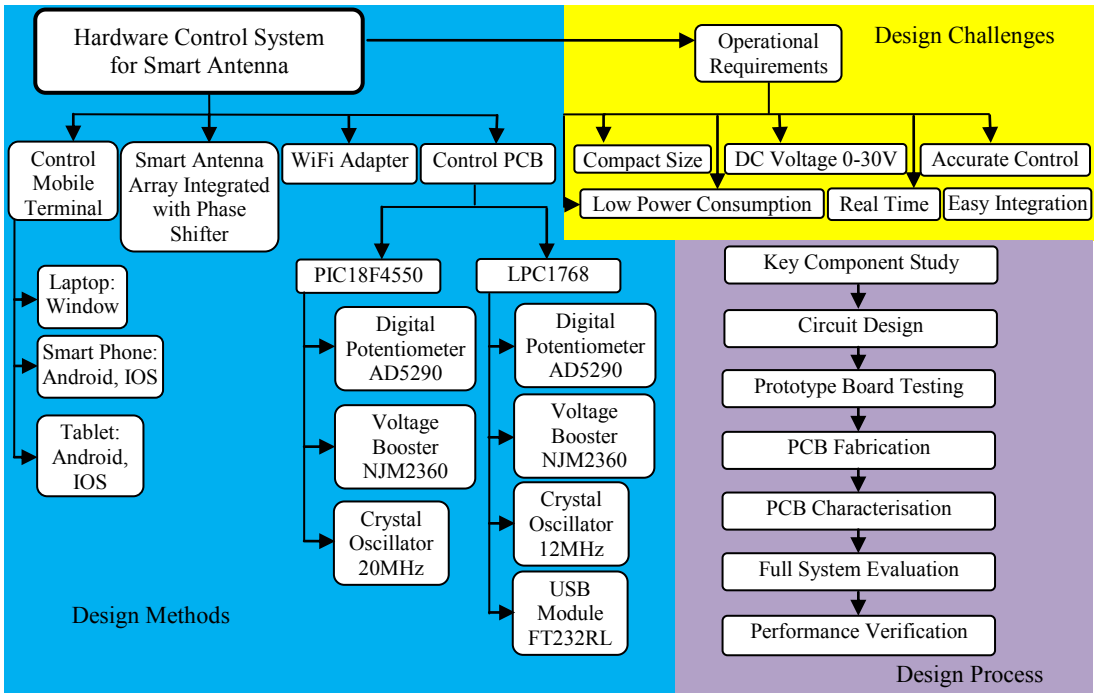
Figure 5.54: Smart Antenna System Hardware Implementation

The hardware control devices presented in this chapter are all compatible with Android and IOS system. The future work will focus on establishing other control loops using Android and IOS mobile devices.

5.6 Summary

In this chapter, the complete hardware control systems for smart antenna array in mobile applications are proposed. The full hardware implementation consists of a smart antenna array integrated with phase shifters, a control PCB containing a microprocessor, a WiFi adapter and a control mobile device. The PCB generates different DC voltages to the phase shifters and achieves the antenna array beam steering. WiFi signal is tested in this design. A WiFi adapter collects the wireless signals and transfers the information into a mobile device. Two separate PCB structures based on microcontroller PIC18F4550 and LPC1768 have been evaluated, respectively. Several digital potentiometers, voltage booster and USB modules are integrated into the PCB layouts. After schematic design and breadboard testing, both of the miniaturised PCB configurations are manufactured and assembled. The two control boards are able to provide required voltages to the analogue phase shifters. Furthermore, the LPC1768 PCB can generate a real time control. Both of the PCB designs are suitable for the hardware control systems.

In the current implementation, a laptop running Windows system is used to evaluate the design due to stability of Windows system. Finally, all of the WiFi signal information including SSID, RSSI, MAC address, channel and vendor at different main beam directions will be distributed on the control software. The software is able to detect signal information and also rotate the main beam to a required direction. Chapter 6 will demonstrate the software design and characterisation.



1. The hardware control system is easy integrated with mobile device.

2. The control PCB is able to provide suitable DC voltages required by the phase shifters.

3. Both of the PCB demonstrates miniaturised dimensions, 57mm×74mm and 42mm×92mm, respectively.

4. The LPC1768 control board is using four-layer PCB design showing compact structure and reduced EMI and RMI. Moreover, real time control between mobile terminal and PCB is achieved.

5. The performance has been confirmed by both of breadboard testing and PCB characterisation.

6. After Bootloader program, both PCB can communicate with laptop through USB connection.

7. The WiFi adapter is able to connect the configured smart antenna array to a laptop and transfer wireless signals.

8. The full hardware control system has been characterised and generates suitable beam steering performance.

Achievements

Figure 5.55: The Investigation of Hardware Control Systems for Smart Antenna

Chapter 6: Software Control Systems for Smart Antenna

6.1 Introduction

The smart antenna array hardware implementation has been discussed in the previous chapter. A PCB containing microcontroller provides suitable DC voltages to the phase shifters and generates the smart antenna array beam steering. The detected WiFi signals are transferred into a mobile device through a WiFi adapter. This chapter will focus on the software design to automatically control the complete smart antenna array system. Since two microcontrollers PIC18F4550 and LPC1768 are used to build control PCBs. There are also two specifically designed software programs developed in order to configure the individual PCB.

For the PIC18F4550, a graphical user interface (GUI) was developed to communicate between a laptop and the control PCB. The GUI sends commands to a Microchip compiler called MPLAB and transfers the control C code into a Hexadecimal (Hex) document. Through the Bootloader program, this Hex code will be copied into the microchip PIC18F4550 and then configures the digital potentiometers to generate variable output voltages. A script using VB is made to link all of the control steps automatically

Several improved versions of the GUI are investigated for the LPC1768 control PCB. By utilising the microcontroller LPC1768, it is able to achieve the real time control, which means there is no need for the Bootloader program again after initialisation. Due to the advantage of LPC1768, two advanced GUIs have been implemented. Both of the GUIs allow the user to detect service set identity (SSID) and received signal strength indicator (RSSI) of WiFi signals surrounding the mobile device. The basic GUI is able to manually configure the

digital potentiometers and display the WiFi information. The control signals are transformed from GUI to a virtual COM port, which is established by the FT232RL, and directly go into the microcontroller. By varying the phase shifter, the beam direction of the antenna array could be changed in order to analyse and optimise the signal strength of the received WiFi signals. Moreover, this chapter provides beta version of an advanced software package, which performs a basic smart antenna adaptive beamforming.

There are mainly four sections in this chapter. Section 6.1 presents the software implementation introduction. GUI designs for PIC18F4550 and LPC1768 are demonstrated in Section 6.2 and Section 6.3, respectively. Finally Section 6.4 summarises this chapter.

6.2 Software Implementation for PIC18F4550 Control System

Figure 6.1 presents the block diagram of software implementation using PIC18F4550 microcontroller.

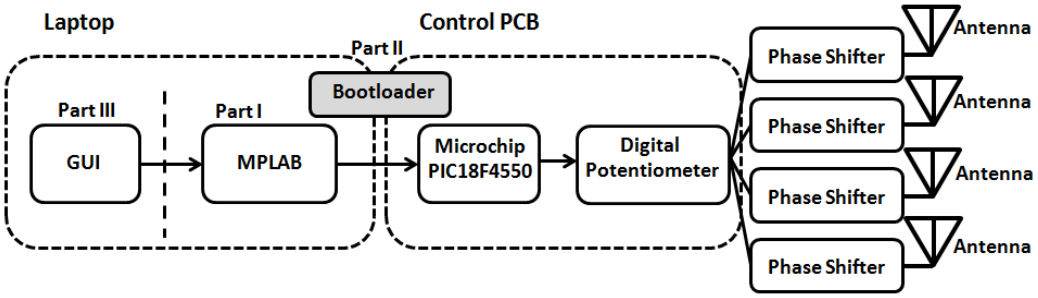


Figure 6.1: Functional Block Diagram for PIC18F4550

The software control system is generally comprised of three parts, as illustrated in Figure 6.1. Part I contains the main algorithm to configure the microchip and digital potentiometers, which simulates the SPI communication. The program is made in C language and compiled in Dev-C++ [137]. Then the C code is transferred into microchip C language to set correct configuration bits, suitable I/O ports and accurate delay time. Finally, MPLAB compiles the program again and generates a hexadecimal document which could be recognised by the microchip.

Part II in the software design is the Bootloader program with the function of communicating between laptop and microcontroller PIC18F4550. After initialisation (discussed in Chapter 5), the hexadecimal code generated by MPLAB is transferred through Bootloader into the microchip.

Finally, Part III is a GUI designed in VC++ for Windows system. The GUI provides two control methods for the phase shifter: manual control and switching control. In the manual

control, some specific values will be sent to the digital potentiometers and generate particular DC voltages. While in the switching control, the output voltages are in square waves. This GUI is used for briefly evaluating the digital potentiometers and phase shifters. More advanced control method will be demonstrated using microchip LPC1768.

6.2.1 Programme PIC18F4550

There are three programs in PIC18F4550: SPI communication, manual control and switching control. These C codes have been evaluated in Dev- C++. Dev- C++ is an integrated development environment (IDE) distributed under the GNU general public license for programming in C and C++. It is bundled with MinGW, a free compiler. The IDE is written in Delphi.

6.2.1.1 SPI Communication

A virtual SPI communication has been established between microcontroller PIC18F4550 and digital potentiometer AD5290. The algorithm is based on the potentiometer's timing diagram.

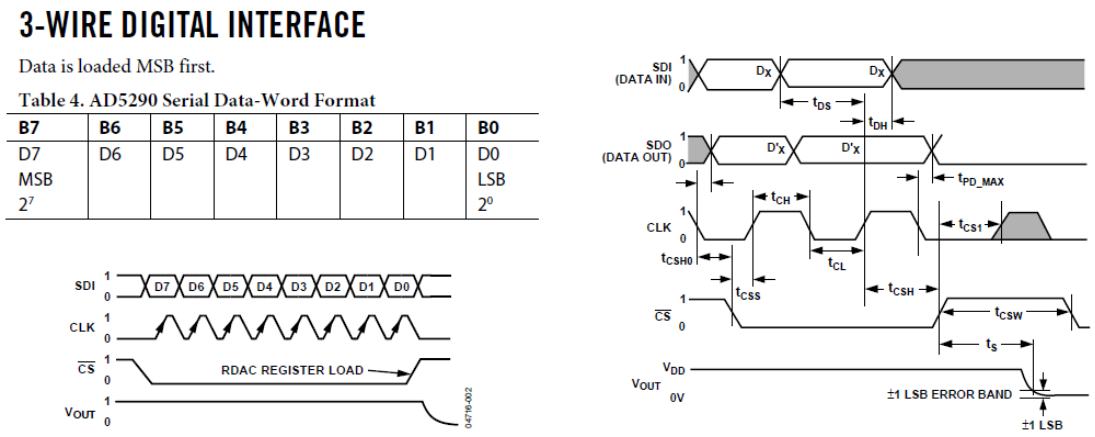


Figure 6.2: Digital Potentiometer AD5290 Timing Diagram [132]

PIC18F4550 controls three signal lines for these digital potentiometers:$\overline{CS}$, CLK, and SDI. Clean transitions are needed by the positive edge sensitive CLK input to avoid clocking incorrect data into the serial input register. When $\overline{CS}$ is low, the potentiometer loads data into the serial register on each positive clock edge and the MSB of the 8-bit serial is loaded first. The data setup and data hold times determine the valid timing requirements. After eight clock cycles, the 8-bit serial input data register transfer the words to the internal RDAC register and the $\overline{CS}$ line returns to logic high. Extra MSB bits will be ignored.

There are two methods to configure the potentiometers: manual control and switching control.

6.2.1.2 Manual Control

In manual control, it is able to control digital potentiometer to generate specific voltage levels to the phase shifter. An example code showing configure only one potentiometer using C in Dev- C++ is as follows:

```
#include <conio.h>
void init();                                    // Declare the  initialisation function
void write_byte(uchar data);                    // Declare the write_byte function
int CLK, dout[8], cs_bar;
void init()
{       cs_bar=1;                               // Before data transfer, CS should be logic high
        CLK=0;          }                       // Initialise the clock signal
int main()
{       uint i,t;
        for (i=1;i>0;i--)                       // Just run the main function once
        {       init();
        write_byte(0xfb);//11111011,251         //Write data "251" into the memory
        }
        for(t=0;t<8;t++)                        //Show the data written into the memory one by one
 {  printf("%d",dout[t]); }
    getch();
     return 0;                  }
void write_byte(uchar data)
{       uint i;
        uchar temp;
        cs_bar=0;                               // Data starts to transfer, CS should be logic low
        for (i=0;i<8;i++)                       // 8-bit data needs the transfer function 8 times
        {       CLK=0;                          // CLK goes to low to simulate a clock signal
                temp=data&0x80;                 // Check this bit is 0 or 1
                if (temp==0x80)                 // If this bit is 1
                        dout[i]=1;              // The output data should be logic high
                else                            // If this bit is 0
                        dout[i]=0;              // The output data should be logic low
                        CLK=1;                  // CLK returns to high to finish a clock cycle
        data=data<<1;   }   // Left shift the data to write next bit into the memory
        cs_bar=1;                       }   //After the function runs for eight times,
                                            // all of the eight bits have been
                                                    // transferred into the memory,
                                  //  CS returns to high and finish the write_byte function
```

This program is exactly following the timing diagram provided in Figure 6.2. The purpose of this code is to write an 8-bit data into the microcontroller and then transfer the data into a digital potentiometer bit by bit on positive clock cycle. The delay time is ignored to simplify the program. If a number 251 is written into the microchip PIC18F4550, its output to the

digital potentiometer should be “11111011”. A Printf function is added into the C code, so the result of 1111011 is showing on the screen, as presented in Figure 6.3.

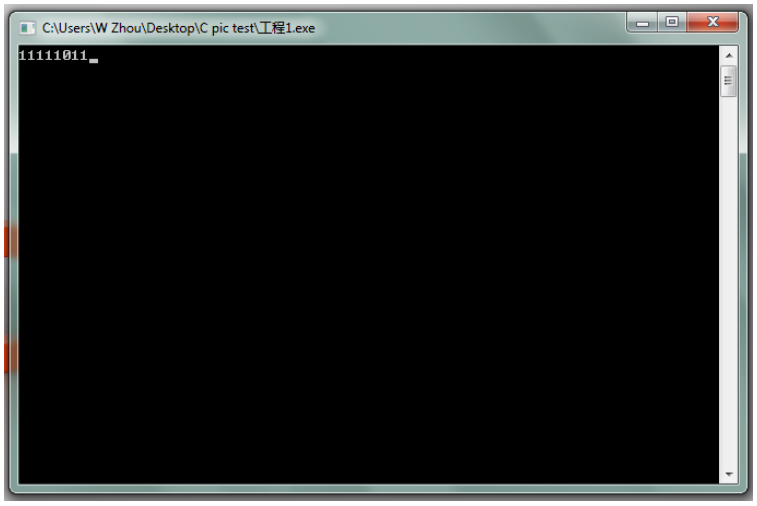


Figure 6.3: C Code Result for SPI Communication

From the results in Figure 6.3, the virtual SPI communication has been successfully established between PIC18F4550 and the digital potentiometers. The algorithm is fully matching the timing diagram. Then, the C code is re-written in MPLAB to configure the microchip I/O ports. MPLAB integrated development environment (IDE) is an integrated toolset for development of embedded applications employing Microchip's PIC and dsPIC microcontrollers [136]. The following example demonstrates using PIC18F4550 configure only one potentiometer in MPLAB.

```
#include <p18f4550.h>                                   // Include the 18f4550 head file
#define REMAPPED_RESET_VECTOR_ADDRESS 0x1000 // Memory from 0x1000
#define cs_bar LATCbits.LATC1    // Set PIN RC1 as CS
#define dout LATAbits.LATA0      // Set PIN RA0 as output data
#define CLK LATCbits.LATC2       // Set PIN RC2 as CLK
extern void _startup (void);       // Set start up
#pragma code REMAPPED_RESET_VECTOR = REMAPPED_RESET_VECTOR_ADDRESS
void _reset (void)
{          _asm goto _startup _endasm          }
#pragma code                        // Set the suitable configuration bits
void delay(uint x);
void init();
void write_byte(uchar data);
void delay(uint x)                  // Make a delay function
{          uint a,b;
           for(a=x;a>0;a--)
                      for(b=275;b>0;b--); }   // After simulation, x represent x milliseconds
void init()
{          TRISAbits.TRISA0=0;    // Set PIN RA0 as an output, for the output data
           TRISCbits.TRISC1=0;    // Set PIN RC1 as an output, for CS
           TRISCbits.TRISC2=0;    // Set PIN RC2 as an output, for CLK
           cs_bar=1;                  // Before data transfers, CS should be logic high
```

```
        CLK=0;   }                  // Initialise the clock signal
void main()
{       uint i;
        for (i=1;i>0;i--)           // Run the main function once
        init();
        write_byte(0x84);//10000100,132   }//Write 132  into the microcontroller's memory
void write_byte(uchar data)
{       uint i;
        uchar temp;
        cs_bar=0;                  // Data starts to transfer, CS should be logic low
        Nop();                      // Make a delay for  CS
        for (i=8;i>0;i--)          // 8-bit data needs the transfer function 8 times
        {       CLK=0;         // CLK goes to low to simulate a clock signal
                temp=data&0x80;    // Check this bit is 0 or 1
                if (temp==0x80)       // If this bit is 1
                        dout=1;     // The output data should be set as logic high
                else                    // If this bit is 0
                        dout=0;    // The output data should be set as logic low
                Nop();                 // Wait for the data processing
                CLK=1;                 // CLK returns to high to finish a clock cycle
                Nop();                // Wait for the clock signal
                data=data<<1;     }  // Left shift the data to write next bit into the memory
                CLK=0;                              // After data transfers, CLK returns to 0
        cs_bar=1;                        //After the function runs for eight times,
                                         // all of the eight bits have been
                                        // transferred into the memory,
                        }              //  CS returns to high and finish the write_byte function
```

Some I/O ports of PIC18F4550 are utilised as $\overline{CS}$, CLK, and SDI signals to simulate the SPI communication. In the code, data 132 is transferred into the digital potentiometer.

According to the Equation 6.1:

$$V_W(D) = \frac{D}{256} \times V_A + \frac{256-D}{256} \times V_B \quad (6.1)$$

When D is 132 in decimal, it is 10000100 in binary and 84 in hexadecimal. $V_W(D)$ = 15.47 V

In MPLAB, after compiling, the code is translated into a hexadecimal document. Bootloader program is used to send the ".hex" file into PIC18F4550. After reseting the control PCB, a voltage of 15.47V is measured at the terminal W of the digital potentiometer, which could configure the phase shifters in the smart antenna array.

Figure 6.4: Measurement Result of PIC18F4550 Manual Control

Figure 6.4 illustrates the measurement of PIC18F4550 manual control for single digital potentiometer, which matches the calculation. Then the algorithm is extended to configure all of the sixteen digital potentiometers together on the control PCB. Finally the PIC18F4550 manual control program will work with the manual control GUI to control the smart antenna array beam steering.

6.2.1.3 Switching Control

In switching control, the target is to generate square waveforms from the digital potentiometers, as presented in Figure 6.5.

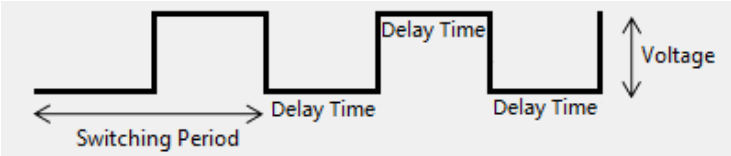


Figure 6.5: Square Waveforms from Switching Control

The fundamental algorithm is similar to the manual control, however, in this implementation, the delay time is very important. In the microchip C code, a delay time has been added after sending the 8-bit values and a for-loop is included in the main function to judge the delay time.

```
void delay(uint x)
{       uint a,b;
        for(a=x;a>0;a--)
        for(b=275;b>0;b--);}                    // Delay function
```

The value of b determines the accuracy of delay time, which has been simulated in MPLAB, as illustrated in Figure 6.6.

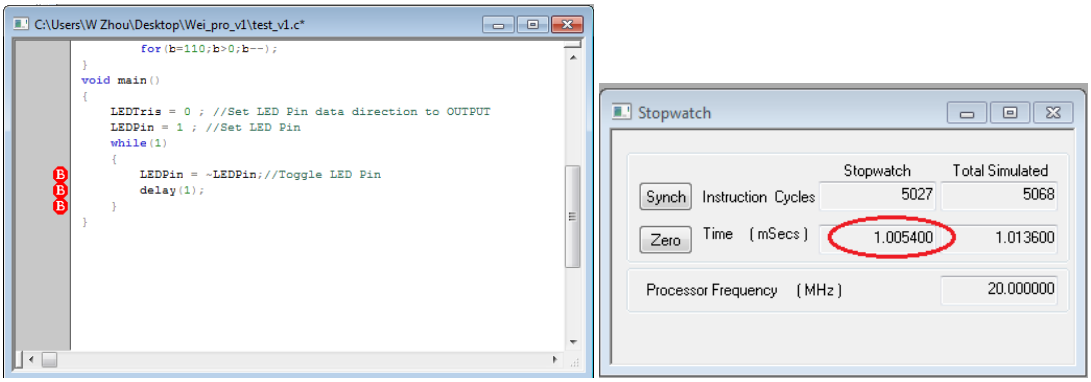


Figure 6.6: Delay Time Simulation in MPLAB

In Figure 6.6, several breakpoints (Red B) are set at the beginning and end of the delay function. The Stopwatch in MPLAB is used to observe the running time. After simulations and optimisations, the value of b is set at 275 and x equals to 1. The program will run for 1 millisecond (Red cycle), and later by controlling the value of x, the required milliseconds can be achieved.

The simulated delay time function has been added into the switching control main code and transferred into the microcontroller PIC18F4550. Figure 6.7 demonstrates the measured results by an oscilloscope. In this code, the DC voltage is switching between 0 and 12V with a delay time of 9 milliseconds.

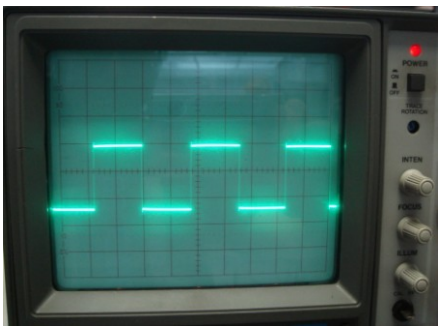


Figure 6.7: Measured Result of the Switching Control

6.2.2 Graphical User Interface for PIC18F4550

A graphical user interface is built to automatically configure the PIC18F4550 control PCB. Figure 6.8 shows the communication loop between GUI and microchip.

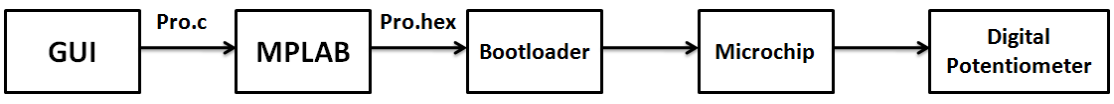


Figure 6.8: Control Loop between GUI and Microchip

The control commands from GUI will automatically generate a C code. MPLAB transfers the C code into a hexadecimal document which will be sent into the microchip through Bootloader. Finally the microcontroller configures the digital potentiometers to provide suitable DC voltages to the phase shifter in smart antenna array.

Figure 6.9 shows the GUI main interface for PIC18F4550. Two control methods are provided according to the algorithm described in Section 6.2.1.

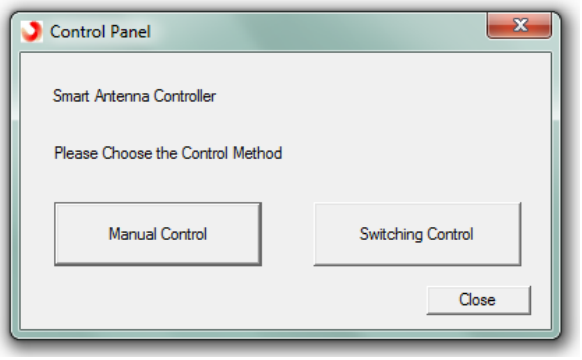


Figure 6.9: GUI Main Window for PIC18F4550

6.2.2.1 Manual Control

The GUI is made using Microsoft Visual Studio 2010 [138], which is a commercial integrated development environment (IDE) product engineered by Microsoft for the C, C++, and C++/CLI programming languages. In this software program, the main section is written in C++.

The manual control interface is illustrated in Figure 6.10.

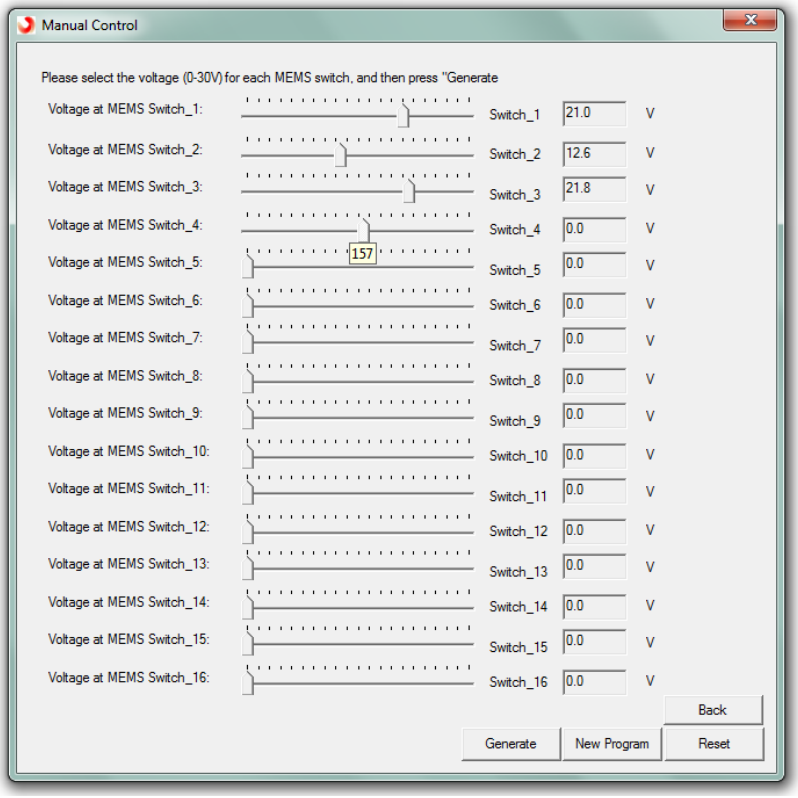


Figure 6.10: Manual Control GUI for PIC18F4550

In manual control GUI, there are sixteen sliders to control the digital potentiometers, with the voltage level from 0V to 30V in the precision of 0.1V. The scale is above the slider and there stands a number showing the position. By using the scales and sliders, it is able to configure the digital potentiometers quickly and accurately. The text boxes are on the right demonstrating the output voltages. The required voltage of the phase shifter is from 0V to 13V, which can be fully covered by this implementation. After pressing the Generate button, a script written in VB will send these sixteen voltage values into a predefined C code. Then MPLAB reads this C code, compiles the program and transfers it into a hexadecimal file. Finally Bootloader burns the .hex document into the microcontroller PIC18F4550 and control the digital potentiometers. By using the manual control GUI, it is able to manually configure the phase shifters in the smart antenna array and estimate the beam steering.

6.2.2.2 Switching Control

In switching control, the digital potentiometers will generate square waveforms to the phase shifters and the main beam of the smart antenna will switch just between two directions. It is a basic evaluating method for the smart antenna array.

Figure 6.11 shows the output waveforms. The voltage levels are different but they share an identical switching period. The software interface is displayed in Figure 6.12.

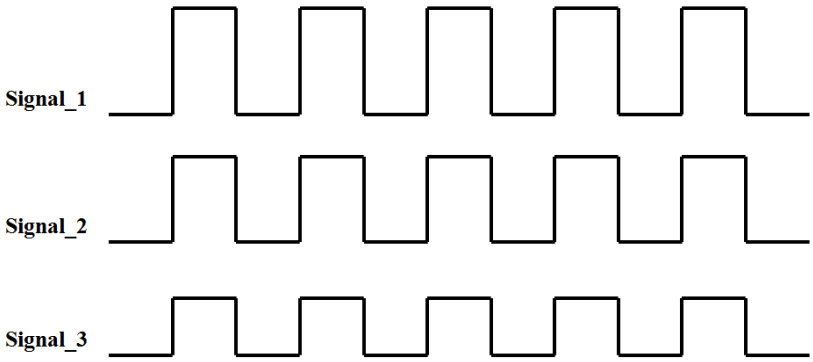


Figure 6.11: Output Square Waveforms

Same as the manual control, for the square waveform, the voltage range is from 0V to 30V with a precision of 0.1V. There are scales and positions of the sliders added into the GUI to achieve the accurate control. Furthermore, in this switching control application, the delay time has been added into the design to setup a switching period. Also, a script is made to automatically link the GUI to MPLAB, Bootloader and PIC18F4550.

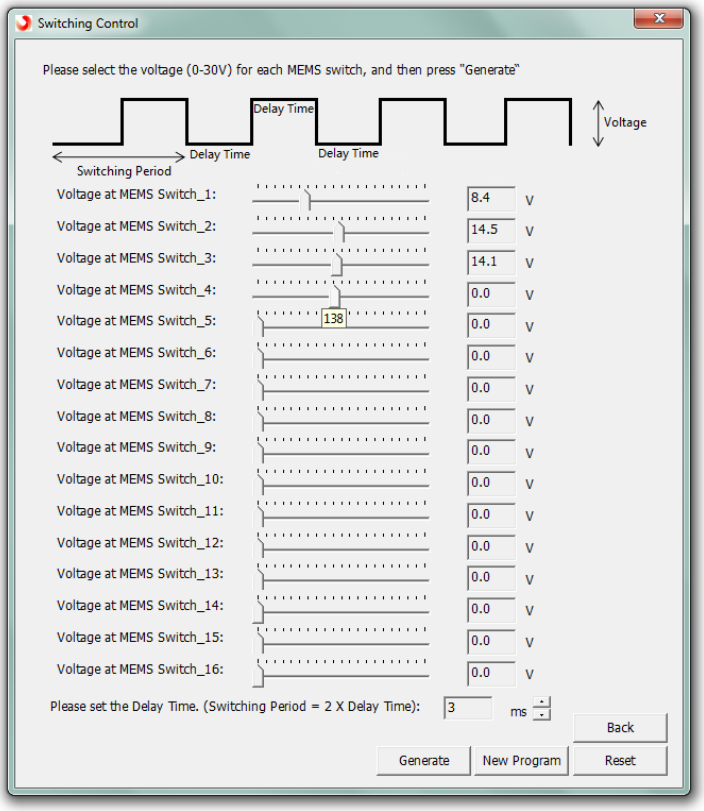


Figure 6.12: Switching Control GUI for PIC18F4550

Based on research and investigation, it is noted that PIC18F4550 is difficult to achieve the real time control, which means the Bootloader program cannot be ignored during the control loop. The script built in the GUI is able to generate an automatic control but each command

requires a long data transfer period and the program is not stable. The basic control methods (manual control and switching control) have already made the algorithms complicated. So the GUI of PIC18F4550 is only used to generally estimate the digital potentiometers and the phase shifters. More advanced software programs are developed using the microcontroller LPC1768.

6.3 Software Implementation for LPC1768 Control System

6.3.1 Programme LPC1768

Figure 6.13 shows the block diagram for programming LPC1768. The microchip control code is written in C language and compiled by an online compiler provided by mbed, as illustrated in Figure 6.14. The compiler generates a binary document. A DOS based program transfers the binary file into a hexadecimal code. Flash Magic burns the .hex file into the microcontroller LPC1768, as demonstrated in Figure 6.15 and Figure 6.16. Flash Magic is a PC tool for programming flash based microcontrollers from NXP utilising a serial protocol [139]. An ISP programmer is communicating between laptop and control PCB.

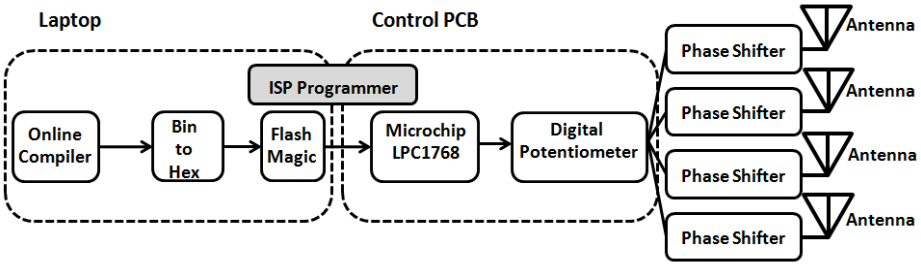


Figure 6.13: LPC1768 Programming Block Diagram

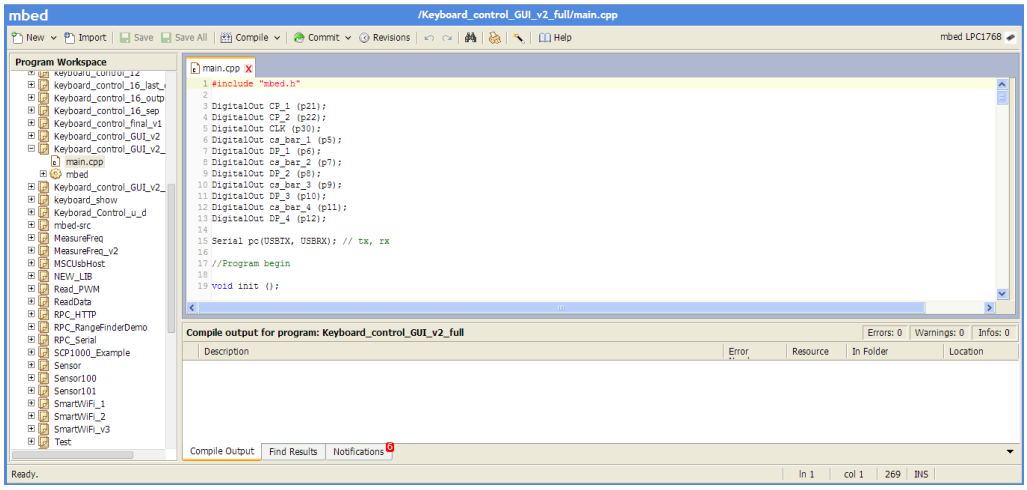


Figure 6.14: LPC1768 Online Compiler

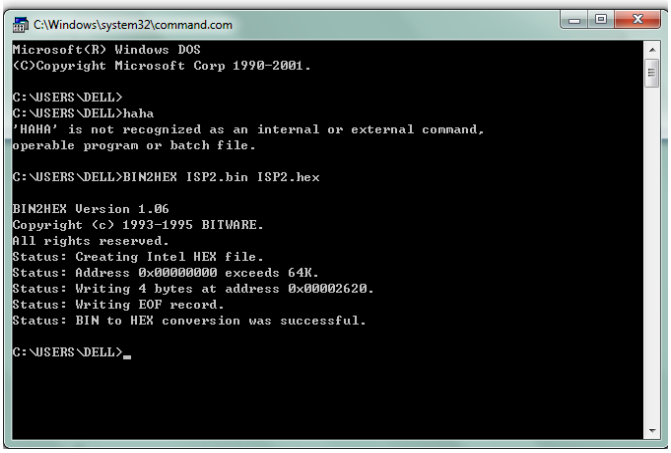


Figure 6.15: LPC1768 BIN to HEX Transformer

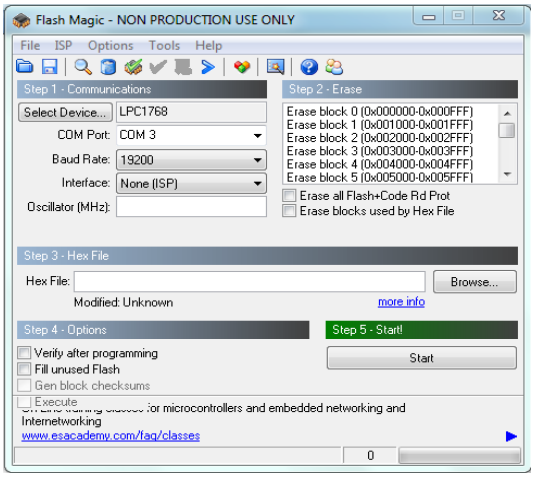


Figure 6.16: Flash Magic to Program LPC1768

Compared to PIC18F4550, the microchip LPC1768 is more advanced. After initialising the microcontroller, as shown in Figure 6.13, the compiler, transformer, flash magic and ISP programmer are not required in the final communication. When the configuration bits and algorithms have been setup correctly, the LPC1768 will generate a virtual COM port (by the FT232RL chip), which can be recognised by a terminal emulator named Tera Term [140]. The GUI for LCP1768 can directly control the digital potentiometers through Tera Term. It is able to achieve the real time control. The communication block diagram for LPC1768 is presented in Figure 6.17.

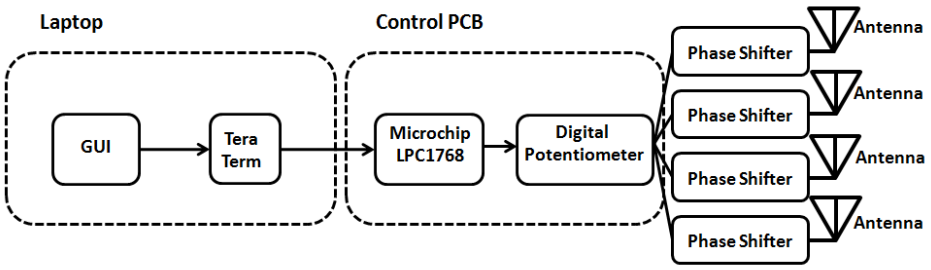


Figure 6.17: Real Time LPC1768 Communication Block Diagram

Similar to PIC18F4550, the LPC1768 also controls the digital potentiometers using virtual SPI communication, and with the same algorithms in Section 6.2.1.

6.3.2 Graphical User Interface for LPC1768

There are also two GUI developed for LPC1768: Manual Control and Automatic control. Both of the software programs are able to detect service set identity (SSID) and received signal strength indicator (RSSI) of WiFi signals surrounding the laptop.

The GUI software can be installed on a computer with the following minimum requirements:

- PC Compatible with Windows XP/7/Vista/ 8 – 32 or 64 bit
- At least 2 free USB Ports

Usually Windows 7 and later versions will recognise the LPC1768 microcontroller automatically and there will be no need to install the drivers. However, for previous Windows version, two drivers for FT232RL microchip and the WiFi adapter are required to be installed.

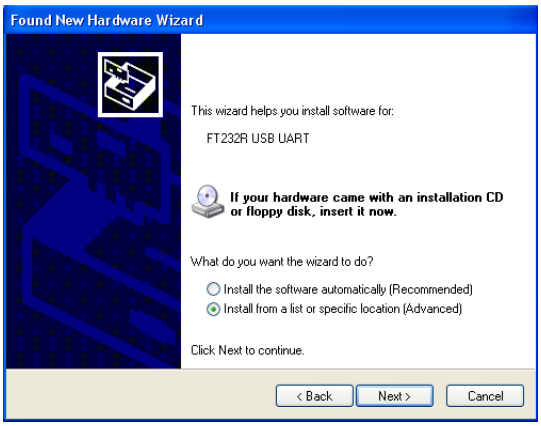
6.3.2.1 Driver Installation

The driver for LPC1768 has been written into FT232RL microchip and the program will automatic start when the USB port is connected to a PC running Windows. Figure 6.18 presents the steps to install the FT232RL.

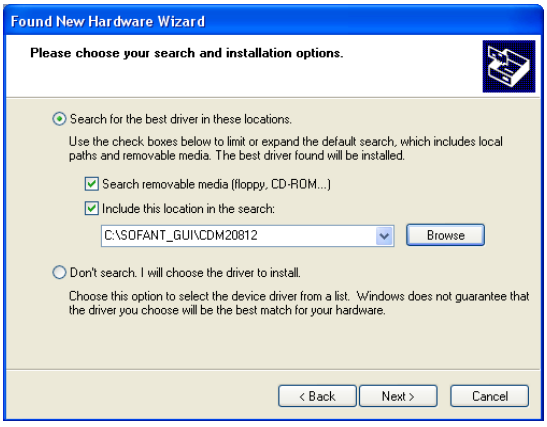

Found New Hardware
FT232R USB UART

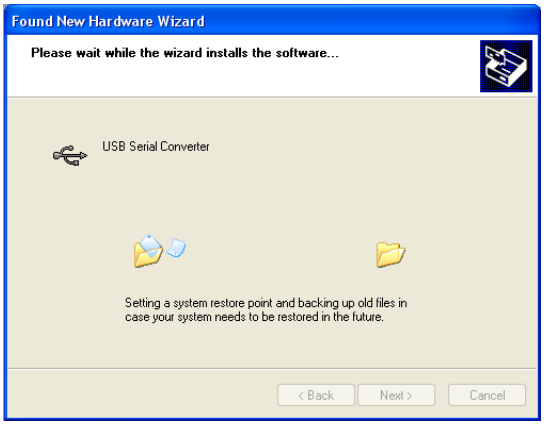
(a) **(b)**


Found New Hardware Wizard
Welcome to the Found New Hardware Wizard
Windows will search for current and updated software by looking on your computer, on the hardware installation CD, or on the Windows Update Web site (with your permission).
Read our privacy policy
Can Windows connect to Windows Update to search for software?
Yes, this time only
Yes, now and every time I connect a device
No, not this time
Click Next to continue.
< Back
Next >
Cancel

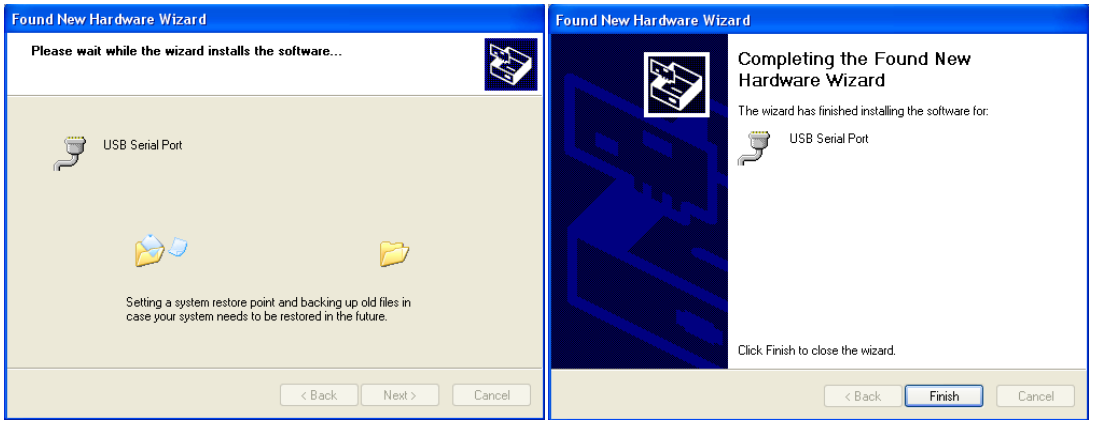

Found New Hardware Wizard
This wizard helps you install software for:
FT232R USB UART
If your hardware came with an installation CD or floppy disk, insert it now.
What do you want the wizard to do?
Install the software automatically (Recommended)
Install from a list or specific location (Advanced)
Click Next to continue.
< Back
Next >
Cancel

(c) **(d)**


Found New Hardware Wizard
Please choose your search and installation options.
Search for the best driver in these locations.
Use the check boxes below to limit or expand the default search, which includes local paths and removable media. The best driver found will be installed.
Search removable media (floppy, CD-ROM...)
Include this location in the search:
C:\SOFANT_GUI\CDM20812
Browse
Don't search. I will choose the driver to install.
Choose this option to select the device driver from a list. Windows does not guarantee that the driver you choose will be the best match for your hardware.
< Back
Next >
Cancel


Found New Hardware Wizard
Please wait while the wizard installs the software...
USB Serial Converter
Setting a system restore point and backing up old files in case your system needs to be restored in the future.
< Back
Next >
Cancel

(e) **(f)**



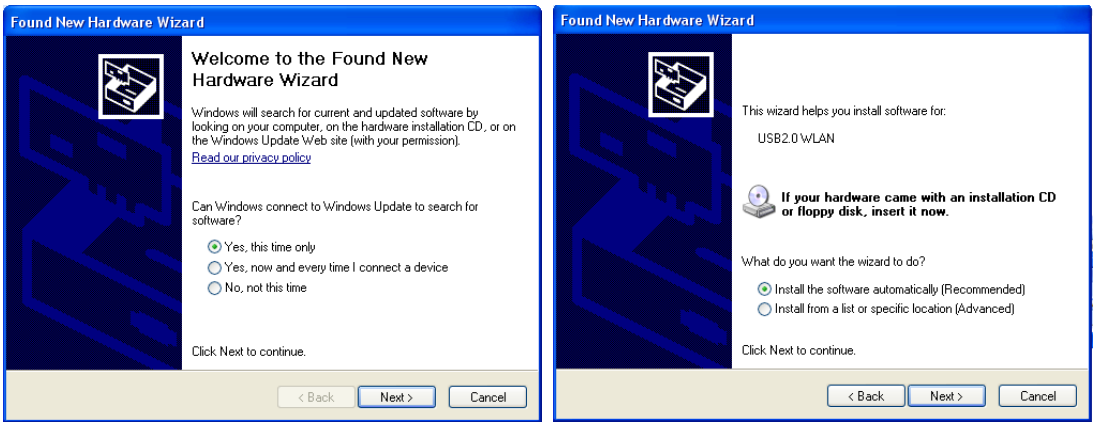
(g) **(h)**

Figure 6.18: FT232RL Diver Installation

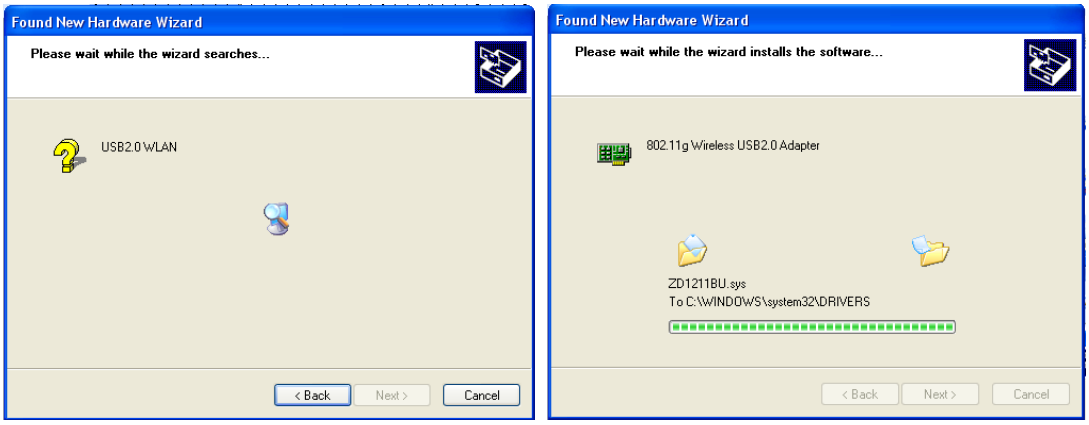
FT232RL provides a USB serial port which can be recognised by Windows system. The laptop communicates to LPC1768 through FT232RL USB to UART.

The installation steps for WiFi adapter are illustrated in Figure 6.19.

(a) **(b)**



(c) **(d)**



(e) **(f)**

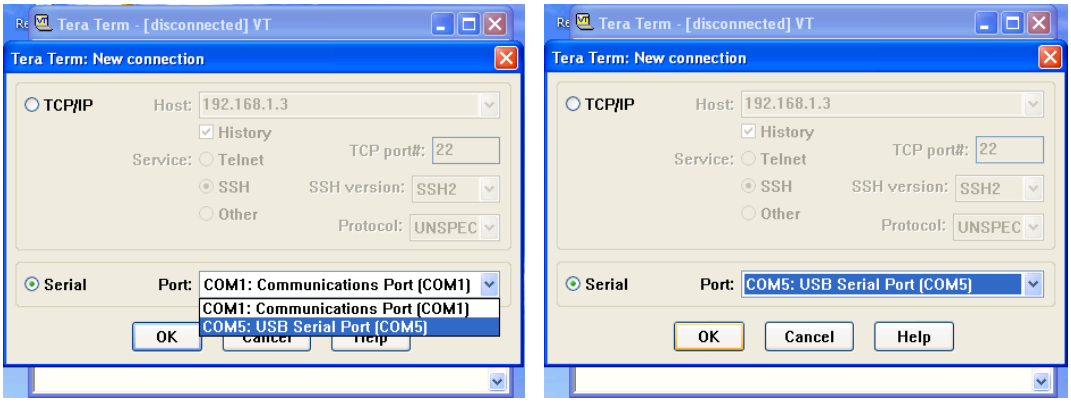
(g) **(h)**

Figure 6.19: WiFi Adapter Driver Installation

After installation, the WiFi adapter will replace the laptop's original WiFi antenna and the smart antenna array will be used to detect WiFi signals around the laptop. The following sections will focus on the GUI design to configure the smart antenna array beam steering.

6.3.2.2 Manual Control

As discussed in Section 6.3.1, the GUI sends the control commands into Tera Term and then directly transfers to the microprocessor LPC1768. Figure 6.20 presents the Tera Term software which makes LPC1768 a virtual COM port to the laptop.



(a) **(b)**

Figure 6.20: Tera Term Connection Setup

Figure 6.21: Manual Control GUI Start Screen for LPC1768

Figure 6.21 presents the GUI start screen developed for microprocessor LPC1768. This software program is written in VC++ and C#. After clicking the Basic SmartWiFi button, the main interface will appear, as displayed in Figure 6.22.

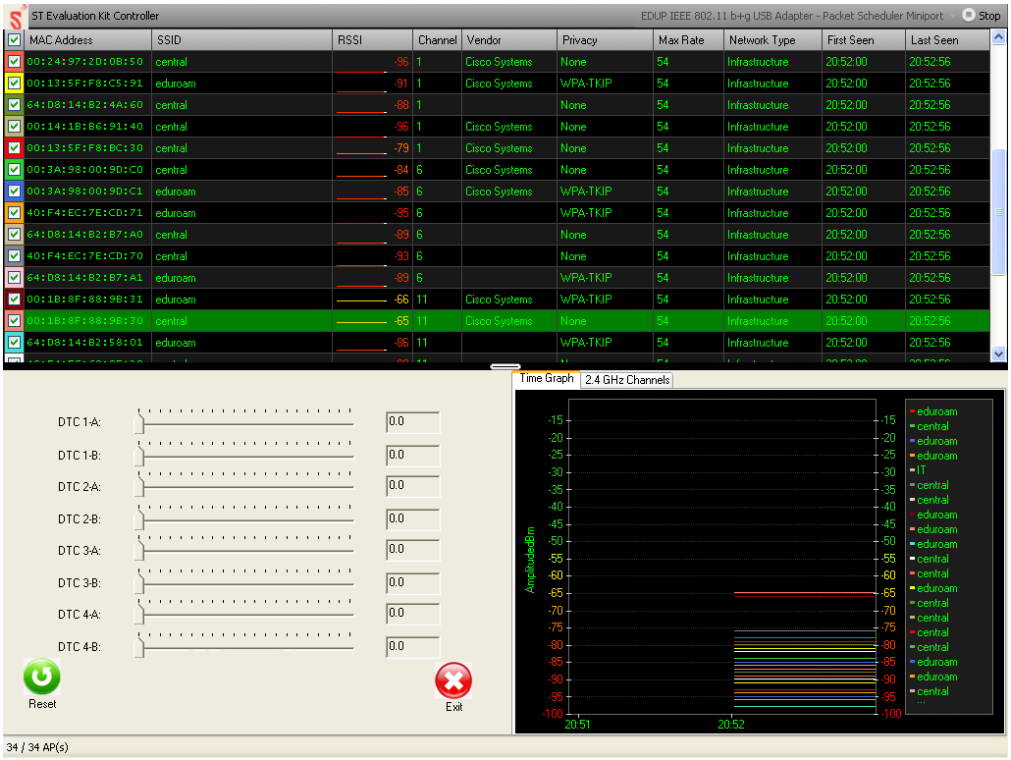


Figure 6.22: Manual Control GUI Main Screen for LPC1768

In the upper right corner, there is a drop down menu item to select the wireless adapter for evaluation. In the smart antenna array system, an EDUP wireless adapter is used in the implementation. So in the menu, "**EDUP IEEE 802.11 b+g USB Adapter – Packet Scheduler Miniport**" is selected.

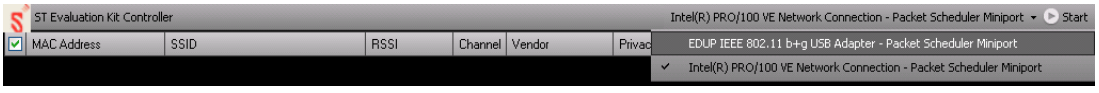


Figure 6.23: Wireless Adapter Selection for LPC1768

There are generally three sections in the software design. On top is the main window showing MAC Address, SSID, RSSI, Channel, Vendor, Privacy, Max Rate, Network Type and Detected Time for all of the WiFi signals around a laptop, as demonstrated in Figure 6.24.

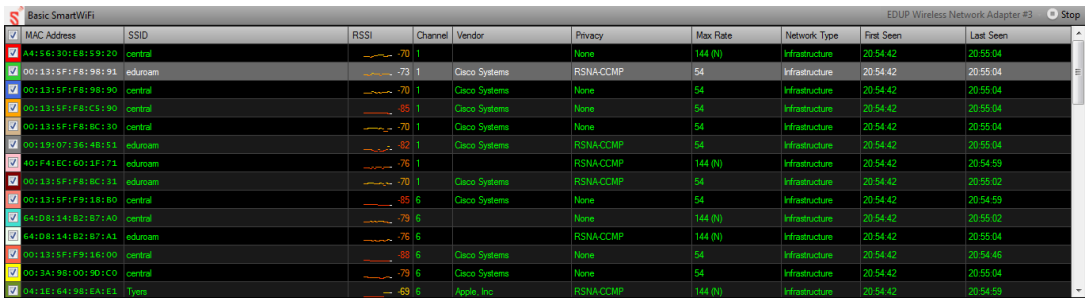
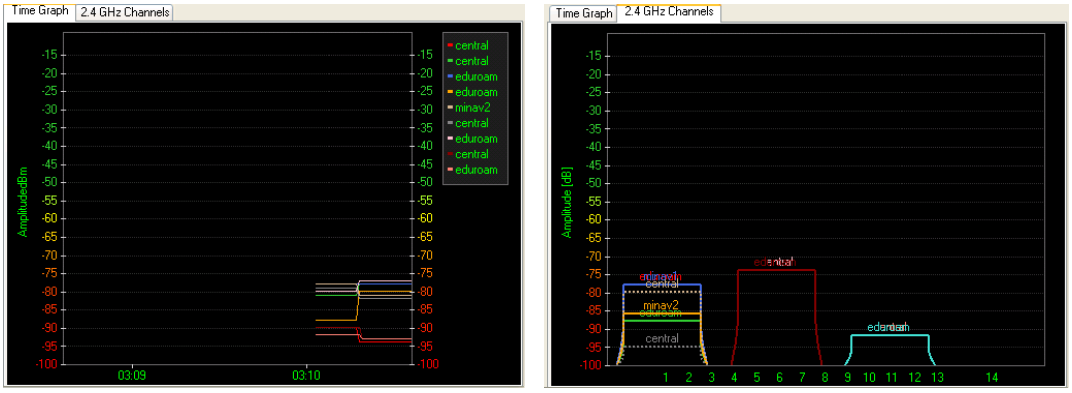


Figure 6.24: WiFi Information of the GUI for LPC1768

On the bottom right, a window is drawing all of the real time signal strength curves (in dBm) for the WiFi signals (as shown in Figure 6.25(a)). Another tab in this window illustrates the signal amplitudes in different channels.



(a) **(b)**

Figure 6.25: (a) WiFi Signal Strength Real Time Curve (b) WiFi Signal Strength in Different Channels

On the bottom left, there exist eight real time sliders controlling the eight Hittite analogue phase shifters on the smart antenna board.

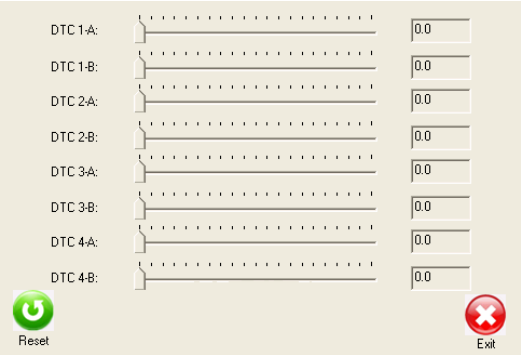


Figure 6.26: Real Time Control Slider for LPC1768

By changing the voltages to the phase shifters, the main beam direction of the antenna array is rotated, which generates a variation of the received RSSI in the manual control GUI. Figure 6.27 shows the evaluated results. Different voltage levels are provided to the antenna array and the received WiFi signal strength curves are able to reflect the diversity.

Figure 6.27: Manual Control Evaluating Results for LPC1768

6.3.2.3 Automatic Control

An improved version of the GUI has been developed which can provide the smart antenna array automatic control. The main screen is illustrated in Figure 6.28.

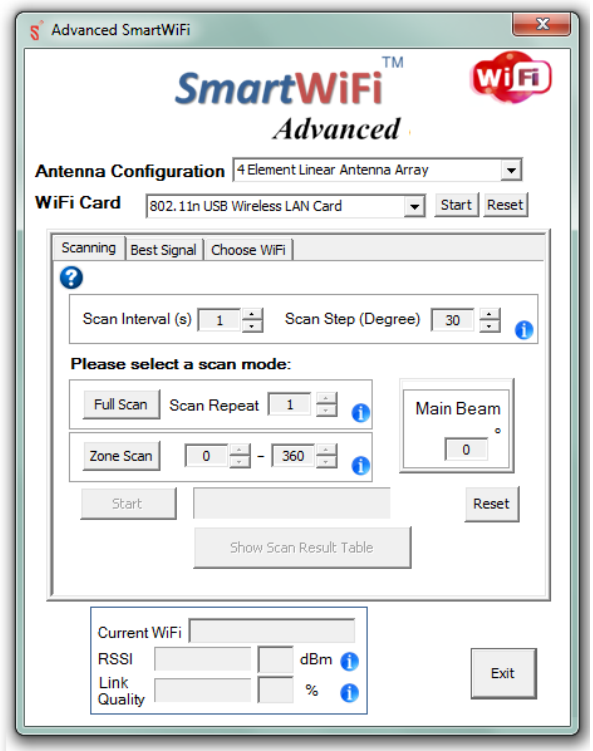


Figure 6.28: Automatic Control GUI for LPC1768

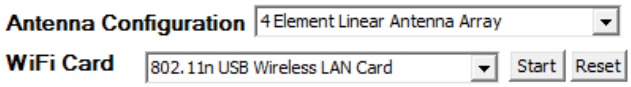


Figure 6.29: Antenna Array and WiFi Adapter Selection

In the current smart antenna array implementation, the four-element linear antenna array with Archimedean spiral slots is used. In Figure 6.29, the "4 Element Linear Antenna Array" and "EDUP 802.11 b+g USB adapter" should be selected. This automatic GUI is also compatible with more elements antenna arrays. By selecting the EDUP USB adapter, the original WiFi card of the laptop will be disabled. The smart antenna array will detect and monitor the WiFi signals for the control laptop.

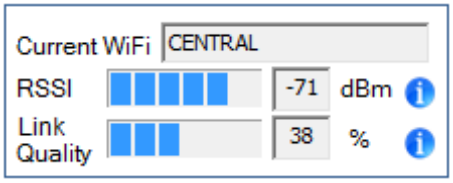


Figure 6.30: Current Connected WiFi Information

On the bottom left of the advanced GUI, the current WiFi information is displayed, as shown in Figure 6.30. Furthermore, in the software program, some information windows help to describe RSSI and Link Quality, as illustrated in Figure 6.31 and Figure 6.32, respectively.

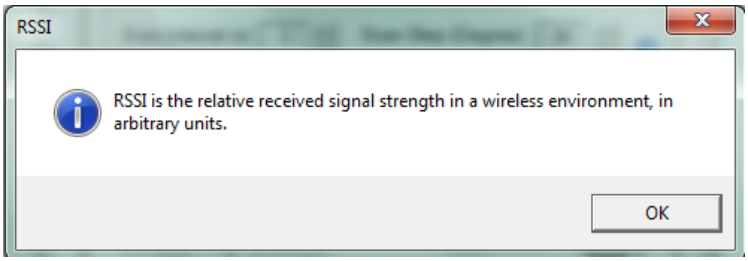


Figure 6.31: RSSI Description

RSSI is the relative received signal strength in a wireless environment, in arbitrary units.

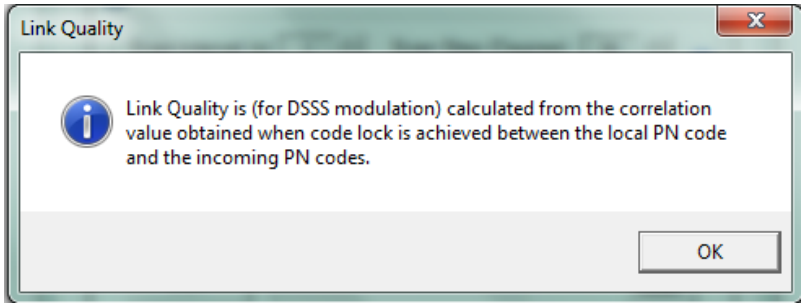


Figure 6.32: Link Quality Description

Link Quality is calculated from the correlation value obtained when code lock is achieved between the local PN code and the incoming PN codes.

There are three functions included in the Advanced GUI for LPC1768: Scanning, Best Signal and Choose WiFi.

6.3.2.3.1 Scanning Function

Scanning: In scanning mode, the program enables scanning of the surrounding environmental for WiFi signals. This takes place by steering the main beam of the smart antenna array.

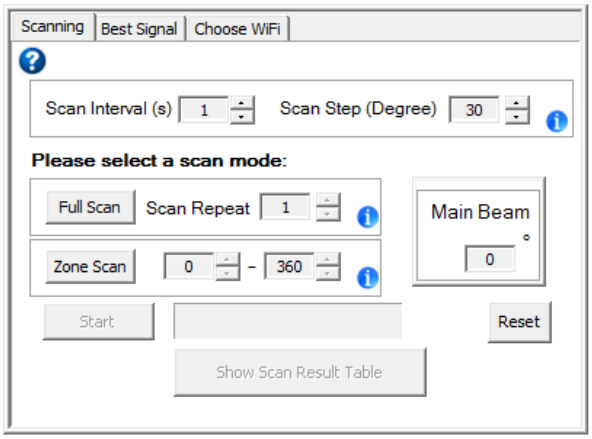


Figure 6.33: Scanning Function of the GUI for LPC1768

In Figure 6.33, the scan interval and scan step can be selected. Scan interval is the time between two sequential scans. Scan step is the angle separation between two sequential scans after steering the beam.

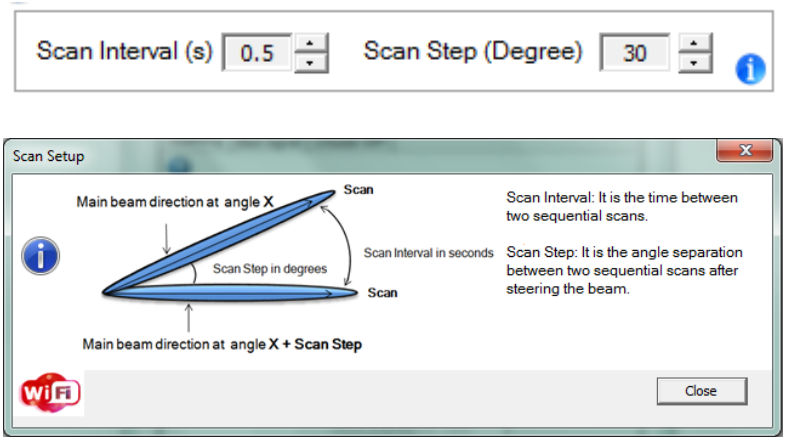


Figure 6.34: Scan Interval and Scan Step Definition

Two modes for the scanning are provided: Full scan and Zone scan.

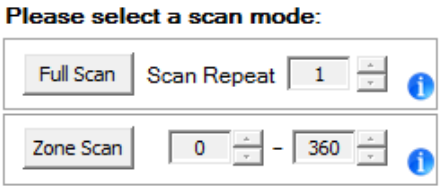


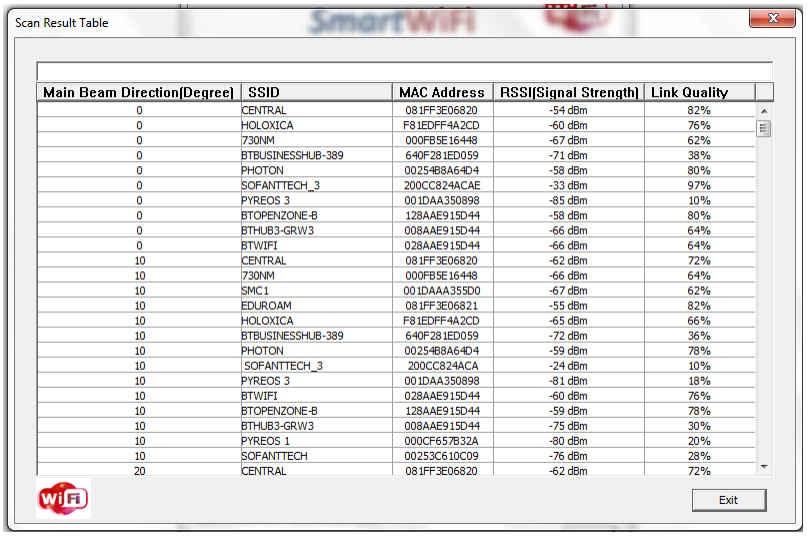
Figure 6.35: Scan Mode Selection

In **Full Scan**, this mode performs a full 360 degrees scanning for all WiFi signals. The Scan Repeat is a parameter to apply the rescanning for another round, up to 5 times, default value is 1.

After clicking the Start button, the full scan will begin and a bar shows the progress. While scanning, another window near the "Reset" button is showing the current main beam direction, as shown in Figure 6.36.

Figure 6.36: Status Bar and Current Main Beam Direction

When the scan finished, a popup table will show the WiFi signals information in surrounding environment. For the current four element linear antenna array, the main beam is able to steer from -50º to +50º for WiFi application. The full scan function has been modified to show only ±50º directions.

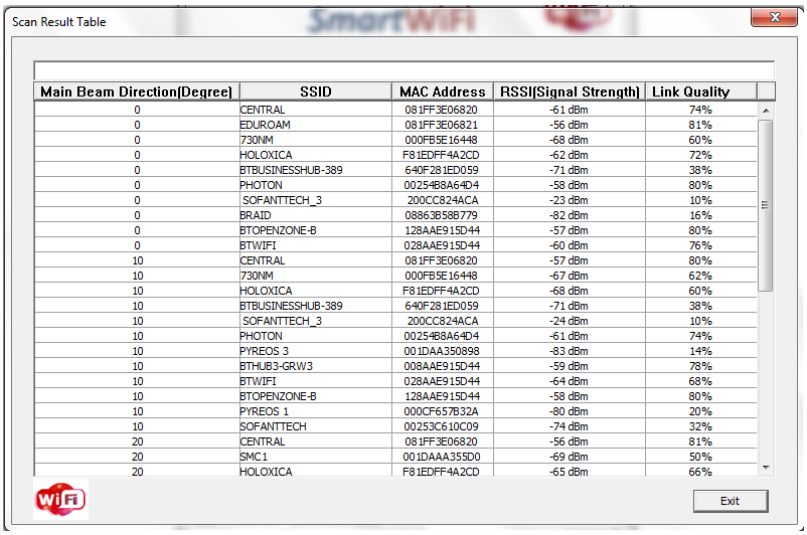


Main Beam Direction(Degree)	SSID	MAC Address	RSSI(Signal Strength)	Link Quality
0	CENTRAL	081FF3E06820	-54 dBm	82%
0	HOLOXICA	F81EDFF4A2CD	-60 dBm	76%
0	730NM	000FB5E16448	-67 dBm	62%
0	BTBUSINESSHUB-389	640F281ED059	-71 dBm	38%
0	PHOTON	00254B8A64D4	-58 dBm	80%
0	SOFANTTECH_3	200CC824ACAE	-33 dBm	97%
0	PYREOS 3	001DAA350898	-85 dBm	10%
0	BTOPENZONE-B	128AAE915D44	-58 dBm	80%
0	BTHUB3-GRW3	008AAE915D44	-66 dBm	64%
0	BTWIFI	028AAE915D44	-66 dBm	64%
10	CENTRAL	081FF3E06820	-62 dBm	72%
10	730NM	000FB5E16448	-66 dBm	64%
10	SMC1	001DAAA355D0	-67 dBm	62%
10	EDUROAM	081FF3E06821	-55 dBm	82%
10	HOLOXICA	F81EDFF4A2CD	-65 dBm	66%
10	BTBUSINESSHUB-389	640F281ED059	-72 dBm	36%
10	PHOTON	00254B8A64D4	-59 dBm	78%
10	SOFANTTECH_3	200CC824ACA	-24 dBm	10%
10	PYREOS 3	001DAA350898	-81 dBm	18%
10	BTWIFI	028AAE915D44	-60 dBm	76%
10	BTOPENZONE-B	128AAE915D44	-59 dBm	78%
10	BTHUB3-GRW3	008AAE915D44	-75 dBm	30%
10	PYREOS 1	000CF657B32A	-80 dBm	20%
10	SOFANTTECH	00253C610C09	-76 dBm	28%
20	CENTRAL	081FF3E06820	-62 dBm	72%

Figure 6.37: Full Scan Results Using Four-Element Linear Antenna Array

The table in Figure 6.37 presents the full scan results for the four-element linear antenna array with the main beam steering from -50º to +50º in the step of 10º. At each direction, the table is displaying Main Beam Direction, SSID, MAC Address, RSSI and Link Quality. It is clear that along with the beam rotating, the RSSI and link quality are showing different values.

In **Zone Scan** mode, it allows scanning a defined area or zone by only steering the beam within this defined zone. When the scan finishes, a popup table will show the WiFi signals information within the selected area. The table presented in Figure 6.38 shows the defined zone scan results for the four-element linear antenna array with the main beam steering from -30º to +30º in the step of 10º.



Main Beam Direction[Degree]	SSID	MAC Address	RSSI[Signal Strength]	Link Quality
0	CENTRAL	081FF3E06820	-61 dBm	74%
0	EDUROAM	081FF3E06821	-56 dBm	81%
0	730NM	000FB5E16448	-68 dBm	60%
0	HOLOXICA	F81EDFF4A2CD	-62 dBm	72%
0	BTBUSINESSHUB-389	640F281ED059	-71 dBm	38%
0	PHOTON	00254B8A64D4	-58 dBm	80%
0	SOFANTTECH_3	200CC824ACA	-23 dBm	10%
0	BRAID	08863B58B779	-82 dBm	16%
0	BTOPENZONE-B	128AAE915D44	-57 dBm	80%
0	BTWIFI	028AAE915D44	-60 dBm	76%
10	CENTRAL	081FF3E06820	-57 dBm	80%
10	730NM	000FB5E16448	-67 dBm	62%
10	HOLOXICA	F81EDFF4A2CD	-68 dBm	60%
10	BTBUSINESSHUB-389	640F281ED059	-71 dBm	38%
10	SOFANTTECH_3	200CC824ACA	-24 dBm	10%
10	PHOTON	00254B8A64D4	-61 dBm	74%
10	PYREOS 3	001DAA350898	-83 dBm	14%
10	BTHUB3-GRW3	008AAE915D44	-59 dBm	78%
10	BTWIFI	028AAE915D44	-64 dBm	68%
10	BTOPENZONE-B	128AAE915D44	-58 dBm	80%
10	PYREOS 1	000CF657B32A	-80 dBm	20%
10	SOFANTTECH	00253C610C09	-74 dBm	32%
20	CENTRAL	081FF3E06820	-56 dBm	81%
20	SMC1	001DAAA355D0	-69 dBm	50%
20	HOLOXICA	F81EDFF4A2CD	-65 dBm	66%

Figure 6.38: Zone Scan Results Using Four-Element Linear Antenna Array

6.3.2.3.2 Best Signal Function

The second tab in the GUI is called Best WiFi, as demonstrated in Figure 6.39. This function enables the user to identify the best available WiFi signals at the location. This is carrying out by fully steering the main beam to enable the full scan the surround environment for the best WiFi signals.

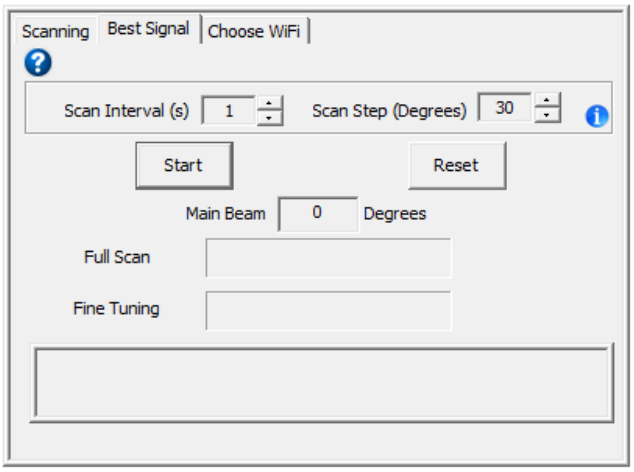


Figure 6.39: Best Signal Function of the GUI for LPC1768

After selecting the scan interval and scan step, the program will automatically perform a full scan and accurate fine tuning. Finally, the detailed best WiFi connect information will be listed, which includes SSID, MAC Address, Signal Strength and Link Quality.

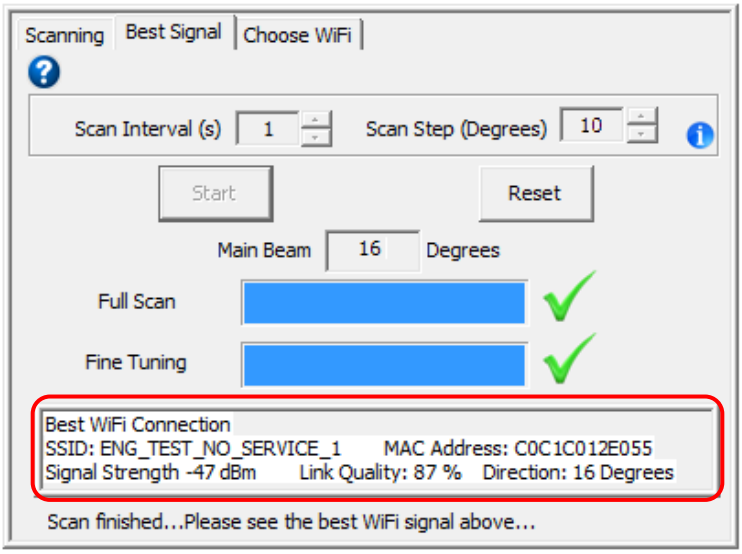


Figure 6.40: Best Signal Scan Results Using Four-Element Linear Antenna Array

6.3.2.3.3 Choose WiFi Function

In this function, the system allows the user to connect to the desired WiFi network. The system will keep steering the beam in order to keep the signal strength above the signal threshold. In this mode, the user has to select the desired WiFi network resulted from the pre-scanning, define the first and second threshold and then start the scanning. The system will automatically connect to the desired wireless network while steering the main beam in the surround environment in order to identify the direction of the best signal strength. The function continues monitoring the performance of the connected signal. If the signal drops

below the first threshold, this will trigger the fine tuning mode. If the system fails to recover it or the signal drop below the second threshold, it will switch to the full scan mode. The system will try to recover the WiFi network of the best signal at all times. If the WiFi network is unavailable, the system will display a warning message.

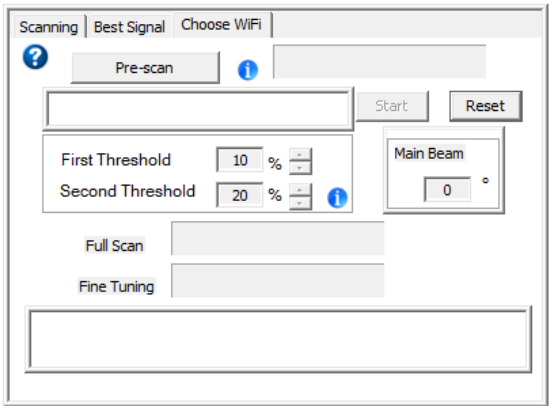


Figure 6.41: Choose WiFi Function of the GUI for LPC1768

Figure 6.41 shows the Pre-scan. In this mode, the system is capturing all WiFi networks (SSID) available to allow the user to select the desired network.

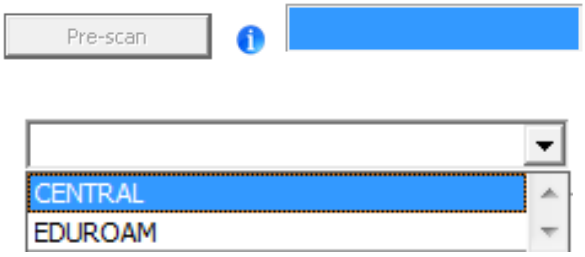


Figure 6.42: Pre-Scan in Choose WiFi Function

The user is able to select a particular WiFi network from the drop down list.

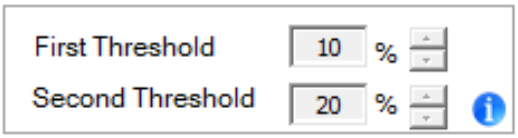


Figure 6.43: Threshold in Choose WiFi Function

Furthermore, it is able to setup the threshold values for the chosen WiFi. In Figure 6.42, **First Threshold** will trigger the fine tuning to take place in order to keep the signal strength above the first threshold. **Second Threshold** will trigger the full scan mode to search for the direction with the highest signal strength for the chosen network. The first threshold value is smaller than the second one.

After setting up the parameters, the software program automatically performs a full scan and accurate fine tuning. Finally, the detailed chosen WiFi information will be listed, which includes SSID, MAC Address, Signal Strength and Link Quality. The system continues monitoring the RSSI using threshold values to maintaining the strongest WiFi signal.

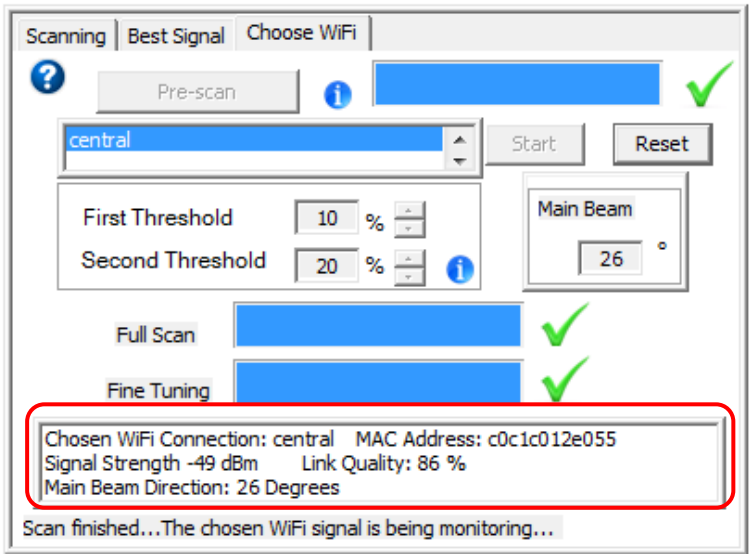


Figure 6.44: Choose WiFi Scan Results Using Four-Element Linear Antenna Array

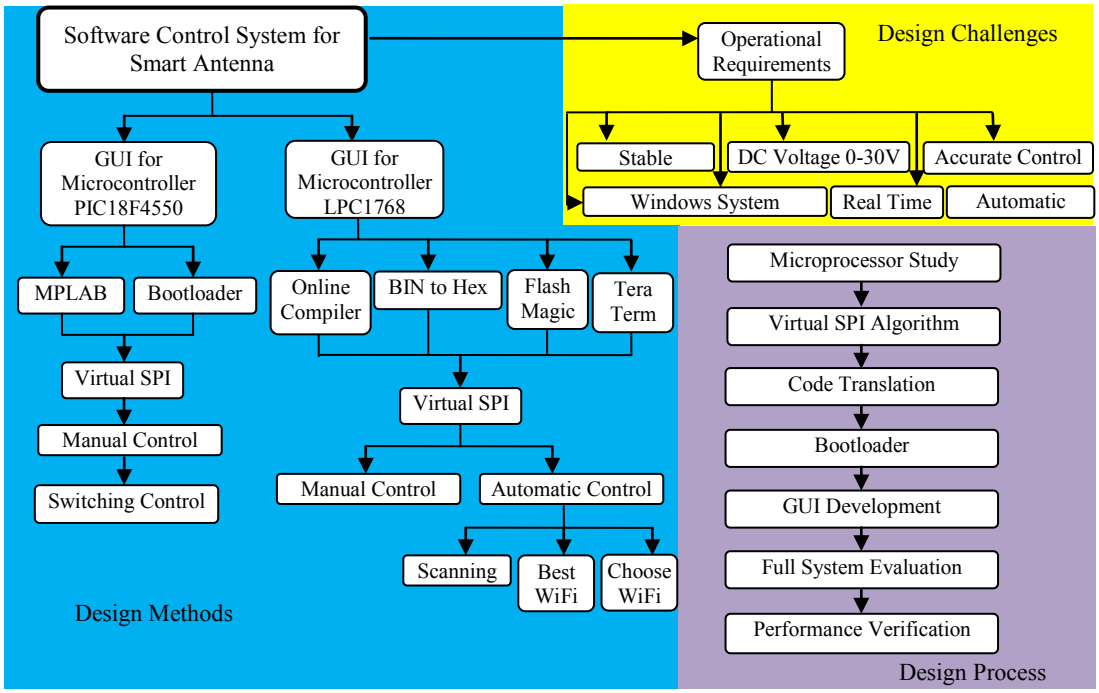
In the above Scanning, Best WiFi and Choose WiFi functions, all of the algorithms are able to cover the main beam steering from 0º to 360º. However, limited by the four elements linear antenna array characterisation, only -50º to 50º beam rotating is performed. Further research will produce a wider scanning range smart antenna array to generate more accurate scanning results.

6.4 Summary

This chapter presents the software implementation to automatically configure the smart antenna array system. Two series of control systems are developed for microprocessor PIC18F4550 and LPC1768, respectively.

For microcontroller PIC18F4550, research begins with a virtual SPI communication algorithm between the microchip and digital potentiometers. A graphical user interface has been proposed to control the microchip through a laptop. After initialising PIC18F4550, the GUI transfers the control signal into a Microchip compiler called MPLAB and changes the C code into a Hexadecimal (Hex) document. By utilising the Bootloader program, this Hex code will be delivered into the microchip PIC18F4550 and then configures the phase shifters on the smart antenna array. Two control methods: Manual Control and Switching Control are provided to achieve particular DC voltage or square waveforms from the digital potentiometers. The PIC18F4550 software control system is able to generally configure the smart antenna array but requires other application to check the WiFi signal variations.

Two improved versions of the GUI are developed for microcontroller LPC1768. This microchip provides real time control between a laptop which makes the GUI more advanced. Both of the GUIs allow the user to detect SSID, RSSI, MAC Address and Link Quality of WiFi signals surrounding the laptop. The basic GUI can manually configure the phase shifters and display all of the WiFi information. By changing the phase shifters, it is able to rotate the antenna array main beam direction in order to analyse and monitor the received WiFi signals. Furthermore, this chapter proposes a beta version of an advanced software package for LPC1768, which demonstrates full scanning and basic adaptive beamforming for WiFi signals.



1. The software control system is compatible with Windows XP/Vista/7 and 8, with stable performance.

2. The virtual SPI algorithm is able to accurately configure the digital potentiometers.

3. The GUI for PIC18F4550 is able to generate particular DC voltages and square waveforms for the digital potentiometers to control the smart antenna array.

4. A VB script is developed for PIC18F4550 to achieve an automatic control between the microcontroller and laptop.

5. Real time control is obtained for microprocessor LPC1768 with steady connections.

6. The GUI for LPC1768 demonstrates Manual Control and Automatic Control. Both of the GUI illustrate detailed received WiFi information based on the smart antenna array system

7. The advanced GUI using LPC1768 is able to perform an automatic antenna beam steering and select a best WiFi signal around the control terminal.

Achievements

Figure 6.45: The Investigation of Software Control Systems for Smart Antenna

Chapter 7: Conclusions

7.1 Summary and Conclusions

This thesis covers the research studies of fully implemented smart antenna systems for future mobile devices. Specifically, the studies are divided into five major directions: (a) Novel antenna and array configuration to achieve wide scanning range (b) Reconfigurable and UWB feeding network geometry to produce suitable amplitude excitation (c) Phase shifter evaluation and UWB transition structure to provide proper phase excitation (d) Hardware implementation for intelligently configuring the phase shifters (e) Software program to demonstrate smart antenna automatic control.

To achieve satisfactory adaptive beamforming, it is necessary to have suitable radiating elements. Chapter 2 presents a novel compact planar monopole antenna with Archimedean spiral slots for WiFi/Bluetooth and LTE applications. The effects of varying slot dimensions and positions on the monopole antenna performance have also been analysed. It is illustrated when the value of Archimedean spiral slots key parameter t is from 0 to 1mm, the presented design demonstrates low reflection coefficient (-19dB, -30dB), high efficiency (79%, 87%), large gain (2.72dBi, 2.88dBi) and omni-directional radiation patterns for 2.45GHz and 2.6GHz, respectively. This antenna structure has application to multi-functional wireless communication systems. Furthermore, a four-element linear planar monopole antenna array using the unit antenna has been designed, simulated and optimised. Different inter-element spacing values are investigated and compared. When the spacing is 40mm, the array geometry displays low reflection coefficient (-17dB, -29dB), suitable mutual coupling (-15dB, -14dB), large efficiency (75%, 84%), high gain (9.9dB, 10.3dB) and directional radiation patterns for WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) standards. In simulation, by providing proper

amplitude and phase excitations, array beam steering from -57° to +54° for 2.45GHz, and -59° to +57° at 2.6GHz in H-plane with the gain fluctuation less than 3dB, narrow half power beamwidth (40°) and low side lobe level (-10dB) have been obtained.

The second aspect of the research focuses on the design and development of feeding networks for the smart antenna array. The feeding network provides RF signal to the radiating element and also controls the excitations. Different power dividers and feeding network geometries have been analysed and compared. Based on the fundamental Wilkinson power divider, a miniaturised structure built on silicon wafers are designed, simulated and characterised. By optimising the λ/4 transmission line, the circuit dimension can be reduced by 65% without significantly increasing the insertion loss or decreasing the bandwidth. At the desired frequency (2.4GHz), the proposed novel silicon-based Wilkinson divider can provide low reflection coefficient (-42dB), suitable forward gain (-3.2dB) and high isolation (-38dB). Then, another novel feeding network structure is proposed, which consists of four 2-way conventional Wilkinson power dividers with outputs revolving at an angle of 45° to suit circular antenna array geometry. Subsequently, a novel reconfigurable feeding network which enables electronic switching of circular polarisation direction in an antenna array is presented. By digitally controlling the PIN diodes, the lengths of the transmission lines are various, leading to different phase shifts between output ports. Integrated with any four antenna elements, the feeding network is able to switch the polarisation between LHCP and RHCP. Both simulation and measurement results demonstrate that high return loss (10dB), suitable insertion loss (8dB) and good isolation (-12dB) can be obtained. Phase errors of ± 9º are achieved for required output ports. Furthermore, another reconfigurable feeding network is investigated, which allows for the electronic switching among four frequency bands: 600MHz-900MHz, 1.2GHz-1.6GHz, 1.8GHz-2.2GHz and 2.4GHz-2.6GHz, in order to cover GSM, GPS, 3G, WiFi and LET applications in different countries. Both simulation and measurement results show that high return loss (20dB) and good insertion loss (3.8dB) have been obtained. Based on the above research, an UWB feeding network configuration is presented. The dimensions of the proposed UWB power divider configuration are only 9.5mm×15mm and the design demonstrates high return loss (10dB), suitable insertion loss (3.2dB) and high isolation (-10dB) through 0.5GHz to 10GHz, providing an ultra wide band performance. Moreover, various output separations are developed, which include 12mm, 16mm, 20mm, 36mm, 40mm and 45mm, which could satisfy different antenna array inter-element spacing. By performing the third order intermodulation distortion measurements, the linearity performance of the UWB device is confirmed. Finally, a linear 1:4 UWB feeding network with separations of 40mm is developed and characterised for the smart antenna array. Suitable S-Parameters are obtained.

Chapter 3 firstly reviews and analyses all of the different phase shifter developments, including ferrite phase shifter, switched delay line phase shifter and loaded transmission line phase shifter. PIN diodes, FETs, MMIC and MEMS are employed as control elements in different configurations. Based on the comparison, a high accuracy and low loss MMIC analogue phase shifter from Hittite has been selected and fully characterised. Through the evaluation board testing, this HMC928LP5E analogue phase shifter demonstrates 180° phase shift at 3.64V and 3.59V, 360° phase shift at 8.22V and 8.11V, with high return loss (10dB) and low insertion loss (3dB), for WiFi/Bluetooth (2.45GHz) and LTE (2.6GHz) standards, respectively, which confirms that the analogue phase shifter is adequate for the smart antenna array application. In addition, two UWB CPW-to-Microstrip transitions are designed to produce smooth field transformation and impedance matching. The proposed structure shows high return loss (10dB) and suitable insertion loss (0.3dB) from 0.5GHz to 9GHz. Finally, the complete smart antenna array is integrated and fully characterised. By appropriately controlling the phase shifters and adjusting the excitations of the elements, beam steering for ±50° and ±52° in H-plane with the gain fluctuation less than 3dB and low side lobe level (-10dB) at 2.45GHz and 2.6GHz have been achieved.

However, in mobile applications, it is necessary to have compact control units with low power consumption. Chapter 5 presents two hardware implementations to configure the smart antenna array using microprocessors PIC18F4550 and LPC1768, respectively. Both of the microchips are integrated with digital potentiometers, voltage boosters, oscillators and USB modules. The miniaturised and fabricated PCB control boards are able to accurately control the phase shifters and manage the beam steering. In particular, real time control is achieved by using microcontroller LPC1768. Both of the two control units are compatible with Windows, Android and IOS mobile operating systems.

Several preliminary software programs to configure the adaptive beamforming are explored in Chapter 6. In the developed smart antenna, a laptop running Windows is used as a processing device and WiFi signals (2.45GHz) are detected and evaluated. Using a microchip PIC18F4550, the developed graphical user interface is able to manually send various DC voltages and square waveforms to the phase shifters. Moreover, the software programs investigated for the microprocessor LPC1768 can achieve both of manual control and automatic steering. In manual control, it is able to send particular control voltages to the phase shifters and observe the variation of WiFi signals detected by the array. For automatic steering, some basic algorithms are implemented and the software program could perform a full scan first and then select the strongest WiFi signal direction in the environment. This work demonstrates that the fully integrated smart antenna can be applied for future mobile applications.

Overall, it is concluded that the required adaptive antenna performance can be achieved using the fully integrated smart antenna systems. Therefore, it is possible to embed the complete smart antenna into future mobile devices in wireless communication industry.

7.2 Summary of Contributions

This section summarises the areas and the challenges in designing smart antenna systems that have been addressed in this thesis. In particular, the research areas include antenna design, array geometry, feeding network structure, phase shifter evaluation, CPW-to-Microstrip transition configuration, hardware implementation and software control system, which are discussed as follows.

7.2.1 Miniaturised and Multiband Antenna Design

The main contribution in this section is the concept of etching Archimedean spiral slots onto planar monopole antenna, in order to generate a compact multiband antenna performance.

For planar monopole antenna, the low frequency limitation will increase the size of the element. Due to this reason, the base of the proposed antenna is a circular patch that operates in high frequency range, targeting compact circuit dimension. To create a multiband antenna, Archimedean spiral slots, acting as resonance paths, have been integrated with the circular patch antenna. Analysis of the current distributions on the antenna reveals that at low frequencies the additional of the slots create new circular current paths, which form a wideband low-frequency response. Different shapes of Archimedean spiral slots have been investigated and compared. In this smart antenna implementation, WiFi (2.45GHz) and LTE (2.6GHz) standards have been targeted. However, based on the presented design topology and by varying the dimension of the Archimedean spiral slots, it is able to develop compact antenna elements for other mobile applications, such as GSM, GPS and Galileo.

7.2.2 Adaptive Array Geometry with Wide Scanning Range

The radiation pattern of an array is determined by the geometrical construction and the relative displacement between the antenna elements. In this thesis, the four-element linear antenna arrays with different inter-element spacing are evaluated from the perspective of adaptive beamforming. The optimised array geometry achieves optimum results as it provides high directivity (10dB), low side lobe level (-10dB), and the main beam and nulls are placed accurately at the desired and interference angles, respectively, even when the desired signal is away from boresight ($\theta = 57°$). The limited number of antenna elements and the linear

geometry simplify the array structure, which is aiming at compact mobile applications. The microstrip technology provides easy integration and reduces the design complexity.

7.2.3 Reconfigurable and UWB Feeding Network

In this research, several novel feeding network structures are investigated and developed for various mobile applications. In literature, the T-Junction, resistive and conventional Wilkinson power dividers suffer from the issues of energy loss, mismatch, low isolation, large dimension and narrow operating frequencies.

Firstly, this thesis proposed a silicon-based and miniaturised Wilkinson power divider. With this technique, not only the circuit dimensions are reduced, it also demonstrates better S-Parameters.

Secondly, this research illustrates a particular feeding network for circular antenna arrays. Nowadays, circular antenna arrays have been widely used in mobile, radar, sensor and commercial satellite communication systems. The proposed network is comprised of four 2-way conventional Wilkinson power dividers with outputs revolving at an angle of 45° to suit circular configuration.

Subsequently, a novel miniaturised reconfigurable, switchable feeding network for a four elements dual circularly polarised antenna array is discussed. The four feeds are in phase quadrature to give a phase shift of 90º between each neighbouring antenna element, producing a circularly polarised pattern. Integrated with any four antenna elements, the feeding network provides the ability to switch the polarisation between LHCP and RHCP quickly and accurately.

Furthermore, this thesis produces another miniaturised reconfigurable and feeding network to cover GSM, GPS, 3G, WiFi and global LET standards. By controlling the bias voltages of PIN diodes on the device, the length of $\lambda/4$ transmission lines are varied, which changes the operating frequency to apply for different mobile applications. In this research, three types of PIN diode models were constructed and simulated in order to improve accuracy. The developed feeding network can be hence applied to multiband wireless communication systems. This work forms an important step towards realising a truly global mobile phone.

Finally, an UWB feeding network for smart antenna arrays have been investigated. A literature review illustrates that the existing power divider structures have relatively limited abilities in miniaturising circuit dimensions and perform inefficiently in low frequency bands. This research demonstrates a compact power divider design with operating frequency from

0.5GHz to 10GHz, which covers all of the mobile communication standards. With the proposed technique, it is able to establish UWB wireless communication systems.

7.2.4 Phase Shifter Evaluation

One of the techniques to establish the adaptive antenna array is applying phase shifters for the antenna elements. By varying the phase excitations, main beam direction can be configured and rotated. In this thesis, different phase shifter topologies are investigated and compared, which included the ferrite phase shifter, the switched delay line phase shifter and the loaded transmission line phase shifter. Pin diodes, FETs, MMIC and MEMS are employed as control elements in different configurations. The selected and evaluated MMIC phase shifter demonstrates the advantages of small size, reduced control voltage, wide frequency range, high phase shift, suitable insertion loss, low power consumption and excellent linearity.

7.2.5 UWB CPW-to-Microstrip Transition

Moreover, this research presents an UWB CPW-to-Microstrip transition structure for smart antenna application. The proposed transition provides the field and impedance matching between adjacent transmission lines with low insertion loss (0.3dB). This transition geometry is able to reduce antenna array design complexity and increase reliability of the adaptive beamforming.

7.2.6 Smart Antenna Hardware Implementation

This work also develops the miniaturised hardware control units for smart antenna systems in mobile devices. Two complete control devices are investigated using microprocessor PIC18F4550 and LPC1768, respectively. All of the communication chips are integrated onto the control PCBs, including digital potentiometers, voltage boosters, oscillators and USB modules. The control units have been initialised, evaluated and programmed with basic algorithms. With the proposed designs, it is able to accurately configure the phase shifter so as to achieve the antenna beam steering. Moreover, the control units provide a wide range of DC voltage values (from 0V to 30V), which also can be used to control other RF devices, such as PIN diodes, FETs and MEMS. The presented control PCBs are compatible with Windows, Android and IOS mobile systems. With this strong compatibility, miniaturised dimension, low power consumption, stable performance, accurate control and simplified structure, the developed control PCBs have wide applications in future mobile communication systems.

7.2.7 Smart Antenna Software Control System

The main contributions in this section are several preliminary software programs to manage the adaptive beamforming. Using the microchip PIC18F4550, the developed graphical user interface is able to manually provide particular DC voltage level and square waveforms to the phase shifters. However, for the microcontroller LPC1768, due to its advantage of real time control, not only the manual control is achieved, it also enables some advanced functions to automatically perform the antenna main beam steering. Furthermore, using some basic algorithm, the software program can intelligently compare the signal information at various beam directions and estimate the best signal in the environment. In the demo, laptop running Windows is utilised to detect and analysis WiFi signals. Nevertheless, the developed software program can be easily transferred into Java and Objective-C for Android and IOS mobile systems. With this technique, it is able to realise intelligent applications on mobile device to configure the smart antenna array adaptive beamforming.

7.2.8 Complete Smart Antenna System Integration

This research demonstrates a complete smart antenna system for future mobile devices. The work includes antenna analysis, RF circuit design, digital circuit implementation and software programming. The proposed design structures have been calculated, analysed, simulated, optimised, manufactured and fully evaluated. The system dimensions are miniaturised to suit compact mobile terminals and the measured results illustrate that the basic adaptive beamforming is achieved. The presented technique will contribute to realise advanced smart antenna on mobile communication systems.

7.3 Future Work

The following are possible topics for further investigations:

7.3.1 Antenna Design

Future work with the proposed antenna design is to further miniaturise the structure. Techniques such as using high permittivity substrates, adding more slots loading and shorting pins can be explored. The challenge will be to maintain the multiband performance and suitable radiation patterns while applying those miniaturising techniques.

7.3.2 Array Geometry

a. Evaluate the Array Performance for DoA Estimation

In this thesis, the performance of the antenna array is evaluated from its 3 dB scanning range and its adaptive beamforming ability. Another important aspect of adaptive array antennas is the ability to estimate the DoA of a signal. Future studies will investigate the performance of the array geometry in estimating the DoA using advanced algorithms such as Capon, Bartlett and MUSIC.

b. Increase the Number of Elements

Four antenna elements are used in the presented array and the limited number restricts the scanning range and gain. Further research will concentrate on increasing the number of radiating elements and enlarge the beam steering range.

c. Array Geometry with Non-Identical Elements

The arrays in this thesis were synthesised for wide scanning range and these geometries consist of omni-directional elements. Future work on this topic would be to evaluate the scanning ranges of antenna array that is comprised of elements with different radiation characteristics such as directional and bi-directional antennas or a possible combination of these elements.

d. Change Antenna Array Configuration

In this work, linear configuration is implemented. Circular, rectangular or faceted geometries will be further investigated to optimise the adaptive beamforming.

7.3.3 Feeding Network Structure

a. Silicon Feeding Network

In this research, silicon-based feeding network has been designed and developed. Further study will integrate this feeding network with antenna elements in order to establish smart antenna array on silicon substrate.

b. Feeding Network for Circular Antenna Array

A feeding network for circular array geometry is demonstrated in this study. Further work will focus on building circular smart antenna arrays using the proposed structure.

c. Reconfigurable Feeding Network

Furthermore, this study investigates two reconfigurable feeding networks to control the polarisation and operating frequency. The next step is to integrate the design with a reliable switching mechanism. Issues regarding the feeding network and switch integrations include

the design of bias network for PIN diodes and the power handling requirement of RF MEMS switches. The additional structures needed to allow the reconfiguration may interfere with the performance of the network.

d. UWB Feeding Network

Similar to the antenna design, future work with the proposed UWB feeding network is to further miniaturise the dimension, by utilising using high permittivity substrates, such as ceramic and silicon.

7.3.4 Phase Shifter Investigation

a. MEMS Phase Shifter

In this thesis, different phase shifter techniques are studied and compared. Several commercially available phase shifters were used in the prototype to validate the design approach. The selected MMIC devices demonstrate high phase shift, excellent linearity and low power consumption. However, the phase shifter is still generating 3dB insertion loss, which will significantly affect the antenna gain and efficiency. Future research will concentrate on RF MEMS phase shifters in order to reduce the insertion loss and improve the adaptive beamforming.

b. Antenna Array and Phase Shifter Integration

Another future direction would be developing the proposed smart antennas with the RF MEMS phase shifters on the same platform to achieve smaller size and lower reflection loss.

7.3.5 Hardware Control

a. Control PCB Miniaturisation

Another compact hardware control unit has been designed, simulated and transferred into PCB layout, as illustrated in Figure 7.1. This board is also using LPC1678 as the microprocessor, and several new components are integrated to further reduce the PCB dimension, such as a switch, a USB module and ISP connectors. This structure is only 34mm × 62.5mm, saving half of the space compared to the original configuration. Future research will focus on the new PCB fabrication and evaluation.

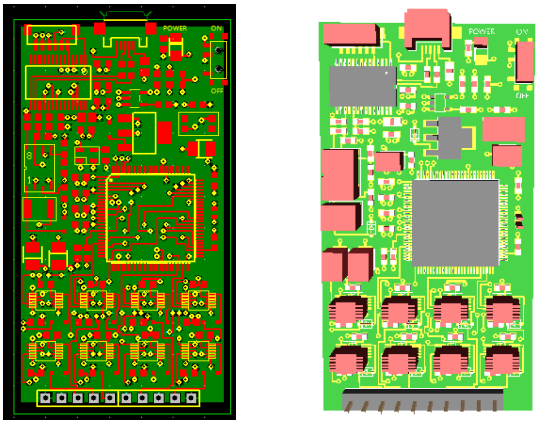


Figure 7.1: Miniaturised PCB Control Unit Using Microprocessor LPC1768

b. Control System Integration

In this work, the ultimate aim would be integrating the proposed hardware control system into a microchip and combining with RF phase shifters through flip chip technology. Figure 7.2 demonstrates the integrated system underneath the encapsulation. Through the single package integration, it is able to avoid high voltage exposure on the system. Furthermore, this technique eliminates the requirement of electrostatic discharge (ESD) network capacitors, which significantly reduces 20pF to 30pF capacitances at input/output (IO) pads. This integration also provides a much smaller packaging than traditional carrier based packaging both in area and height. The short wires in the flip chip technology will greatly decrease the parasitic inductance and allow wider frequency operations.

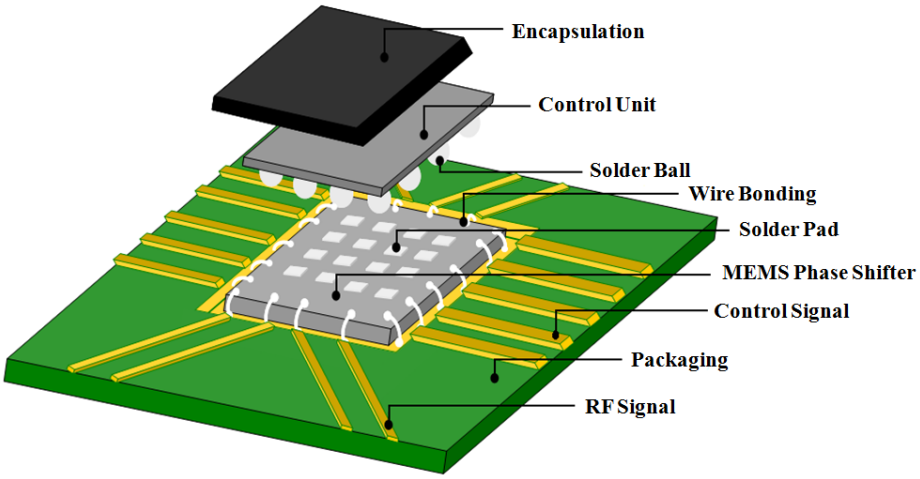


Figure 7.2: Control System Package Level Integration through Flip Chip Technology

7.3.6 Software Programming

a. Transfer the GUI into Android and IOS

This research presented several prototype software programs to detect and analyse WiFi signals using the proposed smart antenna in Windows. Future work will continue to improve the control software and also transfer the algorithms into Android and IOS mobile operating systems. Figure 7.3 presents a developed initial WiFi analyser application on Android device.

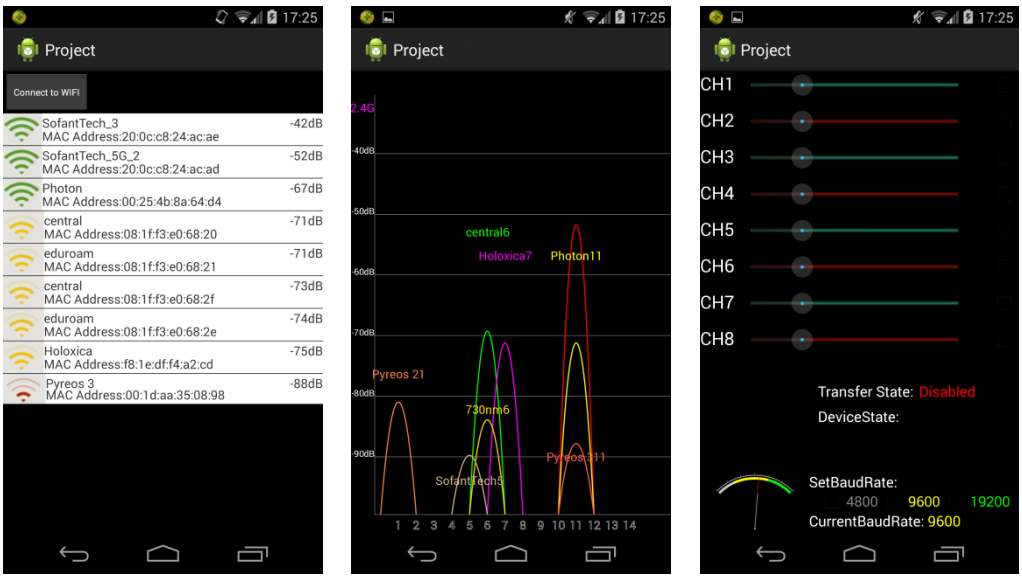


Figure 7.3: Prototype WiFi Analyser on Android 4.4.4 System

b. Analysis Other Mobile Communication Standards

Moreover, other mobile communication standards, such as GPS/Galileo/LET and 4G will be detected and analysed by the developed the software control system.

7.4 Final Comments

Smart antenna and adaptive beamforming used in mobile applications brings many attractive features, such as increasing directivity, extending signal coverage, interference suppression and energy saving. However, the complexity of the system has limited its widespread application in the commercial sector. This thesis demonstrates several techniques to establish and evaluate complete smart antenna systems for mobile communication.

The future mobile devices will be light, compact, flexible, intelligent and multifunctional. The development of smart antennas will also make its contributions to produce advanced smart phones. This thesis proposes a number of solutions that will help to achieve this goal.

REFERENCES

[1] J. A. Stine, "Exploiting smart antennas in wireless mesh networks using contention access," IEEE Wireless Communications, vol. 13, pp. 38-49, 2006.

[2] H. Liu, S. Gao, and T.-H. Loh, "Small Director Array for Low-Profile Smart Antennas Achieving Higher Gain," IEEE Transactions on Antennas and Propagation, vol. 61, pp. 162-168, 2013.

[3] S. A. Zekavat, C. R. Nassar, and S. Shattil, "Oscillating-beam smart antenna arrays and multicarrier systems: achieving transmit diversity, frequency diversity, and directionality," IEEE Transactions on Vehicular Technology, vol. 51, pp. 1030-1039, 2002.

[4] T. S. Ghouse Basha, G. Aloysius, B. R. Rajakumar, M. N. Giri Prasad, and P. V. Sridevi, "A constructive smart antenna beam-forming technique with spatial diversity," IET Microwaves, Antennas & Propagation, vol. 6, pp. 773-780, 2012.

[5] F. Gross, Smart Antennas for Wireless Communications: With MATLAB (Professional Engineering), The McGraw-Hill Professional; 1 Edition 2005.

[6] C. A. Balanis and P. I. Ioannides, Introduction to Smart Antennas, Morgan & Claypool Publishers, 2007. 2007.

[7] Y.-Y. Bai, S. Xiao, M.-C. Tang, Z.-F. Ding, and B.-Z. Wang, "Wide-Angle Scanning Phased Array With Pattern Reconfigurable Elements," IEEE Transactions on Antennas and Propagation, vol. 59, pp. 4071-4076, 2011.

[8] D. T. Pham, H. Subbaraman, M. Y. Chen, X. Xiaochuan, and R. T. Chen, "Light Weight and Conformal 2-Bit, 1 x 4 Phased-Array Antenna With CNT-TFT-Based Phase Shifter on a Flexible Substrate," IEEE Transactions on Antennas and Propagation, vol. 59, pp. 4553-4558, 2011.

[9] L. Hai-Tao, S. Gao, and L. Tian-Hong, "Electrically Small and Low Cost Smart Antenna for Wireless Communication," Antennas and Propagation, IEEE Transactions on, vol. 60, pp. 1540-1549, 2012.

[10] Y.-H. Suh and K. Chang, "A new Millimeter-wave printed dipole phased array antenna using microstrip-fed coplanar stripline tee junctions," IEEE Transactions on Antennas and Propagation, vol. 52, pp. 2019-2026, 2004.

[11] N. Kingsley, G. E. Ponchak, and J. Papapolymerou, "Reconfigurable RF MEMS Phased Array Antenna Integrated Within a Liquid Crystal Polymer (LCP) System-on-Package," Antennas and Propagation, IEEE Transactions on, vol. 56, pp. 108-118, 2008.

[12] D.-C. Chang and C.-N. Hu, "Smart Antennas for Advanced Communication Systems," Proceedings of the IEEE, vol. 100, pp. 2233-2249, 2012.

[13] C.-K. Lin and S.-J. Chung, "A Filtering Microstrip Antenna Array," IEEE Transactions on Microwave Theory and Techniques, vol. 59, pp. 2856-2863, 2011.

[14] Q. Zhang and S. Yan, "A novel dual-frequency and dual-polarized microstrip antenna array for Wireless Sensor Networks GPRS module of cluster nodes," IEEE International Conference on Intelligent Computing and Intelligent Systems (ICIS2010), pp. 791-794, 29-31 Oct. 2010.

[15] E. Garduno-Nolasco, J. Sosa-Pedroza, and H. Jardo-Aguilar, "An UWB microstrip feeding quasi circular antenna," 7th International Conference on Electrical Engineering Computing Science and Automatic Control (CCE), pp. 300-304, 8-10 Sept. 2010.

[16] O. M. Haraz, A. R. Sebak, and T. A. Denidni, "Dual-polarised dielectric-loaded monopole antenna for wideband communication applications," IET Microwaves, Antennas & Propagation, vol. 6, pp. 663-669, 2012.

[17] C. B. Dietrich, Jr., K. Dietze, J. R. Nealy, and W. L. Stutzman, "Spatial, polarization, and pattern diversity for wireless handheld terminals," IEEE Transactions on Antennas and Propagation, vol. 49, pp. 1271-1281, 2001.

[18] W. C. Barott and P. G. Steffes, "Grating Lobe Reduction in Aperiodic Linear Arrays of Physically Large Antennas," IEEE Antennas and Wireless Propagation Letters, vol. 8, pp. 406-408, 2009.

[19] T. Suda, T. Takano, and Y. Kazama, "Grating lobe suppression in an array antenna with element spacing greater than a half wavelength," IEEE Antennas and Propagation Society International Symposium (APSURSI2010), pp. 1-4, 11-17 July 2010.

[20] S. Hossain, M. T. Islam, and S. Serikawa, "Adaptive beamforming algorithms for smart antenna systems," International Conference on Control, Automation and Systems, 2008. ICCAS 2008. , pp. 412-416, 14-17 Oct. 2008.

[21] T.-J. Huang, P.-H. Pan, and H.-T. Hsu, "Adaptive Beam Steering Smart Antenna System for Ultra-High-Frequency Radio Frequency Identification Applications," International Symposium on Computer, Consumer and Control (IS3C2012), pp. 713-716, 4-6 June 2012.

[22] C. A. Balanis, Antenna Theory: Analysis And Design, John Wiley & Sons Inc, Third edition 2005.

[23] "IEEE Standard for Definitions of Terms for Antennas," IEEE Std 145-2013 (Revision of IEEE Std 145-1993), pp. 1-50, 2014.

[24] M. A. Antoniades and G. V. Eleftheriades, "A Compact Multiband Monopole Antenna With a Defected Ground Plane," Antennas and Wireless Propagation Letters, IEEE, vol. 7, pp. 652-655, 2008.

[25] R. A. Sadeghzadeh-Sheikhan, M. Naser-Moghadasi, E. Ebadifallah, H. Rousta, M. Katouli, and B. S. Virdee, "Planar monopole antenna employing back-plane ladder-shaped resonant structure for ultra-wideband performance," IET Microwaves, Antennas & Propagation, vol. 4, pp. 1327-1335, 2010.

[26] A. Foudazi, H. R. Hassani, and S. M. A. Nezhad, "Small UWB Planar Monopole Antenna With Added GPS/GSM/WLAN Bands," IEEE Transactions on Antennas and Propagation, vol. 60, pp. 2987-2992, 2012.

[27] A. M. J. Marindra, S. Promwong, and J. Takada, "Comprehensive characterization of a novel UWB elliptical planar monopole antenna," TENCON 2012 - 2012 IEEE Region 10 Conference, pp. 1-6, 19-22 Nov. 2012.

[28] X.-S. Yang, K.-T. Ng, S. H. Yeung, and K. F. Man, "Jumping Genes Multiobjective Optimization Scheme for Planar Monopole Ultrawideband Antenna," IEEE Transactions on Antennas and Propagation, vol. 56, pp. 3659-3666, 2008.

[29] R. Zaker, C. Ghobadi, and J. Nourinia, "Bandwidth Enhancement of Novel Compact Single and Dual Band-Notched Printed Monopole Antenna With a Pair of L-Shaped Slots," EEE Transactions on Antennas and Propagation, vol. 57, pp. 3978-3983, 2009.

[30] B. S. Yildirim, B. A. Cetiner, G. Roqueta, and L. Jofre, "Integrated Bluetooth and UWB Antenna," Antennas and Wireless Propagation Letters, IEEE, vol. 8, pp. 149-152, 2009.

[31] N. Rahman and M. N. Afsar, "A Novel Modified Archimedean Polygonal Spiral Antenna," IEEE Transactions on Antennas and Propagation, vol. 61, pp. 54-61, 2013.

[32] J. R. Mruk, Y. Saito, K. Kichul, M. Radway, and D. Filipovic, "A directly fed Ku- to W-Band 2-Arm Archimedean spiral antenna," 41st European Microwave Conference (EuMC2011), pp. 539-542, 10-13 Oct. 2011.

[33] J. Kaiser, "The Archimedean two-wire spiral antenna," IRE Transactions on Antennas and Propagation, vol. 8, pp. 312-323, 1960.

[34] J. M. Bell and M. F. Iskander, "A low-profile Archimedean spiral antenna using an EBG ground plane," IEEE Antennas and Wireless Propagation Letters, vol. 3, pp. 223-226, 2004.

[35] A. R. Guraliuc, R. Caso, P. Nepa, and J. L. Volakis, "Numerical Analysis of a Wideband Thick Archimedean Spiral Antenna," IEEE Antennas and Wireless Propagation Letters, vol. 11, pp. 168-171, 2012.

[36] W. Zhou, N. H. Noordin, N. Haridas, A. O. El-Rayis, A. T. Erdogan, and T. Arslan, "A WiFi/4G compact feeding network for an 8-element circular antenna array," Loughborough Antennas and Propagation Conference (LAPC2011), pp. 1-4, 14-15 Nov. 2011.

[37] D. M. Pozar, Microwave Engineering, John Wiley & Sons Inc, Third edition 2005.

[38] S. Jangid and M. Kumar, "An Equivalent Circuit of UWB Patch Antenna with Band Notched Characteristics," International Journal of Engineering and Technology, p. Volume 3 No. 2, February, 2013

[39] R. L. Haupt, Antenna Arrays: A Computational Approach, Wiley-IEEE Press, 2010. 2010.

[40] K. Hettak, C. J. Verver, M. G. Stubbs, and G. A. Morin, "A novel compact uniplanar MMIC Wilkinson power divider with ACPS series stubs," 2003 IEEE MTT-S International Microwave Symposium Digest, pp. 59-62 vol.1, 8-13 June 2003.

[41] N. Ehsan, K. Vanhille, S. Rondineau, E. D. Cullens, and Z. B. Popovic, "Broadband Micro-Coaxial Wilkinson Dividers," IEEE Transactions on Microwave Theory and Techniques, vol. 57, pp. 2783-2789, 2009.

[42] J. Papapolymerou, G. E. Ponchak, and E. M. Tentzeris, "A Wilkinson power divider on a low resistivity Si substrate with a polyimide interface layer for wireless circuits," IEEE Radio Frequency Integrated Circuits (RFIC) Symposium pp. 483-486, 2002.

[43] B. I. a. B. P. MONGIA.R, RF and Microwave Coupled Line Circuits, Artech House Inc, Norwood, MA 1999.

[44] M. Chongcheawchamnan, N. Siripon, and I. D. Robertson, "Design and performance of improved lumped-distributed Wilkinson divider topology," Electronics Letters, vol. 37, pp. 501-503, 2001.

[45] H. S. Nagi, "Miniature lumped element 180 Wilkinson divider," 2003 IEEE MTT-S International Microwave Symposium Digest, pp. 55-58 vol.1, 8-13 June 2003.

[46] L. Chiu, T. Y. Yum, Q. Xue, and C. H. Chan, "A wideband compact parallel-strip 180 degree Wilkinson power divider for push-pull circuitries," IEEE Microwave and Wireless Components Letters, vol. 16, pp. 49-51, 2006.

[47] W. Zhou, T. Arslan, and B. Flynn, "A reconfigurable feed network for a dual circularly polarised antenna array," IEEE 24th International Symposium on Personal Indoor and Mobile Radio Communications (PIMRC), pp. 430-434, 8-11 Sept. 2013.

[48] W. Zhou, T. Arslan, K. Benkrid, A. O. El-Rayis, and N. Haridas, "Reconfigurable feeding network for GSM/GPS/3G/WiFi and global LTE applications," IEEE International Symposium on Circuits and Systems (ISCAS2013), pp. 958-961, 19-23 May 2013.

[49] Z. Wang, J. Jang, and C. Park, "Tri-band Wilkinson power divider using resonators," IEEE Radio and Wireless Symposium (RWS), pp. 287-290, 16-19 Jan. 2011.

[50] S. Fang, H. Guo, X. Liu, and L. Mao, "A miniaturized dual-frequency Wilkinson power divider using planar artificial transmission lines," International Conference on Microwave and Millimeter Wave Technology (ICMMT), pp. 1588-1590, 8-11 May 2010.

[51] H.-H. Chen and Y.-H. Pang, "A tri-band Wilkinson power divider utilizing coupled lines," IEEE International Symposium on Antennas and Propagation (APSURSI), pp. 25-28, 3-8 July 2011.

[52] T. Kawai, I. Ohta, and A. Enokihara, "Design method of lumped-element dual-band Wilkinson power dividers based on frequency transformation," Asia-Pacific Microwave Conference Proceedings (APMC), pp. 710-713, 7-10 Dec. 2010.

[53] A. M. Abbosh, "Broadband multilayer inphase power divider for C-band applications," Electronics Letters, vol. 44, pp. 120-121, 2008.

[54] A. M. Abbosh, M. E. Bialkowski, and J. Mazierska, "An UWB planar out-of-phase power divider employing microstrip-slot and parallel stripline-microstrip transitions," Asia-Pacific Microwave Conference, pp. 905-908, 12-15 Dec. 2006.

[55] S. Jung, M. Kim, H. Kim, H. Park, and Y. Yang, "Compact broadband 180 Degree Wilkinson divider using right- and left-handed transmission lines," IET Microwaves, Antennas & Propagation, vol. 4, pp. 2050-2056, 2010.

[56] H. S. Nagi, "Miniature lumped element 180 Degree Wilkinson divider," IEEE MTT-S International Microwave Symposium Digest, pp. 55-58 vol.1, 8-13 June 2003.

[57] M. C. Scardelletti, G. E. Ponchak, and T. M. Weller, "Miniaturized Wilkinson power dividers utilizing capacitive loading," IEEE Microwave and Wireless Components Letters, vol. 12, pp. 6-8, 2002.

[58] L.-H. Lu, Y.-T. Liao, and C.-R. Wu, "A miniaturized Wilkinson power divider with CMOS active inductors," IEEE Microwave and Wireless Components Letters, vol. 15, pp. 775-777, 2005.

[59] W. Zhou, N. Haridas, A. O. El-Rayis, A. T. Erdogan, K. Benkrid, and T. Arslan, "Enhanced Wilkinson divider on Si substrate for energy efficient microwave applications," Loughborough Antennas and Propagation Conference (LAPC2012), pp. 1-4, 12-13 Nov. 2012.

[60] "Thin Film, Center-Tapped Data Sheet," VISHAY Electro- Films, USA.

[61] T. S. Laverghetta, Microwaves and Wireless Simplified, 1st ed., Artech House, Boston, London, 1998. 1998.

[62] J.-F. Luy, K. M. Strohm, H. E. Sasse, A. Schuppen, J. Buechler, M. Wollitzer, A. Gruhle, F. Schaffler, U. Guettich, and A. Klaassen, "Si/SiGe MMIC's," IEEE Transactions on Microwave Theory and Techniques, vol. 43, pp. 705-714, 1995.

[63] J.-S. Rieh, L.-H. Lu, L. P. B. Katehi, P. Bhattacharya, E. T. Croke, G. E. Ponchak, and S. A. Alterovitz, "X- and Ku-band amplifiers based on Si/SiGe HBT's and micromachined lumped components," IEEE Transactions on Microwave Theory and Techniques, vol. 46, pp. 685-694, 1998.

[64] T. Ji, H. Yoon, J. K. Abraham, and V. K. Varadan, "Ku-band antenna array feed distribution network with ferroelectric phase shifters on silicon," IEEE Transactions on Microwave Theory and Techniques, vol. 54, pp. 1131-1138, 2006.

[65] J. Papapolymerou, G. E. Ponchak, and E. M. Tentzeris, "A Wilkinson power divider on a low resistivity Si substrate with a polyimide interface layer for wireless circuits," 2002 IEEE MTT-S International Microwave Symposium Digest, pp. 593-596 vol.1, 2-7 June 2002.

[66] H. Oraizi and A. R. Sharifi, "Design and optimization of broadband asymmetrical multisection wilkinson power divider," IEEE Transactions on Microwave Theory and Techniques, vol. 54, pp. 2220-2231, 2006.

[67] O. Xing-Ping and C. Qing-Xin, "A modified two-section UWB Wilkinson power divider," Microwave and Millimeter Wave Technology, 2008. ICMMT 2008. International Conference on, pp. 1258-1260, 21-24 April 2008.

[68] B. Li, X. Wu, Y. Li, J. Zhang, and W. Wu, "A dual-band Wilkinson power divider with 6:1 power dividing ratio using coupled lines," IEEE Antennas and Propagation Society International Symposium (APSURSI), pp. 1-4, 11-17 July 2010.

[69] S. Oh, J. J. Koo, M. S. Hwang, C. Park, Y.-C. Jeong, J.-S. Lim, K.-S. Choi, and D. Ahn, "An Unequal Wilkinson Power Divider with Variable Dividing Ratio," IEEE/MTT-S International Microwave Symposium, pp. 411-414, 3-8 June 2007.

[70] J.-L. Li and B.-Z. Wang, "Novel Design of Wilkinson Power Dividers With Arbitrary Power Division Ratios," IEEE Transactions on Industrial Electronics, vol. 58, pp. 2541-2546, 2011.

[71] L. C. Godara, Handbook of Antennas in Wireless Communications, Ed. Boca Raton, FL: CRC 2002.

[72] S. Chandran, Adaptive Antenna Arrays: Trends and Applications, Ed. New York: Springer 2004.

[73] A. Chowdhury, R. Giri, A. Ghosh, S. Das, A. Abraham, and V. Snasel, "Linear antenna array synthesis using fitness-adaptive differential evolution algorithm," IEEE Congress on Evolutionary Computation (CEC), pp. 1-8, 18-23 July 2010.

[74] W.-C. Weng, F. Yang, and A. Z. Elsherbeni, "Linear Antenna Array Synthesis Using Taguchi's Method: A Novel Optimization Technique in Electromagnetics," IEEE Transactions on Antennas and Propagation, vol. 55, pp. 723-730, 2007.

[75] A. Smida, R. Ghayoula, A. Troudi, H. Trabelsi, and A. Gharsallah, "Beam synthesis of phased circular antenna arrays using Taguchi method," 9th International Conference on Communications (COMM), pp. 155-158, 21-23 June 2012.

[76] M. S. Sharawi, F. Sultan, and D. N. Aloi, "An 8-Element Printed V-Shaped Circular Antenna Array for Power-Based Vehicular Localization," IEEE Antennas and Wireless Propagation Letters, vol. 11, pp. 1133-1136, 2012.

[77] W. Zhou, N. H. Noordin, N. Haridas, A. O. El-Rayis, A. T. Erdogan, and T. Arslan, "A WiFi/4G compact feeding network for an 8-element circular antenna array," Loughborough Antennas and Propagation Conference (LAPC), pp. 1-4, 14-15 Nov. 2011.

[78] J.-H. Lim, G.-T. Back, Y.-I. Ko, C.-W. Song, and T.-Y. Yun, "A Reconfigurable PIFA Using a Switchable PIN-Diode and a Fine-Tuning Varactor for USPCS/WCDMA/m-WiMAX/WLAN," IEEE Transactions on Antennas and Propagation, vol. 58, pp. 2404-2411, 2010.

[79] A. Khaleghi and M. Kamyab, "Reconfigurable Single Port Antenna With Circular Polarization Diversity," IEEE Transactions onAntennas and Propagation, vol. 57, pp. 555-559, 2009.

[80] A. Ghasemi, N. Ghahvehchian, A. Mallahzadeh, and S. Sheikholvaezin, "A reconfigurable printed monopole antenna for MIMO application," 6th European Conference on Antennas and Propagation (EUCAP2012), pp. 1-4, 26-30 March 2012.

[81] B. Y. Toh, R. Cahill, and V. F. Fusco, "Understanding and measuring circular polarization," IEEE Transactions on Education, vol. 46, pp. 313-318, 2003.

[82] J. D. Jackson, Classical Electrodynamics John Wiley & Sons Inc, Third edition 1998.

[83] X. M. Qing and Y. W. M. Chia, "Circularly polarised circular ring slot antenna fed by stripline hybrid coupler," Electronics Letters, vol. 35, pp. 2154-2155, 1999.

[84] Y.-F. Lin, H.-M. Chen, and S.-C. Lin, "A New Coupling Mechanism for Circularly Polarized Annular-Ring Patch Antenna," IEEE Transactions on Antennas and Propagation, vol. 56, pp. 11-16, 2008.

[85] K.-F. Tong and T.-P. Wong, "Circularly Polarized U-Slot Antenna," IEEE Transactions on Antennas and Propagation, vol. 55, pp. 2382-2385, 2007.

[86] I. C. Deng, J.-B. Chen, Q.-X. Ke, J.-R. Chang, W.-F. Chang, and Y.-T. King, "A circular CPW-FED slot antenna for broadband circularly polarized radiation," Microwave and Optical Technology Letters, vol. 49, pp. 2728-2733, 2007.

[87] M. K. A. Rahim, T. Masri, O. Ayop, and H. A. Majid, "Circular Polarization Array Antenna," Asia-Pacific Microwave Conference, 2008. APMC 2008., pp. 1-4, 16-20 Dec. 2008.

[88] B. Luo, Y. Wu, and J. Li, "Design of Four-Element Dual-Frequency Circular-Polarization Microstrip Array Antenna," 5th International Conference on Wireless Communications, Networking and Mobile Computing, 2009. WiCom '09., pp. 1-4, 24-26 Sept. 2009.

[89] A. H. Abdelrahman, F. Elhefnawi, A. Z. Elsherbeni, M. Hendi, and S. Elramly, "Compact circularly-polarized microstrip array antenna," Loughborough Antennas and Propagation Conference (LAPC), pp. 113-116, 8-9 Nov. 2010.

[90] S. L. S. Yang, R. Chair, A. A. Kishk, K.-F. Lee, and K.-M. Luk, "Study on Sequential Feeding Networks for Subarrays of Circularly Polarized Elliptical Dielectric Resonator Antenna," IEEE Transactions on Antennas and Propagation, vol. 55, pp. 321-333, 2007.

[91] C. H. Weng, H. W. Liu, C. H. Ku, and C. F. Yang, "Dual circular polarisation microstrip array antenna for WLAN/WiMAX applications," Electronics Letters, vol. 46, pp. 609-611, 2010.

[92] Y. Ushijima, S. Feng, E. Nishiyama, and M. Aikawa, "A novel circular polarization switchable slot-ring array antenna with orthogonal feed circuit," Asia-Pacific Microwave Conference Proceedings (APMC), pp. 1569-1572, 7-10 Dec. 2010.

[93] D. Piazza, N. J. Kirsch, A. Forenza, R. W. Heath, and K. R. Dandekar, "Design and Evaluation of a Reconfigurable Antenna Array for MIMO Systems," Antennas and Propagation, IEEE Transactions on, vol. 56, pp. 869-881, 2008.

[94] P. D. D. S. HSMP-389D, AVAGO TECHNOLOGIES.

[95] S.-H. Wi, Y. P. Zhang, H. Kim, I.-Y. Oh, and J.-G. Yook, "Integration of Antenna and Feeding Network for Compact UWB Transceiver Package," IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 1, pp. 111-118, 2011.

[96] S. Hebib and H. Aubert, "Triband antenna feeding circuit for circular polarization diversity," 41st European Microwave Conference (EuMC), 2011 pp. 890-893, 10-13 Oct. 2011.

[97] J. L. Robert, P. Minard, and A. Louzir, "Feeding Concept for a Multisector Antenna System," Microwave Conference, 2008. EuMC 2008. 38th European, pp. 1102-1105, 27-31 Oct. 2008.

[98] F. Prototype Board (PCB, 100 x 160, SS, 400-034-1), Mega Electronics.

[99] M. F. Ismail, M. K. A. Rahim, and H. A. Majid, "The Investigation of PIN diode switch on reconfigurable antenna," IEEE International RF and Microwave Conference (RFM), pp. 234-237, 12-14 Dec. 2011.

[100] T. D. Nguyen, Y. Duroc, V. Y. Vu, and T. P. Vuong, "Novel reconfigurable 8 - shape PIFA antenna using PIN diode," International Conference on Advanced Technologies for Communications (ATC2011), pp. 272-275, 2-4 Aug. 2011.

[101] B. Kim, B. Pan, S. Nikolaou, Y.-S. Kim, J. Papapolymerou, and M. M. Tentzeris, "A Novel Single-Feed Circular Microstrip Antenna With Reconfigurable Polarization Capability," IEEE Transactions on Antennas and Propagation, vol. 56, pp. 630-638, 2008.

[102] H.-L. Peng, R. Tao, W.-Y. Yin, and J.-F. Mao, "A Novel Compact Dual-Band Antenna Array With High Isolations Realized Using the Neutralization Technique," IEEE Transactions on Antennas and Propagation, vol. 61, pp. 1956-1962, 2013.

[103] W. Zhou and T. Arslan, "A bidirectional planar monopole antenna array for WiFi/Bluetooth and LTE mobile applications," Loughborough Antennas and Propagation Conference (LAPC2013), pp. 190-193, 11-12 Nov. 2013.

[104] F. K. Mirzaee, S. A. Mirtaheri, and S. Chamaani, "Design and analysis of a band-notched UWB 1 to 4 Wilkinson power divider using symmetric defected ground structure," Proceedings of the 5th European Conference on Antennas and Propagation (EUCAP), pp. 860-864, 11-15 April 2011.

[105] L. Yang and Q.-X. Chu, "Design of a compact UWB Wilkinson power divider," International Conference on Microwave and Millimeter Wave Technology (ICMMT 2008), pp. 360-362, 21-24 April 2008.

[106] L. Young, "Tables for Cascaded Homogeneous Quarter-Wave Transformers," IRE Transactions on Microwave Theory and Techniques, vol. 7, pp. 233-237, 1959.

[107] S. B. Cohn, "A Class of Broadband Three-Port TEM-Mode Hybrids," IEEE Transactions on Microwave Theory and Techniques, vol. 19, pp. 110-116, 1968.

[108] L. Stark, "A helical line scanner for beam steering a linear array," IRE Transactions on Antennas and Propagation, vol. 5, pp. 211-216, 1957.

[109] S. K. Koul and B. Bhat, Microwave And. Millimeter Wave Phase Shifters, Volume-I, Dielectric and Ferrite Phase Shifters, Artech House 1993.

[110] S. K. Koul and B. Bhat, Microwave and Millimeter Wave Phase Shifters, Volume-II, Semiconductor and Delay Line Phase Shifter, Artech House 1991.

[111] F. Reggia and E. G. Spencer, "A New Technique in Ferrite Phase Shifting for Beam Scanning of Microwave Antennas," Proceedings of the IRE, vol. 45, pp. 1510-1517, 1957.

[112] G. M. Rebeiz, RF MEMS Theory Design and Technology, John Wiley and Sons Publications, Hoboken, New Jersey 2003.

[113] S. Subbiah, A. Alphones, and T. E. Leong, "Characteristics of microstrip line on YIG–GGG substrate under arbitrary orientation of magnetization," Microwave and Optical Technology Letters, vol. 32, pp. 29-35, 2002.
[114] S. Subbiah and A. Alphones, "Tunable isolator using a coupled microstrip line with an obliquely magnetised YIG substrate," Microwaves, Antennas and Propagation, IEE Proceedings, vol. 150, pp. 219-222, 2003.
[115] I. Viswanathan, High Performance Compact Microstripline Phase Shifter At C-Band Using Yttrium Iron Garnet, MS thesis dissertation Northeastern University Boston MA 2009.
[116] G. McFeetors and M. Okoniewski, "Distributed MEMS analog phase shifter with enhanced tuning," IEEE Microwave and Wireless Components Letters, vol. 16, pp. 34-36, 2006.
[117] M. Skolnik, Radar Handbook, McGraw-Hill, USA, 3rd edition 2008.
[118] J. F. White, "Diode Phase Shifters for Array Antennas," Microwave Theory and Techniques, IEEE Transactions on, vol. 22, pp. 658-674, 1974.
[119] H. Hayashi and M. Mauraguchi, "An MMIC active phase shifter using a variable resonant circuit [and MESFETs]," IEEE Transactions on Microwave Theory and Techniques, vol. 47, pp. 2021-2026, 1999.
[120] N. S. Barker and G. M. Rebeiz, "Optimization of distributed MEMS transmission-line phase shifters-U-band and W-band designs," IEEE Transactions on Microwave Theory and Techniques, vol. 48, pp. 1957-1966, 2000.
[121] A. S. Nagra, X. Jian, E. Erker, and R. A. York, "Monolithic GaAs phase shifter circuit with low insertion loss and continuous 0-360 deg phase shift at 20 GHz," IEEE Microwave and Guided Wave Letters, vol. 9, pp. 31-33, 1999.
[122] E. G. Erker, A. S. Nagra, Y. Liu, P. Periaswamy, T. R. Taylor, J. Speck, and R. A. York, "Monolithic Ka-band phase shifter using voltage tunable BaSrTiO3 parallel plate capacitors," IEEE Microwave and Guided Wave Letters, vol. 10, pp. 10-12, 2000.
[123] Y. Liu, MEMS and BST Technologies for Microwave Applications, PhD Thesis Dissertation, UCSB 2002.
[124] H.-T. Kim, J.-H. Park, S. Lee, S. Kim, J.-M. Kim, Y.-K. Kim, and Y. Kwon, "V-band 2-b and 4-b low-loss and low-voltage distributed MEMS digital phase shifter using metal-air-metal capacitors," IEEE Transactions on Microwave Theory and Techniques, vol. 50, pp. 2918-2923, 2002.
[125] J. Qing, Y. Shi, W. Li, Z. Lai, Z. Zhu, and P. Xin, "Ka-band distributed MEMS phase shifters on silicon using AlSi suspended membrane," Journal of Microelectromechanical Systems, vol. 13, pp. 542-549, 2004.
[126] G. Wang, M. Romeo, C. Henderson, and J. Papapolymerou, "Novel Reliable RF Capacitive MEMS Switches With Photodefinable Metal-Oxide Dielectrics," Journal of Microelectromechanical Systems, vol. 16, pp. 550-555, 2007.
[127] HMC928LP5E Analog Phase Shifter, Hittite Microwave Corporation.
[128] Y.-G. Kim, K. W. Kim, and Y.-K. Cho, "An ultra-wideband microstrip-to-CPW transition," IEEE MTT-S International Microwave Symposium Digest, pp. 1079-1082, 15-20 June 2008.
[129] D. F. Filipovic, R. F. Bradley, and G. M. Rebeiz, "A planar broadband balanced doubler using a novel balun design," IEEE Microwave and Guided Wave Letters, vol. 4, pp. 229-231, 1994.
[130] PIC18F4550 Data Sheet, Microchip Technology Inc, 2009.
[131] LPC1768 Data Sheet, NXP Semiconductors, 2014.
[132] AD5290 Data Sheet, Analog Devices Inc. 2014.
[133] NJM2360 Data Sheet, New Japan Radio Co.Ltd. 2013.
[134] FT232R USB UART I.C. Data Sheet, Future Technology Devices International Ltd. 2005.
[135] http://www.multi-circuit-boards.eu/en/.
[136] http://www.microchip.com/.
[137] http://orwelldevcpp.blogspot.co.uk/.
[138] http://www.visualstudio.com/.
[139] http://www.flashmagictool.com/.
[140] http://ttssh2.sourceforge.jp/index.html.en.