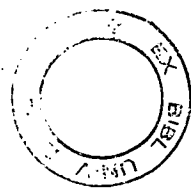# Application of CMP and Wafer Bonding for Integrating CMOS and MEMS Technology

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Abstract

Microelectromechanical systems (MEMS) can provide an interface between the digital electronic world and the analog physical world. Depended on the transduction mechanisms, various micromechanical structures are designed to ensure the transductions with highest efficiency. As a consequence, MEMS devices have to be fabricated using a broad range of techniques, and often require integration with the CMOS circuitry.

The feasibility of a new fabrication approach has been investigated in this thesis, which uses chemical mechanical polishing (CMP) and oxygen plasma assisted low temperature wafer bonding, to integrate prefabricated MEMS and CMOS devices. Fabricating MEMS and CMOS devices on separate wafers enables the optimisation of each technology separately. However, to integrate them requires low temperature bonding of processed wafers, connecting the bonded wafer pair and bringing the electrical signals to the top surface. Test structures have been used to investigate the feasibility of bonding MEMS and CMOS wafers to create an integrated system with electrical connections. Bonding and thinning of prefabricated wafers has been demonstrated using a CMP enabled surface planarisation process and plasma assisted low temperature wafer bonding. Inter-wafer connections can be achieved using two fabrication methods. With oxide to oxide bonding method, resistances of 3.8 - 5.2 Ω have been obtained for the via chain test structures with 9-13 contact vias, whilst an average specific contact resistivity of $1.7 \times 10^{-8}\Omega \cdot cm^2$ has been achieved from the single via test structure. Direct electrical connections between wafers has also been implemented during the bonding anneal stage with an average contact resistance of 2.6×10^{-8} $\Omega \cdot cm^2$.

Declaration of originality

I hereby declare that the research recorded in this thesis and the thesis itself was composed and originated entirely by myself in the School of Engineering and Electronics at The University of Edinburgh. This work has not been submitted for any other degree or professional qualification.

Huamao Lin

Acknowledgements

A special thank you to my parents, sister and other family members for their constant encouragement and support. The most important person I wish to thank is my wife, Huihong Li, for always being there with love and support over the last four years, even though it has meant many sacrifices. I would never have managed to finish this work without her encouragement, patience and understanding.

Publications

Publications by the author relevant to this work include:

1. **H. Lin**, J.T.M. Stevenson, A.M. Gundlach, C.C. Dunare, and A.J. Walton, "Application of CMP for Integrating MEMS and CMOS Technology", *16th European Workshop on MicroMechanics*, pp. 207-210, 2005.

2. **H. Lin**, A.J. Walton, C.C. Dunare, J.T.M. Stevenson, A.M. Gundlach, S. Smith, and A.S. Bunting, "Test Structure for the Characterization of MEMS and CMOS Integration Technology", in *Proceeding of IEEE International Conference on Microelectronic Test Structures*, pp. 143-148, 2006.

3. S. Enderling, **H. Lin**, J.T.M. Stevenson, A.S. Bunting, and A.J. Walton, "Characterisation of a CMP Nanoscale Planarisation-based Process for RF MEMS Resonators", *Proceeding of SPIE: Micro- and Nanotechnology - Materials, Processes, Packaging, and Systems III*, vol. 6415, p. 64150G, 2006.

4. A. J. Walton, J. T. M. Stevenson, I. Underwood, J.G. Terry, S. Smith, W. Parkes, C. Dunare, **H. Lin**, Y. Li, R. Henderson, D. Renshaw, K. Muir, M. Desmulliez, B. Flynn, A. F. Murray, T.B. Tang, A. Bunting, and A.M. Gundlach, "Integration of IC technology with MEMS: Silicon^{+} technology for the future", *IET Seminar on Micro-Electro-Mechanical Systems, MEMS Technology*, pp. 1-11, 2007.

5. **H. Lin**, J.T.M. Stevenson, A.M. Gundlach, C.C. Dunare, and A.J. Walton, "Direct Al-Al Contact using Low Temperature Wafer Bonding for Integrating MEMS and CMOS Devices", in *Proceeding of 33rd International Conference on Micro- and Nano-Engineering*, pp. 357-358, 2007.

6. **H. Lin**, S. Smith, J.T.M. Stevenson, A.M. Gundlach, C.C. Dunare, and A.J. Walton, "An Evaluation of Test Structures for Measuring the Contact Resistance of 3-D Bonded Interconnects", accepted by *IEEE International Conference on Microelectronic Test Structures 2008*.

7. **H. Lin**, A.J. Walton, C.C. Dunare, J.T.M. Stevenson, A.M. Gundlach, S. Smith, and A.S. Bunting, "Test Structures for the Characterisation of MEMS and CMOS Integration Technol-

ogy", accepted by *IEEE Transactions on Semiconductor Manufacturing*.

8. **H. Lin**, J.T.M. Stevenson, A.M. Gundlach, C.C. Dunare, and A.J. Walton, "Direct Al-Al Contact using Low Temperature Wafer Bonding for Integrating MEMS and CMOS Devices", manuscript submitted to journal *Microelectronic Engineering*.

Contents

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Acronyms and abbreviations

AFM	Atomic Force Microscope
BCB	Benzocyclobutane
BEOL	Back-End Of the Line
BiCMOS	A combinded Bipolar and CMOS device
CCD	Charge Coupled Device
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Planarization or Polishing
CVD	Chemical Vapour Deposition
DI	Deionised
DRAM	Dynamic Random Access Memory
DRIE	Deep Reactive Ion Etching
FIB	Focused Ion Beam
FET	Field Effect Transistor
FEOL	Front-End Of the Line
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
ILD	Inter Layer Dielectric
IR	Infrared
MEMS	Microelectromechanical Systems
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PECVD	Plasma Enhanced Chemical Vapor Deposition
RF	Radio Frequency
RIE	Reactive Ion Etching
RPM	Revolutions Per Minute
SEM	Scanning Electron Microscope
SOI	Silicon On Insulator
SRAM	Static Random Access Memory
UV	Ultraviolet

Nomenclature

A_c	Contact area
E	Young's modulus of the wafer
K_p	Preston coefficient
P	Applied downward pressure during CMP
R	CMP removal rate
R_c	Contact resistance
R_{post}	Radius of the curvature after film deposition
R_{pre}	Radius of the curvature before film deposition
t_f	Film thickness
t_s	Substrate thickness
v	Linear relative wafer-pad velocity
w	Line width of the test structure
α_T	Tensile strength of bonded wafer
γ	Surface energy of bonded wafer
ρ	Bulk resistivity
ρ_c	Specific contact resistivity
ρ_g	Contact resistivity extracted from stacked Greek cross test structure
ρ_k	Specific contact resistivity extracted from Kelvin test structure
σ	Stress of thin film
ν	Poisson's ratio
ω_t	Rotational velocity of the polishing table
ω_c	rotational velocity of the wafer carrier

Chapter 1
Introduction

1.1 Introduction

This chapter provides an introduction to the subject of integrating CMOS[1] (complementary metal oxide semiconductor) electronics with MEMS (microelectromechanical systems) devices. The advantages of the CMOS-MEMS integration and the available fabrication approaches are presented. A novel approach is introduced, which is based on the concept that CMOS and MEMS devices are fabricated on separate wafers, and the integration can then be performed using chemical mechanical planarisation and wafer bonding. The challenges and uncertainties of the proposed approach, such as bonding of prefabricated wafers and creating interconnects between the bonded wafer-pair, form the backbone of this research work.

1.2 Background

MEMS represents a broad range of small mechanical structures ranging from a few micrometers to tens of millimetres which can be used to convert real world signals from one form of energy to another [1]. Different from traditional mechanical manufacturing, MEMS fabrication technology is based on the lithographic pattern transferring process, which has the advantage to be able to fabricate hundreds and thousands of identical devices in one substrate in parallel (i.e. a batch processing method). A wide variety of MEMS devices, also termed microsensors and microactuators, have been developed to replace their traditional mechanical counterparts, or invented to be used for many new applications which are otherwise impossible to make [2–4].

MEMS devices have been used for automotive industry, medical and biotechnology applications, environmental monitoring, information technology (IT) and its peripherals, telecommunications and industrial/automation applications. Currently, the commercially successful MEMS

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[1]CMOS has been used in this thesis to represent all types of semiconductor devices, such as bipolar and BiCMOS (a combined bipolar and CMOS device), because: (1) CMOS is the dominate device architecture in digital applications, therefore, it is more likely that MEMS devices are required to be integrated with a CMOS circuit in practice, (2) CMOS-MEMS integration has been conventionally used in literature for this topic.

1

products include microdisplays, inkjet nozzles, pressure sensors, accelerators, gyroscopes, microphones, and others. The MEMS market is expected to grow from U.S. $ 5.1 billions in 2005 to U.S. $ 9.7 billions in 2009, with an annual growth rate close to 15% [5]. The top 15 MEMS companies and their revenues from 2004 to 2006 are listed in Table 1.1, and the forecast of the market shares divided by the application areas is shown in Fig. 1.1. It has been forecasted that a rapid rise of the consumer electronics segment is expected in the next five years in MEMS industry [6], with more and more conventional semiconductor companies being involved in MEMS manufacturing [5].

Rank	MEMS manufacturer	2004	2005	2006	AGR 06/05
1	Texas Instruments	850	780	883	13%
2	Hewlett Packard	687	750	820	9%
3	Robert Bosch	260	325	375	15%
4	Lexmark	201	230	313	36%
5	Seiko Epson	194	199	231	16%
6	STMicroelectronics	200	200	220	10%
7	Canon	161	184	214	16%
8	Freescale	157	182	210	15%
9	Analog Devices	131	133.6	170	27%
10	Denso	118	136	170	26%
11	GE Infrastructure Sensing	120	132	152	15%
12	Systron Donner	171	190	141	-26%
13	Honeywell	102	117	120	3%
14	Delphi Delso Electronics	116	116	116	0%
15	Infineon Technologies	77	88	101	15%

Table 1.1: *List of top 15 MEMS manufacturers in 2006 [5].*
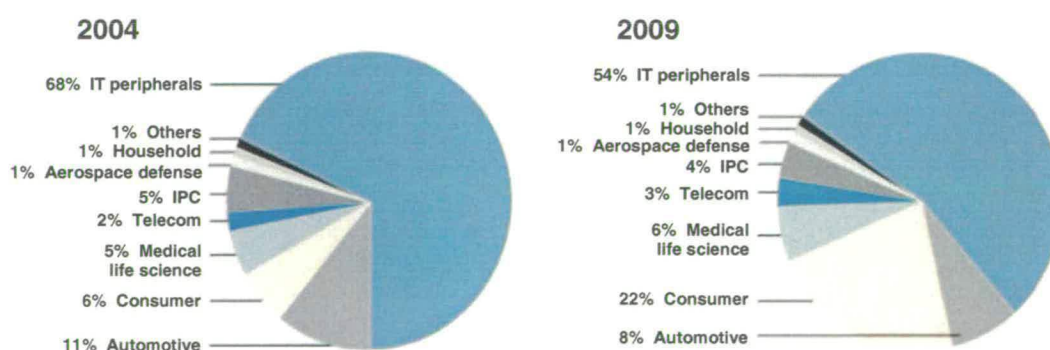
Figure 1.1: *MEMS market by the application fields (2004-2009) [6].*

MEMS devices can provide an interface between the digital electronic world dominated by the integrated circuits (IC) and the analog physical world. Due to the wide variety of non-electrical

signals of interest in the physical world, many different transduction mechanisms are needed to transduce physical signals into electrical signals (i.e. sensors), as well as from electric signals into physical signals (i.e. actuators). Sometimes these sensing and actuating mechanisms can be combined with electronics to form a complete microsystem. Besides the batch fabrication advantage, MEMS devices have two other major advantages over the traditional mechanical sensors and actuators: (1) advantageous scaling properties: some physical phenomena perform better or are more efficient when miniaturised to the micrometer scale [1,3]; (2) possibility of integrating with CMOS IC: both CMOS and MEMS use a batch fabrication method in a clean-room environment and share many common materials, fabrication processes and equipment.

The integration of MEMS devices with their signal processing and controlling CMOS electronics, has attracted great interest because it potentially provides overwhelming advantages in terms of performance, reliability and cost [7–9]. Taking a gyroscope as an example (Fig. 1.2), a signal of two orders of magnitude smaller can be handled when the pre-amplifiers and signal conditioning circuits are integrated with the sensing part compared with a stand-alone sensor [7]. Therefore, smaller sensor size maintains a similar signal to noise level, which can reduce problems caused by non-uniformity of stress distribution in various semiconductor thin films, hence results in a more robust device. Moreover, a smaller sensor size can also increase the number of devices fabricated on the same silicon area, and improve the fabrication yield assuming a similar defect rate. Fabrication cost can be further reduced due to less packaging being required for the integrated system. Other advantages include reduced system size which is important for implantable medical applications, and high density electrical interconnects between CMOS and MEMS which is essential for any array type devices.

The advantage of the CMOS-MEMS integration can be further strengthened by the need to calibrate or tune the MEMS device after the packaging process. Because of the mechanical nature of many MEMS, parasitic stress introduced during packaging may change the performance of the device. As a result, calibration and compensation must often be added, which, in many cases, cost more than the MEMS device, and also cause significant yield loss and reduced reliability [10]. The integrated MEMS device with built-in EEPROM (electrically erasable programmable read-only memory) or electrical programming circuits have proved to be a very attractive alternative [9].

The available approaches for fabricating MEMS devices and CMOS electronics on the same wafer can be divided into three categories:

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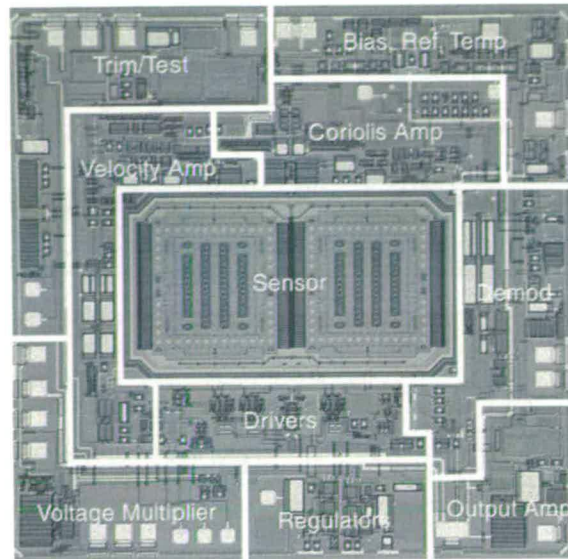
Figure 1.2: *Image of an integrated gyroscope developed by Analog Devices [7].*

- The MEMS devices are fabricated and encapsulated in dielectric layers before the standard CMOS process (pre-CMOS) [11–15].

- CMOS wafers are fabricated by foundries and the MEMS is processed afterwards (post-CMOS) [8, 16–21].

- Completely integrated CMOS and MEMS processes (hybridisation) [22–24].

Although each of these approaches has their own advantages and successful examples [8, 9], they also have their limitations. For example, pre-CMOS approach requires a foundry that is willing to accept MEMS processed wafers due to the contamination and planarisation concerns, whilst the post-CMOS approach limits MEMS process steps to temperatures less than 450 °C since metal structures in fabricated wafers cannot stand higher temperature. The fully integrated approach requires access to both CMOS and MEMS technologies, demanding significant investments on equipment. A more comprehensive comparison of the available options are listed in Table 1.2 and more detailed analysis of this will be presented in chapter 2.

1.3 Motivation and scope of the thesis

In this thesis a new approach is proposed, based on the concept that CMOS and MEMS devices are fabricated on separate wafers, and they can then be integrated by a wafer bonding process. The most important advantage of the new approach is the flexibility of being able to fabricate

	Process	Cost barrier to entry	Wafer scale	Pre-tested dies	Commercial availability	Die assembly
a	Pre-CMOS integration	Medium - High	Yes	No	Limited	No
b	Post-CMOS integration	Medium	Yes	No	Available for some processes	No
c	Fully integrated CMOS and MEMS	High	Yes	No	Extremely limited	No
d	CMOS and MEMS with etch release	Medium - Low	Yes	No	Yes	No
e	Chip to chip (or die to die)	Low	No	Yes	Yes	Yes
f	Multi-chip module	Low	No	Yes	Yes	Yes
g	CMOS-MEMS wafer bonding	Medium	Yes	No	No	No

Table 1.2: *Comparison of different CMOS-MEMS integration technologies [25].*

CMOS and MEMS devices separately which enables the full optimisation of both fabrication technologies. Although the supporting technologies, such as chemical mechanical polishing (CMP), plasma assisted low temperature wafer bonding and standard interconnect technology, are available, there are still many challenges and uncertainties for the new integration approach, which forms the backbone of this research work.

1.4   Arrangement of the thesis

This thesis is divided into 9 chapters and the following gives a brief description of the chapters that follow:

Chapter 2. Chapter 2 describes the technologies involved in the CMOS-MEMS integration. The fabrication technologies of CMOS and MEMS are briefly introduced, and the current status of CMOS-MEMS integration technology presented. The advantages and difficulties of the available integration approaches are discussed.

Chapter 3. The CMP process has been used to achieve local as well as global planarisation across the entire wafer by preferential removal of protruding material on the wafer surface through a combination of mechanical and chemical action. An overview of the CMP process is presented in this chapter.

Chapter 4. Wafer bonding provides means of joining two wafers to form an integrated entity, which is the core process of the proposed integration approach. An overview of the wafer bonding technology is presented in this chapter.

Chapter 5. Chapter 5 examines the issues and developments associated with bonding prefabricated wafers, which is one of the most crucial steps in the proposed CMOS-MEMS integration approach, using CMP and oxygen plasma assisted low temperature wafer bonding.

Chapter 6. The provision of electrical interconnects between bonded MEMS and CMOS wafers is another key step of this new integration approach. Two inter-wafer connection methods are evaluated in this thesis. In one method, processed wafers are aligned and bonded using PECVD oxide as a direct bonding material. Interconnects between wafers are then established through specific designed contact vias using a standard multilevel metallisation process. The detailed fabrication process development and results of this interconnection scheme are presented in this chapter.

Chapter 7. Chapter 7 presents test structures to characterise the electrical interconnects between bonded wafers. Two types of test structures: cross-bridge Kelvin resistors and a stacked Greek cross test structure have been evaluated using an interconnect simulation software. These two structures have also been fabricated and electrically compared by using a two-level aluminium (Al) metallisation process.

Chapter 8. Chapter 8 presents the process developments and results of the second inter-wafer connection method, which uses direct metal contact at the wafer bonding stage to provide interconnections between the integrated MEMS and CMOS wafers.

Chapter 9. Chapter 9 summarises the results and presents the overall conclusions. In addition, possible future work is suggested.

Chapter 2
CMOS and MEMS Integration

2.1 Introduction

This chapter describes the technologies involved in the CMOS-MEMS integration. Firstly the fabrication technologies of CMOS and MEMS are introduced with a brief analysis of the probabilities and challenges for fabricating an integrated CMOS-MEMS system. The current status of CMOS-MEMS integration technology is then presented, and the advantages and difficulties of the available approaches are discussed. Integration through chip to chip bonding and chip to wafer bonding are also briefly introduced in this chapter.

It should be noted that the fabrication technologies of CMOS and MEMS, together with their integration are all big research and development topics, with numerous insightful and comprehensive books and technical articles available [3, 26–33]. This chapter focuses on introducing the basic principles of these technologies and presents some recent achievements.

2.2 CMOS IC fabrication technology

2.2.1 CMOS IC fabrication

IC fabrication has enabled the manufacture of devices and systems, based on the repetition of several basic process steps to produce the desired structures [34, 35]. Thin layers of metal and dielectric materials are sequentially deposited and patterned on semiconductor substrates, using techniques such as chemical vapour deposition (CVD) and sputtering, lithography masking, etching and CMP. Additional processes, such as oxidation, doping and heat treatment are used to further modify material properties of individual layers. Fig. 2.1 illustrates a simplified IC fabrication flow chart, based on four most commonly used process steps, to build up a devices layer by layer. It should be noted that the key difference from other manufacturing technologies is that, in IC fabrication, pattern and assembly occur simultaneously in a batch process manner.

Fig. 2.2 shows a typical sub-micron (0.5-1.0 μm) twin-well CMOS device with two-level metal
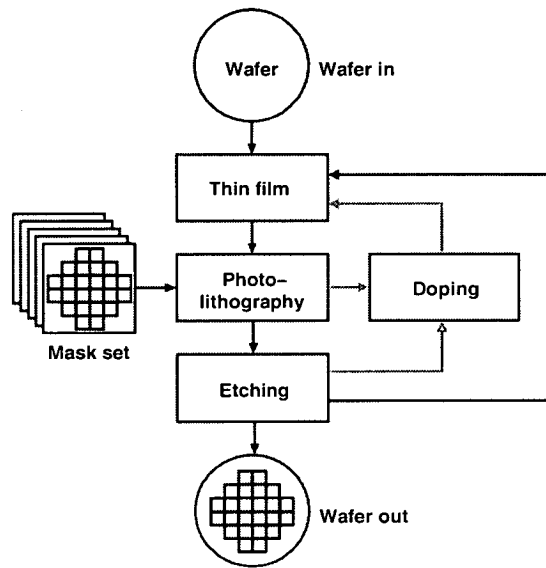
Figure 2.1: *Flow diagram of IC fabrication process using the basic microfabrication techniques: thin film (including growth and deposition), photolithography, etching and doping [34, 35].*

interconnect layers, which is one of the most commercially favoured CMOS technologies used for CMOS-MEMS integration [35]. For this CMOS device, the fabrication starts with a p-type (100) silicon substrate, and p-well and n-well are formed using ion implantation and diffusion processes. Through the subsequent steps, such as field oxidation, gate oxidation, polysilicon deposition, p^+ and n^+ ion implantations and diffusions, both n-channel and p-channel MOS devices with lightly-doped source and drain (LDD) are fabricated. The two metal interconnect layers are then fabricated using tungsten plugs, TiN silicide and Al metallisation. Thermal oxide layers are used to isolate adjacent transistors (field oxidation) and form the gate oxide, whilst chemical vapour deposited silicon dioxide layers are used as dielectric layers between the metallisation levels. PECVD (plasma enhanced CVD) silicon nitride layers or silicon dioxide, silicon nitride sandwiches are employed as passivation layers, and many lithography, etch and CMP steps are used to achieve the desired device structures. It should be noted that many varieties of the semiconductor devices and fabrication sequences exist, and the sequence described here serves just as an illustration.
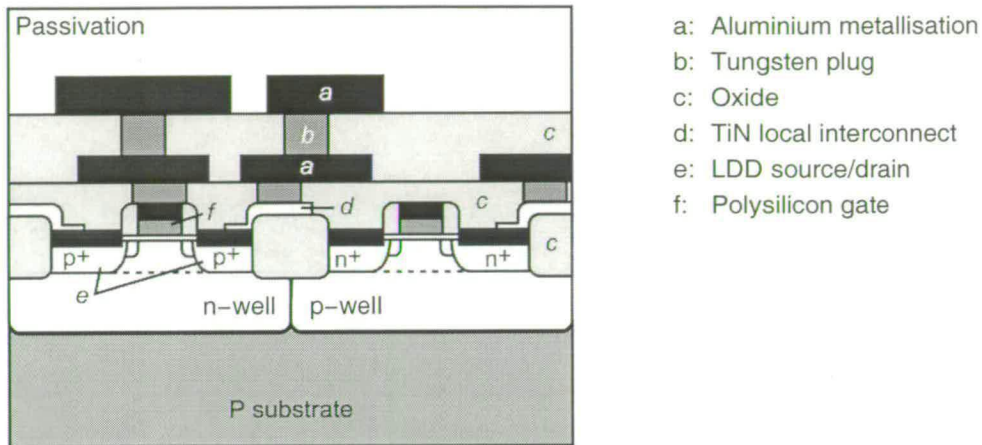
Figure 2.2: *Schematic cross-section of a typical twin-well CMOS device [35].*

2.2.2 Basic fabrication processes

Five of the most commonly used fabrication steps, namely photolithography, thin film, doping, etch and CMP, are briefly described in this section.

1. Photolithography. Photolithography, used to transfer patterns, is the core process of IC fabrication technology. In a photolithographic process, a photoresist layer, comprising an ultraviolet (UV) sensitive polymer, is spin-coated on to the material to be patterned (Fig 2.3(b)). The photoresist-coated substrate is then aligned with a mask and exposed to UV light through the mask in an aligner, as shown in Fig. 2.3(c). Depending on the generation of the lithography tool, the mask and substrate are brought in contact or close proximity (contact and proximity printing) or an image of the mask is projected (projection printing) on to the photoresist-coated substrate. Also, depending on whether positive or negative photoresist is used, the exposed or the unexposed photoresist areas, respectively, are removed during the resist development process (Fig. 2.3(d): positive photoresist is used). The remaining photoresist acts as a protective layer during the subsequent etching process, which transfers the pattern onto the underlying material (Fig.2.3(e)). Alternatively, the patterned photoresist can be used as a mask for subsequent ion implantation steps. After the etching or ion implantation, the remaining photoresist is removed, and the next layer deposition and pattern can be performed.

It should be noted that the desired device structures are patterned utilising patterns on the masks. The mask is a glass or quartz plate with a patterned opaque layer (typically chromium) on the surface. The patterns are designed using computer-aided-design software (e.g. Cadence)

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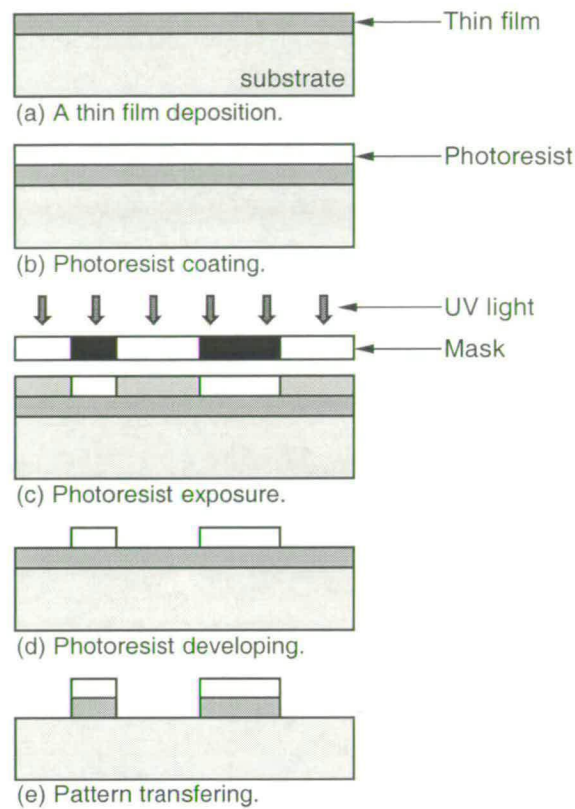
Figure 2.3: *Schematic of a photolithographic process sequence to pattern a thin film layer.*

and are typically written onto glass plates, layer by layer, using an electron-beam lithography process [26, 27, 35].

2. Thin film growth/deposition. Thin film oxides can be created by: (1) oxidation which grows a film on a silicon substrate, and (2) deposition which adds a film on top of a wafer surface. The difference of these two processes is that the former consumes silicon substrate, but the latter does not. The oxidation is typically performed in high temperatures (900-1100 °C) with dry, or wet processing conditions. Thermal oxide can be used to isolate one device from another (e.g. field oxide), and to act as a part of the MOS structures (e.g. gate oxide). The thickness of thermal oxide ranges from several nanometers to a few micrometers.

The two common thin-film deposition methods are chemical vapour deposition, which can be performed at low pressure (LPCVD), atmospheric pressure (APCVD) or as plasma-enhanced (PECVD), and physical vapour deposition (PVD), such as sputtering and evaporating. Deposited thin films in CMOS fabrication are used for several purposes: (1) to serve as a mask against implant or diffusion of dopant into silicon, (2) to provide passivation, and (3) to provide

electrical insulation and connection in the multi-level metal systems. Typical CVD and PVD film thicknesses are in the range of tenths of nanometers up to a few micrometers.

Other film deposition techniques include electro-plating of metal films (e.g. copper plating is used in the state-of-the-art CMOS metallisation [36]), and spin or spray coating of polymeric or dielectric films (e.g. polyimide and spin-on-glass (SOG) have been used to provide electrical insulation and device passivation). Both processes can yield film thicknesses from less than 1.0 μm up to several hundreds of micrometers.

3. Doping. Doping is used to modify the electrical conductivity of semiconductor materials such as single-crystal, poly-crystalline silicon and gallium arsenide. Doping silicon with phosphorus or arsenic yields n-type silicon, whereas p-type silicon results from boron doping. Dopant atoms are introduced by either ion implantation or diffusion from a gaseous, liquid or solid source. Nowadays, ion implantation, which is able to introduce a precisely defined quantities of dopant into a substrate, dominates the doping process in the semiconductor industry. In the ion implantation process, the substrate material is bombarded with accelerated ionised dopant atoms in an ion implanter. This results in an approximately Gaussian distribution [27, 28] of the dopant atoms in the substrate wafer, with a mean penetration depth controlled by the acceleration voltage. A high-temperature diffusion process can then be used to additionally drive-in the dopant until the desired doping profile has been achieved, for example, well formation. For shallow source and drain (S/D) formation, a high temperature short anneal process (rapid thermal processing, RTP) is performed. This activates the dopant and removes any possible defects in the substrate caused by the ion-bombardment, whilst maintaining a shallow doping profile.

4. Etching. Etch techniques consist of wet and dry etch methods, which use liquid chemicals and gas-phase chemistry, respectively. Both methods can be either isotropic (the same etch rate in all directions) or anisotropic (different etch rates in different directions), as illustrated in Fig. 2.4. The important criteria for selecting a particular etching process include the material etch rate, the selectivity for the material to be etched, and the isotropy/anisotropy of the etching process.

Dry etching is typically anisotropic, resulting in an accurate transfer of resist patterns, as undercut is minimised. Dry etch methods include plasma etching, reactive ion etching (RIE), sputtering, ion beam etching, and reactive ion beam etching. Using an RIE system as an exam-
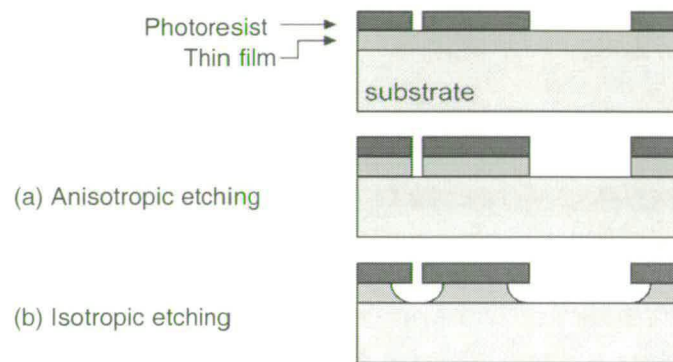
Figure 2.4: *Schematic of (a) anisotropic and (b) isotropic etching processes [35].*

ple, reactive ions are generated in a plasma and are accelerated towards the surface to be etched, thus providing directional etching characteristics. Higher ion energies typically result in more anisotropic etching characteristics, but also in reduced etching selectivity and increased surface damage. Important requirements for dry etching are a faithful reproduction of the lithographic pattern, etch-profile control, selectivity, uniformity, and low plasma induced surface defects and impurities.

Wet etching (usually isotropic) is still an important alternative to dry etch process due to its high-throughput and flexibility. With properly selected chemicals, etch reactions with the primary film are thermodynamically favoured over reactions with other films, and the selectivity can approach infinity. Wet etches are especially suitable for blanket etches of polysilicon, oxide, nitride and metal. A comprehensive review of various etching chemistries used in microfabrication can be found in [2, 37, 38].

5. Chemical mechanical polishing (CMP). To eliminate the difficulties of dry etching certain materials (e.g. Cu), a CMP process has been used as an alternative patterning process to fabricate the desired structures. In this process (illustrated in Fig. 2.5), an oxide layer is initially patterned using the fabrication sequence shown in Fig. 2.3. A blanket metal deposition is then performed to fill the oxide trenches (Fig. 2.5(b), resulting in a conformal coating. The subsequent polishing process tends to remove any material in high spots on the wafer surface through a combination of mechanical and chemical action, gradually planarising the wafer surface (Fig. 2.5(c)), and revealing the required metal structure, as shown in Fig. 2.5(d). Sub-micron feature sizes and various materials can be patterned using this process. It should be noted that metal dishing, dielectric erosion and surface contamination are the main concerns of this process. A detailed discussion of the CMP process will be presented in chapter 3.

(a) Patterned oxide layer.

(b) Blanket metal deposition.

(c) Metal layer polishing.

(d) After the CMP process.
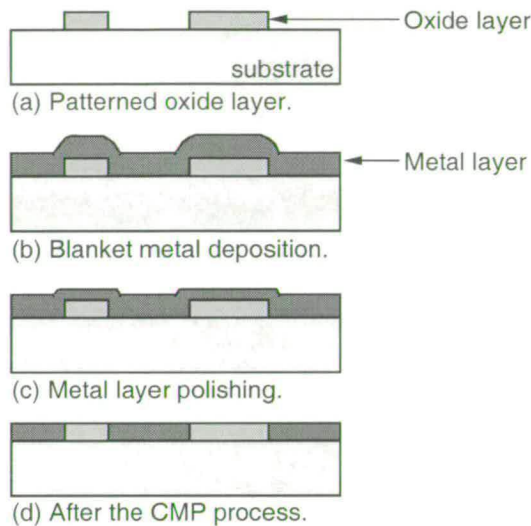
Figure 2.5: *Schematic of a metal damascene process.*

2.3 MEMS fabrication technology

Since many MEMS devices are fabricated on silicon substrates, the basic fabrication steps described in previous section (2.2) can all be used for MEMS fabrication. Additionally, several extra processes, such as surface micromachining, bulk micromachining, and wafer bonding, are also used to fabricate specific MEMS structures.

2.3.1 Surface micromachining

Surface micromachining refers to the fabrication of micromechanical structures using deposited thin films [32]. Thin films, such as polycrystalline silicon, silicon nitride and silicon dioxide, are sequentially deposited, patterned and then selectively removed to build complex multi-level structures. The concept of using sacrificial material [39, 40] has enabled the formation of movable parts in MEMS applications. The schematic of a surface micromachining process is illustrated in Fig. 2.6(a).

Polysilicon is the primary microstructural material due to its superior mechanical properties, and also its simple deposition procedure [39, 40]. It is typically deposited using gas-phase decomposition of silane in a low-pressure chemical vapour deposition furnace at temperatures ranging between 550 °C and 650 °C. Dopant can be added to the gas stream to form in situ doped films if required. The stress of the deposited polysilicon film is typically high, but can
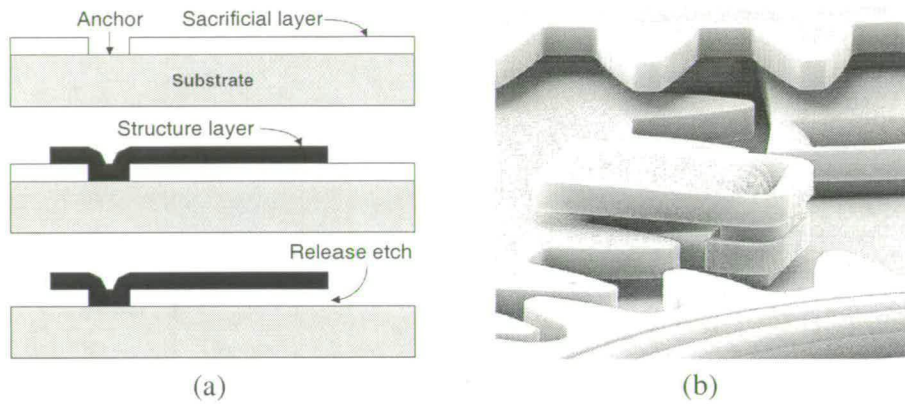
Figure 2.6: *Surface micromachining: (a) schematic of the surface micromachining process [1], and (b) a complex transmission system built using ultra low stress polysilicon deposition and CMP processes (also known as SUMMiT^{TM} technology, developed by Sandia National Laboratories [41, 42]).*

be reduced by further annealing at temperatures between 1000 °C and 1200 °C. One major problem in polysilicon constructed microstructures is the control of the mechanical properties of polysilicon, such as, residual stress, stress gradients through the film thickness, and the effective Young's modulus. These parameters have to be tightly controlled and monitored, as a small variation significantly affects the mechanical behaviour of fabricated device [32]. Another fabrication problem is surface topography which can be an issue when building complex multi-level structures. Fortunately, topography can be reduced using a CMP process [41, 42], as shown in Fig. 2.6(b).

The functionality of the microstructures is typically realised after the movable parts are freed from the substrate by removing the underlying sacrificial layers. However, release of these movable parts by selective wet etching often leads to stiction problems during the device drying process [32]. The stiction is caused by the surface tension of the liquid which results in the released free-standing structures becoming attached to the underlying layer after rinsing and drying. Stiction is a fundamental yield and reliability problem for surface micromachined devices. Several techniques have been developed to solve this problem, for example, the supercritical drying process [43].

2.3.2 Bulk micromachining

In bulk micromachining, substrate material (typically single-crystal silicon) is patterned and shaped to form an important functional component of the resulting device (the substrate does

not simply act as a rigid mechanical support, which is typically the case for surface microma-chining). The geometries of the etched features vary from fully isotropic (rounded, due to equal etch rates in all directions) to anisotropic (typically exhibiting perfectly flat surfaces and well-defined slopes), as illustrated in Fig. 2.7(a). By combining the layout design and an appropriate etching approach, many high-precision complex shapes, such as V-grooves (see Fig. 2.7(b)), channels, pyramidal pits, membranes, vias and nozzles, can be formed by bulk micromachining [2, 31].

Bulk micromachining can be classified into wet and dry etching depended on the phase of the reactant, liquid or gaseous, respectively, which can result in isotropic and anisotropic etching profiles. The fabrication conditions have been reported in numerous articles [2, 3, 31], and they will be not repeated here. As a significant amount of the substrate has to be etched during a typical bulk micromachining process, the main challenges of this technique are: etching uniformity control, etch-stop techniques and the protection of active layers.

(a) (b)
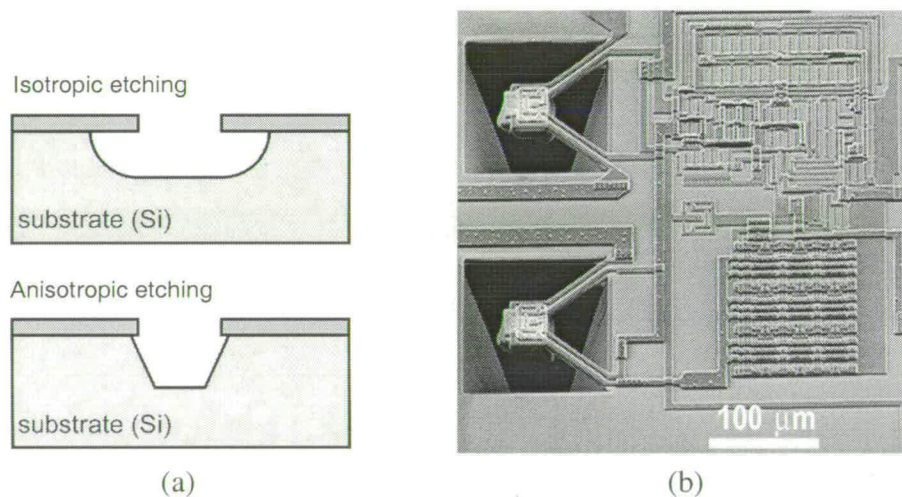
Figure 2.7: *Bulk micromachining: (a) schematic of the isotropic and anisotropic silicon etch-ing [35], (b) SEM (scanning electron microscope) photograph of two bulk-micromachined thermal converters which are integrated with a CMOS circuitry [31]. The MEMS devices are released from the front side of a CMOS wafer by anisotropic silicon etching (TMAH: tetra-methyl-ammorium-hydroxide).*

2.3.3 Wafer bonding

Silicon, glass, metal and polymeric substrates can be bonded together through fusion, anodic, metallic and adhesive bonding [33]. Wafer bonding in MEMS technology is typically per-

formed to achieve a structure that is difficult, or impossible to form otherwise (e.g. large cavities that are hermetically sealed, or a complex system with enclosed channels), or simply to add mechanical support and protection. Fig. 2.8 shows a cross-section of a micro-accelerometer fabricated using wafer bonding [44]. Wafer bonding is one of the key fabrication processes in this research work, and more detailed discussions of this process will be presented in chapter 4.
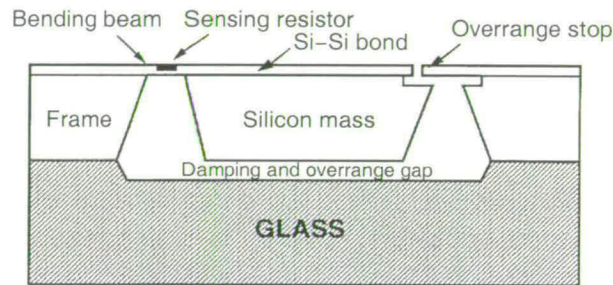
Figure 2.8: *A micro-accelerometer using wafer bonding developed by Lucas NovaSensor [44].*

2.4 Integration of MEMS and CMOS

2.4.1 Introduction

2.4.1.1 Similarities of CMOS and MEMS fabrication technologies

Both CMOS and MEMS use lithographic pattern transfer techniques as the core process, and the devices and microstructures are fabricated by repeatedly performing the basic processes. It is also the case that many CMOS and MEMS devices are fabricated on silicon substrates, and share many common films (e.g. silicon dioxide, silicon nitride, and Al) and fabrication processes (e.g. thin film, etch, lithography, doping, and CMP). Moreover, both CMOS and MEMS technologies utilise the similar manufacturing infrastructure, such as the cleanroom environment and fabrication equipment. These similarities suggest the feasibility of fabricating an integrated CMOS-MEMS system on the same substrate. However, the inherent differences between CMOS and MEMS, and the incompatibility in some of the fabrication technologies create many challenges for CMOS-MEMS integration.

2.4.1.2 Differences between CMOS and MEMS fabrication technologies

A major difference between MEMS and CMOS is that MEMS typically uses silicon (or other substrates, such as glass, polymer and ceramics) as a mechanical material, whilst CMOS de-

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vices use the electrical properties of the silicon substrate (or other materials, e.g. SiGe, AsGa). Based on this perspective, it is easy to understand that some elements such as Au, K^+, Na^+, which are regarded as killer defects for the CMOS IC devices, can be widely used for MEMS fabrication. On the other hand, whilst the built-in stress and strain in the films during the fabrication is usually of less concern for a CMOS IC, it can prevent a MEMS structure from working.

From the fabrication viewpoint, most CMOS IC technology can easily be customised with a change of the mask set, using the same process sequence to create the desired device. In comparison, a MEMS structure typically uses the underlying structures as part of the mechanical device. As a result, standardised processes and fabrication sequence often compromise device performance. Therefore, modifications and re-developments are often required to build each specific device. Moreover, many MEMS processes require double-sided processing, compared with the single-sided processing of a standard IC. This means extra demands are placed on wafer handling, wafer-edge and back-side protection.

2.4.1.3   Current status of the CMOS-MEMS integration

The available options for integrating MEMS devices with CMOS IC electronics can be classified into three types. The additional MEMS fabrication steps can be introduced before (pre-CMOS) [11–15] or after (post-CMOS) [8, 16–21] the regular CMOS processes, or they can be performed in-between the regular CMOS steps (hybridisation) [22–24,45–47]. In the case of post-CMOS micromachining, the microstructures can be built from either the CMOS layers themselves or from additional layers deposited after the CMOS fabrication. The detailed descriptions of these approaches will be presented in the following subsections.

It should be noted that a number of microsystems can be fabricated completely within the regular CMOS process sequence [8,9,35], for example, temperature sensors, magnetic field sensors (especially Hall sensors) and CMOS imaging sensors. Moreover, an additional set of CMOS-based microsystems only requires the modification of a CMOS layer or the deposition and patterning of additional films. Examples of these are various chemical sensors (e.g. palladium-gate and ion-selective FET (field effect transistor) structures and chemoresistors/capacitors [48,49], recording/stimulation of neural activity [50,51]), and a number of physical sensors (e.g. flux-gate sensors [52], fingerprint sensors [53], and force sensors [54]). However, these types of the microsystem count only a small portion of the MEMS market.

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2.4.2 Pre-CMOS micromachining

For the pre-CMOS approach, the microstructures are initially fabricated on the substrate, and then buried and sealed by dielectric layers. The wafer surface is planarised using a CMP process after the initial MEMS fabrication. Theoretically, the planarised wafer with prefabricated MEMS structures can serve as a starting material for any microelectronics foundry service, since the technology does not require significant modification of the CMOS fabrication [8, 9, 55]. However, there is a stringent criterion for the prefabricated MEMS wafers entering a foundry due to contamination and planarisation concerns.

The M^3EMS (Modular, Monolithic MicroElectroMechanical Systems) technology developed at Sandia National Laboratories was one of the first demonstrations of the pre-CMOS integration concept [11]. In this approach, a trench is etched into the bulk silicon substrate using an anisotropic wet etching process. The multi-layer polysilicon microstructure is then built in this trench, and refilled with LPCVD oxide and planarised with a CMP step. Subsequently, the wafers with embedded microstructures are used as starting material in an unmodified CMOS process, fabricating CMOS IC in areas adjacent to the MEMS areas. The CMOS metallisation is used to interconnect circuitry and MEMS devices. Additional processing steps are required to open the protective silicon nitride cap over the MEMS areas prior to the release of the polysilicon structures by etching an oxide sacrificial layer. One challenge of this approach is the fabrication of microstructures in an anisotropic etched trench, which may cause problems during the photoresist coating, exposuring and film deposition. Therefore, a relatively shallow trench has been used for fabricating microstructures, and the polysilicon (maximum 3 μm) used in this approach.

An alternative pre-CMOS approach called Mod-MEMS (Modular MEMS) has been demonstrated by Analog Devices Inc. and University of California, Berkeley [12], which enables the integration of thick (i.e. 5-10 μm) polysilicon MEMS devices with submicron CMOS IC. The schematic of the Mod-MEMS approach is shown in Fig. 2.9. For this approach, the thick polysilicon structures are built on top of the silicon substrate (not in an etched trench). After forming isolation trenches to provide electrical isolation between MEMS and CMOS regions, a capping oxide/nitride sandwich is deposited on the polysilicon, the MEMS structural regions are defined by a polysilicon etch step, and the sidewalls of the MEMS regions are passivated by a thermal oxidation. Next, a selective epitaxial silicon growth process is used to provide planarisation around the thick MEMS structures. With the polysilicon structures encapsulated

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with a silicon oxide layer, the epitaxial silicon layer grows only in the wafer regions surrounding the MEMS regions. After the selective epi-process, the wafer surface is then planarised with a CMP process. At this point, the wafers are ready for standard CMOS or BiCMOS processing. Similar to the M^3EMS process, the CMOS metallisation connects the polysilicon microstructures with the circuitry. After completion of the IC process, the MEMS areas are opened up, the thick polysilicon layer is structured with an anisotropic dry etching step and the microstructures are released by sacrificial oxide etching. Similar to the M^3EMS process, the Mod-MEMS process can be used in conjunction with various IC processes, as long as the starting material can be qualified for the particular IC foundry.
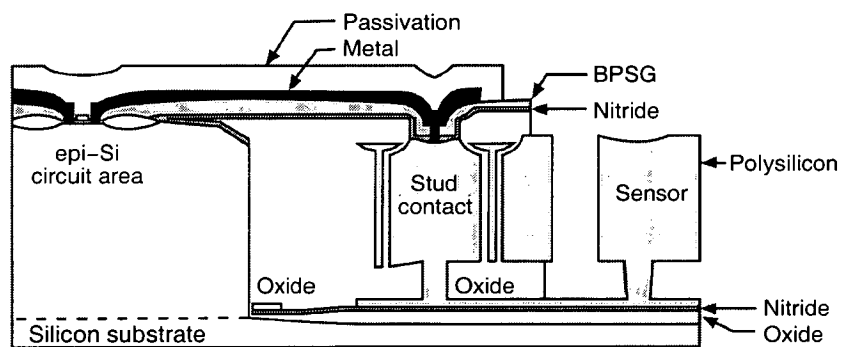
Figure 2.9: *Schematic cross-section of a pre-CMOS approach (Mod-MEMS) for fabricating polysilicon microstructures on the same substrate with a CMOS IC [12].*

The most important advantage of the pre-CMOS micromachining fabrication approach is that MEMS structures can be formed using high temperatures. This benefit is especially important for the fabrication of polysilicon microstructures, which require stress relief anneals at temperatures up to 1100 °C [9, 32]. On the other hand, properly designed MEMS structures, once fabricated, are not degraded by the thermal budget during CMOS processing. However, challenges for this approach include the surface planarisation, contamination control, and also the interconnections between the CMOS circuitry and MEMS devices.

2.4.3 Fully integrated micromachining

When the micromachining processes are appropriately integrated into the regular CMOS IC fabrication, the overall number of fabrication steps can be reduced, since some process steps can be performed for both IC devices and MEMS structures. It is well-known that microstructures often use polysilicon as a building material, requiring high temperature anneal to ensure low stress and small stress gradients. If the polysilicon annealing temperature can be limited to

around 900 °C with a very short processing time, which does not significantly affect the doping profiles of the fabricated CMOS devices, the additional MEMS fabrication steps can then be inserted before the back-end interconnect metallisation process of the CMOS IC fabrication [22, 23]. On occasion, higher anneal temperatures are required to achieve a low film stress for a thick structural polysilicon film, then the deposition and anneal of polysilicon has to be arranged in the early stage of the CMOS fabrication sequence [24].

Infineon Technologies, among others, has developed a fully integrated pressure sensor system by adding MEMS fabrication steps into a BiCMOS process [22], as shown in Fig. 2.10. In this approach, the basic pressure sensor structure is formed within the course of a 0.8 μm-BiCMOS process sequence, using a standard capacitor polysilicon deposition step to form the mechanical layer of the sensor. During the fabrication, the standard BiCMOS process sequence is stopped before the back-end interconnect metallisation to insert a single-mask micromachining module. For the sensor, the lower electrode is made from the n-well, whilst the field oxide (600 nm) serves as sacrificial layer and the capacitor polysilicon (400 nm) as structural layer and top electrode. Within the micromachining module, the polysilicon membranes are released by sacrificial layer etching using vapour HF (hydrofluoric acid), and the cavities are sealed with a cavity vacuum of 300 mbar. After completion of the micromachining module, the regular BiCMOS back-end process is employed to form the aluminium interconnects and passivate the microsystem. The final pad etch is used to open the contact pads and form the oxide block structures on the pressure sensors. It has been reported that the additional processing effort to integrate micromachined pressure sensors with the evaluation circuitry is merely 5% of the BiCMOS process [22].
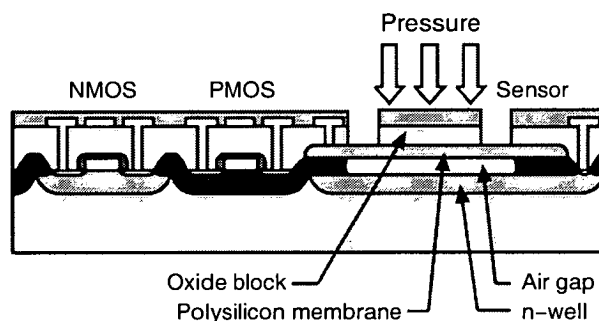
Figure 2.10: *Schematic cross-section of Infineon Technologies's integrated pressure sensors [22].*

For high volume and mature products, the fully integrated micromachining is the best integra-

tion approach because it enables the full utilisation of both CMOS and MEMS fabrication steps. Commercially successful examples using this approach include Analog Devices's accelerometers and gyroscopes [45], Infineon Technologies's pressure sensors [46] and Freescale's (Motorola) pressure sensors [47]. However, it should be noted that, in most of the cases, only surface micromachined MEMS devices can be fabricated using this approach; and also only big institutes and companies, which have both MEMS and CMOS fabrication facilities, have the capability to develop devices using this approach. Device development based on CMOS outsourcing will very likely be unable to use CMOS processes with intermediate MEMS processing steps, because a CMOS foundry will probably not accept wafers back into their line after a number of micromachining steps have been performed elsewhere.

2.4.4 Post-CMOS micromachining

The post-CMOS micromachining is an attractive and popular approach, as both MEMS and CMOS fabrication can be outsourced. Although there is a temperature limitation ($\leq 450\ °C$) for metal contained CMOS substrate, many MEMS fabrication processes, such as PECVD dielectric deposition, metal sputtering, electro-plating and most wet and dry bulk and surface etching processes are well suited for post-CMOS processing. The post-CMOS micromachining approaches can generally be categorised into two types, depending on the microstructures are formed: (1) by building the complete microstructures after the CMOS fabrication, or (2) by machining some of the regular CMOS layers. For the first approach, the MEMS devices can be placed adjacent to the CMOS or on the top of the CMOS circuits. The latter saves valuable CMOS wafer area. In the second approach, most of the microstructure can be formed within the regular CMOS fabrication. The post-CMOS process module typically requires a few low temperature processing steps, such as etching to release the microstructure or additional deposition steps for MEMS passivation.

2.4.4.1 Post-CMOS micromachining using add-on layers

For normal CMOS circuits with Al or Cu interconnect, the maximum post-CMOS processing temperature is limited to around 450 °C, so as not to degrade the interconnect [56, 57]. Several solutions have been developed to either potentially increase the CMOS post processing temperature by using doped-polysilicon or tungsten (W) as CMOS interconnect materials [16]; or using SiGe or Ge as MEMS building materials which require lower deposition and

anneal temperatures [17]. For some post-CMOS add-on microstructures, the required deposition temperatures are in the range of (1) 100-150 °C, being typically based on physical vapour deposition or electro-plated metal layers and use polymers or metals as sacrificial layers, and (2) 300-450 °C, often being based on chemical vapour deposition processes for the structural and the sacrificial layers.

The digital micromirror device (DMD) developed by Texas Instruments is a commercially successful example of adding a metal-based MEMS structure on top of a CMOS substrate [18]. The mechanical structure of a DMD pixel consists of movable layers of patterned aluminium with air gaps and is built on top of a CMOS static random-access memory (SRAM) cell using surface-micromachining techniques, as shown in Fig. 2.11. After completion of a 0.8 μm two-level-metal CMOS process, the final dielectric layer is planarised using CMP and vias are generated for interconnecting the mirror with the underlying circuitry. As can be imagined, the surface planarisation throughout the MEMS process is crucial, as non-uniformities in the mirror surface would result in intolerable contrast changes in the final picture. The formation of the 16 $\times$ 16 μm micromirror requires six additional photolithographic steps to define four aluminium layers and two sacrificial photoresist layers. The four aluminium layers are used for: (1) the yoke address electrodes and the bias/reset bus, (2) the torsional hinges, (3) the mirror address electrodes, yoke and hinge support posts, and (4) the mirror. The aluminium layers are sputter-deposited and the final micromirrors are released by etching the photoresist sacrificial layer in a plasma etcher. An antistiction coating is applied in the end of the fabrication to prevent stiction of the micromirrors to the landing pads during operation.

2.4.4.2 Post-CMOS micromachining using regular CMOS layers

For a number of MEMS devices, the required structural layers can be fabricated using the standard CMOS processing technology. As a result, the desired microstructures can then be patterned and released after the completion of the CMOS fabrication sequence. Both bulk or surface micromachining processes can be used for the post-CMOS fabrication. By far the majority of demonstrated devices are based on bulk micromachining processes, using both wet and dry, anisotropic and isotropic silicon etching techniques, and the developments have been focused on these etching techniques, etch-stop control, and the protection of the fabricated CMOS and MEMS during the lengthy etching processes [2, 35]. Recently, successful surface-micromachining approaches have also been demonstrated [20, 21].
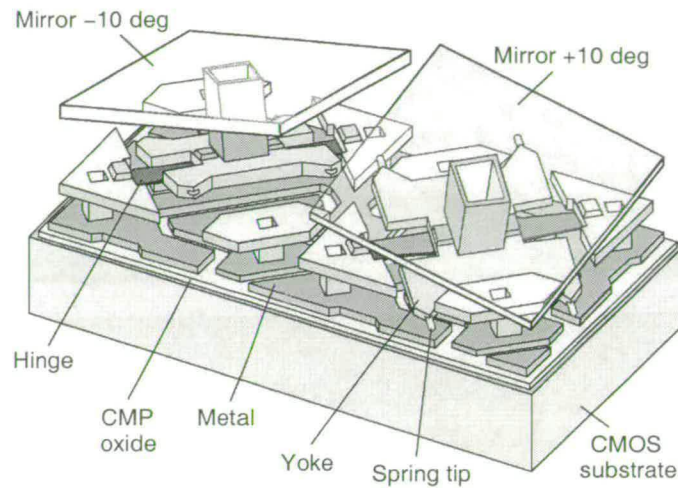
Figure 2.11: *Schematic of the digital micromirror devices developed by Texas Instruments [18].*

Fig. 2.12 shows a maskless post-CMOS micromachining technology, developed at Carnegie Mellon University, which uses dry etching steps to form the MEMS structure from the front side of CMOS wafers [20]. In this approach, the post-CMOS micromachining module uses the top metal interconnect layer as etch mask for the microstructure definition. In this way, the minimum feature sizes, such as minimum beam widths and gaps, are defined by the CMOS design rules and can be scaled with the CMOS technology. The actual laminated microstructures, consisting of the CMOS dielectrics with polysilicon and metal layers sandwiched in between, are released using two dry etching steps (see the schematic in Fig. 2.12(a)-(c)). The first anisotropic etch step uses CHF_3 (trifluoromethane) and O_2 (oxygen) etch chemistry, and the oxide areas not protected by the metal mask are etched to the desired depth. In the second isotropic etch step using SF_6 (sulphur hexafluoride) and O_2 chemistry, the polysilicon sacrificial layer is removed, releasing the microstructures. A SEM image of the processed device is shown in Fig. 2.12(d). This process technology has been used to fabricate integrated accelerometers [58], gyroscopes [59], IR (infrared) sensors [60] and acoustic devices [61].

Depending on the CMOS process, the released dielectric layer sandwich with embedded polysilicon and metallisation lines can be subject to large residual stress and stress gradients, which results in a significant curling of the released microstructures. To minimise the stress mismatch related curling, single-crystalline silicon has been used to replace the polysilicon, and the micromachining process has been combined with deep reactive-ion etching (DRIE) and an anisotropic etch step from the back side of the wafer [21].
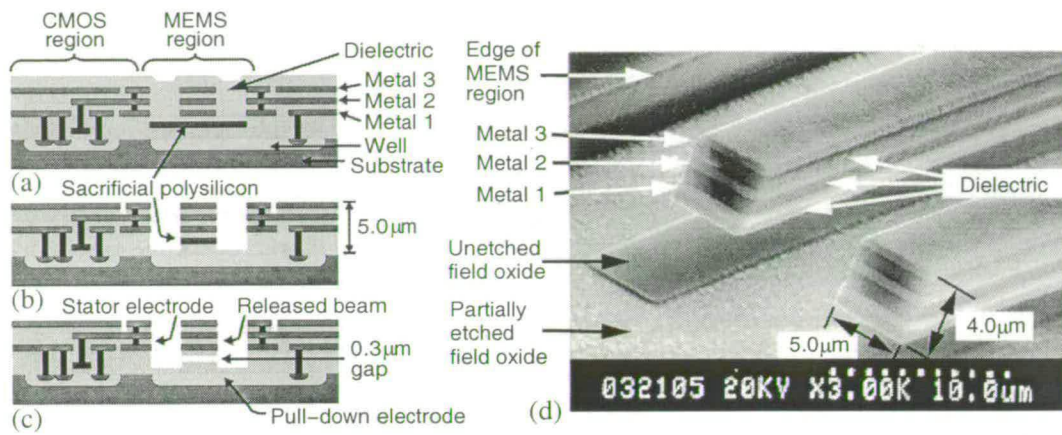
Figure 2.12: *A post-CMOS fabrication approach developed at Carnegie Mellon University [20]: (a) schematic cross-section of a MEMS structure after the CMOS fabrication, (b) after dielectric etch steps, (c) after polysilicon release etch, and (d) a SEM image of the released 3-metal laminated beams.*

2.4.5 Chip-level integration and multi-chip modules

Chip-to-chip (die-die) or chip-to-wafer (die-wafer) bonding has proved to be a viable option for the integration of dissimilar devices, for example, the integration of optoelectronic III-V components with silicon CMOS ICs [62, 63]. This approach is also used commercially for the CMOS-MEMS integration [25]. The main advantage of this approach is that it allows dissimilar devices to be fabricated on different sized wafers and with different chip sizes. As the size of the mainstream industrial CMOS wafers is in the range of 200-300 mm whilst the available MEMS wafers are from 100 mm to 200 mm, the full wafer bonding of different sized wafers is not a good option. Even if the size of the wafers is the same, the size of the individual CMOS and MEMS devices can be different, which implies that the full wafer bonding would result in an inefficient usage of the wafer area. In these situations, chip-level integration is the preferred technology. However, chip-level integration has difficulties with the interconnect process, especially when high density contacts are required. It is not a batch-fabrication process, and also presents problems when additional processing steps (e.g. photolithography or etch) are required after the bonding.

The multi-chip module is a standard approach for assembling more than two ICs and other components, for example, chip capacitors integrated into an electronic module [25, 64]. Being such a readily available technology, this has a low entry barrier and can be used for many applications. Many manufacturing companies such as Bosch, Freescale (Motorola) and SensorNor,

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use this approach with many of their MEMS based systems.

2.5   Conclusions

The similarities between the CMOS and MEMS technologies have enabled integrated CMOS-MEMS systems to be fabricated on the same substrate. Despite of the inherent differences between them and some incompatibilities in fabrication technologies, a large number of process technologies for the integration of MEMS with CMOS circuitry has been demonstrated over the past 20 years. Whilst some of CMOS-based microsystems require the insertion of dedicated micromachining modules in between the regular CMOS process steps (hybridisation), the majority of the demonstrated approaches tend not to interrupt the regular CMOS fabrication sequence. This has been achieved by adding the required MEMS process modules, either before (pre-CMOS) or after (post-CMOS) the CMOS process steps. From the manufacturing point of view, the post-CMOS approach is especially appealing, since both the CMOS process and MEMS modules can be completely outsourced in dedicated CMOS and MEMS foundries. This allows small and medium sized MEMS companies, without in-house fabrication capability, to design and produce CMOS-based MEMS.

Chapter 3
Chemical Mechanical Polishing

3.1 Introduction

The chemical mechanical polishing process has been used to achieve local as well as global pla-narisation across the entire wafer by preferential removal of protruding material on the wafer surface through a combination of mechanical and chemical action. It is a fairly mature technol-ogy which has been widely used in the semiconductor industry for more than a decade, and has become an indispensable process module for 0.18 μm and below technologies [65–68]. CMP is also an enabling technology and has been used in MEMS for building various new devices and structures [68]. An overview of the CMP process is presented in this chapter.

3.2 Introduction of the CMP process

In the CMP process [65,67,68], the wafer is fixed to a wafer carrier via a vacuum, and pressed face-down onto a polishing table which is covered with a pad, as illustrated in Fig. 1. The wafer carrier and polishing table rotate at variable speeds (typically in the order of tens of revolutions per minute), and a pressure between the wafer and polishing pad (also termed as down force, typically in the order of 0.1 - 1.0 bar) is applied by the polishing tool. A slurry, which consists of abrasive particles and appropriate chemistry, is dripped onto the rotating polishing table and distributed to the interface between the wafer surface and the polishing pad.

The CMP process takes place when the wafer surface is moving across the pad, under pres-sure, in the presence of a slurry. At the microscale, the polymeric pad surface provides the rough points, or asperities, which make contact with the wafer. The pad is also used for trans-porting slurry, removing the reacted products, and uniformly distributing the applied pressure across the wafer. The slurry provides the chemical solution and suspended abrasive particles for the CMP process to proceed. During the polishing process, the chemical agents in the slurry weaken or react with the surface film, while the abrasive particles mechanically interact with
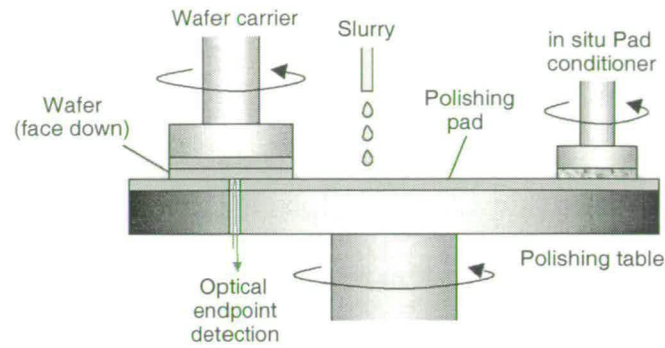
Figure 3.1: *Configuration of a typical chemical mechanical polishing tool [67].*

the chemically modified surface layers, resulting in material removal. A schematic illustration of the typical operating regimes in the CMP process is shown in Fig. 3.2 [69].

(a)   (b)
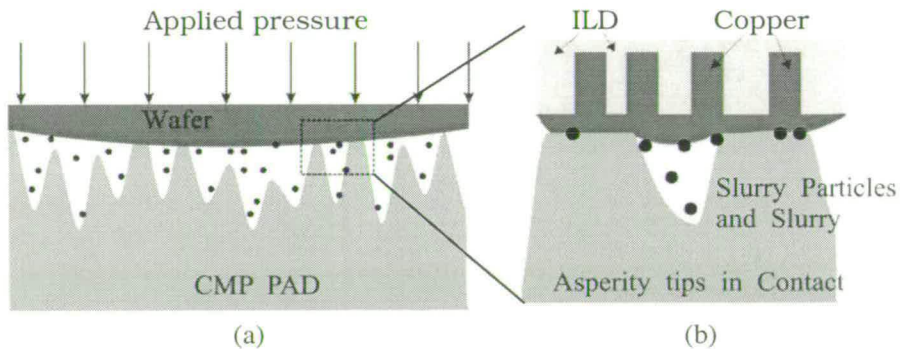
Figure 3.2: *A schematic illustration of the typical operating regimes in the CMP process [69]: (a) wafer-scale and (b) IC device feature size scale.*

The CMP process is a complex process which has a large number of control variables (> 20) detailed in Table 3.1 that need to be optimised [67, 68] to achieve a desirable result. The input control factors include slurry parameters (such as abrasive particles and chemicals), pad parameters (mechanical properties and topography), tool parameters (down pressure and linear velocity), and substrate parameters (pattern density and feature size). In addition, the time-dependent nature of some of these parameters (e.g. pad conditions and wafer surface topography) cause further complexities in the process.

The important output parameters for the CMP process are: (1) film removal rate, (2) uniformity (removal rate across the wafer and between wafers), (3) planarisation (surface topography after the removal process), (4) surface finish (the number and size of the defects on the polished surface), (5) selectivity (when several materials are present on the polishing surface), and (6)

Input variables	Microscale parameters	Nanoscale interactions	Output parameters
Machine parameters Down force Linear velocity Slurry flow	**Pad** Contact area Pressure on pad **Particle on pad** Pressure Coverage **Chemical concentration and distribution** **Contact mode** Direct Hydroplaning Mixed	**Chemomechanical** Dynamics of surface layer formation Thickness Uniformity Formation rate Layer removal Abrasion frequency **Chemical and mechanical** Etching Mechanical removal	**Removal rate** **Planarisation** **Selectivity** **Uniformity** **Surface finish** **Dishing and erosion resistance**
Slurry chemistry Oxidisers pH and pH drifts pH stabilisers Complexing agents Dispersants Concentration			
Slurry abrasive particles Size Size distribution Shape Mechanical properties Chemistry Concentration Agglomeration			
Pad characteristic Mechanical properties Topography Conditioning			
Substrate characteristic Feature size Feature density			

Table 3.1: *Correlation of input variables with micro- and nanoscale effects and output parameters in the chemical mechanical polishing process, adapted from [67,68].*

dishing and erosion resistance.

3.3 Fundamentals of the CMP process

3.3.1 Removal rate modelling

The effect of the applied downward pressure (P) and linear relative wafer-pad velocity (v) on the CMP removal rate (R) is represented by Preston's empirical equation [70],

$$R = K_p P v \qquad (3.1)$$

where K_p is a proportionality constant (also known as the Preston coefficient), and has units of $(\text{pressure})^{-1}$. It should be noted that the mechanical abrasion and chemical effects are all lumped into the K_p in Preston's equation. Therefore, K_p is determined by the mechanical properties of the polishing surface material (hardness and Young's modulus), the polishing slurry, and the polishing pad [27, 67]. It also worth noting that the Preston's equation was derived from glass polishing [70], but it is a good approximation for other polishing processes and is also a good guideline for the design of polishing tools. According to the Preston's equation, to achieve an uniform polishing rate across the wafer, it is desirable for all points on the wafer surface to experience the same velocities and pressure, as well as the same pad surface condition and slurry properties throughout the polishing cycle.

The relationship between the sliding velocity of the wafer across the pad ($\mathbf{v}$) and the angular velocities of the polishing table (ω_t) and wafer carrier (ω_c) is obtained from the polisher geometry shown schematically in Fig. 3.3 [71]. P is an arbitrary point fixed on the wafer carrier, and the length between carrier centre and P ($\mathbf{r}_c$) is a constant but its direction varies as the wafer carrier rotates. $\mathbf{r}_{cc}$ is determined by the setup of the polisher, and $\mathbf{r}_t$ varies in both direction and length as the wafer carrier rotates. These three position vectors are related as follow,

$$\mathbf{r}_t = \mathbf{r}_{cc} + \mathbf{r}_c \qquad (3.2)$$
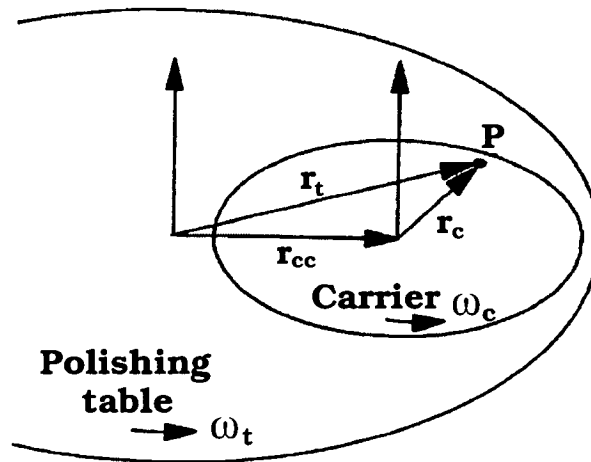
Figure 3.3: *Schematic diagram illustrating the geometry of the polisher [71]. The $\mathbf{r}$'s are position vectors whilst the ω's are the rotational velocity vectors.*

The velocity of P across the pad ($\mathbf{v}$) depends on the rotational velocities of the polishing table

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and wafer carrier (ω_t and ω_c),

$$\mathbf{v} = -(\omega_t \times \mathbf{r}_t) + (\omega_c \times \mathbf{r}_c) \tag{3.3}$$

The negative sign in the first cross product is used since the velocity of P across the polishing table is opposite in direction to velocity of the polishing table to the point P. Combining equations (3.2) and (3.3) leads to

$$\mathbf{v} = -(\omega_t \times \mathbf{r}_{cc}) - [\mathbf{r}_c \times (\omega_c - \omega_t)] \tag{3.4}$$

The second term on the right side of equation (3.4) is zero if ω_t equals ω_c. Since P is arbitrarily chosen, every point on the wafer carrier travels with the same linear speed across the pad if the rotation of wafer carrier is matched to the rotation speed and direction of the polishing table. The resulting relative velocity depends only on the angular velocity of the polishing table and the centre to centre distance of the polishing table and wafer carrier.

In practice, however, the wafer carrier is typically oscillated around its central position at the half radius of the polishing table to utilise more pad area and reduce pad wear, and also to facilitate the distribution of the slurry. This oscillation causes an extra small varying velocity to be added on the constant pad and wafer relative velocity. Various techniques are employed to minimise this effect on the non-uniformity to the wafer-pad relative velocity [27,67].

Another important requirement for the uniform polishing is the even distribution of the polishing slurry under the wafer. Although the grooves on the pad surface are often employed to facilitate slurry distribution, slurry transport is mostly through the surface of the pad where the edge of the wafer gets the more abundant supply of the slurry than the centre of the wafer. Therefore, the edge of the wafer has a polishing rate higher than the centre from the slurry supply aspect. To compensate for this, some equipment uses a slightly convex curvature on the carrier to exert a higher pressure in the centre of the wafer [27,66].

3.3.2 Mechanism of oxide and metal CMP

The CMP process is achieved by the combined interactions of the chemical reaction and mechanical abrasion at the pad-slurry-wafer interface. The involvement of both chemical and mechanical effects can be elaborated more clearly through the discussions of the oxide and

metal CMP processes.

3.3.2.1 Oxide CMP process

For the oxide CMP, the most commonly used abrasive particle is silica with a size of $\sim$ 10 to 90 nm, and the pH value of the slurry solution varies from 1 to 11 [27, 65, 67, 72, 73]. The basic events occurring during an oxide CMP are illustrated in Fig. 3.4. With the presence of the water in slurry solution, the siloxane bonds (Si-O-Si) on both the surfaces of slurry particle and oxide film react with water molecules, which result in Si-OH groups,

$$SiO_2 + 2H_2O \longleftrightarrow Si(OH)_4 \tag{3.5}$$
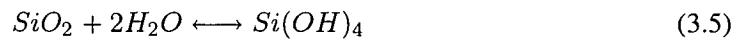
This reaction is also called as hydroxylation and it is reversible. The hydrogen bond is formed between the wafer surface and the slurry abrasive through the -OH groups (Fig 3.4(a)). The weak hydrogen bond may later turn into stronger covalent bond by form a Si-O-Si structure between abrasive particle and the oxide surface, meanwhile release a water molecule (Fig 3.4(b)),

$$Si - OH + OH - Si \longrightarrow Si - O - Si + H_2O \tag{3.6}$$
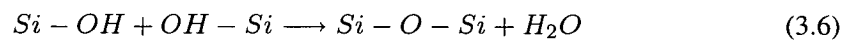
A surface silicon atom is removed when the abrasive particle is brushed away, as shown in Fig. 3.4(c), and the accumulated removal of surface atoms results in the surface layer being polished.

(a)   (b)   (c)
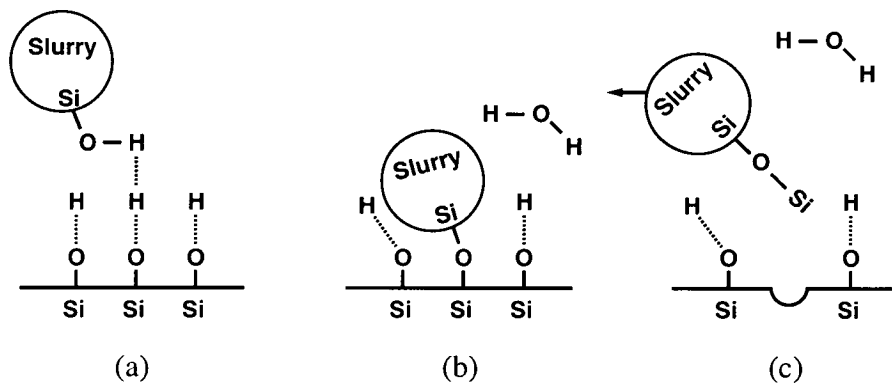
Figure 3.4: *Mechanism of the oxide CMP process [27]: (a) hydrolysis of the oxide surface and slurry abrasive particles in slurry solution, formation of a weak hydrogen bond between the abrasive particle and the oxide surface, (b) formation of a stronger Si-O-Si bond by release a water molecule, and (c) removal of a silicon atom when slurry particle moves away.*

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The oxide polishing process has clearly suggested that CMP, which relies on both the chemical and mechanical actions rather than mechanical abrasion alone, avoids a mechanically damaged surface after the CMP. The mechanical abrasion of the particle removes more material on the high regions of the wafer surface than those for the low regions, which results the planarisation. However, the chemical reaction will remove the high and low regions at the same rate. The chemical nature of bonds formation, the presence of the water and chemistries in the slurry solution has a large effect on the polishing process [65, 66]. It should also be noted that a decreased hardness of the oxide surface has been observed, due to the diffusion of water into the oxide film, which increases the oxide polishing rate [65].

3.3.2.2 Metal CMP process

Metal is readily oxidised in atmosphere conditions and typically possesses a passivation layer (e.g. Al_2O_3 for Al) on the surface. Metal CMP is different from oxide polishing. Kaufman et al. [74] initially proposed that the metal polishing may involve three steps (Fig. 3.5): (1) the passivation layer is removed by the mechanism similar to that for the oxide polishing, which includes hydroxylation, bonds formation between slurry particles and wafer surface and the removal of the wafer surface atoms; (2) once the passivation layer is removed, the metal is etched by the chemicals in the slurry solution; and (3) the exposed metal forms a new passivation layer through oxidation by the solution. In reality, the three steps, the removal of passivation layer, metal etching, and re-passivation, occur simultaneously and the polishing rate is determined by the balance of these processes. Therefore, for metal CMP the polishing slurry must contain all three components: the fine slurry particles, an etching (or corrosion) agent, and an oxidant [27, 65, 66].

Nowadays, it is still believed that the metal polishing proceeds through the repeated processes of passivation layer formation, film abrasion, and re-passivation in the slurry. However, whether there is a step when the metal is fully exposed for chemical etching is not clear [74–78]. It is suspected that the existence of fully exposed metal surface during the CMP largely depends on the selection of the slurry chemicals, abrasive particles and the polishing conditions.

Metal dishing and insulator erosion commonly occur during the metal CMP, which result in a reduced metal line thickness and a degraded planar surface [27, 65–67]. Dishing and erosion normally occur during the over-polish step, a step required to ensure complete metal removal across the entire wafer, and highly depends on the wafer pattern, polishing parameters and the
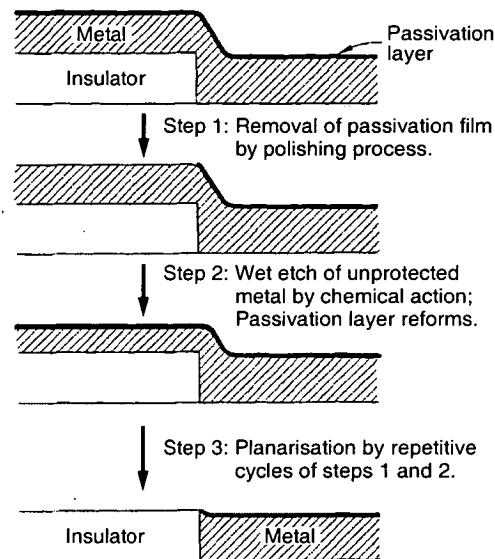
Figure 3.5: *Mechanism of the metal CMP process [74].*

polishing pads. Process optimisation to reduce dishing and erosion will be discussed in later chapters.

3.4 CMP consumables

The CMP consumables consist of polishing pads and slurries, and play important roles in the CMP process.

3.4.1 Polishing pads

The polishing pad plays a crucial role in the CMP process by carrying and distributing slurry, executing the polishing action, and transmitting the normal and shear forces for polishing [66, 67, 79–81]. Since polishing is both a mechanical and a chemical process, the polymeric polishing pad must have sufficient mechanical and chemical resistances to survive the extreme polishing conditions. Important mechanical properties include an appropriate hardness and Young's modulus, high strength to resist tearing, and good abrasion resistance to prevent excessive pad wear during the polishing. Chemically, the pad must be able to survive the aggressive slurry chemistries without degrading, delaminating, blistering or warping. Another important criterion is that the polishing pad must be sufficiently hydrophilic. The aqueous-based slurry

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must wet the surface of the pad and form a liquid layer between the wafer and the pad. If the liquid does not wet but instead beads on the pad surface, it will be swept away by the wafer edge, and this results in a lack of necessary chemistry at the interior of the wafer.

The polishing pads are typically made of polyurethane with many asperities ($\sim$ 1-10 μm in size) on the surface to help hold and transport the slurry, as shown in Fig. 3.6. However, the surface properties of the polishing pad change during the process. After polishing a number of wafers, the surface asperities are flattened, resulting in a state called glazing, shown in Fig. 3.7. When a pad is glazed, it loses some of its capacity to hold polishing slurry, and increases the contact area, which causes a drop in pressure. Both changes reduce the polishing rate. Fortunately, a pad conditioning process can be used to regain the original state of the pad surface. The pad conditioning is performed by placing a diamond-tipped wheel on the pad with some pressure for 1-2 minutes while the polishing pad and the wheel are all rotating. Although it may shorten the lifetime of the pad, the net effect of the pad conditioning is to provide a consistent polishing rate.
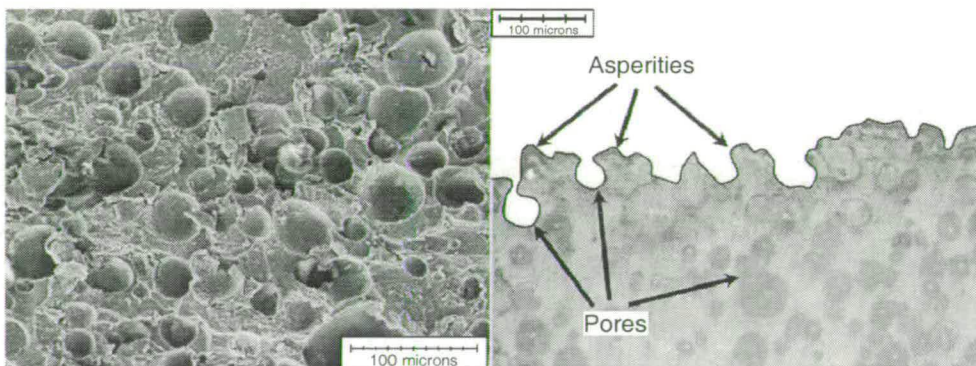
Figure 3.6: *(a) SEM image of the surface of a polishing pad before polishing, and (b) a cross-section image of pad surface (both images are taken from the same pad) [80].*

3.4.2 CMP slurries

The CMP slurry typically consists of abrasive particles in a chemical solution, and the CMP process is greatly influenced by this slurry composition. The important slurry parameters are pH and the chemistry of the solution, concentration, size and charge type of abrasive particles, complexing agents, oxidisers, buffering agents, surfactants, and corrosion inhibitors [27, 66, 67]. An ideal CMP slurry should be able to achieve high removal rate, excellent global planarisation, should prevent corrosion (in case of metal polishing), low surface roughness, low defectivity
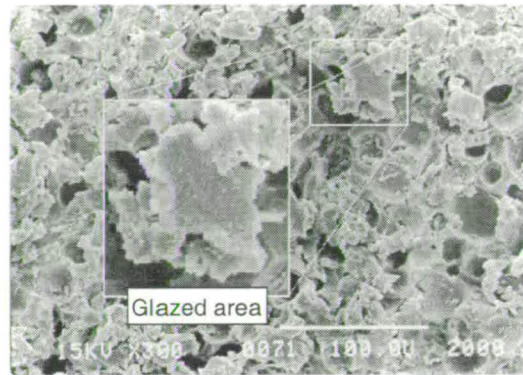
Figure 3.7: *SEM image of a polishing pad with glazed areas [81].*

and high selectivity.

The abrasive particle impacts the surface film and abrades the chemically reacted surface in the CMP process [66, 67]. To provide proper mechanical effects in the polishing process, the abrasive particles should have the correct surface charge to stay suspended in the solution, the correct hardness to impact the wafer surface, the correct chemical properties to not dissolve in the solution and, the correct chemical bonds to adhere to the wafer surface.

The water based solution also plays several important roles during the CMP process, such as providing proper chemical agents that attack the surface to be polished, and an electrostatic or steric balance that stabilises the abrasive suspension. The solution is also used as a lubricant between wafer and pad, transporting waste material, and controlling the polishing temperature. It is worth noting that the matching between slurry and pad is important for the CMP process because the pad is the primary means of the transporting slurry to the wafer surface, and the pad also acts as the reaction chamber during the CMP process.

3.5 Post-CMP clean technology

CMP was generally considered as a "dirty" wet process because of the presence of (1) nanometer abrasive particles in the CMP slurry, and (2) abrasive particles, dielectric and metallic particles and polymeric pad debris on the polished wafer surface. These particles, which are vast in number and may be difficult to completely remove after the polishing process, will not only prevent devices on the polished wafer from functioning properly, but also contaminate the whole cleanroom. Therefore, the post-CMP cleaning process is a critical step to ensure contamination-

free wafers out of the CMP station for further processing.

To remove particles, the van der Waals forces must be overcome to separate the particle from the substrate using mechanical effects such as scrubbing and/or chemical etching the particle [65,67]. Then the electrostatic interaction must be adjusted into favourable conditions to avoid dislodged particles from redepositing on the wafer surface. This can be realised by increasing the repulsion forces between the particles and surfaces through a change of the solution's zeta-potential [67]. Moreover, it is necessary to clean the wafers when they are still wet, immediately after the polishing process, because the dried and adhered particles have proved very difficult to remove [65,67].

The common practical techniques for the post-CMP clean are: brush scrubbing, chemical wet etching, hydrodynamic jets combined with spin-rinse drying, and megasonic acoustic cleaning [67]. The brush scrubbing technique in conjunction with chemical etching is widely employed in the industry nowadays [67, 82]. In this method, the mechanical force for the particle removal is provided by the brush bristles, which use hydrodynamic drag to exert a force on the surface particles. Deionized (DI) water mixed with specific cleaning solutions are typically used to generate electrostatic forces between the wafer surface and the dislodged particles to prevent the redeposition of those particles. The brushes are typically made of polyvinyl alcohol (PVA) material, the texture of which is soft when wet and effective for the particle removal. The brushes are used on single or both sides of the silicon wafer to scrub the surface thereby obtaining a contamination-free wafer, as shown in Fig. 3.8.
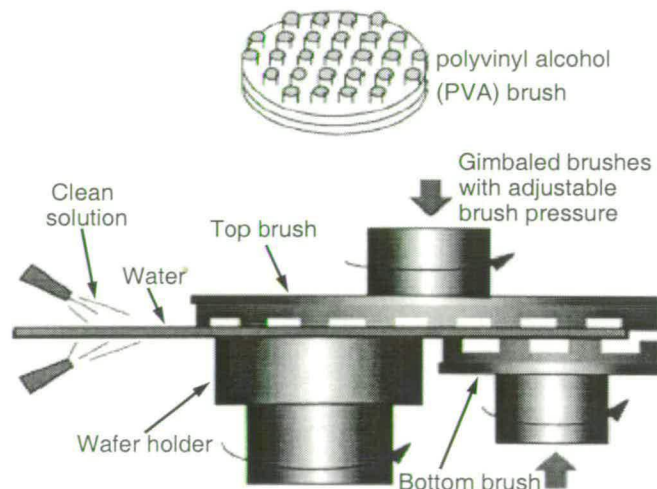
Figure 3.8: *Schematic of double sided brush scrubbing unit [67, 82].*

3.6 CMP for integrated circuits fabrication

3.6.1 Integration of CMP into IC fabrication

The CMP slurries and polished wafers contain various particle contaminants, and the post-CMP cleaning steps used to be problematic. In addition, the CMP process is typically more expensive, and relatively more difficult to develop and maintain. In history, it was the requirement for fabricating multi-level interconnection structures, which forced IC industry to adopt CMP in its fabrication sequence. As the integrated circuits became more complex, more levels of metal layers were required which resulted in several processing difficulties [27, 83], as illustrated in Fig. 3.9(a). The irregular non-planar surface topography causes difficulties with conformal deposition of the thin films and coating of photoresist (A in Fig. 3.9(a)). The accumulated step height (B in Fig. 3.9(a)) causes a problem with lithography pattern transfer due to the depth of focus issue. In addition, undesirable stringers (C in Fig. 3.9(a)) are also generated during the etch process which might result in unintentional metal shorts. Moreover the non-uniformity of the metal layer thickness and contact resistance are all potential problems for low fabrication yield and long-term reliability issues. These challenges can all be solved by the CMP enabled planarisation process which has theoretically removed the limitation of stacking more metal layers. A 6-level metallisation process using Cu and low-κ dielectric is shown in Fig. 3.10(b) which demonstrates the advantages of the CMP enabled surface planarisation.

(a)   (b)
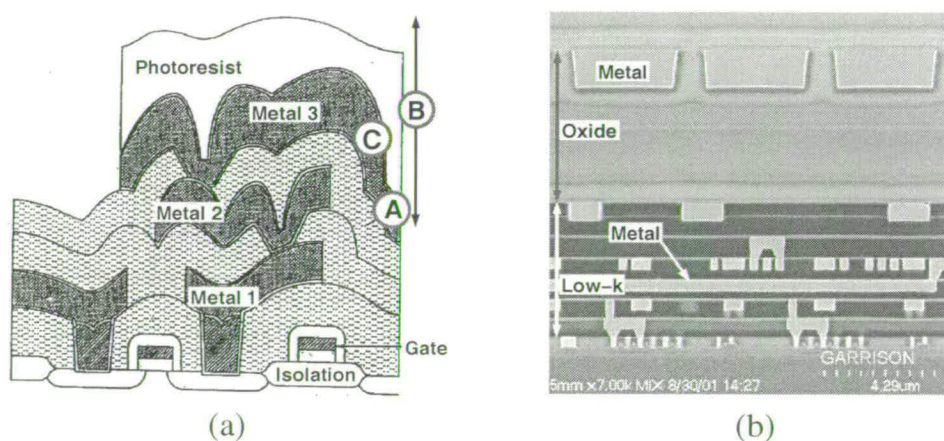
Figure 3.9: *Multi-level metallisation technology (a) without [83] and (b) with [84] planarisation process.*

Other benefits can also be obtained from the adoption of CMP in the IC fabrication process. For example, difficulties in dry etching of Cu can not be solved by wet etching because the undercut

problem is fatal for small device feature size. Fortunately, this can be solved by a damascene process.

3.6.2 Application of CMP in IC fabrication

The CMP process has been mainly used in the semiconductor IC industry and has been used to achieve the following [83]: (1) smooth wafer surfaces for the preparation of wafer substrates (Fig. 3.9(a)), (2) surface planarisation for the fabrication of multi-level interconnection structures (Fig. 3.9(b)), and (3) an alternative to the etch process to eliminate the difficulties of dry etching materials (such as Cu) or to simplify the fabrication process (Fig. 3.9(c)).
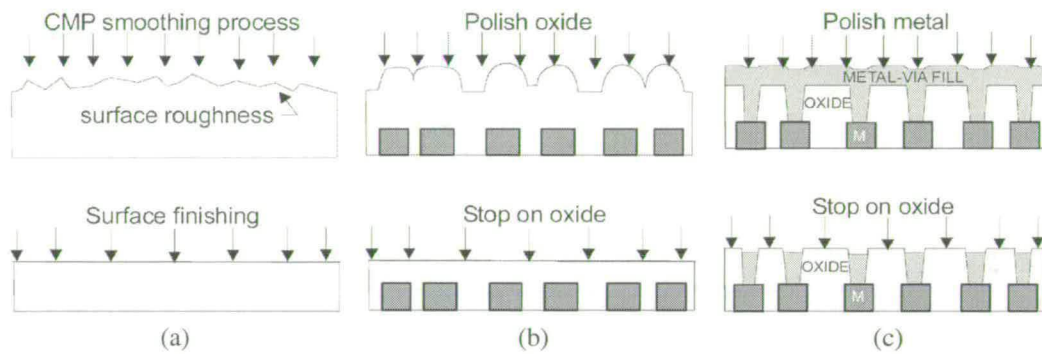
Figure 3.10: *Basic applications of the CMP process [83]: (a) smooth surface preparation, (b) surface planarisation, and (c) damascene process.*

In the backend of the line (BEOL) IC fabrication, CMP has been used to planarise PECVD oxide inter-level dielectric (ILD) and to remove excessive tungsten (W) after the plug filling in the Al interconnection technology. In the more advanced Cu interconnection technology, the vias and wiring are filled in one step and the excess Cu is removed by CMP. To further reduce capacitive losses from the ILD layer, oxide can be replaced by low-κ materials, such as fluorine doped oxide and polymer based materials [85]. In frontend of the line (FEOL) processing, CMP is used to realise shallow trench isolation (STI), to planarise trench capacitors in dynamic random access memories (DRAM) and in novel metal gate fabrication [85, 86]. It should be noted that CMP has also been used in the manufacturing of all types of semiconductor substrates, for example, Si, SiGe, SiC, GaN and silicon-on-insulator (SOI) wafers [85].

3.7 MEMS fabrication using CMP

In MEMS, CMP is an enabling technology which makes the fabrication of new devices and structures possible. In a similar manner to IC fabrication, CMP can be used to achieve the following three main functions: (1) surface planarisation, (2) roughness reduction, and (3) an alternative to etching. The purpose of planarisation process in MEMS is to make planar MEMS devices with better device performance [41], and to build more complex multi-level MEMS structures [41,42,87,88]. In addition to providing planar surfaces, CMP makes wafer bonding applications on various materials possible by reducing the roughness of the bonding surface [89–95], and it also makes subsequent processes possible after wafer thinning using grinding, wet etching or dry etching [96,97]. Like the damascene process used in IC fabrication, CMP can be used in MEMS as an alternative to etching, with the capability of removing more materials [98–101] and allowing the formation of new structures [102–110].

3.7.1 Surface planarisation

CMP based surface planarisation techniques can not only alleviate processing problems associated with the fabrication of multi-level structures and eliminate design constraints linked with non-planar topography, but also enable greater flexibility and complexity for MEMS design and fabrication. CMP is used to eliminate process issues generated by severe topography, and also to simplify the design and fabrication sequences by eliminating several photolithographic steps. Sandia National Laboratories [41,42] has developed a multi-layer polycrystalline silicon surface micro machining technology (SUMMiT^{TM}) by using ultra low-stress-poly deposition and CMP processes. Using this technology, devices and systems for a wide variety of applications, such as gears and transmissions, indexing motors, micro-engines [87] and optical mirrors [88] have been successfully designed and fabricated.

A planar MEMS device fabricated using CMP (Fig 3.11 (b)) shows marked improvement in performance when contrasted against a similar, non-planar device shown in Fig 3.11 (a) [41]. The CMP planarisation process has overwhelming advantages when fabricating complex and planar structures and devices.
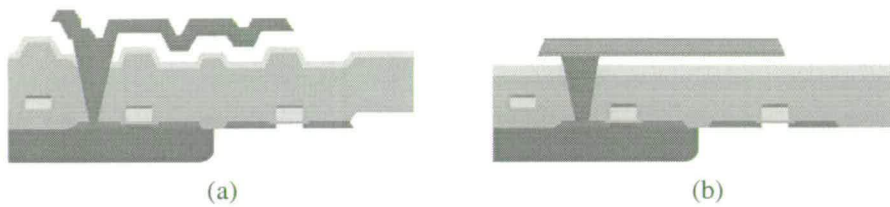
Figure 3.11: *MEMS cantilever fabricated (a) without CMP process, and (b) with CMP process [41].*

3.7.2 Surface roughness reduction

CMP can reduce the surface roughness resulting from the deposition of polysilicon or PECVD oxide layers, therefore, making wafer bonding on these materials possible [89, 91–93]. In general, surface roughness will be in the range of several nanometers after the deposition of a 1.0 μm polysilicon or PECVD oxide layers. This surface roughness increases with the film thickness increasing. The requirement for successful wafer bonding is a surface roughness of approximately half nanometer which can only be achieved by the CMP process.

After wafer thinning using grinding, wet etching or dry etching, the surfaces of processed wafers are typically very rough (Ra: $\sim 1\mu$m). CMP can be used to remove this roughness and to make subsequent processes on this surface possible [96, 97].

3.7.3 Etching alternative

To eliminate the difficulties of dry etching materials, CMP can be used as an alternative process to help pattern the desired MEMS structures. Examples are NiFe and SU-8 formed magnetic sensors [98], SiC micro motors [99], Au and polyimide formed photodiodes [100, 101], etc. These new processes are based on the damascene process which is widely used in IC fabrication, but obviously for a wider variety of materials.

Novel structures can be fabricated by the use of CMP process which otherwise cannot be built by conventional technologies. Examples are high density through wafer interconnections [107–110] and sub-micron trenches fabricated without the use of sub-micron lithography equipment [103, 104]. The fabrication flow and SEM pictures of the later structure are shown in Fig 3.12. The small geometry trenches are achieved via thermal oxide thickness control rather than by lithography and etch. It is relatively simple and easy to form uniform trenches with dimension less than one micron by this method, and it also has the potential to form trenches far smaller
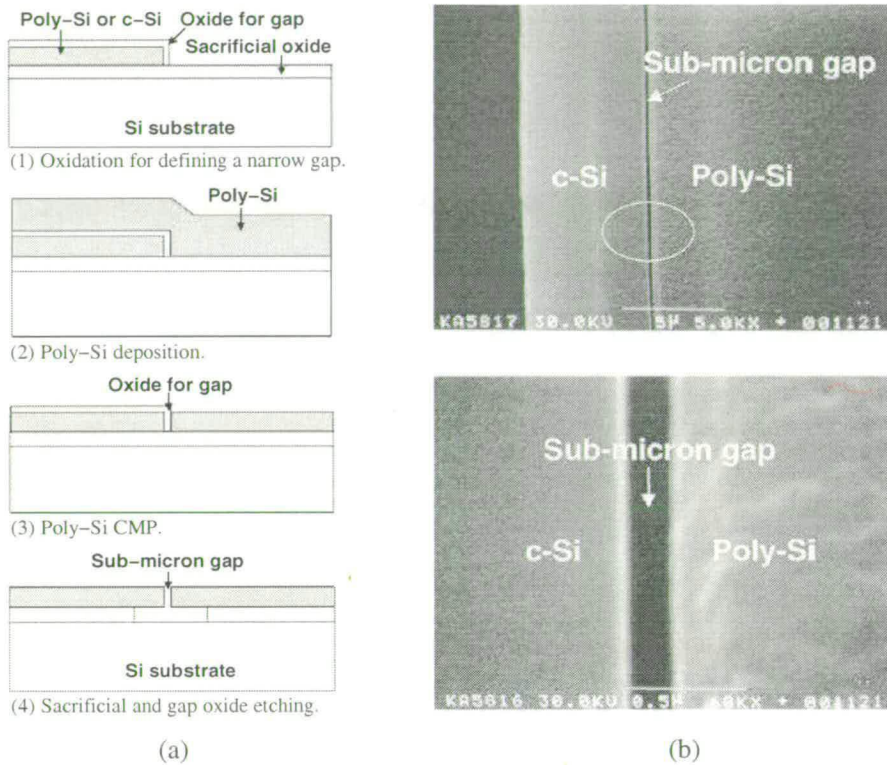
Figure 3.12: *Fabrication of sub-micron trenches using thermal oxidation and CMP [104]: (a) fabrication procedures, and (b) fabricated narrow gap (c-Si refers to single-crystal silicon).*

than the highest resolution of the most advanced lithography equipment.

3.8 Conclusions

In summary, there are three main reasons of using CMP in both CMOS and MEMS applications: (1) surface planarisation, (2) roughness reduction, and (3) an alternative to etching. The evolution of the dry-in and dry-out CMP equipment platform has been the key to the introduction of the CMP into the mainstream fabrication technologies. In semiconductor IC fabrication, CMP is not only used in the backend of the line interconnection process (such as ILD oxide, low κ and Cu), but is also used for critical process steps in the fabrication of the transistors and other key devices elements (such as shallow trench isolation and trench capacitors for DRAM), where control of contamination is crucial for the yield of the device fabrication. As the growth of IC fabrication based on silicon technology is fast approaching the fundamental limits, new technologies that incorporate novel materials and structures onto silicon may become the driv-

ing force to maintain Moore's Law. CMP is expected to play a key role in these next generation micro- and nano-fabrication technologies.

With continuing progress being made in MEMS technology, complex devices and systems with multi-level structures, small geometry structures and ultra smooth optical surfaces which cannot be fabricated without the use of CMP, will be more frequently required in the MEMS applications. It is also predicted that CMP will become more prevalent as a MEMS technology in the future.

Chapter 4
Wafer Bonding Technology

4.1 Introduction

Wafer bonding involves joining two wafers to form a new entity and covers a wide range of techniques. The resulting wafer pairs and structures can be used for many applications. Modern wafer bonding techniques can be generally categorised as wafer direct bonding, anodic bonding and bonding with an intermediate layer [33, 111–114].

This chapter introduces wafer bonding technology. The mechanisms, procedures and requirements of each bonding technique are presented with the emphasis on new developments. Bonding quality evaluation methods and some important applications are also presented.

4.2 Wafer direct bonding

4.2.1 Bonding procedure

When two atomically smooth, flat and clean surfaces are brought into intimate contact at room temperature, they bond to each other spontaneously through weak intermolecular forces such as van der Waals forces or hydrogen bonds [111, 112]. The bonding is typically carried out in air either manually or by using a commercial bonder directly after the cleaning process. Before contact, the wafers usually float on each other due to a thin air cushion between them. By locally pressing them at one point so as to squeeze out the air, bonding is initiated and propagates by itself. Within a few seconds the bonded area spreads over the entire wafer surface, and the two wafers are completely bonded, as illustrated by the infrared transmission images in Fig. 4.1. At this stage the bonding is still reversible, and the wafers can be separated without damage. Bonding strength can then be increased up to the cohesive strength of the bulk materials by an elevated temperature annealing.
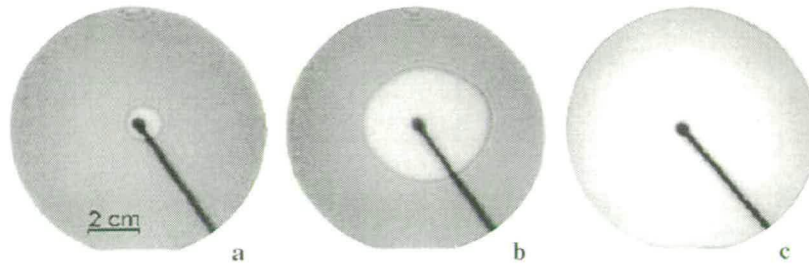
Figure 4.1: *Infrared transmission images of the initiation and propagation of the bonded area during the wafer bonding process [111, 112].*

4.2.2 Requirements for wafer direct bonding

In order to bond two wafers successfully, substrate selection and wafer surface preparation have to be performed to meet the following specifications.

4.2.2.1 Substrate material

Wafer direct bonding is a versatile joining method which can be applied to a large number of materials. However, it does require a flat, smooth and clean surface for the initial contact, which is followed by a thermal treatment for increasing the bonding strength. Therefore, for every new material to be bonded, a surface preparation technique, which includes polishing and cleaning, has to be developed to achieve a surface roughness of less than 0.5 nm. In many cases the bonded pair requires a heat treatment at elevated temperatures to increase the bonding strength. The thermal expansion coefficient of dissimilar materials needs to be considered. It is important that they match reasonably to avoid possible thermally induced strain after the bonding process. Furthermore, the crystal structure and crystal orientation of two bonding surfaces also need to be considered to avoid possible lattice mismatch. Besides silicon, silicon dioxide, quartz and glass wafer bonding, successful bonding of other materials has been achieved, such as III-V compound semiconductors (GaAs and AlGaAs), sapphire and silicon carbide [111, 112, 115].

4.2.2.2 Surface cleaning

Wafer bonding requires surfaces free of contaminants. The contaminations can be classified as (1) particle contamination, such as dust or fibres, (2) organic contamination, such as hydrocarbons from the air or plastics from wafer boxes and (3) ionic contamination, such as metal ions from metal tweezers or glass containers. In order to obtain a high quality bonding interface, it is

important to remove all these types of contaminations without degrading the bonding surface. Fortunately, the cleaning procedures commonly used in semiconductor industry, such as RCA1 (40% NH_4OH : 30% H_2O_2: H_2O = 1:1:5, 70-80 °C), RCA2 (37% HCl : 30% H_2O_2: H_2O = 1:1:6, 70-80 °C) and piranha (98% H_2SO_4: 30% H_2O_2 = 1:4, 120 °C) clean, are suitable and sufficient for wafer bonding [111,112].

4.2.2.3 Smoothness

At room temperature, wafer direct bonding is based on short-ranged intermolecular attraction force (F) which decreases approximately with the inverse third power of the distance (t) [111, 116,117],

$$F \propto t^{-3} \tag{4.1}$$

For bonding to occur spontaneously, the two mating surfaces must be in sufficient proximity which requires an adequate surface smoothness. Typically, a surface separation up to about 10 Å can be bridged to adhere through the clusters of hydrogen-bonded water molecules. This implies that a surface roughness of 5 Å (0.5 nm) is required for a successful wafer bonding [111,116–118].

4.2.2.4 Flatness

For bonding to be successful, the mating surfaces must be able to conform to each other through an elastic deformation during the bonding process. Therefore, the flatness of bonding interface, which is defined by total thickness variation (TTV), h, has to be smaller than a critical value to enable this required deformation. This critical value, however, is determined by the wafer thicknesses d, Young's modulus E, and the surface energy of the bonded pair γ [111,112,119]. For non-flat surfaces with a wave-shaped topography such as shown in Fig. 4.2, the condition for the gap to be closed during bonding depends on the following equations. For R > 2 d (Fig. 4.2(a)), the condition for gap closing depends on wafer thickness d and is given by,

$$h < \frac{R^2}{\sqrt{1.2Ed^3/\gamma}} \tag{4.2}$$

For R < 2d (Fig. 4.2(b)), the condition for closing the gap is independent of wafer thickness,

$$h < 2.6(R\gamma/E)^{1/2} \tag{4.3}$$

45

It should be noted that for bonding wafers with different thicknesses, the thinner wafer thickness (for a constant Young's modulus) determines the bonding behaviour [111,112,119].
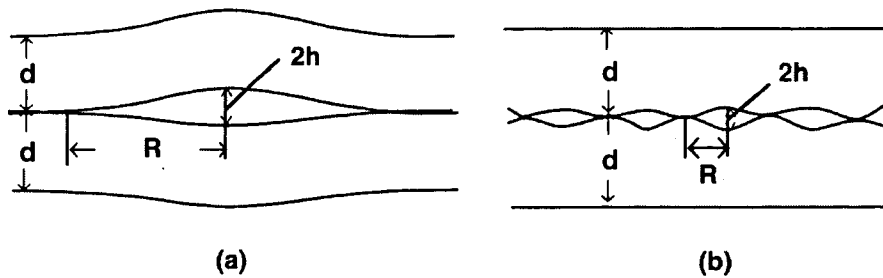
Figure 4.2: *Schematic drawing of gaps caused by non-flat wafer surface [111,112,119].*

4.2.3 High temperature direct bonding

High temperature direct bonding was proposed in 1986 by Shimbo [120] and Lasky [121], and has then been studied extensively. It has evolved to become a fairly mature technology which is evidenced by the successful commercial manufacture of SOI wafers [122]. According to its surface conditions and whether oxide is presented, direct bonding can be divided into two types: hydrophilic bonding and hydrophobic bonding.

4.2.3.1 Hydrophilic bonding

In the hydrophilic bonding process, the increase of the bond strength comes from the conversion of surface silanol (Si-OH) group to siloxane (Si-O-Si) structure during a high temperature anneal [111,112,116]. The reactions at the bonding interface are closely related to the anneal temperatures, and the changes of the interface are depicted in Fig. 4.3 [111,114].

In hydrophilic bonding of silicon, the silicon wafer surface is covered with an oxide layer which can be a thin native oxide, a thermally grown oxide or a deposited oxide. Before bonding, the oxide surface contains both Si-O-Si and Si-OH bonds. However, the hydrophilicity of the surface is determined by the amount of Si-OH groups, and can be enhanced by a number of methods. For example, a warm RCA1 clean or an O_2 plasma treatment can be employed. It should be noted that the hydrophilicity of the surface does not change significantly from room temperature to 110 °C.

After two hydrophilic surface are brought together, Si-O-Si bonds on both of the bonding sur-
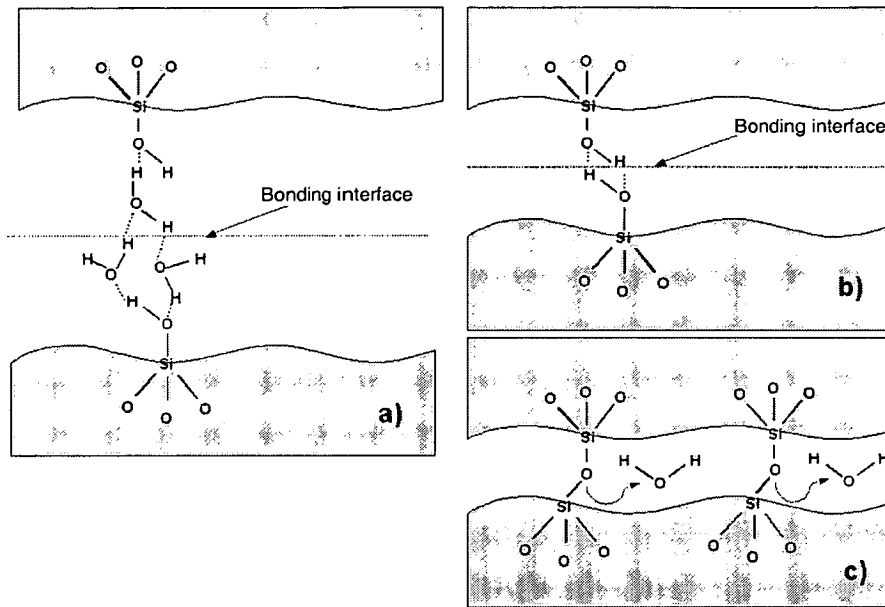
Figure 4.3: *Schematic of the transactions of the hydrophilic wafer bonding interface [111, 114]. (a) bonding via intermediate water molecules, (b) bonding between two -OH groups by van der Waals forces, and (c) formation of Si-O-Si bonds.*

faces react with interface water. This leads to an increased number of -OH groups extending from each surface into the interface region and thus more hydrogen bonds across two mating surfaces.

$$Si - O - Si + H_2O \longrightarrow Si - OH + HO - Si \qquad (4.4)$$
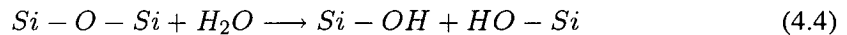
In the meanwhile, the interface molecular water tends to rearrange itself to form more hydrogen-bonded structures, and this tendency is enhanced when the water molecules gain increased surface mobility as temperature increases. At this stage of the bonding process, (25 to 110 °C), the bonding strength comes from the bridges formed by water molecules and -OH$^-$ groups across the wafer surfaces (Fig. 4.3(a)-(b)).

As temperature is increased, from 110 to 800 °C, the conversion of Si-OH at the interface into Si-O-Si dominates the bonding process, which leads to the increase of the bond strength (Fig. 4.3(c)). At this stage of the process, the bonding strength is simply limited by the contact area,

$$Si - OH + Si - OH \longrightarrow Si - O - Si + H_2O \qquad (4.5)$$
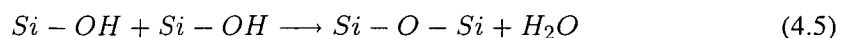
As more Si-O-Si bonds are formed at the bonding interface, more water molecules are produced. In order to continue the reaction, the water molecules produced by the reaction, have

to be able to diffuse out from the interface, dissolve into the surrounding material or react with surface material. If the water molecule reaches the silicon substrate from the interface through the diffusion into the oxide layer, it reacts with the silicon to form silicon dioxide and hydrogen [111, 112, 123],

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2 \tag{4.6}$$
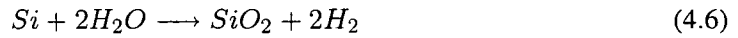
From this, a simple guideline can be derived: if a buried oxide layer is to be produced by wafer bonding, one wafer should contribute the whole oxide, while the other wafer should be bare silicon wafer covered by a native oxide only, to facilitate the diffusion of water molecules to the silicon surface. It is worth noting that hydrogen, produced by the reaction detailed in equation (4.6), has a high solubility in oxide film, and by having an oxide layer of thickness > 50 nm at the bonding interface, hydrogen-induced voids can be avoided.
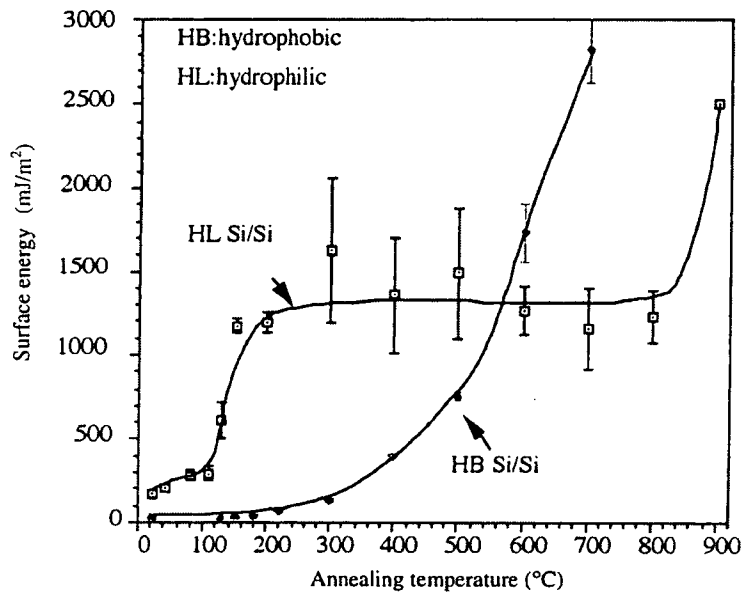
Figure 4.4: *Bonding energy of typical bonded hydrophilic and hydrophobic silicon wafers as a function of annealing temperature [111, 112].*

The oxide at the bonding interface will reflow at a temperature above 800 °C, which helps eliminate possible voids in the bonding interface [111, 112, 116]. Practically, 800 °C has been found to be sufficient for oxide to reflow to fill micro-gaps for a Si-Si bonding with only a thin native oxide. However, temperatures above 1000 °C are necessary for Si-oxide or oxide-oxide bonding, because thick oxide layers may contain water molecules. These are product of the bonding reaction (see equation 4.5), and the existence of water molecules reduces the viscosity of oxide [111, 112, 116]. Due to the oxide reflow, a defect-free bonding can be achieved. The

bond strength as a function of the temperature is shown in Fig. 4.4.

4.2.3.2 Hydrophobic bonding

In hydrophobic Si bonding, silicon wafers are directly joined without any intermediate oxide layer. Typically, a standard hydrofluoric acid etch is performed before bonding to remove native oxide on the wafer surface. This process results in a hydrophobic surface covered with either hydrogen or fluorine terminated dangling bonds [111,112]. The hydrophobic silicon surface is very active and will readily react with hydrocarbons. Therefore, the wafers should be bonded immediately after the treatment to prevent possible contaminations.

At room temperature after contact, the dangling bonds form bridges between two mating surfaces, and the bonding strength comes from van der Waals forces. As the temperature rises to 150-300 °C, additional bonds are formed due to the rearrangement of the hydrogen bonds. If the temperature continues to rise and reaches 400 °C, desorption of hydrogen from the wafer surface starts and the following reaction occurs [111,112],

$$Si - H + Si - H \longrightarrow Si - Si + H_2 \qquad (4.7)$$
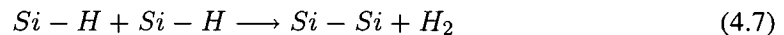
Once the annealing temperature reaches 700 °C, surface diffusion of silicon takes place to close the micro-gaps between the surfaces, which in turn will further increase the bonding strength up to the cohesive strength of bulk silicon, as shown in Fig. 4.4. However, due to the generation of hydrogen which is identified by the reaction detailed in equation (4.7) and the lack of an oxide layer at the interface to dissolve H_2 (hydrogen) gas, undesirable voids may appear at the bonded interface [111,112].

4.2.4 Low temperature direct bonding techniques

4.2.4.1 Introduction

For many applications the high temperatures (800-1000 °C) required to reach sufficient bonding strength present a problem, particularly for pre-fabricated IC wafers or dissimilar materials with different thermal expansion coefficient. Therefore, studies aimed to achieve strong bonding at low temperatures were initiated shortly after the invention of silicon direct bonding. Today, many different approaches for low temperature bonding have been developed and been used

for many applications [111, 112, 114, 124]. In this section, two of the most promising and widely used methods will be presented.

4.2.4.2 Room temperature covalent bonding

The concept behind room temperature covalent bonding is that bonding can be regarded as the reversion of breaking a solid. In principle, for two atomically clean and matching surfaces, the atoms at the surfaces lack part of their nearest neighbours which results in dangling bonds due to this discontinuity. By bringing them together, the formation of the adjoining surface annihilates the dangling bonds, and produces a lower energy level for the covalent bonded structure. This, in turn, motivates the recombination of the whole surface. This concept has been proved to be possible by theoretical calculation and simulation, for example, by the self-consistent pseudo-potential method [125] and semi-classical molecular dynamics simulation [126, 127]. In practice, two broken pieces of a solid usually cannot be joined again after the break, because once broken, the surfaces are oxidised or contaminated immediately. Therefore, to practically realise this concept, the difficulties are surface preparation and preservation. This has been realised for wafer direct bonding and, there are two approaches available with the help of advanced ultra high vacuum technology and surface planarisation techniques.

Gösele et al. [128] demonstrated covalent bonding between two 4-inch (100) silicon wafers at room temperature, and the bonding process is illustrated in Fig. 4.5. In this method, two wafers are first cleaned by RCA1 solution and HF acid to remove any surface contamination and native oxide, which is similar to the standard clean procedure for hydrophobic bonding. Then the wafers are temporarily bonded and transferred into an ultra-high vacuum (UHV) equipment. The bonding performed at this stage preserves the surface condition during the transportation from the clean station to the UHV chamber. Once base pressure of 3×10^{-9} Torr is reached in the vacuum chamber, the wafers are separated. The wafers are then heated up to an elevated temperature (e.g. 500 °C) to remove the hydrogen terminations and to ensure bonding surfaces containing only reactive dangling bonds. The wafers are then cooled to room temperature to prevent any thermal mismatch problems between wafers, and bonded in this UHV chamber. The resulting bonding energy is close to the bond strength of the bulk silicon. Since the bonding process is conducted in the ultra-high vacuum (UHV) environment, this type of bonding is also referred to as UHV-bonding.

Instead of using an elevated temperature (450-500 °C) treatment in an UHV chamber, Takagi
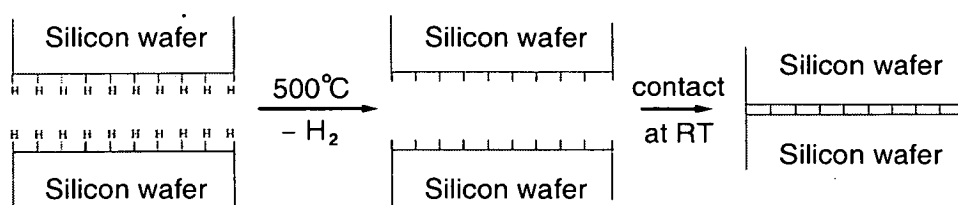
Figure 4.5: *Schematic process flow of the ultra-high vacuum wafer bonding [128].*

et al. [129] and Chung et al. [130] performed their surface treatment using an argon fast atom beam before bonding. In this method, two wafers are firstly cleaned in buffered oxide etchant (BOE, 49% HF : 40%NH$_4$F = 1:6) and piranha solution. Then they are placed into a vacuum chamber with a base pressure of the chamber being 2×10^{-6} Pa. Once the base pressure is reached, the surfaces of the wafers are cleaned by an argon fast atom beam for about 5 minutes with an applied voltage of 1.5 kV and a plasma current of 20 mA. The wafers are then brought into contact in the vacuum chamber with a pressure of 1.0 MPa to result in a strong bond. Since the surface treatment is conducted with an argon fast atom beam, this method is also referred to as surface activated bonding. In addition to the successful bonding of bare wafers, patterned wafers have been bonded with an alignment accuracy better than 2 μm [131].

Room temperature covalent bonding can be performed with all chemically reactive and sufficiently flat materials. Nowadays, not only silicon related materials have been successfully bonded, but also a variety of homogeneous or heterogeneous semiconductor and dielectric materials [129, 132], and even metals [129].

4.2.4.3 Plasma activated direct bonding

For hydrophilic silicon wafer bonding, the increase in bonding energy is based on the conversion of Si-OH groups into Si-O-Si groups. This conversion has been reported [133, 134] to occur at low temperature for the sol-gel materials, which encouraged researchers to think that the achievement of high bonding strength at low temperature was also possible. However, for the condensation process of sol-gel glass, the reaction by-product, water molecules, can be easily diffused out through the film surface, which is not the case for water molecules trapped between two bonded wafers. It is then believed that the diffusion or consumption of water molecules at the bonding interface is the key to achieve a high bond strength at a low anneal temperature. Many approaches have been proposed to modify the wafer surface before bonding in order to remove water molecules at the bonding interface [112]. Of these, plasma activated
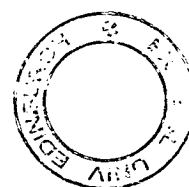
direct bonding is the most promising one.

In this process, bonding wafers are placed into a plasma system for a short time plasma etch. A DI water (deionised water) or RCA1 rinse step, is then performed after the wafers are brought out from the plasma chamber. The wafers are then dried and brought into contact at room temperature in a similar manner to the standard direct bonding procedure. The process is completed with an anneal at elevated temperature, typically, 100-450 °C.

High bond strength (e.g. > 2.0 J/m^{-2}) at low temperature has been reported in many articles that use the plasma activation process before bonding [92,135–140]. However, the exact mechanism behind this treatment is still unclear. Some effects caused by plasma treatment have been observed. For example, it is found that a highly hydrophilic surface has been created due to the plasma treatment and the effect can last for several days [92]. It has also been reported that the plasma exposed surface increases the kinetics of reaction produced water molecules which may increase the water diffusion process [138]. It has been suggested that any attached contaminations, such as hydrocarbons, which are difficult to remove by conventional wet chemical clean processes, can be removed from the bonding surface by the plasma treatment [136]. Since the plasma process is a complex reaction and many effects take place at the same time, the resulting high bonding strength may not rely on one effect, but a combination of many.

Although the exact mechanism behind plasma treatment is not fully understood, it has been possible to optimise the process conditions to achieve high quality bonding. All types of plasma systems, such as RIE (reactive ion etching), ICP (inductively coupled plasma) or barrel type systems, and process gases, such as N_2 (nitrogen), Ar (argon) and O_2, can be used for the surface treatment and have been reported to produce good bonding results. However, the striking power, applied bias, and process time must be optimised to suit the specific plasma system [92, 136, 137, 139, 140]. In general, higher plasma power and longer treatment time increase the bonding strength. However, these are circumstances which may introduce more interfacial bubbles [92, 136, 137]. The RCA1 or DI water rinse step after the plasma treatment is believed to add more -OH^{-} groups on the wafer surface and remove any possible metal or particle contaminations from the plasma treatment (RCA1 is more effective than DI water for doing this). However, the optimum time for an RCA1 dip needs to be determined because RCA1 etches silicon dioxide at a very slow rate which might remove the surface effects generated by previous plasma treatments [136].

Plasma activated bonding is similar to room temperature covalent bonding as it is also capable of bonding similar and dissimilar materials, as well as prefabricated wafers. In addition, plasma assisted bonding has the following advantages: (1) General availability of the required equipment. Plasma etching systems and wet benches are normally available in all semiconductor or MEMS fabrication facilities. (2) Possibility of wafer alignment. Since the wafers can be brought out from the vacuum chamber after plasma treatment, the alignment process can be performed in atmosphere by using a bonding aligner, which is again a common tool for cleanroom operation.

4.3 Anodic bonding

Anodic bonding was first proposed by Wallis and Pomerantz in 1969 [141], and is also referred to as electrostatic or field-assisted bonding. It has been primarily used for bonding silicon to glass, but other material combinations have also been demonstrated over the years. It has been widely used for building MEMS structures, such as micropumps, and encapsulation of MEMS devices, such as pressure sensors, accelerometer and gyroscopes [33].

The anodic bonding process is an electro-chemical process. In anodic bonding, the glass and silicon wafers are placed into intimate contact with an external applied DC voltage (50-2000 V) and at elevated temperature (280-450 °C). The applied DC voltage creates an electrical field which drives sodium ions (Na^+) away from the silicon-glass interface, and the mobility of Na^+ in the glass substrate can be increased by the elevated temperature. The drift of Na^+ forms a Na^+-depletion zone and leaves oxygen ions (O^{2-}) at the bonding interface, as shown in Fig. 4.6. The oxygen ions can diffuse to the silicon surface and react with the silicon which leads to the formation of an amorphous oxide layer. The formation of oxide is responsible for the increase of the bonding strength.
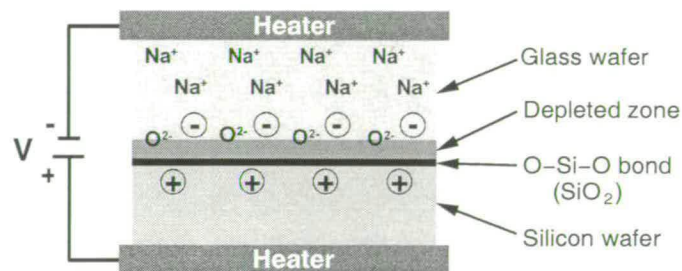
Figure 4.6: *Schematic of the anodic bonding technique.*

The requirements for the anodic bonding are: (1) the glass substrate should contain mobile ions, for example, Na^+; (2) the thermal expansion of the two materials needs to be matched; (3) the bonding surfaces must be clean, flat and fairly smooth (< 5 nm). The most common glasses used for anodic bonding are Pyrex 7740 and Schott 8330, which are sodium borosilicate glasses, and have thermal expansion coefficients close to that of the silicon wafers.

Anodic bonding, at relatively low temperature (280-450 °C), can achieve a bond strength which is higher than the fracture strength of the glass. It can also be performed in vacuum, allowing the formation of hermetical sealed cavities. It is also a high yield and robust process which is more tolerant to surface particles and surface roughness, compared with < 0.5 nm in direct bonding. Moreover, the transparency of the glass enables simple, but highly accurate, alignment of pre-patterned glass and silicon wafers, and also enables visible detection of structures inside the devices through glass, for example, micro fluidic devices. The main drawback of this technique is that the bonded wafer cannot be allowed back into a CMOS process line since it contains alkali metal ions (e.g. Na^+) in the system.

4.4 Intermediate layer bonding

Another method of bonding wafers is via an intermediate layer. This approach has facilitated numerous applications in modern semiconductor IC and MEMS fabrication. Intermediate layer bonding can be generally divided into two categories: adhesive bonding and metallic bonding.

4.4.1 Adhesive bonding

Adhesive bonding, as the name suggests, means that the bonding between two wafers is through an adhesive layer. Examples of adhesive materials are sol-gel [142], spin-on-glass (SOG) [143], parylene [144], photoresists, polyimides and benzocyclobutane (BCB) [145, 146]. A typical adhesive bonding procedure is detailed in Table 4.1. Typically, the bonding can be performed in a vacuum environment in a commercial bonder with an applied pressure for the final curing of the adhesive material.

Adhesive bonding is a low temperature process, and IC-compatible for some of the adhesive materials. It is capable of bonding wafers with different substrate materials and protruding structures. Moreover, it is also cheap, easy to apply and gives high bonding strengths and high

Step	Process
1	Wafer surface cleaning
2	Applying the adhesion promoter to both wafers
3	Spin-coating an adhesive layer on the target wafers
4	Pre-curing of the adhesive layer
5	Wafer aligning and bonding
6	Adhesive material final curing

Table 4.1: *A typical adhesive bonding process.*

process yield. The disadvantages of this technique are that adhesive bonding does not lead to a hermetic seal, and adhesive materials may have a limited thermal stability and problems of long-term reliability. Adhesive bonding has been widely used in applications where hermeticity is not required, for example, processed layer transfer [62, 146, 147], and integration of CMOS circuits with MEMS/MOMS devices [148].

4.4.2 Metallic bonding

Metallic bonding uses an intermediate metal layer between the wafers to provide necessary mechanical strength or electrical interconnections, which consists of solder, eutectic and thermocompression bonding. The solder bonding process works by reflowing low melting point metals to form a seal. In the solder bonding, metal structures can be applied on one of the wafers by various thin film deposition techniques. Once these solder metals are aligned to the contact pads on another wafer, bonding is performed by the reflow of solder at low temperature (e.g. 200 °C) [149]. Typical solder metals are SnPb, SnCu or SnAg. The solder technique is tolerant to surface particles and has been widely used for electrical contacts (e.g. flip-chip bonding).

Eutectic bonding is based on the fact that the eutectic composition material has a lower melting point at the interface than either of the individual materials. Bonding between two wafers can be formed by depositing one of the wafers with one component of the alloy and the other wafer with the second component. When the wafers are heated and brought into contact, eutectic fusion occurs at the interface and bonding is established. Typical eutectic materials are Au-Si, Au-Ge and Au-Sn [150]. The eutectic bonds are strong and hermetic, and have been widely used in MEMS packaging.

In thermocompression bonding [151–153], two metallic surfaces are joined using high pressure

(10 MPa) at temperatures from 200 to 450 °C. The high bonding strength is attributed to the migration of atoms across the interface, and the recrystallisation and growth of the metal grains [154], as can be seen in Fig. 4.7. The most commonly used metals are Au, Cu and Ti, and the required bonding conditions are compatible with most of the commercially available wafer bonders. Since small metal structures can be used in this bonding technique, very high density interconnects between wafers can be established [151, 152].
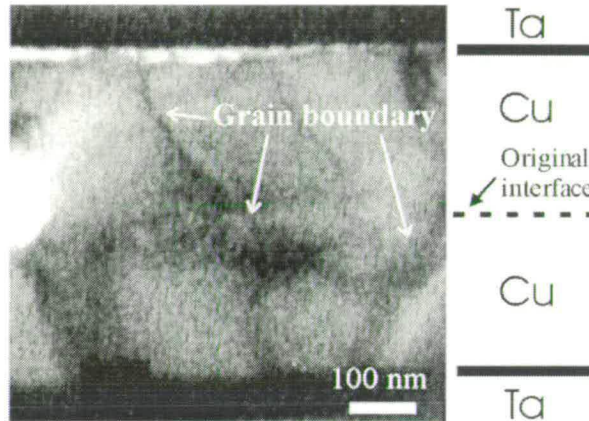
Figure 4.7: *High resolution SEM image of a thermocompression bonded Cu-Cu interface [154].*

Metallic bonding provides a hermetic seal and has very low outgassing, and so it is attractive for sealing evacuated cavities for MEMS applications. With the recently developed IC-compatible Cu and Ti bonding process, the fabrication of three-dimensional ICs and wafer-level packaging are under extensive study [152, 155].

4.5 Bonding quality evaluation

The quality of the bonding is mainly determined by the following measurable quantities: (1) the percentage of voids at the bonding interface, (2) the adhesion strength of the bond, and (3) the electronic properties of the bonded structure [156]. In this section, only the first two aspects will be discussed because they are the most important factors related to integrate MEMS and CMOS wafers using wafer bonding. However, if the bonded interface is part of the device structure, for example, building MOS device on a SOI wafer, the electronic properties of the interface will also be an important aspect.

4.5.1 Void detection

Voids, also known as interface bubbles, are the unbonded areas of the bonding interface which are intended to be bonded. Depending on their origin, voids may be present immediately after contacting the wafers or after storage or annealing process. Uneven surfaces, particles, or trapped gases can cause voids from the beginning of bonding [112]. The generated voids, which appear in the later stages of the bonding process, are caused by the local accumulation of gases. These gases can stem from (1) bonding material outgassing, (2) trapped gas during bonding, (3) thermal decomposition of surface contaminants, such as hydrocarbons, and (4) products of chemical reactions at the bonding interface, such as H_2 [123]. Optical inspection and scanning acoustic microscopy are two widely used non-destructive techniques for the detection of these interfacial voids.

4.5.1.1 Optical inspection

With optical inspection, Newton's rings are observed at the unbonded areas due to the interference of light reflected on internal surfaces. Whilst the shape of the rings shows the shape of the void, the number of rings enables an estimation of the gap between the unbonded surfaces [157]. If one of the bonded wafers is transparent (e.g. glass, quartz, or sapphire), voids can be observed by the naked eye. For silicon wafer bonding, an infrared transmission imaging system is required which consists of a light source and a CCD (charge-coupled device) camera, as shown in Fig. 4.8.
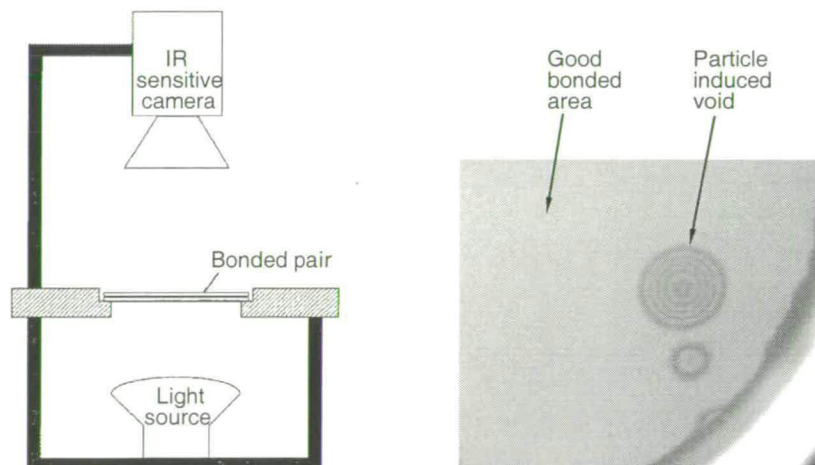
Figure 4.8: *Interface voids inspection using an IR imaging system: (a) schematic illustration of the IR imaging system, and (b) IR image of a bonded silicon wafer sample.*

The advantage of this technique is that it is fast, easy to use, and non-destructive. Additionally, the inspection can be performed immediately after wafer contact, when debonding is possible in the case of unsatisfactory interfacial bonding. However, it does not detect all voids. To detect a void with an IR imaging system, the separation of the surfaces must be at least one fourth of the IR wavelength ($\sim$ 1.0 μm) [158], and the lateral resolution is typically limited to about 1 mm [157].

4.5.1.2 Scanning acoustic microscopy

For voids detection, the scanning acoustic microscopy (SAM) works like a sonar device which sends an acoustic signal and measures the time it takes to reflect back to the detector. The typical intermediate material between the sample and the emitter-receiver is water. Compared to IR inspection where only the large and particle induced voids can be detected, the SAM has a better sensitivity. Theoretically, a lateral resolution of 0.5 μm and vertical resolution of 10 nm can be achieved [159, 160], but this requires a high frequency, a thin sample and very long scanning time. Given a few minutes of scan time for a full 4-inch wafer, a lateral resolution of about 50 μm can be achieved, which is desirable to obtain the information of the bonding interface before further fabrication processing. The major drawback of SAM compared to IR inspection is the necessity to do bond annealing before the detection. This anneal step is used to prevent debonding of the wafer pair when it is immersed in water.

4.5.2 Bonding strength measurement

Bond strength is one of the most important characteristics for the bonded wafer pairs. It is not only a determination of the integrity and reliability of the bonded structures, but is also a critical parameter on the post bonding processes, such as grinding, polishing, patterning, and etching. Moreover, the accurate measurement of the bonding strength can be vital for process understanding, bonding process optimisation, and quality control. Basically, four methods have been used to measure the bonding strength: (1) blade insertion test, (2) tensile test, (3) burst test, and (4) chevron test, which are shown schematically in Fig. 4.9-4.10.

4.5.2.1 Blade insertion test

The blade insertion test is also known as crack open method or the double cantilever beam test. For this test [158, 161, 162], a wedge of a thickness of $2h$ is inserted at the rim of the beams into the bond interface so as to debond an area of crack length c, as shown in Fig 4.9(a). At equilibrium, the fracture surface energy γ can be expressed as follows,

$$\gamma = \frac{3Eh^3d^3}{8c^4} \tag{4.8}$$

with d being the thickness of the beams and E denoting Young's modulus in the direction of crack propagation. It can be observed that the accurate measurement of the cracking length c could be problematic, but the value of c is the most critical parameter in the equation since the surface energy γ is inversely proportional to c^4. It can be deduced that the greater the bonding energy, the smaller the cracking length c, and the bigger the error that will be generated during the measurement. It is also difficult to insert a thin blade into a strongly bonded wafer, as it is quite likely that the bonded wafer pair will break. Therefore, it can be concluded that this method is more suitable for the measurement of low bonding strength. Despite the drawbacks, the blade insertion test is still the most popular method because it can be performed with inexpensive equipment, and no wafer preparation is required.
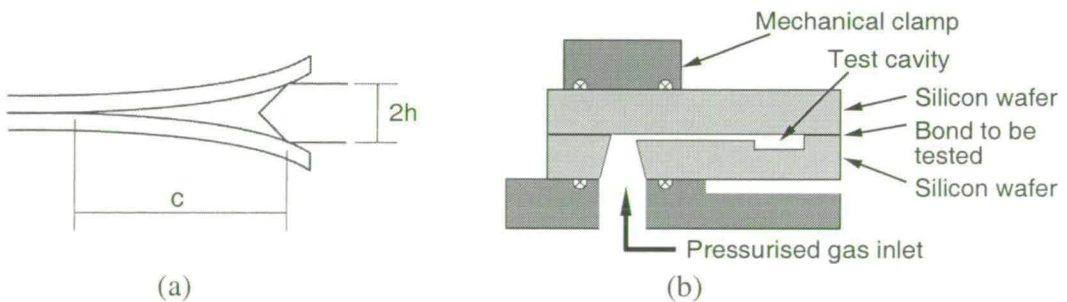
Figure 4.9: *Wafer bonding strength measurement systems [156]: (a) crack open method and (b) burst test.*

4.5.2.2 Burst test

The burst test is also known as blister test. For this test, a load is applied to the bonding interface by pressurising internal cavities which are sealed by wafer bonding (Fig. 4.9(b)). The required pressure for sample debonding is measured and can be used to estimate the surface energy of the bonded interface. For some specific cavity geometries, such as circular and channel-like

structures, expressions for bonding energy have been derived [156].

The burst test is capable of measuring all bond strengths and the repeatability is better than many other evaluation techniques. In addition, with improved test structures (see Fig. 4.9(b)), it does not require a sample gluing procedure, which is the most inconvenient and time-consuming step. However, the method requires test patterns to be made on wafers prior to bonding, and cannot be used for bonds containing macroscopic unbonded areas or non-hermetically sealed samples.

4.5.2.3   Tensile test

The tensile test is also known as pull test. In this case the bonded wafer is diced into small pieces with a defined area (A). Then, both sides of the testing samples are glued to the pulling rods of a test apparatus. Once the glue has fully dried, samples can be installed into the test apparatus for the tensile strength measurements. In the measurement, a pulling force is applied and increased gradually until the joint is separated, as shown in Fig. 4.10(a). The force (F) required to pull apart the joint is recorded and can be used to estimate the tensile strength (α_T),

$$\alpha_T = \frac{F}{A} \tag{4.9}$$
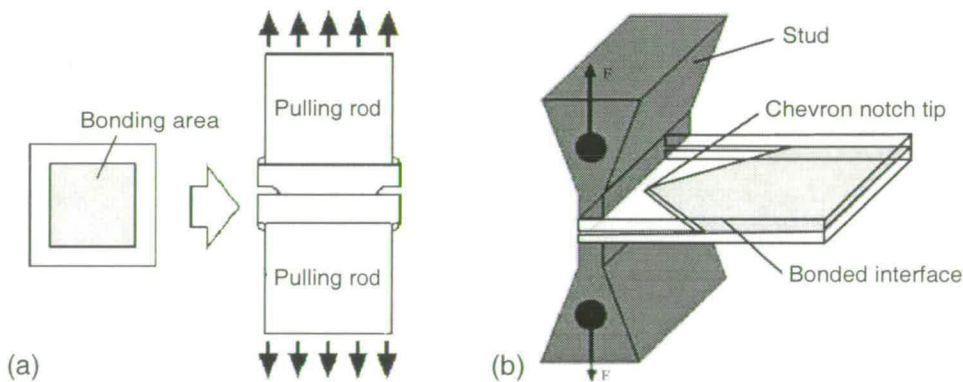
Figure 4.10: *Wafer bonding strength measurement systems [156]: (a) tensile test and (b) chevron method.*

The tensile test is easy to use and capable of measuring all bond strengths. Since the tensile test is able to measure bond strength from small samples, bonding strength maps for the wafers can be obtained (using samples from different parts of the wafer), which is very useful for yield improvement and quality control. However, a large scatter in measurements may occur due to

the brittleness of the materials used in the wafer bonding. During the measurement, the stress is applied to the entire volume of the test joint and is not concentrated on the bond interface. Brittle materials will fracture at their weakest point, which is not necessarily the bonding interface. Consequently, unintended fracture may take place in the bulk silicon substrate or at surface imperfection points, such as edge damage from wafer dicing or at the glue line. Fortunately, this issue has been solved in the chevron method.

4.5.2.4   Chevron method

In chevron method [163], one of the wafers has chevron-shaped patterns on the surface before bonding, and it is bonded to an unpatterned wafer. Pulling studs are then glued to the sample after wafer dicing and a pulling force is introduced (Fig. 4.10(b)). The force is increased gradually and a crack will be started from the tip of the chevron at some point. While the force increases, the crack propagates. When the crack reaches its critical length, the crack growth becomes unstable and a fracture at the bonding interface becomes inevitable. At this point, the loading force is measured. Since the critical crack length depends only on the loading force and the specimen geometry, the critical force for fracture to occur is, therefore, a measure of the bond strength.

This method is considered to be the most accurate measurement technique for determining the bond strength, as the critical loading force can be measured more accurately than the crack length. This method is also suitable for measuring high bond strengths because the fracture has been purposely started at the bonded interface by the patterning of the chevron tip. Moreover, since small chevron shapes can be located all over the bonded wafer, bond strength maps can also be obtained. The main drawbacks of this method are the necessity of wafer patterning before bonding, and gluing during sample preparation.

4.6   Application of wafer bonding

Wafer bonding has numerous applications which can be found in many journals and conference papers and several books [111, 112]. These applications have the greatest diversity, covering many areas of modern semiconductor and MEMS fabrication technology, and cannot be easily summarised in one section. Therefore, in this section, only two important mainstream applications and an emerging one will be presented.

4.6.1 Advanced substrate engineering

4.6.1.1 Silicon-on-insulator (SOI)

A silicon-on-insulator (SOI) wafer consists of a silicon handle wafer, an oxide layer and a silicon device layer. Based on the thickness of the silicon device layer, SOI wafers can be categorised into two types: (1) thick film SOI (a few microns to tens of microns) which is most likely to be used for the fabrication of MEMS structures, (2) thin film SOI (a few nm to 1-2 microns) for the fabrication of advanced MOS devices. Note SOI wafers for IC devices are also fabricated by the implantation of oxygen method (separation by implantation of oxygen, SIMOX [114]), which will not be discussed here. High temperature $Si-SiO_2$ direct bonding, which provides the necessary mechanical strength for the bonded structure, is an indispensable step for the fabrication of SOI. Although the bonding process is quite similar for both thin and thick film SOI wafers, the thinning methods are very different. Thick film SOI wafers are normally made by bonding, grinding and polishing. In this procedure, a standard direct bonding process is performed first to achieve a high bonding strength. Then the grinding process provides a cheap, precise and fast wafer thinning process, and the resulting rough surface can be smoothed by the subsequent polishing (chemical mechanical polishing, CMP). For some applications, thick film SOI is replacing conventional Si wafers as the starting substrate for MEMS fabrication. The advantage of SOI substrates is that the buried oxide layer can be used as sacrificial layer, and by etching it different types of diaphragms, films and beams can be released.

For thin film SOI wafer fabrication, the most common method nowadays is Smart-Cut^{TM} [164]. In this method, hydrogen is implanted into one wafer, donor wafer, which induces an in-depth weakened layer of voids. The donor wafer is then bonded to a handle wafer using standard wafer bonding processes. During the first wafer anneal step at 300-600 °C, while the bonding strength of the donor and handle wafers increases, the splitting of the donor wafer takes place along the in-depth weakened layer which enables the transfer of a thin layer from donor wafer to handle wafer. A treatment should be performed to remove possible particles and the rough surface left after splitting. The bonding strength of the thin transfered layer and handle wafer can then be further increased by a final anneal at 800-1100 °C. The remainder of the donor wafer can be polished and reused for a number of times in the process which saves the material cost. Thin film SOI wafers provide many advantages for IC fabrication. For example, the switching speed of transistors fabricated on SOI is increased by 20-50% compared to those

on a bulk Si wafer, and also, the required operating voltage is lower for ICs on SOI than those on a bulk silicon wafer which decreases power consumption and reduces the problem of chip heating.

4.6.1.2 Strained Si-on-insulator

The performance of MOS devices can be improved if they are fabricated on strained silicon because carrier mobility increases when the silicon device layer is under tensile stress [165,166]. This improvement can be further enhanced by combining with the advantages of SOI, which results in the development of this advanced substrate: strained silicon-on-insulator (sSOI). The strain in silicon is typically introduced by epitaxially growing silicon on a material with a larger lattice constant, such as SiGe. Therefore, sSOI is usually fabricated on a SiGe-on-insulator (SGOI) substrate. Wafer bonding is one promising method to fabricate both of these substrates. In one fabrication method [165], a strain-relaxed SiGe layer is grown on a silicon donor wafer by ultra high vacuum chemical vapour deposition. The SiGe epi-layer is then polished and bonded to an oxidised silicon handle wafer. The donor wafer can be removed by the conventional methods, including grinding and polishing or ion-implantation based Smart-Cut^{TM}. Once the SGOI substrate is prepared, a thin silicon layer, which will be strained due to the lattice mismatch, can be grown on top of the SiGe layer.

Building a strained silicon layer on top of SGOI substrate, however, poses several challenges. For example, it is difficult to develop a controllable procedure which can fabricate sSOI wafers with a combined thicknesses of strained silicon and relaxed SiGe below 30 nm. And also, the presence of the SiGe layer alters the dopant diffusion behaviour and possibly diffuses of Ge into the strained silicon layer. Therefore, it would be advantageous to have sSOI wafers without a buried SiGe-layer.

SiGe-free strained Si-on-insulator substrates have been fabricated by wafer bonding and layer transfer [167]. In this method, a donor wafer containing a strained Si layer on SiGe-on-Si substrate is firstly fabricated. A hydrogen implantation is then performed, which penetrates through the strained thin Si layer (tens of nm) into the SiGe ($Si_{0.68}Ge_{0.32}$) layer. This wafer is then bonded to an oxidised silicon handle wafer, and annealed to strengthen the bonding and to induce the hydrogen splitting of the SiGe layer. After splitting, the remaining SiGe layer on the handle wafer can be removed by a combination of low temperature steam oxidation and dilute HF etching. The handle wafer then becomes a sSOI substrate without a buried SiGe-layer.

4.6.1.3 Compliant substrate

Heteroepitaxy is a common method for fabricating heterogeneous substrates for improving the performance of electronic and optoelectronic devices [168, 169]. However, high density of interface defects, which causes severe deterioration of the optical and electrical properties of the structure, are formed due to the lattice and thermal mismatches between different materials. In order to minimise the amount of these defects, a compliant substrate can be used. The compliant substrate uses a thin sacrificial layer between the epitaxial material and the bulk substrate, to accommodate any misfit by deforming elastically or plastically.
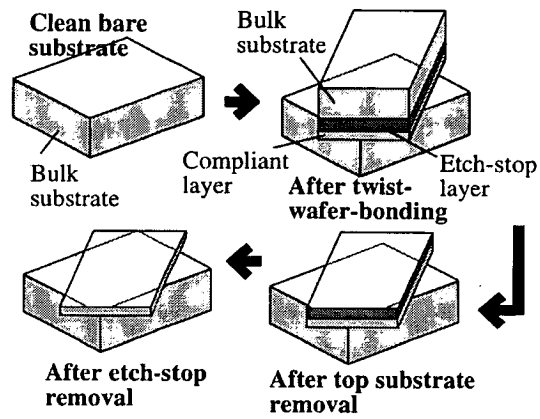
Figure 4.11: *A conceptual schematic illustrating the process of forming a compliant substrate using twist wafer bonding [170].*

Twist-bonding is one of the most promising methods for compliant substrate fabrication [170, 171]. In this method a thin layer of material (several to tens of nm) is transferred (using wafer bonding and Smart-Cut^{TM}) to a handle wafer of the same material with a large angular lattice misalignment (tens of degrees). The twist-bonded thin layer is believed to have a weak boundary due to a network of screw dislocations which can accommodate the slip resulting from growth of a mismatched layer [170, 171]. With the presence of this compliant thin layer, a thick layer of another material can be epitaxially grown onto this handle wafer with low density of interface defects. Using this method, an InSb (14.7% lattice mismatch) layer with thickness of 6500 Å has been grown on a 30 Å twist bonded GaAs layer without observing any threading defects in the grown layer (by cross-sectional transmission electron microscopy, XTEM). This is a remarkable improvement compared to the high density of defects observed in the same layer grown on a bulk GaAs wafer [170]. With the increasing use of heteroepitaxial grown layers in electrical and optoelectrical applications, the development of compliant substrates will remain a hot topic in wafer bonding and substrate engineering.

4.6.2 MEMS fabrication and packaging

Substrate formation, complex structure fabrication and MEMS device packaging are the important areas where wafer bonding provides indispensable contributions for MEMS technology. As mentioned previously, thick film SOI wafers are being used more and more as the starting substrates for MEMS fabrication. The buried oxide layer can be used as a sacrificial layer, with single-crystal silicon film above this oxide, which has better and more controllable mechanical properties than conventional poly-crystalline silicon [32]. Hence, it can be used to form various types of diaphragms and beams. Wafer bonding is one of the common methods for fabricating SOI wafers and can also be used to create a large variety of new substrates by combining different types of materials, such as III-V and II-VI compounds [112], which can be used for fabricating detectors, light sources and other MEMS components.

Wafer bonding has also been widely used to create various complex MEMS structures, such as micro-fluidic elements. The simplest fluidic structure is a flow channel that can be formed by etching trenches into one or both substrates and followed by an aligned wafer bond. This type of bonded structure has been realised in many forms for a wide range of applications, such as ink-jet print heads, biomedical mixers and micro total analytical systems [1]. Other structures can also be formed by bonding two wafers for applications such as optical scanners controlled by vertical comb fingers [172]. The bonding process is not restricted to only two wafers bonding. Stacking more patterned wafers is possible and has been demonstrated for realising more sophisticated MEMS devices. For example, an electrostatic valve has been realised through a four-wafer bonding process and a miniature gas turbine engine has been built by a six-wafer process [173].

Some of the earliest applications of wafer bonding were for packaging of pressure sensors [1, 33]. Nowadays, MEMS packaging still requires wafer bonding technology for the following reasons: (1) Vacuum seal. Many MEMS devices, such as gyroscopes, accelerometers and resonators need to be operated in a high vacuum environment in order to achieve a high quality factor due to the reduced air damping. Wafer bonding can provide the required vacuum and also a reliable vacuum seal. (2) Surface protection. Many MEMS devices contain fragile surface structures which are sensitive to particle contaminations or chemical corrosion, and are easily damaged. Wafer bonding provides the necessary surface protection. (3) Cost-effective. Packaging may contribute up to 90% of the total device fabrication costs. Wafer bonding provides wafer level encapsulation which enables packaging of multiple devices in a single run. This

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can significantly reduce the packaging cost per chip.

For most of the packaging applications, wafer bonding has to be performed at low temperatures (less than 450 °C) in a vacuum chamber. These conditions can be satisfied by many commercially available bonding tools. Anodic bonding and eutectic bonding have been used for this purpose for many years [1, 33]. Recent progress in wafer bonding technology has provided more options for packaging, some of which are IC-compatible. For example, room temperature covalent bonding [129], plasma activated low temperature bonding [174] and anodic bonding [175] have been used for wafer-scale encapsulation.

4.6.3 Processed layer transfer

Processed layer transfer refers to the fabrication technology which can transfer a prefabricated device layer from one wafer onto a new mechanical support or onto another prefabricated wafer. The transfer process consists of surface planarisation, wafer bonding and unwanted substrate removal. The development of the transfer technology has been initiated from the advances in surface planarisation and wafer bonding technologies. As prefabricated wafers normally possess severe topography and a rough surface, and also contain metal structures, modern planarisation techniques, such as chemical mechanical polishing, can be used to produce a flat and smooth surface on the fabricated wafers to meet the requirements for the subsequent wafer bonding process. Many low temperature bonding techniques (< 450 °C) also enable the wafer bonding without affecting existing contained metal structures. In terms of wafer thinning, there are many options, such as grinding, wet or dry etching, which are all readily available. The transfer technology allows the combination of materials which cannot be assembled before processing, for example due to thermal expansion mismatch, or devices built on different technologies. It has been used for 3-dimensional (3D) IC fabrication [155], performance improvement for RF devices [147] and the integration of MEMS and CMOS devices [55, 176].

The improved performance achieved with transfered RF devices [147] clearly demonstrates the advantage of this technology. For RF applications, the silicon substrate produces desirable active devices on one hand, but degrades the performance of these devices and the circuits on the other hand. This is because all the devices on a silicon wafer have a capacitive coupling to the resistive substrate, this results in a dissipation of RF energy, cross-talk, and injection of thermal noise. These issues can be solved by an active device layer transfer process. In this process, RF devices are firstly fabricated on a SOI wafer, which is then bonded, top down, to a

glass wafer through an adhesive layer. After the curing of adhesive by UV exposure through the glass substrate, the silicon substrate can be removed using the buried oxide layer (BOX) as an etch stop. Bond pads can then be opened in the BOX layer after the wafer thinning process, as shown in Fig. 4.12. In addition to glass substrates, other substrates such as aluminium nitride, alumina or ferrite can all be used as alternative carriers to replace the silicon substrate. The successful transfer of the processed layer effectively eliminates the drawbacks of silicon as a substrate for RF circuits and enables the integration of passive components when required.
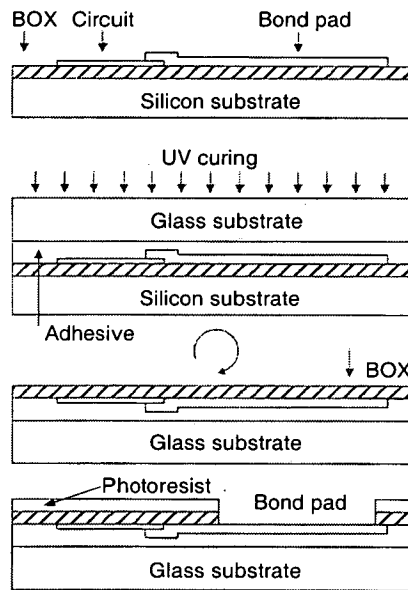
Figure 4.12: *Schematic of an active RF device layer transferred from an SOI wafer to a glass substrate [147].*

4.7 Conclusions

Many advances have been made in wafer bonding technology over the last decade, which have enabled numerous new applications. Two major achievements have been presented during this review are: (1) Low temperature. The required temperatures for direct bonding have dropped from 800 °C or 1100 °C to room temperature with the assistance of ultra high vacuum (UHV). Even without UHV environment, plasma activated wafer bonding and other approaches can achieve high quality bonding at temperatures between 100 °C and 450 °C, which is below the critical temperature that may cause serious performance degradation to prefabricated devices or thermal mismatch to different materials. (2) IC-compatibility. Many IC-compatible bonding techniques have been developed. Examples of these include intermediate layer wafer bond-

ing using materials such as BCB (benzocyclobutane), Ti and Cu, or plasma activated wafer direct bonding. Based on these new advances, various new material combinations have been developed and the integration of prefabricated different devices has also been attempted. In the future, with better understanding of the fundamental principles of various bonding techniques, combined with advances in other fabrication areas, such as planarisation techniques, wafer bonding technology will enable many more new applications.

Chapter 5
Direct Bonding of Processed Wafers

5.1 Introduction

Bonding CMOS and MEMS wafers to create an integrated system requires bonding of prefabricated wafers and the formation of interconnects between bonded wafers. Issues associated with bonding prefabricated wafers using CMP and oxygen plasma assisted low temperature wafer bonding are presented in this chapter.

5.2 Bonding surface preparation using CMP

5.2.1 Top surface layer

Plasma enhanced chemical vapour deposited oxide is a good candidate for a bonding surface because its material properties are suitable for direct wafer bonding [111], and it also has a low deposition temperature (typically 300 °C). However, it is important that the deposition conditions are characterised to ensure appropriate film properties. Two PECVD oxide deposition processes have been evaluated using an STS Multiplex CVD system, and the process conditions are detailed in Table 5.1.

Deposition parameters	High frequency process (HF)	Low frequency process (LF)
Pressure	900 mTorr	550 mTorr
Platen temperature	300 °C	300 °C
Showerhead temperature	250 °C	250 °C
N_2 flow rate	392 sccm	392 sccm
N_2O flow rate	1420 sccm	1420 sccm
SiH_4 flow rate	10 sccm	12 sccm
RF frequency	13.56 MHz	380 kHz
Plasma power	30 W	60 W

Table 5.1: *Parameters for high and low frequency PECVD oxide deposition processes in an STS Multiplex CVD system.*

To characterise these processes, a 2.2 μm PECVD oxide layer was deposited on bare silicon or thermally oxidised wafers, which were then densified for 16 hours at 435 °C to drive out H_2 and to release any residual film stress [93]. The densification temperature was selected to achieve a desirable film stress after the process [177] and also to avoid any degradation of the Al interconnect on the wafer. The wafer curvature, before and after each processing stage, was measured using a Dektak 8000 stylus profiler, and the film stress (σ) calculated as [178],

$$\sigma = \frac{1}{6} \left(\frac{1}{R_{post}} - \frac{1}{R_{pre}} \right) \frac{E}{(1 - \nu)} \frac{t_s^2}{t_f} \qquad (5.1)$$

where, R_{pre} and R_{post} represent the substrate radius of curvature before and after the fabrication process respectively, E: Young's modulus (approximately 130 GPa for silicon substrate), ν: Poisson's ratio (typically 0.22), t_s: substrate thickness, and t_f: film thickness. It should be noted that negative values represent compressive stress (convex wafer surface) and positive values for tensile stress (concave surface). The measured stresses are presented in Table 5.2.

Stress measurement	HF PECVD oxide (HF-SiO$_2$)	LF PECVD oxide (LF-SiO$_2$)
After deposition	- 155 MPa	- 254 MPa
After densification	+ 55 MPa	- 118 MPa

Table 5.2: *PECVD oxide film stress measurement.*

Although a favourable higher deposition rate (800 Å min^{-1} for HF-SiO$_2$ and 500 Å min^{-1} for LF-SiO$_2$) and smoother surface (R_a of 3.0 nm for HF-SiO$_2$ and 5.6 nm for LF-SiO$_2$) can be obtained from high frequency PECVD oxide (HF-SiO$_2$) deposition process, the characteristic for selecting HF-SiO$_2$ is its low film stress after the densification step (see Table 5.2).

5.2.2 Surface roughness reduction

An oxide CMP process was used on all the PECVD oxide deposited wafers using a Presi E460. The range of times and the process condition investigated are listed in Table 5.3. The surface roughnesses of the wafers at different process stages were measured using a Digital Instrument D5000 atomic force microscope (AFM). The measured roughness at different processing stages is presented in Table 5.4, and an example of the surface profile of the oxide film, before and after CMP, is shown in Fig. 5.1. The AFM results indicate that the original PECVD oxide surface is too rough for subsequent bonding which requires the roughness to be less than 0.5 nm [111]. Fortunately this can be reduced with CMP, as demonstrated in Table 5.4 and Fig.

5.1.

Parameter	Setting
Head speed	40 revolutions per minute (rpm)
Table speed	40 revolutions per minute (rpm)
Head pressure	0.30 bar
Back pressure	0.15 bar
Slurry flow	150 ml/min
Temperature	Room temperature
Pad	Rodel IC1400
Slurry	30H50
Time	1-3 minutes

Table 5.3: *Process variables and consumables settings for oxide polishing.*

Surface Conditions	R_a (nm)	R_{MS} (nm)	Z_{range} (nm)
Fresh Silicon Wafer	0.124	0.296	6.177
PECVD Oxide	2.902	3.615	32.90
Oxide Densification	2.819	3.748	26.82
CMP Process	0.119	0.159	2.007

Table 5.4: *Comparison of surface roughness at different processing stages.*

(a)   (b)
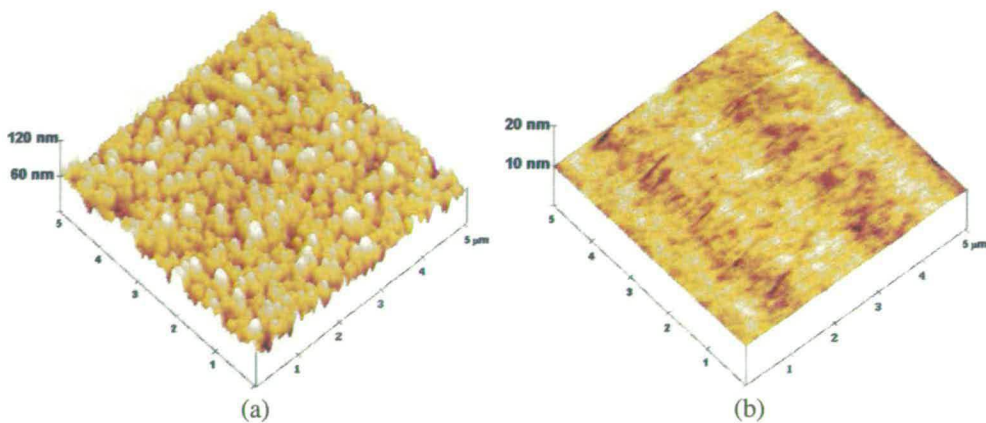
Figure 5.1: *AFM profiles of PECVD oxide film indicate that surface roughness can be reduced by CMP: (a) PECVD oxide film, and (b) after CMP process.*

5.2.3 Surface topography modification

5.2.3.1 Test structures for CMP planarisation

Prefabricated wafers typically possess severe topography which is not compatible with the wafer bonding process. Hence, test structures have been designed to evaluate the robustness

of the bonding process with respect to different surface topographies resulting from the underlying Al interconnect, together with variable oxide topography. These structures have been designed to mimic the extremes that might be observed in actual device wafers. Two CMP test structures have been used for this: a variable [179] and a uniform density layout, as shown in Fig. 5.2, were used for patterning both wafers with an oxide layer, and wafers with an Al layer which were then covered by oxide.

(a)   (b)
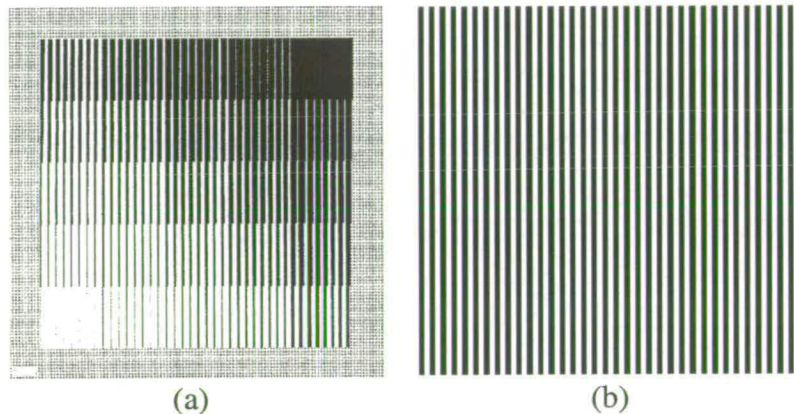
Figure 5.2: *Test structures for evaluating CMP planarisation capability: (a) variable density layout [179], and (b) uniform density layout.*

The variable density structure (Fig. 5.2(a)) provides a very severe test, with the chip surface globally sloping diagonally across the chip after CMP. In this test chip, the pattern density (the ratio of aluminium to the total area) ranges from 4% (lower left corner) to 100% (upper right corner), whilst the pitch of each of the metal (or oxide) stripes is a constant 250 μm. The chip contains a total of 25 structures (each 2×2 mm, consisting of 8 parallel lines) arranged in a 5×5 grid. Surrounding each test chip is a 1 mm border with a density of 25% which acts as a buffer, helping to isolate each test chip from the surrounding sites. The uniform density layout consists of 10 μm metal lines with a space of 10 μm, uniformly distributed across the whole test chip (Fig. 5.2(b)).

5.2.3.2   Experimental results

The effectiveness of the CMP planarisation process for the preparation of wafer bonding surfaces was evaluated using the test chip designs shown in Fig. 5.2, with the objective being to determine the effect of layout on bond strength. For the variable density mask patterned wafers, the polishing pressure applied on each structure is inversely proportional to the ratio of

the protruding area. The lower the density, the higher the local pressure, therefore, the higher the removal rate, so that the surface topography exerted a significant effect on the local polishing rate, as shown in Fig. 5.3. It should be noted that the CMP removal rates in Fig. 5.3 are not exactly inversely proportional to the pattern density, as the removal rate was significantly affected by the density of surrounding structures. As a result of the nonuniform polishing rate, a wedge-shaped surface was created across each chip, as shown in Fig. 5.4. This tends to decrease the contact area during bonding, therefore, potentially reducing the overall wafer bond strength.
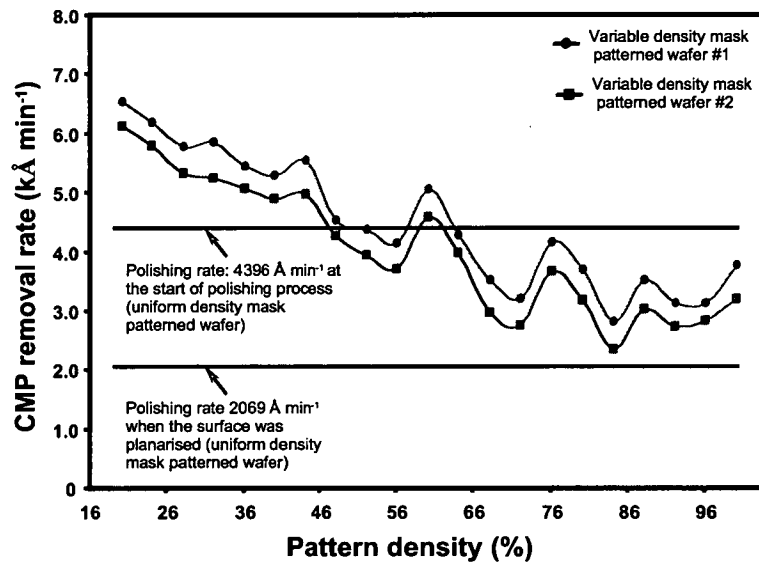
Figure 5.3: *CMP removal rate as a function of the pattern density.*

With the uniform density mask patterned wafers, a uniform polishing rate of 4395 Å min^{-1} was recorded at the start of the polishing process when 50% of the area contacted the polishing pad. The polishing rate then gradually reduced to 2069 Å min^{-1} as the surface became planarised, as shown in Fig. 5.3. The surface topography was simply reduced gradually by CMP and eventually became flat after 3 to 4 minutes, as shown in Fig. 5.5. It is well known [179], and confirmed here, that the distribution of pattern density plays a significant role during the polishing process. Hence, to obtain a flat wafer surface, dummy structures should be added during the design in order to achieve an uniform pattern density for CMP.
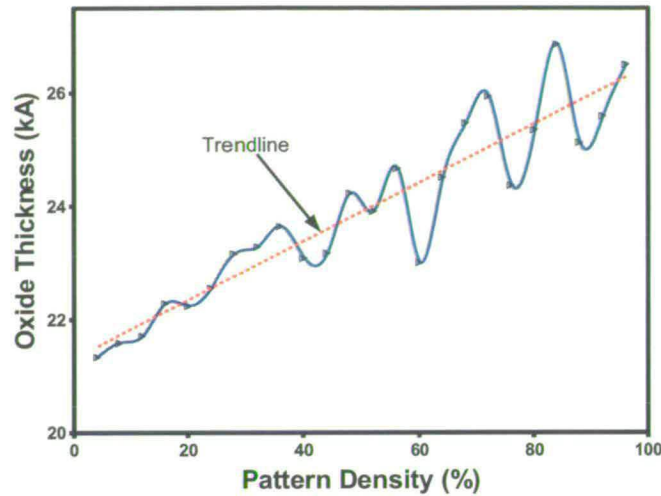
Figure 5.4: *Remaining oxide thicknesses as a function of pattern density. The wafer was patterned using the variable density test structure (Fig. 5.2(a)), with a 6-minute oxide polish.*

5.3 Plasma activated low temperature wafer bonding

5.3.1 Wafer bonding experiments

Four types of surfaces were evaluated for bonding: bare silicon, thermal oxide, PECVD oxide, and patterned aluminium covered with PECVD oxide. Each of the layers used for bonding were deposited/fabricated as follows:

1. The silicon surface used was that of a virgin wafer.

2. The thermal oxide was a 1.0 μm wet oxide, grown at 1100 °C.

3. The PECVD oxide was a 2.0 μm oxide layer, deposited using an STS Multiplex CVD system.

4. The patterned Al surfaces consisted of 1.0 μm aluminium layer, sputtered on a thermal oxide and patterned using a "variable" or "uniform" density test structure masks, as shown in Fig. 5.2. A 2.0 μm PECVD oxide layer was then deposited over the aluminium pattern.

It should be noted that all PECVD oxide deposited wafers were annealed at 435 °C for 16 hours to facilitate out-gassing and release of any residual film stress [93, 177]. CMP was then performed on all the PECVD oxide deposited wafers to reduce the surface topography and

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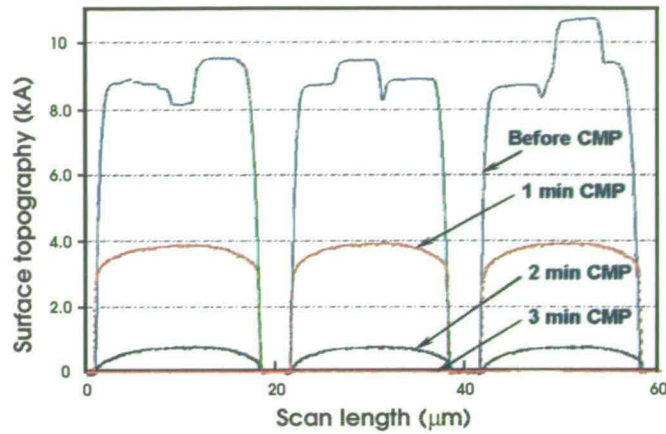
Figure 5.5: *Dektak surface profiles at different polishing times. The wafer was patterned using uniform density test structure (Fig. 5.2(b)).*

roughness. Table 5.5 shows the bonding experimental matrix and the abbreviated nomenclature of the bonded pairs.

Wafer No. 1	Wafer No. 2 Silicon	Wafer No. 2 PECVD Oxide
Thermal Oxide	Ox-Si	-
PECVD Oxide	POx-Si	POx-POx
Patterned Al	APOx-Si	APOx-POx

Table 5.5: *Wafer bonding experiments.*

Whilst smooth, particulate-free surfaces are a prerequisite for bonding, further treatment is essential before bringing the wafers in contact. All wafers were activated using a 1 minute O_2 (oxygen) plasma in a Vacutec RIE etcher. The 30 sccm gas flow resulted in a chamber pressure of 136 mTorr. The DC bias was set to -400 V using an RF power of 280-320 W. After the plasma treatment, the wafers were rinsed with DI water for 10 minutes and dried. The wafers were then bonded manually at room temperature and atmospheric pressure using a vacuum wand after the drying process. The bonded pairs were annealed at 200 °C for 16 hours to enhance the bond strength.

5.3.2 Interfacial voids inspection

The interfacial voids in the bonded pair were inspected using an infrared transmission imaging system equipped with a CCD camera (Hitachi KP-111). For the bonded wafer pair shown in Fig. 5.6, both of the bonding surfaces are polished PECVD oxide, but one of the wafer

has patterned Al films underneath the PECVD oxide which is patterned with either uniform density mask or variable density mask as described in Fig. 5.2. No void was observed in the uniform density mask patterned wafer pair. However, voids were occasionally observed from the variable density mask patterned wafer pairs caused by uneven bonding surface after the CMP process. It should be noted that the patterns observed in Fig. 5.6(b) were not necessarily caused by the voids. Indeed, they were mainly caused by the Al density variations. As Al is not transparent to infrared wavelength, the higher Al density regions are appeared darker than lower density regions in the IR transmission images.

(a)   (b)
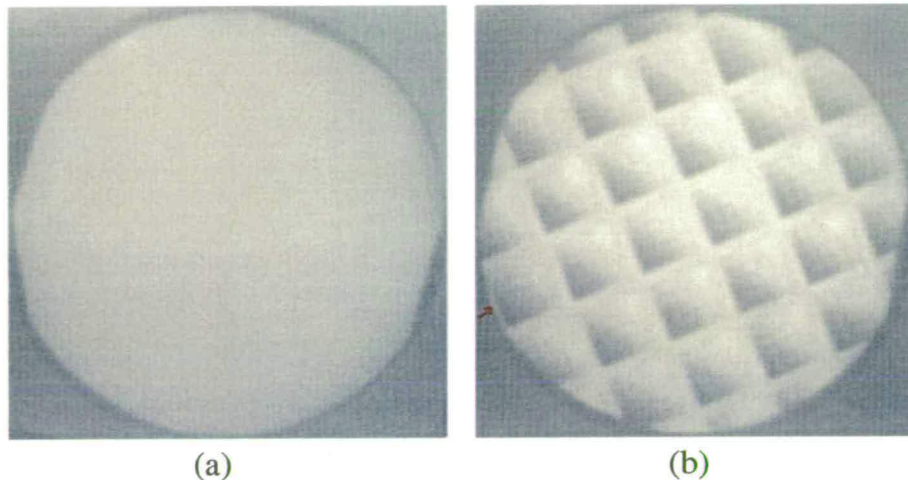
Figure 5.6: *Infrared transmission images of bonded wafer pairs. On one wafer, the Al film was patterned by (a) uniform density mask, and (b) variable density mask.*

5.3.3   Tensile testing

The quality of the bonded wafers were quantitatively evaluated using the tensile testing method. After the annealing process, bonded wafer pairs were sawn into 10×10 mm squares and attached to the sample handlers by epoxy adhesive. These samples were then loaded into an M30K tensile testing machine (LLOYD Instruments Ltd) for the bonding strength measurement. The M30K tensile machine can generate and record forces required to pull apart the bonded samples to a maximum of 30 KN, which results in a tensile strength up to 300 MPa. Whilst the reported tensile strength of bonded wafer is in the range of 5 - 30 MPa [111], it can be concluded that this system covers the required range of the measurement. The measurement results of O_2 plasma activated low temperature bonded samples were also compared with high temperature (1000 °C for 5 hours) annealed wafers, and the fracture point of a single silicon

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wafer. The fracture measurement results are presented in Fig. 5.7.
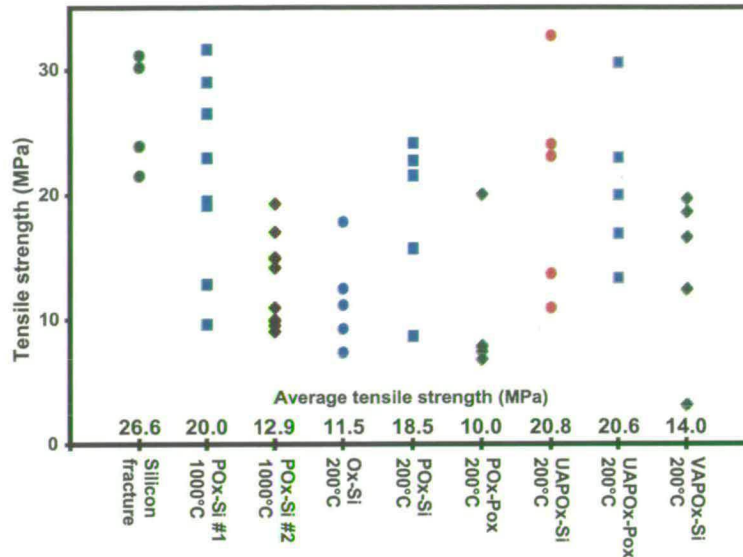
Figure 5.7: *Tensile strength measurement for evaluating bond quality. The abbreviations of the bonded pairs are detailed in Table 5.5. For patterned Al structures, "V" and "U" prepending the abbreviation "APOx" represent the use of "variable" or "uniform" density mask, respectively.*

The low temperature bonding results are distributed around 10 MPa, which is comparable with the high temperature annealed wafers. A large scatter of the measurements is observed in Fig. 5.7, which is typical in this type of bonding strength testing and is due to the brittleness of the materials used in the wafer bonding (also discussed in chapter 4.5.2.3). However, instead of the separation at the wafer bonding interface, it is often observed that the bulk silicon fractures as shown in Fig. 5.8 indicating that a strong bonding was actually achieved for the oxygen plasma assisted low temperature bonding.

It is also worth noting that relatively a high bonding strength was obtained for wedge-shaped wafers (variable density mask patterned), as shown in Fig. 5.7. This is probably because the CMP process tends to remove any sharp steps, producing a smoother surface. The successful bonding of wafers with aluminium tracks indicates the feasibility of integrating prefabricated MEMS and CMOS wafers through the use of CMP and low temperature bonding.
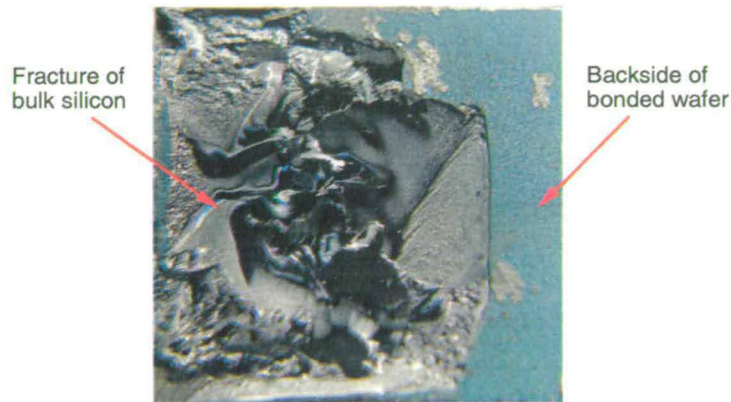
Figure 5.8: *Bulk silicon fractured during the tensile testing indicates a strong bonding at the wafer interface.*

5.4 Bonding and thinning of processed wafers

5.4.1 Fabrication sequence

Typical topography that might be experienced when bonding CMOS and MEMS wafers can be created using PECVD oxide covered wafers with a patterned Al layer underneath. A fabrication sequence was used to evaluate the feasibility of bonding and thinning processed wafers, using CMP and O_2 plasma assisted low temperature bonding processes described in previous sections, as shown in Fig. 5.9. The fabrication started with a 1.0 μm thermal oxide grown on both top and bottom wafers as an insulation layer (Fig. 5.9(a)). For the bottom wafer, a 2.2 μm PECVD oxide layer was deposited (Fig. 5.9(b)) and the rough surface was modified by a subsequent CMP step after the film densification process (Fig. 5.9(c)). It should be noted that the roughness of the deposited PECVD oxide in Fig 5.9 is somewhat magnified for viewing.

For the top wafer, a 1.0 μm Al layer was sputtered on an oxidised wafer (Fig. 5.9(d)) and then patterned using the uniform density layout presented in Fig. 5.9(b) to create a topography similar to one that might be resulted in from typical processed wafers. A 2.2 μm PECVD oxide was then deposited on the patterned Al layer, Fig. 5.1(e), and the wafer surface was then polished by an CMP process, as shown in Fig. 5.9(f). The two wafers brought together manually and bonded at room temperature, followed by a low temperature ($< 450\,^\circ$C) annealing process to increase the bond strength. It should be noted that the bottom wafer could also be prepared using the same fabrication sequence as the top wafer to result in a bonded pair with patterned Al structures on both wafers.
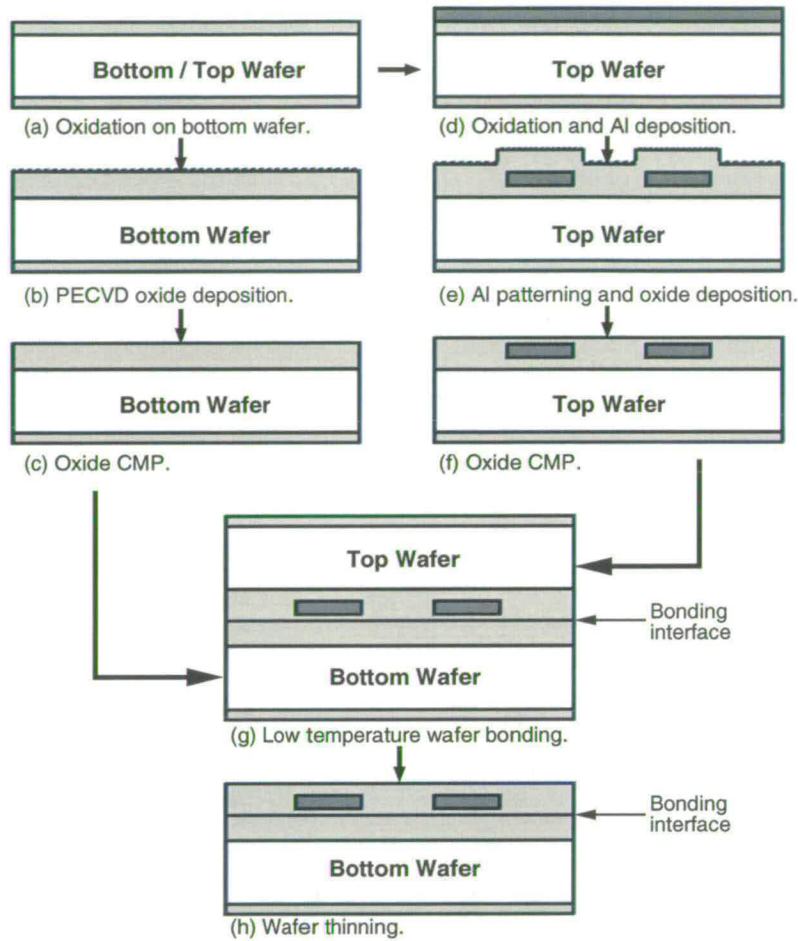
Figure 5.9: *Fabrication sequence for the feasibility study of bonding processed wafers.*

The unwanted silicon substrate can then be removed using a silicon etch (wet KOH etching or dry RIE etching) or wafer grinding. As a demonstration in Fig. 5.9(h), silicon dry etch processes (RIE ICP (inductively coupled plasma) or XeF_2 etchers) were used, with the thermal oxide layer on top wafer acting as an etch-stop. The wafer thinning process served for two purposes: (1) to verify whether the bonding strength is sufficient to sustain the subsequent fabrication processes in CMOS-MEMS integration, and (2) to facilitate the fabrication of interconnect between bonded wafers.

5.4.2 Experimental results

The bonding and thinning of processed wafers using CMP and O_2 plasma assisted bonding has been demonstrated, and Fig. 5.10 shows the successful thinning of bonded wafers, both

covered with PECVD oxide with patterned Al test structures underneath. The result indicates that the strength of low temperature bonding potentially meets the requirements for subsequent integration processing, and also confirms the feasibility of integrating prefabricated CMOS and MEMS wafers using CMP, low temperature bonding and thinning.

<div align="center">(a)   (b)</div>
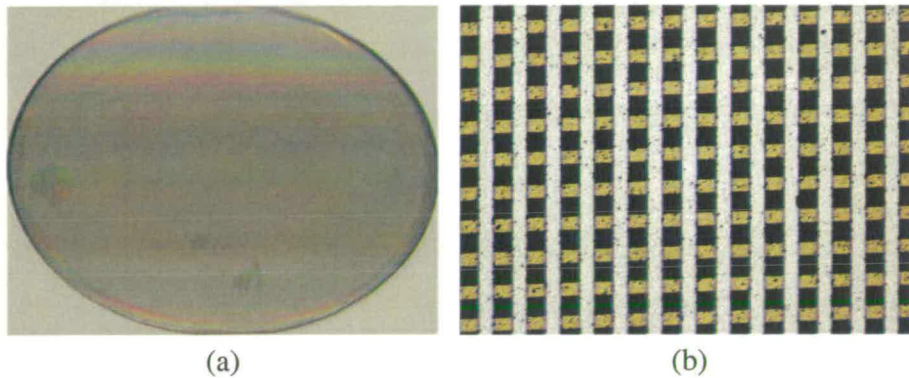
Figure 5.10: *Images of the bonded wafers after the thinning process. (a) thinned wafer, and (b) close-up view of uniform density Al structure with planarised PECVD oxide. The vertical and horizontal lines are Al on the top and bottom wafers, respectively.*

5.5 Conclusions

PECVD oxide has been selected as a top surface layer for both CMOS and MEMS wafers because its surface properties are suitable for direct wafer bonding, and also it has a low deposition (300 °C) and annealing (less than 450 °C) temperatures. In addition, the high frequency deposition process was chosen due to the low film stress that can be achieved after the deposition and densification steps. The surface roughness of PECVD oxide (2.8 nm) can be significantly reduced to less than 0.5 nm through the use of the CMP process. Challenging topography can also be modified using CMP to levels compatible with wafer bonding. Experimentation indicates that the strength of low temperature (200 °C) wafer bonding, when assisted by an oxygen plasma, is comparable with the high temperature (1000 °C) fusion bonding. Finally, the successful bonding and thinning of wafers with patterned Al indicates that the integration of prefabricated CMOS and MEMS wafers is possible, using CMP and low temperature bonding.

Chapter 6
Inter-Wafer Connection — Part I:
Interconnect After Bonding

6.1 Introduction

The provision of electrical interconnects between bonded MEMS and CMOS wafers is a key step of this new integration approach, and two inter-wafer connection approaches are evaluated in this thesis. In the first approach, processed wafers are aligned and bonded using PECVD oxide as a direct bonding material. Interconnects between wafers are then established through specifically designed contact vias using a standard multilevel metallisation process. In this chapter, the fabrication sequence and test structures to characterise this interconnection scheme are introduced. Wafer bond aligning procedure and inspection approaches are described. Finally, the fabrication results together with the electrical measurements are presented.

The second inter-wafer connection approach, which uses direct metal contact at the wafer bonding stage to provide interconnections between the MEMS and CMOS wafers, will be discussed in chapter 8.

6.2 Fabrication sequence and test structures

6.2.1 Contact via structure and its fabrication sequence

The fabrication sequence of the "wafer bonding first and electrically connecting afterwards" approach is shown in Fig. 6.1. In this method, Al tracks on both top and bottom wafers are patterned and then covered with PECVD oxide, which is then polished to provide a smooth and flat surfaces, as illustrated in Fig. 6.1(a)-(d). The processed wafers are aligned and bonded using PECVD oxide as a direct bonding material (Fig. 6.1(e)). Following wafer thinning and patterning of the uppermost oxide layer, the oxide layers between these Al tracks on the top and bottom wafers are dry etched, as shown in Fig. 6.1(f) and (g). Interconnect between wafers

is then established through the vias, using a standard Al sputtering process (Fig. 6.1(h)). The fabrication process is completed with an Al CMP which defines the contact via structure and also the probe pads, as shown in Fig. 6.1(i). Since only oxide layers are presented at the bonding interface, this process is referred to as oxide bonding in this thesis.
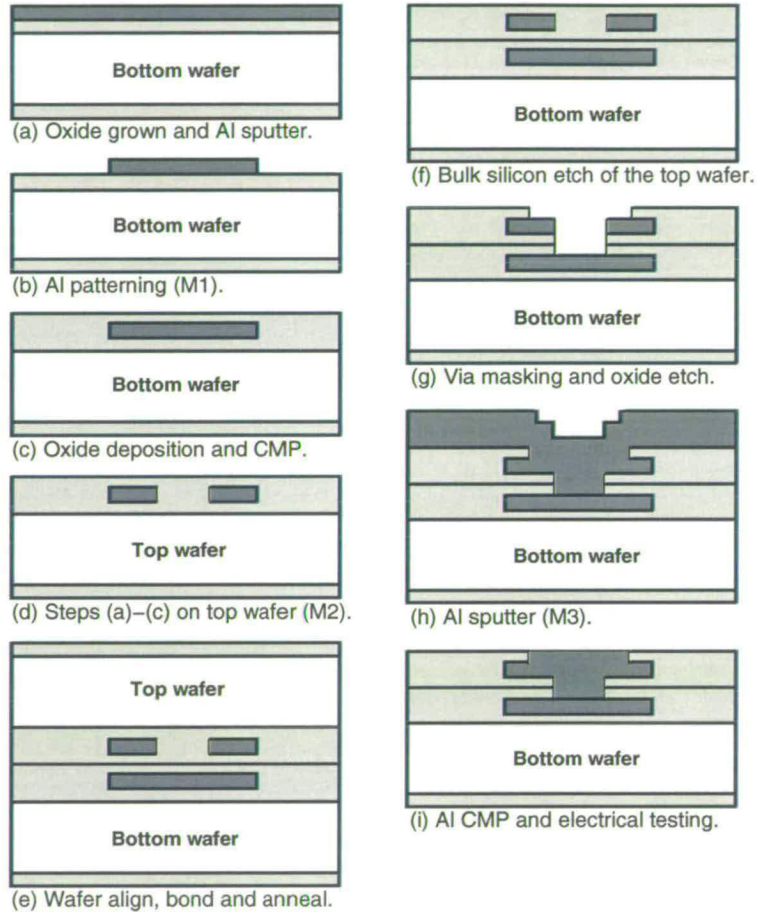
Figure 6.1: *Fabrication sequence of the oxide bonding approach: an interconnection scheme which connects prefabricated wafers electrically after the bonding process.*

6.2.2 Contact via structure for the inter-wafer connections

It should be pointed out that a contact via structure has been specifically designed to connect two processed wafers after the bonding process, as shown in Fig. 6.1 and 6.2. In this design, a doughnut-shaped metal structure is used for the metal contact on the top wafer, doubling up as a hard mask which defines the inter-wafer via, as shown in Fig. 6.2(f). After thinning the top wafer, an oxide window is etched which is several microns larger than the inter-wafer via.

Once the oxide above the top metal layer is removed, the dry etch can be continued until the bottom metal layer is exposed (Fig. 6.2(g)). A metal deposition is then performed to connect the metal layers on both wafers (Fig. 6.2(h) and (i)).
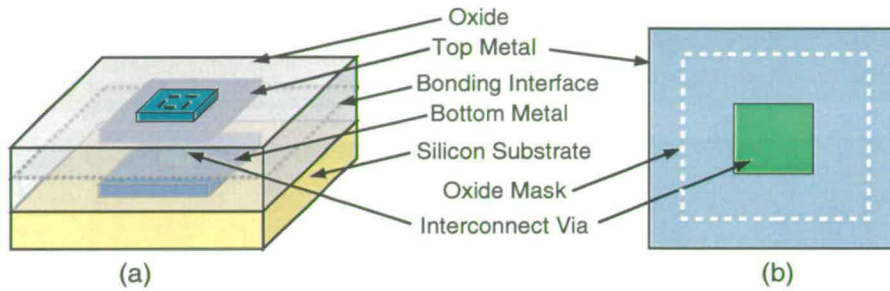
Figure 6.2: *Self-aligned contact via structure for electrically connecting two bonded wafers.*

6.2.3 Test structures for electrical characterisation

A set of test structures based on Kelvin and contact chain designs [176] have been used to evaluate the potential interconnect architectures between two bonded wafers. These include an in-built tolerance to wafer bonding misalignments, in order to obtain a constant contact area and to ensure that continuity measurements do not fail through registration problems. Single contact vias and via chain test structures with via dimensions of 5, 7, 10, 14 and 20 μm have been included on the test chip to evaluate the above approach, as shown in Fig. 6.3.
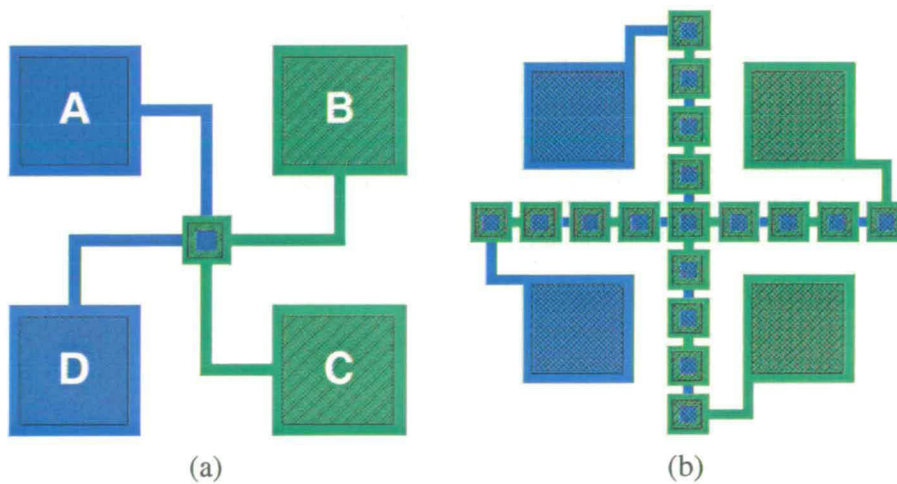
Figure 6.3: *Layout of the test structures for characterisation of the inter-wafer connection process: (a) single via structure and (b) via chain structure.*

6.3 Wafer bonding alignment

When MEMS and CMOS components are fabricated on separate wafers, they must be aligned to form a functional device. Therefore, wafer alignment must be undertaken as part of the bonding process to produce working test structures.

6.3.1 Alignment procedure for wafer bonding

In order to align wafers, the alignment marks specifically designed for this purpose must be presented on all wafers. For the top wafer, the alignment marks on the front side are sufficient for the process. However, they must be located in specific regions[1] because the bottom alignment microscopes in the Karl Suss MA8 aligner can only travel a limited distance (6 mm), and the viewing windows of the bottom bonding chuck also restricts the location of the alignment marks. For the bottom wafer, alignment marks on both sides of the wafer are required, as shown in Fig. 6.4(a).

Once the wafers are prepared, the top wafer is loaded on the top bonding chuck with front side face down. The alignment marks on the wafer frontside are identified by the bottom optical microscopy lenses and the images are locked and stored in the aligner, as shown in Fig. 6.4(b). The second wafer is then loaded on the bottom bonding chuck with the alignment marks on the backside of the wafer being used to align to the stored image of the alignment marks of the top wafer, which enables the front-to-front wafer bonding, shown in Fig. 6.4(c). The key to this alignment process is the storage of the position of the alignment marks on the top wafer, since only the backside alignment marks on bottom wafer can be detected during the alignment operation.

6.3.2 Alignment accuracy and inspection

The integration process examined in this thesis involves aligning and bonding of two processed wafers using a double sided aligner. To monitor the alignment accuracy a vernier structure as shown in Fig. 11 was designed. Since wafer bonding misalignment with a commercially available aligner is typically 1-2 μm, this vernier structure was designed with a rather conservative

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[1] At least two alignment marks are required, and both of them have located in the middle of the wafer with a separation of 60 mm, as shown in Fig. 6.6. It should also be noted that these two alignment marks do not need to be in these exact spots. They can have a vertical variation of 9.5 mm and horizontal variation 2.5 mm.
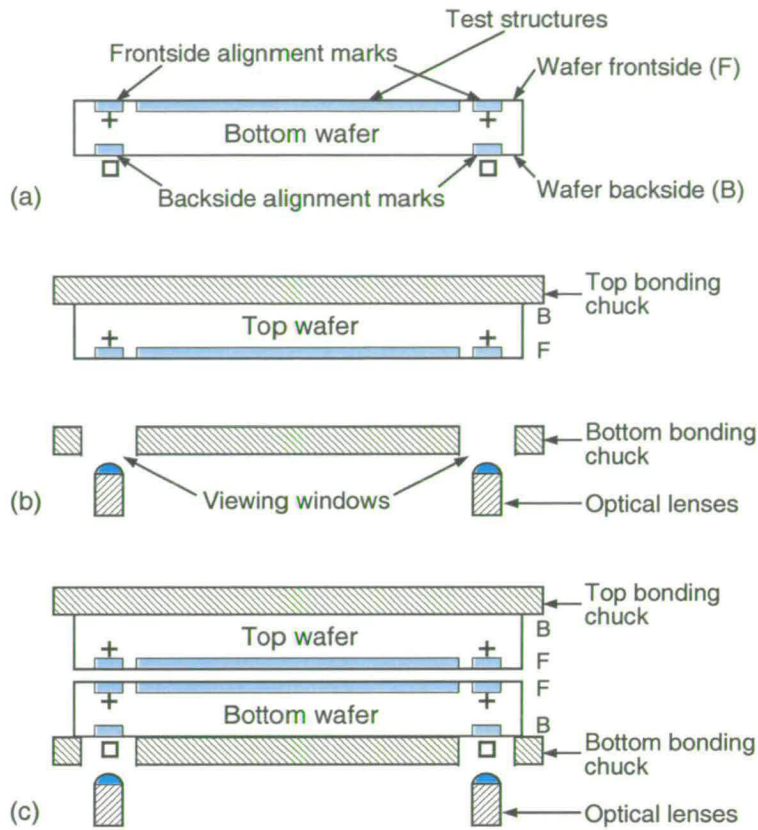
Figure 6.4: *Schematic of a typical wafer bonding alignment process.*

measurement range from 0.5 to 9.0 μm. Based upon the results obtained, future designs would have a smaller measurement range and higher resolution.

The inspection of alignment accuracy can be performed using a normal optical microscope after the wafer thinning process (Fig. 6.5(a)), or an IR microscope in the aligner, as shown in Fig. 6.5(b). Although the IR images are not as clear as with the white light microscope, a misalignment of 0.5 μm can still be discerned, providing the opportunity of inspecting immediately after the wafer contact, which has the advantage that wafer separation can be undertaken without damage. The alignment accuracy measurement results are shown in Table 6.1. Although, occasionally, large misalignment did occur (e.g. bonding test No. 5 in Table 6.1), alignment accuracies of 2 μm were typically achieved using a Karl Suss MA8 aligner.
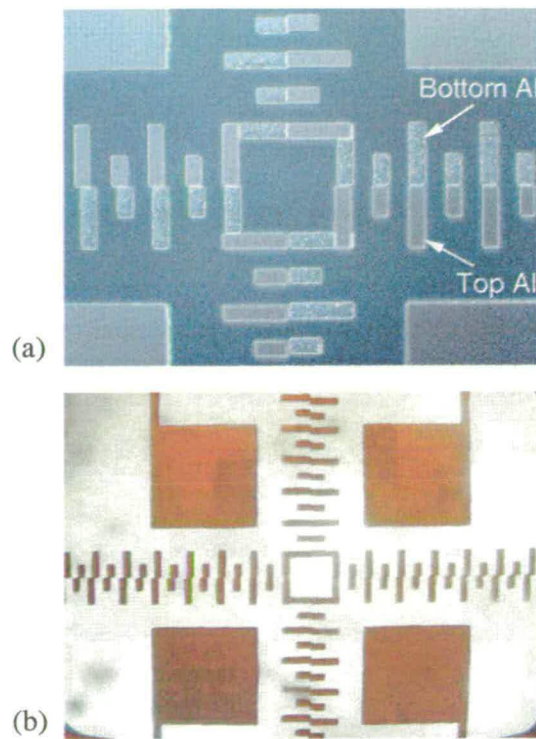
Figure 6.5: *Alignment accuracy inspection using a vernier structure (a) through normal white light microscope after wafer thinning process and, (b) IR microscope before wafer thinning.*

6.4   Integration of prefabricated wafers

6.4.1   Wafer bonding and thinning

A successful thinned oxide bonded wafer pair with patterned Al structures embedded in the oxide is shown Fig. 6.6, using the alignment procedure presented in previous section and bonding and thinning processes described in chapter 5. Two sets of alignment marks detailed in Fig. 6.6 were used for the wafer bonding alignment using a Karl Suss MA8 double sided aligner, which were also used as global alignment marks for the frontside lithography process using a $5\times$ Optimetrix stepper. It can be observed that no void induced delamination occurs in the centre part of wafer, which indicates that the wafer alignment process does not introduce any undesirable particulates at the bonding interface. However, delamination of the top device layer at the wafer edge areas was observed after the thinning process due to the poor bonding in this region. This poorer bonding at the wafer edge was attributed to the wafer handling by metal tweezer which degrades the wafer surface and creates particles. Another possible source of this problem might be due to the non-uniform film deposition rate and polishing rate at the

Wafer No.	Left region (x, y) in μm	Right region (x, y) in μm
1	(-0.5, -0.5)	(-0.5, -2.0)
2	(-0.5, 1.0)	(1.0, 0.5)
3	(-1.0, 1.0)	(-1.0, 0)
4	(0.5, 0)	(2.0, -0.5)
5	(1.5, 7.0)	(-1.0, -4.0)
6	(2.0, 2.0)	(2.0, 1.0)
7	(-0.5, 2.0)	(-1.0, -1.0)
8	(-1.5, -0.5)	(1.0, -1.0)
9	(1.0, 0)	(-1.0, -1.0)

Table 6.1: *Bonding misalignment measured on wafers bonded on a Karl Suss (MA8) aligner.*

wafer edge.

Fig. 6.7 shows a successfully thinned oxide bonded wafer patterned with the test structures presented in Fig. 6.3. This confirms that low temperature bonding of pre-fabricated MEMS and CMOS wafers using CMP, wafer bonding and thinning is a viable integration technology.

Global
alignment
marks
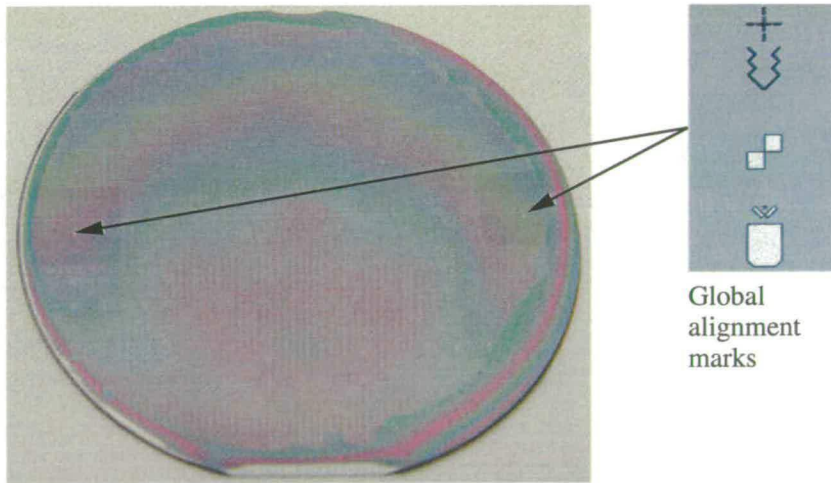
Figure 6.6: *Photograph of bonded wafers after the thinning process together with the alignment marks.*

(a)   (b)
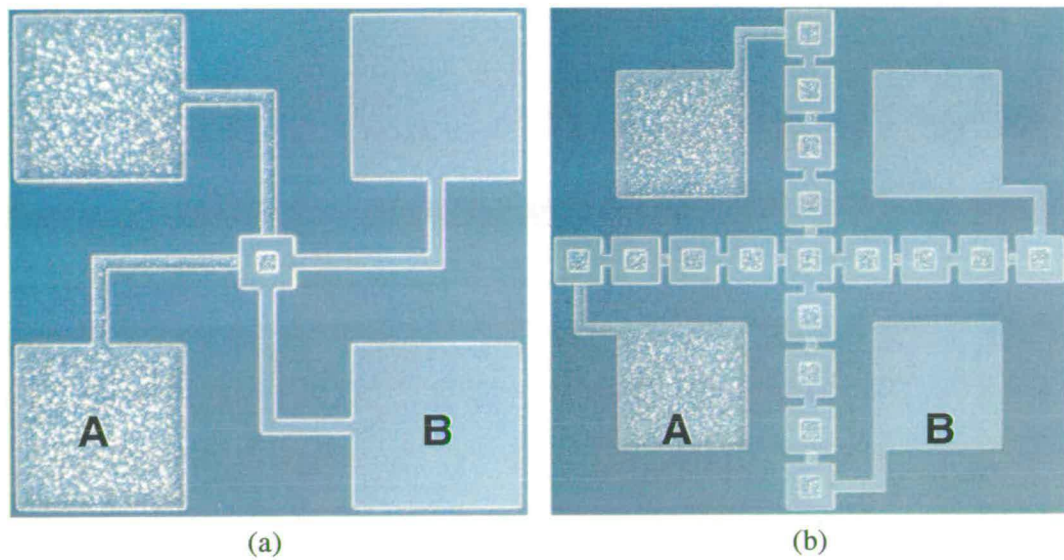
Figure 6.7: *Microscope images of (a) single contact via structure (b) contact via chain structure after the wafer thinning process. A and B represent the Al structures on top and bottom wafers, respectively.*

6.4.2 Metallisation

An oxide to oxide bonded wafer pair can be treated as a single wafer after the removal of the silicon substrate of the handle wafer. This enables contact via lithography to be performed, followed by an oxide etch to expose both top and bottom metals (see process flow in Fig. 6.1). Before Al deposition, an argon milling step was implemented in order to remove any Al_2O_3 and surface contaminations resulting from exposure to the atmosphere. Al was then sputtered without breaking vacuum to electrically connect both wafers. The probe pads are defined by the final Al CMP process, as shown in Fig. 6.8 and Fig. 6.9.

Figure 6.8(d) indicates that there are some issues with the contact via etch and filling during the fabrication of this interconnect structure. Although electrical connection between bonded wafers was established, the first attempt of this approach left significant opportunities for improvement. The main issue was that an approximately 4.0 μm oxide has to be etched at the contact via to expose the bottom metal layer, and 1.5 μm of photoresist SPR350 was unable to survive such a long etch. This resulted in an undesirable oxide loss, leading to the Al protruding out of the oxide surface, as shown in Fig. 6.8(a) compared to the desirable cross-section in Fig. 6.1(g). Hence, after a blanket Al deposition (Fig. 6.8(b)), an over-polish of the top metal is
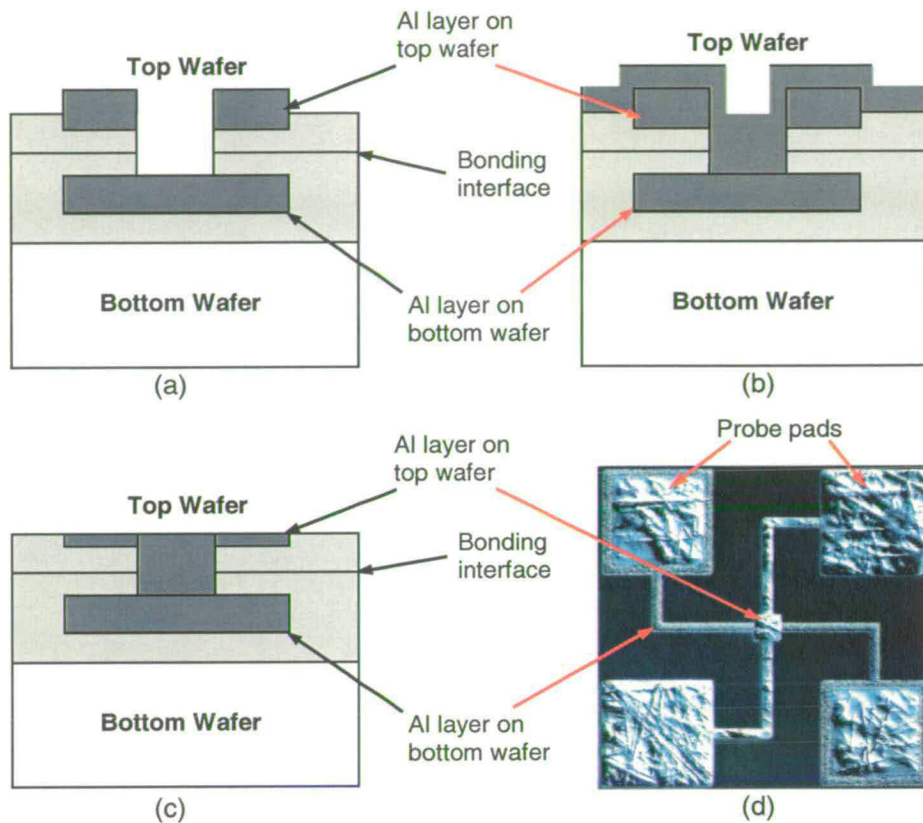
Figure 6.8: *A contact via structure after Al metallisation process (the first attempt): (a) after contact via etch, (b) blanket Al deposition, (c) Al CMP to define the top metal layer, and (d) microscopy image of a fabricated test structure (top view).*

required to pattern the devices, as shown in Fig. 6.8(c). As the targeted top metal thickness was less than 0.3 μm and no stop layer was available, the final Al CMP had only a small process margin and was difficult to control. The rough Al surface of the fabricated device shown in Fig. 6.8(d) was due to the Al CMP process which used high down force to achieve a fast Al polishing rate. The scratches generated on the Al surface can be removed by a more gentle CMP process[2]. However, the additional process was not performed because of the thin Al top layer.

Following this initial process, a second batch used a thick photoresist (SPR2-20, 7 μm) to pattern the contact via. As a result, the uppermost oxide layer was kept intact during the via etch, and served as an Al CMP stop layer because of a high selectivity between oxide and Al. Fig. 6.9 shows a fabricated Kelvin test structure after the final Al CMP process.

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[2]Detailed discussion about this issue can be found in chapter 8 (section 8.3.1.1).
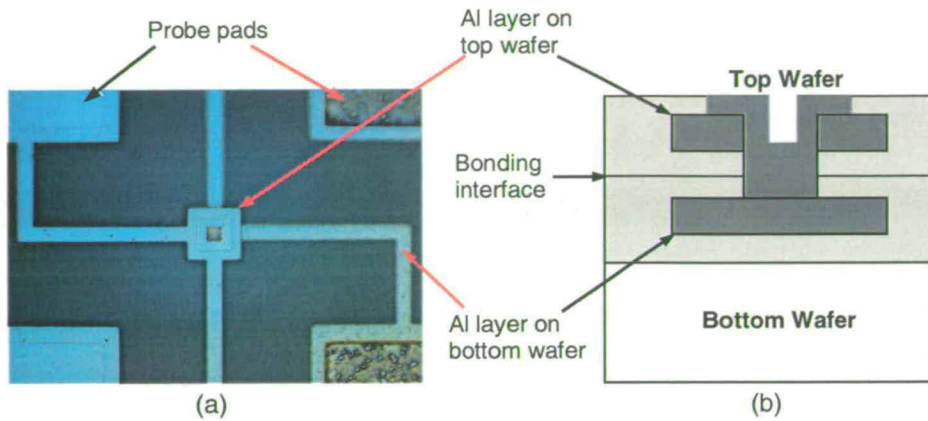
Figure 6.9: *A contact via structure after Al metallisation process (the second batch): (a) microscopy image of a fabricated test structure (top view), and (b) schematic of the fabricated test structure (cross-section view).*

The smallest via size available from the mask was 5 μm, but smaller via size can be used. From this method, the oxide stack can be designed as thin as 2.5 μm (i.e. Al top layer: 1.0 μm, oxide between top and bottom Al layers: 1.0 μm and uppermost oxide layer: 0.5 μm). Assuming a 10:1 aspect ratio via etch and filling technology [28, 30], a minimum via size of 0.25 μm should be achievable. However, a minimum of 2.0 μm wafer bonding accuracy is typically available. Therefore, it can be concluded that wafer bonding misalignment is the limitation of this approach if a high interconnect density is to be achieved.

6.5 Electrical characterisation

Measurements on via chain test structures were performed using a HP4156B semiconductor parameter analyser and the results summarised in Table 6.2 (based on the electrical measurements on 12 different locations on a processed wafer), confirming the electrical continuity of the chain structures and the good quality of oxide bonding across the measured areas. It should be noted that the measurements in table 6.2 include the resistance of probes and Al tracks.

Measurements have also been made on the Kelvin contact via test structures, using a HP4062B and a Solartron 7065 voltmeter, by forcing a current of 10 mA from the top to bottom metal and measuring the voltage drop across the via. The results are presented in Fig. 6.10. Assuming the contact area is defined by the via dimensions of the bottom wafer, these results indicate that the contact resistance is in the order of 1.7×10^{-8} $\Omega \cdot$cm^2 (from the second batch). It should be

Via chain	Via size (μm)	20	14	10	7	5
test structure	Via number	9	11	11	11	13
First	Resistance (Ω)	7.19	8.67	7.84	8.32	9.29
batch	STDEV (Ω)	0.39	0.64	0.60	1.27	2.41
Second	Resistance (Ω)	3.82	4.16	4.26	4.30	5.15
batch	STDEV (Ω)	0.09	0.07	0.07	0.08	0.25

Table 6.2: *Resistance measurement of the via chain structures.*

noted that the contact resistance from the second batch are lower with smaller variations than those from the first batch which can be largely explained by an Al sintering step being added to improve the Al-Al contact, and improved fabrication steps being used for the contact via etch and Al CMP (Fig. 6.8 and Fig. 6.9).
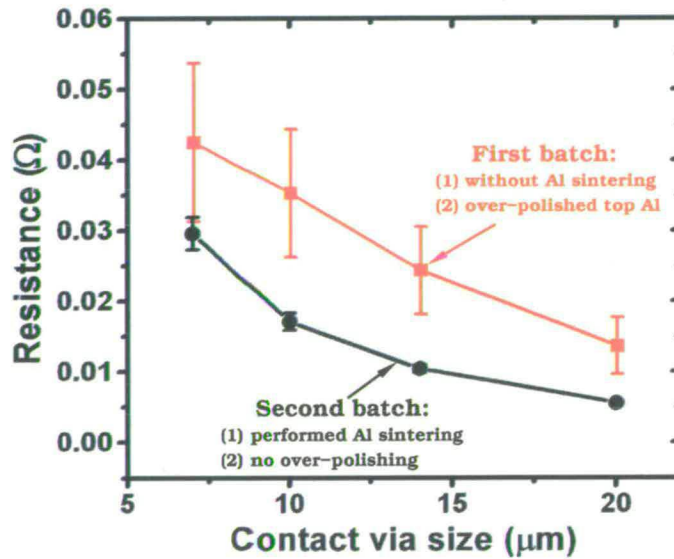
Figure 6.10: *Resistance of vias as a function of size. The differences between first and second batches are: (1) Al sintering process for improving the Al-Al contact, and (2) the fabrication of top Al layer.*

It also worth noting that this connection scheme actually consists of two contacts in series (Fig. 6.9(b)). Hence, it is clear that the actual contact resistance between the top and bottom Al layers is not extracted with this structure. In addition the measurement is also affected by the collar region around the contacts being 12 μm, which was set to ensure any wafer to wafer misalignment did not cause failure of the via. This also introduces more uncertainty into the measurement. Clearly, to rigorously characterise contact resistance, it is necessary to design two structures which directly measure M1-M3 and M2-M3 contact resistances.

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6.6 Conclusions

Test structures have been used to study the feasibility of bonding MEMS and CMOS wafers to create an integrated system with electrical connections. Inter-wafer connections can be achieved using an oxide bonding approach. Resistances of 3.8 - 5.2 Ω have been obtained for the via chain test structures, whilst an average specific contact resistivity of 1.7×10^{-8} $\Omega \cdot cm^2$ has been extracted from the single via structure.

Chapter 7
Contact Resistance Measurement

7.1 Introduction

Electrical interconnects between wafers can be fabricated using a low temperature wafer bonding process for integrating MEMS and CMOS devices [55, 176] and the construction of three-dimensional ICs [152, 155, 180, 181]. Low contact resistivity (ρ_c) is desirable for all applications. Therefore, appropriate test structures for the ρ_c measurement are essential for developing and optimising different fabrication technologies.

This chapter presents test structures to characterise the electrical interconnects between bonded wafers. Two types of test structures (Kelvin and stacked Greek cross) have been fabricated using a two-level aluminium metallisation process. These two structures have also been evaluated using a numerical interconnect simulation software, and the simulation results compared with electrical measurements.

7.2 Test structures and associated fabrication sequences

The Kelvin test structure [182–184] and stacked Greek cross structure [185] have been considered as candidates for measuring the contact resistivity between two metal layers connected by the wafer bonding process.

7.2.1 Cross-bridge Kelvin test structures

7.2.1.1 Ideal Kelvin structure

An ideal Kelvin structure consists of two L-shaped conductive lines (with line-width of w) in both the upper and lower layers. When these layers are perfectly aligned, they form a contact area of A_c ($A_c = w^2$), as illustrated in Fig. 7.1. The contact resistance is determined by forcing a current from arm A to C (I_{AC}) and measuring the potential difference between D and B (V_{DB}).

Then the current is reversed (I_{CA}) and the potential V_{BD} is measured:

$$R_{0°} = \frac{V_{DB} - V_{BD}}{I_{AC} - I_{CA}} \tag{7.1}$$

The current is then forced between B and C and the process repeated:

$$R_{90°} = \frac{V_{AD} - V_{DA}}{I_{CB} - I_{BC}} \tag{7.2}$$

The average resistance of these two measurements is calculated

$$R_c = \frac{R_{0°} + R_{90°}}{2} \tag{7.3}$$

and the contact resistivity derived:

$$\rho_c = R_c \times A_c \tag{7.4}$$

The accurate extraction of ρ_c depends upon the contact area A_c being known precisely. However, the contact area, A_c, which relies on the overlay of upper and lower layers, can not be controlled perfectly because undesirable misalignment will always be present during the lithography step, and the value of this misalignment constantly changes from die to die and wafer to wafer due to its random nature.
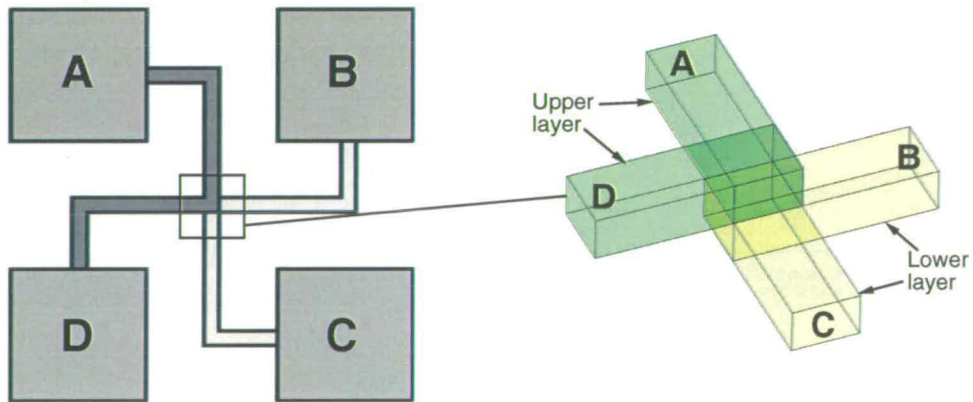
Figure 7.1: *Layout and 3-D image of an ideal Kelvin structure for electrically characterising of the metal interconnects.*

7.2.1.2 L-shape and D-shape Kelvin structures

In order to maintain a constant contact area, the basic Kelvin test structure has been modified to minimise the inevitable misalignment problem from the lithography process [183, 184], as

shown in Fig. 7.2. In these structures, upper and lower layers are larger than the via, as for standard contacts/vias in integrated circuits. Since the contact between the upper and lower structures is through the via, the contact area is defined by the via regardless of the misalignment during the lithography steps. This obviously assumes that the collar width (δ) is sufficiently large to ensure that the via does overlap with both upper and lower conductors. This can be satisfied by choosing the width of the collar to be greater than the expected maximum misalignment. Depending on the arm width and the via size of the test structure, modified Kelvin structures can be categorised into L-shape and D-shape, as shown in Fig. 7.2.
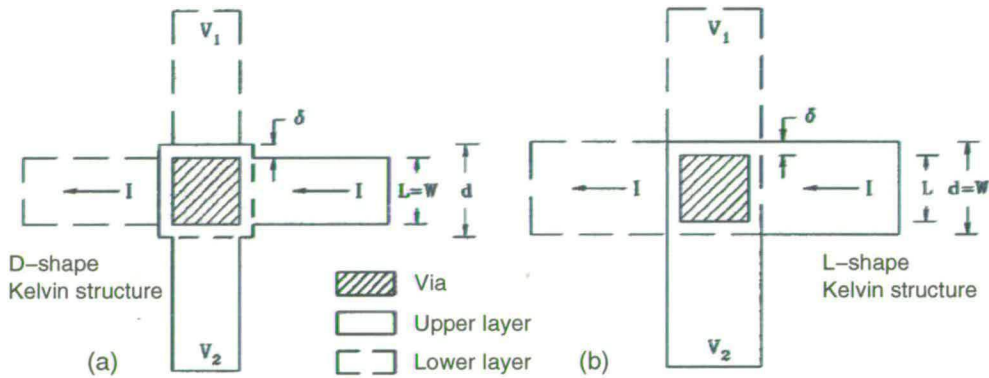
Figure 7.2: *The Kelvin structures for measuring the specific contact resistance between two metal layers [186]: (a) D-shape Kelvin structure, and (b) L-shape Kelvin structure.*

The addition of collars solves the misalignment issue during the fabrication, but, it causes lateral current spreading in the structure during the electrical measurement [187, 188]. Fortunately, these errors can be calculated through simulations and the universal error correction curves are available in literature [186, 189–192]. Another issue with the L-shape and D-shape Kelvin structures is that the contact area is defined by the via dimension, which is not so simple to define in wafer bonding processes.

7.2.2 Stacked Greek cross test structure

7.2.2.1 Stacked Greek cross structure

To overcome the misalignment problem of the ideal Kelvin structure and the difficulties of fabricating L-shape and D-shape Kelvin structures in the wafer bonding process, a test structure, which will be termed as stacked Greek cross structure, has previously been proposed [185], and is illustrated in Fig. 7.3. The fabrication sequence of the stacked Greek cross structure is

suitable for the wafer bonding process [176]. However, it should be noted that the current flow in this structure is different from the Kelvin contact resistance test structure, so it is not valid to extract the contact resistance in a similar manner to the Kelvin structure.
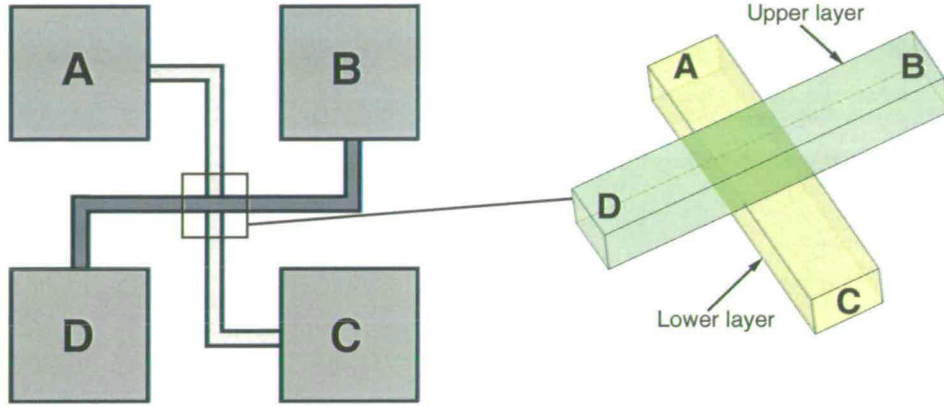
Figure 7.3: *Layout and 3-D image of a stacked Greek cross structure for electrically charac-terising of the metal contacts.*

In this structure, two metal lines (with line-width of w) are perpendicular to each other and placed one after another to create a contact area of A_c ($A_c=w^2$). If the two tracks are orthog-onal, which can normally be satisfied, the resulting contact area A_c is a constant regardless of the lateral and vertical misalignments. When measuring this test structure, the "contact resis-tance" is determined by forcing a current from pad A to B (I_{AB}) and measuring the potential difference between C and D (V_{CD}). After that the current is reversed (I_{BA}) and the potential V_{DC} is measured and the specific contact resistance extracted:

$$R_{0°} = \frac{V_{CD} - V_{DC}}{I_{AB} - I_{BA}} \tag{7.5}$$

The current is then forced between B and D and the process repeated:

$$R_{90°} = \frac{V_{AC} - V_{CA}}{I_{BD} - I_{DB}} \tag{7.6}$$

The average resistance of these two measurements can be calculated using equation (7.3) and the ρ_c derived using equation (7.4).

However, the forced current has to turn 90° when it passes from one metal layer to another through the contact interface as shown in Fig. 7.3. This current path causes current crowding at the corner of the contact region, which results in a nonuniform current distribution at the contact interface. Hence, this test structure will not give the same contact resistance measurement as

the Kelvin structure. Therefore, the ability of this structure to evaluate the contact resistivity requires further study. One observation is that the measurement bears more similarities to a Greek cross sheet resistivity measurement, hence it is referred to as the stacked Greek cross structure in this thesis.

7.3 Fabrication and measurement of the test structures

7.3.1 Fabrication of the test structures

A two-level Al metallisation process associated with a CMP enabled thick Al lift-off technique was used to fabricate the above test structures, as illustrated in Fig. 7.4. The reasons for using an Al metallisation process to mimic the bonding process for the test structures evaluation are: (1) the multi-level Al metallisation process is a well-studied mature process which is consistent and controllable, and (2) the resulting ρ_c mainly depends on the fabrication conditions.

A standard Al damascene process is used to create the bottom metal tracks and a planar wafer surface, Fig. 7.4(a). The following lithography step defines contact vias and the patterned photoresist is used as a shadow mask for the subsequent Al deposition, as shown in Fig. 7.4(b). The top Al layer (1.0 to 1.5 μm) is then deposited (Fig. 7.4(c)) and followed by Al CMP (Fig. 7.4(d)). The Al CMP is completed when the Al thickness on top of photoresist becomes thin enough (0.2 μm) for the lift-off process to work. Assisted by megasonic agitation, the photoresist dissolves in the acetone solvent, and the thin Al film on top of the photoresist breaks into small pieces and is carried away by acetone, as shown in Fig. 7.4(e). The fabrication process finishes with a DI water rinse (15 minutes) and wafer drying.

The use of the lift-off process to define top Al tracks avoids undesirable overetch of the bottom Al or oxide layer. Otherwise, after the damascene process of the bottom Al tracks (Fig. 7.4(a)), either top Al layer deposition and Al patterning can be performed, which would result in an undesirable overetch of bottom Al; or PECVD oxide deposition and oxide patterning can be performed, which would result in an unwanted overetch of oxide. The high etch selectivity of photoresist with both Al and oxide eliminates these overetch problems.
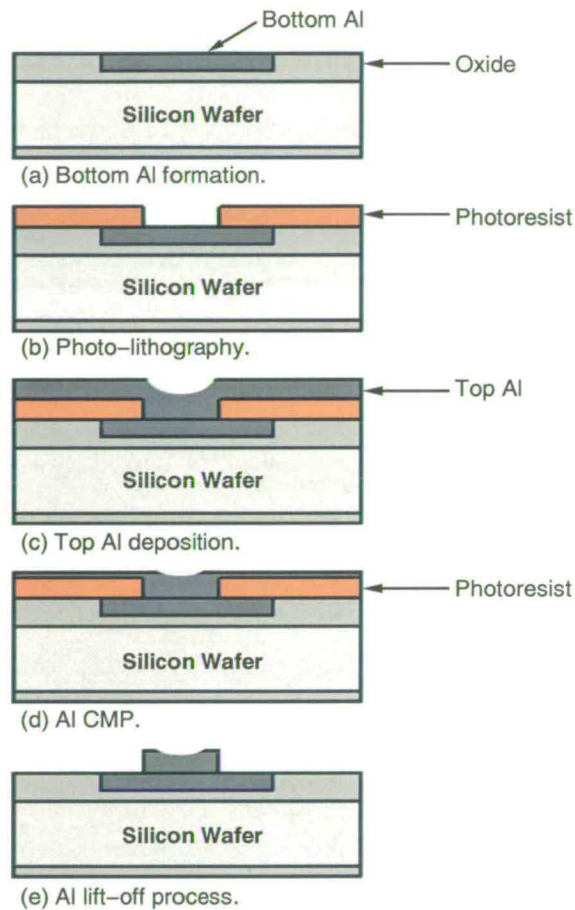
Figure 7.4: *Two-level Al metallisation process for the fabrication of Kelvin structures and stacked Greek cross structures. Damascene process was used for the bottom Al layer formation and lift-off process was used for the top Al patterning.*

7.3.2 Fabrication results

Fig. 7.5 shows a D-shape Kelvin structure and a stacked Greek cross structure after the lift-off step using the two-level Al metallisation process described in Fig. 7.4. The difficulty of this fabrication sequence is related to the ability of Al lift-off. In order to make this lift-off process work, the thickness of Al on top of the photoresist must be reduced to less than half micron. The challenge is then to reduce the thickness of the Al layer without degrading the soft photoresist underneath it. A delicate low-down-force and high-rotation-speed Al CMP has been developed for reducing the thickness of the Al layer at a reasonable polishing rate, while keeping the underlying photoresist intact. Parameters used for this critical Al CMP process are given in Table 7.1. Once the thickness of top Al is reduced to ~ 0.5 μm, lift-off becomes relatively straightforward by using acetone and megasonic agitation. The successful fabrication

of the Kelvin and stacked Greek cross structures made the comparison of these two types of test structures possible.

Parameter	Setting
Head speed	55 revolutions per minute (rpm)
Table speed	25 revolutions per minute (rpm)
Head pressure	0.15 bar
Back pressure	0.07 bar
Slurry flow	150 ml/min
Temperature	Room temperature
Pad	Rodel IC1400
Slurry	PL 1609

Table 7.1: *Process variables and consumables settings for Al damascene process.*

(a)   (b)
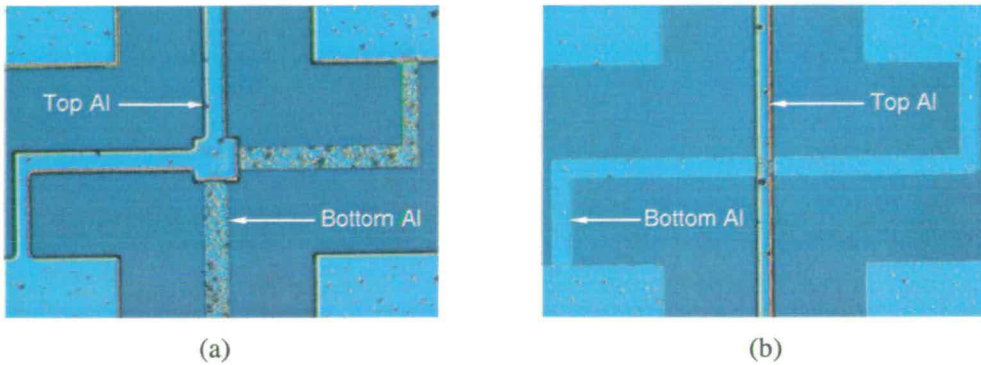
Figure 7.5: *Microscopy images of (a) D-shape Kelvin structure and (b) stacked Greek cross structure after the Al lift-off process.*

7.3.3 Electrical measurements

The Kelvin and stacked Greek cross structures were measured using a HP4062B and a So-lartron 7065 voltmeter by forcing a current of 100 mA from the top probe pad to the bottom one and measuring the voltage drop across the contact area. The contact resistances as a function of contact areas before the Al sintering process are plotted as the two solid lines in Fig. 7.6[1]. It should be noted that the contact resistances of the Kelvin structure were the average values from both L-shape and D-shape structures and revised using error correction curves. The average contact resistivity of 2.008×10^{-8} $\Omega \cdot cm^2$ was extracted from the Kelvin structures and 3.556×10^{-8} $\Omega \cdot cm^2$ from the stacked Greek cross structure. Hence, before the Al sintering

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[1]In Fig. 7.6 and Fig. 7.7, Measured Kelvin refers to the electrical measurements from Kelvin structures, and Simulated Kelvin refers to the Raphael simulation results obtained from the Kelvin structure which will be discussed in the next section. The same convention applies to the stacked Greek cross structure, which has been short-formed as Greek in the figure's legend.

process, the contact resistances extracted from the stacked Greek crosses were 70% higher than the results from the Kelvin structures.
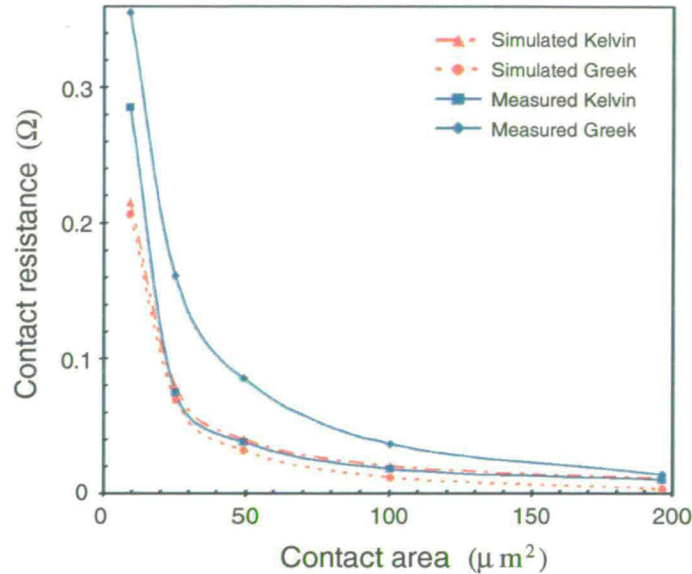
Figure 7.6: *Contact resistance measurements and Raphael simulation results for the Kelvin structures and stacked Greek cross structures before the Al sintering process.*

The contact resistivity (ρ_c) between two Al layers can be reduced by employing a standard Al sintering process at 435 °C with H_2 (5%) and N_2 (95%) for 15 minutes. The measured contact resistances after this process are the two solid lines in Fig. 7.7. The average ρ_c of 4.850×10^{-10} $\Omega \cdot cm^2$ was extracted from the Kelvin structures, which is almost two orders of magnitude smaller than that before the Al sintering process. For the stacked Greek cross structure, however, the extracted contact resistance became independent on the contact areas, which indicates this structure is not providing information about the contact resistance, but is measuring the sheet resistivity of the interconnect at the contact region. It is worth noting that the increase of the contact resistance value for the small geometries for the stacked Greek cross test structure could be due to the self-heating during the measurement and the Al dishing during the bottom metal process.

It is well-known [186, 189–192] and has again been confirmed that the Kelvin structure can be used for measuring ρ_c at all ranges when error correction curves are used. However, these electrical measurements have suggested that the stacked Greek cross structure is capable of providing information about the contact interface at high resistive conditions (e.g. $\rho_c \sim 2.0 \times 10^{-8}$ $\Omega \cdot cm^2$), but is unable to do so at low contact resistive conditions (e.g. $\rho_c \sim 5.0 \times 10^{-10}$ $\Omega \cdot cm^2$).
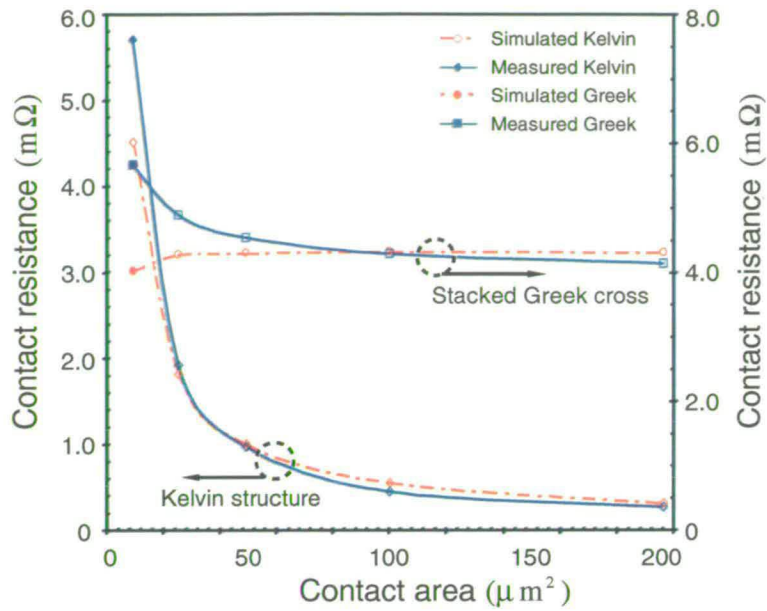
Figure 7.7: *Contact resistance measurements and Raphael simulation results for the Kelvin structures and stacked Greek cross structures after the Al sintering process.*

7.4 Raphael simulation

The contact resistance between two conductive layers can be simulated using a numerical analysis software, TMA Raphael [193]. Raphael is a three-dimensional simulation program for solving Poisson's equation, and is based on the finite-difference method with an automatically adjustable rectangular mesh. It can be used to model both the ideal Kelvin structure and stacked Greek cross structure.

7.4.1 Configurations of the simulation

For the Kelvin structure shown in Fig. 7.8, a potential of 1 volt was applied to the lower arm C with zero volt set on the upper arm A. This results in a current flowing from C to A through the contact area. The difference of the potentials between arms B and D can be extracted from the simulation which enables the contact resistance (R_k) to be calculated,

$$R_k = \frac{V_B - V_D}{I_{CA}} \tag{7.7}$$

The contact resistivity $\rho_k{}^2$ can be derived from equation (7.4), and the contact resistance as function of area can be obtained by varying the contact areas simulated.
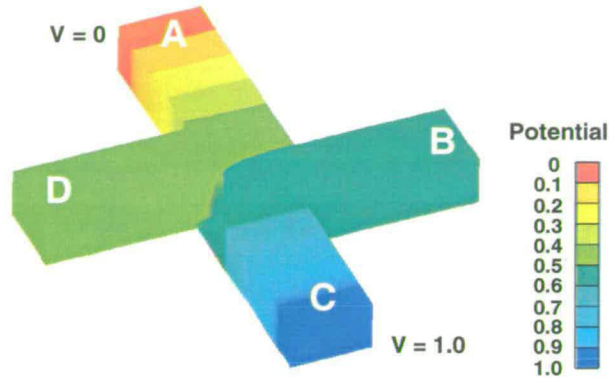
Figure 7.8: *Potential distribution of an ideal Kelvin structure during the simulation of contact resistance extraction.*

A similar procedure can be applied on the stacked Greek cross structure, shown in Fig. 7.9. A potential of 1 volt is applied on the lower arm C and a zero volt on the upper arm D, which results in a current flowing from C to D through the contact area. The difference of the potentials between arms A and B can then be extracted from the simulation to provide a contact resistance (R_g) value,

$$R_g = \frac{V_A - V_B}{I_{CD}} \tag{7.8}$$

A "contact resistivity" figure $\rho_g{}^3$ can also be derived from equation (7.4), which bears some similarities to the extraction scheme in a Kelvin test structure.
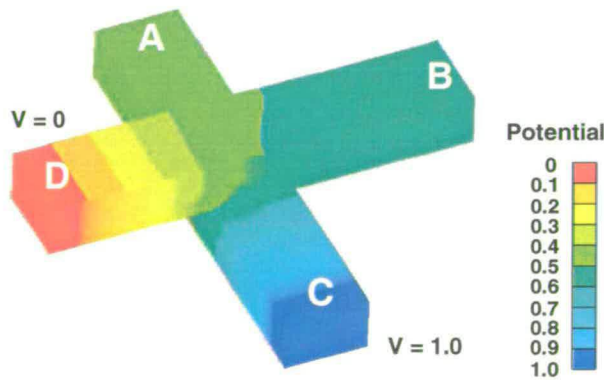
Figure 7.9: *Potential distribution of a stacked Greek cross structure during the simulation of contact resistance extraction.*

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[2] ρ_k is specifically used for the contact resistivity extracted from the Kelvin test structure.
[3] ρ_g is specifically used for the contact resistivity extracted from the stacked Greek cross test structure.

7.4.2 Resistive contact interface

In reality, there is an interface with *infinitesimal* thickness and variable contact resistivity when the conductive layers contact to each other. However, this resistive interface has not been included in the simulation presented above, and also, it can not be directly set within Raphael. Hence, a resistive layer with a *finite* thickness has to be defined as the contact interface, which, inevitably introduces an error to the result. To minimise this error, the thickness of the resistive layer was set to be as thin as possible within the simulation program's limitation.

In Raphael, the resulting contact resistivity between two conductive layers is determined by the thickness and bulk resistivity (ρ) of the contact resistive layer. Since the thickness of this layer was set to be the thinnest within the program's limitation (0.05 μm), the ρ value became the sole parameter to determine the contact resistivity in the Raphael simulation. The ability to control the contact resistivities between two conductive layers in the simulation enables many useful studies.

7.4.3 Simulation results

The comparison between the simulation results and actual electrical measurements provides information about the validation and credibility of the simulation results. In this comparison, the electrical measurement data from Kelvin structure is used as a reference to determine the contact resistance in the simulation, with the same parameters are used for the stacked Greek cross structure. Following the simulation procedures described in section 7.4.1, the simulated results and actual electrical measurements can then be compared, and the comparisons are presented in Fig. 7.6 and Fig. 7.7. It should be noted that in Fig. 7.7, the simulated results at contact area of 9 μm^2 are smaller than expected, which may due to the errors created from the resistive insertion layer in the simulation.

The comparison between an ideal Kelvin structure and stacked Greek cross structure at various contact conditions is also useful for providing information about the usefulness of the stacked Greek cross test structure for different interfacial specific contact resistivity. In the Raphael program, resistive interfaces are created to mimic various contact conditions by varying the resistivity of the insertion layer. The respective contact resistivity ρ_k and ρ_g can then be extracted by using an identical contact resistance for both structures. The comparison is presented in Fig. 7.10 using a normalised contact resistivity (ρ_g/ρ_k).

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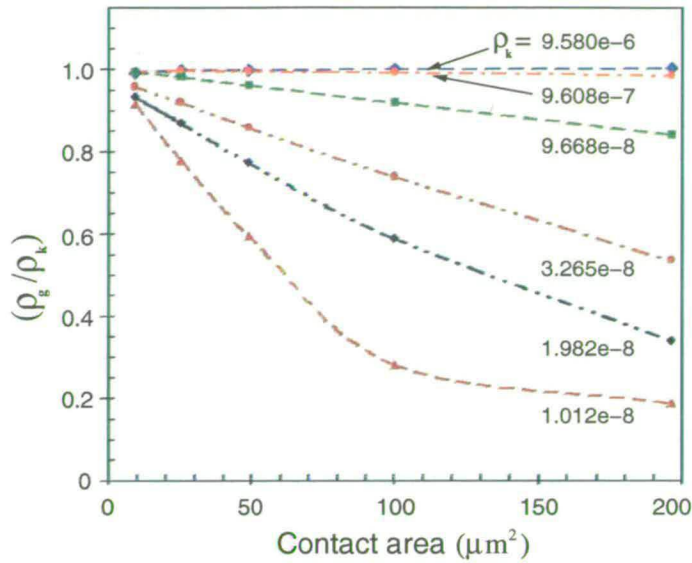
Figure 7.10: *Comparison of extracted contact resistance of the ideal Kelvin and a stacked Greek cross structures using Raphael.*

It can be seen from Fig. 7.10 that ρ_g/ρ_k is close to 1 when ρ_k is in the range of 9.6×10^{-6} - 9.6×10^{-7} $\Omega \cdot cm^2$. This indicates that the stacked Greek cross structure measurement extracts the same R_c as the Kelvin structure when it is used for measuring a high resistive interface. However, as ρ_k decreases, there is a significant difference between the R_c values extracted from the two structures. Since the ideal Kelvin test structure is capable of extracting contact resistivity for all ρ_c, it is clear that the stacked Greek cross structure is not suitable for measuring interfaces with low contact resistivity. For the stacked Greek cross structure, the simulated R_g eventually becomes independent of the contact area when the interface contact resistivity is in the range of 5.0×10^{-10} $\Omega \cdot cm^2$. From these Raphael simulation results, it can be concluded that the stacked Greek cross can be used for contact resistivity measurement when ρ_c is greater than 9.0×10^{-7} $\Omega \cdot cm^2$. However, it can only be used as an indicator of the interconnect quality when the ρ_c less than that critical value.

7.5 Discussions

7.5.1 Validation of the stacked Greek cross structure

From a comparison of the simulations and the actual electrical measurements, it can be concluded that the stacked Greek cross can only be used for measuring a highly resistive contact

interface, such as $\rho_c \geq 9.0 \times 10^{-7}$ $\Omega \cdot \text{cm}^2$. It should be noted that this conclusion has been determined when Al is used as the conductive layer, the critical ρ_c value might change if other materials are used.

The difference between these two test structures is due to their designs and the resulting current flow paths. In an ideal Kelvin structure, a current passes from plane M to plane N through the entire contact interface, as can be seen in Fig. 7.11(a). This results in an essentially one-dimensional current flow over the contact interface regardless of its resistive conditions, Fig. 7.11(b).

(a)

(b)
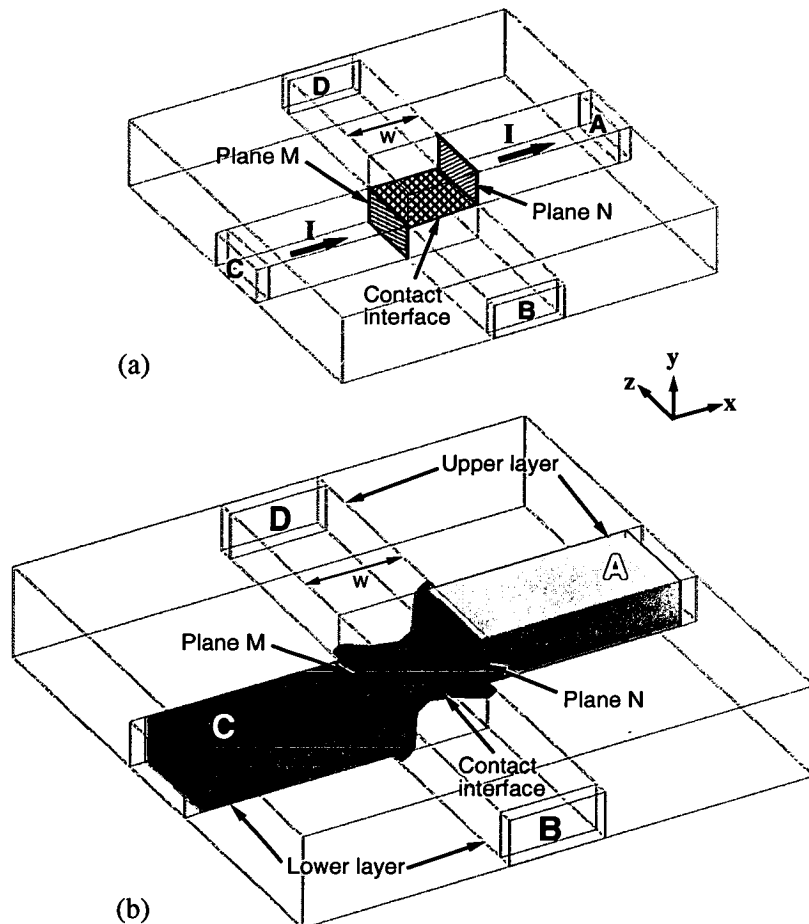
Figure 7.11: *The distribution of current density in an ideal Kelvin test structure: (a) schematic of the current flow path and contact interface, and (b) current density of a Kelvin test structure simulated by the Raphael.*

For the stacked Greek cross structure, when a current passing through the contact interface from arm C to arm D, current flow is not one-dimensional, as shown in Fig. 7.12. Clearly only when

the contact resistance is large, the current flow across the "contact layer" has less crowding in the corner and hence the extracted value better approximates the results giving by the Kelvin structure.
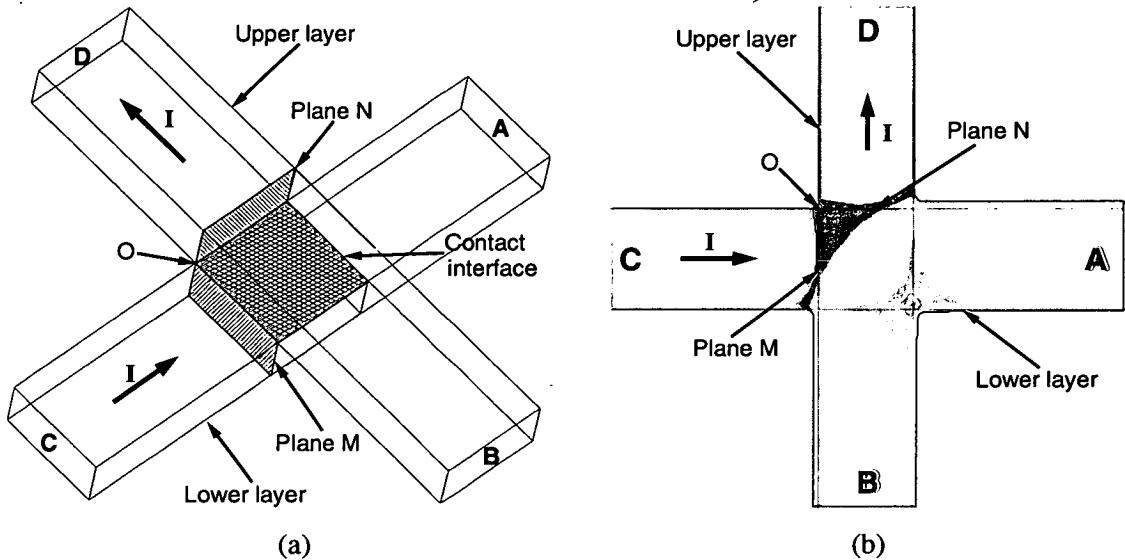
Figure 7.12: *The distribution of current density in a stacked Greek cross test structure: (a) schematic of the current flow path and contact interface, and (b) the current density of a stacked Greek cross test structure simulated by the Raphael.*

7.5.2 Stacked Greek cross structure vs planar Greek cross structure

For the stacked Greek cross structure with a low resistive interface (e.g. $\rho_c < 5.0 \times 10^{-10}$ $\Omega \cdot cm^2$ in Fig. 7.7), the extracted contact resistances (R_g) are independent of the contact area, but there is a relationship with the film thickness. More simulations were conducted for stacked Greek cross structures with $R_c = 0$, and the results compared with those from the planar Greek cross structure, in Fig. 7.13. The inverse proportional of the resistance and film thickness indicates that the stacked Greek cross shows the same character of a planar Greek cross structure which is widely used for the sheet resistance measurement of metal films [194]. This is not surprising as the stacked Greek cross approximates to a planar Greek cross with double the thickness in the centre of the cross.

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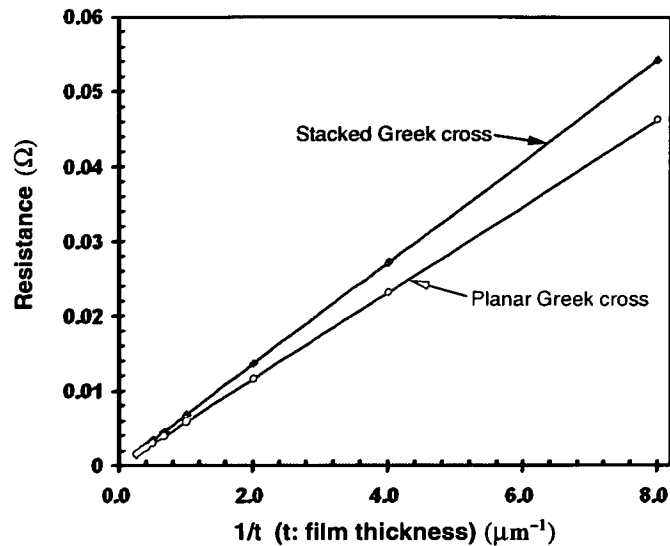
Figure 7.13: *Raphael simulation results: resistance measurements as a function of the film thickness for the stacked Greek cross and planar Greek cross structures.*

7.6 Kelvin structures for wafer bonding

As mentioned before, Kelvin structures are well-established test structures for measuring the contact resistivity between two conductive materials, and accurate ρ_c values can be extracted from this structure with the help of simulated error correction curves [186, 189–192]. Clearly, it would be advantageous if these structures can be used for measuring interconnects between two bonded wafers, and this can be achieved using a modified fabrication sequence.

7.6.1 Modified fabrication process

In this new fabrication sequence, an Al layer is deposited on an oxidised bottom silicon wafer, as shown in Fig. 7.14(a). In order to make the Al structure in the bottom wafer one piece so there are no other contact interfaces in the structure, a partial Al etch is performed after the Al contact area has been defined by the via mask, as shown in Fig. 7.14(b). A second lithography step is then performed (M1 mask) and the exposed Al etched. A PECVD oxide layer is deposited on the bottom wafer and the surface planarised to expose the Al contact areas, Fig. 7.14(c)-(d). A routine Al damascene process is performed on the top wafer using the M2 mask for the lithography step, as shown in Fig. 7.14(e). The two wafers are then aligned and bonded at room temperature and followed by a low temperature anneal to increase the bonding strength, as illustrated in Fig. 7.14(f). Wafer thinning is then performed and probe pads created to enable

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electrical access to the structure from the top surface, as shown in Fig. 7.14(g).

Al layer   Oxide   Al layer

Bottom Wafer

(a) Al deposition on bottom wafer.

Top Wafer

(e) Top Al on top wafer (M2).

Bottom Wafer

(b) Contact area formation (Via).

Bottom Wafer

(c) Al etch (M1) and oxide deposition.

Top Wafer

Bottom Wafer

(f) Wafer bonding.

Bottom Wafer

(d) Oxide CMP.

Top Wafer

Bottom Wafer

(g) Wafer thinning and testing.
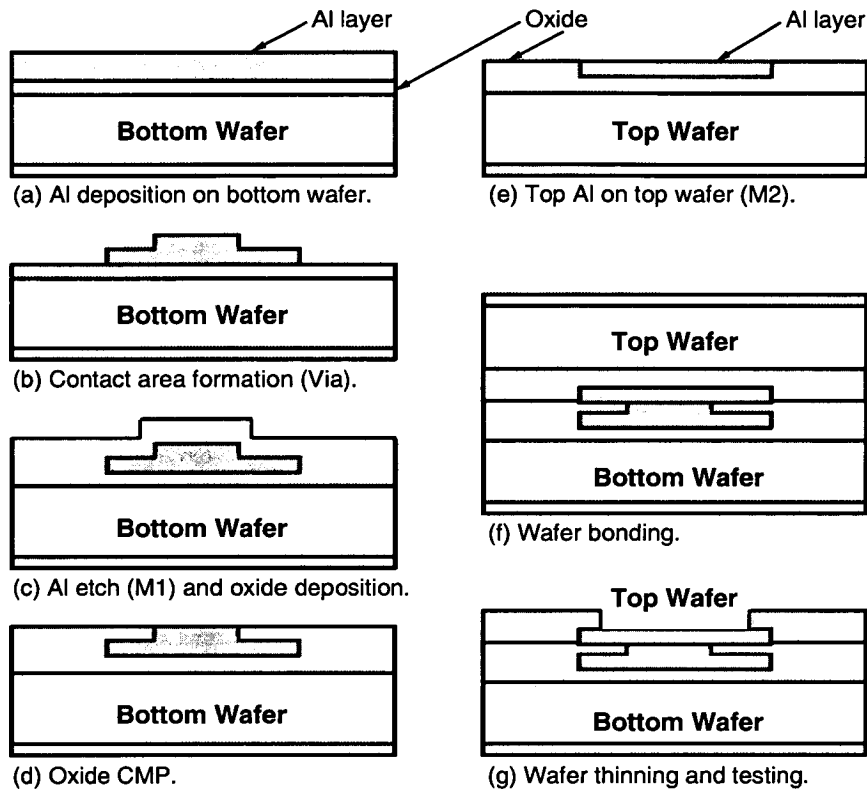
Figure 7.14: *Modified fabrication sequence to form Kelvin contact resistance structures in a wafer bonding process.*

The major modification in this process (Fig. 7.14(a)-(b)) is the two-step Al etch to define the contact area (via mask) and the bottom metal layer (M1 mask). Special attention needs to be paid on the partial etch of the Al (Fig. 7.14(b)), which requires a uniform Al etch rate across the wafer to precisely control the remaining Al thickness.

7.6.2 Fabricated Kelvin structures for bonding process

Using the modified fabrication sequence described in Fig. 7.14, the bottom part of L-shape and D-shape Kelvin structures were fabricated, and the microscope images are shown in Fig. 7.15. The difficulty of this fabrication process was the partial Al etch which did not have a etch stop layer to stop etching at the middle of the Al layer. In order to ease the process requirement, a thicker Al layer (2 μm) was deposited with a target thickness of the first Al etch being 1 μm. With the non-uniformity of the etch rate across the wafer (e.g. loading effect) and etch rate variation (typically 10%) from wafer to wafer, a step between 0.8 to 1.2 μm could be achieved

after the Al etch process, which met the overall fabrication requirement. It should be noted that the rougher bottom Al surface in Fig. 7.15 may due to the etch-rate nonuniformity of this partial Al etch process. The successful fabrication of the Kelvin structures indicated that traditional Kelvin structures can be used for the electrical characterisation of wafer bonding process.

(a)   (b)
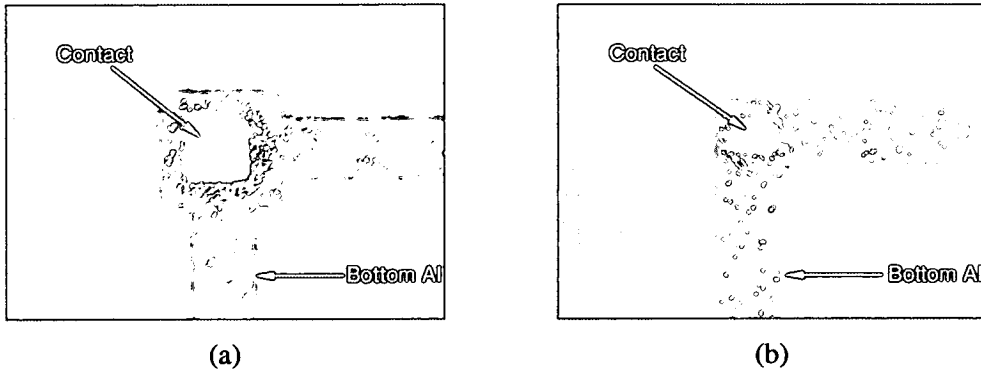
Figure 7.15: *Microscopy images of (a) D-shape Kelvin structure (b) L-shape Kelvin structure, after the formation of bottom metal structures.*

7.7 Conclusions

Using a two-level aluminium metallisation process, Kelvin structure and stacked Greek cross test structure have been electrically compared for their abilities to extract contact resistivity between two conductive layers. Moreover, they have also been compared with Raphael simulation. It can be concluded from the simulation and actual electrical measurement results that the stacked Greek cross can only be used for measuring a high resistive contact interface, such as $\rho_c \geq 9.0 \times 10^{-7}$ $\Omega \cdot cm^2$ for structures using Al as the conductive material.

It has been confirmed that L-shape and D-shape Kelvin structures can be used to measure the ρ_c between bonded wafers by using a two-step Al etch to define the contact area and the bottom metal layer.

Chapter 8
Inter-Wafer Connection — Part II:
Direct Metal Contact

8.1 Introduction

In chapter 6, an oxide bond was performed with aluminium test structures embedded in oxide. Interconnect between bonded wafers were established through contact via after the bonding process. There are obvious attractions for a direct electrical connection to be achieved when wafers are bonded, and the feasibility of this approach is evaluated in this chapter.

8.2 Fabrication sequence and test structures

8.2.1 Fabrication sequence

For the proposed direct metal contact interconnection approach, a damascene process has been used to pattern Al tracks on both the top and bottom wafers, creating an Al and oxide coplanar surface for the subsequent bonding process, as shown in Fig. 8.1(a)-(d). One portion of each wafer surface is a smooth and flat oxide, which will generate mechanical strength for the bonded system. The other surface is a metal which will provide the electrical inter-wafer connections after bonding. It should be noted that, in practice, the Al will exhibit some degree of dishing, causing a step between oxide and Al after the CMP stage. Although this may result in an undesirable gap between the top and bottom Al (Fig. 8.1(e)), slight dishing does ensure full contact of the oxide layers. However, the gap between two Al surfaces is obviously not good for electrical interconnect, but there is the possibility that direct contact can be achieved during the bonding anneal stage due to stress relief in the Al. This is schematically illustrated in Fig. 8.1(e)-(f) [195].

Wafer thinning and probe pad lithography are then performed following the bond anneal step, as shown in Fig. 8.1(g). For this process architecture, the final metallisation process requires

(a) Oxide grown and deposition.

(b) Oxide etch.

(c) Al sputter and Al CMP.

(d) Steps (a) – (c) on top wafer.

(e) Wafer align and bond.

(f) Wafer bonding anneal.

(g) Oxide and bulk silicon etch on the bonded top wafer

(h) Oxide patterning.

(i) Al sputter and CMP.
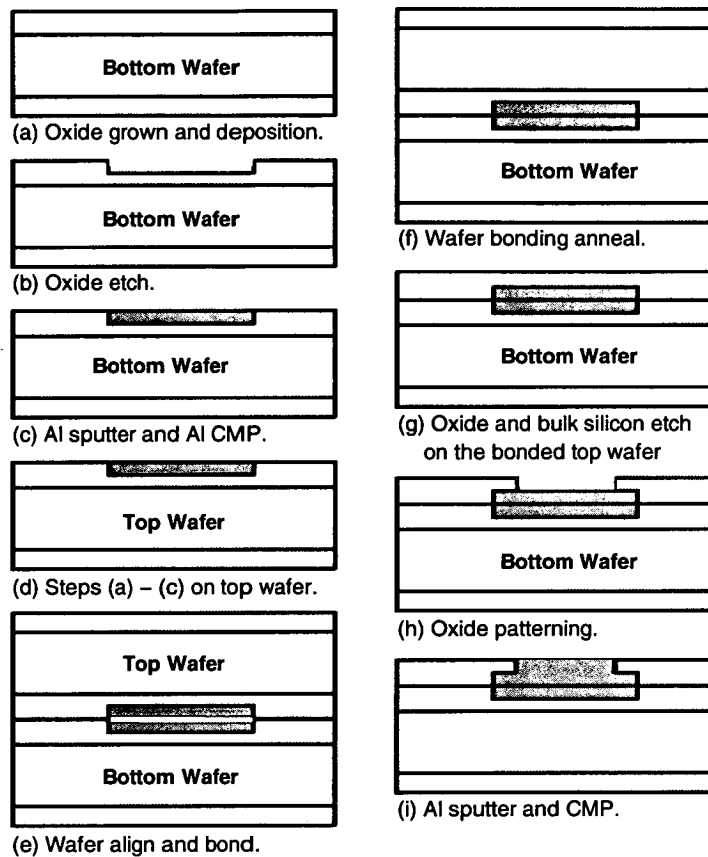
Figure 8.1: *Fabrication process of the direct metal contact approach.*

that only the metal layer on the top wafer needs to be exposed. Therefore, it then becomes possible to perform electrical measurements after an oxide etch (Fig. 8.1(h)). In this example a planar device surface is fabricated by a blanket Al deposition, followed by an Al CMP, as shown in Fig. 8.1(i). Due to the direct connection of the top and bottom metal layers, this process is referred to as direct metal contact in this thesis.

It should be noted that the important parameters for a successful implementation of this approach are (1) a strong oxide to oxide bond to provide mechanical strength for the integrated system, and (2) a good electrical contact between Al structures.

8.2.2   Test structures

The specific contact resistivity of two conductive layers can be extracted using Kelvin test structures with the help of universal error correction curves, and by modifying the fabrica-

tion sequence, Kelvin contact resistance test structures can be made compatible with the wafer bonding process. However, due to its simple fabrication, test structures based on those used in reference [185] have been designed to initially evaluate the direct metal contact architectures. This test structure is referred to as stacked Greek Cross in this thesis. As mentioned before, the crossing tracks of this structure guarantee that the damascened metal layers will contact, even with significant bonding misalignment (Fig. 8.2(a)). The zigzag shape of the contact chain test structure also accommodates bonding misalignment (Fig. 8.2(b)-(c)). A constant metal length is achieved in this design regardless of any wafer bonding misalignment. Structures with contact line widths of 3, 5, 7, 10 and 14 μm have been implemented on the test chip.

(a)

(b)

(c)
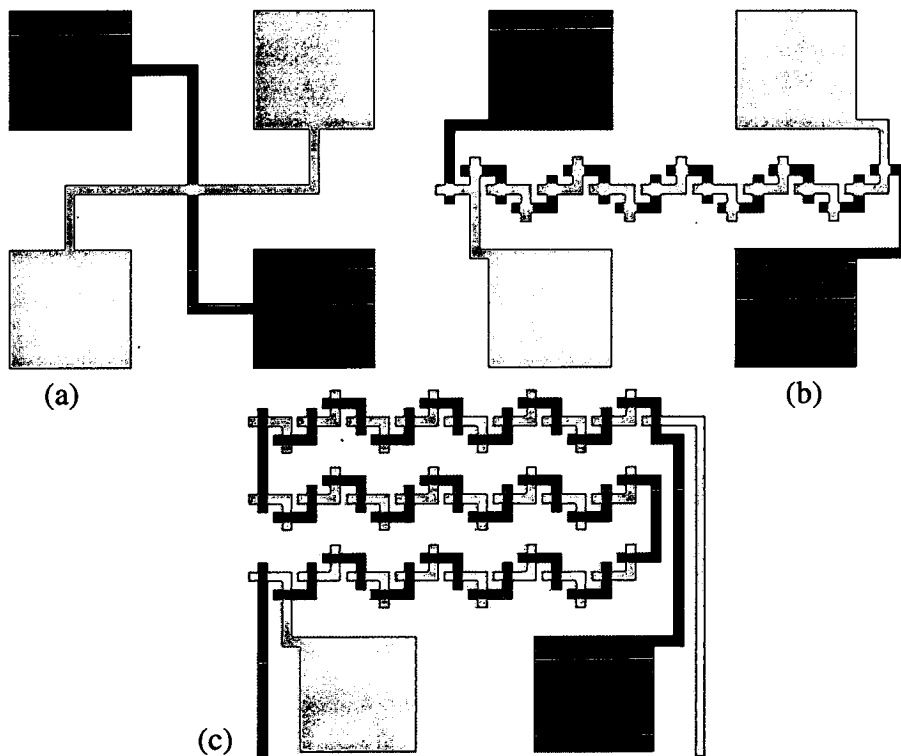
Figure 8.2: *Layouts of the test structures for the direct metal contact approach: (a) single contact structure, (b) short contact chain structure, and (c) long contact chain structure.*

8.3   Fabrication process development

Compared to oxide bonding described in chapter 6, the direct metal contact approach removes the difficulties associated with etching and filling of high aspect ratio inter-wafer vias. However, it poses challenges on the following fabrication steps: (1) Al damascene process to create an Al

and oxide coplanar surface, (2) oxide to oxide bonding with Al structures on the same bonding surface, and (3) controlled stress relief of Al film to establish Al-Al contacts.

8.3.1 Aluminium damascene process

In the damascene process, oxide and Al are present on the same polishing surface, but the production of a co-planar surface is not straightforward. Typically, Al tends to both scratch and dish during the CMP process because of its high malleability and softness (the hardness for Al and SiO_2 are in the range of 2-2.9 and 6-7, respectively [196]). Therefore, the polishing process has to be optimised to reduce mechanical abrasion, enhance chemical reaction and obtain a planarised surface.

8.3.1.1 Scratch prevention

For the damascene process, a trench of 1.2 μm was etched into the oxide layer, and followed by the deposition of 1.5 -1.8 μm of Al. A standard Al polishing process (Table 8.1) was then used to remove Al not in the trenches, and the resulting surface is shown in Fig. 8.3(a). As the Al layer outside the trenches became thinner during the polishing, it becomes possible for Al to be ripped out. This results in very large sized particulates at the interface of pad and wafer surface, and is believed to have caused the severe scratching observed (Fig. 8.3(a)). Poor adhesion between Al and the underlying oxide layer obviously worsens this problem [197].

Hence, a two-stage Al CMP process was developed. Firstly, the standard Al polishing recipe was used to achieve an Al removal rate of $\sim$ 3000 Å min^{-1} using a relatively high down force. When the thickness of Al outside the trenches had been thinned to around 1000 Å, the polishing was switched to a slow Al CMP process (Table 8.1). With low pressing pressure, the polishing rate slowed to around 500-600 Å min^{-1}. This used a slow platen rotation and high slurry flow to dissolve any large Al particulates detached from the wafer that would otherwise scratch the polishing surface. The improved polishing result can be observed (Fig. 8.3(b)) which indicates that the two-stage polishing process overcomes the Al scratching problem.

8.3.1.2 Dishing reduction

One issue was that Al dishing of $\sim$ 3000-4000 Å typically resulted from the above Al CMP process, which was undesirable for the subsequent wafer bonding process. To address this

CMP process parameters	Standard Al polish process	Slow Al polish process	Slow oxide polish process
Head speed	40 rpm	55 rpm	55 rpm
Table speed	40 rpm	25 rpm	25 rpm
Head pressure	0.3 bar	0.15 bar	0.15 bar
Back pressure	0.15 bar	0.07 bar	0.07 bar
Slurry flow	150 ml/min	250 ml/min	150 ml/min
Temperature	Room temperature	Room temperature	Room temperature
Pad	Rodel IC1400	Rodel IC1400	Rodel IC1400
Slurry	PL 1609	PL 1609	30H50

Table 8.1: *Variables and consumables settings for the Al damascene process (rpm - revolutions per minute).*

(a)　　　　　　　　(b)
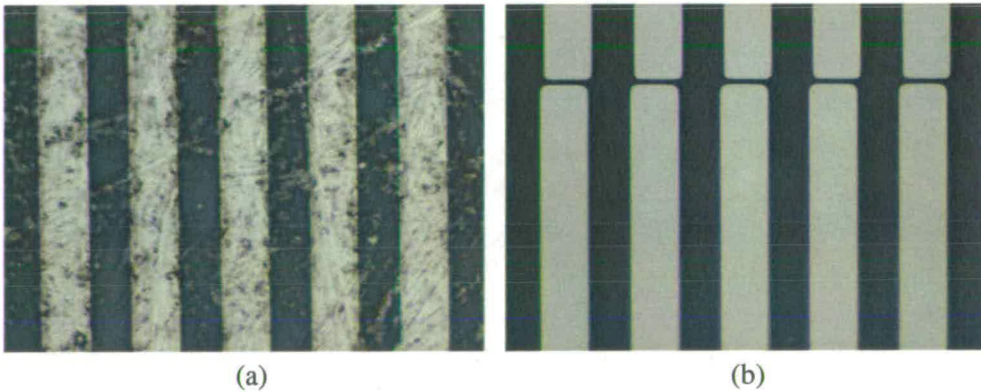
Figure 8.3: *Microscope images of test wafers after the Al CMP process: (a) only use the standard Al CMP recipe, and (b) after a 2-stage Al CMP process where the surface finishes with the slow Al polishing recipe.*

issue, a dry oxide etch was added to reduce the dishing caused by the Al CMP process, and also remove any damaged oxide surface layer that might be present. A very high selectivity between Al and oxide ($> 100{:}1$) can be achieved in an RIE etch system, and so it was relatively straightforward to planarise the oxide and Al at the wafer surface by removing 3000-4000 Å of oxide. Because both Al and oxide could be polished by a low down force oxide CMP process (Table 8.1) at the similar removal rate (600 Å min^{-1}), this process was used to achieve a flat and smooth surface for the subsequent wafer bonding. After 30 to 60 seconds polishing, a smooth oxide surface with Al dishing of less than 200 Å was achieved, as shown in Fig. 8.4. Hence a suitable Al damascened surface can be obtained using an optimised CMP process combined with a dry oxide etch.
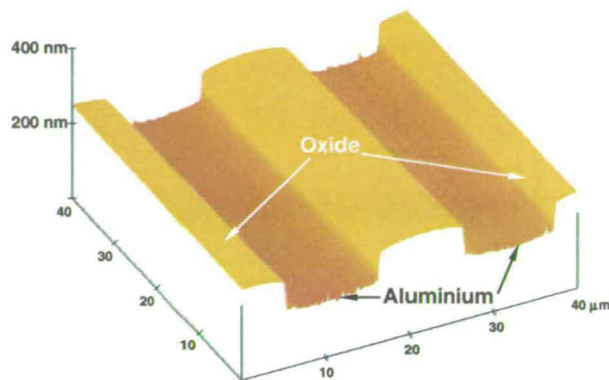
Figure 8.4: *AFM surface profile of an aluminium CMP damascene processed wafer.*

8.3.2 Bonding and thinning of Al damascened wafers

The direct metal contact approach requires bonding and thinning of Al damascened wafers. The initial attempt to bond an Al damascened wafer (10 μm Al tracks separated by 10 μm strips of oxide, Fig. 5.2(b)) to a blanket PECVD oxide covered wafer was not particularly successful, as delamination occurred during dicing. It should be noted that only 50% of the wafer was available for an oxide-oxide bond (see Fig. 5.2(b)), and a closer inspection of Fig. 8.4 shows that the oxide strips are not flat, being rounded near the aluminium tracks, thereby further reducing the bonding contact area. It should be noted that no force was applied during the bond process.

Further wafer bonding experiments on Al damascene patterned wafers were performed using the direct metal contact test structures, with approximately 20-30% of the chip surface area being Al. Fig. 8.5 shows the bonded structures after removal of the top silicon wafer using an STS ICP etcher, as described in section II. It should be noted that the lower percentage of Al surface coverage on the wafer enabled around 30-40% of the wafer area to form an oxide-oxide bond. This indicates that oxygen plasma assisted low temperature oxide to oxide bonding can be performed with Al structures on the same bonding surface.

However, Al areas, together with the surrounding 40-60 μm regions of oxide, appeared not to bond. Al to oxide bonding was not expected, but the poor bonding of the areas surrounding the structures removed any chance of achieving direct metal contact. The results suggest that the conditions used for low temperature bonding of oxide to oxide may not be not suitable for Al damascened wafers, especially where large pad areas of Al are present. The fact that oxide to oxide bonding is successful suggests that the Al damascene polish is not the cause of the
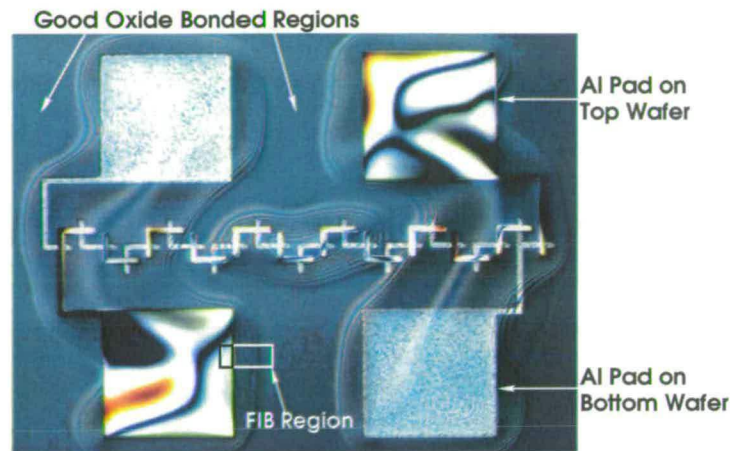
Figure 8.5: *Microscope image of contact chain structure after wafer thinning process (first attempt).*

problem. It was postulated that stresses in the oxide and/or stress mismatches may be sufficient to break the oxide-oxide bonds near the Al areas when the handle wafer is removed. Also, Al dishing and oxide erosion that occur during CMP might be other reasons for the observed poor bonding surrounding the Al structures. Fig. 8.6 shows a cross section of the bond regions at the edge of an Al pad and this suggests that the compressive stresses in the top oxide/Al films cause the top surface to bow after the handle wafer has been removed.
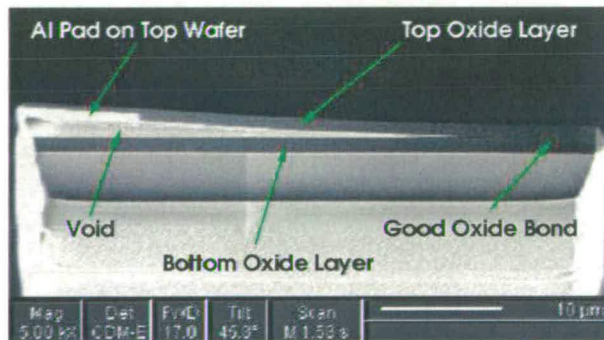
Figure 8.6: *Cross section view of a bonded sample at the edge of Al pad (first attempt). Sample was prepared using focused ion beam (FIB).*

Further experiment results have confirmed that the tendency for the top oxide layer to delaminate upon removal of the silicon donor wafer is mainly due to the compressive oxide stress, which can be prevented by using low stress PECVD oxide film and increasing the oxide thickness to 2.7 μm, as shown in Fig. 8.7. This is in spite of the oxide bonding area being less than 100% and Al structures being present on the bonding surface. The successful bonding and thinning of Al damascened wafers indicates that oxygen plasma assisted low temperature

bonding is able to provide necessary mechanical strength for pairs of bonded wafers with direct metal contact.
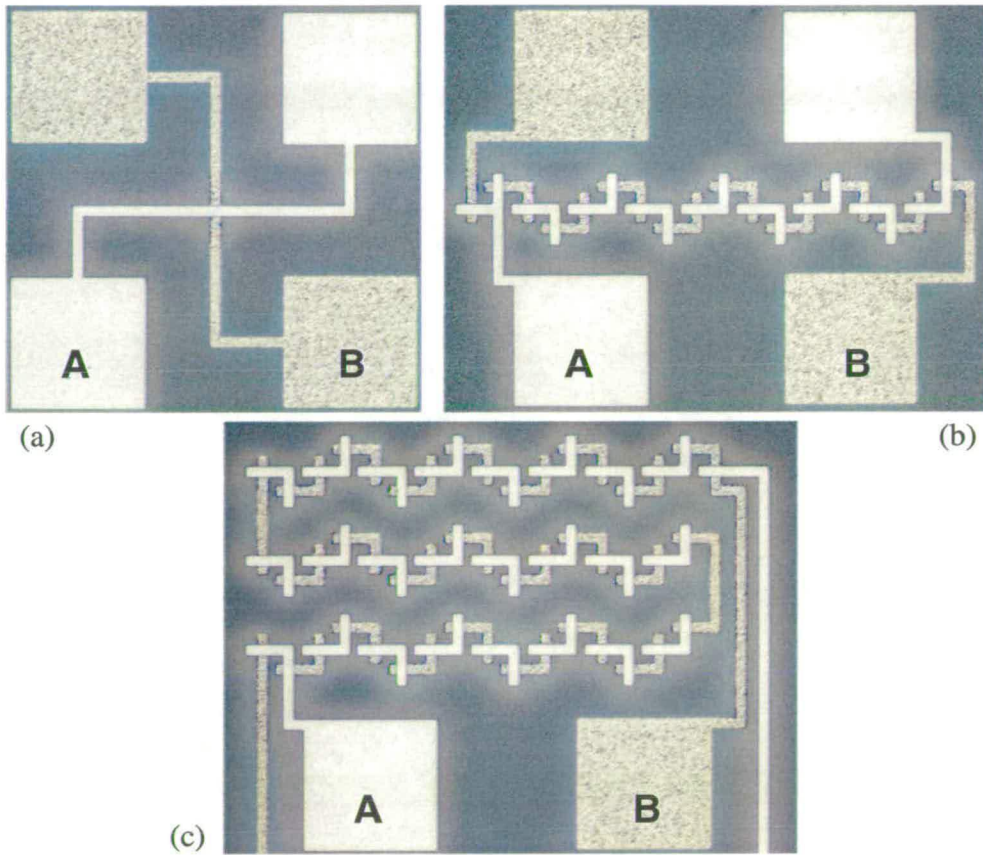
Figure 8.7: *Microscope images of (a) single contact structure, (b) short contact chain structure and (c) long contact chain structure after the wafer thinning process. In these images, Al structures on the top wafer were covered with 2.7 μm oxide. A and B represent the Al structures on top and bottom wafers, respectively.*

8.3.3 Aluminium contact interface

The interface of the Al contact (Fig. 8.8), investigated by sectioning samples with a focused ion beam (FIB), showed that top and bottom metals contacted each other via hillocks that were formed on both wafers during the anneal process. Although top and bottom Al layers were not perfectly joined together, the FIB image indicates that the resulting gap between metal layers caused by the Al dishing, has been bridged and electrical connections established through stress relief.

Whilst Al hillock growth does help to establish electrical contact, it also tends to force the
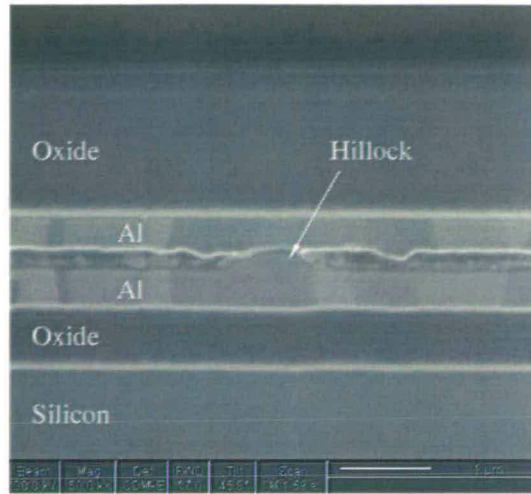
Figure 8.8: *Cross section view of the Al contact (second attempt). Sample was prepared using FIB.*

wafers apart, weakening the oxide bond surrounding Al structures, as illustrated in Fig. 8.9. The small gap observed near the edge of Al region may also due to oxide erosion during the CMP process. However, this gap explains the nonuniform colour of oxide near the Al structures in Fig. 8.7. Further experiments are required to fully characterise the bond surrounding Al structures, and to verify whether delamination can be eliminated using options such as adding pressure during the bonding and annealing steps, or optimising the Al dishing.
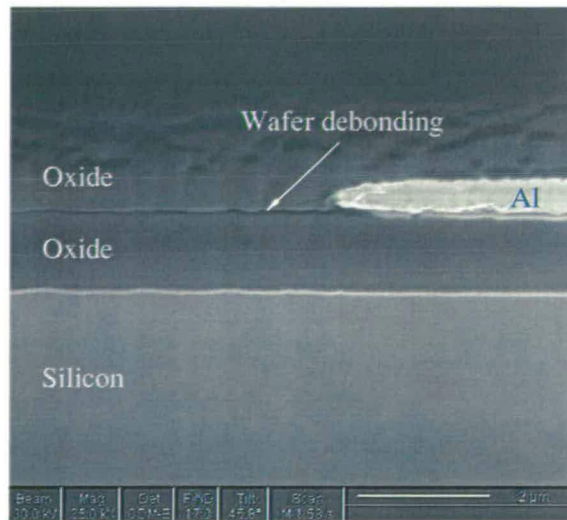
Figure 8.9: *Bonded sample at the edge of Al contact: the formation of Al hillocks pushing the wafers apart.*

8.4 Electrical measurements

A resistance measurement was performed between top and bottom metals using the single contact structures as shown in Fig. 8.2(a)[1], and the results presented in Fig. 8.10. The average "contact resistance" was 2.6×10^{-8} $\Omega \cdot cm^2$ with the tendency for the test structures with larger contact area having a lower resistance and smaller variations. These measurements indicate that hillocks have penetrated the native Al_2O_3 (or the oxide has been reduced) to make ohmic contact. Assuming uniform hillock density across the metal structures, those with a larger contact area will statistically contain more hillocks and provide a more robust electrical connection.
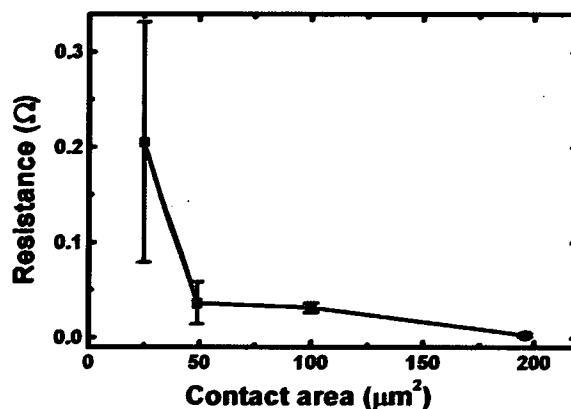
Figure 8.10: *Contact resistance as a function of contact area.*

The contact chain structures (Fig. 8.2(c)) have been used to provide a measure of the yield of the interconnects. Ninety percent of chains with contact areas of 14×14 μm^2 were conducting, with an average chain resistance of 9.76 Ω. This contrasts with only 20% of structures with contact area of 10×10 μm^2 were conducting, with a higher average resistance of 28.7 Ω. Chain structures with a contact area less than 10×10 μm^2 were all open circuit. These results suggest that, although direct metal contact can be established, the process is not robust enough for integration into a manufacturing process.

8.5 Discussions

The mechanical strength of the Al contacts can be observed for the bonded samples after completely removing the oxide layer covering the Al structures. When the oxide on the handle wafer has been removed the compressive stress from oxide pulls (or delaminates) the top Al

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[1]The measurement of this structure and its limitations have been discussed in chapter 7.

layer, as shown in Fig. 8.11, and the possible mechanism of this phenomenon is illustrated in Fig. 8.12. In this situation, an Al to Al bond between the two levels of interconnect is all that holds the top Al layer to the wafer.
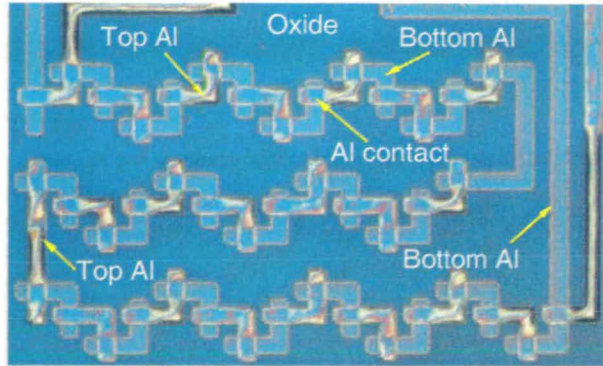
Figure 8.11: *Microscope image of the bonded sample after the removal of top oxide layer. The top metal tracks bowed up during the oxide etch process and would stay in this state for several days before relaxing back to the wafer surface.*
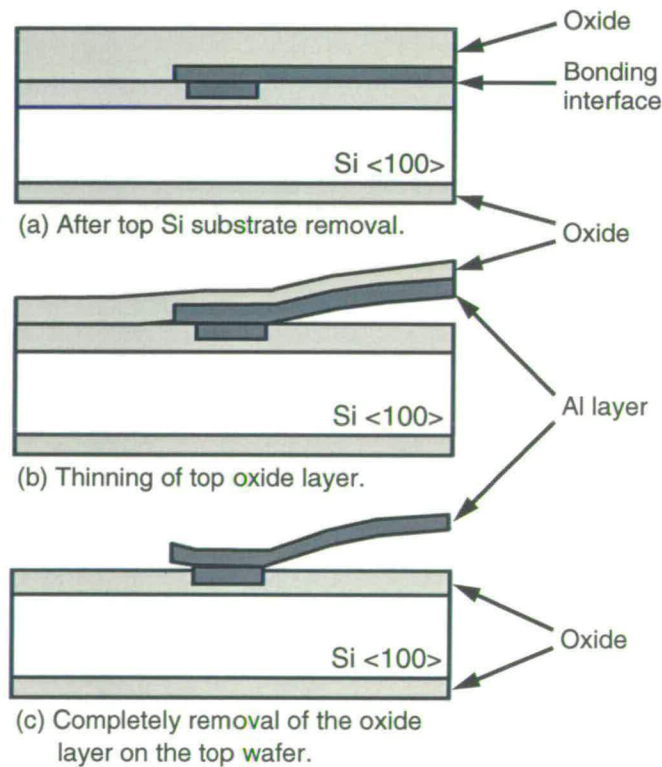
Figure 8.12: *Schematic of the oxide thinning process.*

Figure 8.11 clearly indicates that an Al to Al bond exists which has sufficient strength to ensure the contact chain remains electrically conducting. Wafer bonding using Al as an intermediate

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material in vacuum has been reported [198] using a plasma system to remove the Al_2O_3 on the surfaces and bonding them in the vacuum chamber. To the author's knoweledge, successful bonding of Al in atmosphere has not been reported which might be due to the formation of hard Al_2O_3 layer on the Al surface (typical thickness of this oxide is 3.0 nm [28]). The strong Al bond in Fig 8.11 suggests that Al, despite its hard passivation layer (Al_2O_3), can be bonded which is probably due to the growth of hillocks during the thermal treatment. However, it should be noted that the area of the Al-Al contacts is only a small percentage of the wafer area. The percentage of the Al-Al bonding areas compare to the whole Al film, and the locations of these contacts (such as Al grain boundary triple junction [195, 199]) could be important when Al is bonded in atmospheric conditions. Future experiments could be designed to fully investigate and characterise this.

8.6 Conclusions

The work presented in this chapter has demonstrated the feasibility of integrating MEMS and CMOS technology using CMP and wafer bonding. Plasma assisted low temperature oxide bonding has been shown to provide the necessary mechanical strength for bonded wafers. Electrical connection can be established during the high temperature bond anneal process through the Al stress relief and the subsequent formation of hillocks. Whilst this approach is very attractive because interconnect is established as part of the bonding process, the mechanism associated with the direct electrical connection needs significant attention if it is to be successfully implemented in production. Future work will need to involve the bonding and annealing wafers under pressure to determine if this can be used to improve the bonding and interconnect performance.

Chapter 9
Conclusions and Future Work

9.1 Introduction

The feasibility of using chemical mechanical polishing and oxygen plasma assisted low temperature wafer bonding to integrate prefabricated MEMS and CMOS devices has been investigated in this thesis. This chapter summarises the results and presents conclusions on this integration approach. In addition, future work is suggested.

9.2 Review of the results

9.2.1 Wafer bonding of prefabricated wafers

As prefabricated wafers normally possess severe topography and contain metal structures, the first challenge for the proposed integration approach is to bond prefabricated wafers at low temperature ($\leq$ 450 °C). These results have been presented in chapter 5. PECVD oxide was selected as the top surface layer for both CMOS and MEMS wafers because of the suitability of its surface properties for direct wafer bonding, and also because of its low deposition (300 °C) and annealing (435 °C) temperatures. In particular, a high frequency deposition process was selected to achieve low film stress after the deposition and densification steps. Through the use of an appropriate CMP process, the typical surface roughness of PECVD oxide (2.8 nm) can be reduced to an R_a less than 0.5 nm, and challenging topography can also be modified, to levels compatible with wafer bonding. The tensile measurement results indicate that sufficient bonding strength ($\sim$ 10 MPa) can be achieved from the low temperature (200 °C) bonding of prefabricated wafers when assisted by an oxygen plasma treatment, which is comparable with the high temperature (1000 °C) fusion bonding. Finally, the successful bonding and thinning of wafers with patterned Al indicates that the integration of prefabricated CMOS and MEMS wafers is possible, using CMP and low temperature bonding.

9.2.2 Inter-wafer connection

The provision of electrical interconnects between bonded MEMS and CMOS wafers is obviously another crucial step of the integration approach presented in this thesis, and two inter-wafer connection options were evaluated. In the first approach, presented in chapter 6, processed wafers were aligned and bonded using PECVD oxide as a direct bonding material. Interconnects between wafers were then established through specifically designed contact vias using a standard multilevel metallisation process. The electrical measurements demonstrated that inter-wafer connections can be achieved using this approach with an average contact resistivity of 1.7×10^{-8} $\Omega \cdot cm^2$ from the single contact via test structure.

The second inter-wafer connection scheme, investigated in chapter 8, uses a direct metal contact at the wafer bonding stage to provide interconnections between the MEMS and CMOS wafers. It has been demonstrated that plasma assisted low temperature oxide bonding provides the necessary mechanical strength for the pair of bonded wafers. The electrical connection in this process is established during the bonding anneal by stress relief and the subsequent formation of Al hillocks. The average contact resistance of 2.6×10^{-8} $\Omega \cdot cm^2$ has been extracted, with the tendency for the test structures with larger contact area to have a lower contact resistance and smaller variations. However, the yield on this process was low (approximately 90 % for chain structure with contact areas of 14×14 μm^2 and only 20 % for the same structure with contact areas of 10×10 μm^2), and would need further improvement before it would be considered robust enough for manufacturing.

9.2.3 Test structures

In order to obtain a better understanding and also to optimise the fabrication processes, test structures have been designed and implemented throughout the development of the above integration schemes. These include the CMP test structures (illustrated in Fig. 5.2) to characterise the polishing process for the surface planarisation, and Kelvin type test structures to characterise the inter-wafer connection schemes (indirect metal contact scheme (Fig. 6.4) and direct metal contact scheme (Fig. 8.2)). These test structures have served as indicators to determine the feasibilities of the proposed new fabrication technique.

In addition, chapter 7 has presented an investigation on two types of test structures: Kelvin structure and stacked Greek cross test structure, for their abilities to characterise the electrical

interconnects between bonded wafers. Using a two-level Al metallisation process, these two test structures have been electrically compared for their ability to extract contact resistivity (ρ_c) between two conductive layers. Moreover, these two test structures have also been evaluated using the Raphael simulation. From these simulation and electrical measurements, it has been confirmed that Kelvin structure can be used for measuring ρ_c at all ranges with the help of simulated error correction curves. However, the stacked Greek cross test structure is (not surprisingly) only able to identify contacts with high resistivity (e.g. $\rho_c \geq 9.0 \times 10^{-7}$ $\Omega \cdot cm^2$ when Al is used as a conductive material).

9.3 Future work

For applications of the proposed CMOS-MEMS integration approach better suited to routine manufacturing, further improvements and investigation are required. For example, long-time processes, such as the 16 hours of annealing used for both the PECVD oxide outgassing and stress release, and to increase the wafer bonding strength (pages 74 and 75) should be shortened to ensure the processes are more suitable for commercial manufacturing. And also, the effect of processes such as wafer bonding and thinning on the CMOS and MEMS devices need to be addressed. In addition, the following two areas need special attention: (1) yield improvement for the direct metal contact bonding, and (2) a reliability study of the integrated system.

9.3.1 Optimisation of direct metal contact approach

For the direct metal contact bonding (presented in chapter 8), the electrical measurements suggest that, although direct metal contact can be established, the currently obtained yield provides significant opportunity for further improvement. Possible process development can be performed in the following two areas: (1) optimising the wafer bonding and anneal conditions, and (2) using other metallisation materials to replace Al for the direct metal contact.

1. Wafer bonding process optimisation

For the direct metal contact approach, the electrical interconnect depends on stress relief and the growth of Al hillocks during the bonding anneal stage for the two metal layers to contact. With the reported process, slight Al dishing has been used to ensure full contact of the oxide layers between the two wafers to establish sufficient mechanical strength between the bonded

wafers. This results in an undesirable gap between the metal layers. Therefore, the subsequent thermal treatment, which results in Al expansion as stress is released, serves two purposes: (1) effectively reducing the hard passivation layer (Al_2O_3) on Al surfaces, and (2) to fill the gap between two metal layers. Optimised dishing is essential since less dishing will cause too much Al expansion which breaks good oxide-oxide bond surrounding the Al structures; on the other hand, too much dishing causes the Al gap to be too big to be closed during the thermal treatment. To obtain an appropriate range of the Al dishing is critical for the improvement of the interconnect yield in this approach.

It should be noted that for the reported fabrication sequence, no extra pressure has been applied to force both Al and oxide contact to each other during the thermal treatment. The wafer pair were simply held by the bonding strength generated by the oxide-oxide bond. The coefficient of thermal expansion of Al is $\sim$ 7 times greater than that of the oxide (Al is 23 $\times 10^{-6}$ K^{-1} and oxide is only 3.3 $\times 10^{-6}$ K^{-1} at 20 °C [196]), and the mismatch of these two materials can cause the following: (1) Al expansion breaks the oxide-oxide contact and results in poor oxide bonding surrounding the Al tracks, (2) poor oxide bonding provides unsufficient strength for achieving a good Al-Al connection. Therefore, an improvement of the Al contact quality should be expected if external force are added on the bonded wafers during the wafer anneal process.

2. Other metals for interconnections

As discussed in chapter 4, small geometry metal structures can be bonded using a thermocompression bonding technique, and metals such as Cu and Ti have been reported to be successfully used as wafer bonding materials [151, 152]. They can also be used for the direct metal contact approach. For Cu, more fabrication steps are required to form a Cu difussion barrier layer, but the resistivity of Cu is lower than that of Al. Although Ti has a slightly higher resistivity than Al, a similar fabrication procedure can be used for its integration. It should be noted that both Cu and Ti are IC-compatible materials and have been used for the manufacturing for more than a decade. Therefore, no extra investigation on the material contamination and reliablity are required for these two metals.

9.3.2 Reliability of integrated systems

The reliability of the fabricated system obviously must be determined before the proposed CMOS-MEMS integration approach can be considered production worthy. For this approach, the major concerns on the reliability are the bonding interface and the inter-wafer connections.

1. Bonding interface

For an integrated system, the bonding interface is exposed to mechanical stresses from environmental vibrations, thermo-mechanical mismatch or internal pressure. These degrade the mechanical strength and reliability of the bonded interface. Also, the fatigue and stress corrosion processes can lower the bond strength over the long-term or increased loading cycles [163]. Therefore, even if the level of mechanical stress is considerably less than the initial wafer bonding strength, the device could fail after a finite load-depending lifetime. The knowledge of the bonding interface under such environmental conditions is practically important.

2. Interconnect

The establishment of the inter-wafer connection is an unique process step in the proposed CMOS-MEMS integration approach. Therefore, the reliability of this system requires specific investigation to understand the relationship between the bonding reliablity with the interwafer interconnect reliability. Typical metallisation interconnect reliability issues, such as electromigration, stress voiding, corrision and insulator failures can all occur in the integrated system. The interaction between microstructure, IC devices and behavior of conducting films under applied currents and elevated temperature will also affect the system. Test structures for rapid determination of the wear out as well as the defect assessment are important. Conventional methods, for example, burn-in technique, can be used for determining the reliability of the integrated system. Better reliability can be achieved by understanding potential failure mechanisms and using this understanding to determine the design rules, select appropriate materials and optimise fabrication procedures.

9.4 Conclusions

As mentioned before, MEMS devices are able to act as the interface between the digital electronic world and the analog physical world, and a wide variety of real world signals can be bridged by the MEMS devices. Depending on the transduction mechanism, the micromechani-

cal structure is then designed to ensure the highest efficiency of transduction. As a consequence, it is no surprise that MEMS devices have to be fabricated using a broad range of techniques. It is therefore necessary to have multiple options for integrating MEMS devices with CMOS electronics.

This thesis provides an alternative integration option which enables MEMS and CMOS devices to be fabricated on separate wafers, and then integrated using chemical mechanical planariasation and wafer bonding. It should be noted that from a commercial point of view the best area ratio for the CMOS and MEMS chips is 1:1 where there is no unused or wasted chip area for either the CMOS or MEMS technology. For MEMS and CMOS devices with different chip areas (that can be considered as a yield loss), the analysis of the relationship between the chip size and the ratio of CMOS to MEMS chip area is shown in Fig. 9.1.
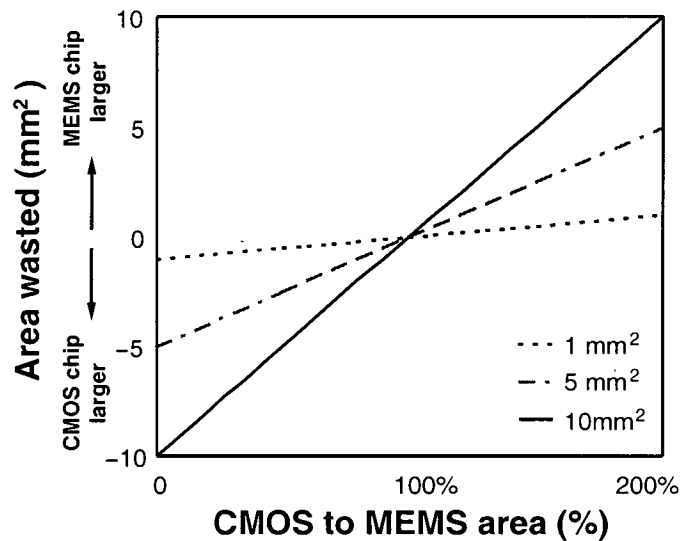
Figure 9.1: *Relationship between MEMS and CMOS area that remains unused for bonded wafers as the ratio of the chip size of the two technologies varies [25].*

The advantages of the approach presented in this thesis can be summarised as following: (1) MEMS and CMOS devices can be fabricated separately, which enables the full optimisation of both fabrication technologies, (2) once developed, the integration process can be applied for many different kinds of MEMS and CMOS devices, (3) the integration processes are realized using exsiting materials (such as PECVD oxide and Al), and standard IC and MEMS fabrication equipments (such as CMP, RIE plasma system and wafer aligner), which makes easy adoption by the manufacturers, and (4) once the bonded wafer pair has been thinned, it can be treated as a normal wafer to go through subsequent processing steps, which gives the manufacturers

more flexibility in the fabrication, and the designers the option of stacking more than one level of devices.

Appendix A
Runsheets

The fabrication sequences of low temperature bonding of prefabricated wafers (Fig. 5.9), electrically connecting bonded wafers using oxide bonding approach (Fig. 6.1) and direct metal contact approach (Fig. 8.1) have been discussed in chapter 5, 6 and 8, respectively. This section presents the fabrication run sheets of these three processes.

Run Sheet – Wafer Bonding Strength Evaluation

Batch number: HL060609	Starting material: 3", n-type, <100>, Si test wafer
Number of wafers: 6	

Step	Process	Tools	Description	Comments
1	Thermal oxidation	Furnace: Tube 10	Grow 1.0 μm thermal oxide Recipe: wetox11 (950 °C) Time: 02:30:00	All wafers #1-6 Top wafers #1-3, and bottom wafer #4-6
2	Oxide thickness measurement	Nanospec	Oxide thickness measurement, 5 points / per wafer	All wafers #1-6
3	Aluminium deposition	Balzers sputter	Deposition 1.0 μm Al Ar: 2×10^{-3} mbar, 1.0 kW	Top wafers #1-3
4	Lithography process	5× Stepper Optimetrix	Mask ID: Bond-Mask (New) Coating: SPR2, 4000 rpm, 1.2 μm Develop: MF-26A, 60 sec Expose: 5× Stepper, 800 ms	Top wafers #1-3
5	Al etch	STS metal etcher	1.0 μm Al etching $SiCl_4$ 37 sccm, Ar: 14.6 sccm Pressure: 170 mTorr, 125 W	Top wafers #1-3
6	Photoresist strip	Barrel asher	Time: 1 hour Oxygen plasma, 350 W, 780 mTorr	Top wafers #1-3
7	Al anneal	Furnace: Tube 8	Wafer annealing 435°C and 15 min	Top wafers #1-3
8	PECVD oxide deposition	STS PECVD Multiplex	Deposit 1.5 μm PECVD oxide Recipe: HFSIO Time: 40 min N_2: 392 sccm, N_2O: 1420 sccm SiH_4: 10 sccm 13.56 MHz, 900 mTorr, 30 W	Top wafers #1-3
9	Oxide thickness measurement	Nanospec	Thickness measurement, 5 points / per wafer	Top wafers #1-3
10	PECVD oxide densification	Furnace: Tube 8	Wafer annealing: 435 °C with N_2 flow for 16 hours	Top wafers #1-3
11	Topography measurement	Dektak 8000 profiler	Step height measurement, 5 points / per wafer	Top wafers #1-3
12	Oxide CMP	Presi Polisher	Topography and roughness removal	Top wafers #1-3
13	Post CMP cleaning	Mask scrubber	1. TMAH 10% 5 min 2. Mask scrubber: both sides 3. DI water rinse 4. Marangoni drier	Top wafers #1-3
14	Thickness measurement	Nanospec	Thickness measurement, 5 points / per wafer	Top wafers #1-3
15	Topography measurement	Dektak 8000 profiler	CMP dishing and wafer bow measurement	Top wafers All wafers
16	Pre-bonding chemical treatment	VacTech and wet bench	1. Oxygen plasma treatment 2. DI water rinse 3. Wafer drying	All wafers
17	Wafer bonding	Karl-Suss	Room temperature bonding	All wafers

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Step	Process	Tools	Description	Comments
18	Infra-red transmission inspection	IR camera	Interface voids inspection	All bonded pairs
19	Bonded wafer dicing	Disco saw	10 × 10 mm squares prepared from the bonded wafers	All bonded wafer pairs
20	Tensile bond strength measurement	M30K tensile test machine	Wafer bonding strength measurement	Diced samples

CMOS-MEMS Integration - Oxide Bonding Approach

Batch number: HL060606-1	Starting material: 3", n-type, <100>, Si test wafer
Number of wafers: 12	

Step	Process	Tools	Description	Comments
1	Thermal Oxidation	Furnace: Tube 10	Grow 2 KÅ thermal oxide Recipe: wetox11 Time: 50 min	All wafers
2	Oxide Thickness Measurement	Nanospec	Thickness measurement	All wafers
3	Lithography Process	Karl Suss	Mask ID: Mask A (for bond align) Coating: 1,1,1 Develop: 1,1,1 Expose: Karl Suss	Top wafers: #1-6 (Frontside)
4	Lithography Process	Karl Suss	Mask ID: Mask B (for bond align) Coating: 1,1,1 Develop: 1,1,1 Expose: Karl Suss	Bottom wafers: #7-12 (Frontside)
5	Oxide Etch	Plasma-Therm	2 KA oxide etching CF_4: 60 sccm, H_2: 10 sccm Power: 750 W, Time: 10 min	Wafers #1-12 (Frontside)
6	Si Etch	STS ICP Etcher	2.0 μm silicon etching Recipe: Scuba6 Time: 3 min	Wafers #1-12 (Frontside)
7	Photoresist Strip	Asher	Time: 1 hour Oxygen plasma, 350 W, 780 mTorr	Wafers: #1-12
8	Topography Measurement	Dektak 8000	Step height measurement, 5 points / per wafer	Wafers: #1-12
9	Oxide Etch	Plasma-Therm	2 KÅ oxide etching Recipe: Oxide-Etch Time: 10 min	Wafers: #7-12 (Backside)
10	Silicon CMP	Presi Polisher	Wafer backside polishing for smooth surface	Bottom wafers: #7-12 (Backside)
11	Post CMP Cleaning	Mask Scrubber and Wet Bench	1. TMAH 10% 5 min 2. Mask scrubber: both sides 3. DI water rinse 4. Marangoni drier	Bottom wafers: #7-12
12	Lithography Process	Karl Suss	Mask ID: Mask C (for bond align) Coating: 1,1,1 Develop: 1,1,1 Expose: Karl Suss	Bottom wafers: #7-12 (Backside)
13	Si Etch	STS ICP Etcher	2.0 μm silicon etching Recipe: Scuba6 Time: 3 min	Wafers: #7-12 (Backside)
14	Photoresist Strip	Asher	Time: 1 hour Oxygen plasma, 350 W, 780 mTorr	Wafers: #7-12
15	Topography Measurement	Dektak 8000	Step height measurement, 5 points / per wafer	Wafers: #7-12
16	Oxide Stripe & Pre-oxidation Clean	Wet Bench	1. BOE (4:1) etch 10 min 2. RCA1 70 °C 15min 3. DI water rinse 4. Wafer drying	All wafers: #1-12
17	Thermal Oxidation	Furnace Tube 10	Grow 1.0 μm thermal oxide Recipe: wetox11 Time: 2:30:00	Wafers: #1-12
18	Oxide Thickness Measurement	Nanospec	Thickness measurement	Wafers: #1-12

Step	Process	Tools	Description	Comments
19	Pre-metallisation Clean	Wet Bench	1. RCA1 70 °C 15min 2. DI water rinse 3. Wafer drying	Wafers #1-12 (Optional)
20	Aluminium Deposition	Balzers Sputter	Deposition 1.0 μm Al (4-point metal thickness measurement after deposition)	Wafers: #1-12.
21	Lithography Process	5× Stepper Optimetrix	Mask ID: TopMetal Coating: 1,1,1 Develop: 1,1,1 Expose: 5× Stepper (Stepper mask should be aligned to Karl Suss align mark from MASK A)	Top wafers: #1-6 (Frontside)
22	Lithography Process	5× Stepper Optimetrix	Mask ID: BottomMetal Coating: 1,1,1 Develop: 1,1,1 Expose: 5× Stepper (Stepper mask should be aligned to Karl Suss align mark from MASK B)	Bottom wafers: #1-6 (Frontside)
23	Aluminium Etch	STS RIE Metal Etcher	1.0 μm aluminium etching Recipe: Al3in Time: 10 min	All wafers
24	Photoresist Strip	Asher	Time: 1 hour Oxygen plasma, 350 W, 780 mTorr	All wafers
25	Topography Measurement	Dektak 8000	Step height measurement, 5 points / per wafer	All wafers
26	Al Sintering	Furnace Tube 8	Temperatures: 435 °C, H_2/N_2 mixed gas flow, 15 min	All wafers
27	PECVD Oxide Deposition	STS PECVD Multiplex	Deposit 2.0 μm PECVD oxide Recipe: HFSIO Time: 50 min	All wafers
28	Oxide Thickness Measurement	Nanospec	Thickness measurement, 5 points / per wafer	All wafers
29	PECVD Oxide Densification	Furnace Tube 8	Wafer annealing: 435 °C with N_2 flow for 16 hours	All wafers
30	Topography Measurement	Dektak 8000	Step height measurement, 5 points / per wafer	All wafers
31	Oxide CMP	Presi Polisher	Topography and roughness removal	Patterned wafers: (Frontside)
32	Post-CMP Cleaning	Mask Scrubber and Wet Bench	1. TMAH 10% 5 min 2. Mask scrubber: both sides 3. DI water rinse 4. Marangoni drier	All polished wafers
33	Oxide Thickness Measurement	Nanospec	Thickness measurement, 5 points / per wafer	All wafers
34	Topography Measurement	Dektak 8000	Step height and wafer bow measurement	All wafers
35	Pre-bonding Chemical Treatment	Wet Bench and VacTech	1. O_2 plasma treatment 2. DI water rinse 3. Wafer drying	All wafers
36	Wafer Bonding	Karl Suss	Room temperature bonding	All wafers

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Step	Process	Tools	Description	Comments
37	Post-bonding Annealing	Furnace Tube 8	200 – 450 °C with N_2 flow Time: 2 – 100 hours	All bonded pairs
38	Infra-red Transmission Inspection	IR camera	Interface voids inspection	All bonded pairs
39	Dicing & sawing	Disco saw	10 × 10 mm squares prepared from the bonded wafers	Optional for selected bonded pairs!
40	Bonding Strength Measurement	M30K tensile test machine	Wafer bonding strength measurement	Selected chips (Optional)
41	Oxide Etch	Plasma-Therm	1 – 1.2 μm thermal oxide etch	Etch oxide on the backside of the bonded pairs
42	Wafer Thinning	ICP Etcher	Bulk silicon substrate etching	Silicon substrate removal, stop at oxide layer
43	Oxide CMP	Presi Polisher	Topography and roughness removal	Thinned wafers (Optional!)
44	Post CMP Cleaning	Mask Scrubber and Wet Bench	1. TMAH 10% 5 min 2. Mask scrubber: both sides 3. DI water rinse 4. Marangoni Drier	All polished wafers (Optional!)
45	Lithography Process	5× Stepper Optimetrix	Mask ID: Pad Mask Coating: SPR220-7, 3000 rpm, 7 μm Develop: MF-26A, 1 min 30 sec Expose: 5× Stepper, 3500 ms	Thinned wafers
46	Oxide Etch	Plasma-Therm	3.5 – 4.0 μm oxide etching Recipe: Oxide-Etch Time: TBD	Thinned wafers (10-15% over etch ensure electrical contact)
47	Photoresist Strip	Asher	Time: 1 hour Oxygen plasma, 350 W, 780 mTorr	Thinned wafers
48	Aluminium Deposition	Balzers Sputter	Deposition 1.5 – 2.0 μm Al	Thinned wafers
49	Al CMP	Presi Polisher	Al Damascene Process	Thinned wafers: Al Damascene CMP
50	Post CMP Cleaning	Mask Scrubber and Wet Bench	1. Detergent clean 2. Mask scrubber: both sides 3. DI water rinse 4. Marangoni drier	All polished wafers
51	Electrical Testing	Probe Station	Resistivity measurement	All polished wafers

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MEMS-CMOS Integration (Direct Metal Contact Approach)

Batch number: HL060606-2	Starting material: 3", n-type, <100>, Si test
Number of wafers: 12	wafer

Step	Process	Tools	Description	Comments
1	Thermal Oxidation	Furnace Tube 10	Grow 2 KÅ thermal oxide Recipe: wetox11 Time: 00:50:00	All wafers
2	Oxide Thickness Measurement	Nanospec	Thickness measurement	All wafers
3	Lithography Process	Karl Suss	Mask ID: Mask A (for bond align) Coating: 1,1,1 Develop: 1,1,1 Expose: Karl Suss	Top wafers: #1-6 (Frontside)
4	Lithography Process	Karl Suss	Mask ID: Mask B (for bond align) Coating: 1,1,1 Develop: 1,1,1 Expose: Karl Suss	Bottom wafers: #7-12 (Frontside)
5	Oxide Etch	Plasma-Therm	2 KÅ oxide etching Recipe: Oxide-Etch Time: 10 min	All wafers #1-12 (Frontside)
6	Si Etch	STS ICP Etcher	2.0 μm silicon etching Recipe: Scuba6 Time: 3 min	All wafers #1-12 (Frontside)
7	Photoresist Strip	Asher	Time: 1 hour Oxygen plasma, 350 W, 780 mTorr	Wafers: #1-12
8	Topography Measurement	Dektak 8000	Step height measurement, 5 points / per wafer	Wafers: #1-12
9	Oxide Etch	Plasma-Therm	2 KÅ oxide etching Recipe: Oxide-Etch Time: 10 min	Bottom wafers: #7-12 (Backside)
10	Silicon CMP	Presi Polisher	Wafer backside polishing for smooth surface	Bottom wafers: #7-12 (Backside)
11	Post CMP Cleaning	Mask Scrubber and Wet Bench	1. TMAH 10% 5 min 2. Mask scrubber: both sides 3. DI water rinse 4. Marangoni drier	Bottom wafers: #7-12
12	Lithography Process	Karl Suss	Mask ID: Mask C (for bond align) Coating: 1,1,1 Develop: 1,1,1 Expose: Karl Suss	Bottom wafers: #7-12 (Backside)
13	Si Etch	STS ICP Etcher	2.0 μm silicon etching Recipe: Scuba6 Time: 3 min	Bottom wafers: #7-12 (Backside)
14	Photoresist Strip	Asher	Time: 1 hour Oxygen plasma, 350 W, 780 mTorr	Bottom wafers: # 7-12
15	Topography Measurement	Dektak 8000	Step height measurement, 5 points / per wafer	Bottom wafers: #7-12 (Backside)
16	Oxide Stripe & Pre-oxidation Clean	Wet Bench	1. BOE (4:1) etch 10 min 2. RCA1 70 °C 15min 3. DI water rinse 4. Wafer drying	All wafers #1-12
17	Thermal Oxidation	Furnace Tube 10	Grow 2.2 μm thermal oxide Recipe: wetox14 Time: 2:30:00	Wafers: #1-12
18	Oxide Thickness Measurement	Nanospec	Thickness measurement	Wafers: #1-12

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Step	Process	Tools	Description	Comments
19	Lithography Process	5× Stepper Optimetrix	Mask ID: TopMetal Coating: 1,1,1 Develop: 1,1,1 Expose: 5× Stepper (Stepper mask should be aligned to Karl Suss align mark from MASK A)	Top wafers: #1-6 (Frontside)
20	Lithography Process	5× Stepper Optimetrix	Mask ID: BottomMetal Coating: 1,1,1 Develop: 1,1,1 Expose: 5× Stepper (Stepper mask should be aligned to Karl Suss align mark from MASK B)	Bottom wafers: #7-12 (Frontside)
21	Oxide Etch	Plasma-Therm	1.0 – 1.2 μm oxide etching Recipe: Oxide-Etch Time: 30 min	Wafers: #1-12 (Frontside)
22	Oxide Thickness Measurement	Nanospec	Remaining oxide thickness measurement	Wafers: #1-12
23	Photoresist Strip	Barrel asher	Time: 1 hour Oxygen plasma, 350 W, 780 mTorr	Wafers: #1-12
24	Topography Measurement	Dektak 8000	Step height measurement, 5 points / per wafer	Wafers #1-12
25	Pre-Metallisation Clean	Wet Bench	1. RCA1 70 °C 15min 2. DI water rinse 3. Wafer drying	Wafers #1-12 (Optional)
26	Aluminium Deposition	Balzers Sputter	Deposition 1.5 μm Al 4-point probe measurement	Wafer: #1-12
27	Al CMP	Presi Polisher	Al Damascene CMP	Patterned wafers: #1-12
28	Post CMP Cleaning	Mask Scrubber and Wet Bench	1. Detergent clean 5 min 2. Mask scrubber: both sides 3. DI water rinse 4. Marangoni drier	All polished wafers
29	Oxide Thickness Measurement	Nanospec	Thickness measurement	All wafers
30	Topography Measurement	Dektak 8000	Step height measurement, 5 points / per wafer	All wafers
31	CMP Dishing Measurement	AFM		Selected wafers
32	Pre-Bonding Chemical Treatment	Wet Bench VacTech	1. O₂ plasma treatment 2. DI water rinse 3. Wafer drying	All wafers
33	Bonding	Karl Suss	Room temperature wafer bonding	All wafers
34	Post-Bonding Annealing	Furnace	Temperature: 200 – 450 °C Time: 2 – 100 hours	All bonded pairs
35	Infra-red transmission	IR camera	Interface voids inspection	All bonded pairs
36	Bonded wafer dicing	Disco saw	10 × 10 mm squares prepared from the bonded wafers	Some bonded wafer pairs (optional)
37	Tensile bond strength measurement	M30K tensile test machine	Wafer bonding strength measurement	Selected chips (optional)

Step	Process	Tools	Description	Comments
38	Oxide Etch	Plasma-Therm	1.0 – 2.0 µm thermal oxide etch	Etch oxide on the backside of the bonded pairs
39	Wafer Thinning	STS ICP Etcher	Bulk silicon substrate etching	Silicon substrate removal, stop at oxide layer
40	Oxide CMP	Presi Polisher	Topography and roughness removal	Thinned wafers (Optional!)
41	Post CMP Cleaning	Mask Scrubber and Wet Bench	1. TMAH 10% 5 min 2. Mask scrubber: both sides 3. DI water rinse 4. Marangoni Drier	All polished wafers (Optional!)
42	Lithography Process	5× Stepper Optimetrix	Mask ID: Pad Mask Coating: 1,1,1 Develop: 1,1,1 Expose: 5× Stepper	Thinned wafers
43	Oxide Etch	Plasma-Therm	1.0 – 2.0 µm oxide etching Recipe: Time:	Thinned wafers (10-15% over etch ensure electrical contact)
44	Photoresist Strip	Barrel asher	Time: 1 hour Oxygen plasma, 350 W, 780 mTorr	Thinned wafers
45	Aluminium Deposition	Balzers Sputter	Deposition 1.5 µm Al	Thinned wafers
46	Al CMP	Presi Polisher	Al damascene process	Thinned wafers
47	Post CMP Cleaning	Mask Scrubber and Wet Bench	1. Detergent clean 5 min 2. Mask scrubber: both sides 3. DI water rinse 4. Marangoni drier	All polished wafers
48	Electrical Testing	Probe Station	Resistivity measurement	All polished pairs

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Appendix B
Raphael Simulation Data Files

Raphael simulation has been used to characterise test structures for measuring the contact resistance between two conductive layers. This section presents the program codes used for the kelvin structure and stacked Greek cross structure.

Raphael simulation code for Kelvin structure

```
* RC3
* Kelvin contact resistance structure
* Dc = wire thickness, Dr = "contact" thickness
PARAM Dc=1.5 Dr=0 D1=Dc+Dr Dt=2*Dc+Dr
* Wc = line width, Lc = Cross arm length
PARAM Wc=3 Lc=2*Wc
* Wt = total simulation size
PARAM Wt=2*Lc+Wc
* x and y coordinates
PARAM x1=0 x2=Lc x3=Lc+Wc x4=Wt
PARAM y1=0 y2=Lc y3=Lc+Wc y4=Wt
* electrode size
PARAM Es=0.5
* simulation area limits
PARAM xmax=Wt+Es ymax=Wt+Es xmin=0-Es ymin=0-Es
PARAM zmin=0 zmax=Dt


* Defines simulation area as insulator
POLY3D NAME=WIN COORD=xmin,ymin;xmin,ymax;xmax,ymax;xmax,ymin; HEIGHT=Dt DIEL=1
color=1


* Metal arms of the structure, rho value is copper material resistivity
POLY3D NAME=aluminium COORD=x1,y2;x3,y2;x3,y3;x1,y3; HEIGHT=Dc rho=2.65e-8 color=3
POLY3D NAME=aluminium COORD=x2,y2;x3,y2;x3,y4;x2,y4; HEIGHT=Dc rho=2.65e-8 color=3

POLY3D NAME=aluminium COORD=x2,y1;x3,y1;x3,y3;x2,y3; v1=0,0,D1 HEIGHT=Dc
rho=2.65e-8 color=4
POLY3D NAME=aluminium COORD=x2,y2;x4,y2;x4,y3;x2,y3; v1=0,0,D1 HEIGHT=Dc
rho=2.65e-8 color=4


* resistive contact, commented out if Dr is zero.
*POLY3D NAME=contact COORD=x2,y2;x3,y2;x3,y3;x2,y3; v1=0,0,Dc HEIGHT=Dr
rho=1e-6 color=4


* Electrodes, two set as very low resistance material, one set to one volt
* and other set to zero volt
POLY3D NAME=e1 COORD=xmin,y2;x1,y2;x1,y3;xmin,y3; HEIGHT=Dc rho=1e-12 color=3
POLY3D NAME=e2 COORD=x2,y4;x3,y4;x3,ymax;x2,ymax; HEIGHT=Dc VOLT=1 color=3
POLY3D NAME=e3 COORD=x4,y2;xmax,y2;xmax,y3;x4,y3; v1=0,0,D1 HEIGHT=Dc rho=1e-12
color=4
POLY3D NAME=e4 COORD=x2,ymin;x3,ymin;x3,y1;x2,y1; v1=0,0,D1 HEIGHT=Dc VOLT=0
color=4


* Commands extract voltages at the two resistive electrodes. e4, e2
EXTRACT X1=Wt/2 Y1=ymin Z1=D1+Dc/2
EXTRACT X1=Wt/2 Y1=ymax Z1=Dc/2


* Declare simulation window
WINDOW3D V1=xmin,ymin,zmin V2=xmax,ymax,zmax DIEL=1


*Set up simulation options like number of grid points FAC_REGRID=2 GRID_SLIP=1e-12
OPTIONS UNIT=1e-6 SET_GRID=60000 MAX_REGRID=0


* Simulation command extracts current at the electrodes with fixed voltages
CURRENT
```

Raphael simulation code for stacked Greek cross structure

```
* RC3
* Alternative bonded contact resistance structure
* Dc = wire thickness, Dr = "contact" thickness
PARAM Dc=1.5 Dr=0 D1=Dc+Dr Dt=2*Dc+Dr
* Wc = line width, Lc = Cross arm length
PARAM Wc=3 Lc=2*Wc
* Wt = total simulation size
PARAM Wt=2*Lc+Wc
* x and y coordinates
PARAM x1=0 x2=Lc x3=Lc+Wc x4=Wt
PARAM y1=0 y2=Lc y3=Lc+Wc y4=Wt
* electrode size
PARAM Es=0.5
* simulation area limits
PARAM xmax=Wt+Es ymax=Wt+Es xmin=0-Es ymin=0-Es
PARAM zmin=0 zmax=Dt

* Defines simulation area as insulator
POLY3D NAME=WIN COORD=xmin,ymin;xmin,ymax;xmax,ymax;xmax,ymin; HEIGHT=Dt DIEL=1
color=1

* Metal arms of the structure, rho value is copper material resistivity e1 e3
POLY3D NAME=aluminium COORD=x1,y2;x3,y2;x3,y3;x1,y3; HEIGHT=Dc rho=2.65e-8 color=3
POLY3D NAME=aluminium COORD=x2,y2;x4,y2;x4,y3;x2,y3; HEIGHT=Dc rho=2.65e-8 color=3

*Metal arms e4 e2
POLY3D NAME=aluminium COORD=x2,y1;x3,y1;x3,y3;x2,y3; v1=0,0,D1 HEIGHT=Dc
rho=2.65e-8 color=4
POLY3D NAME=aluminium COORD=x2,y2;x3,y2;x3,y4;x2,y4; v1=0,0,D1 HEIGHT=Dc
rho=2.65e-8 color=4

* Resistive contact, commented out if Dr is zero.
*POLY3D NAME=contact COORD=x2,y2;x3,y2;x3,y3;x2,y3; v1=0,0,Dc HEIGHT=Dr rho=3e-2
color=4

* Contact interfaces.
*POLY3D NAME=contact COORD=x2,y2;x3,y2;x3,y3;x2,y3; v1=0,0,Dc HEIGHT=D3
rho=2.65e-2 color=4
*POLY3D NAME=contact COORD=x2,y2;x3,y2;x3,y3;x2,y3; v1=0,0,D1 HEIGHT=D3
rho=2.65e-2 color=4


* Electrodes, two set as very low resistance material, one set to one volt
* and other set to zero volt
POLY3D NAME=e1 COORD=xmin,y2;x1,y2;x1,y3;xmin,y3; HEIGHT=Dc VOLT=1.0 color=3
POLY3D NAME=e2 COORD=x2,y4;x3,y4;x3,ymax;x2,ymax; v1=0,0,D1 HEIGHT=Dc VOLT=0
color=4
POLY3D NAME=e3 COORD=x4,y2;xmax,y2;xmax,y3;x4,y3; HEIGHT=Dc rho=1e-12 color=3
POLY3D NAME=e4 COORD=x2,ymin;x3,ymin;x3,y1;x2,y1; v1=0,0,D1 HEIGHT=Dc rho=1e-12
color=4

* Commands extract voltages at the two resistive electrodes.
EXTRACT X1=xmax Y1=Wt/2 Z1=Dc/2
EXTRACT X1=Wt/2 Y1=ymin Z1=Dr+Dc/2+Dc

* Declare simulation window
WINDOW3D V1=xmin,ymin,zmin V2=xmax,ymax,zmax DIEL=1

*Set up simulation options like number of grid points GRID_SLIP=1e-12
OPTIONS UNIT=1e-6 SET_GRID=60000 MAX_REGRID=0

* Simulation command extracts current at the electrodes with fixed voltages
CURRENT
```

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