

Characterisation of organometallic materials for IC processes

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A thesis submitted for the degree of Doctor of Philosophy

The University of Edinburgh
July 2004



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Abstract

DUE to their low resistivity, metals have been a subject of great interest in semiconductor manufacturing, primarily for use as a material for interconnects. Besides, the continuous reduction of feature sizes on silicon based integrated circuits is expected to cause a switch from silicide gates on silicon dioxide to metal gates on advanced dielectrics.

The shrinking of semiconductor structures and emerging new technologies demand for new metallisation processes which overcome the limitations of existing solutions and meet new requirements.

This thesis reports on the characterisation of platinum features which were deposited and patterned using UV (ultra violet) exposure of a solid photosensitive organometallic material through a mask. The work aims to evaluate the process for its use in present and future semiconductor technology.

A range of devices including resistive and capacitive test structures as well as MOS transistors were produced using platinum deposited by the organometallic process and characterised by standard methods. The deposited films were found to be metallic and have a good adhesion to silicon dioxide, although their resistivity is higher than the one of bulk platinum. Measurements on platinum MOS capacitors showed their capacitance curves to agree well with curves from aluminium capacitors on the same substrate albeit the curves of capacitors on chips which incorporated MOS transistors indicated interface traps. Threshold and source-drain characteristics of platinum gate transistors are presented and these results are compared with aluminium gate transistors manufactured on the same substrate. Both sets of characteristics are very similar with the major difference being that the platinum gate devices have a lower sub-threshold slope, an effect which was attributed to trap charges at the silicon/silicon dioxide interface. The work also found that structures produced were generally larger than expected and spectroscopy methods showed contaminants to be present in the films.

The findings of this research indicate that many properties of the platinum films reported herein are superior to those of films deposited by similar means found in the literature. However, the work also identified problems concerning the microstructure of the films and accurate control of feature size which need to be solved before the films can be integrated into a modern semiconductor process.

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Acronyms and abbreviations

AES	Auger Electron Spectroscopy
AFM	Atomic Force Microscopy
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
COD	Cycloocta-1,5-diene
EOT	Equivalent Oxide Thickness
FET	Field Effect Transistor
HOMO	Highest Occupied Molecular Orbital
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
JFET	Junction Field Effect Transistor
LUMO	Lowest Unoccupied Molecular Orbital
MEMS	Microelectromechanical Systems
MIS	Metal Insulator Semiconductor
MOS	Metal Oxide Semiconductor
MPU	Mathematical Processing Unit
PVD	Physical Vapour Deposition
SOI	Silicon On Insulator
TLM	Transmission Line Model
UV	Ultra Violet
VLSI	Very Large-Scale Integration
XPS	X-ray Photoelectron Spectroscopy

Nomenclature

C	Capacitance
C_{FB}	Flatband capacitance
C_{it}	Interface trap charge
C_{max}	Maximum capacitance
C_{min}	Minimum capacitance
C_{Ox}	Oxide capacitance
C_S	Depletion layer capacitance
E_C	Minimum energy of an electron in the conduction band
E_F	Fermi energy
E_i	Intrinsic Fermi energy
E_M	Metal Fermi energy
E_0	Vacuum energy
E_V	Maximum energy of an electron in the valence band
F_S	Electrical field at the silicon surface
h	Plank's constant
I_D	Drain current
k	Boltzmann constant
L	Transistor gate length
n	Electron concentration
n_S	Electron concentration at the silicon surface
N_A	Acceptor density
N_D	Donor density
p	Hole concentration
p_S	Electron concentration at the silicon surface
Q_D	Depletion layer charge
Q_f	Oxide fixed charge
Q_I	Inversion layer charge
Q_{it}	Interface trapped charge
Q_m	Mobile ionic charge
Q_O	Oxide charge
Q_{ot}	Oxide trapped charge
Q_S	Surface charge
q	Electron charge
t	Time
t_{Ox}	Oxide thickness

T	Temperature
V_{FB}	Flatband voltage
V_G	Gate voltage
V_{Ox}	Oxide voltage
V_{TH}	Threshold voltage
w	Depletion layer width
w_{max}	Maximum depletion layer width
W	Transistor gate width
ϵ_0	Vacuum permittivity
ϵ_{Ox}	Oxide permittivity
ϵ_{Si}	Silicon permittivity
λ_n	Debye length (for n-type material)
λ_p	Debye length (for p-type material)
μ	Mobility
ρ	Charge density
ϕ	Potential between Fermi level and intrinsic Fermi level
ϕ_B	Bulk potential
ϕ_M	Metal workfunction
ϕ_{MS}	Workfunction difference
ϕ_S	Surface potential
ϕ_{Si}	Silicon workfunction
ψ	Band bending
ψ_S	Band bending at the silicon surface

Preface

THIS thesis is the result of my studies for a PhD degree from the University of Edinburgh in Scotland (UK). It is based on work done between August 2000 and July 2004 at the Institute for Micro- and Nanosystems at the Scottish Microelectronics Centre in Edinburgh which has partly been published in two conference papers [1, 2] and a journal paper [3].

Outline of the thesis

This thesis can roughly be divided into three main parts. The first part, the introductory chapters, consists of an introduction and a review of semiconductor processes. Part two, the experimental part, includes descriptions of the organometallic process and the manufacturing of the test structures, together with chapters regarding the measurements. The thesis finishes with a chapter concluding this research and giving details about possible future work.

Throughout the thesis, special care has been placed upon the consistent use of nomenclature and abbreviations, the excellent book about the MOS transistor by Tsividis [4] was hereby taken as an example. The nomenclature used corresponds widely with the one used by Nicollian and Brews in their standard reference book on the MOS capacitor [5] and was extended to the MOS transistor.

The figures in the thesis were deliberately kept simple. However, this means that silicon dioxide layers produced by oxidation, for example, are represented by a layer on top of the silicon substrate and it is not shown that silicon is consumed into the oxide during this process. Also, rectangles were used to draw structures and rounded shapes only employed where they were necessary for better understanding.

In the following, the chapters of this dissertation are briefly outlined.

Chapter one. In chapter one a brief introduction is given and the motivation and the objectives of this work are described.

Chapter two. The second chapter of this thesis starts with the historical background to this work, explaining not only the development of semiconductor processes and devices in the past but also giving an outlook into the future. The process steps involved in the manufacturing of modern integrated circuits are described and problems likely to arise are extracted from the ITRS 2003 (International Technology Roadmap for Semiconductors 2003) [6]. It is then focused onto the use of organometallic materials and platinum in semiconductor processing, which are areas of special interest for this project.

Chapter three. Chapter three explains the chemistry of the organometallic material which includes the bonding mechanisms holding the molecule together and the photochemical process which makes this particular compound so useful. Also, the organometallic process is described and platinum structures produced are shown.

Chapter four. Chapter four delineates the design and manufacturing of two test chips, both of which were used for the measurements in the following chapters.

Chapter five. The fifth chapter deals with resistive and dimensional measurements. It starts with the theory necessary to understand resistive test structures as well as mechanisms responsible for the resistance of thin films. Electrical linewidth measurements are then explained and results are shown.

Chapter six. The voltages at the MOS stack and the theory around the capacitance of a MOS structure are introduced in chapter six. The extraction of parameters from C-V curves is described and results obtained from capacitance measurements at capacitors produced using the organometallic process are presented.

Chapter seven. Chapter seven begins by explaining AES (Auger Electron Spectroscopy) and XPS (X-ray Photoelectron Spectroscopy). Spectres obtained using this characterisation methods are then shown, evaluated and the results discussed.

Chapter eight. The characterisation of transistors with a gate manufactured using the organometallic process is reported in chapter eight. Besides, formulas describing the MOS transistor are developed and a model derived which is used for fitting curves to the ones obtained from the transistors manufactured.

Chapter nine. The final chapter reviews the whole thesis in brief, discusses the results and their implications on the state of the art. Besides, possible future work is proposed.

Acknowledgements

I would, of course, not have been able to finish this thesis, had it not been for the help of others.

First of all, I wish to thank my supervisor Anthony Walton for suggesting this work and his guidance throughout the project. I would also like to express gratitude to AMCET Ltd for funding two years of my PhD and Hansjörg Wirz for providing a reference which made this study in Edinburgh possible. I am also deeply in debt to all the people at the Scottish Microelectronics Centre and at the University of Dundee for their valuable suggestions, the synthe-

sis of the organometallic material and help with the processing of the test structures which I characterised during my work. Beside others, I would particularly like to thank Gareth Broxton, Alan Gundlach, Tom Stevenson and James Thomson who were greatly involved in this project and all spent a considerable amount of time helping me with my tasks.

I am especially indebted to the people who provided the social environment at my working place by being good friends, company during the coffee breaks and participants at events outside the university, namely Stefan Enderling, Natalie Plank, Louise Teo, Huamao Lin and Yifan Li from the ranks of the PhD students and Liudi Jiang, a post-doc.

There were also people not directly associated with the project or the Scottish Microelectronics Centre who I would like to mention. First of all, I would like to thank my wife Nanako for her tolerance during the final year of my studies. I do not know how many times we had to change our plans due to delays with my experiments. I also gratefully recognise my family and friends in Switzerland and Japan, who supported me very well and provided something like a backbone by letting me know that I could always count on their help. A special thank goes to Shinya Katsumata who started his PhD studies at the same time as I and was a fast friend over the whole four years.

Besides the people, there were also tools and things which did their part in helping me accomplish my tasks. The toolset that was available at the SMC provided the opportunity to undertake this work but at the same time presented a challenge in terms of both its operation and maintenance. The Sun workstation running Solaris which occupied big parts of my desk always provided the computing power I needed to do my work. I also want to thank Google (<http://www.google.com>) for its great search results and Leo (<http://dict.leo.org>) for its translations between German and English which helped to solve many language problems. Finally, there was Matlab which automated the creation of graphs and \LaTeX which proofed to be the perfect tool to write this thesis.

Declaration of originality

I hereby declare that the research recorded in this thesis is my own work, unaided except where otherwise acknowledged in the text, and the thesis itself was composed entirely by myself in the School of Engineering and Electronics at the University of Edinburgh. This work has not been submitted for any other degree or professional qualification.

Introduction

Contents

1.1	Motivation	1
1.2	Scope and objectives of this work	3

FEW discoveries had an impact on our modern life as the one imposed by semiconductors. Semiconductor and especially silicon technology lies at the core of the majority of computer systems today and made the Internet possible. The silicon industry is of immense proportions and often used as an indicator for the state of the world economy. It is therefore not surprising that a lot of research is undertaken in the field of semiconductors, allowing this sector of industry to maintain a very high speed in which new technologies are developed.

Figure 1.1 and Figure 1.2 show the present state of the art by depicting a PowerPC 970 processor developed by IBM [7]. Its circuitry incorporates 52 million transistor on a 118 mm^2 die and it is manufactured on 300 mm wafers using $0.13 \text{ }\mu\text{m}$ SOI (Silicon On Insulator) technology with eight layers of copper interconnect.

1.1 Motivation

In early integrated circuits based on MOS (Metal Oxide Semiconductor) structures, metals were used for both, gates and interconnects. Later, the metal for the gates was replaced by polysilicon and silicides, thus allowing the channel to be formed using the self-aligned process described later in Chapter 3. However, it was forecasted [6] that in the near future, metals will be used again for gates. The reasons for this are, among other things, the low resistivity of metals compared to polysilicon, the various workfunctions of different metals and their compatibility with novel dielectrics. There are, however, drawbacks linked to the use of metals. First of all, many metals have low melting points or form silicide when in contact with silicon at temperatures as low as $250 \text{ }^\circ\text{C}$, making a high-temperature step impossible to follow the metal deposition. Another difficulty is the deposition and patterning of metals which is more complicated than the one of materials commonly used in present-day semiconductor processing.

Despite the problems likely to arise with the use of metals, the replacement of silicon based gate materials by metals seems to be inevitable and it is therefore of high interest to find

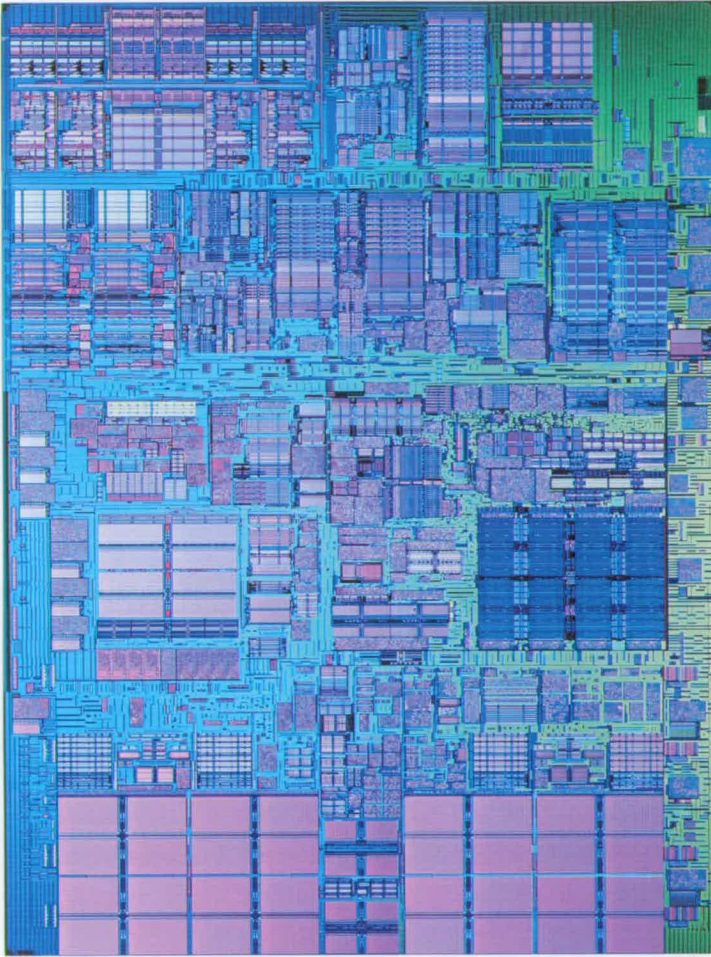


Figure 1.1: Photograph of IBM's PowerPC 970 which is used as processor in Apple's G5 computers [7]. The chip size is 118 mm^2 .

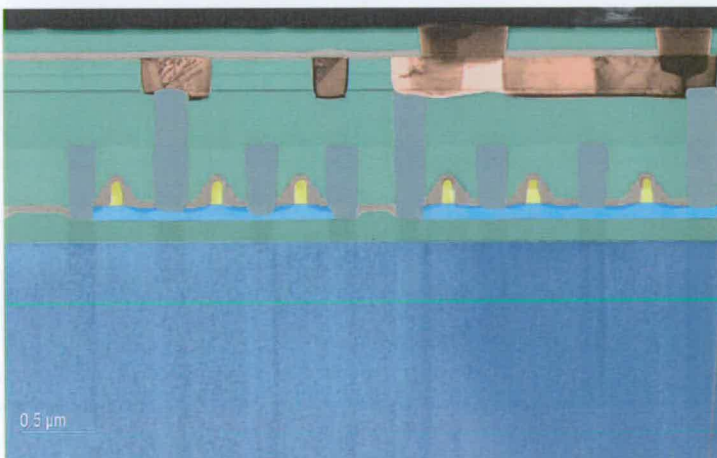


Figure 1.2: Cross section showing the transistor level and one layer of copper interconnect of a PowerPC 970 chip [7].

new processes to deposit and pattern metals which comply with modern integrated circuit manufacturing methods.

1.2 Scope and objectives of this work

This research looks at a new process to deposit patterned platinum layers by UV (ultra violet) light exposure of a solid organometallic material. A platinum compound was chosen because it was the only material available at the start of this work. It is possible to produce organometallics based on other metals, some of which possess properties superior to the ones of platinum.

In conventional semiconductor processes, a patterned metal layer can be produced using the steps shown in Figure 1.3(a). It starts with the deposition of a metal layer on a substrate and putting photoresist on top of it. The photoresist is then exposed and developed and used as a mask to etch the metal. Finally, the photoresist is removed thus leaving behind the metal features.

The organometallic process depicted in Figure 1.3(b) works in a very different way and can be divided into three main parts, namely deposition, exposure and heat treatment. The solid organometallic compound can be spun onto a substrate or deposited using methods like PVD (Physical Vapour Deposition) and sputtering. After the deposition, the layer of organometallic material is exposed using either UV, e-beam or ion-beam lithography. The material behaves like a negative resist and therefore requires a dark field mask for exposure. To finalise the process, the unexposed organometallic material and organic residue are removed using a three-stage heat treatment. The three stages perform different tasks in defining and purifying the metal and are conducted at different temperatures in air or in a hydrogen/nitrogen environment (for a detailed description see Chapter 3). A Greek cross structure [8] made of platinum manufactured from an organometallic material is shown in Figure 1.4(a) and an AFM (Atomic Force Microscopy) image of one of the arms in Figure 1.4(b).

It can be seen that the organometallic process requires less process steps and works without etch steps or solvents, which is favourable from a manufacturing viewpoint.

This thesis investigates the integration of an organometallic compound into the manufacturing process of semiconductor structures. The organometallic materials and associated processes were developed at the University of Dundee under the direction of James Thomson. Throughout the project, parts of the experiments closely related to the organometallic process were performed in collaboration with researchers at the University of Dundee who also synthesised and supplied the organometallics. The work reported herein concerns itself with the application of organometallic compounds and deals only briefly with their chemistry. The design and production of test chips with standard semiconductor test structures as well as MOS transistors are described and their characterisation explained. The results are

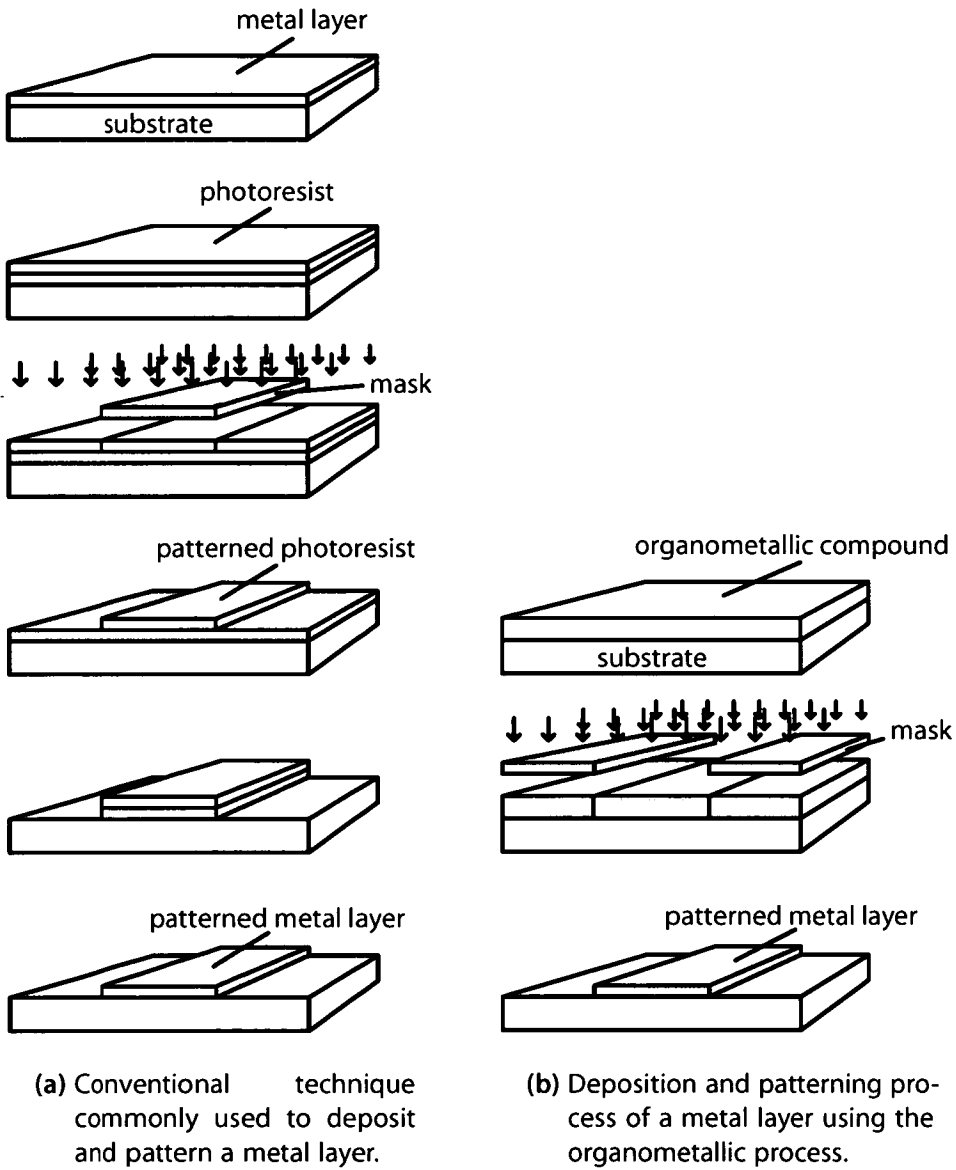
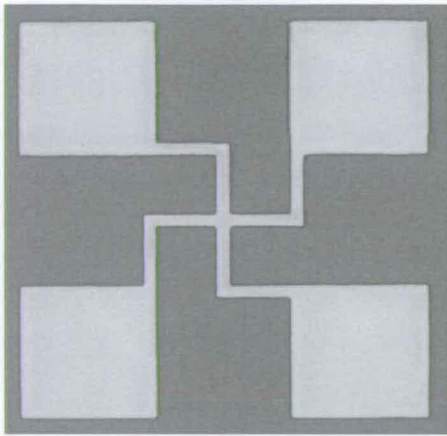
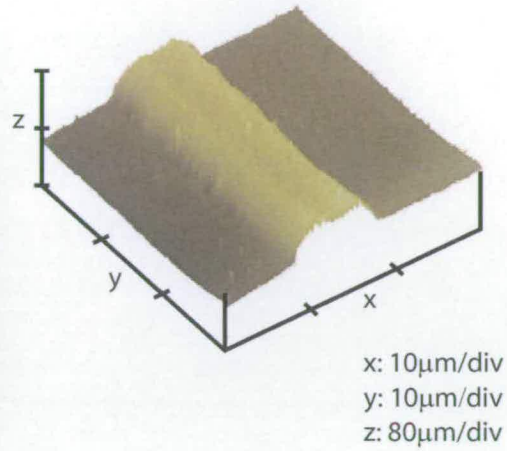


Figure 1.3: Comparison of conventional and organometallic process.



(a) Image taken with a microscope.



(b) AFM picture of one of the arms.

Figure 1.4: A Greek cross test structure produced using UV exposure of a solid organo-metallic material.

then used to evaluate the suitability of the organometallic process for the manufacturing of present and future integrated circuits, which is the main objective of this work.

Historical background and review of subject

2

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THIS chapter gives an introduction to semiconductor processes and provides an outlook on future technologies and arising challenges. First, some semiconductor devices are described in order to facilitate the understanding of the following sections concerning process technology. Here, emphasis is placed on areas which are of importance to this project, namely gate materials and interconnect technology. The use of organometallic materials and platinum in semiconductor processing are then examined thus further focusing on the topic of this work which deals with platinum films deposited from an organometallic material.

A lot of the historical information found in this chapter is based on the book written by Plummer et al. [9].

2.1 Semiconductor devices

The PN diode is the simplest semiconductor device and was one of the earliest semiconductor devices developed. A PN diode can be produced by bringing a n-type semiconductor material in contact with a p-type one.

The bipolar transistor was invented by Bardeen and Brattain in December 1947 at Bell Laboratories [10]. It was built using the point contact method and is shown in Figure 2.1. Soon

afterwards, Shockley developed the theory behind the function of the bipolar transistor [11]. The bipolar transistor was the most important semiconductor device in early integrated circuits but was later replaced by the field effect transistor. Most of modern integrated circuits are based on the field effect transistor but the bipolar transistor is still used for high-speed logic and other special applications.

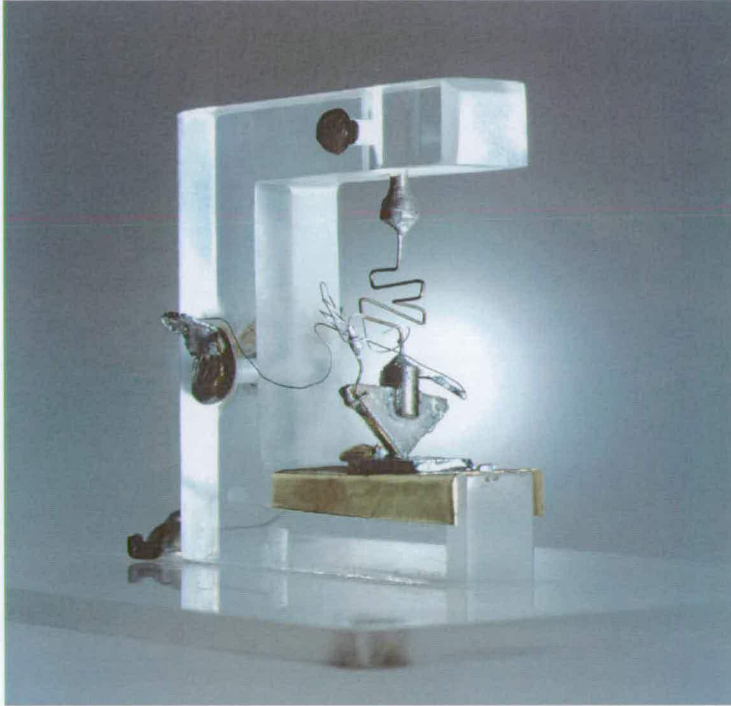


Figure 2.1: The first bipolar transistor as it was built by Bardeen and Brattain at Bell Laboratories [12].

Although the basic principle and structure of the field effect transistor was reported earlier, the first transistor taking advantage of the field effect was not built until 1953 when the JFET (Junction Field Effect Transistor) was invented [13] whose theory was developed a year earlier by Shockley [14]. A MIS (Metal Insulator Semiconductor) structure was reported in 1959 [15] and a working MOS (Metal Oxide Semiconductor) transistor was demonstrated in 1960 [16, 17].

Since then, the basic structure of the transistor depicted in Figure 2.2 did not change significantly, although modern devices are the product of lots of scaling (see Section 2.2.4) and, according to the ITRS 2003 (International Technology Roadmap for Semiconductors 2003) [6], the physical gate length of a transistor of a MPU (Mathematical Processing Unit) will be 28 nm by the year 2006.

Recently, emerging problems with further scaling led to lots of research into new devices. One of the main issues are short channel effects which appear when the depletion layer width

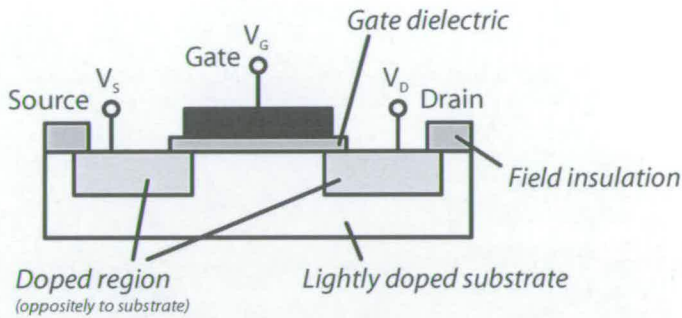


Figure 2.2: Typical structure of a MOS transistor.

of the source and drain junctions becomes comparable to the channel length. This causes the potential distribution in the channel to be dependent on both the gate and the drain voltage, thus changing the device behaviour. Short channel effects can be minimised by strictly sticking to the scaling rules described in Section 2.2.4 but shrinking device dimensions will in the near future make it difficult to follow these rules. Two of the main reasons for this are very shallow junctions and ultrathin oxide layers. Former are difficult to manufacture while very thin oxide layers lead to high leakage currents due to direct tunneling.

The double gate transistor shown in Figure 2.3 seems to eliminate some difficulties [18,19]. Its two gates effectively shield the channel from the drain field and result in a better scalability of the device. Recently, CMOS structures based on double gate transistors with gate lengths down to 10 nm have been reported [20,21].

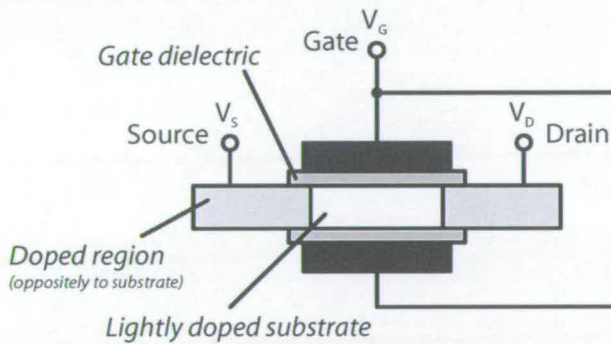


Figure 2.3: Typical structure of a double gate MOS transistor.

A lot of work is also spent in the field of nanotechnology, for example on the carbon nanotube FET [19,22]. Here, a carbon nanotube forms the channel between the source and the drain contacts. However, one of the drawbacks of devices with structures very different from present MOS transistors is their unfamiliar behaviour which requires to be understood before an integration into an integrated circuit technology is possible. Carrier transport in carbon nanotubes is very dissimilar to the one in a semiconductor like silicon and scaling needs to be addressed.

2.2 Process technology

The techniques used to produce semiconductor devices and integrated circuits changed significantly since the early years of semiconductors. This chapter gives a historical outline of the manufacturing methods and describes a modern semiconductor process as it is used for current VLSI (Very Large Scale Integrated) circuits.

2.2.1 Early processes

The first transistors were built using point contact technology and polycrystalline germanium. Shortly afterward it was moved to silicon and single-crystal material which allowed more uniform and reproducible device characteristics.

By the mid 1950s the grown junction and alloy junction technology had been developed by Shockley [10] and were widely used to produce transistors. For the grown junction technology, a single crystal was grown which contained a thin zone of material with opposite doping to the main part of the crystal. The crystal was then sawn into pieces so as to create pnp or npn structures, which could be connected using wires. In the alloy junction technology (Figure 2.4) a semiconductor material was taken and a metal was placed on it. The structure was then heated and the metal melted in order to diffuse the metal into the semiconductor. Materials commonly used for this process were germanium as semiconductor and indium as metal. Indium is a p-type dopant and a pn region is therefore created when it diffuses into an n-doped germanium semiconductor.

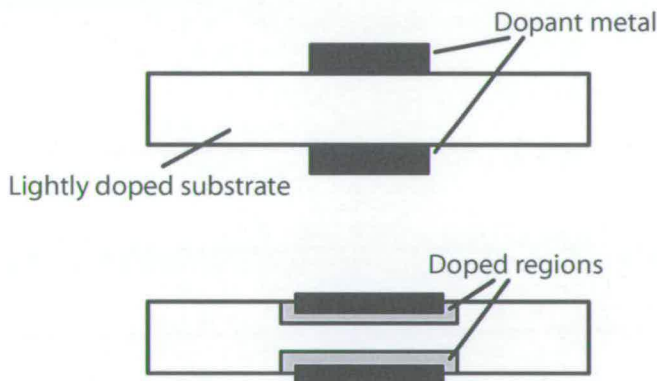


Figure 2.4: Steps involved in the alloy junction technology.

A next step towards multitransistor integrated circuits was the phase diffusion process developed at Bell Laboratories in 1957. The creation of a npn structure using this method involved the diffusion of a p-type dopant, which is in the gas phase, into a n-type substrate and the repetition of this step with a n-type dopant.

2.2.2 Invention of the integrated circuit

In 1959 Kilby built a circuit which integrated transistors, capacitors and resistors on a germanium substrate and therewith invented the integrated circuit [23]. Before his development, capacitors and resistors used in circuits were discrete elements manufactured without the use of semiconductors. Kilby's circuit still employed discrete wires to connect the devices on the substrate.

2.2.3 Planar process

In 1960 Hoerni presented the planar process which used patterned silicon dioxide layers to produce geometrically defined n- or p-type regions. Beforehand, people had started working with silicon dioxide and discovered the good interface between it and silicon. Silicon dioxide has also other properties which make it a very suitable material for the proposed process. First of all, it can easily be produced by oxidation of silicon in a furnace. Even more important is its ability of masking underlying material against the diffusion of dopants when creating doped regions.

Besides the use of silicon dioxide layers as masks for diffusion, the planar process developed by Hoerni also offered the capability of creating patterned metal interconnects between the devices on the substrate.

The manufacturing steps necessary to produce a npn bipolar transistor using the process developed by Hoerni is shown in Figure 2.5. A n-type silicon substrate is the starting material which is oxidised and patterned by etching so as to create a mask for the following diffusion using a p-type dopant. After diffusion the oxide is patterned again and a n-type dopant diffused into the silicon which finishes the creation of the required npn structure. The contact to the base of the transistor is made via a ring-shaped electrode, drain and source contacts are in the middle of the ring-electrode and at the back of the structure, respectively.

2.2.4 Device scaling

Since the development of the bipolar transistor, MOS transistor and planar process, the semiconductor industry continuously decreased feature sizes in integrated circuits. There are two main reasons why the industry is interested in reduced feature dimensions. First of all, it makes it possible to fit more structures onto a certain area, thus being able to manufacture more structures at the same time which reduces cost. Secondly, the speed of an integrated circuit is strongly influenced by its dimensions and electrical properties for reasons which are described using Equation 5.1 in Chapter 5.

The shrinking of devices, of course, created problems which were most of the time anticipated and solved by manufacturers. The FET is the dominant device in present-day integrated circuits due to its simple construction and good suitability for the planar process. A

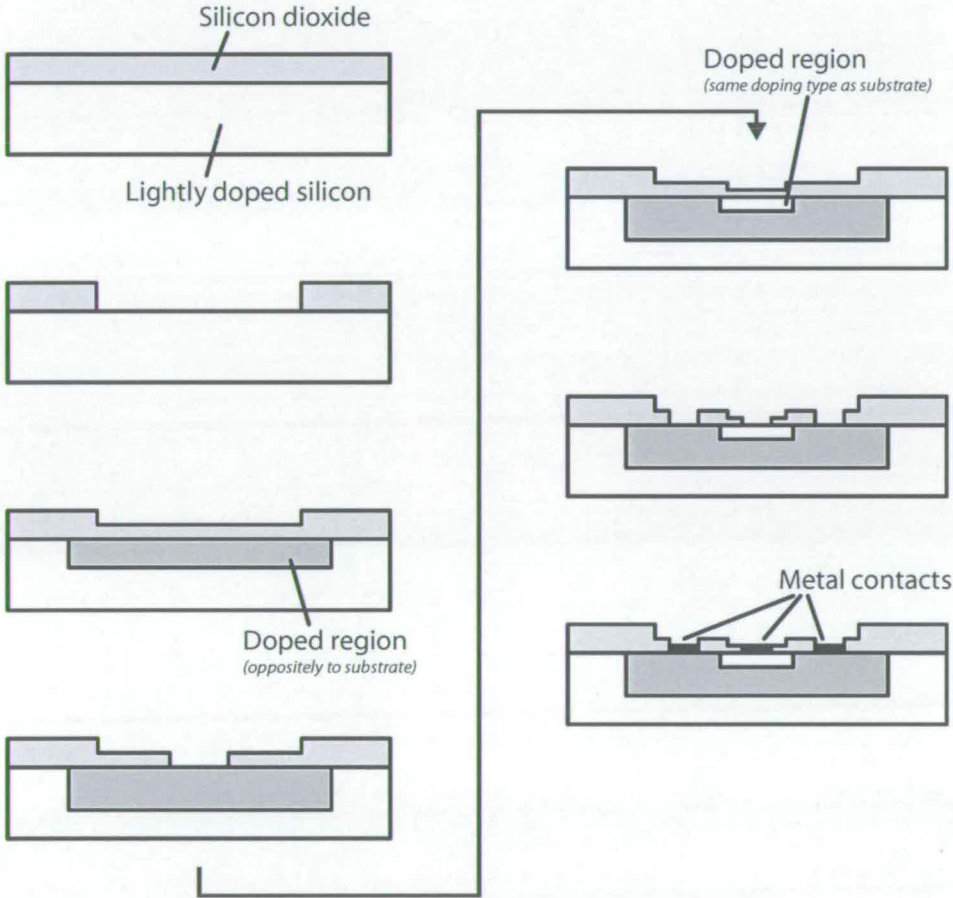


Figure 2.5: The planar process as it was developed by Hoerni to produce transistors.

Dimension	Scaling factor
Gate length l	$1/\alpha$
Gate width w	$1/\alpha$
Oxide thickness t_{Ox}	$1/\alpha$
Doping concentration N_A	α
Operating voltage V	$1/\alpha$
Drive current I	$1/\alpha$
Oxide capacitance C_{Ox}	$1/\alpha$
Delay time per circuit VC/I	$1/\alpha$
Power dissipation per circuit P	$1/\alpha^2$
Power density P/A	1
Interconnect line resistance R_L	α
Line response time $R_L C$	1
Line current density I/A	α

Table 2.1: Dependence of scaling factor α on the circuit performance and interconnect lines.

good way to decrease the size of the device, while keeping its characteristic behaviour, is to reduce all dimensions and voltages so that the electrical fields in the device are the same as of a larger device. Some of the consequences of device scaling according to the constant-field method are given in Table 2.1 [24]. However, it must be noted that in practice, it is often impossible to comply with all scaling rules. Supply and threshold voltage cannot be chosen arbitrary because of compatibility issues and power dissipation [25]. This results in large electrical fields which increase oxide leakage and lead to bad performance of the transistor unless new materials and processes could be developed to overcome these limitations. The problems associated with small devices described in Section 2.1 further complicate the application of the scaling rules. Table 2.1 has therefore only limited validity for very short devices as they are manufactured presently by the semiconductor industry.

The impact of device scaling on the device speed, namely the gate delay, is one of the major concerns in semiconductor manufacturing. The gate delay of a semiconductor device depends on the gate resistance and the capacitance of the gate stack. Early devices used aluminium as a gate material which possessed a low resistivity and was easy to deposit using PVD (Physical Vapour Deposition). However, aluminium was soon replaced by polysilicon (heavily doped silicon) which withstands the high temperatures that are used in the self-aligned gate process [24] described later. Further device scaling required lower resistivities which were achieved by using metal silicides for gate applications [26] (see Table 2.2). Aluminium and, more recently, copper are used as interconnect material in modern IC processes.

Material	Sheet resistance	Properties
Polysilicon	20 – 30Ω/□	suitable for self-aligned process low threshold voltage self-passivation
Metal silicides	1Ω/□	high temperature stability suitable for self-aligned process high temperature stability
Metal	0.05Ω/□	high electromigration resistance easy deposition (evaporation or sputtering) low resistance ohmic contacts to silicon

Table 2.2: Properties of different gate and interconnect materials.

2.2.5 Modern VLSI technology

The invention of the integrated circuit and the planar process in the late fifties and early sixties, respectively, led to the processes used to produce modern integrated circuits. Since their development, the main concepts did not significantly change but were merely refined. Modern VLSI circuits have features with dimensions down to 130 nm and possess up to eight layers of interconnects. Figure 2.6 is a simplified illustration of a structure as it can be found in present-day integrated circuits.

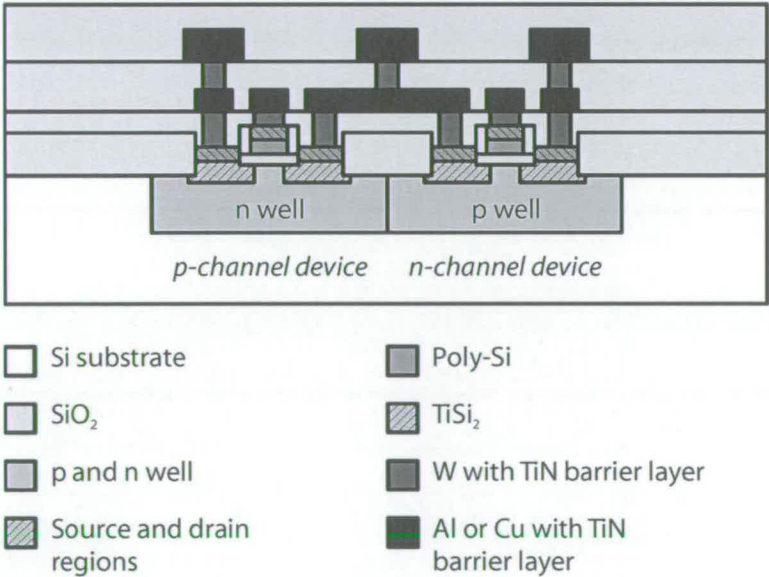


Figure 2.6: A CMOS structure consisting of a n- and a p-channel transistor fabricated using modern manufacturing methods.

The main differences compared to early MOS processes lie in the gate material, the formation of the source and drain regions and interconnect technology. As mentioned earlier,

the first MOS transistors used metal gates. However, device scaling required short channels which could not be manufactured using the standard process as described by Hoerni. The self-aligned process (Figure 2.7) supplied a solution to the problem by the definition of the drain and source regions by the gate itself [24]. This required a gate which masks the underlying substrate when creating the drain and source regions by dopant implantation and could withstand the high temperatures involved in the following heat treatment. This heat treatment is necessary to activate and diffuse the dopant. It was found that heavily doped polysilicon (polycrystalline silicon) met the requirements for the process. The fabrication begins with growing a field oxide which is then patterned to define the active device region. The gate oxide is then grown and the polysilicon gate created. A dopant diffusion is thereafter performed to create the drain and source regions. As a result of this process, the drain and source are perfectly aligned to the gate. The metallisation is done in the conventional way by depositing a dielectric, etching contact holes, depositing a metal layer and patterning it.

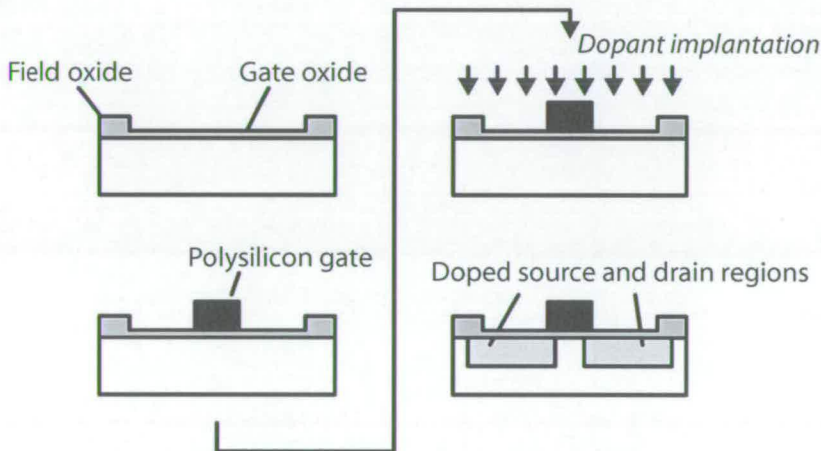


Figure 2.7: Definition of source and drain regions by the self-aligned process.

A further development was the self-aligned silicide (salicide) process to form drain and source contacts together with a low resistance silicide gate as depicted in Figure 2.8. The starting point is a transistor with a polysilicon gate and source/drain regions formed by the self-aligned gate process. To avoid a connection between the gate and the source/drain contacts, it is necessary to create sidewall spacers on the gate. This is usually done by depositing a silicon-dioxide layer and a following anisotropic etch. A metal layer is then deposited onto the wafer and the structure annealed. This results in the formation of metal-silicide in areas where the metal was in contact with silicon but not at locations where it was lying on top of silicon dioxide. The unreacted metal can then be easily removed using a selective wet etch process.

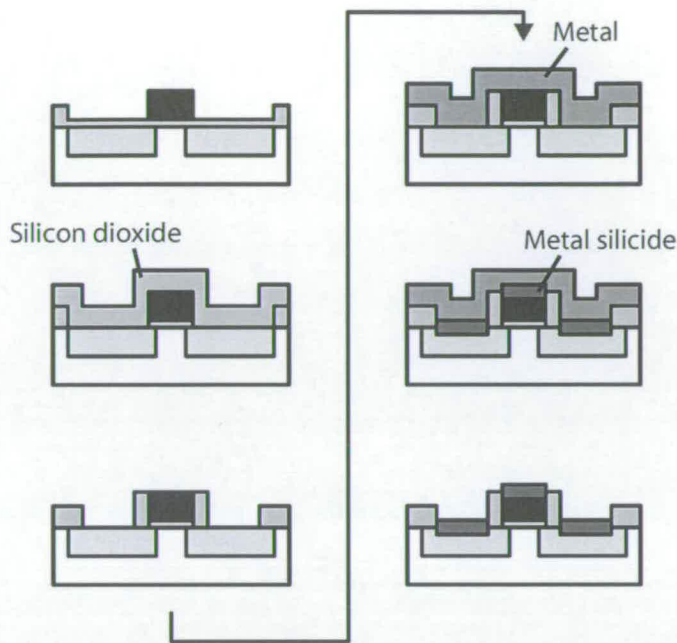


Figure 2.8: Creation of source and drain contacts by the self-aligned silicide process.

Modern integrated circuits are often built of millions of transistors which have to be wired together using local and global interconnects. The layers of interconnects, the vias used to connect them together and the dielectric layers are referred to as back-end technology. While the speed of early circuits mainly depended on transistor speed, the delay of the interconnects is nowadays dominant. Improving the back-end technology is therefore a key-issue in the quest for better integrated circuit performance.

As mentioned earlier, modern VLSI circuits consist of up to eight layers of interconnects. These are nowadays being produced using either the damascene or the double damascene process [9, 27]. Both these techniques use CMP (Chemical Mechanical Polishing) to obtain a flat surface even after many metal layers. The conventional approach used before resulted in non-planar topography and was not suited for many interconnect layers. This is mainly caused by lithography and step coverage limitations. Lithography limitations arise because of the restricted focus depth of exposure tools. The step coverage becomes a problem if deposited layers are not continuous or do not have the thickness required as a consequence of poor deposition on sidewalls resulting from many deposition processes.

Figure 2.9 shows the approach used in early multilayer interconnect structures. First, a contact hole to the lower level is opened in the dielectric. The metal is then deposited and patterned, forming the vias and interconnects. If more layers are required, a dielectric is deposited on top and the procedure repeated. It is obvious that this method works fine for a few interconnect layers but the process becomes more difficult with an increasing number of levels due to the topography created.

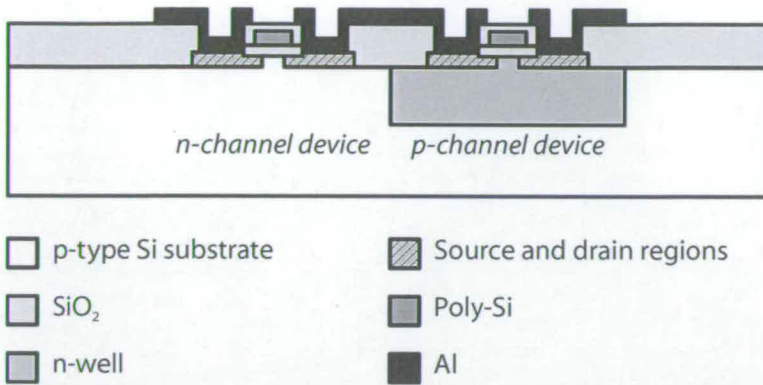


Figure 2.9: A CMOS structure consisting of a n- and a p-channel transistor as it was commonly fabricated in the 80s.

Unlike the conventional method, the damascene process employs a planarisation step to get a planar surface even after creation of many interconnect layers. The technique, which is shown in Figure 2.10, starts with the etching of contact holes to the lower level and the deposition of a tungsten blanket. An etchback is then done to remove the tungsten on the dielectric. After the creation of the via, the dielectric is deposited, the trenches for the metal lines are defined and filled with metal. The metal is then planarised after which another dielectric layer can be deposited and the procedure repeated to create more interconnect levels.

The dual-damascene process (Figure 2.11) works in a similar way. However, the via plug is filled in the same step as the metal line thus reducing the number of steps involved.

2.2.6 Future technologies

The ITRS 2003 (International Technology Roadmap for Semiconductors 2003) [6] mentions several technology trends and challenges which might occur in VLSI technology in the next 15 years. Many of the technologies required to keep up with Moore's law are already known but solutions to some problems still have to be found. A few of the main future trends are described in the following along with relating material and process requirements.

According to the roadmap the number of interconnect layers will continue to increase, adding extra cost to the manufacturing and decreasing the yield. The high number of interconnect layers and devices will increase the overall interconnect length on the chip and lead to cooling problems. The distance between the top of the chip and the layer with the active devices will grow, thus making an efficient heat transfer more difficult. Furthermore, the increasing device density will concentrate the heat on a small area and make power dissipation an even bigger problem.

There are a number of things which can be done to reduce the power dissipation problem. First of all, the devices can be operated at a lower voltage and consequently the power de-

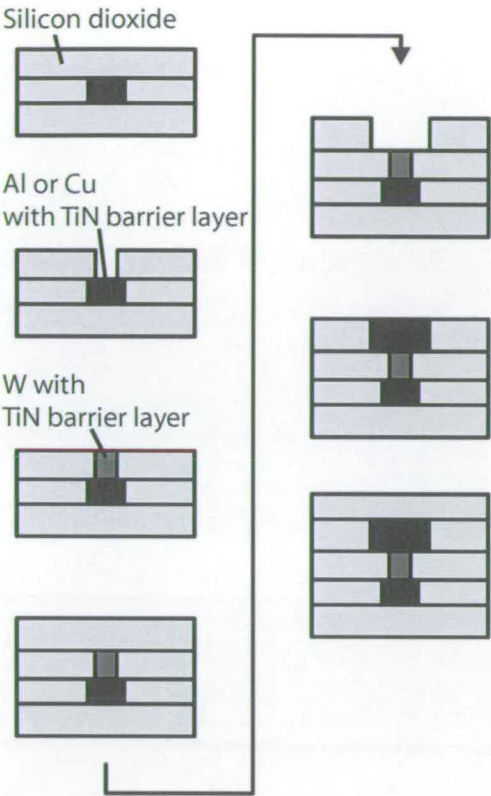


Figure 2.10: Damascene process.

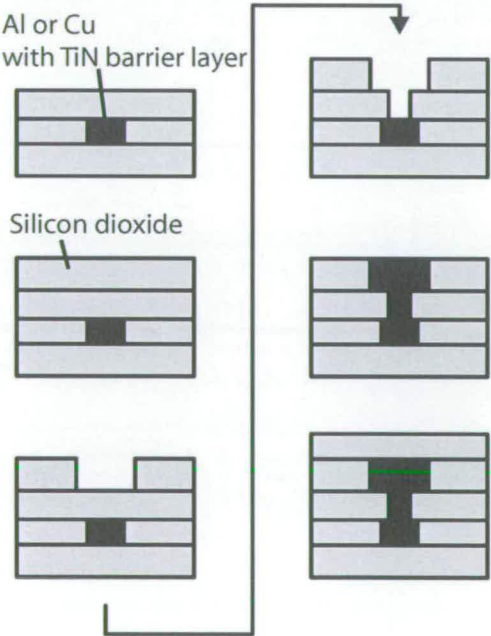


Figure 2.11: Dual damascene process.

creased. Secondly, it can be tried to reduce the resistance of the interconnects by choosing a material with a lower resistivity.

One of the trends predicted and communicated in the ITRS 2001 is the introduction of advanced gate dielectrics (high- κ) to reduce the RC delay. However, most of the dielectrics reported require the use of metal rather than polysilicon as a gate material [28]. This is because many of the dielectrics investigated are metal-oxides and react with silicon.

Metals have a further advantage compared to polysilicon due to their widely different work functions. Polysilicon gates can be doped to adjust the threshold voltage of the MOS devices but this requires an activation anneal thus increasing the overall thermal energy. Metals can be chosen according to their work function so that no channel doping is needed [28]. There are two ways to accomplish this which are depicted in Figure 2.12. Firstly, a metal or conductor with a work function leading to a Fermi level in the middle of the silicon bandgap (TiN for example) can be employed (midgap metal gate). This results in the same threshold voltage for both a n-channel and a p-channel device. Also, the number of masks required is reduced because all gates of a CMOS circuit can be created in the same process step. The second method makes use of two different metals (such as aluminium and platinum) for the gates of the n-channel and the p-channel device (double metal gates).

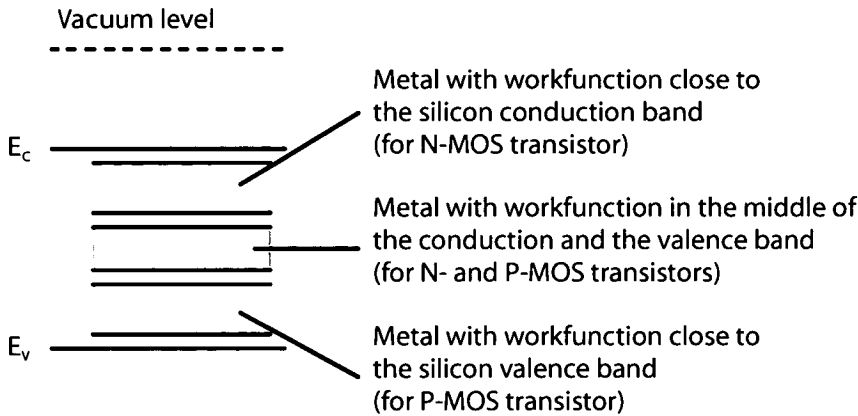


Figure 2.12: Possible positions of materials in the silicon band.

According to the ITRS 2003, metal gates could delay the introduction of high- κ dielectrics until the year 2009 while, with polysilicon gates, they are expected to be necessary from 2006. In present CMOS processes, heavily doped polysilicon is used as the gate material. However, it is difficult to create a high dopant concentration at the interface between the gate and the dielectric. This causes the lower part of the gate electrode to be depleted when the MOS transistor is switched on and this means that the actual dielectric thickness is increased. The increase of the equivalent oxide thickness (EOT) due to gate depletion is typically in the range of 0.4 – 0.5 nm [19], which is a significant amount considering an equivalent physical oxide thickness of 1 nm for the 70 nm technology suggested by the roadmap. The gate

depletion is expected to become a problem for polysilicon gates with a dopant density of $1 \cdot 10^{20} \text{ cm}^{-3}$ in 2006. Besides the thickness of the depletion region in the polysilicon gate, the EOT also consists of a contribution from quantum effects in the channel. The maximum of the carrier density under the dielectric lies a short distance from the interface in the substrate and enlarges the EOT. An increase of the effective oxide thickness therefore also occurs even when metal gates are used.

A major issue when using metal gates is the low melting point of most metals and their interaction with other materials at low temperatures. The self-aligned gate process described earlier requires high temperature to activate the implanted dopants. A possible solution to the problem is the replacement gate process [29]. Here, a polysilicon dummy gate is used to define the source and the drain regions. The polysilicon is then removed and replaced by a metal gate.

2.3 Organometallic materials in semiconductor manufacturing

2.3.1 Organometallic processes

Organometallic materials are widely used in the repair of photolithography masks and integrated circuits. The method usually employed is the focused ion-beam induced deposition of metals using an organometallic precursor gas. To produce a metal feature, the gas is injected into a vacuum chamber via a needle which ends close to the sample surface. The ion beam decomposes the gas and leaves behind a metal film. A review of this technique was written by Prewett [30]. Its applications in the semiconductor field range from the creation of cross-sections of integrated circuits to the repair of microchips by removing or depositing material. The deposition of platinum from an organometallic material was reported by Tao et al. in the early nineties [31].

Other research focused on the direct laser-writing of a metal pattern from a metal containing organic compound which was either solid [32, 33, 34, 35] or in the liquid phase [36, 37] by means of photothermal (pyrolytic) decomposition. In some cases, the sample needs to be rinsed in a liquid after exposure in order to remove organic residue.

Finer and more controllable features can be realised by photochemical (photolytic) decomposition. This principle was employed to deposit and pattern metal by irradiation of a solid organometallic material through a photolithographic mask [38, 39, 40, 41] or by laser-writing [42]. Some of the processes reported require the use of solvents in order to remove organic residue from the exposed film. Also, the photochemical decomposition of a gaseous precursor by exposure using a UV lamp and lasers has been employed to produce copper [43].

Another possible process is the deposition of a thin patterned metal layer from an organometallic material which is then used as a catalyst for the following electroless plating of a conductor [44].

Metal	Precursor	Exposure method	Feature size [μm]	Film thickness [nm]	Resistivity [$10^{-8}\Omega\text{m}$]	Ref.
Al	liquid	laser writing	3	1000	5.6	[36]
Cu	solid	laser writing	–	–	<10	[35]
Pd	liquid	laser writing	10	–	–	[37]
	solid	laser writing	1.8	–	40-240	[34]
Pt	gas	ion-beam writing	0.3	–	70	[31]
	solid	laser writing	–	<100	< 200	[33]
Au	solid	UV light and mask	1.2	–	40	[41]
	solid	UV light and mask	<1	15	–	[38]
	solid	e-beam writing	0.5	100	2.3 ^a	[39]
	solid	laser writing	–	1500	12	[45]
	solid	laser writing	3.5	40	4.5	[42]

^ameasured on conducting substrate

Table 2.3: Properties of some of the organometallic processes reported in the literature.

Metal	Resistivity at 293 K [46] [$10^{-8}\Omega\text{m}$]
Al	2.6548
Cu	1.6730
Pd	10.8
Pt	10.6
Au	2.35

Table 2.4: Resistivities of some metals.

While organometallic materials have a broad use in the repair of small numbers of circuits and masks, they do not yet have an application in modern IC manufacturing.

2.3.2 Properties of metal features deposited from an organometallic

The feature sizes and resistivities achieved by different authors differ widely and are summarised in Table 2.3. For comparison, known bulk resistivity values for some metals are listed in Table 2.4. The resistivity of most films reported lies well above the bulk resistivity, the cause of which can be attributed to inhomogeneity and thin film effects as described in Chapter 5. The exceptionally low resistivity of $2.3 \cdot 10^{-8}\Omega\text{m}$ (bulk resistivity of gold: $2.35 \cdot 10^{-8}\Omega\text{m}$) measured for gold films created by e-beam exposure of a solid organometallic material is questionable due to the film being deposited on a conducting surface and should therefore not be included when comparing films.

2.4 Platinum in semiconductor processes

2.4.1 Applications of platinum in semiconductor manufacturing

Platinum has many applications in semiconductor processes, especially as barrier layers [47] or as a component in the formation of silicides [26]. Barrier layers are used in integrated circuits so as to avoid the diffusion of one material into another. Aluminium for example forms a compound with a silicon content of approximately 0.5% when in contact with silicon and heated to 450 °C [48]. This is a major problem and causes spikes to be formed at aluminium/silicon junctions which can result in the failure of a device. Platinum, in the form of a silicide (e.g. PtSi), effectively prevents the interdiffusion of aluminium and silicon. In modern semiconductor processes, TiN is the most popular barrier layer.

2.4.2 Influence of platinum on semiconductor structures

One of the issues of interest for this work is the impact of platinum on underlying layers in a MOS stack. The influence of platinum on the silicon/silicon dioxide interface was studied early [49] and a shift of the C-V curve (see Chapter 6) of a MOS structure was observed after diffusion of platinum in nitrogen at a temperature of 900 °C. An investigation into the degradation of the silicon dioxide layer of a platinum/silicon dioxide/silicon structure due to annealing in nitrogen at temperatures between 400 °C and 850 °C was reported in the nineties [50]. It was found that, when annealing at temperatures above 600 °C, the breakdown voltage decreases significantly. Also, the interface state density at the silicon/silicon dioxide layer was thought to increase because of thermally induced stress. Based on their findings, the authors excluded the possibility of platinum being used as a gate material for MOS devices. The reaction of platinum with silicon dioxide substrates in a hydrogen environment was described by Lamber et al. [51].

When platinum is in contact with silicon and heated to a temperature of about 350 °C, it forms platinum silicide PtSi in a two stage process via the intermediate Pt₂Si. It was shown that reactions between the two materials already take place at temperatures as low as 170 °C [52].

Organometallic compound and process

3

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THE organometallic process used in this research is based on two photosensitive organometallic materials which can be exposed using UV, e-beam or ion-beam lithography in order to photolithically form the required metal pattern. This chapter describes the chemical structure and photochemical reaction associated with the organometallic compounds as well as the process used to create patterned metal layers on a substrate.

The organometallic material and the associated process used in this work were developed at the University of Dundee [53]. An analysis of the material and study of the chemistry of the compound and the platinum films produced are reported elsewhere [54].

3.1 Organometallic compound

It is important to point out at the beginning of this section that the bonding mechanism and the photochemical reaction described in the following are possible explanations only and research into the exact mechanisms behind the organometallic process is still under way.

An organometallic is a compound containing at least one metal-carbon bond. The fluoro platinum complexes $(C_3F_7)_2Pt^{II}-C_8H_{12}$ (cis bis-(normal-perfluoropropyl) platinum(II) 1,5-cyclooctadiene) [53] and $(C_3F_7)(CH_3)Pt^{II}-C_8H_{12}$ (cis methyl iso-perfluoropropyl platinum(II) 1,5-cyclooctadiene) used for this work are such compounds and the chemical structure of the former is shown in Figure 3.1.

It can be seen that the molecule of $(C_3F_7)_2Pt^{II}-C_8H_{12}$ consists of a platinum atom to which two C_3F_7 groups are attached on one side and a C_8H_{12} group (cycloocta-1,5-diene or COD) on the other. The second organometallic has one of the C_3F_7 groups replaced by a CH_3 group.

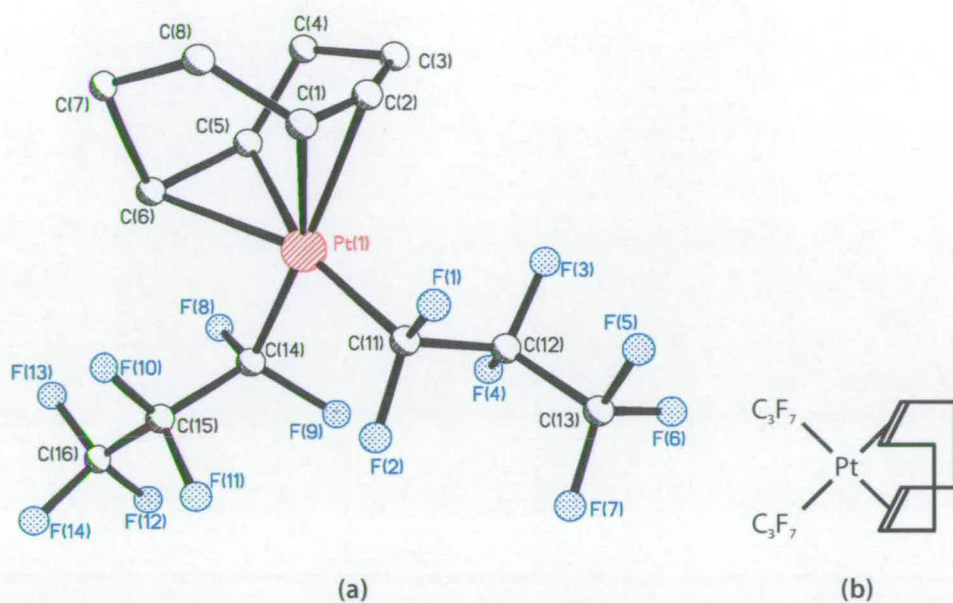


Figure 3.1: Structure of the organometallic material.

It should be noted that, although this research utilises a platinum organometallic, similar compounds based on other metals such as silver, gold, molybdenum, hafnium, tantalum and tungsten can be produced.

3.1.1 Bonding mechanism

The possible bonding mechanisms related to the organometallic material $(C_3F_7)_2Pt^{II} - C_8H_{12}$ can best be explained using electron orbitals which are probability densities for electrons around a nuclei. Orbitals for the 1s, 2p and 3d shell calculated from eigenfunctions for one-electron atoms [55] are shown in Figure 3.2, Figure 3.3 and Figure 3.4, respectively.

The bond between the platinum atom and the cycloocta-1,5-diene is made via backbonding [56] as depicted in Figure 3.5. The cycloocta-1,5-diene acts as a σ donor/ π acceptor ligand and is also called η^4 -cycloocta-1,5-diene due to it having an hapticity of 4 (it has 4 electrons which can be bonded directly to the metal). The σ bond is created by electrons from the COD which fill the bonding orbital. Backbonding occurs if electrons from the metal fill the empty antibonding π -orbitals of the C-C bond, thus weakening it (its length can then similar to a single bond) and creating two metal-carbon bonds which can be represented by σ bonds.

Pt^{II} , as it occurs in the compound, possesses a $(d)^8$ metal centre and therefore forms a square-planar coordination complex. In a free atom, the five d orbitals, which are shown in Figure 3.4, have the same energy. If a ligand is present, ligand field splitting occurs and the $d_{x^2-y^2}$ orbital situated in the xy plane pointing directly at the ligand (e_g set) has a higher

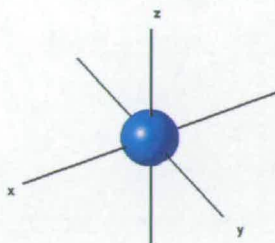


Figure 3.2: Hydrogen atom 1s orbital.

energy than the remaining four d orbitals (t_{2g} set). It is energetically advantageous for the electrons of the COD to occupy the σ bonding molecular orbitals. At the same time, the e_g set of the metal is formed by the antibonding levels of the COD. The empty antibonding orbitals of the COD also lower the t_{2g} set which is subsequently filled with electrons from the metal.

The bonding of the two C_3F_7 groups to the Pt^0 can be explained as follows. C_3F_7 needs a single electron to complete an octet and can therefore accept an electron. Pt^0 , which has an electron configuration of $[Xe](4f)^{14}(5d)^9(6s)^1$, has ten valence electrons and can donate electrons. We thus have electron pair bonds between Pt^0 and the C_3F_7 groups. The bond is a single bond which means that it is a σ bond. Owing to the removal of two electrons from the platinum, it is in the oxidation state Pt^{II} which has an electron configuration of $[Xe](4f)^{14}(5d)^8$. The C_3F_7 groups have a high electron affinity and thus weaken the $Pt - C_8H_{12}$ bond. It is possible to replace the C_3F_7 by some other group in order to adjust the bond strength, which has been done in the case of the $(C_3F_7)(CH_3)Pt^{II} - C_8H_{12}$ compound.

The resulting molecule is a coordination complex, a geometrical isomer called *cis*, and is likely to be stable due to it complying with the 16-electron rule for square-planar molecules [56]. There are four electrons from the C_8H_{12} ligand, ten electrons from the Pt^0 and one electron from each of the C_3F_7 groups.

The bonding effects related to the $(C_3F_7)(CH_3)Pt^{II} - C_8H_{12}$ compound are the same as described above, with the exception of the CH_3 group which replaces one of the C_3F_7

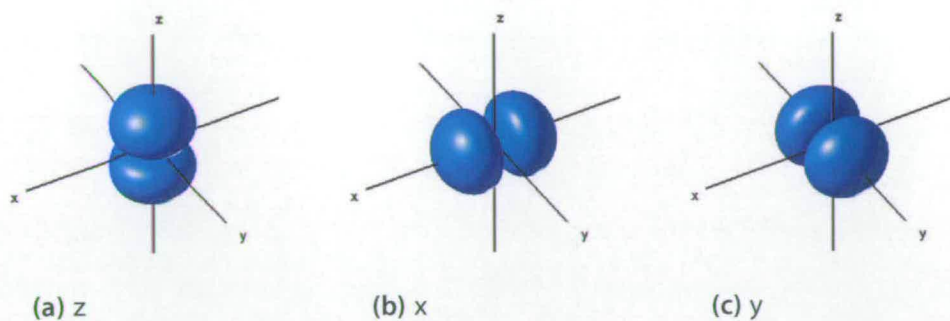


Figure 3.3: Hydrogen atom 2p orbitals.

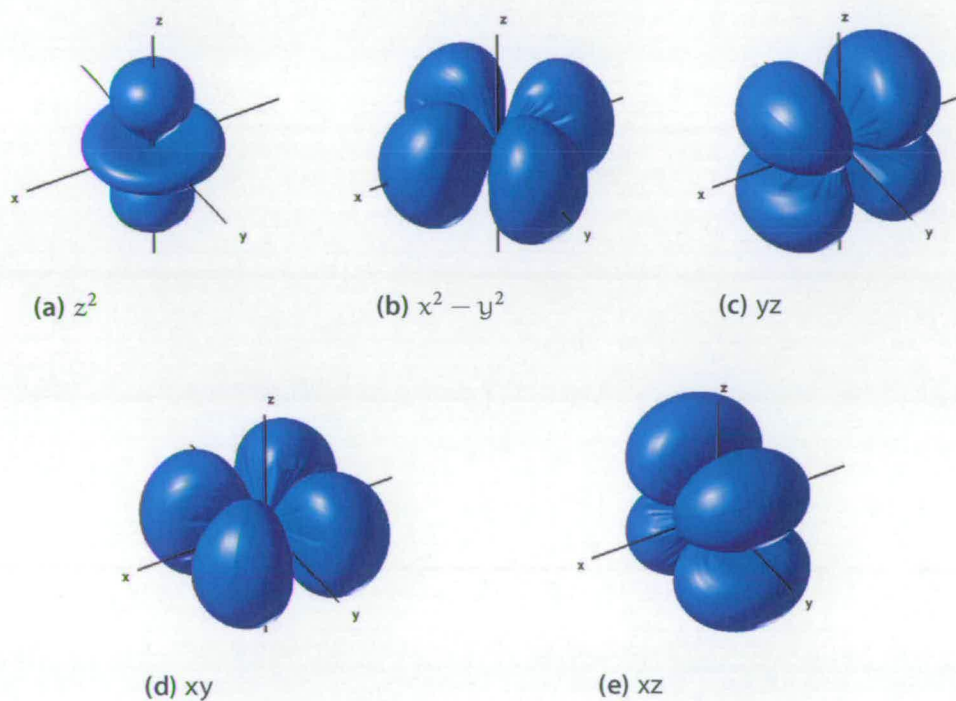


Figure 3.4: Hydrogen atom 3d orbitals.

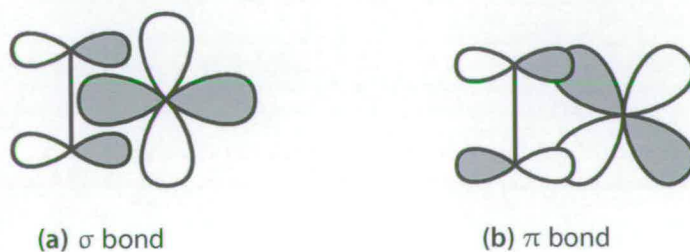


Figure 3.5: The two different types of backbonding mechanisms.

groups. CH_3 also requires a single electron to complete an octet and is therefore bonded to the electron-donating platinum. Thus, there will again be 16 electrons around the platinum atom which predicts that the molecule is stable.

3.1.2 Photochemical reaction

It is thought that the bonds between the COD and the Pt of $(\text{C}_3\text{F}_7)_2\text{Pt}^{\text{II}} - \text{C}_8\text{H}_{12}$ can photochemically be broken by a pericyclic reaction according to a set of rules which are called the Woodward-Hoffmann rules [57]. A pericyclic reaction is a reaction whereby a reorganisation of the bonds of a structure takes place at the same time and without going through intermediate compounds.

The Woodward-Hoffmann rule for a thermal pericyclic reaction [58].

A ground-state pericyclic change is symmetry-allowed when the total number of $(4q + 2)_s$ and $(4r)_a$ components is odd.

The Woodward-Hoffmann rule for a photochemical pericyclic reaction [58].

A pericyclic change in the first electronically excited state is symmetry-allowed when the total number of $(4q + 2)_s$ and $(4r)_a$ components is even.

The term *symmetry-allowed* stands for the continuous transformation of molecular orbitals of reactants into those of products in such a way as to preserve the bonding character of all occupied molecular orbitals at all stages of the reaction [57]. The suffixes *s* and *a* used in the component classifier stand for the terms suprafacial and antarafacial, respectively, and describe the geometrical setting of a reaction. When both ends of a component form new bonds on the same face, the component is suprafacial, if they form on opposite faces, the component is called antarafacial. The $(4q+2)$ kind of component has 2, 6, 10, ... electrons whereas the $(4r)$ kind possesses 4, 8, 12, ... electrons.

As mentioned earlier, there are two types of bonds involved in the Pt/COD structure. Firstly, there is the σ bond between the filled bonding orbitals of COD and the empty d-orbital of the metal. Figure 3.6(a) shows the HOMO (Highest Occupied Molecular Orbital) of COD and the $d_{x^2-y^2}$ orbital of the metal. This situation can be expressed by a suprafacial π bond between the two carbon atoms and a suprafacial σ bond to the Pt. The π bond is a $(4r)_s$ component and thus does not have to be counted. The σ bond is a $(4q + 2)_s$ component. These bonds are present twice and we therefore get a total number of 2. Secondly, the metal is bonded to the LUMO (Lowest Unoccupied Molecular Orbital) of COD via π acceptor interaction which is depicted in Figure 3.6(b). In the extreme, this results in two bonds which resemble σ bonds, thus adding two $(4q + 2)_s$ components. Again, the components are existing twice and lead to a total number of 4. This means that the structure has a total number of $(4q + 2)_s$ and $(4r)_a$ components which is even and a photochemical pericyclic reaction is therefore allowed according to the Woodward-Hoffmann rules.

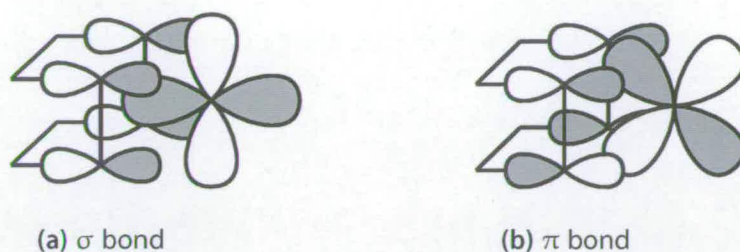
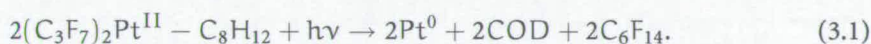


Figure 3.6: The two different types of backbonding mechanisms applied to the organometallic material.

If a photon with high enough energy strikes the molecule, the Pt - C₃F₇ bond breaks. This process is facilitated by the *trans*-effect which states that ligands opposite to the leaving group may influence the rate of substitution in a square-planar complex [59,60]. Strong σ donor or π acceptor ligands, as the COD in the organometallic material, accelerate substitution of the group which lies *trans* or opposite to the ligand, which is one of the C₃F₇ groups. The second C₃F₇ group and the COD then detach themselves because the compound does not comply with the 16-electron rule anymore and free the platinum atom. A similar reaction was reported in the literature [61]. The reaction is thought to conform with the formula



The chemical formula indicates that two molecules of the organometallic material are involved in the photochemical reaction and the two C₆F₁₄ groups are created by bonding of a C₃F₇ group from one molecule with a second one from the other.

The dissociation of the (C₃F₇)(CH₃)Pt^{II} - C₈H₁₂ is thought to work in a very similar manner. However, due to the asymmetry, the molecule is less stable and the photochemical reaction can therefore be faster.

3.2 Process

The deposition of a patterned metal layer using the organometallic materials described above can be divided into three main parts, namely deposition, exposure and heat treatment.

3.2.1 Deposition

For this research, the organometallic material was deposited by PVD (Physical Vapour Deposition) using an Edwards Auto 306 Vacuum Coater. The compound, which was available in the form of a powder, was put into a tungsten boat which was then placed into the bell jar of the evaporation tool. The chamber was evacuated and the compound evaporated onto

the sample by resistive heating of the boat. The sample itself was placed on a rotating disk situated directly above the tungsten boat and fixed at an angle of 45° . Due to the compound having a very low evaporation temperature, the evaporation time was in the range of a couple of seconds and a spatial variation of the resulting film thickness over the wafer was observed.

3.2.2 Exposure

The exposure of the organometallic material was done using an OAI Model 500 Mask Aligner working at a wavelength of 260 nm. The exposure at an output power of approximately 16.5 mWcm^{-2} lasted for typically two hours in the case of $(\text{C}_3\text{F}_7)_2\text{Pt}^{\text{II}} - \text{C}_8\text{H}_{12}$ and forty minutes if $(\text{C}_3\text{F}_7)(\text{CH}_3)\text{Pt}^{\text{II}} - \text{C}_8\text{H}_{12}$ was used, during which the mask was in contact with the underlying sample. Other exposure techniques, e.g. e-beam or ion beam, could potentially be used to produce higher resolution patterns but would also result in low throughput. E-beam and ion-beam lithography usually use maskless direct writing, exposing only a small area at a time.

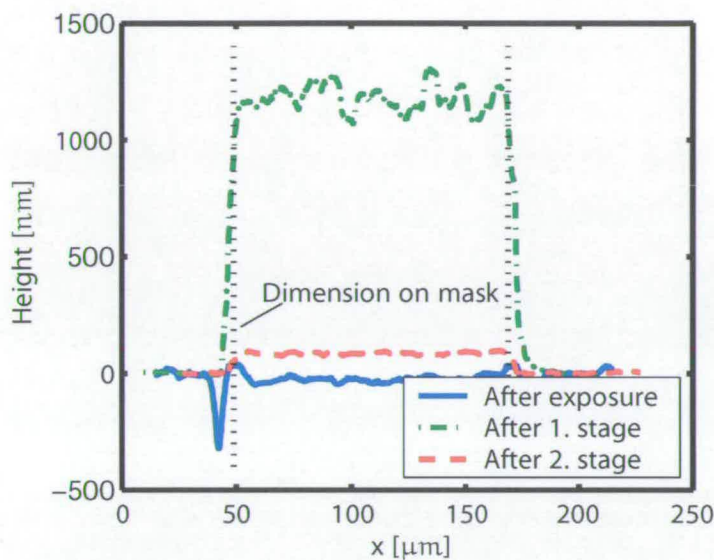
After exposure, organometallic material is left in the unexposed regions and platinum, as well as organic residue, is left in the exposed areas.

3.2.3 Heat treatment

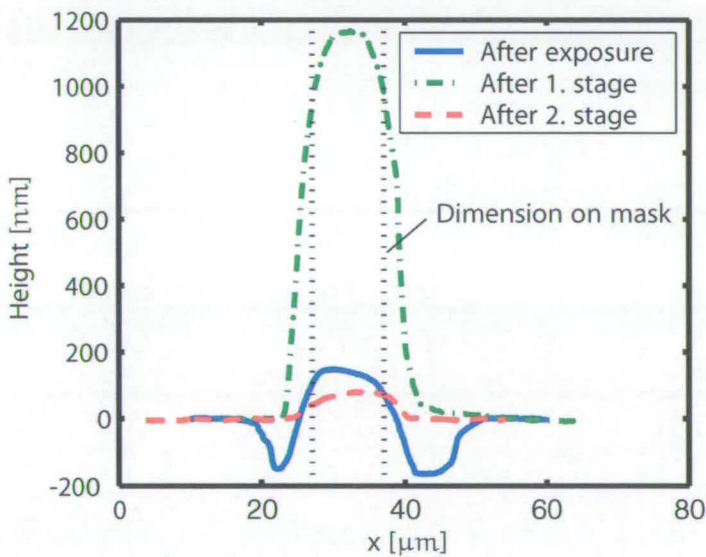
The heat treatment consists of three separate stages which are referred to as sublimation, oxidation and reduction step. The first stage, the sublimation step, is used to remove the unexposed organometallic material. Stage two, the oxidation step, and stage three, the reduction step, are used to remove the organic residue in the exposed regions, thus purifying the deposited metal. A typical change of the topology during the heat treatment is shown in Figure 3.7 on the basis of a pad and a line. It can be observed that after exposure, the pattern can already be identified. After the first heat treatment step, the material around the pattern has been removed and during the second stage, the film thickness is reduced due to the evaporation of the organic parts in the film.

Temperatures and environments for the heat treatment were established at the University of Dundee while developing the organometallic material. The sublimation step is conducted for six hours in nitrogen at 75°C . For stage two, the sample is heat treated for one hour at 250°C in air while stage three is done for four hours at 350°C in a 5% hydrogen in nitrogen atmosphere. Greek cross test structures with an arm width of $10 \mu\text{m}$ produced on a silicon dioxide substrate using the organometallics $(\text{C}_3\text{F}_7)_2\text{Pt}^{\text{II}} - \text{C}_8\text{H}_{12}$ and $(\text{C}_3\text{F}_7)(\text{CH}_3)\text{Pt}^{\text{II}} - \text{C}_8\text{H}_{12}$ are shown in Figure 3.8(a) and Figure 3.8(b), respectively.

However, the facilities in Dundee are designed for small samples only and do not allow the processing of whole wafers. It was therefore necessary to develop a system compatible with three inch wafers as used in this work.

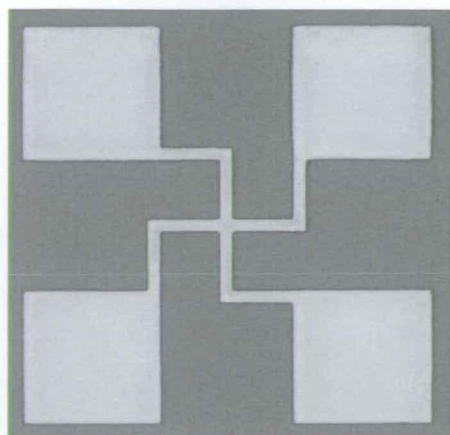


(a) Pad with a width of 120 μm .

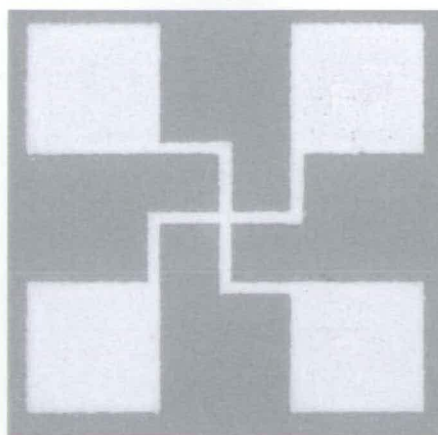


(b) Line with a width of 10 μm .

Figure 3.7: Change of the film topology during the heat treatment.



(a) Greek cross with an arm width of 10 μm produced from $(\text{C}_3\text{F}_7)_2\text{Pt}^{\text{II}} - \text{C}_8\text{H}_{12}$.



(b) Greek cross with an arm width of 10 μm produced from $(\text{C}_3\text{F}_7)(\text{CH}_3)\text{Pt}^{\text{II}} - \text{C}_8\text{H}_{12}$.

Figure 3.8: Platinum features manufactured at the University of Dundee using the organometallic process and a test chip mask designed for this work at University of Edinburgh.

For the first two stages of the heat treatment, a Tenney Junior oven with a setup like shown in Figure 3.9 was used. Whole wafers were placed on a glass holder at the bottom of the oven while chips were put onto the top of a wafer situated on the glass holder. The control system of the oven allows the two stages to be done automatically, without interference of an operator. Stage three is conducted in a furnace with the wafers being placed standing in a boat and chips laying on a wafer.

The maximum temperature of the oven used is 200 °C and the furnace is usually working at 435 °C. This, together with the fact that the samples could only be heat treated in air in the oven, made it necessary to reengineer the heat treatment. Due to the temperature of stage two being lower than the temperature used at the University of Dundee (195 °C was chosen instead of 250 °C), the time was increased from one to four hours, while the times for stages one (75 °C) and three (435 °C) were identical to the ones used during the heat treatment in Dundee. Structures resulting from the heat treatment at the University of Edinburgh are depicted in Figure 3.10(a) for $(\text{C}_3\text{F}_7)_2\text{Pt}^{\text{II}} - \text{C}_8\text{H}_{12}$ and Figure 3.10(b) for $(\text{C}_3\text{F}_7)(\text{CH}_3)\text{Pt}^{\text{II}} - \text{C}_8\text{H}_{12}$.

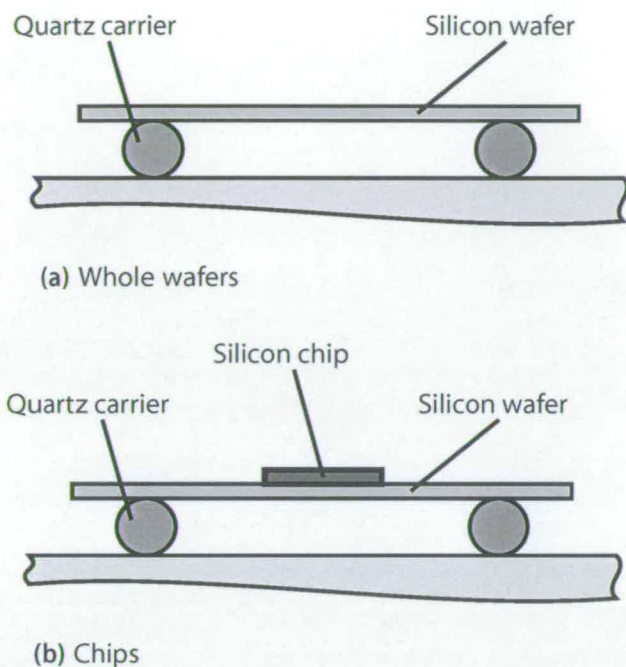
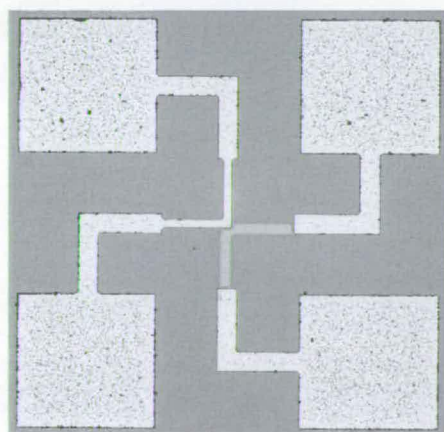
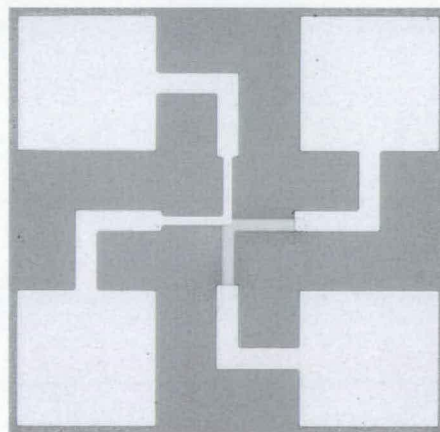


Figure 3.9: Setup used to process the samples in the oven.



(a) Contact resistance test structure with an arm width of $10\ \mu\text{m}$ produced from $(\text{C}_3\text{F}_7)_2\text{Pt}^{\text{II}} - \text{C}_8\text{H}_{12}$.



(b) Contact resistance test structure with an arm width of $10\ \mu\text{m}$ produced from $(\text{C}_3\text{F}_7)(\text{CH}_3)\text{Pt}^{\text{II}} - \text{C}_8\text{H}_{12}$.

Figure 3.10: Platinum features manufactured at the University of Edinburgh using the organometallic process. Note that in contrast to the structures in Figure 3.8, the pads are made of aluminium.

3.3 Discussion

Patterned platinum structures have been deposited using UV exposure of an organometallic material invented at the University of Dundee. A new process was successfully developed which allows the organometallic compound to be utilised together with three inch wafers instead of the 1 cm² chips used previously.

It was found that features produced on whole wafers using the facilities in Edinburgh are of similar quality as the ones on small chips heat treated at the University of Dundee, indicating that the temperatures and times chosen are in a suitable range. A simple test, the scotch tape test [62], was employed to investigate the adhesion of the produced metal films to the substrate. A piece of adhesive tape was attached to the surface and pulled. The films did not peel meaning that they possessed some adhesion to the substrate. Measurements of the film topology at different stages of the organometallic process (Figure 3.7) showed that the pattern produced is larger than the pattern on the mask. This effect is likely caused by diffraction of the UV light when exposing the organometallic.

Test chips

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DURING the course of this work, two test chips were utilised. The first one, called UDEA V0 was designed and manufactured in order to characterise the metal deposited using the organometallic process by means of resistivity and capacitance measurements. This was important for material development and evaluation. The second chip, named UDEA V1, was used to investigate the suitability of the organometallic process for the fabrication of standard metal gate transistors, allowing process development and device evaluation.

This chapter describes the layout of the chips and the processes used for the production. The test structures on the chips are only briefly mentioned and will be explained in detail in later chapters.

4.1 Test chip UDEA V0

The test chip UDEA V0 is a one layer design which meant that in order to compare measurement results, two batches of wafers were processed, one using the organometallic process and the other using standard processes.

4.1.1 Layout

There are three different kinds of test structures on the test chip UDEA V0 (Figure 4.1) which are listed in Appendix A.

- Resistivity test structures
- Linewidth test structures
- Capacitors for C-V measurements

All resistive test structures, which include the ones used to measure the linewidth, are present in two versions, one of which possesses large metal areas to reduce the effect of joule heating [63]. The pads of all devices have a size of $120 \times 120 \mu\text{m}^2$ and are arranged in a $2 \times n$ array.

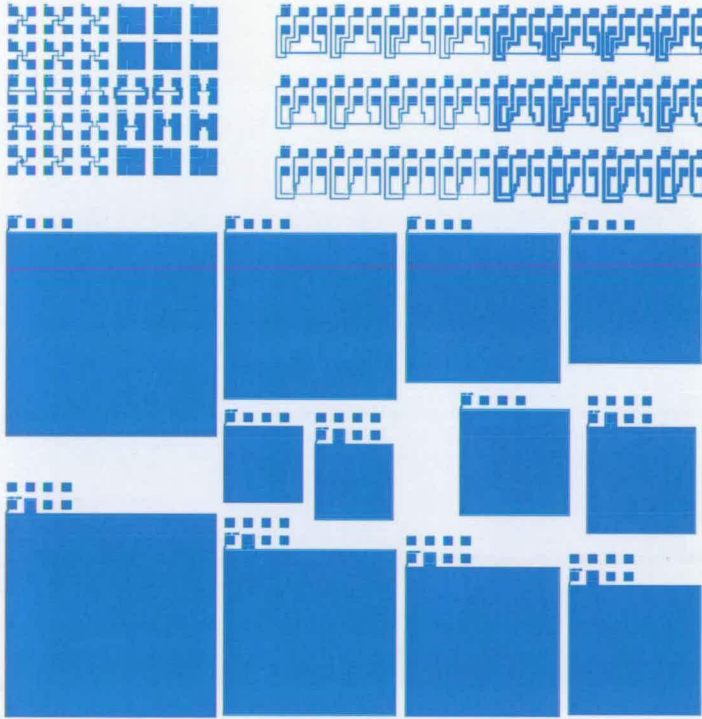


Figure 4.1: Layout of the test chip UDEA V0. The resistivity structures are situated in the upper left-hand corner, linewidth test structures in the upper right-hand corner and the capacitors below.

4.1.2 Process

The starting material for the manufacturing process is a $\langle 100 \rangle$ n-type silicon wafer. First of all, an oxide with a thickness of $0.5 \mu\text{m}$ is grown and the front of the wafer coated with photoresist. The photoresist is then used to mask the layer while etching away the oxide from the back. After stripping the photoresist, the back of the wafer is doped using phosphorus. The doped region is necessary to create a good ohmic contact to the aluminium which is sputtered onto the back of the wafer later in the process. All oxide is then removed and the wafer reoxidised to a thickness of 100 nm (Figure 4.2(a)). Up to this point, all wafers are processed in the same way, regardless of their designation for aluminium structures or structures manufactured using the organometallic process. The metallisation is then done by different techniques.

Film name	Organometallic		Heat treatment done at	
	$(C_3F_7)_2Pt^{II}C_8H_{12}$	$(C_3F_7)(CH_3)Pt^{II}C_8H_{12}$	Univ. of Dundee	Univ. of Edinburgh
a	✓		✓	
b	✓			✓
c		✓	✓	
d		✓		✓

Table 4.1: Names given to the deposited platinum films for UDEA V0.

The aluminium metallisation starts with sputtering a metal layer of 0.5 μm thickness which is then coated with photoresist and exposed using standard lithography. After developing the photoresist, the pattern is transferred onto the aluminium by a dry etch process. The remaining photoresist is finally removed, leaving behind the desired metal structures on the silicon dioxide.

The creation of the metal features using the organometallic process works very differently. First, the organometallic material is deposited onto the silicon dioxide by PVD (Physical Vapour Deposition) in an Edwards Auto 306 Vacuum Coater and exposed for one hour using deep UV light from an OAI Model 500 mask aligner with an exposure system working at a wavelength of 260 nm. The organometallic material deposition was performed in Dundee as they had considerable experience in this process. The lithography was also undertaken at Dundee, partly due to concern about possible emissions from the material during exposure, and also because the material was tuned for 260 nm which did not suit lithography systems at the University of Edinburgh (note that the material is capable of being tuned to any of the standard lithography wavelengths). Unexposed organometallic compound and organic residue is then removed in an oven by the first heat treatment step. Also, the oxidation, which is the second stage of the heat treatment, is done. The final heat treatment step is conducted later together with the aluminium anneal. For future reference, the films are assigned names according to the organometallic material used and the place where the heat treatment was conducted. These are given in Table 4.1.

The wafers now look as shown in Figure 4.2(b) on the base of a structure with platinum metallisation. Both, the wafers with the aluminium pattern and the ones processed using the organometallic process are then coated with photoresist on the front. The oxide on the back is then etched away and aluminium for the back contact sputtered on. To finish the process, the aluminium is annealed in an atmosphere of 40% H_2 in N_2 at 435 °C which leads to the structure depicted in Figure 4.2(c). This annealing step is also the third stage of the heat treatment of the organometallic process. The temperatures and times chosen for the heat treatment depended on the treatment being done either in Dundee or Edinburgh and are given in Chapter 3. Also, in case of films a and c, the anneal of the aluminium was done before the organometallic process.

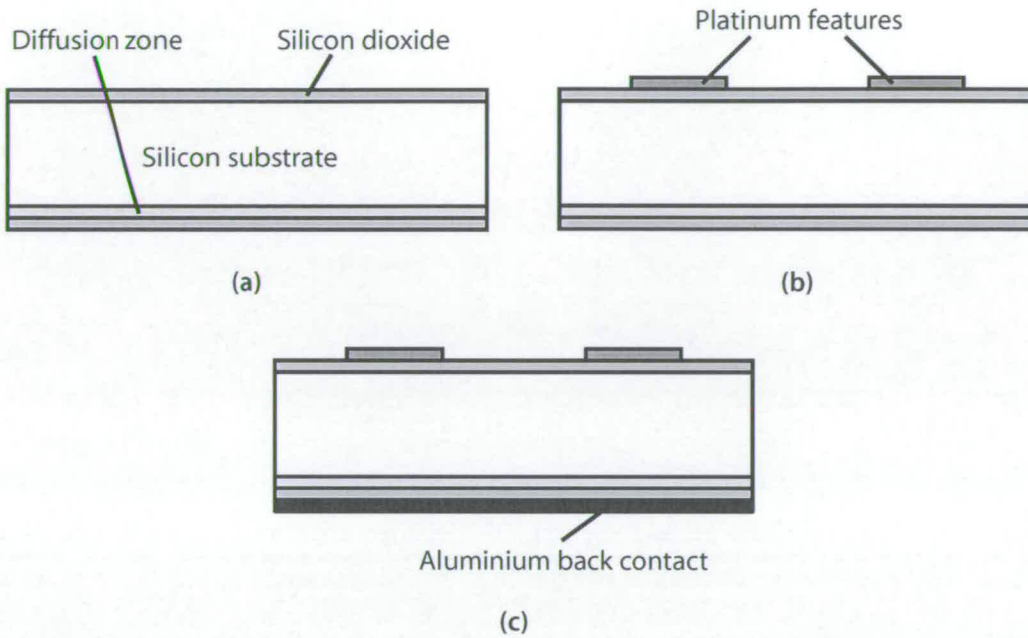


Figure 4.2: Process used to manufacture UDEA V0.

The runsheet used to manufacture the test chip is detailed in Appendix B and a picture of a manufactured chip is shown in Figure 4.3.

4.2 Test chip UDEA V1

4.2.1 Layout

Besides transistors this test chip consists of semiconductor test structures to characterise the MOS stack and materials involved. The test structures on UDEA V1 (Figure 4.4) can be divided into seven groups. All the test structures on the chip and their dimensions can be found in Appendix A.

- P-MOS transistors
- Resistivity test structures
- Linewidth test structures
- Contact resistance test structures
- Capacitors for C-V measurements
- Interdigitated capacitors
- Optical test structures

Note that the chip was designed so that no platinum was in direct contact with silicon. The reason for this is the formation of platinum silicide at temperatures as low as 170 °C (see Section 2.4).

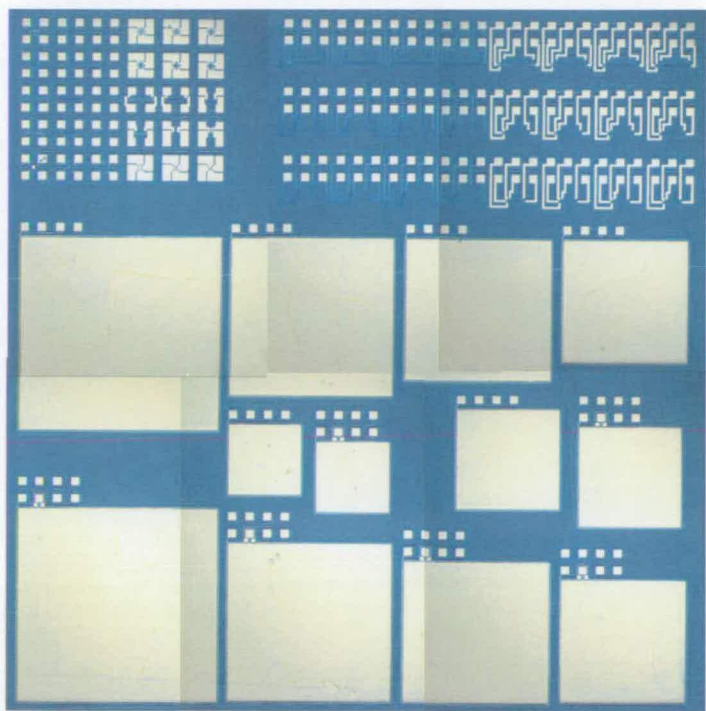


Figure 4.3: Test chip UDEA V0.

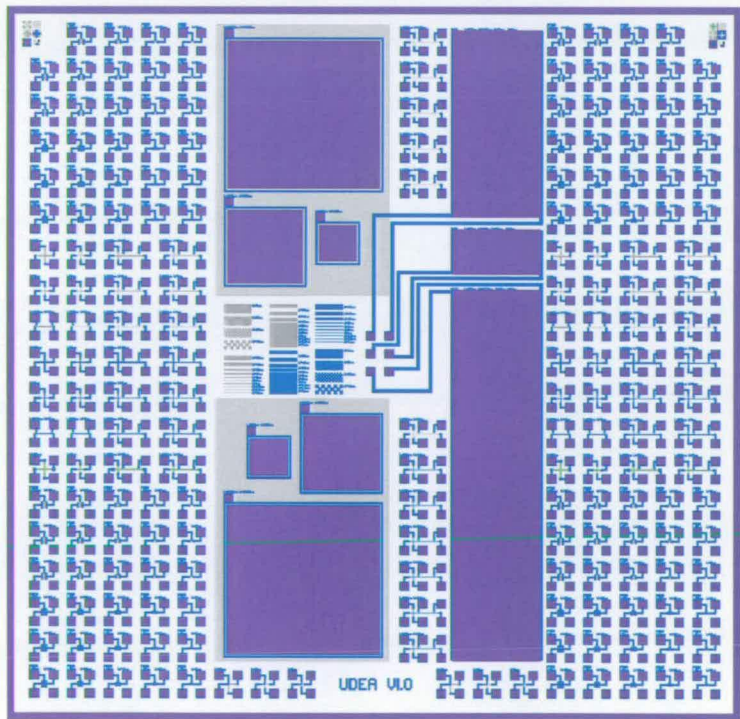


Figure 4.4: Layout of the test chip UDEA V1.

4.2.2 Process

A P-MOS process was employed for UDEA V1. In order to simplify the manufacturing, a technology based on an existing aluminium gate process which did not need ion-implantation for adjustment of the threshold voltage V_T was used. While the gate metal was replaced by platinum deposited from an organometallic material, aluminium was still used for interconnects and pads. The process sequence is shown in Figure 4.5 on the basis of a platinum gate transistor. The creation of the back contact is not shown in the picture but is identical to the process described for UDEA V0. The replacement of the gate material required some considerations based on the issues mentioned in Chapter 2.4.

The starting material for the technology described is a three inch n-type silicon wafer with a $\langle 100 \rangle$ orientation and a resistivity of $20 - 40 \cdot 10^{-3} \Omega\text{m}$. The original process was based on wafers with a $\langle 111 \rangle$ orientation due to the higher oxide fixed charge compared to wafers with a $\langle 100 \rangle$ orientation [64]. The positive oxide fixed charge at the silicon/silicon dioxide results in an accumulation region below the interface and thus isolates the transistor device. However, it was decided to sacrifice the good isolation in favour of better availability and less charges in the silicon dioxide layer of the MOS devices being produced.

To start the processing, an oxide with a thickness of approximately $1 \mu\text{m}$ is thermally grown in a furnace by wet oxidation for one hour at 1100°C . Photoresist is then spun onto the front of the wafer and the oxide on the back removed by dry etching in a CF_4/H_2 plasma before putting it into a furnace at 1000°C for 15 minutes to diffuse phosphorus from solid sources. After deglazing the wafer in a 10% HF bath, the front of the wafer is wet oxidised for one hour at 950°C (Figure 4.5(a)). Next, photoresist is deposited, contact printed using a Karl Suss MA8 mask aligner and developed. The oxide is then patterned by dry etching in a CF_4/H_2 plasma and used as a mask for the following boron diffusion which is done at 1000°C for 30 minutes using boron from solid sources (Figure 4.5(b)). The wafer is afterwards deglazed as described above and the field oxide of $1 \mu\text{m}$ grown (Figure 4.5(c)) by wet oxidation for 15 hours at 950°C . This field oxide is patterned by dry etching in the next step so as to prepare the wafer for the production of the gate oxide (Figure 4.5(d)). The gate oxide with a thickness of 100 nm is then created by wet oxidation for 15 minutes at 950°C followed by a 30-minute anneal at 950°C in a nitrogen atmosphere in order to reduce the interface trap density (Figure 4.5(e)). The wet oxidation reduces the oxidation time compared to a dry process and is less prone to contamination due to the scavenging action of the water vapour. It must be noted that now there is also a thin oxide in the areas where the source and drain contacts will be. This procedure reduces the amount of silicon dioxide which has to be removed when etching the contact holes. At this point of the fabrication, the whole wafer is covered by either thin or thick oxide.

The platinum gate is then deposited and patterned using the organometallic process which starts with the deposition of the organometallic material by PVD (Physical Vapour Deposi-

Film name	Organometallic	
	$(C_3F_7)_2Pt^{II}C_8H_{12}$	$(C_3F_7)(CH_3)Pt^{II}C_8H_{12}$
e	✓	
f		✓

Table 4.2: Names given to the deposited platinum films for UDEA V1.

tion) in an Edwards Auto 306 Vacuum Coater. The film is then exposed using deep UV light from an OAI Model 500 mask aligner with an exposure system working at a wavelength of 260 nm. As for UDEA V0, the evaporation and exposure were done at the University of Dundee. To finalise the organometallic process, the wafer is heat treated as described above for UDEA V0, with the exception of the duration of the third step, for which two hours were chosen. This leads to a structure as depicted in Figure 4.5(f). Table 4.2 shows the names given to the deposited platinum films, according to the organometallic material used. In contrast to the films used for UDEA V1, no samples were heat treated in Dundee because no equipment for whole wafers was available.

The contact holes are then defined and again etched using a CF_4/H_2 plasma (Figure 4.5(g)). It can be seen that in order to produce the contact holes it is only necessary to etch through the thin oxide and not the field oxide. Next, an aluminium layer with a thickness of 0.5 μm is sputtered on and patterned by wet etching using a mixture of phosphoric, acetic and nitric acid at a volume ratio of about 36:5:1. This approach was chosen because of the very thin platinum underlying the aluminium which does not allow any overetching. The high selectivity of a wet etching process avoids this problem even though it reduces the resolution due to underetching. Figure 4.5(h) shows the resulting structure. The front of the wafer is then coated with photoresist, all oxide removed by dry etching and 0.5 μm aluminium sputtered onto the back. Finally, the photoresist is removed, the aluminium sintered for 10 minutes in a 40% hydrogen in nitrogen atmosphere at 435 °C and a protective oxide can be deposited (Figure 4.5(i)).

Appendix B includes the runsheet, mask nomenclature and design rules which were used to produce the test chip. A picture of a typical chip is shown in Figure 4.6.

4.3 Discussion

Two different test chips with a size of approximately 1 mm² and including a range of test structures were designed and successfully manufactured.

The production of the test chips brought to light that the organometallic process lacks controllability and only a fraction of all the samples processed could be used for this work. On some samples, even features with sizes of 50 μm did not resolve, the structures disappeared completely during the heat treatment or did not show any metallic behaviour, rendering the samples useless for this work.

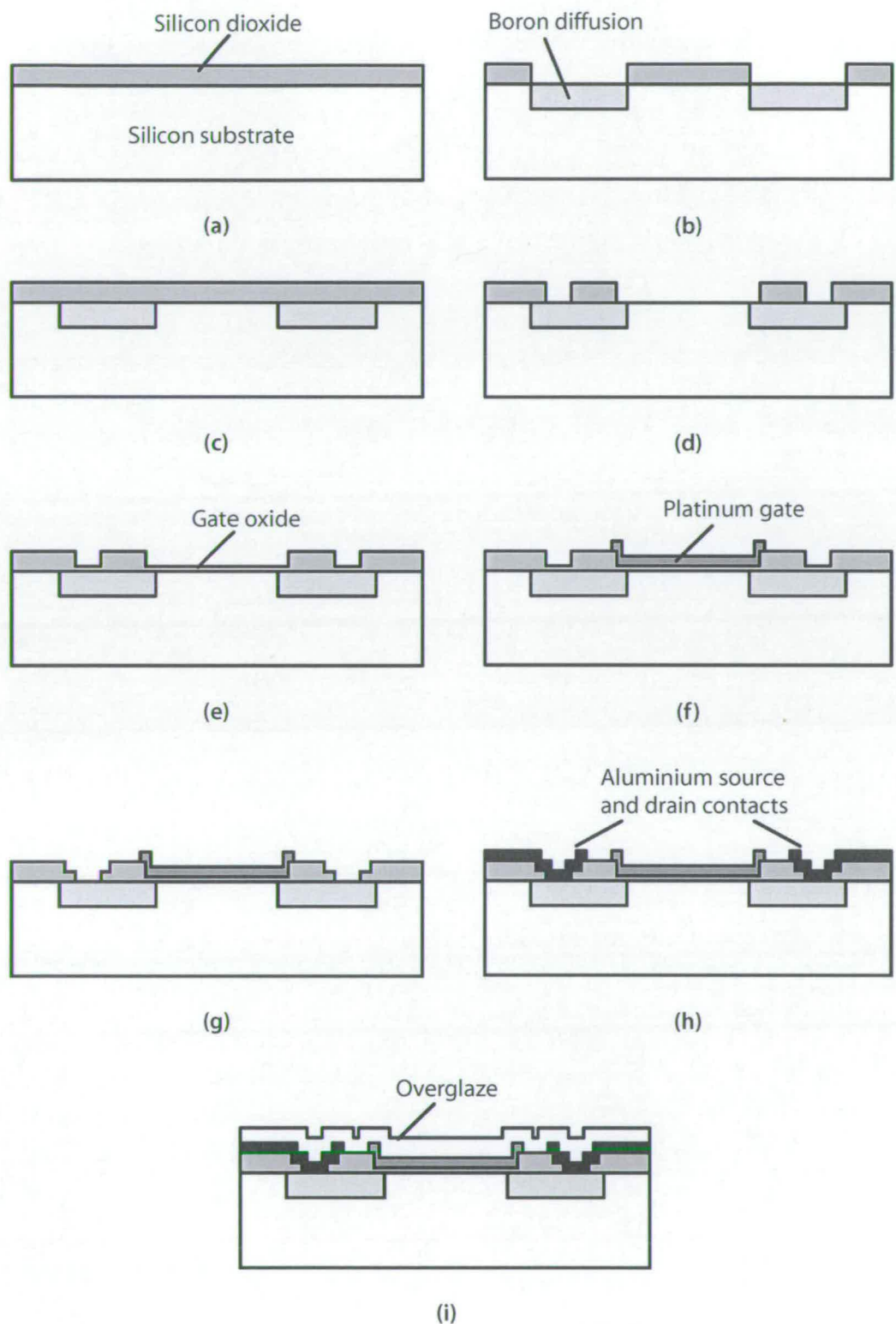


Figure 4.5: Process used to manufacture UDEA V1.

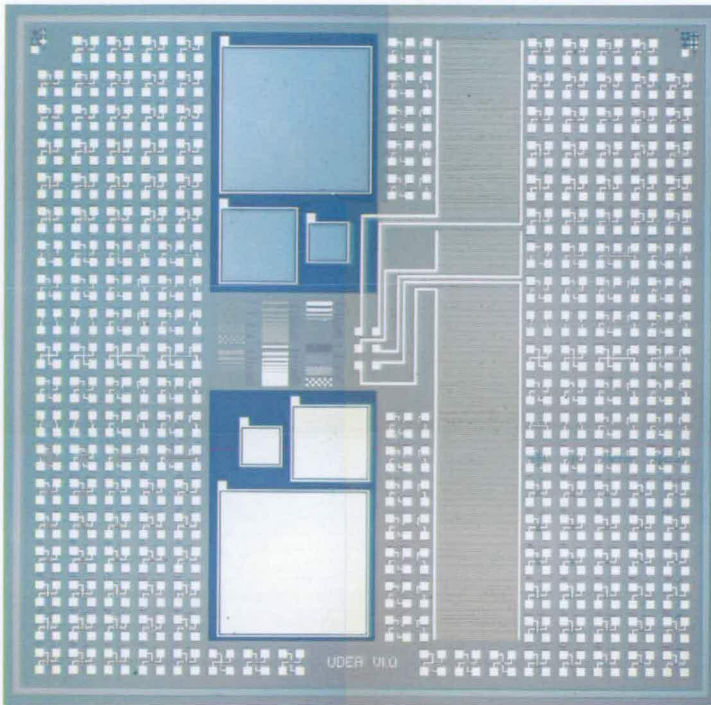


Figure 4.6: Test chip UDEA V1.

Possible reasons for the bad reproducibility can be divided into the three categories material, process and environment. Every batch of material supplied by the chemists at the University of Dundee appeared to be slightly different which could partly have been caused by the project twice being transferred between the university and AMCET Ltd, a spin-off company, and different people being involved in the synthesis of the material. Besides, the properties of the organometallics were thought to change over time. Many processing steps at the University of Dundee being done using cleanrooms and equipment which did not conform with the high standards required for semiconductor manufacturing also meant that the material was exposed to potential contaminants and light. For reasons described in Chapter 3, accurate control of the evaporation process proved to be difficult, a fact which is reflected in the results from thickness measurements presented in the following chapters.

The bad reproducibility and controllability observed during fabrication of the test chips makes the integration of the organometallic into an IC process difficult, if not impossible. Moreover, the long exposure in the range of tens of minutes or even hours is a drawback and needs to be shortened.

Resistance and dimensional measurements

5

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THE resistivity of a material used in an IC process is important because it greatly influences the speed of devices and is the most important criterion when considering a material for gates and interconnects. Interconnect lines are used to link different devices on an IC together and should ideally transfer signals without any losses and delays.

The RC time constant of an interconnect line is given by

$$RC = \frac{\rho l}{wt} \cdot \frac{\epsilon w l}{d}, \quad (5.1)$$

where ρ is the resistivity of the interconnect material, l is the length of the line, ϵ is the dielectric constant, d is the thickness of the insulating film, w is the width and t is the thickness of the conducting film [65, 66, 67].

Resistance measurements indirectly also allow the determination of the width of lines and can thus provide information about accurate control of feature size which is of great significance in modern semiconductor processing. There are other ways of measuring the actual size of a pattern, which include optical and mechanical methods [68], yet the electrical technique has the advantage of being very fast and accurate compared to the others.

5.1 Basics

5.1.1 Sheet resistance and resistivity

From Equation 5.1, it can be seen that the resistivity ρ is the key factor in the RC delay since it is affected by the interconnect material. Its measurement is therefore a simple way to determine the relative performance of an interconnect system. If the material is a semiconductor, its resistivity depends on the free electron density n , the hole density p and the electron and hole mobility μ_n and μ_p , respectively. It can be expressed by the relationship

$$\rho = \frac{1}{q(n\mu_n + p\mu_p)}, \quad (5.2)$$

where q is the electron charge.

In IC manufacturing, the sheet resistance R_S is often used to specify the resistivity. The resistance of a metal layer with length l , width w and thickness t is calculated using the expression

$$R = \frac{\rho l}{wt}, \quad (5.3)$$

where ρ is the resistivity of the material.

The sheet resistance R_S , which has the unit Ω/\square , is the resistance of a square of a film of given thickness and can be calculated by dividing the resistance by the number of squares with side length w which leads to the formula

$$R_S = \frac{Rw}{l} = \frac{\rho}{t}. \quad (5.4)$$

One of the simplest structures for measuring the resistance of a material is the bridge resistor (Figure 5.1). This structure minimises the error introduced by the contact resistance by separating the current and the voltage terminals. Such a layout is called Kelvin arrangement. To determine the resistance a current is forced through contacts C and D and the voltage drop over contacts A and B measured. The sheet resistance can then be extracted using the equation

$$R_S = \frac{V_{AB}}{I_{DC}} \cdot \frac{w}{l}, \quad (5.5)$$

where w is the width of the bridge and l the distance between contacts A and B.

Van der Pauw described a method of measuring the sheet resistance of flat samples of arbitrary shape without knowing the current pattern [69, 70]. In the theory it was assumed that the contacts are at the circumference of the sample, the contacts are sufficiently small, the sample is uniformly thick and the surface of the sample does not contain any isolated

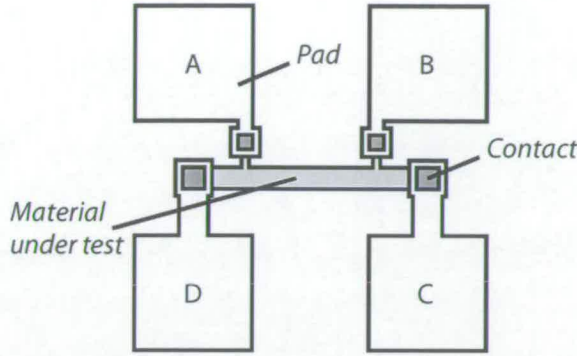


Figure 5.1: Bridge resistor test structure.

holes. For an arbitrary geometry such as the one shown in Figure 5.2,

$$R_S = \frac{\pi}{\ln(2)} \cdot \frac{R_{AB,CD} + R_{BC,DA}}{2} \cdot F \quad (5.6)$$

where $R_{AB,CD} = V_{CD}/I_{AB}$, $R_{BC,DA} = V_{DA}/I_{BC}$ and F is the van der Pauw correction factor. The correction factor depends on the factor $R_{AB,CD}/R_{BC,DA}$ according to the relation

$$\cosh \left[\frac{\frac{V_{DA}}{I_{BC}} - 1}{\frac{V_{DA}}{I_{BC}} + 1} \cdot \frac{\ln(2)}{F} \right] = \frac{1}{2} \exp \frac{\ln(2)}{F}. \quad (5.7)$$

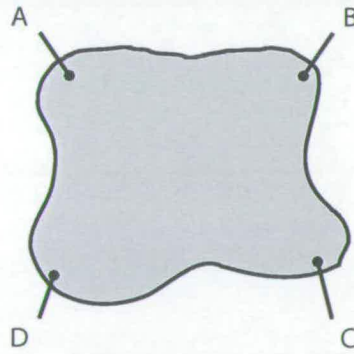


Figure 5.2: Arbitrary shaped sample connected for van der Pauw resistivity measurements.

In case of a symmetrical structure the correction factor F is 1 and the formula can be simplified. The Greek cross (Figure 5.3) was confirmed to be a symmetrical van der Pauw structure with finite contacts if the arm length is greater than the arm width [71, 8]. It is widely used to measure the sheet resistance.

$$R_S = \frac{\pi}{\ln(2)} \cdot R_{AB,DC} = \frac{\pi}{\ln(2)} \cdot \frac{V_{DC}}{I_{AB}} \quad (5.8)$$

The influence of surface leakage current and joule heating have been experimentally studied with various test structures [72,63].

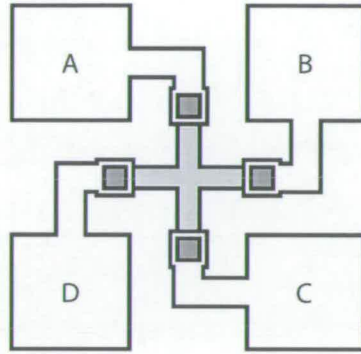


Figure 5.3: Greek cross test structure.

5.1.2 Contact resistivity

Due to decreasing feature sizes on semiconductor circuits, contact resistance and thus contact resistivity is becoming an important factor in semiconductor processing. Berger [73] defined contact resistance R_C as the difference between the resistance expected from an ideal contact and from an actual contact. Assuming a homogeneous current flow through the contact, the contact resistivity ρ_C can be estimated by multiplying the contact resistance by the contact area. There are several ways of experimentally determining the contact resistivity of which the TLM (Transmission Line Model) [74] was one of the most popular in the past. However, this model has the disadvantages that the dimensions of the test structure must be known exactly and there is more than one measurement necessary. Proctor and Linholm [75] made a different approach by using a four-terminal contact resistance test structures like the one shown in Figure 5.4. The measurement proposed is a Kelvin measurement and the resistance introduced by the current and voltage taps does therefore not influence the result. Different layouts of the four-terminal contact resistance test structure and their influence on the resistance values measured have been investigated [76,77,78].

$$R_C = R_{AC,DB} = \frac{V_D - V_B}{I_{AC}} \quad (5.9)$$

5.1.3 Linewidth measurements

The cross bridge resistor test structure [79,80] shown in Figure 5.5 is often used to measure the linewidth electrically and consists of a Greek cross and a bridge resistor, both of which were dealt with earlier.

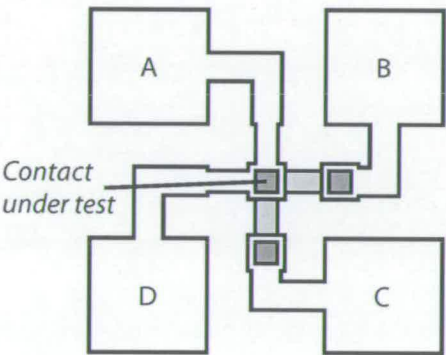


Figure 5.4: Kelvin test structure used for contact resistivity measurements.

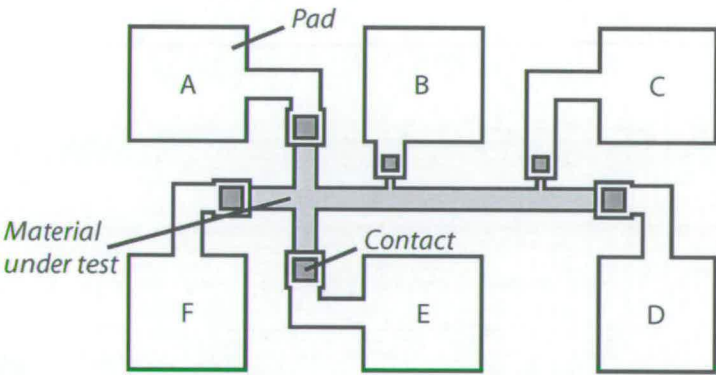


Figure 5.5: Line width test structure.

First of all, the sheet resistance R_S of the film is determined using pads A, B, E and F connected to the Greek cross. Then, the resistance R_B of the bridge is measured and used together with the sheet resistance R_S to calculate the linewidth W_B from the equation

$$W_B = \frac{R_S L_B}{R_B}. \quad (5.10)$$

5.1.4 Resistivity of thin films

The resistance of a crystalline material is the result of electrons scattering at impurities, lattice imperfections and phonons. The average distance travelled in a conductor by an electron between two collisions is called the electron mean free path l and is one of the main factors influencing the resistivity of a material. It is defined as

$$l = v_F \tau, \quad (5.11)$$

where v_F is the velocity at the Fermi surface and τ the mean free time between two collisions [81,82]. v_F can be calculated from

$$v_F = \left(\frac{9\pi}{4} \right)^{\frac{1}{3}} \frac{h}{2\pi m \tau_s} \quad (5.12)$$

with h being the Plank's constant, m the electron mass and τ_s the volume of a sphere whose volume is equal to the volume per conduction electron. Values of τ_s for a variety of materials have been published in the literature [83]. The relationship between the electrical resistivity and τ can be written as

$$\rho = \frac{4\pi \tau_s^3 m}{3q^2 \tau}. \quad (5.13)$$

Using Equations 5.12 and 5.13 in Equation 5.11, it is possible to calculate the electron mean free path from a known resistivity value. Table 5.1 lists calculated values for the electron mean free path and compares them to data available in the literature.

The above model illustrates that reflections of electrons at the surface will increase the electrical resistivity of a thin film. Fuchs [85] and Sondheimer [86] examined the rise of resistance with decreasing film thickness due to the reduction of the electron mean free path and developed suitable models. Mayadas and Shatkyes [87] used an approach which also included the scattering at grain boundaries. These boundaries usually have little effect on the resistivity of a film because the electron mean free path is much larger than the grain size. However, if the films are very thin, the distance between the grain boundaries is smaller than the electron mean free path and thus the influence of the scattering at the grain boundaries can not anymore be neglected. Both, the scattering of an electron at the film surfaces and grain boundaries are depicted in Figure 5.6.

Metal	Resistivity at 293 K [46] [10 ⁻⁸ Ωm]	r _s [83] [10 ⁻¹⁰ m]	Calculated mean free path ^a [nm]	Calculated mean free path [84] [nm]	
				0 °C	100 °C
Li	8.55 ^b	3.13	37.8	11.3	7.9
Cu	1.6730	2.25	99.9	42.1	29.4
Ag	1.59	2.61	141.5	57.5	40.5
Au	2.35	2.54	90.7	40.6	29.0
Ni	6.84	2.14	22.1	13.3	8.0
Co	6.24	2.08	22.9	13.0	7.9
Fe	9.71	2.06	14.4	22.0	15.6
Al	2.6548	2.42	69.9	–	–
Pt	10.6	2.37	17.5	11.0	7.9

^acalculated using Equation 5.11 and r_s data from [83]

^bat 273 K

Table 5.1: Electron mean free path of some metals.

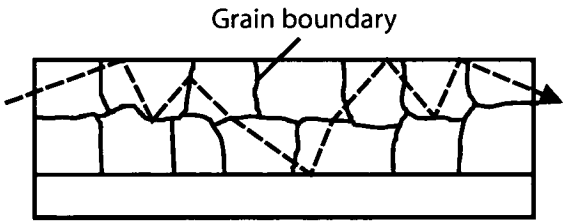


Figure 5.6: Scattering of an electron at the film surfaces and grain boundaries.

Later investigation showed that quantum effects have to be taken into account so as to get adequate results even if the films are very thin and of high purity [88,89,90].

5.2 Materials and methods

5.2.1 Test structures

Four main categories of films were electrically characterised, namely structures deposited from $(C_3F_7)_2Pt^{II}C_8H_{12}$ and $(C_3F_7)(CH_3)Pt^{II}C_8H_{12}$ manufactured at either University of Dundee or University of Edinburgh. Resistivity test structures available on both UDEA V0 and UDEA V1 were used and the names given to distinguish different films are the ones given in Table 4.1 and Table 4.2. If nothing else is mentioned, the samples were produced using the process described in Chapter 4. Due to a very limited number of test structures available, most results are based on a single measurement at one structure.

5.2.2 Measurement setup

The resistance measurements at the test structures were done using a HP 4156B Semiconductor Parameter Analyzer. The sample was placed on a chuck in a metal box which was lightproof and maintained at ground potential. Movable tungsten probes were employed to make electrical contact between the test structures and the measurement equipment.

5.2.3 Measurement procedure

To measure the sheet resistance using the Greek cross structure described in Section 5.1.1, the following procedure was followed. First of all, a current was forced from A to B (Figure 5.3) and the voltage measured at the two remaining pads. The direction of the current was then reversed and the voltage measured again. The procedure was then repeated using A and D as current pads and measuring the voltage at B and C. The sheet resistance was finally calculated by taking the average of resistivity values calculated from all four measurements. To get reliable values, each voltage used to determine the resistivity was based on the average of ten measurements.

To obtain the resistance using bridge resistors (Figure 5.1), a current was first forced in one direction (from pad D to C) and the resistance calculated using the voltage drop, measured at pads A and B. The current was then inverted and the average of both measurements, together with known dimensional information of the bridge, used to compute the resistivity. Again, the resistance values used for the calculation of the resistivity were the result of ten single measurements.

The determination of the contact resistance using the four-terminal contact resistance test structure is done in a similar way as the procedure described for the sheet resistance. The

Film	Sheet resistance [Ω/\square]		
	Bridge resistor	Greek cross	
	$l = 350 \mu\text{m} / w = 10 \mu\text{m}$	$w = 10 \mu\text{m}$	$w = 5 \mu\text{m}$
a	26.93	28.09	37.09
b ^a	132.13	90.42	102.57
c	3.30	3.17	4.18
d	–	–	–

^aheat treated for six hours at 435 °C

Table 5.2: Resistivities for the different films measured using Greek cross and bridge resistor test structures on UDEA V0.

contact resistance is first measured by forcing a current from A to C and measuring the voltage drop from D to B (Figure 5.4). Next, the current is reversed and the resistance measured again. The voltage pads are then exchanged with the current pads and the measurement sequence repeated. Averaging the values from the four measurements leads to the contact resistivity.

The procedure employed to electrically measure the linewidth using the crossbridge resistor (Figure 5.5) begins as the one for the Greek cross structure, the only difference being that the narrow line connected to pad B can not be used to force the measurement current because it is only capable to carry small currents. After the sheet resistance has been determined using the Greek cross between pads A, B, F and E, a measurement current is forced from pad E to pad D and the resistance calculated using the voltage drop over pads B and C. The current is then inverted and the average of both measurements, together with the sheet resistance measured before, used to compute the width of the line. All resistance values used for the calculation were the result of ten single measurements.

A Dektak 8000 profilometer was used to mechanically acquire information about the profile of the features.

5.3 Results and Discussion

The results of resistance measurements on test structures on UDEA V0 and UDEA V1 are listed in Table 5.2 and Table 5.3, respectively.

The tables show a large discrepancy between sheet resistance values measured using Greek crosses of different size and bridge resistors, suggesting errors in the measurements. This seems to be caused by variations of the film structure over the sample and the profile of the tracks which is included differently in the results from the two types test structures. The cross-section of the lines does not resemble a rectangular shape, as it can be seen in Figure 1.4(b). The extraction of the sheet resistance from measurements at bridge resistors and

Film	Sheet resistance [Ω/\square]		
	Bridge resistor	Greek cross	
	$l = 200\text{ }\mu\text{m} / w = 10\text{ }\mu\text{m}$	$w = 10\text{ }\mu\text{m}$	$w = 5\text{ }\mu\text{m}$
e	32.13	32.62	34.37
f	31.25	–	–

Table 5.3: Resistivities for the different films measured using Greek cross and bridge resistor test structures on UDEA V1.

Greek crosses assumes a uniform film thickness over the whole area of the film, errors are therefore likely to occur in the cases shown in Table 5.2 and Table 5.3 above. A solution to the problem is the measurement of the cross-section of a line at different positions along a bridge resistor test structure as shown in Figure 5.7. This data, together with the resistance measured electrically, is then used to calculate an average cross-section area and to compute the resistivity.

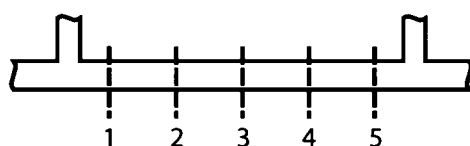
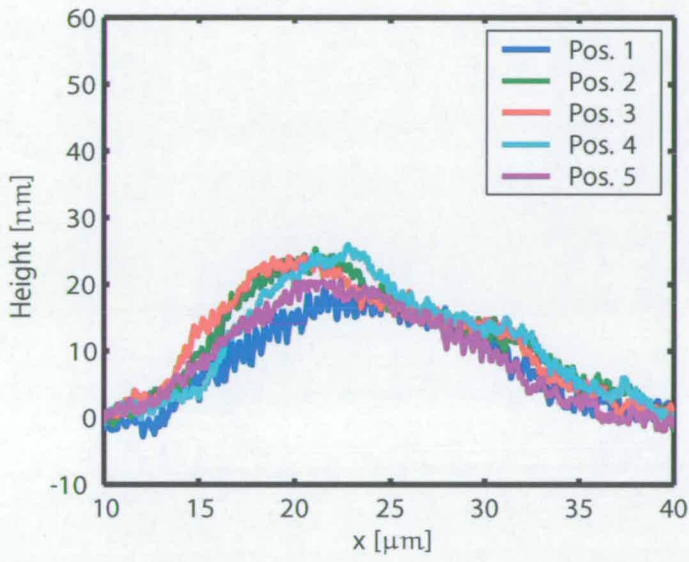


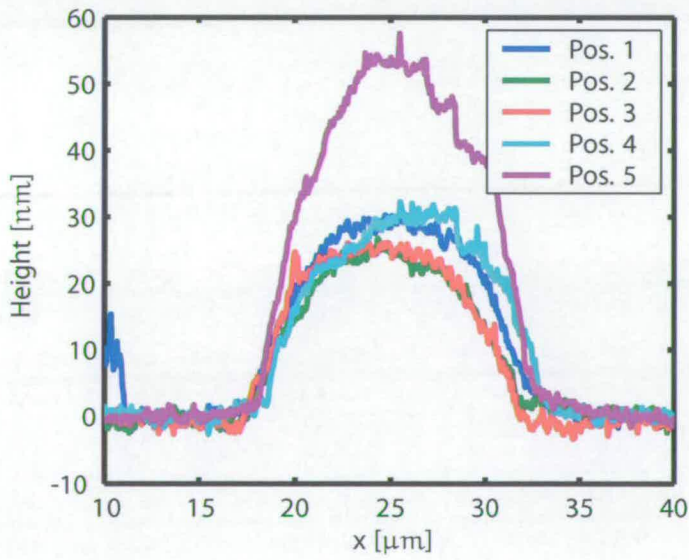
Figure 5.7: The positions of the five profiles obtained from each bridge structure to calculate the average area of the cross section.

To determine the resistivity of a film, the resistance of lines of bridge resistors with a linewidth of $10 \mu\text{m}$ and a length of $350 \mu\text{m}$ on UDEA V0 and of $200 \mu\text{m}$ on UDEA V1 was measured. The cross-section of the lines was then obtained by a profilometer at five different positions, separated by spaces of approximately equal size. Graphs of the measured profiles of different films are shown in Figure 5.8, Figure 5.9 and Figure 5.10. It can be seen that the cross sectional area of the films varies widely over the length of the line. The measurements also indicate that the lines are generally larger than expected. A small proportion of the difference between the actual linewidth and the width on the mask can be attributed to errors introduced by the profilometer which are investigated in Appendix C. Yet the error from the profilometer is small and the resistance and profile data is accurate enough to allow the calculation of the resistivity of which the results are listed in Table 5.4 and Table 5.5.

All films characterised have resistivities which are significantly higher than the reported bulk resistivity of platinum which is $1.06 \cdot 10^{-7} \Omega\text{m}$ [46]. For reasons explained in Section 5.1.4, thin films have higher resistivities than the bulk material but Avrekh, Monteiro and Brown [91] reported an increase as we have measured it only for film thicknesses below 5 nm . The resistivity of film c, resulting from the organometallic material $(\text{C}_3\text{F}_7)(\text{CH}_3)\text{Pt}^{\text{II}} - \text{C}_8\text{H}_{12}$, is closest to the value expected. It is believed that organic residues in the metal lay-

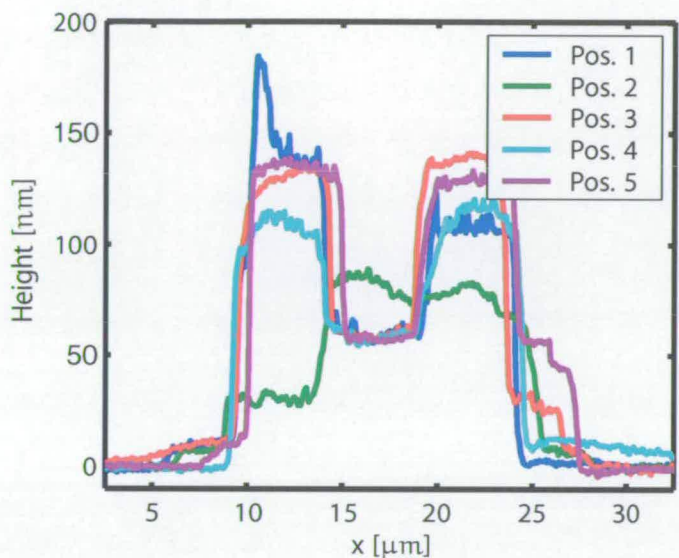


(a) Film a.



(b) Film b.

Figure 5.8: Profiles of bridge resistor structures on UDEA V0 obtained by a profilometer.



(a) Film c.

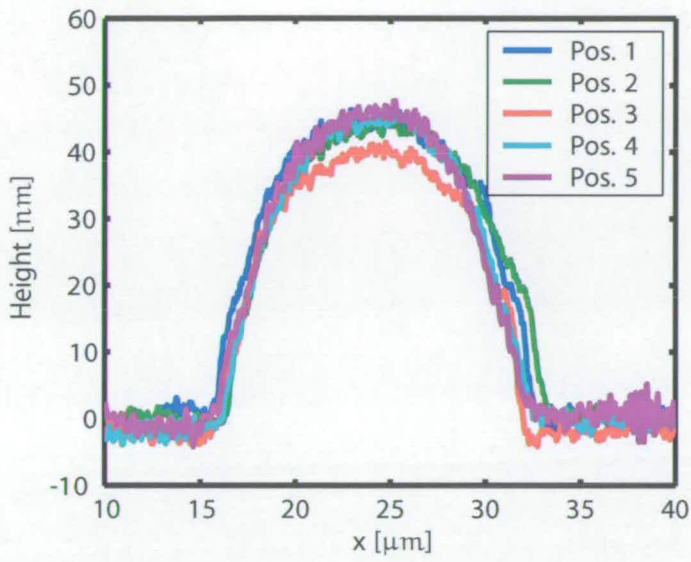
Figure 5.9: Profiles of bridge resistor structures on UDEA V0 obtained by a profilometer.

Film	Area [m ²]	Resistance [Ω]	Resistivity [Ωm]
a	$3.1412 \cdot 10^{-13}$	942.44	$8.4582 \cdot 10^{-7}$
b	$3.4652 \cdot 10^{-13}$	4624.47	$4.5784 \cdot 10^{-6}$
c	$1.4812 \cdot 10^{-12}$	115.59	$4.8917 \cdot 10^{-7}$
d	–	–	–

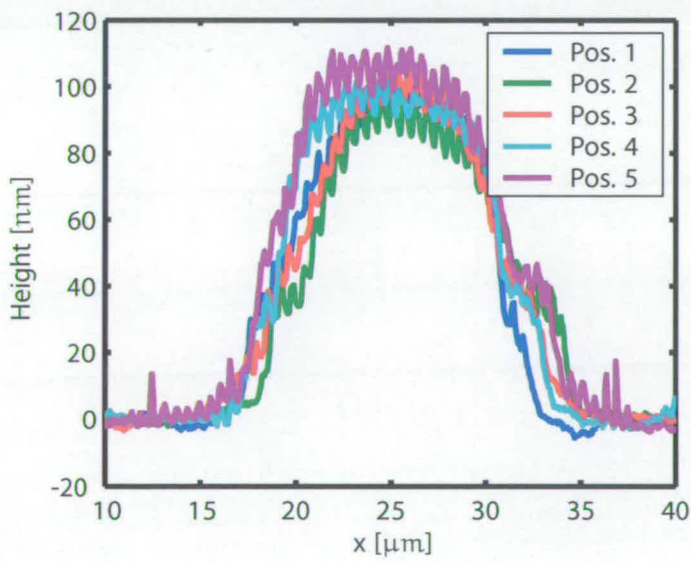
Table 5.4: Calculated resistivities of the different films based on the cross-section area measured at five positions of a bridge resistor on UDEA V0.

Film	Area [m ²]	Resistance [Ω]	Resistivity [Ωm]
e	$5.3734 \cdot 10^{-13}$	642.637	$1.7266 \cdot 10^{-6}$
f	$1.1528 \cdot 10^{-12}$	625.125	$3.6033 \cdot 10^{-6}$

Table 5.5: Calculated resistivities of the different films based on the cross-section area measured at five positions of a bridge resistor on UDEA V1.



(a) Film e.



(b) Film f.

Figure 5.10: Profiles of bridge resistor structures on UDEA V1 obtained by a profilometer.

ers may be responsible for some of the difference in conductivity. Contaminants like carbon from the organometallic precursor gas are also thought to be the cause of measured high resistivities of platinum films deposited using a FIB (Focused Ion Beam) system [92] and a solid organometallic material could behave likewise. It must be noted that the conductivity of the films produced is superior to most of the films deposited in a similar manner and reported in the literature, as it can be seen from Table 2.3.

To further investigate the resistivity of the platinum films deposited by the organometallic process, its dependence on the duration of the last heat treatment step was measured using film b and the results are shown in Figure 5.11. The sheet resistance decreases significantly

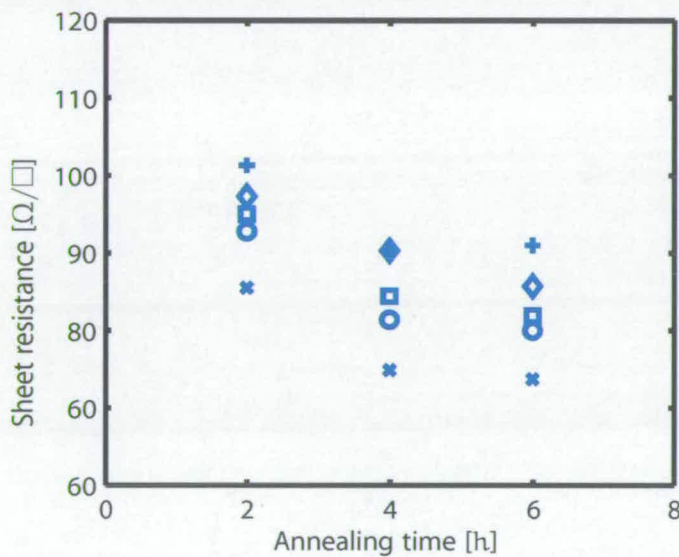


Figure 5.11: Influence of annealing time on the sheet resistance of the deposited films. The data was obtained from measurements at different locations on a wafer.

with increasing annealing time and a trend towards an asymptotical value can be observed.

Using linewidth test structures [79] made of film e available on UDEA V1, deposited platinum tracks of different widths were electrically characterised. The results for linewidths of 3 μm , 5 μm , 10 μm and 20 μm are shown in Figure 5.12 and deviations of up to 23% from the width on the photo mask were observed. The profilometer was again employed to mechanically measure the cross-section of the tracks on the chip and Figure 5.13 depicts the profiles obtained. The shape of the profiles agrees with those shown in Chapter 5, the sidewalls are again not perpendicular and the tracks are significantly wider than the ones on the photo mask. The lines on the chip are up to 50% broader at their half-height than on the mask and the percentage error decreases with increasing line width. A width of approximately 10 μm seems to be the minimum effective size of a line, independent of the feature size on the mask. The electrical linewidth measurements, together with the results from the profilometer, sug-

gest that the outcome of the measurement of the linewidth using bridge resistors depends on the profile and leads to a discrepancy between the electrically measured width and the mechanically acquired width of the line at its half-height.

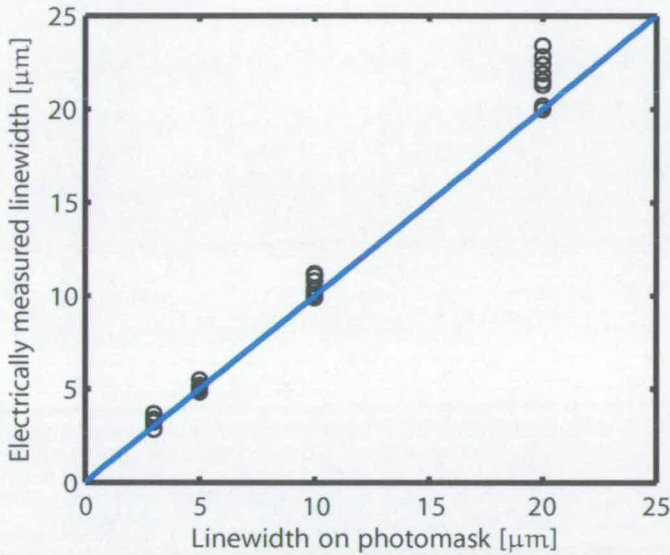


Figure 5.12: Comparison of the linewidth measured electrically and the linewidth on the mask. The circles represent measurements at different positions on the wafer.

The results presented in this chapter lead to the conclusion that the features produced using the organometallic process do not possess characteristics adequate for an application in semiconductor manufacturing. The resistivity of the films is significantly higher than the one of pure platinum and the minimum feature sizes achievable are considerably larger than the smallest metal patterns on integrated circuits. Nonetheless, the properties of the platinum features are better than those of films resulting from other organometallic processes found in the literature.

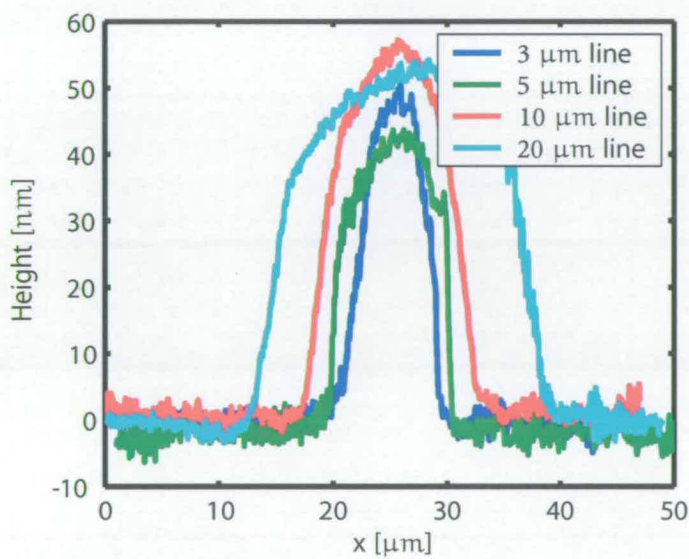


Figure 5.13: Profiles of lines of different width measured with a profilometer.

Capacitance measurements

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ONE of the most important parts of a MOS (Metal Oxide Silicon) transistor is the MOS diode formed by the gate, the insulator and the transistor bulk. The characterisation of this structure can therefore be used to evaluate the suitability of a material or process for manufacturing MOS transistors and important process data can be gathered.

There are different methods of investigating the electrical properties of the MOS system or more generally the MIS (Metal Insulator Semiconductor) system. C-V (capacitance versus voltage) measurements of MOS capacitors [93, 5, 94, 95] are a good method to evaluate the potential performance of gate stacks. This technique features a simple test structure. The evaluation is made by either comparing the curves to a calculated ideal or analysing parameters (e.g. threshold voltage, oxide charge) which have been extracted from the measured data.

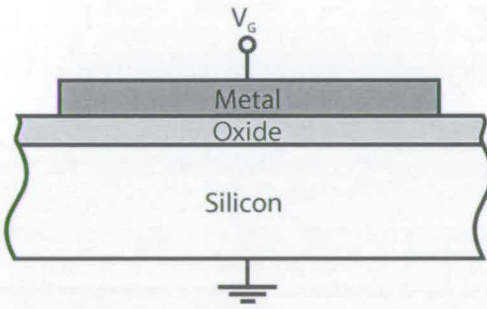
6.1 Basics

The explanation of the basic theory behind the MOS capacitor roughly follows the one by Nicollian and Brews [5], although some changes were made to make it consistent with the rest of the thesis.

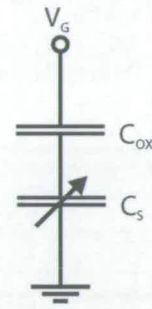
6.1.1 MOS capacitor

A MOS (metal oxide semiconductor) capacitor consists of a metal gate, an oxide layer and a silicon substrate which form a voltage dependent structure. Its physics and technology have been described in the literature by many authors [93, 5, 96, 97]. A typical structure is shown in Figure 6.1(a) with the total capacitance C per unit area consisting of a voltage independent part C_{Ox} and a voltage dependent part C_S (Figure 6.1(b)).

$$C = \frac{1}{\frac{1}{C_{Ox}} + \frac{1}{C_S}} = \frac{1}{\frac{\epsilon_{Ox}}{t_{Ox}} + \frac{1}{C_S}}. \quad (6.1)$$



(a) Construction of a MOS capacitor.



(b) Equivalent circuit of an ideal MOS capacitor.

Figure 6.1: MOS capacitor.

6.1.2 Definition and sign conversion of potentials

In the succeeding sections, different potentials are used to explain the behaviour of the MOS structure. They are shown in Figure 6.2. The potential $\phi(x)$ is defined by

$$\phi(x) = \frac{1}{q} [E_F - E_i(x)], \quad (6.2)$$

where E_F is the Fermi level and E_i the intrinsic energy level. Deep in the bulk where the energy bands run straight, $\phi(x)$ is called the bulk potential ϕ_B which can be written as

$$\phi_B = \frac{1}{q} [E_F - E_i(\infty)] \quad (6.3)$$

which leads to

$$\phi_B = \frac{kT}{q} \cdot \ln \left(\frac{N_D}{n_i} \right) \quad (6.4)$$

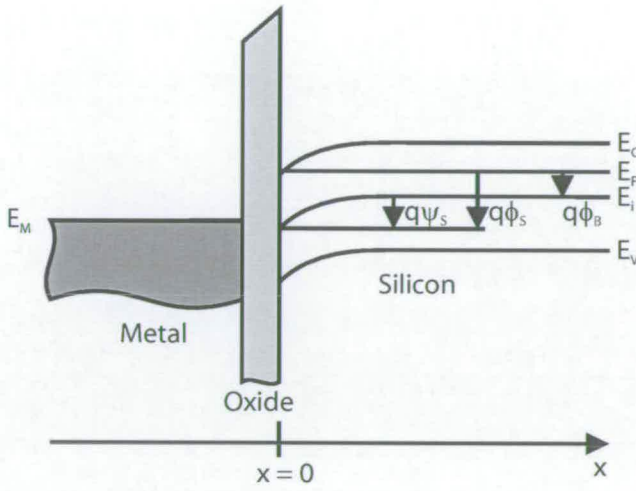


Figure 6.2: Potentials in a MOS structure.

for n-type silicon and

$$\phi_B = -\frac{kT}{q} \cdot \ln \left(\frac{N_A}{n_i} \right) \quad (6.5)$$

for p-type silicon. The band bending $\psi(x)$ is defined as

$$\psi(x) = \phi(x) - \phi_B. \quad (6.6)$$

At the silicon surface Equation 6.6 becomes

$$\psi_S = \phi_S - \phi_B \quad (6.7)$$

where ϕ_S is the surface potential.

6.1.3 Ideal MOS capacitor

When no voltage is applied to the metal gate of an ideal MOS capacitor the energy levels at the interface between silicon and silicon oxide are the same as in the bulk silicon. This case is called flatbands and is defined as the point where the band bending at the silicon surface is zero (Figure 6.3).

If a positive voltage is applied to the metal gate ($V_G > 0$) of a MOS structure with n-type silicon as bulk material, majority carriers are accumulated at the silicon surface and the energy bands will bend down. This case is called accumulation (Figure 6.4).

A negative gate voltage ($V_G < 0$) attracts holes to the silicon surface so that the bands bend up. The reduction of the majority carrier density at the silicon surface results in the creation of a depletion zone below the oxide in the silicon (Figure 6.5).

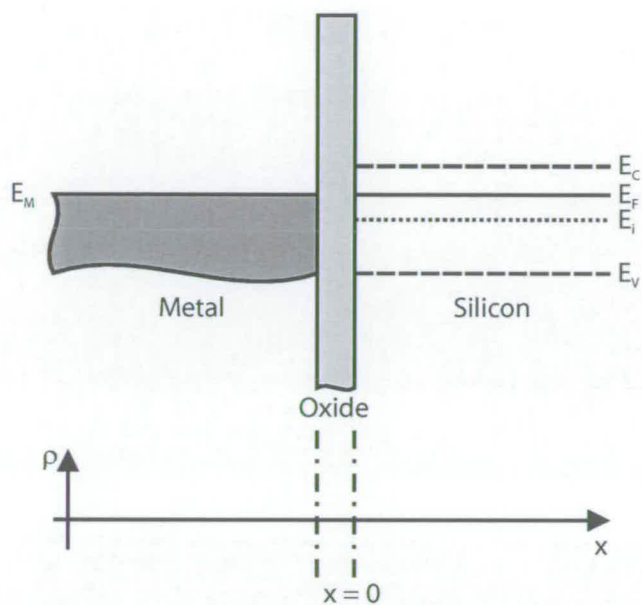


Figure 6.3: Band diagram of a MOS structure at flatband condition (n-type substrate).

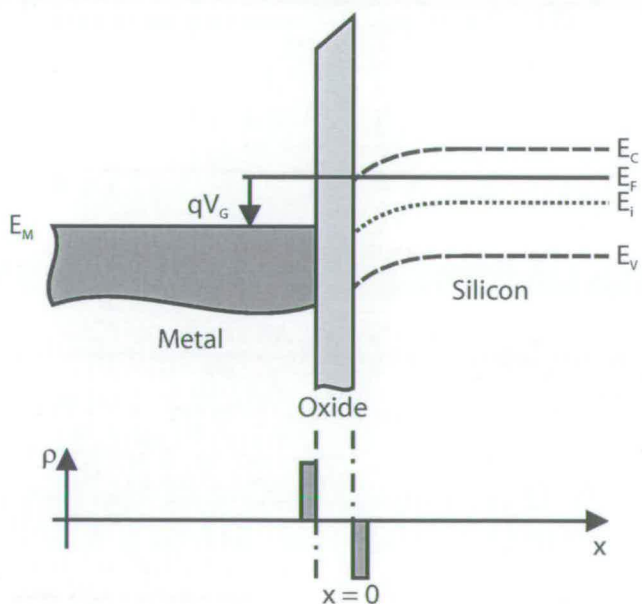


Figure 6.4: Band diagram of a MOS structure in accumulation (n-type substrate).

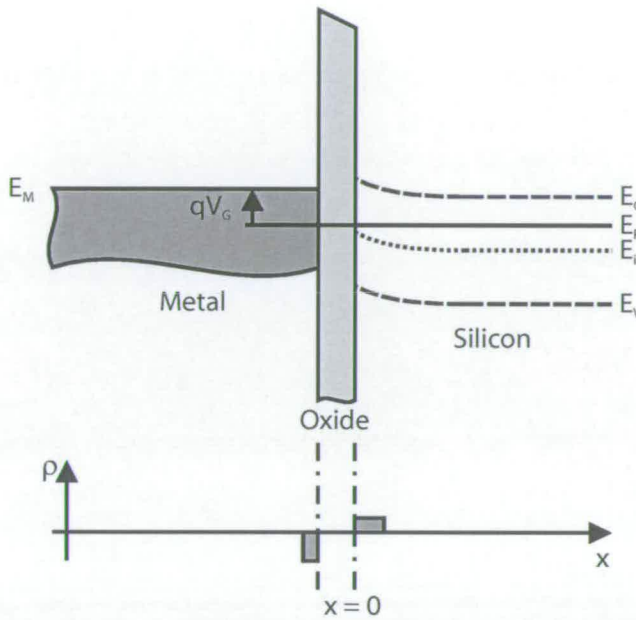


Figure 6.5: Band diagram of a MOS structure in depletion (n-type substrate).

Further reduction of the voltage at the metal gate leads to a point where the minority carrier density at the silicon surface exceeds the majority carrier density at the silicon surface. A state called weak inversion is reached (Figure 6.6).

If the minority carrier density at the silicon surface exceeds the majority carrier density in the bulk we talk about strong inversion. It is reached when the band bending at the silicon surface equals twice the bulk potential which can be expressed by $\psi_S = 2\phi_B$ (Figure 6.7).

6.1.4 Real MOS capacitor

In the previous section it was assumed that band bending is zero when no voltage is applied to the gate material and that the field in the isolator is uniform. However, the behaviour of a practical MOS capacitor will deviate from the ideal model. The non-idealities causing this deviations are described in this section.

6.1.4.1 Workfunction difference

The work function of the gate material is likely to be different from the workfunction of the silicon used as substrate. If this is the case and there is an electrical connection between gate and substrate, electrons will travel from the material with the higher workfunction difference to that with the lower. The substrate will be charged until the Fermi potential of the silicon reaches the Fermi potential of the gate (Figure 6.8). The potential needed to settle the difference is called the workfunction difference W_{MS} . It equals the flatband voltage V_{FB} if oxide charges are neglected.

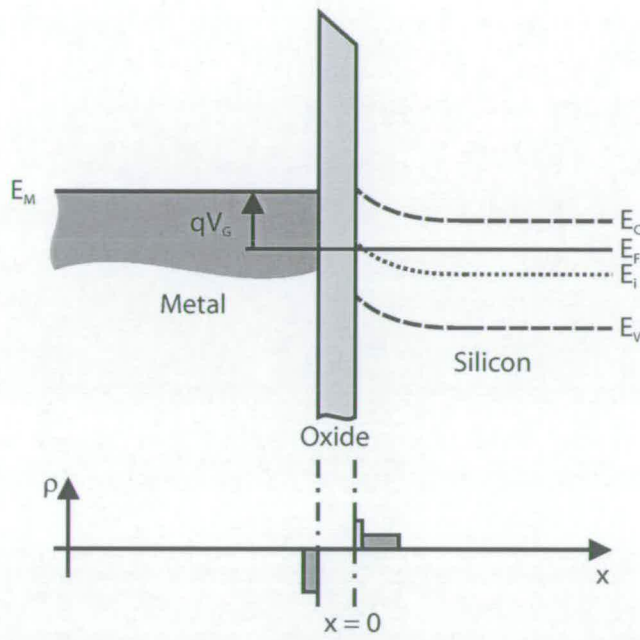


Figure 6.6: Band diagram of a MOS structure in weak inversion (n-type substrate).

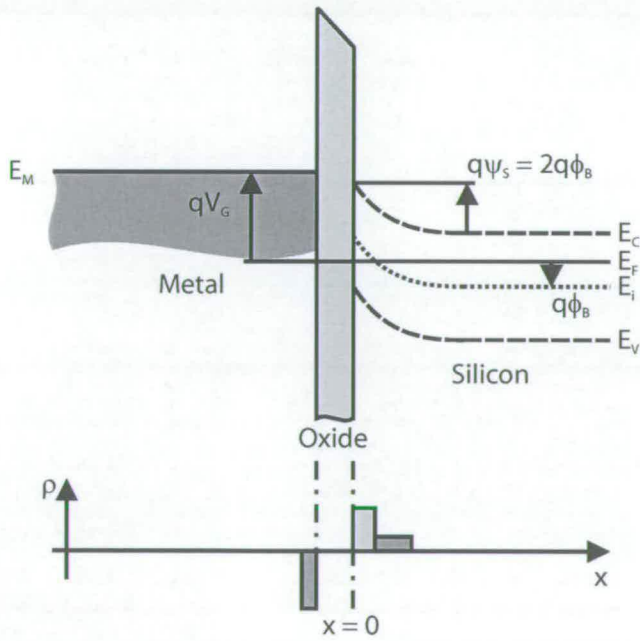


Figure 6.7: Band diagram of a MOS structure in strong inversion (n-type substrate).

The presence of the oxide in a MOS structure has an influence on the barrier height between the materials involved. Measured values of the barrier height between a material (e. g. aluminium) and silicon oxide [98] are therefore commonly used to calculate the workfunction difference. The according equation is

$$W_{MS} = W_M - W_S = \phi_{MO} - \phi_{SO} + \frac{E_g}{2q} + \phi_B \quad (6.8)$$

where ϕ_{MO} is the barrier height between metal and oxide, ϕ_{SO} between silicon and oxide and E_g is the silicon bandgap.

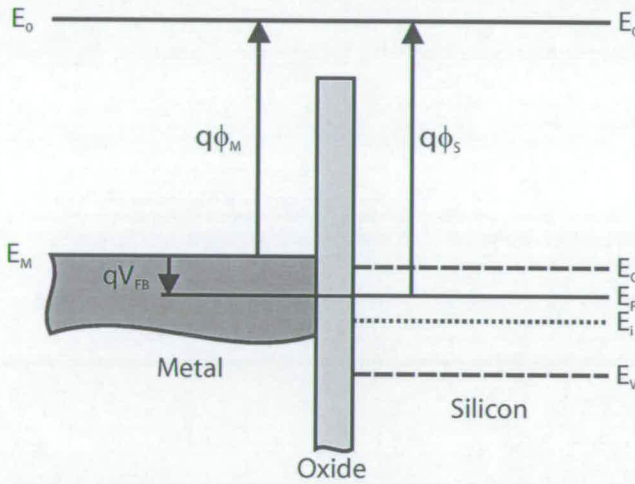


Figure 6.8: Workfunction difference.

6.1.4.2 Charges in the silicon dioxide layer

In contrast to the ideal case there exist charges in the oxide of a real MOS capacitor (Figure 6.9). These charges affect the characteristic of the capacitor. The charges can be classified into four different types which are shown in the figure below.

Oxide fixed charge. Oxide fixed charge Q_f is located near the silicon/silicon dioxide interface and is always positive.

Oxide trapped charge. Oxide trapped charge Q_{ot} is situated either at the silicon/silicon dioxide interface or close to it.

Mobile ionic charge. Mobile ionic charge Q_m is most commonly caused by the presence of ionised alkali metal atoms. The ions are located either at the metal/silicon dioxide interface or at the silicon/silicon dioxide interface. The atom originally entered the silicon dioxide at

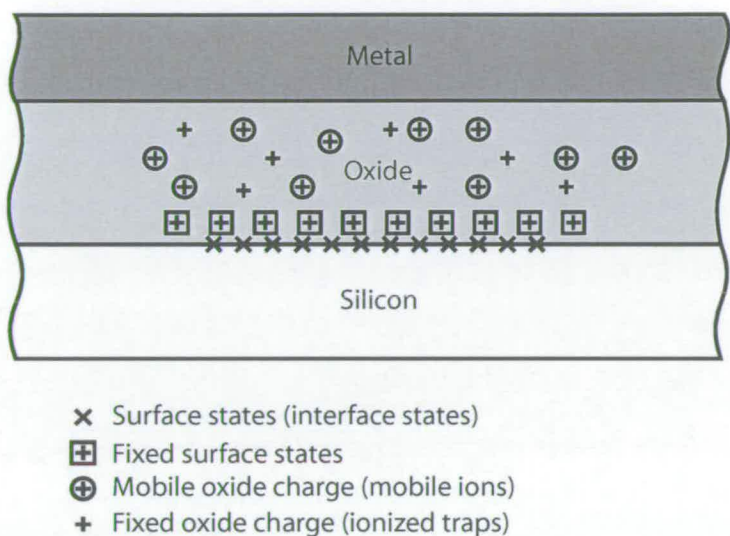


Figure 6.9: Charges in the MOS structure

the metal/silicon dioxide interface. As the name says this type of charge is mobile. The drift in the silicon dioxide depends on the temperature and the applied electric field.

Interface trapped charge. Interface trapped charge Q_{it} is located at the silicon/silicon dioxide interface. It exists due to the interruption of the periodic lattice structure. Interface traps can respond to frequencies up to about 100 MHz. If the measurement frequency is below the response frequency the equivalent circuit of the MOS capacitor looks as shown in Figure 6.10(a). At higher frequencies the MOS capacitor can be represented by the circuit shown in Figure 6.10(b).

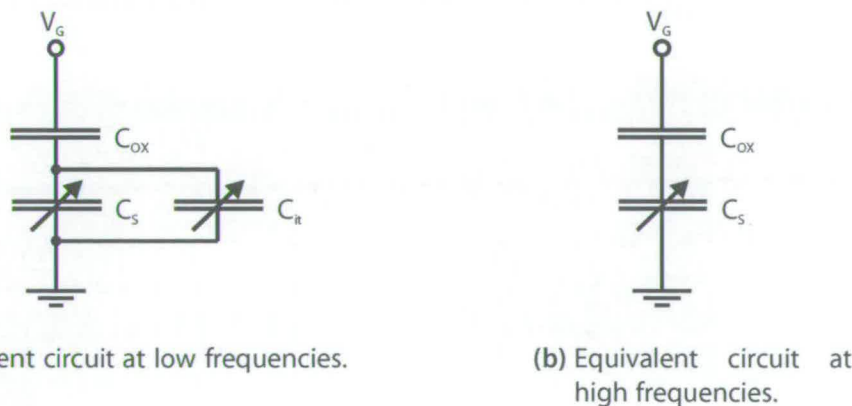


Figure 6.10: Equivalent circuit of a MOS capacitor with interface traps at both low and high frequencies.

6.1.5 Capacitance of MOS capacitor

In practice the capacitance of a MOS capacitor can be measured in two ways. The first method is based on the measurement of the charge moved when changing the bias voltage. It is called low frequency or quasi-static method. The second method measures the capacitance by the phase shift between voltage and current when applying a high frequency voltage (commonly 1 MHz) superimposed on a bias voltage to the capacitor. It is called the high frequency method. This chapter explains the curves gained by the different methods and shows the derivation of both the low frequency and the high frequency capacitance. A third kind, the deep depletion capacitance is also explained. The capacitance formulas gained as a result are later used to simulate curves and analyse measured data. Typical shapes of C-V curves [99, 100] of all three types are shown for capacitors on both n-type and p-type substrates in Figure 6.11. For the derivations a MOS structure as shown in Figure 6.1 was assumed and measures for charge and capacitance are per unit area.

6.1.5.1 Low frequency capacitance

The low frequency capacitance is derived by solving the Poisson equation

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_{Si}}. \quad (6.9)$$

The charge density in the Poisson equation can be expressed by

$$\rho(x) = q[p(x) - n(x) + N_D - N_A] \quad (6.10)$$

where N_D is the electron density in the bulk, N_A is the hole density in the bulk,

$$n(x) = n_i e^{\frac{q\phi(x)}{kT}} \quad (6.11)$$

and

$$p(x) = n_i e^{\frac{-q\phi(x)}{kT}}. \quad (6.12)$$

The charge density in the bulk

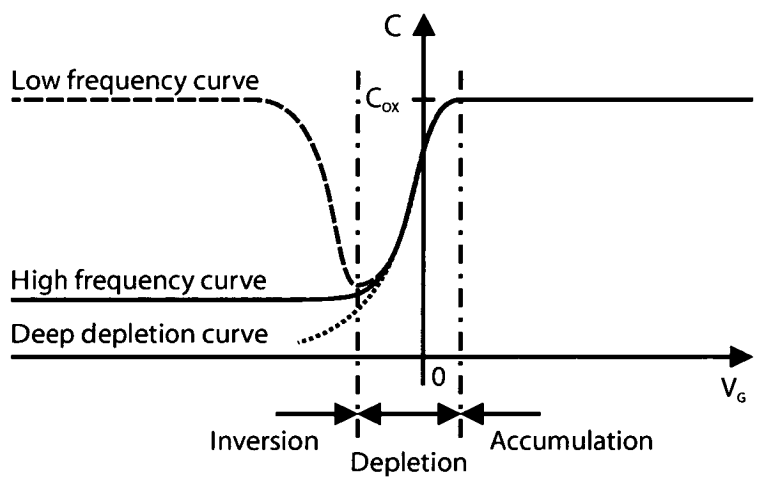
$$\rho(\infty) = p(\infty) - n(\infty) + N_D - N_A = 0. \quad (6.13)$$

Using Equation 6.4 and Equation 6.5 the carrier densities in the bulk can be calculated by

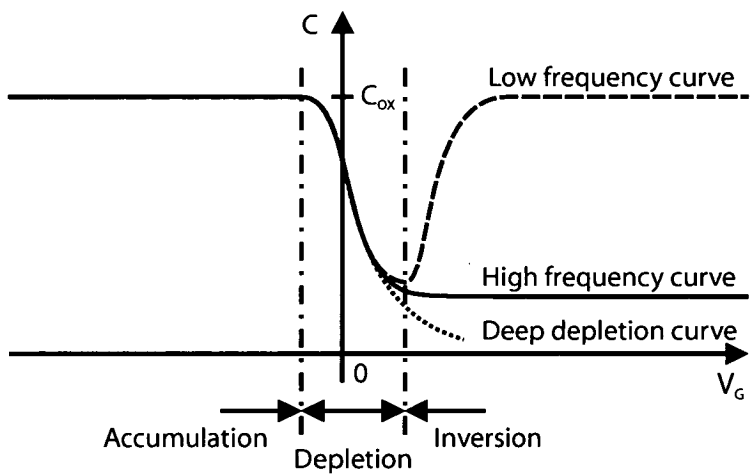
$$N_D = n(\infty) = n_i e^{\frac{q\phi_B}{kT}} \quad (6.14)$$

and

$$N_A = p(\infty) = n_i e^{\frac{-q\phi_B}{kT}}. \quad (6.15)$$



(a) n-type substrate



(b) p-type substrate

Figure 6.11: Typical C-V curves of capacitors on different substrates.

Using Equations 6.10, 6.11, 6.12, 6.14 and 6.15, Equation 6.9 can be rewritten as

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_{Si}} = -\frac{q}{\epsilon_{Si}} \left[n_i \left(e^{\frac{-q\phi(x)}{kT}} - e^{\frac{q\phi(x)}{kT}} + e^{\frac{q\phi_B}{kT}} - e^{\frac{-q\phi_B}{kT}} \right) \right]. \quad (6.16)$$

Integrating Equation 6.16 results in the field at the silicon surface

$$F_S = \int_{x=0}^{\infty} \frac{d^2\phi(x)}{dx^2} dx = \int_{x=0}^{\infty} -\frac{\rho(x)}{\epsilon_{Si}} dx. \quad (6.17)$$

Substitution of $\rho(x)$ with $\rho(\phi)$ yields to

$$\int_{x=0}^{\infty} \frac{d\phi(x)}{dx} \cdot \frac{d^2\phi(x)}{dx^2} dx = \int_{\phi=\phi_S}^{\phi_B} -\frac{\rho(\phi)}{\epsilon_{Si}} d\phi. \quad (6.18)$$

Solving the left part of the equation by substitution leads to

$$\int_{x=0}^{\infty} \frac{d\phi(x)}{dx} \cdot \frac{d^2\phi(x)}{dx^2} dx = \int_{F=F(0)}^{F(\infty)} F dF = \frac{1}{2} \cdot F^2 \Big|_{F=F_S}^0 = -\frac{1}{2} \cdot F_S^2. \quad (6.19)$$

Equation 6.18 can now be rewritten as

$$-\frac{1}{2} \cdot F_S^2 = \int_{\phi=\phi_S}^{\phi_B} -\frac{\rho(\phi)}{\epsilon_{Si}} d\phi \quad (6.20)$$

and the field at the silicon surface can be expressed by

$$F_S = \text{sign}(\phi_B - \phi_S) \sqrt{2 \int_{\phi=\phi_S}^{\phi_B} \frac{\rho(\phi)}{\epsilon_{Si}} d\phi} \quad (6.21)$$

$$F_S = \text{sign}(\phi_B - \phi_S) \sqrt{2 \int_{\phi=\phi_S}^{\phi_B} \frac{q}{\epsilon_{Si}} \left[n_i \left(e^{\frac{-q\phi(x)}{kT}} - e^{\frac{q\phi(x)}{kT}} + e^{\frac{q\phi_B}{kT}} - e^{\frac{-q\phi_B}{kT}} \right) \right] d\phi} \quad (6.22)$$

$$F_S = \text{sign}(\phi_B - \phi_S) \sqrt{2 \frac{q}{\epsilon_{Si}} n_i (I_1 - I_2)} \quad (6.23)$$

with

$$I_1 = \frac{kT}{q} \left(-e^{\frac{q\phi_B}{kT}} - e^{\frac{-q\phi_B}{kT}} \right) + \phi_B \left(e^{\frac{q\phi_B}{kT}} - e^{\frac{-q\phi_B}{kT}} \right) \quad (6.24)$$

and

$$I_2 = \frac{kT}{q} \left(-e^{\frac{q\phi_S}{kT}} - e^{\frac{-q\phi_S}{kT}} \right) + \phi_S \left(e^{\frac{q\phi_B}{kT}} - e^{\frac{-q\phi_B}{kT}} \right). \quad (6.25)$$

The charge per unit area at the silicon surface

$$Q_S = \epsilon_{Si} F_S \quad (6.26)$$

and the capacitance thus becomes

$$C_S = -\frac{dQ_S}{d\phi_S} \quad (6.27)$$

$$C_S = \text{sign}(\phi_S - \phi_B) \sqrt{\frac{qn_i}{2\epsilon_{Si}(I_1 - I_2)}} \left[e^{\frac{q\phi_S}{kT}} - e^{-\frac{q\phi_S}{kT}} - e^{\frac{q\phi_B}{kT}} + e^{-\frac{q\phi_B}{kT}} \right]. \quad (6.28)$$

6.1.5.2 High frequency capacitance

In contrast to the relatively easy calculation of the capacitance measured at low frequency, the calculation of the high frequency capacitance is rather complicated. This is because equilibrium in the semiconductor is disrupted at high frequencies (higher than some 10 Hz).

In accumulation the shape of the curves measured at low frequency and at high frequency are the same. Majority carriers can respond to frequencies normally used for measuring capacitance curves. In inversion the capacity measured at high frequency is lower than that measured at low frequency. The density of minority carriers can not change fast enough to respond to the high frequency part of the measurement voltage. The charge is therefore only compensated by increasing or decreasing the depletion layer width. However, the inversion layer produced by the bias voltage works as a shield and the measured capacitance thus becomes constant in inversion.

A high frequency capacitance curve can be calculated using different approaches. First of all it can be approximated using the low frequency capacitance curve in accumulation and depletion, combined with a calculated minimum capacitance. Secondly, the curve can be obtained by the analytical method described by Brews [100]. The following derivation of the capacitance curve is made using this analytical method.

The derivation of the high frequency capacity requires the introduction of a quasi-Fermi level which varies with the alternating component of the measurement voltage. The calculation is done in the same way as for the low frequency capacitance except that the Fermi potential is replaced by the quasi-Fermi potential for minority carriers. For p-type substrate Equation 6.5 becomes

$$\phi_{Fn} = \frac{1}{q} [E_{Fn} - E_i(\infty)]. \quad (6.29)$$

Using Equation 6.29 the electron density can be calculated by

$$n(x) = n_i e^{\frac{q[\phi_{Fn} + \psi(x)]}{kT}}. \quad (6.30)$$

The bulk electron density

$$N_D = n_i e^{\frac{q\phi_{Fn}}{kT}}. \quad (6.31)$$

Equation 6.16 can now be rewritten as

$$\begin{aligned} \frac{d^2\phi(x)}{dx^2} &= -\frac{\rho(x)}{\epsilon_{Si}} \\ &= -\frac{q}{\epsilon_{Si}} \left[n_i \left(e^{\frac{-q(\phi_B + \psi(x))}{kT}} - e^{\frac{q(\phi_{Fn} + \psi(x))}{kT}} + e^{\frac{q\phi_{Fn}}{kT}} - e^{\frac{-q\phi_B}{kT}} \right) \right]. \end{aligned} \quad (6.32)$$

Integrating Equation 6.32 in a similar manner as for the calculation of the low frequency capacitance leads to

$$F_S = \text{sign}(\phi_B - \phi_S) \sqrt{2 \frac{q}{\epsilon_{Si}} n_i (I_1 - I_2)} \quad (6.33)$$

with

$$I_1 = \frac{kT}{q} \left(-e^{\frac{q\phi_{Fn}}{kT}} - e^{\frac{-q\phi_B}{kT}} \right) + \phi_B \left(e^{\frac{q\phi_{Fn}}{kT}} - e^{\frac{-q\phi_B}{kT}} \right) \quad (6.34)$$

and

$$I_2 = \frac{kT}{q} \left(-e^{\frac{q(\phi_{Fn} + \psi_S)}{kT}} - e^{\frac{-q(\phi_{Fn} + \psi_S)}{kT}} \right) + (\phi_B + \psi_S) \left(e^{\frac{q\phi_{Fn}}{kT}} - e^{\frac{-q\phi_B}{kT}} \right). \quad (6.35)$$

Introducing the small-signal quantities defined by

$$\phi_{Fn} = \phi_B + \delta\phi_{Fn} \quad (6.36)$$

and taking the derivative the surface capacitance becomes

$$\begin{aligned} C_S &= \text{sign}(\phi_S - \phi_B) \sqrt{2 \frac{qn_i}{\epsilon_{Si}} (I_1 - I_2)} \\ &\cdot \left\{ e^{\frac{q\phi_S}{kT}} - e^{\frac{-q\phi_S}{kT}} - e^{\frac{q\phi_B}{kT}} + e^{\frac{-q\phi_B}{kT}} - \frac{\delta\phi_{Fn}}{\delta\phi_S} \left[e^{\frac{q\phi_S}{kT}} - \frac{q}{kT} (\phi_B - \phi_S) e^{\frac{q\phi_B}{kT}} \right] \right\} \end{aligned} \quad (6.37)$$

with

$$\frac{\delta\phi_{Fn}}{\delta\phi_S} = \frac{1}{1 + \Delta}, \quad (6.38)$$

as described in [5], where

$$\begin{aligned} \Delta &= \frac{\sqrt{I_1 - I_2}}{\frac{2q}{kT} \left(e^{\frac{-q\phi_S}{kT}} - e^{\frac{-q\phi_B}{kT}} \right)} \\ &\cdot \left[\left(\int_{\frac{q\psi_{S,bias}=0}^{\frac{q\psi_S}{kT}} \frac{e^{-\frac{q\psi_{S,bias}}{kT}} - e^{\frac{q\psi_{S,bias}}{kT}} + 2 \frac{q\psi_{S,bias}}{kT}}{(I_1 - I_2)^{\frac{3}{2}}} d \frac{q\psi_{S,bias}}{kT} \right) - 1 \right] \end{aligned} \quad (6.39)$$

for a n-type substrate and

$$\Delta = \frac{\sqrt{I_1 - I_2}}{\frac{2q}{kT} \left(e^{\frac{q\phi_S}{kT}} - e^{\frac{q\phi_B}{kT}} \right)} \left[\left(\int_{\frac{q\psi_{S,bias}}{kT}=0}^{\frac{q\psi_S}{kT}} \frac{e^{\frac{q\psi_{S,bias}}{kT}} - e^{\frac{-q\psi_{S,bias}}{kT}} - 2\frac{q\psi_{S,bias}}{kT}}{(I_1 - I_2)^{\frac{3}{2}}} d\frac{q\psi_{S,bias}}{kT} \right) - 1 \right] \quad (6.40)$$

for a p-type one.

6.1.5.3 Deep depletion curve

If the bias voltage is swept so fast that no inversion layer is formed, the measured capacitance does not reach a constant value in inversion. Instead, it decreases gradually. The derivation of the capacitance is done by neglecting the minority carriers in the derivation of the low-frequency capacitance. Equation 6.16 thus becomes

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_{Si}} = -\frac{q}{\epsilon_{Si}} \left[n_i \left(-e^{\frac{q\phi(x)}{kT}} + e^{\frac{q\phi_B}{kT}} \right) \right] \quad (6.41)$$

for a capacitor on a n-type substrate and

$$\frac{d^2\phi(x)}{dx^2} = -\frac{\rho(x)}{\epsilon_{Si}} = -\frac{q}{\epsilon_{Si}} \left[n_i \left(e^{\frac{-q\phi(x)}{kT}} - e^{\frac{-q\phi_B}{kT}} \right) \right] \quad (6.42)$$

for one on p-type silicon. Following the procedure for the low-frequency capacitance, Equation 6.23 changes into

$$F_S = \text{sign}(\phi_B - \phi_S) \sqrt{2\frac{q}{\epsilon_{Si}} n_i (I_1 - I_2)} \quad (6.43)$$

with

$$I_{1,n} = -\frac{kT}{q} e^{\frac{q\phi_B}{kT}} + \phi_B e^{\frac{q\phi_B}{kT}} \quad (6.44)$$

and

$$I_{2,n} = -\frac{kT}{q} e^{\frac{q\phi_S}{kT}} - \phi_S e^{\frac{q\phi_B}{kT}} \quad (6.45)$$

for a n-type substrate and

$$F_S = \text{sign}(\phi_B - \phi_S) \sqrt{2\frac{q}{\epsilon_{Si}} n_i (I_1 - I_2)} \quad (6.46)$$

with

$$I_{1,p} = -\frac{kT}{q} e^{\frac{-q\phi_B}{kT}} - \phi_B e^{\frac{-q\phi_B}{kT}} \quad (6.47)$$

and

$$I_{2,p} = -\frac{kT}{q} e^{\frac{-q\phi_S}{kT}} - \phi_S e^{\frac{-q\phi_B}{kT}} \quad (6.48)$$

for a p-type substrate. Finally, the surface capacitance for a capacitor on a n-type substrate becomes

$$C_S = \text{sign}(\phi_S - \phi_B) \sqrt{\frac{qn_i}{2\epsilon_{Si}(I_{1,n} - I_{2,n})}} \left[e^{\frac{q\phi_S}{kT}} - e^{\frac{q\phi_B}{kT}} \right] \quad (6.49)$$

and

$$C_S = \text{sign}(\phi_S - \phi_B) \sqrt{\frac{qn_i}{2\epsilon_{Si}(I_{1,p} - I_{2,p})}} \left[-e^{\frac{-q\phi_S}{kT}} + e^{\frac{-q\phi_B}{kT}} \right] \quad (6.50)$$

on a p-type substrate.

6.1.6 Gate voltage

The gate voltage can be expressed by

$$V_G = V_{FB} + V_{Ox} + \psi_S. \quad (6.51)$$

For the ideal MOS capacitor

$$V_{FB} = 0 \quad (6.52)$$

which results in

$$V_G = -\frac{Q_S}{C_{Ox}} + (\phi_S - \phi_B). \quad (6.53)$$

If a workfunction difference and oxide charges are present (real MOS capacitor),

$$V_{FB} = W_{MS} - \frac{Q_O}{C_{Ox}}, \quad (6.54)$$

where W_{MS} is the workfunction difference and Q_O is the oxide charge consisting of the oxide fixed charge O_f , oxide trapped charge O_{ot} and mobile ionic charge O_m .

6.1.7 Impact of different factors on C-V curves

The shape of a C-V curve can be affected by several factors, some of which are depicted in Figure 6.12 for a n-type substrate.

Oxide charge. Oxide charge causes a shift of the C-V curve along the x-axis which can easily be concluded from Equation 6.51 and Equation 6.54.

Interface traps. Interface traps introduce a charge which depends on the gate voltage and therefore result in a stretch-out of the capacitance curve.

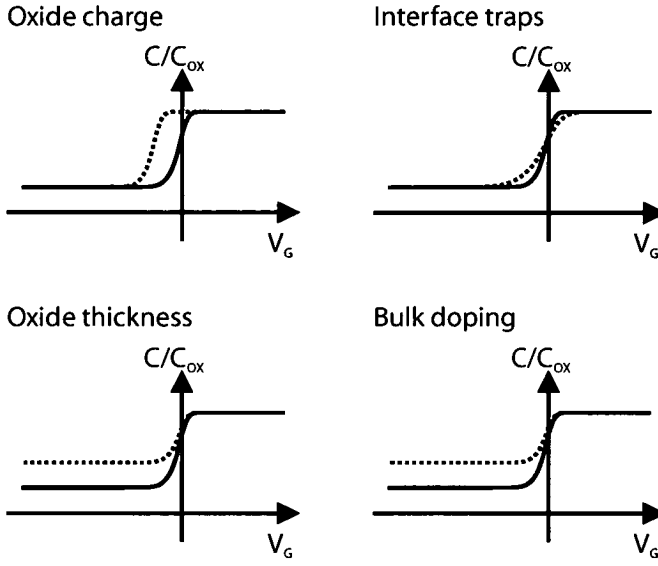


Figure 6.12: Influence of different factors on the C-V curve of a capacitor on a n-type substrate.

Oxide thickness. The oxide thickness changes the capacitance C_{Ox} . If, as it is usually done, the total capacitance is plotted as C/C_{Ox} , the extend of the curve on the y-axis increases with decreasing oxide thickness. This becomes obvious if Equation 6.1 is rewritten as

$$\frac{C}{C_{Ox}} = \frac{1}{1 + \frac{C_{Ox}}{C_S}} = \frac{1}{1 + \frac{\epsilon_{Ox}}{t_{Ox} C_S}}. \quad (6.55)$$

Bulk doping. The bulk doping affects the capacitance C_S at the silicon surface and thus changes the second addend of the denominator in 6.55. An increasing doping density of the substrate decreases the stretch of the curve along the y-axis.

6.2 Materials and methods

6.2.1 Test structures

Capacitive test structures produced from an organometallic material according to Table 4.1 and Table 4.2 were used for the measurements. The manufacturing process was the one described in Chapter 4 if nothing is explicitly mentioned. The capacitance curves shown are typical measurements from a single device due to the low number of samples available from some films, especially the ones heat treated in Dundee.

6.2.2 Measurement setup

The C-V measurements were performed at capacitors on both UDEA V0 and UDEA V1 using a HP4280A 1 MHz C Meter/C-V Plotter. The wafer was held on a vacuum chuck and the measurement connections were made using manually controlled probes with tungsten tips. The wafer chuck was situated in a grounded box which was built so that light could not reach the sample.

As described earlier, the creation of minority carriers in inversion is a slow process. The voltage was therefore held for a certain time before starting the sweep from inversion to accumulation. This hold time was usually five minutes of which 30 seconds were with the microscope light switched on. The light helps creating minority carriers and therefore reduces the hold time necessary. During the measurement, the voltage was swept over a range of 20 V at a rate of 0.02 V/s.

If a guard ring was present around the capacitor, it was connected to the measurement ground.

6.2.3 Extraction of MOS properties from C-V measurements

The shape of the high frequency curve contains information about the structure of the MOS capacitor. This chapter gives details about the extraction of the properties, which was done using a newly written ICCAP program based on previous work by Bienek [101].

6.2.3.1 Series resistance correction and circuit transformation

The measurement device assumes a circuit with a capacitance parallel to a conductance when performing measurements. However, in the case of C-V measurements, it is better to obtain values for a series circuit, with a resistance in series to a capacitance. Furthermore, the values measured need to be corrected for the series resistance R_S caused by the leads and probes. This can be calculated from the values $C_{Ox,m}$ and $G_{Ox,m}$ measured in accumulation using

$$R_S = \frac{G_{Ox,m}}{G_{Ox,m}^2 + \omega^2 C_{Ox,m}^2}. \quad (6.56)$$

The series resistance is then employed to correct the conductance and capacitance values measured by applying the formulas

$$C = \frac{(G_m^2 + \omega^2 C_m^2) C_m}{[G_m - (G_m^2 + \omega^2 C_m^2) R_S]^2 + \omega^2 C_m^2} \quad (6.57)$$

and

$$G = \frac{(G_m^2 + \omega^2 C_m^2) [G_m - (G_m^2 + \omega^2 C_m^2) R_S]}{[G_m - (G_m^2 + \omega^2 C_m^2) R_S]^2 + \omega^2 C_m^2}. \quad (6.58)$$

All values for C and G used later in this chapter are series resistance corrected and represent components of a series circuit.

6.2.3.2 Oxide capacitance and oxide thickness

$$C_{Ox} = C_{acc}. \quad (6.59)$$

where C_{acc} is the maximum measured capacitance in accumulation. The oxide capacitance C_{Ox} can then be calculated using the equation

$$t_{Ox} = \frac{\epsilon_{Ox}}{C_{Ox}}. \quad (6.60)$$

6.2.3.3 Maximum depletion layer width

The maximum depletion layer width is reached when

$$w_{max.} = w(C_{S,min.}) \quad (6.61)$$

where $C_{S,min.}$ is the minimum depletion layer capacitance. The total capacitance C and the depletion layer capacitance C_S are related through the equation

$$\frac{1}{C} = \frac{1}{C_{Ox}} + \frac{1}{C_S}. \quad (6.62)$$

Solving Equation 6.62 for C_S and using the fact that C_S is at its minimum when the minimum of the total capacitance is reached leads to

$$C_{S,min.} = \frac{1}{\frac{1}{C_{min.}} - \frac{1}{C_{Ox}}}. \quad (6.63)$$

C_S and w are linked through

$$C_S = \frac{\epsilon_{Si}}{w}. \quad (6.64)$$

and

$$w_{max.} = \frac{\epsilon_{Si}}{C_{S,min.}} \quad (6.65)$$

where $C_{S,min.}$ is the minimum depletion layer capacitance calculated by Equation 6.63 using C_{Ox} and $C_{min.}$ measured.

6.2.3.4 Doping density

Strong inversion is reached when

$$\psi_S = 2\phi_B. \quad (6.66)$$

To calculate N_D and N_A , respectively, the depletion approximation is made which says that $p = n = 0$ in the depletion region. The depletion approximation and Equation 6.10 lead to

$$\rho = q (N_D - N_A) \quad (6.67)$$

and

$$\frac{d^2\phi}{dx^2} = -\frac{q (N_D - N_A)}{\epsilon_{Si}}. \quad (6.68)$$

Integration of the Poisson equation results in

$$F = \frac{d\phi}{dx} = \sqrt{\frac{2q}{\epsilon_{Si}}} [\psi_s (N_D - N_A)]. \quad (6.69)$$

The field F can also be expressed in terms of the depletion layer width by the equation

$$F = \frac{Q}{\epsilon_{Si}} = \frac{w\rho}{\epsilon_{Si}} = \frac{wq (N_D - N_A)}{\epsilon_{Si}}. \quad (6.70)$$

Combining Equation 6.69 and 6.70 gives

$$\sqrt{\frac{2q}{\epsilon_{Si}}} [\psi_s (N_D - N_A)] = \frac{wq (N_D - N_A)}{\epsilon_{Si}}. \quad (6.71)$$

Solving the equation above results in

$$w = \sqrt{\frac{2\psi_s \epsilon_{Si}}{q (N_D - N_A)}}. \quad (6.72)$$

In strong inversion $w = w(\psi = 2\phi_B)$

$$w(\psi = 2\phi_B) = \sqrt{\frac{4\phi_B \epsilon_{Si}}{q (N_D - N_A)}} = \sqrt{\frac{4kT \ln\left(\frac{N_D}{n_i}\right) \epsilon_{Si}}{q^2 N_D}} \quad (6.73)$$

for n-type silicon and

$$w(\psi = 2\phi_B) = \sqrt{\frac{4kT \ln\left(\frac{N_A}{n_i}\right) \epsilon_{Si}}{q^2 N_A}} \quad (6.74)$$

for p-type silicon. Having Equation 6.73 and Equation 6.74, the total minimum capacitance can be expressed by the equation

$$C_{min.} = \frac{1}{\frac{1}{C_{Ox}} + \frac{1}{C_{S,min.}}} \approx \frac{1}{\frac{1}{C_{Ox}} + \frac{w(\psi=2\phi_B)}{\epsilon_{Si}}}. \quad (6.75)$$

N_D and N_A can now be found by iteration using the equation above and either 6.73 or 6.74, depending on the substrate type.

6.2.3.5 Bulk potential

The bulk potential

$$\phi_B = \frac{kT}{q} \ln \left(\frac{N_D}{n_i} \right) \quad (6.76)$$

for n-type silicon and

$$\phi_B = -\frac{kT}{q} \ln \left(\frac{N_A}{n_i} \right) \quad (6.77)$$

for p-type silicon.

6.2.3.6 Debye length

The Debye length is defined as

$$\lambda_n = \sqrt{\frac{\epsilon_{Si} kT}{q^2 N_D}} \quad (6.78)$$

for an n-type substrate and

$$\lambda_p = \sqrt{\frac{\epsilon_{Si} kT}{q^2 N_A}} \quad (6.79)$$

for a p-type substrate.

6.2.3.7 Flatband capacitance and flatband voltage

The flatband condition is reached when

$$\psi_S = 0 \quad (6.80)$$

which is equal to

$$C_{FB} = C(\psi_S = 0). \quad (6.81)$$

If the condition above is applied to Equation 6.28, the result is undefined (zero divided by zero). In order to find a solution the equation has to be reorganised. For n-type silicon the terms with a negative exponent can be neglected at flatbands. Equation 6.28 then becomes

$$C_S = \text{sign}(\phi_S - \phi_B) \sqrt{\frac{qn_i\epsilon_{Si}}{2(I_1 - I_2)}} \left[e^{\frac{q\phi_S}{kT}} - e^{\frac{q\phi_B}{kT}} \right] \quad (6.82)$$

where

$$I_1 = -\frac{kT}{q} e^{\frac{q\phi_B}{kT}} + \phi_B e^{\frac{q\phi_B}{kT}} \quad (6.83)$$

and

$$I_2 = -\frac{kT}{q} e^{\frac{q\phi_S}{kT}} + \phi_S e^{\frac{q\phi_B}{kT}}. \quad (6.84)$$

This leads to

$$C_S = \text{sign}(\phi_S - \phi_B) \sqrt{\frac{qn_i\epsilon_{Si}}{2e^{\frac{q\phi_B}{kT}} \left(-\frac{kT}{q} + \phi_B + \frac{kT}{q} e^{\frac{q(\phi_S - \phi_B)}{kT}} - \phi_S \right)}} \left[e^{\frac{q(\phi_S - \phi_B)}{kT}} - 1 \right] e^{\frac{q\phi_B}{kT}}. \quad (6.85)$$

Expanding

$$e^{\frac{q(\phi_S - \phi_B)}{kT}} \quad (6.86)$$

around zero results in

$$e^{\frac{q(\phi_S - \phi_B)}{kT}} = 1 + \frac{q(\phi_S - \phi_B)}{kT} + \frac{1}{2} \left[\frac{q(\phi_S - \phi_B)}{kT} \right]^2 + \frac{1}{6} [\dots]^3 + \dots \quad (6.87)$$

Retaining the first three terms we get

$$C_S = \sqrt{\frac{qn_i\epsilon_{Si}}{2e^{\frac{q\phi_B}{kT}} \left\{ \frac{kT}{q} \frac{1}{2} \left[\frac{q(\phi_S - \phi_B)}{kT} \right]^2 \right\}}} \cdot \left\{ \frac{q(\phi_S - \phi_B)}{kT} + \frac{1}{2} \left[\frac{q(\phi_S - \phi_B)}{kT} \right]^2 \right\} e^{\frac{q\phi_B}{kT}}. \quad (6.88)$$

Simplifying 6.88 leads to

$$C_S = \sqrt{\frac{q^2 n_i \epsilon_{Si}}{e^{\frac{q\phi_B}{kT}} kT}} \left\{ 1 + \frac{1}{2} \frac{q(\phi_S - \phi_B)}{kT} \right\} e^{\frac{q\phi_B}{kT}}. \quad (6.89)$$

At flatbands $\phi_S - \phi_B = 0$ and 6.89 can be written as

$$C_{FB} = C_S = \sqrt{\frac{q^2 n_i \epsilon_{Si}}{e^{\frac{q\phi_B}{kT}} kT}} e^{\frac{q\phi_B}{kT}}. \quad (6.90)$$

Finally we substitute the exponential term with N_D/n_i and get

$$C_{FB} = \sqrt{\frac{q^2 n_i \epsilon_{Si}}{\frac{N_D}{n_i} kT}} \frac{N_D}{n_i} = \sqrt{\frac{\epsilon_{Si} q^2 N_D^2}{kT}}. \quad (6.91)$$

Similarly, for p-type the derivation of the flatband capacitance results in

$$C_{FB} = \sqrt{\frac{\epsilon_{Si} q^2 N_A^2}{kT}}. \quad (6.92)$$

V_{FB} can be extracted by finding the voltage V_G belonging to C_{FB} .

6.2.3.8 Maximum depletion layer charge

When the depletion layer width reaches its maximum the depletion layer charge becomes

$$Q_D = \frac{q N_D \epsilon_{Si}}{C_{S,min.}} \quad (6.93)$$

for n-type material and

$$Q_D = \frac{-q N_A \epsilon_{Si}}{C_{S,min.}} \quad (6.94)$$

for p-type material.

6.2.3.9 Threshold voltage

The threshold voltage is the gate voltage at the inset of strong inversion when the minority carrier density at the silicon surface equals the majority carrier density in the bulk. As described earlier in this chapter the band bending equals twice the bulk potential in this condition. Using Q_D calculated above and the value for the band bending at the inset of strong inversion equation 6.51 becomes

$$V_{TH} = V_G (\psi_S = 2\phi_B) = V_{FB} - 2\phi_B - \frac{Q_D}{C_{OX}}. \quad (6.95)$$

6.2.3.10 Oxide charge

All types of charge except mobile ionic charge are located at or close to the silicon/silicon dioxide interface. Mobile ionic charge often enters the MOS structure at the metal/silicon dioxide interface where it does not cause a voltage shift. Neglecting any mobile ionic charge which is not situated at the metal/silicon dioxide interface and assuming that all other charges are situated at the silicon/silicon dioxide interface, equation 6.51 can be employed to evaluate the sum of all oxide charges using

$$Q_O = C_{OX} (W_{MS} - V_{FB}). \quad (6.96)$$

6.3 Results and discussion

The first C-V curves were obtained from measurements on capacitors made of film a and are shown in Figure 6.13, together with the result from an aluminium capacitor on a substrate fabricated at the same time as the one for the platinum capacitor.

Typical C-V curves obtained from measurement on UDEA V0 (made of film b) are shown in Figure 6.14. The figure shows both a curve resulting from a measurement on a platinum and an aluminium capacitor. For comparison a calculated ideal curve is also shown.

From the shift of the C-V curves obtained after six hours annealing time (last heat treatment step) and the known workfunction of 4.1 V of aluminium [96], the workfunction of the platinum film was calculated to be 4.8 V which is close to the value of 4.75 V found in the literature [102]. Both, the shape of the C-V curves measured and the workfunction obtained suggest that the organometallic process can potentially be used to produce transistor gates.

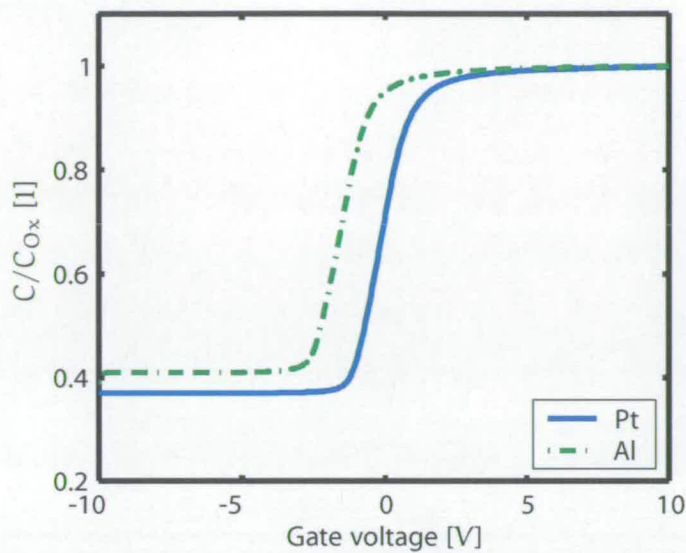
The influence of the reduction time (third stage of the heat treatment involved in the organometallic process) on the workfunction of the deposited platinum films was studied and Figure 6.15 shows the results. The graph shows that the workfunction asymptotically approaches the known value for platinum with increasing annealing time.

The curve obtained from capacitors made of film c and shown in Figure 6.16 agrees very well with the one associated with film a.

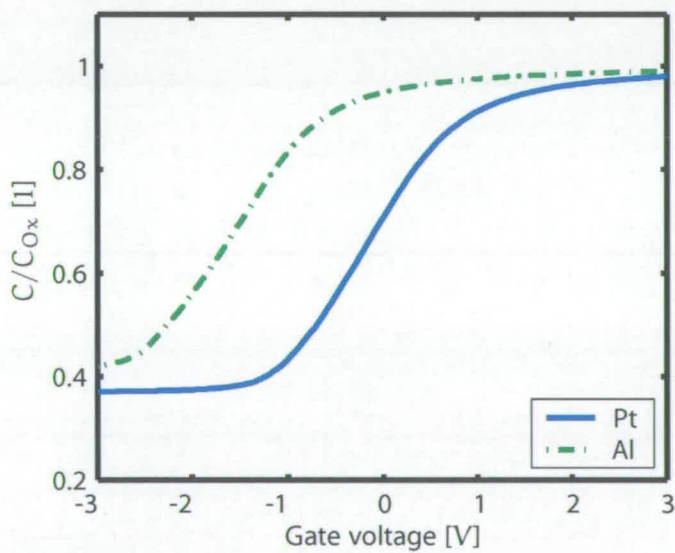
Capacitance measurements were also performed on UDEA V1 so as to be able to correctly interpret any issues concerning the MOS transistors described in Chapter 8. The outcome of a typical measurement is shown in Figure 6.17, with the graphs showing curves from a platinum capacitor, an aluminium capacitor and a simulation.

The capacitance curves from UDEA V1 show the platinum capacitance curve which is stretched out compared with the aluminium capacitor and the results from measurements on UDEA V0. The graph for the aluminium capacitor on the other hand is in good agreement with previous measurements on UDEA V0 and the simulated curve. According to Figure 6.12, a stretch-out as observed in case of the platinum capacitance curve is likely to be caused by interface traps at the silicon/silicon dioxide interface.

The results reported above show discrepancies in the results from measurements on test structures produced from of a one-layer and a multi-layer design. While the C-V curves obtained on capacitors on UDEA V0 forecast a successful use of the platinum films for transistor gates, the measurements on UDEA V1 suggest the presence of interface traps. Evidence for these could only be found on platinum capacitors, which makes it likely that their origin is associated with the organometallic process. Further investigations into the cause for the charges will be necessary to make a clear statement about the possible application of the organometallic process for the creation of transistor gates.

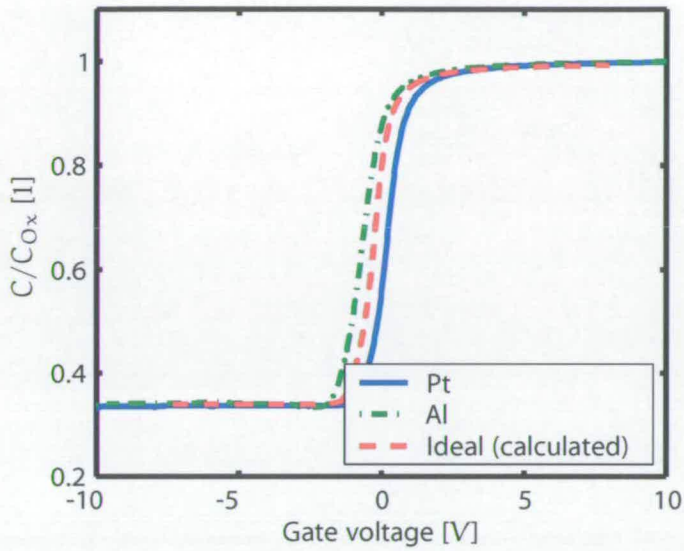


(a) Plot of the C-V curves over the whole measurement range.

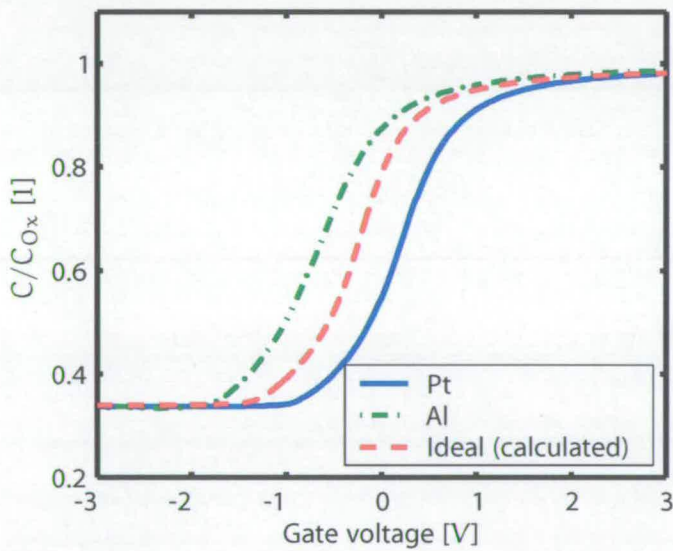


(b) Expanded middle portion of curves shown in Figure 6.13(a).

Figure 6.13: Typical C-V curves obtained at 1 MHz of both a Pt (film a, deposited using the organometallic process) and an Al (deposited by sputtering) capacitor on the n-type substrate of UDEA V0.



(a) Plot of the C-V curves over the whole measurement range.



(b) Expanded middle portion of curves shown in Figure 6.14(a).

Figure 6.14: Typical C-V curves obtained at 1 MHz of both a Pt (film b, deposited using the organometallic process) and an Al (deposited by sputtering) capacitor on the n-type substrate of UDEA V0. A calculated ideal curve is also shown for comparison.

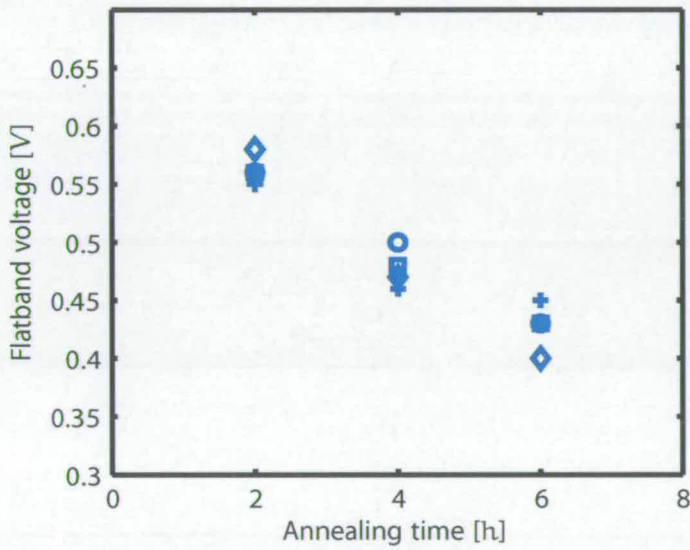
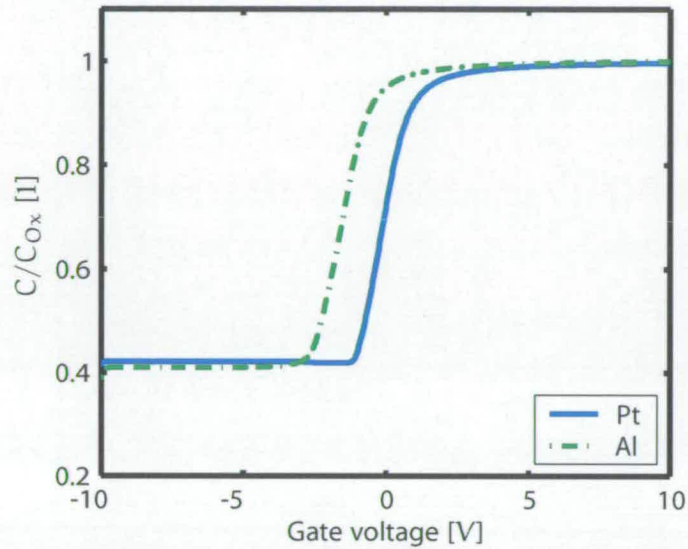
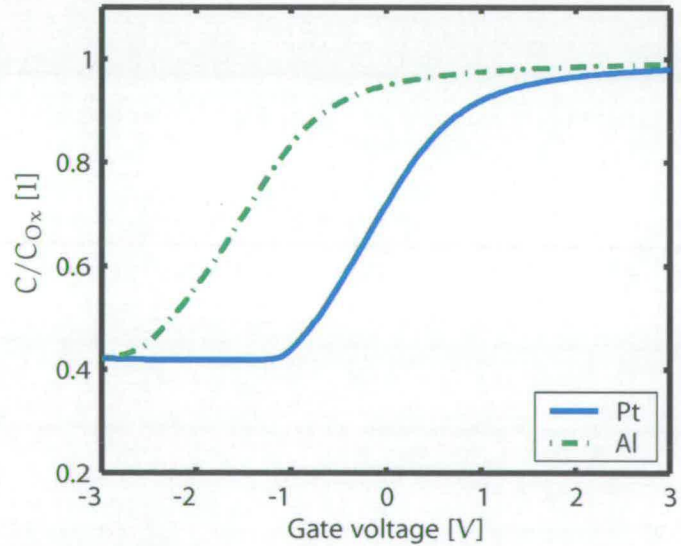


Figure 6.15: Workfunction versus annealing time. The data was obtained from measurements at different locations on a wafer.

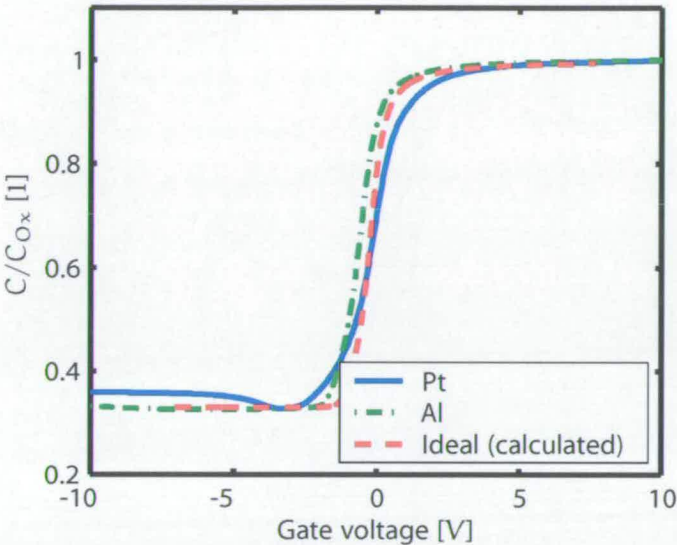


(a) Plot of the C-V curves over the whole measurement range.

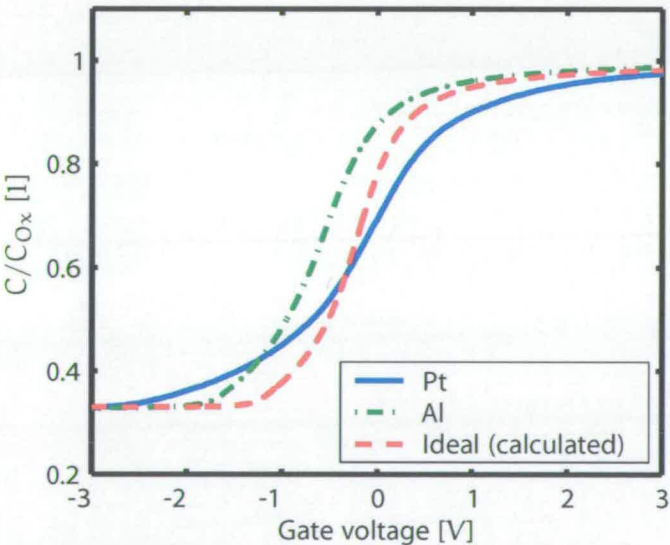


(b) Expanded middle portion of curves shown in Figure 6.16(a).

Figure 6.16: Typical C-V curves obtained at 1 MHz of both a Pt (film c, deposited using the organometallic process) and an Al (deposited by sputtering) capacitor on the n-type substrate of UDEA V0.



(a) Plot of the C-V curves over the whole measurement range.



(b) Expanded middle portion of curves shown in Figure 6.14(a).

Figure 6.17: Typical C-V curves obtained at 1 MHz of both a Pt (film e, deposited using the organometallic process) and an Al (deposited by sputtering) capacitor on the n-type substrate of UDEA V1. A calculated ideal curve is also shown for comparison.

Physical characterisation

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THERE are several requirements to be met by a material for its use in a MOS metallisation process. One of the most important properties is the resistivity which directly influences the speed of an integrated circuit. Impurities in the metal can significantly increase the resistivity of a metal film and thus strongly affect the attractiveness of a process for its use in IC processes. Besides their impact on the resistivity, foreign substances can also contaminate other materials involved in the process and by this means alter the characteristics of semiconductor devices.

It is therefore important to identify any contaminants in the platinum films dealt with in this work so as to evaluate the suitability for their use in semiconductor manufacturing.

7.1 Basics

7.1.1 Auger electron spectroscopy (AES)

For Auger electron spectroscopy (AES), electrons with an energy ranging from 1 – 10 keV are bombarded at a sample. A primary electron from this beam ejects an electron from the core shell of a target atom. The remaining space is then filled with a secondary electron from an outer shell. The energy difference of this electron is compensated by emitting a third electron, the Auger electron. The energy of the Auger electron is unique to each element's atom and by determining the spectrum of the emitted electrons it is possible to identify peaks representing all the elements except hydrogen and helium [103]. Because the Auger process is a three electron process and hydrogen and helium both possess less than three electrons, it is

obvious why these elements can not be detected. Due to scattering, AES is a surface-sensitive technique. Typical analysis depths range from 0.5 nm to 5 nm but it is possible to obtain depth information by removing thin layers of the investigated material by sputtering [68]. A disadvantage of AES is the charging of insulator surfaces caused by the electron bombardment.

7.1.2 X-ray photoelectron spectroscopy (XPS)

Photons from X-rays interact with electrons in the shells of the atoms. If the energy of the X-rays is higher than the binding energy, electrons are emitted. If an atom is part of a molecule, the binding energy of the electrons in the valence shell (and to a smaller extent in the inner shells) is different from the one of a lone atom. Although the shifts observed due to bonding are usually larger in AES spectra, their evaluation is more developed for XPS and often more accurate because of the destruction caused by the electron bombardment in AES analysis. The analysis depth is similar to the one of AES and lies between 0.5 and 5 nm. Depth information can be acquired in a manner equal to the one explained for AES.

7.2 Materials and methods

7.2.1 Sample preparation

For the characterisation of the films by AES and XPS a platinum layer has been deposited on barium borosilicate glass (Corning 7059) using the organometallic $\text{cis} - (\text{C}_3\text{F}_7)_2\text{Pt}(\text{II}) - \text{C}_8\text{H}_{12}$ and tools at the University of Dundee. The deposition process was conducted as follows. Approximately 1.2 μm organometallic material is thermally evaporated onto the glass substrate and flood exposed using a 260 nm lithography tool. A two stage heat treatment completes the manufacturing of the sample. The first step of the heat treatment usually employed is not necessary because no unexposed organometallic compound is present which needs to be removed. During stage one the substrate is put into a furnace at a temperature of 250 °C for one hour in air and for stage two at a temperature of 350 °C for four hours in 5% hydrogen in nitrogen.

7.2.2 Measurement setup

Equipment available at the University of Dundee and operated by university staff was employed for the physical characterisation of the deposited platinum films. The spectra were obtained using a Vacuum Generator HB100 scanning electron microscope with a CLAM100 Spectrometer operating in constant analyser energy mode at a pass energy of 20 eV. For photoelectron excitation a $\text{MgK}\alpha$ X-ray source $h\nu = 1253.6$ eV was used. The electron beam current for AES was 38 nA at an energy of 5 keV.

7.3 Results and discussion

The composition of the films was studied by AES and XPS and a homogeneous model was assumed.

7.3.1 AES

Auger spectra were obtained from the samples before (Figure 7.1) and after sputtering of the surface (Figure 7.2). The film thickness of the original film was some 35 nm of which a few monolayers were removed during the sputtering process. The AES data was smoothed and differentiated using the least-square method proposed by Savitzky and Golay [104, 105]. It can be seen that the carbon peak at 272 eV measured before sputtering is significantly higher than the one seen in the spectra obtained afterwards. The positions of the peaks are in good accordance with published data [106]. Using sensitivity factors derived from standard Auger spectra the relative quantities of Pt and C existing in the film were calculated. It was found that the ratio Pt:C was 0.46 before the sputtering process and increased to 1.52 afterwards. The oxygen peak seen in the spectra was not included in the analysis because of its small peak height and the relative large sensitivity factor of oxygen. However, quantification using the peak-to-peak height of the signal in the differential spectrum introduces large errors and the ratios stated above should therefore be seen as rough estimates only [107].

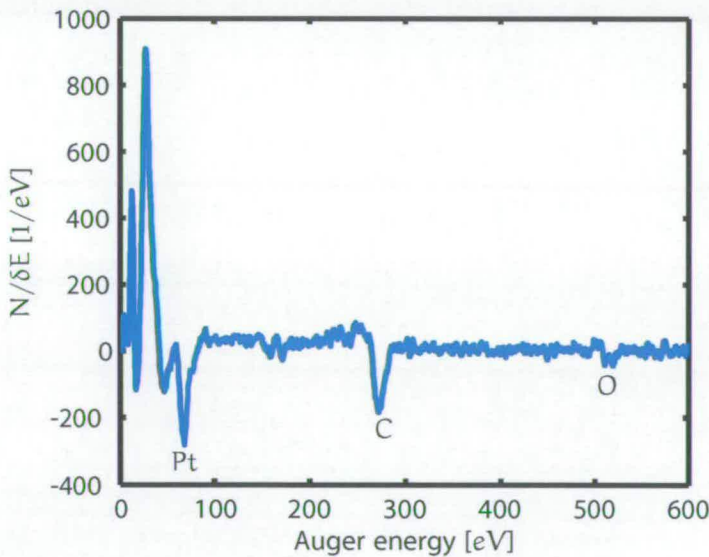


Figure 7.1: AES spectra of the platinum film before sputtering.

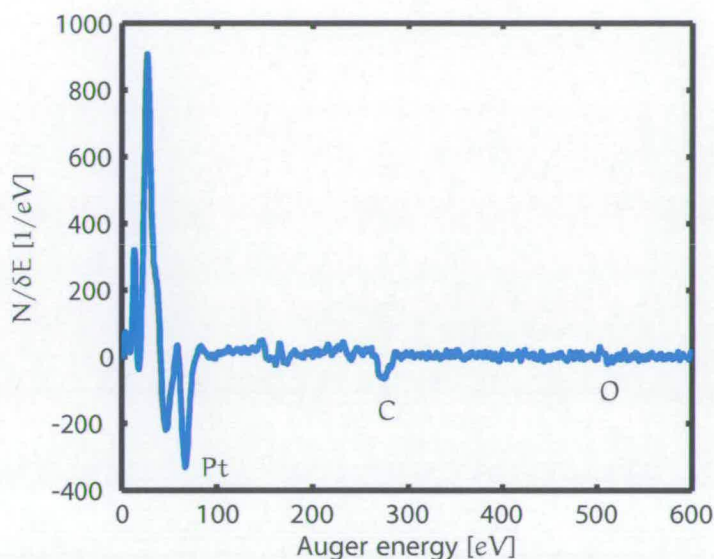


Figure 7.2: AES spectra of the platinum film after sputtering.

7.3.2 XPS

An XPS spectrum (Figure 7.3) was recorded after the sputtering of the sample. The data was calibrated using the C 1s peak at 284.6 eV and the background removed using a linear approach. Peaks were fitted into the curve using the Marquardt algorithm [108]. The positions of the platinum peaks are given in Table 7.1 [109] with the identifier (e.g. $4f_{5/2}$) describing the position of the according electron in the shell of the atom. A reasonable fit in the region around the Pt 4f peaks (Figure 7.4) could be obtained with Doniach-Sunjic peaks [110] with α fixed to 0.24. A Doniach-Sunjic peak shape was chosen because of the metallic nature of platinum which results in an unsymmetric peak shape. The value of the singularity index α is in good agreement with values used by other authors [111]. Because of their interference with the peaks of interest, the $K\alpha_3$ and $K\alpha_4$ satellites listed in Table 7.2 [109] were also taken into account during the fitting process.

The position of the $4f_{7/2}$ peak was determined to be at 71.0 eV which corresponds well with values reported in the literature. The carbon 1s peak used for the calibration and quantification was fitted using a symmetrical Lorentzian-Gaussian peak shape.

Quantification of the components of the film was done by comparison of the areas of the principal peaks which were the Pt $4f_{7/2}$ and the C 1s peak. Using sensitivity factors found in the literature [103] it was estimated that platinum and carbon are present in the film with an atomic ratio Pt:C of about 1.95:1 (66% Pt and 34% C), corresponding to an atomic weight ratio Pt:C of approximately 32:1 (97% Pt and 3% C).

Photoelectron line	Position
4f _{7/2}	73 eV
4f _{5/2}	76 eV
4d _{5/2}	316 eV
4d _{3/2}	333 eV
4p _{3/2}	521 eV
4p _{1/2}	610 eV
4s	726 eV

Table 7.1: Position of the photoelectron lines of Pt [103].

X-ray line	Separation from K $\alpha_{1,2}$	Relative intensity (K $\alpha_{1,2}$ = 100%)
K α'	4.5 eV	1.0
K α_3	8.4 eV	9.2
K α_4	10.0 eV	5.1
K α_5	17.3 eV	0.8
K α_6	20.5 eV	0.5
K α_β	48.0 eV	2.0

Table 7.2: Position and intensity of X-ray satellites from Mg targets [103].

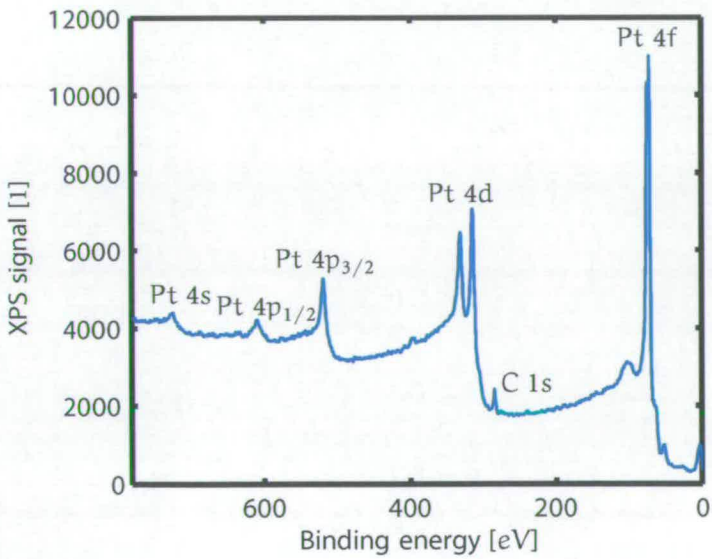


Figure 7.3: XPS spectra of the platinum film after sputtering.

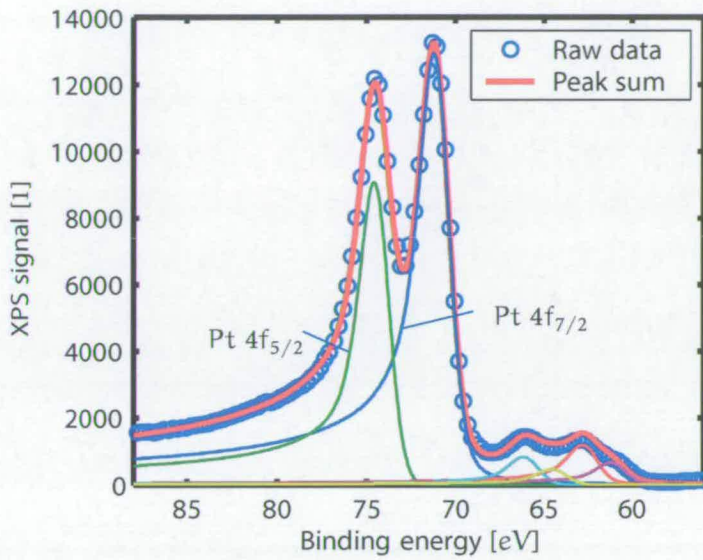


Figure 7.4: Pt4f_{7/2} and Pt4f_{5/2} peaks of the platinum film after sputtering.

7.3.3 Discussion

Both, the AES and the XPS spectra obtained, show that the deposited platinum films are contaminated by carbon. The gross amount of the carbon most likely originates from the organometallic compound. The different intensities of the carbon peaks measured by Auger electron spectroscopy before and after sputtering of the surface suggest that the distribution of the carbon in the film changed during exposure or heat treatment of the sample. The carbon peak at 272 eV does not interfere with major platinum peaks and errors in the detection of carbon are therefore unlikely [112]. Also, because of the the heat treatment involved in the deposition of the platinum films, carbon contamination due to electron beam cracking of volatile carbon compounds can be neglected [112].

The XPS analysis of the film showed that both the platinum and the carbon detected occur in their pure form. Quantification using peak fitting and empirical sensitivity factors indicated that the atomic ratio Pt:C in the analysed film was approximately 1.95:1. Fluorine, which is present in the organometallic compound, could not be detected in the platinum film.

Different procedures for removal of carbon from platinum surfaces were reviewed by Musket et al. [113] some of which could be used to increase the relative platinum content of the films investigated in this thesis.

8

Characterisation of MOS transistors

Contents

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As mentioned in a previous chapter, the MOS transistor is the most important device used in modern integrated circuits due to its low power consumption and simple construction. The results presented earlier indicate that the organometallic process could potentially be used to deposit and pattern the gate material for MOS transistors. In order to verify these findings and to identify any issues associated with the manufacturing process, simple MOS transistors were manufactured and characterised.

8.1 Basics

A MOS transistor is a four-terminal device and is built as depicted in Figure 8.1. Its main parts are the source, drain and back contacts and the MOS capacitor described earlier, which is formed by the gate, the silicon dioxide insulator and the underlying silicon.

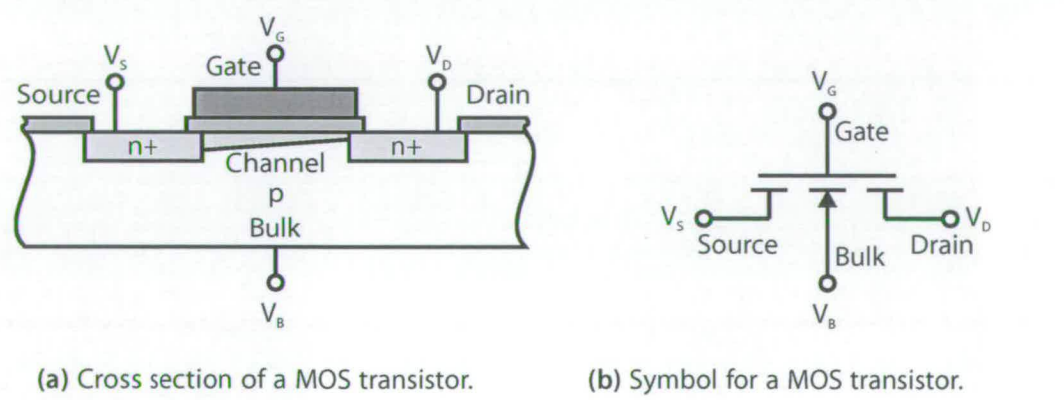


Figure 8.1: MOS transistor.

In order to describe the basic principle of operation, we assume a structure as shown in Figure 8.1(a) and the source contact to be grounded as depicted in Figure 8.2(b). If no gate voltage is applied, a pnp region exists between the source and the drain contact and no current can flow. When a sufficiently high voltage is applied to the gate, an inversion layer is formed which allows a current flow between drain and source. Because the carriers in the inversion layer or channel are holes, this type of MOS transistor is called a p-channel device. If source and drain regions were n-type, the carriers in the channel would be electrons and the transistor would be a n-channel device.

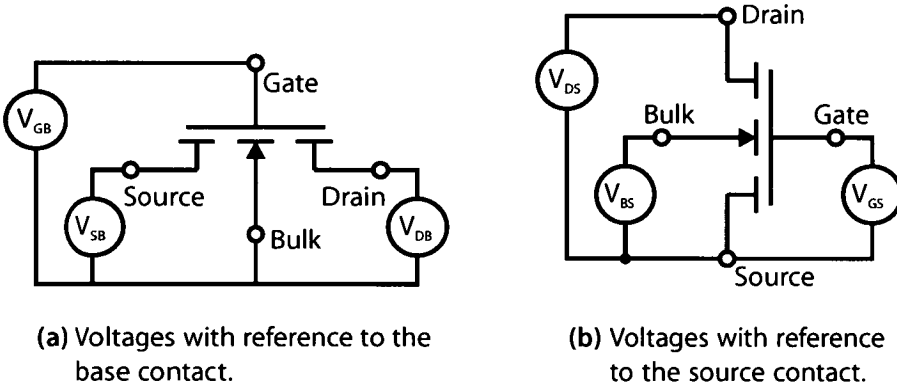


Figure 8.2: Voltages at the MOS transistor.

The explanation of the characteristics of the MOS transistor can be based on the theory for the two-terminal MOS structure derived in Chapter 6. The derivation closely follows the one described in the book by Tsividis [4]. In contrast to the formulas derived for the two-terminal MOS structure, several simplifications have been made. The following derivation assumes a n-type substrate thus resulting in a P-MOS transistor. Also, only the inversion region is considered because this is the region where a MOS transistor is usually operated.

The drain current of the transistor can be expressed by

$$I_D(x) = I_{D,Drift}(x) + I_{D,Diff}(x), \quad (8.1)$$

where

$$I_{D,Drift} = \mu W (-Q_I) \frac{d\phi_S}{dx} \quad (8.2)$$

and

$$I_{D,Diff} = \mu W \frac{kT}{q} \cdot \frac{dQ_I}{dx}. \quad (8.3)$$

The current in the channel, which is equal to the drain current I_D , must be the same over the whole length of it and is therefore a constant value. Thus, substituting Equations 8.3

and 8.2 into Equation 8.1 and integrating it, leads to

$$\int_{x=0}^L I_D dx = \int_{\phi_S=\phi_{S,0}}^{\phi_{S,L}} \mu W (-Q_I) d\phi_S + \int_{Q_I=Q_{I,0}}^{Q_{I,L}} \mu W \frac{kT}{q} dQ_I. \quad (8.4)$$

If we integrate the left part of the above equation and move L to the right-hand side, we get

$$I_D = \frac{W}{L} \int_{\phi_S=\phi_{S,0}}^{\phi_{S,L}} \mu (-Q_I) d\phi_S + \frac{W}{L} \int_{Q_I=Q_{I,0}}^{Q_{I,L}} \mu \frac{kT}{q} dQ_I \quad (8.5)$$

where W and L are the width and length of the transistor, respectively. Assuming μ to be constant we can integrate the current caused by diffusion and Equation 8.5 becomes

$$I_D = \frac{W}{L} \mu \int_{\phi_S=\phi_{S,0}}^{\phi_{S,L}} (-Q_I) d\phi_S + \frac{W}{L} \mu (Q_{I,0} - Q_{I,L}). \quad (8.6)$$

It can be seen that in order to solve this equation, it is necessary to know the inversion charge. The charge at the surface is the sum of the inversion charge and the depletion charge as expressed by

$$Q_S = Q_I + Q_D \quad (8.7)$$

where Q_S is the charge induced in the semiconductor area, Q_I the inversion charge and Q_D the charge of the depletion layer.

If the depletion approximation is made, which states that $n = p = 0$ in the depletion layer, the charge in the depletion layer becomes

$$Q_D = N_D q w = n_i e^{\frac{q\phi_B}{kT}} q w \quad (8.8)$$

where w is the width of the depletion layer. From Equation 8.8 we obtain the charge density in the depletion layer

$$\rho(x) = n_i e^{\frac{q\phi_B}{kT}} q. \quad (8.9)$$

Using Equation 8.9, we then solve the Poisson's equation (Equation 6.9) in the manner described in Chapter 6 and Equation 6.22 becomes

$$F_S = \sqrt{2 \int_{\phi=\phi_S}^{\phi_B} \frac{q}{\epsilon_{Si}} n_i e^{\frac{q\phi_B}{kT}} d\phi}. \quad (8.10)$$

Carrying out the integration and substituting the result into 6.26 leads to

$$Q_D = \sqrt{2\epsilon_{Si} q n_i e^{\frac{q\phi_B}{kT}} (\phi_B - \phi_S)}. \quad (8.11)$$

According to Equation 6.53, the charge Q_S under the oxide as a function of the surface po-

tential ϕ_S is

$$Q_S = -[V_{GB} - (\phi_S - \phi_B)] C_{Ox}. \quad (8.12)$$

Using the equation above and Equation 8.11 in Equation 8.7, we obtain

$$Q_I = -[V_{GB} - (\phi_S - \phi_B)] C_{Ox} - \sqrt{2\epsilon_{Si} q n_i (\phi_B - \phi_S) e^{\frac{q\phi_B}{kT}}}. \quad (8.13)$$

The drift component from Equation 8.6 is

$$I_{D,Drift} = \frac{W}{L} \mu \int_{\phi_S=\phi_{S,0}}^{\phi_{S,L}} (-Q_I) d\phi_S. \quad (8.14)$$

Substituting 8.13 into 8.14 leads to

$$I_{D,Drift} = \frac{W}{L} \mu \int_{\phi_S=\phi_{S,0}}^{\phi_{S,L}} \left\{ [V_{GB} - (\phi_S - \phi_B)] C_{Ox} - \sqrt{2\epsilon_{Si} q n_i (\phi_B - \phi_S) e^{\frac{q\phi_B}{kT}}} \right\} d\phi_S. \quad (8.15)$$

If we integrate 8.15, we get

$$I_{D,Drift} = \frac{W}{L} \mu \left[\left(V_{GB} \phi_S - \frac{\phi_S^2}{2} + \phi_B \phi_S \right) C_{Ox} - \sqrt{\frac{8}{9} \epsilon_{Si} q n_i e^{\frac{q\phi_B}{kT}} (\phi_B - \phi_S)^3} \right] \bigg|_{\phi_S=\phi_{S,0}}^{\phi_{S,L}} \quad (8.16)$$

and carrying out the substitution leads to

$$I_{D,Drift} = \frac{W}{L} \mu \left\{ \left[(\phi_{S,L} - \phi_{S,0}) (V_{GB} + \phi_B) - \frac{(\phi_{S,L} - \phi_{S,0})^2}{2} \right] C_{Ox} - \sqrt{\frac{8}{9} \epsilon_{Si} q n_i e^{\frac{q\phi_B}{kT}}} \left[(\phi_B - \phi_{S,L})^{\frac{3}{2}} - (\phi_B - \phi_{S,0})^{\frac{3}{2}} \right] \right\}. \quad (8.17)$$

The diffusion component from Equation 8.6 is

$$I_{D,Diff.} = \frac{W}{L} \mu (Q_{I,0} - Q_{I,L}). \quad (8.18)$$

Substituting Equation 8.13 into Equation 8.18 leads to

$$I_{D,Diff.} = -\frac{W}{L} \mu \left[-(\phi_{S,L} - \phi_{S,0}) C_{Ox} - \sqrt{2\epsilon_{Si} q n_i e^{\frac{q\phi_B}{kT}}} \left(\sqrt{\phi_B - \phi_{S,L}} - \sqrt{\phi_B - \phi_{S,0}} \right) \right]. \quad (8.19)$$

The equations above still use potentials which are inside the MOS structure. In order to describe the characteristics of a transistor, it is necessary to have expressions for ϕ_S as a function of external voltages.

Due to the contacts to the inversion layer, it is necessary to compensate for the difference caused by the additional voltages. A voltage V_{DB} is needed to restore the minority carrier density at the semiconductor surface close to the drain contact and V_{SB} at the source contact. Equation 6.12 derived for the hole density at the semiconductor surface then becomes

$$p_{S,L} = n_i e^{\frac{-q(\phi_{S,L} - V_{DB})}{kT}} \quad (8.20)$$

at the drain contact and

$$p_{S,0} = n_i e^{\frac{-q(\phi_{S,0} - V_{SB})}{kT}} \quad (8.21)$$

at the source contact. For a p-type substrate, $\phi_S \leq \phi_B$ in inversion and Equation 6.26 can be simplified to

$$Q_S = \sqrt{2\epsilon_{Si} q n_i \left[(\phi_B - \phi_S) e^{\frac{q\phi_B}{kT}} + \frac{kT}{q} e^{\frac{-q\phi_S}{kT}} \right]}. \quad (8.22)$$

If Equation 8.20 and Equation 8.21 are applied, the expression above becomes

$$Q_S = \sqrt{2\epsilon_{Si} q n_i \left[(\phi_B - \phi_S) e^{\frac{q\phi_B}{kT}} + \frac{kT}{q} e^{\frac{-q(\phi_S - V_{CB})}{kT}} \right]} \quad (8.23)$$

where V_{CB} is the voltage between the contact and the bulk which is either V_{DB} or V_{SB} . The majority carriers (first term in the equation) are not influenced because electrons are not attracted to the p+ region at the contact. The equations for $\phi_{S,L}$ and $\phi_{S,0}$ can then be derived by substituting 8.23 into 6.53 which results in

$$V_{GB} = -\frac{1}{C_{Ox}} \sqrt{2\epsilon_{Si} q n_i \left[(\phi_B - \phi_{S,0} + V_{SB}) e^{\frac{q\phi_B}{kT}} + \frac{kT}{q} e^{\frac{-q\phi_{S,0}}{kT}} \right]} + (\phi_{S,0} - \phi_B) \quad (8.24)$$

and

$$V_{GB} = -\frac{1}{C_{Ox}} \sqrt{2\epsilon_{Si} q n_i \left[(\phi_B - \phi_{S,L} + V_{DB}) e^{\frac{q\phi_B}{kT}} + \frac{kT}{q} e^{\frac{-q\phi_{S,L}}{kT}} \right]} + (\phi_{S,L} - \phi_B). \quad (8.25)$$

Using Equations 8.24, 8.25, 8.1, 8.17 and 8.19 derived above, the characteristics of a MOS transistor can be calculated numerically.

8.2 Materials and methods

8.2.1 Test structures

A simple transistor process has been developed and a test chip designed and manufactured as described in Chapter 4. Typical resulting transistors with both platinum and aluminium gate are shown in Figure 8.3(a) and Figure 8.3(b), respectively. Illustrations of the according cross-sections are depicted in Figure 8.4. It can be seen that aluminium was used for interconnects and pads for both transistor types.

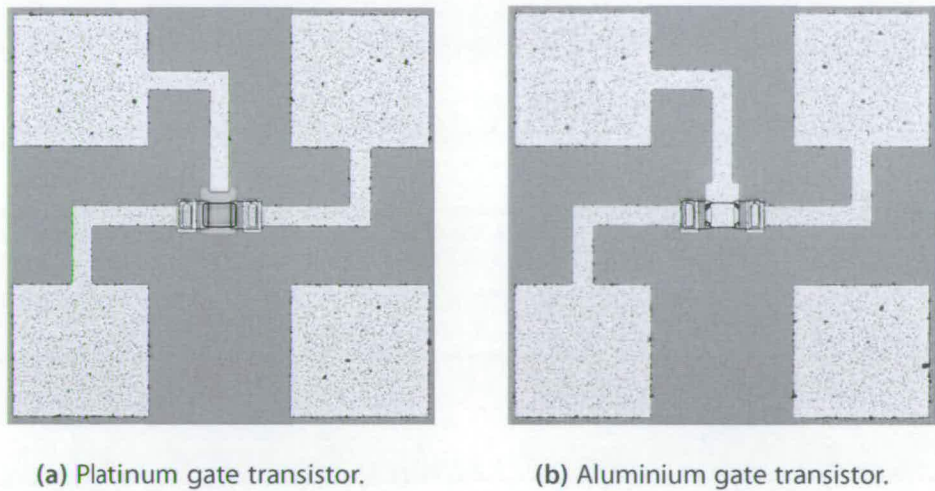


Figure 8.3: Devices with gate length of 20 μm and width of 20 μm .

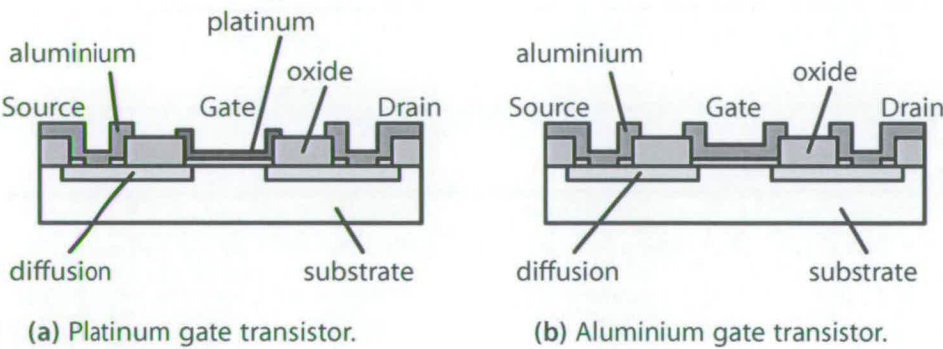


Figure 8.4: Cross sections of the two transistor types.

8.2.2 Measurement setup

For the characterisation, a test system built around a HP4156B Semiconductor Parameter Analyzer was employed. The sample was placed on a chuck in a lightproof box which was grounded. The devices were probed using tungsten tips. The ICCAP software package was used to control the measurement equipment, acquire the data and extract transistor parameters.

8.2.3 MOS transistor parameter extraction

The model used to extract the transistor parameters was obtained by expanding the formulas derived in Chapter 8.1 around $V_{CB} = V_{SB}$ [4]. In saturation, I_D is at its maximum value and can be calculated by setting $dI_D/dV_{DS} = 0$. The model is identical to a Shichman-Hodges model [114] or MOS Model 1 and describes a transistor in its operating regions (Figure 8.5) by the three equations below.

$$I_D = 0 \quad ; \quad V_{GS} < 0 \quad (8.26)$$

$$I_D = \frac{W}{L} \mu C_{Ox} \left[(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad ; \quad V_{DS} < V_{GS} - V_T \quad (8.27)$$

$$I_D = \frac{W}{L} \mu C_{Ox} \frac{(V_{GS} - V_T)^2}{2} \quad ; \quad V_{DS} > V_{GS} - V_T \quad (8.28)$$

The threshold voltage V_T is determined by

$$V_T = V_{T,0} + \gamma + \sqrt{\phi_S - V_B} - \sqrt{\phi_S} \quad (8.29)$$

with $V_{T,0}$ being the threshold voltage at $V_{SB} = 0$ V and

$$\gamma = \frac{\sqrt{2q\epsilon_{Si}N_D}}{C_{Ox}}. \quad (8.30)$$

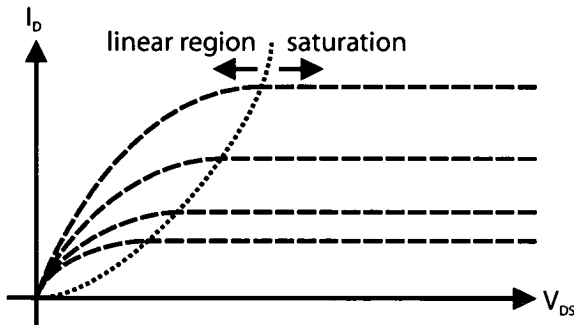


Figure 8.5: Operating regions of the MOS transistor.

The model above is an approximation which does not take the dependence of $-Q_S/C_{Ox}$ on V_{CB} into account. However, the transistors produced have big dimensions, resulting in a large C_{Ox} and the error introduced by this simplification therefore becomes small.

8.3 Results and Discussion

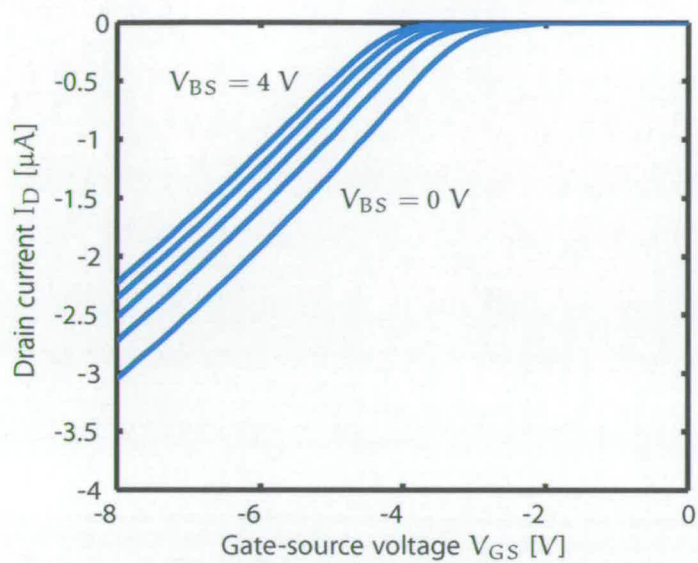
The initial transistor measurements were the output and transfer characteristics. Typical $V_{GS} - I_D$ and $V_{DS} - I_D$ curves of both platinum and aluminium devices are shown in Figure 8.6 and Figure 8.7, respectively. Secondly, parameters such as threshold voltage and oxide capacitance were determined by fitting the simple physical transistor model described in Chapter 8.2.3 to the I_D/V_{DS} data from the measurements. The transistors fitted to the model have large enough dimensions and hence the simple model adequately fits the characteristics [4].

It can be seen that the shapes of saturation and linear region of the two transistor types are similar. However, the region around the threshold voltage reveals that the platinum gate transistor turns on more slowly than its aluminium counterpart.

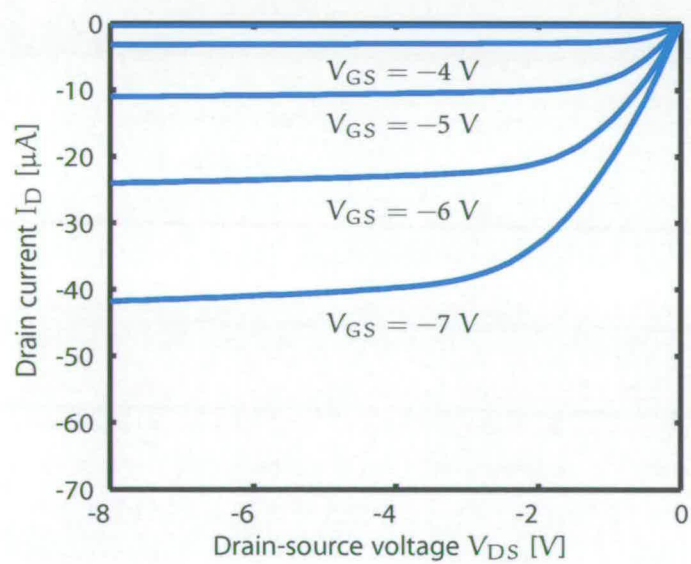
The characteristics shown in Figure 8.8 compare the subthreshold regions of the aluminium and platinum transistors and it can be observed that the slope of the aluminium is much superior to the platinum device. The reasons for this are unclear as the two devices were fabricated on the same wafer. Hence, the gate oxide for both devices was grown at the same time with the platinum device only having an extra heat treatment to pattern and anneal the gate.

The main factors determining the subthreshold slope are gate oxide thickness, channel dopant concentration and interface trap density [115]. C-V measurements on platinum capacitors on the same substrate as the transistors and presented in Chapter 6 showed a stretch-out of the curves which is typical if interface trap charges are present. It is therefore likely that the low subthreshold slope observed for the platinum transistors results from these charges.

The threshold voltage V_{TH} of the platinum and aluminium gate transistor was extracted by fitting the data to the transistor model and determined to be -3.0 V and -2.1 V, respectively. These values indicate that the $V_{GS} - I_D$ curves of the transistor with platinum gate transistor are shifted by 0.9 V to more negative values, which does not agree with expectations drawn from the workfunctions of the two metals reported in Chapter 6. The curves of the platinum gate transistor should be positioned approximately 0.65 V to the right of the curves of the aluminium device. From Figure 8.8, one can see that the platinum gate transistor starts turning on at a gate voltage more positive than the threshold voltage, suggesting that the discrepancy between the measured and expected shift of the threshold voltages is caused by the same effect as the low subthreshold slope.

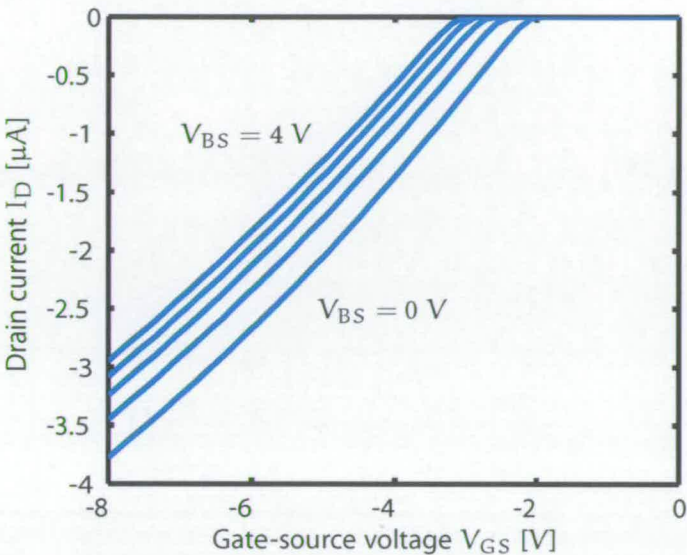


(a) $V_{GS} - I_D$

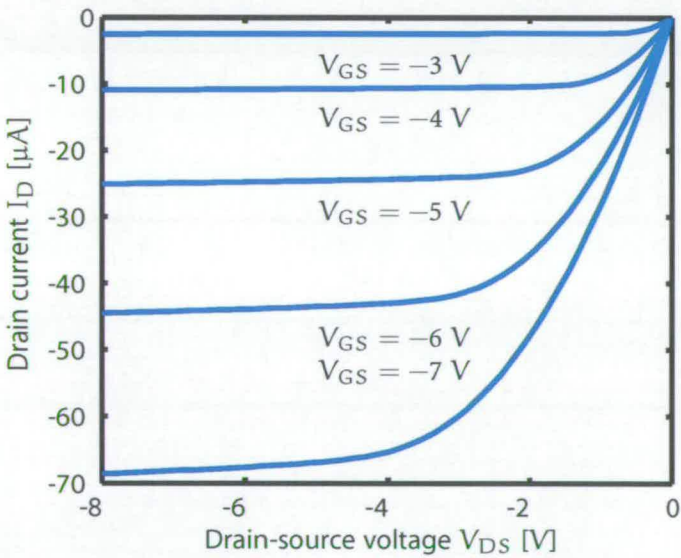


(b) $V_{DS} - I_D$

Figure 8.6: Characteristics of a platinum gate transistor with a gate length of 20 μm and a width of 20 μm .



(a) $V_{GS} - I_D$



(b) $V_{DS} - I_D$

Figure 8.7: Characteristics of an aluminium gate transistor with a gate length of 20 μm and a width of 20 μm .

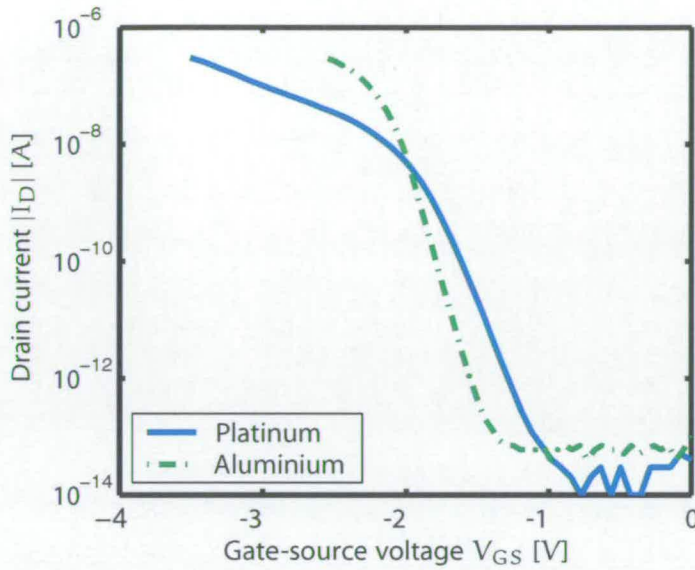


Figure 8.8: Subthreshold characteristic of transistors with a gate length of $20\ \mu\text{m}$ and a width of $20\ \mu\text{m}$.

Transistor characteristics as the ones presented above show the potential of the organometallic process to form transistor gates. However, the low subthreshold slope is an issue which needs to be addressed before the technique can be employed in semiconductor manufacturing. Furthermore, it will be necessary to develop a complete CMOS process to prove that both P-MOS and N-MOS transistors can be fabricated.

Review, discussion and future work

Contents

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9.2	Implications	105
9.3	Further work	108

THIS thesis set out to investigate platinum films deposited by means of an organometallic process and their use in semiconductor manufacturing. This chapter brings together the conclusions from the previous chapters, presents the implications of this research on the use of organometallics in semiconductor processes and provides suggestions for further work.

9.1 Review of experimental findings

Chapter 3 and 4 showed that it is possible to produce test chips incorporating platinum features deposited using processes based on the organometallic materials $(C_3F_7)_2Pt^{II} - C_8H_{12}$ and $(C_3F_7)(CH_3)Pt^{II} - C_8H_{12}$, the latter being a further development of the first compound. It was also demonstrated that a heat treatment similar to the one established at the University of Dundee can be employed to manufacture structures on a wafer scale, which is of great importance in semiconductor manufacturing. Profiles acquired revealed that features resulting from the organometallic process are larger than the corresponding patterns on the mask. This effect limits the minimum feature size achievable and was attributed to diffraction during exposure. The processing of samples also brought to light at an early stage of the project that the material preparation was a challenge and the resources at Dundee were stretched to provide films of repeatable quality with the required optical and electrical characteristics. This obviously had knock on effects in the integration work reported in the thesis and reduced the number of successful process runs and devices characterised.

Chapter 5 reported the resistivity of the platinum films to be between 4.9 and 46 times higher than the bulk resistivity of $1.06 \cdot 10^{-7} \Omega m$, depending on the heat treatment and the type of organometallic material. The resistivity of films deposited from $(C_3F_7)_2Pt^{II} - C_8H_{12}$ was about twice the value of films originating from the second organometallic. Besides, it was found that the cross sections of the films produced do not match a rectangular shape and the usefulness of test structures like the Greek cross for the extraction of resistance data is

therefore questionable. The comparison of features given the heat treatment either in Edinburgh or in Dundee revealed that the cross sections resulting from the conduct in Edinburgh are more uniform. Discrepancies in the results from linewidth measurements acquired using electrical and mechanical methods were also highlighted. Due to the electrical measurement assuming a rectangular profile and being based on a Greek cross test structure, this method is thought to introduce a significant error into the linewidth measured. This conclusion is supported by the analysis of the error introduced by the ball-shaped tip of the profilometer used for the mechanical measurement, which is reported in Appendix C. The calculations showed that, for cases encountered in this work, the tip does not substantially influence the outcome.

Chapter 6 found that the C-V curves obtained from platinum capacitors on the one-layer test chip heat treated in Edinburgh match curves from aluminium capacitors on a substrate manufactured at the same time as the one for the platinum capacitors. The workfunction of the platinum was determined to be 4.8 V which agrees well with the value of 4.75 V found in the literature. However, it also revealed inconsistencies in the C-V characteristics of capacitors made of platinum films used for transistors, namely a stretch-out of the capacitance curves. This can likely be attributed to traps at the silicon/silicon dioxide interface and could not be observed at capacitors manufactured using a single-mask process. The fact that the stretch-out was only seen on curves of the platinum capacitors and not on the ones of aluminium control samples, provides strong evidence that the properties of the MOS stack are influenced by the platinum layer deposited. Tsui and Chen [50] investigated the degradation of the dielectric of a Pt/SiO₂/Si structure during annealing and found an increased density of interface traps and a decreased dielectric strength after a heat treatment at temperatures above 600 °C (see Figure 9.1 and comments in Section 9.2). These effects were attributed to thermal stress and platinum dissolution into silicon dioxide, respectively. According to the findings published, the annealing temperatures of maximum 435 °C used in the present work and the 100 nm oxide result in good MOS stacks. This statement, however, should be applied carefully due to the long annealing times used in this research.

Chapter 7 analysed the microstructure of the platinum films by means of AES (Auger Electron Spectroscopy) and XPS (X-ray Photoelectron Spectroscopy) and found the films to be contaminated with large amounts of carbon with the atomic ratio Pt:C being 1.95:1. It has been reported earlier that organic contaminants can significantly increase the number of interface charges under very thin gate oxides [116]. Chapter 7 identified carbon in the metal films which could be the origin of the interface charges expected on grounds of Chapter 6 and Chapter 8. Although the organic contamination of oxides investigated in the literature [116, 117, 118] relates to silicon dioxides much thinner than the one of 100 nm thickness used in this work, it provides a possible explanation for the behaviour of the platinum capacitors characterised in Chapter 6.

Chapter 8 reported on working P-MOS transistors and provided further evidence for interface traps in the MOS stack. In contrast to transistors with an aluminium gate, the platinum gate devices did not show a steep subthreshold slope in the output characteristic which can be the result from charges at the silicon/silicon dioxide interface. The threshold voltage of the platinum gate transistors, which was extracted by fitting a simple physical model to measured $V_{GS} - I_D$ and $V_{DS} - I_D$ curves, was found to be more negative than the one of the aluminium gate device which is likely to have the same cause as the low subthreshold slope.

9.2 Implications

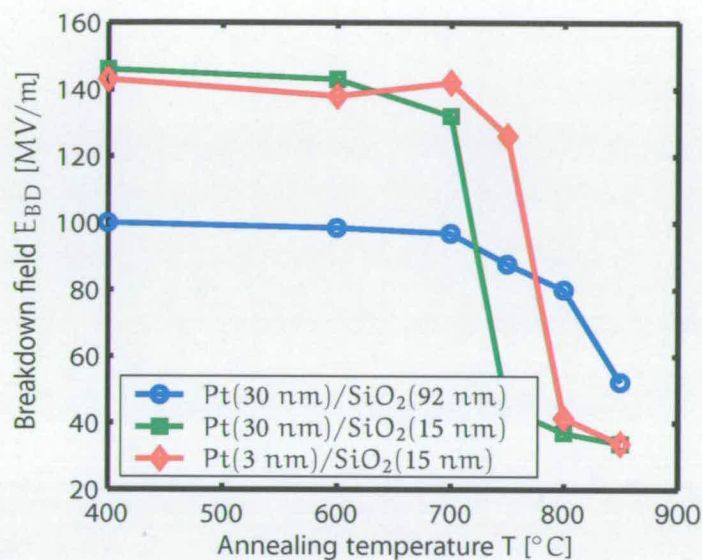
The above findings indicate that the films produced are of metallic nature and have properties which make the films superior compared to many metal layers produced by similar processes reported in the literature, as it can be seen when comparing the results from the films dealt with herein to data listed in Table 2.3. However, the research highlighted that the repeatability of the material supplied left something to be desired and to overcome this engineering resource is required to develop a robust and manufacturable product. It should be noted that the coater system that was used may well have contributed to the variability of the film performance and the combination of these effects made the dimension of features difficult to control. In addition the deposition system was only able to produce very thin films and these two factors make it difficult to use even in CMOS processes where feature sizes are in the range of $1\ \mu\text{m}$.

An investigation into the use of the organometallic process in semiconductor manufacturing done in 2001 and based on preliminary results identified several possible applications of the process [119]. These were high quality passive components for analog circuits, local interconnects and under-pad wiring. The conclusion, however, was based on data which, in this work, was found to be too optimistic and is therefore doubtful.

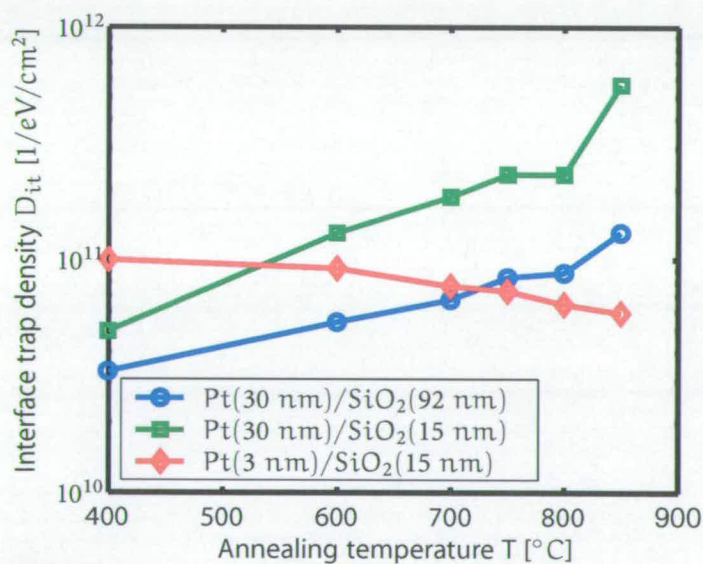
Still, the simple process which works without etching nor solvents, together with the good conductivity and small feature size compared to films reported in the literature, could make the layers useful for a wide range of applications, especially in the field of MEMS (Microelectromechanical Systems). Here the feature sizes are often large and a conducting layer made of a certain metal is often the main interest with the actual resistivity and purity being of lower priority. Thicker films would certainly increase the attractiveness of the process but also create further challenges. As seen in Chapter 3, the organometallic material before exposure is more than ten times thicker than the resulting metal layer. If the function of this ratio is linear, a layer of organometallic $10\ \mu\text{m}$ thick needs to be deposited to create a metal layer of $1\ \mu\text{m}$ thickness. Due to its photosensitivity, the organometallic material absorbs light and thus prevents an uniform exposure from its surface to the underlying substrate [120]. A film ten times thicker than the one used in this research would increase the absorption

substantially, perhaps result in a very weak exposure of the lowest regions and prevent the formation of a good interface between the metal and the substrate. Cross sections of platinum features showed also that the dimensions of structures produced are generally larger than on the mask. A possible explanation for this is the diffraction of the UV light at the crystal structure of the organometallic material during exposure. According to the laws of optics, the diffraction depends, among other things, on the wavelength of the incident light. Light sources other than the UV exposure tool used in this work, together with a suitable organometallic, should consequently allow an improved resolution of the process. Light of higher energy could also help to expose thick layers of organometallic and exceed the platinum thickness of approximately 150 nm achieved in this work.

As briefly mentioned in Chapter 3, the chemistry of the organometallic material can also be adapted to deposit metals such as silver, gold, molybdenum, hafnium, tantalum and tungsten. The refractory metals molybdenum and tungsten included in this list were found to have properties suitable for self-aligned metal gate processes [121, 122, 123]. Because of characteristics like their high conductivity and compatibility with advanced dielectrics, metals are thought to play a significant role as gates in future semiconductor technologies (see Chapter 2). An organometallic material based on molybdenum or tungsten, together with an improved process, could provide an efficient way to deposit and pattern metal for such a process. Platinum, which was used in this work, has a melting point of 1772 °C [46] which is well above the usual annealing temperature necessary for implant activation in a self-aligned gate process. However, research showed that thermal annealing of Pt/SiO₂/Si structures increases the density of surface states at the silicon/silicon dioxide interface and decreases the dielectric strength of the oxide if heated to temperatures above approximately 600 °C [50]. The degradation of the oxide is strongly dependent on the thickness of the films involved. While for a sample with 30 nm of platinum on 92 nm silicon dioxide the degradation of the breakdown voltage begins at temperatures above some 700 °C (see Figure 9.1(a)), it starts about 100 °C lower if the two films involved have thicknesses of 30 nm and 15 nm, respectively. Figure 9.1(b) shows a linear behaviour of the interfaced trapped charge plotted against the annealing temperature. Because of its effect on underlying oxide at elevated temperatures, platinum can thus not be deposited before an implant activation step, which is necessary for a self-aligned gate process. The creation of transistors with platinum gates and short lengths is therefore difficult to achieve. The replacement gate technology [29] provides a solution to the problem by masking the source/drain implantation with a polysilicon gate which is then replaced by one made of metal.



(a) Breakdown field.



(b) Interface trap charge.

Figure 9.1: Influence of annealing temperature on oxide breakdown field and interface trap density of a MOS structure [50].

9.3 Further work

The simplicity of the organometallic process reported in this work and the properties of the films produced certainly give good reasons for further investigations into the use of organometallic materials for integrated circuit manufacturing processes and MEMS.

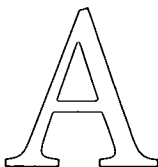
The research presented in this thesis provides clues about the quality of films which can be achieved by the method but to go a step further, it will be necessary to optimise and characterise organometallic material and process so as to reach a good level of reproducibility. The limited number of samples available for this work prevented in-depth analysis of problems encountered and did not allow conclusive conclusions. The lack of resource available at Dundee to address the reproducibility/material quality issues limited the scope of the work that was possible. The non-availability of well characterised material unfortunately prevented a full CMOS process being developed and other studies such as investigating different deposition processes, ageing properties of the material after synthesis and the influence of film thickness on exposure time as well as contamination.

After sufficient progress in material development has been made, the methods used in this work can be applied to characterise the films and the results employed to modify the process for specific applications. In the case of transistors, an analysis of the compatibility of the deposited layers with advanced dielectrics and the fabrication of a complete CMOS structure could provide important information necessary to evaluate the use of the films in future processes.

Beside the application of the organometallic compound in integrated circuits manufacturing, one could also investigate the use of the material for other technologies which do not allow standard lithography and etch techniques. Once a technology has been identified, suitable characterisation methods can be selected and applied for evaluation of the process for the according technology.

While the work on the existing organometallic processes is important, the development of new materials which allow a shorter exposure and the deposition of metals other than platinum is also essential. The forty minutes necessary for exposure of the organometallic $(C_3F_7)(CH_3)Pt^{II}-C_8H_{12}$ have already been reduced to less than half the time of its predecessor $(C_3F_7)_2Pt^{II}-C_8H_{12}$ but are still far from the few seconds needed to expose conventional photoresist. Lithography tools usually work on one wafer at a time, which is in contrast to equipment like furnaces where a batch of wafers is processed simultaneously, and a short run time is therefore crucial. The findings of the measurements reported herein also show the newer one of the two materials having a lower resistivity than the older one. An investigation into this outcome could provide valuable information leading to materials which result in metal films with even better conductivity.

Test structures



A.1 UDEA V0

Type	Name	Dimension
Resistive	Greek cross	w = 1 μm
		w = 2 μm
		w = 3 μm
		w = 4 μm
		w = 5 μm
		w = 10 μm
	Bridge resistor	w = 1 μm / l = 50 μm
		w = 1 μm / l = 150 μm
		w = 5 μm / l = 100 μm
		w = 5 μm / l = 300 μm
		w = 10 μm / l = 150 μm
		w = 10 μm / l = 350 μm
	Box cross	w = 50 μm
		w = 25 μm
		w = 10 μm
	Cross bridge	w = 0.8 μm / l = 200 μm
		w = 0.9 μm / l = 200 μm
		w = 1 μm / l = 200 μm
		w = 1.2 μm / l = 200 μm
		w = 2 μm / l = 300 μm
		w = 3 μm / l = 300 μm
		w = 4 μm / l = 300 μm
		w = 5 μm / l = 300 μm
		w = 6 μm / l = 400 μm
		w = 7 μm / l = 400 μm
		w = 8 μm / l = 400 μm
		w = 10 μm / l = 400 μm
Capacitive	Capacitor	A = 1 mm ²
		A = 2 mm ²

Type	Name	Dimension
		A = 3 mm ²
		A = 4 mm ²
		A = 5 mm ²
		A = 7.5 mm ²

A.2 UDEA V1

Type	Name	Material	Dimension
Transistor	P-MOS transistor	Platinum	$l = 12\text{ }\mu\text{m} / w = 10\text{ }\mu\text{m}$
			$l = 12\text{ }\mu\text{m} / w = 10\text{ }\mu\text{m}$
			$l = 12\text{ }\mu\text{m} / w = 20\text{ }\mu\text{m}$
			$l = 12\text{ }\mu\text{m} / w = 40\text{ }\mu\text{m}$
			$l = 12\text{ }\mu\text{m} / w = 60\text{ }\mu\text{m}$
			$l = 12\text{ }\mu\text{m} / w = 80\text{ }\mu\text{m}$
			$l = 15\text{ }\mu\text{m} / w = 10\text{ }\mu\text{m}$
			$l = 15\text{ }\mu\text{m} / w = 20\text{ }\mu\text{m}$
			$l = 15\text{ }\mu\text{m} / w = 40\text{ }\mu\text{m}$
			$l = 15\text{ }\mu\text{m} / w = 60\text{ }\mu\text{m}$
			$l = 15\text{ }\mu\text{m} / w = 80\text{ }\mu\text{m}$
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			$l = 20\text{ }\mu\text{m} / w = 40\text{ }\mu\text{m}$
			$l = 20\text{ }\mu\text{m} / w = 60\text{ }\mu\text{m}$
			$l = 20\text{ }\mu\text{m} / w = 80\text{ }\mu\text{m}$
		Aluminium	$l = 12\text{ }\mu\text{m} / w = 10\text{ }\mu\text{m}$
			$l = 12\text{ }\mu\text{m} / w = 10\text{ }\mu\text{m}$
			$l = 12\text{ }\mu\text{m} / w = 20\text{ }\mu\text{m}$
			$l = 12\text{ }\mu\text{m} / w = 40\text{ }\mu\text{m}$
			$l = 12\text{ }\mu\text{m} / w = 60\text{ }\mu\text{m}$
			$l = 12\text{ }\mu\text{m} / w = 80\text{ }\mu\text{m}$
			$l = 15\text{ }\mu\text{m} / w = 10\text{ }\mu\text{m}$
			$l = 15\text{ }\mu\text{m} / w = 20\text{ }\mu\text{m}$
			$l = 15\text{ }\mu\text{m} / w = 40\text{ }\mu\text{m}$
			$l = 15\text{ }\mu\text{m} / w = 60\text{ }\mu\text{m}$
			$l = 15\text{ }\mu\text{m} / w = 80\text{ }\mu\text{m}$
			$l = 20\text{ }\mu\text{m} / w = 10\text{ }\mu\text{m}$
			$l = 20\text{ }\mu\text{m} / w = 20\text{ }\mu\text{m}$
			$l = 20\text{ }\mu\text{m} / w = 40\text{ }\mu\text{m}$
			$l = 20\text{ }\mu\text{m} / w = 60\text{ }\mu\text{m}$
			$l = 20\text{ }\mu\text{m} / w = 80\text{ }\mu\text{m}$
Resistive	Greek cross	Platinum	$w = 2\text{ }\mu\text{m}$
			$w = 5\text{ }\mu\text{m}$

Type	Name	Material	Dimension
Bridge resistor		Aluminium	w = 10 μm
			w = 20 μm
			w = 2 μm
			w = 5 μm
			w = 10 μm
			w = 20 μm
		Platinum	w = 5 μm / l = 200 μm
			w = 10 μm / l = 200 μm
		Aluminium	w = 5 μm / l = 200 μm
			w = 10 μm / l = 200 μm
Cross bridge		Platinum	w = 0.1 μm / l = 200 μm
			w = 0.2 μm / l = 200 μm
			w = 0.3 μm / l = 200 μm
			w = 0.4 μm / l = 200 μm
			w = 0.6 μm / l = 200 μm
			w = 0.8 μm / l = 200 μm
			w = 1 μm / l = 200 μm
			w = 2 μm / l = 200 μm
			w = 3 μm / l = 200 μm
			w = 5 μm / l = 200 μm
			w = 10 μm / l = 200 μm
			w = 20 μm / l = 200 μm
		Aluminium	w = 0.1 μm / l = 200 μm
			w = 0.2 μm / l = 200 μm
			w = 0.3 μm / l = 200 μm
			w = 0.4 μm / l = 200 μm
			w = 0.6 μm / l = 200 μm
			w = 0.8 μm / l = 200 μm
			w = 1 μm / l = 200 μm
			w = 2 μm / l = 200 μm
			w = 3 μm / l = 200 μm
			w = 5 μm / l = 200 μm
Contact resistance test structure		Platinum	w = 5 μm
			w = 10 μm

Type	Name	Material	Dimension
Capacitive	Capacitor	Aluminium	$w = 20 \mu\text{m}$
			$w = 5 \mu\text{m}$
			$w = 10 \mu\text{m}$
			$w = 20 \mu\text{m}$
		Platinum	$A = 500 \mu\text{m} \times 500 \mu\text{m}$
			$A = 1000 \mu\text{m} \times 1000 \mu\text{m}$
			$A = 2000 \mu\text{m} \times 2000 \mu\text{m}$
	Interdigitated capacitor	Aluminium	$A = 500 \mu\text{m} \times 500 \mu\text{m}$
			$A = 1000 \mu\text{m} \times 1000 \mu\text{m}$
			$A = 2000 \mu\text{m} \times 2000 \mu\text{m}$
		Platinum	$n = 84 / l = 1100 \mu\text{m}$
			$/ w = 2510 \mu\text{m} / x = 20 \mu\text{m}$
			$/ s = 10 \mu\text{m}$
			$n = 20 / l = 1100 \mu\text{m}$
			$/ w = 590 \mu\text{m} / x = 20 \mu\text{m}$
			$/ s = 10 \mu\text{m}$
			$n = 170 / l = 1100 \mu\text{m}$
			$/ w = 4970 \mu\text{m} / x = 20 \mu\text{m}$
			$/ s = 10 \mu\text{m}$
		Aluminium	$n = 84 / l = 1100 \mu\text{m}$
			$/ w = 2510 \mu\text{m} / x = 20 \mu\text{m}$
			$/ s = 10 \mu\text{m}$
			$n = 20 / l = 1100 \mu\text{m}$
			$/ w = 590 \mu\text{m} / x = 20 \mu\text{m}$
			$/ s = 10 \mu\text{m}$
			$n = 170 / l = 1100 \mu\text{m}$
			$/ w = 4970 \mu\text{m} / x = 20 \mu\text{m}$
			$/ s = 10 \mu\text{m}$
Optical	Lines	Platinum	$w = 0.1 \mu\text{m}$
			$w = 0.2 \mu\text{m}$
			$w = 0.5 \mu\text{m}$
			$w = 1 \mu\text{m}$
			$w = 2 \mu\text{m}$
			$w = 5 \mu\text{m}$

Type	Name	Material	Dimension
		Aluminium	w = 10 μm
			w = 20 μm
			w = 40 μm
			w = 60 μm
			w = 0.1 μm
			w = 0.2 μm
			w = 0.5 μm
			w = 1 μm
			w = 2 μm
			w = 5 μm
			w = 10 μm
			w = 20 μm
			w = 40 μm
			w = 60 μm
Gaps		Platinum	w = 0.1 μm
			w = 0.2 μm
			w = 0.5 μm
			w = 1 μm
			w = 2 μm
			w = 5 μm
			w = 10 μm
			w = 20 μm
		Aluminium	w = 40 μm
			w = 60 μm
			w = 0.1 μm
			w = 0.2 μm
			w = 0.5 μm
			w = 1 μm
			w = 2 μm
			w = 5 μm
			w = 10 μm
			w = 20 μm
			w = 40 μm
			w = 60 μm

Type	Name	Material	Dimension
	Checker board	Platinum	w = 5 μm
			w = 10 μm
			w = 20 μm
			w = 40 μm
		Aluminium	w = 5 μm
			w = 10 μm
			w = 20 μm
			w = 40 μm

Process

B

B.1 UDEA V0

B.1.1 Runsheet

Process runsheet				
Process name:		UDEA V0.0 A1 (Batch MHD 03 11 20 B)		Run number: 2
Starting material:		3", n-type, <100>, Si wafers		Number of wafers: 1
Step number	Description	Date	Initials	Comments
1	Oxidation Tube 1, program WOXHCL14, 1 hour			
2	Photoresist coat Front of wafer, SPR2, 5200 rpm			
3	Oxide etch Plasmatherm, CF_4/H_2 , ca. 40 minutes, 750W			
4	Photoresist strip Barrel asher, 1 hour			
5	Phosphorous deposition Tube 5, program SLDSCE12, solid source, 15 minutes			
6	Oxide etch 4:1 buffered HF (40% NH_4F : 48% HF), 3 minutes			
7	Oxidation Tube 1, program WOXHCL11, 20 minutes			
8	Anneal Tube 1, 30 minutes, 950°C, N_2			
9	Aluminium sputter Balzers, pre-clean, 1µm aluminium			
10	Photoresist coat Front of wafer, SPR2, 5200 rpm			
11	Exposure Cobilt, 15 seconds			
12	Photoresist develop HB115C			
13	Aluminium etch STS, program AL3INL.SET, ca. 20 minutes			
14	Photoresist strip Barrel asher, 1 hour			
15	Photoresist coat Front of wafer, SPR2, 5200 rpm			
16	Oxide etch 4:1 buffered HF (40% NH_4F : 48% HF), 1 minute			
17	Aluminium sputter Balzers, pre-clean, 0.5µm aluminium			

Step number	Description	Date	Initials	Comments
18	Photoresist strip Barrel asher, 1 hour			
19	Aluminium sinter Tube 8, program HNSINT01, 2 hours			

B.2 UDEA V1

B.2.1 Runsheet

Process runsheet				
Process name: UDEA V1.0 (Batch MHD 03 11 19 A)			Run number: 5	
Starting material: 3", n-type, <100>, Si wafers			Number of wafers: 5	
Step number	Description	Date	Initials	Comments
1	Oxidation Tube 1, program WOXHCL14, 1 hour			
2	Photoresist coat Front of wafer, SPR2, 5200 rpm			
3	Oxide etch Plasmatherm, CF_4/H_2 , ca. 40 minutes, 750W			
4	Photoresist strip Barrel asher, 1 hour			
5	Phosphorous deposition Tube 5, program SLDSC12, solid source, 15 minutes			
6	Deglaze 10% HF dip, 80 seconds			
7	Oxidation Tube 1, program WOXHCL11, 1 hour			
8	Photoresist coat Front of wafer, SPR2, 5200 rpm			
9	Exposure Mask 1, Karl Suss, soft contact, 8 seconds			
10	Photoresist develop HB115C			
11	Oxide etch Plasmatherm, CF_4/H_2 , ca. 40 minutes, 750W			
12	Photoresist strip Barrel asher, 1 hour			
13	Boron deposition Tube 7, program BNDEP12, solid source, 30 minutes			
14	Deglaze 10% HF dip, 80 seconds			
15	Field oxide Tube 1, program FOXHCL11, 15 hours			
16	Photoresist coat Front of wafer, SPR2, 3300 rpm			
17	Exposure Mask 2, Karl Suss, soft contact, 8 seconds			

Step number	Description	Date	Initials	Comments
18	Photoresist develop HB115C			
19	Oxide etch Plasmatherm, CF_4/H_2 , ca. 60 minutes, 750W			
20	Photoresist strip Barrel asher, 1 hour			
21	Pre-oxidation clean 10% HF dip, 5 seconds			
22	Gate oxide Tube 1, program WOXHCL11, 15 minutes			
23	Anneal Tube 1, 30 minutes, 950°C, N_2			
24	Deposition of organometallic material PVD, 100 mg organometallic material			
25	Exposure Mask 4, 2 hours			
26	Heat treatment Oven idling at 25°C, ramp temperature to 70°C within 10 minutes, hold temperature for 6 hours, ramp temperature to 195°C within 25 minutes, hold temperature for 4 hours, let oven cool down to 25°C, furnace treatment at 435°C for 2 hours in a 40% H_2 in N_2 atmosphere			
27	Clean Ultrasonic bath in acetone, 1 minute, rinsing with IPA			
28	Photoresist coat Front of wafer, SPR2, 5200 rpm			
29	Exposure Mask 3, Karl Suss, soft contact, 8 seconds			
30	Photoresist develop HB115C			
31	Oxide etch Plasmatherm, CF_4/H_2 , ca. 5 minutes, 750W			
32	Photoresist strip Fuming nitric, 5 minutes			
33	Aluminium sputter Balzers, 0.5µm aluminium			
34	Photoresist coat Front of wafer, SPR2, 3300 rpm			
35	Exposure Mask 5, Karl Suss, soft contact, 8 seconds			

Step number	Description	Date	Initials	Comments
36	Photoresist develop HB115C			
37	Aluminium etch MIT aluminium etch, 45°C			
38	Photoresist strip Fuming nitric, 5 minutes			
39	Photoresist coat Front of wafer, SPR2, 3300 rpm			
40	Oxide etch Plasmatherm, CF_4/H_2 , ca. 60 minutes, 750W			
41	Aluminium sputter Balzers, pre-clean, 0.5µm aluminium			
42	Photoresist strip Fuming nitric, 5 minutes			
43	Aluminium sinter Tube 8, program HNSINT01, 10 minutes			

B.2.2 Design rules

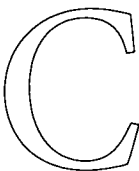
Mask no.	Description	Drawn dimension [μm]	Required mask tolerance [μm]	Dimension on wafer [μm]
1	Minimum space between unrelated p ⁺	15	15 - 16	14 - 15
	Minimum p ⁺ source to drain separation	12	12 - 13	11 - 12
	Minimum p ⁺ source or drain extension beyond transistor width	2		
	Minimum p ⁺ line width	6	5 - 6	6 - 7
	Minimum separation of p ⁺ and scribe channel	24		
2	Minimum gate width	6	5 - 6	6 - 7
	Minimum gate to source or drain overlap	4		
	Minimum space between gate cuts	15		
	Minimum separation of gate and unrelated p ⁺	18		
	Minimum contact thinning to diffusion edge separation	4		
3	Contacts drawn oversize with relation to mask 2	2		
	Minimum contact size	10 × 10	9 × 9 - 10 × 10	
4	Minimum track width	15		
	Minimum separation of metal 1 and scribe channel	24		
	All gate oxide must be covered by metal			
5	Minimum track width	15	15 - 16	13 - 14
	Minimum space between tracks	6	5 - 6	7 - 8
	Minimum separation of metal 2 and metal 1	6		

Mask no.	Description	Drawn dimension [μm]	Required mask tolerance [μm]	Dimension on wafer [μm]
	Minimum overlap of metal and contact thinning	6		
	Bonding pad size	120 × 120		
	Minimum separation of bonding pads	100		
	Minimum separation of metal 2 and scribe channel	24		
6	Opening spacing within bonding pad	8		

B.2.3 Mask nomenclature and sequence

Mask number	Description	Layer name	Alignment
1	Boron Diffusion	Diffusion	
2	Thin oxide for gates and contacts	Thin oxide	Aligns to mask 1
4	Gate metal	Metal 1	Aligns to mask 2
3	Contact holes	Contacts	Aligns to mask 2
5	Metal interconnection and pads	Metal 2	Aligns to mask 2
6	Protective oxide	Overglaze	Aligns to mask 5

Errors introduced by profilometer tip



PROFILOMETERS provide a simple way for surface profiling. However, the construction of a profilometer introduces errors into the profiles measured and these need to be considered when evaluating the results. Some of the problems associated with profilometers are described in the literature [124, 125].

The error of interest for this project is visualised in Figure C.1(a). It can be seen that in the example shown, the dimension of the structure along the x-axis is larger than the actual feature.

A Dektak 8000 profilometer with a ball shaped tip with a radius of 2.5µm was used in this work. The size of the error depends on the angle α between a horizontal line and the slope of the feature (Figure C.1(b), representing the steepness of the feature). The angle can be used to calculate the correction for the x and the y axis which are

$$\Delta x = r \cdot \cos \left(\frac{\pi}{2} - \alpha \right) \tag{C.1}$$

and

$$\Delta y = r \cdot \sin \left(\frac{\pi}{2} - \alpha \right), \tag{C.2}$$

respectively, where r is the radius of the tip.

The expressions above can be used to compute the error expected at any position of a profile. Three different profiles, which are shown in Figure C.2, were chosen and the maximum error in the x-axis calculated. The largest difference between the measured and the actual profile occurs most often at the position where the tip touches a feature on a flat surface for

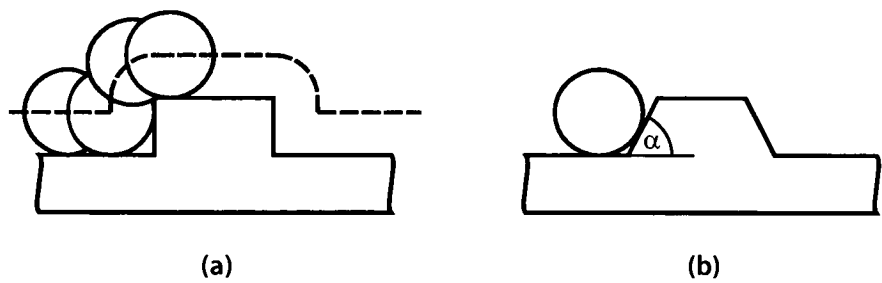


Figure C.1: Illustration (a) shows a profile (solid line) and the curve resulting from a measurement with a ball-shaped profilometer tip (dashed line). The angle α used to investigate the error is depicted in (b).

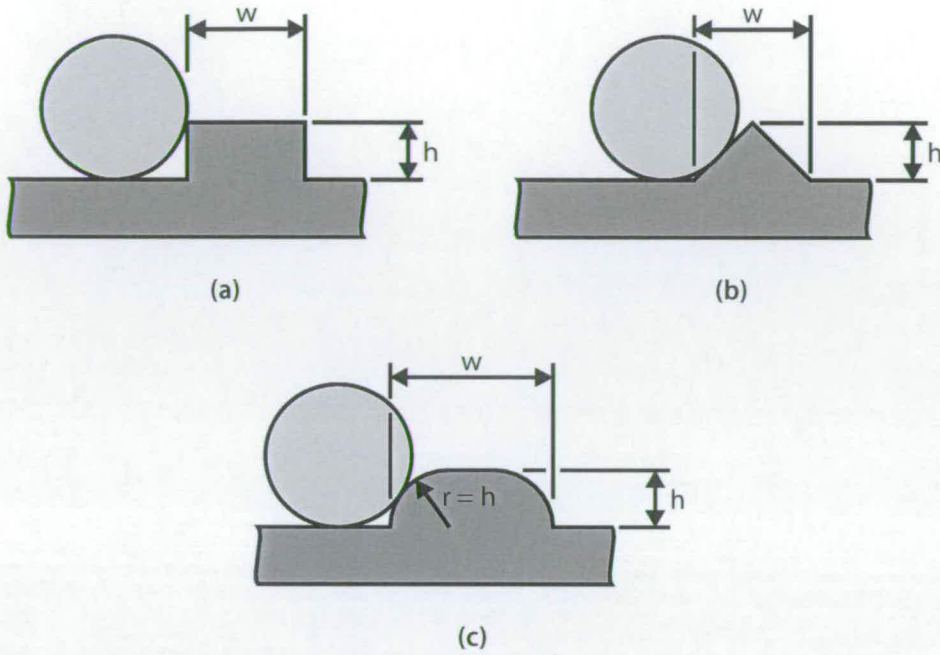


Figure C.2: Profiles used to investigate the errors caused by the tip of the profilometer.

the first time. The points of maximum error for the profiles discussed are visualised in Figure C.3 and are represented by coloured dots. The cross section depicted in Figure C.2(a) would be the one of an ideal film, while the one in Figure C.2(c) is thought to roughly represent the film topography of the actual films deposited using the organometallic process. The results are listed in Table C.1.

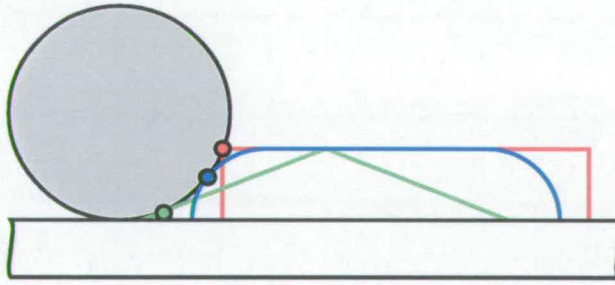


Figure C.3: The points of maximum error for the three different feature shapes discussed in this chapter.


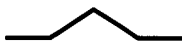

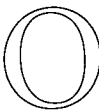
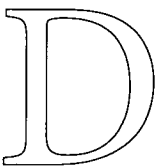
Shape	Height h [μm]	Maximum error [μm]
	1	2.00
	0.5	1.50
	0.1	0.70
	0.05	0.50
	1	0.93
	0.5	0.49
	0.1	0.10
	0.05	0.05
	1	1.75
	0.5	1.38
	0.1	0.69
	0.05	0.49

Table C.1: Maximum errors expected for structures characterised using a profilometer with a tip radius of 2.5 μm . A value of 5 μm was used for the width w shown in Figure C.2.

Published papers



n the following pages, papers are contained which were presented at ICMTS (International Conference on Semiconductor Test Structures) and published in IEEE Transactions on Semiconductor Manufacturing.

**D.1 International Conference on Semiconductor Test Structures
(Monterey, USA, 2003)**

Use of Test Structures for Characterising a Novel Photosensitive Organometallic Material for MOS Processes

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ABSTRACT

A novel process is presented which produces platinum features using direct UV exposure of a photosensitive organometallic material. The deposited films are metallic and have a good adhesion to silicon dioxide. A test chip with MOS capacitors and sheet resistance structures fabricated using the new organometallic material has been characterised.

I. INTRODUCTION

As microelectronic device geometries reduce in size there is a need for new materials and processes that meet the requirements and overcome the limitations of existing solutions. We have developed a photosensitive organometallic material that can readily be patterned on a standard silicon wafer [1]. The organometallic film is photo-sensitive and can be exposed using conventional lithography tools to produce patterned metal layers without the need for photoresist or etch processes. The reduction of process steps has great significance from the manufacturing viewpoint.

The method commonly used to produce metal features (Figure 1) involves the deposition of the metal followed by a layer of photoresist which is then exposed and developed. This mask is then used to etch the metal to create the required features. A similar type of procedure is employed in a damascene metallisation process with the addition of a CMP (Chemical Mechanical Polishing) step. The organometallic material reported in this work reduces the number of steps involved in patterning a metal layer (Figure 2). First an organometallic compound is deposited on the wafer and exposed to UV light which causes the platinum to dissociate. A final heat treatment removes any remaining unexposed organometallic material and residues and leaves behind the required metal pattern.

This paper presents details of the deposition and patterning process and reports on the characterisation of the resulting metal.

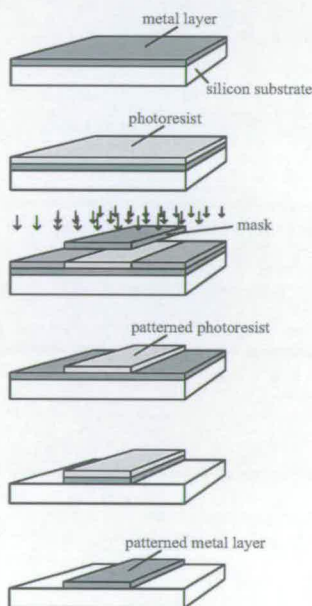


Fig. 1. Conventional technique commonly used to deposit and pattern a metal layer.

II. MATERIALS AND METHODS

For the characterisation of the platinum layers a test chip (Figure 3) consisting of resistive and capacitive test structures has been manufactured using the fluoro platinum complex [1], *cis* - $(C_3F_7)_2Pt(II) - C_8H_{12}$, whose chemical structure is shown in Figure 4. Capacitors for C-V measurements have areas ranging from 1 mm^2 to 7.5 mm^2 and possess guard rings to avoid errors due to condensation water on the surface of the wafer. The resistivity structures include Greek crosses and bridge resistors which have track widths between $0.8\text{ }\mu\text{m}$ and $10\text{ }\mu\text{m}$.

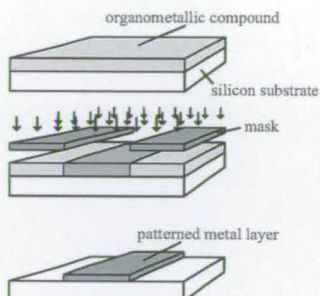


Fig. 2. Deposition and patterning process of a metal layer using the organometallic process described in this paper.

μm thus allowing the same design to be used for further research on organometallic material with an improved resolution.

Standard processes have been employed for all but the metallisation step during production of the test structures. A 500 nm oxide is grown on a n-type $\langle 100 \rangle$ silicon wafer with a resistivity of 2-4 Ωcm . The back of the wafer is then heavily n-type doped to create a good ohmic contact to the aluminium which is deposited later in the process. The masking oxide on the front is removed and the whole wafer then reoxidised to a thickness of 100 nm.

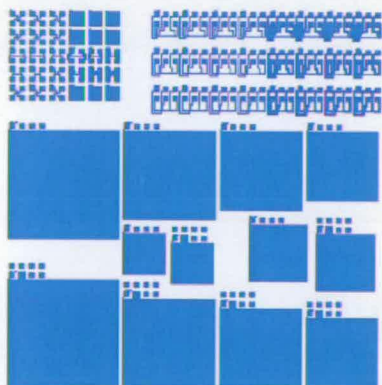


Fig. 3. Test chip produced for resistance and capacitance measurements.

After this preparation, 100 mg of organometallic compound is evaporated onto the silicon dioxide using an Edwards Auto 306 Vacuum Coater. During the process some 9.25 mg of material is deposited which corresponds

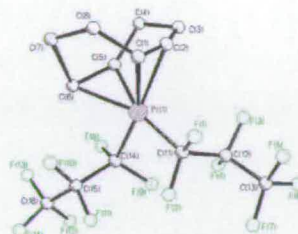


Fig. 4. Chemical structure of the organometallic compound.

to a layer thickness of approximately $0.75 \mu\text{m}$. The pattern is then contact printed using a 260 nm exposure tool with an output of 16.5 mWcm^{-2} . During exposure the metallic part of the organometallic material dissociates from the organic part, which is removed together with the unexposed compound using a three stage heat treatment, of which the first two are conducted at this point. For stage 1 the wafer is furnace treated at a temperature of 70°C for six hours in air and during stage 2 at a temperature of 195°C for four hours in air. The oxide on the back of the wafer is then stripped off and an aluminium layer of 500 nm sputtered on the back of the wafer. The manufacturing is finalised with the last stage of the heat treatment which is also used to sinter the aluminium on the back of the wafer and is conducted in an atmosphere of 40 % hydrogen in nitrogen at a temperature of 435°C . The duration of this last annealing stage was thought to have a strong influence on the film composition and was varied between two and six hours so as to study the influence of the time on flatband voltage and resistivity. Silicon wafers with both platinum and aluminium structures were processed for the work described in this paper. The platinum structures were manufactured using the organometallic process described above whereas the aluminium features were produced using sputtering and standard lithography. The processes used for both the wafers with the platinum and the aluminium pattern were kept as identical as possible so as to allow direct comparison of results gained from capacitance measurements.

III. RESULTS

Figure 5(a) and Figure 5(b) show a Greek cross [3] and a bridge resistor, respectively, both of which had a designed track width of $10 \mu\text{m}$ and were produced using the organometallic process. The pictures also show a residue in between the pattern and the exact cause of this is unknown. This is not observed in large open areas of the test pattern which indicates that the residue might

be caused by some sort of proximity effect. Figure 6 shows examples of cross sections obtained from measurements on structures of different sizes using a Dektak 8000 profilometer. The measurements showed that the dimensions of the features were generally larger than expected, walls were not perpendicular and the thickness of the platinum film varied between 30 and 50 nm over the whole wafer. This dependence of the film thickness on the location on the wafer is believed to be a result from a nonuniform evaporation process. A Scotch tape test indicated that the film had a good adhesion to the substrate.

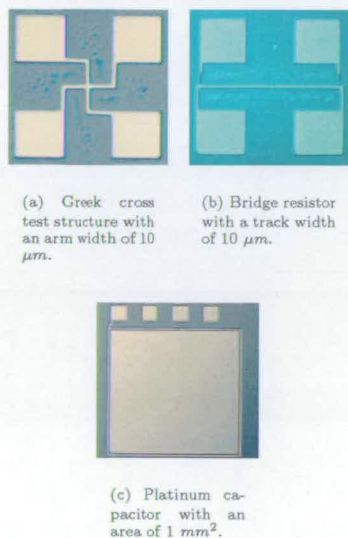


Fig. 5. Test structures produced using the organometallic process.

Figure 7 shows a typical C-V curve of a platinum capacitor measured at 1 MHz [2] using a HP4280A C-V meter. For comparison a similar measurement of an aluminium capacitor on the same substrate and a curve calculated using the theory described by Brews [4] are also shown. It can be seen that both curves follow the same trend. This, together with no difference between the measured oxide leakage currents, indicates that the gate stack is potentially suitable for transistor operation. Measurements of the flatband voltage after different annealing times showed that the flatband voltage moves towards lower values with longer time and seems to asymptotically approach a constant value (Figure 8(a)). From the shift of the C-V curves obtained after six hours an-

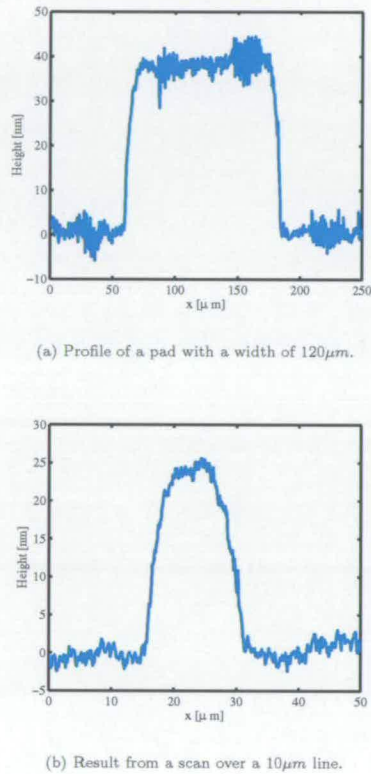
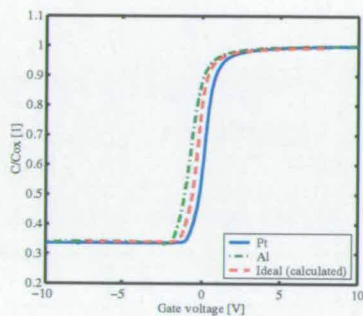
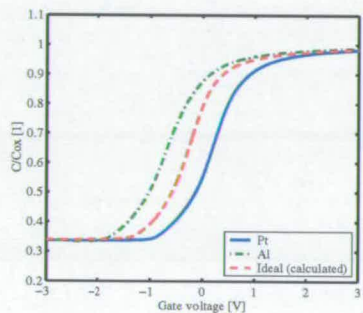


Fig. 6. Typical profiles of the deposited platinum films obtained using a Dektak.

nealing time and the known workfunction of 4.1 V of aluminium [5], the workfunction of the platinum film was calculated to be 4.8 V which is close to the value of 4.75 V found in the literature [6]. The resistivity of the platinum films deposited by the organometallic process has been measured using both Greek cross structures and bridge resistors. The sheet resistance decreased significantly with increasing annealing time and a trend towards an asymptotical value was observed. Due to the sloping walls and line widths which were typically larger than designed after the heat treatment, the calculation of the resistivity required to take the track width, height and profile into account. It was observed that the resistivity values measured using the



(a) Plot of the C-V curves over the whole measurement range.

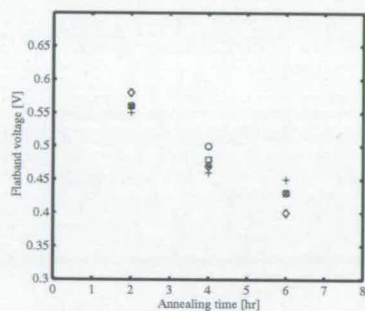


(b) Expanded middle portion of curves shown in Figure 7(a).

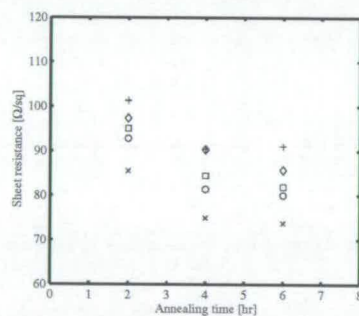
Fig. 7. Typical C-V curves obtained at 1 MHz of both a Pt (deposited using the organometallic process) and an Al (deposited by sputtering) capacitor on a n-type substrate. A calculated ideal curve with $V_{FB} = 0V$ is also shown for comparison.

Greek cross structures were generally higher than the values from measurements at bridge resistors. This seems to be caused by the profile of the tracks which is included differently in the results from the two types test structures. In order to get a reliable value for the resistivity, the area of a track was calculated using profiles measured at several positions on a bridge resistor and the outcome combined with the resistance. The resistivity of the films after a six-hour anneal was determined to be $4.58 \times 10^{-6} \Omega m$ which is significantly higher than the reported resistivity of $1.06 \times 10^{-7} \Omega m$ [7]. It is well-known that thin

films have higher resistivities than the bulk material but Avrekh, Monteiro and Brown [8] reported an increase as we have measured it only for film thicknesses below 5 nm. It is suspected that in this case organic residues may be responsible for some of the difference and this requires further investigations. Contaminants like carbon from the organometallic precursor gas are also thought to be the cause of measured high resistivities of platinum films deposited using a FIB (Focused Ion Beam) system [9] and a solid organometallic material could behave likewise.



(a) Flatband voltage versus annealing time.



(b) Sheet resistance as a function of annealing time.

Fig. 8. Influence of annealing time on the flatband voltage and sheet resistance of the deposited films. The data was obtained from measurements at different locations on a wafer.

IV. DISCUSSION

This work has demonstrated that metal features in the form of test structures can be produced using a novel organometallic film which is patterned directly with UV light followed by very simple low temperature heat treatment steps. The measurements have shown that the deposited film is electrically conductive and the results from the capacitor dots indicate that it could potentially be used as a gate material for MOS transistors. However, the test patterns produced also indicate that the resolution of the deposited films is reduced by the bloating of the structures during the heat treatment process. The metal structures produced did not meet the requirements for an integration into a modern semiconductor process and further optimisation of the process is necessary before this can be achieved. Future work will also involve the design and fabrication of transistors using the organometallic process.

It should be noted that the chemistry used in this organometallic film is also capable of being adapted to produce patterns made of metals such as Ag, Au, Mo, Hf, Ta and W.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the help of L J Millar and G Smith in preparing the organometallic materials and thank A M Gundlach for his assistance in manufacturing the test structures.

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**D.2 International Conference on Semiconductor Test Structures
(Awaji, JP, 2004)**

A test chip to characterise P-MOS transistors produced using a novel organometallic material

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ABSTRACT

A test chip is reported to characterise MOS transistors with a platinum gate fabricated using a solid organometallic material. Threshold and source-drain characteristics are presented along with oxide leakage measurements. These results are compared with aluminium gate transistors manufactured on the same substrate. Both sets of characteristics are very similar with the major difference being that the platinum gate devices have a lower sub-threshold slope.

I. INTRODUCTION

It has been reported earlier [1] that the organometallic fluoro platinum complex *cis*-(C₃F₇)₂Pt(II)-C₈H₁₂ with the structure shown in Figure 1 could potentially be used to produce platinum gates for MOS transistors. The organometallic compound is a solid photosensitive material which can be exposed using UV, e-beam or ion-beam lithography to deposit patterned platinum layers onto a substrate.

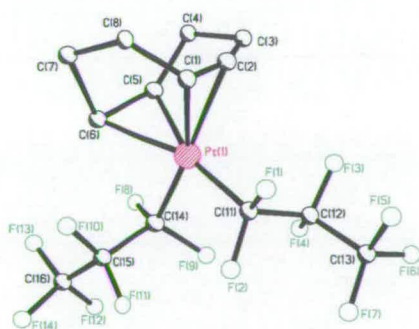


Fig. 1. Chemical structure of the organometallic material.

Metal features are typically produced by deposition of a metal layer onto a substrate which is then patterned using a photoresist mask and an etch step as shown in Figure 2(a).

The compound and associated process reported in this paper reduces the number of steps as shown in Figure 2(b). The organometallic material is first deposited onto the substrate and exposed using standard lithography which causes the platinum to dissociate. The organic residue in the exposed regions and the unexposed organometallic material are then removed using a low temperature heat treatment thus leaving behind the patterned metal layer.

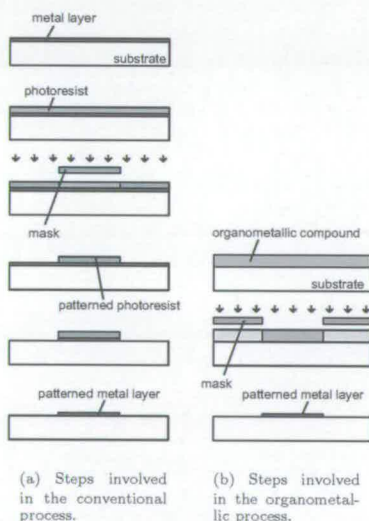


Fig. 2. Comparison of conventional and organometallic process when depositing a patterned metal layer.

Organometallic materials have been used in several areas of semiconductor manufacturing, mainly for the repair of integrated circuits or photolithographic masks. The method commonly used is focused ion beam induced deposition from an organometallic precursor gas [2]. Other techniques make use of the photothermal decomposition of an organometallic material, which can be in a solid [3], [4], [5] or a liquid phase [6], [7], by direct laser-writing. The photochemical decomposition of an organometallic allows smaller features and was employed to produce patterned metal layers by exposing organometallic materials through a photolithographic mask [8], [9], [10]. The processes reported require later treatment with a liquid developer or are used only to produce clusters for a following electroless metallisation.

The organometallic process used in this work is based on the photolytic decomposition by conventional UV lithography and does not require any laser, ion-beam or electron-beam exposure tools nor liquid developers.

This paper describes the manufacture and characterisation of a test chip which includes MOS transistors with platinum gates created using UV definition of an organometallic material. The purpose of the work is to demonstrate that photosensitive organometallic films can be integrated into a MOS process to produce fully functional transistors.

II. MATERIALS AND METHODS

A previously reported test chip [1] has established that organometallics have the potential to be used in an IC technology. This work describes a new chip (Figure 3) which incorporates a set of MOS transistors, capacitors for C-V measurements, resistive test structures and patterns for optical characterisation. All structures are realised both using the organometallic process and conventional processes using aluminium.

For this demonstration the number of process steps was minimised by basing the process and design rules on an existing metal gate process which produced p-MOS transistors with a platinum gate without the requirement for V_T implants. Figure 4(a) and Figure 4(b) show the cross-section of the platinum and aluminium gate transistors and it can be observed that aluminium was used for all the interconnect. Transistors with lengths of $12 - 20\mu\text{m}$ and widths of $10 - 80\mu\text{m}$ were fabricated.

The manufacturing process starts with the growth of an oxide onto a $<100>$ n-type silicon wafer. The oxide on the back is then removed and phosphorus diffused into the back of the wafer to be used later for a back contact. After reoxidation, the oxide on the front is patterned and used as a mask for the boron diffusion which forms the source and drain regions of the transistor. The field oxide is then created, gate and source/drain contact holes are opened and the gate oxide grown.

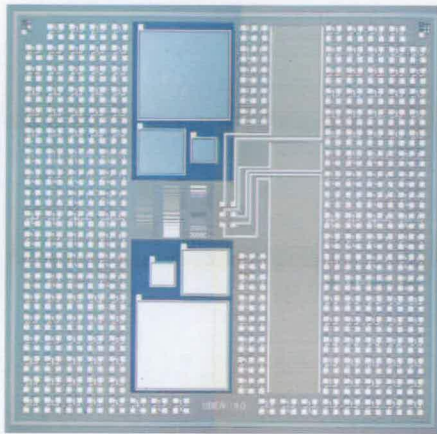


Fig. 3. Layout of the test chip.

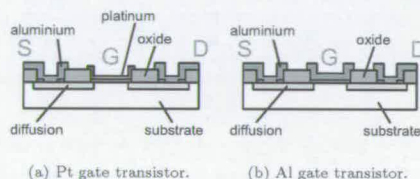


Fig. 4. Cross sections of the two transistor types.

The next step is the evaporation of 100mg organometallic compound which forms a layer with a thickness of some $0.75\mu\text{m}$ on the wafer. The organometallic film is then UV exposed using the gate mask which breaks the bonds between the metallic and organic part of the organometallic material. The organic part in the exposed regions, together with the unexposed compound, is then removed using a three-stage heat treatment. During stages one and two the wafer is furnace treated in air for six hours at a temperature of 70°C and for four hours at a temperature of 195°C , respectively. The final stage of the heat treatment is conducted in an atmosphere of 40% hydrogen in nitrogen for four hours at a temperature of 435°C . The resulting platinum layer had a thickness of approximately 50nm.

Contact holes are then opened by removing the gate oxide in the bottom and $0.5\mu\text{m}$ of aluminium deposited and patterned to create connections and pads. Next, the oxide on the back is removed and the aluminium back contact sputtered.

Figure 5(a) and Figure 5(b) show pictures of transistors with platinum and aluminium gate, respectively.

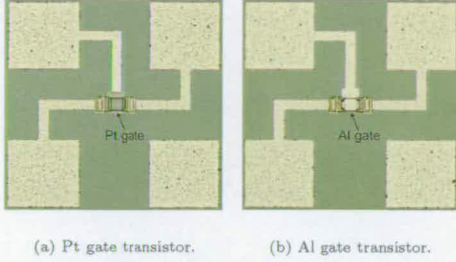


Fig. 5. Devices with gate length of 20 μm and width of 20 μm.

A magnified picture of a platinum gate transistor can be seen in Figure 6.

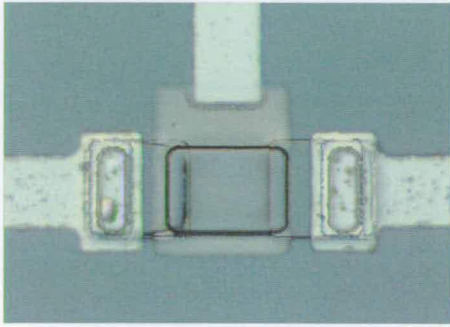


Fig. 6. Picture of a platinum gate transistor with a gate length of 20 μm and a width of 20 μm.

The transistors were characterised using a HP4156B semiconductor parameter analyzer together with the IC-CAP software package.

III. RESULTS

To characterise the transistors, $V_{GS}-I_D$ and $V_{DS}-I_D$ curves of both the platinum and aluminium transistors were acquired. Typical curves from a platinum gate transistor are shown in Figure 7 and Figure 8. Results from measurements at an aluminium transistor of the same size are shown in Figure 9 and Figure 10.

It can be seen that saturation and linear region of the two transistor types compare very well. A simple physical transistor model identical to the Shichman-Hodges model [11] or MOS Model 1 was fitted to the data

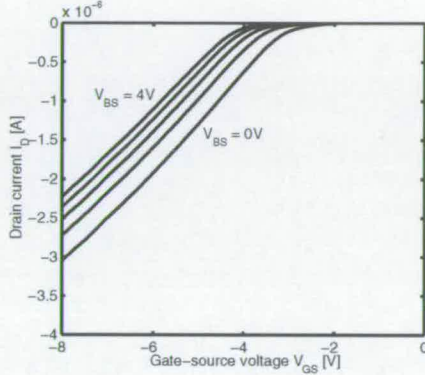


Fig. 7. $V_{GS}-I_D$ characteristic of a platinum gate transistor with a gate length of 20 μm and a width of 20 μm.

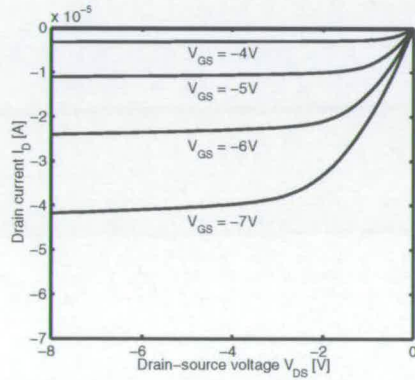


Fig. 8. $V_{DS}-I_D$ characteristic of a platinum gate transistor with a gate length of 20 μm and a width of 20 μm.

from the measurements. The transistors produced have big dimensions and the errors introduced by the simple model were therefore thought to be negligible [12]. The threshold voltage V_{TH} of the platinum and aluminium transistor was extracted and determined to be -3.0V and -2.1V, respectively. The region around the threshold voltage reveals that the platinum transistor turns on more slowly than its aluminium counterpart.

The characteristics shown in Figure 11 compare the sub-threshold regions of the aluminium and platinum transistors and it can be observed that the slope of the aluminium is much superior to the platinum device. The

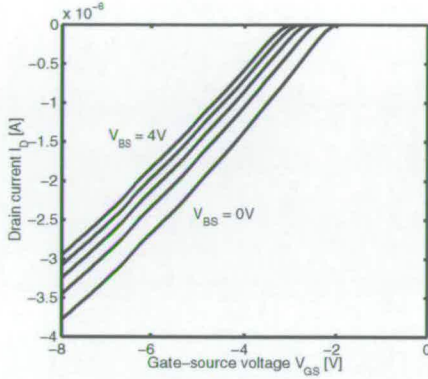


Fig. 9. V_{GS} - I_D characteristic of an aluminium gate transistor with a gate length of $20\mu m$ and a width of $20\mu m$.

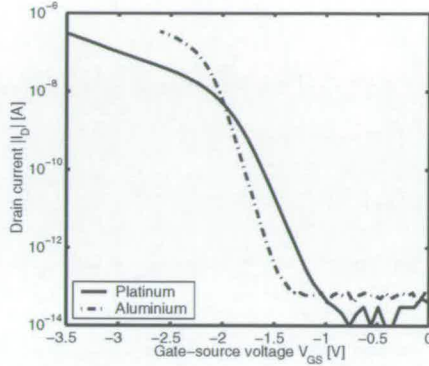


Fig. 11. Subthreshold characteristic of a transistors with a gate length of $20\mu m$ and a width of $20\mu m$.

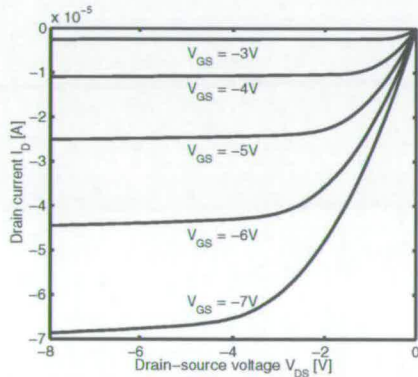


Fig. 10. V_{DS} - I_D characteristic of an aluminium gate transistor with a gate length of $20\mu m$ and a width of $20\mu m$.

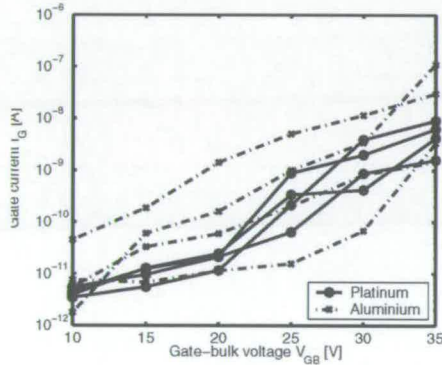


Fig. 12. I-V characteristic of the oxide measured using capacitors with an area of $4mm^2$.

IV. DISCUSSION

reasons for this are unclear as the two devices were fabricated on the same wafer. Hence, the gate oxide for both devices was grown at the same time with the platinum device only having an extra heat treatment to pattern and anneal the gate.

The I-V measurements shown in Figure 12 presents the oxide leakage current as a function of voltage and the results are in line with data available in the literature [13].

This paper reports on the fabrication and characterisation of a test chip incorporating the first MOS transistors with a gate produced using an organometallic material. The measured transistor characteristics are typical for those expected for a p-MOS device except for the subthreshold region and this effect is still being examined. The above transistors are the first reported devices to have been fabricated using a novel photosensitive organometallic material to deposit and pattern the gate using neither etching nor solvents. This new technology requires 50% less process steps than conventional gate

definition which is a key attribute from a manufacturing point of view. In addition, the organometallic material can be modified by replacing the Pt in the structure shown in Figure 1 with another metal (e.g. Au, Mo, Hf, Ta and W) making the technology flexible and potentially capable of replacing polysilicon based gate technology.

Now that it has been proved that the material can be integrated into a MOS technology, we are in the process of incorporating the organometallic into a standard CMOS process.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the help of L. J. Millar and G. Smith in preparing the organometallic materials.

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**D.3 IEEE Transactions on Semiconductor Manufacturing (vol. 17,
may 2004)**

Characterization of Platinum Films Produced by UV Exposure of a Novel Photosensitive Organometallic Material

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Abstract—A novel process is presented which produces platinum features using direct UV exposure of the photosensitive organometallic material $\text{cis}-(\text{C}_3\text{F}_7)_2\text{Pt}(\text{II})-\text{C}_8\text{H}_{12}$. The technique reduces the number of process steps involved when creating a metal pattern on a substrate by not requiring photoresist, solvents, or etch processes. In contrast to processes already reported in the literature, the method is compatible with microelectronic processes and does not require costly special equipment. Two test chips with MOS capacitors and resistive structures fabricated using the new organometallic material have been characterized. The results show that the deposited films are metallic and have a good adhesion to silicon dioxide. The work function of the platinum films is in agreement with the value found in the literature, but the measured resistivity and XPS indicate that the metal film contains some remaining organometallic residue after pattern development.

Index Terms—Metallization, organometallics, platinum, test structures, work function.

I. INTRODUCTION

As microelectronic device geometries reduce in size, there is a need for new materials and processes that meet the requirements and overcome the limitations of existing solutions. We have developed a photosensitive organometallic material [1] which can be exposed by UV light to produce patterned metal layers.

Organometallic materials are widely used in the repair of photolithography masks and integrated circuits. The method usually employed is focused ion-beam induced deposition of metals using an organometallic precursor gas, and a good review of this technique can be found in [2]. The deposition of platinum from an organometallic material was reported in the early 1990s [3]. Other research focused on the direct laser writing of a metal pattern by means of photothermal (pyrolytic) decomposition of a metal containing organic compound which can be either a solid [4]–[6] or in the liquid phase [7], [8]. Finer and more con-

trollable features can be realized by photochemical (photolytic) decomposition. This principle was applied to deposit and pattern metal by irradiation of an organometallic material through a photolithographic mask [9]–[11]. Some of these processes require the use of solvents in order to remove organic residue from the exposed film or an electroless metallization.

The technique used in this work employs photolytic decomposition of a solid organometallic material and conventional UV lithography in order to deposit a patterned metal layer on a substrate. The method offers advantages over the techniques mentioned above by being compatible with existing semiconductor technology and working without laser, ion-beam and electron-beam exposure tools, or liquid developers. The process does not require photoresist, solvents, or etch processes and allows a reduction of process steps when creating a metal pattern, a factor which is of great significance from the manufacturing viewpoint. A method commonly utilized in semiconductor manufacturing to produce metal features [Fig. 1(a)] involves the deposition of the metal followed by a layer of photoresist which is then exposed and developed. This mask is then used to etch the metal to create the required features. A similar type of procedure is employed in a damascene metallization process with the addition of a chemical mechanical polishing (CMP) step.

The organometallic material reported in this paper reduces the number of steps involved in patterning a metal layer [Fig. 1(b)]. First, an organometallic compound is deposited on the wafer and exposed to UV light which causes the platinum to dissociate. A final heat treatment removes any remaining unexposed organometallic material and residues and leaves behind the required metal pattern.

This paper presents details of the deposition and patterning process and reports on the characterization of the resulting metal.

II. MATERIALS AND METHODS

For the characterization of the platinum layers two test chips consisting of resistive and capacitive test structures have been manufactured using the fluoro platinum complex [1], $\text{cis}-(\text{C}_3\text{F}_7)_2\text{Pt}(\text{II})-\text{C}_8\text{H}_{12}$, whose chemical structure is shown in Fig. 2.

The first test chip (Fig. 3) incorporates capacitors for $C-V$ measurements as well as Greek crosses and bridge resistors. The capacitors have areas ranging from $1\text{--}7.5\text{ mm}^2$ and pos-

Manuscript received July 23, 2003; revised January 30, 2004.

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Digital Object Identifier 10.1109/TSM.2004.826965

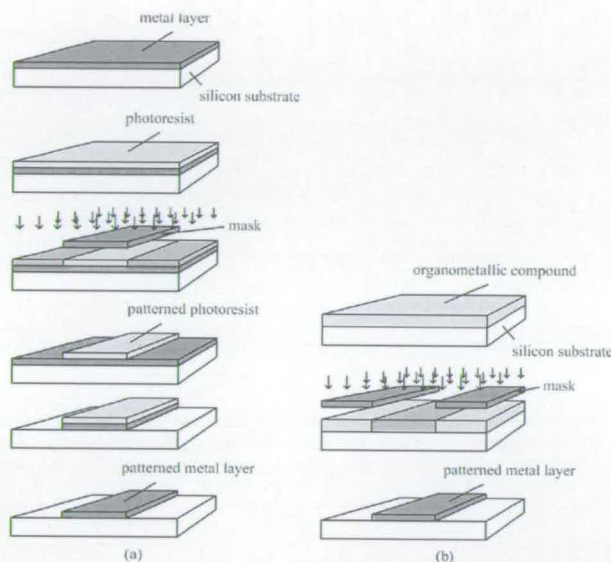


Fig. 1. (a) Conventional technique commonly used to deposit and pattern a metal layer and (b) deposition and patterning process of a metal layer using the organometallic process described in this paper.

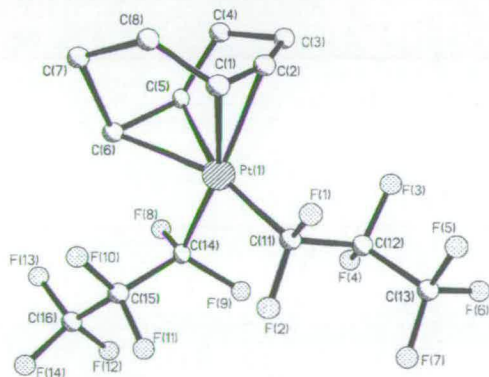


Fig. 2. Chemical structure of the organometallic compound.

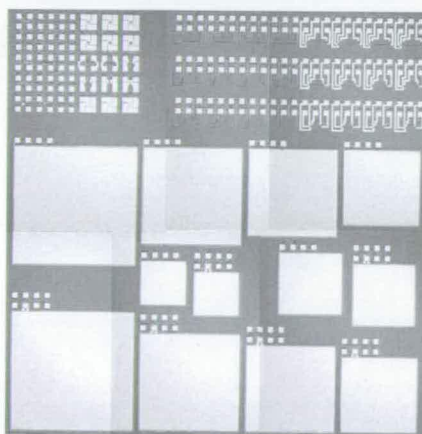


Fig. 3. Test chip produced for resistance and capacitance measurements.

sess guard rings to avoid errors due to condensation water on the surface of the wafer. The resistivity structures have track widths between 0.8 and 10 μm , thus allowing the same design to be used for further research on organometallic material with an improved resolution.

Standard processes have been employed for all but the metalization step during production of this test chip. A 500-nm oxide is grown on an n-type (100) silicon wafer with a resistivity of 2–4 $\Omega\cdot\text{cm}$. The back of the wafer is then heavily n-type doped to create a good ohmic contact to the aluminum which is deposited

later in the process. The masking oxide on the front is removed and the whole wafer then reoxidized to a thickness of 100 nm.

After this preparation, 100 mg of organometallic compound is evaporated onto the silicon dioxide using an Edwards Auto 306 Vacuum Coater. During the process some 9.25 mg of material is deposited which corresponds to a layer thickness of approximately 0.75 μm . The pattern is then contact printed using a 260-nm exposure tool with an output of 16.5 $\text{mW}\cdot\text{cm}^{-2}$. During

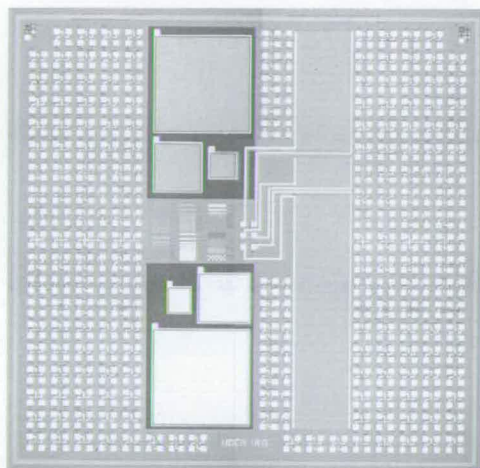


Fig. 4. Test chip containing bridge resistors for linewidth measurements.

the two-hour exposure, the metallic part of the organometallic material dissociates from the organic part, which is removed together with the unexposed compound using a three stage heat treatment, of which the first two are conducted at this point. For stage one, the wafer is furnace treated at a temperature of 70 °C for 6 h in air and during stage two at a temperature of 195 °C for 4 h in air. The oxide on the back of the wafer is then stripped off and an aluminum layer of 500 nm sputtered on the back of the wafer. The manufacturing is finalized with the last stage of the heat treatment which is also used to sinter the aluminum on the back of the wafer and is conducted in an atmosphere of 40% hydrogen in nitrogen at a temperature of 435 °C. The duration of this last annealing stage was thought to have a strong influence on the film composition and was varied between 2 and 6 h to study the influence of the time on flatband voltage and resistivity.

Silicon wafers with both platinum and aluminum structures were processed. The platinum structures were manufactured using the organometallic process described above, whereas the aluminum features were produced using sputtering and standard lithography. The processes used for both the wafers with the platinum and the aluminum pattern were kept as identical as possible to allow direct comparison of results gained from capacitance measurements.

The second test chip (Fig. 4) includes bridge resistors for measuring the width of metal tracks created using the organometallic compound. The chip incorporates other structures not used in this paper, and the process description only gives details about steps relevant for the production of the bridge resistors. The procedure is very similar to the one described earlier with the main differences being the use of a thicker oxide layer and the integration of aluminum for pads and interconnects. The oxide with a thickness of approximately 1.5- μm thickness was grown before the deposition of the

organometallic film. The third stage of the heat treatment is performed before deposition of the 0.5- μm sputtered aluminum layer and a 15-min sinter step is therefore included to complete the process.

III. RESULTS

Fig. 5(a) and (b) shows a Greek cross [12] and a bridge resistor, respectively, both of which have a designed track width of 10 μm and were produced using the organometallic process. A capacitor with an area of 1 mm^2 for C - V measurements and a bridge resistor for linewidth measurements are depicted in Fig. 5(c) and (d). Some of the pictures also show some residues in between the pattern. This is not observed in large open areas of the test pattern which indicates it might be caused by some sort of proximity effect. Later batches have not exhibited this problem and it is believed this may have been caused by issues associated with the preparation of the organometallic material. Fig. 6 shows examples of cross sections obtained from measurements on structures of different sizes after an annealing time of 6 h using a Dektak 8000 profilometer with a 2.5- μm tip. It is known that profilometers introduce errors if the features measured have dimensions similar to the tip size but calculations showed that in our case, the error should not exceed 1 μm . The measurements indicate that the dimensions of the features are generally larger than expected and the walls are nonperpendicular. The thickness of the measured platinum film varied between 30 and 50 nm over the whole wafer. This dependence of the film thickness on the location on the wafer is believed to be a result from a nonuniform evaporation process. The deposition of the film takes only a couple of seconds and due to the wafer rotating at an angle of 45° directly above the sample, a spatial variation of the film thickness is likely to occur. A Scotch tape test indicated that the film had a good adhesion to the substrate.

To check the integrity of the silicon dioxide layer, the leakage current was measured as a function of the applied voltage. The outcome of the measurements is shown in Fig. 7 and it can be observed that the leakage associated with the platinum and the aluminum capacitors is very similar.

Fig. 8 shows a typical C - V curve of a platinum capacitor measured at 1 MHz [13] using a HP4280A C - V meter. For comparison, a measurement of an aluminum capacitor fabricated in a similar manner to the platinum capacitor and a curve calculated using the theory described by Brews [14] are also shown. The measured samples were both annealed for 6 h and it can be seen that both curves follow the same trend. This, together with no difference being observed between the measured oxide leakage currents, indicates that the gate stack is potentially suitable for transistor operation.

Measurements of the flatband voltage after different annealing times showed that the flatband voltage moves toward lower values as time increases and seems to asymptotically approach a constant value [Fig. 9(a)]. The aluminum reference sample treated identically did not show this behavior. From the shift of the C - V curves of the platinum and the aluminum capacitors obtained after a 6-h anneal and the known work function of 4.1 V of aluminum [15], the work function of the

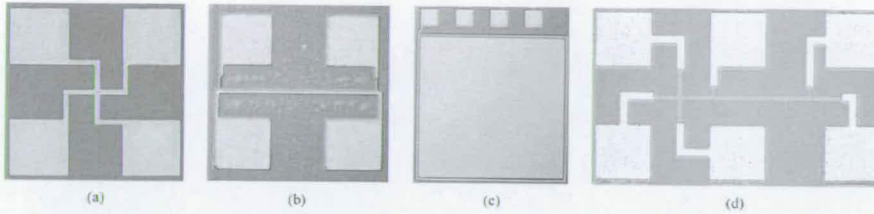


Fig. 5. Test structures produced using the organometallic process: (a) Greek cross test structure with an arm width of $10\ \mu\text{m}$, (b) bridge resistor with a track width of $10\ \mu\text{m}$ and a length of $350\ \mu\text{m}$, (c) platinum capacitor with an area of $1\ \text{mm}^2$, and (d) linewidth test structure with a width of $10\ \mu\text{m}$ and a length of $200\ \mu\text{m}$.

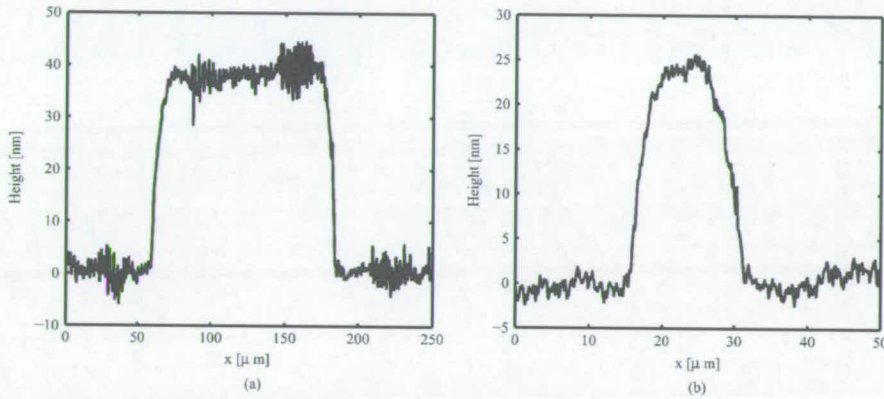


Fig. 6. Typical profiles of the deposited platinum films obtained using a profilometer: (a) pad with a width of $120\ \mu\text{m}$ and (b) scan over a $10\text{-}\mu\text{m}$ line.

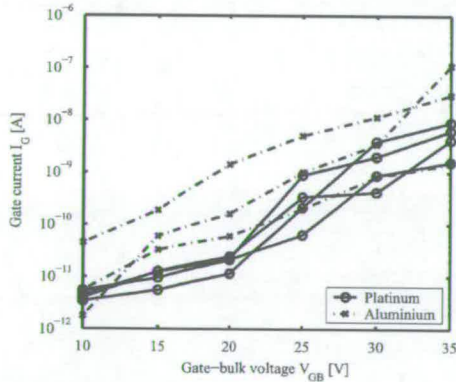


Fig. 7. I-V characteristic of the oxide measured using capacitors with an area of $4\ \text{mm}^2$ available on the second test chip.

platinum film was calculated to be $4.8\ \text{V}$, which is close to the value of $4.75\ \text{V}$ found in the literature [16].

The resistivity of the platinum films deposited by the organometallic process has been measured using both Greek

cross structures and bridge resistors. The sheet resistance decreased significantly with increasing annealing time and a trend toward an asymptotic value was observed [Fig. 9(b)].

Due to the sloping walls and the larger than designed linewidth values resulting from the heat treatment, the calculation of the resistivity requires account to be taken of the track width, height, and profile. It was observed that the resistivity values measured using the Greek cross structures were generally higher than the values from measurements of the bridge resistors. This seems to be caused by the profile of the tracks which affect the results differently for the two test structures. In order to get a reliable value for the resistivity, the cross-sectional area of a track was calculated using profiles measured at several positions on a bridge resistor and the outcome combined with the resistance. The resistivity of the films after a 6-h anneal was determined to be $4.58 \times 10^{-6}\ \Omega\cdot\text{m}$, which is significantly higher than the reported resistivity of $1.06 \times 10^{-7}\ \Omega\cdot\text{m}$ [17]. It is well known that thin films have higher resistivities than the bulk material but an increase as high as this has only been reported for film thicknesses below $5\ \text{nm}$ [18]. It is suspected that in this case organic residues may be responsible for some of the difference and this requires further investigations. Contaminants like carbon from the organometallic precursor gas are thought to be the cause of measured high resistivities of platinum films deposited using

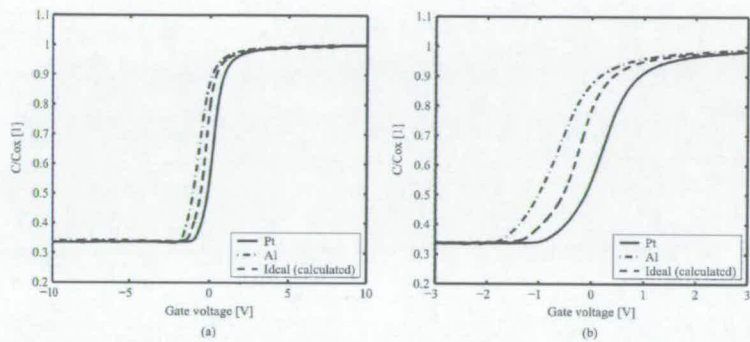


Fig. 8. Typical C-V curves obtained at 1 MHz of both a Pt (deposited using the organometallic process) and an Al (deposited by sputtering) capacitor on a n-type substrate. Calculated ideal curve with $V_{FB} = 0$ V is also shown for comparison. (a) Plot of the C-V curves over the whole measurement range. (b) Expanded middle portion of the curves shown in (a).

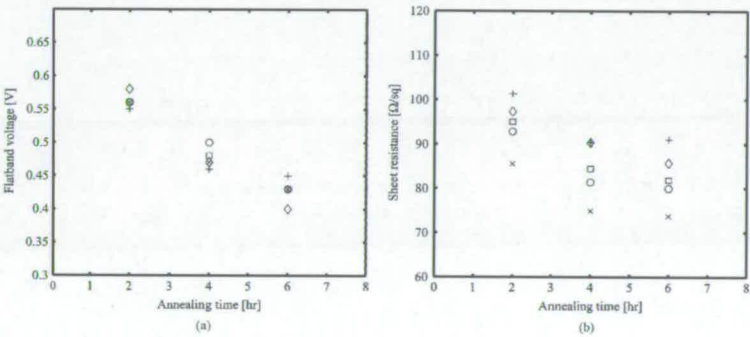


Fig. 9. Influence of annealing time on the flatband voltage and sheet resistance of the deposited films. Data were obtained from measurements at different locations on a wafer. (a) Flatband voltage versus annealing time. (b) Sheet resistance as a function of annealing time.

a focused ion beam (FIB) system [19] and X-ray photoelectron spectroscopy (XPS) measurements indicate carbon is also present in the Pt produced from UV exposure of our organometallic films.

Using the linewidth test structures [20] available on the second test chip, deposited platinum tracks of different widths were electrically characterized. The annealing time was 6 h. The results for linewidths of 3, 5, 10, and 20 μm are shown in Fig. 10 and deviations of up to 23% from the width on the photo mask were observed. The profilometer was again employed to mechanically measure the cross section of the tracks on the chip and Fig. 11 depicts the profiles obtained. The shape of the profiles agrees with those observed on the first test chip (Fig. 6), although the film thickness is significantly greater. Once again, the sidewalls are not perpendicular and the tracks are significantly wider than the ones on the photo mask. The lines on the chip are up to 50% broader at their half-height than on the mask and the percentage error decreases with increasing line width. These results suggest that the outcome of the measurement of the linewidth using bridge resistors

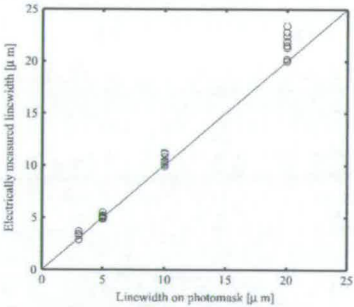


Fig. 10. Electrical linewidth measurements. Data points represent the results from different positions on the wafer.

depends on the profile and leads to a discrepancy between the electrically measured width and the mechanically acquired width of the line at its half-height.

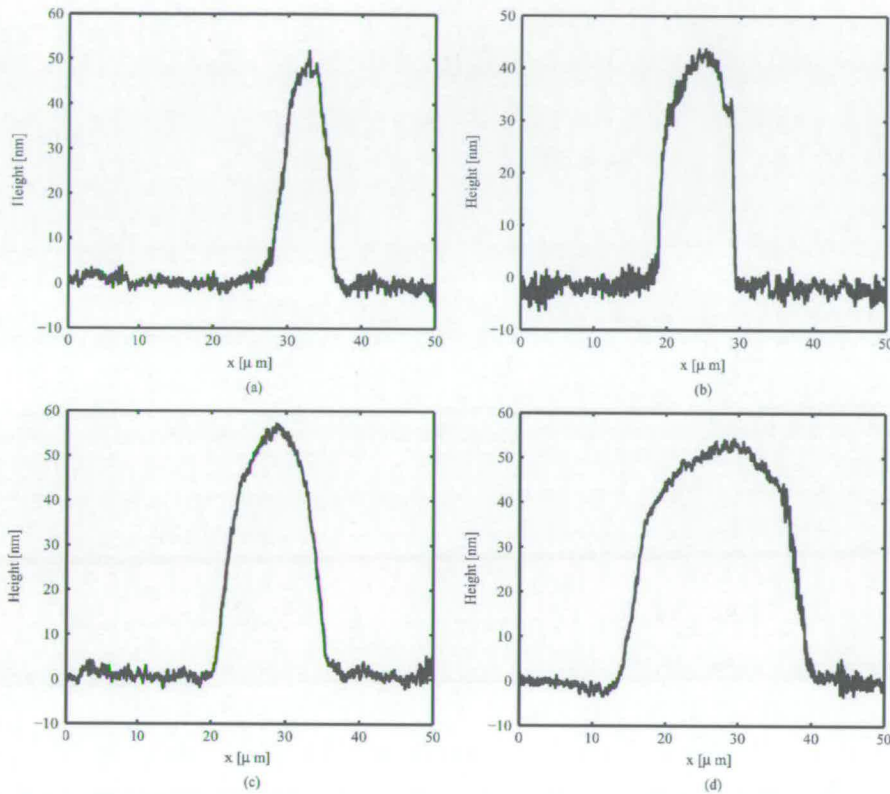


Fig. 11. Typical profiles of tracks with widths of (a) 3 μm , (b) 5 μm , (c) 10 μm , and (d) 20 μm obtained mechanically using a profilometer.

IV. CONCLUSION

This paper has demonstrated that metal features in the form of test structures can be produced using a novel organometallic film which is patterned directly with UV light followed by very simple low-temperature heat treatment steps. The measurements have shown that the deposited film is electrically conductive and the results from the capacitors show that it is suitable for use as a gate material for MOS transistors. However, the test patterns produced also indicate that the resolution of the deposited features is limited by the organometallic process. The exact cause for this cannot yet be attributed to either the exposure or the heat treatment. This lack of dimensional control does not meet the requirements for integration into a modern semiconductor process. Further optimization of both the material and process technology is being undertaken to overcome this issue as well as work to integrate the organometallic process into a process sequence to produce Pt gate MOS transistors. It should be noted that the chemistry used in this organometallic film is also capable of being adapted to produce gates made of metals such as Ag, Au, Mo, Hf, Ta, and W.

ACKNOWLEDGMENT

The authors would like to acknowledge the help of L. J. Millar and G. Smith in preparing the organometallic materials and thank A. M. Gundlach for his assistance in manufacturing the test structures.

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