Electrical Test Structures and Measurement Techniques for the Characterisation of Advanced Photomasks

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Abstract

Existing photomask metrology is struggling to keep pace with the rapid reduction of IC dimensions as traditional measurement techniques are being stretched to their limits. This thesis examines the use of on-mask probable electrical test structures and measurement techniques to meet this challenge and to accurately characterise the imaging capabilities of advanced binary and phase-shifting chrome-on-quartz photomasks. On-mask, electrical and optical linewidth measurement techniques have highlighted that the use of more than one measurement method, complementing each other, can prove valuable when characterising an advanced photomask process.

Industry standard optical metrology test patterns have been adapted for the direct electrical equivalent measurement and the structures used to characterise different feature arrangements fabricated on standard and advanced photomasks with proximity correction techniques. The electrical measurements were compared to measurements from an optical mask metrology and verification tool and a state-of-the-art CD-AFM system and the results have demonstrated the capability and strengths of the on-mask electrical measurement. For example, electrical and AFM measurements on submicron features agreed within 10nm of each other while optical measurements were offset by up to 90nm. Hence, electrical techniques can prove valuable in providing feedback to the large number of metrology tools already supporting photomask manufacture, which in turn will help to develop CD standards for maskmaking.

Electrical test structures have also been designed to enable the characterisation of optical proximity correction to characterise right angled corners in conducting tracks using a prototype design for both on-mask and wafer characterisation. Measurement results from the on-mask structures have shown that the electrical technique is sensitive enough to detect the effect of OPC on inner corners and to identify any defects in the fabricated features. For example less than 10Ω (5%) change in the expected resistance data trends indicated a deformed OPC feature. Results from on-wafer structures have shown that the correction technique has an impact on the final printed features and the measured resistance can be used to characterise the effects of different levels of correction. Overall the structures have shown their capability to characterise this type of optical proximity correction on both mask and wafer level.

Test structures have also been designed for the characterisation of the dimensional mismatch between closely spaced photomask features. A number of photomasks were fabricated with these structures and the results from electrical measurements have been analysed to obtain information about the capability of the mask making process. The electrical test structures have demonstrated the capability of measuring tool and process induced dimensional mismatches in the nanometer range on masks which would otherwise prove difficult with standard optical metrology techniques. For example, electrical measurements detected mismatches of less than 15nm on 500nm wide features.

Declaration of Originality

I hereby declare that the research recorded in this thesis and the thesis itself was composed and originated entirely by myself in the School of Engineering at The University of Edinburgh.

List your exceptions here and sign before your printed name.

Optical CD measurements with the MueTec <M5K> were made by Andrew Hourd at Compugraphics.

CD-AFM measurements with the Veeco SXM320 were performed by Ronald Dixson at NIST.

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In memory of my grandfather Aristoteles

Είς μνήμην του παππού μου Αριστοτέλη

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Acronyms and Abbreviations

AFM	Atomic Force Microscope
Alt-PSM	Alternating Aperture Phase-Shifting Mask
ARC	Anti-Reflective Coating
ArF	Argon Fluoride
Att-PSM	Attenuated Phase-Shifting Mask
BIM	Binary Intensity Mask
BJT	Bipolar Junction Transistor
BSE	Back Scattered Electrons
CAD	Computer Aided Design
CD-SEM	Critical Dimension Scanning Electron Microscope
CMOS	Complementary Metal Oxide Semiconductor
Cr	Chrome
CrON	Chromium Oxynitride
DC	Direct Current
DOF	Depth of Focus
DPT	Double Patterning
DUV	Deep Ultra Violet
ECD	Electrical Critical Dimension
FIB	Focused Ion Beam
FPP	Four Point Probe
GIMP	Gnu Image Manipulation Program
HP	Half-Pitch
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
KrF	Krypton Fluoride
LSR	Line to Space Ratio
LWR	Linewidth Roughness
MEEF	Mask Error Enhancement Factor
MG	Mentor Graphics

MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
NA	Numerical Aperture
NGL	Next Generation Lithography
NIST	National Institute of Standards and Technology
OAI	Off-Axis Illumination
OCD	Optical Critical Dimension
OPC	Optical Proximity Correction
OPE	Optical Proximity Effects
PEC	Proximity Effect Correction
PECVD	Plasma-Enhanced Chemical Vapor Deposition
POT	Progressional Offset Technique
PSM	Phase-Shifting Mask
RET	Resolution Enhancement Technique
RIE	Reactive Ion Etch
Rim-PSM	Rim Phase-Shifting Mask
SA-PSM	Subresolution-Assisted Phase-Shifting Mask
SCCDRM	Single Crystal Critical Dimension Reference Material
SE	Secondary Electrons
SMU	Source Monitor Unit
SPM	Scanning Probe Microscope
STM	Scanning Tunneling Microscope
Utt-PSM	Unattenuated Phase-Shifting Mask

Chapter 1
Introduction

1.1 Background

The invention of the point-contact transistor at the Bell Telephone Laboratories by Bardeen and Brattain in 1947 signalled the beginning of the revolution in microelectronics technology. Around the same time Shockley developed the theory behind the bipolar junction transistor (BJT) as part of an effort to replace vacuum tubes with solid states devices [1]. In 1951 the first bipolar transistor was fabricated and by 1954 it was an essential component of the telephone system. The first commercial device to make use of the transistor was a hearing aid and soon after the first transistor radio was put on the market. Although small in size and low in power consumption, transistors were not small enough for some applications which required whole miniaturised circuits. The drive for miniaturisation was the impetus for the work which led to the invention of the integrated circuit (IC).

The concept of the integrated circuit was first conceived by radar scientist Dummer in 1952, who was however unsuccessful in building such a circuit in 1956. The first integrated circuits were manufactured independently by two scientists who were unaware of each other's activities. Kilby of Texas Instruments filed a patent for a "Solid Circuit" made of germanium in 1959, however it was Noyce of Fairchild Semiconductor who was first awarded a patent for a more complex "unitary circuit" made of silicon in 1961 [2]. While Kilby's idea to make all circuit components out of the same semiconductor material was groundbreaking, Noyce's circuit solved several practical problems that Kilby's concept had, mainly the problem of interconnecting all the parts on the chip. This made ICs more suitable for mass production. The first integrated circuits were oscillators and simple digital flip-flops using a few active devices along with the passive elements. By 1971 IC technology had advanced to the stage that the first microprocessor, the 4-bit Intel 4004, was fabricated with 2300 transistors [3].

Over the last 50 years ICs have evolved in terms of complexity and thus are often

classified by the number of transistors they contain. The first integrated circuits, called Small Scale Integration (SSI), were developed in the 1960s and contained only a few transistors numbering in the tens. SSI circuits were crucial to early aerospace projects. The next step in the development of ICs took place in the late 1960s and introduced devices which contained hundreds of transistors. Medium Scale Integration (MSI) circuits were attractive economically, as their fabrication cost was little more than SSI devices, but allowed more complex systems to be produced. Economic factors led to further development and Large Scale Integration (LSI) in the mid 1970s, with tens of thousands of transistors per chip. In the early 1980s circuits with hundreds of thousands of transistors were manufactured and the term Very Large Scale Integration (VLSI) was introduced. To reflect further growth of complexity the term Ultra Large Scale Integration (ULSI) was proposed for chips with more than 1 million transistors.

The growth of complexity of integrated circuits has been following a trend called "Moore's Law" which was described by Moore of Intel in 1965 and predicted that the number of devices in an integrated circuit would double each year [4]. In 1975 Moore amended the law to state that the numbers of transistors in an IC would double every 18 months [5]. Although Moore's law was initially made in the form of an observation and prediction, as it became more widely accepted, the more it served as a goal for an entire industry. This prediction has been successfully followed for the last 40 years and on average, the numbers of transistors in a state-of-the-art chip has doubled every 18 months.

Since the late 1960s, when circuits had linewidths of 5μm, to now, where 65nm devices are in mass production, optical lithography has been a key technology for the advancement of IC fabrication and performance. Optical projection lithography is the process used to transfer the patterns that define integrated circuits through a mask onto semiconductor wafers. It is the first choice for mass production in the IC industry as no other technology has approached the same levels of cost-effectiveness and wafer throughput capability [6]. A lithographic system includes an exposure tool, masks, resist, and all of the processing steps required to accomplish pattern transfer.

Continued improvements have enabled the printing of ever finer features which in turn has allowed the industry to produce faster and more powerful semiconductor devices. The drive for smaller feature sizes has pushed optical lithography to its very limits. IBM

has recently fabricated distinct and uniformly spaced, high quality line patterns only 29.9nm wide [7] and this is one of the many examples of recent advances. This is less than half the size of the 65nm features now in mass production and below the 32nm that the industry consensus held as the limit for photolithography techniques.

The continuous increase in IC performance has been achieved by the introduction of reduced exposure wavelengths and modern resolution enhancement techniques (RETs), which allow the printing of features much smaller than the wavelength of the exposure light [8]. The resolution of a photolithographic system can be enhanced by methods such as off-axis illumination (OAI) [9], pupil filtering [10, 11] and as devices in the 45nm technology node move from development into production, techniques such as immersion lithography [12–14] and double patterning (DPT) [15] become essential.

Of significant importance is the manufacture of photomasks that are capable of perfectly replicating the artwork generated by the IC designer. To enable the latest technologies to be resolved on wafer, advances in photomask resolution enhancement technologies such as optical proximity correction (OPC) and the various types of phase-shifting masks (PSMs) [16, 17], have been introduced into mask making. In addition the manufacturing process has to result in zero defects and this is a significant challenge with tremendous pricing pressures. This is reflected in the cost of a set of leading-edge mask plates, which is now considerably more than $1M [18, 19]. Therefore, it comes as no surprise that the ability to accurately test and characterise advanced photomasks, for the purposes of process verification and control, is becoming increasingly important. The increases in complexity and cost have placed a premium on mask metrology, which now has to keep up with the strict requirements introduced by the IC industry.

Mask metrology is a challenging issue for the semiconductor industry and an absolute key if the industry is to successfully follow the requirements for future technologies, as charted by the International Technology Roadmap for Semiconductors (ITRS) [20]. It is an industrial process worth over $2.5B worldwide that underpins the >$200B integrated circuit industry, which is solely becoming an area of significant economic and social consequence.

Traditional methods for mask metrology and verification use optical [21, 22], critical dimension scanning electron microscopy (CD-SEM) [23–25] and atomic force

microscope (AFM) measurement systems [26–29]. The progress made in optics fabrication could not have been achieved with out access to appropriate metrology tools. However, in addition to the challenges involved in fabricating advanced masks, the manufacturers are now struggling to characterise them. The established techniques not only require expensive equipment well in the region of $1.5M, but as dimensions continue to rapidly reduce, they are being stretched to their limits and are unable to meet the requirements for accurate and repeatable results. Optical distortions can confound optical measurements, while charging on fused silica photomasks can adversely affect CD-SEM results. In addition, both of these techniques are effectively subjective and require careful calibration of the measurement tool for meaningful results. On the other hand a high resolution CD-AFM can be an excellent means for CD calibration but it suffers from low throughput which makes it unsuitable for a process inspection environment.

Much of the work in this thesis addresses the challenges involved with the measurement and characterisation of advanced photomasks. These challenges have provided the incentives for the development of alternative measurement approaches. The thesis investigates a novel application of electrical test structures and measurement techniques which are adapted for on-mask metrology. Test structures and measurements techniques were originally developed to characterise the IC manufacturing process and their integration onto advanced masks can take full advantage of the considerable developments of the last 30 years.

While enhancement techniques such as phase-shifting masks are essential to achieve the sub-wavelength dimensions required in advanced CMOS (Complementary Metal Oxide Semiconductor) technologies, approximately 85% [30–33] of all masks currently manufactured are binary and binary masks typically form up to 85-90% of the mask set used in an advanced process. Obviously the electrical measurement approach requires a conductive film such as the chrome used in standard binary photomasks or for example PSMs with the alternating design. The most commonly used form of phase-related, reticle enhancement technology used at present, the attenuated phase-shift [34], or chromeless type masks are not suitable for direct electrical probing. However, the process used to create these masks typically uses a chrome layer as a hard mask during patterning and etching of the phase-shifting features and it should be possible to

measure them before the chrome layer is removed. Therefore, the proposed electrical techniques are ideally suited for process control measurements on the most widely used photomask types.

A problem with the inclusion of electrical test structures is that they take up valuable space on a mask which could be occupied by the design of the product. For the purposes of photomask characterisation, the full area of a mask plate can be covered by test patterns, as the development engineers attempt to characterise the fabrication process. A major attraction to this is that similar structures can be printed and measured on-wafer using the same electrical techniques for the characterisation of the photolithographic process. However, in a mature/production process the photomask will include only the minimum number of structures required for the purposes of process verification. The test sites can be located outside the circuit area with the alignment marks, the maskmakers identification marks and other process control/inspection structures. One other issue associated with the adoption of electrical test structures for mask metrology is the perception that the photomask could be damaged during probing in the measurement. In comparison to aluminium, the chromium light blocking film on a standard photomask is extremely scratch resistant and robust, so the probe pads are left unmarked after probing. Delicate ICs on expensive wafers are routinely probe tested as a standard part of the IC manufacturing process and so there is little doubt that masks, which are much less susceptible to probe damage, can be characterised electrically without damage.

Electrical test structures are connected to the test equipment through metal probe pads (normally 80-120μm square) which are typically arranged in a $2\times N$ array where the pitch of the pads is twice their width. The probe pads can be contacted either with manual probe needles controlled by micro-manipulators or through a probe card. Probe cards are generally used with a probe station which can step the probe tips between test structures. This is integrated with computer controlled measurement equipment to create a complete test system.

Electrical dimensional metrology has the potential to meet the requirements set by the photomask industry whilst it remains a highly repeatable, fast, cost-effective and robust technique. The proposed technique not only can provide an alternative measurement approach, but will also act as a reference point with which to compare

traditional measurement methods. In addition, it can provide feedback to help create better calibrations for the large number of metrology tools already supporting photomask manufacture and underpin the requirements for developing CD standards for maskmaking. Finally, the same measurement techniques can be applied equally to on-mask and on-chip features, providing a transferable metrology from mask to wafer.

1.2 Thesis Structure

This section presents a description of the thesis structure and briefly outlines the contents of the chapters which follow.

Chapter 2: Background. The fundamentals of optical lithography and resolution enhancement techniques are presented. Special attention is being paid to the operating principles, the correction and enhancement procedures of photomasks. The measurement of sheet resistance and linewidth is described. Traditional linewidth measurement methods are presented, but the main focus is on electrical techniques. Examples from the literature of electrical test structures for the measurement of other important maskmaking parameters are examined.

Chapter 3: Linewidth Measurement Techniques for the Characterisation of Binary and Alternating Aperture Phase-Shifting Masks. This chapter briefly describes the earlier work done on electrical test structures for the measurement of photomasks. It then presents the on-mask structure design, fabrication and measurement results from electrical and optical techniques on binary and alternating aperture phase-shifting masks. The advantages and limitations of these mask characterisation techniques are shown.

Chapter 4: Development of Electrical On-Mask CD Test Structures Based On Optical Metrology Features. The first part of this chapter investigates the adaptation of standard optical metrology features to electrical equivalents. A prototype mask with the electrical designs is fabricated and the features are electrically and optically measured to investigate the fabrication process and compare the metrology techniques. The second part examines potential electrical on-mask test structures through 2-D and 3-D computer simulations for the characterisation of other important parameters.

Chapter 5: Comparison of Metrology Techniques for the Characterisation of Advanced Photomask Processes. The first section of this chapter describes the design and fabrication of binary on-mask test structures on a plate written using an e-beam proximity correction technique. Results from electrical and optical measurements made on the structures examine the effectiveness of the correction method and further evaluate the performance of the metrology techniques. The second section presents a comparison of CD-AFM measurements made with a state-of-the-art tool, fully calibrated to a reference standard, with electrical and optical metrology results. An analysis of the uncertainties involved in the different measurement techniques is also presented.

Chapter 6: Electrical Test Structures for the Characterisation of Optical Proximity Correction. This chapter begins by examining the use of an on-mask resistive test structure for the characterisation of a corner type of optical proximity correction, using simulations and measurements on a prototype photomask. The photomask is then used to print structures on wafer. Simulations and measurements at wafer level are also performed and a comparison between the two is presented.

Chapter 7: Matching Resistor Test Structures for the Characterisation of the Photomask Fabrication Process. This chapter presents the design and fabrication of electrical on-mask test structures for the characterisation of the dimensional mismatch between closely spaced photomask features. A number of photomasks were patterned with these structures and the results have been analysed to obtain information about the capability of the mask making process.

Chapter 8: Conclusions and Future Work. In this chapter the conclusions drawn from the work reported in the preceding chapters are reviewed. Suggestions for future work on the topics covered in this thesis are also made.

Chapter 2
Background

2.1 Optical Lithography Fundamentals

Optical lithography has been the key technology for semiconductor patterning since the early days of integrated circuit production. Although predictions of its demise have been made on many occasions, new techniques have pushed optical lithography beyond the generally accepted theoretical resolution limits. These enhancements have significantly extended the manufacturing capabilities of the IC industry. However, optical lithography does have real physical and economic barriers and an accurate estimation of these limitations is essential for extending its life and preparing for the transition to next generation lithography (NGL) techniques in the future.

Optical lithography is essentially a photographic process by which a light-sensitive polymer called photoresist is exposed through a master pattern called photomask and developed to form 2D patterns on a substrate [35]. A schematic of an optical projection tool where an image of the photomask is projected onto the substrate is presented in figure 2.1.

The resolution limit in optical lithography differs depending on the type of feature being printed. The two types of resolution that are used by the IC industry are the minimum printable pitch and feature size (see figure 2.2 [36]). Although related, they have different limits defined by the physics of lithography and different implications in terms of device performance [35]. Feature size resolution determines the characteristics and performance of a transistor. Pitch resolution (the smallest printable linewidth and spacewidth pair) determines how closely transistors can be packed in a chip.

The imaging performance of a photolithographic system is determined by the Rayleigh resolution criterion, developed more than 100 years ago by Lord Rayleigh to describe the diffraction limits of telescopes. It describes the ability of an imaging system to resolve two closely spaced objects and in optical lithography this essentially defines the

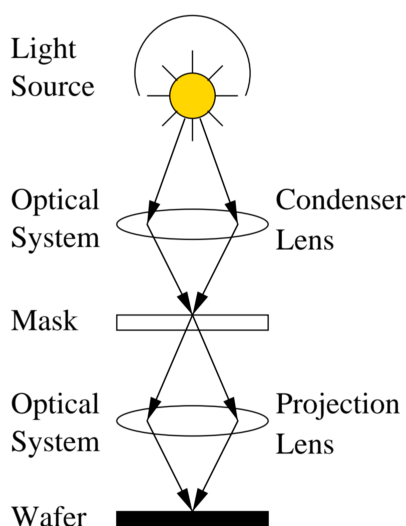


Figure 2.1: *Diagram of an optical projection lithography "stepper" tool used for exposing semiconductor wafers.*

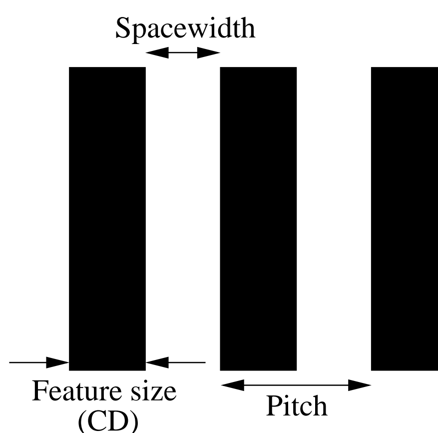


Figure 2.2: *Diagram of a line and space pattern.*

smallest printable half-pitch (HP). According to Rayleigh's criterion the resolution (*R*) of an optical projection lithography system can be obtained by

$$R = k_1 \frac{\lambda}{NA} \tag{2.1}$$

where (λ) is the wavelength of the imaging light and (NA) is the numerical aperture of the imagining lens system used in the lithographic process (NA = sinθ is the maximum diffraction angle that a projection lens can capture and use for image formation). The Rayleigh factor (k_1) is a constant which depends on the details of the imaging process, such as the configuration of the illumination system and the optical parameters of

the photoresist. Ultimately k_1 can be as low as 0.25 (the fundamental limit) but this requires tremendous effort and is not achievable with conventional lithography.

Equation 2.1 offers two physical quantities for the reduction of the printable half-pitch. This can be achieved by decreasing λ or increasing NA. As resolution is increased through the use of higher-NA tools and lower wavelengths, another limitation is presented with the reduction of the second fundamental lithography parameter. The depth of focus (DOF) is defined as the range of focus over which adequate feature fidelity is maintained within specifications (linewidth, sidewall angle, resist loss and exposure latitude). It is expressed by

$$DOF = k_2 \frac{\lambda}{NA^2} \tag{2.2}$$

where (k_2) is a constant which also depends on the lithographic process. A greater DOF indicates a more tolerant lithographic process, while a poor value of DOF will introduce the need for high process specifications such as tight wafer flatness and highly uniform resist thickness.

2.2 Photomask Basics

Although photomasks have always been an integral component in the photolithographic process of semiconductor manufacturing, they are now more than a stencil that maps the design of an IC for projecting onto wafers. Driven by the demand for faster and cheaper devices, photomasks are rendered as a critical and enabling technology in optical lithography. Photomasks which are at the forefront of miniaturisation require complex mathematical algorithms to design and sophisticated manufacturing techniques [37].

A photomask is usually a transparent high purity quartz (fused silica - SiO_2) or glass substrate containing precision images of ICs, defined through a light absorbing chrome (Cr) layer covering one side of the mask. The chrome is covered with an anti-reflective coating (ARC)[1] and a photosensitive resist. The complete layout of an unprocessed mask can be seen in figure 2.3. The optical ARC applied to a photomask, alters the

[1] A common ARC material used on chrome photomasks is chromium oxynitride (CrON)

refractive index in to order to minimise reflections of specific wavelengths of light, but also acts as a protection to the chrome layer. The photoresist layer is a light sensitive material used in a mask making process, to form a temporary patterned coating on the mask surface.

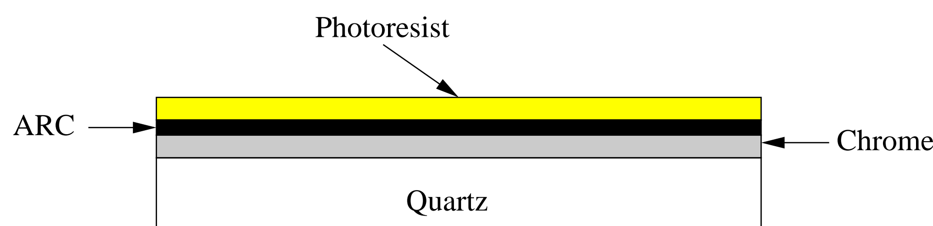


Figure 2.3: *Layout on an unprocessed photomask (also known as a blank).*

The current generation of semiconductors has 30 or more layers, each requiring a unique photomask. In a mass production environment the image of the mask is projected several times side by side on the wafer surface. This is achieved by steppers with reduction optics and the masks used for such process are known as reticles.

There are a number of process steps involved with the production of a photomask. Firstly the electronic data of the IC design is formatted for the lithography tool. This includes translating the data in a language the write tool can understand (fracturing) and making a jobdeck (the instructions for placing all patterns on the mask). Binary intensity masks (BIMs) are the most common type of photomasks produced (85% of total masks currently produced are binary) [30–33]. The fabrication process of a binary mask is presented below.

1. The pattern is generated on the plate by exposing the resist with an electron beam or laser tool (see figure 2.4(a)). This alters the chemical composition of the resist in the exposed areas (a MEBES 5500 e-beam writer was used for this work).

2. The exposed resist is removed to develop a temporary pattern to serve as a mask for etching (see figure 2.4(b)).

3. A permanent pattern is defined in chrome by etching the ARC and chrome, wherever the resist has been removed (see figure 2.4(c)). The areas where the chrome and ARC have been removed are referred to as clear (or glass), while areas where the chrome and ARC have remained, are referred as dark (or chrome).

4. The temporary masking layer is then removed by stripping all the remaining resist from the mask (see figure 2.4(d)).

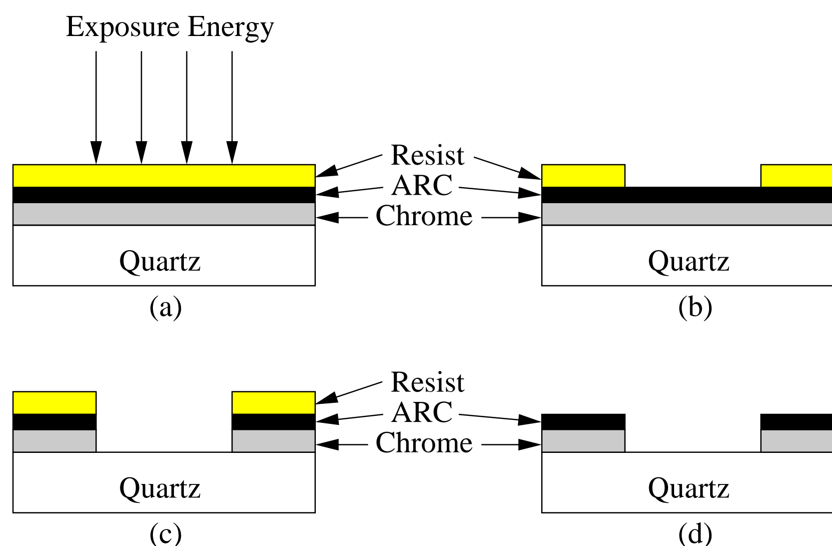


Figure 2.4: *Fabrication process steps for a binary photomask (a) Pattern generation (b) Photoresist development (c) Chrome etch (d) Photoresist strip.*

A complete industrial fabrication process will also include steps for critical dimension (CD) measurements, surface clean, defect inspection, repair and pellicle application. A pellicle is a dust proof membrane applied to protect the mask surface from contamination.

2.3 Improving Resolution in Optical Lithography

Assuming that Moore's law continues to hold into the future and is financially justifiable, optical lithography will be pushed to its very limits. As lithography gets harder and is expected that there will be no revolution that can change this, it is now more important than ever to predict its limitations. This can be achieved by examining the resolution drivers which effectively also set the practical limits, for optical lithography. This section introduces the methods used by the lithography industry to improve resolution. The progress made so far and the limits for each method are presented. Particular attention is being paid to the techniques involved with the advancement of photomasks. These are presented in detail, as they have to be fully understood before characterising an advanced photomask.

2.3.1 Introduction

Two approaches offering resolution improvement (pitch and feature) can be identified from Rayleigh's criterion. The first involves reducing the exposure wavelength. Since the 1970's the industry has been steadily changing to shorter wavelengths of light, however each change has progressively become more expensive and the light source more complex. Initially the light source was a mercury lamp filtered for g- (436nm) and h-lines (405nm). The wavelength has further decreased in 1984 to 365 nm (i-line of mercury), to 248nm in 1989 (KrF laser) and from 1999 onwards to 193nm (ArF excimer laser). Reducing the wavelength is desirable, however it is practically limited by the ability to engineer materials with the required optical properties, but mostly by the initial lack of maturity of the photoresist [36]. In addition only few light sources can deliver adequate power to expose wafers at cost-effective throughput rates. It is quite likely that 193nm will be the last mainstream wavelength in lithography, as the transition to 157nm (F_2 laser) has been abandoned for other methods of resolution enhancement. A reason for this is that the atmosphere attenuates light significantly at wavelengths below 193nm, requiring an oxygen and water free environment.

In addition, Rayleigh's criterion offers resolution improvement by increasing the numerical aperture of the imaging lens. As NA is the sine of an angle, its physical limit for exposure systems using air as a medium between the lens and the wafer, is 1. At this point the imaging system captures light rays propagating in all directions. However its practical limit is around 0.9 as the cost to benefit trade-off for higher values is not very promising. Although increasing NA improves resolution it adversely impacts the depth of focus. Despite this optical designers have been vigorously developing systems with higher numerical apertures and from a typical value of 0.4 in the mid 1980s conventional (dry) scanners have now reached NAs higher than 0.9. Recently immersion lithography [12–14] has enabled numerical apertures higher than 1. Immersion fluids will push the theoretical limits of the highest possible NA to that of the refractive index value (e.g. 1.44 for pure water), but will also slow down the exponential rise in cost and complexity that comes with approaching the current physical limits of NA [36]. In addition with the use of immersion lithography comes an improvement in DOF of at least the immersion index.

2.3.2 Binary and Phase-Shifting Masks

Phase-shifting masks (PSMs) take advantage of the interference effect in a coherent (or partially coherent) imaging system, to reduce the spatial frequency and enhance the edge contrast of an object [17]. This improves the resolution of the system without loss of DOF.

The phase-shifting elements are created by changing the thickness of the mask substrate. This can be seen in figure 2.5 [17] and is accomplished either by adding an extra layer of transmissive material on the mask, or by etching the mask substrate. As the light propagates through the mask substrate and the phase-shifting layer, its wavelength is reduced (from that in air) by the refractive index of the substrate and the PS layer. The difference between the optical path with the phase-shifting layer and the path without it is (n - 1) $\times$ d , where (n) is the refractive index of the extra layer (or substrate material) and (d) is the layer thickness or the etch depth. The phase difference (θ) is calculated using

$$\theta = 2\pi \frac{d}{\lambda}(n-1) \tag{2.3}$$

where (λ) is the wavelength of the light. Normally a phase difference of 180° is desirable. The layer thickness or etch depth required to give 180° phase shift is calculated by

$$d = \frac{\lambda}{2(n-1)} \tag{2.4}$$

To illustrate the improvement in resolution with a PSM scheme figure 2.6 [16] compares the imaging process for a binary and an alternating aperture phase-shifting mask (Alt-PSM). The alternating aperture phase-shifting mask design was first introduced by Levenson et al. [16] and is characterised by phase-shifting every other element in a close packed array.

For a binary mask the (normalized) amplitude of the electric field (E-field) at the mask is either +1 or 0. When light passes through two adjacent apertures it spreads due to diffraction. The E-field amplitudes at the wafer overlap and interfere constructively. The light-intensity (which is proportional to the square of the electric field amplitude) is high everywhere, therefore blurring individual features together.

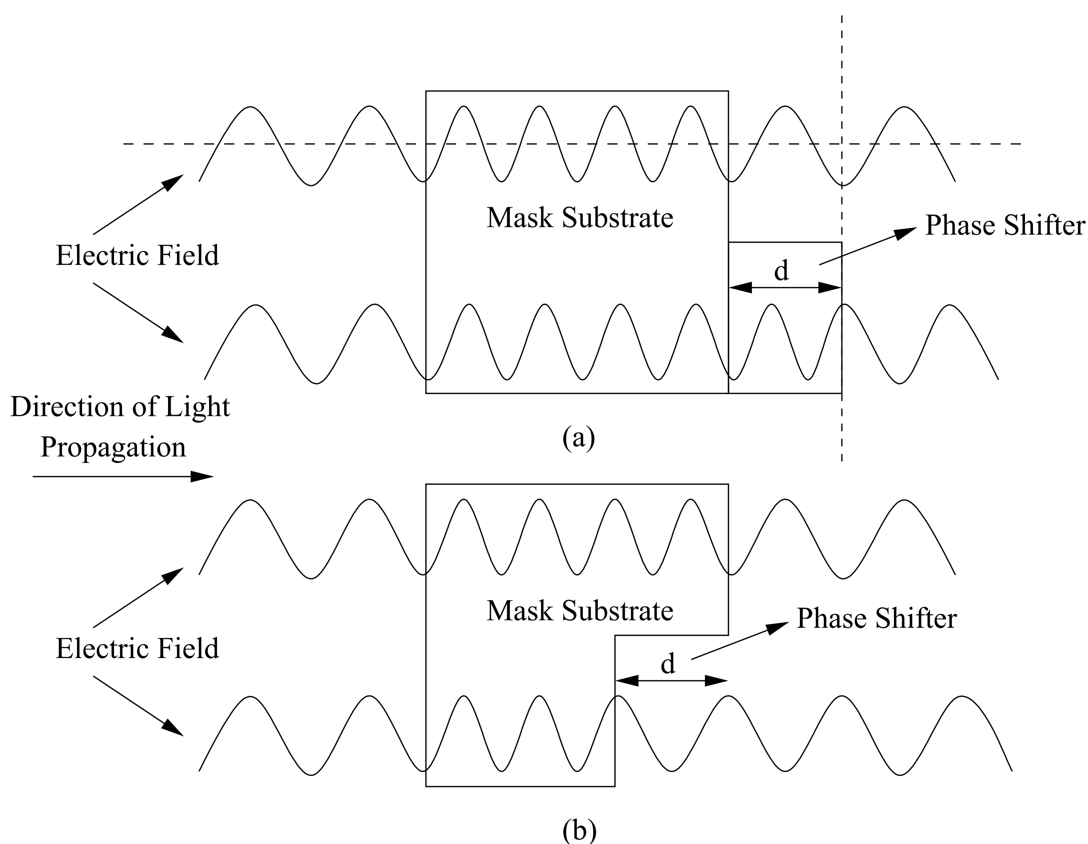


Figure 2.5: *A phase-shifting layer which is created either by (a) adding an extra layer of transmissive material or by (b) etching the mask substrate introduces a difference of $\lambda / 2$ (in this case) in the optical path.*

For an Alt-PSM the electric field amplitude is -1 for features with a phase-shift and +1 for features with no phase-shift. Again light passing through each aperture spreads and because one component is phase-shifted, there is destructive interference between the electric-field amplitudes. Hence the net amplitude of the imaging light between adjacent apertures becomes zero (or dark). This minimises the intensity in this region and therefore resolution of these features is enhanced.

There are many approaches for introducing the phase-shifting elements to the mask pattern, each with different configurations and working principles [38]. Subresolution-assisted phase-shifting masks (SA-PSM) provide phase-shifting to circuit layouts with isolated openings, such as holes which are far from adjacent patterns. Rim phase-shifting masks (Rim-PSM) can be used for an arbitrary mask layout and unlike the PS schemes presented so far can provide phase-shifting for opaque patterns. Attenuated phase-shifting masks (Att-PSM) can also be applied to an arbitrary layout

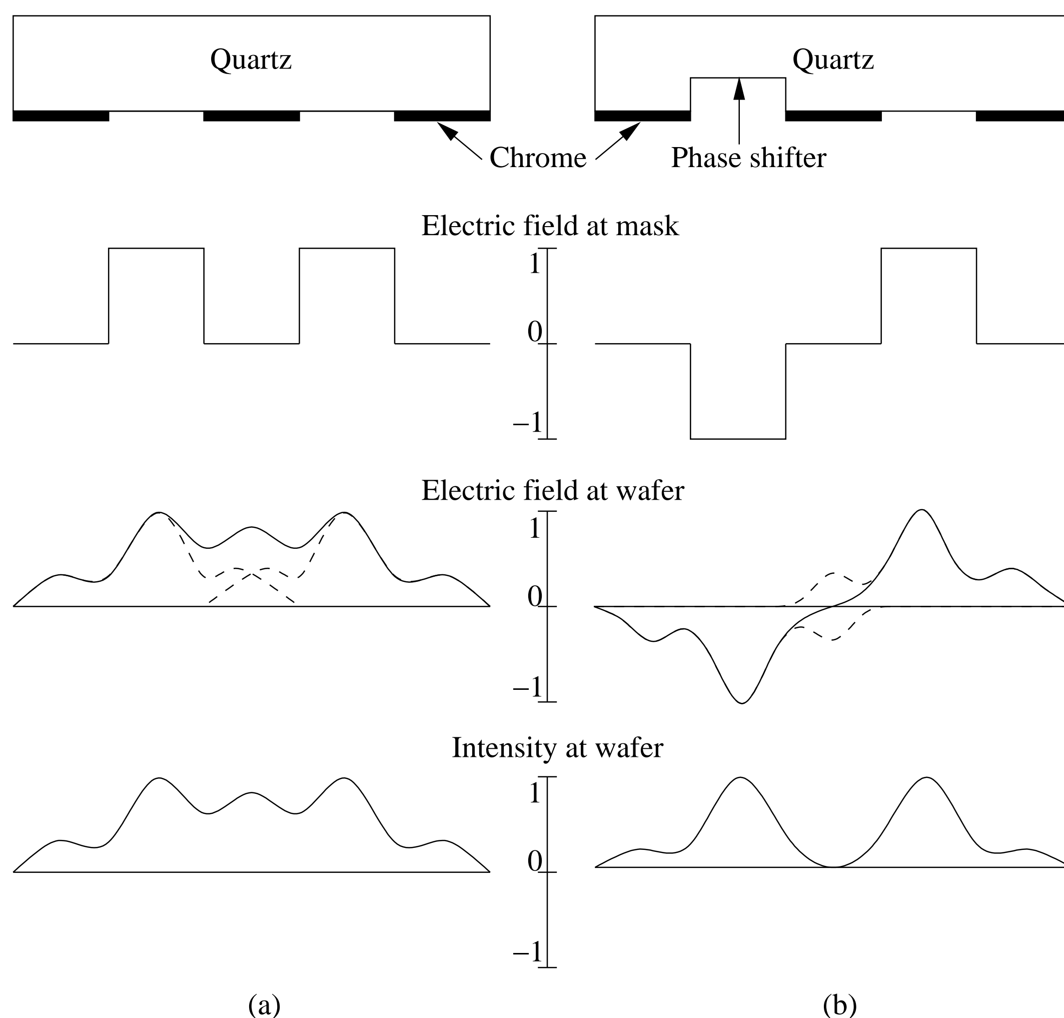


Figure 2.6: *Comparison of imaging process for (a) a conventional binary mask and (b) an alternating aperture phase-shifting mask.*

and can be implemented for transmissive or reflective materials. Unattenuated phase-shifting masks (Utt-PSM) use transparent phase-shifters and can improve the optical image without the use of a mask absorber.

2.3.3 Proximity Correction Techniques

Proximity effects are variations in width or shape of a printed feature due to the proximity of nearby features. Proximity effects were first observed with electron beam lithography, where it was found that the dose that a feature receives is affected by backscattered electrons from nearby features [39]. An example of the proximity effect is the iso-dense bias. This is the difference in printed linewidth between isolated

and dense line patterns and is a feature size dependent effect. Proximity effects also manifest as deformations of the fabricated features compared to their designed pattern. These may arise in the form of corner rounding and line-end shortening.

One of the major RETs, optical proximity correction, is applied to a photomask in order to compensate for the distorting optical effects introduced by the exposure pattern environment and density. OPC was first considered for microlithography with imaging systems in the early 1980's [40], although it was not until the 1990's that commercial application of this technique for chip fabrication became available [41]. Throughout the development of OPC, its primary purpose has been to correct the shape printed upon the wafer to replicate the original mask feature design as closely as possible. This requires very well-defined corrections to pattern feature sizes and/or the addition of sub-resolution assist features to homogenise the aerial image density of the exposed field [42, 43]. In order to build the correction models for application of OPC, as well as to verify the corrected pattern, it is vital to know exactly what is being rendered on the mask by the image generation process. However, mask pattern density also affects the way the mask image is created and effects such as etch micro-loading and mask writer proximity effects will alter the nominal linewidth. This must be considered prior to applying any OPC to correct for the optical transfer process. In addition to biasing of CDs to correct for local pattern density, OPC is also used to alter the mask pattern at corners and line ends. For two dimensional corners, complex structures are used, incorporating either additive or subtractive OPC serif-type features to produce the desired shape. Figure 2.7 shows an example of a simple design with no correction and the corresponding design after a set of OPC rules has been applied [35].

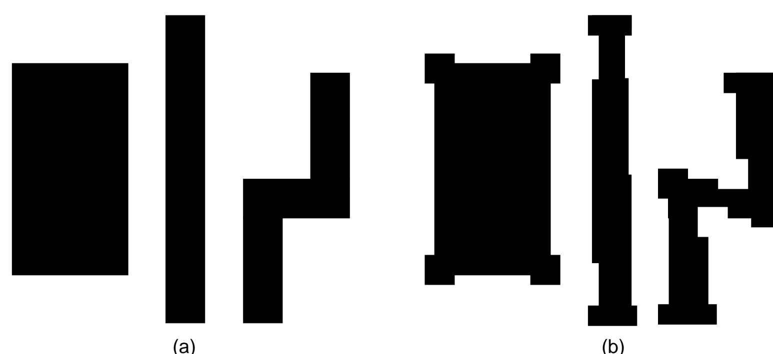


Figure 2.7: *Section of design (a) with no OPC (b) with OPC.*

All this has resulted in OPC application and verification being performed using

increasingly complicated optical models [44]. In addition, the shapes appearing on masks are becoming more and more abstract when compared to the final desired pattern. This has resulted in masks being drawn on small grid sizes, requiring high overhead in data handling, long write times, difficult inspections, and increasingly high prices. Throughout the progression of OPC technology, uncertainty has remained regarding how close to the originally drawn shape the printed features must be to enable the circuit to function correctly. While this is likely to vary from one circuit to another, if the specific circuit functionality can be maintained while the pattern on the wafer is not ideal, then there is the potential to reduce mask costs significantly.

E-beam lithography is very common technique of mask patterning and a number of different schemes have been devised to minimise proximity effects [45]. Multilayer resists reduce the proximity effect, at the cost of an increase in process complexity. One common correction technique is dose modulation, where each point in a pattern is assigned a dose parameter such as the pattern shape prints at its correct size. Unfortunately, the calculations needed to evaluate the dose corrections, can be computationally very time consuming. A similar technique to dose modulation is pattern biasing. In this approach, the size of the dense patterns is reduced to compensate for the extra dose they receive. Another technique for proximity correction, GHOST [46], works by equalising the background dose caused by electron scattering in a pattern.

2.3.4 Other Resolution Enhancement Techniques

Other techniques have been introduced to push optical lithography even further and although they are not involved with enhancements applied on photomasks, it is useful to have a complete picture of all major technologies which have extended the useful life of optical lithography.

The third major RET that reduces k_1 to improve resolution, is off-axis illumination [9, 47, 48]. The concept of OAI was introduced in 1991 and is now a widespread technology in the IC industry [49, 50]. Its low added cost has allowed all modern scanners to be equipped with illuminators allowing several types of off-axis illumination. The OAI approach changes the angle at which light passes through the mask by inserting special holographic elements into the illumination

system. These elements shape the light in to a particular geometric pattern that significantly reduces the on-axis component of the illumination (the light striking the mask at near normal incidence). By tilting the illumination away from normal incidence, the diffraction pattern of the mask is shifted within the objective lens.

Typical illumination shapes are shown in figure 2.8 [35]. The quadruple shape offers illumination with four main incident angles and provides strong resolution enhancement and DOF increase. However its image performance is pattern dependent and although it works well with densely packed features, it has limited applicability on isolated features. The annular shape overcomes this limitation as it has a less pattern dependent image performance, however it is also far less powerful.

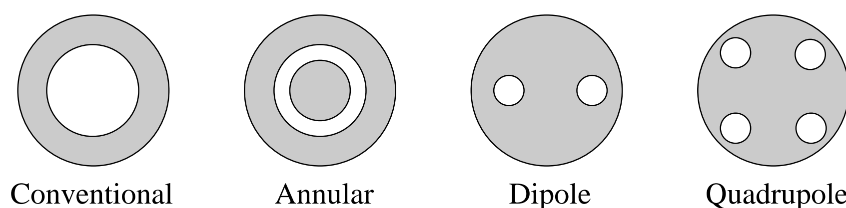


Figure 2.8: *Examples of light source shapes for the off-axis illumination technique. Note that the grey areas are opaque and the white areas are transparent.*

2.4 Photomask Metrology and Requirements

Many of the issues challenging on-wafer dimensional metrology are usually reduced by a factor of 4 or 5 with on-mask metrology. However, this is rapidly changing and in particular where advanced masks are used for the latest circuit generations. Smaller photomask feature sizes, highly dense patterns, and resolution enhancements such as phase-shifting and OPC technologies, are challenging to traditional mask metrology techniques. Photomask metrology must now be examined in the context of design, specification, manufacture, and application [51]. The drive towards reducing critical dimensions requires that the maskmaking industry produces high quality photomasks. To do so, the maskmakers have to fully understand the photomask process. Therefore, the goal of metrology is not only to accurately measure a feature, but to accurately describe and quantify it. Measurements are required for each process step of the photomask and the total number of measurements that is needed to understand the effects of the photomask fabrication process is large [52].

In the manufacturing environment, the most pervasive tools for mask metrology are optical and scanning electron microscopes. Atomic force microscopes and other profiling technologies typically function as reference metrology tools. Inter-method comparisons and cross-method calibrations do involve significant challenges. In addition to the inherent uncertainties of each measurement, care must be taken to understand the implicit measurement definitions of each method in order to compare equivalent quantities [29]. Electrical measurement methods on photomask features can prove valuable, providing reference metrology to traditional techniques which continue to be challenged. Performance and repeatability of a metrology tool remain the most critical factors to maskmakers. However, as the quantity of measurements required to characterise an advanced mask continues to grow, throughput and cost effectiveness of a tool become important [22].

The next part of this chapter presents the operating principles of electrical and traditional critical dimension measurement techniques. Examples of test structures from the literature, which can be adapted for photomask metrology are also reviewed.

2.5 Sheet Resistance Measurement

2.5.1 Resistivity

Resistivity (ρ) is a fundamental physical parameter for any conductor or semiconductor material, which describes how well a material inhibits current flow. It is expressed in units of ohm-meter (Ω-m). Figure 2.9 shows a bar of conducting material with uniform resistivity. The resistance (R) between two electrodes can be expressed as

$$R = \frac{\rho l}{wd} \tag{2.5}$$

where (l) is the length of the conducting bar, (w) is the width, (d) is the thickness and (ρ) is the resistivity of the conducting material.

The four-point probe (FPP) technique [53] is one of the most common methods used to measure resistivity. It was originally proposed by Wenner [54] in 1916 to measure the earth's resistivity. It involves bringing four electrically conducting pins in contact with the surface of the material being measured. The probe tips are generally arranged

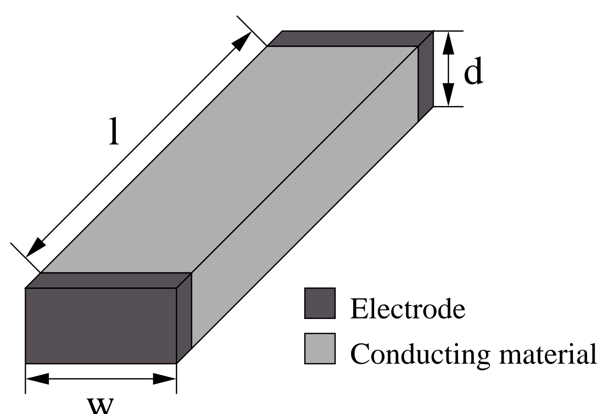


Figure 2.9: *Diagram demonstrating the dimensions of a bar of conducting material.*

in-line with equal probe spacing (s) (i.e. collinear) and such an arrangement is shown in figure 2.10. However other configurations are possible.

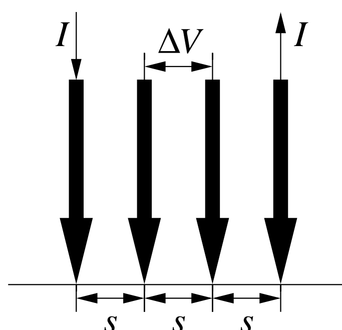


Figure 2.10: *Setup of four-point probe measurement technique.*

A current (I) is forced between the two outer probes and the potential difference (ΔV) between the two inner probes is measured. If the length, width and thickness of the sample being measured, are much greater than the probe spacing, then the resistivity of the semi-infinite sample can be calculated by [55]

$$\rho = 2\pi s \left(\frac{\Delta V}{I} \right) \tag{2.6}$$

This technique however is most commonly used to measure samples which are not semi-infinite (e.g. semiconductor wafers). Therefore, for finite geometries equation 2.6 must be corrected by adding a correction factor (F) that depends on the sample geometry. F is usually a product of several independent correction factors, which correct for probe placement near sample edges, sample thickness, diameter and temperature [53, 56, 57].

2.5.2 Sheet Resistance

In microelectronics, the FPP technique would normally be used for the characterisation of a conducting material whose thickness (t) is significantly smaller than the spacing between the measurement probes ($t \ll s$). A quartz mask coated with a thin chrome layer, or a wafer coated with a thin film of aluminium are such examples and in this case the equation for resistivity becomes

$$\rho = \frac{\pi t}{\ln 2} \frac{\Delta V}{I} \tag{2.7}$$

Measuring the thickness of thin conducting films can be difficult, therefore they are often characterised by their sheet resistance (R_S), which represents the resistance of a square area of the film. It is expressed in units of ohms per square ($\Omega/\square$) and can be calculated from the FPP measurement as

$$R_S = \frac{\rho}{t} = \frac{\pi}{\ln{(2)}} \frac{\Delta V}{I} \tag{2.8}$$

For a non semi-infinite sample the equation for the sheet resistance is given by

$$R_S = k \frac{\Delta V}{I} \tag{2.9}$$

where k is a correction factor which depends on the shape of the sample and the position of the measurement probes [57].

FPP measurements are typically useful with large uniform samples where the correction factors are known for each measurement and large non-patterned areas are available. This may be undesirable in a microfabrication process, however reference [58] demonstrates that it is possible to extract the sheet resistance from a small area of silicon film, by reconciling electrical measurements with results of computer simulations on similar geometries.

2.5.3 Van der Pauw Structure

When a thin conducting sample is too small to be measured with the FPP method, its sheet resistance can be extracted with a four-terminal van der Pauw test structure.

Van der Pauw developed a technique for measuring the resistivity of a thin film sample with arbitrary shape [59, 60]. The method requires that the following conditions are satisfied:

- The contacts are at the circumference of the sample and sufficiently small, tending towards point contacts.
- The sample material is homogeneous in thickness and resistivity, with a singly connected surface (i.e. does not contain any isolated holes).

For a flat sample of conducting material with successive contacts A, B, C and D as illustrated in figure 2.11, the resistance $R_{(AB,CD)}$ is defined as

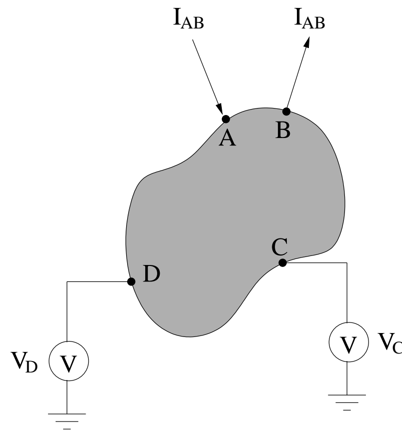


Figure 2.11: *Van der Pauw test structure of arbitrary shape and contact location, used to measure the resistivity.*

$$R_{(AB,CD)} = \frac{V_D - V_C}{I_{AB}} \tag{2.10}$$

That is the potential difference between D and C per unit current forced from A to B. If $R_{(BC,DA)}$ is defined similarly then the general van der Pauw formula

$$\exp\left(-R_{(AB,CD)}\frac{\pi t}{\rho}\right) + \exp\left(-R_{(BC,DA)}\frac{\pi t}{\rho}\right) = 1 \tag{2.11}$$

can be solved numerically to find ρ. If the sample has a 90° symmetry and the contacts are equally spaced around its circumference, then $R_{(AB,CD)} = R_{(BC,DA)}$ and equation (2.11) becomes

$$\rho = \frac{\pi t}{\ln(2)} R_{(AB,CD)} \tag{2.12}$$

Using equation (2.12) the general van der Pauw formula (2.11) can be rewritten to

$$\rho = \frac{\pi t}{\ln(2)} \frac{R_{(AB,CD)} + R_{(BC,DA)}}{2} f \tag{2.13}$$

where (f) is a correction factor which is a function of the ratio $r = R_{(AB,CD)} / R_{(BC,DA)}$ and satisfies the relation

$$\cosh\left(\frac{r-1}{r+1}\frac{\ln(2)}{f}\right) = \frac{1}{2}\exp\left(\frac{\ln(2)}{f}\right) \tag{2.14}$$

One of the main sources of error introduced on the measurements of van der Pauw structures, is when the contacts are of finite size and not at the circumference of the sample. However, van der Pauw found that a “clover shaped” sample could significantly reduce the influence of the contacts.

2.5.4 Greek Cross Structure

The measurement techniques and structures described so far were developed for resistivity measurements on large discrete samples of semiconductor material. The next step on this field were structures, which are easy to layout and define photolithographically, and on the the same scale as microelectronic devices, in order to measure the sheet resistance of thin films or diffused layers. The Greek cross sheet resistor [61–63] shown in figure (2.12) is a refinement of the four-terminal van der Pauw test structure. The sheet resistance is extracted at the heart of the cross and an accuracy of better than 0.1% can be achieved in practise [64]. The assumptions made by the van der Pauw method also apply for the Greek cross. However, the current forced and the voltage measured are not at an infinitesimally small point. This is not a problem provided that length of the arm (L) is greater than or equal to twice the arm width (W), in which case the sheet resistance error will be less than 1% [61, 65, 66].

For an ideal structure a single resistance measurement would be sufficient in order to

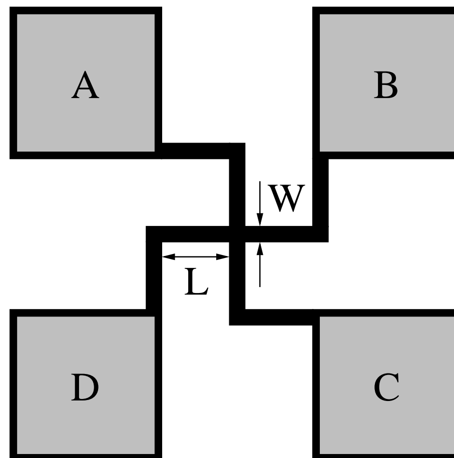


Figure 2.12: *Layout of four terminal Greek cross sheet resistance test structure.*

extract the sheet resistance, however in practise four measurements are required. Two are measured at a static, "zero-degree" (0°) orientation

$$R_0(+I) = \frac{V_D - V_C}{I_{AB}} \tag{2.15}$$

$$R_0(-I) = \frac{V_C - V_D}{I_{BA}} \tag{2.16}$$

and two at a "ninety-degree" (90°) orientation

$$R_{90}(+I) = \frac{V_C - V_B}{I_{DA}} \tag{2.17}$$

$$R_{90}(-I) = \frac{V_B - V_C}{I_{AD}} \tag{2.18}$$

The four measurement results are averaged to give a single resistance value

$$R(\pm I) = \frac{R_0(\pm I) + R_{90}(\pm I)}{2} \tag{2.19}$$

which is used to calculate the sheet resistance with

$$R_S = f\left(\frac{\pi R(\pm I)}{\ln(2)}\right) \tag{2.20}$$

The correction factor (*f*) which accounts for asymmetry in the structure is calculated using equation (2.14) where

$$r = \frac{R_0(+I) + R_0(-I)}{R_{90}(+I) + R_{90}(-I)} \tag{2.21}$$

The asymmetry of a structure is quantified in reference [62] through the asymmetry factor (F_A) which can be calculated from *r* using

$$F_A = 2\frac{r-1}{r+1} \tag{2.22}$$

The paper also compares values between the asymmetry and correction factors and shows that when $F_A \leq$ 10.74% (0.1074), the correction factor *f* is approaching unity. In this case the correction required (1 - *f*) will be less than 0.1% of the uncorrected value, which effectively reduces the equation for the sheet resistance to

$$R_S = \frac{\pi R}{\ln(2)} \tag{2.23}$$

It should be noted that for all sheet resistance measurements made for the work presented in this thesis, the asymmetry factors of the Greek cross structures were also calculated. These values were found to be well below 10.74% and so no correction for asymmetry was needed.

Measurements at forward and reverse currents at each orientation will highlight any offsets in the test equipment. The zero-offset factor (F_0) is defined as

$$F_0 = \frac{(|R_0(+I) - R_0(-I)| - |R_{90}(+I) - R_{90}(-I)|)}{2R(\pm I)} \tag{2.24}$$

and a small value indicates that the measurement is not greatly affected by voltage

offsets in the test system.

2.6 Linewidth Measurement

Linewidth or Critical Dimension (CD) measurements are essential for the characterisation and control of the lithographic and photomask processes, however they become increasingly difficult as device dimensions reduce. The main methods for measuring linewidth are optical, scanning electron or probe microscopy and electrical techniques. Unfortunately, there is no single metrology that can deliver all needed information. This section will discuss each technique but will primarily focus on electrical measurements which form a large part of the body of work presented in this thesis.

2.6.1 Optical Metrology

Optical techniques are capable of CD measurements of both conducting and insulating features. However, as dimensions reduce they become limited by the wavelength of light being used. There are a number of techniques for measuring CD optically [55]. In a *video scanning* system an image of the feature being measured is obtained using a video camera connected to a microscope. This image is manipulated to provide a light intensity profile across the feature from which a value of the linewidth can be extracted. To produce a profile in a *slit scanning* system the sample is illuminated through a narrow slit which is stepped across the feature. The reflected light intensity is measured by a photodetector and plotted against the slit position.

Figure 2.13 illustrates how an optical critical dimension (OCD) measurement is performed on a photomask feature. Firstly the image of the feature is captured and the data processed to generate an intensity profile for the area of interest. The linewidth is measured by applying a set threshold that determines the edges of the feature from the points at which the intensity crosses the threshold. Finally the feature width is calculated as the difference between the edge positions.

Although CD metrology using optical microscopy has traditionally used threshold algorithms for calculating the edge position, they are usually non-linear in linewidth

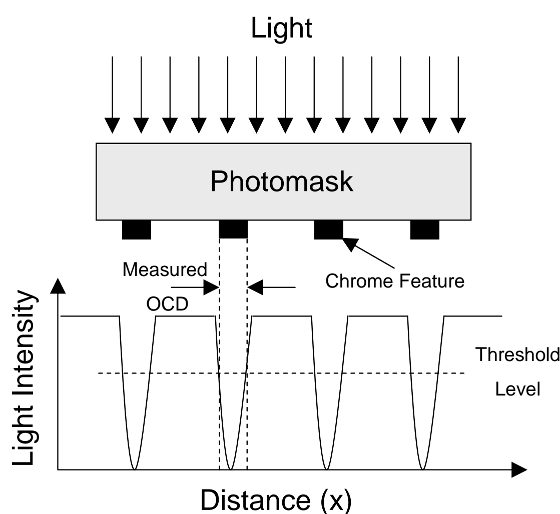


Figure 2.13: *Optical CD measurement by applying a threshold to a light intensity profile.*

(in particular for small features) and suffer from optical proximity effects (OPE). For this reason correction offsets have to be applied to compensate for the errors introduced with the optical measurement. These errors are corrected with the use of multi-point calibration techniques, each appropriate to the type, density and dimension of the feature being measured. These corrections are usually determined from measurements made on reference test sites, which unfortunately can become complicated and impractical.

Laser scanning is another method for optical CD measurement where the beam from a laser is scanned across the sample and scatters off the line edges producing an intensity signal in a photodetector mounted alongside the microscope objective. This system produces an intensity profile with two peaks at the line edges.

Although limited in resolution and thus becoming less useful as feature sizes reduce, optical microscopy is still the first choice for metrology on large features. It remains the primary inspection method in photomask fabrication environments where features sizes are normally four times larger than as printed, although phase shift and optical proximity correction features are roughly half the size of the printed structures. In addition there have been advancements with deep ultra-violet (DUV) sources, near-field and immersion microscopy, which allow imaging for sub-micron process control [20].

2.6.2 Critical Dimension Scanning Electron Microscopy (CD-SEM)

CD-SEM metrology has advanced significantly in the last 20 years and is now an industry standard inspection technique for high-volume wafer manufacturing. A scanning electron microscope uses a focused electron beam (e-beam) to produce an image of a surface [67]. It is made up of a series of subsystems and the first is the electron gun. This consists of an electrode source (cathode) and two electrodes (grid and anode) which extract and accelerate the electrons. The first SEMs used thermionic emission sources [45, 68], unlike modern systems which use field emission sources [45]. The beam then goes through one or two sets of lens and apertures, which condense the beam and control the incident beam current. Finally a set of scan coils deflects the beam to raster scan it across the sample and a final objective lens focuses the electrons to a point on the sample surface. The layout of a typical SEM column is shown in figure 2.14.

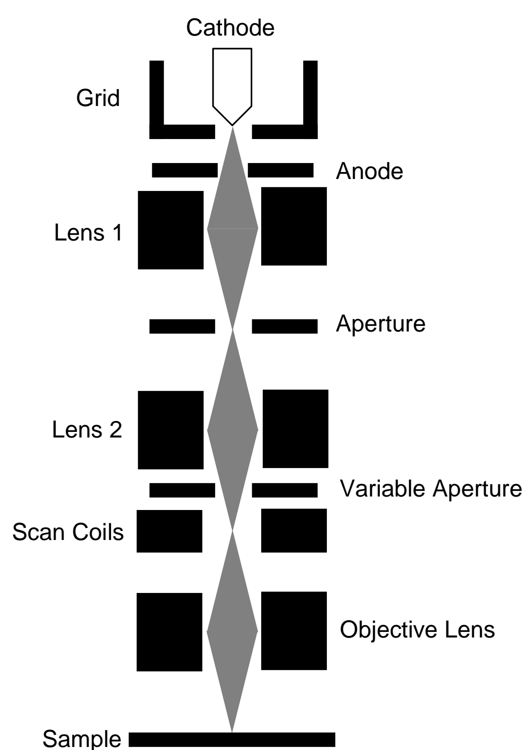


Figure 2.14: *Cross-sectional schematic of a standard SEM.*

When the beam hits the surface of the sample it produces secondary electrons (SE) and back scattered electrons (BSE). Secondary electrons can be collected by means of a grid

placed on one side of the specimen, while high energy back scattered electrons require detectors be mounted with a large solid angle of collection [67]. These signals are used to produce the image of the surface and a different image will be obtained depending on the signal being used to produce it.

For the measurement of linewidth with an SEM, an intensity profile from the image of the feature being measured is extracted and a threshold is then applied, in a similar manner to the optical technique. Given the differences in origin between backscattered and secondary electrons it should come as no surprise that there will be CD measurement variations between the two detection modes [23]. In addition an SEM measurement is considerably complicated because the image contrast is not only dependent on the material being scanned but also on the topography of the surface. Charging of the specimen is a problem for SEM metrology. Non-conductive samples accumulate charge when exposed to an e-beam, which can distort the image and even possibly damage the specimen. A chrome-on-quartz mask is an example of a sample charging in an SEM chamber, therefore producing images with poor contrast which is undesirable when attempting to make accurate CD measurements [69]. However, high-pressure SEM instrumentation in conjunction with large chamber and sample transfer capabilities can be potentially used for charge neutralisation. The methodology employs a gaseous environment to help compensate for the charge build-up that occurs under irradiation with the e-beam.

2.6.3 Scanning Probe Microscopy (SPM) and the Atomic Force Microscope (AFM)

Scanning probe microscopy uses a probe to scan a specimen and form an image of a surface. The most common type of SPM is the atomic force microscope and unlike its precursor, the scanning tunneling microscope (STM), it can image both conducting and insulating surfaces [26, 27]. The AFM consists of a probe tip mounted on a cantilever and a system which detects the vertical position of the tip. When the tip is in close proximity to the sample surface it experiences van der Waals forces. The surface information can be recorded by monitoring the deflection of the cantilever when the sample is scanned beneath the tip. An AFM can operate in several imaging modes. In contact mode the tip is brought close to the surface and the overall force is

repulsive, while in non-contact mode the separation is greater and the tip is attracted to the surface. In tapping or intermittent-contact mode the cantilever is driven to oscillate up and down at near its resonance frequency and the probe tip is tapped across the surface. This mode is less likely to damage the surface than contact AFM because it eliminates lateral forces between the tip and the sample. In addition it is more effective than non-contact mode when imaging surfaces with greater variation in sample topography [70].

Linewidth characterisation with an AFM is very sensitive to the interactions between probe tip and sample. The surface profile returned by the AFM will be affected by the shape of the probe tip as is shown in figure 2.15 [55]. Since the probe scan will depend on the probe shape, an error will be introduced in the measured linewidth and line shape, which can be corrected if the probe geometry is known. A high resolution AFM system can reach the atomic scale. However, it is very slow at performing measurements. Although it is not routinely used when large numbers of measurements are required, such as a process inspection environment, it is an excellent means for CD calibration [28, 71].

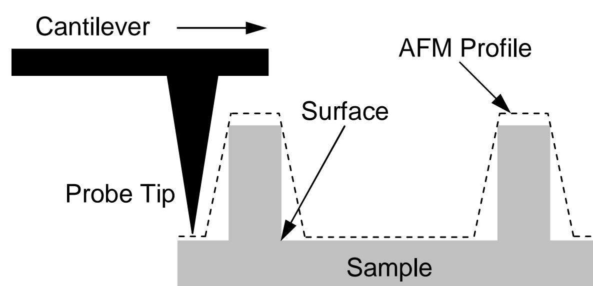


Figure 2.15: *Schematic illustrating an AFM scan and the resulting surface profile as affected by the tip shape.*

2.6.4 Electrical Test Structures and Measurement Techniques

2.6.4.1 Cross-Bridge Test Structure

The electrical critical dimension (ECD) or linewidth measurement differs from all other measurement techniques presented so far, in that the characteristic being measured is the conducting width of a feature, rather than the physical width. The standard technique for measuring ECD uses the cross-bridge test structure which is a combination

of a Greek cross and a four-terminal bridge resistor [72, 73]. A schematic of such a structure is shown in figure 2.16.

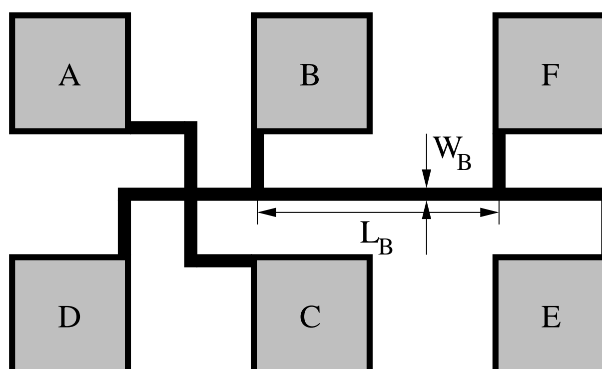


Figure 2.16: *Diagram of cross-bridge electrical test structure for sheet resistance and linewidth measurement.*

The electrical width (W_b) of the bridge section between the voltage terminals *B* and *F* is calculated with

$$W_b = \frac{R_S L_b}{R_b} \tag{2.25}$$

where (L_b) is the length of the bridge as shown in figure (2.16) and (R_S) is the sheet resistance of the material and is extracted from the Greek cross section as in 2.5.4. The value of W_b from equation (2.25) is the average value of the conductive width of the bridge section. To measure the bridge resistance (R_b) two measurements are made and the average resistance is calculated. Firstly a current I_{DE} is forced between terminals *D* and *E* and the voltage V_{BF} between terminals *B* and *F* is measured. The resistance is given by

$$R_b(+I) = \frac{V_{BF}}{I_{DE}} \tag{2.26}$$

The measurement is repeated with the current reversed and the resistance is once again determined

$$R_b(-I) = \frac{V_{FB}}{I_{ED}} \tag{2.27}$$

The average bridge resistance is then calculated using

$$R_b = \frac{(V_{BF} + V_{FB})}{(I_{DE} + I_{ED})} \tag{2.28}$$

There are two assumptions made in the calculation of the electrical width. Firstly it is assumed that the sheet resistance is uniform, so the value extracted at the Greek cross section applies to the whole of the structure. Any error in the sheet resistance will be directly translated to an error in the calculation of the linewidth in equation (2.25). Therefore it is necessary that the accuracy of the sheet resistance measurements is the same or better than that required for the linewidth measurement. Errors may be introduced by limits in the resolution of the voltmeter used in the Greek cross measurement or by non-uniformities in the thickness of the material.

The second assumption is that the length L_b of the bridge section is the designed length between the centres of the voltage taps. However this is complicated by the effect of the taps which effectively widen the bridge and lead to an over-estimation of the value of linewidth [74, 75]. This tap induced error can be minimised so that no correction is required by using the following design rules for the dimensions of the structure of figure 2.17 [65, 66]:

- $L_b > 150\mu$m
- $L_b > W_b$
- $W_b \geq W_t$

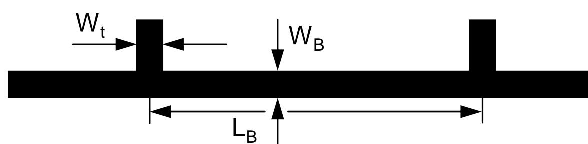


Figure 2.17: *Schematic of bridge section showing which dimensions need to follow the design rules.*

Reference [76] suggests that greater attention must be given to the design of cross-bridge structures with sub-micron geometries and presents additional guidelines for their design. In some processes it may be undesirable to follow the design given

above due to limitations in the structure layout. For example the length of the bridge may have to be shorter than the design rules and reference [75] describes a modified test structure which can measure the effect of the voltage taps and correct for them in the measurement of a short bridge section.

2.6.4.2 Split-Cross-Bridge Test Structure

A variation to the cross-bridge structure is the split-cross-bridge resistor [74] which can be used to measure the spacing between lines in addition to measuring sheet resistance and linewidth. The layout of the structure can be seen in figure (2.18). It consists of three sections; a Greek cross, a bridge resistor of length (L_B) and a split-bridge resistor of length (L_S).

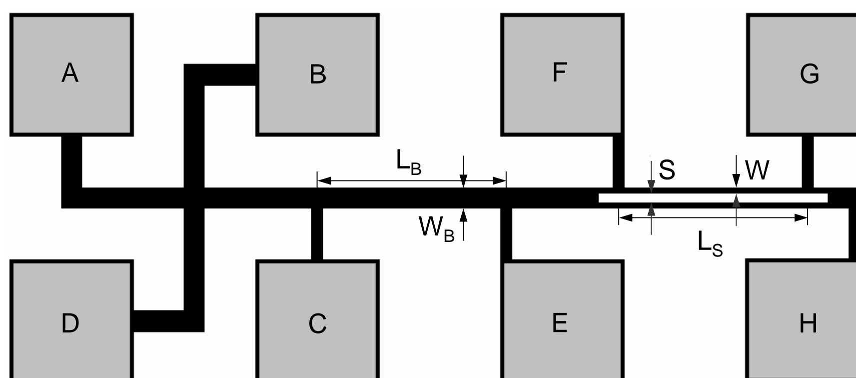


Figure 2.18: *Split-cross-bridge test structure used to measure sheet resistance, linewidth and line-spacing.*

The bridge resistor has a single conducting track of width W_B = *2W+S*. The split-bridge section has two conducting channels, each of width (*W*) so that the effective width is W_S = *2W*. Once the sheet resistance of the conducting material has been extracted, the linewidth of both the bridge sections can be measured electrically. The width of the split-bridge resistor is calculated in a similar manner to the bridge resistor from

$$W_S = \frac{R_S L_S}{R'_S} \tag{2.29}$$

where (R'_S) is the resistance of the split bridge. The line spacing (*S*) can then be determined by subtracting W_S from W_B and is calculated with *S* = W_B - *2W*. Finally

the pitch of the split bridge tracks can be calculated as $P = W + S$.

The design of the split-cross-bridge resistor follows from four geometrical design rules. If these rules are applied the equations presented can be used directly to obtain results that are accurate within 1%.

- The length (L) of the arm of the Greek cross must be at least twice the arm width (W).
- The width (W_t) of the voltage taps must be designed at the minimum width allowed. The distances, L_B and L_S, between the voltage taps must be large enough to minimise the error in measuring the linewidth, which is caused by disturbances in the channel current flow at the voltage taps.
- The length (L_t) of the voltage taps from the current carrying line must be at least twice the width of the voltage taps.
- The distances (H_B) and (H_S) from the edge of the voltage taps to a change in the linewidth must be at least twice the width of the channel.

2.7 Other Electrical Test Structures

Other electrical test structure designs have been presented in a number of publications, which could be adapted for the characterisation of photomasks. This section will briefly describe them and explain their use.

2.7.1 Alignment Test Structures

Overlay describes the positional accuracy with which a lithographic pattern is printed on top of an existing pattern on wafer [35]. Overlay control is a vital part of lithographic quality and like CD control it is essential for producing high-yield and high-performance semiconductor devices. There is a wide range of electrical test structures which can be used to measure errors in the alignment between successive layers in a process. References [77, 78] propose a van der Pauw sheet resistance structure which can be used to extract the misregistration between two masking layers, in both X and Y directions simultaneously. The differential linewidth bridge is another structure,

which is fabricated in a single conducting film and measures the overlay between two mask layouts [79, 80]. The voltage-dividing potentiometer and its derivatives are widely used for the measurement of alignment [81, 82]. Other test structures for the measurement of misalignment include the triangular transistor [83, 84], digital alignment verniers [85, 86] and the modified Wheatstone bridge structure [87].

For masks, pattern placement errors normally describe the deviation of the position of a printed feature from a designed coordinate grid. However, for chrome-on-quartz phase-shifting masks the measurement of chrome/phase registration is also very important. The phase-shifters are fabricated by etching into the quartz substrate and the required depth depends on the wavelength (λ) of the light intended to be used with the mask and the refractive index (n) of the substrate material. The etch depth required to give 180° phase-shift is calculated using [16]

$$d = \frac{\lambda}{2(n-1)} \tag{2.30}$$

The removal of the quartz changes the effective capacitance between two chrome tracks on the mask and this effect can be used in a test structure to investigate the misalignment between the two mask layers. An interdigitated on-mask capacitor test structure [88–90] has been proposed for the measurement of the overlay between the chrome and phase-shifting elements on phase-shifting masks. The layout of the proposed interdigitated capacitor can be seen in figure 2.19 with part of the structure expanded to show the interdigitated fingers and the phase-shifting regions. The structure contains 2001 electrode fingers, giving a total of 2000 lateral capacitor elements, with each being 1000μm long. A progressional offset technique (POT) [91, 92] has been used to extract the degree of alignment error between the metal and the phase-shifter elements.

A photomask was fabricated with sets of POT arrays to measure X and Y-offsets. Each array consists of test structures with different amounts of in built misalignments. The test structure with the lowest capacitance will indicate the actual misalignment. The prototype mask was exposed with a deliberate misalignment in X direction, to help verify the suitability of the technique. Initial results exhibit a minimum capacitance value, which confirms that the structures have the required sensitivity for

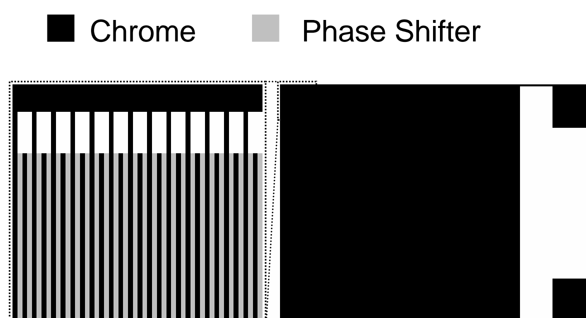


Figure 2.19: *Schematic layout of an interdigitated capacitor alignment test structure.*

the measurement of the misalignment.

Similar interdigitated capacitor structures could be used to measure the depth of the phase-shifting trenches, which is a very important parameter for phase-shifting masks. The test structure would detect the change in the fringing field as a function of the quartz etch depth. If the mask is intended for use with 193nm illumination and n_{quartz}=1.56 then the phase-shifter depth should be 172.3nm. Simulations at this target depth on simple capacitive structures using the 2-D solver for interconnect analysis *Raphael* [93], suggest that the depth sensitivity of a capacitor structure with an electrode spacing of 400nm is $\sim 2 \times 10^{-20}$ Fμm^{-1} per nm of offset. Therefore a test structure with 2000 capacitive elements, each 2000μm long would have a sensitivity of $\sim$ 0.1pF per nm offset. Hence it may be possible to monitor the depth of phase-shifting trenches using this method.

2.7.2 Electrical Test Structure for the Measurement of Contact Holes

A technique to electrically measure isolated features such as the size and area of contact holes has been been proposed by B.J. Lin et al. [94]. The proposed test structure consists of two 4-terminal bridge resistors for the extraction of the ECD and two modified ones as shown in figure (2.12). A Greek cross sheet resistance monitor is also included. The modified structures contain a large number of isolated holes in the lines running in the X and Y direction. Because of the contact holes, the electrical linewidth of the modified lines is reduced. Subtracting the reduced linewidth from that of the solid reference line running in the same direction, will provide the information

required to extract the size of the contact holes. Both the horizontal and vertical line pairs are required to detect subtle hole dimension changes in the X and Y directions.

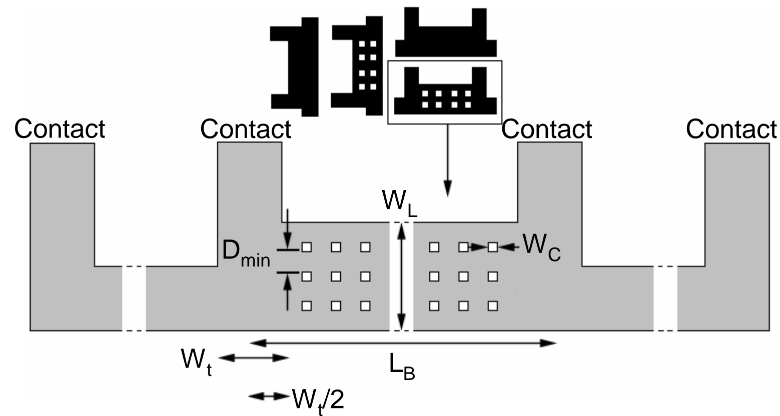


Figure 2.20: *Partial layout of bridge resistor test structures for the measurement of contact holes.*

The relationship between the hole size and the perturbed linewidth is taken from Hall's work [95]. This gives the resistance of a bar with one small round hole, as

$$R = R_S[\frac{L_B}{W_{ref}} + \frac{\pi}{2}\epsilon^2 + \frac{\pi^2}{24}\epsilon^4 ... \qquad (2.31)$$

where *(L_B)* and *(W_{ref})* are the length and the width of the reference bar respectively (L_B is also the length of the hollow bar). ϵ is the ratio of the hole diameter *(W_C)* to W_{ref}. For a bar with many holes well separated from each other (isolated), so that the current flow pattern near each hole is not disturbed by the presence of the others, the total resistance of the line is evaluated by multiplying the second and higher order terms in equation (2.31) by *N* (*N* is the total number of identical holes in the test structure). Hence

$$R = R_S[\frac{L}{W_{ref}} + \frac{N\pi}{2}\epsilon^2 + \frac{N\pi^2}{24}\epsilon^4 + ...] \qquad (2.32)$$

The expression in equation (2.32) can used to solve for the hole size with a given pair of measured hollow and solid lines. By using

$$W_{ref} = R_S \frac{L}{R_{ref}} \tag{2.33}$$

where (R_{ref}) is the resistance of the reference bar and

$$W_L = R_S \frac{L}{R} \tag{2.34}$$

where (W_L) is the width of the hollow bar, equation 2.32 can be rewritten to solve for W_C.

2.7.3 Matching Test Structures

Closely spaced IC devices which are identically designed form a matching pair. By definition such devices are manufactured at the same time, and with the same equipment and processing conditions. However, mismatches or offsets can always be observed and when a large group of matched pairs is measured, the mismatch varies from pair to pair. Measuring, quantifying and understanding the mismatch fluctuations of IC components is very important. The knowledge gained from such studies improves the performance of mismatch sensitive ICs, which leads to better electronic circuit performances and higher product yields.

Early studies on parametric mismatch fluctuations for IC components, by McCreary [96] and Shyu et al. [97], dealt with matching issues for Metal Oxide Semiconductor (MOS) technology and switched capacitor applications. Significant work on electrical measurement methods and characterisation techniques for matched IC components has been made by Tuinhout [98]. There is a great number of matching related papers in the literature. Examples which contributed to a wider understanding include [99] which presented requirements for matching test structures focusing on matched BJT pairs. In [100, 101] the systematic mismatch between MOSFET (Metal Oxide Semiconductor Field-Effect Transistor) pairs was investigated. Reference [102] employed a new resistor test structure approach and data analysis procedure to identify mismatch effects associated with mask writing artefacts. A technique that uses DC parametric measurement systems for measuring capacitor mismatch is reported in [103]. Finally [101, 102, 104, 105] investigated the importance of robust

measurement and analysis techniques.

2.8 Conclusions

Continuing advances have allowed optical lithography to remain the technology of choice for semiconductor patterning. Although, photomasks have been an integral component in the lithographic process, they are now more than a master pattern that maps the IC design onto wafers. An introduction to the operation and fabrication of photomasks has been made and some methods that offer resolution improvement have been briefly described. In addition, the operating principles of resolution enhancement techniques such as phase-shifting masks and off-axis illumination have been presented. The effects of proximity and proximity correction techniques have also been discussed. The advancement in photomask technologies has challenged significantly the traditional photomask measurement and verification techniques, which have to be able to fully characterise an advanced photomask process.

This chapter has also presented methods for the extraction of the sheet resistance of thin conducting layers. The four-point probe is useful for un-patterned films. The four-terminal van der Pauw method can be used to extract the sheet resistance of small, arbitrarily shaped, samples of uniform thickness and resistivity. The Greek cross is a special case of the van der Pauw structure with finite contacts and a scalable geometry which makes it ideal for use as an on-mask test structure. In addition, it is a critical component for the measurement of the electrical linewidth.

Critical dimension measurements are very important for the characterisation of the photomask and the lithographic process. The operation and limitations of optical, CD-SEM and AFM measurement techniques have been presented. OCD and CD-SEM metrologies require a subjective decision to determine the feature edges, which can lead to errors. AFM metrology is very sensitive, but is also slow and requires that the tip shape is known for accurate measurements. Electrical linewidth measurements are typically performed using a four-terminal Kelvin bridge resistor in combination with a Greek cross sheet resistance structure. Although limited to conducting features, it is a highly repeatable and cost effective technique. Furthermore, the basic cross-bridge test structure can be adapted to measure many different parameters such as pitch,

line-spacing or the diameter of contact holes.

Chapter 2 has also briefly reported a range of different test structures used to measure the overlay between successive lithographic layers. A test structure for the measurement of the misalignment between the chrome patterns and the phase-shifting layers on a photomask was described. A similar test structure could be used for the measuring the depth of the phase-shifting trenches on masks. Finally, matching test structures and their measurement techniques were introduced. These could be adapted for on-mask mismatch measurements.

Chapter 3
Linewidth Measurement Techniques for the Characterisation of Binary and Alternating Aperture Phase-Shifting Masks

3.1 Introduction and Early Work Background

Modern photolithographic enhancement techniques such as off-axis illumination, immersion lithography, optical proximity correction and the use of phase-shifting masks have driven advances in microelectronics in recent years. It is now possible, through a combination of these technologies, to produce CMOS transistors with a gate length that is less than half the wavelength of the light used in the photolithographic system. Advanced photomasks using OPC or phase-shifting technologies are extremely complex and expensive to manufacture and so the ability to test and characterise them is becoming increasingly important. Traditionally, metrology and verification of photomasks is performed using either optical or critical dimension scanning electron microscopy, both of which require expensive equipment. Electrical measurements, made with relatively inexpensive equipment, have the potential to be both faster and more repeatable than both these methods.

Electrical linewidth measurement test structures have been designed in the past by Lin et al. [106], to investigate binary and phase-shifting masks. Different photomask schemes were used to print the structures on wafer, in order to examine exposure latitude, depth of focus and proximity effects. Smith et al. [69, 107] at the University of Edinburgh took this concept a step further by patterning the structures so they can be electrically measured on the mask. Cross-bridge [72] test structures which were originally developed to investigate metal damascene interconnect processes [108], were modified for use on a prototype mask with the alternating aperture phase-shifting

design [16] (Alt-PSM). The test structures were designed for measuring the sheet resistance of the light blocking chrome material and the electrical critical dimension of the on-mask features. Initial electrical measurement attempts showed that it is extremely hard to probe through the chrome oxynitride anti-reflective coating (ARC) covering the chromium layer. Therefore to achieve good electrical contact between the probes and the chrome pads, the mask had to undergo further processing which removed the ARC.

Further electrical measurements were made and the results compared very favourably with measurements made on the same structures using a CD-SEM. In fact the CD-SEM measurements proved difficult to make, as charging of the mask in the SEM chamber led to images with poor contrast and long measurement times. This lowered the measurement repeatability of the CD-SEM to a level which was significantly worse than the ECD method. The initial work on references [69, 107] raised a number of issues, so additional measurements, including AFM scans [88–90], were made to further explain the results. The AFM scans confirmed that the process of removing the ARC partially etched the chromium underneath in a way that lead to errors in some of the sheet resistance and ECD measurements. The narrowest Greek cross structures became very asymmetrical and did not have a constant thickness required by a van der Pauw structure. Nevertheless the ECD technique was more repeatable than the CD-SEM extraction, which was affected by the phase-shifting regions.

An enhanced test structure design for Alt-PSMs, that overcame the problems encountered with the prototype mask, was fabricated and initial results were reported in reference [109]. The new mask (PSM3920) was designed so that the ARC over the probe pads would be exposed and removed during the phase-shift etch process. However, the fabrication process was still under development, and the phase-shifting elements did not get etched to the full depth required for an $180°$ phase difference. Therefore the ARC was not completely removed over the pads and during electrical measurements the probe tips accumulated ARC residue after a few probing cycles. A secondary layout was prepared to selectively etch the ARC over the probe pads without affecting the test structures themselves and this allowed the electrical measurement of a full set of structures. The results from sheet resistance measurements showed little or no variation with feature size and therefore no significant asymmetries from

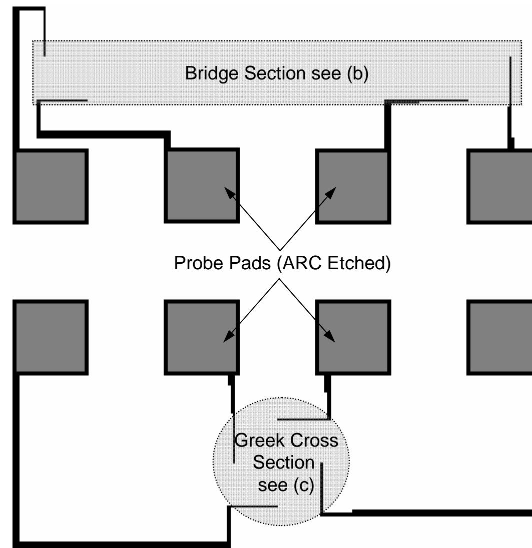
uneven chrome etching. This facilitated the extraction of the sheet resistance required for the ECD measurement from a structure adjacent to where the ECD measurement is performed. Using a local R_S value reduces the possibility of errors being introduced by variations in the chrome layer thickness. Nevertheless sheet resistance measurements on the masks under investigation showed a chrome thickness variation of $\approx 1\%$ across 100mm. This indicates that the uniformity of the chromium film is very good, as would be expected from the specifications on advanced photomask plates. Typically the thickness of the chrome layer is 70nm, while the ARC material covering the chrome film is 30nm thick.

The work on this chapter continues from this point to further investigate PSM3290. A second mask (PSM3926) was also designed and fabricated, with the same layout but with the correct phase-shifter etch depth. This mask could be measured electrically without any further processing required and the CD results were compared to those from the prototype mask. The two masks were also measured optically with an industry standard optical mask metrology tool and the complete sets of results were analysed to investigate the capability of the two measurement techniques [110, 111].

3.2 Test Structures and Photomask Layout

PSM3920 and PSM3926 consist of on-mask electrical cross-bridge test structures and their design is illustrated in figure 3.1(a). Each structure is partitioned into a four-terminal, 600μm long, Kelvin bridge resistor [65, 66, 72] and a Greek cross Van der Pauw component [59, 60, 62] and their layouts are presented in figures 3.1(b) and 3.1(c). The measurement procedures for these structures to extract the R_S and ECD are detailed in Chapter 2. In most structures the electrically measured lines are surrounded by dummy features. These provide the layout needed to apply the phase shift and are designed in a similar way to the Alt-PSM test sites described in [106]. As seen in figure 3.1(b) the chrome lines are surrounded by un-etched (white areas) and phase-shifted etched quartz (gray areas) in an alternating nature. In addition the Greek cross section uses the "L-Type" design described in [69, 107], where the dummy unmeasured features follow the shape of the cross.

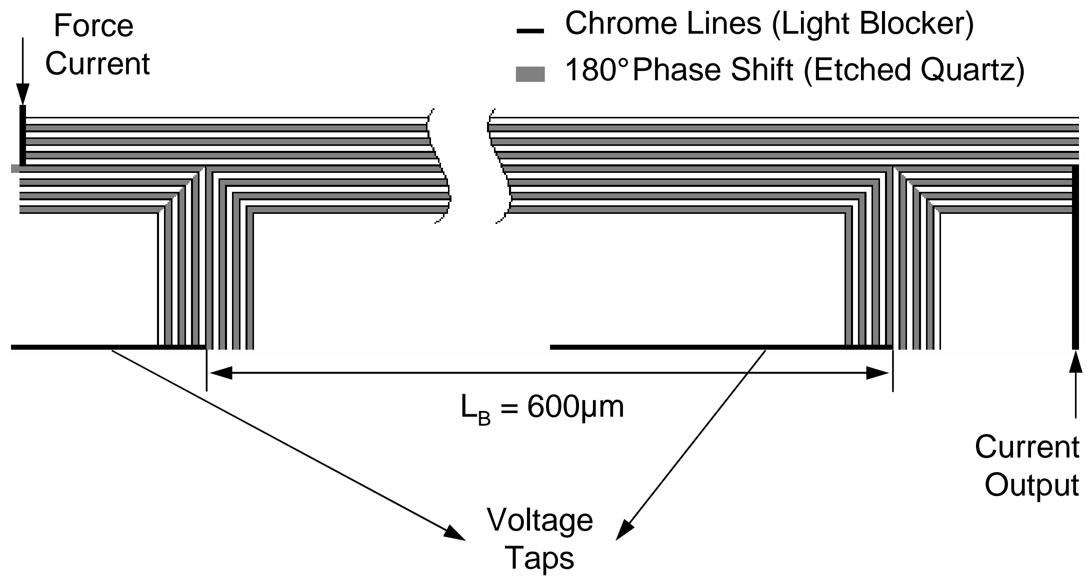
Both masks consist of a binary and a phase shifted section, each with 12 identical blocks



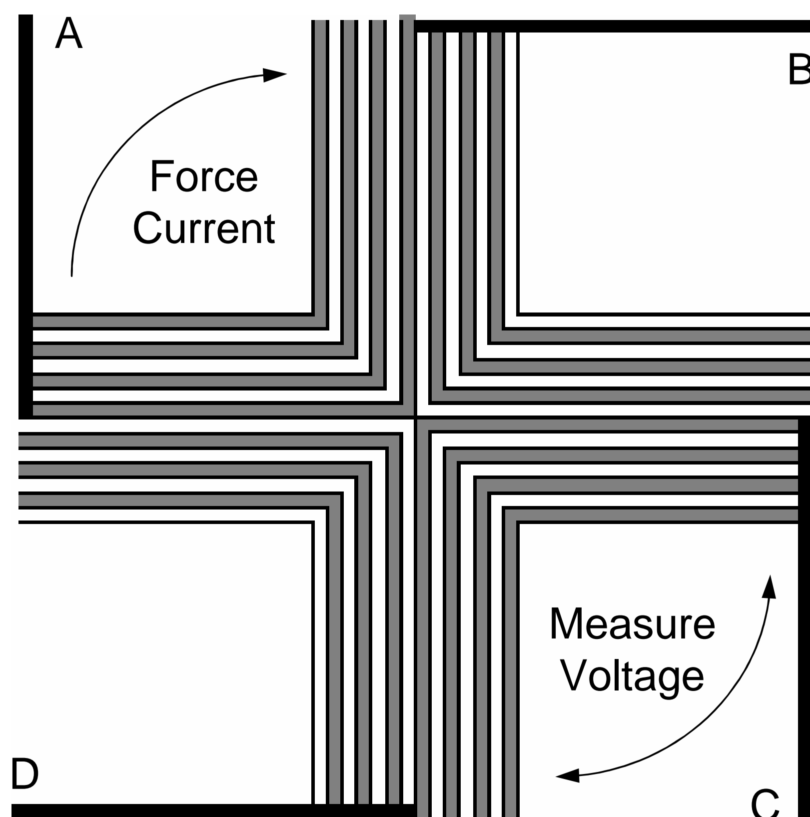
(a) Schematic layout of Cross-bridge resistor with on-mask pads.

Figure 3.1: *Layout and close up view of Cross-bridge on-mask electrical test structure.*

of on-mask test structures. The complete mask layout can be seen in figure 3.2(a). Each block of structures has 126 cross-bridge pairs, split into 18 sets with on-mask feature dimensions of 240, 260, 280, 300, 320, 340, 360, 380, 400, 500, 600, 700, 800, 900, 1000, 1100, 1200 and 1500nm (see figure 3.2(b)). Each set (see figure 3.2(c)) has an isolated structure with no dummy features and six dense line structures with line to space ratios (LSR) of 1:1, 1:1.5, 1:2, 1:3, 1:5 and 1:10. An LSR of 1:1 means that the design line-spacing is equal to the linewidth while an LSR of 1:10 means that the spacing is 10 times the linewidth. For example if the nominal CD of the chrome line is 500nm, then the space between the lines will vary from 500nm (1:1) to 5000nm (1:10). For reference purposes the isolated lines, without any phase shift, are also included in the phase-shifted block.

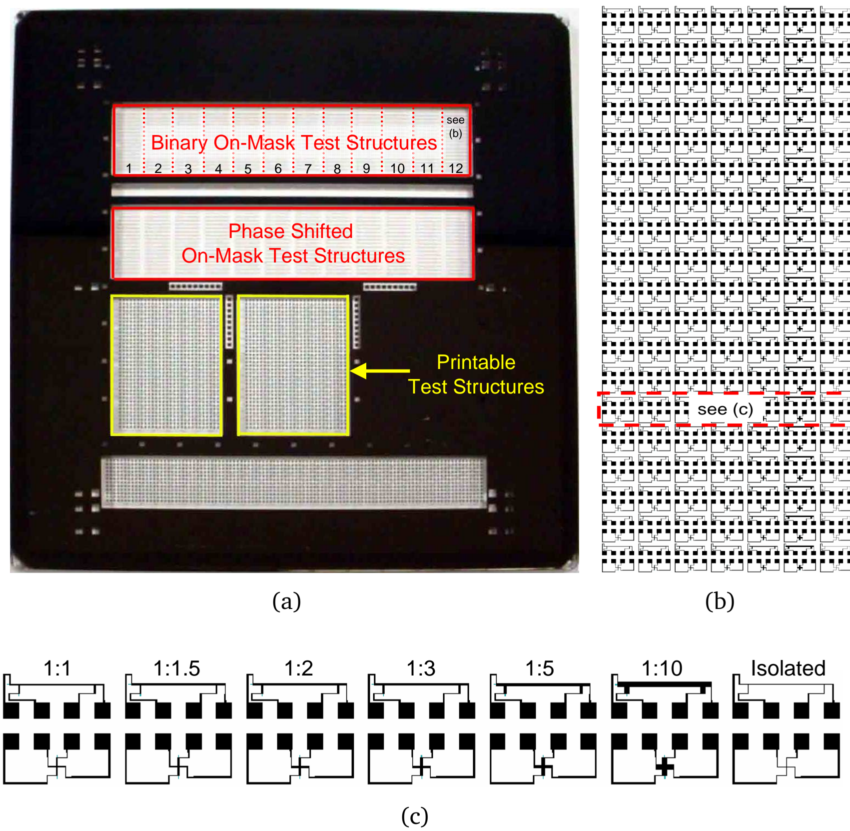


(b) Expanded view of phase-shifted Kelvin bridge section.



(c) Expanded view of phase-shifted Greek cross section.

Figure 3.1: *Layout and close up view of Cross-bridge on-mask electrical test structure (continued).*



(a) (b)

(c)

Figure 3.2: *(a) Layout of alternating aperture phase-shifting masks PSM3920 and PSM3926 (b) Block of on-mask test structures (c) Set of on-mask structures for one feature dimension.*

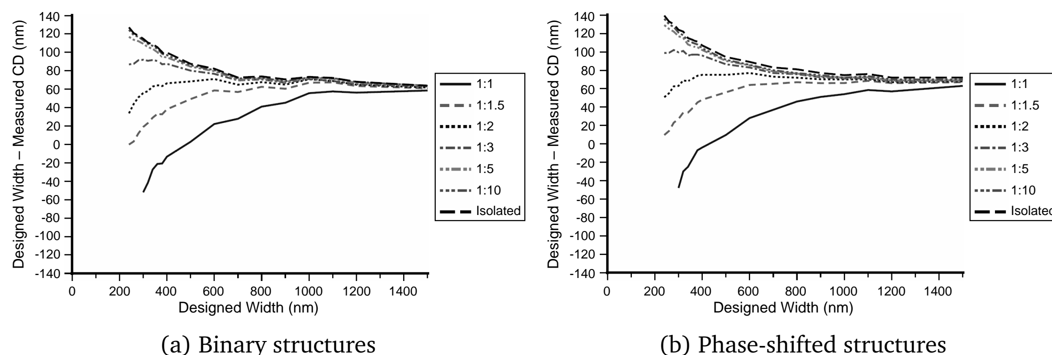
In addition to the on-mask test structures there are layouts of printable versions, which can be used to pattern the structures on wafer when exposed by a 4X photolithography system. Although the dimensions of the wafer-level features will be four times smaller than the on-mask dimensions, the printable pads have been designed so that the wafer structures can be probed with the standard 2×4 probe card used for the on-mask measurements.

3.3 Electrical and Optical CD Measurements

Electrical and optical CD measurements were performed on blocks of binary and phase-shifted structures, for both masks PSM3920 and PSM3926. The electrical measurements were performed using an HP4062B Semiconductor Parametric Test System [112] and a high resolution Solartron 7065 voltmeter [113]. To extract the

optical CD values a MueTec <M5k> mask metrology system [22, 114, 115] using 248nm DUV illumination was used. The optical measurement procedure has been described in Chapter 2. In practice, the process of extracting an accurate optical CD can be complicated. The intensity profile is affected by the feature size and the proximity of other features and calibration offsets are applied to correct for these effects. These corrections are determined from measurements of reference artefacts and are especially complicated when the feature sizes approach the wavelength of light used to obtain the image. At present, the optical inspection tools used in mask verification are often a generation behind the lithography systems so that 365nm i-line light may be used to measure DUV masks. This problem is reduced because the mask features are four times larger than the printed dimensions and for this work a mask metrology system with DUV illumination is used. Nevertheless, the range of structures measured was limited to nominal dimensions between 320nm and 1500nm, due to the quality of the photomask image as the resolution limits of the metrology tool are approached.

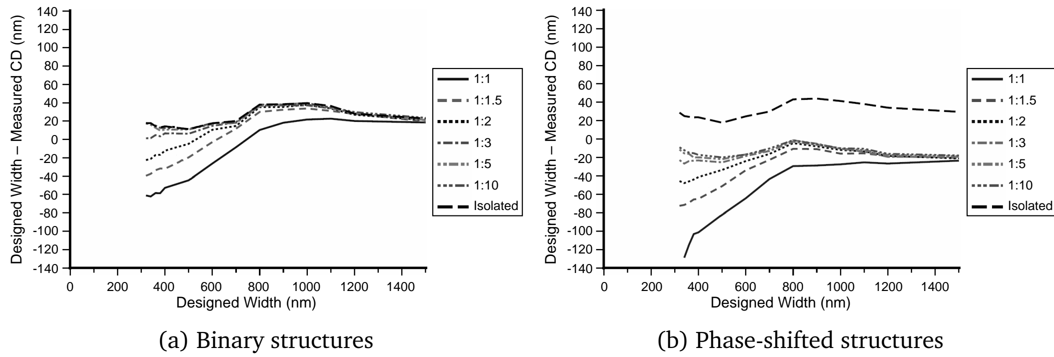
Plotting the CD results against the nominal dimensions is unhelpful as the wide range of values tends to hide small changes and offsets in feature size, making it difficult to observe any trends in the data. Therefore, the measured CD values are subtracted from the nominal dimensions. This means that a positive value indicates a measured width that is narrower than the designed dimension, while a negative value means that the line appears wider than it should. The full electrical and optical results of the measurements can be seen in figures 3.3 - 3.4 for PSM3920 and 3.5 - 3.6 for PSM3926.



(a) Binary structures

(b) Phase-shifted structures

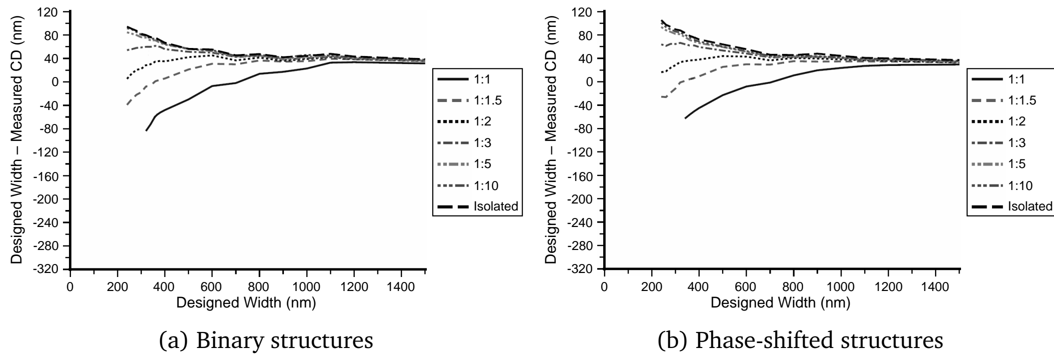
Figure 3.3: *Electrical CD measurement results from mask PSM3920 for a range of line to space ratios.*



(a) Binary structures

(b) Phase-shifted structures

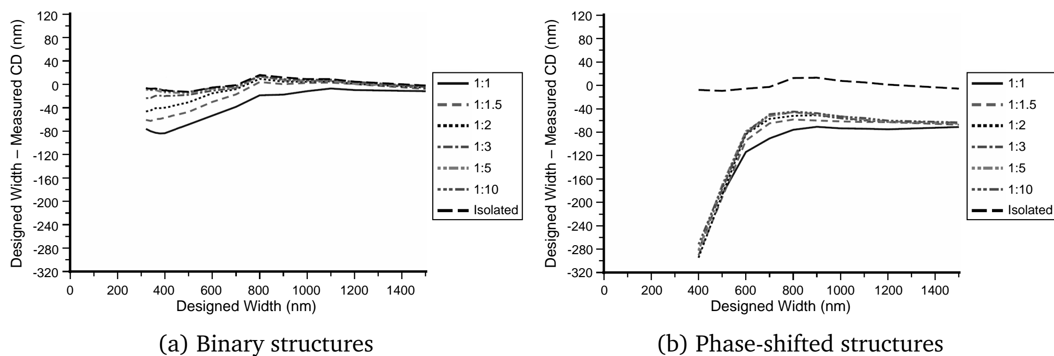
Figure 3.4: *Optical CD measurement results from mask PSM3920 for a range of line to space ratios.*



(a) Binary structures

(b) Phase-shifted structures

Figure 3.5: *Electrical CD measurement results from mask PSM3926 for a range of line to space ratios.*



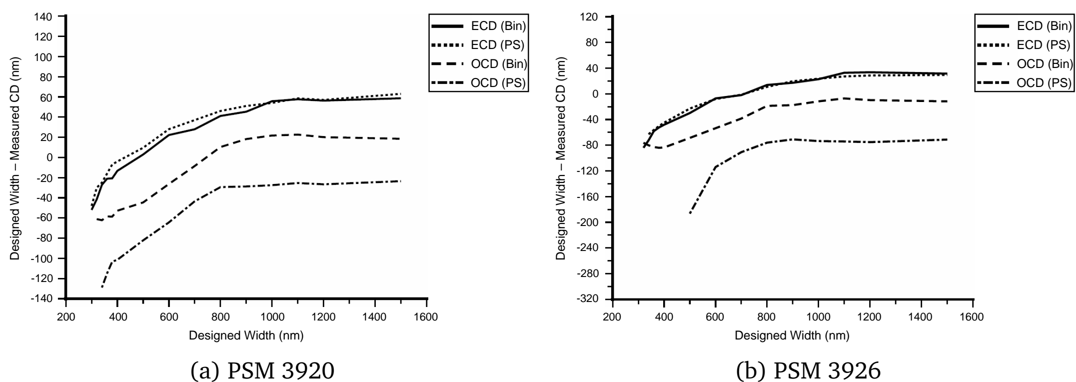
(a) Binary structures

(b) Phase-shifted structures

Figure 3.6: *Optical CD measurement results from mask PSM3926 for a range of line to space ratios.*

It is clear that the alternating phase-shifting elements have a significant effect on the optical measurement, leading to an offset between the binary and phase-shifted results for mask PSM3920. This is highlighted in the results of figure 3.4(b) from the block of phase-shifted structures where the isolated reference lines, without phase-shift, appear to be narrower than the structures with 1:10 LSR. This offset is not present in the electrical measurement results from the same same structures, in figure 3.3(b). This effect is similar to that observed with CD-SEM measurements on earlier on-mask test structure work, where phase-shifted features appeared wider than binary lines [69, 88, 90]. The electrical results from mask PSM3926 show similar patterns to PSM3920 for both binary and phase-shifted structures. This is also the case for the optical results from the binary structures but the phase-shifted structures are quite different. At nominal linewidths below 600nm, the optical measurement fails and the lines appear significantly wider than expected. This indicates a serious issue with the optical measurement of narrow phase-shifted features on PSM3926.

The electrical and optical results also show a change in the measurement offset with proximity. While the isolated and widely spaced lines show a relatively small variation with feature size, the most densely packed lines are measured as being significantly wider and this effect increases as the dimensions are reduced. This can be seen in figure 3.7, which compares electrical and optical results from structures with a 1:1 line to space ratio.



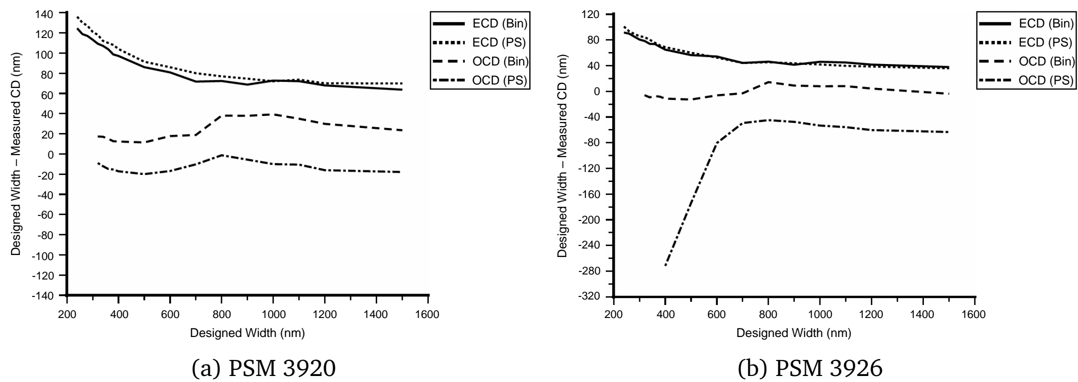
(a) PSM 3920

(b) PSM 3926

Figure 3.7: *Comparison of electrical and optical measurement results from binary and phase-shifted structures with 1:1 line to space ratio.*

Although there is clearly a significant offset between results obtained by different measurement methods, the trends of both sets of curves are similar for both masks,

apart from the phase-shifted lines below 600nm on PSM3926. As the electrical results reflect the actual physical structure, this suggests that the calibration of the optical measurements of dense features is reasonably accurate but that an offset is required to correct the phase-shifted results. This is not the case for more isolated features as is shown in figure 3.8, which compares results from structures with a 1:10 line to space ratio.



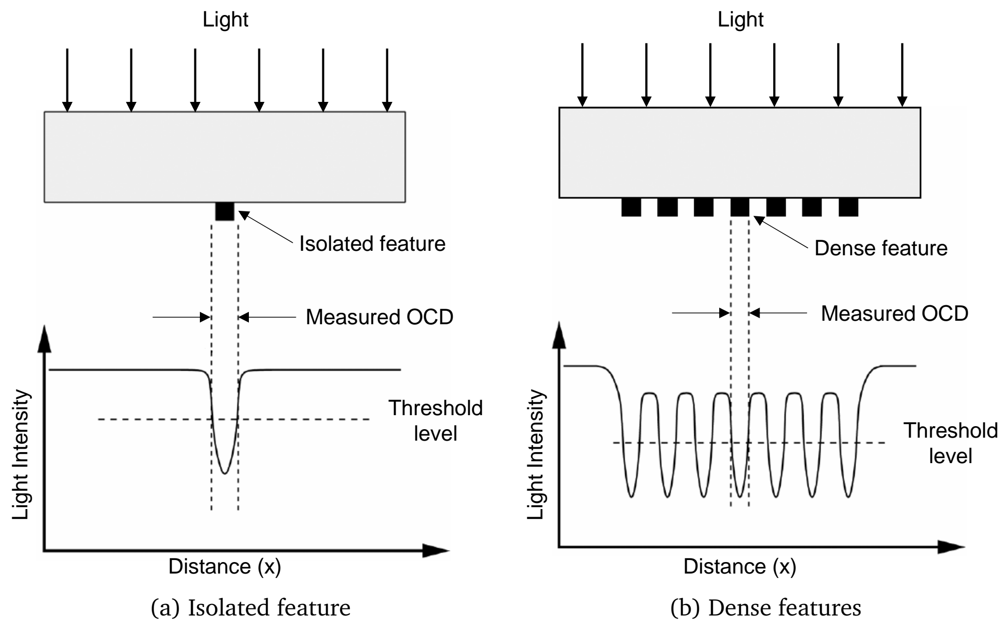
(a) PSM 3920 (b) PSM 3926

Figure 3.8: *Comparison of electrical and optical measurement results from binary and phase-shifted structures with 1:10 line to space ratio.*

For nominal feature sizes between 1500nm and 800nm, the results track each other well with a constant offset between optical and electrical measurements. However, below this value the electrical measurements indicate a reduction in feature size while the optical CDs tend to increase. This finding is similar to results presented in reference [116], where an optical tool was found to overestimate the dimensions of isolated features smaller than 700nm when compared to AFM reference measurements. The electrical measurements cannot be directly affected by the proximity of other features, and represent the way in which proximity effects alter the dimensions during fabrication of the mask. The optical measurements, on the other hand, depend on the ability to obtain accurate images of the features, relevant to the calibration used. The results suggest that this is difficult in the case of the narrowest isolated features, despite them being resolvable by the microscope optics. The phase-shifted OCD results from PSM3926 again show a significant error for structures with a designed linewidth below 600nm.

One possible reason for the observed effect is that the intensity does not reach a true zero value under the narrow isolated features. However, the percentage intensity

threshold for the CD measurement is still applied as if the full contrast was achieved. This means that the threshold, and therefore the measurement point, is pushed up the intensity curve to a different level, making the line appear wider. In the more dense structures the maximum intensity in the image taken by the measurement system is typically reduced, which balances the previous effect so that the threshold is more representative of the true CD. These effects are illustrated in figure 3.9.



(a) Isolated feature

(b) Dense features

Figure 3.9: *Illustration of possible sources of errors with optical CD measurements.*

The explanations offered so far for some of the issues with the optical measurements do not explain the problem with the optical CD measurements on the narrowest phase-shifted structures of mask PSM3926. Figure 3.10 shows a correlation plot of the phase-shifted OCD against the binary OCD for the same designed width, for both masks. Results from PSM3920 are well correlated with a small offset from the ideal, probably caused by the sidewalls of the phase-shifting trenches. PSM3926 shows a similar correlation down to a binary linewidth of about 600nm. Below this value the apparent optical CD of the phase-shifted features becomes almost constant at around 680nm. A significant difference between the two masks is the depth of the quartz etch used to create the phase-shifting trenches. The trench depths, measured optically on standard test features, and the effective phase angle with 248nm DUV illumination are presented in table 3.1 along with the target values.

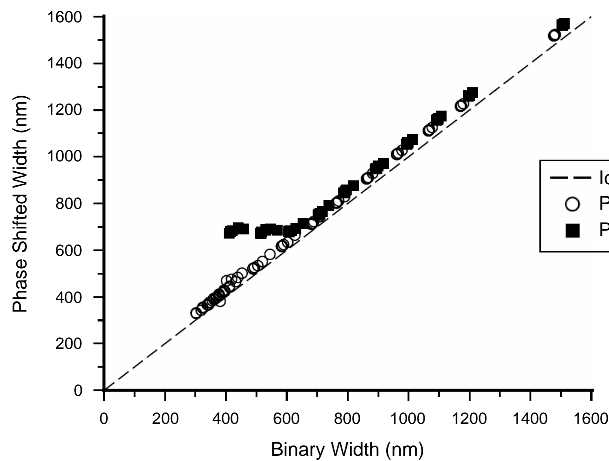


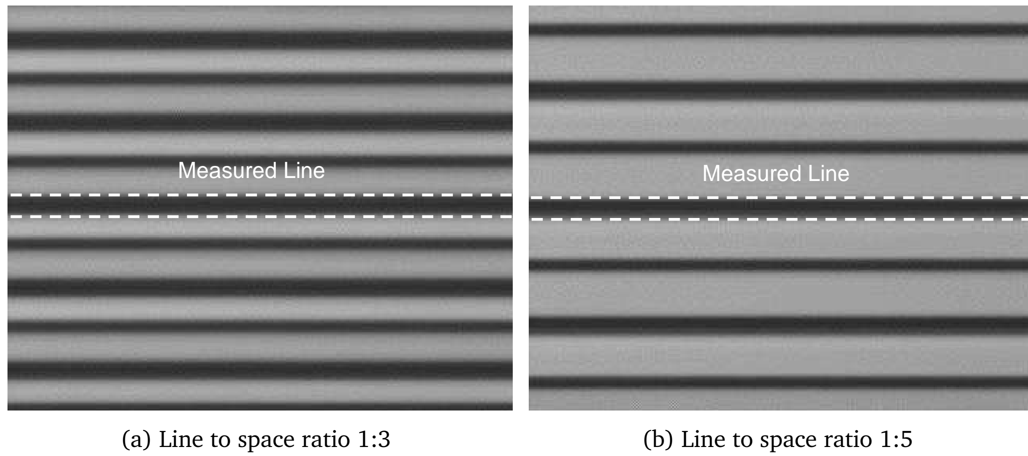
Figure 3.10: *Correlation plot of phase-shifted against binary optical CD measurements.*

Parameter	Target	PSM3920	PSM3926
Trench Depth	243nm	180nm	260nm
Phase Angle	180°	135°	195°

Table 3.1: *Measured and target phase-shift trench depths and phase angles.*

In published on-mask test structure work [69, 110] it was found that the phase-shifting trenches can affect traditional optical CD and CD-SEM metrology methods. However, the results from PSM3926 show that a much more extreme error can be introduced into the optical measurement, which is most likely caused by the the presence of the phase-shifting trench. This error is illustrated in figure 3.11, which shows two images captured from structures on PSM3926 using the MueTec mask metrology system. The nominal linewidth in each case is 400nm.

All of the lines shown in figure 3.11 should have the same width, but there appear to be two different widths in the images obtained from the metrology tool. The optically measured line is marked in each case and the extracted CDs are 682.6nm for figure 3.11(a) and 681.3nm for figure 3.11(b). This "thick/thin" line effect can be interpreted as the result of an error introduced by the phase-shifting elements, as it is not observed with the binary structures on this mask. Comparisons between electrical and optical measurements (see figures 3.7(b) and 3.8(b)) suggest that this is an optical effect related to the phase-shifting elements as only these results are affected. Figure 3.12 shows an image from a 400nm nominally wide phase-shifted structure with an LSR of 1:3 on mask PSM3920. The image was captured using the MueTec



(a) Line to space ratio 1:3 (b) Line to space ratio 1:5

Figure 3.11: *MueTec (M5k) images of phase-shifted structures from mask PSM3926.*

tool, however, all the lines in the structure appear to have the same width and the phase-shifters do not cause the optical effect seen with PSM3926.

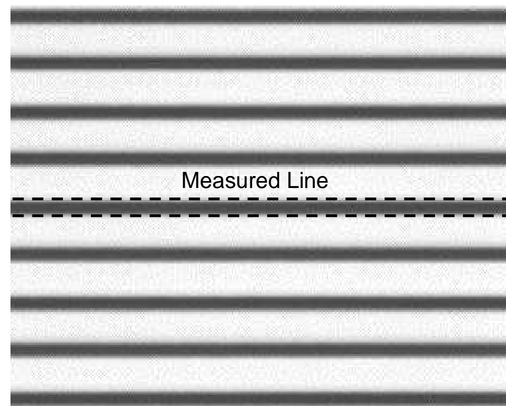
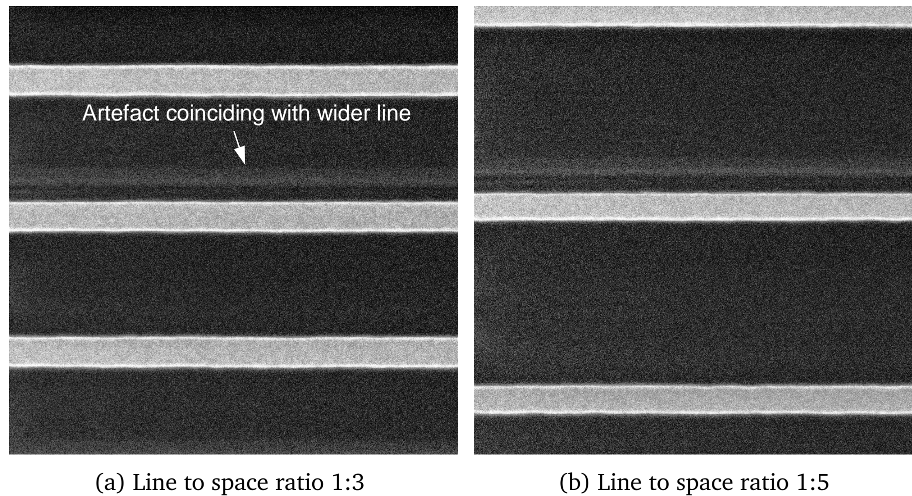


Figure 3.12: *MueTec (M5k) image of phase-shifted structure with 1:3 line to space ratio from mask PSM3920.*

To further investigate this effect high resolution images were obtained with a Focused Ion Beam (FIB) mask repair tool. Figure 3.13 shows images of the two structures from mask PSM3926, captured with a Seiko Instruments SIR 500 [117] repair system. It should be noted that for the purposes of this investigation the contrast of the images has been enhanced using the image processing software ImageJ. The high resolution images indicate that there is an artefact coinciding with the side of the chrome feature which is affected by the phase-shifter for the lines that were found to be optically wider. However, the images confirm that the "thick/thin" line effect is not a physical fabrication problem with the chrome tracks. The electrical technique is measuring the

conducting width of the chrome lines correctly and so the artefact visible in the FIB images, which also causes the optical effect, should be related to the etched quartz forming the phase-shifters.

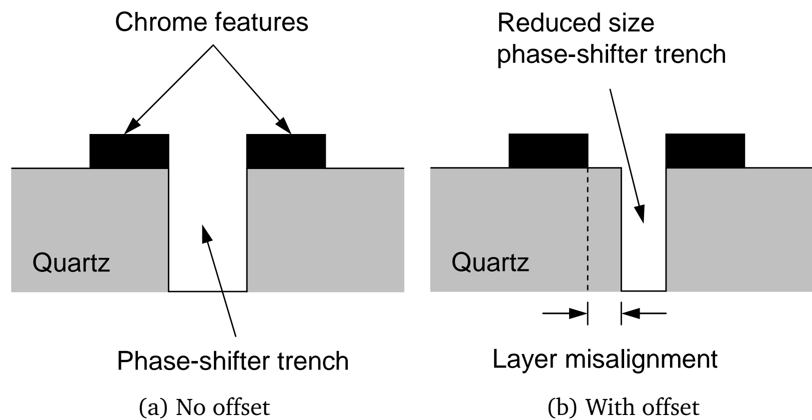


(a) Line to space ratio 1:3 (b) Line to space ratio 1:5

Figure 3.13: *FIB images of phase-shifted structures from mask PSM3926.*

The phase-shifting mask is fabricated in a two stage process. First, the chrome layer is patterned to form the light blocking features and then the phase-shifting areas are etched into the quartz substrate. A possible reason for the effects seen is an overlay error between the chrome layout and the phase-shifting layer. The ideal phase-shifting design and a design with misalignment between the two layers can be seen in figure 3.14. Measurements were made to check the misalignment of the 2nd layer processing and the mean offset taken from five targets was found to be +80nm in X and +280nm in Y. This offset in the Y-axis is large enough to give an overlap in the trench of the structures and this effect should be worse for the narrowest tracks.

On an SEM the intensity of a signal is dependent on the number of electrons scattered towards the detector by the sample surface. Metal surfaces and the edges of features scatter more of the electron beam and so these appear brighter in the image. Reference [90] shows an example where an SEM misinterprets the width of an on-mask phase-shifted structure. In the image captured by the SEM the sidewall of the etched phase-shifted element gives a stronger signal than the edge of a chrome feature and this makes the phase-shifted line to appear wider. In a FIB system the surface of a sample is imaged in a similar way to an electron beam, where the generated secondary



(a) No offset (b) With offset

Figure 3.14: *Schematic diagrams of phase-shifted structures showing no misalignment or with misaligned chrome and phase-shifting layers.*

electrons or ions are collected and analyzed as signals to form an image. Therefore the artefacts observed on the FIB images in figures 3.13(a) and 3.13(b) most likely represent a stronger signal by the edge of the sidewall in the misaligned phase-shifter.

To explain the optically wider lines of figures 3.11(a) and 3.11(b) the effect of the etched quartz step off the side of a chrome line should be considered (as shown in figure 3.14(b)). For a perfectly etched phase-shifter trench the transition from un-etched to etched quartz will result in a very narrow dark (practically zero intensity) line during exposure. In fact these features are known to print into resist when using etched-quartz PSMs. In the case of PSM3926 the positioning is off-target and the etched sidewall is probably sloping to some extent. This would blur the line caused by this edge but it would still represent a drop in optical intensity along the edge of the shifter trench. This drop in intensity will have the effect of moving the right edge of the adjacent left chrome line, as perceived by the optical metrology tool, further to the right thereby making the line appear wider. Compensating for a random misalignment via specialised calibration strategies would be practically impossible.

This is another indication of the usefulness of electrical measurements of CD on advanced photomasks where resolution enhancement features can have a negative effect on traditional metrology techniques. It is also possible that the effects seen are more of a problem when measuring CDs using an optical measurement tool operating at the wavelength for which the PSM was designed.

3.4 Conclusions

A key result from this comparison of electrical and optical CD metrology is that the ECD results from both binary and phase-shifted features track each other very closely. The optical measurements from mask PSM3920 also track each other, but with a significant offset between the binary and phase-shifted structures. This highlights the subjective nature of optical metrology where a measurement is made of an image of the structure rather than of the structure itself. The optical results from PSM3926 also show an offset between binary and phase-shifted structures for wider features but where the designed CD is less than 600nm the measurement fails and the phase-shifted lines appear significantly wider than indicated by the electrical tests.

Another issue with the optical measurements is the difference between the results from dense and isolated binary structures. While the optical and electrical measurements of the dense structures with a 1:1 LSR track each other with a reasonably constant offset, the same cannot be said for the more isolated lines with a 1:10 LSR. For dimensions below 800nm the optical and electrical results do not follow the same trend and, as the ECD measurements are not affected by proximity in the measurement, this suggests that the optical system using a single calibration reference is struggling to measure these features accurately. This indicates the need for optical tools to have a series of calibrations, each appropriate to the type and density of feature being measured. The electrical characterisation of linewidth behaviour can be seen as a means of identifying limitations in optical metrology. This will help to better understand and manage the range of calibrations that are required to support the use of optical metrology tools.

The issue with the optical measurement of the narrowest phase-shifted structures on PSM3926 is more complex. It may be that the “thick/thin” effect of the misaligned phase-shifters is more severe with optical metrology using illumination at or near the wavelength that the mask is designed. However, this study showed that it is the combination of different types of measurement methods which helped identify the misalignment between the mask layers. In the case of the electrical technique the width of the affected chrome lines could be measured accurately but the results could not suggest a fabrication problem with the non conducting phase-shifting material. The error introduced in the optical measurement was not the result of incorrectly resolved lines, as the ECD method verified, but this lead to further investigation. The

work presented, has shown that the use of more than one measurement technique, complementing each other, can prove valuable when characterising an advanced photomask process.

Chapter 4
Development of Electrical On-Mask CD Test Structures Based On Optical Metrology Features

4.1 Introduction

Industry standard inspection of feature size and shape is usually performed at the wafer level using an SEM. This provides the manufacturer with information about the deviations between the final fabricated product and the CAD layout. However, with the rapid miniaturisation that has been seen over the past few years the CAD layout must be modified to produce the desired final pattern on the wafer. This modification is known as Optical Proximity Correction (OPC) and a highly sophisticated technology has grown up around it. The correction applied addresses two major error sources, these being the errors generated at the time of mask manufacture and those from the imaging system that reproduced the mask pattern on the wafer. The standard approach to generate the data for automated proximity correction requires a set of patterned features to be measured using an optical tool or a CD-SEM.

The work presented in Chapter 4 proposes electrical test structures to characterise the photomask thereby decoupling the two error sources to produce a more accurate and reproducable final pattern. The test structures are electrical equivalents to a set of industry standard optical test sites and perform the same task with a number of advantages. These measurements are designed to extract information about proximity effects in the mask making process and to generate rules or models for the correction of the mask designs.

The first part of this chapter presents a number of structures which have been designed and fabricated on a mask plate without any correction for e-beam proximity effects [118]. The electrical test structures are based on the Kelvin bridge resistor to

measure the widths of isolated and densely packed lines and spaces. Electrical results from the test mask are presented and compared with optical measurements of the same structures made with an industry standard mask metrology tool. The second part investigates the feasibility of adapting optical patterns to electrically measure the separation between abutting ends of lines, spaces and corners and the diameter of contacts and holes. Simulations are performed to examine the sensitivity of capacitive and resistive structures to feature dimension variations and structure designs are proposed for on-mask metrology.

4.2 Test Structures and Photomask Layout

4.2.1 Optical Test Structures

The starting point for this work is a set of industry standard on-wafer metrology test patterns (version 11) provided by Mentor Graphics (MG) [119]. The isolated and densely packed line arrangements, presented in figure 4.1, are used for investigating proximity distortion effects, which in turn helps to determine the rules and calculate the parameters required for proximity correction schemes. In addition experimental data taken from measurements on such patterns are used to optimise optical lithography process simulation models. By adapting the test set for photomask metrology similar information can extracted for the mask making process. Furthermore real reference data can be used at the mask step of the lithographic models, which typically do not take in to account mask effects but assume nominal dimensions and conditions for the mask as defined in the CAD data.

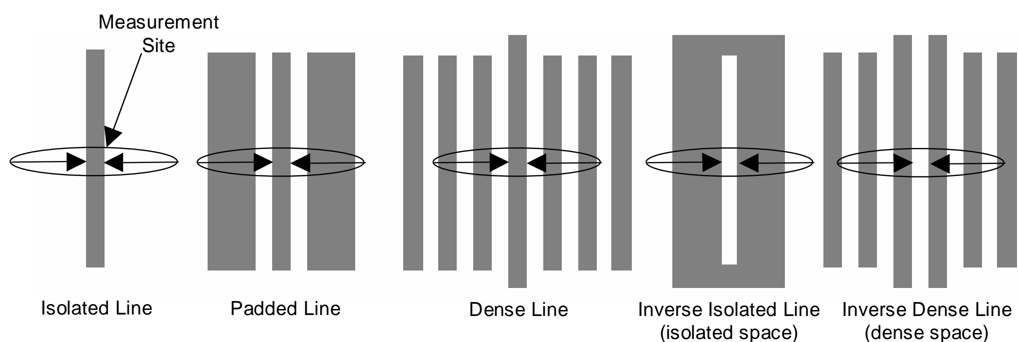
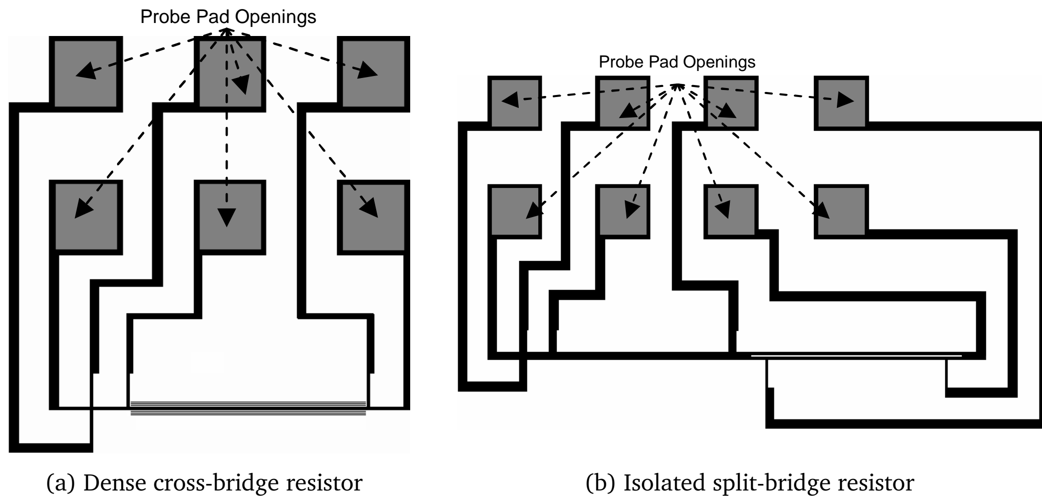


Figure 4.1: *Layouts of the Mentor Graphics optical test features.*

4.2.2 Electrical Test Structures

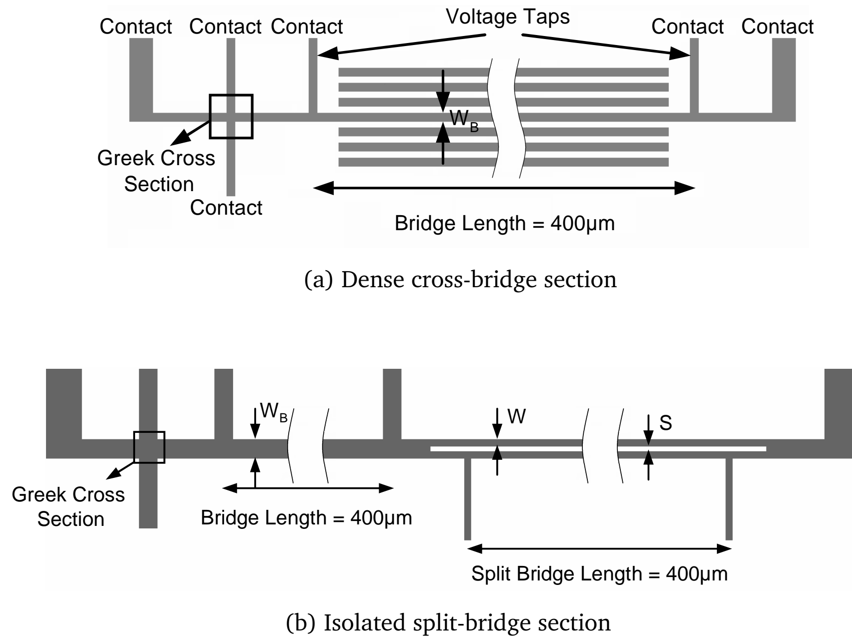
A prototype binary mask (MSN5757) was fabricated to investigate the proposed measurement test sites. It includes on-mask, electrical test structures based on the well understood cross-bridge resistor [72] and an extension of it, termed the split-cross bridge resistor [74]. The test structures are patterned into the conductive chrome layer of the photomask and their layouts are illustrated in figures 4.2 and 4.3. The photomask also includes an anti-reflective coating (ARC) of insulating chromium oxynitride and so a second level of patterning is required to remove the ARC over the pads so that good electrical contacts can be made. The nominal linewidth of a bridge is (W_B), the spacing between two lines is (S) and the width of the two half lines in a split bridge is (W). The measurement techniques for these structures have been presented in Chapter 2. To provide clear and unambiguous information about the capability of the fundamental mask making process, this mask has been written without any of the correction strategies usually applied for manufacture.



(a) Dense cross-bridge resistor (b) Isolated split-bridge resistor

Figure 4.2: *Schematic layouts of the on-mask test structures.*

The mask layout (see figure 4.4(a)) contains 9 blocks of identical test structures (A1-C3) and two blocks of large pad printable test structures designed to be measured when reduced by a 4X photolithography system. Each block (see figure 4.4(b)) consists of 108 structures which are split into 9 sets of 12 structures designed to characterise the feature arrangements presented in figure 4.1. Seven sets consist of isolated and dense cross-bridge resistors with nominal widths (W_B) ranging from 480 to 4800nm. The two



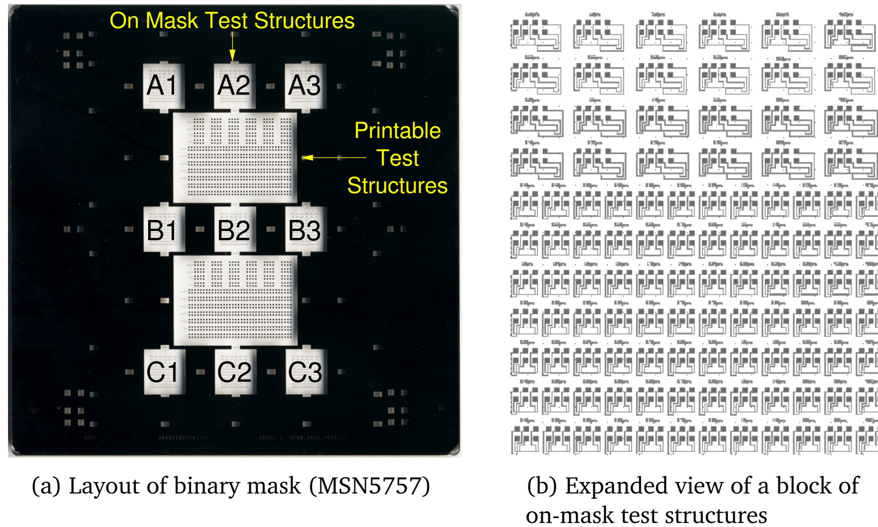
(a) Dense cross-bridge section

(b) Isolated split-bridge section

Figure 4.3: *Expanded views of the on-mask test structures.*

remaining sets consist of isolated and dense split-cross-bridge structures with nominal line-spacings (*S*) ranging from 480 to 4800nm. The dimensions of the on-mask features are four times larger than those in the Mentor test set, which are defined for on-wafer metrology. The complete range of designed dimensions for the on-mask features is listed bellow.

- Isolated set, W_B (nm): 480, 520, 560, 600, 680, 720, 880, 1120, 1480, 2120, 3120, 4800.
- Dense set, Constant W_B = 480nm, S (nm): 560, 600, 640, 680, 720, 800, 960, 1160, 1560, 2200, 3200, 4840.
- Dense set, Constant W_B = 520nm, S (nm): 520, 560, 600, 640, 680, 720, 760, 800, 840, 920, 960, 1040, 1120, 1240, 1360, 1560, 1720, 1960, 2240, 2600, 3000, 3520, 4080, 4800.
- Dense set, Constant W_B = 560nm, S (nm): 480, 520, 560, 600, 680, 720, 880, 1120, 1480, 2120, 3120, 4760.
- Dense set, Constant W_B = 600nm, S (nm): 440, 480, 520, 560, 600, 680, 840, 1080, 1440, 2080, 3080, 4720.



(a) Layout of binary mask (MSN5757)

(b) Expanded view of a block of on-mask test structures

Figure 4.4: *Layout of binary mask (MSN5757) with a close up view of one block of on-mask test structures.*

- Inverse Isolated set, Constant W = 520nm, S (nm): 480, 520, 560, 600, 640, 720, 880, 1120, 1480, 2120, 3120, 4800.
- Inverse Dense set, Constant S = 520nm, W (nm): 520, 560, 600, 640, 680, 800, 920, 1120, 1520, 2160, 3160, 4800.

4.3 Measurements and Results

Electrical measurements on mask MSN5757 were made using an HP4062B Semiconductor Parametric Test System [112] and a high resolution Solartron 7065 voltmeter [113], which has been connected to the 4062B system. The HP4062B consists of an HP4141B DC source monitor tool with four source monitor units (SMUs), an HP4280A capacitance meter, and an HP4085A switching matrix. The system is programmed and controlled from an HP9000 series 300 workstation running HP-BASIC 5.1. The current source for the resistance measurement is one of the SMUs on the HP4141B, while the voltage is measured with the Solartron voltmeter. The Solartron has a 1μV sensitivity on a range of $\pm$10mV, which is within the voltage sensing resolution requirements of this work. In addition the accuracy of the tool is within $\pm$0.001% of the measured voltage. The current through the structure is measured with another SMU on the HP4141B, in voltage source mode, which is set to

0V. The range of force currents available from one of the SMU runs from $\pm$100mA to $\pm$1000pA with a four digit resolution.

Optical measurements were made with a 248nm DUV (MueTec <M5k>) dedicated photomask CD metrology system [22, 114, 115]. This tool has been extensively characterised in a reticle production environment and demonstrated the ability to resolve sub-100nm chrome lines, with a usable measurable line and space resolution down to 200nm [22].

4.3.1 Short and Long-Term CD Measurement Repeatability

To test the repeatability of the electrical measurement technique with forced current, the ECDs of isolated lines were measured ten times, with the test structures being reprobed for each measurement. A current of 500μA was chosen as this gave the lowest short term standard deviation (σ), for currents between 10μA and 1mA. This is less than 0.4nm or a 0.05% variation, for structures with nominal CD values between 480nm and 4800nm. For long-term stability testing the electrical CDs were sequentially measured ten times each day for five consecutive days, with the structures being reprobed each day. This gave a σ_{ECD} <0.8nm, i.e. less than 0.08% variation. The purpose of longer-term repeatability testing is to observe variations which may be the result of changes in the temperature of the measurement environment or due to instrumentation drift. Whilst five days have been deemed a long-term period for the purposes of this work, repeatability verification in an industrial production environment would normally require many weeks of testing, with many measurement cycles performed each day.

Optical CD measurements were repeated three times on the same structures and gave a short-term σ_{OCD} <0.5nm for all dimensions, i.e. a variation below 0.1% for all measured linewidths. Although optical long-term repeatability testing was not performed using mask MSN5757, reference [22] reports a 3σ_{OCD} <0.5nm for sub-micron isolated lines on a binary chrome-on-glass mask measured with the same <M5k> tool.

4.3.2 Linewidth Measurements on Isolated and Dense Features

Electrical and optical CDs have been measured from one set (part of block B2) of isolated structures. The measured linewidths have been subtracted from the designed dimensions and the results are presented in figure 4.5. All of the isolated lines appear narrower than the designed CDs, but the optical and electrical results do not show the same trends. ECD results suggest that for sub-micron dimensions the fabricated lines become significantly narrower from the nominal as their design width decreases. This could be attributed to the exposure of the resist or the etching of the chrome being feature size dependent. On the other hand for nominal widths <720nm the optical results indicate an increase in feature size as the design width decreases.

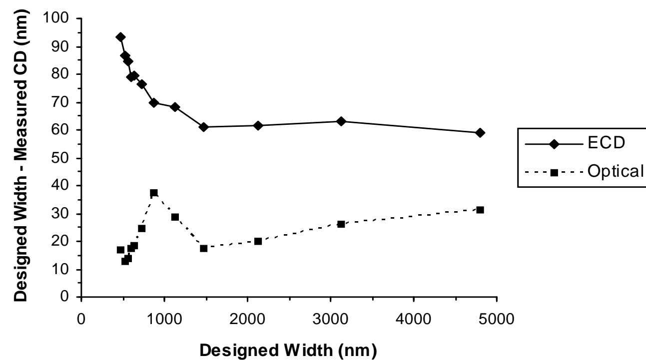


Figure 4.5: *Comparison of ECD and optical results from isolated structures for a range of dimensions.*

The optical measurements depend on the ability to obtain accurate images from which to extract the width of the features. The results suggest that this is not the case for the narrowest features, although they can be clearly resolved. One possible reason for this is that for narrow isolated features the light intensity range is reduced, however the percentage threshold is still applied. This shifts the threshold upwards in the intensity curve to a level that positions the edges of the feature at a greater distance between them making the line appear wider.

Although a multi-point calibration for isolated features has been applied to the optical tool used for these measurements, the reference mask used only allows the calibration of linewidths ≥700nm and this is directly reflected in the results. The electrical CD

offset is almost constant for dimensions wider than 1.5μm, while the optical offset increases with the designed width. This again suggests that the optical tool requires better calibration.

The electrical and optical linewidths for one set of 600nm wide dense line structures were extracted and the results are shown in figure 4.6. For line-spacings $>$1.5μm, the ECD and optical results track each other well with a nearly constant offset ($<$2nm variation for both types of measurements). The proximity of neighbouring features which are separated by over 1.5μm does not appear to affect the CD and so dense line formations at such distances can be considered isolated.

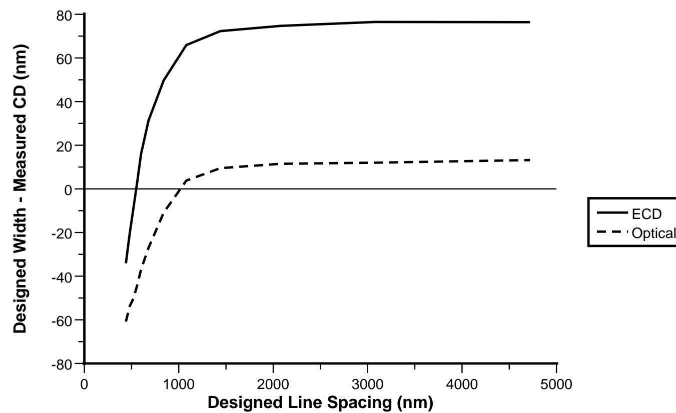


Figure 4.6: *Comparison of ECD and optical results from 600nm wide dense structures for a range of line to space ratios.*

For structures with line-spacings $<$1.5μm the CD offset decreases as the line-spacing decreases up to the point where lines appear wider than the nominal width. This is an indication that the proximity of the neighbouring features is having an effect on the CD. In addition, it can be observed that the offset between the optical and electrical measurements does not remain constant when the spacing is below 800nm. The electrical measurements indicate how proximity effects alter the dimensions of the features during the mask fabrication process, while for the optical technique this effect is also compounded with the optical measurement itself. In particular proximity effects caused by the convolution of the intensity profiles of adjacent lines introduce errors in the determination of the line edge location and thus the measured OCD, as reported in reference [120].

Calibration offsets have to be applied to the optical tool to correct for these effects. It should be noted that in this case the calibration reference plate used does not contain any dense features and so should be considered raw data. The ECD results show that the measured lines are wider than their design width when the line-spacing is less than the nominal width of the lines. In other words when the line to space ratio of the dense pattern is greater than unity, the measured lines are electrically wider than designed. It can also be observed that with optical measurements dense lines with spacings below $\sim 1\mu$m appear to be wider than the nominal CD.

4.3.3 Line-Spacing Measurements on Isolated and Dense Features

The line-spacing in the split bridge structures can be measured directly with the optical tool. The electrical measurement is more complicated and both the solid bridge width (W_b) and the widths of the two half lines (W) are required. The line-spacing S is then $W_b - 2W$. Optical and electrical line-spacing results from one set of inverse isolated structures are presented in figure 4.7.

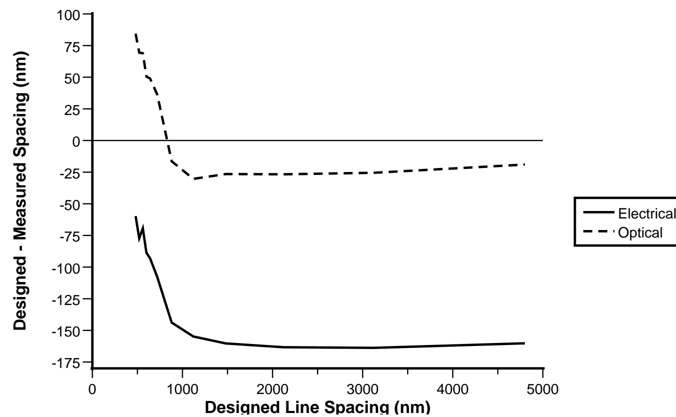


Figure 4.7: *Comparison of electrical and optical line-spacing results.*

For nominal line-spacing larger than 880nm the measured values appear wider than designed for both measurement methods. Furthermore, for spacing dimensions $>1.5\mu$m the offset is almost constant. For nominal spacing values $<$880nm there is a rapid change in the offset as dimensions reduce, but the difference between the optical and electrical measurements remains constant. For both results the extracted spacings get narrower as dimensions reduce. This is due to proximity effects between

the internal sides of the abutting tracks forming the spacing. This effectively increases the fabricated width of the lines but decreases their line-spacing. One interesting thing to note is that both techniques detect a change in the trends of the curves between 520nm and 560nm spacings. This is most clear in the electrical results and most likely represents a real effect on the mask.

The inverse dense set consists of dense line features with varying linewidths. The nominal line-spacing between the split-lines (and between the surrounding dummy lines) is 520nm for all structures. The split-lines are the two abutting half-lines of each structure defining the line-spacing under investigation. Optical and electrical line-spacing results from one set of inverse dense structures (that of block B2) are presented in figure 4.8.

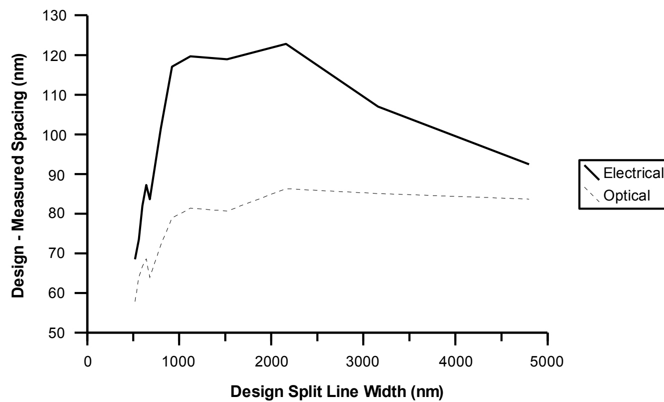


Figure 4.8: *Comparison of electrical and optical line-spacing results from dense structures.*

Both measurement techniques show the measured line-spacing to be narrower than the nominal value; however, the offset between the two methods is not constant except for a small range of split-linewidths. It can be seen that for sub-micron split-lines the offset between the measured line-spacing and the design target decreases as the width of the split-lines decreases. Since the nominal line-spacing remains constant for all structures, the split-line to space ratio decreases as the width of the split-line decreases. Split-lines with smaller split-line to space ratio appear more narrow (from the nominal) than the lines with a higher ratio. This in turn makes the measured line-spacing appear wider, causing the decrease in the offset observed in figure 4.8. The unexpected change in the trend between 680nm and 640nm tracks is most likely caused by a local effect on the mask and not a measurement error, as it has been detected by

both measurement techniques. In addition, for sub-micron split-lines the line-spacing offset between the two measurement techniques is not constant, but increases as the split-lines get wider. This effect is similar to the CD offset variations observed with the dense lines of section 4.3.2. For the optical measurement the determination of the location of the edges of a line or space feature and consequently the measured OCD, is affected by the proximity of adjacent feature edges.

It is only for linewidths between 920nm and 2160nm that the curves of figure 4.8 track each other reasonably well and with a nearly constant offset. For split-lines wider than 2160nm the optical line-spacing offset seems to level to a nearly constant value (<2nm variation). This is expected since the split-lines have become wide enough that further increases in their linewidth does not alter the effect they have on the dimensions of the spacing between them. This is not the case for the electrical results, where the offset reduces significantly. This effect is almost certainly caused by the isolated bridge which has been used as a reference for the electrical calculation of the line-spacing. The calculation assumes that the outer width of the split-lines is the same as that of the solid bridge line. This is not the case here as the split-lines are surrounded by dummy features. There are proximity effects on the inner and outer edges of the split-lines although the line-spacing calculation should only depend on the inner sides of the split-lines which become wider. The proximity of the outer edges of the split-lines with the dummy features alters the outer width of the fabricated split-lines in a different manner to that of the reference bridge line. Therefore, the trend of the electrical line-spacing is masked by the above effect for these dimensions and the optical results can be trusted more confidently. This design error was modified for the next mask, which includes proximity corrections and initial results suggest that the two techniques track each other. A detailed analysis of these results are presented in the next chapter.

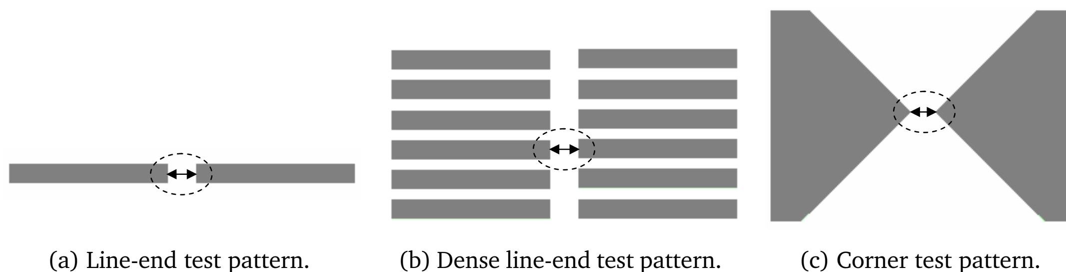
4.4 Investigation of Resistive and Capacitive Test Structures for the Characterisation of Optical Features

The complete Mentor Graphics test set includes patterns for measuring the separation between line and corner ends, as well as measuring the dimensions of contacts and holes. Distortion effects such as line-end shortening and corner rounding contribute

to the loss of pattern fidelity of features, which is critical for device functionality. This section proposes electrical test structures and their limitations, for characterising these features. This has been performed using simulations which investigate the effects of altering the critical feature dimensions.

4.4.1 Line End and Corner Patterns

The line-end and corner MG patterns presented in figure 4.9 are used to measure the separation between ends of line and corner features. The line-end test pattern consists of two adjacent lines separated by a gap (*G*). The proposed set of dimensions includes features with linewidths (W_L) ranging from 0.52 to 2.40μm and gaps ranging from 0.44 to 2.40μm. The dense line-end pattern consists of six sets of line pairs, each separated by a line-spacing (S_L). For each pair there is a gap *G* between the abutting line ends. The are two sets of lines with different widths and line-spacings and each set has a number of structures with different gaps between the line-ends. The range of the gaps is from 0.44 to 2.40μm for W_L, S_L = 0.52μm and from 0.64 to 2.40μm for W_L, S_L = 0.72μm. The corner pattern consists of two lines with triangular shaped line-ends (corners) which are separated by a gap. The range of dimensions includes two sets of lines with different widths and each set has a number of structures with different corner gaps. The range of the corner gaps is from 0.52 to 4.80μm for W_L = 0.52μm and from 0.72 to 4.80μm for W_L = 0.72μm. Simulations for chrome-on-quartz capacitive structures have been performed to investigate the use of test structures to measure the gap between the two ends of the features. The software used was the three-dimensional (*3D*) solver of the interconnect analysis software, *Raphael* [93].



(a) Line-end test pattern. (b) Dense line-end test pattern. (c) Corner test pattern.

Figure 4.9: *Mentor Graphics optical test patterns.*

For line-end patterns the simulated structure consists of two tracks on a substrate

with a gap between them. The two electrodes are connected to 1V (*E1*) and 0V (*E2*) respectively and so a single capacitance is estimated. The simulation area for such a structure is presented in figure 4.10.

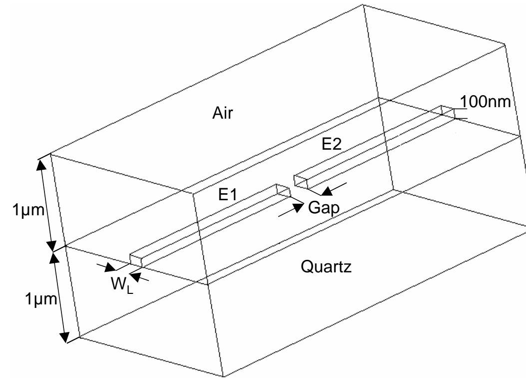
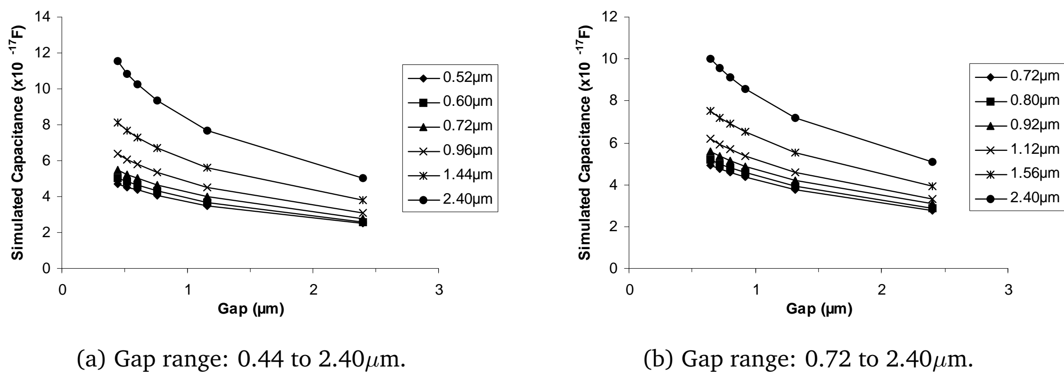


Figure 4.10: *Three dimensional simulation environment used to model an on-mask capacitor test structure for the measurement of the gap between two line-ends.*

A number of simulations for different linewidths and gaps have been performed and the results are presented in figure 4.11. These indicate that a variation of 1nm from the nominal gap between the lines will change the capacitance between the two electrodes by $\approx 10^{-20}$F. An HP 4280A 1MHZ C-Meter/CV Plotter [121] with a 0.1% accuracy on a 1fF - 1.9nF range can be used for such measurement. However, it will not detect any changes in the capacitance which are less than 1fF. Therefore, an on-mask test structure designed as indicated in figure 4.10 will not be sensitive to this magnitude of gap variation between the lines.



(a) Gap range: 0.44 to 2.40μm.

(b) Gap range: 0.72 to 2.40μm.

Figure 4.11: *Simulated capacitance against line-end gap for a range of linewidths.*

A test structure with 100,000 isolated line-end pairs as shown in figure 4.12 will have

the necessary sensitivity for the proposed measurement. For the features to be isolated, the spacing (S) between the adjacent pairs must be 1.5μm or greater. A structure consisting of the widest lines will be 390mm long, so in order to achieve a measurable change in the capacitance a narrow and long structure is required. However, the area of the standard mask plate is 152$\times$152mm and so the required dimensions make the fabrication of this structure not feasible.

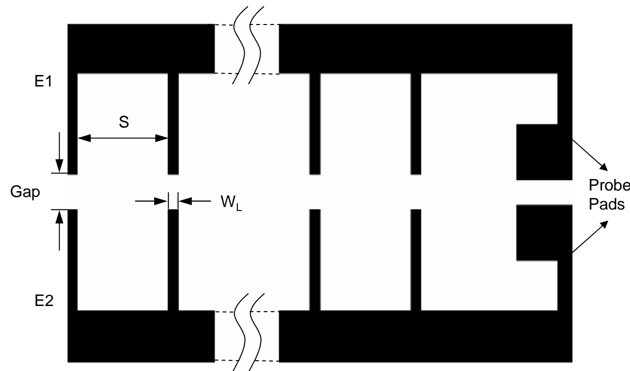


Figure 4.12: *Schematic layout of proposed capacitive test structure for measuring the gap between isolated line-end pairs.*

Similar simulations were performed for the dense line-end pattern. The simulated structure consisted of six sets of line pairs on a quartz substrate with a gap between the line-ends of each pair. The two electrodes for each line pair are connected to 1V (*T1*) and 0V (*T2*) respectively and so there are effectively six lateral capacitances. The simulation area for such a structure is presented in figure 4.13.

Simulations for different gaps have been performed and the capacitance results suggest that a variation of 1nm in the gap between the line-ends of each pair will alter the overall capacitance of the simulated structure by $\approx 5\times10^{-20}$F. If the proposed design was to be implemented, the on-mask structure would again not have the required sensitivity. To achieve the required sensitivity, the test structure should consist of a minimum of 130,000 dense-line sets. For the largest dimensions, the proposed test structure will be 187.2mm wide and therefore, as before there is a dimensional constraint preventing its fabrication on a standard mask plate.

Finally capacitive simulations were performed to investigate the use of a structure for the measurement of the gap between corners. The simulated structure consists of two tracks with triangular shaped abutting ends, on a quartz substrate with a gap between

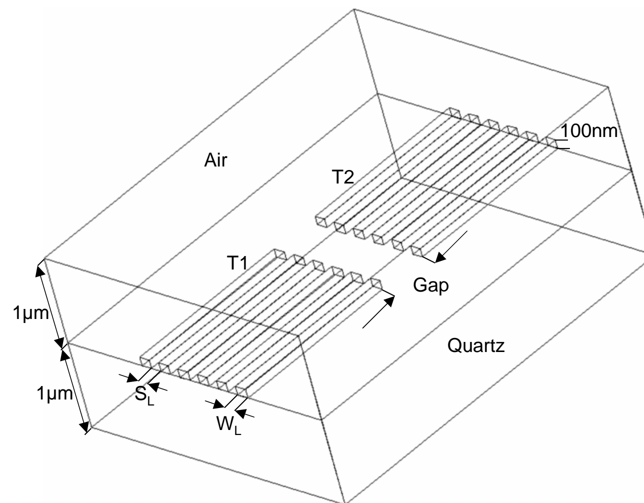


Figure 4.13: *Three dimensional simulation environment used to model an on-mask capacitor test structure for the measurement of the gap between pairs of line-ends.*

them. The two electrodes are connected to 1V (*E1*) and 0V (*E2*) respectively and so the capacitance between two tracks is derived. The simulation area for such a structure is presented in figure 4.14.

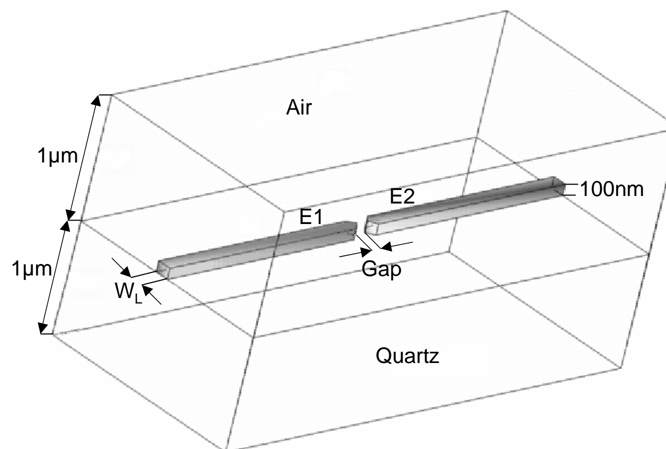


Figure 4.14: *Three dimensional simulation environment used to model an on-mask capacitor test structure for the measurement of the gap between two corners.*

Simulations for different gaps have been performed and the capacitance results indicate that a variation of 1nm in the nominal gap between the corners of the lines will alter the capacitance of the structure by $\approx 5\times10^{-21}$F. An on-mask test structure with 100,000 corner pairs will provide the sensitivity required for the measurement of the corner gaps. A variation of 1nm in the nominal gap between each corner pair, will result in

a 1fF change in the overall capacitance of the test structure. This design presents the same challenge as before, since the capacitive structures can be up to 222mm wide. Therefore in order to reach a measurable change in the capacitance, the size of the test structures will have to be larger, than what would be feasible for a standard mask plate.

Due to dimensional requirements, it would not be possible to pattern the simple capacitive structures presented so far on a standard six inch mask. The inter-digitated capacitor shown in figure 4.15, could minimise the required dimensions of the test structures. Two capacitor fingers, each having a number of lines with a spacing between them, can form line-end and corner arrangements. A large number of capacitor fingers will provide the required sensitivity for the capacitance measurements and avoid the size constraints.

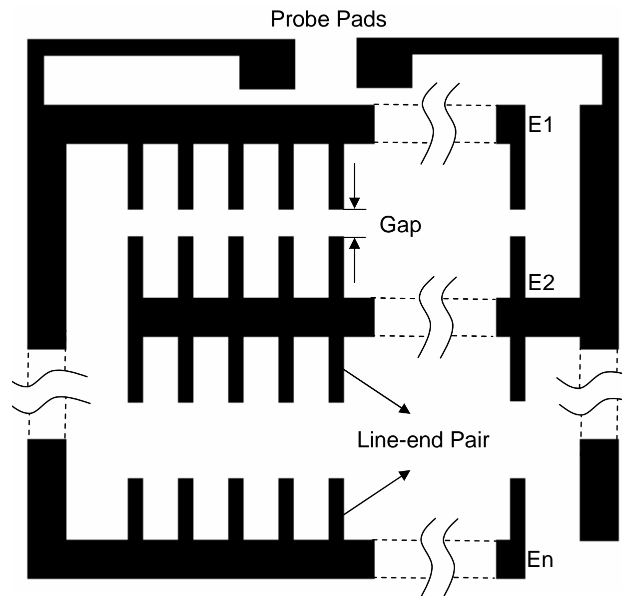


Figure 4.15: *Schematic layout of an inter-digitated capacitor test structure for measuring the gap between line-ends, for the line-end, dense line-end and corner test patterns.*

4.4.2 Inverse Line End Structure

The inverse line-end test pattern consists of a $16\times16\mu$m patch with two sections removed to form inverse lines. The pattern which measures the separation between the ends of abutting spaces can be seen in figure 4.16. The proposed set of dimensions includes features sizes, with line spaces between 0.52 and 2.40μm and inverse gaps

between 0.44 and 2.40μm. To investigate the use of a resistive test structure which will enable the measurement of the inverse gap, simulations have been performed using the two-dimensional (*2D*) solver of *Raphael*.

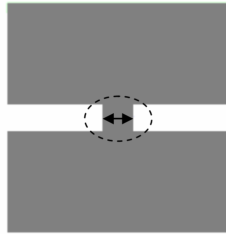


Figure 4.16: *Mentor Graphics inverse line-end optical test pattern.*

The simulated structure consists of the 16$\times$16μm patch where two probe pads have been placed at the top and bottom edges of the patch and are connected to 1V (E1) and 0V (*E2*) respectively. The simulation area for such a structure is presented in figure 4.17. The sheet resistance of the conducting material has been set to $R_S = 1\Omega/\Box$ and the current distribution and resistance of the simulated structure are calculated.

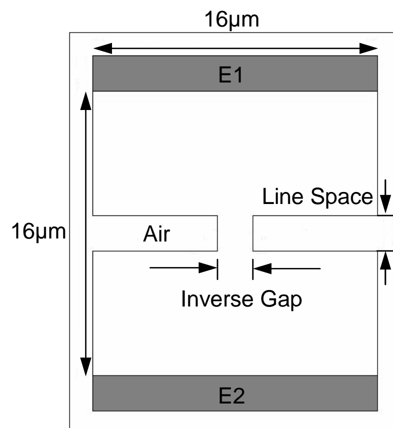


Figure 4.17: *2D simulation area used to model an on-mask resistor test structure for the measurement of the gap between the ends of line-spaces.*

Simulations for different inverse gap and line space dimensions have been performed and the resistance results are presented in figure 4.18. The simulation results suggest that a variation in the nominal inverse gap of a structure will cause the resistance to change and this rate of change increases as the line space of the structure increases. For example a 1nm variation in the inverse gap of the structure will cause a change of 0.559mΩ in the resistance of a structure with a 0.52μm line space and 1.588mΩ for one

with a 2.40μm line space. The non-linear behaviour of the results indicate that this rate of change is higher for structures with narrower inverse gaps. A method of determining whether the change in the resistance is caused by a variation in the inverse gap or the line space (length of the resistor) is required.

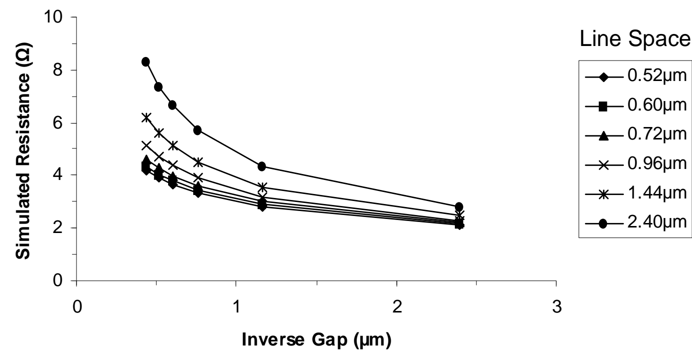


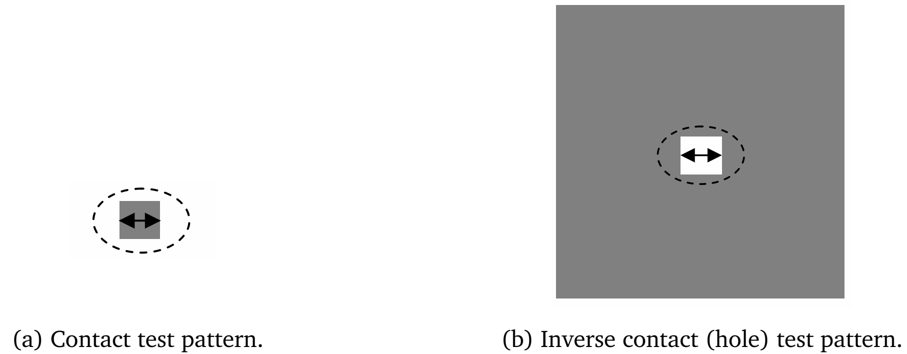
Figure 4.18: *Simulated resistance against inverse gap for a number of different line space dimensions.*

4.4.3 Contact and Inverse Contact Structures

The shape of contact holes laid out by IC designers is not faithfully transferred to the wafer. This is well known in wafer fabrication environments and is partly due to the inability of the lithographic process to resolve the corners of contacts, which as a consequence become rounded. In addition the mask pattern shape is not an ideal representation of the design data and contacts suffer from corner rounding which affects the printed wafer. These effects are not too significant at large geometries but as dimensions reduce, the corner effect becomes more dominant and the contact starts to take on a circular shape. For this reason the measurement of contact size can be very important.

The contact test pattern consists of an isolated square post as shown in figure 4.19(a), while the inverse contact presented in figure 4.19(b) consists of a 16x16μm patch with a square hole at the center of it. The proposed set of dimensions includes contacts and holes with widths ranging from 0.76 to 4.80μm.

Simulations of capacitive structures have been performed using the 2D solver of *Raphael*, to investigate the use of an inter-digitated capacitor test structure for



(a) Contact test pattern. (b) Inverse contact (hole) test pattern.

Figure 4.19: *Mentor Graphics optical test patterns.*

measuring the width of isolated chrome contacts. The simulated structure consists of two electrodes on a quartz substrate, with a rectangular post placed between the capacitor fingers. By taking advantage of the reflective boundary condition which is applied in the simulation window, the two electrodes are reduced to half of their size. The symmetry on the structure can then be exploited to accurately estimate the lateral capacitance between two interior elements, of a structure with a large number of electrode fingers. The simulation area for such structure is presented in figure 4.20. The two chrome electrodes are connected to 1V (*E1*) and 0V (*E2*) respectively and so a single lateral capacitance is estimated. The dimensions of interest are the width (W_C) of the square posts and the distance (D_{min}) from the edges of a contact to the edges of any other nearby features (D_{min} represents the minimum distance required for a feature to be considered isolated).

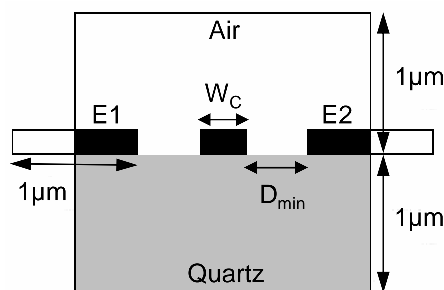


Figure 4.20: *2D simulation area used to model an inter-digitated capacitor test structure for the measurement of the contact width.*

A number of simulations for different contact widths and distances have been performed and the capacitance results presented in figure 4.21. These suggest that the

smallest capacitance change (which depends on the nominal W_C and D_{min}) caused by 1nm variation in the nominal contact width is 10^{-21}F.

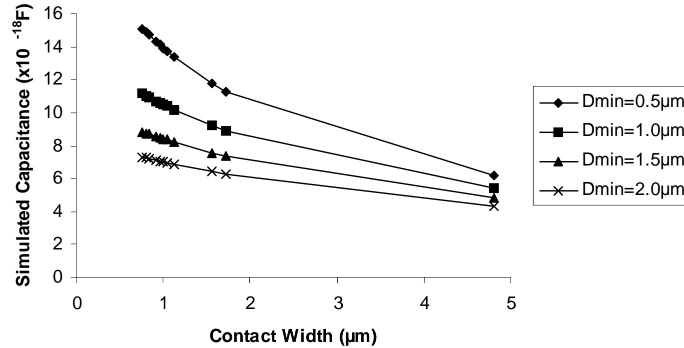


Figure 4.21: *Simulated capacitance against contact width for a number of different distance (D_{min}) dimensions.*

Therefore, to achieve the required sensitivity, the actual on-mask test structures should consist of 2000 capacitor elements (2001 electrode fingers) and the length (L_E) of each finger should be 2000μm. The layout of an inter-digitated capacitor test structure can be seen in figure 4.22. For the largest proposed feature dimension the structures will be 17.6mm wide, which is a feasible size to fabricate on a typical mask plate. The simulated data can be used to estimate the actual capacitance of the suggested test structures. To achieve this, the results of the simulations should be multiplied by 2000 to take in to account the number of capacitor elements and by 2000 to take in to account the length of the fingers. It should be noted that these simulations are 2D and therefore are for a structure consisting of 3 parallel conducting tracks. This is an approximation to the actual inter-digitated capacitor which proposes that a number of isolated square posts are placed between two capacitor fingers, instead of the simulated single continuous track.

Test structures have been proposed in a number of publications to electrically measure contact size. Freeman et al. [122] presented a digital vernier in a 2 by 12 pad array using three masking layers, that could measure the contact width. Walton et al. proposed methods of modelling the area of contact together with suggested techniques for measuring the required dimensions [123].

The technique proposed by B.J. Lin et al. in reference [94] can be used to adapt the inverse contact test pattern to an electrical equivalent. The test structure and

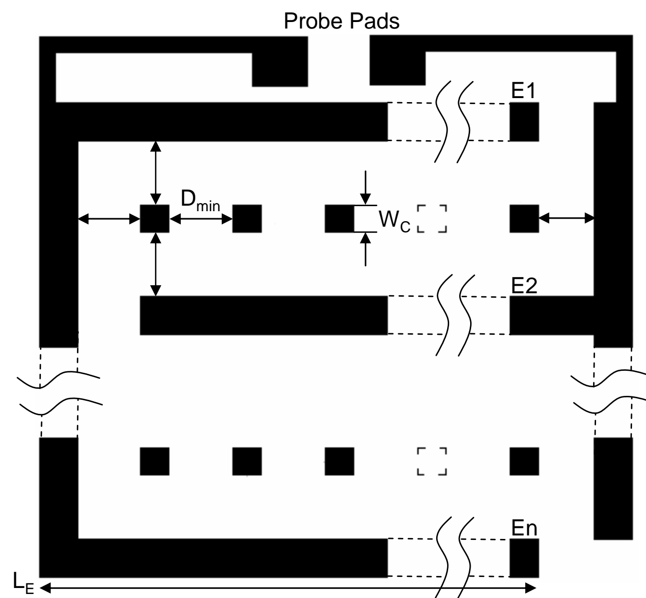


Figure 4.22: *Schematic layout of an inter-digitated capacitor test structure for measuring the contact width.*

measurement technique have been presented in Chapter 2, section 2.7.2 and measures the diameter and area of isolated contact holes. The theoretical base for the relationship between hole size and linewidth is taken from Hall's work [95]. The equation for measuring the resistance of a bar with holes has to be modified to correctly interpret the electrical linewidths. An empirical modification is taken by calibrating the measured perturbed linewidth with physical measurements. Therefore for a new test pattern or a different imaging system the coefficients would have to be recalibrated. When the hole size increases, the shape deviates from that of a circle and resembles the square shape which is constantly changing as a function of size. At this point it is not possible to derive an analytical expression and this could be the case for on-mask features which are normally 4 or 5× larger than on wafer. However, as dimensions continue to reduce the on-mask holes will also resemble the shape of a circle and the technique could be applied.

4.5 Conclusions

In the first part of this chapter, a set of optical/SEM metrology reference test sites provided by Mentor Graphics formed the basis for the design and fabrication of direct

on-mask electrical equivalents to allow the measurement of linewidth and line-spacing on these features. A prototype binary mask was fabricated with cross-bridge and split-cross-bridge test structures to measure isolated and dense patterns. Electrical and optical measurements were made and the ECD results have been shown to outperform industry standard optical mask metrology and verification methods, especially for deep sub-micron dimensions. The results suggest that the electrical technique is not affected by the type, dimension, density or the proximity of the features, unlike the optical technique where proximity effects are compounded with the measurement itself. This is very important as effects seen when electrically characterising a feature can be more confidently attributed to the mask fabrication process and not to the measurement technique. Information which is unaffected by the ambiguities that may arise with traditional light measurement techniques, can then be used to determine the rules and calculate the parameters of one dimensional proximity effect models for the correction or biasing of feature sizes.

The second part of this chapter investigated the feasibility of adapting other optical measurement patterns to electrical equivalents, which could measure the separation between line, space and corner ends, as well as the dimensions of contacts and holes. 2-D and 3-D simulations were performed to examine the sensitivity of capacitive and resistive structures to feature dimension variations. It was found that for most test patterns, an interdigitated capacitor design could have the sensitivity required for detecting any variations in feature dimensions. This test structure has a smaller footprint than the simulated capacitive equivalents, which in order to achieve a measurable change, will be too large to be fabricated on a standard photomask. In addition, a resistive structure has been proposed to detect variations in the separation between line-space ends. Finally, a test structure which is a combination of cross-bridge and modified cross-bridges structures could be used for measuring the diameter and area of contact holes.

Chapter 5
Comparison of Metrology Techniques for the Characterisation of Advanced Photomask Processes

5.1 Introduction

The use of direct electrical measurement of critical dimension on advanced photomask plates has been presented in earlier chapters of the thesis and in a number of publications [69, 88, 107, 110, 111, 118]. These have described the design, fabrication, and testing of sheet resistance, electrical linewidth and pitch test structures capable of being electrically probed on-mask. In addition to the on-mask electrical measurements, more traditional metrology techniques such as CD scanning electron microscopy [69, 88, 107] and optical CD [110, 111, 118] measurements have been evaluated. The results have demonstrated that there are serious issues with the extraction of linewidth from SEM or optical images of photomask features. This is especially true for alternating aperture phase-shifting masks, and where optical proximity effects dominate imaging.

Regardless of these results, persuading the mask-making community to integrate on-mask electrical measurements into their manufacturing process has proved to be difficult. One problem is the issue of probe needles coming into contact with the mask surface, even though the electrical structures would be located outside the exposure area, and the fact that delicate ICs are routinely probed during test. Another concern is the nonphysical nature of the electrical measurement, which could mean that effects observed do not transfer to dimensions of features on wafer. Finally, it should be noted that although a traceable standard for photomask linewidth is available from NIST [124] it is not employed throughout the industry and maskshops tend to still carry out individual correlation exercises with each customer.

This chapter demonstrates the strength of on-mask electrical measurements to

characterise advanced photomasks and compares the measurement results with state-of-the-art metrology tools. The first section picks up from the work presented in Chapter 4, which adapted industry standard optical metrology patterns into electrically measured, on-mask test structures. A binary plate (MSN5757 - No PEC), written without any corrections for e-beam proximity effects, was electrically and optically measured, to investigate a fundamental photomask fabrication process. This section describes the design and fabrication of binary, on-mask electrical test structures on a chrome-on-quartz plate that was written using the GHOST proximity correction technique [46]. Results from the electrical and optical measurements made on the test structures, have been used to examine the effectiveness of this method of e-beam proximity correction and to further evaluate the performance of the electrical and optical metrology methods.

A subset of the electrically adapted structures were then measured using one of the few CD atomic force microscope tools in the world that is fully calibrated to a CD reference standard [125]. The second part of this chapter presents a comparison of CD-AFM measurements with electrical and optical metrology results [126, 127]. In addition, an analysis of the uncertainties involved in the different measurement techniques is presented in order to aid comparison of the measurements. This analysis is based on the methods described in reference [128], which compared different metrology techniques used to measure submicrometre, single crystal silicon features.

5.2 CD Measurement Techniques for the Characterisation of GHOST Proximity Corrected Features

5.2.1 Test Structures and Photomask Fabrication

A GHOSTed binary mask (MSN6659 - GHOST) was fabricated, in an attempt to correct the proximity effects normally introduced in a standard e-beam lithography exposure [118]. The GHOST technique works by performing a second exposure where the inverse of the main pattern is written with a defocused electron beam of lower dose. The beam conditions for the correction exposure are adjusted to mimic the shape of the backscatter energy distribution produced by the design pattern exposure [46]. The backscattered electron energy dose received by all points in the pattern is equalised,

resulting in a pattern that will have an energy distribution within the resist that is roughly uniform. A schematic of GHOST is shown in figure 5.1. This is intended to produce features which are largely free from proximity induced CD variations.

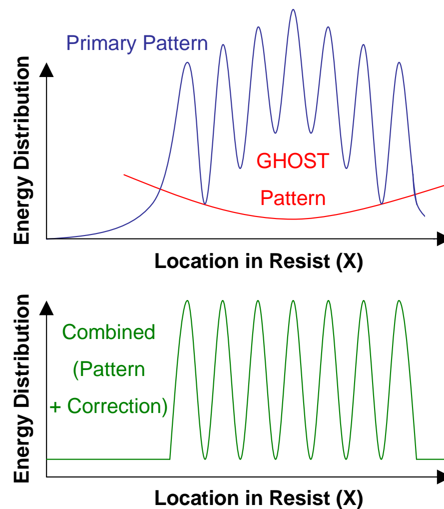
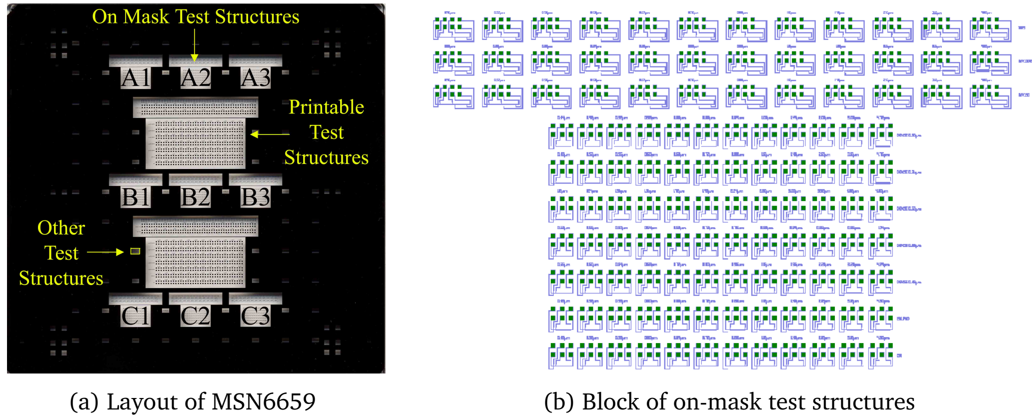


Figure 5.1: *Schematic showing how GHOST can be used for proximity effect correction.*

Mask MSN6659 [129] includes 9 identical blocks (A1-C3) of on-mask, electrical test structures and two blocks of printable versions. Figure 5.2(a) is an image of the mask, which also includes mismatch resistor structures [130], while the layout of a block of on-mask structures is presented in figure 5.2(b). This design consists of 120 structures split into 10 sets of 12 structures. Nine of the sets consist of isolated and dense, dark and clear line combinations, which are identical to the test structure designs on mask MSN5757 [118] presented in Chapter 4. The design of the cross-bridge [72] and split-cross-bridge resistors [74] has been adapted from isolated and dense, line and space optical test sites supplied by Mentor Graphics. These are normally used by the mask making industry to investigate proximity effects or other fabrication artifacts, to improve the current proximity correction models and thus increase the dimensional agreement between rendered and designed features. A full description of these optical test features can be found in Chapter 4 [118].

However, unlike MSN5757 each set of split-bridge structures on MSN6659 is confined within a single row to minimise any CD variation due to the position of the test structure on the mask. As these structures are used to characterise fabrication effects that are



(a) Layout of MSN6659

(b) Block of on-mask test structures

Figure 5.2: *Layout of the binary mask with a close up view of one block of on-mask test structures.*

proximity or dimension dependent, it is consequently very important to minimise any other CD variations, which may be introduced during the writing process. Hence, another alteration from the original design is that on MSN6659 the width of the bridge voltage taps (W_t) is always equal to the minimum CD (480nm for this mask). This was not the case for MSN5757 where $W_t = W_B$ (i.e., the designed linewidth of the measured line). By keeping the width of the voltage taps at the smallest possible dimension the electrical measurement error caused by current shunting at the taps is minimised [66].

5.2.2 Linewidth Measurements on Isolated and Dense Features

Electrical and optical measurements were performed using the same tools as those used in Chapter 4. Detailed information on the procedures employed to measure the cross-bridge and split-bridge structures can be found in Chapter 2.

The linewidths for a set of isolated structures were measured electrically and optically. The measured widths have been subtracted from the nominal widths and the results are presented in figure 5.3. The electrical results from similar structures on MSN5757 are also included for reference and the two measurement techniques track each other well for nominal CDs $>$1500nm. These results show that the fabrication process is independent of the feature dimension. For linewidths $<$1500nm both measurement techniques suggest that the lines appear wider as dimensions reduce. However, the

optical method indicates that lines become wider at a much faster rate. This again shows how ambiguities in the optical measurement may affect the interpretation of the capability of the mask making process.

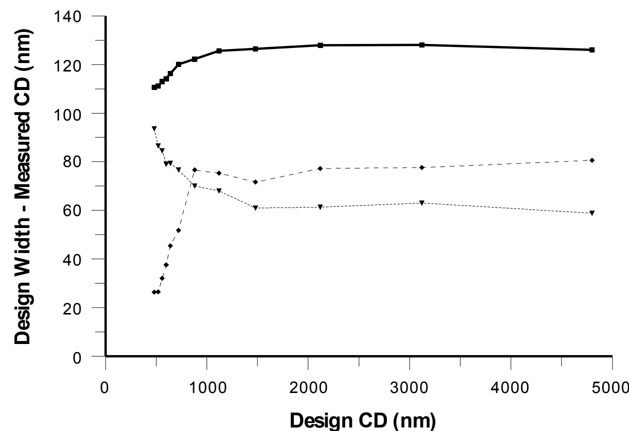


Figure 5.3: *Comparison of ECD and optical results for a set of isolated cross-bridge structures (GHOSTed MSN6659) with reference ECD measurements from a standard exposure mask (MSN5757).*

For CDs >1500nm the ECD results from the GHOSTed lines and those on MSN5757 track each other well. The offset between them indicates that fabrication process parameters, such as resist development time, need to be changed to accommodate the GHOST exposure. For linewidths <1500nm, and in particular for sub-micron features, the fabricated dimensions become non-linear. On MSN5757 forward and backward electron scattering through the resist causes narrow sub-micron lines located between large clear areas to receive more electrons (i.e. a greater dose is delivered to the resist by the e-beam tool) and thus become overexposed. For isolated lines the inverse image in the GHOST process is an isolated space. Narrow isolated space features would normally lose most of their electron energy due to scattering and will develop incompletely. Therefore, superimposing the correction exposure on the pattern exposure will result in a reduced energy dose and incomplete development. This effect appears to be causing sub-micron isolated lines on MSN6659 to become wider as the nominal dimensions reduce.

Measurements were made on dense line structures and the results from the set of 520nm wide lines are presented in figure 5.4. For all features the nominal width of

the measured line is 520nm, while the line-spacing (*S*) between the measured and surrounding dummy lines varies. For reference purposes the electrical results from the same structures on MSN5757 are included.

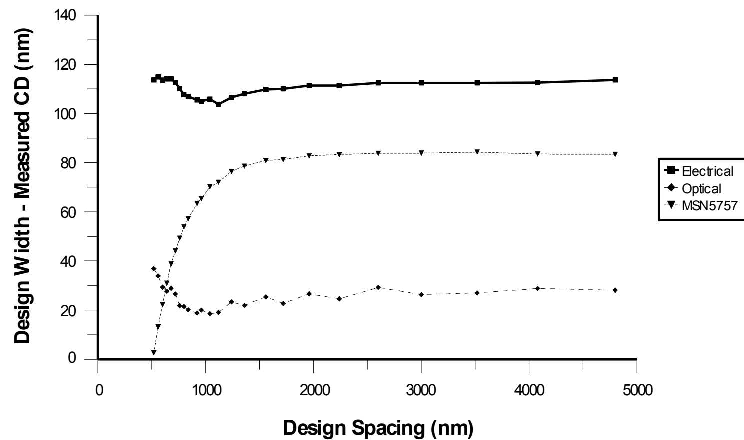


Figure 5.4: *Comparison of ECD and optical results for a set of 520nm wide dense cross-bridge structures (GHOSTed MSN6659) with reference ECD measurements from a standard exposure mask (MSN5757).*

While for $S < 1500$nm proximity has a very clear effect on the fabricated lines of MSN5757, the results from MSN6659 indicate that the GHOST correction appears to be effective, particularly above one micron. For sub-micron *S*, although there are still proximity related effects with the GHOSTed results, the CD range of the fabricated lines has reduced significantly from that of MSN5757. The effect seen on the lines of MSN6659 is most likely related to the secondary exposure of the GHOST technique. The inverse of a dense line pattern is a dense space pattern that produces an energy distribution approximating that caused by backscattering on the primary pattern. The sum of the exposures would ideally result in a constant energy distribution across the dense pattern. However, there is obviously a dimensional variation for the narrowest spaces which appears to be density dependent. The measurement results for other CDs presented in figure 5.5 show that there is also a clear dependance on design linewidth. One explanation for this is that the total energy dose delivered to the resist is above or below the ideal uniform dose and this is dependent on the nominal linewidth and line spacing.

The dense set consists of four groups of structures, each with features of equal design

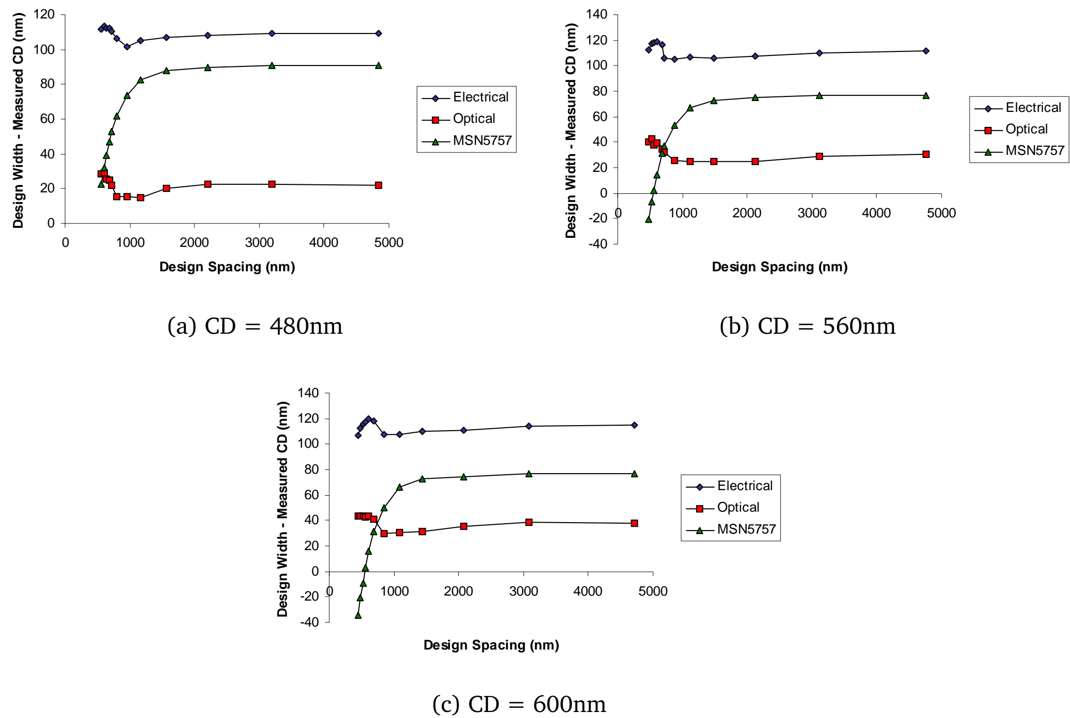
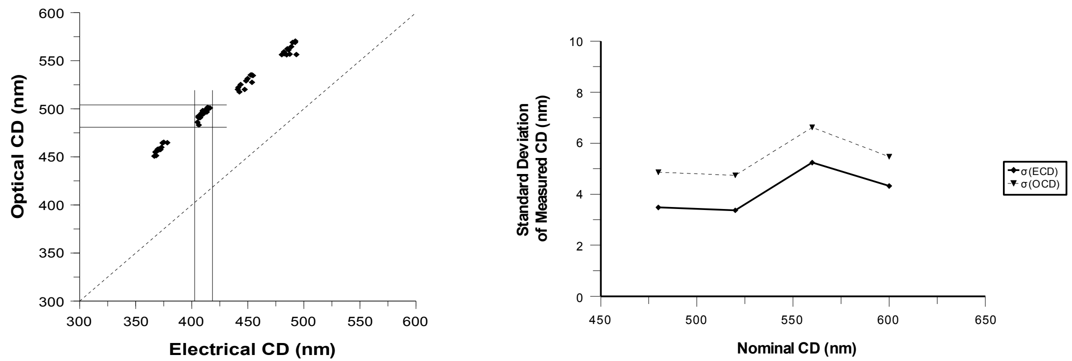


Figure 5.5: *Comparison of ECD and optical results for three sets of dense cross-bridge structures (GHOSTed MSN6659) with reference ECD measurements from a standard exposure mask (MSN5757).*

widths and varying line-to-space ratios. A correlation plot between electrical and optical measurement results can be used to visualise the data from all groups of structures. This is presented in figure 5.6(a) for MSN6659 and suggests that the variation of the ECD measurement results is smaller than the variation of the OCD results. To confirm this, the standard deviations (σ) of the measured CDs for each group of dimensions have been calculated for the electrical and optical measurements and the results are plotted in figure 5.6(b).

It would be expected that the linewidth variability and therefore the standard deviation values would remain nearly the same for both measurement techniques. However the standard deviation for each group of OCD measurements is higher, by over 1nm, than that of the ECD measurements. This suggests that there is an error associated with the OCD measurement, which is caused by optical proximity effects between the measured and surrounding dummy patterns of the dense feature. Although the GHOST correction scheme reduces proximity effects significantly, it cannot yield ideal features and the



(a) Correlation plot between ECD and OCD measurement results

(b) Standard deviation of ECD and OCD measurement results against design linewidth

Figure 5.6: *Comparison of electrical and optical measurement results for four groups of dense features with similarly sized CDs on different duty cycles, on MSN6659.*

fabrication process will be characterised by a proximity based non-linear CD transfer. This can be seen in figure 5.6(a) as linewidth variations between dense features of nominally equal widths and different design densities. However the fabricated range of dimensions for each base CD is reduced with GHOST when compared to the correlation plot for MSN5757 presented in figure 5.7.

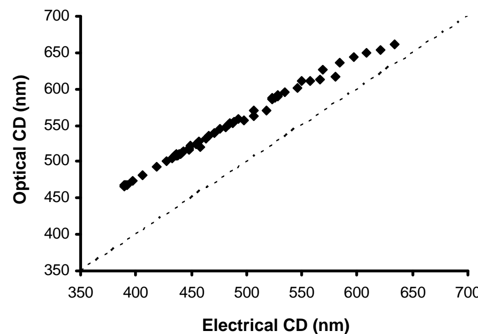
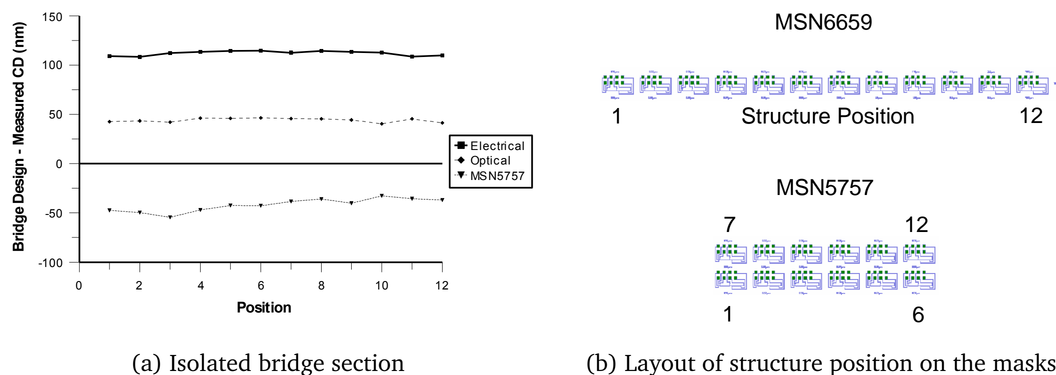


Figure 5.7: *Correlation plot between ECD and OCD measurement results (MSN5757).*

5.2.3 Line-Spacing Measurements on Isolated and Dense Features

In order to electrically measure the line-spacing associated with a split-bridge structure, firstly the widths of the solid line (W_B) and the split-line (W_S) have to be measured. The line-spacing is then $S = W_B - W_S$. Figure 5.8(a) shows the measurement results

of the, nominally 16μm wide, solid line sections of an inverse isolated line (i.e. isolated space) set on MSN6659; reference ECD results from a similar set on MSN5757 are also presented. The designed solid bridge width is equal for all structures, so the results are plotted against the on-mask position of each structure, as illustrated in figure 5.8(b). It can be seen that the ECD variation between each set is significantly reduced for the corrected mask with σ = 2.3nm on MSN6659 compared with 6.6nm on MSN5757. Unlike MSN5757 there is also no change in the measured CD with position. These effects are most likely related to the fact that the structures on MSN6659 are located in a single row, while those on MSN5757 are located across two rows. Finally, the width of the taps has been reduced from 16μm on MSN5757, to the minimum feature dimension on the GHOSTed mask. This is at least part of the reason that the lines on MSN5757 appear electrically wider than those on MSN6659.



(a) Isolated bridge section

(b) Layout of structure position on the masks

Figure 5.8: *Comparison of ECD and optical results for the solid bridge section from a set of inverse isolated (space) structures (GHOSTed MSN6659) with reference ECD measurements from a standard exposure mask (MSN5757).*

Figure 5.9 presents the ECD results from measurements made on the split-line sections of the same two sets of inverse isolated structures. Note that as the design CD of the split-lines increases, the line-spacing between them decreases. The results from the non-GHOSTed lines show that due to proximity effects there is an increase in the ECD of the split-lines whose nominal width is >14.5μm (i.e. $S < 1500$nm). The GHOSTed results show that the lines appear to have been corrected for proximity induced effects and this is the case for split-lines up to 15μm. Hence, when S is greater than 1000nm, the GHOST technique is at its most effective and the width of the fabricated lines is similar to features which are largely free from proximity induced CD variations.

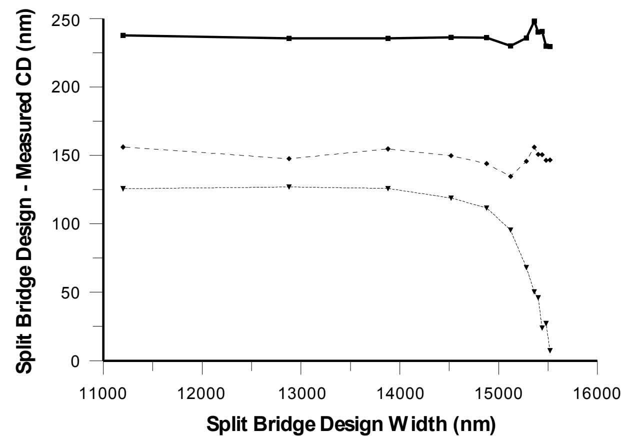


Figure 5.9: *Comparison of ECD and optical results for the split-bridge section from a set of inverse isolated (space) structures (GHOSTed MSN6659) with reference ECD measurements from a standard exposure mask (MSN5757).*

For sub-micron line-spacings the rate of change of ECD on the uncorrected lines increases significantly as S reduces. In addition, for the GHOSTed lines the correction exposure has partially compensated for proximity. However, the linewidth variation across these features is greatly reduced. The inverse pattern of a two-line and space combination (i.e. an isolated split-bridge) is an isolated line. For the dimensions discussed here the inverse pattern consists of narrow sub-micron lines which suffer from scattering effects and receive a higher energy dose than the ideal. Therefore the total energy dissipated in the patterns is still not uniform. However, this is a better approximation to the nominal than the uncorrected version.

Once the two bridge sections have been measured, the electrical line-spacing can be calculated. Figure 5.10 shows the line-spacing results for the structures on MSN6659 and the reference electrical results from MSN5757. The results from MSN5757 illustrate that for two closely spaced lines (nominal $S < 1500$nm) the space between them is underexposed and appears narrower than normal. Although these spaces are approaching their design target this is misleading as they are actually moving away from the mean fabrication process target. To investigate the dimensional offset from design targets in a fabrication process, features that do not suffer from proximity effects should be considered. In this case the wider line-spacings ($>$1500nm), which also appear to have the highest offset, should be the point for comparison.

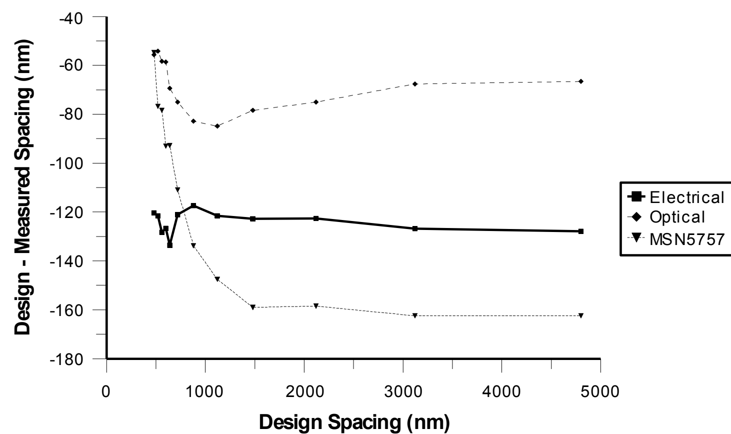
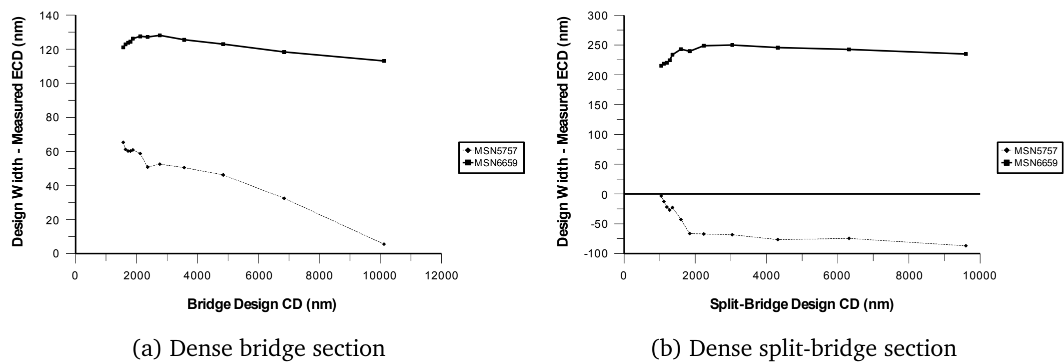


Figure 5.10: *Comparison of electrical and optical line-spacing results from a set of inverse isolated (space) structures (GHOSTed MSN6659) with reference ECD measurements from a standard exposure mask (MSN5757).*

The line-spacing results from MSN6659 show that GHOSTing is most effective for spaces >1000nm. These dimensions are normally affected by proximity, although not as severely as narrower dimensions. In this case the correction process can achieve a relatively uniform energy distribution across the pattern. Although the technique has not completely corrected the features for sub-micron dimensions, the range of line-spacing results is greatly reduced. The trend of the data in the sub-micron region is most likely related to a feature size dependent energy distribution achieved from the combination of the primary and inverse exposures. That is, the sum of the two exposures produces an overall energy dose that is either below or above the nominal distribution.

Figure 5.11(a) presents the results from electrical measurements made on the bridge sections of an inverse dense (space) set (reference results from a similar set on MSN5757 are also included). Although the structures on both masks investigate dense spaces, their solid bridge sections not only differ in their fabrication process but also at their design level. The features on MSN5757 are isolated lines. However, as this was a design error the bridges on the new mask are all dense, with a 520nm nominal spacing between them. The lines on MSN5757 show a decrease in the offset between design and measured ECD, which appears to be feature size dependent and this would be expected for narrower dimensions. However, for dimensions $>1\mu$m the CD offset should remain nearly constant. This is most likely related to the design width of the

bridge voltage taps which are wide enough to cause a line to appear electrically wider than is the case. For the dense lines on MSN6659 the tap effect has been eliminated, but the trend of the curve suggests that the width of the fabricated lines depends on their base CD and line-spacing. Due to GHOSTing the widths of these lines also depend on the inverse pattern exposure, which in this case is narrow (520nm) lines with wide spaces between them. Figure 5.11(b) shows the ECD results from measurements made on the split-lines of the same sets of structures.



(a) Dense bridge section

(b) Dense split-bridge section

Figure 5.11: *Comparison of ECD results from a set of inverse dense (space) structures on a GHOSTed (MSN6659) and a standard exposure mask (MSN5757).*

For design linewidths >2240nm, the ECD offset between the two sets remains nearly constant. Although there are proximity related effects for these split-lines, their design CD is sufficiently wide to keep this effect minimal. By design, when the CD increases so does the line to space ratio. When the line to space ratio increases the lines get wider, which is also the case here although at a very slow rate. For a base CD <1600nm the results from the two masks do not agree. The uncorrected split-lines appear narrower as their design width decreases. In addition, line to space proximity reduces significantly for narrow dimensions making the effects more apparent. This means that the fabricated split-lines get narrower at a faster rate, the line-spacing between them becomes also wider at a faster rate. This effect is reversed for the split-line results on MSN6659 where the lines become wider when their nominal CD decreases. Again this is related to GHOST and the exposure of the inverse pattern, which is used to equalise the energy distribution across the pattern. The inverse pattern of a dense split-bridge is a dense space pattern and superimposing this inverse exposure on the main exposure appears to result in an energy distribution which resembles that of the inverse pattern. Therefore the results of the GHOSTed split-lines are similar to the line-spacing results

for the uncorrected fabrication process.

Figure 5.12 compares the electrical and optical results from measurements on the spacings between the split-lines on MSN6659 and similar structures on MSN5757. The first thing to notice, is that due to the design error with the structures on MSN5757 the assumption that the outer widths of the bridge and split-bridge sections are equal was not valid. This led to errors and misleading trends with the electrical line-spacing offset for the widest split-lines, which has been corrected for the GHOSTed mask. For split-line CDs >2240nm the results of the spacing curves track each other well with a constant offset (both measurement techniques and fabrication processes with the exception of the electrical results on MSN5757). This is expected since the split-lines are wide enough that any further increase in their linewidth does not alter the proximity effects they have on the dimensions of the spacing between them.

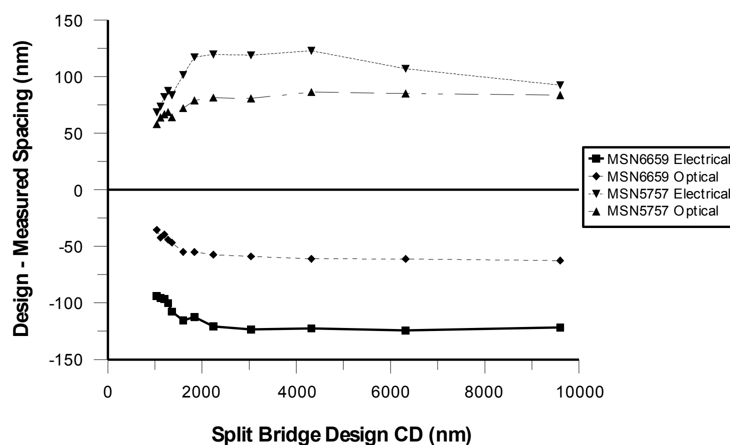


Figure 5.12: *Comparison of electrical line-spacing results from inverse dense structures on masks MSN5757 (optical results included for reference) and MSN6659.*

For split linewidths <1840nm the line-spacing results of the two masks exhibit different trends. On MSN5757 the measured spacing gets wider as the nominal width of the split lines decreases. Since the nominal line-spacing (520nm) remains constant for all structures, the split-line to space ratio decreases as the width of the split-line decreases. Split-lines with smaller split-line to space ratios appear more narrow (from the nominal) than the lines with a higher ratio and this causes the spacing between them to appear wider. On the other hand the line-spacing results from MSN6659 appear to get narrower as the design CD of the split-lines is reduced. In fact this is the same

trend that the split-line results of the uncorrected mask follow (see figure 5.11(b)). In addition a split-line is the inverse pattern of the spacings under investigation. This suggests that when the energy dose from the inverse pattern exposure is superimposed with that of the main pattern exposure it does not create a uniform energy distribution across the pattern. Instead it creates an energy signature that resembles that of the inverse pattern. Finally the range of CD and spacing offset for the proximity affected results has only been reduced by a small fraction. This suggests that the GHOST technique has encountered problems with the correction of the dense features in the inverse dense set.

5.3 Comparison of Measurement Techniques for Sub-micron Linewidth Photomask Metrology

5.3.1 Test Structures

The photomasks used for the work presented in this section are MSN6659 and MSN5757. Both masks have the same test structures and are from similar mask blanks but the fabricated linewidths are slightly different due to the GHOST processing on MSN6659. The on-mask electrical test structures are based on optical/SEM metrology features used to measure iso-dense proximity effects and examine proximity correction techniques on binary photomasks [118, 119, 129]. The basic electrical structure is the cross-bridge resistor [72] and the measured features are isolated lines with nominal CDs of: 480, 520, 560, 600, 680 and 720nm.

5.3.2 Electrical Measurements

The sheet resistance (R_S) of the chrome layer of the mask is measured using the Greek cross structure and the method is described in Chapter 2. For this work the sheet resistance measurement procedure is repeated five times with a force current of 500μA and the results averaged. The average standard deviation over the five measurements was determined from a set of 200 measurements with a 10 minute delay between each group of five. This was found to be about 2.8m$\Omega/\square$ for an average sheet resistance of 22.47$\Omega/\square$. The overall variability for that set of the measurements (3σ) was 22m$\Omega/\square$

or about 0.1%.

The cross-bridge resistor is used to measure the resistance R_B of the 400μm long bridge section on these structures. The complete measurement method can be found in Chapter 2. A similar set of 200 measurements of the bridge resistor showed a 3σ variability of 2.6Ω for an average resistance of 22102Ω (I_{Forced} = 500μA). The repeatability figures for sheet resistance and bridge resistance measurements translate into linewidth uncertainties of 0.4 and 0.05nm, respectively, for an average ECD of 406.7nm (nominal CD = 480nm). It should be noted that the measurements of repeatability were performed on mask MSN5757.

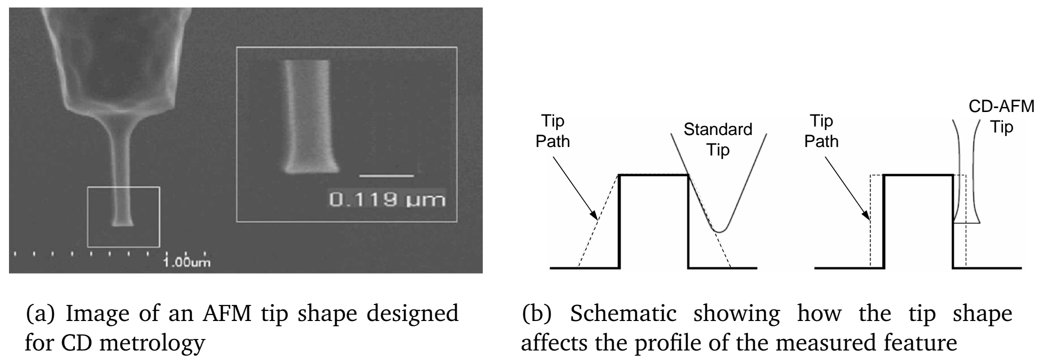
5.3.3 Optical Measurements

Optical CD measurements have been made using a MueTec <M5k> mask metrology system with 248nm ultraviolet illumination. This captures an image of a feature on the mask, always in transmission at 248 nm, and determines the CD [22,114,115]. This is a subjective measurement requiring careful calibration and it has been demonstrated that this technique has problems when measuring phase-shifted masks [110,111] or isolated features below 700 nm [118], as a consequence of the calibration methodology used in these references.

5.3.4 CD-AFM Measurements

CD-AFM measurements were performed using a Veeco SXM320 at the National Institute of Standards and Technology (NIST). This tool is effectively a three-dimensional (3D) AFM where the deflection of the tip can be measured in-plane as well as out of plane. The tip itself does not come to a point like a standard AFM tip but instead is wider at the bottom, which enables it to directly measure the shape of features with vertical or re-entrant sidewalls. This is shown in figure 5.13. The tip width of this instrument is calibrated using a single crystal, critical dimension reference material (SCCDRM), which was developed at NIST and has atomically flat side walls making it easy to extract the shape of the AFM tip. This calibration enables the CD-AFM tool to perform linewidth measurements with expanded uncertainties as low as 1.5nm (k = 2) [125, 131].

The AFM measurements were obtained near the center of the bridge resistor. However,



(a) Image of an AFM tip shape designed for CD metrology

(b) Schematic showing how the tip shape affects the profile of the measured feature

Figure 5.13: *Comparison between standard and CD-AFM probe tips.*

this positioning is only approximate due to the length of the structures and the absence of nearby navigation markers. Twenty AFM scan lines are taken over a 1μm length of track and the average width is calculated. An example of a scan can be seen in figure 5.14. The first stage in the measurement is to subtract the tip shape which is found by scanning the reference feature after each measurement. This also helps to evaluate the uncertainty associated with the wear on the AFM tip. Next the width is measured at the top (TW), middle (MW) and bottom (BW) of the line and an average linewidth is extracted. The results from a 480nm bridge are presented in table 5.1; the average width is 373.97nm and the average standard deviation (σ) is 5.31nm.

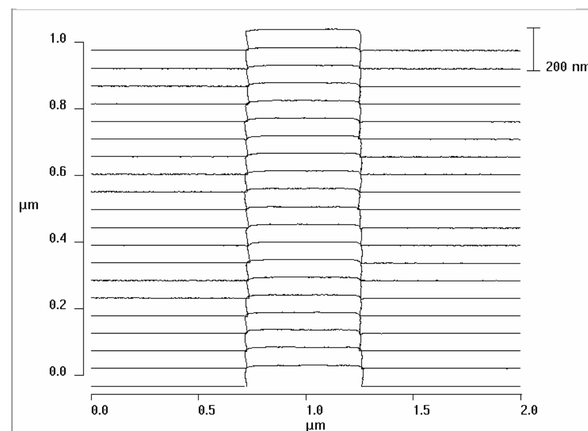


Figure 5.14: *A 2μm by 1μm AFM scan area.*

The typical standard deviation of the 20 measurements is 5-7nm. The expanded uncertainties of the values as measured by the AFM ranged between 1.7 and 3.8nm, with tip wear driving the larger uncertainties. However, it should be noted that these

	Top (nm)	Middle (nm)	Bottom (nm)
Average	379.21	377.28	365.43
Standard Deviation	4.79	5.65	5.5

Table 5.1: *Measured linewidths at the top, middle and bottom of a feature.*

estimates do not include the uncertainty resulting from linewidth roughness (LWR). In order to investigate any longer range changes in linewidth one of the structures was remeasured at five different positions, about 70μm apart, along the length of the bridge.

5.3.5 Results

Due to the length of time required for CD-AFM measurements these results only cover the narrowest of the isolated linewidth structures. There are also difficulties with the measurement of dense features using the CD-AFM due to the shape of the tip. As a result, there are measurements from six isolated cross bridge structures with designed linewidths between 480 and 720nm. These results are plotted along with ECD and OCD results in figure 5.15. It should be noted that this graph shows the measured CD subtracted from the designed linewidth.

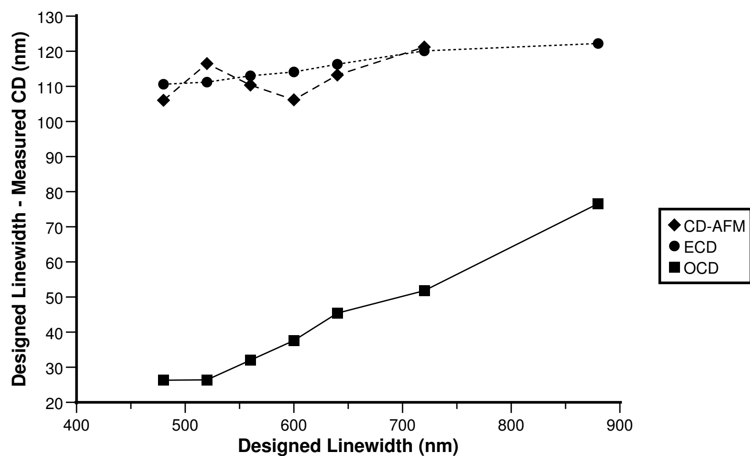


Figure 5.15: *Comparison of optical, electrical and AFM metrology.*

The results show excellent agreement between the CD-AFM and ECD measurements, but a significant offset between them and the optical CD results. The level of agreement between the electrical and standards calibrated CD-AFM results is surprisingly good. It is expected that there would be a systematic offset between any two measurement

techniques, associated with the type of measurement used [132–134]. The variation of the AFM results away from the smooth trend of the ECD measurement can be explained by noting that the AFM measurement is looking at a relatively short (1μm) length of the bridge while the electrical results give the average width of a 400μm long line.

In order to investigate this, further measurements were made at five different positions along a bridge structure with a nominal width of 520nm. This is the second point for the CD-AFM in 5.15 with a measured width of 403.5nm. These measurements were made using an AFM tip with significant wear so they should be considered as indicative of the variation of width along the line rather than of absolute CD. The results have been normalized to the value for the center of the line given above (i.e., 403.5nm) and are presented in table 5.2, along with the standard deviation of the twenty individual measurements made at each position. Note that the column labeled “Distance” gives the approximate position of the AFM measurement along the measured line. These results suggest that the variation of linewidth at this long range is very small and is of a similar scale to the standard deviation of the individual measurements at each point.

Distance (μm)	Width (nm)	Standard Deviation (nm)
60	404.92	7.95
130	402.15	5.92
200	403.51	7.88
270	400.55	7.22
340	400.28	4.96

Table 5.2: *CD-AFM measurements made at five different positions.*

Figure 5.16 is a more direct comparison of the three different measurement methods. It shows the differences between the measurement results plotted against the CD measured with the NIST CD-AFM. The offset between the ECD and AFM results is less than 10 nm for each of the test structures and does not display an obvious dependence on the width. This is not the case for the optical results where the offset is significantly larger and also seems to reduce as the dimensions increase.

5.3.6 Analysis of Electrical Measurement Uncertainties

Electrical linewidth repeatability measurements of structures on mask MSN5757 were made using a Hewlett Packard, HP4062UX [135]. This is a production semiconductor

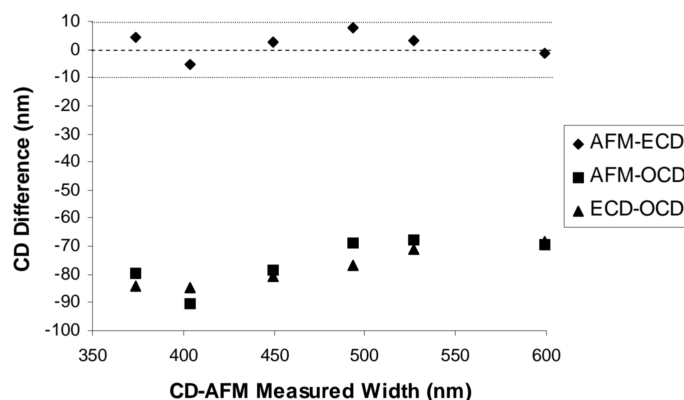


Figure 5.16: *Linewidth measurement offsets for isolated structures.*

characterization system consisting of an HP4142B modular source monitor tool [136], an HP4280A capacitance meter, and an HP4085B switching matrix. The system is programmed and controlled from an HP745i workstation running HP-UX and HP-BASIC. The current source for the resistance measurement is an HP41421B source monitor unit (SMU), while the voltage is measured with an HP3457A digital multimeter [137], which has been added to the 4062UX system. The current through the structure is measured with another HP41421B SMU, in voltage source mode, which is set to 0 V. The current measurement accuracy at 500 μA is $\pm 2\mu$A, which is equivalent to a possible systematic offset of up to $\pm$1.6nm in both the Greek cross and the bridge measurements. However, these are likely to be in the same direction for both measurements and as such will cancel out. The standard deviation of the current measurement is $\sim$50nA taken over 500 measurements at 500μA. This is equivalent to a change in linewidth of less than 0.05nm when applied to the Greek cross measurements and 0.09nm for the bridge resistance measurements.

The voltmeter typically measures around 2.5mV for the Greek cross with a force current of 500μA. The accuracy of the meter in this range is $\pm 3.75\mu$V, which is equivalent to a change in linewidth of about $\pm$0.6nm. The measured voltage for the 480nm bridge structures at 500μA is around 11V ($R_B \approx$ 22.1kΩ) with an accuracy of $\pm$0.4mV, which is equivalent to a change in linewidth of less than $\pm$0.02nm. These will not cancel out in the same way as the effects of any inaccuracy in the current measurement and so there is the possibility of a systematic linewidth offset due to the voltage measurement.

The repeatability of the voltage measurements on the Greek cross is less than 0.5μV, which equates to a linewidth uncertainty of 0.08nm. Similarly for the bridge, the voltage repeatability for 500 measurements is about 0.1mV or less than 0.005nm. The combined statistical uncertainty derived from this analysis is $\sqrt{\sum \sigma_i^2} =$ 0.13nm with a possible systematic offset of 0.62nm if the effects of inaccuracies in the voltage measurements are additive.

The analysis of electrical linewidth metrology described in reference [128] suggests a number of possible sources of uncertainty. For example, any uncertainty in the length of the bridge resistor will affect the calculation of the ECD. The estimate of the possible misplacement of the voltage taps is 60nm (3σ) which, for a bridge with a nominal length of 400μm, is equivalent to an uncertainty of about 0.06nm in linewidth. The uncertainty caused by the tap shortening effect is difficult to determine for these test structures but it is likely to be extremely small as the bridge length is approximately 800 $\times$ the tap width. There are a number of factors, such as line edge roughness, sidewall angle, and oxidation, which might be expected to cause a systematic offset in the electrical measurement of linewidth. It is not clear how much of a contribution to the measurement uncertainty these will cause; oxidation is likely to be less of a problem than for the silicon structures in [128] but the contributions from roughness and sidewall angle could well be larger. Another assumption is that the sheet resistance measured at a certain measurement current is relevant to the bridge measurement. Figure 5.17 shows the extracted sheet resistance from Greek crosses with two different nominal widths. This indicates the extracted sheet resistance is a function of the level of the force current with both structures showing a similar dependence.

The results in figure 5.17 are averages of the first five results from a set of 500 measurements, as this best reflects the protocol used for the ECD measurements of mask MSN6659 that have been compared with the other metrology techniques. The full sheet resistance results from a Greek cross with a nominal arm width of 480nm can be seen in figure 5.18. It shows that the apparent sheet resistance changes more for the low current measurements. This effect is caused by changes in the measured voltage as the current does not vary significantly with measurement number. The fact that this has a larger effect on the low current measurements, where the measured voltage is small, suggests that it is caused by a voltage offset that is not corrected for by reversing

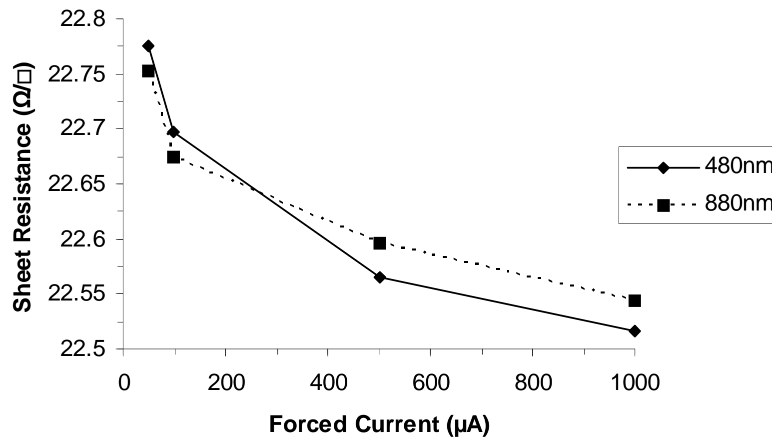


Figure 5.17: *Sheet resistance plotted against force current for two different Greek crosses. This shows a variation of around 1% over the range of currents used.*

the measurement current and furthermore has a thermoelectric component, which accounts for the initial increase in the offset before leveling off in thermal equilibrium. If this was caused by Joule heating of the device under test it might be expected that the effect on resistance would be greater for the higher measurement currents, which is not the case. The measured voltage at a current of 50μA is around 250μV and at that level the accuracy of the voltmeter is 3.7μV. This could result in a measured sheet resistance of up to 23$\Omega/\square$, which is near to what is observed in figure 5.18.

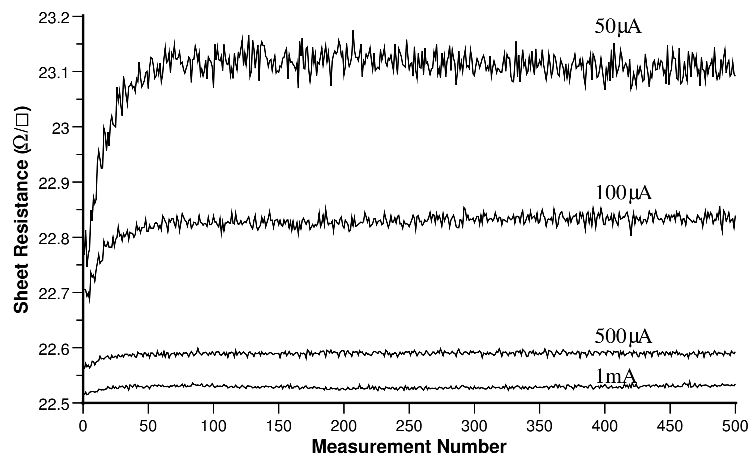
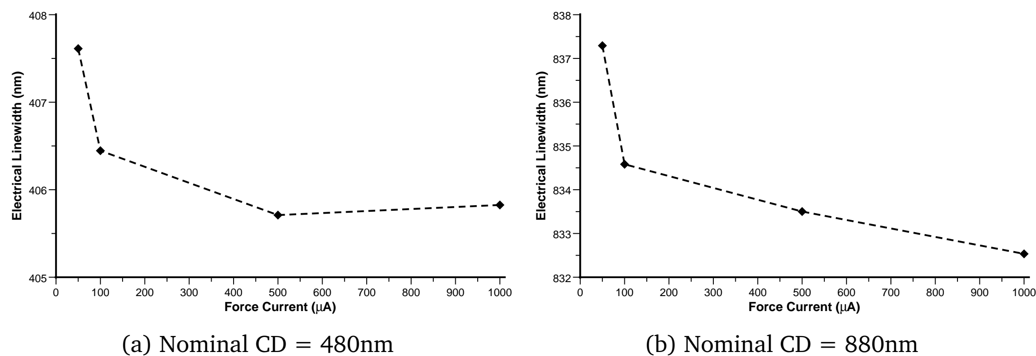


Figure 5.18: *Sheet resistance variation over 500 measurements for different measurement currents.*

The electrical linewidth results derived from the sheet resistance measurements in

figure 5.17 are shown in figure 5.19. The variation of the linewidth is dominated by the sheet resistance measurements. For the 480nm nominal lines the range is about 2nm, while it is larger at nearly 5nm for the wider lines. The effect is greater for the wider lines because when calculating the electrical CD the sheet resistance is divided by the bridge resistance. Therefore, the effects of sheet resistance errors are exaggerated for wider lines, which have a lower resistance. It is possible to explain some of this variation of linewidth with current by referring to the accuracy of the voltage measurements, but it seems likely from the variation with time that there is an additional voltage offset that is affected by heating when measurements are repeated. However, it does suggest that the measurements made at higher currents, where small voltage offsets are swamped, are more reliable.



(a) Nominal CD = 480nm (b) Nominal CD = 880nm

Figure 5.19: *Electrical linewidth plotted against force current for two different test structures.*

The overall uncertainty of the electrical linewidth measurements, made at a current of 500μA for both the Greek cross and bridge resistors, is less than 0.5nm (k = 2) but there is the possibility of larger systematic errors due to the voltage measurement accuracy and the choice of force current used, perhaps as much as 1% of the measured linewidth or ∼5nm for the narrowest structure. It may be that it was simply fortuitous that the measured ECDs are so close to the AFM results with no apparent systematic offset. On the other hand, the analysis predicts larger systematic errors for wider features but no divergence between the ECD and AFM results can be observed in figure 5.16 over the range of dimensions measured.

Measurements of a 10Ω resistor in an Agilent 16346B Calibration Module suggest that the analysis above is correct as they show an overestimation of the resistance at low current values due to an offset in the voltage measurement. A current of 500μA or

above was required in order to achieve resistance measurements that are within the quoted uncertainty ($\pm 0.07\%$) of the resistor calibration. These measurements were performed with a protocol that is as close as possible to that used for the sheet resistance extraction from the on-mask test structures.

5.3.7 Analysis of Optical Measurement Uncertainties

The repeatability performance of the MueTec <M5k> has been rigorously evaluated via a formal Equipment Assessment activity [22] to verify the suitability of the tool to support the 90nm manufacturing node of the 2001 International Technology Roadmap for Semiconductors (ITRS) within a typical production environment. A methodology was developed to characterize the tool performance that consisted of measuring a range of clear and opaque feature sizes (200-1000nm) sequentially over 30 loops each day for three consecutive days.

This study showed that, for isolated chrome lines, the tool was able to sustain a short-term measurement repeatability (i.e., precision) of $\leq$0.5nm (3σ) against a target tool specification of 1.0nm (3σ). In fact, the three day long-term repeatability, which represented accuracy against the calibration that the tool was using, could be sustained at a similar level against a specification of 1.5nm (3σ). Full details of similar measurements made on isolated spaces and dense lines and spaces can be found in [22].

5.3.8 Analysis of CD-AFM Measurement Uncertainties

The CD-AFM measurements were performed using a Veeco SXM320 with tip calibration being performed before each measurement [125]. A detailed description of the methodology and the analysis used to determine the uncertainty of the CD-AFM measurements made on photomasks can be found in [29]. In summary, the major contributions to the uncertainty of the CD-AFM measurement are from the tip shape calibration, around 1nm using the SCCDRM, and tip wear, which is more difficult to assess. Other contributions come from the repeatability of the measurement, which can be strongly affected by the linewidth roughness of the feature being measured. The standard deviation over the 1μm measurement length is typically around 6nm, as

mentioned previously.

5.4 Conclusions and Further Work

On-mask, electrical test structures based on industry standard OPC layouts have been designed and fabricated on a photomask using the GHOST proximity correction technique. These structures are direct electrical equivalents of optical metrology patterns, which are specifically designed to characterise OPC. Both electrical and optical measurements have been performed to evaluate the effectiveness of the GHOST correction strategy and to further examine the capability of two different metrology techniques. The analysis, presented in the first section of this chapter, has shown that GHOST correction has a significant, and positive, effect on the mask manufacturing process. However, the test structures have highlighted that there are limitations associated with the procedure which depend on the density and dimensions of the features being fabricated. The conditions for the correction exposure must be carefully considered, or the CD trends of the fabricated features may resemble those of their uncorrected inverse pattern and in some cases exhibit unexpected CD variations across a range of dimensions.

Future work should concentrate on fabricating proximity corrected photomasks, which are designed for a 90nm (360nm 4X) lithography process. These will be used to print test structures and will therefore allow comparison between dimensions at the mask and wafer level. This will provide a great deal of information on how the e-beam mask writer and photolithographic tools behave when they are operating near the limit of their capabilities.

In the second part of this chapter, three different techniques, electrical, optical and CD-AFM, have been used to measure the linewidths of metal features on a standard chrome on quartz photomask. ECD measurements are made by direct probing onto the mask, while optical measurements are made using a mask metrology and verification tool. The CD-AFM measurements are made using a state-of-the-art system, which is calibrated using a traceable reference standard and has an uncertainty of less than 4nm.

Measurements of isolated cross-bridge linewidth structures with nominal widths

between 480 and 720nm show good agreement between ECD and CD-AFM measurements. The offset is less than $\pm$10nm and shows no obvious dependence upon nominal size over the range of dimensions measured. This is not the case for the optical measurements which are offset by 60 to 90nm from the electrical and AFM measurements. The optical results also show a dependence on the nominal width with the offset reducing as dimensions increase. The AFM measurement is taken over a very short (1μm) distance while the ECD is an average over the length of a 400μm line. For this reason, further AFM measurements were taken at $\sim$70μm steps along a bridge structure. These demonstrated a surprisingly small variation in width of less than 5nm.

Overall, the ECD and CD-AFM measurements show very good agreement with no obvious systematic offset while the optical measurements overestimate the width of these narrow isolated features by as much as 90nm. These results demonstrate the capability of the on-mask electrical measurement technique, especially when compared to the optical tool. However, it should be recognized that the accuracy performance of the optical tool is governed by the calibration artefact used to establish the calibration within the manufacturing environment, and this artefact is not traceable to the NIST standards. The closeness between the independent electrical measurements and calibrated CD-AFM measurements does show that we are approaching a situation where an absolute linewidth standard for binary photomasks may be definable, as we are now directly probing the physical material that composes the measurement feature. This, in turn, will provide feedback to help create better calibration artefacts for the large number of optical metrology tools that are already in place supporting photomask manufacture.

Chapter 6
Electrical Test Structures for the Characterisation of Optical Proximity Correction

6.1 Introduction

The introduction of resolution enhancement techniques has allowed photolithographic systems to image features with dimensions lower than the exposure wavelength of the tool. A significant issue with printing sub-wavelength features however, is that patterns become distorted because of optical or process proximity effects [8, 138–141]. These distortions which can be seen in figure 6.1(a), arise in the form of shortening of the ends of lines and rounding of corner features. Optical proximity correction [43] was developed in the early 1970's as a means of addressing lithographic distortions in semiconductor manufacturing. It applies systematic changes to photomask geometries to compensate for non-linear effects, as an attempt to make the final printed feature match more closely the desired layout. A mask incorporating OPC is thus a system that attempts to negate undesirable distortion effects during pattern transfer.

To compensate for line-end shortening, the line is extended using a hammerhead shape, which results in a line that is much closer to the original layout. To compensate for corner rounding, serif shapes are added to external corners and opaque material is removed from internal corners. A typical mask with OPC features and the desired printed feature is presented in figure 6.1(b). Printed features however do not have simple relationships to reticle dimensions and this makes it difficult to manually layout a photomask that will produce the desired features on wafer, as the optimal type, size and symmetry is very complex and depends on neighbouring geometries and process parameters.

The work presented in this chapter extends electrical measurement techniques to two-dimensional OPC features [43], in particular the characterisation of corner serifs.

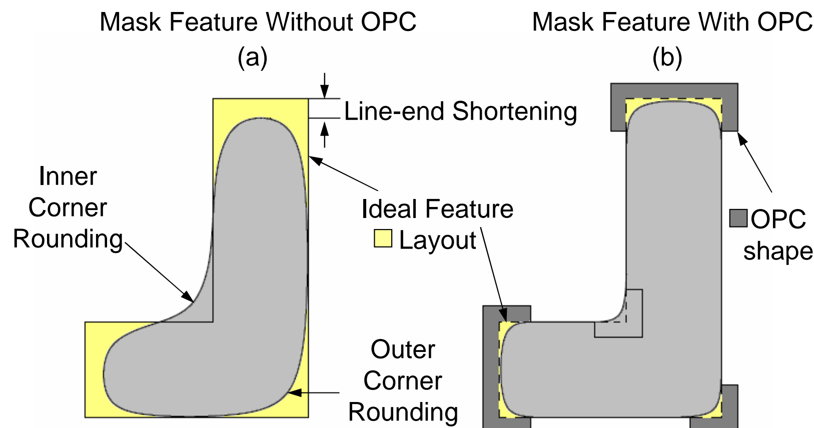


Figure 6.1: *(a) Layout of feature printed with a mask without OPC. (b) Layout of feature printed with a mask with OPC; the feature matches more closely the desired layout (dashed line).*

The corner serif is found with increasing frequency on advanced mask designs and presents a particular challenge to conventional metrology techniques [142]. This is even more relevant where less than ideal image rendering and over-aggressive design may lead to serif features becoming “pinched off” from the main corner feature. Electrical techniques should be suited to detecting these abnormalities, particularly on inner corner serifs [143], and it should be possible to relate these measurements to serif area as a means of process control of the mask making process.

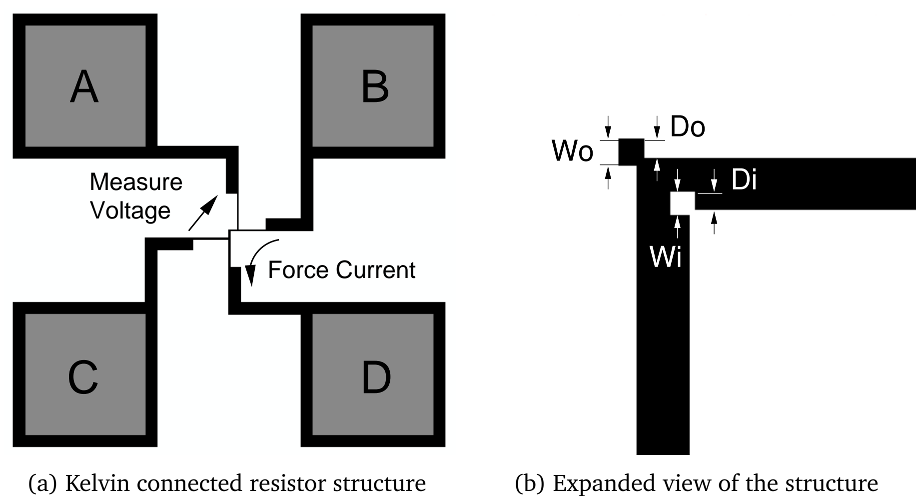
Chapter six begins by examining the use of an on-mask resistive test structure for the characterisation of corner OPC using simulations and measurements on a prototype photomask. The photomask is then used to print the structures on wafer. Simulations and measurements at wafer level are also performed and a comparison between the two is presented.

6.2 Test Structure Design and Photomask Layout

The test structure designed for this work is a Kelvin connected resistor consisting of a short section of metal track turning through a right angled corner, as shown in figure 6.2(a). In order to measure the resistance of the track a current is forced between pads B and D while the resulting potential difference is measured at pads A and C. The resistance of the section of track between the voltage taps is then

$$R = \frac{V_{AC}}{I_{BD}} \tag{6.1}$$

The effect of OPC is examined by altering the layout of the right angled corner of the structure. Specifically, a square of metal is added to the outside of the corner while a square is subtracted from the inside. This is illustrated in figure 6.2(b). The degree of OPC is altered by changing the size of the square (W_i and W_o) and the amount by which it overlaps with or protrudes from the original layout (D_i and D_o).



(a) Kelvin connected resistor structure

(b) Expanded view of the structure

Figure 6.2: *Layout of Kelvin test structure and closeup showing parameters of OPC features.*

The photomask design has test structures with 3 different base values of CD: 1.6μm, 2.0μm and 2.4μm. These correspond to printed dimensions of 320nm, 400nm and 480nm when imaged with a 5X projection lithography tool. The dimensions of the OPC elements are defined as fractions of the base CD: 0.25, 0.3, 0.35, 0.4, 0.45 and 0.5. Subsequently, the value of D_i/D_o is then defined as some fraction of W_i/W_o: 0.25, 0.5 or 0.75. The design has the full range of OPC dimensions for the 1.6μm structures and a reduced set for the other CDs with only the D_i/D_o values defined as half of W_i/W_o.

A prototype mask (MSN6754) was fabricated with this design, which includes one block of printable (see figure 6.3(a)) and two blocks of on-mask test structures (see figure 6.3(b)). The large pad test structures have been designed in such a way that when printed on wafer with a 5X photolithography system, they can be probed with the same card used for the on-mask structures.

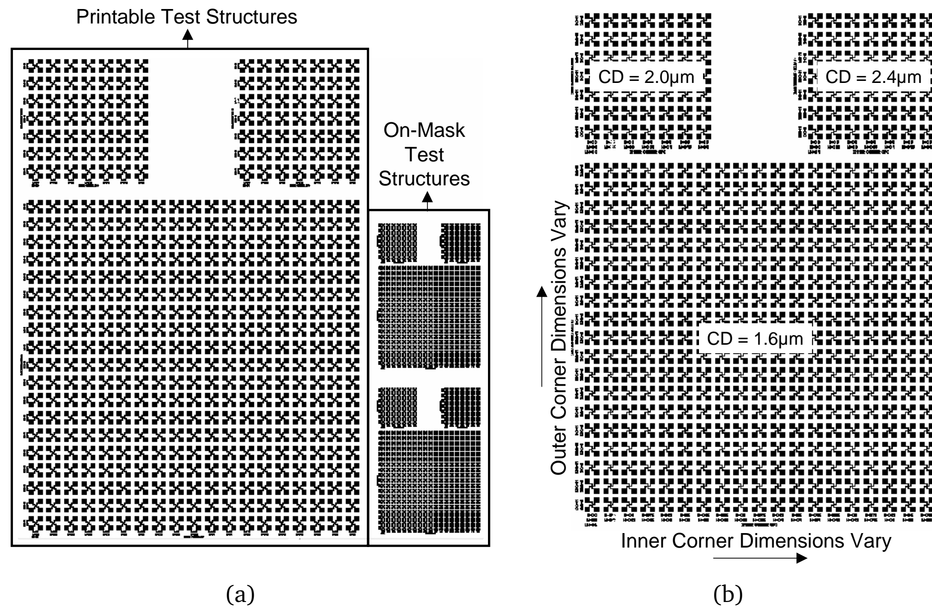


Figure 6.3: *(a) Complete photomask layout (b) Expanded view of block of on-mask test structures.*

6.3 Simulations

The two-dimensional (2D) solver for interconnect analysis (*Raphael*) [93] was used to model the resistance of test structures with different levels of OPC applied either to the inner or the outer corner. Having the mask design as a starting point, simulations were performed on structures with OPC features in either or both the inside and outside corners. A sheet resistance of 22.5Ω/□ was chosen for the material of the simulated structures, as this represents a typical value of the chrome layer, measured on similar masks. The layout of the structure used for the simulations can be seen in figure 6.4. For each simulation, a current is forced between terminals T1 and T2. T1 is grounded and T2 has a voltage applied to it so that a current flows between them. The voltage is then measured between T3 and T4 and these two measurements are used to calculate the resistance ($R = V/I$) between terminals T3 and T4.

The results of simulations for test structures with a base CD of 1600nm and serifs removed from the inner corners are presented in figure 6.5(a), while those for structures with serifs added to the outer corners can be seen in figure 6.5(b). The results show that when the correction is applied to the inner corner there is a significant resistance change with respect to the dimensions of the OPC feature. In

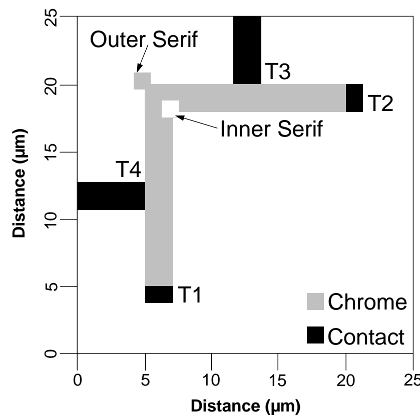
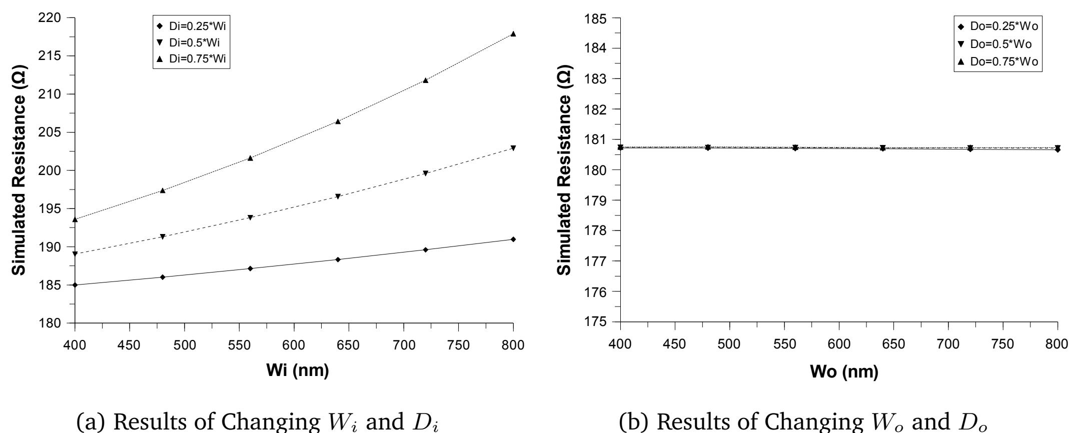


Figure 6.4: *Test structure used for simulating different degrees of corner OPC.*

particular, it appears that the resistance strongly depends on the area of the material removed to form the serif in the structure. This behaviour is to be expected as most of the current flow in the structure is concentrated around the region of the inner corner. This is illustrated in figure 6.6 which shows a contour plot of the current density around the corner of a 1600nm wide structure with inner and outer serifs. On the other hand there is little variation of resistance when the area of the outer serif changes and this is to be expected as there is minimal current flow in this region of the structure. Any resistance variation caused by altering the dimensions of the outer serif will be swamped by real mask effects (such as R_S and CD variations) that are not present in the simulations.



(a) Results of Changing W_i and D_i (b) Results of Changing W_o and D_o

Figure 6.5: *Simulation results showing the effects of changing the dimensions of the OPC features.*

Finally, simulation results from 1600nm wide test structures with OPC features on both

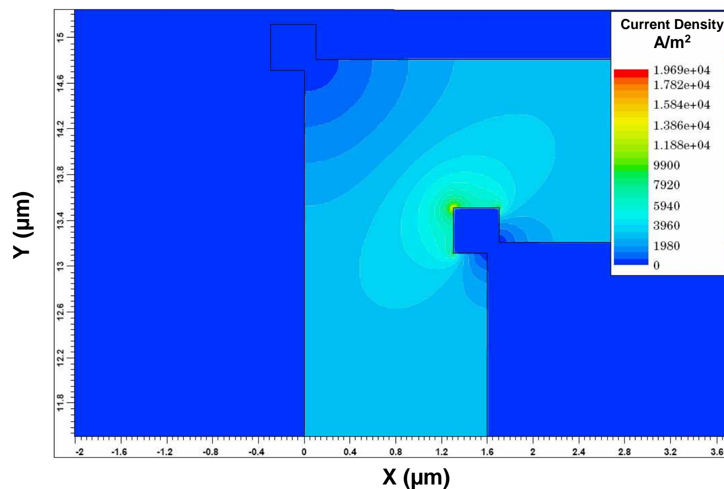
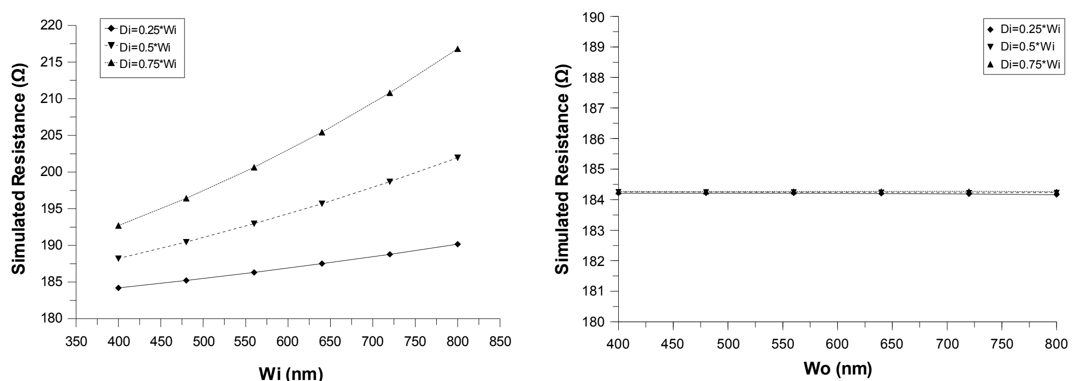


Figure 6.6: *Current density scalar contour plot for a simulated corner structure with inner and outer serifs.*

the inside and the outside corners are presented. Figure 6.7(a) shows the resistance values for structures where the inner serif dimensions vary while the the outer serif feature remains the same ($W_o = 0.25 \times$ CD and $D_o = 0.25 \times W_o$). Similarly, figure 6.7(b) shows the results for structures with varying outer serif dimensions and the same inner serif feature ($W_i = 0.25 \times$ CD and $D_i = 0.25 \times W_i$). It can be seen that the addition of an outer OPC feature has little effect, certainly smaller than any resistance change associated with varying the inner serif dimensions. In contrast the addition of an inner serif changes the resistance of a structure far more than any resistance variation caused by the alteration of the outer serif area.



(a) Results of changing W_i and D_i, with constant outer serifs

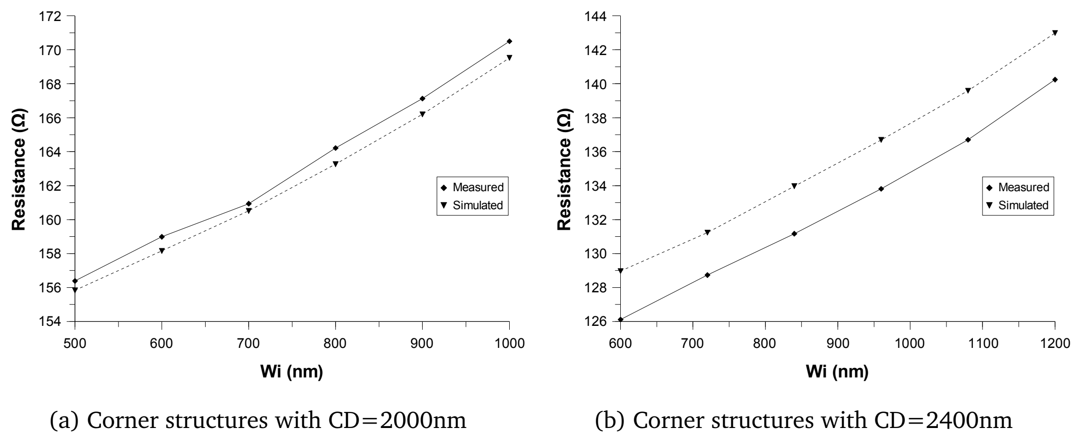
(b) Results of changing W_o and D_o, with constant inner serifs

Figure 6.7: *Simulation results showing the effects of changing the dimensions of the OPC features for structures with both inner and outer serifs.*

6.4 On-Mask Measurements and Results

6.4.1 Electrical Measurements

On-mask electrical measurements on structures that match the simulations have been made on mask MSN6754. Figures 6.8(a) and 6.8(b) show both the measured and simulated results for 2000nm and 2400nm wide structures with inner corner serifs and $D_i = 0.5 \times W_i$. These are part of the reduced sets, which have wider corner structures with larger OPC feature dimensions. The electrical measurements and simulation results are very similar, though the offset in resistance is obvious. This offset is most probably due to differences in the sheet resistance or CD. While the simulated structures use the designed CD, for on-mask features there is usually a non-linear transfer between fabricated and nominal width. In fact the trend in the offset between measured and simulated resistance changes from positive to negative as the nominal CD increases, which suggests just that. In addition the simulations use a constant R_S value, while in reality there will be R_S variations from structure to structure (albeit small). Finally, there are differences between the slopes of the measured and simulated results which is likely to be caused by inconsistencies, such as corner rounding, between the geometry of the structures on the mask and the designed structure used in the simulations.



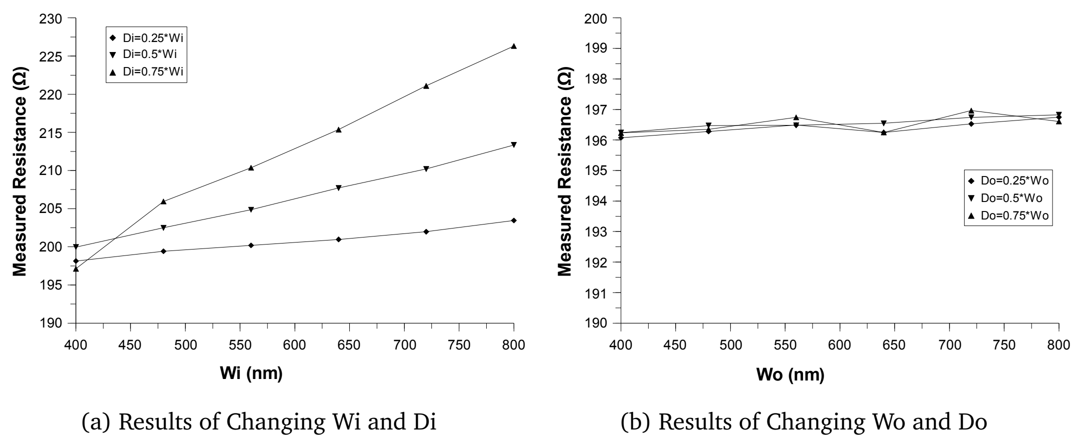
(a) Corner structures with CD=2000nm

(b) Corner structures with CD=2400nm

Figure 6.8: *Comparison of simulation results and on-mask measurements.*

In any case, the presence of OPC shows the expected strong effect on the resistance of a conducting track when applied to the inside of a right angled corner but little effect when applied to the outside. The rate of change of measured resistance with inner corner serif size is sufficient to make an unambiguous relationship between the

two parameters. This can be seen more clearly in figures 6.9(a) and 6.9(b), which present the results for 1600nm wide structures with OPC applied either to the inside or outside corner. As it was stated previously the electrical technique would be suited for detecting abnormalities on the fabricated serif features, particularly on inner corners. The resistance results of figure 6.9(a) follow the anticipated trends except for the structure with $D_i = 0.75 \times W_i$ and $W_i = 400$nm, where the resistance is smaller than normally expected. This is not a local mask effect as it can be seen in every structure with these inner serif dimensions, independent to their position on the mask and to the presence or absence of an outer serif. Therefore this is an indication that there is excess chrome at the area where a square of material should have been removed to form the inner serif. The deformed serif is most likely caused by the bridging of its two abutting corners, which would nominally be in close proximity.



(a) Results of Changing Wi and Di

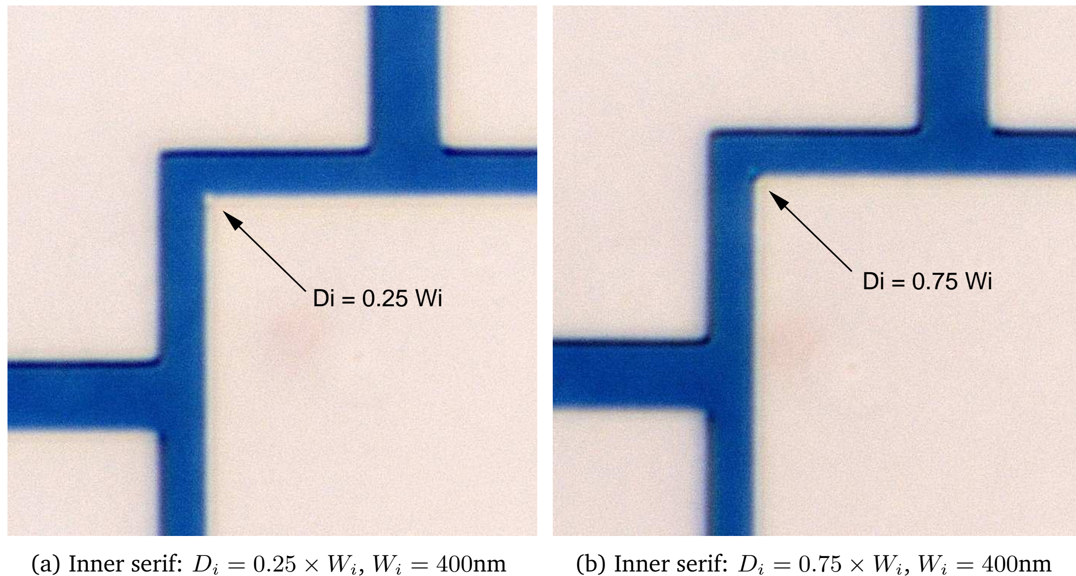
(b) Results of Changing Wo and Do

Figure 6.9: *Electrical measurement results obtained from binary mask (MSN6754).*

6.4.2 Optical Inspection

In order to visually investigate this effect a high-resolution Reichert Jung Polyvar optical microscope [144] with Nomarski differential interference contrast optics was used to capture reflected light images of corner structures with and without the over-aggressive design dimensions. Figures 6.10(a) and 6.10(b) show the images of corner structures where $W_i = 400$m, while $D_i = 0.25 \times W_i$ and $D_i = 0.75 \times W_i$ respectively. For $D_i = 0.75 \times W_i$ it appears that no chrome material has been removed from the area that forms the inner serif. For $D_i = 0.25 \times W_i$ although the design area that defines the inner serif is smaller than that of figure 6.10(b), it appears that the material has been removed. It

is clear however, that the resolution of the images is inadequate and the optical tool is struggling to resolve the OPC features and thus clearly identify any difference between the structures. This confirms the problem of characterising advanced mask designs with OPC features, on conventional optical tools. Although mask features are usually four or five times larger than the printed dimensions, the OPC features are far smaller, similar to typical features on wafer level.



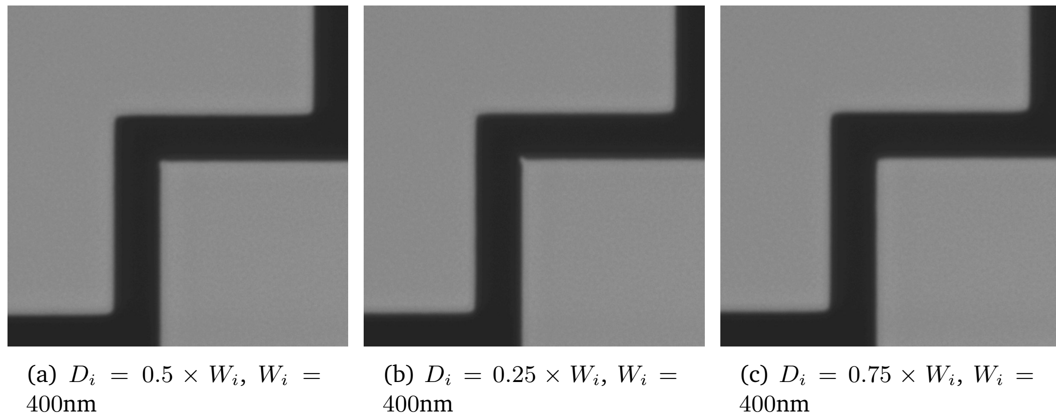
(a) Inner serif: $D_i = 0.25 \times W_i$, $W_i = 400$nm (b) Inner serif: $D_i = 0.75 \times W_i$, $W_i = 400$nm

Figure 6.10: *Optical images for corner structures with inner OPC features only.*

Further optical images were obtained in transmitted light for the $W_i = 400$nm features using a MueTec <M5k> mask metrology system [22, 114, 115] operating with 248nm DUV illumination. These can be seen in figure 6.11 where (a) and (b) respectively show that inner corner serifs are defined for the $D_i = 0.25 \times W_i$ and $D_i = 0.5 \times W_i$ structures. Figure 6.11(c) reveals that there is no apparent modification to the $D_i = 0.75 \times W_i$ corner at all, consistent with an improperly formed (or missing) corner serif at this aggressive placement level. Other imaging techniques with better resolution are required in order to better understand the nature of the serif defect.

6.4.3 Atomic Force Microscope Inspection

A Digital Instruments D5000 Atomic Force Microscope [145] with superior resolution than the optical tools, was used to further investigate the reason for the change in



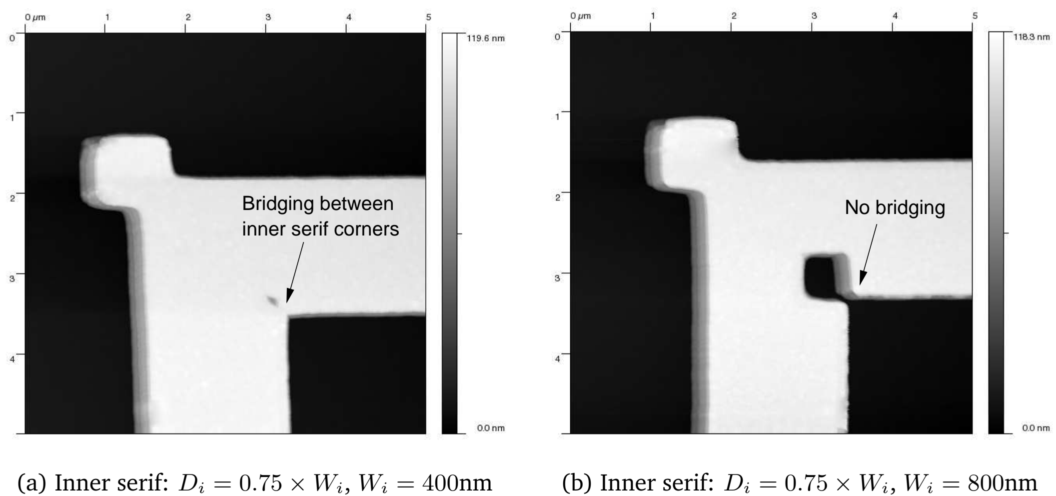
(a) $D_i = 0.5 \times W_i$, $W_i =$ 400nm

(b) $D_i = 0.25 \times W_i$, $W_i =$ 400nm

(c) $D_i = 0.75 \times W_i$, $W_i =$ 400nm

Figure 6.11: *Optical images for structures with inner corner serifs.*

resistance. The AFM scans cover the area surrounding the corner where the OPC features are located. The images of 1600nm wide structures with $D_i = 0.75 \times W_i$, $W_i = 0.25 \times$ CD = 400nm and $D_i = 0.75 \times W_i$, $W_i = 0.5 \times$ CD = 800nm can be seen in figures 6.12(a) and 6.12(b) respectively. Although there are outer OPC features also in these structures, the resistance values are similar to structures with no outer serifs. Differences in the resistance between structures with and without outer corner serifs are more likely to be caused by R_S, CD and inner corner rounding variations, rather than the actual presence or absence of an outer serif.



(a) Inner serif: $D_i = 0.75 \times W_i$, $W_i = 400$nm

(b) Inner serif: $D_i = 0.75 \times W_i$, $W_i = 800$nm

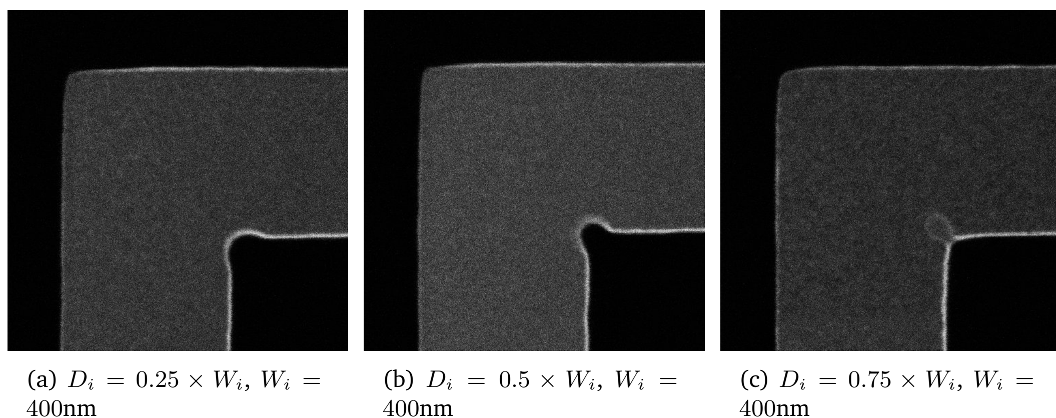
Figure 6.12: $5\mu m \times 5\mu m$ *AFM scans of corner structures with inner and outer OPC features.*

Figure 6.12(a) confirms that there is a problem with the fabrication of the inner serif

for the specified dimensions. It appears that the spacing between the two neighbouring corners of the inner serif is too narrow to be resolved during fabrication. This causes the bridging of the two corners, which results in a very small partially processed area instead of a well defined inner serif. As this area is smaller than the diameter of the AFM tip, it is not possible to probe down to the surface of the quartz and assess properly the extent of the partial processing. Figure 6.12(b) shows the scan for an inner serif which retains the designed shape. Although the dimensions of this structure are larger, this is the desired effect as it will yield a well defined corner on the wafer.

6.4.4 Focused Ion Beam (FIB) Images

Another way of obtaining high resolution images is from a FIB mask repair tool. Figure 6.13 shows images of three progressively more aggressive corner serif offsets captured by a Seiko Instruments SIR 500 repair system [117], with the defective serif structure imaged in 6.13(c). This high resolution image indicates that the Cr layer is continuous at the serif location - the degree of offset is essentially too extreme for a feature of this size and the serif has detached itself from the line edge into a spot unresolvable by the lithography process. The electrical behaviour of such a corner is more like that of an uncorrected one, albeit with a thinning of the Cr layer at the corner point. This is consistent with the measured resistance behaviour seen in figure 6.9(a).



(a) $D_i = 0.25 \times W_i$, $W_i =$ 400nm (b) $D_i = 0.5 \times W_i$, $W_i =$ 400nm (c) $D_i = 0.75 \times W_i$, $W_i =$ 400nm

Figure 6.13: *FIB images for structures with inner corner serifs.*

6.5 On-Wafer Test Structures

The mask that was electrically measured was used to print test structures for on-wafer characterisation [146]. The printed structures and electrical measurement methods applied so far, could form a valuable tool for investigating the quality of the lithographic transfer and for optimising the corner serif structures.

6.5.1 Fabrication

On-wafer test structures were fabricated in a 300nm thick layer of doped polysilicon deposited on a 0.5μm thick layer of thermal silicon dioxide on 200mm silicon substrates. The wafers were spin coated with Ultra-i 123 i-line photoresist and printed using a 5$\times$ Nikon NSR-2005i9C i-line step and repeat lithography tool with an NA of 0.50. After development the polysilicon was etched in a reactive ion etch (RIE) tool before passivation with a 0.5μm thick layer of plasma-enhanced chemical vapor deposition (PECVD) silicon oxide. Holes in the oxide were then etched over the probe pads before deposition of a 0.5μm thick layer of sputtered aluminium. The final step was to pattern the aluminium to create contacts suitable for probing. A schematic of the test structure fabrication process is shown in figure 6.14.

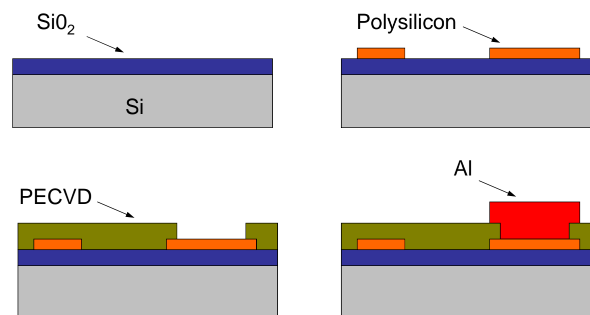
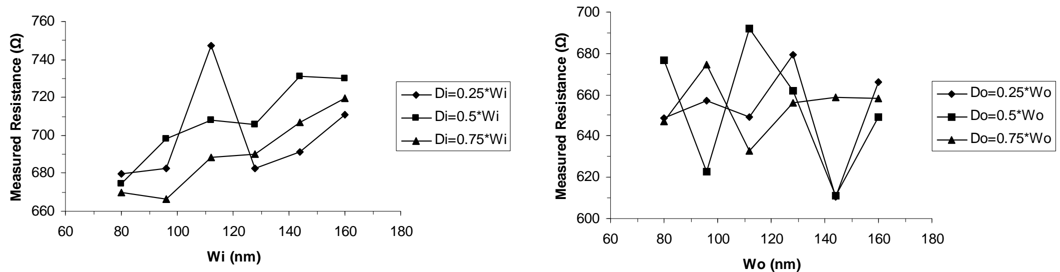


Figure 6.14: *Fabrication process steps for on-wafer test structures.*

6.5.2 On-Wafer Electrical Measurements

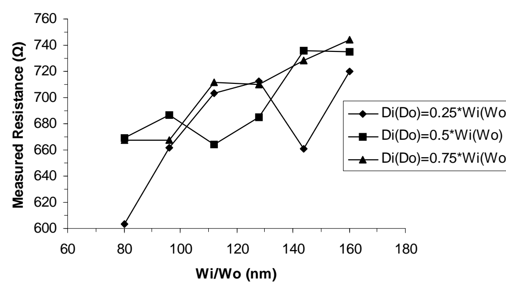
Three sets of 320nm wide on-wafer structures with varying nominal OPC feature dimensions were measured electrically and the results are presented in figure 6.15. One set consists of structures with inner corner OPC serifs only, one with outer corner serifs only and one with both. The resistance results of figure 6.15(a) suggest an upward

trend in resistance as W_i increases, as would be expected.



(a) Measured resistance against inner corner OPC dimensions

(b) Measured resistance against outer corner OPC dimensions



(c) Measured resistance against inner and outer corner OPC dimensions

Figure 6.15: *Resistance measurements for on-wafer structures with inner and outer corner OPC arrangements.*

However, the nature of the results suggest that other factors also affect the resistance of the structure. The reason behind this could be related to fabrication artifacts such as non-uniform lithography or etching, which tends to mask the data trends because the resistance changes are not only due to the OPC features. Another factor that could strongly affect the results is any variability in the localised sheet resistance of the polysilicon layer. This could introduce some of the structure-to-structure variations shown in the resistance results. Reference [147] examines the effect that the geometry of a structure has upon the value of resistivity extracted from Greek crosses. The sheet resistance of a polysilicon film is a function of the size and distribution of the grains and [147] identifies how the grain structure increases the variability of R_S measured using Greek crosses with narrow arm widths. Unfortunately there are no structures such as these on the wafer to confirm whether this is the cause of the variability observed in the measured results. A wafer map of the measured sheet resistance of the polysilicon layer on a wafer from the same batch as the test structures is presented in figure 6.16.

This was made using a four-point probe system which unfortunately does not have sufficient resolution to identify very localised sheet resistance variations that might cause the observed variation in the resistor test structures.

Figure 6.15(b) indicates that the presence of OPC has little or no effect on the resistance of the conductive track when applied to the outside of the right angled corner. This behaviour is to be expected as most of the current flow in the structure is concentrated around the region of the inner corner. This is illustrated in figure 6.15(c) which shows results from structures with both inner and outer corner serifs. It is clear that the dominant effect in the measured resistance is from the inner corner section, as a similar trend is observed for structures with only inner corner serifs. These results are obviously also affected by significant resistance variation. Unfortunately only small numbers of the test structures have been tested and the inter-die variation has not been determined.

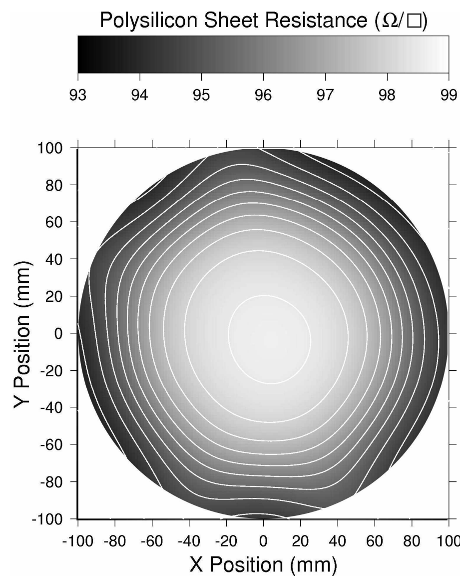
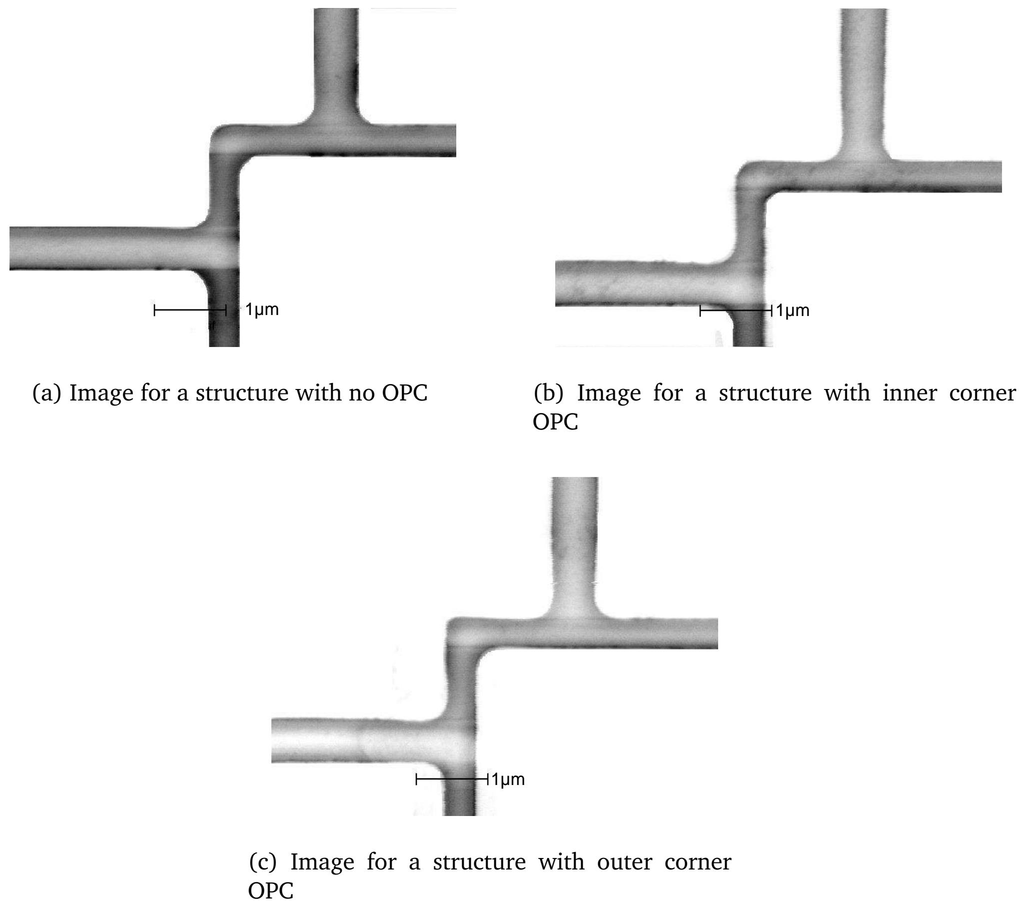


Figure 6.16: *Sheet resistance variation across one wafer with corner OPC electrical test structures.*

6.5.3 Scanning Electron Microscope Inspection

In order to visually investigate the effects, a Philips XL40 SEM was used to capture images of the structures which were measured electrically. Imaging software was then used to invert the SEM images and filter out their background. Figure 6.17(a) shows a structure with no OPC, while figures 6.17(b) and 6.17(c) show structures with the most

aggressive inner and outer corner serif dimensions respectively. The images suggest that when OPC is applied to the inner or the outer corner of a structure the shape of the corner changes and in particular the level of corner rounding.



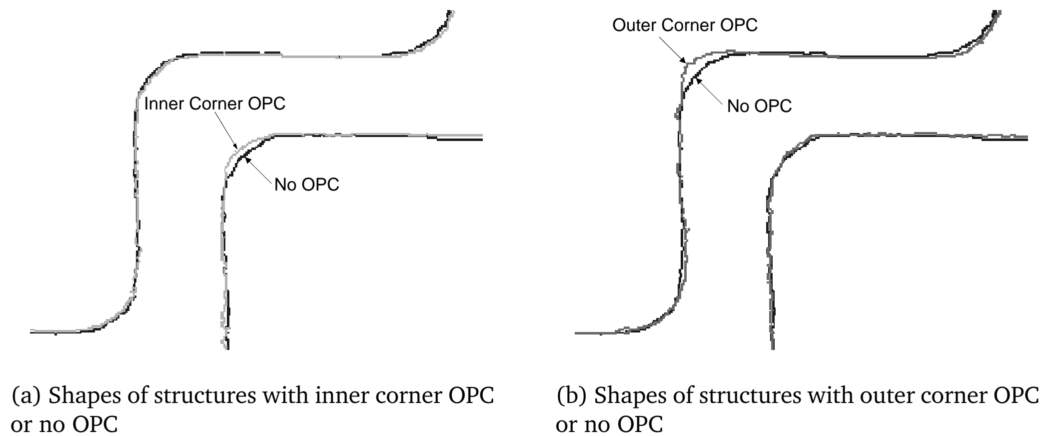
(a) Image for a structure with no OPC

(b) Image for a structure with inner corner OPC

(c) Image for a structure with outer corner OPC

Figure 6.17: *SEM images of structures with different OPC arrangements.*

To help compare the structures an edge detection filter in the Gnu Image Manipulation Program (GIMP) was applied to the images which are subsequently overlaid on one another. Comparisons of the structure with no OPC with the structures with the most aggressive OPC on the inner and outer corners are presented in figure 6.18. These confirm that when OPC is applied the shape of the inner and outer corners changes with respect to an uncorrected corner. Therefore, for inner corners OPC does have an effect and is likely to be the cause of the observed trends in electrical measurement results. On the other hand while OPC does affect the rounding of the outer corner it has no effect on the measured resistance and could be omitted from designs in many cases.



(a) Shapes of structures with inner corner OPC or no OPC

(b) Shapes of structures with outer corner OPC or no OPC

Figure 6.18: *Overlaid shapes of structures with different OPC arrangements.*

6.5.4 Simulations

The *Raphael* software was used to model the resistance of printed test structures with different levels of corner rounding applied to the inner or outer corner. The simulations provide a wider range of corner rounding dimensions than the fabricated features, which were estimated to be between 275-330nm for inner corners and 190-300nm for outer corners. A sheet resistance of 97Ω/□ was chosen for the material of the simulated structures, as this represents a typical value for the polysilicon taken from the four point probe results shown in figure 6.16. The layout of the structure, which records the simulated resistance as described in section 6.3, can be seen in figure 6.19. The radii of the two circles define the level of inner and outer corner rounding.

The results of the simulations for test structures with inner corner rounding are presented in figure 6.20(a), while those for structures with outer corner rounding can be seen in figure 6.20(b). The results of figure 6.20(a) show that there is a significant resistance change with respect to the inner corner rounding. In particular, it appears that the resistance strongly depends on the radius of the corner rounding and thus the area of the material added to the structure. This behaviour is to be expected as most of the current flow in the structure is concentrated around the region of the inner corner. This confirms that for the inner corner measurement results of figure 6.15(a), OPC has an effect on the fabricated corner of the printed structure, which is dependent to the dimensions of the OPC square.

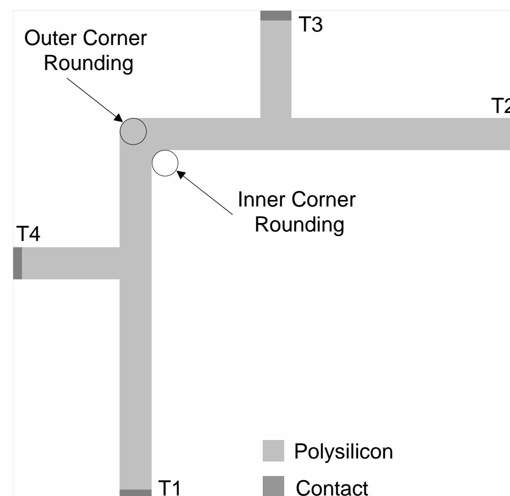
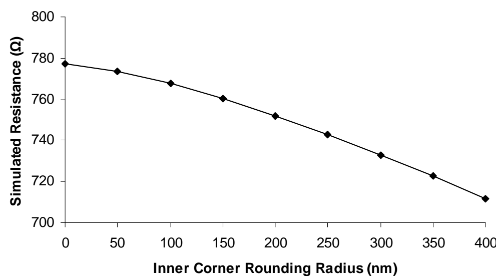
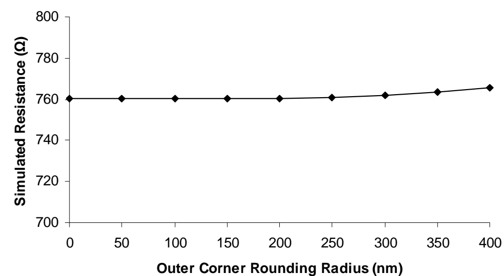


Figure 6.19: *Layout of structure used to simulate the effect of inner and outer corner rounding.*

The simulations for outer corner rounding on figure 6.20(b) confirm that there is little variation of resistance when the area of the outer corner changes and this is to be expected as there is little or no current flow in this region of the structure. Any resistance variation caused by altering the dimensions of the radius of the outer corner rounding will be minimal compared to other fabrication effects on wafer. This can be seen on the results of figure 6.15(b) which appear noisy and show no trend with respect to dimensions.



(a) Simulated resistance against inner corner rounding dimensions



(b) Simulated resistance against outer corner rounding dimensions

Figure 6.20: *Simulated resistance for structures with inner and outer corner OPC arrangements.*

6.6 Conclusions and Further Work

This chapter has demonstrated the feasibility of extending electrical measurement techniques to the characterisation of two-dimensional OPC serif structures. Whilst restricted in practical application to inner corner serifs, it should be highlighted that it is this circuit feature that is most relevant to achieving the desired device electrical performance (and is indeed why it is sensitive to the described measurement technique in the first place). Inner corner serif structures are also the most notoriously difficult to manufacture and quantify using conventional optical metrology techniques.

The results from this work have clearly shown that electrical techniques are sensitive enough to measure the effects of small inner corner structures reliably and in good agreement with theoretical predictions. Any departures from the simulated results have been found to be attributable to defects in the serif structure. The agreement with simulation is a good indicator that it is the material physically present on the mask which is being characterised, removing some of the ambiguity inherent when interpreting indirectly acquired images of the mask pattern.

Corner test structures were also designed to investigate the impact they have on printed features. Results of electrical measurements of polysilicon test structures printed using the measured photomask suggest that OPC applied to the inner corner has a significantly greater effect on the resistance than outer corner serifs. SEM imaging of the test structure geometries confirmed that OPC does alter the shape of corner rounding. Therefore, it is primarily the inner corner OPC that affects the resistance of a measured structure, while outer corner OPC has little or no effect on the measurement. However, it appears that, unlike measurements on the mask, the effects of OPC are confounded by other fabrication artefacts when printed with i-line technology. Local variations cannot be explained by dimensional effects and the most likely explanation is the grain structure of the polysilicon, which is a well known cause of sheet resistance variation.

Further measurements should be made on polysilicon test structures to extend the analysis of the results presented in this chapter. Two papers have been recently prepared (see section A.2), which present new data on the variation of the resistance of the printed features with respect to the levels of OPC applied. In addition it would be

useful to determine if the observed effects are maintained when the size of the features is reduced, or when the material of the structures is a metal with much lower resistance.

Further work should focus on correlating the measured resistance with actual mask serif or wafer corner rounding area. In addition an investigation should be made on how the offset between theoretical and measured values can be related to area loss arising from pattern fidelity of the rendered serif features.

Chapter 7
Matching Resistor Test Structures for the Characterisation of the Photomask Fabrication Process

7.1 Introduction

The differences between identically designed integrated circuit components are commonly referred to with the terms matching or mismatch. Electrical test structures, measurement methods and characterisation techniques, for evaluating mismatch fluctuations of IC components, have been studied extensively in the past [98]. The knowledge gained from this work helps improve IC technologies and leads to better electronic circuit performances.

This chapter investigates the use of on-mask, electrical, mismatch test structures and measurement techniques to characterise the capability of the mask making process [130, 148, 149]. Results from the literature [150], which looked at similar structures fabricated on-wafer as diffused resistors in a CMOS process, have shown effects related to spin processing of photoresist during photolithography. In the mask making process an additional, important source of dimensional systematic mismatch is the exposure tool itself. As errors on the mask directly affect the dimensions on the wafer the characterisation and control of these issues is fundamental.

The first section of Chapter 7 describes the design and fabrication of the matching structures, on protype masks, which also include other types of test structures for the work presented in previous chapters [118, 129]. The results from electrical measurements on the structures are analysed to obtain information about the capability of the photomask fabrication process. The second part of this chapter describes the fabrication of matching structures on a new set of advanced photomasks. This design takes advantage of the full mask area and consists of a regular array of structures, which provides a greater volume of data. Results from on-masks measurements are

analysed to further investigate the dimensional systematic mismatch due to tool or process induced effects.

7.2 Electrical Measurement of Prototype Photomasks

7.2.1 Test Structures

The matching resistor test structure design consists of pairs of ostensibly identical Kelvin connected bridge resistors as shown in figure 7.1, which are suitable for direct on-mask electrical measurements. The bridge sections are 600μm long with a designed linewidth of 500nm and a separation of 30μm between each pair. The layout of the structures is defined so that each pair is identical in design and orientation. Both resistors in a pair are connected using the same interconnect frame and contacted with identical probe pad frames. This consistency helps avoid systematic mismatches caused by the asymmetry in the placement of the devices or unequal device orientation [99].

There are two different arrangements with resistors running either horizontally or vertically, which means that offsets can be measured along two axes. Figure 7.1 also shows the probe pad openings created by a second lithography and etch process after the test structures have been patterned. This exposes the chromium under the ARC layer allowing good electrical contact to the test structures.

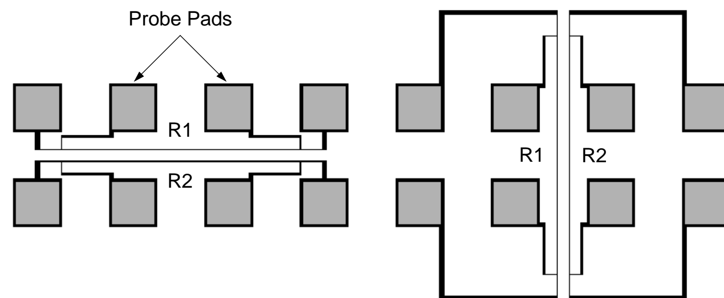


Figure 7.1: *Layout of mismatch bride resistor test structures.*

There are a total of 54 instances of the mismatch resistor cell in the prototype test mask design, which also includes test structure patterns for the work presented in Chapters 4 and 5. Figure 7.2 shows a test mask and indicates the position of a number of the sets of mismatch resistors. Two photomasks have been prepared using this design. The

first (MSN5757 - No PEC) was fabricated without any attempt to correct for proximity effects. The second plate (MSN6659 - GHOST) was fabricated using the GHOST technique [46] which attempts to correct proximity effects in e-beam lithography by equalisation of background dose.

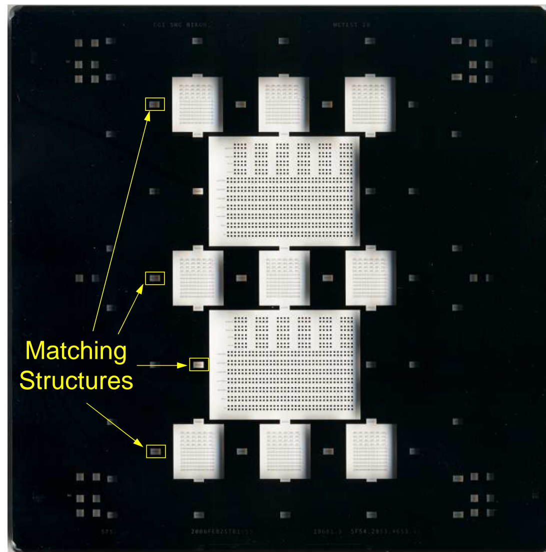


Figure 7.2: *Layout of a photomask with the matching structures highlighted.*

7.2.2 Measurement Technique

The resistor structures are measured by forcing a current (I) between the two outer pads and measuring the voltage (V) between the taps connected to the inner pads, as shown in figure 7.3. The current is then reversed, the measurement is repeated and the resistance ($R = V/I$) of each line is calculated. The resistors are measured in pairs and the measurement is repeated five times for each structure. A current of 10μA was chosen as this gave the lowest short term standard deviation (σ) over the five measurements. This is less than 1Ω for a typical resistance of 31kΩ, i.e. less than 0.003$\%$ variation.

The estimation of the electrical width of a feature requires a value for the sheet resistance (R_S) of the chrome layer. The chrome sheet resistance will vary across the mask but a short range variation is likely to be significantly lower and two closely spaced lines are likely to be fabricated from material with the same sheet resistivity. In addition the long 600μm bridge resistor will also serve to average out any small variations or

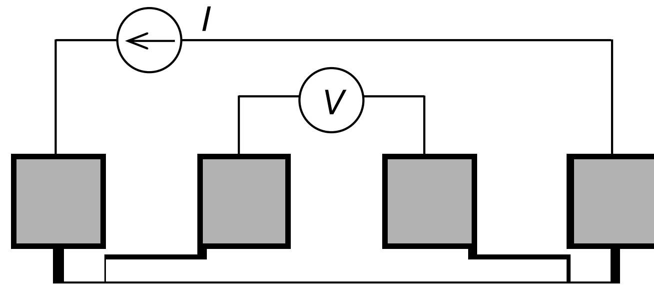


Figure 7.3: *Measurement of a Kelvin bridge resistor forming the half section of a horizontal matching structure.*

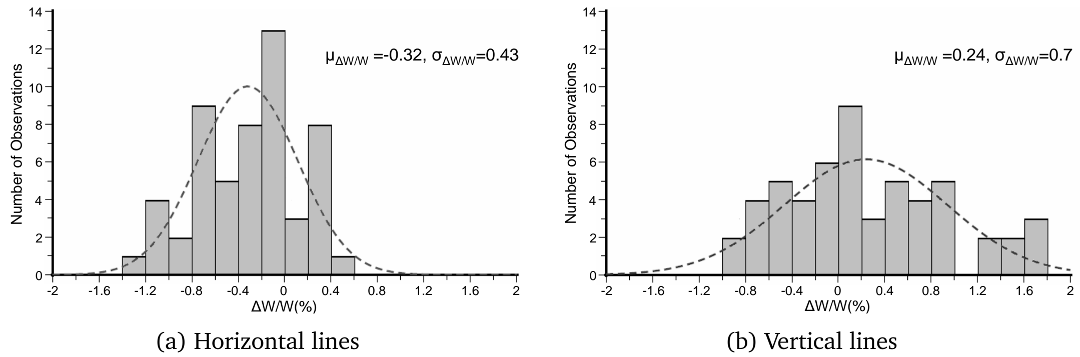
non-uniformities. Therefore, any significant resistance mismatch is most likely to be caused by a difference in CD between the two resistors. The length of the bridge will also tend to average out effects such as defects or line edge roughness and an actual CD bias between the two lines is more likely to be observed. The sheet resistance is normally derived from the measurement of a Van der Pauw structure located close to the bridge structure, but this is not available for the matching pairs. However, measurements of R_S obtained from cross-bridge structures on the two chrome masks have shown a less than 1% variation across the mask with an average value of 22.5$\Omega/\Box$.

The CD mismatch between the two resistors R1 and R2 is the difference between the widths WR1 and WR2 divided by the average width, or ΔW/W, expressed as a percentage. It should be noted that any errors introduced by the estimation of the sheet resistance will be cancelled out.

7.2.3 Measurement Results and Analysis

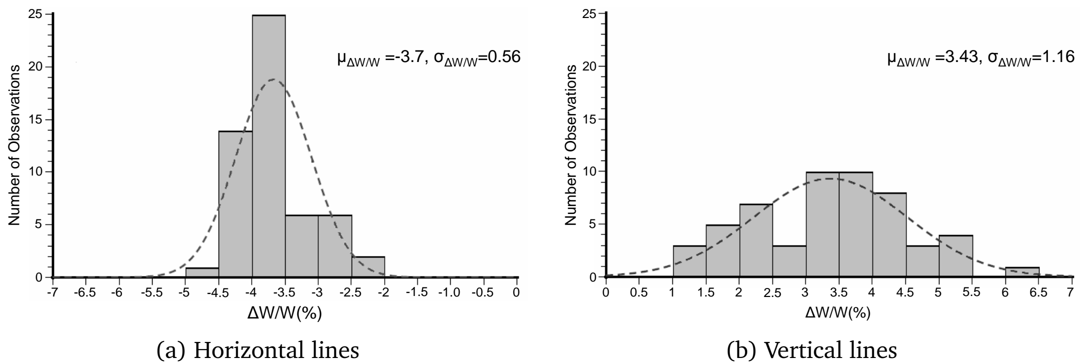
The CD mismatch has been calculated for each of the horizontal and vertical resistor pairs on the two masks and the results are plotted as histograms in figures 7.4 and 7.5 for MSN5757 and MSN6659 respectively. A normal distribution has been fitted to each set of results and the mean (μ) and standard deviation (σ) have been calculated.

The histograms indicate that what is observed is more than a random statistical variation of resistance. The results from MSN5757 show a small systematic mismatch which is less than the standard deviation. Results from MSN6659 show a mean ΔW/W of more than 3% for both horizontal and vertical lines and an increase in the spread



(a) Horizontal lines (b) Vertical lines

Figure 7.4: *Histograms of CD mismatch results for MSN5757 (No PEC).*



(a) Horizontal lines (b) Vertical lines

Figure 7.5: *Histograms of CD mismatch results for MSN6659 (GHOST).*

of the data as well. Examination of the write data revealed a difference in grid size between data in the primary and GHOST exposure such that the features in the GHOST pattern overlap the main pattern by 10nm in X and Y. This offset is applied to the right hand and upper edges of the features as can be seen in figure 7.6. However, the average values of CD mismatch are greater than the GHOST pattern error at 14.32nm for vertical lines and -14.92nm for horizontal lines. In addition the GHOST pattern offset should be the same for both lines in a pair so it is certainly not clear that the GHOST exposure is the source of the systematic offset. The fact that this large constant mismatch is only observed on the GHOSTed mask is suggestive of this conclusion.

References [150, 151] have shown that spin processing during lithography can introduce a CD mismatch between adjacent features, which varies with the position on the wafer. In order to investigate this the data from both masks have been plotted against the position of the structure, in X or Y directions, on the mask in figure 7.7. The results in figure 7.7(a) do not vary significantly from one side of the mask to the other.

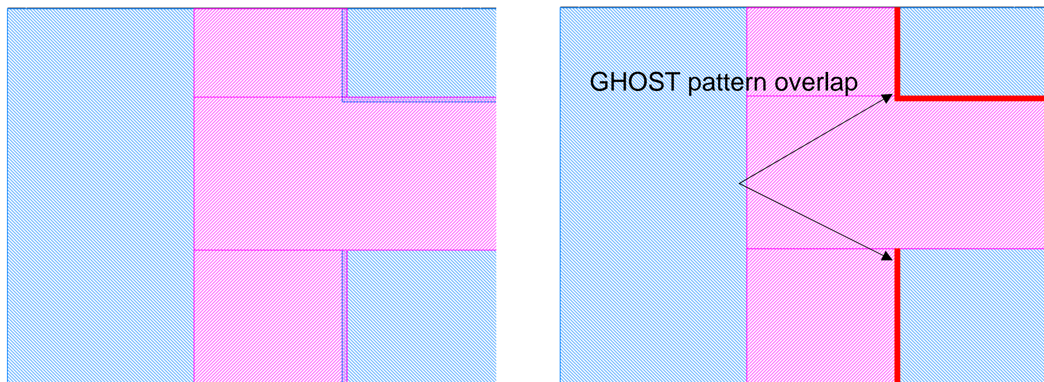
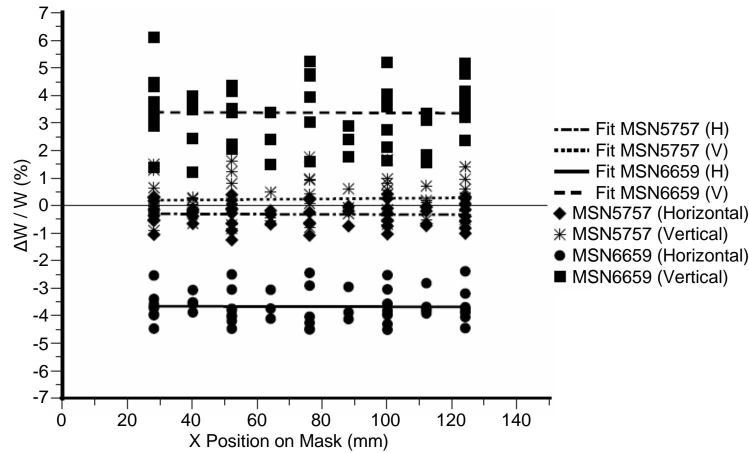


Figure 7.6: *Schematic showing the pattern overlap caused by the difference in the grid size between the two exposures.*

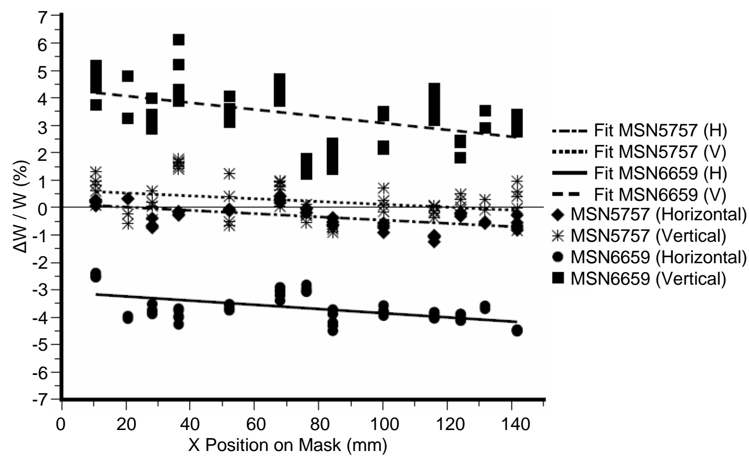
Any variation with position is much less than the spread of the data. Figure 7.7(b) shows there is a downward trend in ΔW/W going from the bottom to the top of the mask. This is true for both the vertical and horizontal lines, and has a similar slope for both masks. Although this suggests some additional systematic source of mismatch, it is unlikely to be caused by spin process effects, as a difference in trend would be expected between the vertical and horizontal lines. The absence of a significant trend in the results plotted against horizontal position on the mask also suggests that this is not the source of the observed mismatch.

The un-normalised CD mismatch values ΔW_h and ΔW_v can be turned into a CD bias vector for each set of test structures on the masks. These are plotted in figures 7.8(a) and 7.8(b) to show the linewidth mismatch and its dependence on position. An arrow pointing up indicates that the upper line in the horizontal pair is wider while an arrow pointing left indicates that the leftmost line in the vertical pair is wider.

The vector plot for MSN5757 shows a systematic matching offset behaviour that cannot be attributed to the signature expected from the processing steps used to manufacture the mask. This suggests that we are observing some form of footprint being introduced by the electron beam lithography tool used to write the basic mask pattern. Any similar effect in the results from MSN6659 is swamped by the large systematic mismatch. In order to compare the two masks the average value of horizontal, or vertical CD bias is subtracted from the result to leave the underlying variation. These results are plotted for both masks in figure 7.9.



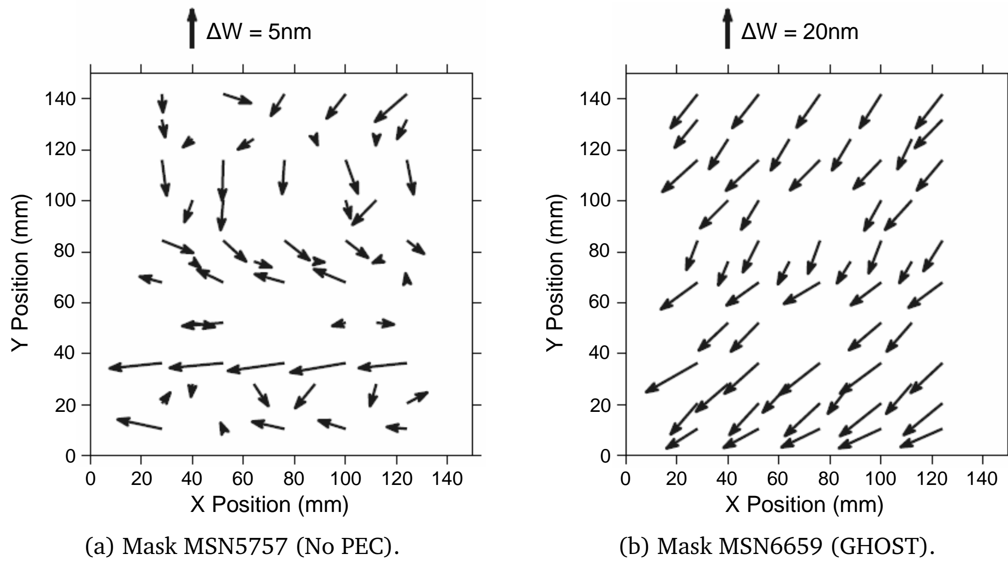
(a) ΔW/W against X position.



(b) ΔW/W against Y position.

Figure 7.7: *CD mismatch ΔW/W against mask position for masks MSN5757 (No PEC) and MSN6659 (GHOST).*

The results from the two masks are in agreement in the direction of the offset for many of the measurement positions but the magnitude of the vector is generally larger for mask MSN6659. The source of the observed systematic errors is thought most likely to be stage position/travel or pattern segment butting issues from the lithography tool. The mask data is written by the e-beam tool in segments which are 655.36μm high and 20971.52μm wide. The electron beam is scanned vertically while the stage moves horizontally. Vertical boundaries between segments indicate the point at which the tool loads a new block of pattern data from memory. The electron beam scans always from left to right across the whole mask before moving to the next row, while the stage



(a) Mask MSN5757 (No PEC). (b) Mask MSN6659 (GHOST).

Figure 7.8: *Vector plots showing CD biases.*

travels horizontally from right to left. This is illustrated in figure 7.10.

The boundaries between the write segments are potential sources for the observed mismatch, either through butting errors between the blocks or issues with timing of the electron beam and stage. All the structures in a row will have the same horizontal segment boundaries while structures in the same column should have the same vertical segment boundaries. It seems likely that the horizontal boundaries will have a greater effect on horizontal lines, for example if the segment boundary falls between the two lines. A similar effect would be expected for the vertical lines and vertical segment boundaries. From figure 7.9 it can be seen that structures in the same row tend to have approximately the same matching values, both vertical and horizontal, and this is especially true if the mismatch is quite large. However, there is no obvious agreement between structures in the same column. For example the CD bias vectors for the structures above and below the middle row are in almost the opposite directions. This perhaps suggests that the vertical segment boundaries have little effect on any of the matching structures and that instead the arrangement of the horizontal edges affects both pairs of structures. This result is perhaps not surprising due to the longer elapsed time and greater stage travel associated with writing segments that neighbour across the horizontal boundary.

From the write data and the positions of the centre points of the matching structure

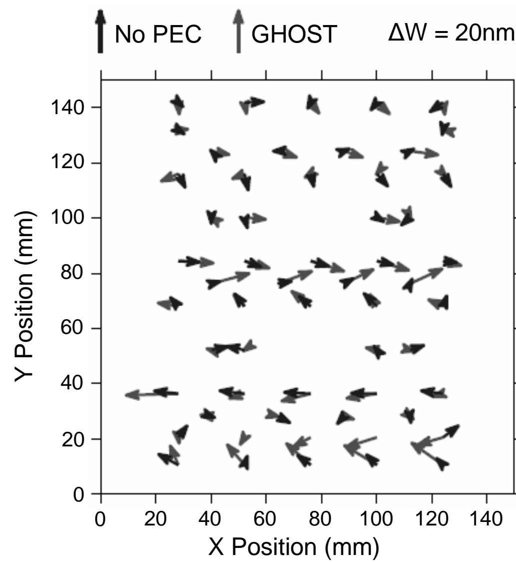


Figure 7.9: *Vector plot comparing CD biases on masks MSN5757 (No PEC) and MSN6659 (GHOST).*

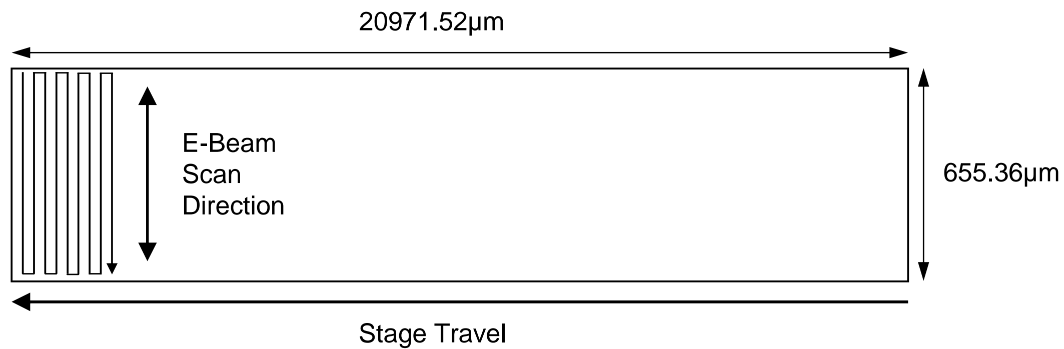


Figure 7.10: *Diagram illustrating the e-beam writing method.*

sets on the masks it is possible to determine the distance from the centre point to the closest vertical or horizontal segment boundary. If the vertical boundary is between 450μm and 510μm right of the centre point then it will lie between a pair of vertical lines. Similarly, if the horizontal boundary is within $\pm15\mu$m of the centre then it will lie between the horizontal lines. The boundary positions relative to each column and row of structures have been calculated and are presented in tables 7.1 and 7.2.

Table 7.1 suggests a reason for the lack of a systematic mismatch between structures which are in the same column. The closest that any vertical segment boundary gets to a matching structure set is 1281.13μm. This places it several hundred microns

Column Number	X Position (μm)	Boundary Distance (μm)
1	28200	7208.87
2	40200	-1739.55
3	52200	10229.55
4	64200	1281.13
5	76200	-7667.29
6	88200	4301.81
7	100200	-4646.6
8	112200	7322.5
9	124200	-1625.92

Table 7.1: *Distances of vertical segment boundaries from the centres of matching structures sets.*

Row Number	Y Position (μm)	Boundary Distance (μm)
1	10624	137.24
2	20624	306.84
3	28200	18.52
4	36412	-289.16
5	52200	-229.8
6	67987	-171.44
7	76200	177.24
8	84412	-130.44
9	100200	-71.08
10	115987	-12.72
11	124200	-319.4
12	131775	46.64
13	124200	216.24

Table 7.2: *Distances of horizontal segment boundaries from the centres of matching structures sets.*

away from the test structures and it is unlikely that it will have any significant effect. Table 7.2 shows only one row where the horizontal segment boundary is between the two measured lines. This is row 10, and on mask MSN5757 this row shows the largest mismatch between horizontal lines. However, this is not the case for mask MSN6659 which should have the same segment boundaries. Most of the other rows have horizontal boundaries which intersect with the measured part of the vertical lines. There is no obvious reason, however, why this should lead to a mismatch.

Although the source of the observed mismatch is unclear the electrical structures have demonstrated their usefulness in providing information about the capability of the mask making process. In addition, the electrical measurements have proved to be

extremely sensitive and repeatable. Measurements made several months apart on the same on-mask structure show variations in the measured resistances, in ΔR and ΔW/W of less than 1%. Table 7.3 shows the results of measuring a single pair of resistors at three different times, in a lab with no environmental control. The observed variation may be the result of changes in ambient temperature in the lab or instrument drift.

Measurement Time	R1 (Ω)	R2 (Ω)	ΔR (Ω)	ΔW/W (%)
April	30617.5	30449.0	168.5	-0.552
June	30771.2	30602.3	168.9	-0.55
October	30801.0	30632.2	168.8	-0.55

Table 7.3: *Variation of resistance measurement with time.*

7.2.4 Conclusions

On-mask electrical test structures consisting of pairs of Kelvin connected resistors have been designed to examine the capability of an advanced mask making process to produce identical isolated lines. Results from the prototype masks show systematic differences between adjacent resistor structures but the observed pattern of the mismatch data across the mask does not suggest an obvious process related source. The suggestion is that the data is a result of errors introduced by the electron-beam lithography tool used to print the features.

The electrical measurements have shown to be extremely repeatable and capable of revealing detailed information about the process capability. The requirement now is to further investigate the sources of the mismatch. This is done by analysis and redesign of the matching structure locations to more strategically probe the segment boundary positions. A number of plates have been fabricated with the new design, which is presented in the next section, with the the expectation that this may lead to improvements in the mask making process.

7.3 Electrical Characterisation for an Improved Photomask Design

7.3.1 Test Structures and Photomasks

New photomasks have been fabricated in order to further investigate the effects described in section 7.2.3. The primary plate used for this work (MSN7520 - NoPEC) can be seen in figure 7.11. This design takes advantage of the full available mask area and consists of an array of matching structures with a pitch of 6mm. The array of 357 sets of mismatch structures provides a volume of data which is larger than all of the masks presented earlier in this chapter and is without spatial gaps caused by the inclusion of other types of test structures. Each set of structures has a horizontal and a vertical pair of resistors, with the same dimensions as those described in section 7.2.1.

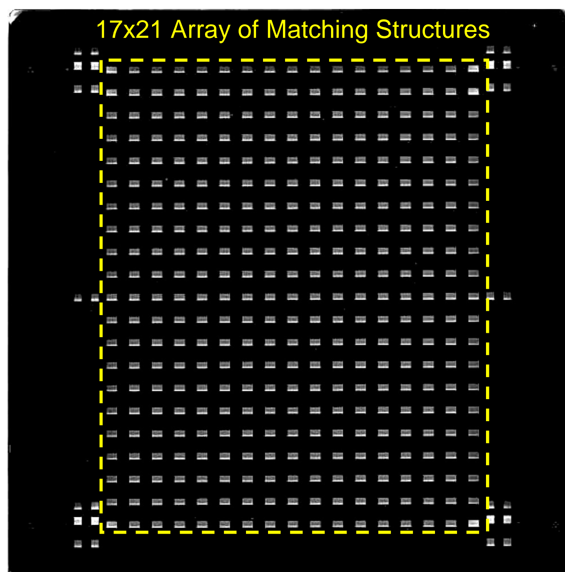


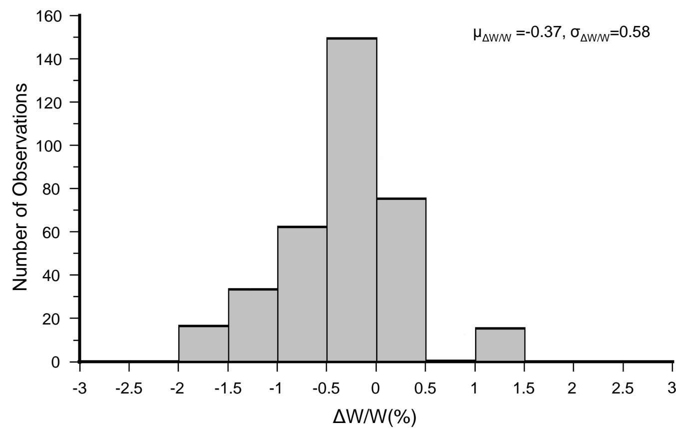
Figure 7.11: *Layout of photomask MSN7520.*

Mask MSN7520 was fabricated without any standard proximity correction techniques. A second photomask (MSN7544 - GHOST) was fabricated using the GHOST process [46] which attempts to correct for iso-dense bias effects. A problem with a low exposure dose meant that the mask was unsuitable for measurements. However, this turned out to be useful as the underexposed plate clearly shows the boundaries between the e-beam patterning segments. These boundaries were a possible source for the observed pattern of misalignment of section 7.2.3. As mask MSN7544 was

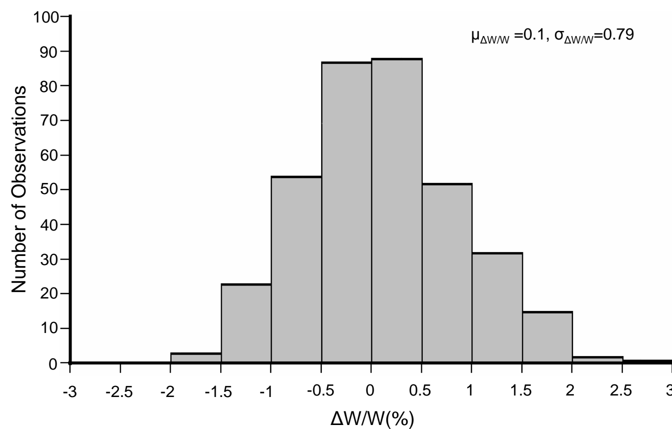
fabricated using the same lithography job file with MSN7520 it provides an opportunity for further investigation.

7.3.2 Measurements and Results

The measurement technique for the matching structures has been described in section 7.2.2. $\Delta W/W$ has been calculated for each pair of resistors on MSN7520 and the results from the horizontal and vertical lines are plotted as histograms in figures 7.12(a) and 7.12(b) respectively, which also show the mean (μ) and standard deviation (σ). The range of mismatch values for this mask is less than $\pm 2\%$ for the horizontal lines and less than $\pm 3\%$ for the vertical lines. This is comparable with the the results from the unGHOSTed mask MSN5757 in section 7.2.3.



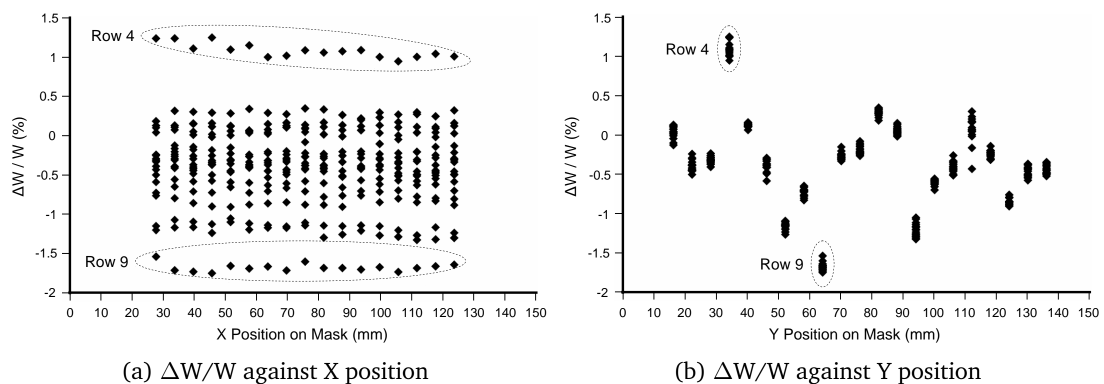
(a) Horizontal lines



(b) Vertical lines

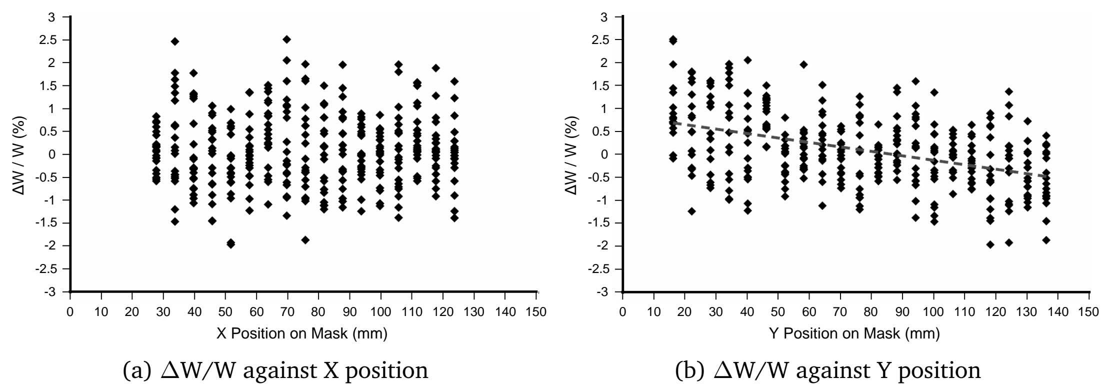
Figure 7.12: *Histograms of CD mismatch results for MSN7520 (No PEC).*

To determine if there are any trends in the measurement results which are related to the position of the structures on the mask the CD matching values are plotted against their horizontal or vertical position in figures 7.13 and 7.14. Figure 7.13(b) shows that the results for the horizontal lines are strongly grouped by row or vertical position. However there is no clear pattern to this or agreement between rows. The results from the vertical lines show a much more random distribution but there is a suggestion of a downward trend in ΔW/W from the bottom to the top of the mask. This is highlighted in figure 7.14(b) where a linear fit to the data has been made. However, this trend is relatively small compared to the range of variation in the data and so may not be significant.



(a) ΔW/W against X position (b) ΔW/W against Y position

Figure 7.13: *CD mismatch as a function of position for horizontal lines on MSN7520 (No PEC).*



(a) ΔW/W against X position (b) ΔW/W against Y position

Figure 7.14: *CD mismatch as a function of position for vertical lines on MSN7520 (No PEC).*

Figure 7.15 is a vector plot showing the linewidth offset (ΔW) in X and Y for each block of matching structures. Due to the fact that the linewidth values are calculated from an

assumed value of sheet resistance these results should be considered as indicative rather than showing absolute values of linewidth offset. This plot shows good agreement in the vertical component, taken from the horizontal lines, within each row. However, it also suggests there is some sort of pattern to the horizontal component that was masked by the way the data was represented in figure 7.14.

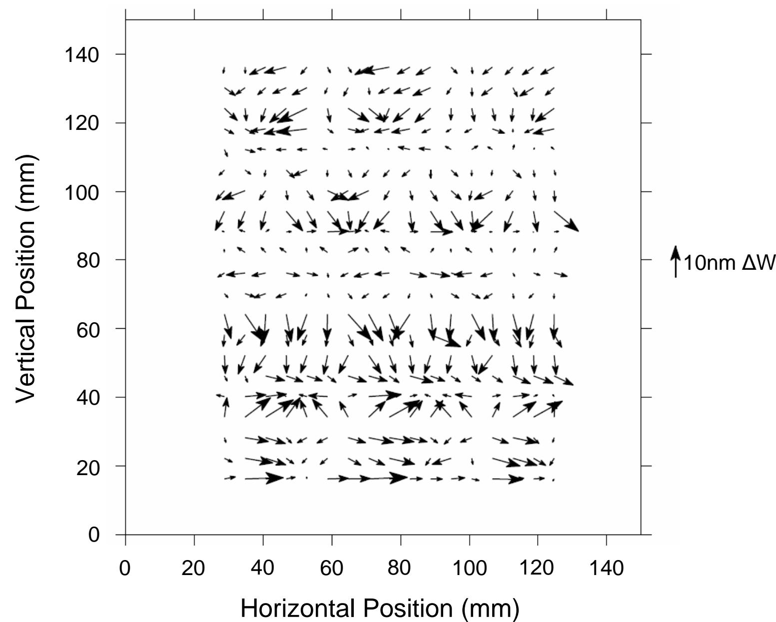
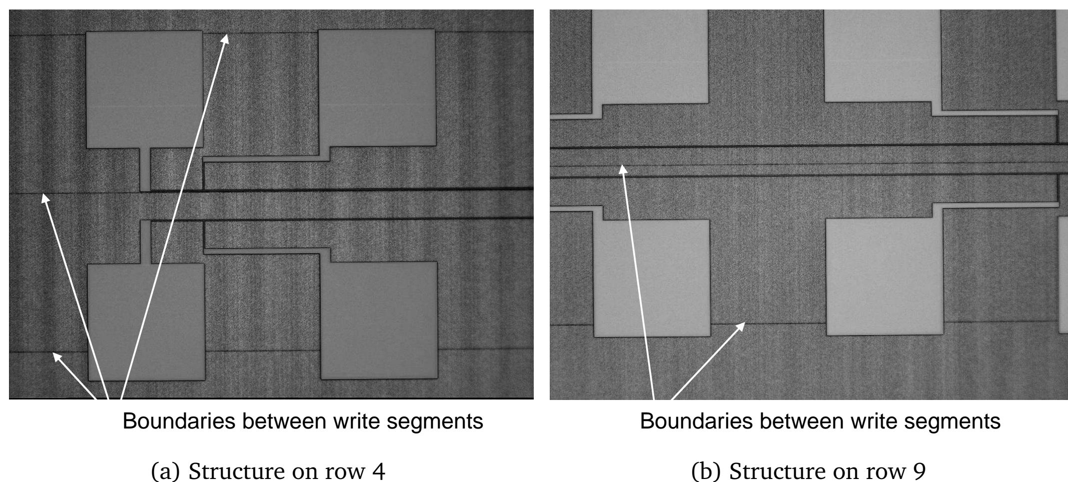


Figure 7.15: *Vector plot showing CD bias on MSN7520 (No PEC).*

Earlier in the chapter it was suggested that a possible source for the mismatch patterns observed on masks MSN5757 and MSN6659 was the position of the boundaries between the data segments in the mask writing tool. The data is sent to the mask writing tool in segments which are 20971.52μm wide by 655.36μm high and the patterns are written by moving the mask horizontally while the e-beam is scanned vertically. At the end of each segment a new set of data is loaded into the tool and the next segment in the row is written. When the edge of the plate is reached the mask is moved back to the start of the next row. This suggests that if there are any issues with differences between adjacent segments they are more likely to occur at the horizontal boundaries and will therefore affect horizontal lines more than vertical lines. It was suggested that this could be the source of the characteristic agreement within a row for horizontal lines as shown in 7.13(b). The highest and lowest values of mismatch are highlighted in this graph and are from rows 4 and 9.

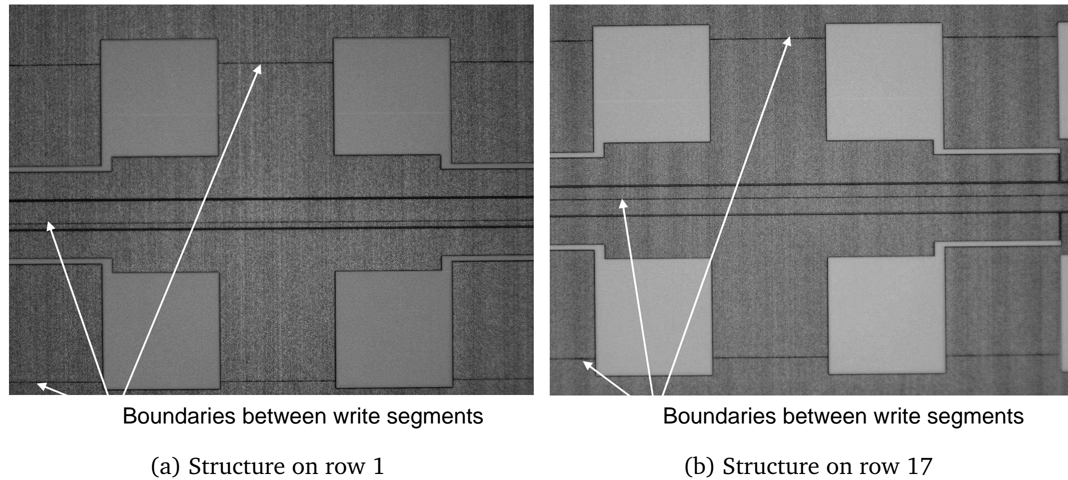
To highlight the physical positions of the write boundaries microscope images were taken from the underexposed mask MSN7544 presented in section 7.3.1. Figure 7.16 shows images with the write segment boundaries running through horizontal structures located in rows 4 and 9. It is clear from these images that the height of the write segments is not as defined (i.e. 655.36μm) and is in fact approximately 160μm. The height is the distance between two horizontal write segment boundaries as measured from the microscope images. The control system for the mask writing tool sends the data to a rasterising engine, which re-segments them to optimise the write operation. Although it is possible to define the dimensions of the data segments in the file sent to this system it is, unfortunately, practically impossible to determine exactly how this will be finally written by the lithography tool following rasterisation.



(a) Structure on row 4 (b) Structure on row 9

Figure 7.16: *Images of underexposed mask MSN7544 showing write segment boundaries.*

Both rows 4 and 9 have a horizontal segment boundary between the two horizontal lines and, in the case of row 4, it is within a few microns of one of the lines. Consequently it could be concluded that this might be the cause of the observed mismatch. However, images from rows 1 and 17 in figure 7.17 show that they also have a segment boundary which runs between the horizontal test structures and they have a mean mismatch which is close to zero. Similar images were taken of vertical test structures in each column of the array but only column 9 was observed to have a boundary running between the lines. There is no obvious consequence of this in the data in figure 7.14.



(a) Structure on row 1 (b) Structure on row 17

Figure 7.17: *Images of underexposed mask MSN7544 showing write segment boundaries.*

7.3.3 GHOST Proximity Corrected Photomasks

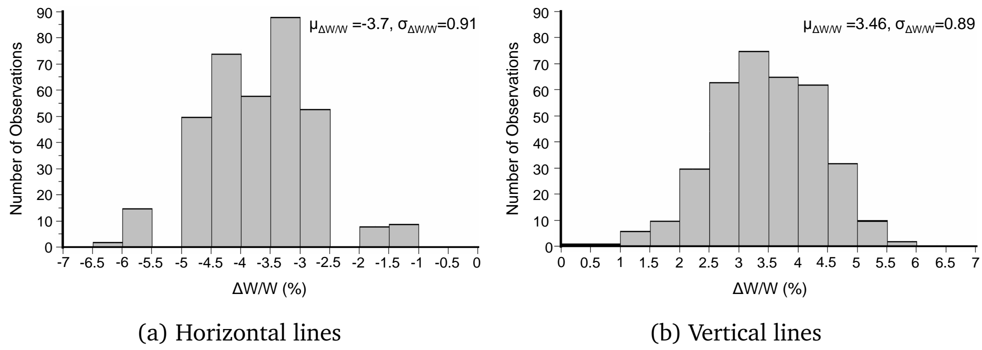
Two more masks were fabricated using the GHOST proximity correction technique [46] and the same regular array design of MSN7520. Mask (MSN7553 - GHOST) used the standard GHOST process where the secondary pattern was written with a larger grid size to speed up the process. In order to identify the source of the observed dimensional offsets, mask (MSN7864 - Slow GHOST) was fabricated using a process with the grid size kept the same on both exposures.

7.3.4 Results and Analysis

The full sets of horizontal and vertical matching structures have been measured on both MSN7553 and MSN7864 and the results are presented as histograms in figures 7.18 and 7.19 respectively. These graphs also show the mean values (μ) and standard deviations (σ).

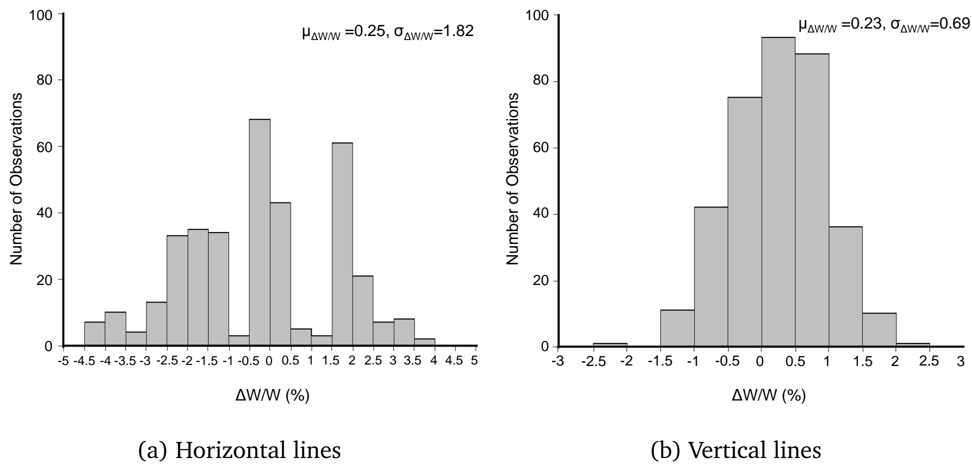
It can be observed that the systematic offsets observed on previous GHOSTed masks are also present on the MSN7553 using the standard GHOST process while the results from the Slow GHOST mask MSN7864 have mean values closer to zero. Table 7.4 summarises these results and includes data from the no PEC mask MSN7520.

The slow GHOST process reduces the mean mismatch to a similar level to that seen on the no PEC photomask MSN7520. However, it also appears to greatly increase the range



(a) Horizontal lines (b) Vertical lines

Figure 7.18: *Histograms of CD mismatch results for MSN7553 (GHOST).*



(a) Horizontal lines (b) Vertical lines

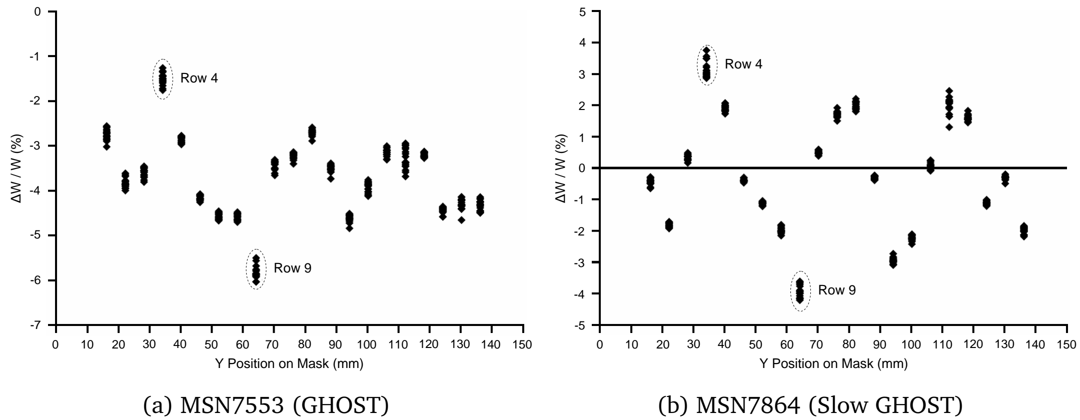
Figure 7.19: *Histograms of CD mismatch results for MSN7864 (Slow GHOST).*

of the results from the horizontal lines. It is clear that the results from the horizontal lines do not show a random, statistical variation. Therefore, the standard deviations given in figures 7.18(a) and 7.19(a) cannot be used to predict the distribution of ΔW/W. It is for that reason that the range value, representing the difference between maximum and minimum mismatch, is provided in table 7.4. The results presented earlier for horizontal structures on MSN7520 plotted against the vertical position on the mask show good agreement between structures in the same row. Similar results have been obtained for the two GHOSTed masks and can be seen in figure 7.20.

These results show a similar pattern to that observed for MSN7520, in particular with the maximum mismatch occurring in row 4 of the mask and the minimum in row 9. A possible reason for this was the fact that there is an e-beam pattern boundary which runs between the two horizontal lines on these rows. However, as previously noted

Mask MSN	Horizontal $\Delta W/W$ (%)			Vertical $\Delta W/W$ (%)		
	μ	σ	Range	μ	σ	Range
7520 (No PEC)	-0.37	0.58	3.01	0.1	0.79	4.48
7553 (GHOST)	-3.7	0.91	4.77	3.46	0.89	5.05
7864 (Slow GHOST)	-0.25	1.82	7.96	0.23	0.69	4.19

Table 7.4: *Comparison of matching results from three different masks.*



(a) MSN7553 (GHOST) (b) MSN7864 (Slow GHOST)

Figure 7.20: *CD mismatch as a function of vertical position for horizontal lines.*

there are also similar pattern boundary conditions on rows 1 and 17 which do not lead to large mismatches. The similarity between the results from the three masks for horizontal mismatch structures can be seen more clearly in figure 7.21 which plots the average mismatch for each row. The error bars, where visible, give the standard deviation of the mismatch across the 17 sets of structures in each row.

The data in figure 7.21 has been normalised in each case by subtracting the mean mismatch figure for the whole mask and it is clear that all three masks show the same overall pattern. However, the slow GHOST mask, MSN7864, shows much greater variation. One possible reason for this observed effect is interaction between the primary and secondary exposures in the GHOST process. These results confirm the suspicion that the systematic offset of around $\pm 3.5\%$ observed in the standard GHOSTed mask MSN7553 results are due to the fact that the secondary GHOST exposure is performed at a lower resolution. This means that the GHOST pattern overlaps the main pattern by 10nm on one side of each of the bridge resistors. However it is unclear how this leads to a systematic offset between the resistors in a pair as

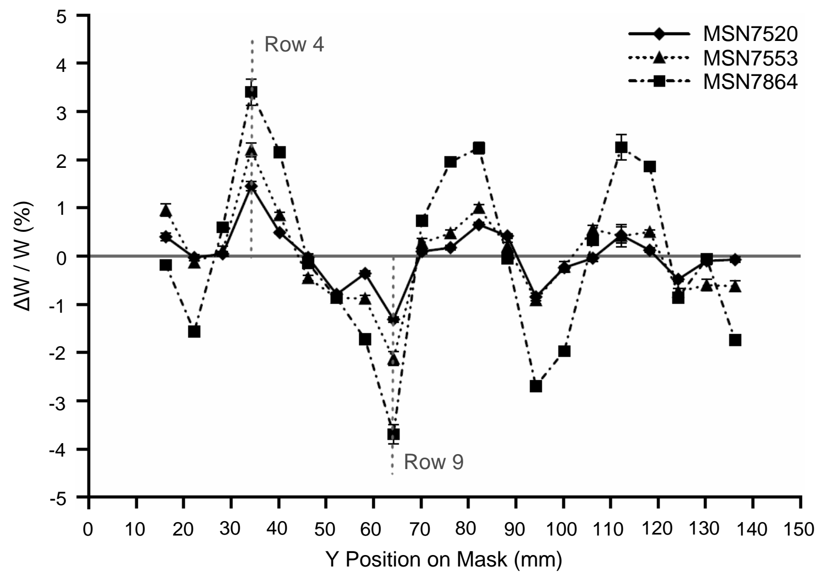
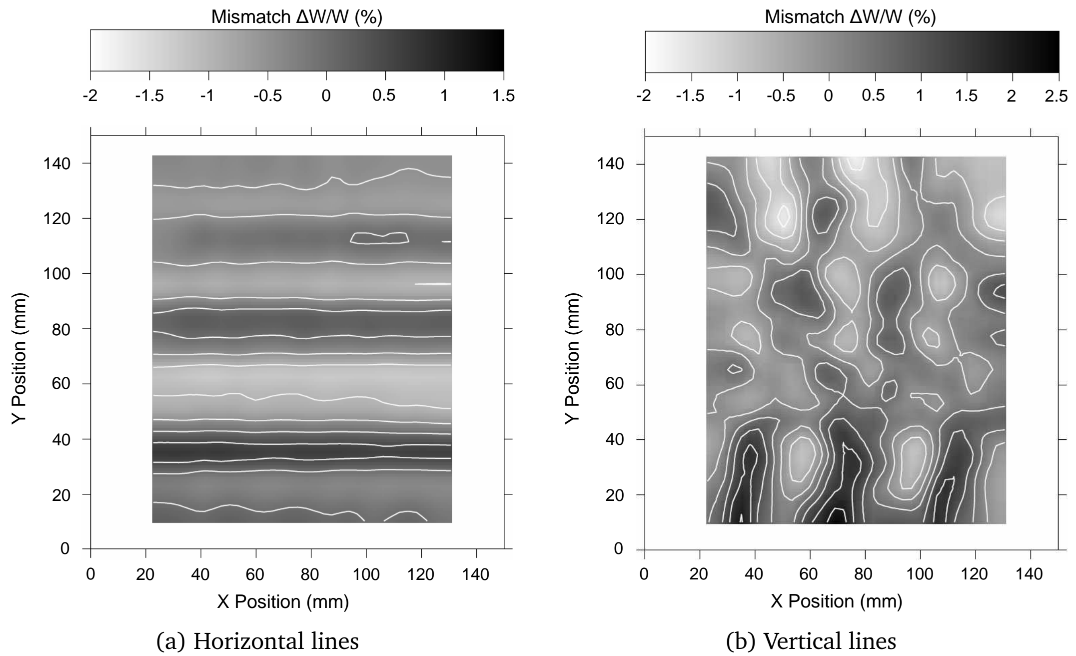


Figure 7.21: *Comparison of matching data for horizontal structures from three different photomasks.*

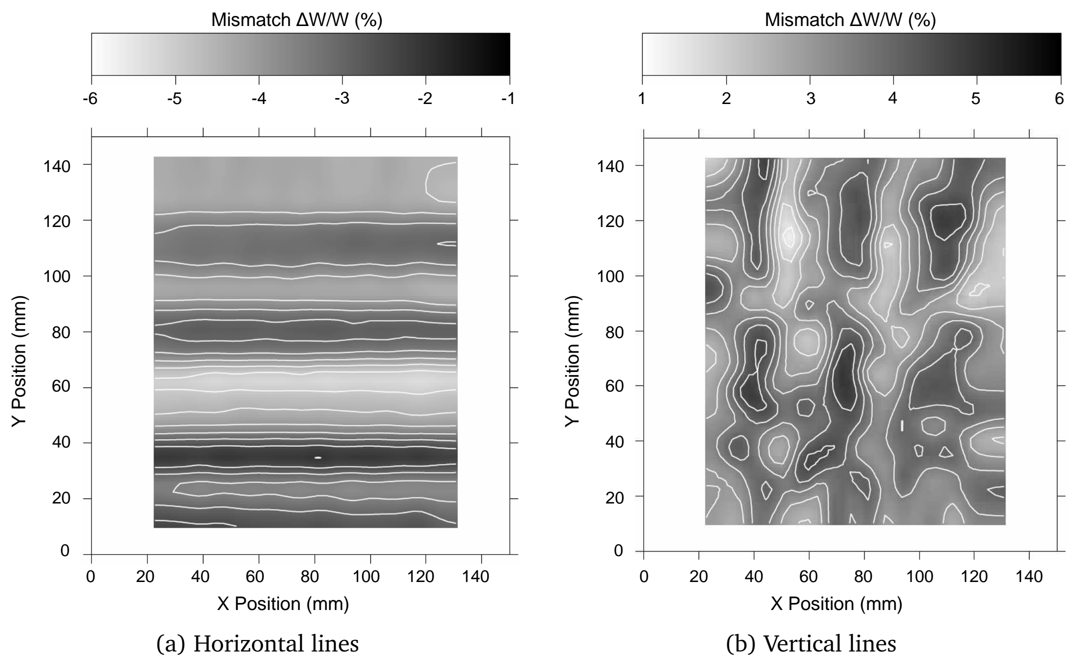
both should have similar secondary exposure patterns. In the slow GHOST mask the resolution of the secondary pattern is the same as the main pattern but the increased write time means that offsets between the two patterns are more likely. This obviously has a significant, adverse effect on the horizontal lines, increasing the mismatch range to more than $\pm 3\%$, equivalent to linewidth offsets of more than $\pm$15nm.

The vertical lines on MSN7864 do show the elimination of the systematic offset when compared with MSN7553 but they do not show an increase in the range of the mismatch results. As was noted earlier the pattern is split into write segments which are around 160μm high. This means that the vertical lines are split between several write segments while the horizontal lines are contained within a single segment. The result of this may be an averaging of adverse effects associated with the high resolution GHOST pattern. Although the mismatch results from the vertical lines appear to be randomly distributed in figures 7.18(b) and 7.19(b) this is not actually the case as can be seen in the contour plots of the mismatch from the vertical structures (figures 7.22(b), 7.23(b) and 7.24(b)). Similarly, clear patterns of horizontal bands can be seen in contour plots of results from the horizontal lines (figures 7.22(a), 7.23(a) and 7.24(a)).



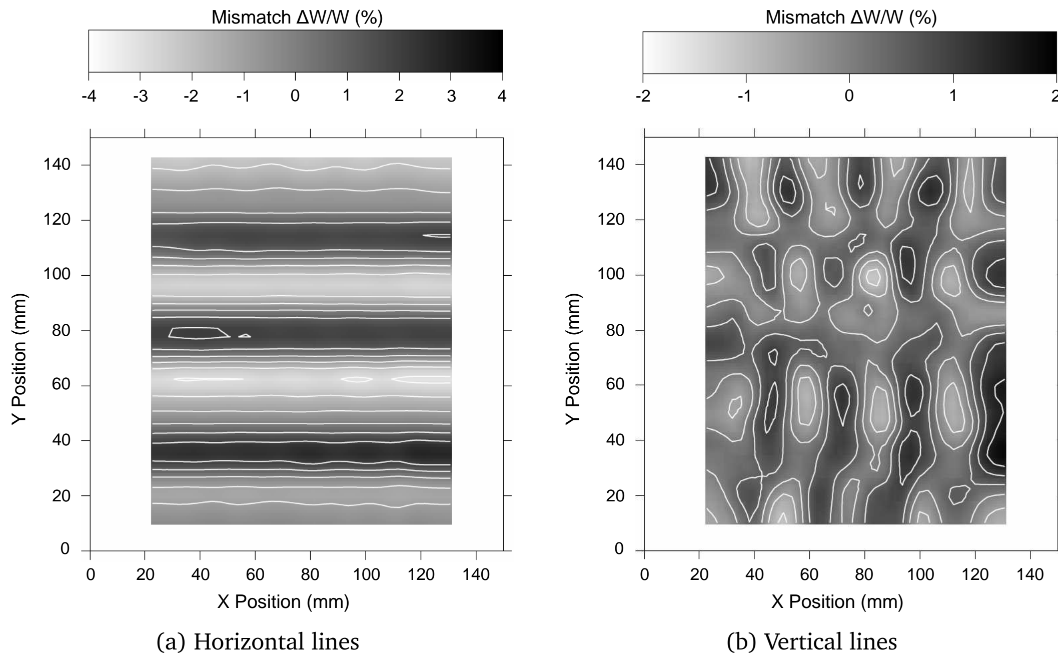
(a) Horizontal lines (b) Vertical lines

Figure 7.22: *Contour plots of CD mismatch data from MSN7520 (No PEC).*



(a) Horizontal lines (b) Vertical lines

Figure 7.23: *Contour plots of CD mismatch data from MSN7553 (GHOST).*



(a) Horizontal lines (b) Vertical lines

Figure 7.24: *Contour plots of CD mismatch data from MSN7864 (Slow GHOST).*

7.3.5 Conclusions

Electrical measurement results from mismatch resistor structures patterned as regular arrays on standard chrome-on-quartz photomask plates have been presented. The masks have nominally identical features but have been processed differently. Mask MSN7520 (No PEC), was processed without any correction for process or pattern dependent biases. MSN7553 (GHOST) has been prepared using a standard GHOST process commonly used to remove pattern dependent biases in electron-beam lithography. Finally, MSN7864 (Slow GHOST) used an adaption of this process in an attempt to identify the source of systematic dimensional offsets observed in results from mismatch test structures described in section 7.2.3. It was believed that the systematic mismatch observed in GHOSTed structures was due to the fact that the secondary GHOST pattern was printed with a lower resolution than the primary pattern. The slow GHOST process uses the same resolution for the secondary exposure, increasing the write time but removing any systematic offset between the patterns.

The effect of the slow GHOST process on both horizontal and vertical lines was to remove the overall systematic bias as expected. However, it also had the effect of significantly increasing the overall range of the mismatch results for horizontal lines. It

is likely that the increased write times involved in the slow GHOST process exacerbate the tool induced pattern seen in figure 7.21. Contour plots of mismatch data from the three masks show a clear, row by row, pattern in the mismatch data from horizontal lines which is similar for each mask. However, the range of the mismatch variation increases from mask to mask as the write time gets progressively longer for the no PEC, GHOST and slow GHOST write strategies. This suggests that the increased write time could be compromising the re-registration performance of the write tool in some way, perhaps by a mechanism such as thermal drift within the mask writing chamber. Although the mismatch data from the vertical lines appears at first to be more randomly distributed, a clear pattern emerges in the contour plots. However, unlike the results for the horizontal structures the pattern is significantly different in each case. Overall, the application of either GHOST process has little effect on the range of the results from the vertical structures and only affects the mean value. GHOST processing has a much more significant effect on the horizontal structures, with the slow GHOST process in particular leading to mismatches of as much as $\pm4\%$ or $\pm$20nm. This is understandable since for the vertical structures the variation in registration of the scanned beam will tend to contribute to the line edge roughness rather than shifting the whole edge as would be the case for the horizontal lines. This effect would explain the lower measured range for the vertical features. Vertical lines will have their width governed by the electron beam being blanked on or off rather than its scanned position and will therefore be less prone to linewidth variation from registration drifts.

Chapter 8
Conclusions and Further Work

This thesis has presented the results of investigations of applications of electrical test structures and measurement techniques for the characterisation of advanced photomasks. This final chapter begins by briefly covering the important conclusions made in each of the preceding chapters. The chapter ends with describing some areas for future investigation that have been suggested by this work.

8.1 Conclusions

8.1.1 Linewidth Measurement Techniques for the Characterisation of Binary and Alternating Aperture Phase-Shifting Masks

The use of electrical linewidth test structures for binary and alternating phase-shifting mask metrology was investigated in Chapter 3. Two photomasks were fabricated featuring a large number of on-mask test structures with a range of different linewidths and line to space ratios. Some of the structures were binary and some phase-shifted. The masks are capable of being used to print test structures on-wafer which can also be electrically tested. The linewidths of one complete set of binary and one set of phase-shifted structures were measured electrically and optically on both masks.

The ECD results from both binary and phase-shifted features track each other very closely. For most features, the optical measurements also track each other, but the alternating phase-shifting elements have a significant effect on the optical measurement, leading to an offset between the binary and phase-shifted results. Another issue with the optical measurements is the difference between the results from dense and isolated binary structures. While the optical and electrical measurements of the most dense structures track each other with a reasonably constant offset, the same cannot be said for the more isolated lines with dimensions below 800nm. The optical and electrical results do not agree and, as the ECD measurements are not affected by

proximity, this suggests that the optical system is struggling to measure these features accurately.

Finally for one of the photomasks where the designed CD for the phase-shifting features is less than 600nm, the optical measurement fails and the phase-shifted lines appear significantly wider than indicated by the electrical tests. This optical effect was found to be caused by the misalignment between the two masking layers. However, in this study it is the combination of different types of inspection methods which helped identify the misalignment between the mask layers. This is clearly the case where the use of more than one measurement technique, complementing each other, can prove valuable when characterising an advanced photomask process.

8.1.2 Development of Electrical On-Mask CD Test Structures Based On Optical Metrology Features

The work presented in Chapter 4 proposed test structures which are electrical equivalents to a set of industry standard optical/SEM test sites, normally used for investigating proximity distortion effects.

In section 4.2, part of the Mentor Graphics metrology reference test set formed the basis for the design and fabrication of direct on-mask electrical structures to allow the measurement of linewidth and line-spacing on these features. A prototype binary mask was fabricated with cross-bridge and split-cross-bridge test structures to measure isolated and dense patterns. Electrical and optical measurements were made on these structures and the ECD results of section 4.3 have been shown to outperform industry standard optical mask metrology and verification methods, especially for deep sub-micron dimensions. The results suggested that the electrical technique is not affected by the type, dimension, density or the proximity of the features, unlike the optical technique where proximity effects are compounded with the measurement itself. This is very important as effects seen when electrically characterising a feature can be more confidently attributed to the mask fabrication process and not to the measurement technique.

Section 4.4 investigated the feasibility of adapting optical measurement patterns to electrical equivalent structures, which measure the separation between line, space

and corner ends, as well as the dimensions of contacts and holes. Simulations were performed to examine the sensitivity of capacitive and resistive structures to feature dimension variations. It was found that for most test patterns, an interdigitated capacitor design could have the sensitivity required for detecting any changes in feature dimensions. This test structure has a smaller footprint than the simple capacitive equivalents, which would be too large to be fabricated on a standard photomask. In addition, two resistive structures were proposed, one of which is a modified cross-bridge structure.

8.1.3 Comparison of Metrology Techniques for the Characterisation of Advanced Photomask Processes

Chapter 5 demonstrates the strength of on-mask electrical measurements to characterise advanced photomasks and compares the measurement results with state-of-the-art metrology tools. Section 5.2 described the design and fabrication of binary, on-mask electrical test structures on a chrome-on-quartz plate that was written using the GHOST proximity correction technique. Both electrical and optical measurements have been performed on isolated and dense line/space features and the analysis has shown that GHOST correction has a significant, and positive, effect on the mask manufacturing process. However, the test structures have highlighted that there are limitations associated with the procedure, which depends on the density and dimensions of the features being fabricated. Furthermore, comparisons between electrical and optical measurements showed how ambiguities in the optical measurement may affect the interpretation of the capability of the mask making process.

Section 5.3 presented a comparison between electrical, optical and CD-AFM measurements. These different techniques were used to measure the linewidths of submicron isolated chrome features. The CD-AFM measurements were made with a system, which is calibrated using a traceable standard and showed excellent agreement with the ECD measurements. The offset was less than $\pm$10nm and showed no systematic dependence upon nominal size over the range of dimensions measured. This was not the case with the optical measurements which overestimated the width of these features by as much as 90nm. The optical results also showed a dependence

on the nominal width with the offset reducing as dimensions increase. An initial analysis of the measurement uncertainties for each technique was also made. The good agreement between the independent electrical and calibrated CD-AFM measurements suggests that a CD standard for binary masks may be definable.

8.1.4 Electrical Test Structures for the Characterisation of Optical Proximity Correction

In Chapter 6, a Kelvin connected resistor structure was used to demonstrate the feasibility of extending electrical measurement techniques to the characterisation of corner serif OPC features. A prototype photomask was fabricated which contained arrays of on-mask and printable corner test structures, with different levels of OPC aggressiveness. The results from the work in sections 6.3 and 6.4 have shown that the electrical technique is sensitive enough to measure the effects of inner corner structures reliably and in good agreement with theoretical predictions. This agreement is a good indication that it is the material physically present on the mask which is being characterised. Any departures from the simulated results have been found to be attributable to defects in the serif structure. Furthermore, an optical microscope, a dedicated optical mask metrology system, an AFM scanner and finally a FIB system, were used to characterise the effects observed electrically. Overall, the electrical measurements were able to observe the degree of aggressiveness of the OPC and could potentially be employed for monitoring the OPC pattern transfer process onto masks.

Section 6.5 investigated the impact of the corner features on structures printed on-wafer. Results of electrical measurements of polysilicon test structures printed using the previously measured photomask suggest that OPC applied to the inner corner has a significantly greater effect on the resistance than outer corner serifs. SEM imaging of the test structure geometries confirmed that OPC does alter the shape of corner rounding on both the inner and outer corners. However, it appears that, unlike measurements on the mask, the effects of OPC are confounded by other fabrication artefacts. Whilst the measurement technique is restricted in practical application to inner corner serifs, it is this circuit feature that is most relevant to achieving the desired device electrical performance.

8.1.5 Matching Resistor Test Structures for the Characterisation of the Photomask Fabrication Process

Chapter 7 investigated the use of on-mask, electrical, mismatch test structures and measurement techniques to characterise the capability of an advanced mask making process. The test structures consist of pairs of identically designed Kelvin connected bridge resistors that can be measured simultaneously. Results from the prototype masks showed systematic differences between adjacent resistor structures. However, the observed pattern of the mismatch data across the mask did not suggest an obvious process related source but a result of errors introduced by the electron-beam lithography tool used to print the features. The larger systematic mismatch observed on the GHOST proximity corrected mask, was believed to be due to a difference in resolution between primary and secondary exposures, that caused an overlap between the primary and GHOST patterns.

Section 7.3 described the fabrication and measurement analysis of matching structures on a set of advanced photomasks, which have nominally identical features but have been processed differently. This design takes advantage of the full mask area and consists of a regular array of structures, which provides a greater volume of data. A modified GHOST process was used on one mask, to confirm that the systematic mismatch observed in GHOSTed structures was due to the fact that the secondary GHOST pattern was printed with a lower resolution than the primary pattern. The slow GHOST processed mask, used the same resolution for the secondary exposure, which removed the overall systematic bias at a cost of an increased write time. In addition, it was found that the range of the mismatch variation increased from mask to mask as the write time got progressively longer.

Overall, the electrical measurements have shown to be extremely repeatable and capable of revealing tool and process induced dimensional mismatches in the nanometer range on masks, which could otherwise prove difficult with standard optical metrology techniques.

8.2 Further Work

A number of suggestions for further work have arisen from the work presented in this thesis. One of the major attractions of the mask metrology method, is that similar structures can be printed with the test masks and measured on-wafer using the same electrical techniques. The photomasks used in Chapters 3-5 contain structures with probe pads scaled appropriately for reduction lithography but the same dimensions for the measured features as the on-mask structures. Measurements of structures in silicon will be compared with those from the mask and the offsets or non-linearities determined. This will provide information about the Mask Error Enhancement Factor (MEEF) of the photolithographic process. On-mask CD values can be obtained by using electrical measurements techniques, but a very important issue is how this actually relates to the on-wafer printed features. Finally, printable versions of the matching test structures described in Chapter 7, can also be designed to examine the capability of a photolithographic process to produce identical features.

Further work arises from the investigation on phase-shifting mask metrology in Chapter 3. At present, the most commonly used form of phase-shifting technology is attenuated PSM, where the chrome blocking features are replaced by a semi-transparent material. A common material is molybdenum silicide oxynitride, which unfortunately is unsuitable for direct probing. However, the fabrication process of these masks uses a chrome layer during patterning and it should be possible to apply the test structures and electrical measurement methods before the Cr is removed. The attenuated photomasks can then be used to print structures in order investigate pattern transfer.

In Chapter 4, simulations were used to investigate the feasibility of adapting optical measurement patterns to electrical equivalents. There is plenty of scope for further investigation examining the issues with the measurement of these features. The next step would be to correlate capacitance and resistance measurements to the actual feature dimension that is being investigated. The proposed test structures should be designed and fabricated on-mask in an attempt to confirm that the measurement methodologies drawn from the simulation results are valid.

Further on-wafer measurements were made on corner OPC polysilicon test structures, as part of the work presented in Chapter 6. The data suggest that OPC on the outside

corner has little impact upon the performance of a simple circuit, but care should be taken with OPC on the inner corners, particularly with regard to the size of the OPC serifs used. The level of corner rounding is dependent upon the dimensions of the serifs employed and the measured resistance can be used to characterise the effects of different levels of OPC applied to the inner corners. Two papers have been prepared with this recent work (see section A.2), one submitted to the IEEE Transactions on Semiconductor Manufacturing and one presented at the SPIE Photomask Technology 2009 [152].

The initial work was completed at a lithographic k_1 value of 0.5. Further work using lower k_1 factors and narrower lines would be useful to verify if the effect is the same, or indeed more critical, as the width of the polysilicon line narrows. It would also be useful to determine if this relationship is maintained when the conducting material is a metal with much lower resistance. This knowledge would be relevant as technology is moving forward into the realm where metal rather than polysilicon transistor gates are used. The same structures have been recently patterned in a thin layer of aluminium and a paper with the initial results of this work will be submitted to IEEE Conference of Microelectronic Test Structures 2010 (see section A.2).

8.3 Final Conclusions

The work presented in this thesis has shown a novel application of electrical test structures and measurement techniques to characterise advanced photomasks. It is a transferable metrology from mask to wafer, which can provide the ultimate measurement, to confirm that a photomask pattern can be transfered onto the wafer. Traditionally, optical and CD-SEM metrology have been the verification methods in photomask fabrication environments. However, as these techniques continue to be challenged, the development of new technologies is critical. Although electrical techniques require a conducting layer, this is not a problem for the most widely used photomask types. In addition, as this work has demonstrated, they do have the high repeatability and accuracy required for metrology in the future. Some of the structures are of the earliest to be reported in the field, and have been able to benefit of all developments that have been made over time. These electrical techniques still have important applications today and will almost certainly remain as important in the

future.

According to the International Technology Roadmap for Semiconductors [20], by 2015 CD measurement techniques have to be capable of measuring linewidths of 10nm with an uncertainty of 1nm. Mask feature dimensions are normally 4$\times$ or 5$\times$ larger than wafer. However, even these requirements are a challenge to existing measurement capabilities. This thesis has presented and analysed test structures and measurement techniques for the electrical charecterisation of photomasks, providing a greater insight into their operation. The results of this study will help to develop the appropriate metrology for current and future mask technologies.

Appendix A
Publications

A.1 Published Papers

The following papers written by the author of this thesis have been published in conference proceedings or in a peer reviewed journal:

- S. Smith, A. Tsiamis, M. McCallum, A.C. Hourd, J.T.M. Stevenson and A.J. Walton "Comparison of Optical and Electrical Measurement Techniques for CD Metrology on Alternating Aperture Phase-Shifting Masks" in Proceedings of IEEE International Conference on Microelectronic Test Structures, Austin, Texas, USA, Mar. 2006, pp. 119–123.

- Andreas Tsiamis, Stewart Smith, Martin McCallum, Andrew C. Hourd, J. Tom M. Stevenson and Anthony J. Walton "Electrical Test Structures for the Characterisation of Optical Proximity Correction" in Proceedings of the SPIE, vol. 6533: 23rd European Mask and Lithography Conference, Grenoble, France, Jan. 2007, 65330M.

- S. Smith, A. Tsiamis, M. McCallum, A.C. Hourd, J.T.M. Stevenson and A.J. Walton "Electrical Measurement of On-Mask Mismatch Resistor Structures" in Proceedings of IEEE International Conference on Microelectronic Test Structures, Tokyo, Japan, Mar. 2007, pp. 3–8.

- A. Tsiamis, S. Smith, M. McCallum, A.C. Hourd, O. Toublan, J.T.M. Stevenson and A.J. Walton "Development of Electrical On-Mask CD Test Structures Based on Optical Metrology Features" in Proceedings of IEEE International Conference on Microelectronic Test Structures, Tokyo, Japan, Mar. 2007, pp. 171–176.

- Ronald Dixson, Ndubuisi G. Orji, James Potzick, Joseph Fu, Richard A. Allen, Michael Cresswell, Stewart Smith, Anthony J. Walton and Andreas Tsiamis "Photomask Applications of Traceable Atomic Force Microscope Dimensional

Metrology at NIST" in Proceedings of the SPIE, vol. 6730: Photomask Technology 2007, Monterey, California, USA, Sep. 2007, 67303D.

- A. Tsiamis, S. Smith, M. McCallum, A.C. Hourd, O. Toublan, J.T.M. Stevenson and A.J. Walton "Investigation of Electrical and Optical CD Measurement Techniques for the Characterisation of On-Mask GHOST Proximity Corrected Features" in Proceedings of IEEE International Conference on Microelectronic Test Structures, Edinburgh, UK, Mar. 2008, pp. 29−34.

- S. Smith, A. Tsiamis, M. McCallum, A.C. Hourd, J.T.M. Stevenson, A.J. Walton, R.G. Dixson, R.A. Allen, J.E. Potzick , M.W. Cresswell and N.G Orji "Comparison of Measurement Techniques for Advanced Photomask Metrology" in Proceedings of IEEE International Conference on Microelectronic Test Structures, Edinburgh, UK, Mar. 2008, pp. 35−39.

- S. Smith, A. Tsiamis, M. McCallum, A.C. Hourd, J.T.M. Stevenson and A.J. Walton "On-Mask Mismatch Resistor Structures for the Characterisation of Maskmaking Capability" in Proceedings of IEEE International Conference on Microelectronic Test Structures, Edinburgh, UK, Mar. 2008, pp. 228−232.

- S. Smith, A. Tsiamis, M. McCallum, A.C. Hourd, J.T.M. Stevenson and A.J. Walton "Comparison of Optical and Electrical Techniques for Dimensional Metrology on Alternating Aperture Phase-Shifting Masks" in IEEE Transactions of Semiconductor Manufacturing, May 2008, vol. 21, no 2, pp. 154−160.

- S. Smith, A. Tsiamis, M. McCallum, A.C. Hourd, J.T.M. Stevenson, A.J. Walton, R.G. Dixson, R.A. Allen, J.E. Potzick, M.W. Cresswell and N.G. Orji "Comparison of Measurement Techniques for Linewidth Metrology on Advanced Photomasks" in IEEE Transactions of Semiconductor Manufacturing, February 2009, vol. 22, no 1, pp. 72−77.

- S. Smith, A. Tsiamis, M. McCallum, A.C. Hourd, J.T.M. Stevenson and A.J. Walton "Application of Matching Structures to Identify the Source of Systematic Dimensional Offsets in GHOST Proximity Corrected Photomasks" in Proceedings of IEEE International Conference on Microelectronic Test Structures, Oxnard, CA, USA, Mar. 2009, pp. 50−55.

- A. Tsiamis, S. Smith, M. McCallum, A.C. Hourd, J.T.M. Stevenson and A.J. Walton "Electrical Test Structures for Investigating the Effects of Optical Proximity Correction" in Proceedings of IEEE International Conference on Microelectronic Test Structures, Oxnard, CA, USA, Mar. 2009, pp. 162−167.

A.2 Further Work

In this section, reprints of two full papers and a four page abstract are presented. The first paper has been recently presented at SPIE Photomask Technology 2009 and published in the conference proceedings.

- M. McCallum, A. Tsiamis, S. Smith, A.C. Hourd, J.T.M. Stevenson and A.J. Walton "Practical Application of OPC in Electrical Circuits" in Proceedings of the SPIE, vol. 7488: Photomask Technology 2009, Monterey, California, USA, Sep. 2009, 74883B. *See figures A.1 to A.7.*

The second paper has been submitted for publication to the IEEE Transactions on Semiconductor Manufacturing.

- A. Tsiamis, S. Smith, M. McCallum, A.C. Hourd, J.T.M. Stevenson and A.J. Walton "Electrical Test Structures for the Characterisation of Optical Proximity Correction". *See figures A.8 to A.25.*

The four page abstract will be submitted to the IEEE International Conference on Microelectronic Test Structures 2010.

- S. Smith, A. Tsiamis, M. McCallum, A.C. Hourd, J.T.M. Stevenson and A.J. Walton "Kelvin Resistor Structures for the Investigation of Corner Serif Proximity Correction". *See figures A.26 to A.29.*

Practical Application of OPC in Electrical Circuits

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ABSTRACT

Today's Optical Proximity Correction (OPC) is becoming increasingly complex and necessitates using smaller and smaller grid sizes to produce the fine patterns required. These small grids lead to very high overhead in data handling, as well as for the tools that will write and inspect the mask; which together make masks extremely expensive. For two dimensional structures such as corners, we use complex structures incorporating either additive or subtractive OPC features to produce the desired shape. It is unclear though, how precisely the final structures must match the original design to perform their intended electrical functions. In this work we have created a number of corner type electrical test structures and applied different degrees of OPC to both the outer and inner corners of the structures. These features were then printed on doped polysilicon wafers, and the wafers were etched and electrically tested. The electrical effect of OPC on the outer corner was found to be minimal, whereas the inner corner shape had a significant effect upon the electrical resistance of the circuit feature. The data suggests that OPC on the outside corner has little impact upon a simple circuit's performance, but care should be taken with OPC on the inner corners, particularly with regard to the size of the OPC serifs used.

Keywords: OPC, corner rounding, electrical test structure

1. INTRODUCTION

OPC was first considered for microlithography with imaging systems in the early 1980's [1] although the technique was proposed many years before then [2]; however, it was not until the 1990's that commercial application of this technique for chip fabrication became available [3]. Throughout the development of OPC, its primary purpose has been to correct the shape printed upon the wafer to replicate the original mask feature design as closely as possible. This has resulted in OPC application and verification being performed using increasingly complicated optical models [4]. In addition, the shapes appearing on masks are becoming more and more abstract when compared to the final desired pattern. This has resulted in masks being drawn on small grid squares requiring long write times, difficult inspections, and increasingly high prices. Throughout the progression of OPC technology though, uncertainty has remained regarding how close to the originally drawn shape that the printed circuit features on the wafer must be to enable the circuit to function correctly. While this is likely to vary from one circuit to another, if specific circuits' functionality can be maintained while the pattern on the wafer is not 'ideal', then there is the potential to reduce mask costs significantly.

2. METHOD

In this paper we studied two dimensional corner structures which typically have serif-type OPC added [5]. Structures that can be tested electrically were built using Kelvin connected resistors consisting of a short section of track turning through a right

Figure A.1: *Reprint of paper presented at the SPIE Photomask Technology 2009, page 1.*

angled corner, as shown in figure 1. To measure the resistance of the track, a current is forced between pads B and D and the resulting potential difference is measured at pads A and C. The resistance of the section of track between the voltage taps is then calculated with:

$$R = \frac{V_{AC}}{I_{BD}} \quad (1)$$

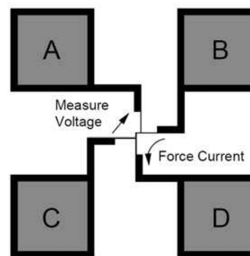

Figure 1. The Kelvin connected resistor structures

The effect of OPC was investigated by altering the layout of the right angled corner of the structure. This was achieved by adding a square serif pattern to the outside of the corner, whilst a square is removed from the inside, as illustrated in figure 2. The size of the squares for the inner and outer corner (Wi or Wo), together with the amount by which it overlaps with, or protrudes from, the original layout (Di or Do) were varied. The Wi/Wo variation is defined as fractions of the base CD: 0.25, 0.3, 0.35, 0.4, 0.45 and 0.5. Subsequently, the value of Di or Do is then defined as some fraction of Wi or Wo: 0.25, 0.5 or 0.75. These were arranged in a 19 x 19 array in which each column has a different value of Wi and Di, while each row has a different value of Wo and Do.

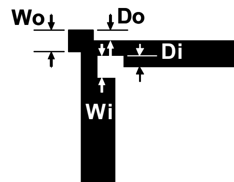

Figure 2.Diagram of the corner structure showing positions of the varied parameters.

The test structures were written on a chrome binary mask at 5X nominal using a MEBES 5500 e-beam lithography system using GHOST, processed on a Steag Hamatech ASE 5000 and then dry etched using a Unaxis Versalock 700 Mask Etcher. Nominal CD measurements were made optically using a MueTec <M5k> system.

Wafers were then prepared for printing. 200mm wafers had 500nm of oxide grown, then 300nm of polysilicon was deposited and doped using ion implantation to deliver a sheet resistance of 95-98 ohm/square (measured by four point probe.) Wafer printing was then performed using Rohm and Haas Ultra-i 123 resist on a Nikon NSR-2005i9C stepper with a numerical aperture (NA) of 0.5. After development, the polysilicon was etched in a reactive ion etch tool before passivation with a

Figure A.2: *Reprint of paper presented at the SPIE Photomask Technology 2009, page 2.*

0.5µm thick layer of PECVD silicon oxide. Holes in the oxide were then etched over the probe pads prior to deposition of a 500nm thick layer of sputtered aluminium. The final step was then to pattern the aluminium to create contacts suitable for probing. An image of the final structure can be seen in figure 3.

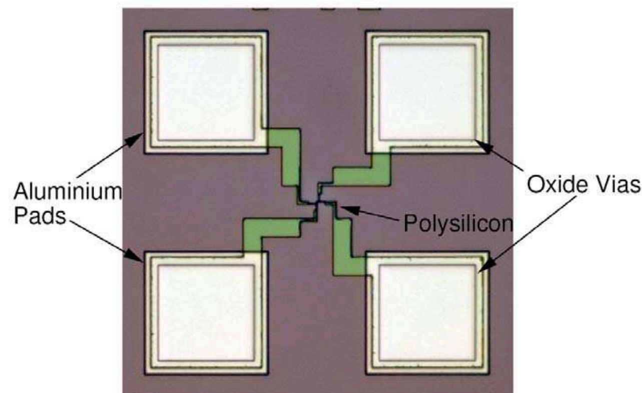

Figure 3. Optical Lithograph of the final test structure.

Electrical testing of the features utilised a semi-automatic prober using an HP-4062UX test system and a force current of 500µA.

3. RESULTS

The 320nm (at the wafer scale) features, corresponding to a k_1 of 0.44, were used for electrical resistance measurement. Imaging at such a low k_1 factor requires OPC; therefore these features were considered representative of typical OPC usage. The electrical measurements taken were analysed for each of the different OPC conditions, i.e. for both inner and outer corner OPC with the following conditions:

i) by varying the size of each corner serif (W) for different overlap positions (D)
ii) by varying the amount of overlap (D) for each size of OPC (W)

For easier interpretation, the data has been graphed and is shown in the figures below. The notation used is such that the letter "i" is added after the W or D for inner corner and the letter "o" for outer corner. The number following is a ratio against the nominal CD used, in this case 320nm. As such, Di0.25 is an overlap of 80nm (0.25 x 320nm) on the inner corner, and Wo0.5 is a 160nm serif (0.5 x 320nm) on the outer corner.

3.1. Variation of OPC on the inner corner

Figure 4 shows the variation of the size of the inner serif (Wi), for the smallest (Di=0.25) and largest (Di=0.75) overlaps, for each of the smallest (Wo=0.25) and largest outer (Wo=0.50) serifs. A clear trend of increasing electrical resistance is observed as the serif size gets larger and lesser amounts of material are present on the inner corner.

Figure 5 shows variation of the position of the inner serif (Di) (also referred to as the overlap) for the smallest (0.25) and largest (0.5) inner serifs (Wi), for each of the smallest and largest outer serifs (Wo). In the case of the smallest overlap, there is no clear dependence of the electrical resistance on the size of the serif. However, in the case of the largest overlap, some weak dependence appears to exist.

Figure A.3: *Reprint of paper presented at the SPIE Photomask Technology 2009, page 3.*

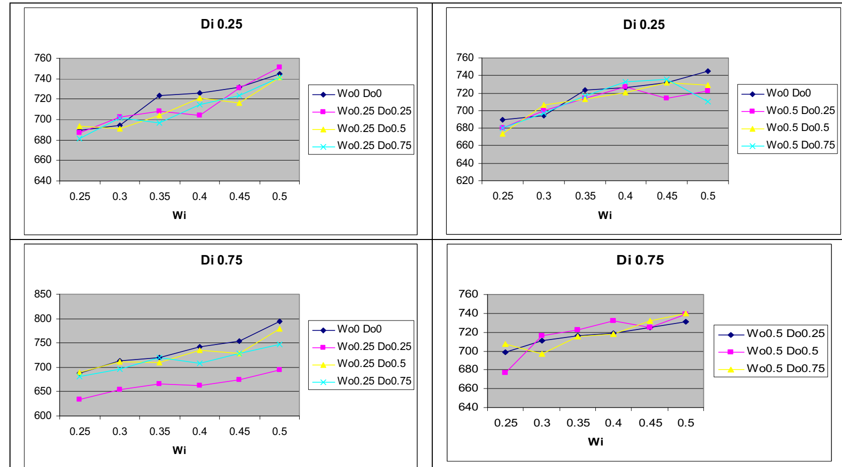

Figure 4. Variation of the size of the inner serif (Wi), for the 0.25 and 0.75 overlaps (Di), for each of the smallest and largest outer serifs (Wo).

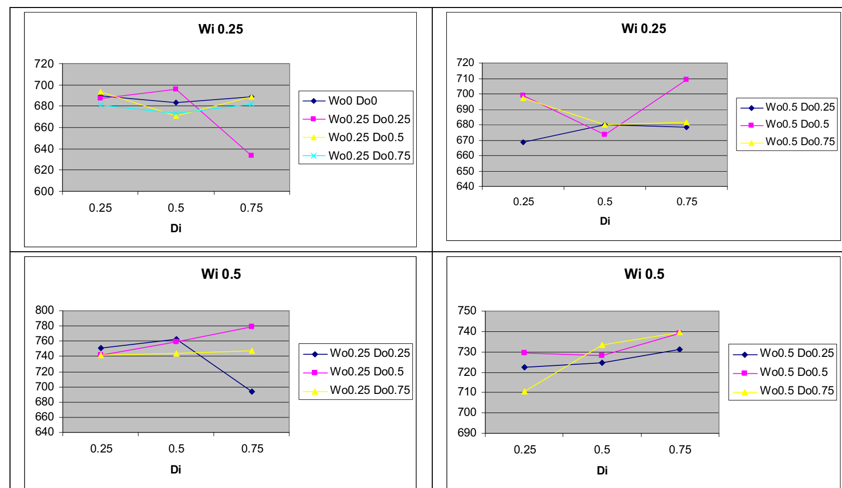

Figure 5. Varying the overlap of the inner serif (Di) for the smallest (0.25) and largest (0.5) inner serifs (Wi), for each of the smallest and largest outer serifs (Wo).

Figure A.4: *Reprint of paper presented at the SPIE Photomask Technology 2009, page 4.*

3.2. Variation of OPC on the outer corner

Figure 6 shows the variation of the size of the outer serif (Wo), for the smallest (Do=0.25) and largest (Do=0.75) overlaps, for each of the smallest and largest inner serifs (Wi). No clear relationship can be observed.

Figure 7 shows variation of the position/overlap of the outer serif (Do) for the smallest (0.25) and largest (0.5) outer serifs (Wo) for each of the smallest and largest inner serifs (Wi). Once again no dependence can be seen.

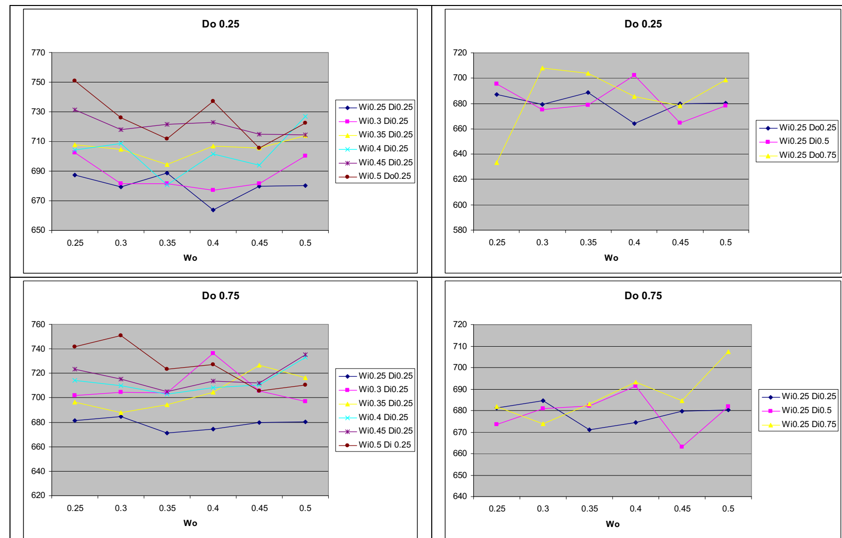

Figure 6. Variation of the size of the outer serif (Wo) for the smallest and largest overlaps (Do) for each of the smallest and largest inner serifs (Wi).

Figure A.5: *Reprint of paper presented at the SPIE Photomask Technology 2009, page 5.*

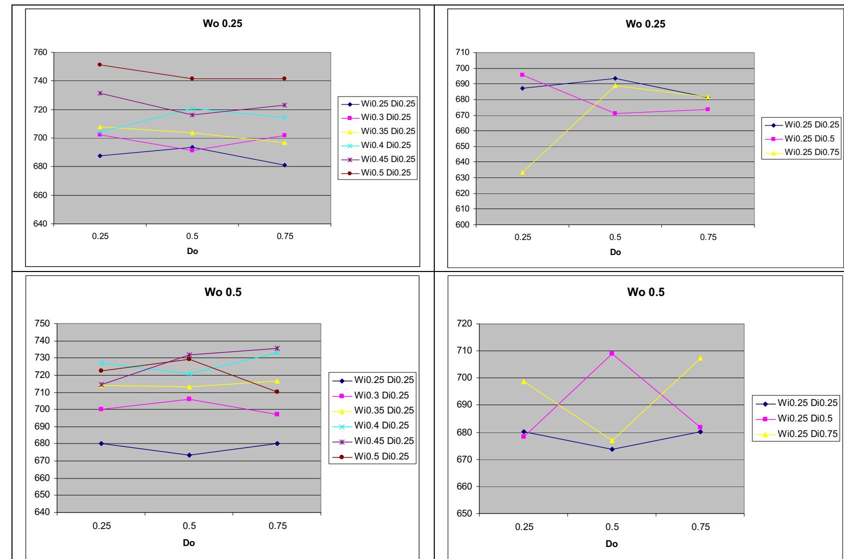

Figure 7. Variation of the size of the overlap of the outer serif (Do), also referred to as its position, for the smallest (0.25) and largest (0.5) outer serifs (Wo) for each of the smallest and largest inner serifs (Wi).

4. DISCUSSION

The graphs above show that the inner serif has a far greater effect upon the overall electrical resistance of the poly lines. Enlarging the size of the inner serif, i.e. reducing the amount of conducting material in the inner corner, has a clear increasing effect (which is almost linear) upon the resistance of the line for all positions of the serif. If the position of the inner serif is changed, it is only for the largest of these serifs that any relationship can be noted, and the rate of change is more gradual and the effect less pronounced than that resulting from altering the serif size. In contrast, changing the size and position of the outer serif has no clear discernable relationship with the overall resistance of the line being tested.

As a result of this finding some electrical simulations of the structure were run using Raphael interconnect simulation software. Figure 8 shows a simulation of the corner and as can be seen there is a much higher current density in the inner corner of structure than at the outer. This clearly explains why there is much more effect from the inner corner than the outer. An explanation for why the resistance is more sensitive to size of the serif than its position is not entirely clear; however, it is thought that this is likely to be due to the cases studied here where a (relatively speaking) less 'rounded corner' was present when the size of the inner serif was increased rather than when its position was changed. An attempt was made to verify this via SEM inspection using a Philips XL40 SEM and image analysis with ImageJ software, but the SEM resolution was found to be insufficient to accurately test and verify this.

Figure A.6: *Reprint of paper presented at the SPIE Photomask Technology 2009, page 6.*

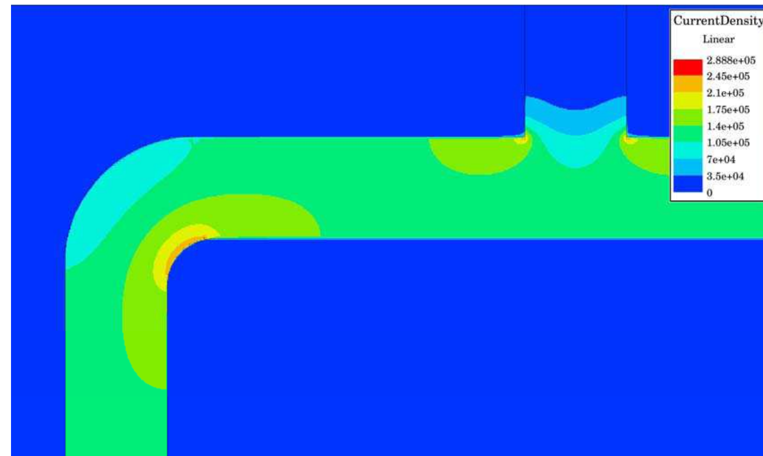

Figure 8. Simulation using Raphael showing the high current density at the corner where the inner serif is located and the lack of current at the outer corner.

5. CONCLUSION

This work attempted to investigate the accuracy requirements for corner structures using serif type OPC. This study highlighted that in the case of the doped polysilicon lines used, the OPC applied to the outer corner had very little effect upon the electrical characteristics of the circuit feature. However, the OPC applied to the inner corner, and in particular the size of the OPC, had a great effect upon electrical resistance. This initial work was completed at a lithographic k_1 value of 0.5, further work using lower k_1 factors and narrower lines would be useful to verify if the effect is the same, or indeed more critical, as the width of the polysilicon line narrows. It would also be useful to determine if this relationship is maintained when the conducting material is a metal with much lower resistance. This learning would be relevant as technology moves forward into the realm where metal rather than polysilicon transistor gates will be used.

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Figure A.7: *Reprint of paper presented at the SPIE Photomask Technology 2009, page 7.*

Electrical Test Structures for the Characterisation of Optical Proximity Correction

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Abstract

Resistive electrical test structures have been designed to enable the characterisation of optical proximity correction (OPC) applied to a right angled corner in a conducting track. The OPC consists of square serifs which are either added to the outside corner or subtracted from the inner corner. Varying degrees of OPC can be applied by changing the size of the square serif or by changing the amount by which it encroaches on or protrudes from the corner. A prototype test mask has been fabricated which contains test structures suitable for on-mask electrical measurement. The same mask was used to print the test pattern in polysilicon using an i-line lithography tool and results from these structures clearly show that OPC has an impact on the resistance of the final printed features. In particular, the level of corner rounding is dependent upon the dimensions of the serifs employed and the measured resistance can be used to characterise the effects of different levels of OPC applied to the inner corners.

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Figure A.8: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 1.*

Electrical Test Structures for the Characterisation of Optical Proximity Correction

I. Introduction

The work presented in this paper is part of an ongoing project which is focused on developing techniques for the characterisation of advanced photomasks, and photolithographic processes, using electrical test structures. Previous publications have demonstrated that on-mask test structures are capable of fast and repeatable sheet resistance and critical dimension (CD) measurements on binary and alternating aperture phase shifting masks (Alt-PSMs) [1]–[4]. More recently, industry standard optical metrology patterns have been adapted into electrical equivalents for the characterisation binary mask fabrication processes. These have been used to investigate iso-dense proximity effects [5], to characterise the GHOST e-beam proximity correction technique [6] and to compare different metrology methods [7]. In addition, novel test structures have been developed to characterise the dimensional mismatch variation between closely spaced chrome features [8]. Results from masks fabricated using this pattern have revealed previously unseen variations and have isolated one source of systematic mismatch caused by the GHOST process [9].

One of the most common forms of optical proximity correction is the two-dimensional corner serif feature [10]. This is an attempt to make a printed feature more closely resemble the design by adding serifs to outer corners or subtracting them from inner corners as illustrated in Fig. 1.

This style of proximity correction is frequently used in advanced photomask designs and it presents a challenge to conventional metrology techniques [11]. Electrical test structures have been designed which enable the effects of applying serifs to right angled corners to be investigated. Initial results were obtained from a prototype binary mask (MSN6754) and these demonstrated that it is feasible to electrically characterise this method of OPC [12] on mask. Although practically restricted to inner corner serifs, this is not considered a problem, as it is this feature that is most relevant to achieving low resistance in an interconnect. Furthermore, inner corner serif structures are the most difficult to manufacture and characterise using

Figure A.9: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 2.*

conventional optical metrology techniques.

On-mask, corner serif test structures enable the characterisation of the mask making process in terms of the reproduction of the OPC features but, to actually assess their impact on the photolithographic process, measurements at the wafer level are also required. The mask with electrical test structures has been used to print similar structures on-wafer and initial results have been published [13]. This is the first time that a mask including on-mask, electrical test structures has been used to print comparable features for on-wafer, electrical measurement. This paper extends the analysis of the results published in [13] and presents new data on the variation of the resistance of the printed features with respect to the levels of OPC applied.

II. Test Structures and Fabrication

The OPC test structure is a Kelvin connected resistor consisting of a short section of metal track turning through a right angled corner, as shown in Fig. 2(a). To measure the resistance of the track a current is forced between pads B and D and the resulting potential difference is measured at pads A and C. The resistance of the section of track between the voltage taps is then calculated with

$$R = \frac{V_{AC}}{I_{BD}} \tag{1}$$

The effect of OPC is investigated by altering the layout of the right angled corner of the structure. Specifically, a square of metal is added to the outside of the corner while a square is removed from the inside. This is illustrated in Fig. 2(b). The OPC aggressiveness is altered by changing the size of the square (W_i or W_o) and the amount by which it overlaps with, or protrudes from, the original layout (D_i or D_o).

The test mask design has test structures with 3 different base values of CD: 1.6µm, 2.0µm and 2.4µm. These correspond to printed dimensions of 320nm, 400nm and 480nm when imaged with the 5× projection lithography tool used for this work. The dimensions of the OPC elements are defined as fractions of the base CD: 0.25, 0.3, 0.35, 0.4, 0.45 and 0.5. Subsequently, the value of D_i or D_o is then defined as some fraction of W_i or W_o: 0.25, 0.5 or 0.75. The test mask has the full range of OPC dimensions for the 1.6µm (320nm on-wafer) structures and a reduced set for the other CDs with test structures where D_i and D_o are equal to half of W_i and W_o.

In addition to the test structures which are probeable on-mask, the test mask also includes a full set of structures where the probe pads are 5 times larger. This means that the same probe

Figure A.10: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 3.*

card can be used to contact the printed structures as is used for the on-mask measurements. On-wafer test structures were fabricated in a 300nm thick layer of doped polysilicon deposited on a 0.5µm thick layer of thermal silicon dioxide on 200mm silicon substrates. The wafers were spin coated with Ultra-i 123 i-line photoresist and printed using a 5× Nikon i-line step and repeat lithography tool. After development the polysilicon was etched in a reactive ion etch tool before passivation with a 0.5µm thick layer of PECVD silicon oxide. Holes in the oxide were then etched over the probe pads before deposition of a 0.5µm thick layer of sputtered aluminium. The final step was to pattern the aluminium to create contacts suitable for probing. The final structure can be seen in Fig. 3

III. Measurements and Results

A. Electrical Measurements

The results from the on-mask test structures show that the electrical technique is sensitive enough to measure the effects of inner corner structures reliably [12]. In addition there is good agreement between the the on-mask results (Fig. 4) and simulations based on the designed dimensions (Fig. 5). These results are for structures with no outer serif and varied dimensions of inner serif, varying the serif on the outer corner has no significant effect on the resistance for the dimensions used in these test structures.

This strongly suggests that it is the chrome material present on the mask which is being characterised, removing some of the ambiguities inherent when interpreting indirectly acquired images of the mask pattern. Any departures from the simulations have been found to be attributable to defects in the serif structure. This can be seen in Fig. 5 as a measurement point which deviates from the anticipated trend of the curves. It is now hoped that the printed structures and the electrical measurement methods applied so far, will form a valuable tool for investigating the quality of lithographic transfer and for optimising the corner serif structures.

Each die on the wafer printed using the test mask contains a full set of corner serif structures with a nominal linewidth of 320nm. These are arranged in a 19×19 array where each column has a different value of W_i and D_i while each row has a different value of W_o and D_o. Measurements have been made of one complete set of structures using a force current of 500µA. The first row of structures have no serifs on the outer corner and the results are plotted against the inner corner serif dimension in Fig. 6. Similarly, the first column of structures have no serifs on the inner corner and the results can be seen in Fig. 7.

Figure A.11: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 4.*

Fig. 6 suggests an upward trend in resistance as W_i increases, as would be expected. However, the nature of the results suggest that other factors also affect the resistance of the structure. The reason behind this could be related to fabrication artifacts such as non-uniform lithography or etching, which conceal the data trends because the resistance changes are not only due to the OPC features. Another factor that could strongly affect the results is any variability in the localised sheet resistance of the polysilicon layer. This could introduce some of the structure-to-structure variations shown in the resistance results. The effect that the geometry and grain structure has upon the value of resistivity extracted from a Greek cross structure has been reported in [14]. This work identifies that the sheet resistance (R_S) measured using such a structure is a function of the size and distribution of the grains in the conducting material. Furthermore, the effect of the grain structure on the variability of R_S is greater in Greek crosses with very narrow arm widths. Unfortunately, there are no structures such as these on the wafer to confirm whether this is the cause of the variability observed in the measured results. A wafer map of the sheet resistance of the polysilicon layer, measured using a four point probe system on a wafer from the same batch as the test structures, is presented in Fig. 8. Unfortunately, this measurement does not have sufficient resolution to identify local sheet resistance variations that might cause the observed variation in the resistor test structures. It seems likely though that in these narrow polysilicon structures, where the current flow is concentrated around the inner corner, the position of the grain boundaries in the polysilicon, relative to the edges of the patterned structures, will have a significant effect on the variability of the measured resistance.

Fig. 7 confirms that the presence of OPC has little or no effect on the resistance of the conductive track when applied to the outside of the right angled corner. This behaviour is to be expected as most of the current flow in the structure is concentrated around the region of the inner corner, as confirmed by simulations.

More useful results can be obtained by taking the average value of resistance for all the structures in each column of the array. As the size of the outer corner serif is expected to have little effect on the resistance any variation within the column is likely to be due to the variability of the polysilicon resistivity. Fig. 9 plots the average resistance of the 19 test structures in each column against the inner corner serif dimension. The error bars show the standard deviation of the set of 19 results as a measure of the variability of the resistance.

The upward trend in resistance with serif size demonstrates that applying OPC to the inner corner has an effect on the printed structure. However, there is no significant difference

Figure A.12: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 5.*

between different values of D_i, unlike the on-mask results, which is probably related to the OPC structure dimensions approaching the resolution limits of the i-line lithography that was employed. The resistance variation at each point is significant and accounts for the variability observed in the results from a single row of structures shown in Fig. 6. The rate of increase of resistance with W_i observed for each set of data in Fig. 9 is similar to that seen only where $D_i = 0.75 \times W_i$ on mask. This is an interesting result and suggests a proximity effect in the photolithographic process which amplifies the effect of increasing W_i while reducing the effect of changing D_i.

Fig. 10 shows the average value from each row of the array of test structures, which represents a single value of W_o and D_o, plotted against the size of the outer corner serif. There is no obvious trend in the data as should be expected but there is significant variation as shown by the large error bars, which again indicate the standard deviation of resistance for the 19 structures in each row. The larger standard deviation in this case is due more to the effect of changing the inner corner serif rather than variations in the polysilicon resistivity.

B. Scanning Electron Microscope (SEM) Inspection

In order to visually investigate the effects, a Philips XL40 SEM was used to capture images of the structures which were measured electrically. Fig. 11(a) shows a structure with no OPC, while Fig. 11(b) and 11(c) show structures with the most aggressive inner and outer corner serif dimensions respectively. The images suggest that when OPC is applied to the inner or the outer corner of a structure the shape of the corner changes and in particular the level of corner rounding.

To help compare the structures an edge detection filter in the GNU Image Manipulation Program (GIMP) was applied to the images which are subsequently overlaid on one another. Comparisons of the structure with no OPC with the structures with the most aggressive OPC on the inner and outer corners are presented in Fig. 12. These confirm that when OPC is applied the shape of the inner and outer corners changes with respect to a uncorrected corner. Therefore, for inner corners OPC does have an effect and is likely to be the cause of the observed trends in electrical measurement results. On the other hand while OPC does affect the rounding of the outer corner it has no effect on the measured resistance and could be omitted from designs in many cases.

Figure A.13: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 6.*

TABLE I
ANALYSIS OF CORNER ROUNDING ON INNER CORNERS

Serif Size (W_i)	Serif Position (D_i)		
	$0.25 \times W_i$	$0.5 \times W_i$	$0.75 \times W_i$
0 nm	340 nm		
80 nm	330 nm	325 nm	320 nm
160 nm	280 nm	260 nm	240 nm

TABLE II
ANALYSIS OF CORNER ROUNDING ON OUTER CORNERS

Serif Size (W_o)	Serif Position (D_o)		
	$0.25 \times W_o$	$0.5 \times W_o$	$0.75 \times W_o$
0 nm	310 nm		
160 nm	250 nm	230 nm	210 nm

IV. Corner Rounding Simulations

The effects of applying corner serif OPC to these structures can be approximated as a change of the amount of corner rounding. Analysis of the SEM images described in section III-B has enabled the estimation of the radius of curvature of the inner and outer corners affected by the OPC. The results for inner and outer corners are summarised in tables I and II respectively. It should be noted that these are rough estimations of the radius of curvature which have been rounded to the nearest 10nm.

These results can be compared with simulations of the resistance of test structures with various levels of corner rounding applied to the inner or outer corner, which have been performed using the two-dimensional (2D) solver of the interconnect analysis software *Raphael*. A sheet resistance of $97\Omega/\Box$ was chosen for the material of the simulated structures, as this represents a typical value for the polysilicon taken from the four point probe results shown in Fig. 8.

Simulation results for test structures with inner corner rounding are presented in Fig. 13(a), while those for structures with outer corner rounding can be seen in Fig. 13(b). The results of Fig. 13(a) show that there is a significant resistance change with respect to the inner corner rounding. In particular, it appears that the resistance strongly depends on the radius of the

Figure A.14: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 7.*

corner rounding and thus the area of the material added to the structure. This behaviour is to be expected as most of the current flow in the structure is concentrated around the region of the inner corner. However, the change in resistance seen in the fabricated test structures as the corner rounding changes is significantly greater than is suggested when examining Fig. 13(a). For example, changing the corner rounding in the simulated structure from 340nm to 240nm leads to an increase in the resistance of about 20Ω. However, in Fig 9 the resistance increases by as much as 90Ω for structures with similar levels of corner rounding. The reasons for this are unclear but one possibility is non-uniform resistivity in the polysilicon such that the material at the edges of the features are more resistive. As the corner rounding decreases the current flow is more concentrated closer to the edge of the structure where the resistivity may be higher. Another possibility is that the sidewall angle of the etched polysilicon feature is not 90°, which could again lead to larger than expected resistances as the corner rounding is reduced.

The simulation results for outer corner rounding in Fig. 13(b) confirm that there is little variation of resistance when the area of the outer corner changes and this is to be expected as there is minimal current flow in this region of the structure. Any resistance variation caused by altering the dimensions of the radius of the outer corner rounding will be minor compared to other fabrication effects on wafer. This can be seen in the results of Fig. 7 which appear noisy and show no significant trend with respect to dimensions.

CONCLUSIONS

Electrical test structures have been designed to characterise OPC in the form of corner serifs and to investigate the impact they have on printed features at the wafer level. Results from on-mask structures have shown that the electrical measurement technique is sensitive enough to detect the effects of OPC on inner corners and also to identify any abnormalities in the fabricated features. In addition the presence of OPC has little effect on the measured resistance when applied to the outside of the corner structure.

Results of electrical measurements of polysilicon test structures printed using this photomask suggest that OPC applied to the inner corner has a significantly greater effect on the resistance than outer corner serifs. However, there is also significant variability between structures with the same dimensions of inner corner serif, and this is thought to be most likely due to local variations in the resistivity of the polysilicon caused by the grain structure of the material and conduction related edge effects. The size of the inner corner serif (W_i)

Figure A.15: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 8.*

has a significantly greater effect on the resistance of the structure than its position (D_i) which is not the case for the on-mask test structures. This can probably be explained as an artifact of the imaging process and is certainly an interesting result.

SEM imaging of the test structure geometries confirms that OPC does alter the shape of corner rounding on both the inner and outer corners. It is clear from this result that the inner corner OPC has a significant effect on the resistance of the printed structure, while outer corner OPC has little or no effect. Analysis of the SEM images has allowed the estimation of the radius of the rounded corners for structures with and without OPC applied. Simulations of test structures with similar levels of inner corner rounding do not show the same change in resistance as is observed in the measured structures. This could be due to non-uniform sheet resistance in the fabricated structures, which gives a larger increase in resistance than is predicted by simulation as the inner corners become less rounded. Simulations of rounding on the outer corner show little variation in resistance, which is as expected.

If the only concern in applying OPC to the corners of features like these was the resistance of the resulting printed structure then these results would suggest that there is no return for the extra time and expense involved in preparing the corrected design. However, there are other reasons for performing proximity correction, for example to make sure that printed structures meet design rules for interlayer overlay or for capacitance. These structures have certainly shown their capability to enable the characterisation of certain OPC features at both mask and wafer level. This is the first time that on-mask electrical test structures have been used to print features with an i-line lithography system so that electrical measurements can also be made on-wafer. The next step is to take this forward employ more advanced photolithography for the production of features with dimensions closer to the state of the art. OPC, and other resolution enhancement techniques, are even more essential at those dimensions and the ability to characterise both masks and the printed features becomes ever more important for good process control and development.

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Figure A.16: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 9.*

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Figure A.17: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 10.*

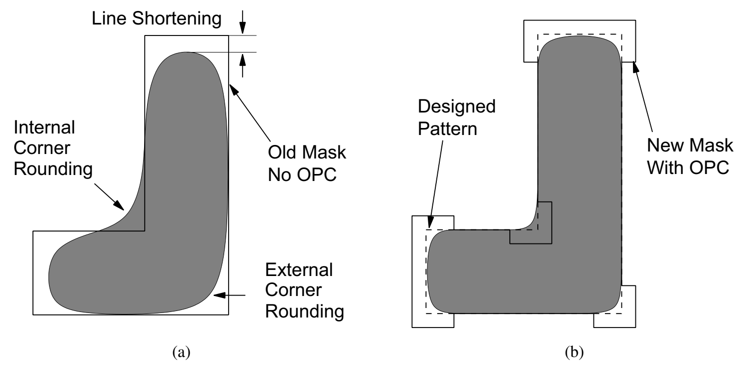


Fig. 1. (a) Schematic showing mask layout without OPC and the resulting printed feature with corner rounding and line shortening. (b) Layout with OPC applied which more closely fits the designed pattern (dashed line)

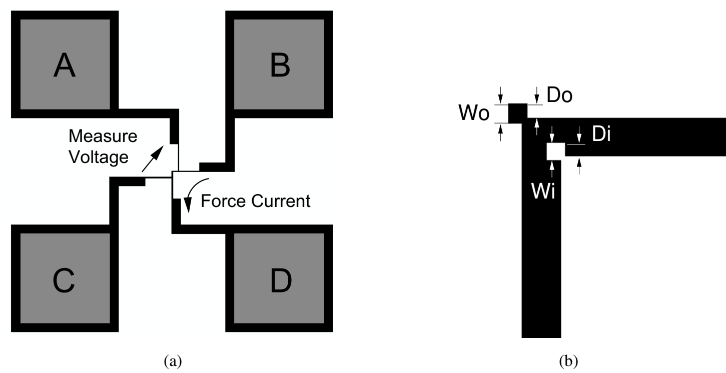


Fig. 2. (a) Layout of Kelvin connected OPC test structure showing electrical measurement scheme. (b) Expanded view of central part of the test structure showing the parameters of the OPC features.

Figure A.18: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 11.*

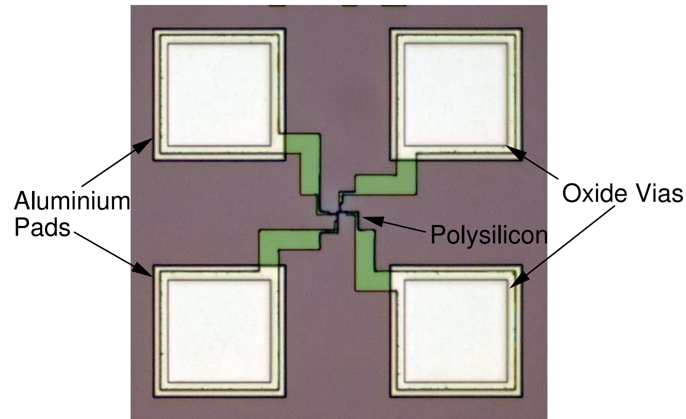


Fig. 3. Photomicrograph of an OPC test structure fabricated in polysilicon

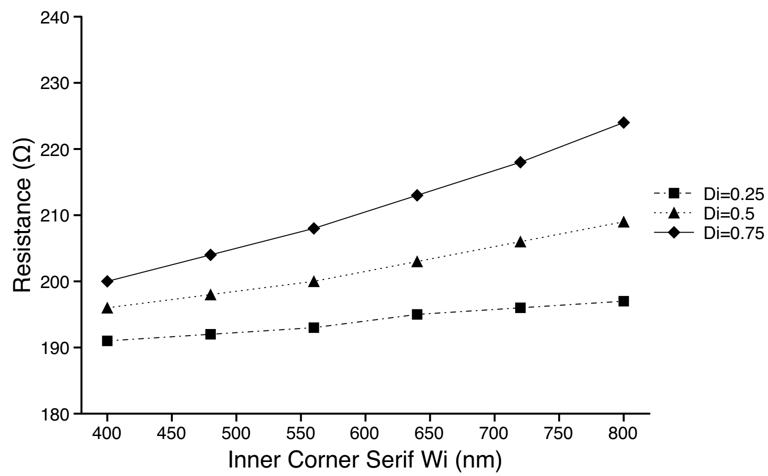


Fig. 4. On-mask resistance simulations from structures with inner corner OPC features.

Figure A.19: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 12.*

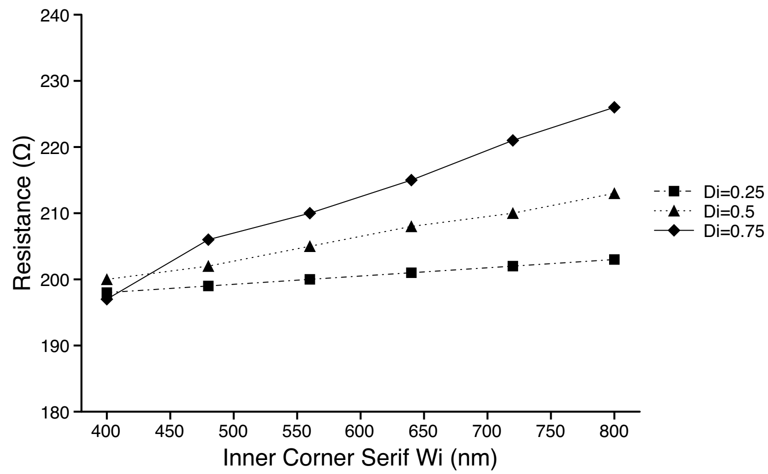


Fig. 5. On-mask electrical measurement results from structures with inner corner OPC features.

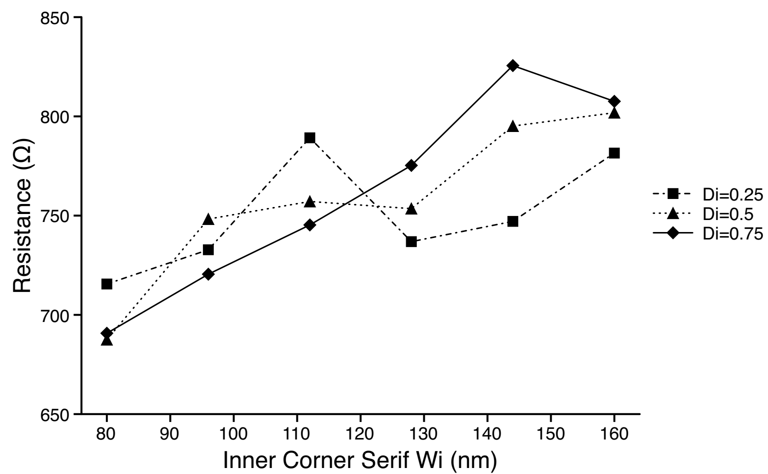


Fig. 6. On-wafer electrical measurements of structures with inner corner OPC features.

Figure A.20: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 13.*

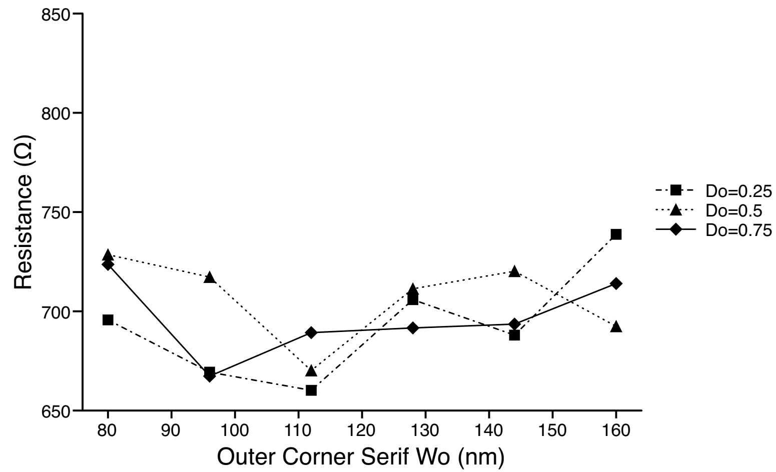


Fig. 7. On-wafer electrical measurements of structures with outer corner OPC features.

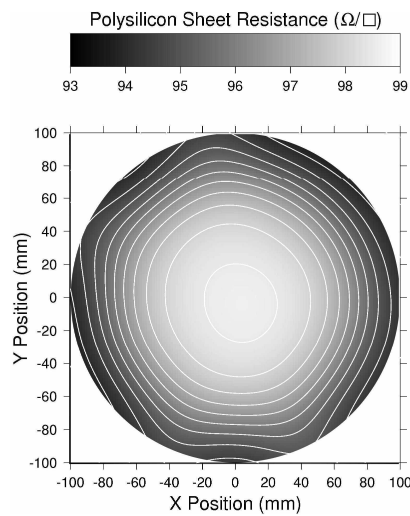


Fig. 8. Sheet resistance variation across one wafer with corner OPC electrical test structures.

Figure A.21: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 14.*

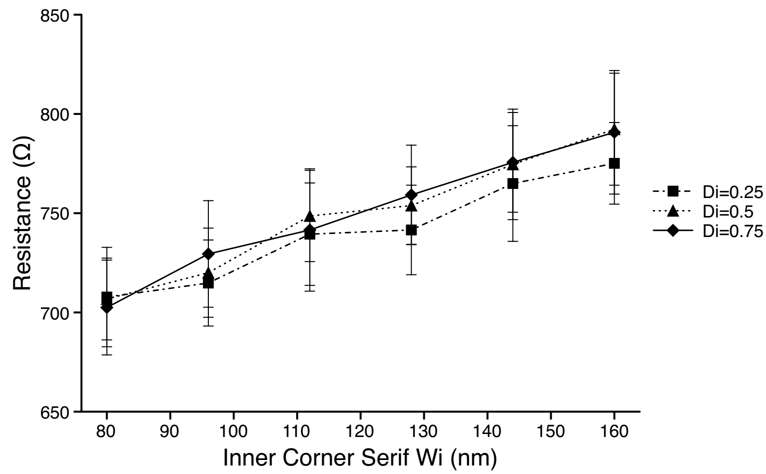


Fig. 9. Average measured resistance versus inner corner serif dimensions

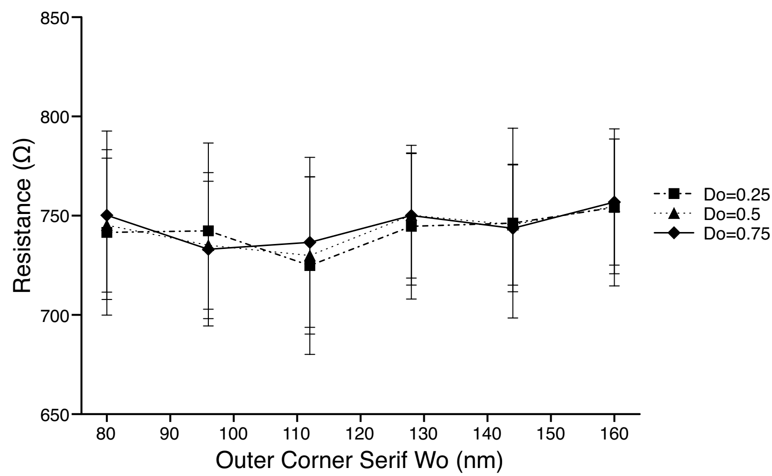
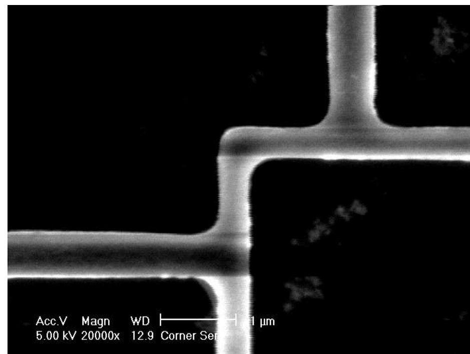
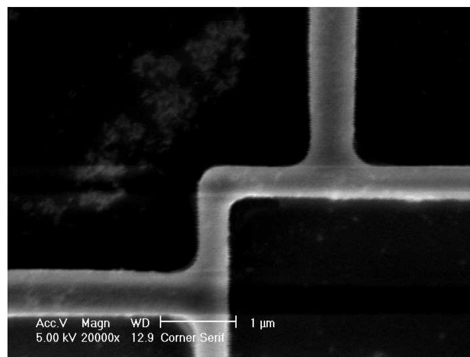


Fig. 10. Average measured resistance versus outer corner serif dimensions

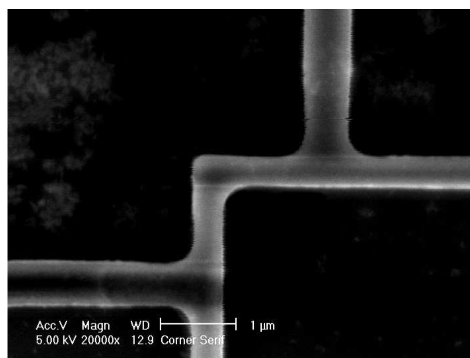
Figure A.22: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 15.*



(a)



(b)



(c)

Fig. 11. SEM images of structures with different OPC arrangements: (a) No OPC; (b) Maximum inner corner OPC; (c) Maximum outer corner OPC.

Figure A.23: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 16.*

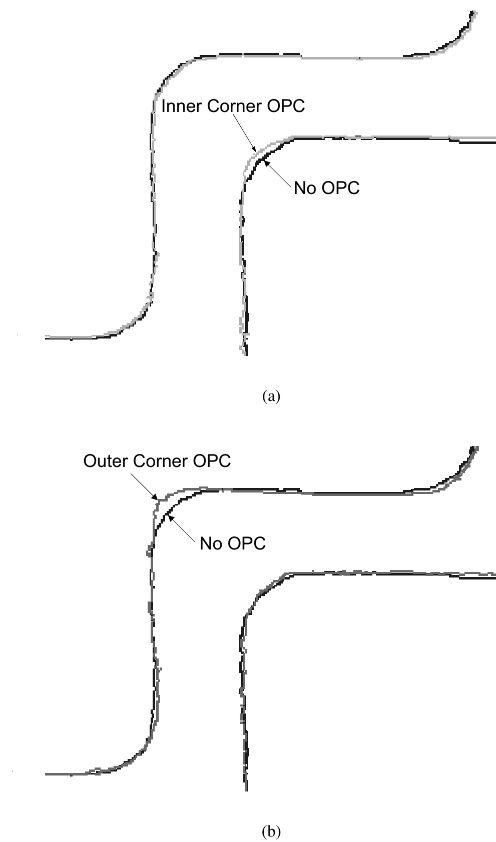
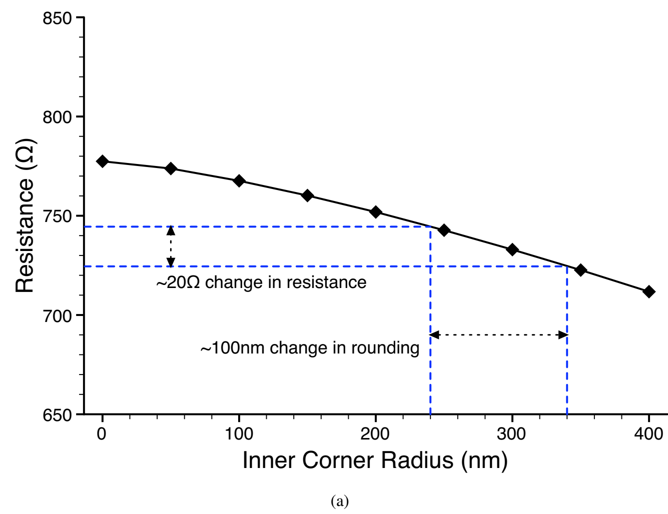
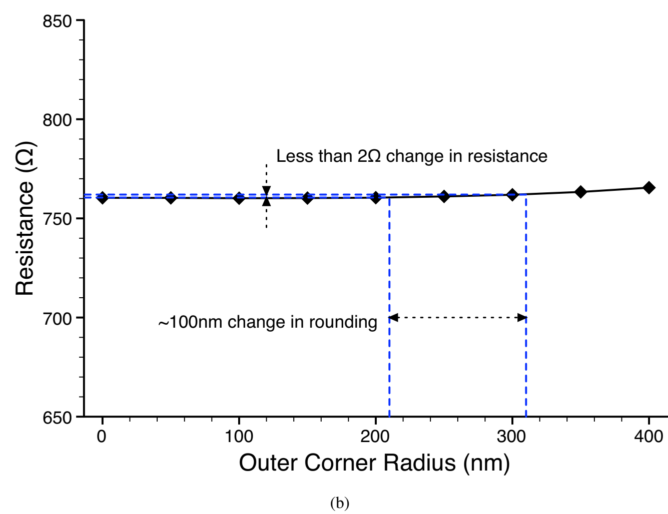


Fig. 12. Overlaid shapes of structures with different OPC arrangements: (a) Inner corner OPC; (b) Outer corner OPC.

Figure A.24: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 17.*



(a)



(b)

Fig. 13. Simulation results for polysilicon test structures with varying levels of corner rounding applied to (a) the inner corner or (b) the outer corner.

Figure A.25: *Reprint of paper submitted for publication to the IEEE Transactions on Semiconductor Manufacturing, page 18.*

Kelvin Resistor Structures for the Investigation of Corner Serif Proximity Correction

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†Nikon Precision Europe,
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Abstract

Electrical test structures for the characterisation of Optical Proximity Correction (OPC) have been fabricated using i-line lithography in aluminium film patterned with a reactive ion etch process. Initial electrical measurements are presented which show an increase in the resistance of a right angled section of Al track as the level of OPC on the inside corner is increased. Structures with OPC applied to the outer corner do not show the same change in resistance. SEM images of similar Al test structures clearly show the effects of applying OPC and suggest that inner corner serif OPC leads to a narrowing of the conducting track.

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Submitted for Oral Presentation

Figure A.26: *Reprint of four page abstract to be submitted to the IEEE International Conference on Microelectronics Test Structures 2010, page 1.*

I. Introduction

Optical Proximity Correction is a method of resolution enhancement in microlithography where a sub-resolution pattern is added to the mask design. As today's OPC becomes ever more complex it requires the use of smaller and smaller feature sizes and ever more expensive processing to produce the patterns on the photomasks. This also impacts on data preparation for designs and adds to the already high costs for masks used in advanced semiconductor processes. The present work is a continuation of an investigation into the application of OPC through the use of resistive electrical test structures. It is specifically concerned with determining the need for aggressive OPC in interconnect patterning where it may be that the circuit performance could be adversely affected by attempting to replicate the ideal drawn design rather than simply producing a functional pattern. This study has grown out of an ongoing collaboration concerned with test structures for the characterisation of advanced photomasks [1], [2]. The test structures were originally measured on-mask [3] where the reproduction of the OPC pattern could be determined through electrical probing. Subsequently the test structures were printed in doped polysilicon using i-line reduction lithography [4], [5]. This identified issues with the variability of the measurements and the present work investigates if this can be addressed by printing the same structures in a thin layer of aluminium. The rationale behind this was that there would be less variability resulting from the grain structure, and from short range variation of resistivity, in a more conductive metal film. This paper presents the initial results from these aluminium test structures.

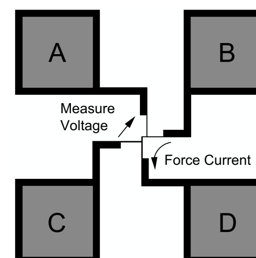


Fig. 1. Schematic layout of Kelvin connected corner structure

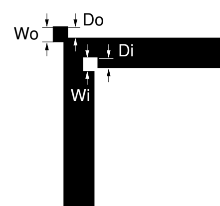


Fig. 2. Closeup of the corner showing the variables associated with OPC serifs

II. Test Structures

The basic test structure used in this study is a right angled, Kelvin connected, section of conducting track as shown in figure 1. The test chip design consists of an array of these structures which have varying levels of OPC applied to the inner and outer corners by adding or subtracting squares of different dimensions, as shown in figure 2. There are two variables which determine the level of OPC, the size of the serif (Wi or Wo) and the amount by which it encroaches on or protrudes from the corner of the structure (Di or Do). Obviously the "i" refers to the inner corner and "o" to the outer. In each case the serif size, Wi or Wo, is defined as a fraction of the nominal feature size ranging between 0.25 and 0.5. Similarly, the position, Di or Do, is some fraction of the serif size, either 0.25, 0.5 or 0.75.

The test chip design includes two sets of test structures, one set which is designed to be electrically measured by probing the photomask directly as described in [3]. The other set of structures has probe pads which are 5 times larger than the on-mask structures so they can be successfully probed on-wafer when printed with a 5X step-and-repeat lithography tool. The nominal on-mask feature size is 1.6μm meaning that the printed dimension is 320nm. Initial results from test structures printed using the test mask to pattern doped polysilicon were presented in [4] and [5]. These showed significant short range variability in the resistivity of the polysilicon and it was suggested that this was due to the grain structure of the material. In order to investigate this affect further the structures were printed in a thin layer of aluminium in the expectation that this would improve their performance.

III. Processing

The test structures were fabricated on 200mm (8") silicon wafers coated with a 0.5μm layer of thermal silicon dioxide. A 300nm thick layer of aluminium was deposited on the device side using a Plasmalab 400 sputter coating system from Oxford Plasma Technology. The wafers were then spin coated with a 900nm layer of Ultra 123i i-line photoresist from Rohm and Haas and soft baked. The wafers were printed using a Nikon NSR-2005i9C step-and-repeat tool with an NA of 0.50. One major advantage of printing the structures directly into aluminium was that no subsequent lithography steps were required to make probeable metal pads as was the case with the polysilicon structures. The photoresist was developed using a standard process and the aluminium was then etched using an STS Multiplex reactive ion etch tool with a $SiCl_4$ and Ar plasma. After the resist was removed in an oxygen plasma barrel asher the test structures were ready to be measured electrically. Figure 3 shows one of the printed test structures.

Figure A.27: *Reprint of four page abstract to be submitted to the IEEE International Conference on Microelectronics Test Structures 2010, page 2.*

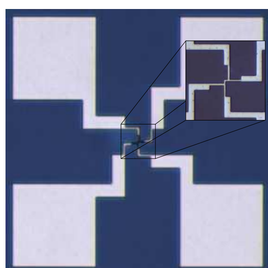


Fig. 3. Microscope image of an aluminium OPC test structure with inset showing magnification of the centre of the structure

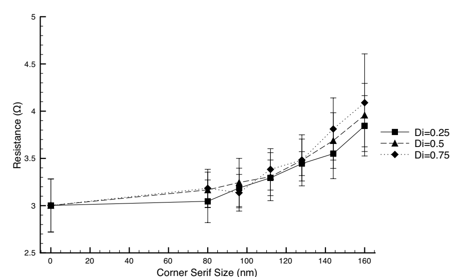


Fig. 4. Resistance measurement results for inner corner OPC

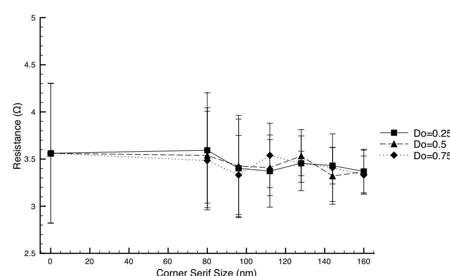


Fig. 5. Resistance measurement results for outer corner OPC

IV. Measurements and Results

A. Electrical Measurements

The on-wafer electrical measurements were made using a SÜSS MicroTec PA200 semi-automatic prober controlled by an HP-UX workstation with an HP4062UX semiconductor parameter analysis system. Current was forced between pads B and D (see figure 1) using an HP4142B DC source/monitor unit and the resulting voltage between pads A and C measured with an HP3457A digital multimeter. In order to determine the optimal current for these measurements one structure was subjected to a range of force currents between 10µA and 10mA. The measurement was made 10 times at each voltage and the average and standard deviation calculated. The lowest value of measurement variability occurs at the highest current used (10mA) but the average resistance at this point is slightly higher than for a current of 5mA. This suggests Joule heating with a potential to damage the structure and so all of the subsequent measurements were made at the lower force current of 5mA. At this current level the standard deviation of 10 measurements is around 0.1% of the average measured resistance.

A complete set of test structures consists of a 19×19 array where each column contains structures with a defined value of Wi and Di while each row contains those with a particular combination of Wo and Do. In addition the first row has structures without any OPC on the outer corner and the first column has structures without any OPC applied to the inner corner. Figures 4 and 5 show the results of measuring the full set of structures plotted against the inner and outer corner dimensions respectively. Each point in the graph represents the average from one complete column of structures for inner corner OPC and one complete row for outer corner OPC. The error bars show the standard deviation of the resistances measured for each row or column.

The results for the inner corner OPC show a definite increase in resistance as the size of the serif on the mask increases. However, unlike the results from the on-mask measurements previously presented in [3] there is no significant dependence on the position (Di). There is significant variability around each average value which was expected to be reduced when compared to the polysilicon structures. Further investigation is required to determine the source of this variability. The results for the outer corner OPC do show some reduction in resistance with increasing serif size but this is not significant compared to the variation for each value of Wo. This is expected from previous results as the current flow during the measurement is concentrated around the inner corner.

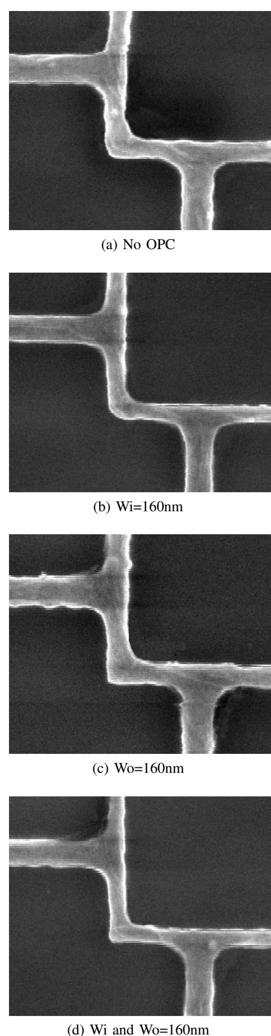
B. SEM Measurements

Scanning Electron Microscope (SEM) imaging was performed on a selection of aluminium test structures and the results are presented in figure 6.

The effects of applying OPC to the inner and outer corners is clear from these images. The outer corner becomes much less rounded and more square while the effect of inner corner OPC has a less obvious effect on the rounding of the corner. In fact, it actually appears to make the line significantly narrower around the right angled bend. This could explain the significant (between 15 and 20%) increase in resistance between the structures with no OPC on the inner corners and those with the largest values of Wi and Di.

In previous papers [4], [5] SEM images of polysilicon structures were used to estimate the radius of curvature of the corners affected by the applied OPC. These values were then used in simulations of test structures with similar dimensions.

Figure A.28: *Reprint of four page abstract to be submitted to the IEEE International Conference on Microelectronics Test Structures 2010, page 3.*



(a) No OPC

(b) Wi=160nm

(c) Wo=160nm

(d) Wi and Wo=160nm

Fig. 6. SEM images of OPC test structures

The results suggested that the change in resistance observed in the printed structures, as the inner corner rounding was reduced by more aggressive OPC, was greater than would be expected from the simulations. For example, the simulations would predict a change in resistance of no more than 3% for the same change in corner rounding that is observed between figures 6(a) and (b). It seems likely that there is a further effect of applying OPC to the inner corner which narrows the line significantly and causes the observed change in resistance.

The SEM images also reveal significant line edge roughness in these structures which may be the source of the variability between test structures that is represented by the error bars in figure 4.

V. Conclusions and Future Work

Corner serif test structures for the measurement of OPC have been successfully fabricated in a thin aluminium layer which is suitable for direct electrical probing. The results show a significant increase in resistance as more aggressive correction is applied to the inside of a right angled corner while applying OPC to an outside corner has little effect. The measurements also demonstrate significant variability in the resistance between structures which should be very similar, such as in structures where it is only the OPC on the outer corner that is changing. This was expected to be improved when compared with the polysilicon structures investigated previously. The reason for the variability may be revealed by SEM images which show significant line edge roughness but further investigation is required. The same SEM images clearly show the effects of applying OPC to the inner and outer corners and may explain some discrepancies between electrical and simulation results that were previously presented. Further electrical measurements will be made in order to present results from a full 200mm wafer. These will provide an increased data set for the determination of the variability of the measurement and the relevance of the observed changes in resistance with OPC.

Acknowledgements

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