Improving the phase modulating properties of electrically addressed Liquid Crystal on Silicon Devices

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Submitted for the degree of PhD.

School of Engineering & Electronics
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2004

Acknowledgements

First, I would like to thank my parents Kun-tae and Jung-suk, and parents-in-law Keun-sik and Han-soon for their support and encouragement. I thank my wife Mi-ran, for her patience and encouragement. I also thank my daughter Yun-a and my son Jong-hun, for being together and keeping me active.

I would like to thank my supervisor Dr. Ian Underwood for suggesting the project, and for his guidance support, and encouragement during the course of the work. I would also like to thank Dr. Will Hossack for his practical advice and expertise shared during several helpful discussions. Thanks to Dr. Georg Bodammer, Dr. James Gourlay and Mr. Christophe Miremont for their enthusiastic advice and assistance while working in the microfablication laboratory.

Support from the technical staff, in particular Dr. William Parkes, Mr. Andrew Garrie, and Mr. Alec Ruthven is also appreciated. I also thank Mr. A. M. Gundlach and Dr. J. T. M. Stevenson for their support in making the backplane sample devices. I also would like to thank Dr Dwayne Burns of Microemissive Displays Ltd for technical assistance of the LCoS backplane driving circuit designing and Dr. Kevin Heggarty of the ENST Bretagne for his helpful comments in the diffraction grating.

Finally, I would like to thank Edinburgh University for funding the research project.

Declaration

I declare that this thesis was composed by myself and that the work contained therein is my own, except where otherwise acknowledged.

September 2004

Abstract

The objective of the work described in this thesis was to improve the optical phase modulating properties of liquid crystal on silicon (LCoS) devices for non-display applications. This thesis presents the characterization of oxide two deposition processes, modelling of binary phase modulation in ferroelectric liquid crystal SLMs using electronic equivalent circuit, and characterization of multi-phase modulation in nematic liquid crystal with pulse-width drive scheme.

For optimal optical performance of a phase modulating LCoS device, the degree of surface planarisation of the CMOS backplane must be superior to that of conventional CMOS. Two oxide-deposition processes have been characterized to evaluate their effectiveness in planarising microdisplay backplanes. In order to investigate the trench-filling capabilities of the respective oxide deposition processes, I prepared test samples that had a set of trench patterns (1 - 6μm wide) etched into 4μm-thick thermal oxide on a Si-substrate. I found that the trench filling capability of an electron cyclotron resonance chemical vapor deposition (ECR CVD) process is superior to that of a pyrolytic CVD process. I investigated the effects of ECR CVD deposition parameters on trench-filling properties and demonstrated the ability to produce deposited oxide layers which fill high aspect ratio trenches without producing voids.

Modelling of binary phase modulation is required for optimal performance of ferroelectric liquid crystals (FLC) on silicon SLMs when used in coherent optical systems. This thesis presents a modelling technique by which an HSpice model can be used for characterization of phase modulation properties for designing FLC-on-silicon SLMs. The simulation and experimental measurements of phase modulation are described. For the theoretical model simulation, FLC parameter measurements are described. I experimentally verified the modeled prediction of phase modulation by investigating reflective FLC test cells. I have shown agreement within 9 % between the measured and simulated values of phase modulation.

In phase modulating diffractive optical devices multi-phase modulation provides improved performance over binary modulation. Multi-phase modulation can be achieved by using nematic liquid crystal spatial light modulators (NLCSLM) with pulse-width modulation driven from a binary CMOS backplane. This thesis presents the characteristics and the driving scheme of the 512×512 Si-backplane SLM for the implementation of the multi-phase modulation while comparing the binary and four-level phase holograms. A diffraction efficiency of 39.7% for binary grating and 72.7% for four-level blazed grating were obtained at a spatial frequency of 0.78 lines per mm.

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Chapter 1: Introduction

1.1 Background

Since the 1980's a great deal of research activity has centered around the development of optical systems for information processing [165]. In many such systems spatial light modulators (SLMs) are key components for performing optical data or image processing. SLMs are devices capable of applying a spatially controlled modulation to an incident wavefront. One hybrid SLM technology combines a modulating liquid crystal layer with a CMOS-silicon active-matrix backplane. Many different SLMs have been developed since the first such SLM was conceived at the University of Edinburgh in 1983 [164]. From the late 1980's onwards, it has been recognized that many liquid crystal SLMs can also be configured as miniature displays. Today the technology is called Liquid Crystal on Silicon (LCoS) and the resulting displays are called microdisplays.

In a microdisplay backplane, a highly planarised and smooth surface is very important in determining the device's optical modulation capability. However, trenches in the backplane that are located between pixels, to provide electrical isolation between adjacent pixel pads, present a challenge to the backplane planarisation process. In order to construct the pixel pads as high efficiency mirrors with high fill factor, a planarisation process is required to flatten the dielectric layer that covers the underlying circuitry and upon which the metal for the pad is subsequently deposited and patterned. The degree of flatness necessary from the planarisation process is more stringent than that from the typical insulator Chemical-Mechanical-Polishing (CMP) step in a conventional CMOS process, because a highly reflective optical surface is required with large aperture-ratio pixels. Aperture ratio is the ratio of area between the actual size area of a sub-pixel and the area of

that sub-pixel that can reflect light. After oxide deposition, the oxide film is polished back in the CMP process, leaving a 0.5 - 1μm-thick layer above the uppermost CMOS metal layer. If voids in the oxide are located at a higher position than the top CMOS metal layer before the polishing process, there is the likelihood of exposing the voids during the CMP process. The voids in the oxide cause not only a reliability problem, with the possibility of trapped chemicals in the void, but can also cause breaks or shorting in bus lines in the underlying CMOS metal layer. Several deposition / CMP cycles are often required in order to fill the voids; this prolongs, complicates, and adds to the cost of the overall planarization process. In order to reduce processing time and effort while still achieving extremely smooth surfaces, a most suitable deposition technique must be identified.

Secondly, phase modulation is used for many non-display applications of liquid crystal displays such as optical correlators, optical interconnects, neural networks and adaptive optics. Various SLMs have been developed for these applications, of which ferroelectric liquid crystal on-silicon (FLCoS) SLMs are used for binary phase modulation. To achieve better optical performance, a study has been carried out to model phase modulation assisting the characterization of FLCoS SLMs.

Ferroelectric liquid crystals are birefringent and act like a waveplate, interacting with the polarisation of the light passing through it. If FLC material is constrained in a thin layer that is less than the FLC helical pitch, as the chiral rotation is unwound by the thin layers, the FLC directors' optical axis can move from one bistable state to another state by application of an electric field. This makes the FLC cell a uniaxial phase plate with a switchable optical axis. In this configuration, the device is a surface stabilized ferroelectric liquid crystal (SSFLC) device. SSFLC devices are well suited to binary phase modulation because of this binary switching property with fast switching speed. Important aspects of the interaction between the FLC molecules and coherent polarized light can be modeled by using an electronic circuit model. Using the model of an FLC cell we can predict how phase modulation varies with the FLC parameters.

An electronic equivalent circuit has been developed that models the binary phase modulating properties of a SSFLC cell. The model is used to optimize the design of an FLCoS device by simulating its behavior, and implementing it in HSpice. The model requires experimental measurements for rotational viscosity, chevron tilt angle and restoring torque of the FLC material, since the values of these parameters depend on cell construction.

Finally, the combination of a modulating liquid crystal layer with a CMOS-silicon backplane has resulted in a key component in coherent optical applications. CMOS-silicon active-matrix backplanes provide small geometry, high mobility, reflective mode operation and system-on-chip capability. Binary CMOS backplane devices typically contain an array of 1-bit digital memory cells and provide binary modulation of light. Analogue CMOS backplane devices need analogue switches and storage transistors that accumulate the charge representing each pixel value on its gate. Due to the complexity of the design, resolution of analogue CMOS backplanes is limited and fabrication cost is high compared to binary CMOS backplanes.

The use of binary phase levels restricts the diffraction efficiency of computer-generated holograms (CGHs) because the binary phase profile directs more light energy into the unwanted orders. Multi-level phase modulation increases diffraction efficiency, and eliminates the intrinsic inversion symmetry in the Fourier plane. Thus, multi-level phase modulation is highly desirable and has to be characterized for those optical applications. Various multi-level phase modulators have been reported. Cascaded FLC SLMs have been proposed to produce multi-phase levels based on cascading binary phase modulators [131][132]. However, the cascaded SLMs are too complex to optically align, and too bulky to be used in an optical system. Nematic liquid crystal (NLC) SLMs are also capable of multi-phase modulation by controlling their voltage level [162][163], but using this approach it is difficult to manage precise phase modulation. Moreover, for this application the Si-backplane circuitry must be analogue making it more complicated than digital circuitry. Therefore, I introduce multi-phase modulation with NLC SLMs driven from a binary CMOS backplane.

1.2 Objectives

The objective of this project is to improve the optical phase modulating properties of LC-over-silicon devices for non-display applications by considering, a) oxide deposition processes, b) modelling of ferroelectric liquid crystal with equivalent electronic circuit and c) characterization of multi-phase levels in nematic liquid crystals with pulse width modulation. To accomplish this, the following objectives were met:

1. Compare the trench-filling capability of electron cyclotron resonance (ECR) chemical vapor deposition (CVD) and pyrolytic CVD techniques, investigate the parameter dependent trench-filling properties of oxide deposited with an ECR CVD technique on a backplane, and report an effective deposition technique for void-free oxide deposition on microdisplay backplanes.

2. Characterize an electronic equivalent circuit which describes the binary phase modulating properties of a SSFLC cell, and evaluate the performance of the circuit model by measuring experimental values of phase modulation from constructed FLC cells; to optimize an FLC-on silicon device by simulating its behavior, and implementing it in HSpice.

3. Develop a pulse-width modulation scheme to drive binary CMOS backplane and characterize multi-level phase modulation with a NLC SLM driven from a binary CMOS backplane.

1.3 Thesis outline

Chapter 2 reviews optical phase modulating properties for reflective LC-SLMs. The major SLM technologies and their applications will be discussed. Issues in using LCoS devices as phase modulating SLMs will be described. LCoS devices use the electro-optic effects of liquid crystals. Hence it is necessary to review how LCoS devices interact with light by describing the properties of polarized light, retardation

plates and mirror reflection. This chapter also compares how phase modulation and amplitude modulation work in SLMs.

Chapter 3 provides the basics of liquid crystals for LCoS devices with nematic and ferroelectric materials, and describes their electro-optical properties. Liquid crystal phases will be described. This section also describes how the dielectric anisotropy of a liquid crystal interacts with an electric field and how the optical anisotropy of a liquid crystal interacts with the optical field. Nematic cells are divided into untwisted mode and twisted mode. Electro-optical effects in those two modes will be discussed. There are many different types of ferroelectric LCs such as surface stabilized FLCs, deformed helix FLCs, soft mode FLCs and antiferroelectric LCs. Electro-optical effects in each different FLC mode will be discussed. Surface stabilized FLCs are suitable for binary phase modulation. The details of surface stabilized FLCs will be discussed including the cell geometry (chevron structure) and switching properties. Liquid crystal alignment is essential to the optical performance of a SLM. Advantages and disadvantages of several alignment techniques are discussed.

In chapter 4 oxide-deposition processes will be characterized to evaluate their effectiveness in planarising LCoS backplanes. A pyrolytic CVD system and an ECR CVD system are used to investigate trench-filling properties with SiO_2. The trench-filling capability of pyrolytic CVD and ECR CVD are compared. To investigate the trench-filling capabilities of the CVD processes, construction of test samples will be discussed and major parameters of the CVD processes will be discussed. The effects of ECR CVD parameters on the trench-filling properties will be investigated, and an improved deposition technique for void-free oxide deposition will be reported.

Chapter 5 presents a modelling technique by which an HSpice model can be provided for characterization of phase modulation properties for designing FLC-on-silicon SLMs. The principle of phase modulation will be introduced using Jones matrices. This chapter also describes how to construct a reflective SSFLC cell as a half wave plate. Appraisal techniques for the constructed FLC cell will be described including measurement of spontaneous polarisation current, switching speed,

bistability, and contrast ratio. Then this section describes the phase modulation measurement technique for a reflective cell based on a Fizeau interferometer. By introducing an electronic equivalent circuit, the rotation of FLC directors can be modeled with time and applied voltage. Some of the model parameters, such as chevron tilt angle, restoring torque and rotational viscosity, require direct measurements from test cells. The measurement techniques of those parameters will be described. To evaluate the model performance, phase modulation comparisons will be made between the experimental and simulated results.

In chapter 6, I describe how multiple phase modulation is achieved by using nematic liquid crystals with pulse-width modulation driven from a binary CMOS backplane. This chapter describes the development of a pulse width modulation (PWM) driving scheme to control the multiple phase of the nematic liquid crystals. The performance of multi-phase modulation is evaluated by measuring diffraction efficiencies. The basic principle of pulse-width modulation will be introduced and the phase-shift properties in NLC as a function of duty ratio will be characterized. The architecture of a CMOS backplane with 512^2 pixels and addressing circuitry specifications will be described. The 512LCoS interface board will be described which is a key part for driving the 512 by 512 array of backplane. Design of the PWM-driving scheme will be described with the detailed timing diagram of the driving scheme. The performance of multi-phase modulation will be evaluated in comparison with binary phase modulation. Diffraction-efficiency measurements and computer-generated holograms, which replay 4 by 4 spots, will be introduced for the performance evaluation.

Finally, chapter 7 concludes this thesis by reviewing the chapters 4-6 briefly, and discusses possible future work.

Chapter 2:
Spatial light modulators and phase modulation

2.1 Introduction

This chapter reviews the optical phase modulating properties of reflective liquid crystal spatial light modulators. The basic working principle of spatial light modulators and their applications are described. The major spatial light modulator technologies are reviewed including liquid crystal on silicon (LCoS) devices. A comparison with alternative technologies is presented in order to understand advantages and disadvantages in using liquid-crystal based devices. Finally, the principle of phase modulation and issues in using LCoS devices as phase modulators is discussed.

2.2 Spatial light modulators

Spatial light modulators (SLMs) are fundamental to the fields of optical computing, optical signal processing, and flat panel displays. SLMs are devices that spatially modulate an optical wave, so that they have an ability to imprint information onto an optical wavefront. Depending on the function of spatial coordinates and time, the modulation types can be divided into the amplitude, phase, polarization and spatial frequency. Currently, amplitude and phase modulation are the ones mostly used in the optical device applications. Depending on the addressing technique, SLMs can be divided into two categories, optically addressed SLMs (OASLMs) and electrically addressed SLMs (EASLMs) as shown in Fig. 2.1. In some applications both optical

and electrical addressed SLMs are used [1]. SLMs are also classified by transmissive type and reflective type. Transmissive SLMs are designed to allow or block light from light source illuminating from the backside of a SLM. Reflective SLMs use light source from the front of a SLM. The light source from the front is then reflected off a reflector at the back of the SLM.

The work of this thesis will only use EASLMs which modulate light by applying electric fields. EASLMs are pixelated devices, which leads to some diffraction related effects when used in coherent optical systems. There are three types of EASLMs: direct addressing, passive matrix addressing and active matrix (Si-backplane) addressing. In active matrix devices, each pixel has its own driving circuit element so that it reduces addressing time. Active matrix addressing is the best method for driving a large number of pixels in optical processing and high-resolution displays.

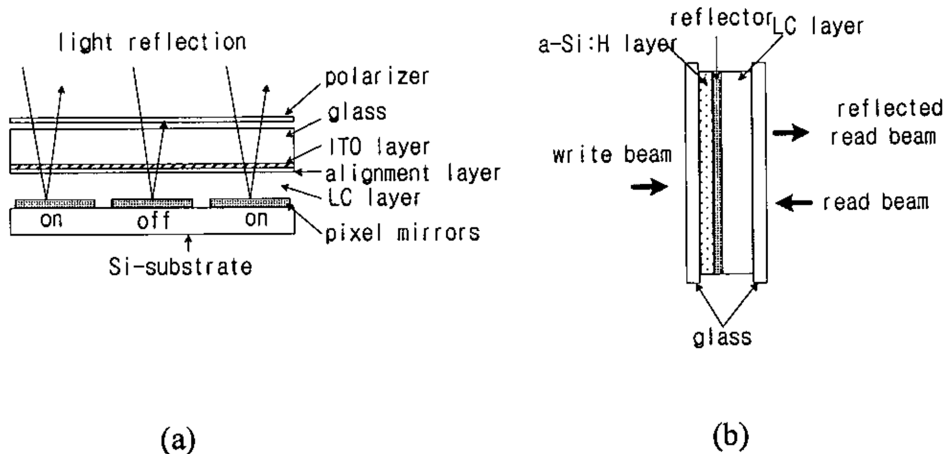


Fig. 2.1: Spatial light modulator configurations (a) Electrically addressed SLM (b) Optically addressed SLM

OASLMs use a photosensitive surface as part of the device structure, which allows light intensity on the OASLMs to display a desired pattern. One typical OASLM uses a hydrogenated amorphous silicon (a-Si:H) photoconductor as shown in Fig. 2.1 (b) [2]. The resistivity of the photoconductor varies with intensity of the illuminated light. In a dark state, for example, the resistivity is high and most of the voltage is

applied to the photoconductor so that there is not enough voltage left to switch the LC layer on. The optical resolution of OASLMs is 10-100 times higher than that of EASLMs and response time is usually limited by removal rate of the photogenerated carriers in the photoconductor layer.

2.2.1 Applications of SLMs

There are many nondisplay applications of SLMs, and I will briefly review some important examples such as optical interconnects, optical correlators, wavelength filters, optical neural networks and optical tweezers.

In telecommunications transmission, optical interconnections are used to carry information because they have more capacity and bandwidth than electronic systems [3] [4]. The optical interconnections may use free space optics with reconfigurable interconnection patterns. Free-space optical interconnections have large interconnection density, high distance-bandwidth product, low power dissipation, and superior crosstalk performance at high-speeds [5] [6]. There are two types of optical switches: holographic switches (see Fig. 2.2(a)), in which the light is directed to the desired channels by reconfigurable holograms, and shutter-based switches (see Fig. 2.2(b)), in which the routing mechanism is based on the blocking of light to unwanted channels. An optically transparent crossbar switch was demonstrated using reconfigurable holograms based on a ferroelectric liquid crystal (FLC) on silicon SLM, with a 3×3 optical crossconnect for use in the telecommunications network [7]. The crossbar switch can provide a nonblocking connection between any number of transmitter and receiver with the insertion loss of 5 dB and crosstalk figure of -25dB.

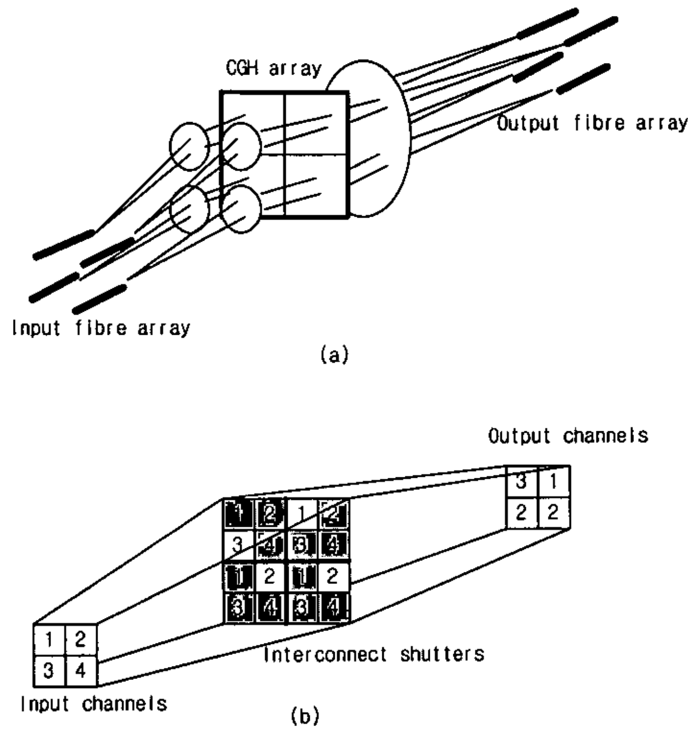


Fig. 2.2: Schematics of the interconnect switches [177]

(a) holographic switches using reconfigurable holograms. (b) shutter-based switches blocking of light to unwaned channels.

Optical correlators are capable of matching input objects with known objects stored in a database. Optical correlators are used for optical character recognition, optical inspection in manufacturing, and object identification and tracking [8]. There are two main methods (see Fig. 2.3): Vander Lugt correlators and joint transform correlators.

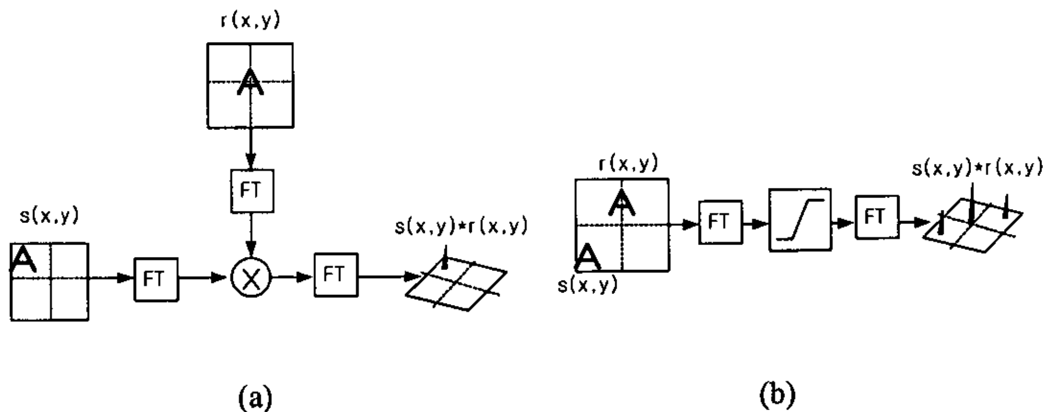


Fig. 2.3: Basic principles of correlators [177] (a) Vander Lugt correlator (b) joint transform correlator

Vander Lugt correlators [9] perform a correlation between the Fourier transforms of the input image and the reference images, and if the two images are identical the correlation peaks occur at the output. These correlation peaks are however smaller if the objects are rotated, or have different sizes. Thus fast frame rate SLMs are needed for useful operation. Joint transform correlators [10] [11] perform optical correlation by displaying the input and reference images side by side in a SLM and then Fourier transform them to produce a joint power spectrum with a single lens. Nonlinear processing of the joint power spectrum is needed to improve the quality of the correlation. Another Fourier transformation is necessary to produce the output.

Wavelength tunable filters can be used for telecommunications and RGB colour filters. Within optical telecommunications, the technique of wavelength-division multiplexing (WDM) carries many signals at different wavelengths down the same fibre. Affordable high-performance wavelength tunable filters are needed to make economic and reliable WDM components. For a wavelength filter that requires channels separated by 0.8nm centered at a wavelength of 1550nm, a simple grating can be used as different wavelengths are diffracted at different angles as the light passes through the grating. As shown in Fig. 2.4 (a), the tuning mechanism for the wavelength filter can be achieved as the angle of the diffracted light β for a wavelength λ is varied by changing the grating pitch d of an SLM [12]. For RGB colour filter applications polarization modulation of a SLM can be used to convert the band of wavelengths to a polarization state which can be blocked by a polarizer. A fast-tunable colour filter based on the effect of polarization modulation is shown in Fig. 2.4 (b) [13]. This colour filter system consists of five ferroelectric LC cells with different thickness, placed between three polarizers. Five different colours can be selected by switching different combinations of cells that each cell has an associated birefringence and switching angle. The colour filter system has fast switching time (350μs) and can be used for producing colour sequential backlighting to achieve a full-colour image.

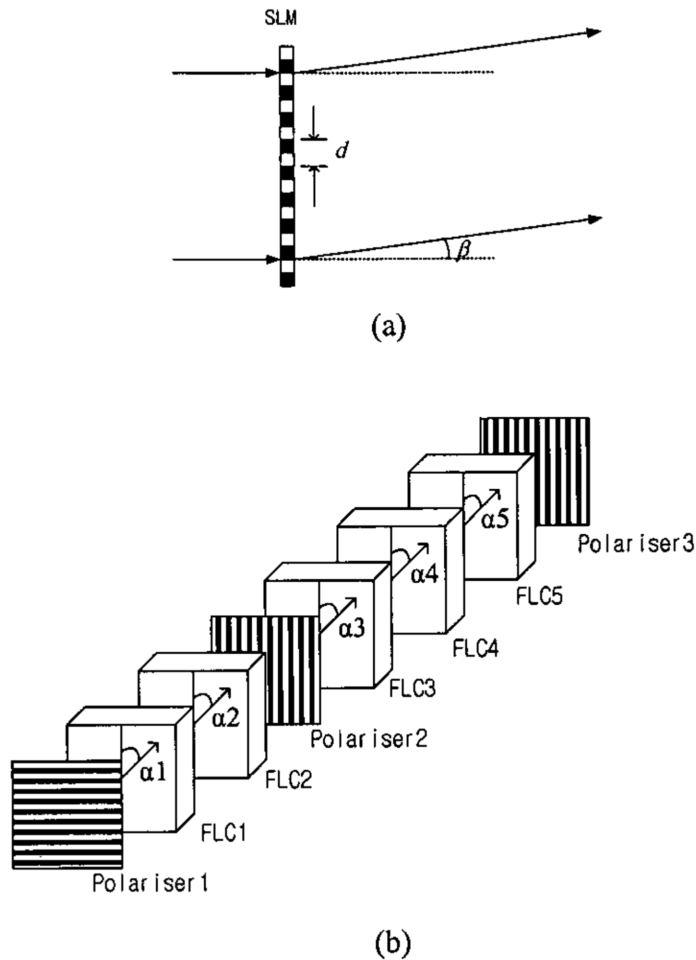


Fig. 2.4: Applications of wavelength tunable filters [177] (a) optical tuning for telecommunications (b) cascaded FLC system for colour filters

Neural networks have been established for the implementation of computing architectures, especially for large-scale problems that require highly parallel and enormous numbers of interconnections [14][15]. Neural networks include several layers of processors that map a set of input conditions onto a set of output conditions to perform a system function. The functionality of the system is determined by the interconnection weights and the network trainings by modifying the interconnection weights. SLMs can be used as optical shutters for optical vector processing in neural network systems shown in Fig. 2.5 (a) [16]. In this system two SLMs are used as binary weighting masks and the diffuser is used to eliminate any angular information between the two stages. SLMs also can be used as holographic devices to control weights in neural networks like that shown in Fig. 2.5 (b) [17] [18]. In this system an array of neuron outputs is interconnected to an array of neuron inputs through a

multifaceted hologram. Each neuron input illuminates a single sub-hologram, which forms weighted connections to the other neuron inputs in the output plane.

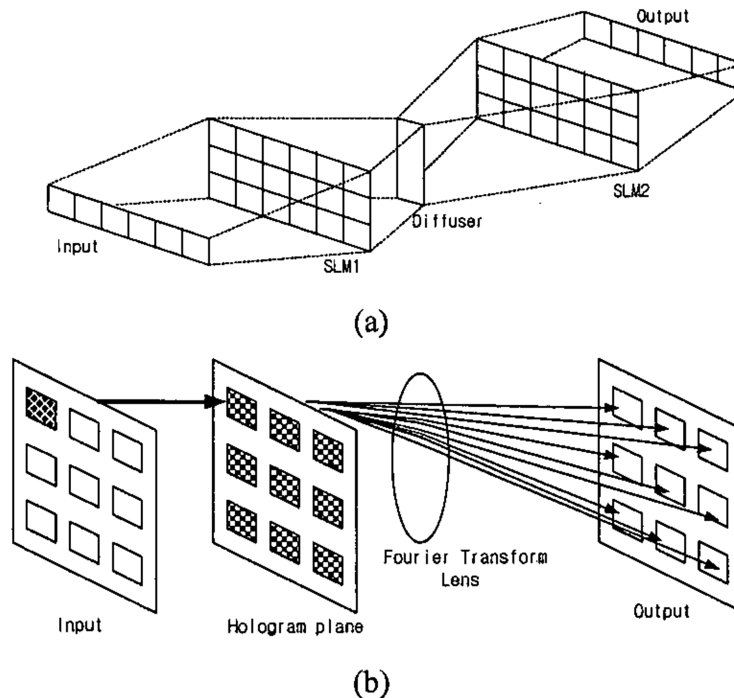


Fig. 2.5: Neural network systems [177] (a) using an optical vector processor (b) using a computer generated hologram device

Another application of SLMs is optical tweezers that are capable of trapping microscopic particles in a strongly focused beam of light. Optical tweezers have been developed for trapping and positioning of objects [19] [20], cells and bacteria [21], since the first optical tweezers were developed by A. Ashkin in 1986 [22]. A computer-generated hologram on a SLM in the optical tweezers can transform a single laser beam into multiple optical traps, each with individually specified characteristics, manipulated in real time.

2.2.2 Device technologies

A number of modulating technologies have been developed recently, using electro-optic, magneto-optic or mechanical properties. Some typical devices include Self Electro-optic Devices (SEED), magneto-optic modulator, Digital Micromirror Devices (DMD), PLZT devices, Grating Light Valves (GLV) and liquid crystal

devices.

Self Electro-optic Devices (SEED) are a kind of Multiple Quantum Well (MQW) device, which allow absorption of certain wavelength of light known as the Quantum Confined Stark Effect (QCSE). Amplitude light modulation can be obtained by applying the electric field to the MQW stack layers. The MQW structure has very high switching time (10 picoseconds) and high contrast ratio (12 dB) [178], although it requires very high powers for its optical and electrical control [23] [166]. Self Electro-optic Devices (SEED) can be constructed by placing MQW structures into p-i-n (or n-i-n) diode structures. Using the high speed of SEED devices, flip-chip bonding SEED devices have been developed onto Si-substrates [24] [167]. This device is suitable for optical systems such as telecommunication switching, due to its high switching ability with integrated large arrays [168].

Magneto-optic modulators are electrically addressed solid-state devices, which use the Faraday effect to rotate incident polarized light [25] [169] [170]. A magneto-optic substrate is pixelated and the magnetic domains are aligned to the film surface. A bistable magnetic domain is produced on the intersection of the address lines, which causes a different rotation of the polarization of incident light. The devices suffer from some issues such as slow switching speed, low contrast and high heat dissipation.

Digital micromirror devices (DMD) have been developed by Texas Instruments, which consist of arrays of micro-mechanical mirrors fabricated on CMOS Si-Substrates [26] [27] [171]-[173]. The electrostatically deflected mirrors can produce amplitude modulation. The schematic diagram of Fig. 2.6 shows an exploded view of a typical DMD pixel mirror. The mirror is connected to an underlying yoke which is suspended by two thin torsion hinges to support posts. The yoke is electrostatically attracted to mirror address electrodes. The address electrodes and yoke are connected to the complimentary sides of the underlying SRAM circuit. The state of the SRAM circuit (1,0) determines the mirror rotation angle to $+10°$ or $-10°$. When the mirror rotates to its on state ($+10°$), the incident light is directed into the optical imaging

system and the pixel appears bright. When the mirror rotates to its off states (-10°), the light is directed to out of the optical imaging system and the pixel appears dark. Despite its binary mode, grey scale is achieved by pulse width modulation (PWM) and colour is also achieved by time multiplexing with separated R,G,B light sources.

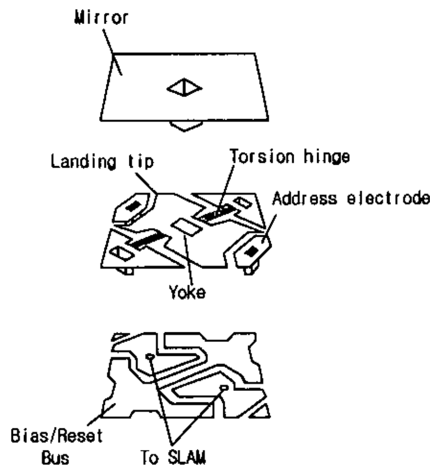
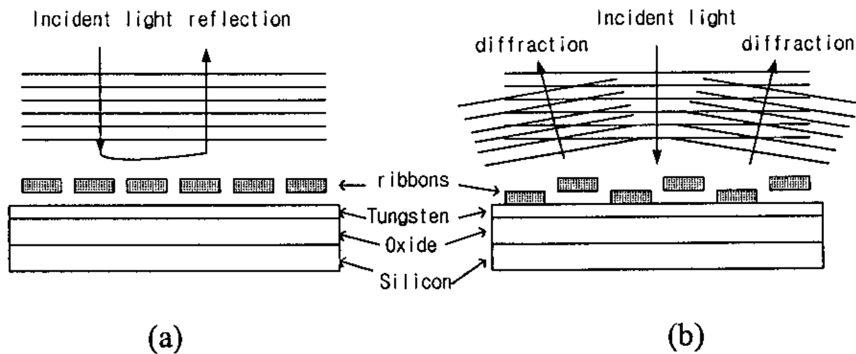


Fig. 2.6: Schematic of a digital micromirror device. The mirror can tilt ±10 degrees.

PLZT devices use Lead lathanum zirconate titanate (PLZT), which is an excellent material for use in SLMs due to their large electro-optic effect and low absorption for thin wafers [28] [174] [175]. PLZT materials show the Pockels effect that exhibits birefringence of the materials proportional to an applied electric field [29] [30]. Although phase or amplitude modulation is achieved by the induced birefringence, PLZT devices are very expensive to manufacture and need high electric field to drive the devices.

A grating light valve (GLV) is a micro-mechanical device on the surface of a silicon chip [31] [32]. A GLV pixel consists of a number of aluminum-coated ribbons, each about 100μm long, 100nm thick silicon nitride and about 3μm wide. The ribbons float above a thin air gap (about 650nm) allowing them to move vertically relative to the plane of the surface. Figure 2.7 shows the principle of a GLV pixel. When no voltage is applied, the surface of ribbons acts as a mirror so that the incoming beam is reflected back. When voltage is on, the ribbons are electro-statically pulled down a controlled distance into the air gap and the ribbons form a square-well diffraction

grating which introduces phase offsets between the wavefronts of beam reflected off stationary and deflected ribbons. By varying the width and spacing at each pixel, analog control over the proportion of light can be achieved. The GLV switching takes about 20 ns, about 1,000 times faster than a DMD's switching time. This fast switching property allows GLV systems to use one-dimensional arrays that are scanned to produce a two-dimensional image.



(a) (b)

Fig. 2.7: Operating principles of a GLV pixel. (a) When the pixel is off state, the ribbons acts as a mirror so that the incoming beam is reflected back. (b) When the pixel is on state, the ribbons are pulled down a distance and form a diffraction grating.

Liquid crystal (LC) devices are suitable for SLMs because they exhibit high birefringence with low driving voltage and power, which allows low-cost devices. With the applied voltage on pixels, liquid crystal devices achieve either phase or amplitude modulation. Most LC devices or configurations actually modulate polarisation. External components (polarisers, analysers) then convert to amplitude or phase. The switching time is mainly dependant on the liquid crystal; nematic LC material is slow (10-100ms) and ferroelectric LC is fast (10-100μs). Ferroelectric LCs have a permanent non-zero polarization known as spontaneous polarization, which exhibits bistability and allows high-speed optical switching in SLMs. In most transmissive type SLMs, a simple passive-matrix addressing switches one line at a time basis which results in low frame rate. For high-speed switching and high-frame rates, it is suitable to introduce active matrix addressed devices such as thin film transistors (TFT) for the transmissive type and silicon backplane (LCoS) devices for the reflective type. TFT devices are superior for image display, but panels are rather

large with small fill-factor, and not flat enough for coherent optics applications. However, LCoS devices have excellent optical properties with respect to diffractive optical element, pixel fill factor, and surface flatness.

2.2.3 LCoS devices

LCoS devices [33] are hybrid displays that combine LCD technology with CMOS silicon technology. As shown in the Fig. 2.8, a reflective LCoS device features a silicon backplane fabricated in a CMOS foundry, with a liquid crystal layer and cover glass on top. Electro-optic modulation is achieved by sandwiching a very thin layer of liquid crystal material between a conductive and transparent electrode (ITO coated glass) and a CMOS silicon backplane. The silicon backplane, made of an array of 1-bit digital memory cells/pixels, allows local light modulation via switching of liquid crystal molecules. Ferroelectric liquid crystals (FLCs) are commonly used because these achieve fast switching which is preferable in many optics applications. A spacer layer is used to control the gap between the two electrodes. In order to obtain the appropriate molecular ordering in the liquid crystal medium, alignment layers are deposited on top of the backplane surfaces. Planarised aluminum mirrors are electrically connected to the underlying circuitry to address the liquid crystal layer and reflect the incoming light [34].

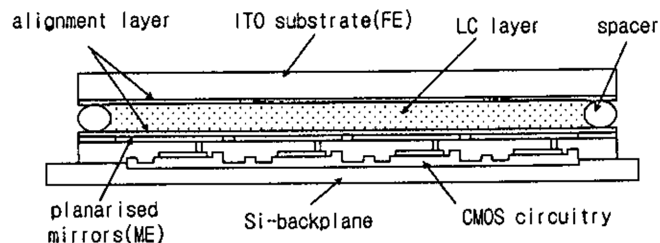


Fig. 2.8: Simplified schematic cross section of an LCoS device. The CMOS circuitry includes CMOS transistors and capacitors. Planarised mirrors are connected to the drain of a transistor and a capacitor.

The LCoS devices are advantageous in terms of viewing angle and switching voltage. Since the devices need a cell gap about half of that of transmissive devices, the

viewing angle will be wider and the switching voltage will be lower to maintain the same electric field effect. However, its disadvantage is that the reflective devices need a more complicated optical system.

2.3 Spatial light modulation in reflective LCoS devices

LCoS devices use electro-optic effects based on liquid crystals. This section investigates how LCoS devices interact with light by describing the properties of polarized light, retardation plates and reflection on a mirror.

Monochromatic light sources can be represented in terms of an orthogonal set of propagating eigenwaves. If an incident light with polarization state, we can describe it with a Jones vector

$$\mathbf{V} = \begin{pmatrix} V_x \\ V_y \cdot e^{j\phi} \end{pmatrix} \tag{2.1}$$

where V_x and V_y are two complex numbers, and ϕ is a phase difference. The left side of Fig. 2.9 (a) shows the electric field of linearly polarized state where two light waves are in phase and the propagation of the wave in the z direction. The right side of Fig. 2.9 (a) shows the polarisation state of the wave in the xy plane. If the two waves have 90° phase difference, the resulting wave is circularly polarized as shown in Fig. 2.9 (b).

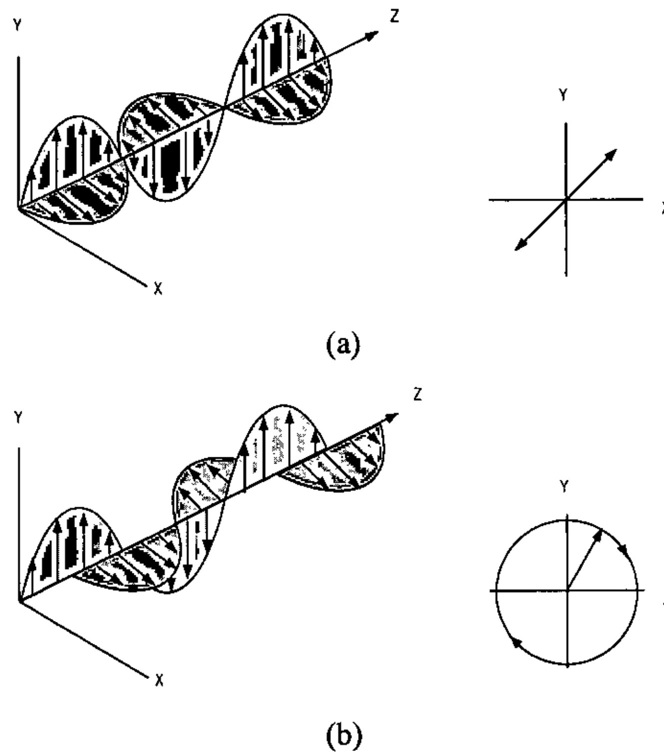


Fig. 2.9: Eigenwaves of polarized light (a) linearly polarized light (b) circularly polarized light

If linearly polarized light travels through a birefringent crystal, a phase difference will be introduced between the light with V parallel to the optic axis and the light with V perpendicular to the optic axis. When light of wavelength λ passes through a birefringent crystal of thickness d, the phase retardation for a transmissive type SLM is defined as [158]

$$\Gamma(transmissive) = \frac{2\pi}{\lambda}(n_e - n_o)d \tag{2.2}$$

where n_e and n_o are the refractive indices extraordinary and ordinary to the crystal director.

In a reflective type SLM, the retardation is doubled in the same thickness d, due to the double pass in the liquid crystal layer, defined as

$$\Gamma(reflective) = \frac{4\pi}{\lambda}(n_e - n_o)d \tag{2.3}$$

A coordinate transformation is needed to determine how the light propagates in the retardation plate. The general retardation plate can be defined as [157]

$$W = R(-\psi)W_0 R(\psi) \tag{2.4}$$

where $R(\psi)$ is the coordinate rotation matrix and W_0 is the Jones matrix for the retardation plate. If the retardation plate has an arbitrary angle Ψ about the y-axis, then the coordinate rotation matrix can be defined as [157]

$$R(\psi) = \begin{pmatrix} \cos\psi & \sin\psi \\ -\sin\psi & \cos\psi \end{pmatrix} \tag{2.5}$$

By assuming that the fast axis of the retardation plate is parallel to the y-axis, we can define the Jones matrix W_0 as

$$W_0 = \begin{pmatrix} e^{-j\Gamma/2} & 0 \\ 0 & e^{j\Gamma/2} \end{pmatrix} \tag{2.6}$$

The general retardation plate can be rewritten by substituting $R(\psi)$ and W_0,

$$\begin{aligned} W &= \begin{pmatrix} \cos\psi & -\sin\psi \\ \sin\psi & \cos\psi \end{pmatrix} \begin{pmatrix} e^{-j\Gamma/2} & 0 \\ 0 & e^{j\Gamma/2} \end{pmatrix} \begin{pmatrix} \cos\psi & \sin\psi \\ -\sin\psi & \cos\psi \end{pmatrix} \\ &= \begin{pmatrix} e^{-j\Gamma/2}\cos^2\psi + e^{j\Gamma/2}\sin^2\psi & -j\sin\frac{\Gamma}{2}\sin(2\psi) \\ -j\sin\frac{\Gamma}{2}\sin(2\psi) & e^{j\Gamma/2}\cos^2\psi + e^{-j\Gamma/2}\sin^2\psi \end{pmatrix} \end{aligned} \tag{2.7}$$

If a wave plate has phase retardation of $\Gamma = \pi$, the plate is called a half wave plate. The Jones matrix for a half waveplate at an angle Ψ will be

$$W=\begin{pmatrix} -j\cos 2\psi & -j\sin 2\psi \\ -j\sin 2\psi & j\cos 2\psi \end{pmatrix} \tag{2.8}$$

For an azimuth angle Ψ relative to the optic axis, the half wave plate will rotate the polarization by an angle of 2Ψ shown in Fig. 2.10.

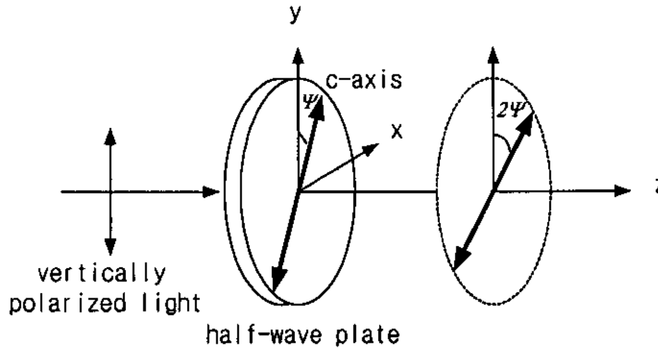


Fig. 2.10: Effect of a half-wave plate on the polarization state of linearly polarized light

If a wave plate has a phase retardation of $\Gamma = \pi/2$, the plate is called a quarter wave plate. A quarter wave plate can convert linearly polarized light into circularly polarized light and vice versa. If the quarter wave plate has the azimuth angle of 45 and the input light is vertically polarized, the Jones matrix for the output light through the quarter wave plate will be

$$\begin{pmatrix} V'_x \\ V'_y \end{pmatrix} = \begin{pmatrix} \cos 45^\circ & -\sin 45^\circ \\ \sin 45^\circ & \cos 45^\circ \end{pmatrix} \begin{pmatrix} e^{-j\pi/4} & 0 \\ 0 & e^{j\pi/4} \end{pmatrix} \begin{pmatrix} \cos 45^\circ & \sin 45^\circ \\ -\sin 45^\circ & \cos 45^\circ \end{pmatrix} \begin{pmatrix} 0 \\ 1 \end{pmatrix}$$
$$= \frac{-j}{\sqrt{2}} \begin{pmatrix} 1 \\ j \end{pmatrix} \tag{2.9}$$

The equation shows that the vertically polarized input changes to left-hand circularly polarized output shown in Fig. 2.11.

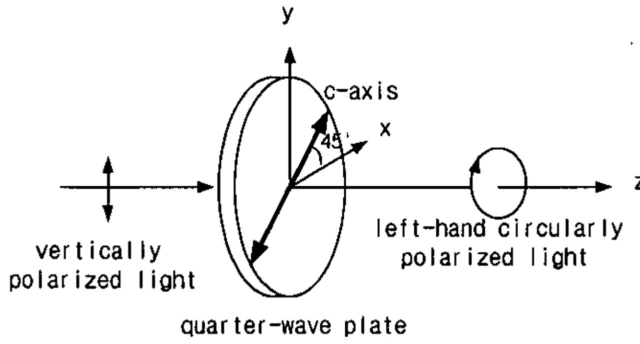


Fig. 2.11: Effect of a quarter-wave plate on the polarization state of a linearly polarized light

When a beam is reflected on a mirror, the Jones matrix for the mirror-reflected beam M_m can be defined as [157]

$$M_m = \tilde{M}(\theta, \phi + \pi) \tag{2.10}$$

where θ is the polar angle and ϕ is the azimuth angle. The equation (2.10) reflects the fact that the azimuth angle of π has been shifted on the reflected beam. This means if the left-hand circularly polarized beam is incident on the mirror then right-hand circularly polarized beam will be reflected from the mirror.

Optical properties in an LCoS device can be depicted as shown in Fig. 2.12. A polarizer is attached to the front side of the FLC layer and placed parallel to the optical axis of the FLC layer. The polarizer passes a single linear state while blocking all other polarisation states. When the FLC cell is in its off-state, linearly polarized light is parallel to the optical axis of the FLC layer and passes through the FLC without optical modulation. The reflected light passes through the polarizer due to the same polarisation. When the FLC cell is in its on-state, the FLC cell acts as quarter-wave plate and changes the linearly polarized light to left-hand circularly polarized light. With reflection on the mirror, the left-hand circularly polarized beam is changed to light-hand circularly polarized beam. When the light-hand circularly polarized beam passes through FLC layer again, the circularly polarized beam is changed to a linearly polarized light which is blocked at the polarizer.

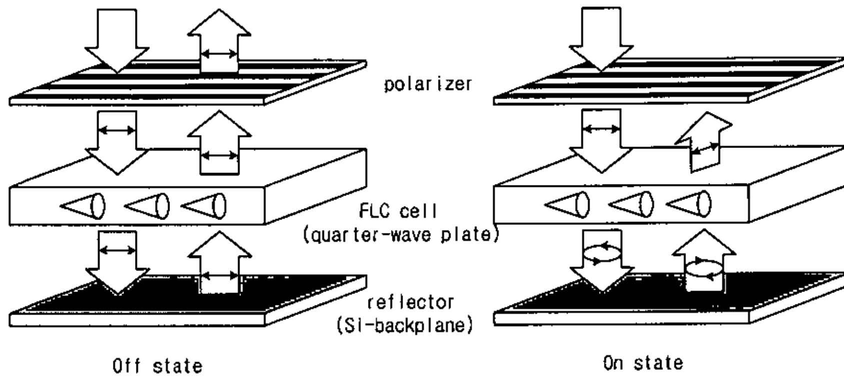


Fig. 2.12: The configuration of optical properties in an LCoS device. When the FLC cell is off state, no optical modulation occurs in the FLC layer. When the FLC cell is on state, the FLC cell acts as quarter-wave plate.

2.4 Phase modulation

This section compares how phase modulation and amplitude modulation work in SLMs. SLMs have an ability to control not only the intensity of light but also the phase of the light. Phase modulation has benefits in its applications over amplitude modulation such as increased efficiency, ease of alignment in axial optics, lower spatial frequencies and superior performance in optical correlators [35].

An amplitude modulator can be constructed by using a LCSLM. If we use binary switching SLMs like SSFLC devices we can get binary amplitude modulation shown in Fig. 2.13. If incident light is parallel to the ordinary axis of the FLC, then no optical modulation occurs due to the birefringence and the transmitted light being blocked at the crossed analyzer. By switching the modulator to the other state, the FLC switching angle θ rotates the incident light by 2θ and transmits the analyzer if the FLC acts as a half-wave plate. The reflected output intensity in a reflective mode can be calculated by [159]

$$I = I_0 \sin^2(4\varphi)\sin^2(\frac{2\Delta n d\pi}{\lambda}) \quad (2.11)$$

where I is the reflected output intensity, I_0 is the input intensity, φ is the angle between input polarizer and LC alignment direction, Δn is the birefringence, d is the cell gap and λ is the wavelength of light. If the thickness of the FLC layer is correctly set and the switching angle (2φ) is 45°, then the maximum intensity will be transmitted.

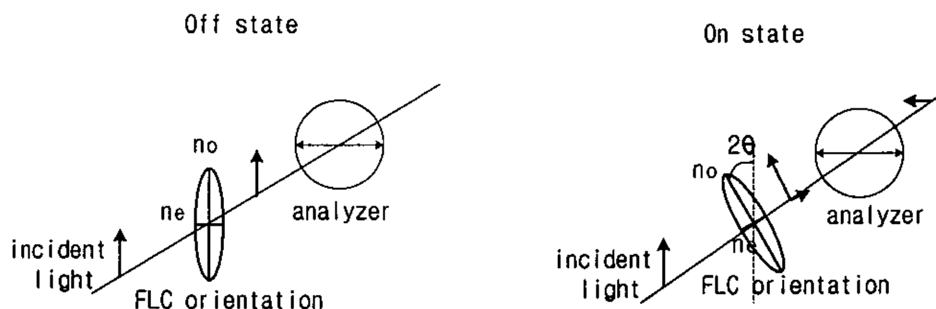


Fig. 2.13: The two states of FLC for amplitude modulation

A phase modulator can be constructed by using a FLC half-wave retarder with two stable orientations for the optical axes, and its operation principle is shown in Fig. 2.14 [147]. If we take vertically polarized light as an input, then the FLC pixel fast axis positions must bisect the vertical axis and will be oriented at angles of θ and $-\theta$, respectively. The difference between two switching states results in π phase modulation.

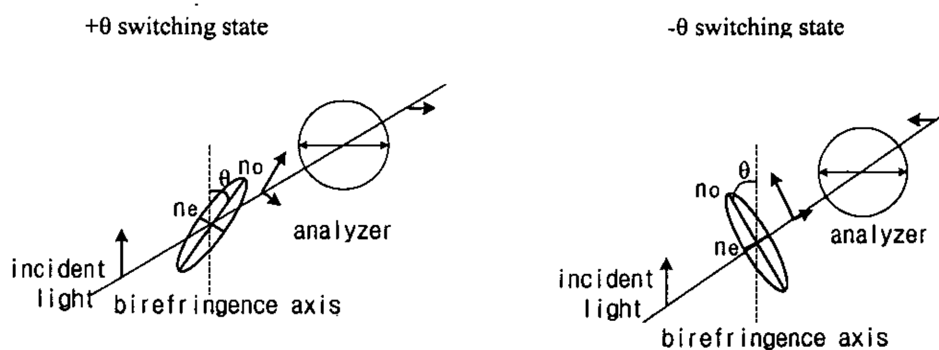


Fig. 2.14: The two states of FLC for phase modulation

2.5 Issues for phase modulation of LCoS devices

In constructing LCoS devices, there are several parameters that affect phase modulation performance. The main issues requiring improvement in LCoS devices are cell gap uniformity, LC alignment, and the backplane flatness.

The optical modulation of LCoS devices is sensitive to cell gap. Any variation in thickness of the LC layer across the active display area will result in a reduction in performance [36]. The variation in cell gap also affects the liquid crystal flow, when the LC material is injected into the device, resulting in poor LC alignment [37]. The cell gap is mainly determined by the size of the spacer balls available. Various spacer layer configurations have been developed for uniform cell gap [38].

Any improper LC alignment also reduces the optical modulation performance of LCoS devices. During the injection of LC into the cell the LC alignment is affected by critical factors such as the LC cell filling speed, the LC flow front direction, and the substrate topology [39]. The LC flow control method was investigated using microfabrication techniques [37].

A LCoS backplane consists of an array of pixels where each pixel controls the voltage on an electrode. These electrodes should be flat and as close as possible to perfect mirrors reflecting incident light. The surface flatness of the mirrors for phase modulation has to be at least $\lambda/10$ [40]. The optical performance is also influenced by the pixel mirror fill factor, the area of the mirror to the pixel size. Any uneven surface features like trenches between adjacent mirrors degrade phase modulation performance. Planarisation techniques [41] [42] that include chemical mechanical polishing are used to provide the large fill factor and the flat surfaces necessary for good mirrors.

Another limiting factor in using LCoS devices is the pixelated structure. The structural size of LCoS devices is small enough to create diffraction effects. The

detailed diffraction theory and issues in using LCoS devices as phase elements are presented in Appendix I. The pixel size is important as a design parameter for optical applications; however, the pixel size of an LCoS device cannot be changed easily. The pixelated structure also causes diffraction noise and energy loss [43]. Thus the phase modulation properties are somewhat limited and cannot be optimised easily at a specific wavelength.

LCoS devices can be operated as a phase modulator to generate diffraction patterns in a Fourier transform optical system. The diffraction patterns can be generated by gratings or computer generated holograms (CGHs) that are displayed on the SLM. The detailed CGH theory and limitations concerning the optical efficiency in the system are presented in Appendix II.

2.6 Summary and discussion

Spatial light modulators are devices capable of applying a spatially controlled modulation to an incident wavefront which makes them ideally suited for optical processing systems. There are two basic types of SLMs: electrically addressed SLMs which convert electrical signals to spatial modulation and optically addressed SLMs which convert incoherent light to spatial modulation. OASLMs can achieve higher resolution than EASLMs but it is very expensive to make these devices. Even though OASLMs are more suitable for compensation of phase distortions of wavefront due to the non-pixelated structure, EASLMs are presently the major components in most optical processing applications.

SLMs are key components in a wide range of optical processing applications such as optical interconnects, optical correlators, wavelength filters, optical neural networks and optical tweezers. These applications have been widely researched, and the evolution of the SLM technology is a key factor in commercialising these applications. The advantages of using SLMs in optical systems over electronic systems are higher efficiency, faster response, high bandwidth and longer lifetime.

A number of modulating technologies have been introduced. The main characteristics of the technologies are summarized as below.

- Self Electro-optic Device: Non-linear optical effect can be obtained by using Multiple Quantum Well stack layers. High switching speed (10 picoseconds) and high contrast ratio (>100:1), but difficult to make large arrays.
- Magneto-optic Modulators: Pixelated crystal film switched by array of magnetic domains using the Faraday effect. Slow switching speed, low contrast and high heat dissipation.
- Digital Micromirror Devices: Formed by arrays of micro-mechanical mirrors on to Si-substrates. Switching in binary mode and expensive to manufacture.
- PLZT devices: Use Pockels Effect that exhibits birefringence of PLZT.
- Grating Light Valve: One dimensional arrays that consists of aluminum-coated ribbons with fast switching (20 ns). Very high optical efficiency by driving analog phase control, but the device is not commercially available yet.
- Liquid Crystal devices: High birefringence with low driving voltage and power, and low-cost device, thus widely used for SLMs.

LCoS devices consist of a silicon-CMOS backplane and a liquid crystal layer in direct contact with the silicon chip. LCoS devices are attractive for use in optical processing systems because of their compact size and ease of system integration. LCoS devices can be made optically flat, and small enough for matching with small optics, thus the devices are ideal for coherent applications. The LC layer acts as half-wave plate to modulate the optical properties, combining with mirror electrodes. The electro-optic effects of LCoS device were reviewed by describing the properties of polarized light, retardation plates and mirror reflection.

There are several issues in manufacturing LCoS devices for coherent optical applications. Firstly, any cell-gap variation across the panel is critical due to reduction in optical performance. LC alignment technique is also important because the optical performance is affected by LC cell filling speed, the LC flow front direction, and the substrate topology. Another factor is backplane flatness which needs at least $\lambda/10$. The pixelated structure is also another limiting factor because it

causes diffraction noise and energy loss.

Phase modulation has several advantages over amplitude modulation in the coherent optical applications. The advantages are higher efficiency, ease of alignment in axial optics and lower spatial frequencies. Thus characterization of phase modulation on LCoS devices is highly demanded for coherent optical applications.

Chapter 3:

Liquid Crystals for LCoS Devices

3.1 Introduction

This chapter reviews the basic theory of light modulation for liquid crystal on silicon (LCoS) devices using nematic and ferroelectric materials, and describes their optical and electrical properties. A brief introduction of liquid crystals shall lead quickly to an appreciation of their use in phase modulating SLMs.

Nematic liquid crystals (NLCs) are widely used in SLMs due to their relative ease of fabrication. Nematic LC modes utilizing polarization rotation and birefringence effects are the most commonly used modes in LCoS devices due to their flexibility and maturity of fabrication. The nematic electro-optical effects for reflective LCoS applications are reviewed, for both non-twisted and twisted mode systems.

Ferroelectric liquid crystals (FLCs) are attractive materials for use in display applications as well as integrated optical non-display applications because of their fast (μs) non-linear electro-optic effects. A brief overview of the electro-optical properties of ferroelectric and antiferroelectric LC materials will be made, together with the equations to enable these electro-optical properties to be used in the electronic circuit simulations of the subsequent chapter, which will be used for a device optimisation.

3.2 Liquid crystals

Liquid crystals are intermediate states between isotropic liquids and solid crystals. Molecules in the solid state have fixed position and orientation, with a small amount of variation relative to the intermolecular separation. Most solids are difficult to deform due to their large intermolecular forces which impose positional and orientational order. On the other hand, the molecules of a liquid phase have no fixed position or orientation and are free to move in a random motion. A liquid can be described as positionally and orientationally isotropic.

In the liquid crystal state, liquid crystal materials possess some degree of orientational ordering, and may also have some positional ordering. Two main classes of liquid crystal materials exist:

- Thermotropic liquid crystals: Thermotropic materials are not solutions and the liquid crystalline phase changes depend only on temperature.
- Lyotropic liquid crystals: Lyotropics are solutions and the liquid crystalline phase changes occur with the influence of solvents.

For this study, we are only interested in themotropic liquid crystals with a rod-like molecular structure. When a solid substance melts to a liquid state, the substance undergoes a phase change to the liquid crystal mesophase such as smectic C (SmC), smectic A(SmA), nematic(N) and ultimately an isotropic liquid as shown in Fig. 3.1.

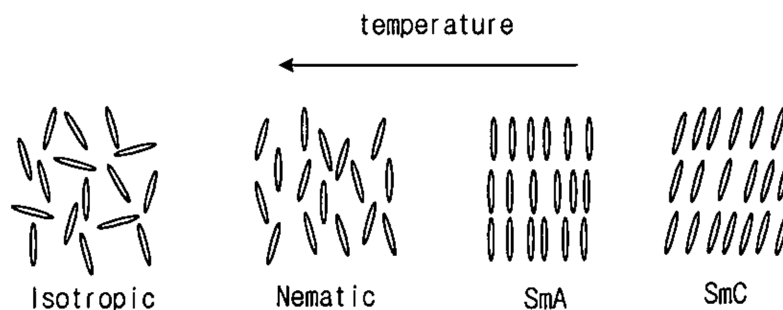


Fig. 3.1: Molecular orientations in different LC phases

3.2.1 Liquid crystal phase

Liquid crystal mesophases are grouped into three classes: nematic, cholesteric, and smectic. This section reviews these liquid crystal phases.

Nematic phase

The nematic liquid crystal molecules exhibit orientational order but no positional order [44]. This ordering causes the molecules to align parallel to one another but still remain fluid. The average direction of the molecules is defined by a vector **n**, called the director. The molecules still tumble and move, but they tend to settle in the average direction **n** (Fig. 3.1). The order parameter of the nematic phase is a measure of the average degree of alignment of the molecules with the director **n**. The order parameter S is given as follows [45]:

$$S = \tfrac{1}{2} \langle 3\cos^2\theta - 1 \rangle \tag{3.1}$$

where < > represents a thermal averaging, θ is the average angle between an individual molecule and the director **n**. The order parameter decreases as the temperature is raised until a transition temperature is reached. S is zero in isotropic liquids, around 0.3 near the nematic-isotropic phase transition and 0.7 near the SmA-nematic phase transition. When all molecules are perfectly aligned, S reaches unity. Optically, nematic liquid crystals constitute a uniaxial medium, with the optical axis along **n**.

Cholesteric phase

Cholesteric liquid crystals have a chiral nematic (N*) structure with a helical precession of the director orientation. The chiral molecules consist of a chiral centre within the molecular structure, and the director spontaneously adopts a helical

arrangement as shown in Fig. 3.2. In this phase the orientation of adjacent molecules is slightly tilted from layer to layer. This induces a complete rotation of the orientation of the director through the material. The helical internal structure can diffract visible light and the periodicity of the helical pitch is temperature dependent with colour change. If the helical pitch is much larger than optical wavelengths, the direction of linearly polarized light incident on the liquid crystal is rotated by the helix as it travels through the liquid crystal. The cholesteric material can be applied in a thermometer because it responds to temperature changes with a colour change of the material.

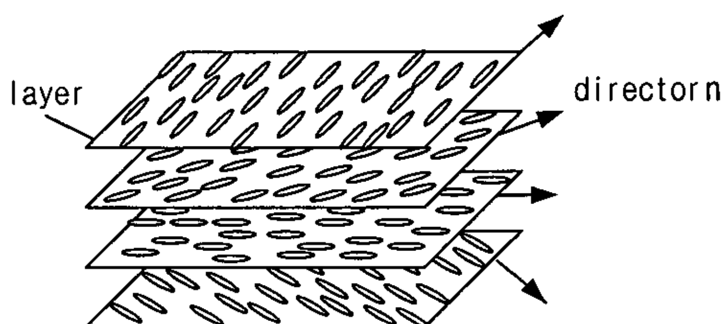


Fig. 3.2: Schematic representation of molecules and director alignment in the chiral nematic phase

Smectic phase

Smectic phases exhibit positional order in that the molecules form parallel layers. The smectic phases form well-defined layers along one direction at lower temperatures than the nematic phase. The molecules can move and rotate within the layer, but maintain the general orientational order of the nematic phase. As shown in Fig. 3.1, the smectic A (Sm A) phase has the director perpendicular to the plane of the layers, and there is no particular positional order within the layer. The smectic C phase forms similar layers, but the director is at a constant tilt angle to the layer normal.

The smectic C phase also may have a chiral state when the director of adjacent layers still has a constant tilt angle from the layer normal, but the tilt angle rotates from layer to layer forming a helix as shown in Fig. 3.3. The chiral smectic phase, denoted by SmC*, possesses permanent polarisation and is thus ferroelectric. These ferroelectric liquid crystals are of particular interest for electro-optical devices, because they typically respond much more quickly to an applied electric field than nematic liquid crystals. For ease of alignment, a liquid crystal material may go through several phases as the temperature is lowered from its isotropic liquid form (e.g. nematic, smectic A, smectic C*); the nematic phase responds to the surface forces more readily than the more viscous smectic phases, and the smectic A phase defines the layering.

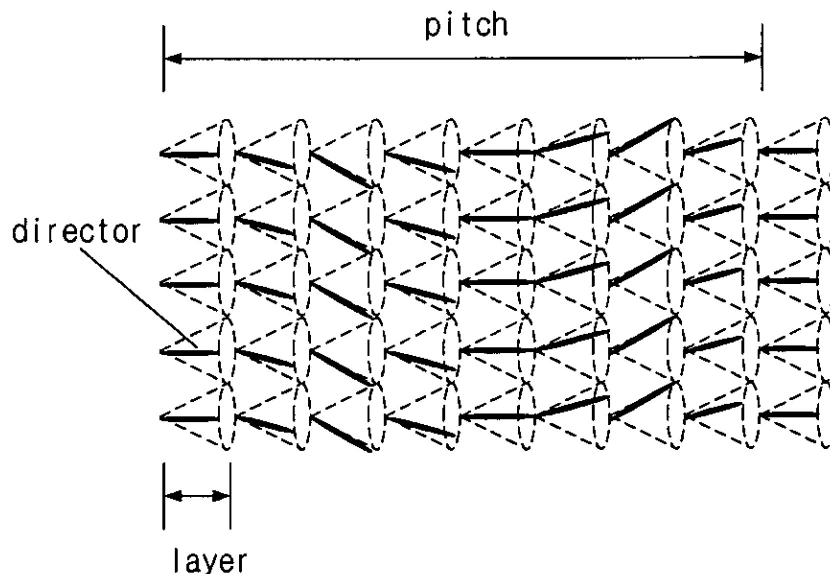


Fig. 3.3: Schematic representation of layer structure and director alignment in the Chiral Smectic C phase

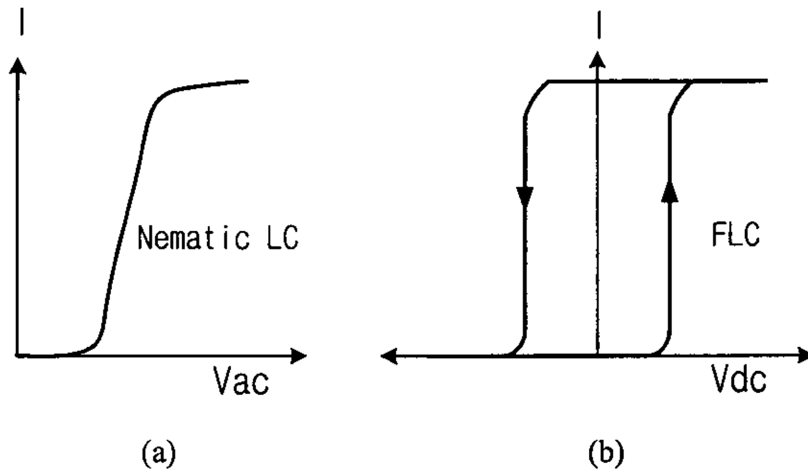
3.2.2 Electric field effects

Liquid crystal molecules tend to have small permanent electric dipoles. This causes the director to align along an external electric field. Even if some liquid crystal molecules do not possess permanent electric dipoles, the electric field can displace

the positive charge to one side and the negative charge to the other side of the molecule. These induced electric dipoles are proportional to the applied field, but generally not stronger than permanent electric dipoles. Generally, liquid crystal molecules possess either permanent or induced electric dipoles that are responsible for their alignment in electric fields.

Nematic liquid crystals (NLC) respond to a DC voltage as the molecules possess an induced dipole, however DC voltages cause decomposition of electrodes in a device. Thus, alternating (~1kHz) voltages with no net DC component are generally used to drive NLCs, as they cannot follow an alternating field and only respond to their RMS value. The molecules relax back to their initial orientations in response to elastic forces if the electric field is removed. The direction of the torque is dependent only on its rms value but it is independent of the sign of the electric field (see Fig. 3.4 (a)). Nematic mode devices are based on the dielectric effect and consequently switching is generally very slow (10ms to 50ms range). The rise time is typically 10 to 20% of the decay time. The rise time and decay time decrease as the temperature rises, the viscosity decreases and the cell thickness decreases.

FLCs, however, have an intrinsic polarization (even in the absence of an applied electric field). Hence the molecules are sensitive to an applied electric field and the torque varies linearly with its magnitude. Due to the spontaneous polarisation, FLCs show hysteresis in response to an applied switching voltage (see Fig. 3.4 (b)). If the hysteresis is sufficiently broad and the transition from one state to the other is sufficiently steep, the FLC remains in its prior state when the applied field is removed.



(a) (b)

Fig. 3.4: LC transfer characteristics (a) Nematic LC devices respond to V_{AC} rms value. (b) FLC devices show hysteresis in response to V_{DC}.

In general, LCoS devices can be operated at low voltage (5-6V), limited by the CMOS circuitry. The operating voltages of NLC are typically 4-6V to achieve minimum transmission and the threshold voltages are in the range of 1-2V. The threshold voltage is related to the dielectric property of a liquid crystal, i.e. the higher the dielectric anisotropy, the lower the threshold voltage obtained. The dielectric anisotropy ($\Delta\varepsilon$) is determined by [160]:

$$\Delta\varepsilon = \varepsilon_{\parallel} - \varepsilon_{\perp} \tag{3.2}$$

where $\varepsilon_{\parallel}$ and $\varepsilon_{\perp}$ are the dielectric constants parallel and perpendicular to the director **n** of the liquid crystal. It is the sign of $\Delta\varepsilon$ which determines how the molecules align themselves in the electric field. LC materials with a positive dielectric anisotropy align themselves parallel to the field whereas LC materials with a negative dielectric anisotropy align themselves perpendicular to the field. In general, nematic liquid crystals have a positive $\Delta\varepsilon$ (the order of 5).

3.2.3 Optical effects

When light propagates through a liquid crystal, the optical anisotropy of the liquid crystal enables light to propagate at a different speed parallel to the director compared with the propagation of light perpendicular to the director. Since the two components propagate at different speeds, the polarisation state of the output waves has changed due to the phase difference. Therefore liquid crystals are said to be birefringent and optically uniaxial. As the refractive index defines the ratio of the speed of light in a vacuum to that in a material, the maximum birefringence (Δn) of the material is given by [160]:

$$\Delta n = n_e - n_o \tag{3.3}$$

where n_e and n_o are the refractive indices extraordinary and ordinary to the liquid crystal director. Depending on the direction of light propagation, Δn varies from zero to the maximum birefringence. For typical liquid crystals with nematic and SmC* phase, the birefringence (Δn) is between 0.15 and 0.2 which gives strong optical effects in thin layers of the liquid crystal material. With this birefringence, either amplitude or phase modulation can be achieved by suitable orientation of a pair of linear polarizers.

3.3 Electro-optical effects in nematic LC

There are two typical nematic LC modes: untwisted mode and twisted mode. The electro-optical effects of those modes are investigated when they are used in reflective SLMs.

3.3.1 Untwisted nematics

A reflective untwisted nematic cell consists of two (ITO on glass and reflective surface) substrates with a polarizer, and a nematic liquid crystal layer between them [46]. Figure 3.5 shows the operation principle for general display applications (this is normally black mode; normally white mode cannot be achieved in a reflective cell),

in which the cell is placed between parallel alignment layers and the polarizer is located at an angle (normally 45°) to the LC alignment layers. In the no-electric field state (Off state) the incoming polarized light is divided into the ordinary wave and the extraordinary wave due to the angle between polarization of the incoming light and the LC alignment layers. There is 90° rotation of polarisation after passing through the cell (if the cell is a half wave retarder) which appears to be dark. When the electric field is applied across the cell (On state) and is gradually increased, the rotation of polarisation decreases, and the cell passes light. There is a threshold voltage (the Fréedericksz transition), determined by liquid crystal properties, cell thickness, and temperature, above which molecular reorientation occurs as the dielectric torque outweighs the alignment forces. As the field continues to increase, more of the molecules in the space between the electrodes are aligned, but the molecules at the surface are still anchored. The rotation of the polarised light is now reduced, so that the majority of the light passes through the liquid crystal layer unrotated. An intermediate field will rotate the director to some intermediate value, so the cell is capable of variable modulation (grey levels) of the light transmission. This mode of operation is called electrically controlled birefringence (ECB).

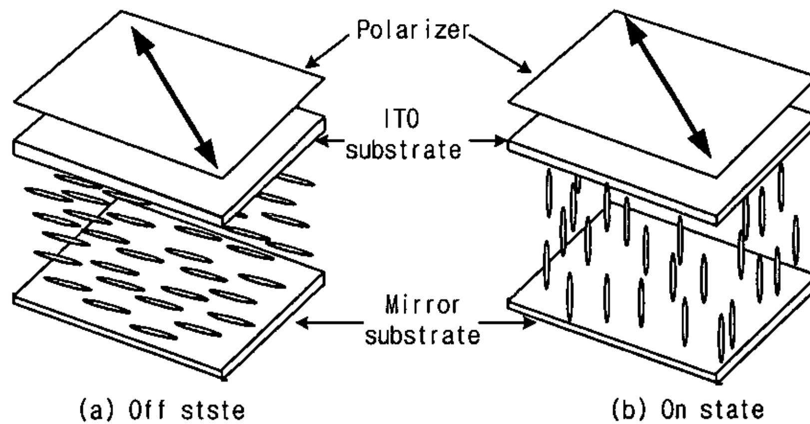


Fig. 3.5: A reflective NLC cell with parallel aligning surfaces for display application (a) In the no electric field state, there is 90° rotation of polarisation which appears to be dark. (b) When the electric field is applied, there is no light modulation that appears to be bright.

After having passed through the cell in the off state, the two orthogonal components of linearly polarised light propagate through the cell at different speeds and result in right-handed circularly polarised light. The light is then reflected at the mirror (left-handed circularly polarised) and propagates back upwards. After the light has reflected through the cell, the delay between the extraordinary ray and the ordinary ray is equal to 180°, which is linearly polarised with the plane of polarisation rotated through 90° ($\lambda/4$). This retardation of $\lambda/4$ transforms linearly polarized light into circularly polarized light as desired at the mirror of the reflective cell. From $\Delta n d$ = $\lambda/4$, the cell gap (d) required for the reflective cell is

$$d = \lambda / 4 \Delta n \tag{3.4}$$

where λ is the light wavelength and Δn is the birefringence.

If ψ is the angle between the polarisation axis of the input light and the axis of the extraordinary refractive index, and incident light enters the cell perpendicularly, the rotation angle of the polarisation will be 2ψ. When ψ is 45°, the light transmission will be maximised. As shown in Fig. 3.6 the intensity of transmitted light (I_T) for this half-wave retarder is given by [161]:

$$I_T = \sin^2\left(2\pi \ d\Delta n/\lambda\right), \tag{3.5}$$

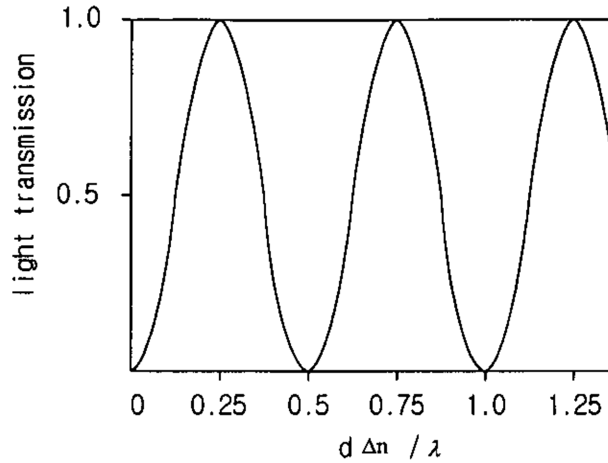


Fig. 3.6 : Relative light transmission of untwisted nematic mode with the LC alignment layer at 45° to the input polarisation axis plotted as a function of cell thickness (expressed $d \cdot \Delta n/\lambda$)

Phase modulation, independent of amplitude modulation, can be achieved using the untwisted nematic mode [47]. Figure 3.7 shows phase modulation in the untwisted nematic LC mode, operating in a reflective SLM. The incoming plane of polarization is parallel to the LC alignment layers. In the off state, the LC molecules align in parallel and the variation of the angle of the molecules through the layer is almost zero. In the on state, the molecules tilt in the direction of the light transmission, maintaining the parallel alignment. If linearly polarized incident light with **E** parallel to director **n** passes through the layer, phase modulation occurs without changing the polarization state. As the molecules tilt, the effective refractive index is decreased, and this leads to the advanced phase of the output wave. If the polarization of the incident light is tilted from the vertical axis, phase modulation occurs only to the component of polarization parallel to the director in the off state and the output state is typically elliptically polarised.

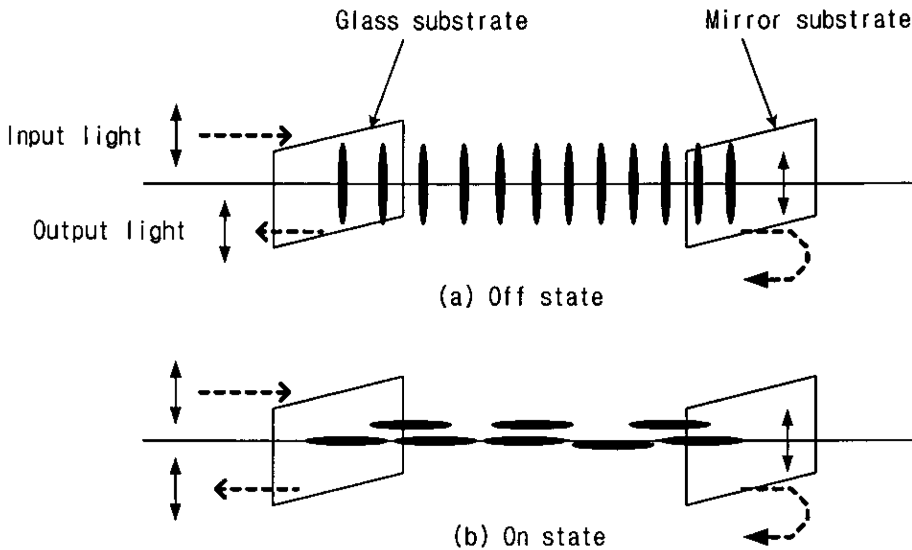


Fig.3.7: Schematic cross section showing mechanism for phase modulation of a reflective SLM when untwisted mode NLC is used. (a) delayed phase of the light output (b) advanced phase of the light output

3.3.2 Twisted nematics

Twisted nematic liquid crystal cells exhibit a twist in the orientation of the LC director axis in the volume between the two alignment layers [48]. The operating principle of the twisted nematic structure in reflective mode is shown in Fig. 3.8. The polarizer is located at an angle to the LC alignment layer. When no external field is applied to the device, surface forces ensure that the device relaxes to its guiding state and undergoes a twist through the thickness of the LC material. The polarizer blocks the output light because the polarization of the input light is changed after passing through the cell. Application of an electric field across the cell rotates the LC molecules parallel to the electric field, which removes the twist and reduces the rotation of the polarised light, therefore the output light passes through the polarizer.

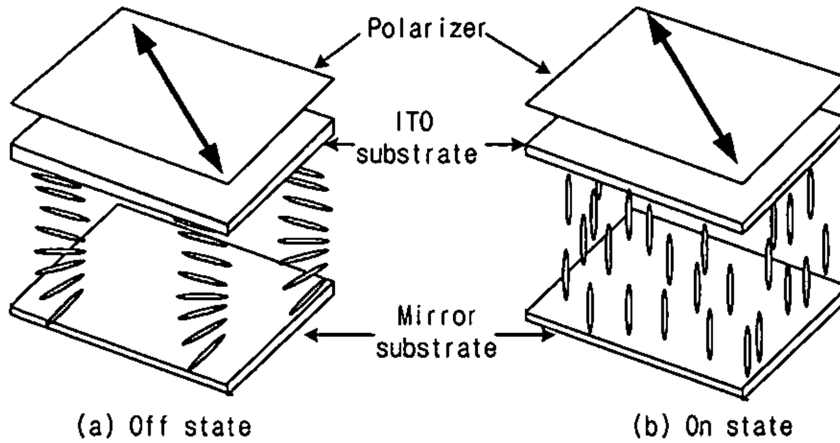


Fig. 3.8: A reflective NLC cell with twisted mode. (a) When off state, the polarisation of input light is changed after passing through the cell and blocked by the polarizer. (b) When on state, the polarisation of input light is not changed so that the output light passes the polarizer.

In this twisted nematic mode, light-transmission efficiency is decided by several different variable combinations such as retardation, input polarisation angle and twist angle. Figure 3.9 shows a case of the light transmission in the twisted nematic mode when the twist angle is around 60° [161].

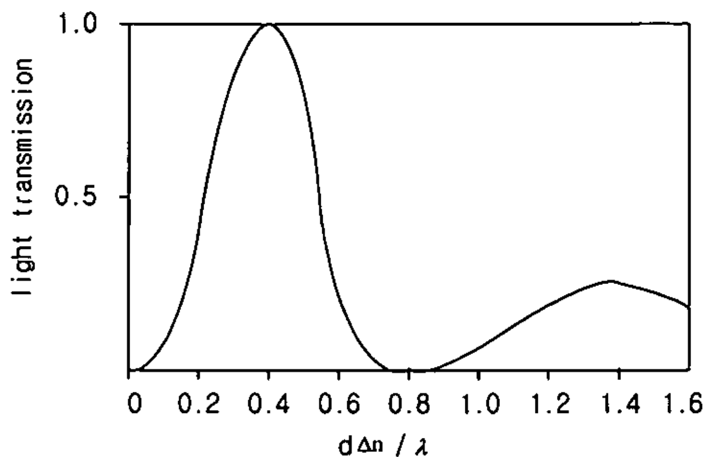


Fig. 3.9: Light transmission of twisted nematic mode plotted as a function of cell thickness (expressed $d \cdot \Delta n/\lambda$)

The twisted nematic device has a poor viewing angle as the cell gap is greater (5~10 μm) than that of a non-twisted nematic device. Response times are typically 10ms (on) and 50ms (off). For transmissive SLMs, the twisted nematic structure has been utilized most frequently since it was firstly introduced in 1971 [48]. However, for reflective SLMs, the twisted nematic structure is not widely used because its optical efficiency is extremely low although it shows high contrast ratio.

In twisted nematic mode, the amplitude of an optical wavefront cannot be modulated independently of its phase [49]. This mode was widely used in early days for Hughes liquid crystal light valve (LCLV) [176]. Figure 3.10 shows the phase modulation of a twisted nematic liquid crystal operating in the reflective mode.

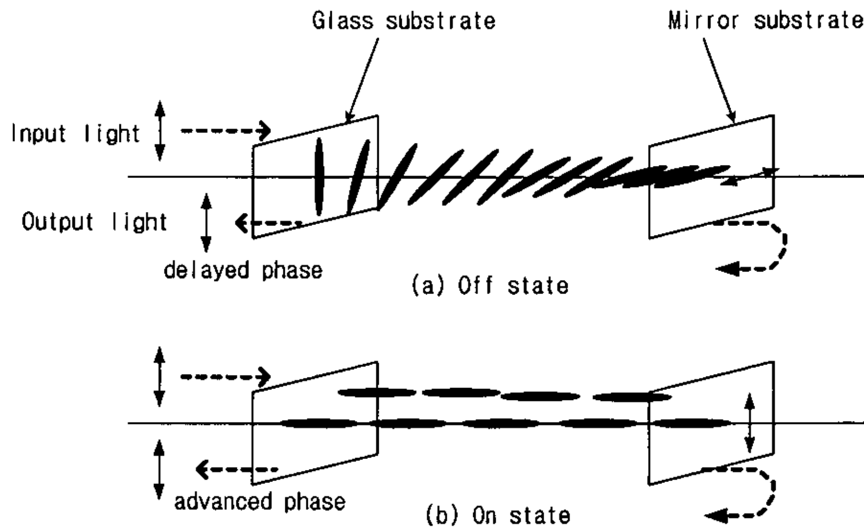


Fig. 3.10: Schematic cross section showing mechanism for phase modulation of a reflective SLM when twisted mode NLC is used. (a) delayed phase of the light output (b) advanced phase of the light output.

In the off state, the polarization direction of vertically polarized light transmitted and reflected through the device occurs with LC molecules aligned in a helix between the substrates. In the on state, the LC molecules are tilted in accordance with the electric field. In a transmissive SLM this changes not only the phase of the light but also the polarization state at the output. The polarization changes are normally undesirable in

many optical applications. To avoid this problem, parallel-aligned liquid crystal SLMs are preferred for use in these applications [50].

3.4 Electro-optical effects in ferroelectric liquid crystals

LC molecules in chiral smectic C materials (SmC*) exhibit a spontaneous polarization (P_s), and create a helical structure with the pitch being the distance required for the molecular director to rotate by 360° as shown in Fig. 3.3. As the spontaneous polarization (P_s) is directed along the layer plane and perpendicular to the molecular director, the polarization vectors will be at a tangent to the circle of intersection with the plane. The amplitude of the P_s is dependent on the rotational order of the molecules, and the sign on the direction of tilt of the molecules [52]. The molecules within each smectic layer would be in alignment with each other. Thus each layer in SmC* phase can exhibit ferroelectricity [51]. These ferroelectric materials respond very quickly to an applied electric field, and are of interest for electro-optical devices.

However, there are no ferroelectric domains in the bulk samples as the spontaneous polarisation will macroscopically average out to zero, because the polarisation vectors traverse an entire circle.

The ferroelectric effects utilizing Clark-Lagerwall mode, deformed helix mode, soft mode and antiferroelectric mode are investigated in the following sections.

3.4.1 Clark-Lagerwall effect

Clark and Lagerwall produced surface stabilised FLCs by suppressing the dipole induced helix by constraining the LC in a cell gap that is less than the helical pitch [53]. By anchoring the molecules in contact with the alignment layers in thin cells (normally 1~3μm) with the smectic layers running perpendicularly between them, the chiral rotation will be suppressed by surface anchoring energy and unwound by the walls. The directors in the cell can adopt only one of two states determined by the

alignment of cell surfaces. Thus the spontaneous polarisation is not averaged out from layer to layer, and hence the phase becomes ferroelectric. This is called surface stabilised ferroelectric liquid crystal (SSFLC) structure (see Fig. 3.11). This also makes the FLC cell a uniaxial phase plate.

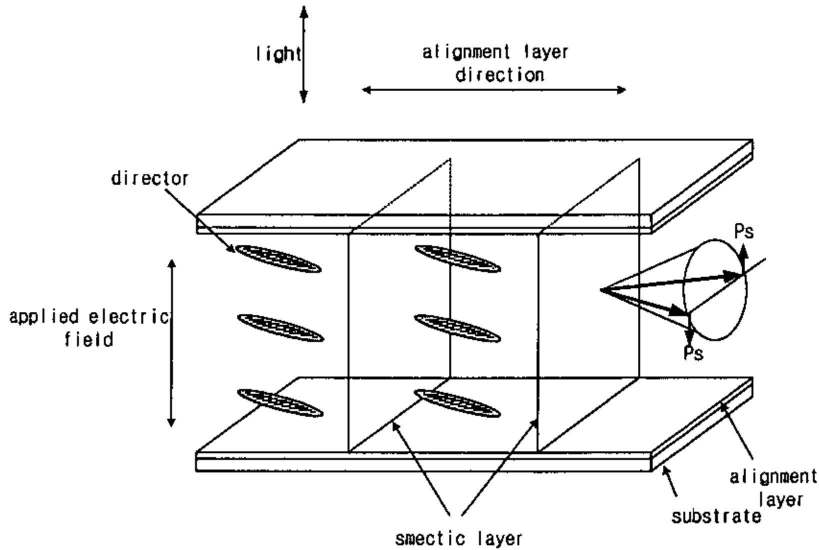


Fig. 3.11: Schematic diagram of SSFLC cell, showing the two stable FLC molecular orientation

When one of the FLC molecular axes is parallel to one of the crossed polarizer axes, the maximum transmitted intensity can be achieved. The optical transmission can be defined as [54]:

$$I = I_0 \sin^2 4\theta \sin^2(\pi \Delta n d / \lambda) \tag{3.6}$$

where I_o is the incident intensity, θ is the tilt angle of the mixture, Δn is the optical anisotropy of the medium, d is the cell thickness, and λ is the wavelength of the light. When the tilt angle $\theta = 22.5°$, there will be maximum transmission contrast between two states.

SSFLC cells have a threshold voltage at approximately 0.1V. Switching time is of the order of tens of microseconds as opposed to several milliseconds for nematic

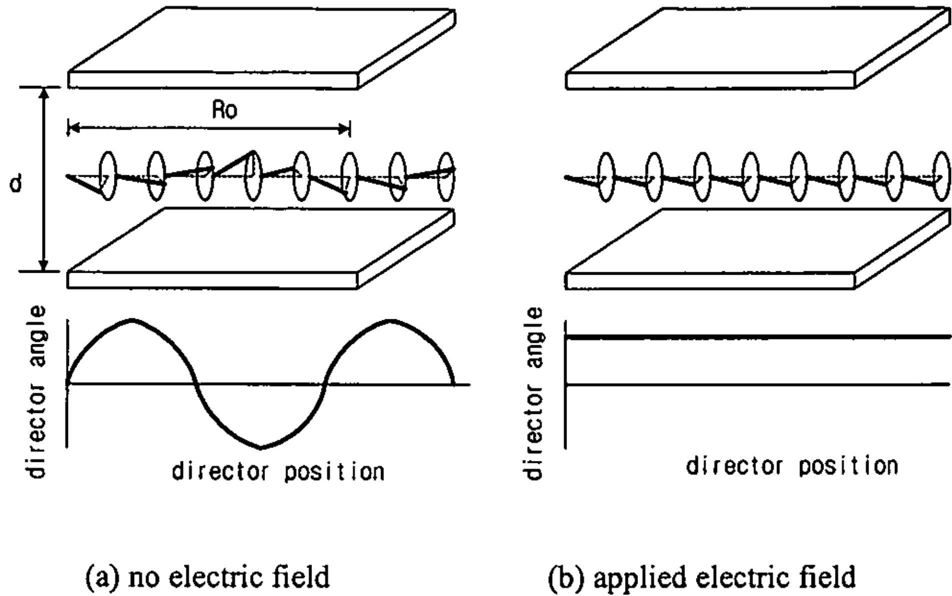
cells. The reason for the fast switching is that the torque on the FLC director is proportional to spontaneous polarisation and the electric field. Clearly, fast switching time can be obtained with low rotational viscosity and high spontaneous polarisation, and the switching time decreases as the electric field increases. In general, both spontaneous polarisation and rotational viscosity decrease with increasing temperature, and the net effect is that fast switching speeds can be achieved at high LC temperature [55].

The SSFLC structure can be applied to LCoS devices, which are fast (about 30μs), bistable and have the advantage of using digital Si backplanes. However, it requires strict cell-gap control, DC-balanced driving, digital grey scale and a large peak current to switch the spontaneous polarization.

3.4.2 Deformed helix ferroelectric effect

When the FLC layers are perpendicular to the substrates and the thickness of the layer d is much greater than the helix pitch R_0 ($R_0 << \lambda$), the DHF effect can be achieved in the smectic C* phase [56]. The FLC helical structure deforms with an electrical field so that the directors oscillate symmetrically in $\pm E$ electric fields.

The operational principle of the DHF cell is shown in Fig. 3.12. When there is no applied electric field, the molecular director varies sinusoidally as a function of position. If an electric field is applied then the helix is gradually unwound as the dipoles rotate to align with the applied field across the cell. This structure is very unstable to achieve the surface treatment and less sensitive to the cell gap adjustment than the SSFLC [57]. The DHF effect allows analogue grayscale with voltage and high switching time (250μs) with 1~2V driving voltages [58]. However it is difficult to use the DHF effect for analogue grayscale due to scattering.



(a) no electric field (b) applied electric field

Fig. 3.12: Configuration of molecular directors in DHFLCs. (a) the molecular director angle varies sinusoidally as a function of position parallel to the boundary substrates. R_0 is the helix pitch which represents one period of the helix. (b) the molecular director angle is uniform as the helix is unwound.

3.4.3 Soft-mode effect

Soft-mode effect can be obtained in smectic A* liquid crystals, which are usually produced by heating smectic C* above a phase transition temperature Tc [59]. The term soft-mode arises because one of the elastic constants vanishes as the liquid crystal is cooled through Tc, softening the restoring force which keeps the molecules perpendicular to the smectic layers.

The geometry of the soft-mode FLC cell is shown in Fig. 3.13. The tilt angle θ in the smectic A phase is linearly related to the electric field E [82],

$$\theta = \mu E / \alpha (T - T_c) \tag{3.7}$$

where μ and α are material constants and $T - Tc$ is the temperature above the $S_C{}^*$-S_A transition. The tilt angle is linearly increased with increasing electric field. The optical transmission is defined as [60]:

$$I = \sin^2 2(\Psi_0 + \theta(E)) \tag{3.8}$$

where $\Psi_0 + \theta(E)$ is the angle between the polarizer and the director projection on the substrate plane. The switching time is approximately $1\,\mu s$ for the voltage range of 10-40V, which is more than 10 times faster than SSFLC. The soft mode also provides linear grayscale as the tilt angle is a linear function of the applied electric field, hence analogue optical modulation can be achieved [61] [62]. The problems of soft mode FLC are its temperature dependence and small modulation tilt angle.

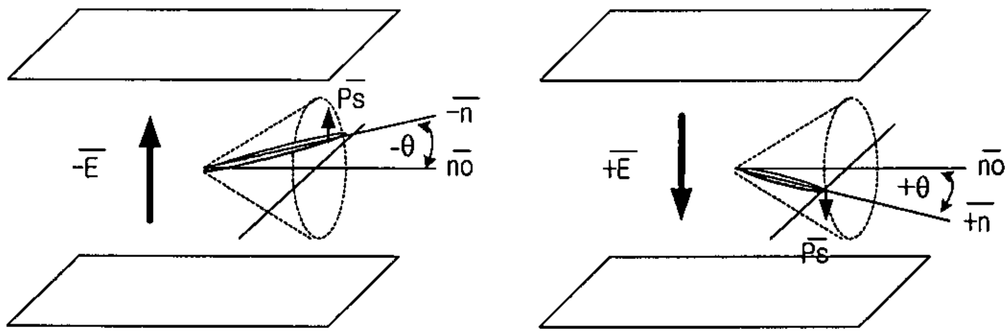


Fig. 3.13: The deviation of director in soft mode LC. (θ is tilt angle, P_s is spontaneous polarisation, n_0 is the axis of middle point of two director positions ±n)

3.4.4 Antiferroelectric LCs

Antiferroelectric liquid crystals (AFLCs) create optimum optical switching by using a phase transition from the antiferroelectric phase to the ferroelectric phase, which is caused by an electric field. In AFLCs, the third state appears at zero electric field, in addition to the two stable up and down states [63]. In this antiferroelectric state, the average macroscopic polarization equals zero both for the helical and unwound structures, resulting in a "dark" state. In the ferroelectric state when an electric field

is applied, the optical axis tilts and causes double refraction, resulting in a "bright" state. The geometry and operation of an AFLC cell with crossed polarizers is shown in Fig. 3.14.

The AFLC device has the advantage of analogue greyscale with fast switching (50μs), contrast ratio of 30:1, and large viewing angle due to its in-plane switching. The other advantage is that AFLC material does not need timing for DC balancing since it produces a bright state both in a positive and negative electric field. However, AFLCs need further improvements in terms of stability, temperature range, size of the spontaneous polarization and alignment for practical applications. The electro-optical properties of AFLCs are modelled using an electronic circuit [64] and the AFLC material characterization for reflective CMOS backplanes has been done by Lu *et al.* [65].

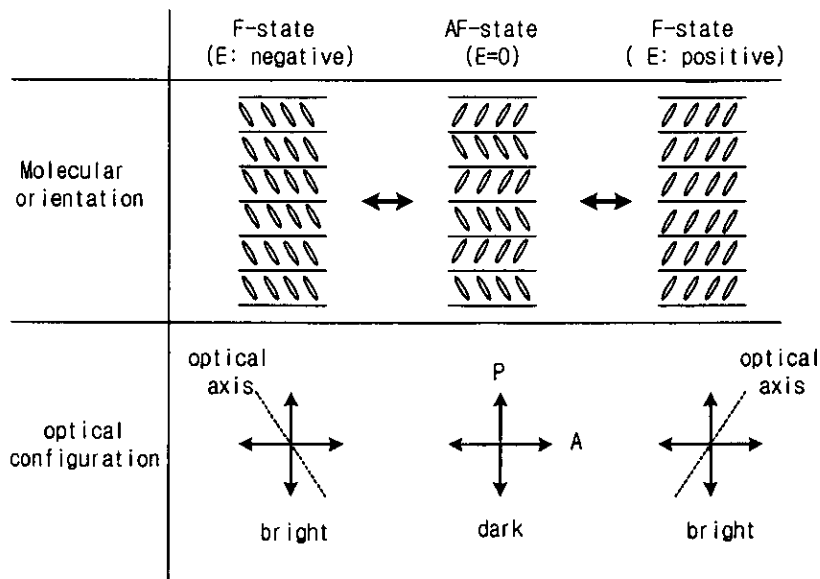


Fig. 3.14: Geometry and operation of an AFLC cell between crossed polarizers [66]

3.4.5 Discussion of FLC devices

A summary of the FLC modulator characteristics discussed in this chapter is shown in Table 3.1. DHF material works in analogue mode with very low voltage but shows low contrast. Soft-mode material has a fast switching time, but it is temperature dependent and shows modest tilt. AFLC material offers a simple structure with a wide viewing angle, but still needs further improvement in terms of stability, operating temperature range, and alignment. Although a number of the other types of FLC materials have been examined, the most suitable FLC material for LCoS devices is found to be the SSFLC in terms of binary switching mode, fast switching and high contrast. The detailed SSFLC characteristics will be discussed in the next section.

	SSFLC	DHF	Soft mode	AFLC
Applying voltage (V)	3~30	1~5	10~40	1~5
Switching time (μs)	20~30	100~250	1~5	50
Contrast	100:1	30:1	2:1	30:1
Modulation mode	Binary	Analogue	Analogue	Analogue

Table 3.1: Characteristics of FLC devices

3.5 Characteristics of SSFLCs

The molecular orientations of SSFLC devices are classified by two layer structures: a bookshelf layer and a chevron layer.

3.5.1 Bookshelf structure

SSFLC devices are normally formed between two glass substrates spaced closer than the ferroelectric helix pitch (2~5μm). The cell surfaces are treated to cause the molecular axis to align parallel to the cell surfaces which results in smectic layers arranged perpendicular to the substrates as shown in Fig.3.15. This is called a "bookshelf structure" and is the simplest and most preferable geometry for SSFLC

devices [67]. The molecules are constrained to move about a tilt cone and have two stable positions, separated by an angle 2θ (twice the cone angle).

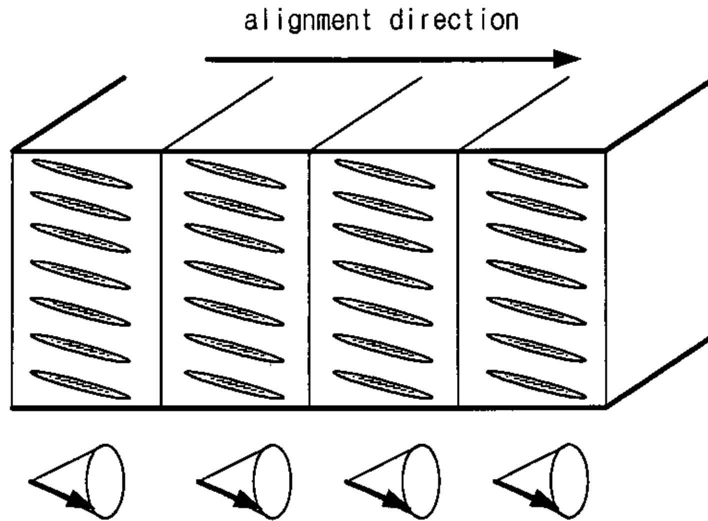


Fig. 3.15: Bookshelf structure, showing molecular director position in each smectic layers

The surface anchoring of the molecules tries to impose the constraint that all directors in a layer are parallel, so every vertical layer has the same molecular orientation, and a spontaneous polarisation appears across the cell. The spontaneous polarisation (P_s) varies from the order of one to hundreds of $nCcm^{-2}$. The switching charge requirement for an area and thickness of a FLC cell defines the optimal electrical interface to it. With DC bias, FLC dipoles align with the electric field and when the applied electric field reverses, the dipoles follow the electric field hindered by viscosity. A switching charge Q_{sw} is required to reverse the dipoles in a FLC cell which is used in the design of backplane pixels for LCoS devices.

$$Q_{sw} = 2A \cdot P_s \tag{3.9}$$

where A is cell area and P_s is spontaneous polarisation. The switching charge Q_{sw} should be applied to a pixel by a matrix of CMOS switches, the charge being stored by the pixel capacitance.

It is known that six possible states of director configuration exist in a bookshelf structure as shown in Fig. 3.16 [68]. Two uniform states give extinction when observed in a polarizing microscope and the four other splayed states do not extinguish between crossed polarizers, as the rotated optical axis between two substrates guides the polarization of light like a twisted nematic material. However, these states do not explain the relaxation in effective optical axis rotation after the electric field is removed [69].

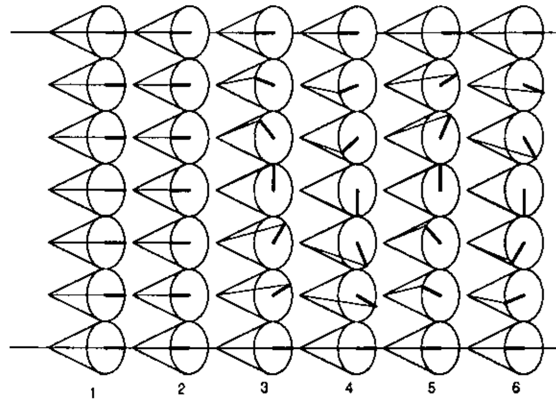


Fig 3.16: The six states of director configuration in a bookshelf structure (column 1 and 2 show uniform states, and column 3, 4, 5 and 6 show splayed states)

The concept of pre-tilt angle was added to the above model, where the azimuthal angle of rotation of the optic axis around the smectic cone is offset by a pre-tilt angle of α at the cell surfaces [70]. The surface pre-tilt angle is determined by alignment materials and treatments. The projection of the molecular director on the cell plane is shown in Fig.3.17. The position of the director can be switched back and forth by application of different polarity voltages.

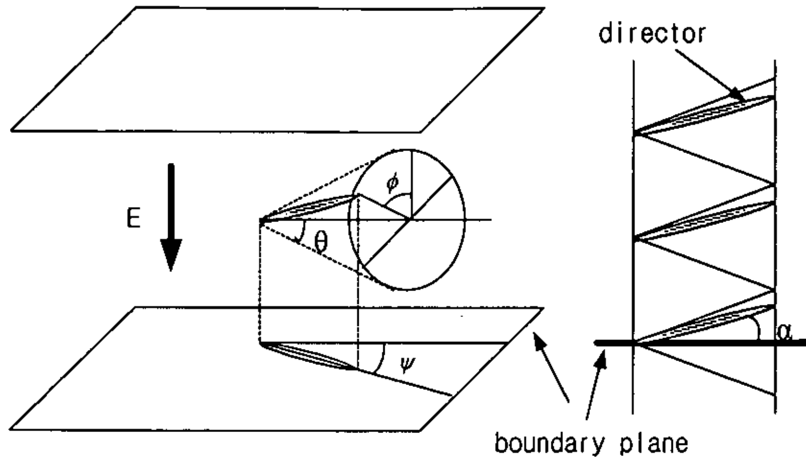


Fig. 3.17: Position of a molecular director on a cone with a pre-tilt angle α, and the projection of the director angle ψ onto the cell boundary plane.

As the director rotates around its cone in the surface stabilised bookshelf structure, the projection of the director angle ψ on the plane of cell from the alignment direction is given by:

$$\tan \psi = \sin \phi \tan \theta \tag{3.10}$$

where ϕ is the angle of the director around the cone, and θ is the cone angle.

The molecules rotate together and surface effects are related to an elastic force. The dynamics of the FLC material obeys the viscous elastic equation [71] [72] in terms of the angle of the director round the cone:

$$\gamma \frac{d\phi}{dt} = P_S E \cos \phi + K(\phi) \tag{3.11}$$

where γ is the rotational viscosity, P_S is the spontaneous polarisation, E is the applied electric field, ϕ is the angle of the director around the cone, and $K(\phi)$ is the elastic force.

Depending on the material, cell thickness, and temperature, values of P_S, γ, $K(\phi)$ and θ will vary [73]. In particular, the elastic force $K(\phi)$ is dependent on the thickness of the cell layer. The elastic force at the alignment surface moves the director to one of the bi-stable positions around the cone, and the column of molecules in the bulk of the liquid crystal above it will be aligned in the same direction. The FLC molecules can only be moved over an energy barrier between one stable position to the other by an external force, which is provided by the electric field and spontaneous polarisation. This bookshelf structure can provide a large initial torque due to the effective angle between the polarisation direction and the electric field direction, but this structure reduces its switching angle (2Ψ).

The bookshelf structure is known to be difficult to achieve because the molecules at the surface of the anchoring layers are unlikely to be exactly parallel to the surface, and any pre-tilt angle on the surface alignment layer will move them around the surface of the cone. However, a quasi-bookshelf structure can be achieved by applying an AC electric field [74].

3.5.2 Chevron structure

It has been known that SSFLC structures were usually far more complex than the originally proposed bookshelf structure. In general, chevron structures are the most usual configurations obtained with current FLC materials and surface treatments. The chevron structure (see Fig.3.18) can be observed when a cell filled with smectic A material is cooled into the smectic C* phase [75] [76]. Once the layers are formed in the smectic A phase, the surface positional anchoring is frozen and the layers do not move along the surface plates. As the cell is further cooled during formation of the smectic C* phase the layers want to become thinner which results in tilting the layer. The non-shrinkage of smectic layer thickness due to the tilt of the molecules creates undesired chevron structures from bookshelf layers [77]. The periodicity of the LC material at the alignment surface is maintained, and the interface where the two

oppositely tilted molecules meet is parallel to the substrates. The layer tilt is normally 2~3° less than the cone angle at room temperature [78].

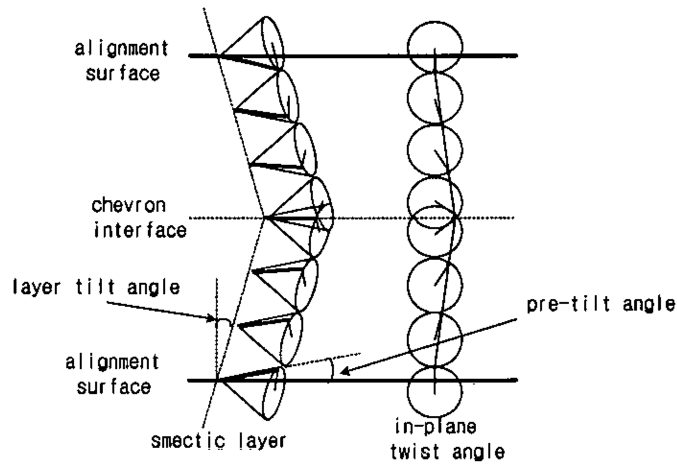


Fig 3.18: Chevron structure

The chevron structure can be classified into C1 and C2 states [79] [80], as shown in Fig.3.19, based on the relationship between the direction of the chevron layer structure and the direction of the pre-tilt of the LC molecules on the alignment surface.

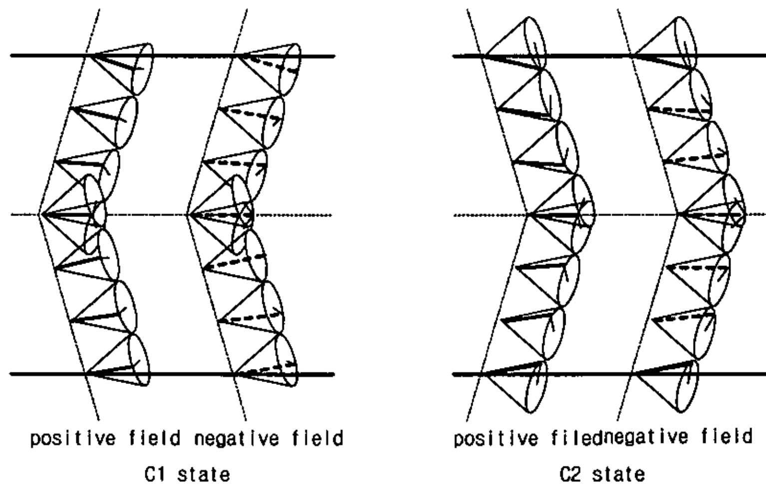


Fig.3.19: C1 and C2 state in chevron structure

In the C1 state, molecular directors are tilted to one side of the smectic layer normal. In the C2 state, the director at the alignment surfaces is almost perpendicular to the

surface plane. The C1 and C2 state can be easily determined by the direction of the chevron layer, confirmed by the direction of the pre-tilt which is consistent with the rubbing direction. If $\theta + \delta > \alpha$ the C1 state will be formed, where θ is the cone angle, δ is the layer tilt angle, and α is the pre-tilt angle. On the other hand, if $\theta - \delta > \alpha$ the C2 state will be allowed. This indicates that when the C2 condition is met, the C1 condition will also hold, by forming so-called zigzag defects. Thus, a uniform C1 state has been obtained by introducing a high pre-tilt angle alignment [81].

The zigzag defect, a mismatch of the bent direction in smectic layers, originates in the C1-C2 chevron structure transformation [76][83]. The chevron-structural transformation from C1 to C2 usually occurs in a cooling process. If this transformation cannot progress smoothly and uniformly, C1 and C2 structures coexist, forming zigzag defects. It is also known that the uniform C1 chevron structure can be achieved in a SSFLC cell without zigzag defects, by introducing weak-surface anchoring alignment.

Figure 3.20 shows the tilted bistable director position, at the plane of alignment surface in the chevron structure C1 state. The cone angle θ and layer tilt angle δ are assumed to be constant. For the C2 state, the layer tilt angle should be of opposite sign. The bistable states of the molecular director when projected onto the cell surface, appear to be smaller than twice the cone angle. From the chevron structure (C1) geometry in Fig. 3.20, the projected director angle ψ_S in its stable position is specified as in equation (3.12), whose values depend on the cone angle θ and chevron tilt angle δ:

$$\cos \psi_S = \frac{\cos \theta}{\cos \delta} \tag{3.12}$$

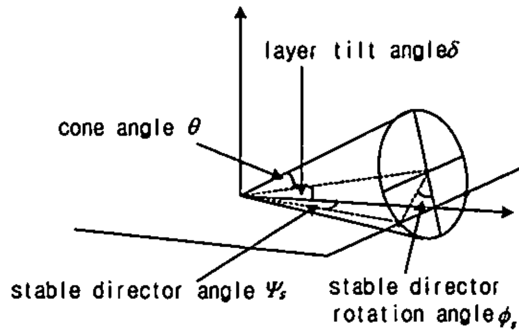


Fig.3.20: Geometry of the director position in a chevron structure (C1 state)

The director at the surface is inclined with respect to the cell plane at an angle $\pm\phi_s$. As the director tilts away from the cell plane, there are two distinct stable director states with the same free energy. These bistable states are very important for use in optical applications. Figure 3.21 shows the FLC free energy as a function of the azimuthal angle ϕ. There are two stable positions at $+\phi_s$ and $-\phi_s$ (with an energy barrier between them) where the molecular energy is minimized for LC orientations parallel to $+\phi_s$ and $-\phi_s$. The elastic force $K(\phi)$ tends to push the molecules back to the stable positions. The energy barrier becomes lower and the two stable positions come closer to each other if a chevron structure has a higher layer tilt angle, which indicates that the decrease of the layer tilt angle in a chevron structure induces the increase of the surface energy barrier [84] [85]. This implies that a bookshelf structure (layer tilt angle = 0°) has the highest energy barrier and stable positions at ϕ = -90° or ϕ = 90°.

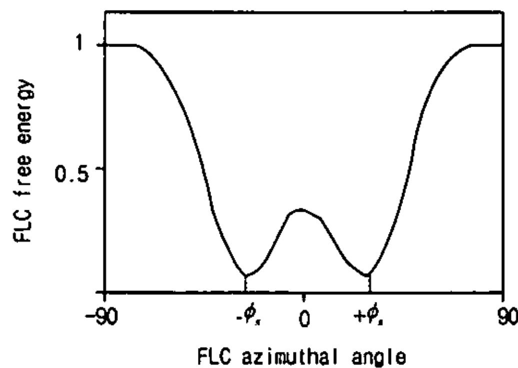


Fig. 3.21: Free energy of a FLC bounded at a surface as a function of the azimuthal angle ϕ

From the geometry in Fig. 3.20, the angle (ϕ_S) between the directors of the stable states rotated about the circular face of the cone is specified as:

$$\cos\phi_S = \frac{\tan\delta}{\tan\theta} \tag{3.13}$$

In this chevron structure, the viscous elastic equation (3.11) is also changed to [84]:

$$\gamma\frac{d\phi}{dt} = P_s\, E\, \cos\,\phi\, \cos\delta + K(\phi) \tag{3.14}$$

As the applied electric field increases, the FLC directors can be rotated further round the cone and the switching angle can be increased towards its extreme cone position. If the applied field is removed, the directors will be returned to the stable position in the chevron structure by a strong restoring force, at a rate dependent on the rotational viscosity and the elastic force. When the switching angle is greater than the bistable position angle, it represents the average director angle observed on the cell surface. The switching angle ψ of the director, projected onto the surface plane that varies with the rotation angle ϕ around the cone, is defined as [84] [152] [153]:

$$\tan\,\psi = \frac{\sin\,\theta\,\sin\,\phi}{\cos\,\theta\,\cos\delta + \sin\,\theta\cos\,\phi\,\sin\,\delta} \tag{3.15}$$

3.6 Alignment techniques

In this section, we present a brief review on techniques for the molecular alignment of liquid crystals. Firstly, we describe the surface alignment of a liquid crystal on a solid substrate and then we compare techniques that have been proposed for aligning liquid crystals. Finally we discuss which technique is the most appropriate for this study.

When in contact with a solid phase surface, rod-like liquid crystal molecules will anchor on the surface with certain orientation due to some interaction at the interface between the two phases: homogeneous and homeotropic alignment. The homogeneous and homeotropic alignments are determined by the relative magnitude of the surface free energy of the liquid crystal γ_L and the surface free energy of the solid substrate γ_S [86]. The difference

$$\Delta\gamma = \gamma_L - \gamma_S \tag{3.16}$$

is a measure of the free energy favouring liquid crystal molecular orientation normal to a surface over orientation parallel to a surface. Homeotropic alignment occurs when the condition is $\Delta\gamma > 0$ and homogeneous alignment occurs when the condition is $\Delta\gamma < 0$. For the purposes of this study only homogeneous alignment will be considered.

Depending upon the treatment on the surface of the substrate, the alignment techniques can be divided into two categories: contact or non-contact techniques (see Table 3.2). In the contact technique, mechanical rubbing is typical: the substrate is covered with a layer of polymer and rubbed in one direction. There are many different non-contact techniques such as oblique deposition of SiO layer, the deposition of Langmuir-Blodgett films, field induced molecular alignment, and the photo-modification of polymers using polarized UV light.

Technique	Advantages	Disadvantages
polymer film rubbing [87] [88]	- simple process (low cost) - easily applicable to large areas	- particle contamination - static charge - scratches reduce contrast ratio
oblique deposition of SiO [89] [90]	- non contact process - applicable even with a high temperature process - the pretilt angle can be changed widely	- long process time - complicated process - difficult to cover a large area display
Photo alignment [91] - [93]	- non contact process (particle free) - simple process	- need further research on thermal stability and electro-optics
Langmuir-Blodgett films [94] [95]	- non contacting process	- short circuit problem - difficult to cover large area
Field induced molecular alignment [96] [97]	- non contacting process	- the use of high magnetic field

Table 3.2: Comparison between various alignment techniques

The alignment techniques change the surface properties of the polyimide in such a way that it anchors the liquid crystal molecules in a certain orientation. For electrooptical bistable switching, SSFLCs need homogeneous alignment. A practical method to obtain homogeneous alignment for SSFLCs is mechanical rubbing, although finding the optimum rubbing conditions is difficult in terms of alignment uniformity, reproducibility and stability. The formation of homogeneous alignment in SSFLC requires weak anchoring, whilst nematic LC requires strong anchoring [98].

SSFLC alignment often shows unfavourable zig-zag defects of chevron structure because it's SmC* phases are difficult to form with a unique molecular axis. However, rubbing is not ideal for use in LCoS backplane, since the small particles generated from the rubbing process cause multi-pixel defects and the electrostatic discharge can damage the LCoS backplane.

Non-contact alignment techniques are preferable for alignment of LCoS displays. Photo-alignment is considered a promising candidate for replacing the rubbing technique as it does not lead to the particle contamination and simplifies the alignment process. However, the photo-alignment technique requires further research on thermal stability and electro-optical properties, which is outside the scope of this study. Obliquely evaporated films of SiO would seem to be the most suitable for the following study because this non-contact process is well established and it is easy to control LC pretilt angle.

3.7 Summary and Discussion

There are three different phases of liquid crystals that have useful optical properties: nematic, cholesteric, and smectic. In a nematic liquid crystal the molecules tend to be parallel but their positions are random. The preferred molecular orientation is called the director **n**, and the nematic phase is symmetric about ±**n** providing uniaxial optical properties. When the constituent molecules of a nematic liquid crystal are chiral they vary in a cyclical manner with location, and the phase is called cholesteric. The order of the cholesteric phase is periodic with a spatial period derived from the pitch of the helix. The molecules of the smectic phase are also parallel but their centres are stacked in parallel layers, within which they are randomly located.

Nematic LCs have considerable advantages for use in LCoS devices, as switchable and tuneable uniaxial birefringent slabs whose optical axis is fixed but whose birefringence is a function of the applied voltage. However, the response of nematic LCs requires improvement because LCoS devices are operated at low voltage

provided by CMOS circuitry. This can be achieved by using a material with higher dielectric anisotropy or lower viscosity. Applied electric field will result in a change in the birefringence of the LC device, causing a change in the retardance of the LC device. Thus, Nematic LCs are good for applications when a large phase modulation is required. Nematic LCs are also capable of continuous phase shift with response to an applied field, which is useful in the application of multilevel phase modulation discussed in a later chapter.

Several different FLC modes were investigated for LCoS applications. SSFLCs can be used as an optical waveplate whose retardance is fixed, but the direction of optical axis is a function of the applied voltage. SSFLC devices have not only fast switching but also bistability which is advantageous for binary phase modulation and/or using digital Si backplane. However, the uniform alignment of LCs, precise cell gap control, and DC-balanced driving are obstacles to practical use.

The SSFLC model has progressed from the bookshelf structure to the chevron structure with the addition of the pre-tilt concept. Now it is known that SSFLC cells have a chevron structure, with a kink in the middle of the cell. The chevron structure degrades the electrooptical properties of the device, because the effective switching angle becomes smaller than 2θ. The chevron layers can be formed with two opposite bends termed C1 and C2 states. If these two states coexist, the zigzag defects occur along the domain boundary between two oppositely bent layers, which degrades the electro-optical performance of FLC devices. Therefore, it is important to form the chevron structure with only uniformly oriented C1 or C2 state layers for zigzag defect-free FLC cells. In general, it is easier to get C1 layer structure than C2 structure.

The alignment of LCs can be achieved by a variety of techniques such as polymer film rubbing, oblique deposition of SiO, photo alignment, Langmuir-Blodgett films, and field induced molecular alignment. The most commonly used technique is polymer film rubbing. However, drawbacks of polymer film rubbing are generation

of dust, electrostatic charges and scratches on the alignment layers. Scratches are particularly serious when the pixel structures are as small as in LCoS devices. To avoid scratches, rubbing has to be done very gently, which however reduces surface anchoring of the LC to the substrate and therefore reduces the contrast ratio. Non-contact alignment techniques are preferable for LCoS devices.

Chapter 4:

Characterization of inter-metal dielectric deposition processes on CMOS backplanes for LCoS devices

4.1 Introduction

In an LCoS backplane, a highly planarised and smooth surface is very important to perform optical modulation. In many optical applications, LCoS devices use a coherent light source which is very sensitive to the flatness of the reflective surface. Figure 4.1 shows detailed cross-section diagram of an LCoS device with a planarised surface. However, there were some difficulties in applying a planarisation process caused by uneven topography on the silicon backplane at Edinburgh University. The surface of a standard silicon backplane, when it was received from a foundry, was not flat. The pixel circuitry causes topography that is too rough to use for LCoS devices. An example of this is shown in Fig. 4.2. The trenches in Fig. 4.2 have 10μm-length, 2μm-width and 2μm-depth.

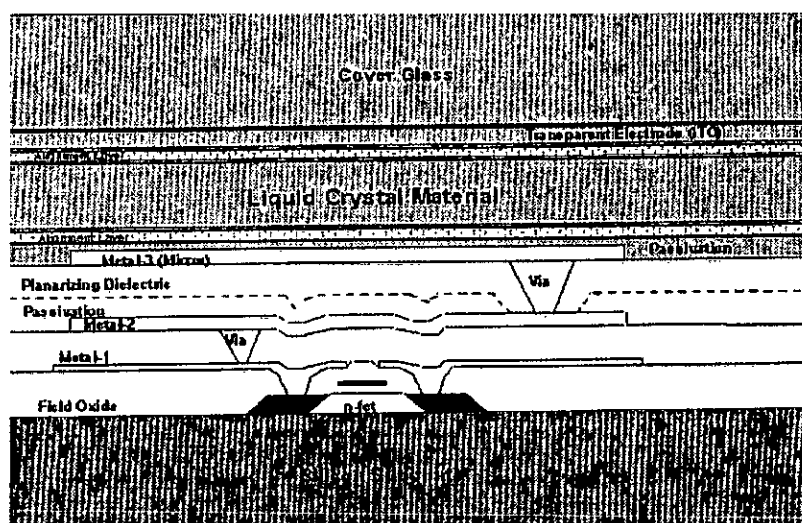


Fig. 4.1: A cross-section of an LCoS device [154]

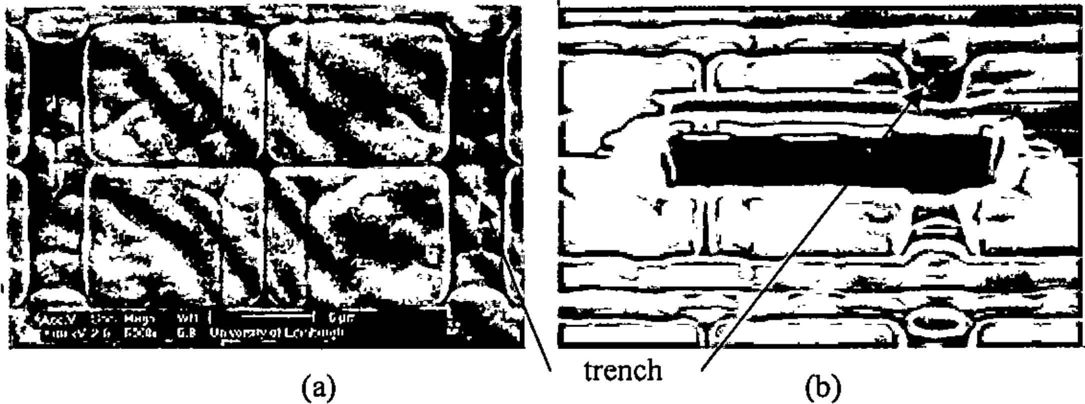


Fig. 4.2: The topography of a Si-backplane for an LCoS device (a) top view (b) cross section view

In order to use the pixel areas as light reflectors, planarisation is required to flatten the pixel layer that covers the underlying circuitry. This is a more difficult process than the typical insulator chemical mechanical polishing (CMP) step in a CMOS process, because the topography is bigger and the chip size larger than normal IC devices. However, various foundries can supply LCoS backplanes as a standard process now, with very flat backplanes and highly reflective pixels.

Deposition with a dielectric material such as SiO_2 or borophosphosilicate glass [99], and CMP planarisation are required to flatten the uneven topography of a Si-substrate [100]. After oxide deposition, the oxide film is polished back in the CMP process, leaving a 0.5 - 1μm-thick layer above the uppermost CMOS metal layer. If voids in the oxide are located at a higher position than the top CMOS metal layer before the polishing process, there is the likelihood of exposing the voids during the CMP process. Figure 4.3 shows the case of exposed voids during a CMP process in Edinburgh University. The voids in the oxide cause not only a reliability problem with the possibility of trapped chemicals in the void but can also cause breaks or shorting in bus lines in the underlying CMOS metal layer [101].

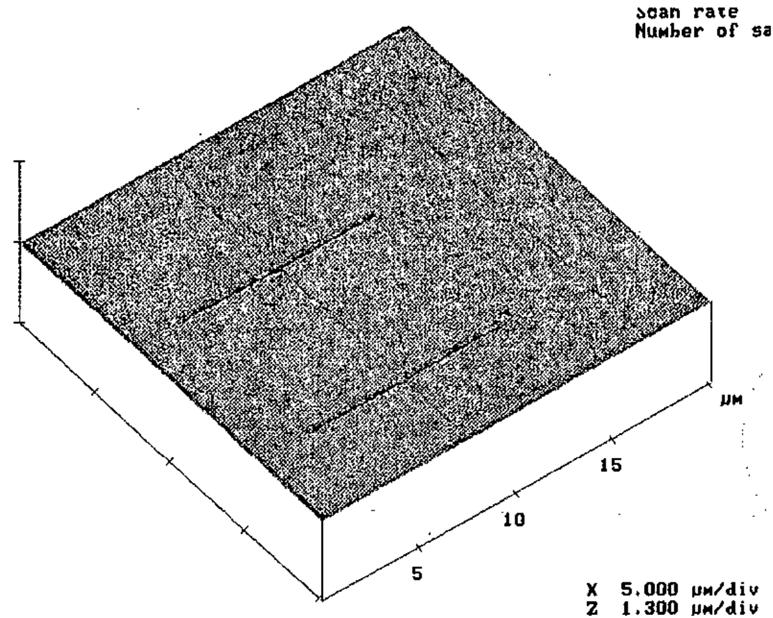


Fig. 4.3: Atomic Force Microscope image of exposed voids in a CMP process

Chemical vapor deposition (CVD) is a method of depositing thin films, used extensively in the microelectronics industry. Plasma–assisted CVD is a good method for dielectric films, which are subsequently subjected to CMP. It has the ability to fill small gaps, and the process can be done at a room temperature [102] [103]. Although the deposited film is not totally stress free it induces less stress than many other deposition techniques [104]. However, the deposition particles mainly have oblique incident angles to the substrate so that the intermediate oxide film cannot be deposited in the concave region of trenches as the aspect ratio nears to 1:1 [105]. Thus, it will become difficult to obtain a perfect planar structure for LCoS devices.

On the other hand, this planarisation problem can be avoided by an appropriate design of the deposition equipment. As will be shown later, trench filling problems occur in a certain range of trench aspect ratios and widths. In the chip design, however, one has to make compromises between pixel sizes and manufacturability regardless of a certain width and aspect ratio of a trench, which cause planarisation problems. Sometimes design rules are such that trench filling is going to be a problem. For example, the design rule in Edinburgh University for minimum gap in metal lines is 2 microns, so that for a typical feature height of 2 microns, the aspect ratio is unity. There are other processes (photolithography, underlying design, etc.)

that require this gap to be just this size. LCoS developers must recognize that semiconductor fabs are governed by certain design rules and defined processes. Therefore, design changes are not necessarily a solution to problems in LCoS unless they use a commercially available LCoS process.

For a successful trench-filling deposition, the deposition rate along the walls and at the bottom should be the same. However, the deposition rate is proportional to the arrival angle of the gas molecules if the absorbed reactants do not migrate predominantly along the surface and have short mean free path. This causes the different deposition rates between top and bottom of a trench. In this case, the arrival angle $\o$ is represented as

$$\o = \arctan(w/t), \tag{4.1}$$

where w is the width of the trench and t is the depth of the trench. The larger the arrival angle is, the higher is the deposition rate. Therefore, the film thickness will gradually decrease along the step wall and the deposit is thinnest at the bottom [101]. Furthermore, lateral growth near the tops of the trench close the gap before they are completely filled, leaving voids inside [106]. The step coverage of oxide which affects the gap-filling ratio can be changed by controlling CVD parameters such as rf bias, table height, magnet currents and plasma density in ECR CVD [107]-[111].

For effective planarisation, several deposition / CMP cycles are often required in order to fill the voids; this prolongs, complicates, and adds to the cost of the overall planarisation process. In order to reduce processing time and effort while still achieving extremely smooth surfaces, I investigated the trench-filling properties of oxide deposition processes on a microdisplay backplane to find the most suitable deposition technique.

4.2 Experimental

The trench-fill properties of two different types of oxides (pyrolytic CVD and ECR CVD) were investigated using a set of line-width test patterns. The oxide deposition techniques were evaluated and the most promising method was optimized.

A pyrolytic CVD system (Pacific Western PWS 2000) and an ECR CVD system (Oxford Plasma Technology AMR ECR system) were used to investigate trench-filling properties with SiO_2. Each of the processes has different variables that will affect the deposition properties as shown in Table 4.1. In a pyrolytic CVD process [112], there are three main variables: hot-plate speed, temperature and gas composition. The ECR-CVD process has five major variables: the magnetic field, microwave source, as well as the table height, chamber pressure and gas composition [113].

CVD techniques	Main parameters
Pyrolytic CVD	hot plate speed, hot plate temperature, gas composition
ECR-CVD	magnetic field (M1, M2), microwave source, table height, chamber pressure, gas composition

Table 4.1: List of parameters

4.2.1 Sample preparation

I used wafer samples that had a set of line-width trench patterns (1 - 6μm wide) etched into 4μm thick thermal oxide. The patterns were produced as follows. A 4-micron thick oxide layer was produced by thermal oxidation on a three-inch Si-substrate (Tempress Omega L furnace with 1100°C and 30 hours oxidation time). An aluminum (Al) layer was then deposited on the wafer in a sputter coater with 6kW DC power. The thickness of aluminum layer was 200 nm, and it is needed for the patterning on the wafers. The sputtered aluminum layer was used to mimic the top metal layer of the CMOS wafer as delivered from the foundry in real devices. The

aluminum layer also helps to distinguish the layers between thermal oxide and deposited oxide in the measurement. A simple array of lines and spaces was designed to produce the different aspect ratio of trench width and depth [114], covering a range of widths from 6μm to 1μm as shown in Fig. 4.4. After the photo-resist coating, a wafer stepper was used for printing the pattern on the photoresist-coated wafer. After the resist has been developed, two steps of dry etching were applied to remove the aluminum and the thermal oxide layer for producing trenches on the wafer. After the dry etch process, the photoresist was stripped from the wafer. The trench production process diagrams and process parameters are shown in Fig. 4.5 and Table 4.2, respectively.

After the trench-filling process, the wafers were characterized by a scanning electron microscope (SEM) to measure gap-filling ratios and deposition rates. The gap-filling ratio is defined as the proportion of the deposition rate at the bottom of a trench to the deposition rate at the top between trenches. The deposition rate is defined as the film thickness per specified period of time.

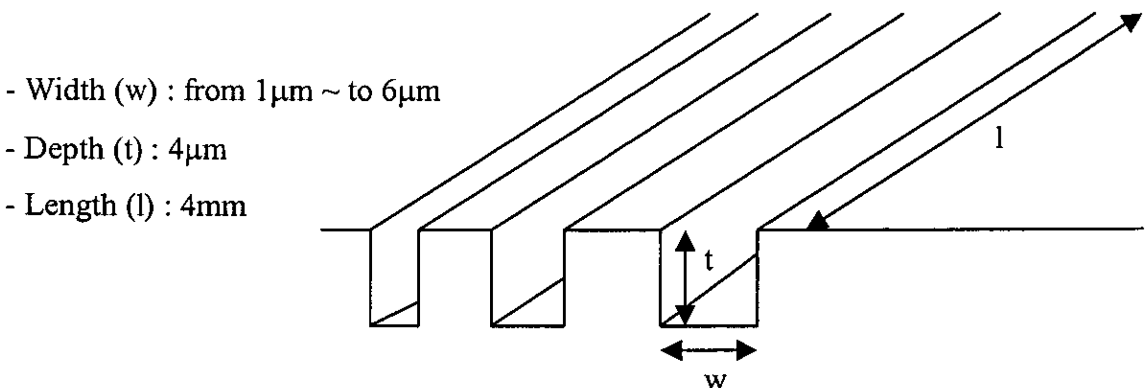


Fig. 4.4: Design of trench pattern

Processes	Process parameters	Equipment
1) Thermal oxidation on the Si-wafer	- thermal oxide thickness 4μm - furnace temperature 1100°C - time 30 hrs	Three quad stack Tempress Omega L furnaces
2) Al deposition	- Al thickness 200 nm - DC power 6 kW	Balzers BAS450 sputter-coater
3) photoresist coating	- photoresist type SPR 2 - spin speed 3300 RPM - spin duration 1 min - softbake temperature 110°C	SVG 8600 track system
4) pattern printing	- exposure time 2100 mS - focus +2.0	Optimetrix 8010 Wafer stteper
5) Al dry etching	- etching time 4 min	STS Multiplex load locked Al etcher
6) oxide dry etching	- etching time 146 min	Plasmatherm PK2440 RIE system
7) photoresist strip-off	- ashing time 60 min	STS PF 508 barrel reactor

Table 4.2: Process parameters of trench pattern production

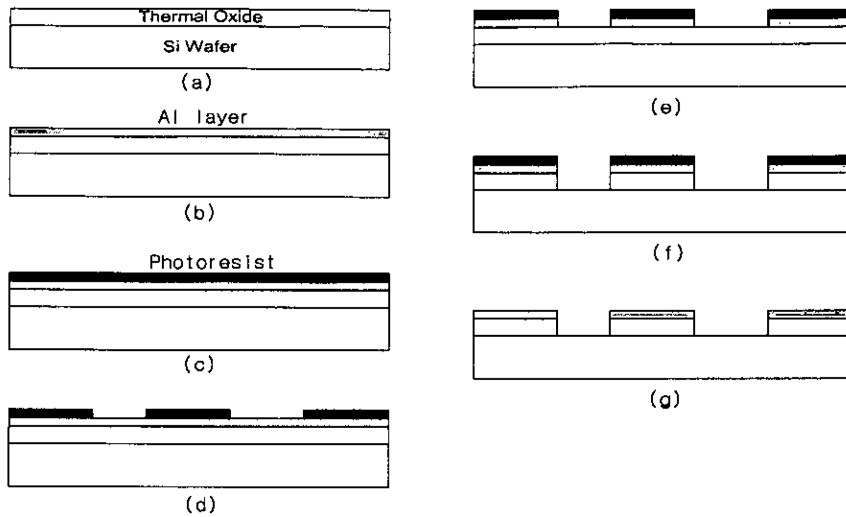
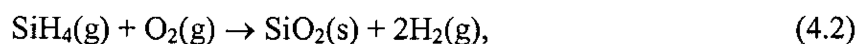


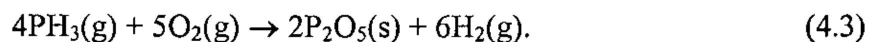
Fig. 4.5: Process diagram of trench patterns production
(a) Thermal oxidation (b) Al layer deposition (c) Photoresist coating (d) Patterning (e) Al dry-etching (f) Oxide dry-etching (g) photoresist removal

4.2.2 Parameter setting

The pyrolytic CVD system (Pacific Western PWS 2000) is a gas injection-type continuous-processing APCVD reactor and the schematic diagram of the system is shown in Fig. 4.6. Silane, phosphine and nitrogen are used as first reactant gases, and oxygen and nitrogen are used as second reactant gases. Normally, phosphine is added to prevent cracks on the surface of the deposited layer in the process. The chemical reactions are expressed as



$$SiH_4(g) + O_2(g) \rightarrow SiO_2(s) + 2H_2(g), \quad (4.2)$$



$$4PH_3(g) + 5O_2(g) \rightarrow 2P_2O_5(s) + 6H_2(g). \quad (4.3)$$

The major variables that could be controlled and that affect the film deposition range and uniformity are hot plate temperature and speed. When the hot plate temperature was below 400°C, the film uniformity was enormously decreased. The maximum hot plate temperature was limited to 430°C in the reactor. Therefore, hot plate temperature levels were determined to be between 400°C and 430°C. The mid-point was then set as 415°C. The hot plate speed was set to 100, 200 and 400, which

corresponds to 3.5 inch/min, 5.25 inch/min and 8.25 inch/min. All other input parameters were set to optimized values from existing deposition recipes for the equipment. One of the problems in this type of CVD is frequent need of reactor cleaning. The CVD system was cleaned with a vacuum cleaner every 15 to 20 runs to avoid any particle contamination.

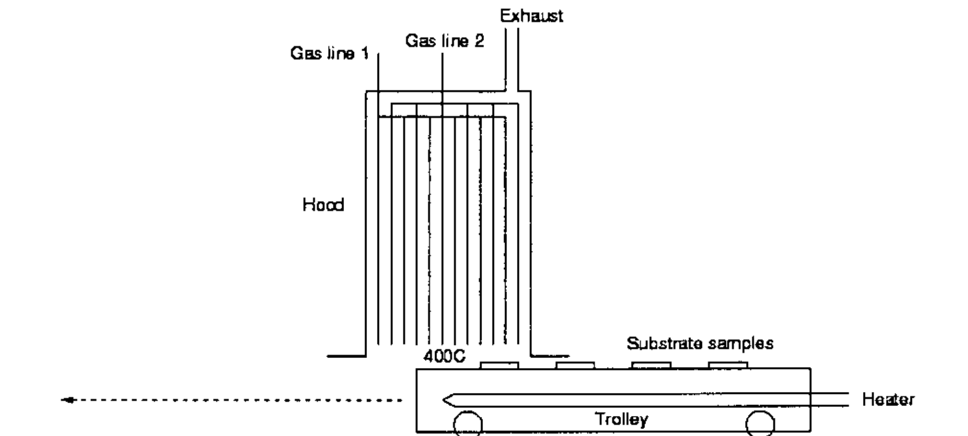
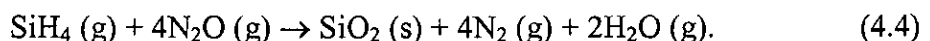


Fig. 4.6: Schematic diagram of pyrolytic oxide deposition system (Feedstock gas 1: N_2 4.0 l/min. + O_2 0.65 l/min., Feedstock gas 2: N_2 2.9 l/min. + 5% SiH_4 in N_2 1.3 l/min)

The ECR CVD process has been described elsewhere [106] [113]. A diagram of the ECR CVD system (Oxford Plasma Technology) is shown in Fig. 4.7. Microwave power (2.45 GHz) is introduced into the plasma chamber through a rectangular waveguide and magnets coils are set around the periphery of the plasma chamber for ECR plasma excitation. The specimen-table height can be changed from 0 mm to 100mm. The specimen-table height defines the distance from the extraction window of the plasma chamber (0 mm) to the specimen-table. The table temperature is maintained at 45°C - 50°C. The reactant gas mixtures are introduced through two separate inlets into the plasma chamber (N_2O) and the specimen chamber (SiH_4). Non-reactive Ar gas can be introduced through the plasma chamber inlet. By reacting silane and nitrous oxygen in plasma, silicon dioxide films are deposited. The reaction is expressed as



$$SiH_4\,(g) + 4N_2O\,(g) \rightarrow SiO_2\,(s) + 4N_2\,(g) + 2H_2O\,(g). \quad (4.4)$$

A DC bias voltage is applied to the table by a 13.6MHz RF generator through a matching circuit. Because the ECR CVD process is more complex and because of the limited time available, we have confined our study to five major variables: the magnetic field, DC bias voltage, the table height with respect to the extraction window, chamber pressure and gas composition.

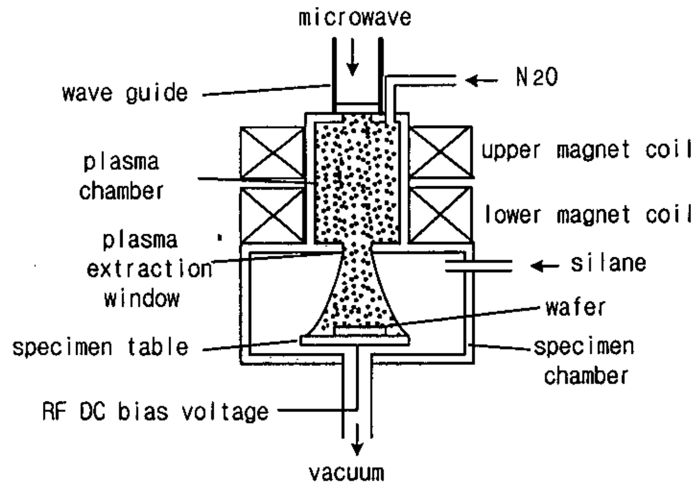


Fig. 4.7: Schematic diagram of the ECR CVD system

The parameter values of pyrolytic and ECR CVD are selected and the parameter level settings are shown in Table 4.3. The parameter space to be investigated was determined from known level settings.

CVD technique	Parameters	Initial conditions (Edinburgh Univ.)	Parameter level settings
pyrolytic CVD	hot-plate temperature	430°C	400°C, 415°C, 430°C
	hot plate speed	5.25in/min	3.5in/min, 5.25in/min, 8.25in/min
ECR-CVD	chamber pressure	4mT	1mT, 2mT, 4mT
	upper magnet current(M1)	100A	100A, 110A, 120A
	table height	100mm	30mm, 65mm, 100mm
	DC bias voltage	-200V	-200V, -300V, -400V
	Ar gas rate	0sccm	0sccm, 50sccm, 100sccm
	reactant gas flow rate*	normal flow rate	normal flow rate, half flow rate

Table 4.3: Parameters setting of pyrolytic and ECR CVD
(* normal flow rate: N_2O:35sccm SiH_4/He :100sccm,
half flow rate: N_2O:17.5sccm SiH_4/He :50sccm)

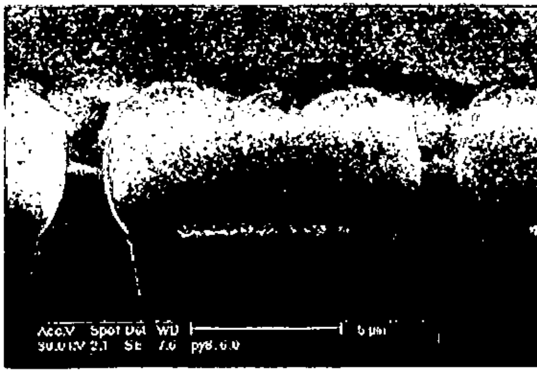
4.3 Comparison of the gap-filling capability

I varied the chosen parameters in both pyrolytic deposition and ECR CVD process to obtain the optimum conditions for trench filling. The thickness of filling oxide deposited was 3.8µm – 4.4µm as measured by a Nanospec spectro-reflectometer. A scanning electron microscope (SEM) was used to view the trench cross-section and to measure the trench-filling ratio and deposition rate. As shown in Fig.4.10, the trench-filling ratio (R) is defined as

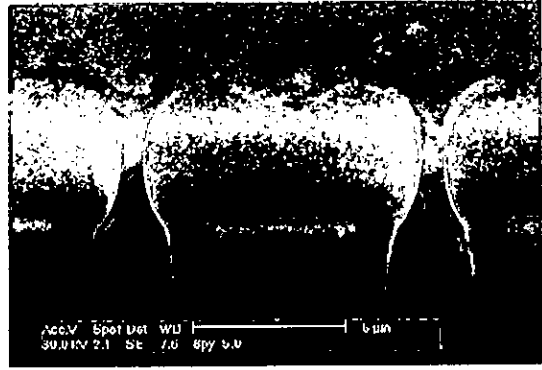
$$R = \frac{D_b}{D_t}, \tag{4.5}$$

where D_b is the deposition thickness of filling oxide at the bottom of a trench and D_t is the deposition thickness of filling oxide at the top of trench.

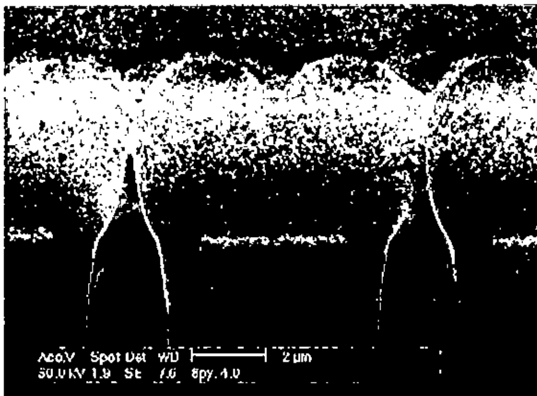
Figure 4.8 and Figure 4.9 compare cross-sections from both processes, in which the pyrolytic CVD sample exhibited a lower trench-filling ratio because the gap at the top of the trench had pinched off early in the process while the gap in the ECR CVD sample remained open during the deposition of ~4μm oxide.



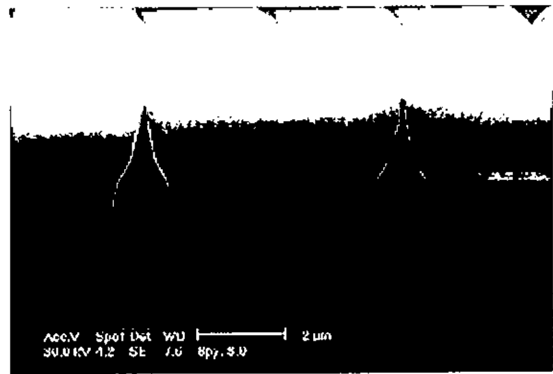
a) 6 µm-trench width



b) 5µm-trench width

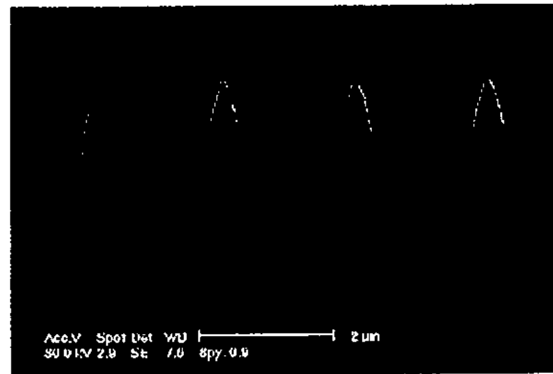


c) 4 µm-trench width



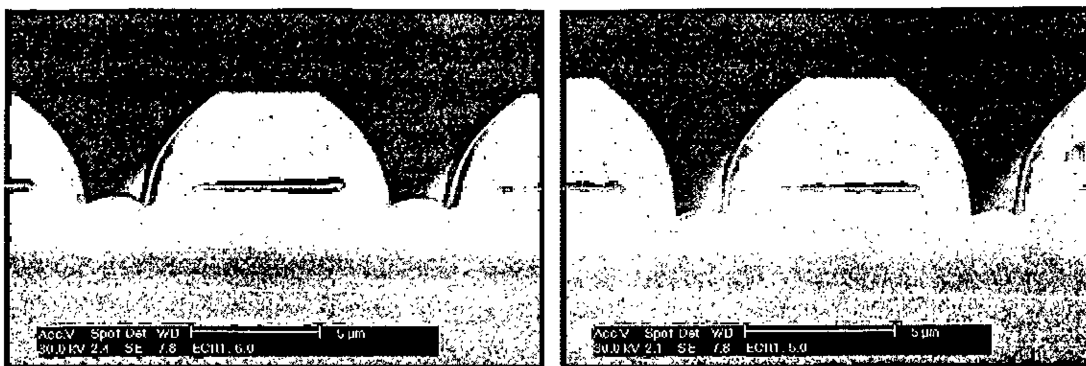
d) 3µm-trench width

e) 2 µm-trench width

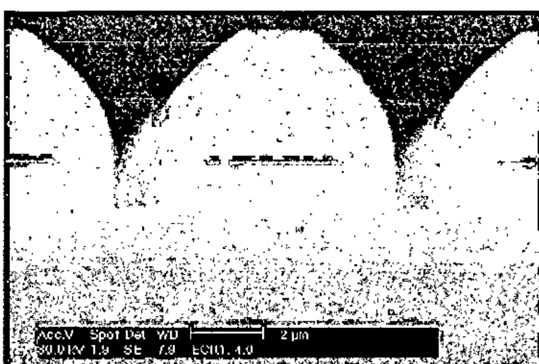


f) 1µm-trench width

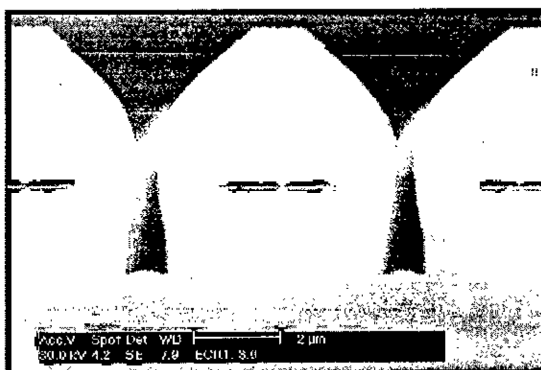
Fig. 4.8: SEM cross-sections of pyrolytic oxide deposition at different trench width (at temperature 430 °C and hot plate speed 5.25 inch/min)



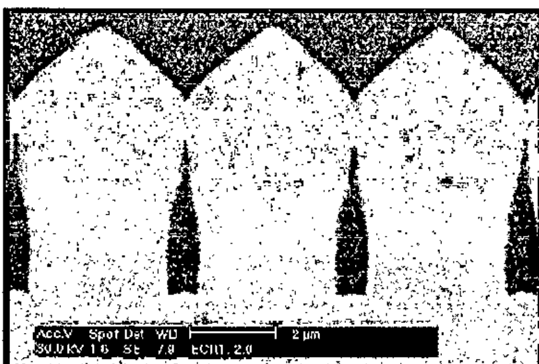
a) 6 µm-trench width b) 5µm-trench width



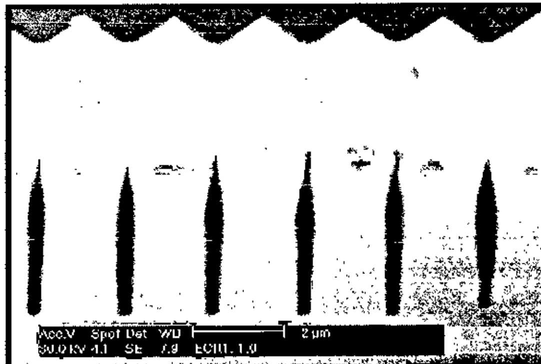
c) 4 µm-trench width



d) 3µm-trench width



e) 2 µm-trench width



f) 1µm-trench width

Fig. 4.9: SEM cross-sections of ECR-CVD at different trench width (chamber pressure: 4mT, top magnet current: 100 A, table height: 100 mm, DC bias voltage: –200 V, Ar gas rate: 0sccm, reactant gas: N_2O: 35sccm SiH_4/He: 100sccm)

Figure 4.10 shows the relationship between the aspect ratio of trenches and the trench-filling ratio for both ECR CVD and pyrolytic CVD. The respective parameter values in Fig. 4.10 refer to the initial conditions in the third column of Table 4.3. The

depth of the trench (t) is 4.0 μm constant and the width of the trench (w) is varied. For an aspect ratio of 1.0, the trench-filling ratio of ECR deposition is higher than 0.6 while the ratio of pyrolytic deposition is only 0.12, shown in Fig. 4.10. Although the trench-filling ratio of both techniques decreases as the aspect ratio increases, the ECR deposition shows a higher trench-filling ratio than the pyrolytic deposition for all aspect ratios. It is concluded that the trench-filling capability of ECR deposition is better than that of the pyrolytic deposition.

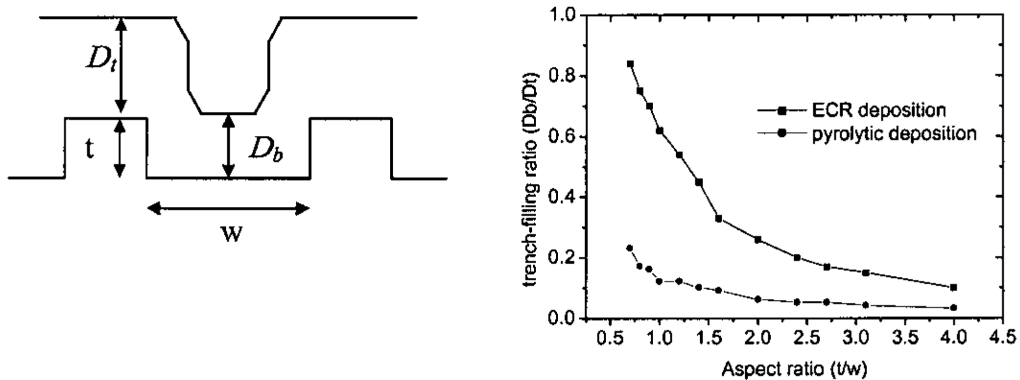
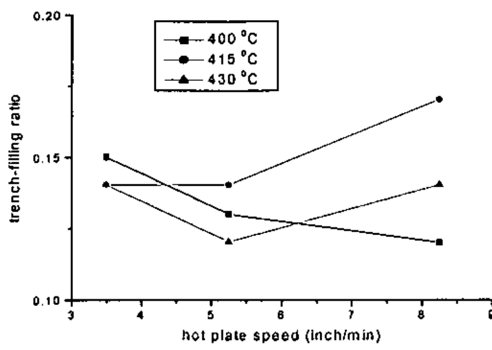


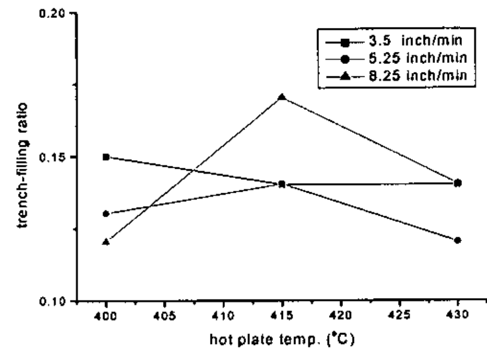
Fig. 4.10: Dependence of the trench-filling ratio on the trench aspect ratio (D_b is the deposition thickness of filling oxide at the bottom of a trench and D_t is the deposition thickness of filling oxide at the top of trench)

4.4 The effects of pyrolytic CVD parameters

For pyrolytic deposition the relationship between various deposition parameters and the resulting trench-filling ratio have been investigated. The parameters of each pyrolytic CVD experiments are shown in Table 4.4. As shown in Fig. 4.11, there is no significant change in the filling ratio with changes of the hot plate speed and hot plate temperature. More cases are shown in Fig. 4.12 and Fig. 4.13. There is also no significant change in those cases. It was found that even when the pyrolytic parameter values were varied as shown in Table 4.4, there was insignificant change from the lower curve in Fig. 4.10.

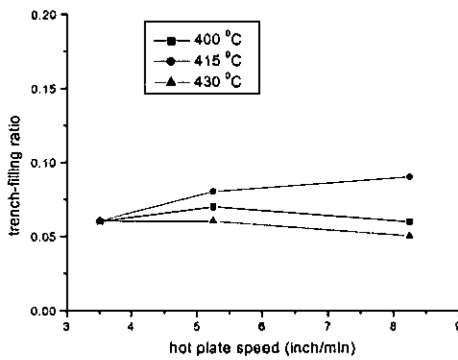


(a)

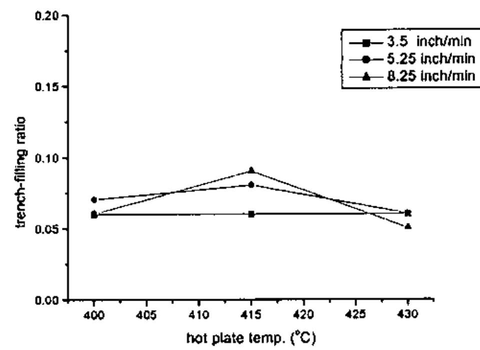


(b)

Fig. 4.11: The effect of pyrolytic-CVD variable changes at the trench aspect ratio 1.0
(a) the effect of hot plate speed (b) the effect of hot plate temperature

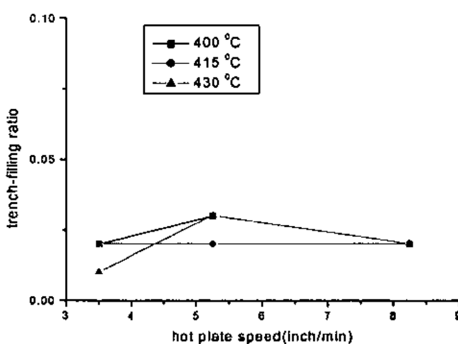


(a)

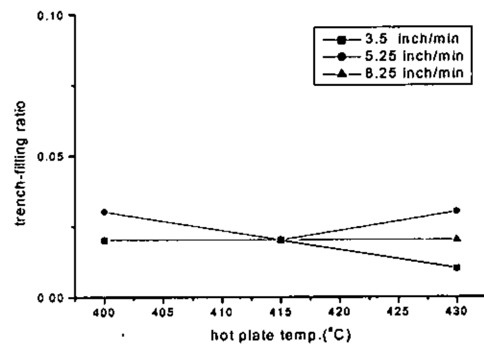


(b)

Fig. 4.12: The effect of pyrolytic-CVD variable changes at the trench aspect ratio 2.0
(a) the effect of hot plate speed (b) the effect of hot plate temperature



(a)



(b)

Fig. 4.13: The effect of pyrolytic-CVD variable changes at the trench aspect ratio 4.0
(a) the effect of hot plate speed (b) the effect of hot plate temperature

pyrolytic CVD experiments	hot-plate temperature (°C)	hot-plate speed (inch/min)
Pyro.#1	400	3.5
Pyro.#2	400	5.25
Pyro.#3	400	8.25
Pyro.#4	415	3.5
Pyro.#5	415	5.25
Pyro.#6	415	8.25
Pyro.#7	430	3.5
Pyro.#8	430	5.25
Pyro.#9	430	8.25

Table 4.4: The parameters of pyrolytic CVD experiments

4.5 The effects of varying the ECR-CVD parameters

In this section the effect of each parameter on the trench-filling properties and ECR deposition process will be discussed. In order to improve the ECR process to the point where voids were eliminated, I investigated the effects of each parameter on the trench-filling properties with ECR CVD.

4.5.1 The effects of chamber pressure

The trench-filling ratios of ECR CVD with different chamber pressures are shown in Fig. 4.14. The parameters of three ECR CVD cases are shown in Table 4.5. Exp.#1 represents the experiment with the initial recipe, and Exp.#2 and Exp.#3 represent the experiments with lower chamber pressure. It was found that the trench-filling ratio increases as the chamber pressure decreases as shown in Fig. 4.14. The lower chamber pressure causes fewer ion collisions in the chamber, which results in highly anisotropic ion directionality and increases the deposition rate in trenches. It was also found that there are smaller differences of trench-filling ratios between the chamber pressures in the higher aspect ratio range than in the lower. The deposition rate on a flat sample increases slightly with the increase of chamber pressure as shown Fig. 4.15. The reason is that the deposition rate (at chamber pressures higher than 1mT) is

affected mainly by radicals rather than ions [110]. At these chamber pressures the electron temperature is high enough to dissociate silane molecules near the wafer even though both plasma density and electron temperature decrease with increasing the pressure, and hence ions deliver less kinetic energy on the wafer surface for the activation of the reactions.

ECR-CVD experiments	chamber pressure (mT)	upper-magnet current (A)	table height (mm)	DC-bias voltage (V)	Ar gas rate (sccm)	reactant gas flow rate
Exp. #1	4	100	100	-200	0	normal
Exp. #2	2*	100	100	-200	0	normal
Exp. #3	1.3*	100	100	-200	0	normal

Table 4.5: The parameters of ECR CVD for chamber pressure
(* cells denote values which deviate from the initial conditions in Exp. #1)
(normal flow rate: N_2O:35sccm SiH_4/He :100sccm)

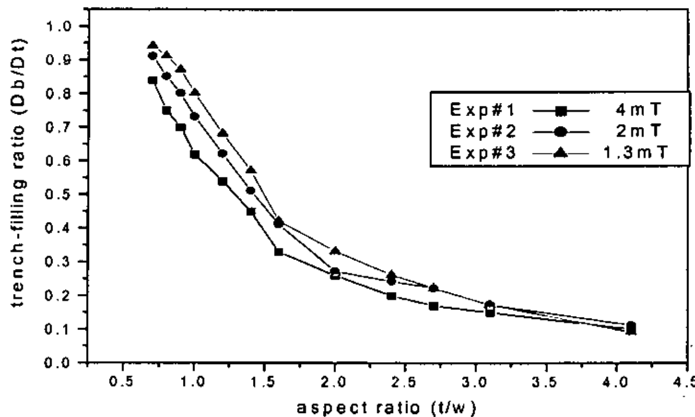


Fig. 4.14: Trench-filling ratio of ECR CVD as a function of aspect ratio, showing effects of chamber pressure

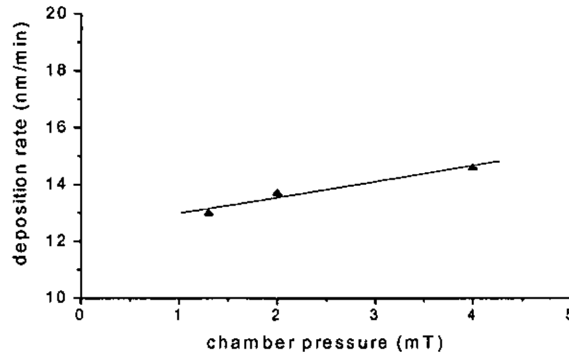


Fig. 4.15: Chamber pressure dependence on deposition rate

4.5.2 The effects of magnet current

The magnet current controls the magnetic flux density to attain the ECR condition which enables the plasma to absorb the microwave energy. The intensity of the magnetic field in the specimen chamber decreases gradually from the plasma chamber to the specimen table [103]. The parameters of three ECR CVD cases are shown in Table 4.6. Exp.#1 represents the experiment with the initial recipe, and Exp.#4 and Exp.#5 represent the experiments with higher upper magnet current. In Fig. 4.16 we show the effects of current in the upper magnet coil (Fig. 4.7) on the trench-filling ratio as a function of aspect ratio. Figure 4.16 indicates the higher trench-filling ratios as the upper-magnetic currents are increased. Shufflebotham et al. have emphasized that microwaves launched into a plasma are reflected where the magnetic field increases into an ECR region, and prefer a 'magnetic beach' profile of a continuously decreasing field from the microwave window [115]. Also Stevens et al. have found that high plasma densities near the microwave window produce stronger absorption [111]. We therefore consider here that variations in the upper coil field are more significant than those in the lower. The current in the upper coil was always maintained $\geq$ 100A to ensure a considerable ECR volume for microwave absorption immediately below the entrance window. As the upper-magnet current increases from 100A to 120A, a higher trench-filling ratio was obtained. This is because the higher magnet current tends to keep a larger volume of plasma subject to the ECR condition in the plasma chamber and produces more ions in a near-vertical direction in the chamber. Hence a greater flux of ions is transferred to the substrate,

which results in relatively higher deposition rates inside the trenches. However, there was no significant change in deposition rate on the horizontal wafer surface with the change of the magnet current.

ECR experiment	chamber pressure (mT)	magnet current (A)	table height (mm)	DC-bias voltage (V)	Ar gas rate (sccm)	reactant gas flow rate
Exp. #1	4	100	100	-200	0	normal
Exp. #4	4	110*	100	-200	0	normal
Exp. #5	4	120*	100	-200	0	normal

(* cells denote values which deviate from the initial conditions in Exp. #1)

Table 4.6: The parameters of ECR CVD for upper-magnet current

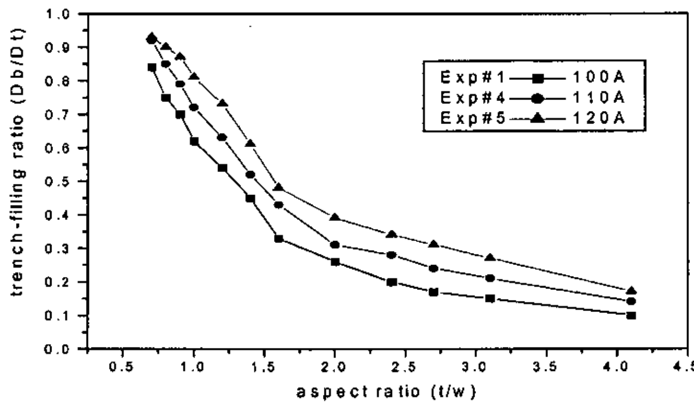


Fig. 4.16: Trench-filling ratio of ECR CVD as a function of aspect ratio, showing effects of magnet current

4.5.3 The effects of specimen-table height

The specimen-table height defines the distance from the extraction window of the plasma chamber to the table on which a wafer is located. The trench-filling ratios of ECR CVD with different table height are shown in Fig. 4.17. The parameters of three

ECR CVD cases are shown in Table 4.7. Exp.#1 represents the experiment with the initial recipe, and Exp.#6 and Exp.#7 represent the experiments with lower table height. The trench-filling ratio decreases as the specimen-table height decreases from 100mm to 30mm as shown in Fig. 4.17. I postulate that the effect of decreasing the table height increases the arrival angle of the ions on the substrate, which results in a higher deposition rate on the sidewall of trenches situated closer to the plasma source than those located at a longer distance. This promotes lateral growth near the tops of the trenches (refer Fig. 4.19) on a flat substrate and decreases trench-filling ratio gradually. I found that the deposition rate, when the table height was 30mm, increased 1.6 times in comparison with the two other table positions as shown in Fig.18. Fukuda et al. have found that the decomposition efficiency of SiH_4 increases and the deposition rate increases, when the table is located near the SiH_4 inlet position, due to the excitation by the electron cyclotron resonance in addition to the usual excitation by the oxidizing agent [116]. As shown in Fig. 4.19, the trench shape with 100mm of table height is partly tapered and partly vertical so that with continuing deposition it would fill up completely. The trench with 30mm of table height has a re-entrant shape which would eventually fill the gap, but with included voids. It is evident that the severe overhang caused by the lateral growth of the dielectric results in low trench-filling capability.

ECR experiment	chamber pressure (mT)	magnet current (A)	table height (mm)	DC-bias voltage (V)	Ar gas rate (sccm)	reactant gas flow rate
Exp. #1	4	100	100	-200	0	normal
Exp. #6	4	100	65*	-200	0	normal
Exp. #7	4	100	30*	-200	0	normal

(* cells denote values which deviate from the initial conditions in Exp. #1)

Table 4.7: The parameters of ECR CVD for specimen-table height

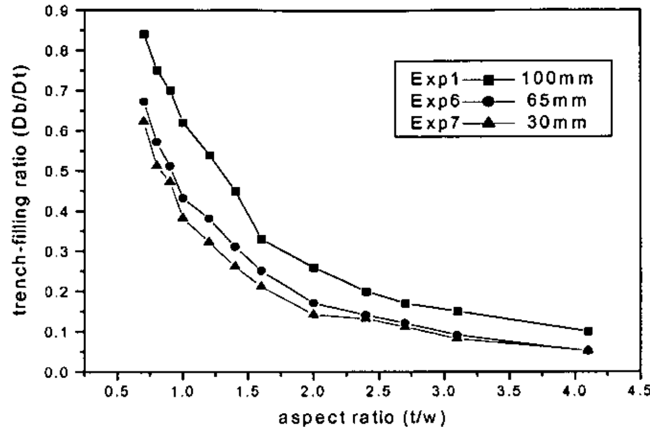


Fig. 4.17: Trench-filling ratio of ECR CVD as a function of aspect ratio, showing effects of specimen-table height

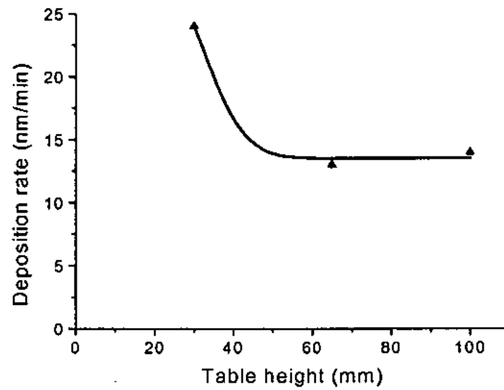
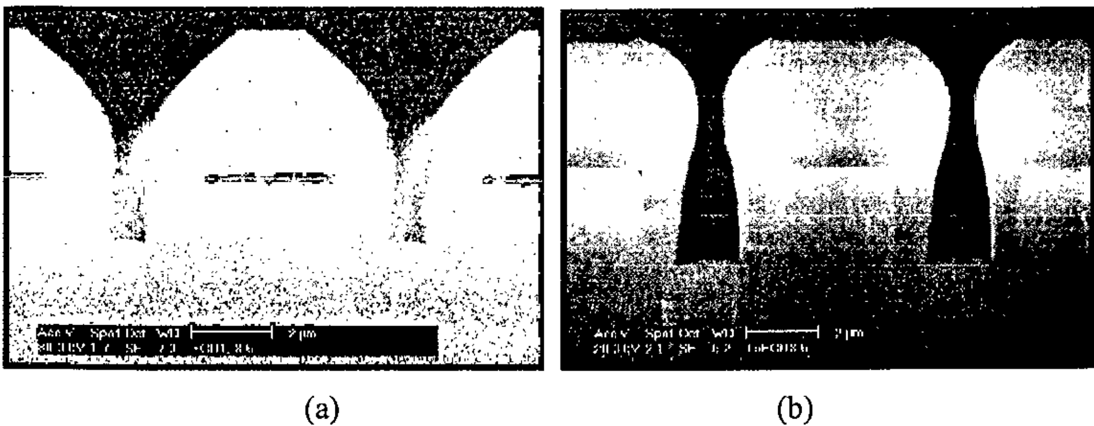


Fig. 4.18: Table height dependence on deposition rate
(Table height zero represents the extraction window position)



(a) (b)

Fig. 4.19: SEM cross-sections at different table height (trench width: 3.5um)
(a) table height 100mm, (b) table height 30mm

4.5.4 The effects of DC bias voltage and Ar gas flow rate

The parameters of ECR CVD with different DC bias voltage and Ar flow rate are shown in Table 4.8. Exp.#1 represents the experiment with the initial recipe (DC bias voltage -200V, Ar flow rate 0 sccm), Exp.#8 represents the experiment with higher DC bias voltage -300V, and Exp.#9 represents the experiment with Ar flow rate 50 sccm. The attempt to attain a bias of –400V was not successful because of a RF matching problem. This reduced the bias to a lower value, even at the maximum power obtainable from the RF supply. The experiment with Ar gas rate 100 sccms also was not successful because the higher Ar gas rate seemed to affect to the reactant gas flow rate and made the plasma unstable.

ECR experiment	chamber pressure (mT)	magnet current (A)	table height (mm)	DC-bias voltage (V)	Ar gas rate (sccm)	reactant gas flow rate
Exp. #1	4	100	100	-200	0	normal
Exp. #8	4	100	100	-300*	0	normal
Exp. #9	4	100	100	-200	50*	normal

(* cells denote values which deviate from the initial conditions in Exp. #1)

Table 4.8: The parameters of ECR CVD for DC bias voltage and Ar flow rate

The trench-filling ratios of the experiments with different DC bias voltages and Ar gas flow rate are shown in Fig. 4.20 and Fig. 4.21, respectively. We found that the trench-filling ratio increases as both the DC bias voltage and Ar gas flow rate increase. However, the deposition rate decreases slightly with the increase of DC bias voltage and Ar gas flow rate as shown in Fig. 4.22. The DC bias voltage is applied to the substrate to control the incident velocity of the ions (hence the energy of the plasma ions) to the wafer so that the surface of the wafer can be simultaneously sputter-etched as deposition proceeds [105]. Addition of Ar into the SiH_4/N_2O deposition chemistry transfers a higher energy to the sample surface due to the heavier ion bombardment compared with the reactant species alone [117]. These

parameters help to increase the sputter rate. Due to the dependencies on the angle of incidence of the ions, the sputter rate becomes a maximum near 45 [118]. The net result is that sputtering is greatest at the top corners of the trenches, which maintains an open gap. In addition, a part of the sputtered material would be expected to be re-deposited into the trenches. However, it is considered that higher sputter rate results in lower deposition rate because not all the sputtered material is re-deposited. Figure 4.23 compares one representative cross-section from Exp.#8 and Exp.#9 at 2-μm trench width, in which the gap in Fig. 4.23 (a) remained open while the gap in Fig. 4.23 (b) had already pinched off.

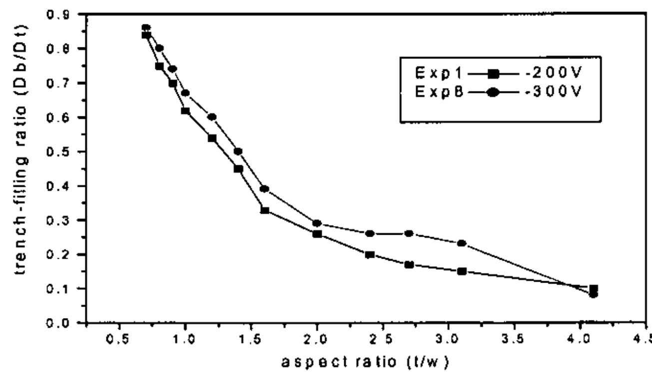


Fig. 4.20: Trench-filling ratio of ECR CVD as a function of aspect ratio, showing effects of DC bias voltage

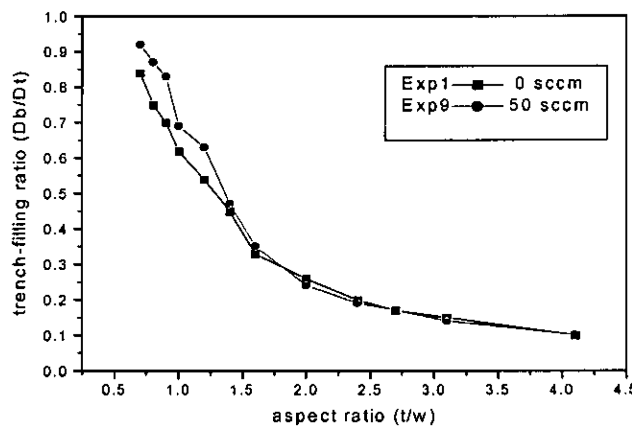


Fig. 4.21: Trench-filling ratio of ECR CVD as a function of aspect ratio, showing effects of Ar gas rate

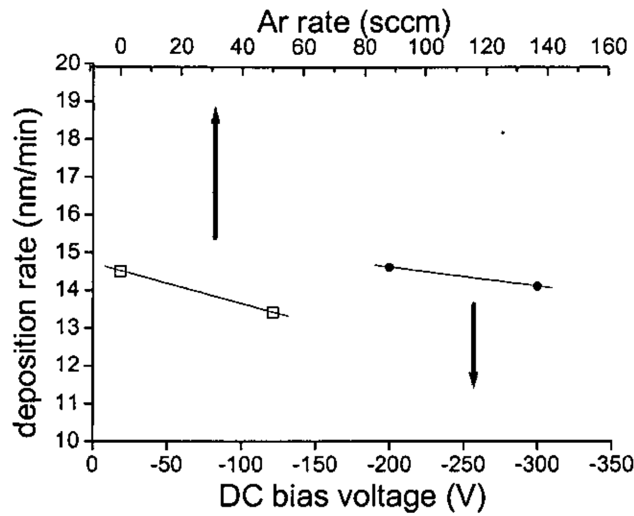
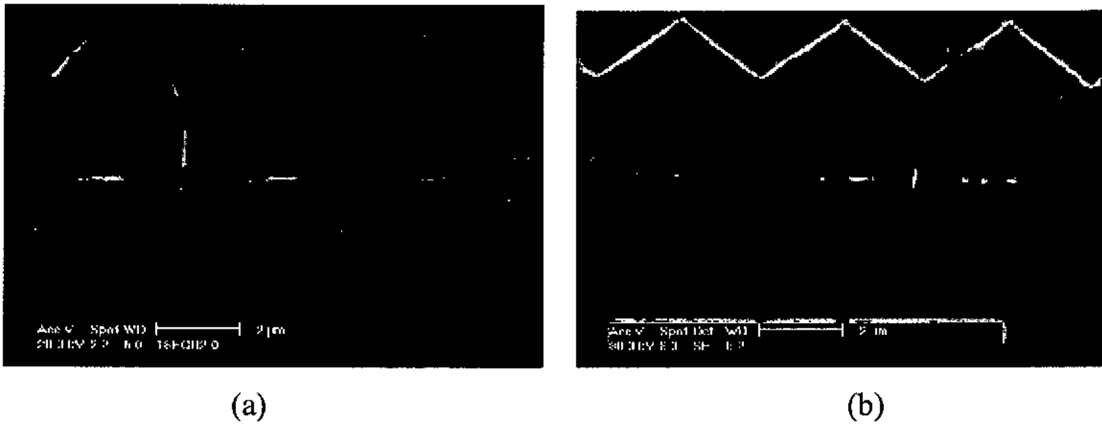


Fig. 4.22: Deposition rate as a function of DC bias voltage and Ar flow rate



(a) (b)

Fig. 4.23: SEM cross sections at 2-μm trench width (a) DC –300V (b) Ar gas rate 50sccms

4.5.5 The effects of reactant gas flow rate

The parameters of the experiments with different reactant gas flow rates are shown in Table 4.9. Exp.#1 represents the experiment with the initial recipe that includes the normal reactant gas flow rate (N_2O: 35sccm, SiH_4/He: 100sccm), and Exp.#10 represents the experiment with half flow rate (N_2O: 17.5sccm, SiH_4/He: 50sccm). The trench-filling ratios of the experiments with different reactant gas flow rates are shown in Fig. 4.24. I found that the trench-filling ratio increases as the reactant gas flow rate decreases which supports the findings of Machida and Oikawa [105].

However, I found that the flat deposition rate linearly decreases with the decrease of the reactant gas flow rate as shown in Fig. 4.25, in agreement with Lassig and Tucker [106]. The deposition rate varied from 7.7 nm/min to 14.6 nm/min as the silane flow rate was increased from 50 sccm (half flow rate) to 100 sccm (normal flow rate).

ECR experiment	chamber pressure (mT)	magnet current (A)	table height (mm)	DC-bias voltage (V)	Ar gas rate (sccm)	reactant gas flow rate
Exp. #1	4	100	100	-200	0	normal
Exp. #10	4	100	100	-200	0	half*

(* cell denotes values which deviate from the initial conditions in Exp. #1)

(normal flow rate: N_2O:35sccm SiH_4/He :100sccm,

half flow rate: N_2O:17.5sccm SiH_4/He :50sccm)

Table 4.9: The parameters of ECR CVD for reactant gas flow rate

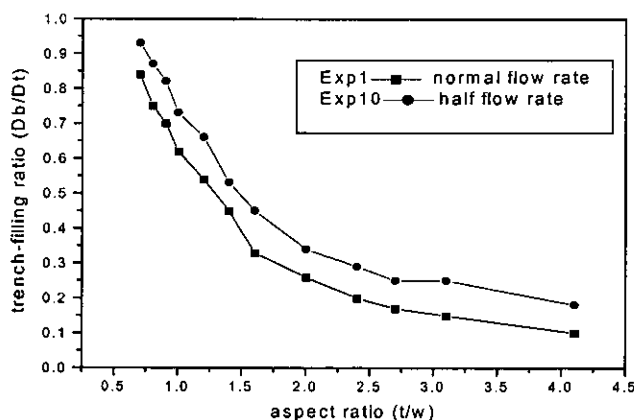


Fig. 4.24: Trench-filling ratio of ECR CVD as a function of aspect ratio, showing effect of reactant gas flow rate

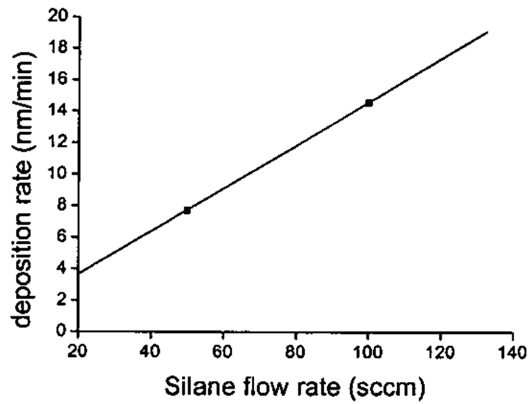


Fig. 4.25: Deposition rate versus gas flow rate

4.6 Application to planarisation of liquid crystal on silicon backplanes

Choosing the parameter values that produce the better trench filling, I improved the gap filling properties with two stage processes as shown in Fig. 4.26. The first stage (Exp.#11-1 in Table 4.10) was carried out with argon sputtering condition (Ar 25 sccm, N_2O 17.5 sccm, SiH_4/He 50sccm, chamber pressure 3.6mT, DC bias voltage –300V, magnetic current 120A) in order to keep the gap open. After 3 hours of process time, the deposited oxide was only 0.3μm thick on the top of the trenches (D_t) due to the sputtering while 1.35μm on the bottom of the trenches (D_b). The second stage (Exp.#11-2 in Table 4.10) was carried out in the higher rate deposition mode (N_2O 35 sccm, SiH_4/He 100sccm, chamber pressure 2.1 mT) to reduce the deposition-process time. The oxide deposition rate was 16 nm/min and trenches were completely filled up to 1.7μm-gap width (aspect ratio 2.4).

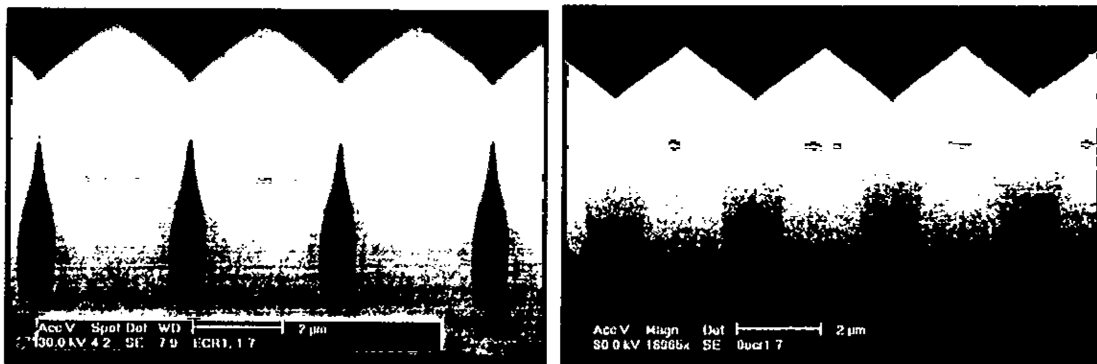
I demonstrated the improvement of the trench-filling capabilities with voids/ no voids analysis [119] [99] as shown Fig. 4.27, in which the straight lines represent the critical conditions between trench-fills with voids and trench-fills without voids, and the steeper slope of the line means better trench-filling capability. The voids tend to increase as trench width is decreased and aspect ratio is increased. Figure 4.27 shows the improvement depending on trench width and aspect ratio, which demonstrates

that the improved recipe (Exp. #11) gives better results that the original recipe (Exp. #1). Using the improved recipe, I achieved a planarised surface profile on a microdisplay backplane in a single process cycle without the need to repeat the oxide deposition / CMP process.

ECR experiment	chamber pressure (mT)	magnet current (A)	table height (mm)	DC-bias voltage (V)	Ar gas rate (sccm)	reactant gas flow rate
Exp. #1	4.0	100	100	-200	0	normal
Exp. #11-1	3.6*	120*	100	-300*	25*	half*
Exp. #11-2	2.1*	120*	100	-280*	0	normal

(* cells denote values which deviate from the initial conditions in Exp. #1)

Table 4.10: The parameters of improved recipe for application to planarisation of FLCOS backplanes



(a) (b)

Fig. 4.26: Comparison of SEM images of trench-fill patterns between original recipe and improved recipe with ECR CVD (trench width: 1.7μm, aspect ratio:2.4)
(a) trench-fill with original recipe, (b) trench-fill with improved recipe

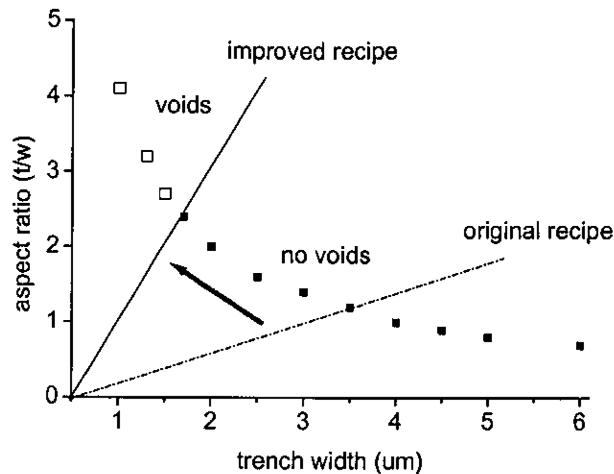


Fig. 4.27: Analysis of voids / no voids area as a function of trench width and aspect ratio

□ trench fill with voids

■ trench fill without voids

4.7 Conclusions

I compared the trench-filling capability of ECR CVD and pyrolytic CVD techniques and demonstrated that the trench-filling capability of ECR CVD is better than that of the pyrolytic CVD. I investigated the effects of ECR CVD parameters on the trench-filling properties and applied an improved recipe for better trench filling in deposition process of backplanes. The following results were obtained by varying the ECR CVD parameters:

(1) The trench-filling ratio (R) increases as the chamber pressure decreases (4mT – 1.3mT) because fewer ion collisions in the chamber result in highly anisotropic ion directionality and increase the deposition rate (D_b) in the trenches.

(2) The ratio (R) increases as the magnet current increases (100A – 120A) because it maintains a large volume of plasma and produces more ions in a near-vertical direction in the chamber, which results in higher deposition rate inside trenches.

(3) For the specimen-table height, the ratio (R) decreases as the table height

decreases (100mm – 30mm). This effect seems to be an increase in arrival angle of the ions on the substrate, which results in the higher deposition rate on the sidewall of trenches.

(4) The ratio (R) increases as both the DC bias voltage (-200V – -300V) and Ar flow rate (0sccm – 50 sccm) increase. The DC bias voltage and Ar flow rate assist to increase the sputter rate, which helps to maintain the trench open.

(5) Even though the ratio (R) increases considerably as the reactant gas flow rate decreases (N_2O: 35 sccm – 17.5 sccm, SiH_4/He: 100sccm – 50sccm), the deposition rate decreases to an impractical level.

Chapter 5:

Modeling of binary phase modulation on reflective FLC-SLMs

5.1 Introduction

Modelling of binary phase modulation is required to assist with achieving optimal performance of ferroelectric liquid crystals on silicon SLMs when used in coherent optical systems. This chapter involves characterization and modeling of phase modulation for FLCoS devices. This work involves development of a theoretical model, which describes the phase properties of the pixel thus allowing its use to simulate the performance of the device in a coherent application.

An electronic equivalent circuit, which describes the binary phase modulating properties of a SSFLC cell, will be characterized. The procedure for determining the circuit parameters, which describe the behavior of SSFLCs, will be discussed. To evaluate the performance of the HSpice model, experimental values of phase modulation will be measured from reflective FLC cells using an interferometer. This chapter first addresses the issues associated with characterizing LC cells which is essential for the development of any model. It then addresses existing models and their limitations and proposes the addition of a voltage-controlled current source. This new model is then evaluated using the results from the cells that have been characterized.

5.2 Theory of binary phase modulation

To describe phase modulation, the Jones matrix description is suitable for analyzing

the polarization of an optical signal as it passes through a FLC layer with polarizers [120]. Phase modulation can be calculated by multiplying an input Jones vector for the polarizers and a FLC layer using spreadsheets:

$$\begin{pmatrix} V'_x \\ V'_y \end{pmatrix} = \mathrm{P}(\alpha_A)\cdot \mathbf{W}(\theta)\cdot \mathrm{P}(\alpha_P)\cdot \begin{pmatrix} V_x \\ V_y \cdot e^{j\phi} \end{pmatrix}, \qquad (5\text{-}1)$$

where, V_x and V_y are the horizontal and vertical polarization components of the input, $\mathrm{W}(\theta)$ is the Jones matrix for the FLC at the tilted angle θ to the optic axis, α_A and α_P are the angles of the analyzer and polarizer, $\mathrm{P}(\alpha)$ is the Jones matrix for a linear polarizer rotated by angle α, and V'_x and V'_y are the horizontal and vertical polarization components of the output. Parameters of FLCs and polarizers are needed to develop the Jones matrix. As a result, the output profiles will include intensity and phase status of the light.

A phase modulator can be constructed by using a FLC half-wave retarder with two stable orientations for the optical axes, and its operational principle is shown in Fig. 5.1 [177]. If we take linearly polarized light along the y-axis as an input, then the FLC pixel fast axis positions must bisect the y-axis and will be oriented at angles of θ and $-\theta$, respectively. The Jones matrix for the one switching state (θ) will be

$$\begin{pmatrix} V'_x \\ V'_y \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix}\cdot \begin{pmatrix} e^{-J\Gamma/2}\cos^2\theta + e^{J\Gamma/2}\sin^2\theta & -J\sin\frac{\Gamma}{2}\sin(2\theta) \\ -J\sin\frac{\Gamma}{2}\sin(2\theta) & e^{J\Gamma/2}\cos^2\theta + e^{-J\Gamma/2}\sin^2\theta \end{pmatrix}\cdot \begin{pmatrix} 0 \\ V_y \end{pmatrix}$$

$$= \begin{pmatrix} -V_y J\sin\frac{\Gamma}{2}\sin(2\theta) \\ 0 \end{pmatrix} \qquad (5.2)$$

The other switching state ($-\theta$) will be

$$\begin{pmatrix} V'_x \\ V'_y \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix} \cdot \begin{pmatrix} e^{-J\Gamma/2}\cos^2\theta + e^{J\Gamma/2}\sin^2\theta & J\sin\frac{\Gamma}{2}\sin(2\theta) \\ J\sin\frac{\Gamma}{2}\sin(2\theta) & e^{J\Gamma/2}\cos^2\theta + e^{-J\Gamma/2}\sin^2\theta \end{pmatrix} \cdot \begin{pmatrix} 0 \\ V_y \end{pmatrix}$$

$$= \begin{pmatrix} V_y J\sin\frac{\Gamma}{2}\sin(2\theta) \\ 0 \end{pmatrix} \tag{5.3}$$

From the above equations, it is evident that the only difference between the two switching states is the minus sign, which means a π phase modulation.

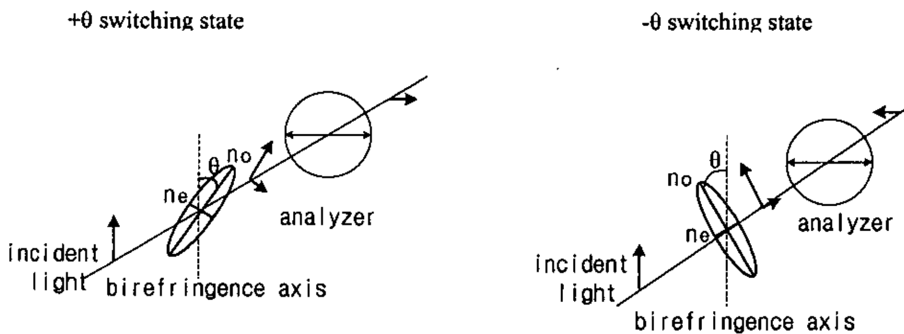


Fig.5.1: Operation principle of binary phase modulation in a SSFLC device, θ is the FLC cone angle, n_o, n_e are the ordinary and extraordinary refractive indices

5.3 Reflective FLC cell construction procedures

Reflective SSFLC cells were constructed with a thin layer of smectic C* FLC material sandwiched between an ITO-coated substrate and a reflective-mirror substrate, as shown in Fig. 5.2. Using the processes shown in Table 5.1, reflective FLC cells were constructed. The fabrication of the cell is such that the molecule directors align in the same direction by the influence of surface alignment layers. An aluminum film was coated onto a glass substrate to produce a reflective mirror. A polyimide solution, LQ1800 from Dupont Chemical, was coated onto the substrates and rubbed using a velvet cloth to form surface alignment layers. The ITO coated substrate and the aluminum-evaporated substrate were assembled together having a

cell gap 2.4μm. The assembled cells were filled at the isotropic phase (>97°C) of the FLC by capillary action and then slowly cooled (1°Cmin^{-1}) to room temperature. FLC materials, FELIX015/100 (Clariant GmbH) and CS1031 (Chisso Co.), were used for the experiments. The mixtures have a spontaneous polarisation of 33nCcm^{-2} and –28.1nCcm^{-2}, respectively. Two test cells were constructed using each FLC material, to confirm reproducibility of the experiment.

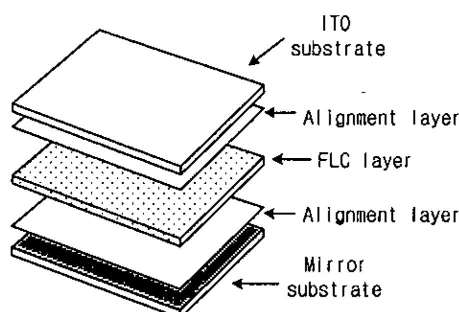


Fig. 5.2: Construction of a reflective FLC cell

The ITO coated glass should be optically flat (cell area 1.2cm^2), and the coated ITO should be uniform, have good optical transmission and low resistance. Merck in Germany supplied the ITO coated glass used for the majority of test cells. The substrate is soda lime glass (1.1 mm-thick) with an ITO coating of 125nm with a low resistivity of 20 Ω/square.

Substrate cleaning is a crucial procedure since any particles on the substrate can interfere with the required cell gap or affect to the surface morphology of the alignment film, which cause defects in the cell and result in low optical performance of the cell. It is extremely difficult to remove small particles because the adhesion forces increase as the particles' size decreases. After the cleaning process, substrates are stored in propanol as it evaporates more slowly than acetone.

The aluminum film was deposited in an Edwards E306 evaporator. The samples were placed 110mm directly above the W-filament source that had pieces of aluminum wires inside. When the chamber pressure reached 1.5×10^{-1} Torr, the HT power supply was used to form an Argon plasma for 20 mins. Then, the chamber was evacuated to

10^{-5} Torr to avoid any contamination to the film. The LT power was set to 30~40%, and aluminum was evaporated until the FTM display showed the desired thickness. As shown in Fig. 5.3, we need a minimum of 60-70nm thick film of evaporated aluminum film to reflect the incident light completely [121].

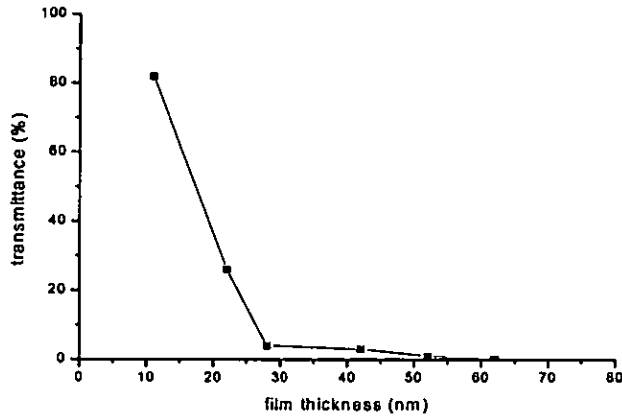


Fig. 5.3: Transmittance of the evaporated Al film against film thickness

For binary phase modulation, the reflective FLC cell is designed to act as a half-wave plate. This requires the reflective cell thickness t to be given by $t = \lambda/(4\Delta n)$, where Δn is the FLC birefringence and λ is wavelength of light. The cell should be of a uniform thickness to avoid splay distortions and allow good alignment. Unlike a transmissive cell, a reflective cell further complicates cell investigation due to the double pass of incident light in and out of the cell, which is more sensitive to the poor optical alignment. However, the reflective cell proved a useful tool in assessing phase modulation performance of reflective SLM devices.

process step	process details
1) ITO substrate cleaning	- Clean ITO substrates in an ultrasonic bath with acetone for 5 min. - Clean the substrates in the ultrasonic bath at 60°C with a detergent (Neutracon) for 60 min. - Rinse the substrates in the ultrasonic bath at 60°C with distilled water for 30min. - Store the substrates in propanol.
2) Al film coating	- Evaporate or sputter Al layer (200nm) on a substrate in order to make reflective electrode.
3) Polyimide coating	- Mix polyimide solution (1%) with NMP solvent. - Spin coat on a substrate with 3000 rpm speed for 90 sec. - Bake at 150°C for 10 min. - Bake at 250°C for 60 min.
4) Rubbing	- Rub the polyimide-coated surface on substrates using velvet cloth.
5) Packaging	- Glue two substrates (ITO coated glass, Al film coated glass) together at each corner using an UV curing glue (UVS 91) that contain spacer balls, with anti-parallel rubbing direction. - Put the cell on a hot plate at 110°C, and fill FLC material into the cell by capillary action. - Cool down slowly to room temperature (1°C/min.). - Seal the cell with an UV curing glue, and connect wires to each electrode.

Table 5.1: Reflective FLC cell preparation process

5.4 FLC cell appraisal techniques

5.4.1 Spontaneous polarisation

The value of the spontaneous polarisation can vary with the molecular characteristics of the FLC material and the achiral dopant introduced into the material. To measure the spontaneous polarisation, a commonly used method is the current reversal technique [122]. With this technique, the spontaneous polarisation and the rotational viscosity can be measured by applying a triangular-waveform voltage across the cell, and measuring the polarisation reversal current. The electric field applied to the cell changes the *Ps* dipole associated with each molecule flipping through 180°. If all the molecules in the cell are driven to move in the same direction, a current pulse can be observed as the bulk polarisation vector reverses its direction. The circuit configuration of the measurement is shown in Fig. 5.4. A triangular waveform voltage is applied to the cell and the series resistor. The current passing into the cell can be obtained by measuring the voltage across the resistor. Figure 5.5 shows the measured current to a triangular waveform voltage of $10V_{p\text{-}p}$ from the oscilloscope trace. The frequency of the applied voltage was 60 Hz and the value of the series resistor was 5.6 kΩ. The shape and position of this polarisation reversal current is found to be affected by the frequency and the amplitude of applied voltages, and the surface-anchoring condition [123] [124].

The area of the polarisation reversal current determines the total switching charge *Q*, supplied to the cell to reverse the polarisation (refer equation 3.9). The area of the polarisation reversal current is equal to twice the spontaneous polarisation. Hence, the spontaneous polarisation P_s can be calculated as

$$P_s = Q/2A \tag{5.4}$$

where A is the cell area.

The current reversal technique also allows measuring the current pulse height and the

voltage where the current peak occurs. The rotation viscosity γ can be calculated as [55]

$$\gamma = \frac{AP_s^2 E_m}{I_m \sin^2 \theta} \tag{5.5}$$

where E_m is the voltage on the triangular wave where the current peak occurs, I_m is the amplitude of the current peak and θ is the cone angle. However, this equation can be used only for bookshelf structures, as a chevron structure has some restoring torques which changes its bistable positions.

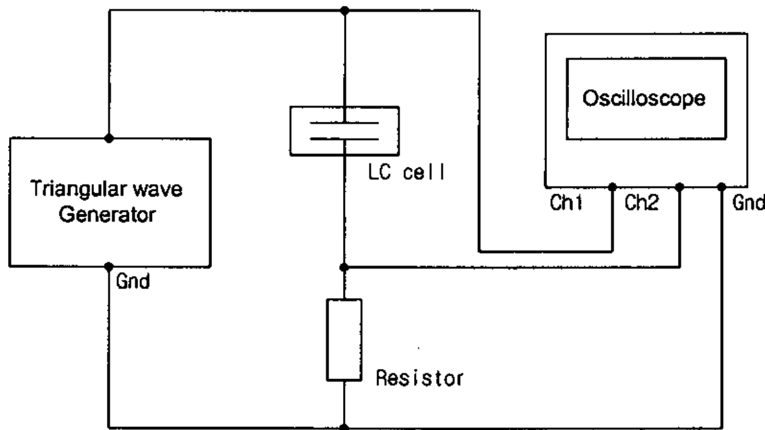


Fig.5.4: The circuit configuration for measuring polarisation reversal current

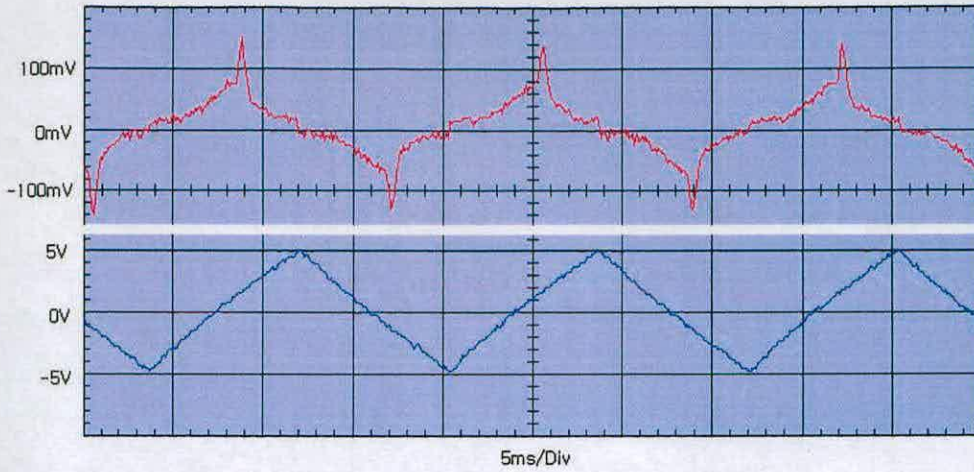


Fig.5.5: Measurement of polarisation reversal current
(top: measured polarisation reversal current, bottom: applied triangular voltage)

5.4.2 Optical output measurement

Figure 5.6 shows the optical arrangement for analyzing reflective test cells. A PC with customized software is connected through a GPIB interface between the Wavetek AWG75 signal generator and the Fluke PM3382A digital oscilloscope. Both input voltage and light output were captured by the oscilloscope. A collimated light source (λ = 632.8nm) was aligned for maximum transmission with an input polarizer, then the light passes through the test cell, and then passes through an output (crossed) polarizer. The resulting response of the reflective cell was measured with a photodiode amplifier at a room temperature of 20°C.

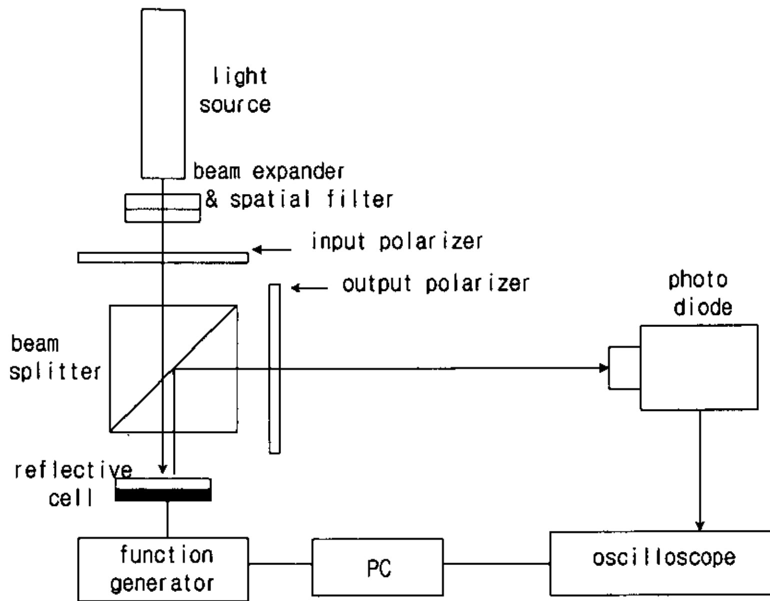


Fig. 5.6: Optical measurement setup for a reflective LC cell

Switching time

Switching time is important as it is needed to set the minimum period between electrical addressing and viewing time in SSFLC devices. Switching time is defined as the time period between 10% and 90% of the full switching range of the FLC. The switching time (τ) of a SSFLC device is proportional to the viscosity and inversely proportional to the spontaneous polarization of the FLC material [155]:

$$\tau = \frac{\gamma}{\mathbf{P}_s \mathbf{E}} \tag{5.6}$$

where γ is a viscosity, $\mathbf{P}_s$ is a spontaneous polarization and **E** is the applied external field.

Using the measurement setup in Fig.5.6, switching time versus applied voltage is measured as shown in Fig.5.7. In this case the switching time is around 80μs, and it normally increases with decreasing applied voltage, decreasing temperature and increasing cell gap. Switching times generally range from around 10 to 200μs for cell

gap of 1 to 2μm and typical CMOS drive voltages of 3 to 10V [33]. Switching time also linearly decreases with decreasing the alignment layer thickness [39]. Ouchi and *et. al* found that switching time is slower in chevron structures than in bookshelf structures of SSFLCs [125].

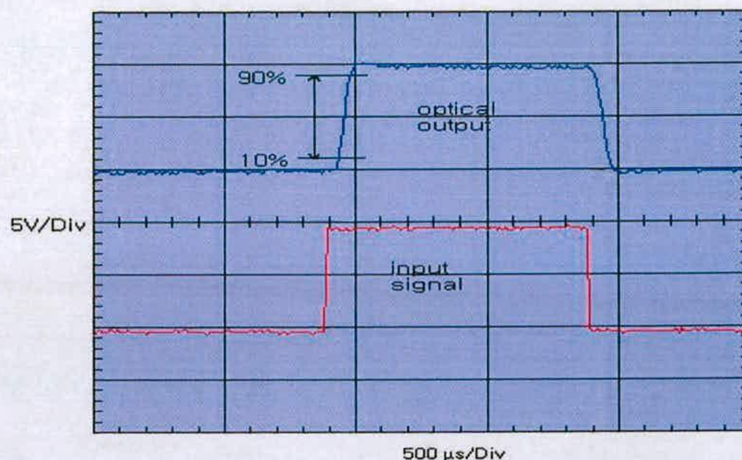


Fig.5.7: Switching time measurement of an FLC (CS1031) cell, at 10Vp-p applied voltage

Bistability

Bistability is an important factor to achieve high degrees of multiplexing in SSFLC devices. Bistability is mainly affected by surface interactions between the alignment layers and FLC material [126]-[129]. To achieve good bistability, the driving condition should be above a threshold voltage which is defined as the voltage giving 90% stable intensity to the maximum intensity.

Using the optical measurement setup in Fig.5.6, bistability of a SSFLC cell is measured as shown in Fig.5.8. The FLC used in the cell is CS1031 and the PI material is LQ1800 (Dupont). The frequency of the applied voltage is 83Hz with 9V positive and negative pulses of 0.5ms duration. The quality of bistability can be appraised by the ratio between 'dynamic contrast ratio' and the 'tail contrast ratio' of the photodiode response [39] as shown in Fig.5.8. If the cell were totally bistable, this ratio would be 1.

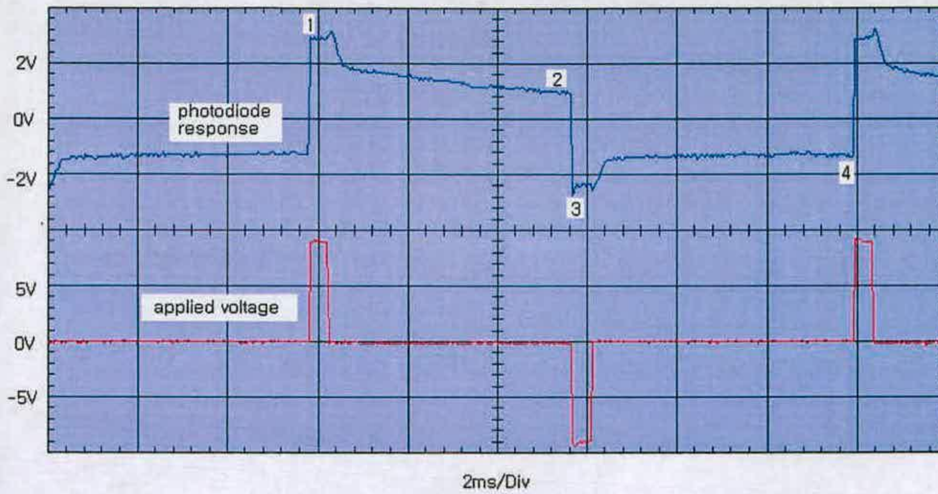


Fig. 5.8: Bistability measurement of a SSFLC cell.
(dynamic contrast ratio: ratio of the intensities at points 1 and 3,
tail contrast ratio: ratio of the intensities at points 2 and 4)

Contrast ratio

Contrast ratio of a reflective cell is ratio of the reflected luminance of the cell in its switched-on state to the luminance on its switched-off state. The FLC alignment uniformity of a cell before the elimination of any defects can be assessed by 'static contrast ratio', which can be measured by rotating the cell without applied voltage from light to dark under a microscope. Contrast ratio in normal operating condition can be assessed by 'dynamic contrast ratio', which is measured by applying a 100Hz square pulse (±10 V) to the cell. The dynamic contrast ratio of CS1031 material has been characterized by Bodammer and good dynamic contrast ratio (>200:1) was achieved over a broad range of alignment parameters [39].

When a FLC cell turns to the switched-on state, rotation angle to the switched-off state tends to be twice the cone angle. In the case of CS1031 measurement at room temperature (20°C), the rotation angle was 41°±1 which means the cone angle should be around 20.5°. This is in close agreement with the datasheet value of 19° at 25°C. It is considered that the angular discrepancy between measurement and datasheet value is caused by temperature dependency of cone angle. In general, cone angle

increases with decreasing temperature.

5.5 Phase shift measurement

A measurement technique based on Fizeau interferometer system was used for phase modulation on a reflective FLC cell as shown in Fig. 5.9. A laser beam (He-Ne) is expanded, spatially filtered, and linearly polarized to produce a vertically polarized collimated source. The beam is projected via a beamsplitter towards the Fizeau plate, which is optically flat. A portion of the beam is reflected from the Fizeau plate back to the beamsplitter as a reference beam. The rest of the beam travels towards the FLC cell that reflects a portion of the beam energy back into the system where it interferes with the reference beam and produces interference fringes on CCD camera.

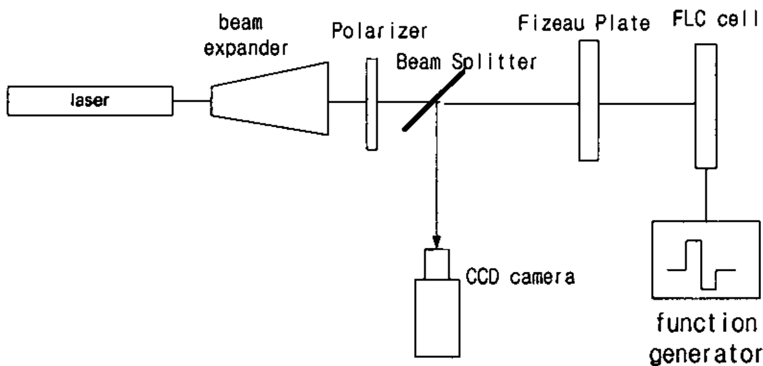


Fig.5.9: Setup for measuring phase shift on a reflective FLC cell

Driving the reflective test cell with rectangular pulses, two different interference patterns were recorded by a CCD camera. After transferring the patterns to an image handling software package, the fringe data was used to measure the shifted distance between two patterns. Then the phase shift was calculated from the measured data that was exported to a spreadsheet.

Fig.5.10 shows two different fringe patterns and the phase shift in degrees $\Delta\phi$ can be measured by:

$$\Delta\phi = 2\pi \times \frac{x}{d} \tag{5.7}$$

where, d is the period of fringe pattern and x is shifted distance of the pattern between two bistable states of an FLC cell. The period d can be varied by adjusting the position of the Fizeau plate and the FLC cell on a tilt mount which enables horizontal or vertical tilt fringes to be aligned for the measurement.

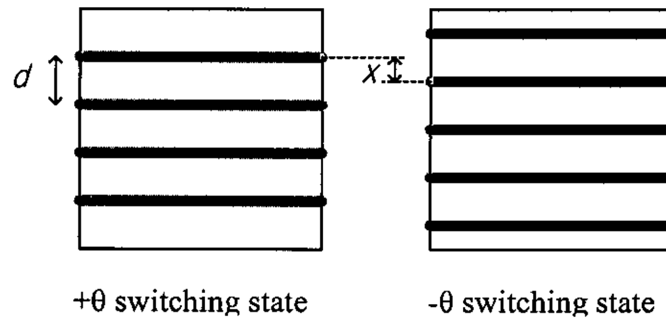
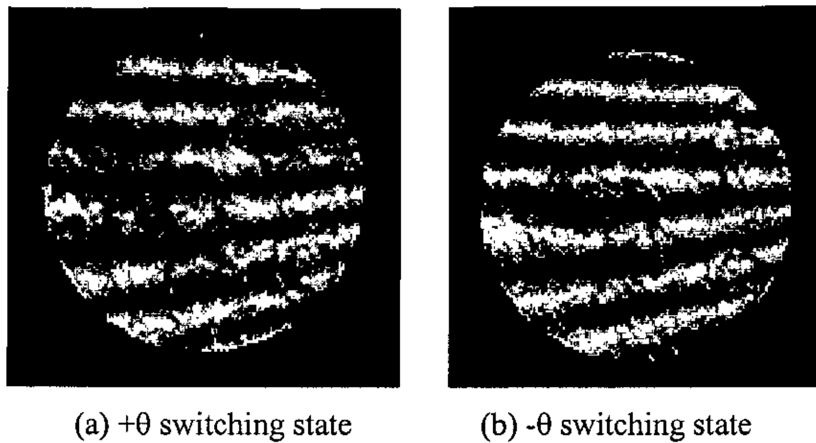


Fig. 5.10: Principle of phase shift measurement from two different fringe patterns

Figure 5.11 shows an actual measurement of fringe patterns in which (a) was switched to the +θ state and (b) was switched to the –θ state.



(a) +θ switching state (b) -θ switching state

Fig. 5.11: Recorded fringe patterns from the measurement setup in Fig. 5.9 (FLC material: FELIX015-100)

With this setup, values of phase modulation were measured with the two different FLC materials, FELIX015-100 and CS1031. The phase modulation measurements of test samples are given in Table 5.2 with an accuracy of ±8%. We can achieve pure binary phase modulation by adding an analyzer but the transmission efficiency decreases. If the FLC cell were an ideal half wave retarder, phase modulation should be four times the corresponding cone angle (refer Table 5.3), i.e., phase modulation in ideal conditions will be 0.57π in FELIX015-100 cells and 0.42 π in CS1031 cells.

	Sample #1-a	Sample #1-b	Sample #2-a	Sample #2-b
LC material	FELIX 015-100	FELIX 015-100	CS1031	CS1031
Measured phase modulation (rad.)	0.46± 0.03 π	0.53± 0.04 π	0.41± 0.02 π	0.37± 0.03 π

Table5.2: Phase modulation measurement of test samples

5.6 Model development

5.6.1 Equivalent circuit model

FLC material sandwiched between two glass substrates is a dielectric and can be regarded as a resistor and a capacitor connected in parallel. In an FLC cell with a chevron structure, the angle of the director round the cone (ϕ) is changed related to the rotational viscosity (γ), a restoring torque $K(\phi)$ and layer tilt angle (δ) (refer equation 3.14).

$$\gamma \frac{d\phi}{dt} = P_s E \cos\phi \cos\delta + K(\phi) \tag{5.8}$$

The equivalent circuit for phase modulation is shown in Fig. 5.12 in which the equivalent circuit for an FLC cell is derived from Moore and Travis' PSpice equivalent circuit [130]. This model treats the rotation of FLC directors with time and applied voltage as bulk mechanical effects, such that the director rotation angle ϕ is proportional to the charge on the capacitor C_{ps}. Using the charge on the capacitor C_{ps} of the Moore and Travis' model I derived the phase modulation by inserting an additional voltage-controlled current source E_{ph}. E_{OUT} represents light transmission and E_{ph} represents phase modulation. To run a simulation tool, Agilent's ICCAP, in a UNIX environment, the conversion of the equivalent circuit is needed from PSpice to HSpice model. Detailed simulation code of the equivalent circuit is shown in Appendix III.

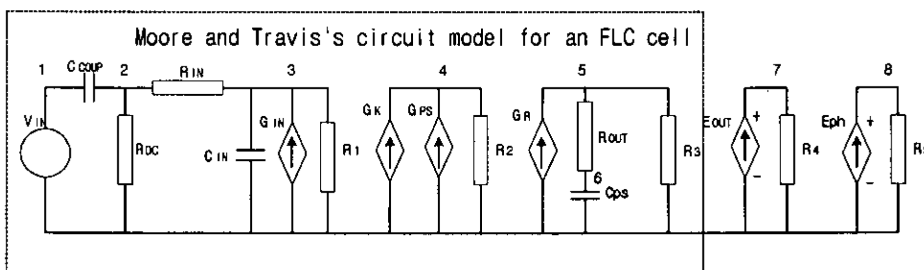


Fig. 5.12: HSpice equivalent circuit for phase modulation

- V_{in} is the input voltage
- C_{coup} is an AC coupling capacitor and R_{dc} is a DC restoring resistor
- R_{in} is a cell series resistance which represents the cell ITO resistance and the impedance of the input-voltage source
- C_{in} is the input capacitance with initial voltage
- R_l is the leakage resistance of the cell
- G_{in} is the ferroelectric input-current source determined by the charging current of the integrating capacitor C_{ps}. V_{tilt} represents the converted voltage in radians of the chevron tilt angle ($\delta \times \pi / 180$)

$$I_{Gin} = \frac{P_S(V_5 - V_6)\cos(V_6)\cos(V_{tilt})}{R_{out}} \tag{5.9}$$

- R_2 is the torque-sensing resistor. The voltage across R_2 is proportional to the sum of the restoring torque and the rotational torque
- G_k is the voltage-controlled current source which represents a restoring torque dependent on the director position around the cone

$$I_{Gk} = f(V_{Cps}) \tag{5.10}$$

- G_{ps} is the current source which represents the rotational torque

$$I_{Gps} = V_{Cin}\cos(V_{Cps})\cos(V_{tilt}) \tag{5.11}$$

- R_3 is DC continuity resistor, R_4 is light amplitude sensing resistor and R_5 is phase sensing resistor
- G_R is the viscosity setting current source, which charges the capacitor C_{ps} with a current dependent on the rotational viscosity

$$G_R = V_4 / \gamma R_2 \tag{5.12}$$

- R_{out} is a current sensing resistor, which detects the current in the capacitor C_{ps}
- C_{ps} is the integrating capacitor, whose voltage represents the director rotation angle ø in radians
- E_{out} is amplitude of transmitted light output and E_{ph} is phase of the transmitted light output

To define the current source E_{ph} in the HSpice equivalent circuit, the geometry of director position in SSFLC devices is investigated. SSFLC devices usually exhibit a chevron structure, which causes the smectic layers buckle through the depth of the device and layer tilt angle to the surface normal. Fig. 5.13 shows the tilted director position at the plane of alignment surface in the chevron structure. The cone angle θ defines a hypothetical cone of angle 2θ in which the molecular director switches within the cone in the surface plane, and varies with the FLC material. The chevron tilt angle δ is the angle that the FLC smectic layers make with the aligning surface normal. ϕ is the angle of the director rotating around the cone and ϕ_S is the case when the director is on the bistable position. From the geometry in Fig. 5.13 the switching angle Ψ is derived between projection of the director onto the plane of the cell and rubbing direction, and it is greater than the director angle Ψ_s on the plane of cell (refer equation 3.15).

$$\tan \Psi = \frac{\sin\theta \ \sin\phi}{\cos\theta \cos\delta + \sin\theta \cos\phi \sin\delta} \tag{5.13}$$

where, θ is the FLC cone angle, ϕ is the director rotation around the cone and δ is the chevron tilt angle.

If we make an FLC cell as a half wave plate, the cell will have the effect of rotating the phase of incident light by an angle of 2Ψ, which is phase modulation and denoted as E_{ph} in the HSpice model.

$$E_{ph} = 2\Psi = 2\,\mathrm{atan}\frac{\sin\theta\ \sin\phi}{\cos\theta\cos\delta + \sin\theta\cos\phi\sin\delta} \tag{5.14}$$

For the HSpice model the angles θ, ϕ and δ in equation (5.14) have to be converted into voltage per radian as shown in equation (5.15), for the simulation to work successfully. The equation (5.15) is inserted into the HSpice model as an additional voltage-controlled current source E_{ph} to give the voltage equivalent to the phase modulation of the cell.

$$E_{ph} = 2\,\mathrm{atan}\frac{\sin(V_{cone})\sin(V_{Cps})}{\cos(V_{cone})\cos(V_{tilt}) + \sin(V_{cone})\cos(V_{Cps})\sin(V_{tilt})} \tag{5.15}$$

where, V_{cone} represents the converted voltage of the cone angle in radian ($\theta \times \pi / 180$), V_{Cps} is the voltage of the capacitor (C_{ps}) in the HSpice model representing the director rotation around the cone in radian ($\phi \times \pi / 180$) and V_{tilt} represents the converted voltage in radians of the chevron tilt angle ($\delta \times \pi / 180$).

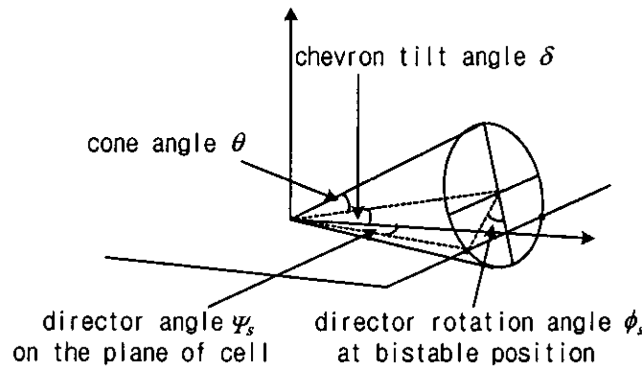


Fig. 5.13: Geometry of the tilted bistable director position at the plane of alignment surface in chevron structure

5.6.2 Model parameters measurements

For the simulation of the HSpice model, some ferroelectric cell parameters are needed: the cell gap, the cell active area, the cell capacitance, the spontaneous polarisation, the restoring torque, the director cone angle, the chevron tilt angle, and the viscosity. Table 5.3 shows the model parameters associated with four test cells, constructed for this study.

Some of the model parameters, such as restoring torque and rotational viscosity, vary with the cell gap and the alignment layer treatment [73] [124], and in this case we need direct measurements from the test cells rather than using data sheet values. These parameter measurements are carried out using the setup shown in Fig. 5.6.

	Sample #1-a	Sample #1-b	Sample #2-a	Sample #2-b
LC material	FELIX 015/100	FELIX 015/100	CS1031	CS1031
cell gap* (μm)	2.4	2.4	2.4	2.4
spontaneous polarisation* (nC/cm^2)	33	33	-28.1	-28.1
cone angle* (deg.)	25.5	25.5	19	19
cell capacitance (nF/cm^2)	5.9	5.7	8.9	8.3
effective cell area (cm^2)	1.2±0.1	1.2±0.1	1.2±0.1	1.2±0.1
cell resistance (MΩ)	> 20	> 20	> 20	> 20

* values from material supplier's data

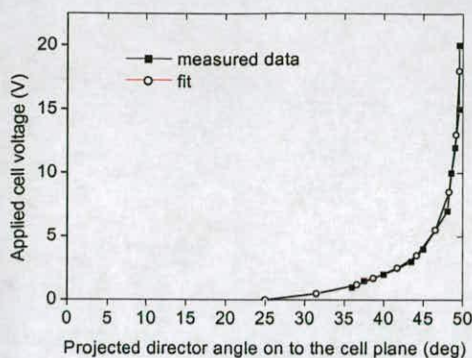
Table 5.3: Model parameters of test cells

Chevron tilt angle

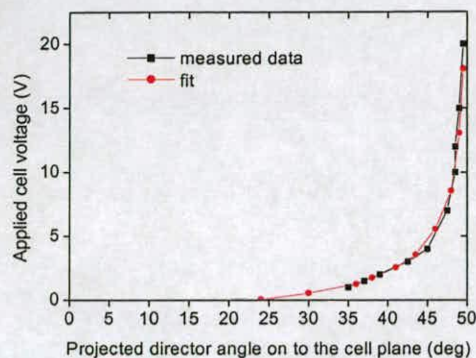
The value of chevron tilt angle is needed for the measurement of the director rotation angle ϕ_s and can be derived from the projected director angle Ψ_s. From the chevron structure geometry in Fig. 5.13, the projected director angle Ψ_s is specified as equation (5.16), whose values depend on the cone angle θ and chevron tilt angle δ (refer equation 3.12).

$$\cos\psi_s = \frac{\cos\theta}{\cos\delta} \tag{5.16}$$

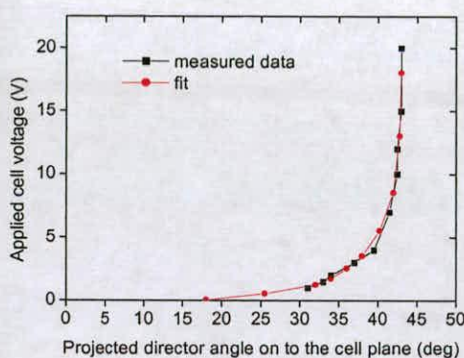
The projection of the director angle 2Ψ on to the cell plane is measured by applying a symmetrical square wave voltage across a test cell in the measurement setup (Fig. 5.6). Light transmission corresponding to the applied square wave voltage is altered by rotation of the cell position under crossed polarizers. As the cell is rotated, first a set of square wave maxima and minima are seen on the oscilloscope. With continued rotation, the pattern disappears and later appears with the maxima and minima of the first pattern interchanged. The angle 2Ψ is obtained as the difference in angular position between one set of maxima in light transmission and the opposite set of maxima. Fig. 5.14(a) shows the projection of the director onto the cell plane 2Ψ against peak drive voltage for cell (Sample #1-a), where we can find the projected director angle Ψ_s is 12.5°±0.5, given by $2\Psi_s$ = 25°±1. The measurements in other test cells have shown that the graphs produced in Fig. 5.14(a) and 5.14(c) can be similarly reproduced. Using the equation (5.16), we can find the chevron tilt angle δ is 22.4°, calculated from the measured projected director angle Ψ_s and the cone angle θ. The results of the chevron tilt angle δ measurements are shown in Table 5.4.



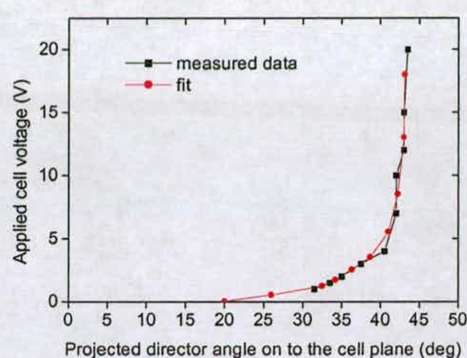
(a) Sample #1 (FELIX015/100)



(b) Sample #2 (FELIX015/100)



(c) Sample #3 (CS1031)



(d) Sample #4 (CS1031)

Fig. 5.14: The projected director angle (2Ψ) on to the cell plane against applied square-wave voltage

	Sample #1-a	Sample #1-b	Sample #2-a	Sample #2-b
projected director angle (Ψ_s)	12.5°±0.5	12°±0.5	9°±0.5	10°±0.5
cone angle (θ)	25.5°	25.5°	19°	19°
chevron tilt angle (δ) $\cos\delta = \cos\theta / \cos\Psi_s$	22.4°	22.7°	16.8°	16.2°

Table 5.4: Chevron tilt angle δ measurements from four samples

Restoring torque

If a director exceeds either two position, the restoring torque $K(\phi)$ tends to put the director back to the nearest stable positions. The restoring torque has nonlinear properties and can be simulated with a look-up table as shown in Fig. 5.15 [130]. The bistable positions of directors vary with the FLC cells, so the position angles should be measured from the actual test cells.

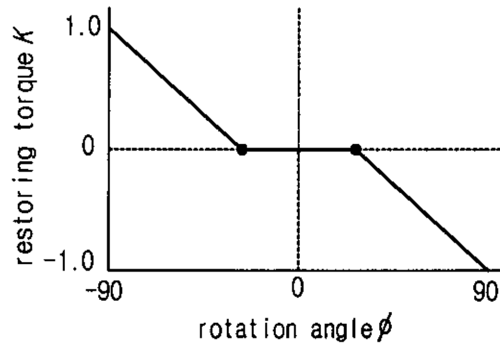


Fig. 5.15: Restoring torque with bistable positions of the director as a function of rotation angle ϕ (bistable positions are shown as dark spots)

From the chevron structure geometry in Fig. 5.13, the stable position of the director rotated about the circular face of the cone is (refer equation 3.13):

$$\cos\phi_s = \frac{\tan\delta}{\tan\theta} \tag{5.17}$$

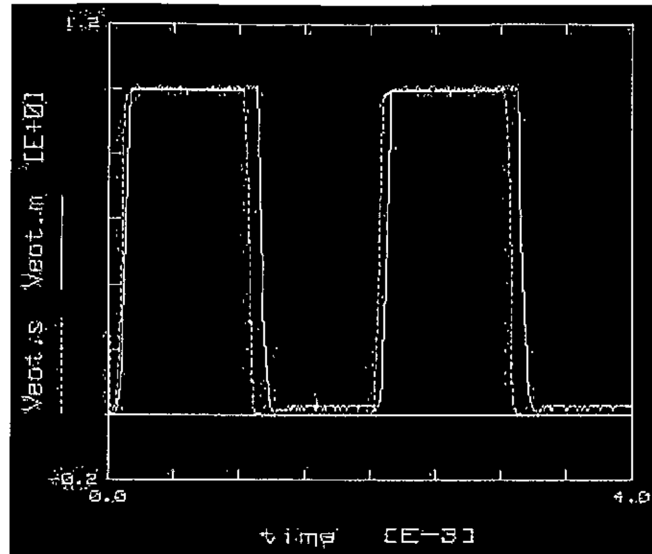
We already know chevron tilt angle (δ) from the measurement (section 5.6.2) and cone angle from Table 5.3. We can calculate the director rotation angle ϕ_s using the equation (5.17) and the results are shown in Table 5.5.

	Sample #1-a	Sample #1-b	Sample #2-a	Sample #2-b
chevron tilt angle (δ)	22.4°	22.7°	16.8°	16.2°
cone angle (θ)	25.5°	25.5°	19°	19°
director rotation angle (ϕ_s) $\cos\phi_s =$ $\tan\delta / \tan\theta$	30.6°	28.7°	28.7°	32.5°

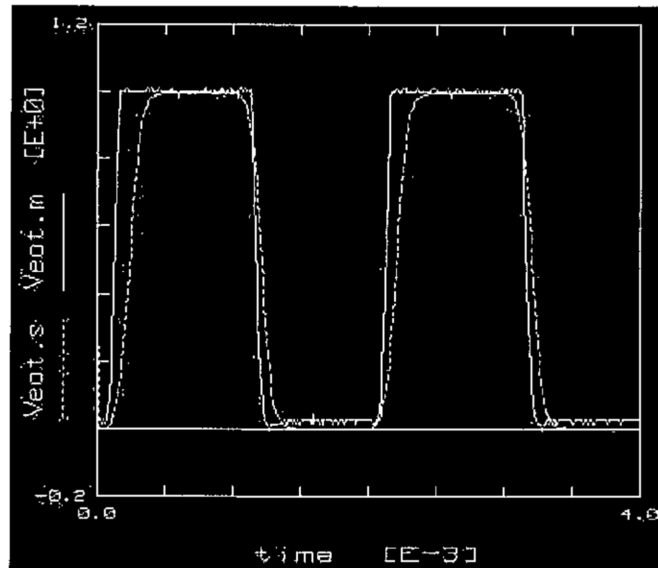
Table 5.5: Stable position angle ϕ_s measurements from four samples

Rotational viscosity

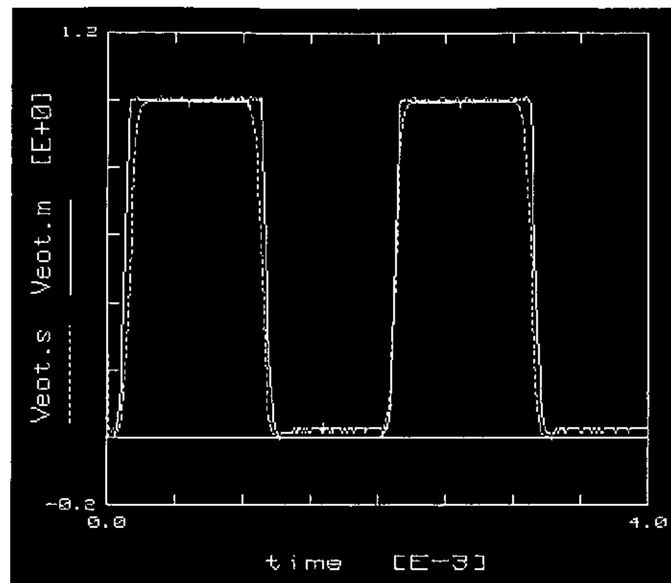
The last parameter we need for the model is rotational viscosity. As the direct measurement of the rotational viscosity is difficult, I have obtained the value of rotational viscosity of a cell by running the simulation with best fit. The actual light transmission pulse can be measured from the setup (Fig. 5.6). Simulated light transmission is plotted by setting the $E_{OUT} = \sin^2 2\Psi$ in the HSpice model. I compared the simulated light transmission pulse shape and position of the model with the measured light transmission pulse and choose the best fit between simulated and measured transmission pulses from simulation sets. For example, Fig. 5.16 shows the simulated light transmission response and measured light transmission for the sample #1-a cell with various values of the rotational viscosity, driven by ±5V square wave. The closest fit is indicated a rotational viscosity of approximately 215 mPa.s ±10.



(a) rotational viscosity of 100mPa.s



(b) rotational viscosity of 300mPa.s



(c) closest fit with a rotational viscosity of 215mPa.s

Fig. 5.16: Simulation with different rotational viscosity, for the applied ±5V square-wave input voltage (Veot.s : simulated waveform, Veot.m: measured waveform)

The results of the rotational viscosity measurements are shown in Table 5.6.

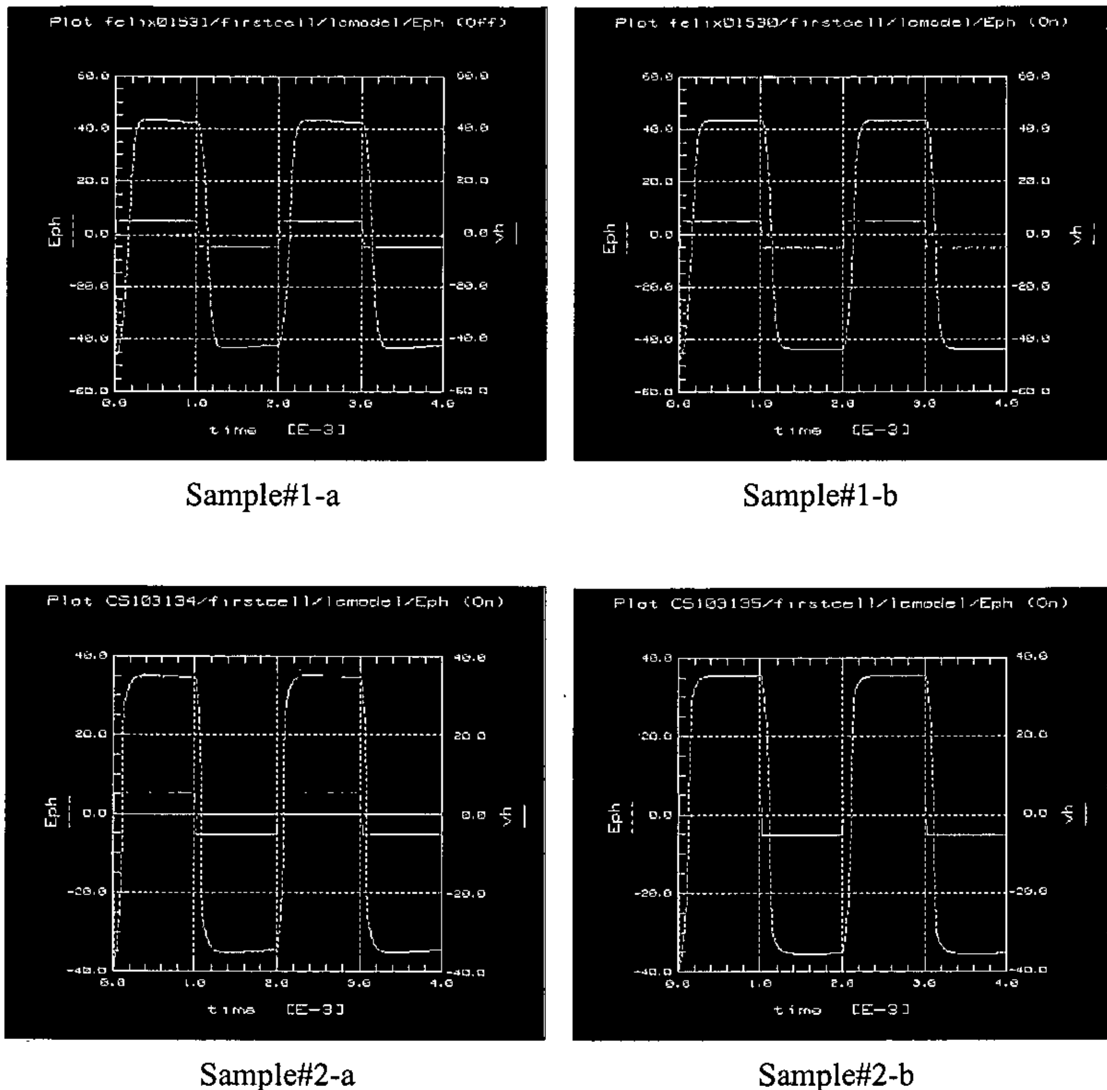
	Sample #1-a	Sample #1-b	Sample #2-a	Sample #2-b
Rotational viscosity (mPa.s)	215 ±10	170 ±10	11 ±2	42 ±5

Table 5.6: Rotational viscosity measurements from simulation

5.7 Simulation results and discussion

With the measured parameters the test sample performance was simulated. Figure 5.17 show the simulation results with the drive voltage and phase modulation curve

for ±5 V drive. The values of phase modulation can be derived from the simulation curves.



Sample#1-a Sample#1-b

Sample#2-a Sample#2-b

Fig.5.17: Modeled phase modulation curve for test cells
(Vh : applied input voltage, Eph: simulated phase modulation output)

Figure 5.17 show that the switching time of phase modulation output in both samples 1a and 1b much slower than the switching time in samples 2a and 2b. This is because the switching time is attributed to the higher rotational viscosity (refer Table 5.6) which depends on the FLC materials. The FLC switching time is proportional to rotational viscosity and inversely proportional to spontaneous polarisation and applied electric field [155].

To test the model performance, phase modulation comparisons are made between the experimental (refer Table 5.2) and simulated curves as shown in Table 5.7. The values of the measured phase modulation agree with values of the simulated within 9 %.

	Sample #1-a	Sample #1-b	Sample #2-a	Sample #2-b
LC material	FELIX 015-100	FELIX 015-100	CS1031	CS1031
measured phase modulation (rad.)	0.46± 0.03 π	0.53± 0.04 π	0.41± 0.02 π	0.37± 0.03 π
simulated phase modulation (rad.)	0.47± 0.01 π	0.48± 0.01 π	0.38± 0.01 π	0.38± 0.01 π

Table 5.7: Comparison of phase modulation between measured and simulated data

As mentioned in section 5.5, phase modulation in ideal conditions will be 0.57π in FELIX015-100 and 0.42π in CS1031 cells. One of the factors contributing to these deviations from ideal cells comes from the fact that for the ideal cell the cell-gap is selected to produce a half wave plate (retardation $\Gamma = \pi$). If the retardation of the FLC device is π and the cone angle of the FLC is 45°, it is possible to achieve pure binary phase modulation with 100% transmission. However, if the retardation is not π or cone angle of the FLC is not 45°, as is the case with our device, polarizers have to be introduced to achieve pure binary phase modulation and the power transmission decreases as shown in Fig. 5.18. The deviation from optimum cell-gap affects the efficiency of phase modulation. As Γ deviates from π rad, phase shift between the two output states is moved away from an expected value and power is transferred into undesired un-modulated light resulting in reduced efficiency [131].

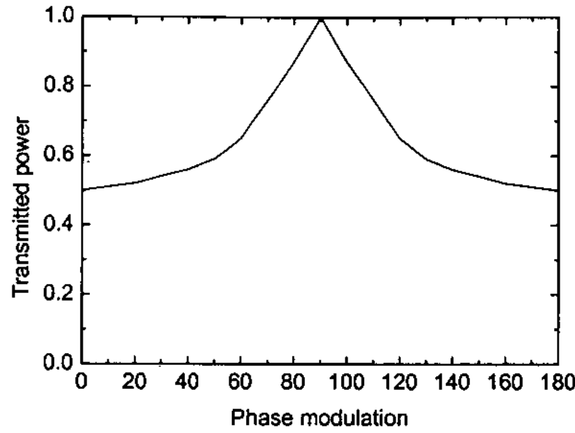


Fig. 5.18: Normalized transmitted power associated with a given phase modulation for a 22.5° (cone angle) FLC material

To verify the effect of cell-gap variations from a half wave plate, the phase shift produced by a FLC SLM is presented by use of Jones matrix. The FLC is considered as a retarder with a Jones matrix **W** at an arbitrary angle:

$$\mathbf{W} = \begin{pmatrix} e^{-J\Gamma/2}\cos^2\theta + e^{J\Gamma/2}\sin^2\theta & -J\sin\frac{\Gamma}{2}\sin(2\theta) \\ -J\sin\frac{\Gamma}{2}\sin(2\theta) & e^{J\Gamma/2}\cos^2\theta + e^{-J\Gamma/2}\sin^2\theta \end{pmatrix} \tag{5.18}$$

where, its optical axis is at an angle θ to the vertical and has a retardance of Γ.

The incident light **V** is vertically polarized and is described by

$$\mathbf{V} = \begin{pmatrix} 0 \\ 1 \end{pmatrix}, \tag{5.19}$$

and the transmitted output light **T** without an analyzer is then given by

$$\begin{aligned}\mathbf{T} &= \mathbf{W}\cdot\mathbf{V}\\ &= \begin{pmatrix} e^{-J\Gamma/2}\cos^2\theta + e^{J\Gamma/2}\sin^2\theta & -J\sin\frac{\Gamma}{2}\sin(2\theta) \\ -J\sin\frac{\Gamma}{2}\sin(2\theta) & e^{J\Gamma/2}\cos^2\theta + e^{-J\Gamma/2}\sin^2\theta \end{pmatrix}\cdot\begin{pmatrix}0\\1\end{pmatrix}\\ &= \begin{pmatrix} -J\sin\frac{\Gamma}{2}\sin(2\theta) \\ e^{J\Gamma/2}\cos^2\theta + e^{-J\Gamma/2}\sin^2\theta \end{pmatrix}\end{aligned} \tag{5.20}$$

Phase shifts as cell gap variations have been calculated with the above matrix equation using Matlab programme as shown in Appendix IV. The correct cell gap should be 2.97μm for FELIX015/100 cell and 2.79μm for CS1031 cell. Figure 5.19 shows that the thickness variation from a half wave plate introduces a relative phase shift between the two output states. It is thought that this phase deviation caused by the cell thickness variation results in the mismatch between the ideal and simulated (or measured) phase modulation.

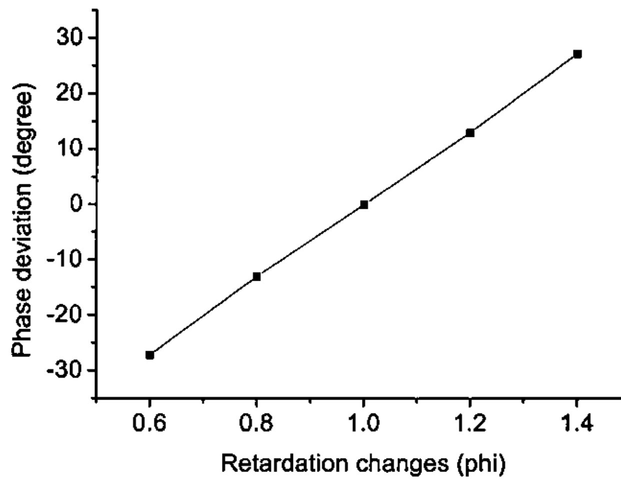


Fig. 5.19: Relative phase shift between the two-bistable states of FLC caused by deviations in the thickness of the cell gap from a half wave plate

5.8 Conclusion

I have presented a model for binary phase modulation by using an electronic equivalent circuit to describe the electro-optical properties of an SSFLC cell. To my knowledge this is the first time this has been reported and this model can be used in the characterization of phase modulation properties for designing FLC-on-silicon SLMs. I have described measurement techniques: phase modulation on a reflective SLM and modeling parameters such as rotational viscosity, chevron tilt angle and restoring torque. I have shown reasonable agreement within 9 % between the measured and simulated values of phase modulation of reflective FLC cells. The close agreement of the phase modulation results, for both sets of samples, has shown that the quality of the cells is reproducible.

Chapter 6:

Characterisation of multi-level phase modulation with NLCs using pulse-width modulation driving

6.1 Introduction

In phase modulating diffractive optical devices, multi-phase modulation provides improved performance over binary modulation. The use of binary phase levels restricts the diffraction efficiency of computer-generated holograms (CGHs) because the binary phase profile directs more light energy into the higher orders. Multi-phase modulation increases diffraction efficiency, eliminates the intrinsic inversion symmetry in the Fourier plane, and more accurately controls the phase-modulated output. The benefits of multi-phase modulation can be summarized as follows [132]:

(1) the maximum diffraction efficiency is increased because more power can be diffracted into a single order as the phase level is increased . The efficiency is given by [133]

$$\eta_{\max}(M) = \left[\frac{M}{\pi}\sin\left(\frac{\pi}{M}\right)\right]^2 \tag{6.1}$$

where, M is the number of phase levels. This equation shows the values of efficiency $\eta_{\max}(2) = 0.405$, $\eta_{\max}(4) = 0.811$, and $\eta_{\max}(8) = 0.950$.

(2) multiple phase levels eliminate the intrinsic inversion symmetry in the Fourier plane.

(3) multiple phase levels reduce quantization steps which enables a more accurate approximation to a required wavefront.

Thus, multi-phase modulation is highly desirable and must be characterized for optical applications. Nematic liquid crystals (NLC) SLMs are capable of multi-phase modulation by controlling their voltage level, but using this approach it is difficult to manage precise phase modulation. Moreover, the Si-backplane circuitry must be analogue (in particular those replicated in arrays) which suffers from the detrimental effect of random variation in the wafer fab process, making it more complicated than digital circuitry. Due to the complexity of the design, resolution of analogue CMOS backplanes are limited and their cost is high compared to binary CMOS backplanes. Pulse width modulation is required to control the multi phase of the nematic liquid crystals on a digital CMOS backplane. By introducing a pulse-width modulation driving scheme, multi-phase modulation can be achieved on a digital CMOS backplane with nematic liquid crystals.

In this chapter I introduce multi-phase modulation with NLCSLMs driven from a binary CMOS backplane. To drive binary CMOS backplanes for multi-phase levels, a pulse-width modulation driving scheme has been developed and a parallel-aligned NLC SLM constructed for its phase modulator. The diffraction efficiency properties for binary phase grating and 4-level blazed grating have been measured along with a comparison of far-field diffraction patterns being performed between binary and four-level phase hologram displayed by the 512×512 Si-backplane SLM.

6.2 Binary Si-backplane spatial light modulator

The Si-backplane used in this study is the 512×512 array of DRAM-type pixels [134] [135]. It was designed at Edinburgh University in 1996 and the backplane schematic is shown in Fig. 6.1. The backplane architecture has 64 data buslines (D00~D63) and 15 control buslines (PH1, PH2, LAL, IID, etc.) operating the device. The detailed specifications of the backplane are presented in Table 6.1.

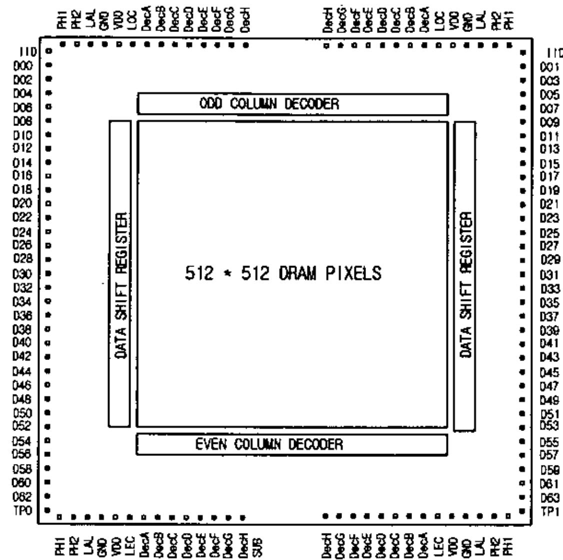


Fig. 6.1: Schematic diagram of 512 × 512 backplane

Number of pixels	512 × 512
Active pixel array area	10.24 × 10.24 mm²
Die area	14 × 14 mm²
Technology	1.2 μm n-well CMOS
Pixel circuit	pMOS pass transistor and MOS capacitor
Pixel pitch	20μm
Electrode mirror area	18.4 × 18.4 μm² (planarised)
Operating frequency	48 MHz
Data bus	64 bit
Frame scan time	84 μs
Drive voltage	5-6 V
Power dissipation	<100mW

Table 6.1: The 512 × 512 backplane specifications

The backplane addressing circuitry uses two 8-to-256 column decoders to enable the 512-pixel column lines and multiple serial shift register architecture (64 × 8 bit shift

registers) to load data. The column decoders are placed along the top and bottom of the display area, and the top decoder selects the odd columns and the bottom decoder selects the even columns. As shown in Fig. 6.2, the column decoders manage the enable buslines vertically located in the backplane. When all the eight decoder bits are high and load column signal (LOC or LEC) is high, the enable busline goes low and enables the relevant column line. As shown in Fig.6.3, the data shift registers are placed on the left and right side of the backplane and they manage the horizontal data buslines in the backplane. Data is loaded from the framestore on the interface board 64 bits at a time to the backplane device.

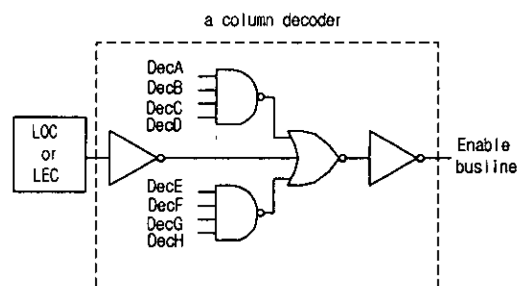


Fig. 6.2: Schematic diagram of a single column decoder

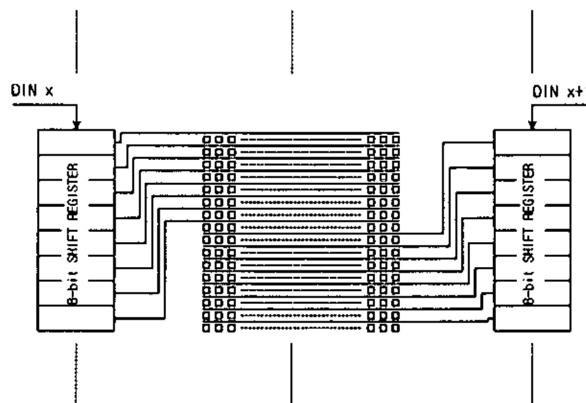
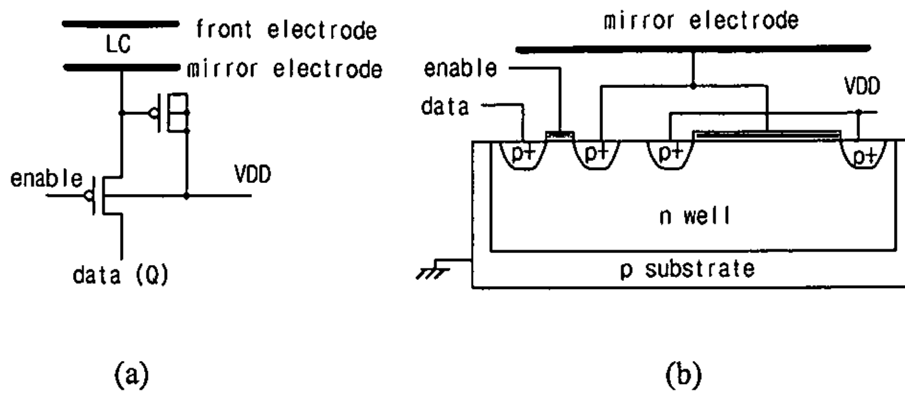


Fig. 6.3: Schematic diagram of the data shift registers and pixel array

Each pixel includes a pMOS pass transistor and a storage transistor capacitor along with the data, address and power lines. Fig 6.4(a) shows the schematic of a dynamic random access memory (DRAM) pixel circuit and Fig 6.4(b) shows a schematic cross sectional view of the DRAM pixel.



(a) (b)

Fig. 6.4: (a) Schematics of a DRAM pixel circuit, (b) a cross sectional view of the DRAM pixel

As the unplanarised backplanes have low pixel fill factors and optically rough surfaces, highly planarised pixels are required to improve optical performance in phase modulation. Each pixel is enlarged using a chemical mechanical polishing (CMP) planarisation technology [41] [136]. Due to the structure of the pixelation and repetition of the deadspace (the area between pixel electrodes), backplanes generate higher light intensity in the higher orders of the far field diffraction pattern. Figure 6.5 shows the planarised pixels (mirrors) on the 512 backplane, which have a 20-μm pitch and the 85% fill factor.

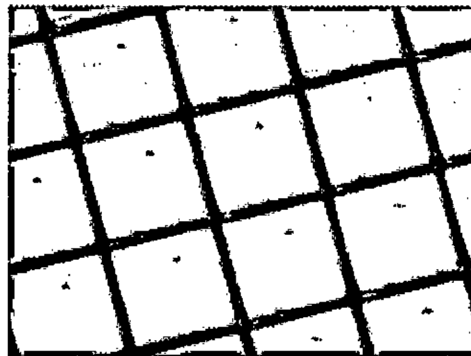


Fig. 6.5: Planarised pixels on the 512 backplane

The schematic cross-section of an assembled 512-backplane SLM is shown in Fig. 6.6. A 9-μm-thick layer of nematic liquid crystal was sandwiched between the front ITO substrate and the reflective backplane. The LC molecules were aligned parallel to the two substrates to allow phase-only modulation of light linearly polarized in the

same orientation as the LC director without changing the polarization direction of the light [137]-[139]. The LC alignment layers were achieved by obliquely evaporated SiO, which is better than the rubbing alignment to protect against any scratches of the alignment surfaces.

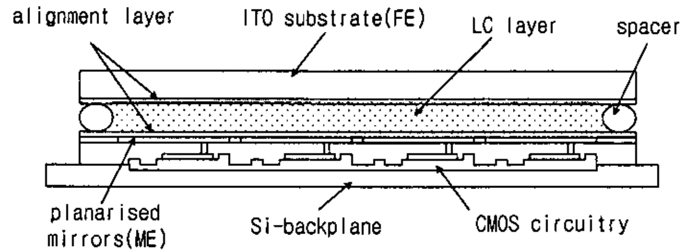


Fig. 6.6: The schematic cross-section of an assembled 512-backplane SLM

6.3 Pulse-width modulation driving scheme

6.3.1 Pulse-width modulation with a NLC cell

Multiple-phase modulation can be achieved by using pulse-width modulation of the NLC driven from a binary CMOS backplane. Pulse-width modulation is required to control the multi phase of the NLCs. The voltage waveform in Fig. 6.7 shows a pulse-width modulation scheme. The NLC phase information can be controlled by changing duty ratios of the applied voltage waveform.

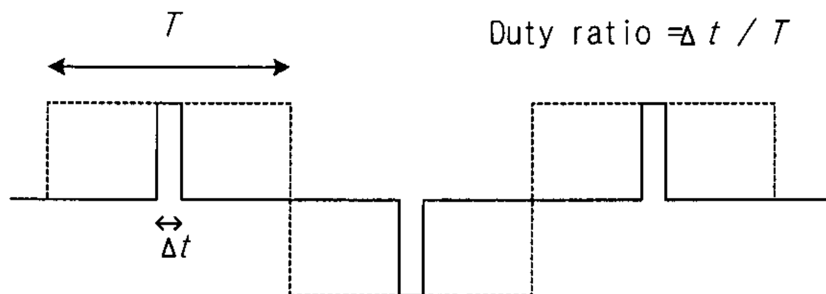


Fig. 6.7: Pulse-width modulation scheme

The characteristics of the NLC with pulse-width modulation were investigated using the experimental setup as shown in Fig. 6.8. A parallel-aligned NLC cell was used for measuring phase-shift properties. The cell was fabricated with 9μm-gap and NLC

(E7) was then injected into the empty cell at room temperature. Figure 6.9 shows the phase-shift properties of the NLC with different duty ratios and different applied voltages. This shows that the phase shift of NLC increases as the duty ratio of the applied pulse increases. Thus, multi-phase modulation can be achieved by applying pulse-width modulation to a NLC SLM. The phase shift of NLC begins earlier as the applied voltage increases, as shown in Fig. 6.9. The frequency of applied voltages was 1kHz. The phase shift properties are not changed as the frequency of applied voltages changes between 100Hz and 5kHz. The response time of the SLM depends on the type of LC material and applied voltage level. These results show useful phase shift relation against duty cycle and in particular an almost linear relation when using 3 volt peak-to-peak drive with a phase shift range of 6π.

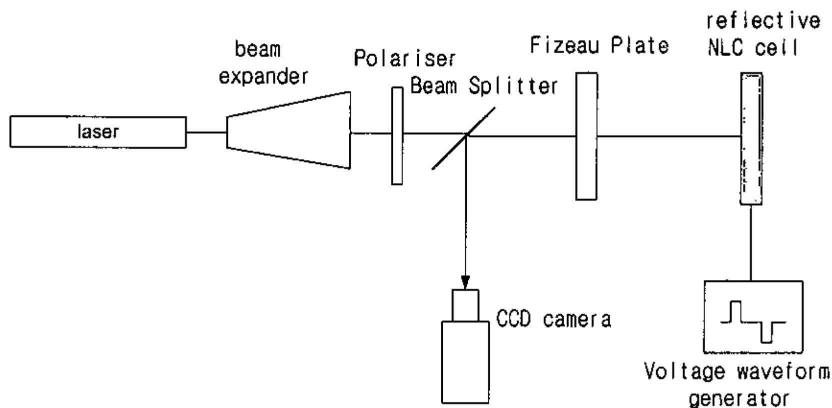


Fig.6.8: Measurement setup for phase-shift properties

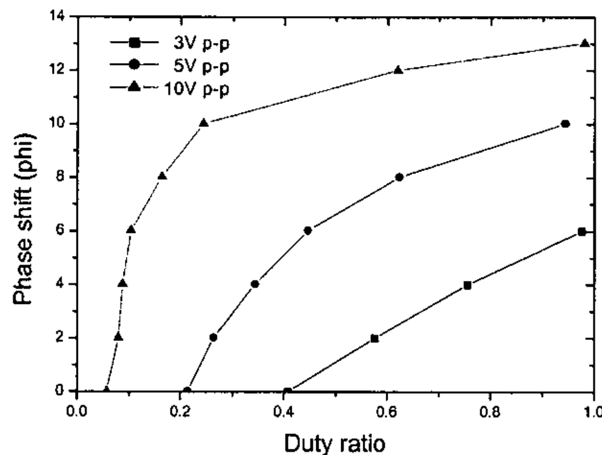


Fig. 6.9: Phase-shift properties of NLC (E7) as a function of duty ratio, showing effect of applied voltages (1kHz duty cycle)

6.3.2 Development of the driving scheme for Si-backplane SLM

Interface board

To drive the 512 × 512 array backplane, a custom digital interface was used (see Fig. 6.10), developed by MicroEmissive Displays Ltd. The board was designed to connect to a PC via a 78-way connector and PCI272 DIO card. A hardware-description programmed file ('rawbits' format) was needed to drive this interface board.

The interface board includes a field programmable gate array (FPGA) device that consists of an internal array of logic blocks with a ring of programmable input/output blocks. The FPGA configures the driving scheme and loads image data to a framestore. The FPGA used in the board was a Xilinx Spartan-XL XCS40XL-5-PQ240.

The interface board also includes a framestore which consists of two 64kb × 32 synchronous static random access memory. The framestore has space for 16 bit-planes where a bit-plane is 512×512 bits of data. A frame with a bit depth of 8bits was used for this study to apply multi-level phase modulation.

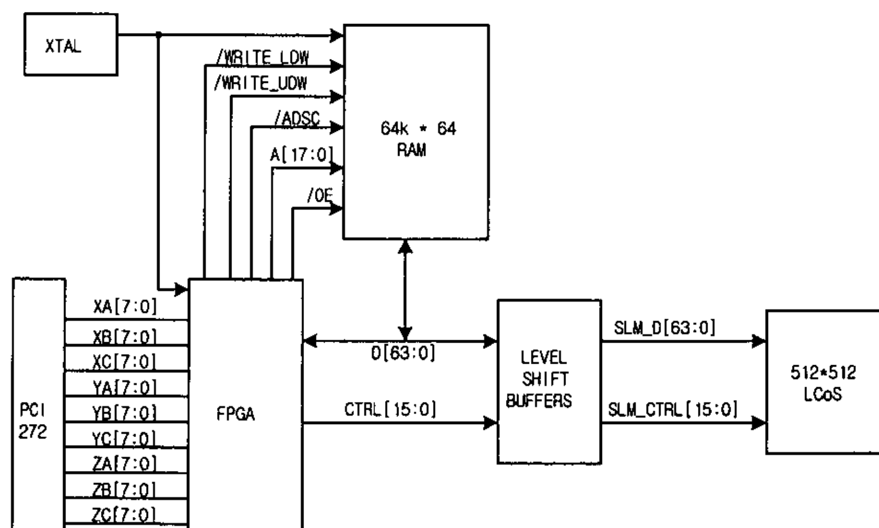


Fig. 6.10: Block diagram of 512×512 LCoS interface board

Circuit design tools

To design the control circuit for driving the LCoS backplane with nematic liquid crystals, a simulator (ModelSim SE 5.5 version) was used using a source code which was written in very high speed hardware description language (VHDL). The basic source code used in this study was optimized by a 4th year project student in the department of Physics & Astronomy at the University of Edinburgh to drive FLCoS backplanes [140]. ModelSim provides all of the various digital circuit timing and has a debugging capability in gate-level optimization. ModelSim was used for both functional simulation (code development) and post layout simulation (estimate the result after downloading the 'rawbits' file to FPGA) of the VHDL code. Functional simulations were executed using a testbench file with source code files. The output of the functional simulation includes a timing diagram of signals which is a very useful reference for developing the expected VHDL code.

A synthesis tool (FPGA Compiler II) was used to create a FPGA implementation file from the VHDL code. FPGA Compiler II synthesizes the FPGA design and integrates the output file (netlist format and constraints) that interface with the FPGA chip. As only the 'rawbits' format was available to download to the FPGA, the Xilinx software (Xilinx Alliance Series 3.1) was used to transform the 'rawbits' format from the netlist format. The Xilinx tool can often detect additional errors even if the VHDL code is successfully synthesized in the FPGA Compiler II.

A customized graphic user interface programme (written in Visual Basic) was used to download the 'rawbits' file and image data to the interface board.

Driving scheme development

The driving scheme defines how the backplane is addressed and how the memory loading sequence is synchronized. To produce multi-phase modulation, it was decided to use eight bit-planes that are normally used for driving an eight-bit grayscale (256-grey levels) display. The waveform-timing scheme in Fig. 6.11 shows the DC balanced PWM for multi-level phase modulation. The calculations for this

timing diagram were based on the 50 MHz (20ns) clock frequency which is set by the clock speed (oscillator) on the interface board.

In the timing diagram the signal DATA shows eight bit-planes in which each bit plane is a 512 × 512 array of data, and consists of both addressing period (0.18ms) and blanking periods (2μs). In the normal LC microdisplay, the blanking period can be used as an illumination time whose duration is varied in accordance with the number of bit planes. The ratio of the illumination times are $1 : 2 : 2^2 : 2^3 \ldots : 2^{(\text{number of bit-planes}-1)}$. The combination of this illumination times produces $2^{(\text{number of bit-planes})}$ of grayscale. In this study, however, I needed constant periods of each bit-plane time to produce equally divided pulse widths for multi-level phase modulation.

A three bit-width counter (BC_q0, BC_q1, BC_q2) is used to select each bit plane in the framestore.

In Fig. 6.11 the signal IID, which is placed in front of data input of each DRAM pixels, can invert or non-invert the input data, i.e. when IID is High, the input data is inverted, and when IID is Low, the data is non-inverted. This achieves DC balanced addressing with positive and negative addressing cycles which is necessary for liquid crystal displays. If DC balanced addressing is not applied the liquid crystal can be damaged and results in image sticking on the display.

Figure 6.12 represents the timing diagram of the DC balanced PWM in case of 50% of duty ratio. The signal ME represents the applied voltage to the mirror electrode and the signal FE controls the front electrode voltage. The signal ME-FE in Fig. 6.12 represents the voltage applied across the liquid crystal layer which is located in between the front and the mirror electrode.

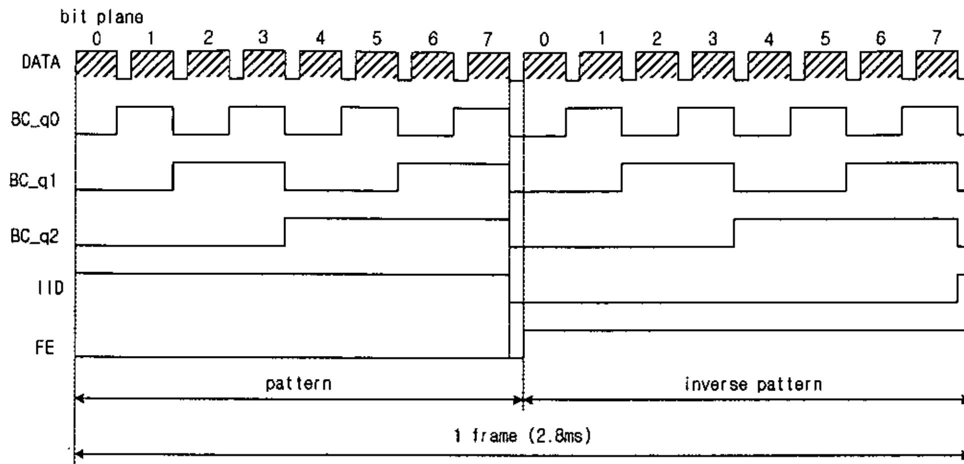


Fig. 6.11: Timing diagram of DC balanced pulse-width modulation

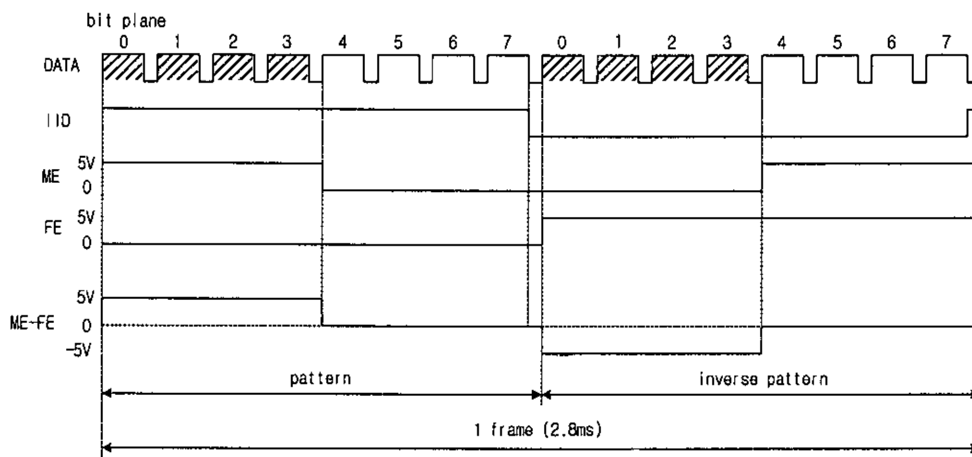


Fig. 6.12: Timing diagram of DC balanced pulse-width modulation (50% duty ratio)

The phase-modulation characteristic of the 512 NLCSLM was measured using a He-Ne laser at 632.8 nm (see Fig. 6.8). Figure 6.13 shows output fringe patterns obtained with a range of duty-ratios, generated by different gray area patterns, i.e., the upper half area had the zero duty ratio (gray level 255) and the bottom half area had an arbitrary duty ratio (gray level between 0~254). Thus the relative phase shift caused by the different duty ratios can be obtained by observing the fringe shift of the bottom half area with respect to the fringe in the upper half area. The phase shift $\Delta\phi$ in degrees between top and bottom area can be measured by:

$$\Delta\phi = 2\pi \times \frac{x}{d} \tag{6.2}$$

where, d is the period of fringe pattern and x is shifted distance of the pattern between two different patterns. It can be observed that the fringe clearly shifts between the different duty ratios and by more than a 2π-rad shift at 0.375 duty-ratio with a 5-V drive voltage.

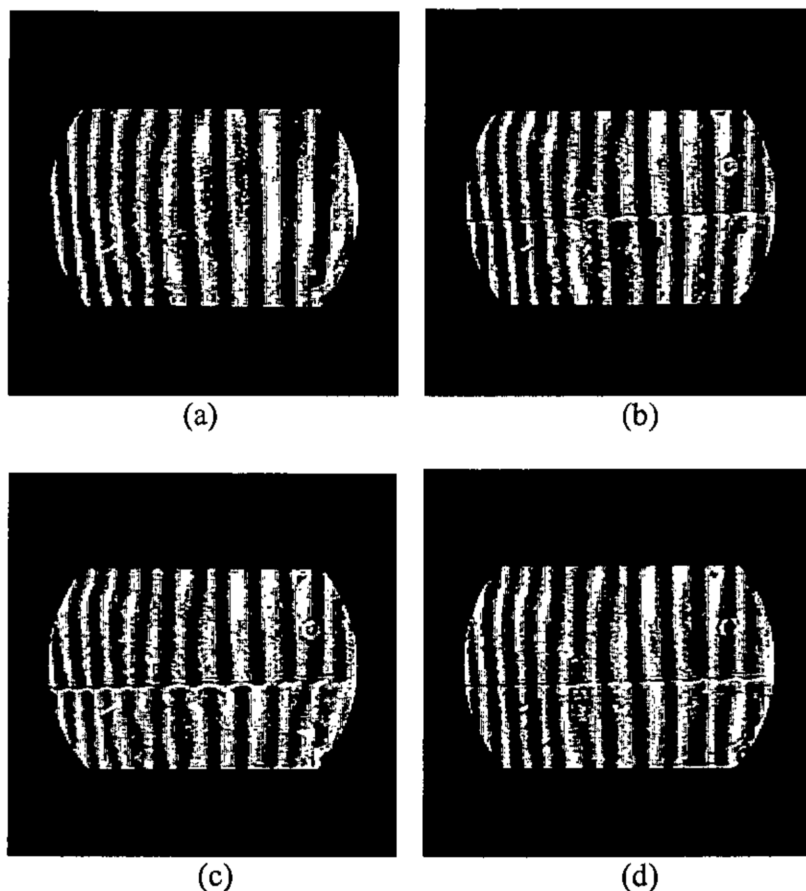


Fig. 6.13: Measured fringe patterns from the phase-measurement setup (a) zero phase shift (duty-ratio difference 0). (b) 0.25π phase shift (duty-ratio difference 0.125). (c) 1.07 π phase shift (duty ratio difference 0.25). (d) 2.1π phase shift (duty ratio difference 0.375).

The results of detailed phase-shift measurements are shown in Fig. 6.14, which gives the phase-modulation properties for duty ratio differences type of ranging between 0 and 1. It is possible to achieve around 6π phase modulation with this PWM driving.

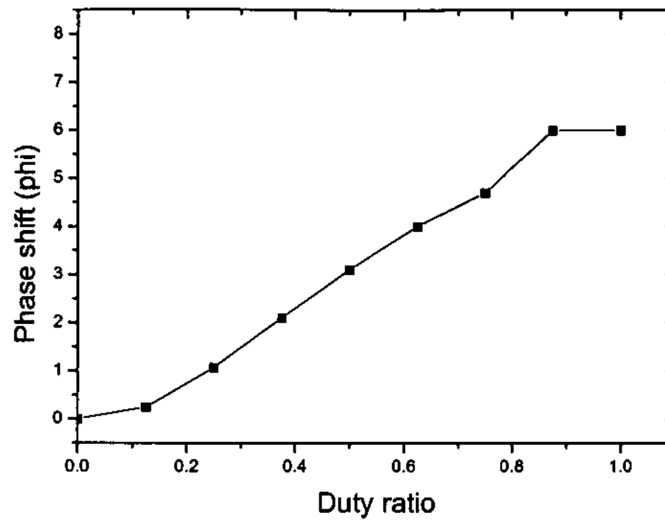


Fig. 6.14: Phase-shift properties of 512×512 NLC SLM as a function of duty ratio

6.4 Characterization of 2π phase modulation

In practical optical applications we only require a 2π phase modulation. We can therefore choose the most linear region, that between a duty ratio of 0.375 and 0.625 which gives a 2π phase shift with a duty ratio difference of 0.25 as shown in Fig. 6.15.

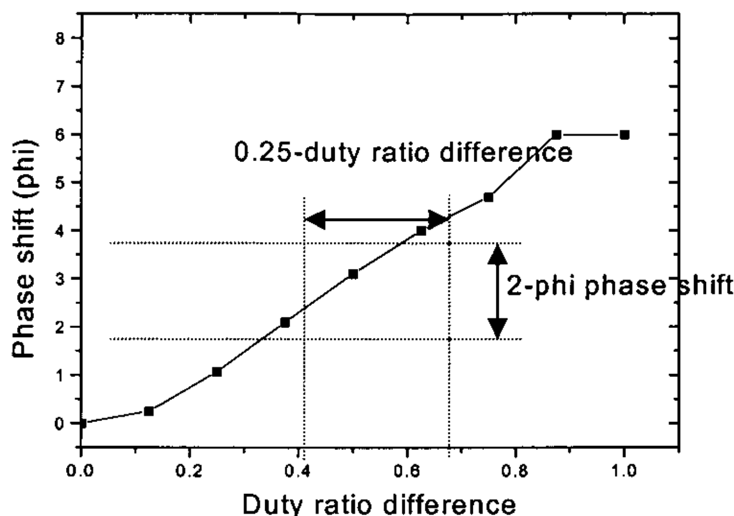


Fig. 6.15: Adjustment to 2π phase shift using the diagram of 512×512 NLC SLM phase-shift properties

Figure 6.17 shows the waveform timing for the revised driving scheme. The degree of phase shift can be controlled by adjusting the blanking time. To produce 2π phase shift, we need a long blanking time after bitplane7 addressing. To change the blanking time, the driving circuit was redesigned using a multiplexer as shown in Fig. 6.16. The loop_counter7 produces the blanking time (4.2ms) after bitplane7 addressing and ViewInvDel_counter produces the blanking time (2μs) after bitplane 0~6 addressing. Each data addressing time (bitplane0~bitplane7) is set to 1.42ms and the time for a frame is set to 11.24ms. During the blanking period after bitplane7 alternating voltage must be applied to the front electrode so that the NLC material responds to the RMS value of the alternative field. If the alternating frequency is not high enough, the NLC material follows the alternating field and phase modulation cannot be achieved. With this new driving scheme, exact 2π phase modulation was achieved with four different phase levels.

To get more than four phase levels, the most important factor is the number of data bit planes in data address time. If the driving scheme is designed with higher number of data bit planes, more phase levels can be achieved. The frame rate, the choice of NLC or different mode of cell construction would be less effective to achieve higher

phase levels.

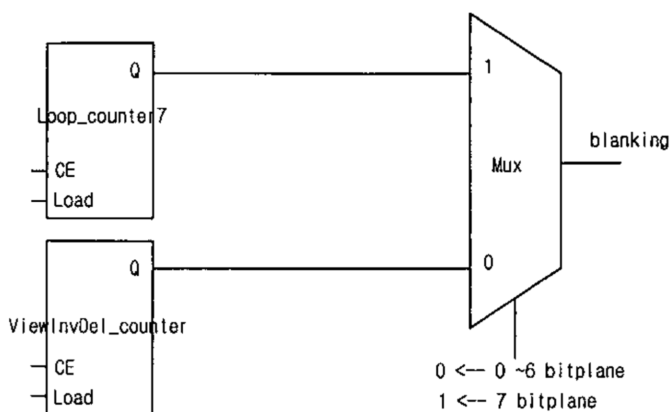


Fig. 6.16: Circuit design for blanking timing

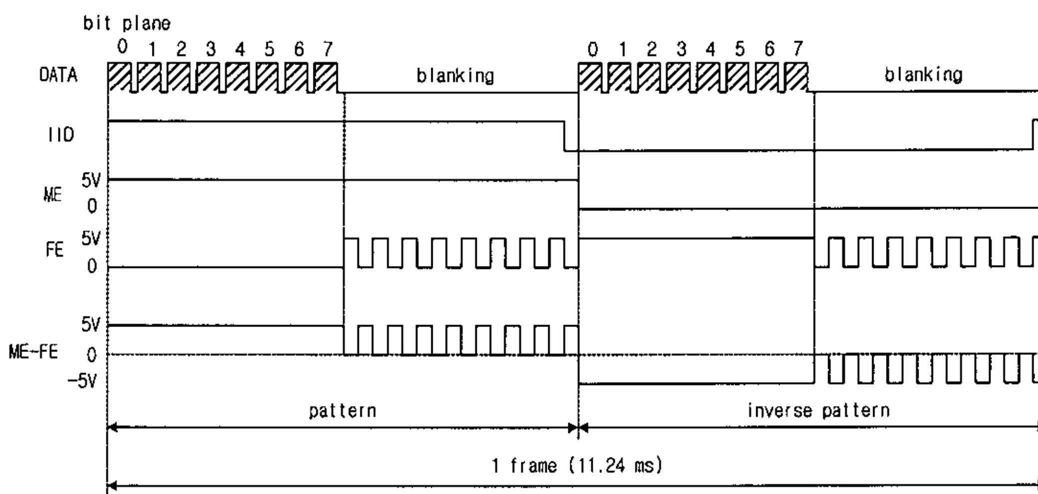


Fig. 6.17: Timing diagram of the driving scheme for 2π phase modulation

6.5 Modulation performance

6.5.1 Diffraction efficiency

Diffraction efficiency characteristics for a binary and four-level phase grating on the SLM were measured using the setup in Fig. 6.18. A He-Ne laser (10mW power) with wavelength of 632.8 nm was collimated by a lens (f = 200mm), and the polarization direction of the collimated light was adjusted to the direction of LC molecules using a polarizer. The Fraunhofer diffraction pattern of the light was observed with a 1000-

mm focal-length lens. An optical power meter with an aperture in front of the detector was used to measure the intensities of the diffracted orders. A 1.5mm-diameter pinhole was used to isolate a single diffracted peak in the replay field for measurement on the optical power meter.

Efficiency measurements of the optical system were performed on the SLM. The light intensity from the laser source at the SLM was 2.5 ± 0.2μWcm^{-2} and total light intensity at the Fourier plane was 255 ± 10 nWcm^{-2}. The light intensity in the DC spot was 135 ± 5 nWcm^{-2}. From the measured values, the overall system efficiency (light from laser source / light in DC spot) was 5.4% and the reflected diffraction efficiency (light from Fourier plane / light in DC spot) was 53%.

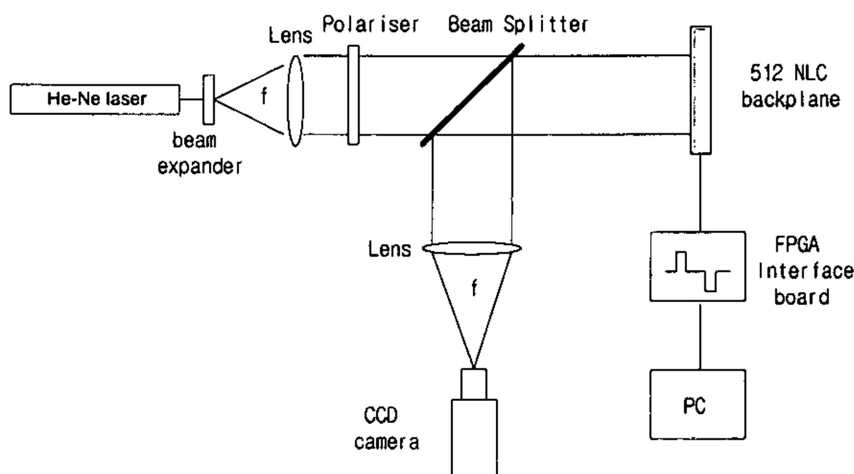


Fig. 6.18: Measurement setup for diffraction efficiency

The 1st order diffraction efficiency is defined as,

$$\eta_1 = \frac{I_1}{I_0} \tag{6.3}$$

where, η_1 is the diffraction efficiency into the 1st order, I_0 is the intensity of the zeroth order without modulation, and I_1 is the intensity of the first order. The drive voltage to the SLM was 5.5 V. The diffraction efficiency increases as the phase level is increased because more power can be diffracted into a single order. The efficiency is

given by the equation (6.1).

As a test of binary phase performance, a one-dimensional periodic phase grating was displayed on the SLM by altering the phase 0 and π. For the four-level phase performance a one-dimensional blazed phase grating was displayed of four periods, (zero, $\pi/2$, π, and $3\pi/2$ in sequence). Figure 6.19 shows the phase gratings and each grating has the same spatial frequency of 0.78 line pairs per mm. The actual grating patterns for the 512×512 SLM are shown in Fig. 6.20. The resolution of the SLM is 50 pixels mm^{-1}.

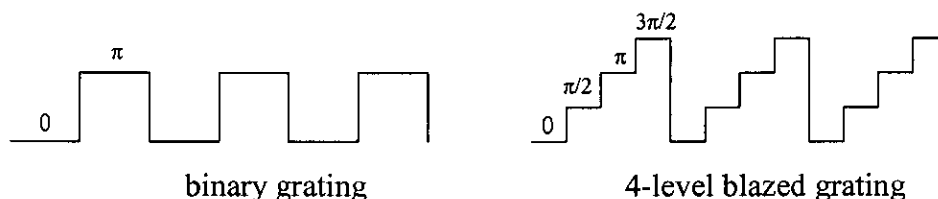


Fig. 6.19: Phase grating patterns

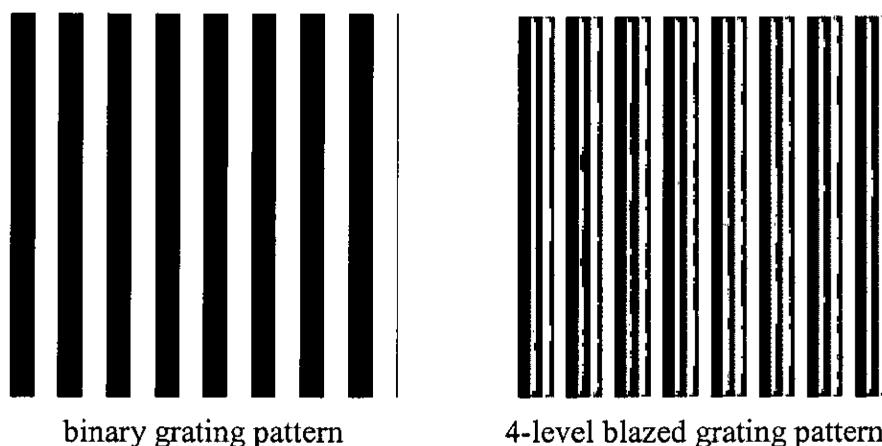
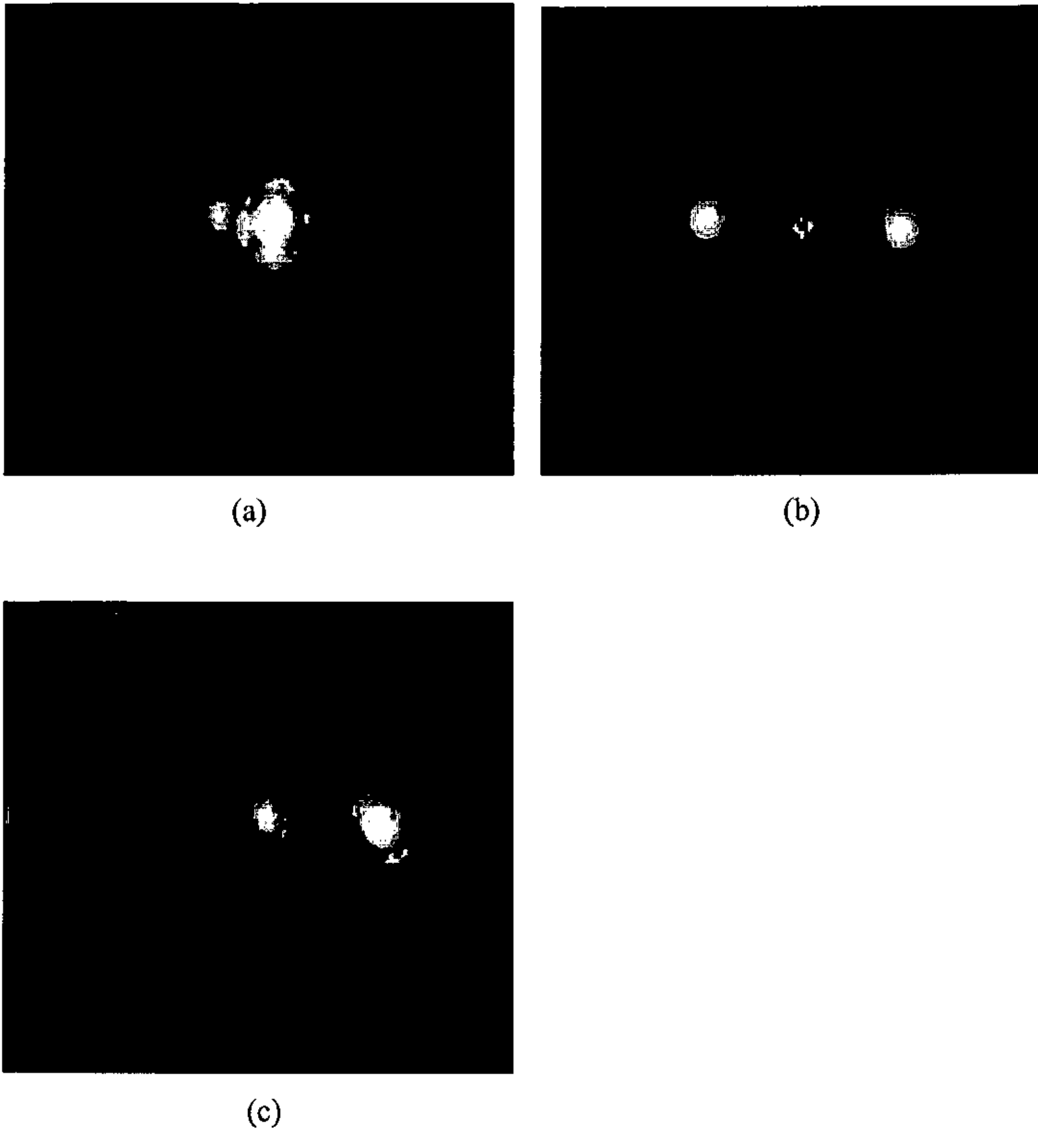


Fig. 6.20: Actual grating patterns for 512×512 SLM (0.78 line pairs per mm)

Figure 6.21(a), (b) and (c) show diffraction patterns for no modulation, binary grating and 4-level blazed grating, respectively. Table 6.2 shows the experimental results of the 1st order diffraction efficiency and simulated values for binary grating and 4-level blazed grating. The diffraction efficiency was 39.7% for the binary

grating and was 72.7% for the 4-level blazed grating (at the spatial frequency 0.78 line pairs per mm). As expected from the theoretical values, the diffraction efficiency increased as the number of phase levels rises from binary to four levels.



(a) (b)

(c)

Fig. 6.21: Diffraction patterns (a) no modulation (DC spot). (b) binary grating. (c) 4-level blazed grating.

	simulated values	measured values
binary grating	40.5 %	39.7 ± 1 %
4-level blazed grating	81.1%	72.7 ± 2 %

Table 6.2: Measurement of the 1st order diffraction efficiency

Diffraction efficiency generally decreases as the spatial frequency is increased (period length is decreased). This is mainly because SLM devices tend to decrease the response at high spatial frequencies [137] [141]. Bouvier and Scharf have also found that the phase profile changes from nearly binary to sinusoidal when the spatial frequency is increased. The limit of spatial resolution results in the decrease of diffraction efficiency [142]. Figure 6.22 shows the measured diffraction efficiency for the first order diffraction lights with various spatial frequencies. The spatial frequency was varied between 0.78 lines per mm and 6.25 line pairs per mm in both for the binary and 4-level blazed grating. The diffraction efficiency decreased from 39.7% to 34.8% for the binary grating and also decreased from 72.7% to 40.1% for the 4-level blazed grating. Although the diffraction efficiency in both cases decreases as the spatial frequency increases, it was found that the diffraction efficiency of the 4-level blazed grating decreases more than the diffraction efficiency of the binary grating. It is believed that the larger decrease associated with the 4-level blazed grating comes from the limit of spatial resolution which is more sensitive to spatial frequency than the binary grating.

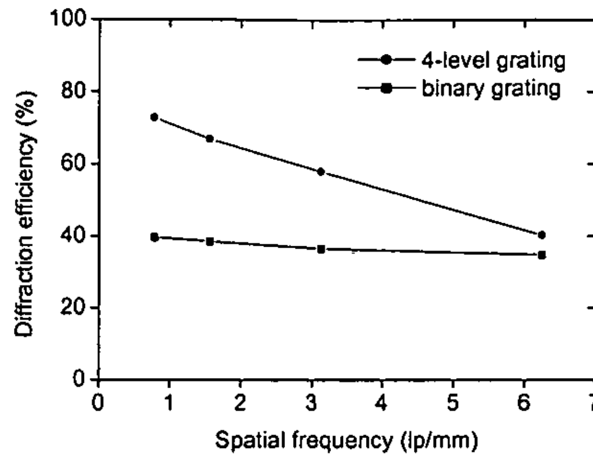
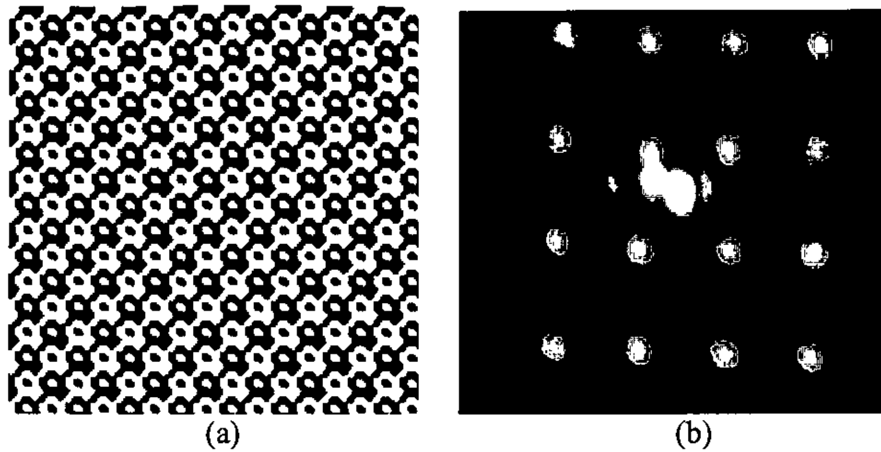


Fig. 6.22: Measured diffraction efficiency as a function of grating spatial frequency

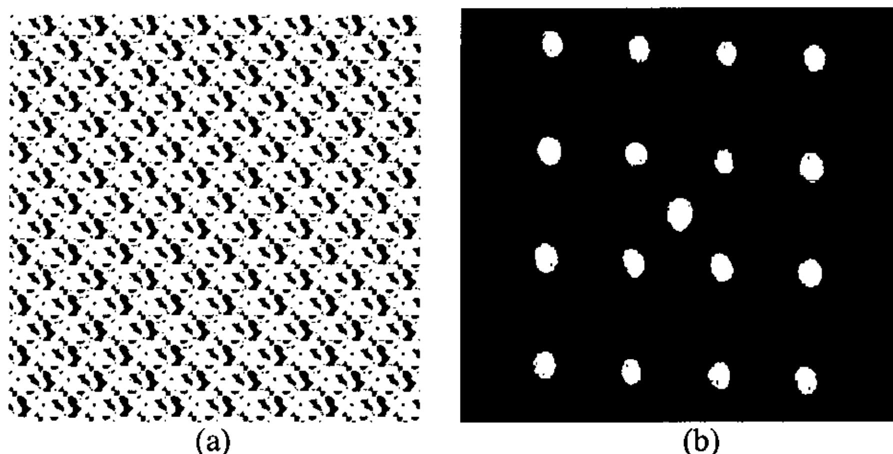
6.5.2 Computer Generated Holograms (CGHs)

The optical setup for the replay field of CGHs with the Si-backplane SLM is shown in Fig. 6.18. For capturing the replay field pattern the optical power meter was replaced by a CCD camera. Fig. 6.23 (a) shows the binary hologram for 4×4 spot array displayed on the Si-backplane SLM and Fig. 6.23 (b) shows the replay field of the binary hologram captured with a frame grabber. The four-level phase hologram for 4×4 spot array is shown in Fig. 6.24 (a) and its replay field was also captured with a frame grabber as shown in Fig. 6.24 (b). There was no temporal wobble or noise on the holograms. A DC spot is observed in both figures because any uneven shapes on the surface of pixels and dead spaces between the pixels cause higher order diffraction that results in noise in zero order. It can be observed that the replay field of four-level phase hologram shows a much clearer and brighter spot size pattern than the replay field of binary hologram. The result demonstrates that diffraction efficiency of four-level phase modulation is superiors to that of binary phase modulation.



(a) (b)

Fig. 6.23: (a) binary hologram for 4×4 spot array. (b) replay field generated by writing the binary hologram on the 512×512 SLM.



(a) (b)

Fig. 6.24: (a) four-level phase hologram for 4×4 array. (b) replay field generated by writing the four-level phase hologram on the 512×512 SLM.

6.6 Conclusions

A Si-backplane NLC SLM has been developed that is capable of multi-phase modulation using pulse-width modulation driving. Successful four-level phase reconstructions have been demonstrated using the binary Si-backplane SLM. The diffraction efficiency increases as the number of phase levels rises from binary to four levels as predicted from the theory. A diffraction efficiency of 39.7% was obtained for binary grating and 72.7% for four-level blazed grating at the spatial frequency 0.78 line pairs per mm. Diffraction efficiency characteristics for the spatial frequency have been examined for both binary and four-level blazed grating. This found that the diffraction efficiency of the four-level blazed grating decreases more

than the diffraction efficiency of the binary grating although the diffraction efficiency in both cases decreases as the spatial frequency increases. This is because the limit of spatial resolution in four-level blazed grating is more sensitive to spatial frequency than binary gratings. Hologram replay characteristics of the SLM were also examined by displaying the binary hologram and four-level phase hologram of 4×4 spot array. This demonstrated that the replay field of four-level phase hologram shows a much clearer and brighter spot size pattern than the replay field of a binary hologram. These results confirm that the diffraction efficiency of four-level phase modulation is superior to that of binary phase modulation.

Chapter 7:
Conclusions and Future work

7.1 Introduction

In this concluding chapter the work presented in this thesis will be summarized, and some ideas for future work will be discussed. The objective as reported in this thesis was to optimize the optical phase modulating properties of LC-on-silicon devices for non-display applications by considering gap-fill oxide deposition processes, modelling of ferroelectric liquid crystal with an equivalent electronic circuit, and characterization of multi-phase levels in nematic liquid crystal with pulse width modulation.

7.2 Characterization of inter-metal dielectric deposition processes

For the highly planarised surface of a LC-on-silicon device, an effective deposition technique for void-free oxide deposition was characterized. The trench-filling capabilities of ECR CVD and pyrolytic CVD techniques were compared using a scanning electron microscope. Then it was demonstrated that the trench-filling capability of ECR CVD was better than that of the pyrolytic CVD.

The effects of ECR CVD parameters on the trench-filling properties have been investigated. The following results were obtained by varying the ECR CVD parameters such as chamber pressure, magnet current, specimen-table height, DC bias voltage, Ar gas flow rate, and reactant gas flow rate. The trench-filling ratio (*R*) increases as the chamber pressure decreases (4mT – 1.3mT) because fewer ion collisions in the chamber result in highly anisotropic ion directionality and increase the deposition rate (D_b) in the trenches. The ratio (*R*) also increases as the magnet current increases (100A – 120A) because it maintains a large volume of plasma and

produces more ions in a near-vertical direction in the chamber, which results in higher deposition rate inside trenches. For the specimen-table height, the ratio (*R*) decreases as the table height decreases (100mm – 30mm). This effect seems to be an increase in arrival angle of the ions on the substrate, which results in the higher deposition rate on the sidewall of trenches. The ratio (*R*) increases as both the DC bias voltage (-200V – -300V) and Ar flow rate (0sccm – 50 sccm) increase. The DC bias voltage and Ar flow rate assist to increase the sputter rate, which helps to maintain the trench open. Even though the ratio (*R*) increases considerably as the reactant gas flow rate decreases (N_2O: 35 sccm – 17.5 sccm, SiH_4/He: 100sccm – 50sccm), the deposition rate decreases to an impractical level.

Choosing the ECR CVD parameter values that produce the better trench filling, an improved recipe was proposed for application to the planarisation of LCoS devices. Using the improved recipe, it could be achieved that a planarised surface profile on a silicon backplane in a single process cycle without the need to repeat the oxide deposition / CMP process.

Suggestions for further work specific to this project are outlined below.

(1) The microwave power may be an important parameter in the trench filling capability. In the present study the microwave power was held constant at 280W. However there is evidence that there is a dependence of deposition rate of the flat on microwave power but that the side etch rate is not affected when silane, oxygen, nitrogen and argon are used [105]. An improvement can be made if the effect of microwave power is investigated in the present ECR system where SiH_4/He and N_2O are the feedstock gases.

(2) Oxide deposition using plasma enhanced (PE) CVD technique instead of ECR CVD technique may be considered to be investigated for the improvement of trench filling. The only difference to ECR CVD system is that PECVD system uses rf power instead of microwave power for ECR CVD. Even though the required power of PECVD to generate a high density of plasma is much higher than that of ECR CVD, PECVD technique can achieve higher deposition rates than ECR CVD technique [101]. A PECVD

system was not available at the time of this study in our department.

7.3 Modelling of binary phase modulation on FLC-SLMs

An electronic equivalent circuit model has been presented to describe the electro-optical properties of an SSFLC cell for binary phase modulation. This model can be provided for characterization of phase modulation properties for designing FLC-on-silicon SLMs. The model required experimental measurement techniques: phase modulation on a reflective SLM and modeling parameters such as rotational viscosity, chevron tilt angle and restoring torque of the FLC material, since the values of the parameters are changed depending on cell construction. Phase modulation on a reflective FLC cell was measured a measurement technique based on Fizeau interferometer system.

To test the model performance, comparisons were made between the measured and simulated values of phase modulation of reflective FLC cells. Reasonable agreement within 9% of the phase modulation results, for both sets of samples, has shown that the quality of the cells is reproducible.

Further investigations could improve this model:

1) The FLC parameters used in this simulation are temperature dependent [156]. The modelling parameters such as rotational viscosity, spontaneous polarisation, chevron tilt angle and restoring torque at different temperatures would affect switching performance and director orientation.
2) In my model, the switching angle (Ψ) between the projection of the director onto the FLC cell plane and the alignment direction does not include the pre-tilt angle (α) of the alignment surface as a parameter. It was difficult to measure the pre-tilt angle [143] [144] in our lab, so the pre-tilt angle could not be used as a parameter in this model. If we take into account the parameter in this model we have to use a different equation as the parameter for the switching angle (Ψ). Further study is needed since the pre-tilt angle may have a considerable influence on the electrooptical properties of the FLC

cell.

3) The effect of anchoring strength can be incorporated to the model since the polarisation reversal current is different for different anchoring conditions at the alignment surfaces such as rubbing strength, polar and non-polar interaction [123] [145]. It is known that double peaks appear in the polarization reversal current due to the delay in polarisation reversal at the alignment surface or the chevron interface relative to that in the bulk.

7.4 Multi-phase modulation for nematic LCoS SLMs using PWM driving

The objective was the development of a PWM driving scheme to drive a binary CMOS backplane and characterize multi phase modulation with NLC SLMs driven from the binary CMOS backplane. The first step was to characterize the phase modulation ability of the NLCSLM. After the phase modulation was characterized with pulse-width modulation driving, the information was used to create and encode multi-level phase modulation. A demonstration was performed using the binary and four-level phase quantization and the benefits of using multi-phase quantization were observed.

As expected from the theoretical values, the diffraction efficiency increased as the number of phase levels rises from binary to four levels. Measured diffraction efficiency of 39.7% for binary grating and of 72.7% for four-level blazed grating at the spatial frequency 0.78 line pairs per mm were obtained. Diffraction efficiency characteristics for the spatial frequency have been examined for both binary grating and four-level blazed grating. The diffraction efficiency of the four-level blazed grating was decreased more than the diffraction efficiency of the binary grating although the diffraction efficiency in both cases decreased as the spatial frequency increased. This is because the limit of spatial resolution in four-level blazed grating is more sensitive to spatial frequency than binary grating. It was also demonstrated that the replay field of a four-level phase hologram shows a much clearer and brighter spot size pattern than the replay field of a binary hologram. The results

confirmed that the diffraction efficiency of four-level phase modulation is superior to that of binary phase modulation. A Si-backplane NLC SLM was successfully developed that is capable of multi-phase modulation using pulse-width modulation driving.

Future work should include the following,

1) One of the most common problems in LCoS devices is the large fringe field due to their small pixel geometry. The electric field near the edge of the pixel electrode becomes inhomogeneous and may cause reorientation of the LC molecules in the reverse tilt directions [142] [146] [147]. The molecules may take longer time to relax back to the original state and show different light transmission in the switching-off process. The effects of the fringe-field-induced disclination on phase modulation characteristics cannot be neglected.
2) Unsymmetrical electrodes (ITO and Al) across the LCoS devices cause problems for the SLM quality. There are two problems associated with the Al electrode: work function difference between the Al and ITO electrodes [148], and charge trapping [149] between polyimide film and the LC mixture. The effect of unsymmetrical electrodes on phase modulation properties can be investigated.
3) In this research, four-level phase modulation was achieved with new PWM driving scheme. If the driving scheme is designed with higher number of data bit planes, more phase levels can be achieved.

7.5 Concluding Remarks

LCoS devices have been developed recently for phase modulating applications because the devices can be made optically flat, and small enough for matching with small optics. Although future work needs to be carried out, this study has demonstrated many advantages and great potential of LCoS devices for coherent optical systems. It is hoped that the work presented here is an initial characterization showing that LCoS devices can be used in phase modulating optical systems and that they will play a major role in future work.

Appendix

Appendix I. Diffraction theory for SLMs

When a beam of light is partially obstructed by an obstacle, some of the light is diverted sideways, which is known as diffraction. Depending on the distance between an object screen and the diffracting aperture plane, there are two types of diffraction: Fresnel and Fraunhofer. If the distance between the object plane and the aperture plane is greater than 100×(aperture area / optical wavelength), the diffraction will be Fraunhofer. We can use the Huygens-Fresnel integral equation for modeling of diffraction patterns written as,

$$E(P) = \frac{j}{\lambda} \int_{\Sigma} E(M) \frac{e^{-jkL'}}{L'} d\sigma$$

where E is the complex intensity of the field, P is the object point, M is a point on the surface of an aperture, L' is the distance between the points M and P, λ is the optical wavelength, and k is the wave number. Suppose that we have a 2-dimensional aperture located in the plane z =0. The light passing through the aperture will be diffracted at its edges and the intensity distribution at the point P on the $x_0\, y_0$ plane can be calculated.

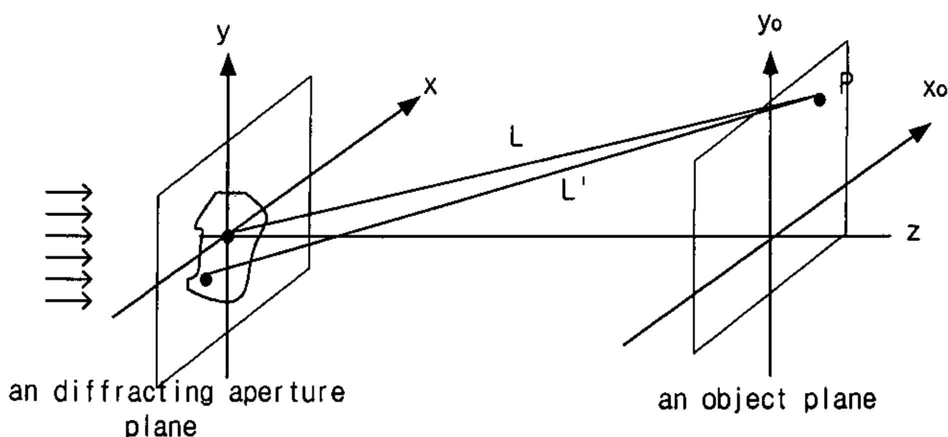


Fig. A.1: diffraction of light by an aperture on an object plane

According to the coordinate system in the figure we can define the parameter L' as

$$L' = \sqrt{z^2 + (x - x_0)^2 + (y - y_0)^2}\,.$$

Dealing with narrowly diverging beams of light, we can put the distance z >> x, y, x_0, y_0. Using the condition we can regard the distance L' as

$$L' = L + \frac{x^2 + y^2}{2L} - \frac{xx_0 + yy_0}{L}$$

The diffraction optical field at the point P can be expressed as

$$E(P) = \frac{j}{\lambda L} e^{-jkL} \int \int_{-\infty}^{\infty} E_0(x, y) e^{jk(x_0 x + y_0 y)/L} dxdy$$

The general expression for far-field diffraction will be

$$E(k_x, k_y) = \frac{j}{\lambda L} e^{-jkL} \int_{-\infty}^{\infty} \int_{-\infty}^{\infty} E_0(x, y) e^{jk(k_x x + k_y y)} dxdy$$

$$= \frac{j}{\lambda L} e^{-jkL} E_0(k_x, k_y)$$

where $k_x = kx_0/L$, $k_y = ky_0/L$.

The spatial spectral distribution $E_0(k_x,k_y)$ corresponds to the Fourier transformation of the aperture field distribution $E_0(x, y)$. According to the two dimensional Fourier Transformation, the time domain $f(x,y)$ maps to the frequency domain $F(u,v)$ which coordinates the spatial frequencies in the Fourier plane.

$$F(u, v) = \iint_{\pm\infty} f(x, y) e^{2\pi j(ux + vy)} dxdy$$

$$f(x, y) = \iint_{\pm\infty} F(u, v) e^{-2\pi j(ux + vy)} dudv$$

Hence, the far-field diffraction $E(k_x,k_y)$ is also related to the Fourier transformation of the aperture field distribution $E_0(x,y)$.

In practical applications the far field distance L limits the fabrication of an optical system, so it is needed to shorten the distance. If a positive focal length lens is located after the aperture plane, as shown in Fig. A2, the far-field pattern (a Fourier transform of the aperture) appears in the focal plane of the lens. If the aperture field $E_0(x,y)$ is located just in front of a positive lens of focal length f, then the field after lens can be calculated by the paraxial approximation [150]

$$E_0(x,y)' = E_0(x,y)e^{-j\frac{\pi}{\lambda f}(x^2+y^2)}$$

This equation implies that the far field pattern occurs at the focal plane of the lens. If the lens is located a distance d from the aperture plane, then the diffracted pattern for the field $E_0(x,y)'$ includes phase distortion of the Fourier transform. However the phase distortion can be reduced when the distance is set to $d=f$.

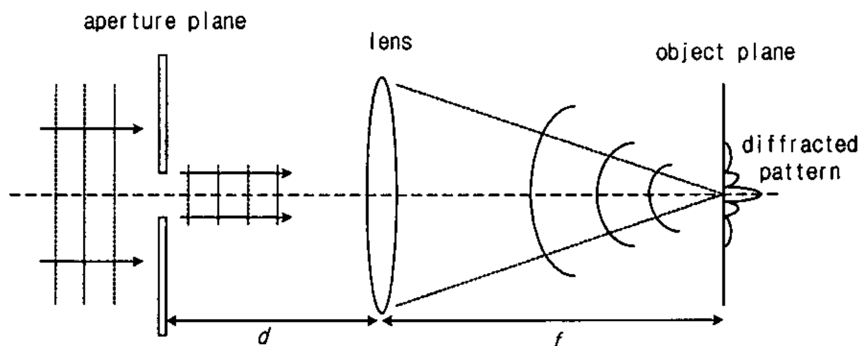


Fig. A.2: Optical system for producing Fraunhofer diffraction. An aperture plane is placed a distance d in front of a lens with focal length f and illuminated with plane waves.

In these optical processing systems it is essential to understand the Fourier transform properties of the system. A couple of points concerning the Fourier transforms of

SLMs are summarized as below [151].

- Resolution: The maximum spatial frequency is determined by the aperture in the input plane. It is defined as $\omega_0 = Nd/2\lambda f$, where N is number of pixel, d is separated distance between pixels, λ is the wavelength of light, f is the focal length of the lens.

- Zeroth order: Light going straight through the SLM without deviation is in the zeroth order. Light is diffracted out of the zeroth order due to the pixellated input data. This reduces the intensity in zeroth order.

- Replication: Since the Fourier transform of a Tophat function is a sinc function, the pixellated SLM produces an infinite number of replicated orders. The power in the orders can be found using the pixel function's transform. The Fourier transform of the rectangular pixel function is $[sinc(\pi ax)\ sinc(\pi bx)]$,where a is horizontal pixel width and b is vertical pixel width. The replications will be positioned at $x_n = m/d$, $y_n = n/d$, for $m, n = 0, \pm1, \pm2, \ldots$

- Noise: Any imperfections in the surface causes higher order diffraction, resulting in noise in the zeroth order.

Appendix II. Computer generated holograms for SLMs

Holograms are devices that store the intensity and phase of a wavefront emanating from an object. For visible light, recording both intensity and phase needs a reference wave that is coherent with the object's wave. The two waves interfere and produce fringes that encode the intensity and phase of the object wave. When the reference wave illuminates the hologram, the diffracted field contains the object wave so an image can be produced from the data stored in a hologram. Computer generated holograms (CGHs) are very useful for calculating the far-field in two-dimensional optical information-processing systems. If we create a hologram from an array of rectangular pixels with pixel pitch d and amplitude A, the far-field diffraction pattern of the hologram is [177]

$$Ad^2 \sin c(\pi au) \sin c(\pi bv)$$

where a is the horizontal length of a pixel and b is the vertical length of a pixel. The information coding ability of CGHs can be measured by several parameters in SLMs as below [151].

- Fill factor: The dead spaces between pixels cause uncontrolled reflection, decreasing the diffraction efficiency. Hence, a higher fill factor of pixels on the SLM backplane will increase the efficiency. By using planarisation techniques, the fill factor can be increased to over 90%.

- Modulation efficiency: For optimum efficiency the phase should be altered exactly desired phase values. In reality, the fabrication conditions limit the maximum attainable efficiency. The tilt angle of a liquid crystal mainly affects the modulation efficiency. If the tilt angle is 45 , then lossless phase modulation can be achieved.

- Pixel pitch: The pixel pitch determines the separation of the diffracted orders.

The smaller pixel pitch creates the larger angle of diffraction.

- Space bandwidth product (SBWP): This is the number of pixels of a SLM. For the efficient encoding of a large amount of information the phase device should have a high SBWP.

Apendix III: HSpice simulation code for FLC equivalent circuit

```
.SUBCKT camhspice 1=IN 7=EOT 3=GIN 8=EPH 6=COUT 5=GR 2=RDC

 #echo .PARAM VSC=$mpar (VSC=260)     ;viscosity
 #echo .PARAM D=$mpar (D=2.4)         ;cell gap
 #echo .PARAM PS=$mpar (PS=28)        ;spontanious polarisation
 #echo .PARAM CAP=$mpar (CAP=8.4)     ;cell capacitance
 #echo .PARAM SIZE=$mpar (SIZE=1)     ;effective cell area
 #echo  .PARAM  INPOLAR=$mpar  (INPOLAR=-19)   ;input  polariser
orientation
 #echo .PARAM CONE=$mpar (CONE=19)        ;cone angle
 #echo .PARAM TILT=$mpar (TILT=17)        ;tilt angle
 #echo .PARAM LEAK=$mpar (LEAK=1000)      ;cell leakage resistance

 #echo .PARAM PO = ' 3.14159 * INPOLAR / 180 '
 #echo .PARAM SC = ' SIN ( 3.14159 * CONE / 180 ) '
 #echo .PARAM CC = ' COS ( 3.14159 * CONE / 180 ) '
 #echo .PARAM CT = ' COS ( 3.14159 * TILT / 180 ) '
 #echo .PARAM ST = ' SIN ( 3.14159 * TILT / 180 ) '
 #echo .PARAM CN = '  CC * CT '
 #echo .PARAM SN = '  SC * ST '

 CCOUP    1 2 1UF  ;AC coupling capacitor
 RDC      2 0 1Meg ;DC restoring resistor
 RIN      2 3 100  ;cell series resistance
 #echo CIN     3 0 ' CAP * SIZE * 1E-7 ' IC=-6.5  ;input capacitance
 #echo R1      3 0 ' LEAK * 1MEG / SIZE '        ;leakage resistance
 R2       4 0 1    ;torque sensing resistor
 R3       5 0 1G   ;DC continuity resistor
 R4       7 0 1G   ;amplitude sensing resistor
 R5       8 0 1G   ;phase sensing resistor
 #echo GR      0 5 VALUE = ' V(4,0) * 1E-4 * PS / ( VSC * D ) '
;current source for viscosity setting
 COUT     6 0 1N IC=-1         ;integrating capacitor
 ROUT     5 6 1               ;current sensing resistor
 #echo GPS     0 4 VALUE = ' COS (V(6,0)) * V(3,0) * CT '
;current source for rotational torque
 GK       0 4 PWL (1 5,0 -1.57,3.0 -1.41,2.5 -1.22,2.0 -1.05,1.5
-.79,1.0 -.53,0 .53,0 .79,-1.0 1.05,-1.5 1.22,-2.0 1.41,-2.5
1.57,-3.0)  ;voltage controlled current source for restoring torque
 #echo GIN      3 0 VALUE = ' COS (V(6,0)) * V(5,6) * PS * CT * SIZE
'
 ;input current source
 #echo EOT      7 0 VALUE = ' SIN ( 2 * ( PO - ATAN ( SIN (V(6,0))
* SC /( CN + SN * COS (V(6,0)))))) * SIN ( 2 * ( PO - ATAN ( SIN
(V(6,0)) * SC /( CN + SN * COS (V(6,0)))))) '  ;amplitude of the
light transmission
 #echo EPH       8 0 VALUE = ' 1.0 * 2 * 180 / 3.14159 * ATAN ( SIN
(V(6,0)) * SC /( CN + SN * COS (V(6,0)))) '   ;phase of the light
transmission

 .ENDS
```

Appendix IV: Matlab programme for phase shift as cell gap variations

```
================================================
Programme for the effect of cell-gap variations
================================================
clear all;

Gamma=1.0*pi
Theta_degree= -45

function [R_1, R_2] = flc(Gamma, Theta_degree)

%%%%%%%% Input===========================
%Gamma=         % gamma input = retardation
%Theta_degree=  % Theta degree
%%=========================================

Theta= Theta_degree*pi/180;
ima_i=sqrt(-1);

R_1=  -ima_i*sin(Gamma/2)*sin(Theta);
R_2= exp(ima_i*Gamma/2)*cos(Theta/2)^2
+ exp(-ima_i*Gamma/2)*sin(Theta/2)^2;


[a1,a2]=flc1(Gamma, Theta_degree);

disp(['R_1: ' num2str(a1)]);
disp(['R_2: ' num2str(a2)]);

abs_R1 = abs(a1);
abs_R2 = abs(a2);
abs_R=abs(a1+a2);

disp(['Amp_R_1: ' num2str(abs_R1)]);
disp(['Amp_R_2: ' num2str(abs_R2)]);
disp(['Amp_Result: ' num2str(abs_R)]);

ang_R1 = angle(a1)*180/pi;
ang_R2 = angle(a2)*180/pi;
ang_R=angle(a1+a2)*180/pi;

disp(['Ang_R_1: ' num2str(ang_R1)]);
disp(['Ang_R_2: ' num2str(ang_R2)]);
disp(['Ang_Result: ' num2str(ang_R)]);
```

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Author's published papers

I. Yongmin Lee, W. Parkes, G. Bodammer, and I. Underwood, "*Characterisation of inter-metal dielectric deposition processes on CMOS backplanes for liquid crystal on silicon microdisplays*", IEE Proc.-Optoelectron., Vol. 151 (1) pp.53-59, 2004

II. Yongmin Lee, J. Gourlay, W.J. Hossack, I. Underwood, A.J. Walton, "*Modelling of binary phase modulation in surface stabilized ferroelectric liquid crystal spatial light modulators*", Microelectronics Journal, Vol.35, pp.193-201, 2004

III. Yongmin Lee, J. Gourlay, W.J. Hossack, I. Underwood, A.J. Walton, "*Multi-phase modulation for nematic liquid crystal on silicon backplane spatial light modulators using pulse-width modulation driving scheme*", Optics Communications Vol. 236/4-6, pp.313-322, 2004

26 May 2004
Our ref: HW/SS/May 04/J217

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Dear Mr Lee

MICROELECTRONICS JOURNAL, Vol 35, 2004, pp 193-201, Lee et al, "Modelling of binary phase modulation in surface stabilized ferroelectric liquid crystal spatial light modulators "

OPTICS COMMUNICATIONS, Vol 236, No 4-6, 2004, pp 313-322, Lee et al, " Multi-phase modulation for nematic liquid crystal on silicon backplane spatial light modulators using pulse-width modulation driving scheme "

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Characterisation of inter-metal dielectric deposition processes on CMOS backplanes for liquid crystal on silicon microdisplays

Yongmin Lee, W. Parkes, G. Bodammer and I. Underwood

Abstract: For optimal optical performance of a microdisplay, the degree of surface planarisation of the CMOS active matrix backplane has to be superior to that of conventional CMOS. Oxide-deposition processes have been characterised to evaluate their effectiveness in planarising microdisplay backplanes. To investigate the trench-filling capabilities of the respective oxide deposition processes, the authors prepared test samples that had a set of trench patterns (1–6 μm wide) etched into 4 μm-thick thermal oxide on a Si substrate. They found that the trench-filling capability of an electron cyclotron resonance chemical vapour deposition (ECR CVD) process is superior to that of a pyrolytic CVD process. They have investigated the effects of ECR CVD deposition parameters on trench-filling properties and demonstrated the ability to produce deposited oxide layers which fill high aspect ratio trenches without producing voids.

1 Introduction

Since the 1980s a great deal of research activity has centred around the development of optical systems for information processing. In such systems spatial light modulators (SLMs) are key components for performing optical data or image processing. SLMs are devices capable of applying a spatially controlled modulation to an incident wavefront. One hybrid SLM technology combines a modulating liquid crystal layer with a CMOS-silicon active-matrix backplane. Many different SLMs [1] have been developed since the first such SLM was conceived at the University of Edinburgh in 1983 [2]. From the late 1980s onwards, it has been recognised that many liquid crystal SLMs can also be configured as miniature displays. Today the technology is called 'liquid crystal on silicon' (LCoS), and the resulting displays are called 'microdisplays'.

In a microdisplay backplane, a highly planarised and smooth surface is very important in determining its optical modulation capability. However, trenches in the backplane that are located between pixels to provide electrical isolation between adjacent pixel pads present a challenge to the backplane planarisation process. To construct the pixel pads as high efficiency mirrors with high fill factor, a planarisation process is required to flatten the dielectric layer that covers the underlying circuitry and upon which the metal for the pad is subsequently deposited and patterned as shown in Fig. 1. The degree of flatness necessary from the planarisation process is more stringent than that from the typical insulator chemical-mechanical-polishing (CMP) step [3] in a conventional CMOS process, because a highly reflective optical surface is required with large fill-factor pixels. After oxide deposition, the oxide film is polished back in the CMP process, leaving a 0.5–1 μm-thick layer above the uppermost CMOS metal layer. If voids in the oxide are located at a higher position than the top CMOS metal layer before the polishing process, there is the likelihood of exposing the voids during the CMP process. The voids in the oxide cause not only a reliability problem, with the possibility of trapped chemicals in the void, but can also cause breaks or shorting in bus lines [4] in the underlying CMOS metal layer. Several deposition/CMP cycles are often required to fill the voids; this prolongs, complicates and adds to the cost of the overall planarisation process. To reduce processing time and effort while still achieving extremely smooth surfaces, we have investigated the trench-filling properties of two oxide deposition processes on a microdisplay backplane to find the more suitable deposition technique.

In this paper, we compare the trench-filling capability of ECR CVD and pyrolytic CVD techniques. We also investigate the parameter dependent trench-filling properties of oxide deposited with an ECR CVD technique on a backplane, and report an effective deposition technique for void-free oxide deposition on microdisplay backplanes.

2 Experimental

We use wafer samples that have a set of line-width trench patterns (1–6 μm wide) etched into 4 μm-thick thermal oxide as shown in Fig. 2. A sputtered aluminium layer is used to mimic the top metal layer of the CMOS wafer as delivered from the foundry in real devices. The aluminium layer also helps to distinguish the layers between thermal oxide and deposited oxide in the measurement. A pyrolytic CVD system (Pacific Western PWS 2000) and an ECR CVD system (Oxford Plasma Technology AMR ECR system) are used to investigate trench-filling properties with SiO_2. Each of the processes has different variables that will affect the deposition properties. In a pyrolytic CVD process [5], there

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IEE Proceedings online no. 20040137

doi: 10.1049/ip-opt:20040137

Paper first received 16th April 2002 and in revised form 16th June 2003

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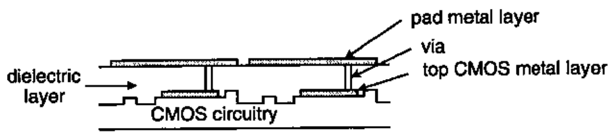


Fig. 1 *Cross-section of a microdisplay backplane*

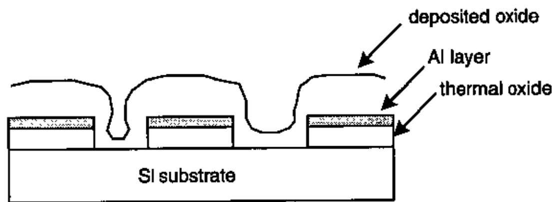


Fig. 2 *Trench patterns*

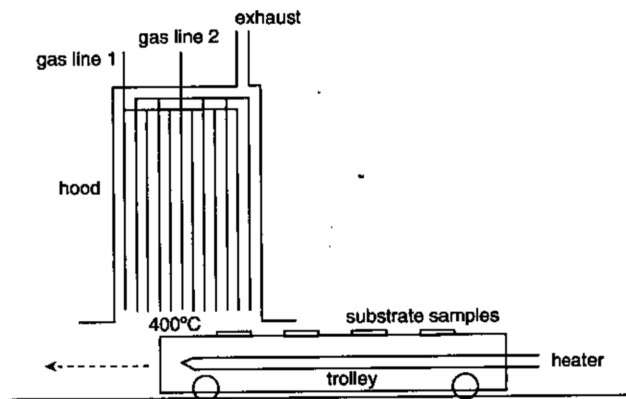


Fig. 3 *Schematic diagram of pyrolitic oxide deposition system*

Feedstock gas 1: N_2 4.0 l/min + O_2 0.65 l/min
Feedstock gas 2: N_2 2.9 l/min + 5% SiH_4 in N_2 1.3 l/min
Temperature of substrates is maintained at 400 °C
Trolley speed under the hood determines the SiO_2 thickness in a single pass

are two main variables: hot plate speed and hot plate temperature. The system is shown diagrammatically in Fig. 3.

The ECR CVD process has been described elsewhere [6, 7]. A diagram of the ECR CVD system is shown in Fig. 4. Microwave power (2.45 GHz) is introduced into the plasma chamber through a rectangular waveguide, and magnet coils are set around the periphery of the plasma chamber for ECR plasma excitation. The specimen-table height can be changed from 0 to 100 mm. The specimen-table height defines the distance from the extraction window of the plasma chamber (0 mm) to the specimen table. The table temperature is maintained at 45–50 °C. The reactant gas mixtures are introduced through two separate inlets into the plasma chamber (N_2O) and the specimen chamber (SiH_4). Non-reactive Ar gas can be introduced through the plasma chamber inlet. A DC bias is applied to the table by a 13.6 MHz RF generator through a matching circuit. Because the ECR-CVD process is more complex, we have confined our study to five major variables: the magnetic field, DC bias voltage, the table height with respect to the extraction window, chamber pressure and gas composition.

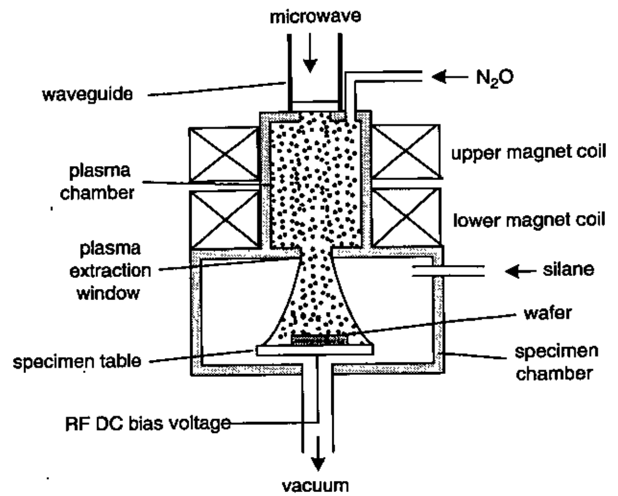


Fig. 4 *Diagram of ECR CVD system*

The parameter values of pyrolytic and ECR CVD are selected and the parameter level settings are shown in Table 1. The parameter space to be investigated was determined from known level settings. The thickness of filling oxide deposited was 3.8–4.4 µm and measured by a Nanospec spectro-reflectometer. A scanning electron microscope (SEM) is used to view the trench cross-section and to measure the trench-filling ratio and deposition rate. As shown in Fig. 5, the trench-filling ratio (R) is defined as

$$R = \frac{D_b}{D_t} \quad (1)$$

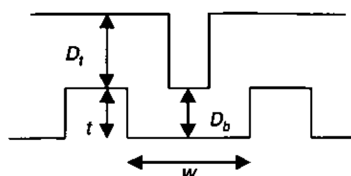
where D_b is the deposition thickness of the filling oxide at the bottom of a trench and D_t is the deposition thickness of the filling oxide at the top of trench.

We have varied the chosen parameters in both a pyrolytic deposition and an ECR CVD process to obtain the optimum conditions for trench filling. In Fig. 5 we show the relationship between the aspect ratio of trenches and the

Table 1: Variable settings of pyrolytic and ECR CVD

CVD technique	Variables	Initial conditions (Edinburgh University)	Variable level settings
Pyrolytic CVD	hot-plate temperature	430 °C	400 °C, 415 °C, 430 °C
	hot-plate speed	5.25 in/min	3.5 in/min, 5.25 in/min, 8.25 in/min
ECR-CVD	chamber pressure	4 mTorr	1 mTorr, 2 mTorr, 4 mTorr
	uppermagnet current	100 A	100 A, 110 A, 120 A
	table height	100 mm	30 mm, 65 mm, 100 mm
	DC bias voltage	−200 V	−200 V, −300 V, −400 V
	Ar gas rate	0 sccm	0 sccm, 25 sccm, 50 sccm
	reactant gas flow rate*	Normal flow rate	Normal flow rate, half flow rate

*Normal flow rate: N_2O: 35 sccm, SiH_4/He: 100 sccm, half flow rate: N_2O: 17.5 sccm, SiH_4/He: 50 sccm



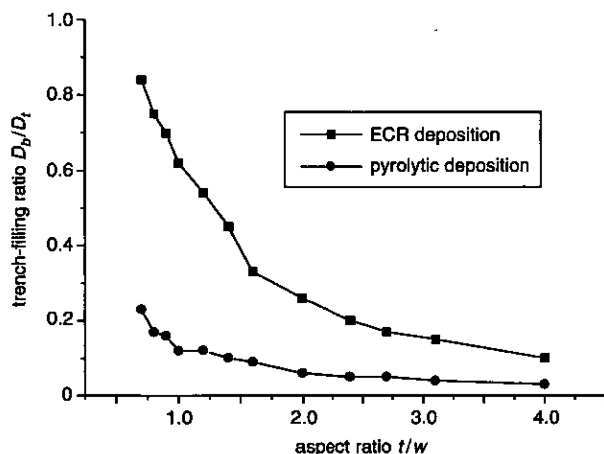


Fig. 5 *Dependence of trench-filling ratio on aspect ratio*

Table 2: Parameters of pyrolytic CVD experiments

Pyrolytic CVD experiments	Hot-plate temperature, °C	Hot-plate speed, in/min
Pyro 1	400	3.5
Pyro 2	400	5.25
Pyro 3	400	8.25
Pyro 4	415	3.5
Pyro 5	415	5.25
Pyro 6	415	8.25
Pyro 7	430	3.5
Pyro 8	430	5.25
Pyro 9	430	8.25

trench-filling ratio for both ECR CVD and pyrolytic CVD. The respective parameter values in Fig. 4 refer to the initial conditions in the third column of Table 1. We found that even when the pyrolytic parameter values were varied as shown in Table 2, there was insignificant change from the lower curve in Fig. 5 We therefore concluded that the ECR process was basically superior to the pyrolytic process.

To improve the ECR process to the point where voids were eliminated, we investigated the effects of each parameter on the trench-filling properties with ECR CVD. The parameters of each ECR CVD experiment are shown in Table 3.

3 Results

3.1 Comparison of trench-filling capability

We have compared the trench-filling capability of ECR CVD and pyrolytic CVD techniques. Figure 6 compares one representative cross-section from each process, in which the pyrolytic CVD sample exhibited a lower trench-filling ratio because the gap at the top of the trench had pinched off early in the process while the gap in the ECR CVD sample remained open during the deposition of $\sim$4 μm oxide. For an aspect ratio of 1.0, the trench-filling ratio of ECR deposition is higher than 0.6 while the ratio of pyrolytic deposition is only 0.12, shown in Fig. 4. Although the trench-filling ratio of both techniques decreases as the aspect ratio increases, the ECR deposition shows a higher trench-filling ratio than the pyrolytic deposition for all aspect ratios. We conclude that the trench-filling capability of ECR deposition is better than that of the pyrolytic deposition.

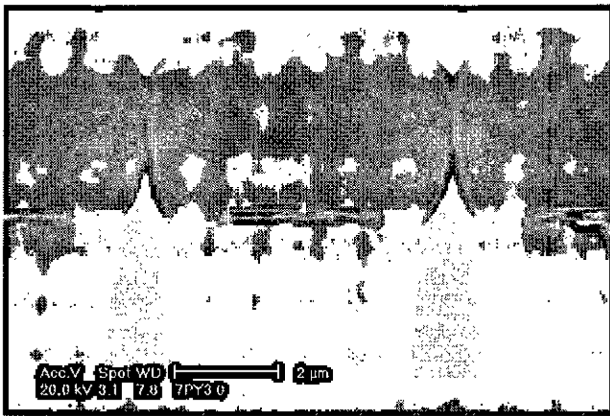
3.2 Effects of varying ECR CVD parameters

3.2.1 Effects of chamber pressure: The trench-filling ratios of ECR CVD with different chamber pressures are shown in Fig. 7. The parameters of three ECR CVD cases are shown in Table 3. Experiment 1 was the experiment with the initial recipe, and experiments 2 and 3 were experiments with lower chamber pressure. It is found that the trench-filling ratio increases as the chamber pressure decreases, as shown in Fig. 7. The lower chamber pressure causes fewer ion collisions in the chamber, which results in highly anisotropic ion directionality and increases the deposition rate in trenches. It is also found that there are smaller differences of trench-filling ratios between the chamber pressures in the higher aspect ratio range than in the lower. The deposition rate on a flat sample increases

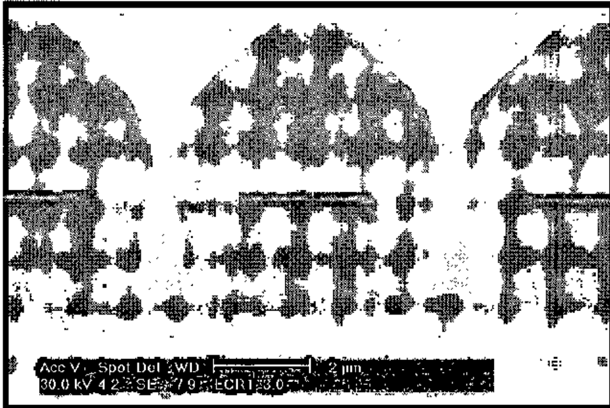
Table 3: Parameters of ECR CVD experiments

ECR-CVD experiments	Chamber pressure, mTorr	Upper magnet current, A	Table height, mm	DC-bias voltage, V	Ar gas rate, sccm	Reactant gas flow rate
Expt. 1	4	100	100	−200	0	normal
Expt. 2	2*	100	100	−200	0	normal
Expt. 3	1.3*	100	100	−200	0	normal
Expt. 4	4	110*	100	−200	0	normal
Expt. 5	4	120*	100	−200	0	normal
Expt. 6	4	100	65*	−200	0	normal
Expt. 7	4	100	30*	−200	0	normal
Expt. 8	4	100	100	−300*	0	normal
Expt. 9	4	100	100	−200	50*	normal
Expt. 10	4	100	100	−200	0	half*
Expt. 11-1	3.6*	120*	100	−300*	25*	half*
Expt. 11-2	2.1*	120*	100	−280*	0	normal

*Cells denote values which deviate from the initial conditions in experiment 1



a



b

Fig. 6 *Comparison of cross-sectional images from curves in Fig. 5 at aspect ratio 1.33 (trench width 3 µm)*
a Sample of pyrolytic CVD
b Sample of ECR CVD

slightly with the increase of chamber pressure as shown Fig. 8. The reason is that the deposition rate (at chamber pressures higher than 1 mTorr) is affected mainly by radicals rather than ions [8]. At these chamber pressures the electron temperature is high enough to dissociate silane molecules near the wafer even though both plasma density and electron temperature decrease with increasing pressure, and hence ions deliver less kinetic energy on the wafer surface for the activation of the reactions.

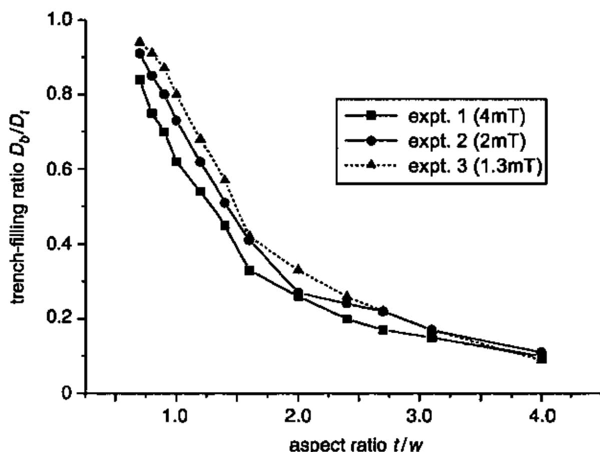


Fig. 7 *Trench-filling ratio as a function of aspect ratio, showing effects of chamber pressure*

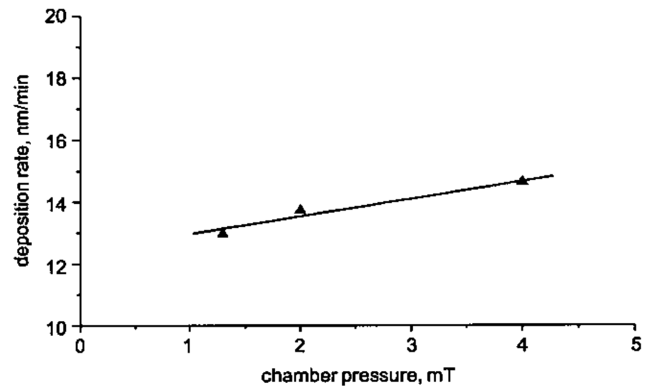


Fig. 8 *Chamber pressure dependence on deposition rate*

3.2.2 Effects of magnet current: Magnet current controls magnetic flux density to attain the ECR condition which enables the plasma to absorb the microwave energy. The intensity of the magnetic field in the specimen chamber decreases gradually from the plasma chamber to the specimen table [9]. In Fig. 9 we show the effects of current in the upper magnet coil (Fig. 4) on the trench-filling ratio as a function of aspect ratio. Shufflebotham and Thomson have emphasised that microwaves launched into a plasma are reflected where the magnetic field increases into an ECR region, and prefer a 'magnetic beach' profile of a continuously decreasing field from the microwave window [10]. Also, Stevens *et al.* [11] have found that high plasma densities near the microwave window produce stronger absorption. We therefore consider here that variations in the upper coil field are more significant than those in the lower. The current in the upper coil was always maintained $\geq$100 A to ensure a considerable ECR volume for microwave absorption immediately below the entrance window. As the upper-magnet current increases from 100 A to 120 A, a higher trench-filling ratio was obtained. This is because the higher magnet current tends to keep a larger volume of plasma subject to the ECR condition in the plasma chamber and produces more ions in a near-vertical direction in the chamber. Hence a greater flux of ions is transferred to the substrate, which results in relatively high deposition rates inside the trenches. However, there was no

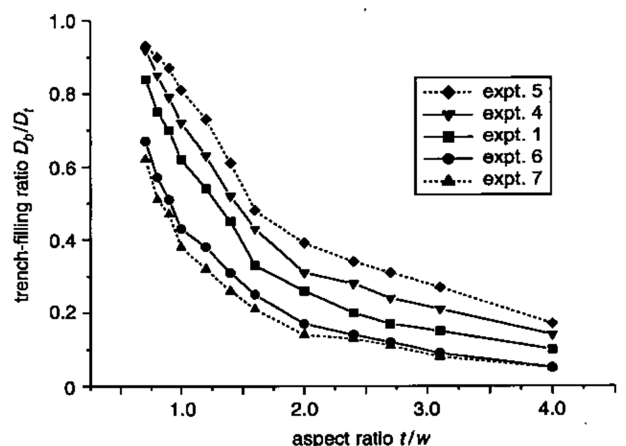
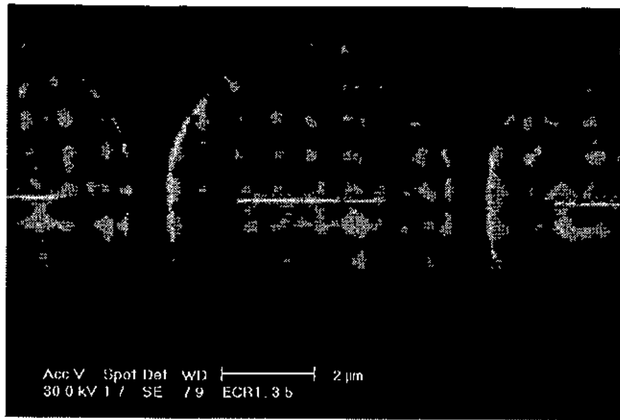


Fig. 9 *Trench-filling ratio as a function of aspect ratio, showing effects of magnet current and specimen-table height*
Expt. 5: magnet current 120 A, table height 100 mm
Expt. 4: magnet current 110 A, table height 100 mm
Expt. 1: magnet current 100 A, table height 100 mm
Expt. 6: magnet current 100 A, table height 65 mm
Expt. 7: magnet current 100 A, table height 30 mm



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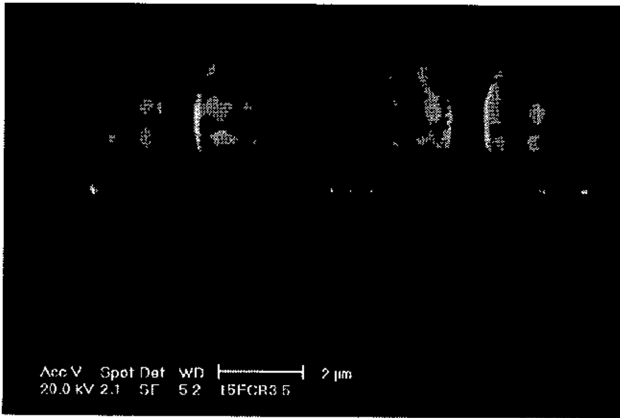


b

Fig. 10 *SEM cross-sections at different table heights*
Trench width: 3.5 µm
a Table height 100 mm
b Table height 30 mm

significant change in deposition rate on the horizontal wafer surface with the change of the magnet current.

3.2.3 Effects of specimen-table height: The trench-filling ratio decreases as the specimen-table height decreases from 100 mm to 30 mm as shown in Fig. 10. We postulate that the effect of decreasing the table height increases the arrival angle of the ions on the substrate, which results in a higher deposition rate on the sidewall of trenches situated closer to the plasma source than those located at a longer distance. This evidently promotes lateral growth near the tops of the trenches (see Fig. 10*b*) on a flat substrate and

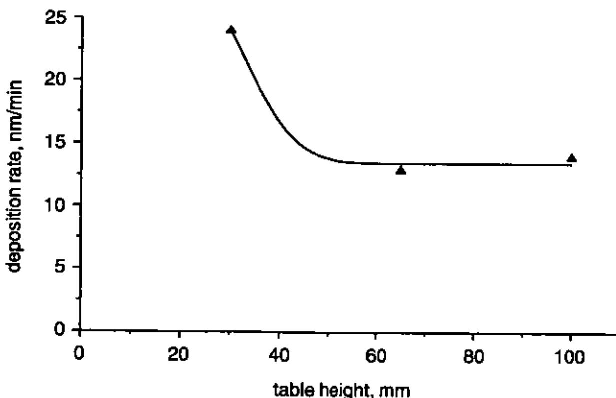


Fig. 11 *Table height dependence on deposition rate*
Table height zero represents extraction window position

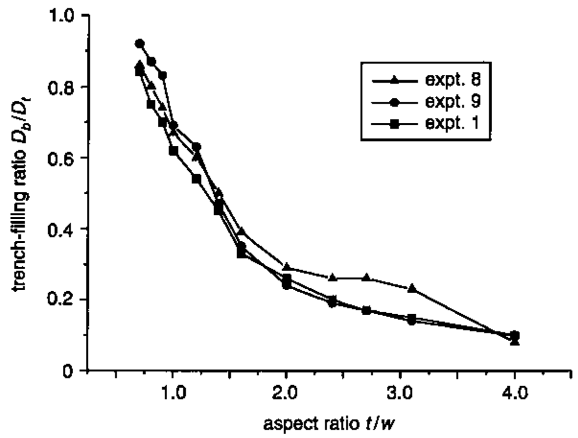


Fig. 12 *Trench-filling ratio as a function of aspect ratio, showing effect of DC bias voltage and Ar gas rate*
Expt. 8: DC bias voltage −300 V, Ar gas rate 0 sccm
Expt. 9: DC bias voltage −200 V, Ar gas rate 50 sccm
Expt. 1: DC bias voltage −200 V, Ar gas rate 0 sccm

decreases the trench-filling ratio gradually. We found that the deposition rate, when the table height was 30 mm, increased 1.6 times in comparison with the two other table positions as shown in Fig. 11. Fukuda *et al.* [12] have found that the decomposition efficiency of SiH_4 increases and the deposition rate increases when the table is located near the SiH_4 inlet position, due to the excitation by the electron cyclotron resonance in addition to the usual excitation by the oxidising agent. As shown in Fig. 10*a*, the trench shape with 100 mm of table height is partly tapered and partly vertical so that with continuing deposition it would fill up completely. The trench with 30 mm of table height has a re-entrant shape which would eventually fill the gap, but with included voids. It is evident that the severe overhang caused by the lateral growth of the dielectric results in low trench-filling capability.

3.2.4 Effects of DC bias voltage and Ar gas flow rate: Figure 12 shows the trench-filling ratios of the experiments with different DC bias voltages and Ar gas flow rate. The attempt to attain a bias of −400 V was not successful because of an RF matching problem. This reduced the bias to a lower value, even at the maximum power obtainable from the RF supply. We found that the trench-filling ratio increases as both the DC bias voltage and Ar gas flow rate increase. The DC bias voltage is applied to

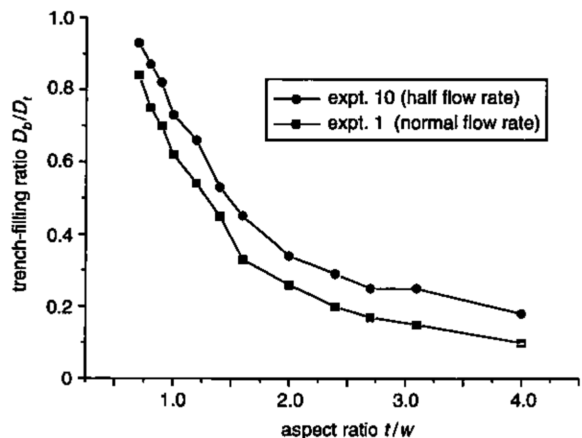
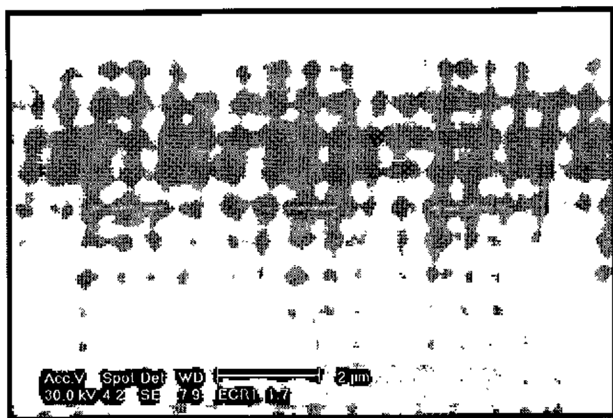


Fig. 13 *Trench-filling ratio as a function of aspect ratio, showing effect of reactant gas flow rate*



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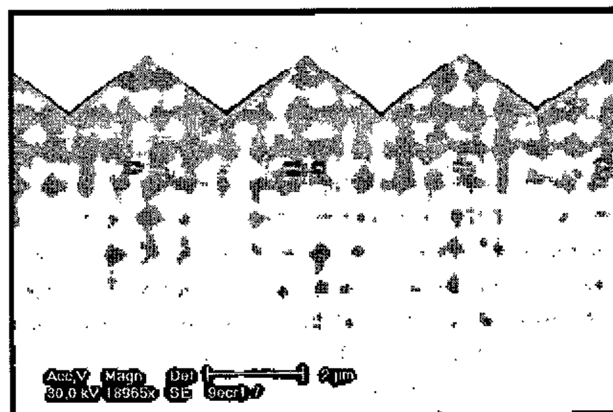

b

Fig. 14 *Comparison of SEM images of trench-fill patterns between original recipe and improved recipe with ECR CVD*

Trench width: 1.7 µm, aspect ratio: 2.4
a Trench fill with original recipe
b Trench fill with improved recipe

the substrate to control the incident velocity of the ions (hence the energy of the plasma ions) to the wafer so that the surface of the wafer can be simultaneously sputter-etched as deposition proceeds [13]. Addition of Ar into the SiH_4/N_2O deposition chemistry transfers a higher energy to the sample surface due to the heavier ion bombardment compared with the reactant species alone [14]. These parameters help to increase the sputter rate. Owing to the dependencies on the angle of incidence of the ions, the sputter rate becomes a maximum near 45° [15]. The net result is that sputtering is greatest at the top corners of the trenches and maintains the gap open. In addition, a part of the sputtered material would be expected to be re-deposited into the trenches.

3.2.5 *Effects of reactant gas flow rate:*

The trench-filling ratios of the experiments with different reactant gas flow rate are shown in Fig. 13. Experiment 1 was the experiment was the initial recipe that includes normal reactant gas flow rate (N_2O: 35 sccm, SiH_4/He: 100 sccm), and experiment 10 was the experiment with half flow rate (N_2O: 17.5 sccm, SiH_4/He: 50 sccm). The trench-filling ratio increases as the reactant gas flow rate decreases. This corresponds to the finding of Machida and Oikawa [13]. However, we find that the flat deposition rate linearly decreases with the decrease of the reactant gas flow rate, in agreement with Lassig and Tucker [6]. The deposition rate varies from 7.7 nm/min to 14.6 nm/min as the silane flow

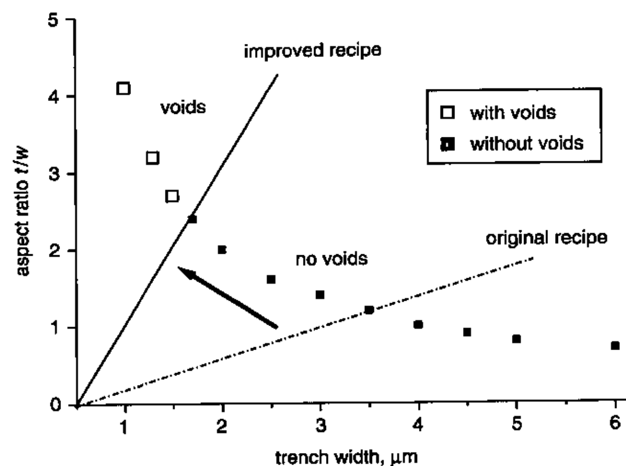

Fig. 15 *Analysis of voids/no voids area as a function of trench width and aspect ratio*

rate varies from 50 sccm (half flow rate) to 100 sccm (normal flow rate).

3.3 *Application to planarisation of ferroelectric liquid crystal on silicon backplanes*

Choosing the parameter values that produce the better trench filling, we improved the gap filling properties as shown in Fig. 14. The first stage (experiment 11-1 in Table 3) was carried out with argon sputtering condition (Ar 25 sccm, N_2O 17.5 sccm, SiH_4/He 50 sccm, chamber pressure 3.6 mTorr, DC bias voltage −300 V, magnetic current 120 A) to keep the gap open. After 3 h of process time, the deposited oxide was only 0.3 µm thick on the top of the trenches (D_t), due to the sputtering, and 1.35 µm on the bottom of the trenches (D_b). The second stage (experiment 11-2 in Table 3) was carried out in the higher rate deposition mode (N_2O 35 sccm, SiH_4/He 100 sccm, chamber pressure 2.1 mTorr) to reduce the deposition-process time. The oxide deposition rate was 16 nm/min and trenches were completely filled up to 1.7 µm-gap width (aspect ratio 2.4). We demonstrated the improvement of the trench-filling capabilities with a voids/no voids analysis [16, 17] as shown Fig. 15, in which the straight lines represent the critical conditions between trench-fills with voids and trench-fills without voids, and the steeper slope of the line means better trench-filling capability. The voids tend to increase as trench width is decreased and aspect ratio is increased. Figure 15 shows the improvement depending on trench width and aspect ratio, which demonstrates that the improved recipe (experiment 11) gives better results than the original recipe (experiment 1). Using the improved recipe, we achieved a planarised surface profile on a microdisplay backplane in a single process cycle without the need to repeat the oxide deposition/CMP process.

4 Conclusions

We have compared the trench-filling capability of ECR CVD and pyrolytic CVD techniques and demonstrated that the trench-filling capability of ECR CVD is better than that of the pyrolytic CVD. We have investigated the effects of ECR CVD parameters on the trench-filling properties and proposed an improved recipe for better trench filling. The following results were obtained by varying the ECR CVD parameters:

(i) The trench-filling ratio (R) increases as the chamber pressure decreases (4 mTorr–1.3 mTorr) because fewer ion collisions in the chamber result in highly anisotropic ion directionality and increase the deposition rate (D_b) in the trenches.
(ii) The ratio R also increases as the magnet current increases (100–120 A) because it maintains a large volume of plasma and produces more ions in a near-vertical direction in the chamber, which results in higher deposition rate inside trenches.
(iii) For the specimen-table height, the ratio R decreases as the table height decreases (100–30 mm). This effect seems to be an increase in arrival angle of the ions on the substrate, which results in the higher deposition rate on the sidewall of trenches.
(iv) The ratio R increases as both the DC bias voltage (−200 V to −300 V) and Ar flow rate (0–50 sccm) increase. The DC bias voltage and Ar flow rate assist to increase the sputter rate, which helps to maintain the trench open.
(v) Even though the ratio R increases considerably as the reactant gas flow rate decreases (N_2O: 35–17.5 sccm, SiH_4/He: 100–50 sccm), the deposition rate decreases to an impractical level.

The authors are aware that the microwave power may be an important parameter in the trench filling capability. In the present study the microwave power was held constant at 280 W. However, there is evidence when silane, oxygen, nitrogen and argon are used that there is a dependence of horizontal deposition rate on microwave power but that the side etch rate is not affected [13]. Hence there may be a limit to the microwave power that can be applied which will allow a trench of a given aspect ratio to be filled. It is intended that this effect will be investigated in the present ECR system where SiH_4/He and N_2O are the feedstock gases.

5 Acknowledgments

The authors wish to thank A.M. Gundlach and J.T.M. Stevenson for their support in making the test devices.

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Microelectronics Journal 35 (2004) 193–201

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Modelling of binary phase modulation in surface stabilized ferroelectric liquid crystal spatial light modulators

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Received 18 July 2003; accepted 2 September 2003

Abstract

Modelling of binary phase modulation is required for optimal performance of ferroelectric liquid crystals (FLC) on silicon SLMs when used in coherent optical systems. This paper presents a modelling technique by which an HSpice model can be provided for characterization of phase modulation properties for designing FLC-on-silicon SLMs. The simulation and experimental measurements of phase modulation are described. For the theoretical model simulation, FLC parameter measurements are described. We experimentally verify the modelled prediction of phase modulation by investigating reflective FLC test cells. We have shown reasonable agreement within 9% between the measured and simulated values of phase modulation.
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Keywords: Phase modulation; Ferroelectric liquid crystal; HSpice model

1. Introduction

Phase modulation is used for many non-display applications of liquid crystal displays such as optical correlators [1], optical interconnects [2], neural networks and adaptive optics [3]. Various SLMs have been developed for these applications, of which ferroelectric liquid crystals (FLC) on silicon SLMs [4,5] are used for binary phase modulation (typically 0 and π). To achieve better optical performance, a study is needed to model phase modulation that helps to characterization of FLC-on-silicon SLMs.

FLC material has birefringent properties and it acts like a waveplate to incident light as it interacts the polarisation of the light passing through it. If FLC material is constrained in a thin layer that is less than the FLC helical pitch as the chiral rotation is unwound by the thin layers, FLC directors' optical axis can move from one bistable state to another state by application of an electric field. This makes the FLC cell a uniaxial phase plate which can switch the optical axis. This is called surface stabilized ferroelectric liquid crystal (SSFLC) device [6]. SSFLC devices are well suited to binary phase modulation because of this binary switching property with fast switching speed. The interaction between the FLC molecules and coherent polarized light can be modelled by using an electronic circuit model. Using the model of an FLC cell we can predict how phase modulation varies with the FLC parameters. We introduce Moore and Travis' electronic circuit model [7] for this study because the model defines the rotation of FLC director as the charging voltage on a capacitor. Other equivalent circuit models for deformed helix FLCs [8] and antiferroelectric LCs [9] have been proposed, but the models are too simple to apply to FLC in this study.

In this paper we characterize an electronic equivalent circuit which describes the binary phase modulating properties of a SSFLC cell. The model will be used to optimize an FLC-on silicon device by simulating its behavior, and implementing it in HSpice. The model requires experimental measurements for rotational viscosity, chevron tilt angle and restoring torque of the FLC material, since the values of the parameters are changed depending on cell construction. The procedures for determining the circuit parameters, which describe the behavior of SSFLCs, are discussed. To evaluate

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0026-2692/$ - see front matter © 2003 Elsevier Ltd. All rights reserved.
doi:10.1016/j.mejo.2003.09.006

the performance of the HSpice model, we measure experimental values of phase modulation from reflective FLC cells using an interferometer.

This paper first addresses the issues associated with characterizing LC cells which is essential for the development of any model. It then addresses existing models and their limitation and proposes the addition of a voltage-controlled current source. This model is then evaluated using the results from the cells that have been characterized.

2. Cell characterization

2.1. Cell preparation

Reflective SSFLC cells are constructed as a thin layer of smectic C* FLC material sandwiched between an ITO-coated substrate and a reflective-mirror substrate, as shown in Fig. 1. The fabrication of the cell is such that the molecule directors align in the same direction by the influence of surface alignment layers. Aluminum film was coated on a glass substrate to produce a reflective mirror. Polyimide solution, LQ1800 from Dupont Chemical, was coated and rubbed using a velvet cloth to form surface alignment layers on both substrates. An ITO coated substrate and an aluminum-evaporated substrate were assembled together having a cell gap 2.4 μm. The assembled cells were filled at isotropic phase (>97 °C) by capillary action and then slowly cooled (1 °C min^{-1}) to room temperature. FLC materials, FELIX015/100 (Clariant GmbH) and CS1031 (Chisso Co.), were used for the experiments. The mixtures have a spontaneous polarisation of 33 and −28.1 nC cm^{-2}, respectively. Two test cells were constructed using each FLC material, to confirm reproducibility of the experiment.

The basic theory of binary phase modulation is presented in Appendix A. For a binary phase modulation, the reflective FLC cell is designed to act as a half-wave plate. This requires the reflective cell thickness t to be given by $t = \lambda/(4\Delta n)$, where Δn is the FLC birefringence and λ is wavelength of light. The cell should be of uniform thickness to avoid splay distortions and allow good alignment. Unlike a transmissive cell, a reflective cell further complicates cell investigation due to the double pass of incident light in and out of the cell, which is more sensitive to the poor optical alignment. However, the reflective cell proved a useful tool in assessing phase modulation performance of reflective SLM devices.

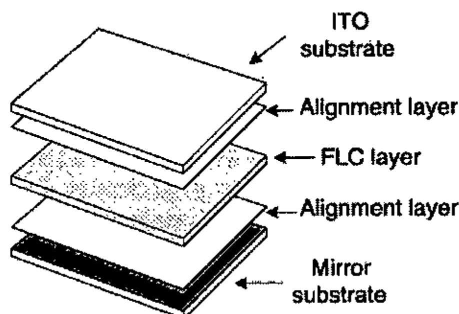


Fig. 1. Construction of a reflective FLC cell.

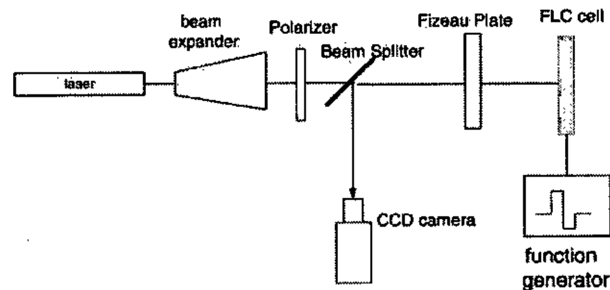


Fig. 2. Setup for measuring the phase modulation on a reflective FLC cell.

2.2. Phase shift measurement

A measurement technique based on Fizeau interferometer system was used for phase modulation on a reflective FLC cell as shown in Fig. 2. A laser beam (He–Ne) is expanded, spatially filtered, and linearly polarized to produce a vertically polarized collimated source. The beam is projected via a beamsplitter towards the Fizeau plate, which is optically flat. A portion of the beam is reflected from the Fizeau plate back to the beamsplitter as a reference beam. The rest of the beam travels towards the FLC cell that reflects a portion of the beam energy back into the system where it interferes with the reference beam and produces interference fringes on CCD camera.

With driving rectangular pulses on the reflective test cell, two different interference patterns are recorded by a CCD camera. After transferring the patterns to an image handling software, the fringe data were used to measure the shifted distance between two patterns. Then the phase shift is calculated from the measured data that is exported to a spreadsheet.

Fig. 3 shows two different fringe patterns and the phase shift in degrees can be measured by: $\Delta\phi$

$$\Delta\phi = 2\pi \frac{x}{d} \quad (1)$$

where d is the period of fringe pattern and x is shifted distance of the pattern between two bistable states of an

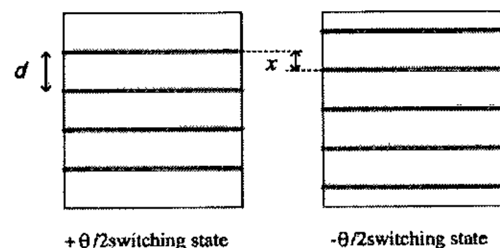


Fig. 3. Principle of phase shift measurement from two different fringe patterns.

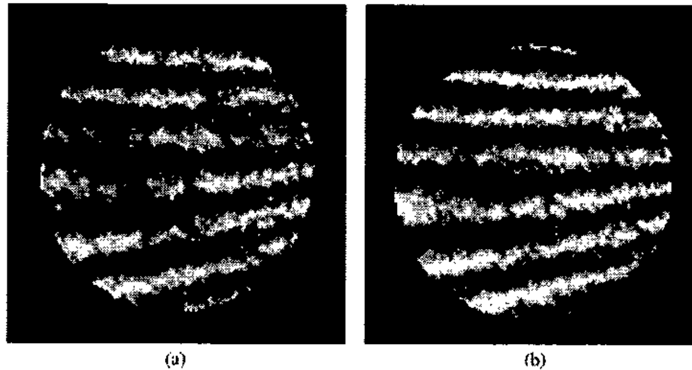


Fig. 4. Fringe patterns (FLC: FELIX015-100). (a) $+\theta/2$ Switching state, (b) $-\theta/2$ switching state.

FLC cell. The period d can be varied by adjusting the position of the Fizeau plate and the FLC cell on a tilt mount which enables horizontal or vertical tilt fringes to be aligned for the measurement.

Fig. 4 shows actual measurement of fringe patterns in which (a) was switched to the $+\theta/2$ state and (b) was switched to the $-\theta/2$ state.

With this setup, values of phase modulation are measured with two different FLC materials, which is FELIX015-100 and CS1031. The phase modulation measurements of test samples are given in Table 1 with the accuracy of $\pm 8\%$. We can achieve $0/\pi$ phase modulation by adding an analyzer but the transmission efficiency decreases as discussed in Section 3.3. If the FLC cells were an ideal half wave retarder, phase modulation should be four times the corresponding cone angle (refer Table 2), i.e. phase modulation in ideal conditions will be 0.57π in FELIX015-100 cells and 0.42π in CS1031 cells.

3. Model development

3.1. Equivalent circuit model

FLC material sandwiched between two glass substrates is dielectric and can be regarded as a resistor and a capacitor connected in parallel. The equivalent circuit for phase modulation is shown in Fig. 5 in which the equivalent circuit for an FLC cell is derived from Moore and Travis' PSpice equivalent circuit [7]. This model treats the rotation of FLC directors with time and applied voltage as bulk mechanical effects, such that the director rotation angle ϕ is proportional to the charge on the capacitor C_{ps}. Using the charge on the capacitor C_{ps} of the Moore and Travis' model we derived phase modulation by inserting an additional voltage-controlled current source E_{ph}. E_{OUT} represents light transmission and E_{ph} represents phase modulation. To run a simulation tool, Agilent's ICCAP, in a UNIX environment, the conversion of the equivalent circuit is needed from PSpice to HSpice model.

To define the current source E_{ph} in the HSpice equivalent circuit, the geometry of director position in SSFLC devices is investigated. SSFLC devices usually exhibit a chevron structure, which causes the smectic layers buckle through the depth of the device and layer tilt angle to the surface normal. Fig. 6 shows the tilted bistable director position at the plane of alignment surface in the chevron structure. The cone angle θ defines a hypothetical cone of angle 2θ in which the molecular director switches within the cone in the surface plane, and varies with the FLC material. The chevron tilt angle δ is the angle that the FLC smectic layers make with the aligning surface normal. ϕ is the angle of the director rotating around the cone and ϕ_s is the case when the director is on the bistable position. From the geometry in Fig. 6 the switching angle Ψ is derived between projection

Table 1
Measurement of phase modulation

	Sample #1-a	Sample #1-b	Sample #2-a	Sample #2-b
LC material	FELIX015-100	FELIX015-100	CS1031	CS1031
Measured phase modulation (rad.)	$0.46 \pm 0.03\ \pi$	$0.53 \pm 0.04\ \pi$	$0.41 \pm 0.02\ \pi$	$0.37 \pm 0.03\ \pi$

Table 2
Model parameters of test cells

	Sample #1-a	Sample #1-b	Sample #2-a	Sample #2-b
LC material	FELIX 015/100	FELIX 015/100	CS1031	CS1031
Cell gap[a] (μm)	2.4	2.4	2.4	2.4
Spontaneous polarisation[a] (nC/cm^2)	33	33	−28.1	−28.1
Cone angle[a] (deg)	25.5	25.5	19	19
Cell capacitance (nF/cm^2)	5.9	5.7	8.9	8.3
Effective cell area (cm^2)	1.2 ± 0.1	1.2 ± 0.1	1.2 ± 0.1	1.2 ± 0.1
Cell resistance (MΩ)	>20	>20	>20	>20

[a] Values from material supplier's data.

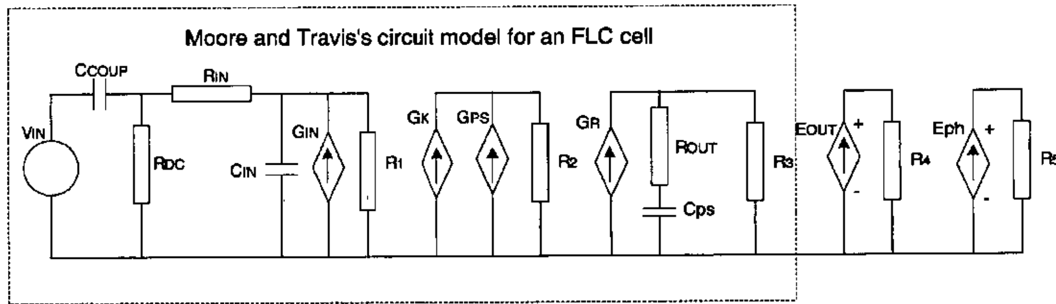


Fig. 5. HSpice equivalent circuit for phase modulation.

of the director onto the plane of the cell and rubbing direction, and it is greater than the bistable director angle Ψ_s on the plane of cell

$$\tan \Psi = \frac{\sin \theta \sin \phi}{\cos \theta \cos \delta + \sin \theta \cos \phi \sin \delta} \quad (2)$$

where θ is the FLC cone angle, ϕ is the director rotation around the cone and δ is the chevron tilt angle.

If we make an FLC cell as a half wave plate, the cell will have the effect of rotating the phase of incident light by an angle of 2Ψ, which is phase modulation and denoted as E_{ph} in the HSpice model

$$E_{ph} = 2\Psi = 2\,\mathrm{atan}\frac{\sin \theta \sin \phi}{\cos \theta \cos \delta + \sin \theta \cos \phi \sin \delta} \quad (3)$$

For the HSpice model the angles θ, ϕ and δ in Eq. (3) have to be converted into voltage per radian as shown in Eq. (4), for the simulation to work successfully. Eq. (4) is inserted into the HSpice model as an additional voltage-controlled current source E_{ph} to give the voltage equivalent to the phase modulation of the cell

$$E_{ph} = 2\,\mathrm{atan}\frac{\sin(V_{cone})\sin(V_{cps})}{\cos(V_{cone})\cos(V_{tilt}) + \sin(V_{cone})\cos(V_{cps})\sin(V_{tilt})} \quad (4)$$

where V_{cone} represents the converted voltage of the cone angle in radian ($\theta \times \pi/180$), $V_{C_{ps}}$ is the voltage of the capacitor (C_{ps}) in the HSpice model representing the director rotation around the cone in radian ($\phi \times \pi/180$) and V_{tilt} represents the converted voltage in radian of the chevron tilt angle ($\delta \times \pi/180$).

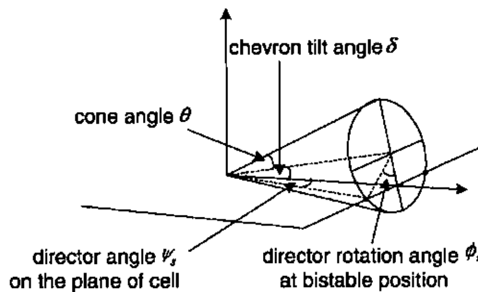


Fig. 6. Geometry of the director position in chevron structure.

3.2. Model parameters measurements

For the simulation of the HSpice model, some ferroelectric cell parameters needed are the cell gap, the cell active area, the cell capacitance, the spontaneous polarisation, the restoring torque, the director cone angle, the chevron tilt angle, and the viscosity. Table 2 shows the model parameters associated with its four test cells, constructed for this study.

Some of the model parameters, such as restoring torque and rotational viscosity, vary with the cell gap and the alignment layer treatment [10,11], and in this case we need direct measurements from the test cells rather than using data sheet values. These parameter measurements are carried out using the setup shown in Fig. 7. A PC with the customized software is connected through a GPIB interface between the Wavetek AWG75 signal generator and the Fluke PM3382A digital oscilloscope. Both input voltage and light output are captured by the oscilloscope.

3.2.1. Chevron tilt angle

The value of chevron tilt angle is needed for the measurement of the director rotation angle ϕ_s and can be derived from the projected director angle Ψ_s. From the chevron structure geometry in Fig. 6, the projected director angle Ψ_s is specified as Eq. (5), whose values depend on

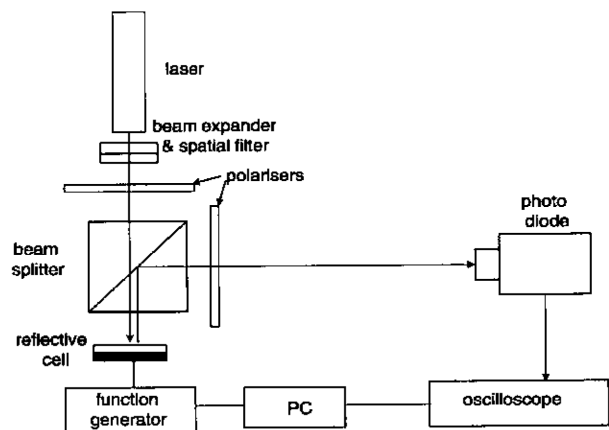


Fig. 7. Measurement setup for the FLC model parameters.

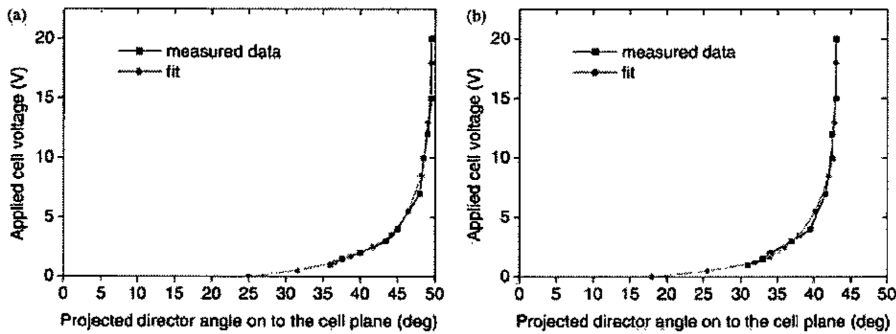


Fig. 8. The projected director angle (2Ψ) on to the cell plane against applied square-wave voltage. (a) Sample #1-a (FELIX015/100), (b) sample #2-a (CS1031).

the cone angle θ and chevron tilt angle δ.

$$\cos \Psi_s = \frac{\cos \theta}{\cos \delta} \tag{5}$$

The projection of the director angle 2Ψ on to the cell plane is measured by applying a symmetrical square wave voltage across a test cell in the measurement setup (Fig. 7). Light transmission corresponding to the applied square wave voltage is altered by rotation of the cell position under crossed polarizers. As the cell is rotated, first a set of square wave maxima and minima are seen on the oscilloscope. With continued rotation, the pattern disappears and later appears with the maxima and minima of the first pattern interchanged. The angle 2Ψ is obtained as the difference in angular position between one set of maxima in light transmission and the opposite set of maxima. Fig. 8(a) shows the projection of the director onto the cell plane 2Ψ against peak drive voltage for cell (Sample #1-a), where we can find the projected director angle Ψ_s is $12.5 \pm 0.5°$, given by $2\Psi_s = 25 \pm 1°$. The measurements in other test cells have shown that the graphs produced in Fig. 8(a) and (b) can be similarly reproduced. Using Eq. (5), we can find the chevron tilt angle δ is 22.4°, calculated from the measured projected director angle Ψ_s and the cone angle θ. The results of the chevron tilt angle δ measurements are shown in Table 3.

3.2.2. Restoring torque

If a director exceeds either bistable positions, the restoring torque $K(\phi)$ tends to put the director back to the nearest stable positions. The restoring torque has nonlinear properties and can be simulated with a look-up table as shown in Fig. 9 [7]. The bistable positions of directors vary with the FLC cells, so the position angles should be measured from the actual test cells.

Table 3
Chevron tilt angle δ measurements from four samples

	Sample #1-a	Sample #1-b	Sample #2-a	Sample #2-b
Projected director angle, Ψ_s (deg)	12.5 ± 0.5	12 ± 0.5	9 ± 0.5	10 ± 0.5
Cone angle, θ (deg)	25.5	25.5	19	19
Chevron tilt angle, δ (deg)	22.4	22.7	16.8	16.2
$\cos \delta = \cos \theta / \cos \Psi_s$				

From the chevron structure geometry in Fig. 6, the stable position of the director rotated about the circular face of the cone is:

$$\cos \phi_s = \frac{\tan \delta}{\tan \theta} \tag{6}$$

We already know chevron tilt angle (δ) from the measurement (Section 3.2.1) and cone angle from Table 2. We can calculate the director rotation angle ϕ_s using Eq. (6) and the results are shown in Table 4.

3.2.3. Rotational viscosity

The last parameter we need for the model is rotational viscosity. As the direct measurement of the rotational viscosity is difficult, we have obtained the value of rotational viscosity of a cell by running the simulation with best fit with an arbitrary rotational viscosity. The actual light transmission pulse can be measured from the setup (Fig. 7). Simulated light transmission is plotted by setting the $E_{\mathrm{OUT}} = \sin^2 2\Psi$ in the HSpice model. We compare the simulated light transmission pulse shape and position of the model with the measured light transmission pulse and choose the best fit between simulated and measured transmission pulses from simulation sets. For example, Fig. 10 shows the simulated light transmission response and measured light transmission for the sample #1-a cell with

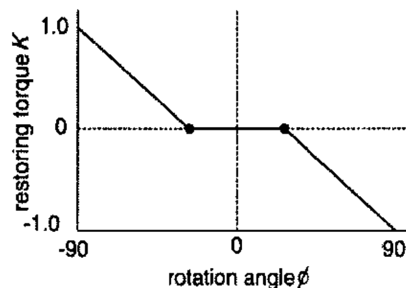


Fig. 9. Restoring torque with bistable positions of the director (bistable positions are shown as dark spots).

Table 4
Stable position angle ϕ_s measurements from four samples

	Sample #1-a	Sample #1-b	Sample #2-a	Sample #2-b
Chevron tilt angle, δ (deg)	22.4	22.7	16.8	16.2
Cone angle, θ (deg)	25.5	25.5	19	19
Director rotation angle, ϕ_s (deg) $\cos\phi_s = \tan\delta/\tan\theta$	30.6	28.7	28.7	32.5

various values of the rotational viscosity, driven by ±5 V square wave. The closest fit is indicated a rotational viscosity of approximately 215 ± 10 mPa s. The results of the rotational viscosity measurements are shown in Table 5.

3.3. Simulation results and discussion

Using the measured parameters we simulated the test sample performance. Fig. 11 shows the simulation results with the drive voltage and phase modulation curve for ±5 V drive. We can derive the values of phase modulation from the simulation curves.

Fig. 11 shows that the switching time of phase modulation output in both samples 1a and 1b much slower than the switching time in samples 2a and 2b. This is because the switching time is attributed to the higher rotational viscosity (refer Table 5) which depends on the FLC materials. The FLC switching time is proportional to rotational viscosity and inversely proportional to spontaneous polarisation and applied electric field.

To test the model performance, phase modulation comparisons are made between the experimental (refer Table 1) and simulated curves as shown in Table 6. The values of the measured phase modulation agree with values of the simulated within 9%.

As mentioned in Section 2.2, phase modulation in ideal conditions will be 0.57π in FELIX015-100 and 0.42π in CS1031 cells. One of the factors contributing to these deviations from ideal cells comes from the fact that for the ideal cell, the cell-gap is selected to produce a half wave plate (retardation $\Gamma = \pi$). If the retardation of the FLC device is π and the cone angle of the FLC is 45°, it is possible to achieve 0/π phase modulation with 100% transmission. However, if the retardation is not π or cone angle of the FLC is not 45°, as is the case with our device, polarizers have to be introduced to achieve 0/π phase modulation and the power transmission decreases as shown in Fig. 12. The deviation from optimum cell-gap affects the efficiency of phase modulation. As Γ deviates from π rad, phase shift between the two output states is moved away

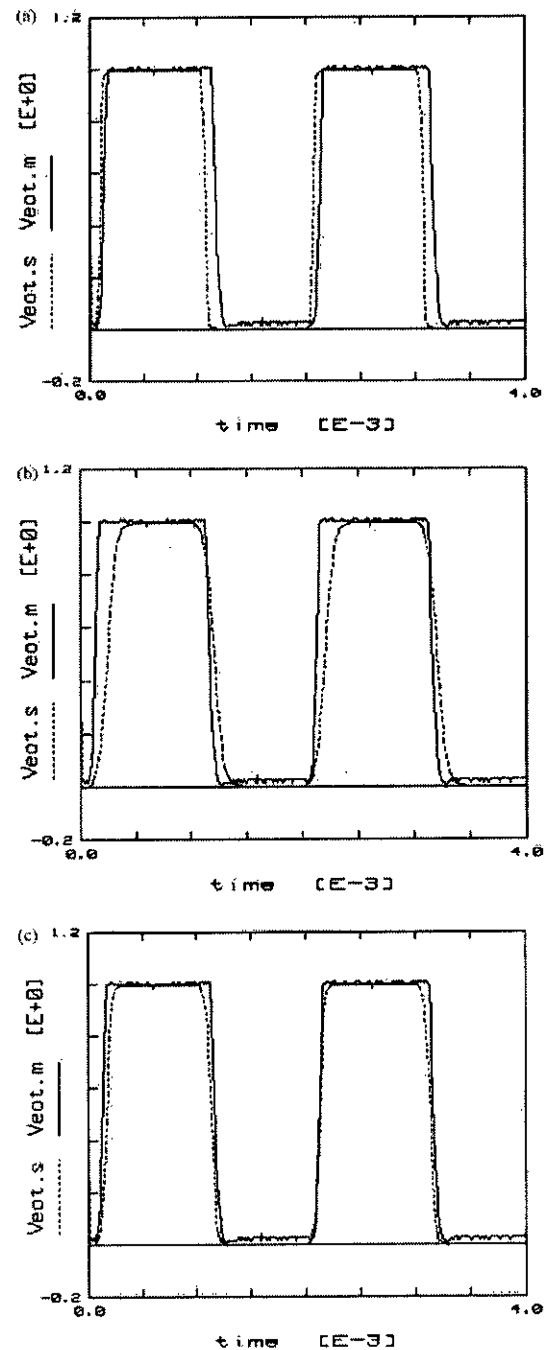


Fig. 10. Simulation with rotational viscosity, for the ±5 V square-wave input (Veot.s, simulated waveform; Veot.m, measured waveform). (a) The rotation viscosity of 100 mPa s, (b) the rotational viscosity of 300 mPa s, (c) closest fit with the rotational viscosity of 215 mPa s.

from an expected value and power is transferred into undesired mode resulting in reduced efficiency [12].

To verify the effect of cell-gap variations from a half wave plate, the phase shift produced by a FLC SLM is

Table 5
Rotational viscosity measurements from simulation

	Sample #1-a	Sample #1-b	Sample #2-a	Sample #2-b
Rotational viscosity (mPa s)	215 ± 10	170 ± 10	11 ± 2	42 ± 5

presented by use of Jones matrix. The FLC is considered as a retarder with a Jones matrix **W** at an arbitrary angle:

$$\mathbf{W}=\begin{pmatrix} e^{-j\Gamma/2}\cos^2\frac{\theta}{2}+e^{j\Gamma/2}\sin^2\frac{\theta}{2} & -J\sin\frac{\Gamma}{2}\sin(\theta) \\ -J\sin\frac{\Gamma}{2}\sin(\theta) & e^{j\Gamma/2}\cos^2\frac{\theta}{2}+e^{-j\Gamma/2}\sin^2\frac{\theta}{2} \end{pmatrix} \tag{7}$$

where its optical axis at an angle $\theta/2$ to the vertical and a retardance of Γ.

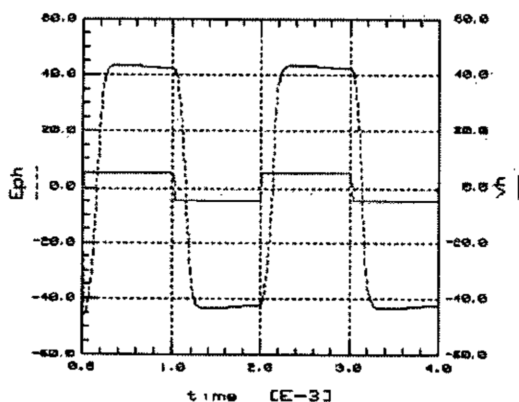
The incident light **V** is vertically polarized and is described by

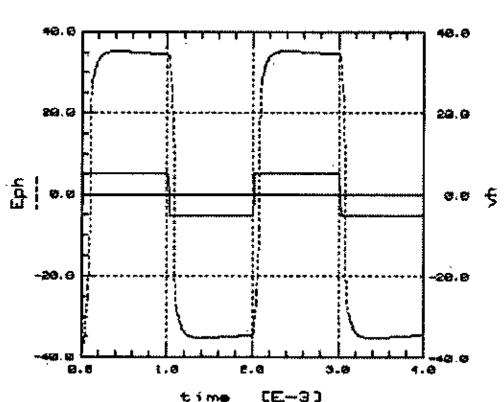
$$\mathbf{V}=\begin{pmatrix} 0 \\ 1 \end{pmatrix}, \tag{8}$$

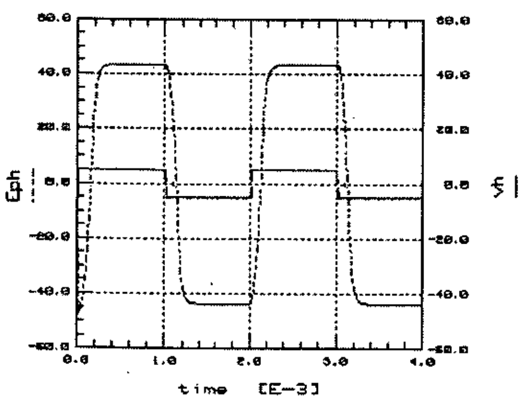
and the transmitted output light **T** without an analyzer is then given by

$$\begin{aligned}\mathbf{T}&=\mathbf{W}\cdot\mathbf{V}\\ &=\begin{pmatrix} e^{-j\Gamma/2}\cos^2\frac{\theta}{2}+e^{j\Gamma/2}\sin^2\frac{\theta}{2} & -J\sin\frac{\Gamma}{2}\sin(\theta) \\ -J\sin\frac{\Gamma}{2}\sin(\theta) & e^{j\Gamma/2}\cos^2\frac{\theta}{2}+e^{-j\Gamma/2}\sin^2\frac{\theta}{2} \end{pmatrix}\cdot\begin{pmatrix} 0 \\ 1 \end{pmatrix}\\ &=\begin{pmatrix} -J\sin\frac{\Gamma}{2}\sin(\theta) \\ e^{j\Gamma/2}\cos^2\frac{\theta}{2}+e^{-j\Gamma/2}\sin^2\frac{\theta}{2} \end{pmatrix}\end{aligned} \tag{9}$$

Phase shift as cell gap variations have been calculated with the above matrix equation using Matlab. Fig. 13 shows that the thickness variation from a half wave plate introduces







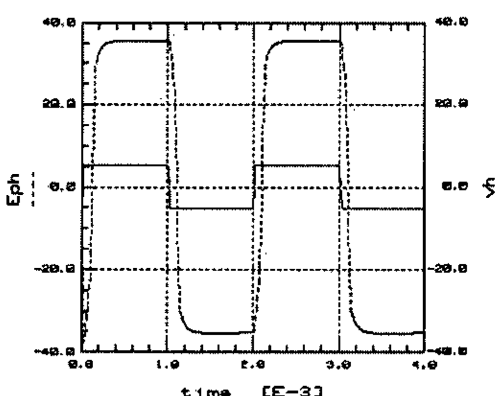


Fig. 11. Modelled phase modulation curve for test cells (Vh, applied input voltage; Eph, phase modulation output). (a) Sample #1-a, (b) sample #1-b, (c) sample #2-a, (d) sample #2-b.

Table 6
Comparison of phase modulation between measured and simulated data

	Sample #1-a	Sample #1-b	Sample #2-a	Sample #2-b
LC material	FELIX015-100	FELIX015-100	CS1031	CS1031
Measured phase modulation (rad.)	0.46 ± 0.03 π	0.53 ± 0.04 π	0.41 ± 0.02 π	0.37 ± 0.03π
Simulated phase modulation (rad.)	0.47 ± 0.01 π	0.48 ± 0.01 π	0.38 ± 0.01 π	0.38 ± 0.01 π

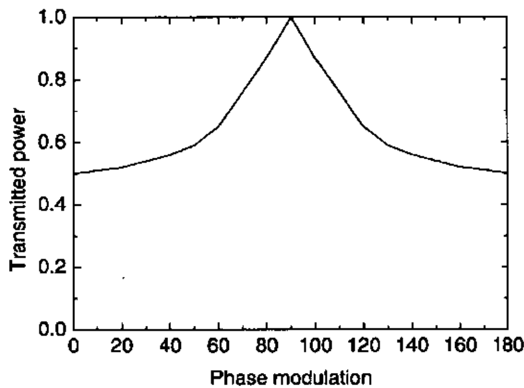


Fig. 12. Normalized transmitted power associated with a given phase modulation for a 22.5° (cone angle) FLC material.

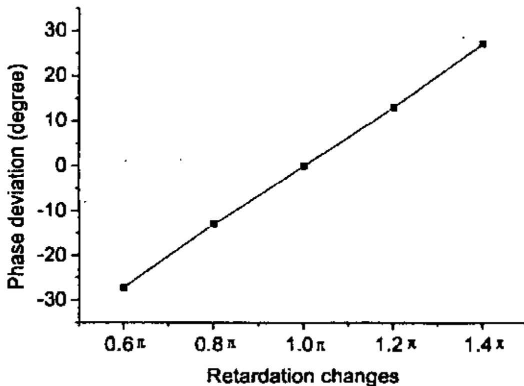


Fig. 13. Relative phase shift between the two outputs of FLC caused by deviations in the thickness of the cell gap from a half wave plate.

a relative phase shift between the two output states. It is thought that this phase deviation caused by the cell thickness variation results in the mismatch between the ideal and simulated (or measured) phase modulation.

4. Conclusions

We have presented a model for binary phase modulation by using an electronic equivalent circuit to describe the electro-optical properties of an SSFLC cell. To our knowledge this is the first time this has been reported and this model can be used in the characterization of phase modulation properties for designing FLC-on-silicon SLMs. We have described measurement techniques: phase modulation on a reflective SLM and modelling parameters such as rotational viscosity, chevron tilt angle and restoring torque. We have shown reasonable agreement within 9% between the measured and simulated values of phase modulation of reflective FLC cells. The close agreement of the phase modulation results, for both sets of samples, has shown that the quality of the cells is highly reproducible.

Acknowledgements

The authors would like to acknowledge EPSRC (GR/M 39305) for financial support.

Appendix A. Theory of binary phase modulation

To describe phase modulation, Jones matrix is suitable for analyzing the polarization of an optical signal as it passes through a FLC layer with polarizers. Phase modulation can be calculated by multiplying an input Jones vectors for the polarizers and a FLC layer using spreadsheets:

$$\begin{pmatrix} V'_x \\ V'_y \end{pmatrix} = P(\alpha_A)\cdot\mathbf{W}(\theta)\cdot P(\alpha_P)\cdot\begin{pmatrix} V_x \\ V_y \end{pmatrix},$$

where V_x and V_y are the horizontal and vertical polarization components of the input, $\mathbf{W}(\theta)$ is the Jones matrix for the FLC at the tilted angle θ to the optic axis, α_A and α_P are the angles of the analyzer and polarizer, $P(\alpha)$ is the Jones matrix for a linear polarizer rotated by angle α, and V'_x and V'_y are the horizontal and vertical polarization components of the output. Parameters of FLCs and polarizers are needed to develop the Jones matrix. As a result, the output profiles will include intensity and phase status of the light.

A phase modulator can be constructed by using a FLC half-wave retarder with two stable orientations for the optical axes, and its operation principle is shown in Fig. 14. If we take vertically polarized light as an input, then the FLC pixel fast axis positions must bisect the vertical axis

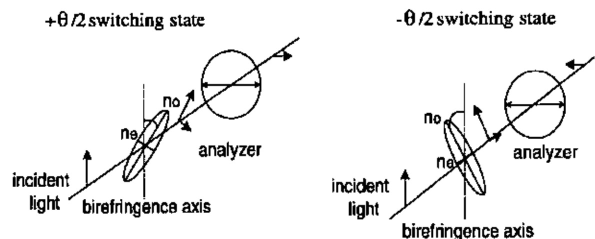


Fig. 14. The two states of FLC for phase modulation.

and will be oriented at angles of $\theta/2$ and $-\theta/2$, respectively. The Jones matrix for the one switching state ($\theta/2$) will be

$$\begin{pmatrix} V_x^t \\ V_y^t \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix} \cdot \begin{pmatrix} e^{-j\Gamma/2}\cos^2\frac{\theta}{2} + e^{j\Gamma/2}\sin^2\frac{\theta}{2} & -J\sin\frac{\Gamma}{2}\sin(\theta) \\ -J\sin\frac{\Gamma}{2}\sin(\theta) & e^{j\Gamma/2}\cos^2\frac{\theta}{2} + e^{-j\Gamma/2}\sin^2\frac{\theta}{2} \end{pmatrix} \cdot \begin{pmatrix} 0 \\ V_y \end{pmatrix} = \begin{pmatrix} -V_y J\sin\frac{\Gamma}{2}\sin(\theta) \\ 0 \end{pmatrix}$$

The other switching state ($-\theta/2$) will be

$$\begin{pmatrix} V_x^t \\ V_y^t \end{pmatrix} = \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix} \cdot \begin{pmatrix} e^{-j\Gamma/2}\cos^2\frac{\theta}{2} + e^{j\Gamma/2}\sin^2\frac{\theta}{2} & J\sin\frac{\Gamma}{2}\sin(\theta) \\ J\sin\frac{\Gamma}{2}\sin(\theta) & e^{j\Gamma/2}\cos^2\frac{\theta}{2} + e^{-j\Gamma/2}\sin^2\frac{\theta}{2} \end{pmatrix} \cdot \begin{pmatrix} 0 \\ V_y \end{pmatrix} = \begin{pmatrix} -V_y J\sin\frac{\Gamma}{2}\sin(\theta) \\ 0 \end{pmatrix}$$

From the above equations, it is notified that the only difference between two switching states is the minus sign, which means π phase modulation.

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Multi-phase modulation for nematic liquid crystal on silicon backplane spatial light modulators using pulse-width modulation driving scheme

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Received 2 December 2003; received in revised form 1 March 2004; accepted 15 March 2004

Abstract

In phase modulating diffractive optical devices multi-phase modulation provides improved performance over binary modulation. Multi-phase modulation can be achieved by using nematic liquid crystal spatial light modulators (NLCSLM) with pulse-width modulation driven from a binary CMOS backplane. This paper presents the characteristics and the driving scheme of the 512 × 512 Si-backplane SLM for the implementation of the multi-phase modulation while comparing the binary and four-level phase holograms. Diffraction efficiency of 39.7% for binary grating and 72.9% for four-level blazed grating were obtained at the spatial frequency 1.56 lines/mm.
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PACS: 42.79.K; 42.79.H; 42.25.F

Keywords: Multi-phase modulation; Liquid crystal SLM; LCoS devices

1. Introduction

Liquid crystal spatial light modulators are devices capable of processing information onto an optical wavefront. CMOS-silicon active-matrix backplanes provide small geometry, high mobility, reflective mode operation and system on chip capability. The combination of modulating a liquid crystal layer with a CMOS-silicon backplane has resulted in a key component in coherent optical applications for optical interconnection [1,2], optical correlation systems [3,4],

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doi:10.1016/j.optcom.2004.03.043

adaptive optics [5] and holographic animation [6].

Binary CMOS-backplane devices typically contain an array of 1-bit digital memory cells and provide binary modulation of light. Analogue CMOS-backplane devices need analogue switches and storage transistors that accumulate the charge representing each pixel value on its gate. Due to the complexity of the design resolution of analogue CMOS backplanes are limited and their cost is high compared to binary a CMOS backplane.

The use of binary phase levels restricts the diffraction efficiency of computer-generated holograms (CGHs) because the binary phase profile directs more light energy into the higher orders. Multi-phase modulation increases diffraction efficiency, eliminates the intrinsic inversion symmetry in the Fourier plane, and more accurately controls the output. Thus, multi-phase modulation is highly desirable and must be characterized for those optical applications. Various multiple phase modulators have been reported. Cascaded ferroelectric liquid crystal (FLC) SLMs [7,8] have been proposed to produce multi-phase levels based on cascading binary phase modulators. However, the cascaded SLMs are too complex to arrange the optical features, and too bulky to apply in an optical system. Nematic liquid crystals (NLC) SLMs [9,10] are also capable of multi-phase modulation by controlling their voltage level, but using this approach it is difficult to manage precise phase modulation. Moreover, the Si-backplane circuitry must be analogue, making it more complicated than digital circuitry.

In this paper, we introduce multi-phase modulation with NLCSLMs driven from a binary CMOS backplane. To drive binary CMOS backplanes for multi-phase levels, a pulse-width modulation driving scheme has been developed and a parallel-aligned nematic liquid crystal spatial light modulator constructed for its phase modulator.

The diffraction efficiency properties for binary phase grating and four-level blazed grating have been measured along with a comparison of far-field diffraction patterns being performed between binary and four-level phase hologram displayed by the 512 × 512 Si-backplane SLM.

2. Binary Si-backplane spatial light modulator

The Si-backplane [11] used in this study consists of a 512 × 512 array of DRAM-type pixels. The backplane architecture shown in Fig. 1 has 64 data buslines (D00–D63) and 15 control buslines (PH1, PH2, LAL, IID, etc.) operating the device. The detailed specifications of the backplane are shown in Table 1.

The backplane addressing circuitry uses two 8-to-256 column decoders to enable 512 pixel column lines and multiple serial shift register architecture (64 × 8 bit shift registers) to load data.

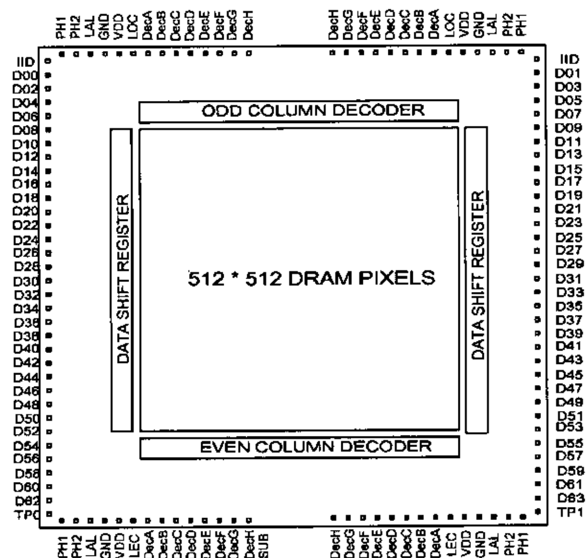

Fig. 1. 512 × 512 backplane architecture.

Table 1
The 512 × 512 backplane specifications

Number of pixels	512 × 512
Active pixel array area	10.24 × 10.24 mm^2
Die area	14 × 14 mm^2
Technology	1.2 μm n-well CMOS
Pixel circuit	pMOS pass transistor and MOS capacitor
Pixel pitch	20 μm
Electrode mirror area	18.4 × 18.4 μm^2 (planarized)
Operating frequency	48 MHz
Data bus	64 bit
Frame scan time	84 μs
Drive voltage	5–6 V
Power dissipation	<100 mW

The column decoders are placed along the top and bottom of the display area, and the top decoder selects the odd columns and the bottom decoder selects the even columns. The column decoders manage the enable buslines vertically located in the backplane. The data shift registers are placed on the left and right side of the backplane and they manage the horizontal data buslines in the backplane. Data are loaded from the framestore on the interface board 64 bits at a time to the backplane device.

As the unplanarized backplanes have low pixel fill factors and optically rough surfaces, highly planarized pixels are required to improve optical performance in phase modulation. Each pixel is enlarged using CMP (chemical mechanical polishing) planariz ation technology [12,13]. Due to the structure of the pixelation and repetition of the deadspace, backplanes generate higher light intensity in the higher order of the far field diffraction pattern. Fig. 2 shows the planarized pixels (mirrors) on the 512 backplane, which have a 20-μm pitch and an 85% fill factor.

The schematic of an assembled 512-backplane SLM is shown in Fig. 3. A 9-μm thick layer of nematic liquid crystal is sandwiched between the front ITO substrate and the reflective backplane. The LC molecules are aligned parallel to two substrates to obtain phase-only modulation without changing the polarization direction of the LC molecules [14–16]. The LC alignment layers are achieved by obliquely evaporated SiO.

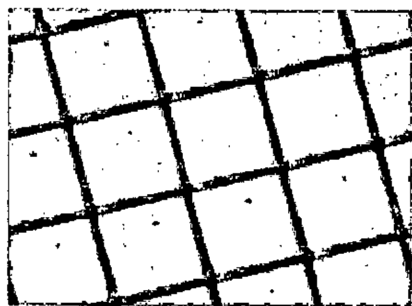

Fig. 2. Planarized pixels on the 512 backplane.

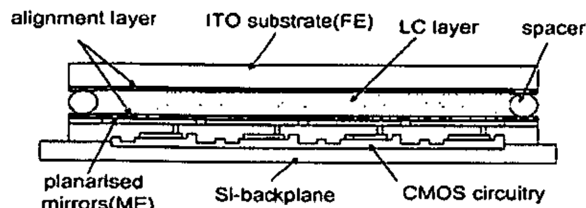

Fig. 3. The schematic cross-section of an assembled 512-backplane SLM.

3. Pulse-width modulation driving scheme

3.1. Pulse-width modulation with a NLC cell

Multi-phase modulation can be achieved by using NLCs with pulse-width modulation driven from a binary CMOS backplane. Pulse-width modulation is required to control the multi-phase of the NLCs. The voltage waveform in Fig. 4 shows the pulse-width modulation scheme. We can control the NLC phase information by changing duty ratios of the applied voltage waveform.

The characteristics of the NLC with pulse-width modulation were investigated using the experimental setup shown in Fig. 5. A parallel-aligned NLC cell is used for measuring phase-shift properties. The cell was fabricated with 9-μm gap and

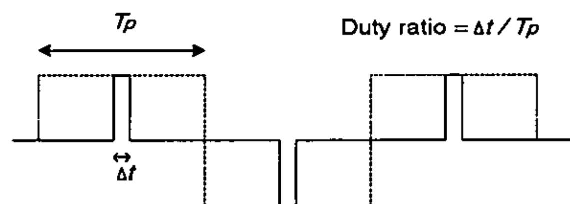

Fig. 4. Pulse-width modulation scheme.

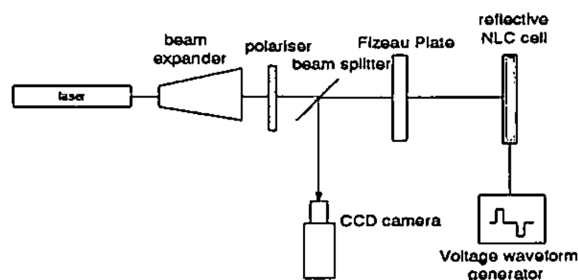

Fig. 5. Measurement setup for phase-shift properties.

NLC (E7) was then injected into the empty cell at room temperature. Fig. 6 shows the phase-shift properties of the NLC with different duty ratios and different applied voltages. This shows that the phase shift of NLC increases as the duty ratio of the applied pulse increases. Thus, multi-phase modulation can be achieved by applying pulse-width modulation to a NLCSLM.

The phase shift of NLC begins earlier as the applied voltage increases, as shown in Fig. 6. The frequency of applied voltages was 1 kHz. The phase shift properties are not changed as the frequency of applied voltages changes from 100 Hz to 5 kHz. The response time of the SLM depends on the type of LC material and applied voltage level.

These results show useful phase shift relation against duty cycle and in particular an almost linear relation when using 3 V peak-to-peak drive with a phase shift range of 6π.

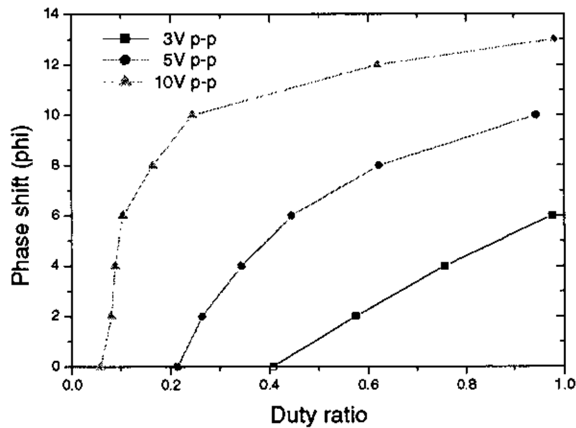

Fig. 6. Phase-shift properties of NLC (E7) as a function of duty ratio, showing the effect of applied voltage (1 kHz duty cycle).

3.2. Driving scheme for Si-backplane SLM

To drive the 512×512 array of backplane, a custom digital interface [17] was used (see Fig. 7). This was designed to connect to a PC via a 78-way connector and PCI272 DIO card. The interface board includes a field programmable gate array (FPGA) device that consists of an internal array of logic blocks with a ring of programmable input/output blocks. The FPGA configures the driving scheme and loads image data to a framestore. The interface board also includes a framestore which consists of two $64\text{Kb} \times 32$ synchronous static random access memory. The framestore has a space for 16 bit-planes where a bit-plane is a 512×512 binary data. An 8 bit-plane data was used for this study to apply multi-level phase modulation.

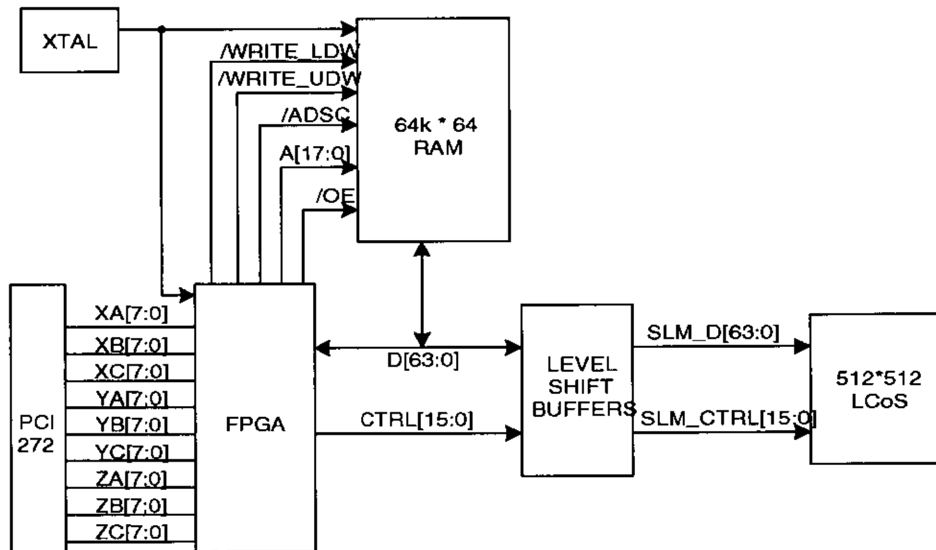

Fig. 7. Block diagram for 512 LCoS interface board.

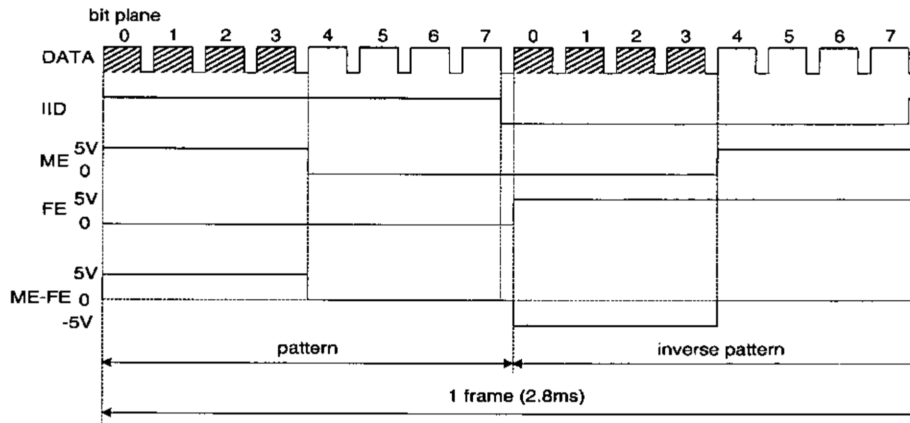

Fig. 8. Timing diagram for pulse width modulation (50% duty ratio).

The waveform-timing scheme in Fig. 8 shows the DC balanced PWM for multi-level phase modulation. The calculations for this timing diagram were based on the 50 MHz (20 ns) clock frequency which is set by the clock speed on the interface board.

In the timing diagram the signal DATA shows eight bit-planes in which each bit plane has 512×512 array of data, and consists of both addressing (0.18 ms) and blanking periods (2 μs). In the normal LC microdisplay, the blanking period can be used as an illumination time and the duration is varied in accordance with the number of bit planes. The ratio of the illumination periods of which are $1{:}2{:}2^2{:}2^3{:}\cdots{:}2^{(\text{number of bit-planes}-1)}$ and the combination of these produces $2^{(\text{number of bit-planes})}$ of grayscale. In this study, however, we need constant periods for each bit-plane time to produce equally divided pulse widths for multi-level phase modulation.

In Fig. 8 the signal IID, which is placed in front of data input of each DRAM pixels, can invert or non-invert the input data, i.e., when IID is High, the input data is inverted, and when IID is Low, the data is non-inverted. This achieves DC balanced addressing with positive and negative addressing cycles which is necessary for liquid crystal displays. If DC balanced addressing is not applied the liquid crystal can be damaged and results in image sticking on the display. The signal ME represents the applied voltage to the mirror electrode and the signal FE controls the front electrode voltage. The signal ME-FE in Fig. 8 represents the voltage applied across the liquid crystal layer which is located in between the front and mirror electrode.

The phase-modulation characteristic of the 512 NLCSLM was measured using a setup with He-Ne laser light at 632.8 nm (see Fig. 5). Fig. 9 shows output fringe patterns obtained with a range of duty-ratios, generated by different gray area patterns, i.e., the upper half area had the zero duty ratio and the bottom half area had an arbitrary duty ratio. Thus the relative phase shift caused by the different duty ratios can be obtained by observing the fringe shift of the bottom half area with respect to the fringe in the upper half area. The phase shift $\Delta\phi$ in degrees between top and bottom area can be measured by:

$$\Delta\phi = 2\pi \times \frac{x}{d}, \tag{1}$$

where d is the period of fringe pattern and x is shifted distance of the pattern between two different patterns. It can be observed that the fringe clearly shifts between the different duty ratios and by more than a 2π-rad shift at 0.375 duty-ratio with a 5-V drive voltage.

The results of detailed phase-shift measurements are shown in Fig. 10, which gives the phase-modulation properties for duty ratio differences ranging between 0 and 1. It is possible to achieve

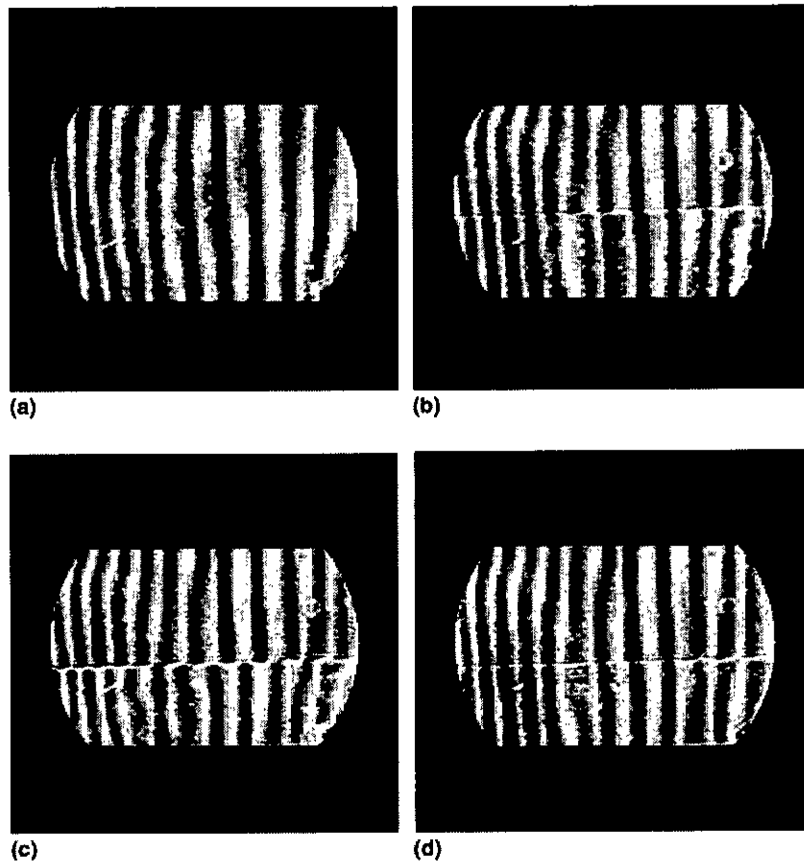

Fig. 9. Fringe patterns from the phase-measurement setup (a) zero phase shift (duty-ratio difference 0). (b) 0.25π phase shift (duty-ratio difference 0.125). (c) 1.07π phase shift (duty-ratio difference 0.25). (d) 2.1π phase shift (duty ratio difference 0.375).

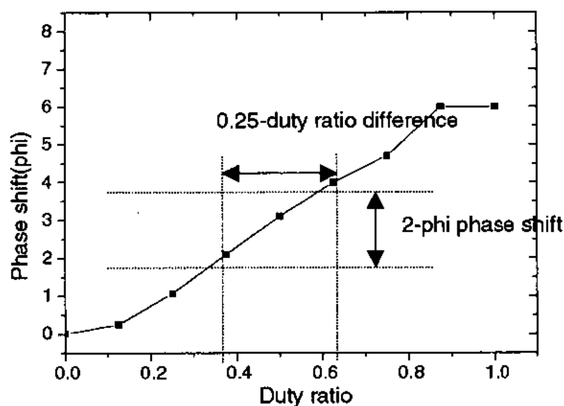

Fig. 10. Phase-shift properties of 512 NLCSLM as a function of duty ratio and adjustment of 2π phase shift.

around 6π phase modulation with this type of PWM driving.

3.3. Characterization of 2π phase modulation

In order to obtain 2π phase modulation the driving scheme should be adjusted, as only 0.25-duty ratio is required rather than full-duty ratio as shown in Fig. 10.

Fig. 11 shows the waveform timing for the revised driving scheme. The degree of phase shift can be controlled by adjusting the blanking time. To produce 2π phase shift, we need a long blanking time after bitplane7 addressing. To change the blanking time after bitplane7 addressing, the driving circuit was redesigned using a multiplexer. Each data addressing time (bitplane0–bitplane7) is

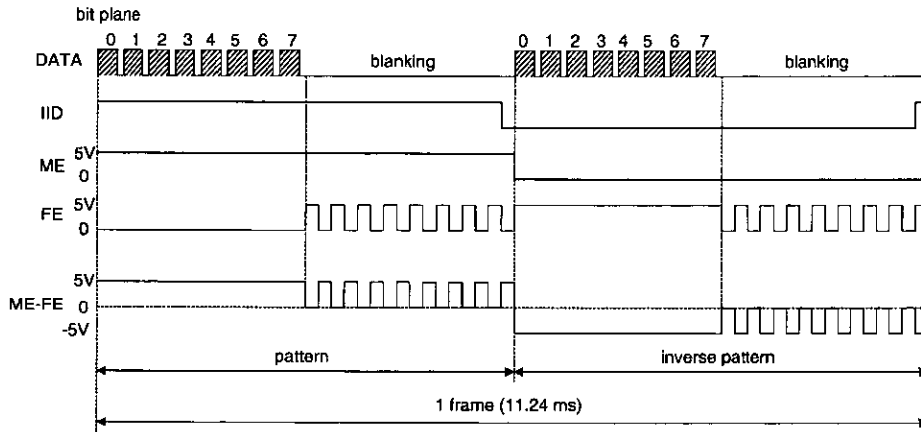

Fig. 11. Timing diagram of the driving scheme for 2π phase modulation.

set to 1.42 ms and the time for a frame is set to 11.24 ms. During the blanking period after bit-plane7 alternating voltage must be applied to the front electrode so that the NLC material responds to the RMS value of the alternative field. If the alternating frequency is not high enough, NLC material follows an alternative field and phase modulation cannot be achieved. With this new driving scheme, exact 2π phase modulation was achieved with four different phase levels. To get more than four phase levels, the most important factor is the number of data bit planes in data address time. If the driving scheme is designed with higher number of data bit planes, more phase levels can be achieved. The frame rate, the choice of NLC or different mode of cell construction would be less effective to achieve higher phase levels.

4. Performance

4.1. Diffraction efficiency

Diffraction efficiency characteristics for binary and four-level phase grating of the SLM were measured using the setup in Fig. 12. A He-Ne laser (10 mW power) with wavelength of 632.8 nm was collimated by a lens ($f = 200$ mm), and the polarization direction of the collimated light was adjusted to the direction of LC molecules using a

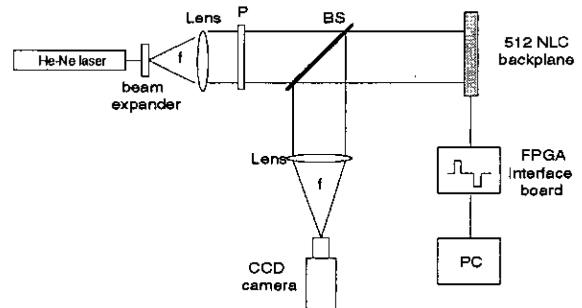

Fig. 12. Measurement setup for diffraction efficiency.

polarizer. The Fraunhofer diffraction pattern of the light was taken with a 1000 mm focal-length lens. An optical power meter with an aperture in front of the detector was used to measure the intensities of the diffracted orders. A 1.5 mm pinhole was used to isolate a single diffracted peak in the replay field for measurement on the optical power meter.

Efficiency measurements of the optical system were performed on the SLM. The light intensity from laser source to the SLM was 2.5 ± 0.2 $\mu W\,cm^{-2}$ and total light intensity at Fourier plane was 255 ± 10 $nW\,cm^{-2}$. The light intensity of the DC spot was 135 ± 5 $nW\,cm^{-2}$. From the measured values, the overall system efficiency (light from laser source/light in DC spot) was 5.4% and the reflected diffraction efficiency (light from Fourier plane/light in DC spot) was 53%.

The 1st order diffraction efficiency is defined as,

$$\eta_1 = \frac{I_1}{I_0}, \quad (2)$$

where η_1 is the diffraction efficiency into the 1st order, I_0 is the intensity of the zeroth order without modulation, and I_1 is the intensity of the first order. The drive voltage to the SLM was 5.5 V.

The diffraction efficiency increases as the phase level is increased because more power can be diffracted into a single order. The efficiency is given by [18]

$$\eta(M) = \left[\frac{M}{\pi}\sin\left(\frac{\pi}{M}\right)\right]^2, \quad (3)$$

where M is the number of phase levels. From Eq. (3) we can simulate the value of diffraction efficiency as $\eta(2) = 0.405$ and $\eta(4) = 0.811$.

As a test of binary phase performance a one-dimensional periodic phase grating was displayed on the SLM by altering the phase 0 and π. For the four-level phase performance a one-dimensional blazed phase grating was displayed of four periods (zero, π/2, π, and 3π/2 in sequence). The resolution of the 512 × 512 SLM is 50 pixels per mm.

Table 2 shows the experimental results of the 1st order diffraction efficiency and simulated values for binary grating and four-level blazed grating. The diffraction efficiency was 39.7% for the binary grating and was 72.9% for the four-level blazed grating (at the spatial frequency 1.56 lines/mm). As expected from the theoretical values, the diffraction efficiency increased as the number of phase levels rises from binary to four levels.

Diffraction efficiency generally decreases as the spatial frequency is increased (period length is decreased). This is mainly because SLM devices tend to decrease the response at high spatial frequencies [14,19]. Bouvier and Scharf [20] have also found that the phase profile changes from nearly binary to sinusoidal when the spatial frequency is increased. The limit of spatial resolution results in the decrease of diffraction efficiency. Fig. 13 shows the diffraction efficiency for the first order diffraction lights with various spatial frequencies. The spatial frequency was varied between 1.56 and 12.5 lines/mm in both for the binary and four-level blazed grating. The diffraction efficiency decreased from 39.7% to 34.8% for the binary grating and also decreased from 72.9% to 53.4% for the four-level blazed grating. Although the diffraction efficiency in both cases decreases as the spatial frequency increases, it was found that the diffraction efficiency of the four-level blazed grating decreases more than the diffraction efficiency of the binary grating. It is believed that the larger decrease associated with the four-level blazed grating comes from the limit of spatial resolution which is more sensitive to spatial frequency than the binary grating.

Table 2
Measurement of the 1st order diffraction efficiency

	Simulated values	Measured values
Binary grating	40.5%	39.7 ± 1%
Four-level blazed grating	81.1%	72.9 ± 2%

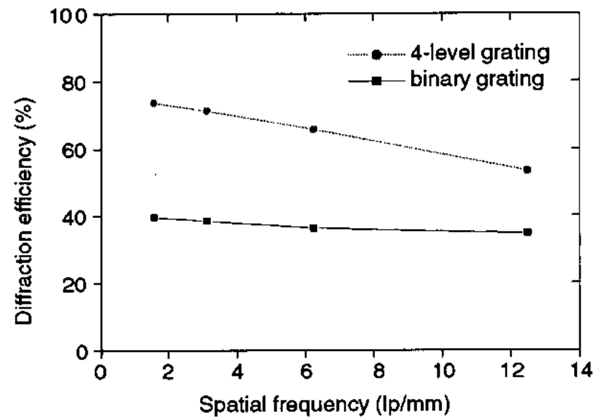

Fig. 13. Diffraction efficiency as a function of grating spatial frequency.

4.2. Computer generated holograms (CGHs)

The optical setup for the replay field of CGHs with the Si-backplane SLM is shown in Fig. 12. For capturing the replay field pattern the optical power meter was replaced by a CCD camera. Fig. 14(a) shows the binary hologram for 4 × 4 spot array displayed on the Si-backplane SLM and Fig. 14(b) shows the replay field of the binary hologram captured by a frame grabber. The four-level phase

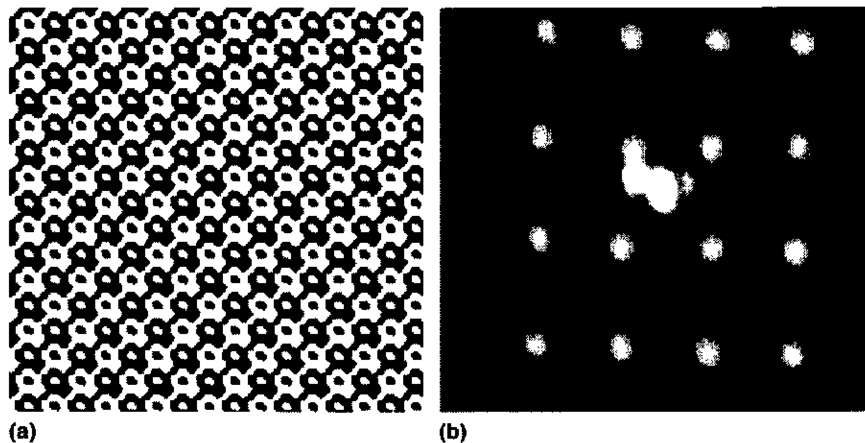

Fig. 14. (a) Binary hologram for 4 × 4 spot array. (b) Replay field generated by writing the binary hologram on the 512 × 512 SLM.

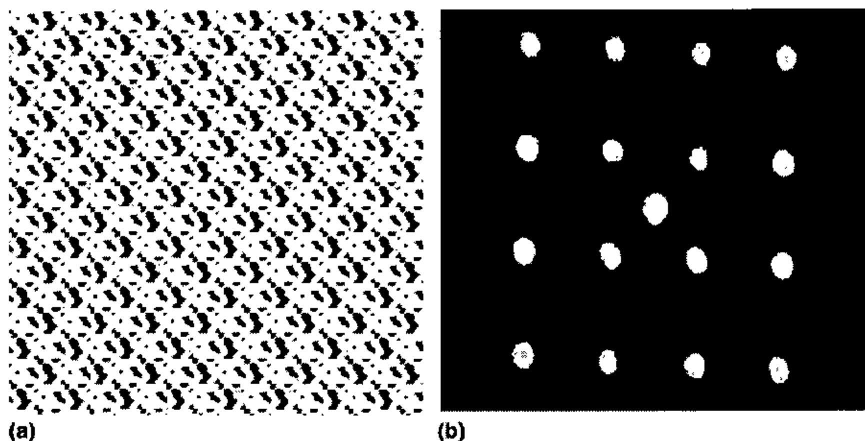

Fig. 15. (a) Four-level phase hologram for 4 × 4 array. (b) Replay field generated by writing the four-level phase hologram on the 512 × 512 SLM.

hologram for 4 × 4 spot array is shown in Fig. 15(a) and its replay field was also captured with a frame grabber as shown in Fig. 15(b). There was no temporal wobble or noise on the holograms. A DC spot is observed in both figures because any uneven shapes on the surface of pixels and dead spaces between the pixels cause higher order diffraction that results in noise in zero order. It can be observed that the replay field of four-level phase hologram shows a much clearer and brighter spot size pattern than the replay field of binary hologram. The result demonstrates that diffraction efficiency of four-level phase modulation is superior to that of binary phase modulation.

5. Conclusions

A Si-backplane NLCSLM has been developed that is capable of multi-phase modulation using pulse-width modulation driving. Successful four-level phase reconstructions have been demonstrated using the binary Si-backplane SLM. The diffraction efficiency increases as the number of phase levels rises from binary to four levels as predicted from the theory. A diffraction efficiency of 39.7% was obtained for binary gratings and 72.9% for four-level blazed grating at the spatial frequency 1.56 lines/mm. Diffraction efficiency characteristics for the spatial frequency have been

examined for both binary and four-level blazed grating. This found that the diffraction efficiency of the four-level blazed grating decreases more than the diffraction efficiency of the binary grating although the diffraction efficiency in both cases decreases as the spatial frequency increases. This is because the limit of spatial resolution in four-level blazed grating is more sensitive to spatial frequency than binary gratings. Hologram replay characteristics of the SLM were also examined by displaying the binary hologram and four-level phase hologram of 4×4 spot array. This demonstrated the replay field of four-level phase hologram shows a much clearer and brighter spot size pattern than the replay field of binary hologram. These results confirm that the diffraction efficiency of four-level phase modulation is superior to that of binary phase modulation.

Acknowledgements

The authors thank Dwayne Burns of Microemissive Displays Ltd for technical assistance with designing the driving circuit and Kevin Heggarty of the ENST Bretagne for his helpful comments.

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