A STUDY OF THE THIN FILM TRIODE

by

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CHAPTER 1.

INTRODUCTION.

Microelectronics now has an accepted place in electronics and is having an impact on the electronics industry rivaling the invention of the transistor. The desire to miniaturize produced a revolution in the design and manufacture of electronic components which involves the mass fabrication and integration of these components together with their interconnections, encapsulations and external contacts, the end product being an integrated circuit. Over the years, different approaches have been taken to the miniaturization of components and circuits and consequently different technologies have evolved, each providing in its own way an integrated form of circuit. Hence, in its widest sense, an integrated circuit may be defined as [1]:

> "the physical realization of a number of circuit elements, inseparably associated on or within a continuous body to perform the function of a circuit."

Integrated circuits generally break down into two major categories, one utilizing semiconductor techniques only, the other using film technology to supplement semiconductor contributions. These categories and their position in the microelectronic classification [1] are shown in Figure 1.1.

In the first category, all the components of a circuit form an integral part of a piece of bulk semiconductor material. Techniques such as diffusion, epitaxial growth and passivation are used to obtain the particular components

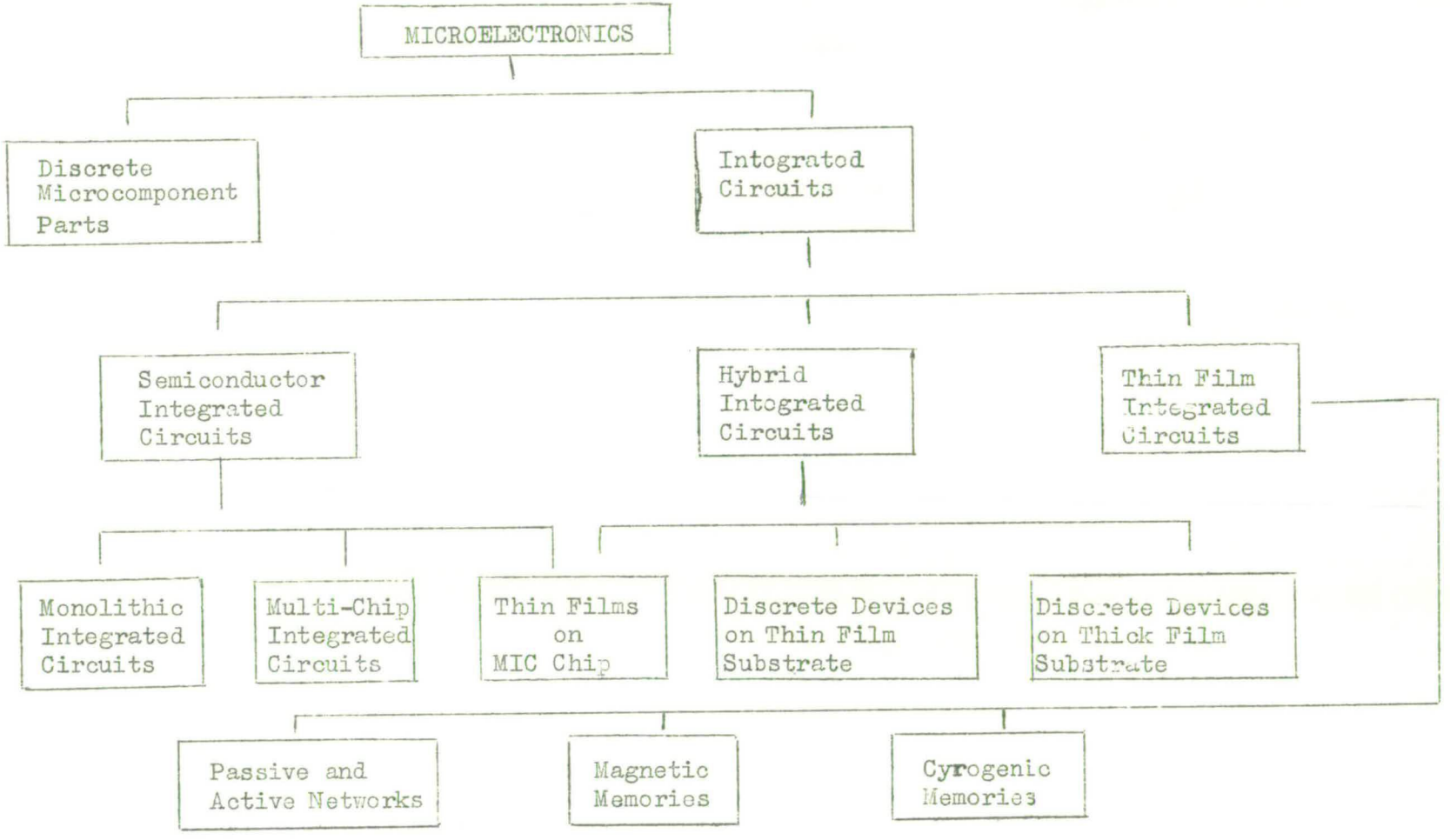


Figure 1.1 Basic Microelectronic Classification.

required within the circuit. Interconnections within the block of material are made by deposition of thin film material. This type of circuit is referred to as a monolithic circuit. They have been used extensively for digital requirements in such forms as RTL, DTL and TTL logic. More recently successful linear circuits have been produced using these techniques. In addition to the monolithic semiconductor integrated circuit, a multi-chip approach to integration has been used. In this case, resistors, capacitors, transistors and diodes are fabircated as individual components which are then connected together to form an integrated circuit. This procedure represented a stepping stone on the way to monolithic integrated circuits.

The second broad category consists of hybrid integration. This is a very general classification which often leads to some misunderstanding owing to the fact that there are hybrid circuits which are a combination of thin film, thick film, metal film and multi-chip circuits. A thin film circuit is usually designated as such if the resistor and dielectric material used in conjunction with the active devices are formed by techniques such as vacuum evaporation. The thickness of these films is measured in terms of Angströms, thus the reference to thin film. Thick films on the other hand incorporate resistor and dielectric materials which have been deposited by silk or metal screening techniques. The material is of the order of 1 micron or more in thickness. Metal film circuits usually refer to a material such as tantalum which is anodised to form resistor material.

Semiconductor integrated circuits find most applications where highly repetitive digital requirements exist, and where relatively few circuit types

are involved. Under these conditions the volume justifies the high design and tooling costs while the use of batch processing reduces the production costs. On the other hand, thin film hybrid integrated circuits are used for close tolerance analogue applications which require extreme resistor stability and where relatively small total numbers are involved. The economic production of small runs of custom built circuits arises from the low capital cost in the thin film process chosen. The thick film system lends itself to the use of mechanised processing equipment and hence is used for larger runs of any given circuit where the emphasis is on minimum cost.

The classic reasons for using either monolithic or hybrid microelectronics technology are:

(a) reliability

(b) cost

(c) size and weight

Perhaps the most talked about factor is reliability. Integrated circuits in general have fewer connections of dissimilar materials and therefore less connection failures. Historically, electrical connections have been a major problem from a reliability standpoint. Deposited connections are inherently more reliable than discrete soldered connections. There is also control over the formation of the complete circuit. With a circuit of discrete components different components come from different places and so have different reliabilities. However, some of this control is lost in the hybrid forms of integration. In addition, the use of redundancy, brought about by the opportunity to achieve more circuits per unit volume, has contributed to increased overall reliability.

When integrated circuits were first introduced at the beginning of this decade they were extremely expensive but had the important features of small size and high reliability. The immediate applications that were seen for integrated circuits at that time were mainly confined to military and space systems where small size and high reliability justified the high cost. During the 6 years or so since integrated circuits were first designed into equipment, the manufacturing cost and selling price has decreased faster than anyone could have foretold. Fabrication yields have greatly improved and fabrication cost has become an almost insignificant part of the manufacturing cost. The most significant cost involved in integrated circuits now occurs at the assembling and testing stages of manufacture. Thus individual handling of the devices for bonding, sealing and testing contribute greatly to the total manufacturing cost of the devices and it is this that has led to the concept of large scale integration (LSI).

Today, in many types of electronic equipment - military, space and aviation systems, communications, control and laboratory instruments and the consumer electronics industry - integrated circuits have become the basis of design. Although the initial impetus for the development of integrated circuits was the necessity for reducing size and weight, it is now apparent that integrated circuits allow equipment to be made at a lower cost than can be achieved with discrete components and the other advantages which accrue, size and reliability, may be regarded as bonuses.

The basic classification shown in Figure 1.1 points to the possibility of thin film integrated circuits. At present the most satisfactory form of active

device for incorporation in any form of thin film circuit, thick or thin, is the inverted chip transistor. It is possible to fit such chip transistors by soldering to conducting areas of both thin and thick circuit systems. However, the unity of the thin film process is broken by this technique and there is a requirement for an evaporated thin film active device to permit the formation of thin film integrated circuits. Weimer [2] and his co-workers at the R.C.A. laboratories have produced such a device and experimentation on completely integrated circuits is now being actively carried out.

The all-thin-film approach to integrated circuits utilizes an inert insulating substrate in place of the single crystal used in semiconductor integrated circuits (MOS and bipolar). Complete electrical isolation of the individual components is readily attained and therefore parasitic coupling effects are avoided. As large area substrates do not present any great problem to vacuum evaporation techniques, thin film integrated circuits are likely to find a specialized application in solid-state image-scanning devices.

This thesis is devoted to a study of the thin film transistor.

CHAPTER 2.

FUNDAMENTALS OF THE THIN FILM FIELD EFFECT TRANSISTOR.

2.1 HISTORY OF FIELD EFFECT.

The basic idea of using a transverse electric field to control the longitudinal electric current between two electrodes, or simply the field effect principle, was disclosed by J.E. Lilienfeld [3] of New York in a series of patents, the first of which was issued in 1930. Lilienfeld proposed the structure shown in Figure 2.1. In this case, a thin layer of semiconductor, copper sulphide, was separated from a control electrode, aluminium, by a layer of insulation, aluminium oxide. When an electric field is applied across the insulator, the layer of semiconductor charges up, and this increase in charge results in an increase in the number of carriers available for conduction. Thus, it is capable of modulating the conductivity of the current path in the semiconductor.

Other early experiments along these lines were undertaken by O. Heil [4] in Germany and were recorded in a British patent in 1935. He suggested the use of tellurium, iodine, cuprous oxide or vanadium pentoxide as a semiconductor, this layer being separated from one or more metal plates by either a solid dielectric, a vacuum or an air space. The proposed device is shown in Figure 2.2. These were the first attempts to realize active solid state devices.

The effects to be expected from such arrangements are quite pronounced. The amount of induced charge can be determined from the applied voltage and the capacitance of the system. If the mobility of the charge carriers is known, then the expected change in conductance can be calculated. Consider, for

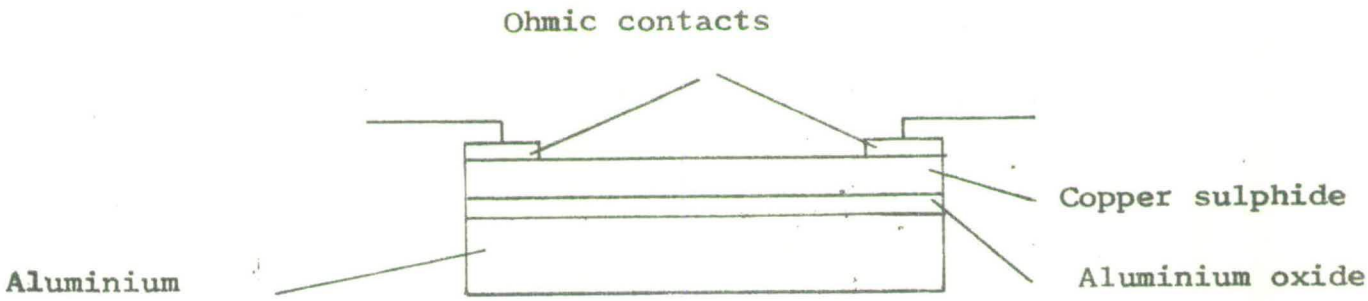


Fig. 2.1 The metal-oxide-semiconductor transistor proposed by Lilienfeld.

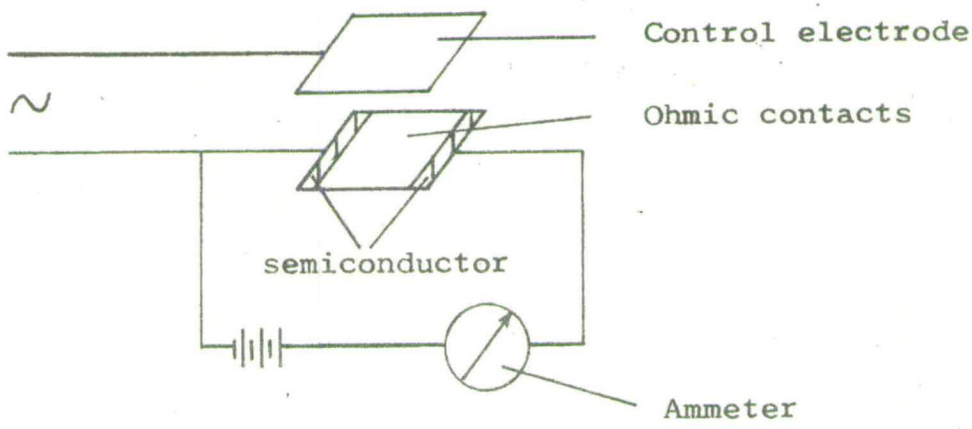


Fig. 2.2 The metal-insulator-semiconductor transistor proposed by Heil.

example, a layer of semiconductor of thickness 1600 Å. Let the resistivity be 10 ohm-cm and the mobility of the electrons be 100 cm^2/volt.sec. The electron concentration in the semiconductor may be calculated from the expression,

$$\sigma = \frac{1}{\rho} = ne\mu$$

Hence, $$n = \frac{1}{1.6} \times 10^{15} \text{ ohms/cm}^3$$

In a layer of thickness t = 1600 Å = 6×10^{-5}cm. there will be nt = 1.0×10^{10} electrons per sq.cm.

Consider now the application of a voltage to the control electrode. Owing to the presence of the transverse electric field a charge will be induced on the surface of the semiconducting layer. A control electrode at a potential of 1.0 volts and separated from the semiconducting layer by a dielectric layer of thickness, 1000 Å, and dielectric constant 5, would produce a field of 10^5volts/cm. This field in turn will produce a displacement of $\varepsilon\varepsilon_0 E$ coulombs. A simple calculation using the above values shows that the number of induced electrons is $0.9 \times 10^{10}/cm^2$. It can be seen that the number of induced electrons is approximately the same as the number normally present. Such a field should thus double the conductivity of the semiconducting layer.

Experiments have been carried out with layers of semiconductors and effects of the kind described on the previous pages have been observed. However, the degree of modulation has been somewhat less than that predicted by calculation. Shockley and Pearson [5] in 1948 took measurements on a number of films of p-type germanium. In these experiments, a thin film of germanium with laterally

spaced contacts was evaporated on to one side of a thin mica sheet. The field electrode consisted of an evaporated metal film deposited on the opposite side of the mica substrate. Copper oxide and n-type silicon were also used. In general, the results showed that only about 10 per cent of the induced charges were effective in changing the conductance. Shockley and Pearson used Bardeen's [6] surface states model of a semiconductor to explain this phenomenon. The concept of surface states was introduced by Tamm [7] who showed from fundamental quantum-mechanical considerations that, in contrast to the situation in bulk, localized states can occur at the surface and have energies distributed in the forbidden range between the filled band and the conduction band. Kronig and Penney [8] approximated the potential energy of an electron in a crystal by a periodic array of square wells and were able to show that the electron energy spectrum consisted of allowed bands separated by forbidden zones. Tamm modified the model to include the abrupt termination of the lattice at the surface and treated the crystal as a periodic array of square wells ending with a potential wall, which corresponds to the binding energy of an electron in the crystal. From this modal theory predicted the presence at the surface of allowed energy levels, surface states, within the forbidden zone. Further modifications to the model were made by Shockley [9], who showed in a more general treatment that surface states can only occur if there is a separate potential trough at the surface, or if the energy bands arising from separate atomic levels overlap. Bardeen proposed that electrons which move in the bulk of the semiconductor could become tightly bound in surface states on the surface of the semiconductor and thus become immobilized. In this way, a portion of the induced charge becomes ineffective, and makes no contribution to the conduct[illegible]

Figure 2.3 represents the surface of an n-type semiconductor and shows, in part (a), eight electrons trapped in the surface states. These electrons repel other electrons in the conduction band and thus produce a layer of depleted conductivity below the surface. The semiconductor surface as a whole is neutral. When the metal capacitor plate is charged positively, an equal negative charge appears on the surface of the semiconductor. In accordance with the results obtained by Shockley and Pearson, 90 per cent of this charge is trapped in surface states. Surface states are believed to be associated with the unsaturated or dangling bonds of the surface atoms. Hence their density should be approximately equal to the number of surface atoms, 10^{14} - 10^{15} per cm^2.

2.2 EVOLUTION OF TFT.

The initial attempts to achieve a solid state amplifier by modulating the electric field at the semiconductor surface were not too successful, and this method of conductivity modulation was subsequently used to study the electronic properties of the semiconductor surfaces. However, an alternative approach to an active solid state field-effect device was conceived by Shockley. In order to get round the effects of surface states and other surface problems, Shockley in 1952 [10] introduced a completely different field effect configuration which made use of the extension of the depletion region of two reverse biased p-n junctions to control the conductance between two electrodes at the ends of a bar of semiconducting material. The construction is shown in Figure 2.4. Carrier concentration is negligible in the space charge regions and as a

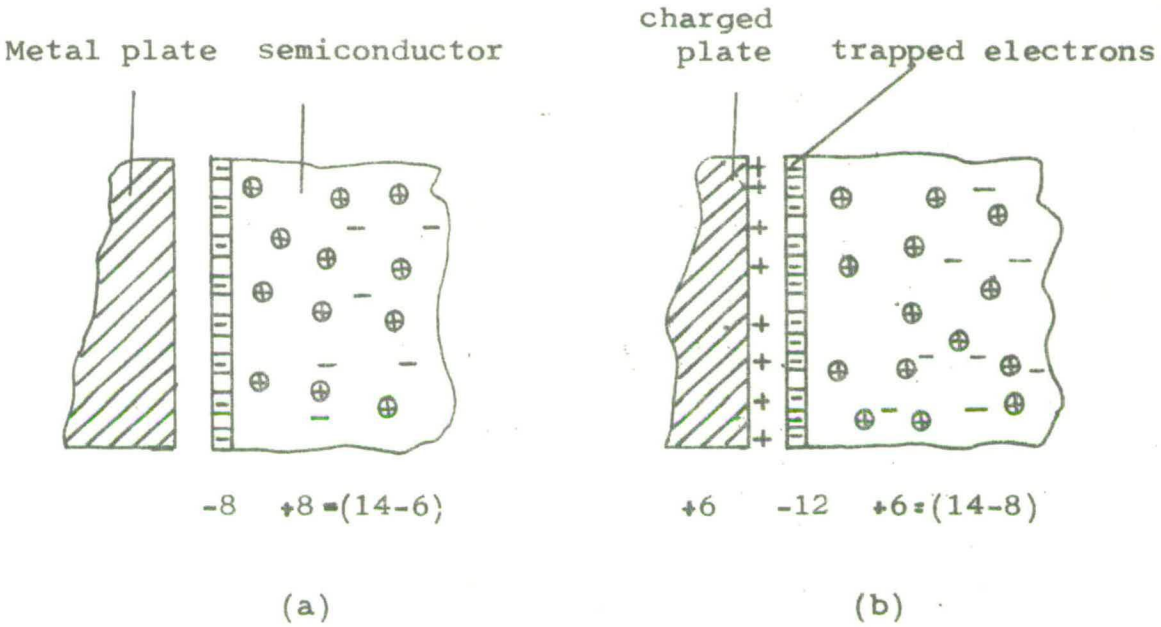


Fig. 2.3 Surface states diagram showing how induced charge may be immobilized (Shockley). (a) neutral semiconductor surface (b) negatively charged surface.

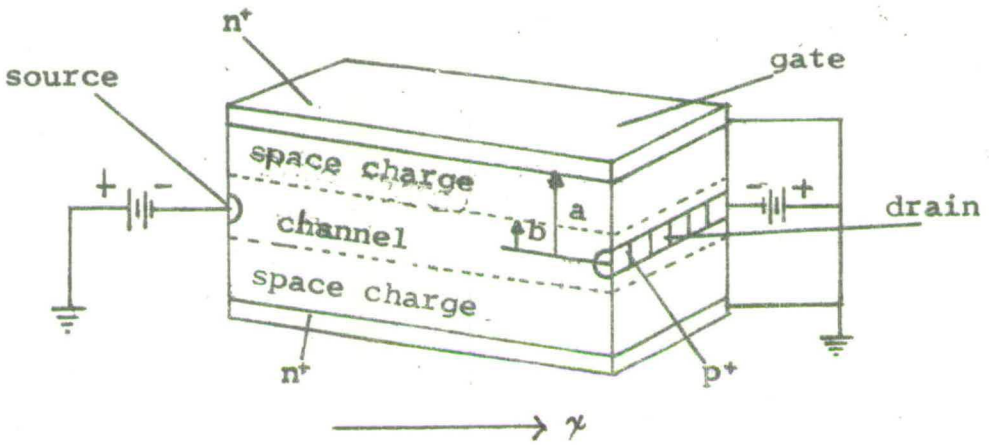


Fig. 2.4 Space charge region and channel in a npn structure

consequence the current flows in a channel, of p-type material in this case, bounded by space charge regions. In Figure 2.4 the reverse bias is the same at each p^+ terminal and the channel width is uniform over the length of the device. If the reverse bias is made larger at one end, the depletion region increases towards that end, and hence the channel narrows with a consequent change in conductance. A further increase in reverse bias causes the two space charge regions to meet and the current through the channel to saturate. This is known as the "pinch-off" point. With this proposal, then, to move away from the surface with its attendant problems and into the bulk, Shockley suggested a method of modulating the current in a block of semiconducting material. The method bears a closer analogue to the vacuum triode than to conventional bipolar transistors. A signal applied between the control electrode and ground has the effect of altering the width of the channel and hence the current through the device. The current flow is carried by one type of carrier only and the device is said to be "unipolar". This is closely analogous to the action of the grid in a thermionic valve. Shockley also suggested a new electrode terminology for field effect devices. He designated the "source" and "drain" as the electrodes into and out of which current flows and the "gate" as the control electrode. Such transistors were subsequently built and tested by Dacey and Ross in 1955 [11] but had the limitation that rather high voltages were required to pinch off the channel owing to the physical dimensions of the device, thus introducing other adverse effects such as mobility deviation due to high fields and junction leakage problems. The junction gate field effect transistor has since become available commercially.

The junction gate field effect transistor described above has little in common with thin film transistors and contains no thin film parts, the semiconductor being a single crystal. However, Shockley made a further contribution to the study of field effect transistors by producing a theoretical analysis to explain the current-voltage relationship of the junction gate transistor and some features of the approach have been used by others to explain the operation of the thin film transistor up to the current saturation point. This will be dicussed in Chapter 3.

Interest in the original idea of conductivity modulation by an electrode insulated from the surface still persisted. The advent of the conventional bipolar transistor produced a concentration of research work on single crystal germanium and silicon, and the subsequent availability of high purity materials facilitated the study of surface phenomena. The stability of silicon surfaces when they were provided with a chemically bound solid-solid interface was studied by Atalla et.al. [12], and stable surfaces were obtained with the silicon-silicon dioxide system when the oxide was thermally grown. The metal oxide semiconductor field effect transistor (MOST) arose directly from this work. The structure of the device is shown in Figure 2.5. The source and drain electrodes are formed, in this case, by a heavy doping of n-type material. Current is injected at the source by forward biasing the p-n junction and modulated by the gate electrode, usually of aluminium, placed on top of the silicon dioxide insulator.

The thin film version of this transistor did not follow directly from the work of Atalla et.al., but originated more or less simultaneously from a quite

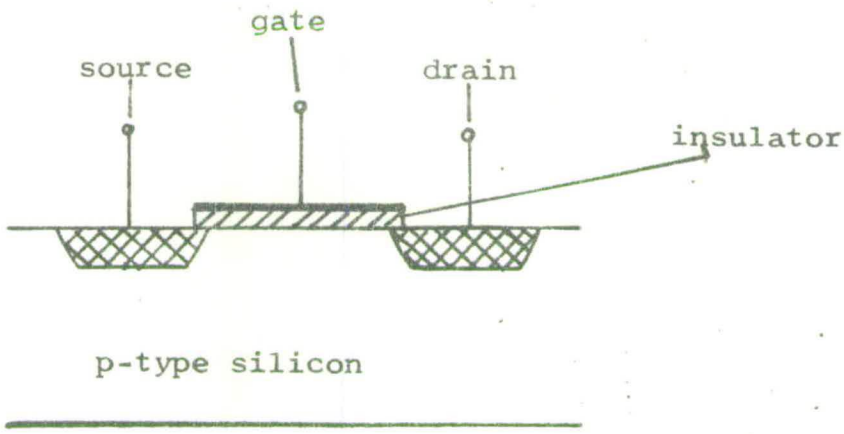


Fig. 2.5 The metal-oxide-semiconductor transistor

different source, namely the study of space charge limited currents (scl) in wide band gap materials. Transient scl currents in cadmium sulphide crystals were observed by Smith and Rose in 1955 [13]. These currents rapidly decayed to very small values because of carrier trapping and considerable work has since been carried out to understand the influence of carrier trapping on scl currents. The Mott-Gurney square law dependance of current upon voltage was observed by Wright [14] in cadmium sulphide in 1958 and scl dielectric diodes were demonstrated by Conning et.al. in 1959 [15]. At this time, Ruppel and Smith [16] reported the fabrication of an experimental solid state triode which operated under scl conditions. A significant departure from the study of single crystals occurred when Dresner and Shallcross [17], drawing on considerable technological experience with thin films of cadmium sulphide which had been acquired in the fabrication of photoconductive devices [18], reported the observation of scl currents in evaporated polycrystalline cadmium sulphide diodes. They had observed rectification ratios of 10^5 using an underlying gold electrode as the injecting contact and an overlying tellurium electrode as the blocking contact.

An early attempt at constructing an scl triode was made by embedding an evaporated grid of tellurium lines in a double layer of evaporated cadmium sulphide [2]. Another approach used a single pair of laterally spaced electrodes with an intervening tellurium gate strip in contact with the cadmium sulphide[16]. Owing to the large trap density and the low mobility of the films, poor control was obtained in these experiments. Finally Weimer [2], by introducing an insulating layer into the gate structure, produced a successful thin film transistor with the configuration shown in Figure 2.6(a).

In Weimer's device, all materials, including the metal electrodes, the semiconductor, and the insulator were deposited by evaporation on an insulating glass substrate. The semiconductor has, in most cases, been a polycrystalline layer of cadmium sulphide, although other materials, notably cadmium selenide, (n-type), and tellurium, (p-type), have been used successfully. The source and drain electrodes were formed of metals which made low resistance contacts with the semiconductor and for this structure, gold was initially used. The requirements for the gate electrode are less stringent and either gold or aluminium can be used. The thickness of each film is greatly exaggerated in the cross-sectional drawings. The metal electrodes are several hundred Angstroms in thickness, the insulating layer ranges from 1000 Å to 2000 Å, and the semiconductor from a few hundred Angstroms to one or more microns. The insulating layers are usually of silicon monoxide or calcium fluoride. The spacing between, and the length of the source and drain electrodes are generally of the order of 10 microns and 0.25 cm respectively. Other configurations are possible for the thin film transistor and these are also shown in Figure 2.6(b) and Figure 2.7(a) and (b). As can be seen from these diagrams, there are two main structures for the thin film transistor, depending upon whether all the electrodes are on one side of the semiconductor, referred to as the coplanar electrode structure, or whether electrodes are placed on both sides of the semiconductor, referred to as the staggered electrode structure. Using these materials and similar dimensions, Weimer was able to fabricate devices with transconductances varying between 4000 μ a/volt and 25,000 μ a/volt.

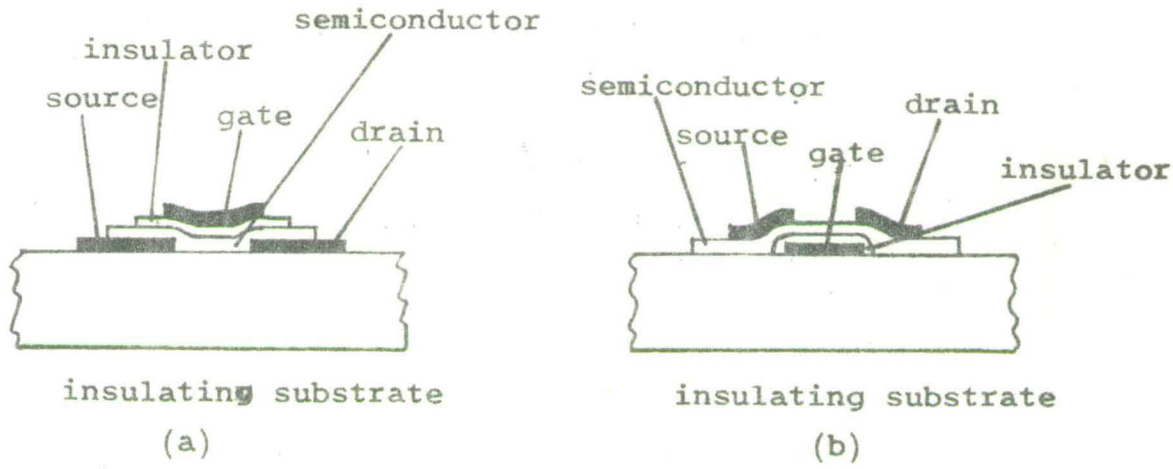


Fig. 2.6 Cross-sectional diagrams of two T.F.T.s having the "staggered electrode" structure.

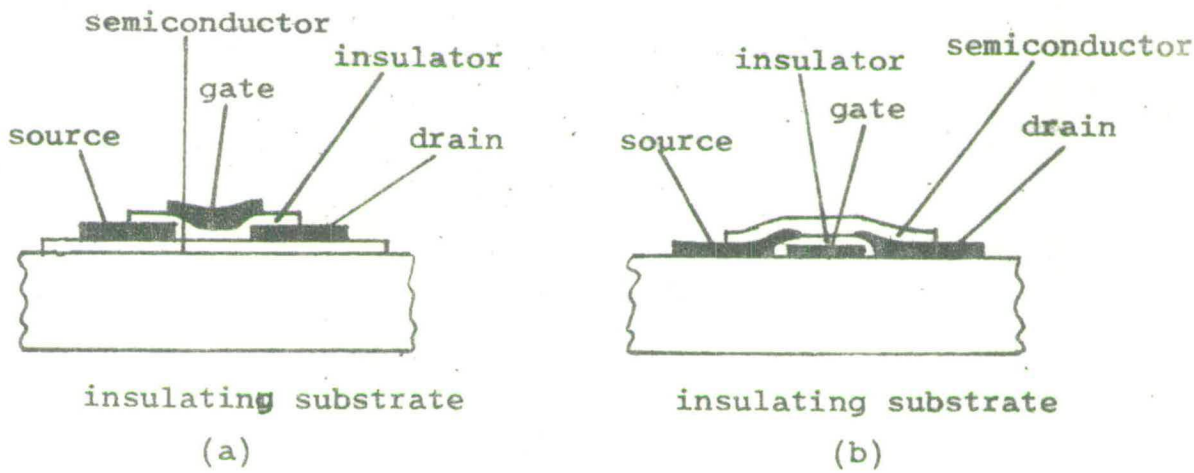


Fig. 2.7 Cross-sectional diagrams of two T.F.T.s having the "co-planar electrode" structure.

2.3 PHYSICAL PROCESSES IN TFT.

The structures used for the classical field effect experiments, in which current modulation was found to be impractical, and the thin film transistor, in which current modulation is possible, have a distinct similarity, the main differences being in the materials and the dimensions used. The very thin evaporated layer of insulation in the thin film transistor allows the control electrode to be anything up to 1000 times closer to the semiconductor than was possible in the early field effect experiments, where an insulating spacer of mica or a vacuum gap of 12 microns was fairly typical. The difference yields correspondingly higher transconductances and a more effective control of the surface potential. Owing to the high capacitance, free carriers can be drawn to the interface at moderate voltages to fill traps and surface states and so inactivate them. The thermally grown oxide on silicon in the MOS transistor also provides a close spacing. The choice of insulating material also determines the surface potential of the semiconductor. For example, with cadmium sulphide, calcium fluoride forms a depletion layer at the surface, whereas silicon oxide can form either a depletion or accumulation layer depending on whether monoxide or a dioxide is used. By mixing calcium fluoride and silicon monoxide in different proportions, it is possible to vary the surface potential between the values obtained for these materials separately.[19]

It is obvious that the semiconductor to insulator interface has some considerable bearing on the operation of a thin film transistor. The formation of a depletion layer at the interface causes no drain current to flow in the transistor when there is zero gate voltage, and it is necessary to apply a positive voltage to

the gate in the case of an n-type semiconductor to turn the transistor on. Such a circuit is said to operate in the enhancement mode. A depletion type thin film transistor is one which has a useful current at zero gate bias, and this is provided by the formation of an accumulation layer at the semiconductor to insulator interface. In this case, a negative gate voltage is required to turn the transistor off. Such a unit is capable of operation in either the depletion or enhancement mode.

Consider now the effect of surface states on the energy bands of an n-type semiconductor. In the absence of surface states, the energy bands of the semiconductor continue flat up to the surface, provided there is no external field, Figure 2.8(a). When acceptor-like surface states are introduced below the Fermi level, they will not be in equilibrium with the energy bands as long as they remain unoccupied. The situation is illustrated in Figure 2.8(b), where the surface states have been introduced at an energy level E_t. Since the states are empty and below the Fermi level, some of the conduction band electrons fall into them In the process the surface becomes negatively charged, and consequently the energy bands at the surface bend upwards with respect to the Fermi level. Since the energy position of the surface states in the forbidden gap is determined by short-range atomic forces and is not affected by the bulk potential, the surface levels rise together with the band edges. The process of charge transfer continues until equilibrium is reached - Figure 2.8(c). Thus the larger the surface state density, the greater the bending of bands near the surface. The situation for donor-like states is analogous and shown in Figure 2.9.

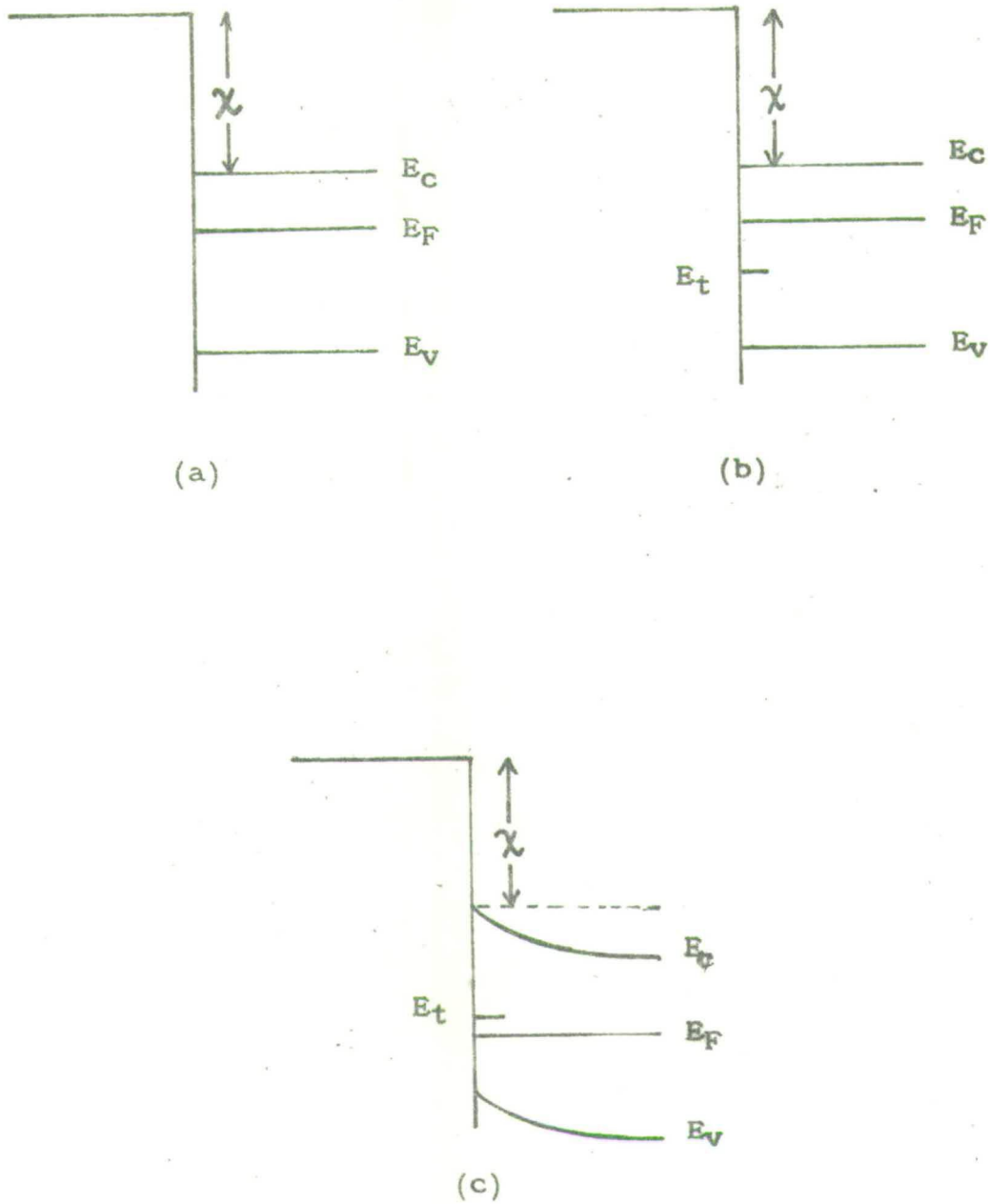


Fig. 2.8 Energy level diagram for an n-type semiconductor (a) no surface states (b) Acceptor-like surface states not at equilibrium (c) at equilibrium.

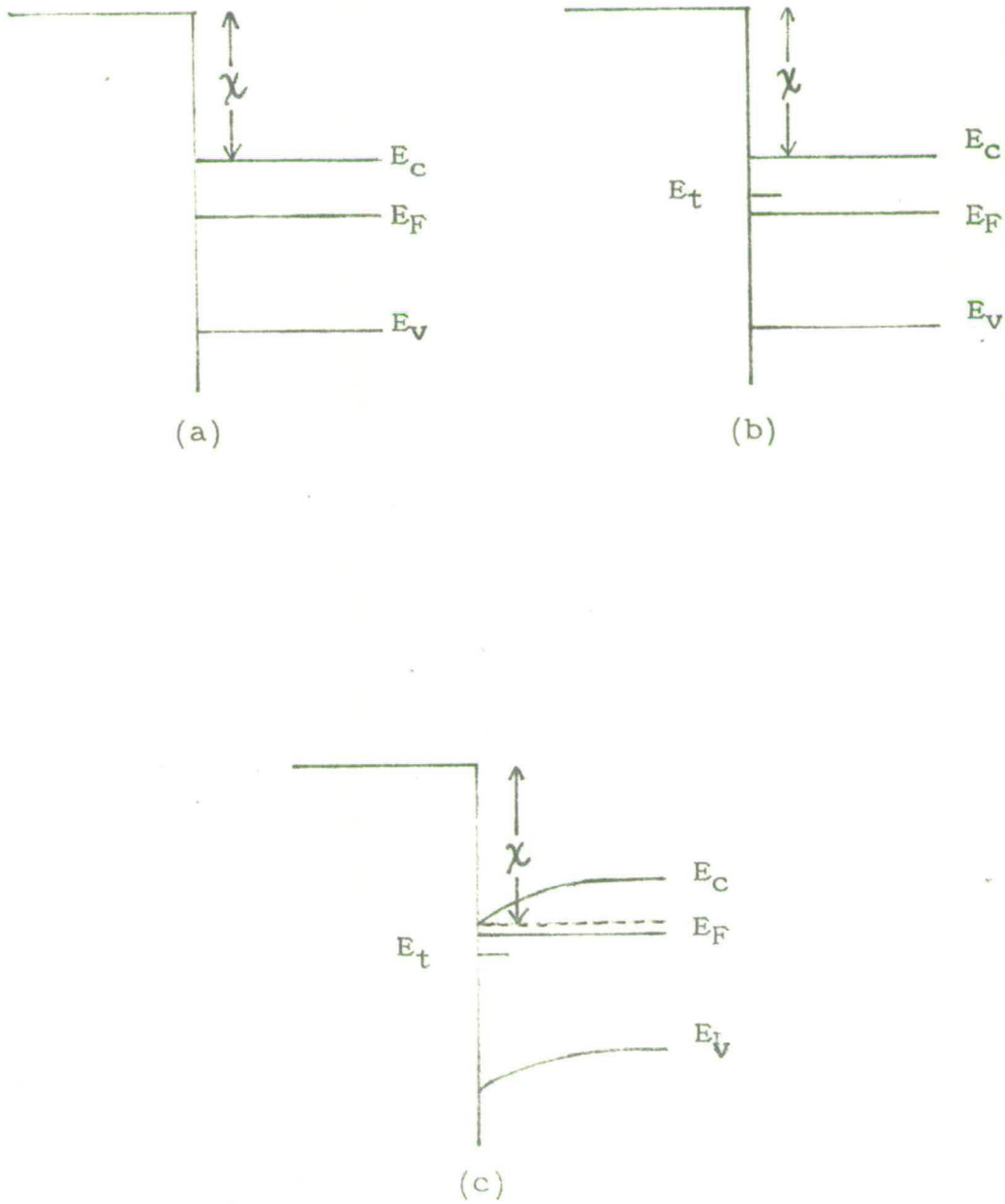


Fig. 2.9 Energy level diagram for an n-type semiconductor (a) no surface states (b) donor like surface states not at equilibrium (c) at equilibrium.

Weimer [20] has considered the role that surface states at the semiconductor to insulator interface play in the performance of the thin film transistor and reasons in the following manner. Figure 2.10(a) shows the energy band structure for the gate-insulator-semiconductor system of a thin film transistor. The contact potential difference due to the work function of the metal gate may also play a part. A system with a high density of acceptor-like states or deep traps requires a positive gate bias to convert the depletion layer into an accumulation layer, Figure 2.10(b), and so turn the transistor on. This condition yields an enhancement type transistor. Let N_o represent the number of unfilled traps or surface states initially present, and let C_g be the gate capacitance, then the gate bias required for onset of current is given by:

$$V_o = \frac{N_o q}{C_g}$$

Likewise a high density of donor-like states at the interface provides an accumulation layer at zero bias and yields a depletion type transistor - Figure 2.10(c) and (d). In this case, V_o is the gate bias required to turn the device off and N_o represents the number of electrons initially present in the gap region. Weimer has attempted to control the value of V_o in the fabrication of thin film transistors by processing the semiconductor prior to evaporation of the insulator and also by proper choice of insulator and gate materials.

2.4 CONSIDERATION OF MATERIALS FOR TFT.

Weimer's choice of cadmium sulphide for the semiconducting layer was dictated

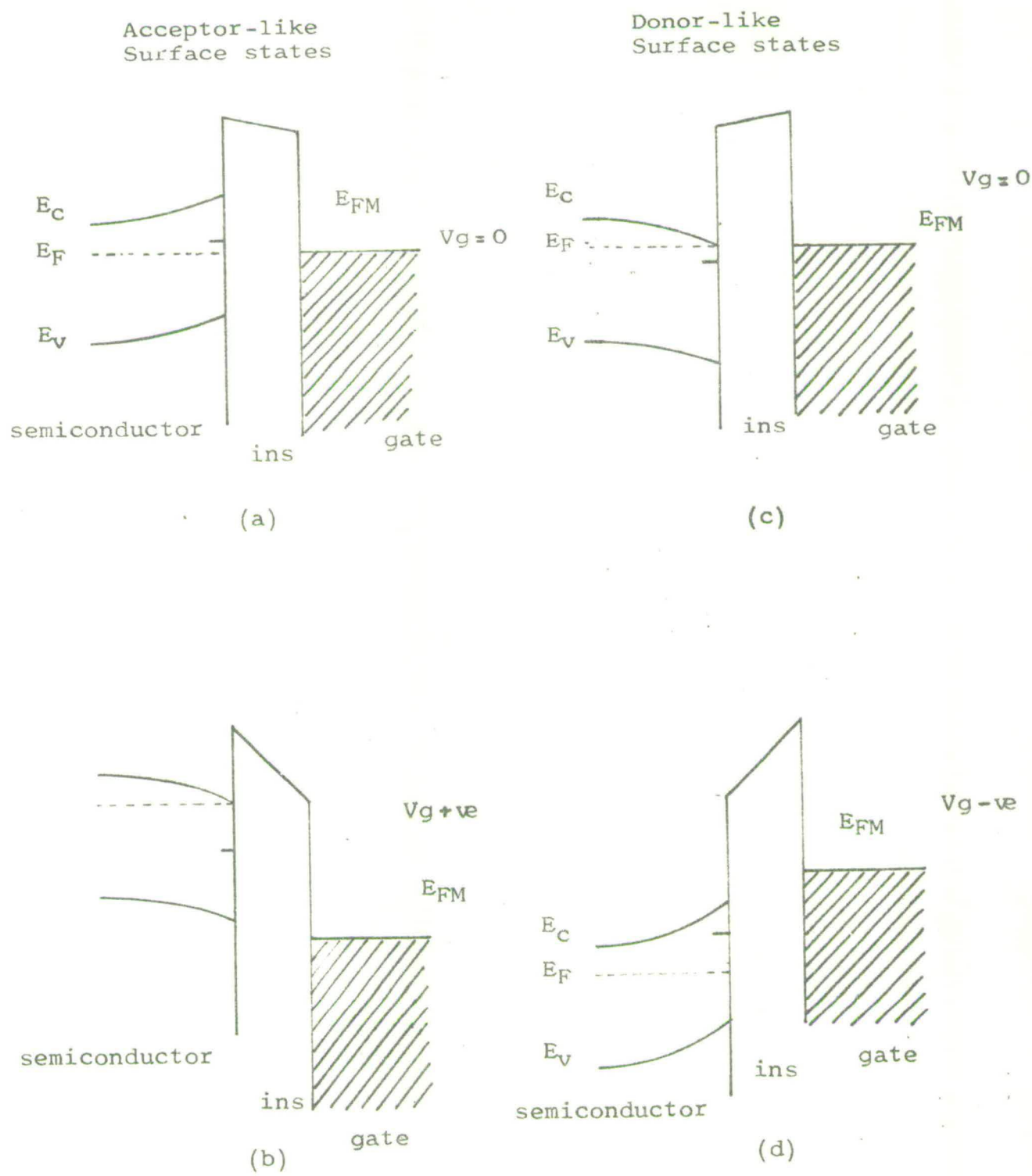


Fig. 2.10 The effect of donor-like and acceptor-like surface states upon the energy bands of the semiconductor at the insulator interface.

by the volume of information accumulated over some years of study of its photoconductive behaviour. In previous years in this department, although there was no experience in evaporation techniques to draw on, single crystal platelets of cadmium sulphide had been grown by the vapour phase technique and used to study the fabrication problems and noise properties associated with insulator diodes.[21, 22]. The decision to use cadmium sulphide as the semiconductor in a study of the thin film transistor was, in a sense, a natural extension of this work.

Several different materials have been used as insulators in thin film transistors, the commonest being calcium fluoride, and silicon monoxide. It was decided to use silicon monoxide. This material has been ever present over the years in the ~~evaluation~~ evolution of thin film circuits, being mainly used as a dielectric for capacitors. Although it is relatively easy to evaporate, its reaction with oxygen leaves some doubt as to its ultimate composition as an evaporated thin film. However, the fact that it was readily obtainable and a large volume of technical information was available led to its selection.

2.4.1 SUBSTRATE MATERIALS.

The substrate does not play an ~~actual~~ active role in the electrical performance of a thin film transistor, but its properties are important and capable of having considerable effect on the electrical performance of the device. Ideally a substrate should have the following properties:

1. Chemical inertness.
2. Low electrical conductivity.
3. A flat, smooth surface.
4. High thermal conductivity.
5. Compatibility with vacuum processing.
6. Be readily available at low cost.

Few materials, if any, which satisfy all these requirements are available at present. One of the main considerations is that since a great deal of processing takes place in vacuum and at elevated temperatures, organic plastic materials cannot be used. Thus the only materials suitable are glass and ceramics. The well established use of high quality ceramics for discrete film resistors has led to the use of ceramic substrates for microcircuits both in the United States and in this country. In addition, a number of companies advocate the use of glass substrates.

From the point of view of thin films, a good finish is necessary to provide uniformity and reproducibility of component values. R.J. Settzo [23] of the Corning Glass Works has examined materials for their suitability as substrates for thin resistive films of tin oxide and his report suggested that a high alumina ceramic with its high mechanical strength and high thermal conductivity would be the preferable substrate to use, were it not for the normal surface condition of the material. This disadvantage of ceramics can be overcome if the surface is coated with a suitable glaze. The problem with this approach is that most low temperature glazes have a high alkali content which influences the electrical conductivity and corrosion resistance and so makes them unsuitable for microcircuits. Considerable advances have been made and several

manufacturers have developed a glazed ceramic of sufficient flatness and with a low alkali glass surface. However, the necessary surface finish for thin film components can most readily be obtained on glass. Soda glass, of which ordinary microscope slides are made, cannot be used owing to the alkali content giving rise to conduction by sodium ion migration. To overcome this, slides of borosilicate glass were used. In addition, glass is transparent and this property can be used to advantage if it is necessary to monitor the formation or thickness of the film by optical means. In fact considerable use of this property was made when depositing the thin film of semiconducting cadmium sulphide.

The crystalline structure of the substrate can also be important. The use of amorphous materials such as glass or a ceramic for substrates has little influence on the crystalline growth of the thin evaporated film and, in order to form single crystal films or increase the crystallite size, it is necessary to use a substrate with a crystalline structure similar to that of the film. Mica has a crystalline structure not too dissimilar from that of cadmium sulphide and freshly cleaned slices were also used as substrates in an attempt to encourage an epitaxial growth.

2.5 MASKING PROCEDURE.

In the formation of evaporated thin films of materials it is nearly always necessary to form a repeatable defined profile. Take, for example, the evaporation of a thin film resistor. For a given thickness of film, the aspect ratio determines the value of the resistor. Hence, the accuracy with

which the aspect ratio can be found determines the tolerance within which a resistor can be deposited. The ~~working~~ masking of the substrate can be of some importance, particularly when high accuracy is required. Two main methods of masking are used, usually referred to as:

1. In contact masking.
2. Out of contact masking.

In the first method the film is evaporated over the whole substrate, and then covered with a photo-sensitive resist. The resist is exposed through a photograph of the desired pattern to ultra-violet light, which polymerises it. The unexposed resist is then dissolved away to expose the evaporated film underneath, which in turn can be selectively removed by chemical etching, thus leaving the required pattern.

Out of contact masking has the virtue of simplicity but does not lend itself to a very accurate delineation of the pattern. The required film profile is formed on the substrate merely by evaporating the material through a metal foil on which the pattern has previously been cut, usually by the photo-sensitive resist technique. Out of contact masking has been used throughout this work.

It was realized that a combination of both methods could be used in the fabrication of a TFT. In an inverted coplanar structure it would be possible to form a very narrow gate electrode by in contact masking, and add the remaining layers using out of contact masking. Likewise, the source-drain electrodes in a staggered electrode TFT could be formed by selective etching and it is almost certain that the spacing between source and drain attainable

by this method would be smaller than by out of contact masking. Thus, the photo-resist process does offer a good method for forming the initial layers of a TFT, provided that the layer is metallic, i.e. either the gate or the source and drain electrodes. However, other factors have to be taken into account, in particular, the problem of keeping the substrate clean. Thin films of some materials stick better to glass than others, and in general, it appears that elements which tend to oxidise readily adhere much more strongly. This high adhesion of oxygen active metals to glass has also been observed in glass to metal seal technology and, as an explanation, bonding of the metal is believed to occur by chemical reaction with an OH layer on the glass. Thin films of the noble elements, such as gold, scarcely adhere at all to glass and can be rubbed off very easily. On the other hand, it is almost impossible to remove a thin film of chromium from a glass substrate. Aluminium, which readily forms aluminium oxide, also adheres well. However, no thin film will adhere to the substrate unless the substrate is scrupulously clean. The in contact photo-resist masking process demands that the substrate be cleaned prior to the evaporation of the thin film. Selective etching is then carried out by masking in various chemical compounds and the substrate undergoes a fair amount of handling and great care has to be exercised if additional cleaning prior to further evaporations is to be avoided. "Clean room" facilities were not available during the experimental work, and it was thought desirable to reduce the handling and chemical processing of the substrate to a minimum. It was thus decided to use out of contact masking entirely. In addition, this adds a certain uniformity to the process of fabricating a thin film transistor and certainly allows the different layers to be evaporated in any order desired.

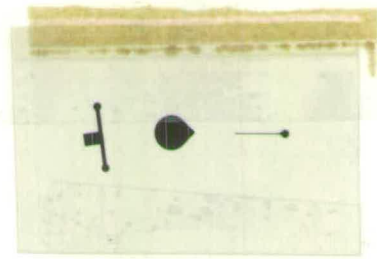
The problem of obtaining a suitable masking material remained. Brass foil was readily available in many thicknesses with a minimum of 1 mil and its easiness to etch chemically made it attractive. The high vapour pressure of the zinc proportion in brass does not recommend it for use in high vacuum systems, particularly if elevated temperatures are required. As the vacuum system available in this laboratory only attained at best 10^{-6} torr and the vapour pressure of zinc at 350°C is 10^{-10} torr, the use of brass as a masking material was not excluded initially. However, two other properties made its use impossible. Firstly, brass reacts chemically with cadmium sulphide, and secondly, it crinkles very easily, so that close contact with a substrate is not possible. A sharply delineated pattern of the evaporated film cannot then be obtained.

The most suitable material was found to be mild steel feeler strip. This can be readily obtained in a number of thicknesses with a minimum of 1 mil, but unfortunately is only available at a fixed length and breadth of 12 ins. and 0.5 in. respectively. While this length was adequate, the breadth was rather narrow and did not mask completely the 3cm x 2cm borosilicate glass substrate. Apart from a tendency to rust if left exposed to the atmosphere, the feeler strip was very easy to etch, had a smooth surface and did not crinkle.

Ordinary printed circuit techniques were used to make the masks. It is necessary to make a drawing of the pattern to a printed scale, photograph it and reduce it in size to produce a negative of the exact dimensions of the mask. The foil is placed on a platform, wetted with a small quantity of

photo-resist and spun to produce a uniformly thick layer of photo-resist. The required pattern is now produced by first exposing the photo-resist through the negative to ultra-violet light. It is important that the negative and the coated foil should be in intimate contact with one another. This is best ensured by using a vacuum printing frame with a sheet of glass on which the negative and foil are placed. A flexible membrane is placed over the negative and foil, and the air between the plate and membrane is removed by vacuum pumping, causing the membrane to exert a uniform pressure over the glass plate. After developing the exposed resist, the foil can be etched by gentle brushing with ferric chloride or warm dilute nitric acid. Care should be taken to place the emulsion side of the negative next to the resist, otherwise the ultra-violet light is scattered behind the emulsion. This is usually of little consequence when making printed circuit boards, but is certainly detrimental to the formation of masks containing lines a few mils wide.

To illustrate the technique, Figure 2.11 shows the negative used to form the masks for the evaporation of a coplanar thin film transistor. During the evaporation, a fine wire was placed in position midway across mask (a) to provide the separation between the source and drain electrodes. In fact, the structure in Figure 2.11 was the one finally chosen for the thin film transistor, with the evaporations being performed in the order listed. This is the coplanar electrode structure. The choice of configuration was dictated to a large extent by the evaporation difficulties associated with the cadmium sulphide film.



(a) (b) (c)

Figure 2.11 Photographic negative used to form masks (a) source-drain electrodes (b) insulator (c) gate electrode.

2.6 CONSIDERATION OF TFT CONFIGURATION.

Cadmium sulphide tends to dissociate readily when heated. The vapour pressures of the constituents differ greatly, and this results in the formation of low resistivity cadmium rich films. It is sufficient at the moment to say that careful evaporation of cadmium sulphide in a separate system is required, and post evaporation heat treatment in an inert atmosphere is generally necessary to improve the stoichiometry of the films. These processes will be described in a later chapter. Furthermore, gold, which normally forms a blocking contact with cadmium sulphide, may be used to inject electrons under certain conditions, viz. when it is deposited beneath the cadmium sulphide. Hence, in some TFT configurations, gold in addition to aluminium is available for an ohmic contact. With these facts in mind and with reference to Table 1, consider now in turn the four different configurations as shown in Figure 2.6 and Figure 2.7.

i. The Staggered Electrode Structure.

As the cadmium sulphide has to be deposited in a separate system, the evaporation sequence must be interrupted after evaporating the source and drain contacts on to the substrate. This exposure of the system to the atmosphere followed by a heat treatment process for the cadmium sulphide makes it inadvisable to use aluminium as an injecting contact, owing to its readiness to oxidize. The use of gold also presents a difficulty in that it does not adhere strongly to glass. It is necessary to first deposit an underlay of chromium. To ensure a sharply defined narrow gap between the source

STAGGERED TFT STRUCTURE			
Step	Semiconductor evaporator	External processing	Precision mask evaporator
1			S - D evaporation
2	Semiconductor deposition		
3		Semiconductor heat treatment	
4			Insulator deposition
5			Gate evaporation

COPLANAR TFT STRUCTURE			
Step	Semiconductor evaporator	External processing	Precision mask evaporator
1	Semiconductor deposition		
2		Semiconductor heat treatment	
3			S - D evaporation
4			Insulator deposition
5			Gate evaporation

Table 2.1. Fabrication procedure for making the two main types of thin film transistor.

and drain, a double evaporation such as this should be avoided. Having removed the substrate to deposit and heat treat the cadmium sulphide, it is necessary to realign the mask changing system to ensure that the gate electrode is evaporated directly over the source-drain gap. In addition, the surface of the cadmium sulphide can easily be damaged during the realignment.

ii. The Inverted Staggered Electrode Structure.

This unit has the fabrication difficulties of the staggered electrode structure. Furthermore, the source-drain region is exposed to the atmosphere and would certainly require encapsulation. This would alter the surface potential of the cadmium sulphide within the source-drain region and add another parameter to be considered in any assesment of the performance of the device.

iii. The Coplanar Electrode Structure.

In this configuration, the cadmium sulphide may be deposited and heat treated without having to consider the effect on the other layers. Also, since the sequence of evaporations is not broken between the formation of the source and drain electrodes and the gate electrode, no critical realignment of the masking system is necessary. Apart from the evaporation of cadmium sulphide, the transistor can be formed during one pump down of the vacuum system. The fabrication process is simple and straightforward.

iv. The Inverted Coplanar Electrode Structure.

This unit has the advantages in fabrication of the coplanar configuration. However, the fact that the final evaporation is the cadmium layer, does mean

that all the previously deposited layers, i.e. the complete transistor, are also subjected to heat treatment.

It is obvious that there is a technological advantage in the use of the coplanar electrode structure, and that it lies in the fact that the cadmium sulphide deposition and processing can be done prior to the laying down of the electrodes. However, the use of a different semiconductor, elemental rather than compound, would require a reappraisal of the fabrication difficulties involved in the various configurations.

CHAPTER 3.

THEORY OF THE THIN FILM TRANSISTOR.

3.1 THE GRADUAL APPROXIMATION.

As described by Shockley, the unipolar field effect transistor utilizes the depletion region of a reverse biased p-n junction to control the effective cross-section, and hence the conductance, of a bar of semiconductor material, Figure 2.4. Shockley was able to derive an expression describing the static current voltage characteristic by relating the conductance of the channel to the reverse bias voltage. To do this, he used what has come to be known as the "gradual approximation".

Consider the situation in Figure 2.4 when no current flows. If V represents the potential, E_y the electric field and y the distance from the centre of the p-layer, then

$$\frac{d^2V}{dy^2} = -\frac{\rho(y)}{\epsilon_o \epsilon_1}$$

where $\rho(y)$ is the charge density. The depletion layer extends to $y = b$ and therefore $E_y = o$ for $y < b$. Near $y = b$ the charge density changes from $\rho = 0$ to $\rho = \rho_o$

$$\therefore \qquad \frac{dE_y}{dy} = -\frac{\rho_o}{\epsilon_o \epsilon_1} \qquad \text{for } y > b$$

$$\text{and} \qquad E_y = -\frac{\rho_o (y - b)}{\epsilon_1 \epsilon_o}$$

Since the n-region is heavily doped, the reverse bias voltage may be considered to occur wholly across the p-region. Thus,

$$V = -\int E_y dy$$

$$= \frac{\rho_o}{\epsilon_o \epsilon_1} \int (y - b) dy$$

$$= \frac{\rho_o}{2\epsilon_o \epsilon_1} [(y - b)^2 - (a - b)^2]$$

Where the constant of integration has been chosen to make V = 0 when y = a, corresponding to grounding the n-region. The potential at y = b, the reverse bias, is

$$V(b) = -\frac{\rho_o}{2\epsilon_o \epsilon_1} (a - b)^2$$

Shockley used W, a positive quantity, to represent the reverse bias, giving

$$W = \frac{\rho_o}{2\epsilon_o \epsilon_1} (a - b)^2$$

$$= \frac{\rho_o a^2}{2\epsilon_o \epsilon_1} \left(1 - \frac{b}{a}\right)^2 \qquad (3.1)$$

When b = 0, the depletion region extends completely across the p-region. The magnitude of the reverse bias required for this situation is

$$W_o = \frac{\rho_o a^2}{2\epsilon_o \epsilon_1}$$

Equation 3.1 can be written in the form

$$W = \left(1 - \frac{b}{a}\right)^2 W_o \qquad (3.1a)$$

W_o is the voltage required to reduce the channel to zero and so pinch off the conducting path. Equation 3.1 relates the channel thickness to the reverse bias and the pinch-off voltage.

When the current flows in the x-direction in the channel, an electric field with a component E_x must be present. The potential changes along the channel and hence the reverse voltage between the channel and the n^+-region varies As a result, the channel width varies with x. Consequently,

$$E_x = -\frac{dV}{dx} \neq 0$$

and in the general case $\frac{d^2V}{dx^2}$ will not vanish. In such circumstances the reverse bias, W, cannot be expressed as a function of the channel width, b, alone and in calculating the relationship between W and b it is necessary to consider a two-dimensional Poissons' equation, including $\frac{dE_x}{dx}$. However, if $\frac{dE_x}{dx}$ is small compared to $\frac{\rho_o}{\epsilon_o \epsilon_1}$ an approximation may be made by using the one-dimensional case which was derived for zero current, and considering the electric field in the depletion

region to be entirely transverse in direction. The approximation is valid when conditions change gradually along the channel, hence the term "gradual approximation".

For the gradual case, the conductance of the channel can be calculated by making use of Equation 3.1a

$$b = b(W) = \{1 - \left(\frac{W}{W_o}\right)^{\frac{1}{2}}\}a$$

If σ is the conductivity, the conductance per unit square of a layer 2b thick is

$$g(W) = 2\sigma b(W)$$

or

$$g(W) = 2\sigma\{1 - \left(\frac{W}{W_o}\right)^{\frac{1}{2}}\}$$

The current, I, in the device can be calculated from

$$I = g(W)\frac{dW}{dx}$$

If the values of W at the source and drain are W_s and W_d and L is their separation

$$I = \frac{1}{L}\int_{W_S}^{W_D} g(W)dW$$

Shockley has pointed out that this is the basic equation for a field effect device within the terms of the gradual approximation, and can be used to describe structures other than Figure 2.4, provided an appropriate g(W) can be derived.

3.2 ANALYSIS DUE TO BORKAN AND WEIMAR.

A similar approximation has been applied in the theoretical analysis of insulated-gate field effect transistors, both MOS and thin film types. In these cases, if the channel length is several times longer than the thickness of the insulating layer and the drain voltage is of the same order of magnitude as the gate voltage, the electric field in the insulating layer is approximately transverse in direction. The following analysis of the thin film transistor has been suggested by Borkan and Weimer [24] and, as mentioned by these authors, is based on unpublished work of A. Many. In a sense, the analysis follows Shockley's technique and, implicitly, an expression for g(W) is derived and used in the equation

$$I \int dx = \int g(W)\, dW$$

to obtain the drain characteristics.

In this analysis, a homogenous layer of semiconductor of thickness, h, as shown in Figure 3.1. is assumed. The gap between the source and drain electrodes provides an active region of length, L, and a width, W. The gate electrode is a narrow metal strip having a width equal to the channel length and is spaced from the semiconductor by an insulating layer of thickness, t. Two simplifying assumptions are made:

1. The gate capacitance is a constant independent of the gate voltage.
2. The mobility of the carriers throughout the conducting channel is a constant independent of the gate voltage over the useful operating range of the device.

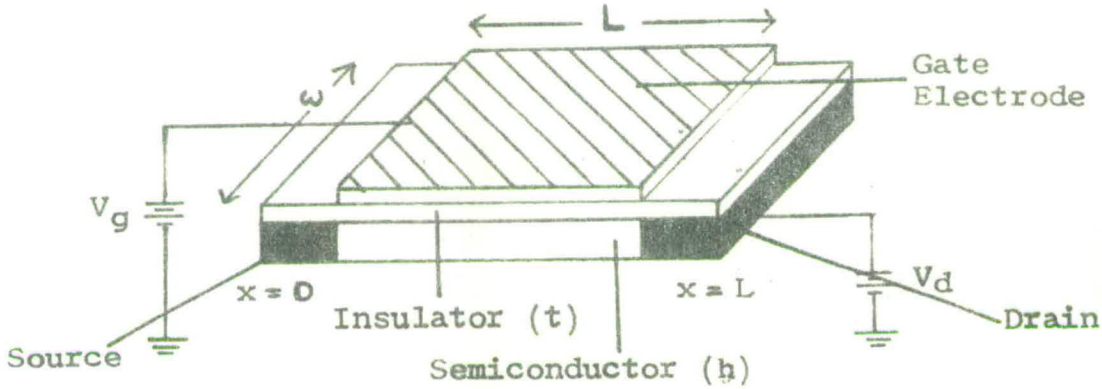


Fig. 3.1 T.F.T. structure use for analysis

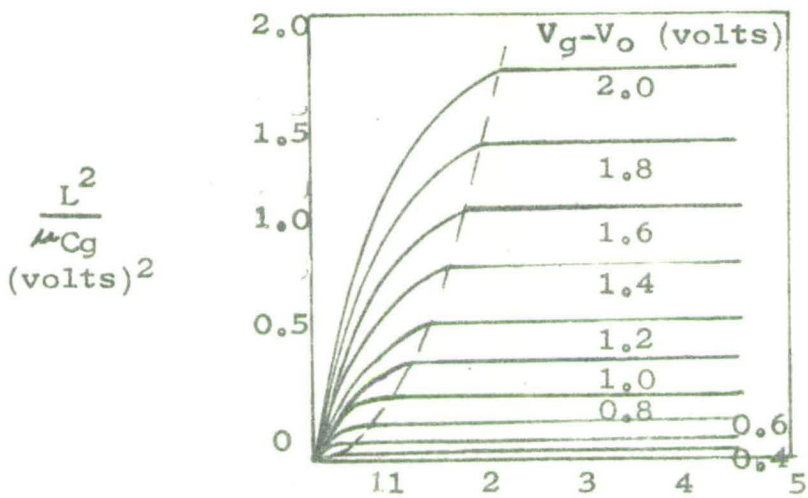


Fig. 3.2 Theoretically predicted T.F.T. drain characteristics.

Let the capacitance across the insulator be C_g. The potentials applied to the gate and drain electrodes relative to the source electrode are V_g and V_d and the potential of the semiconductor at an arbitrary point, x, measured from the source electrode is given by V(x). With $\Delta N(x)$ charges per unit area impressed on the gate electrode, an equal number of charges of q coulombs per charge is induced in the semiconductor. The charge induced per unit area in the channel region by application of a gate voltage V_g is given by

$$q\Delta N(x) = \frac{C_g}{wL}[V_g - V(x)] \qquad (3.2)$$

Now let μ_d = effective drift mobility.

E_x = electric field between source and drain.

N_o = the total number of charges initially present in the gap region of the semiconductor.

N_o is positive for a depletion type unit having an initial excess of donor-type states and negative for an enhancement typeunit having an initial excess of unfilled traps or acceptor-type states. The value of N_o is a function of the volume density of donors and acceptors as well as the thickness of the semiconductor. The drift velocity, v_d, of an electron is related to the electric field.

$$v_d = \mu_d E$$

Hence the current density, J, can be written as

$$J = nq\mu_d E$$

The drain current may be calculated by summing the contributions from the

initially present charge and the induced charge. Thus the total drain current I_d may be expressed by

$$I_d = \frac{qwN_o}{wL}\mu_d E_x + qw\Delta N(x)\mu_d E_x$$

$$= w\mu_d\left[\frac{qN_o}{wL} + q\Delta N(x)\right]E_x \qquad (3.3)$$

Combining equations 3.2 and 3.3

$$I_d = w\mu_d\left[\frac{qN_o}{wL} + \frac{C_g}{wL}(V_g - V(x))\right]E_x$$

$$= \frac{\mu_d C_g}{L}\left[\frac{qN_o}{C_g} + V_g - V(x)\right]\frac{dV(x)}{dx}$$

$$\therefore \quad I_d dx = \frac{\mu_d C_g}{L}\left[\frac{qN_o}{C_g} + V_g - V(x)\right]dV(x)$$

$$I_d\int_0^L dx = \frac{\mu_d C_g}{L}\int_0^{V_d}\left[\frac{qN_o}{C_g} + V_g - V(x)\right]dV(x)$$

Hence

$$I_d L = \frac{\mu_d C_g}{L}\left[\frac{qN_o V(x)}{C_g} + V_g V(x) - \frac{V(x)^2}{2}\right]_o^{V_d}$$

$$\therefore \quad I_d = \frac{\mu_d C_g}{L^2}\left[\left(\frac{qN_o}{C_g} + V_g\right)V_d - \frac{V_d^2}{2}\right] \qquad (3.4)$$

The term $\frac{qN_o}{C_g}$ in Equation 3.4 may be replaced by a voltage $-V_o$, where V_o is the gate voltage required for the onset of drain current. For an n-type semiconductor, V_o is positive for an enhencement type unit and negative for a depletion type unit. The expression for the drain current becomes

$$I_d = \frac{\mu_d C_g}{L^2}[(V_g - V_o)V_d - \frac{V_d^2}{2}] \qquad (3.5)$$

This equation relates the drain current to both the drain and gate voltages. The resulting characteristics calculated from the equation are shown in Figure 3.2. Figure 3.4 is valid for $0 \leq V_d < V_g - V_o$ up to the knee of the I_d versus V_d characteristic, the point where the slope is zero. Beyond the knee the current is assumed to be substantially constant as predicted by Shockley for the unipolar field effect transistor.

It was suggested by Weimer that the main operating mechanism in the thin film transistor was the formation of a conducting channel by field effect in the semiconductor adjacent to the under-surface of the insulator. To test this proposal, Weimer compared theoretically predicted properties of the drain characteristic with experimentally determined properties. In particular, the maximum drain current at the knee can be determined from Equation 3.5. This occurs when

$$V_d = V_g - V_o$$

and so

$$I_{d(max)} = \frac{\mu C_g}{2L^2}(V_g - V_o)^2$$

Hence there is a square law relationship between the saturated drain current and the effective gate voltage. Good agreement was found for this and other properties, notably the output conductivity and the transconductance below the knee, and thus good evidence was provided for Weimer's proposal that the operation of the TFT is similar to that of the conventional field effect transistor in that the observed characteristics ~~revert~~ result from modulation of the conductivity of a channel connecting the source and drain electrodes.

In their analysis, Borkan and Weimer have assumed the gate capacitance C_g to remain constant. Measurements [25] have been made on coplanar thin film transistors of the variation of gate capacitance with gate voltage and it has been found that for both source and drain at ground potential the capacitance increases and levels off with gate voltage, but when the drain is positive, as it would be in normal operation, the capacitance reaches a maximum near the value of gate voltage required for the onset of drain current. The gate capacitance thus changes according to the variation of the thickness of the space charge region. At high drain voltages, the major portion of the capacitance appears between the gate and source.

Neumark [26] has considered the case when all the voltage applied to the gate electrode does not fall across the insulating layer but extends into depletion regions. In the theory the capacitances of the insulating layer and the depleted part of the semiconductor are included and the approach given by Borkan and Weimer is followed. The theory is again only valid at most up to the pinch-off point. Furthermore, as there are no depleted regions in the thin film transistor below the pinch-off point, the theory does little to further the description of its operation.

The second assumption made in the Borkan-Weimer analysis - that the mobility of the carriers in the conducting channel was constant and independent of the gate voltage - has also been investigated. [2] Using the expression for drain current, Equation 3.5, the mutual conductance below pinch-off can be obtained by differentiating with respect to V_g. Thus,

$$g_m = \frac{\partial I_d}{\partial V_d} = \frac{\mu_d C_g V_d}{L^2} \qquad (3.6)$$

If the g_m and the device dimensions are known, it is possible to derive an effective mobility from Equation 3.6. It is found that the mobilities derived in this way yield values considerably greater than those normally obtained for polycrystalline films, and in fact tend to approach the value for a single crystal. This is remarkable when one considers that no allowance has been made for electron trapping or for the decrease in the surface mobility as the surface channel narrows.

The carrier mobility in the surface channel is thought to alter in several ways in the presence of a transverse field. As impurity or trap states become occupied, their electrical charge changes and hence their scattering cross section changes. The mobility of free carriers decreases when an electrically neutral trapping site is filled. On the other hand, if the impurity site becomes electrically neutral when filled, then the free carrier mobility will decrease. In addition, the carrier mobility can vary because of changes in the height of the inter-crystalline potential barriers. Weimer has found devices in which both the drift and the Hall mobility are functions of the gate bias [2] and Miksic [27] has reported cases where the effective mobility is a function of both bias and frequency.

The mobility of carriers in a surface channel has been of interest for some time and Schrieffer [28] has calculated the mobility of electrons in surface space charge layers, and has found that the electron mobility in an n-type channel should decrease with increasing surface potential. In fact, experimental work on single crystals of germanium ~~have~~ has shown the surface mobility to decrease with surface potential as predicted. The variation of carrier mobility with gate voltage in a thin film transistor appears to be at variance with these results. A single crystal was used in the case of the germanium whereas a polycrystalline film was used to fabricate the transistor. By making use of this fact, Weimer [29] was able to explain the mobility variation as a function of surface potential by using the polycrystalline inhomogenous film model [30]. This model considers the film to be a matrix of high-and low-resistivity regions between which potential barriers exist. The theory accounts for the increase in the effective mobility by the suppression of intercrystalline potential barriers by the increased surface potential.

It is clear that the single field effect theory proposed by Borkan and Weimer is able to provide (as far as it goes - to the pinch-off point) an insight into the physical processes involved in the operation of the thin film transistor. Wright [31], among others, has taken the theory beyond this point and into the saturation region

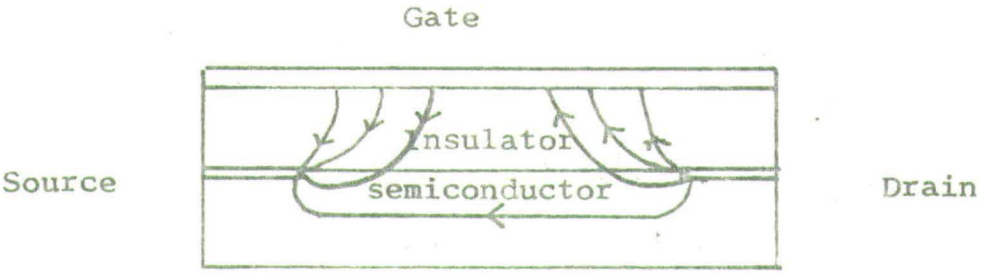
3.3 WRIGHT'S ANALYSIS OF THE SURFACE CHANNEL DIELECTRIC TRIODE.

In his analysis of his surface channel dielectric triode, which is more commonly known as the Insulated Gate Field Effect Transistor (IGFET), Wright

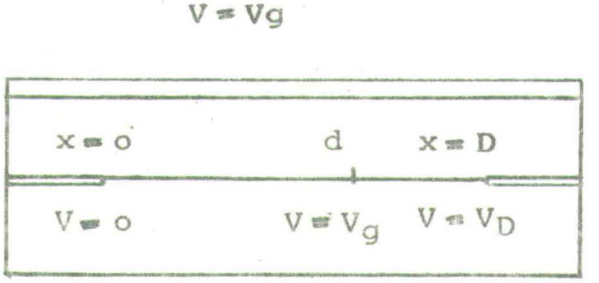
distinguished between a source region where the gradual approximation was valid and a drain region, in which a longitudinally directed electric field existed, and a space charge limited current flowed. Wright's approach and the operating mechanisms of the device can best be understood by referring to Figure 3.3.

Figure 3.3 is essentially the configuration of the coplanar thin film transistor. The source and drain electrodes are on the surface of the semiconducting layer and separated from the gate by an insulating layer. The electrostatic field pattern in the device is shown for $V_D > V_g$, in the absence of space charge. This portrays Wright's idea of a division into source and drain regions. The potential difference across the insulating layer at the source is $+V_g$ and at the drain $(V_g - V_D)$. Since $V_D > V_g$ there is some intermediate point between the source and drain at which the potential across the insulator is zero. Let this be at the point $x = d$. The region to the left of this point is influenced by the gate potential while that to the right is influenced by the drain potential. This point, then, marks the end of the source region and the beginning of the drain region.

When current flows in the semiconducting layer, lines of force from the gate electrode terminate in the space charge layer which exists between the source and drain. The forces existing in the space charge layer are due to electric fields and to electron concentration gradients. In the y-direction, the electric field E_y which acts across the insulator produces a drift force which moves electrons towards the interface between the insulator and semiconductor. The electron density increases at the interface until the drift force due to E_y is balanced by the diffusion forces originating from the concentration



(a)



(b)

Fig. 3.3 Wright's Co-planar T.F.T. structure. The electrostatic field configuration in the absence of space charge is shown in (a) for $V_D > V_g$

gradient of the electrons. In the x-direction the electric field E_x is produced in the source region by the potential difference V_g which exists along this region and in the drain region by the potential difference $(V_D - V_g)$ which exists along this region. The charge held in the space-charge layer varies from a maximum at the source to smaller values on proceeding towards the drain. However, the current is a constant at all points between these electrodes and so the field E_x must increase on proceeding towards the drain.

The model used by Wright in his analysis is shown in Figure 3.4 and contains simplifying assumptions. The space-charge layer is assumed to have a uniform charge density in the y-direction and also to be of uniform thickness throughout. The essential features of the device do not appear to be changed by making these simplifications. In terms of this model, Wright divided the space-charge in the conducting channel into two components; one in which the lines of force emanating from the gate electrode terminate and the other in which the lines of force from the drain electrode terminate.

Let N be the charge density for the former and n be the charge density which produces divergence of the field E_x in the drain region. At a distance x from the source the potential in the space charge region is V. Then the charge held in this layer by the electrostatic action of the gate is

$$qNh = \varepsilon_0 \varepsilon_1 E_y = \varepsilon_0 \varepsilon_1 (V_g - V)/t \qquad (3.6a)$$

where 't' is the thickness of the insulator and 'h' is the thickness of the space-charge layer.

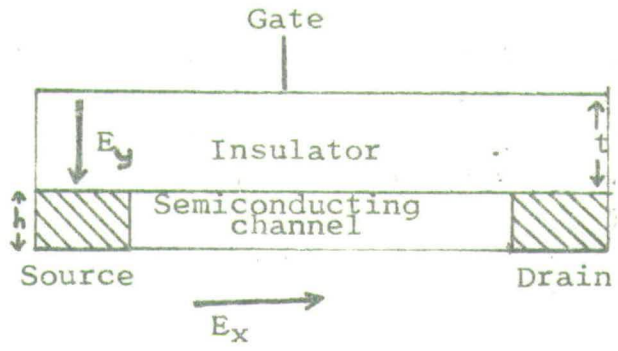


Fig. 3.4 Model used for analysis by Wright.

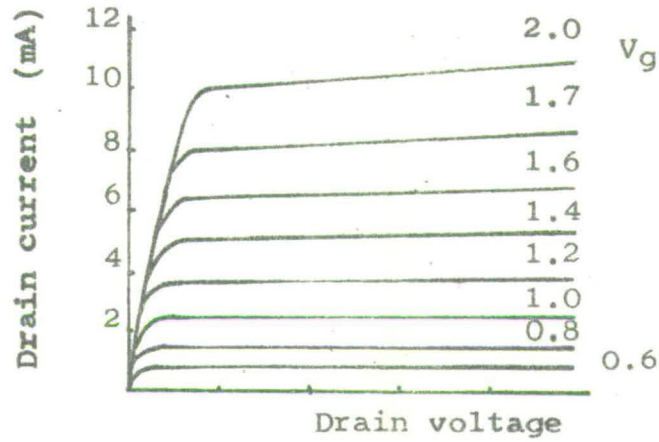


Fig. 3.5 Drain characteristics calculated by Wright

The divergence of the field E_x is given by

$$\frac{dE_x}{dx} = -\frac{qn}{\epsilon_2 \epsilon_o} \tag{3.7}$$

ϵ_1 and ϵ_2 are the dielectric constants of the insulating and semiconducting layers respectively.

The current is carried by the total space-charge and is given by

$$J = q\mu(N + n)E_x \tag{3.8}$$

μ is the mobility of the electrons in the semiconductor.

From the Equation 3.6a

$$N = \epsilon_o \epsilon_1 (V_g - V)/qht \tag{3.9}$$

and from Equation 3.7

$$n = -\frac{\epsilon_o \epsilon_2}{q}\frac{dE_x}{dx} = \frac{\epsilon_o \epsilon_2}{q}\frac{d^2V}{dx^2} \tag{3.10}$$

substitution of Equation 3.9 and Equation 3.10 into Equation 3.8 gives

$$-J = \epsilon_o \mu \left[\frac{\epsilon_1}{ht}(V_g - V) + \epsilon_2 \frac{d^2V}{dx^2}\right]\frac{dV}{dx} \tag{3.11}$$

This is the basic equation describing the operation of the device. It can be integrated to yield an expression which describes the longitudinal field in the channel. Thus,

$$\left(\frac{dV}{dx}\right)^2 - \left(\frac{dV}{dx}\right)^2_{x=0} = -\frac{2Jx}{\epsilon_o \epsilon_2 \mu} - \frac{\epsilon_1 V}{\epsilon_2 ht}(2V_g - V) \tag{3.12}$$

It is not possible to carry out any further integration of this equation. However, Wright was able to obtain a description of transistor operation from it by applying it in turn to the source and drain regions of the conducting channel, and neglecting the appropriate terms.

Firstly, consider the source region of the transistor. In this region E_x is of the order $\frac{V_g}{d}$ and E_y is of the order $\frac{V_g}{h}$. The insulating layer is much thinner than the source to drain spacing. Thus $E_x << E_y$ and the terms on the left hand side of Equation 3.12 can be neglected as each is smaller than either term on the right hand side.

Therefore, Equation 3.12 can be written as:

$$\frac{2ix}{\varepsilon_o \varepsilon_i \mu w} = \frac{V}{t}(2V_g - V) \qquad (3.13)$$

Where $i = -Jwh$, 'w' is the width of the channel and 'i' is the actual current between source and drain. This equation is valid in the source region where the condition $E_y >> E_x$ is satisfied. At the end of the source region E_y decreases to zero, near $x = d$, and E_x becomes greater than E_y. If E_x is assumed to be constant in the source region, then

$$\frac{(E_y)_{x=0}}{E_x} = \frac{d}{d - d'}$$

where d' is the point at which $E_y = E_x$. Then

$$(d - d') = \frac{E_x}{(E_y)_{x=0}} d \qquad (3.14)$$

is the very short distance over which $E_y < E_x$. Equation 3.14 is valid up to $x = d^1$, where $(d - d^1) << d$. In Equation 3.14 itself, the difference between d and d^1 may be neglected and the current given by

$$i = \frac{\varepsilon_o \varepsilon_1 \mu w V_g^2}{2td} \qquad (3.15)$$

Wright described the conditions within the source region further by deriving expressions for the potential electric field and the charge density. The potential can be obtained using Equation 3.15 and Equation 3.13.

Hence,

$$V = V_g[1 - [1 - \frac{x}{d})^{\frac{1}{2}}] \qquad (3.16)$$

The variation of E_x follows directly from Equation 3.16 by differentiating with respect to x, giving

$$E_x = - \frac{V_g}{2d}(1 - \frac{x}{d})^{-\frac{1}{2}} \qquad (3.17)$$

Expressions for the charge densities, N and n, can be obtained from Equation 3.6a and Equation 3.7 respectively. Thus,

$$N = \frac{\varepsilon_o \varepsilon_1}{qht} V_g (1 - \frac{x}{d})^{\frac{1}{2}} \qquad (3.18)$$

and

$$n = \frac{\epsilon_0 \epsilon_2 V_g}{4qd^2}\left(1 - \frac{x}{d}\right)^{-3/2} \qquad (3.19)$$

The drain region, where $x \geq d$, can be treated in a similar manner by making appropriate approximations in Equation 3.12. For $d \leq x \leq D$, where D is the source to drain spacing, N = 0, and the last term on the right hand side of the equation can be neglected. In this way Wright obtained the expression

$$E_x^2 - E_d^2 = -\frac{2J}{\epsilon_2 \mu}(x - d) \qquad (3.20)$$

where E_d is the electric field at the point x = d in the conducting channel. E_d cannot be given an exact value because the description of the source region is not valid right up to the pinch-off point. Consequently, it is difficult to link the solutions in the source and drain regions. Wright has accepted the drain region as one of high field in the x-direction and, by neglecting E_d in Equation 3.20, obtained

$$E_x = \sqrt{\frac{\epsilon_1}{\epsilon_2}}\left(\frac{x - d}{h + d}\right)^{\frac{1}{2}} V_g \qquad (3.21)$$

Equation 3.21 can be used to obtain expressions for the electric potential and charge density. Thus,

$$V - V_g = \left(\frac{\epsilon_1}{\epsilon}\right)^{\frac{1}{2}} \frac{2htd}{3}\left(\frac{x - d}{h + d}\right)^{3/2} V_g \qquad (3.22)$$

and

$$n = \frac{\varepsilon_0 \epsilon_2 V_g}{2qhtd}\left(\frac{\epsilon_1}{\epsilon}\right)^{\frac{1}{2}}\left(\frac{x - d}{htd}\right)^{-\frac{1}{2}} \qquad (3.23)$$

By assigning values which suitably describe a cadmium sulphide TFT to the various parameters ~~- see subscript to Figure 3.5 -~~ and using the relevant expressions which characterise the source and drain regions, Wright deduced the current voltage characteristic for the transistor. Thus if the drain voltage does not exceed the gate voltage, then the source region extends over the complete distance between source and drain, and in this case

$$i = \frac{\varepsilon_0 \epsilon_1 \mu W}{2tD}(2V_g - V_D)V_D \qquad (3.24)$$

On the other hand, if the drain exceeds the gate voltage

$$i = \frac{\varepsilon_0 \epsilon_1 \mu W V_g^{\,2}}{2td} \qquad (3.25)$$

Equation 3.25 is valid in the source region up to the point $x = d$ where $V = V_g$. By substituting for V_D and V_g in Equation 3.22, Wright obtained a value for d, and hence from Equation 3.25 the current for a given value of V_g and V_D. In this way, Wright obtained the characteristic shown in Figure 3.5.

Winslow [32] used the same approach as Wright and likewise obtained the basic

equation

$$J = \varepsilon_d \mu \frac{dV}{dx}\left[\frac{\epsilon_1}{ht}(V_g - V) + \epsilon_2 \frac{d^2V}{dx^2}\right]$$

No attempt was made to solve this equation analytically but a numerical solution was obtained. The dimensionless variables $\phi = V/V_D$ and $\theta = \frac{X}{D}$ were introduced to give the dimensionless equation

$$\phi'[\phi'' + K_1(\phi_g - \phi)] = K_2 \qquad (3.26)$$

where

$$\phi_g = \frac{V_g}{V_D}$$

$$K_1 = \frac{D^2 \epsilon_1}{\epsilon_2 ht}$$

$$K_2 = \frac{JD^3}{\epsilon_0 \epsilon_2 \mu V_D^2}$$

The boundary conditions which must be satisfied are

(1) $\phi = 0$ at $\theta = 0$

(2) $\phi' = 0$ at $\theta = 0$

(3) $\phi = 1$ at $\theta = 1$

Condition (2) expresses the ohmic quality of the source electrode. Equation 3.26 is a second order differential equation on which three boundary conditions are impressed. Winslow solved the equation by assigning a value to K_1 and

determined K_2 for several values of ϕ_g . The drain characteristics obtained in this way agreed well with Weimer's experimental characteristics.

3.4 THE CURRENT SATURATION PROBLEM AND GEURST'S ANALYSIS.

In all types of field effect transistor the transport mechanism in the saturation range is not well understood, and in actual devices, complete current saturation does not occur. In Shockley's theory the channel resistance appears to reach a finite value, at the pinch-off point, and any further increase in drain voltage falls across the pinch-off region. A rough estimate of the length of the high resistance pinch-off region as a function of the drain voltage was made and, consequently, an idea of the channel length was obtained. A slow variation in the channel length with drain voltage occurs and therefore, the I-V characteristics of the transistor show a very small slope beyond pinch-off. In this way the high but finite output resistance was accounted for.

Several other arguments have been put forward to explain the current saturation phenomena. Grosvalet et.al. [33] proposed that the saturation current, again in the junction gate type of field effect transistor, was due to the limiting drift velocity at high fields. However, this model is useful only for short channels, the width of which is equal to or is the same order of magnitude as the length. It fails to account for the current saturation effect in long thin channels. The field dependent mobility model was applied to the insulated gate transistor by Root and Vodasz [34] but the I-V characteristic varied from the observed. Hofstein and Heinman [35] have related the saturation resistance to the capacitance from the drain to the source region of the channel through

the substrate to channel depletion region. Hence, the output resistance becomes dependent on the induced charge in the channel from the substrate side of the device. Johnson [36] approached the problem in an entirely different way. He has shown that a uniform distribution of donors in the semiconductor, which is only partly ionized, can lead to devices which fail to saturate. The saturation region corresponds to the ionization of donors at deeper lying levels. Complete saturation would only occur when all the donors were ionized. This would require large drain voltages, and, in practice, breakdown of the device would occur before complete saturation was attained.

Apart from the work of Johnson, which was applied to the thin film transistor, attention has been focussed mainly on the saturation phenomena in MOS transistors. There are several features of this transistor which have no counterpart in the thin film transistor; for example, the substrate underlying the channel and separated from it by a depletion layer is a conductor, or at least a semiconductor and the p-n depletion layer at the drain changes in thickness with drain voltage and interacts with the channel. A discussion of current saturation in an MOS transistor involves the inclusion of features which are not present in a thin film transistor, and so a direct comparision is not possible.

Geurst [37], while realizing that current saturation may depend on the physical properties of the device, such as field dependent mobility and partially ionized donors in the semiconductor, has suggested that the geometrical configuration of the electrodes may also be of importance. Geurst has formulated a sophisticated mathematical theory for a double gate field device and he has shown that current saturation in this device is dependent on the ratio of insulator thickness to source and drain separation.

The model used by Geurst is shown in Figure 3.6. It differs from an actual device in that a symmetrical twin gate structure is employed. Several assumptions were made for mathematical simplicity. The thickness of the channel in the model is assumed to be infinitely small. In actual devices the semiconducting channel between the source and drain is likely to be much thinner than the insulating layer. The same assumption is made with respect to the source and drain electrodes which can be looked upon as knife-like contacts. All electrodes extend to infinity.

The current per unit width of the transistor, I, traversing the channel from the source to drain is given by

$$I = \sigma v \tag{3.27}$$

where σ denotes the charge per unit surface area and v represents the drift velocity of the carriers.

Let N_o be the number of charge carriers originally present in the semiconducting layer, and q the electronic charge. Then, if D_y^+ and D_y^- represent the y-components of the displacement vector $\underline{D}$ at the upper and lower sides of the channel respectively,

$$\sigma + \frac{N_o q}{L} = D_y^+ - D_y^- \tag{3.28}$$

Using the symmetry of the configuration and expressing N_o in terms of voltage V_o gives,

$$\frac{2\ \epsilon_o \epsilon_r}{h} V_o = -\frac{qN_o}{L}$$

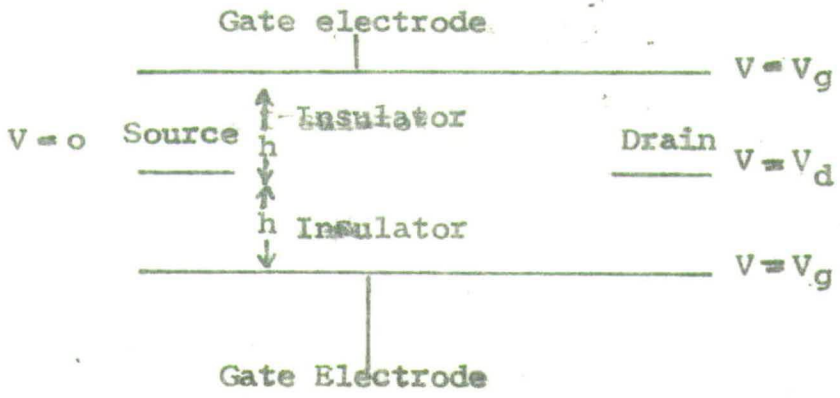


Fig. 3.6 Two gate structure used by Geurst in his analysis.

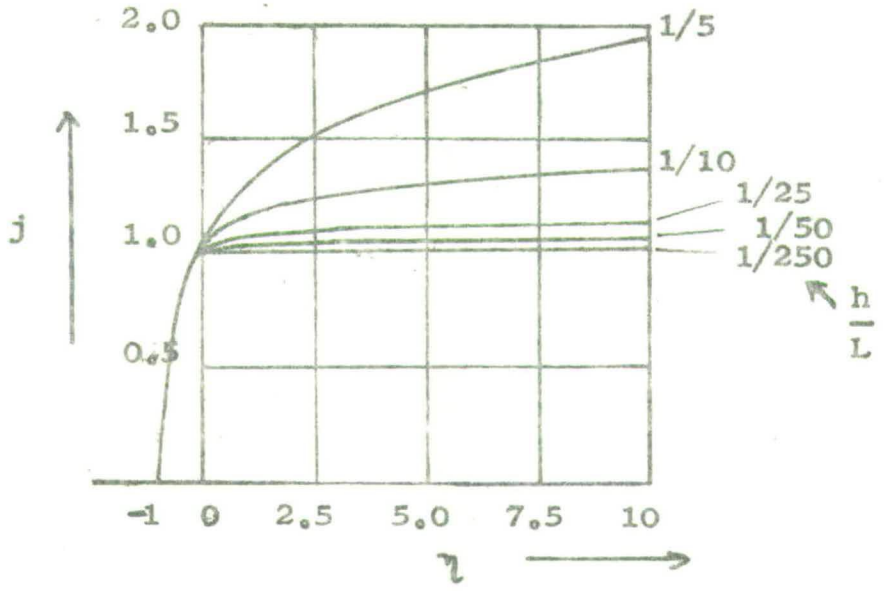


Fig. 3.7 The dimensionless drain current j plotted as a function of the dimensionless drain voltage

Equation 3.28 becomes

$$\sigma = 2\,\epsilon_o\epsilon_f\left(E^+_y + \frac{V_o}{h}\right) \tag{3.29}$$

Substituting

$$v = \mu E_x \tag{3.30}$$

into Equation 3.27 yields

$$I = 2\,\mu\epsilon_o\epsilon_f\left(E_y^+ + \frac{V_o}{h}\right)E_x \tag{3.31}$$

Since the longitudinal component of E_x is continuous across the channel, Equation 3.31 may be written as

$$I = 2\,\mu\epsilon_o\epsilon_f\left\{\left(E_y^+ + \frac{V_o}{h}\right)E_x\right\}^+ \tag{3.32}$$

where the plus superscript denotes the limiting value at the upper side of the x-axis.

When the electric field between the gate electrodes and the semiconducting channel is perpendicular to the channel, Equation 3.32 may be written in the following way:

$$I = -2\mu\,\frac{\epsilon_o\epsilon_f}{h}(V_g - V_{(x)} - V_o)\frac{dV}{dx}$$

Here again V_g denotes the gate potential and $V_{(x)}$ is the potential at a point x

in the channel. Apart from the factor 2 which results from the presence of two gate electrodes, this equation is the same as that obtained by means of the gradual approximation analysis, and describes what has come to be known as the source region.

The situation in the drain region of the channel, where space charge limited current occurs, is also described by Equation 3.32. Consider the general formula for space-charge-limited-currents,

$$J = \mu(\text{div}\underline{D})E_x \qquad (3.33)$$

where E_x is the component of the electric field parallel to the direction of motion of the charge carriers. For infinitely thin semiconducting layers, Equation 3.33 reduces to

$$J = 2\,\mu\underline{D}_n E_x$$

or

$$J = 2\,\mu\epsilon_0\epsilon_r E_y E_x \qquad (3.34)$$

which is the same as Equation 3.32 if $V_o = 0$.

The one-dimensional case of Equation 3.33 was used by Wright in his theory of the thin film transistor to describe the drain region. It is given by

$$J = \mu\epsilon_0\epsilon_r \frac{dE_x}{dx} E_x$$

$$= \mu\epsilon_0\epsilon_r \frac{d^2V}{dx^2}\frac{dV}{dx} \qquad (3.35)$$

Geurst's expression for the current obviously has a greater generality than the expressions derived and employed by either Borkan and Weimer or Wright. Geurst used Equation 3.32 as a nonlinear boundary condition for the electric field in the insulator region, bounded by the upper gate electrode, the source and drain electrodes and the semiconducting channel. For given electrode voltages the current, I, is a constant at any point along the channel. The boundary conditions at the metal electrodes are given simply by

$$E_x = 0$$

The electric field has to satisfy there boundary conditions in the specified region. Geurst was able to solve this nonlinear boundary value problem by obtaining a transcendental equation involving I as a function of V_g, the gate voltage, and V_d, the drain voltage. The geometric ratio $\frac{h}{L}$ occurs in the transcendental equation, written below, as an independent parameter.

$$\log\left\{\left(1 - \frac{\lambda_1}{\lambda_2}\right)^{-1} \frac{\pi L}{h}\left[1 - \frac{1 - \eta^2}{j}\right]\right\} + 1 -$$

$$\left(1 - \frac{\lambda_1}{\lambda_2}\right)^{-1} \frac{\pi L}{h}\left[1 - \frac{1 - \eta^2}{j}\right] + \frac{\pi L}{h}\,\eta^2\,\frac{1}{j} = 0 \qquad (3.36)$$

where $\lambda_1 = e^{\frac{\pi L}{2h}}$ and $\lambda_2 = e^{\frac{\pi L}{2h}}$. j and η are dimensionless quantities defined by

$$j = \frac{I}{\frac{\mu \epsilon_o \epsilon_r}{hL}(V_g - V_o)^2}$$

and $$\eta = \frac{V_d}{V_g - V_o} - 1$$

This equation was solved numerically for various values of the ratio $\frac{h}{L}$ and the results obtained are shown in Figure 3.7. From the results, it can be seen that the degree of saturation of the device is dependent on the ratio $\frac{h}{L}$, small values of this ratio producing better drain current saturation. Up to drain voltages near pinch-off, the characteristics show the parabolic shape predicted by the gradual approximation approach.

Geurst also investigated the solution of Equation 3.36 by means of asymptotic methods. In this way he obtained analytical expressions for j valid over certain ranges of η and for large values of $\frac{\pi L}{h}$. For $-1 < \eta < 0$ below pinch-off, Geurst obtained

$$j = (1 - \eta^2)\{1 + \frac{h}{\pi L} \exp(- 1 - \frac{h}{\pi L} \frac{\eta^2}{1 - \eta^2}) + ---\}$$

in which higher order terms are omitted. It follows that

$$j \to (1 - \eta^2) \quad \text{as} \quad \frac{\pi L}{h} \to \infty$$

Substituting for j and η gives

$$- \frac{I}{\frac{\mu \epsilon_0 \epsilon_r}{hL}(V_g - V_o)^2} = 1 + \frac{V_d^2}{(V_g - V_o)^2} - \frac{2V_d}{(V_g - V_o)} - 1$$

$$\therefore \quad I = \frac{\mu \epsilon_0 \epsilon_r}{hL}(2V_d(V_g - V_o) - V_d^2)$$

which is the expression obtained by means of the gradual approximation.

For $\eta > 0$, drain voltages above pinch-off, the asymptotic solution is

$$j = 1 + \frac{h}{\pi L}\log\left(\frac{h}{\pi L}\right) + \frac{h}{\pi L}(1 + \log \eta^2) + \text{---}$$

Thus $$j \to 1 \text{ as } \frac{\pi L}{h} \to \infty$$

Therefore, in the saturation region

$$I = -\frac{\mu\epsilon_0\epsilon_r}{hL}(V_g - V_o)^2$$

It must be kept in mind that the above expressions for drain current were developed for a two gate structure and do not apply directly to actual devices. However, ~~it does~~ they do have some relevance. Geurst suggested that an insight into the operation of a single gate device, particularily with regard to its saturation properties, could be obtained by considering the total current in it to be due to half the current in a symmetrical transistor with gates, added to half the current in a similar transistor without gates.

For the structure with no gates, the current may be obtained by letting $\frac{\pi L}{h}$ tend to zero. In this way, Geurst showed that the current is

$$I = -\frac{2\ \mu\epsilon_0\epsilon_r}{\pi}\frac{V_d^2}{L^2} \qquad (3.37)$$

Half of this current would flow in a conventional device and the output ~~impedance~~ admittance would be

$$\frac{dI}{dV_d} = -\frac{2\ \mu\epsilon_0\epsilon_r}{\pi L^2}V_d$$

The current contribution from the symmetrical transistor with gates is

$$I = -\frac{\mu\epsilon_0\epsilon_r}{2hL} V_g^2 j$$

and the output ~~impedance~~ admittance is

$$\frac{dI}{dV_d} = -\frac{\mu\epsilon_0\epsilon_r}{\pi L^2} \frac{V_g}{\left(\frac{V_d}{V_g} - 1\right)}$$

These contributions are of the same order of magnitude and suggest that in a single gate structure, although as pointed out earlier there may be other reasons for non saturation of current, the ratio of insulator thickness to channel length should not be ignored. In this way, Geurst's novel approach has directed attention to an aspect of thin film transistor operation which had not previously been seriously considered.

CHAPTER 4.

THE EVAPORATION OF CADMIUM SULPHIDE FILMS.

The properties of the III-V compounds resemble those of the group IV elements because their atomic bonding and structures are similar. The widths of the forbidden energy gaps in III-V compounds are greater than those of the group IV elements and this is attributed to the partial ionic character of the bonding. This trend continues in the II-VI compounds. Here, the average valency per atom is also 4, so that covalency is likely, but the increased electronegativity of the group VI elements introduces considerable ionicity. As a result II-VI compounds, such as cadmium sulphide, can be considered as semiconductors but more nearly resemble insulators. This trend reaches a maximum in th I-VII compounds, the alkali halides, which are normally insulators having forbidden-energy gaps greater than 5eV. Substances in which the bonding is predominantly covalent generally form crystals with either the zincblende structure or with one of the related structures, while those with predominantly ionic bonding form crystals with one of the cubic structures, rather like the alkali halides.

Cadmium sulphide is dimorphoric and has cubic and hexagonal forms. However, it normally crystallizes with the hexagonal modification of zinc sulphide, wurtzite. The forbidden energy gap of cadmium sulphide is 2.45eV and pure or compensated crystals are essentially insulators having resistivities in the dark of about 10^{12} ohm.cm. The dielectric constant is 11.6 and the electron mobility is 210 cm^2/volt.sec.[38] Because of its importance as a photoconductor the trap distribution [39, 40] has been examined in some detail.

4.1 PROPERTIES OF CADMIUM SULPHIDE FILMS.

Cadmium sulphide thin films have been investigated by many workers [41, 42], primarily with respect to their photoconductive properties and different methods [41, 42] of preparation have been used. More recently the evaporation method has become the most popular, mainly due to the advent of the thin film transistor [43, 44] and to the search for an acousto-electric transducer. [45, 46, 47] Unfortunately, by virtue of the dissociation of the compound on heating, the properties of the cadmium sulphide films are extremely sensitive to the evaporation conditions. Goldfinger and Jeunehomme [48] have investigated the vapour species using mass spectrometer techniques and found no evidence for the existance of cadmium sulphide molecules in the vapour. Only separate molecules of cadmium and sulphur were found. Thus the sensitivity to the evaporation conditions can in part be understood by considering the vapour pressures of the elements. Table 4.1 shows the vapour pressures for cadmium and sulphur, and also the other group IV elements, selenium and tellurium. For a given temperature, cadmium has a much lower vapour pressure than sulphur and so condenses more rapidly on the substrate, forming a cadmium rich film.

	10^{-5}	10^{-4}	10^{-3}	10^{-2}	10^{-1}
S	37	55	90	109	147
Te	242	280	323	374	433
Se	133	164	199	243	297
Cd	146	177	217	265	320

Table 4.1. Vapour pressure in torr (top row) against temperature (^{o}C).

Consider the effect of having an excess of one of the constituents, i.e. cadmium, in a crystal. The excess cadmium atoms are thought to occupy mould lattice sites. The vacant anion (sulphur) sites have an effective positive charge with respect to a perfect crystal and will, therefore, attract electrons. The binding energy of the electrons trapped in the anion vacancy is so small that at room temperature electrons are released into the conduction band, producing an n-type material. In cadmium sulphide excess sulphur does not give free holes. This means that the vacant cation site is too far from the valence band to be ionized at room temperature.

Various processing measures can be undertaken to reduce this evident deviation from stoichiometry. The diffusion of acceptor impurities into the films has also been used.[49]. It has also been shown by Gilles and Van Cakenberghe [50] that thin films of cadmium sulphide can be recrystallized by use of an activator such as silver, copper, lead or indium. De Klerk and Kelly[46] abandoned the use of cadmium sulphide powder alone as a source material and overcame the lack of stoichiometry by evaporating simultaneously either cadmium sulphide and sulphur, to fill the sulphur vacancies, or cadmium and sulphur from separately controlled sources. Both methods were found to be succesful although the latter combination yielded more reproducible results. These methods have come to be referred to as "co-evaporation". However, no matter which technique is used, the properties of the cadmium sulphide films are still sensitive to the evaporation conditions and the evaporation rate, the source temperature and the substrate temperature are among parameters which it is necessary to control. In this work, all films were formed by evaporation of the compound alone.

The effect of the substrate temperature is very marked and governs many properties of the deposited layer. This is illustrated by the fact that considerable colour and resistivity variations can be obtained when cadmium sulphide is evaporated on substrates at different temperatures. Cadmium sulphide appears dark in colour when evaporated on a cold substrate, whereas yellow films are obtained when the substrate is maintained at a temperature above 150°C. The corresponding resistivities for these films are 10^{-1} to 10^{6} ohm-cm approximately.[44] A significant increase in crystallite size is also noted with increasing temperature. This was clearly shown by Berger et.al. [51] by using carbon replica techniques in electron microscopy studies of thin films of cadmium sulphide, and also cadmium selenide. Shallcross[52] obtained similar results in a study of cadmium selenide. His films were amorphous on room temperature substrates but consisted of crystals up to 2 microns in size when deposited at 350°C.

Hall efect measurements on films have been made by several workers [17, 53] and have shown the electron mobility to be of the order of 1 cm^2/volt.sec. Recrystallization increases the mobility by an order of magnitude but it is remains much smaller than the bulk crystal value. The mobility and carrier density have been found to increase with temperature, showing an approximately exponential ~~experimental~~ dependence on $\frac{1}{T}$. This increase in mobility can be explained in terms of barriers arising from inhomogenities within the films, using the model proposed by Petritz [30], and suggests that the low mobility is largely due to defects, e.g. point defects, dislocations, internal surfaces within the films.

The deposition of cadmium sulphide has generally been on non-orientated

substrates, viz. glass, although more recently studies of epitaxial growth have been initiated. Aggarwal and Goswani [54] have deposited cadmium sulphide epitaxially on rock salt and the author has reported on epitaxial formation on mica [55].

4.2 TECHNIQUES FOR INVESTIGATION OF CRYSTAL STRUCTURE.

Conventional methods can be employed for observing the extent and nature of crystal growth in thin films, e.g. X-ray examination, electron diffraction, electron microscopy, and scanning electron microscopy. [44, 51] Reflection electron diffraction is particularly suitable for examining the near surface structure. In many cases optical examination alone shows no evidence of crystal structure and in isotropic crystals only structures such as cleavage planes and crystal boundaries can be observed. In particular, cubic compounds are not amenable to optical observations of their recrystallization. In hexagonal compounds, such as cadmium sulphide, crystalline areas, if they are sufficiently large in area, can be distinguished from the amorphous regions under polarized transmitted light, except the (0001) plane where such crystals are isotropic. The evaluation of etch pits has also been employed in the study of crystal structures and phosphoric acid has been used to etch cadmium sulphide. No serious attempt was made to use this technique.

4.3 SUBSTRATE CLEANING PROCEDURE.

It has been pointed out that the substrate can have a profound effect on the

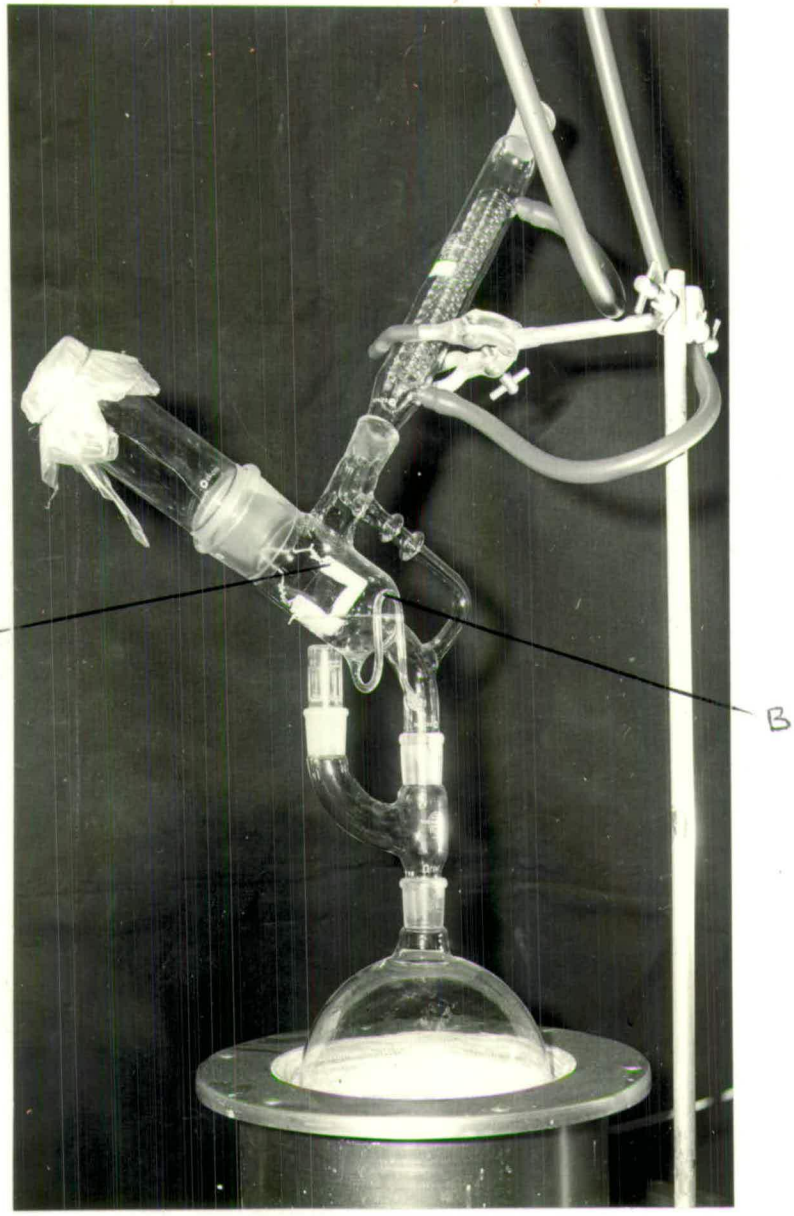


Fig. 4.1 Substrate cleaning and drying apparatus, using iso-propyl alcohol vapour.

nucleation and growth of an evaporated film. Quite apart from the influence of the crystalline structure of the substrate, the presence of dirt on the surface leads to the formation of an uneven and irregular film usually with poor adherence to the substrate. In such circumstances it would be difficult, if not impossible, to obtain reproducible results and a clean substrate is a prerequisite in any evaporation work.

There are many different cleaning procedures suggested in the literature [46] on thin films, but basically the same process is involved in all. This takes the form of cleaning with a strong detergent, sometimes in an ultrasonic bath, followed by washing in a pure low boiling point solvent, usually an alcohol, to ensure that no precipitate remains on drying.

Apart from the actual cleaning process, some difficulty was initially experienced in drying the substrate after cleaning. The final washing in the solvent, isopropyl alcohol, invariably resulted in a drying stain - most likely owing to impurities - appearing on the substrate. To overcome this, the substrate was dried in isopropyl alcohol vapour. For this purpose, the apparatus shown in Figure 4.1, the design of which was due to C. Challacombe of R.R.E. Malvern, was constructed. The operation of the system depends on the syphoning action which takes place in the chamber marked A. Vapour from the boiling isopropyl alcohol is condensed and allowed to run into Chamber 'A' in which the substrate is suspended. When the liquid reaches level 'B' the syphon operates and Chamber 'A' empties. A cycling action is set up and vapour is continually swept into the chamber. In this way, it is possible to obtain a dry, stain-free substrate.

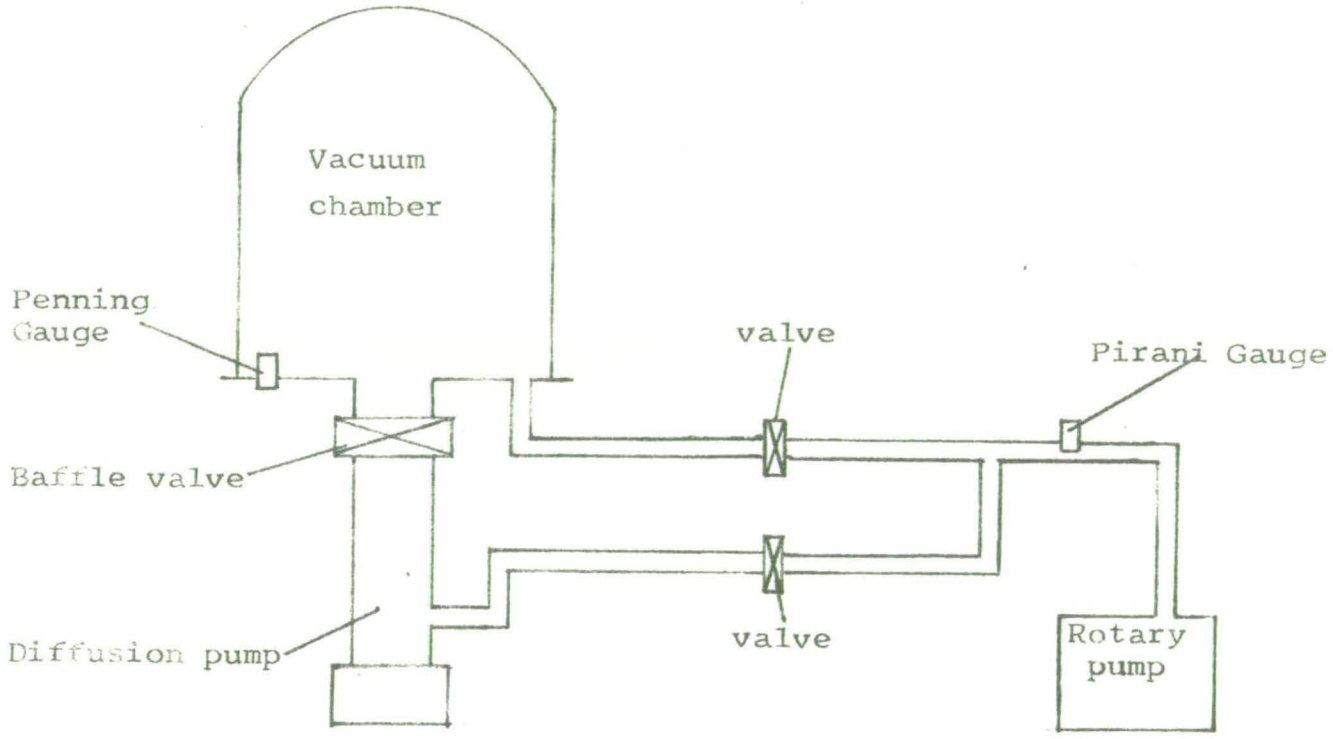


Fig. 4.2 Diagram of vacuum chamber and pumping system

Prior to washing in the alcohol the substrate was cleaned, usually by rubbing with cotton wool, in the detergent. It was then placed in a solution of warm concentrated sulphuric acid and chromium trioxide, rinsed in water and washed in isopropyl alcohol.

4.4 THE VACUUM SYSTEM.

A standard Edward's High Vacuum 19E vacuum system was used for all evaporation work. The pumping unit consisted of a conventional oil diffusion pump backed by a rotary pump, Figure 4.2. The evaporation chamber was of steel and 19 ins in diameter. A liquid nitrogen cold trap in the form of a coil of copper tubing was situated beneath the chamber, immediately above the baffle valve. Pressures between 10^{-5} and 10^{-6} torr could readily be obtained using the cold trap. Penning and Pirani gauges were used to measure pressure. All materials were evaporated upwards by resistance heating from a rotary filament holder which contained six evaporation points. It was thus possible to evaporate a number of different materials without exposing the system to atmospheric pressure. The chamber also contained a radiant heater to enable the walls to be outgassed.

4.5 VAPOUR DEPOSITION OF CADMIUM SULPHIDE.

Two evaporation methods were examined and these are described. Both methods contain the same underlying idea and were attempts to contain the cadmium sulphide evaporant within a small volume in order to facilitate control of

the evaporation parmeters. It was hoped to increase the vapour pressure of the evaporant to the exclusion of impurities present in the vacuum system, and so obtain more stoichiometric and more reproducible films. The cadmium sulphide powder was obtained from Kochlights Laboratories, Buckinghamshire. It was of 5N purity, and a spectrographic analysis obtained from the suppliers is listed below:

Calcium	1 ppm
Zinc	2 ppm
Copper	1 ppm
Iron	2 ppm
Magnesium	1 ppm
Lead	1 ppm
Silicon	1 ppm

4.5.1 METHOD 1: KNUDSEN SOURCE.

This method follows directly from that employed by Zuleeg[56]. The source used is sometimes referred to as the Knudsen source, the principle of the vapour deposition being based on the application of Knudsen's Law of gas flow in a tube where the mean free path of the particles is much larger than the transverse dimensions of the tube. If the diameter of the tube is D, then the velocity of flow, v, is given by

$$v = \frac{D}{3(\rho P)^{\frac{1}{2}}} \frac{dP}{dl}$$

where ρ is the gas density, P is the gas pressure and l the length of the tube. At a given pressure and pressure gradient the volume of the vapour passing through a specific cross-section is proportional to $\rho^{-\frac{1}{2}}$ Since ρ is a function of the source temperature, T, it can be varied over a wide range. Assuming that D, P and $\frac{dP}{dl}$ for a given system are constant, then the deposition rate is constant for a fixed source temperature. The thickness of the deposit is then a linear function of time.

A quartz tube, shown in Figure 4.3, of 0.75 ins diameter and 3 ins in length and closed at one end was uniformly heated from the outside by a coil of resistance tape. The cadmium sulphide was placed in a small quartz boat which was positioned on the indentation at the closed end of the tube. A thermocouple was used to monitor the temperature of the cadmium sulphide as shown in the diagram. Borosilicate glass and mica (muscovite) substrates were used and positioned about one diameter length from the mouth of the tube. The substrate temperatures were varied from 100°C to 250°C and for this purpose a simple heater, consisting of a soldering iron element sandwiched between two pieces of alumiunium, was constructed. The substrates were attached to the heater by a spring clip and the temperature was monitored by a thermocouple embedded in the aluminium.

Figure 4.4 shows a typical film obtained by this method. The annular formation indicates that the film does not have a uniform thickness and certainly decreases in thickness towards the edges. Zuleeg [56] also found this to be the case but was able, presumably with critical positioning of substrates and accurate source and substrate temperature control, to obtain films of more uniform

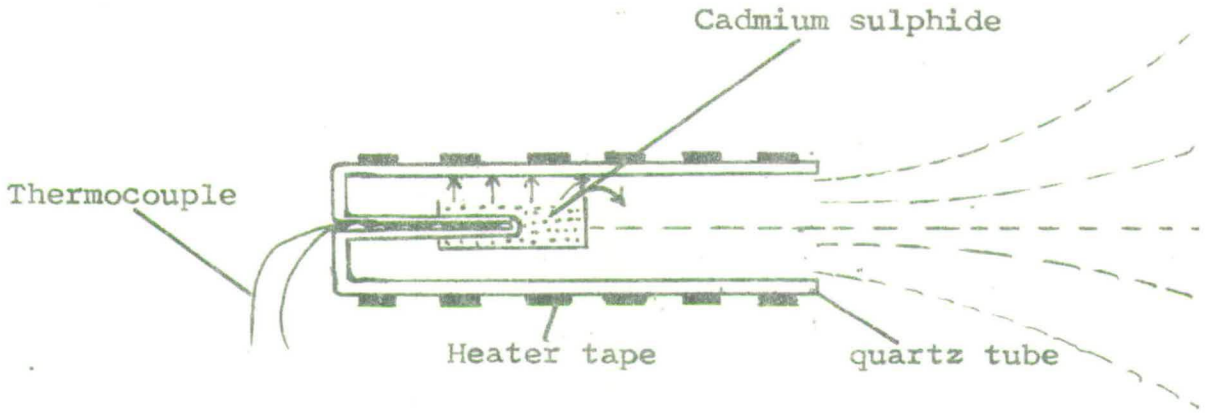


Fig. 4.3 The Knudsen source for Method 1.

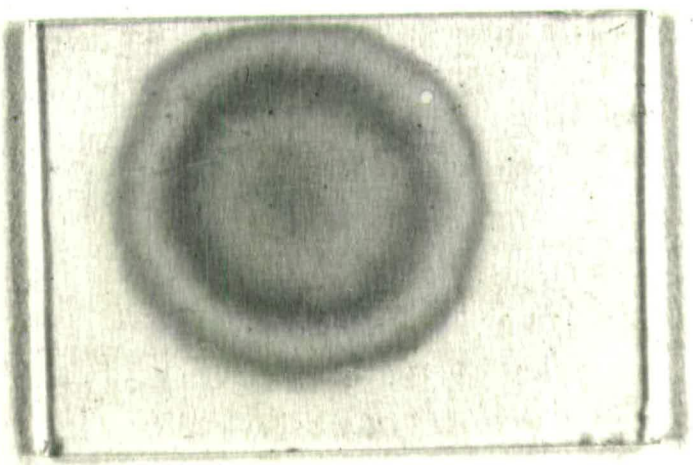


Fig. 4.4 Annular formation of Cadmium Sulphide film on glass.

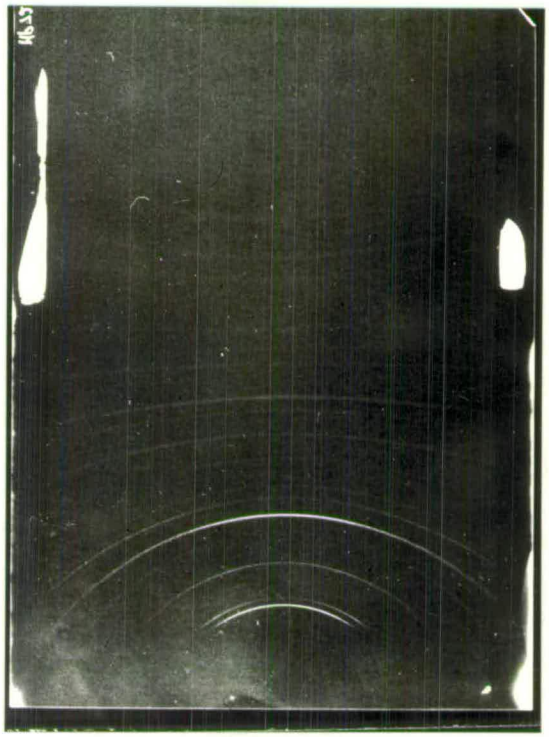


Fig. 4.5 X-ray reflection diffraction photograph of CdS on glass (Knudsen source).

Fig. 4.6 X-ray reflection diffraction photograph of CdS on mica (Knudsen source).

thickness. Generally, films which were deposited slowly and at the higher substrate temperatures were more yellow in colour, and therefore more stoichiometric.

X-ray diffractometer studies of films deposited on glass show predominantly the (002) and higher order diffraction peaks. Reflections from the (101) and (103) planes appear at a much lower intensity. Reflection diffraction photographs show a series of Debye-Scherer rings, Figure 4.6. Thus, the films consist of small crystallites, less than one micron in size, mainly orientated with their c-axes normal to the substrate. Post evaporation treatment in the form of heating to 500°C for 30 minutes in an inert atmosphere of helium, produced films which were more yellow in colour but not significantly different in structure.

Films deposited on mica, Figure 4.7, show a more ordered structure. The Debye-Scherer rings are not complete and this suggests that the crystallites are larger. All films were evaporated under the same conditions and the change in structure merely reflects the influence of the substrate.

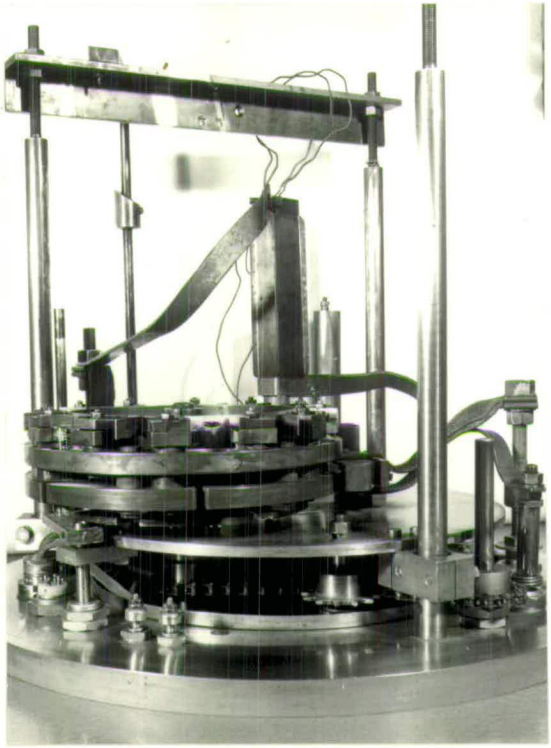
While the stoichiometry of films can be improved by this method of evaporation, some difficulty was experienced in measuring the temperature of the source and hence in controlling the rate of evaporation. The cadmium sulphide, although it is known to evaporate at approximately 700°C, appeared to evaporate at temperatures as low as 600°C. The positioning of the thermocouple was found to be critical and a considerable temperature gradient existed within the indentation within which the thermocouple was inserted. Furthermore, while it was not difficult to measure the actual temperature of the substrate heater,

it was by no means certain that the substrate itself was at the same temperature. Poor thermal contact is likely to exist between the glass or mica substrate and the aluminium heater and temperature differences of up to 100 C degrees have been reported. [57] It is possible to improve the thermal contact by evaporating a low melting point metal backing on to the substrate. Lastly, as the substrate is positioned close to the mouth of the quartz tube, it is not easy to monitor or observe the formation of the film. These are the main disadvantages associated with this method.

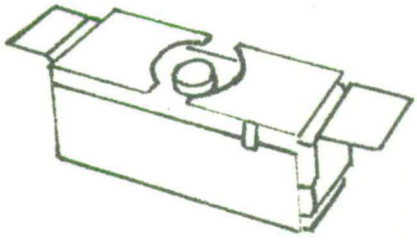
4.5.2 CHIMNEY METHOD.

Brunnschweiler [58] was able to deposit single crystals of cadmium selenide of some 1.5cm diameter on mica by evaporation of the compound. The essential difference in his method lay in the high substrate temperature used. The mica substrate was initially held at 200°C when the sticking coefficient is sufficiently large to enable a film to form. Immediately the initial layers of the film formed, the substrate temperature was increased to approximately 450°C. Further deposition was allowed to take place slowly and an epitaxial formation was obtained. The vapour pressures of cadmium and selenium are much closer in value than those of cadmium and sulphur. In such circumstances, epitaxial growth could reasonably be expected to occur more readily. However, the technique was applied using cadmium sulphide, and using substrates of borosilicate glass and mica.

The evaporation system is shown in Figure 4.8. The tantalum baffle source was supplied by the Allen-Jones Corporation, California. Cadmium sulphide was



(a)



(b)

(c)

Fig. 4.8 Evaporation Systems for Method 2.

(a) Tantalum chimmey
(b) Tantalum baffled source
(c) Cross-sectional view of source

placed in the compartments at each end and the evaporant issued from the funnel in the centre. The substrates were encased by a "chimney", also of tantalum. They were placed on a ledge half way down the chimney which was of similar cross-section and 15cm in length. The cadmium sulphide source was placed close to the bottom of the chimney, thus forming an almost closed chamber between the substrate and the source. The chimney was heated by by passing current through it and the temperature was monitored by inserting a thermocouple from the top and placing it near to the substrate. With this method, the temperature of the substrate could be controlled easily and measured accurately. Also the chimney served both as a substrate holder and heater. Attempts were made to measure the source temperate, again using thermocouples but this proved to be difficult and to have a critical dependence on the positioning of the thermocouple.

Prior to any evaporation, the chimney and substrate were outgassed at 500°C. The initial film deposit was made with the substrate temperature at 200°C to 220°C. It was then raised to between 450°C and 500°C. The inability to control the source temperature accurately made it necessary to monitor the formation of the film continuously during the evaporation and particularly during the initial evaporation at the lower temperature. At this stage, the film forms quickly and it is necessary to reduce the evaporation rate, i.e. source temperature, in addition to increasing the substrate temperature. Failure to do this results in a thick film forming quickly at the lower temperature and evidence will be produced later in the chapter to show that the crystalline structure of such films is not as well ordered. This monitoring was performed rather crudely by eye, by directing a beam of light along the chimney through

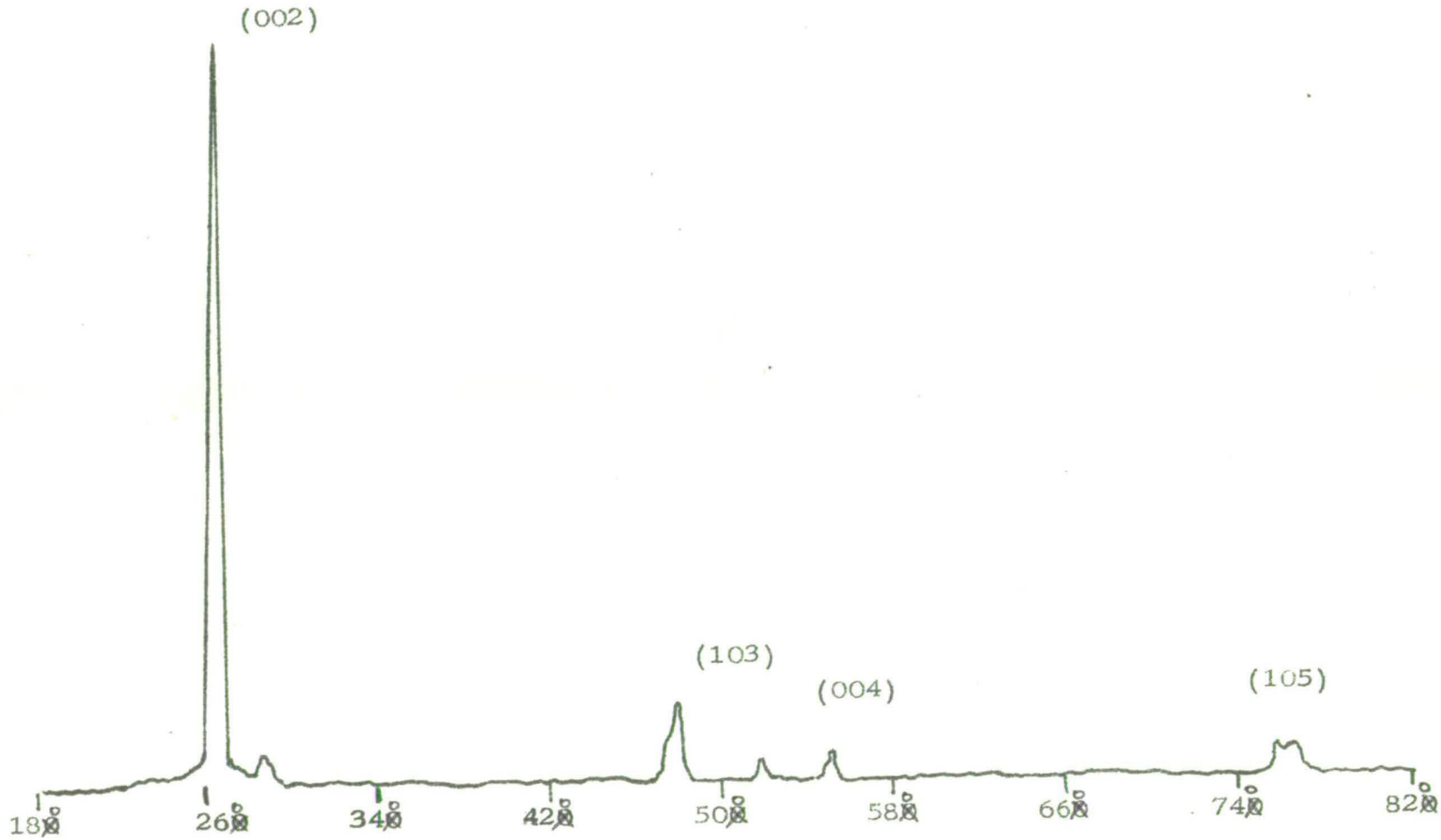


Fig. 4.9 X-ray diffractometer trace of CdS film on glass showing predominance of (002) reflection.

the substrate and reflecting the transmitted light out of the chamber. The use of "dead reckoning" procedures, setting temperatures at the same value for each evaporation, yielded results which were quite unpredictable and produced films varying in thickness and colour. On occasions no films formed.

It was found that a slow evaporation rate was required to obtain light-yellow high resistivity films, e.g. the deposition time for a film of 3000Å to 5000 Å was approximately 30 minutes. Films deposited on glass were polycrystalline. X-ray diffraction charts (Figure 4.9) showed strong (002) reflections indicating that the crystallites were orientated with their c-axes normal to the substrate. In some cases, relatively strong reflections occurred at the (103) plane and the K_{α_1,α_2} doublet was usually resolved by the (105) reflection. X-ray diffraction photographs yielded a series of Debye-Scherer rings.

Films deposited on mica, which was freshly cleaned immediately prior to placing in the evaporation chamber, showed a high degree of orientation and an epitaxial formation. No X-ray diffractometer traces were taken, owing to the difficulty of removing the background reflections from the mica, but X-ray reflection diffraction photographs yielded a distinct pattern of spots, Figure 4.10. In order to identify completely the reflections from the cadmium sulphide films, an X-ray reflection diffraction photograph was taken of a single crystal of cadmium sulphide and this is shown in Figure 4.11. For transmission electron diffraction studies attempts were made to remove the cadmium sulphide film from the mica, but these were unsuccessful apart from one occasion. In this instance, the film formed quickly and mostly at the lower temperature. The diffraction pattern obtained is shown in Figure 4.12 and does not reveal the degree of epitaxial formation attained in Figure 4.10.

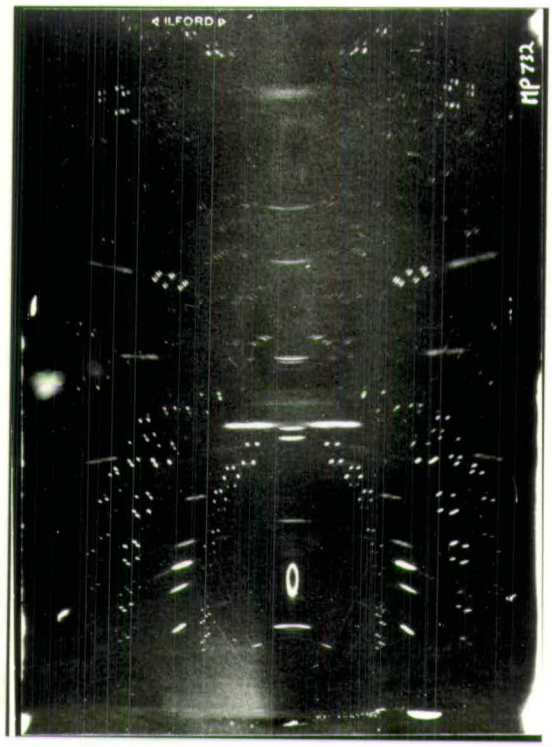


Fig. 4.10 X-ray reflection diffraction photograph of CdS on mica (chimney method).

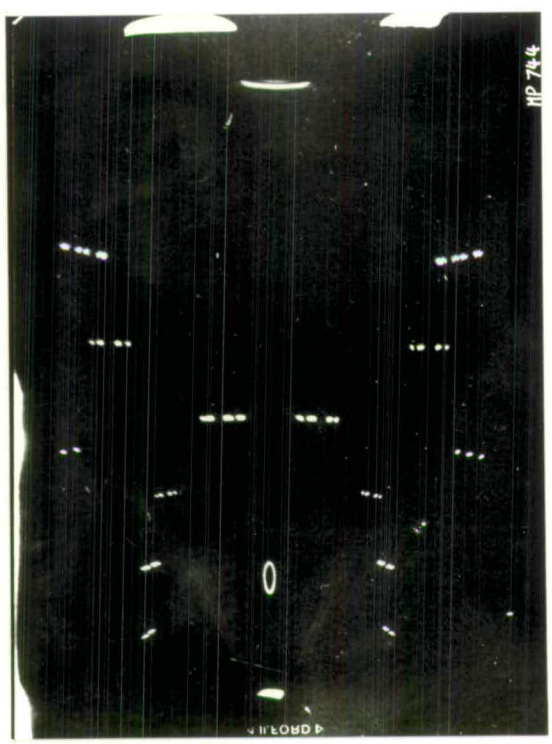


Fig. 4.11 X-ray reflection diffraction photograph of a single crystal of CdS.

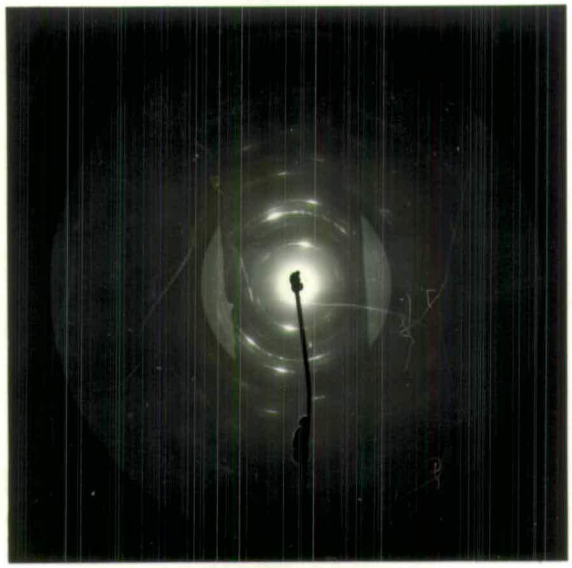


Fig. 4.12 Transmission electron diffraction photograph of CdS on mica (film deposited quickly).

It was indicated earlier that attempts have been made by various workers to improve the stoichiometry of cadmiun sulphide films. No serious effort was made to investigate these methods fully, but two of them, heating in selected atmospheres and heating in the presence of an activator, were considered. In the case of the former method dark coloured films, containing an excess of cadrium, which were deposited on glass, were heated in air or an inert gas such as argon at 500°C for 15 minutes. A pronounced colour change occurred, each film becoming more yellow. However, no difference could be discerned in X-ray diffractometer reflections obtained before and after heating. Following the activator method used by Gilles and Van Cakenberghe [50], a thin film of silver about 200 Å thick was evaporated on to the cadmium sulphide layer and baked in argon at 500°C. Recrystallization took place and this was detected by the X-ray diffractometer technique. This showed a significant decrease in the intensity of the reflection from the (002) plane and a similar increase from the (103) plane. However, the metallic silver layer on the surface precludes the possibility of fabricating a thin film transistor with the cadmium sulphide as semiconductor. The evaporation sequence was reversed but no recrystallization of the cadmium sulphide took place, probably because of a chemical reaction occurring between the silver and the sulphur which interfered with the catalytic action of the silver. No further work was performed on recrystallization of films.

In most cases it was found that films deposited on glass substrates were opaque and had a matted appearance. Several unsuccessful attempts were later made to fabricate thin film transistors using these films and this led to an investigation of the film surface. The opaque matted appearance is due to light being

scattered at the surface, suggesting that the surface was not smooth. An estimate of the roughness was obtained using the Talysurf. This revealed that films of some 5000 Å in thickness could have surface spikes up to 1000 Å in height. Electron micrographs, using the carbon replica technique, were taken and a typical surface for a glass substrate is shown in Figure 4.13. The crystallite structures were less than 1 micron in size. Figure 4.14 shows a surface micrograph which has been shadowed at an angle of 45° with a gold-palladium alloy. The irregularities on the surface can clearly be observed and are calculated to be up to 1500 Å in height.

The epitaxial film obtained on mica suggested that a similar formation could be obtained on other substrates of suitable crystalline structures. Small sapphire slides polished on one side but unfortunately not cut in any preferred direction were available. Films evaporated on to these substrates, which were cleaned in the same way as the glass substrates, did not show an epitaxial growth. A micrograph of a film surface taken with the scanning electron microscope is shown in Figure 4.15. The crystallite structures are similar in size to those obtained on glass substrates. It should be added that only a few films were evaporated on to sapphire substrates.

Films deposited on mica substrates were found to be smooth, as can be seen from the micrograph in Figure 4.16. The essential difference in the formation of these films lay in the cleaning procedure adopted. It was thus decided to use ion bombardment cleaning. An aluminium probe was placed in the lower half of the chimney and an a.c. glow discharge was initiated using argon. The probe voltage was approximately 800 volts with an argon pressure of 0.15 torr.

Fig. 4.13 Electron micrograph of CdS film on glass (x 35,000).

Fig. 4.14 Electron micrograph, shadowed at angle of 45°, of CdS film on glass (x 35,000).

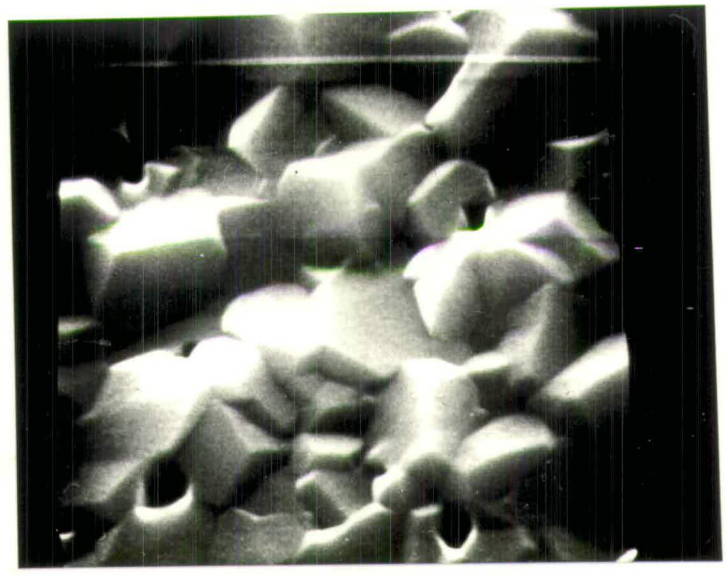


Fig. 4.15 Scanning electron micrograph of CdS film on sapphire (x 24,000).

Fig. 4.16 Electron micrograph of CdS film on mica (x 35,000).

It was difficult to restrict the discharge to within the chimney walls and generally breakdown occurred near the voltage feedthrough electrode. The duration of the discharge was 20 minutes. Evaporation of the cadmium sulphide was then performed in the normal manner. Films deposited on glass in this way were clear and exceptionally smooth, the same interference fringe colour frequently extending over the complete film. An electron micrograph of a smooth film is shown in Figure 4.17. An X-ray diffraction photograph yielded a series of Debye-Scherrer rings. The pronounced difference in texture of the two cases is obvious from the colour photograph of Figure 4.18.

The chimney method of evaporation overcomes the difficulty of holding and heating the substrate and permits the temperature to be measured easily. It also provides films of better crystal order and orientation than the first method. All cadmium sulphide films used in the device work to be described were prepared by the chimney method. The pronounced effect of ion bombardment of the substrate on the texture of the films suggests that a more sophisticated cleaning procedure, probably avoiding the use of chromium trioxide, is necessary.

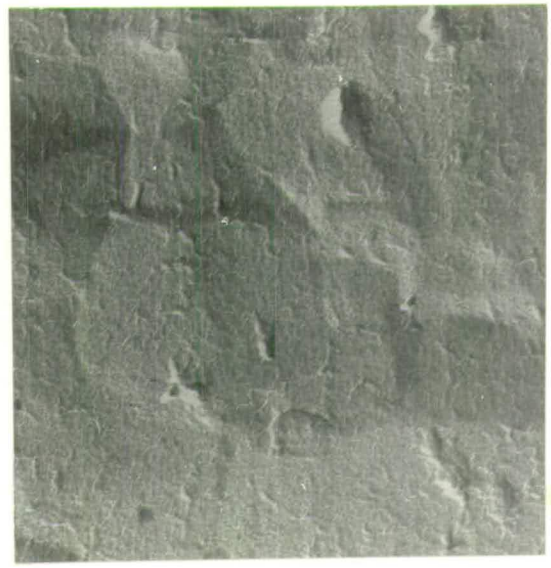


Fig. 4.17 Electron micrograph of CdS film on glass, substrate ion bombarded.

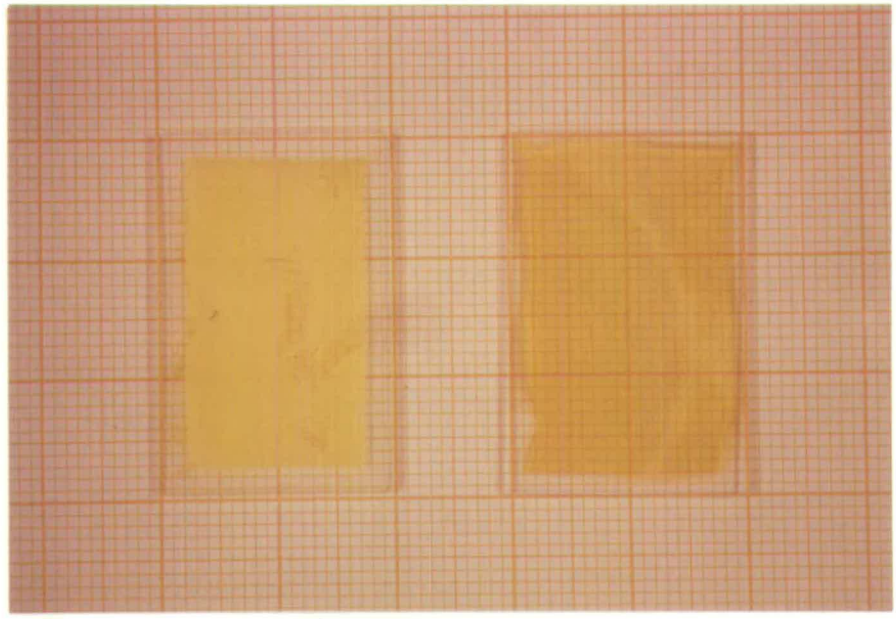


Fig. 4.18 Colour photograph of CdS on glass; without ion bombardment (L.H.S.), and with ion bombardment (R.H.S.).

CHAPTER 5.

THE METAL - SEMICONDUCTOR CONTACT.

5.1 HISTORICAL NOTES.

The earliest studies of metal to semiconductor contacts were concerned with rectification effects. Braun [59] as long ago as 1874 worked with a variety of natural crystals, mostly lead and ferrous sulphide, to which he applied various base electrodes and a point contact by means of a fine wire. He noted the dependence of the total resistance on the polarity of the applied voltage. In addition, Braun [59] made the first observations of rectification effects in selenium, and also worked with copper oxide. In later years plate rectifiers using copper oxide, and selenium, found practical application in power rectification. A copper rectifier consisted of a copper plate (METAL) on which a layer of cuprous oxide (SEMICONDUCTOR) was formed by heating, the surface of the oxide being pressed into a lead plate. Point contact rectifiers were employed in the early days of radio telegraphy - between 1920 and 1930 - as detectors, i.e. the crystal detector. Some of the more satisfactory devices were based on lead sulphide. It was then almost entirely replaced by the vacuum tube until in 1939, application of a silicon detector for microwave work was reported by Southworth and King [60]. The point contact was made by means of a tungsten wire. Research on germanium and silicon was carried out during the war in connection with point contact detectors for radar. It was the continued study of the nature of the forward and reverse currents to a

point contact to germanium which later led to the discovery of the transistor effect as embodied in the point-contact transistor.

The understanding of rectification phenomena developed slowly. Owing to the commercial importance, Schottky showed that in the direction of resistance, practically all the potential difference occurred at the contact between the copper and the oxide. He then postulated [61] that an insulating layer existed between the copper and the copper oxide and that this was owing to the formation of a cupric oxide layer nearest to the copper. Capacitance measurements permitted an estimate of the thickness of this "blocking layer" to be made. For this particular case, Mott [62] developed a theory to describe the current flow by considering the electrons to be thermally excited across the barrier. Schottky [63] realized that a potential barrier could be formed without the presence of a chemically distinct layer and suggested that it arose from stable charges in the semiconductor. He considered these charges to arise from the presence of the metal electrode. Davydov [64] then emphasised the need for a difference in the thermionic work functions of the materials. It was in this manner that the "Schottky barrier" model of a metal to semiconductor rectifying contact developed.

5.2 THE SCHOTTKY BARRIER.

Consider now, according to the Schottky model, the barrier which results from improper matching of the work functions between the metal and the semiconductor forming the contact. Figure 5.1(a) shows the energy level diagrams of an n-type semiconductor . The energy levels are illustrated for a metal with

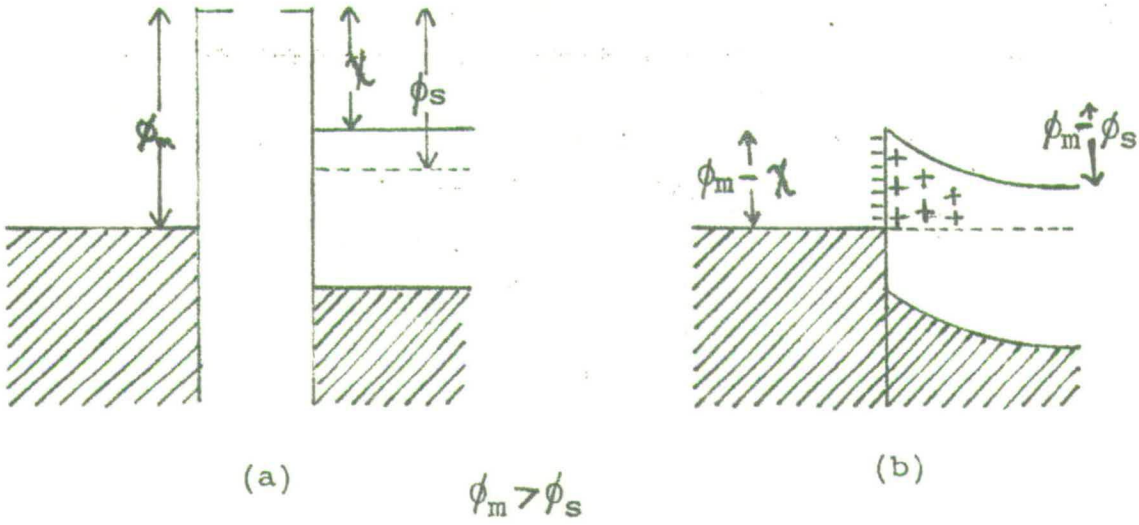


Fig. 5.1 Energy level representation of a contact between a metal and an n-type semiconductor (a) before contact (b) after contact. Metal had greater work function than semiconductor.

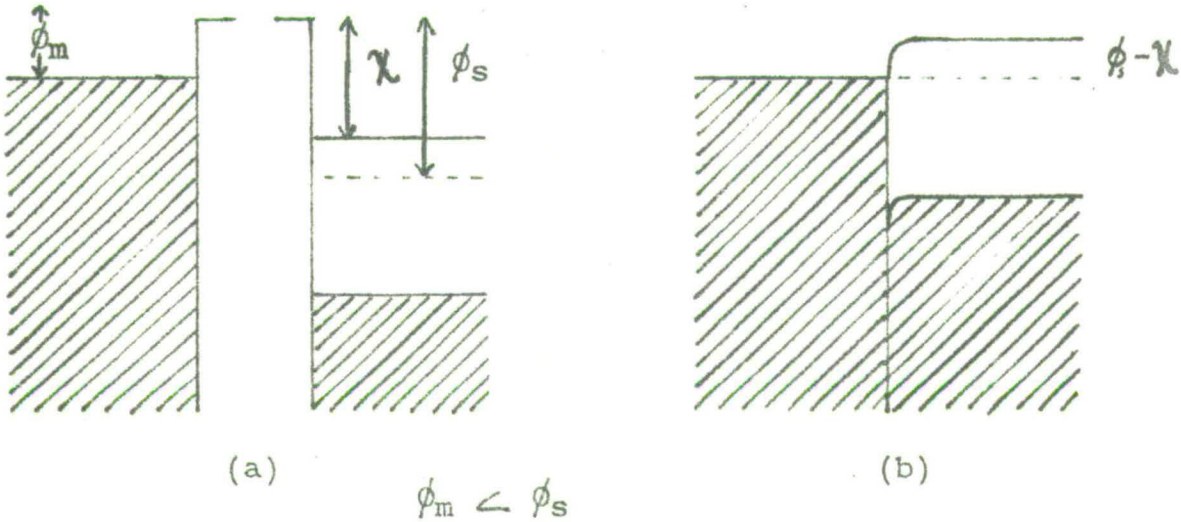


Fig. 5.2 Energy level representation of a contact between a metal and an n-type semiconductor (a) before contact (b) after contact. Metal with smaller work function than semiconductor.

work function ϕ_m, and for a semiconductor with electron affinity χ and work finction ϕ_s, when the metal and semiconductor are still separate. For the case illustrated, the work function of the metal exceeds the work function of the semiconductor. When the metal and semiconductor are brought into contact, electrons flow from the semiconductor into the metal until the Fermi levels equalize. This transfer of electrons continues until the field set up by the double layer established in this way is sufficient to balance the diffusion current due to the electron concentration gradient. Finally the situation shown in Figure 5.1(b) will be obtained, a barrier having been formed by negative charge at the contact and positive charge, in the form of ionized donors, distributed in a volume of the semiconductor.

Figure 5.1(a) and Figure 5.1(b) show the alternate case for a contact between a metal and n-type semiconductor when the work function of the metal is less than that of the semiconductor. No barrier forms when contact is made. Instead a reservoir of electrons exists in the semiconductor near the contact. Such a contact is commonly called an ohmic contact, because no rectification occurs and the currents passing through the contact obey Ohm's law over a large range of applied voltage. It is this type of contact which the source and drain electrodes in a thin film transistor must make with the cadmium sulphide layer.

Many experiments were carried out to obtain evidence for the behaviour of metal to semiconductor contacts in accordance with the Schottky theory. Schwerchent, as quoted by Schottky [65], has found a relation between the resistance of selenium rectifiers in the blocking direction and the work function of the metal. Selenium is a p-type semiconductor and high reverse

resistance was found for low work function metals. Brattain has ~~formed~~ found a good [66] ~~correlation~~ relation between degree of rectification and work function for metal contacts evaporated on cuprous oxide and n- and p-type silicon. On the other hand, Ioffe [67] and Meyerhof [68], particularly the latter, did not find such clear cut relationships. Meyerhof studied the relation between the contact potential difference and rectification for metal point contacts applied to silicon and germanium and found that the contact potential difference was independent of the work function of the metal for silicon rectifiers. To explain the contradictory nature of these results, Bardeen [6] proposed that the existence of surface states could modify the formation of the Schottky barrier. As shown in Chapter 2, the presence of surfaces states causes an intrinsic potential barrier to exist at the surface of the semiconductor, and the energy bands will be bent before any contact is made with the metal electrode. If the density of surface states is sufficiently large, the field caused by the contact potential is almost entirely terminated by the surface states rather than by the space charge in the semiconductor. The barrier height then remains practically independent of the work functions of the materials and the system behaves as though the semiconductor surface were a thin metallic film screening the bulk from external fields. As an example of this, Bell and Leivo [69] have shown that rectification with semiconducting diamond was independent of the work function of the metal and depended on the presence of surface states.

It should be noted that owing to the adsorption of impurities on the surfaces great difficulty is generally experienced in obtaining a pure metal to semiconductor contact. The presence of a third layer, such as an oxide, can alter the work function and the surface state density and so form a potential

barrier. The lack of consistency in experimental results may, in part, be attributed to this fact. As an instance, it was shown by Poganski [70] that in the selenium rectifier, the barrier layer does not occur at the boundary between the tin-cadmium alloy and the selenium. A chemical reaction between the tin-cadmium electrode and the selenium during preparation of the rectifiers leads to the formation of a cadmium selenide layer and the potential barrier is located at the boundary between the two semiconductors, cadmium selenide and selenium, rather than at the metal to semiconductor contact.

5.3 OHMIC CONTACTS TO CADMIUM SULPHIDE.

The electron affinity, χ, of single crystal cadmium sulphide is 4.5eV [71]. For cadmium sulphide films, Shuba found the electron affinity to be 3.3eV, [71] assuming a band gap of 2.4eV. On the basis of the Schottky model, the work function, ϕ_m, of the metal contact should not differ appreciably from this value if an ohmic contact is to be obtained. The density of carriers, N_o, available to the semiconductor at the interface in terms of the barrier height, $(\phi_m - \chi)$, is shown in table 5.1 below. [72]

TABLE 5.1

$(\phi_m - \chi)$eV	0.1	0.5	1.0
N_o (cm^{-3})	10^{17}	10^{10}	10^{2}

It is obvious from the table that at room temperature excited electrons can pass over a barrier of approximately 0.5eV in sufficient number that the contact may be regarded as ohmic.

The work functions of the elements have been collated in the form of a table by Michaelson [73], although there is considerable variation in some cases in the values obtained by different workers. R.W. Smith [74] examined the problem of metal contacts on to insulating crystals of cadmium sulphide and found that the lower work function elements, indium and gallium, formed an ohmic contact, whereas the higher work function elements, silver, gold and copper, did not. He suggested that a low work function can overcome the effect of the surface states to the extent of reversing the curvature of the band structure at the surface. Most of the low function metals are extremely reactive chemically, and so in practice are not suitable for electrodes. In addition to indium and gallium, aluminium is suitable both from work function (4.2eV) and chemical considerations. Walker and Lambert [75] investigated the rectifying properties of point contacts of various metals in a conducting crystal of cadmium sulphide and found no rectification if the point contact were indium or gallium. Kroger et.al. pointed out that indium and gallium are both n-type impurities [76] in cadmium sulphide, whereas other metals, such as copper, silver and gold, which do not form ohmic contacts, are p-type impurities. Kroger argued that the ohmic contacts found with indium and gallium (and n-type cadmium sulphide) were the result of diffusion of the indium and gallium into the cadmium sulphide around the contact, resulting in the formation of a highly n-type region.

Figure 5.3 shows the band model of the contact according to Kroger.

The material in contact with the metal electrode is an n-type semiconductor, in which the Fermi level lies between the donor levels and the bottom of the conduction band. Since the donor levels lie near the conduction band, the

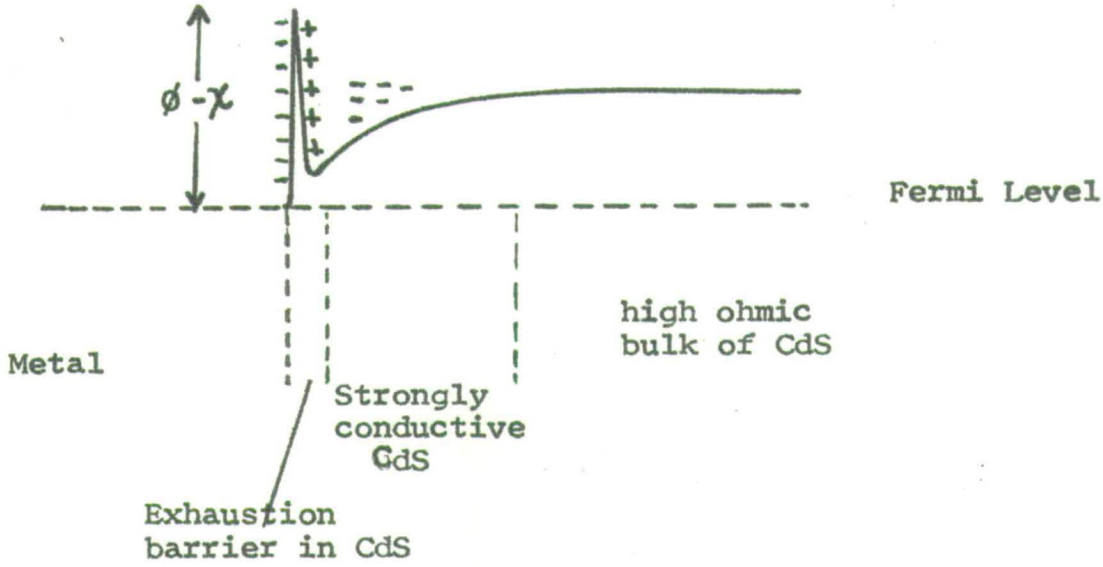


Fig. 5.3 Proposed band model of ohmic contact.

Fermi level is just below the conduction band and is therefore above the Fermi level of the metal before contact. After contact, there exists adjacent to the electrode an exhaustion barrier which, in a highly doped material, is so thin that electrons may easily tunnel through it. This highly doped region acts as a supply of electrons for the highly resistive bulk.

Butler and Muscheid [77] have shown that ohmic contact could be made to cadmium sulphide crystals independently of the electrode work function, if the contact area were first subjected to electron bombardment. In addition, Fassbender [78] has reported that ohmic contacts could be formed by ionic bombardment by an electric discharge. Anderson [21] has made use of this technique in this department in his study of scl currents in insulator diodes.

5.4 EVAPORATION OF SOURCE AND DRAIN ELECTRODES.

On the basis of the Schottky barrier model of a metal to semiconductor contact, gallium, indium and aluminium have work functions which are small enough to make an ohmic contact with cadmium sulphide. Furthermore they are chemically stable. The work functions and melting points for these elements in the order listed above are 3.96eV, 4.0 eV and 4.2eV and 29.4°C, 150°C and 660.1°C. The low melting point of gallium and indium precludes the use of the former completely in thin film transistors and raises doubts about the suitability of the latter owing to high temperature processing required for subsequent layers.

The spacing between the source and drain electrodes in a thin film transistor is generally less than 25 microns and Weimer has used separations as small as

7 microns. A small separation provides a short carrier transit time between the source and drain, and this improves the frequency response of the device. A fine wire was used as a mask to achieve this small separation. The smallest diameter wire readily available was 15 microns, although a limited quantity of wire of approximately 10 microns diameter was obtained. It proved extremely difficult to handle and only wire of 15 and 25 micron diameter was used.

The set of masks, etched from mild steel feeler strip for the complete TFT structure is shown in Figure 5.4. The supporting jig was made of stainless steel. The profile for the source and drain electrodes is on the left hand side of the set, the fine wire for the separation being positioned beneath the feeler strip. This results in the wire being out of contact with the substrate, which rests on the jig, by a distance equal to the thickness of the feeler strip, 1 mil. All materials were evaporated upwards. Despite the fact that the wire was not in contact with the substrate, a sharply delineated gap was obtained provided evaporation took place at a pressure not greater than 10^{-5} torr.

With higher pressures it was found that the evaporant scattered behind the wire mask causing a short circuit between the source and drain. Figure 5.5 illustrates aluminium electrodes, of 36 microns separation, evaporated on to a cadmium sulphide film deposited on a glass substrate. It can be seen that the gap region is not as sharply defined as the edge of the source-drain region where the mask is in contact with the substrate, showing that there is some scattering of the evaporant behind the wire.

The problem of attaching leads to the electrodes remained and several methods were considered. The standard microelectronic technique of thermal compression

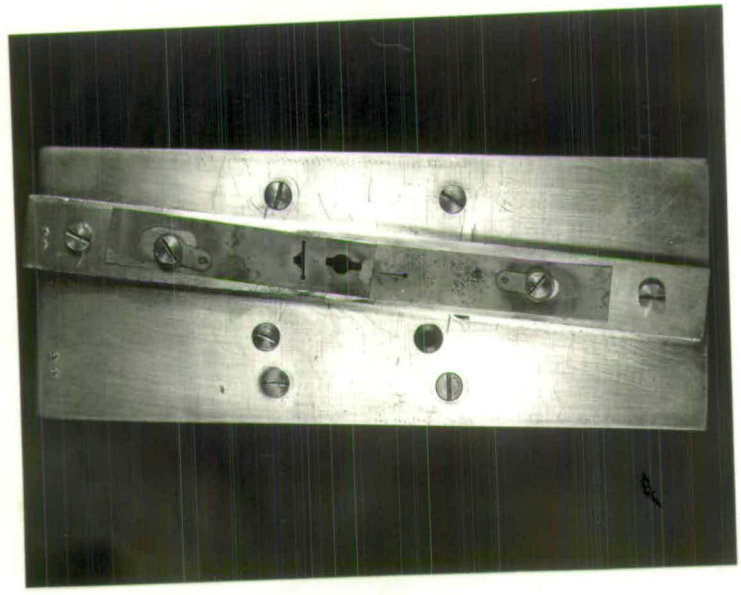


Fig. 5.4 Mild steel masks for TFT evaporation on supporting jig.

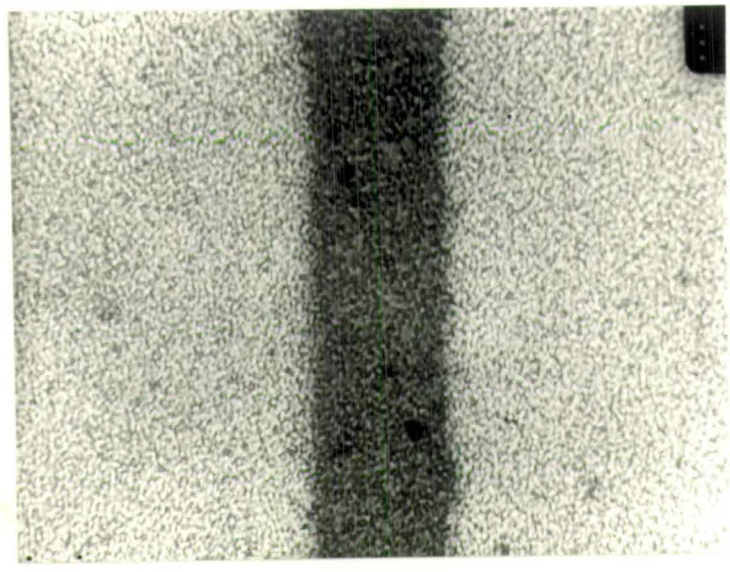


Fig.5.5 Aluminium source-drain electrodes (x 600).

banding of gold wire was not available. Apart from this, the method requires a substrate temperature of at least 250°C, usually 300°C, and it was not thought advisable from differential expansion considerations to subject the device, with its layered structure of different materials, to such high temperatures. In addition, gold bonding in this way to aluminium, which would oxidise readily at 250°C, results in the formation of a number of alloys, the most common of which is referred to as "purple plague". This introduces an unreliability into the method and eventually can cause the bond to become open circuit.

The initial method used, shown in Figure 5.6, was not entirely satisfactory and involved the evaporation of gold lands, with an underlay of chromium as the former does not adhere to glass, on to which lead wires were soldered. Additional masking was required for the cadmium sulphide deposition. During the evaporation of silicon monoxide for the complete device, a high substrate temperature, approximately 300°C, is recommended by some authors [79] and it was found that a "purple plague" formed where the aluminium of the source and drain overlapped the gold. The aluminium film has a thickness of 600 Å to 800 Å. The steps formed at the edges of the cadmium sulphide and gold-chromium layers could thus, if they were sharp, be points of weakness and cause a break in the aluminium film. Furthermore, the additional evaporation and the masking requirements made it difficult to keep the substrate clean.

In the semiconductor industry, individual microcircuits or transistors are tested using needle shaped probes, which are lowered on to the silicon slice. These probes scratch the films, which are usually of aluminium, but as each

circuit is examined only once, this is of little consequence. A similar method, using gold plated probes, was adopted. Probes with rounded ends were used but despite this there was a distinct tendency to scratch the film (Figure 5.7) and frequent use produced an unreliable contact. Indium, which is softer than aluminium, is particularly easy to scratch and for this reason, coupled with its low melting point of 150°C, it was not considered seriously as a contact material. However, the simplicity of the method is attractive and one is generally able to distinguish between an open circuit probe and a blocking metal to semiconductor contact. This was not always possible in the first method described.

Aluminium is chemically active at high temperatures and refractory materials such as tantalum and molybdenum are not suitable for evaporation boats. A slower reaction occurs with tungsten and it is possible to carry out several evaporations from a tungsten basket before having to discard it. However, it was not easy to obtain a well controlled evaporation with such a boat. Aluminium readily forms an oxide and it is necessary to evaporate this off in the presence of a shutter before exposing the substrate to the evaporant. It is also advisable to evaporate aluminium quickly in order to reduce oxidation by the residual gases in the vacuum chamber. It was found that the aluminium, which was cut from an ingot of 6N purity, fell through the wire basket on melting and consequently it was difficult to obtain from a small basket, a film greater than 600 Å in thickness on a substrate placed 8 inches from the source. A small boat was necessary to obtain a point source and so reduce scattering of the evaporant behind the fine wire mask used for the formation

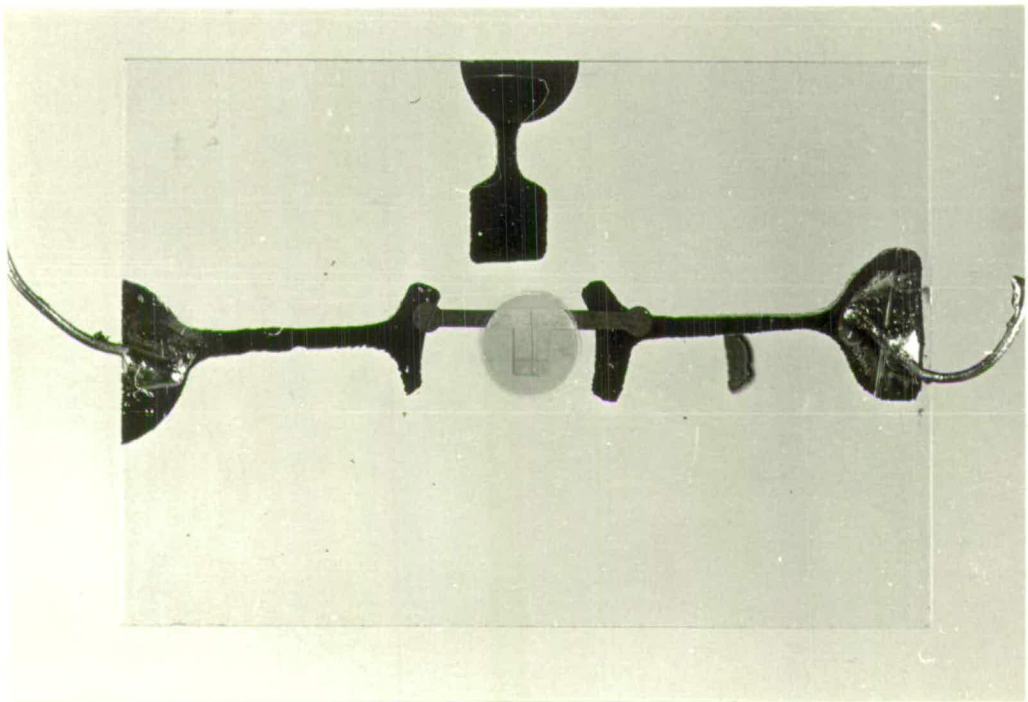


Fig. 5.6 Photograph of evaporation of gold-chrome lands.

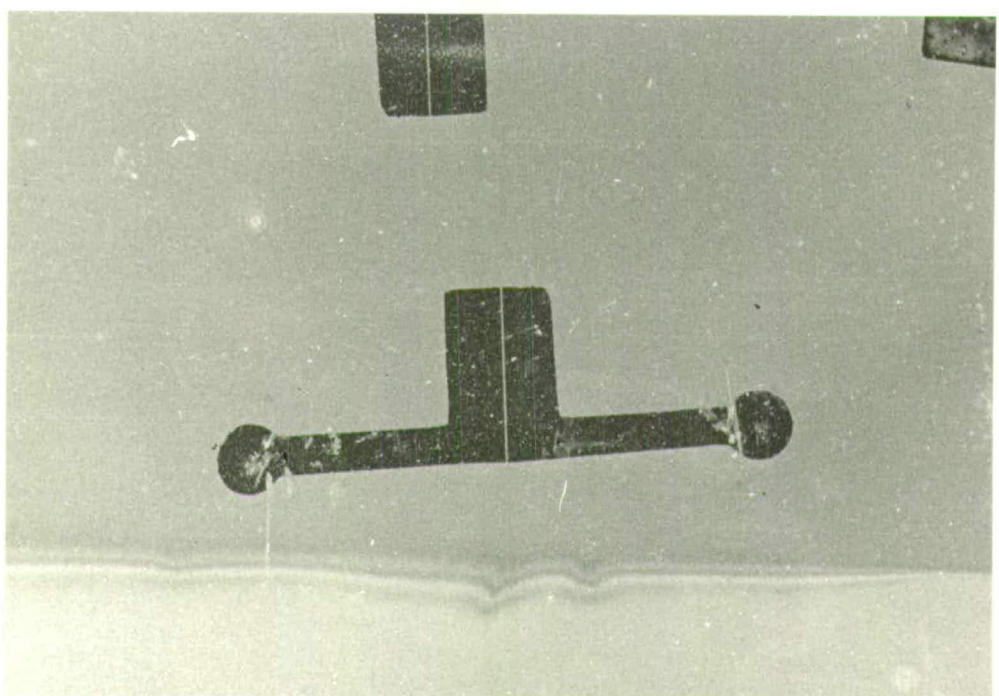


Fig. 5.7 Photograph revealing scratching of film by probes.

of the source-drain gap. In an attempt to gain more control over the evaporation of aluminium, a boron nitride boat, positioned in a tungsten wire basket, was used. Owing to the insulation of the aluminium by the boron nitride boat, it was necessary to run the tungsten basket at a much higher temperature, near white heat, before evaporation was initiated. The larger source produced a less sharply delineated gap and in many cases a short circuit between the source and drain. Also the high temperature required caused considerable out-gassing, producing additional impurities, and it was not possible during an evaporation to maintain a pressure less than 10^{-5} torr. The use of the boron nitride boat was abandoned in favour of the small tungsten basket. However, this method leaves much to be desired and there is little doubt that the electron beam heating offers a cleaner and more controllable means of evaporating aluminium. A quartz crystal was used to monitor film thickness. The mass of the evaporant adhering to the crystal face causes the natural frequency of the crystal to decrease. An absolute measurement of film thickness may be obtained using a Talysurf and it is then possible to calibrate the crystal for a given evaporant and for a given geometrical arrangement of the source, substrate and crystal. The variation of crystal frequency with change in mass is not a linear function but the method was sufficiently accurate for the estimates of film thickness required.

5.5 I-V CHARACTERISTICS USING SOURCE-DRAIN ELECTRODES.

The approach adopted initially was the complete evaporation of the thin film transistor on to the cadmium sulphide layer without exposing the system to

atmospheric pressure between evaporations. These devices invariably suffered from faulty source to drain contacts or poor gate insulation and it became evident that each evaporation required individual investigation.

Considerable difficulty was experienced in obtaining a current injecting contact to cadmium sulphide. The early work described at the beginning of this chapter suggested that indium or gallium were the most suitable materials. Probably with this in mind, Weimer used a "flash" of indium beneath a layer of aluminium. The diffusion coefficient of indium into cadmium sulphide is greater than that for aluminium and this, it was thought, contributed to the formation of an ohmic contact. The first attempts at forming an ohmic contact used this technique but did not yield reproducible results. The procedure followed in some typical attempts is listed below.

Sample 7-125.

Cadmium sulphide heated in a vacuum for 2 hours at 350°C, at a pressure of $< 10^{-5}$ torr, with substrate at 180°C. A liquid nitrogen cold trap was employed.

Result: A blocking contact formed.

Sample 3-115.

Cadmium sulphide heated in a vacuum for $1\frac{1}{2}$ hours at 390°C. Indium-aluminium evaporation at a pressure $< 10^{-5}$ torr at a substrate temperature of 200°C. A liquid nitrogen cold trap was used.

Result: A blocking contact formed.

Sample 20-16.

Procedure similar as in two previous cases except that indium alone used as electrode material.

Result: A blocking contact formed.

By heating the cadmium sulphide in vacuum it was hoped that recrystallization might occur with a corresponding increase in resistivity. It was also thought that some of the adsorbed gases would be removed from the film. Another sample, 18-36, was not heat treated prior to the evaporation of indium electrodes. In this case an injecting contact was formed. The film was photoconductive, of thickness 2800 Å and had a resistance between the source and drain electrode of 2.16 megohms in the dark. Subsequent heating for 1 hour at 300°C in a nitrogen atmosphere reduced this resistance to 0.58 megohms. A scanning electron micrograph, Figure 5.8, showed that the indium had melted and although the gap was in general sharply defined, some spreading of the indium was possible. This could, apart from indium diffusing into the cadmium sulphide, contribute to the apparently more ohmic characteristic obtained after heating. The I-V characteristic and log I - log V plot are shown in Figures 5.9 and 5.10. On the same sample, aluminium formed poor ohmic contact with an inter-electrode resistance of 5 megohms. In the presence of light, the I-V characteristic saturated as shown in Figure 5.11. A further evaporation, using aluminium alone, produced a similar effect, and this will be discussed in more detail later. A final aluminium evaporation with an underlay of indium yielded an ohmic contact. The above evaporations were repeated using another cadmium sulphide film, Sample 25-46, which had been heat treated in nitrogen at 380°C.

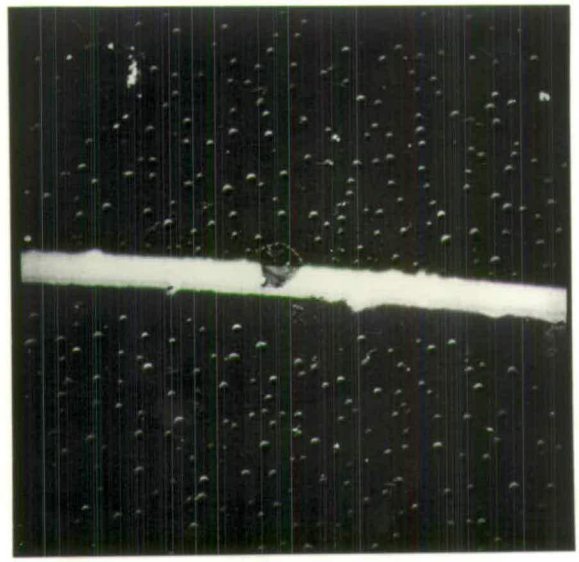


Fig. 5.8 Scanning electron micrograph showing melting of indium (x 170).

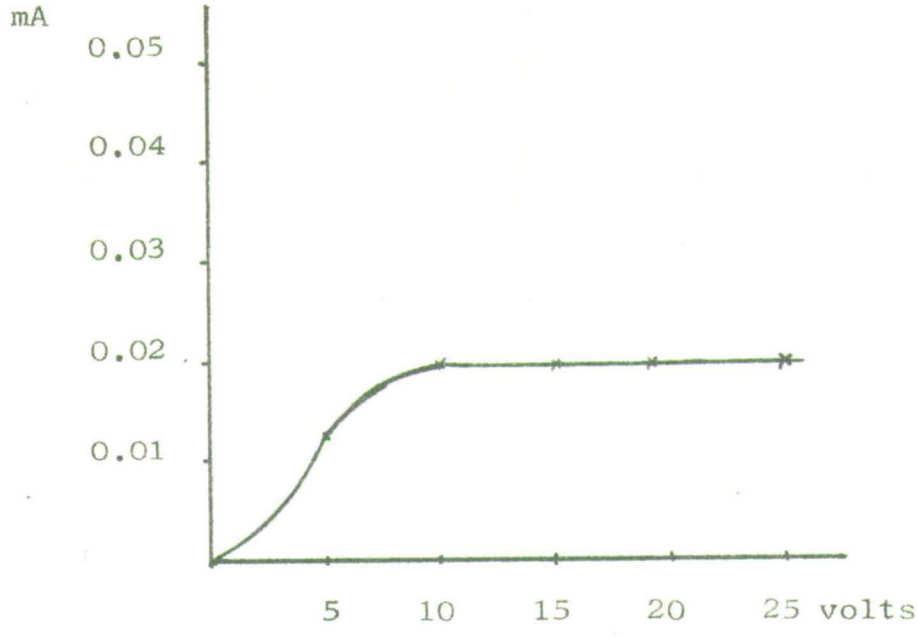


Fig. 5.11 Current saturation obtained with Al electrodes (sample 18-36)

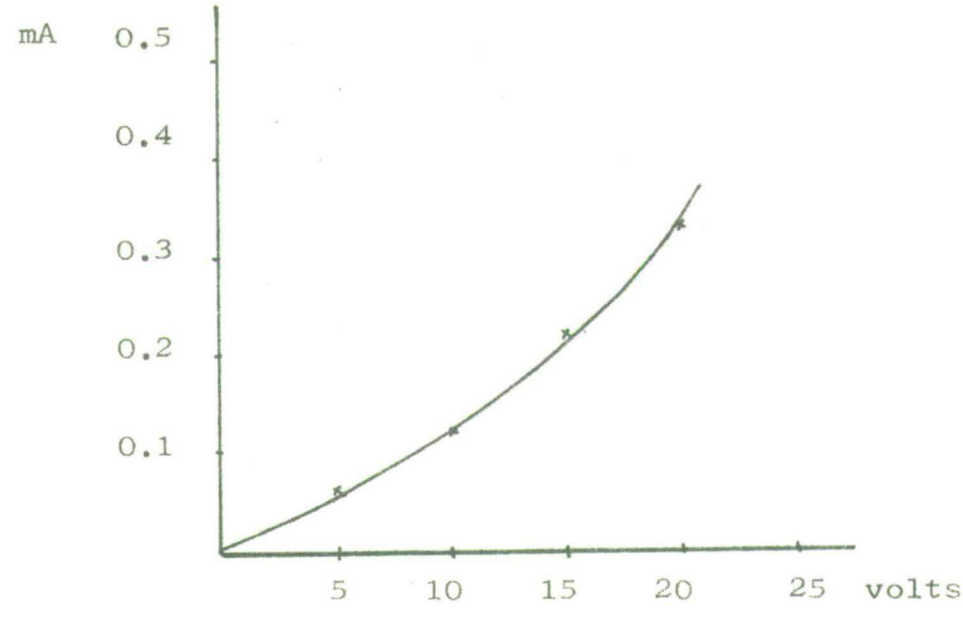


Fig. 5.9 I-V characteristic for In-Al electrodes (sample 18-36)

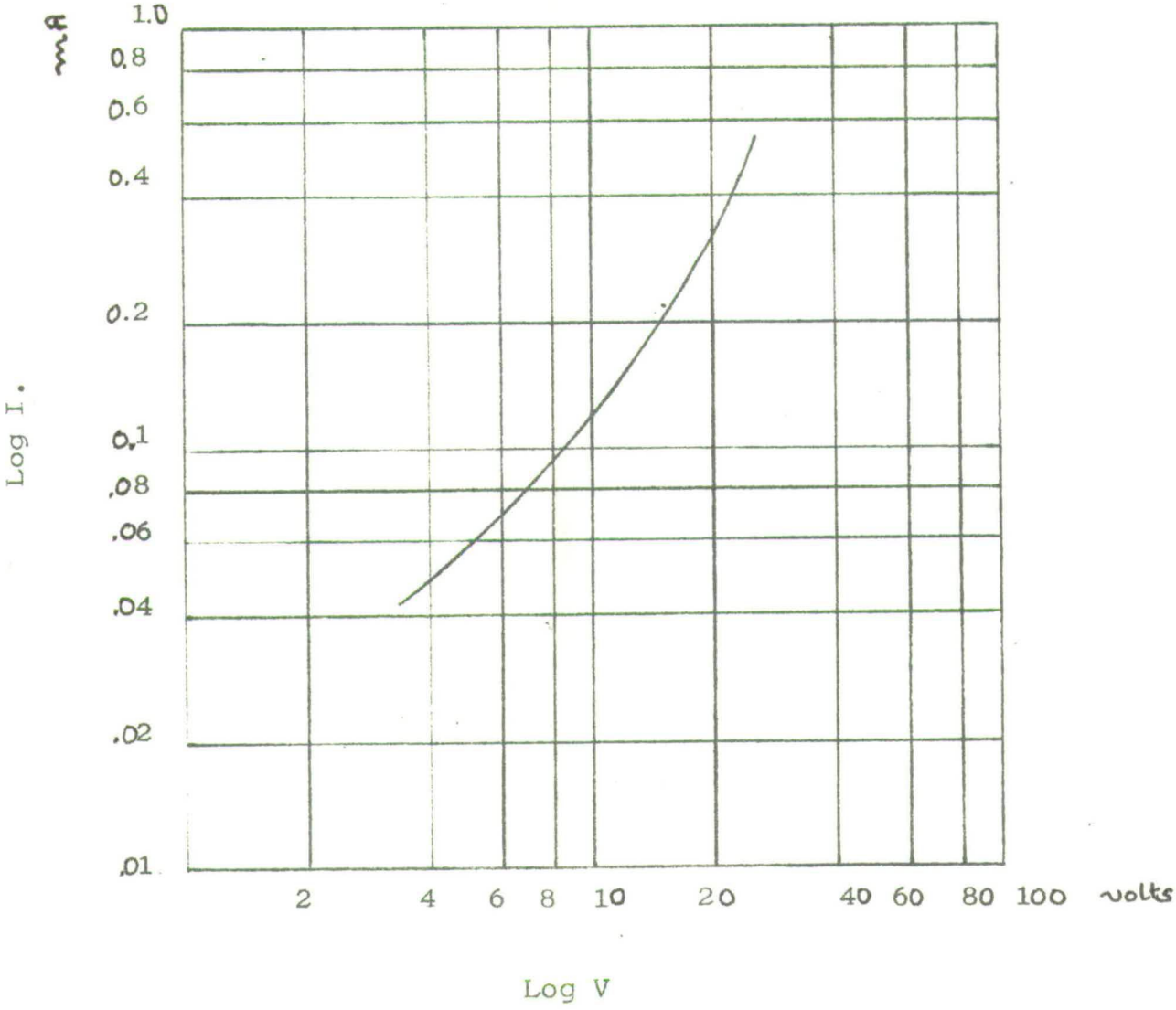


Fig. 5.10 Log I - Log V characteristics for In-Al electrodes.

Two sets of aluminium electrodes formed blocking contacts, whilst a set with a layer of indium preceding the aluminium formed an injecting contact, thus confirming the results obtained with Sample 18-46. The inter-electrode resistance of the latter was reduced by baking in nitrogen at 250°C for 15 minutes.

It became obvious from the results obtained during the early work on contacts, that aluminium did not easily provide an ohmic contact to cadmium sulphide. There were indications that current could be injected as can be seen from Figure 5.11, but such instances were few, and generally a blocking contact was formed. Indium, under certain conditions, was more likely to form an injecting contact which could be improved by heating in an inert atmosphere. The history of the cadmium sulphide film was important and heat treatment in air or in vacuum appeared to hinder the formation of an ohmic contact. Aluminium with an underlay of indium was used in the first attempts to fabricate a thin film transistor. Prior to the evaporation, the chamber was flushed out with argon, and a liquid nitrogen cold trap was used to reduce the water vapour content in the chamber. The substrate was subsequently heated to approximately 300°C during the silicon monoxide evaporation and it was thought that this treatment would aid the formation of an injecting contact. The use of temperatures higher than the melting point of indium required that the indium layer should be thin in order to prevent destruction of the aluminium overlay.

The first successful transistors were made using the above method. However, it was not possible to obtain an ohmic contact regularly and several complete devices were fabricated with blocking source contacts. In addition, problems

arose concerning the gate insulation, and occasions occurred when, owing to breakdown of the insulator, the gate shorted the source and drain making it impossible to determine whether the source formed an ohmic contact or not. Nevertheless, it is essential to be able to inject current freely into the semiconductor, and a reappraisal of the method of forming ohmic contacts had to be made.

It is obvious that the presence of an intervening layer of material between the metal and the semiconductor could completely alter the band structure at the interface and lead to the formation of a blocking contact. There are several ways in which this can occur.

(1) The surface of the cadmium sulphide film can be affected (a) by the adsorption of gases from the atmosphere or (b) by heat treatment in selected atmospheres.

(2) The indium or the aluminium, which has a well known "gettering" action, may react (a) during evaporation with residual gases in the chamber or (b) with the adsorbed gases on the cadmium sulphide surface.

To investigate possibility 2(a) a mass spectrometer was fitted to the top of the vacuum chamber directly above the substrate holder. Figure 5.12 shows that the major constituent in the residual gases was water vapour. The effectiveness of the liquid nitrogen cold trap in reducing the concentration of water vapour is shown in Figure 5.13. An aluminium evaporation was then carried out and the "gettering" action, leading possibly to the formation of an oxide layer can clearly be seen from the water vapour peak in Figure 5.13. The cold trap, a coil of copper tube, was situated above the baffle valve

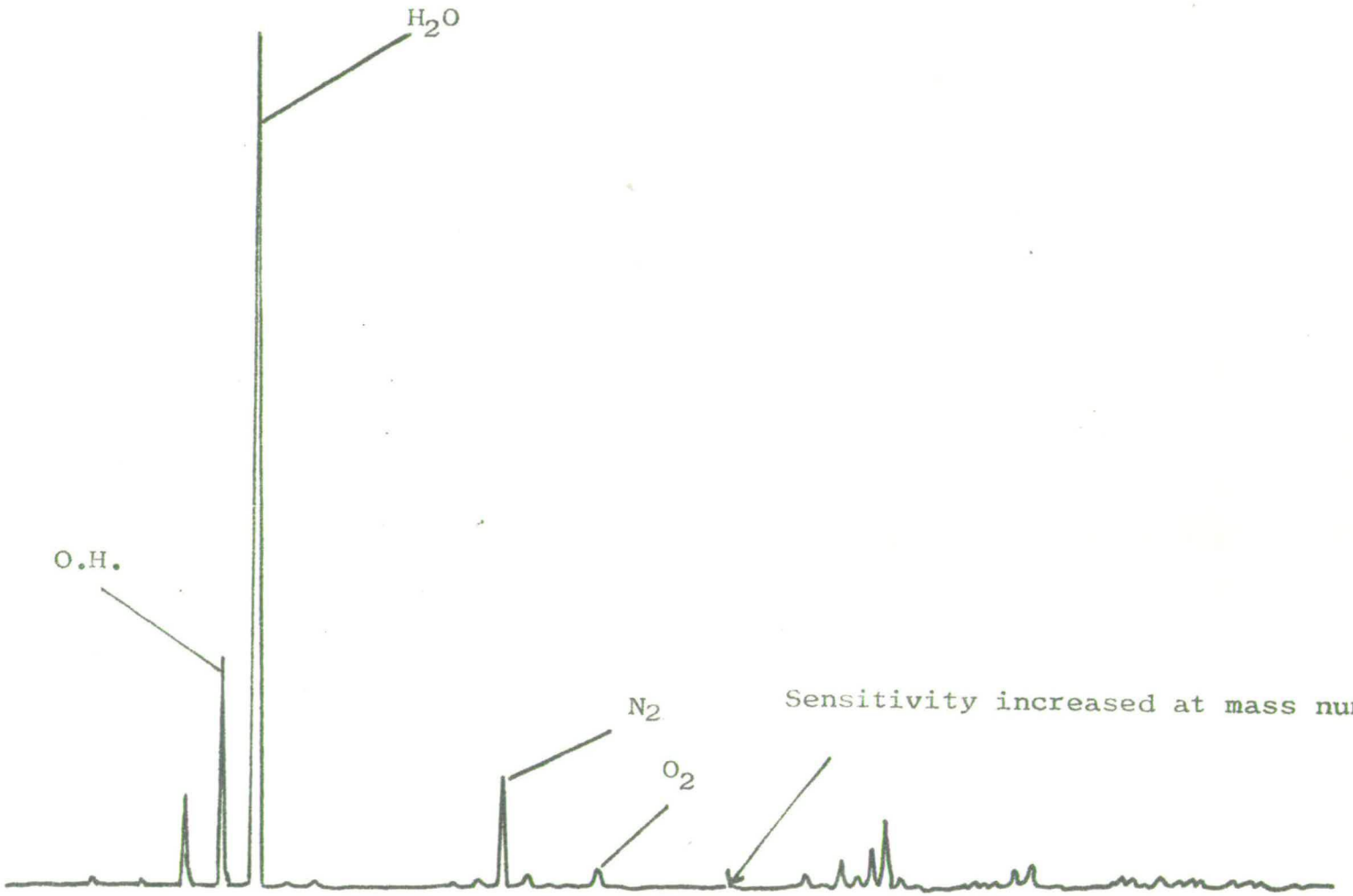


Fig. 5.12 Mass spectrometer plot for mass numbers 12 to 200

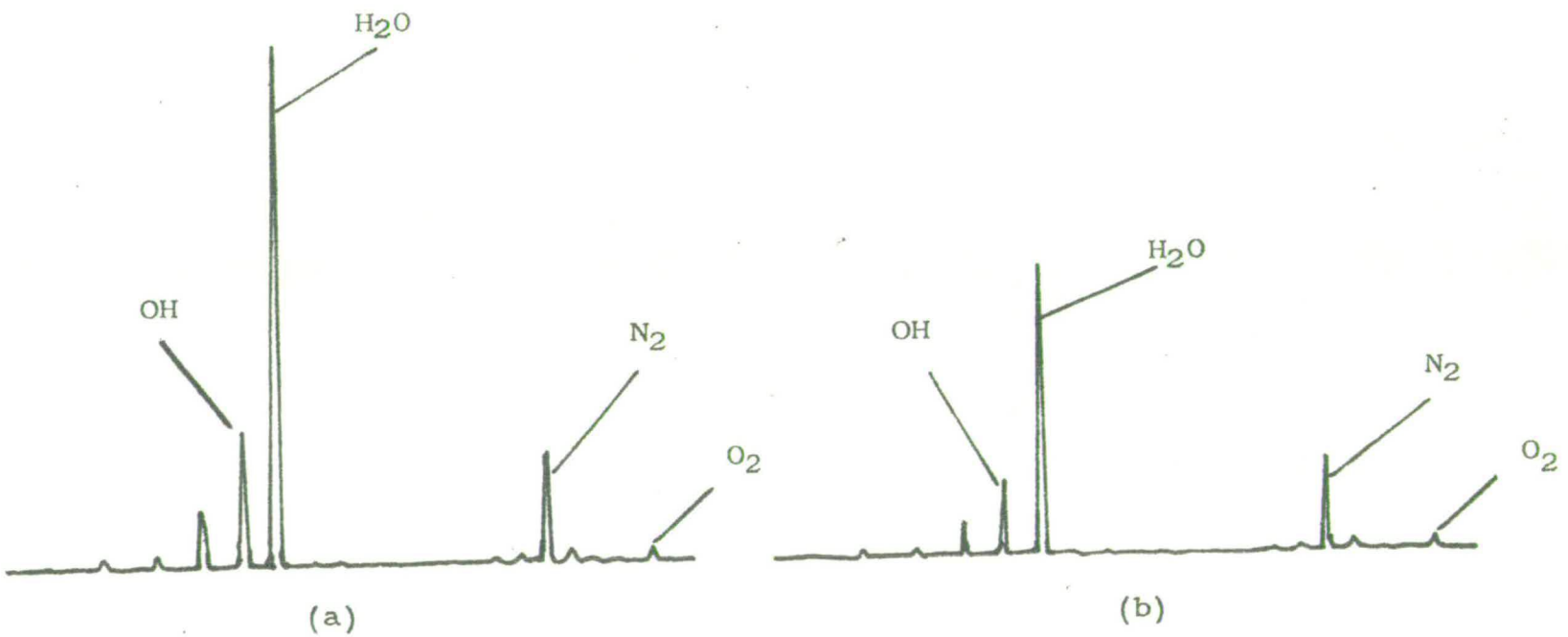


Fig. 5.13 Mass spectrometer plot for mass numbers 12 to 36
(a) before aluminium evaporation
(b) after aluminium evaporation

beneath the vacuum chamber. It was, therefore, remote from the work area and not efficient.

To overcome conditions 1(a) and 2(b), it is necessary to remove adsorbed gases from the cadmium sulphide surface. It was indicated earlier in this chapter that various workers have made use of ion or electron bombardment to produce ohmic contacts and these techniques were adopted. An a.c. glow discharge initiated by an aluminium probe at 500 to 700 volts in an argon atmosphere of approximately 150 microns pressure was used. The duration of the discharge was about 10 minutes. It was found that aluminium, Figure 5.14 and gold, Figure 5.15 readily formed good ohmic contacts. Accurate positioning of the probe with respect to the substrate, generally some 6 inches apart, was not important. Furthermore the previous history of the cadmium sulphide film did not appear to be a discriminating factor and ohmic contacts were formed on films which had previously been heat treated in air or nitrogen. Several log I - log V characteristics were drawn and there was no indication from any of the samples of a square law space charge limited dependence of current on voltage. The gradient of the characteristic varied from sample to sample. Rose [80] has shown theoretically that although a crystal containing shallow traps follows a law $I \propto V^2$, this is not true for traps having a distribution in energies. He also showed that for a uniform distribution of trap energies below the condiction band, $I \propto V.e^{aV}$. The exponential factor is due to the uniformity of the distribution and, for a distribution which decreases with distance from the conduction band, the exponential is replaced by a high power function of the voltage, so that $I \propto V^n$ where $n > 2$. The variability in

I-V characteristic for gold electrodes on CdS (forward and reverse)

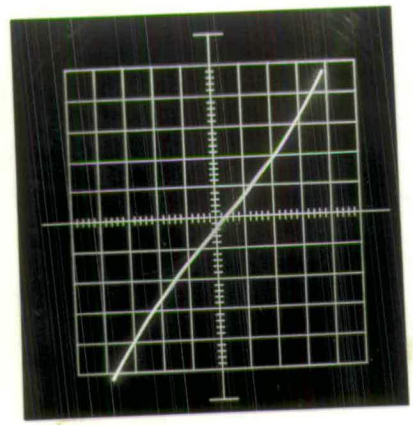


Fig. 5.14 Vertical 0.02 mA/div.
Horizontal 2.0 Volt/div.

I-V characteristic for aluminium electrodes on CdS (forward)

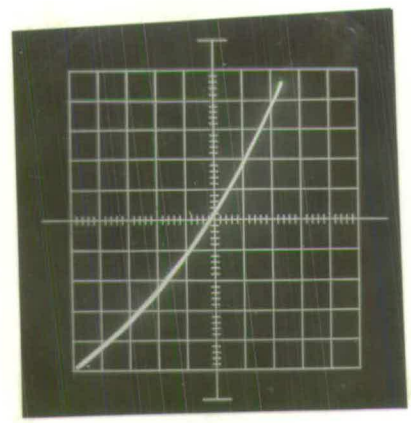


Fig. 5.15 Vertical 0.01 mA/div.
Horizontal 2.0 Volt/div.

the logarithmic plots can therefore be attributed to the variation in trapping levels and densities in the films.

The surface of the cadmium sulphide film was investigated further by taking contact potential measurements. Kelvin's vibrating electrode method was used and for this reason it was necessary to use a non-insulating substrate. The cadmium sulphide was evaporated on to aluminium and contact potential measurements were made with aluminium, which has a work function of 4.1eV, as a reference electrode. The values obtained for the work function of cadmium sulphide after various treatments are shown below.

(a) No post evaporation treatment. 4.85eV

(b) Heat treated in air at 350°C for 10 minutes. 5.15eV

(c) Ion bombardment for 15 minutes. 4.95eV

The results indicate that heat treatment, in air at least, increases the work function of the cadmium sulphide and so forms a less n-type film. Ion bombardment has the opposite effect, and produces a film with an increased surface conductivity, as noticed by Fassbender [78]. In the latter case, Krõger et.al. [76] have attributed the formation of an ohmic contact irrespective of the work function of the metal to a tunnelling mechanism brought about by this high conductivity. The change in conductivity could possibly be brought about by surface damage of the film by the ion bombardment. The pronounced change in work function on heating the cadmium sulphide in air is probably related to a chemical reaction with, and adsorption of, oxygen. It was noted earlier that heating in air invariably formed a blocking contact, whereas heating in nitrogen, an inert gas, yielded on occasions, although not predictably, an injecting contact.

A further test was carried out on a cadmium sulphide film which had undergone no post evaporation heat treatment, and had been placed in a desiccator between evaporations. A set of aluminium and gold electrodes was evaporated on to the film. Gold formed a blocking contact but aluminium produced the partially injecting contact shown in Figure 5.16 which revealed the saturation effect described earlier. The characteristic is symmetrical about the origin (zero volts). On applying a greater voltage, the characteristic in Figure 5.17 was obtained. The increase in current was not due to breakdown of the cadmium sulphide film, as reversing the polarity of the applied voltage still produced a saturation effect. The requirements for saturation brought about by electron-phonon interaction demand an unrealistically high mobility (200 cm^2/Volt.sec approximately) and moreover the saturation effect would not be expected to occur in one direction and not the other. This effect has been noted by Weimer [25] and related to an insulating layer between the injecting contact and the cadmium sulphide. The saturation effect is not always as pronounced as can be seen from Figure 5.18. In this case, the aluminium electrodes were evaporated on to a film which had been ion bombarded immediately beforehand.

Ion bombardment offers a simple method of obtaining a current injecting contact to cadmium sulphide. The mechanism of contact formation is not entirely clear and, if it is due mainly to a removal of the surface impurities on the cadmium sulphide, it may cause damage to the film with a corresponding increase in trap density. From the point of view of a stable active device, it would seem to be necessary to anneal out the damage.

I-V CHARACTERISTICS FOR ALUMINIUM ELECTRODES SHOWING CURRENT SATURATION

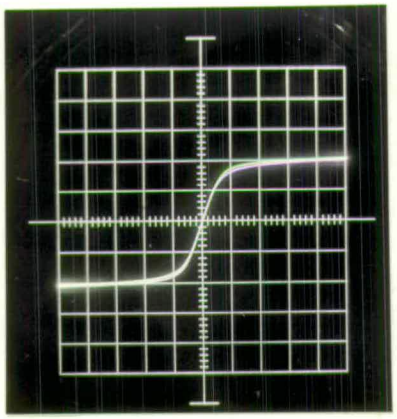


Fig. 5.16 Vertical 0.1 mA/div.
Horizontal 1.0 Volt/div.

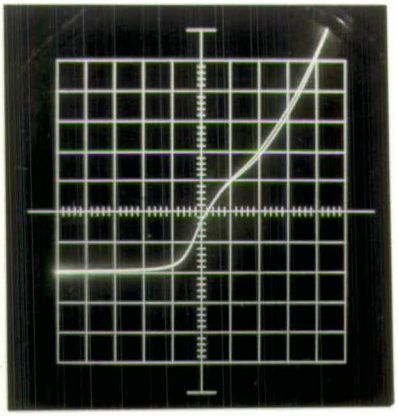


Fig. 5.17 Vertical 0.1 mA/div.
Horizontal 1.0 Volt/div.

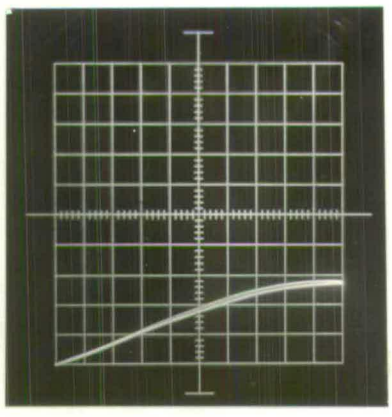


Fig. 5.18 Vertical 0.01 mA/div.
Horizontal 2.0 Volt/div.

CHAPTER 6.

EVAPORATION OF THIN FILM TRANSISTOR.

6.1 THE MASK CHANGER.

One of the main advantages of the coplanar thin film transistor lies in the prospect of evaporating all layers subsequent to the cadmium sulphide in one pump down of the vacuum system. To this end, a mask changer was contructed which permitted four mask changing operations and is shown in Figure 6.1. The jig on which the masks were aligned can be seen in this figure but a separate photograph illustrating the masks positioned on the jig is shown in Figure 5.4.

A scanning electron micrograph of a device fabricated using the above masks is shown in Figure 6.2, in which the source and drain electrodes, insulating layer and gate electrode can be clearly seen. Before discussing the characteristics of such a device, it is necessary to consider some of the difficulties associated with the evaporation of silicon monoxide.

6.2 EVAPORATION OF SILICON MONOXIDE.

Vacuum deposited silicon monoxide is one of the most commonly used dielectrics for thin film capacitors and is often combined with evaporated aluminium electrodes. It can easily be evaporated at temperatures between 1200^{o}C to 1300^{o}C. The dielectric and optical properties of the films are affected by

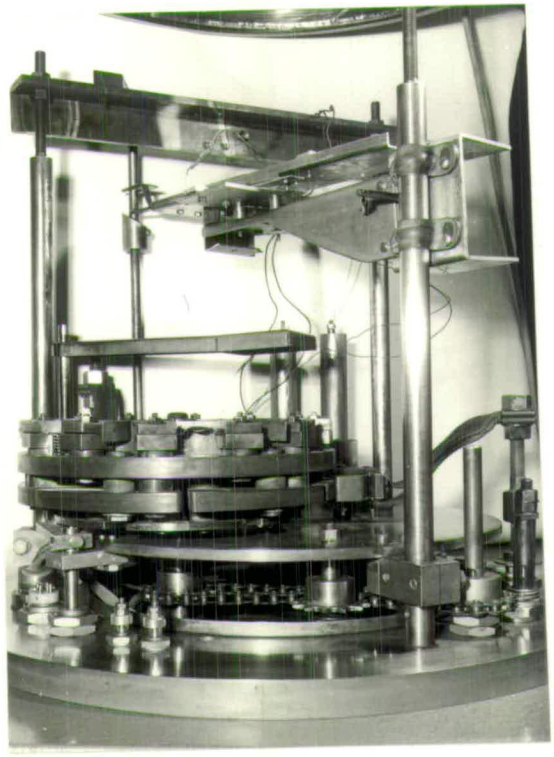


Fig. 6.1 Photograph depicting vacuum chamber with mask changer.

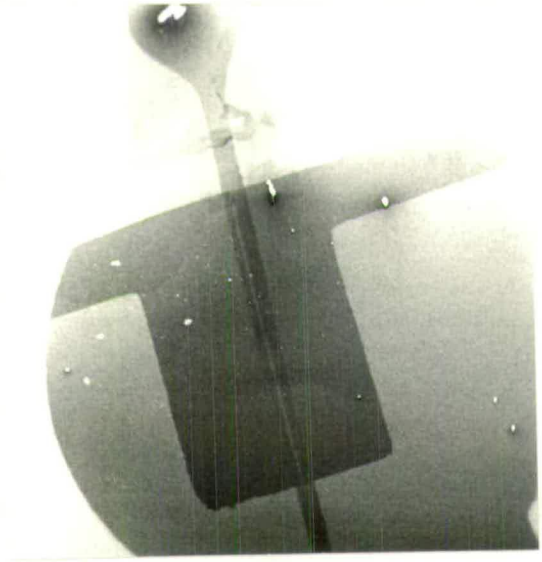


Fig. 6.2 Scanning electron micrograph of evaporated thin film transistor.

the deposition rate and the residual gases present in the vacuum chamber during deposition. When silicon monoxide is evaporated the resulting vapour comprises mainly single SiO molecules. Upon condensation, however, additional oxygen can be taken up if it is available with the result that the film can have any state of oxidation between SiO and SiO_2. The oxygen and water vapour content of the residual gases in the chamber are important constituents which do not readily allow the formation of reproducible films.

The properties of silicon oxide-aluminium capacitors have been reported by many workers including Siddall [79], Manfield [81] and more recently Hirose and Wada [82]. Siddall showed in his experimental work that thick films of silicon monoxide (10,000 Å) peeled or "crinkled" after exposure to the atmosphere. He also observed that this tendency was reduced if the films were annealed at 250°C during deposition. It was assumed that stresses were set up in the film during deposition and were reduced by the annealing. Novice [83] followed up this work by studying the effect of atmospheric exposure on the stress and showed that the water vapour content was a contributing factor. He also annealed the films at temperatures up to 300°C to remove stresses.

The initial evaporations of silicon monoxide followed the techniques evolved by Siddall and Novice. Generally the substrate was held at a temperature between 250°C and 300°C during evaporations and the baffle type tantalum boat used with cadmium sulphide was also used to evaporate powdered silicon monoxide obtained from the Kemet company. A cold trap was used and the pressure maintained at 10^{-5} torr. The evaporation rate varied between 1 Å/sec and 3 Å/sec. On rare occasions, the silicon monoxide crinkled on exposure to

the atmosphere but little trouble was experienced in this respect. The dielectric constant of the films was estimated to be 4.7 at 1.5kHz by making a thin film capacitor with aluminium electrodes. This value for the dielectric constant lies between that of silicon (11.6) and silicon dioxide (3.8), and shows that the film has reached some intermediate oxidation state. The film thickness was 2200 Å although showing some leakage capacitor breakdown did not occur at voltages less than 12 volts. When films of a similar thickness were evaporated, to form the gate insulator of a transistor, breakdown occurred frequently. This can be seen in Figure 6.3 which is a particularly severe case. In some cases transistor action was observed prior to breakdown but more often the insulator appeared to be faulty on removal from the evaporation chamber. Precautions were taken to minimize the amount of dust present which could cause breakdown (Figure 6.4) but no noticeable improvement was found. It was observed during the formation of the capacitor that the silicon monoxide surface was smooth whereas in a transistor it followed the topography of the cadmium sulphide surface. The Talysurf and electron micrographs had shown the surface of the latter to be rough with peaks of 500 Å to 1000 Å depending on the thickness of the film. It was felt that this roughness could contribute greatly to the breakdown of the silicon monoxide. This led to a further investigation of the cadmium sulphide evaporation procedure which has previously been described.

An immediate improvement was found using the smooth cadmium sulphide films and generally some form of transistor action was obtained provided ohmic source and drain contacts could be made. The transistors were characterized by a lack of saturation in the I-V characteristic.

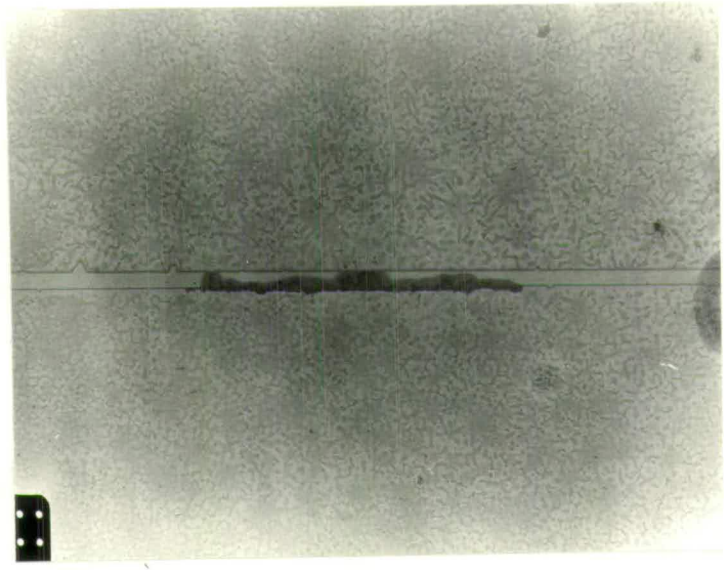


Fig. 6.3 Photograph of gap region showing breakdown (x 100)

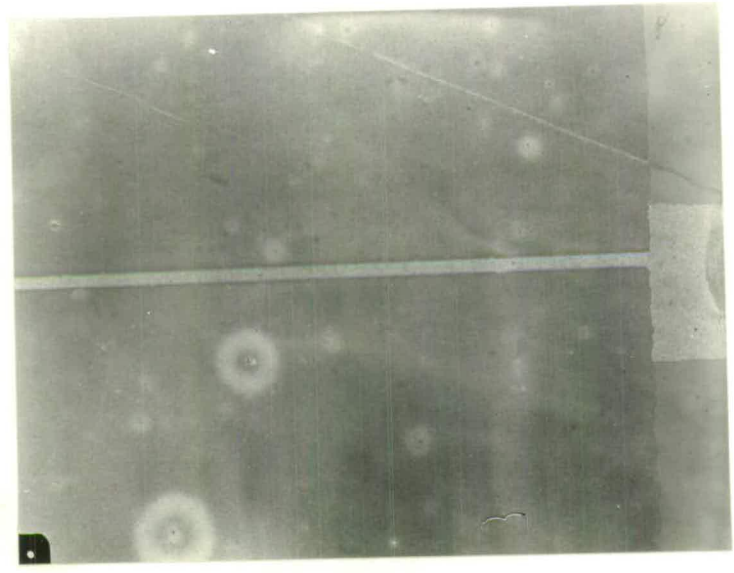


Fig. 6.4 Photograph of gap region showing pin holes due to dust (x 100).

Siddall also evaporated silicon monoxide at faster rates, up to 30 Å/sec, but found that such films had a lower dielectric strength. Using lumps of silicon monoxide, a rate approaching this value was attained with the tantalum baffle boat. The transistors made in this way showed improved current saturation.

During the early attempts to fabricate a transistor mis-alignment of the gate electrode and the source-drain gap occurred frequently. This was traced to differential expansion of the mild steel mask and the stainless steel jig during the substrate heating for the silicon monoxide deposition and was overcome by cutting the mask in half (Figure 5.4). It was realized that the different coefficients of expansion of cadmium sulphide and silicon monoxide could cause differential strains to be present in these films. In addition, at higher substrate temperatures there is an increased possibility of a chemical reaction occurring between the two materials. In the experimental work undertaken, although the better devices were formed without substrate heating, there is no conclusive evidence which suggests that the dielectric strength of the insulator is impaired by the substrate heating.

6.3 DISCUSSION OF TRANSISTOR I-V CHARACTERISTICS.

The importance of being able to make an injecting contact and to provide good insulation for the gate electrode in a thin film transistor is obvious. The evaluation of a more stable device as the above requirements are attained is described in the case histories below.

TFT 1-66 (Figure 6.5).

The cadmium sulphide received no post evaporation heat treatment. The source-drain electrodes - 12 microns apart - consisted of aluminium (1000 Å) with an underlay of indium. Silicon monoxide (1500 Å) was evaporated slowly (2 Å/sec). Breakdown of the insulator occurred when testing on Tektronix curve tracer at the voltages shown in Figure 6.5.

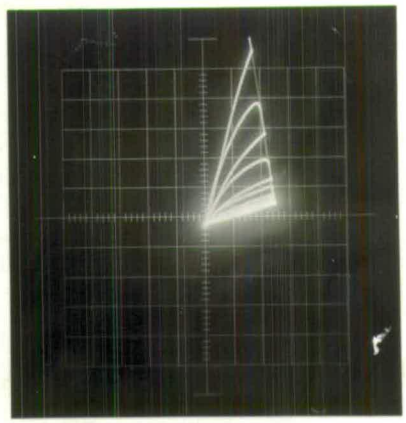


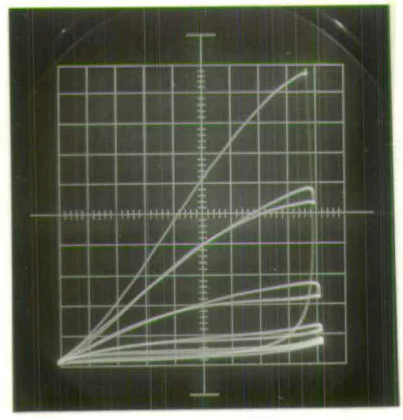
Fig.6.5

Vertical 0.1 mA/div.
Horizontal 1.0 Volt/div.
Gate 0.2 Volt/step.

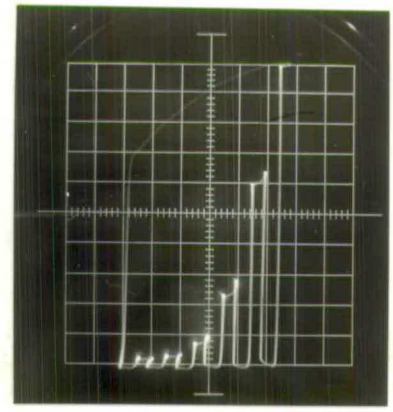
TFT 22-116 (Figures 6.6(a) and (b).

This was essentially a repetition of the evaporation procedure used for TFT 1-66. It was decided to increase the insulating layer to 2500 Å and decrease the aluminium source-drain electrode thickness to 500 Å in order to provide a

less rugged surface for the insulating film. Breakthrough also occurred although this was due to the accidental application of a high drain voltage, about 18 volts. This produced a field of 7×10^5 volts/cm across the silicon monoxide layer. The g_m of the device was 0.02 mA/volt at a gate vottage of 1.0 volt.



(a)



(b)

Fig. 6.6 Vertical 0.01 mA/div.
Horizontal 2.0 Volt/div.
Gate 0.2 Volt/step.

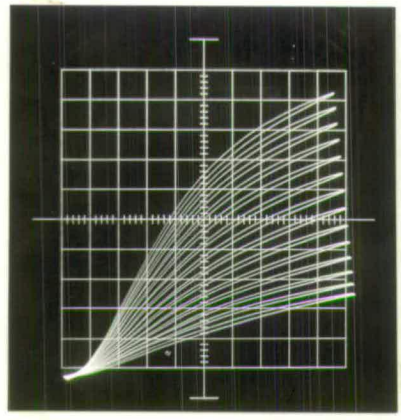
Vertical 0.01 mA/div.
Horizontal 0.2 Volt/div.

TFT 8-17 (Figures 6.7(a), (b)

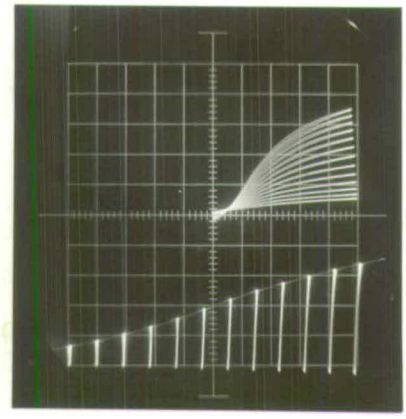
The evaporation procedure for TFT 22-116 was repeated. In the first instance, the gate was shorted to the source and drain showing poor insulation. A subsequent attempt resulted in a working device, TFT 8-17. Current flowed in the device at zero gate voltage. This was not the case with TFT 22-116 which required about 0.6 volts to turn it on. In addition, the drain current

does not saturate with increasing drain voltage. Both these conditions, the current flow at zero gate voltage and the lack of saturation, could be owing to a leaky insulator providing a shunt conduction path.

The other notable features are the "crowding" of the characteristic with increasing gate voltage and a diode type curvature at the origin. The saturation of the drain current with gate voltage can clearly be observed from Figure 6.7(b). This is due to current limiting, of the type discussed in the previous chapter, by the source electrode. Weimer considers that, if there is an insulating layer between the source contact and the cadmium sulphide, a pinch-off mechanism similar to that in a field effect transistor, can occur. Furthermore, a similar layer under the drain has the effect of placing



(a)



(b)

Fig. 6.7 Vertical 0.2 mA/div.
Horizontal 1.0 Volt/div.

Vertical 0.2 mA/div.
Horizontal (Top) 2.0 Volt/div.
Horizontal (Lower) 0.5 Volt/div

a diode in series with the transistor. No experimental investigation was undertaken in connection with these features of the characteristic.

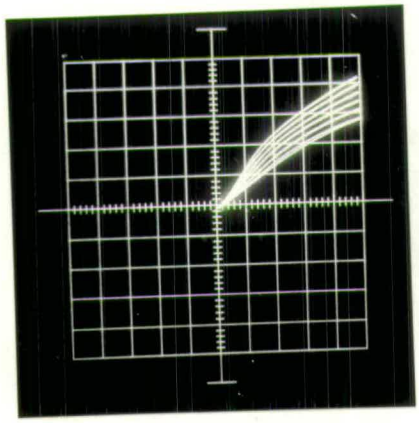
The g_m of the transistor at a gate voltage of 2.5 volts (before crowding begins) is 0.13 mA/volt.

All the devices discussed so far which were deposited on "rough" cadmium sulphide have shown a weakness in gate insulation and poor source-drain contacts. The use of smooth cadmium sulphide films increased the yield of working devices but in many cases a leaky insulator was still prevalent.

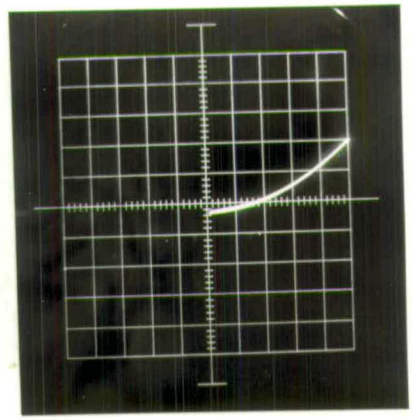
Consider the following cases.

TFT 20-27 (Figures 6.8(a), (b) and (c)).

This device was formed in the same manner as those described. The I-V characteristic did not saturate and there was pronounced leakage between the gate and source-drain electrodes (Figure 6.8(b)).



(a)



(b)

Fig. 6.8

Vertical	0.5 mA/div.		Vertical	0.01 mA/div.
Horizontal	2.0 Volt/div.		Horizontal	1.0 Volt/div.
Gate	1.0 Volt/step.			

The transistor was examined under a microscope and breakdown appeared to occur mainly along the edges of the gate electrode (Figure 6.8(c)). The area within the gate overlap was relatively free from pin holes suggesting that high fields at the electrode edges may initiate breakdown.

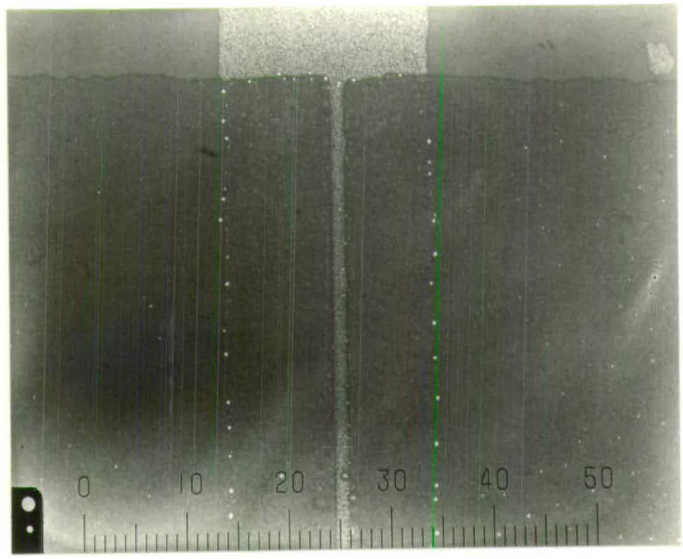
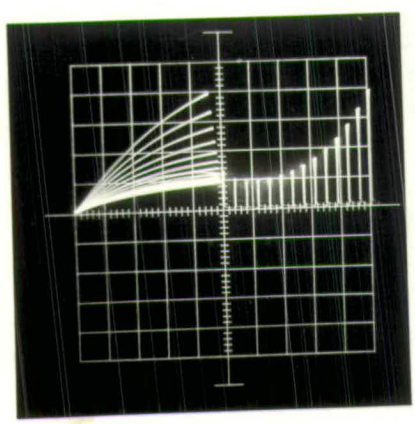


Fig.6.8(c) Photograph of insulator breakdown (x 100).

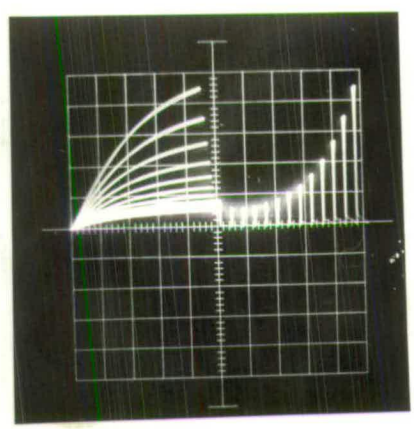
TFT 22-37 (Figures 6.9(a), (b), (c), (d) and (e)).

This transistor was not evaporated completely in one pump down of the vacuum system. Aluminium source-drain electrodes were evaporated on to a smooth post-evaporation heat treated cadmium sulphide film which had been ion bombarded beforehand. Good ohmic contacts were obtained. The substrate was replaced in the jig, the mask re-aligned and silicon monoxide evaporated at 30 Å/sec at a pressure of 10^{-4} torr, this being controlled by allowing air into the chamber through a needle valve. During the silicon monoxide evaporation the substrate was not heated. The aluminium gate electrode was evaporated during the same pump down.

The characteristic shown in Figure 6.9(a) was obtained. After some time, about 2 hours, this characteristic had altered to that in Figure 6.9(b). It was noticed that the characteristic was highly dependent on the number of voltage steps applied to the gate. This drift can be clearly seen in Figure 6.9(c). The complete device was annealed for 12 hours at 190°C in an atmosphere of nitrogen and a more stable characteristic resulted (Figure 6.9(d)). Little change occurred in this device over several months. Over the complete sequence of treatments, the transistor changed from an enrichment to a depletion mode of operation, indicating an instability originating in the insulator to semiconductor interface. At no stage was there any indication of "crowding" of the characteristic and it can probably be assumed that the injecting contact was good (Figure 6.9(e)). The g_m of the device at a gate voltage of 2.0 volts was 0.05 mA/volt and the effective mobility of the charge carriers was 3 cm^2/Volt.sec.



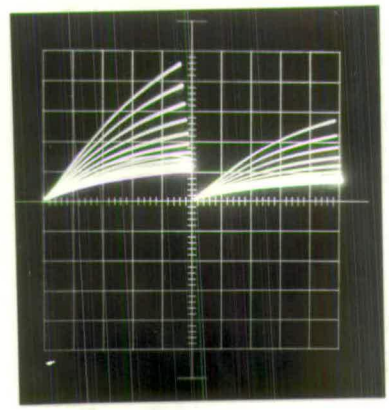
(a)



(b)

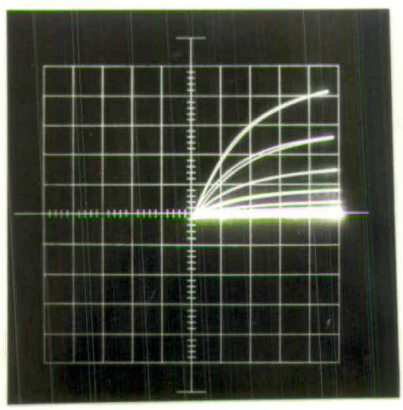
Fig. 6.9

Vertical	0.1 mA/div.		Vertical	0.05 mA/div.
Horizontal (L.H.S.)	1.0 Volt/div.		Horizontal (L.H.S.)	1.0 Volt/div.
Horizontal (R.H.S.)	0.5 Volt/div.		Horizontal (R.H.S.)	0.5 Volt/div.
Gate	0.2 Volt/step.		Gate	0.2 Volt/step.



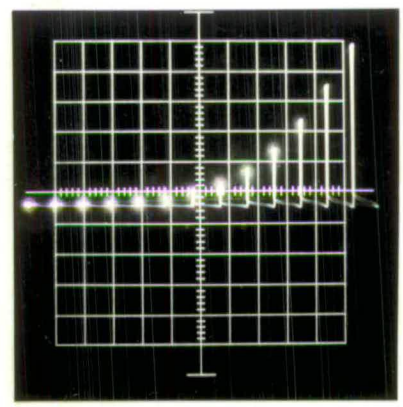
(c)

Vertical 0.1 mA/div.
Horizontal 1.0 Volt/div.
Gate 0.2 Volt/step.



(d)

Vertical 0.01 mA/div.
Horizontal 1.0 Volt/div.



(e)

Vertical 0.5 mA/div.
Horizontal 0.02 Volt/div.

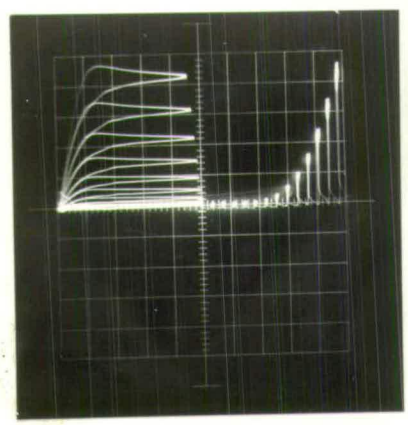
Figure 6.9

TFT 20-37 (Figures 6.10(a) and (b)).

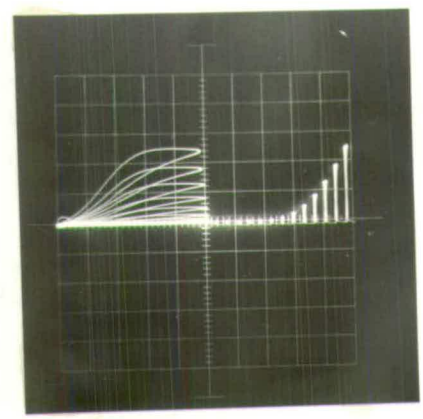
This device was fabricated in the same manner as TFT 22-37, except that the complete device was formed on the cadmium sulphide film in a single pump down of the vacuum system. Good current saturation occurred (Figure 6.10(a)) but in a short time, 20 minutes, the I-V characteristic had taken the form shown in Figure 6.10(b).

A pronounced hysteresis effect was present in the characteristic and can be attributed to the presence of trapping levels in the semiconductor-insulator interface.

The g_m of the device at a gate voltage of 1.2 volts was 0.1 mA/volt and the effective mobility of the charge carriers was 18 cm^2/Volt.sec.



(a)



(b)

Fig. 6.10

	Vertical	0.05 mA/div.
	Horizontal	1.0 Volt/div.
	Gate	0.2 Volt/step.

Vertical	0.05 mA/div.
Horizontal	1.0 Volt/div.
Gate	0.2 Volt/step.

Proceeding along the same lines as described and using ion bombardment to make ohmic contacts in each case, other working devices were fabricated. However, the characteristics were unpredictable and drifted rapidly. In some cases degradation took hours, in others, a few minutes.

CHAPTER 7.

CONCLUSIONS.

7.1 DISCUSSION OF RESULTS.

This report has encompassed several aspects of the thin film transistor. The initial approach towards fabrication of the device was to evaporate the required layers in a single pump-down of the vacuum chamber without a detailed investigation of the individual films beforehand. The mask changer was constructed for this purpose. It became obvious that this approach was too ambitious and that some study of the separate layers was required. In essence this thesis is a study of the materials from the device point of view.

The difficulties associated with the fabrication of a cadmium sulphide thin film transistor resolved themselves into two main categories.

The first of these concerned the metal to semiconductor contact. The Schottky model is normally used as a theoretical foundation on which the selection of materials to give an injecting or blocking contact is based. However, in practice it is difficult, if not impossible, to obtain the ideal conditions on which the theory is based. The experimental work on contacts to cadmium sulphide has shown this to be the case. It was generally not possible to obtain an ohmic contact using aluminium or indium without ion bombardment of the cadmium sulphide surface. This was particularly true in the case of cadmium sulphide which had been heat treated in air and work function measurements have ~~been~~ shown that some form of compensation takes place on

heating, the film becoming less n-type. It is possible that cadmium oxide forms at the surface.

In addition to the alteration of the composition at the surface by heat treatment, it is necessary to consider the formation of aluminium oxide during the contact evaporation process. The factors leading to the formation of aluminium oxide are

(a) the gettering action of the aluminium during evaporation

and

(b) the adsorption on the cadmium sulphide surface of gas molecules normally present in the atmosphere, the most important being oxygen and water vapour.

It is possible that by removing one of these sources of contamination a good ohmic contact could be obtained. It could be argued that ion bombardment does this and simply removes the surface of the cadmium sulphide. However, gold then forms an ohmic contact and this is difficult to explain on the basis of the Schottky barrier model. It would be preferable to avoid the use of ion bombardment and instead try to eliminate the contamination of the aluminium during evaporation by using a system of cold traps placed near the evaporation region of the chamber.

The second category concerns the gate insulation. The early attempts at forming a thin film transistor generally failed owing to, in part, breakdown of the silicon monoxide layer. The roughness of the underlying cadmium sulphide film proved to be a contributing factor. In addition, it is thought that heating the substrate to the rather high temperature of 300°C may have caused a chemical action or diffusion of constituents to occur during the silicon .

monoxide evaporation, with a consequent reduction in the dielectric strength of the insulator. No attempt was made to isolate these two factors but it may be significant that the transistors which exhibited the best I-V characteristics, TFT 20-37 and TFT 22-37, were fabricated without heating the substrate.

The most notable feature of the few working devices obtained with good characteristics was their lack of stability. TFT 20-37 (Figure 6.10(a)) showed a sharp degradation with time (about 20 minutes) with a corresponding deterioration in g_m. In such cases, it is possible that ion migration occurring within the insulating layer and producing an intrinsic electric field, contributes to the change in g_m. Pronounced hysteresis loops are also present in the characteristic of this device, as mentioned previously. This is an effect about which little is known and although an attempt may be made to attribute the effect to trapping levels in the semiconductor to insulator interface, there is no experimental evidence to substantiate this suggestion. TFT 23-37 (Figure 6.9) showed considerable variation of the characteristic with time, although at a much slower rate than TFT 20-37. In this case the characteristic eventually settled to a stable state. An obvious instability of the characteristic with variations in gate bias is present (Figure 6.9(c)). It is obvious that a variation of this kind in the characteristic would make the device difficult to use from a circuit design point of view. These are a few of the more obvious instabilities which plague the thin film transistor and their origin probably lies in the silicon monoxide insulating film or at the interface formed with the cadmium sulphide. In order to make a constructive study of such phenomena a batch formation process would be necessary for the devices.

The values obtained for the work function of the cadmium sulphide films, using apparatus constructed by J. Mitchinson of this department have some agreement with the values obtained by Scheer and Van Laar [71] for the top of the valence band and the electron affinity of single crystalline cadmium sulphide. They have reported the top of the valence band to be 7.0eV below vacuum level and, therefore, for intrinsic material with a band gap of 2.5eV the work function is 5.75eV. The largest value obtained, 5.05eV for cadmium sulphide heated in air, is in agreement with the above figure if one considers the film to be n-type as is normally the case.

Shuba[71] has estimated the top of the valence band to be 5.7eV below vacuum level for cadmium sulphide films and in this case, if the band gap is 2.5eV, the work function for intrinsic material is 4.45eV. On this basis, our films would be p-type, and it is suggested that Shuba's value for the top of the valence band may be low.

7.2 CONCLUSION.

The stable operation of the thin film transistor is heavily dependent on an understanding of interfaces between different materials. The MOST, while it also has a semiconductor to insulator interface, avoids the contact problem by using diffused p-n junctions. Vacuum evaporation of materialsdoes not offer control over impurity content to the same extent as is possible in silicon semiconductor integrated circuit technology. Consequently, whether the fabrication of the stable thin film transistor can be achieved will depend on the understanding and control of the interfaces between surfaces. Careful control of the evaporation processes will be necessary.

In particular, if the above problems could be solved, the polycrystalline cadmium sulphide device would still suffer from the low mobility of the charge carriers. This could possibly be improved by using epitaxial films which, as was shown in Chapter 3, can be grown on mica. As an alternative, the frequency response of the device could be increased by reducing the source to drain spacing. This reduction is limited if out of contact masking is employed. Hence, the use of semiconductors, preferably elemental to avoid problems in stoichiometry, with a higher intrinsic mobility would be advantageous.

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