Integrated Interface Circuits For Switched Capacitor Sensors

by

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Abstract

This thesis reports an investigation into integrated interface circuits for switched capacitor sensors for application in industrial process control instrumentation networks.

Three circuits are presented: an absolute capacitance to voltage converter; a capacitance ratio to frequency ratio converter; and a capacitance ratio to voltage ratio converter. Of the circuits, the first two are subject to most thorough investigation with the capacitance ratio to frequency ratio converter being of particular interest. This circuit is based upon a switched capacitor, frequency controlled, negative feedback loop which permits implementation with modest quality analogue components, such as are provided with a standard-cell ASIC CMOS process.

Initial investigations, accomplished with discrete component implementations of the interface circuits, reveal a significant departure in behaviour from that predicted by first-order analysis. Switch induced charge-feedthrough is shown to be responsible for the deviation. In addition, parasitic induced jitter and frequency locking are identified as a second source of error.

The three interface circuits are implemented as an integrated circuit using the European Silicon Structures (ES2) ASIC CMOS process, with a modification to permit the inclusion of full-custom designed, charge-feedthrough compensated switches. This implementation exhibits greatly reduced charge-feedthrough, and circuit behaviour is in accordance with a modification to the first-order analysis that includes the effects of charge-feedthrough. Importantly, no frequency locking and much reduced jitter is observed. Significantly, linear performance is obtained for the capacitance ratio to frequency ratio converter over a 20 to 1 capacitance range, with operation demonstrable down to 5pF sensor capacitance.

Declaration

This thesis, composed entirely by myself, reports work carried out solely by myself in the Department of Electrical Engineering, University of Edinburgh between October 1987 and September 1990.

Acknowledgements

I am grateful to my supervisors, Prof. J.R.Jordan and Dr. D.Renshaw, for their unsparing support and guidance during the course of this work. I would also like to thank the other members of the Instrumentation and Digital Systems Group, namely Mr. S.Lytollis, Dr. I.M.Flanagan and Dr. K.Sylvan, for invaluable conversations and assistance, and acknowledge the able technical support of Mr. R.Stevenson. Mr. A.M.Gundlach of the Edinburgh Microfabrication Facility and Dr. G.M.Blair merit acknowledgement for their assistance with the EMF and ES2 IC designs.

Finally, I wish to thank my parents for their unfailing encouragement and support over the years.

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Index of Abbreviations

ADC	Analogue-to-Digital Converter	IS	Intrinsic Safety
ASIC	Application Specific Integrated Circuit	MSB	Most Significant Bit
CAD	Computer Aided Design	NMOS	N-type
CMOS	Complementary Metal Oxide Semiconductor	PMOS	P-type Metal Oxide Semiconductor
CRO	Cathode Ray Oscilloscope	RTD	Resistive Temperature Device
DAC	Digital-to-Analogue Converter	SAR	Successive Approximation Register
ES2	European Silicon Structures	SC	Switched-Capacitor
IC	Integrated Circuit	VCO	Voltage Controlled Oscillator

List of Symbols

C_{GD}	Gate-drain overlap capacitance (Fm^{-1})	U	Gate voltage falling-rate (Vs^{-1})
C_{GS}	Gate-source overlap capacitance (Fm^{-1})	W	Channel width (m)
C_{OX}	Oxide capacitance (Fm^{-2})	β	Conductance coefficient (AV^{-2})
L	Channel length (m)	ϵ	Permittivity (Fm^{-1})
q_{dm}	Feedthrough charge (C)	k	Boltzmann's constant (JK^{-1})
R_{ON}	MOS on-resistance (Ω)	μ	Carrier mobility ($m^2V^{-1}s^{-1}$)
T_o	Channel transit time (s)	q	Charge on an electron (C)
v_{dm}	Feedthrough voltage (V)	N_{SUB}	Dopant density (m^{-3})
V_G	Gate voltage (V)	n_i	Intrinsic carrier concentration (m^{-3})
V_H	Gate high voltage (V)	γ	Body effect parameter ($V^{\frac{1}{2}}$)
V_L	Gate low voltage (V)	Φ_f	Fermi potential (V)
V_T	Threshold voltage (V)	$V_{HT} = V_H - V_S - V_T$	

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Chapter 1
Pressure Sensing and Industrial Process Control: An Overview

1.1 Introduction

This thesis describes research into integrated Fieldbus interface circuits for switched capacitor sensors undertaken in collaboration with ABB Kent-Taylor. The work is part of a wider research effort by the Instrumentation and Digital Systems Group of the Department of Electrical Engineering, Edinburgh University, into electronic instrumentation for process industry applications.

Before defining the scope and primary objectives of the work presented here and stating the layout of the thesis, an overview of existing process control systems is given and their limitations identified. Recent developments, which attempt to address these problems, are discussed in the following section. Finally pressure measurement is reviewed with an emphasis on capacitive techniques.

1.2 Present Process Control Systems

The term industrial process control describes the automatic regulation of manufacturing processes. Process industries include such diverse interests as oil, chemicals, electrical power, pulp and paper, mining, metals, cement, pharmaceuticals, foods and beverages [1-3].

The origins of process control can be traced to the early part of the century from the inception of on-off control in the mid-1920s to the widespread use of proportional control by the end of the decade. The early control systems were "open loop" and

relied wholly on manual intervention. As the operations within process industries became more complex the demands on the operator increased, making uniformity of quality harder to achieve. The requirement for improved quality necessitated the incorporation of closed loop control (to reduce dependence on manual control) and the application of electronic instrumentation. By the start of the nineteen-fifties process control systems had evolved into a form that remains recognisable in contemporary systems. The control system was modularised in terms of sensors, transducers, regulators, actuators and recorders. Conventions for signal transmission were adopted that simplified design, installation, operation and maintenance and permitted the combining of equipment from different manufacturers. An example of this is the 4-20mA standard for electrical signal transmission; this remains in use to the present day [4]. Centralised control came into being since the distribution of control centres throughout a process plant was deemed to be uneconomic. However, the wide-spread adoption of serial data highway techniques, as seems likely by the year 2000, will probably lead to a return to the redistribution of control functions to measurement and actuator sites.

Digital computers were increasingly used from the nineteen-fifties through to the nineteen-seventies as the benefits of computer-controlled systems were realised [1, 2, 5]. At the outset, computers, on account of their unreliability and cost were used in supervisory tasks, while analogue controllers continued to be used for the primary control functions. Latterly, analogue technology was completely replaced by digital technology; the term *direct digital control* was coined to emphasise that the computer controlled the process directly.

Process control practices that typically are employed today are illustrated in *Fig.* 1 [6]. Each field device, a sensor or actuator, is connected to a single pair of wires that are then run to a controller or a data-acquisition device. Structural variations from one control system to another can be considerable, but most are based upon this simple model.

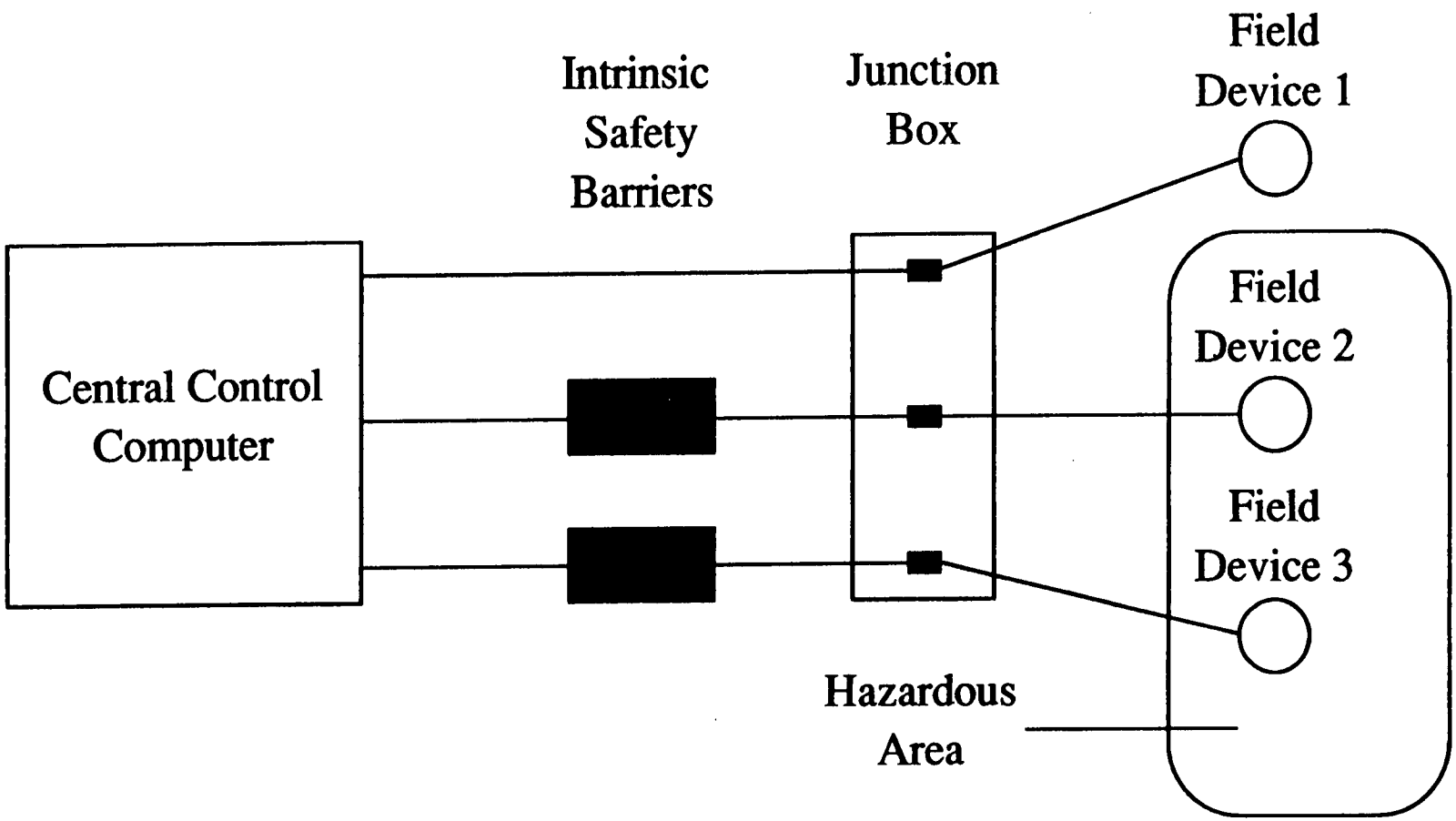


Figure 1: A star connected industrial process control instrumentation network

The development of process control, summarised above, has been driven by a variety of incentives that continue to exert influence and are rapidly rendering the above type of process control system obsolete. The incentives for investment in process control are: cost reduction, improvements in quality and reliability, more economic use of energy and raw materials, increased production, improved reporting, ease of use, simplicity of fault tracing, and safety [1,7,8]. Over the last decade academic and industrial sectors have been pursuing many research areas in common; this is in stark contrast with the previous four decades [9]. Research areas of note are: sensor development; digital computer control; and fault detection and reliability. Edgar [9] has suggested that the increase in interest and commitment has been fuelled by a greater emphasis on productivity and efficiency, and by the availability of inexpensive computer hardware. Smart sensors that are self-calibrating and self-checking for example, are identified as being a high priority as are sensors with an accuracy better than 0.1% [10]. Morris [7] has claimed that the proportion spent on instrumentation is rising as a percentage of the total costs of processing plant as a consequence of the above stated incentives.

The inclusion of technological improvements into, and the resultant complexity of the essentially primitive system, shown in *Fig.* 1, can create problems and prevent the potential advantages from being realised. A considerable cost saving could be made for example, by reducing the number of wire-pairs between field device and controller. The full potential of distributed control, identified by Medlock [8] and afforded by the advent of the microprocessor and advances in communications technology, cannot be realised readily with this system [2]. For example, communications among the central controller and other distributed control centres is not easily implemented. Moreover, the contribution of local autonomy to system integrity, fault tolerance, and fault recovery, claimed by Brignell [11], cannot be realised. Pauly [5] has suggested that the disadvantages of interconnection of Programmable Logic Control (PLC) functions and instrumentation in distributed control systems could be avoided by allowing them

to communicate via the same highway.

Safety is an important consideration that constrains the design of a process control system [12]. All or part of the control system may be subject to Intrinsic Safety (IS) limits if the wiring runs through hazardous areas, and intrinsic safety barriers, shown schematically in *Fig.* 1, are required to limit the energy within these areas. A severe power budget may consequently be imposed on the wiring and instrumentation. Towie [13] and Hutcheon [14] have published histories of the development of Intrinsic Safety (IS) regulation in which the implications for process control system design are discussed.

In conclusion, if recent innovations are to be incorporated and present shortcomings resolved the design of process control instrumentation must be considered from a systems perspective.

1.3 Recent Developments in Process Control

The international fieldbus initiative is an example of a whole system approach and is an attempt to adopt an all embracing communications protocol for process control [15]. A fieldbus is a real-time serial digital data link connecting controllers, actuators, sensors and similar devices allowing for the frequent exchange of data amongst the devices [12, 16]. Data can be measurement information, control messages or alarms. A typical process control system based upon a fieldbus-type network is illustrated in *Fig.* 2.

The use of such a system has many benefits. The cabling cost of the control system in *Fig.* 1, is reduced [2, 4]. The digital data transmission system is more robust than the analogue 4-20mA system presently in use [17], an important factor in the adverse electromagnetic environment of many process plants. Communications can be structured to reflect the needs of the process and ease the distribution of control and

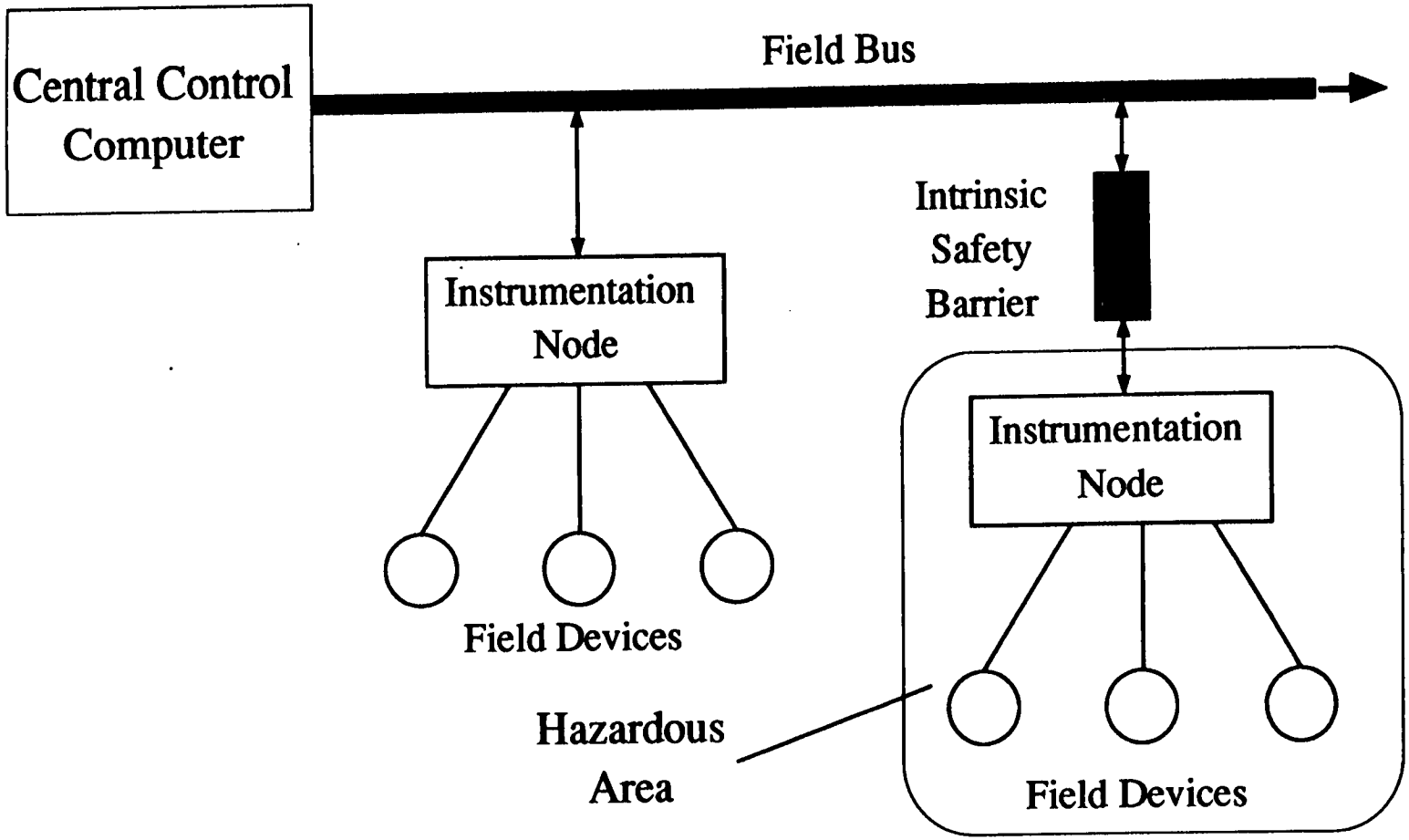


Figure 2: A representation of a field-bus type network

equipment [2, 6].

Pimental [16], McClelland [15] and Burton [12] have all reported great interest in fieldbus, with Ingrey [2] recording the emergence of a number of proprietary fieldbus systems. The Hart Smart Communications Protocol, marketed by Rosemount Ltd., is an example of such a proprietary bus system [15]. However, the difficulty is not only technological but also lies in making communication possible among diverse products built to different standards so that the whole can operate together as an integrated system [16]. At present there is no international standard that can meet both this criterion and all the information needs throughout a process plant. The adoption of a multi-vendor non-proprietary network by the process industries could provide the solution [6]. Standards committees and industrial collaborative groups are currently reviewing fieldbus options on a world-wide basis to this end [6, 12, 15].

The use of a fieldbus-type network, shown in *Fig.* 2, has implications for the design of sensors employed at an instrumentation node. In fact some form of intelligence is required at the node if distributed control is to be implemented. Medlock [8] has published a review of transducers, instruments and measurements in process control. This broad-based publication comprises a brief history of the subject in addition to sections on sensor classification, the current position, recent developments and future trends. In this last section the smart sensor, in conjunction with a fieldbus network, is identified as a key component in the movement towards distributed control. The importance of smart sensors to the development of advanced process control systems has been noted by other authors [9, 18]. A complete field-mountable measurement system is commonly called a transmitter. *Fig.* 3 illustrates a typical smart transmitter.

The smart sensor has many advantages when used with a fieldbus-type network. Addressable sensors can be interrogated and programmed remotely and can be made to talk to each other. For example information from a neighbouring sensor, say

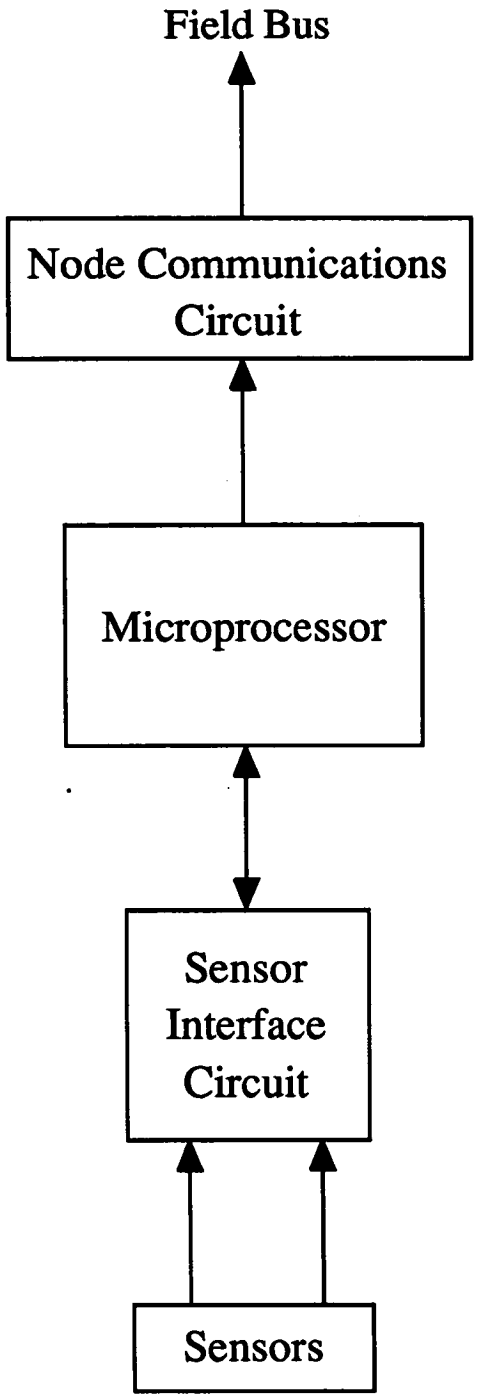


Figure 3: A typical smart sensor

temperature, could be used to modify a sensor's own output to solve a cross-sensitivity problem [11]. Enhanced sensors are needed to realise the full benefits of distributed control and processing. The presence of microprocessor and signal processing circuitry in a smart sensor permits the implementation of self-test and calibration features. Transducer compensation, e.g. linearisation, offset adjustment and filtering, can also be achieved at the sensor site [4, 11, 17, 19]. Brignell [11] has observed that sensor compensation should be carried out at the sensor node since it avoids loading the system processor, degrading system performance and making control program maintenance difficult when other sensors are added. In addition, uncompensated features, such as drift, may take up some of the usable dynamic range. Most importantly the distribution of processing around the network helps to modularise a potentially large and complex system thus containing problems and facilitating maintenance.

The presence of digital circuitry in a smart sensor and the digital protocol of fieldbus places fresh emphasis on frequency output sensors and interface circuits that can convert an analogue variable into a frequency output or digital word.

There are a few smart sensors already on the market. The Philips PDL 1000 system has field mounted analogue-to-digital converters that can process signals directly from up to eight sensors of the same type [4]. The converters are connected together on a ring bus and have a separate power supply. The Honeywell ST 3000 smart pressure transmitter is an example of an enhanced sensor capable of 0.1% accuracy, although it does not have, as yet, the capability for bus-type communications, and measurement information is transmitted as a 4-20mA signal [4, 19]. McClelland [18] has stated that smart sensor interest is growing fast and predicts a doubling of sales of smart transmitters by 1993 from a 1988 European base of $164 million; furthermore it is suggested that manufacturers that do not provide intelligent instrumentation may lose their share of the market.

The development of a smart sensor is subject to two important constraints: Intrinsic Safety and cost reduction. Intrinsic Safety (IS) considerations limit the power available within a hazardous area and thus run contrary to the demand for increased complexity at the node. For example, IS imposes a limit of four sensors of the type currently used with the 4-20mA standard when they are employed in a fieldbus-type system [6]. Hence low power sensors are required if a fieldbus system is to be effective. The low power requirement is somewhat mitigated by the low polling rate of instrumentation nodes in a process control network, being typically of the order of 100mS [10]. Recent developments in CMOS IC design and process technology have demonstrated that both analogue and digital circuits can be fabricated on the same substrate with a performance that is superior in certain respects to that obtainable from other technologies. Power consumption is low and a high density of both analogue and digital components can be achieved [20, 21]. This latter feature is important if complex smart transmitter circuits are to be implemented without recourse to a more costly multi-IC solution with the concomitant, highly power dissipative IC interface buffers. Such a single-IC solution is more commonly known as an Application Specific Integrated Circuit (ASIC) [22]. *Figs.* 4(*a*) and (*b*) show the multi-IC option and the preferred single-ASIC solution respectively. The single-ASIC ideally comprises all the node functions, communications, computer and sensor interface circuitry, with the exception of the sensor element. However, the inclusion of these functions may result in a large and costly IC.

The second constraint, cost reduction, was identified as a fundamental incentive for investment in process control in §1.2. Brignell [17] has stated that there is some market resistance to the smart sensor as a result of compartmentalised thinking despite the savings accrued at a system level. Therefore if a smart sensor is to be marketed successfully the additional intelligent functions should be provided for as small a cost overhead as possible.

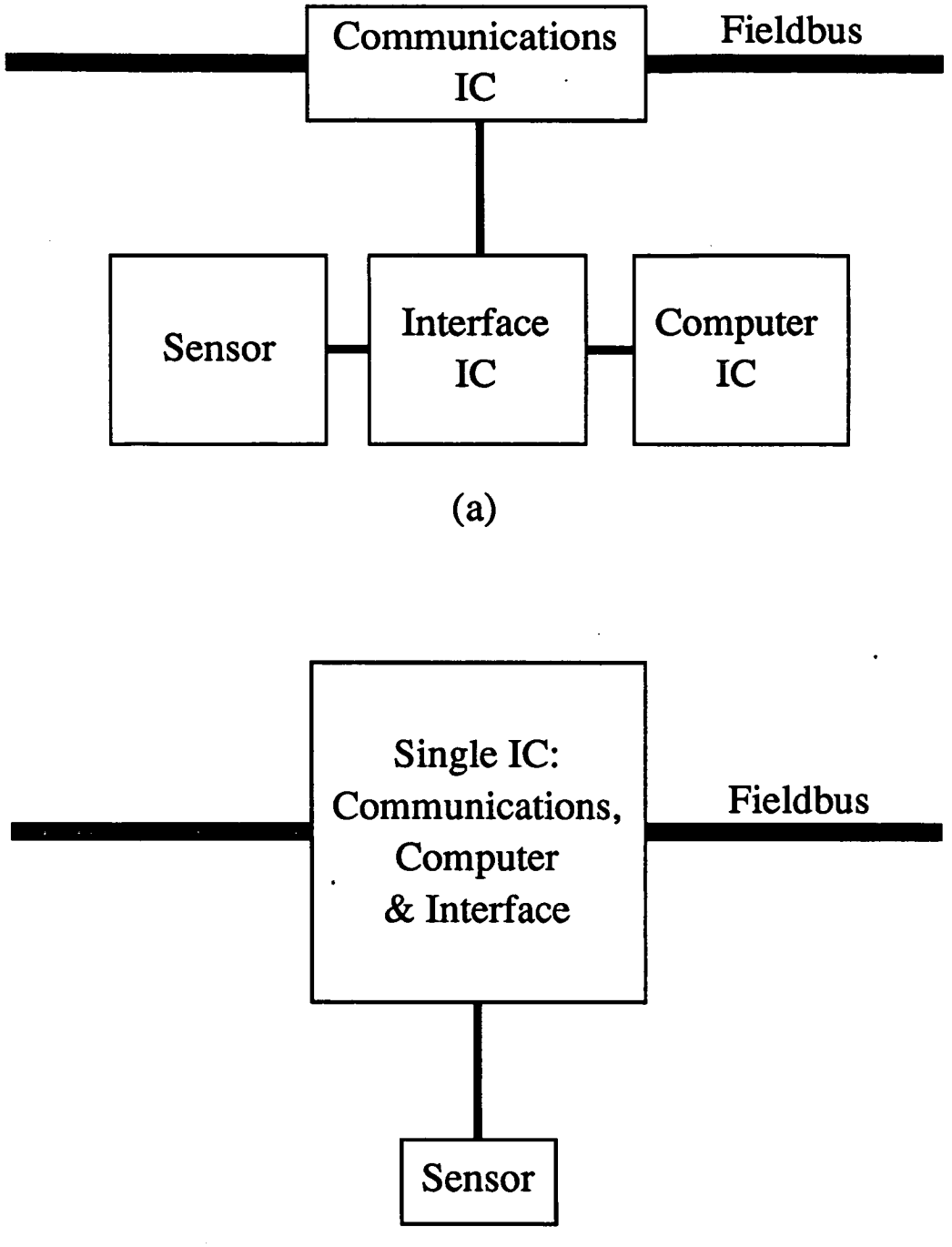


Figure 4: Two contrasting options for integration, **(a)** the multi-IC option and **(b)** the preferred single-IC option

The two available options for the production of a CMOS smart transmitter ASIC combining analogue and digital circuitry are *full-custom design* and *standard−cell design* [20]. The standard-cell option has certain cost advantages over full-custom design that are of particular relevance to the research reported in this thesis. Fey and Paraskevopoulos [22] have found the standard-cell approach to be more cost effective than full-custom design at lower levels of production and high gate density. Typically a 12,000 gate standard-cell design running to 1K units over a four year production period costs nearly a third of an equivalent full-custom design, with the cost benefits reducing significantly as production rises to 10K units. Full-custom design gains a small cost advantage somewhere between 10K and 100K units of production. The major gain of the standard-cell approach is made primarily in IC-development costs at low volume production. Considering that a complex, i.e. high gate density, design with lower production volume is envisaged for a smart transmitter IC, the standard-cell approach offers the lower cost solution. Moreover, the design cycle time for the full-custom approach can be excessive [20] making it unsuitable for the production of the integrated interface circuits within the lifetime and resources of short or small scale projects. The full-custom route was explored initially as part of this project but abandoned for the above reasons. Some relevant features of this work are reported in *Chapter* 5 and detailed in *Appendix B*, *p* 185.

The compromise inherent in the choice of standard-cell design is a reduction in the performance of the analogue components [20]. The performance reduction is evident from an inspection of the analogue cell-library of the European Silicon Structures Solo 1200 process, which was used for the fabrication of the interface circuits reported here, and is characterised by the provision of an 8-bit ADC and DAC [23]. Thus circuit techniques are required that can overcome this disadvantage so as to facilitate the design of interface circuits that can still achieve the industrially specified 0.1% accuracy but with limited accuracy components.

Research into electronic instrumentation systems for process industry applications has been active in the Instrumentation and Digital Systems Group at the Department of Electrical Engineering, Edinburgh University, for several years. Gater [10] published a thesis describing the development of a battery-powered fault-tolerant communications network for use in distributed measurement systems. The design incorporated a specially designed CMOS communications IC, and communication was via fibre-optic cables for IS compliance. This network was later improved upon with the addition of features desired of intelligent instrumentation [24]. These included self-test functions, alarms and inputs for frequency output sensors. Another thesis reporting the design of hardware for a fieldbus system is currently under preparation [25]. The hardware is based on the MIL-STD-1553B protocol and has been implemented as a single low power IC that incorporates all the communications functions. Other research has included the assessment of IS implications for fieldbus systems [26, 27]. Investigations within the research group have demonstrated that the maximum intrinsically safe power budget for sensor interface circuitry is dependent on several factors. IS considerations impose a limit on the total power consumption of a bus system and the power consumption of a node as a proportion of that of the bus as a whole constrains both the number of nodes supportable by the bus system and the utility, and therefore complexity, of each node. Each node is composed in its simplest form of a sensor, an interface circuit and communications circuitry. Assuming the sensor power requirements to be negligible, those of the communications circuitry, which can be considered to be performing an essential function, leave a maximum power budget for the sensor interface circuitry. Calculation of a maximum power budget for the sensor interface circuitry is further complicated by the variable requirements of the communications circuitry, which are dependent on bus utilisation and supply voltage levels [28]. Operation of the MIL-STD-1553 protocol communications IC, for example from a 5 volt supply and with 5% bus utilisation has a power requirement of 17.5mW. Increasing bus utilisation to 50% increases the power consumption to 35.3mW. Other work has

demonstrated that IS constraints permit up to three nodes, each with a power consumption of 40mW, to be connected to a bus of length 2000m [29]. Hence, assuming a typical process control bus utilisation to be 5%, a figure of 22.5mW remains for operation of the sensor interface circuitry. A lower power consumption would permit more than three nodes to connected to the bus and/or greater complexity at each node.

In summary, the development of interface circuits for process control is subject to the influence of many factors including the present international fieldbus initiative, the smart sensor, intrinsic safety and cost. A variety of design criteria and constraints arise from these factors: interface circuits with digital output; a slow rate of data-acquisition; high accuracy and the desire for a low power low cost single-IC smart transmitter.

Before the project objectives are stated an overview of pressure measurement in process control will be given to assist in defining the design criteria more clearly.

1.4 Pressure Measurement

Pressure in liquids and gases can be measured by a variety of mechano-electric transducers. These include variable resistance devices, such as rheostats, potentiometers and strain gauges that convert linear or rotary motion to an electrical output; variable inductance devices, such as the differential transformer and the variable-reluctance bridge; and capacitance-type pressure transducers [30, 31]. This last sensor type belongs to a group of transducers that can be fabricated by silicon IC technology, i.e. the intelligent sensor defined in §1.3, as well as functioning as discrete devices. Other transducers in this category are quartz and silicon resonating structures, surface acoustic wave (SAW) resonator sensors, piezoresistive transducers and FET-based sensors [32, 33].

Variable capacitance transducers have a number of advantages over the more commonly used variable resistance and inductance-type devices [34]. Some of these

advantages are: a large fractional capacitance change; almost non-existent hysteresis error; and high dynamic response. The ruggedness and the ability of capacitance transducers to withstand extreme environmental conditions makes them suited to industrial process applications. Several comparative studies are agreed on the issue that integrated capacitive sensors have greater potential than their piezoresistive counterparts as regards sensitivity, temperature behaviour, stability and power consumption [35].

Pressure can be measured in one of three ways: as absolute, gauge or differential pressure [30]. Absolute pressure is measured with reference to zero pressure; gauge pressure is measured with reference to ambient pressure; and differential pressure transducers measure the difference between two pressures. Differential pressure transducers can also be applied to flow and level sensing, and the measurement of specific gravity and temperature fluctuations [36]. A typical variable capacitance pressure sensor operates as follows. An isolating diaphragm protects the sensor from contact with the process being monitored and the sensor is connected to the process piping so that the process pressure is exerted against the diaphragm. The deformation of the diaphragm under pressure variation is hydraulically conveyed to the capacitive element via the intermediate fill-fluid. Differential pressure sensors operate on the same basis, with diaphragm(s) linked to two or four capacitors. The capacitors usually have an absolute capacitance in the range 20-70pF [10]. This thesis concentrates on interface circuits for the two capacitance sensor, where capacitance ratio is linearly related to differential pressure, a particular interest of the collaborating industrial organisation ABB Kent-Taylor. Gauge pressure measurement can be considered to be a special case of differential pressure measurement where, rather than two varying sensor capacitances, the sensor consists of one varying capacitance and one reference capacitance that remains fixed at ambient pressure.

The use of capacitance sensors is, unfortunately, beset by one principal difficulty: the value of the capacitance and the magnitude of variation is usually small

[34, 35, 37]. Typically, the full-scale capacitance ratio variation is 10% to 15% of zero scale for the capacitance ratio type of sensor, and the absolute capacitance size is in the range 20-70pF [10]. Insensitivity to parasitic capacitance is therefore a necessity if a resolution of 0.1% is to be achieved, and can be gained by the use of a parasitic-insensitive interface circuit. In addition, the parasitic capacitance can be reduced by situating the interface circuit very close to the sensor. This latter solution is made feasible by the use of IC technology. Moreover, the use of capacitance ratio rather than direct capacitance measurements reduces the effects of parasitic and environmental effects [38]. Puers *et al.* [35] have proposed a capacitive pressure sensor in silicon combined with a dedicated CMOS interface circuit as a solution to this difficulty. This approach was not attempted for several reasons. Firstly, the difference in the processing steps for fabrication of the sensor and of the circuitry makes integration on a single IC difficult, requiring a process more sophisticated than that provided for full-custom design, described in §1.3 above. As a result the processing requirements of integrated capacitive sensors even further exceed the capabilities of the standard-cell approach intended for this work. Secondly, the development of an ASIC interface circuit for off-IC capacitive sensors would permit its more immediate employment in an industrial process control system with the non-integrated sensors already in use. Finally, integrated capacitive sensors are not, as yet, widely used and confronting the considerable problems of coupling an integrated capacitive pressure sensor to a fabrication process was considered to be outside the scope of this thesis. Accordingly, the investigation was restricted to integrated interface circuits for non-integrated capacitive pressure sensors.

There are three basic techniques that can be used to convert capacitance variation to some corresponding digital or analogue electrical form:

- Amplitude modulation schemes, where the system consists of a constant amplitude and frequency carrier voltage source that is used to excite a bridge-type circuit, which

is comprised in part by the sensing capacitors.

- Frequency modulation schemes, where the sensing capacitance acts as the frequency determining component in a frequency modulation oscillator, i.e. a current controlled oscillator, or where the sensing capacitance acts as a timing component for a linear ramp.

- Switched-capacitor schemes, where a voltage, scaled by the switched sensing capacitance, is applied to an analogue-to-digital converter, or to a voltage controlled oscillator (VCO).

These schemes will be examined in more detail in the next chapter. The research objectives will now be summarised.

1.5 Research Objectives

The scope of the work reported here can be stated as the investigation of interface circuits for capacitance sensors, in particular capacitance ratio sensors, suitable for integration on silicon using the ES2 CMOS ASIC process [23]. The research objectives are the investigation and characterisation of discrete component, bread-boarded versions of the interface circuits followed by the production of an integrated implementation with the following attributes:

- Low power operation: less than 22.5mW for each interface circuit.

- Long data-acquisition time: a multiple of 20mS, for 50Hz rejection, within the node polling time of 100mS.

- Operation over the industrial temperature range: $-40^{o}C$ to $+80^{o}C$ [8].

- High precision: better than 0.1%.

- Operation with sensor capacitance of down to 20pF.

- A low cost, standard-cell ASIC implementation with a minimum of external components and silicon area.

1.6 Achievements

This research programme has required the acquisition of a wide range of CAD software skills including experience of both full-custom CMOS design and layout, and standard-cell ASIC CMOS design. CAD software employed in full-custom design included the circuit simulator 'HSPICE' and IC layout packages 'Caesar' and 'Magic'. Standard-cell design was accomplished using the ES2 Solo 1200 suite of software.
The major achievements of this work can be listed as follows:

- A novel capacitance ratio to frequency ratio converter interface circuit was developed that is capable of being integrated using a standard-cell ASIC process.

- The inadequacy of the interface circuit first order theory was demonstrated and a second-order theory that accurately predicted the performance of a discrete component version of the capacitance ratio circuit was developed.

- An integrated implementation of the capacitance ratio converter has been designed. A prototype sample of this circuit, which was fabricated by ES2, has been shown to operate according to first-order theory and thus confirm the expected benefits of integration.

- An ASIC implementation of the capacitance ratio converter is demonstrated as being capable of meeting the requirements for field-bus operation within an industrial process control environment.

1.7 Thesis Layout

Switched-capacitor techniques for capacitance sensor interfacing are reviewed in *Chapter* 2, beginning with general purpose analogue-to-digital converters and progressing onto interface circuits. Charge-injection and clock-feedthrough are also examined followed by schemes to minimise this source of inaccuracy. The capacitance sensor interface circuits devised and investigated in this project are presented in *Chapter* 3, along with an analysis of their performance. Experimental investigations of these circuits in a discrete component, bread-boarded form are reported in *Chapter* 4. *Chapter* 5 contains a description of the design and test of the standard-cell implementation of the interface circuits. Finally, the conclusions from the research reported in this thesis and recommendations for further work are presented in *Chapter* 6.

Chapter 2
Capacitance Sensor Interfacing Using Switched-Capacitor Techniques

2.1 Introduction

Three techniques for the conversion of a capacitance variation to a corresponding *digital* or *analogue form* were identified in §1.4, *p* 16. The conversion of capacitance variation to a *digital word* can similarly but more specifically be considered as belonging to one of three methods. The first method makes use of the general purpose analogue-to-digital converter, illustrated in *Fig.* 5. Here, the capacitance variation is transformed into a voltage level suitable for application to the voltage input of such a general purpose ADC. The ADC then performs the voltage level to digital word conversion. Note the presence of a digital-to-analogue converter (DAC) to provide the feedback to program the amplifier and signal processing circuitry characteristics. Secondly, a general purpose ADC can be modified to convert a capacitance variation directly into a digital word. This can be achieved for instance by applying a reference level to the voltage input and using one or two of the ADC capacitances that normally appear as constants in the transfer function as input variables. The third and final option is the use of an interface circuit to convert the capacitance variation into a frequency or duty-cycle output. A digital-word can be produced from this frequency by pulse counting techniques. The three different options are represented as block diagrams in *Fig.* 6(*a*),(*b*) and (*c*) .

The concept of replacing a resistor by a frequency controlled switched-capacitor (SC) was introduced by Fried [39] in 1972, permitting the minimum component, MOS technology compatible implementation of filters with frequency controllable characteristics. The switched-capacitor integrator later became an alternative to the Miller

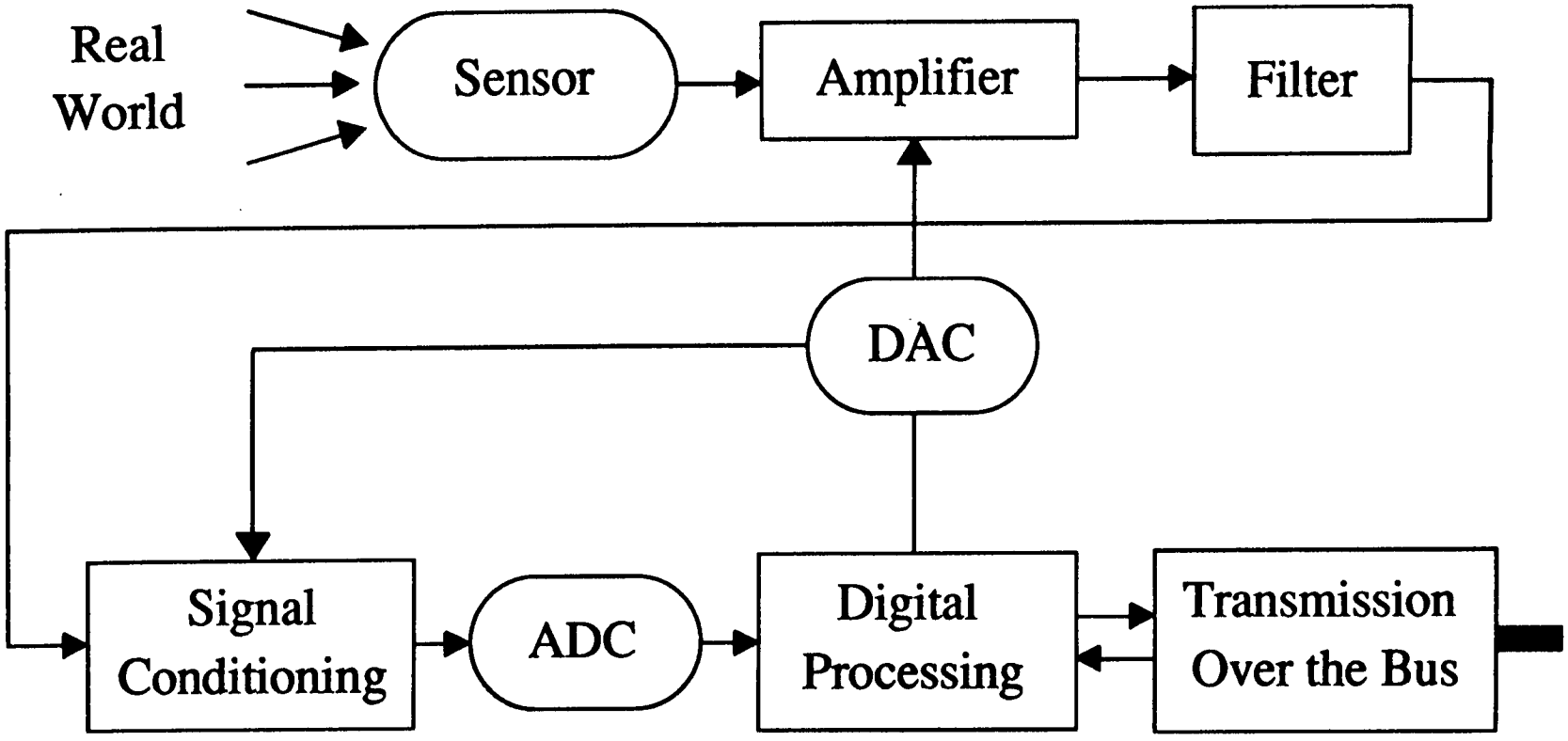
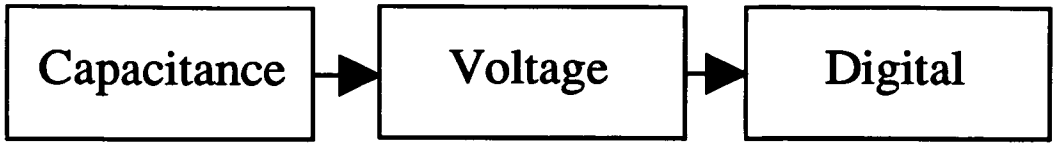
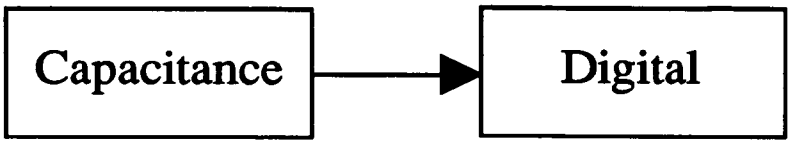


Figure 5: A representation of a general purpose ADC



(a)



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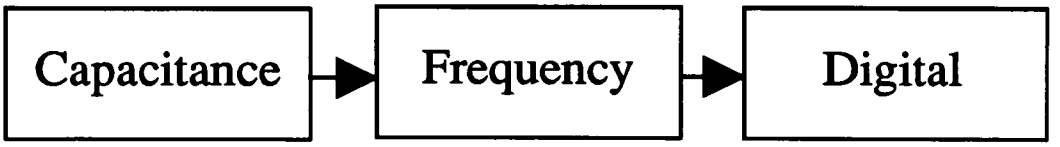


(c)

Figure 6: Three methods of capacitance conversion based upon **(a)** the general purpose ADC, **(b)** the modified ADC and (c) the interface circuit

integrator as a basic active filter building block [40]. This circuit, shown in *Fig.* 7(*b*), comprises a capacitor, C_1, and two MOS switches between the voltage input and the non-inverting input of the operational amplifier, rather than the single resistor, R, of the Miller integrator, illustrated in *Fig.* 7(*a*). The two switches are driven by two non-overlapping clocks, ϕ_1 and ϕ_2. However, the sensitivity of this SC integrator to parasitic capacitances limits the minimum value of the switched-capacitor, C_1. The stray-free (or parasitic insensitive) non-inverting integrator, described by Martin [40] and shown in *Fig.* 7(*c*), permits the use of smaller integrated capacitors reducing the silicon area requirements of the circuit. Initially switched-capacitor techniques were restricted to filter applications, although they subsequently found wider use, in analogue-to-digital conversion for example. The ability of a switched-capacitor to convert a capacitance variation to a stream of proportional charge pulses makes it suitable for capacitance sensing. Furthermore, the stray-insensitive integrator is valuable in eliminating the effects of parasitic capacitance associated with sensor to circuit wiring, as can be observed from the frequency of its employment in interface circuits covered in the following review.

This chapter focuses upon the three capacitance to digital word conversion methods. General purpose switched-capacitor ADCs are reviewed first, with a discussion of binary-search and serial converters, the two slowest general purpose converter types. Circuit techniques that permit low-power, minimum silicon area and high accuracy design in an integrable form are identified and clock-feedthrough and charge-injection are discovered to be important sources of error. Next, interface circuits based upon these two groups of general purpose ADCs are reviewed followed by the third category of capacitance converter circuits. Circuit and device imperfections that limit resolution are given particular attention and circuit structures that avoid or minimise sources of error are identified; techniques that permit design with a standard-cell ASIC process are highlighted. To conclude the review of SC interface circuits their characteristics, including power consumption, silicon area, conversion time and resolution,

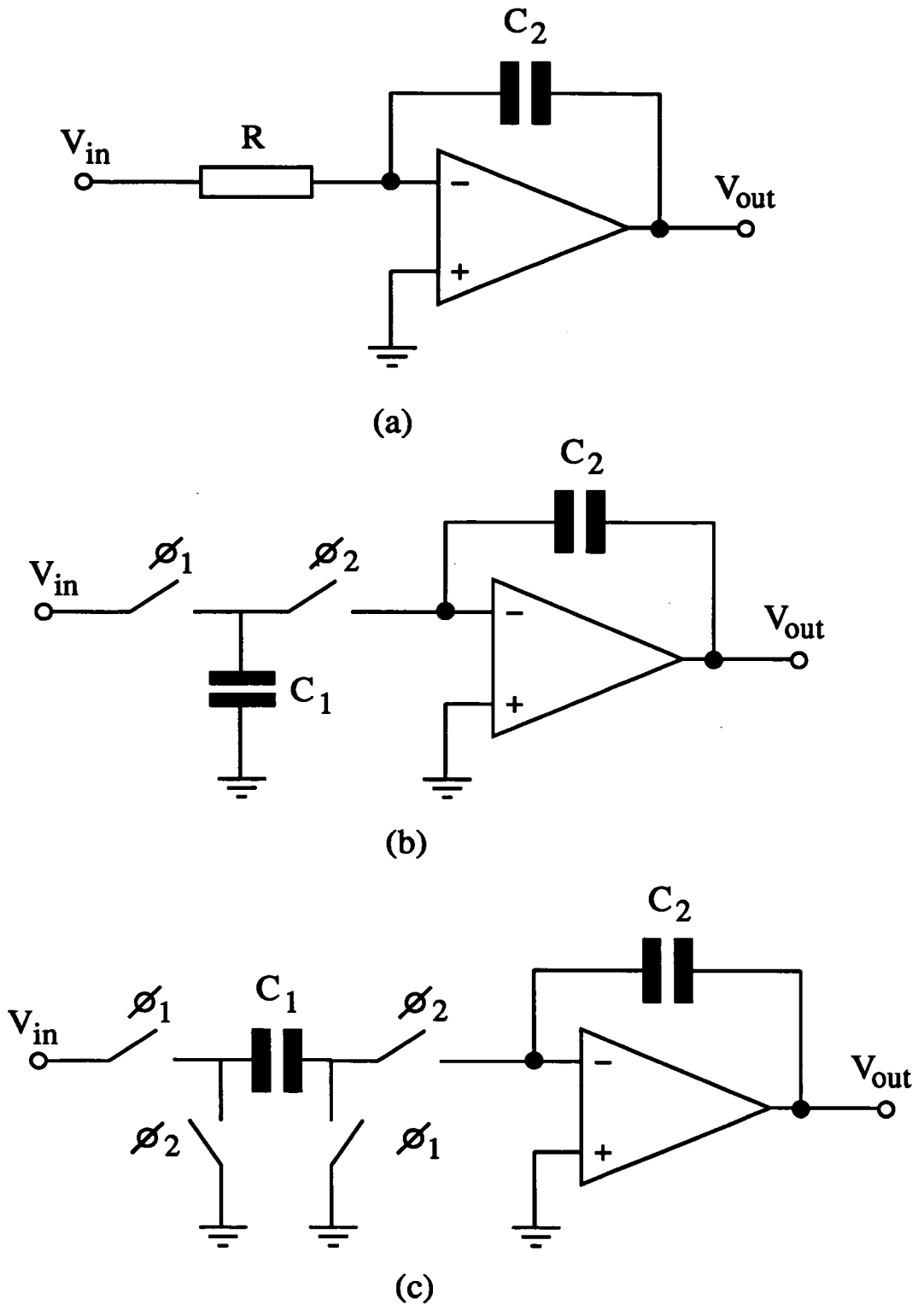


Figure 7: Three integrators, **(a)** the Miller integrator, **(b)** a SC integrator, and **(c)** a stray-free SC integrator

are then analysed within the context of the project research objectives, in order to gain an appreciation of the performance of present capacitance interface circuits and to assist in the selection of suitable circuits. Finally, charge-injection and clock-feedthrough are considered. Investigations into these error mechanisms are reported, followed by a review of cancellation schemes.

2.2 General Purpose SC Analogue-to-Digital Converters

The analogue-to-digital converter circuits reviewed in this section are of a general purpose nature, i.e. they convert a voltage more commonly than current, into a digital form. As *Fig.* 5, *p* 21 illustrates, additional circuits are needed to apply the general purpose ADC to the measurement of a transducer output. The circuits required depend both on the nature of the transducer and the ADC. For instance, an RTD may require a current to voltage conversion stage; or the design of the ADC may dictate that an anti-alias filter and/or sample-and-hold module be used. However, the analogue-to-digital converters considered here are not intended for general purpose use, but specifically for capacitance sensor interfacing with capacitance ratio sensors in particular, as was established in *Chapter* 1. Thus the diverse preconditioning circuits required for interfacing various sensors to a general purpose ADC will not be considered. The conversion of absolute capacitance, differential capacitance and capacitance ratio to voltage can be achieved by three similar circuits, illustrated in *Fig.* 8 along with expressions describing their steady-state behaviour. The first circuit, shown in *Fig.* 8(*a*), produces an output voltage proportional to the ratio of two sensor capacitances. A circuit resembling that used by Huang *et al.* [41] and reproduced in *Fig.* 8(*b*), converts absolute capacitance to a proportional voltage and, with the addition of another input stage as illustrated in *Fig.* 8(*c*), permits output of voltage proportional to differential capacitance.

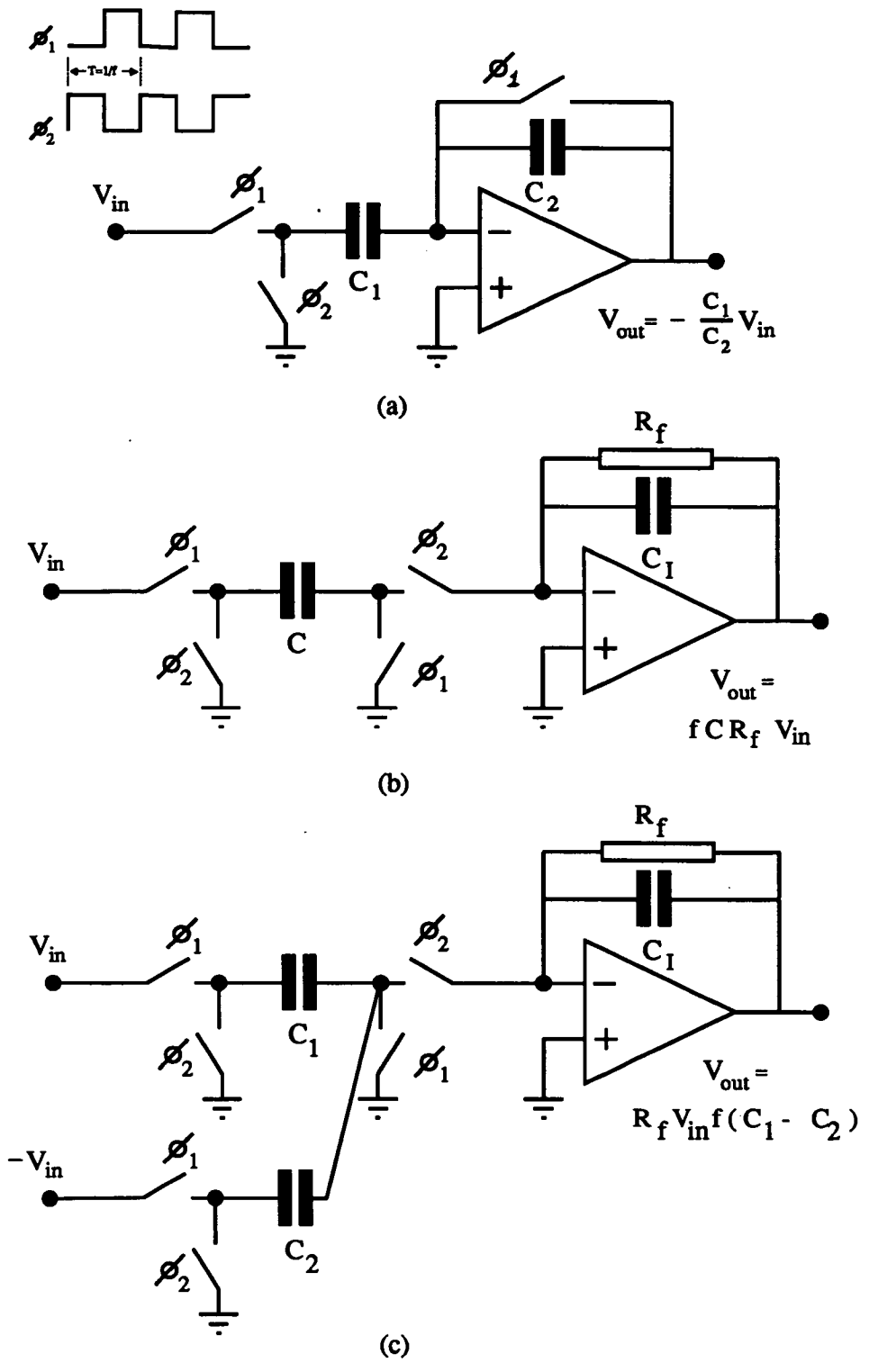


Figure 8: Three SC interface circuits, **(a)** a capacitance ratio converter, **(b)** an absolute capacitance converter, and **(c)** a differential capacitance converter

Other interface circuits, which convert capacitance variation to voltage, have been proposed. Yeh, Dendo and Ko [42] have described a switched-capacitor interface circuit for capacitive transducers that is insensitive to large fixed stray capacitances and has independently programmable offset and sensitivity. This latter feature avoids the need for trimming operations necessary when the capacitive transducers are to be interchangeable. Hagiwara *et al.* [43] have presented a converter that has an output voltage proportional to a sensor capacitance. The circuit is stray-insensitive and has an error of less than 0.1% for a sensor capacitance of 10pF. More recently Puers *et al.* [35] described the design of a silicon pressure sensor combined with a dedicated CMOS interface circuit for biomedical applications. The interface circuit is a switched-capacitor capacitance-to-voltage converter in a differential measuring arrangement.

The use of a general purpose analogue-to-digital converter with one of the above interface circuits can be improved upon for the present application. This improvement can be achieved by absorption of the sensor capacitance into the ADC, thus effecting a reduction in component count and thence power consumption and silicon area. Switched-capacitor ADCs are particularly suited to such a modification.

Switched-capacitor ADCs that generally cannot be interfaced directly with capacitance sensors are reviewed in the following two subsections. Those that can, upon modification, are identified and the unsuitable types discounted in an attempt to clarify what alternative schemes are available and to "clear the field" prior to a more detailed look at capacitance interface circuits. Highly parallel techniques, flash converters for instance, are not considered, since their conversion speed and power consumption are much greater than are desired for industrial process control applications [44]. This review will concentrate on conversion techniques that are not limited by the matching of active or passive components, which generally restricts precision to around 0.1% [45, 46]. Matching accuracies better than 0.1% can be achieved if component adjustment techniques, such as laser-trimming, are used. This approach, however, is costly in terms of fabrication processing and IC area [47]. An alternative method is the

addition of a calibration network to the ADC to improve matching accuracy, as for example employed by Leme and Franca [48] in a capacitor-array successive approximation converter to obtain 16-bit resolution. Nevertheless ADCs based upon capacitance matching must incorporate certain design features, for instance common-centroid layout and a constant ratio of capacitor area to perimeter, if high matching accuracy is to be achieved [49]. This precludes the use of a standard-cell ASIC process.

Returning to the general purpose ADC two broad categories are identifiable: the serial and the binary search converters. The former category comprises two converter types: the dual-slope converter and the delta-sigma modulator or converter. The latter category also embraces two categories: the successive approximation converter and the algorithmic converter.

2.2.1 Serial or Integrating SC Analogue-to-Digital Converters

The serial or integrating converter represents the linear search method of analogue-to-digital conversion and is the slowest conversion category requiring at least 2^n clock cycles per conversion for n-bit resolution. There are two analogue-to-digital conversion methods within this category to which switched-capacitor techniques have been applied successfully: dual-slope and sigma-delta conversion. Both methods operate on an integration and charge-equalisation principle [50], with the former being based upon voltage-to-time conversion and the latter upon voltage-to-frequency conversion [51]. Serial converters have two important advantages [52]:

- Tolerance of component inaccuracy and instability. For example, the use of the same capacitor for the signal under measurement and the reference relaxes the capacitance accuracy and stability requirements.

- The converter can be made insensitive to mains pick-up on the input signal by chosing the integration time to be a multiple of 20mS.

Dual-slope integration, illustrated in *Fig.* 9 [44], has long been used for low-speed precision instrumentation and measurement by virtue of its stability and linearity [53]. The conversion process, illustrated in *Fig.* 9, has two distinct phases. The first, the measurement phase, begins with the closure of switch '1' and the integration of the input voltage, V_{in}, until the threshold voltage, V_{th}, is reached. The digital controller now permits the integration of V_{in} to continue for a fixed time, t_1, and the accumulation of a reference count, N_{ref}. The fixed time should be a multiple of 20mS to reject 50Hz. Phase two, the count phase, begins with the reset and restart of the counter and with the closure of switch '2' after switch '1' has been opened initiating a negative integration of the reference voltage, V_{ref}. The negative integration continues until V_{th} is reached and the second count, N_{out} is accumulated.

Thus:

$$N_{out} = N_{ref} \frac{V_{in}}{V_{ref}} \tag{2.1}$$

The count, N_{out}, is not a function of the threshold of the comparator, the slope of the integrator or the clock rate, proving this technique to be suitable for implementation with the low quality components generally provided with a standard-cell ASIC process. Moreover, dual-slope conversion has good temperature stability and a simple, low cost construction.

Kondoh and Watanabe [53] developed a dual-slope converter in which the conventional RC integrator was replaced with a switched-capacitor integrator. A floating-point technique was used to avoid the 2^n capacitance ratio required to obtain an n-bit resolution, thus achieving a faster conversion speed. A discrete component prototype had a resolution of 10-bits with an additional 2½ bits for the exponent. Conversion speed is not explicitly stated, however it can be deduced from a diagram of the

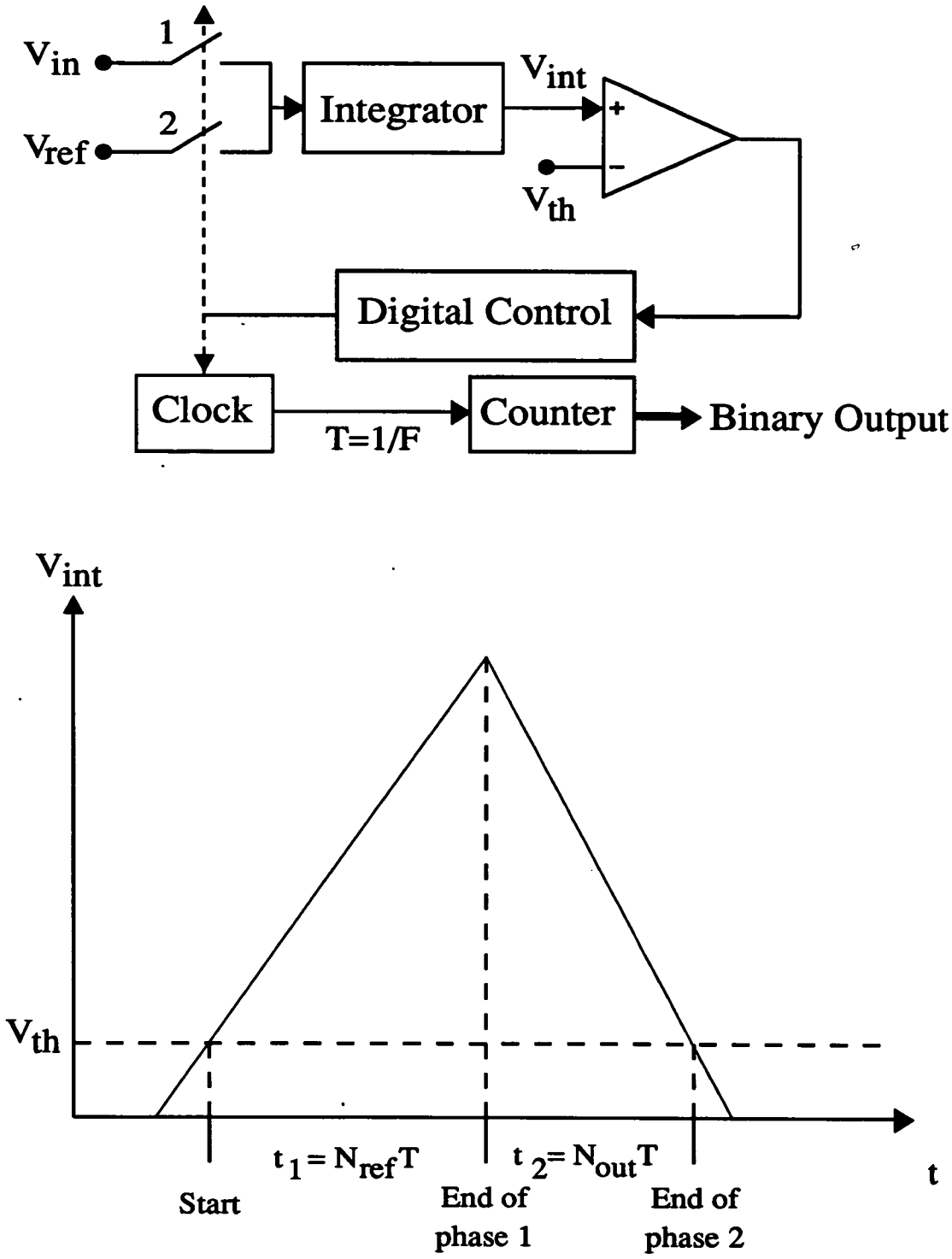


Figure 9: The dual-slope ADC, showing a block diagram of the circuit and a plot of the ADC integrator output voltage during both phases of the conversion process

experimentally observed output waveform that the conversion time was approximately 2mS. The circuit, which is offset-free, parasitic insensitive and unaffected by the finite open-loop gain of the operational amplifier, can be modified to become insensitive to capacitance ratio variations. The main source of error is clock-feedthrough. A capacitance interface circuit based on this converter is described in §2.3.1, *p* 41.

Sigma-delta conversion is a newer technique based upon a charge-balancing, or quantised feedback principle, that was introduced in 1978 by van de Plassche [54]. In this publication the sigma-delta converter is discussed as an alternative to the dual-slope converter. The circuit achieved 3½ digit resolution in a conversion time of 10mS with a clock rate of 200kHz, but was constructed using switched current sources and integrated on two ICs in a bipolar technology. Power consumption was 27mW for ± 7.5 volt supplies.

A decade later Robert *et al.* [55] presented a CMOS switched-capacitor implementation of the sigma-delta converter in which all the signals were represented by charges rather than currents. A block diagram of the sigma-delta converter and a representation of the integrator output with respect to time are illustrated in *Fig.* 10. In contrast with the dual-slope technique with its two-phase process, sigma-delta conversion combines the measure and count functions in one, fixed time interval [50]. After the integrator and the counter are reset a fixed number, 2^n, of integration steps are performed, where n is the number of bits required. The measurement voltage, V_{in}, is integrated positively until interrupted by a negative integration step contributed by the reference voltage, V_{ref}. This occurs when the integrator output voltage, V_{out}, rises above zero volts as indicated by b. Each positive transition of b is accumulated on the counter until the 2^n steps are complete.

Thus:

$$N = 2^n \frac{V_{in}}{V_{ref}} \tag{2.2}$$

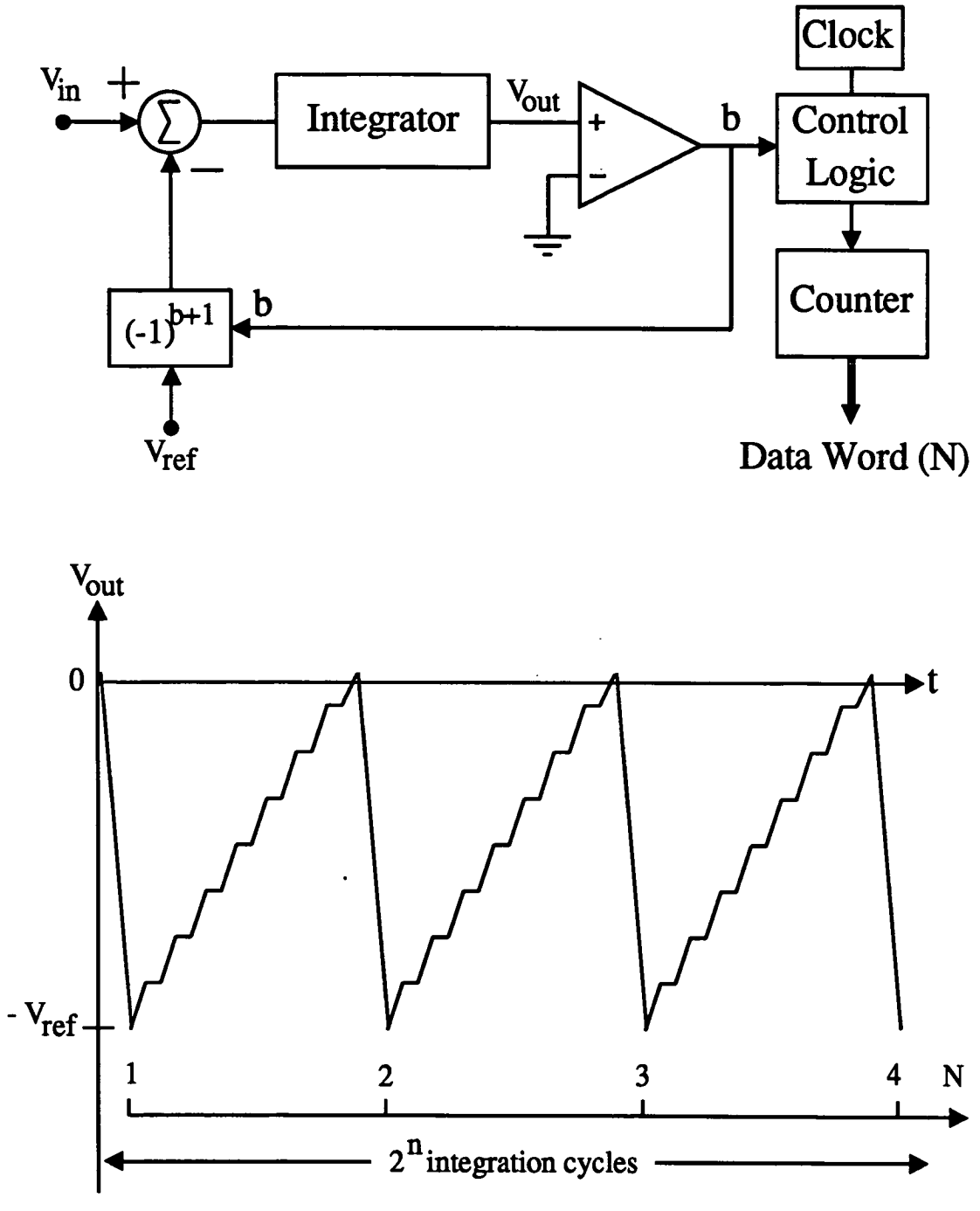


Figure 10: The delta-sigma ADC, showing a block diagram of the circuit and a plot of the ADC integrator output voltage during a complete conversion cycle

This SC sigma-delta ADC is intended for *data−acquisition* applications, in instrumentation or measurement for example, in contrast with the oversampled sigma-delta converter, which is intended for *signal−acquisition* [56]. This latter type of ADC samples continuous-time signals converting them into discrete-amplitude, discrete-time sequences suitable for digital signal processing and transmission over digital communication channels [57]. Returning to Robert's *et al.* SC sigma-delta ADC, specific differences in operation can be identified when compared with the oversampled converter:

- The input signal is converted once every 2^n clock cycles rather than once every F cycles, where F is the oversampling ratio.
- The integrator and counter are reset before each conversion.
- The digital circuitry following the integrator contains a counter rather than a digital low-pass filter.

Consequently this circuit is simpler than the oversampling ADC; however it is much slower, restricting its use to instrumentation and measurement applications. Rejection of 50Hz can be achieved by setting the conversion time to be a multiple of 20mS, although this was not stated by Robert *et al.* Primary sources of error were identified to be charge-injection and the offset voltage of the operational amplifier, and one digital and one analogue compensation scheme was proposed to reduce the effects. Other error sources were noise, finite amplifier dc gain effects and capacitor non-linearity. To test each compensation scheme a version of each of converter was integrated in an area of less than $1mm^2$ using a $4\mu m$ low-voltage CMOS process. A resolution of 16-bits was obtained with both circuits, with a power consumption of $65\mu W$ and conversion time of 1.32s for the digitally compensated converter, and a power consumption of $150\mu W$ and conversion time of 5.1s for the analogue compensated ADC.

Robert *et al.* followed this first order sigma-delta converter with a second order version that demonstrated a considerable improvement in conversion time at the cost of

increased silicon area and power consumption. The converter consisted of two inter-linked first-order loops to avoid the unstable two integrator, single loop configuration. Offset voltage and charge-injection were again identified as the primary sources of error and a digital compensation scheme was incorporated to reduce their effects. The ADC was integrated in a 3-μm low-voltage CMOS process in a die area of $4.6mm^2$. A 15-bit resolution was attained in a 10mS conversion time and with a power consumption of 325μW.

Kondo and Watanabe [51] have combined dual-slope and sigma-delta conversion techniques in a two-stage switched-capacitor ADC that increases conversion speed. The ADC comprises a voltage-to-frequency stage that produces the most significant bits and a voltage-to-time stage that produces the least significant bits. The two converter stages share most of their components thus improving speed for a minimal increase in component count. Resolution is limited by clock-feedthrough and one capacitance ratio. Error analysis has shown that a conversion resolution higher than 12-bits is possible at a conversion rate that compares favourably with that of a successive approximation ADC when realised in CMOS. The approach was selected by Kondo and Watanabe in preference to multi-slope conversion on account of the precisely weighted current sources required for this type of measurement.

Switched-capacitor dual-slope and sigma-delta analogue-to-digital converters have been shown to achieve high accuracy in reasonable conversion times, although the improved conversion time of the second order sigma-delta converter was gained with the loss of 50Hz rejection. In general, both techniques remove dependence on passive and active component matching and are suitable for a simple, standard-cell CMOS ASIC implementation. Moreover each has the parasitic insensitive integrator as a main component, a necessity for the present application, although both have proven to be subject to the effects of charge-injection and clock-feedthrough.

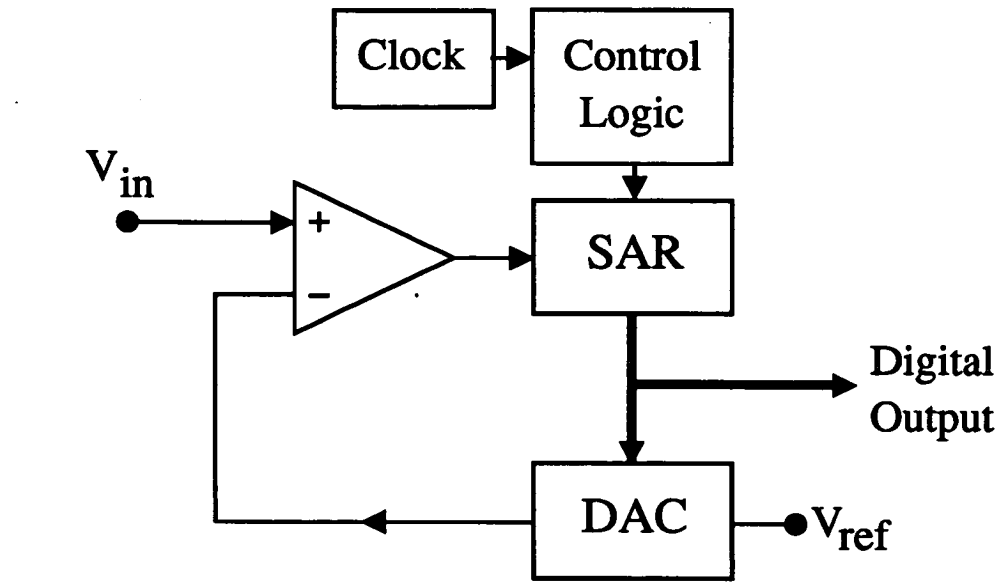
The switched-capacitor dual-slope or sigma-delta converter can be modified to permit conversion of absolute capacitance, capacitance ratio, or capacitance difference to a digital form by the addition of one of the three interface circuits discussed in §2.2, *p* 25. An alternative is to modify the ADC itself to function specifically, for example as a capacitance ratio to digital-word converter. Circuits with this latter structure are the subject of §2.3, *p* 39. However, before this converter type is reviewed binary search conversion, the second class of ADC, will be considered.

2.2.2 Binary-Search SC Analogue-to-Digital Converters

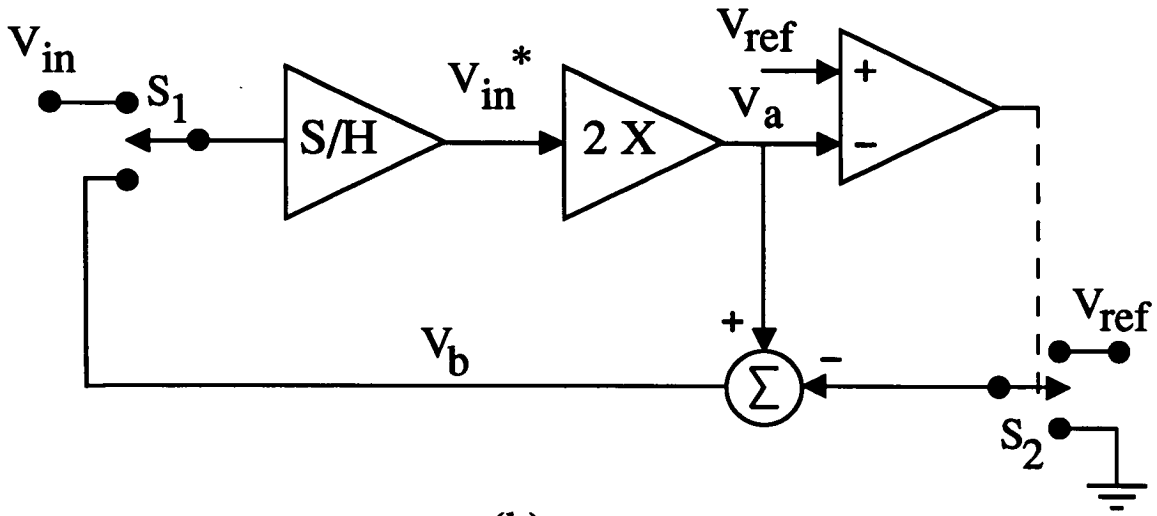
Analogue-to-digital converters based on binary-search techniques have a higher conversion rate: only n clock cycles are required for a n-bit conversion. The successive approximation and the algorithmic converter are the two principal types of binary-search ADC.

A block representation of the successive approximation converter is illustrated in *Fig.* 11(*a*) [52]. The analogue input, V_{in}, is successively compared with the output of the digital-to-analogue converter (DAC), which is directly coupled to the successive approximation register (SAR). The comparison begins with 0.5 V_{ref} at the DAC output, and depending on whether the MSB is 1 or 0, i.e. whether V_{in} is greater or smaller than 0.5 V_{ref}, the DAC scales V_{ref} to 0.75 V_{ref} or 0.25 V_{ref} before the next comparison is performed and the second most significant bit is generated. Thus the comparator makes a decision on the state of each bit until the contents of the SAR are the nearest representation of the analogue input, conforming to the binary-search technique.

This technique typically has a conversion time in the range of $1\mu S$ to $50\mu S$ [52] - far faster than that required for the present application. In addition the complexity,



(a)



(b)

Figure 11: Two binary-search ADCs, **(a)** the successive approximation ADC, and **(b)** the algorithmic ADC

cost, and dependence on closely toleranced components compounds the technique's unsuitability. A good example is the switched-capacitor digital capacitance bridge developed by Watanabe and Temes [58] based on the successive approximation principle that achieved 10-bit quantisation accuracy. Digital-to-analogue conversion was performed by a binary-weighted capacitor array, that limited the accuracy through the effects of capacitance ratio mismatch. The limitations of capacitance matching were discussed more fully in §2.2, *p* 25

The second type, the algorithmic converter, can be implemented as a series of N stages, each comprising a comparator and a multiply-by-two stage and determining the state of one of the N output bits [44]. Replication and iteration can reduce the excessive number of comparators required for this pipelined form of the algorithmic converter. The resultant second, cyclic version is represented as a block diagram in *Fig.* 11(*b*) [59]. The conversion begins with a sample-and-hold of the input voltage, V_{in}, under the control of switch, S_1. V^*_{in} is then applied to the multiply-by-two module and compared, as V_a, with the reference voltage, V_{ref}. If V_a is larger than V_{ref} then the corresponding bit is set to one and V_{ref} is subtracted from V_a under the control of switch S_2. If V_a is less than V_{ref} the bit is set to zero and V_a is unchanged. The resultant voltage, V_b, is circulated back round the loop, via S_1, for another iteration. The iterations are repeated until the desired number of bits are obtained.

Li *et al.* [59] have described a cyclic analogue-to-digital conversion technique that achieves 12-bit resolution without the use of matched capacitors when integrated with a CMOS process. Sources of error were the offset voltage and gain of operational amplifiers, charge-injection and capacitance voltage effects. The use of fully differential circuitry reduced the effects of charge-injection and capacitance voltage variation. Results are presented for a 5 μm CMOS implementation of the converter that achieved a 12-bit resolution at a sample rate of 8kHz. The analogue circuitry required an area of $1.55mm^2$ and consumed 17mW from 10 volt supplies. The most important limiting factor in this implementation was the residual loop offset; this is the operational

amplifier offset voltage accumulated as the signal is circulated around the loop.

An alternative cyclic converter was later presented by Shih and Gray [60] that periodically modified the reference voltage to compensate for the non-ideal signal transfer loop gain. This scheme achieved independence from the matching accuracy of the multiply-by-two block thus obviating the need for a ratio-independent multiplier, such as that described in the paper above. Similarly, fully differential circuitry was employed to reduce clock-feedthrough and charge-injection errors, with the residual loop offset remaining as the most significant source of error. The converter was integrated using a 5 μm CMOS process in an area of $2.26mm^2$. Resolution was 13-bits at a sampling rate of 8kHz.

A more recent algorithmic converter by Onodera *et al.* [61], based on a simpler conversion sequence, achieved an 8-bit resolution at a sample rate of 8kHz. The converter was integrated in an area of $0.79mm^2$ using a 2μm CMOS process and had a power consumption of 5mW when operated from a single 5 volt supply. Onodera *et al.* claim a 10 to 12-bit accuracy at a sampling rate of up to 30kHz with refinement of the design. Charge-injection and the finite gain of the amplifier were identified as the main sources of inaccuracy.

Dual-slope, delta-sigma and cyclic converters are all capable of achieving more than 10-bit resolution in conversion times faster than 20mS, suiting them for the present application where a conversion time of 20mS to 100mS is required. A common feature of all three techniques is independence from passive component matching thus circumventing a considerable impediment to high precision. Moreover, the techniques are capable of being integrated on silicon in a small area and with small power requirements by virtue of their low component count. This last feature applies particularly to the two serial techniques which both consist of an integrating operational amplifier, a comparator and other digital circuitry. However, the presence of a sample-and-hold element in the binary-search ADC could necessitate the use of a 50Hz

notch filter if this technique were to be used in an environment contaminated by mains noise. 50Hz noise can be eliminated from the two serial conversion processes by setting the integration time to be multiple of 20mS. Clock-feedthrough and charge-injection from MOS switches were identified as significant sources of inaccuracy in virtually all the ADC circuits reviewed in the present and the previous section. This is of consequence for the experimental work presented later in this thesis.

The algorithmic converter can be modified in a similar fashion to the serial converter, as detailed at the end of §2.2.1, *p* 28, to produce specific capacitance interface circuits. Indeed the three switched-capacitor ADC techniques have been developed to produce capacitance sensor interface circuits that are capable of achieving high accuracy in an integrable form. These and other interface circuits are discussed in the following section.

2.3 SC Interface Circuits

Serial and binary-search, general-purpose SC analogue-to-digital converters were reviewed in the previous section. These converter types conform to the first model identified in §2.1, *p* 20, and illustrated in *Fig.* 6(*a*), *p* 22, where capacitance is converted by an appropriate interface circuit to a voltage level suitable for input to an ADC. The ADC then completes the conversion to a binary digital word. In this section interface circuits that correspond to the second and third models, represented in *Fig.* 6(*b*) and *Fig.* 6(*c*) respectively, are reviewed.

As was stated in §2.1, *p* 20, switched-capacitor converters can be modified by the absorption of capacitance sensors into the general-purpose ADC to produce a "degenerate" ADC or interface circuit that is more compact and power efficient. However the "degenerate" ADC can then only be used for a specific application. The circuits

thus produced belong to the second category of converters where capacitance is converted directly into a binary digital word.

The third category, interface circuits that convert capacitance to a digital word with frequency as an intermediate variable, comprises circuits based upon a number of techniques. These circuits can be further characterised by the absence of a controlled conversion sequence. They are, in reality, free-running.

Recently there has been increasing interest in the development of circuits belonging to the latter two categories producing capacitance interface circuits capable of achieving high accuracy in a small silicon area and with low power requirements. Early circuits were concerned with measurement of on-chip capacitance. McCreary and Sealer's technique [62] was based on a special software algorithm in which the capacitance array under test was used as a precision voltage divider. Later Watanabe and Temes [58] proposed a switched-capacitor capacitance bridge that was capable of measuring discrete and MOS IC absolute capacitance as well as capacitance ratio. This circuit is an example of one of the earliest SC interface circuits capable of being integrated on silicon. Stray-insensitivity was ensured by connecting the four arms of the capacitor bridge between a low-impedance output and the virtual ground of an operational amplifier. Conversion was accomplished by comparing the charge stored on the capacitance under measurement with charges quantised by a binary-weighted capacitor array under the control of a successive-approximation register. Measurement accuracies of 0.08% and 1.79% were achieved for capacitances of 2200pF and 1pF respectively. The discrepancy with the resolution of 0.1%, yielded by error analysis, was attributed to the effects of clock-feedthrough. This circuit was cited earlier as an example of successive approximation conversion in §2.2.2, *p* 35.

Later, interface circuits for capacitance sensors were developed. It should be noted that there are three main categories of capacitive measurement: absolute capacitance, differential capacitance and capacitance ratio. The last two categories may

consist of one variable and one reference capacitor or two varying capacitors. The presence of two varying capacitors has implications for interface circuit design and can make calibration difficult, as is reported subsequently in *Chapter* 4. Referring to the three pressure measurement situations described in §1.4, *p* 14, both differential and ratio types where both capacitances vary, are usually applied to differential pressure measurement. The same types, where one capacitance is fixed and one varies, can be applied to gauge pressure measurement.

Interface circuits derived from the serial ADC will be reviewed in the next subsection and interface circuits developed from the algorithmic technique will be the subject of the following subsection. Successive approximation conversion has been discarded on account of its unsuitability for the present application. Finally, circuits that conform to the third, capacitance-to-frequency-to-digital model will be detailed.

2.3.1 SC Interface Circuits Based on Serial ADCs

Kondo and Watanabe [63] have developed a switched-capacitor interface for absolute capacitance sensors that is a modification of the switched-capacitor ADC reviewed in §2.2.1, *p* 28 [53]. Essentially the two-phase operation of the dual-slope technique, described in §2.2.1, is modified to comprise of a measurement stage during which the sensor capacitance, C_{in}, is positively integrated over a fixed number of steps, N_{ref}, and a count stage when a reference capacitor, C_{ref}, is negatively integrated. Thus *Eqn.* (2.1) becomes:

$$N_{out} = N_{ref} \frac{C_{in}}{C_{ref}} \tag{2.3}$$

In addition, an autoranging function is incorporated to accommodate a wide dynamic range of sensor capacitance and to obviate the need to cancel the potentially large sensor offset capacitance. Clock-feedthrough and uncertainty in the value of C_{ref} are

identified as the main error sources. Tests carried out on a discrete component prototype achieved a precision of 0.07% to 1% over a sensor capacitance range of 1 to 5600pF. The results were apparently obtained without feedthrough cancellation, although Kondo and Watanabe suggest incorporating a calibration stage to eliminate the main errors.

Matsumoto *et al.* [64] have developed a switched-capacitor ADC that can be applied to capacitance measurement. The circuit is based upon the charge-balancing principle with the integrator simultaneously accumulating the charge on the sensor capacitance, C_{in}, and extracting the charge on the reference capacitance, C_{ref}, over a fixed number of steps, 2^n. Thus *Eqn.* (2.2) becomes:

$$N = 2^n \frac{C_{in}}{C_{ref}} \tag{2.4}$$

Three applications for this technique were detailed. The first, a capacitance meter measured absolute capacitance with respect to a known reference capacitor and had an accuracy of approximately 1% over a measured capacitance range of 1pF to 1000pF when constructed in discrete component form. This error was attributed to clock-feedthrough. For the second application, hygrometry, the interface circuit was modified to cancel any offset capacitance associated with the transducer. No quantitative accuracy claims were made for this version. Finally, the charge-balancing circuit was used for signal-processing of a differential pressure transducer. Here, both the accumulation and extraction capacitances are sensing elements, with the differential pressure expressed as the ratio of N to 2^n according to *Eqn.* (2.4) above. Again no quantitative accuracy claims are made although the inclusion of clock-feedthrough compensation could improve precision to 14-bits.

Finally, Cichocki and Unbehauen [65] have presented three switched-capacitor configurations of interface circuits for capacitance transducers, of which one is based upon delta-sigma modulation. This circuit converts a capacitance ratio into binary word. The main sources of error are clock-feedthrough and operational amplifier

offset voltages, identified from computer simulation and experimental testing. Modified configurations that reduced the effect of these error sources were described. Resolution was not detailed.

2.3.2 SC Interface Circuits Based on Algorithmic Conversion

The algorithmic, or cyclic analogue-to-digital converters reviewed in §2.2.2, *p* 35 were considered to have many of the features deemed necessary of an integrated interface circuit for capacitive sensors.

Two switched-capacitor circuits based on the cyclic converter have been developed. The first, presented by Watanabe and Chung [66] and intended ostensibly for absolute capacitance measurement, was applied to humidity sensing. This circuit incorporated a differential integrator that provides a voltage output that is the difference between the charge accumulated on the transducer capacitance and a reference capacitor. 50Hz rejection was obtained by chosing the integration time to be a multiple of 20mS. Thus the requirement for some form of mains hum elimination is inherent in the initial sample-and-hold module shown in *Fig.* 11(*b*), §2.2.2, a property not recorded by Watanabe and Chung. The scaled differential voltage is then applied to a switched-capacitor cyclic ADC to provide a binary output. A reduced component count was gained by using the operational amplifier of the differential integrator in the cyclic conversion process. In addition, the conversion process is independent of offset voltages of operational amplifiers and capacitance ratios. However clock-feedthrough and the finite open-loop gains of operational amplifiers remain as the primary sources of error. Although a discrete component implementation of the circuit with partial clock-feedthrough cancellation had a resolution limited to 8-bits for a capacitance difference of 30pF with respect to a reference capacitance of 513pF, error analysis indicated that this could be improved to 13-14 bits in an IC realisation

with full clock-feedthrough cancellation.

The second interface circuit, developed by Matsumoto and Watanabe [67], was intended for application as an on-chip absolute capacitance meter or for built-in interfacing of intelligent capacitive transducers. This circuit similarly incorporates a switched sample-and-hold integrator that could be used for 50Hz rejection, although this was not stated by Matsumoto and Watanabe. The main sources of error were clock-feedthrough and the finite open-loop gain of the operational amplifiers. These errors limit the estimated precision when fabricated in a MOS IC form to 12-bits, and 14-bits if some form of clock-feedthrough compensation has been incorporated. Once again the resolution of a discrete component implementation was limited to 1% when measuring capacitors in the range of 2pF to 22000pF by the large feedthrough charge contributed by the discrete switches.

The above two algorithmic ADC-based capacitance interface circuits are capable of attaining up to 14-bit accuracy if implemented as an IC with some form of clock-feedthrough compensation. The importance of a parasitic insensitive configuration was acknowledged by both Watanabe and Chung, and Matsumoto and Watanabe when attempting to measure capacitance as low as a few picofarads. In addition, the use of an operational amplifier for both the sample-and-hold and multiply-by-two functions reduces the analogue component count to two amplifiers - the same number used in converter circuits based on serial techniques.

All the analogue-to-digital converters and their capacitance interface derivatives reviewed so far have had a controlled and recognisable conversion sequence. For example the dual-slope conversion process comprises a measurement and a count phase. Likewise the sigma-delta technique is composed of a fixed number of integration steps initiated by a start-of-conversion command. In contrast the interface circuits reported in the next section have no such discernible internal control sequence and are free-running or self-oscillating. This type of circuit conforms to the third category of

converter circuit, identified in §2.1, *p* 20 and illustrated in *Fig.* 6(*c*), *p* 22, that continuously converts capacitance variation to a corresponding frequency or duty-cycle output. The conversion to a digital-word is completed by an appropriate, synchronous digital counting scheme.

2.3.3 SC Interface Circuits with Frequency or Duty Cycle Output

Generally, two types of self-oscillating interface circuit can be identified. The first is the frequency converter [68], which is illustrated in *Fig.* 12 with typical graphs of integrator output voltage, V_I, and circuit output voltage, V_{out}, against time. The module labelled a represents a capacitor arrangement comprising control switches and measurement capacitors. The variation in the continuous frequency output, V_{out}, is proportional to a change in the measurement capacitance. The second type is the duty-cycle converter illustrated in *Fig.* 13, along with typical graphs of integrator output voltage and the circuit output voltage against time. The modules labelled a_1 and a_2 represent two measurement capacitors and their associated switches [68]. The output signal of this type is the duty cycle of a pulse-width modulated square-wave voltage that corresponds to the ratio of two measurement capacitances, or of one measurement and one reference capacitance.

Recently, Cichocki and Unbehauen [69] have reported a switched-capacitor interface circuit for capacitive sensors that is based on the latter technique. Although the circuit was only tested by computer simulation and no quantitative performance claims were made, a modified relaxation oscillator based circuit was discussed that compensates the offset voltage of the operational amplifier and clock-feedthrough effects. This circuit employed a different MOS switch control sequence, discussed later in §2.4.1, *p* 62, and a modified control strategy to compensate for offset voltage and clock-feedthrough. However, it is not clear how the strategy compensates clock-feedthrough.

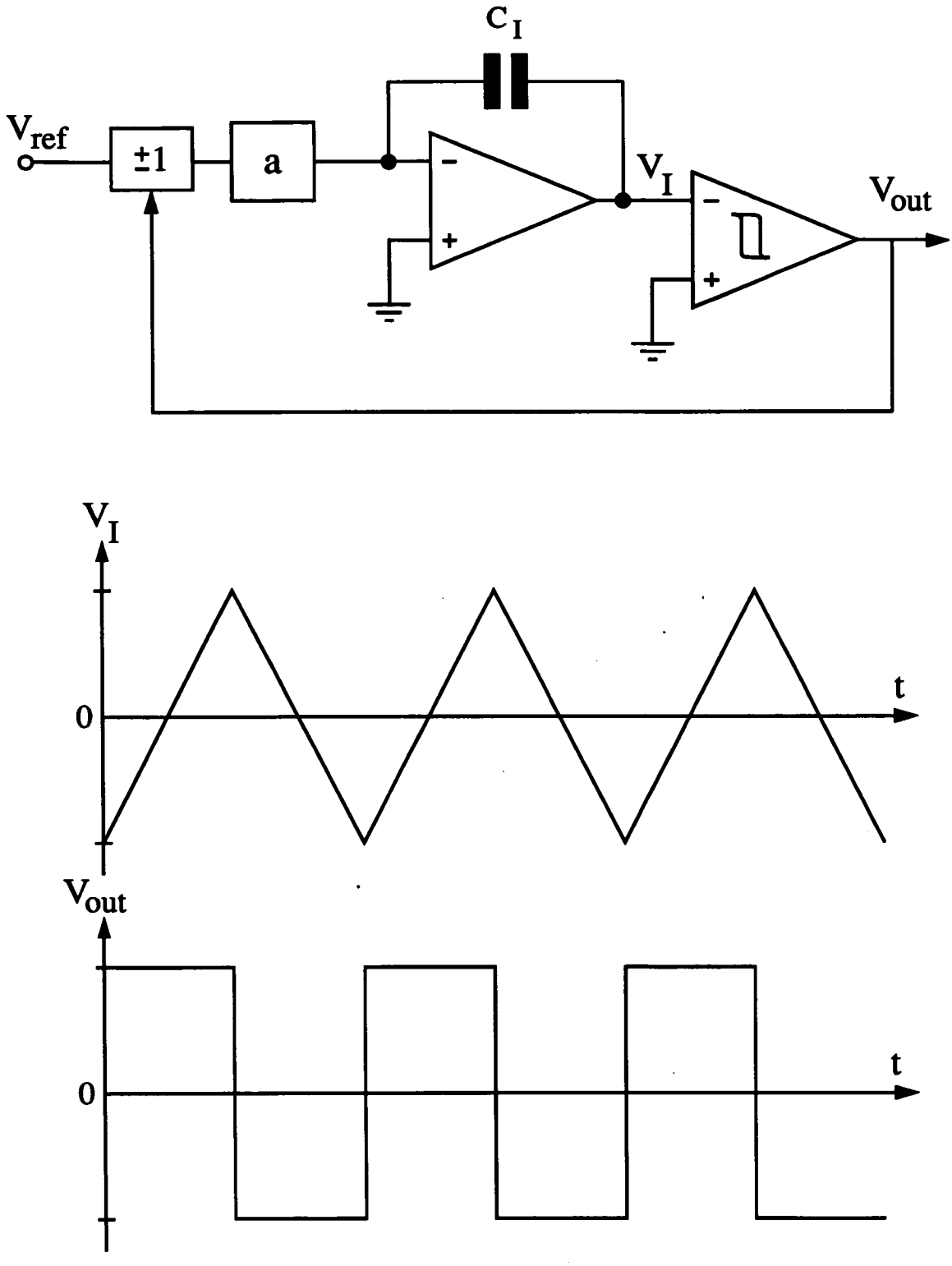


Figure 12: The frequency output SC interface circuit and a plot of the integrator output voltage and the circuit output signal over several cycles

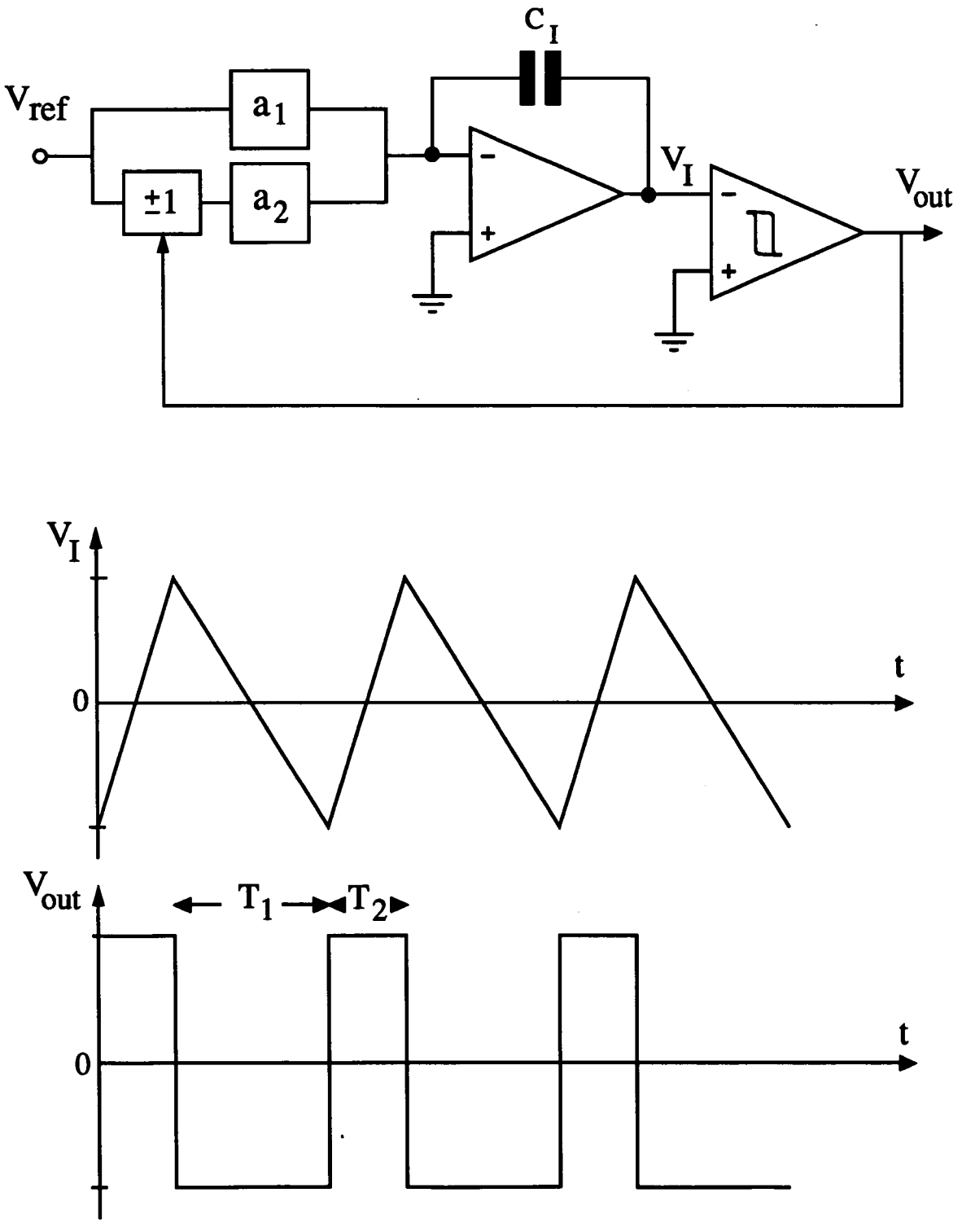


Figure 13: The duty-cycle output SC interface circuit and a plot of the integrator output voltage and the circuit output signal over several cycles

Component count is low, comprising an integrating operational amplifier in a stray-insensitive configuration, and a comparator. A more general publication by Cichocki and Unbehauen [68] encompassed a variety of CMOS switched-capacitor techniques applied to the conversion of resistance, inductance and capacitance to a frequency or digital signal. Circuits with frequency output, identified as the first type of self-oscillating interface circuit, and circuits operating on the charge-balancing principle, discussed in §2.3.2 above, were investigated and discussed in addition to circuits based on pulse-width modulation techniques. Although, again, no experimental results were presented, interface circuits based on these techniques were stated to be capable of high resolution, low cost and low power operation.

In contrast with pulse-width modulation or duty-cycle output converters, interface circuits with frequency output have been subject to wider research interest. One of the earliest capacitance-to-frequency converter was proposed by Krummenacher [70]. This circuit, which had an output frequency proportional to an external capacitor of value 2-20pF, was based upon a switched-capacitor, stray-insensitive two integrator loop. The circuit was fabricated in a full-custom, low-voltage CMOS process in an area of $1.1mm^2$ and had a power consumption of less than 0.1mW. Resolution was 16-bits at 10Hz and 10-bits at 1kHz clearly demonstrating the accuracy-conversion time compromise inherent in measurement. In addition, the circuit featured a low sensitivity to parasitic capacitances and operational amplifier and comparator offset voltages without recourse to compensation schemes. However, the presence of a sample and hold module makes the rejection of unwanted signals, e.g. 50Hz, difficult. Moreover the circuit design does not easily lend itself to standard-cell implementation as it contains less common components such as a voltage controlled amplifier and operational transconductance amplifiers.

A switched-capacitor voltage to frequency converter circuit, proposed by Watanabe *et al.* [71], operated on a principle similar to that of delta-sigma conversion. However, rather than counting the positive transition of pulses (*b* in *Fig.* 10, *p* 32) the

pulse stream is made symmetrical. Thus the output frequency is proportional to a capacitance ratio scaled by two references voltages and the reference frequency. The circuit, which consists of a parasitic insensitive SC integrator and a comparator, is unaffected by offset voltages. Although input-output curves were obtained for the circuit that show close correspondence with calculated values, no quantitative accuracy claims are made. It should be noted that the values of capacitance used for the measurements were large, being greater than 400pF. This circuit would be suited to integration with a standard cell ASIC process.

Kjensmo *et al.* [37] have reported two, non switched-capacitor front-end circuits for capacitive silicon pressure sensors fabricated with a $3\mu m$ p-well CMOS process in an area of $0.12mm^2$. The power consumption of each circuit was 3mW. Both circuits convert the variation of an integrated measurement capacitor, with respect to a reference capacitor, to frequency thus permitting the inclusion of a calibration stage to cancel any error terms. Consequently Kjensmo *et al.* were primarily concerned with temperature and time drifts. One design consisted of two matched RC oscillators. This circuit had a linearity of less than 1% over the capacitance range 0 to 50pF. The second circuit comprised a phase-locked loop and an additional voltage controlled amplifier. With calibration a linearity of better than 1% is claimed for a measurement capacitor of 10-50pF. Both circuits require close matching of their respective oscillator circuits to minimise the effects of time and temperature drifts. This indicates that full-custom layout ought to be used. Moreover, it is not clear if the circuit configuration is insensitive to parasitic capacitances.

Finally, Viswanathan *et al.* [72] have developed a switched-capacitor frequency tracking loop for digital transduction of resistance, capacitance and current. The circuit, illustrated in *Fig.* 14, consists of a resistor, R, and a switched-capacitor, C, connected in parallel between a voltage source, V_{ref}, and the virtual earth of an integrating operational amplifier in the familiar parasitic-insensitive configuration. The current contributed from R causes a corresponding negative going ramp voltage at the output

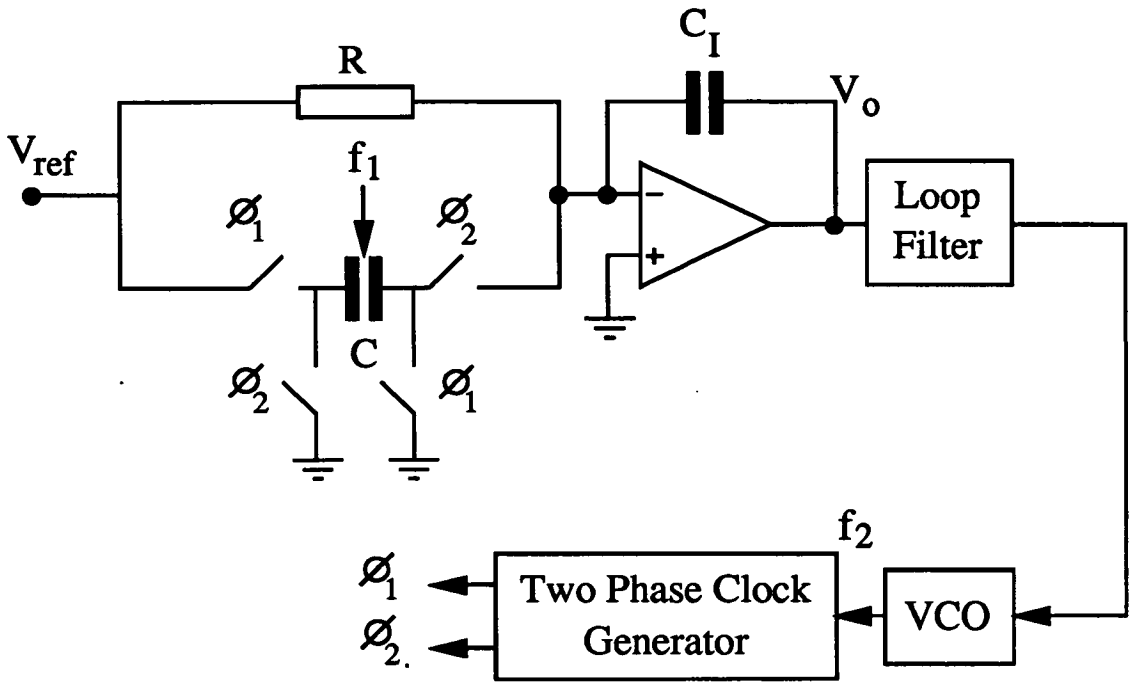


Figure 14: The Viswanathan SC frequency tracking loop

of the integrator. This voltage, V_O, filtered by the loop filter, is input to the voltage controlled oscillator (VCO). As the VCO input voltage decreases the output frequency, f_2, which controls the switched-capacitor stage, increases. Thus the capacitor supplies charge packets that increase the integrator output voltage in opposition to the resistor forming a negative feedback loop. In the steady state f_2 is a function of the switched-capacitor frequency, f_1, the capacitance, C, the resistance, R, and the reference voltage, V_{ref}. The circuit has the notable advantage of being insensitive to soft-nonlinearity or temperature dependence of the VCO. Moreover the frequency control loop can be implemented using standard-cell components. Experimental work was concerned with measurement of the frequency and transient response with a capacitance, C, of value 100-468pF. Viswanathan *et al.* suggested several variations of the circuit of *Fig.* 14. One of these alternatives was the replacement of R with a second switched-capacitor input stage, driven by a reference frequency, followed by a current averaging network that feeds a continuous current into the integrator. Configured in this fashion the frequency control loop would be capable of converting a capacitance ratio to a corresponding frequency output. However, this modification was not discussed in the publication and it was not made clear why it was necessary to use an averaging network. THIS CIRCUIT WILL BE DISCUSSED IN MORE DETAIL LATER IN THIS WORK, SEE §3.2, p 70.

Duty-cycle and frequency output, self-oscillating circuits have been reviewed. Generally, all the circuits have a simple construction requiring few analogue components and thus permitting implementation in integrated form in a small area. Many feature the parasitic capacitance insensitive integrator, a necessity for the present application. Of the six publications reviewed in this subsection only that of Krummenacher [70] has demonstrated experimentally that low value measurement capacitance can be converted to an output frequency with high resolution. In addition the silicon area and power requirements of the circuit recommend it to the present application. However, the need for full-custom design and the presence of a sample and hold module in the circuit negate these advantages. In contrast the frequency control loop of

Viswanathan *et al.* [72] has many of the attributes desired of a smart transmitter circuit for industrial process control applications, namely: low component count, parasitic insensitivity and the capability of being implemented using a standard-cell ASIC process.†

2.3.4 An Analysis of SC Interface Circuits

The review of switched-capacitor techniques for capacitance sensor interfacing has encompassed a variety of circuits, from serial and binary-search general-purpose analogue-to-digital converters to free-running interface circuits. In the selection of suitable circuits for capacitance sensor interfacing all the above techniques should be analysed within the context of the research objectives stated in §1.5, *p* 17.
Two questions should be answered:

- Do interface circuits that employ switched-capacitor techniques provide the required performance ?

- If so, which of the many techniques reviewed has the most appropriate characteristics and is best suited to a standard-cell ASIC implementation ?

The performance objectives, stated in §1.5 are: power consumption of less than 22.5mW; better than 10-bit resolution, when measuring differential capacitance with capacitive elements of an absolute value down to 20pF; a data-acquisition or conversion time in the range of 20mS to 100mS; implementation as a standard-cell ASIC with minimal area requirements; and finally, operation over the industrial temperature

† It should be noted that the publication by Viswanathan *et al.* [72] was discovered some time after a switched-capacitor ratio converter of similar configuration had been developed independently and was under investigation as part of this project.

range.

In answering the first question each of the stated performance objectives will be considered in turn and compared with those of all the serial and cyclic, general-purpose ADCs and their associated interface circuits, and the free-running interface circuits.

All the circuits reviewed in this chapter have a power consumption, if detailed, of less than 17mW, lower than the target dissipation of 22.5mW, with the exception of that of van de Plassche [54] which was fabricated in a bipolar technology. In fact some circuits achieved a power dissipation of less than 1mW, notably Krummenacher's [70] at $80\mu W$ and Robert's *et al.* [55] digital and analogue compensated circuits at $65\mu W$ and $150\mu W$ respectively.

An experimentally proven resolution of better than 10-bits was more difficult to attain with the ADC-derived interface circuits and the free-running interface circuits even for measurement capacitance much greater than 20pF. Krummenacher's capacitance-to-frequency converter [70] was the only circuit that conformed to the specification with 16-bit resolution over a measurement capacitance range of 2-20pF. The other circuits were limited to 8 to 9-bit resolution on the evidence of results from discrete component implementations, although several authors [64, 66, 67] indicated from error analyses that up to 14-bit precision might be attainable from integrated versions of their respective discrete interface circuits with some form of feedthrough compensation.

The conversion time specification is, in contrast with power consumption and resolution, more generous with 20-100mS available. All the ADCs and interface circuits reviewed were capable of meeting this specification. The only exception was Robert's *et al.* [55] two versions of the switched-capacitor delta-sigma converter which required 1.3s and 5.1s. It is of interest that these two circuits had particularly low power consumption, noted above, indicating a trade-off with conversion time.

This highlights one of the compromises encountered when designing converter and interface circuits for fabrication on silicon. The trade-offs encompass such aspects of performance as power consumption, speed, accuracy and IC area. Another good example is the conflict between resolution and converter bandwidth of the Krummenacher circuit [70], which was capable of resolving 16-bits at 10Hz but only 10-bits at 1kHz.

The silicon area requirements for the proposed interface circuits are less easily quantified. In general the objective is to achieve an integrated version in as small an area as possible. Bearing in mind that a complete instrumentation node consisting of interface circuits, computer and communications circuitry is envisaged beyond the immediate objective of producing prototype integrated interface circuits, these prototype circuits should be designed to occupy as small an area as is feasible. A single ASIC is limited primarily by yield considerations to a maximum size of, typically 10mm by 10mm, and this size will not be cheap. Economics may dictate significantly smaller area for cost effectiveness. Hence, if a multi-function ASIC containing several sensor inputs is to be realised then the interface circuits, which are composed of inherently large analogue components, must be compact. The probable area required can be equated approximately to the analogue component count. The serial ADCs and the free-running interface circuits typically require an operational amplifier and a comparator, or some similar device. The cyclic ADCs, reviewed in §2.2.2, *p* 35, contained three such devices, although the derived interface circuits reduced this number to two by absorption of the sample-and-hold module. All the interface circuits are, accordingly, equally well suited in this respect. However the general purpose, voltage input ADCs require a preconditioning circuit to commit the ADC to a specific capacitance sensing function, as detailed in §2.1, *p* 20, increasing their area requirements.

Hitherto a target for silicon area requirements has remained to be established with the objective only loosely defined. The review of ADCs and interface circuits revealed area requirements of between $0.8mm^2$ and $4.6mm^2$. Minimum area

requirements can therefore be defined as belonging to the lower end of this range, i.e. less than $2mm^2$.

Thus far all the ADC-derived and free-running interface circuits have met the research objectives. Consideration of the operating temperature criterion permits some distinctions to be made among the circuits and techniques. The performance of all electronic circuits is influenced by temperature variation which is manifested in the deterioration of non-ideal circuit characteristics, for example leakage currents and offset voltages of operational amplifiers. Temperature measurement and compensation is one method of counteracting the effects. Clearly this approach requires additional circuitry to implement and should be avoided. The effect of temperature on performance was considered in a few of the above publications with Kjensmo *et al.* [37] relying on circuit matching to cancel any temperature-induced drift. Unfortunately the demands of close circuit and layout matching cannot easily be met with a standard-cell process. The negative feedback loop structure employed by Viswanathan *et al.* [72] compensates for temperature-induced variations in any component within the loop. Implementation with this particular technique, on the other hand, is possible with the standard-cell approach. The above performance comparisons are summarised below:

Performance Comparison		
Parameter	Objective	Published Achievements
Conversion time	20mS-100mS	2mS-20mS
Power consumption	<22.5mW	80μW-17mW
Resolution	10+ bits	8 to 16-bits
Capacitance size	20pF	greater than 2pF
Silicon area	$<2mm^2$	$0.8mm^2$ to $4.6mm^2$

Table 1

The centre column details each performance objective, with the corresponding specifications taken from the circuits reviewed above in the right-most column. Clearly the various switched-capacitor circuits are, in general, capable of meeting the target specifications.

Turning to the second question, which has been addressed to some extent in the assessment of the effects of temperature, other aspects of operation must be considered. Foremost is the need to have some parasitic-insensitive configuration. The stray-free integrator is the most obvious choice, since its practicability has been demonstrated by its frequent use in many of the circuits reviewed. The negative feedback loop structure of Viswanathan's *et al.* [72] frequency control loop, in addition to compensating for the effects of temperature, permits the use of lower-quality components within the loop.† Moreover the circuit, which can be configured to be stray-insensitive, does offer the prospect of being able to convert a low value capacitance ratio to frequency ratio. Indeed this circuit was developed as one of the three interface circuits for the prototype interface.

Several sources of error were common to many of the circuits detailed above, namely the offset voltage of operational amplifiers and comparators, and switch charge-injection and clock-feedthrough. This latter source of error was usually the more significant and is the subject of the remainder of this chapter.

† The capacitance ratio converter resulting from the research programme reported here is similar to the Viswanathan circuit. It was developed before the Viswanathan paper was discovered.

2.4 Charge-Injection and Clock-Feedthrough

The resolution of many of the interface circuits, reviewed in the previous chapter, was limited by the effects of charge-injection and clock-feedthrough. Experimental measurements made on a discrete component implementation of the prototype interface circuits, which are the subject of the investigations reported here, proved to be similarly limited. These findings are reported in §4.2, *p* 89.

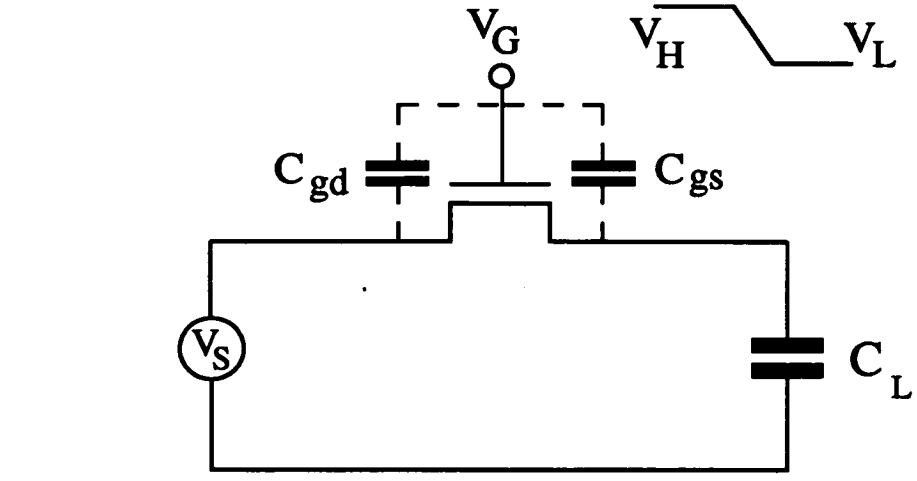
Charge-injection and clock-feedthrough occur during the turn-off of MOS switches. Referring to *Fig.* 15(*a*), two distinct phases of turn-off operation can be defined [73-75]:

- The gate voltage, V_G, is above the switch threshold voltage and a conduction channel of charges extends from the source to the drain of the transistor. As the gate voltage falls a proportion of the mobile channel charges flows to the source and drain nodes contributing to a charge error. This is termed *charge−injection*. Charge is also coupled via the gate-drain and gate-source overlap capacitances, C_{GD} and C_{GS}, to the source and drain nodes. This charge transfer mechanism is called *clock−feedthrough*.

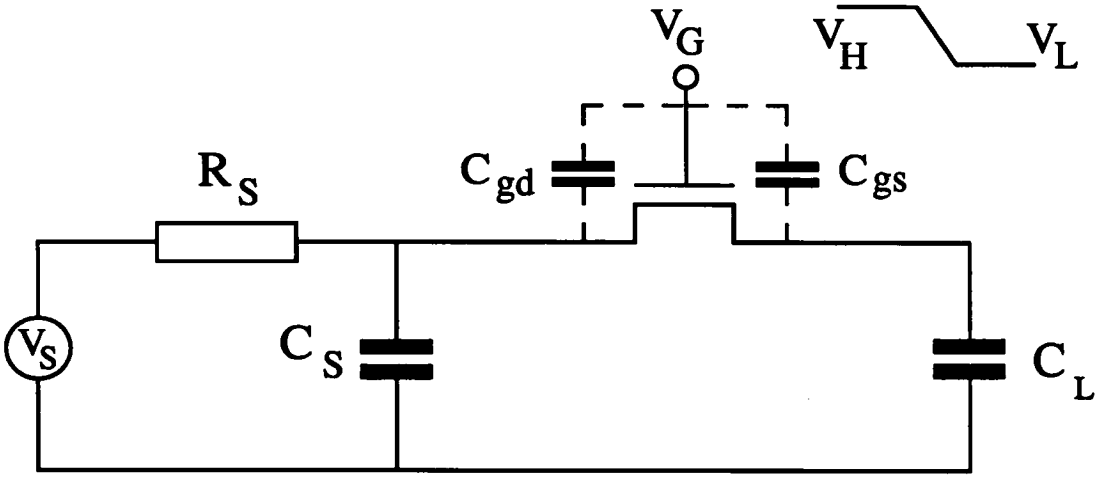
- The gate voltage is below the threshold voltage and the conduction channel has disappeared, i.e. the switch is off. Clock-feedthrough alone now contributes to the charge error.

The mobile channel charges exit into the substrate as well as to the source and drain nodes. This is termed charge-pumping and is usually insignificant [73, 74]. The operation of the two mechanisms is complex and depends upon several process and design parameters. FEEDTHROUGH EFFECTS UPON SWITCH TURN-ON ARE DISCUSSED IN §4.3.3, p107.

The terminology to describe the above two mechanisms was often confused in many of the publications under review with one or the other applied to describe their



(a)



(b)

Figure 15: Two switched-capacitor models, with **(a)** representing the simpler scenario, and **(b)** including the source resistance and capacitance

combined effect. In this thesis charge-feedthrough describes the combined effect of charge-injection and clock-feedthrough.

In the following section these two error mechanisms are examined in detail. Next, various clock feedthrough and charge injection cancellation schemes are reviewed and those that are inapplicable are discounted.

2.4.1 A Detailed Examination of Charge-Feedthrough

Charge-pumping was observed as early as 1969 when Brugler and Jespers [76] investigated this phenomenon concluding that it could set a limit upon the use of MOS transistors in charge switching applications. Later, clock-feedthrough was identified in one of the earliest switched-capacitor publications by McCreary and Gray [77] who stated feedthrough voltages to be a primary source of ADC linearity and offset error.

MacQuigg [78] was the first author to model the feedthrough error on a switched-capacitor. His semi-empirical model ignored the changing channel resistance during turn-off treating the channel as an on-off switch. *Fig.* 15(a) shows the switch circuit that was the subject of this investigation; note that V_S is an ideal voltage source with no series resistance and parallel capacitance. Later, the first analytical model was published by Sheu [73] demonstrating the dependence of feedthrough upon such factors as gate voltage falling rate, source voltage level, switch width and length, substrate doping, oxide thickness and source resistance. Two design equations were presented for the extreme cases of fast and slow gate voltage fall rate. Further work was described by Wilson *et al.* [79] in which the effects of source voltage, tub voltage, channel length and load capacitance on feedthrough were measured. A model was also presented. The model was divided into four sections, inversion, depletion-accumulation, accumulation-depletion and accumulation with the conclusion that the

feedthrough process is dominated by the inversion channel charge. Shieh *et al.* [74] and Wegmann *et al.* [80], generalised the feedthrough model by the inclusion of source resistance and capacitance. This model is shown in *Fig.* 15(*b*).

Feedthrough was modelled analytically by Sheu [73] for the simpler switching scenario shown in *Fig.* 15(*a*). The total error voltage on the switched-capacitor, C_L, was expressed for the extreme cases of fast and slow turn-off of an NMOS switch. For slow turn-off the error voltage, V_{dm}, is:

$$v_{dm} = -\left[\frac{C_{gd}+\frac{C_{ox}}{2}}{C_L}\right]\sqrt{\frac{\pi U C_L}{2\beta}}-\frac{C_{gd}}{C_L}(V_S+V_T-V_L) \tag{2.5}$$

when

$$\frac{\beta V^2_{HT}}{2C_L} >> U$$

where

$$\beta = \mu C_{ox}\frac{W}{L},$$

C_L is the load capacitance, C_{gd} is the gate-drain overlap capacitance, C_{ox} is the oxide capacitance, μ is the carrier mobility, W is the channel width, L is the channel length and U is the gate falling rate. The voltages V_S, V_T and V_L are the source voltage, the threshold voltage and the gate low voltage after turn-off, respectively. Re-expressing as the error charge, q_{dm}, on the load capacitor, C_L, *Eqn.* (2.5) becomes:

$$q_{dm} = -\left[C_{gd}+\frac{C_{ox}}{2}\right]\sqrt{\frac{\pi U C_L}{2\beta}}-C_{gd}(V_S+V_T-V_L) \tag{2.6}$$

Several parameters in *Eqn.* (2.6) can be considered to be constants: β is layout and process dependent; V_T is process dependent; and U and V_L are design dependent and not easily or usually modified. The feedthrough charge error is consequently a function of the oxide capacitance, C_{ox}, the overlap capacitance, C_{gd} and the source voltage, V_S. The error is also, but not so strongly dependent on the load capacitance, C_L.

For fast turn-off of an NMOS switch the error voltage, V_{dm}, is:

$$v_{dm} = -\left[\frac{C_{gd}+\frac{C_{ox}}{2}}{C_L}\right]\left[V_{HT}-\frac{\beta V^3{}_{HT}}{6UC_L}\right]-\frac{C_{gd}}{C_L}(V_S+V_T-V_L) \tag{2.7}$$

when

$$\frac{\beta V^2{}_{HT}}{2C_L} \ll U$$

where

$$V_{HT} = V_H - V_S - V_T,$$

and V_H is the gate voltage before turn-off.

Re-expressing again as the error charge q_{dm} on the load capacitor C_L *Eqn.* (2.5) becomes:

$$q_{dm} = -\left[C_{gd}+\frac{C_{ox}}{2}\right]\left[V_{HT}-\frac{\beta V^3{}_{HT}}{6UC_L}\right]-C_{gd}(V_S+V_T-V_L) \tag{2.8}$$

Similarly, β, U, V_H, V_L and V_T can be considered to be constants. Now, however, the error charge is negligibly dependent on C_L via the term $\frac{\beta V^3{}_{HT}}{6UC_L}$, if the switch arrangement is implemented with a typical CMOS process and C_L is of the order of 10pF. It should be noted that *Eqns.* (2.5) to (2.8) hold for a PMOS switch, but with a change of sign.

For both fast and slow switch turn-off rates a reduction in charge error can be accomplished by reducing C_{gd} and C_{ox}. The oxide capacitance, C_{ox}, scales with channel area, W × L, hence a small switch size is required. The gate-drain overlap capacitance, C_{gd}, varies with channel width, W. This indicates that implementing control switches with a small feature size process would result in a smaller charge error than that obtained from discrete switches. It should be noted that the charge error is temperature dependent through the threshold voltage, V_T, and the charge mobility, μ.

Furthermore Shieh *et al.* [74], have discovered that half the channel charge exits from the source node and half from the drain if the turn-off time, U, is fast. For slower turn-off times the equi-partitioning of charge is largely maintained provided the source resistance, R_S in *Fig.* 15(b), is small and the source capacitance, C_S, is matched moderately closely to the load capacitance C_L. If the source impedance increases with respect to the load capacitance a larger proportion of the charge is injected onto C_L.

Haigh and Singh [81] have reported that a reduction in clock-feedthrough can be effected by operating the switches in a particular order. Referring to the stray-insensitive capacitance-to-voltage converter in *Fig.* 16, the parasitic capacitances associated with M1 and M3, (i.e. C_{M1} and C_{M3}), do not contribute to the charge error if M2 and M4 open marginally before M1 and M3, respectively. It is presumed that the parasitic capacitances C_{M1}, C_{M2}, C_{M3} and C_{M4} consist of the gate-drain or gate-source overlap capacitance and any other inter-line capacitances. Although Haigh and Singh do not speculate on the effects of the clocking scheme on the channel charge, established as a contributor to the charge error, it can be concluded that the channel charge of devices M1 to M4 is similarly affected. If, for example, M2 turns-off first, the mobile charge in M1 is presented with an infinite impedance at C and exits towards the input voltage source, V_{in}. Likewise, the channel charge of device M3 exits towards ground. Thus the feedthrough, composed of channel charge and charge coupled via the overlap capacitance, is independent of the source voltage, since both source and drain of M2 and M4 are always at either earth or virtual earth potential irrespective of the value of V_{in}. This is confirmed by Robert *et al.* [82] although Cichocki and Unbehauen [69] confuse the issue by claiming that this technique compensates for clock-feedthrough.

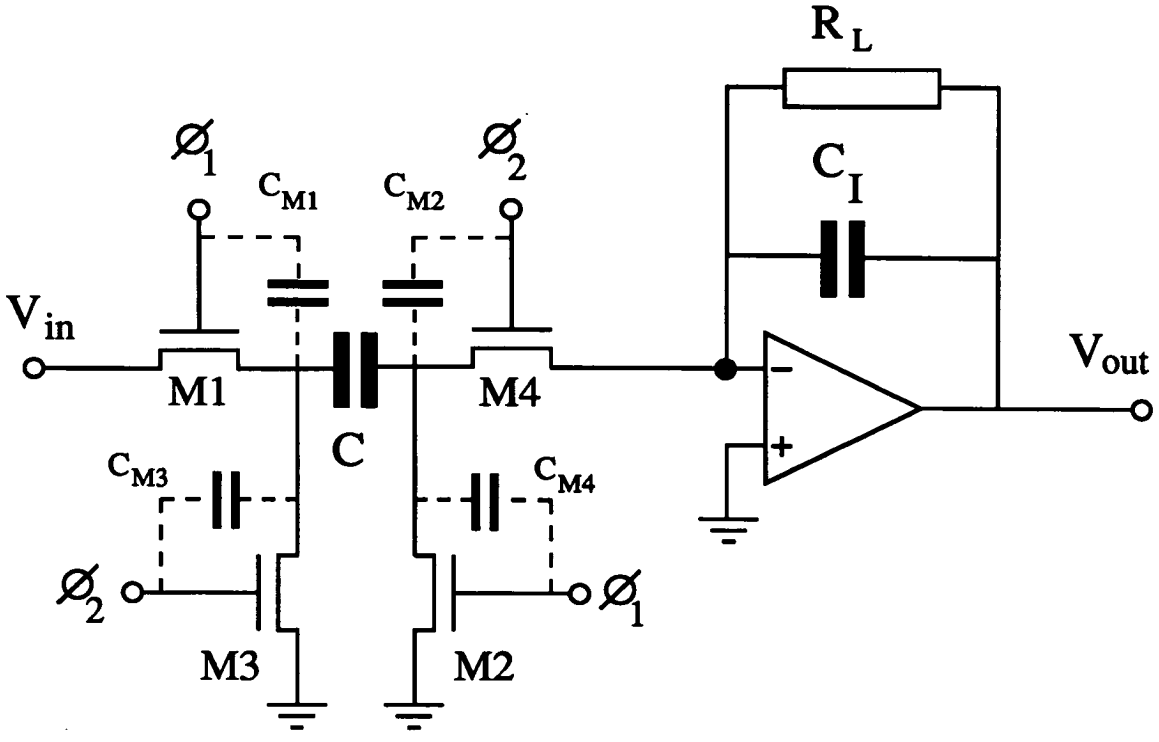


Figure 16: A SC capacitance-to-voltage converter with clock-feedthrough contributing gate-drain overlap capacitances included

2.4.2 Charge-Feedthrough Cancellation Schemes

Clock-feedthrough and charge-injection can be eliminated, or at least reduced significantly, by five different schemes. Each of these schemes will be described in turn and their usefulness considered.

The use of fully differential circuitry can effect a considerable reduction in clock-feedthrough and charge-injection [59]. This approach requires the use of fully-differential operational amplifiers, i.e. an amplifier with differential inputs and outputs, a component that is usually not found in a standard-cell ASIC library. Moreover parasitic insensitivity is lost, since the non-inverting input of the integrating operational amplifier can no longer be tied to ground, unless a more complex circuit arrangement is employed [83].

An alternative is to use the CMOS transmission gate [44]. This switch is constructed by placing an NMOS and a PMOS transistor in parallel and operated by driving their gate voltages in anti-phase to ensure that they are either both on or off. This configuration has two advantages over the single transistor switch. Firstly, the dynamic analogue signal range when the switch is on is increased to the power supplies. Secondly, there is some degree of clock-feedthrough cancellation. Good cancellation can be difficult to achieve, since it is dependent on matching of the NMOS and PMOS devices. Oxide capacitance, C_{ox}, charge mobility, μ, and threshold voltage, V_T are all different for NMOS and PMOS transistors. Inspection of *Eqn.* (2.6) and *Eqn.* (2.8) reveals that these parameters influence the magnitude of the charge error. In addition, the last two parameters, μ and V_T, are temperature dependent, making cancellation over the full industrial temperature more difficult to accomplish. The poor cancellation of discrete transmission gates was confirmed by experimental work reported in §4.3.2, *p* 100.

Two, more complex cancellation schemes have been proposed that compensate for operational amplifier input offset voltage as well as feedthrough. The first is a matched network scheme by Martin [84], and is shown in *Fig.* 17(a). The network, connected to the non-inverting input of the amplifier and comprising switches $M1$ and $M2$ and capacitors C_2 and C_3, injects an amount of charge equal to that injected by the input stage onto capacitor C_2. C_2 and C_1 must be matched for this technique to work; this is not possible when C_1 is a continuously varying sensor capacitance. In addition the matched network raises the potential of the non-inverting input thus removing the stray-insensitive properties of this arrangement.

The second technique is compensation using a sampled data network [82]. The compensated integrator is shown in *Fig.* 17(b) with the clock-feedthrough charge, q_c, shown entering node N. Closure of the switches marked '2' puts the circuit into an autozero mode. After the switches marked '0' discharge C_2, the switches in the input stage, designated ϕ_1 and ϕ_2, operate causing C_I to charge, V_{out} to change and an autozero voltage $V_a = -A_2V_{out}$ to be generated. To return to normal operation the switches marked '2' return to their former position. However as with the matched network technique, the potential at node N is raised thus disabling the stray-insensitivity. The autozero voltage could be used to modify the reference voltage, V_{ref}, thus maintaining parasitic-insensitivity, but this would probably require the use of additional operational amplifiers to make the scheme operable, increasing the device count and consequently area and power consumption.

The final and probably most simple scheme is dummy switch compensation. The earliest use of this technique was by Suarez *et al.* [77] and is illustrated in *Fig.* 17(c). The dummy switch, M2, with source and drain tied together has the same channel length as the control switch, M1, but half the channel width. Switches M1 and M2 are either both NMOS or PMOS devices and M2 is driven by an inverted version of the clock signal that drives M1. Hence, when M1 injects charge onto C_L upon turn-off M2 is turned on and removes the same amount of charge, since the amount of mobile

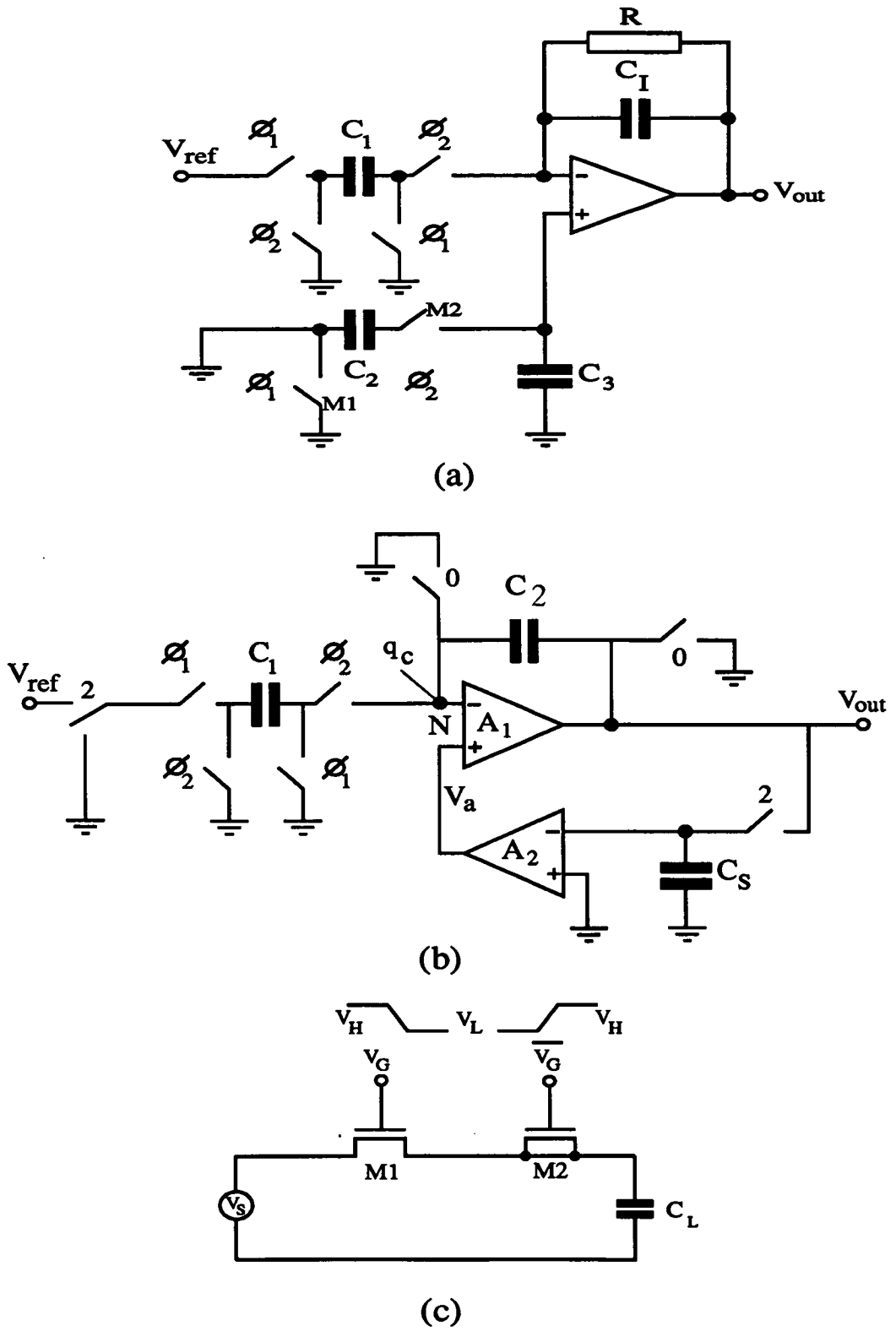


Figure 17: Three charge-feedthrough compensation schemes, **(a)** matched network compensation, **(b)** sampled data feedback compensation and **(c)** dummy switch compensation

channel charges is proportional to channel area. This assumes that an equal amount of channel charge exits from the source and drain of M1, as detailed in §2.4.1 above. A significant but unreported advantage of this approach is that the temperature dependent parameters, V_T and μ, should both track for M1 and M2 if the devices are situated together on the same substrate, providing compensation for charge-injection and clock-feedthrough over the industrial temperature range of operation. This technique provides the best solution to the clock-feedthrough and charge-injection errors.

Eichenberger and Guggenbuhl [75] have recently reported investigations into the feasibility and limits of dummy switch compensation. Eichenberger and Guggenbuhl state that if the switching time, U, is of the order of the intrinsic channel transit time of the switch, compensation is guaranteed even for asymmetric source and drain impedances. The channel transit time, T_O, is the longest time needed by mobile charges to reach one end of the channel [80], and is proportional to the channel length, L, and the on value of the gate voltage, V_H in *Fig.* 15, *p* 58:

$$T_O = \frac{n_o L^2}{\mu(V_H - V_T)} \tag{2.9}$$

where

$$n_o = 1 + \frac{\gamma}{\sqrt{\Phi_f}},$$

γ is the body effect parameter, Φ_f is the Fermi level, μ is the carrier mobility and V_T is the threshold voltage. The dependence of the channel transit time on channel length and its effect on injected channel charge with respect to turn-off time make it desirable for both the controlling switch, M1 in *Fig.* 17(*c*), and and the dummy switch, M2, to have the same channel length as detailed above. As a result, scaling of the channel area of M2, with respect to M1, should be accomplished by varying the channel width. Eichenberger and Guggenbuhl have also found that the time delay in operation of the dummy switch, with respect to the control switch, significantly influences the effectiveness of the cancellation. Typically, good cancellation of feedthrough can be obtained

with simultaneous switching, i.e., no time delay.

2.5 Chapter Summary

Serial and binary-search, general purpose analogue-to-digital converters have been described and reviewed. Switched-capacitor interface circuits derived from the general purpose A-to-D converters were then discussed as a more compact but specialised solution to the conversion of capacitance variation to a binary digital word. The frequency or duty-cycle output interface circuit was introduced as the third category of interface or converter circuit.

The converter and interface circuits were evaluated as to the general suitability of switched-capacitor techniques for capacitance sensing by analysing each performance objective, stated in §1.5, *p* 17, in turn. As summarised in *Table* 1, the required power consumption, and data-acquisition or conversion time, are both attainable. The published circuits performed less satisfactorily as regards resolution, particularly at low sensor capacitance, with Krummenacher's full-custom integrated circuit [70] the exception. However several authors indicated that up to 14-bit resolution might be attainable from integrated versions of their respective circuits with charge-feedthrough compensation. Target silicon requirements, which hitherto had been only loosely defined, were specified drawing upon the requirements of the ADCs and interface circuits under review.

A standard-cell approach to the design of high-precision integrated interface circuits, with its library of analogue components of limited performance, was not employed in any of the publications under review. As discussed in §1.3, *p* 5 standard-cell analogue library components are not designed for high precision applications. Interface circuits are required that can overcome these limitations and achieve the required precision.

The negative feedback loop structure, which features in Viswanathan's *et al.* frequency control loop [72], was selected to this end.

Charge-feedthrough, the primary source of error in many of the circuits under review, was discussed and compensation schemes detailed. Of these schemes, the dummy switch technique was selected as that most suited to the present application.

In the next chapter the interface circuits selected for investigation are presented and their first order behaviour analysed.

Chapter 3
ASIC CMOS Sensor Interface Circuits

3.1 Introduction

Of the ADC-derived and free-running interface circuits reviewed in *Chapter* 2 one, the frequency control loop illustrated in *Fig.* 14,*p* 50, was considered to have the attributes required of a switched capacitor interface circuit for capacitance ratio sensing that is capable of being integrated with a standard-cell ASIC process. In this chapter, the operation of a modified version of this circuit will be described and the first-order, steady-state behaviour modelled. Two other similar circuits that complete the family of three interface circuits under investigation will also be presented: one is an absolute capacitance-to-voltage converter circuit; the other, the voltage control loop, converts capacitance ratio to voltage. The first order behaviour of these two circuits will be analysed. Focusing on the frequency control loop, some notable aspects of operation will be considered including frequency counting strategies and circuit sensitivity. The first-order frequency control loop model is then modified to take operational amplifier imperfections into account. Finally, a brief assessment of noise and aliasing problems is made and the implications for interface circuit design determined.

3.2 SC Interface Circuits for Capacitance Ratio Sensors

An interface circuit with a remote capacitance sensor should be insensitive to the stray capacitance associated with the sensor to interface wiring. The switched-capacitor integrator was identified in *Chapter* 2 as having the necessary stray-insensitive properties [63, 66, 70]. The absolute capacitance measuring instrument proposed by Huang

et al. [41], and first introduced in §2.2, *p* 25, is based on this switched-capacitor, stray-insensitive integrator. This transducer achieves high sensitivity and stability in addition to parasitic insensitivity and is suitable for integration onto an IC using a CMOS process [41]. Inspection of Viswanathan's *et al.* frequency control loop [72], shown in *Fig.* 14, *p* 50, and comparison with Huang's *et al.* circuit of *Fig.* 8(*b*), *p* 26 reveals that the former circuit is composed partially of the latter. The stray-insensitive integrator, applied as a capacitance-to-voltage converter, was accordingly selected as one of the three interface circuits as an aid to the characterisation of the frequency control loop, over and above its application as an absolute capacitance sensor circuit.

The second circuit, the switched-capacitor frequency control loop has, as was discussed in §2.3.4, *p* 52, the potential, upon modification, to be implemented as an IC with a standard-cell ASIC process, whilst achieving high accuracy. This circuit uses the switched-capacitor integrator in a feedback loop comprising the switch block and a VCO, and an input resistor, as illustrated in *Fig.* 14, *p* 50. Soft non-linearity or temperature dependence in the input-output relationship of the VCO does not affect accuracy by virtue of the feedback loop. This closed loop technique was previously used by Abidi [85] to linearise the voltage-frequency characteristics of any voltage controlled oscillator (VCO). The oscillation frequency is also insensitive to power supply or temperature variations.

Viswanathan *et al.* suggested that the control loop could be modified to function as a capacitance ratio to frequency ratio converter by replacing the resistor R in *Fig.* 14, *p* 50 by a second switch block, driven by a reference frequency, followed by a current averaging network. The value of including the current averaging network is not apparent and the circuit can in fact function adequately without it. The second, resultant interface circuit is illustrated in *Fig.* 18.

A more compact circuit, termed a voltage control loop, that has a voltage output but no frequency output can be created by removing the VCO and applying the

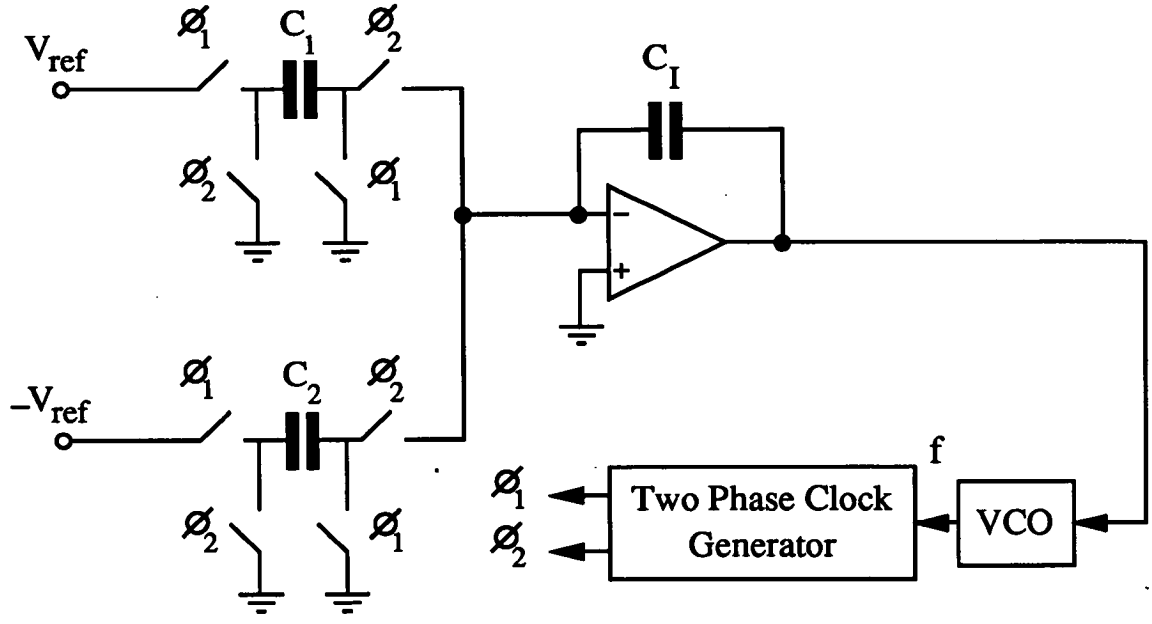


Figure 18: The SC frequency control loop

voltage at the output of the amplifier to the feedback switch block. Both switches are now driven by the same reference frequency. This third and final circuit is shown in *Fig.* 19.

The design of a family of interface circuits suitable for integration using a standard-cell CMOS process has been facilitated by the use of a closed loop structure and the familiar switched-capacitor integrator. In the following section first order expressions describing the operation of the three interface circuit types will be derived.

3.3 A Family of Switched-Capacitor Circuits for Capacitance Sensors

In this section the operation of each of the three interface circuits is described in turn and expressions that model the steady-state behaviour of each circuit derived. The order of treatment is: capacitance-to-voltage converter, frequency control loop and voltage control loop.

3.3.1 The SC Capacitance-to-Voltage Converter

Fig. 20(*a*) shows a non-inverting SC capacitance-to-voltage converter. The switch block comprising switches M1 to M4 is driven by a two-phase non-overlapping clock: the switches marked ϕ_1 close together whilst those marked ϕ_2 are open and vice-versa. A stream of charge pulses flows out of the amplifier nodal point and is integrated on the amplifier. Assuming the frequency content of the capacitance variation to be much lower than the switching clock rate the mean current flowing out of the amplifier nodal point:

$$i = \frac{V_R C}{T} = V_R C f \tag{3.1}$$

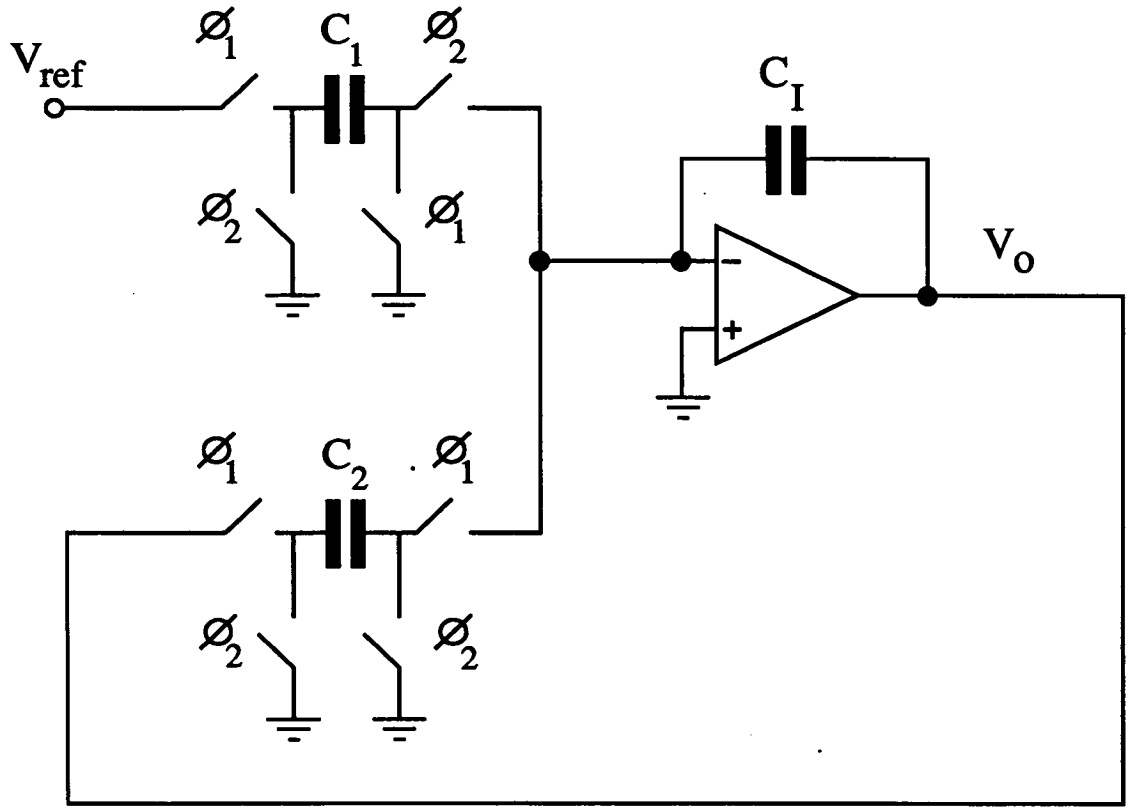


Figure 19: The SC voltage control loop

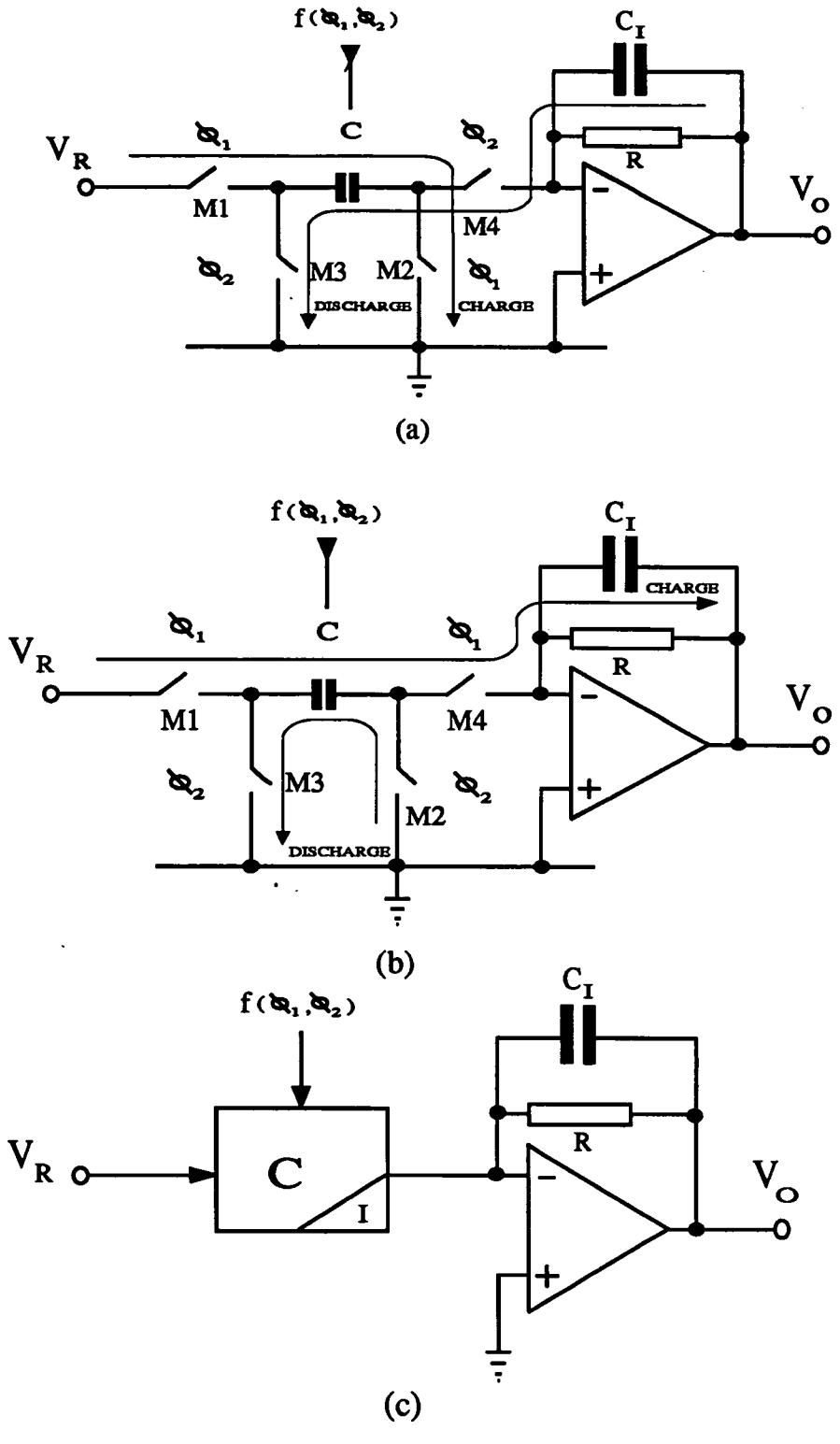


Figure 20: Three SC capacitance-to-voltage converters, **(a)** non-inverting, **(b)** inverting, and **(c)** a block representation of **(b)**

where T is the clock period and $\frac{1}{T}$ the clock frequency.

The output voltage, assuming a large integration time constant, $T = RC$, with respect to the switching frequency, is given by:

$$V_O = iR = V_R CfR \tag{3.2}$$

An inverting version of this circuit can be implemented by changing the clocking scheme as shown in *Fig.* 20(b). For illustrative purposes the non-inverting and inverting switch blocks will be represented as shown in *Fig.* 20(c) with the 'I' indicating that the block is inverting.

3.3.2 The Frequency Control Loop

Fig. 21(a) shows the frequency control loop. This circuit is essentially a negative feedback loop with the input voltage of the VCO controlled by the operational amplifier output in such a way as to force the currents summed at the virtual earth to zero. When a single reference voltage is used, as illustrated in *Fig.* 21(b), the inverting and non-inverting forms of the switch array are connected in parallel.

Considering *Fig.* 21(c), when the circuit is in steady state:

$$V_1 C_1 f_1 - V_2 C_2 f_2 = 0 \tag{3.3}$$

Hence:

$$V_1 C_1 f_1 = V_2 C_2 f_2 \tag{3.4}$$

and

$$\frac{f_2}{f_1} = \frac{C_1}{C_2}\frac{V_1}{V_2} \tag{3.5}$$

Thus this circuit can be operated either as a capacitance ratio to frequency ratio converter or as a voltage to frequency ratio converter. For this latter mode of operation

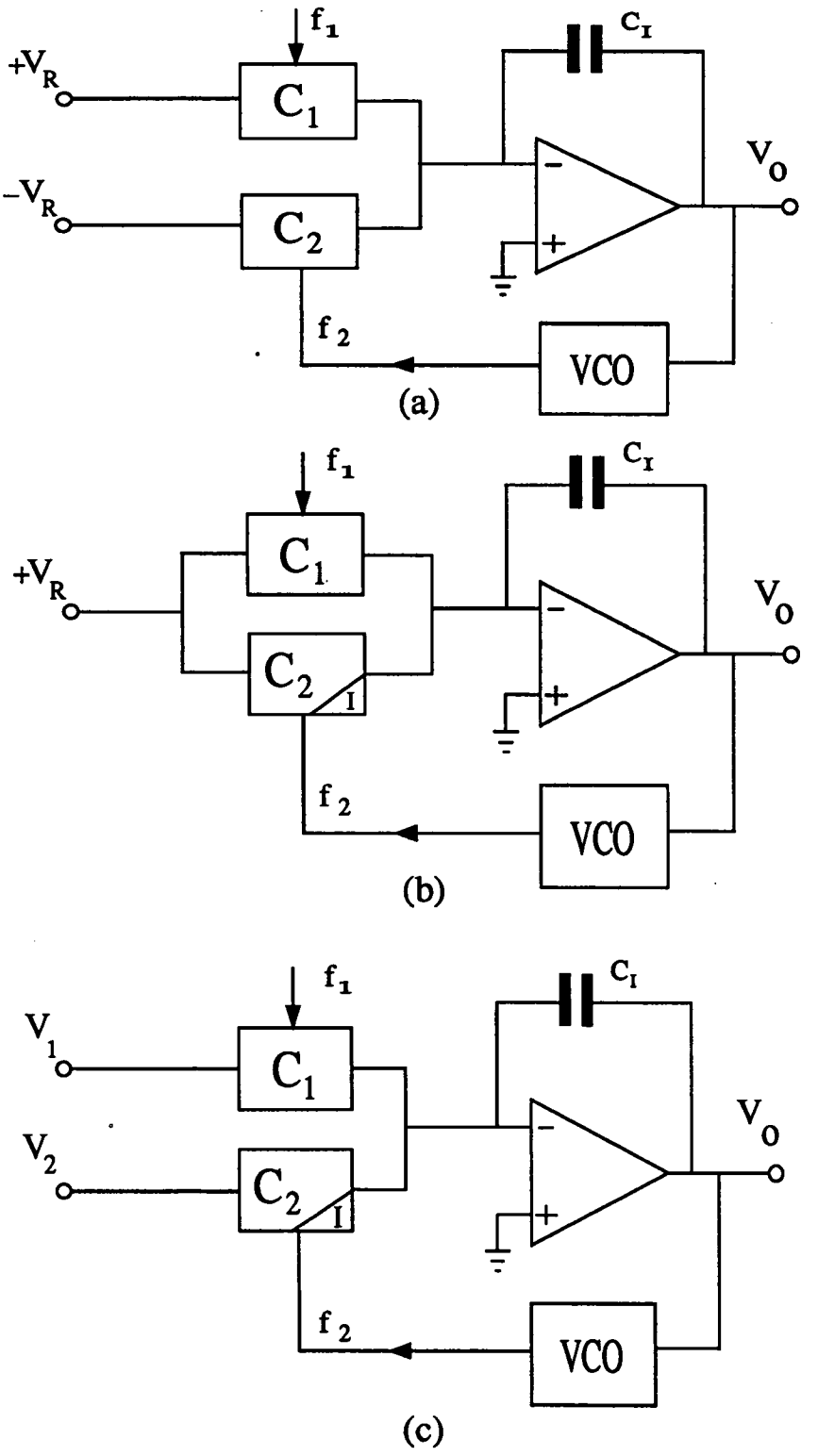


Figure 21: Three switch phasing dependent implementations of the SC frequency control loop

C_1 and C_2 are matched external capacitances and V_1 and V_2 can be a sensor output voltage and a reference voltage respectively.

For the capacitance ratio mode $V_1 = V_2 = V_R$:

$$\frac{f_2}{f_1} = \frac{C_1}{C_2} \tag{3.6}$$

After conversion of f_1 and f_2 to digital words, N and n respectively, by pulse counting:

$$\frac{n}{N} = \frac{C_1}{C_2} \tag{3.7}$$

The sensitivity of the converter can be increased by the inclusion of a frequency divider in the feedback path.

The balance equation now becomes:

$$V_R C_1 f_1 = \frac{V_R C_2 f_2}{D} \tag{3.8}$$

where D = frequency divider.

Hence:

$$\frac{f_2}{f_1} = \frac{DC_1}{C_2} \tag{3.9}$$

Later experimental work, reported in §4.4.3, *p* 120, demonstrated the inclusion of the divider to be effective in reducing frequency locking and jitter by separating the operating frequency range of the VCO, f_2, from the reference frequency, f_1. The integrating capacitance C_I ensures that the current balance equation is obeyed. C_I must be large enough to act as a smoothing component but not so large as to impair the transient performance of the circuit.

3.3.3 The Voltage Control Loop

The voltage control loop, shown in *Fig.* 19, *p* 74, is the capacitance ratio converter described above with the VCO removed and the voltage at the output node of the amplifier applied to the feedback switched-capacitor block. f_2 is supplied by an external reference frequency and whilst one of the switch stages is inverting the other is non-inverting. The balance condition is the same as that for the capacitance ratio circuit. When $f_2 = f_1$ *Eqn.* (3.4) becomes:

$$\frac{V_2}{V_1} = \frac{C_1}{C_2} \tag{3.10}$$

The corresponding expression for *Fig.* 19 is:

$$\frac{V_O}{V_{ref}} = \frac{C_1}{C_2} \tag{3.11}$$

This circuit could be used in conjunction with a general purpose ADC to produce a digital word that characterises the capacitance ratio, $\frac{C_1}{C_2}$.

3.4 Notable Aspects of Frequency Control Loop Operation

In this section some notable aspects of operation of the frequency control loop are considered.

Inspection of *Fig.* 21(*a*) reveals that a positive reference voltage, $+ V_R$, and a negative reference voltage, $- V_R$, are required. Unfortunately the circuitry needed to derive the negative reference from the positive reference voltage, or vice versa, is likely to be subject to time and temperature drifts. In addition, the circuitry would probably be affected by static process dependent errors, by offset voltages for instance, if an operational amplifier is used. The configuration shown in *Fig.* 21(*b*) circumvents this

problem by using one inverting and one non-inverting switched-capacitor stage permitting the use of the same voltage reference for both stages.

The frequency output of the frequency control loop, f_2 in *Fig.* 21, needs according to *Eqn.* (3.7) to be converted to a digital word as does the reference frequency, f_1. This can be achieved by the counting of the VCO output frequency, f_2, over a fixed time interval; a count time that is a multiple of 20mS is required to reject 50Hz pick-up. Alternatively a fixed number of f_2 pulses can be counted over a variable time interval; this method does not remove the effects of 50Hz pick-up. Another reference frequency, f_3, is essential to implement both methods. This second reference frequency should be derived from f_1, or vice versa.

The two frequency counting methods impose different constraints on the values of f_2 and f_3 if a resolution better than 10-bits is to be achieved. If a fixed-time count is employed with a desired accuracy of 10-bits in 20mS, then f_2, the variable frequency must be greater than 50kHz. In contrast f_3, which determines the fixed 20mS count time, can be much lower. The second method is to count a fixed number of f_2 pulses. Now the VCO output frequency, f_2, does not have a minimum frequency constraint because it is subject to a fixed pulse count; f_3 however must exceed 50kHz. The second method, with the whole control loop operable at a lower frequency, could potentially have a lower power consumption. Unfortunately the necessity to have 50Hz rejection renders it unusable. The resolution of the frequency control loop scales with the conversion time. For example, assuming f_2 to be 100kHz and a conversion time of 20mS an accuracy of 11-bits is possible; with a conversion time of 40mS the accuracy is 12-bits.

Sensor capacitance ratio variation is typically small, limiting the sensitivity of the frequency control loop. The Taylor Instrument 400T differential pressure transmitter, for example, has a change of approximately 12% in $\frac{C_1}{C_2}$ from zero to full scale [10].

According to *Eqn.* (3.6) an equivalent variation in $\frac{f_2}{f_1}$ would result. Including a divider could, as *Eqn.* (3.9) above illustrates, make more use of the dynamic range of the circuit and increase resolution. To illustrate this effect consider the frequency control loop with f_1 and f_2 at 100kHz. Assume a variation of 12%. With a fixed count time of 20mS a maximum count of 2240 is obtained at a full scale frequency, f_2, of 112kHz. The resolution is 0.044%. If a divide by two module is included after the VCO a maximum count of 4480 at a full scale frequency of 224kHz is obtained; this corresponds to a resolution of 0.022%. In conclusion, the divider increases the flexibility of the circuit improving resolution when the full dynamic range is not used.

The scale factor, N in *Eqn.* (3.7) could be made programmable to maximise accuracy and to utilise the dynamic range of the frequency control loop, by employing a two-stage frequency conversion. To minimise the total conversion time the first phase of the conversion could be a short, low accuracy pulse count. Now, knowing the approximate value of f_2, N could be adjusted to improve the accuracy obtainable from a fixed-time count. Alternatively, the first short low-accuracy count could be used to shorten the count time, for example from 100mS to 20mS, if a faster conversion was required.

3.5 Operational Amplifier Imperfections in the Frequency Control Loop

The integrating operational amplifier has two significant imperfections that degrade the performance of the frequency control loop: input offset voltage and input bias current. The effect of each will be considered in turn.

The frequency control loop is illustrated in *Fig.* 22(*a*) with the input offset voltage modelled as a voltage source, V_{os}, at the non-inverting input of the operational amplifier. The switches associated with C_1 are operated for non-inverting integration

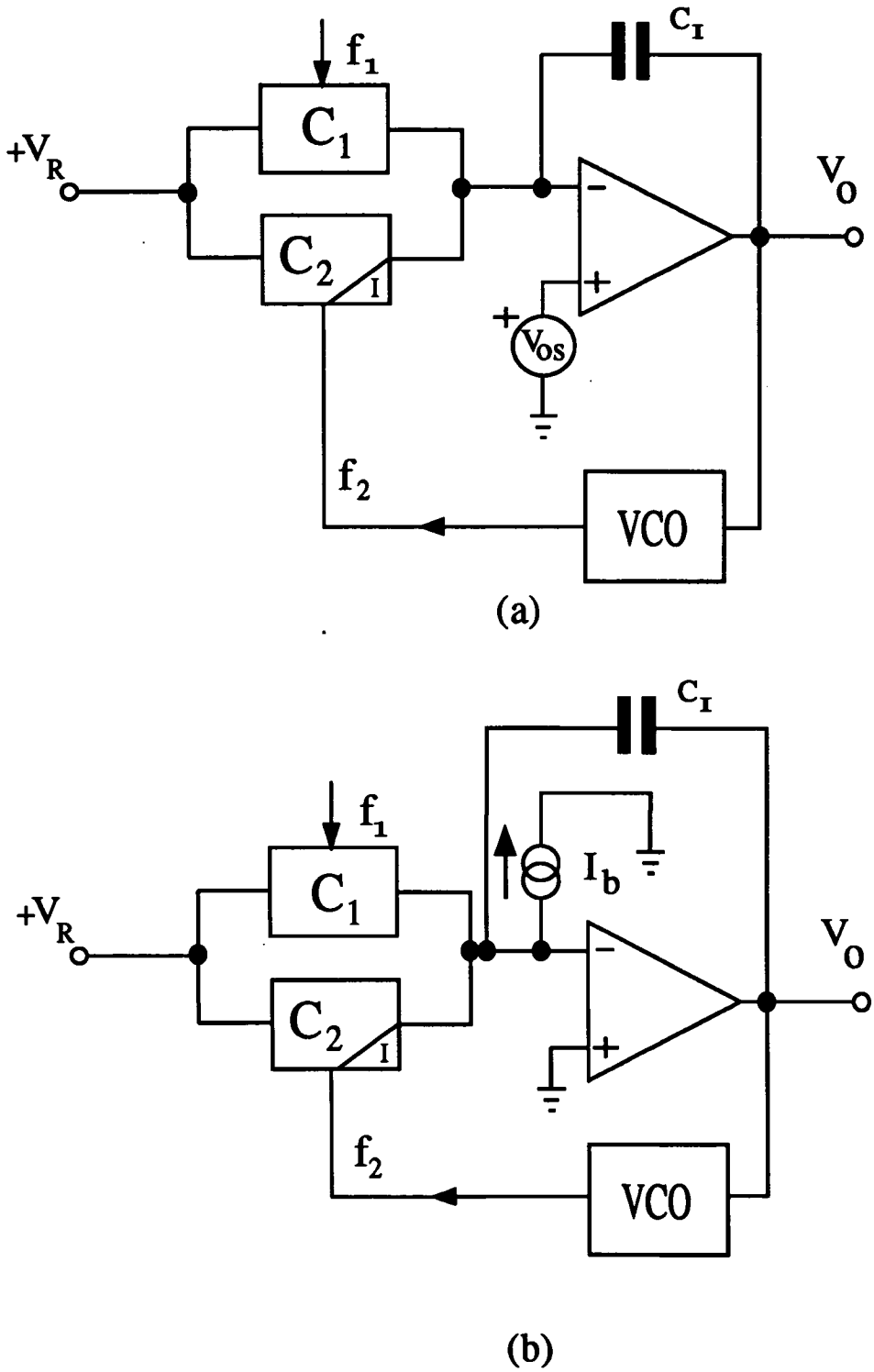


Figure 22: The SC frequency control loop including in **(a)** a model for the operational amplifier input-offset voltage, and in **(b)** the input bias current

of the positive reference voltage, V_{ref}. Those associated with C_2 are operated, conversely, for inverting integration of the same V_{ref}. During steady-state operation a charge balance is maintained at the inverting input of the operational amplifier:

$$(V_{ref} - V_{os})C_1 f_1 + (-V_{ref} - V_{os})C_2 f_2 = 0 \tag{3.12}$$

Rearranging to make the frequency ratio the subject of the relationship:

$$R_1 = \frac{f_2}{f_1} = \frac{C_1(V_{ref} - V_{os})}{C_2(V_{ref} + V_{os})} \tag{3.13}$$

Thus the offset voltage is manifested as gain error in the otherwise linear relationship between capacitance and frequency ratio. For a reference voltage of 1.5 volts and a typical offset voltage of 5mV the resultant gain error is approximately 0.7%. This value is larger than the industrially specified 0.1% accuracy. The effect of the offset voltage can be removed by using a technique proposed by Viswanathan *et al.* [72]. If the sequence of operation of the switches in the C_1 and C_2 stages are exchanged, to make the reference switch stage inverting and the feedback switch block non-inverting, then re-evaluating:

$$R_2 = \frac{f_2}{f_1} = \frac{C_1(V_{ref} + V_{os})}{C_2(V_{ref} - V_{os})} \tag{3.14}$$

Now, if one count of f_2 is taken with the first switch sequence and one with the second an offset voltage independent frequency ratio, R, can be obtained at the cost of an increased conversion time, where

$$R = \sqrt{R_1 R_2} \tag{3.15}$$

The input bias current can be modelled as a current source, I_b as illustrated in *Fig.* 22(b). Now the balance equation becomes:

$$V_{ref} C_1 f_1 - V_{ref} C_2 f_2 + I_b = 0 \tag{3.16}$$

Hence:

$$\frac{f_2}{f_1} = \frac{C_1}{C_2} + \frac{I_b}{f_1 V_{ref} C_2} \tag{3.17}$$

The offset error cannot unfortunately be calibrated out or eliminated since it is dependent on one of the varying measurement capacitances. For $V_{ref} = 1$ volts, $C_2 = 10pF$, $f_1 = 10kHz$, and for $I_b = 1pA$ [52] a value typical of a CMOS operational amplifier, the error is insignificantly small at 0.001%. The bias current is however temperature dependent approximately doubling for every 10° C increase in temperature [52]. Thus for an increase from ambient temperature to 80° C, the bias current increases sixty-four-fold with a proportional increase in the offset error to 0.064% - close to the industrially specified resolution. Inspection of *Eqn.* (3.17) reveals that the reference frequency, f_1, is the only significantly variable parameter capable of reducing the effects of the bias current. Consequently a lower limit is set on f_1.

3.6 Noise and Aliasing

The resolution of all the SC interface circuits is limited by internally generated circuit noise and by noise contributed by the sensor capacitance. The two main sources of circuit noise are thermal (or Johnson) noise and 1/f (or flicker) noise. Thermal noise has a flat, i.e. frequency independent, spectral density up to 10^9Hz or more [86]. 1/f noise has a spectral density that varies inversely with frequency and predominates over thermal noise below the corner frequency f_{cr}. f_{cr} is typically 10kHz for MOS circuits [83]. The noise contributed by capacitive sensors that are based upon deformable diaphragms is mechanical in origin and is due to the excitation of the diaphragm by broadband molecular activity and by high frequency process fluctuations [86]. Sensors are mechanically designed so that this source of noise is insignificant compared with the internal circuit noise.

The sampling action of the switched-capacitor stage of each of the interface circuits causes the undersampling of noise that is of a frequency that is greater than half that of the clock-rate, namely the aliasing effect, thus raising the noise floor and reducing the possible resolution. Careful design can minimise the problem. For example selection of a clock frequency that is at least 2 f_{cr}, i.e. 20kHz, prevents aliasing of 1/f noise. Aliasing of thermal noise will increase the noise level. Gregorian and Temes [83] have shown that the power spectral density (PSD) of the low frequency thermal noise is multiplied by $\frac{2f_{noise}}{f_c}$, where f_c is the clock frequency and f_{noise} is the bandwidth of the thermal noise after being bandlimited by the circuit.

The noise bandwidth, f_{noise}, is determined by the time constant of the on-resistance of the switches multiplied by the sensor capacitance, and by the operational amplifier bandwidth. Two independent bandlimiting processes occur during one complete, two-phase clock cycle. The first bandlimiting effect occurs in the non-inverting SC integrator of *Fig.* 20(*a*),*p* 75, whilst ϕ_1 is high. Noise that is subject to the bandlimiting effect during this phase is contributed by switches M1 and M2 with the resultant direct noise bandwidth given by [83]:

$$f_{sw} = \frac{1}{4R_{ON}C} \tag{3.18}$$

where R_{ON} is the combined on-resistance of switches M1 and M2, and C is a sensor capacitance. For a wide and hence low on-resistance NMOS switch fabricated in a typical CMOS process, R_{ON} = 200Ω [44]. C, the sensor capacitance is outwith design control and will typically be of value 20-70pF [10]. Letting R_{ON} = 200Ω and C = 20*pF* in *Eqn.* (3.18) results in a direct noise bandwidth of 62.5MHz, a figure that has a negligible bandlimiting effect. Increasing R_{ON} to decrease f_{sw} increases the thermal noise power density of the switches and the two effects cancel. Thus the clock frequency, f_c, is the only means of control over the aliasing of thermal noise during this first bandlimiting phase.

The second phase occurs whilst ϕ_2 is high and is subject to the bandlimiting effect of both the operational amplifier and the rise time on C, and M3 and M4. For the operational amplifiers available with the standard-cell ES2 Solo 1200 process, $f_o << f_{sw}$. The key bandlimiting element during the second phase is therefore the operational amplifier.

In conclusion, a high clock frequency reduces aliasing of thermal noise during the first phase, and a high clock frequency and a low operational amplifier bandwidth reduce aliasing during the second phase. However the integrator settling time requirement imposes a lower limit on the operational amplifier bandwidth: Gregorian and Temes suggest $f_o >= 5\ f_c$ [83]. A bandwidth lower than this suggested limit would result in a resolution limiting ripple in the integrator output voltage, and a failure of the stray-free charge transfer mechanism, as a consequence of the loss of the virtual earth at the inverting input of the integrating operational amplifier.

Drawing from the above discussion the preliminary recommendations for operation of the three interface circuits are a clock frequency that is greater than 20kHz, to prevent aliasing of 1/f noise, and the observation of the clock frequency-operational amplifier bandwidth limit. A fuller treatment of noise and aliasing should include an noise analysis during the two phases of operation of the circuits supported by measurements. This area of investigation was not considered to be a priority in the characterisation of the interface circuits and on account of time constraints remains as part of a plan for future work.

3.7 Chapter Summary

Three interface circuits that are suitable for implementation in an integrated form using a standard-cell CMOS process have been presented. All three circuits are based

upon the stray-insensitive switched-capacitor integrator, where the switched capacitor is an external sensor capacitance. First-order steady-state expressions were derived for each circuit. Several notable aspects of operation of the frequency control loop were highlighted including reference voltage and clock drifts and frequency counting strategies. The effect of operational amplifier imperfections on the frequency control loop performance was also considered. Finally, noise and aliasing in the interface circuits was discussed and the implications for interface circuit design discussed.

Before an integrated circuit design of the three interface circuits was attempted the above circuits were constructed in discrete component, bread-board form to verify the validity of the first order expressions derived in this chapter. These experimental investigations and results are the subject of the next chapter.

Chapter 4
Discrete Implementation of the Interface Circuits

4.1 Introduction

Three switched-capacitor interface circuits were presented in *Chapter* 3 where basic first-order steady-state models were derived for each circuit. As was stated in §1.5, *p* 17, a primary research objective is the fabrication of the three circuits using a standard-cell ASIC CMOS process. However, before committing the designs to silicon the validity of the first-order models was tested experimentally with discrete bread-boarded versions of two of the three circuits, namely the SC capacitance-to-voltage converter and the frequency control loop. This approach permits rapid and inexpensive prototyping of the interface circuits preventing the waste of ill conceived silicon design. A further benefit of this approach is that it allows errors due to second order effects to be quantified experimentally. A difficulty and disadvantage associated with this approach, which must be taken into consideration, is that of variable and difficult to quantify parasitic components.

The results from the discrete experimentation are presented in this chapter, including an investigation into charge-feedthrough, which is identified as the primary cause of error in the two interface circuits. The first-order models, derived in *Chapter* 3, are modified to include the effects of charge-feedthrough and the resultant second-order models are demonstrated to predict circuit behaviour with good accuracy.

The chapter concludes with a consideration of several aspects of performance of the frequency control loop, namely locking and jitter, power consumption and transient response.

4.2 Steady-State Measurements on Discrete Implementations of the Interface Circuits

4.2.1 Section Introduction

The SC capacitance-to-voltage converter and the frequency control loop were constructed using components from ES2's analogue library, which for experimental purposes were provided as two user-configurable evaluation ICs [87]. Since only two switches were available on the evaluation ICs, standard CMOS 4000 series M4016 quad transmission gates were used to implement the switch block [88]. Likewise the two-phase clock generator, illustrated in *Fig.* 23, was constructed with 4000 series CMOS gates on account of the absence of standard logic. The delays, t_1 and t_2, between the two phases, ϕ_1 and ϕ_2, were controlled by the time constants R_1C_1 and R_2C_2, respectively. Both t_1 and t_2 were set at approximately 2μS. A set of silvered mica capacitors of value 5pF to 270pF was selected for use as measurement capacitors.

Several layout techniques were employed to minimise the effects of capacitively coupled noise [89]. These included: constructing the circuits on a copper-plated board that functions as a ground plane; separation and decoupling of analogue and digital power supplies [83]; keeping leads as short as possible; and using shielded cables for clock inputs and long lines.

The experimental results for the SC capacitance-to-voltage converter will now be presented followed by those for the frequency control loop.

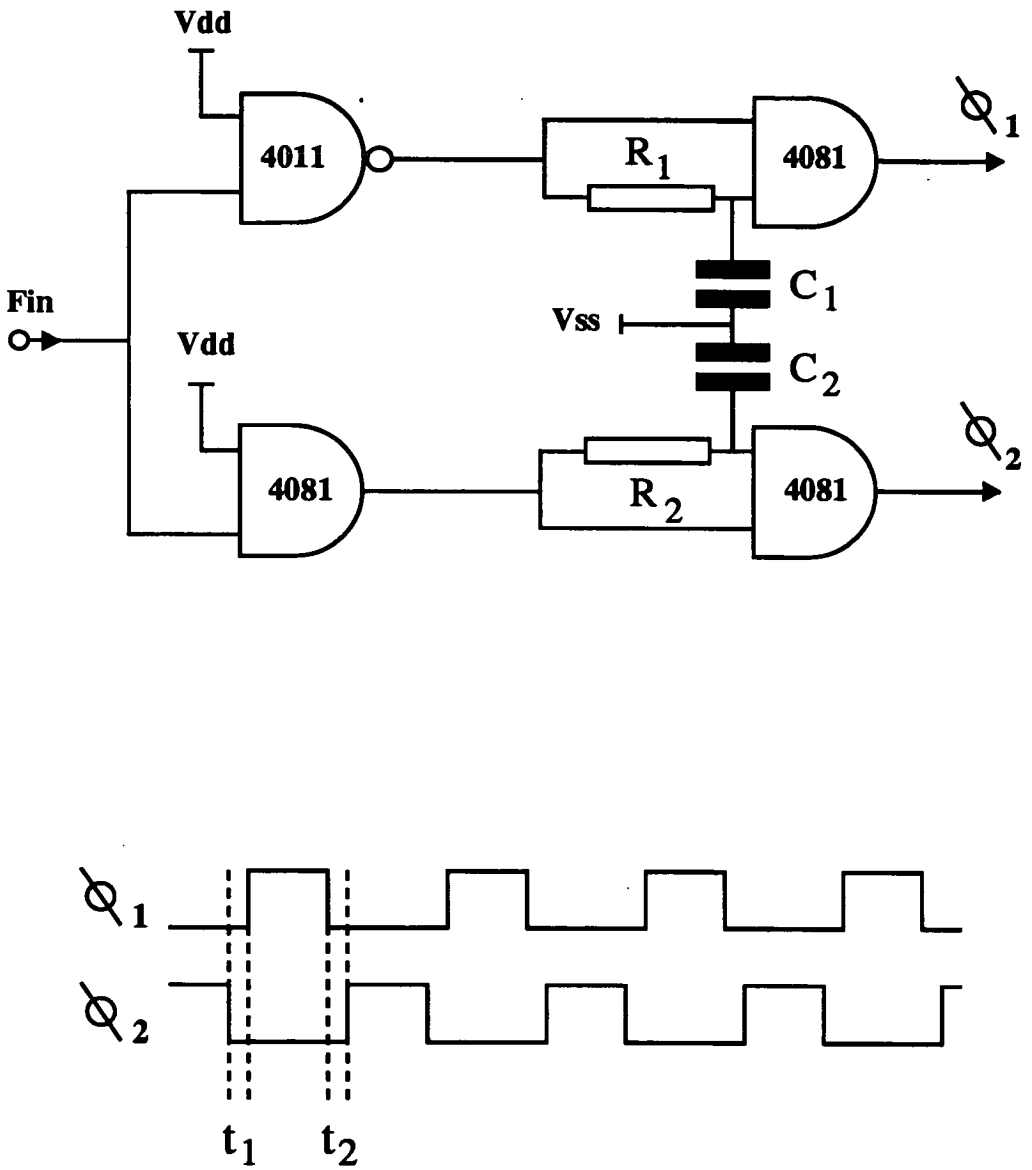


Figure 23: A two-phase clock generator circuit

4.2.2 The SC Capacitance-to-Voltage Converter

The steady-state behaviour of the SC capacitance-to-voltage converter, illustrated in *Fig.* 20, *p* 75, is modelled by *Eqn.* (3.2) for non-inverting operation of the switches:

$$V_O = V_R f R_f C$$

The relationship between V_O and C, V_R and f was determined for the non-inverting configuration of the circuit. OP-22 [23], a high drive operational amplifier with large output voltage swing was selected from one of the ES2 evaluation ICs as the integrating amplifier. *Appendix A.* 1, *p* 182 contains data for OP-22. The resistor R_f was of value 916 kΩ and C_f was a 0.22μF polyester capacitor. One two-phase clock generator circuit, described in §4.2.1 above, was used to drive switches M1 to M4.

The measurements made on the SC capacitance-to-voltage converter are shown plotted in *Figs.* 24, 25 and 27 and designated by 'O' along with plots generated from the non-inverting, first-order equation, *Eqn.* (3.2), designated by 'X'. *Fig.* 24, SC capacitance-to-voltage converter output voltage, V_O, as a function of measurement capacitance, C, has one set of lines for f = 10kHz and one for f = 20kHz. *Fig.* 25, V_O as a function of the reference voltage, V_R, likewise has two sets of lines but for C = 10pF and 68pF. *Fig.* 26, V_O as a function of the input frequency, f, also has two sets of lines for C = 10pF and 68pF.

The graphs demonstrate that the SC capacitance-to-voltage converter does behave linearly as a function of C, V_R and f as the theoretical expression *Eqn.* (3.2) predicts. However, there are offset and gain errors present in the output voltage.

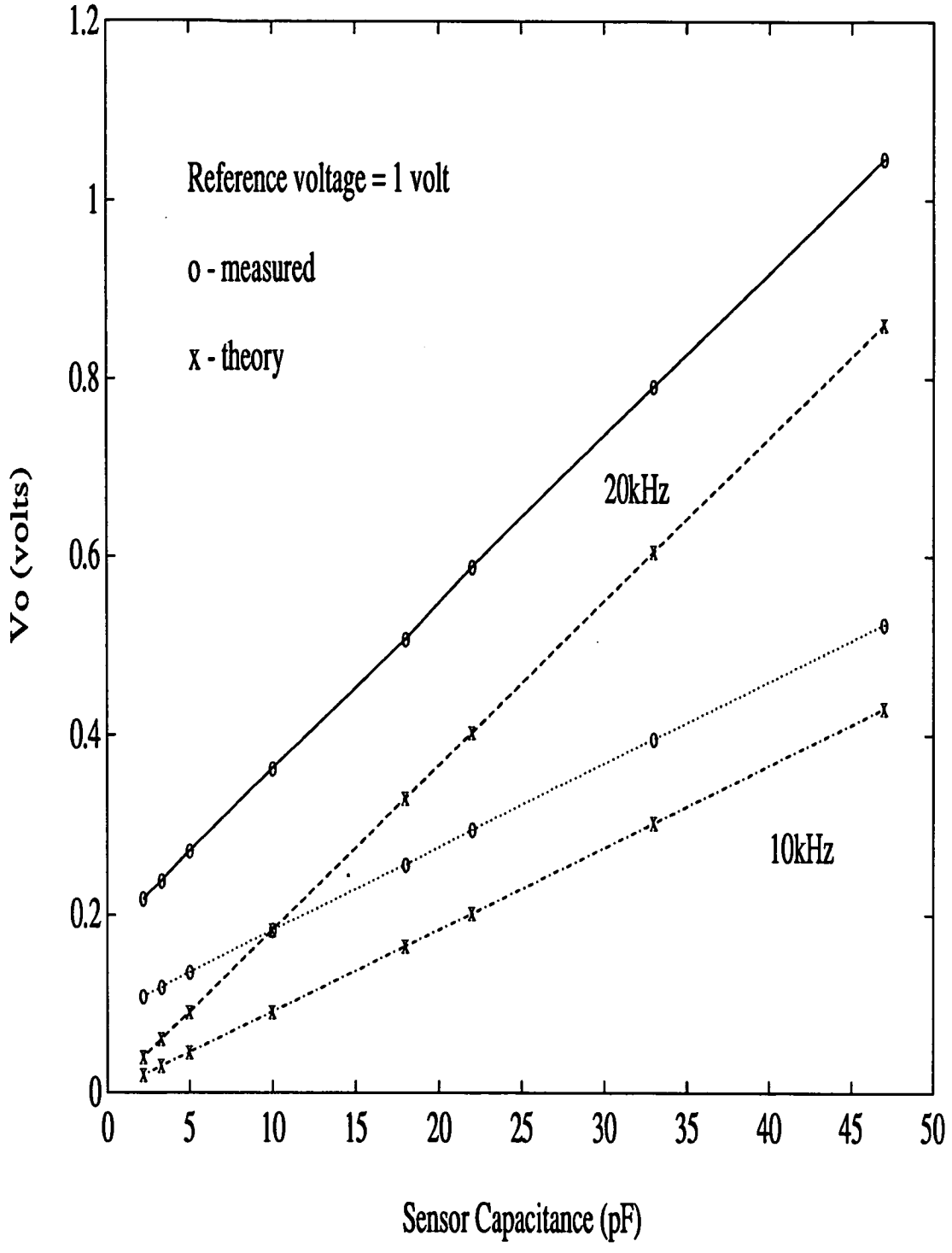


Figure 24: Graph of output voltage against sensor capacitance for the capacitance-to-voltage converter

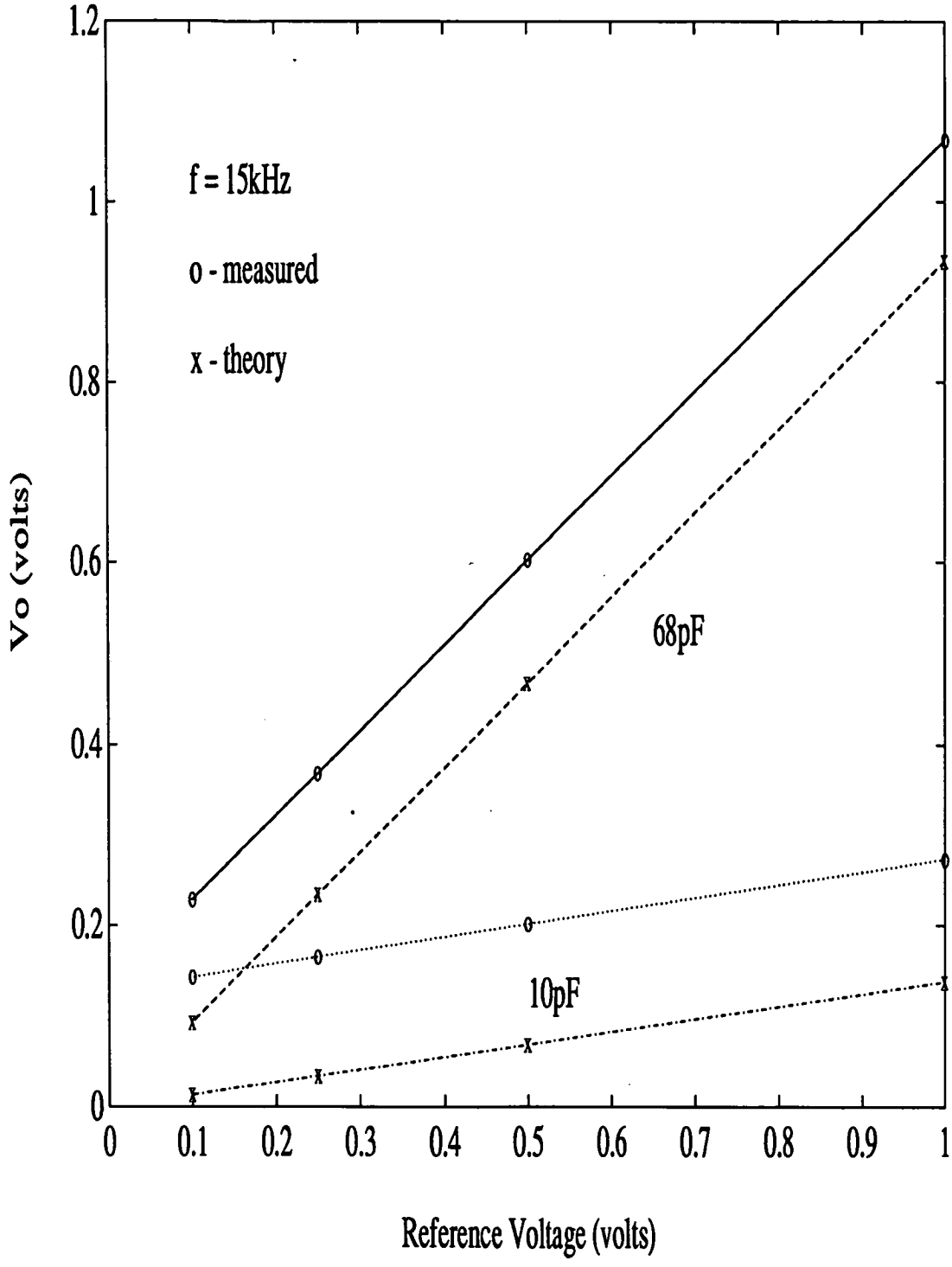


Figure 25: Graph of output voltage against reference voltage for the capacitance-to-voltage converter

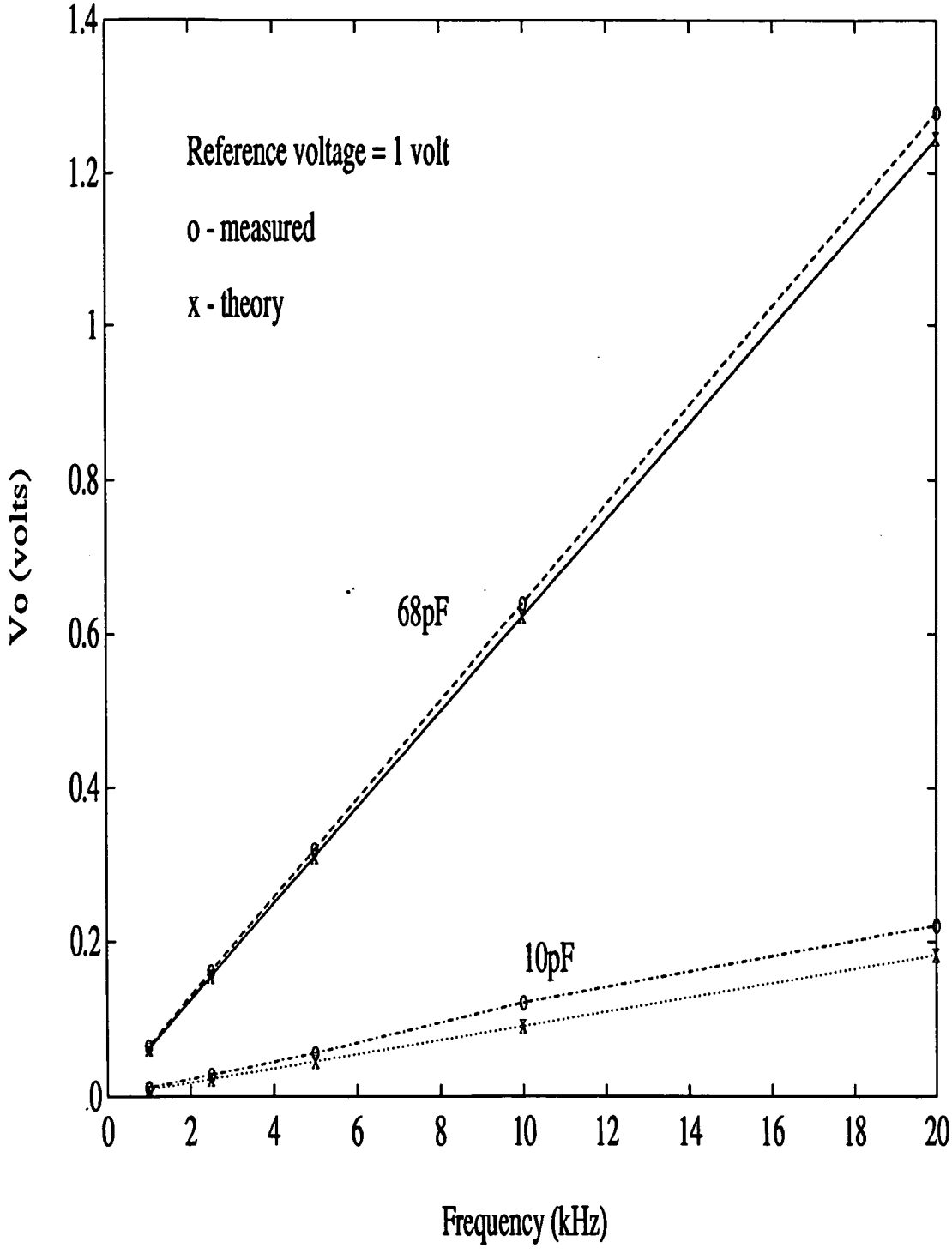


Figure 26: Graph of output voltage against frequency for the capacitance-to-voltage converter

4.2.3 The Frequency Control Loop

The operation of the frequency control loop, illustrated in *Fig.* 21, *p* 77, is described by *Eqn.* (3.5):

$$\frac{f_2}{f_1} = \frac{C_1}{C_2}\frac{V_1}{V_2}$$

The relationships between the frequency ratio, $\frac{f_2}{f_1}$, and the absolute capacitance when $C_1 = C_2$, and between frequency ratio and the reference voltage when $V_1 = V_R$ and $V_2 = -V_R$, were measured and plotted in *Fig.* 27 and *Fig.* 28 respectively, designated by 'O'. The theoretical values obtained from *Eqn.* (3.5) were also plotted, designated by 'X'. Components were as detailed for the SC capacitance-to-voltage experimentation with the addition of a second switched-capacitor block and two-phase clock generator, and VCO1 which is provided in the ES2 analogue library [23]. VCO1 is a voltage controlled oscillator which has its output frequency range set by an external capacitor and resistor. *Appendix A.3, p* 184 contains data for VCO1.

Fig. 27 demonstrates that the experimental behaviour deviates increasingly from that predicted by *Eqn.* (3.5) as the absolute capacitance, $C_1 = C_2$, is reduced. According to *Eqn.* (3.5) frequency ratio is constant when $C_1 = C_2$, as illustrated in *Fig.* 27. *Fig.* 28 also shows a significant departure from predicted behaviour as the absolute voltage approaches zero.

4.2.4 Section Summary

The results recorded in *Fig.* 24 to *Fig.* 28 have shown the first-order models to be inaccurate indicating the presence of an unmodelled source of error. This however is not always an inherent problem. A calibration stage could be introduced down-line

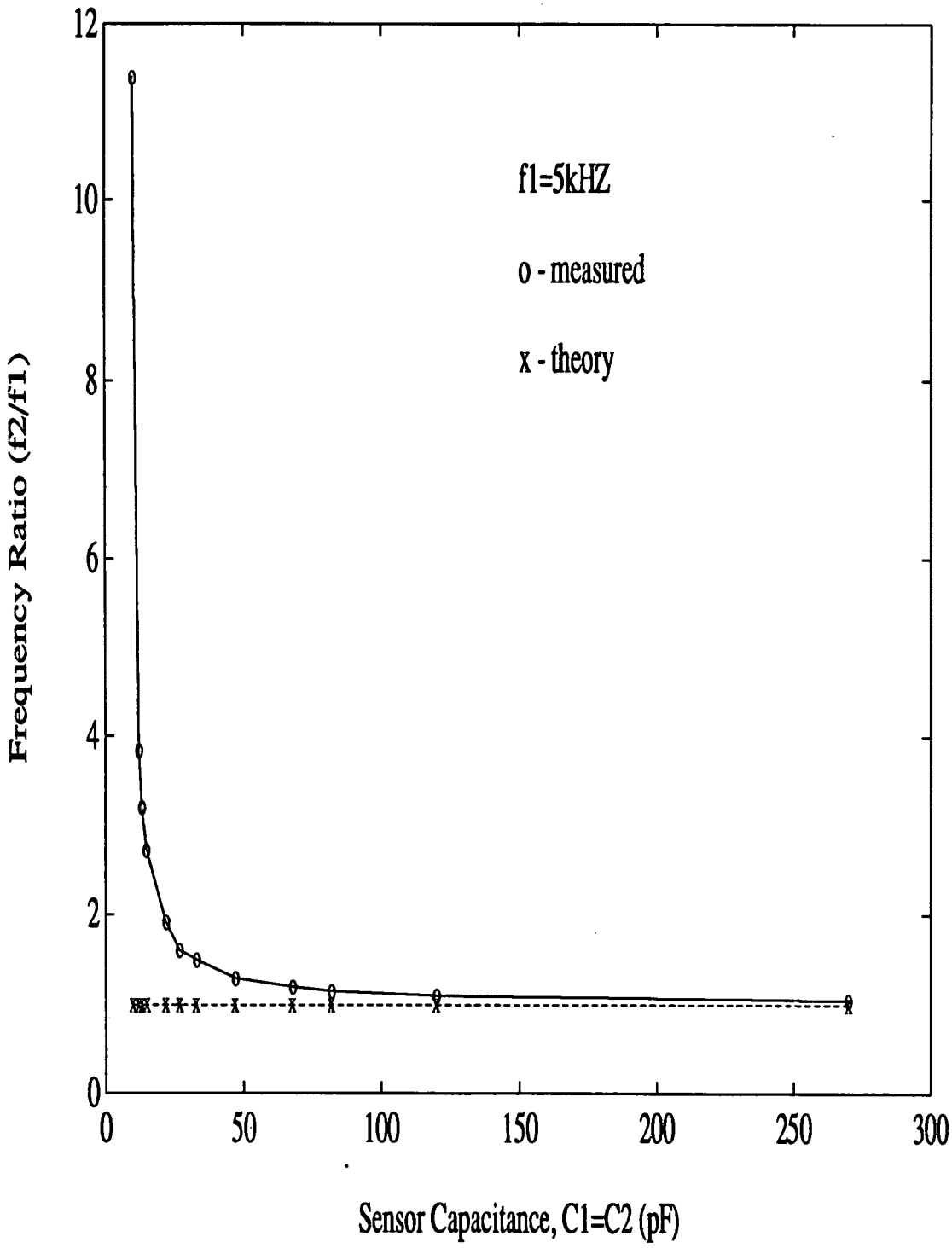


Figure 27: Graph of frequency ratio against absolute sensor capacitance for the frequency control loop

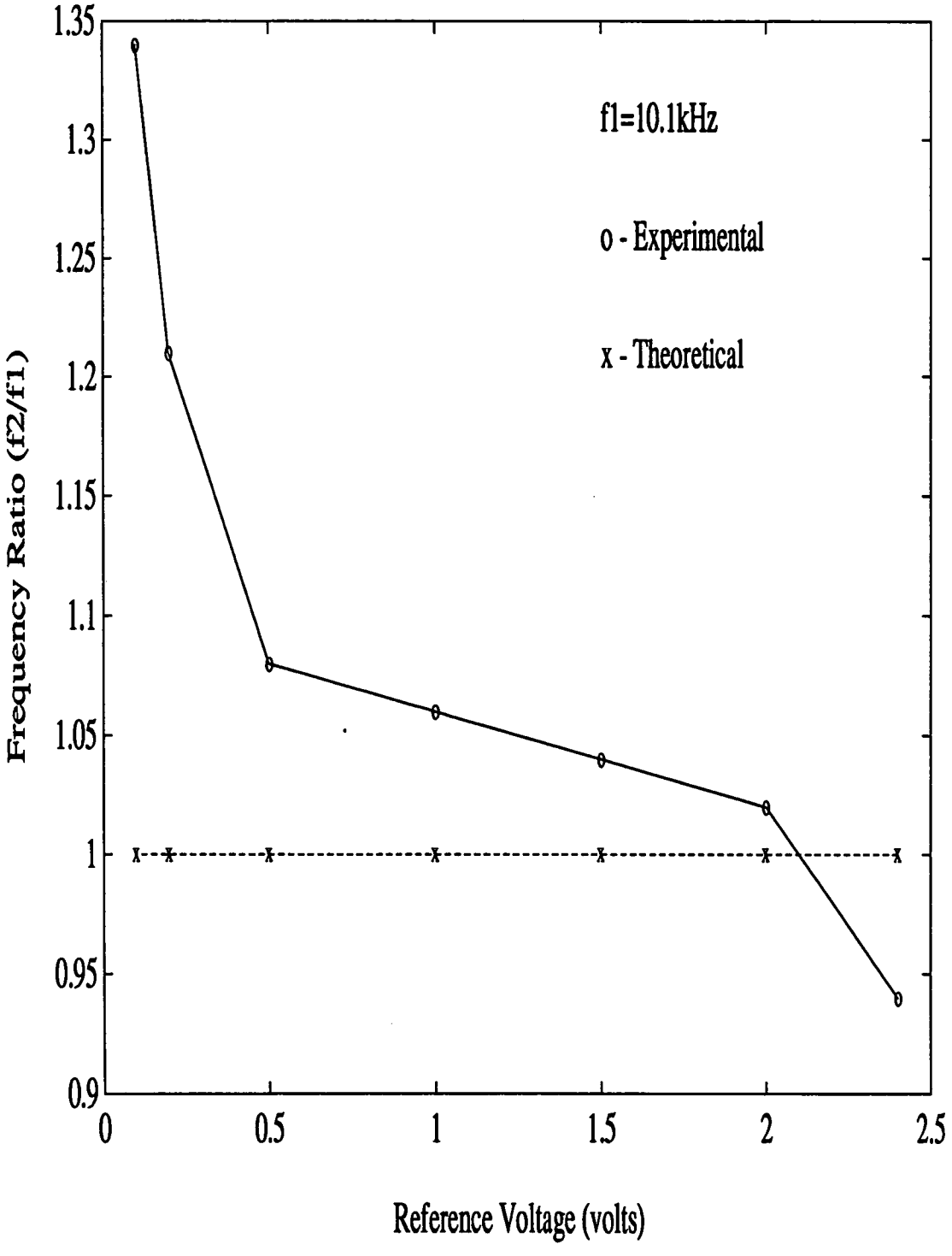


Figure 28: Graph of frequency ratio against reference voltage for the frequency control loop

of the interface circuit and curves such as those above, provided they are reproducible, be used to provide an accurate output. This is always true of the SC capacitance-to-voltage converter. On the other hand, using such a calibration scheme with the voltage control loop and frequency control loop depends on the operation of the two measurement capacitances. When one of C_1 or C_2 is a reference capacitor and the other a measurement capacitor a unique calibration curve exists. When both C_1 and C_2 are varying measurement capacitors an infinite number of calibration curves exist. As a result calibration cannot be accomplished. Another undesirable consequence of the unmodelled error is a reduction in the dynamic range of operation of all three interface circuits. Thus the error must be characterised and eliminated, if possible, to achieve the required high precision at low absolute values of measurement capacitance.

In *Chapter* 2 charge-injection and clock-feedthrough, both subsequently referred to collectively as charge-feedthrough, were identified as a significant source of d.c. error in many switched-capacitor circuits. The 4016 switches used in the above experiments have a rated maximum of 5pC of injected charge per gate transition [88]. If the first-order expression for the SC capacitance-to-voltage converter is modified to include an injected charge element, Q, then *Eqn.* (3.2) becomes:

$$V_o = R_f f [V_R C + Q] \tag{4.1}$$

Letting Q, the feedthrough contributed by a single switch be 5pC, V_R, the reference voltage be 1 volt, f be 20kHz, R_f, the feedback resistance be 916kΩ and C be 10pF yields an output voltage of 0.27 volts. This value is midway between the experimental value of 0.36 volts, obtained from inspection of *Fig.* 24, and the 0.18 volts predicted by *Eqn.* (3.2). It is probable that the combined feedthrough effect of switches M1 to M4, in *Fig.* 20(a), p 75, is the main source of error in both the SC capacitance-to-voltage converter and the frequency control loop.

The next section comprises a detailed investigation of charge-feedthrough within the four switch block demonstrating that the modification of the first-order expressions

for the SC capacitance-to-voltage converter and the frequency control loop to include charge-feedthrough effects, significantly improves their accuracy.

4.3 Charge-Feedthrough within the Four Switch Block

4.3.1 Section Introduction

Charge-feedthrough has been identified as the probable primary source of error in the operation of the SC capacitance-to-voltage converter and the frequency control loop. This section comprises a detailed investigation of the behaviour of charge-feedthrough within the four switch block.

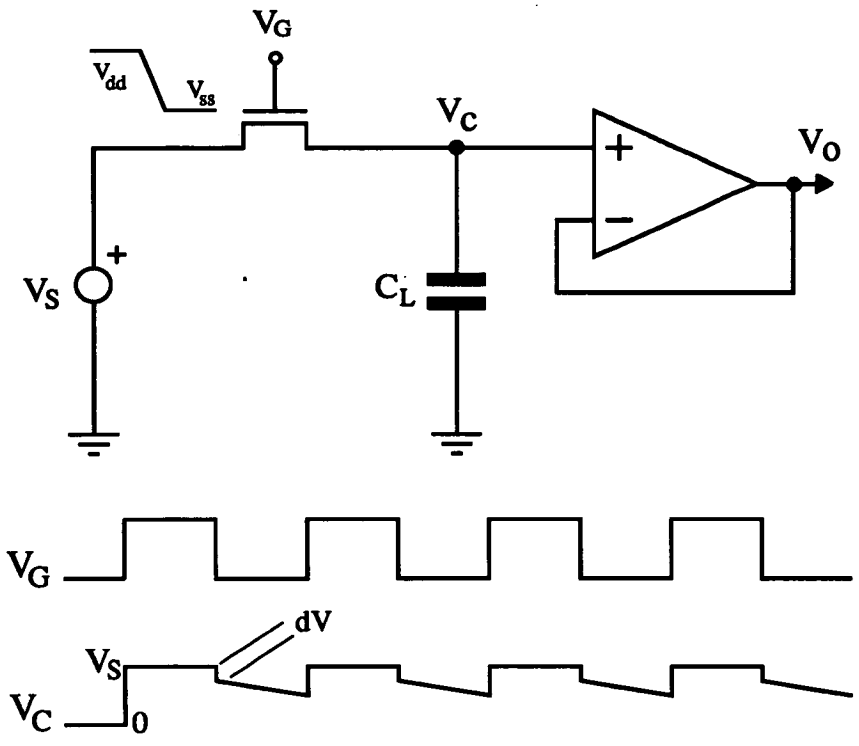
Firstly, the operation of various M4016 switches from the same and different manufacturers are compared. Next, having experimentally examined charge-feedthrough within the four switch block, an empirical second-order expression is obtained for the SC capacitance-to-voltage converter that includes the effects of feedthrough. This expression is shown to correspond to feedthrough behaviour in a single CMOS transmission gate and to published investigations into charge-feedthrough in single NMOS and PMOS devices.

Finally, the basic first-order expression for the frequency control loop is modified to include the effects of feedthrough. The resultant second-order model is shown to predict circuit behaviour with a high degree of accuracy.

4.3.2 Charge-Feedthrough in the 4016 CMOS Transmission Gate

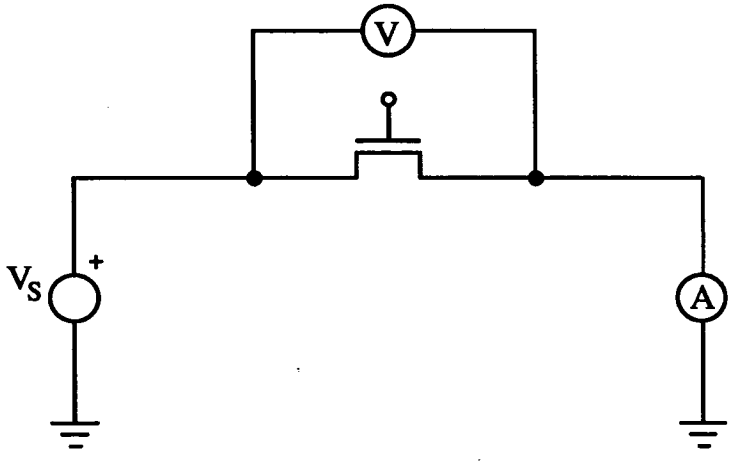
In this subsection results are presented of an investigation of charge-feedthrough in a series configuration of voltage source, switch and load capacitor. *Fig.* 29(*a*) shows the experimental set-up. The voltage source V_S charges the load capacitor, C_L, via a single CMOS switch. The change of voltage on the top plate of C_L was measured after a negative transition of the gate voltage, V_G, from V_{dd} to V_{ss}. *Fig.* 29(*a*) also shows several transitions of the gate voltage, V_G, with the corresponding voltage, V_C, on the top plate of C_L. Notice the charge-feedthrough induced step on V_C after the negative transition of V_G. Charge-feedthrough also occurs on the positive edge of V_G, but the resultant voltage step on C_L is masked by the rise of V_C to the source voltage level, V_S. The V_C trace also includes a small drop in voltage whilst V_G is low, i.e. the switch is off, representing charge lost through several leakage current mechanisms. These leakage mechanisms include operational amplifier input bias current and switch surface-leakage current. Display and measurement was on a CRO, either directly or via a LF356 operational amplifier configured as a non-inverting buffer as shown in *Fig.* 29(*a*). M4016 CMOS switches were used throughout this subsection and C_L was a 68pF silvered mica capacitor.

An outline of the experiments reported in this subsection will now be given. The magnitude of the feedthrough contributed by M4016 switches from various manufacturers was measured as a function of source voltage. The switch on-resistance, R_{ON}, was also measured as a function of source voltage. In addition, feedthrough magnitude was measured as a function of load capacitance, C_L. There was insufficient time available to investigate the effect of clock rise and fall times on the charge-feedthrough magnitude. This however was not considered to be a serious omission and to be of academic interest only, since the standard-cell implementation of the interface circuits did not permit the modification of the clock rise and fall times.



Charge Feedthrough = C_L dV

(a)



(b)

Figure 29: Experimental set-up for the measurement of
(a) charge-feedthrough and **(b)** on-resistance in a single switch

The effect of variation of source voltage on the charge-feedthrough magnitude was investigated as follows. The supply voltages, V_{dd} and V_{ss}, were set at 2.5 and -2.5 volts respectively. The gate voltage, V_G, of a Motorola M4016 switch was clocked continuously with a square wave between V_{dd} and V_{ss}, and V_S, the source voltage, was varied over the same voltage range. The charge-feedthrough magnitude was measured on the falling edge of V_G on the output voltage trace. The feedthrough charge is plotted as a function of source voltage, V_S in *Fig.* 30, designated 'X' and labelled 'M4016-1'.

This experiment was repeated with other switches of the same type. Three additional lines are shown in *Fig.* 30 to illustrate the significant variation in charge-feedthrough magnitude in 4016 switches from the same and different manufacturers. Two of these lines, designated 'O' and '+' and labelled 'RS-1' and 'RS-2', were obtained from measurements made on two different 4016 switches supplied by Radio Spares. The fourth line was obtained from a second Motorola M4016 switch and is designated by '*' and labelled 'M4016-2'.

The switch on-resistance, R_{ON}, was measured as a function of source voltage by means of a voltmeter, V, and an ammeter, A, as illustrated in *Fig.* 29(b) for one M4016 switch only. The same circuit conditions as above were maintained with the exception of the voltage levels which were changed to 0 and 5 volts. This did not have an effect on the operation of the circuit permitting comparison of the results, shown in *Fig.* 31, with the feedthrough results.

Finally, to assess the effect on charge-feedthrough of variation of the load capacitance the output voltage, V_O, was measured as C_L was varied over the range 10 to 120pF with the source voltage held constant at 2 volts. *Fig.* 32 shows the feedthrough charge plotted against the load capacitance.

Inspection of *Fig.* 30, which shows feedthrough voltage as a function of source voltage, reveals that the feedthrough charge magnitude varies in an approximately

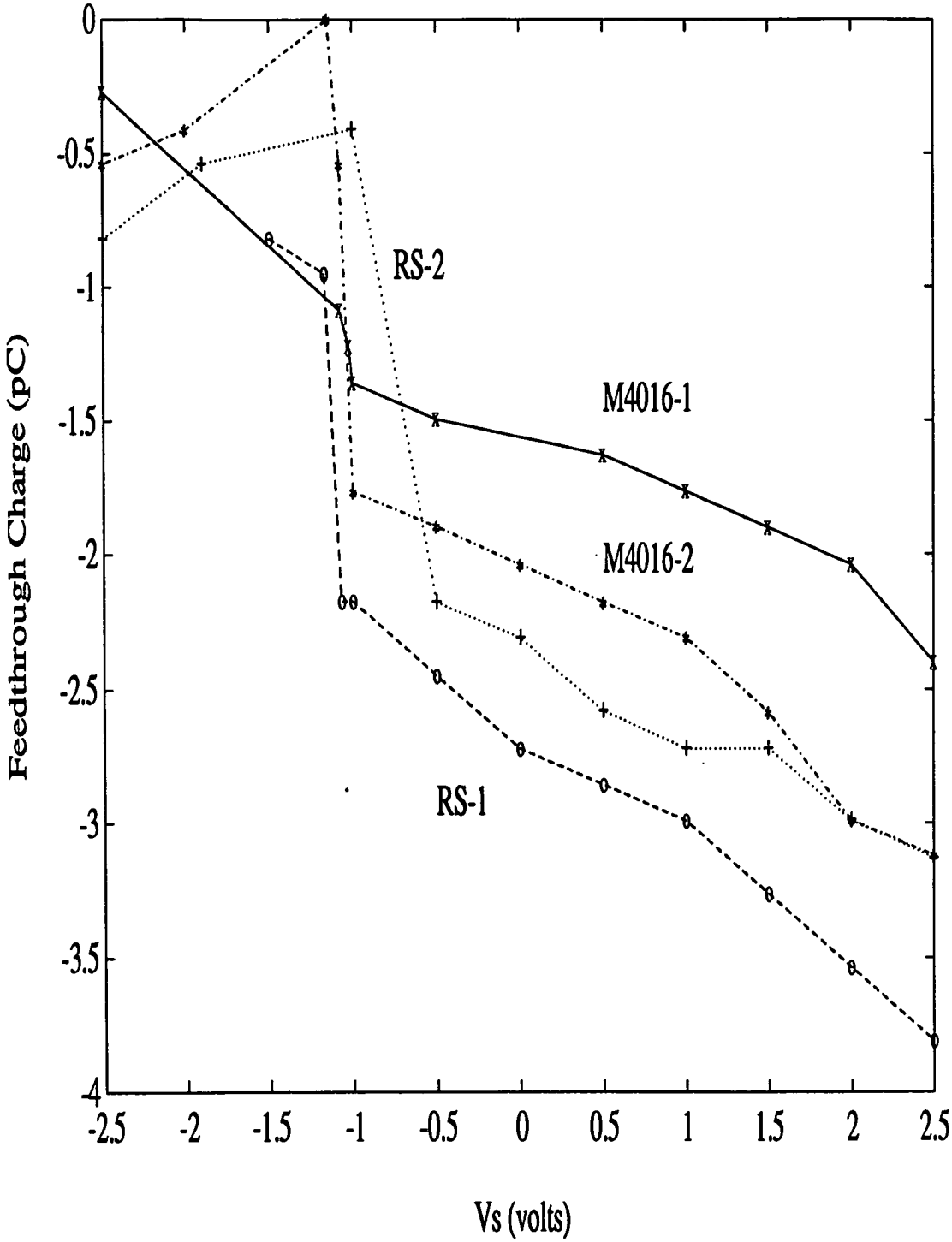


Figure 30: Charge-feedthrough against source voltage for four different 4016 transmission gates

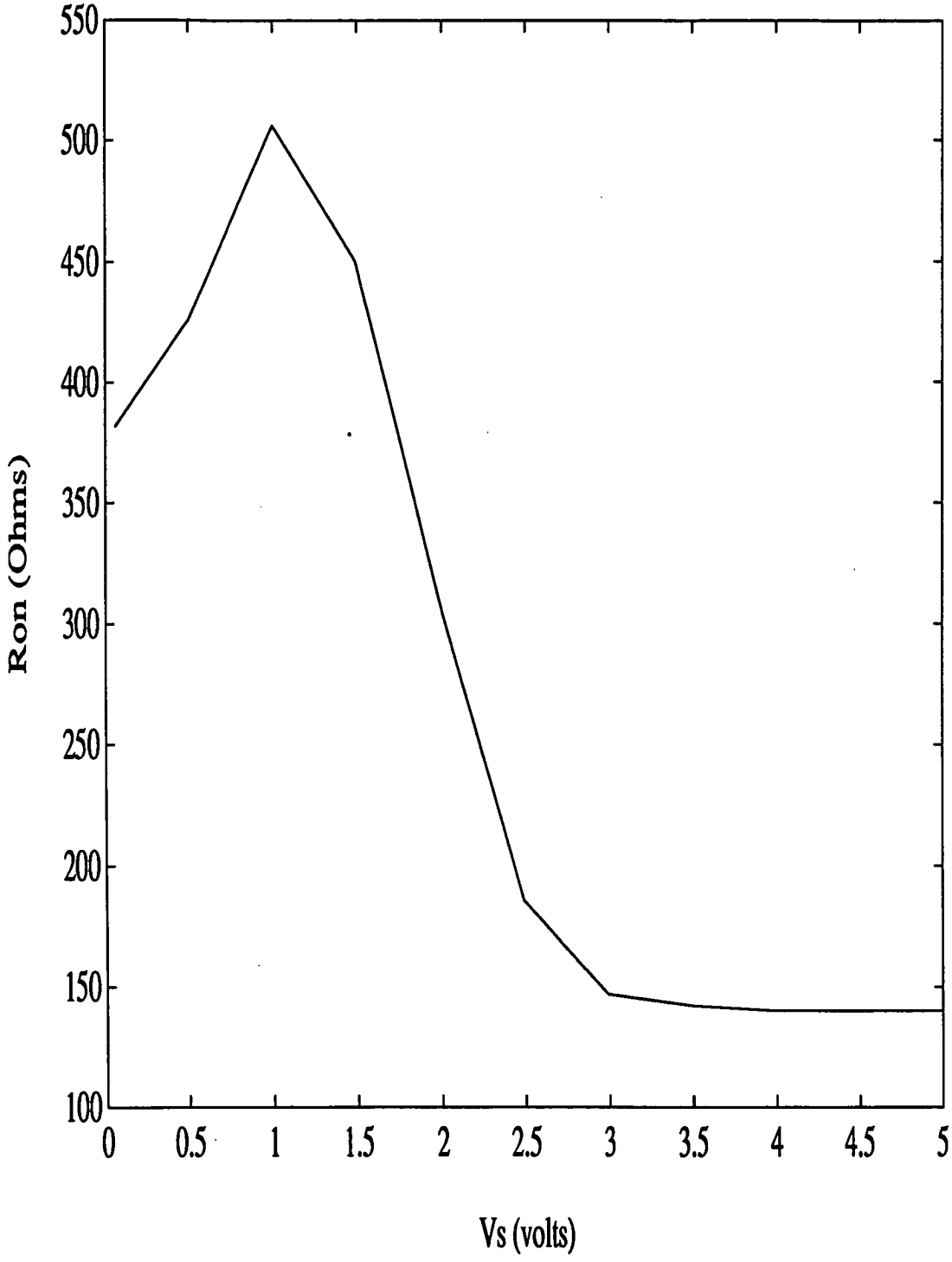


Figure 31: On-resistance against source voltage for a 4016 transmission gate

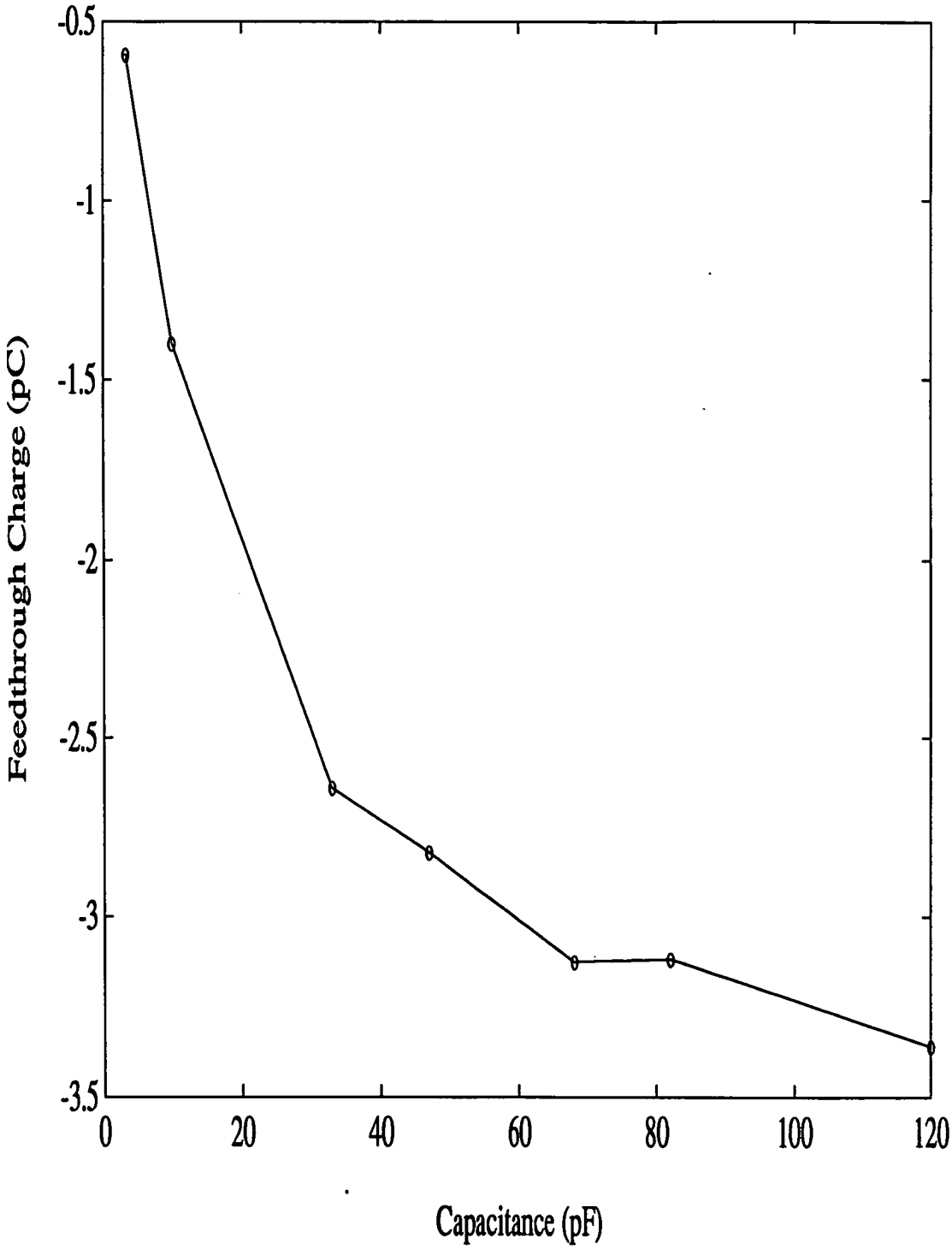


Figure 32: Charge-feedthrough against load capacitance for a 4016 transmission gate

linear fashion with source voltage, V_S. Referring to *Eqn.* (2.6) and *Eqn.* (2.8), in §2.4.1, *p* 59, a linear relationship should be expected for a single NMOS or PMOS transistor. Here however a CMOS transmission gate is used comprising an NMOS and a PMOS transistor connected in parallel. This type of switch does effect some degree of feedthrough cancellation, as detailed in §2.4.2, *p* 64, but it is dependent upon matching of the two transistors. Clearly the NMOS and PMOS devices fail to cancel each others feedthrough charge with that contributed by the NMOS transistor prevailing, since the net feedthrough effect is negative. Moreover, the two transistors fail to cancel the feedthrough charge in a linear fashion, as is evident from the marked decrease in magnitude between -0.5 volts and -2.5 volts source voltage in *Fig.* 30. Most commercial switches are optimised for low on-resistance for operation at high frequencies, which is unfortunately not a requirement for the present application. The design of a switch for low on-resistance is incompatible with low charge-feedthrough, as is demonstrated later in §5.4, *p* 140. This is supported by a comparison of *Fig.* 30 and *Fig.* 31. *Fig.* 31, on-resistance as a function of source voltage, displays a significant increase of on-resistance, R_{ON}, at between 0 volts and 2.5 volts source voltage. This is coincident with the marked decrease in charge-feedthrough in *Fig.* 30, after adjustment for the difference in supply voltage levels used during the charge-feedthrough experiment and the on-resistance experiment. Significantly, *Fig.* 30 demonstrates that feedthrough behaviour varies from switch to switch - even in those from the same manufacturer.

Inspection of *Fig.* 32 reveals that charge-feedthrough varies with load capacitance, C_L, with a reducing increment in magnitude noticeable as C_L is increased, as is predicted by *Eqn.* (2.6) and *Eqn.* (2.8), which describe charge-feedthrough for slow and fast gate turn-off times respectively. It is not possible to determine whether the fast or slow expression is applicable, since an NMOS and PMOS transistor are operating in conjunction and contributing to the charge-feedthrough.

4.3.3 Charge-Feedthrough in a Four-Switch Arrangement

The experiments on the single switch configuration yielded a maximum feedthrough charge of between 3pC and 4pC, approximately half the value required to cause the errors present in the results for the SC capacitance-to-voltage converter reported in §4.2.2. To resolve the discrepancy the operation of the four switch block used in the SC capacitance-to-voltage converter will now be analysed over a complete clock cycle.

Referring to *Fig.* 20(a), p 75, the non-inverting SC capacitance-to-voltage converter, the cycle begins with the closure of switches M1 and M2 upon the positive transition of ϕ_1. Charge is deposited onto the measurement capacitor, C, by both M1 and M2. However, considering that the left plate of C settles to source voltage potential and the right plate settles to ground potential, charge-feedthrough does not affect the measured charge stored on C.

When M1 and M2 open, upon the negative transition of ϕ_1, both M1 and M2 remove charge from the left and right plates of C respectively. Considering that the feedthrough charge is a strong function of source voltage, and that switches M1 and M2 have source potentials of V_R and zero volts respectively, the charge removed by M1 when $V_R = 0$, and that removed by M2 should be equal. Thus the net feedthrough charge on C should be zero. However, as V_R is increased the net feedthrough charge should increase proportionately. It should be noted that the effectiveness of the cancellation of feedthrough charge for $V_R = 0$ is dependent on the matching of switches M1 and M2.

The second phase of the clock cycle begins with the closure of switches M3 and M4 upon the positive transition of ϕ_2. Both M3 and M4 contribute to charge on the the left and right plates of the measurement capacitance, C. This charge is added to the now inverted feedthrough charge contributed by M1 and M2. M4 also contributes

feedthrough charge to C_I, the smoothing capacitor, assuming that half the channel charge exits through the source node and half through the drain node.

The clock cycle is completed with opening of M3 and M4 upon the negative transition of ϕ_2. Charge removed from C by M3 and M4 does not contribute to the net charge error, since the measured charge is now stored on C_I and C is subsequently connected to V_R and ground at the start of the next clock cycle. M4 also removes a charge packet from C_I which should cancel that deposited by M4 during switch closure.

To summarise, the net charge feedthrough error in the SC capacitance-to-voltage converter is composed of charge removed from C by M1 and M2, upon the negative transition of ϕ_1, and of charge added to the inverted charge on C by M3 and M4, upon the positive transition of ϕ_2.

The above analysis of charge-feedthrough within the non-inverting SC capacitance-to-voltage converter was validated experimentally as follows. To measure the net feedthrough charge on C as a function of source voltage after the negative transition of ϕ_1, the X and Y inputs of a CRO were used to monitor the voltages on the left and right plates of C. A CRO invert and add operation permitted the display and measurement of the net feedthrough charge on C. C was of value 10pF. *Fig.* 33 shows the magnitude of the feedthrough charge, designated 'O', increasing with source voltage in an approximately linear fashion as predicted above. Note that the net charge contributed by M1 and M2 is approximately half that for the single switch arrangement feedthrough, shown in *Fig.* 30. Also, the marked non-linearity present in *Fig.* 30 has been cancelled. To assess the effect of charge-feedthrough on the complete non-inverting SC capacitance-to-voltage converter the circuit output voltage was measured as a function of source voltage, V_R. *Eqn.* (4.1) was used to obtain a set of values for the feedthrough charge, Q, where V_O was a set of measured voltages, R_f was of value 916kΩ, f = 50kHz and C = 10pF. The values for the feedthrough

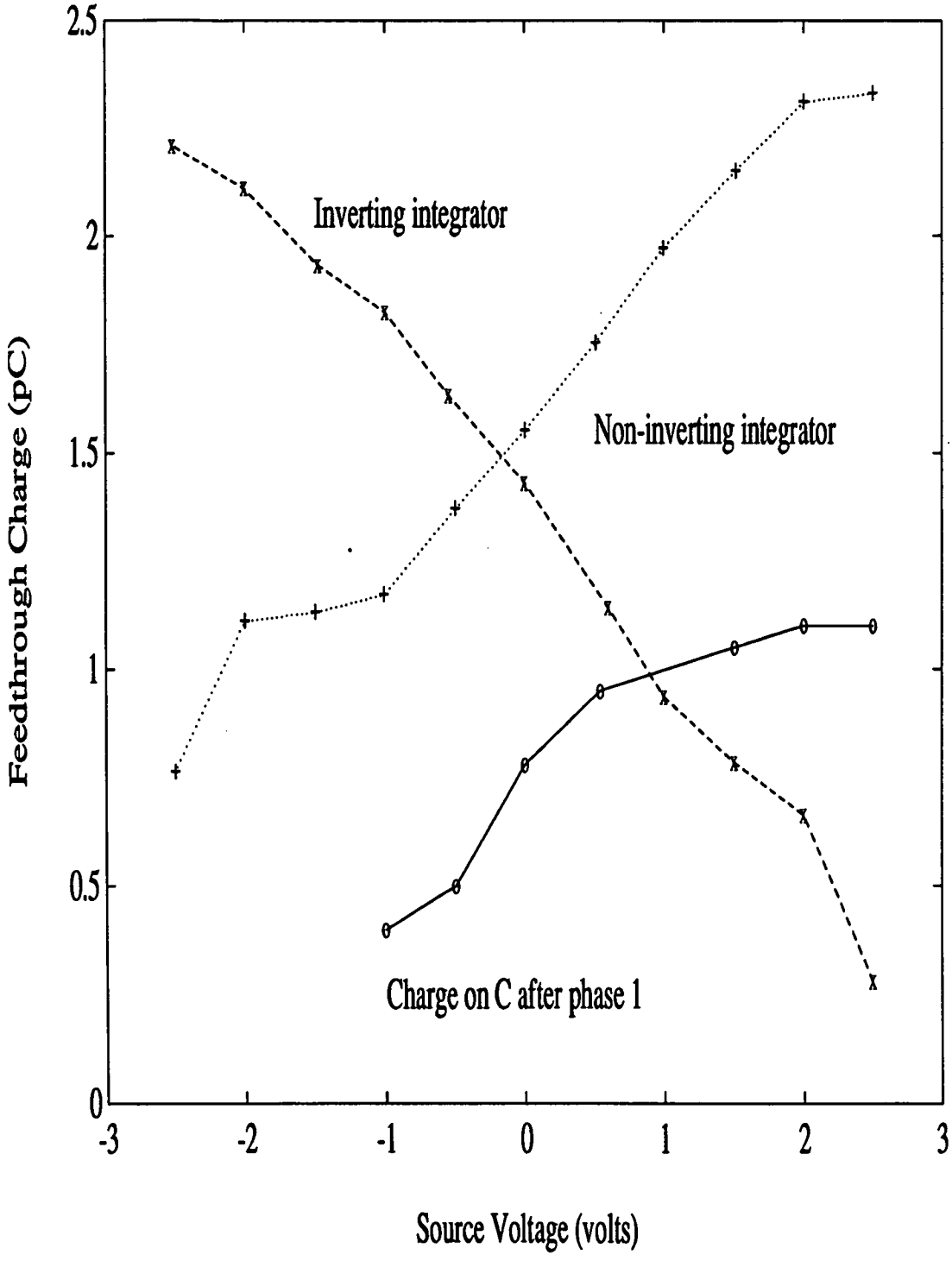


Figure 33: Charge-feedthrough against source voltage for the non-inverting and inverting capacitance-to-voltage converters, and after clock phase 1 of the non-inverting configuration of the capacitance-to-voltage converter

charge are plotted against source voltage in *Fig.* 33, designated '+'. Again the charge-feedthrough behaviour and magnitude is in accordance with the above analysis. The magnitude is approximately double that obtained for the two switch experiment. Moreover, the feedthrough increases in an approximately linear fashion with source voltage. The significant non-linearities present in the non-inverting circuit's curve as the source voltage approaches the supply voltages are caused by one of the NMOS and PMOS transistors in the M4016 switch turning off, and the resultant failure of the limited charge-feedthrough cancellation of this switch configuration, as described in §4.3.2, *p* 100.

The above experiment was repeated for the inverting capacitance-to-voltage converter, for the same circuit conditions and component values. The results are shown in *Fig.* 33, designated 'X'. Here, the feedthrough decreases linearly with increasing source voltage. This behaviour can be explained by an analysis of the net feedthrough effect within the inverting SC capacitance-to-voltage converter of *Fig.* 20(*b*), *p* 75, over a complete clock cycle. At the start of the clock cycle M1 and M4 close upon the positive transition of ϕ_1. Feedthrough charge is deposited on the left and right plates of C by M1 and M4 respectively. The two charge packets do not cancel if $V_R > 0$. M4 also contributes charge to C_I. When M1 and M4 open, M4 removes an equivalent amount of charge from C_I. On the other hand the charge removed from C by M1 and M2 does not affect the net feedthrough error, since the measurement charge is now stored on C_I. The subsequent closure of switches M2 and M3 grounds both plates of C prior to the start of another clock cycle. However, upon opening M2 and M3 deposit charge on C, although the two packets should cancel to some degree since both switches are at zero potential.

Finally, the effect of measurement capacitance, C, on charge-feedthrough was measured for the non-inverting converter. The results are plotted in *Fig.* 34 and display an approximately linear increase in feedthrough charge with increasing capacitance. This increase in the net feedthrough charge for the four switches within the SC

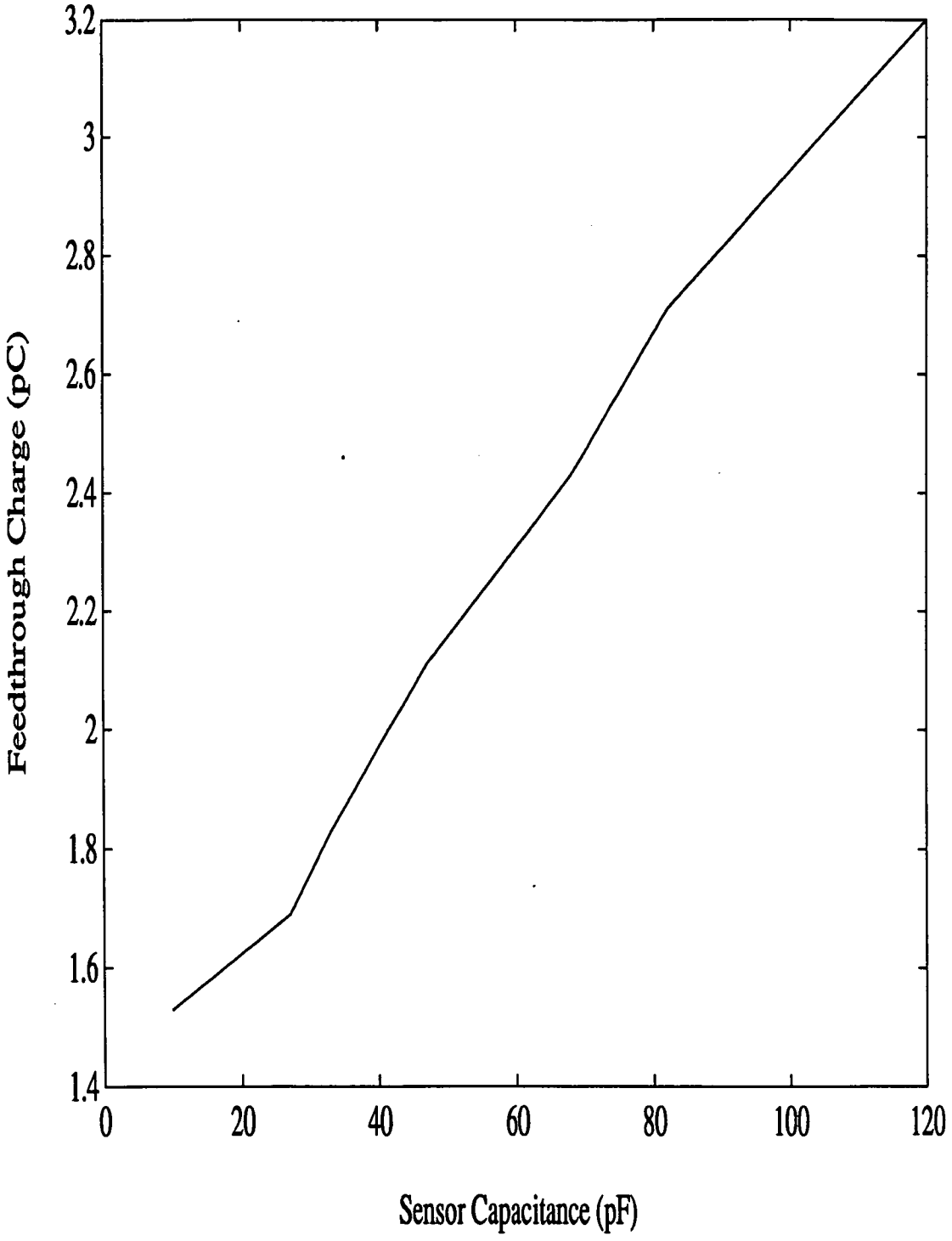


Figure 34: Charge-feedthrough against sensor capacitance for the non-inverting capacitance-to-voltage converter

capacitance-to-voltage converter is consistent with the increase in magnitude recorded for a single M4016 switch in *Fig.* 32, *p* 105. One, however is linear and the other non-linear.

4.3.4 Derivation of a Charge-Feedthrough Expression

Inspection of the behaviour of the SC capacitance-to-voltage converter, detailed in §4.2.2, *p* 91, and of the above results suggests that feedthrough is the primary source of error. Charge-feedthrough is primarily a function of the reference voltage, V_R. Including, $\delta q(V_R)$, representing the source voltage dependent, net feedthrough charge added to the measured charge stored on the smoothing capacitor each clock cycle in *Eqn.* (3.2) results in:

$$V_O = R_f f(CV_R + \delta q(V_R)) \tag{4.2}$$

The relationship between charge-feedthrough and reference voltage was investigated as follows. The experiment on the non-inverting SC capacitance-to-voltage converter, detailed in §4.3.3 above, was repeated with $C = 10\text{pF}$. Likewise, *Eqn.* (4.1) was used to obtain a set of values for the feedthrough charge, $\delta q(V_R)$, where V_O was a set of measured voltages, R_f was of value 916kΩ and f was 50kHz. The relationship between $\delta q(V_R)$ and V_R is plotted in *Fig.* 35. The plot shows the linear dependence of $\delta q(V_R)$ on V_R.

From *Fig.* 35, $\delta q(V_R)$ can now be expressed as a function of V_R:

$$\delta q(V_R) = mV_R + Q_O \tag{4.3}$$

where $m = 3.5\text{pF}$ and $Q_O = 10\text{pC}$.

Comparing *Fig.* 33 and *Fig.* 35, although the feedthrough charge is linearly dependent on source voltage in both cases, the feedthrough magnitude is considerably greater in the latter illustrating the large variation from switch to switch. In fact,

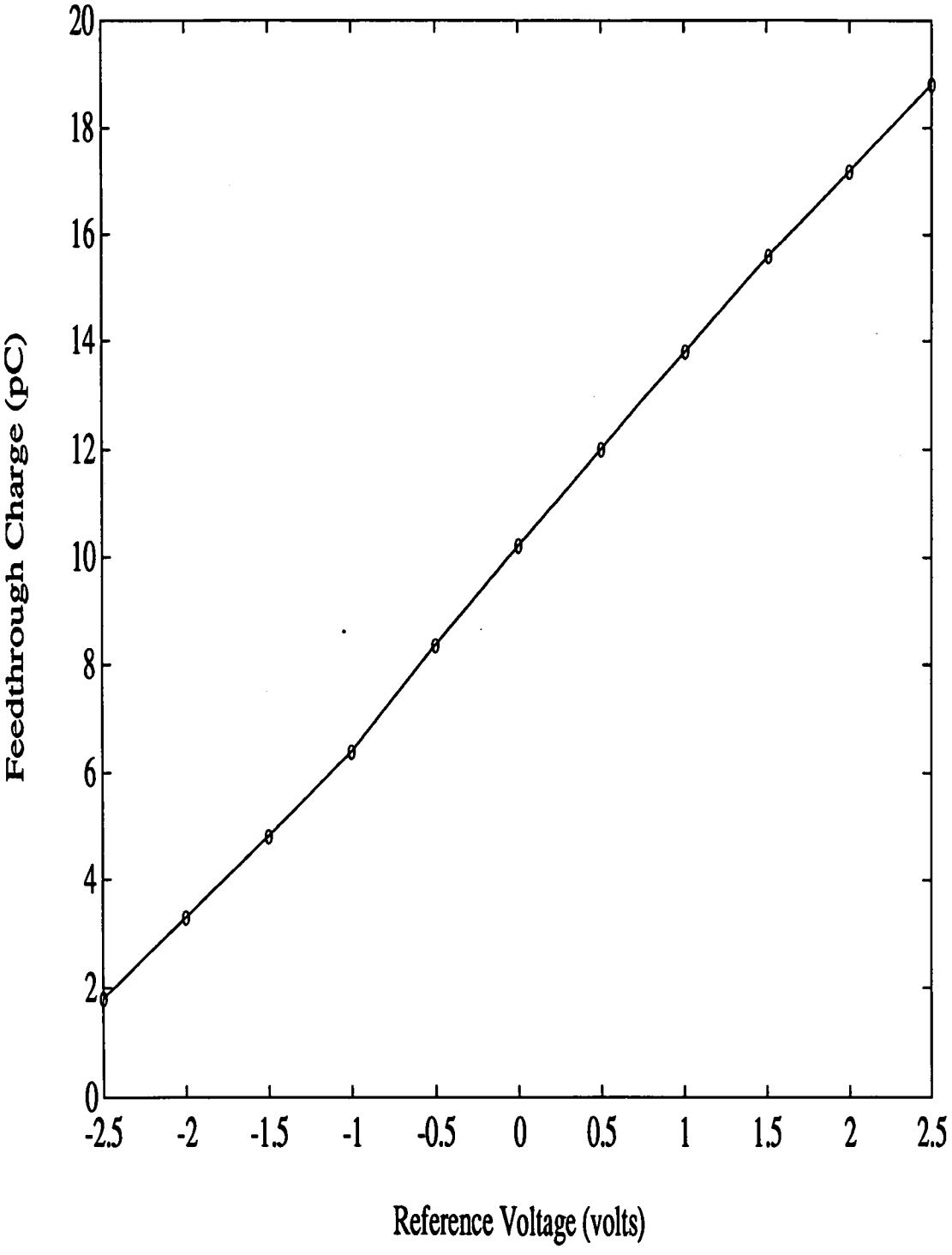


Figure 35: Charge-feedthrough against reference voltage for the non-inverting capacitance-to-voltage converter

measurements on the SC capacitance-to-voltage converter using several sets of M4016 switches revealed that the slope constant, m, varied from zero to 5pF, and the offset, Q_o, varied from zero to 10pC.

Consider *Eqn.* (2.6), the slow switch turn-off expression, and representing $\sqrt{\frac{\pi UC_L}{2\beta}}$ as A, *Eqn.* (2.6) becomes for a single NMOS switch:

$$q_{dm} = -[C_{gd}V_S + A\,(C_{gd} + \frac{C_{ox}}{2}) + C_{gd}(V_T - V_L)] \tag{4.4}$$

where C_{gd} and C_{ox} are the gate-diffusion overlap and oxide capacitances of the transistor, V_T is the transistor threshold voltage and V_L is the gate low voltage.

Consider the fast switch turn-off expression *Eqn.* (2.8). For a typical CMOS process $\frac{\beta V^3_{HT}}{6UC_L}$ is negligibly small. Hence, *Eqn.* (2.8) becomes, after rearrangement and substitution of $V_{HT} = V_H - V_S - V_T$:

$$q_{dm} = \frac{C_{ox}}{2}V_S - \frac{C_{ox}}{2}(V_H - V_T) - C_{gd}(V_H - V_L) \tag{4.5}$$

According to both *Eqn.* (4.4) and *Eqn.* (4.5) the charge feedthrough q_{dm} is a linear function of source voltage, V_S, with the former expression predicting a decrease in charge-feedthrough with increasing V_S, and the latter an increase with increasing V_S. Despite the fact that charge-feedthrough decreases with increasing source voltage for the single switch configuration, as illustrated in *Fig.* 30, *p* 103, there is insufficient experimental evidence to conclude that the slow turn-off expression models the M4016 switch charge-feedthrough behaviour on account of the complication introduced by the paralleled NMOS and PMOS structure of the switch. However, it can be concluded that Sheu's analytical model [73], of which the fast and slow turn-off expressions are simplifications, the experimental results for the single M4016 switch, and the experimental results for the SC capacitance-to-voltage converter are all in agreement regarding the influence of source, or reference voltage, on charge-feedthrough.

Having established the validity of the charge-feedthrough expression, *Eqn.* (4.3), the first-order model for the frequency control loop was modified as follows. Including *Eqn.* (4.3) in *Eqn.* (3.5) the first order equation for the frequency control loop becomes:

$$f_1(C_1V_R + m_1V_R + Q_{O1}) - f_2(C_2V_R + m_2V_R + Q_{O2}) = 0 \tag{4.6}$$

and hence:

$$\frac{f_2}{f_1} = \frac{1}{1+[\delta Q_2/C_2V_R]}\frac{C_1}{C_2} + \frac{\delta Q_1}{C_2V_R + \delta Q_2} \tag{4.7}$$

where $\delta Q_1 = m_1V_R + Q_{O1}$ and $\delta Q_2 = m_2V_R + Q_{O2}$.

Eqn. (4.7) was confirmed experimentally as follows. A new set of results were taken for the SC capacitance-to-voltage converter, as described above, to obtain accurate values for the feedthrough gain, m, and offset, Q_O, in two switched-capacitor blocks. The first calibrated switch block had an m_1 of 1.1pF and a Q_{O1} of 1.1pC; the second an m_2 of 0.72 pF and a Q_{O2} of 9.5pC. The two calibrated switch blocks were employed in a discrete component implementation of the frequency control loop. *Fig.* 36 shows frequency ratio, $\frac{f_2}{f_1}$, plotted against absolute capacitance when the capacitance ratio was held at unity, designated by 'O'. The second curve, designated by 'X', shows the predicted frequency ratio obtained from *Eqn.* (4.7) using the calibrated feedthrough gains and offsets. Clearly the second order extension of the first order theory enables the performance of this circuit to be modelled with good accuracy.

Eqn. (4.7) can be shown to model the frequency control loop containing one inverting and one non-inverting switch block, as illustrated in *Fig.* 21(*b*),*p* 77. Generalising for *Fig.* 21(*c*):

$$\frac{f_2}{f_1} = \frac{V_1}{V_2+[\delta Q_2/C_2]}\frac{C_1}{C_2} + \frac{\delta Q_1}{C_2V_2+\delta Q_2} \tag{4.8}$$

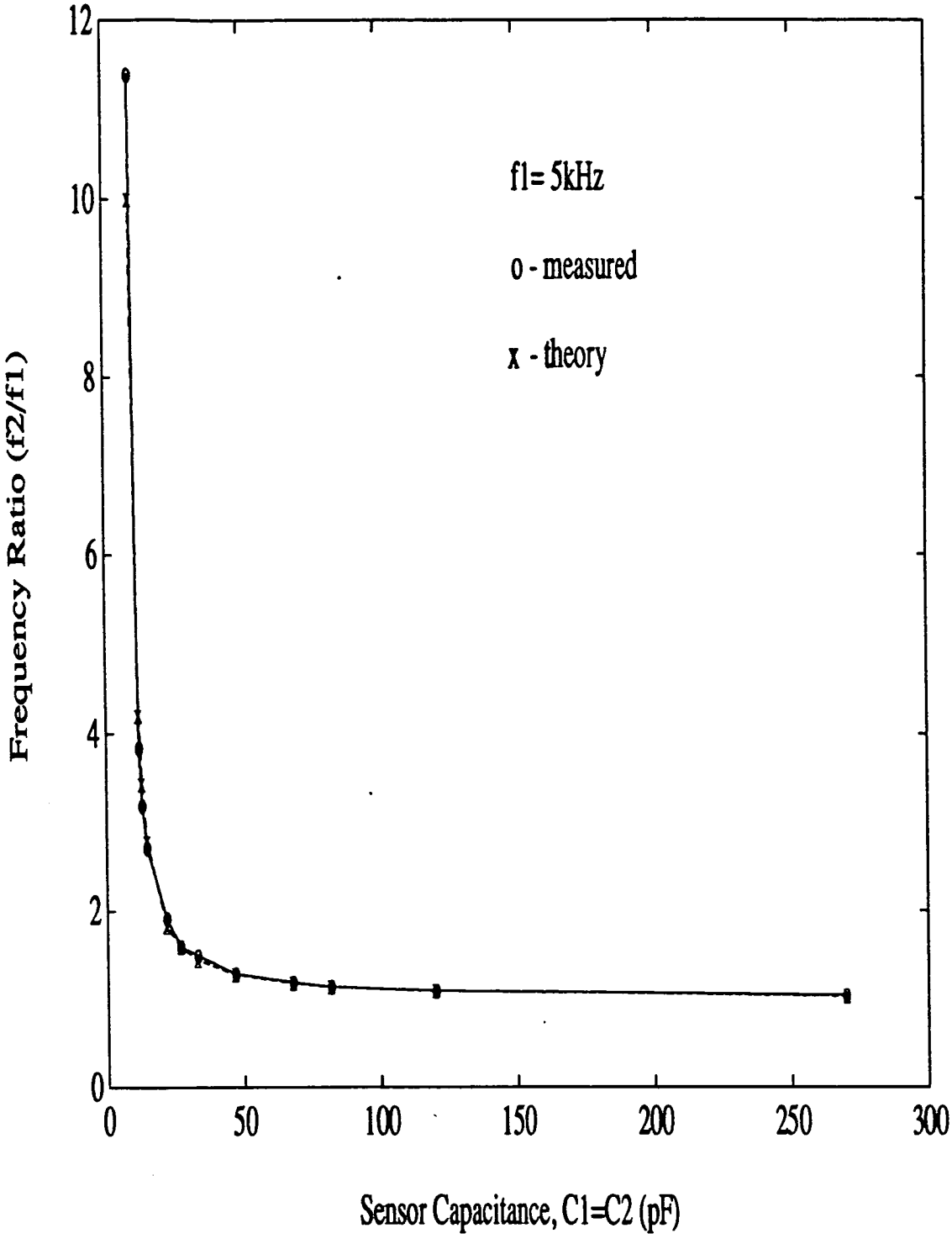


Figure 36: Measured and 2nd order theoretical frequency ratio against absolute sensor capacitance for the frequency control loop

4.3.5 Section Summary

The charge-injection and feedthrough contributed by a single switch has been analysed and the feedthrough cancellation effected by the CMOS transmission gate structure found to be poor. Moreover the switches are optimised for low on resistance, not a priority for the present application, and exhibit widely varying charge-feedthrough characteristics. Investigation of feedthrough within the SC capacitance-to-voltage converter has demonstrated that the net feedthrough charge contributed by the four switches within the switch block is responsible for the inaccuracy of the first-order model. Finally, and most importantly, the inclusion of a model for charge-feedthrough effects in the basic equation for the frequency control loop has produced an expression that models circuit behaviour with good accuracy.

As was discussed in §4.2.4, *p* 95 the option to include a calibration stage after the interface circuits is not viable. Consequently elimination of the feedthrough must be achieved by some other means. Charge-feedthrough compensation schemes were reviewed in §2.4.2, *p* 64, with the conclusion that the dummy-switch method was best suited to the present application. The inclusion of this compensation technique in the integrated implementation of the interface circuits is described in §5.4, *p* 140.

4.4 Locking and Jitter

4.4.1 Section Introduction

This chapter has been concerned so far with the steady-state performance of the three interface circuits. In this section two aspects of the dynamic behaviour of the frequency control loop that limit performance will be reported. Firstly, locking-up of the feedback frequency will be discussed prior to a consideration of coupling of the reference and feedback frequencies.

4.4.2 Lock-Up of the Feedback Frequency in the Frequency Control Loop

Charge-feedthrough can under certain circuit conditions cause the feedback frequency, f_2, to lock-up at the maximum output frequency of the VCO.

As illustrated in *Fig.* 18, *p* 72, the time for the voltage across the measurement capacitor, C_1, to settle whilst ϕ_1 is high is controlled by the product of the switch on resistance and any line resistance, and the capacitance of C_1 itself. The final voltage, V, on C_1 can be determined by:

$$V = V_{ref}(1-exp(-\frac{\tau}{RC_1})) \qquad (4.9)$$

where τ is the time ϕ_1 is high, V_{ref} is the reference voltage, and R is the combined switch and line resistance.

If $C_1 = C_2$ then $f_2 = f_1$ according to the first order expression *Eqn.* (3.5). Consequently ϕ_1 is high for the same length of time in both switch blocks, SC_1 and SC_2 of *Fig.* 21(*a*), *p* 77. However as has been demonstrated in §4.3.4, *p* 112, charge-feedthrough causes $f_2 > f_1$ when $C_1 = C_2$, shortening the period of ϕ_1 of f_2 and

preventing the voltage on C_2 reaching $-V_{ref}$. Hence an error charge, the difference between the charge injected by SC_1 and SC_2, is integrated on C_I, producing an increase in the voltage at the output node of the amplifier. This in turn increases f_2 in an attempt to correct the charge imbalance at the inverting input of the amplifier. Unfortunately the period of ϕ_1 is further shortened, reducing the final voltage on C_2 and eventually pushing f_2 to the maximum frequency deliverable by the VCO. Thus a positive feedback mechanism exists within the negative feedback loop as a consequence of the charge-feedthrough error.

This positive feedback mechanism only operates if the time constant in the feedback switched-capacitor block is large with respect to $\frac{1}{f_2}$, where f_2 is the VCO output frequency. For example, when the frequency control loop is set up with C_1 = 330pF and C_2 = 270 pF, and f_1 is increased gradually from 100kHz, f_2 locks up when f_1 exceeds 119kHz. The effect of the rise time on C_2 on the failure of the negative feedback mechanism was further substantiated by introducing a resistance in series with $-V_{ref}$ and C_2 to increase the settling time requirement. As expected f_2 locked-up at a lower frequency.

This additional disadvantage of feedthrough strengthens the argument for introducing the dummy switch compensation discussed in the previous section. The limits of operation of this positive feedback mechanism have not been defined, although from experimental evidence it typically operates when the measurement capacitances are in excess of 100pF and the frequencies are greater than 100kHz. Thus the positive feedback mechanism does not present a problem for the present application where much smaller values will be used.

4.4.3 Locking and Jitter in the Frequency Control Loop

Jitter in f_2, the feedback frequency, and locking of f_2 to f_1 are another source of error in the frequency control loop in addition to charge-feedthrough. *Fig.* 37 shows the frequency ratio, $\frac{f_2}{f_1}$, plotted against capacitance ratio, $\frac{C_1}{C_2}$. The two curves, designated 'O' and 'X', demonstrate that as C_2 is reduced from 8.7pF to 8.2pF the relationship deteriorates from one which is linear to one which is randomly non-linear in addition to exhibiting jitter in the frequency ratio via f_2. The third plot, designated '+', shows the same relationship but with C_2 further reduced to 6.6pF. Here, f_1 and f_2 display a significant degree of locking. Furthermore this behaviour was not repeatable, particularly for small values of measurement capacitor. It was concluded that both locking and jitter were caused by coupling of f_1 and f_2 through the power supplies and across signal lines. Fractional changes in interconnect wire positions and the effects of "hand capacitance" significantly changed the jitter and locking behaviour making investigation of this phenomenon difficult. This emphasises the unsuitability of the discrete component circuit as a result of its unstable parasitic environment for the measurement of particularly low values of capacitance. Circuit layout precautions were taken to minimise the effect of these mechanisms: the positive and negative power rails to the analogue and digital parts of the circuit were decoupled and separated to prevent glitches from the digital circuitry becoming impressed on the analogue supplies; and screened cable was used for the longer signal lines. Despite the precautions locking generally was observable at measurement capacitance values of less than 10pF, and jitter at all values of capacitance. Typically, as C_1 was increased with respect to C_2, f_2 increased through frequency bands where jitter was negligible to bands where it was at a maximum. This behaviour is symptomatic of locking on harmonics of f_1 and f_2.

The time taken to measure f_2 was demonstrated to influence the effect of jitter. For example, for measurement times of 10mS and 64mS the jitter, expressed as a

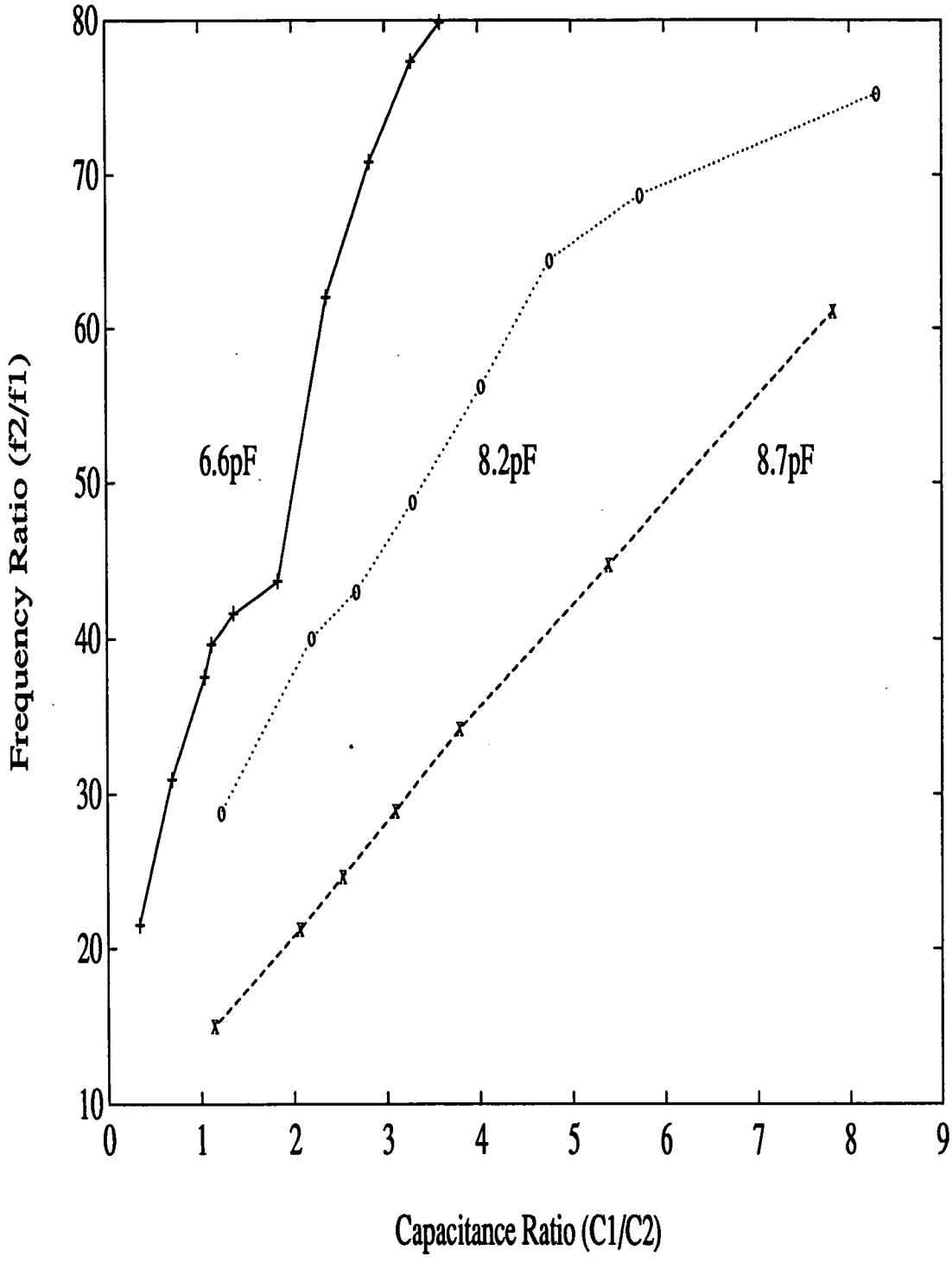


Figure 37: Measured frequency ratio against capacitance ratio for the frequency control loop illustrating the effects of locking and jitter

percentage of the frequency ratio, was 0.68% and 0.1%.

Inclusion of a divider in the feedback loop, as described in §3.3.2, *p* 76, separates f_1 and f_2 and therefore minimises the coincidence of their harmonics. This modification significantly reduced the jitter magnitude. A second, but untried remedy is the inclusion of a zener diode at some reference point within the frequency control loop feedback loop [52]. The broad-band noise produced by the zener diode should perturb f_2 preventing it from synchronising with f_1 and hence minimise jitter and lock-up.

Locking and jitter behaviour and the effectiveness of the two remedial schemes will be more fully investigated in an integrated implementation of the frequency control loop.

4.5 Power Consumption and Transient Response

4.5.1 Section Introduction

An analysis of power consumption and an expression for the settling time of the frequency control loop is presented in this section. As a result of discussions with research staff in the Department of Electrical Engineering, Edinburgh University, researching low power process control field-bus instrumentation, a power consumption of less than 22.5mW was established as a design priority for each of the interface circuits, as detailed in §1.3, *p* 13. In this section the power consumption measurements of components of the frequency control loop and of the circuit as a whole are presented. All three interface circuits are intended for low speed operation with a data-acquisition time of between 20mS and 100mS, and this generally has the advantage of permitting a low power consumption. It should be noted that the power consumption estimates and measurements presented in the next section give an accurate

indication of the power consumption of an integrated version of the frequency control loop, since the analogue components, which are the main power consumers, are those of the ES2 evaluation ICs and are of identical design to those in the ES2 ASIC process analogue cell library.

4.5.2 Power Consumption of the Frequency Control Loop

The power consumption of comparable interface and converter circuits has been reviewed in *Chapter* 2. For power consumption estimates the frequency control loop can be considered as comprising four subsections: the VCO, the integrating amplifier, the switch capacitor blocks and the two-phase clock generators. Before the experimental measurements are detailed the power consumption of the circuit and its subcircuits will be calculated theoretically.

The VCO dissipates 3.7 mW when running at 1MHz and OP22 dissipates 18 mW when operating without a load [23]. The dissipation in the switch block depends on the measurement capacitor sizes and the frequency of operation.

The power dissipation in a switched-capacitor block is given by:

$$P_{DISS} = fC|(V_H - V_L)|^2 \tag{4.10}$$

where V_H and V_L are the high and low gate voltages and f is the switch frequency. For $C_1 = C_2 =$ 10pF, f = 5 kHz, V_H = 2.5 volts and V_L = -2.5 volts the power dissipation in both switched-capacitor blocks is 2.5μW.

The power dissipation of the two-phase circuitry was calculated as follows. The power dissipated by an HEF 4011B quad AND gate is:

$$P_{DISS} = 1300f_i + f_o C_L V_{DD}^2 \tag{4.11}$$

and the power dissipated by an HEF 4081B quad NAND gate is:

$$P_{DISS} = 450f_1 + f_o C_L \times V_{DD}^2 \tag{4.12}$$

where f_i and f_o are the input and output frequencies, and C_L is the gate load capacitance for a HEF 4081 NAND gate. Thus for the two two-phase clock generators, illustrated in *Fig.* 23, *p* 90, which comprise two 4011 and six 4081 gates, the power consumption is 5μW when $f_i = f_o$ = 5kHz and C_L is typically 5pF. Hence, the total requirement for the two-phase generators and the switched-capacitors is 10.16μW, and 21.7mW for the complete circuit.

To measure the power consumption the total current drawn from the power supplies was measured with a multimeter. The circuit had component values C_I = 0.022μF, $C_1 = C_2$ = 10pF, f_1 = 5 kHz, f_2 = 25.9 kHz, V_1 = 1.25 volts and V_2 = -1.25 volts. The measured current was 5.74 mA, hence for a supply voltage of 5 volts P_{DISS} = 28.7 mW. Of the above total 26.2 mW was dissipated by the VCO and integrator and 2.6 mW dissipated by the switches and two-phase clock generator. This latter figure is higher than that calculated above and can be explained when the effects of feedthrough are considered. Charge-feedthrough, which acts to raise f_2 with respect to f_1 when $C_1 = C_2$, increases the power consumption unnecessarily although not significantly as a proportion of the whole. The remaining difference in calculated and measured power consumption can be explained by the fact that the power rating for OP22 was incompletely specified.

The primary power consumer in the frequency control loop circuit is the operational amplifier. The power requirement was significantly reduced by replacing OP-22 with OP-32, the low power amplifier in the European Silicon Structures library. *Appendix A.2, p* 183 contains data for OP-32. The compromise was a reduction in output voltage swing. The measured output voltage swing was 0.7 to 3.7 volts when V_{DD} = 5 volts and V_{SS} = 0 volts, compared with a swing of 0 to nearly 5 volts obtainable with OP-22.

The output frequency of the VCO is given by:

$$f_{OUT} = kV_{IN} \tag{4.13}$$

where $k = \frac{1}{0.8V_{DD}R_{EXT}C_{EXT}}$ and is the VCO gain factor. R_{EXT} and C_{EXT} are external components. V_{IN} is supplied by the voltage at the output node of the integrating operational amplifier and is limited to a maximum of 3 volts [23]. This results in a reduction in dynamic range of 23% when OP-32 is used in the circuit, since V_{IN} can now only drop as low as 0.7 volts. Moreover, the minimum output frequency of the VCO is limited unless the gain factor k is reduced to a low value. The result is a further, considerable reduction in the dynamic range of the circuit.

To overcome this problem *Eqn.* (4.13) can be modified:

$$f_{OUT} = \frac{V_{IN} - V_R}{0.8V_{DD}R_{EXT}C_{EXT}} \tag{4.14}$$

where V_R is a voltage applied to the external resistance, R_{EXT}, or capacitor, C_{EXT}; normal operation of the VCO requires both R_{EXT} and C_{EXT} to be connected directly to circuit earth. The VCO output frequency is determined by the rate at which C_{EXT} is charged by a current proportional to R_{EXT} and V_{IN}. Thus, raising the potential of R_{EXT} from zero volts has the same desired effect as reducing V_{IN}, as shown in *Eqn.* (4.14). V_R was chosen to be 0.7 volts, the minimum output voltage of OP-32, to utilise the full input voltage range of the VCO.

The power consumption of the circuit was measured as above with the same component values and parameters. The drawn current was 2.04 mA, hence P_{DISS} = 10.2mW, which is comfortably within the maximum power consumption of 22.5mW for fieldbus operation, stated in §1.5, *p* 17.

4.5.3 The Settling Time of the Frequency Control Loop

The settling time to within 0.1% accuracy for the frequency control loop can be shown to be:

$$t_s = \frac{C_I}{k}\frac{7.7}{C_2 V_{ref}} \tag{4.15}$$

where k is the VCO gain factor defined above. In deriving *Eqn.* (4.15) a continuous time approximation was made for the operation of the two switch blocks which results in the loss of f_1 and f_2. Measurements on the discrete component implementation of the circuit confirmed the validity of this expression.

Considering that the settling time is controlled by the gain factor, k, and the smoothing capacitor, C_I, limits are placed on their values if the circuit is to settle and leave sufficient time for pulse counting within the required 100mS conversion time, as stated in §1.5, *p* 17. A conflict exists in the selection of the gain factor, k. A large k is required for a fast settling time, but a small k is required for maximum dynamic range. C_I, the smoothing capacitance is also subject to conflicting design considerations. C_I should be sufficiently large to smooth the charge packets injected into the operational amplifier inverting input. However, according to *Eqn.* (4.16) a large value of C_I increases the settling time. A more detailed investigation of these conflicts is required.

4.6 Chapter Summary

Experimental investigations of two of the three interface circuits presented in *Chapter* 3, namely the SC capacitance-to-voltage converter and the frequency control loop, have been reported in this chapter. The findings of the investigations can be best summarised by considering each of the research objectives, stated in §1.5, *p* 17, in turn, beginning with power consumption.

The measured power consumption of the frequency control loop was 10.2mW, a figure that is comfortably within the specified 22.5mW. Moreover, this figure compares favourably with the 80μW to 27mW spread of values for published converter and

interface circuits, summarised in *Table* 1, *p* 55, particularly when it is considered that it was achieved with analogue components from a standard-cell library.

The specified data-acquisition time of 20mS to 100mS can also be achieved. However, the acquisition time, or more specifically the time taken to measure the frequency control loop VCO output frequency, must be considered in conjunction with resolution. The acquisition time has a strong influence on the resolution; for example a longer acquisition time reduces the effect of jitter through an averaging process. Furthermore the transient response and the dynamic range are additional interdependent factors. The relationship among acquisition time, resolution, transient response and dynamic range requires more work and will be more fully investigated as part of the testing of the integrated frequency control loop.

Performance over the industrial temperature range was not investigated experimentally and should also form part of any future testing of integrated versions of the interface circuits. It should be noted that the closed loop structure of the voltage control loop and the frequency control loop compensates for any degradation in the performance of components within the loop.

The precision of the frequency control loop was poor, particularly for measurement capacitance below 20pF. In fact the required 0.1% resolution is difficult to achieve even at much higher values of capacitance. However, a steady-state model that includes the effects of charge-feedthrough, the main source of error, was derived and proved to predict experimental behaviour with good accuracy. Based upon a review of candidate schemes in *Chapter* 2 the dummy switch compensation technique was selected for incorporation in integrated versions of the interface circuits. Jitter and locking observed in the frequency control loop was the other significant source of error. This error source was difficult to investigate on account of the variable parasitic nature of the discrete component circuit.

The final objective, the design of a low cost, minimum silicon area ASIC prototype of the interface circuits is the subject of the next chapter.

Chapter 5
The Integrated Implementation of the Interface Circuits

5.1 Introduction

An investigation of high-precision interfaces for capacitive sensors in an integrated form that have low power consumption, minimal area requirements and low cost was stated in *Chapter* 1 to be the fundamental aim of this research. Implementation with a standard-cell ASIC CMOS process was established as means of achieving this aim. Moreover, this approach permits integration on the same substrate of both the analogue interface circuitry, and the digital circuitry required for control purposes and for conversion of a frequency output to a digital word. Thus, sizable, power consumptive and costly multi-IC solutions are avoided. Potentially a complete node comprising sensor interfaces, digital processing and communications controller, and represented in *Fig.* 4, *p* 11, can be produced as a single IC. However the integration of analogue and digital circuitry on the same substrate is beset by one principal problem: coupling between digital and analogue portions, and in particular the coupling of digital logic switching transients into the analogue circuitry. Coupling can take the form of signal cross-talk (interference from one signal line to another) or result from communications via the power supplies [90]. The likely extent of the problem is not easily quantified although several measures can be taken to minimise its occurrence. Cross-talk can be reduced by partitioning of the digital and analogue portions; the use of guard-rings can also be of benefit. Power supply coupling can be eliminated by isolating the analogue and digital supply lines. A further precaution is the turning-off of digital circuitry whenever possible whilst the analogue circuitry is operating.

Measurements on discrete component, bread-boarded versions of the SC capacitance-to-voltage converter and the frequency control loop, reported in *Chapter* 4, demonstrated that accuracy is limited primarily by charge-feedthrough. The error contributed by these mechanisms is to first order directly proportional to the channel area of the switch and the gate-source and gate-drain overlap capacitances. Integration of the interface circuits using a small feature size CMOS process affords a smaller switch size with a corresponding reduction in feedthrough [58]. Onodera *et al.* [61] estimated that the injected charge for a NMOS switch with $W = 2\mu m$ and $L = 3\mu m$ would be 0.01pC without feedthrough cancellation, and Kondoh and Watanabe [53] claimed that an injected charge of 5fC could be achieved with cancellation. This latter figure is approximately three orders of magnitude less than that obtained for the discrete circuits reported in *Chapter* 4. Furthermore, an integrated approach allows for the inclusion of the precisely scaled dummy switches, discussed in §2.4.2, *p* 64, that are needed for compensation.

Stability was observed to be a problem with the discrete circuits. The frequency output of the frequency control loop was prone to random jitter caused by variable effects, such as hand and inter-line capacitance. These effects were reported in §4.4.3, *p* 120. It was expected that the stable parasitic environment of an integrated version would produce a repeatable frequency output and permit the investigation of schemes to compensate for this phenomenon.

In conclusion, the integration of the circuits under investigation potentially increases their precision and stability of operation whilst remaining in accordance with the wider research aims.

The following section describes the IC design process and details the CAD tools used. Next, the design of each interface circuit is covered prior to a description of the design of the full-custom switches. Finally, the test of the prototype ASIC is detailed concluding with an assessment of the performance of the integrated interface circuits.

5.2 Integrated Circuit Process Options

Two options for the production of integrated interface circuits were identified in §1.3, *p* 5, namely full-custom design and standard-cell design. The latter approach was considered to be commensurate with the project resources and aims and, accordingly, the ES2 Solo 1200 process was selected to implement the IC. However, as was detailed in §4.2.1, *p* 89, the ES2 evaluation ICs employed in the discrete experimentation stage were provided with an insufficient number of switches to construct the simplest interface circuit. Thus satisfactory characterisation of the switches was not possible nor was inclusion of the required dummy switches. Consequently it was necessary to include full-custom switches within the standard-cell IC. This section contains a description of the design procedure and CAD packages used in both the full-custom and standard-cell approaches in the realisation of the IC. The following description also reinforces the justification for the selection of a standard-cell approach as the main design method.

Full-custom design is complex, particularly when analogue components are included, demanding much design time and often more than one fabrication run. It is also the more costly option, as was discussed in §1.3, *p* 5. Essentially all the components, digital and analogue, are designed, simulated and laid-out at device level. The design flow comprises several distinct steps from an initial specification for an analogue component to a Caltech Intermediate Format (CIF) computer file that describes the desired physical layout of the circuit. However precise process parameters that characterise the operation of the active and passive devices must be provided before any initial design is undertaken. These parameters are obtained by the measurement of specially designed test structures fabricated using a particular process. Commercial silicon foundries provide their customers with these process parameters. The first step in the design procedure is approximate design by means of hand-calculation using some of the more basic process parameters. Having achieved a circuit performance that is moderately close to that required, the design can be improved

by the use of a circuit simulator. SPICE [91] is the most commonly used general purpose circuit simulator and manufacturers' process parameters usually correspond to its control parameters. Next, the circuit is laid-out using an appropriate CAD tool. The circuit layout is extracted to check its correctness and to obtain more precise information, e.g. regarding device areas and parasitics, and resimulated to gain a more accurate estimate of the fabricated circuit performance. If necessary the layout is modified and the circuit resimulated until the required performance is attained. The circuit can now be submitted for fabrication. More than one processing run may be required if a high precision or complex integrated analogue circuit is required. This procedure is often time consuming and costly but does give the designer complete freedom to produce optimally designed circuits.

A CMOS process with a standard-cell library, on the other hand, provides the designer with predesigned and characterised analogue components thus obviating the lengthy simulation-layout-resimulation procedure. Often a target specification can be met after one fabrication run. Unfortunately this simpler design procedure restricts the designer to a relatively small selection of library parts and limited or compromised performance. Hence this approach cannot produce optimally designed circuits although it is quicker and usually less costly than full-custom design.

As was stated in §1.3,*p* 5, the full-custom route was explored initially, as part of this project before selection of the standard-cell ES2 Solo 1200 process. *Appendix B* ,*p* 185 details the contents of a full-custom design fabricated in the Edinburgh Microfabrication Facility using a 3μm p-well CMOS process as part of this initial exploration. The microphotograph shows one of the two 5mm × 5mm dies required to implement the design. The design largely comprises test structures capable of providing SPICE parameters, since these were not provided. Also included are some switches, operational amplifiers and comparators that would permit the construction of simple interface circuits.

This initial approach, although offering the prospect of optimally designed analogue circuits, was discontinued on account of the time constraints imposed by the project lifetime in favour of the standard-cell route to integration, which afforded a quicker solution. As was stated above, the reduction in design and fabrication time was gained at the cost of the limited performance obtainable from standard-cell library parts. This important consideration was reflected in the perspective of the review in *Chapter* 2 where techniques that could circumvent this limitation were identified, and in the selection of the three interface circuits detailed in *Chapter* 3. In fact the investigation of high-precision integrated interface circuits for capacitance sensors using a standard-cell CMOS process is a novel feature of the research presented in this thesis.

The ES2 Solo 1200 CAD suite [23], selected to produce the IC, gives access to the ECDM20 2μm n-well CMOS process [92] and has an analogue cell library from which it was possible to implement the three interface circuits: the SC capacitance-to-voltage converter, the voltage control loop and the frequency control loop. As detailed above, the lack of characterised and compensated switches necessitated the inclusion of full-custom switches. Thus the design was, for the most part composed of standard-cell components with the addition of a few relatively easily designed full-custom elements. Modifications to the Solo 1200 design flow were required to effect this hybrid of full-custom and standard-cell processing. The modifications are detailed elsewhere [93, 94]. The design of the ASIC will now be detailed.

5.3 Integrated Interface Design

Five distinct circuits were included in the IC: four analogue interface circuits and a fifth digital communications circuit. This last circuit was a modification of a fieldbus node communications controller designed by Sylvan [24] using Solo 1200. The controller is equipped with a frequency counting input which would enable the ASIC to

operate as a remote node with the addition of some circuitry to control the frequency measurement time [95]. It would thus be feasible to construct a loop with several such nodes, as shown in *Fig.* 38. The design of the four interface circuits will now be described.

The SC capacitance-to-voltage converter, shown in *Fig.* 20, *p* 75, was implemented using OP-22 as the integrating amplifier. *Appendix A.* 1, *p* 182 contains data for OP-22 [23]. OP-22 is a high drive op-amp with a rail-to-rail output voltage swing; power consumption is 18mW. The control switches are not compensated with dummy switches and have a sufficiently large aspect ratio to allow the circuit to be clocked at high frequency without loss of accuracy. The switches were left uncompensated to permit comparison with an identical but compensated converter circuit accessible as part of the voltage control loop. The SC capacitance-to-voltage converter has an area of approximately 0.7 mm^2.

The voltage control loop, illustrated in *Fig.* 19, *p* 74, was similarly implemented with OP-22. The control switches are the same size as those in the SC capacitance-to-voltage converter but with half-size dummy switches for compensation. This circuit has an area of approximately 0.95 mm^2.

The remaining two interface circuits are both versions of the frequency control loop. The first was constructed with compensated switches that are identical to those in the voltage control loop and has a silicon area of 1.3 mm^2. The second has minimum sized compensated switches to further reduce feedthrough at the cost of a reduced maximum clock rate. This circuit has an area of 0.95 mm^2. In addition two-phase circuits, required for both switch blocks of this last circuit, are included on the IC in preference to that illustrated in *Fig.* 23, *p* 90 to reduce external circuitry and to therefore minimise any external parasitic effects. The two-phase circuit, shown in *Fig.* 39, is based on transmission-gate D-type flip-flops with assorted logic gates included to ensure that the switch control signals toggle in a particular order and with

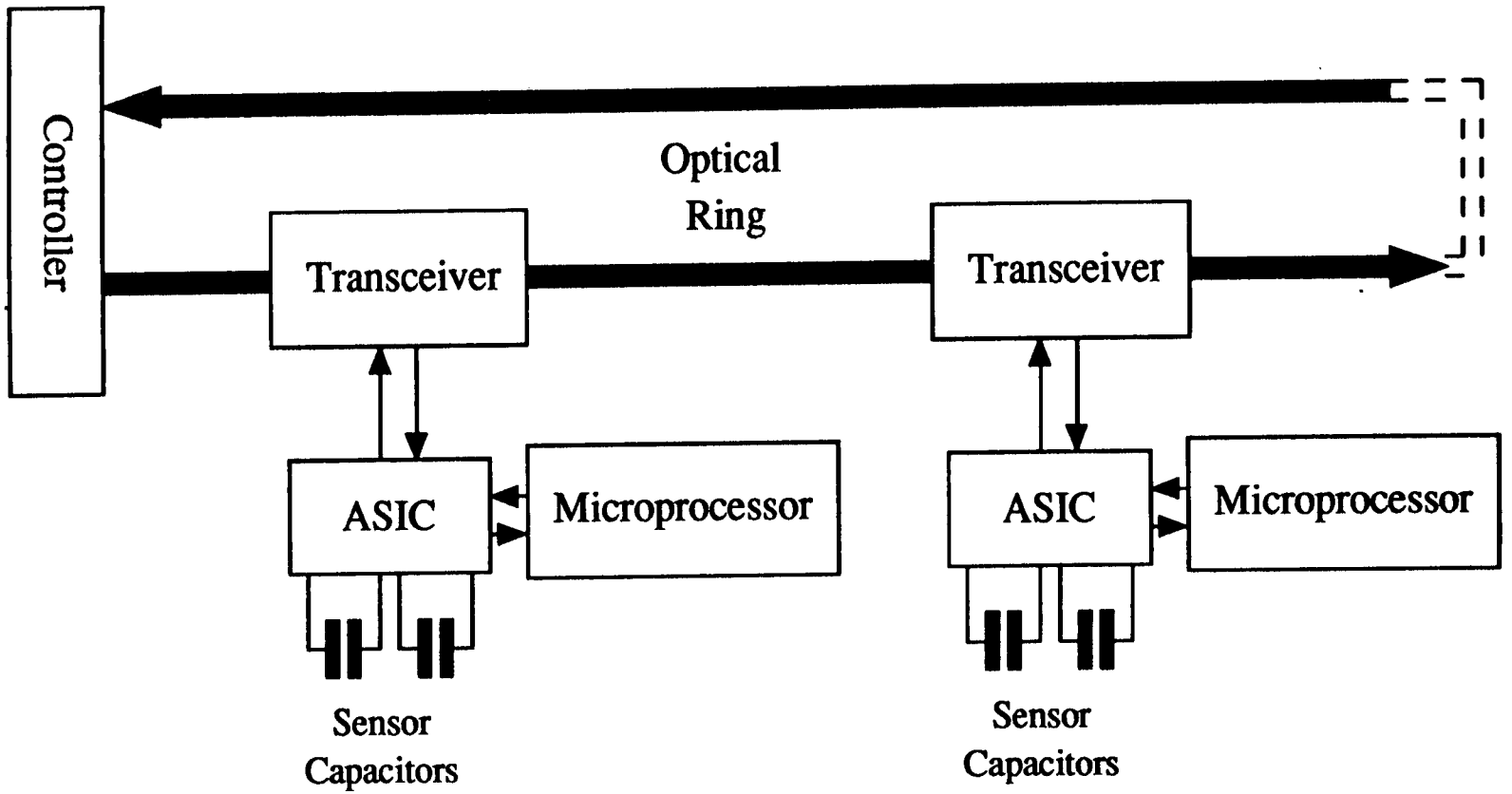


Figure 38: An instrumentation network based on an optical ring

the required delay to minimise feedthrough, as discussed in §2.4.1, *p* 59. *Fig.* 39 also shows the timing of the switch control signals. Referring to *Fig.* 40(*a*) 'phase11' drives switch M2, 'phbar11' drives its associated dummy switch M6, 'phase12' drives switch M1 and 'phbar12' drives dummy switch M5. The remaining four control signals drive control switches M3 and M4 and their associated dummy switches in a similar fashion. Both of these frequency control loop circuits use the low power OP-32 as the integrating amplifier and VCO1 as the voltage controlled oscillator. *Appendices A.2* and *A.3* contain data for OP-32 and VCO1 respectively [23]. OP-32 has a rated power dissipation of less than 1mW but a limited output voltage range, which limits the dynamic range of the frequency control loop. The reduction in dynamic range can be overcome as detailed in §4.5.2, *p* 123. In addition the bandwidth of OP-32 is significantly less than that of OP-22; the significance of the reduction will be detailed in the next section. The OP-22 operational amplifiers contained in the SC capacitance-to-voltage converter and the voltage control loop can however be accessed and used in the frequency control loop in place of OP-32. The output frequency range of VCO1 is controlled by the gain factor k, as detailed in §4.5.2, *p* 123, which is set with an external resistor and capacitor. The maximum output frequency of the VCO is 1MHz.

Care was taken with the IC design to provide for testability and to minimise the effects of design or processing faults. For example the four interface circuits are isolated from each other electrically and are constructed to allow for the interchange of their constituent sub-circuits. *Fig.* 41 illustrates the four interface circuits on the IC, and identifies the major components. *Appendix C*, *p* 187 contains pin-out details for the ASIC and a microphotograph of the fabricated device with a transparent overlay to identify the important features and the major components identified in *Fig.* 41. Of note is the partitioning of analogue and digital portions, stated as advantageous in minimising noise coupling in §5.1, *p* 129, with the analogue circuitry situated in the bottom peripheral area of the IC, isolated in this fashion from the digital circuitry in the core area. *Appendix C* also includes a brief description of the node

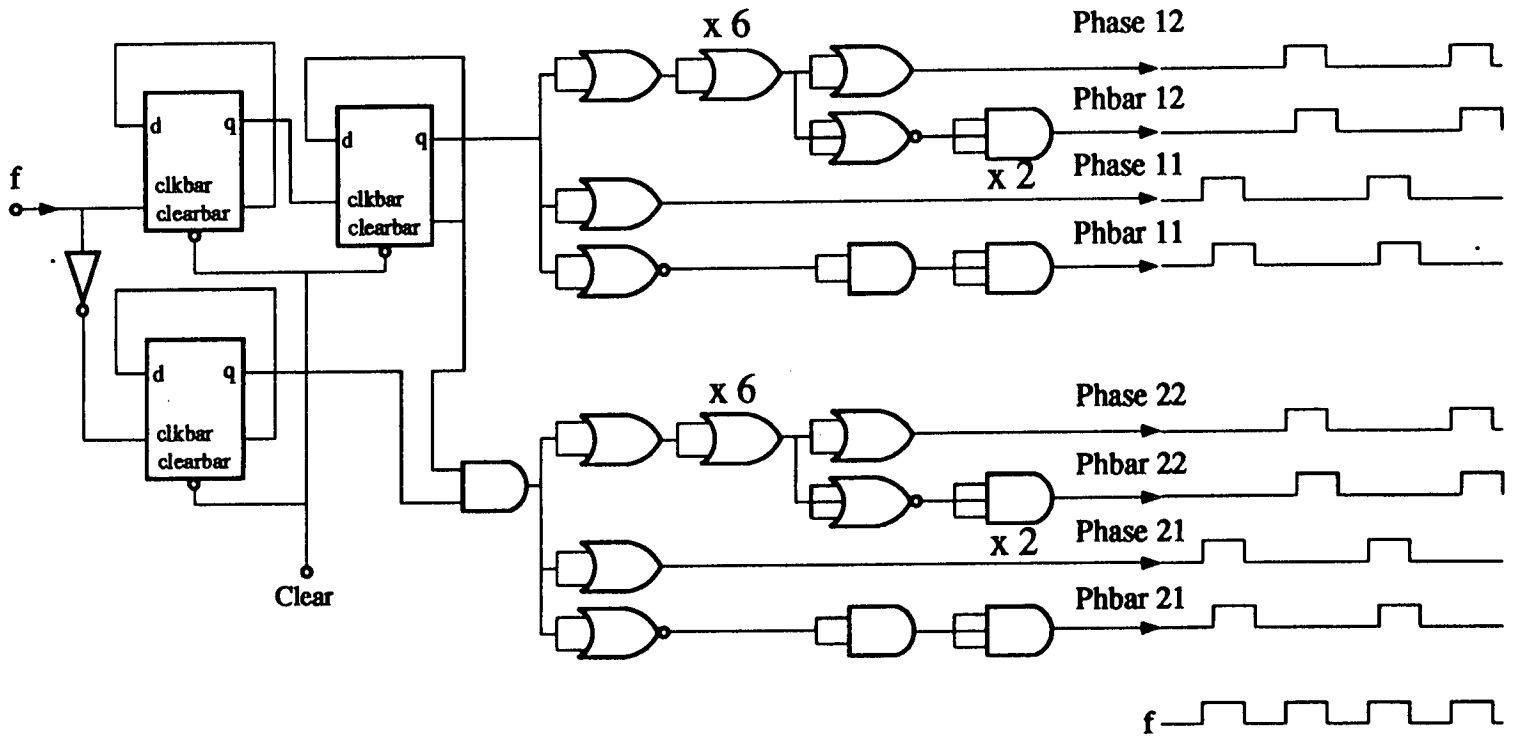


Figure 39: The integrated two-phase clock generator circuit

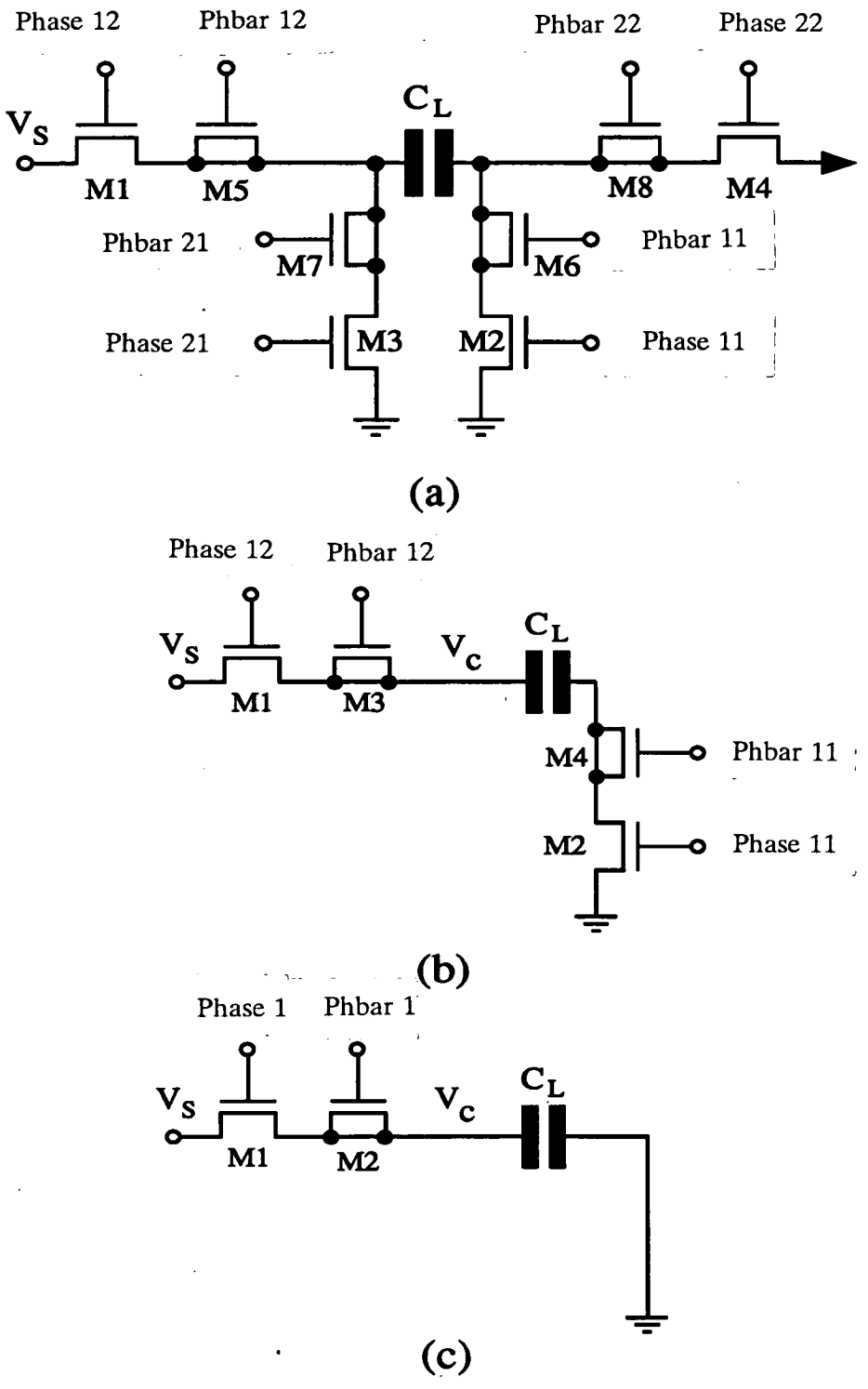


Figure 40: Three switch configurations, **(a)** a complete compensated switch block, **(b)** the switch arrangement that operates during clock phase 1 and **(c)** a single compensated switch

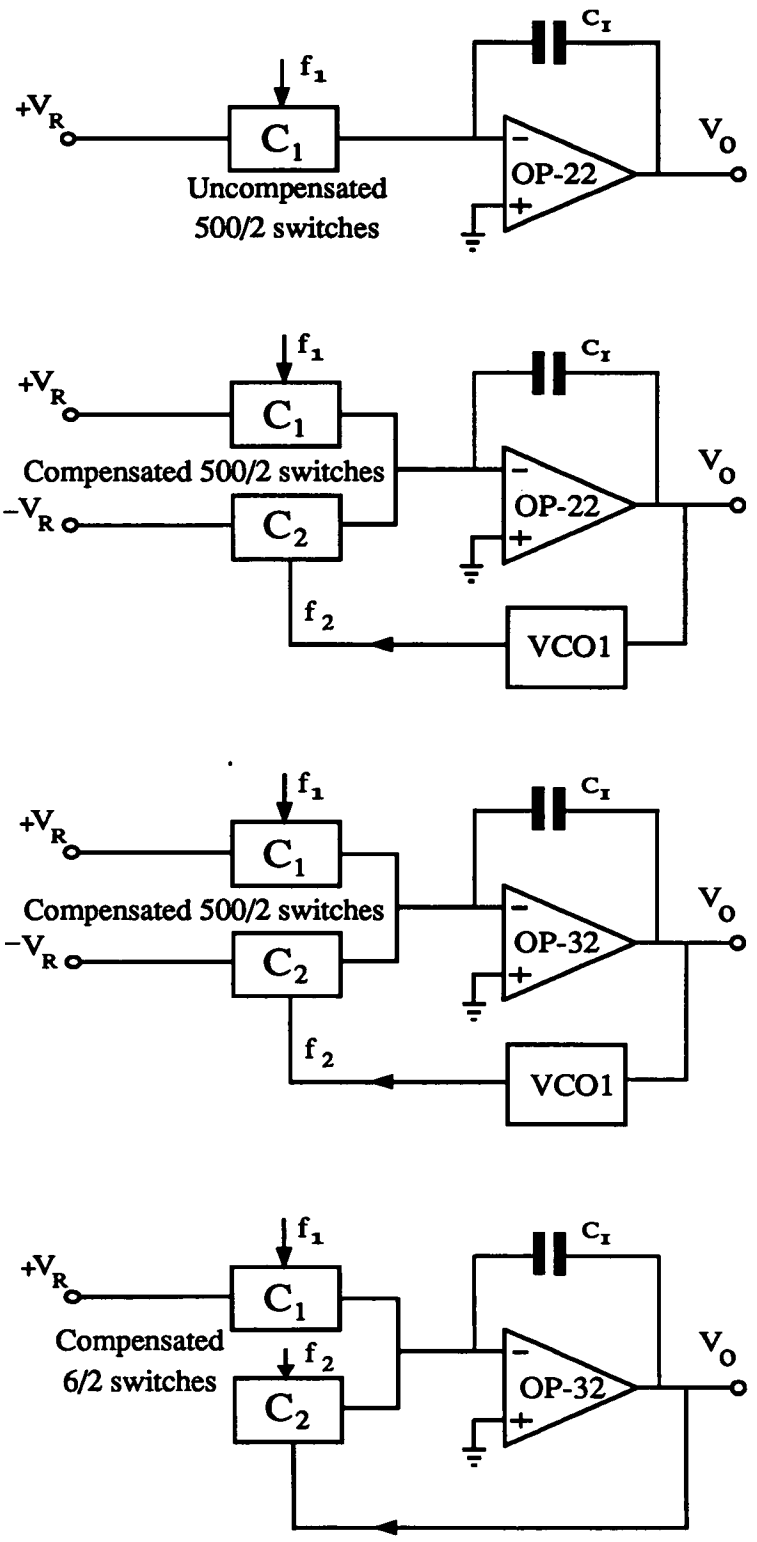


Figure 41: Diagram of the four integrated interface circuits identifying the analogue components and switch blocks

communications circuit. The design of the full-custom switches will now be detailed.

5.4 Full Custom Switch Design

Three sets of full-custom switches were designed for this IC: a set of uncompensated 500/2 aspect ratio switches, a set of compensated 500/2 aspect ratio switches and a set of compensated 6/2 aspect ratio switches. *Fig.* 40(*a*) shows a compensated eight-switch block. *Table* 2 below summarises the switch characteristics of each of the four interface circuits:

Full-Custom Switches		
Circuit	Compensated	Control Switch Size
SC Converter	No	500/2
Voltage Control Loop	Yes	500/2
Frequency Control Loop No. 1	Yes	500/2
Frequency Control Loop No. 2	Yes	6/2

Table 2

The gate terminals of the larger, 500/2 aspect ratio switches present a large capacitive load to their driving signals which necessitated the inclusion of buffer circuits. Buffer stages with a relative drive of 3-5 were chosen to minimise the propagation delay [96].

The general switch design and layout procedure and the computer packages used will now be detailed prior to a more detailed description of each type of switch block.

Following the full-custom method, described above in §5.2, *p* 131, initial design was by hand-calculation. The design was refined by simulation using HSPICE level 2 [97]. Layout and extraction of the switches was accomplished using Northwest LIS CAD package 'Magic'. Extracted data was post-processed using Northwest LIS computer packages 'ext2sim' and 'sim2spice' [98] yielding a SPICE format file for the final, accurate simulation. The detailed design of the switches for the SC capacitance-to-voltage converter will now be described.

Two conflicting priorities were encountered during the design of switches for the present application. Firstly, a switch with a small channel area injects less channel charge onto a measurement capacitor. Secondly, during the first phase of operation of a four switch block the measurement capacitor must be connected via the switches to the voltage source and ground for a sufficient length of time to allow the voltage on the capacitor to settle to within that required to achieve better than 0.1% accuracy. This settling time on the measurement capacitor is a first order function of the product of the measurement capacitance and the combined on-resistance of the two controlling switches and any line resistance present. The on-resistance, R_{ON}, of a MOSFET is directly proportional to the aspect ratio [44]:

$$R_{ON} = \frac{L}{\mu_o C_{OX} W (V_{GS} - V_T)} \tag{5.1}$$

Increasing the aspect ratio reduces R_{ON} at the cost of increased feedthrough. Accuracy and clock frequency requirements override charge-feedthrough considerations, consequently imposing a lower limit on the switch aspect ratio. NMOS switches were chosen since electron mobility, μ_o in *Eqn.* (5.1) above, is approximately double the hole mobility of PMOS switches.

A further design priority is ensuring that the settling time on C is sufficiently short to permit a clock frequency that is fast enough to obtain a resolution of 0.1% in the 20mS to 100mS measurement interval. The clock frequency should also be greater than 20kHz to minimise the aliasing of 1/f noise. For example a clock frequency, f_c,

of 50kHz yields a 0.1% resolution over a measurement time of 20mS.

Two mechanisms cause a loss in charge from the measurement capacitance. The channel resistance of a switch is ideally infinite when it is off. A typical value is in the range of $10^{12}\ \Omega$ [44] and this is not sufficiently large to be of concern. Leakage current, which is a combination of the subthreshold current, the surface-leakage current and package-leakage current, is of more importance. Typically this leakage current is $15.5mA/m^2$ at room temperature [83] and doubles for every $8°C$ increase in temperature [44]. For a switch with channel dimensions of $500\mu m$ by $2\mu m$, the largest switch size used in the IC, the leakage current is 15.5pA. This leakage current only affects the operation of the SC capacitance-to-voltage converter during a small stage of the two-phase clock cycle, described as follows. When one phase of the clock signal is high the measurement capacitor is connected to a voltage source, i.e. during the period when ϕ_1 is high the sensor capacitor, C_L in *Fig.* 42, is connected to the voltage source V_S; while ϕ_2 is high C_L is connected to the output of the amplifier via the integration capacitor C_I. Hence leakage does not reduce the charge on C_L during these periods. Charge is only effectively lost during the gap between the positive pulses of the two-phase signals. The SC capacitance-to-voltage converter, the voltage control loop and the first frequency control loop, which are without on-chip two-phase circuitry, require the external two-phase clock generator circuit illustrated in *Fig.* 23, *p* 90, where the gap between the two phases is determined by the settling time on the two sets of resistors and capacitors. This gap is at most 500nS resulting in a total charge loss on the measurement capacitance of 0.031fC through the four switches. This error is an insignificant 0.0006% of the charge stored on a 5pF capacitor charged to 1 volt and does not compromise accuracy, even over the full industrial temperature range. The second frequency control loop has a different design of two-phase generator that has a gap between clock phases equal to the phase length. *Fig.* 39 shows the circuit and its timing diagram. The leakage current is now inversely proportional to the clock frequencies in the control loop. At the minimum clock frequency of 20kHz the charge

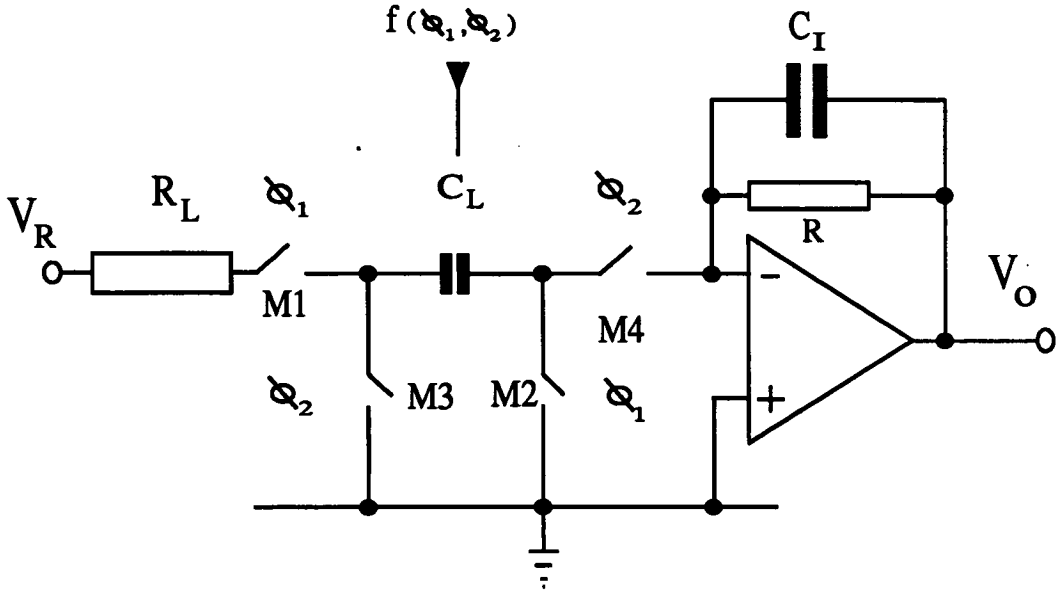


Figure 42: The non-inverting capacitance-to-voltage converter including the lumped component R_L representing the interconnect resistance

lost from the measurement capacitance through four 6/2 aspect ratio switches is 0.001fC. Thus the increase in leakage time is more than compensated for by the reduction in the switch channel area.

The final important aspect of operation of the switch is the range of voltages on the switch terminals compared to the switch gate voltage. Consider the operation of the SC capacitance-to-voltage converter shown in *Fig.* 42. As the voltage V_S approaches $V_{DD} - V_T$, where V_{DD} is the gate on voltage, i.e. the positive supply, and V_T is the threshold voltage, the switch $M1$ starts to turn off. This effect further reduces the maximum voltage obtainable on the capacitance C_L since it is intended to operate the interface circuits from low voltage supplies of ± 2.5 volts. Consequently, error voltage levels, feedthrough or noise for example, are proportionately greater with respect to this maximum voltage.

The design of each switch type will now be detailed considering each of the above design aspects in turn. For the SC capacitance-to-voltage converter illustrated in *Fig.* 42 assume the maximum measurement capacitance to be 50pF and the maximum line resistance, R_L, to be 200 Ω based on a maximum length of 10 mm of metal for the ES2 ECDM20 process [23]. V_{DD} was set at 2.5 volts and V_{SS} at -2.5 volts. An HSPICE simulation showed the voltage V_C on C_L in *Fig.* 40(b) to settle to within 0.05% of 1 volt in 140nS, when the aspect ratio of the two NMOS transistors was 500/2. *Appendix D.*1, *p* 194 shows a sample HSPICE input file used to obtain this result. Including a factor of ten safety margin the switches must be on for a minimum of 1.4μS. An estimated maximum frequency of operation of 357kHz results, since a two-phase clock scheme is required to operate a complete switch block. The maximum clock frequency for the circuit, f_c, is set by the circuit settling time requirement of $f_o \geq 5f_c$, where f_o is the unity gain bandwidth of the operational amplifier, as detailed in §3.6, *p* 84. f_o for OP-22 is typically 2.8MHz, therefore imposing an upper limit on f_c of 560kHz for the SC capacitance-to-voltage converter.

The transfer function of the NMOS transistor with a 500/2 aspect ratio was simulated and the output terminal reached a maximum of 1.3 volts when the gate voltage was 2.5 volts; this corresponds to a maximum voltage range of ± 1.3 volts on the sensor capacitance of each of the three interface circuits when operated from ± 2.5 volt supplies. A sample HSPICE input file is shown in *Appendix D.2, p* 195.

The design of the compensated switch block for both the voltage control loop and the first of the two frequency control loops will now be described. The controlling switches of these two circuits have the same aspect ratios as those in the uncompensated switch block of the SC capacitance-to-voltage converter, as summarised in *Table* 2. As a result the above on-resistance and leakage current calculations apply. The first frequency control loop has OP-32 as its integrating operational amplifier, which has a unity gain bandwidth of 310kHz - considerably lower than that of OP-22. Consequently the maximum clock frequency of the circuit is 62kHz according to $f_c \leq 5f_o$. Should a faster clock be required, to obtain increased resolution for instance, an OP-22 amplifier can be accessed from the SC capacitance-to-voltage converter to increase the maximum clock frequency to 560kHz, as calculated above. When operated with OP-22 the first frequency control loop has a 12-bit resolution for a measurement time of 20mS, if the clock frequency is taken to be the conservatively estimated 350kHz obtained from the sensor capacitor rise time calculation above. With OP-32 and a maximum frequency of 62kHz a 10-bit resolution is attainable in a 20mS measurement time.

The circuit of *Fig.* 40(*c*) was simulated using HSPICE to obtain an estimate for the likely magnitude of the charge-feedthrough in the compensated and uncompensated switch blocks. The HSPICE option 'CAPOP=4' was set to select the channel charge conservation model [97] and the gate voltage rise and fall times were set at 0.5nS, a figure that is in accordance with a typical ES2 Solo 1200 inverter propagation delay of 0.7nS [23]. A feedthrough charge of -1.1pC was obtained on the measurement capacitance C_L without operation of the compensating switch M2. With half-size dummy

switch M2 of aspect ratio 250/2 the feedthrough charge on C_L was reduced to 250fC. A sample HSPICE input file is shown in *Appendix D.3, p* 196. It should be noted that the absolute accuracy of the error charge magnitude is doubtful, since the simulation results were sensitive to the particular HSPICE model or algorithm used. However, the results do demonstrate that dummy switch compensation does effect a relative reduction in the feedthrough charge contributed by a single switch.

A microphotograph of the layout of a compensated switch block is shown in *Appendix E, p* 197. A transparent overlay identifies the important features. Note that a P-diffusion guard ring, connected to ground and in a n-well, surrounds the switches to minimise the occurrence of latch-up and to reduce the coupling of transient noise to and from the switches [99]. Guard rings were included in all the switch blocks.

The final switch block for the second frequency control loop consists of compensated minimum sized switches to reduce the feedthrough effects further. The controlling switches and the dummy switches have aspect ratios of 6/2 and 3/2 respectively. A conservative estimate for the maximum permissible clock frequency, determined from the settling time requirement on the sensor capacitance as detailed above, was 33kHz and the HSPICE simulated maximum switch output voltage was 1.2 volts. The feedthrough error without and with dummy switch compensation was -11fC and less than 0.5fC respectively. Note that the compromise for the reduction in charge-feedthrough is an estimated decrease in the possible resolution to 10-bits over an 40mS measurement time, although the considerable factor of ten safety margin introduced in the calculation of the settling time on C should allow for a faster clock frequency up to the 62kHz maximum imposed by the settling time requirement on OP-32. Thus a maximum resolution of 10-bits for the shorter measurement time of 20mS is possible. Note that OP-32 can be replaced with OP-22 to circumvent the 62kHz maximum frequency limitation, but at the cost of increased power consumption.

To achieve independence of charge-feedthrough and charge-injection from source voltage each control switch terminal was made independently accessible external to the IC, permitting those at earth or virtual-earth potential to be turned-off first, as detailed in §2.4.1, *p* 59. Unfortunately a shortage of IC package pins did not allow for the dummy switches to be made operable independently from their associated control switches. Consequently the effects of delay between operation of control and dummy switches, discussed by Eichenberger and Guggenbuhl [75], and reported in §2.4.2, *p* 64, could not be investigated.

The effectiveness of the dummy switch compensation technique can be assessed as follows. As was stated in §2.4.2, if the switching time is of the order of the channel transit time of the switch then compensation is guaranteed even for unsymmetrical source and drain impedances. Using *Eqn.* (2.9), for the transit time:

$$T_O = \frac{n_o L^2}{\mu(V_H - V_T)}$$

where

$$n_o = 1 + \frac{\gamma}{\sqrt{\Phi_f}},$$

$$\gamma = \frac{\sqrt{2\,\epsilon_{si}\,q\,N_{SUB}}}{C_{OX}},$$

$$\Phi_f = \frac{kT}{q}\ln\left(\frac{N_{SUB}}{n_i}\right),$$

L is the channel length, V_H the high gate voltage, μ is the carrier mobility, V_T is the threshold voltage, ϵ_{si} is the permittivity of silicon, q is the charge on an electron, N_{SUB} is the dopant density, n_i is the intrinsic carrier concentration, k is Boltzmann's constant and finally T is the temperature. Evaluating for the ECDM20 process at ambient temperature [44,92], and for V_H = 2.5 volts, yields a transit time of 9.1×10^{-11} seconds. As detailed above, the switching time was assumed to be 0.5nS, a value that is approximately five times the channel transit time figure, thus ensuring effective

compensation of charge-feedthrough.

Finally, the dependence of charge-feedthrough upon sensor capacitance should be considered. In §4.3.3, *p* 107 the discrete SC capacitance-to-voltage converter was observed to have a net feedthrough charge that was significantly dependent upon the sensor capacitance. Considering *Eqn.* (2.6) and *Eqn.* (2.8), the slow and fast gate turn-off charge-feedthrough expressions, both exhibit dependence on load or, in the case of the present application, sensor capacitance. For a typical CMOS process the dependence upon sensor capacitance variation of the fast turn-off expression is significantly smaller than that of the slow turn-off expression. Clearly fast turn-off behaviour is required of both the 500/2 and 6/2 aspect ratio switches if this source of error is to be minimised. For fast turn-off [73]:

$$\frac{\beta V^2_{HT}}{2C_L} \ll U$$

where $V_{HT} = V_H - V_S - V_T$.

Evaluating for the 500/2 aspect ratio switch under worst case conditions, where $\beta = 7.7\times10^{-3} A/volt^2$ [92], $V_{HT} = 2.6\ volts$ and $C_L = 10pF$, yields $\frac{\beta V^2_{HT}}{2C_L} = 2.6\times10^9$. If the gate fall time is assumed to be 0.5nS, as detailed above, then $U = 1\times10^{10} V/s$. Thus, the fast turn-off condition is satisfied. Considering that β for the 6/2 aspect ratio switch is $1.34\times10^{-4} A/volt^2$ then fast turn-off is also guaranteed.

5.5 Test of the Prototype ASIC

The test of the prototype ASIC comprised of three phases. Firstly, measurements were made on dummy switch compensated and uncompensated switches. Secondly, the performance of compensated and uncompensated SC capacitance-to-voltage

converters was investigated. Finally, the charge-feedthrough compensated SC frequency control loop was investigated.

The charge-feedthrough compensated and uncompensated single switch arrangements, accessible as part of SC frequency control loop No.1 and the SC capacitance-to-voltage converter respectively, were used to obtain measurements of the charge feedthrough, δq, as the source voltage, V_S was varied from -1 to + 1 volts. The experimental set-up is illustrated in *Fig.* 40(b). Both the compensated and uncompensated control switches have aspect ratios of 500/2, as detailed in *Table* 2. The results are presented in *Table* 3 below along with the best and worst feedthrough charge figures obtained from the measurement of a set of discrete M4016 switches, as detailed in §4.3.4, *p* 112.

Charge-Feedthrough in a Single Switch		
Switch type	δq	
	V_S = -1volt	V_S = + 1volt
Discrete M4016 switches	best:-0.5pC worst:-2.2pC	best:-1.5pC worst:-3pC
Uncompensated integrated switch	-1.29pC	+0.64pC
Compensated integrated switch	-0.37pC	+0.2pC

Table 3

Referring to *Table* 3, the compensated switch effects a factor of three reduction in charge-feedthrough magnitude when compared with the uncompensated integrated switch. The uncompensated integrated switch has a charge-feedthrough magnitude that is as low as the discrete switches with the best charge-feedthrough characteristics,

and a magnitude that is approximately three times lower than those with the worst feedthrough characteristics. Thus the compensated integrated switch has a charge-feedthrough magnitude that is an order of magnitude lower than that of the worst discrete switches. Note that the measured charge-feedthrough magnitudes for the uncompensated and compensated single switch arrangements are close to the HSPICE predicted figures of -1.1pC and -250fC respectively, as detailed in §5.4, *p* 140. Having confirmed the accuracy of the HSPICE simulations, a repetition of the simulation of the circuit arrangement shown in *Fig.* 40(*c*), with the aspect ratio of M2 increased to 325/2, resulted in a charge-feedthrough magnitude of -1fF.

Considering the fast and slow turn-off expressions *Eqn.* (2.6) and *Eqn.* (2.8) for charge-feedthrough in an NMOS switch, the former predicts an increase in charge-feedthrough with increasing source voltage, V_S, and the latter a decrease in charge-feedthrough with increasing V_S. As was detailed in §4.3.4, *p* 112 and §5.4, *p* 140 fast turn-off charge-feedthrough behaviour is required if minimal dependence of charge-feedthrough on load capacitance is to be gained. Inspection of *Table* 3 reveals that δq for both the uncompensated and compensated switches increases as the source voltage, V_S, is increased from -1 to +1 volts. Therefore the fast turn-off expression, *Eqn.* (2.6), models the charge-feedthrough contributed by the integrated switches:

$$q_{dm} = (C_{gd} + \frac{C_{ox}}{2}) \left(\frac{\beta V^3_{HT}}{6UC_L} - V_{HT} \right) + C_{gd}(V_L - V_S - V_T)$$

where

$$V_{HT} = V_H - V_S - V_T,$$

Re-arranging *Eqn.* (2.6):

$$q_{dm} = C_{gd} \left(V_L - V_H + \frac{\beta V^3_{HT}}{6UC_L} \right) + \frac{C_{ox}}{2} \left(V_S + V_T - V_H + \frac{\beta V^3_{HT}}{6UC_L} \right) \qquad (5.2)$$

where

$$\beta = 0.7\mu_O C_{ox} \frac{W}{L}$$

for operation of an NMOS switch within the non-saturation region [44].

Eqn. (5.2) was evaluated to assess the validity of the fast turn-off model by determining U, the gate fall-rate, using experimental parameters and measurements, and IC process parameters. The experimental parameters were: V_H = +2.5 volts; V_S = 0 volts; V_L = -2.5 volts; and q_{dm} = -1pC. The process parameters were as follows [92]: C_{gd} = 75fF; C_{ox} = 862fF; β = $7.7\times10^{-3} A/volt^2$; V_T = 0.9 volts; and C_L = 20.1pF. Calculated in this fashion $U = 1.16\times10^{10} V/s$. This figure corresponds to a fall-time on the gate of the switch from +2.5 to -2.5 volts of 0.42nS. Although fall-time data was not provided by ES2 the high-to-low propagation delay of an inverter from input to output, a longer measurement than fall-time, was typically 0.7nS [23]. This value is in agreement with the figure of 0.42nS for the fall-time obtained above. From *Eqn.* (5.2) above, q_{dm} is dependent on U and the load capacitance, C_L, via the term $\frac{\beta V^3_{HT}}{6UC_L}$. Further confirmation of the validity of the fast turn-off model was provided by comparing measured charge-feedthrough, q_{dm}, as C_L was varied, with q_{dm} evaluated from *Eqn.* (5.2) using the figure of $1.2\times10^{10} V/s$ for U. The measured values for q_{dm} were accurate to within 10% of those calculated from *Eqn.* (5.2).

Having determined the validity of the fast turn-off expression and obtained a value for U an estimate for the charge-feedthrough for the smaller 6/2 aspect ratio switches contained within frequency control loop No.2 can now be made. Evaluating *Eqn.* (5.2) for V_H = +2.5 volts, V_S = 0 volts, V_L = -2.5 volts, V_T = 0.9 volts, C_{gd} = 0.3fF, C_{ox} = 10.4fF, $\beta = 1.34\times10^{-4} A/volt^2$, C_L = 20.1pF and $U = 1.16\times10^{10} V/s$ yields a value of -10fC for q_{dm}. This figure is two orders of magnitude smaller than that obtained for the 500/2 aspect ratio switch under the same circuit conditions; it is also very close to the value of -11fC predicted by HSPICE. Furthermore the dependence of q_{dm} upon C_L via the term $\frac{\beta V^3_{HT}}{6UC_L}$ in *Eqn.* (5.2) is reduced, since $\beta = 0.7\mu_O C_{OX} \frac{W}{L}$. Thus the reduction of the control switch aspect ratio from 500/2 to

6/2 reduces β by nearly two orders of magnitude reducing in turn the dependence of q_{dm} upon C_L. These result cannot be confirmed experimentally, since access cannot be gained to individual switches within frequency control loop No.2.

The relationship between V_S and V_C in the circuit arrangement of *Fig.* 40(b) was explored to determine the maximum voltage that can be stored on C_L; this in turn imposes a limit to the maximum switched-capacitor stage reference voltage in all of the interface circuits. Measurement yielded a voltage range of -2.5 to +1.4 volts on V_C, for V_S varied from -2.5 to +2.5 volts as the gate voltage, V_G, was clocked between -2.5 and + 2.5 volts. Note that the switch threshold voltage prevents V_C from tracking V_S above +1.4 volts, as described in §5.4, *p* 140. This experimentally obtained result is close to that obtained from HSPICE simulations, as detailed in §5.4.

The final measurement made in the first phase of tests was that of the settling time on the capacitance, C_L, in the arrangement of *Fig.* 40(b). The settling time imposes a limit to the accuracy of capacitance measurement as described in §5.4. When M1 is a 500/2 switch the voltage V_C settles to within 0.05% of V_S within 94nS, after switch turn-off. Making a pessimistic estimate of twice this figure for operation of a two-phase clock circuit of the type illustrated in *Fig.* 23, *p* 90 results in a maximum frequency of operation of 5.2MHz. This measured figure is significantly greater than the 357kHz obtained from a conservative estimate based upon HSPICE simulations, as described in §5.4. The estimate for the maximum frequency of operation of frequency control loop No.2, with its 6/2 aspect ratio control switches, can be modified to 165kHz adjusting for the reduction in switch on-resistance. This frequency corresponds to a maximum pulse count of 3300 in 20mS, i.e. an 11-bit resolution.

Summarising thus far, two important results have been obtained. Firstly, experimental measurements of charge-feedthrough have agreed with both hand-calculations and HSPICE simulations. The accurate predictive abilities of HSPICE would permit the future design of more accurately compensated switches, in contrast with the rule-

of-thumb half size dummy switch approach used for the prototype IC. Secondly, the measured settling time on the sensor capacitance was considerably shorter than the pessimistic design figures detailed in §5.4, *p* 140. Consequently minimum feature size switches, with their significantly smaller charge-feedthrough, would permit 11-bit resolution within the 20mS measurement time. An increased settling time dependent resolution requires the use of larger aspect ratio switches with their increased charge-feedthrough.

The second phase of measurements, on the SC capacitance-to-voltage converter, will now be detailed. The experiment of §4.3.4, *p* 112 was carried out on the uncompensated SC capacitance-to-voltage converter, and the two compensated SC capacitance-to-voltage converters accessible as part of frequency control loop No.1. *Fig.* 20(*a*), *p* 75 shows the experimental set-up, with R_f =919k f =20kHz, V_{ref} = 1 volt and C_I = 0.022μF. *Fig.* 43 shows the results of output voltage V_{out} with varying sensor capacitance, C_L. The line designated '+' is that obtained in §4.2.2, *p* 91 from the discrete circuits. The lines designated '*', 'o' and 'x' are those obtained for the first order theory given by *Eqn.* (3.2), and for the uncompensated capacitance-to-voltage converter and the compensated capacitance-to-voltage converter respectively. *Fig.* 43 illustrates that both integrated versions of the circuit exhibit significantly improved behaviour in comparison with the discrete circuit. The effectiveness of the dummy switch compensation technique is, however, not apparent from inspection of *Fig.* 43.

To provide a better indication of the effectiveness of the cancellation technique the charge feedthrough coefficients m and Q of *Eqn.* (4.3) were determined experimentally for the integrated circuits, as detailed in §4.3.4, *p* 112, at a sensor capacitance of 10pF. The results are summarised in *Table* 4 below:

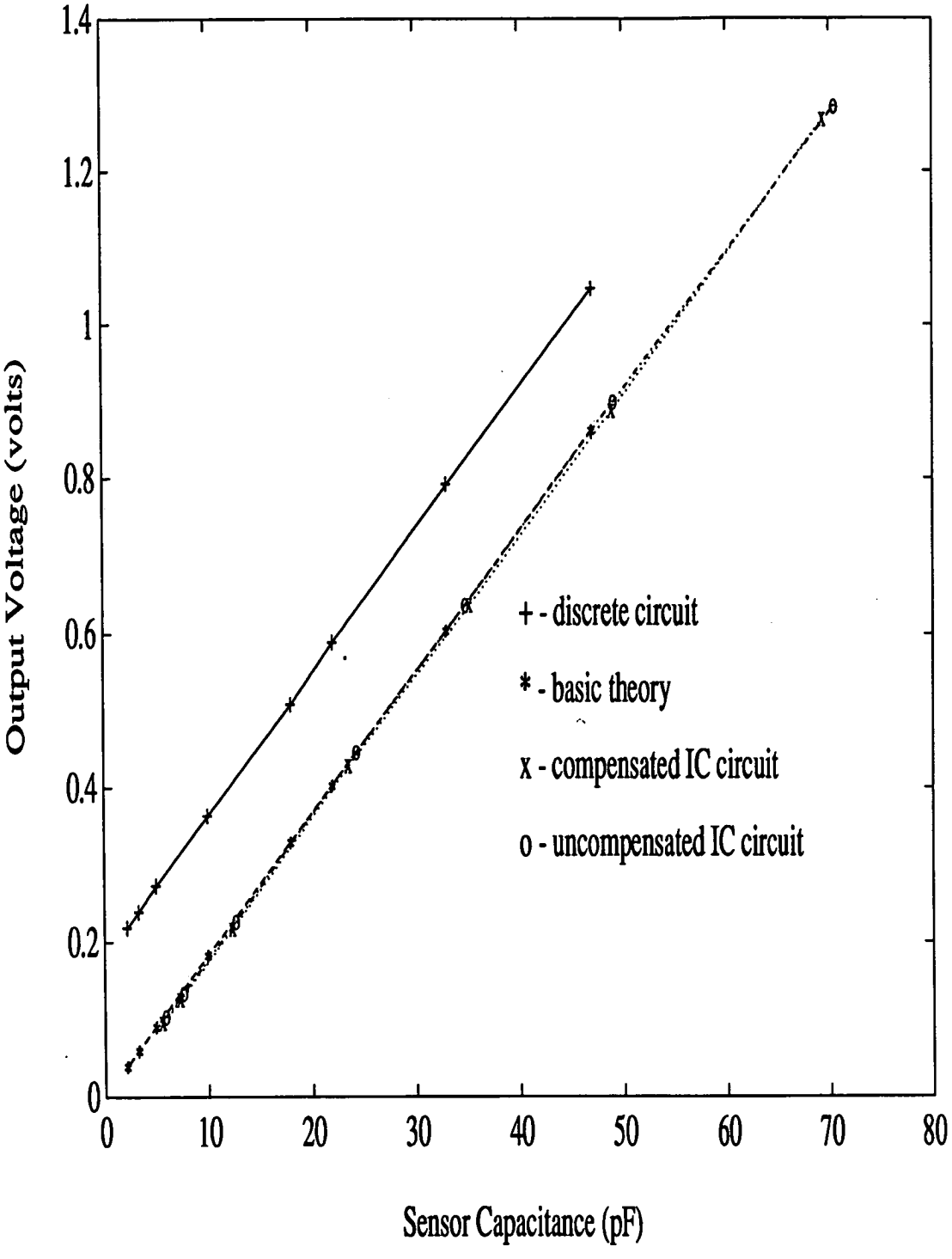


Figure 43: Output voltage against sensor capacitance for the capacitance-to-voltage converter for the discrete component circuit, the basic theory, and the compensated and uncompensated integrated implementations

Charge-Feedthrough Coefficients		
Capacitance-to-Voltage Converter	m	Q
Discrete circuit	0 to 5pF	0 to 10pC
Uncompensated integrated circuit	-0.135pF	-0.422pC
Compensated integrated circuit No.1	-0.281pF	-0.557pC
Compensated integrated circuit No.2	+0.54pF	-0.945pC

Table 4

Comparing the uncompensated and discrete capacitance-to-voltage converters, the former demonstrates a considerable improvement over the latter. However, compensation has not improved the performance of the integrated version contrary to what was indicated by the measurements on the single switch configuration. In fact the compensation technique has increased the magnitude of both m and Q in both the compensated capacitance-to-voltage converter circuits. Measurements on several other ICs and on the compensated capacitance-to-voltage converter accessible as part of the voltage control loop have revealed m and Q to be dependent on processing spreads, and more significantly on the IC layout of the particular switch-block under measurement. Moreover m and Q are dependent on the sensor capacitance. For example for compensated integrated converter No.1 of *Table* 4 above at a sensor capacitance of 68pF, m = -0.155pF and Q = -0.071pC, a three to four-fold reduction over the uncompensated integrated converter circuit. This factor of reduction in m and Q corresponds to the reduction in δq for the single switch arrangement. Further work is required to investigate the influence of IC layout and processing spreads on the effectiveness of dummy switch charge-feedthrough compensation.

The final set of measurements were carried out on frequency control loop No.1. The frequency ratio, $\frac{f_2}{f_1}$, was measured as the sensor capacitance was varied, maintaining $C_1 = C_2$. Referring to *Fig.* 21(*a*), *p* 77, f_1 was set at 20kHz, C_I set at 0.22μF and $|V_{ref}|$ set at 1.025 volts. The results are plotted in *Fig.* 44, designated '+', along with those obtained from the second-order circuit expression *Eqn.* (4.7), designated 'o', where m_1, Q_{O1}, m_2 and Q_{O2} are as detailed for compensated capacitance-to-voltage converters Nos.1 and 2 in *Table* 4 above. *Fig.* 44 demonstrates a significant improvement in performance of the integrated frequency control loop over that of the discrete version of the circuit, illustrated in *Fig.* 36, *p* 116. Comparing measured and theoretical results, this figure confirms the validity of the second-order theory, although their frequency ratios are offset by 0.05 over the sensor capacitance range 10-70pF. A systematic error in the measurement of the sensor capacitance is the probable cause of, or at least a contributing factor to, this offset. Further measurements would require more accurate measurement techniques. Referring to *Fig.* 44, the measured curve indicates that above $C_1 = C_2 = 20$pF, a constant frequency ratio of approximately 1.04 is obtained. This represents an offset error of approximately 4% of the frequency ratio of one that is required for circuit operation according to first-order theory. Although this error could be reduced by calibration the probable sensitivity of the offset error to temperature variations might require a reduction in its magnitude if 10-bit resolution is to be achieved over the industrial temperature range. Noting from above that the measured charge-feedthrough for 500/2 and 6/2 aspect ratio switches is -1pC and -10fC respectively at a source voltage of zero, a considerable reduction in the offset error would be achieved by using the smaller switch size. Furthermore, as detailed above, the settling time on the sensor capacitance is sufficiently short with the smaller switch size to permit the conversion of a capacitance ratio to a frequency ratio within the required 20mS measurement interval and with a possible precision of 11-bits.

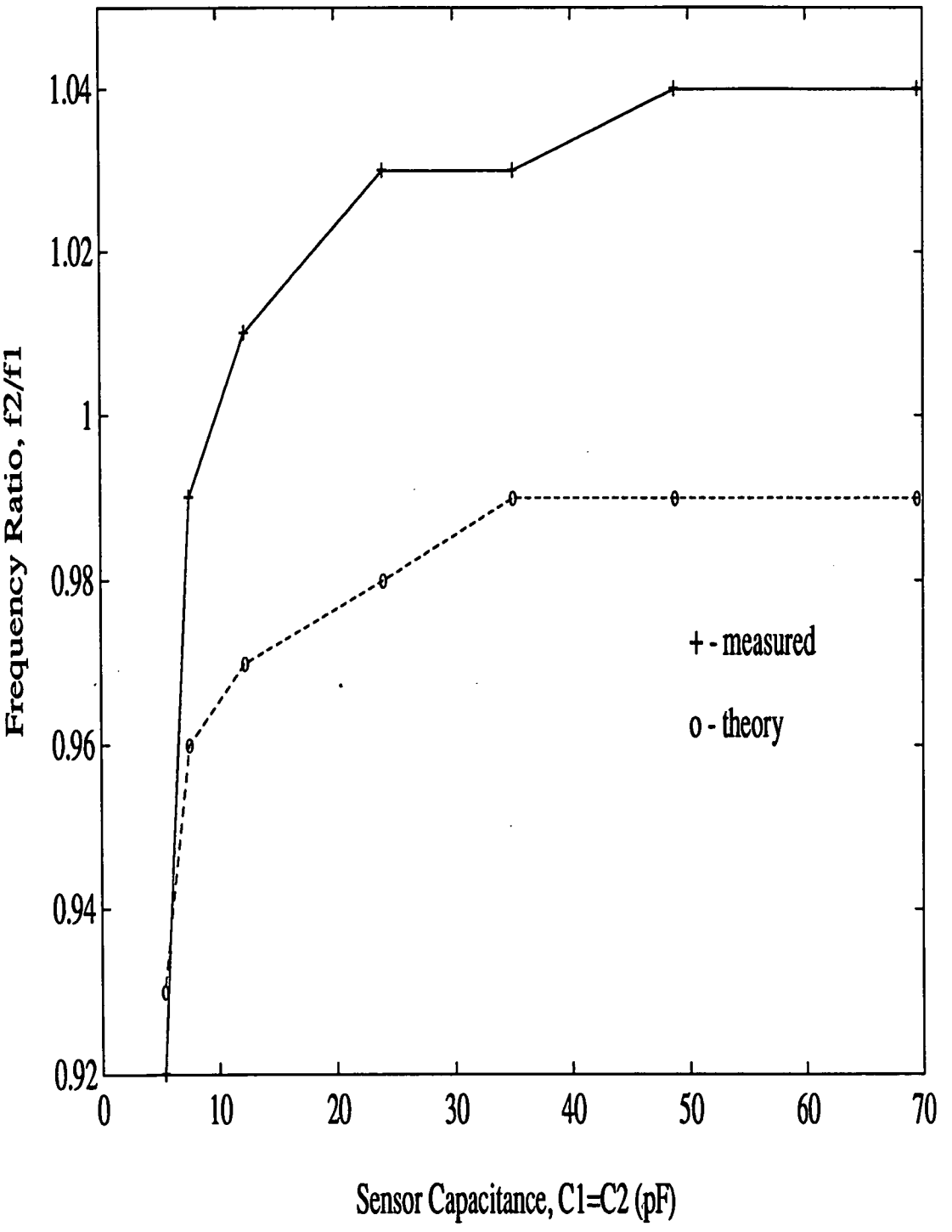


Figure 44: Measured and 2nd order theoretical frequency ratio against absolute sensor capacitance for the frequency control loop

The above experiment on frequency control loop No.1 was repeated with $C_1 \neq C_2$. Three lines of frequency ratio, $\frac{f_2}{f_1}$, against sensor capacitance ratio, $\frac{C_1}{C_2}$, for C_2 = 22pF, 33pF and 47pF, are shown in *Fig.* 45. All three lines are straight as required of circuit operation according to first-order theory, *Eqn.* (3.6), with the presence of small gain and offset errors that are consistent with the offset error of *Fig.* 44. The accuracy of conversion of capacitance ratio to frequency ratio is at worst 2% for the data represented in *Fig.* 45. Close inspection of *Fig.* 45 reveals that the three lines are not completely coincident and have slight non-linearities. This behaviour is consistent with the variation of the feedthrough coefficients with load capacitance in the integrated SC capacitance-to-voltage converter, and with *Eqn.* (4.7) which predicts a varying gain and offset error as C_2 is varied. A more detailed analysis of conversion precision would require further investigation using more accurate measurement techniques, particularly of sensor capacitance. This remains as part of a plan for future work. As detailed above, use of the smaller 6/2 aspect ratio switches, such as are present in frequency control loop No.2, is expected to reduce charge-feedthrough based errors by two orders of magnitude. However the need for more accurate test equipment dictates that the test of this second, more accurate frequency control loop should remain as part of future work.

Jitter in the output frequency, which was the second significant source of error in the discrete version of the frequency control loop, was reduced considerably. Further work is required to determine the magnitude of the jitter error in the integrated version, and to investigate the effect of C_I, the smoothing capacitor, which is now observed to influence the jitter magnitude in a more obvious and repeatable fashion. Most importantly no locking of the output frequency, f_2, to the reference frequency, f_1, was observed.

The validity of the settling time expression, *Eqn.* (4.15), was demonstrated. Further work is required to investigate the interdependence of settling time, dynamic

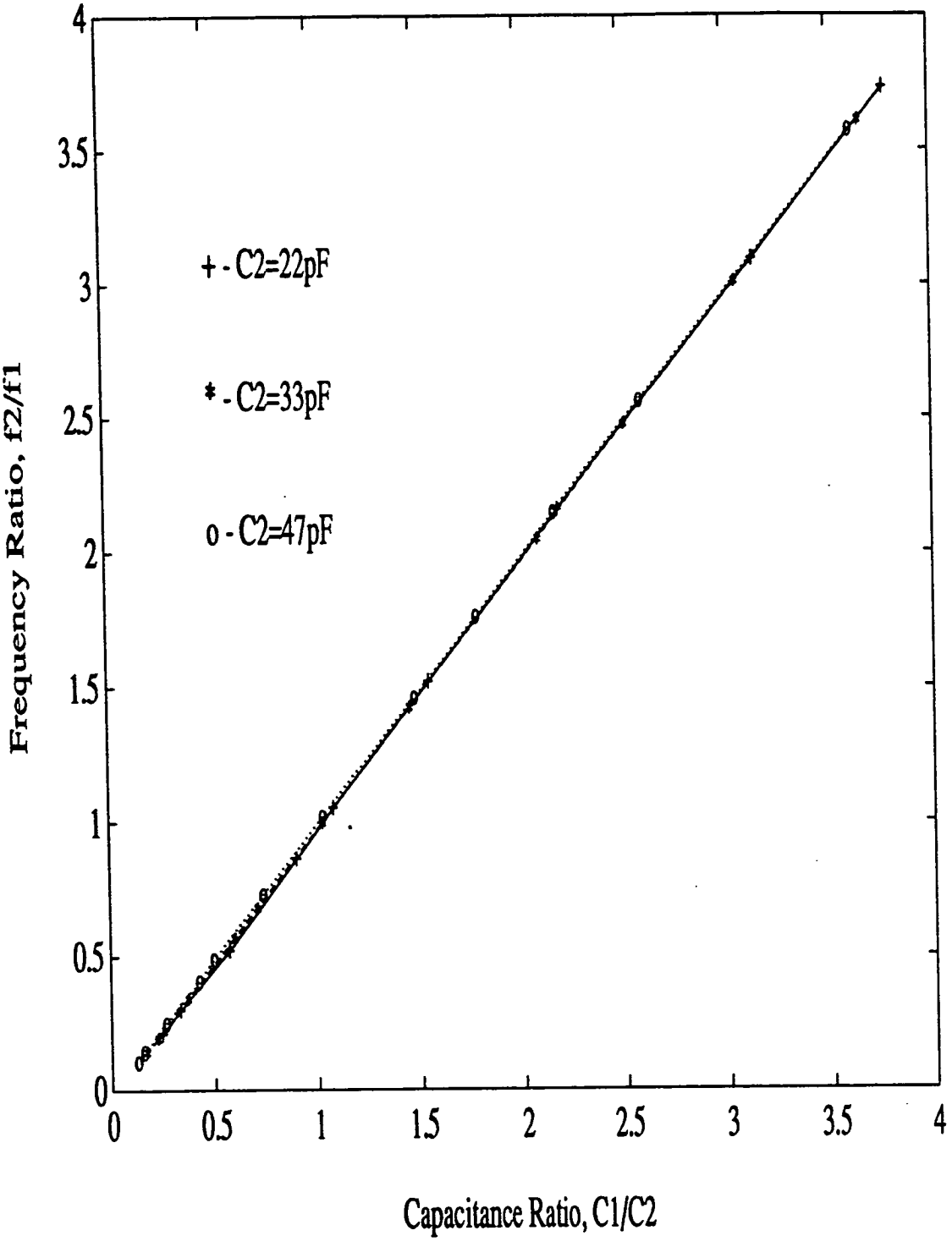


Figure 45: Frequency ratio against sensor capacitance ratio for the frequency control loop at three different values of C_2

range and jitter, which operates principally via C_I and the VCO gain factor k, as described more fully in §4.5.3, *p* 125. The noise characteristics also require exploring, as detailed in §3.6, *p* 84. Finally, the power consumption of frequency control loop No.1 was measured as 8.9mW, a figure that is slightly lower than that of the discrete version and within the maximum of 22.5mW for fieldbus operation.

5.6 Chapter Summary

Capacitance sensor interface circuits have been implemented as a prototype ASIC. The ASIC was produced using the ES2 Solo 1200 standard-cell process and contains a SC capacitance-to-voltage converter, a voltage control loop, two versions of the frequency control loop and a node communications circuit. Each of the four interface circuits has a silicon area requirement of no more than 1.3 mm^2. The integrated approach facilitated the employment of measures to reduce charge-feedthrough and jitter, which were found to be the two major sources of error in the discrete versions of the interface circuits, whilst remaining in accordance with the wider research aims of production of low power, minimum area and low cost circuitry. The first of these measures was the inclusion of charge-feedthrough compensating dummy switches. The non-availability of compensated switches in the ES2 analogue cell library necessitated the full-custom design of compensated switches and the modification of the standard-cell design procedure to permit the inclusion of these full-custom elements. The second of these measures was the use of guard rings and the partitioning of the analogue and digital portions of the interface circuits, an inherent feature of the Solo 1200 process, to further improve upon the stable parasitic environment afforded by the integrated circuit approach.

The test of frequency control loop No.1 confirmed that the jitter was considerably reduced and that there was no evidence of locking of the output frequency to the

reference frequency. Measurements on single uncompensated and compensated switches confirmed that the smaller feature size of the integrated switches reduced the charge-feedthrough compared with that of the discrete switches. The dummy switch compensation technique was also demonstrated to effect a reduction in the charge-feedthrough magnitude. Furthermore, for future design of optimally sized switches HSPICE was shown to predict charge-feedthrough behaviour accurately and minimum sized switches were discovered not to impair the settling time requirement on the sensor capacitance.

Measurements on the compensated and uncompensated SC capacitance-to-voltage converters both demonstrated a reduction in charge-feedthrough over that of the discrete version. However, dummy switch compensation had a variable effect on the net charge-feedthrough magnitude of the integrated converter circuits. In some instances the reduction in magnitude corresponded with that of the single switch; in others the magnitude was increased. Further work is required to investigate the effects of IC layout and processing spreads on the effectiveness of the dummy switch charge-feedthrough compensation technique.

Measurements on frequency control loop No.1 revealed a significant improvement in steady-state performance over that of the discrete circuit. The resolution of the conversion of capacitance ratio to frequency ratio was approximately 2%, and at the limit of measurement precision using the present experimental apparatus.

In conclusion, better than 10-bit resolution within the 20mS measurement period is potentially attainable when the charge-feedthrough magnitudes of the single 6/2 aspect ratio switch are considered. A significantly greater resolution might be attainable if the switch aspect ratio dependent compromise between charge-feedthrough and

settling time on the sensor capacitance is investigated more thoroughly. Should a large aspect ratio switch, i.e. >> 6/2, be required for, say 14-bit resolution then the effect of IC layout and processing spreads upon the efficiency of dummy switch charge-feedthrough compensation would require investigation.

Chapter 6
Summary and Conclusions

6.1 Summary

This thesis describes an investigation of interface circuits for capacitance sensors, in particular capacitance ratio sensors, suitable for integration on silicon using the ES2 standard-cell ASIC CMOS process. Interface circuits based upon the switched-capacitor integrator were selected for special investigation because of their performance when implemented using analogue components of limited performance such as are usually provided in analogue standard-cell libraries.

Simple, first-order mathematical models were derived to describe their steady-state behaviour. The principle of operation of the three interface circuits is as follows. Firstly, the switched-capacitor integrator converts absolute capacitance to a voltage level. Secondly, the frequency control loop comprising two, four switch blocks, an integrating operational amplifier and a VCO, converts capacitance ratio to a frequency ratio. Of the three interface circuits this circuit was the subject of the most thorough investigations. Lastly, the voltage control loop consisting of two, four switch blocks and an integrating operational amplifier, converts capacitance ratio to a voltage ratio. This third circuit was not tested experimentally although a first-order model was presented and an integrated implementation included in the prototype ASIC.

Prior to the design of the integrated versions of the three interface circuits the validity of a first-order analysis of their performance was examined by means of discrete, bread-boarded circuits. An extensive programme of experiments revealed a significant departure from first-order theory, particularly at low values of sensor capacitance. Charge-feedthrough contributed by the switches was identified as the primary

source of error and the first-order theory was extended to include this error mechanism. The frequency control loop second-order model thus developed was demonstrated to predict circuit performance with good accuracy. A dummy switch charge-feedthrough compensation technique was selected for incorporation in the integrated interface circuits to reduce this source of error. Jitter and locking behaviour within the frequency control loop was encountered as a secondary source of inaccuracy. Characterisation of this phenomenon was, however, not possible as a result of the variable parasitic nature of the discrete circuit. Further investigations of the frequency control loop included a measurement of power consumption and some initial exploration of the transient behaviour.

Having identified the main sources of error and extended the first-order model a prototype ASIC containing the interface circuits was produced. The design was accomplished using the ES2 Solo 1200 standard-cell process. The prototype ASIC contains a capacitance-to-voltage converter, a voltage control loop, two versions of the frequency control loop and a node communications circuit. This last circuit would facilitate the construction of a bus system comprising interlinked sensor nodes. A full-custom approach was employed in the design of the switches to circumvent the non-availability of suitable, compensated switches in the process cell library. Dummy switch compensated and un-compensated switches were included to assess the effect on charge-feedthrough in the first instance of the reduced switch size afforded by an integrated approach, and secondly to measure the improvement effected by the compensation technique. Furthermore, two sizes of switches were included for high frequency operation but large charge-feedthrough on the one hand, and limited frequency operation but reduced charge-feedthrough on the other. A further expected benefit of integration is the associated stable parasitic environment which would allow the jitter and locking behaviour to be examined and remedial schemes to be tested.

The test of the prototype ASIC demonstrated the jitter to be significantly reduced and no evidence of locking was observed in the SC frequency control loop. The

steady-state performance of both the SC capacitance-to-voltage converter and the SC frequency control loop was demonstrated to be considerably improved, principally as a result of the smaller feature size of the full-custom switches reducing charge-feedthrough. The dummy switch charge-feedthrough compensation scheme was observed to reduce the net feedthrough charge in a single switch arrangement. Of importance for any future development of the circuits the measured charge-feedthrough magnitudes were in agreement with those predicted by both hand-calculation and HSPICE computer simulation. However, the dummy switch compensation of the SC capacitance-to-voltage converter was less successful: in some instances there was a reduction in the net feedthrough charge that was in accordance with that obtained for the single switch arrangement; in others the technique increased the net feedthrough charge. Initial investigations have indicated that IC layout variations, and to a lesser extent IC process variations are responsible for the variable behaviour. Finally the power consumption and transient response of the frequency control loop were measured and confirmed to be in agreement with measurements of the discrete version of the circuit.

6.2 Conclusions

Analogue-to-digital converters and interface circuits that utilise switched-capacitor techniques were acknowledged in many of the publications reviewed in *Chapter* 2 as being eminently suited for application as capacitance sensor interface circuits. Moreover, switched-capacitor circuits, where the switched-capacitors are external sensor capacitances, can be implemented using a standard CMOS process, an important factor in the realisation of a single multi-function ASIC comprising sensor interface circuits, digital signal processing and communications circuitry. The review of analogue-to-digital converters and interface circuits based on switched-capacitor techniques

established that such circuits are capable of high resolution and low power performance with minimum silicon area requirements, although there were few instances of high performance being maintained at low values of sensor capacitance.

The selection of an ASIC design method commensurate with the resources of this project was of crucial importance. The lengthy full-custom approach was explored initially but abandoned owing to problems of meeting the required objectives within the project lifetime. The standard-cell method, in contrast, provided the means to the successful fabrication of a prototype ASIC containing four interface circuits and node communications circuitry. The choice of this latter approach with its restrictive library of analogue components of moderate performance capability presented a significant challenge to the development of high precision capacitance interface circuits resulting in the investigation of the three interface circuits presented in *Chapter* 3. This specific bias is in fact a novel feature of the investigations reported in this thesis. The first interface circuit, the capacitance-to-voltage converter, which is similar to the familiar switched-capacitor integrator, is a sub-circuit of the other two circuits, the frequency control loop and the voltage control loop. The frequency control loop was proposed as a capacitance ratio to frequency ratio converter independently of a similar but earlier circuit proposed by Viswanathan *et al.* [72]. The voltage control loop is a novel capacitance ratio to voltage ratio converter.

As a result of extensive characterisation of discrete implementations of the interface circuits, which revealed charge-feedthrough to be the primary cause of steady-state errors, a second-order analytical model was proposed for the frequency control loop that incorporated this error mechanism. This model was demonstrated to predict the performance of the discrete frequency control loop with good accuracy. Jitter in the output frequency of the frequency control loop and locking of the output frequency to the reference frequency were also serious impediments to achieving high resolution.

The integrated circuit approach, in addition to providing the means to produce low power, compact and low cost interface circuits facilitated the reduction of the effects of charge-feedthrough and jitter. In the first instance integration permitted the inclusion of the required, charge-feedthrough compensating dummy switches. In the second, the stable parasitic environment of the ASIC was expected to allow the characterisation and reduction of the jitter phenomenon with two suggested remedial schemes. The incorporation of dummy switches was, however, achieved using a full-custom method and a modification to the standard-cell process on account of the non-availability of suitable switches in the ES2 library.

The test of the prototype ASIC demonstrated that the SC capacitance-to-voltage converter and the SC frequency control loop both had improved performance over that of the discrete versions. The reduction in the feature size of the switches and the associated reduction in charge-feedthrough was responsible for the improvement in the steady-state performance, with the integrated frequency control loop capable of accurately converting a sensor capacitance ratio to a frequency ratio. The conversion accuracy was maintained over a large capacitance ratio variation. It should be noted that available test equipment did not allow the 0.1% performance of the circuit to be investigated.

The resolution could be further improved by the reduction of the switch aspect ratio from 500/2, which was discovered to have a smaller than necessary on-resistance for sensor capacitance settling time requirements. Switches with an aspect ratio of 6/2, such as are incorporated in frequency control loop No.2 of the prototype ASIC, were estimated to increase the resolution of the frequency control loop to 11-bits within the required 20mS measurement time. However, confirmation of this estimated resolution would require new and more accurate measurement techniques and apparatus: this remains as part of future work. Importantly for future development and analysis of the interface circuits, charge-feedthrough measurements made on integrated single switch arrangements were in close agreement with both hand-calculations and HSPICE

computer simulations. Thus it is with confidence that a reduction in charge-feedthrough of two orders of magnitude can be expected of frequency control loop No.2 with a corresponding improvement in resolution.

Measurements on the compensated single switch arrangement demonstrated a reduction in charge-feedthrough in accordance with that predicted by HSPICE computer simulations. Having established the predictive accuracy of HSPICE, more effective scaling of dummy switches is possible to improve the charge-feedthrough compensation. However, despite the effectiveness of this technique with a single switch, measurements of several SC capacitance-to-voltage converters revealed an increase in the net charge-feedthrough in some instances and a reduction in others. Preliminary investigations indicated that IC layout, and to a lesser extent IC process variations, were responsible for the general failure of dummy switch compensation. Further work is required to verify the cause of the variation and to assess if a more controlled layout of the switch blocks could make compensation viable.

A resolution greater than the 11-bits predicted for frequency control loop No.2 could be attained by increasing the switch aspect ratio to satisfy settling time requirements on the sensor capacitance at the cost of increased charge-feedthrough. This compromise between settling time and charge-feedthrough requires further investigation. Should the increase in charge-feedthrough be such that it compromises accuracy a reduction could be achieved by dummy switch compensation, subject to the resolution of the present shortcomings of this technique.

Jitter, which was the second significant source of error in the discrete implementation of the frequency control loop, was much reduced. Of importance was the absence of any locking of the output frequency to the reference frequency.

To assess the extent to which the project objectives, stated in §1.5, *p* 17, have been met, each aspect of performance will be summarised in turn drawing upon the results obtained from the discrete and integrated circuits.

The measured power consumption of integrated frequency control loop No.1 was 8.9mW, a figure that is comfortably within the specified 22.5mW.

The data-acquisition time of 20mS to 100mS was also, in the broadest of terms, achievable. However, acquisition time must be considered in conjunction with resolution, a conflicting aim that will be subject of future testing of the prototype ASIC when improved measurement apparatus is used. Furthermore, the transient response and the dynamic range are additional interdependent factors that require further investigation.

Performance over the industrial temperature range was not investigated experimentally and should form part of any future testing of the prototype ASIC.

The precision of integrated frequency control loop No.1 was maintained over a capacitance ratio range of greater than 20 to 1. Estimates based upon measurements of single integrated switches and hand-calculations predict that frequency control loop No.2 is capable of converting a capacitance ratio to a frequency ratio with 11-bit precision within 20mS.

The final objective, that of a low cost, standard-cell ASIC implementation with a minimum of external components has been realised, with each of the three interface circuits requiring no more than $1.3mm^2$. The external component count is low with each of the three interface circuits requiring a smoothing capacitor, and the frequency control loop a capacitor and resistor to set the VCO gain.

The performance of the integrated frequency control loop is summarised in *Table* 5 below. The performance objectives are as presented in *Table* $1, p\,55$.

Performance Comparison		
Parameter	Objective	Achieved
Conversion time	20mS-100mS	20mS (estimated)
Power consumption	<22.5mW	8.9mW
Resolution	10+ bits	11+ bits (estimated)
Capacitance size	20pF	5pF to 120pF
Silicon area	$<2mm^2$	$1.3mm^2$ maximum

Table 5

6.3 Recommendations for Future Work

The following seven areas of investigation constitute the recommendations for future work. The eighth and final recommendation is considered to be a longer term option of secondary importance.

- High resolution measurement of integrated frequency control loops Nos.1 and 2 using improved measurement apparatus.

- Investigation of the compromise between settling time on the sensor capacitance and charge-feedthrough.

- Investigation of the effect of IC layout and processing spreads on the effectiveness of dummy switch charge-feedthrough compensation.

- A fuller investigation of the transient response and dynamic range of the frequency control loop, and the interdependence between precision and data-acquisition time.

- Test and characterisation of the integrated voltage control loop

- Characterisation of the interface circuits over the industrial temperature range.

- Noise analysis and measurement

- Construction of a bus system comprising interlinked prototype ASICs, where each ASIC is interfaced with one or more capacitive sensor.

The results of the research presented in this thesis indicate that the integrated interface circuits provide a solution to some of the present problems within industrial process control instrumentation. Potentially, the techniques presented here are capable of achieving a precision of better than 0.1%, as required by some process applications.

It is hoped that the work presented in this thesis will have made some contribution to this challenging field.

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Appendix A: ES2 Analogue Library Component Data

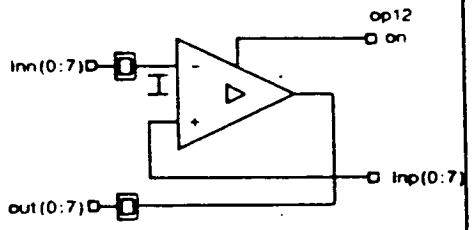
A.1 OP-22 the High Drive Operational Amplifier

Analoglib V 1.4 March 1988

Op Amp 22 op22

Input: inp(0:7) *
inn(0:7) *
on

Output: out(0:7) *



Size: Width= 800 µm
Height= 581.5 µm

* analogue signal

General Description
High drive operational amplifier.
Internally compensated for Cload<200pF.
Standby mode with input ON at low level.
Output high Z during standby mode.

Fan in

Pin	Load
ON	1

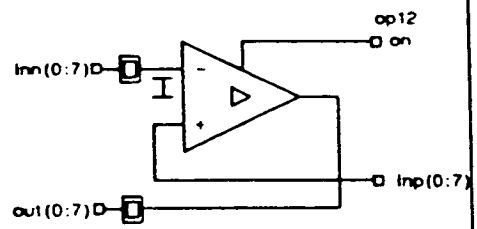
Cload=200pF Rload=1MOhm	Min	Typ	Max	Unit
Input offset voltage	-5		+5	mV
Offset voltage drift		+0.2		uV/K
Open loop gain	85	92		dB
Unity gain bandwidth	1.4	2.8	6	MHz
Phase margin	70	80		degree
Common mode input range	0.5		VDD-0.9	V
Output range Rload=10kOhm	0.1		VDD-0.2	V
CMRR dc/1kHz		99		dB
PSRR+ dc/1kHz		84		dB
PSRR- dc/1kHz		72		dB
Output source current	23	39	72	mA
Output sink current	59	125	234	mA
Settling time 1V step 1% (rise/fall)	.25/.32	.6/0.7	1.4/2	u s
Input referred noise 10Hz		470		nV/(Hz)^1/2
Input referred noise 1kHz		50		nV/(Hz)^1/2
Input referred noise 100kHz		16		nV/(Hz)^1/2
DC power dissipation	6.8	18	48	mW
Standby power dissipation			5	uW
Start up time		1.45	2.6	u s
Slew rate rise/fall	.7/0.75	1.7/1.9	4/4.5	V/u s
Output resistance		2.3	5	kOhm
Input capacitance Cinp		2.8		pF
Input capacitance Con		100		fF
Input capacitance Cinn		2.8 +Cpackage		pF

Analoglib V 1.4
March 1988

Op Amp 32 op32

Input: inp(0:7) *
inn(0:7) *
on

Output: out(0:7) *



Size: Width= 505 µm
Height= 581.5 µm

* analogue signal

General Description
Low power operational amplifier.
Low output impedance.
Standby mode with input ON at low level.
Output high Z during standby mode.

Fan in

Pin	Load
ON	1

Cload=200pF Rload=1MOhm	Min	Typ	Max	Unit
Input offset voltage	-5		+5	mV
Offset voltage drift		+0.5		uV/K
Open loop gain	85	91		dB
Unity gain bandwidth	150	310	620	kHz
Phase margin	65	70		degree
Common mode input range	0.5		VDD-0.9	V
Output range Rload=10kOhm	1.1		VDD-1.5	V
CMRR dc/1kHz		97		dB
PSRR+ dc/1kHz		70		dB
PSRR- dc/1kHz		70		dB
Output source current	1.2	3.4	8	mA
Output sink current	1.6	3.6	8.3	mA
Settling time 1V step 1% (rise/fall)	1.3/2.7	3.2/3	7.8/9.5	u s
Input referred noise 10Hz		4600		$nV/(Hz)^{1/2}$
Input referred noise 1kHz		470		$nV/(Hz)^{1/2}$
Input referred noise 100kHz		100		$nV/(Hz)^{1/2}$
DC power dissipation	0.09	0.24	0.66	mW
Standby power dissipation			5	uW
Start up time	3.5	6.5	21	u s
Slew rate rise/fall	.12/.18	.34/.45	1/.94	V/u s
Output resistance		1.1	2.3	kOhm
Input capacitance Cinp		2.8		pF
Input capacitance Con		100		fF
Input capacitance Cinn		2.8 +Cpackage		pF

A.3 VCO1 the Voltage Controlled Oscillator

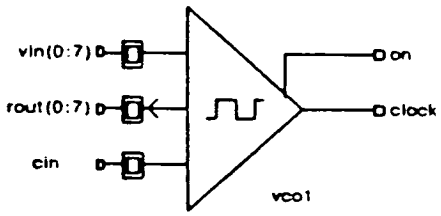
Analoglib V 1.4

March 1988

Voltage Controlled Oscillator vco1

Input: vin(0:7) *
cin
on

Output: clock
rout(0:7) *



Size: Width= 655 µm
Height= 581.5 µm

* analogue signal

General Description

Frequency range 10Hz to 1MHz.
Standby mode with input ON at low level.
Output CLOCK low during standby mode
Frequency= VIN/(0.8*VDD*Rout*Cin)

Fan in

Pin	Load
ON	1

Drive Strength

Pin	Strength
CLOCK	2

Duty cycle (mark/space ratio) 50%

Parameter	Min	Typ	Max	Unit
Supply voltage VDD	4.5		5.5	V
Offset voltage at VIN	-5		5	mV
External resistance value Rout	30		1000	kOhm
VIN range	0		VDD-2	V
Input capacitance Cin		100		fF

VDD=5V Vin=3V Rout=30kOhm Cin=250pF	Min	Typ	Max	Unit
Frequency	94.7	98	102	kHz
Frequency drift with temperature		260	1000	ppm/K
Frequency drift with supply (VIN=0.6*VDD)		1.6	2.5	%/V
Linearity error (0V<VIN<3V)		1.1	2	%
Frequency jitter		22		Hz
Power dissipation		2.2	3.6	mW

VDD=5V Vin=3V Rout=30kOhm Cin=20pF	Min	Typ	Max	Unit
Frequency	816	980	1080	kHz
Frequency drift with temperature		500	1000	ppm/K
Frequency drift with supply (VIN=0.6*VDD)		6.7	10	%/V
Linearity error (0V<VIN<3V)		0.6	4.5	%
Power dissipation			3.7	mW

Appendix B: The EMF Test IC

The circuits and devices integrated on the EMF IC are of three types: firstly, test-structures to permit the extraction of certain circuit and SPICE parameters; secondly, basic analogue circuits to obtain data on circuit performance and compromises; and finally, two complete comparators and an operational amplifier that incorporate some of the basic circuits. Each circuit is connected to a standard eight pad frame for automatic probing, using parametric test equipment such as the HP 4061 series.

Summary of Test-Structures and Circuits

Test-structures:

- A graduated array of poly-oxide capacitor ratios.
- An array of transistors with different channel lengths and geometries to permit the extraction of SPICE parameters.
- Arrays of matched transistors with varying geometries to permit the measurement of drain current matching.

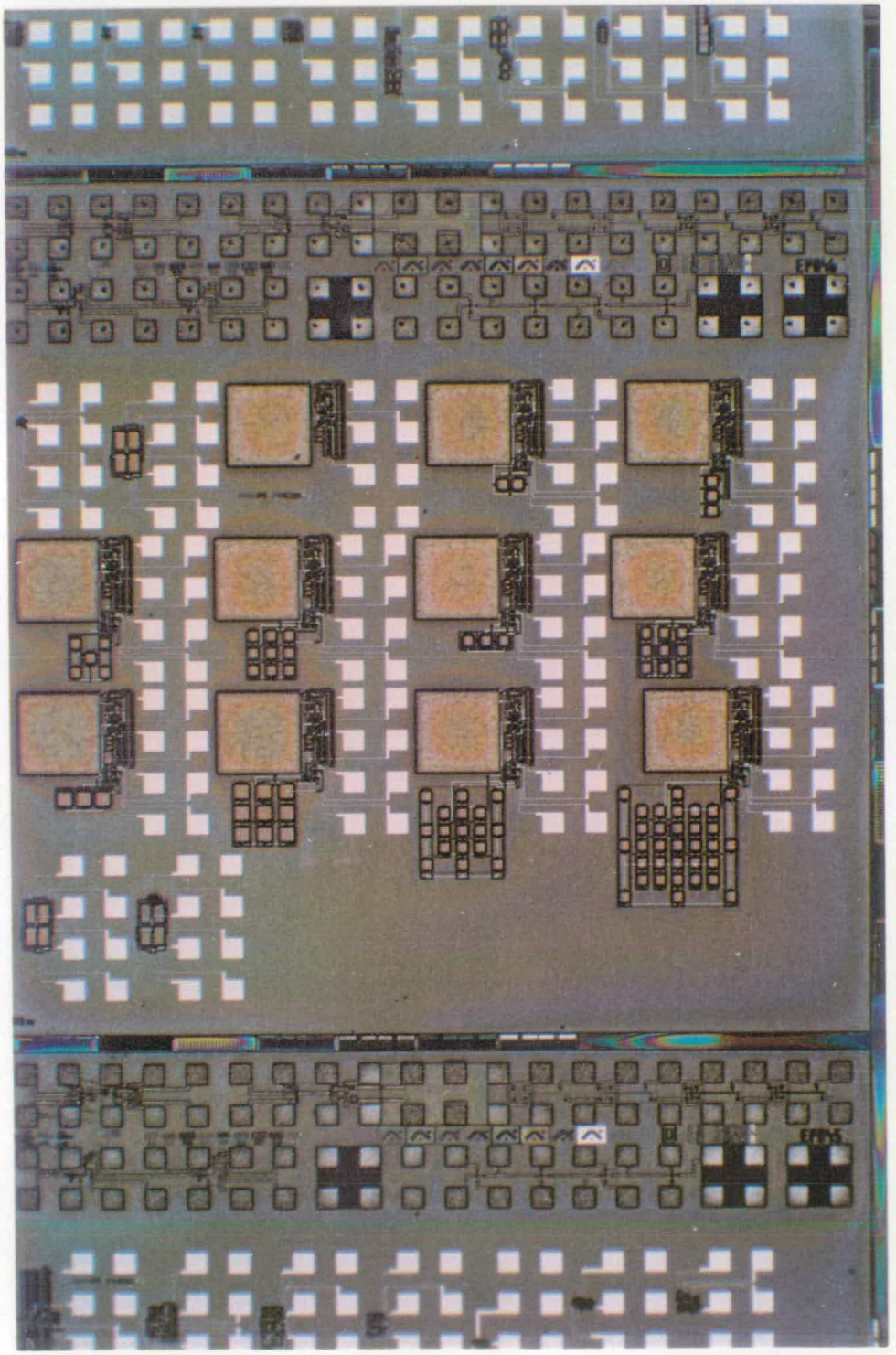
Basic circuits:

- Basic, cascode and wilson current mirrors.
- Differential pairs.
- Analogue switches
- Current sources.

Circuits:

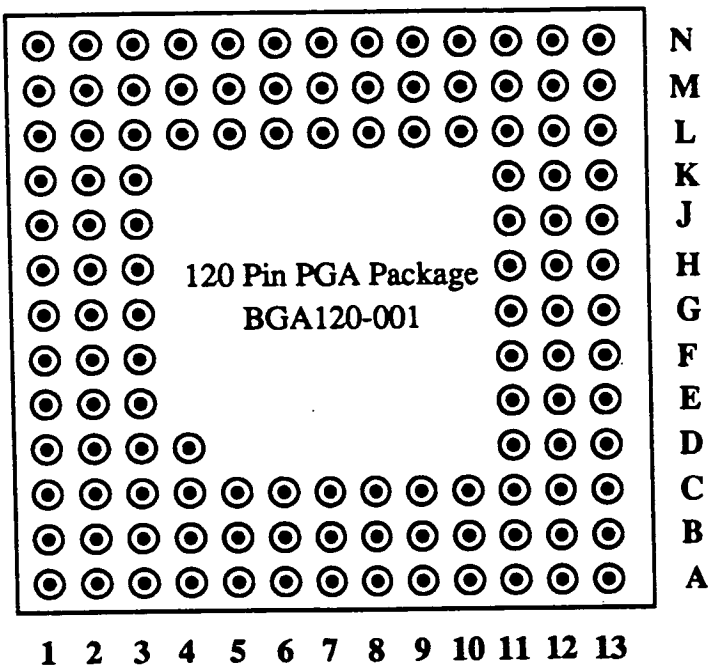
- An operational amplifier configured as a unity-gain buffer.
- Two low power comparators.

Microphotograph of EMF Test IC



Appendix C: The ES2 Prototype IC

Pinout Details of the Prototype IC



Power and Ground Pins:

Pin No.	Function
E1	Vsspadn - digital ground
J3	Vddpad - digital power
L4	Vsspadn - digital ground
M13	AVddcw - analogue power
B13	AGndac - analogue ground
B11	Vddpad - digital power
A9	Vsspadn - digital ground
A6	Vddpad - digital power
A3	Vsspadn - digital ground

Circuit Select Lines:

Pin No.	Function
K1	sel1 - frequency control loop No.1
K2	sel3 - voltage control loop
L1	sel2 - frequency control loop No.1
M1	sel1 - capacitance-to-voltage converter

Capacitance - to - Voltage Converter

Pin No.	Name	Function
G2	iph11	clock input
G3	iph21	clock input
G1	iph12	clock input
H1	iph11	clock input
M6	icin	sensor capacitance
N6	icout	sensor capacitance
L13	iearth(0:7)	non-inv i/p of opamp
K13	ioearth(0:7)	switch block earth
H11	ivout(0:7)	opamp output
H12	ifb(0:7)	inv i/p of opamp
L5	ivin	reference voltage

Voltage Control Loop

Pin No.	Name	Function
N5	vv1in	reference voltage No.1
E2	v2ph21	clock i/p to switch block No.2
F3	v2ph12	clock i/p to switch block No.2
F2	v2ph22	clock i/p to switch block No.2
F1	v2ph11	clock i/p to switch block No.2
H2	v1ph11	clock i/p to switch block No.1
H3	v1ph21	clock i/p to switch block No.1
J1	v1ph22	clock i/p to switch block No.1
J2	v1ph12	clock i/p to switch block No.1
M8	v1cout	sensor capacitor No.1
L8	v2cout	sensor capacitor No.2
N9	v1cin	sensor capacitor No.1
M9	v2cin	sensor capacitor No.2
K11	vearth(0:7)	non-inv i/p of opamp
J11	voearth(0:7)	earth on switch blocks No.1 & No.2
F12	vvout(0:7)	opamp output
F11	vfb(0:7)	inv i/p of opamp
C13	vvin(0:7)	reference voltage No.2

Frequency Control Loop No.1

Pin No.	Name	Function
M5	f1vin	reference voltage No.1
L6	f2vin	reference voltage No.2
D1	ffout	VCO o/p
M3	f1ph21	clock i/p to switch block No.1
N3	f1ph11	clock i/p to switch block No.1
C10	f1ph22	clock i/p to switch block No.1
A12	f1ph12	clock i/p to switch block No.1
B1	f2ph11	clock i/p to switch block No.2
C1	f2ph22	clock i/p to switch block No.2
D2	f2ph12	clock i/p to switch block No.2
E3	f2ph21	clock i/p to switch block No.2
N10	f1cout	sensor capacitance No.1
L9	f2cout	sensor capacitance No.2
M10	f1cin	sensor capacitance No.1
N11	f2cin	sensor capacitance No.2
K12	foearth(0:7)	earth of switch blocks No.1 & 2
J13	fearth(0:7)	non-inv. i/p of opamp
E13	fcin	Cext of VCO
E12	frout(0:7)	Rext of VCO
D13	fvcoin(0:7)	voltage i/p to VCO
E11	fvout(0:7)	o/p of opamp
D12	ffb(0:7)	inv. i/p of opamp

Frequency Control Loop No.2

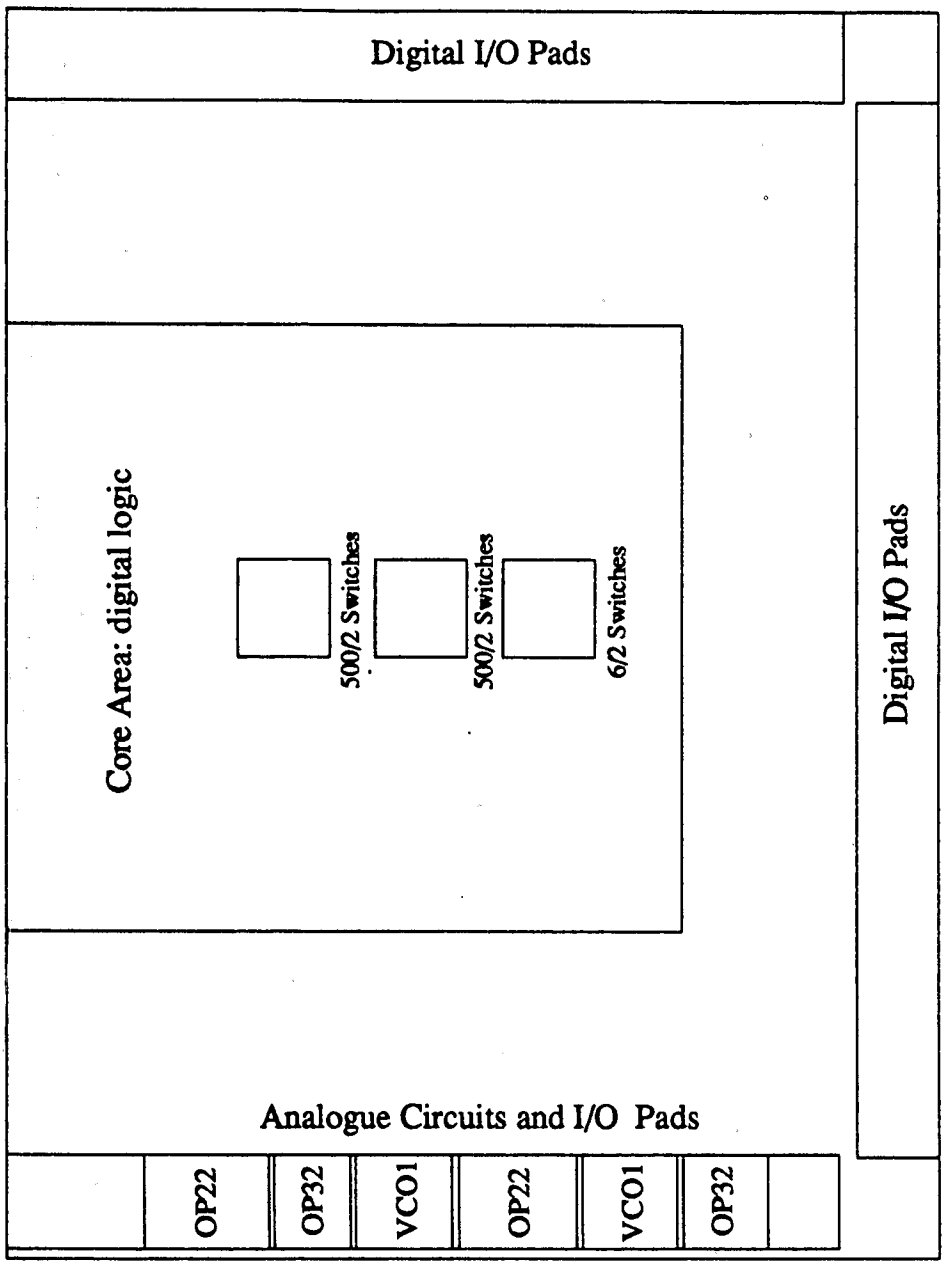
Pin No.	Name	Function
N4	cfv1in	reference voltage No.1
D3	cffreq	reference frequency
C2	cffop	VCO o/p
M7	cfc1in	sensor capacitance No.1
L7	cfc2in	sensor capacitance No.2
N7	cfc2out	sensor capacitance No.2
N8	cfc1out	sensor capacitance No.1
L12	ffearth(0:7)	non-inv. i/p of opamp
J12	ffoearth(0:7)	earth of switch blocks No.1 & 2
H13	cfvout(0:7)	o/p of opamp
G12	cffb(0:7)	inv. i/p of opamp
G11	cfcin	Cext of VCO
G13	cfrout(0:7)	Rext of VCO
F13	cfvcoin(0:7)	voltage i/p to VCO
M4	cfv2in	reference voltage No.2

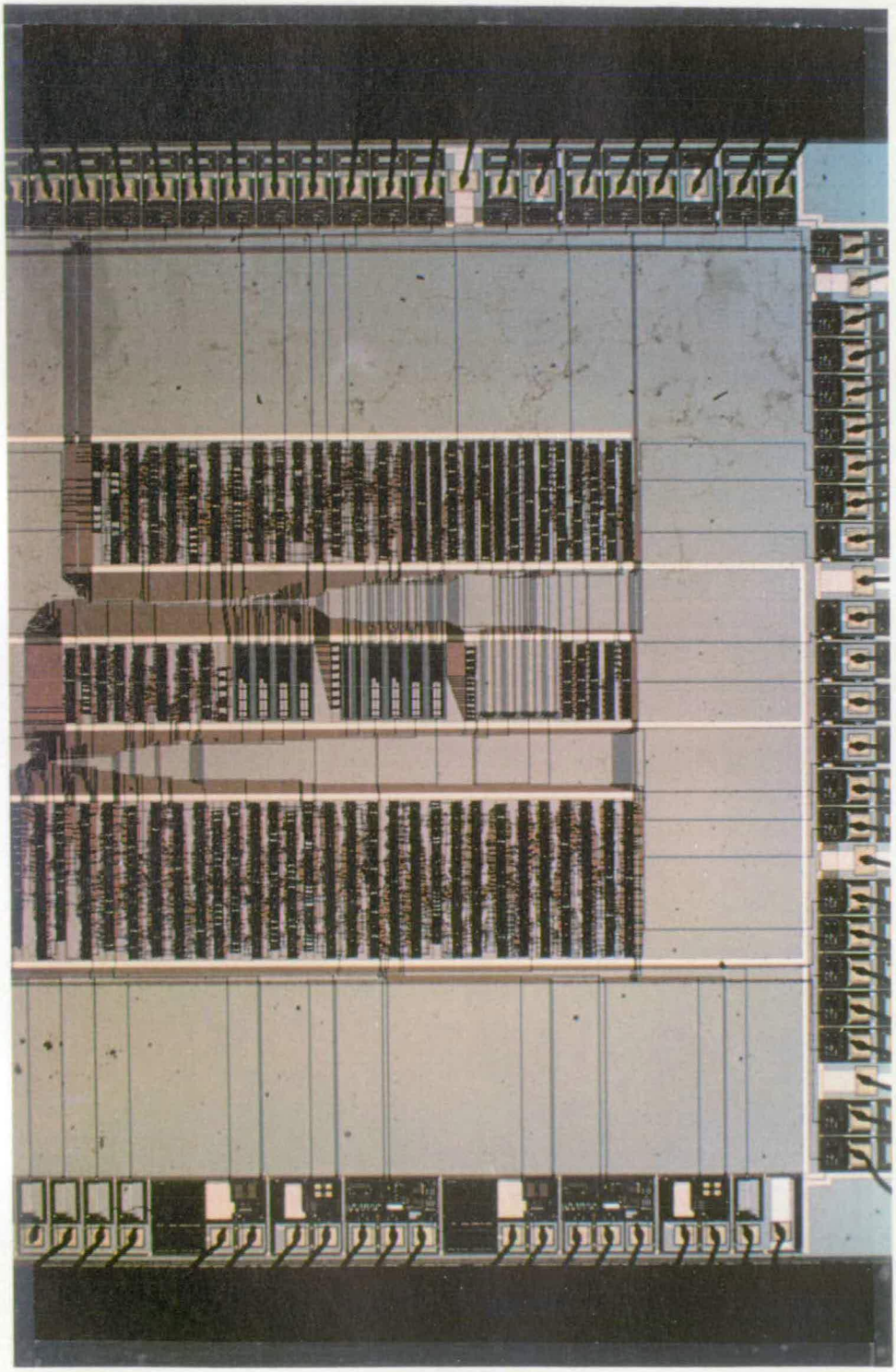
Node Communications Circuit

Pin No.	Name	Function
A11	atrig	triggers packet transmission
B10	asel	select frequency data transmission
C9	afrequ	frequency transducer i/p
A10	aread	assert to access stored data
B9	ana1	node address pin
C8	ana2	node address pin
B8	ana3	node address pin
A8	aac1	analogue control bit
B7	aac2	analogue control bit
C7	adtaout	data o/p
A7	ama	address match flag
B6	aout1	optically driving o/p
C6	amr	master reset
A5	amhz	master clock
B5	ainput1	optically driven i/p
A4	aload	assert to load data
C5	amdata	data i/p
B4	aclockm	toggle i/p for data i/p and o/p
A2	ascanm	assertion inhibits data regeneration

Microphotograph of ES2 Prototype IC:

identifying major features and components





Node Communications Circuit

The node communications circuit described here is a modification of a circuit originally designed by Sylvan [24]. The circuit is intended to control data communications among optical bus nodes and requires a microprocessor to utilise its full capabilities. However, a microprocessor is not required when the circuit is operated in conjunction with frequency output sensors, such as the frequency control loop, on account of the provision of a frequency counter and the availability of a 2-bit data field, read from an incoming data packet, that is assigned to data control purposes. The communications circuit operates in one of four modes, as follows. As a regenerator, to receive and retransmit a data packet to the next node. As a receiver, to receive and read out all the data fields within the packet for use at the node. As a transmitter, to load data fields into a packet and trigger transmission. Finally, as a storage controller, to receive and store a data packet prior to re-transmission following a trigger from the node.

Circuit features:

- 8 node address space within packet
- 24-bit data field within packet
- Single error correction and double error detection of received packets
- On-board counter for frequency output sensors
- 2-bits automatically available upon packet receipt for analogue control
- Low transmitter power by use of on-off keying

Appendix D

D.1 HSPICE Input File for Rise Time Simulation

```
RISE TIME TEST ON SERIES RESISTANCE AND TWO NMOS SWITCHES
* 500 x 2 MICRON SWITCHES: RISE TIME TEST ON 50pF LOAD
* POWER SUPPLIES
VSS 0 2 DC -2.5
VS 1 0 DC 1.5
VCLOCK- 5 0 PULSE(-2.5 2.5 0 5N 5N 1U 1.01U)
* CIRCUIT TOPOLOGY
M1 4 5 3 2 N L=2U W=500U AD=2.5N AS=2.5N PD=1.01M PS=1.01M
M2 6 5 0 2 N L=2U W=500U AD=2.5N AS=2.5N PD=1.01M PS=1.01M
* PASSIVE COMPONENTS
CL 4 6 50P
RS 1 3 200
* ES2 MODELS
*** nmos nominal parameters ** ECDM20 process **
.options tnom=25
.MODEL N NMOS LEVEL=2
+ VTO=0.9 TOX=40E-9 NSUB=.53E16 LD=0.15U
+ UO=510 UEXP=1.29e-2 UCRIT=1E3 VMAX=3.79E4
+ UTRA=0 XJ=.5E-6 NEFF=2.74 NFS=0
+ RSH=40 JS=1E-4 CGDO=150P CGSO=150P
+ CJ=110E-6 CJSW=250E-12 MJ=0.48 MJSW=0.27 PB=0.45
*** pmos nominal parameters ** ECDM20 process **
.MODEL P PMOS LEVEL=2
+ VTO=-0.6 TOX=40E-9 NSUB=1.9E16 LD=0.2U
+ UO=175 UEXP=3.11E-2 UCRIT=4.72E3 VMAX=3.72E4
+ UTRA=0 XJ=6E-7 NEFF=1 NFS=0
+ RSH=50 JS=1.E-4 CGDO=210P CGSO=210P
+ CJ=350E-6 CJSW=450E-12 MJ=0.48 MJSW=0.4 PB=0.45
* SIMULATION
.IC V(4)=-2.5
.TRAN 5N 1U UIC
.PRINT TRAN V(1) V(5) V(4) V(3)
.END
```

D.2 HSPICE Input File for Transfer Function Simulation

```
TRANSFER FUNCTION OF SINGLE NMOS SWITCH
* 500 x 2 MICRON SWITCH: TRANSFER FUNCTION TEST
* POWER SUPPLIES
VDD 1 0 DC 2.5
VSS  0 2 DC -2.5
VS   3 0 DC 0.5
* CIRCUIT TOPOLOGY
M1 5 1 4 2 N L=2U W=500U AD=2.5N AS=2.5N PD=1.01M PS=1.01M
* PASSIVE COMPONENTS
CL 5 0 50P
RS 3 4 200
* ES2 MODELS
***   nmos nominal parameters    ** ECDM20 process **
.options tnom=25
.MODEL  N       NMOS        LEVEL=2
+       VTO=0.9       TOX=40E-9      NSUB=.53E16 LD=0.15U
+       UO=510        UEXP=1.29e-2   UCRIT=1E3   VMAX=3.79E4
+       UTRA=1.64     XJ=.5E-6       NEFF=2.74    NFS=0
+       RSH=40        JS=1.E-4       CGDO=150P    CGSO=150P
+       CJ=110E-6     CJSW=250E-12   MJ=0.48      MJSW=0.27    PB=0.45
***   pmos nominal parameters    ** ECDM20 process **
.MODEL  P       PMOS        LEVEL=2
+       VTO=-0.6      TOX=40E-9      NSUB=1.9E16  LD=0.2U
+       UO=175        UEXP=3.11E-2   UCRIT=4.72E3 VMAX=3.72E4
+       UTRA=0.817    XJ=6E-7        NEFF=1       NFS=0
+       RSH=50        JS=1.E-4       CGDO=210P    CGSO=210P
+       CJ=350E-6     CJSW=450E-12   MJ=0.48      MJSW=0.4
+       PB=0.45
* SIMULATION
.DC VIN 2 5 0.1
.PRINT DC V(3) V(5)
.END
```

D.3 HSPICE Input File for Charge-Feedthrough Simulation

```
CHARGE-FEEDTHROUGH MEASUREMENT
* CHARGE-FEEDTHROUGH TEST ON ONE COMPENSATED,
* 500/2 NMOS SWITCH
* POWER SUPPLIES
VSS 0 2 DC -2.5
VIN 1 0 DC 0
VCLK1+ 6 0 PULSE(2.5 -2.5 20N 0.5N 0.5N 200N 200N)
VCLK1- 7 0 PULSE(-2.5 2.5 21N 0.5N 0.5N 200N 200N)
* CIRCUIT TOPOLOGY
M1 5 6 4 2 N L=2U W=500U AD=2.5N AS=2.5N PD=1.01M PS=1.01M
M2 5 7 5 2 N L=2U W=500U AD=2.5N AS=2.5N PD=1.01M PS=1.01M
* PASSIVE COMPONENTS
CL 4 6 20P
RS 1 3 200
* ES2 MODELS
***   nmos nominal parameters   ** ECDM20 process **
.options tnom=25
.MODEL  N       NMOS        LEVEL=2
+       VTO=0.9       TOX=40E-9      NSUB=.53E16 LD=0.15U
+       UO=510        UEXP=1.29e-2   UCRIT=1E3   VMAX=3.79E4
+       UTRA=0        XJ=.5E-6       NEFF=2.74   NFS=0
+       RSH=40        JS=1.E-4       CGDO=150P   CGSO=150P
+       CJ=110E-6     CJSW=250E-12   MJ=0.48     MJSW=0.27    PB=0.45
+       CAPOP=4
***   pmos nominal parameters   ** ECDM20 process **
.MODEL  P       PMOS        LEVEL=2
+       VTO=-0.6      TOX=40E-9      NSUB=1.9E16  LD=0.2U
+       UO=175        UEXP=3.11E-2   UCRIT=4.72E3 VMAX=3.72E4
+       UTRA=0        XJ=6E-7        NEFF=1       NFS=0
+       RSH=50        JS=1.E-4       CGDO=210P    CGSO=210P
+       CJ=350E-6     CJSW=450E-12   MJ=0.48      MJSW=0.4
+       PB=0.45
+       CAPOP=4
* SIMULATION
.TRAN 0.1N 200N
.PRINT TRAN V(4) V(5) V(6) V(7)
.END
```

Appendix E: Microphotograph of a Compensated Switch Block