

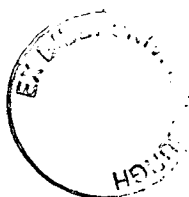
Phase Shifted Bridge Converter for a High Voltage Application

Chee Keong Richard Marcus Loh



**Thesis submitted for the degree of Doctor of Philosophy
The University of Edinburgh**

December 2003



Abstract

In airborne applications, the size and weight of equipment are critical parameters. The power supply for an airborne radar needs to have a high output power density while operating with a high efficiency. Conventional Travelling Wave Tube (TWT) radars require a high voltage power supply for operation and is prone to arcing. As the radar is a crucial piece of equipment, its power supply must be designed to withstand such operation.

The Phase Shifted Pulse Width Modulation Zero Voltage Switching Full Bridge Converter has been the subject of many papers due to its ability to provide high output powers with high efficiency. As the output inductive / capacitive filters used by the present low voltage, high current, phase shifted converters are unsuitable for high output voltage applications, it is replaced with a capacitive filter, altering the basic operation of the converter.

In this thesis the theory and design implementation of the Phase Shifted Bridge with Capacitive Filter (PSBCF) is described. Two auxiliary circuits developed for the conventional phase shifted bridge are analysed and implemented in the new PSBCF. Detailed cycle-by-cycle transient simulations on PSPICE are used to study the converters' behaviour and these are verified with experimental results. An averaged model of the PSBCF running in PSPICE is described and verified using the cycle-by-cycle transient simulations.

Finally, the features and limitations of the PSBCF converter and the use of the auxiliary circuits are discussed and evaluated against each other and against the currently used airborne TWT radar power converter to demonstrate that this technology is a viable replacement.

Declaration

I declare that this thesis has been completed by myself and that, except where indicated to the contrary, the research documented is entirely my own.

Chee Keong Richard M. Loh

Dedication

I would like to dedicate this work to my late brother, Bernard Loh. You are an inspiration to all of us and will be forever in our hearts and minds.

Acknowledgements

I am greatly indebted to my parents for their continuous support and encouragement throughout the period of the research. They have stood by my side and believed in me through the dark periods and celebrated with me during the good times too. I will never be able to repay all their efforts and love, and can only hope that they are proud of my achievements.

Dr. Ewen Macpherson, my supervisor, has always been there whenever I needed him, offering both technical expertise and moral support. His ability to explain difficult problems using simple concepts and provide a reassuring voice whenever I have self doubt is invaluable. For this and much more, I wholeheartedly thank you.

I am grateful to BAE Systems and GEC-Marconi, for providing the scholarship to fund this research, making this project possible. I am very lucky to have Frank Fisher as my industrial liaison, providing both specialist technical knowledge on Radar Systems and industrial expertise during the project, without which certain problems might have taken much longer to solve. Additional thanks also goes to the UK Overseas Research Scholarship council for providing the ORS award which has lighten the burden of expensive school fees on both my parents and me.

To my colleagues in the Institute of Energy Systems (formerly Energy Systems Group) at the University of Edinburgh: Gareth Harrison, Edward Lord, Konstantinos Papastergiou, Selena Feng, Douglas Carmichael, Sarah Graham and Simon Forrest (to but name a few), I thank you for being my Scottish family during my time in the UK. I appreciate your efforts in brainstorming, providing technical assistance, proof-reading and much more. Your hand of heart-warming friendship makes it all worthwhile and because of this, I have never regretted coming to this wonderful university.

I am thankful to the following companies for their kind assistance and generosity in sourcing and providing samples of state-of-the-art components for the research: International Rectifier, Advanced Power Technology, IXYS, Magnetics (Sprang), MMG Sailcrest, Unitrode (Texas Instruments) and Philips Magnetics (Ferroxcube).

Abbreviations

AC	Alternating Current
AP	Active–Passive
ARCP	Active Resonant Commutated Pole
BAe	British Aerospace
BC	Boundary Condition
CCM	Continuous Conduction Mode
CFB	Current Fed Bridge
CRT	Cathode Ray Tube
CW	Continuous Wave
DAB	Dual Active Bridge
DC	Direct Current
DCM	Discontinuous Conduction Mode
EM	Electromagnetic
EMI	Electromagnetic Interference
ESR	Equivalent Series Resistance
FB	Full Bridge
FREDFET	Fast Recovery Epitaxial Diode Field Effect Transistor
HV	High Voltage
IGBT	Insulated Gate Bipolar Transistor
LC	Inductor-Capacitor
LCC	Inductor-Dual Capacitor
LDD	Inductor-Dual Diode
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPP	Molypermalloy Powder
MTBF	Mean Time Between Failure
OC	Open-Circuit
PA	Passive–Active
PCB	Printed Circuit Board
PFC	Power Factor Correction
PPS	Pulses per Second
PRC	Parallel Resonant Converter

PRF	Pulse Repetition Frequency
PS	Phase Shifted
PSB	Phase Shifted Bridge
PSBCF	Phase Shifted Bridge with Capacitive Filter
PWM	Pulse Width Modulation
QRC	Quasi Resonant Converter
RC	Resistor-Capacitor
RF	Radio Frequency
RMS	Root-Mean-Square
SC	Short-Circuit
SEPIC	Single Ended Primary Inductance Converter
SIM	Switched Inductor Model
SMPS	Switched Mode Power Supplies
SPICE	Simulation Program with Integrated Circuit Emphasis
SRC	Series Resonant Converter
SRPC	Series Parallel Resonant Converter
SSA	State Space Averaging
TWT	Travelling Wave Tube
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching
ZVT	Zero Voltage Transition
ZVZCS	Zero Voltage Zero Current Switching

Symbols

ΔX	Change in the Value of X
$\frac{dX}{dt}$	Rate of Change of X with Respect to Time
ω	Angular Frequency in Radians per Second
ω_{AB}	Natural Frequency of PA Leg Resonant Components During PA Transition in Radians per Second
ω_{CD}	Natural Frequency of AP Leg Resonant Components During AP Transition in Radians per Second
μ_e	Magnetic Core Effective Permeability
ϕ_1	Transformer Primary Total Flux
ϕ_2	Transformer Secondary Total Flux
ϕ_c	Transformer Core Linked Magnetic Flux
ϕ_{lk1}	Transformer Primary Leakage Flux
ϕ_{lk2}	Transformer Secondary Leakage Flux
ϕ_l	Total TWT Phase Length
A_e	Effective Cross Sectional Area of Magnetic Core
A_L	Magnetic Core Inductance Factor
A_{min}	Minimum Cross Sectional Area of Magnetic Core
\hat{B}	Peak Flux Density of Magnetic Core
$B_{sat100^\circ C}$	Magnetic Core Saturation Flux Density at 100°C
C_{AB}	Equivalent Capacitance Value for C_{oss} of MOSFET TA and TB Summed
C_{auxn}	LCC Auxiliary Capacitor Number n
C_{block}	Transformer DC blocking Capacitor
C_{CD}	Equivalent Capacitance Value for C_{oss} of MOSFET TC and TD Summed
C_{db}	MOSFET Drain–Base Capacitance
C_{dg}	MOSFET Drain–Gate Capacitance
C_{diodes}	Diode Junction Capacitance Value
C_{dist}	Transformer Distributed Inter-turn Winding Capacitance

C_{dist1}	Transformer Primary Distributed Inter-turn Winding Capacitance
C_{dist2}	Transformer Secondary Distributed Inter-turn Winding Capacitance
C_{ds}	MOSFET Drain–Source Capacitance
C_{gd}	MOSFET Gate–Drain Capacitance
C_{gs}	MOSFET Gate–Source Capacitance
C_n	Capacitor Number n
C_{oss}	MOSFET Output Capacitance
$C_{ossDataSheet}$	Value of C_{oss} Obtained from Manufacturer's Datasheet
$C_{ossEquivalent}$	Equivalent Value of MOSFET Output Capacitance if MOSFET is Subjected to a Step Change in v_{ds}
C_{out}	Output Filter Capacitive Value
C_p	Parallel Capacitor
C_{res}	Resonant Capacitor
C_s	Series Capacitor
d	Duty
D_{auxn}	LDD Auxiliary Diode Number n
d_{BC}	Duty at Boundary Condition
d_{CFBoff}	Equivalent Duty of the Free-wheeling Current Interval for CFB
d_{Cond}	Equivalent Duty of Semiconductor when Conducting Current
d_{fall}	Equivalent Duty of the Passive Interval for PSBCF Operating in DCM
$D_{Freewheel}$	Free-wheeling Diode
d_{loss}	Duty Loss
D_n	Diode Number n
d_{off}	Equivalent Duty of the Passive Interval
d_{offDCM}	Equivalent Duty of the Passive Interval Operating in DCM
d_{on}	Equivalent Duty of the Active Interval
d_{Prec}	Equivalent Duty of the Power Recovery Interval for PSBCF Operating in CCM
D_{rectn}	Output Rectifier Number n
$D_{RvseBlock}$	Reserve Current Blocking Diode
$Delay_{AB}$	Dead Time between Gate Voltage Waveforms of MOSFET A and B for PA Transition
$Delay_{AC}$	Delay between Gate Voltage Waveforms of MOSFET A and C

Delay_{BD}	Delay between Gate Voltage Waveforms of MOSFET B and D
Delay_{CD}	Dead Time between Gate Voltage Waveforms of MOSFET C and D for AP Transition
E_{CossAB}	Amount of Energy Stored in the C_{ossAB}
E_{CossCD}	Amount of Energy Stored in the C_{ossCD}
E_L	Amount of Energy Stored in the Inductor
E_{Laux}	Amount of Energy Stored in the L_{aux}
E_{Lpri}	Amount of Energy Stored in the L_{pri}
$e(X)$	Instantaneous Energy Loss in Component X
f	Frequency
f_{pole}	Frequency of the First Pole for the Error Amplifier
f_{res}	Resonant Frequency
f_{sw}	Switching Frequency
$G(X)$	SPICE Current Generator X Used in Switched Inductor Model
Gain(dB)	Error Amplifier Gain in decibel
$\text{GainBandwidthProduct}$	Error Amplifier Gain Bandwidth Product
i_{arc}	Current Flowing into SPICE Arc Model
$I_{average}$	Averaged Current Value
$i_{average}$	Current Averaged Over a Switching Cycle
I_{BC}	Averaged Boundary Condition Current
I_{D100°	MOSFET Drain Current Rating at 100°C
I_{D25°	MOSFET Drain Current Rating at 25°C
I_{DM}	MOSFET Maximum Peak Pulsed Current
i_{Dn}	Instantaneous Current of Diode n
i_{ds}	MOSFET Drain–Source Current
i_{dsOff}	MOSFET Drain–Source Current Prior to Switch Off
$i_{ds(TX)}$	Drain–Source Current of MOSFET X
i_F	Diode Forward Current
$i_{F(TX)}$	Forward Current for MOSFET X Parasitic Diode
i_{gs}	MOSFET Gate–Source Current
I_{in}	Averaged Converter Input Current
$I_{in(Pk)}$	Converter Peak Input Current Value Within Half a Switching Cycle
I_{inj}	Injected Current Value During Detailed MOSFET Switching Simulation
i_l	Instantaneous Inductor Current
i_{Laux}	Instantaneous Current in L_{aux}
$I_{Laux(Pk)}$	Peak Current Value in L_{aux}
$i_{Laux(RMS)}$	RMS Current Value in L_{aux}

$i_{L_{aux}}(t_n)$	L_{aux} Current Value at Time t_n
$I_{L(Avg)}$	Averaged Inductor Current for Switched Inductor Model
$i_{L_{choke}}$	Instantaneous Current flowing in L_{choke}
$i_{L_{choke}}(t_{mtn})$	Change in L_{choke} Current Value from Time t_m to Time t_n
$i_{L_{choke}}(t_n)$	L_{choke} Current Value at Time t_n
$i_{L_{out}}$	Instantaneous Current of L_{out}
$I_{L_{out}}$	Averaged Current of L_{out}
i_{out}	Instantaneous Converter Output Current
I_{out}	Averaged Converter Output Current
i_{pri}	Instantaneous Current in L_{pri}
I_{pri}	Averaged Current Value of Transformer Primary Winding for Half a Switching Cycle
$I_{pri}(Pk)$	L_{pri} Peak Current Value Within Half a Switching Cycle
$i_{pri}(RMS)$	RMS Current Value of L_{pri} Within Half a Switching Cycle
$i_{pri}(t_{mtn})$	Change in L_{pri} Current Value from Time t_m to Time t_n
$I_{pri}(t_{mtn})$	Averaged Current Value in L_{pri} Between Time t_m to Time t_n
$i_{pri}(t_n)$	L_{pri} Current Value at Time t_n
I_{RM}	Peak Reverse Recovery Current for Diode
I_{SC}	Peak Short-Circuit Current
i_{sd}	MOSFET Source–Drain Current
$i_{sd}(TX)$	Source–Drain Current for MOSFET X
I_{SCmax}	Maximum Peak Short-Circuit Current
i_{sec}	Instantaneous Current Value of Transformer Secondary Winding
I'_{sec}	Averaged Current Value of Transformer Secondary Winding Reflected to the Primary During Half a Switching Cycle
$I'_{sec}(BC)$	Averaged Current Value of Transformer Secondary Winding Reflected to the Primary at Boundary Condition During Half a Switching Cycle
$I_{sec}(Pk)$	Transformer Secondary Winding Peak Current Value Within a Switching Cycle
$I_{SecRect}$	Averaged Rectified Current Value of Transformer Secondary Winding
$I_{t_{mtn}}$	Averaged Current Value During Time Interval between t_m and t_n

i_{Vin}	Instantaneous Input Current Value
I_X	Averaged Current Flowing into Terminal X of Switched Inductor Model
k	Transformer Coupled Inductor Model Coupling Coefficient
K_{SCBC}	Converter Boundary Condition Output Power Coefficient
$K_{SCBCmax}$	Maximum Value of Converter Boundary Condition Output Power Coefficient
L_1	Transformer Coupled Inductor Model Primary Inductance
L_2	Transformer Coupled Inductor Model Secondary Inductance
L_{add}	Value of Series Inductance Required in Additional to L_{leak}
L_{aux}	Auxiliary Inductance
L_{Avg}	Inductor Used in Switched Inductor Model
L_{choke}	CFB DC Choke
l_e	Effective Length of Magnetic Core
L_{leak}	Transformer Leakage Inductance
L_{leak1}	Transformer Primary Leakage Inductance
L_{leak2}	Transformer Secondary Leakage Inductance
L_{lk1}	Transformer Primary Leakage Inductance
L_{lk2}	Transformer Secondary Leakage Inductance
L_{mag}	Transformer Magnetising Inductance
L_{out}	Output Filter Inductor
L_{outn}	Output Filter Inductor Number n
L_{pri}	Equivalent Lumped Inductor Located in Series with Transformer Primary Winding
L_{res}	Resonant Inductor
L_s	Series Inductor
m	Mass
M	Modulation Index
M_{opt}	Optimum Modulation Index
N	Transformer Primary Secondary to Primary Turns Ratio
N_p	Number of Turns on Transformer Primary Winding
N_s	Number of Turns on Transformer Secondary Winding
P_A	Average Power of Pulsed Radar
P_{BCmax}	Maximum Power at Boundary Condition
$P_{Capacitors}$	Total Power Loss in Capacitors
$P_{CauxEsr}$	Power Loss to Equivalent Series Resistance of Auxiliary Capacitors

P_{CEst}	Power Loss to Equivalent Series Resistance of Output Capacitors
P_{Cond}	Semiconductor Conduction Power Loss
$P_{CondFWDiode}$	CFB Free-wheeling Diode Conduction Power Loss
$P_{condLoss}$	Semiconductor Conduction Power Loss
$P_{CondMOSFET}$	MOSFET Conduction Power Loss
P_{condTX}	Conduction Power Loss in MOSFET X
P_{Diodes}	Total Diode Power Loss
P_{Doff}	Diode Turn-off Power Loss
P_{HVRect}	High Voltage Rectifier Diode Power Loss
P_{in}	Converter Input Power
$P_{LauxCore}$	CFB L_{aux} Core Power Loss
$P_{LauxWdg}$	CFB L_{aux} Winding Power Loss
$P_{LChokeCore}$	CFB L_{choke} Core Power Loss
$P_{LChokeWdg}$	CFB L_{choke} Winding Power Loss
P_{LD}	Power Loss Density of Magnetic Core
P_{loss}	Power Loss
$P_{LpriCore}$	L_{pri} Core Power Loss
$P_{LpriWdg}$	L_{pri} Winding Power Loss
P_M	Peak Power of Pulsed Radar
$P_{Magnetics}$	Total Power Loss for Magnetic Components
P_{out}	Converter Output Power
P_{outBC}	Output Power at Boundary Condition
$P_{RadarAvg}$	Averaged Power of Pulsed Radar
P_{SC}	Converter Output Power During an Output Short-Circuit
P_{Sw}	Semiconductor Switching Power Loss
$P_{SwFWDiode}$	CFB Free-wheeling Diode Switching Power Loss
$P_{SwMOSFET}$	MOSFET Switching Power Loss
$P_{TotalMOSFET}$	Total MOSFET Power Loss
$p(X)$	Instantaneous Power Loss in Component X
$P_{XfmrCore}$	Transformer Core Power Loss
$P_{XfmrWdg}$	Transformer Winding Conduction Power Loss
Q_{rr}	Reverse Recovery Charges
R_b	MOSFET Base Resistance
R_{core}	Transformer Core Loss Equivalent Resistance
R_{DCn}	Transformer Winding n DC Resistance
R_{DSon}	Drain–Source Resistance Value
R_{Load}	Output Resistive Load Value
R_n	Resistor Number n
S	Softness of Diode During Reverse Recovery

T	Period of a Single Switching Cycle
t	Time variable
$T_{0.5}$	Half Period of a Switching Cycle
t_{80pc}	Time Taken for the v_{ds} to Charge to 80% of Its Final Value when Determining C_{oss} Value
t_a	Time Taken for Diode to Reach I_{RM} During Reverse Recovery
t_b	Time Taken for Reverse Recover Current to Reduce from I_{RM} to $I_{RM}/10$
T_D	Pulse Duration of Pulsed Radar Waveform
t_{fall}	MOSFET Switching Fall Time
t_n	Time at Point n
t_{off}	Duration of Passive Current Free-wheeling
t_{on}	Duration of Active Power Transfer
T_R	Pulse Spacing of Pulsed Radar Waveform
$t_{resonant}$	Duration of Parasitic Resonant Interval After i_{pri} has Fallen to Zero
t_{rise}	MOSFET Switching Rise Time
t_{rr}	Diode Reverse Recovery Time
TX	MOSFET X
v_A	Voltage at the Midpoint of the PA Leg
v_{arc}	Voltage Across SPICE Arc Model
$v_{average}$	Voltage Averaged Over a Switching Cycle
v_B	Voltage at the Midpoint of the AP Leg
V_{Cath}	TWT Cathode Voltage
V_{Coss}	Drain–Source Voltage Value to which the MOSFET is Charged to Determine its C_{oss} Value
v_d	Instantaneous Drain Voltage
$v_{drive}(TX)$	Driving Waveform for MOSFET X
v_{ds}	Instantaneous Drain–Source Voltage
V_{dsOff}	MOSFET Drain–Source when Switched Off
$v_{ds}(TX)$	Drain–Source Voltage of MOSFET X
V_{DSS}	MOSFET Maximum Reverse Blocking Voltage
V_e	Effective Volume of Magnetic Core
V_F	Diode Forward Voltage Drop During Conduction
v_g	Instantaneous Gate Voltage
v_{gs}	Gate–Source Voltage
$v_{gs}(TX)$	Gate–Source Voltage of MOSFET X
$v_{GS}(TX)$	Gate–Source Voltage of MOSFET X within the Packaging
V_{in}	Converter Input Voltage

V_{inmax}	Maximum Converter Input Voltage
$V_{L(Avg)}$	Averaged Inductor Voltage for Switched Inductor Model
v_{Lchoke}	Instantaneous Voltage Across L_{choke}
V_{out}	Converter Output Voltage
v'_{out}	Instantaneous Transformer Secondary Winding Voltage Value Reflected Back to Primary
V'_{out}	Output Voltage DC Value Reflected Back to Primary Winding of Ideal Transformer
v_{pri}	Instantaneous Voltage Across Transformer Primary Winding and L_{pri}
$v_{s0}(TPWM)$	Source–Ground Voltage of MOSFET TPWM
$v_{sd}(TX)$	Source–Drain Voltage of MOSFET X
V_R	Diode Reverse Blocking Voltage
V_{rr}	Reverse Blocking Voltage for Fully Recovered Diode
V_X	Voltage of Terminal X of Switched Inductor Model
x	Inductor Current State Variable
y	Capacitor Voltage State Variable

Contents Summary

Abstract	i
Abbreviations	v
Symbols	vii
Contents Summary	xv
List of Figures	xviii
List of Tables	xxii
1 Introduction	1
2 Switched Mode Power Supplies	6
3 Airborne TWT Radar Power Supplies	30
4 Method of Design	60
5 Modelling and Simulation	79
6 Testing and Results	104
7 Evaluation, Comparison and Discussion	142
8 Conclusions and Future Work	164
References	168
A Additional Results	175
B C_{oss} Value Derivation	185
C PSBCF Average Model PSPICE Code	187
D Publications	190

Contents

Abstract	i
Abbreviations	v
Symbols	vii
Contents Summary	xv
List of Figures	xviii
List of Tables	xxii
1 Introduction	1
1.1 Thesis Background	1
1.2 Project Objectives and Scope	2
1.3 Thesis and Contribution to Knowledge	3
1.4 Thesis Outline	4
2 Switched Mode Power Supplies	6
2.1 Switched Mode Power Supply Basics	6
2.1.1 Basic Converter Types	6
2.1.2 Output Voltage Control	8
2.1.3 Current Conduction Modes	10
2.1.4 Types of Switching	11
2.2 Resonant Topologies	14
2.2.1 Load Resonant Converters	14
2.2.2 Quasi Resonant Converters	17
2.3 Phase Shifted Bridge Converters	18
2.3.1 PS-PWM-ZVS-FB Converter	18
2.3.2 PS-PWM-ZCS-FB Converter	25
2.4 High Voltage Application Voltage Step Up Techniques	26
2.5 Chapter Summary	29
3 Airborne TWT Radar Power Supplies	30
3.1 TWT Radar Introduction	30
3.2 Problems with TWT Radar	34
3.2.1 Spectral Purity of Signal	34
3.2.2 Arcing	35
3.3 Current Fed Bridge Converter	37
3.4 Capacitive Filter Versus LC Filter	39
3.5 Phase Shifted Bridge Converter with Capacitive Filter	40

3.5.1	Detailed Operation in DCM	40
3.5.2	Detailed Operation in CCM	45
3.5.3	Deficiencies	49
3.5.4	Operation Under Extreme Conditions	51
3.5.5	Improvements to the PSBCF	52
3.5.6	LDD Auxiliary	52
3.5.7	LCC Auxiliary	56
3.6	Chapter Summary	58
4	Method of Design	60
4.1	Background	60
4.2	Determination of Operating Conditions	60
4.2.1	Power Limitation	60
4.3	MOSFET	67
4.3.1	Determination of C_{oss}	69
4.4	Transformer	71
4.5	Inductor	72
4.6	Output Capacitors	74
4.7	Other Components	76
4.7.1	Resonant Transition Setting	77
4.8	Chapter Summary	77
5	Modelling and Simulation	79
5.1	Computer Simulation	79
5.2	Comparison of Averaging Techniques	80
5.2.1	State Space Averaged Models	82
5.2.2	PWM Switch Averaged Model	82
5.2.3	Switched Inductor Model	84
5.3	PSPICE Implementation	85
5.3.1	Switched Model	85
5.3.2	Model of MOSFET	86
5.3.3	Transformer Modelling	87
5.3.4	Determination of Transformer Parasitic Values	89
5.4	Mathcad Simulation	97
5.5	SIM Transient Average Model Equations	98
5.6	Small Signal Model	100
5.7	Arc Simulation Using Low Resistance Load	101
5.8	Chapter Summary	103
6	Testing and Results	104
6.1	Background	104
6.2	Hardware Prototype	105
6.2.1	Prototyping Difficulties	109
6.3	Test Procedure	110
6.3.1	Steady-state Operation	111
6.3.2	Output Short-circuit Operation	124
6.4	Switching Transition Simulations Using Accurate MOSFET Models	133
6.4.1	Orcad PSPICE Model Limitation	133
6.4.2	Switch Transitions Under Different Conditions	133
6.5	Efficiency and Temperature Readings	139

6.6	Chapter Summary	140
7	Evaluation, Comparison and Discussion	142
7.1	Discussion	142
7.2	Losses	146
7.2.1	MOSFET Conduction Losses	146
7.2.2	ZVS Sensing Drive Circuitry	153
7.2.3	Diode Losses	154
7.2.4	Magnetic Component Losses	155
7.2.5	Overall Estimated Losses	156
7.3	Comparison of PSBCF with CFB	158
7.4	Short-circuit Performance	160
7.4.1	Limitation of Simulation	162
7.5	Chapter Summary	163
8	Conclusions and Future Work	164
8.1	Conclusion	164
8.2	Future Work	166
	References	168
A	Additional Results	175
A.1	LDD Auxiliary Circuit	175
A.2	LCC Auxiliary Circuit	180
B	C_{oss} Value Derivation	185
C	PSBCF Average Model PSPICE Code	187
D	Publications	190

List of Figures

2.1	Basic Converter Types	7
2.2	Full Bridge Converter Topology	8
2.3	Waveforms of Various Duty Modulation Techniques	9
2.4	Current Waveforms for Different Conduction Modes	10
2.5	Typical MOSFET Hard Switching Waveforms	12
2.6	Simple ZCS Circuit and Waveforms	12
2.7	Simple ZVS Circuit and Waveforms	13
2.8	Generic Resonant Mode Loading	14
2.9	Various Resonant Switch Replacement Configurations for QRCs . . .	17
2.10	Schematic and Waveforms for PS-PWM-ZVS-FB Converter	20
2.11	Various PA Leg Resonant Transition Waveforms	23
2.12	PS-PWM-ZVS-FB Converter with Current Doubler Rectifier	25
2.13	Cockcroft-Walton Voltage Multiplier	27
2.14	Various High Voltage Transformer Configuration	28
3.1	Cross Section of TWT Radar	30
3.2	A Pulsed Radar Loading Waveform	34
3.3	TWT Crowbar Circuit with Self-triggering 3-electrode Spark Gap . .	36
3.4	Typical Waveforms for 3-electrode Spark Gaps	37
3.5	Current Fed Bridge Topology and Operating Waveforms	38
3.6	PSBCF Topology and Operating Waveforms	41
3.7	Voltage and Current Waveform for PSBCF (DCM)	42
3.8	Circuit Representation for PSBCF during DCM Sub-Intervals	42
3.9	Voltage and Current Waveform for PSBCF (CCM)	46
3.10	Circuit Representation for PSBCF during CCM Sub-Intervals	47
3.11	Equivalent Circuit Showing $C \frac{dv}{dt}$ Turn-on	49
3.12	Reverse Recovery Time for MOSFET Body Diode	51
3.13	PSBCF with LDD Auxiliary Circuit	53
3.14	Diode Voltage and Current Waveforms During Reverse Recovery . . .	54
3.15	PSBCF with LCC Auxiliary Circuit	57
4.1	Converter Output Power at Various Modulation Index and Duty . . .	61
4.2	Converter Input Current at Various Modulation Index and Duty . . .	62
4.3	Converter Output Current at Various Modulation Index and Duty . .	62
4.4	Characteristics of PSBCF Converter when V_{out} is Held Constant . . .	63
4.5	Characteristics of PSBCF Converter when V_{in} is Held Constant . . .	63
4.6	Graph of i_{pri} at Boundary Condition	64
4.7	Graph of K_{SCBC} Against M	66
4.8	L_{pri} Current and Converter Duty for Worst Case Output Short-circuit	67
4.9	Body Diode Reverse Recovery Comparison	69

4.10 Test Setup for Measuring MOSFET C_{oss}	70
4.11 Boundary Condition P_{out} at Various Transformer Turns Ratio	71
4.12 U-core Transformer with Excessive Leakage Magnetic Fields	72
5.1 Switched and Averaged Voltage and Current Waveforms	80
5.2 State Space Averaging Model	82
5.3 PWM Switch Averaging Models	83
5.4 Switched Inductor Averaging Model	84
5.5 PSPICE Model Editor Software Screen Capture	86
5.6 Cross Section of a Transformer	88
5.7 Transformer Model	88
5.8 Transformer Model with Secondary Components Referred to Primary	88
5.9 Magnetics Analyser Impedance Magnitude Measurement Printout for Prototype Transformer (OC)	91
5.10 Magnetics Analyser Phase Measurement Printout for Prototype Transformer Model (OC)	91
5.11 Mathcad Impedance Magnitude Plot for Transformer Model (OC) with Parasitic Inductances and Capacitances.	91
5.12 Mathcad Phase Plot for Transformer Model (OC) with Parasitic Inductances and Capacitances	91
5.13 Magnetics Analyser Impedance Magnitude Measurement Printout for Prototype Transformer (SC)	92
5.14 Magnetics Analyser Phase Measurement Printout for Prototype Transformer Model (SC)	92
5.15 Mathcad Impedance Magnitude Plot for Transformer Model (SC) with Parasitic Inductances and Capacitances	92
5.16 Mathcad Phase Plot for Transformer Model (SC) with Parasitic Inductances and Capacitances	92
5.17 PSPICE Schematic of Open Loop PSBCF (No Auxiliary)	93
5.18 Non-ideal Transformer PSPICE Model Referred to Primary	93
5.19 PSPICE Schematic of Closed Loop PSBCF (No Auxiliary)	95
5.20 PSPICE Digital Circuitry for Producing Phase Shifted Driving Waveforms	96
5.21 Feedback Circuitry for Closed Loop Simulation	96
5.22 PSPICE Schematic of Closed Loop PSBCF (LDD)	96
5.23 PSPICE Schematic of Closed Loop PSBCF (LCC)	97
5.24 Averaged Model of PSBCF	98
5.25 PSPICE AC Simulation Schematic for PSBCF Averaged Model	101
5.26 PSPICE AC Simulation Results for PSBCF Averaged Model	102
5.27 PSPICE Output Load and Resistive Short Circuit Model	102
6.1 Schematic of PSBCF Prototype	106
6.2 Photograph of PSBCF Prototype with No Auxiliary Circuit	108
6.3 Photograph of PSBCF Prototype with LDD Auxiliary Circuit	109
6.4 Photograph of PSBCF Prototype with LCC Auxiliary Circuit	109
6.5 Prototype PSBCF (No Auxiliary) Transformer Waveforms (Half Load)	113
6.6 PSPICE PSBCF (No Auxiliary) Transformer Waveforms (Half Load)	113
6.7 Prototype PSBCF (No Auxiliary) MOSFET TB Waveforms (Half Load)	114
6.8 Prototype PSBCF (No Auxiliary) MOSFET TB Waveforms (Half Load)	114
6.9 Prototype PSBCF (No Auxiliary) MOSFET TD Waveforms (Half Load)	115

6.10	Prototype PSBCF (No Auxiliary) MOSFET TD Waveforms (Half Load)	115
6.11	Prototype PSBCF (LDD) Transformer Waveforms (Full Load)	116
6.12	PSICE PSBCF (LDD) Transformer Waveforms (Full Load)	116
6.13	Prototype LDD Auxiliary Inductor Waveforms (Full Load)	117
6.14	PSICE LDD Auxiliary Inductor Waveforms (Full Load)	117
6.15	Prototype PSBCF (LDD) MOSFET TB Waveforms (Full Load)	118
6.16	PSICE PSBCF (LDD) MOSFET TB Waveforms (Full Load)	118
6.17	Prototype PSBCF (LDD) MOSFET TD Waveforms (Full Load)	119
6.18	PSICE PSBCF (LDD) MOSFET TD Waveforms (Full Load)	119
6.19	Prototype PSBCF (LCC) Transformer Waveforms (Full Load)	120
6.20	PSICE PSBCF (LCC) Transformer Waveforms (Full Load)	120
6.21	Prototype LCC Auxiliary Inductor Waveforms (Full Load)	121
6.22	PSICE LCC Auxiliary Inductor Waveforms (Full Load)	121
6.23	Prototype PSBCF (LCC) MOSFET TB Waveforms (Full Load)	122
6.24	PSICE PSBCF (LCC) MOSFET TB Waveforms (Full Load)	122
6.25	Prototype PSBCF (LCC) MOSFET TD Waveforms (Full Load)	123
6.26	PSICE PSBCF (LCC) MOSFET TD Waveforms (Full Load)	123
6.27	PSICE Simulation (SC) for PSBCF (No Auxiliary)	126
6.28	PSICE Simulation (SC) for PSBCF (No Auxiliary) (Detailed)	126
6.29	PSICE Simulation (SC) for PSBCF (LDD)	127
6.30	PSICE Simulation (SC) for PSBCF (LDD) (Detailed)	127
6.31	PSICE Simulation (SC) for PSBCF (LCC)	128
6.32	PSICE Simulation (SC) for PSBCF (LCC) (Detailed)	128
6.33	PSICE Simulation (SC) for PSBCF Using Averaged Model	129
6.34	PSICE Simulation (SC) for PSBCF Using Ideal Model	129
6.35	PSICE Simulation (SC) for CFB	130
6.36	PSICE Simulation (SC) for CFB (Detailed)	130
6.37	PSICE PSBCF Outputs During Short-circuit	131
6.38	PSICE CFB Outputs During Short-circuit	131
6.39	Output Short-circuit Waveform for PSBCF (LDD)	132
6.40	Output Short-circuit Waveform for PSBCF (LCC)	132
6.41	Transition Waveforms During Switching of Orcad PSICE MOSFET Model	134
6.42	Transition Waveforms During Switching of Infineon PSICE MOSFET Model	135
6.43	PSICE Schematic for Simulation of Infineon MOSFET Model Switching	135
6.44	PSICE Simulation of Hard Switching Using Infineon MOSFET Model, $I_{inj} = 0A$	136
6.45	PSICE Simulation of Hard Switching Using Infineon MOSFET Model, $I_{inj} = 2A$	137
6.46	PSICE Simulation of Hard Switching Using Infineon MOSFET Model, $I_{inj} = 8A$	137
6.47	PSICE Simulation of ZVS Transition Using Infineon MOSFET Model, $I_{inj} = -8A$	138
6.48	PSICE Simulation of ZVS Transition Using Infineon MOSFET Model with Zero Voltage Sensing Circuitry	138
7.1	Effect of Parasitic Resonance on ZVS	142
7.2	MOSFET Parasitic Diode Recovery with High $\frac{dv}{dt}$	143
7.3	Bipolar Gate Pulse Transformer Circuit	144

7.4	Graph of PSBCF $i_{pri(RMS)}/I'_{sec}$ Against I'_{sec}	149
7.5	MOSFET Conduction Losses Against Output Power	149
7.6	MOSFET Conduction Losses for PA Leg with LDD Auxiliary Against Output Power	150
7.7	MOSFET Conduction Losses for PA Leg with LCC Auxiliary Against Output Power	151
7.8	Automatic ZVS Sensing Drive Circuitry	154
7.9	Chart of Losses for the Various Converters	158
7.10	Chart of Losses Expressed as Percentage of the Overall Losses for the Various Converters	159
7.11	Diode Modifications to MOSFET to Prevent Body Diode Conduction	159
A.1	Prototype PSBCF (LDD) Transformer Waveforms (Half Load)	176
A.2	PSPICE PSBCF (LDD) Transformer Waveforms (Half Load)	176
A.3	Prototype LDD Auxiliary Inductor Waveforms (Half Load)	177
A.4	PSPICE LDD Auxiliary Inductor Waveforms (Half Load)	177
A.5	Prototype PSBCF (LDD) MOSFET TB Waveforms (Half Full Load)	178
A.6	PSPICE PSBCF (LDD) MOSFET TB Waveforms (Half Load)	178
A.7	Prototype PSBCF (LDD) MOSFET TD Waveforms (Half Load)	179
A.8	PSPICE PSBCF (LDD) MOSFET TD Waveforms (Half Load)	179
A.9	Prototype PSBCF (LCC) Transformer Waveforms (Half Load)	181
A.10	PSPICE PSBCF (LCC) Transformer Waveforms (Half Load)	181
A.11	Prototype LCC Auxiliary Inductor Waveforms (Half Load)	182
A.12	PSPICE LCC Auxiliary Inductor Waveforms (Half Load)	182
A.13	Prototype PSBCF (LCC) MOSFET TB Waveforms (Half Load)	183
A.14	PSPICE PSBCF (LCC) MOSFET TB Waveforms (Half Load)	183
A.15	Prototype PSBCF (LCC) MOSFET TD Waveforms (Half Load)	184
A.16	PSPICE PSBCF (LCC) MOSFET TD Waveforms (Half Load)	184

List of Tables

3.1	Some TWTs by Litton Electron Devices	32
3.2	A Selection of Typical Pulsed Radars	33
3.3	Breakdown Voltages for Various Media	35
4.1	Survey of MOSFETs from Three Manufacturers	68
4.2	Data for Ferroxcube EE65/32/27-3F3 E-core	73
4.3	Winding Data for Main Transformer	73
4.4	L_{add} Design Data	74
4.5	LDD Auxiliary L_{aux} Design Data	75
4.6	LCC Auxiliary L_{aux} Design Data	75
4.7	UC3879 Setup Data	76
4.8	IR2113 Setup Data	77
5.1	Simulation Strategies for Some Typical Power Supply Analysis	81
5.2	Summary of Transformer Parameter Extraction	90
5.3	MOSFET Gate Drive Settings for Open Loop PSPICE Simulation	90
5.4	Values Used to Configure Operational Amplifier Model Within UC3879 Model	94
6.1	Components for Prototype PSBCF Converter Schematic Shown in Figure 6.1	107
6.2	Voltmeter, Ammeter Readings and Efficiency Results	139
6.3	Temperature Readings for Various Converter Components	140
7.1	Assumption Used for Estimating Losses for the CFB and PSBCF Converters	147
7.2	Parameters Used for Loss Estimation	147
7.3	Current Values Used for Loss Estimation	147
7.4	MOSFET Losses for the Various Converters	152
7.5	Core Loss Information for the Various Magnetic Components	155
7.6	Breakdown of Estimated Losses for the Various Converters	156

Chapter 1

Introduction

1.1 Thesis Background

The total estimated market for switched mode power supplies (SMPS) is considerable, estimated to be worth around US\$10.1 billion in 2002 growing to US\$15.6 billion in 2009 [1]. Of this, alternating current–direct current (AC–DC) SMPS still accounts for the majority of the sales with 64.4% of the total revenue in 2002. However, DC–DC converters are expected to increase its share to 41.7% of the market by the end of the forecast period, fuelled by the use of a single AC–DC converter equipped with power factor correction and several distributed DC–DC converters. [2] also predicts a growth in the DC–DC converter market from US\$2.68 billion in 2002 to US\$4.33 billion in 2007. With recent military conflicts in Afghanistan (2002) and Iraq (2003) contributing to an economic slowdown, the growth during this period is expected to be fuelled by military and defence needs, after which, the consumer market is expected to take over.

In most SMPS markets such as computer and telecommunication systems the demand has been concentrated at the low voltage range, such as an increasing demand for 2.5 V outputs for computers, 48 V inputs for both computer and communication systems [2] and 48 V outputs for new hybrid electric cars.

In the aerospace defence market, the demand for switched mode converters is expected to come from replacement of old equipment with new models with modern power supplies. To speed up development, reduce cost and ease replacement of faulty power supplies, there have been attempts to replace the custom military power supplies with standardised high efficiency commercial products. However, due to the stringent operation requirements for military products such as reliability, ruggedness and wide operating temperature ranges, customisation of the power supply to the equipment, its specific use and environmental condition is still required.

The market for power supplies for medical equipment too is important, estimated to grow at a rate of around 8.9% annually up to 2009. Medical equipment is required to measure sensitive signals and needs to operate in an environment relatively free of electromagnetic interference. The power requirements for medical equipment can also range from simple battery powered thermometers to power hungry Electromagnetic Resonance Imaging machines. It is foreseen that while the demand for High Voltage (HV) medical power supplies remain, there will be an increased importance of lightweight, portable and reliable power supplies for use in easily transportable medical equipment.

There are many applications, both commercial and research, which require the use of high voltage power supplies. These can range from use in commercial semiconductor manufacturing processes such as ion implantation and electron beam lithography to powering of large research equipment such as particle accelerators and cyclotron sources, from medical X-ray systems to military radar power supplies.

Radar systems play an important role in modern society. They have been attributed as a key factor in helping the allies win the war during World War II and are still being used as the 'eyes' for military installations around the world. They are an essential item in modern transport for aircraft, ships and increasingly in prototype cars for navigation and collision avoidance.

A particular application for a regulated high voltage power supply is for a Travelling Wave Tube (TWT) radar. Invented in 1943, by Rudolf Kompfner, the TWT requires a high voltage input supply for operation. As these are used in both aircraft radar systems and in space satellites, its power supply must be rugged, lightweight and highly efficient for there is usually a limited energy resource in such applications.

As data concerning such applications are very sensitive, not much information and published papers are available in the public domain. From discussions with the industrial sponsor of this project (BAe Systems), it is understood that the SMPS in use for their particular systems is in need of replacement.

SMPS manufacturers in recent years, have been increasingly interested in using the phase shifted full bridge (PSB) converter as their choice of high power converter due to its simple design, high efficiency and availability of dedicated control chips. However, due to the growing demand in the low output voltage sector, development has been primarily in that area.

1.2 Project Objectives and Scope

The project had several distinct objectives:

1. To develop the standard phase shifted bridge converter to be suitable for a high voltage application (airborne TWT radar) and study its operation.
2. To have a method of design which maximises the output power of the converter while maintaining high efficiency.
3. To create various models of the converter so as to allow simulation to gain a better understanding of the converter.
4. To build a prototype converter based on the new design using the method developed.
5. To study, implement and test if auxiliary circuits would improve the performance of the PSB converter.
6. To verify the simulations with results from the prototype.

The scope of the project is contained within designing a high voltage phase shifted bridge converter with capacitive filter which operates at a reduced output voltage of 1 kV but at the full output power normally required by a typical TWT radar. The auxiliary circuits examined in the thesis to aid performance are the inductor–dual capacitor (LCC) and inductor–dual diode (LDD) circuits. Simulations are carried out using a variant of the industry standard circuit simulation package SPICE. The merit for performance criterion is primarily measured in terms of efficiency and immunity to output short-circuits (SCs) which is critical to reliability in this application.

1.3 Thesis and Contribution to Knowledge

Overall, the project will test the hypothesis that: The phase shifted bridge converter with capacitive filter is a suitable converter for high voltage applications and is a suitable replacement for the current fed bridge converter presently used in airborne TWT radars.

The conventional phase shifted bridge converter has been studied in detail for many years, but most of this work has been concentrated on low to medium output voltages with high current. Not much work has been done to investigate into the operation and performance of the converter with high output voltages, by removing the output filter inductor. The operation of this new variation of the phase shifted bridge converter differs from the conventional converter and this thesis shows how this operates and how it can be improved with two auxiliary circuits adapted from the conventional converters.

While most switched mode converters rely on a large choke and/or quick over-current sensors to detect and limit the damage caused by output short-circuits, this converter

achieves output short-circuit immunity with the use of a single inductor located in series with the main transformer. This thesis also shows how the converter can be designed to maximise output power for the converter while limiting the short-circuit currents and still maintain high efficiency.

As the converter operates differently from other converters, a new averaged PSPICE simulation model is developed and tested which simulates the converter in both continuous and discontinuous conduction mode.

1.4 Thesis Outline

The thesis consists of eight chapters, together with necessary appendices.

Chapter 2 introduces the basics of Switched Mode Power Supplies. It describes some of the common topologies used in DC–DC converters and the benefits and disadvantages of each topology and how it leads up to the present day phase shifted converter. Converters for high voltage applications are also briefly discussed.

Chapter 3 highlights a particular application for high voltage SMPS: Airborne TWT radar power supply. The TWT radar is introduced along with the particularly stringent operational requirements for its power supply. The operation of the current fed bridge converter presently in use and the proposed modified phase shifted bridge converter with capacitive filter are described. Two possible improvement auxiliary circuits for the phase shifted bridge converter are introduced along with how they change the operation of the converter.

Chapter 4 details how the proposed phase shifted bridge converter should be designed to maximise its output power while maintaining high efficiency and be immune to output short-circuits. Various components of the converter are described along with how they are selected to best suit this particular application.

Chapter 5 specifies how the converter is modelled and simulated on a computer primarily using PSPICE. It compares the trade-offs between speed and accuracy of simulation result between the averaged and transient model and suggests when each should be used. Accurate models for the transformer and other important components of the converter are also detailed.

Chapter 6 presents results of various simulations and the tests carried out using the prototype phase shifted bridge converter. Simulation results for different loadings are compared and verified against experimental results. Averaged mode simulations were verified against transient simulations. Short-circuit tests results are also presented and are verified against transient simulations. Short comings of each simulation are also highlighted.

Chapter 7 discusses some problems encountered when designing the prototype phase shifted bridge converter. The converter's overall efficiency and losses for its various components are evaluated and compared to those of the current TWT radar power supply. The performance of the converter during an output short-circuit is also discussed.

Finally, Chapter 8 describes the recommended future work for the project, summarises the thesis and draws conclusions from the work carried out.

Chapter 2

Switched Mode Power Supplies

2.1 Switched Mode Power Supply Basics

2.1.1 Basic Converter Types

There are three basic SMPS configurations commonly used: Buck, Boost and Buck-Boost. Figure 2.1 show the three configurations in a non-isolated setup. The different configurations are achieved by changing the positions of the switch, diode and inductor in the 'T-cell'. Other less commonly used topologies include the Cuk converter and the Single-Ended Primary Inductance Converter (SEPIC).

Power is transferred differently in the three converter configuration. Buck converters perform inductor current charging and power transfer during the period when the switch is on (t_{on}) while current circulates through the diode during the off period (t_{off}). Boost and Buck-Boost converters operate in a similar manner whereby inductor charging occurs during t_{on} and power transfer during t_{off} . Due to the difference in converter configuration, the output voltage also differs between the three setups. Voltage is always stepped down in a Buck converter, stepped up in a Boost converter while the Buck-Boost has an output voltage which is stepped up or down but inverted in polarity. The equations which govern the output voltage, V_{out} , and input voltage, V_{in} , relationships in continuous conduction mode are shown in Figure 2.1 [3] in terms of the duty ratio, d (ratio of switch t_{on} to switching period).

By themselves, these converters are of limited use. The lack of isolation limits their operation to low voltages, and the confined way in which voltage is modulated restricts their operation to a narrow range. The use of a transformer solves these problems by providing isolation between input and outputs while allowing the output voltage range to be expanded. Some examples of isolated topologies are the Forward (Buck derived), Flyback (Buck-Boost derived), Push-Pull, Half Bridge and

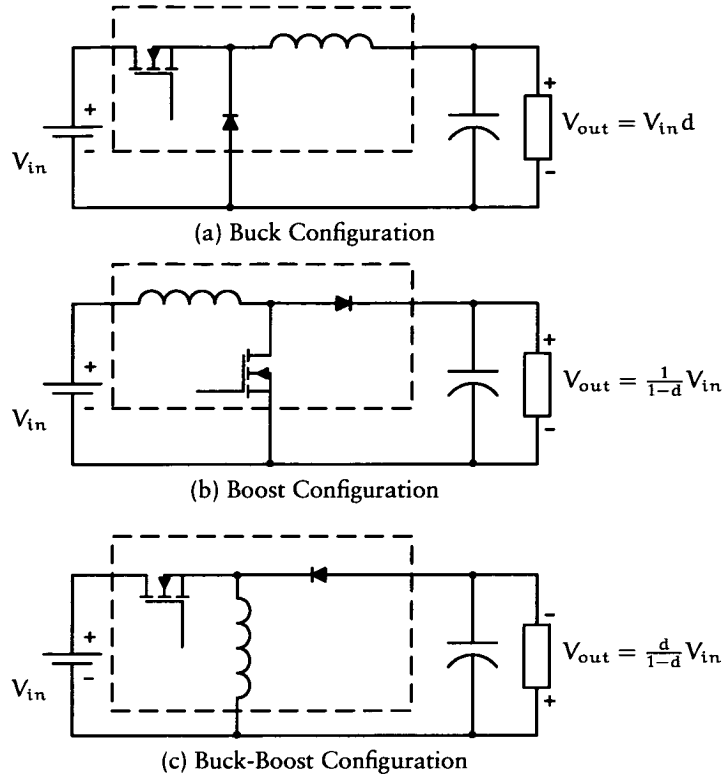


Figure 2.1: Basic Converter Types

Full Bridge (FB). In particular, the full bridge converter is the topology of choice when high powered converters are required.

Full Bridge Converter

The full bridge converter consists of four switches, Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) in this example, arranged in a 'H' configuration as shown in Figure 2.2. It is the preferred topology for high powered converters because of low voltage and current stress on the MOSFETs while maximising the utilisation of the transformer's capability. Voltage stress across each of the MOSFET is just that of the input voltage. The traditional Full Bridge converter operates by alternately switching on the diagonally opposite pairs of MOSFETs to transfer power from the input to the output through the transformer. During the period where all MOSFETs are switched off, the currents will continue to circulate in the transformer secondary until excitation in the opposite direction by the second diagonal pair of MOSFETs.

Due to parasitic inductances and capacitances not shown in Figure 2.2, snubbers are usually required around each MOSFET to reduce voltage and current ringing and power loss. Snubbers can come in the form of passive or active circuits, the choice being usually a trade-off between power loss and complexity.

If the input voltage is higher than the blocking voltage of the available MOSFETs,

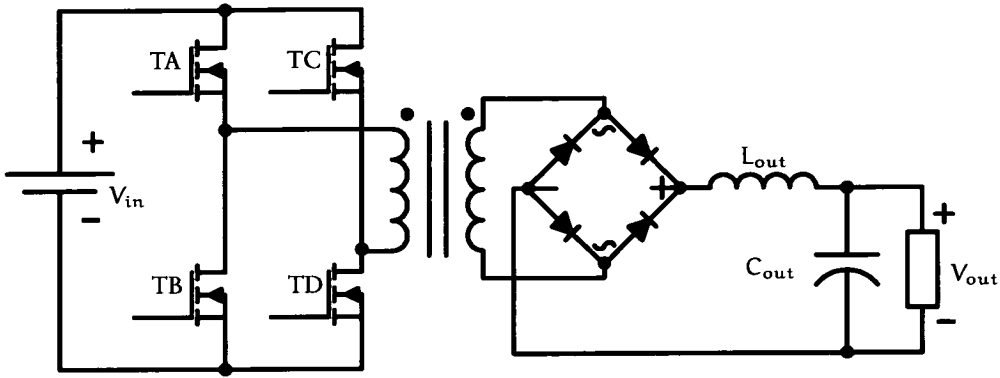


Figure 2.2: Full Bridge Converter Topology

the solution is to either replace the MOSFETs with Insulated Gate Bipolar Transistors (IGBTs) or use another topology such as the three level Pulse Width Modulation (PWM) converter [4] or the soft switching version of it described in [5]. Unfortunately, IGBTs suffer from higher switching losses than MOSFETs due to the tail current present when the IGBT is turned off. The switching losses limit the operation of the converter to relatively low switching frequencies.

2.1.2 Output Voltage Control

The desired output voltage is achieved by two means. First, the basic topology of converter determines if the output voltage of the converter is stepped up (*e.g.* Boost) or stepped down (*e.g.* Buck) (Figure 2.1). This is followed by the use of a high frequency transformer, which transforms the pulsed waveform to the required output level. Then the converter's duty, d , is controlled dynamically by the control loop allowing for fine control of the output voltage. There are several different ways of performing duty modulation and they can be classified under fixed frequency or variable frequency (Figure 2.3).

Fixed Frequency

Duty is modulated by varying the on time within a fixed period such that the overall switching and operating frequency remains constant. This is known as Pulse Width Modulation (PWM) control. PWM control has the benefit of keeping the operating frequency constant. This allows multiple converters to be synchronised and paralleled up for high power conversion. The operating conditions for magnetic and filter components are also better defined for easier design.

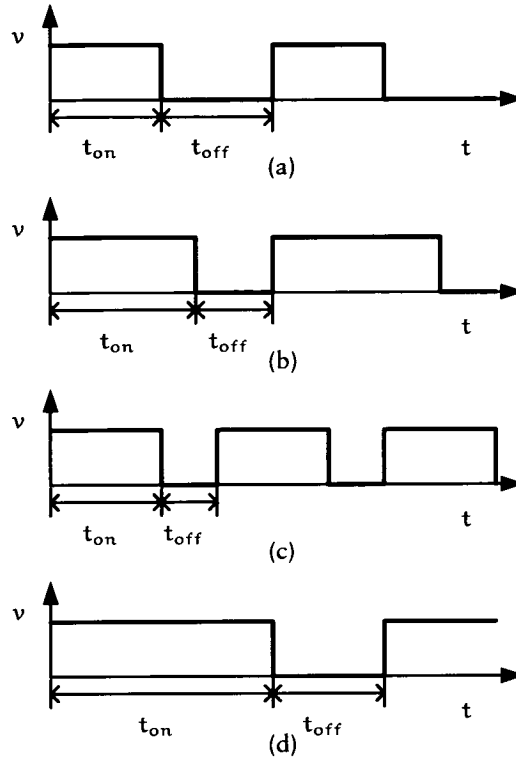


Figure 2.3: Waveforms of Various Duty Modulation Techniques. (a) Original Waveform; (b) PWM; (c) Variable Off-time Modulation; (d) Variable On-time Modulation

Variable Frequency

Duty can also be controlled by keeping either the on-time or off-time constant while varying the other to control the overall duty (Figures 2.3c and 2.3d respectively). The overall period, hence operating frequency, of the converter varies with the operating duty. As operating frequency is dependent on loading and circuit parameters, synchronisation to an external component (such as switched loads or paralleled converters) is impossible. When multiple converters are used in parallel, in order to provide greater output power, each converter will inevitably operate with a slightly different frequency, which results in low-frequency beat harmonics which are difficult to filter [6]. It is also more difficult to design adequate transformers, EMI and output filters for converters which operate with a wide frequency range.

There is an additional variable t_{on} and variable t_{off} hysteretic control scheme [7]. The on-and off periods are determined by sensing the output voltage ripple. The switch is turned on when the output voltage falls below a preset voltage and turned off when it rises above the upper preset limit. This form of control offers very fast response to transient load changes, but as there is no restriction as to how long a switch can remain turned on, it is not suitable for converters which may experience short-circuits on their outputs.

2.1.3 Current Conduction Modes

A switched mode converter usually operates in either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM). This refers to whether the current in the main inductor, during steady state, goes to zero during a switching period. Figure 2.4 shows the three possible current waveforms for the main inductor.

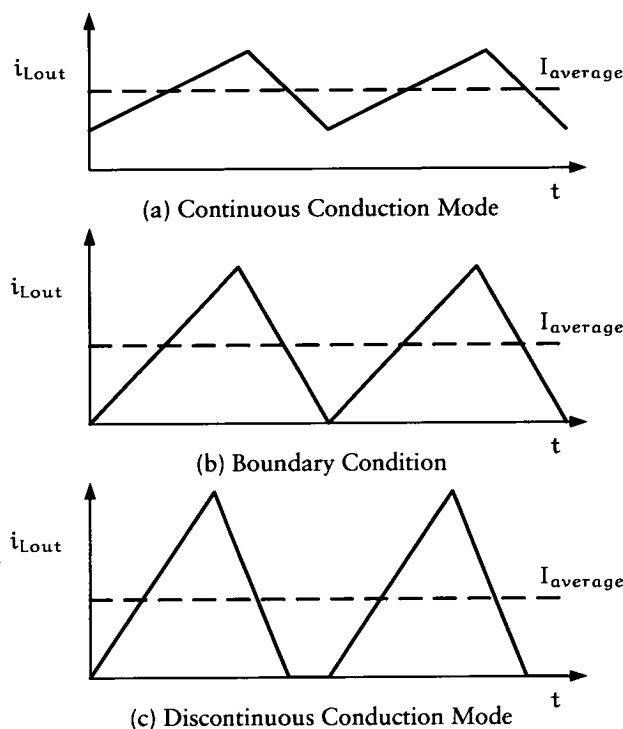


Figure 2.4: Current Waveforms for Different Conduction Modes

Most converters are designed to operate exclusively in a single mode, although this is not always possible due to load changes.

Continuous Conduction Mode

In CCM (Figure 2.4a), the inductor current does not fall to zero during the switching cycle. As a result, it requires a minimum value of inductance to limit the current ripple to keep the inductor current waveform above zero for the minimum load current. The inductor current starts and ends at a non-zero current during a switching period.

Converters operating in CCM generally operate with lower peak current stress, as the peak current during each switching cycle is less than twice the averaged output current, $I_{average}$. This is due to the use of a larger value of inductance for the main inductor which limits the rate of current rise and fall during each cycle. As a result, the output current ripple is lower thus requiring a lower value of C_{out} to achieve the required output voltage ripple. On the negative side, the large inductance

together with the output capacitor produce a second order characteristic which is more difficult to stabilise.

If the inductor current starts at zero and only falls to zero only at the end of the switching period, it is defined to be at the Boundary Condition (BC) (Figure 2.4b), which is the transition point between CCM and DCM.

Discontinuous Conduction Mode

In DCM, the inductor current falls to zero during a switching period and carries no current for a short period of time before the next switching cycle begins.

A main benefit of operating in DCM is good closed loop response from the converter [8]. The average inductor current can be changed quickly from cycle to cycle since the start and end current values are always zero enabling the converter to respond quickly to line voltage and load current changes.

DCM operation suffers from disadvantages such as high peak currents and poor open loop load regulation. Higher peak currents result in increased resistive losses due to higher Root-Mean-Square (RMS) currents, placing an increased demand on the output capacitors for output ripple filtering. As most converters require regulated outputs, feedback is used and so a converter's open loop performance is less significant.

2.1.4 Types of Switching

Ideally, a MOSFET should conduct no current when switched off, have no voltage drop when on, and have an instantaneous transition when switching. However, real MOSFETs carry leakage currents (though insignificant), experience voltage drops due to internal resistances and take a finite time to switch.

Hard Switching

During switching transitions, the overlap of the current and voltage waveform across the Drain-Source terminals of the MOSFET results in power loss occurring every time it is switched (Figure 2.5). Power loss thus is proportional to the switching frequency. Switching frequency is therefore limited by the maximum operating temperature of the switch. Components operate with a better reliability when not stressed either electrically with high voltages or currents, or mechanically, with extreme temperatures or physical shocks. (An accepted 'rule-of-thumb' for electronic components is that Mean Time Between Failure (MTBF) is halved for every 10°C rise in temperature.)

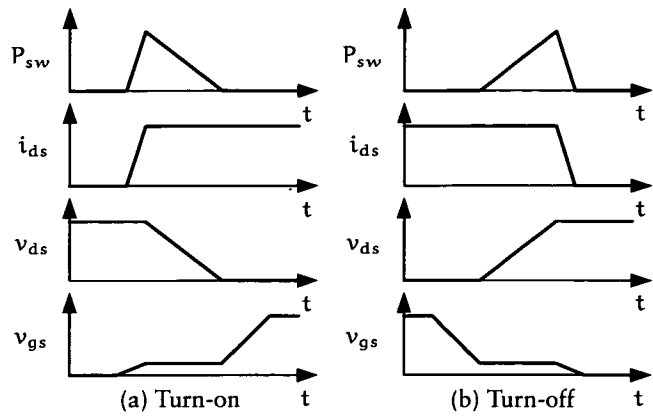


Figure 2.5: Typical MOSFET Hard Switching Waveforms

Soft Switching

To reduce losses caused by the switching action during each cycle, converters can be designed with switches which undergo soft switching. These converters are designed to have the switches switched when either voltage or current is zero. In doing so the power loss (the product of voltage times current) at switching is reduced to a minimum. A common way of achieving this is to use resonant converter topologies which utilise inductive and capacitive components which resonates with each other to bring the voltage or current to zero naturally before switching occurs.

There are two types of soft switching: Zero Voltage Switching (ZVS) and Zero Current Switching (ZCS).

Zero Current Switching (ZCS)

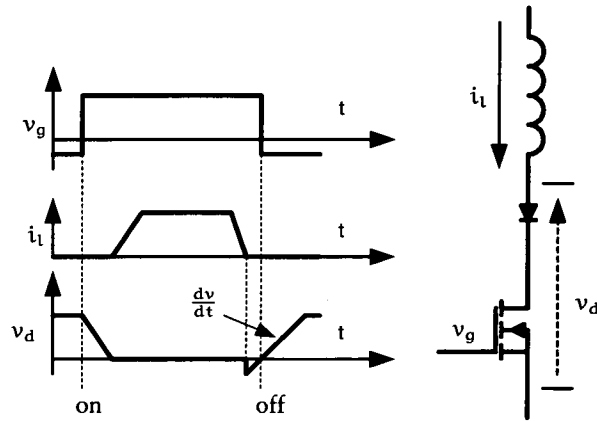


Figure 2.6: Simple ZCS Circuit and Waveforms

In Figure 2.6 [9], when the switch turns on, the inductive load limits the rate of current rise while V_d falls to zero, reducing turn-on losses. The switch is turned off

when the current has dropped to zero and is switched on with a zero current. This provides the switch with a lossless turn-off. However, when the MOSFET is switched on, energy stored in the switch capacitance is lost. This is known as charge dumping. Power loss due to charge dumping becomes significant when MOSFETs with large die sizes are operated with a high drain-source voltage, V_{DS} , and at a high switching frequency.

ZCS is particularly suitable for high power converters utilising IGBTs which suffer from a turn-off tail current that increases with temperature, thus, limiting its operating at high frequency. ZCS is used mainly to reduce turn-off losses and there are converters which combine both zero voltage and zero current switching techniques (ZVZCS).

Zero Voltage Switching (ZVS)

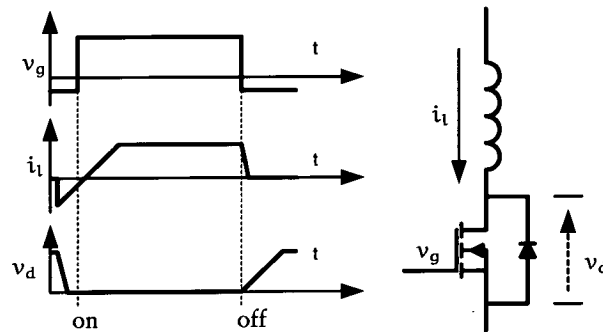


Figure 2.7: Simple ZVS Circuit and Waveforms

In Figure 2.7 [9], current is flowing in the negative direction when the switch is off, forcing zero volts across the switch. The switch is then turned on with no switching loss. As the switch is turned on at zero volts, ZVS switches do not suffer from charge dumping loss and are able to switch at higher frequencies compared to ZCS switches. However, there is usually a significant amount of current flowing within the switch, required for forcing the voltage to fall to zero prior to turn-on, which results in increased conduction losses for the switch. The ZVS switch would still undergo a lossy turn-off, although these turn-off losses can be minimised by using high-current MOSFET drivers which reduce the duration required for the MOSFET to turn-off, which in turn reduces turn-off switching losses. Fortunately, as the switching frequency is increased, the savings gained from switching related charge dumping loss still outweigh that of the increased conduction loss and therefore ZVS is still preferable over ZCS at high switching frequencies.

2.2 Resonant Topologies

This section introduces the resonant topologies that are used in high frequency converters, namely the load resonant type converters, the quasi resonant converters and the phase shifted bridge converters.

2.2.1 Load Resonant Converters

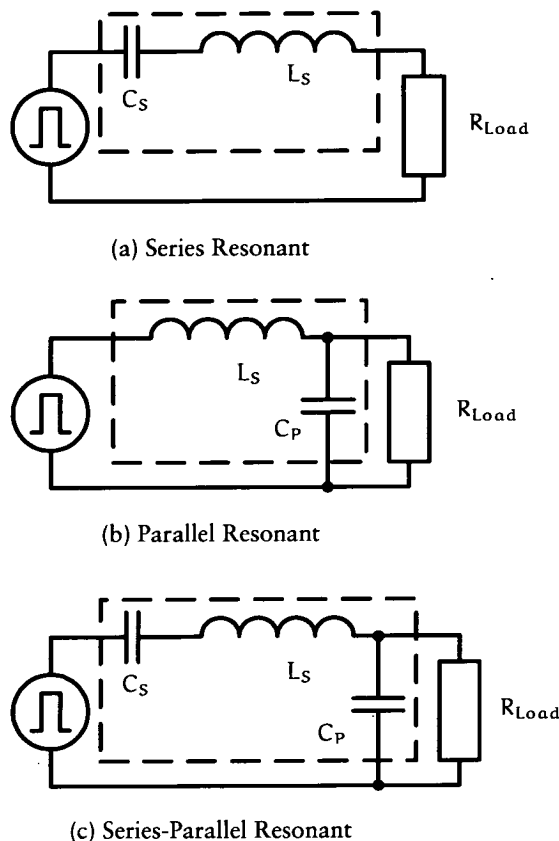


Figure 2.8: Generic Resonant Mode Loading

Load resonant converters can be implemented in various bridge topologies: for example, Half Bridge, Full Bridge *etc.* These generally consist of a resonant network of capacitors and inductors located between the legs of the bridge which impresses an AC pulsed waveform on the network (represented by the AC source in Figure 2.8). The pulsed voltage input to the resonant network forces the components to resonate and allows the switch to either turn-on with ZVS (when the switching frequency is greater than the natural frequency of the resonant components) or turn-off with ZCS (when the switching frequency is lower than the resonant components' natural frequency) [10]. Due to the nature of the resonating waveforms, the switches experience either greater current or voltage stress when compared to conventional PWM converters.

Most load resonant converters operate with variable frequency control which makes it difficult to provide adequate filtering as mentioned in Section 2.1.2.

LRC are commonly used in HV applications due to the ability to integrated the large leakage inductance value of the high voltage transformer into the resonant tank of the converter. This large leakage inductance usually limits the use of PWM type converters in HV application as the leakage inductance causes a 'duty loss' during the interval when the transformer primary current is resetting.

Series Resonant Converters

The SRC operates with a wide frequency range in order to provide regulation for a wide range of output loads [10]. Applications should not have to operate with no load connected [11] due to the series connection of the transformer. Various control methods exists which gives the SRC inherent output overload and short-circuit protection [12]. Series resonant converters suffer from high current stress and conduction losses when operating with a high input voltage and has low efficiency as a result.

In [10], the Series Resonant Converters (SRC) is found to be best suited for use in high voltage, low current application with a relatively narrow input voltage range due to the high output ripple current of the converter, thus requiring a large output filter capacitor. However, performance of the SRC is degraded by the parasitic winding capacitance of a transformer, lowering the output voltage and current of the converter [13]. Compensation by using a larger resonant tank capacitor, requires a large value of capacitance and results in a unnecessarily low resonant tank and switching frequency. Therefore the SRC is not as ideal as the next two resonant converter for use in a high voltage application.

Parallel Resonant Converters

In contrast to the SRC, the PRC is able to operate without any load as the size of output load does not affect the switch current much [13], due to the parallel location of the output load. Unfortunately, this results in a poor low load performance as switch losses remain high even though output demand is low. Parallel resonant converters are found to be best suited for low voltage high current applications, again with a narrow input voltage range [10] when used with an inductive output filter as the output current ripple was much lower than the SRC. However, this advantage is not present if a capacitive output filter is used instead.

PRC have generally been regarded as short-circuit-proof due to the fact that the amount of energy delivered to the output is predetermined by the impedance of the

resonant tank. However, as the converter is usually operated in a variable frequency mode at a switching frequency above the natural resonance frequency of the resonant LC tank, to minimise the physical size of the magnetic components, the control circuitry lowers the frequency to increase the output current when the output voltage drops. In the case of a short-circuit, the converter will be unable to maintain the output voltage and frequency will drop below the natural frequency of the resonant tank forcing it into positive feedback. Although the output power will reduce, the current in the primary side will continue to rise with the lowering of frequency. It is therefore necessary to limit the lower switching frequencies to limit the short circuit currents.

[14, 13] the full bridge parallel resonant converter with a capacitive output filter is analysed in detail and compared with other resonant converters. This topology has low losses at high output loads and can operate with frequencies that go up into the hundreds of kilohertz range. The parasitic leakage inductance and winding capacitance of the transformer are put to good use, forming the resonant LC tank, along with the output bulk capacitors. Due to the better utilisation and integration of the of the transform's winding capacitance, the PRC is better suited for high output voltage applications, operating with the highest switching frequency and lowest inductor current.

In [15], the phase shifting technique was applied to the Parallel Resonant Converter (PRC) with a capacitive output filter for an X-ray Generator, making use of the parasitic capacitance in the transformer and output cables. Utilising the phase shifted method of PWM control, constant switching frequency is attained but as a LC resonant circuit is used, both leakage inductance and parasitic capacitance have to be designed to achieve the required output power and switching frequency requirements. [16] improves on this topology by adding additional resonant poles to each leg of the full bridge as auxiliary circuits to provide zero voltage switching for all switches.

Series-Parallel Resonant Converters

This converter combines the positive features of both the SRC and PRC converters, by being able to operate with no loads like the PRC, while having better low load efficiencies like the SRC. With a careful selection for the values of resonant components, the effects of C_P is negligible when the output load is high, making the converter resemble a SRC, and when the output load is low, C_P dominates, making the converter resemble a PRC instead. As with the other resonant converters, it is a variable frequency switching converter, and dependent on the values of the transformer parasitics and output loading. The series-parallel resonant converter integrates the transformer winding capacitance into its operation and hence avoids the capacitance's negative effects as faced by the SRC. C_S when properly rated also functions as a DC blocking

capacitor which prevents the transformer from saturating when operating with voltage mode control. However, as with the PRC converter, the transformer will be more difficult to design and manufacture to the specifications required as the converter now depends on both its parasitic inductance and capacitance for normal operation. This is especially true if the converter uses the parasitic components solely without any discrete resonant components.

[17, 18, 19] describe a hybrid series-parallel resonant converter utilising both transformer parasitic capacitance and leakage inductance together with the transformer DC blocking capacitor to create a high voltage, high power, full bridge, clamped mode LCC type Parallel Resonant Converter with capacitive output filter.

The use of various resonant converters for a high voltage medical X-ray power supply have been previously investigated [20]. It is found that the choice of converter type depends very much on the loading and power demand which the X-ray equipment requires. The series parallel resonant converter is particularly suitable for such an application due to its ability to supply the required power at the various output loads.

2.2.2 Quasi Resonant Converters

In Quasi Resonant Converters (QRCs), the current and voltage waveforms of the switch are modified using a high frequency LC resonant network to reduce switch losses while transferring energy to the output similar to resonant converters. Any single-ended PWM topology can be modified to obtain its ZCS-QRC or ZVS-QRC variant by replacing the PWM with a resonant switch instead (*e.g.* Figure 2.9), the addition of a resonant capacitor, inductor and a free-wheeling diode [10, 21].

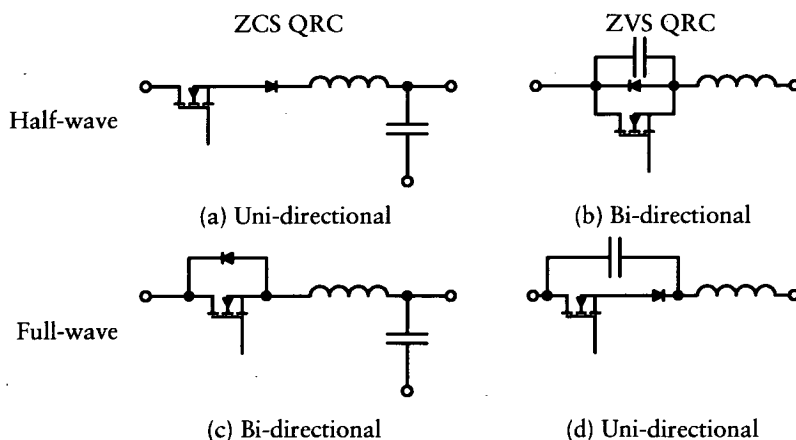


Figure 2.9: Various Resonant Switch Replacement Configurations for QRCs

Other configurations of the resonant switch are possible [10, 21] and the leakage inductance of the transformer (if present) can be used as the resonant inductor if the

resonant capacitor is placed on the secondary of the transformer, thus lowering component count and costs. The use of the leakage inductance also improves efficiency as a discrete inductor on the primary side is usually subjected to high voltages and currents leading to increased losses.

QRCs generally operate with variable frequency control with ZCS QRCs using fixed on-time control and ZVS QRCs using fixed off-time control. QRCs can operate in either a full-wave or half-wave mode depending on the type of switch used. Half-wave and full-wave operation QRC converters differ in the amount of circulating energies available for soft switching. Half-wave converter ZCS QRC converter circulate less energy and thus have a higher efficiency. Their DC gains also differ, with half-wave QRCs more sensitive to load changes, such that a wider range of operating frequencies is required. The upper limited of switching frequencies for ZCS QRC converter is still limited by the inherent charge dumping problem which plagues ZCS converters. Thus, the ZCS QRC is particularly suitable for low input voltage and high output voltage applications where the charge dumping problem is minimised and transformer leakage inductance is used as the resonant inductor. ZVS QRCs are limited in their application due to the high voltage stress on the switch which limits the operation to low input voltages and a limited out load range. In addition, due to the lack of high frequency uni-directional switches, the full-wave ZVS QRC can not be implemented [10].

2.3 Phase Shifted Bridge Converters

2.3.1 PS-PWM-ZVS-FB Converter

There are several ways of performing the phase shifting in order to achieve various forms of soft switching for the Bridge converter. [22] shows nine ways of modulating the driving waveforms to the Bridge MOSFETs while maintaining the same ideal voltage waveform between the midpoints of each leg of the H-bridge. Depending on which modulation scheme is used, the resulting converter could be a hard-switched, ZVS or ZVZCS converter.

In [23, 24] Steigerwald compares experimentally several 100 kW soft-switching converters against the standard full bridge converter. He shows that the efficiencies for the soft-switching converters did not differ by more than 2%. Though the active auxiliary resonant commutated bridge had the lowest relative weight of the magnetic components, and highest efficiency, its design was complicated by having to control the additional auxiliary circuits for the provision of soft switching to the MOSFETs. Steigerwald considered the phase shifted bridge to have the best balance of relative weight of the magnetic components, efficiency and simplicity of control.

Theory of Operation

As can be observed in Figure 2.10, the conventional PS-PWM-ZVS-FB converter operates by driving all four MOSFETs at near 0.5 duty. MOSFETs TA and TB are known as the lagging leg as their driving waveforms are delayed with respect to their diagonally opposite counterparts, MOSFETs TD and TC, which form the leading leg.

The time delay between the v_{gs} waveforms of MOSFETs on either the top (Delay_{AC}) or bottom (Delay_{BD}) of the bridge determines the duty, d , of the voltage waveform, (Equation 2.1) between the midpoints of the H-bridge where the transformer is located.

$$\begin{aligned} \text{Delay}_{AC} &\approx \text{Delay}_{BD} \\ d &= \frac{\text{Delay}_{AC}}{T_{0.5}} \end{aligned} \quad (2.1)$$

From the waveforms in Figure 2.10, it can be seen that power is transferred from the primary to the secondary of the transformer when diagonally opposite MOSFETs are conducting. This is known as the active or power transfer interval. When two MOSFETs on either the top or the bottom half of the bridge are conducting, current will freewheel in that half of the bridge without transferring power to the secondary. This is known as the passive or freewheeling interval.

Although the H-bridge can be divided into leading and lagging legs, it can cause confusion at times as to which MOSFET the phase lead or lag is referenced to. It can be observed that whenever MOSFETs TA or TB switch on, the converter goes from a passive state to an active state of operation. Conversely, whenever MOSFETs TC or TD switch on, the converter switches from an active to passive state. Thus, MOSFETs TA and TB are described as being in the passive-active (PA) leg of the phase shifted bridge and MOSFETs TC and TD in the active-passive (AP) leg of the converter. There is a need to differentiate between the two legs of the bridge so that the delay timings for each MOSFET can be appropriately set, as the amount of stored inductive energy available for soft switching of the MOSFETs on each leg is different.

Slew Interval (t_0 - t_2)

The slew interval begins when TB is switched off. i_{pri} flowing in a negative direction in the transformer leakage inductance is now forced to flow through the body diode of TA back into the supply. TA is then switched on. During this interval, the voltage imposed on L_{pri} forces the current, i_{pri} , to change its direction of flow. Power is not transferred to the secondary as i_{pri} reflected to the secondary is less than the circulating current in L_{out} . The slew rate is determined by Equation 2.2 and the

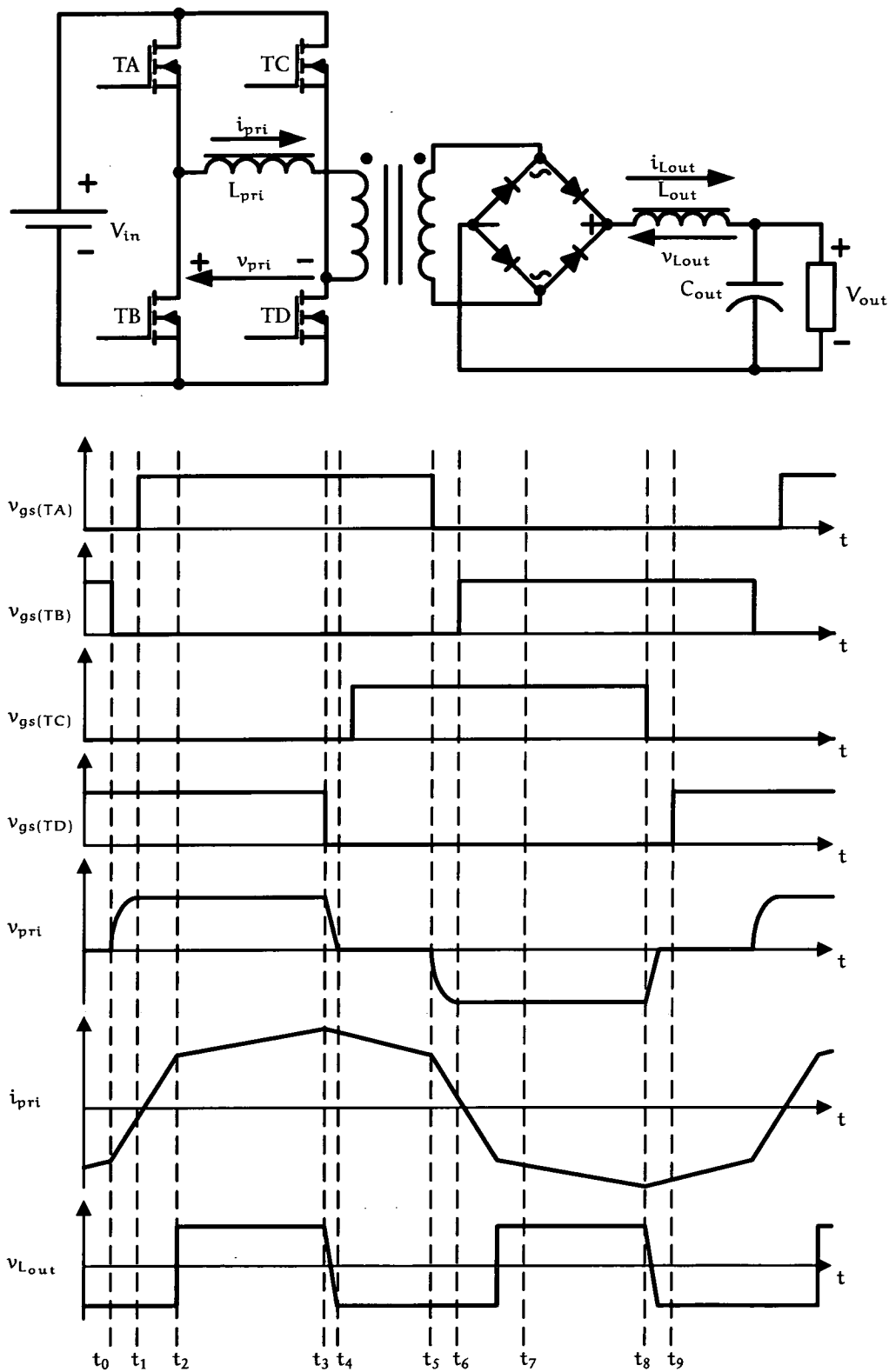


Figure 2.10: Schematic and Waveforms for PS-PWM-ZVS-FB Converter

duration of the slew interval depends on the load current (Equation 2.2) [25].

$$\frac{\Delta i_{pri}(t_0 t_2)}{t_2 - t_0} = \frac{V_{in}}{L_{pri}} \quad (2.2)$$

where

$$\Delta i_{pri}(t_0 t_2) = i_{pri}(t_2) - i_{pri}(t_0) \quad (2.3)$$

$$t_2 - t_0 = \frac{\frac{N_s}{N_p}}{\frac{V_{in}}{L_{pri}}} (2I_{out} - \frac{V_{out}}{L_{out}} (1 - d) T_{0.5}) \quad (2.4)$$

Active Interval (t_2 - t_4)

The active interval starts when i_{pri} reflected to the secondary equals the circulating output currents. During the active interval, power is being transferred from the input to the output of the converter. Currents in both L_{pri} (Equation 2.5) and L_{out} rise as the inductors are charged during the active power transfer interval. The end of the active interval occurs after TD is switched off and v_{pri} has fallen to zero.

$$\frac{\Delta i_{pri}(t_2 t_4)}{t_4 - t_2} = \frac{V_{in} \frac{N_s}{N_p} - V_{out} \frac{N_s}{N_p}}{L_{out}} \quad (2.5)$$

Passive Interval (t_4 - t_5)

During the passive interval, no voltage appears across v_{pri} . Current stops flowing from the input supply and no power is transferred to the converter while i_{pri} continues to circulate through TA and TC. During this interval, i_{pri} (Equation 2.6) is a reflection of $i_{L_{out}}$ across the transformer and therefore has a negative gradient. When TA is switched off, the passive interval terminates and the other half of the switching cycle (t_5 - t_9) begins.

$$\frac{\Delta i_{pri}(t_4 t_5)}{t_5 - t_4} = \frac{-V_{out} \frac{N_s}{N_p}}{L_{out}} \quad (2.6)$$

Active-Passive Transition Interval (t_3 - t_4)

The active-passive (AP) transition interval occurs at the end of the active interval, after TD is switched off. During this interval, energy stored in L_{pri} and L_{out} will

keep i_{pri} flowing and charge TD's C_{oss} while discharging TC's C_{oss} , bring v_{pri} to zero and end both the active and active-passive transition intervals. Energy stored in L_{out} assists with providing ZVS for the AP leg because the output current flowing in L_{out} is reflected back to the transformer primary. As the converter is usually operated in CCM and the value of L_{out} is designed to be large enough to maintain operation in CCM, ZVS will be achieved under most conditions as the stored inductive energy is much greater than the stored capacitive energy [25]. Therefore, the time required to achieved ZVS can be approximated by the linearised Equation 2.7. During this interval, energy stored in the inductance has also to discharge energy stored in the transformer winding inter-turn capacitance, C_{dist1} .

$$t_4 - t_3 = \frac{V_{in}(C_{CD} + C_{dist1})}{i_{pri}(t_3)} \quad (2.7)$$

Passive-Active Transition Interval (t_5 - t_6)

After TA turns off, the remaining level of current $i_{pri}(t_0)$ flowing in L_{pri} resonates with the output capacitances of MOSFET TA and TB, C_{AB} . As the current in L_{out} is no longer reflected back to the primary during this interval and transformer current has fallen during t_4 - t_5 , the amount of energy available to achieved ZVS is reduced. The resonating waveforms can no longer be assumed to be linear and the drain-source voltage of TB, $v_{ds(TB)}$ is described by Equation 2.8 (derived from equations 9.1 – 9.8 in [26]).

$$v_{ds(TB)}(t) = Z_{AB} i_{pri}(t_5) \sin \omega_{AB}(t - t_5) \quad (2.8)$$

where

$$\omega_{AB} = \frac{1}{\sqrt{L_{pri} C_{AB}}} \quad (2.9)$$

$$Z_{AB} = \sqrt{\frac{L_{pri}}{C_{AB}}} \quad (2.10)$$

The duration of the PA transition interval should be set to a quarter of the resonant frequency (Equation 2.11) as this ensures that switching losses are reduced even if ZVS is not achieved during low loads, while still maintaining ZVS during normal operation (Figure 2.11) [25].

$$t_6 - t_5 = \frac{\pi}{2} \sqrt{L_{pri} C_{AB}} \quad (2.11)$$

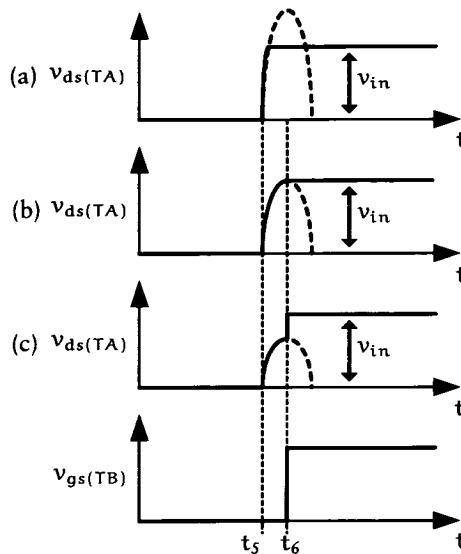


Figure 2.11: Various PA Leg Resonant Transition Waveforms. (a) High Loads; (b) ZVS Critical Load; (c) Low Loads

Improvements

A potential problem with the PS-PWM-ZVS-FB converter is the loss of ZVS for the MOSFETs when operating on light loads. Many ways have been attempted to extend the range of operating conditions while maintaining soft switching.

Auxiliary circuits have been placed on both the primary side and secondary side of the high frequency transformer. The use of the current doubler rectifier on the transformer secondary has reduced the significance of these circuits as it can enable the PS-PWM-ZVS-FB converter to work with soft switching even at no load.

[27] added an auxiliary inductor and two MOSFETs to the PS-PWM-ZVS-FB converter to modify it to a Zero-Voltage-Transition (ZVT) converter. As the auxiliary circuitry is active, the amount of circulating energy has been reduced, while being able to maintain soft switching. However, the control circuitry becomes more complex which is undesirable.

Saturable inductors, placed in series with the transformer, are used to replace additional supplementary inductors [28, 29, 30, 31]. The reason for this is that large inductances in series with the transformer (leakage or otherwise) reduced the effective duty ratio in CCM, as the current carried by the series inductance changes direction of flow in each half cycle, during which power is not actively being transferred to the secondary of the transformer. Saturable inductors act as inductors at low current:

having stored the maximum amount of energy possible by the inductor, it saturates and loses its inductive behaviour. Therefore, designers could set the amount of energy stored in the series inductance to the minimum amount required by the circuit to perform soft switching, but not so high as to significantly rob the converter of duty at high loads. This has been used both on the primary side of the transformer [29, 30] and on the secondary [31]. Unfortunately, by the very nature of saturable inductors, lacking inductive properties at high currents, they are not useful in a converter which depends on the inductance present in the circuit to limit short-circuit currents.

[32] introduces the use of an auxiliary inductor with two diodes to the basic PS-PWM-ZVS-FB Converter. This is used to ensure that a minimum amount of inductive energy will be circulating in the circuit to perform the soft switching operation.

[33] improves on this auxiliary circuit by placing it on the secondary side of the full bridge while utilising the magnetising current to assist in the provision of inductive soft switching energy. This enables the designer to reduce reliance on a large leakage inductance as this reduces the effective duty ratio of the circuit.

Even resonant converters have used auxiliary circuits to improve efficiencies when operating above the resonant tank frequency to provide ZVS [34].

For converters requiring higher output power, utilising IGBTs, the turn-off losses usually limit the switching frequency of the converter. The phase shifted bridge has been modified in [27, 35, 36] to accommodate ZCS and ZVS hybrid switching to reduce switching losses caused by the IGBT tail-end current. Active [29] and simpler passive [37, 38, 39, 40] auxiliary circuits have also been created for these converters on the secondary side. These help to reflect a voltage source back to the primary during the free-wheeling period instead of a current source, to quickly reduce the primary circulating currents such that a zero current condition occurs for the IGBT to soft switch. Such a technique has also been used for the MOSFET based PS bridge, not to provide ZCS, but to reduce the duty loss experienced by the converter due to the presence of a large resonant inductor when the converter undergoes a Passive-Active transition [41].

Current Doubler Rectifier

The current doubler rectifier circuit, Figure 2.12, first reported in as early as 1924 [42] is particularly useful for circuits with low output voltages and a wide range of output loads.

This circuit enables the soft switching to proceed even with no loads [43] as the current doubler rectifier circuit keeps the current flowing in the opposite direction even if the load decreases below the otherwise critical value for the standard output

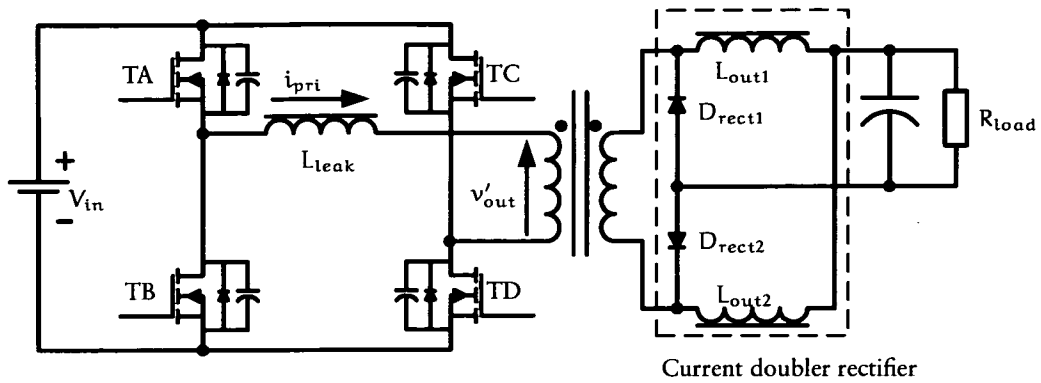


Figure 2.12: PS-PWM-ZVS-FB Converter with Current Doubler Rectifier

diode rectifiers. This is possible as the diodes do not prohibit the current in the output filter inductors from going negative during DCM operation as would be the case in a standard output rectifier circuit.

As the output inductors currents can be bi-directional, they do not go discontinuous, thus, converter gain is maintained from no-load to full load condition.

[44] uses the current doubler rectifier to increase the range of soft switching operation, but modifies the switching waveform to direct the circulating currents to only circulate in the lower bridge MOSFETs. In [45] synchronous rectification was used along with the current doubler rectifier to increase the efficiency further. [46] modified the PS-PWM-ZVS-FB converter in an attempt to increase efficiency and extend the soft switching range by operating the full bridge close to maximum duty ratio with no phase shifting. Two of the secondary rectifier diodes are replaced by MOSFETs which are driven with a phase shift referenced to the bridge MOSFETs to control the output duty. This is a hybrid of the Active Resonant Commutated Pole (ARCP) Converter and Dual Active Bridge (DAB) Converter as specified in [24], using two additional inductors to provide soft switching to the bridge MOSFETs. [47] used this idea and incorporates it into the standard PSB to provide soft switching for the PA Leg of the MOSFET to improve efficiency, while maintaining the benefit of [46] not having to add additional inductance in series with the transformer which reduces the effective duty.

2.3.2 PS-PWM-ZCS-FB Converter

Recently, it has become necessary for off-line power supplies to include some form of power factor correction in the circuit. One possibility is to create a two stage converter by using a Boost converter as a pre-regulator to the Bridge converter to provide PFC [48]. Another method of achieve PFC with a FB converter is to operate the FB in a boost manner, moving the output inductor to before the bridge MOSFETs. To improve efficiencies, active clamps are used to provide ZVS/ZCS to the MOSFETs

[49, 50].

Just as with the conventional full bridge converter, a dual version of the Phase Shifted Full Bridge converter exists, which operates with the inductor located in the primary before the full bridge instead of the secondary [51]. This converter operates with a zero current switching scheme to achieve soft switching. It uses an input DC inductor located between the bridge and input supply operating in a boost manner where the driving signals to switches are $>50\%$ and thus overlap. During this overlap sub-period, the input inductor is charged up and the energy later released in the full bridge to be transferred to the output. However, as with most converters employing the ZCS soft-switching scheme, the switching frequency is limited due to the dumping of stored charge in the MOSFET C_{oss} at every switching cycle. It also suffers from duty loss during the resonant sub-period (between the leakage inductance and parasitic capacitance) due to the time taken to charge and discharge the parasitic capacitance.

If IGBTs are used instead of MOSFETs, due to the large tail current during turn-off, it is preferable to use a ZCS soft switching technique to reduce the switching losses. [52] uses auxiliary circuits on both sides of the bridge to achieve ZCS for all MOSFETs.

2.4 High Voltage Application Voltage Step Up Techniques

In high voltage applications, the choice of voltage step up technique depends on the output power requirements. For simple mass produced applications such as television and other Cathode Ray Tubes (CRTs), a simple Flyback converter is often used as it is cost efficient. The transformer and inductor are combined allowing for a reduction in the number of components while still providing isolation for safety. In addition, the Flyback converter is particularly suited for use in analogue television as the sawtooth waveforms produced are used by the circuit to scan across the screen.

For high-powered applications, other voltage step up techniques include using either a Cockcroft-Walton Multiplier or a transformer based solution.

Cockcroft-Walton Multiplier

The Cockcroft-Walton voltage multiplier is a low cost means of stepping up and rectifying an AC voltage. It consists of capacitor and diode rectifier stages as shown in Figure 2.13. The output voltage could theoretically be stepped up infinitely, using n number of diode and capacitor stages to step up the input voltage by n times. However, the output voltage regulation suffers and it takes longer to charge the rectifier

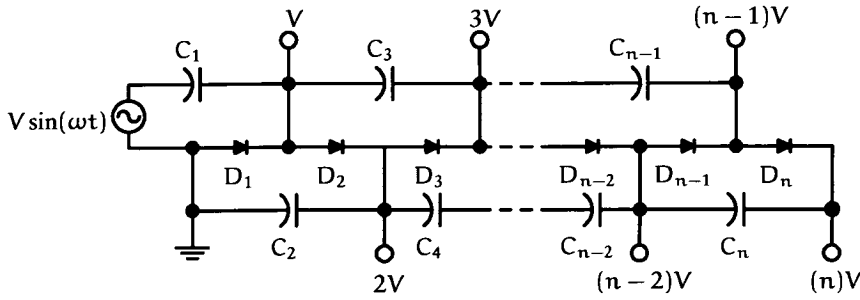


Figure 2.13: Cockcroft-Walton Voltage Multiplier

up to the required output voltage as the number of output stages is increased [53]. Therefore, the Cockcroft-Walton voltage multiplier is not suitable for use in a sensitive application such as a TWT radar power supply. Nevertheless, to this day the Cockcroft-Walton circuit is often still used to supply a high voltage at the injector stage of large particle accelerators and as rectifiers for X-Ray power supplies.

Multiple Secondaries

In high powered applications, transformers are often used to provide the voltage step up as well as the isolation requirements. In mission critical systems, such as defence and aerospace equipment, it is also often required to have multiple power converters to either provide greater output power while maintaining high reliability or for backup purposes. Depending on the power requirements and redundancy requirements, the converter may be designed in three ways [54]:

1. Single primary, multiple secondaries (Figure 2.14a)
2. Multiple primaries, multiple secondaries (Figure 2.14b)
3. Multiple converters, multiple primaries, multiple secondaries (Figure 2.14c)

The benefit of the converter in Figure 2.14a is its simple design. It is small and light as only a single transformer is required. The converter may have multiple outputs at each stage of the rectified outputs, which is useful for TWT radar requirements, though these are not directly regulated. The power transfer capabilities of Figure 2.14a is limited, as with an increase in power, the transformer losses start to increase. To increase the amount of power available to the load, the converter in Figure 2.14b transfers its power using several transformers to maintain a suitable temperature gradient across the insulation to maintain reliability. For true versatility, the modular system in Figure 2.14c may be used, whereby output voltage and power is only limited by the high voltage insulation and the output impedance of the AC source.

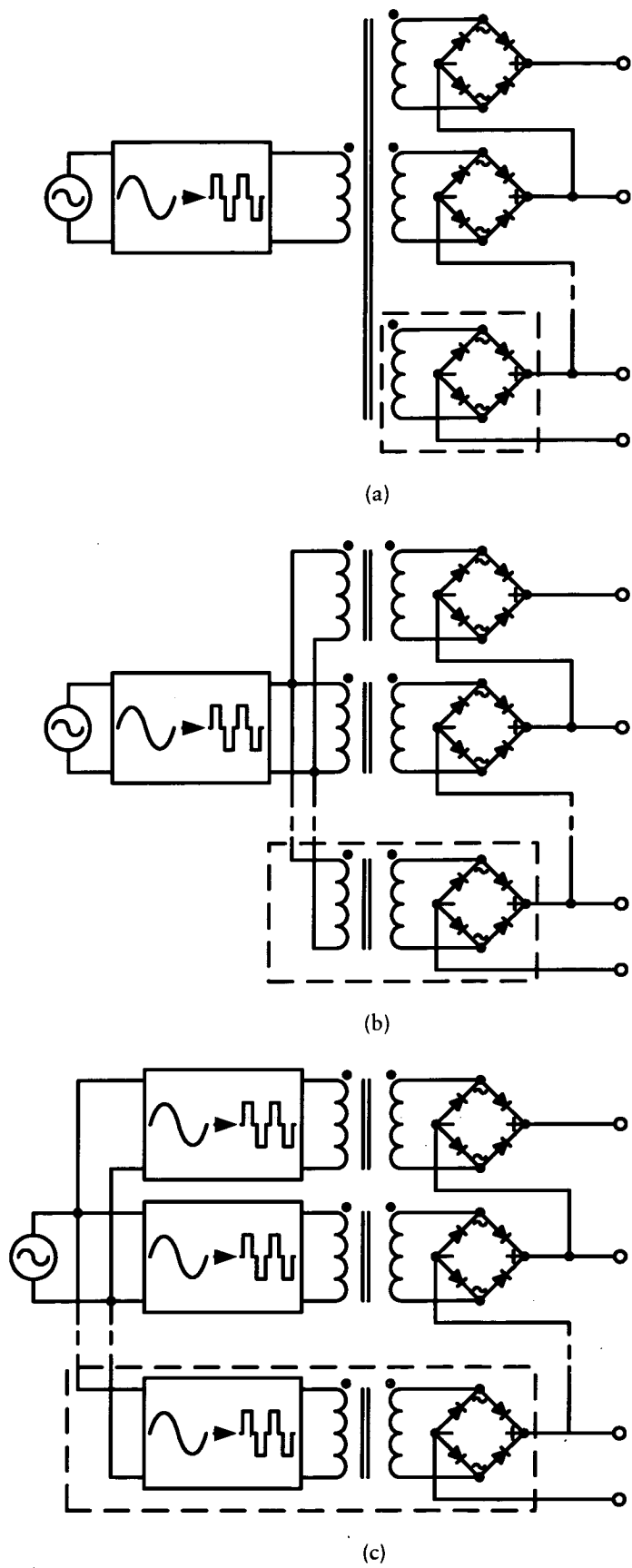


Figure 2.14: Various High Voltage Transformer Configuration

2.5 Chapter Summary

Chapter 2 presents some of the basic converter topologies along with how output voltage control is achieved and the different current conduction modes in which a converter can operate. The principle of hard lossy switching and soft lossless switching is introduced. Soft switching converters can be achieved using zero voltage switching and/or zero current switching techniques. Zero current switching techniques tend to be more suitable for converters using IGBTs due to the natural tail current during switch off. However, the use of ZCS techniques at high frequencies are limited due to energy stored in the MOSFET's output capacitance being dumped each time the MOSFET turns on. Lossless soft switching allows for higher switching frequencies and a reduction in the physical size of magnetic components while maintaining high overall efficiency. A brief description and advantages and disadvantages of various topologies which utilise soft switching to achieve higher efficiencies included: resonant, quasi resonant and resonant switch converters. The Phase Shifted Pulse Width Modulation Zero Voltage Switching Full Bridge converter achieves zero voltage soft switching by phase shifting the simple 0.5 duty driving waveforms of the left and right leg of the bridge. Phase shifting directly controls the pulse width modulation of the transformer voltage waveform. The energy stored within the leakage inductance of the transformer is transferred to/from the MOSFET's output capacitance during the switching transition between MOSFETs on the same leg of the bridge. This elegant design utilises two parasitic components, which would otherwise reduce efficiency and lower switching speeds, to resonate with each other to achieve soft switching. In the conventional phase shifted bridge converter, there must be a minimum output load for zero voltage switching to occur. Auxiliary circuits have been developed to assist ZVS and improve efficiency when operating at light loads. Due to market demands, development of the phase shifted bridge converter has been concentrated on the lower voltage high current output configuration.

To achieve the voltage step up, a single primary converter with a single transformer primary winding with multiple rectified stacked secondaries is a simple and economic solution and is sufficient for the current application.

Chapter 3

Airborne TWT Radar Power Supplies

3.1 TWT Radar Introduction

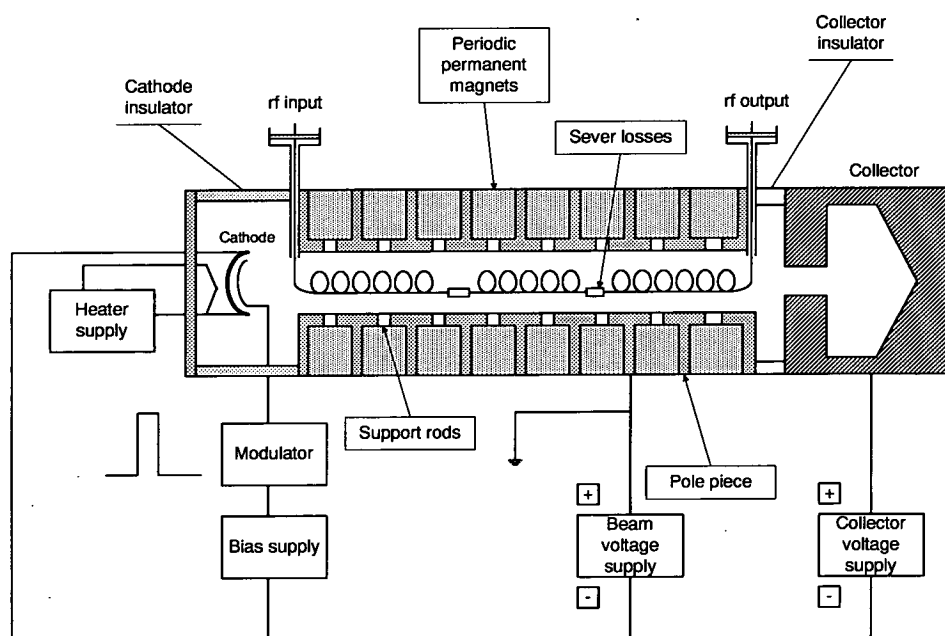


Figure 3.1: Cross Section of TWT Radar

A cross-section of a TWT Radar is shown in Figure 3.1 (Provided by Mr Frank Fisher of BAe Systems). The TWT radar can be operated in either continuous-wave mode or pulsed mode. A CW radar emits radio waves continuously and is used for measuring moving objects using the principle of Doppler frequency shift. In a Frequency Modulated Continuous Wave radar, the frequency of the transmitted signal is continuously

being modulated to enable the return signal to tell the time taken to reach the object and therefore its distance.

Most radars are of the pulsed mode variety where high energy, short duration pulses of Electromagnetic (EM) waves are transmitted repeatedly. When the transmitter is not transmitting, the receiver listens for pulse reflections to determine the distance of the object by measuring the time taken for the pulses to travel back to the receiver.

Table 3.1 and 3.2 [55] shows a variety of TWT radars of various functions and different specifications. As the table shows, the electrical power requirements of a TWT varies from model to model. A typical TWT generates high frequency radio waves (0.25 GHz – 90 GHz), requires high voltage (-10 kV – -30 kV) and high powered (approximately 1 kW).

A pulsed TWT radar amplifies and outputs high power pulsed signals and thus has a pulse load profile (Figure 3.2). The radar power supply output voltage sags when an pulse output is initiated. This is typical of pulse loading as it demands a high peak output power, many times the average output power, in just a small duty cycle. However, the TWT radar load can still be approximated as a constant load if a sufficiently large output capacitor is used to store the energy required.

All TWTs possess four major sub-assemblies: an electron gun that produces a high density electron beam; a microwave slow-wave circuit that supports a travelling wave of electromagnetic energy with which the electron beam can interact; the collector that collects the spent electron beam emerging from the slow-wave circuit; and the TWT package, which provides points for attachment to the using system, provides cooling for power dissipated within the TWT, and, in some cases, includes all or part of the beam focussing structure. Other functions may also be included as required.

High energy pulses are required, as the pulse energy determines the maximum distance from which the radar can locate its objects. The Pulse Repetition Frequency (PRF) determines the maximum definition of the object. Due to high energy switching constraints and pulse delivery components with a limited recovery rate, PRF (and hence definition) is limited when maximum output power is required for locating distant objects. PRF typically ranges between 200 and 6,000 pulses per second (pps) while the duration of each pulse might range from 0.1 to 10 μ s.

The PRF of the system can vary in a given range dependent on the requirements of the radar application. At every frequency, the radar power supply must be able to recharge the output capacitors to the desired rated output voltage to within a few millivolts by the time the next pulse is initiated.

Although the peak power required for the TWT can go up to several megawatts, the average power required from its power supply is much less due to the short duration of the pulses, T_D , when compared to the rest duration. The average power

TWT Type	Model	Freq (GHz)	Power (kW)	Duty Cycle (%)	Cathode Voltage (kV)	Cathode Current (A)	Collector Voltage (kV)
Pulsed	L-5827	1.0–2.0	1.000	4.00	–7.7	2.100	5.8
Pulsed	L-5785	16.0–17.0	3.000	5.00	–11.0	2.300	8.6
CW	L-2086	1.8–3.6	0.500		–5.5	0.770	4.0
CW	L-5832	6.5–18.0	0.150		–10.3	0.270	5.5/3.4
Ring Loop	L-5714	2.1–2.6	20.000	0.01	–22.0	5.800	22.0
Ring Loop	L-5538	3.1–3.5	2.000	4.00	–7.5	1.500	5.5
Satellite Communications	L-5750	3.0–5.5	0.125		–4.7	0.017	2.8/1.4
Satellite Communications	L-5991	13.75–14.5	0.700		–12.6	0.440	6.6/5.1/1.9
Coupled Cavity	L-5630-50	8.8–9.3	17.500	1.60	–24.5	4.700	
Coupled Cavity	L-5649-02	16.1–16.9	45.000	0.13	–37.1	6.200	

Table 3.1: Some TWTs by Litton Electron Devices

Band	Frequency (GHz)	PRF (pps)	Pulse Duration (μ s)	Peak power	Range (nautical miles)	Typical Application
Ground						
50cm (P)	0.6	500	3	500kW	100	Air Traffic Control (ATC) – terminal area
50cm (P)	0.6	370	3	500kW	180	ATC – en-route
23cm (L)	1.2	600	2.5	2MW	100	ATC – terminal area
23cm (L)	1.2	350	4	2MW	180	Search and ATC – en-route
23cm (L)	1.2	3,600	3.5	5kW	200	Tertiary Radar (TACAN)
10cm (S)	3	250	2 or 5	2.5MW	250	Long range search
10cm (S)	3	250	4	2.5MW	250	Long range height-finding
10cm (S)	3	700	1	650kW	75	ATC – airfield approach
6cm (C)	5.5	300	5	1MW	120	Height finding
3cm (X)	9	3,279	0.18 (variable)	60kW	13	ATC – airfield approach (precision)
Airborne						
3cm (X)	10	800	0.5	175kW	46	Airborne search, navigation and bombing
		400	1	175kW	92	
		200	2	175kW	184	
3cm (X)	8.5	1,000	1	175kW	25	Airborne interception
3cm (X)	9	400	2	60kW	120	Cloud and collision warning
6cm (C)	4.3	10,000	0.035 – 0.125	5kW	1	Altimeter
7mm (Q)	45	3,800	0.15	50kW	5	Airborne reconnaissance and mapping
		1,900	0.15	50kW	10	

Table 3.2: A Selection of Typical Pulsed Radars

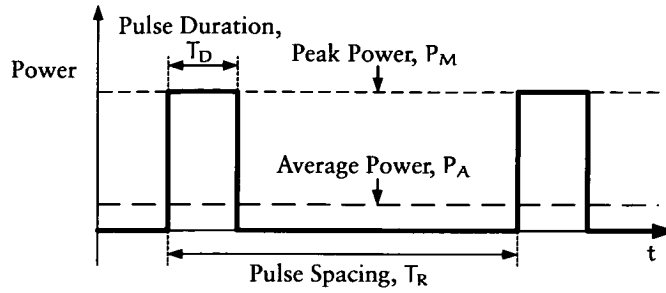


Figure 3.2: A Pulsed Radar Loading Waveform

requirements can be calculated using Equation 3.1.

$$P_A = P_M \cdot T_D \cdot \text{PRF} \quad (3.1)$$

The radar requires such high peak powers because only a fraction (typically a few picowatts) is returned to the receiver due to scattering. The high voltage power supply must be lightweight, minimum volume, reliable, contain as few components as possible, and operate over a wide temperature range. The power supply also requires adequate electrical insulation to prevent any electrical breakdown caused by high voltages present.

3.2 Problems with TWT Radar

Although the TWT radar is generally a rugged device, operation of the radar does occasionally present difficulties which must be considered for correct operation. TWT radars requires high voltages for operation but occasionally a HV arc occurs, also, the TWT which is a high-powered amplifier, suffers from noise problems which can degrade the quality of the received signals.

3.2.1 Spectral Purity of Signal

For the spectral purity of the transmitted radar signal to be high, EMI from the the radar power supply needs to low, thus the EM emissions need to be predictable and easily filtered. This is achieved by using a power supply with a predetermined switching frequency whose emitted EMI profile is known and filtered by a properly designed filter. Synchronising the switching waveforms of the radar's switched mode power supply to the pulse signals helps to reduce spurious noise within a pulse signal which would occur if the power supply was operating independently of the radar signal. By operating with a high switching frequency, the EM emission profile will be shifted up in frequency thus reducing the size of EMI filters. Use of low EMI

power supply configuration, such as the resonant and quasi-resonant power types, also helps reduce the complexity and size of the EMI filters. The inter-pulse voltage deviation is a critical criterion. Ripple on the TWT cathode voltage causes spurious phase modulations; these must be kept to a minimum by filtering the output of the HV power supply. The amount of phase shift caused by a voltage ripple can be determined by the pushing factor of the TWT, shown in Equation 3.2 [56].

$$\frac{\Delta\phi_l}{\Delta V_{\text{Cath}}} = -\frac{1}{3} \frac{\phi_l}{V_{\text{Cath}}} \quad (3.2)$$

where ϕ_l is total TWT phase length and V_{Cath} is cathode voltage.

Using Equation 3.2 the maximum allowable inter-pulse voltage ripple can be determined which gives a maximum phase shift. If exceeded, the degraded transmitted signal may show up as a false image on the receiver.

3.2.2 Arcing

A TWT may fail from electrical breakdown due to the high voltages present within the tube. As seen from the approximate breakdown voltages of various media shown in Table 3.3, it is most likely that the breakdown will occur in either a gas or non-ideal vacuum medium [56].

Medium	Breakdown Voltage (V/cm)
Vacuum (Ideal)	$> 10 \times 10^6$
Vacuum (Non-Ideal)	$0.5 \times 10^5 - 3 \times 10^5$
Gas	$< 100 - 1 \times 10^5$
Liquid	$0.5 \times 10^6 - 1 \times 10^6$
Solid	$0.5 \times 10^6 - 1 \times 10^6$

Table 3.3: Breakdown Voltages for Various Media

Vacuum pumps are used to remove gas particles present within the TWT to increase the breakdown voltage. However, the tube is never completely free from particles, increasing the possibility of DC breakdown in a vacuum, known as a vacuum arc or metal vapour plasma arc. During a vacuum arc, the surface of the negative electrode vaporises to form an ionised medium for currents to conduct between the electrodes. The amount of material removed from the electrodes depend on the energy that is fed into the arc, and the duration of the arc is proportional to the current passing through the arc. The likelihood and severity of an arc depends greatly on electrode shape, spacing and electric field potential. These are considerations which must be taken into account when designing the TWT radar power supply to minimise arc occurrences. A sustained arc will cause permanent damage and render the tube useless. Arcing is most likely to occur in the following areas:

- Electron gun: cathode-ground, grid-ground
- Collector: collector-ground
- High powered section within the radio frequency (RF) structure

A triggerable surge arrestor is used in a crowbar circuit to protect the TWT. A triggerable surge arrestor is essentially a spark gap which can be triggered to arc by a control signal, providing the voltage across the electrodes of the spark gap exceeds its breakdown voltage specification. When an arc is detected the surge arrestor is triggered to initiate its own breakdown, diverting the energy away from the tube, thus protecting and prolonging the life of the TWT.

This circuit protects the load against faults originating from within the load itself. In most cases, such faults will produce an increase in load current or voltage, so a 3-electrode gap is used and triggered by a circuit arranged to sense the fault condition. A travelling wave tube crowbar circuit with a self-triggering 3-electrode spark gap is shown in Figure 3.3. The purpose of the crowbar circuit is to divert power from the load immediately after a fault occurs, giving time for a mechanical circuit breaker to operate. If the trigger pulse has a fast rise time, the breakdown time can be less than 1 ms; if the reaction time of the fault sensing circuit is similarly short it is possible to remove anode power from the pulse amplifier tube before the end of the pulse in which the fault first occurs. The breakdown profile of the triggerable spark gap is shown in Figure 3.4 [57].

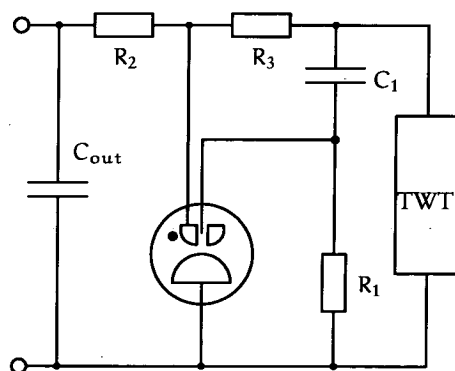


Figure 3.3: TWT Crowbar Circuit with Self-triggering 3-electrode Spark Gap

The crowbar circuitry only protects the TWT itself. The SMPS will still experience the equivalent of an output short-circuit, and must therefore be designed to withstand such a condition as standard. A common topology currently used for such purpose is the Current Fed Bridge Converter.

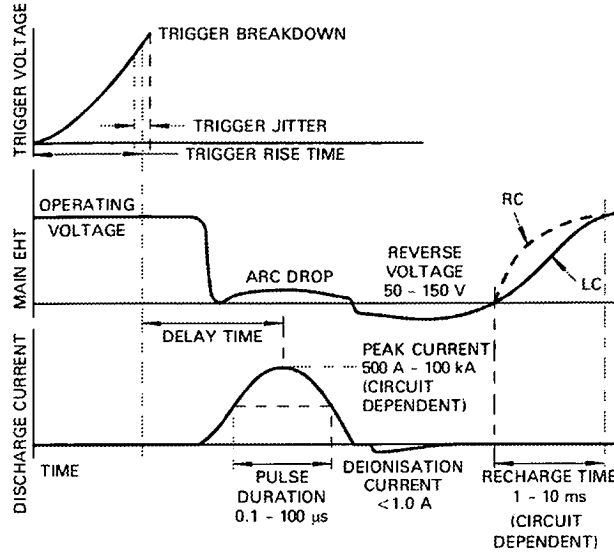


Figure 3.4: Typical Waveforms for 3-electrode Spark Gaps

3.3 Current Fed Bridge Converter

The Current Fed Bridge (CFB) Converter [58] (Figure 3.5) is basically a standard FB converter operating at a constant duty ratio of approximately 0.95 – 1.05. To enable output voltage control, a Buck converter is placed in front of the FB converter (shown within the dotted box in Figure 3.5). Varying the switching duty ratio of TPWM controls the amount of current fed to the FB converter for transfer to the output.

Diode D2 is required if the FB converter is operating with a duty ratio of less than 1. This provides a path for current to flow during the interval when all the switches in the FB converter are switched off. Diode D2 does not affect operation if left in circuit while the FB converter is operating with a duty ratio greater than 1. The waveforms in Figure 3.5 assume that the full bridge converter is running with a constant duty of less than unity.

Active Interval ($t_0 - t_1$)

During the active interval, power is actively transferred from the inputs of the CFB to the output. Current flows through TPWM, L_{choke} , and the full bridge where it is stepped up using the main transformer. The amount of current rise in L_{choke} within this interval is calculated using Equation 3.3 and 3.4.

$$\Delta i_{L_{\text{choke}}}(t_0 t_1) = i_{L_{\text{choke}}}(t_1) - i_{L_{\text{choke}}}(t_0) \quad (3.3)$$

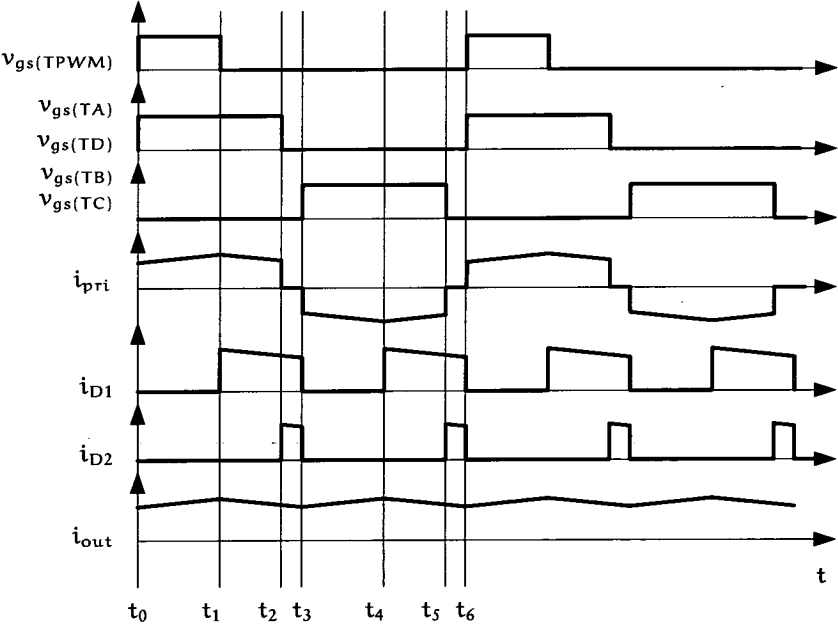
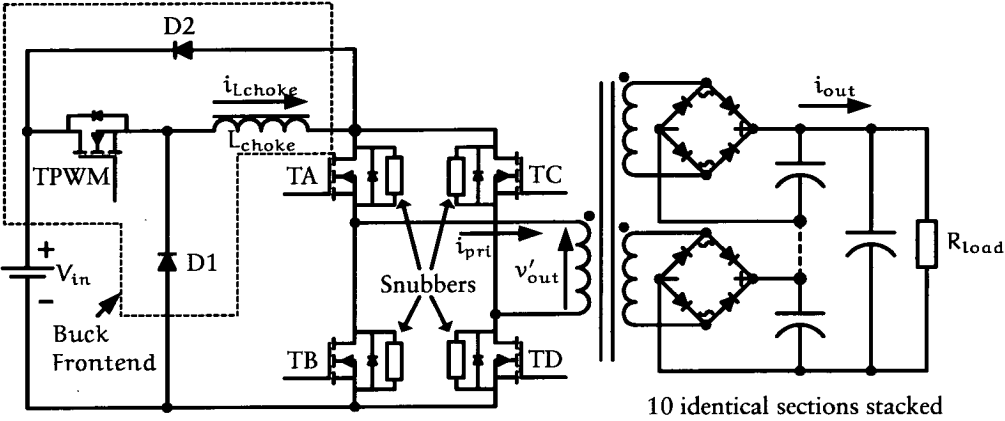


Figure 3.5: Current Fed Bridge Topology and Operating Waveforms

$$\Delta i_{\text{pri}(t_0 t_1)} = \frac{(V_{\text{in}} - V'_{\text{out}})T_{0.5}d}{L_{\text{choke}}} \quad (3.4)$$

where d is the duty of TPWM which is also the duty of the CFB.

Passive Interval ($t_1 - t_2$)

After TPWM is turned off, the converter enters the passive interval. As the current in L_{choke} must keep flowing, it freewheels through the full bridge using diode D_1 . Equation 3.5 calculates the current fall experienced by L_{choke} during this time.

$$\Delta i_{\text{pri}(t_1 t_2)} = \frac{-V'_{\text{out}}d_{\text{off}}T_{0.5}}{L_{\text{choke}}} \quad (3.5)$$

where

$$d_{\text{off}} = \frac{t_2 - t_1}{T_{0.5}} \quad (3.6)$$

Free-wheeling Current Interval ($t_2 - t_3$)

At the end of the half period, when all MOSFETs are switched off, D_2 now provides a path for current in L_{choke} to flow. As the current is now feeding back into the supply, L_{choke} current continues to fall as described by Equation 3.7.

$$\Delta i_{\text{pri}(t_2 t_3)} = \frac{-V_{\text{in}}d_{\text{CFBoff}}T_{0.5}}{L_{\text{choke}}} \quad (3.7)$$

where

$$d_{\text{CFBoff}} = \frac{t_3 - t_2}{T_{0.5}} \quad (3.8)$$

3.4 Capacitive Filter Versus LC Filter

SMPS with high voltage output often use capacitive output filters instead of the standard LC filters. This is due to the fact that a high voltage output inductor requires heavy insulation on its windings to prevent insulation breakdown. This makes the inductor difficult to wind and increases the likelihood of a converter failure. Therefore any inductors used should preferably be located on the low voltage primary side

of the transformer. The stringent filtering requirements of the TWT radar require the use of large capacitors to sustain output voltage during the high power pulse. The frequency response, therefore, will not be the typical two-pole LC filter, but that of a low frequency single pole due to the large capacitor. This can cause a sluggish closed response if the feedback loop is designed incorrectly.

3.5 Phase Shifted Bridge Converter with Capacitive Filter

The phase shifted bridge converter with capacitive filter (PSBCF) is controlled in a similar manner as the conventional PS-PWM-ZVS-FB Converter (Figure 3.6). The operation of the PSBCF is similar to that proposed in [59], the difference being that the output filter inductor is replaced by a resonant inductor located on the primary side, between the legs of the full bridge. The high leakage inductance inherent in high voltage transformers can be fully utilised for this topology. The output rectifier losses are mainly switching losses at low currents, high voltages as the reverse recovery times tend to be extended. However, because the current rate of rise and fall in the secondary are limited by the leakage inductance and operates in DCM, I_{RM} is reduced and subsequently t_{rr} is reduced too, reducing switching losses.

3.5.1 Detailed Operation in DCM

Figure 3.7 shows the main transformer primary winding voltage and current waveform in greater detail. The following sections describe the waveforms using equations derived from the simplified equivalent circuit diagrams during each interval (Figure 3.8). As the waveforms are symmetrical about the half period ($T_{0.5}$), it is sufficient to describe the operation of the circuit considering only the first half period.

Active Interval ($t_0 - t_1$)

When diagonally opposite MOSFETs TA and TD are switched on, current rises in the transformer primary as the primary inductors charge. Power is actively being transferred from the converter's input to its output.

$$I_{pri(Pk)} = \frac{(V_{in} - V'_{out})(t_1 - t_0)}{L_{pri}} \quad (3.9)$$

where

$$L_{pri} = L_{add} + L_{leak} \quad (3.10)$$

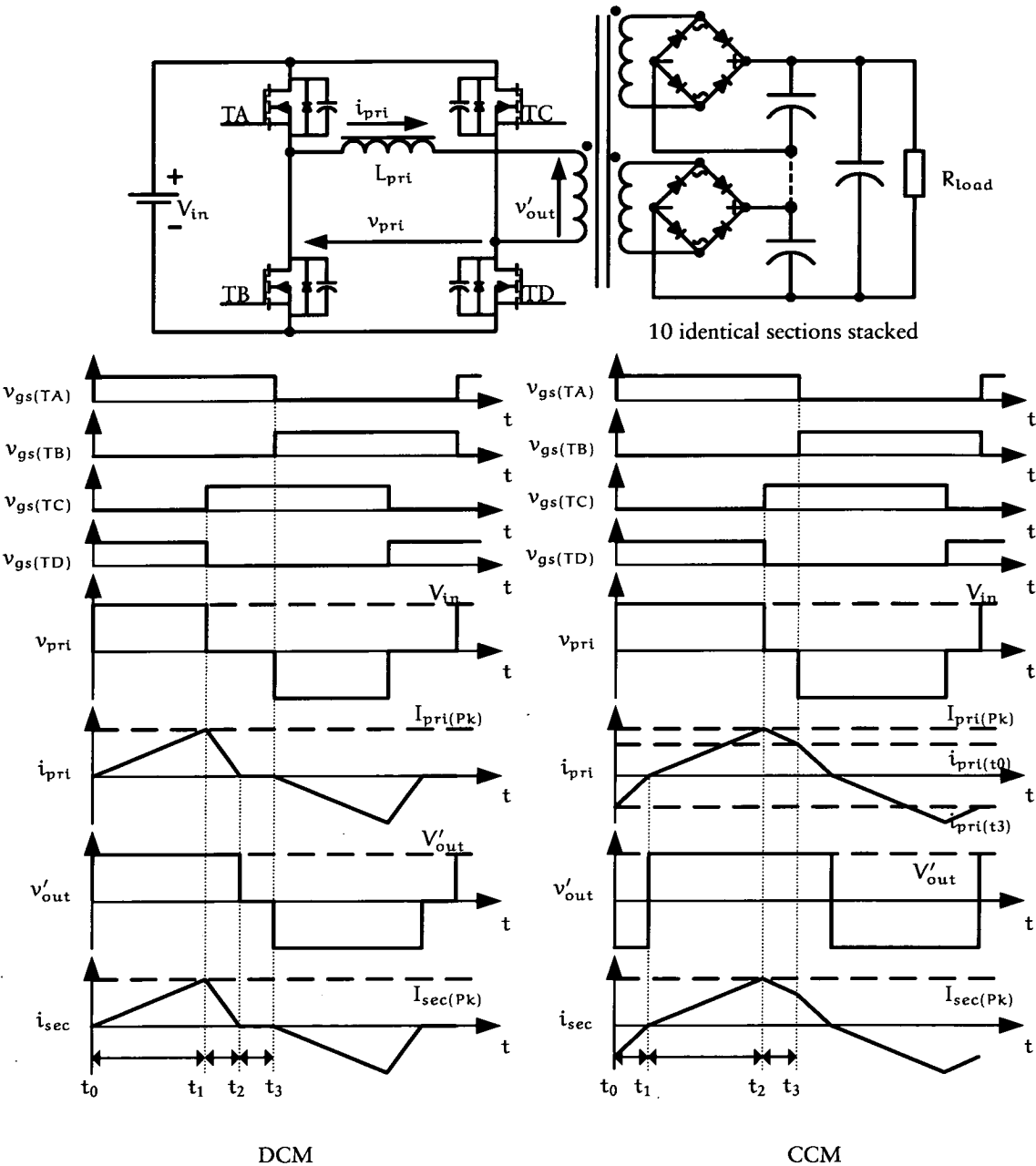


Figure 3.6: Phase Shifted Bridge with Capacitive Filter Topology and Operating Waveforms

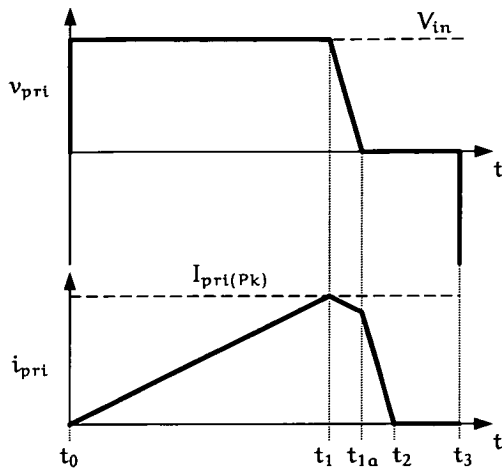


Figure 3.7: Voltage and Current Waveform for PSBCF (DCM)

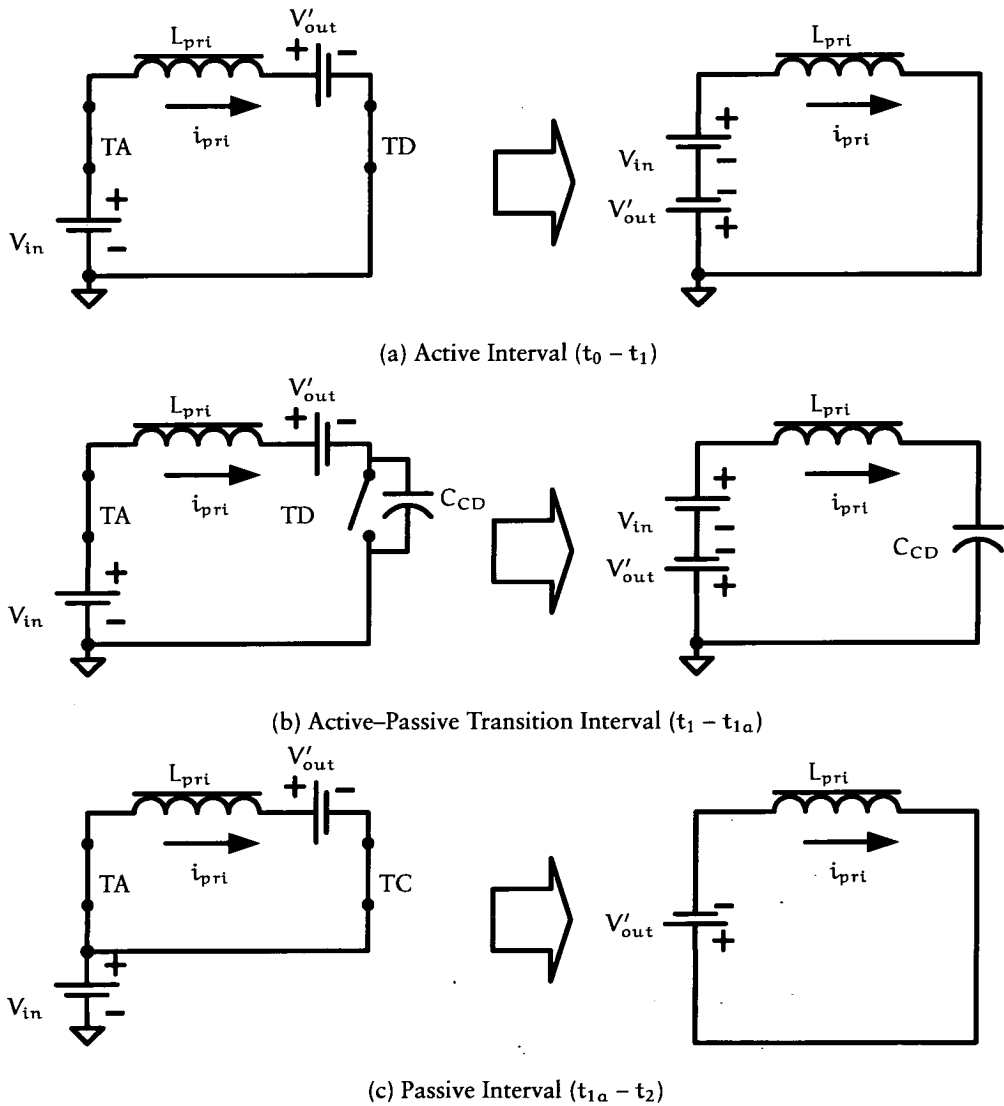


Figure 3.8: Circuit Representation for PSBCF during DCM Sub-Intervals

$$(t_1 - t_0) = d \cdot T_{0.5} \quad (3.11)$$

In the PSBCF the L_{pri} is the total value of inductance located in series with the main transformer between the legs of the full bridge. This includes the leakage inductance of the transformer, L_{leak} , and any additional value of inductance required, L_{add} .

Active–Passive Transition Interval ($t_1 - t_{1a}$)

When MOSFET TD is switched off, the inductor current continues to flow, charging up the output capacitance of TD and discharging that of TC, hence, lowering $v_{ds(TC)}$ to zero, preparing TC for zero voltage turn-on. This interval can be represented by the sub-circuit shown in Figure 3.8b and the voltage waveform described by Equation 3.12 (derived in a similar manner to Equation 2.8). However, due to the additional voltage source, not present in the resonant sub-circuit of the conventional PSB converter, an additional $(V_{in} - V'_{out}) - (V_{in} - V'_{out}) \cos \omega_{CD}(t - t_1)$ term is present in Equation 3.12. It can be shown that this additional term is always positive and makes it easier for the circuit to achieve ZVS when compared to a resonant sub-circuit without the voltage source. Therefore, if the amount of inductive energy stored is greater than the capacitive energy required to charge the MOSFET output capacitance to the input voltage, ZVS can be achieved.

If $E_{Lpri} > E_{CossCD}$

$$v_{ds(TD)}(t) = (V_{in} - V'_{out}) - (V_{in} - V'_{out}) \cos \omega_{CD}(t - t_1) + Z_{CD} i_{pri}(t_1) \sin \omega_{CD}(t - t_1) \quad (3.12)$$

where

$$\omega_{CD} = \frac{1}{\sqrt{L_{pri} C_{CD}}} \quad (3.13)$$

$$Z_{CD} = \sqrt{\frac{L_{pri}}{C_{CD}}} \quad (3.14)$$

and

$$t_{1a} - t_1 = \frac{\pi}{2} \sqrt{L_{pri} C_{CD}} \quad (3.15)$$

If the stored inductive energy is much greater than the stored capacitive energy, the inductor can be modelled as a constant current source using linearised Equation 3.16.

If $E_{L_{pri}} \gg E_{C_{ossCD}}$

$$t_{1a} - t_1 = C_{CD} \frac{V_{in}}{I_{pri(pk)}} \quad (3.16)$$

Passive Interval ($t_{1a} - t_2$)

During the passive interval, current continues to circulate in the upper half of the bridge (through MOSFETs TA and TC) and both the transformer primary and secondary. This interval begins when either the midpoint of the AP leg has been clamped to the high voltage supply line and current is flowing through the body diode of TC or when TC is switched on if ZVS does not occur. Although energy is still being transferred to the converter output, this is coming from the energy stored in the primary inductors and not from the input supply. As a result the inductor currents fall linearly as the inductors discharge.

$$t_2 - t_{1a} = L_{pri} \cdot \frac{I_{pri(pk)}}{V'_{out}} \quad (3.17)$$

Zero Current Interval ($t_2 - t_3$)

When the inductor current has fallen to zero, it stops flowing with the transformer and resonant inductor reset awaiting for the the same operation to occur in the opposite direction in the second half of the switching cycle.

Average DCM Currents

The current in L_{pri} is averaged by averaging the various sub-intervals within half a switching period when operating in DCM. An assumption is made that the resonant transition intervals are negligible in comparison to the overall switching period.

From $t_0 - t_1$, solving for $I_{pri(pk)}$:

$$I_{pri(pk)} = (V_{in} - V'_{out})d \frac{T_{0.5}}{L_{pri}} \quad (3.18)$$

From $t_1 - t_2$, solving for d_{fall} (assuming that the AP transition interval is negligible):

$$d_{fall} = (V_{in} - V'_{out}) \frac{d}{V'_{out}} \quad (3.19)$$

where

$$d_{fall} = \frac{t_2 - t_1}{T_{0.5}} \quad (3.20)$$

Averaging for half the period, the averaged input DC current, I_{pri} , and the averaged output DC current reflected back to the primary side of the transformer, I'_{sec} , are:

$$I_{pri} = \frac{1}{2} \cdot (V_{in} - V'_{out}) d^2 \frac{T_{0.5}}{L_{pri}} \quad (3.21)$$

$$I'_{sec} = \frac{1}{2} \cdot (V_{in} - V'_{out}) d^2 \frac{T_{0.5} V_{in}}{L_{pri} V'_{out}} \quad (3.22)$$

Assuming the converter is lossless, the equations balance out as:

$$\frac{I_{pri}}{I'_{sec}} = \frac{V'_{out}}{V_{in}} \quad (3.23)$$

From Equation 3.22, an equation can be obtained which links the converter's output power to input conditions (Equation 3.24).

$$P_{out} = I'_{sec} V'_{out} = \frac{1}{2} \cdot (V_{in} - V'_{out}) d^2 \frac{T_{0.5} V_{in}}{L_{pri}} \quad (3.24)$$

3.5.2 Detailed Operation in CCM

Figure 3.9 shows that the PSBCF operates with a few key differences when operating in CCM instead of DCM. A power recovery interval exists at the start of the switching cycle ($t_0 - t_1$).

Power Recovery Interval ($t_0 - t_1$)

During this interval, the converter is returning energy stored in L_{pri} , at the end of the last half cycle (t_0), back to the supply. This allows L_{pri} to reset as i_{pri} gradually goes back to zero. The power recovery interval steals duty, d_{prec} (Equation 3.26), from the overall duty, d , of the converter and it is this property that provides the converter with a power limiting feature.

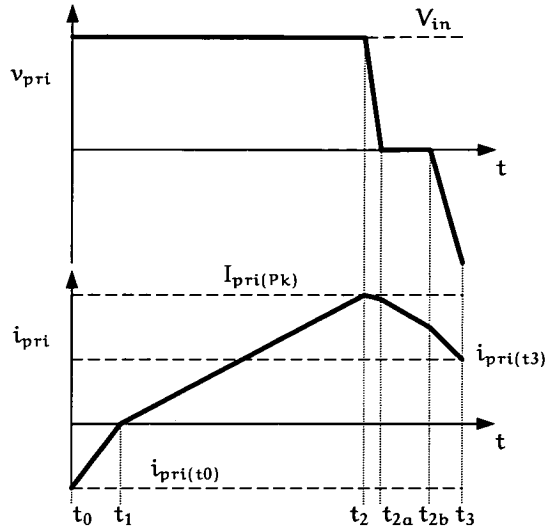


Figure 3.9: Voltage and Current Waveform for PSBCF (CCM)

$$V_{in} + V'_{out} = L_{pri} \frac{i_{pri}(t_0)}{d_{prec} T_{0.5}} \quad (3.25)$$

$$d_{prec} = \frac{t_1 - t_0}{T_{0.5}} \quad (3.26)$$

Active Interval ($t_1 - t_2$)

This interval is similar to that found in DCM operation with the exception that it starts at a later time with a reduced duty value.

$$V_{in} - V'_{out} = L_{pri} \frac{I_{pri}(Pk)}{(d - d_{prec}) T_{0.5}} \quad (3.27)$$

Active–Passive Transition Interval ($t_2 - t_{2a}$)

Again, this section operates in a similar manner to that found in DCM. However, since current values are naturally higher in CCM than in DCM, it is acceptable use the linearised equations to describe the waveforms.

$$t_{2a} - t_2 = C_{AB} \frac{V_{in}}{I_{pri}(Pk)} \quad (3.28)$$

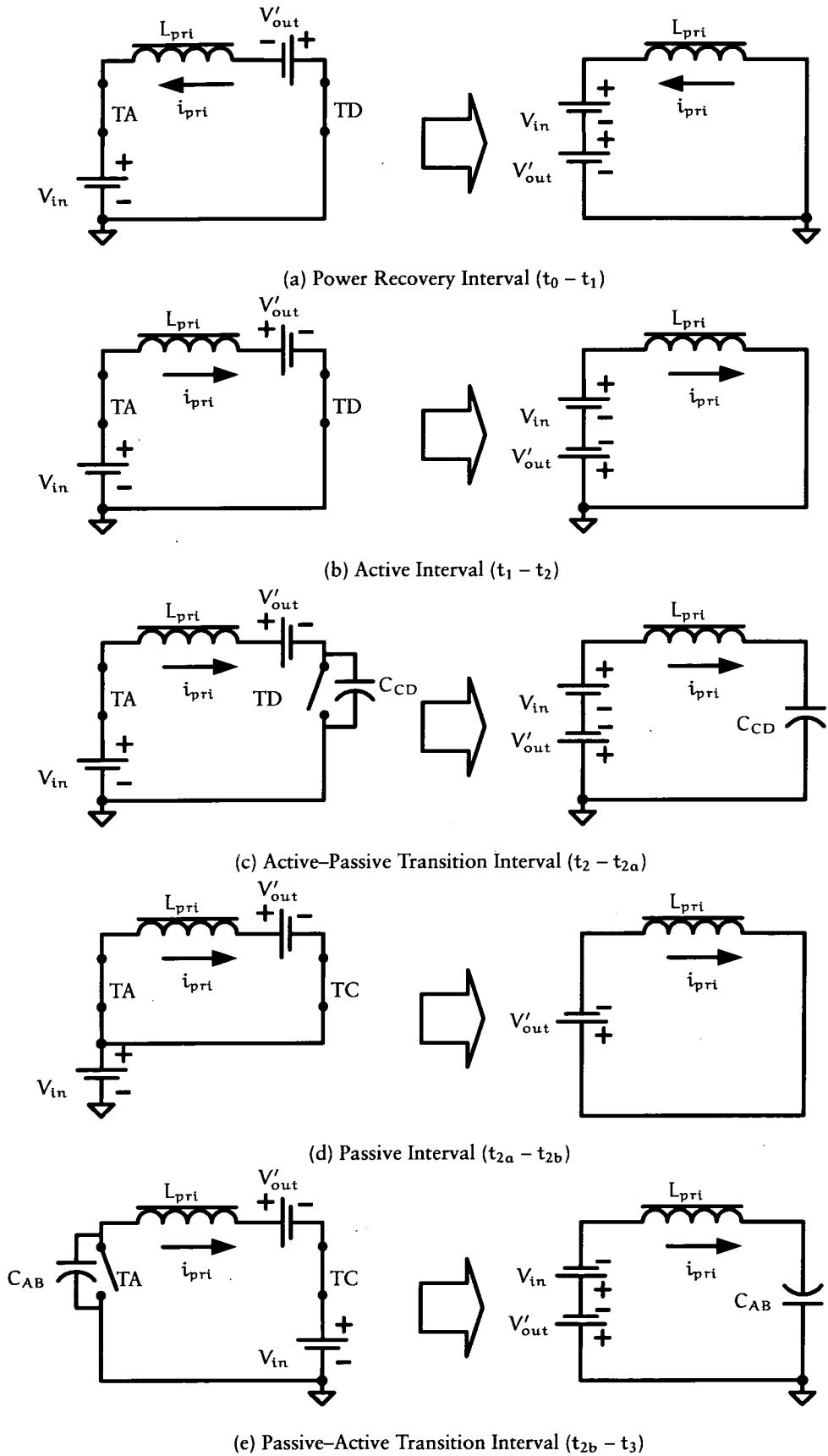


Figure 3.10: Circuit Representation for PSBCF during CCM Sub-Intervals

Passive Interval ($t_{2a} - t_{2b}$)

The passive interval does not last long enough for the current to fall to zero to reset L_{pri} .

$$V'_{out} = L_{pri} \frac{(I_{pri(pk)} - i_{pri(t0)})}{(1 - d)T_{0.5}} \quad (3.29)$$

Passive-Active Transition Interval ($t_{2b} - t_3$)

With a now reduced current, $i_{pri(t2b)}$, ZVS might still be achievable due to the large L_{pri} employed by this circuit design.

Average CCM Currents

Solving for the various points on the graph, the following results are obtained:

$$I_{pri(pk)} = \frac{1}{2} \cdot (V_{in} - V'_{out})T_{0.5} \frac{(d \cdot V_{in} + V'_{out})}{L_{pri} V_{in}} \quad (3.30)$$

$$i_{pri(t0)} = \frac{1}{2} \cdot T_{0.5} \frac{(V_{in} + V'_{out})(d \cdot V_{in} - V'_{out})}{L_{pri} V_{in}} \quad (3.31)$$

$$d_{prec} = \frac{1}{2} \cdot \frac{(d \cdot V_{in} - V'_{out})}{V_{in}} \quad (3.32)$$

Averaging for the intervals:

$$I_{pri(t0t1)} = \frac{1}{2} \cdot d_{prec} i_{pri(t0)} \quad (3.33)$$

$$I_{pri(t0t1)} = \frac{1}{8} \cdot T_{0.5} (V_{in} + V'_{out}) \frac{(d \cdot V_{in} - V'_{out})^2}{L_{pri} V_{in}^2} \quad (3.34)$$

$$I_{pri(t1t2)} = \frac{1}{2} \cdot (d - d_{prec}) I_{pri(pk)} \quad (3.35)$$

$$I_{pri(t1t2)} = \frac{1}{8} \cdot T_{0.5} (V_{in} - V'_{out}) \frac{(d \cdot V_{in} + V'_{out})^2}{L_{pri} V_{in}^2} \quad (3.36)$$

$$I_{pri(t2t0)} = \frac{1}{2} \cdot (1 - d) (I_{pri(pk)} + i_{pri(t0)}) \quad (3.37)$$

$$I_{pri}(t_2t_0) = \frac{1}{2} \cdot T_{0.5}(d \cdot V_{in}^2 - V_{out}'^2) \frac{(1-d)}{L_{pri}V_{in}} \quad (3.38)$$

To calculate the average currents for V_{in} :

$$I_{pri} = I_{pri}(t_1t_2) - I_{pri}(t_0t_1) \quad (3.39)$$

$$I_{pri} = \frac{1}{4} \cdot T_{0.5}V_{out}' \frac{(2d \cdot V_{in}^2 - d^2V_{in}^2 - V_{out}'^2)}{L_{pri}V_{in}^2} \quad (3.40)$$

and the secondary currents reflected back to the primary:

$$I'_{sec} = I_{pri}(t_0t_1) + I_{pri}(t_1t_2) + I_{pri}(t_3t_0) \quad (3.41)$$

$$I'_{sec} = \frac{1}{4} \cdot \frac{T_{0.5}}{V_{in}} \cdot \frac{(2d \cdot V_{in}^2 - d^2V_{in}^2 - V_{out}'^2)}{L_{pri}} \quad (3.42)$$

3.5.3 Deficiencies

If large MOSFETs are used to withstand short-circuit currents, the converter with a capacitive filter will suffer from a slightly increased duty loss to allow for the resonant Active–Passive Transition Interval. As MOSFET C_{oss} is proportional to the MOSFET die size, a larger L_{pri} is required to achieve ZVS. The natural resonant frequency of the resonant LC circuit is then reduced, requiring a larger AP transition interval to charge the C_{oss} to V_{in} .

As the passive–active leg undergoes ZCS at turn-on, charge dumping occurs each time TA or TB switches. Thus as frequency increases, the losses will increase and the effective duty is reduced.

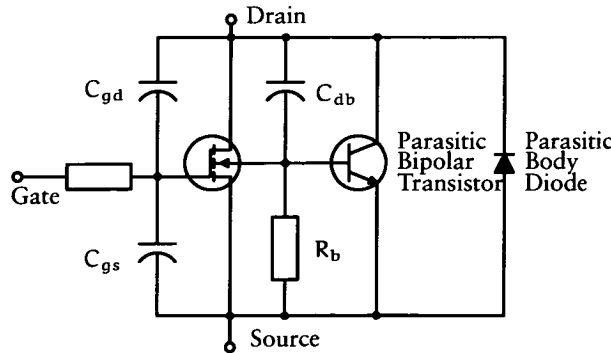


Figure 3.11: Equivalent Circuit Showing $C \frac{dv}{dt}$ Turn-on

Further problems can arise due to ‘cross-conduction’ (two transistors in the same leg conducting simultaneously) when operating the converter at high frequencies without ZVS. When charge dumping occurs the MOSFETs experiences a very high $\frac{dv}{dt}$. For example, if TA turns on without ZVS, there will be high $\frac{dv}{dt}$ across the drain and source, V_{ds} , of TB. From Figure 3.11, it can be seen that the capacitive components of the MOSFET will start to pull v_{ds} to V_{in} . In addition, $v_{gs}(TB)$ will be pulled high. This may cause TB to turn on and cross-conduction to occur if $v_{gs}(TB)$ exceeds the MOSFET’s threshold voltage.

This can be avoided by either ensuring that the reverse recovery $\frac{dv}{dt}$ characteristic of the MOSFET is high enough or that the turn-on speed of the MOSFET is limited to prevent the high $\frac{dv}{dt}$ rise. In addition, by ensuring that all MOSFETs undergo ZVS, cross-conduction caused by high $\frac{dv}{dt}$ can be avoided as the rate of voltage rise is limited by the resonant components.

The inductor added to make the converter resilient to short-circuits must be rated for the short-circuit current. If the core saturates during a short-circuit its inductance will reduce causing a cascade short-circuit. Thus the inductor core design area product must be over-rated to store the energy during peak short-circuit current, I_{SC} , and not just for normal operating currents. This is also true for the large input choke used by the current fed bridge converter.

The large input choke in the normal current fed bridge can only slow down the rate of rise of current. The maximum peak current is limited only by internal parasitic impedances. However, with the PSB, the currents are limited by the switching frequency of the converter together with the inductance due to the bipolar voltage waveforms seen by the inductor.

The requirements for rating the inductors for the short-circuit condition make it difficult to design a gapped ferrite core inductor. Molypermalloy Powder (MPP) cores are a good choice although they were designed to be operated at lower frequencies for optimum efficiency due to core loss. Air core inductors are a good alternative as they cannot saturate and do not suffer from magnetic core losses. The overall size of the inductor does not change when I_{SC} changes. Unfortunately the A_L value of air is low and a larger inductor results. A major disadvantage of using air core inductors is that by not using a magnetic material to contain and direct the magnetic flux, large EM radiation results. At high frequencies, this is especially serious for applications such as airborne radar systems where EM radiation must be limited as it is likely to interfere and disrupt the operation of sensitive equipment on board. The use of a toroidal air core inductor would force the flux to flow within the donut shaped toroid and reduce leakage flux radiating EMI. A better solution is to contain the air core inductor in a magnetic material to prevent the flux from straying out. However, this means that the size and weight of the inductor will increase. In addition, any

high frequency flux flowing within the container will cause eddy current losses.

3.5.4 Operation Under Extreme Conditions

When the converter is operated under extreme conditions, such as output short-circuits, the PSB may sometimes fail [60, 61, 62]. This phenomena is caused by the MOSFET failure. Normally MOSFETs are designed to conduct current in the direction from drain to source (N-type MOSFET). However, the PSB utilises the MOSFET body diode to allow current to flow in the opposite direction. Figure 3.12 shows what happens in MOSFET TD before and after ZVS occurs.

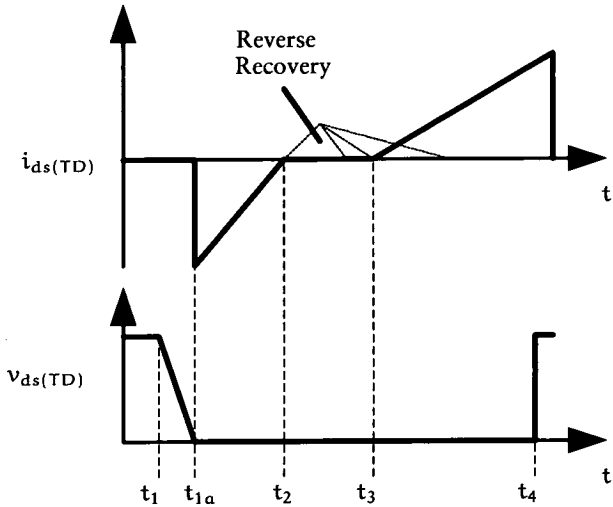


Figure 3.12: Reverse Recovery Time for MOSFET Body Diode

Just as in Figure 3.7, the AP transition begins after TC switches off at t_1 . $v_{ds}(TD)$ falls to zero by t_{1a} and is clamped at zero by the forward conduction of the body diode (shown by the negative $i_{ds}(TD)$ current) allowing TD to turn on under ZVS. Current continues to flow in the diode until t_2 when current stops flowing except for the reverse recovery current (shown in fine dotted lines). At t_3 , TA turns on and the direction of current flow begins to change, assisting the diode to recover.

The different reverse recovery lines shown in Figure 3.12 represent MOSFETs with different reverse recovery times. Reverse recovery is achieved when forward current passes through the drain-source channel creating a voltage drop across the PN junction, allowing the minority carriers in the PN junction to recombine. This is shown in Figure 3.7 by the dotted waveform falling back to zero again.

The body diode of the MOSFET is a parasitic diode and is not normally used due to the long reverse recovery time. When the body diode is used, it must be allowed to fully recover before a reverse voltage is applied at t_4 or else the body diode will undergo reverse conduction and breakdown. Diodes with short reverse recovery



times allow the converter to operate at higher frequencies and with smaller duties. Reverse recovery time for the body is inversely proportional to the input voltage [62] and should not pose a problem when supplying high powers operating from a high input voltage. However, the parasitic diode is inherently a poor performing diode compared to discrete diodes, although manufacturers have begun designing MOSFETs with fast recovery body diodes for specific use in ZVS converters.

Although reverse recovery times are reduced as the diode forward currents are reduced, the MOSFET might still not conduct forward currents for long enough to allow the body diode to recover before being forced to block the full input voltage. This will cause the MOSFET to continue conducting when the opposing MOSFET on the same leg is about to turn on, resulting in cross-conduction. This might occur when the converter is experiencing an output short-circuit and has reduced duty to a minimum or is operating at low loads with extremely low duty.

Conduction of the MOSFET body diode can be avoided using discrete diodes around the MOSFET to steer the current away. However, the diode in series with the MOSFET (blocking reverse current) will add to conduction losses when allowing current to flow in the normal direction. Another possible solution is to accurately turn on the MOSFET just before ZVS is about to be achieved. If this could be achieved at, say, turn on at $v_{DS} = 1$, that will mean only $\frac{1}{2}C \cdot 1^2$ joules is dissipated. Conduction losses will also be lowered as the currents will only conduct through the more efficient Drain-Source channel.

3.5.5 Improvements to the PSBCF

As the PSBCF operates with the PA leg utilising ZCS, it is inherently less efficient than if it were to operate with ZVS. The two passive auxiliary circuits designed for the conventional phase shifted bridges were the LDD and LCC auxiliary circuits. These circuits generally use the inductor to keep current flowing around the PA leg until the PA transition when the current is used to charge or discharge C_{AB} .

3.5.6 LDD Auxiliary

ZVS can be achieved by adding an auxiliary circuit with two diodes, D_{aux1} and D_{aux2} , and an additional inductor, L_{aux} . L_{aux} is connected between the midpoint of the PA leg and L_{pri} . This allows currents to circulate through the MOSFETs on the PA leg, L_{aux} and the auxiliary diodes to achieve ZVS after current in L_{pri} has fallen to zero. However, due to the higher circulating currents, conduction losses increase. Turn-off losses also increase due to the increase in circulating currents.

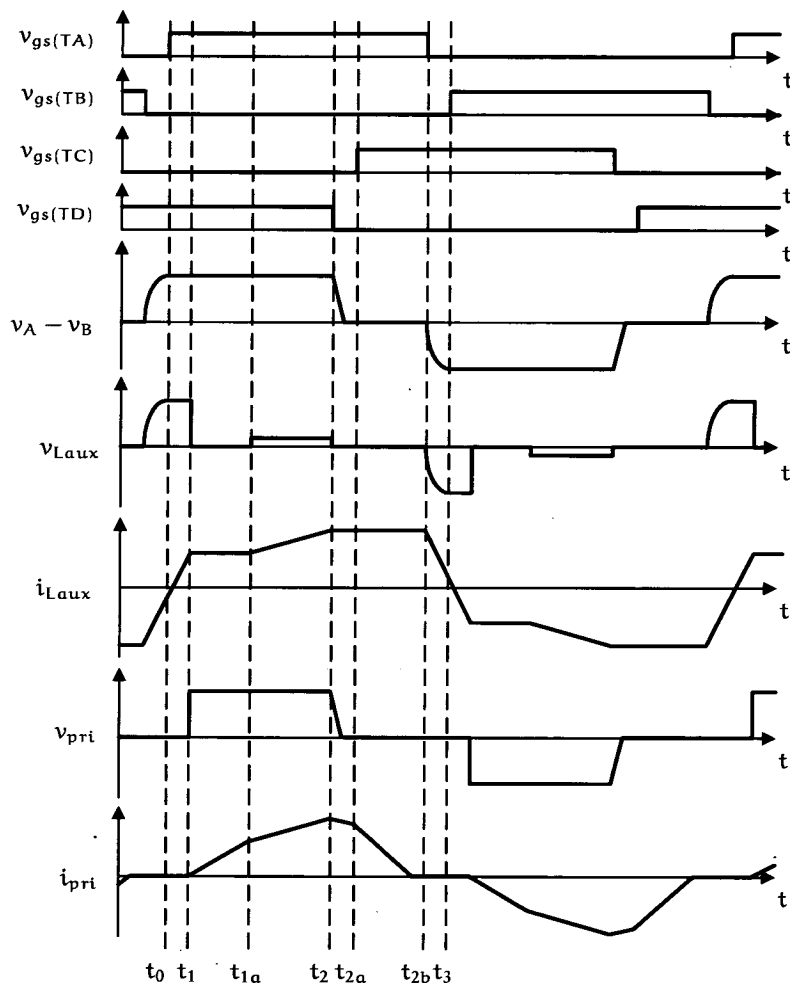
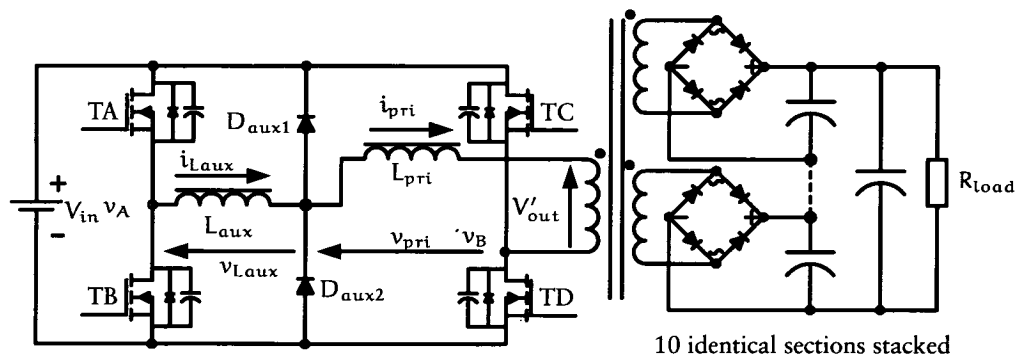


Figure 3.13: PSBCF with LDD Auxiliary Circuit

Operation of the LDD Auxiliary

Recovery Interval ($t_0 - t_1$)

At t_0 ZVS has been achieved for TA. TA is now switched on and due to the change in polarity of voltage across L_{aux} the current through L_{aux} , $i_{L_{aux}}$, starts to change direction. The gradient of the current change can be determined using Equation 3.43.

$$\frac{di_{L_{aux}}}{dt} = \frac{V_{in}}{L_{aux}} \quad (3.43)$$

The current continues to rise until it reaches $i_{L_{aux}}(t_1)$. $i_{L_{aux}}(t_1)$ is determined by the I_{RM} value of the auxiliary diode, D_{aux2} , which was previously conducting (Figure 3.14). During this interval $i_{L_{aux}}$ has to go to zero before D_{aux2} can begin to recover and V_{in} only appears across the transformer at t_1 when D_{aux2} reaches its peak recovery current value. This is shown in voltage and current waveforms of a diode undergoing reverse recovery in Figure 3.14. This results in a loss of duty for the converter and the duty loss can be expressed as in Equations 3.44 and 3.45.

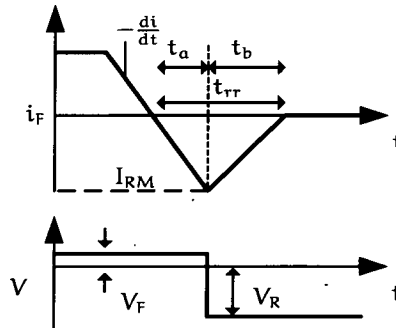


Figure 3.14: Diode Voltage and Current Waveforms During Reverse Recovery

$$d_{loss} = \frac{t_1 - t_0}{T_{0.5}} \quad (3.44)$$

$$t_1 - t_0 = \frac{i_{L_{aux}}(t_0)}{\frac{di_{L_{aux}}}{dt}} + t_a \quad (3.45)$$

The ratio of t_b to t_a , S , is also known as the 'softness' factor (Equation 3.46). [63] provides formulas to estimate S , I_{RM} , recovery charges (Q_{rr}) and t_{rr} , parameters which are often missing from manufacturers' datasheets.

$$S = \frac{t_b}{t_a} \quad (3.46)$$

As $\frac{di}{dt}$ is fixed by the inductor, the peak recovery value depends on S and Q_{rr} . Thus, it is better to select a soft diode with low recovery charges to minimise the duty loss and keep circulating currents to a minimum.

First Active Interval ($t_1 - t_{1a}$)

During this interval, current in L_{pri} is being charged up after D_{aux2} has recovered. During this time, $i_{L_{aux}(t1)}$ continues to circulate around TA, L_{aux} and D_{aux1} . As the current builds up in L_{pri} it approaches $i_{L_{aux}(t1)}$ which occurs at t_{1a} .

Second Active Interval ($t_{1a} - t_2$)

At t_{1a} , the current flowing in D_{aux1} has dropped to zero and the currents now flow through TA, L_{aux} , L_{pri} and TD, satisfying $L_{pri} = i_{L_{aux}(t1)}$. Current in L_{pri} now rises at a rate determined by the summed primary and auxiliary inductance value (Equation 3.47).

$$\frac{di_{pri}}{dt} = \frac{(V_{in} - V'_{out})}{(L_{aux} + L_{pri})} \quad (3.47)$$

Active–Passive Transition Interval ($t_2 - t_{2a}$)

The AP transition interval is again similar to that of the PSBCF without any auxiliary circuit. Equations 3.12 to 3.16 can be used to describe the waveform with the exception that the resonant inductor value of L_{pri} should be replaced with $(L_{aux} + L_{pri})$. TC should be able to switch on with ZVS due to the high levels of current flowing through the summed resonant inductance by t_{2a} .

Passive Interval ($t_{2a} - t_{2b}$)

During the Passive interval, the currents in the two inductors are free to take their own values again. i_{pri} ramps down as with the PSBCF without auxiliaries while $i_{L_{aux}}$ circulates around TA, L_{aux} and D_{aux1} .

Passive–Active Transition Interval ($t_{2b} - t_3$)

Depending on the value of L_{aux} chosen, the voltage waveforms for the PA transition can be obtained by modifying Equation 2.8. MOSFET capacitance values are those of the PA leg and the resonant inductor is now L_{aux} instead of L_{pri} .

Effective duty is reduced due to the reverse recovery of the auxiliary diodes with L_{aux} limiting $\frac{di_{L_{aux}}}{dt}$. Therefore using fast recovery ‘soft’ diodes with low recovery charge helps reduce duty loss. A PSBCF converter can be simply modified by adding the additional required components to an existing PSBCF design. A minimum value of L_{aux} should be used to avoid disrupting the converter circuit’s operation. If the duty loss caused by the auxiliary is unacceptable, it can be compensated for by reducing the value of L_{pri} by an appropriate amount such that the overall power capability of the converter remains the same. As the energy stored within L_{aux} is determined by the peak current in L_{pri} (Equation 3.48), a minimum load is required for the converter so as to stored enough energy in L_{aux} to overcome the energy stored in C_{AB} (Equation 3.49) for ZVS to occur. d for the minimum load can be calculated using Equation 3.24 and $I_{pri(pk)}$ can then be calculated using Equation 3.49.

$$E_{L_{aux}} = \frac{1}{2} L_{aux} i_{pri(t2a)}^2 \quad (3.48)$$

$$\frac{1}{2} L_{aux} I_{pri(pk)}^2 > \frac{1}{2} C_{AB} V_{in}^2 \quad (3.49)$$

Equation 3.49 must be satisfied for soft switching to occur.

If the minimum value of inductance is used, duty loss is reduced and more power is obtained from the converter. The maximum amount of inductance is determined by the reverse recovery characteristics of the diode, which in turn determines the duty loss.

3.5.7 LCC Auxiliary

An alternative LCC auxiliary circuit can be used to assist the PA leg achieve ZVS. The LCC auxiliary circuit is attached to the PA leg as shown in Figure 3.15.

Operation of the LCC Auxiliary

The PSBCF with LCC auxiliary circuit operates in a similar manner to the PSBCF. This is because the current in L_{aux} flows only through the MOSFET on the PA leg and not through the transformer, thus the auxiliary circuit does not affect general operation except during the PA transition interval.

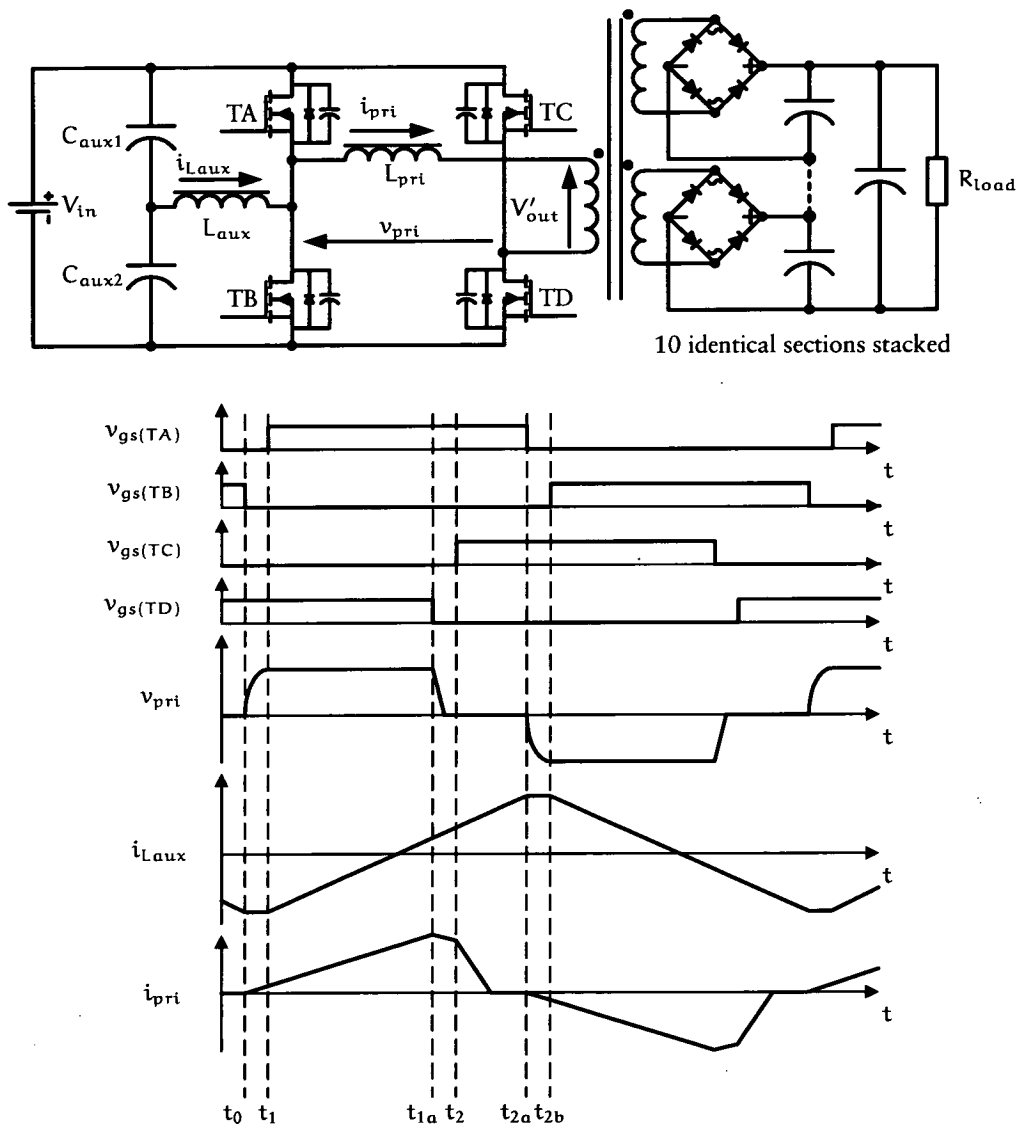


Figure 3.15: PSBCF with LCC Auxiliary Circuit

Passive–Active Transition Interval ($t_0 - t_1$)

As MOSFETs on the PA leg operate with approximately 0.5 duty, the voltage waveform developed across L_{aux} will also be 0.5 duty waveform with an amplitude of $V_{in}/2$. Therefore, the current in L_{aux} at t_0 , can be approximated in Equation 3.50.

$$i_{L_{aux}(t_0)} = \frac{V_{in} T_{0.5}}{4L_{aux}} \quad (3.50)$$

A sub-circuit representation similar to that in Figure 3.8b can be derived for this interval with a voltage source of $V_{in}/2$ and L_{aux} as the resonant inductor. As with the previous analysis, if L_{aux} stores enough energy to charge both the MOSFET output capacitances and transformer distributed inter-turn winding capacitance, C_{dist} , then ZVS of the Passive–Active leg MOSFETs is achieved. Therefore, the value of L_{aux} can be calculated using Equation 3.52 assuming that there is a 20% spread in capacitance values.

$$L_{aux} > \frac{(C_{AB} V_{in}^2 + C_{dist} V_{out}'^2) \times 1.2}{\left(\frac{V_{in} T_{0.5}}{4L_{aux}}\right)^2} \quad (3.51)$$

$$L_{aux} < \frac{(V_{in} T_{0.5})^2}{(C_{AB} V_{in}^2 + C_{dist} V_{out}'^2) \times 4.8} \quad (3.52)$$

The two input capacitors can replace the input bulk capacitors which are required to filter out the input voltage ripples and hold up the input voltage in case of any disruptions.

3.6 Chapter Summary

A brief introduction to the TWT radar is given in Chapter 3. The general pulsed loading patterns, voltage and current requirements for a pulse TWT are also presented. Stringent requirements for the TWT radar power supply such as noise coupled from the power supply to the radar and the TWT's arc prone nature due to its construction and high voltages present were also discussed. The operation of the current-fed bridge converter, presently used by BAe Systems, is presented. To reduce the effects of coupled noise from the radar's power supply, it is preferable to synchronise the switching of the converter to the radar's pulse to enable the effects to be better filtered. Unfortunately, due to the hard switching employed by the CFB, the converter is unable to switch at the high frequencies of the radar pulses. To avoid damage to the radar power supply, the converter utilises a large input choke to limit the rate of

current rise in event of a short-circuit. However, this requires the use of an additional over-current sensor, as this method does not actually limit the maximum short-circuit currents.

Chapter 4

Method of Design

4.1 Background

A method of designing the PSBCF was created in order to get a proper functioning PSBCF converter which takes into account the input, output power requirements and component specifications. This requires the converter to be analysed to determine its output power capability, and to optimise this by limiting short circuit current and component stress while maximising output power and switching frequency. Following this, the other components of the converter are discussed, *i.e.* MOSFETs, transformers, inductors, capacitors and others, to determine the best choice of components for use in the PSBCF.

4.2 Determination of Operating Conditions

4.2.1 Power Limitation

A feature of the Phase Shifted Bridge with capacitive filter is that it can be designed to limit power output during output faults. Therefore, the maximum power output of the circuit needs to be defined before designing the circuit. In this project, a prototype converter was built with the following specifications.

- V_{out} : 1 kV
- V_{in} : 370 V
- P_{out} : 1 kW
- f_{sw} : 250 kHz

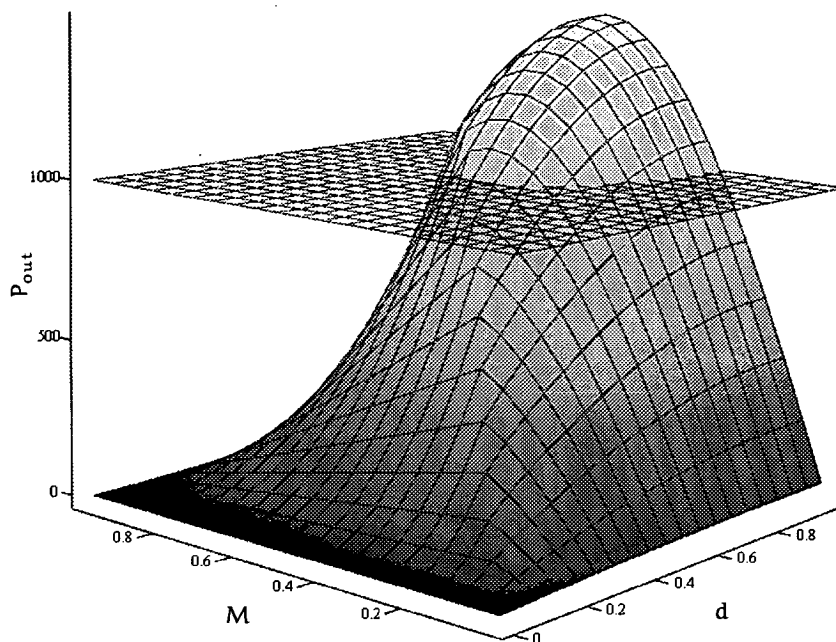


Figure 4.1: Converter Output Power at Various Modulation Index and Duty

A 3D graph (Figure 4.1) shows how output power varies against the modulation index, M , and converter duty, d . Modulation index, M , is defined as:

$$M = \frac{V'_{out}}{V_{in}} \quad (4.1)$$

M is an important factor as observed from Figure 4.1, the maximum output power is determined by the correct selection of M . The horizontal plane shown on the graph shows the 1 kW minimum output power requirement of the converter.

The converter operates in DCM, on the left hand side of the figure, where $M > d$. Output power increases exponentially as duty is increased up to the boundary condition ($M = d$). In CCM (right hand side of the figure), where $M < d$, output power continues to increase with duty and is limited when $d = 1$. Figure 4.1 shows that maximum power output can be achieved with a modulation index of 0.5 in CCM. From the previous chapter it is shown that it is preferable to operate in DCM due to current being returned to V_{in} when operating in CCM during t_0 - t_1 (Section 3.5.2). The power limitation can be seen in Figure 4.4, where V_{out} is held constant, and duty is plotted against I_{out} (normalised to the boundary condition current, I_{BC}). (Plots of various M values are overlaid on the same graph) Figure 4.4 also shows that the converter can achieve a greater range of output power in DCM than in CCM provided an optimum modulation index is used.

By holding V_{in} constant, Figure 4.5 again shows the power limitation imposed on the circuit as the operation moves in the CCM region.

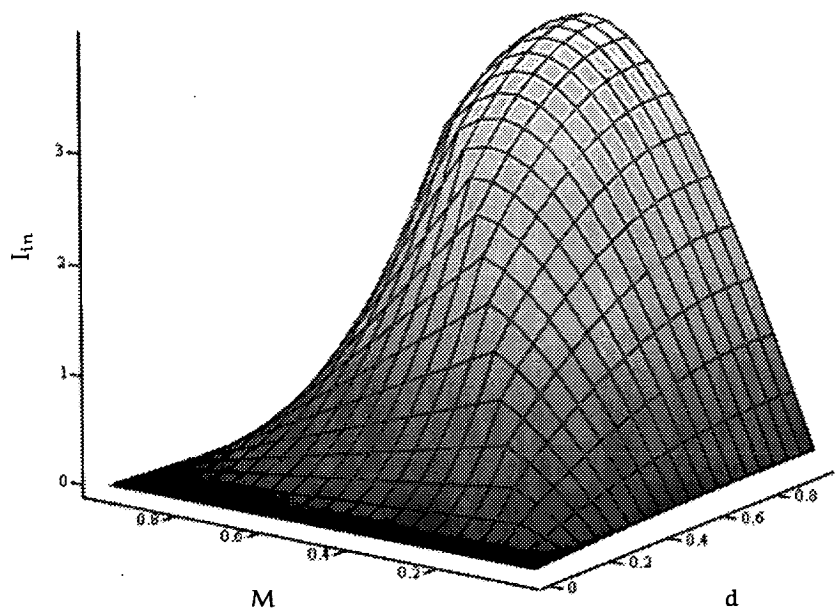


Figure 4.2: Converter Input Current at Various Modulation Index and Duty

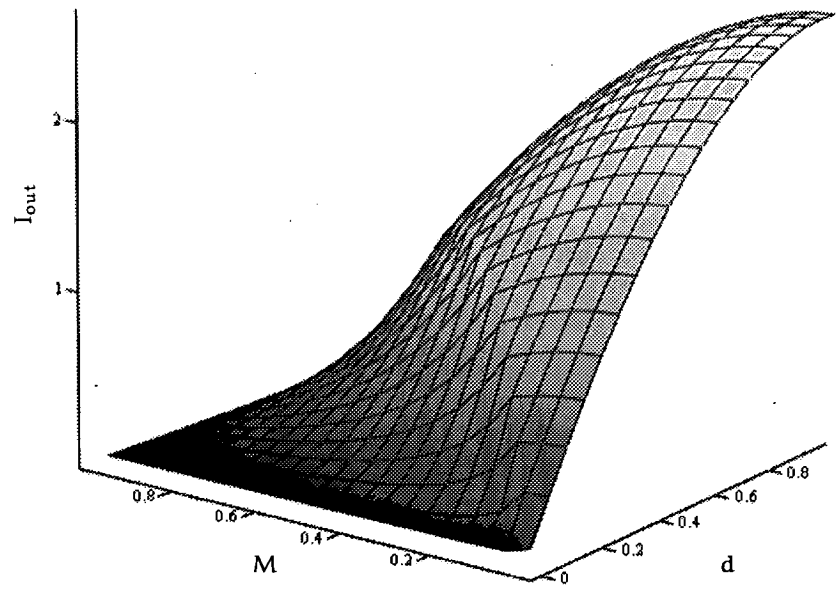


Figure 4.3: Converter Output Current at Various Modulation Index and Duty

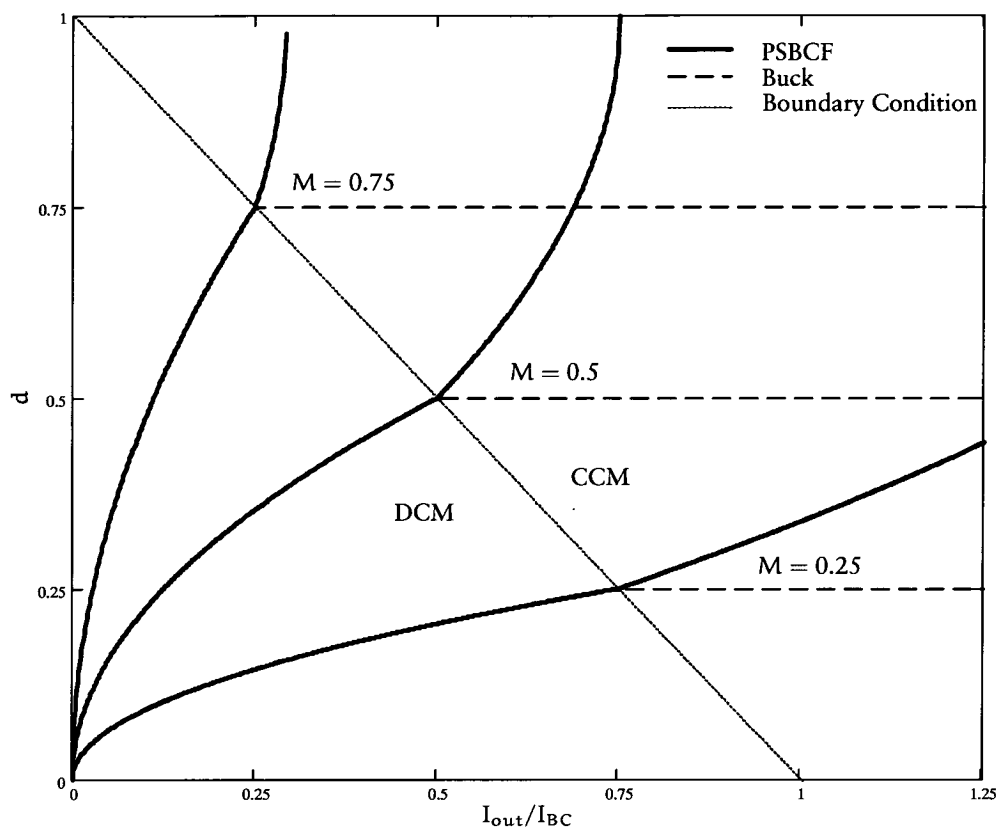


Figure 4.4: Characteristics of PSBCF Converter when V_{out} is Held Constant

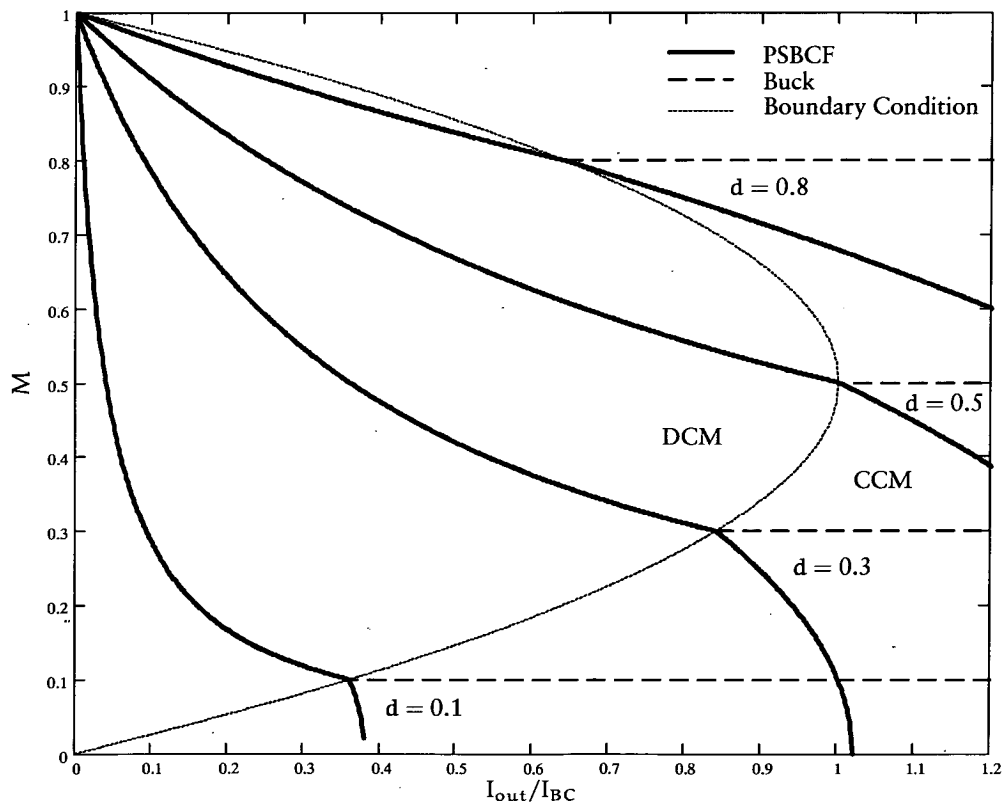


Figure 4.5: Characteristics of PSBCF Converter when V_{in} is Held Constant

Figures 4.1, 4.4 and 4.5 all show that the choice of M is crucial in determining output power. As it is preferable to operate the converter in DCM, the maximum power output is defined as the maximum amount of power the converter is able to output in boundary condition, P_{BCmax} , which avoids CCM.

Figure 4.6 shows the current in the primary inductance, L_{pri} , at the boundary condition.

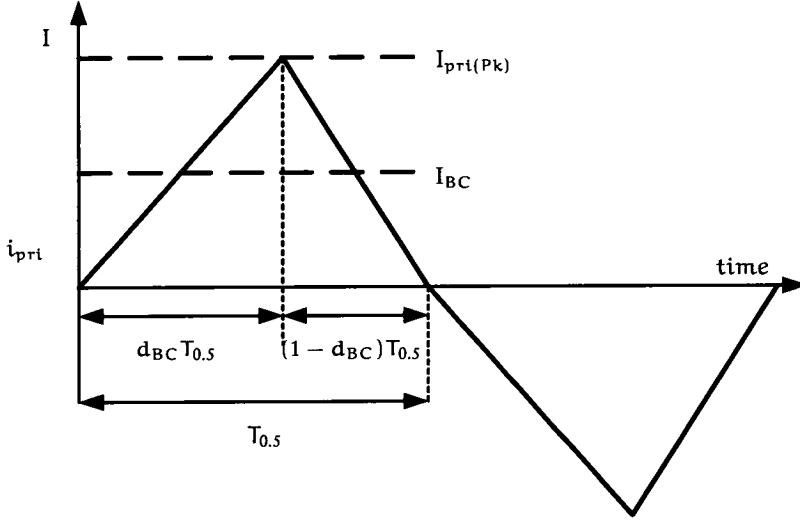


Figure 4.6: Graph of i_{pri} at Boundary Condition

Considering only half of the cycle at the boundary condition, Equation 4.2 describes how V'_{out} forces i_{pri} to fall to zero during the passive interval.

$$-V'_{out} = L_{pri} \frac{0 - I_{pri(pk)}}{(1 - d_{BC})T_{0.5}} \quad (4.2)$$

Average inductor current and duty at boundary condition, I_{BC} and d_{BC} , are defined as follows:

$$I_{BC} = 0.5 I_{pri(pk)} \quad (4.3)$$

$$d_{BC} = M \quad (4.4)$$

Equation 4.2, obtained from Figure 4.6, can be re-expressed as in Equation 4.5 by replacing d_{BC} and V'_{out} according to Equations 4.4 and 4.1.

$$I_{BC} = \frac{(1 - M)M V_{in} T_{0.5}}{2L_{pri}} \quad (4.5)$$

Multiplying Equation 4.5 by V'_{out} , as defined by Equation 4.1, the power obtained, P_{outBC} , at the boundary condition in various setups can be determined (Equation 4.6).

$$P_{outBC} = \frac{(1 - M)M^2 V_{in}^2 T_{0.5}}{2L_{pri}} \quad (4.6)$$

As the converter is designed to withstand output short-circuits, a maximum allowable peak short-circuit current, I_{SC} , must be assigned. The value of I_{SC} then determines the value of L_{pri} required (Equation 4.7).

$$L_{pri} = \frac{V_{in} T_{0.5}}{I_{SC}} \quad (4.7)$$

By substituting Equation 4.7 into Equation 4.6, P_{outBC} can be defined independent of the operating frequency and primary inductance required.

$$P_{outBC} = \frac{(1 - M)M^2}{2} \cdot V_{in} I_{SC} \quad (4.8)$$

Equation 4.8 can be redefined as Equation 4.9,

$$P_{outBC} = K_{SCBC} \cdot P_{SC} \quad (4.9)$$

where K_{SCBC} describes how the output power capability changes with a different modulation index (Equation 4.10).

$$K_{SCBC} = \frac{(1 - M)M^2}{2} \quad (4.10)$$

P_{SC} (Equation 4.11) is the short-circuit power which describes the theoretical capabilities of the selected MOSFET, by substituting V_{in} with V_{DSS} (MOSFET maximum reverse blocking voltage) and I_{SC} with I_{DM} (MOSFET maximum peak pulsed current).

$$P_{SC} = V_{in} I_{SC} = V_{DSS} I_{DM} \quad (4.11)$$

By differentiating Equation 4.10 and setting to zero, an optimal modulation index can be found, M_{opt} (Equation 4.12), giving a maximum value of K_{SCBC} (Equation 4.13).

$$M_{opt} = \frac{2}{3} \quad (4.12)$$

$$K_{SCBCmax} = \frac{2}{27} \quad (4.13)$$

This can be confirmed by plotting a graph of K_{SCBC} against M , Figure 4.7. In addition, this graph also shows power drops more rapidly when $M > M_{opt}$ than when $M < M_{opt}$.

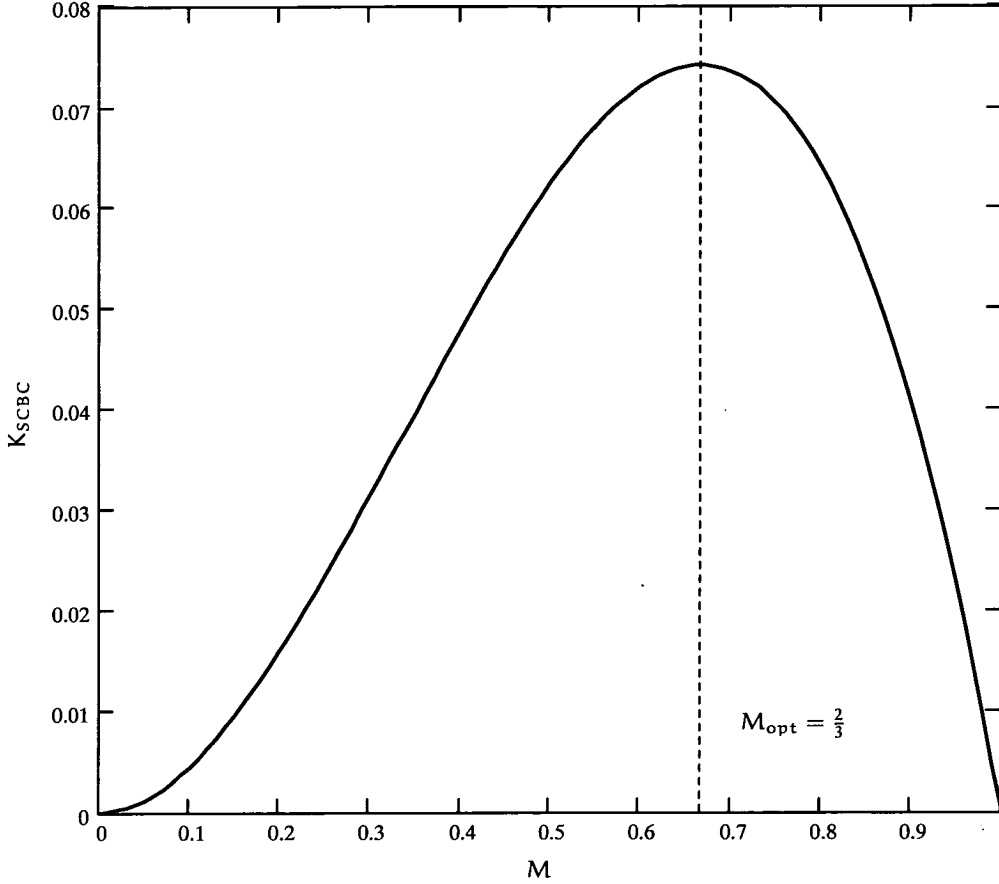


Figure 4.7: Graph of K_{SCBC} Against M

This design assumes a worst case situation, in which the duty increases to a maximum of 1 when the short-circuit occurs thus giving a maximum peak $+I_{SCmax}$ for an initial few cycles (Figure 4.8). This creates an asymmetric current transfer condition which would not allow the main transformer to reset at the end of the switching cycle. The resultant DC offset voltage on the transformer will cause the transformer to saturate with time and a DC blocking capacitor, C_{block} , is required to prevent any DC voltage from building up in the transformer primary winding. C_{block} is also required when designing the converter to operate with voltage mode control as it will prevent any DC offset voltage from building up during normal operation where minor duty fluctuation might cause the peak current during each half of the switching cycle to be unequal. After a few cycles, the peak currents falls to $\pm \frac{I_{SCmax}}{2}$ at the start and end of each half cycle. The actual peak current value should be less because at the onset of the output short-circuit, the output voltage is held up by the

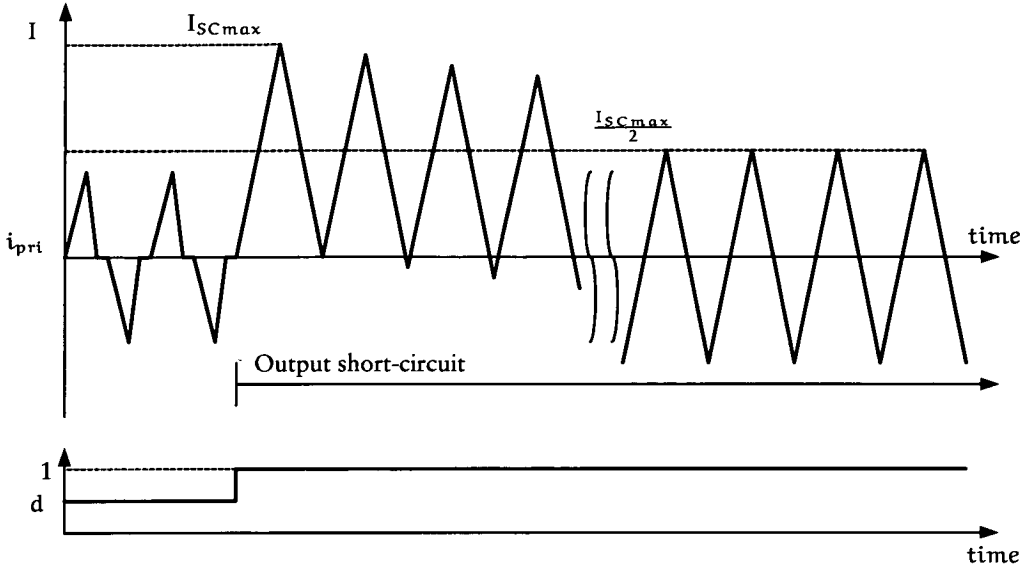


Figure 4.8: L_{pri} Current and Converter Duty for Worst Case Output Short-circuit

output filter capacitors for a few cycles, depending on the value of the capacitors, as it discharges through a low but finite short-circuit impedance. This slows down the duty rise to 1 for a few cycles under voltage mode control, allowing the DC blocking capacitor to rebalance the currents to $\pm \frac{I_{SCmax}}{2}$ (assuming the control circuitry has no duty limiting function).

$$I_{SCmax} = \frac{V_{inmax} \cdot T_{0.5}}{2 \cdot L_{pri}} \quad (4.14)$$

Solving for the given specifications using a turns ratio of 4 gives $I_{SC} = 36.5$ A. Calculating the average primary input currents during an output short-circuit (Equation 4.15) gives $I_{in} = 2.7$ A which, assuming that this occurs at the boundary condition, (Equation 4.16) gives the peak full load current $I_{in(pk)} = 8$ A.

$$I_{in} = \frac{P_{out}}{V_{inmax}} \quad (4.15)$$

$$I_{in(pk)} = \frac{2P_{out}}{V_{inmax}d_{BC}} \quad (4.16)$$

4.3 MOSFET

From Equation 4.17, an initial selection of MOSFETs can be made with the output power pre-defined. Conversely, with a given MOSFET, the maximum output power

Manufacturer	MOSFET Model	Package	V_{DSS} (V)	I_{DM} (A)	I_{D25° (A)	P_{SC} (kW)	P_{BCmax} (kW)
IR	IRFPS43N50K	Super-247	500	190	47	23.5	1.741
IR	IRFP354	TO-247AC	450	56	14	25.2	1.867
IR	IRFP360LC	TO-247AC	400	92	23	36.8	2.726
APT	APT5014BFLL	TO-247	500	140	35	70	5.185
APT	APT50M50L2FLL	TO-264MAX	500	356	89	178	13.19
IXYS	IXFH30N40Q	TO-247	400	120	30	48	3.556
IXYS	IXFX55N50	ISOPLUS247	500	220	55	110	8.148
Infineon	SPW20N60S5	P-TO247	600	40	20	24	1.778

IR - International Rectifier
APT - Advanced Power Technology

Table 4.1: Survey of MOSFETs from Three Manufacturers

of the phase shifted bridge with capacitive filter can be determined.

Re-evaluating P_{outBC} gives:

$$P_{outBC} = \frac{2}{27} V_{DSS} I_{DM} \quad (4.17)$$

Table 4.1 shows a sample of MOSFETs from three manufacturers and their capabilities. It also includes the ideal maximum power output possible, P_{BCmax} , of each MOSFET. Current ratings are inversely proportional to the R_{DSon} values as the current carrying capacity of the MOSFET is determined by the ability of the MOSFET to dissipate the heat generated (values given by manufactures consider only conduction losses) by R_{DSon} within the given MOSFET packaging. Due to $K_{SCBCmax}$ being only $\frac{2}{27}$, this implies that the normal operating currents should easily fall within recommended operating MOSFET drain currents I_{D25° and I_{D100° (ratings of MOSFET drain currents at case temperature of 25°C and 100°C respectively). This is due to the fact that the converter is overrated to survive an output short-circuit. However, it is still important to ensure appropriate heatsinks are used to keep the MOSFET junction temperature below the maximum rated junction temperature in case of a prolonged output short-circuit.

The current readings are only valid at a temperature of 25°C . A more useful value to take would be the values at 100°C , however not all MOSFET manufacturers provide such information. By overrating the MOSFETs to withstand I_{SC} , the MOSFET R_{DSon} value tends to be very small, thus minimising overall conduction loss.

To avoid the converter failing due to the MOSFETs as described in Section 3.5.4, it is advisable to use MOSFETs with fast intrinsic diodes designed to have short recovery times. One such MOSFET is FREDFET (Fast Recovery Epitaxial Diode Field Effect Transistors). These MOSFETs have intrinsic diodes which recover more quickly than ordinary ones, *e.g.* Figure 4.9 shows the reverse recovery currents for a FREDFET by International Rectifier (IRFPS40N50L), another FREDFET by company A and a standard MOSFET [62]. The use of MOSFETs with fast recovery body diodes allows

the converter to extend its operation to higher frequency and minimises the failures when operating at low loads.

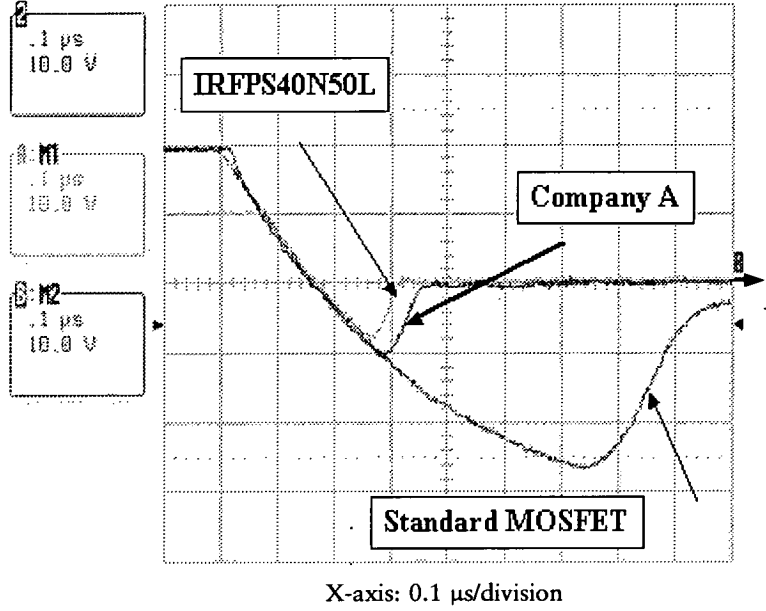


Figure 4.9: Body Diode Reverse Recovery Comparison

The MOSFET chosen for the initial prototype was SPW20N60S5 by Infineon as these were easily available and relatively cheap compared with other MOSFETs. Several units of the other MOSFETs were obtained for efficiency comparison.

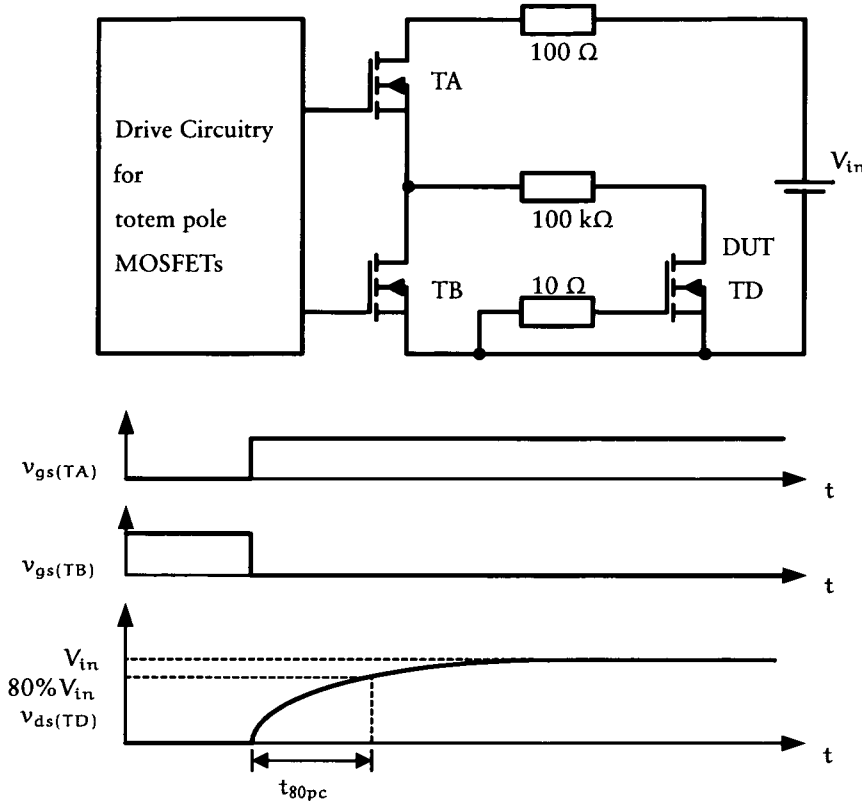
4.3.1 Determination of C_{oss}

The MOSFET output capacitance, C_{oss} is a combination of the drain-source capacitance, C_{ds} , and the drain-gate capacitance, C_{dg} (Equation 4.18).

$$C_{oss} = C_{ds} + C_{dg} \quad (4.18)$$

It is necessary to use the value of C_{oss} and not C_{ds} for calculation because inductive currents are charging both C_{ds} and C_{dg} to raise the v_{ds} to V_{in} for ZVS. In addition, as these parasitic capacitances are based on stored charges within the MOSFET, C_{oss} depends on V_{in} . This means that the value quoted on data sheets might be inaccurate. It has been generally accepted by industry that the effective value of C_{oss} , when used in a ZVS manner, can be estimated approximately by Equation 4.19. The derivation of this equation is shown in Appendix B.

$$C_{ossEquivalent} = \frac{4}{3} C_{ossDataSheet} \quad (4.19)$$

Figure 4.10: Test Setup for Measuring MOSFET C_{oss}

To measure the MOSFET's C_{oss} , a test circuit should be set up as shown in Figure 4.10 [64]. This simple test circuit can be obtained by modifying the Phase Shifted Bridge converter, replacing the transformer with $100\text{ k}\Omega$ resistor, removing MOSFET TC and replacing the gate circuitry of MOSFET TD with a $10\text{ }\Omega$ resistor. By measuring the v_{ds} waveform for MOSFET TB and MOSFET TD, a step waveform for MOSFET TB can be observed and a RC charging waveform for MOSFET TD. By measuring the time taken for v_{ds} on MOSFET TD to reach $80\% V_{in}$ the effective C_{oss} of the MOSFET can be calculated.

$$v_{ds(TD)} = 0.8 \cdot V_{in} = V_{in}(1 - e^{-t_{80pc}/R_t C_{oss}}) \quad (4.20)$$

$$C_{oss} = -\frac{t_{80pc}}{R_t \cdot \log_e(0.2)} \quad (4.21)$$

where t_{80pc} is the time taken for $v_{ds(TD)}$ to reach $80\% V_{in}$.

4.4 Transformer

As the input voltage is required to be stepped up many times to achieve the high output voltage, it is preferable to keep the primary turns ratio to a minimum to reduce overall physical size of the transformer and also to reduce conduction losses. Using Equation 4.12 and 4.1, the ideal value for V'_{out} is 247 V and turn ratio is 4.05. However, as the transformer can only have an integer number of turns, it is not always possible to achieve M_{opt} . Figure 4.11 shows how P_{outBC} varies with turns ratio. As shown previously in Figure 4.7, output power decreases gradually as M decreases from the optimum, hence, it is better to use the turns ratio at or above the optimal rather than to use a turns ratio below optimal, especially in cases where the transformer windings are at a minimal and a fine turns ratio can not be obtained.

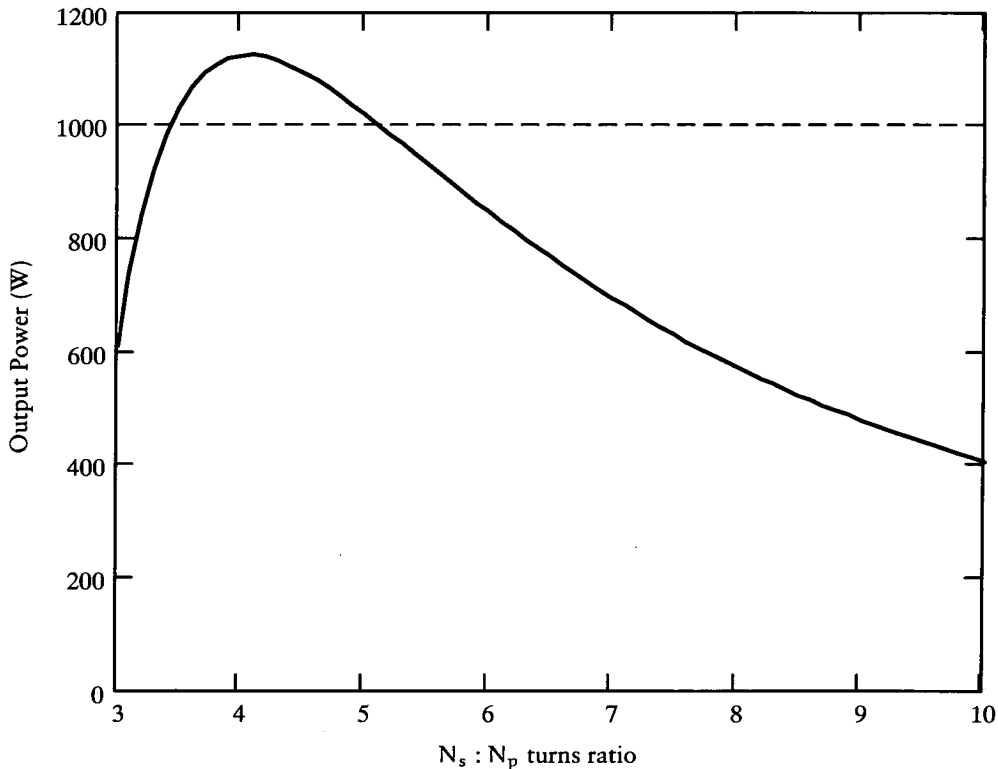


Figure 4.11: Boundary Condition Power Output at Various Transformer Turns Ratio

A transformer can be made from 2 U-cores with the primary and secondary windings located on opposite limbs (Figure 4.12). Due to the large leakage magnetic field created by locating the windings on opposite limbs, the resultant leakage inductance is 200 μ H. This excessive leakage inductance made this form of transformer unsuitable for the converter.

The transformer has to be designed to avoid core saturation. This is done by keeping the flux deviation low ($\pm 10\%$ of the saturation flux density at 100°C , B_{sat100°). This reduces hysteresis core losses which would heat the core causing B_{sat} to decrease.

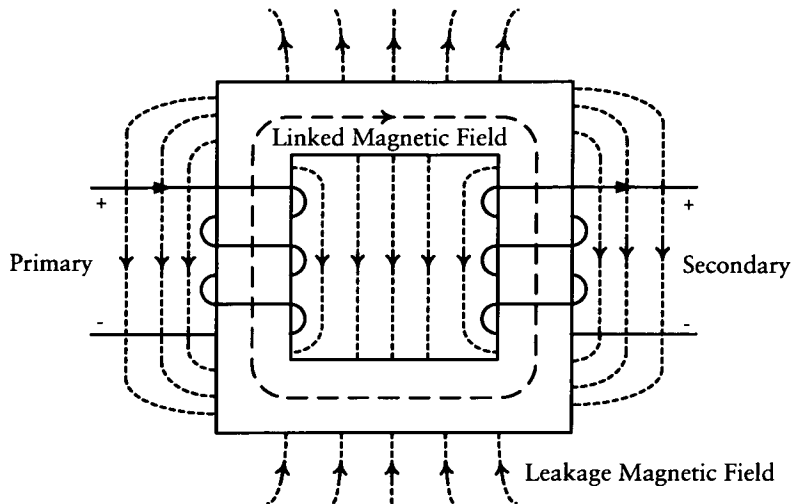


Figure 4.12: U-core Transformer with Excessive Leakage Magnetic Fields

The final core chosen was an EE core made from 2 Ferroxcube E65/32/27 cores of 3F3 high frequency ferrite material (Table 4.2).

4.5 Inductor

To optimise the design, it is best to select the largest inductor value which allows the converter to give the required output power while limiting the maximum peak currents that the switches have to conduct (Equation 4.14). The inductor will then be at a minimal physical size as size is proportional to the maximum amount of energy it can store ($E_L = \frac{1}{2} L_{add} I_{SC}^2$). As discussed in the previous chapter, it is important to rate the inductors using I_{SC} , to calculate the cross section area required of the core, to ensure that the inductor does not saturate when an output short-circuit occurs. From Equation 4.14, the necessary L_{pri} required for the converter is $20.27 \mu\text{H}$. Due to locating the inductor next to the transformer and driving it with an AC source, the losses for the inductor are AC core and winding losses as it does not carry any DC current. Due to the high energy storage requirement during a short-circuit condition, inductors designed using normal ferrite cores were found to be unsuitable as the air gap required for storing the energy is found to be too large. Ferrite inductors should not be designed with large discrete air gaps as the excessive fringing fields make the design non-linear and creates EMI problems. In addition, for prototyping purposes, toroidal cores are preferable as it is difficult to gap a ferrite core to the distance required. The most suitable core material was found to be a Molypermalloy Powder (MPP) core. MPP cores are a type of toroidal core with a distributed air gap made of Nickel, Molybdenum and either iron or copper. It offers a compromise between traditional ferrites, which offers low hysteresis and eddy current losses when operated at high frequencies, and iron powder cores which offer high flux saturation, B_{sat} , for

Parameter	Symbol	Value
Core Material		E65/32/27 3F3
Effective volume	V_e	79000 mm^{-3}
Effective length	l_e	147 mm
Effective area	A_e	540 mm^2
Minimum area	A_{\min}	530 mm^2
Mass of core half	m	$\approx 205 \text{ g}$
Inductance Factor	A_L	$7300 \pm 25\%$
Effective permeability	μ_e	≈ 1590
Air gap		≈ 0
Saturation flux density (100°C)	$B_{\text{sat}100^\circ\text{C}}$	330 mT
Core loss at:		
Frequency	f	100 kHz
Peak Flux Density	\hat{B}	100 mT
Temperature	T	100°C
Core loss		$\leq 10.5 \text{ W}$
Frequency	f	400 kHz
Peak Flux Density	\hat{B}	50 mT
Temperature	T	100°C
Core loss		$\leq 21 \text{ W}$

Table 4.2: Data for Ferroxcube EE65/32/27-3F3 E-core

Parameter	Value
Winding	Primary
Wire gauge	21 SWG insulated
Wire diameter	0.8 mm
Strands	4
Turns	11
Winding	Secondary
Wire gauge	21 SWG insulated
Wire diameter	0.8 mm
Strands	1
Turns	44
L_{leak} estimate	$0.33 \mu\text{H}$

Table 4.3: Winding Data for Main Transformer

Parameter	Value
Core Manufacturer	Sprang Magnetics
Part Number	55441 – A2
Physical Characteristics	
Window area	427mm ²
Cross sectional area	199mm ²
Path Length	107.4mm
Volume	21300mm ³
Weight	171g
Area Product	8.5cm ⁴
Outer Diameter	47.6mm
Inner Diameter	23.3mm
Height	18.92mm
Permeability	14
A_L (nH/turn ²)	32
Wire gauge	21 SWG insulated
Wire diameter	0.8mm
Strands	4
Turns	26
Inductance estimated	19.9μH

Table 4.4: L_{add} Design Data

use in low frequency DC chokes. The design data for L_{add} is given in Table 4.4. The inductors for use in the LDD and LCC auxiliary circuits were also designed using MPP cores (Table 4.5 and 4.6).

4.6 Output Capacitors

The PSBCF converter depends solely on the output capacitors to smooth the output voltage. For conventional converters, a two stage LC filter is used provide output filtering. The current ripple is first filtered using the inductor then the voltage ripple is filtered using the capacitor. This provides low voltage and current ripple on the converter's output. However, in the pulsed TWT radar, the inter-switching-period voltage ripple is of secondary importance in comparison to the inter-pulse voltage ripple (Section 3.2.1). Therefore the capacitors must be sized such that the output voltage droop during a pulse must be within a certain limit ($\approx 0.1\%$) so that the converter is able to charge the output back to the required output voltage by the time the next pulse is activated.

If it is assumed that the TWT load is purely resistive and draws a constant current

Parameter	Value
Core Manufacturer	MMG Neosid
Part Number	Genalex G48V
Physical Characteristics	
Window area	4.3855cm ²
Cross sectional area	106mm ²
Path Length	96.4mm
Volume	10300mm ³
Outer Diameter	39.88mm
Inner Diameter	24.13mm
Height	14.48mm
Permeability	26
A_L (nH/turn ²)	32.5
Wire gauge	21 SWG insulated
Wire diameter	0.8mm
Strands	2
Turns	15
Inductance estimated	7.3μH

Table 4.5: LDD Auxiliary L_{aux} Design Data

Parameter	Value
Core Manufacturer	MMG Neosid
Part Number	Genalex G56VH
Physical Characteristics	
Window area	2.9681cm ²
Cross sectional area	67.9mm ²
Path Length	79.8mm
Volume	542mm ³
Outer Diameter	33.02mm
Inner Diameter	19.94mm
Height	11.18mm
Permeability	26
A_L (nH/turn ²)	25.2
Wire gauge	21 SWG insulated
Wire diameter	0.8mm
Strands	2
Turns	31
Inductance estimated	24 μH

Table 4.6: LCC Auxiliary L_{aux} Design Data

Component	Function	Value
C_T	Oscillator Timing Capacitor	220 pF
R_T	Oscillator Timing Resistor	8.2 k Ω
F_{ocs}	Oscillator Frequency	500 kHz
C_{SS}	Soft Start Capacitor	2.2 nF
T_{SS}	Soft Start Duration	1.1 ms
$R_{delayAB}$	Delay Setting Resistor for PA leg	2.2 k Ω
$T_{delayAB}$	PA Leg Delay Duration	0.23 μ s
$R_{delayCD}$	Delay Setting Resistor for AP leg	2.2 k Ω
$T_{delayCD}$	AP Leg Delay Duration	0.23 μ s

Table 4.7: UC3879 Setup Data

during the pulse. The output capacitors can be assumed to discharge according to the basic equation for a capacitor (Equation 4.22).

$$I_{out} = C \frac{dv}{dt} \quad (4.22)$$

On every TWT radar, a nameplate with the operating specifications of the radar lists the input voltage range. The difference between the upper and lower input voltage should be halved to give an appropriate safety margin and assigned to the dv value in Equation 4.22. The nameplate also lists the averaged operating current of the radar and this is assigned to I_{out} . To ensure that the voltage sag does not exceed the lower limit, dt is assigned a maximum value calculated from the lowest PRF which the TWT is designed to operate. A typical value of the output capacitors at 25 kV is 0.1 μ F.

The output capacitors for the prototype converter are sized such that the capacitive energy stored is equivalent to that stored on a fully rated 25 kV converter (Equation 4.23). This is to enable the start-up conditions to be tested on the converter, where the converter has to supply a large discharge output capacitor, which resembles an output short-circuit.

$$C_{out} = \frac{0.1\mu F \times 25kV^2}{1kV^2} = 66\mu F \quad (4.23)$$

4.7 Other Components

The Unitrode UC3879 control chip is selected for this converter design as it is designed specifically for the traditional Phase Shifted Bridge topology [65, 66]. Components used to program the UC3879 chip to operate the converter at the desired specifications are listed in Table 4.7.

Component	Value
Bootstrap Capacitors	1 μ F tantalum capacitor (15 V)
Bootstrap Diode	UF4006

Table 4.8: IR2113 Setup Data

In addition, as the UC3879 control chip did not provide enough driving capability for the MOSFETs, a high/low side driver chip from International Rectifier is used (IR2113). In addition to driving the MOSFETs, it provides the necessary isolation (up to 600 V) between the control chip and the high side MOSFETs TA and TC without using pulse transformers. The components required to set up the IR2113 are as listed in Table 4.8.

4.7.1 Resonant Transition Setting

The delay timing for each MOSFET of the AP leg, calculated using Equation 3.15, is 109 ns ($C_{AB} \approx 267$ pF, $L_{pri} = 18.06$ μ H). However, a delay timing of twice the calculated value was used (2.2 k Ω) so as to provide a better opportunity to observe the resonant transition interval for the initial prototype.

Although the PA leg of the converter was expected to operate with ZCS turn-on, it was programmed with the same delay time so as to provide adequate dead time to prevent cross-conduction.

A load sensing circuit can be used to replace the delay timing resistor so that the delay timings vary according to the load condition [45]. It is also possible to use automatic ZVS detection circuits between the MOSFET and driver circuitry which switch the MOSFETs on, when either the ZVS condition is detected or when the control chip drives it (Section 7.2.2).

4.8 Chapter Summary

In Chapter 4, a method of design for the PSBCF was presented. The converter is shown mathematically to limit output power when the operation moves into CCM. With this, the theoretical maximum output power of the converter can be determined. This is shown to be dependent on the input voltage, modulation index, primary inductance and frequency. The converter is best operated in DCM as it avoids having power fed back to the converter inputs as occurs in CCM, which is how the converter limits output power. The design is optimised for maximum power transfer at the boundary condition when the modulation index (M) is $\frac{2}{3}$. Using this, the optimal turns ratio for the transformer can be determined. Using Equation 4.17 a preliminary range of MOSFETs can be checked to see if the converter is able to deliver

the required output power at the boundary condition while still falling within the MOSFET maximum peak current specification, during an output short-circuit.

Having narrowed the range of suitable MOSFETs, a final MOSFET with a minimum body diode reverse recovery time should be chosen. The MOSFET should have a low $R_{DS(on)}$ as a result of optimising the design for maximum output power with minimum short-circuit currents. A theoretical and experimental method of determining C_{oss} is presented.

Using Equation 4.7 to calculate the optimal value of primary inductance, short-circuit currents can be kept to a minimum while maintaining high output powers for the converter. If the switching frequency is too low then the converter will have an unreasonably high value of I_{SC} while maintaining high output powers. This design is optimised for maximum output power operating while maintaining best chances of survivability during an output short-circuit. If a short-circuit is unlikely, then smaller inductance values can be used to give higher output powers during normal operation. For this particular application, both the main transformer and series inductor should be overrated to withstand the short-circuit currents, as the converter depends on their summed inductance value for short-circuit protection. Although this results in a larger physical size, this is slightly compensated for as switching frequencies increase.

The experimental converter is controlled by a UC3879 conventional Phase Shifted Bridge Controller by Unitrode and its MOSFETs are driven by two IR2113 High-Low drivers by International Rectifiers. The converter was tested in open loop at 250 kHz with the transition delay duration set by simple resistors. UC3879 is able to accept an external signal to synchronise the switching to either another converter when operating in parallel with other converters for higher powers or for synchronisation with the radar's control circuitry.

Chapter 5

Modelling and Simulation

Why use simulation? Engineers cannot afford to experiment on every single converter by prototyping as it is both time consuming and cost ineffective. Therefore, simulation is a way to experiment with initial designs and reduce simple mistakes in a safe environment before the first prototype is built. Furthermore, some analysis can be performed by the simulation engineer without having to purchase additional specialist equipment.

5.1 Computer Simulation

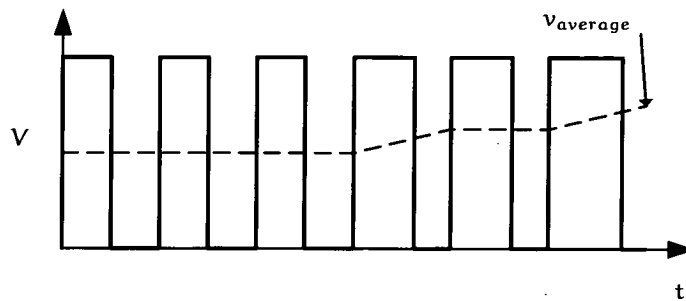
The bulk of simulations in this research are carried out with a variant of the Simulation Program with Integrated Circuit Emphasis (SPICE) package by OrCAD (PSPICE AD version 9.2). It has the ability to carry out mixed-mode simulations. This allows both analogue and digital circuits to be simulated at the same time which is useful for simulating analogue circuits utilising logic circuitry, which SMPS consists of. OrCAD is tried and tested software (originally called PSPICE, produced by MicroSim Corp) and is available on the internet to download for a trial. However, other implementations of SPICE exist, each having slight differences in terms of components implementation (*e.g.* voltage/current sources, switches, and component libraries). Sandler has listed some differences between the main versions of SPICE implemented by three main companies [67]: OrCAD (PSPICE), Intusoft (IsSpice) and Synopsys (HSPICE) and the syntax conversions required when migrating from one to another.

In addition Mathcad is used to perform symbolic calculations. Although Mathcad is unable to perform circuit based simulations, by expressing the circuit in an equation form the analytical performance of the converter can be analysed in time, frequency and other domains. In addition, it can be used to mathematically analyse the converter in a way not possible with SPICE. This may also be performed by Matlab, a

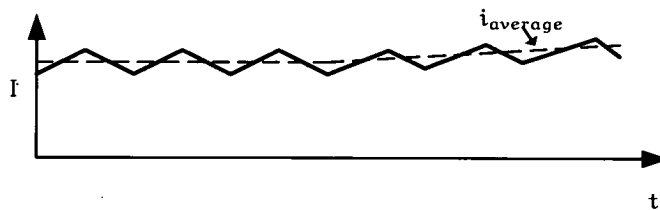
more sophisticated mathematical package utilising matrices to perform mathematical operations.

5.2 Comparison of Averaging Techniques

Generally, PSPICE simulates power electronic circuits which are constructed from discrete semiconductor switches which are switched with a very short period compared to the overall length of simulation, requiring many switching cycles to be computed. This is known as a switch model and it allows detailed events within a switching cycle to be observed. This is time consuming due to the presence of high speed switching events which are discontinuous by nature and simulations frequently suffers from convergence problems. Due to the long computation times required, simulation times for switched models are limited to several milliseconds. In order for the simulation to reach steady-state to obtain sensible readings, C_{out} was reduced by a factor of 100 to $0.66\ \mu\text{F}$. However, PSPICE can also be used to simulate the converter in an averaged mode, where switches and their drive control circuitry are replaced by a behavioural model which performs an averaging of the switched voltage $v_{average}$ and current $i_{average}$ values within a switching cycle, thus greatly reducing computational time (Figure 5.1) and allowing much longer simulation times to be performed with the correct C_{out} value of $66\ \mu\text{F}$.



(a) Switched and averaged voltage waveforms



(b) Ramped and averaged current waveforms

Figure 5.1: Switched and Averaged Voltage and Current Waveforms

When a SMPS topology is averaged, the non-linear portions of the converter, ie. switch and diode, are replaced by an averaged model which has the same voltage and currents as if the values had been averaged over a switching cycle. When averaging

Type of Analysis	Strategy
Power stage semiconductor stress analysis at startup	Switched Models – Accelerate startup by reducing soft-start time constant, if applicable. Use average model transient results as a road map.
Power stage semiconductor stress analysis at steady state	Switched Models – Initialise close to steady state average DC results. Only initialise largest time constants such as output filter L and C, or compensation capacitors.
Power stage stress analysis with short-circuited output	Switched Models – Initialise circuit then dynamically short output with voltage controlled switch.
Line or load transient response	Average Models – Disable under-voltage lockout for correct DC results. Do not initialise circuit. Allow natural DC solution, then run transient analysis using source or switch to cause line or load transient:
Magnetic saturation, short-circuit condition	Switched Models – Initialise circuit for steady state, then short output with a switch.
AC loop stability analysis	Average Models – Allow natural DC solution. Do not use initial conditions. Split feedback loop using a large inductor (blocks AC) then couple AC source signal to input side with a large capacitor.
Input noise filter design – ripple current measurement	Average or Switched Models – Drive the power stage using a voltage source with a fixed duty cycle. Controller with feedback is not necessary.

Table 5.1: Simulation Strategies for Some Typical Power Supply Analysis

the circuit, both the switch and diode are treated as lossless and ideal. The three main techniques of averaging a switched mode power converter are: State Space averaging, PWM switch averaging and Switched Inductor averaging.

5.2.1 State Space Averaged Models

The state space averaging (SSA) technique was first introduced by Middlebrook and Cuk in 1976 [68]. For state space averaged models, a separate circuit model is created for each state of the switch (Figure 5.2).

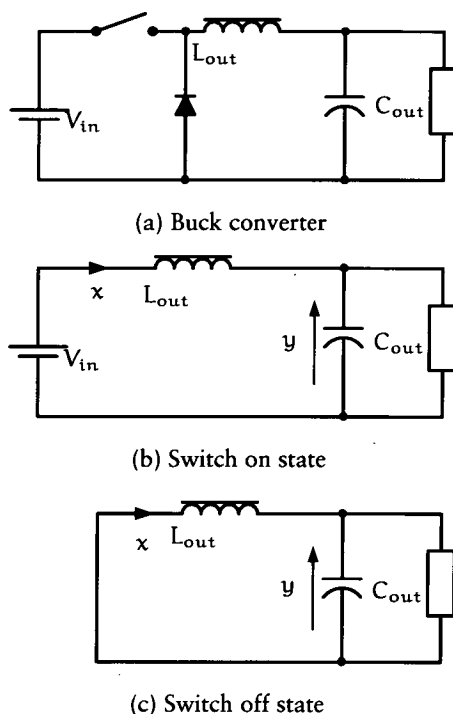


Figure 5.2: State Space Averaging Model

Differential mesh and nodal equations for each of the state variables, inductor current, x , and capacitor voltage, y , during each state are created. These are then averaged by weighting the matrices according to the relative duration of each state. SSA is valid if the time constants of the circuit are very much larger than the switching frequency. Both large and small signal simulations are possible with this model.

5.2.2 PWM Switch Averaged Model

The PWM switch averaged model was first introduced by Vorperian in 1990 [69, 70]. In this model the non linear switch and diode of the circuit is replaced by a model containing three terminals a (active), p (passive) and c (common) (Figure 5.3).

The small (AC) and large (DC) signal transfer function of the switch-diode combina-

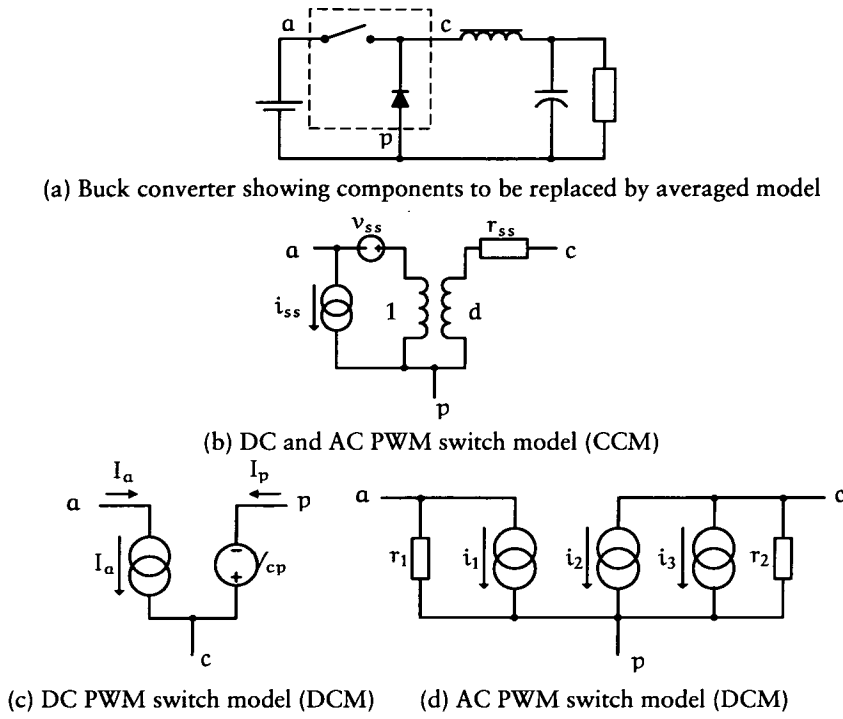


Figure 5.3: PWM Switch Averaging Models

tion are embedded within the three-terminal model for the CCM model. The ideal transformer with 1 : d turns ratio represents the large signal transfer function in CCM. i_{ss} , v_{ss} and r_{ss} are the small signal components of the model and take into account how the small signal AC perturbations on d, R_{esr} of the output capacitor and load affect the small signal analysis of the converter.

Separate AC models (Figure 5.3) exist for both DCM and CCM due to differences in small signal analysis. As a result of including the small signal models within the PWM switch representation, the model is able to give more accurate DCM AC analysis results. When simulating in DCM, separate models exist for AC and DC simulations. To obtain the DC simulations, the average output voltage V_{cp} is calculated from the average input voltage V_{ap} and average input current I_a is calculated from the average passive current I_p according to Equation 5.1. This equation agrees with Equation 3.23 and the model simply models it as an ideal variable transformer with a ratio dependent on the operating condition of the converter.

$$v_{cp} = \mu v_{ac} \quad (5.1a)$$

$$i_a = \mu i_p \quad (5.1b)$$

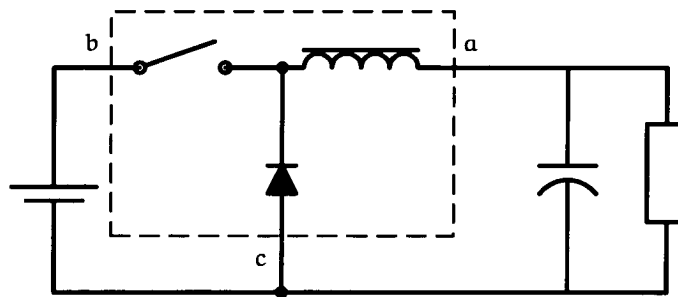
$$\mu = \frac{d^2}{2f_{sw}L} \frac{v_{cp}}{i_a} = \frac{d^2}{2f_{sw}L} \frac{v_{ac}}{i_p} \quad (5.1c)$$

$$\mu = \frac{v_{cp}}{v_{ac}} = \frac{i_a}{i_p} \quad (5.1d)$$

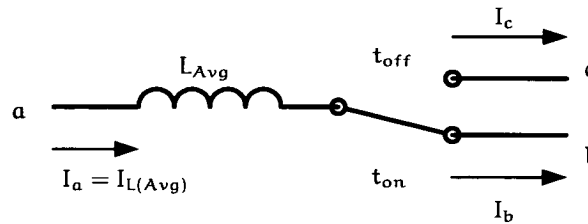
Due to the use of different models for different modes and the ability to better model the converter's AC response compared with the other averaging models [70, 71], the PWM switch averaging technique is best used for AC simulations.

5.2.3 Switched Inductor Model

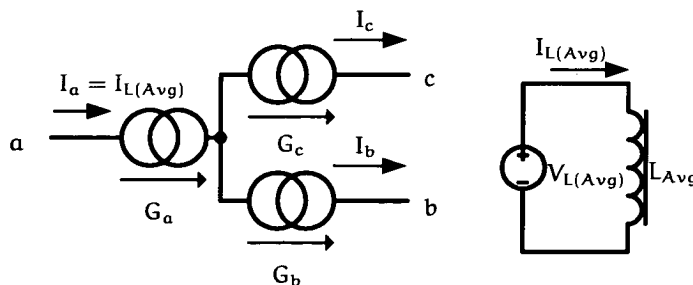
Ben-Yaakov first introduced the switched inductor model (SIM) in 1989 [72]. Ben-Yaakov modelled the traditional 'T-cell' (shown previously in Figure 2.1) as an inductor attached to a single pole double throw switch (Figure 5.4).



(a) Buck converter showing components to be replaced by averaged model



(b) Switched inductor assembly



(c) SPICE implementation of SIM

Figure 5.4: Switched Inductor Averaging Model

The inductor appears on the common terminal, a , and carries the averaged current.

Current entering or leaving each terminal is generated by three dependent current sources, G_a , G_b and G_c . The averaged amount of current entering terminal a is equal to what the inductor carries during a switching cycle (Equation 5.2a). This is simulated by driving the inductor, L , with the average voltage seen across the inductor during the switching cycles, $V_{L(Avg)}$, which is calculated using Equation 5.3.

$$G_a = I_{L(Avg)} \quad (5.2a)$$

$$G_b = I_{L(Avg)} \frac{d_{on}}{d_{on} + d_{off}} \quad (5.2b)$$

$$G_c = I_{L(Avg)} \frac{d_{off}}{d_{on} + d_{off}} \quad (5.2c)$$

$$V_L = (V_a - V_b) \cdot d_{on} + (V_a - V_c) \cdot d_{off} \quad (5.3)$$

Equations 5.2b and 5.2c show what proportion of the averaged current is contributed by terminals b and c. When in CCM, the diode conducts for the entire interval when the switch is off (*i.e.* $d_{off} = 1 - d_{on}$). While in DCM, there is an interval where both switch and diode are not conducting and so $d_{off} < 1 - d_{on}$. Therefore to account for this reduced conduction interval which would affect Equations 5.2 and 5.3, d_{off} in DCM, d_{offDCM} , has to be calculated by solving the inductor current equations. To enable the mode to seamlessly transit from DCM to CCM, d_{off} is assigned the value of d_{offDCM} with a maximum limit of $1 - d_{on}$. With this feature, the model is able to simulate the converter over the full range of load and duty. In addition, the SIM model under SPICE is able to determine its own operating conditions and can thus perform DC (steady state) analysis and is automatically linearised by SPICE for AC (small signal) analysis.

5.3 PSPICE Implementation

5.3.1 Switched Model

To create the full switched model of the phase shifted bridge converter with capacitive filter, models are required for the following: transformer, MOSFET, drive, control and feedback circuitry. With this information, the circuit can be constructed using schematic input as shown in Figure 5.17.

5.3.2 Model of MOSFET

For a particular MOSFET an existing SPICE model may be available from the manufacturer. Sometimes, it might be better to create a model from the parameters supplied in the manufacturer’s datasheets if the supplied model is too complex for the simulations being performed or if no existing models are available. The PSPICE Model Editor software creates new MOSFET models from specification and graphs supplied in the manufacturer’s data sheet. The most important information required from the datasheet are: $R_{DS(on)}$, turn-on charge, output capacitance, switching time and reverse drain current (if present).

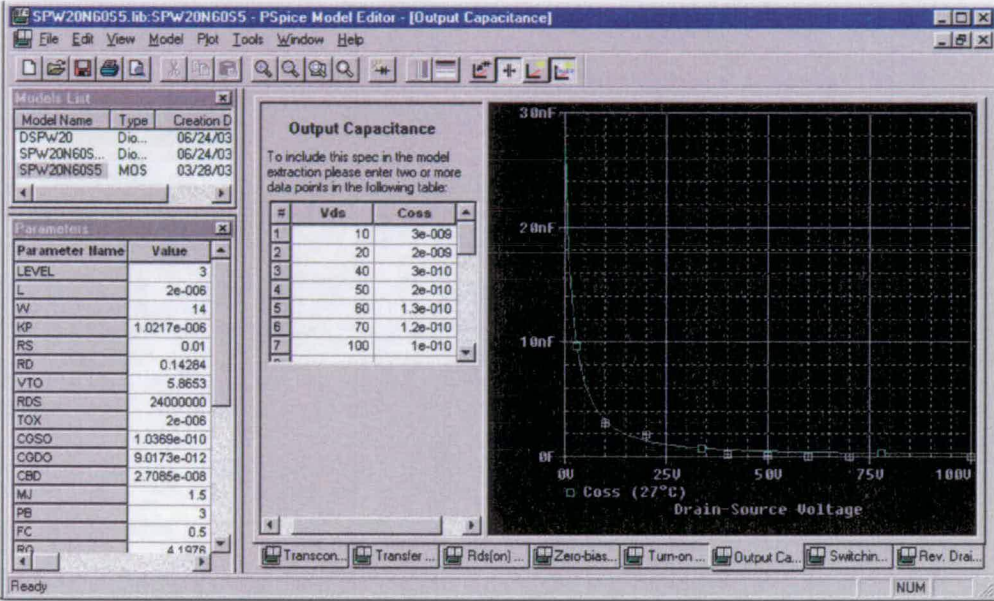


Figure 5.5: PSPICE Model Editor Software Screen Capture

Having created the model, it is then necessary to test the model for the validity of the C_{oss} . The International Rectifier test method (Section 4.3.1) is used to test the MOSFET model and the time it takes for v_{ds} to rise to 80% of V_{in} is noted. Substituting the value into Equation 4.21, the calculated value of C_{oss} for the SPW20N60S5 MOSFET model is found to be 407 pF which is the estimated value calculated using Equation 4.19, thus there is no need to include a separate discrete capacitor in parallel with the MOSFET. It is prudent to double check the value of the capacitance measured with the MOSFET datasheet charts to ensure that the values are sensible. It is better to use a slightly larger value of capacitance, to take into account component drift, so that the converter can be designed to ensure that ZVS occurs even when the actual component value is larger than the initial estimates.

5.3.3 Transformer Modelling

Transformers are used in a wide variety of applications, each having their own particular requirements and operating conditions. As such, different transformer circuit models exist to model the non-ideal characteristics of the transformer. Using an inappropriate transformer model for simulation would mean that the simulation results are not representative of the real circuit. In particular, when designing a soft-switching converter which utilises parasitic components for its basic operation, the various parasitics of the components must be measured and appropriately modelled.

At the basic level, a transformer can be modelled as two coupled inductors, L_1 and L_2 , as done in SPICE, with a coupling coefficient, k , which determines how closely coupled the transformer windings are. The values for the L_1 , L_2 and k can be found using Equations 5.4.

$$L_1 = L_{\text{leak1}} + L_{\text{mag}} \quad (5.4a)$$

$$L_2 = L_{\text{leak2}} + N^2 L_{\text{mag}} \quad (5.4b)$$

$$k = \frac{N L_{\text{mag}}}{\sqrt{(L_{\text{leak1}} + L_{\text{mag}})(L_{\text{leak1}} + N^2 L_{\text{mag}})}} \quad (5.4c)$$

where N is the secondary to primary turns ratio.

However, this model has two main deficiencies; the inability to ‘look into’ the model to examine the detailed effects of the various components, and the use of an abstract variable, k , make it difficult to relate to the actual physical characteristics of the transformer. Therefore, a physical model of the transformer is best suited for this application. From a physical model of a U-core transformer, Figure 5.6 [26], derives an electrical equivalent circuit model of the transformer with N_p and N_s primary and secondary turns respectively. R_{DC1} and R_{DC2} represent the finite DC resistance of the wires used to wind the primary and secondary windings and R_{AC} represent the hysteresis core losses which occur each cycle. L_{mag} represents the magnetising inductance, while L_{leak1} and L_{leak2} represent leakage inductance of the primary and secondary respectively. These inductances are related to the magnetic flux, ϕ_c , ϕ_{lk1} and ϕ_{lk2} , according to Equation 5.5.

$$L_{\text{mag}} = \phi_c \frac{N_p^2}{N_p i_1 - N_s i_2} \quad (5.5a)$$

$$L_{\text{leak1}} = \phi_{lk1} \frac{N_p}{i_1} \quad (5.5b)$$

$$L_{\text{leak2}} = \phi_{lk2} \frac{N_s}{i_2} \quad (5.5c)$$

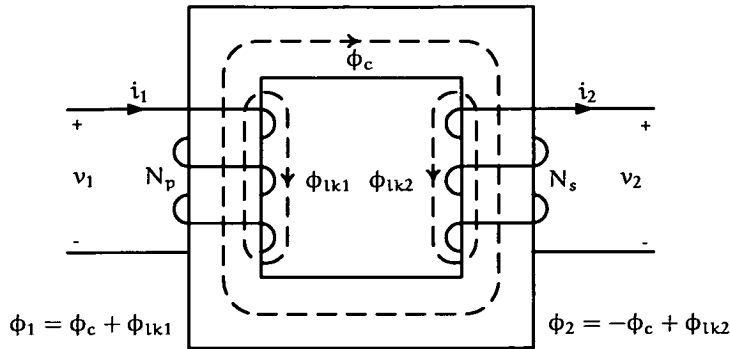


Figure 5.6: Cross Section of a Transformer

This model is adequate for most simulations. To further improve the model for high frequency simulation, the inter-turn capacitance which exists between each turn-on the primary and secondary windings should be included. These parasitic capacitances can be lumped into two discrete capacitors to be included into the transformer model (Figure 5.7). To simplify the model, parasitic components on the high voltage secondary side of the model can be reflected back to the primary side of the transformer (Figure 5.8). Note that the values of L_{leak2} , R_{DC2} and C_{dist2} in Figure 5.7 are not equal to those in Figure 5.8. L_{leak2} and R_{DC2} have to be divided by N^2 and C_{dist2} multiplied by N^2 when reflecting them to the primary side. Collecting all the components on the primary side makes it easier to determine the individual component values and understand what is happening in the transformer during simulation.

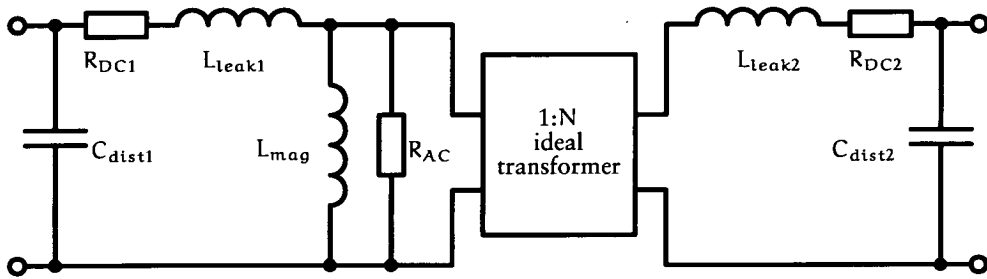


Figure 5.7: Transformer Model

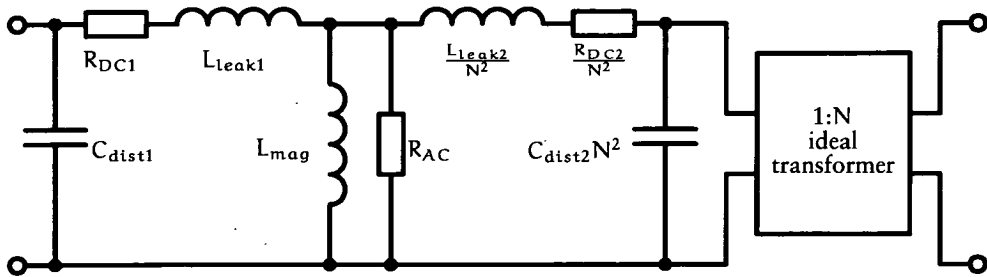


Figure 5.8: Transformer Model with Secondary Components Referred to Primary

5.3.4 Determination of Transformer Parasitic Values

In most textbooks, it is recommended to simply perform open-circuit and short-circuit inductance measurements to determine the various parasitic inductance values. This can be misleading as inductance values can vary with frequency due to the parasitic capacitances, C_{dist1} and C_{dist2} , which affects impedance measurements. Therefore a mathematical model of the equivalent electrical circuit is required to observe the frequencies at which various parasitics dominate.

By creating s-domain equations for each component of the transformer and then combining them according to whether the components are in series or parallel with each other, a transfer function of the transformer can be obtained using Mathcad, from which various impedance plots can be generated.

It can be observed from open-circuit impedance and phase plots in Figures 5.9 and 5.10 that the impedance changes with frequency with several resonant frequencies where the peak and valleys occur.

The transformer parameters can be extracted from the graph obtained from the Magnetics Analyser by performing impedance sweeps across the whole range of frequencies for both the open-circuit (OC) and short-circuit (SC) test. L_{mag} can be assigned with the lowest inductance value, measure at the primary in parallel configuration, at low frequencies up to the first resonant frequency in the OC test. At the first resonant frequency, the resistance value measured is assigned to R_{ac} . With the secondary winding short-circuit, the lowest inductance value below the resonant frequency is L_{lk1} . It is common to lump L_{lk1} and L_{lk2} together and replace it with a single leakage inductance, L_{lk} . At the resonant frequency, L_{lk1} resonates with C_{dist1} as C_{dist2} is shorted. C_{dist1} can be calculated using the LC resonant frequency equation, Equation 5.6.

$$f_{res} = \frac{1}{2\pi\sqrt{L_{res} \cdot C_{res}}} \quad (5.6)$$

To measure C_{dist2} , the primary winding is short-circuited and then the test is repeated with the secondary short-circuited to obtain C_{dist1} . Alternatively, if the resonant frequency of the SC test with the secondary shorted is very high, indicating a very small value of C_{dist1} , then the value of C_{dist2} may be obtained by substituting the first resonant frequency of the OC test and the value of L_{mag} in Equation 5.6.

Having extracted the transformer parameters from the transformer OC (Figure 5.9 and 5.10) and SC (Figure 5.13 and 5.14) measurement waveforms, the parameters were reinserted into the transformer model in Figure 5.8 and the Bode plots were obtained for the OC (Figure 5.11 and 5.12) and SC (Figure 5.15 and 5.16) tests. The

measured and transformer model waveforms match reasonably well and show that the proposed model is adequate for use up to the converter's transformer frequency of 250 kHz.

Parameter	Method of extraction
R_{DC1}	DC resistance measure measurement of primary winding
R_{DC2}	DC resistance measure measurement of secondary winding
L_{mag}	Open-circuit test: Lowest inductance value (parallel configuration) before the first resonant frequency
R_{AC}	Open-circuit test: Resistance measurement (parallel configuration) at the first resonant frequency
L_{leak}	Secondary winding short-circuit test: Lowest inductance value (series configuration) before the first resonant frequency
C_{dist1}	Secondary winding short-circuit test: Use value of L_{leak} measured and first resonant frequency to determine value of C_{dist1}
C_{dist2}	Primary winding short-circuit test: Repeat the L_{leak} test with the primary winding shorted and use the inductance value obtained and the first resonant frequency to determine the value of C_{dist2}

Table 5.2: Summary of Transformer Parameter Extraction

Open Loop PSPICE Simulation

To simulate the circuit shown in Figure 5.17 in an open loop configuration, the operating duty required has to be first calculated using Equation 3.24. The voltage sources V_a , V_b , V_c and V_d are gate drives for the bridge MOSFETs with the setup shown in Table 5.3.

	Pulsewidth	Delay
V_a	$T_{0.5} - \text{Delay}_{AB} - (t_{rise} + t_{fall})$	0
V_b	$T_{0.5} - \text{Delay}_{AB} - (t_{rise} + t_{fall})$	$T_{0.5}$
V_c	$T_{0.5} - \text{Delay}_{CD} - (t_{rise} + t_{fall})$	$(d \cdot T_{0.5}) + (\text{Delay}_{CD} - \text{Delay}_{AB})$
V_d	$T_{0.5} - \text{Delay}_{CD} - (t_{rise} + t_{fall})$	$((1 + d) \cdot T_{0.5}) + (\text{Delay}_{CD} - \text{Delay}_{AB})$

Table 5.3: MOSFET Gate Drive Settings for Open Loop PSPICE Simulation

Closed Loop PSPICE Simulation

The simple MOSFET gate drive voltage pulse sources are replaced with a PSPICE digital circuit implementation of the UC3879 control chip (Figure 5.20). Within the original circuit a square pulse waveform at switching frequency is generated from the ramp waveform which is running at twice switching frequency. To simplify matters, the 0.5 duty square pulse waveform, necessary for the function of the logic circuitry,

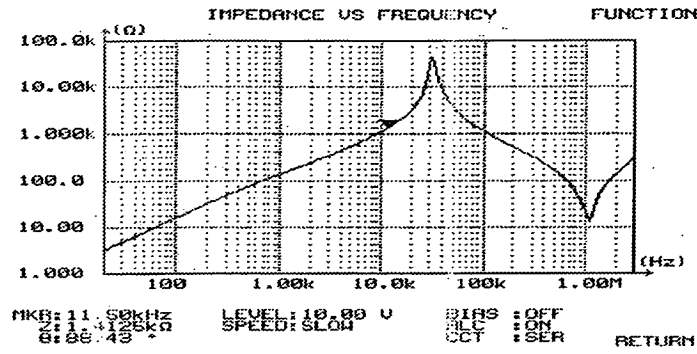


Figure 5.9: Magnetics Analyser Impedance Magnitude Measurement Printout for Prototype Transformer (OC)

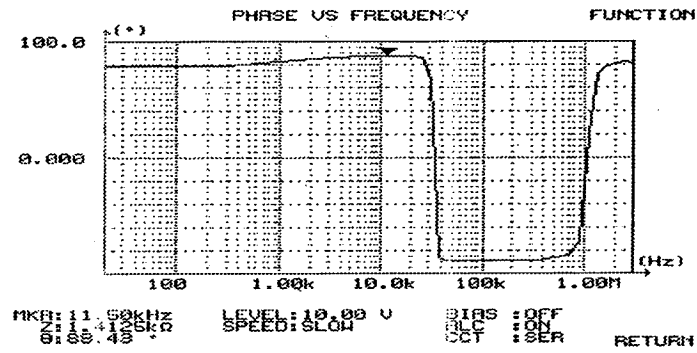


Figure 5.10: Magnetics Analyser Phase Measurement Printout for Prototype Transformer Model (OC)

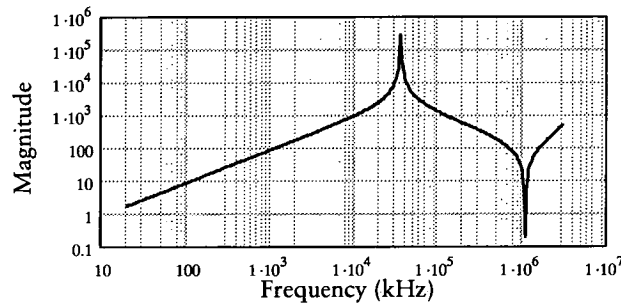


Figure 5.11: Mathcad Impedance Magnitude Plot for Transformer Model (OC) with Parasitic Inductances and Capacitances.

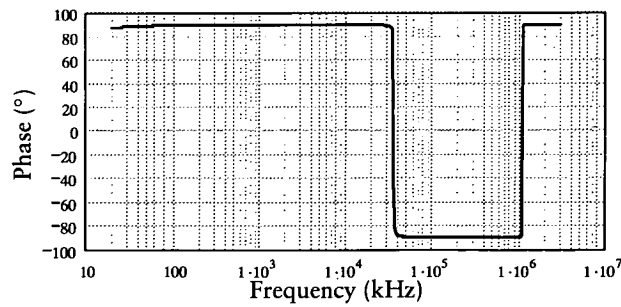


Figure 5.12: Mathcad Phase Plot for Transformer Model (OC) with Parasitic Inductances and Capacitances

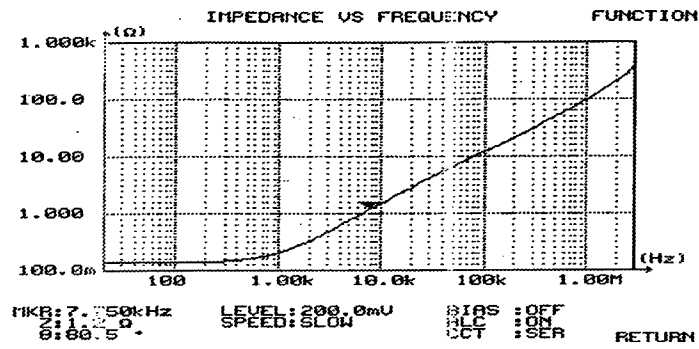


Figure 5.13: Magnetics Analyser Impedance Magnitude Measurement Printout for Prototype Transformer (SC)

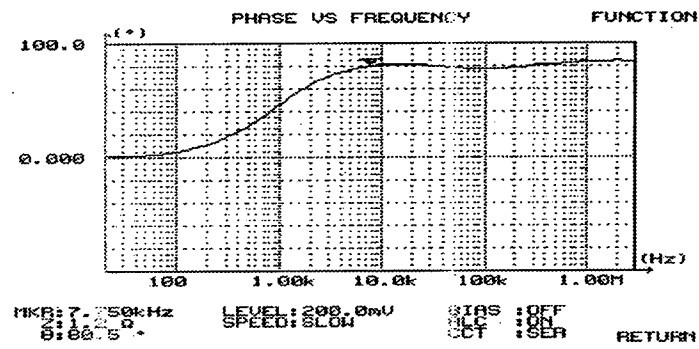


Figure 5.14: Magnetics Analyser Phase Measurement Printout for Prototype Transformer Model (SC)

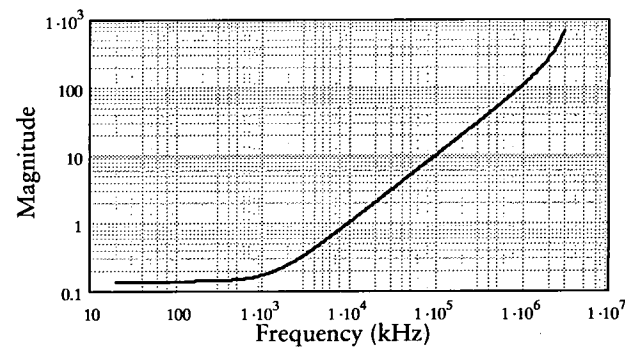


Figure 5.15: Mathcad Impedance Magnitude Plot for Transformer Model (SC) with Parasitic Inductances and Capacitances

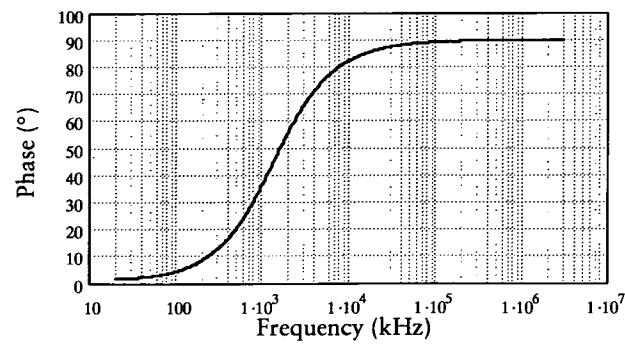


Figure 5.16: Mathcad Phase Plot for Transformer Model (SC) with Parasitic Inductances and Capacitances

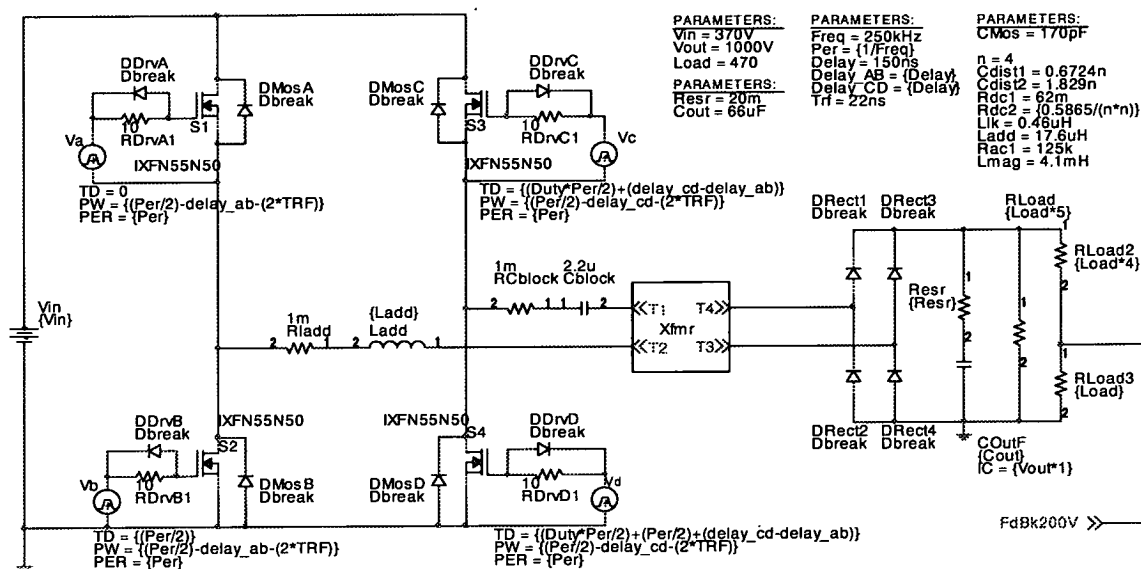


Figure 5.17: PSpICE Schematic of Open Loop PSBCF without Auxiliary Circuitry

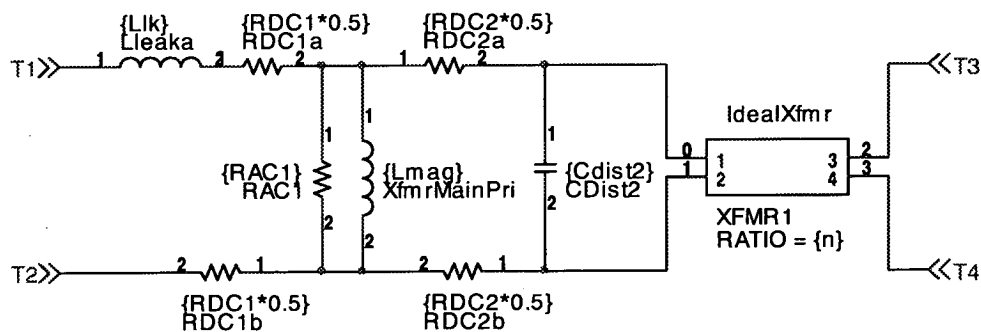


Figure 5.18: Non-ideal Transformer PSPICE Model Referred to Primary

is generated independently but is synchronised to the oscillator / ramp generator input. The circuit generates drive A from the square wave generator and drive B from the inverse signal. The amount of phase shift for drive C and D is generated by the duration where V_{PWM} is lower than $V_{oscillator}$.

The simulation is able to perform open loop simulation by feeding a voltage signal between 1.3 V to 4.2 V to vary the duty from 0 to 1. The reason this is modelled as such is that the oscillator / ramp signal input (0 V - 2.9 V) within the chip is shifted by 1.3 V. This allows the converter to shut down with zero phase shift when the duty signal falls before 0.9 V. To close the loop, an error amplifier needs to be introduced into the circuit Figure 5.21.

A simple error amplifier model can be created using a voltage controlled voltage source with the output value set to:

$$V_{out} = (V(+) - V(-)) \times 31622 \quad (5.7)$$

where 31622 (90 dB) is the amount of voltage gain the UC3879 internal error amplifier offers. This should be able to function as an ideal error amplifier for most purposes. For a more accurate model of the error amplifier, the one presented in [73] is chosen. The model includes other non-idealities of the real error amplifier such as a Gain-Bandwidth limitation and current source and sink limitations. This provides a more accurate simulation when the error amplifier is operated in an unconventional manner, *e.g.* it prevents an infinite gain feedback network situation when the error amplifier is operated without any feedback compensation components. In addition, AC analysis of the error amplifier network will also be more accurate since it takes the gain-bandwidth product and gain information to model a single pole response of a non-ideal error amplifier. Following the specifications of the UC3879 chip, the values listed in Table 5.4 are used for the model.

Parameter	Value
Gain	31622 (90 dB)
First Pole	316 Hz
Current Sink (Max)	2.5 mA
Current Source (Max)	1.3 mA
V_{out} (Min)	0.5 V
V_{out} (Max)	4.7 V

Table 5.4: Values Used to Configure Operational Amplifier Model Within UC3879 Model

The location of the first pole is calculated using the gain-bandwidth product and maximum gain available (Equation 5.8).

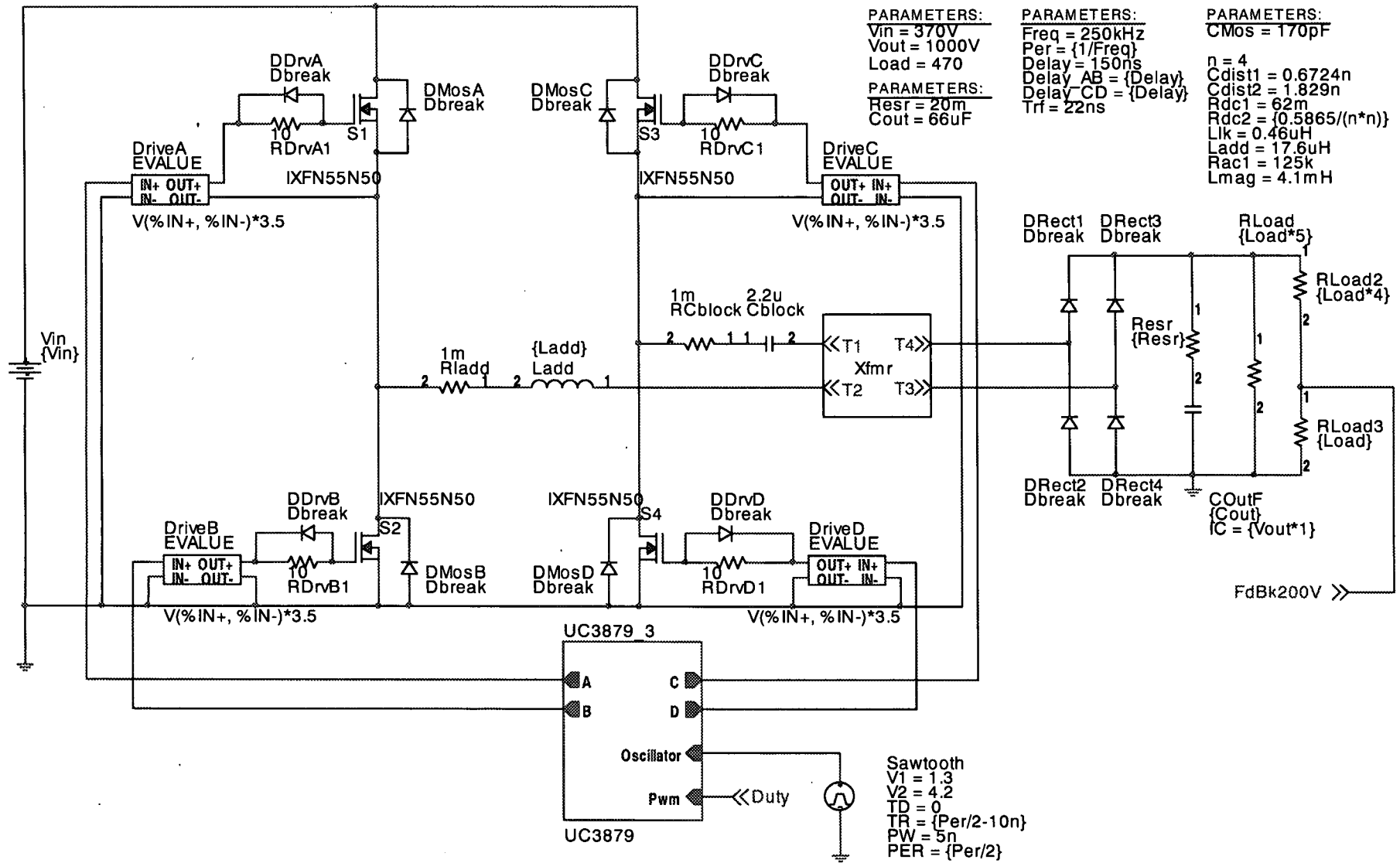


Figure 5.19: PSPICE Schematic of Closed Loop PSBCF without Auxiliary Circuitry

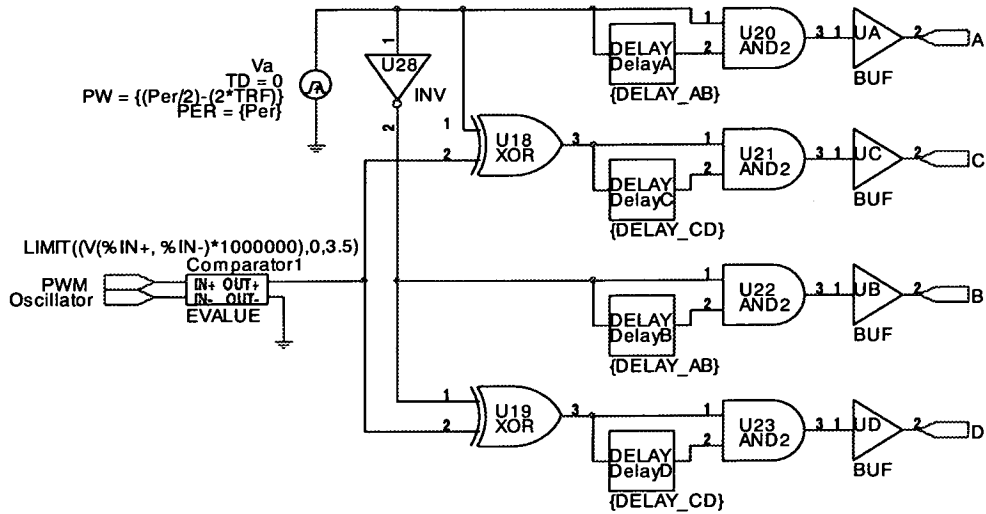


Figure 5.20: PSPICE Digital Circuitry for Producing Phase Shifted Driving Waveforms

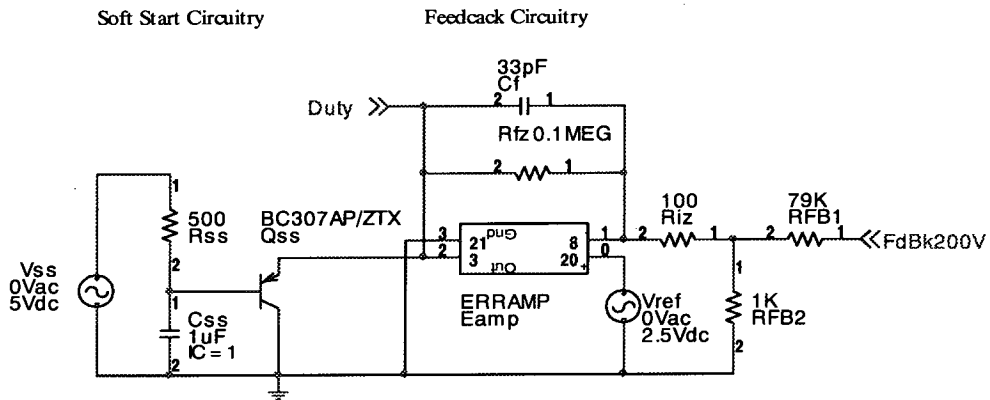


Figure 5.21: Feedback Circuitry for Closed Loop Simulation

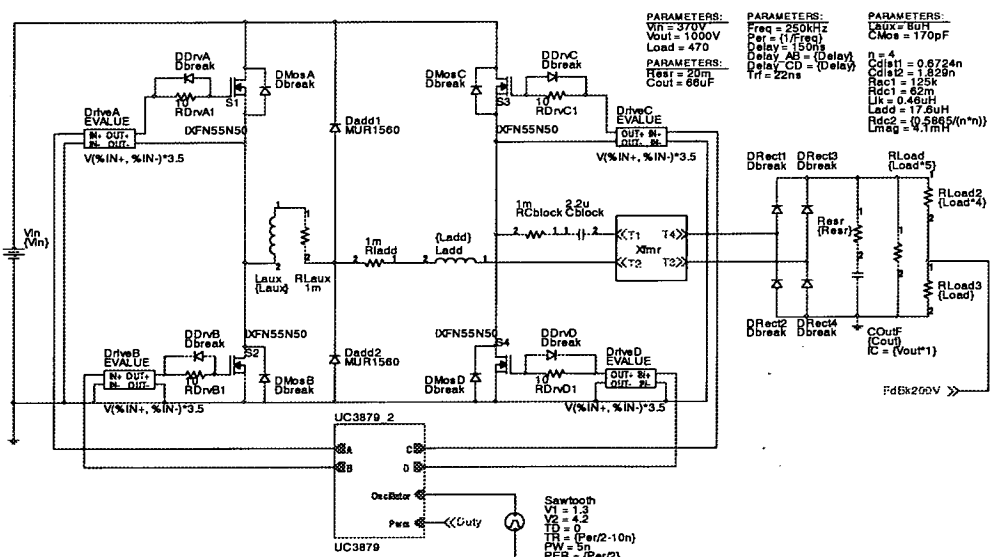


Figure 5.22: PSPICE Schematic of Closed Loop PSBCF with LDD Auxiliary Circuit

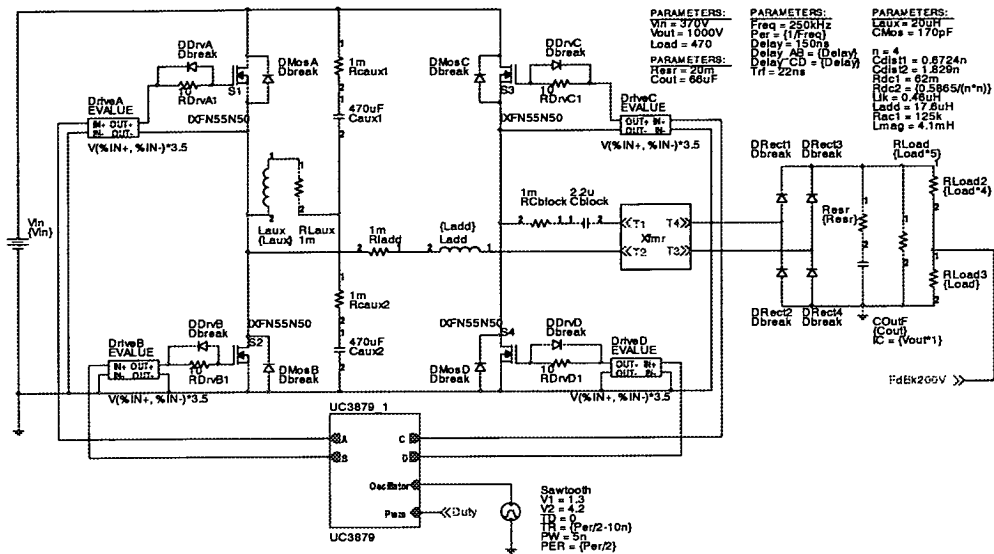


Figure 5.23: PSPICE Schematic of Closed Loop PSBCF with LCC Auxiliary Circuitry

$$f_{\text{pole}} = 10^{\log_{10}(\text{GainBandwidthProduct}) - (\text{Gain(dB)}/20)} \quad (5.8)$$

As seen from Figure 5.21, an external soft-start circuitry can be added to the simulation as in the real prototype by connecting it to the error amplifier output or compensation pin. This allows the converter models, both transient and averaged, to perform accurate start-up simulations.

5.4 Mathcad Simulation

Although Mathcad is more of a symbolic calculator than a dedicated circuit simulator, it is useful for plotting graphs which can be described using equations (*e.g.* Figure 4.7), particularly when certain component values or operational parameters can be altered to observe and compare changes (*e.g.* Figures 4.1 and 4.4). Graphs of complicated systems can still be plotted if the individual components can be described and combined together, nesting the simple equations within the complex ones (*e.g.* Figure 5.11). However, Mathcad is not optimised to handle large complicated systems, and is therefore limited to simple steady state waveforms when used to generate converter waveforms.

5.5 SIM Transient Average Model Equations

The Switched Inductor model, mentioned in Section 5.2.3, is particularly suitable for use in modelling the capacitive filtered Phase Shifted Converter as the inductor is encapsulated within the model which replaces the four Bridge MOSFETs and transformer in the converter (Figure 5.24).

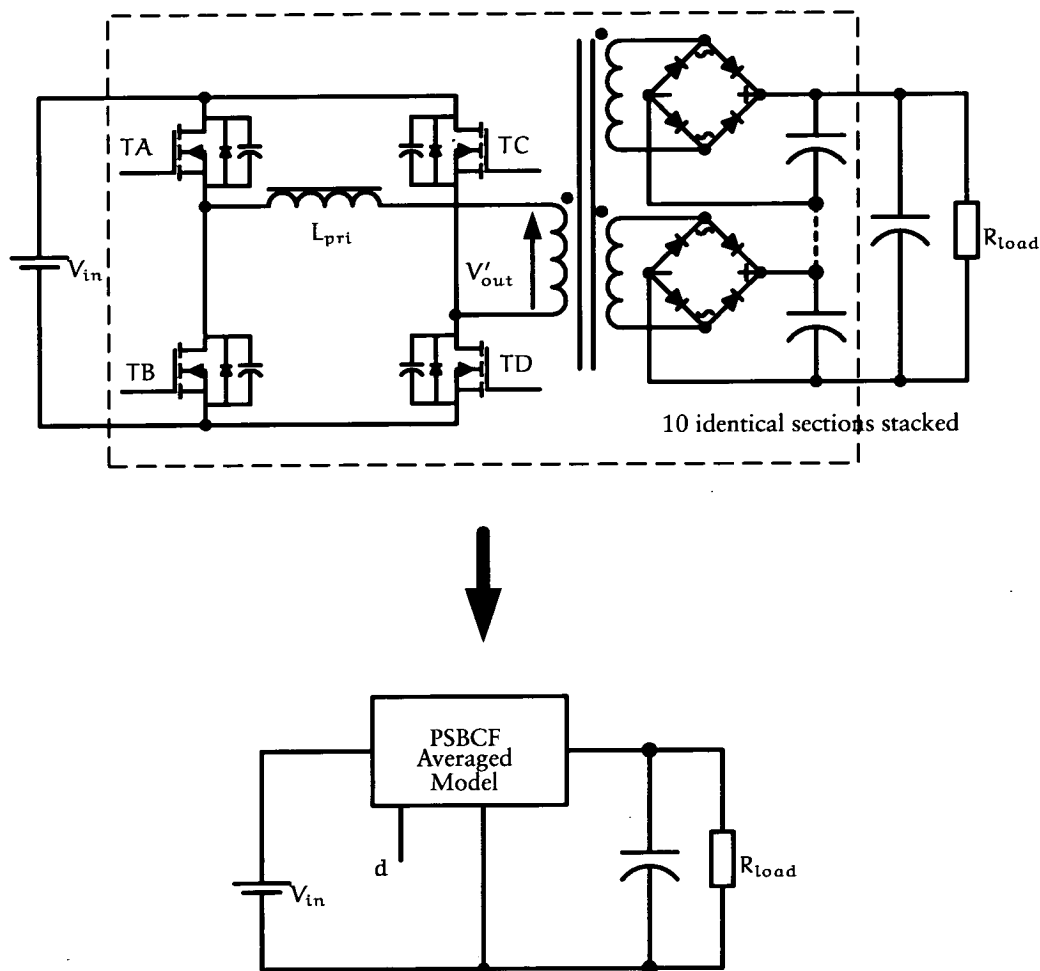


Figure 5.24: Averaged Model of PSBCF

As the converter is utilising an output capacitive filter, it is the output voltage which is assumed to be constant and not output current as used in the PWM switch model. To utilise the PWM switch averaged model for the phase shifted bridge would require the inductor to be placed in the usual LC filter manner and an output voltage signal fed back into the model. This would enable calculation of a voltage which would give the necessary averaged output currents flowing through the inductor. The problem with this is that it is not reflective of the true nature of the converter as most of the inductance is essentially located with the bridge MOSFETs in series with the transformer. Thus it is non-intuitive to convert a capacitive filtered converter into an LC filtered one in order to utilise the model.

The average currents across the inductors during the two modes are derived in Chapter 3.

For DCM operation:

$$I_{pri} = \frac{1}{2} \cdot (V_{in} - V'_{out}) d^2 \frac{T_{0.5}}{L_{pri}} \quad (5.9)$$

$$I'_{sec} = \frac{1}{2} \cdot (V_{in} - V'_{out}) d^2 \frac{T_{0.5} V_{in}}{L_{pri} V'_{out}} \quad (5.10)$$

$$I_{sec} = \frac{1}{2} \cdot (V_{in} - V'_{out}) d^2 \frac{T_{0.5} V_{in}}{L_{pri} V'_{out} N} \quad (5.11)$$

For CCM operation:

$$I_{pri} = \frac{1}{4} \cdot T_{0.5} V'_{out} \frac{(2d \cdot V_{in}^2 - d^2 V_{in}^2 - V'_{out}{}^2)}{L_{pri} V_{in}^2} \quad (5.12)$$

$$I'_{sec} = \frac{1}{4} \cdot \frac{T_{0.5}}{V_{in}} \cdot \frac{(2d \cdot V_{in}^2 - d^2 V_{in}^2 - V'_{out}{}^2)}{L_{pri}} \quad (5.13)$$

$$I_{sec} = \frac{1}{4} \cdot \frac{T_{0.5}}{V_{in}} \cdot \frac{(2d \cdot V_{in}^2 - d^2 V_{in}^2 - V'_{out}{}^2)}{L_{pri} N} \quad (5.14)$$

As a result of using a capacitive filter, the output voltage is smoothed but the voltage step up is no longer that of the turns ratio, as with a normal LC filtered converter. This set of equations can be reduced to half by just considering secondary currents alone and multiplying then by the appropriate gain between the output and input voltages.

In the original model, the d_{fall} sub-period was simply limited to a maximum of $(1 - d)$ to allow for transition between DCM and CCM. However, to extend this to the PS bridge, yet another variable would have to be created to monitor the d_{prec} sub-period which would have to be limited to $0 < d_{prec} < d$. In order to simplify matters and ease understanding, another approach is used. Note that in all converters, the boundary condition must be satisfied by both DCM and CCM equations. For the PSBCF converter the boundary condition equation is as shown in Equation 5.15.

$$I_{BC} = \frac{1}{2} \cdot (V_{in} - V'_{out}) \frac{V'_{out}}{V_{in}} \frac{T_{0.5}}{L_{pri}} \quad (5.15)$$

$$I'_{\text{secDCMnom}} = (d \frac{V_{\text{in}}}{V'_{\text{out}}})^2 \quad (5.16)$$

$$I'_{\text{secCCMnom}} = \frac{(d \cdot V_{\text{in}}^2 \cdot (2 - d) - V_{\text{out}}'^2)}{2(V_{\text{in}} - V'_{\text{out}}) \cdot V'_{\text{out}}} \quad (5.17)$$

To create a simulation which will transfer smoothly from one mode to the other, first normalise both DCM and CCM equations with the boundary condition equation (Equation 5.16 and 5.17 respectively). Then limit the normalised DCM equations to ≤ 1 and the normalised CCM equations to > 1 and multiply the equations to create a combined DCM/CCM equation with a smooth transition. Next the current value is de-normalised by multiplying the combined DCM/CCM equation with the boundary condition (Equation 5.15). Finally, the input current can be obtained from the de-normalised equation by the instantaneous value of M (Equation 3.23) and the output current by dividing the current by the transformer turns ratio.

To implement this in PSPICE, voltage sources representing the normalised DCM and CCM equations and boundary conditions are created. The mathematical operation for the equations are carried out using the voltage dependent voltage source generator in PSPICE. This new averaged model differs from the switched inductor model technique employed by Ben-Yaakov as the model does not actually use an inductor in the PSBCF model but calculates its effect using mathematical equation. This is due to the fact that L_{pri} is a bi-directional inductor and is able to immediately change its averaged current value from each half switching cycle to next which the original inductor in the switched inductor model is unable to.

Using the same method, the peak L_{pri} information can be included in the averaged PSBCF model. The listing for the PSPICE averaged PSBCF model is included in Appendix C.

5.6 Small Signal Model

The small signal AC analysis can be directly performed on the PSBCF SIM model relying on PSPICE to linearise the model having obtained the DC operating point [74]. In addition, the DCM PWM switch AC model could also be used as the converter predominantly operates in DCM.

AC simulation can be carried out using the new averaged PSBCF model by inserting a 1 V AC voltage source between the output of the error amplifier and the duty input of the averaged model (Figure 5.25). Due to the lack of an output inductor, the transfer function of the converter has to be the output current with respect to either duty

(shown in Figure 5.26) or the input voltage.

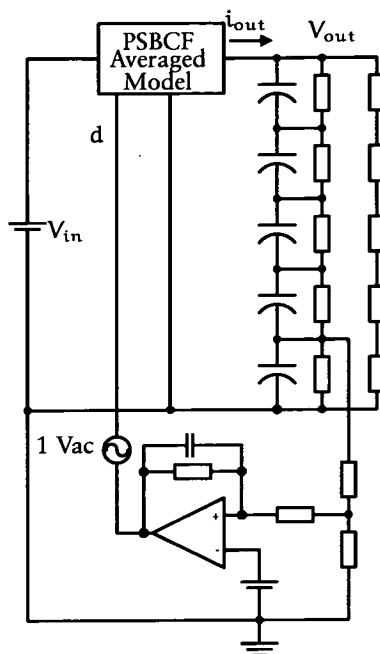


Figure 5.25: PSPICE AC Simulation Schematic for PSBCF Averaged Model

5.7 Arc Simulation Using Low Resistance Load

The simplest way to simulate an arc within PSPICE is to use a switch with a low resistance connected across the output load triggered to switch on when an arc is required (Figure 5.27). The 'on' resistance of the arc switch model is set to $1\ \Omega$ to draw enough current such that the output voltage would collapse in less than half a switching cycle to stress the converter under test and to continue drawing current as long as the switch is kept on. Unfortunately this is only a crude model and will not model the arc or spark gap with much accuracy. However, it does give an insight into how the converter will operate when faced with a large load increase such as a output short-circuit.

A better way for simulating an arc or triggered spark gap is to use the model of the surge arrester developed in [75]. However, due to the lack of detailed specifications of the surge arrester used by BAe Systems, it has not been possible to create a reasonable model of this surge arrester. Therefore, short-circuit simulations were carried out using the simple resistive model.

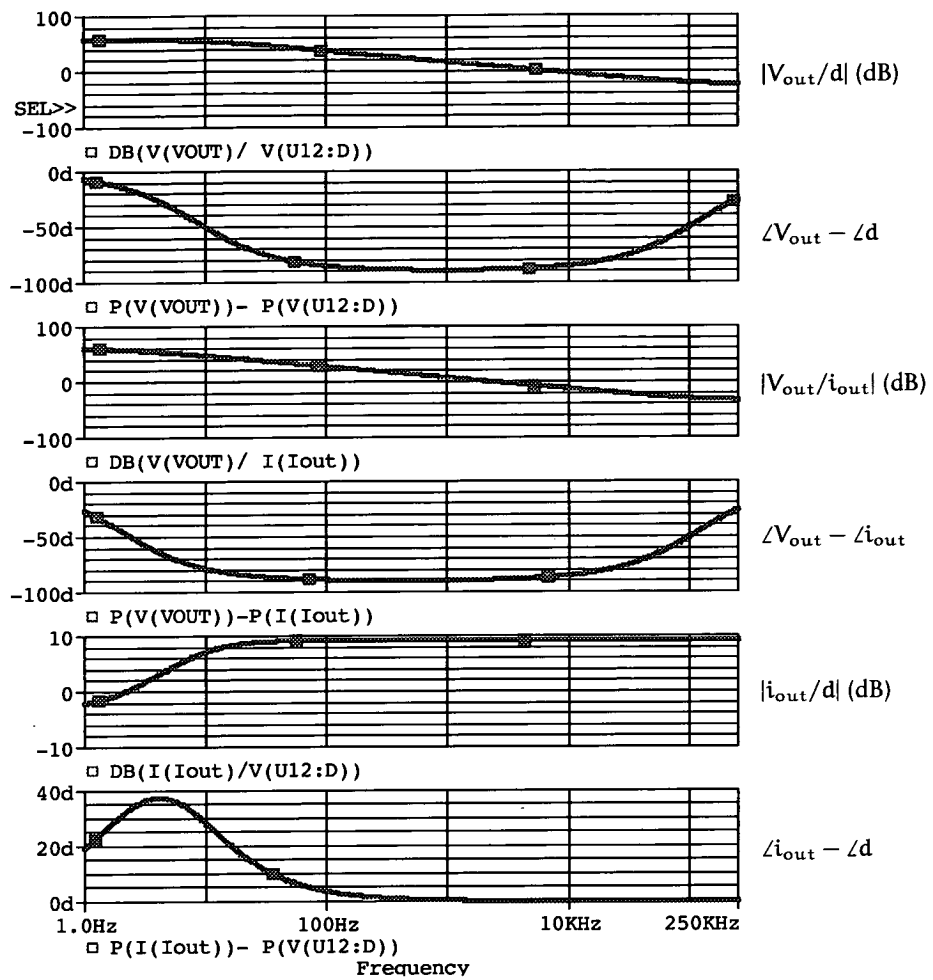


Figure 5.26: PSPICE AC Simulation Results for PSBCF Averaged Model

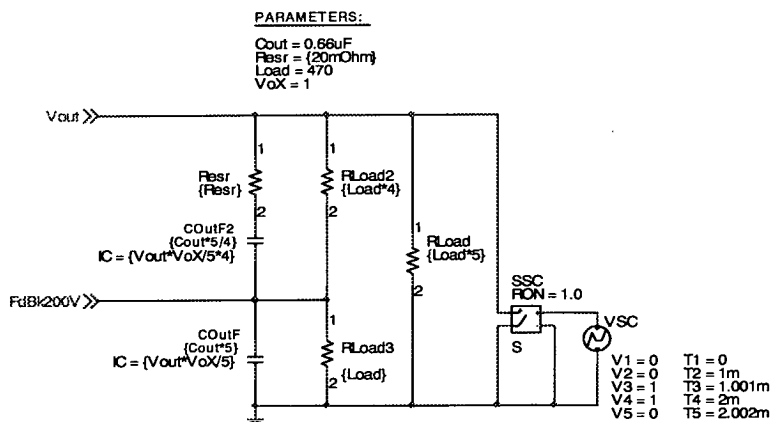


Figure 5.27: PSPICE Output Load and Resistive Short Circuit Model

5.8 Chapter Summary

Chapter 5 explains the need for simulation, compares the difference between averaged and switched models and states the benefit of each. Three popular averaging techniques are introduced, namely, State-Space Averaging, PWM Switch Averaging and Switched Inductor model. A new averaged model for the PSBCF was created, based on the Switched Inductor model concepts, by treating L_{pri} as a switched inductor and encapsulating it within the averaged model.

In order to obtain a reasonably accurate transient switched model of the converter under PSPICE, models of the various components have to be created. Simplified MOSFET models can be created with data from the manufacturer's data sheet, using the model editor which accompanies PSPICE, or a detailed model can be obtained directly from the manufacturer if available. C_{oss} for the model can be tested using the test circuit as with the actual MOSFET (Figure 4.10).

Due to the high frequency operation of the converter, the transformer should be characterised properly in order to obtain an accurate simulation. This is achieved by performing AC impedance measurements of the prototype transformer while sweeping across a range of frequencies in both open and closed circuit. These Bode plots were then compared to those produced by the simulation model, which uses parasitic values extracted from prototype measurements, to ensure an accurate simulation of the transformer's response at various frequencies. A model of the UC3879 control chip is created to enable both open and closed loop simulation of the converter.

Chapter 6

Testing and Results

6.1 Background

After designing the capacitive filtered phase shifted bridge, a prototype converter was built to verify the theory and PSPICE simulations. The converter was designed and built on three separate printed circuit boards (PCBs), consisting of a power converter, high voltage rectification and control circuitry stage. The power converter PCB contains the main bridge MOSFETs, with the ability to integrate the LDD and LCC auxiliary circuits to aid soft switching of the PA leg. The main transformer is also located on the power converter PCB. The secondary windings are terminated with a connector which enables the high voltage bridge rectifier PCB to be connected to it. The loads and output filter capacitors are housed in a grounded metal casing for safety concerns. Two parallel loads of five $470\ \Omega$ resistors connected in series, drawing an equivalent power of $425.5\ \text{W}$ each at $1\ \text{kV}$, are cooled by mounting the resistors on a large heatsink ($0.33\ \text{K/W}$) with six fans providing forced cooling.

Simulation results for the various converters subjected to a $1\ \text{ms}$ output resistive arc are also presented. Included in this section is a simulation for the CFB (model provided by Frank Fisher of BAe Systems) for performance comparison. The PSBCF averaged model arc simulation results are presented for verification.

Results for switching transition simulations using various PSPICE MOSFET models are presented to show the limitations of the simplified Orcad PSPICE models used.

Finally, the steady state voltage, current, efficiency and temperature readings are presented.

6.2 Hardware Prototype

The converter was build with the specifications listed in Section 4.2.1 according to the design method presented in Chapter 4. The final schematic and component list for the prototype converter is as shown in Figure 6.1 and Table 6.1. R_{DelayAB} and R_{DelayCD} values had to be increase to 4.6 k Ω due to parasitic inductance present in the MOSFET package causing a delayed turn-off effect. This is discussed and shown in detailed in Section 6.4.1. The inductance values listed in Table 6.1 are the final measure inductance value and differs slightly from the values estimated in Section 4.5.

The converter was designed such that the auxiliary circuits could be integrated into the PSBCF converter without requiring much modifications to the main converter board.

The final PSBCF prototype with no auxiliary circuit is as displayed in Figure 6.2. The PSBCF converter when used with either the LDD or LCC auxiliary circuit is as shown in Figure 6.3 and 6.4 respectively. As the converter is operating in open loop, the V_{200} feedback voltage signal from the output loads is currently unused. The white sticky foam tape visible on heatsinks, inductors and output resistors are used to attach the thermocouples to the point of interest for measuring component temperature.

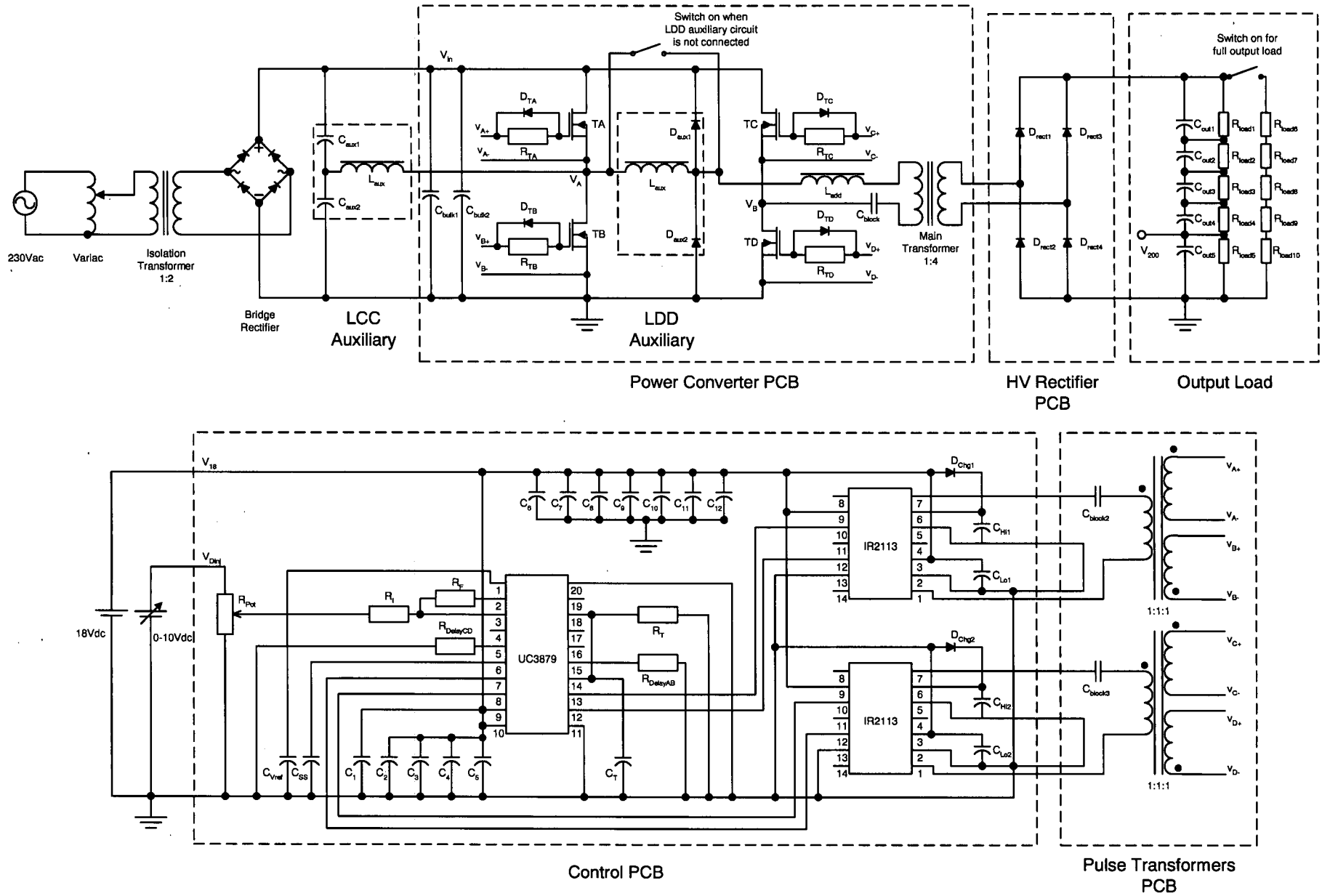


Figure 6.1: Schematic of PSBCF Prototype

PSBCF Prototype Component Values	
LCC Auxiliary	
C_{aux1}, C_{aux2}	330 μ F, 250 V, electrolytic
L_{aux}	20 μ H
LDD Auxiliary	
D_{aux1}, D_{aux2}	MUR1560
L_{aux}	8 μ H
Power Converter PCB	
C_{bulk1}, C_{bulk2}	470 μ F, 450 V, electrolytic
TA – TD	SPW20N60S5
$D_{TA} - D_{TD}$	1N4148
$R_{TA} - R_{TD}$	10 Ω , $\frac{1}{2}$ W
C_{block}	3.2 μ F, 400 V, polystyrene
L_{add}	15.1 μ H
HV Rectifier PCB	
$D_{rect1} - D_{rect4}$	STTA512F
Output Load	
$C_{out1} - C_{out5}$	330 μ F, 250 V
$R_{load1} - R_{load10}$	470 Ω , 100 W
Control PCB	
R_{Pot}	1 k Ω , $\frac{1}{2}$ W
R_F, R_I	100 Ω , $\frac{1}{4}$ W
$R_{DelayAB}, R_{DelayCD}$	4.6 k Ω , $\frac{1}{4}$ W
R_T	6.7 Ω , $\frac{1}{4}$ W
C_T	0.22 nF, ceramic
C_{SS}	2.2 nF, ceramic
C_{Vref}	0.01 μ F, 50 V, ceramic
C_1, C_2	33 μ F, 25 V, tantalum
$C_3 - C_5$	0.01 μ F, 50 V, ceramic
C_6	47 μ F, 36 V, tantalum
C_7, C_8	33 μ F, 25 V, tantalum
$C_9 - C_{12}$	0.1 μ F, 50 V, ceramic
D_{Chg1}, D_{Chg2}	UF4006
C_{Hi1}, C_{Hi2}	4 μ F, 36 V, tantalum
C_{Lo1}, C_{Lo2}	4 μ F, 36 V, tantalum
C_{block2}, C_{block3}	2.2 μ F, 50 V, ceramic

Table 6.1: Components for Prototype PSBCF Converter Schematic Shown in Figure 6.1

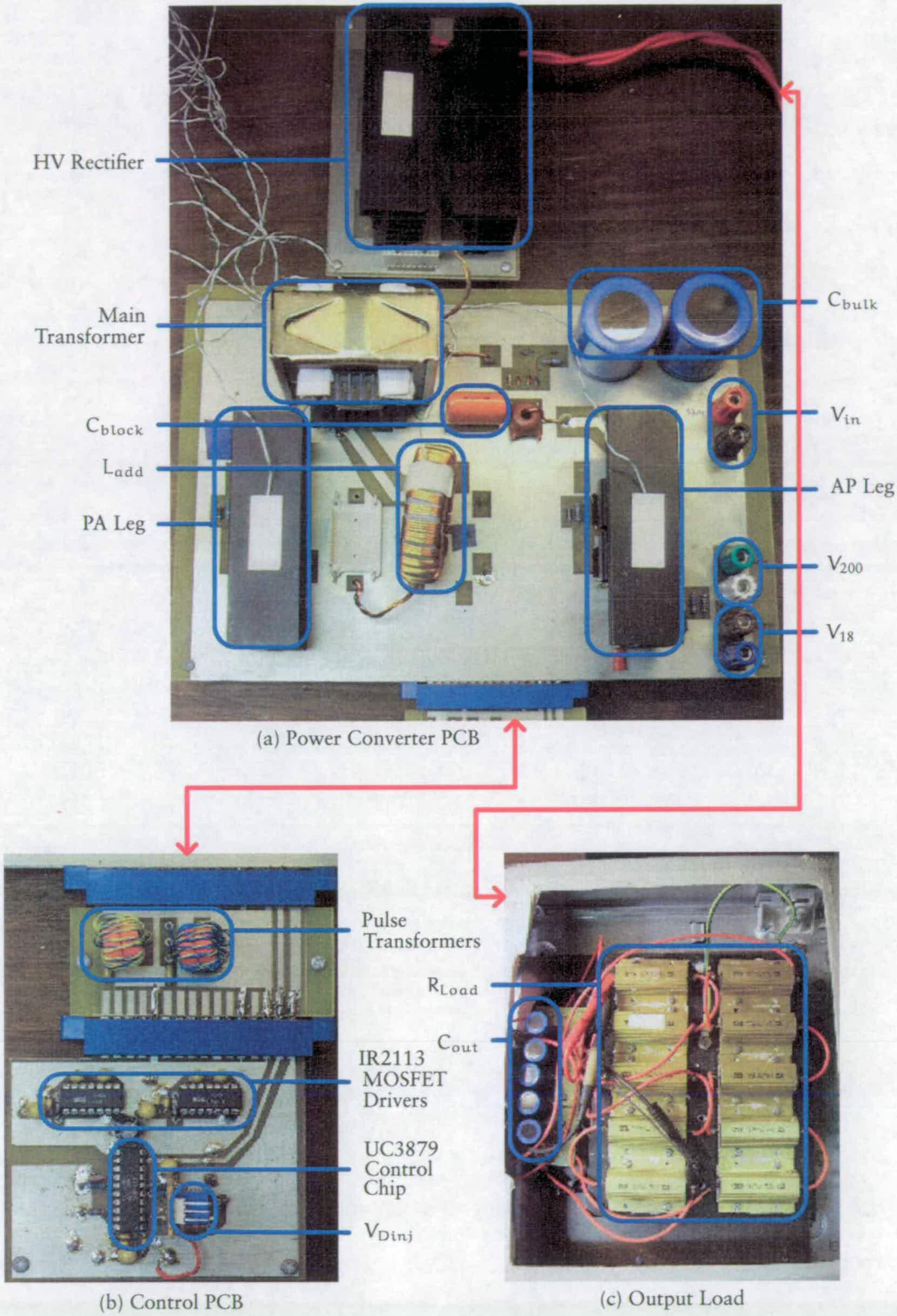


Figure 6.2: Photograph of PSBCF Prototype with No Auxiliary Circuit

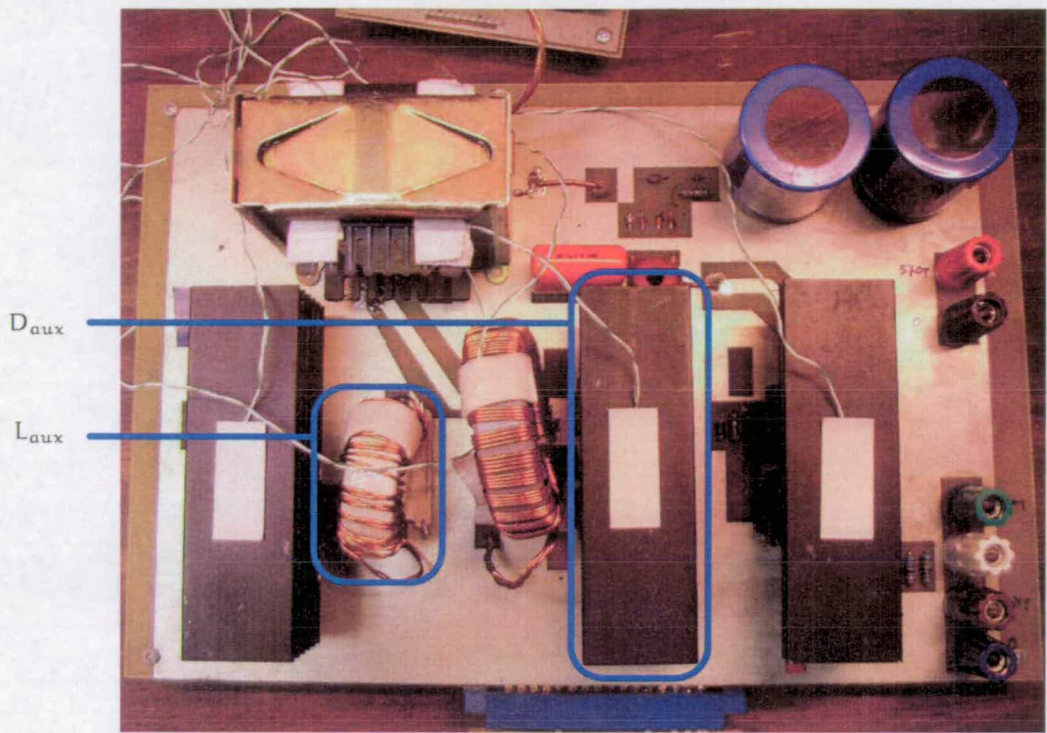


Figure 6.3: Photograph of PSBCF Prototype with LDD Auxiliary Circuit

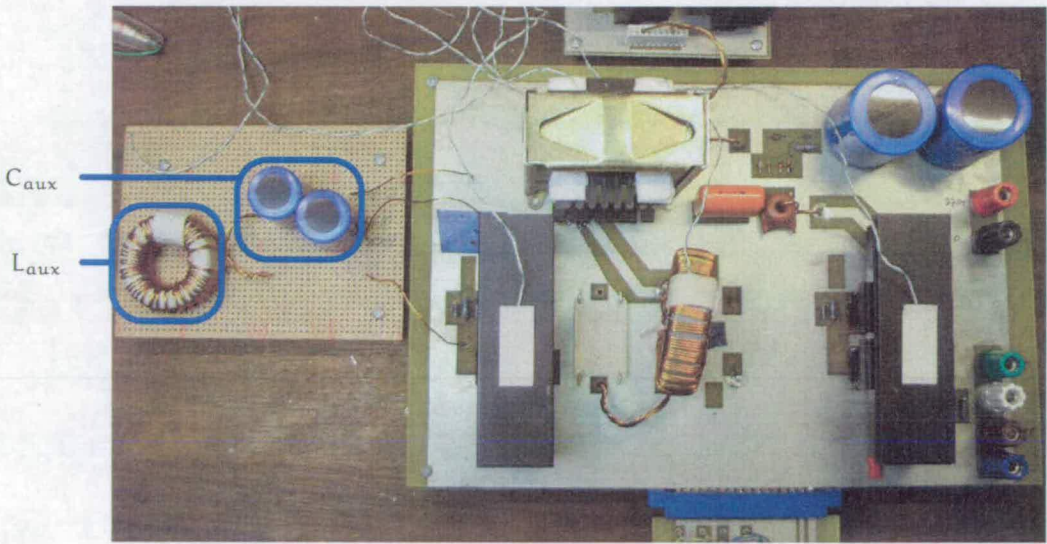


Figure 6.4: Photograph of PSBCF Prototype with LCC Auxiliary Circuit

6.2.1 Prototyping Difficulties

Due to a lack of experience designing PCBs for high frequency, high power circuit boards, many problems were encountered when producing a working prototype. Most of these problems were EMI related. Although the converter is a soft switched converter with $\frac{dv}{dt}$ limited by resonant voltage transitions and $\frac{di}{dt}$ limited using dis-

continuous conduction current mode, the high input voltage and output power would still result in a significant amount of EMI being generated, especially at full output power. These problems could manifest as irregular driving waveforms caused by the UC3879 internal timing oscillator experiencing electromagnetic interference or noise picked up by oscilloscope probes which appears on the voltage waveforms. This is most significant during attempts to start up the converter under closed loop, due to large inrush currents on the input. The noise picked up by the UC3879 causes erratic operation which triggers the over-current protection to activate which results in a hiccup start up condition and the converter is unable to self regulate and achieve full output voltage. The over-current protection should not be de-activated as this has resulted in converter failure caused by MOSFET failure. This is most likely due to the spurious turn-on of the MOSFETs, either due to noise on the control chip or at the gates of the MOSFET, resulting in cross-conduction. In addition, due to the lack of an ideal DC voltage source for V_{in} , the large inrush currents during start-up causes a voltage sag, due to the impedance of the isolation transformers and variac used, which in turn causes duty to be increased to compensate, resulting in a positive feedback situation.

Measures were taken to solve most of the problems encountered. Ground planes were used extensively to provide a low impedance grounding point to reduce noise conduction. It would be also ideal have a power plane too. Unfortunately, only dual layer PCB could be manufactured in house and so a ground plane was selected instead. The ground leads of the oscilloscope probes were kept to minimum length. Excess lengths of the ground lead were wrapped around the probe to minimise pick-up of electromagnetic noise. Wires carrying DC voltages were wrapped around ferrite cores with a couple of turns to reduce high frequency noise. The use of jumper wires was avoided where possible (*e.g.* by connecting signals between the control PCB to the power converter PCB using PCB connectors). Unfortunately, due to the high output voltage nature of the converter it was necessary to physically separate the high voltage sections of the converter from the mid and low voltage sections. To reduce noise pick-up, the positive and return current carrying wires were twisted together. Low equivalent series resistance (ESR) capacitors ($C_1 - C_{12}$) are also used to filter noise on the input supply of the integrated circuit chips. Capacitors with the lowest ESR (multi-layer ceramic) were located nearest to the chip, while those with higher ESR were situated further away. Unfortunately, the feedback loop could not be closed successfully and the tests were carried out using open loop control instead.

6.3 Test Procedure

The converter's control circuit was first set up to enable duty control in open loop so that the output voltage can be controlled manually. This is achieved by breaking the

feedback loop and injecting a voltage into the input resistor, R_I , of the UC3879 internal error amplifier. As it is difficult to make fine adjustments on the potentiometer, R_{Pot} , a variable DC power supply, V_{Dinj} (0 – 10 V), was connected to R_{Pot} instead. R_{Pot} was adjusted such that the full range of duty could be controlled by varying V_{Dinj} from 0 V to 10 V.

The approximate duty for the converter for the particular output load is first calculated and the duty is then set using V_{Dinj} . V_{in} , initially kept at 0 V, is slowly increased by adjusting the variac until $V_{in} = 370V$. V_{Dinj} is then adjusted until the output voltage is 1 kV.

6.3.1 Steady-state Operation

Each configuration of the converter was tested at half load (425.5 W) and full load 851 W for its steady-state performance. The main operating waveforms are presented along with the results of the PSPICE simulation for the particular configuration to validate the PSPICE circuit model (Figures 6.5 – 6.26). Four sets of steady state waveforms were captured for each test for the PSBCF converters with auxiliary circuits and three for the PSBCF without auxiliary circuit.

The first set consists of the main transformer waveforms for the converters. Voltages of the midpoints of both the PA (v_A) and AP (v_B) leg along with their difference ($v_A - v_B$) which shows duty as a result of the phase shifting of the PA and AP waveforms. The current waveform for the transformer primary winding (i_{pri}) is also shown.

The next set of waveforms shows the voltages and currents for the auxiliary inductor and primary of the transformer.

The final two sets of waveforms show the lower MOSFETs (TB and TD) as they are about to be switched on. The current entering the midpoints of the bridge legs are shown. This is the current which discharges the C_{oss} of the lower MOSFET preparing it for ZVS. The MOSFET drain-source ($v_{ds(TX)}$) and gate-source ($v_{gs(TX)}$) voltage waveforms are included. Additional results are include in Appendix A for further reference.

PSBCF without Auxiliary Circuit

The PSBCF converter without auxiliary circuit could not supply full output load at the required voltage due to MOSFETs failure from excessive switching losses. The voltage oscillation on v_A and v_{pri} waveform just prior to the active period is an indication that there was some form of resonant transition present but that was unable to charge v_A to V_{in} for ZVS when running at half load (Figure 6.5). Unfortunately

this is not clear in the PSPICE waveform in Figure 6.6. The loss of ZVS for the PA leg is much more visible in Figures 6.7 and 6.8 where it can be seen that $v_{ds(TB)} \approx v_{in}$ when $v_{gs(TB)}$ goes high. Gate pulse transformers with bipolar gate pulse signals are used to drive the MOSFETs of the prototype PSBCF with no auxiliary circuits as explained later in Section 7.1.

MOSFETs on the AP leg continue to switch with ZVS as can be seen by the $v_{ds(TD)}$ falling to zero when TD is turned on in both Figures 6.9 and 6.10.

LCC Auxiliary Circuit

Comparing the transformer waveforms for the PSBCF with LCC auxiliary circuit (Figures 6.19 and 6.20) to that with the LDD auxiliary circuit (Figures 6.11 and 6.12), it can be seen that the PSBCF converter with LCC auxiliary circuit can operate with a smaller duty while supplying the same output load. The auxiliary inductor operates with a 50% duty as expected (Figures 6.21 and 6.22) but unlike the LDD auxiliary, it is no longer the $i_{L_{aux}}$ which determines soft switching for the PA leg but rather $i_{pri} - i_{L_{aux}}$. The $i_{pri} - i_{L_{aux}}$ waveform capture is obtained by measuring the currents in both L_{aux} and L_{add} and displayed using the internal mathematical subject function of the oscilloscope. $v_{gs(TD)}$ shows a dip below zero when $v_{ds(TD)}$ fall to zero just before ZVS turn-on in Figure 6.22 while no such dip is seen in Figure 6.25. This is due to the limitation of the PSPICE MOSFET model being used and is discussed further in Section 6.4.1.

LDD Auxiliary Circuit

As with the results for the PSBCF with no auxiliary circuits, the i_{pri} current waveform does not stop flowing after falling to zero during the passive interval (Figures 6.11 and 6.12). However, the LDD auxiliary can be seen to be working from Figures 6.15 and 6.16 providing enough current to discharge the output capacitance of TB and bring $v_{ds(TB)}$ to zero before it is switched on. Small oscillations can be observed on $v_{L_{aux}}$ and $v_{x_{fmr}}$. This is caused by the reverse recovery of the auxiliary diode which was conducting. The auxiliary diodes when recovering behave like a capacitor and resonate with auxiliary inductor L_{aux} (Figures 6.13 and 6.14. MOSFETs on the AP leg switch with ZVS as expected (Figures 6.17 and 6.18. Noise appears on $v_{gs(TD)}$ after it has turned on in Figure 6.18). This is due to timing anomalies within the digital logic circuit of the UC3879 PSPICE model. This noise appears on the AP leg driving waveforms and appears during the transition from one interval to the next. Such noise can also be observed during the transition from one interval to the next in the $v_{gs(TD)}$ waveform in Figure 6.17, though this is probably due to EMI pick-up rather than noise from the actual UC3879 chip.

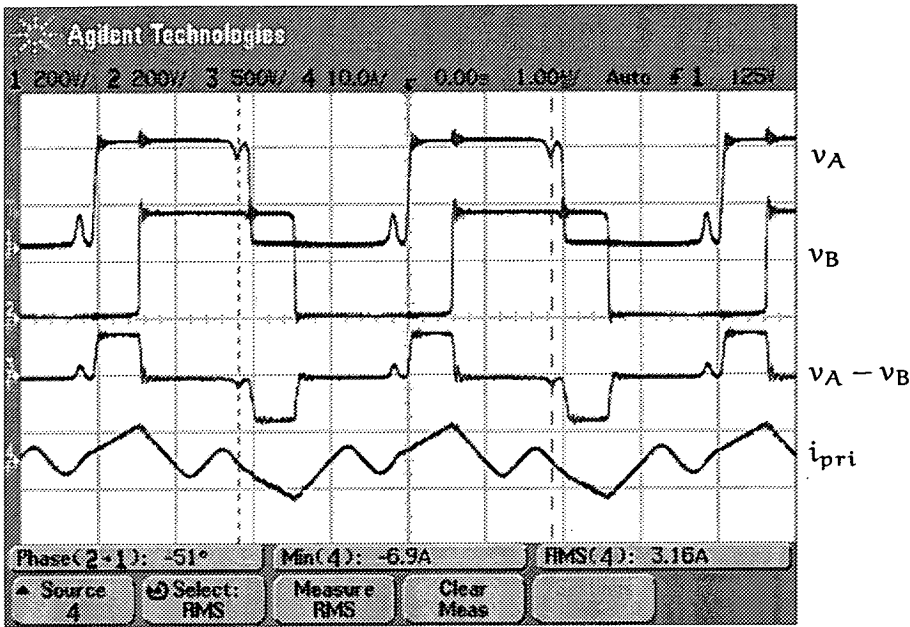


Figure 6.5: Prototype PSBCF without Auxiliary Circuit Waveforms (Half Load)

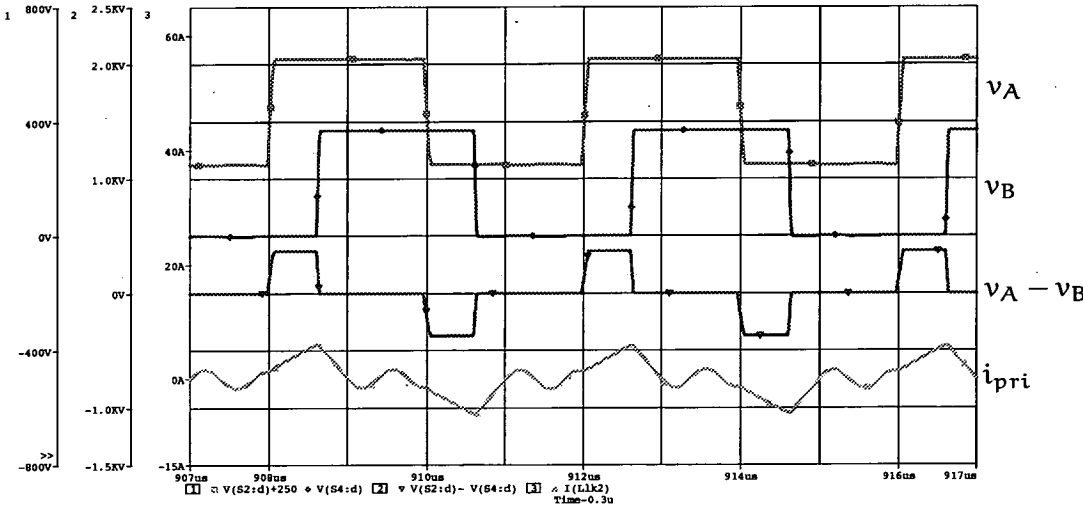


Figure 6.6: PSPICE PSBCF without Auxiliary Circuit Transformer Waveforms (Half Load)

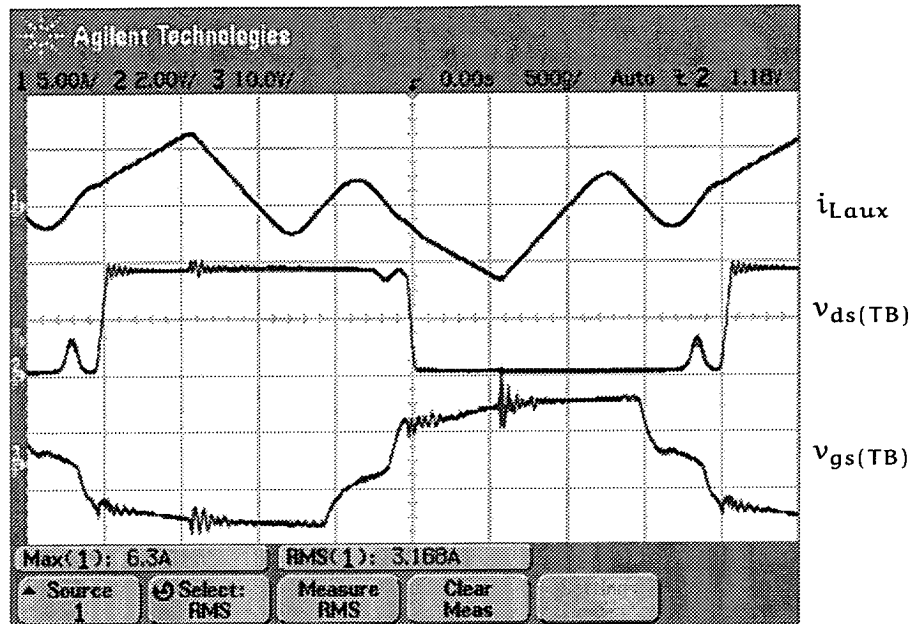


Figure 6.7: Prototype PSBCF without Auxiliary Circuit MOSFET TB Waveforms (Half Load)

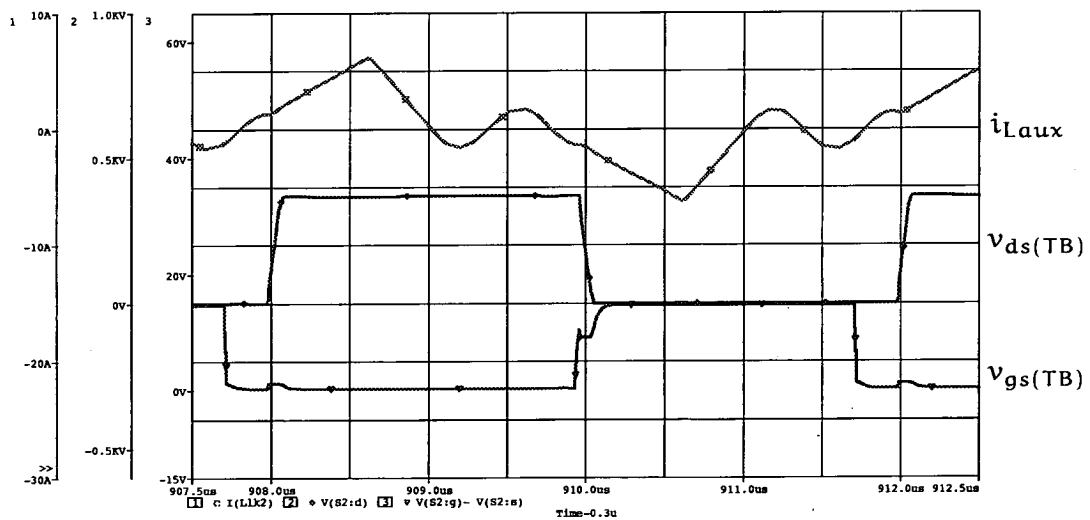


Figure 6.8: PSPICE PSBCF without Auxiliary Circuit MOSFET TB Waveforms (Half Load)

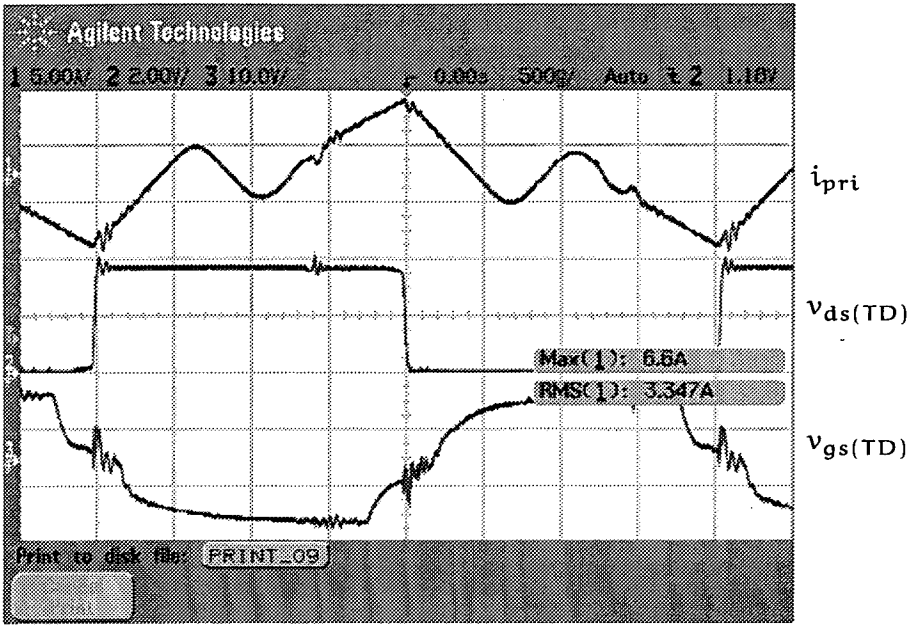


Figure 6.9: Prototype PSBCF without Auxiliary Circuit MOSFET TD Waveforms (Half Load)

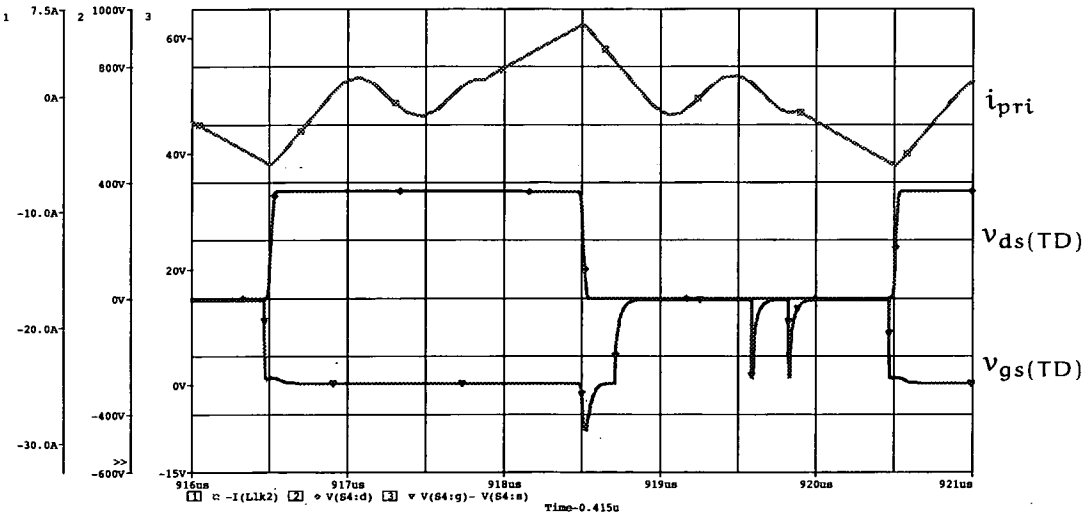


Figure 6.10: PSPICE PSBCF without Auxiliary Circuit MOSFET TD Waveforms (Half Load)

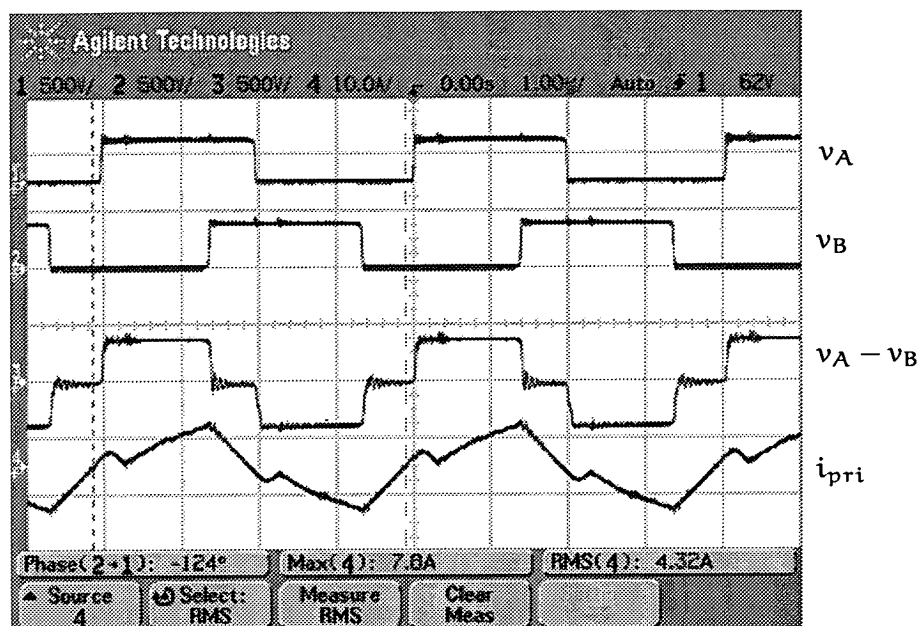


Figure 6.11: Prototype PSBCF with LDD Auxiliary Circuit Transformer Waveforms (Full Load)

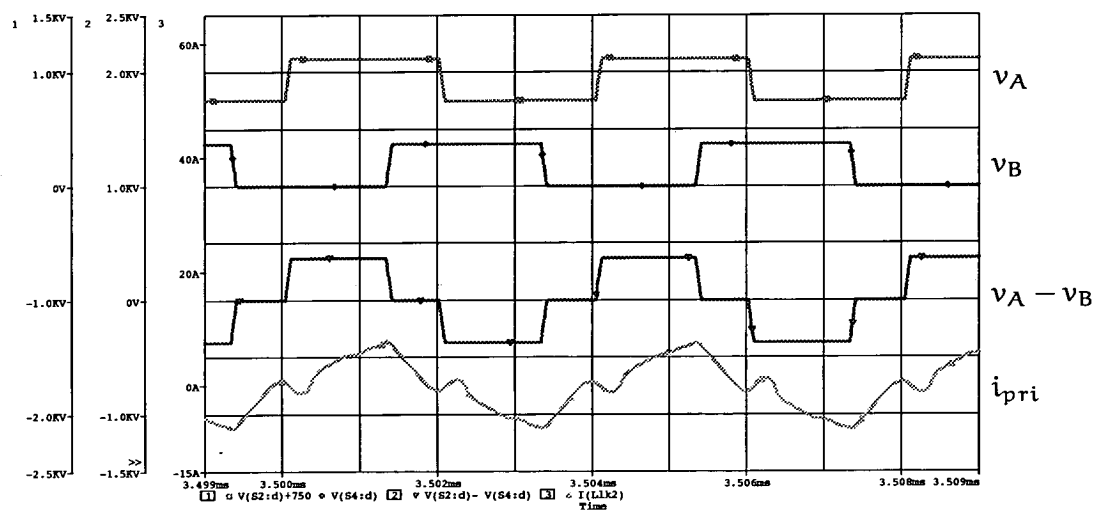


Figure 6.12: PSPICE PSBCF with LDD Auxiliary Circuit Transformer Waveforms (Full Load)

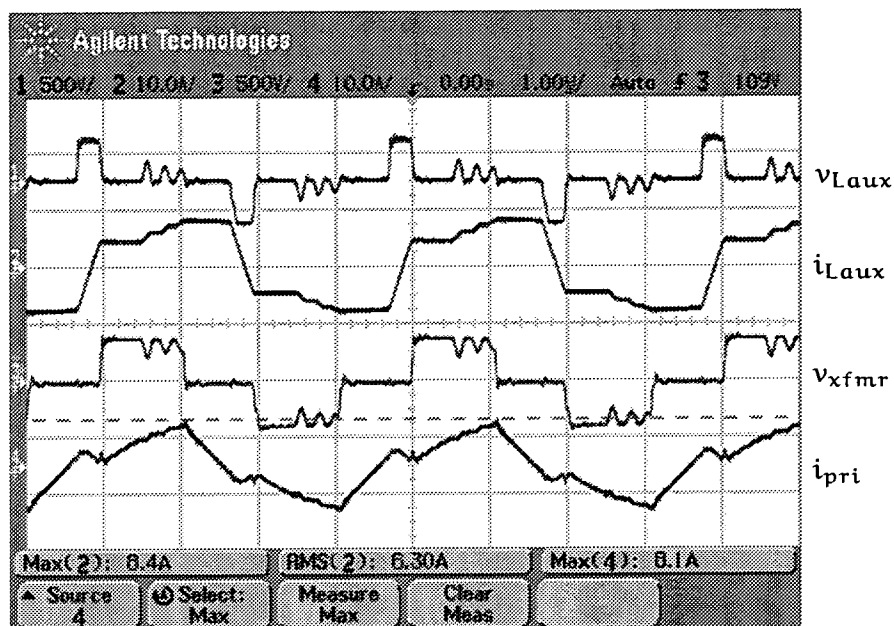


Figure 6.13: Prototype LDD Auxiliary Inductor Waveforms (Full Load)

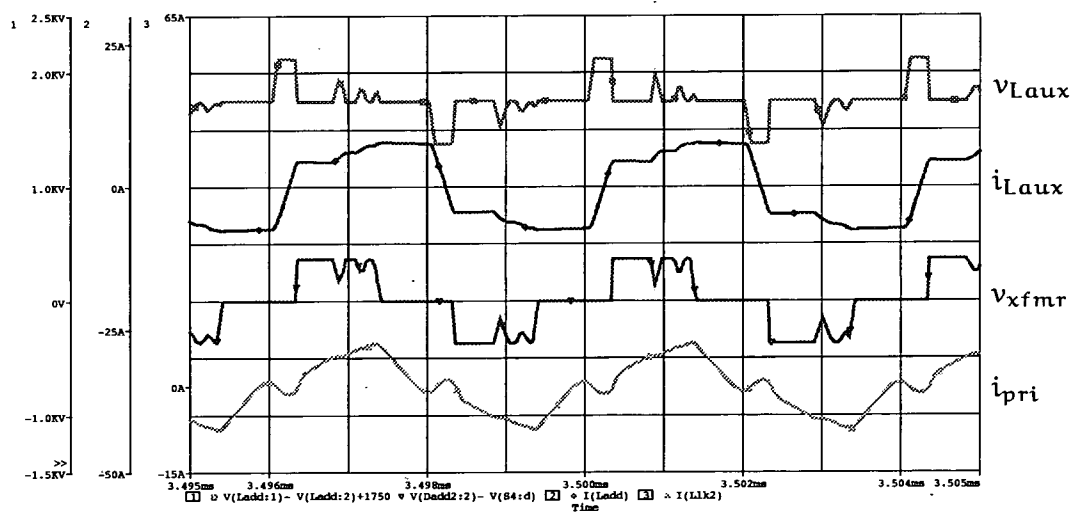


Figure 6.14: PSPICE LDD Auxiliary Inductor Waveforms (Full Load)

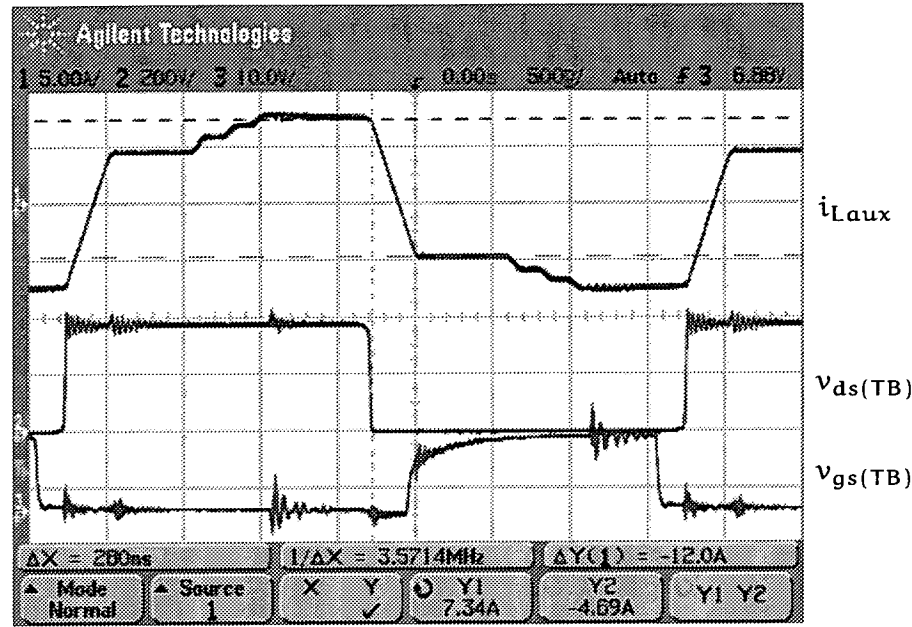


Figure 6.15: Prototype PSBCF with LDD Auxiliary Circuit MOSFET TB Waveforms (Full Load)

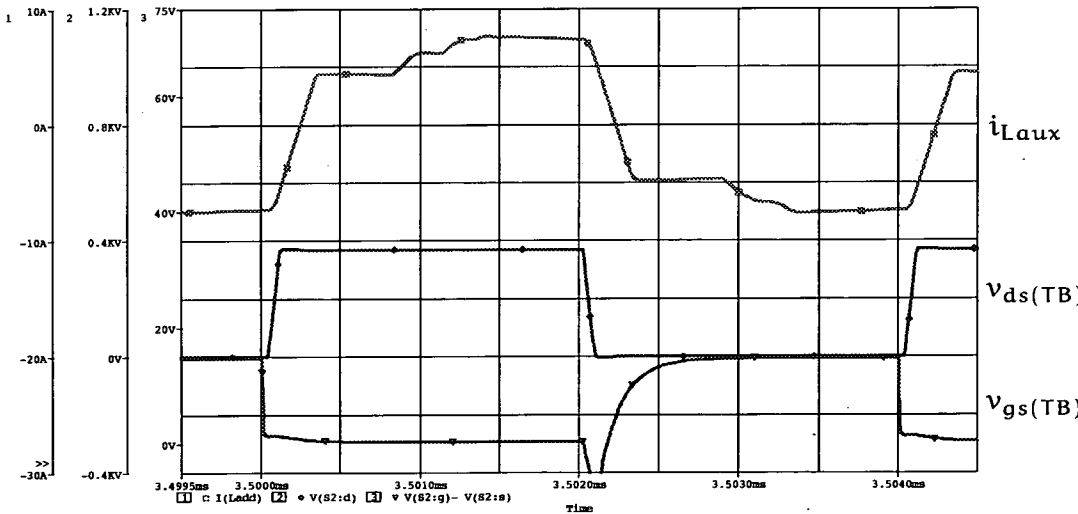


Figure 6.16: PSPICE PSBCF with LDD Auxiliary Circuit MOSFET TB Waveforms (Full Load)

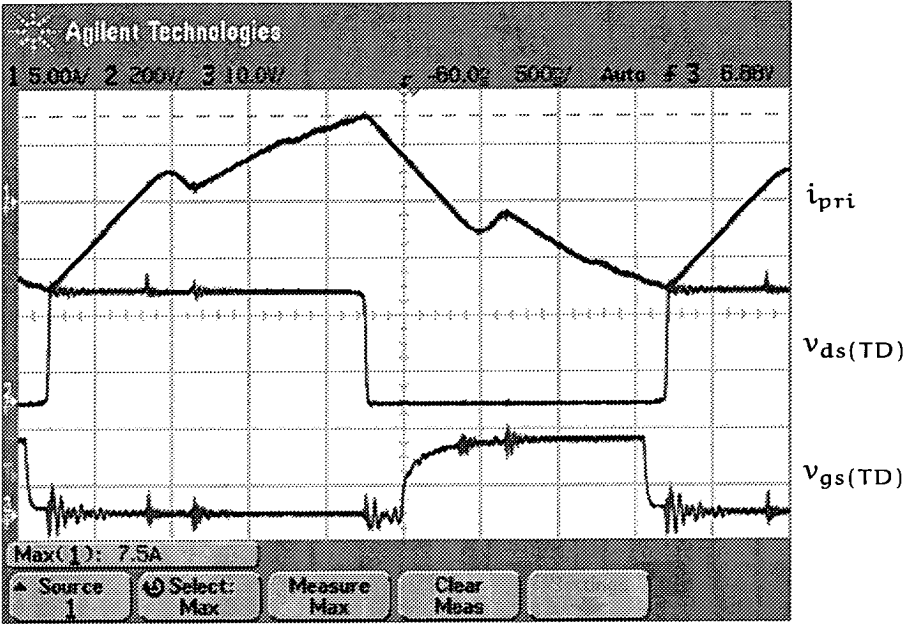


Figure 6.17: Prototype PSBCF with LDD Auxiliary Circuit MOSFET TD Waveforms (Full Load)

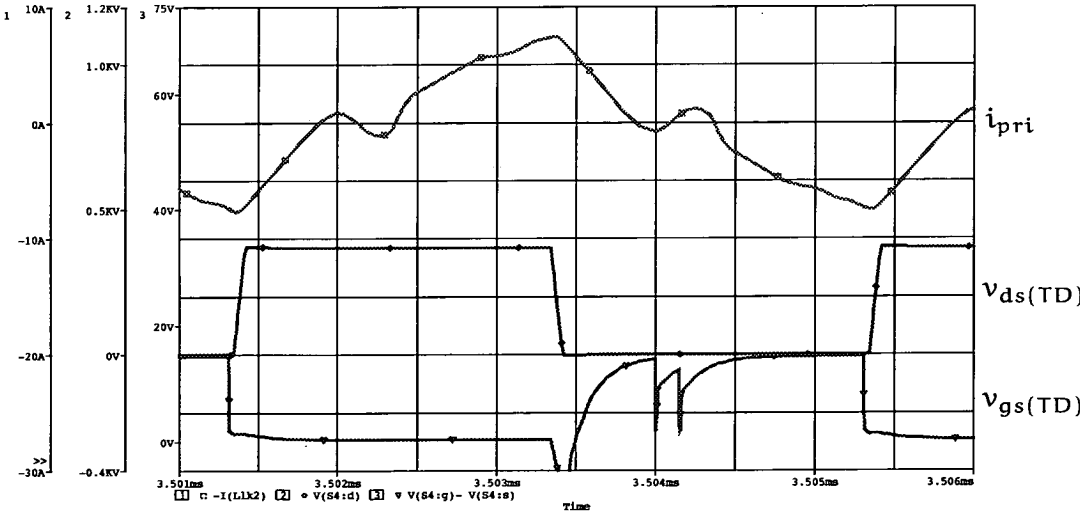


Figure 6.18: PSPICE PSBCF with LDD Auxiliary Circuit MOSFET TD Waveforms (Full Load)

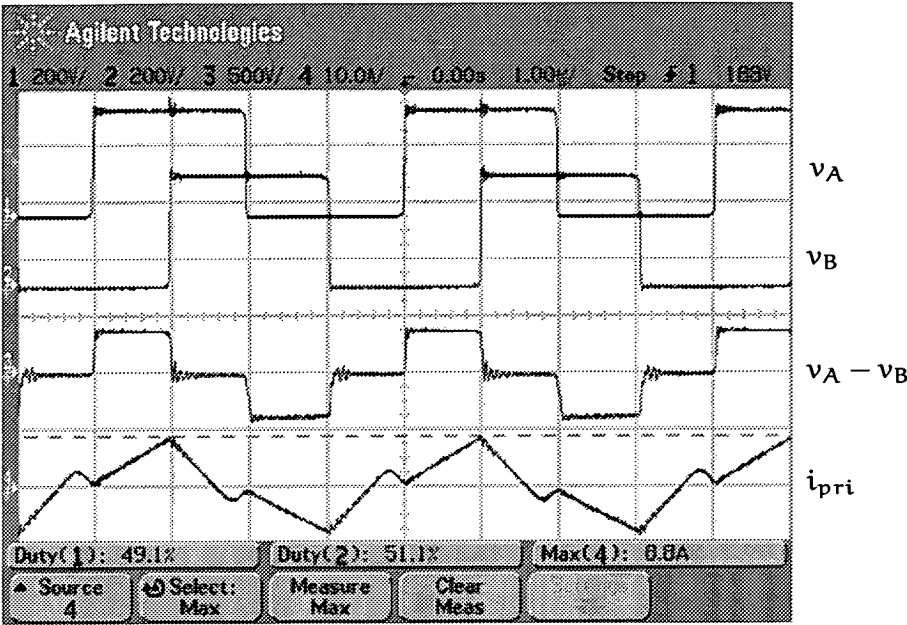


Figure 6.19: Prototype PSBCF with LCC Auxiliary Circuit Transformer Waveforms (Full Load)

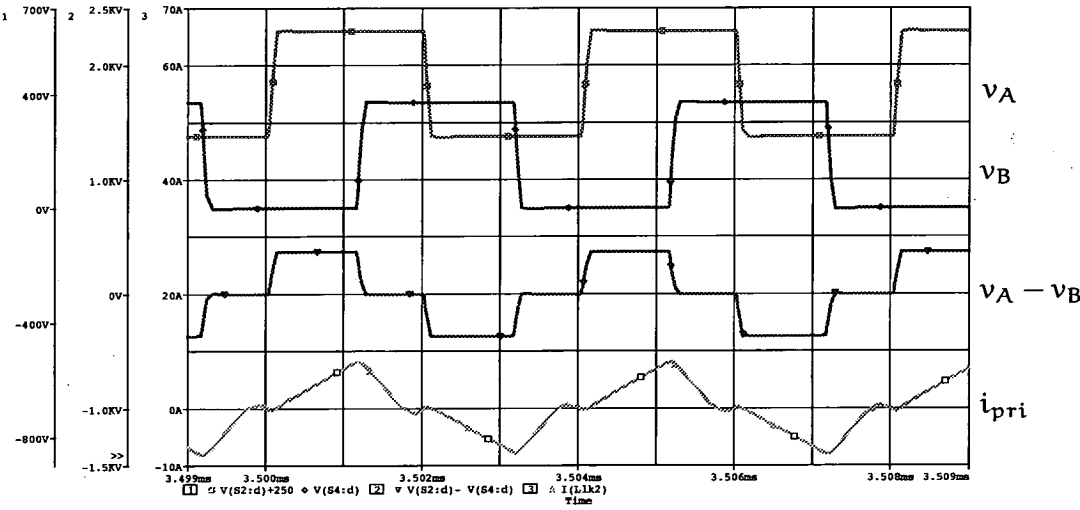


Figure 6.20: PSPICE PSBCF with LCC Auxiliary Circuit Transformer Waveforms (Full Load)

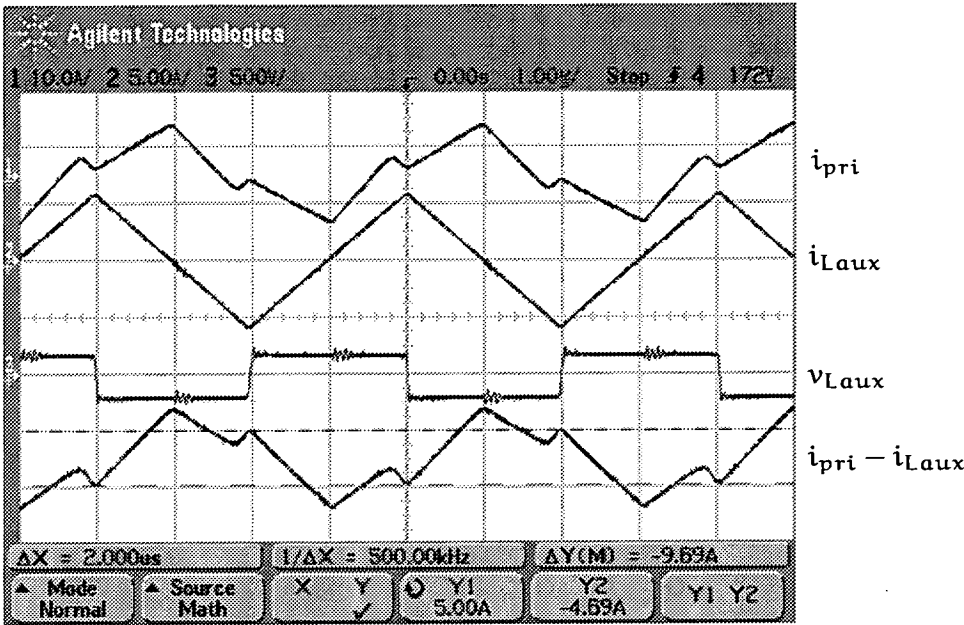


Figure 6.21: Prototype LCC Auxiliary Inductor Waveforms (Full Load)

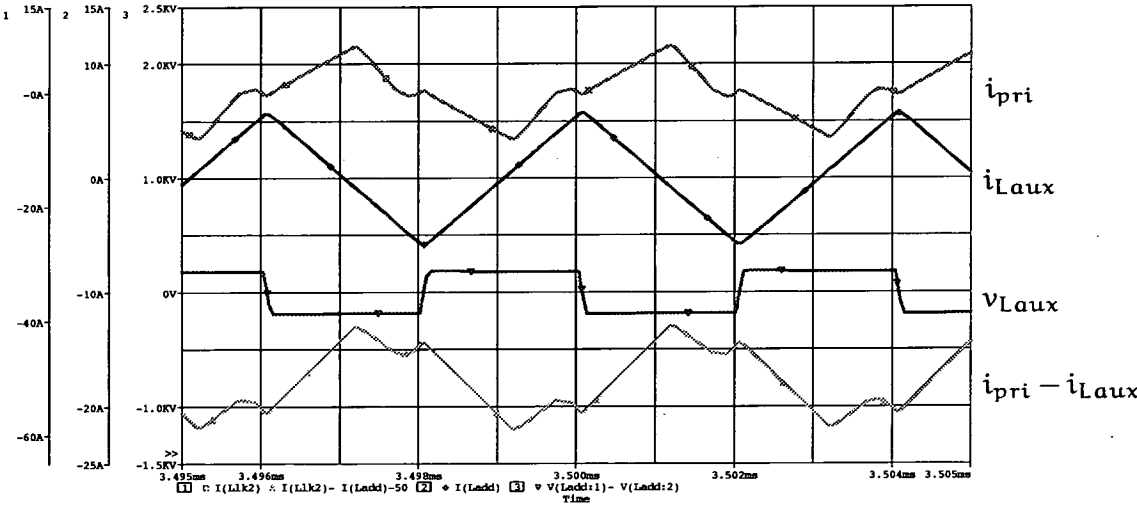


Figure 6.22: PSPICE LCC Auxiliary Inductor Waveforms (Full Load)

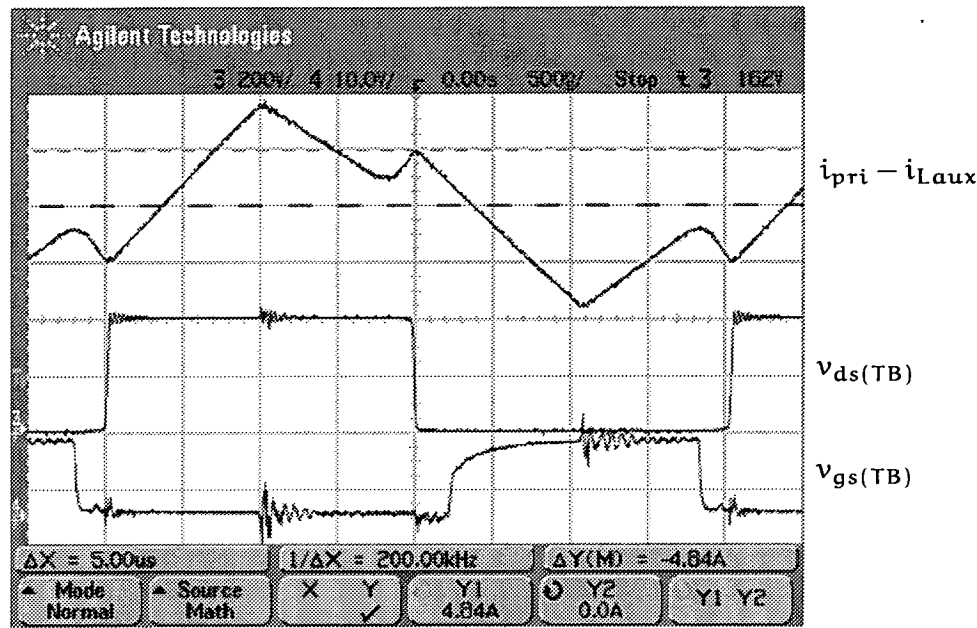


Figure 6.23: Prototype PSBCF with LCC Auxiliary Circuit MOSFET TB Waveforms (Full Load)

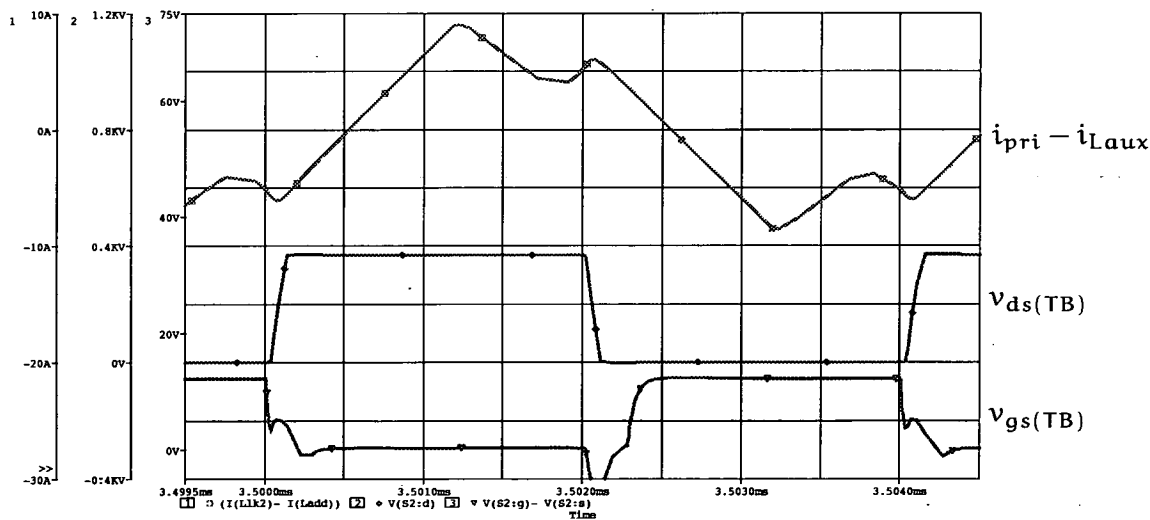


Figure 6.24: PSPICE PSBCF with LCC Auxiliary Circuit MOSFET TB Waveforms (Full Load)

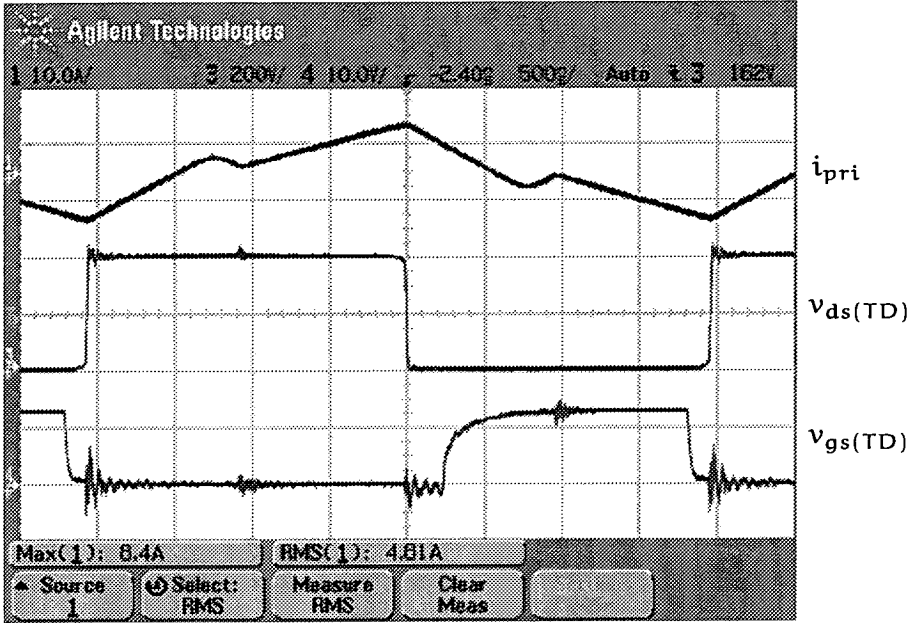


Figure 6.25: Prototype PSBCF with LCC Auxiliary Circuit MOSFET TD Waveforms (Full Load)

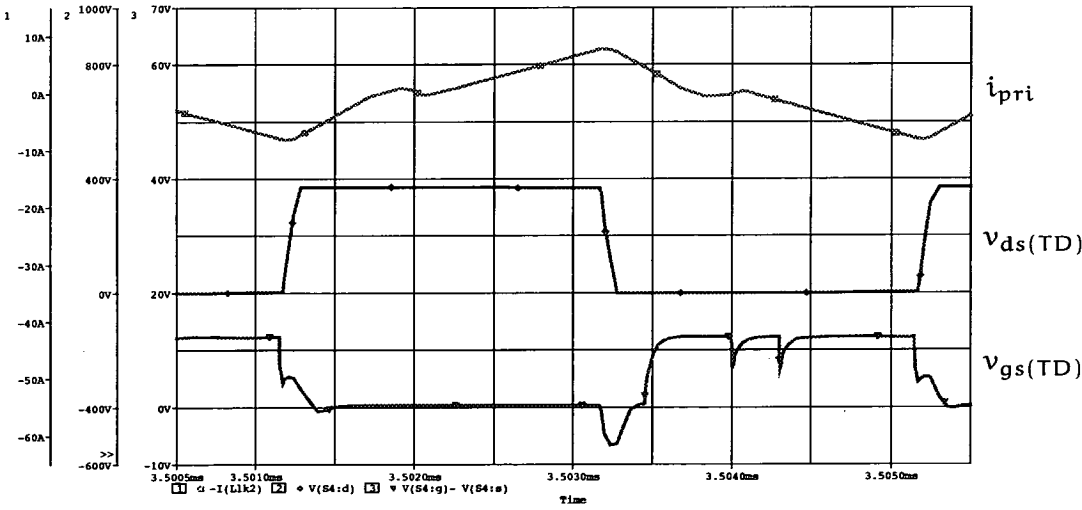


Figure 6.26: PSPICE PSBCF with LCC Auxiliary Circuit MOSFET TD Waveforms (Full Load)

6.3.2 Output Short-circuit Operation

Closed loop short-circuit simulations for the various configurations of the PSBCF were carried out by using the simple resistive arc model (Section 5.7). The arc was applied after the converter has been running for 1 ms (to allow the converter to arrive at a steady state). The arc lasts for 1 ms after which it is cleared and the converter allowed to recover to normal operation. In order to keep time required to perform the simulation acceptable, the output filter capacitor was reduced to 1/100th of its original size of 0.66 μF . This allows the converter to settle at its steady state at the start of the simulation and after the arc clears in a much shorter time. The current fed bridge is simulated in the same manner to provide a frame of reference for comparison purposes. The full simulation waveforms over the entire duration for the three converters are as shown in Figures 6.27, 6.29 and 6.31, while a close up of waveforms at the moment when the short-circuit is applied is shown in Figures 6.28, 6.30 and 6.32. Full and close up waveforms for the CFB are presented in Figures 6.35 and 6.36.

In addition, the results for the averaged PSBCF model are also presented (Figure 6.33) to allow both its steady-state and dynamic performance to be verified. The average PSBCF model was created without taking into account the inter-turn winding capacitance of the transformer. Therefore, a short-circuit simulation of the PSBCF converter with no auxiliary circuit was carried out (Figure 6.34), with the inter-turn winding capacitance of the transformer removed, for comparison with the PSBCF average model simulation results.

As the averaged model only provides averaged input and output voltage and current waveforms, the waveforms for the full switched models have been mathematically averaged and rectified when necessary.

The peak to peak currents for i_{pri} for PSBCF without auxiliary circuit, with LDD auxiliary circuit and LCC auxiliary circuit as observed from Figures 6.28, 6.30 and 6.32 are 50 A, 30 A and 50 A respectively. It can be also observed from these three figures that the output voltage has been simulated to collapse in less than one switching cycle, to observe the converter's performance when the maximum peak current occurs in this worst case scenario.

The waveforms for the averaged PSBCF model (Figure 6.33) match reasonably well to that of the PSBCF model which omitted the transformer parasitic capacitance (Figure 6.34). It also matches reasonably to the PSBCF model without auxiliary circuit (Figure 6.27) and that with the LCC auxiliary (Figure 6.31). However, due to the auxiliary inductor being located in series with the main transformer, the PSBCF averaged model is less able to predict the PSBCF converter with LDD auxiliary circuit's performance with much accuracy.

In comparison, short-circuit simulation results for the CFB converter (Figures 6.35 and 6.36), show that the CFB converter is unable to limit the short-circuit current in the input and bridge MOSFETs to any sensible value. It has to depend on circuit parasitic impedances to limit the peak short-circuit current. In addition, from Figure 6.35, it can be seen that the converter has to be shut down before the converter can recover, or else the current built up in L_{choke} might raise the output voltage to beyond what it was designed for. Figures 6.37 and 6.38 show the currents flowing into the resistive arc and the voltage across it for the PSBCF and CFB converter respectively. If the PSBCF converter can be designed such that the current flowing into the arc is unable to sustain the arc, the arc should extinguish and the converter should be able to recover automatically, unlike the CFB converter, which is likely to continue feeding current into the arc until the output short-circuit is sensed and the converter shut down.

Output short-circuits for the prototype PSBCF converter with LDD and LCC auxiliary circuits were also carried out to verify the inherent short-circuit protection feature of the converter. As the UC3879 chip suffers from a discontinuous duty transition between duty problem from 0.95 to 1, the duty was fixed at a maximum of approximately 0.95 in order to prevent noise from causing the converter from going unstable. The high voltage rectifier is disconnected from the secondary winding of the converter and replaced with a 3 A fuse. The variac is adjusted to give an output voltage of 370 V but left turned off. The control circuitry for the converter is first turned on, and the oscilloscope is set to trigger once on the full input voltage across the transformer. The variac is then switched on momentarily and off again to enable the oscilloscope to capture the short-circuit event. The transformer waveforms for the PSBCF converter with LDD and LCC auxiliary circuits are shown in Figures 6.39 and 6.40 respectively. The short-circuit peak to peak current value for the PSBCF with LDD auxiliary circuit is only 27.5 A, while using the LCC auxiliary circuit gave a value of 41.6 A.

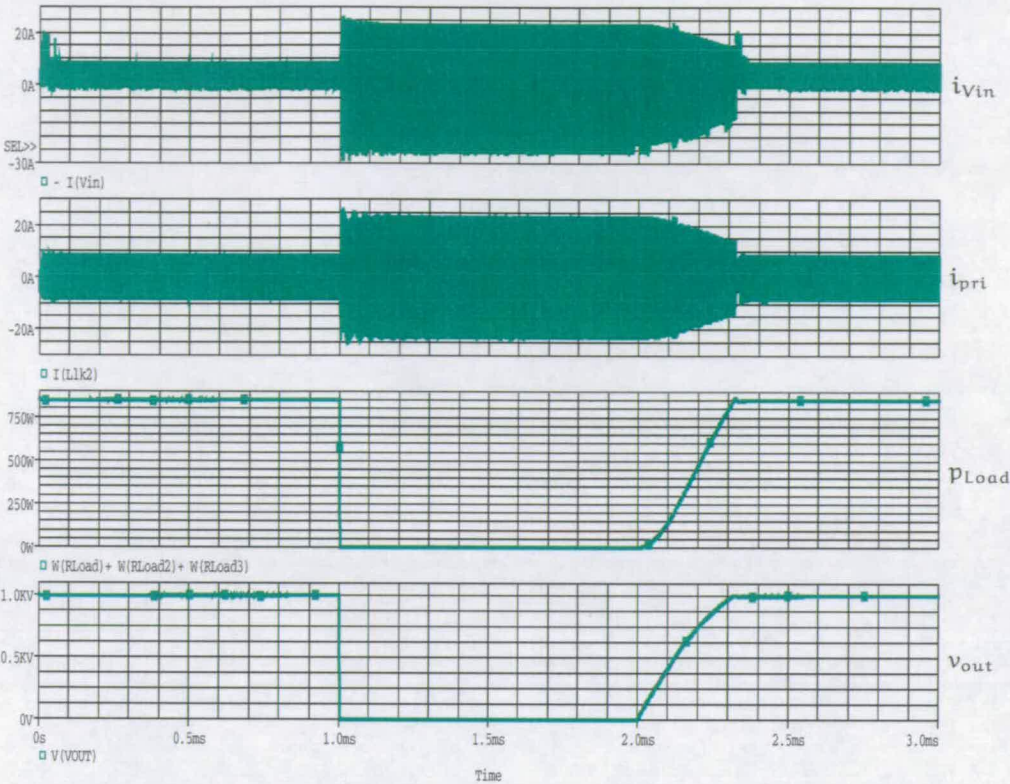


Figure 6.27: PSPICE Simulation (SC) for PSBCF without Auxiliary Circuitry

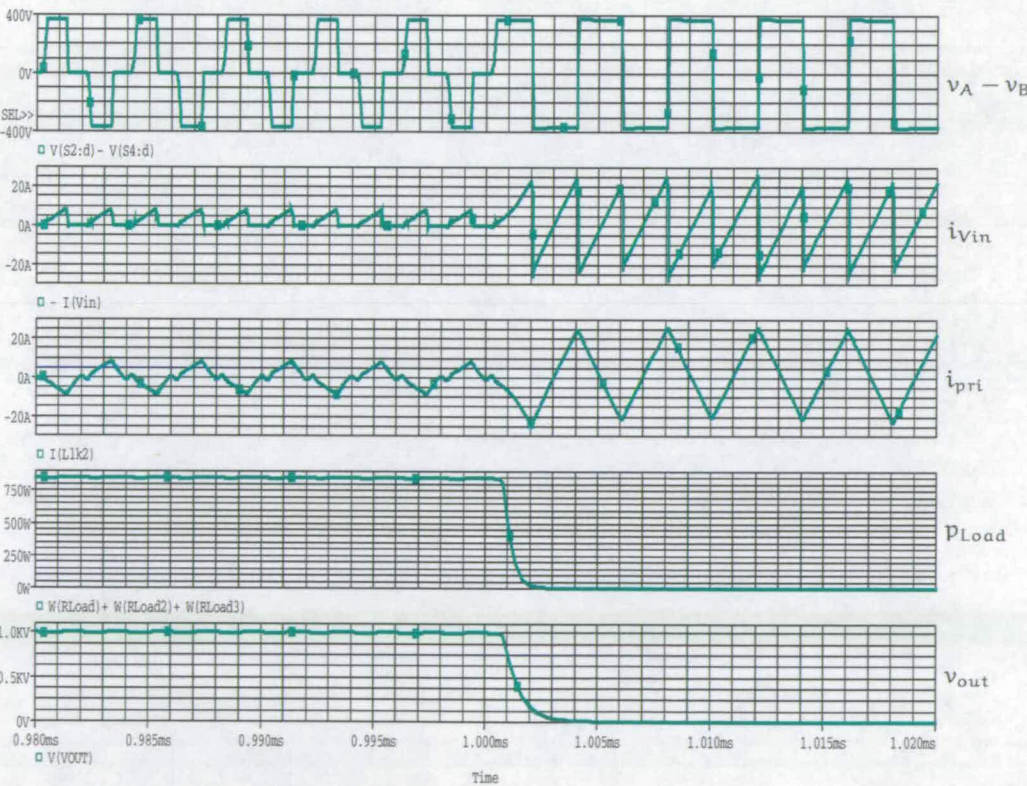


Figure 6.28: PSPICE Simulation (SC) for PSBCF without Auxiliary Circuitry (Detailed)

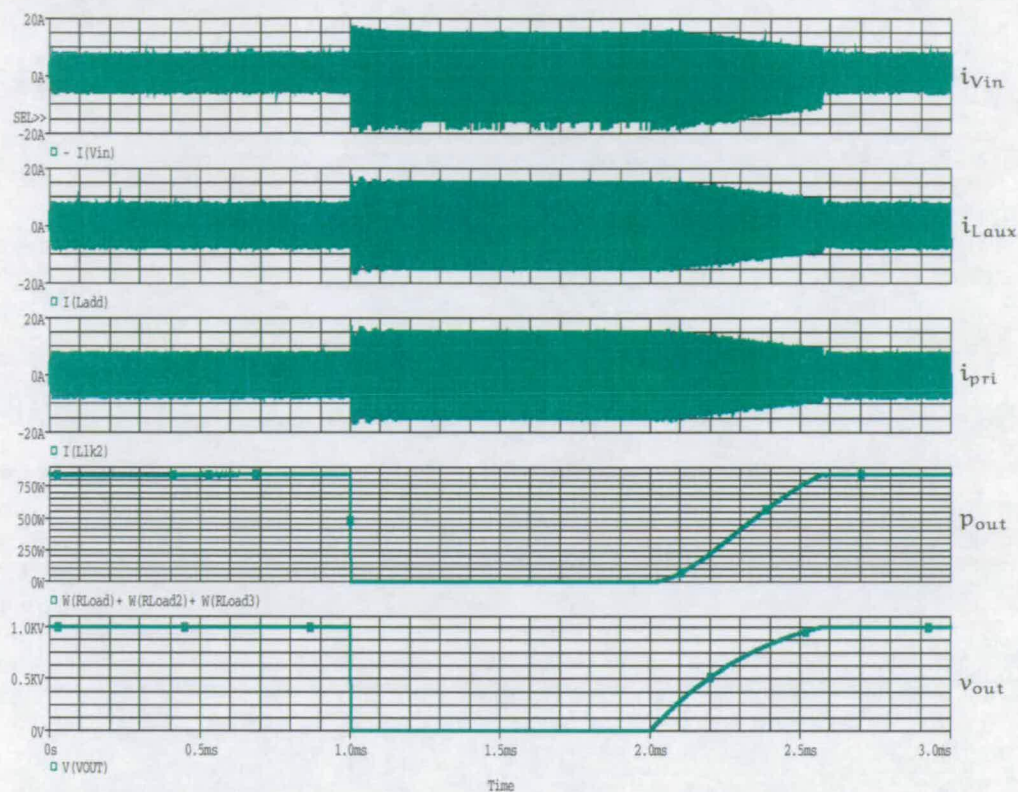


Figure 6.29: PSPICE Simulation (SC) for PSBCF with LDD Auxiliary Circuitry

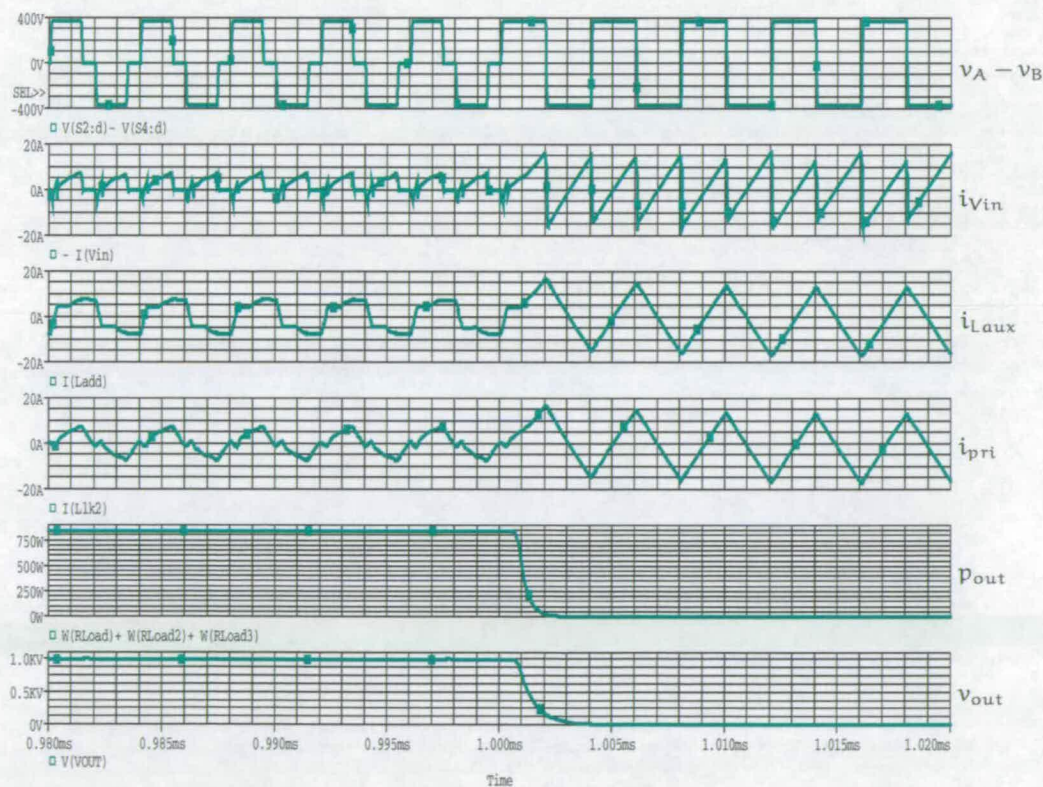


Figure 6.30: PSPICE Simulation (SC) for PSBCF with LDD Auxiliary Circuitry (Detailed)

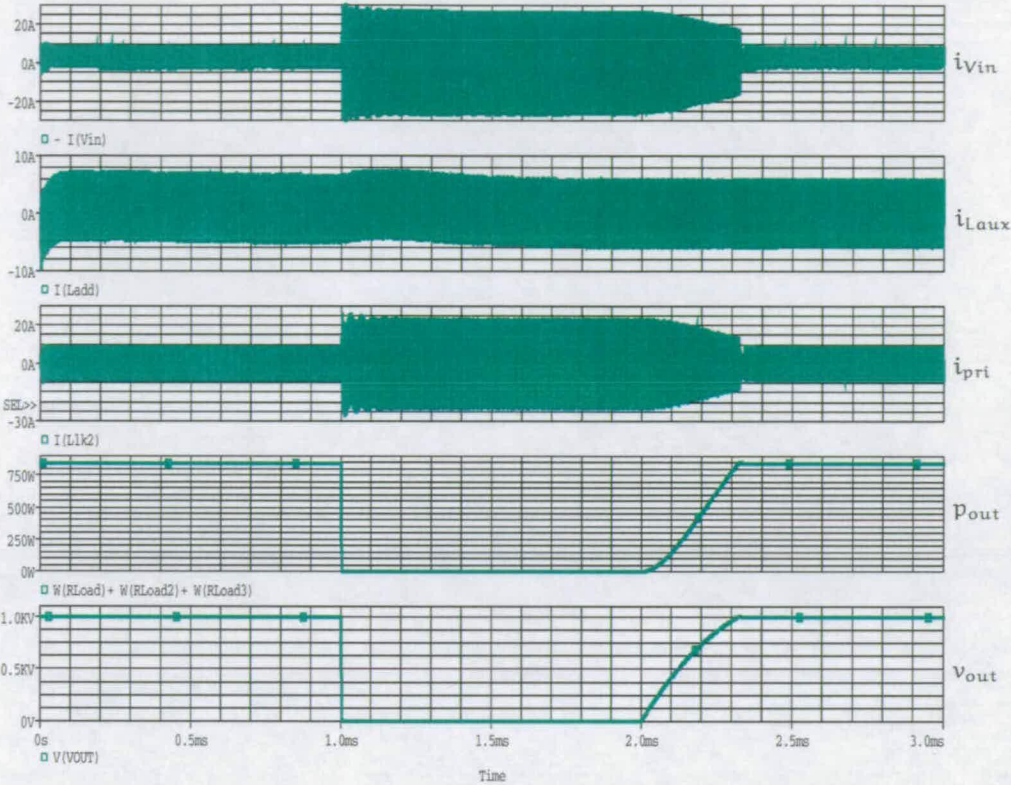


Figure 6.31: PSPICE Simulation (SC) for PSBCF with LCC Auxiliary Circuitry

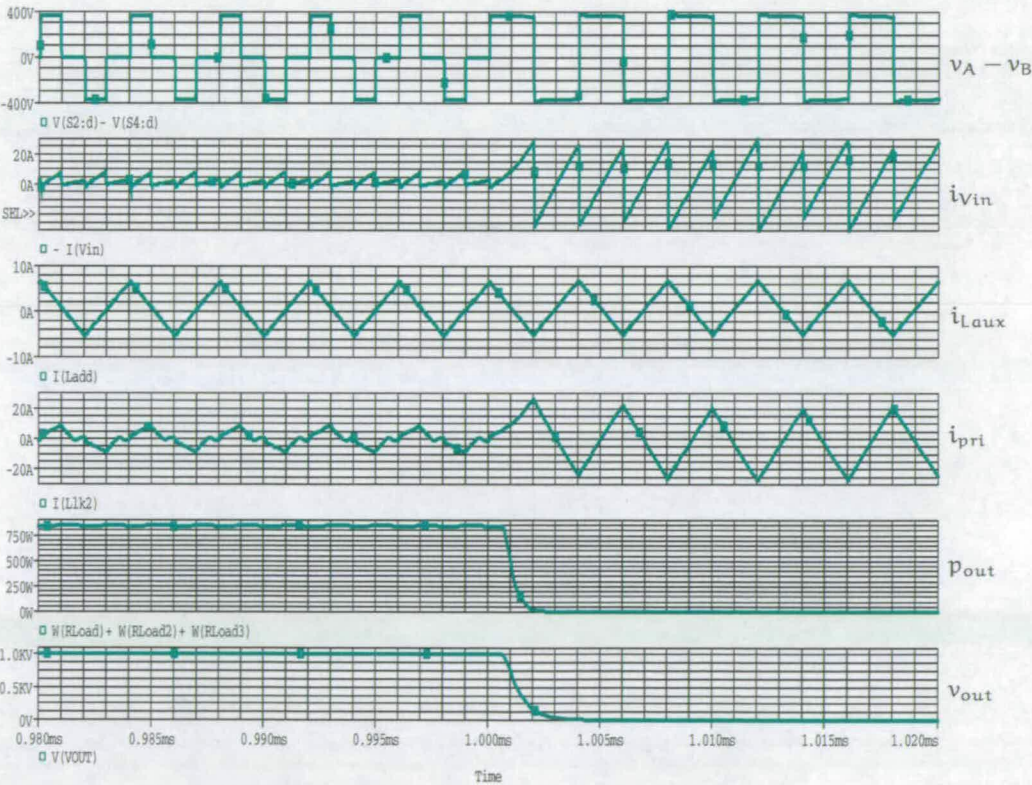


Figure 6.32: PSPICE Simulation (SC) for PSBCF with LCC Auxiliary Circuitry (Detailed)

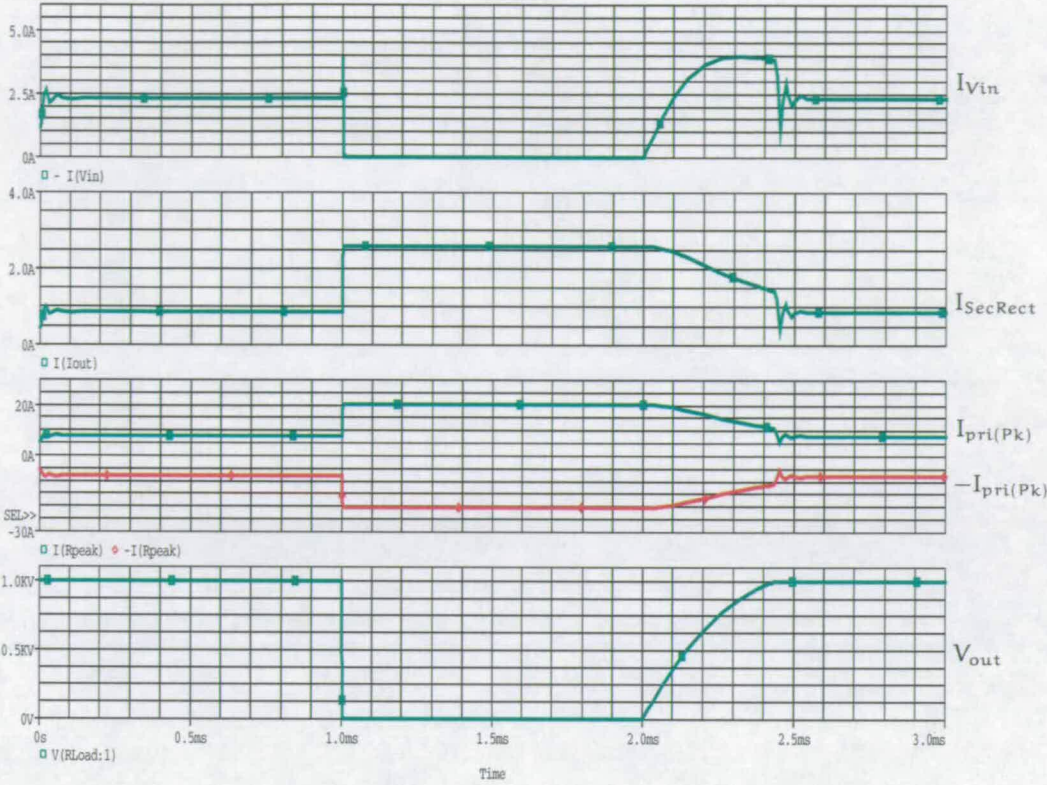


Figure 6.33: PSPICE Simulation (SC) for PSBCF Using Averaged Model

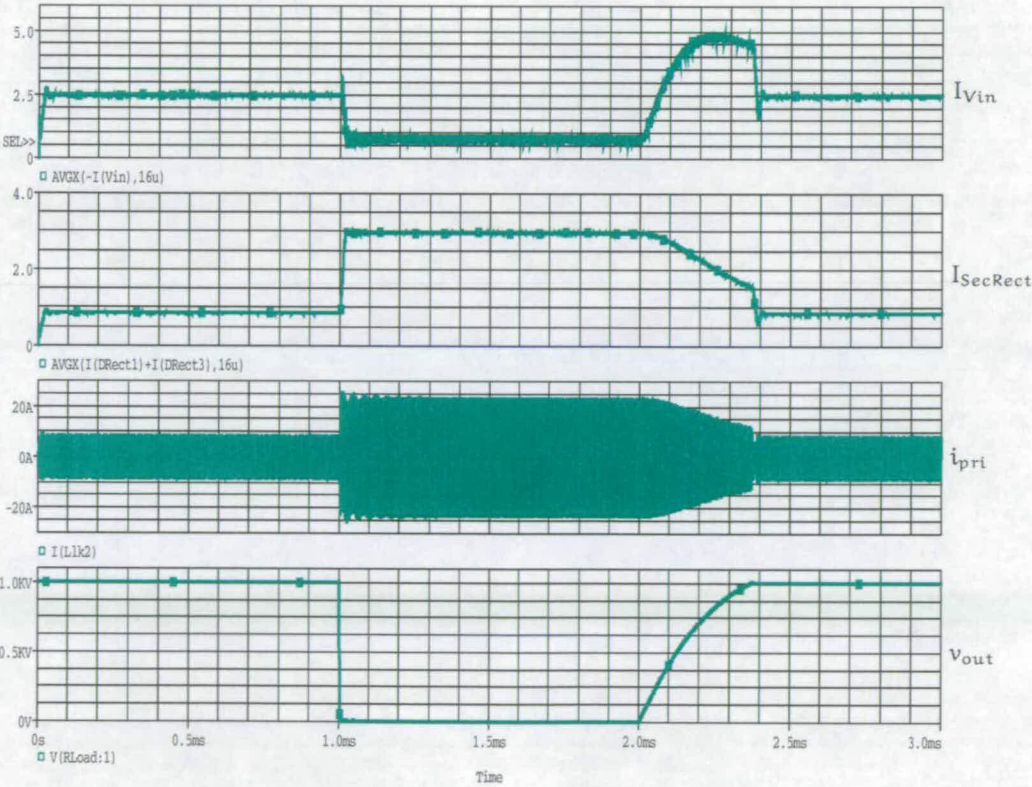


Figure 6.34: PSPICE Simulation (SC) for PSBCF Using Ideal Model

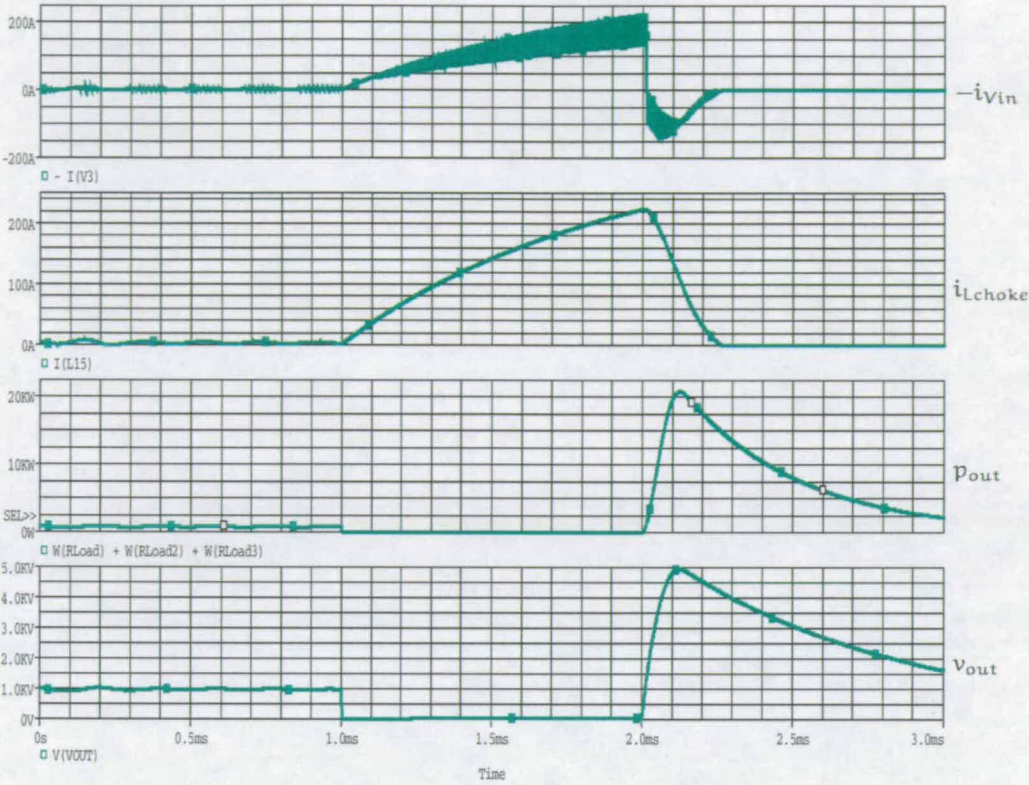


Figure 6.35: PSPICE Simulation (SC) for CFB

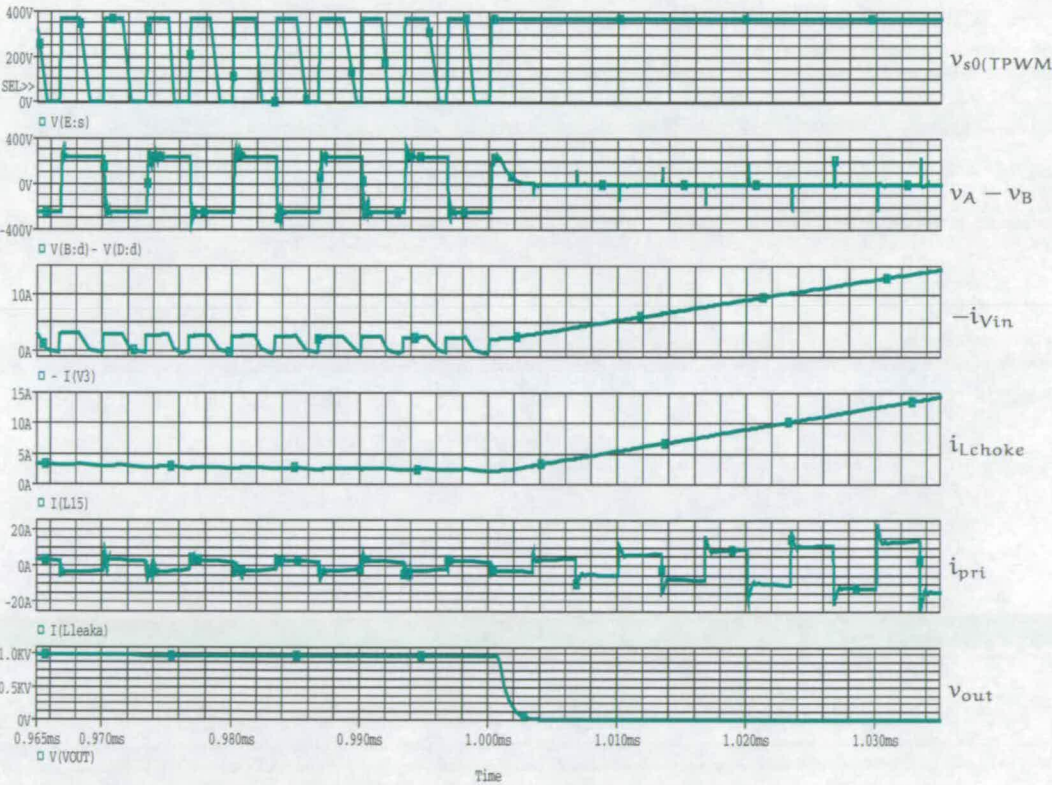


Figure 6.36: PSPICE Simulation (SC) for CFB (Detailed)

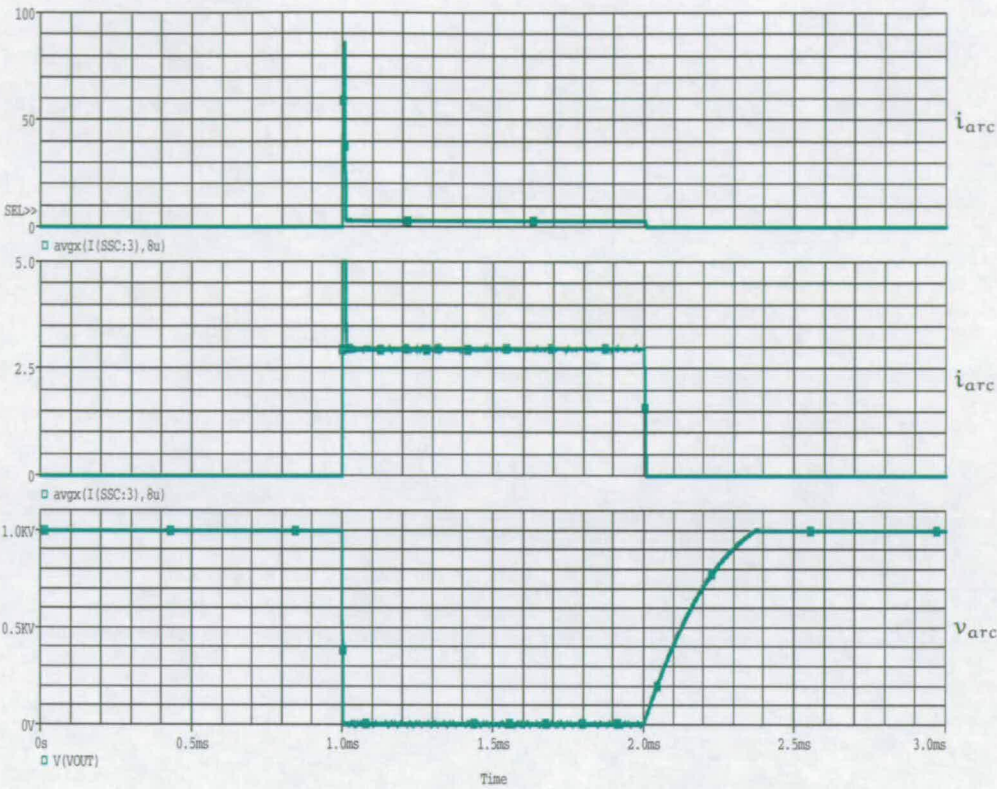


Figure 6.37: PSPICE PSBCF Outputs During Short-circuit

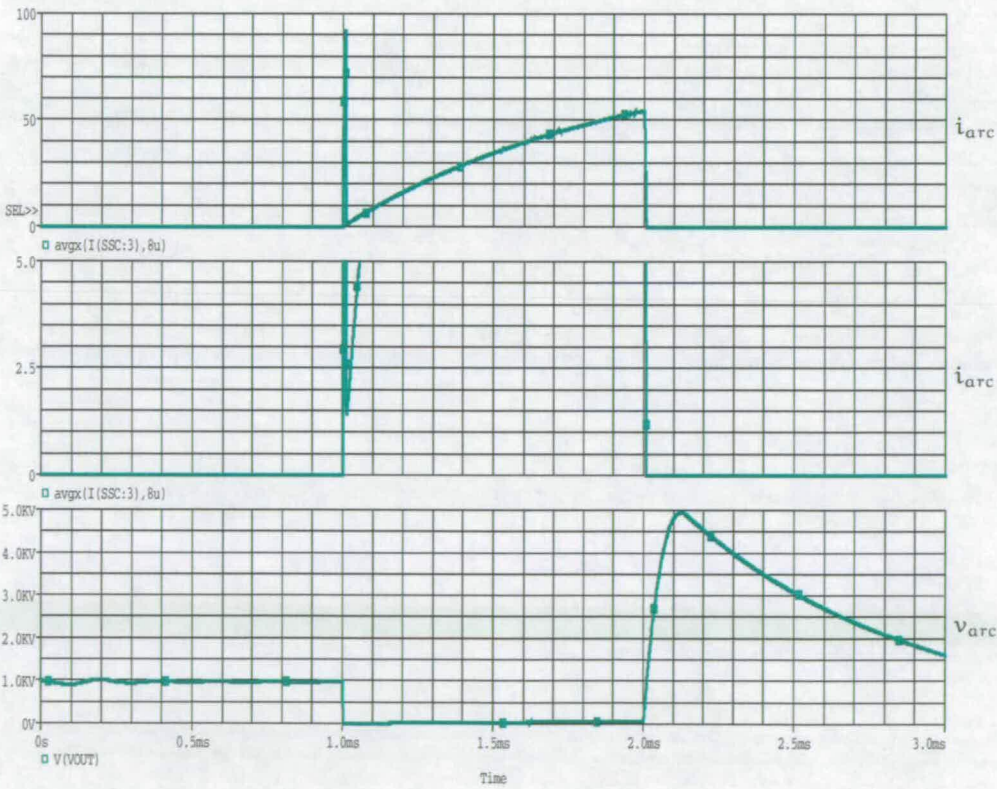


Figure 6.38: PSPICE CFB Outputs During Short-circuit

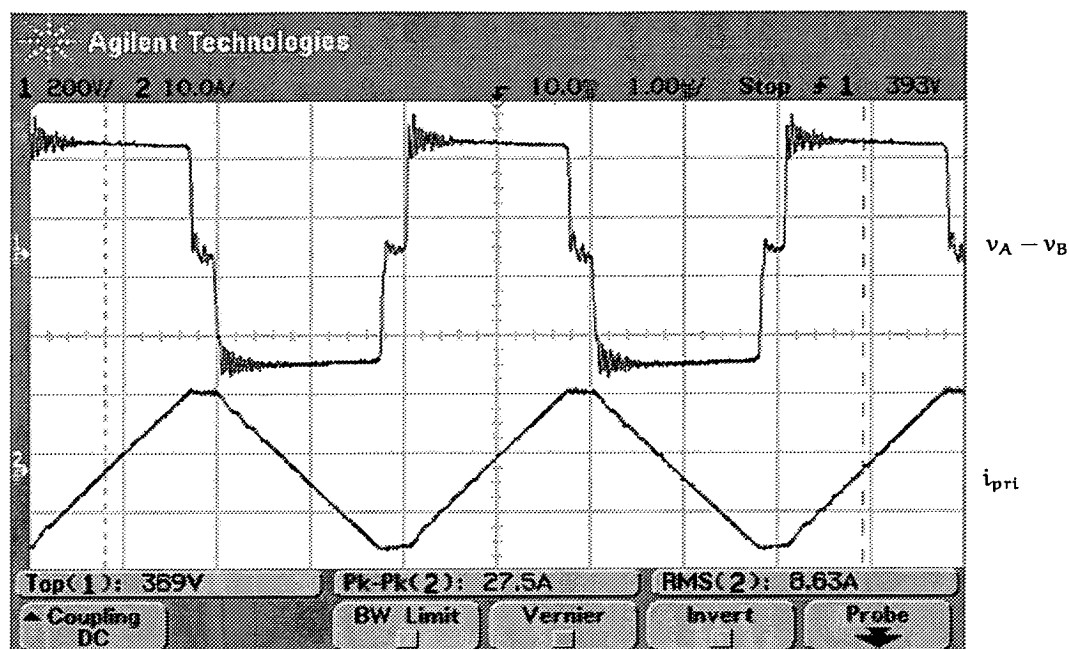


Figure 6.39: Output Short-circuit Waveform for PSBCF with LDD Auxiliary Circuitry

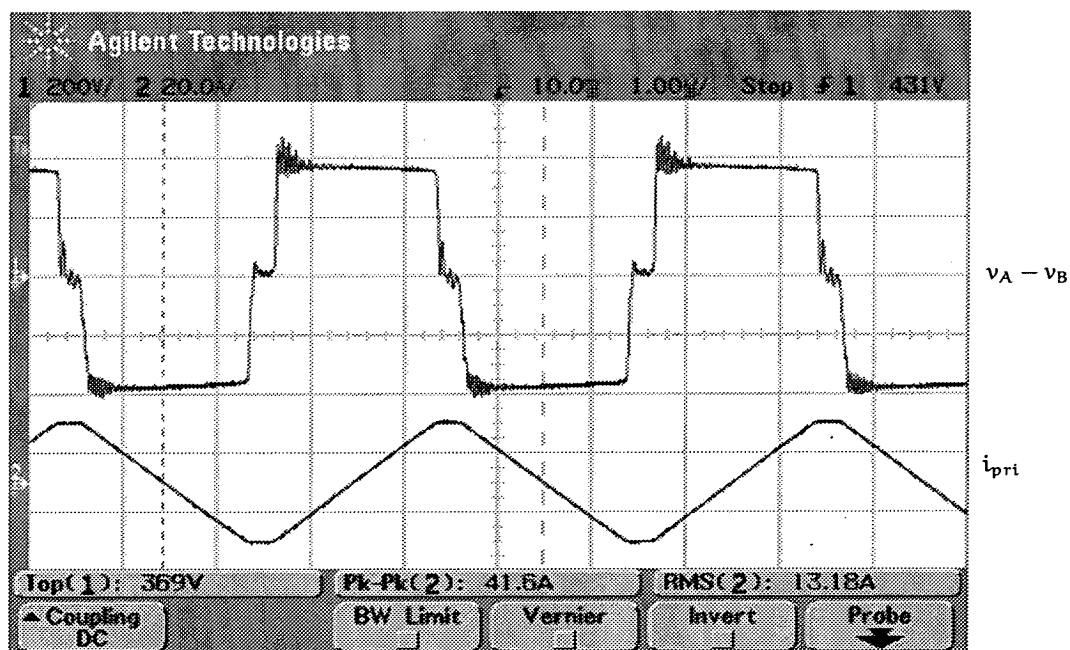


Figure 6.40: Output Short-circuit Waveform for PSBCF with LCC Auxiliary Circuitry

6.4 Switching Transition Simulations Using Accurate MOSFET Models

In this section, simulation waveforms are presented for a ZVS transition using a simplified MOSFET model created using Orcad PSPICE Model Editor and a more detailed one provided by the MOSFET manufacturer (Infineon).

6.4.1 Orcad PSPICE Model Limitation

In Figures 6.41 and 6.42, the PA leg of the bridge was used to test the difference between the model created using the model editor and that provided by Infineon. A current is being injected into v_A and TA is switched off. $v_{ds(TB)}$ falls to zero and TB switches on with ZVS. The simple PSPICE model shows the voltage dip in the $v_{gs(TB)}$ while the Infineon model does not. $v_{GS(X)}$ is the gate-source voltage waveform seen at the MOSFET within the packaging after the parasitic resistances and inductances (Figure 6.43). More importantly, the PSPICE model does not predict the delay in $v_{ds(TB)}$ falling to zero after TA is switched off, while this is predicted by the Infineon model which matches that observed in any of the waveforms showing the MOSFET undergoing ZVS (*e.g.* In Figure 6.26 $v_{ds(TD)}$'s rise to V_{in} is delayed after TD is switched off). The manufacturer's model is able to do this because the model includes, amongst other components, the MOSFET package lead resistances and inductances. This has the effect of requiring the AP and PA transition times to be increased, taking into account delays caused by the MOSFET package inductance, in order to allow ZVS to occur. It can be observed from Figure 6.15, there is a delay of around 200 ns after $v_{gs(TB)}$ begins to fall to zero before the $v_{ds(TB)}$ starts to rise. The simulation results in Figure 6.42 also roughly predicts a 200 ns delay in $v_{ds(TB)}$ after $v_{gs(TA)}$ starts to fall to zero. Thus, the $R_{DelayAB}$ and $R_{DelayCD}$ values were increased to 4.6 k Ω from the initial design value of 2.2 k Ω .

6.4.2 Switch Transitions Under Different Conditions

Using the method described in Section 6.4.1, various simulations were carried out varying the value of the injected current, I_{inj} , to observed the effects of what happens when the MOSFETs on the PA leg loses soft switching. Instantaneous power ($p_{(X)}$) and energy ($e_{(X)}$) loss waveforms for each switch are also included.

Figure 6.44 shows the MOSFETs undergoing hard switching when no current is injected. $i_{sd(TA)}$ is the forward current of the parasitic diode of TA, while $i_{ds(TB)}$ shows the drain-source current of TB. This has a similar effect to the PA leg being disconnected from the L_{add} and operating in isolation. It can be observed that under

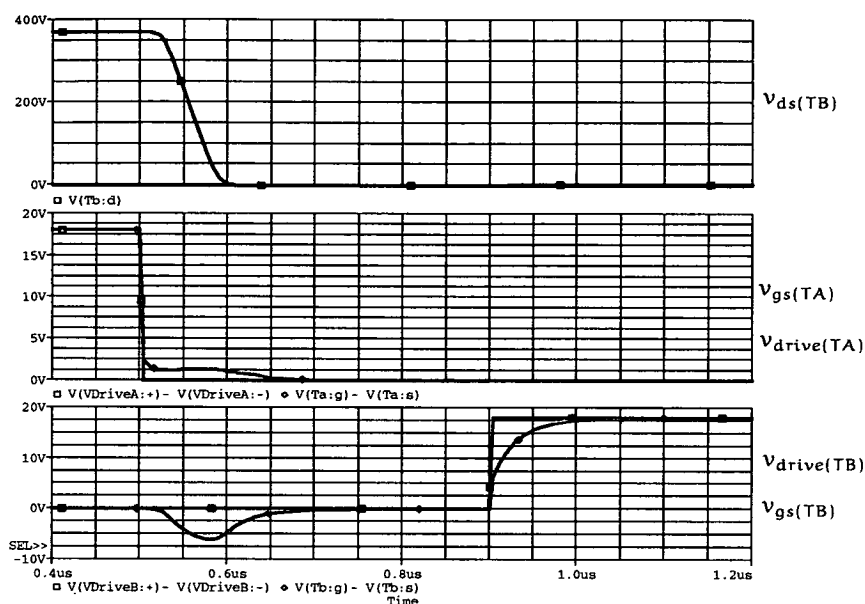


Figure 6.41: Transition Waveforms During Switching of Orcad PSPICE MOS-FET Model

hard switching, $v_{GS(TA)}$, the actual gate-source voltage within the MOSFET package can be seen to experience a voltage pull-up even when it is supposed to be switched off when TB undergoes hard switching.

This can also be seen in Figure 6.45 as TB undergoes hard switching with $I_{inj} = -2$ A. The turn-on losses for TB and turn-off losses for TA also increase from around $22 \mu J$ and $7 \mu J$ to $150 \mu J$ and $60 \mu J$ respectively. This energy loss is further increased to around $800 \mu J$ for TA and $400 \mu J$ for TB as the injected current is increased to -8 A in Figure 6.46. As shown in Figures 6.45 and 6.46, hard switching of the MOSFETs when the parasitic diode of the other MOSFET of the leg is conducting results in high switching losses. In addition, it can also be observed from these two figures that TB experiences very high peak current stress when hard switched in this manner, as in addition to carrying I_{inj} , which mimics i_{pri} , it has to also carry the reverse recovery current of the parasitic diode of TA which is usually many times higher than I_{inj} .

In Figure 6.47, TB undergoes soft switching with $I_{inj} = 8$ A. From the e_{TA} and e_{TB} waveforms, it can be seen that TB achieves lossless ZVS turn-on but would still suffer from turn-off losses (MOSFET TA). There is no current spike on either $i_{sd(TA)}$ or $i_{ds(TB)}$ as the body diode of TA is not used prior to its turn-off.

A ZVS sensing circuitry was implemented in PSPICE which switched TB on when $v_{ds(TB)} < 5$ V with $I_{inj} = 8$ A as in Figure 6.47. The effects of this circuitry is similar to that of TB undergoing normal ZVS turn-on with the major difference that under the adaptive ZVS driving alternative in Figure 6.48, the guess work of setting the timing delay between $v_{drv(TA)}$ and $v_{drv(TB)}$ is eliminated.

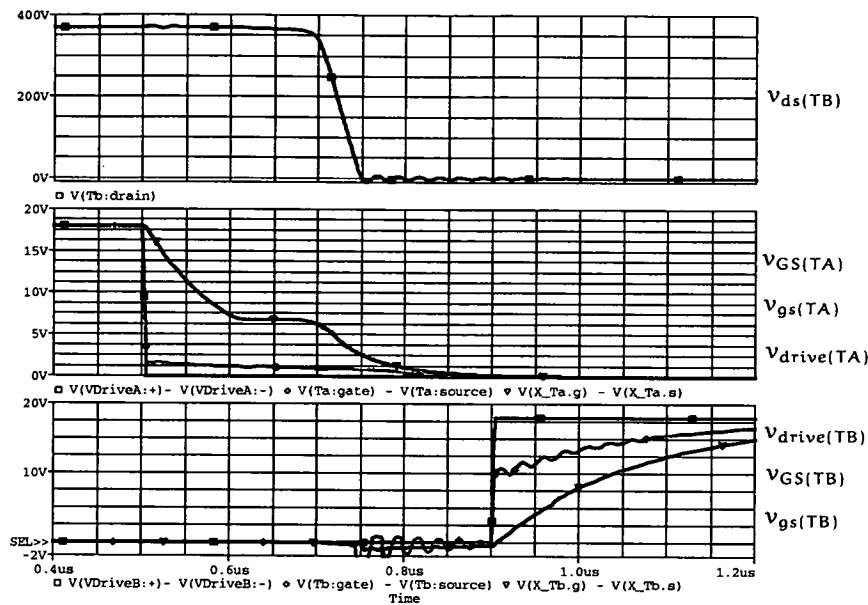


Figure 6.42: Transition Waveforms During Switching of Infineon PSPICE MOSFET Model

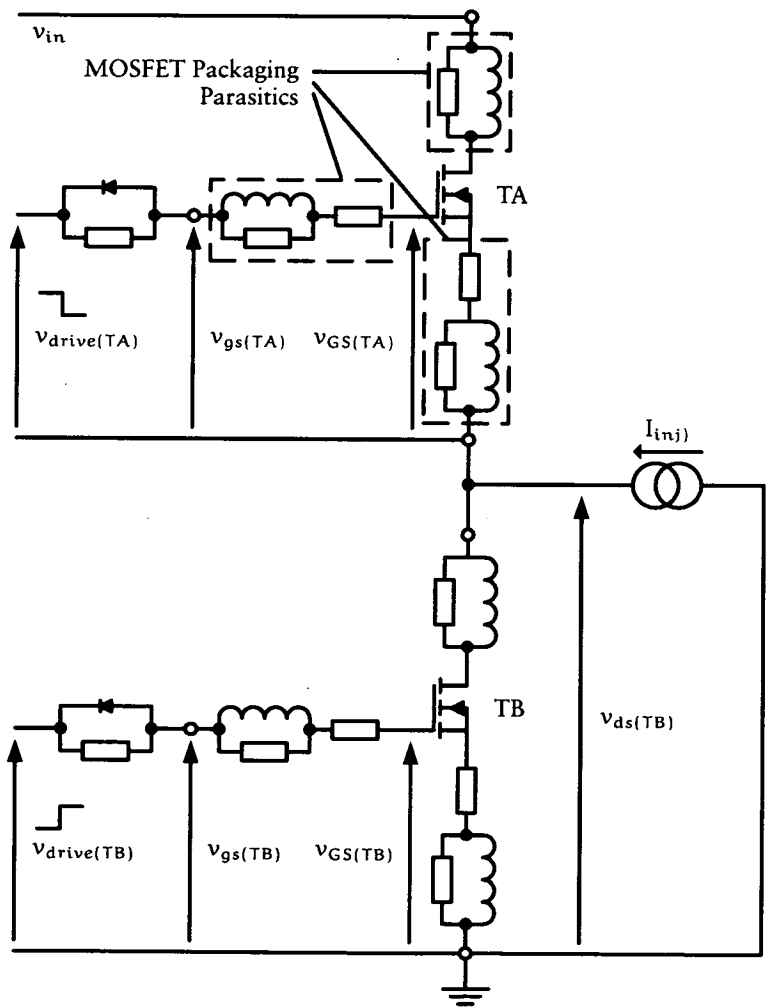


Figure 6.43: PSPICE Schematic for Simulation of Infineon MOSFET Model Switching

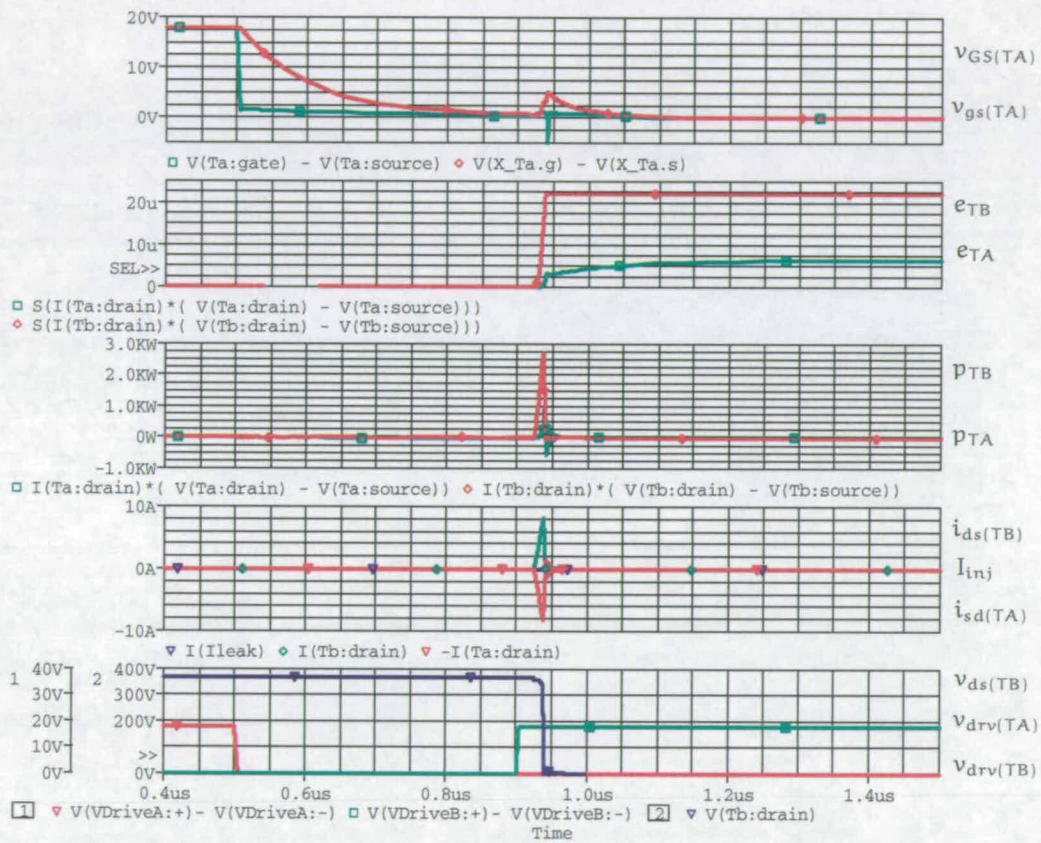


Figure 6.44: PSPICE Simulation of Hard Switching Using Infineon MOSFET Model, $I_{inj} = 0A$

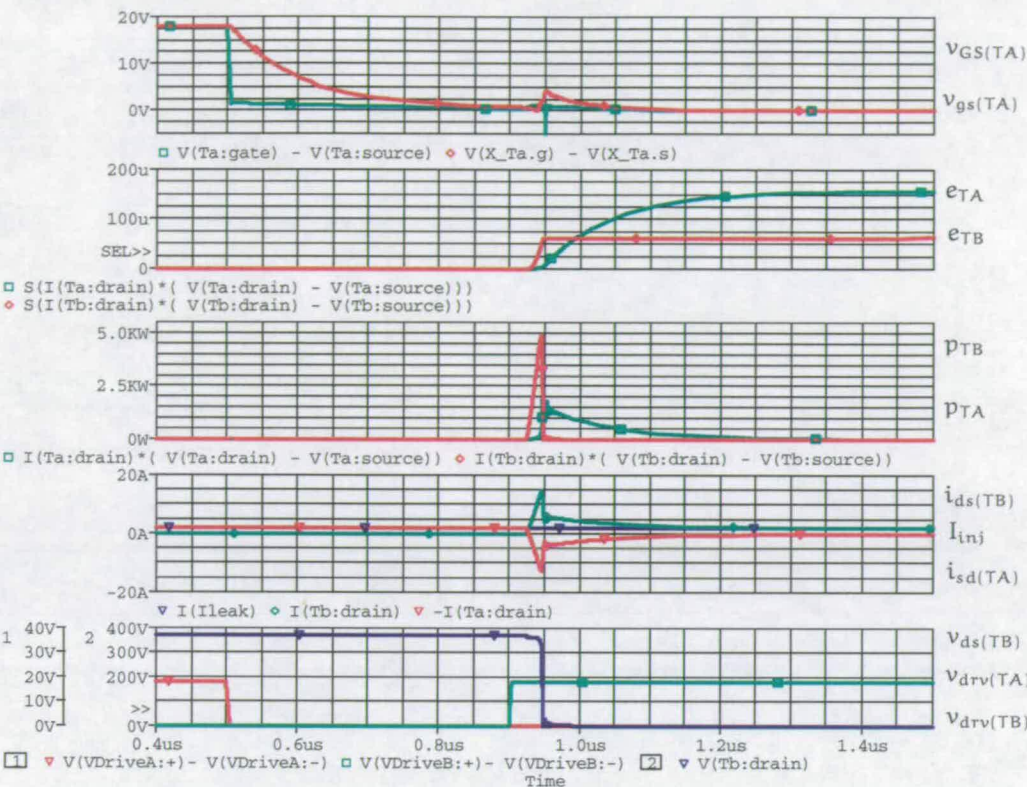


Figure 6.45: PSPICE Simulation of Hard Switching Using Infineon MOSFET Model, $I_{inj} = 2A$

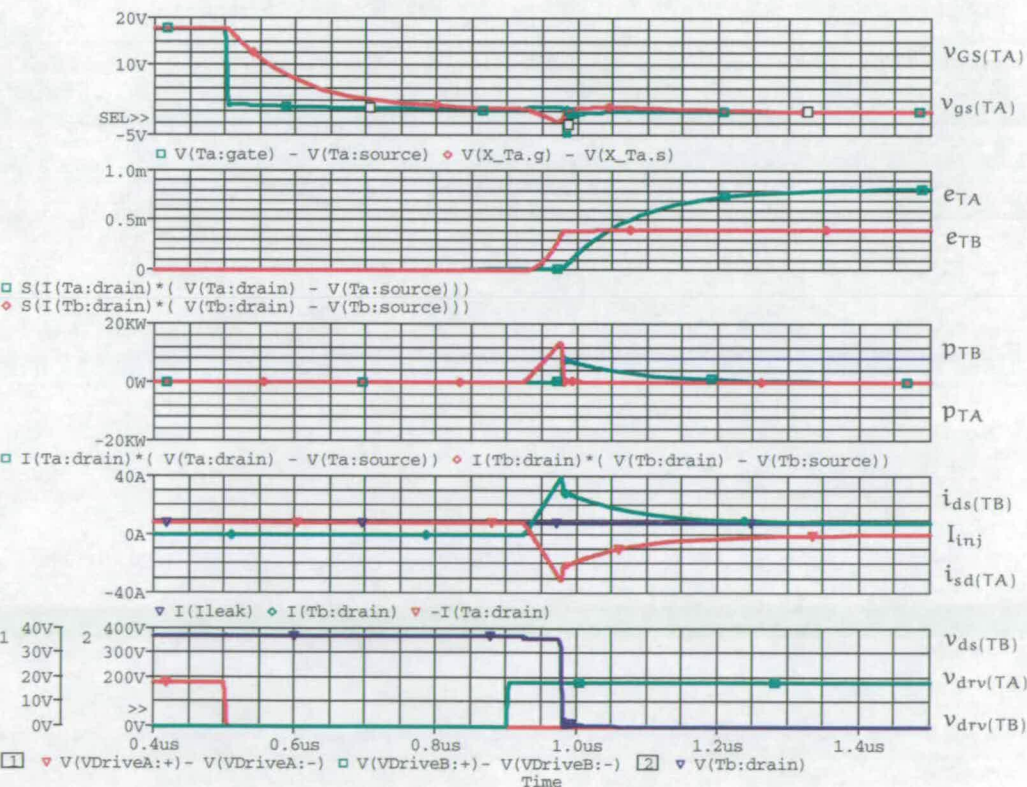


Figure 6.46: PSPICE Simulation of Hard Switching Using Infineon MOSFET Model, $I_{inj} = 8A$

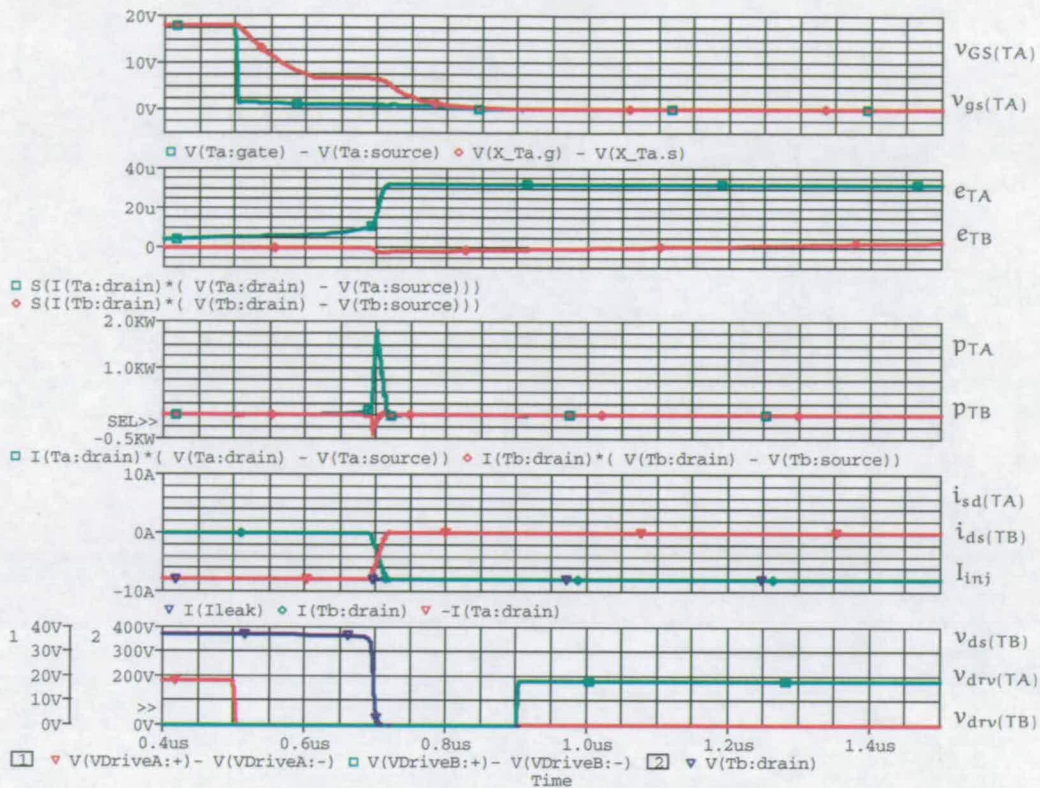


Figure 6.47: PSPICE Simulation of ZVS Transition Using Infineon MOSFET Model, $I_{inj} = -8A$

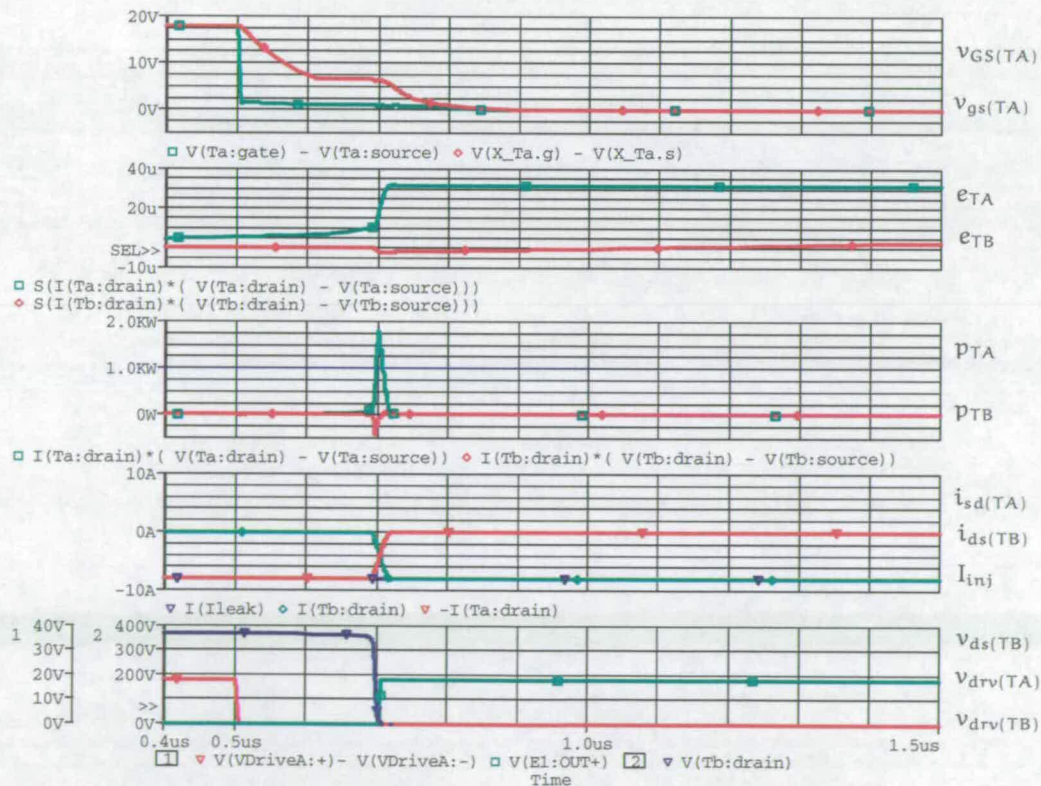


Figure 6.48: PSPICE Simulation of ZVS Transition Using Infineon MOSFET Model with Zero Voltage Sensing Circuitry

6.5 Efficiency and Temperature Readings

The input and output voltages and currents for the prototype PSBCF converter with auxiliary circuits were measured using DC multimeters and are presented in Table 6.2. Waveforms were also taken using oscilloscope DC current and voltage probes and internally multiplied by the oscilloscope itself. 1024 waveforms were averaged and the final waveform itself averaged and the results were found to be reasonably consistent with the meter readings as the waveforms were reasonably DC in nature. However, due to availability of only a single DC current probe, only the results of the multi-meter readings are presented. This is because the converters were running in open loop and readings tended to fluctuate. In addition the current probe had to be zeroed each time it was clamped onto a different wire for accurate results especially on the high voltage low current output line. This made it impossible to achieve accurate instantaneous input and output power readings to obtain the efficiency results. In addition, although the PSBCF converter operating with any auxiliary circuits managed to run at half load, the multimeter readings was affected by noise and did not settle down to allow sensible readings to be taken. This is probably caused by an increased in EMI due to the hard switched nature of the PA leg.

Auxiliary Circuit	LDD	LDD	LCC	LCC
Load	Full	Half	Full	Half
$V_{in}(V)$	369.0	368.5	369.5	370.0
$I_{in}(A)$	2.520	1.290	2.490	1.275
$P_{in}(W)$	929.88	475.36	920.06	471.75
$V_{out}(V)$	1000.0	1000.5	1000.0	1000.0
$I_{out}(A)$	0.844	0.422	0.845	0.422
$P_{out}(W)$	844.0	422.21	845.0	422.0
Efficiency(%)	90.8	88.8	91.8	89.5

Table 6.2: Voltmeter, Ammeter Readings and Efficiency Results

The temperature readings in Table 6.3 were obtained by attaching thermocouples to the semiconductor and load heatsinks and also the windings or the cores of the magnetic components. Due to the sensitivity of the thermocouples to EMI, the readings have to be taken after the converter has settled to a steady state and then switched off to allow readings to be taken. These can only be used to show if components are running hotter than others which may indicate a shortened lifespan and where potential power losses could be achieved by optimising the component selection and design.

	Temperature ($^{\circ}\text{C}$)			
	LDD	LDD	LCC	LCC
Auxiliary Circuit	Full	Half	Full	Half
Load	34.8	34.3	28.4	25.7
TA, TB	30.3	23.4	30.6	26.5
TC, TD	34.1	28.8	33.4	31.8
Transformer Core	39.7	33.2	40.0	38.3
Transformer Windings	27.0	23.6	29.7	27.0
HV Rectifier	33.2	29.1	35.2	32.3
L_{add}	64.6	48.4		
LDD L_{aux}	28.8	25.4		
LDD Diodes			46.1	41.5
LCC L_{aux}	79.7	49.8	76.2	65.5
R_{Load}	20.9	19.1	21.8	21.5
Room Temperature				

Table 6.3: Temperature Readings for Various Converter Components

6.6 Chapter Summary

A prototype was created to validate the operation of the converter and to verify the accuracy of the simulation models used. The simulated results presented in Chapter 6 show good agreement with those measured from the prototype. The converter was tested at output loads of 425 W and 850 W with and without auxiliary circuits such as LDD and LCC. The results show good agreement between simulation and prototype waveforms. The waveforms show that the theory in Chapter 2 is slightly inaccurate as the original theory did not take into account the distributed winding capacitances of the transformer and the junction capacitances of the high voltage rectifier diodes which caused the current to ring during the ‘off’ intervals. This made the solving of the steady state simultaneous equations in Chapter 3 much more difficult, as not only did it mean more equations had to be solved, but the number of additional equations or states are dependent on whether the direction of current flow, after the parasitic resonance in the transformer, resulted in the PA leg MOSFETs turning on with either partial or full ZVS or hard switching. Due to this phenomenon, the PS-BCF without the auxiliary circuit turned on without ZVS at the two output loads and resulted in very high losses. The converter could not run at full output load as the excessive switching losses in the PA leg caused the MOSFETs to fail. Thus, the converter should not operate at such high frequencies without some form of soft switching to reduce switching losses.

The limitations of PSPICE could be seen at times, when accuracy was lost due to the wide voltage and current value ranges present in the circuit which sometimes either caused the circuit to be unable to converge to sensible values or sacrificed precision in order to achieve convergence.

Simulations of an output short-circuit using a low resistance load were simulated on

the various configurations of the PSBCF. These were compared to that of the Current Fed Bridge and the results showed that the PSBCF performed much better in its ability to withstand short-circuits. These simulations were tested based on the worst case scenario where the output voltage completely collapses in less than a cycle, causing the simple voltage control to open its duty to 1 resulting in a high I_{SCmax} . In reality the output voltage will be held up by the output capacitors and the voltage loop will not respond that quickly and the resultant I_{SCmax} would not be as high. The closed-loop short-circuit simulations also verified the averaged model of the PSBCF. The averaged model is reasonably accurate with slight deviations being caused by the parasitic resonance within the transformer.

Waveforms captures for the short-circuit tests for the PSBCF with auxiliaries prove the inherent short-circuit protection of the converter.

Further simulation waveforms show the limitations of the various MOSFET models and the trade-offs which had to be made. Detailed MOSFET models provided good insight into the switching transition of the converter but were useless for normal simulations as PSPICE kept coming up with convergence problems. The simple PSPICE model editor models enabled the simulations to run, albeit slowly, for longer simulations but gave inaccurate switching transitions. Averaged models of the converter were very useful in obtaining general behaviour of the converter over much longer periods of time but are unable to provide much detail into what is happening within a switching cycle. Thus, the models have to be selected with care and the limitations of each understood when using these models to simulate the behaviour of the PSBCF under PSPICE.

Chapter 7

Evaluation, Comparison and Discussion

7.1 Discussion

The prototype PSBCF converters performed well in tests and simulations showed good agreement with the experimental waveforms. However, a couple of problems were encountered when running the PSBCF converter without auxiliaries.

The converter could only carry half the load of 451W at full output voltage. The main problem was that of excessive power loss on the PA leg which caused the MOSFETs to overheat and eventually fail. The secondary problem was that of high $\frac{dv}{dt}$ during hard switching of the PA leg which caused cross-conduction.

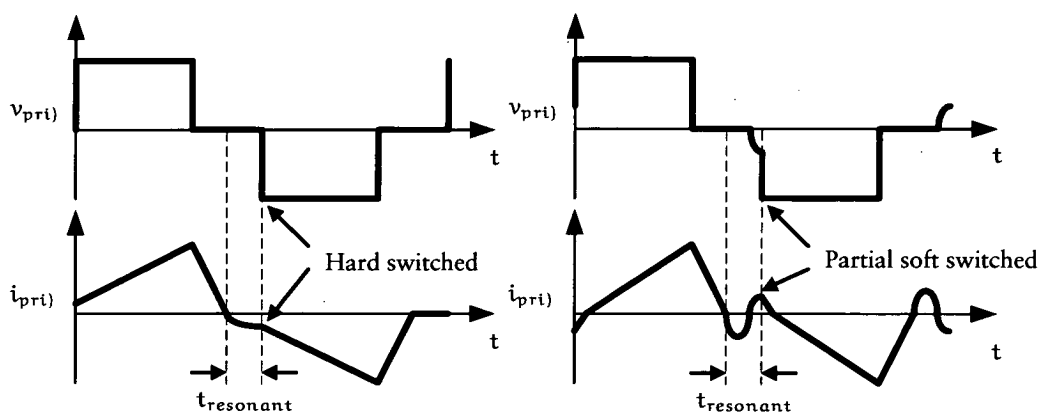


Figure 7.1: Effect of Parasitic Resonance on ZVS: (a) Hard Switched (b) Partial Soft Switching

The excessive power loss is caused by the oscillation within the transformer parasitics. This causes i_{pri} to continue flowing in the MOSFET's parasitic diodes even

after i_{pri} has fallen to zero during the passive interval (Figure 7.1). This oscillation is clearly visible on the i_{pri} waveforms when $v_A - v_B = 0$ in Figure 6.5. When the currents flow in the opposite direction, the body diode of the MOSFET just turned off must conduct. If the complementary MOSFET then turns on during this condition, the MOSFET loses soft switching and resembles a normal hard switched bridge converter where the MOSFET just turned off is now acting as the free wheeling diode (Figures 6.45 and 6.46). The parasitic body diode of the MOSFET is poor and suffers from greater losses than a discrete diode, and the losses are all generated within a package (as opposed to two if a discrete one were to be used). In addition, when the body diode recovers, the turn-on MOSFET must carry this reverse recovery current as well as the transformer current previously flowing, increasing losses (Figure 7.2).

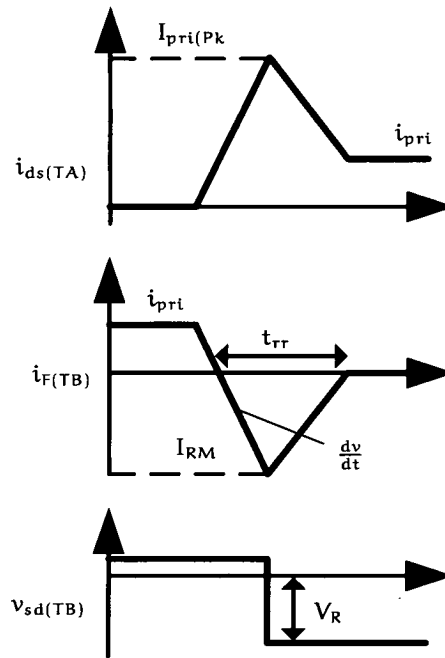


Figure 7.2: MOSFET Parasitic Diode Recovery with High $\frac{dv}{dt}$

This manner of hard switching the MOSFETs gives rise to the problem of the high $\frac{dv}{dt}$ and is similar to that faced by the forward converter with a synchronous rectifier [76]. The MOSFETs on the PA leg plays the main switching role at turn-on and resembles a synchronous rectifier or freewheeling diode upon turn off. This is in contrast to the ideal ZVS PSBCF case where the MOSFET acts as a free wheeling diode before turn-on and conducts as a MOSFET on turn off. The synchronous rectifier forward converter also suffers from high $\frac{dv}{dt}$ when the MOSFET acting as the synchronous rectifier switches off. The high rate of recovery causes its gate-source capacitance to charge up above the threshold voltage and switch itself back on causing cross-conduction.

An important difference between the synchronous rectifier and the PSBCF is that operation of both MOSFETs in the same leg of the PSBCF is identical (apart from

a phase shift of 180°) unlike the forward converter with synchronous rectifier. The difference between the PSBCF and the forward converter with synchronous rectifier is that in the latter the two MOSFETs can be driven at different speeds because the waveforms for the synchronous rectifier MOSFET and main switching MOSFET are not symmetrical. If the source-drain current carried by the MOSFET to be turned off is large then there is the risk of the recovery current being too large for the other MOSFET. If the source-drain current are very small, the body diode will recover much more quickly, resulting in the high $\frac{dv}{dt}$ of the MOSFET v_{ds} . This causes v_{gs} to be pulled up as well, as evident in Figures 6.44 and 6.45. If the value exceeds the MOSFET's threshold voltage, the MOSFET will turn on, causing cross-conduction and very likely destroying both MOSFETs.

A possible solution is to reduce the value of the gate resistance in order for the built up charges in the gate to dissipate before the threshold voltage can be reached. However, the finite parasitic resistance in the MOSFET packing and leads and the output impedance limits the speed at which the charges can dissipate. In addition, by reducing the gate resistance, the MOSFETs will turn-on more quickly, again resulting in the high $\frac{dv}{dt}$ problem. [43] calculates the gate resistance required for both MOSFETs for the case of the forward converter with synchronous rectifier which closely resembles this situation.

The above then makes it pointless to use different gate resistance for MOSFETs on the same leg. Although turn-off enhancement circuitry helps to alleviate the problem by allowing a quick turn-off while limiting the speed at which the MOSFET turns-on, it might still not be quick enough for the fast recovery of the body diode.

The use of a bipolar pulse transformer as shown in Figure 7.3, is a possible solution to the problem. By connecting the driving signals for both MOSFETs to the primary of the transformer, a bipolar driving signal can be generated for both MOSFETs of the leg. This ensures that only one MOSFET can be switched on at a time.

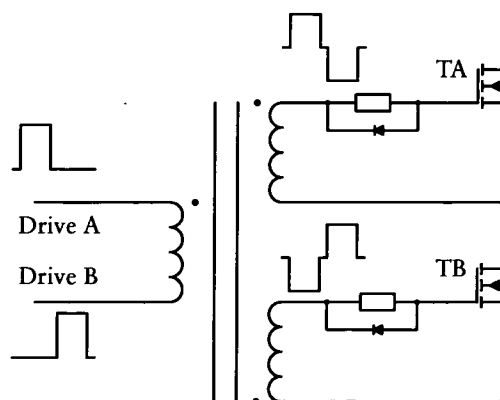


Figure 7.3: Bipolar Gate Pulse Transformer Circuit

As TA is about to be turned on, TB experiences a negative voltage which forces the

MOSFET to be off. The limitation of this approach is that with the use of high current MOSFETs, the gate source capacitance tends to be large. In order to get a good driving waveform at the gate, the resonant frequency of the pulse transformer leakage inductance and C_{gs} should be a couple of decades higher than the switching frequency. This requires a pulse transformer with very low leakage inductance, which most commercial ones are unable to meet.

Early prototypes of the PSBCF without auxiliary circuits failed due to high $\frac{dv}{dt}$ recovery of the body diode when acting as a free wheeling diode in a hard switched mode. Only the gate pulse transformer solution solved the problem, using twisted trifilar wire wound on toroidal transformer cores to reduce leakage inductance. The leakage inductance of most commercial offerings is too high and only a sinusoidal waveform was observed at the gate instead of the required bipolar pulse waveform.

Average Mode Simulation

The PSBCF averaged model does not take into account conduction losses. Therefore, if there are significant losses, *e.g.* switching, conduction or magnetic, then the model does not work as well. The simulation predicts an operating duty slightly lower than in reality. However, the averaged model can still be used for very general behaviour work. The time taken to carry out a simulation is reduced greatly, enabling longer simulations times which would otherwise be impractical due to the long calculation times and the large data files produced. In addition, the averaged model is able to analyse the converter's performance in the frequency domain with Bode plots, which the transient simulation is not able to generate. In Figures 6.27, 6.29, 6.31, 6.33 and 6.34 it can be observed that the waveforms of the averaged models are reasonably close to the waveforms of the switched models. The average model was created assuming an ideal sawtooth waveform, and does not consider the effects of the transformer parasitic oscillation. This accounts for the difference in time required to recover from the short-circuit when compared to the PSBCF with no auxiliaries. When comparing the averaged model to the full simulation of the PSBCF ideal model (with the transformer parasitic capacitances removed), the waveforms match reasonably well (Figures 6.33 and 6.34). The averaged model is able to model the converter in both DCM and CCM mode and transit between the two when operating conditions change. In Figure 6.33 during normal operation at the beginning and at the end, the converter is operating in DCM mode as it was designed to. During the short-circuit and recovery period, the converter operates in CCM mode, where the inherent power limiting nature of the converter is active. In addition to the averaged transformer currents, the model is also able to show the peak transformer currents of each cycle, giving the designer information about current ratings to assist in specifying the appropriate MOSFET for the particular design.

Transient Simulation

The transient simulation has its own limitations. There is a limit to the accuracy with which the parasitics can be included into the simulation model. Magnetic component core hysteresis losses have not been included, as the impedance analyser measuring the component values does so with a maximum excitation voltage of 10V. The MOSFET models used were created using the model editor provided by PSPICE as mentioned in Chapter 6. While these models can be used to simulate the conduction losses, the simulated switching event is not an accurate simulation of the actual circuit. While more accurate models are provided by the manufacturer, these are much more complex and the simulator has difficulty converging to a DC bias point for the simulation. Thus, the manufacturer's models could only be used to examine the switching in detail in isolation from the rest of the circuit.

7.2 Losses

Losses in a SMPS converter can be attributed to the following components:

- Semiconductors: MOSFETs and diodes
- Magnetic components: Transformers and inductors
- Capacitors

The following sections analyses the losses for the PSBCF generated by the various components and compares them to the CFB as a means of evaluating performance.

7.2.1 MOSFET Conduction Losses

Semiconductor losses fall into two categories: conduction and switching losses. Conduction losses are generated due to the finite resistance of the semiconductor when carrying a current. This section estimates MOSFET conduction losses for the various converters and compares them to each other. Calculations assume that semiconductor blocking losses resulting from the leakage currents during the off state are negligible and thus these have been omitted. Some other assumptions made are listed in Table 7.1.

PSBCF MOSFET Losses

The conduction losses for the PSBCF MOSFETs can be calculated by calculating the RMS value of i_{pri} . As the transformer current has to flow through either the top or

	Assumptions for CFB	Assumptions for PSBCF
Current shape	Ripple free due to large L_{Choke}	Ideal sawtooth waveform with no oscillations after i_{pri} has fallen to zero
Transformer turns ratio	1:4	1:4
MOSFETs	Infineon SPW20N60S5	Infineon SPW20N60S5
Diodes	Motorola MUR1560	Motorola MUR1560
Switching frequency	160 kHz (TPWM) 80 kHz (Bridge)	250 kHz
Duty	0.67 (TPWM) 0.95 (Bridge)	0.67

Table 7.1: Assumption Used for Estimating Losses for the CFB and PSBCF Converters

Loss calculation Parameters	Value
MOSFET R_{DSon}	0.19 Ω
Transformer Primary R_{DC1}	16.8 m Ω
Transformer Secondary R_{DC2}	176 m Ω
DC resistance of L_{pri}	20.4 m Ω
DC resistance of LDD L_{aux}	13 m Ω
Forward voltage of LDD D_{add}	1.2 V
DC resistance of LCC L_{aux}	33 m Ω
ESR of LCC C_{aux1}, C_{aux2}	230 m Ω
Forward voltage of HV Rectifiers	2 V
ESR of Filter Capacitors	20 m Ω

Table 7.2: Parameters Used for Loss Estimation

Currents (A)					
CFB			PSBCF		
			No Auxiliary	LDD	LCC
$I_{pri}(Pk)$	3.8	$I_{pri}(Pk)$	8.3	7.8	8.4
$i_{pri}(RMS)$	3.6	$i_{pri}(RMS)$	4.4	4.3	4.6
$I_{TPWM}(Pk)$	3.8	$I_{Laux}(Pk)$		7.8	6.6
$i_{TPWM}(RMS)$	3.1	$i_{Laux}(RMS)$		6.0	3.6
$I_{Lchoke}(Pk)$	3.6	RMS ($i_{pri} - i_{Laux}$)		3.8	4.9
$i_{Lchoke}(RMS)$	3.4	Average ($ i_{pri} - i_{Laux} $)		2.6	

Table 7.3: Current Values Used for Loss Estimation

bottom MOSFETs on the AP leg, and the conduction time for the parasitic MOSFET body diode is small in relation to the main conduction time, the conduction losses for each leg can simply be approximated as $i_{\text{pri(RMS)}}^2 \times R_{\text{DSon}} \cdot d_{\text{cond}}$. d_{cond} is the equivalent duty for when the MOSFET is conducting current.

$$i_{\text{pri(RMS)}} = \sqrt{\frac{1}{3} d_{\text{cond}} \cdot I_{\text{pri(Pk)}}^2} \quad (7.1)$$

$$I_{\text{pri(Pk)}} = 2 \cdot \frac{I'_{\text{sec}}}{d_{\text{cond}}} \quad (7.2)$$

$$i_{\text{pri(RMS)}} = \sqrt{\frac{4}{3} \frac{1}{d_{\text{cond}}} \cdot I'_{\text{sec}}^2} \quad (7.3)$$

$$d_{\text{cond}} = d \frac{V_{\text{in}}}{V'_{\text{out}}} \quad (7.4)$$

$$I'_{\text{sec}} = \frac{1}{2} (V_{\text{in}} - V'_{\text{out}}) \cdot d^2 \frac{T_{0.5} V_{\text{in}}}{L_{\text{pri}} V'_{\text{out}}} \quad (7.5)$$

$$d = \sqrt{\frac{2 I'_{\text{sec}} L_{\text{pri}} V'_{\text{out}}}{T_{0.5} V_{\text{in}} \cdot (V_{\text{in}} - V'_{\text{out}})}} \quad (7.6)$$

$$i_{\text{pri(RMS)}} = \sqrt{\frac{4}{3} \cdot \sqrt{\frac{T_{0.5} V'_{\text{out}} \cdot (V_{\text{in}} - V'_{\text{out}})}{2 I'_{\text{sec}} L_{\text{pri}} V_{\text{in}}}} \cdot I'_{\text{sec}}} \quad (7.7)$$

If there are no auxiliary circuits attached to the PA leg, the conduction losses should be the same as those for the AP leg. Conduction losses for the PSBCF bridge MOSFETs can be compared to those in an ideal CFB by making the assumptions listed in Table 7.1.

By substituting the circuit parameters into Equation 7.7, and plotting $i_{\text{pri(RMS)}}/I'_{\text{sec}}$ against I'_{sec} , the increase in RMS transformer current due to the discontinuous nature of the phase shifted bridge can be shown (Figure 7.4). Figure 7.4 shows that the RMS current can be up to three times the average current at very low I'_{sec} currents. The difference is not as noticeable when the loading is close to full load at the boundary condition I'_{secBC} (5.068 A) where $i_{\text{pri(RMS)}}$ is only 1.155 times of I'_{sec} .

By using an R_{DSon} value of 0.19Ω for the SPW20N60S5 MOSFET, a plot of the conduction losses per leg is shown in Figure 7.5 for both the PSBCF and the CFB

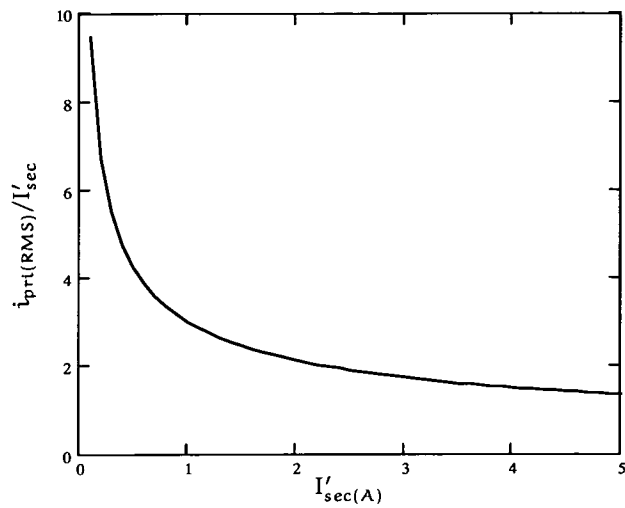


Figure 7.4: Graph of PSBCF $i_{pri(RMS)}/I'_{sec}$ Against I'_{sec}

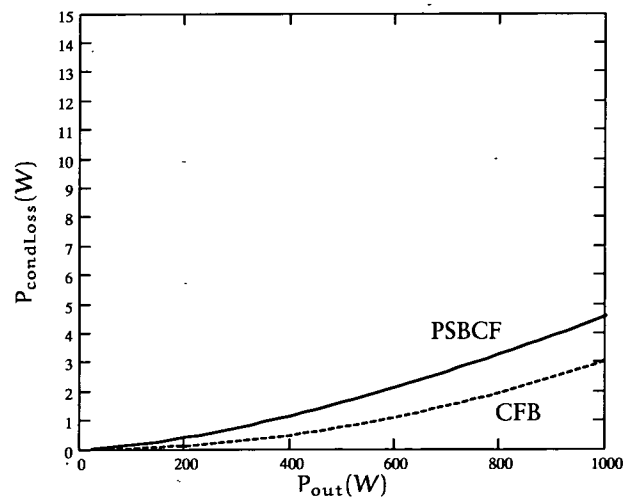


Figure 7.5: MOSFET Conduction Losses Against Output Power

converter. It can be seen that at 1 kW output power, although conduction losses have increased by about 50%, it only represents 0.15% of the total output power.

If the LDD auxiliary circuit is employed, the current entering the PA leg can be assumed, in the worst case scenario, to have an AC pulsed waveform of $\pm I_{pri(pk)}$. This can only occur if the auxiliary diodes can recovery instantaneously and that the peak recovery current value is that of the the forward peak transformer current.

$$i_{L_{aux}(RMS)} = I_{pri(pk)} \quad (7.8)$$

See Equation 7.2 – 7.4

$$d_{cond} = \sqrt{\frac{2I'_{sec}L_{pri}V_{in}}{T_{0.5}V'_{out}(V_{in} - V'_{out})}} \quad (7.9)$$

$$i_{L_{aux}(RMS)} = \sqrt{\frac{2I'_{sec}T_{0.5}V'_{out} \cdot (V_{in} - V'_{out})}{L_{pri}V_{in}}} \quad (7.10)$$

Figure 7.6 shows the MOSFET conduction power loss at various output powers for the PSBCF PA leg compared with that of an ideal CFB converter. The difference in power loss between the two is only 0.65% of the output power at 1 kW.

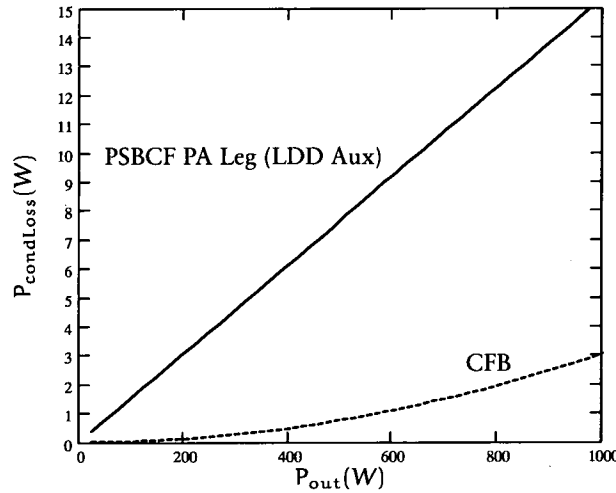


Figure 7.6: MOSFET Conduction Losses for PA Leg with LDD Auxiliary Against Output Power

As for the PA leg with the LCC auxiliary circuit, the waveform is more difficult to generalise and the simplest method of finding the RMS currents is to create the waveform equations using MATHCAD and calculate the RMS currents and averaged currents at various duties. The conduction power loss values obtained are then plotted against the output power obtained at the respective duties (Figure 7.7).

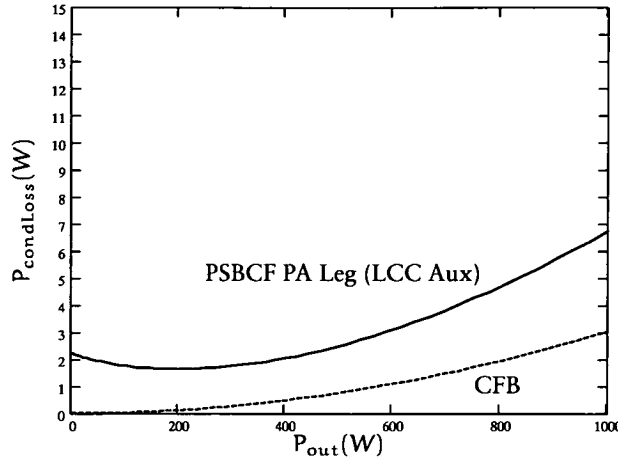


Figure 7.7: MOSFET Conduction Losses for PA Leg with LCC Auxiliary Against Output Power

Although MOSFET switching losses are greatly reduced using ZVS techniques, from eliminating MOSFET turn-on losses, there would still be some MOSFET switching losses due to turn-off. Equation 7.11 can be used to estimate the MOSFET turn-off losses [26].

$$P_{Sw} = \frac{1}{2} \cdot f_{Sw} V_{dsOff} i_{dsOff} t_{fall} \quad (7.11)$$

where i_{dsOff} is the drain-source current flowing in the MOSFET just prior to being turned off.

Turn-off losses depend on how quickly the gate charge can be removed from the gate capacitance and can be reduced by using better MOSFET gate drive circuitry which is capable of turning off the MOSFET faster. One such enhancement for the gate drive circuitry is the use of the anti-parallel diode, D_{TX} , which reduces the gate drive impedance when turning off the MOSFET which allows the gate-source capacitance to be discharged quickly (Figure 6.1). In addition, the value of i_{dsOff} depends on the leg on which the MOSFETs are located on. i_{dsOff} for the PA leg is particularly difficult to estimate any degree of accuracy. As such, MOSFET switching losses were obtained more accurately using the PSPICE waveforms.

Power Loss Estimation Using PSPICE Waveforms

Power loss for any device can be calculated from the SPICE waveform using Equation 7.13.

$$e_{TX} = \int_{t1}^{t2} i(t)v(t)dt \quad (7.12)$$

MOSFET Losses (W)					
CFB		PSBCF			
		No Auxiliary	LDD	LCC	
TA – TD (80 kHz)	PA leg (250 kHz)				
P_{Sw}	28.48	P_{Sw}	54.82	7.18	2.91
P_{Cond}	4.14	P_{Cond}	3.32	6.71	4.11
TA – TD Total	32.61	PA Total	58.14	13.90	7.01
TPWM (160 kHz)	AP leg (250 kHz)				
P_{Sw}	24.88	P_{Sw}	7.45	8.25	9.52
P_{Cond}	1.46	P_{Cond}	5.68	3.33	4.09
TPWM Total	26.35	AP Total	13.13	11.58	13.61
Total	58.96		71.27	25.48	20.62

Table 7.4: MOSFET Losses for the Various Converters

$$P_{loss} = f_{sw} \cdot e_{TB} \quad (7.13)$$

The procedure is as follows. Multiply the current and voltage waveforms for the device of interest and integrate with respect to time. Then pick the difference in the integration values between the start and end times of the particular event to be measured and multiply the energy difference by the switching frequency of the device to calculate the power loss (or gain) contributed to the overall loss by the event.

From e_{TX} traces in Figures 6.44 to 6.48, the turn-off losses for TA and turn-on losses for TB can be observed under hard switching and ZVS conditions. Any negative power dip is caused by device capacitance, such as MOSFET C_{oss} , returning energy to the system, causing a gain in energy, when the MOSFET is soft switched. This can be observed in the trace for e_{TB} in Figures 6.47 and 6.48.

This method of estimating component power loss is more accurate, if a steady-state simulation of the converter can be performed, as the current waveform can be more accurately simulated than the quick estimation method mentioned above. Continuing with this PSPICE method of loss estimation for MOSFETs in the various converters, Table 7.4 presents a summary of the losses incurred when running at 1 kV, 850 W.

CFB TPWM MOSFET Losses

Assuming that the CFB is running with a duty similar to that of the PSBCF at full load ($d = 0.667$), transistor TPWM in the CFB then conducts load current for two thirds of the period while D1 conducts for the other third. The RMS currents and conduction losses ($P_{condTPWM}$) can then be calculated using Equation 7.14 and 7.15.

$$i_{pri(RMS)} = I'_{sec} \sqrt{d} \quad (7.14)$$

$$P_{condTPWM} = I'^2_{sec} d \cdot R_{DSon} \quad (7.15)$$

Equation 7.16 can be used to perform a quick estimate of switching losses for the CFB MOSFETs [26].

$$P_{Sw} = \frac{1}{2} \cdot f_{Sw} V_{dsOff} i_{dsOff} (t_{rise} + t_{fall}) \quad (7.16)$$

7.2.2 ZVS Sensing Drive Circuitry

As shown in Section 7.1 and 7.2.1, the body diode of the MOSFET should be used with care. It should not be used as a conventional free-wheeling diode as the turn-off losses incurred makes the converter inefficient and unreliable. Even when the body diode is being used to provide ZVS for the MOSFET, it has been found to cause converter failure under extreme operations as mentioned Chapter 2. An alternative is to implement a zero voltage sensing circuit to automatically sense the presence of the zero voltage condition before switching on the MOSFET. Figure 7.8 shows one such circuit adapted from one proposed by [77].

The ZV sensing circuit is broken up into three parts:

1. Zero voltage zero current detector
2. Gate pulse rising edge detector
3. Gate pulse falling edge detector

The comparator senses a low voltage at the drain - source terminals of the MOSFET and outputs a low (0) signal. If the gate drive signal is low too, then logic gate 2 will output a high (1) signal to turn the MOSFET on. Having switched the MOSFET on, the comparator senses the non-zero current condition and gate 3 will keep the MOSFET switched on as long as the output of gate 7 is high.

The gate pulse rising edge detector uses an RC network and comparator to delay and invert the gate pulse signal. The original gate pulse signal is then compare to its inverted delayed counterpart by gate 4 which effectively senses the rising edge of the signal. By using a different logic gate (gate 5) to compare the signals, a falling edge detector is achieved. However, unlike the rising edge detector, the falling edge detector outputs a low signal when a falling edge is detected.

The three logic components are then linked up using gates 6 and 7 which switched on the MOSFET when either $v_{ds} = 0$ and the gate signal is still low, or when the gate signal is turned on. The MOSFET is switched off when either the gate signal is still high and a zero drain source current is detected, or when a falling edge is detected on the gate signal.

The circuit can be set to switch the MOSFET on when a low v_{ds} is sensed instead of zero to ensure that the body diode does not conduct. Efficiencies will not be greatly affected as most of the energy stored in the MOSFET C_{oss} would have been recovered.

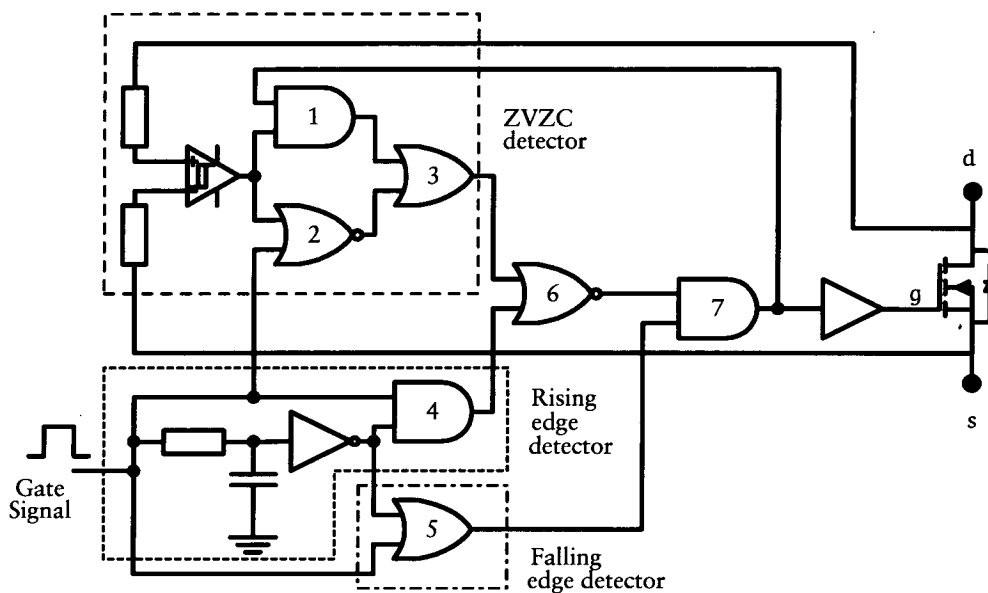


Figure 7.8: Automatic ZVS Sensing Drive Circuitry

7.2.3 Diode Losses

If the opposing MOSFET is turned on too quickly under hard switching operation, the parasitic diode recovery losses will be high. Conversely, a slow turn-off increases turn-off losses. Thus a fast turn-off circuit is needed while keeping turn-on slower. The main diode losses occur during turn-off where the reverse recovery charges have to be supplied while the diode is recovering to its full reversed state (Equation 7.17).

$$P_{Doff} = f_{sw} \cdot 0.5 \cdot \frac{Q_{rr}}{t_{rr}} V_{rr} \quad (7.17)$$

The diode turn-on losses can be assumed to be negligible. Assuming that the diodes have no dynamic resistance (which adds an additional resistive loss to that cause by the forward voltage) the conduction losses can be estimated using Equation 7.18.

Converter	CFB		PSBCF		
	Transformer	Transformer	L_{add}	LDD L_{aux}	LCC L_{aux}
Frequency (kHz)	80	300	250	50	50
ΔB (mT)	0.14	0.066	0.516	0.1	0.1
Manufacturer	Philips	Philips	Sprang Magnetics	MMG	MMG
Material	3F3	3F3	A2	Genalex VH	Genalex V
P_{LD} (mWcm ⁻³)	200	150	752	2000	600
V_e (cm ⁻³)	158	158	20.65	5.42	10.30
P_{loss} (W)	31.6	23.7	15.53	10.84	6.18

Table 7.5: Core Loss Information for the Various Magnetic Components

$$P_{Dcond} = I_{pri} V_F \quad (7.18)$$

The average currents entering the diode leg of the LDD auxiliary can simply be obtained by subtracting the average transformer primary winding current from the average auxiliary inductor current. Since it is assumed that $i_{L_{aux}} = I_{pri(pk)}$, the average value is simply the difference between the $I_{pri(pk)}$ and I_{pri} . In addition, due to the presence and operation of L_{aux} , the energy stored in the auxiliary diodes reverse recovery charge is not dissipated during switching but transferred to L_{aux} . Thus, the auxiliary diodes mainly suffer from conduction losses.

The body diodes for MOSFETs tend to be poorly characterised, with only a few characteristics provided by manufacturers which are condition specific. This prevents the calculation of any sensible loss values. However, the detailed MOSFET SPICE models are more revealing and can provide an estimate to the losses incurred.

7.2.4 Magnetic Component Losses

Magnetic components such as transformers and inductors suffer mainly from two forms of losses: resistive losses of the windings and AC hysteresis core losses. A simple method of estimating copper losses is to measure the DC resistance, and multiply it by the RMS current squared. However, this is a basic estimate and does not include other effects such as skin depth and proximity effect. Due to the lack of information for the CFB L_{choke} , winding losses were assumed to be roughly equivalent to that of the auxiliary inductors used.

Hysteresis losses can be estimated by obtaining the power loss per unit volume P_{LD} for the core material. This requires knowledge of the operating frequency, flux density and volume of the component. An example is shown in Table 7.5.

Core losses for L_{choke} are assumed to be zero because the choke mainly carries DC current with a low AC ripple. Hysteresis losses will also be low.

Unfortunately, the core loss information for Genalex cores used is not detailed and

	Losses (W)			
	CFB	PSBCF		
	80 kHz	250 kHz		
		No Auxiliary	LDD	LCC
P_{SwMOSFET}	53.36	62.27	15.43	12.42
$P_{\text{CondMOSFET}}$	5.60	9.00	10.04	8.20
$P_{\text{TotalMOSFET}}$	58.96	71.27	25.48	20.62
$P_{\text{SwFWDiode}}$	0.03			
$P_{\text{CondFWDiode}}$	0.79		2.33	
P_{HVRect}	1.64	1.62	1.69	1.69
P_{Diodes}	2.45	1.62	4.02	1.69
P_{XfmrWdg}	0.35	0.54	0.54	0.57
P_{XfmrCore}	31.60	23.70	23.70	23.70
P_{LpriWdg}		0.40	0.40	0.42
P_{LpriCore}		15.53	15.53	15.53
$P_{\text{LChokeWdg}}$	0.50			
$P_{\text{LChokeCore}}$	0.00			
P_{LauxWdg}			0.50	0.42
P_{LauxCore}			10.84	6.18
$P_{\text{Magnetics}}$	32.45	40.16	51.51	46.82
P_{CEsr}	4.77m	9.38m	9.66m	11m
P_{CauxEsr}				1.47
$P_{\text{Capacitors}}$	4.77m	9.38m	9.66m	1.48
Total Losses	93.87	113.06	81.01	70.61
P_{out}	851.00	851.00	851.00	851.00
P_{in}	944.87	964.06	932.01	921.61
Efficiency	90.07	88.27	91.31	92.34
Percentage Loss	9.93	11.73	8.69	7.66

Table 7.6: Breakdown of Estimated Losses for the Various Converters

power loss was calculated from data obtained under the manufacturer's test condition.

7.2.5 Overall Estimated Losses

The overall estimated losses for the CFB, the PSBCF with no auxiliaries, the PSBCF with LDD and the PSBCF with LCC are tabulated in Table 7.6. Generally, operating the PSBCF with auxiliary circuits reduces total MOSFET losses by more than half, with the LCC auxiliary circuit offering even greater savings. Although the total conduction losses for the PSBCF MOSFETs are increased in comparison to the CFB converter, this is more than compensated for by the reduction in switching losses.

The reduction in switching losses is significant in that the PSBCF converter is operating at a much higher frequency of 250 kHz while still managing to reduce switching losses when compared to the CFB which only operates at a switching frequency of 80 kHz. It is the significant amount of switching losses which prevents the CFB converter from operating at higher frequencies to provide a better performance for the TWT radar. MOSFETs on the AP leg of the PSBCF with LDD auxiliary have lower losses (Table 7.4) than the those of the PSBCF with LCC auxiliary due to the lower peak and RMS currents present in L_{pri} (Table 7.3) due to the placement of the LDD L_{aux} in series with the transformer resulting in a larger impedance value. However, the PA leg of the PSBCF with LDD auxiliary does not perform as well (Table 7.4) due to the higher circulating currents in the auxiliary (Table 7.3) and overall, the LCC auxiliary circuit performs slightly better than the LDD auxiliary circuit in reducing MOSFET losses.

The PSBCF converter without auxiliary circuit might appear to have a reasonably high efficiency in the Table 7.6 estimates, but it is important to note that most of the losses are actually MOSFET switching losses (Table 7.6) in particular, switching losses for the two MOSFETs on the PA leg of the converter (Table 7.4). The MOSFETs are unable to dissipate the large amount of heat generated and therefore the converter fails.

The use of either auxiliary circuit naturally results in higher losses for the components which makes up the circuit. *i.e.* The LDD auxiliary circuit will suffer greater diode losses and the LCC auxiliary circuit will have greater capacitor losses. However, it is probably easier to reduce the capacitor losses for the LCC auxiliary circuit, by using large electrolytic capacitors with low ESR values which would also function input bulk capacitors. Reducing diode conducting losses is quite difficult at the forward voltage rating of a diode tends to increase with increasing reverse blocking voltage and the high input voltage of the converter forbids the use of Schottky diodes.

It is very difficult to accurately compare the losses in the magnetic components of the converters for several reasons. Firstly, the specifications for the CFB magnetic components were not available and a very rough estimate is provided to provide some of idea of the losses which might be incurred. The loss values of the CFB magnetic components were given a very low and ideal estimate so that any increase in efficiency when comparing the PSBCF to the CFB is not due to an over estimate of the CFB magnetic losses. Next, the auxiliary inductor designs were not optimised for both auxiliaries due to the lack of MPP cores available and the limited core material data supplied by the manufacturer which prevents core losses from being accurately estimated. Finally, high frequency AC losses were not included for any of the components. These AC losses are a result of skin effect, proximity effect, many attempts have been made to estimate these losses [78, 79], however, due to the two reasons listed above, an accurate estimate of the AC losses would not significantly increase

the accuracy of the overall estimate of the magnetic component losses. The R_{AC} resistance used to model the AC losses are only a rough estimate as the transformer was not tested at the full input voltage to test the core loss with the actual flux swing when used in the converter.

Overall the estimate efficiency of the PSBCF with LCC auxiliary is around 92% at full load compared to 91% for the PSBCF with the LDD auxiliary circuit. This compares reasonably well to the efficiency readings taken off the prototype converter (Table 6.2) at full load. The efficiency of the actual CFB approximately 80% (efficiency value provided by Mr Frank Fisher of BAe Systems). The difference in efficiency reading could be assigned to an under-estimate of the magnetic component losses, increased component count and losses due to operating at the output load of 1 kW at 25 kV full output voltage instead of 851 W at 1 kV. Losses of the control circuitry and circuits which provide monitoring services to the main converter are also included.

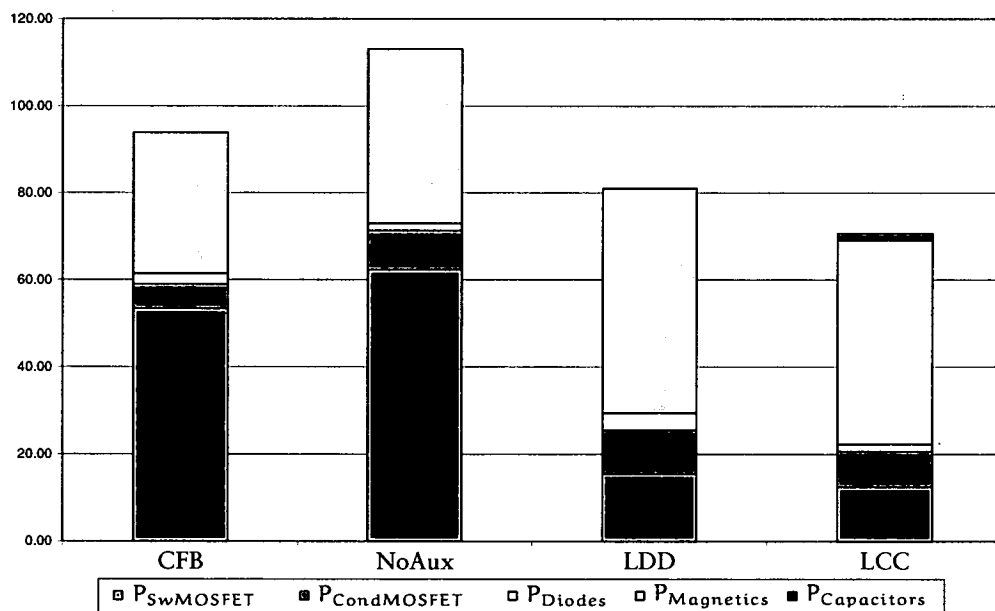


Figure 7.9: Chart of Losses for the Various Converters

7.3 Comparison of PSBCF with CFB

From experiments with the various prototype PSBCF, it was found that operation of the PSBCF without auxiliaries on the PA leg is not suitable without modifying the PA leg with snubbers to reduce the losses caused by the hard switching. Although the PA leg of the PSBCF was initially thought to operate with a ZCS turn-on, this was found to be incorrect due to the presence of parasitic capacitances in the transformer which caused oscillations during the off period which resulted in current flowing.

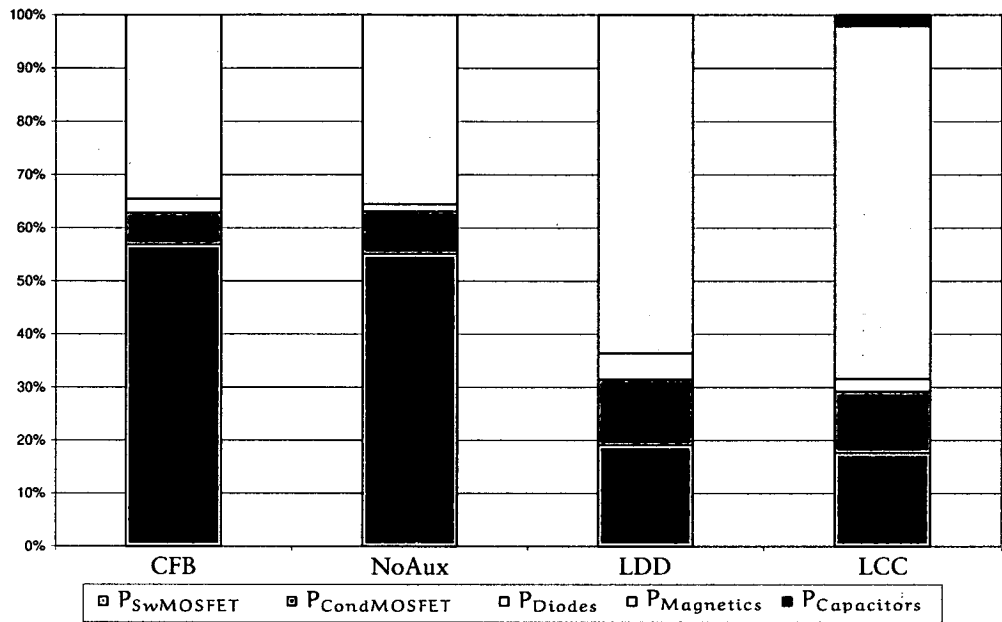


Figure 7.10: Chart of Losses Expressed as Percentage of the Overall Losses for the Various Converters

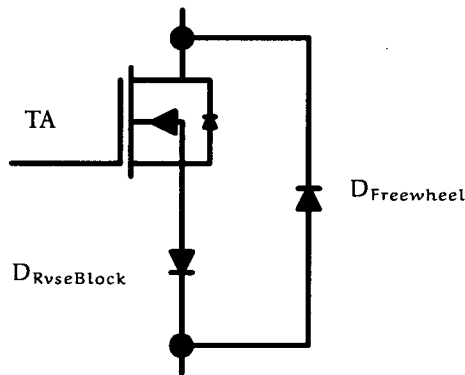


Figure 7.11: Diode Modifications to MOSFET to Prevent Body Diode Conduction

The current could be diverted away from the main MOSFETs by using blocking diodes ($D_{RVseBlock}$) in series with the MOSFET together with freewheeling diodes ($D_{Freewheel}$) (Figure 7.11). However, the dumping of charge stored in the MOSFET C_{oss} and reverse recovery losses of the $D_{Freewheel}$ would still occur every switching cycle. Thus, operating the PSBCF without auxiliaries would require more additional components to make it work efficiently than by using either one of the auxiliaries. The use of the auxiliaries has an added benefit of helping avoid cross-conduction by subjecting the MOSFET just switched off to the reverse blocking voltage under resonance when both MOSFETs are switched off. This is unlike the hard switched condition where the turn-off MOSFET experiences a high $\frac{dv}{dt}$ (limited only by the turn-on speed of the other MOSFET when it turns on risking cross-conduction).

By operating with soft-switching, the converter is able to reduce switching losses and increase efficiency to over 90% at an output power of 851 W. This allows the PSBCF converter with auxiliaries to operate at a much higher switching frequency of 250 kHz.

7.4 Short-circuit Performance

From Figures 6.29, 6.31, 6.39 and 6.40 it can be observed that during an output short-circuit, the PSBCF performs as designed with the transformer primary currents never exceeding I_{SCmax} , unlike the CFB which is only able to limit the rate of increase in choke current but not the current itself. When using the LDD auxiliary circuit, the short-circuit peak current is further reduced due to the presence of the L_{aux} in series with L_{pri} . If the current is not sensed and the converter shut down, all MOSFETs will eventually be destroyed. The PSBCF converter is resistant to output load short-circuits due to the location of its main inductor. By having the inductor in series with the transformer, it experiences bipolar excitation and thus carries no DC current. If an extended period of short-circuit is anticipated, appropriate cooling must be provided for the MOSFETs. If current sensors are used in addition to the inherent protection, this will enable the short-circuit or overload condition to be detected much earlier as the currents will rise to its designed maximum value much quicker (in half a cycle for Figures 6.30 and 6.32) as it does not have a large choke to slow the current rise thus delaying the detection.

However, tests of the PSBCF with no auxiliaries have shown that the PSBCF is not protected against cross-conduction failures where MOSFETs on the same leg conduct simultaneously. The likelihood of this occurring can be reduced by the use of bipolar driving signals for the MOSFETs and also over-current sensors to the input of the bridge to shut down the converter when such a situation is detected. However, the converter has no inherent protection built in, unlike the use of L_{choke} for the CFB.

Advantages of the PSBCF

The large input choke previously required by the CFB is now replaced by a smaller inductor in series with the transformer and a small auxiliary inductor. By removing the DC choke and operating in DCM the PSBCF should be able to respond to transients more quickly.

The series PWM MOSFET used in the CFB is not required in the PSBCF. This reduces the control chip required to only one, simplifying the design. The PSBCF has no need for anti-parallel diodes or snubber circuitry around the MOSFETs. If ZVS sensing circuitry is implemented, there would be no need to use MOSFETs with fast recovery body diodes to reduce the chance of failure while operating with extremely small duty ratios.

Due to the reduction in losses, the heatsink requirements of the converter can be reduced to provide the same operating temperatures for the semiconductors. Conversely, if the heatsinks remained the same, the semiconductors will run cool providing better reliability.

With the increase in efficiency, obtained primarily from the reduction of switching losses, the operating frequency of the converter can be increased to enable synchronisation with the radar. When using the PSBCF with the LDD auxiliary circuit the short-circuit performance is better than with the LCC auxiliary, with lower peak short-circuit currents due to the increased inductance between the legs of the bridge.

Disadvantages of the PSBCF

Due to the discontinuous nature of the current waveform, conduction losses increased due to the increased RMS value. However, this is more than compensated for by the reduced switching losses. The PSBCF MOSFETs will experience higher peak currents during normal operation when compared to the CFB.

When using the LDD circuit the converter suffers from duty cycle loss due to the reverse recovery time of the auxiliary diodes. This can be compensated for by designing the converter with a lower L_{pri} value, which would not appreciably affect the short-circuit peak current due to the presence of the additional L_{aux} .

Unfortunately, by not using L_{choke} , the converter now lacks the ability to protect itself against cross-conduction faults. This is not necessarily crucial if the right MOSFET driving circuitry is used as explained at the beginning of this chapter.

Generally, although efficiencies have been improved, the magnetic losses can be further reduced by optimising the magnetic components.

7.4.1 Limitation of Simulation

Simulations are useful in showing how the converter operates, but are limited in a few ways.

One particular limitation, as mentioned previously, is the trade-off between accuracy and complexity of the simulation. The use of simple component models or averaged converter models allows the designer to quickly observe operation but may be inaccurate in the finer details such as during switching transition or losses prediction. They allow simulations to be carried out much more quickly than when using complex models, which sometimes cannot be run when integrated into the main simulation due to convergence problems. Therefore various levels of detailed simulation have to be carried out in order to be able to observe details on different time scales. Thus, care has to be taken not to extract too much detail from a simulation which it has not been designed for, and the results should always be verified with experimental converter readings as in Chapter 6.

Another limitation of simulations is the lack of temperature data. Some component models include such a feature to alter the component's behaviour when operated under different temperatures. Temperature dependent models are useful in determining failure modes where components overheat due to excessive power loss. Although power loss can be calculated by PSPICE, it does not necessarily mean that the operation falls within the safe operating area suggested by the manufacturer.

These PSPICE simulations can be extended to simulate the converter in the actual 25 kV high voltage output for a pulsed TWT load to observe its performance for the actual application. This is simply achieved by using 25 stacked secondary rectifier sections each with a secondary to primary turns ratio of 1:4 to maintain the optimal modulation index for maximum output power. As the operation of the converter on the primary side of the transformer has been proved to work in both simulations and actual prototype waveform captures, the model should work even when the secondary output voltage is stepped up. However, the model will need to reflect the actual components of the converter in order for the simulation results to be sensible and accurate. For example, the transformer needs to be accurately modelled so that the effects of the parasitics can be studied and checked to see that it does not affect the operation of the converter significantly. The design of the converter might then require adjustments in order to compensate for the parasitics of new transformer and additional high voltage rectifier sections, *e.g.* L_{pri} might need to be reduced if L_{leak} is increased and the inductor values for the auxiliary circuits might need to be re-adjusted if the parasitic capacitances of the transformer is increased to ensure ZVS for the PA leg. With these adjustments made to the PSPICE model, the model should be able to accurately model the converter's performance when used in a high output voltage environment.

7.5 Chapter Summary

Chapter 7 highlights some of the problems faced when prototyping the PSBCF converter. One of the more serious problems is that of cross-conduction which this converter has no inherent protection against, unlike the current fed bridge which has the large DC choke to slow current rise. One of the causes of this problem is due to the parasitic ringing which results in the hard switching of the MOSFETs on the PA leg. This problem is easily solved by using either of the auxiliary circuits to aid soft switching. Cross-conduction and shoot-through can also be caused by incorrect programming of the transition delay on the UC3879 chip. Although the time taken for the resonant transition can be calculated, the lead inductance of the MOSFET package caused the turn-off to take much longer than expected. Switching on one MOSFET when the other on the same leg has not been totally switched off resulted in a cross-conduction situation. This was solved later by the use of bipolar gate pulse transformers to drive all the bridge MOSFETs.

Loss comparisons between the various configurations of the PSBCF and current fed bridge showed that although the PSBCF converter components carried a greater RMS current due to the discontinuous operation, the overall savings from the reduction in switching losses resulted in an increase of efficiency from around 80% for the current fed bridge to over 90% for the PSBCF with auxiliaries. Equally important is that this was achieved at a switching frequency of 250 kHz instead of the 80 kHz used previously. Switching frequency was previously limited by switching losses, as would also be the case in the PSBCF converter without an auxiliary circuit when the PA leg failed due to loss of ZVS. A possible ZVS sensing MOSFET driving circuit is suggested which should enable the MOSFETs to optimally switch under ZVS.

From the tests carried out, it is found that the PSBCF with LCC auxiliary gives a slightly higher efficiency than the PSBCF with LDD auxiliary. The LCC auxiliary when designed correctly can allow the converter to operate with ZVS from no-load to full load condition. The soft switching assistance can also be extended to the AP leg by connecting another small inductor from the midpoint of the AP leg to the existing auxiliary if the converter is expected to operate at very low loads for extended periods. The LDD auxiliary does not provide ZVS down to no-load condition and suffers from the fact that its operation depends on the reverse recovery characteristics of the diodes used, which reduces the effective duty of the converter. However, its short-circuit performance is much better than that of the PSBCF with LCC auxiliary due to the increased impedance offered by the location of the auxiliary inductance. Thus, this circuit is particularly suitable for applications which are expected to experience output short-circuits regularly.

Chapter 8

Conclusions and Future Work

In Chapter 1, switched mode power supplies, used in most modern electronic equipment, is estimated by market researchers to be worth an estimated US\$10.1 billion in 2002 and expected to increase by half by 2009. While AC–DC converters out-sell DC–DC converters, the latter is increasing its market share due to the increasing trend of using distributed modular converters and point of load converters. High voltage SMPS play an important role in society, both directly and indirectly. They are required by important commercial semiconductor, scientific research, medical, aerospace and defence applications. Radar is a very significant application and the TWT radar in particular requires a high voltage power supply to operate.

The objectives and scope of the project were also stated in Chapter 1 along with how this project contributes to knowledge. The hypothesis put forward is: The phase shifted bridge converter with capacitive filter is a suitable converter for high voltage applications and is a suitable replacement for the current fed bridge converter presently used in airborne TWT radar applications.

8.1 Conclusion

The project has shown that the phase shifted bridge converter with capacitive filter is a suitable converter for high voltage applications and performs better than the current fed bridge converter presently used in airborne TWT radar applications. The test results presented in Chapter 6 taken from the experimental prototype converter demonstrate that the PSBCF converter (with the use of auxiliary circuits) is able to perform at a higher switching frequency (250 kHz) than the CFB converter (80 kHz) while increasing overall efficiency from 80% to around 90%. Test results also show that the PSBCF converter is inherently short-circuit proof while the CFB converter was not and depended on a large input choke to slow the rate of rise of short-circuit

current. In addition, with the removal of the active component, TPWM, from the converter the number of control integrated circuit chips can be reduced by one which reduces the converter's complexity and improves reliability. All of these properties make the PSBCF a good choice for replacing the CFB converter as the power supply for use in in airborne TWT radar applications.

The project developed the phase shifted bridge converter for use in a high voltage application. This was previously not possible due to the high transformer leakage inductance present which causes a duty loss which reduces the converters output voltage and power capability at high frequency. In addition, the PSBCF eliminates the need for the expensive high voltage output filter inductor of the conventional PSB and the input DC choke of the CFB, which keeps the overall weight of the converter low. This is replaced by two smaller inductors, L_{add} and L_{aux} , which provides zero voltage switching to the bridge MOSFETs.

The PSBCF converter avoids the problem with variable frequency faced by resonant converters and thus allows the converter to be paralleled up to provide as much output power as required by the application. In addition, this allows the converter to be synchronised to the radar to eliminate the effects of the noise at the switching frequency from affecting the radar. Operating with a fixed frequency or limited range of frequency when synchronised to the radar allows the transformer to be more easily designed then when operating with a wide operating frequency using a resonant converter.

By operating the PSBCF in DCM, it avoids returning current to the input each half switching cycle, which may cause increased voltage ripple on the input bulk capacitors. Although this means that the peak component currents are higher, but as the overall MOSFET switching loss savings is much more than the increase in conduction loss, MOSFETs run cooler than the those of the CFB and allows for an increased in switching frequency. While operating in DCM generally results in a higher output voltage ripple and requires a larger output filter capacitor, the output capacitors of the TWT radar are over-rated anyway to sustain the peak output pulses of the TWT and is adequate in filtering the increased output ripple.

However, this are limitations to the PSBCF converter. Tests show that the basic PSBCF converter is unable to function reliably at the full range of output loads due to the parasitic transformer capacitance causing the loss of soft switching on the PA leg. This problem is easily overcome by the use of auxiliary circuits (LDD and LCC) adapted from those used in the conventional phase shifted bridge converters. Both auxiliary circuits assist MOSFETs on the PA leg to achieve ZVS improving overall efficiency. Using the LDD auxiliary circuit in the converter results in lower peak currents during output short-circuits. The use of the LCC auxiliary gives the converter a higher efficiency than the LDD auxiliary and can be designed to provide

ZVS from no-load to full output load condition. The LCC auxiliary can also be extended to provide ZVS to the AP leg when operating at low output loads for an extended period of time by simply adding another inductor. The LCC auxiliary also offers better integration into the converter as the capacitors can be also used as bulk input capacitors.

Another limitation of the PSBCF is that there is no inherent protection against cross-conduction, when both MOSFETs on a leg conduct current simultaneously, causing an input short-circuit. Precautions are taken while designing the PSBCF to prevent cross-conduction, with timing delays between the drive waveforms of MOSFETs on the same leg together with the use of bipolar gate pulse transformers for the MOSFETs. However, if a MOSFET were to fail, short-circuiting all its terminals, it would result in a cross-conduction condition when the other MOSFET on the same leg is switched on.

As the converter possesses inherent short-circuit protection, a power limiting characteristic exists. Therefore, a design method was developed for the PSBCF converter, in particular the sizing of the L_{pri} and transformer design, to achieve maximum output power while limiting output short-circuit currents. As a result of the power limiting feature, the converter operates in discontinuous current conduction mode and requires a relatively narrow range of high input voltage in order obtain high output powers. Although the converter has the ability for synchronise operation, the range of frequencies is limited by the short-circuit peak current when operating at the lowest switching frequency.

The simulation of the PSBCF has also been improved with the new averaged model of the PSBCF developed from the switched inductor averaging model. The speed of simulation is increased many fold in comparison to the full switched model of the PSBCF allowing for simulations of longer durations to be carried out to study the effects of components with long time constants (*e.g.* large output capacitors). The averaged model also allows for small signal analysis of the converter which is not possible with the full switched model.

8.2 Future Work

To further improve on the PSBCF, the next step of the work would be to close the feedback loop to study how the converter starts up and evaluate the response of the feedback loop. This will allow the averaged PSPICE model of the converter to be verified in the frequency domain in addition to the time domain.

The averaged model of the PSBCF can be improved to take into account the non-idealities of the converter such as conduction losses, resonance of the transformer

parasitic capacitance when it discharges before the next active period and the effects of the auxiliary circuits.

The zero voltage sensing circuit should be investigated further with the building of a prototype to test if the circuit offers significant improvements over the simple resistive programming of the transition timing delay over various output loads.

The PSBCF's performance should also be compared to other fixed frequency resonant converters to see if the PSBCF is the best choice of converter for use in a TWT radar application.

References

- [1] V. Sapru. World Switch-mode Power Supplies Market Part II (Market Forecast). Technical report, Frost & Sullivan, April 2003.
- [2] Darnell Group. DC/DC Converters: Global Market Forecasts, Low-Voltage Powering Trends and Competitive Environment. <http://www.darnell.com/services/01-dcmkt.stm>, 2003.
- [3] C. Bunlaksananusorn. *Investigation of Voltage Injection Control for Power Supplies for in Radar Applications*. Ph.d. thesis, University of Edinburgh, 1998.
- [4] A. Narbal, I. Takahashi, and H. Akagi. A Neutral-Clamped PWM Inverter. In *IAS '80. Industry Applications Society Annual Meeting. Industry Applications Conference Proceedings*, volume 2, pages 761–6. IEEE, 1980.
- [5] J. R. Pinheiro and I. Barbi. The three-level ZVS PWM converter-a new concept in high voltage DC-to-DC conversion. In *Industrial Electronics, Control, Instrumentation, and Automation, 1992. 'Power Electronics and Motion Control', Conference Proceedings*, volume 1, pages 173–178. IEEE, IEEE, 1992.
- [6] M. M. Jovanovic. Merits and Limitations of Resonant and Soft-Switched Converters. In *INTELEC '92. 14th International Telecommunications Energy Conference. Conference Proceedings*, pages 51–8. IEEE, October 1992.
- [7] R. Miftakhutdinov. An Analytical Comparison of Alternative Control Techniques for Powering Next-Generation Microprocessors. *2001 UNITRODE DESIGN SEMINARS - SEM1400*, pages 1/1–1/39, 2001.
- [8] L. H. Jr. Dixon. Switching Power Supply Topology Review. *1993 UNITRODE DESIGN SEMINARS, SEM900*, pages P1/1–12, 1993.
- [9] R. L. Steigerwald. Power Electronic Converter Technology. *Proceedings of the IEEE*, 89(6):890–7, June 2001.
- [10] M. M. Jovanovic. Resonant, Quasi-Resonant, Multi-Resonant and Soft-Switching Techniques—Merits and limitations. *International Journal of Electronics*, 77(5):537–54, 1994.
- [11] R. L. Steigerwald. A Comparison of Half-Bridge Resonant Converter Topologies. *Power Electronics, IEEE Transactions on*, 3(2):174–82, April 1988.
- [12] R. J. King and T. A. Stuart. Inherent Overload Protection for the Series Resonant Converter. *IEEE Transactions on Aerospace & Electronic Systems*, 19(6):820–30, 1983.

- [13] S. D. Johnson, A. F. Witulski, and R. W. Erickson. Comparison of Resonant Topologies in High-Voltage DC Applications. *IEEE Transactions on Aerospace & Electronic Systems*, 24(3):263–74, 1988.
- [14] R. L. Steigerwald. Analysis of a Resonant Transistor DC-DC Converter with Capacitive Output Filter. *IEEE Transactions on Industrial Electronics*, IE-32(4):439–44, 1985.
- [15] H. Hino, T. Hatakeyama, T. Kawase, and M. Nakaoka. High-Frequency Parallel Resonant Converter for X-ray Generator Utilizing Parasitic Circuit Constants of High-Voltage Transformer and Cables. In *INTELEC '89. 11th International Telecommunications Energy Conference. Conference Proceedings*, volume 2, pages 20.5/1–20.5/8. IEEE, IEEE, October 1989.
- [16] M. Nakaoka, S. Nagai, Y. J. Kim, Y. Ogino, and Y. Murakami. The State-of-the-Art Phase-Shifted ZVS-PWM Series and Parallel Resonant DC-DC Power Converters Using Internal Parasitic Circuit Components and New Digital Control. In *PESC '92. 23rd Annual IEEE Power Electronics Specialists Conference. Conference Proceedings*, volume 1, pages 62–70, Toledo, Spain, June 1992. IEEE, IEEE.
- [17] V. Garcia, M. Rico, J. Sebastian, and M. M. Hernando. Using the Hybrid Series-Parallel Resonant Converter with Capacitive Output Filter and with PWM Phase-Shifted Control for High-Voltage Applications. In *IECON '94. 20th International Conference on Industrial Electronics, Control and Instrumentation. Conference Proceedings*, volume 3, pages 1659–64. IEEE, September 1994.
- [18] V. Garcia, M. Rico, J. Sebastian, M. M. Hernando, and J. Uceda. Study of an Optimized Resonant Converter for High-Voltage Applications. In *CIEP '94. 3rd International Power Electronics Congress. Technical Proceedings.*, pages 114–21. IEEE, August 1994.
- [19] V. Garcia, M. Rico, J. Sebastian, M. M. Hernando, and J. Uceda. An Optimized DC-to-DC Converter Topology for High-Voltage Pulse-Load Applications. In *PESC '94. 25th Annual IEEE Power Electronics Specialists Conference. Conference Proceedings*, volume 2, pages 1413–21, Taipei, Taiwan, June 1994. IEEE.
- [20] Y. J. Kim, M. Nakaoka, H. Takano, and T. Hatakeyama. Comparative Performance Evaluations of High-Voltage Transformer Parasitic Parameter Resonant Inverter-Linked High-Power DC-DC Converter with Phase-Shifted PWM Scheme. In *PESC '95. 26th Annual IEEE Power Electronics Specialists Conference. Conference Proceedings*, volume 1, pages 120–7, Atlanta, USA, June 1995. IEEE.
- [21] Muhammad H. Rashid. *Power Electronics: Circuits, Devices and Applications*. Prentice-Hall, second edition, 1993.
- [22] Ruan Xinbo and Yangguang Yan. Soft-Switching Techniques for PWM Full Bridge Converters. In *PESC 2000. 31st Annual IEEE Power Electronics Specialists Conference. Conference Proceedings*, volume 2, pages 634–9, Galway, Ireland, June 2000. IEEE, IEEE.
- [23] R. L. Steigerwald, R. W. De Doncker, and M. H. Kheraluwala. A Comparison of High Power DC-to-DC Soft-Switched Converter Topologies. In *IAS '94. 29th*

- IAS Annual Meeting of the Industry Applications Society. Conference Proceedings*, volume 2, pages 1090–6. IEEE, October 1994.
- [24] R. L. Steigerwald. A Review of Soft-Switching Techniques in High Performance DC Power Supplies. In *IECON '95. 21st International Conference on Industrial Electronics, Control, and Instrumentation. Conference Proceedings*, volume 1, pages 1–7. IEEE, November 1995.
- [25] J. A. Sabate, V. Vlatkovic, R. B. Ridley, F. C. Lee, and B. H. Cho. Design Considerations for High-Voltage High-Power Full-Bridge Zero-Voltage-Switched PWM Converter. In *5th Annual Applied Power Electronics Conference and Exposition, APEC '90 Conference Proceedings*, pages 275–284, Los Angeles, California, March 1990. IEEE.
- [26] N. Mohan, T. M. Undeland, and W. P. Robbins. *Power Electronics: Converters, Applications and Design*. John Wiley & Sons, Inc., second edition, 1995.
- [27] J. G. Cho, J. A. Sabate, Hua Guichao, and F. C. Lee. Zero-Voltage and Zero-Current-Switching Full Bridge PWM Converter for High Power Applications. In *PESC '94. 25th Annual IEEE Power Electronics Specialists Conference. Conference Proceedings*, volume 1, pages 102–8, Taipei, Taiwan, June 1994. IEEE.
- [28] G. Hua, F. C. Lee, and M. M. Jovanovic. An Improved Full-Bridge Zero-Voltage-Switched PWM Converter Using a Saturable Inductor. *IEEE Transactions on Power Electronics*, 8(4):530–4, 1993.
- [29] J. G. Cho, G. H. Rim, and F. C. Lee. Zero Voltage and Zero Current Switching Full Bridge PWM Converter Using Secondary Active Clamp. In *PESC '96. 27th Annual IEEE Power Electronics Specialists Conference. Conference Proceedings*, volume 1, pages 657–63, Baveno, Italy, June 1996. IEEE.
- [30] C. Cuadros, C. Y. Lin, D. Boyevich, R. Watson, G. Skutt, F. C. Lee, and P. Ribardiere. Design Procedure and Modeling of High Power, High Performance, Zero-Voltage Zero-Current Switched, Full-Bridge PWM Converter. In *APEC '97. 12th Annual Applied Power Electronics Conference and Exposition. Conference Proceedings*, volume 2, pages 790–8, Atlanta, Georgia, February 1997. IEEE.
- [31] M. M. Walters and W. M. Polivka. Extending the Range of Soft-Switching in Resonant-Transition DC-DC Converters. In *INTELEC '92. 14th International Telecommunications Energy Conference. Conference Proceedings*, pages 343–50. IEEE, October 1992.
- [32] R. Redl, N. O. Sokal, and L. Balogh. A Novel Soft-Switching Full-Bridge DC/DC Converter: Analysis, Design Considerations, and Experimental Results at 1.5 kW, 100 kHz. *IEEE Transactions on Power Electronics*, 6(3):408–18, 1991.
- [33] R. Redl, L. Balogh, and D. W. Edwards. Optimum ZVS Full-Bridge DC/DC Converter with PWM Phase-Shift Control: Analysis, Design Considerations, and Experimental Results. In *9th Annual Applied Power Electronics Conference and Exposition, APEC '94 Conference Proceedings*, volume 1, pages 159–65, Orlando, Florida, February 1994. IEEE.

- [34] V. Vlatkovic, M. J. Schutten, and R. L. Steigerwald. Auxiliary Series Resonant Converter: A New Converter for High-Voltage, High-Power Applications. In *APEC '96. 11th Annual Applied Power Electronics Conference and Exposition. Conference Proceedings*, volume 1, pages 493–9, San Jose, California, March 1996. IEEE.
- [35] J. G. Cho, J. A. Sabate, G. H. Hua, and F. C. Lee. Zero-Voltage and Zero-Current-Switching Full Bridge PWM Converter for High-Power Applications. *IEEE Transactions on Power Electronics*, 11(4):622–8, 1996.
- [36] Ruan Xinbo and Yan Yangguang. An Improved Phase-Shifted Zero-Voltage and Zero-Current Switching PWM Converter. In *APEC '98. 13th Annual Applied Power Electronics Conference and Exposition. Conference Proceedings*, volume 2, pages 811–15, Anaheim, California, February 1998. IEEE, IEEE.
- [37] Kim Eun-Soo, Joe Kee-Yeon, Kye Moon-Ho, Kim Yoon-Ho, and Yoon Byung-Do. An Improved Soft-Switching PWM FB DC/DC Converter for Reducing Conduction Losses. *IEEE Transactions on Power Electronics*, 14(2):258–64, March 1999.
- [38] J. G. Cho, J. W. Baek, D. W. Yoo, H. S. Lee, and G. H. Rim. Novel Zero-Voltage and Zero-Current-Switching (ZVZCS) Full Bridge PWM Converter Using Transformer Auxiliary Winding. In *PESC '97. 28th Annual IEEE Power Electronics Specialists Conference. Conference Proceedings*, volume 1, pages 227–32, St. Louis, Missouri, USA, June 1997. IEEE.
- [39] J. G. Cho, J. W. Baek, C. Y. Jeong, D. W. Yoo, H. S. Lee, and G. H. Rim. Novel Zero-Voltage and Zero-Current-Switching (ZVZCS) Full Bridge PWM Converter Using a Simple Auxiliary Circuit. In *APEC '98. 13th Annual Applied Power Electronics Conference and Exposition. Conference Proceedings*, volume 2, pages 834–839, Anaheim, California, February 1998. IEEE, IEEE.
- [40] J. G. Cho, J. W. Baek, C. Y. Jeong, D. W. Yoo, and K. Y. Joe. Novel Zero-Voltage and Zero-Current-Switching Full Bridge PWM Converter Using Transformer Auxiliary Winding. *IEEE Transactions on Power Electronics*, 15(2):250–257, March 2000.
- [41] S. Valtchev, B. V. Borges, and V. Anunciada. 1 kW/250 kHz Full Bridge Zero Voltage Switched Phase Shift DC-DC Converter with Improved Efficiency. In *INTELEC '95. 17th International Telecommunications Energy Conference. Conference Proceedings*, pages 803–7. IEEE, October 1995.
- [42] A. Cook. *Elements of Electrical Engineering*, pages 476–478. John Wiley and Sons, 1924.
- [43] L.-Balogh. Design and Application Guide for High Speed MOSFET Gate Drive Circuits. *2001 UNITRODE DESIGN SEMINARS*, pages 2/1– 2/39, 2001.
- [44] W. A. Peterson, R. Kolbet, and R. Saint-Pierre. A Clamped Transformer Power Supply Producing Zero Voltage Resonant Transitions Over the Full-Load Range. In *APEC '94. 9th Annual Applied Power Electronics Conference and Exposition. Conference Proceedings*, volume 1, pages 287–83, Orlando, Florida, February 1994. IEEE.

- [45] L. Balogh. Design Review: 100W, 400kHz, DC/DC Converter with Current Doubler Synchronous Rectification Achieves 92%. *1996 UNITRODE DESIGN SEMINARS - SEM1100*, pages 2/1–2/25, 1996.
- [46] M. Michihira, T. Funaki, K. Matsu-ura, and M. Nakaoka. A Novel Quasi-Resonant DC-DC Converter Using Phase-Shift Modulation in Secondary Side of High-Frequency Transformer. In *PESC '96. 27th Annual IEEE Power Electronics Specialists Conference. Conference Proceedings*, volume 1, pages 670–5, Baveno, Italy, June 1996. IEEE.
- [47] J. P. Beirante and B. V. Borges. Full Bridge Zero Voltage Switched Phase Shifted DC-DC Converter with Enlarged Duty Cycle and ZVS Range. In *EPE-PEMC 2000. 9th Power Electronics and Motion Control Conference. Conference Proceedings*, volume 2, pages 1–6, 2000.
- [48] D. Abud, F. Canales, and J. Arau. Design of a Two Stage, 1 kW AC/DC Power Factor Pre-Regulator, Using the FB-ZVS-PWM Topology. In *CIEP '93. 2nd International Power Electronics Congress. Technical Proceedings.*, pages 129–134, August 1993.
- [49] R. Watson and F. C. Lee. A Soft-Switched, Full-Bridge Boost Converter Employing an Active-Clamp Circuit. In *PESC '96. 27th Annual IEEE Power Electronics Specialists Conference. Conference Proceedings*, volume 2, pages 1948–54, Baveno, Italy, June 1996. IEEE.
- [50] V. Yakushev, V. Meleshin, and S. Fraidlin. Full-Bridge Isolated Current Fed Converter with Active Clamp. In *APEC '99. 14th Annual Applied Power Electronics Conference and Exposition. Conference Proceedings*, volume 1, pages 560–6, Dallas, Texas, March 1999. IEEE.
- [51] C. Iannello, Luo Shiguo, and I. Batarseh. A Full Bridge ZCS PWM Converter for High Voltage and High Power Applications. In *PESC 2000. 31st Annual IEEE Power Electronics Specialists Conference. Conference Proceedings*, volume 2, pages 1064–71, Galway, Ireland, June 2000. IEEE.
- [52] M. Marx and D. Schroder. A Novel Zero-Current-Transition Full-Bridge DC-DC Converter. In *PESC '96. 27th Annual IEEE Power Electronics Specialists Conference. Conference Proceedings*, volume 1, pages 664–9, Baveno, Italy, June 1996. IEEE.
- [53] M. D. Bellar, E. H. Watanabe, and A. C. Mesquita. Analysis of the Dynamic and Steady-State Performance of Cockcroft-Walton Cascade Rectifiers. *IEEE Transactions on Power Electronics*, 7(3):526–534, July 1992.
- [54] I. A. Krichtafovitch and I. Z. Sinitsyna. Multi-Output Modular High-Voltage Power Supplies for Airborne and Space Applications. In *IECEC '96. 31st International Energy Conversion Engineering Conference. Conference Proceedings*, volume 1, pages 577–81. IEEE, August 1996.
- [55] Ministry of Defence. *R.A.F Standard Technical Training Notes (STTN) AP3302 Part 3*, 2nd edition edition, 1971. <http://www.radarpages.co.uk/theory/ap3302/sec1/ch3/sec1ch341.htm>.
- [56] A. S. Jr Gilmour. *Principles of Traveling Wave Tubes*. Artech House, Inc, 1994.

- [57] Marconi Applied Technologies. Three-Electrode Spark Gap Preamble, July 2000.
- [58] A. I. Pressman. *Switching Power Supply Design*, pages 175–87. McGraw-Hill, second edition, 1998.
- [59] I. D. Jitaru. A 3 kW Soft Switching DC-DC Converter. In *APEC 2000. 15th Annual IEEE Applied Power Electronics Conference and Exposition. Conference Proceedings*, volume 1, pages 86–92, New Orleans, Louisiana, February 2000. IEEE.
- [60] A. Pietkiewicz and D. Tollik. Operation of From Power Soft-Switched Phase-Shifted Full-Bridge DC-DC Converter Under Extreme Conditions. In *INTELEC '94. 16th International Telecommunications Energy Conference. Conference Proceedings*, pages 142–7. IEEE, October 1994.
- [61] L. Saro, K. Dierberger, and R. Redl. High-Voltage MOSFET Behavior in Soft-Switching Converters: Analysis and Reliability Improvements. In *INTELEC '98. 20th International Telecommunications Energy Conference. Conference Proceedings*, pages 30–40. IEEE, October 1998.
- [62] A. Fiel and T. Wu. MOSFET Failure Modes in the Zero-Voltage-Switched Full-Bridge Switching Mode Power Supply Applications. In *APEC 2001. 16th Annual IEEE Applied Power Electronics Conference and Exposition. Conference Proceedings*, volume 2, pages 1247–1252, Anaheim, California, March 2001. IEEE, IEEE.
- [63] A. Guerra, K. Andoh, and S. Fimiani. Ultra-Fast Recovery Diodes Meet Today's Requirements for High Frequency Operation and Power Ratings in SMPS Applications. Application note, International Rectifier, 2000.
- [64] International Rectifier. A More Realistic Characterization Of Power MOSFET Output Capacitance C_{oss} . Application Note AN-1001, International Rectifier, 1999.
- [65] Unitrode Corporation. Phase Shift Resonant Controller (UC2879, UC3879). Datasheet, Unitrode Corporation, September 1999.
- [66] L. Balogh. The New UC3879 Phase-Shifted PWM Controller Simplifies the Design of Zero Voltage Transition Full-Bridge Converters. Application Note U154, Unitrode Corporation, September 1999.
- [67] S. M. Sandler. *SMPS Simulation with SPICE3*. McGraw-Hill Education, 1997.
- [68] R. Middlebrook and S. Cuk. A General Unified Approach to Modeling Switching-Converter Power Stages. In *PESC '76. 7th Annual IEEE Power Electronics Specialists Conference. Conference Proceedings*, pages 18–34. IEEE, IEEE, 1976.
- [69] V. Vorperian. Simplified Analysis of PWM Converters Using Model of PWM Switch. II. Discontinuous Conduction Mode. *IEEE Transactions on Aerospace & Electronic Systems*, 26(3):497–505, 1990.
- [70] V. Vorperian. Simplified Analysis of PWM Converters Using Model of PWM Switch. Continuous Conduction Mode. *IEEE Transactions on Aerospace & Electronic Systems*, 26(3):490–6, 1990.

- [71] S. Ben-Yaakov and V. Vorperian. Modeling the Switch of PWM Convertors (Comments, with Reply, on 'Simplified Analysis of PWM Converters Using Models of PWM Switch' by V. Vorperian). *IEEE Transactions on Aerospace & Electronic Systems*, 28(3):921–925, July 1992.
- [72] S. Ben-Yaakov. SPICE Simulation of PWM DC-DC Converter Systems: Voltage Feedback, Continuous Inductor Conduction Mode. *Electronics Letters*, 25(16):1061–1063, August 1989.
- [73] C. P. Basso. *Switch-Mode Power Supply SPICE Cookbook*. McGraw-Hill Education, 2001.
- [74] S. Ben-Yaakov. Average Simulation of PWM Converters by Direct Implementation of Behavioral Relationships. In *APEC '93. 8th Annual Applied Power Electronics Conference and Exposition. Conference Proceedings*, pages 510–516, San Diego, California, March 1993. IEEE, IEEE.
- [75] C. P. Basso. Spark Gap Modeling. In C.E. Hymowitz and B. Halal, editors, *Power Specialist's App Note Book*, pages 103–7. Intusoft, 1998.
- [76] R. McArthur and H. Hess. Optimizing MOSFET and IGBT Gate Current to Minimize dv/dt Induced Failures in SMPS Circuits. Application Note APT0102 Rev – October 29, 2001, Advanced Power Technology, 2001.
- [77] P. T. Krein. Tricks of the Trade: The Automatic Resonant Switch. *IEEE Power Electronics Society Newsletter*, 13(3):5, July 2001.
- [78] C. R. Sullivan. Computationally Efficient Winding Loss Calculation with Multiple Windings, Arbitrary Waveforms, and Two-Dimensional or Three-Dimensional Field Geometry. *Power Electronics, IEEE Transactions on*, 16(1):142–50, January 2001.
- [79] W. G. Hurley, E. Gath, and J. G. Breslin. Optimizing the AC Resistance of Multilayer Transformer Windings with Arbitrary Current Waveforms. *Power Electronics, IEEE Transactions on*, 15(2):369–76, March 2000.
- [80] D. J. Hamo. A 50W, 500kHz, Full-Bridge, Phase-Shift, ZVS Isolated DC to DC Converter Using the HIP4081A. Application Note 9506, Intersil Corporation, 1995.

Appendix A

Additional Results

The following are additional results for the waveform capture and simulation results PSBCF converter with LDD and LCC auxiliary circuits on half load.

A.1 LDD Auxiliary Circuit

The various waveforms captures for the PSBCF with LDD auxiliary circuit on half load are as shown in Figures A.1, A.3, A.5 and A.7, along with their corresponding PSPICE simulation waveforms in Figures A.2, A.4, A.6 and A.8.

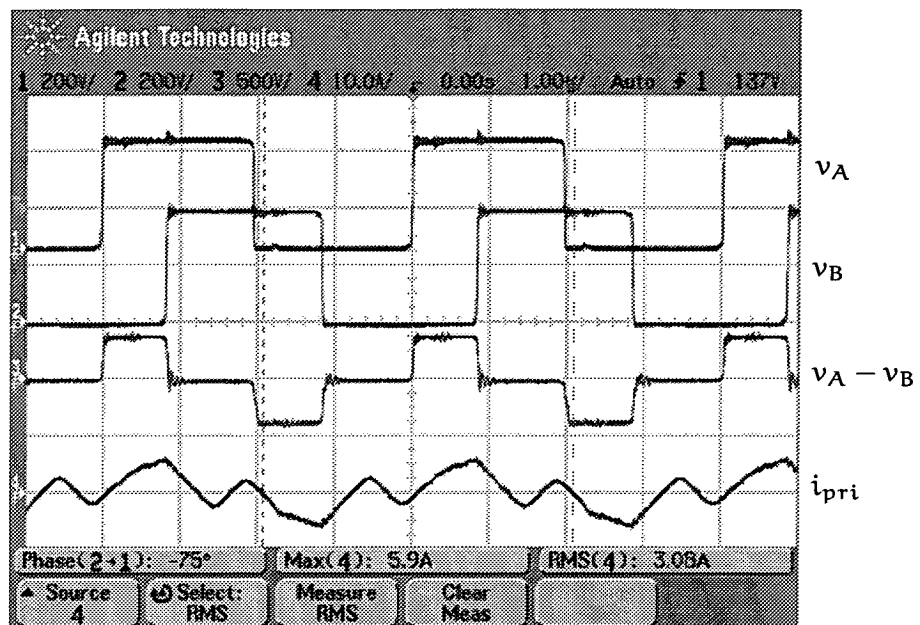


Figure A.1: Prototype PSBCF with LDD Auxiliary Circuit Transformer Waveforms (Half Load)

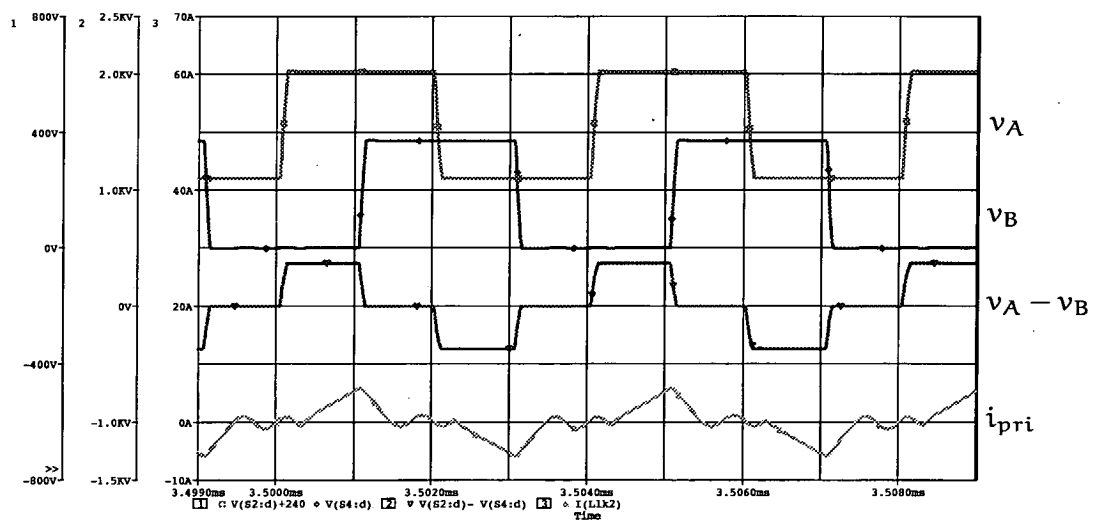


Figure A.2: PSPICE PSBCF with LDD Auxiliary Circuit Transformer Waveforms (Half Load)

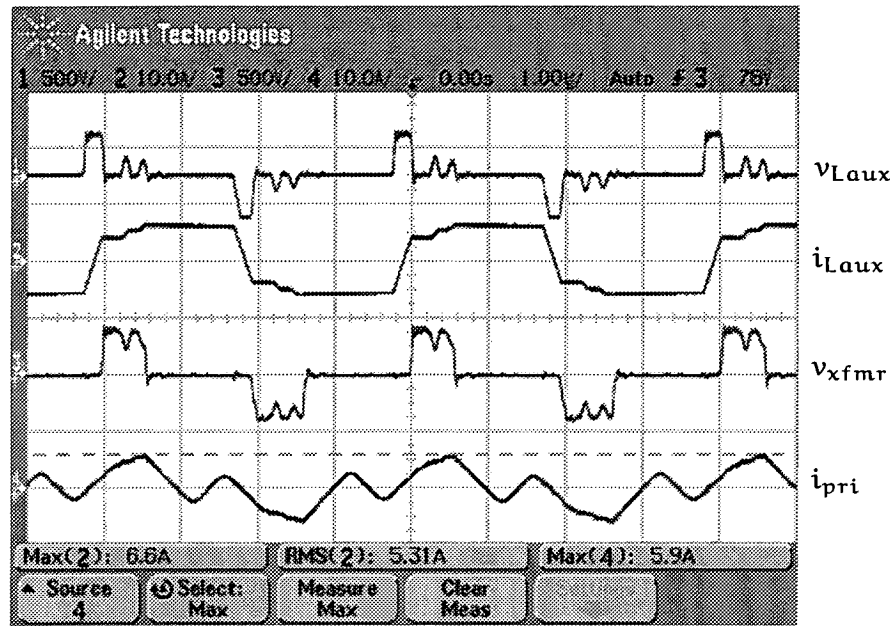


Figure A.3: Prototype LDD Auxiliary Inductor Waveforms (Half Load)

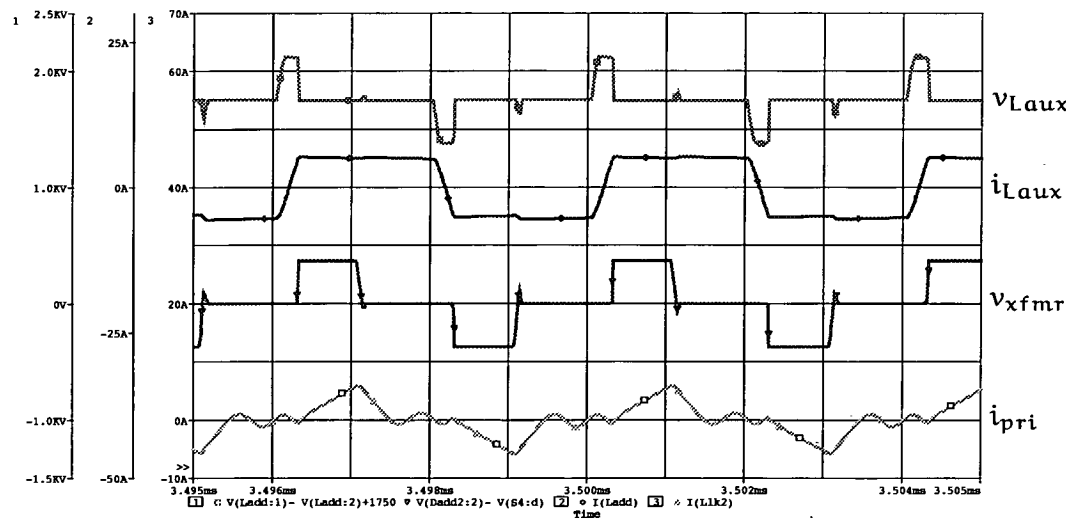


Figure A.4: PSPICE LDD Auxiliary Inductor Waveforms (Half Load)

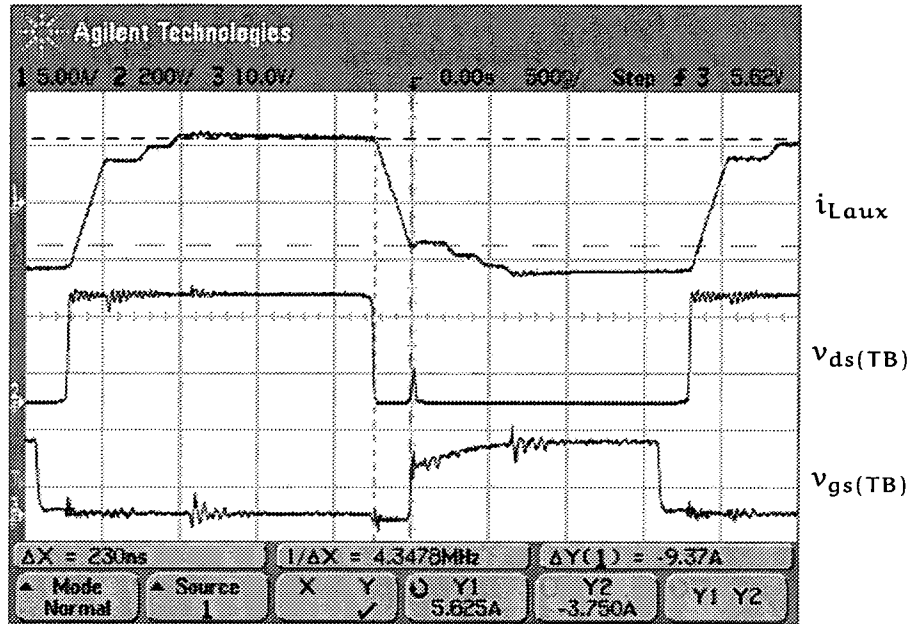


Figure A.5: Prototype PSBCF with LDD Auxiliary Circuit MOSFET TB Waveforms (Half Load)

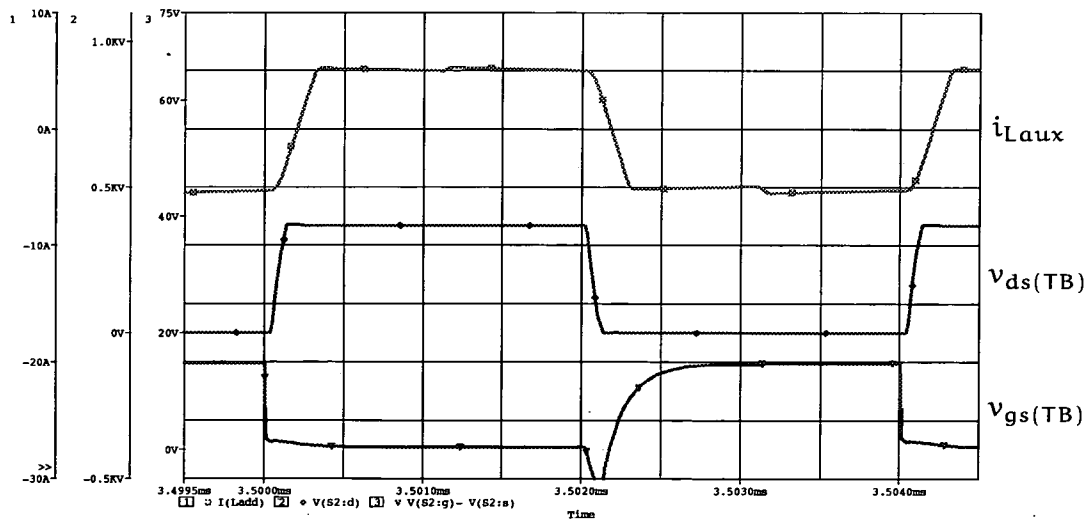


Figure A.6: PSPICE PSBCF with LDD Auxiliary Circuit MOSFET TB Waveforms (Half Load)

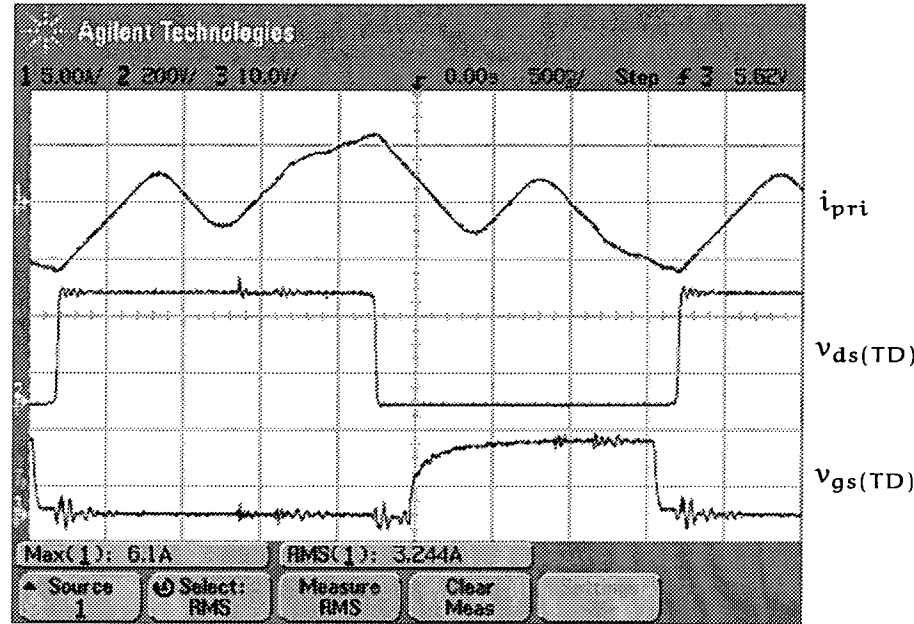


Figure A.7: Prototype PSBCF with LDD Auxiliary Circuit MOSFET TD Waveforms (Half Load)

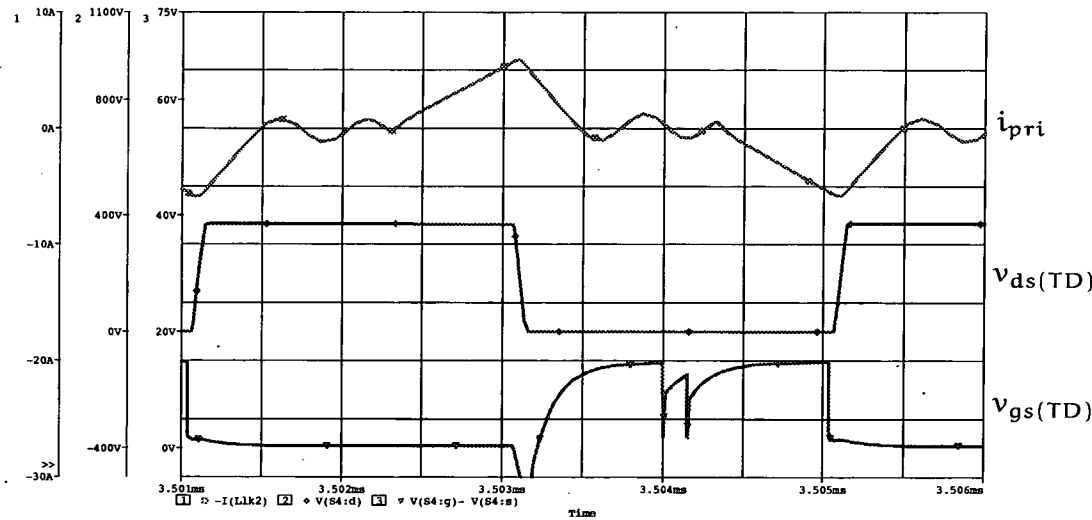


Figure A.8: PSPICE PSBCF with LDD Auxiliary Circuit MOSFET TD Waveforms (Half Load)

A.2 LCC Auxiliary Circuit

These are the waveforms for the LCC auxiliary circuit on half load. The various waveforms captured for the PSBCF with LCC auxiliary circuit on half load are as shown in Figures A.9, A.11, A.13 and A.15, along with their corresponding PSPICE simulation waveforms in Figures A.10, A.12, A.14 and A.16.

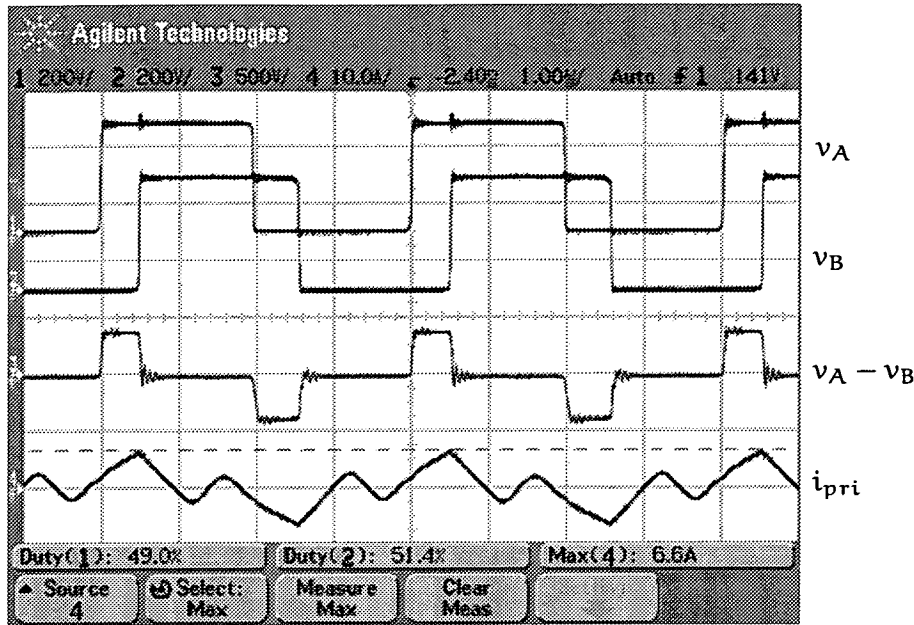


Figure A.9: Prototype PSBCF with LCC Auxiliary Circuit Transformer Waveforms (Half Load)

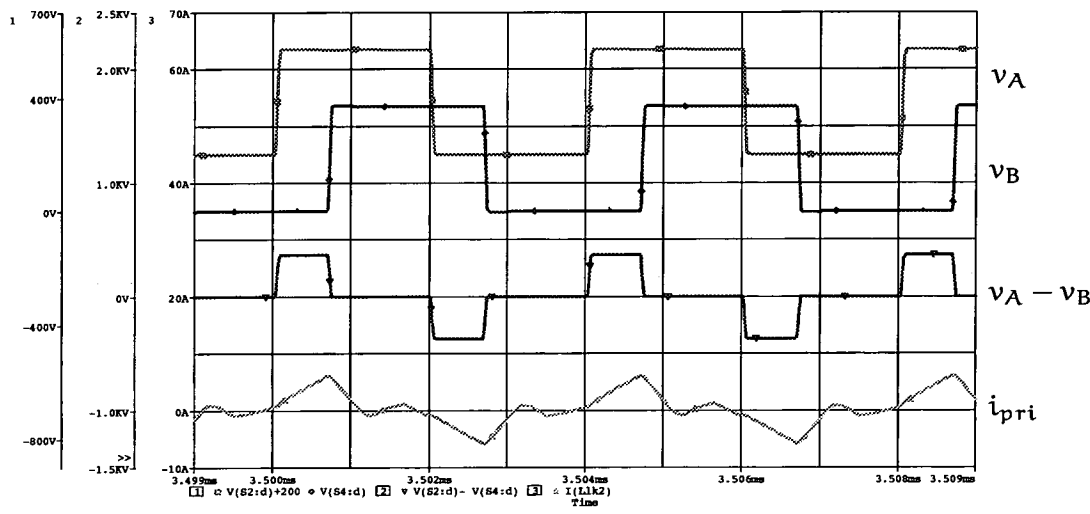


Figure A.10: PSPICE PSBCF with LCC Auxiliary Circuit Transformer Waveforms (Half Load)

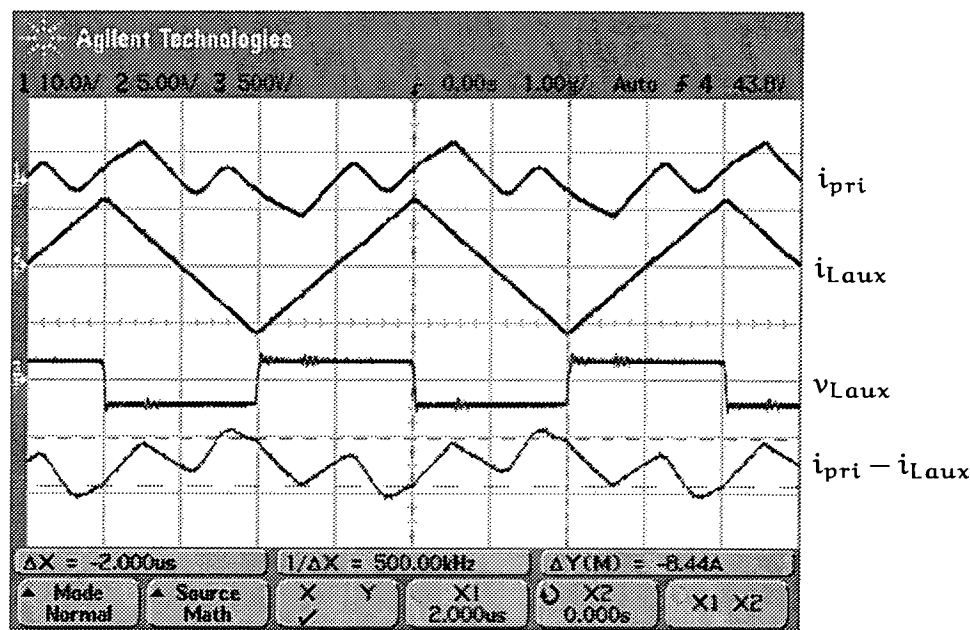


Figure A.11: Prototype LCC Auxiliary Inductor Waveforms (Half Load)

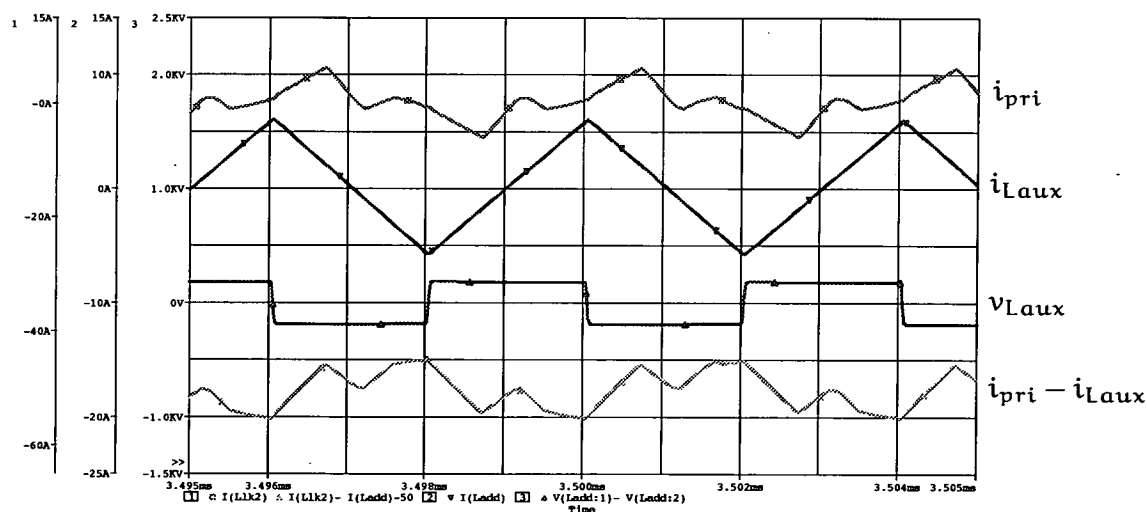


Figure A.12: PSPICE LCC Auxiliary Inductor Waveforms (Half Load)

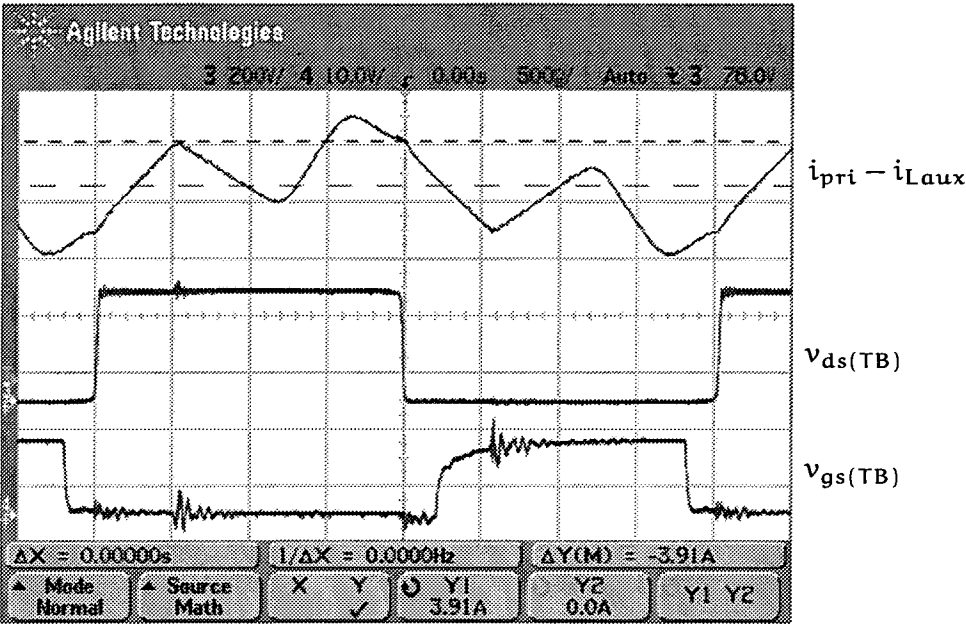


Figure A.13: Prototype PSBCF with LCC Auxiliary Circuit MOSFET TB Waveforms (Half Load)

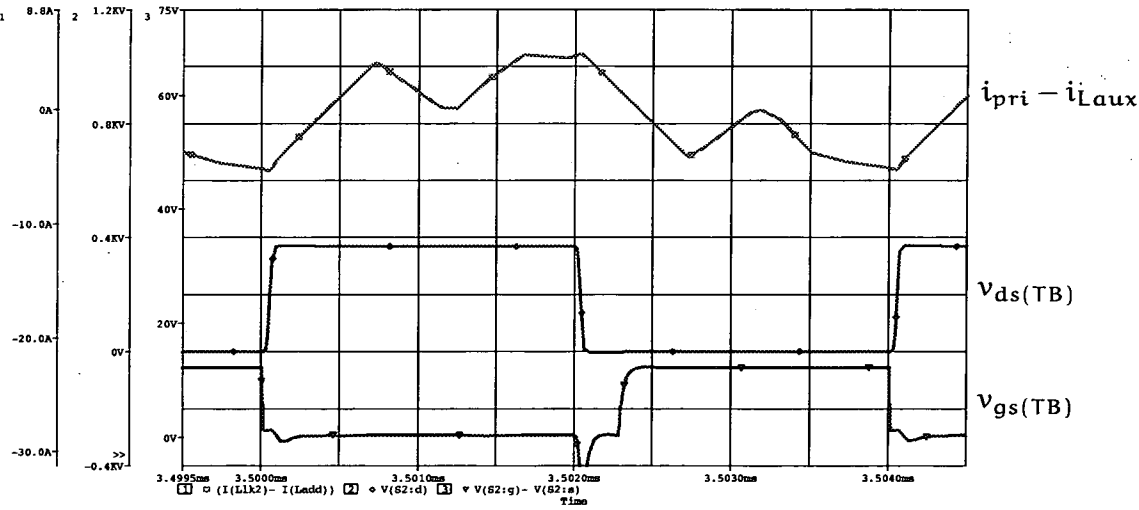


Figure A.14: PSPICE PSBCF with LCC Auxiliary Circuit MOSFET TB Waveforms (Half Load)

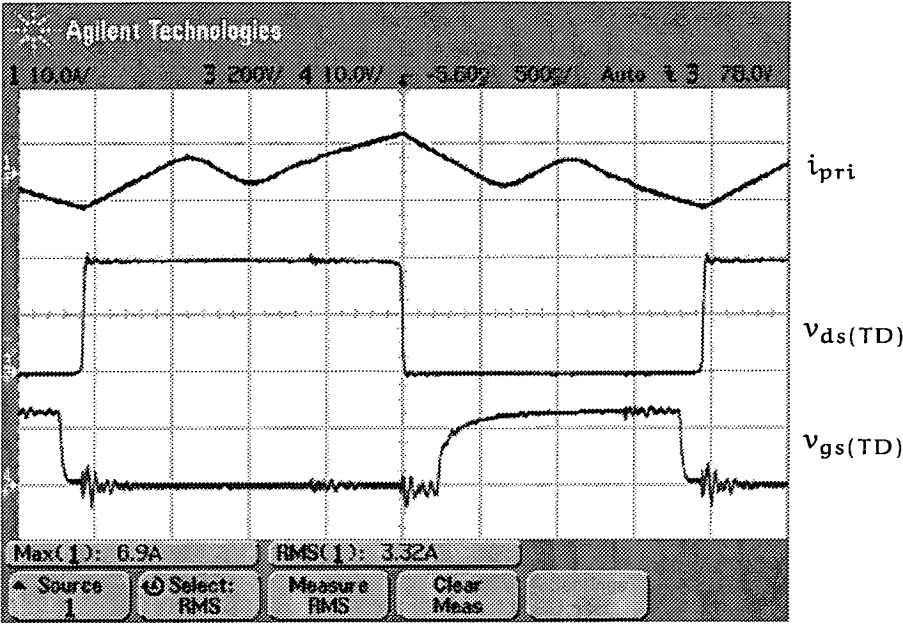


Figure A.15: Prototype PSBCF with LCC Auxiliary Circuit MOSFET TD Waveforms (Half Load)

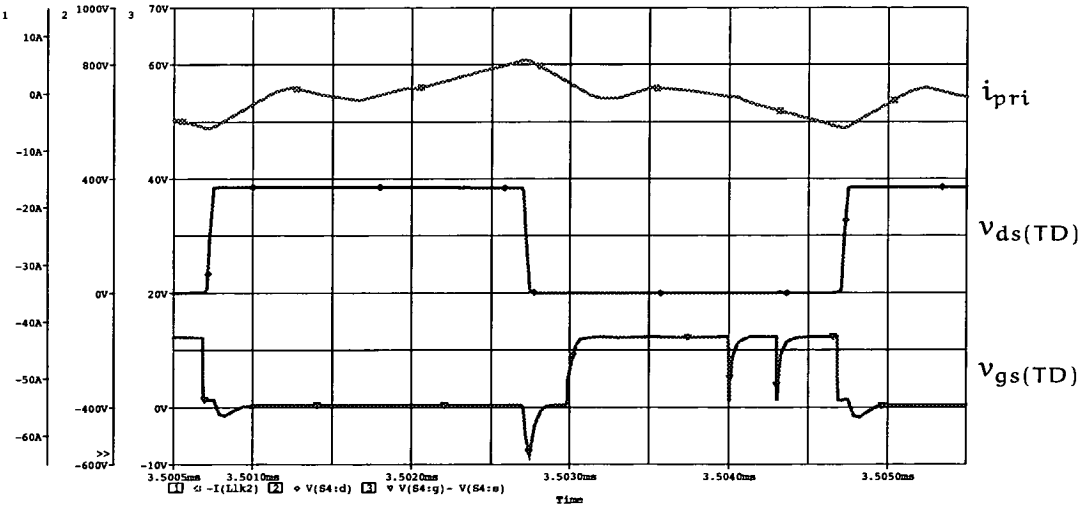


Figure A.16: PSPICE PSBCF with LCC Auxiliary Circuit MOSFET TD Waveforms (Half Load)

Appendix B

C_{oss} Value Derivation

The following is the derivation of the estimated equivalent value of C_{oss} , $C_{ossEquivalent}$, at the appropriate V_{ds} , which the phase shifted bridge MOSFETs are subjected to, from the C_{oss} values quoted in the MOSFET data sheet [80].

The output drain-source capacitance can be approximated by C_{ds} in Equation B.1, where n is a value between $\frac{1}{2}$ – $\frac{1}{3}$ for most MOSFETs.

$$C_{ds}(V_{ds}, n) = C_{oss} \left(\frac{V_{oss}}{V_{ds}} \right)^n \quad (B.1)$$

As most manufacturers measure the C_{oss} using a drain-source voltage, V_{oss} , of 25 V.

$$V_{oss} = 25V \quad (B.2)$$

From the basic definitions for energy and current (Equations B.3 to B.5)

$$E = \int (v \times i) dt \quad (B.3)$$

$$i = \frac{dQ}{dt} \quad (B.4)$$

$$E = \int v dQ \quad (B.5)$$

the energy requirements for the MOSFET output capacitances can be derived for a actual drain-source voltage of the converter, $C(V_{ds})$.

$$C(V_{ds}) = \frac{dQ}{dV_{ds}} \quad (B.6)$$

$$E(V_{ds}, n) = \int V_{ds} C_{ds}(V_{ds}, n) dV_{ds} \quad (B.7)$$

$$E(V_{ds}, n) = C_{oss} V_{oss}^n \int V_{ds}^{1-n} dV_{ds} \quad (B.8)$$

$$E(V_{ds}, n) = \frac{C_{oss} V_{oss}^n V_{ds}^{2-n}}{2-n} \quad (B.9)$$

Assuming that $n = \frac{1}{2}$ for the MOSFET (Estimated value for Harris IRFR120).

$$E = \left(\frac{2}{3} C_{oss}\right) (V_{oss}^{\frac{1}{2}}) (V_{ds}^{\frac{3}{2}}) \quad (B.10)$$

$$E = \frac{1}{2} \left(\frac{4}{3} C_{oss}\right) (V_{oss}^{\frac{1}{2}}) (V_{ds}^{\frac{3}{2}}) \quad (B.11)$$

Therefore the equivalent output capacitance value of a single MOSFET, $C_{ossEquivalent}$ can be approximated by Equation B.12.

$$C_{ossEquivalent} \approx \frac{4}{3} C_{ossDataSheet} \quad (B.12)$$

Appendix C

PSBCF Average Model PSPICE Code

The following is the PSPICE source code for the PSBCF switched inductor averaged model used.

```
.subckt AvgPSB in common out peak d params: L=17.83u, fs=250k, nsnp=4, Dmax=0.98
*****
* Note L is total inductance between legs of bridge
*   nsnp is secondary turns/primary turns ratio
*   fs is switching frequency which needs to be doubled
*   Dmax is maximum duty which is achievable by chip
*
* V(in,common) is Vin : Iin = ISecAvg*(Voutpri/Vin)
*
* V(out,common) is Vout : Iout = ISecAvg/nsnp
* NOTE! Voutpri is used instead of Vout for most calculations
* V(9,0) is Voutpri
*
* V(peak,common) is peak currents seen in converter
*
* V(d,common) is duty used to calculate Dlimit
* NOTE! Dlimit is used instead of D for most calculations
* V(8,0) is Dlimit - Limit(0,Dmax)
*
* Averages current values for SECONDARY under BC, CCM, DCM,
* separately and combined
*
* V(10,0) is the IBC Average Secondary currents during
*   boundary condition reflected back on primary.
* V(20,0) ISecAvg = (IdcmSecNomLtd*IccmSecNomLtd)*IBC
* V(30,0) IdcmSecNomLtd = (IdcmSecNom) Limit(0,1) 0->1
* V(40,0) IccmSecNomLtd = (IccmSecNom) Limit(1,1k) 1->1000
*
* Peak Current values in PRIMARY under BC, CCM and DCM,
* separate and combined
*
* V(110,0) is the IPeakBC Peak Primary currents during
*   boundary condition
* V(120,0) IPeak = (IdcmPeakNomLtd*IccmPeakNomLtd)*IPeakBC
* V(130,0) IdcmPeakNomLtd = (IdcmPeakNom) Limit(0,1) 0->1
* V(140,0) IccmPeakNomLtd = (IccmPeakNom) Limit(1,1k) 1->1000
*
*****
```

```

* Parameters and other functions which are used.
*
.param Ts={0.5/fs}
*
.func FIBC(V1,V0)
+{(0.5*Ts/L)*(V1-V0)*(V0/V1)}
*
.func FIdcmSecNom(D,V1,V0)
+{pwr((D*V1/V0),2)}
*
.func FIccmSecNom(D,V1,V0)
+{((D*(V1**2)*(2-D))-(V0**2))/(2*V0*(V1-V0))}
*
.func FIPeakBC(V1,V0)
+{(Ts/L)*(V1-V0)*(V0/V1)}
*
.func FIPeakDCMNom(D,V1,V0)
+{D*V1/V0}
*
.func FIPeakCCMNom(D,V1,V0)
+{((D*V1)+V0)/(2*V0)}
*****
* Calculates Iin and Iout
*
* Iin = ISecAvg*(Voutpri/Vin)
GIin in common value={V(20,0)*(V(9,0)/V(in,common))}
*
* Iout = ISecAvg/nsnp
GIout common out value={V(20,0)/nsnp}
*
*****
* Calculates V:Dlimit
*
* RD d common 1
GDlimit 0 8 value={limit(V(d,common),0,Dmax)}
RDlimit 8 0 1
*
*****
* Calculates Vout reflected on primary
*
GVoutpri 0 9 value={V(out,common)/nsnp}
RVoutpri 9 0 1
*
*****
* Calculates V:IBC
*
GIBC 0 10 value={FIBC(V(in,common),V(9,0))}
RIBC 10 0 1
*
*****
* Calculates V:ISecAvg
*
GISecAvg 0 20 value={V(30,0)*V(40,0)*V(10,0)}
RISecAvg 20 0 1
*
*****
* Calculates V:IdcmSecNomLtd
*
GIdcmSecNomLtd 0 30 value={limit(FIdcmSecNom(
+V(8,0),
+V(in,common),
+V(9,0)),0,1)}

```



```

RIdcmSecNomLtd 30 0 1
*
*****
* Calculates V:IccmSecNomLtd
*
GIccmSecNomLtd 0 40 value={limit(FIccmSecNom(
+V(8,0),
+V(in,common),
+V(9,0)),1,1k)}
RIccmSecNomLtd 40 0 1
*
*****
* Ipeak is the peak primary current
* IpeakBC is the Peak Primary Current at Boundary Condition
* Again this is used to provide transition between CCM and DCM
* IpeakDCM is the current rise in Lpri after D*T0.5
* IpeakCCM is the current rise in Lpri after D1*T0.5
*
* EIpeak peak common value={2/V(8,0)*V(20,0)*(V(9,0)/V(in,common))}
EIpeak peak common value={V(120,0)}
*
*****
* Calculates V:IpeakBC
*
GIpeakBC 0 110 value={FIpeakBC(V(in,common),V(9,0))}
RIpeakBC 110 0 1
*
*****
* Calculates V:Ipeak
*
GIpeak 0 120 value={V(130,0)*V(140,0)*V(110,0)}
RIpeak 120 0 1
*
*****
* Calculates V:IdcmPeakNomLtd
*
GIIdcmPeakNomLtd 0 130 value={limit(FIpeakDCMNom(
+V(8,0),
+V(in,common),
+V(9,0)),0,1)}
RIIdcmPeakNomLtd 130 0 1
*
*****
* Calculates V:IccmPeakNomLtd
*
GIccmPeakNomLtd 0 140 value={limit(FIpeakCCMNom(
+V(8,0),
+V(in,common),
+V(9,0)),1,1k)}
RIccmPeakNomLtd 140 0 1
*
*****
.ends AvgPSB

```

Appendix D

Publications

The work described in this thesis has been reported in the following publications :

- [D-1] C. K. R. M. Loh, D. E. Macpherson, and F. Fisher. Phase Shifted Full Bridge Converter for High Voltage Applications, In *Proceedings of the 36rd Universities Power Engineering Conference (UPEC '98)*, University of Wales, Swansea UK, 12-14 September 2001.
- [D-2] C. K. R. M. Loh and D. E. Macpherson. An Improved Phase Shifted Full Bridge Converter for High Voltage Applications, In *Proceedings of the Second IEE International Conference on Power Electronics, Machines and Drives (PEMD 2004)*, volume 2, pages 844–9, University of Edinburgh, Edinburgh UK, 31 March-2 April 2004.

PHASE SHIFTED FULL BRIDGE CONVERTER FOR HIGH VOLTAGE APPLICATIONS

C.K.R.M. Loh⁽¹⁾, D.E. Macpherson⁽¹⁾ and F. Fisher⁽²⁾

(1) University of Edinburgh, UK (2) BAE Systems, UK

ABSTRACT

This paper examines the use of a modified phase shifted soft switching full bridge converter in high voltage applications. A conventional current-fed bridge presently in use is described. The general operation of the phase shifted bridge and its detailed switching cycle is analysed. SPICE simulation results for both the current-fed bridge and the phase shifted bridge under normal and short circuit operation are presented. A comparison between the two converters is made and conclusions drawn from the findings.

INTRODUCTION

High Voltage (HV) Switch Mode Power Supplies (SMPS) are used regularly in everyday life. They can be found in television sets, computer monitors, X-ray machines, radar power supplies and more. As these converters are required to step the input voltage up to much higher voltages, the transformer needs to have adequate and proper insulation between its primary and secondary windings. This results in a transformer with less than ideal coupling between its windings which can be modelled as a parasitic leakage inductance. Leakage inductance has the undesired effects of causing duty loss in many converters and resonating with parasitic capacitances resulting in ringing on the voltage and current waveforms. To limit this, the secondary windings can be separated into several sections of intermediate voltages, each having their own output rectifiers charging a capacitor ladder up to the require output voltage. High voltage output inductors tend to be bulky and expensive due to the same high voltage considerations, therefore, it is preferable to use a capacitive output filter.

Typical requirements for a Travelling-Wave-Tube (TWT) RADAR system power supply onboard an aircraft are shown below.

Airborne TWT RADAR Power Supply Requirements

Input voltage: 330V rectified DC
Output voltage: 10kV, 25kV

TWTs are also prone to arcing. This appears as an output short circuit, lasting for approximately 10ms. Current-fed power supplies are used to slow current rise during arcing.

This paper describes a Current-Fed Full Bridge (CFB) topology currently used as a high voltage power supply and introduces a new Phase Shifted Full Bridge (PSB) converter based on the conventional Phase Shifted (PS)

Zero-Voltage-Transition (ZVT) Pulse-Width-Modulation (PWM) Full-Bridge (FB) converter. The new PSB converter has the conventional PSB's advantage of soft switching while being immune to short circuits.

An analysis of a switching cycle of the new PSB is provided, and results from SPICE simulations are included in a later section. The merits and shortcomings of this particular circuit are presented and conclusions drawn from it.

CURRENT-FED BRIDGE CONVERTER

A CFB converter (Figure 1) is currently used as the supply for the TWT RADAR high voltage requirements. It consists of a conventional hard switched FB converter running at near unity duty ratio at a frequency, Freq, of 80kHz. Snubbers around each MOSFET are required to limit resonance between parasitic inductances and the output capacitance of the MOSFET itself. In common with all hard switched converters this topology exhibits a switching loss which is proportional to switching frequency. This limits the maximum frequency at which this bridge can be operated. During an arc, the circuit's impedance determines the maximum current ratings for components on the transformer primary. Thus, a large input choke, L_{Choke} , is placed between the full bridge converter and TPWM, to slow down and limit the

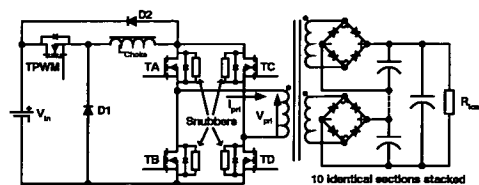


Figure 1 CFB Converter Circuit Diagram

current rise.

The output voltage is controlled by pulse width modulation of the series MOSFET TPWM Gate drive V_{GatePWM} (Figure 2). Diodes D1 and D2 are required for current to freewheel during periods when either TPWM or all MOSFETs are off.

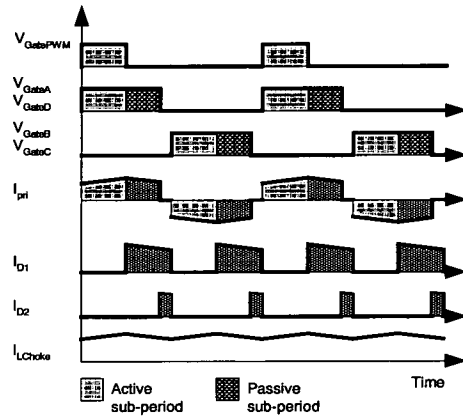


Figure 2 CFB Operation Waveforms

PHASE SHIFTED BRIDGE CONVERTER

The PS-ZVT-PWM-FB converter is a topology of choice amongst high power SMPS designers [1]. Leakage inductance is used to provide soft switching of the four MOSFETs. The need for snubbers is eliminated, and the MOSFETs' internal body diode replaces the traditional anti-parallel diodes. The new PSB converter (Figure 3) is primarily the same as the conventional PS-ZVT-PWM-FB converter. The new PSB operates in a discontinuous current conduction mode (DCM) (Figure 4) as opposed to the conventional PSB, which operates in a continuous current conduction mode (CCM). It uses a larger primary inductance L_{pri} , consisting of leakage inductance, L_{leak} , and a supplementary inductor, L_{add} . L_{pri} not only drives the Zero-Voltage-Transition around the primary MOSFETs, it is also used to slow the rate of rise of primary current, I_{pri} , during an arc. This together with the way the converter is operated, ensures that the converter does not fail during an arc.

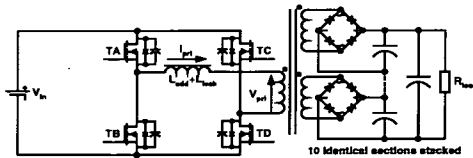


Figure 3 PSB Converter Circuit Diagram

Assumptions for Mathematical Analysis

MOSFETs and diodes are treated as ideal with no forward voltage drop and *on*-state resistance. Equivalent fixed value capacitors C_{AB} and C_{CD} model the variable parasitic MOSFET drain-source capacitances, C_{DS} , for the left and right legs of the full bridge respectively.

The output capacitive filter is assumed to be ideal and can be modelled as a constant voltage source V_{out} (Equation 1) in parallel with the transformer primary.

$$V_{\text{out}}' = V_{\text{out}} \cdot \frac{\text{turns}_{\text{primary}}}{\text{turns}_{\text{secondary}}} \quad (1)$$

Detailed Analysis

Operating waveforms for the converter are as shown in Figure 4. All four MOSFETs operate at near 50% duty. PWM is achieved by phase shifting the MOSFET gate drive waveforms of the left and right leg. This controls the overlap between diagonally opposite MOSFETs and determines the active period. A delay time is inserted between the *on*-duration of each MOSFET on the same leg to prevent cross conduction. Zero Voltage Switching (ZVS) of MOSFETs TC and TD is achieved by proper setting of the delay time between their gate drives [1]. Due to the large inductance within the bridge, the converter is operated in discontinuous mode to avoid duty loss, while providing Zero Current Switching (ZCS) for TA and TB.

The operation of the new PSB can be broken up into sub-periods as shown in Figures 4 and 5. Operation in t_4 - t_8 is symmetrical with the first half of the switching period, t_0 - t_4 , thus operation of the PSB during each sub-period is analysed for the first half period only.

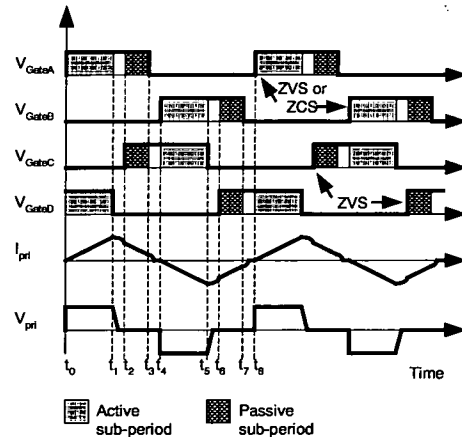


Figure 4 PSB Operation Waveforms

t_0 - t_1 : (Active power transfer sub-period)

TA & TD are both switched on; inductor current I_{pri} rises linearly with Equation 2

$$I_{pri}(t) = I_{Lstart} + \frac{V_L}{L_{pri}}(t - t_{start}) \quad (2)$$

under the following initial conditions as shown in Figure 5a.

$$I_{Lstart} = I_{d0} = 0 \quad (3)$$

$$V_L = V_{in} - V_{out}' \quad (4)$$

At the end of this sub-period, the current would have risen to its peak of

$$I_{pk} = I_{d1} = I_{d0} + \frac{V_{in} - V_{out}'}{L_{pri}} \left(\frac{2 \cdot D}{Freq} \right) \quad (5)$$

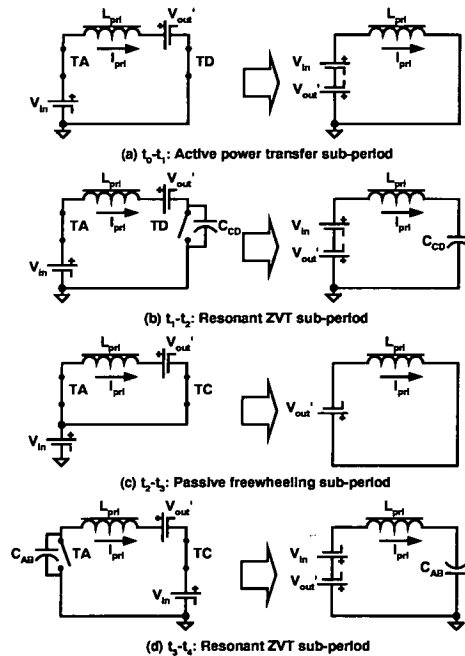


Figure 5 Simplified Equivalent Circuit Diagrams for (a) t_0 - t_1 , (b) t_1 - t_2 , (c) t_2 - t_3 and (d) t_3 - t_4 sub-periods

 t_1 - t_2 : (Active – Passive resonant transition sub-period)

TD is switched off; current in the inductor and transformer charges C_{cd} to raise drain-source voltage of TD to V_{in} , thus preparing TC for ZVS. Equations for the simplified resonant voltage source, inductor and capacitor circuit shown in Figure 5b are provided in [2].

The duration of delay between TD switching off and TC switching on is set to enable the equivalent capacitor C_{cd} to fully charge and clamp to V_{in} for ZVS turn on of TC. When C_{cd} has clamped to V_{in} , currents continue to flow through TC's inherent anti-parallel diode and freewheel around the top half of the bridge before TC switches on. When this happens the converter is ready to proceed to sub-period t_2 - t_3 .

 t_2 - t_3 : (Passive freewheeling sub-period)

Figure 4 shows that current I_{pri} falls linearly in the primary of the transformer while freewheeling through TA and TC during t_2 - t_3 . The inductor current equation for this is obtained by substituting the conditions shown in Figure 5c into Equation 2 where:

$$V_L = -V_{outpri}' \quad (6)$$

$$I_{Lstart} = I_{d2} \quad (7)$$

 t_3 - t_4 : (Passive – Active resonant transition sub-period)

TA turns off, any residual current in the inductor and transformer will discharge the equivalent C_{AB} lowering the drain-source voltage of TB down to zero for lossless switching. However, if the current has already fallen to zero, then TB will switch on under ZCS.

During this sub-period, the simplified circuit in Figure 5d looks similar to Figure 5b. However, I_{d3} is much smaller than I_{d1} and the source voltage is negative. Soft switching under ZCS is therefore much easier than ZVS, which requires a larger current I_{d3} , resulting in operation under CCM giving rise to duty loss. Therefore the delay time between the gate drives of TA and TB, need only be set to a minimum to avoid cross-conduction.

SPICE SIMULATION OF BOTH CIRCUITS

The two circuits described were simulated using ORCAD PSPICE with the following conditions:

Output voltage:	2.5kV
Input voltage:	330VDC
R_{load} :	7352 Ω
Output power:	850W
L_{leak} :	3.6 μ H
L_{add} :	6.3 μ H
L_{choke} :	1mH

Normal Operation

During normal operation of the current-fed bridge converter, ringing caused by leakage inductance can be clearly seen on the primary winding waveforms of the transformer (Figure 6). All five MOSFETs undergoing hard switching can also be observed.

The voltage, current waveforms and sub-period information for a period of operation of the PSB converter is shown in Figure 7. ZVS can be observed

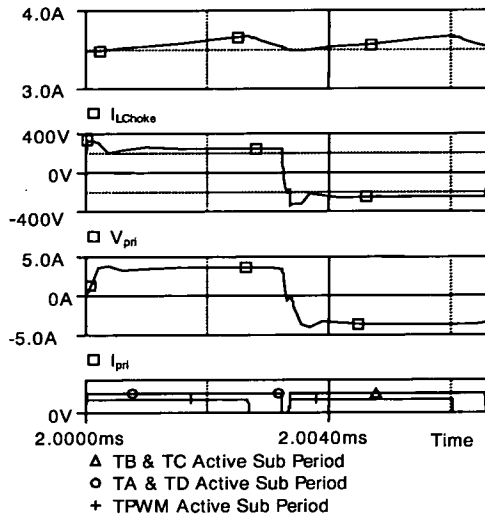


Figure 6 CFB PSPICE Simulation Waveforms

on V_{pri} waveform where it has gently fallen to zero under resonance just before TC and TD are switched on to initiate the passive sub-period. ZCS can also be observed on the I_{pri} waveform where its value is zero when TA and TB are switched on before the active sub-periods. Voltage and current waveforms on the transformer are free of the ringing caused by leakage inductance in conventional converters.

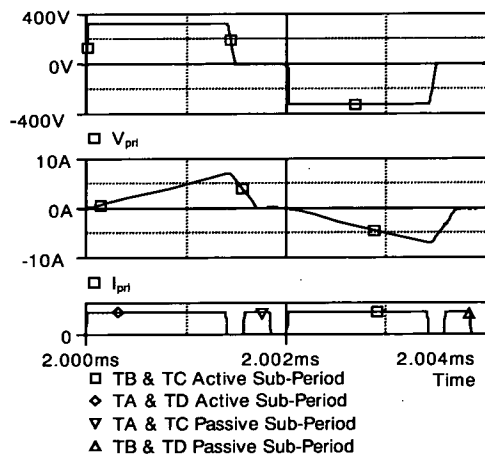


Figure 7 PSB PSPICE Simulation Waveforms

Simulation of an Output Arc

The arcing condition is modelled as a switch with an *on*-state resistance of 100Ω short-circuiting the output at $t=2.5\text{ms}$. This has the effect of causing the output capacitive filter to dump its charge into the corona

discharge. In a conventional voltage-fed converter using a voltage mode feedback loop, the collapse of the output voltage causes the duty to further increase, hence feeding the discharge and destroying the primary MOSFETs with huge currents. Therefore, current mode feedback control is used in addition for such arc prone converters.

As current mode control requires time to react to load changes, the converters are simulated in open loop so that the behaviour of the converter can be observed when a corona discharge has occurred and duty has remained constant.

Figure 8 shows that when the CFB converter output short-circuits, the voltage waveform on the primary collapses too, except for spikes caused by leakage inductance. The current in the transformer primary continues to rise slowly, and may only be detected by the feedback circuit after a few cycles, during which it would have been feeding the discharge, potentially damaging the TWT RADAR.

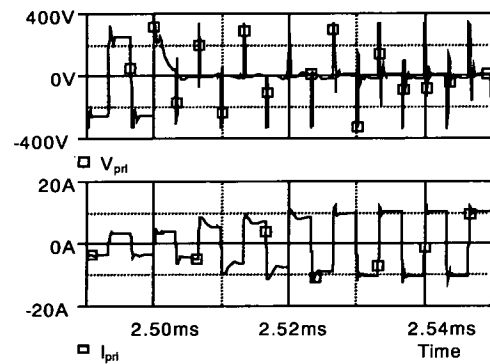


Figure 8 CFB Converter Short Circuit Waveforms

On the other hand, it can be seen from Figure 9, that the new PSB converter can detect the arc in one cycle of its operation. The peak current in the transformer primary is determined by the primary inductance, switching period, and maximum duty (Equation 8).

$$I_{MAX} = \frac{2 \cdot V_{inMAX}}{L_{pri} \cdot Freq} \quad (8)$$

As the inductance is located between the legs of the bridge, the peak currents are limited and forced to change polarity at each cycle, thus protecting the MOSFETs.

COMPARISON AND COMMENTS

When compared to the current-fed bridge, the new phase shifted bridge has the following advantages:

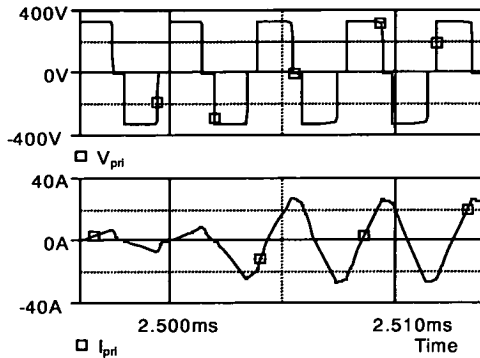


Figure 9 PSB Converter Short Circuit Waveforms

- Reduction in component count (snubbers, freewheeling diodes, TPWM removed).
- Large L_{choke} is replaced by smaller L_{pri} which fully utilises the high leakage inductance inherently present in high voltage transformers.
- All MOSFETs are soft switched.
- PSB waveforms have lower $\frac{dv}{dt}$ and $\frac{di}{dt}$, thus the converter should emit less electromagnetic interference.
- Current rise caused by short circuits can be detected in the first cycle enabling the converter to shut down quickly.
- Higher efficiency and thus reduced cooling requirements.

However, there are certain trade-offs when using the new PSB converter:

- MOSFETs have to be rated for higher currents.
- Inductor losses will be higher due to DCM operation
- Component values have to be calculated carefully for correct operation and short circuit protection.
- Input voltage operation range, transformer turns ratio and converter output power requirements have to be balanced. As Figure 10 shows, the PSB output power is limited by the variables mentioned.

CONCLUSIONS

This paper has presented a current-fed full bridge currently used as an HV SMPS. A new phase shifted bridge converter, based on the conventional PS-ZVT-

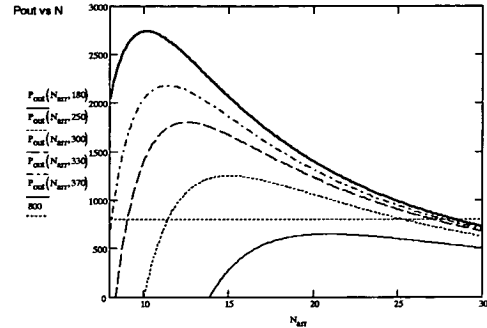


Figure 10 Graph of Output Power Against Turns Ratio at Various Input Voltage Levels

PWM-FB converter, was introduced and shown to be particularly suited for use as a HV SMPS due to its efficient use of parasitics and immunity to an output arc. The next stage is to build a prototype, test and verify its capabilities. The energy reclaimed by using soft switching has to be also evaluated against higher conduction losses, transformer and inductor hysteresis losses.

ACKNOWLEDGEMENTS

The authors would like to thank BAE Systems for their kind support and funding of this research.

REFERENCES

1. Sabaté, J.A. et al, Design Considerations for High-Voltage High-Power Full-Bridge Zero-Voltage-Switched PWM Converter, APEC '90, Fifth Annual Applied Power Electronics Conference and Exposition Conference Proceedings, Los Angeles, USA, pp 275-84, 1990.
2. Mohan, N. et al, Power Electronics: Converters, Applications, and Design, Wiley, pp 254, 1995.

AUTHOR'S ADDRESS

The first author can be contacted at

ESG, Room 115,
Department of Electronics and Electrical Engineering
University of Edinburgh
King's Buildings, Mayfield Road
Edinburgh EH9 3JL
Scotland UK

Email: Richard.loh@ieee.org

An Improved Phase Shifted Bridge Converter for High Voltage Applications

C.K.R.M. Loh and D.E. Macpherson

School of Engineering and Electronics, University of Edinburgh, Scotland, UK.
Richard.Loh@ee.ed.ac.uk, Ewen.Macpherson@ee.ed.ac.uk, Fax: + 44 131 650 6554

Keywords: Converter circuits, high voltage DC power supplies, zero voltage switching, LDD auxiliary circuits, switch mode power supplies.

Abstract

In high voltage (HV) applications, it is attractive to dispense with the expensive output inductor and operate with a purely capacitive filter. This paper shows that the HV Phase Shifted Bridge with capacitive filter (PSBCF) converter can lose soft switching in two MOSFETs. This can result in a lower efficiency and a limitation of operation to the lower switching frequencies. The LDD auxiliary circuit developed for the standard PS-PWM-ZVS-FB converter is adapted to assist the HV PSBCF with ZVS. The operation of the auxiliary circuit is explained and its performance examined

1 Introduction

High voltage switch mode power supplies (SMPS) used in airborne travelling wave tube radar applications require very high efficiency and low EMI emissions, and are prone to suffer from problems with load arcing. Resonant converters have been used to improve efficiency, but to reduce and filter coupled noise the power supply should be synchronised to the radar pulses, thus variable frequency controlled resonant converters are not ideal. A common solution is to use a current fed bridge converter (CFB) [1], consisting of a Full Bridge (FB) converter running at a constant near maximum duty with a front-end buck converter controlling the dc current, and with a simple capacitive output filter. The front-end buck uses a large choke to provide current smoothing and, importantly, to slow current rise in event of an arc occurring in the TWT radar. In an arc, surge arresters are triggered to protect the radar by diverting all energy away into the surge arrester; the output thus effectively resembles a short circuit. Without a large choke, currents will quickly rise to beyond the switches' current carrying ability if the control circuitry is unable to detect and respond in time. The large choke considerably increases the converter weight and also stores large amounts of energy that can prolong the arc by feeding into it.

2 High Voltage Phase Shifted Bridge Converter

The HV PSBCF described in [1] is particularly useful for this application. This has been developed from the standard Phase Shifted (PS) Pulse Width Modulation (PWM) Zero Voltage

Switching (ZVS) FB Converter [4] using multiple secondary rectifier sections to stack the output voltage but without an output inductor. Instead, it uses a much smaller inductance located in series with the transformer, incorporating the large leakage inductance already present in the transformer (unavoidable in high voltage transformers) that would otherwise degrade converter performance. Even the conventional PS-PWM-ZVS-FB converter would suffer from excessive duty loss due to the large value of leakage inductance, although it already utilises it to assist with soft-switching. In addition, the PSBCF, eliminates the need for an output filter inductor, which is physically large, heavy and expensive. Being a PWM converter it can be easily synchronised to the radar.

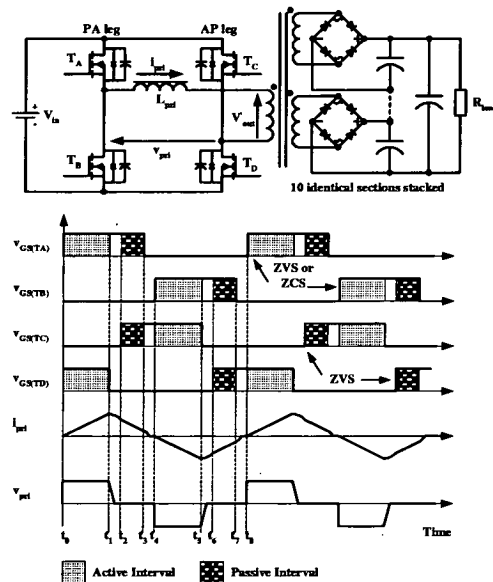


Figure 1: Schematic and Waveforms for the HV PSBCF

The PSBCF operates in discontinuous current mode (DCM), thus the active-passive (AP) leg of the bridge should turn on with ZVS and the passive-active (PA) leg with ZCS. In practice the PA leg rarely achieves any form of soft switching due to the parasitic distributed capacitance of the transformer

windings and reverse recovery of the secondary rectifier diodes. Charges stored in these parasitic capacitances resonate with the primary inductance after current in the primary has dropped to zero (Figure 2). Depending on the natural frequency of the resonating components, the direction of current flow in L_{pri} affects whether soft switching is achieved.

2.1 Detailed Operation (Figure 1)

Active interval (t_0 - t_1)

During the active interval, power is transferred to the secondary when TA and TD are both switched on. The current level through L_{pri} increases linearly as it is charged by the input voltage less the reflected output voltage, $V_{in} - V_{out}$.

Active-Passive transition interval (t_1 - t_2)

At t_1 , TD is switched off and the summed MOSFET output capacitance of the AP leg, C_{CD} , resonates with L_{pri} , to bring $V_{GS(TD)}$ to zero allowing it to undergo zero voltage switching turn-on at t_2 .

Passive interval (t_2 - t_3)

From t_2 , the current circulates in the output through both the secondary and primary of the transformer during this passive interval. i_{Lpri} is falling as it is flowing against the reflected output voltage held up by the output capacitors.

Passive-Active interval (t_3 - t_4)

At t_3 , after TA turns off, if there is any energy left in the inductor, it will resonate with the summed output capacitance of the PA leg, C_{AB} . If the energy level is sufficient (Equation 1), TB would be able to turn-on with ZVS, otherwise, TB would turn on with partial soft-switching, which would reduce the effect of charge dumping by reducing $v_{DS(TB)}$ at turn-on.

$$\frac{1}{2} L_{pri} i_{pri}^2 \geq \frac{1}{2} C_{AB} V_{in}^2 \quad (1)$$

However, in experiments, when the converter was operating below the critical duty for boundary condition, i_{pri} continued to flow in the opposite direction after having fallen to zero before the next MOSFET turns on. In Figure 2a, i_{pri} continues to flow through the body diode of TA, after TA turns off, and when TB turns on, it has to undergo hard switching. It is also possible for TB to undergo soft-switching (Figure 2b) if the resonance interval, $t_{offResonance}$, is greater than half the natural resonant period of the parasitic resonant network, thus bringing i_{pri} positive again.

The hard-switching during turn-on for the PA leg MOSFETs, charge dumping and reverse recovery losses for the poorly performing body diode all contribute to the increased switching losses on the PA leg.

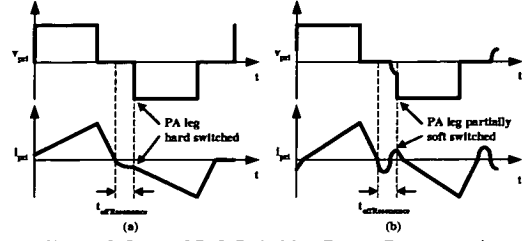


Figure 2: Loss of Soft Switching Due to Resonance in Transformer Parasitics

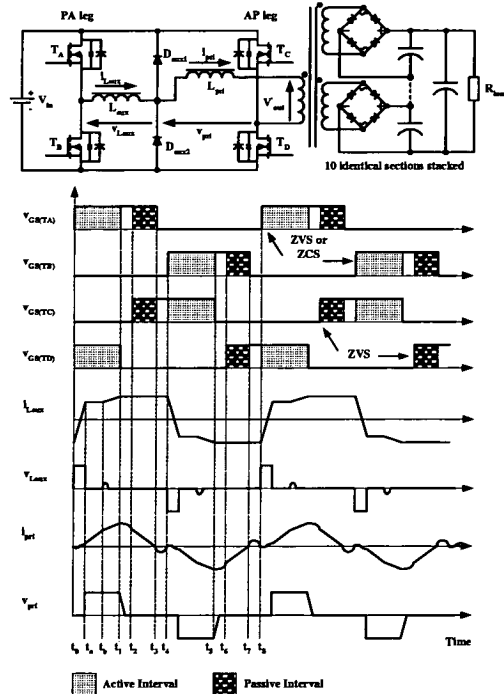


Figure 3: Schematic and Waveforms for the HV PSBCF with LDD Auxiliary Circuit

3 LDD Auxiliary Circuit

To improve the efficiency, the inductor-dual diode (LDD) auxiliary circuit is adapted from the conventional PS-PWM-ZVS-FB converter for use in the PSBCF. The LDD auxiliary circuit was first examined for use with a LC filtered PSB converter in [2]. An inductor is added in series with the primary inductor next to the PA leg. The inductor, L_{aux} , is used to provide the energy required for ZVS of the PA leg, and the diodes are used to allow the current in L_{aux} to flow after current in L_{pri} has fallen to zero. In the conventional PSB, the LDD auxiliary circuit was later attached to the AP

leg instead and used the transformer's magnetising currents to aid soft switching in addition to the auxiliary circuit [3]. However, this results in a higher magnetising current that will contribute to the current stress during an output short circuit. Thus, only the LDD auxiliary circuit attached to the PA leg is considered here. As the circuit operates in discontinuous conduction mode (DCM) with a capacitive filter compared to the conventional continuous conduction mode (CCM) with an LC filter, the LDD auxiliary circuit behaves differently than when in the conventional PSB.

3.1 Detailed Operation (Figure 3)

Recovery interval (t_0 - t_1)

At t_0 in Figure 3, ZVS has been achieved for TA. TA is now switched on and due to the change in polarity of voltage across L_{aux} the current through L_{aux} , $i_{L_{aux}}$, starts to change direction. The gradient of the current change can be determined using Equation 2.

$$\frac{di_{L_{aux}}}{dt} = \frac{V_{in}}{L_{aux}} \quad (2)$$

The current continues to rise until it reaches $i_{L_{pri}(t_1)}$. $i_{L_{pri}(t_1)}$ is determined by the I_{RM} value of the auxiliary diode, D_{aux2} , which was previously conducting. During this interval $i_{L_{aux}}$ has to go to zero before D_{aux2} can begin to recover and V_{in} only appears across the transformer at t_1 when D_{aux2} reaches its peak recovery current value. This is shown in voltage and current waveforms of a diode undergoing reverse recovery in Figure 4. This results in a loss of duty for the converter and the duty loss can be expressed as in Equations 3 and 4.

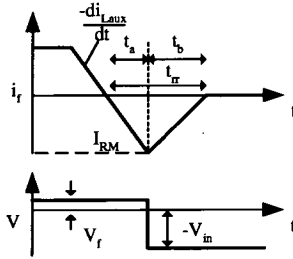


Figure 4: Prototype waveforms for PSBCF without auxiliary circuit at half load

$$d_{loss} = \frac{t_1 - t_0}{T_{0.5}} \quad (3)$$

$$t_1 - t_0 = \frac{i_{L_{aux}(t_0)}}{\frac{di_{L_{aux}}}{dt}} + t_a \quad (4)$$

The ratio of t_b to t_a , S , is also known as the 'softness' factor. As di/dt is determined by the inductor, the peak recovery value depends on the softness factor and reverse recovery charges of the diode. Thus, it is better to select a soft diode with low recovery charges to minimise the duty loss and keep circulating currents to a minimum.

First active interval (t_1 - t_{1a})

During this interval, current in L_{pri} is being charged up after D_{aux2} has recovered. During this time, $i_{L_{aux}(t_1)}$ continues to circulate around TA, L_{aux} and D_{aux1} . As the current builds up in L_{pri} it approaches $i_{L_{aux}(t_1)}$ which occurs at t_{1a} .

Second active interval (t_{1a} - t_2)

At t_{1a} , the current flowing in D_{aux1} has dropped to zero and the currents now flow through TA, L_{aux} , L_{pri} and TD, satisfying $i_{pri} = i_{L_{aux}(t_1)}$. Current in L_{pri} now rises at a rate determined by the summed primary and auxiliary inductance value (Equation 5).

$$\frac{di_{pri}}{dt} = \frac{(V_{in} - V_{out})}{(L_{aux} + L_{pri})} \quad (5)$$

Active-Passive transition interval (t_2 - t_{2a})

The AP transition interval is again similar to that of the PSBCF without any auxiliary circuit, with the exception that the resonant inductor value of L_{pri} should be replaced with $L_{aux} + L_{pri}$. TC should be able to switch on with ZVS due to the high levels of current flowing through the summed resonant inductance by t_{2a} .

Passive interval (t_{2a} - t_{2b})

During the passive interval, the currents in the two inductors are free to take their own values again. i_{pri} ramps down as with the PSBCF without auxiliaries while $i_{L_{aux}}$ circulates around TA, L_{aux} and D_{aux1} .

Passive-Active transition interval (t_{2b} - t_2)

During this interval, the summed MOSFET output capacitance of the PA leg, C_{AB} , resonates with L_{aux} . As the current in L_{pri} has now fallen below that of L_{aux} , the current flow is now separated again.

The overall effective duty of the converter is reduced due to the reverse recovery of the auxiliary diodes with L_{aux} limiting $di_{L_{aux}}/dt$. Therefore using fast recovery 'soft' diodes with low recovery charge helps reduce duty loss. A PSBCF converter can be simply modified by inserting the additional required components to an existing PSBCF design. A minimum value of L_{aux} should be used to avoid disrupting the converter circuit's operation. If the duty loss caused by the auxiliary is unacceptable, it can be compensated for by reducing the value of L_{pri} by an appropriate amount such that the overall power capability of the converter remains the same.

As the energy stored within L_{aux} is determined by the peak current in L_{pri} (which is $i_{pri(2)}$), a minimum load specification is required for the converter so as to allow the value of L_{aux} to be determined for enough energy to be stored in L_{aux} to overcome the energy stored in C_{AB} (Equation 6) for ZVS to occur.

$$\frac{1}{2} L_{aux} i_{pri(Peak)}^2 \geq \frac{1}{2} C_{AB} V_{in}^2 \quad (6)$$

If the minimum value of inductance is used, duty loss is reduced and more power is obtained from the converter. The maximum amount of inductance is determined by the reverse recovery characteristics of the diode, which in turn determines the duty loss.

4 Circuit for comparison

To compare the circuits a HV PSBCF converter with the specifications listed in Table 1 was built and simulated in PSPICE and compared with one utilising the LDD auxiliary circuit

Prototype converter specifications	
Power	850W
Switching Frequency	250kHz
Input voltage (V_{in})	370V
Output Voltage (V_{out})	1kV
Turns ratio (Secondary/Primary)	4
L_{pri}	18uH
L_{aux}	8uH

Table 1: Specifications for PSBCF prototype

5 Results

Figure 5 shows the prototype waveform captures for the PSBCF without auxiliary circuit running at half load (425W). The transformer parasitic resonance can be seen on the i_{pri} waveform when v_{pri} has fallen to zero and i_{pri} changes its direction. This also appears on the midpoint of the AP leg, V_{AP} , as either a spike before it rises to V_{in} or a dip before it falls to zero. The loss of soft-switching can also be observed in Figure 6, where $v_{DS(TB)}$ can be seen to be falling only after $v_{GS(TB)}$ is turned on. As explained in the previous section, this is due to i_{pri} flowing in the wrong direction through the body diode of TA instead of TB. Due to the partial loss of soft switching in the PSBCF, high frequency operation at full load could not be achieved.

By utilising the LDD auxiliary circuit, the main converter waveforms remain largely unchanged as shown in Figure 7. However, when TB is observed closely in Figure 8, it can be seen that $v_{DS(TB)}$ is at zero volts when $v_{GS(TB)}$ is turned on, thus achieving ZVS for the PA leg. The current flowing through the PA leg is kept positive by the LDD auxiliary circuit which prevents the body diode of TA from conducting.

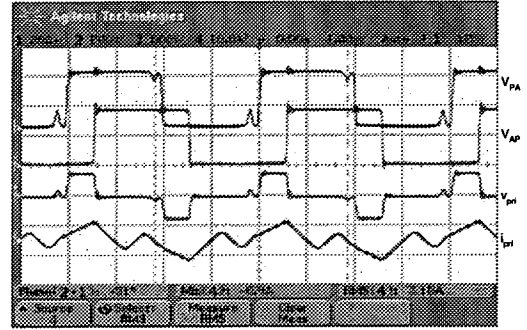


Figure 5: Prototype waveforms for PSBCF without auxiliary circuit at half load

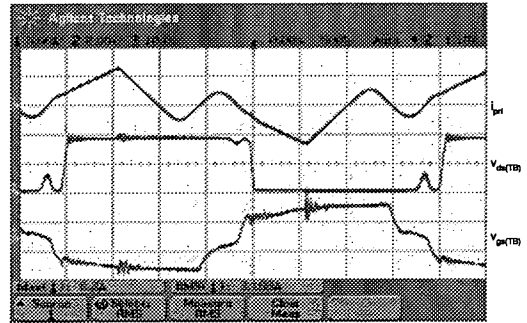


Figure 6: Prototype MOSFET TB for PSBCF without auxiliary circuit hard-switching waveforms

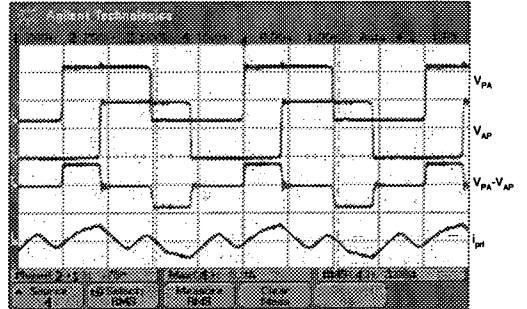


Figure 7: Prototype waveforms for PSB with LDD Auxiliary at half load

The PSPICE simulation waveform in Figure 9 shows the converter being subjected to a 1ms short circuit (represented by a switch with an 'on' resistance of 1ohm) directly applied across the high voltage output of the converter. It can be seen

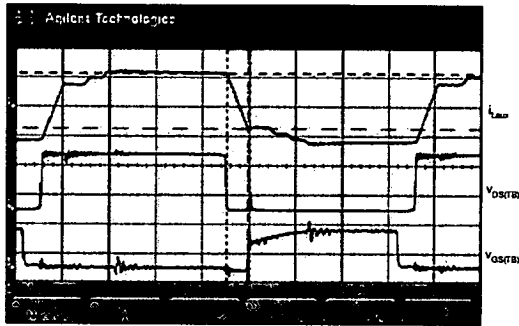


Figure 8: Prototype MOSFET TB for PSBCF with LDD auxiliary circuit hard-switching waveforms

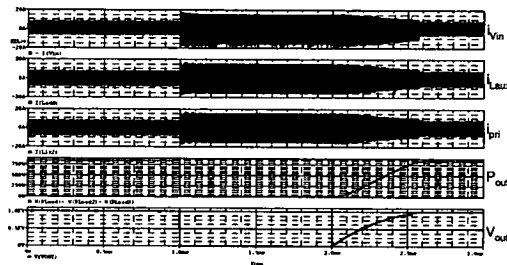


Figure 9: PSBCF with LDD auxiliary circuit short circuit simulation waveforms

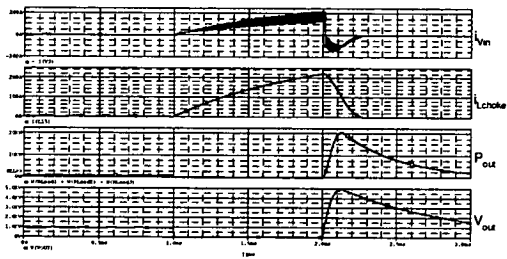


Figure 10: Current Fed Bridge short circuit simulation waveforms

that at no point during the short circuit simulation does the currents in L_{pri} , L_{aux} or input exceed the predetermined value set when designing the PSBCF converter. Figure 10 shows that when the same short circuit is applied to the current fed bridge currently in used, the DC choke currents and converter input currents continue to rise unless otherwise limited either by parasitic resistances in the circuit or when the over current is sensed and converter shut down. Figure 11 shows the prototype PSBCF converter with auxiliary circuit undergoing a short circuit in steady state. This is achieved by replacing

the high voltage secondary rectifiers with a fuse and switching the converter input supply on.

Power	Efficiency
Load	850W
PSBCF (No Auxiliary)	88%
PSBCF (LDD Auxiliary)	91%

Table 2: Full load efficiencies for the various PSBCF converters

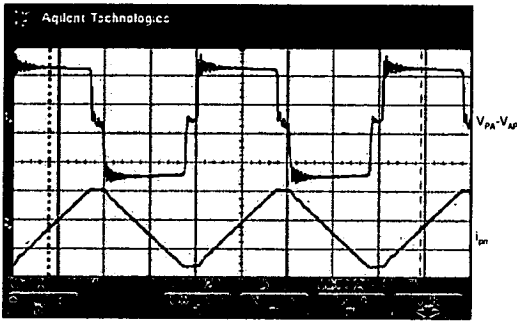


Figure 11: Actual prototype PSBCF with LDD auxiliary circuit short circuit waveforms

Table 2 shows the full load efficiencies for the PSBCF converter with and without the LDD auxiliary circuits. The efficiency readings for the PSBCF without auxiliary circuit are obtained from loss estimates using PSPICE simulations. Although these estimates show that the overall efficiencies do not vary by much between the two converters, a detailed analysis of the switching losses show that the PA leg MOSFETs suffer from an overall 55W switching loss compared to the AP leg which has only 7W switching losses. MOSFETs on either leg of the PSBCF with LDD auxiliary circuit also only suffer from switching losses of approximately 7W to 8W. The actual efficiency of the PSBCF converter with LDD auxiliary is 90.8%.

5.1 Advantages and disadvantages of the LDD auxiliary circuit

Using the LDD auxiliary circuit enables the PSBCF converter to operate with ZVS on all MOSFETs, which it was unable to do previously due to the DCM operation. The efficiency and operation of the converter is much easier to predict as the PA leg MOSFETs now switch with ZVS over a predetermined load range whereas previously it depended on the resonant frequency of the transformer parasitics and output load. There is also an increase in efficiency of 3% (approximately 32W)

The additional L_{aux} located in between the PA and AP legs mean that during a short circuit, the peak short circuit currents are lower than when operating with just L_{pri} alone.

Unfortunately, this added protection comes at a price and duty is lost due to the reverse recovery of the auxiliary diodes and additional impedance during the active interval. This can be compensated for by lowering the value of L_{pri} to increase the overall output power of the converter. Overall, the converter will still experience lower short circuit peak currents while being able to provide the required output power.

6 Conclusions

The paper has presented a means of improving the high voltage PSBCF converter by adapting the LDD auxiliary for it. The original PSBCF converter suffered from a loss of soft-switching on the PA leg due to transformer parasitics, and the use of the LDD auxiliary circuit ensures that ZVS is achieved on that leg. As a result, efficiency and reliability is improved and in addition, the inherent short circuit protection is improved too. The PSBCF topology with LDD auxiliary circuit is now a viable converter topology for use in a high voltage application.

Acknowledgements

The authors would like to thank BAe Systems for funding this research, especially to Mr Frank Fisher for his expertise and advise on high voltage radar applications.

References

- [1] C.K.R. Loh, D.E. Macpherson and F. Fisher, "Phase Shifted Full Bridge Converter for High Voltage Applications", *36th Universities Power Engineering Conference, UPEC 2001 Conference Proceedings*, University of Wales Swansea, UK
- [2] R. Redl, N.O. Sokal and L. Balogh, "A Novel Soft-Switching Full-Bridge DC/DC Converter: Analysis, Design Considerations, and Experimental Results at 1.5kW, 100kHz", *IEEE Transactions on Power Electronics*, volume 6, No. 3, July 1991, pp. 408-418
- [3] R. Redl, L. Balogh, D.W. Edwards, "Optimum ZVS full-bridge DC/DC converter with PWM phase-shift control: analysis, design considerations, and experimental results", *9th Applied Power Electronics Conference and Exposition, APEC 1994 Conference Proceedings*, February 1994, pp 159-165
- [4] J.A. Sabate et al, "Design Considerations for High-Voltage High-Power Full Bridge Zero-Voltage-Switched PWM Converter", *5th Applied Power Electronics Conference and Exposition, APEC 1990 Conference Proceedings*, March 1990, pp. 275-284