

# CMOS VLSI CIRCUITS FOR IMAGING

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## **Declaration**

Unless otherwise stated, the material contained herein was researched and composed entirely by myself in the Department of Electrical Engineering, University of Edinburgh between December 1987 and May 1993.

Wang Guoyu (G. Wang)

## **Acknowledgements**

I am grateful to my supervisors, Dr. D. Renshaw and Professor P. B. Denyer, for their unsparing support and constant encouragement during the course of this work.

A special word of thanks must go to M. Lu for her invaluable cooperation in the development of the project.

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## Abstract

MOS technology is very attractive for achieving low-cost miniature cameras. It also permits the inclusion of the sensor with other control and processing functions on the same chip. However, this technique has never been developed to the point at which MOS sensor performance matches that of CCD cameras.

The objective of this project has been to develop design techniques to achieve single chip video cameras, in unmodified CMOS processes, with improved performance (aimed to match the performance of CCD cameras) and enhanced functionality.

In this thesis, following an overview of solid state image sensors, the fundamentals and basic sensor array structure suitable for CMOS implementation is presented. The pixel structure and sensor array, the sense amplifier, scan circuitry, and the output amplifier and buffer are described. Noise analysis is also presented with the main noise sources highlighted and compensation schemes proposed. Other useful on-chip techniques including auto-exposure control, gain control, and data conversion are then discussed. A successfully designed device, named ASIS-1011 which incorporates all these circuit techniques, is finally reported. This design shows that the aim of achieving good picture quality and incorporating sensors and control logic on one chip can be achieved.

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# Chapter 1 INTRODUCTION

## 1.1 Project Background

The research and development of solid state silicon image sensors has attracted and maintained considerable interest.

The driving forces behind this are the increased video camera market and widespread potential for electronic vision applications. Examples include:

- consumer camcoders and still cameras,
- television broadcast cameras,
- telecommunications (video telephones),
- security cameras,
- image capture for personal computers,
- bar-code and text readers,
- biometric verification (fingerprint, faces, etc.),
- production line inspection,
- military use (target tracking, etc.),
- traffic control,
- robot visions, and automotive applications,
- smart toys, etc.

All these applications are sensitive to cost, size, and power consumption. Commonly they use commodity camera modules and image processing hardware and/or software. These systems can hardly be described as miniature, and usually, their cost, size, and power consumption are limitations for wider applications. The camera module itself is one of the dominant limiting factors.

It is well known that silicon can act as an excellent photoreceptor over the visible

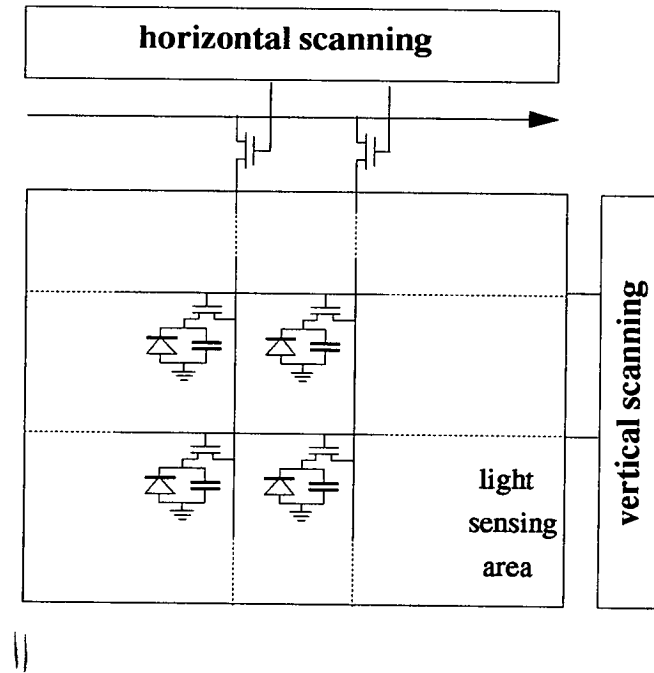
spectrum. One of the most significant developments leading to the realization of a practical solid-state image sensor was the utilization of the p-n junction photodiode operating in an integration mode. Charge-storage operation is based on the principle that, if a p-n junction is reverse-biased and then isolated, the charge stored on the depletion layer capacitance decays at a rate proportional to the incident illumination level [Sze, 1981; Middelhoek, 1989; Haskard, 1988].

Compared with vacuum video tubes solid-state image sensors have obvious advantages. They are small, lightweight, of low power consumption, require little maintenance, and have a long life. Solid-state image sensors come in several technologies, including CCD (Charge Couple Device), MOS (Metal Oxide Semiconductor), and CID (Charge Injection Device). All these sensors use the p-n junction as the photoreceptor. The difference among them is in the readout techniques utilized [Wechder, 1965; Tseng, 1965; Chamberlain, 1986]. The majority of solid-state cameras today use CCD technology which, over two decades, has been highly refined to optimize its performance. However, cameras and vision systems addressed by today's CCD technology are still power-hungry and expensive, and fall short of the highest level of integration.

On the other hand, MOS technology, as a popular VLSI technology, is very attractive for achieving low-cost miniature cameras. Another important factor is that MOS technology, especially CMOS, permits the inclusion of the sensor with other control and processing functions on the same chip, to achieve smart vision application systems. Despite encouraging results, however, this technique has never been developed to the point at which MOS sensor performance matches that of CCD cameras.

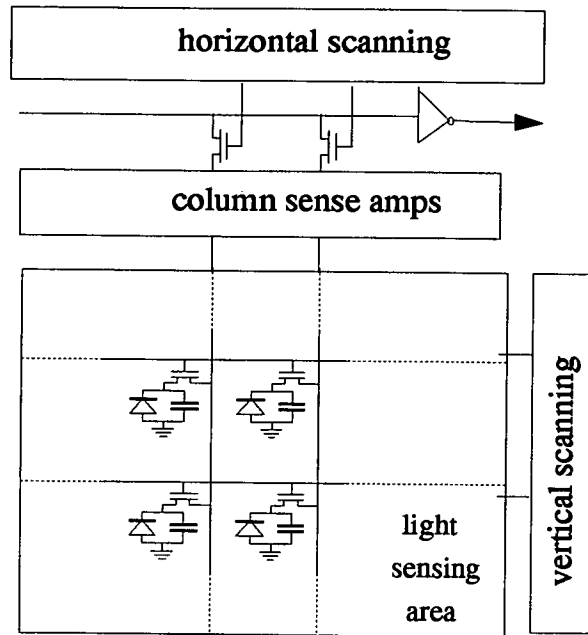
Noise remains a fundamental problem which limits the development of MOS sensors and MOS vision systems. In fact, it is a limitation which hampers the huge potential application and market of MOS image sensors. The main emphasis has been on reducing the noise and improving the picture quality. The research work of our project is a contribution to this.

In the normal structure of MOS sensors (Figure 1.1), the signal charge is usually read out through the column line with large parasitic capacitance. Commonly, the column lines are gated through an analogue multiplexer to a single external charge sense amplifier. The requirements of this amplifier are daunting considering that wide dynamic range and high-speed must be achieved from a charge packet in the pixel which may be of the order of fC.



*Figure 1.1 Normal structure of MOS sensors*

Accordingly a scheme was proposed by Professor P. B. Denyer to overcome this problem [Denyer, 1989]. The novel feature of the scheme is the integration of analogue CMOS charge sensing amplifiers at the top of every bit line, as shown in Figure 1.2. The benefits are that these amplifiers need not work so quickly, since their activation frequency is equal to the line rate rather than the pixel rate; and they are situated as close as possible to the pixel array so the line capacitance is reduced.



*Figure 1.2 New structure of MOS sensors*

A prototype was designed and fabricated in unmodified CMOS ASIC technology. Although the design itself, as a final year student project, is very basic, the image is surprisingly better than expected. The image signal is not drowned by the noise, due to the on-chip amplifiers, even in the dark.

Although the picture quality is far from perfect, the prototype did show that, with the amplifiers on the top of the array, the readout of the MOS sensor array became easier. Therefore, further development along this direction looked worthwhile. The objective of such work could include:

- Modification of sense amplifiers to optimize their function;
- Addition of an output buffer to improve the driving ability;

- Increased resolution;
- Integration of the control logic with the sensor array;
- Implementation of more camera functions on chip;
- Noise sources should be investigated and the chip should be more carefully designed to minimize the noise.

## 1.2 Project review

I have taken part in the project since the end of 1987. The project was then supported by the Science & Engineering Research Council (Grant GR/F 36538 IED2/1/1159, August/1989-July/1992) with Dr. D. Renshaw and Professor P. B. Denyer as principal investigators [Renshaw, 1992]. I registered as a part-time Ph.D. student in October, 1989.

The objective of my project has been to develop design techniques to achieve single chip video cameras, in unmodified CMOS process, with improved performance (aimed to match the performance of CCD cameras) and enhanced functions.

The first task facing me was to reduce noise so that picture quality of MOS image sensors improves. The work involved was to investigate all noise sources, highlight the main ones, and then eliminate them, or reduce them to an acceptable level. Only if this could be achieved without special requirements for process modification or external circuitry, can it be realistic to develop viable single chip video cameras implemented entirely in commodity ASIC CMOS technology.

The second task of the research was then to integrate a photodiode array together with all the necessary sensing, addressing and amplifying circuitry, as well as control logic on the same substrate. A subsequent aim was to achieve some enhanced functionality on chip, such as automatic exposure control, automatic gain control, analogue to digital



conversion, using CMOS design techniques.

With cooperation from another researcher and informative instructions from my supervisors, the objectives of this research have been met. We have developed unique CMOS circuit design techniques to realize single chip video cameras, in unmodified CMOS technology, which match and in some respects exceed the performance of CCD cameras and enjoy unprecedented reductions in size, cost and power consumption.

The main technical achievements are summarized as follows:

- Fixed pattern noise has been reduced to 40dB, by automatically compensating each sense amplifier to give near zero offset.
- Automatic exposure control has been implemented on chip, enabling the use of a single fixed-aperture lens. Control is achieved by varying the integration time prior to reading photo-pixels, giving a total exposure range of 40,000:1, wider than that of most commercial cameras.
- Gain control is implemented through putting a digitally controlled MDAC (Multiplying Digital to Analogue Converter) as an adjustable load. It extends sensitivity in low ambient light so that a dim image can become more visible on a monitor and more detail is retained in data conversion. The MDAC also supports successive approximation analogue to digital conversion.
- Digital control logic such as TV-formatting, exposure control, and gain control have been integrated on the same substrate to implement single chip video cameras.

- Other technical features include auto-calibrated video black level, a simple method to implement  $\gamma$  correction and a solution for wafer stage test.

Six different designs of single chip CMOS video cameras have been completed during the past 4 years, including 3 commercial products [Wang, 1988-1992]. These designs have proven that three technical barriers which most greatly influence new product development: namely cost, power consumption and size, can all be dramatically reduced when compared with today's solid-state camera technologies.

Nine technical papers have been published [see publications], of which one paper entitled "CMOS Video Cameras", won the "Best Circuit Award" in the conference of EURO ASIC 91. Another paper entitled "On-chip Automatic Exposure Control Technique" won the "Best Paper Award" in the conference of ESSCIRC'91. There was also an "Award for Innovative Technology", at the International Fire and Security Conference at Olympia in 1992, granted for a remote alarm verification system which is based on a customized image sensor chip developed by us [Watts, 1992; Wang 1990].

The most immediate commercial benefit and probably the most significant outcome of this research has been that it has successfully engendered a new line of business, with the foundation of VLSI Vision Ltd. This is a company set up to trade in CMOS image sensor and sensor-processor designs and techniques, and has over the three years of its existence profitably developed products for third parties from British and overseas industry. This has lead to quantifiable benefits to the research programme, the University and the wider academic, research and commercial communities.

### **1.3 Thesis structure**

In this thesis, following the first chapter of introduction is a chapter of overview which reviews the evolution and present status of research and development in the field of solid state image sensors. Three category sensors (CCD, CID, and MOS) are introduced with the comparison between them. Some new photo-element structures aimed at future high definition television applications are also mentioned.

The fundamentals and architecture of an array sensor suitable for CMOS implementation are introduced in the third chapter. The pixel structure and the sensor array, the sense amplifier, the scan circuitry, and the output amplifier and buffer are covered.

The fourth chapter is on noise. The analysis is carried out for both random noise and fixed pattern noise, with main noise source highlighted. A compensation scheme to eliminating fixed pattern noise caused by mismatch of sense amplifiers is presented. Other techniques to reduce noise are also discussed.

The fifth chapter discusses dynamic range. On-chip automatic exposure control and on-chip automatic gain control are introduced with both algorithm and circuitry covered.

Other techniques such as on-chip data conversion, on-chip black level calibration, on-chip  $\gamma$  correction, and wafer stage testing are then described in the sixth chapter.

As a design example, the seventh chapter presents a single chip video camera, named ASIS-1011, which we believe is the smallest commercial video camera in the world. The features, the design, and the characterization of the device are covered in details.

The last chapter contains some discussions on remaining problems, recommendations for future work, and conclusions.

## **Chapter2 SOLID STATE IMAGE SENSORS: AN OVERVIEW**

### **2.1 Introduction**

Work on solid state image sensors was started in 1960s, with the aim of replacing vacuum tube image sensors. The obvious disadvantages of vacuum devices are the large amount of space required for the electronics and coils, and big power consumption. On the other hand, solid state image sensors offer significant advantages: much greater compactness, low voltage and power reduction, reliability and expected cost reduction. Also, digital scanning provides a geometric accuracy of scan and a versatility of addressing. These advantages could introduce many new applications which were not feasible for vacuum image devices. During the course of the past two decades, solid state image sensors have experienced a tremendous amount of development due to the huge commercial success of home-video cameras, as well as security and industrial applications.

It is well known that silicon can act as an excellent photoreceptor over the visible spectrum. One of the most significant developments leading to the realization of a practical solid-state image sensor was the utilization of the p-n junction photodiode in integration mode. Charge-storage operation is based on the principle that, if a p-n junction is reverse-biased and then isolated, the charge stored on the depletion layer capacitance decays at a rate proportional to the incident illumination level [Sze, 1981; Middelhoek, 1989; Haskard, 1988; Sequin, 1975]. Therefore, a photodiode array can be used to produce electronic signals corresponding to a focused image. To electronically “read” this picture, each pixel on the array is selected in the sequence, controlled by the scan circuitry along both y-direction and x-direction. The image, in the form of electronic charge, can be restored by display devices such as TV monitor and computer terminal.

The entire function of image sensors may be likened to a single-transistor DRAM (Dynamic Random Access Memory) module, except data is written optically. Both

devices have a cell array constructed in a regular two-dimensional format, plus address and amplification circuitry. However, the design of sensors is more difficult than that of DRAM, in that sensors deal with analogue signals whilst RAMs only have to store and output digital signals. The challenge of the sensor design is how to achieve rapid, low-noise detection of the tiny charge within each pixel.

Solid state image sensors are classified into three main categories: CCD (Charge Couple Device), MOS (Metal Oxide Semiconductor), and CID (Charge Injection Device). In fact, all these sensors work on the principle of charge storage, employing essentially the same photodiode structure to sense incident light and convert it into an electric signal. The main difference is in the way they read out signals. CCD devices transfer the signal charge by manipulation of MOS potential wells. It shifts the signal charge in series to an output sensing node. CID devices transfer the collected signal charge within an individually addressed pixel, and sense displacement values across the electrodes at the site. MOS devices transfer the signal charge by multiplexing the photoarray, using a digital scanner, in the way similar to RAM readout. Each of these technologies has its merits as well as drawbacks. They all have come a long way from the first primitive forms to their present structures [Wechder, 1965; Tseng, 1985; Chamberlain, 1986; Hobson, 1978; Michon, 1973; Sun, 1988; Tompsett, 1973].

There are appreciable advantages to be gained by building color image sensors using solid state sensors instead of vacuum tubes. In color cameras using vacuum tubes, the incident light from the scene is separated into the red, green and blue components by a prismatic assembly located immediately behind the camera lens. The three color components are then sensed separately by three tubes. Great care has to be taken to ensure that the three beams sweep with nearly perfect mutual registration. In replacing these tubes with solid state sensors, the discreteness and precision geometry of the integration sites and the clock controlled readout can automatically ensure linear and mutually aligned tracking of the scan in all three sensors, once the initial mechanical positioning has been done.

Solid state cameras have the advantage of geometric scan accuracy. This makes it possible to make compact color cameras only using one sensor array. This is achieved

by depositing color stripes directly onto the photo-array, making 3 neighbour pixels produce different color information. The resolution of the array for the use of color cameras will have to be 3 times that of monochrome cameras. The reduction in yield associated with a larger devices and problems with the fabrication of the color stripes have been solved. Today, color solid state cameras with TV standard resolution are in wide use.

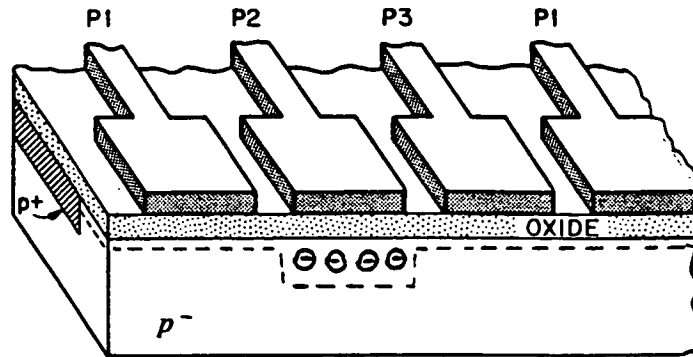
Compared to monochrome solid state image sensors, color sensors require higher resolution, higher sensitivity, and more complicated circuitry for balancing and combining 3 color components. Other than this, basic design techniques are the same as for monochrome sensors. So far as the market is concerned, there still are big requirements for monochrome cameras where the color of the picture is not important and the cost is of more concern. Examples of these requirements are security application and production line inspection. The research reported in this thesis concerns monochrome devices only.

This chapter will review the evolution and the present status of research into three main categories of solid state image sensors: CCD image sensors, CID image sensors, and MOS image sensors. Comparison will be made between them. Following this is an introduction to some new photo-element structures which are being investigated for future high definition television applications.

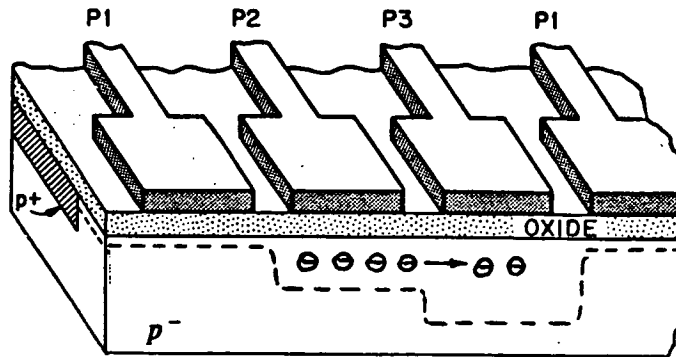
## **2.2 CCD image sensors**

In the simplest implementation, CCDs consist of closely spaced capacitors on an isolated surface of a semiconductor, as shown in Figure 2.1 [Tseng, 1985; Chamberlain, 1986; Amelio, 1974]. Figure 2.1a shows the potential well during integration and storage when only one electrode is turned on. During charge transfer, with two adjacent electrodes simultaneously turned on to the same potential, the charge packet will distribute uniformly underneath the two electrodes. When the first electrode is turned off, the charge will be pushed completely to the second one (Figure 2.1b). To continue

this charge transfer, the following electrode is pulsed to a high potential, and so on.



(a) during integration and storage



(b) during charge transfer

Figure 2.1 Basic cell of a 3-phase CCD

The device is referred to as a surface channel CCD if it transfers and stores the signal charge in the potential wells at the interface between the silicon and silicon dioxide. The interaction of the signal charge with interface states imposes certain lower limits on transfer inefficiency and transfer noise. These limitations can be alleviated by using a bulk channel device, which involves the use of an epitaxial or ion implanted silicon layer (or both) of opposite polarity to that of the substrate. This shifts the maximum

potential of the wells away from the interface and into the bulk, as shown in Figure 2.2.

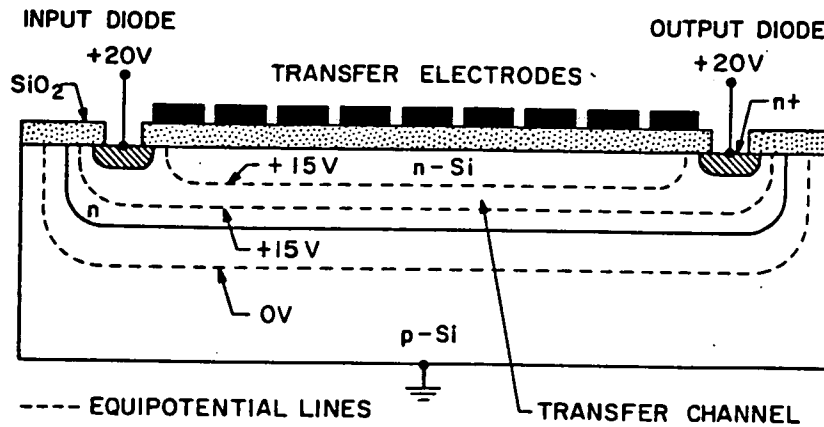


Figure 2.2 Longitudinal cross section through a bulk channel CCD

Whenever charge is transferred from one gate to the next in a CCD a fixed fraction of the signal charge is left behind. *Charge Transfer Efficiency (CTE)* is a parameter measuring the amount of charge transferred from one cell to the next, and is expressed as a number between 0 to 1. CTE values can range anywhere from 0.9995 to 0.99999. Thus, CCD is a nearly ideal analog shift register.

Two readout organizations have been developed for area image sensors. They are frame-transfer structures and interline transfer structures, as shown in Figure 2.3. Figure 2.3a shows the frame-transfer structure, in which, a separate shielded storage area is needed. After integration, the charge packets collected in the sensing area are shifted rapidly into the storage area. Signal charge packets in the storage area are then read out line by line, while the sensing area is integrating the next field. Figure 2.3b shows an interline structure, in which a separated shielded vertical CCD register is needed along each column of sensing cells. After integration, the charge packets in the sensing cells are transferred into the vertical shift register in parallel. Vertical shift registers then transfer the charge into the horizontal readout register one line at a time, while the photo pixels are integrating the next field.



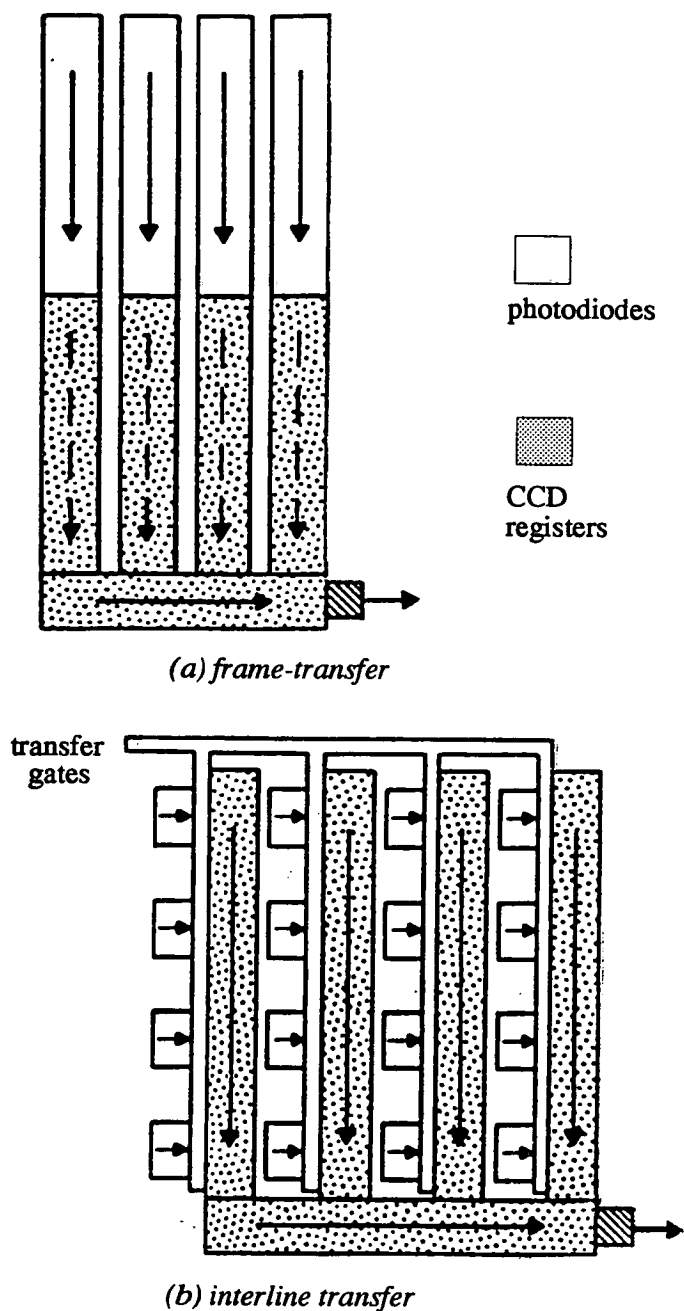


Figure 2.3 Readout organization of CCD

The development of CCD began in 1969 at Bell Labs. A prototype of color camera was demonstrated in early 1970 which uses three small resolution CCD sensor chips. In

1978 a prototype of color camera using only one CCD sensor chip was reported [Dillon, 1978]. Since then, CCD image sensors have been highly refined to improve picture quality, increase the resolution and sensitivity, reduce the pixel size and chip area, and optimize their performance. Today, 2/3 inch and 1/2 inch CCD sensors with the resolution of around  $256 \times 256$  and  $512 \times 512$  are widely used. In fact, the majority of present solid state cameras use CCD sensors [E. Martin, 1990].

However, efforts to improve all features including higher resolution, and lower cost have never stopped. Recent trends are toward small size and high resolution. For this purpose, 1/3 inch format CCD sensors with around 250K pixels have been developed [Kuriyama, 1991; Hojo, 1991; Losee, 1989; Matsunaga, 1991; Akimoto, 1991]. Miniaturization of CCD cameras keeps making progress. On the other hand, CCD sensors with million of pixel have been developed [Blouke, 1985; Akiyama, 1986; Stevens, 1987; Oda, 1989; Yonemoto, 1990; Nobusada, 1988]. These sensors are aimed for the future high definition television (HDTV) system which requires much higher resolution than that for the current standard television systems [Crooijmans, 1991; Geiger, 1991].

The diagonal of the image area for 1/2 and 1/3-in image sensors are respectively 8.0 and 6.0 mm. A 1/3 inch format will reduce the chip area to approximately 60% of conventional 1/2 inch devices, along with cost reduction and power consumption reduction. However, the pixel size is essentially reduced if the resolution is the same. This causes degradation in performance (mainly photo sensitivity). To tackle this problem, either on-chip microlenses are implemented and/or a high sensitivity amplifier is used [Kuriyama, 1991; Hojo, 1991, Furukawa, 1992].

The recent advances in the miniaturization of CCD cameras is related to the trend to reduce size, weight and power in hand-held camcorders for the consumer market. A Japanese company, Sony, launched its first camcorder, light weight video camera, in 1989. It then has shrunk the size and cost of its products through development of the tape mechanism and optical subsystems. Smaller lenses in turn require smaller and more sensitive image array. [Wilson, 1992]

Improved sensing and signal amplification techniques have enabled Sony to increase optical sensitivity at the same time as reducing the sensor area. This has been achieved by increasing the number of pixels per unit area and improving the sensitivity of pixels with new charge amplifiers. The sensitivity has been increased by a factor of four while reducing sensor array size from 1/2 inch to 1/3 inch. Sony's 1/2 inch CCD contains 440K pixels while 1/3 inch CCD has achieved 290K (figure of 1992) and Sony believes it can improve this figure further.

It is a challenge to achieve CCD sensors for HDTV. It requires not only high resolution ( $1920 \times 1035$  pixels), but also very high operational speed (74.25 MHz). It is difficult to reduce pixel size and to increase the operational speed both by such a large amount, while maintaining a wide dynamic range, and high signal-to-noise ratio. As feasibility research for future HDTV cameras, a 1-in format, 2 million pixel, interline CCD image sensor has been reported [Oda,1989], which adapts to the 16:9 aspect ratio, 1125 scanning lines, 60 fields, and 2:1 interlace HDTV system proposed at CCIR'86. In order to follow up ultrahigh-speed, the device uses a dual channel horizontal CCD register configuration and hybridize a bipolar buffer transistor chip in the same package as the sensor chip.

A 4 million pixel CCD has previously been developed [Blouke,1985], it is only applicable to a slow-scanning television system and only usable for capturing still images. [Akiyama, 1986; Stevens, 1987] reported one million pixel CCD image sensors, applicable to special-use systems. [Sakakibara, 1991] reported a 1-inch format 1.5M pixel CCD image sensor for an HDTV camera system. To achieve a low smear ratio while maintaining a high level of sensitivity, they developed a new impurity profile of a buried p+ layer and an on-chip micro lens array whose material is a deep-UV resist. Other papers reporting 2M pixel HDTV image sensors include [Manabe,1988; Negishi, 1991, Harada, 1992; and Shibata,1992].

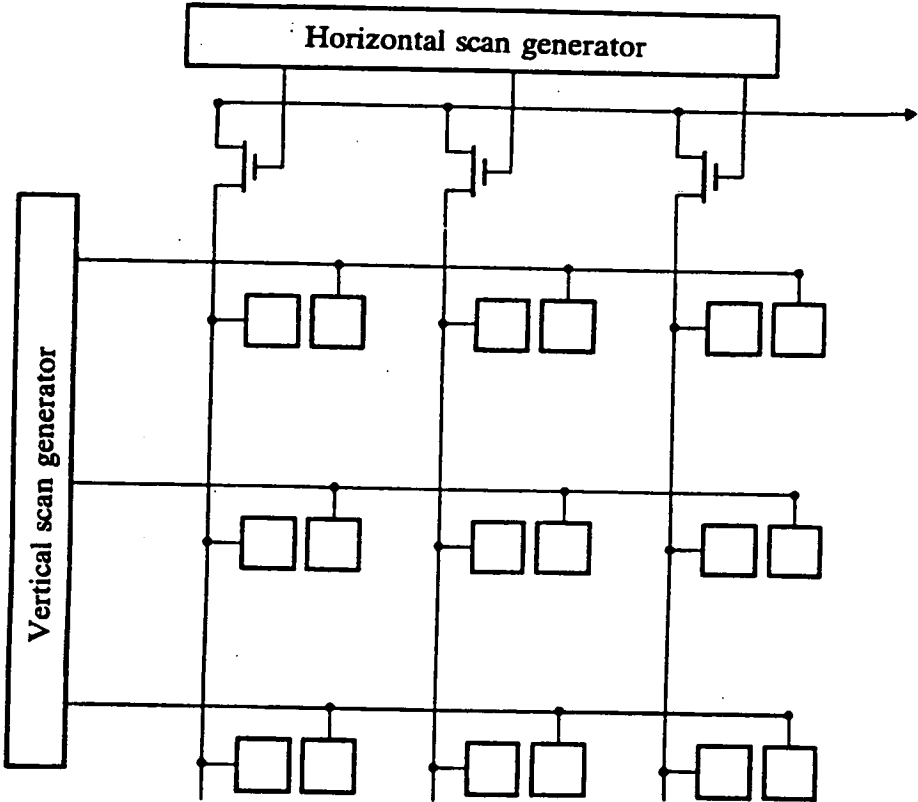
## 2.3 CID image sensors

The development of charge injection device (CID) image sensors started in the early 70's at General Electric [Michon, 1973; Sun, 1988; CIDTEC; Williams]. CID use the

same type of potential well minority carrier storage as CCD does but charge transfer can only occur between two cells. The transfer can occur in either direction but otherwise the pair of cells are isolated from other cells. Basically the CID consists of a two dimensional matrix with a pair of adjacent MOS capacitors at each crosspoint (Figure 2.4a). As long as at least one of these two electrodes is biased on, the photogenerated charge can be stored. Alternatively it can be shuffled back and forth repeatedly between these capacitors (Figure 2.4b). When both capacitors are pulsed to zero simultaneously, the potential well collapses, and the charge is injected into the substrate, where it recombines (Figure 2.4c).

This is the process of charge injection. A corresponding charge flow occurs in the external circuit and it can be sensed through the column bias line. However, the recombination process may take many microseconds in the high lifetime material which is required to give low dark current, and thus the minority carriers may spread into neighbouring elements, or the signals of subsequently read elements may be mixed together. To overcome these problems, most CID image sensors are fabricated on epitaxial material. The epitaxial junction, which underlies the imaging array acts as a buried collector for the injected charge.

Readout can also be implemented by measuring charge transfer between two storage capacitors of each pixel. The transfer can be performed on all sensing sites along a row in parallel. Each row can also be cleared of signal charge by performing the injection operation in parallel at all pixels in the selected row. This readout technique has been termed "parallel injection". A diagram of a  $4 \times 4$  array using parallel injection is illustrated in Figure 2.5 with the relative surface potential and signal charge included. At the beginning of a line scan, all rows have voltage applied and the column lines are reset to a reference voltage,  $V_s$  by means of switches S1 through S4 and then allowed to float. A row (X3 in Figure 2.5) is selected for readout, causing the signal charges at all pixels of that row to transfer to the column electrodes. The voltage on each floating column line then changes by an amount equal to the signal charge divided by the column capacitance. The horizontal scanning register is then operated to scan all column voltage.



(a) basic readout organization

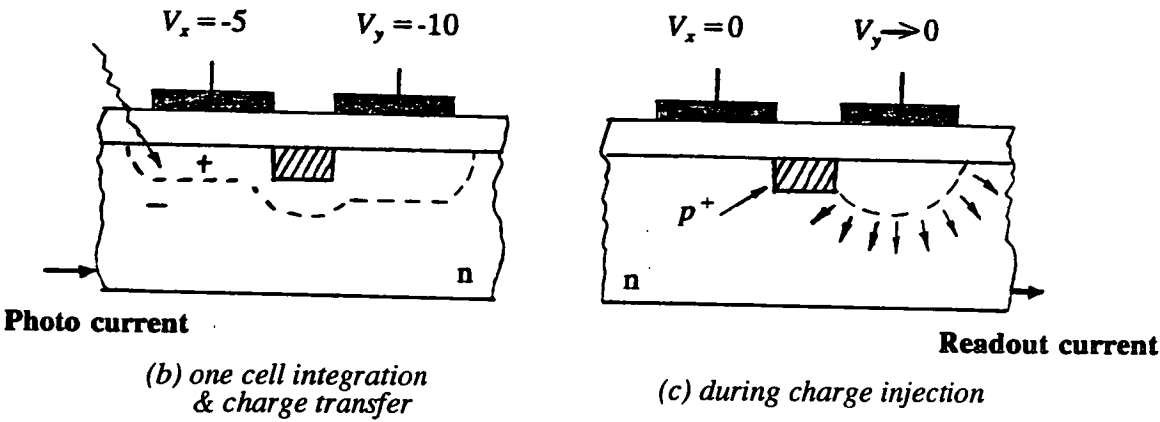


Figure 2.4 Charge injection device (CID)

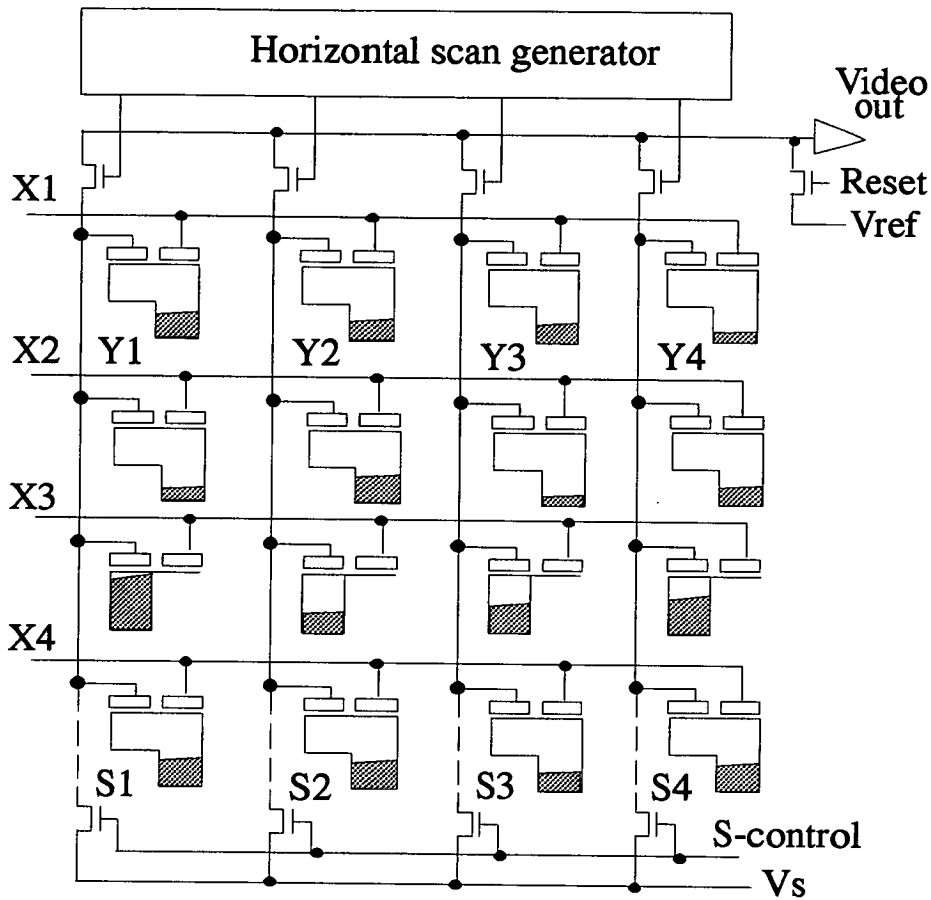


Figure 2.5 A  $4 \times 4$  CID array designed for parallel-injection readout

At the end of each line scan all charges in the selected row can be injected simultaneously by driving all column voltage to zero through switches S1 to S4. Alternatively, the injection operation can be omitted and voltage reapplied to the row after readout, causing the signal charge to transfer back under the row electrodes. This action retains the signal charge and constitutes a nondestructive readout operation.

Generally speaking, CID cameras are not competitive with CCD cameras. The main reason is fixed pattern noise and high video line capacitance which make image quality

poor, especially in the low light conditions. The other drawback is the requirement for an epitaxial substrate which is not compatible with standard VLSI ASIC processes. The epitaxial layer also causes loss of sensitivity due to absorption of photons by the layer.

On the other hand, CID has its merits such as nondestructive readout, contiguous pixel structure, and better anti-blooming performance. While CCD cameras are dominating the home video and commercial security markets, CID development is taking a different tack. Targeting system automation, CID sensors focus on achieving complete, accurate, and distortion-free image data acquisition for computer processing with fast, flexible timing and function control.

Nondestructive readout techniques enhance user control of light integration and image readout, useful for low-light applications. Integration may proceed for milliseconds or up to hours with the addition of sensor cooling, applied to retard accumulation of thermally-generated dark current. Camera readout may continue at video rates, but charge injection is inhibited, so the developing image can be viewed on a TV monitor as integration proceeds. This real-time exposure control is especially useful for resolving faint details in low-light scientific applications, significantly expanding dynamic range.

Blooming is a condition when excessive charges spill from over-saturated elements to adjoining pixels or the charge transfer paths. It will eradicate portions of the image. CID sensors are more tolerant to intense light due to the epitaxial layer which draws the excessive charges. This inherent anti-blooming performance ensures accurate image details even under extreme lighting conditions, making CID cameras particularly effective for testing and measurement (especially laser analysis), missile tracking, and a wide variety of other applications where reflections and the appearance of specular light intensities give rise to over-saturated regions within a properly exposed image.

The contiguous pixel structure of CID arrays further contributes to accurate imaging because there are virtually no opaque areas between pixels where image detail can be lost. This attribute is important for applications where precise dimensional data is critical. Examples include the determination of object edges for inspection,

measurement, positioning, and tracking. It is also essential for applications where complete data is crucial, as in particle analysis where illuminated particles may disappear if they fall into opaque regions.

Pixels in the CID array can be addressed individually. This makes flexible readout and processing options possible. For maximum flexibility random access CID is currently under development. The random access CID incorporate address decoders instead of sequential shift registers to provide programmable access to individual pixels in any sequence for readout and special charge manipulation routines.

## **2.4 MOS image sensors**

The predecessor of the MOS image sensor can be dated back in 1965 when the first monolithic integrated photodiode array structure was announced [Wechder, 1965; Tseng, 1985; Chamberlain, 1986]. It consists of 200 photodiodes, each associated with an MOS FET. The gates of MOS FETs are individually driven by an external scan generator. However, this structure wasn't developed further at that time because MOS technology was in its infancy. Instead, a phototransistor structure was pursued. It was thought to be better due to the transistor gain. The major disadvantages and factors which eventually returned the photodiode to favour, were the random variations in transistor gain and the low level threshold due to the emitter offset. Only after MOS technology was developed (in particular silicon gate technology was developed), the marriage between MOS technology and the photodiode array operating in storage mode has resulted in today's MOS image sensor.

MOS sensors use a digital scanner to multiplex signal charges from photo pixels to the output, in the way similar to RAM readout. A typical structure of MOS sensors has been shown in Figure 1.1.

The light sensing area consists of a diode array matrix, schematically indicated by the columns and rows of individual photo-pixels. The photodiodes are pre-charged to a fixed bias voltage and then isolated. This results in a fixed charge being stored on the associated junction capacitance. The photodiodes are then left isolated for a suitable



exposure time. During this time, incident light upon each pixel partially discharges the junction capacitance. The rate of discharge is proportional to the incident light level. The final charge retained on the capacitor, after a fixed time interval, will represent the light intensity at that point of the image. The pixel signal is read out by opening the gate, connecting the photodiode to the MOS transistor drain. All of the drains in each column are connected in common and only one row is read at any time. The column lines are then gated through an analogue multiplexer to a single external charge sense amplifier.

The attraction of MOS sensors is that it is this technology, especially CMOS, that is the dominant technology for VLSI chips. Therefore, this technology is more easy-access and cost effective. More importantly, this technology has the advancing capability, permitting the integration of control and process logic on the same substrate. A smart vision system may be implemented on a single chip with the advantages of both solid state image sensors and VLSI systems.

Other virtues include the full inherent sensitivity, low voltage driving, custom pixel structure, and flexible readout scheme. Unlike CCD or CID pixel structure, MOS sensors require no surface electrode on the top of discrete photodiodes so that there is no interference pattern or light loss. Like all MOS devices, The sensors only require a single low voltage driving (normally 5 volt).

Other than a photodiode and an access transistor on each pixel, extra transistors can be put in to enhance the function of the pixel. For example, a transistor connecting the photodiode to ground may be added to increase the anti-blooming ability [Renshaw, 1991]. Another example is a image-motion detection device [Chong, 1992]. A pixel of this device consists of a photodiode, a switch, and a cell called current-mirror differentiator which detects the light current variation of the pixel.

The sensor array can be read out in the normal sequence or in other scan out scheme. One example is a CMOS image sensor chip for fingerprint verification [Anderson, 1991]. The addressing and read out circuits have been modified to allow local two dimension smoothing ( $3 \times 3$ ) to take place as the image data is scanned out. Just by changing the readout scheme, the required low-pass filtering is implemented without

any hardware overhead.

Hitachi is the leading company to develop MOS sensors. It introduced color video cameras in 1981 and camcorders in 1985 [Noda, 1986; Asano, 1988]. A array structure called TSL (Transversal Signal Line) structure, as shown in Figure 2.6, was developed by the company.

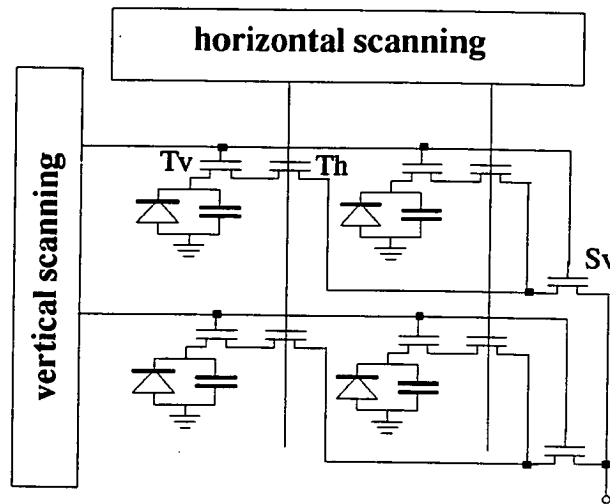


Figure 2.6 TSL structure

Compared with the normal structure of Figure 1.1, a new MOS switch is added to each pixel and the signal readout line is laid out horizontally. The information stored in each photodiode is read out in the following manner: the vertical shift register turns on the Tv and readout transistor (Sv), and the horizontal shift register turns on Th by transferring information to the external. The essence of this structure is that electric charges from each pixel stay only a short time on the signal line so that smear noise is suppressed. The normal structure may suffer from smear noise from overcharging of the vertical signal lines during the horizontal scanning period.

However, MOS sensors suffer a significant problem: high noise. The big video line capacitance results in the high random noise. The process nonuniformity results in the high fixed pattern noise. Most commercial MOS cameras (such as Hitachi's) at present

do not integrate control logic together with the sensor array. They usually consist of a X-Y addressable MOS photoarray chip, along with boards of components. One reason is that MOS sensors are so noisy that complicated off-chip sense and amplification circuits are needed. Another reason is that although the digital circuitry can be put on chip, the digital interference causes a big problem. The cameras assembled in this way do not enjoy the real virtue of the MOS technology, *integration*. They can not compete with CCD cameras because of the inherent high noise.

On the other hand, even though the image quality may not be as good as that of CCD, it is still very attractive to include a sensor array with other control and processing functions on the same chip. There are many applications where the image quality may not be so crucial but other matters such as cost, volume, power consumption, and system integration are more important.

One early example is a one-dimensional motion detector [Tanner, 1984] which consists of an array of photodiodes for detecting the light pattern, a storage array for the image, circuitry to compute the correlation between the stored image and the current one, decision circuitry to determine where the correlation is greatest, and a self timed controller to sequence the entire system.

Another example is a matrix array picture processor which can handle image processing tasks such as sensing, digitization and data reduction. [Forchheimer, 1990]. The device contains a  $256 \times 256$  photosensor array, 256 8-bit serial A/D converters, 256 bit-serial processors and a  $256 \times 128$  memory. Two  $256 \times 8$  bi-directional shift registers are used for communication between processor elements and I/O (Figure 2.7). This chip is aimed at pre-processing of gray level images and binary images, eliminating the bottleneck of sequential image read-out that characterizes conventional systems. It is suitable in applications demanding high-frame rate digital image processing with greatly reduced I/O bandwidth, complexity and system cost. [Gibertoni, 1991] also reported a smart image sensor for computer vision. The chip comprises a grid of light sensitive pixels and a set of processors operating in parallel.

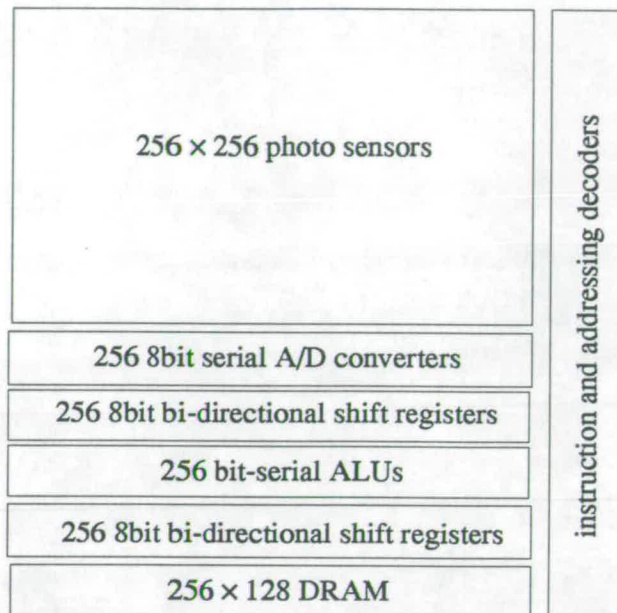


Figure 2.7 a matrix array picture processor

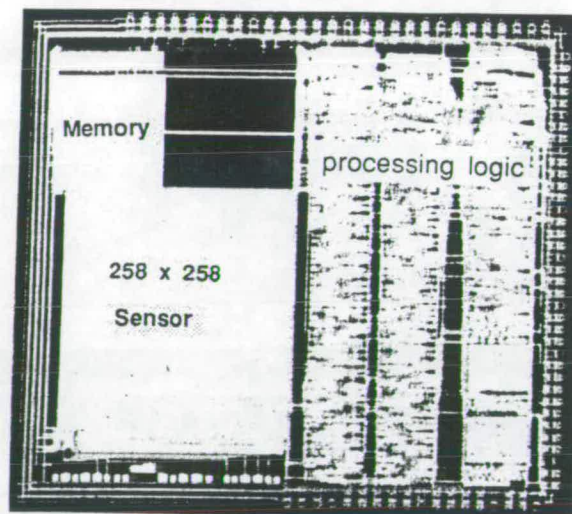


Figure 2.8 a sensor chip for fingerprint verification

Our group also implemented a smart image sensor chip for fingerprint verification [Anderson, 1991]. Other than a  $258 \times 258$  pixel array, it includes image preprocessing

and quantisation circuitry to form a normalised binary image, 64-cell 2000 M op/sec correlator array, post-correlation decision logic, 16K bits RAM, and 16K ROM (Figure 2.8). With the aid of two external devices (one 64Kbit RAM and one 8052 microcontroller), this device performs all of the image sensing and processing functions necessary to capture and verify a fingerprint against a stored reference print within one second. It shows that challenging imaging applications, such as fingerprint verification, can become possible within a few tens of cubic inches, consuming a few watts of power if MOS technology is used. This is perhaps the best example to show how powerful a single chip MOS vision system can be.

Noise remains a fundamental problem which limits the development of MOS sensors and MOS vision systems. In fact, it is a limitation which hampers the huge potential application and market of MOS image sensors. The main emphasis has been on reducing the noise and improving the picture quality. The research work of our project is a contribution to this.

In the normal structure of MOS sensors (Figure 1.1 as well as Figure 2.6), the signal charges are usually read out through the sense line with large parasitic capacitance and amplified by an external charge sense amplifier. The requirements of this amplifier are daunting considering that wide dynamic range and high-speed must be achieved from a charge packet in the pixel which may be of the order of fC.

Accordingly a scheme was proposed in 1987 by Professor P. B. Denyer to overcome this problem [Denyer, 1989]. The novel feature of the scheme is the integration of analogue CMOS charge sensing amplifiers at the top of every bit line (Figure 1.2). The benefits are that these amplifiers need not work so quickly, since their activation frequency is equal to the line rate rather than the pixel rate; and they are situated as close as possible to the pixel array so the line capacitance is also reduced. The sense time can be as short as a few pixel clock periods so that smear noise is suppressed too. The common lines are then connected to bias voltage to prevent blooming. Their sole constraints are the need to achieve a good dynamic range and to be realised within the

pixel pitch (of the order of 10-20  $\mu\text{m}$ ).

A prototype was designed and fabricated in unmodified CMOS ASIC technology in 1987 [Suen, 1987]. It comprises a  $128 \times 128$  pixel array, and includes basic address, sense and amplification circuitry. The chip works from a single 5 volt power supply and a 1M Hz clock source, and delivers a sequentially-scanned, low-impedance analogue output of 1 volt peak-to-peak.

Actually, the design itself, as a final year student project, is very basic. Other than the top sense amplifier array and an output amplifier, there are no special considerations about reducing noise, even without protection to the analogue circuit and analogue signals. However, the image, captured by a frame grabber is surprisingly better than expected. The image signal has not been swamped by the noise, due to the on-chip amplifiers, even in the dark. This shows that with the amplifiers on the top of the array, the readout of the MOS sensor become easier. The main problem is still noise, especially fixed pattern noise. We learnt later that one source of the fixed pattern noise is from the sense amplifiers themselves. Process nonuniformity causes the mismatch of the amplifiers.

The idea to place amplifiers at each bit common signal line was also reported by Japanese researchers. Their first report was a device which combines a MOS pixel array and a horizontal bulk charge-transfer device (BCD) [Ando, 1985]. The device has noise suppression (RANS) cells on the top of each bit line, as shown in Figure 2.9. [Ozaki, 1991] proposed and analysed another scheme, close to ours, as shown in Figure 2.10. The paper expected this scheme to improve signal to random noise ratio, but fixed pattern noise will remain a problem. However, they didn't actually design and fabricate any such devices.

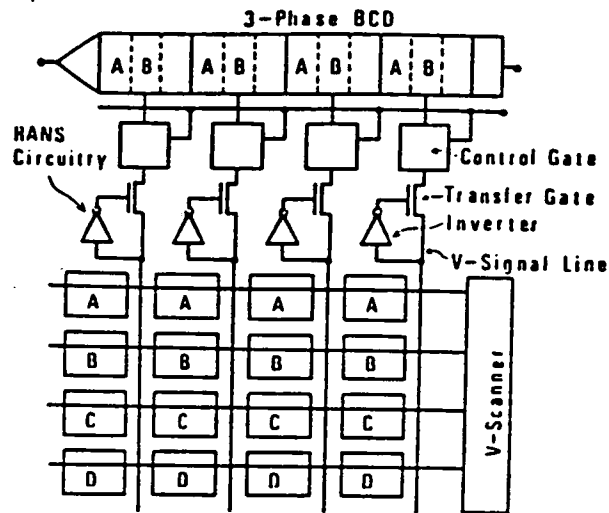


Figure 2.9 A device with a MOS array, a BCD, and RANS cells

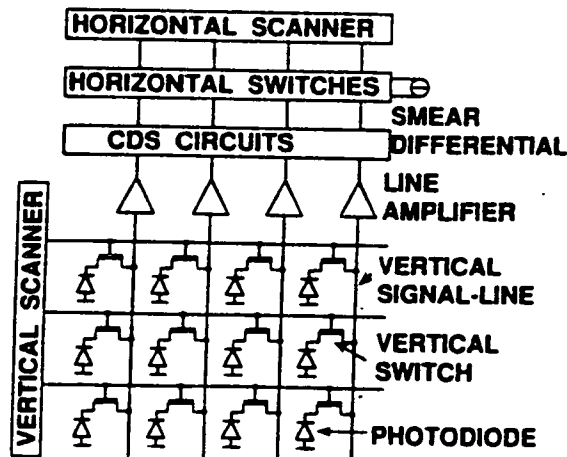


Figure 2.10 A device with line amplifiers on the top of the array

Fixed-pattern -noise is a common issue to photo array and analogue image storage circuits fabricated in unmodified ASIC process. [Franchi, 1992] reported a analogue frame buffer for early vision. The device has 6K analogue memory cells. The measurement result shows the main limiting factor to the higher precision is FPN induced by parameter mismatches, while the errors caused by different charge injection

and by charge decay during the retention time are not critical. This is in consistent with our results. A mismatch-compensation scheme was then developed.

## **2.5 Comparison between CCD, CID, and MOS image sensors**

Compared with other solid state image sensors, CCD sensors have been developed to the most advanced state. Today, CCD cameras are being widely used, mainly due to their low noise characteristics. However, CCD technology has the following disadvantages:

- Expensive production cost due to complicated fabrication process;
- Less flexibility of design compared with other types of sensors;
- Not compatible with standard VLSI process;
- Poor quantum efficiency and spectral response for multi-layer gate structures;
- CCD transfer path needs extra area, this become more severe for high resolution.

Of these disadvantages, high production cost and non-compatability with VLSI process are the most important. These explain why commercial CCD cameras are so expensive and so complicated.

On the other hand, MOS sensors have the advantage of

- cheap technology;
- compatible with standard VLSI process.

Therefore, smart vision application systems can be integrated only using MOS sensor arrays along with control logic and processing circuitry. With today's advanced MOS



technology, such system can achieve both high scale integration (near million devices) and low cost (about one pound per chip in mass production).

Other advantages are:

- small volume;
- low power consumption;
- single power supply (5 volt);
- simple pixel structure suitable for high resolution;
- design flexibility (custom pixel structure and custom readout scheme).

The main drawback of MOS sensors is high noise due to high video line capacitance and process nonuniformity. This has been hampering the development of MOS sensors.

CID sensors also suffer from

- Fixed pattern noise;
- High video line capacitance;

Other drawbacks of CID sensors include:

- Requires an epitaxial substrate, which is not compatible with standard VLSI processes;
- Loss of sensitivity due to absorption of photons by epitaxial layer;
- Poor spectral response due to absorption of long wavelength photons by polysilicon gates.

It seems that CID is the poorest technology for solid state image sensors because it has both main drawbacks of CCD and MOS sensors, i.e., not compatible with standard VLSI process and high noise. However, CID has its unique advantages:

- Flexibility of operation (with nondestructive readout mode);
- Random access readout;
- Low blooming due to epitaxial structure;
- Entire active area is sensitive to light;
- Opaque region between adjacent pixels is very small.

It is these merits that make CID sensors survive. In fact, CID sensors have their own market, focusing on achieving complete, accurate, and distortion-free image data acquisition for computer processing with fast, flexible timing and function control.

## 2.6 New photo-element structures

To realize future HDTV image sensors, other new photo-element structures are also being investigated since it is difficult to meet the more stringent requirements with present day techniques. There are several approaches which use photocells with a charge gain built into them in order to increase the light sensitivity when the size of the pixel sensing area is reduced [Yusa, 1986; Hynecek, 1988; Ogata, 1991; Matsumoto, 1991; Tanaka, 1989; Nakamura, 1991]. Here we look at some examples.

Figure 2.11 shows the cell structure of the device using a static induction transistor (SIT) [Yusa, 1986]. The n- epitaxial layer is grown on the n+ source substrate that acts as the SIT drain. A shallow n+ source region is formed on the epitaxial layer, so that the p+ gate region surrounds the source. An MOS capacitor is formed on the gate, and the gate pulse is applied through this capacitor. When the gate is reverse biased, a depletion layer forms outside the gate. If hole-electron pairs are generated by incident light in this region, electrons are swept away to the source or to the drain, while holes are stored on

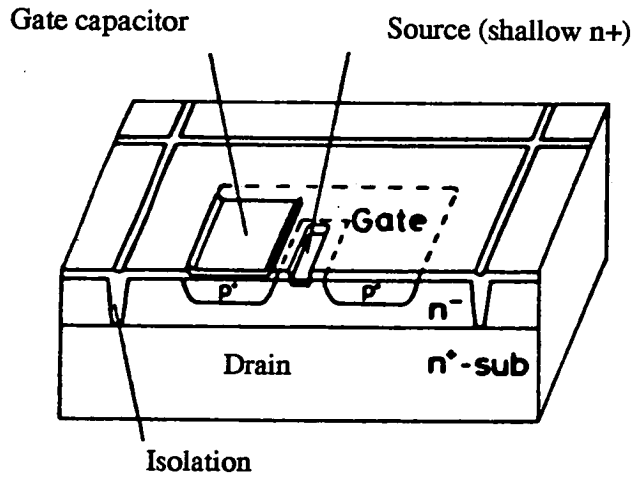


Figure 2.11 SIT structure

The drain-source current is modulated by this voltage change, and an amplified light-dependent signal is obtained. Image sensors consisting of  $170 \times 124$  pixels were fabricated using a combined SIT and MOS process. The signal current from the cell is 18 times larger than that of normal MOS cells having same pixel area. The main problem is nonuniformity. One primary cause is the lack of uniformity on the SIT  $I$ - $V$  characteristics. This produces nonuniformity of output offsets.

Figure 2.12 shows the cell structure of the device called floating gate array (FGA) [Hynecek, 1988]. The cell consists of a  $n$ -channel JFET connected as a source follower with its gate floating and capacitively coupled to an address line. The pull-down transistor in the diagram is common to a column of pixels. The function of this circuit can be understood from the output waveform shown in the diagram in Figure 2.12(b). An arbitrary pulse  $V_A$  presets the circuit and charges the capacitor  $C_O$ . The floating gate remains fully reverse biased if no light injected into it. On the other hand, if there is light, the photogenerated carriers partially discharge the capacitor and increase the potential of the gate. The source potential follows the gate potential and the waveforms corresponding to different light intensities can be observed, as shown in Figure 2.12(b). The photogenerated signal can then be obtained by measuring the output voltage

difference before and after the preset pulse. The layout shape of pixels is an equilateral hexagon with an enclosed gate and the source in the center. It holds promise for smaller cells and much larger arrays that are needed for future high-resolution image sensors. However, this structure still places strict requirements on the geometry tolerances and process parameter controls. The nonuniformity of a test device is around 2%.

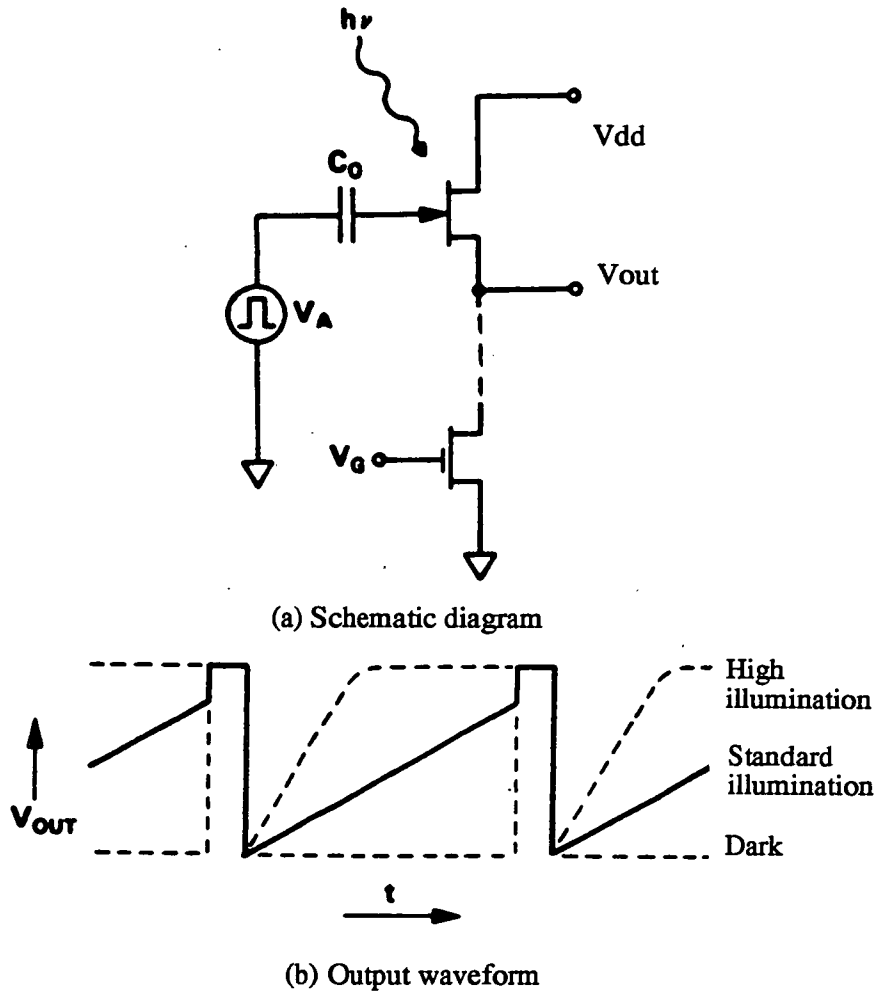
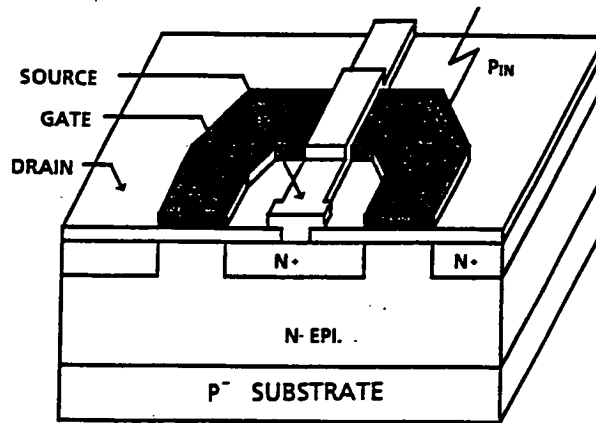


Figure 2.12 FGA structure

The cell structure for a charge modulation device (CMD) [Nalamura, 1986; Ogata, 1991; Matsumoto, 1991] is shown in Figure 2.13. The device is built on an n-type epitaxial layer which is on the top of p-type substrate. The gate electrode polycrystalline silicon is deposited and then patterned to an annular shape. The n+

source is inside the gate and the n+ drain is outside. The positively biased drain region between the pixels acts as an optical isolator. The gate electrodes are negatively biased with respect to both source and drain during charge collection periods, so that the surface of the semiconductor beneath the gate electrodes is depleted of carriers.



*Figure 2.13 CMD structure*

The p- substrate is also negatively biased, preventing the holes in the substrate from flowing to the surface. The incident light travels through the semi-transparent gate electrode structure and is absorbed in the Si bulk beneath the gate electrode. The holes generated near the surface drift to the Si/SiO<sub>2</sub> interface under the gate, where they are stored until removal by the image reset process. On the other hand, the holes, generated deeper down, drift to the p- substrate. The stored holes increase the surface potential, thus lowering the potential barrier height for electrons. Therefore, the electron current flows in accordance with the number of stored holes, and an amplified light-dependent current is obtained. When a positive bias is applied to the gate electrode, the stored holes are swept away to the p- substrate, resulting in the surface channel having a ready supply of electrons from the source region.

An experimental chip has been fabricated. The signal to noise ratio is limited by fixed pattern noise which originates mainly from exposure nonuniformity in the wafer

An experimental chip has been fabricated. The signal to noise ratio is limited by fixed pattern noise which originates mainly from exposure nonuniformity in the wafer fabrication process. The FPN in the dark is 5% of the saturation signal. The adjacent pixel nonuniformity is roughly 2%.

There is another pixel structure called base-stored image sensor (BASIS) [Tanaka, 1989; Nakamura, 1991]. The pixel is composed of an NPN bipolar transistor and a PMOS switch, as shown in Figure 2.14. The pixel is operated through the control gate of the switch. The pixel is first reset by applying a negative voltage to the gate of PMOS switch. The device is then off, isolating the base of bipolar transistors. The voltage level of base node of the bipolar transistor will be determined by the light intensity during storage operation when both base and emitter are floating. During readout operation, the emitter is connected to a load. The voltage of emitter will follow that of base because it now works as an emitter follower. In order to reduce fixed pattern noise, nonuniformities of bipolar parameters such as  $h_{FE}$  and  $C_{bc}$  should be made as small as possible.

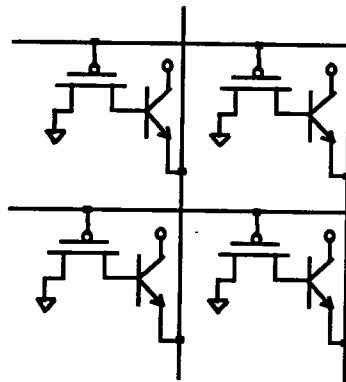


Figure 2.14 BASIS structure

These new structures all have achieved high gain built into pixels, and are thus affected less by noise originating from readout circuitry and are therefore expected to offer a high signal to noise ratio. However, nonuniformity of pixels causes fixed pattern noise, a common problem which requires solutions.

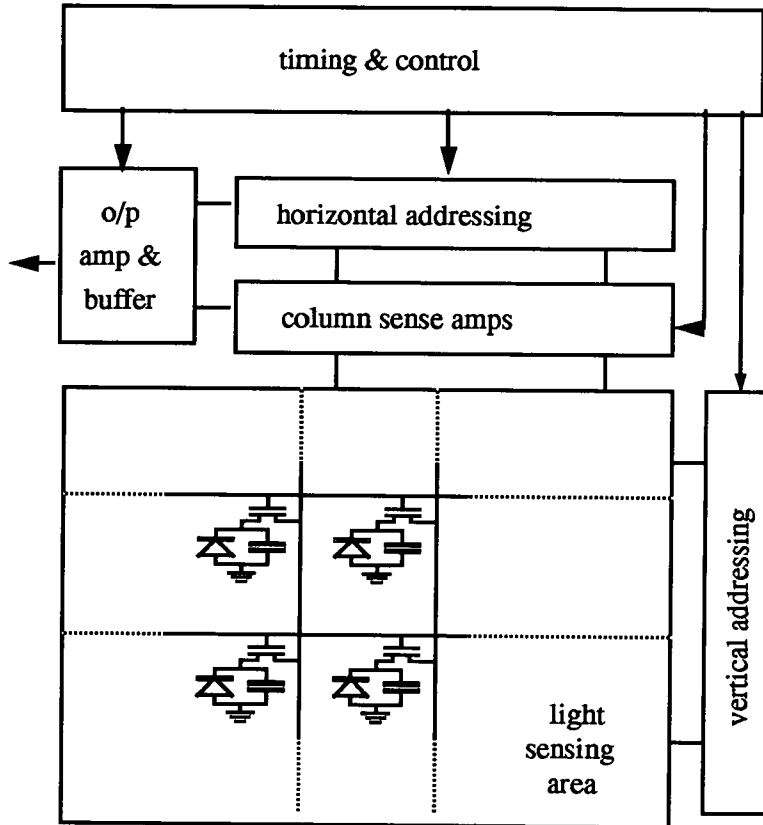
## **2.7 Chapter summary**

The evolution and present status of solid state image sensors have been reviewed. Three categories, CCD, CID, and MOS, have been covered with comparisons made between them. New photo-element structures aimed at future high definition television applications have also been described.

Although CCD image sensors have the most advanced development, MOS sensors have potential to implement smart vision application system with higher scales of integration and lower cost. This is an area worthy of further research efforts.

## Chapter3 BASIC ARCHITECTURE

The fundamentals and architecture of an array sensor suitable for CMOS implementation are introduced in this chapter. The pixel structure and the sensor array, the sense amplifier, the scan circuitry and the output amplifier and buffer are all covered.



*Figure 3.1 Basic architecture of MOS image sensors*

The basic architecture of the image sensor is shown in Figure 3.1. The light sensing area consists of a diode array matrix, schematically indicated by the columns and rows of individual photodiodes. The photodiodes are accessed on the basis of sequential selection of each row, along y-direction, through a vertical shift register. At the top of



each column is a sense amplifier. The sensed information is read out sequentially, along the x-direction, under control of a horizontal shift register. At the end of the signal amplification path there is an output amplifier and a buffer. The operation of these cells is coordinated by on-chip timing and control logic.

### 3.1 Sensor array

#### 3.1.1 Charge storage operation of the photodiode

One of the most significant developments leading to the realization of a practical solid state image sensor is the utilization of the p-n junction photodiode in an integrating or storage mode [Sze, 1981; Middelhoek, 1989; Haskard, 1988; Sequin, 1975]. Charge storage operation is based on the principle that, if a p-n junction is reverse biased and then isolated, the charge stored on the depletion layer capacitance decays at a rate proportional to the incident illumination level.

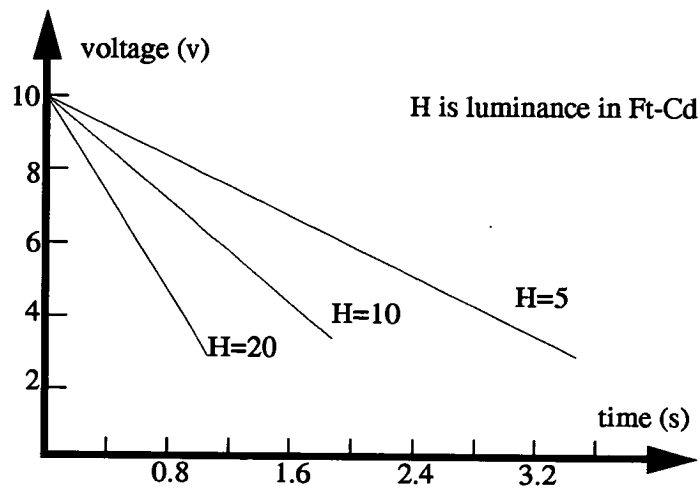


Figure 3.2 Voltage decay of an illuminated p-n junction

In the dark, only generation recombination current (dark current) is available to discharge the depletion layer capacitance; since both depletion layer capacitance and generation recombination current are directly proportional to area, the time constant is

independent of area. In the dark at room temperature, time constants of seconds may be attained for most standard MOS processes.

Figure 3.2 shows decay characteristics of a diode for several illumination levels [Tseng, 1985]. The photon-generated current is directly proportional to the illumination level and therefore the amount of charge removed in a given interval of time is directly proportional to the integral of illumination, taken over that interval. Thus, the final charge retained on the junction, after a fixed time interval, will represent the light intensity at that point of the image.

The charge storage operation mode has a few advantages.

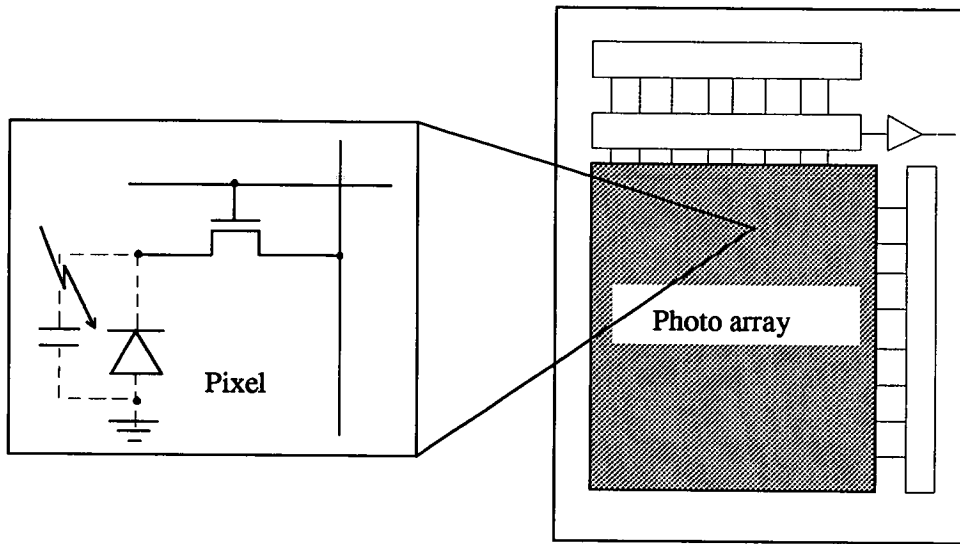
- The integration of the incident illumination results in improved sensitivity;
- Electronic exposure control can be implemented by varying the integration time.

In a standard ASIC CMOS process there are three possible photodetector device structures available: photoconductor, photodiode and photo-transistor. Factors affecting the choice of device include device area, response time, and gain. Photoconductors are unsuited to use in array sensor devices, due to large area and slow response time. Comparing photodiode with phototransistor, the photodiode has advantages of simpler structure, smaller area and faster response time. The phototransistor benefits from greater gain but its use in array device is complicated by inevitable device and operating condition variation. For these reasons the photodiode is the basic sensing element used in our designs.

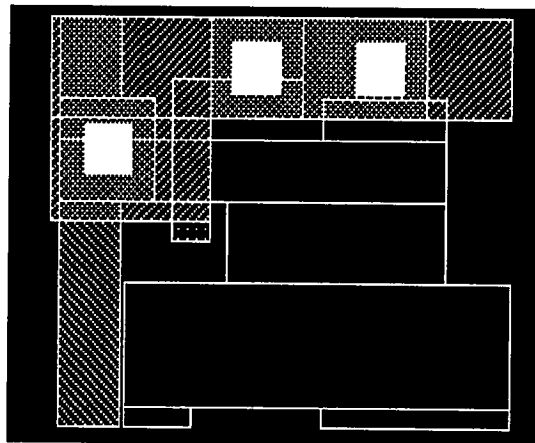
### 3.1.2 Pixel structure and operation

In common with others we use a photodiode array comprising MOS transistors, one per pixel, as shown in Figure 3.3. The photodiode is implemented by extending the source

region of the transistor. The layout of a pixel is shown in Figure 3.4.



*Figure 3.3 Pixel structure*



*Figure 3.4 Pixel layout*

In operation, the photodiode is reset to a voltage reference level  $V_{\text{ref}}$  by opening the MOS transistor gate. This stores a fixed charge package on the p-n junction capacitor of the source area of that transistor. The p-n junction is then isolated. The photocurrent,

produced by the effect of photons impinging on the diode, discharges the capacitor. The rate of discharge is proportional to the photocurrent, which is in turn proportional to the incident light level. The final charge retained on the capacitor, after a fixed time interval will represent the light intensity at that point of the image. The pixel is read by opening the gate, connecting the photodiode to the MOS transistor drain. All of the drains in each column are connected in common and only one row is read at any time.

## 3.2 Sense amplifiers

### 3.2.1 Structure and transfer function of sense amplifiers

Commonly, as stated in the first chapter, the column lines of the sensor array are gated through an analogue multiplexer to a single external charge sense amplifier(Figure1.1). The requirements of this amplifier are daunting considering that high-speed and wide dynamic range must be achieved from a charge packet in the pixel which may be of the order of  $fC$ .

A novel feature of our design is the integration of a sense amplifier at the top of every column line (Figure 1.2). These amplifiers need not work so quickly, since their activation frequency is equal to the line rate rather than the pixel rate and they are situated as close as possible to the pixel array. Their sole constraints are the need to achieve a good dynamic range and to be realised within the pixel pitch.

A charge integrator is used as a sense amplifier. Its function is analysed as follows with reference to Figure 3.5.

The capacitor  $C_{\text{line}}$  indicates the bit line capacitance, and capacitor  $C_{\text{pix}}$  indicates the photo-diode junction capacitance. The capacitor  $C_{\text{int}}$  is the integration capacitor.

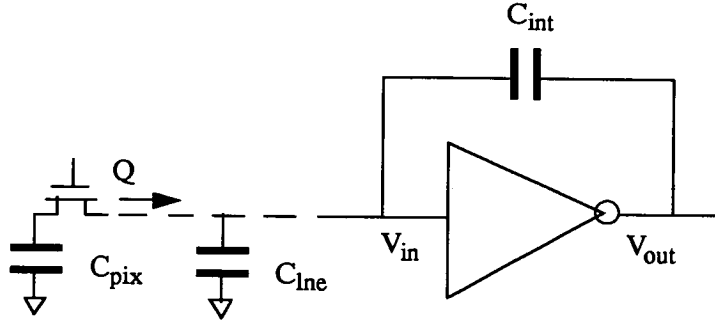


Figure 3.5 A charge integrator

Assume everything starts w.r.t. a notional zero and  $Q$  is the signal charge stored on  $C_{pix}$ . When a pixel is selected this charge  $Q$  is injected into the bit line and redistributed over capacitors  $C_{line}$ ,  $C_{pix}$ , and  $C_{int}$ . The equation describing the distributed charge is

$$V_{in} \times (C_{line} + C_{pix}) + (V_{in} - V_{out}) \times C_{int} = Q \quad \text{Eq(3.1)}$$

Using the equation for the gain of the inverter;

$$V_{out} = -A_v \times V_{in} \quad \text{Eq(3.2)}$$

to eliminate  $V_{in}$  and solving for  $V_{out}$  yield,

$$V_{out} = \frac{-Q}{C_{int} + \frac{C_{line} + C_{pix} + C_{int}}{A_v}} \quad \text{Eq(3.3)}$$

Assume  $C_{line}$  is much bigger than  $C_{pix} + C_{int}$ , then

$$V_{out} = \frac{-Q}{C_{int} + \frac{C_{line}}{A_v}} \quad \text{Eq(3.4)}$$

If  $A_v$  is high enough to make  $\frac{C_{le}}{A_v}$  much less than  $C_{int}$ , thus

$$V_{out} = \frac{-Q}{C_{int}} \quad \text{Eq(3.5)}$$

Furthermore, because  $Q = C_{pix} \times V_{pix}$  ( $V_{pix}$  is the voltage level remained on photo-diode), we get

$$V_{out} = \frac{-C_{pix} \times V_{pix}}{C_{int}} \quad \text{Eq(3.6)}$$

This equation shows that to first order the gain of ideal integrators is determined by the ratio of two capacitors.

### 3.2.2 High gain amplifier

High gain amplifiers are key elements to achieve good performance charge integrators. However, the realisation of such high gain amplifiers within a narrow pixel pitch presents an engineering challenge. CMOS inverters, the simplest possible amplifiers, have been chosen for this purpose.

It is known that the transfer characteristics of CMOS inverters, especially near the switching region, is largely depending on a second order effect, called channel-length modulation. Figure 3.6 shows the transfer characteristic of CMOS inverters. As a result, it is possible to obtain a linear high gain region providing the input of the inverter is restricted to the voltage value between  $V_1$  to  $V_2$ .

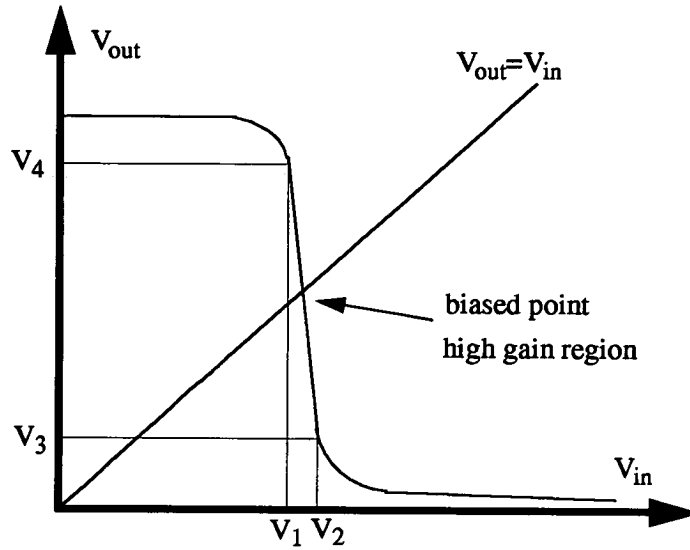


Figure 3.6 Transfer characteristic of CMOS inverters

This condition is ensured by self biasing the inverters, such that  $V_{out} = V_{in}$ , each time before photodiodes are to be sensed. The self biasing is implemented by turning on a transistor across the input and the output. This operation is called “balance”.

The balance enable signal for sense amplifiers is  $cv$ , which is the clock signal driving vertical shift register (see section 3.4: scanning circuitry).

### 3.2.3 Performance

Figure 3.7 shows the detailed diagram of the first sensing stage: from the pixel, through the sense amplifier, to the hold capacitor. The activation of sense amplifiers is coordinated with the vertical shift register, under the control of line clock  $cv$ . The sense amplifier balances when  $cv$  is high, and then samples a selected line. The voltage representation at the output is stored on a capacitor  $C_{hld}$ .

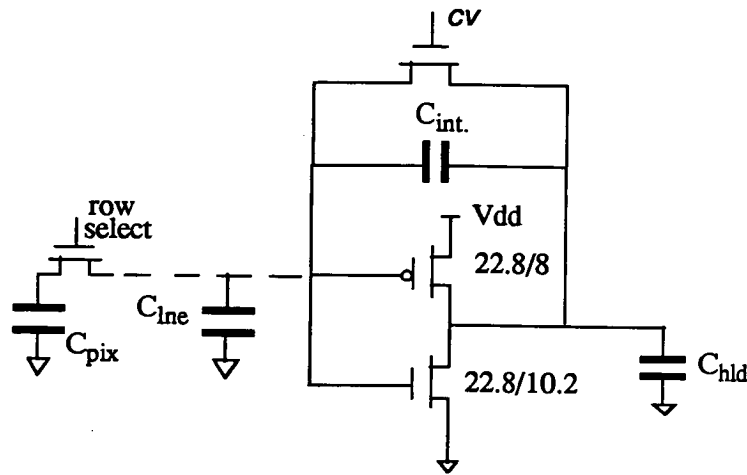


Figure 3.7 The first sensing stage

SPICE simulations have been carried out to optimize the performance of the sense amplifiers. The sense amplifier gives a low impedance 2 v analogue representation of the pixel charge. The sensing time is approximately 300 ns. Figure 3.8 shows the simulation results for both black and white light conditions.

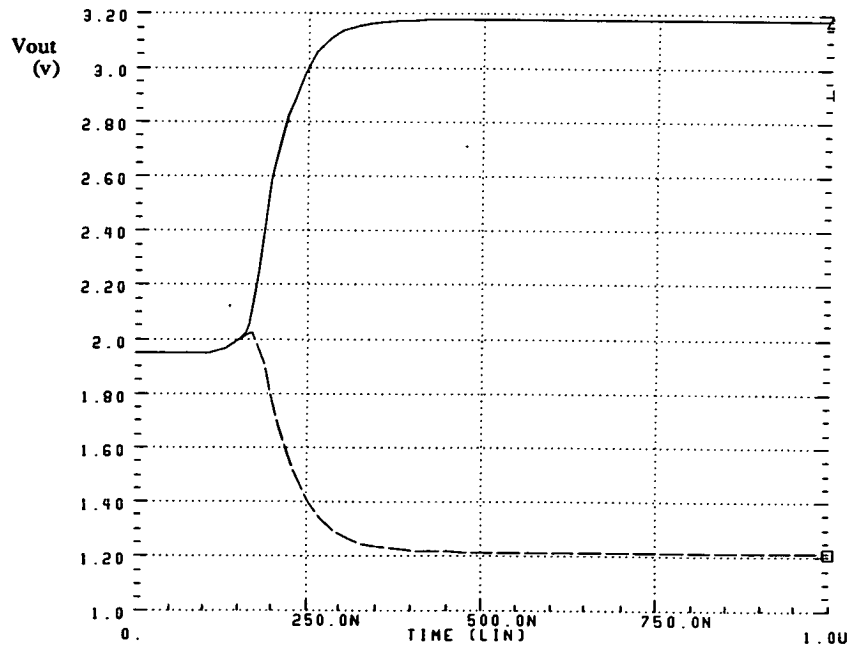


Figure 3.8 Simulation result of the first sensing stage



The single parameter of concern for this simple circuitry is the fixed pattern noise from mismatches between these amplifiers. This effect can be eliminated by implementing an offset compensating phase during idle period, which will be discussed in Section 4.2.

### 3.3 Output amplifier and buffer

#### 3.3.1 Output amplifier

The output amplifier has the same structure as sense amplifiers, shown in Figure 3.9, to implement the second stage of amplification. The difference is that the output amplifier needs bigger transistors (bigger width to length ratio) because it works at the pixel rate which is much faster than the line rate. Fortunately, there are no constraints on layout area, such as pixel pitch match. Secondly, there are no problems of matching multiple amplifiers, as all pixels are sequentially read out through the same output stage.

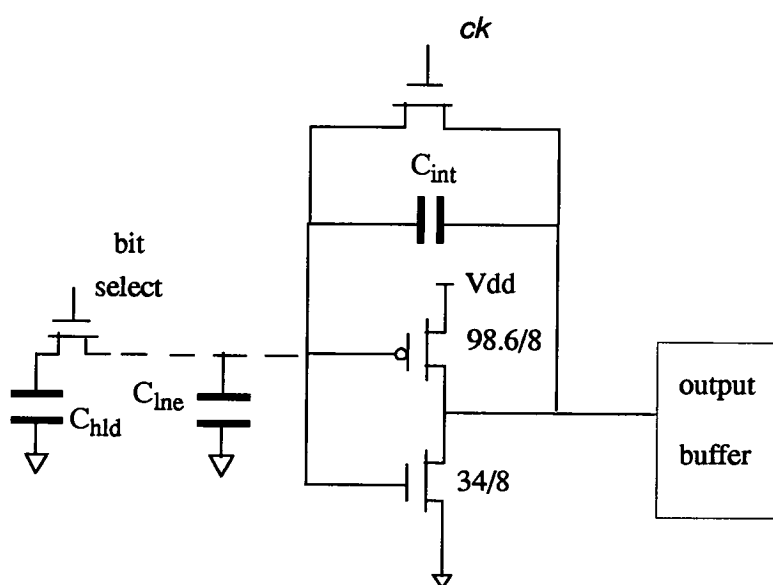


Figure 3.9 The second sensing stage

The balance enable signal for the output amplifier is  $ck$ , which is the clock signal driving horizontal shift register (see section 3.4: scanning circuitry).

Analysing the output amplifier in a similar manner to the column sense amplifier gives

$$V_{out} = \frac{-Q}{C_{int} + \frac{C_{ine} + C_{hld} + C_{int}}{A_v}} \quad \text{Eq(3.7)}$$

where,  $C_{hld}$  is a capacitor storing the signal amplified by the first sensing stage. If  $A_v$

is high enough to make  $\frac{C_{ine} + C_{hld} + C_{int}}{A_v}$  much less than  $C_{int}$ , thus

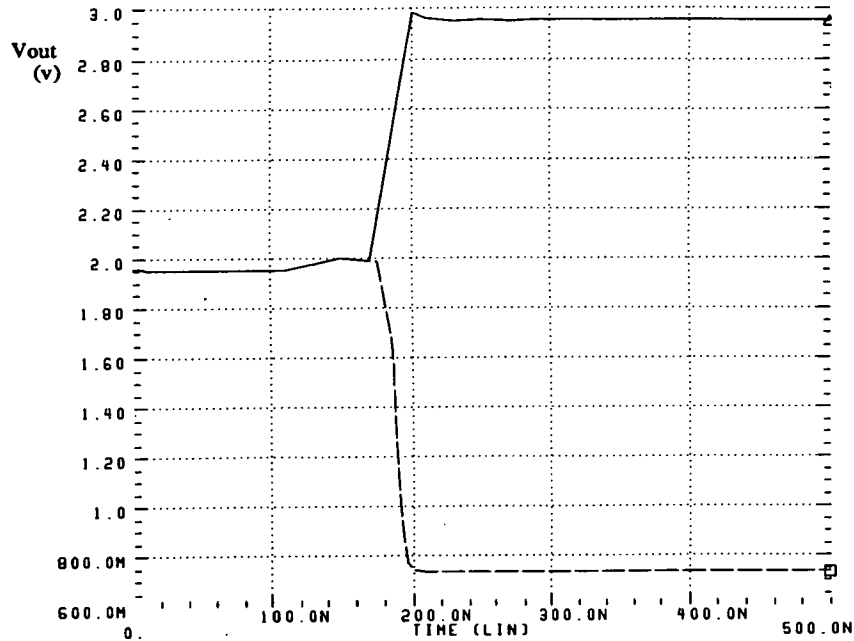
$$V_{out} = \frac{-Q}{C_{int}} \quad \text{Eq(3.8)}$$

Furthermore, because  $Q = C_{hld} \times V_{hld}$  ( $V_{hld}$  is the voltage level storing on the capacitor  $C_{hld}$ ), we get

$$V_{out} = \frac{-C_{hld} \times V_{hld}}{C_{int}} \quad \text{Eq(3.9)}$$

This shows that to first order the gain is determined by the ratio of two capacitors.

Figure 3.10 show the SPICE simulation results of output amplifier for both black and white light conditions. The sensing time is about 50 ns.



*Figure 3.10 Simulation result of the second sensing stage*

However, if the output amplifier directly drives a pad, the readout speed will deteriorate. Further more, the balance/amplification operation mode will result in thick vertical stripes, when displayed on a video monitor. Thus, an output buffer is needed to drive the output pad and implement sample/hold functions to improve picture quality.

### 3.3.2 Output buffer

Figure 3.11 shows an output buffer which has been implemented to improve the drive ability and picture quality. It works well at 6 MHz clock, making it possible to achieve a reasonable video rate readout. It has two sample/hold stages to get rid of vertical stripes arising from balance of the output amplifier.

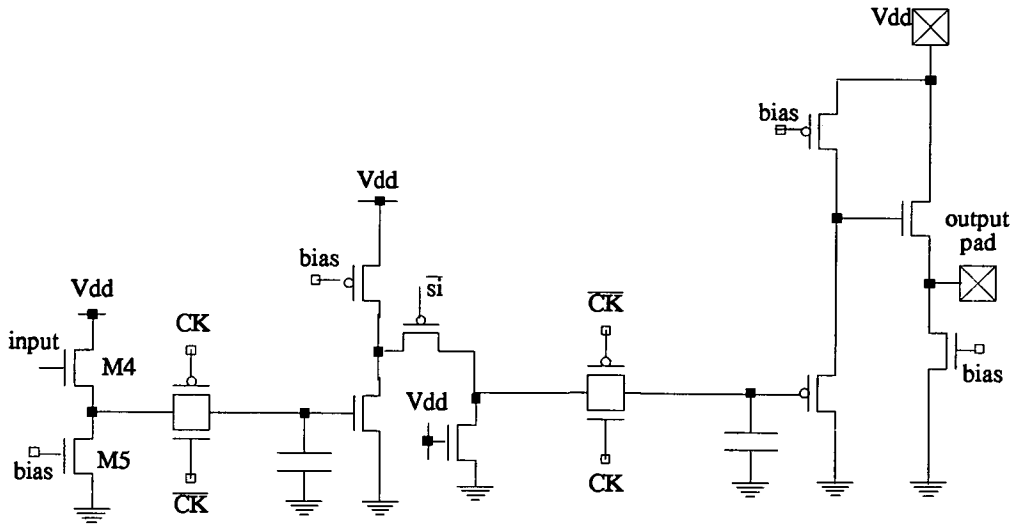


Figure 3.11 an output buffer

For applications requiring a composite video waveform it is relatively easy to format at this stage. Let us briefly review the format of composite TV signal (CCIR) [Grob, 1984; Bohlman, 1990]. It takes 25 frames a second. Each frame consists of 2 fields with a theoretically infinite horizontal resolution, and 312.5 lines per field vertically. Each field consists of a vertical retrace interval plus about 287 worthwhile lines of video data. Each line is composed of a sync signal, a blanking period, plus actual video. The vertical sync is a longer version of the horizontal signal. The sync, blanking, and video signals can be encoded in an analog voltage multiplexing scheme, as shown in Figure 3.12. Figure 3.13 shows the composite video waveform.

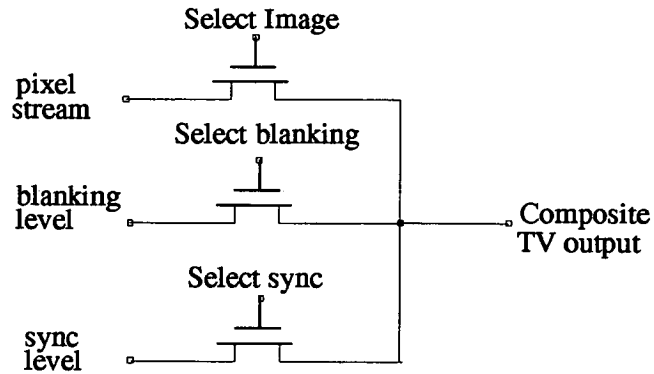


Figure 3.12 An multiplexer for formatting Composite TV output

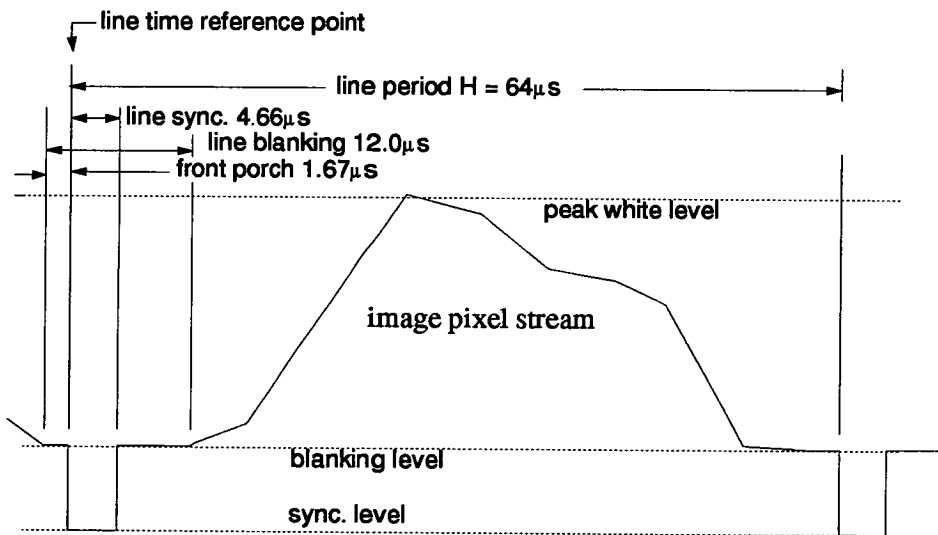


Figure 3.13 Composite video waveform (line level details)

### 3.4 Scanning circuitry

MOS sensors transfer the signal charges by multiplexing the photoarray, using digital

scanner, in the way similar to RAM readout. A vertical scanner selects one row at a time, transfers the diode charges into bit lines. The signal charges, amplified by the first stage and stored on the hold capacitor, are then gated through a multiplexer, controlled by a horizontal shift register, to the second sensing stage.

### 3.4.1 Horizontal register

Each register cell consists of a pair of transmission gates, which are controlled by clock  $ck$  and its inverse  $ckb$ , and two inverters as shown in Figure 3.14. The logic from the previous register  $n-1_{th}$  is injected to the  $n_{th}$  register and is stored on the gates of the first inverter, as  $ck$  goes high. When  $ck$  goes low again, this register immediately gives out the logic which has just been injected, through the two inverters, and thus accomplishes the shifting action.

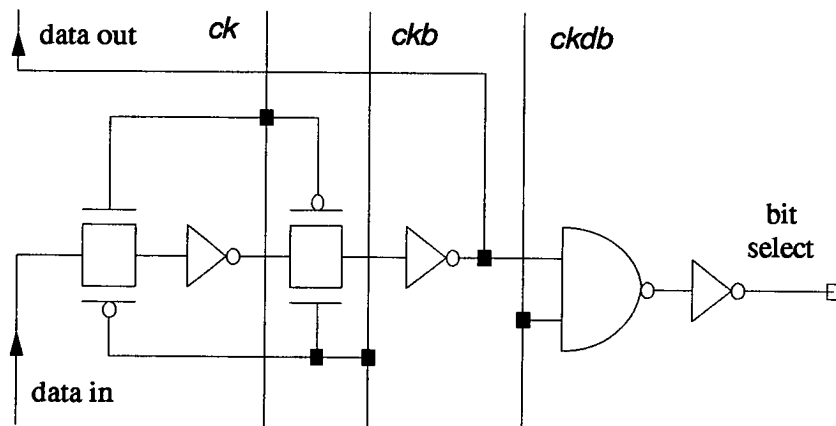


Figure 3.14 Horizontal Shift Register Cell

As only a single data value can be fed to the output amplifier from the sense amplifiers at one time, the shift register must give only one logic “high” at one of the outputs of the cells, during the reading processes.

A race problem may occur between the output amplifier and one of the switch transistors opened by the horizontal shift register. The output amplifier works in balance phase when  $ck$  goes high, and then in amplification phase when  $ck$  goes low.



Signal charge will be lost if a switch transistor turns on a little earlier than the balance phase ends.

To eliminate this problem, the horizontal register cell is modified to ensure that the switch opens a few nano seconds later than the balance of the output amplifier. A clock signal called *ckdb* is used to achieve this delay, as shown in Figure 3.15.

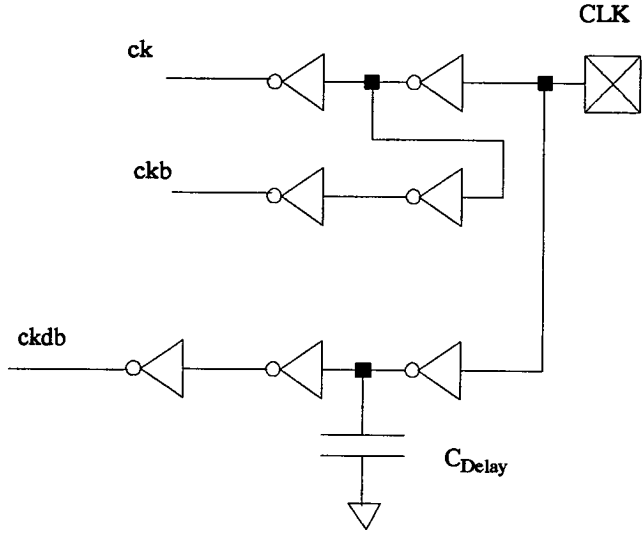


Figure 3.15 A Circuit Generating *ck*, *ckb*, and *ckdb*

### 3.4.2 Vertical shift register

The vertical shift register works at much slower frequency than the horizontal one. A simple dynamic CMOS shift register may not be sufficient to retain the correct logic during the prolonged clock period. A static shift register may be required. This will consume larger area.

Figure 3.16 shows a “semi-static” structure. Similar to the operation of the horizontal shift register, the logic signal from the  $m-1_{th}$  stage is injected to the  $m_{th}$  stage and is then stored on the gate of an inverter, at the time when *cv* is high. It passes the logic to the end of the stage when *cv* goes low. Note that an introduced feedback loop is also

turned on to reinforce the logic signal, no matter how long  $cv$  is low.

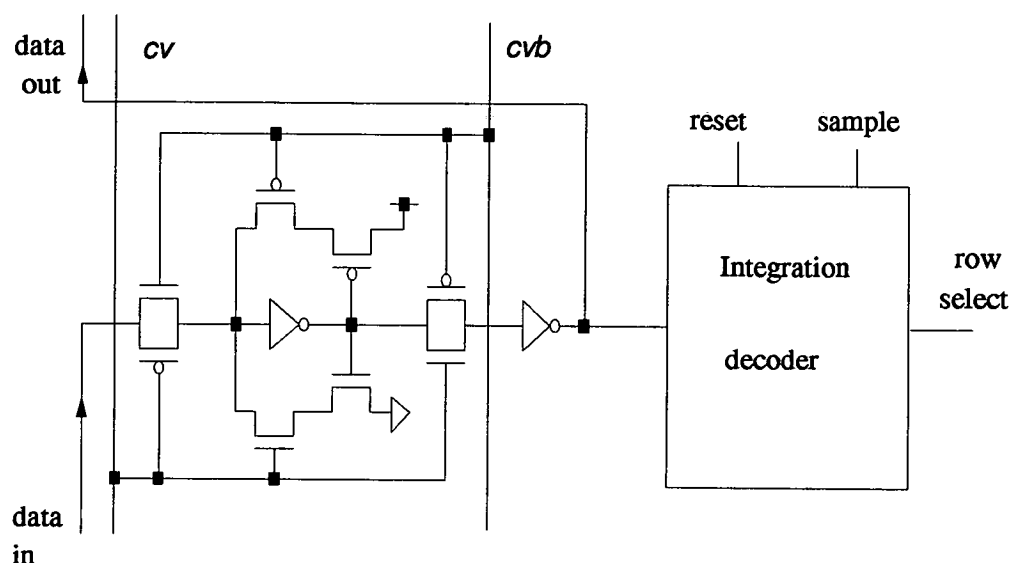


Figure 3.16 Vertical Shift Register Cell

On chip automatic exposure control requires a decode cell which is attached to each register cell. This will be discussed in Chapter 5.

### 3.5 Control logic

The elements described above must be driven by control logic. Our technique provides the feasibility of designing a self-contained, single chip integrated system, which requires minimal components for its operation.

For a single chip video camera, approximately 2,600 gate logic is required to implement digital control. Half is used to generate synchronisation timing, including line-sync and frame-sync signals to format a standard composite video output. The other half is to control the exposure and the gain.

The design of control logic has been the responsibility of another researcher and will



not be covered in this thesis.

### **3.6 Chapter summary**

The basic architecture of an MOS image sensor has been described. The operation of each cell has been discussed. These cell circuits are all suitable for CMOS ASIC implementation.

The photodiode comprises an MOS transistor which is implemented by extending the source region of the transistor.

The sense amplifier is implemented by employing a charge integrator, which consists of a high gain inverter and an integration capacitor. To ensure the inverter works in the linear high gain region, the inverter is self biased prior to sensing such that  $V_{\text{out}} = V_{\text{in}}$ . The single parameter of concern for this simple circuit is fixed pattern noise which arises from mismatches between these amplifiers. This is the topic of the next chapter.

In addition to the basic structure described in this chapter, more enhanced functions will be discussed in the following chapters.

## Chapter 4 NOISE ANALYSIS, NOISE ELIMINATION AND COMPENSATION

### 4.1 Introduction

Apart from the expected integrated signal charge which is in proportional to the incident light intensity, the output signal has superimposed on it dark current and other noise. The dark current is negligible at room temperature for current MOS technology [Denyer, 1990] but the other noise sources are not. In fact, MOS technology is more prone to noise than CCD technology.

The noise of MOS sensors can be classified as random noise and fixed pattern noise. The random noise is non-repetitive fluctuations of electrons, due to the fact that electrical charge is not continuous but is carried in discrete amounts equal to the charge of an electron. The noise manifests itself by representing a lower limit below which electrical signals cannot be amplified without significant deterioration in the quality of the signal.

Fixed pattern noise (FPN) appears as a constant interference superimposed on the image. The causes of FPN are mainly non-uniformity of processes and coupling of digital pattern onto analogue power supply and signal path. In theory, it can be removed by signal processing, such as extracting the fixed pattern from every field of picture. However, this method is complicated and expensive.

This chapter analyses various sources of noise and highlights the main ones. It then discusses techniques to eliminate and compensate for these main sources.

### 4.2 Random noise

Based on the circuitry described in the last chapter, the primary charge sensing path from the photo diode to the output pad can be divided into three stages. The first stage

is from the pixel, through the sense amplifier, to the hold capacitor. The second stage is from the hold capacitor to the output amplifier. The third stage is from the output buffer to the pad. So far as noise analysis is concerned, the third stage is less important because the charge signal has been amplified before reaching this stage. The amount of noise in this stage is less than in previous stages.

#### 4.2.1 First sensing stage

Figure 4.1 shows the random noise analysis diagram for this stage. The noise sources of this stage are: the pixel noise, the bit line noise, and the inverter noise. Each noise source is analysed as follows.

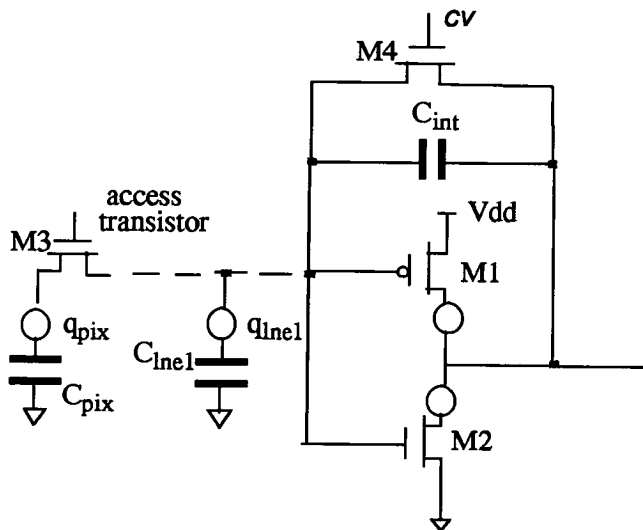


Figure 4.1 noise analysis diagram of the first sensing stage

##### Pixel noise and bit line noise

The noise on the pixel and bit line is called *Johnson noise*, which is relevant to the storage of charge in capacitors [Hobson 1978]. The fluctuation in the stored energy of a capacitor is given by

$$\frac{1}{2} \kappa T = \frac{1}{2} C \Delta V^2 \quad \text{Eq (4.1)}$$

where  $\kappa$  is Boltzman's constant,  $T$  is absolute temperature.

The fluctuations cause a voltage fluctuation at the capacitor terminals which is given by

$$\Delta V^2 = \frac{\kappa T}{C} \quad \text{Eq (4.2)}$$

When the capacitor is connected to other circuitry so that charge flow can occur, there is a charge fluctuation given by

$$\Delta q^2 = \kappa T C \quad \text{Eq (4.3)}$$

This fluctuation process is often known as “kTC noise”.

The rms value  $q_{\text{pix}}$  of the noise charge on the pixel capacitor  $C_{\text{pix}}$  is

$$q_{\text{pix}} = \sqrt{\kappa T C_{\text{pix}}} \quad \text{Eq (4.4)}$$

Pixel noise is directly additive to the signal charge  $Q$  which has the maximum value of

$$Q = C_{\text{pix}} \times V_{\text{reset}} \quad \text{Eq (4.5)}$$

where  $V_{\text{reset}}$  is pixel reset voltage.

Therefore, the signal to noise ratio on the pixel is

$$\frac{Q}{N} = V_{\text{reset}} \times \sqrt{\frac{C_{\text{pix}}}{\kappa T}} \quad \text{Eq (4.6)}$$

For  $C_{\text{pix}} = 0.03 \text{ pF}$ ,  $V_{\text{reset}} = 2.8 \text{ V}$ , the signal to noise ratio is about 77 dB.

However, when signal  $Q$  is switched into the bit line, much bigger bit line capacitance noise will directly add to the signal charge.

The noise on the bit line capacitance is

$$q_{\text{line1}} = \sqrt{\kappa T C_{\text{line1}}} \quad \text{Eq (4.7)}$$

where  $C_{\text{line1}}$  is bit line capacitance.

The bit line capacitance consists of all drain diffusion capacitance of the switch transistors connected to one column line, plus metal wire capacitance. It is proportional to the number of lines. When the signal  $Q$  on a pixel is switched into the bit line, the signal to noise ratio is reduced to

$$\frac{Q}{N} = \frac{V_{\text{reset}} \times C_{\text{pix}}}{\sqrt{\kappa T C_{\text{line1}}}} \quad \text{Eq (4.8)}$$

$C_{\text{line1}}$  is roughly 2.5 pF for a 300 line array. Thus the signal to noise ratio is 58dB.

### Inverter Noise

The inverter has two MOS transistors which generate noise, including thermal noise in the channel and additional flicker noise which is peculiar to MOS devices. With the type of switch-stabilized operation practised in these circuits (as described in section 3.2.2), the majority of flicker noise is cancelled.

The thermal channel noise for devices in saturation is approximately equivalent to that generated by a conductor of value equal to the transconductance of the saturated device (Cobbold, 1970);

$$g_m = \frac{2I_D}{V_{gs} - V_T} \quad \text{Eq (4.9)}$$

The transconductance of M2 is  $139 \mu\text{A}/\text{V}^2$ , so  $R_{\text{on}} = 7.2 \text{ k}$ , giving output noise voltage



The maximum signal charge on the hold capacitor is

$$Q = C_{\text{hld}} \times V_{\text{hld}} \quad \text{Eq (4.11)}$$

where  $V_{\text{hld}}$  is the maximum voltage of the signal storing on the capacitor.

Therefore, the signal to noise ratio referring to the hold capacitor is

$$\frac{Q}{N} = V_{\text{hld}} \sqrt{\frac{C_{\text{hld}}}{\kappa T}} \quad \text{Eq (4.12)}$$

For  $C_{\text{hld}}=0.16\text{pF}$ ,  $V_{\text{hld}} = 1.8\text{V}$ , the signal to noise ratio here is about 81 dB.

However, when signal  $Q$  is switched into the horizontal line, much bigger line reset noise will directly add to the signal charge. This noise is

$$N_{\text{line2}} = \sqrt{\kappa T C_{\text{line2}}} \quad \text{Eq (4.13)}$$

where  $C_{\text{line2}}$  here is the horizontal line capacitance. It consists of all diffusion capacitance of switch transistors, plus metal wire capacitance. It is proportional to the number of pixels. The signal to noise ratio is reduced to

$$\frac{Q}{N} = \frac{V_{\text{hld}} \times C_{\text{hld}}}{\sqrt{\kappa T C_{\text{line2}}}} \quad \text{Eq (4.14)}$$

$C_{\text{line2}}$  is roughly 2.5 pF for a 300 pixel array. Thus the signal to noise ratio is only 69 dB.

### Inverter noise

The inverter of the output stage has much bigger W/L ratio than that of the first stage (refer to the section 3.3.1). Therefore, the thermal noise of M5 and M6 is lower than that of M1 and M2 of the first stage. This noise is obviously negligible.

### 4.2.3 Dominant random noise

The dominant random noise source is the bit line capacitance noise. The horizontal line capacitance is about equal to the bit line capacitance, but the KTC noise is not dominant because the signal has been amplified by the first sensing stage. The horizontal line capacitance noise can become more important if horizontal resolution is much higher than vertical resolution and/or the gain of the first stage is not big enough.

It should be pointed out that the bit line capacitance noise could be much bigger if the sense amplifiers were not directly on the top of pixel array. The line capacitance could be as large as 20 PF, or even bigger, for a sum of bit line capacitance, horizontal line capacitance, and pad capacitance. The signal to noise ratio in that case will degenerate to less than 49 dB. This is the reason why MOS technology was concluded to have high line capacitance and high KTC noise. This conclusion has to be changed in the case of our new scheme. Here we see the significance of sense amplifiers at the top of pixel array.

The line KTC noise is proportional to the resolution. The ultimate lower limit on detectable light intensity is set by these noise sources.

## 4.3 Fixed Pattern Noise

Another class of noise is fixed pattern noise which is due to the parameter mismatch from cell to cell and the interference from digital circuitry coupling to the analogue circuitry. There are many potential sources of FPN. Figure 4.3 provides a circuit diagram of the analogue path with FPN sources indicated.



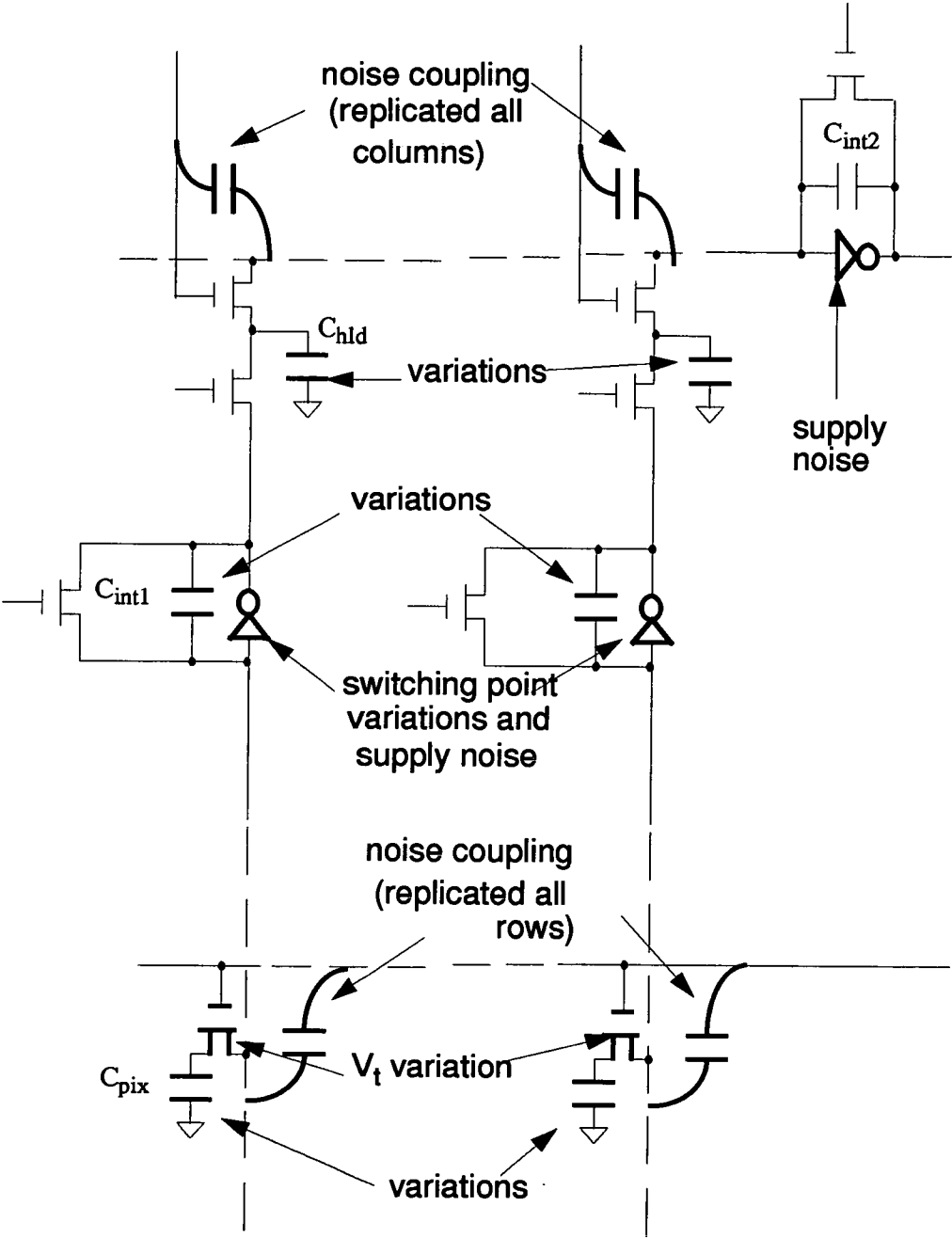


Figure 4.3 Noise analysis diagram of fixed pattern noise

### 4.3.1 Parameter mismatch

Ideally, all pixels should be exactly the same. We also expect all sense amplifier cells behave the same. However, there are differences among them.

#### Pixel Reset Offsets

Random offsets in pixels can be caused by threshold variations in the access transistors. The variation is of the order of 100 to 200 mV on ES2 1.5 micron e-beam written wafers.

Normally, pixels are precharged to  $V_{dd}$  during the reset procedure. The actual voltage value written to pixels is

$$V_{rst} = v_{dd} - V_T \quad \text{Eq (4.15)}$$

where,  $V_T$  is a threshold voltage of each access transistor.

The actual reset voltage to each pixel has the same order of variation as that of threshold voltage, that is:

$$\Delta V_{rst} = \Delta V_T \quad \text{Eq (4.16)}$$

Therefore, 200 mv variation may exist among pixels. This figure is too large compared with the maximum signal voltage which is about 3.0 volt. The signal to noise ratio is only 23.5 dB. Without compensation, this variation of the pixel reset voltage will cause obvious speckles on the screen of monitors. We have noticed this effect for a prototype (ASIS-1020).

#### Column Sense Amplifier Offsets

The column sense amplifiers derive a reference point for their operation by resetting such that  $V_{out} = V_{in}$ . We call this action as *balance*.

Considering the open-loop transfer function of the inverter, this relationship forces the

operating point for  $V_{in}$  to lie at the high-gain portion of the inverters open loop characteristic (Figure 3.6). This is ideal for automatically setting the correct operating point, but the balance voltage will vary due to threshold and transconductance mismatch.

To simplify the argument here, only the threshold variation is considered and only the effect of balance voltage difference is concerned, there will be up to 200 mv offset at the first sensing stage. The maximum signal amplitude of this stage is about 1.8 volt, giving the signal to noise ratio of only 19 dB.

SPICE simulation has been carried out to calculate the balance voltage for different threshold voltage values. The result is given in the following table.

Table 1: Balance level for different  $V_T$  without compensation

$V_{TN}$	$V_{TP}$	Balance level
<b>0.85</b>	<b>-1.07</b>	<b>1.9513</b>
0.75	-0.97	1.9191
0.75	-1.17	1.8519
0.95	-1.17	1.9832
0.95	-0.97	2.0501

Because this variation is repeated by lines, severe vertical stripes will appear on the output. We have noticed this effect for a prototype, named ASIS-1020 and the test of this chip has confirmed the fixed pattern noise is up to 10-20%.

### Other variations

Other possible variations can be pixel capacitance variation and hold capacitor variation. These variations may be caused by technology non-uniformity such as geometry non-uniformity and process non-uniformity.

### 4.3.2 Digital pattern interference

Our sensor includes both digital logic and analogue sensor array on the same substrate. Digital breakthrough onto the analogue output is an important problem.

#### Supply-bourne noise

In principle, supply-bourne noise may affect the column sense amplifiers. As these work synchronously, any effects will show up as row offsets. Theoretically the PSRR is only 6dB at this point.

Similarly, supply-bourne noise will also affect the output amplifier and output buffer. Effects will mainly show up as pixel offsets and repeat on lines.

#### Bit-line Breakthrough

Another implicit FPN source is the coupling of noise on the word lines onto the bit lines.

Because all word lines cross each bit-line, a small coupling capacitance at each pixel becomes a large overall effect if the noise is identical in each word line, as shown in Figure 4.4. Because of the parallel nature of the bit-lines and their operation any such noise will be row-oriented. Any breakthrough can have an effect if it occurs at critical moments such as *balance*, *sample*, and *reset*. Although this is a very short interval and efforts should be made to ensure that the supplies are “quiet” at this time, as far as possible.

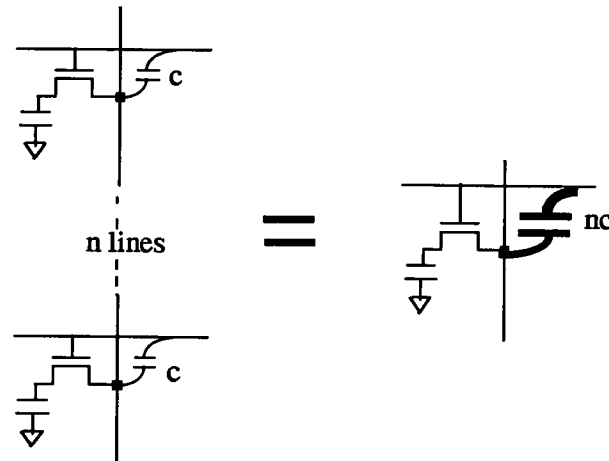


Figure 4.4 Bit line breakthrough

### Output Line Breakthrough

As with bit-line breakthrough, the long line to the output amplifier is coupled at every column to a set of sampling gate signals. If these contain (digital induced) noise, and such noise is not stationary between the end of *balance* and the end of *read* then the multiply-coupled noise will be represented in the output stream.

This stage operates at the pixel rate, so the noise may appear randomly; however any component coming from pixel-level counters may be repeated in each line and therefore lead to apparent vertical striping.

### 4.3.3 Main sources of FPN

Based on the above analysis and the test of prototypes, we have noticed that fixed pattern noise is mainly from two sources: threshold variations in the MOS pixel access transistors causing speckles, and mismatches between the column sense amplifiers causing vertical stripes. Without compensation these effects can have an rms value up to around 20% of saturation. This figure is certainly too big.

Analogue supply noise is also noticeable. The main interference is from the digital counter, causing vertical stripes repeated in the periods of  $2^N$  of pixels. The analogue power supply is effected by digital counters probably through substrate coupling.

## **4.4 Reducing fixed pattern noise**

The fixed pattern noise is the first problem to be solved, or else our new scheme is useless.

### **4.4.1 Eliminating speckles caused by access transistors**

The speckles caused by the threshold variation of access transistors can be eliminated by letting the access devices work in the linear region. In that way, the actual reset voltage will be independent of the gate potential and threshold.

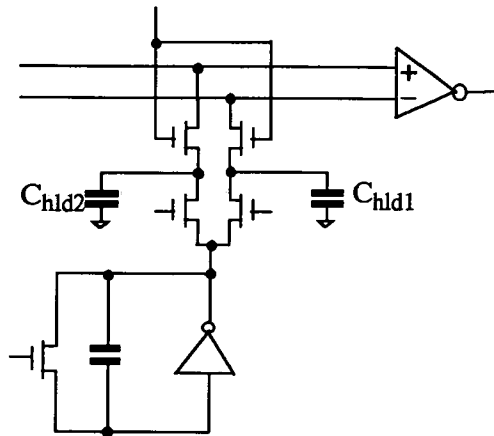
To achieve this, we reduce the reset voltage so that it is more than  $V_T$  below the gate potential of access transistors. Therefore, no speckles appear.

### **4.4.2 Compensating vertical stripes**

The vertical stripes can be compensated by recording the pattern, and then subtracting it from the signals. There are several methods to achieve this.

#### **Scheme 1**

An extra load capacitor can be added for each bit in the first sensing stage, as shown in Figure 4.5. The mismatch among sense amplifiers will be stored in this capacitor and will be subtracted from the signals in the second sensing stage.



*Figure 4.5 Compensation scheme1*

The operation will be:

- phase 1: dummy sensing of a line, probably a black line, to record the variation on  $C_{hld2}$ ;
- phase 2: normal sensing of a line, storing in  $C_{hld1}$ ;
- phase 3: horizontal scan, the variation is subtracted.

## Scheme 2

The compensation can be implemented in the output stage. The stream of a particular line (probably a black line) of the pixels will be compared with a reference level. The difference will be recorded in the storing elements (storing capacitor, register, or RAM cell et. al.), and then fed back to the amplifiers.

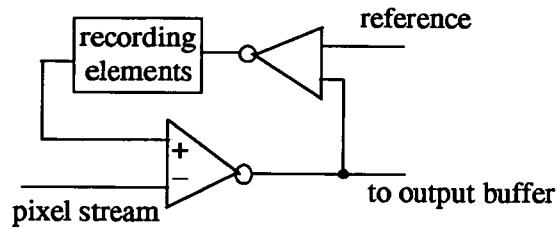


Figure 4.6 Compensation scheme2

In this scheme, all sorts of the line patterns, from the sensor array to the second sensing stage, can be compensated. This scheme also allows the black signal level to be calibrated to the reference level so that the amplification path is offset free.

The operation will be:

- phase1: a black line is sensed by the first sensing stage;
- phase2: this line is scanned out through the second sensing stage. The black signal of each pixel is compared with a reference and the difference is stored;
- phase3: normal lines are sensed and scanned, and the stored pattern is subtracted.

### Scheme 3

Instead of recording the pattern, another method is to calibrate the sense amplifiers themselves so that the balance voltage is insensitive to the variation of threshold voltage. This is achieved by adjusting the switch threshold of sense amplifiers to be close to an externally giving voltage. The scheme is discussed in detail in the following section.



### 4.4.3 Sense amplifier calibration

A circuit is shown in Figure 4.7 for the case of an arbitrary inverter. Please note that an n-channel MOS transistor is connected in series with the Gnd power connection of the inverter. The drain voltage  $V_y$  of this transistor effectively becomes the new ground voltage reference for the inverter. Accordingly, the transfer characteristic of the inverter is dependent upon  $V_y$  and generally the switching threshold will vary in some proportionate relationship to  $V_y$ , as shown in Figure 4.8. Now  $V_y$  is determined by the inverter supply current and the channel resistance of M1. The channel resistance of M1 is in turn determined by  $V_x$ . Therefore the switching threshold of the inverter can be controlled and adjusted by varying the gate voltage on transistor M1.

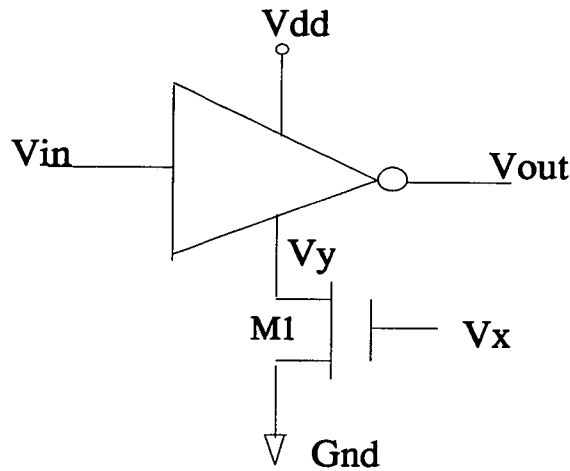


Figure 4.7 inverter threshold compensation circuitry

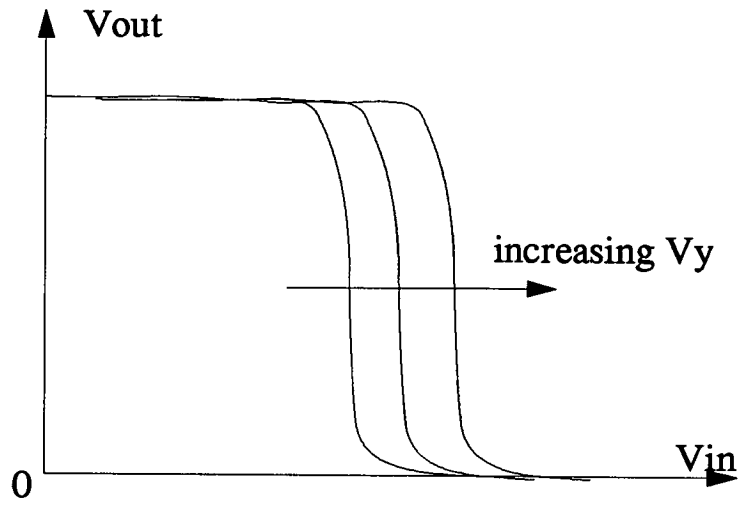


Figure 4.8 transfer characteristic of the inverter

To achieve automatic adjustment of the inverting amplifier switching threshold to approach a given reference voltage, an external reference voltage  $V_{cl}$  is supplied to the inverter input as shown in Figure 4.9.

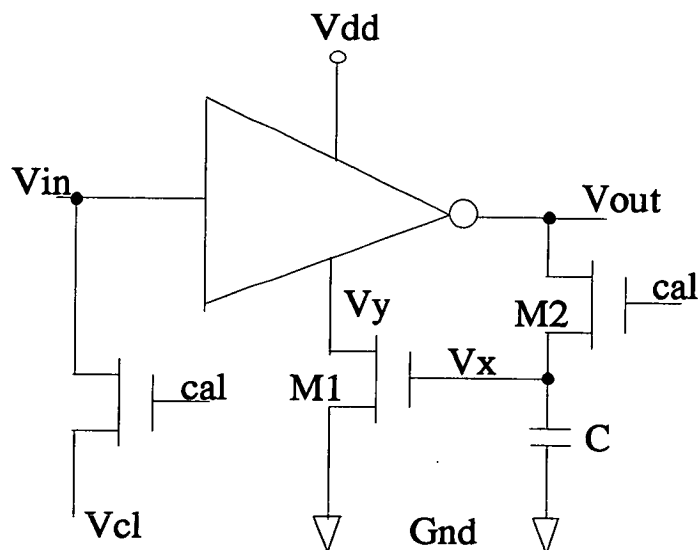
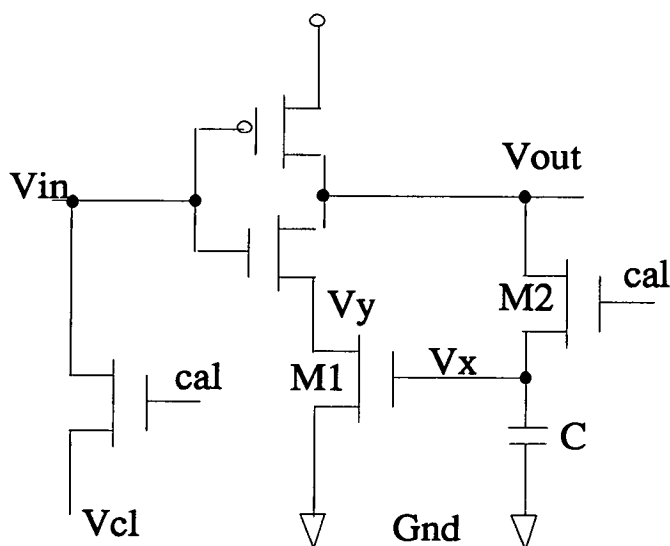


Figure 4.9 automatic adjustment of switching threshold

At the same time transistor M2 is enabled thereby connecting the gate of M1 to the inverter output. This is a configuration of negative feedback and for suitable design values the circuit will settle to a stable value of  $V_x$ . It is possible to further select design values such that the value of  $V_x$  will normally lie within the high gain portion of the inverter transfer characteristic. Under this circumstance therefore the circuit has automatically adjusted  $V_x$  such that the switching threshold is achieved at an inverter input voltage of  $V_{cl}$ . this is the desired operating point. Once this condition has been reached M2 may be turned off, thereby breaking the feedback loop but leaving the correctly adjusted value of  $V_x$  held on capacitor C. The inverter may now be used in its normal capacity and will exhibit a switching threshold approximately equal to the programmed value  $V_{cl}$ .



*Figure 4.10 a inverter with automatic threshold compensation*

SPICE simulation has been carried out to verify this scheme. The results are given in the following table. Please compare with the table 4.1, where the balance difference is nearly 200 mv. After calibration, the balance voltage difference is 4 mv. The signal to noise ratio is increased to 53db.

Table 2: Balance level for different  $V_T$  with compensation

$V_{TN}$	$V_{TP}$	Balance level
<b>0.85</b>	<b>-1.07</b>	<b>2.4077</b>
0.75	-0.97	2.4077
0.75	-1.17	2.4119
0.95	-1.17	2.4077
0.95	-0.97	2.4080

The calibration is not ideal because of second order effects, such as non-infinite inverter gain, which limit the accuracy of the adjusted switching threshold.

#### 4.4.4 Reducing interference between digital and analogue circuitry

In order to minimize interference from the digital parts, complete guard rings are put around all analogue parts, and double guard rings around the array. Routing is arranged with priority to analogue output and analogue power supplies. Separate analogue power rails are used and kept as “clean” as possible. Choosing twin-tub technology will further help to eliminate the interference from digital circuitry to analogue part.

To eliminate the breakthrough through bit-lines and horizontal lines, the word-line drivers and the bit select drivers should have clean power supplies. It is possible to either provide a separate supply for them or share analogue power supplies.

On the other hand, we try to ensure that the digital part is as “quiet” as possible, especially during critical time of analogue part. Preferably, it is kept quiet for the *balance*, *sample*, *calibration* and *reset* periods, and no signal is changed on-chip between the end of output balance and the end of output sense.

#### 4.5 Reducing random noise

Based on the analysis of last section, we know that the dominant random noise sources

are bit line capacitance noise and horizontal line capacitance noise. For our technique, the bit line noise is not a serious problem. However, if the resolution is increased and the fixed pattern noise is reduced, the line noise may need to be reduced in order to further increase the signal to noise ratio.

To reduce the line noise, it is recommended to choose small dimension technology, make the pixel size small, and more importantly make the drain capacitance of each pixel as small as possible.

## 4.6 Chapter summary

The main noise sources of both random and fixed-pattern noise have been studied.

The dominant random noise source is line capacitance noise which is proportional to the resolution, and set a ultimate lower limit on detectable light intensity. The analysis has shown that with sense amplifiers on the top of the array, the line capacitance noise can be reduced significantly.

Fixed-pattern-noise is mainly from two sources: threshold variations in the MOS pixel access transistors and mismatches between column sense amplifiers. Schemes to eliminate and compensate these noise sources have been discussed.

The solution to the pixel threshold variation is to reduce the pixel reset voltage below  $V_{dd} - V_T$  so that the reset voltage is insensitive to the variation of the threshold  $V_T$ .

One solution to mismatches between column sense amplifiers is to calibrate each amplifier to give zero offset during each line synchronization interval. Other solutions include compensation at different stages.

## **Chapter5    Techniques to Improve Dynamic Range: Auto-exposure & Auto-gain Control**

### **5.1    Introduction**

Automatic exposure control (AEC) and automatic gain control (AGC) are common camera features required to improve dynamic range. This chapter describes on-chip solutions to implement these features.

Normally in good lighting it is necessary to control the exposure so that the distribution of grey levels within the image is reasonably well balanced. Over-exposure (e.g. in bright lighting) can push the grey level distribution mostly towards the white extreme, causing loss of useful contrast, saturation, and possibly blooming. Under-exposure results in similar loss of contrast as the majority of the image is compressed into the black end of the range.

Automatic exposure control is of significance to avoid mechanical iris control in electronic vision systems. We control exposure by varying the light integration time prior to reading each row of pixels. The integration time can be as long as one field, or as short as three cycles of pixel clock. In this way, a very wide range of 40,000:1 has been achieved.

Regarding exposure control, this chapter discusses two related issues:

- how to electronically set and vary exposures (electronic aperture),  
          and
- how to automatically control the exposure (electronic controller).

Under dim lighting conditions exposure tends to be set at maximum and as the image reduces further in intensity the grey level distribution again shifts towards black. Although useful picture content remains, the information may not remain visible on a TV monitor and where A/D conversion is used, useful information may be lost within

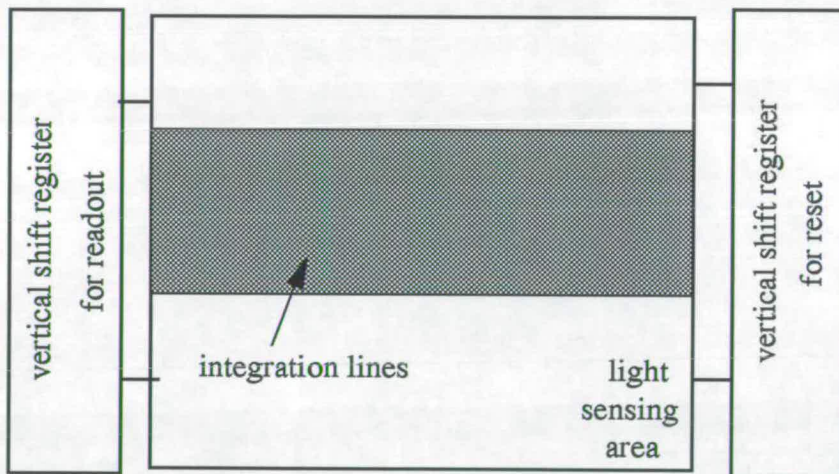
the quantisation step size. It is common practice to compensate for these effects by providing electronic gain within the output stage to restore the image amplitude. Of course the reduced dynamic range of the dim image is not improved, but the signal becomes more visible on a monitor and more detail is retained in data conversion.

This chapter will discuss two issues relating to gain control:

- how to electronically set the gain; and
- how to automatically control the gain.

## 5.2 Electronic aperture

An on-chip electronic aperture, equivalent to eight stops of a mechanical system has been reported before [Asano, 1988]. It uses two vertical shift registers, one for readout and another for reset (Figure 5.1).



*Figure 5.1 A sensor array with two vertical shift registers*

The exposure is adjusted by varying the time between reset and readout. This scheme only allows exposure adjustment on the basis of line time. A novel scheme is used for our designs, which enables exposure adjustment not only on the basis of line time, but

also pixel time. We refer the line time adjustment as coarse adjustment and pixel time adjustment as fine adjustment. This scheme allows a much wider adjustment range of 40,000:1, equivalent to 15 stops of a mechanical system. Another advantage is that with fine adjustment, oscillation will be less likely to happen for automatic exposure control schemes.

### 5.2.1 Algorithm

The architecture of the MOS image sensor has been shown before (Figure 3.1). The light sensing area consists of a photodiode array. The photodiodes are pre-charged to a fixed bias voltage during a reset cycle and then isolated for a suitable exposure time. During this time incident light partially discharges the junction capacitance, through the generation of photo-current in the diodes. For each pixel, the exposure is determined by the pixel integration time i.e. the time between resetting and sampling. When using the normal scheme of scan registers this integration time has to be a fixed number of clock cycles (usually a field time).

The novel scheme is to define the sample and reset signals in such a way that the time between them can be varied. The integration time  $t_{\text{int}}$  is then defined to be the sum of a variable number  $m$  of line intervals plus a variable number  $n$  of clock intervals:

$$t_{\text{int}} = m \times t_{\text{line}} + n \times t_{\text{clk}} \quad (5.1)$$

where  $t_{\text{clk}}$  is the pixel clock period and  $t_{\text{line}}$  is the line period.

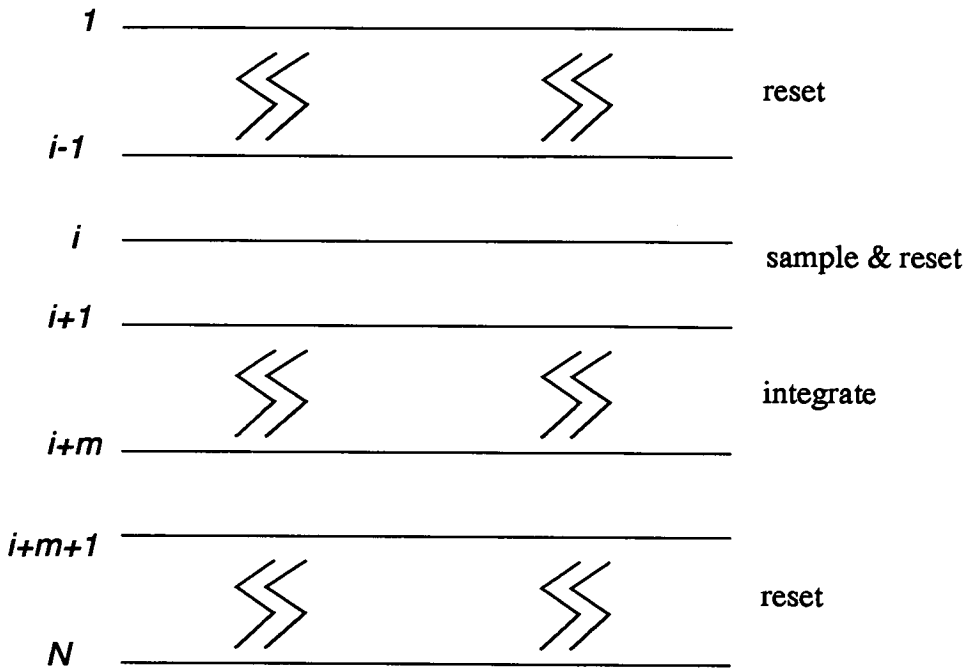
We refer  $m \times t_{\text{line}}$  as *coarse setting*, and  $n \times t_{\text{clk}}$  as *fine setting*.

#### Coarse setting:

At a particular line time, row  $i$  is being sampled and then reset, rows  $i+1$  through  $i+m$  are integrating and all other rows are being reset during the line period, as shown in



Figure 5.2.

*Figure 5.2 Exposure function at each row***Fine setting:**

Fine setting is achieved by varying the reset period. The reset time can range between a few clock intervals and nearly one line time, resulting in extra integration time  $n \times t_{\text{clk}}$  added to the coarse setting. The fine setting becomes more important when  $m \times t_{\text{line}}$  is smaller. In fact, the exposure is dominated by the fine setting when  $m$  equals 0.

The fine setting can be as short as several cycles of pixel clock and the coarse setting can be as long as one field. If a sensor has a resolution of  $312 \times 287$  and work on 6 MHz clock frequency, the minimum integration time is 500 nS (3 pixel clock cycles) and the maximum integration time is 20 mS. Totally, adjustment range is 40,000:1.

### 5.2.2 Circuitry

The problem then is to generate and decode suitable signals in such a way as to enable the correct rows and columns of the array in sequence. The vertical scan register has been replaced by a scan register with decoding, as shown in Figure 5.3 and Figure 5.4. The single-bit data-stream has been augmented with other signals, such as scan, sample, and reset.

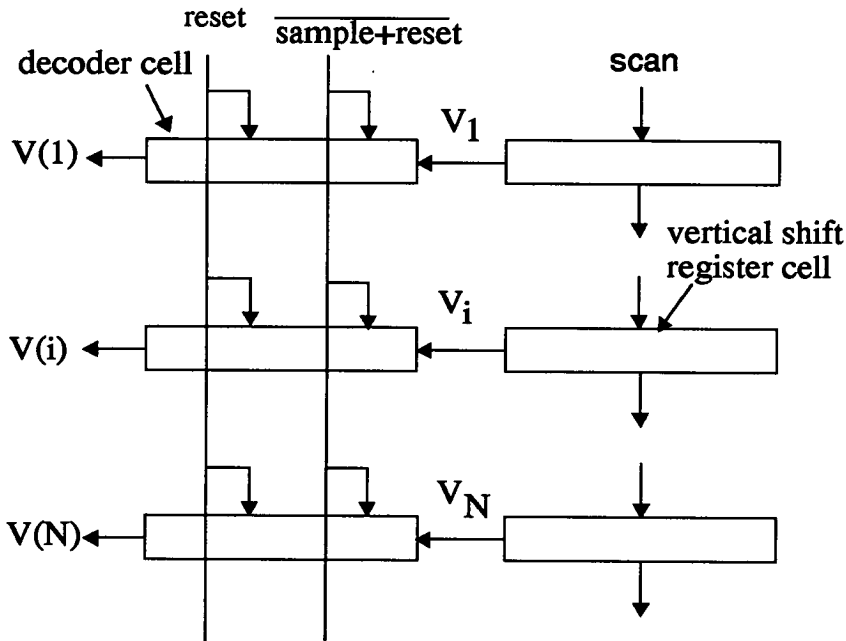


Figure 5.3 Vertical shift register with decoding

## 5.3 Electronic exposure controller

If we now alter the exposure setting in response to the monitored image, we can implement fully automatic electronic exposure control. A simple control mode is described in this section, which costs approximately 1,000 gates to implement. The control is achieved by monitoring the image pixel stream and estimating the fractions of each picture which are very white and very black. On the basis of this information, the device decides whether the picture contrast is acceptable, or too bright, or too dark. If necessary, the exposure time is then changed in the appropriate direction [Lu, 1991].

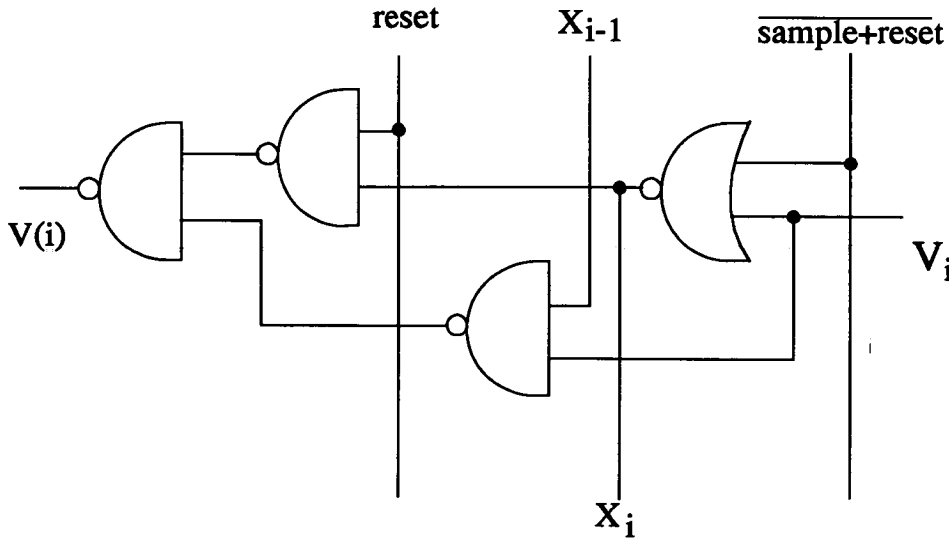


Figure 5.4 Decode circuitry

### 5.3.1 Algorithm

The image pixel stream is compared with two DC references to pick up “very white pixels” and “very black pixels”. A “very black pixel” means its value is below a black reference and a “very white pixel” is above a white reference. These occurrences are counted, and a threshold number is set to judge the present exposure. If “very black pixel” number is greater than the threshold number and “very white pixel” number is less, the picture is thought to be too dark, and the exposure should be increased. On the other hand, if the “very white pixel” number is greater than the threshold number and the “very black pixel” number is less, the picture is thought too bright, and the exposure should be decreased. When the numbers are both greater or both less than the threshold, the exposure is thought to be acceptable. No action will needed in this case.

The new integration time is calculated according to the following formula:

$$T_{\text{new}} = T_{\text{pre}} \times (1 \pm \text{step})$$

Eq(5.2)

if exposure is increased/decreased;

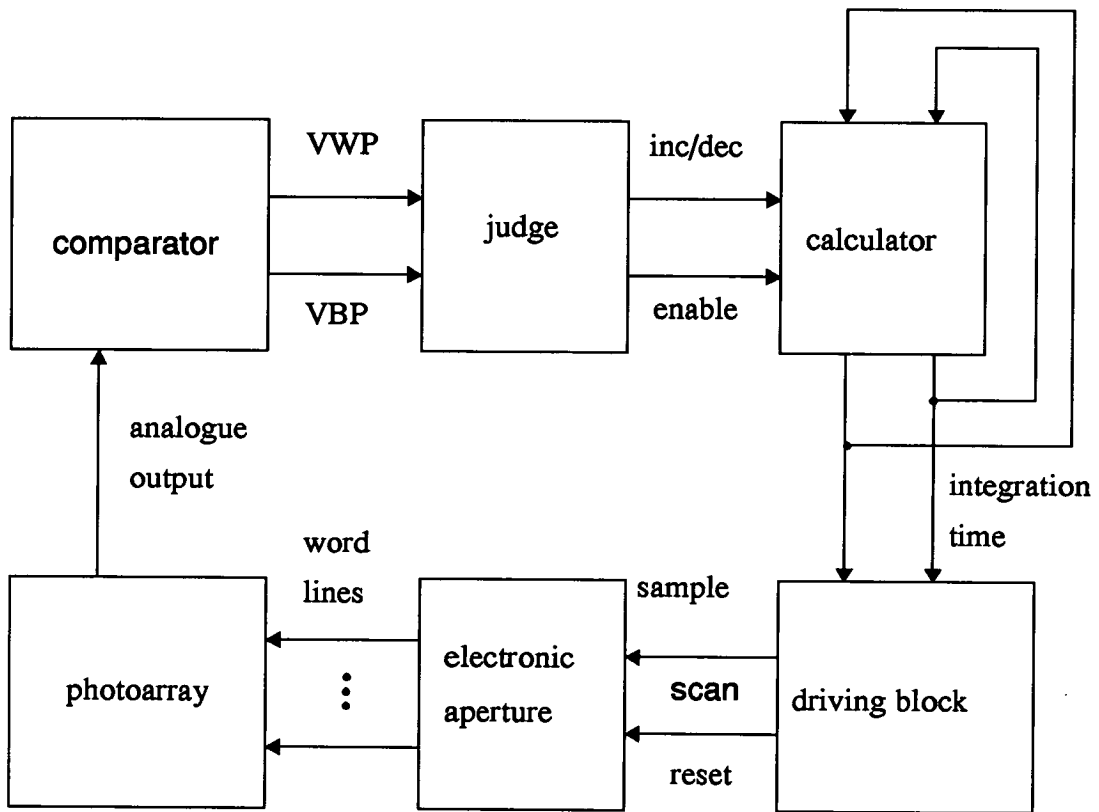
$= T_{pre}$

if no action.

where,  $T_{new}$  is new integration time for the next frame,  $T_{pre}$  is the present integration time. The step can be either 1/4, 1/8, or 1/16. The smaller step will take longer time to adjust when the light condition changes but the adjustment is more smooth, i.e. the variation of the brightness of the picture on the screen is less noticeable.

### 5.3.2 Circuitry

Figure 5.5 shows the block diagram of the exposure controller. Each block is introduced as follows.



*Figure 5.5 Block diagram of electronic exposure controller*

**Comparator:**

The video stream is fed into this block. Two DC voltage references are set to identify “very white pixels” and “very black pixels”.

#### **Judge:**

This block judges the present exposure by counting numbers of “very black” and “very white” pixels according to the above algorithm.

#### **Calculator:**

The new integration time is calculated here according to the above formula.

#### **Driving block:**

This block produces the driving signals, according to  $T_{\text{new}}$ , needed by electronic aperture, such as *scan*, *reset* and *sample*.

## **5.4 Gain setting circuitry**

Gain setting is implemented through putting a digitally controlled MDAC, (Multiplying Digital to Analogue Conversion), at the output stage of the sensor.

### **5.4.1 MDAC circuit**

Figure 5.6 shows the MDAC circuit which has a number of N-type MOS transistors in parallel as a load.

All these transistors have to work in their linear region and their sizes (ratio of the width to length) decrease by a factor of 2 in sequence to form a binary-ratioed series. The conductance of the load is  $G.D$ , where  $G$  is the conductance of the smallest device in the binary series and  $D$  is the digital word formed by the control bits applied to the series of gates. The input current is then converted into a voltage value (on the node A) equals to  $I/G.D$ .

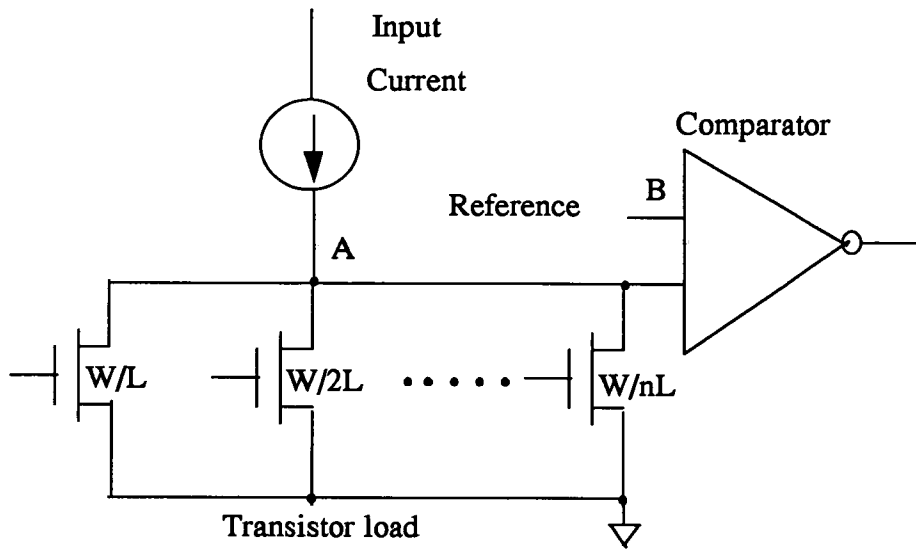


Figure 5.6 Gain setting and monitoring circuitry

### 5.4.2 Gain setting

For gain control purposes, the input current is modulated by the preceding signal amplifier, while MDAC input coefficients set the gain. If the gain is too low (i. e., the voltage values of the data-stream at the point A are too low), the coefficients will change so that the conductance of the load decreases. On the other hand, if the gain is too high (i. e., the voltage values of the data-stream are too high), the conductance of the load will be increased. The gain can only be adjusted during the sensor idle period, between two fields.

The wider range of the gain setting requires more bits of the load transistors. A 4-bit load will cover 24 dB of the gain setting. However, for auto-gain control scheme, more bits are needed to achieve smooth adjustment of the gain, or else oscillation will occur. We aim to control the gain over the range of 20 dB and choose a 7-bits load.

## 5.5 Auto-gain control

The gain is set to minimum (or a default setting near minimum) at initialisation and remains so for normally good lighting. When the lighting becomes dim, we first adjust exposure to cope with the variation of the light intensity. The AGC function will not turn on until exposure reaches maximum and the picture is still too dark. AGC can be thought to be an extension of AEC at its maximum end although they work on different circuit principles.

Similar to the exposure control, automatic gain control is achieved by monitoring the image pixel stream and estimating the fractions of each picture which are very white and very black. On the basis of this information, the device decides whether the picture contrast is acceptable, or too bright, or too dark. If necessary, the gain setting is then adjusted in the appropriate direction.

### 5.5.1 Algorithm

The algorithm used to control auto gain is similar to that for exposure. The image pixel stream is compared with two DC references to pick up “very white pixels” and “very black pixels”. These occurrences are counted, and a threshold number is set to judge the present gain. If “very black pixel” number is greater than the threshold number and “very white pixel” number is less, the picture is thought to be too dark, and the gain should be increased (the conductance of the load decreased). On the other hand, if the “very white pixel” number is greater than the threshold number and the “very black pixel” number is less, the picture is thought too bright, and the gain should be decreased (the conductance of the load increased). When the numbers are both greater or both less than the threshold, the gain is thought to be acceptable. No action will needed in this case.

The new gain setting (new conductance value) is calculated according to the following formula:

$$S_{\text{new}} = S_{\text{pre}} \pm S_{\text{step}} \quad \text{Eq(5.3)}$$

if Gain is decreased/increased;

$= S_{\text{pre}}$  if no action.

where,  $S_{\text{new}}$  is new conductance of the load for the next frame,  $S_{\text{pre}}$  is the present conductance,  $S_{\text{step}}$  is the smallest quantised conductance of the parallel transistor load.

AGC will turn off when gain returns to minimum (or nominal) and the picture is still too bright. Then the sensor will come back to normal AEC mode.

### 5.5.2 Circuitry

Figure 5.7 shows the block diagram of the digital control circuit which is similar to the control circuit for exposure. In fact, both control circuits share much circuitry so that only approximately 200 more gates are needed to implement AGC as well as AEC.

Each block is briefly described as follows:

#### Comparator:

The video stream is fed into this block. Two DC voltage references are set to identify “very white pixels” and “very black pixels”.

#### Judge:

This block judges the present gain setting by counting numbers of “very black” and “very white” pixels according to the above algorithm.

#### Calculator:

The new gain setting (the conductance of the load) is calculated here according to the above formula.



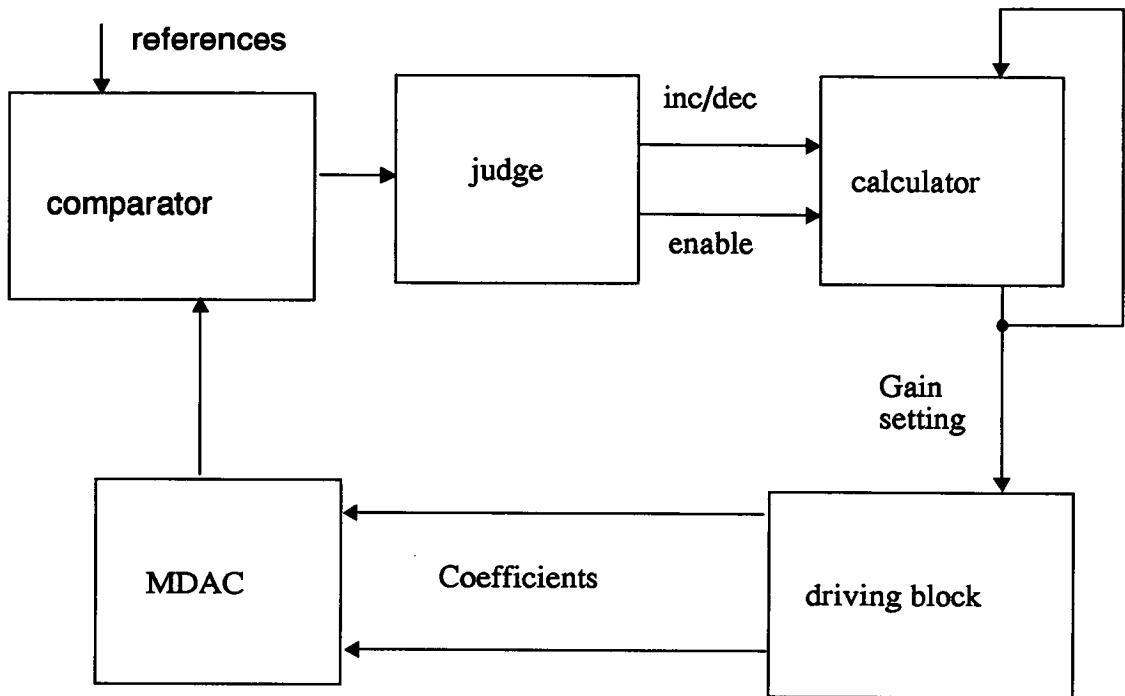


Figure 5.7 Block diagram of auto-gain control

#### Driving block:

According to the new value of the conductance of the load, this block produces the input coefficients applied to the gates of load transistors.

## 5.6 Chapter summary

Novel electronic aperture and gain setting circuitry, as well as control logic blocks, have been introduced. The algorithms and the circuitry are suitable for integration. Therefore, CMOS cameras can include these functions, together with the basic sensor array, to enhance the performance. Such single chip cameras will have a wide dynamic range without any mechanical iris and/or external amplification circuitry, which will make MOS sensors more attractive in many applications.

## Chapter6 OTHER TECHNIQUES

This chapter discusses some other useful techniques such as analogue to digital data conversion,  $\gamma$  correction of the image signal, and a simple solution for wafer test. These techniques are useful to either enhance the functionality, or improve the quality, or reduce the fabrication cost.

### 6.1 Data conversion

On-chip data conversion is of significance in order to integrate digital signal processing with a sensor array on the same substrate. It will also benefit machine vision applications by further reducing the cost, size, and power consumption. A simple approach is described here, which can be used for successive-approximation analogue to digital conversion with 7 bits accuracy and conversion time of 1 micro second.

#### 6.1.1 Approximation sequence

The MDAC and the comparator used for AGC (refer to Section 5.4.1, Figure 5.6) can also be used for successive approximation analogue to digital conversion. In this case, the MSB is the transistor with biggest conductance and the reference voltage of the comparator is set to be equal to the white signal level of the image data at node A (Figure 5.6). The conversion cycle begins by assuming that the MSB is 1 and all other bits are zero. The coefficients are applied to the gates of the load transistors and these generate an analogue signal at node A, which is then compared to the white reference level at the node B. If the comparator output is high, the digital control logic makes the MSB 0. If the comparator output is low, the digital control logic makes the MSB 1. After the first step in the approximation sequence, the value of the MSB is known. The approximation process continues by once more applying a coefficient to the load transistors, with the MSB having its proven value, the next lower bit being 1, and all the other remaining bits being 0. Again, the voltage level at node A is compared to the reference level at node B. If the output of the comparator is high, the second bit will be set 0. If the output of the comparator is low, the second bit will be set 1. This completes

the second step in the approximation sequence. The process continues in this manner until all bits of the digital word have been determined.

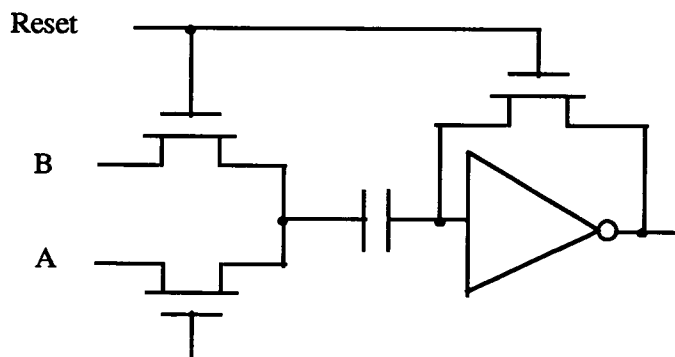
### 6.1.2 AEC and AGC with the conversion

As the MDAC and the comparator are fully used for data conversion they are not available for monitoring the image and setting the gain. In this case, the quality of the picture can be measured from the digital output obtained. One way is to count grey levels in four coarse intervals, e.g. using the top two bits after conversion.

The gain setting can be carried out by changing the reference level on the node B. If the reference level is half of the white level, 2 times of the gain will be achieved during the conversion. The cost is that the half signal range towards the white end is lost. Similarly, if the reference level is a quarter of the white level, 4 times gain will be achieved.

### 6.1.3 Comparator

We use a capacitive input differential circuit in place of the conventional differential pair and current source [Denyer, 1978]. Figure 6.1 shows the diagram. The comparator has inherent immunity to common-mode signals and bias variations.



*Figure 6.1 capacitive differential input comparator*

The operation of the comparator consists of 2 phases. The first one is a reset phase, during which the amplification stage (an inverter) is self balanced, in the same way as the balance of sense amplifiers (Chapter 3). A reference voltage level is sampled on the input capacitor when the inverter is balanced. The second phase is then a signal phase, during which the signal to be compared is sampled on the input capacitor. The difference between the signal and the reference will be coupled to the input of the inverter. If the signal is greater than the reference level, the input of the inverter will be greater than its balance value, the output will become 0. If the signal is lower than the reference level, the output will be 1.

The problem of drift in the normal differential stage is completely eliminated by the reset action. There is also no error because both input signals are time multiplexed onto the same input capacitor. Amplification stages usually suffer from bias and drift problems, which cause shifts in the output zero level and thus apparent offsets at the input. These problems are completely eliminated by the balance of the inverter.

In practice, we actually don't reset the comparator for every pixel output. It is reset once per line. The reason for this is that we wish to minimise the number of S/H actions at the pixel rate happening at the output stage.

## 6.2 Black level calibration

It is important to have a constant black level to get the right TV format and good picture quality. There will be synchronization problems if the black level is too low (lower than blanking level). On the other hand, the black contents will look less than black if the level is too high. Data conversion also needs a constant black level. However, ASIC processes can not guarantee such a constant level for different batches because electronic parameters may change (such as value of threshold voltage). Variation in operating temperature will also result in a shift in black level.

To maintain image stability and obviate the need for external adjustments, the chip should include facilities for automatic black level (offset) calibration. For this purpose, extra lines of "black pixels" are added to the photo array. These pixels have exactly the

same structure as normal pixels but are shielded from light and are reset just before readout. These “black lines” are readout as normal, providing a black level reference value.

Calibration takes place at the output stage with the addition of transistors M5 - M8 as well as a capacitor  $C_{BCK}$  (Figure 6.2). When the “black lines” are clocked through the output amplifier, “breb” is set low. At the same time the output to the MDAC is disabled. With M7 is turned on, the gate voltage of M6 will vary until the current in M6 matches the current in M5 resulting from the black reference.

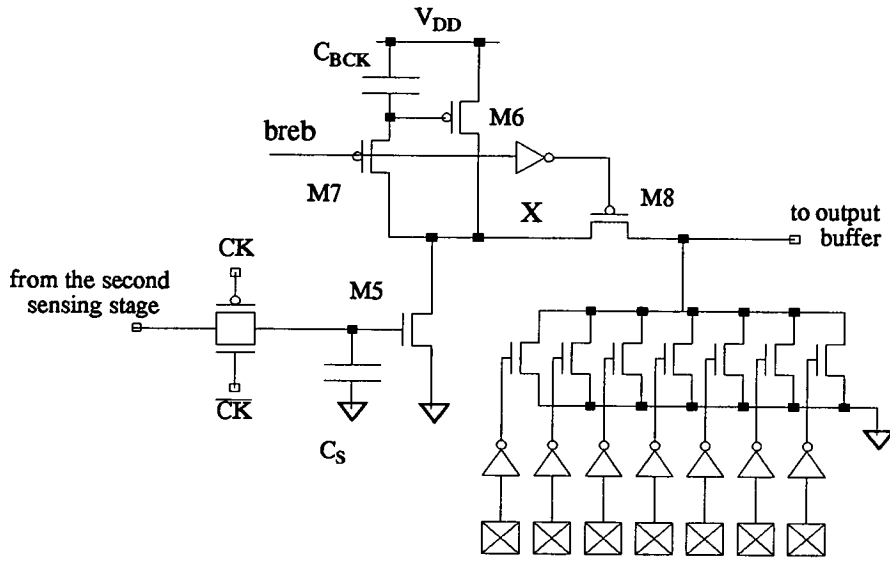


Figure 6.2 Black level calibration circuitry

For normal pixel readout, M7 is turned off. The gate voltage of M6 is then stored on  $C_{BCK}$  for the duration of a field. M8 is turned on, and the signal current goes through M8 and load transistors of MDAC circuitry.

The signal current is equal to

$$I = I_{M6} - I_{M5} = I_{\text{black}} - I_{M5} \quad \text{Eq(6.1)}$$

For black pixels,  $I_{M5}$  is equal to  $I_{\text{black}}$ . Therefore, the signal current  $I$  and the voltage across load transistors are zero. For non-black pixels, the  $I_{M5}$  will be less than  $I_{\text{black}}$ , and there will be a voltage, proportional to  $I$ , across load transistors.

In this scheme, the black level voltage is kept zero although the gate voltage of M5 may vary from chip to chip for black signal. Therefore, the circuitry is ideally free of any external analogue offset.

### 6.3 $\gamma$ Correction

To first order, a television system ought to be linear, i.e. the light emitted from the receiver display should be directly proportional to the light falling upon the camera target. However, picture display-tubes do not emit light in direct proportion to the voltage applied between its grid and cathode, due to the non-linearity of the beam current against grid/cathode voltage characteristic. If the luminance ( $L$ ) of the screen is plotted against the grid/cathode input voltage  $V_g$ , the curve (for low values of  $V_g$ ) is roughly parabolic. The non-linear relationship between light output and voltage input may be expressed as [Trundle, 1987]:

$$L = V_g^\gamma \quad \text{Eq(6.2)}$$

where  $\gamma = 2.2$

If a linear video signal (to which no compensation has been applied) is supplied to a picture tube, then the output of the tube will result in a compression of contrast in the dark regions of the picture, and a stretching of contrast in the lighter areas. Correct reproduction in images requires the signal to be compensated by an equal and opposite characteristic (Figure 6.3):

$$Y = X^{\frac{1}{\gamma}} \quad \text{Eq(6.3)}$$

where  $\gamma = 2.2$

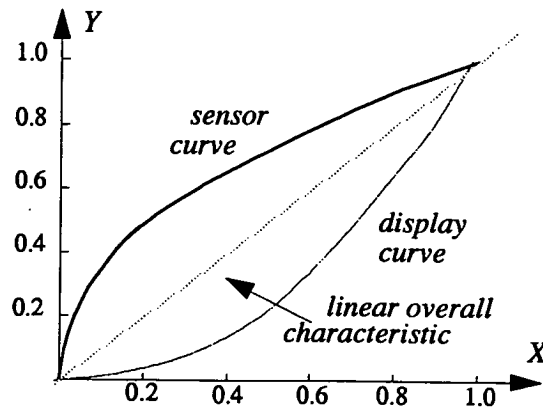


Figure 6.3 The display and sensor device gamma curves

This is termed  $\gamma$  correction and is usually implemented using discrete components, e.g. a ladder-network of diodes, resistors and reference voltage, as shown in Figure 6.4. As the video signal reaches reference voltage  $V_1$ ,  $V_2$ , and  $V_3$ , progressively more diodes turn on to shunt away the signal and reduce its level.

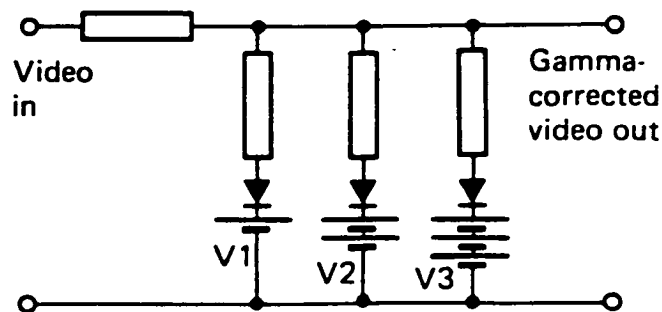


Figure 6.4 A ladder network for  $\gamma$  correction

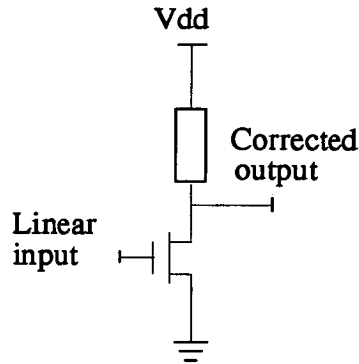


Figure 6.5 a simple  $\gamma$  correction circuit

Unfortunately this ladder network  $\gamma$  corrector, is not ideally suited to integration. In our design approximate  $\gamma$  correction is achieved by a simple solution which uses the nonlinear  $I_D$ - $V_{GS}$  characteristic of the MOS FET. One solution involves the construction of an inverting amplifier using a transistor as the active device and a resistor as the load as shown in Figure 6.5. So long as the active device is operated in a suitable region it will provide a relationship between input and output that is approximately the inverse of the square of the inverted input signal. This relationship corresponds to the desired compensation characteristic, which has to progressively compress the white and expand the black portions of the input signal. Figure 6.6. shows both SPICE simulation result for this circuit and theoretical curve of ideal  $\gamma$  correction.

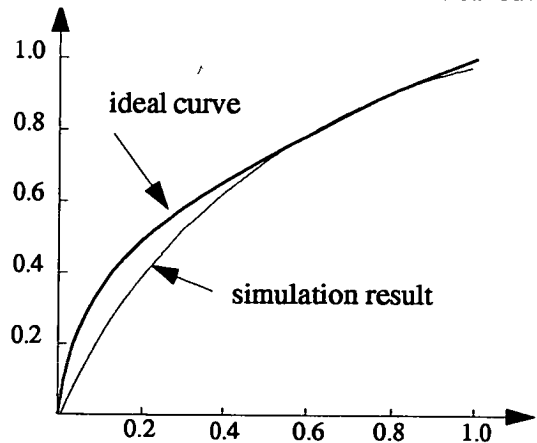


Figure 6.6 Simulation result and theoretical curve



Figure 6.7 shows a second  $\gamma$  correction circuit which is based on the output buffer of Figure 3.11. This is performed by exploiting the saturation  $I_{DS}$  to  $V_{DS}$  characteristic of M15. The simulation result is similar to that of the resistor load scheme discussed earlier (Figure 6.5 and 6.6).

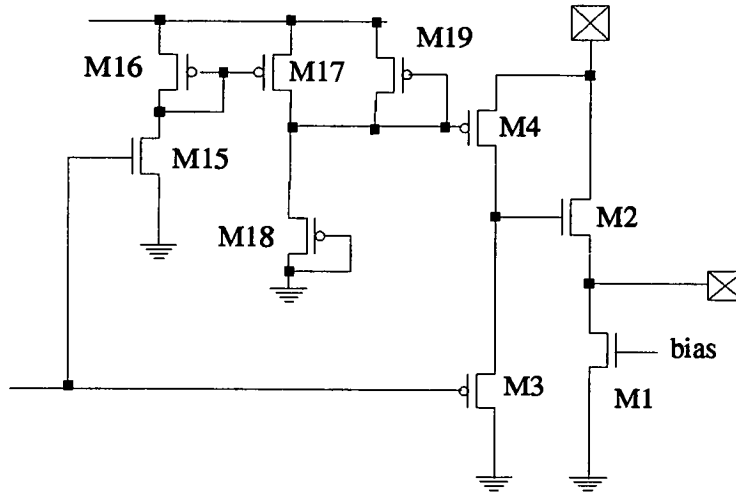


Figure 6.7 Another  $\gamma$  correction circuit

## 6.4 Simple solution for test

This section discusses how image sensor arrays can be designed and tested such that the techniques of conventional digital integrated circuit production can be used to achieve a high level of production fault testing at the wafer test stage. Therefore, both optical and analogue tests can be avoided in this stage. In our solution, predetermined digital patterns of data are loaded to word-lines, bit-lines and array pixels, and output patterns are compared with the simulation vectors to assess the level of production faults.

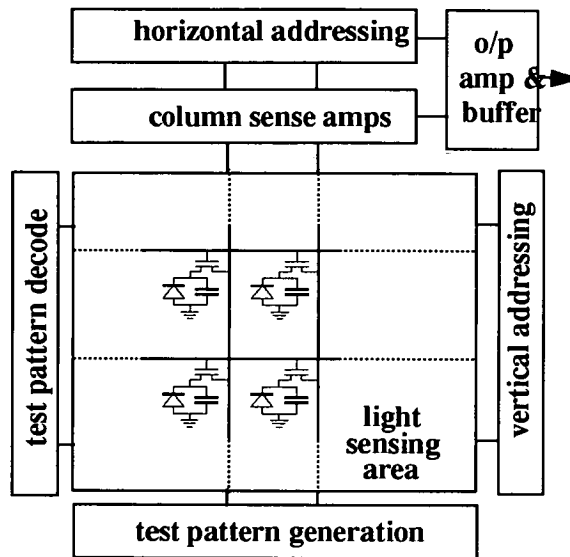
### 6.4.1 Principle

Integrated circuit sensor arrays are difficult to test in production. Referring to Figure 3.1, the desired result is that each sensing site (pixel) should be responsive to the

anticipated radiation and should be capable of storing an analogue charge packet for a suitable integration period. The charge packet should then be readable by activating word-lines to enable a row of pixels to be sensed via bit-lines which connect the pixels to sense amplifiers at the top of the sensing array.

A complete optical test is awkward to perform when the integrated circuits are in wafer form. It is more convenient to perform this test after the circuits have been separated and packaged. However, it is economically desirable only to package good circuits or those which are most likely to pass the final tests.

A simple solution has been used for the testing of the customisable sensor array, in order to reduce production costs. Special consideration has been given to avoid both optical test and analogue test. Therefore, the techniques of conventional digital integrated circuit production can be used to achieve a high level of production fault testing at the wafer test stage. This is achieved by loading predetermined digital patterns to word-lines, bit-lines and array pixels, and comparing output patterns with the simulation vectors to assess the level of production faults. To enable this, extra test circuits are included at the periphery of the sensor array, as shown in Figure 6.8. The circuit on the left of the array is for decoding the word-line states and the circuit at the bottom is for loading the patterns to bit-lines and individual pixels.



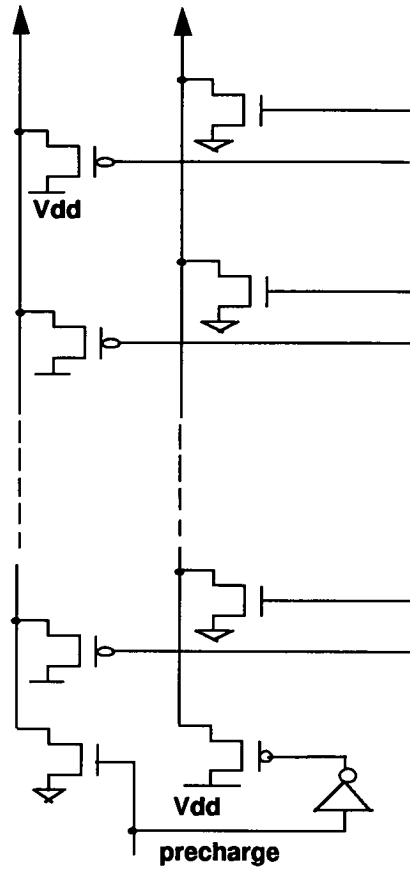
*Figure 6.8 Image array with test circuits*

We consider three classes of tests. The first class of test verifies the integrity of the word-lines and the associated drive circuitry. The second class of tests verifies the integrity of the bit-lines and the associated sensing and read-out circuits. A third class of tests may be applied to test the functionality of individual pixels, if required.

#### 6.4.2 Word-line Test

Word-lines are tested by feeding a sequence of digital patterns, 101010...., to the vertical shift register. The patterns will appear on those word lines. A test pattern decoder is placed on the other side of the array to detect this pattern. We then examine the pattern decode outputs to determine whether the expected patterns are being driven onto the word-lines.

Figure 6.9 shows the diagram of the decoder.



*Figure 6.9 Word line pattern decoder*

This includes two distributed dynamic gates. On the right is a distributed dynamic NOR gate which provides n-type transistors connected to every word line on which a low voltage (0) is expected. If any of these word lines is at fault and carries a high voltage (1) then the output of the NOR gate will go low, signalling a fault. On the left is a distributed dynamic NAND gate which provides p-type transistors connected to every word line on which a high voltage (1) is expected. If any of these word lines is at fault and carries a low voltage (0) then the output of this NAND gate will go high, signaling a fault.

The first class of tests therefore covers open- and short-circuit word line faults and gives

a digital functionality check of the word-line drive circuitry.

### 6.4.3 Bit-line (Associated Sensing & Read-out Circuits) Test

This test is carried out by writing digital patterns into the bit-lines. To enable this to be done we include additional circuitry at the bottom of the array. The normal sense and read-out mechanisms are then employed to output the detected states of the bit-lines. By suitably thresholding the output buffer, a single digital pixel-stream vector will appear on the analogue output pad.

Typically we use two test patterns; one is 101010...., giving alternating highs and lows on consecutive bit lines and the other is 010101...., giving a complementary pattern of lows and highs. In this way each bit line is tested in the low and high state in opposition to its physical neighbours. Figure 6.10 shows the diagram of the test pattern generation circuit.

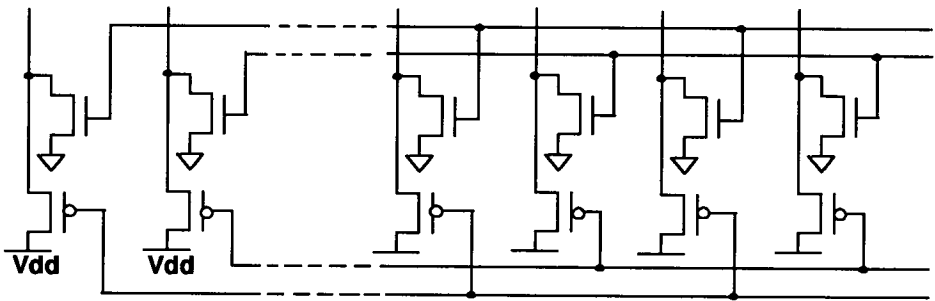


Figure 6.10 bit line test pattern generation circuitry

This second class of tests therefore covers open- and short-circuit bit line faults and gives a digital functionality check of the sense and read-out circuitry.

### 6.4.4 Pixel Test

A third class of tests may be applied to test the functionality of individual pixels. In this test we use the test pattern generation circuit to load saturated high or low charge

packets into rows of pixels at their normal time of reset. After loading in this way, each row may subsequently be read by scanning in the normal manner and the stream of output pixels is tested to determine whether it contains the expected pattern of highs and lows. In this class of tests the bit-line test vector generator is being used to generate a binary pseudo-image within the array without requiring any optical input.

This latter test requires a long test vector set for large arrays. Additionally, we have designed a self-generated checkerboard pattern which may be displayed on a monitor screen, or captured by a frame grabber, allowing easy detection of defective pixels. Thus, pixel testing can be run separately at a later stage. This checkerboard pattern can be used not only to find defective pixels but also to test analogue performance parameters, such as read out speed and uniformity.

## 6.5 Chapter summary

Techniques for the data conversion, black level calibration,  $\gamma$  correction, and the test have been introduced in this chapter.

A simple approach for successive-approximation analogue to digital conversion enables on chip data conversion. This is of significance for the integration of image sensor with digital signal processing. It will also benefit machine vision applications by further reduce the cost, size, and power consumption of the systems. To maintain image stability and obviate the need for external adjustments, automatic black level calibration is needed. On-chip implementation of  $\gamma$  correction is achieved by using the nonlinear  $I_d$ - $V_{GS}$  characteristic of an MOS FET.

Image sensor arrays can be designed and tested using techniques of conventional digital integrated circuit production to achieve a high level of production fault testing at the wafer test stage. In this way, both optical and analogue tests can be avoided in this stage but improved screening can be achieved.

## Chapter 7    Implementation: A Single-chip Video Camera

### 7.1    Introduction

In order to test the techniques described in the previous chapters, a single chip video camera has been designed and fabricated.

The device, named ASIS-1011, is a highly-integrated CMOS camera chip. In addition to a  $312 \times 287$  pixel image sensor array, it includes all necessary circuits to drive and sense the array, delivering a fully-formatted composite video signal.

The device features automatic electronic exposure control over a wide range, enabling the use of a fixed-aperture lens. Automatic gain control (AGC) provides up to +10dB gain boost at low light levels, while automatic black-level calibration maintains image stability, obviating the need for externally-adjusted components.

The die measures  $7.95 \text{ mm} \times 7.05 \text{ mm}$ , using the  $1.5 \text{ }\mu\text{m}$ , 2 level metal CMOS technology of ES2 (European Silicon Structure).

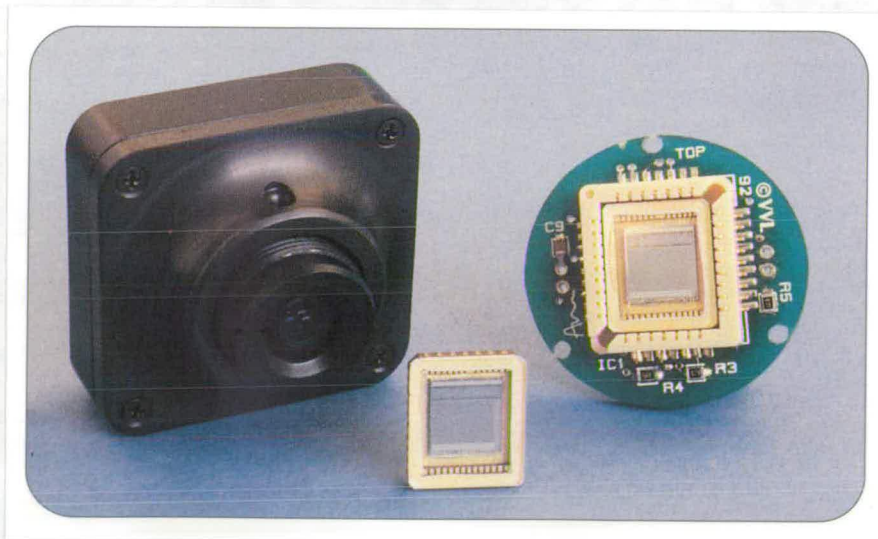
A miniature PCB integrates the chip with all necessary components to implement a complete CCIR-standard video camera, requiring a single unregulated DC voltage supply to produce a buffered composite video output capable of driving a 75 ohm load at 1 volt peak-to-peak. These components are:

- a 12 MHz crystal or ceramic resonator as clock source;
- a 5v regulator for stabilizing the power supply;
- a bipolar transistor for buffering video output;
- a few resistors and capacitors for biasing and decoupling.

The PCB, including chip and all other components weighs 5gm, measures 30 mm diameter, and consumes 150 mW. Figure 7.1 and 7.2 show photographs of a chip, a PCB, and miniature cameras.



*Figure 7.1 A photograph of a miniature camera*



*Figure 7.2 A photograph of a chip, a PCB, and a camera*



Both devices and cameras are now commercially available.

## 7.2 Main features

Main features of the chip and the camera are:

- $312 \times 287$  pixel array
- $19.6 \mu\text{m} \times 16.0 \mu\text{m}$  pixel size
- $6.12 \text{ mm} \times 4.59 \text{ mm}$  effective array size
- $7.97 \text{ mm} \times 7.05 \text{ mm}$  die size
- automatic black-level calibration
- automatic exposure control (range 40,000:1)
- automatic gain control (up to +10 dB)
- field-start and pixel clock outputs to facilitate frame grabbing
- 0.5" format lens-compatible
- CCIR-standard composite video output.
- 2 lux operation at f1.2
- power consumption < 150mW

### 7.2.1 Fixed pattern noise

Fixed-pattern noise caused by threshold variations in the MOS pixel access transistors

and mismatches between the column sense amplifiers have been reduced by the schemes presented in Chapter 4. The fixed-pattern noise of this design is -40 dB.

Faint vertical stripes still remain at -40 dB. This is mainly due to the interference of the digital power supply coupling to the analogue power supply. One form of digital noise is caused by the turn over of the counters. We have carefully separated the digital and analogue power supplies and tried to make the analogue supplies as “clean” as possible to minimize the interference. However, there is interference through the substrate, which we have no control for the present technology. Fortunately, the scaled down technology (say, below 1  $\mu\text{m}$  technology) will have twin-tub which should further reduce the interference through the substrate. Noise performance is also very sensitive to PCB routing.

### 7.2.2 Automatic Exposure Control (AEC)

The device automatically controls its exposure over a range of 40,000:1 by the scheme described in Chapter 5. This is the main mechanism for adjusting sensitivity to track varying picture conditions. The integration time can be as long as one field, or as short as three cycles of the pixel clock. The exposure is set by monitoring the video stream and estimating the fraction of each picture which is very white (above VWT) and very black (below VBT). VWT and VBT are pins which set white and black threshold levels. On the basis of this information the device decides whether the picture is too white, too dark, or OK.

The exposure time is varied if necessary, in steps of 6.25%, in the appropriate direction until the correct exposure for the scene is obtained. Two choices of thresholding algorithm are available under control of a pin labelled ITS. Setting coarse thresholds (ITS = 0) minimizes the risk of flicker on uneventful scenes, at the risk of stalling at a sub-optimal exposure value.

### 7.2.3 Automatic Gain Control

The output gain of the device is controlled by the scheme described in Chapter 5. A 7-

bit MDAC has been implemented on chip. In theory, it can provide gain adjustment of more than 100 times. However, in practice, we should put margins on both ends. We can not use minimum gain as normal setting because it may cause trouble if the gain is still high. This could happen by technology variations. Therefore, the normal gain is set higher and the setting can be adjusted by external pull-up and pull-down of pins. At the other end, we don't use the very high gain settings because a single step there actually means a big step. Thus, we use the middle range of the setting and expect a gain control of 10 for this design.

AGC function is optional. When pin AGC is pulled low, the device automatically increases the gain of its output stage when exposure is maximum and the picture is still too dark. Otherwise gain is maintained at its normal value which can be set externally by pins GS5, GS6 and GS7.

The gain control works well over the expected range for the nominal gain setting. However, the PCB tuning changes a few of bias value (such as BCK) in order to get better picture. The gain setting then has to follow those bias changes. The actual normal setting was more than 2 times higher than expected setting, leaving the gain adjustment of about 4 (10 dB).

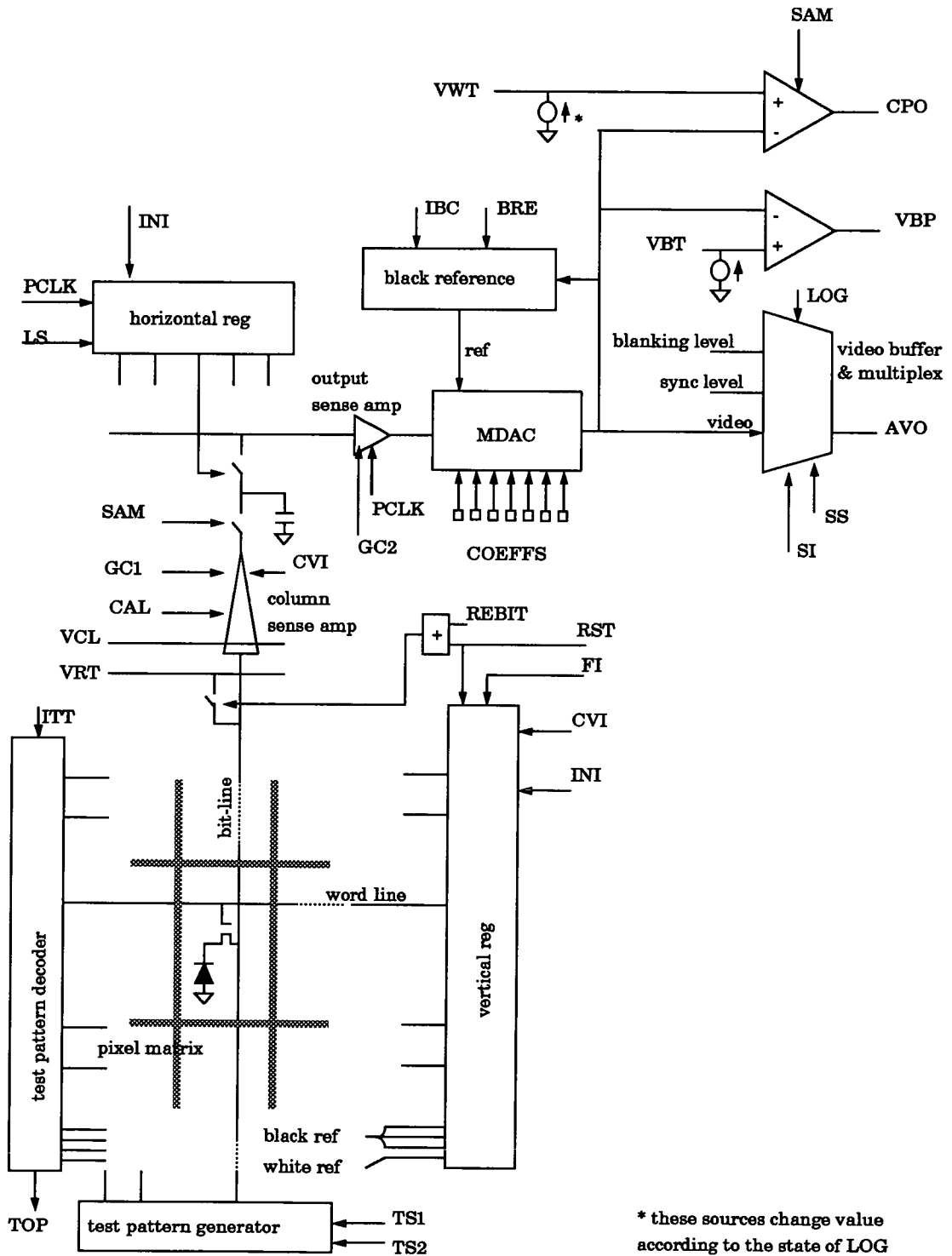
### **7.2.4 Automatic Black-level Calibration**

This device automatically calibrates video black level using the method described in chapter 6. Three extra lines of “black pixels” are added on the bottom of the photo array, of which, the second line is used for calibration. The reason to put three extra lines is to avoid leakage from neighbouring non-black pixels. Calibration occurs every field. It can be inhibited by setting the pad IBC = 1, in which case an internal bias voltage sets a nominal black level. This bias voltage can be overridden externally on pin BCK for fine adjustment.

## **7.3 Analogue circuit and layout**

The main part of a camera chip is the analogue block which comprises of a pixel array

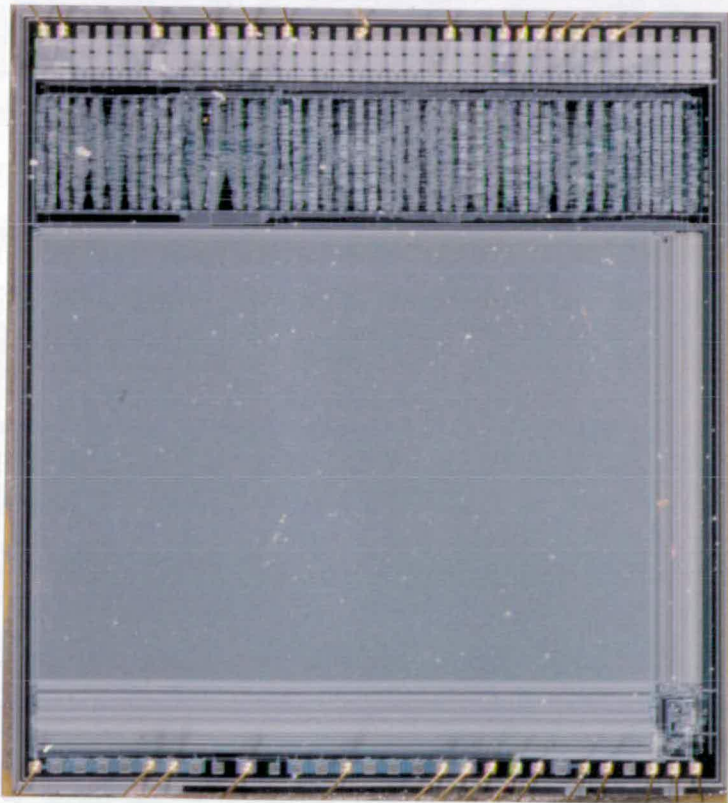
together with the necessary sensing and addressing circuitry.



The core of the chip is the photo-array. Around the array are associated addressing, sensing, and testing circuitry. The layout of these parts is custom designed (using MAGIC) to make it as compact as possible. Figure 7.3 shows the circuit architecture of the analogue part, and all I/O signals are explained in the appendices.

Figure 7.4 is the photo-micrograph of the chip. At the top of the chip is the 2,600 gate digital logic processor, laid out using a semi-custom standard-cell compiler (SOLO 1400). Half of this logic generates driving signals to the array, such as synchronization timing, including line-sync and frame-sync signals to format a 625line/50Hz standard composite video output.

The other half of the logic are included for automatic exposure and gain control. all logic only occupy less than 1/5 area of the chip. This shows the potential to put much more intelligent and powerful control logic on the chip.



*Figure 7.4 Photo-micrograph of ASIS-1011*

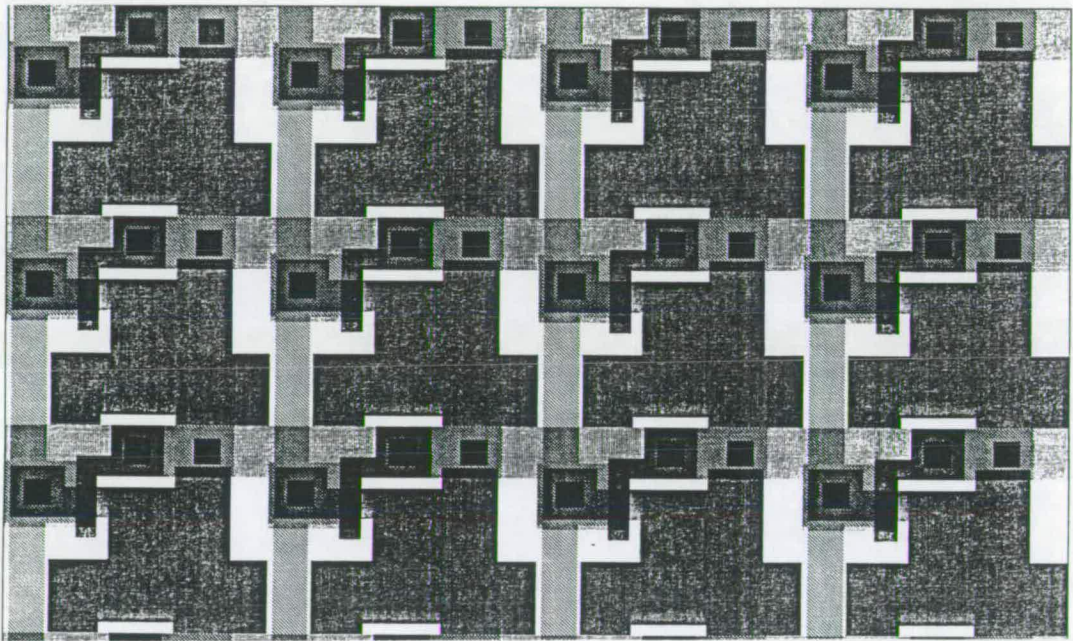
The custom layout is presented as follows.



### Pixel and pixel array

Figure 3.4 has shown the layout of a pixel. The layout of an array is composed by simply repeating pixels in both x and y direction. The efficiency of the sensor is improved by maximising the fraction of each pixel occupied by the exposed diode. The fraction will be improved if the pixel size increases. However, we have an interest in keeping the pixel pitch small to maximise the sensor resolution achievable within a given cost. A fill factor of 47% was achieved for this design.

Figure 7.5 shows the layout of several pixels.



*Figure 7.5 Layout of pixel array*

### Pixel-pitch-matched circuitry

Sense amplifiers and horizontal shift registers are on the top of the sensor array, while vertical shift registers with encoding circuitry are physically put on the left of the array. They all have to be pitch-matched to the pixel array. The realisation of these cells within a narrow pixel pitch and the achievement of good performance, especially for analog amplifiers, present the main engineering challenges of layout design.

Figure 7.6 shows layouts of sense amplifier and horizontal shift register cells.

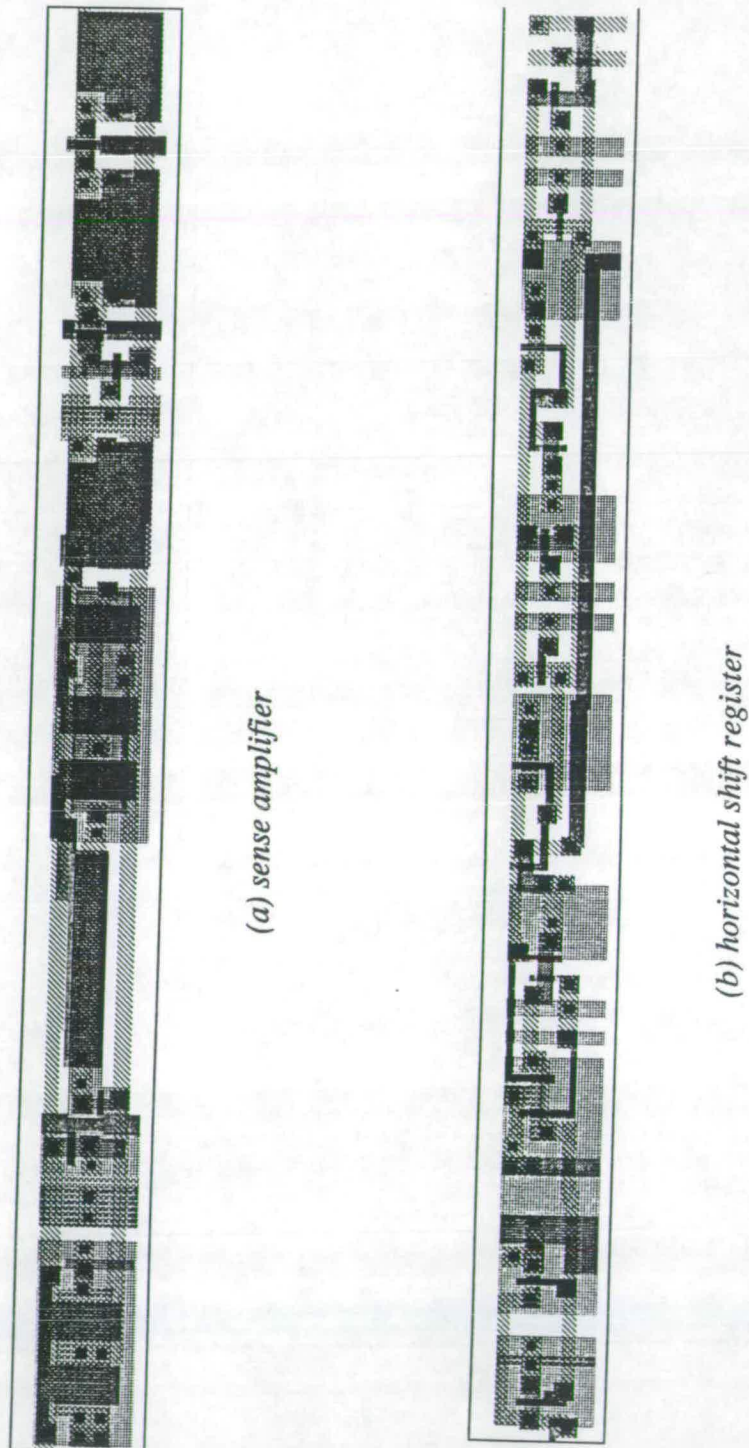


Figure 7.6 Layout of sense amplifier and horizontal shift register cells



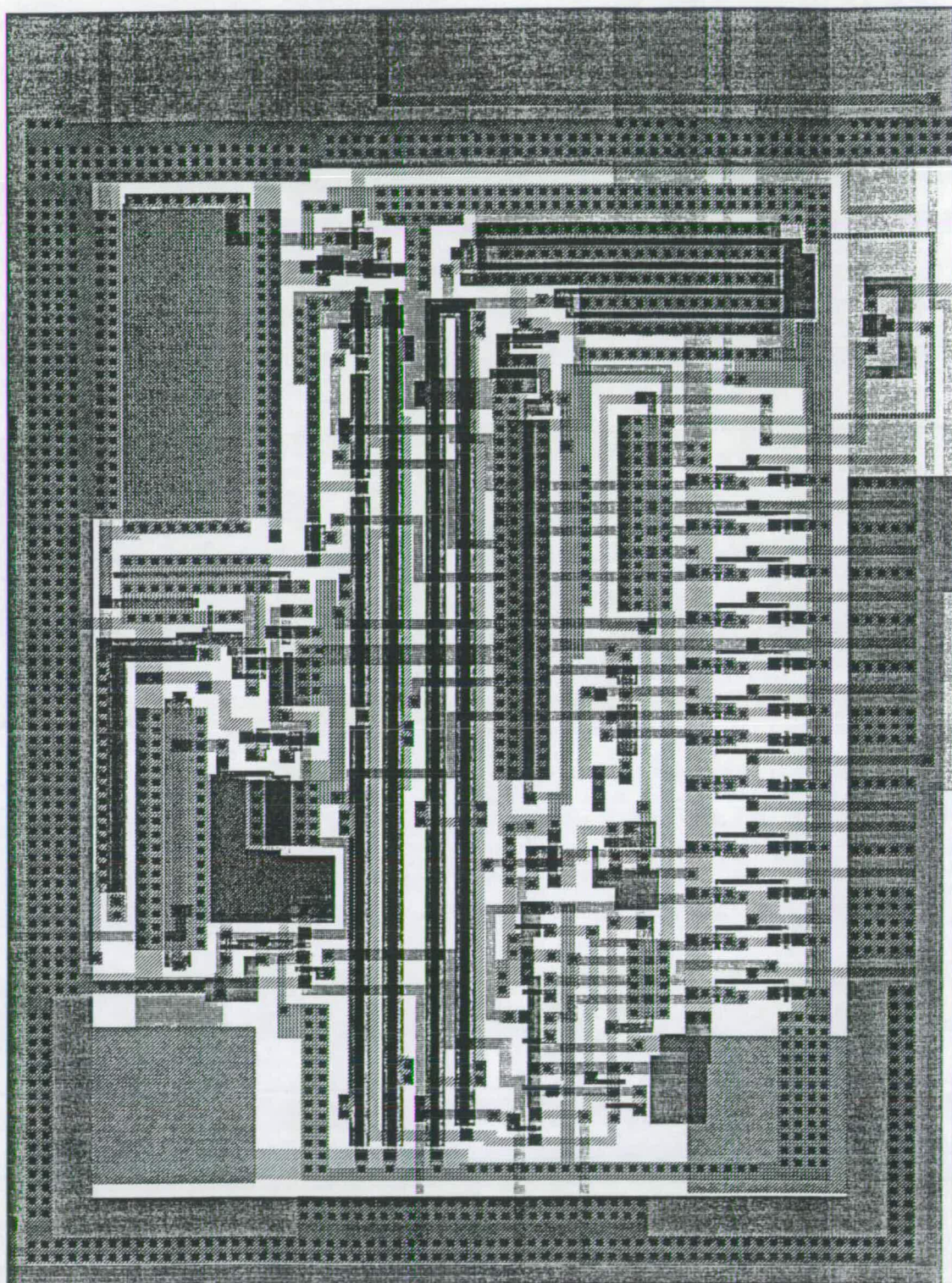


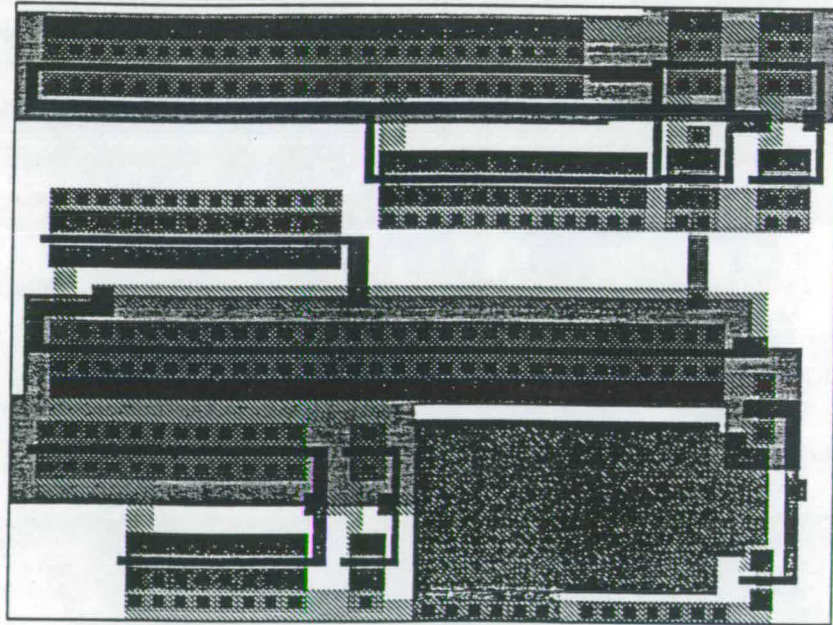
Figure 7.7 Layout of the output amplifier and buffer



### Non-pixel-pitch-matched circuitry

Other cells include an output amplifier, a output buffer, and several comparators which are not pixel pitch matched. However, in order not to enlarge the chip area, it is better to contain all these cells within the Top-Left corner area defined by the height of horizontal shift register and the width of vertical shift register (refer to Figure 7.4), otherwise the total area occupied by the custom block will be increased by empty boarder area.

Figure 7.7 shows the layout of output amplifier and buffer, and Figure 7.8 shows the layout of a clock driving circuit. (Figure 3.15).



*Figure 7.8 layout of a clock driving circuit*

## 7.4 Characterization

The chip and the camera have been tested and characterized. The table on the next page summarizes the electrical and optical parameters.

	units	min.	typ.	max.
IDD <sup>(1)</sup>	mA		12.0	
ID1 <sup>(1)</sup>	mA		8.0	
ID2 <sup>(1)</sup>	mA		8.0	
ID3 <sup>(1)</sup>	mA		negligible	
Video Peak White <sup>(2)</sup>	V		3.25	
Video Black <sup>(2)</sup>	V		1.25	
Video Blanking <sup>(2)</sup>	V		1.25	
Video Sync. <sup>(2)</sup>	V		0.65	
Output Impedance	$\Omega$		100	
Saturation Exposure	nJ/cm <sup>2</sup> mJ/cm <sup>2</sup>		60 <sup>(3)</sup> 2.4 <sup>(4)</sup>	
Dark Current <sup>(5)</sup>	times sat.		0.0004	
Fixed-Pattern Noise <sup>(6)</sup>	dB rms		-40	
Random Noise	dB rms		-54	
Clock Breakthrough	V			0.05
Blooming Tolerance <sup>(7)</sup>	times sat.	60		

1. At VD = 5.0V.

2. Video signal levels. Black clip on video can be avoided by forcing black level to blanking + 0.1V.

3. At maximum exposure (full field).

4. At minimum exposure (1/40,000th field).

5. Contribution as a multiple of saturation, at 25°C, 20ms integration time.

6. Referred to saturation level, excluding clock breakthrough.

7. Overexposure factor causing contribution of 6.5% of saturation at a diode 15 pixels vertically from centre of bright spot of diameter 10 pixels. At max. exposure and 6 MHz pixel rate.



## 7.5 Remaining problems

The design has proven to be successful. However, there are still several problems to be solved. The main points are:

- the fixed-pattern vertical stripes haven't been completely eliminated;
- the total gain is not high enough;
- the  $\gamma$  correction effect is weak;
- when the picture is dark, a variable single bright vertical bar appears.

The causes of these effects, along with possible ways to cure them, are discussed in the next chapter.

## 7.6 Chapter summary

In order to verify the techniques developed, a single-chip CMOS video camera chip has been designed and fabricated. A miniature camera has been built using this chip. The design, with its main features and performance introduced in this chapter, has proven to be successful and all the main functions work well.

The aims of achieving good picture quality and incorporating sensors and control logic on one chip have been substantiated. The device has shown significant reduction in size, cost, and power consumption as compared with CCD image sensors.

However as indicated above, there still remain areas for improvement which will be discussed in the next chapter.

## Chapter 8 Future Research Opportunities and Conclusions

It is clear from the characterization of ASIS-1011 that further research is required in the areas of circuits design and architecture, in order to solve the remaining problems and improve the performance. This chapter discusses the possible causes of performance limits and the methods of improvement, and then gives the conclusions of this thesis.

### 8.1 Future research opportunities

#### 8.1.1 Further reduction of fixed pattern noise

The remaining vertical stripes are mainly due to interference from the digital power supply coupling noise to the analogue part. The main component of this digital noise is due to the turn over of the counters and is repeated in the same place on each line. For the design of ASIS-1011, we have carefully separated the digital and analogue power supplies and tried to make the analogue supplies as “clean” as possible in order to minimize interference. However, there is interference through the substrate, for which we have little control in the present technology.

We also found that the routing of power supplies and critical analogue signals of PCB are as important as internal routing. The critical routings include: VRT, VCL, AVO, BCK, and the analogue power supplies. These pads have to be carefully decoupled.

ASIS-1011 is fabricated using a single N well technology, in which N wells can be powered individually but the P substrate is the common to both digital and analogue parts. In the latter designs, twin-tub processes are recommended so that both N and P wells can be powered individually. Fortunately, the scaled down technologies (say, below 1  $\mu\text{m}$  technology) usually are twin-tub processes.

On the circuit side, it will be helpful if the current spikes of digital counting are reduced. One solution to this is to use gray-code counters to minimize switching current on



adjacent transitions. Another solution is to use shift registers as the timing reference instead of flip-flop counters.

### 8.1.2 High gain

The range of gain is right for normal lighting conditions but needs improving for low-level light sensitivity.

Referring to Chapter 3, the gain of the first sensing stage and the second stage are determined by the ratio of capacitors. The gain will be improved if the integration capacitors ( $C_{int1}$ ,  $C_{int2}$ ) are reduced. However, the parasitic capacitance of inverter transistors will then dominate. The parasitic capacitance is due to the overlap of gate (poly) to the drain (diffusion), which is proportional to the width of transistors. For ASIS-1011, the parasitic capacitance is about 30 fF.

For the applications where high gain is required, we suggest that the width of inverter transistors is reduced and just the parasitic capacitance is used as integration capacitor. The smaller transistors will need longer balance and sample times. This is the consequent design compromise.

### 8.1.3 Better $\gamma$ correction

The  $\gamma$  correction scheme described in chapter 6 works but the effect is weak, especially at the black signal end which is not expanded well. The result is that picture details are lost at the black end of the range.

The weak  $\gamma$  correction can be explained by reviewing the circuit shown in Figure 6. 7. The correction is achieved by feedback from the input of the output buffer (gate of M3), through M15 - M17, to the gate of M4. When the input is high (corresponding to a white signal), the feedback makes node B lower, compressing the signals in the white end. However, during the black signal end, the feedback is not active because transistor M15 does not turn on until the input voltage is beyond its threshold voltage. Therefore, there is no effect for signals at the black end.

To solve this problem, the circuitry should be modified so that feedback has effect for whole range of signals. We expect that signals at white end should be further compressed and signals at the black end are relatively expanded.

Another solution might be to let the MDAC load transistors work in their saturation instead of linear region. The gates of selected bit transistors could be connected to their drains, as shown in Figure 8.1. Simulation of this shows better results than for the circuit shown in Figure 6.6.

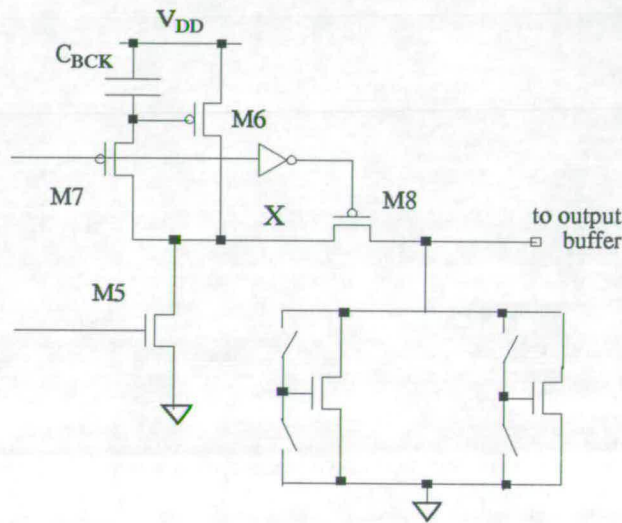


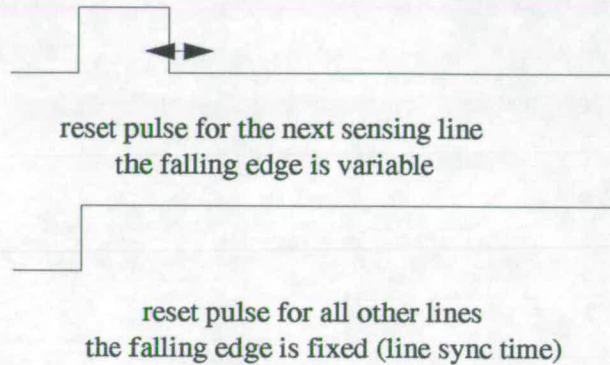
Figure 8.1 A solution to improve  $\gamma$  correction

#### 8.1.4 Single bright vertical bar

When the picture is dark, a variable single bright vertical bar appears. We believe the bar is caused by the turn over of the driving gates of the vertical shift registers. When the lighting condition is bright, the exposure will be reduced to be less than a line time. For this situation, all lines will be reset simultaneously and the reset can finish at any time during line time. When reset finishes, all driving gates of the vertical shift register will turn off, causing a voltage drop on the analogue power. This drop will make the balance value of the second sensing stage lower and a particular pixel value will be lower when it goes through this sensing stage.



To overcome this problem, we can modify the exposure control scheme. When exposure is less than a line time, we will make the reset time variable only for one line which will be read after the sample line. All other lines will be reset for whole line times, this means that most of the driving gates will turn off during the line sync time. It will not effect the pixel readout. The Figure 8.2 shows the different reset pulses.



*Figure 8.2 different reset pulses*

To implement this modified exposure scheme, the vertical encode circuit (Figure 5.4) has to be modified.

## 8.2 Conclusions

This thesis has covered the basic technique for CMOS image sensor design and techniques for enhanced on-chip camera functions which are required by smart vision applications. The work involved in this project has shown that the quality images can be obtained by carefully designed sensors implemented in a standard ASIC CMOS process, with the following advantages:

- greatly reduced size through a very high level of integration.
- greatly reduced power consumption.
- greatly reduced cost.

We have put digital control logic such as automatic exposure control, automatic gain control, and TV formatting on chip to form a single chip video camera. Because these digital logic functions still occupy only a fraction of chip area, there is no reason why we can not encompass more elements of imaging systems on the same chip to achieve powerful “smart” sensors.

Our single chip camera has achieved low power consumption and low cost. These factors will become more important for system applications. It is feasible to expect system cost reductions of 90% by integration of more functions on chip.

These advantages are relevant to many applications in the vision marketplace, but nowhere so much as in personal computing and telecommunications, where multimedia applications are growing. We conclude by giving two multimedia examples [Denyer, 1993]: a PC still camera peripheral, and a fully-integrated sensor/compressor videophone device. These both illustrate the potential for all-CMOS video systems. In addition to integrating the camera function, most of the remainder of the system may in principle be included on chip. The only off chip components needed are those that are not physically realisable in an ASIC CMOS process (e.g. clock crystal) or quantities of RAM which are more economically provided by commodity parts.

<i>system</i>	<i>Potential on chip functions</i>	<i>off chip functions</i>
PC camera peripheral	Sensor	5v Regulator
	Exposure Control	Crystal
	Gain Control	RAM
	A/D	Decoupling
	RS232 Format	RS232 Driver
	RAM Control	
videophone	Sensor	5v Regulator
	Exposure Control	Crystal
	Gain Control	RAM



A/D	Decoupling
Display Format	Comm. Driver
Comm. Format	Disp. driver
Compress/Decompress	Display
Block Format	

Before finishing this thesis, I would like to conclude that, with the progress of our project, the three technical barriers which most greatly influence new product development: cost, power consumption and size can be all dramatically reduced in comparison to today's solid-state camera technologies. We see a new capability that extends the CMOS ASIC marketplace in a sector of high growth rates, and expect it to be substantial and likely to change the nature of the vision market fundamentally.

However, in order to make this happen more work is needed. The most important issues are reducing fixed pattern noise further and increasing sensitivity at the same time as achieving smaller pixel size and higher resolution. These improvements are required, not only to compete with CCD in every aspect of performance, but also to be prepared for future HDTV system and related vision applications.

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## Appendix 1

### HPICE Simulation input files:

#### *file 1:*

\*\*\* This is the simulation of the first sensing stage (black input) \*\*\*

.width in=80 out=80

M11 2 21 0 0 N1 L=8.0U W=18U

M21 2 21 3 3 P1 L=8.0U W=18U

M31 21 23 2 0 N1 L=1.6U W=2.4U

M41 21 24 25 0 N1 L=1.6U W=2.4U

Cpix 25 0 .04PF

Cint1 2 21 .025PF

Cine1 21 0 2.5PF

Chld 2 0 0.16P

Vdd 3 0 5

Vbal 23 0 pwl(0 5 100N 5 150N 0 1U 0)

Vsel 24 0 pwl(0 0 150N 0 200N 5 1U 5)

.TRAN 50N 1U

.PRINT TRAN V(21) V(2)

.MODEL N1 NMOS LEVEL=6 UPDATE=1 TLEV=1 XL=-0.35U WDEL=0.0U LATD=0.1U

+ VTO=0.85 TOX=250 BETA=83E-6 GAMMA=0.73 VBO=1.6 LGAMMA=0.4 CLM=3 MOB=3

+ RSH=55 WIC=0 WEX=0 NSS=0 NFS=0 BEX=-1.6 TCV=-1.2M XJ=0.4U MCL=1

+ KCL=1.5E-2 VSH=1.3 KA=1 MAL=0.27 NSUB=1.5E+16 LAMBDA=1.5E-5 MBL=0.72

+ DND=1E+20 NWE=1E-10 NWM=4E-4 SCM=2.4 FDS=1E-3 UFDS=0 VFDS=0 F1=0.14

+ UEXP=0.33 NU=1 ECRIT=80K KU=5.2 VF1=0 KL=0 F4=1 UTRA=0.1 VMAX=0 CJ=130U

+ MJ=0.53 CJSW=620P MJSW=0.53 PB=0.68 CGDO=320P CGSO=320P JS=2U

.MODEL P1 PMOS LEVEL=6 UPDATE=1 TLEV=1 XL=-0.35U WDEL=0.0U LATD=0.025U

+ VTO=-1.07 TOX=250 BETA=33E-6 GAMMA=0.50 VBO=0.46 LGAMMA=0.8 CLM=3 MOB=3

+ RSH=75 WIC=0 WEX=0 NSS=0 NFS=0 BEX=-1.6 TCV=1.7M XJ=0.5U MCL=0.1

+ KCL=0.21 VSH=2.2 KA=1.1 MAL=1.3E-2 NSUB=2.0E+16 LAMBDA=8E-6 MBL=0.50

+ DND=1E+20 NWE=6E-8 NWM=0 SCM=3.1 FDS=0.44 UFDS=0 VFDS=0 F1=0.41

+ UEXP=0.50 NU=1 ECRIT=200K KU=2.0 VF1=0 KL=0 F4=0.93 UTRA=0.1 VMAX=0 CJ=490U

+ MJ=0.46 CJSW=590P MJSW=0.46 PB=0.78 CGDO=320P CGSO=320P JS=10U



.END

**file 2:**

\*\*\* This is the simulation of the first sensing stage (white input) \*\*\*

```
.width in=80 out=80
M11 2 21 0 0 N1 L=8.0U W=18U
M21 2 21 3 3 P1 L=8.0U W=18U
M31 21 23 2 0 N1 L=1.6U W=2.4U
M41 21 24 25 0 N1 L=1.6U W=2.4U
Cpix 25 0 .04PF
Cint1 2 21 .025PF
Cln1 21 0 2.5PF
Chld 2 0 0.16P
Vdd 3 0 5
Vbal 23 0 pwl(0 5 100N 5 150N 0 1U 0)
Vsel 24 0 pwl(0 0 150N 0 200N 5 1U 5)
.TRAN 50N 1U
.PRINT TRAN V(21) V(2)
*** model omitted *****
.END
```

**file 3:**

\*\*\* This is the simulation of the second sensing stage (black input) \*\*\*

```
.width in=80 out=80
M11 22 1 0 0 N1 L=8.0U W=68U
M21 22 1 3 3 P1 L=8.0U W=68U
M31 1 23 22 0 N1 L=1.6U W=2.4U
M41 1 24 25 0 N1 L=1.6U W=2.4U
Chld 25 0 0.16P
Cint2 22 1 .04PF
Cln2 1 0 2.5PF
Vdd 3 0 5
Vbal 23 0 pwl(0 5 100N 5 150N 0 1U 0)
Vsel 24 0 pwl(0 0 150N 0 200N 5 1U 5)
```

```
.TRAN 50N 1U
.PRINT TRAN V(1) V(22)
.*** model omitted *****
.END
```

**file 4:**

```
*** This is the simulation of the second sensing stage (black input) ***
.width in=80 out=80
M11 22 1 0 0 N1 L=8.0U W=68U
M21 22 1 3 3 P1 L=8.0U W=68U
M31 1 23 22 0 N1 L=1.6U W=2.4U
M41 1 24 25 0 N1 L=1.6U W=2.4U
Chld 25 0 0.16P
Cint2 22 1 .04PF
Cln2 1 0 2.5PF
Vdd 3 0 5
Vbal 23 0 pwl(0 5 100N 5 150N 0 1U 0)
Vsel 24 0 pwl(0 0 150N 0 200N 5 1U 5)
.TRAN 50N 1U
.PRINT TRAN V(1) V(22)
.*** model omitted *****
.END
```

## Appendix 2

### ASIS-1011 Pads List:

VDD	Digital power.
VD1	Analogue power (array and column sense amplifiers).
VD2	Analogue power (output amplifier and buffer).
VD3	Analogue power (row access drivers).
GND	Digital ground.
GN1	Analogue ground (array and column sense amplifiers).
GN2	Analogue ground (output amplifier and buffer).
GN3	Analogue ground (row access drivers).
VRT	Pixel reset level. Drive externally.
CVO	Composite video output.
PVB	Pixelvalid(bar)clockoutput. Used for external image capture. Video signal should be sampled on falling edge of PVB. (Valid over 312 x 287 pixels).
HLD	Input pad to hold exposure. Freezes the current internal exposure value. HLD=1 to enable continuous automatic exposure evaluation.
AGC	Input pad to enable AGC circuit. AGC = 0 to inhibit AGC function. The AGC circuit requires automatic black-level calibration for correct operation.
FST	Field-start output. Used for frame grabbing.
ITS	Input pad to select integration threshold. Controls sensitivity parameter in automatic exposure control algorithm. Typically ITS = 0, selecting the larger gap in the integration threshold algorithm.
CPE	Input pad to enable central 256 x 256 pixel output clock on TAE pad when CPE = 0.

<b>TAE</b>	Test output from auto-exposure and gain computer when CPE = 1. Central pixel output clock when CPE = 0.
<b>SYN</b>	Frame synchronization input, active on falling edge.
<b>CKI</b>	Oscillator input pad.
<b>CKO</b>	Oscillator output pad.
<b>MAX</b>	Input pad to force maximum exposure when MAX = 1.
<b>IBC</b>	Input pad to inhibit black-level calibration when IBC = 1. Auto black-level calibration must not be inhibited if AGC circuit is in operation.
<b>VCL</b>	Analogue input pad to provide sense amplifier calibration voltage.
<b>ITT</b>	Precharge word line test input. Active low.
<b>TOP</b>	Word line test output.
<b>TS1</b>	Input pad enable bit line test vector 1 (101010... is forced onto bit lines).
<b>TS2</b>	Input pad to enable bit line test vector 2 (010101... is forced onto bit lines).
<b>INI</b>	Input pad to initialises the device when high.
<b>PCLK</b>	Pixel clock input for horizontal shift register.
<b>LS</b>	Input to horizontal shift register. Starts horizontal scan.
<b>CVI</b>	Line clock input (to vertical shift register), also balances column sense amplifiers.
<b>FI</b>	Input to vertical shift register. Duration determines coarse exposure time.
<b>RST</b>	Resets photodiodes in selected row(s). Duration determines fine exposure time.
<b>SAM</b>	Control input to sample column sense amplifiers.
<b>REBIT</b>	Resets bit-lines to alleviate antiblooming outside sensing period.
<b>CAL</b>	Input enables calibration of column sense amplifiers.

GB[1:7]	MDAC input coefficient in output stage. Active low. MSB is GS7.
SS	Input selects sync level at AVO.
SI	Input selects sensor output (video) at AVO.
	<i>N.B. Blanking level appears at AVO when SS,SI = 0.</i>
BRE	Input enables automatic black-level calibration.
IBC	Inhibit automatic black level calibration, use BCK instead.
BCK	Analogue black level adjustment. Nominal value (1.5 v) set within part 1, but may be overridden externally when IBC = 0.
LOG	Selects linear analogue output characteristic (1 -> gamma = 1.0) or gamma-corrected (0 -> gamma = 2.1).
VWT	Threshold for very white pixels. Nominal value (2.15 v for gamma, 1.6 v for linear) set within part 1, but may be overridden externally.
VBT	Threshold for very black pixels. Nominal value (1.86 v) set within part 1, but may be overridden externally.
CPO	Very white pixel comparator output. CPO=1 when sensor output > VWT.
VBP	Very black pixel comparator output. VBP=1 when sensor output < VBT.
GC1	Gain control for the first sensing stage.
GC2	Gain control for the second sensing stage.

## Appendix 3

### PUBLICATIONS:

The following is a list of the papers published during the course of this PhD. The papers have not been included to keep the size of the thesis down, but the papers are available if required.

P.B.Denyer, D.Renshaw, G.Wang, and M.Lu, "CMOS Image Sensors for Multimedia Applications", *Proc. IEEE CICC 93*, San Diego, 11.5.1

G.Wang, P.B.Denyer, D.Renshaw, and M.Lu, "A Simple Solution for Image Sensor Test", *Proc. ISIC-91*, Singapore, pp.202-205.

G.Wang, P.B.Denyer, D.Renshaw, and M.Lu, "CMOS Video Cameras", *Proc. EURO ASIC 91*, Paris, pp.100-103.

This paper won the "*Best Circuit Award*" in the conference.

M.Lu, G.Wang, D.Renshaw, and P.B.Denyer, "On-chip Automatic Exposure Control Technique", *Proc. ESSCIRC'91*, pp.281-284.

This paper won the "*Best Paper Award*" in the conference.

D.Renshaw, P.B.Denyer, M.Lu, and G.Wang, "A Single-chip Video Camera with On-chip Automatic Exposure Control", *Proc. ISIC-91*, Singapore, pp.346-349.

P.B.Denyer, D.Renshaw, G.Wang, M.Lu, and S.Anderson, "On-chip CMOS Sensors for VLSI Imaging Systems", *Proc. VLSI 91*, Edinburgh, pp.4b1.1-1.10

S. Anderson et al. and G.Wang, "A single chip sensor and image processor for fingerprint identification", *Proc. IEEE CICC 91*, San Diego, 7.3.

D. Renshaw, P.Denyer, G.Wang, & M. Lu, "ASIC Vision", *Proc. IEEE Custom Integrated Circuits Conference*, 1990, pp 3038-3041.

D. Renshaw, P.Denyer, G.Wang, & M. Lu, "ASIC Image Sensors", *Proc. IEEE International Symposium on Circuits and Systems*, 1990, pp 7.3.1-7.3.4.