Developments in manufacturability of ferroelectric liquid crystal on silicon microdisplays

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I wish to thank all those who have believed in me over the years, Clare, my parents, Karine and her family, Margaret and Helen.

In humble memory of Hugh and Rafael.

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Declaration

I declare that the composition of this thesis, and all the work described within, has been carried out by myself, except where otherwise acknowledged.

Abstract

Exploiting the advantageous properties of Ferroelectric Liquid Crystals (FLCs) in Liquid-Crystal-on-Silicon (LCoS) microdisplay devices has proved very challenging for several reasons. Means of controlling the small cell gap required for optimum electro-optical performance (typically around 0.8 μm) even across the small active area of such displays had to be developed. Improving the compatibility of the silicon chip with this particular liquid crystal configuration and its intrinsically high susceptibility to cosmetic defects was also required. This thesis presents some process development work aimed at solving these issues.

An advanced post-processing procedure for the preparation of silicon backplanes relying on the use of chemical mechanical polishing (CMP) has been employed to prepare realistic sample surfaces for studying the resulting topography on the liquid crystal layer.

A process sequence for producing integrated peripheral spacer structures on silicon backplanes is presented and its compatibility with ferroelectric liquid crystals assessed.

The use of thin films deposited on the back of silicon wafers for flattening the silicon chip in order to improve the cell gap uniformity across the device was demonstrated. It is also shown that patterning of this stress compensation layer offers the possibility of controlling the symmetry of its flattening effect. Such option is advantageous in terms of the additional latitude it provides in terms of IC design.

Successful alignment of ferroelectric liquid crystals in glass test cells and within microdisplay envelopes was achieved by weak rubbing of a polyimide layer. The effect of the backplane topography brought by various post-processing strategies was investigated under such alignment conditions. The dynamic switching angle and switching time of the systems fabricated were found to be suitable for microdisplay operation. The effect of alignment layer thickness on the electro-optical properties is also studied.

Non-contact alignment methods based on the use of photopolymers were evaluated. Such materials proved very promising both in terms of the cosmetic aspect of the alignment achieved and the resulting electro-optical properties.

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Abbreviations

AFM	Atomic Force Microscopy
AM-LCD	Active Matrix Liquid Crystal Display
a-Si	Amorphous Silicon
BS	Beam Splitter
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing
CRT	Cathode Ray Tube
CVD	Chemical Vapour Deposition
DMD	Digital Micro-mirror Device
DOP	Degree of Planarisation
DRAM	Dynamic Random Access Memory
ECR	Electron Cyclotron Resonance
FLC	Ferroelectric Liquid Crystal
FLCoS	Ferroelectric Liquid Crystal on Silicon
HMD	Helmet Mounted Display
IC	Integrated Circuit
ITO	Indium Tin Oxide
LC	Liquid Crystal
LCD	Liquid Crystal Display
LCoS	Liquid Crystal on Silicon
LED	Light Emitting Diode
LEP	Light Emitting Polymer
LPCVD	Low Pressure Chemical Vapor Deposition
LPUV	Linearly Polarized UV
LSB	Least Significant Bit
MEMS	Micro-Electro-Mechanical Structure
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NLC	Nematic Liquid Crystal
NW-TN	Normally White Twisted Nematic

OLED	Organic Light Emitting Diode
OLEDoS	Organic Light Emitting Diode on Silicon
PBS	Polarising Beam Splitter
PCM	Pulse Coded Modulation
PDP	Plasma Display Panel
PECVD	Plasma Enhanced Chemical Vapour Deposition
PI	Polyimide
PM-LCD	Passive Matrix Liquid Crystal Display
p-Si	Polycrystalline Silicon
PWM	Pulse Width Modulation
RGB	Red Green Blue
RIE	Reactive Ion Etching
RPTV	Rear Projection Television
sccm	Standard cubic centimetre per minute
SOI	Silicon on Insulator
SRAM	Static Random Access Memory
STN	Super Twisted Nematic
SSFLC	Surface Stabilized Ferroelectric Liquid Crystal
TFT	Thin Film Transistor
TN	Twisted Nematic
UV	Ultra-Violet
VAN	Vertically Aligned Nematic

Chapter 1. Introduction

1.1 The future of information displays

The last thirty years have seen a digital revolution where microelectronics based devices have become available to a larger public. Nowadays in the age of broadband Internet, digital imaging, digital television and mobile telephony manufacturers are faced with incorporating high-resolution displays into a variety of consumer products. For some of these products, portability is an extra requirement translating into the need for low power consumption and reduced size and weight.

Cathode Ray Tube (CRT) technology [1] remains to date the most successful high-information-content direct-view display technology. Despite numerous ingenious developments over the years it is the physics underlying the reliability and cost-effectiveness of CRT technology that will eventually bring about its downfall. CRTs are bulky, heavy and some might say "ugly". Thinner direct-view display technologies such as Plasma Display Panels (PDPs) and Liquid Crystal Displays (LCDs) are now challenging the CRT's monopoly.

A new category of display devices known as microdisplays has emerged over the last two decades. The term "microdisplay" describes devices less than one inch in diagonal and capable of TV/video quality or better. As a direct result of their small geometry the image these devices produce must be magnified for presentation to the user. Microdisplay technologies discussed in this work utilise silicon based microelectronics and more particularly Complementary Metal-Oxide Semiconductor (CMOS) technology.

As will be described in section 1.3.2, CMOS based microdisplays find applications in a wide range of products. One of the main driving forces behind the use of small imagers is to reduce the cost of the whole display systems when compared to more common technologies such as CRTs, PDPs and LCDs. Image/video quality (contrast, resolution and frame rate) is also expected to benefit from this new approach. In addition, their "postage stamp" size and intrinsic lower power consumption are perfectly suited to their incorporation into a new range of lightweight portable products.

As illustrated in section 1.3, the various microdisplay technologies that have emerged over the last two decades are based on different principles. This thesis will focus on a technology that employs the light modulation capability of a certain type of liquid crystal material often referred to as Ferroelectric Liquid Crystal (FLC). Because it combines FLC and CMOS, this technology is often referred to as Ferroelectric Liquid Crystal on Silicon (FLCoS) microdisplays.

1.2 Liquid crystal displays: historical and technological overview

1.2.1 From liquid crystals to displays

It all started when, in 1888, the Austrian botanist F. Reinitzer reported on the peculiar thermal behaviour of an ester of cholesterol commonly found in plants and animals [2]. Upon heating from the solid state the substance appeared to exhibit two melting points, first turning into a cloudy liquid at 145 °C then into a clear liquid at 178 °C. With the assistance of O. Lehmann and his "crystallisation microscope" this peculiar behaviour could be confirmed [3]. Despite some initial degree of controversy Reinitzer and Lehmann rightly linked this behaviour to the existence of intermediate phases (mesophases) exhibiting some degree of ordering combined with fluid-like behaviour of isotropic liquids. This type of substance was baptised "liquid crystals" (LCs).

The unique structure of liquid crystals (LCs) is at the origin of its modern use in display application. LCs are anisotropic materials with some degree of molecular ordering. This molecular anisotropy results in birefringence or optical anisotropy which can be exploited to alter the properties of the light passing though it.

Birefringence of liquid crystals is dependent on the organisation of the molecules relative to the direction of the polarisation of light. In addition, the level of molecular ordering is not fixed as in solids. The fluid-like behaviour of liquid crystals permits, through the motion of their molecules, to control their optical properties by using external influences such as an electric field. The nature of liquid crystals (molecular structure and phases) strongly affects both their optical properties and the way they behave in an electric field. The mesomorphic behaviour and electro-optical properties of liquid crystals and more particularly those of FLCs will be described in more detail in chapter 2.

Despite the early discovery of LC materials , one had to wait eighty years to see the appearance of the first viable LCDs, at the time in products such as pocket calculators and wristwatches. Man-made thermotropic liquid crystals appeared rapidly after Reinitzer and Lehmann's discovery with the synthesis of azoxybenzene compounds by L. Gatterman [4] in 1890. However their poor chemical stability and the absence of liquid crystalline behaviour at room temperature prevented their use in displays. In the 1960s, G. Heilmeier's team at RCA laboratories (New Jersey, USA) proposed and demonstrated the feasibility of liquid crystal based displays by developing devices based on the dynamic scattering effect [5] and the guest host effect [6]. Such activities led to an increasing interest in liquid crystal technology which resulted, in 1969, in the synthesis of the first room temperature LC material suitable for scattering effect based displays by Kelker, Schuerle and Minihg [7]. A few years later, another major breakthrough took place when G. Gray developed cyano-biphenyl materials [8], which proved to be the first commercial quality LC materials suitable for display application. The race to fabricate commercially viable LCDs could then start.

1.2.2 LCDs in practice

1.2.2.1 The TN cell

Many LC display configurations have been developed in order to maximise the electro-optical performances achievable. The so-called twisted nematic mode (TN) is

one, if not the most common, mode employed in LCDs nowadays. The use of the TN cell for display application was proposed in 1971 by W. Helfrich and M. Schadt [9]. As illustrated in figure 1.1, it employs nematic LC materials with positive dielectric anisotropy to control the polarisation of light passing through the LC cell. Transparent electrically conductive electrodes are employed to apply the electric field across the LC layer.
They typically consist of Indium Tin Oxide (ITO) film deposited onto a glass substrate (figure 1.1c). An alignment layer is deposited onto the substrates. Its purpose is to control the orientation of liquid crystal molecules in the vicinity of the substrates, which in turn affects the molecular orientation in the bulk of the cell due to intermolecular forces.

The TN cell relies on the twist of the LC molecules generated by orthogonal alignment on the top and bottom substrates (see figure 1.1). In the absence of an electric field this molecular twist causes the polarisation direction of the light entering the cell to be rotated 90 degrees. The polarisation direction therefore coincides with that of the exit polariser (or analyser) so that light can pass through the cell. The cell looks bright (see figure 1.1a). Under the application of an electric field of sufficient amplitude ($V>V_{th}$) the twist of the molecules becomes disrupted. As the field reaches a saturation value (V_{sat}) molecules align themselves along the field direction due to their positive dielectric anisotropy. The polarisation direction of the light remains unchanged across the cell and as a result the light is blocked by the analyser (see figure 1.1b). The cell looks dark. Greyscale can be achieved by controlling the voltage applied to the cell (between V_{th} and V_{sat}) as shown in figure 1.1d.

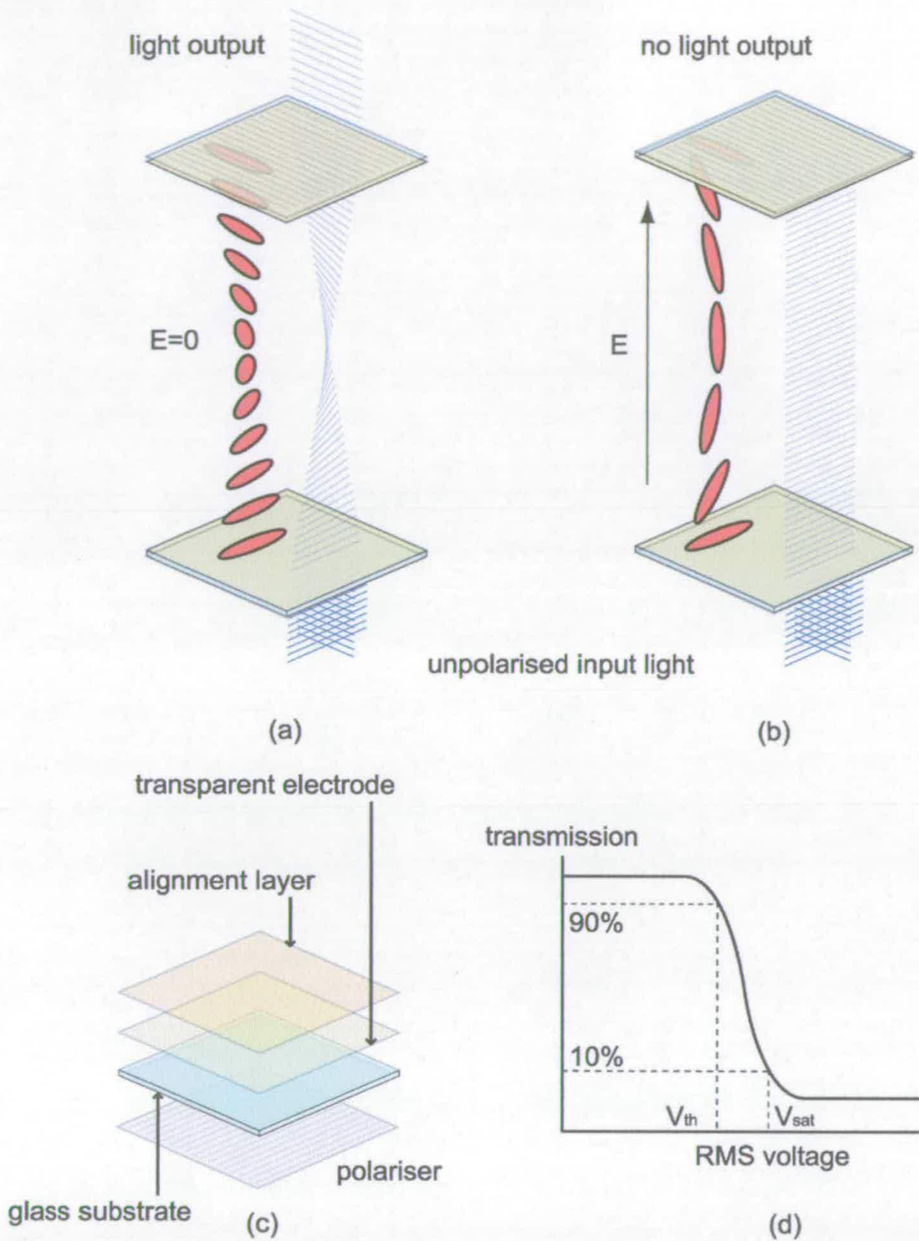


Figure 1.1: The (normally white) twisted nematic cell (NWTN). In the bright state (no field applied) the polarisation direction light is rotated and light can exit the cell (a). In the dark state when a voltage is applied to the cell the polarisation direction of light is unaffected and light is blocked by the analyser (b). Expanded view of the layers of the bottom electrode including polariser (c). Typical optical response of a NWTN cell to the rms voltage applied across the LC layer (d).

1.2.2.2 Direct addressing of LCDs

The development of liquid crystal materials and modes constitutes only one aspect of LCD technology. For any information to be displayed, modulation of light must be controlled spatially across the display device. Grey levels and colour are also necessary to fulfil modern display applications requirements. Various architectures and principles of operation have been developed to this effect over the last 30 years.

The earliest LCDs such as the ones found in wristwatches and pocket calculators represent, from today's perspective, the simplest of situations in term of achieving spatial light modulation using a liquid crystal layer. Because of the low information content displayed a method known as direct addressing can be employed. The principle behind direct addressing and the associated device architecture are illustrated in figure 1.2.

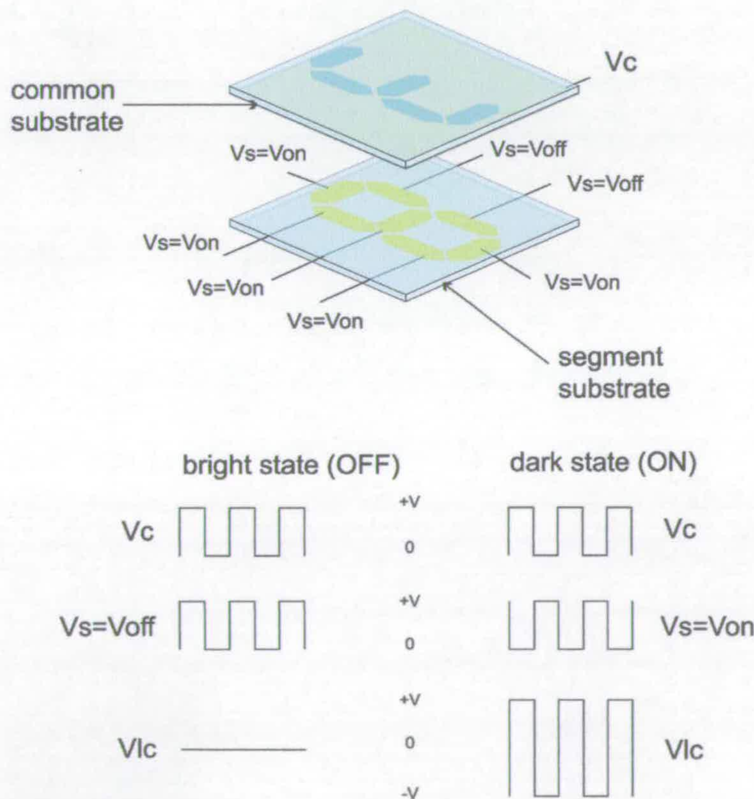


Figure 1.2: Electrode architecture and waveforms employed for direct addressing of LCDs. Vs is applied to the segment substrate and Vc to the common substrate.

The direct addressing technique requires each switching element to be individually connected to the outside electronics and power supply. As a result its use is limited to low-information-content displays.

1.2.2.3 Passive matrix addressing of LCDs

In order to produce higher resolution images using liquid crystals, a technique known as passive matrix (PM) addressing was developed. As illustrated in figure 1.3, spatially distinct switching elements (pixels) can be created in a liquid crystal cell without the need for their individual connection to the drive electronics. A matrix of pixels is created by the intersections of rows and columns deposited on the inner surfaces of the cell substrates in an orthogonal fashion.

As demonstrated by Alt and Pleshko, the optical performance of PM-LCDs is limited by the number of rows (N) being addressed [10]. The selection ratio V_{on}/V_{off} defined as the ratio between the rms ON and OFF pixel voltages is given by:

$$\frac{V_{on}}{V_{off}} = \sqrt{\frac{\sqrt{N}+1}{\sqrt{N}-1}} \tag{1.1}$$

Increasing the number of rows causes the selection ratio to decrease. As can be observed from figure 1.1d reducing the difference between V_{on} and V_{off} limits the contrast ratio achievable (i.e. the transmittance difference between the ON and OFF states). It is generally accepted that a maximum of 80 rows can be addressed using the technique described above with conventional TN materials [11].

In PM-LCDs, an image is created by scanning the pixel matrix one row at a time and supplying an adequate signal to the column lines simultaneously. As shown in figure 1.3, the voltage across the cell over a given pixel and hence the optical state of the liquid crystal can be controlled by the column signal. A pulse of fixed amplitude is used to sequentially scan all the rows of the device in order to create an image.

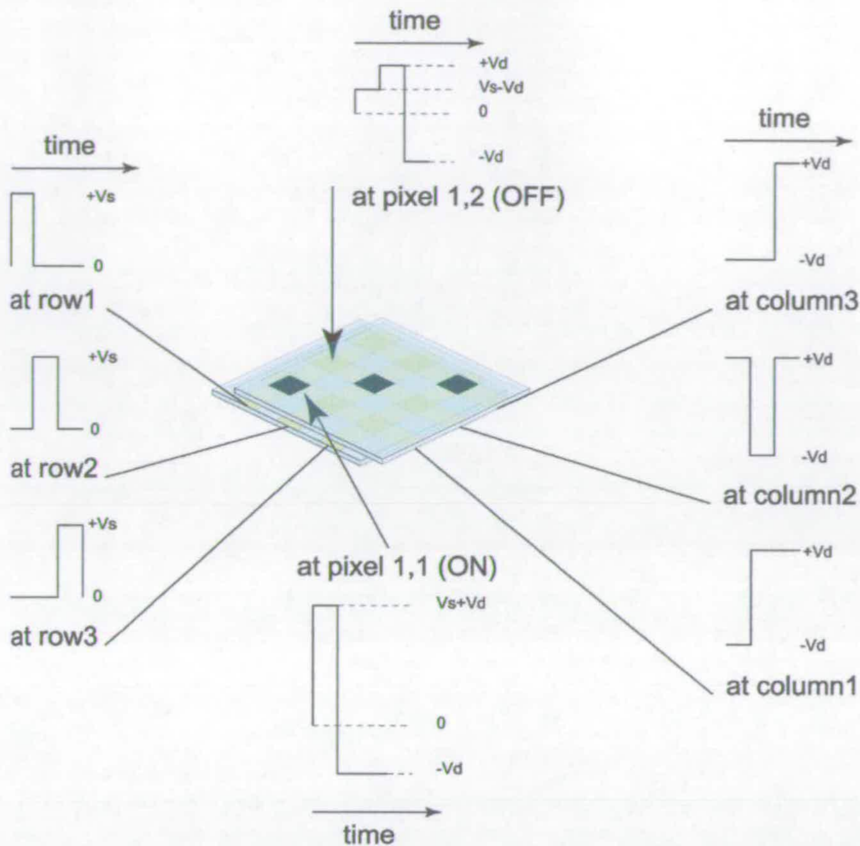


Figure 1.3: Electrode architecture and driving waveforms employed in PM-LCDs. The array of pixels is addressed row by row with the signal controlling the state of the liquid crystal layer (video data) being fed through the columns.

For a given selection ratio, the contrast ratio of a passive matrix LCD based on the TN mode can be improved by using LC materials exhibiting a higher steepness in their transfer-characteristic curve. In 1983 using computer-modelling Amstutz et al. demonstrated that a steeper transfer characteristic could be achieved using a twisted nematic configuration with an increased molecular twist (e.g. 180 and 270 degrees) [12]. Such configuration baptised super-twisted nematic (STN) was demonstrated by Scheffer and Nehring the following year [13]. In practice, a higher twist is obtained by the addition of a small amount of chiral dopant to the nematic mixture. It is important to note however, that ultimately the STN geometry obeys Alt and Pleshko's law that sees the decrease in contrast achievable with the increase in the number of lines to be addressed. Using conventional matrix architecture and STN

materials the number of lines addressable for satisfactory operation is increased to 250 [11].

In order to further increase the resolution and frame rate of PM-LCDs, the dual scan matrix architecture has been introduced [14] (see figure 1.4b). The electrical, architectural and liquid crystal related factors affecting the operation and performance of PM-LCDs are beyond the scope of this thesis. Excellent reviews of the subject can be found in the literature [15,16,17].

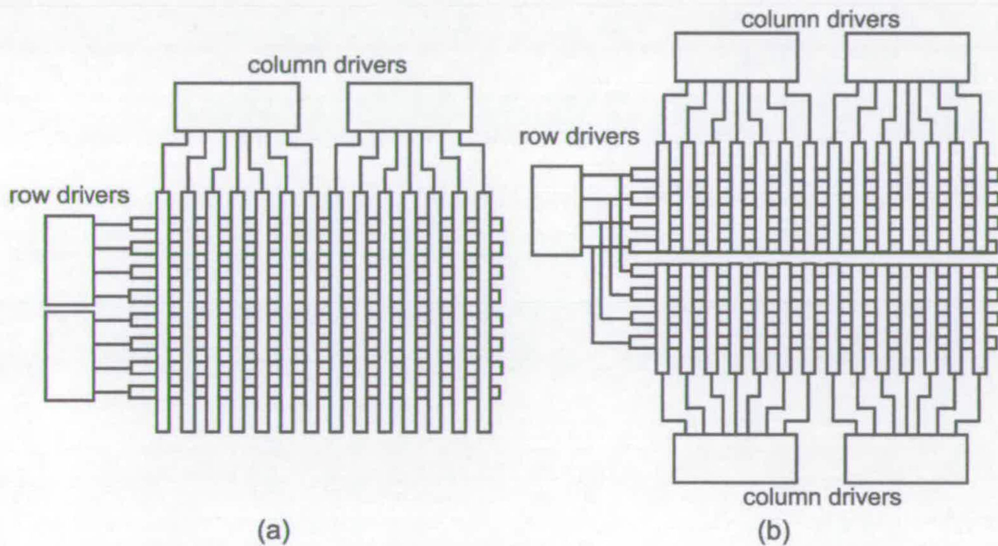


Figure 1.4: Example of matrix architectures of PM-LCDs showing the basic design (a) and one of its variations to allow dual scan addressing (b).

1.2.2.4 Active matrix addressing of LCDs

As early as 1971 Lechner proposed to integrate an active element at the pixel level to achieve the same optical contrast in high-resolution displays as with direct addressing [18]. This approach, known nowadays as active matrix (AM) addressing, eliminates the dependence of the achievable contrast on the number of rows as discussed above, hence allowing the fabrication of LCDs with a larger number of pixel elements.

The architecture of a typical AM-LCD is illustrated in figure 1.5. It comprises an array of pixels individually formed by a transistor, a storage capacitor and a pixel electrode. A row signal pulse is applied to switch all the transistors of that row to their conductive state. Simultaneously the video data assembled in the column drivers is fed in parallel to all the pixels of that same row. A storage capacitor is employed to retain the pixel charge during the rest of the frame, i.e. the time required to address all the rows one after another.

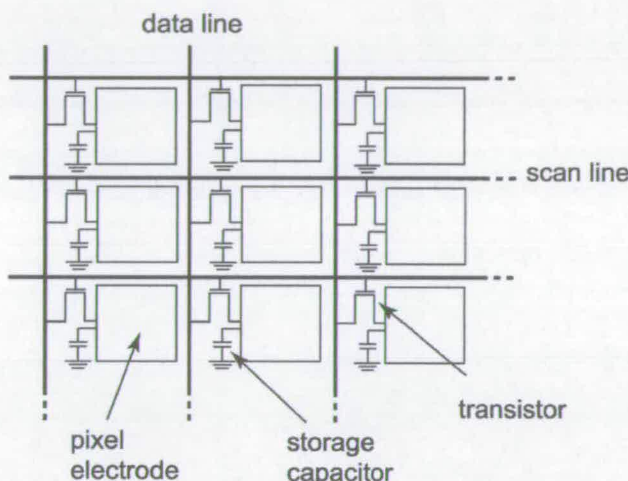


Figure 1.5: Schematic representation of the pixel array of an AM-LCD. A transistor whose state is controlled by scanning the rows permits the video data (fed in parallel through the columns) to flow towards the pixel electrode and storage capacitor.

The type of transistors employed in AM-LCDs is known as thin film transistors (TFTs) due to the fact that their fabrication required multiple deposition steps onto the glass substrate. The first AM-LCD was demonstrated by Brody in 1973 using CdSe thin film transistors (TFTs) [19]. An improved pixel technology based on amorphous silicon (a-Si) TFTs was reported by LeComber in the early 1980s [20]. It remained until recently the main transistor technology utilised in AM-LCDs and is illustrated in figure 1.6.

For faster charging of the pixel it is favourable for the on-resistance of the TFT (R_{ON}) to be as low as possible. As illustrated in equation 1.2, for a given electron mobility

(μ) and area charge density (σ) the resistance depends on the width (w) and length (l) of the channel:

$$R_{ON} = \frac{l}{\mu \sigma w} \tag{1.2}$$

The electron mobility of a-Si (around 0.5 $cm^2/V.s$) therefore dictates the size of the source-drain area. This area in turn affects the aperture ratio[1] of the display since due to the light sensitivity of a-Si, the area of the pixel occupied by the TFT must be shielded from light.

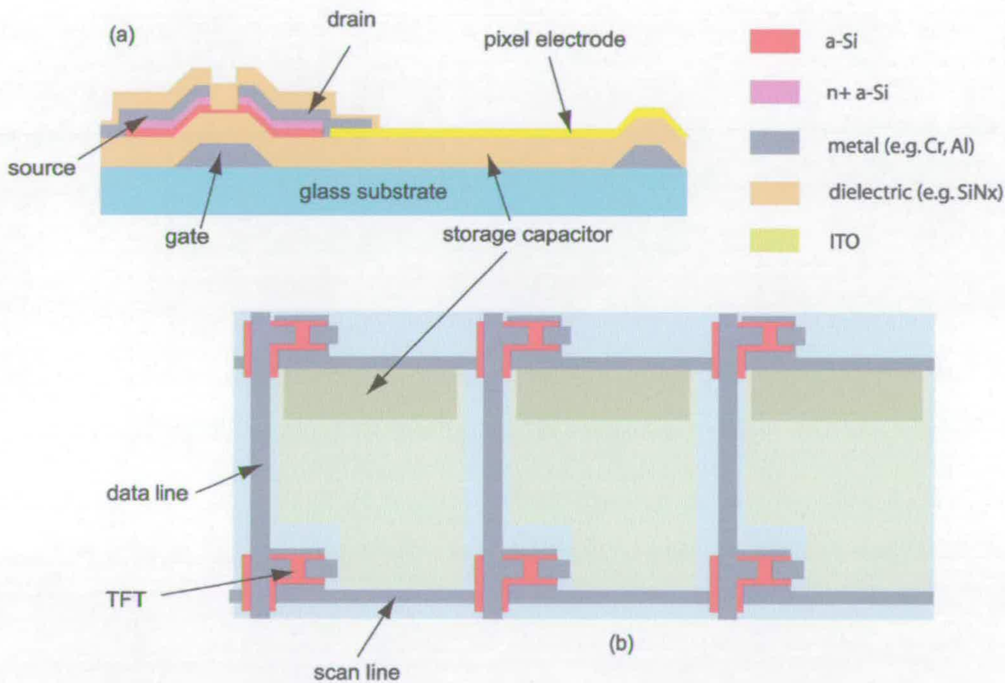


Figure 1.6: Cross section (a) and top view (b) of a "bottom gate" a-Si TFT pixel showing the various areas covered by the transistor, pixel electrode area and storage capacitor.

[1] The ratio between the total pixel area and that covered by transmissive pixel electrode

Polysilicon (p-Si) has been the subject of much interest recently from AM-LCD manufacturers. The reason for this is its higher electron mobility (200-300 $cm^2/V.s$), which can directly benefit TFT-LCD technology by allowing faster operation and larger aperture. In addition the speed of p-Si transistors permits some of the interface electronics such as row and column drivers to be fabricated onto the substrates at the same time as the addressing pixel matrix.

Polysilicon is commonly deposited using low pressure chemical vapour deposition (LPCVD) [21]. Subsequent thermal treatment is required to enhance the electrical properties of as deposited p-Si films [22]. The temperature requirements (> 600 °C) associated with these processes prohibit the use of conventional glass and require more expensive quartz substrates to be used. Recently, very promising techniques have been developed in order to produce high mobility p-Si TFT at temperatures compatible with glass substrates (< 450 °C). These consist of using excimer laser radiation to crystallise a-Si films. Annealing can be performed by laser scanning [23] or in a single step process using powerful light sources [24].

1.3 Ferroelectric Liquid Crystal on Silicon (FLCoS) microdisplays

1.3.1 The LCoS concept

In the late 1970s a new type of liquid crystal display architecture was proposed, at the time, aimed at developing portable TV applications [25,26,27]. Known as Liquid Crystal on Silicon (LCoS) it is based on the active matrix architecture similar in principle to that of TFT-LCDs but using Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) technology fabricated from single crystal silicon (x-Si).

As will be presented in chapter 3, in the case of ferroelectric liquid crystal based devices, a variety of pixel designs has been developed around the use of MOSFETs. The simplest design, commonly called the dynamic random access memory (DRAM) pixel is illustrated in figure 1.7. It consists of a single transistor and its operation is similar to that of the TFT based pixel described earlier in paragraph 1.2.2.4. One can note the intrinsic capacitance between the diffusion zone acting as storage capacitor.

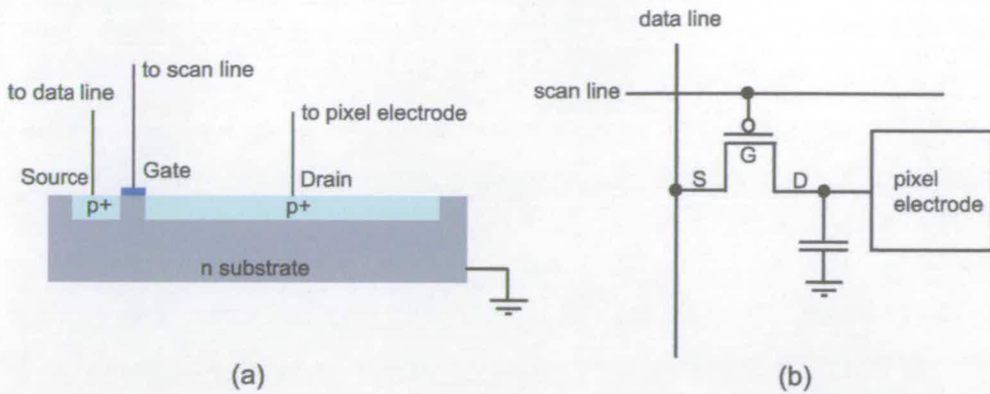


Figure 1.7: Schematic representation of the cross-section of a single MOSFET based DRAM pixel (a) and its circuit symbol equivalent in relation to the addressing of an LCoS device (b).

The high channel electron mobility (around 450 $cm^2.V^{-1}.s^{-1}$) associated with the use of single crystal silicon allows the fabrication of fast switching transistors. In practice, this means smaller pixels ranging in size from typically 20 μm down to below 10 μm. This feature allows high-resolution images to be formed over the very small area of what is better described as a liquid crystal microdisplay. The high electron mobility of x-Si also permits the fabrication of high-speed circuitry in the periphery of the active area of the device to fulfil other functions than purely addressing the pixel array.

Another advantage of using MOSFET technology is the lower fabrication cost compared to TFTs. This is due to several factors. Unlike TFTs that are fully created from several deposition processes, in MOSFETS the active area material acts also as a substrate. In addition, silicon based semiconductor technology is associated with fabrication techniques that will allow batch processing of numerous microdisplay devices.

Finally another interesting feature of using x-Si transistor technology with regard to manufacturing liquid crystal based displays is that – unlike in the case of LCDs manufacturers - the technical challenges involved in developing and manufacturing smaller or higher performance transistor geometries is left to silicon foundries rather than the LCoS displays manufacturers.

From a basic operation perspective the architecture of LCoS devices is also advantageous. Because LCoS technology is reflective in nature, it allows the pixel circuitry to be separated from the light path and hence leads to a much higher aperture ratio. As will be described later in chapter 2, when combined with fast liquid crystals, LCoS devices can be used to generate colour without the need for colour filters, therefore further enhancing the optical efficiency of the display.

1.3.2 Liquid crystal modes for LCoS microdisplays

Numerous types of liquid crystal electro-optical modes have been developed since the 1970s. A comprehensive review of these modes would be too lengthy and falls outside the scope of this thesis. Recent reviews of the LC configuration suitable for LCoS display operation [28,29,30] highlight the potential of Vertically Aligned Nematic (VAN) and 45-degree Twisted Nematic (45degTN) electro-optical modes. Some of their properties of interest with regard to LCoS display applications are listed in table 1.1.

	VAN	45degTN	SSFLC
Electro-optical response	analog	analog	binary
Switching speed	++	+	+++
Contrast ratio	+++	++	+++
Alignment sensitivity	++	+++	+
Cell gap tolerance	+++	++	+
Materials availability	++	+++	+
References	[31]	[32]	[33]

Table 1.1: Properties of VAN, 45degTN and SSFLC electro-optical modes suited for use LCoS microdisplays.

The remainder of this thesis will focus on the use of materials often referred as Ferroelectric Liquid Crystals (FLCs) in a configuration most accurately described as Surface Stabilized Ferroelectric Liquid Crystals (SSFLCs).

SSFLCs are the fastest liquid crystal mode discovered to date. Their switching speed (i.e. the time necessary to switch between two molecular orientations under the influence of an electric field) is of the order of tens of microseconds at room temperature using voltage compatible with LCoS devices. In comparison, nematic liquid crystal modes exhibit switching speed of the order of a few tens of milliseconds. As will be presented later in this thesis, faster switching time directly translates into higher frame rate, larger greyscale and colour depths.
SSFLCs exhibit bistability (i.e. the existence of two stable states of molecular orientations) which in turn leads to a binary optical response. In other words, unlike analog NLC based modes, such as VAN and 45degTN (where the optical response is proportional to the rms amplitude of the applied electric field), SSFLCs are "digital" liquid crystals. While at first sight such a feature may appear problematic in terms of greyscale generation, as will be shown later, it is very well suited to the digital nature of the LCoS architecture. Furthermore, the means by which greyscale can be achieved from a binary optical response will be presented later in this thesis where it will become obvious that the techniques employed are only practically viable because of the high switching speed of SSFLCs.
Finally, another advantage of using SSFLCs is their intrinsic large viewing angle due to the fact that field driven molecular motion takes place in a plane parallel or closely parallel to that of the polarisation optics. Most of us are familiar with earlier laptop LCDs and the drawback of limited viewing angle. On a microdisplay scale, better viewing angle directly translates into the opportunity to employ low F# optical magnification for a more compact optical system and/or higher flux illumination/collection.

1.3.3 Display applications of LCoS technology

1.3.3.1 Near-eye applications

In good ambient light, the human eye is capable of resolving image features as small as one 60th of a degree. The most instinctive way to improve resolvability of small features is to reduce the distance between the image and the eye, which then requires

to focus more closely. However there is a minimum distance the eye is able to do so, known as the "near-point" and equivalent to about 20 cm. The size of a microdisplay pixel, typically in the range of 10-20 μm therefore falls far below the limit of resolvability of the eye by at least a factor of 10 when viewed at the near point. Therefore the image from a microdisplay must be magnified for presentation to the user. As described in figure 1.8, a virtual resolvable image can be presented to the user through magnification using a single magnifier lens. A polarising beam-splitter (PBS) is employed to separate the illumination path from the viewing path and create suitable polarisation direction. An excellent review of the optics related factors affecting the image quality produced using LCoS microdisplays can be found in the literature [34].

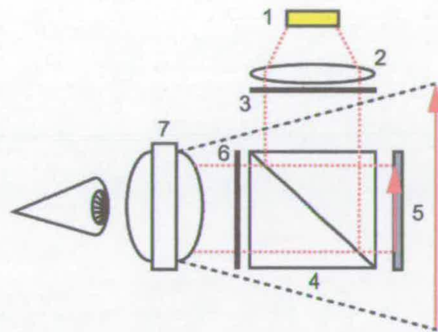


Figure 1.8: Schematic diagram of the optics employed for magnifying the image from a LCoS display for near-eye applications. 1. Illumination, 2. Collimating lens, 3. Polariser, 4. Beam-splitter, 5. LCoS display, 6. Analyser, 7. Magnifying lens.

A wide range of applications can benefit from high-resolution colour images from microdisplay modules. Viewfinders for digital cameras and camcorders are the most obvious. The incorporation of LCoS microdisplays in this area is not only motivated by size, weight and performance considerations but is also, maybe to a larger extent, driven by the lower cost and power requirements of LCoS devices compared to existing miniature LCD technologies. In addition, LCoS microdisplays can be employed as display engines in a more exotic range of products such as portable DVD players and "true internet" compatible mobile phones, where high-resolution and colour depth are prerequisite.

1.3.3.2 Projection applications

LCoS microdisplays can also be used to generate large size high-resolution images. Two configurations can be distinguished as illustrated in figure 1.9. In rear projection systems the microdisplay engine, electronics and associated optics are placed behind the screen onto which the image is projected. At the inverse, front projection systems see the image projected from the same side as the user with respect to the screen.

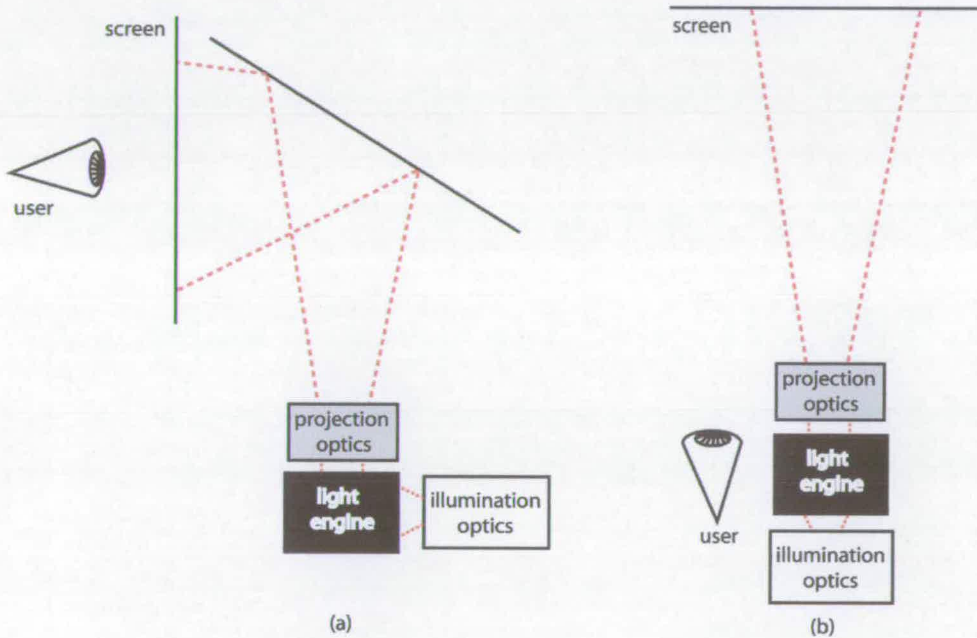


Figure 1.9: Basic configuration for rear projection (a) and front projection (b) systems.

Unlike in the case of near-eye applications, projection based products offer the opportunity to use three imagers. In order to increase brightness and performances such as frame rate and colour depth each of the three microdisplays can be dedicated to the modulation of one of the three primary colours (red, green and blue). The architecture and optics of such arrangement is illustrated in figure 1.10.

The use of several microdisplays however presents an obvious economical drawback by the fact it requires multiple imagers and also more complex optics. The high switching speed of SSFLCs makes possible the production of full colour images using a single microdisplay panel. In this case, colour separation is temporal rather

than spatial. As illustrated in figure 1.11, this is most commonly accomplished by using a colour wheel.

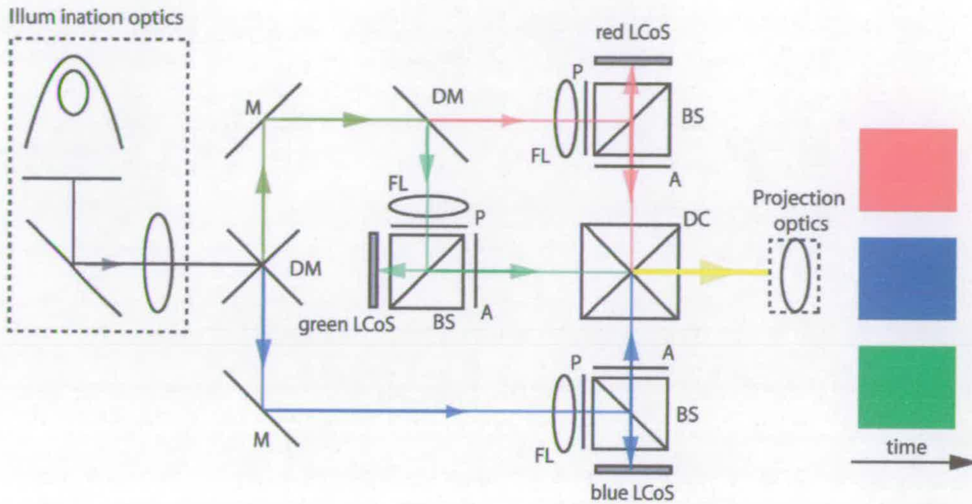


Figure 1.10: Schematic representation of the optics employed in a 3 LCoS panel projection system. L: lamp, UV: UV/IR filter, CM: cold mirror, RL: relay lens, DM: dichroic mirrors, M: mirror, FL: field lens, P:: polariser, BS: beam-splitter, A: analyser, DC: dichroic cube, PL: projection lens.

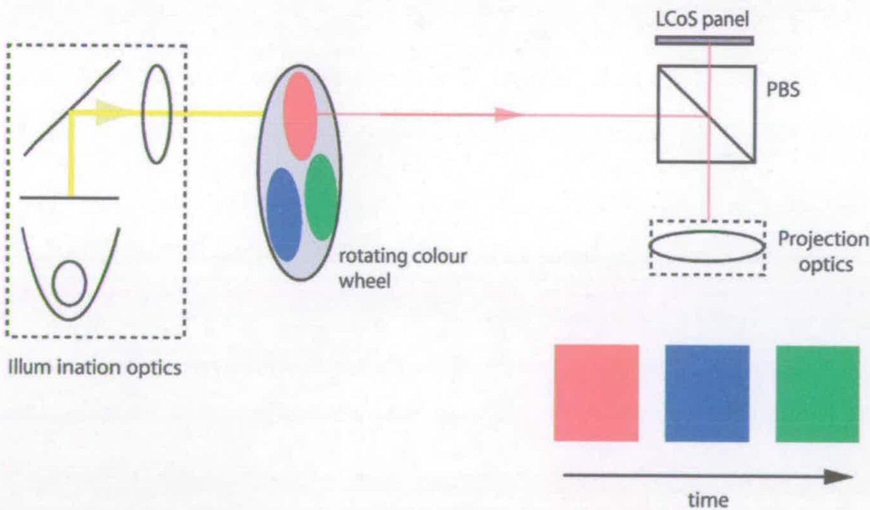


Figure 1.11: Schematic representation of the light engine optics in a single LCoS panel projection system based a rotating colour wheel which causes the LCoS panel to be illuminated sequentially with the three primary colours.

Alternatively, light scrolling illumination systems have been developed over the years where white light is split into bands of red, green and blue which can be simultaneously scanned across the display device [35, 36]. An example of such architecture based on rotating prisms developed recently by Philips is illustrated in figure 1.12.

The main microdisplay projection markets are that of Rear-Projection-Television (RPTV) and multimedia front projectors. The former is typically based on a rear projection approach while the latter employs front projection.

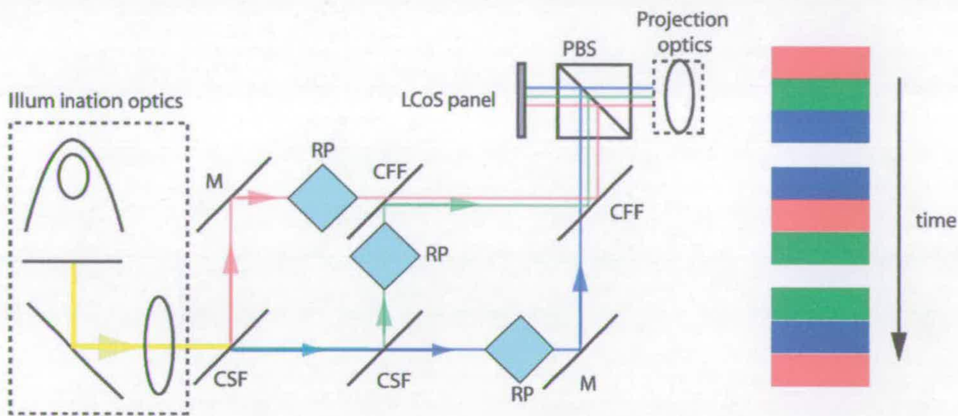


Figure 1.12: Schematic representation of the light engine optics in a single LCoS panel projection system based on rotating prisms. At all times, the display is illuminated with the three primary colours. CSF: colour separating filter, M:mirror, CFF: colour fusing filter, RP: rotating prism, PBS: polarising beam-splitter.

1.3.4 Competing microdisplay technologies

The potential of producing high-resolution images using microdisplays motivated extensive industrial and academic research activities over the last two decades. The fruits of such efforts have been several microdisplay technologies, some of which have proven to be more successful than others. This section presents the principle of operation of two of the most competitive microdisplay technologies to date, which are not based on liquid crystals. Not surprisingly, both types of devices are also based on x-Si CMOS technology.

1.3.4.1 Micromechanical microdisplays

Micro-Electro-Mechanical Structures (MEMS) can be exploited to form microdisplays. Indeed, the integration of mobile and electrically controllable structures onto a silicon chip proved to be a very efficient way of producing high-resolution images.

The most commercially successful micro-mechanical microdisplay technology has been by far the Digital Micro-mirror Device (DMD) invented by Texas Instruments in 1987 [37]. As illustrated in figure 1.13, DMDs employ tilting micro-mirrors to reflect the light shone upon them and control its direction. This is accomplished in a binary fashion with each pixel capable of tilting in one of two possible orientations (± 10 degrees). Depending on the potential of the surrounding electrodes (controlled by a CMOS circuitry) each pixel is tilted so that the reflected light is directed through the viewing optics (bright state) or towards an absorber layer (dark state). Switching between the ON and OFF states takes place in around 10 μs.

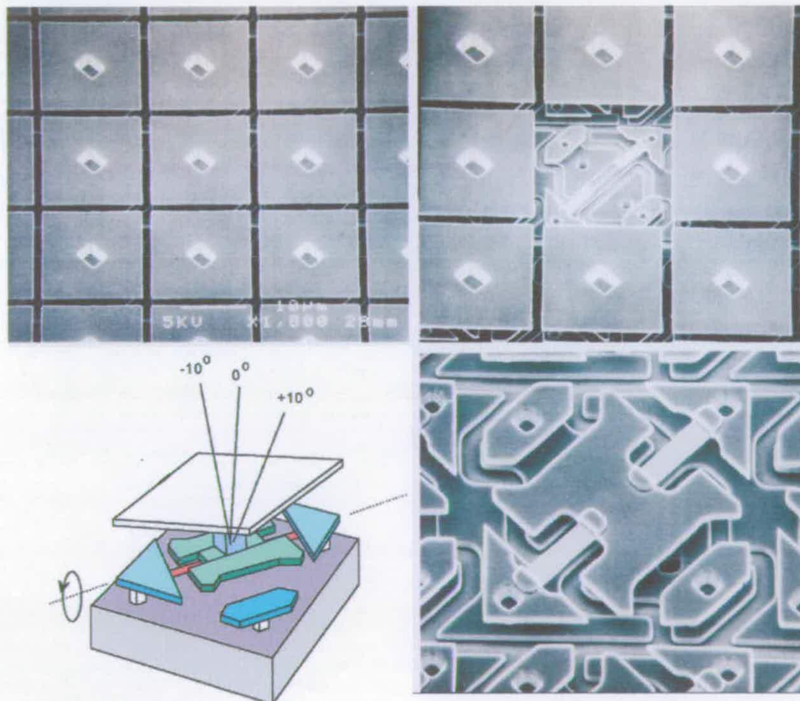


Figure 1.13: SEM pictures and schematic representation of the DMD developed by Texas Instruments. High resolution images are created by an array of tilting micro-mirrors controlled by CMOS based circuitry. From [38].

DMD technology is digital in nature, i.e. the mirrors are tilted in one of the two positions. In order to produce greyscale images, as with FLCoS devices, pulse coded modulation is employed. Basically, it consists of controlling the ratio of the time each pixel spends in one ON and OFF position. If this is accomplished at high speed, the human brain is "fooled" into perceiving shades of grey. The principle behind this method will be covered in more detail in the context of the addressing of SSFLCs in section 2.3.2.

Colour can be accomplished in two ways. A single DMD chip can be employed to create colour by being sequentially illuminated with red, green or blue light. To increase the duty cycle of the whole system three separate imagers can be employed, each being illuminated with red, green or blue. The three-chip design is capable of producing 35 trillion colours while the single imager approach produce 1.7 million colours [38].

1.3.4.2 Emissive microdisplays

A new breed of miniature display devices that shows great promise is based on Organic Light Emitting Diodes (OLEDs) [39,40]. Unlike other microdisplay technologies discussed so far, it does not require any light source as light is emitted from the device itself. A silicon backplane using an array of MOSFET based pixels is employed to control a light-emitting organic layer, so that such devices have been baptised by a few as Organic Light Emitting Diodes on Silicon (OLEDoS).

Two types of emissive materials are available. In "small molecules" materials also known as low molar mass OLEDs (LMM-OLEDs) the light is emitted from discrete molecules while Light Emitting Polymers (LEPs) rely on long chains of molecules to such effect. The latter is more favourable from a volume manufacturing perspective as the nature of LEPs is well suited to high throughput deposition techniques such as spin coating and ink-jet printing while LMM-OLEDs films are formed by vapour deposition.

The schematic cross section of a pair of pixels of an emissive microdisplay is illustrated in figure 1.14. A layer of the light-emitting material is sandwiched between an array of pixels (connected to the underlying CMOS circuitry) and a transparent electrode. Each pixel acts as a cathode where electrons are injected into the LEP stack while the common transparent electrode (typically made ITO) sees holes injection taking place. The active layers can include a hole transport layer which allows hole and electron to combine in an underlying emissive layer leading to light being generated. The wavelength of the light emitted depends on the difference in energy between the valence and conduction bands of the light emitting material. Materials emitting blue, red, green and white have been developed.

Several options exist to produce colour images using OLEDoS devices. A blanket of white-emitting material can be deposited in combination with RGB colours filters. Blue-emitting materials can also be used in a similar fashion but require red and green converters.

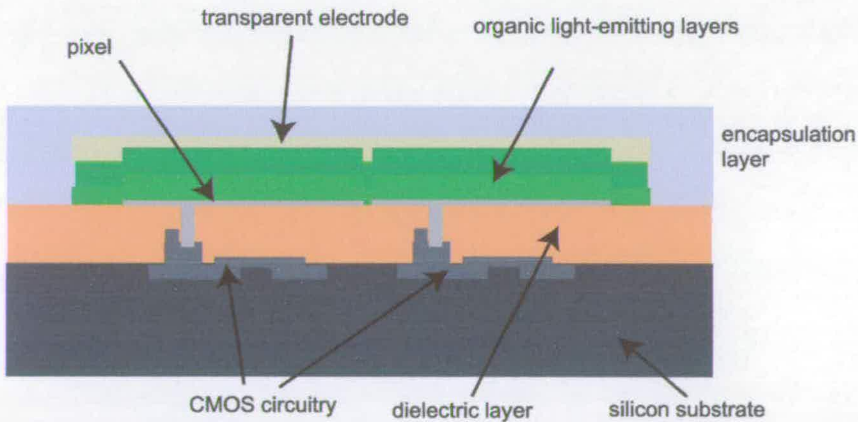


Figure 1.14: Schematic illustration of the cross-section of an OLEDoS microdisplay showing the light-emitting layer sandwiched between the CMOS backplane and the top transparent electrode.

1.3.4.3 Transmissive liquid crystal microdisplays

One of the most surprising and successful microdisplay technologies has been the miniature display option developed by Kopin [41]. As illustrated in figure 1.15, at the heart of the manufacturing sequence lies a patented process employed to transfer the CMOS circuitry manufactured on silicon-on-insulator (SOI) wafers to a glass substrate. The resulting transmissive solution is able to take advantage of simpler and cheaper optics. Because light modulation achieved using liquid crystals is dependent on the thickness of the LC layers, the thicker single pass transmissive technology is therefore less sensitive to cell gap variation than the reflective conventional LCoS technology where the light passes through the half cell gap twice. However, production costs compared to LCoS are increased due to the use of SOI substrates as well as the added complexity brought by the transfer process. Finally, like TFT-LCD Kopin's microdisplay technology still fundamentally suffers from a limited aperture despite the smaller transistor geometry employed.
One can however appreciate the technological challenges that have been tackled by Kopin when developing their technology and particularly that associated with the transfer process. As one of the earliest company to reach high volume production Kopin has been rewarded with significant commercial success.

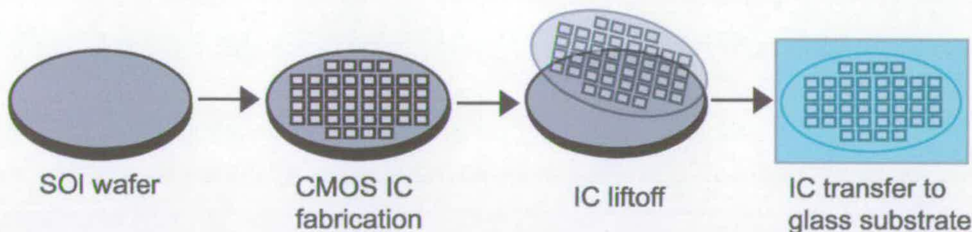


Figure 1.15: Main steps of the manufacturing sequence employed for the fabrication of Kopin's transmissive microdisplaybackplanes. From [41].

It is important to highlight at this point that TFT-LCD technology is not limited to direct view display applications. Thin film transistor technology for a time could be found in miniature displays typically around an inch in diagonal with moderate resolution up to 640x480 pixels. Recently, HTPS TFT displays with HDTV compatible resolutions have been demonstrated [42].

1.3.5 Prospects of FLCoS microdisplay technology

In order to estimate the prospects of any microdisplay technology in the various existing and predicted markets, one must take into consideration the performances of this technology (contrast, frame rate, colour depth), its manufacturing cost and the cost-sensitiveness of the particular market. Table 1.2 lists some of the attributes of the various microdisplay technologies presented so far in this thesis.

	LCoS	TFT-LCD	DMD	OLEDoS
Pixel geometry	+++	+	++	+++
Resolution	+++	++	+++	+++
Projection applications	YES	YES	YES	NO
Near-eye applications	YES	YES	NO	YES
Fabrication	++	+	+	+++
Cost	++	+	+	+++

Table 1.2: Table showing the relative properties of various microdisplay technologies.

The low power consumption and potentially lower fabrication costs of OLEDoS technology are expected to be a deciding factor for the penetration of portable products markets such as camera and camcorder viewfinders.
It is doubtful that FLCoS microdisplay will be competitive in such areas. However, the high switching speed associated with FLCoS technology permits high frame rate and high colour content to be achieved on a single panel without the need to compromise image quality by sub-pixel colour separation. This combination of factors makes it a unique candidate for applications where image quality is prioritised over power consumption and cost considerations. It is therefore not surprising to witness the recent interest of HMD manufacturers in high-resolution FLCoS devices [43,44].

The versatility of FLCoS technology permits its incorporation into projection systems. As mentioned earlier, the cost-sensitiveness of the markets like that of RPTV will favour FLCoS displays due to the possibility of producing high quality images using a single imager. DMD technology is expected to dominate the front projection market because of its performance and its robustness to the high luminous flux required for such applications. Its higher fabrication cost might prove to be an obstacle to its success within the very cost-sensitive RPTV market. It remains to be seen what part FLCoS technology will occupy in this particular area where it will be faced with competition from nematic based LCoS technologies.

1.4 Thesis outline

While it is difficult to anticipate which microdisplay technology will be the most successful at penetrating the various markets, one thing remains certain; microdisplays will revolutionise the whole information display industry and provide very lucrative opportunities.

The part FLCoS technology will occupy in the whole picture will depend on numerous factors, not the least of these being its optical performance and its fabrication cost. It is with these factors in mind that the work towards this thesis has been carried out.

Chapter 2 will present, in more details the liquid crystal mode at the heart of FLCoS microdisplays. The principle of operation of SSFLCs, the reasons behind their advantages and limitations will also be discussed. An overview of the whole FLCoS microdisplay manufacturing sequence will be presented in chapter 3. Chapter 4 will present developments aimed at improving silicon backplanes used in FLCoS microdisplays. Chapter 5 will present work carried out in 2000-2001 on the alignment of SSFLCs. Both the "rubbed polymer" alignment method and photo-alignment techniques have been investigated. A conclusion chapter will review the technical achievements presented in this thesis. Relevant further work will also be suggested.

Chapter 2. FLCoS microdisplays: principles of operation

2.1 Introduction

In order to gain understanding of the principles behind the operation of FLCoS microdisplays it is essential to review what lies at the heart of this technology, ferroelectric liquid crystals.

This chapter will present the unique molecular structure of the materials commonly referred as ferroelectric liquid crystals. The resulting physical and electro-optical properties as well as various means to exploit them will be also be presented.

2.2 Ferroelectric Liquid Crystals

2.2.1 Ferroelectric liquid crystal molecules

FLCoS microdisplay technology exploits the particular molecular structure of chiral smectic liquid crystals. Such materials are made up of elongated or “calamitic” molecules. The size of the molecules is typically of the order of 20-30 angstroms in length for a width of about around 5 angstroms. Traditionally the molecular director vector (noted $\vec{n}$) is used to refer to the long axis of a LC molecule (see figure 2.1).

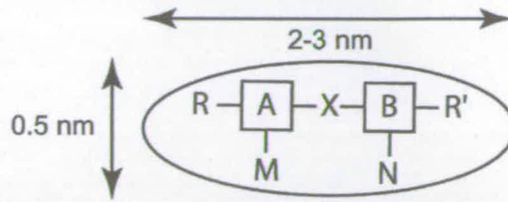


Figure 2.1: Template of the chemical structure of calamitic liquid crystal molecules including ring systems (A,B), linking group (X) and terminal groups (R,R').

As illustrated above, linearly linked ring systems, typically saturated benzene or unsaturated cyclohexane, are at the origin of the rigidity of the LC molecules and hence of their anisotropy in shape. These ring units can be directly joined together or separated by a linking group such as another ring or molecules of the form C_nH_{2n}. Such molecules however exhibit a certain degree of flexibility due to the presence of terminal groups such as alkyl (C_nH_{2n+1}) or alkoxy ($C_nH_{2n+1}O$) chains. Terminal groups incorporating polar units such as CN, F and Cl and lateral units such as F, Cl, Br, CN, NO_2 can also be attached to the ring system.

2.2.2 The thermotropic behaviour of smectic liquid crystals

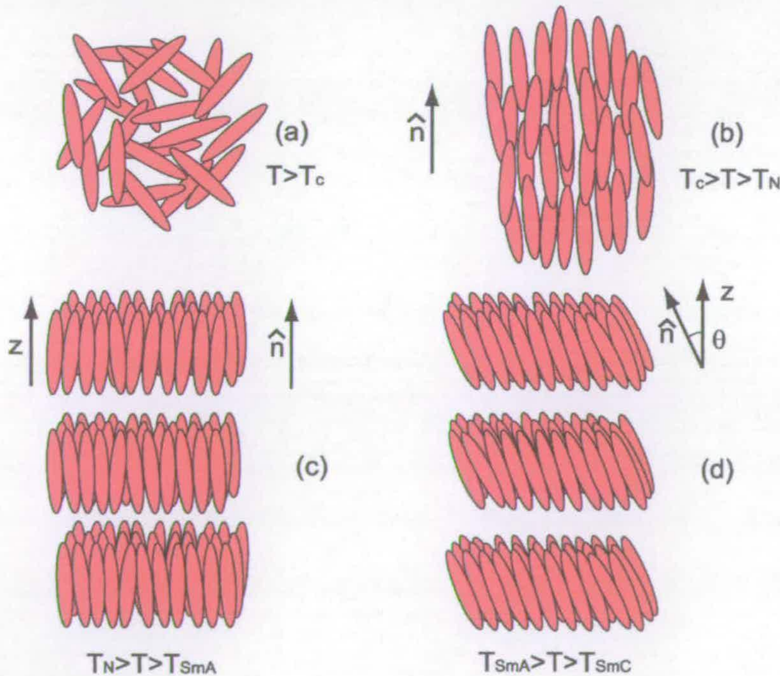


Figure 2.2: Plane view of the typical mesophases encountered when cooling a smectic liquid crystal from isotropic phase (a): Nematic phase (b), smectic A phase (c) and smectic C phase (d).

Chiral smectic liquid crystals are thermotropic, i.e. their molecular ordering is dependent on temperature. This lead to the apparition of so called mesophases (often referred more simply as phases) within certain temperature ranges.
Figure 2.2 illustrates this feature for a smectic LC material exhibiting a nematic and two smectic phases. The pure liquid state often referred as isotropic phase is similar to conventional liquid and is characterised by the absence of positional or orientational order. The temperature above which this phase exists is referred as clearing temperature (T_c).
As the temperature is lowered further, the material enters the nematic phase (N) characterized by partial orientational ordering and the absence of positional ordering.

The average molecular orientation is known as the director ($\hat{n}$). The degree of ordering of the nematic phase can be expressed by using the order parameter S defined by [45]:

$$S = \left\langle \frac{3}{2}\cos^2\beta - \frac{1}{2} \right\rangle \quad (2.1)$$

where β is the angle between individual molecules long axis and the director (n). In the nematic range, near T_c S is around 0.3 and can increase up to about 0.7 nearer the more ordered smectic phases [46].

The first smectic phase met upon cooling from the nematic phase is called the smectic A phase (SmA). In this phase the molecules arrange themselves in a layered fashion with the director normal to the layers. Upon further cooling the director tilts away from the layer normal z by an angle known as the tilt angle θ. This phase is known as the smectic C phase (SmC). The layered structure of the smectic phases is directly related to the composition of the individual molecules with either hydrogen or Van Der Waals bonding providing the necessary intermolecular interaction [47]. The orientational ordering within the smectic layer is similar to that exhibited in the nematic phase (see equation 2.1).

2.2.3 Ferroelectricity of the chiral smectic C phase

In 1975, Meyer proposed (based on symmetry considerations) that chiral smectic liquid crystal phases (noted SmC*) can exhibit ferroelectricity[2] [48]. The concept was experimentally demonstrated two years later [49].

As illustrated in figure 2.3a, smecticA mesophases (as well as nematic phases) exhibit a high degree of symmetry. In the case of the SmA phase the molecular director ($\vec{n}$) is parallel to the z-axis itself perpendicular to the smectic layer plane (x,y). The molecule is free to rotate along the z-axis. Two-fold symmetry (i.e. 180°) also exists about the x and y axes as well as mirror symmetry about planes (z,x) and (z,y).

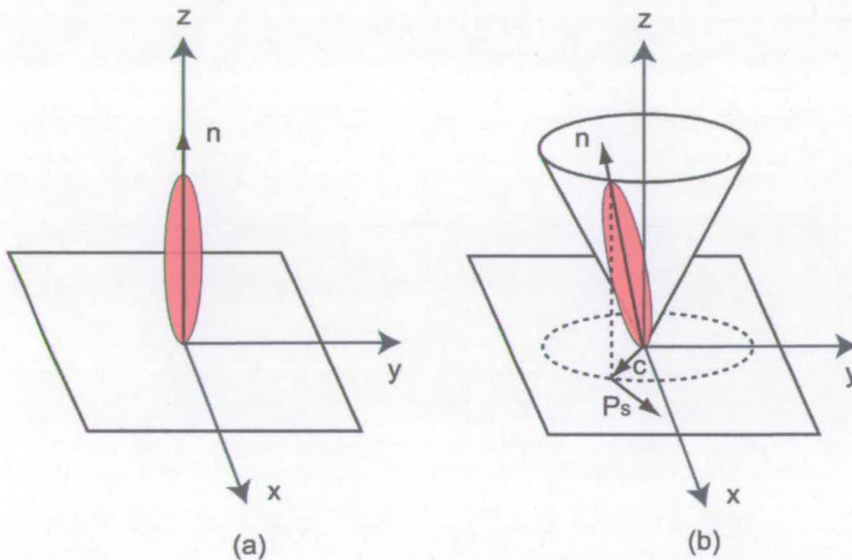


Figure 2.3: Schematic illustration of the molecular orientation of Smectic A phase (a) and the smectic C phase (b). A cone is defined by the possible molecular orientations with molecular tilt θ with respect to the normal z to the smectic layer plane (x,y). The c-director and spontaneous polarisation vectors are also represented in the case of a chiral smectic C phase.

As mentioned previously SmC phases exhibit both positional and orientational order. The possible molecular orientations with molecular tilt θ define a cone whose axis is perpendicular to the smectic layer plane (see figure 2.3b). The c-director vector ($\vec{c}$)

[2] Ferroelectric materials exhibit polarisation in the absence of an electric field.

is defined as the projection of the molecular director ($\vec{n}$) onto the smectic layer plane. Tilted smectic phases such the SmC phase offer no rotational symmetry. Mirror symmetry is however possible as well as symmetry with axis perpendicular to the molecular director and parallel the layer plane (x,y). Such symmetry conditions would lead to zero net polarisation due to the averaging of the local dipoles. If the molecule is chiral as for the chiral smectic C phase (SmC*) no mirror symmetry is possible and the only symmetry axis left is the axis parallel to the smectic layer and normal to the tilt plane. As deduced by Meyer there exists therefore a spontaneous polarisation vector ($\vec{P_s}$) associated with each smectic layer along this unique symmetry axis.

One can note that the existence of permanent polarisation is not the direct result of the polar nature of liquid crystal molecules. Its existence is due to the unique symmetry of the SmC* phase which is brought about by the chiral nature of the molecules.

The amplitude of the spontaneous polarisation depends on a number of inter-related factors. The two main factors are temperature and the molecular tilt angle, which is also temperature dependent. From an engineering point a view (i.e. for a given material) the temperature dependence of P_s is of prime interest as it will affect the electro-optical performance of any devices based on the SmC* phase.

The chemical structure of the molecule also affects polarisation, notably nature and position of the chiral centre in the molecule. A review of the factors affecting the spontaneous polarisation of chiral smectic liquid crystals can be found in the literature [50].

So far the thermally driven rotation of the molecules along their long axis has been ignored. Neutron scattering studies revealed that very fast rotation was taking place at a rate of about 10^{11} revolution per second [51]. Molecules have also been reported to group themselves in domains whose size and existence varies in time [52]. Despite being worth mentioning, these features can be ignored to describe the fundamental principle behind such complex materials. In the remainder of this thesis we will treat

the SmC* phase as a "frozen" liquid while accepting the concept of molecular motion induced by external influences and the macroscopic fluid like behaviour coupled with ordering that make liquid crystals such a unique state of matter.

Chirality is also responsible for another feature of the SmC* phase. It forces the molecular director to vary in a helical fashion from layer to layer while maintaining a constant molecular tilt angle (see figure 2.4). Spontaneous polarisation will average to zero over a distance equal to the helix pitch. In the bulk therefore the SmC* phase does not exhibit ferroelectricity. Typically, the helix pitch is in the range to a few hundreds to thousands of molecules.

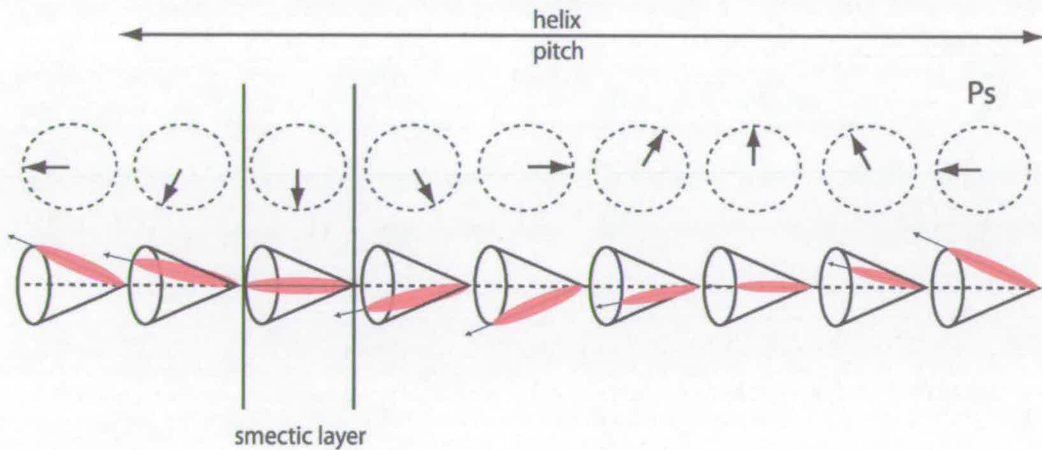


Figure 2.4: Schematic representation of the helical arrangement of the molecules in the SmC* phase. The rotation of the molecular director and hence the associated polarisation averages zero along the pitch.

2.2.4 Alignment of liquid crystals

Before examining the principles behind the use of SSFLCs for microdisplay applications, one must introduce the notion of liquid crystal alignment. The term "alignment" in the context of liquid crystals describes the orientation of the liquid crystal molecules at the surface of the boundary planes defining the LC cell. In the case of pure homogeneous alignment these molecules are made to lie parallel to the boundary plane. As it will be observed throughout this thesis, the case of homogenous alignment is again a very idealised situation. In reality, an angle often

exists between the molecules axis and the boundary planes. This angle is known as the pretilt angle (α).

Alignment of liquid crystals was first demonstrated by Mauguin in 1911 when a uniformly orientated cell was obtained by sandwiching p-azoxyanisole between two substrates previously rubbed with paper [53]. Since then, a tremendous amount of work has been carried out in order to develop techniques to promote alignment configurations suitable for the operation of LCDs. Two main alignment techniques emerged over the years. These are known as the "oblique evaporation" technique [54,55,56,57,58] and the "rubbed polymer film" method [59,60,61].
The "oblique evaporation" technique is based on the deposition (by evaporation) of a very thin film (typically around 20 nm) of silicon oxide (SiO_x) at a given angle onto the substrate. The evaporation angle and the film thickness can be used to control the pretilt of the molecules near the surface [62,63,64]. Despite being very successful in aligning liquid crystals this technique is not well suited to the treatment of large substrates. As demonstrated by Bodammer [65], the larger area to be treated, the greater the change in local evaporation angle and film thickness leading to variation in the induced pretilt across the substrate. This renders the treatment of large substrates such as 8 in. silicon wafers challenging even if in practice the situation can be improved by the use of large deposition systems.

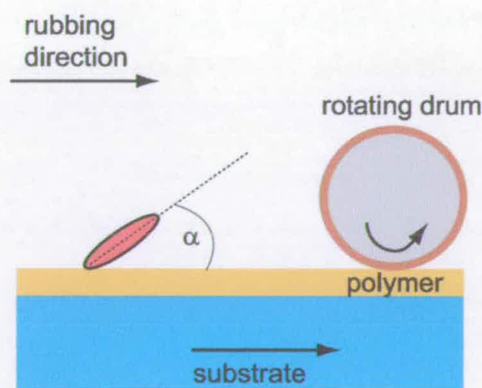


Figure 2.5: Schematic representation of the rubbed polymer alignment method. The substrate, coated with a thin layer of polymeric materials, is moved under a rotating drum itself coated with cloth like material. Often this technique leaves liquid crystal molecules lying at an angle (pretilt angle, α) with respect to the substrate surface.

The use of rubbed polymer alignment layers has proven the most popular alignment strategy due to its relative simplicity and its suitability to mass production. It consists of rubbing the surface of a polymeric film previously deposited onto the cell substrates with a velvet type cloth. While a wide range of polymers has been employed to achieve this effect, polyimides (PIs) have proven to be by far the most popular due to their strong thermal and chemical stability. PI films can be easily and reproducibly deposited onto substrates by spin coating (at speed of around 3000 rpm) from polyamic acid solutions (up to 10% in weight).

Thermal bake steps are subsequently required to evaporate the remaining solvent and allow imidization of the polyimide precursor. The resulting films are much thicker than obliquely evaporated film with practical ranging from around 10 to several hundred nm. As illustrated in figure 2.5, unidirectional rubbing is carried out using highly specialized equipment, where typically the polymer coated substrate is moved under a rotating cylinder wrapped with the rubbing cloth like material. The amplitude of the pretilt angle generated by such a technique is dependent on numerous factors including polymer and liquid crystal chemistries, substrate speed, rotating drum speed and distance/pressure between the cloth and the polymer layer. However it can safely be assumed that the orientation of the molecules with respect to the resulting rubbing direction is always as represented in figure 2.5.

2.2.5 The Clark-Lagerwall effect

In 1980 Clark and Lagerwall invented a simple way of unwinding the helix of chiral smectic materials hence allowing for their spontaneous polarisation to be exploited on a macroscopic scale [33]. This is achieved by surface stabilisation. It consists of constraining a chiral smectic material between two surfaces separated by a distance much smaller that its helix pitch. Typically, this distance or cell gap is less than a quarter of the helix pitch [66].

Under these conditions, the boundary surface conditions force the molecules to lie in a plane parallel to the bounding planes with smectic layer perpendicular to the latter. As it will be shown in chapter 4, the molecules axis can depart from this direction. The description of the molecular structure of SSFLCs using the much idealised "bookshelf" analogy is however sufficient in order to demonstrate their unique

electro-optical properties. As illustrated in figure 2.6, SSFLCs exhibit two stable states of opposite polarisation direction. They correspond to the two opposite molecular orientations on the smectic cone, lying in the plane (xz) and symmetrical with respect to the smectic layer normal z. In the absence of an electric field the two surface stabilised states are degenerate and the SSFLC systems will exhibit distinct regions, often referred as domains, corresponding to both orientations.

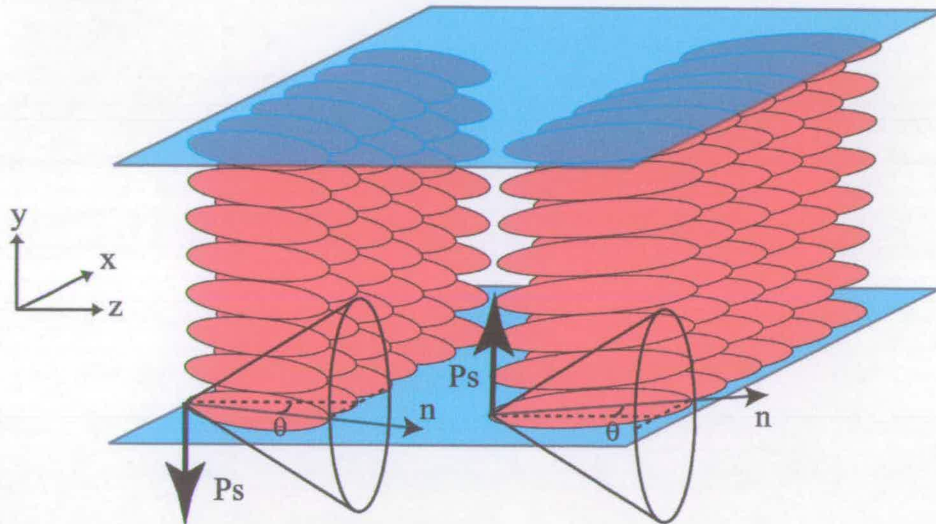


Figure 2.6: Schematic representation of the "Bookshelf" structure of SSFLCs with its two possible states of opposite polarisation direction.

Under the application of an electric field of given polarity the SSFLC molecules can be driven to one of the two states with its associated spontaneous polarisation vector pointing in the same direction as the electric field. Switching to the other driven state is achieved by simply reversing the polarity of the applied electric field.

Ideally SSFLCs exhibit bistable memory. In other words, after SSFLC molecules in one or the other state, molecular orientation will be retained upon removal of the applied field. As it will be shown later in this thesis, pure bistable memory is difficult to achieve in practice.

2.2.6 Chevron structure and zigzag defects

As mentioned earlier aligning SSFLCs in the idealised bookshelf structure is difficult. This is caused by the molecular tilt taking place at the SmA-SmC* phase

transition leading to the shrinkage of the smectic layers . In order to maintain smectic layer density and because of the anchoring brought by alignment at the boundary surfaces prohibiting molecular motion, smectic layers bend forming the so-called chevron structure (see figure 2.7). The existence of tilted smectic layers was first demonstrated by Reiker using X-ray scattering [67] and then confirmed by Elston using a guided mode techniques [68].

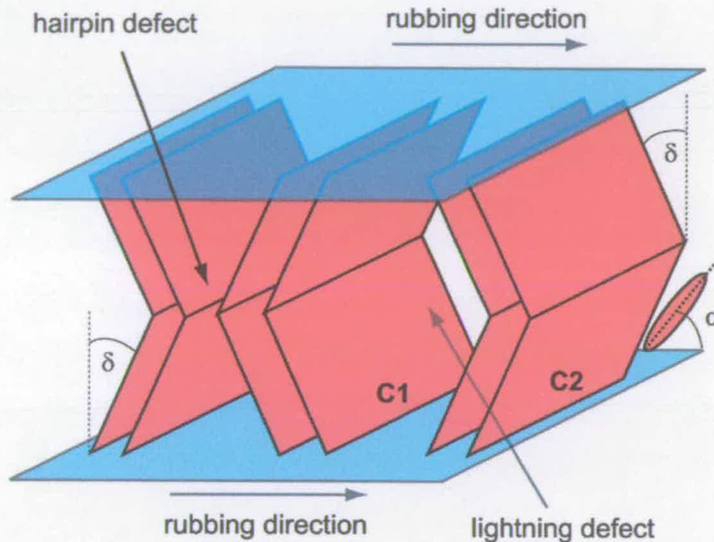


Figure 2.7: Schematic representation of the chevron structures often observed in SSFLC cells. One can distinguish between two chevron orientations (C1 and C2), each characterized by the direction of the apex with respect to the alignment direction. One can distinguish between two types of chevron defects: lightning and hairpin defects.

The existence of the chevron structure can be very detrimental for display applications. As it will be shown later in this thesis it often leads to the presence of chevron defects. Such defects appear at the interface between two regions of opposing chevron orientations and cause localized light leakage. As illustrated in figure 2.7, one can distinguish between two types of chevron defects. In the case of the hairpin defect, the distance between two adjacent layers is reduced in the interior of the cell. Lighting defects see that distance reduced at the boundary planes of the cell. The relationship between tilt angle (θ), pretilt angle (α) and the layer tilt angle (δ) as well as their influences on the chevron orientation (C1 or C2) will be discussed in chapters 5 and 6.

2.3 Exploiting SSFLCs in LCoS devices

2.3.1 Binary Light amplitude modulation

Binary amplitude modulation can be achieved by placing an SSFLC layer between crossed polarisers. In order to achieve the best extinction possible, the cell is orientated so that one of its driven states sees the molecules long axis parallel to the direction of the input polariser (see figure 2.8a). In that case, the polarisation of the incident light (now parallel to the molecular axis) remains unchanged so that light exiting the cell is blocked by the analyser. This defines the "dark state" or "off state".

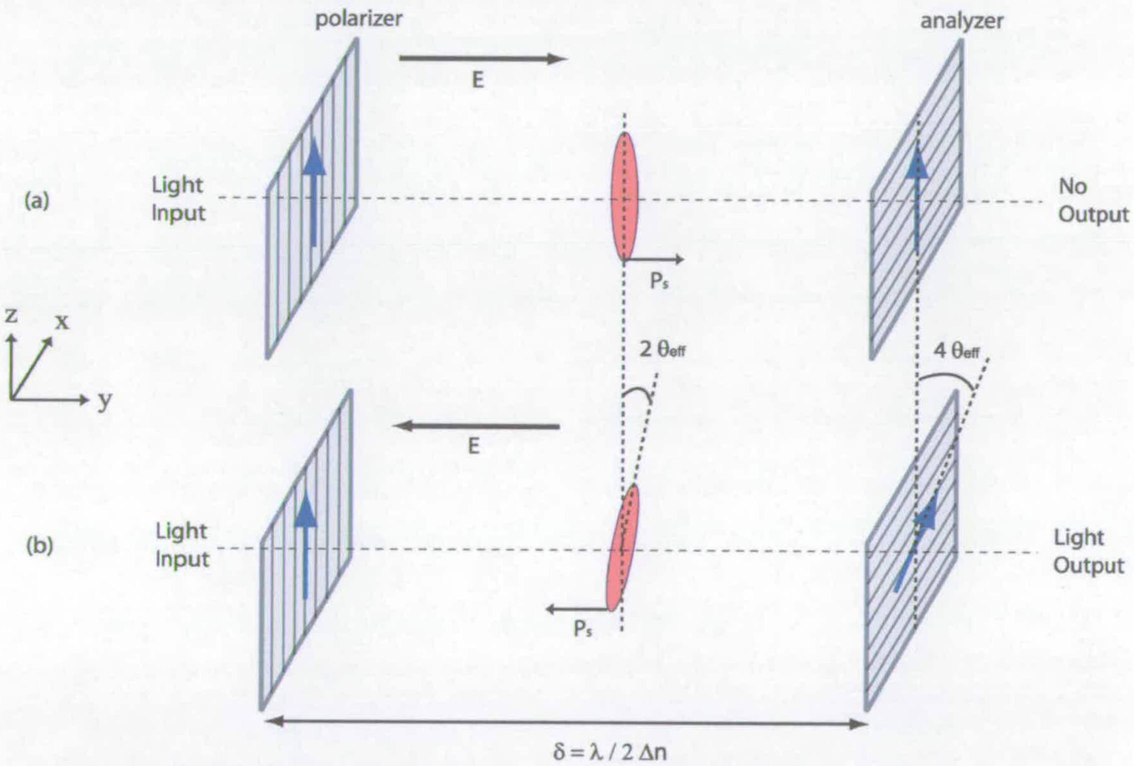


Figure 2.8: Schematic representation of the optical configuration employed to achieve binary amplitude modulation with SSFLCs. In the dark state the molecules are aligned parallel to the input polariser (a). In the bright state the molecules and the light polarisation direction is rotated by inversing the electric field polarity (b).

Under the application of an electric field of opposite polarity, the molecules rotate by twice the value of the effective tilt angle (θ_{eff}) in the plane (zx) (see figure 2.8b).

Under such conditions, the intensity of the light exiting through the second polariser is given by [69]:

$$I = I_0 \ \sin^2 \ (4\theta_{eff}) \ \sin^2 \ (\frac{\Delta n \ d \ \pi}{\lambda}) \tag{2.2}$$

with: I_0 the intensity of the light entering the SSFLC layer,

Δn the birefringence of the FLC,

d the thickness of the SSFLC layer,

λ the wavelength of light.

From equation 2.2, one can see that optimum modulation can be achieved with SSFLC systems exhibiting an effective cone angle of 22.5° and with a thickness d satisfying the half-wave plate conditions:

$$d = \frac{(2i+1)\lambda}{2\Delta n} \tag{2.3}$$

with: $i = 0, 1, 2, 3$, etc...

While equation 2.3 describes the optimum cell thickness in transmission, one must note that the reflective nature of LCoS devices causes the requirements on the thickness of the SSFLC layer to be halfed. Assuming a birefringence value of 0.160, as indicated by the manufacturer of the FLC material FELIX-015-100 employed in this work (see Appendix A); one can estimate the optimum SSFLC layer thickness in a reflective configuration to be around 0.86 μm for 550 nm light.

The switching time of SSFLC molecules from a driven state to another can be approximated to [70]:

$$\tau_{off} \simeq \tau_{on} \simeq \frac{\eta}{P_s E} = \frac{d\,\eta}{P_s V} \tag{2.4}$$

with: η the rotational viscosity of the liquid crystal,

P_s the spontaneous polarisation,

E the electric field across the cell,

V the voltage applied across the cell.

Assuming a rotational viscosity of 80 mPas and a spontaneous polarization of 33 nC/cm^2, as indicated by the manufacturer of the FLC material FELIX-015-100 employed in this work (see Appendix A); one can estimate the switching time of an SSFLC layer with the optimum thickness of 0.86 μm and under the application of a CMOS compatible voltage of 2.5V to be around 83 μs at 25°C.

2.3.2 Grey-scale and colour

In the absence of an intrinsic grey-scale, a method known as binary weighted time dithering can be employed for rendering full colour images from the binary electro-optical response of SSFLCs. Each full colour frame to be displayed is split into red, green and blue sub-frames or colour field, which are individually rendered by a sequence of black and white images or bit-planes. The high switching speed of SSFLCs combined with the high speed of CMOS transistor technology allow the bit-plane sequence to be carried fast enough so that the human eye integrates the separate binary images into a full colour image.

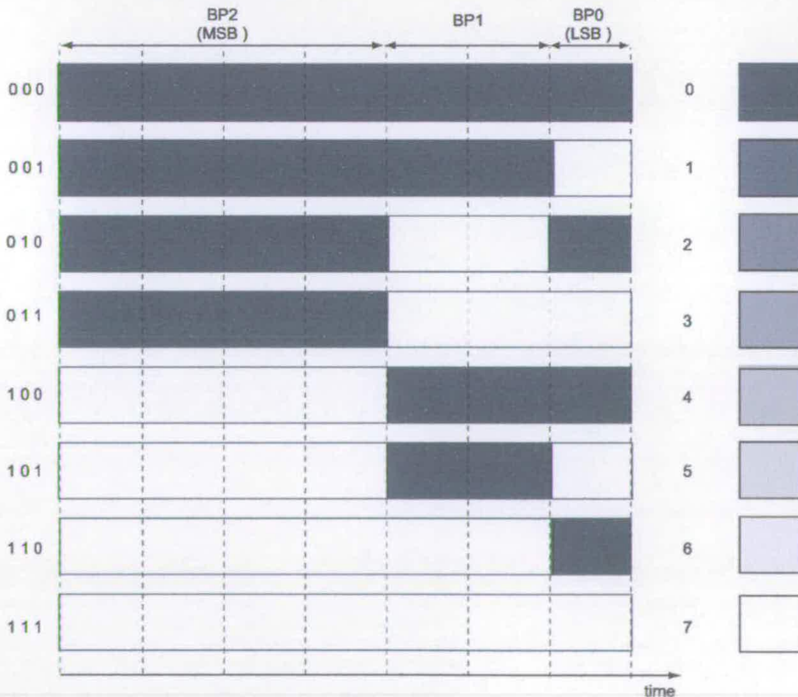


Figure 2.9: Schematic illustration of the principle of pulse coded modulation using binary bit-planes to render grey-scale.

Figure 2.9 illustrates the principle of pulse coded modulation where a series of 3 binary bit-planes (BP0, BP1 and BP2) is used to render 2^3=8 different grey-levels from black (0) to white (7). The period for which each bit-plane is valid is directly proportional to its binary weight. In the example above, the bit-plane corresponding to the most significant bit (MSB) is kept valid for a period equal to 4/7 of the sub-frame period, the following bit-plane for a period of 2/7 of the sub-frame period and the bit-plane corresponding the least significant bit (LSB) for a period of 1/7 of the sub-frame period.

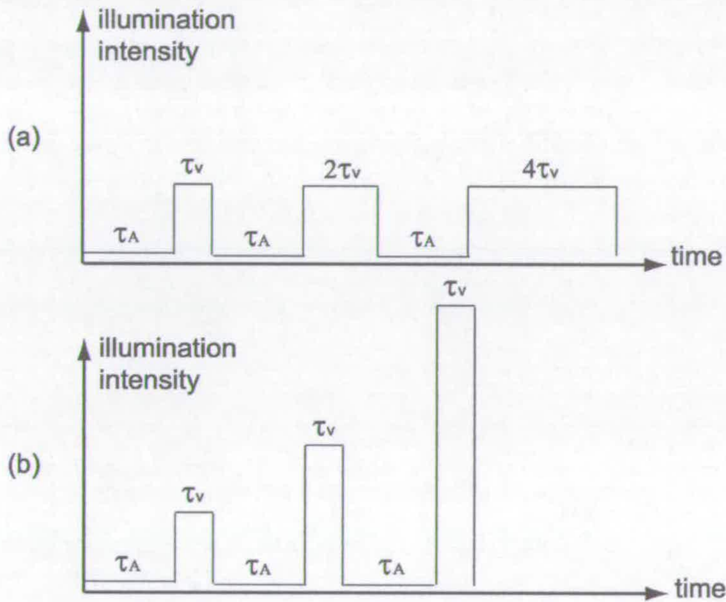


Figure 2.10: Schematic illustration of the illumination sequence employed for rendering greyscale using a sequence of (a) binary weighted temporal dithering and (b) binary weighted intensity dithering.

As illustrated in figure 2.10a, a period (τ_A) is necessary to address the pixel array prior to displaying each bit-plane. It includes the electronic addressing period (τ_E) which is required to load the frame of data into the pixel array row by row and the settling time period (τ_S) necessary for the FLC to switch from one state to another. The latter is directly related to the switching time described in the previous paragraph (see equation 2.4). The electronic addressing period necessary to load the display one row at a time is given by:

$$\tau_E = \frac{M\,N}{f\,w} \tag{2.5}$$

with: N the number of rows,

M the number of columns,

f the bus clock frequency,

w the bus width.

The minimum viewing period (τ_V) associated with the bit-plane corresponding to the LSB is known as the slot time. As shown below, the slot-time depends on the bit-depth (n) of the grey-scale displayed in each colour sub-frame and the overall frame rate (f).

$$\frac{1}{f} = 6\left[n\left(\tau_E + \tau_S\right) + \tau_V\left(2^n - 1\right)\right] \tag{2.6}$$

So far in this thesis, the technique discussed to achieve grey-scale has been based on varying the period of illumination (assumed of constant intensity) for each bit-planes in relation to its weight. As illustrated in figure 2.10b, an alternative approach consists of varying the intensity of the illumination rather than the time. For a given sub-frame period and addressing time it allows more grey-levels to be displayed and/or longer illumination periods. Such method is indeed feasible using illumination with conventional Light-Emitting Diodes (LEDs) in low intensity near eye systems. However it is less suitable for projection systems employing high power arc lamp which cannot be turned off repetitively.

2.3.3 DC balance requirements

In order to avoid the irreversible and destructive migration of the ionic species present in the liquid crystal materials one must ensure that the voltage applied across the LC cell averages zero over time.

NLCs based electro-optical modes are based on the dielectric properties of liquid crystals. One of the optical state (off-state for normally black modes and on-state for normally white mode) is achieved in the absence of any applied electric field and the optical transmission is controlled by the amplitude an AC field.

In the case of SSFLCs where the electro-optical effect is based on the polar properties of the materials the direction of the electric field dictates which optical state is achieved. In practice this means that for each bit-planes displayed, the inverse or negative bit-plane must be set for the amount of time. While the inverse image is present in the display the illumination is turned off. From a practical point of view this can be easily achieved using LEDs based illumination. When arc lamps are used as illumination source, blanking regions are introduced into the colour wheel.

Both adjacent balancing where each bit-plane is immediately followed by the respective negative bit-plane and grouped balancing where several bit-planes are illuminated before to set their complement onto the display are possible. The 50%-50% duty cycle associated with the requirements for inverting each bit-planes is very detrimental when considering projection applications where the amount of light output is very important to the appearance of the displayed image.

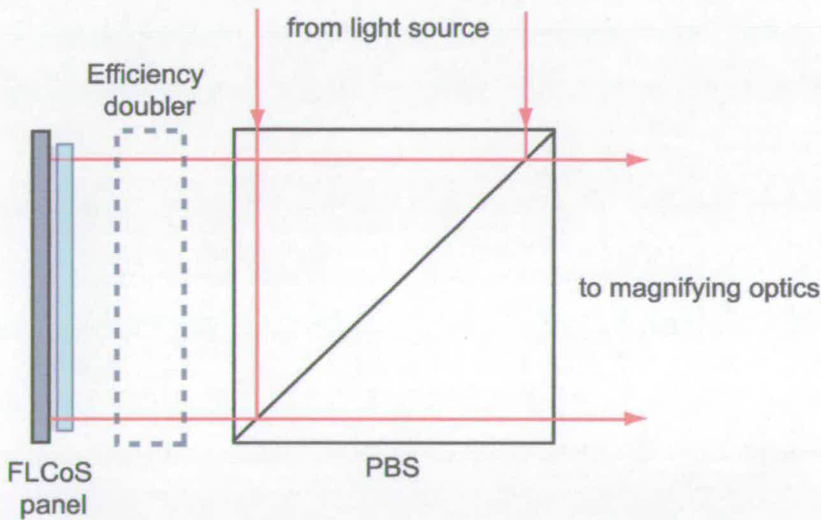


Figure 2.11: Schematic illustration of the optical arrangement in which a transmissive SSFLC cell is employed as efficiency doubler.

As it will presented in the next chapter, certain backplane designs allow for DC balancing without the need for loading the data for the inverted bit-plane however pulsed illumination is still required.

The duty cycle of display systems based on binary amplitude modulation with SSFLCs can be improved by optical means. As illustrated in figure 2.11, a device known as efficiency doubler can be inserted between the polarising beam-splitter cube and the reflective FLCoS panel. It is used to optically invert the contrast of the complement data so that it can be illuminated for viewing along with the normal data. Efficiency doubler systems using NLCs [71] and FLCs [72] have been developed

Chapter 3. FLCoS microdisplays: principles of construction

3.1 Silicon backplanes

3.1.1 Introduction

Several silicon backplane designs have been developed to drive liquid crystals. This section will focus on backplane architectures that have been combined with SSFLCs. Table 3.1 lists the various designs developed at the University of Edinburgh or in collaboration with an industrial partner. The various designs have been reviewed more extensively in the literature [73,74,75].

Resolution	Pixel pitch (μm)	Pixel type	Year	Reference
176 × 176	30	DRAM	1990	[76]
256 × 256	40	SRAM	1995	[77]
512 × 512	20	DRAM	1995	[78]
1024 × 768	12	DRAM	1997	[79]

Table 3.1: Specifications of the silicon backplane designs developed at the University of Edinburgh or in collaboration with industrial partners.

3.1.2 DRAM backplanes

As mentioned in section 1.3.1, the simplest LCoS backplane design is the single transistor DRAM pixel (see figure 3.1) [76]. It relies on using a single MOSFET

transistor as a switch so that when a particular row is scanned the data (delivered through the columns) is allowed to flow to the pixel in the form of a charge.

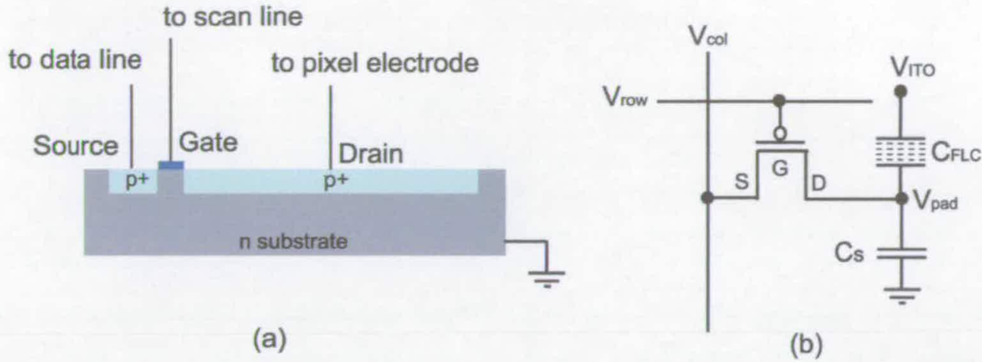


Figure 3.1: Schematic representation of the cross-section of a single transistor DRAM pixel (a) and its circuit symbol equivalent including the capacitance of the SSFLC cell C_{FLC} (b).

In order to guarantee switching of the SSFLC layer, the charge stored (Q_s) in the pixel must remain above a critical value (Q_c) with:

$$Q_c = 2 P_s A \tag{3.1}$$

and

$$Q_S = C_S V_{pad} + C_{FLC} (V_{pad} - V_{ITO}) \tag{3.2}$$

with: P_s is the spontaneous polarization of the FLC,
A is the pixel electrode area,
Cs is the storage capacitance,
C_{FLC} is the capacitance of the FLC cell,
V_{ITO} is the voltage applied to the top electrode,
V_{pad} is the voltage present at the pixel electrode.

While such a simple design has its advantages in terms of reliability, fabrication yield and pixel packing density it exhibits several limitations. Parasitic capacitances can degrade the efficiency of the storage. Photo-induced carriers can also migrate into the storage diffusion region and accelerate pixel discharge.

In addition, the single transistor DRAM design is intrinsically prone to loss of drive voltage. Assuming that the voltage pixel electrode V_{pad} is high when the supply rail voltage V_{DD} is applied to both the column and row lines, its maximum voltage value is:

$$V_{pad,\max} = V_{DD} - V_T \qquad (3.3)$$

with: V_T the threshold voltage.

The value of the threshold voltage is increased when a positive potential is present between the source and the bulk of the MOSFET transistor. Typical values V_T of around 1.5V are expected for V_{DD} values of 5V. This feature is an additional drawback of the single transistor DRAM design as it results in a reduced potential at the pixel electrode which in turn leads to a slower switching of the FLC molecules as well as a smaller charge stored in by the pixel.

An additional problem arises due to the fact that the switching of SSFLCs is associated with the motion of dipoles which has for effect to reduce the effective voltage stored across the capacitor. The voltage reduction is given by [80]:

$$\Delta V = \frac{2P_S}{C_{FLC} + C_S} \qquad (3.4)$$

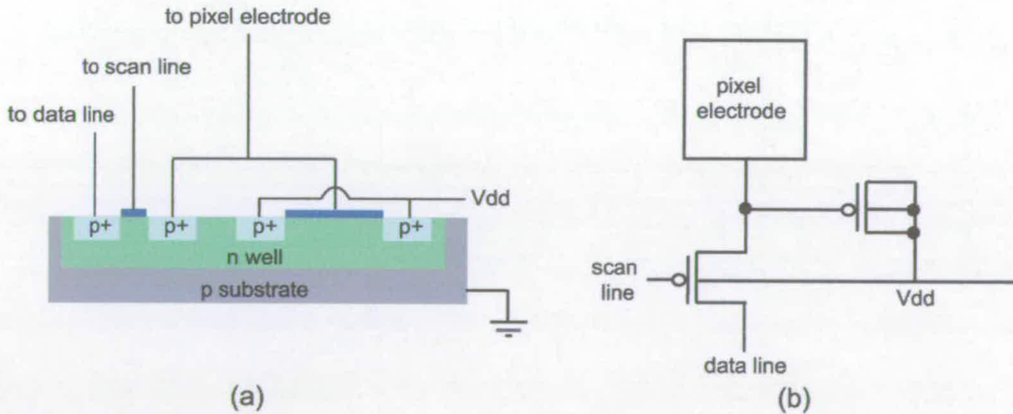


Figure 3.2: Schematic representation of the cross-section of an enhanced DRAM pixel using two MOSFET transistors (a) and its circuit symbol equivalent in relation to the addressing of an LCoS device (b).

An improved design based on the DRAM concept is illustrated in figure 3.2 [81]. It relies on the use of an additional transistor to act as storage capacitor. The effect of parasitic capacitances on data storage is reduced by the increase in the storage capacitance brought by the gate oxide of the storage capacitor. Such design is also less sensitive to drive signal degradation through the flow of photo-induced carriers. The junction bias between the n well and the p substrate prevent the migration of such carriers when generated in the substrate to the n well [82].
As it will presented later in this chapter, certain steps can be taken during the fabrication of the silicon backplanes to further reduce photo-induced charge leakage.

3.1.3 SRAM backplanes

Another type of silicon backplanes has been employed to drive SSFLCs. It is based on the use of Static-Random-Access- Memory (SRAM) [77]. As illustrated in figure 3.3, it employs a 6 transistors SRAM latch in combination with a 4 transistors XOR gate.

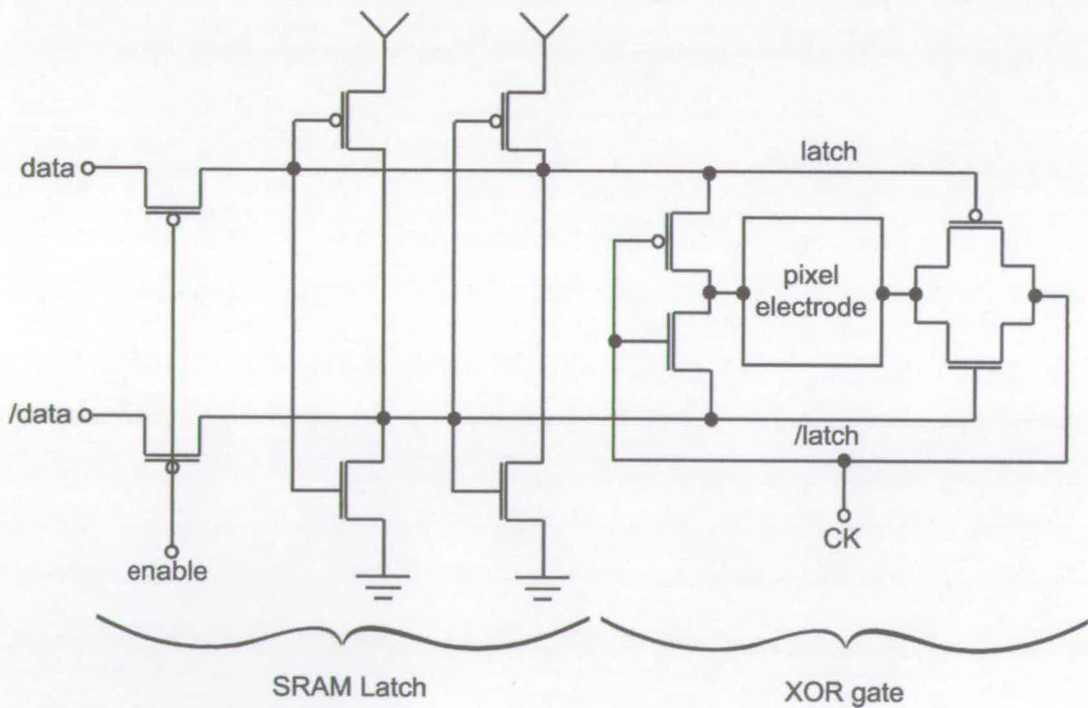


Figure 3.3: Schematic representation of the SRAM-XOR design developed to drive SSFLCs.

In the SRAM-XOR design, the pixel electrode is connected to the output of the XOR gate having as inputs the output of the SRAM latch and the clock signal (CK). The CK signal is also applied to the top electrode. Under such configuration the voltage signal at the pixel electrode is in anti-phase with the top electrode signal when a logic 1 is stored in the SRAM latch. When a logic 0 is stored in the latch, the pixel electrode signal and the top electrode signal are in phase which results in a net zero voltage across the FLC layer. The relationship between the various signals is illustrated in figure 3.4.

It can be seen that operating the clock signal with a 50% duty cycle permits the FLC layer to be DC-balanced automatically. In addition, in the event of a logic zero being stored in the latch, SSFLC systems exhibiting bistable memory will remain in the optical state they were last switched to.

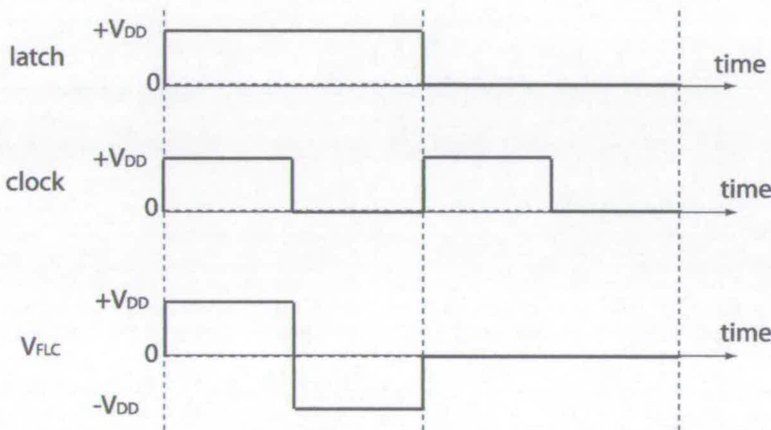


Figure 3.4: Schematic representation of the relationship between the latch and clock signals in the SRAM-XOR pixel and the resulting voltage signal across the FLC layer (VFLC).

Unlike the DRAM pixel design which suffers from the effect of the transistor threshold voltage, the full power rail voltage is available for driving the FLC in the case of the SRAM-XOR architecture. It exhibits unlimited charge capacity as the pixel electrode is constantly connected to one of the power rails. This also means that the pixel electrode voltage is not affected by the switching of the FLC layer as in the case of the DRAM pixel.

While the SRAM-XOR design overcomes the limitations of the DRAM, it is important to note that this is achieved at the expense of space due to the large number of transistors involved. SRAM-XOR pixels are known to be susceptible to "latchup" (leading to permanent and destructive failure), as well as damage from the large transient current that can occur when switching a large number of SRAM cells [73].

3.1.4 Hybrid analog/digital backplanes

Several pixel designs incorporating dynamic logic components have been developed in order to drive SSFLCs [83]. This section will present the hybrid pixel architecture developed by Displaytech illustrated in figure 3.5.

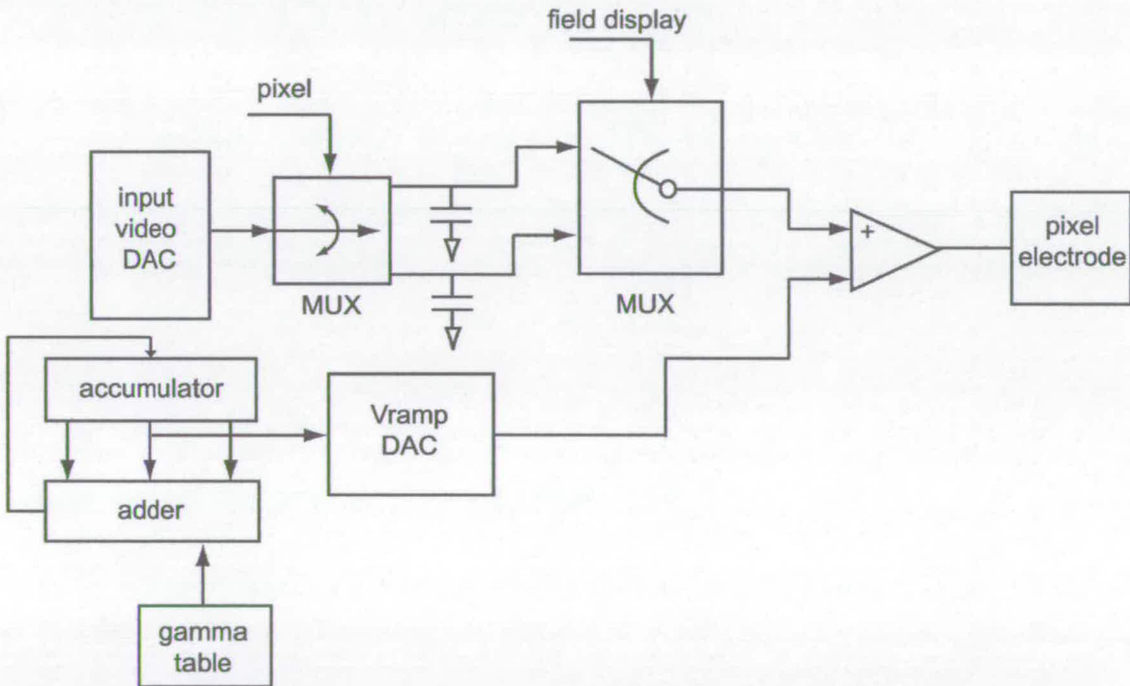


Figure 3.5: Schematic illustration of the pixel architecture developed by Displaytech to drive FLCs [83].

The pixel data loaded into the display is converted from an 8-bit digital value to an analog voltage (via an integrated DAC) prior to being stored in one of the two capacitors present in each individual pixel. The use of two capacitors allows the data for the next sub-frame to be loaded in one capacitor while the other one controls the current display field.

As illustrated in figure 3.6, grey-scale for each colour sub-frames is rendered using a technique known as Pulse-Width-Modulation (PWM) rather than using a series of binary weighted bit-planes as presented previously.
PWM is achieved by comparing the voltage stored in the individual pixels to a global ramp signal (applied to all pixels in the array). The ramp signal consists of a monotonically increasing signal (adjustable through a gamma table). Each pixel is switched on at the start of each sub-frame and remains on until the ramp signal equals the stored voltage. However, as with the weighted time dithering technique, in order to maintain DC balance, the sub-frame is subsequently inverted and the illumination turned off. The main advantage of using PWM is that it requires less transitions between optical states. As shown in equation 3.4, this results in an improved duty cycle when compared to equation 2.6.

$$\frac{1}{f}=6\left(\tau_E+\tau_S+\left(2^n-1\right)\tau_V\right) \tag{3.5}$$

with: f the frame rate

τ_V the slot-time

τ_E the electronic addressing period

τ_V the solt-time

n the greyscale bit-depth

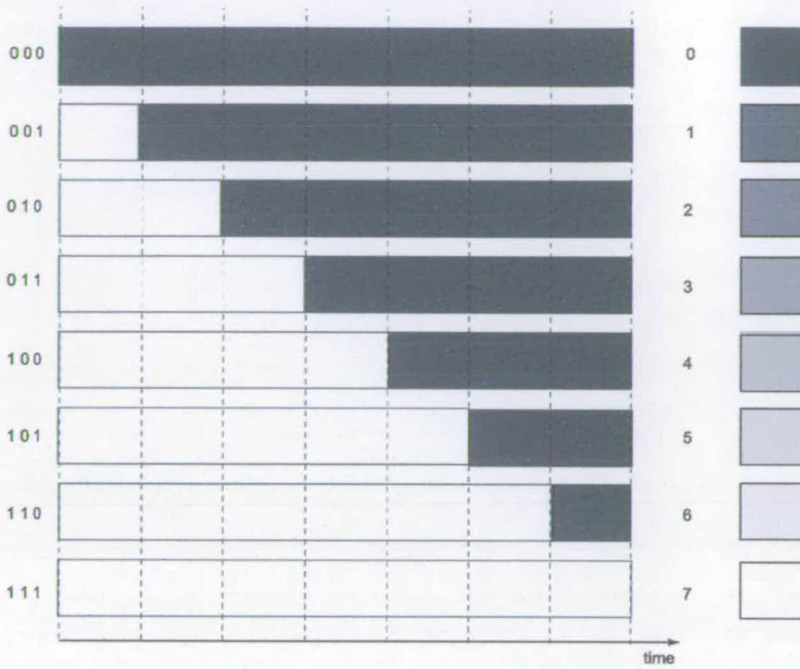


Figure 3.6: Schematic illustration of the principle of pulse width modulation to render grey-scale.

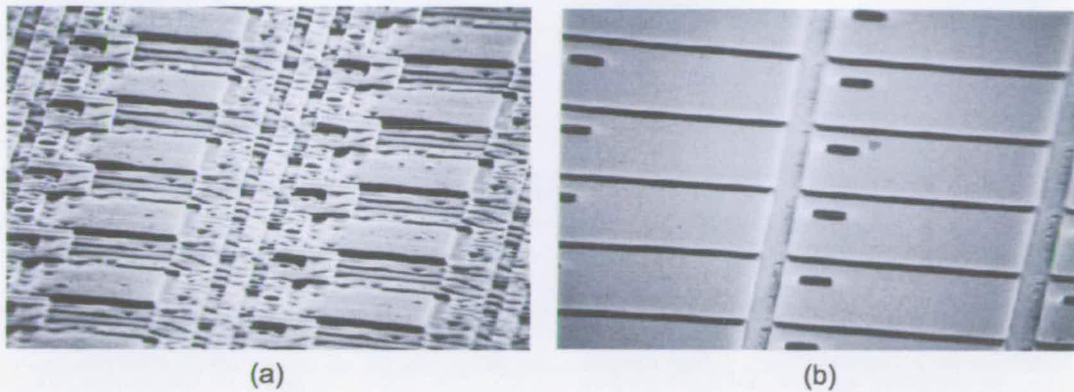
3.2 Silicon backplane post-processing

3.2.1 The need for backplane post-processing

In LCoS devices, in addition to supplying the LC layer with adequate voltage, the pixel electrode layer of silicon backplanes must fulfil an optical role by providing a highly reflective surface suitable.

As illustrated in figure 3.7a, the "raw" circuitry of silicon backplanes is very inadequate for microdisplay application. The high surface roughness not only decrease optical reflection but as it will be put on evidence later in this work, causes additional issues in terms of the alignment of FLC molecules. Maybe most importantly for display application the "raw circuitry" exhibits a very low fill factor[3].

[3] The fill factor is used to express the ratio of the active area of the device to its total area.



(a) (b)

Figure 3.7: SEM micrograph of the top surface of a 256x256 SRAM-XOR silicon backplane before (a) and after the conventional post-processing sequence (b). The pixel pitch is 40 μm.

A sequence of microfabrication processing steps, known as post-processing, is employed to improve the optical characteristics of the silicon backplanes. As illustrated in figure 3.7, when applied to the 256x256 SRAM-XOR, such procedure permitted an increase in fill-factor from 22% to 84% [77].

3.2.2 Backplane planarisation

The first step of the post-processing sequence is known as backplane planarisation. Its aim is to improve the topography of the silicon chip to allow for further processing towards improving the optical quality of the device. Several methods have been employed to this effect. The first attempt at planarising LCoS devices was made using a spin coated polyimide film [84] and resulted in a low planarisation (DOP[4] < 30%). Other spun cast materials such spin-on glass also exhibited limited planarising effects with DOP <60% having been demonstrated [85]. Specialists spun-cast materials such as benzocyclobutene (BCB) have recently been employed for LCoS backplane planarisation with much more success allowing a DOP around 80% to be achieved [86].

A very high degree of planarisation (DOP >95%) has been demonstrated by the introduction of a technique known as Chemical-Mechanical-Polishing (CMP) [87]. In this case, a layer of dielectric material (typically silicon oxide) is deposited on the

[4] Degree of planarisation (DOP) is defined by the formula 1-a/b, where b is the original step height and a the remaining step height after planarisation.

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silicon wafer by chemical vapour deposition (CVD). The resulting conformal layer is then polished to achieve the desired surface roughness (see figure 3.8a). CMP uses a chuck to maintain the silicon wafer to be planarised in contact with a polishing pad. Both chuck and pad are rotating and typically the chuck is made to oscillate over the pad (see figure 3.8b). Planarisation takes place due to the abrasive and chemically reactive solution (slurry) fed onto the pad. Tight control of the main process parameters such as wafer down-force, chuck and pad rotating speeds ultimately allows surface finish with roughness in the nm scale to be produced. Critical aspects of the CMP process when applied to the planarisation of the silicon backplanes of microdisplay devices will be discussed in chapter 4.

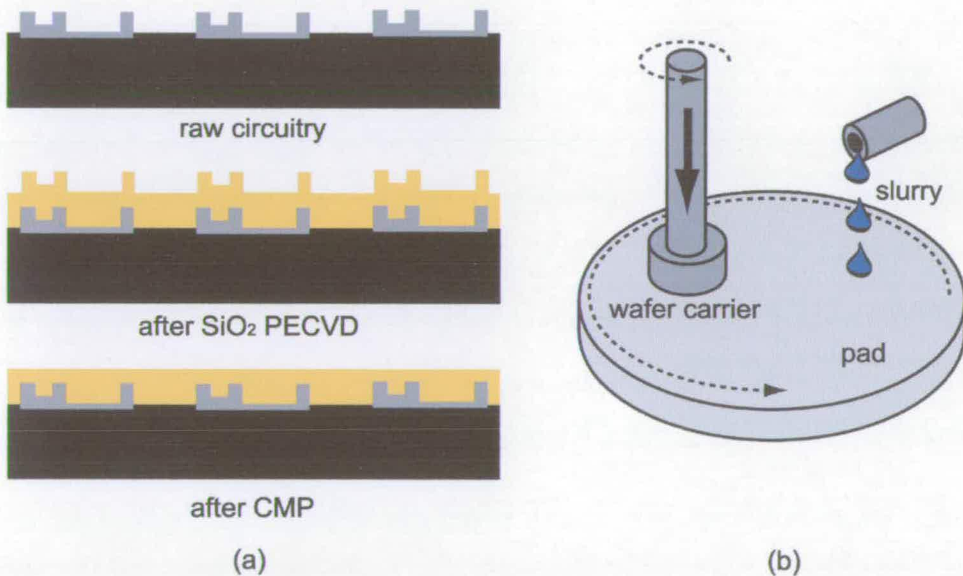


Figure 3.8: Principle of CMP planarisation where material removal is induced by both the abrasive and chemical actions of the slurry.

3.2.3 Pixel layer fabrication

As illustrated in figure 3.9a, via holes are etched through the planarised dielectric layer to allow for the electrical connection between the CMOS circuitry and the top pixel electrode. This is typically carried out using dry-etching techniques such as Reactive Ion Etching (RIE). Aluminium sputtering is then employed to deposit the pixel layer which is subsequently dry-etched to define the pixel electrode.

In order to reduce the photo-induced charge leakage effects in DRAM pixel architectures an additional metal layer can be fabricated to block the light passing between the individual pixel electrode [88] (see figure 3.9b).
The shortcomings of this simple post-processing procedure will be discussed in more details in chapter 4 where additional techniques aimed at improving the optical properties of silicon backplanes will be presented.

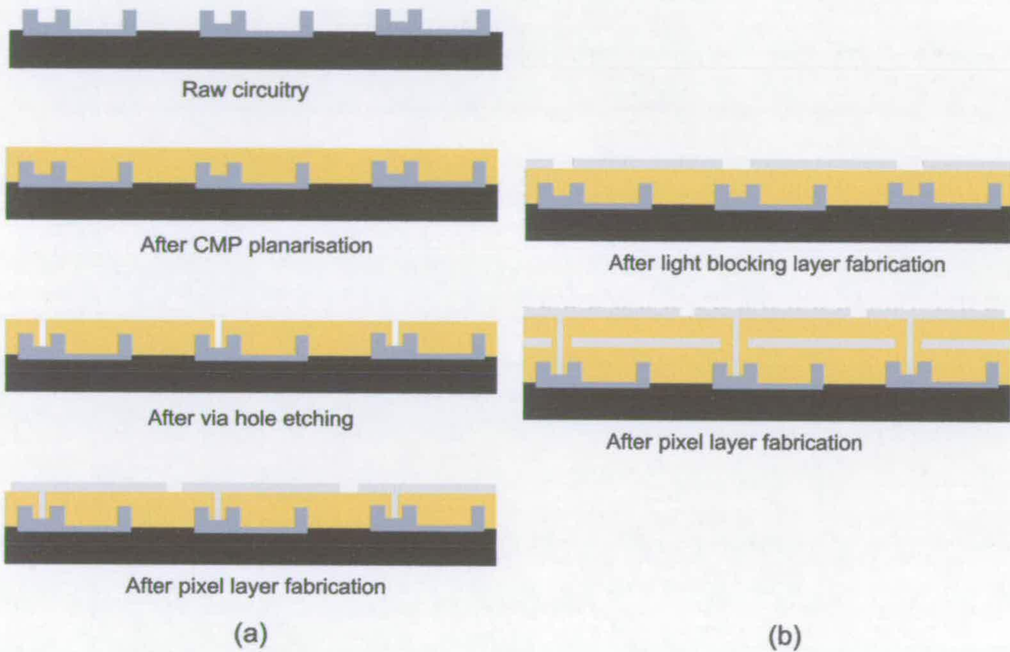


Figure 3.9: Via contact holes are etched through the planarised dielectric layer to allow for contact between the CMOS circuitry and the top pixel electrode layer (a). An additional metal layer can be used to shield the underlying circuitry from the light (b).

3.3 Glass substrates

Glass substrates employed to manufacture LCoS microdisplays are typically 0.7 or 1.1 mm in thickness. Table 3.2 lists some of the glass materials employed in the fabrication of LCoS devices [89]. Like the silicon wafers they are round and supplied with a notch for coarse alignment. The edge of the glass wafers are rounded to reduced the likelihood of cracking during handling. It is often the case that the surface of the glass substrate is polished by their manufacturer to achieve a surface

roughness suitable to LCoS technology. Unlike the surface finish the flatness of glass wafers is strongly related to the type of material used and cannot be altered easily.

Manufacturer	Glass
Schott	Borofloat 33
Corning	Eagle 1737
Hoya	NA40

Table 3.2: Some of the glass materials employed in the manufacture of LCoS microdisplays.

As illustrated in figure 3.10, an ITO layer is deposited on the surface to be facing the silicon backplane. The material selected for its electrical and optical properties can be deposited by thermal evaporation and sputtering [90,91,92,93]. Deposition parameters are critical to achieving the above properties as well as achieving a suitable topography. The resistance of ITO films decreases with increasing thickness. Thicker films are typically rougher and offer reduced optical transmission.
Additional layers are deposited onto the glass substrates. Anti-reflection coatings are deposited onto the top surface of the glass substrates to reduce reflection from incoming light that surface and increase the amount of light penetrating the device. Protective coatings can also be employed to increase the resistance to scratching.

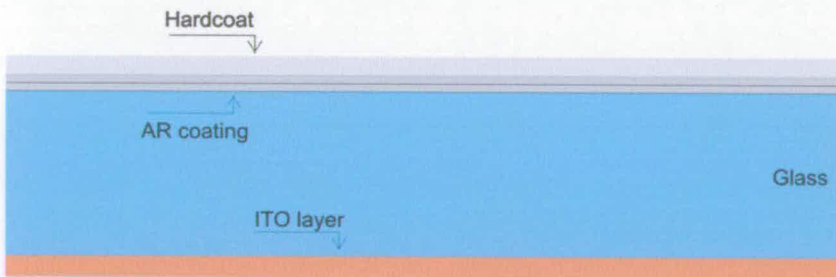


Figure 3.10: Layered structure of glass substrates employed in LCoS manufacturing.

3.4 FLCoS microdisplays manufacturing sequence

3.4.1 Wafer scale processing

3.4.1.1 Cleaning

Prior to fabrication both silicon and glass substrates are put through a very extensive cleaning procedure. It typically consists of a combination of mechanical and chemical processes aimed at removing particulates and organic contaminants. Initial cleaning is carried out to remove particles and organic films in detergent or in solvent solutions. Brush scrubbing can be carried out to remove adhering particles. Megasonic agitation is preferable in the case of LCoS devices substrates due to the reduced likelihood of mechanical damage to the surfaces as well as its efficiency at removing sub-micron particulates [94]. Chemical cleaning targeted to organic contaminants removal can be carried out in several ways using wet or dry cleaning agents. Throughput considerations favours spin cleaning where the substrates are rotated at the same time as they are subjected to the interaction of liquid cleaning solutions. Organic solvents or neutral detergents solution can be employed to this effect; the later also favouring adhered particles removal [94]. Dry chemical cleaning in the gas-phase using various plasma chemistries is also efficient at removing organic contaminants, however it is conventionally associated with lower throughput systems.

Ultra-pure deionised water is employed for rinsing surfaces after chemical cleaning. A combination of immersion (with or without ultrasonic agitation) and spraying is commonly employed. Spin drying of the surfaces after cleaning and rinsing is very efficient and suitable for wafer types substrates. Alternatively, Marangoni drying, where the substrates are pulled through a meniscus into an isopropyl alcohol (IPA) atmosphere can be used. As a final cleaning step, complete removal of organic contaminants including residual detergent is carried out by exposure to ozone (generated by UV light exposure in an oxygen rich atmosphere).

3.4.1.2 Alignment layer deposition and treatment

The suitable orientation of the LC molecules necessitates the deposition of an alignment layer on the inner the substrates surfaces. For polymer layers, this is most commonly achieved using spin coating. Alternatively flexographic printing (developed in LCD industry for large rectangular substrates) can be employed. Spin coating provides better thickness control, however the resulting blanket deposition can be problematic. As a result patterning of the alignment layer can be required in order to promote electrical connection over bond pads and inter-substrate adhesion. While this requires an extra etching step in the case of spun cast films, flexographic printing allows selective deposition of the substrates by the use of patterned printing mats.

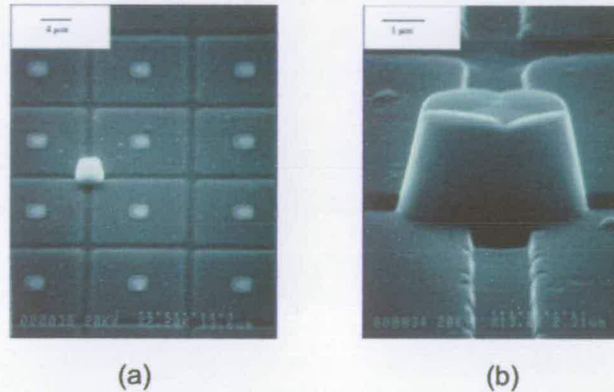
Subsequently to deposition, alignment layers are thermally cured to remove residual solvent (around 100°C). Polyimide films require a further thermal treatment for imidization (around 200°C). Baking can be carried out in batch in ovens or individually on hotplates.

When the "rubbed polymer" alignment method is used, a rubbing or buffing stage is necessary to control the molecular orientation of the alignment material (see chapter 5). As mentioned previously (see figure 2.5) this is typically carried out by bringing the substrates in contact with a rotating roller coated with a velvet-like cloth material. Subsequently, cleaning is necessary to remove particles generated by the buffing process.

3.4.1.3 Cell gap control

Traditionally, in the LCD industry, spacer particles are employed to control the gap between the two substrates of a liquid crystal display or in the case of an LCoS device the silicon chip and the top ITO coated glass electrode. These particulates are made of silica or polymer (e.g. polystyrene) and take the shape of balls or rods. They can be sprayed randomly across the whole surface of one of the substrates by dedicated dispersal techniques or by spin coating in a solvent suspension. Alternatively, the hybrid architecture of LCoS devices provides a unique opportunity to manufacture spacers structure on the silicon chip. Oxide or nitride of silicon can

be used at this effect. The dimensions of the spacer structure are controlled accurately using standard semiconductor fabrication techniques. One of the first attempts to use integrated spacer structures in LCoS devices was reported by IBM [95,96]. As illustrated in figure 3.11, it consisted of fabricating spacer SiO_2 posts regularly spread across the device and positioned at the intersection of four adjacent pixels.



(a) (b)

Figure 3.11: SEM image pf IBM spacer posts made of SiO2 and positioned in the gap between the pixels (reproduced from [95]).

The presence of spacers in the active area can disrupt the liquid crystal alignment in their close periphery. While in direct view nematic based LCDs such features can remain invisible to the user, the magnification associated with LCoS devices is likely to make them more of an issue. Furthermore, in the case of SSFLCs, spacers are known to promote pin defects whose size renders their presence unacceptable under any magnification [97].

In order to prevent such occurrence in FLCoS devices, it is therefore preferable to limit the presence of any spacer structures (particles or fabricated) to the periphery of the device (i.e. away from the pixel array). If spacer particles are to be used, these can be mixed with the perimeter seal material applied to one of the substrates before assembly. Alternatively and in a similar fashion, integrated spacer structures can be fabricated in this peripheral region. The motivation behind uniformly placing spacer across any LC based device is to improve cell gap uniformity. Avoiding the presence of spacers across the active area of devices therefore increase the requirement for substrates flatness. While it can be assumed that glass substrates can be produced with a sufficient degree of flatness it is not the case for the silicon backplane. As it

will be discussed in chapter 4, techniques have been developed to resolve the issue brought by the lack of flatness of the silicon chips.

3.4.1.4 Lamination

Prior to assembling the glass substrate and the silicon wafer together to form a laminate, adhesive material is applied to one of the two substrates. It is common practice to dispense the seal material onto the silicon substrate rather than the glass. The high visibility of patterns at the surface of the silicon substrate can be used for alignment of the dispensing system as well positioning of the glass substrate.

The adhesive material fulfils two functions. It defines the area to be occupied by the liquid crystal and provides the mechanical link between the two substrates. The perimeter seal material can be deposited by flexographic printing using a dedicated patterned printing mat or by robot controlled syringe dispense systems.

The choice of seal material is very critical. It must provide suitable mechanical bonding strength between both substrates within the desired temperature range. In addition, its chemical properties must be such that it does not react with the liquid crystal and exhibits low outgassing.

An interesting alternative approach to conventional seal materials was developed by P. Kazlas [98]. It consisted of using a specialized material known as photo-BCB that acted as spacer, seal and adhesive at the same time.

Once the perimeter seal has been produced, the lamination process can be carried out. Robot systems can be used to flip other the glass substrate and position it accurately onto the glass substrate. Alternatively substrates can be loaded manually into an alignment system.

Several options are available to press both substrates together. Several laminates can be pressed together in a mechanical press. Alternatively, vacuum bag or air bladders can be used to compress the assembly. Curing of the seal material is typically carried out with the laminate under mechanical pressure to in order to achieved the desired cell gap. To improve throughput, partial curing can be selected to allow for curing to be completed in a batch process. The type of seal material employed whether it is cured thermally or by exposure to UV light will affect the approach selected for the lamination process.

3.4.1.5 Singulation

The separation of individual LCoS microdisplays, a process known as singulation, can be carried out by a variety of means. While silicon wafers are traditionally sawn through in the semiconductor industry, LCoS technology requires the glass and silicon substrates to be processed separately prior to the breaking process. As illustrated in figure 3.12, the offset of the silicon chip and the glass cover is necessary in order to make electrical connection to the bond pads of the silicon chips and the inner ITO electrode.

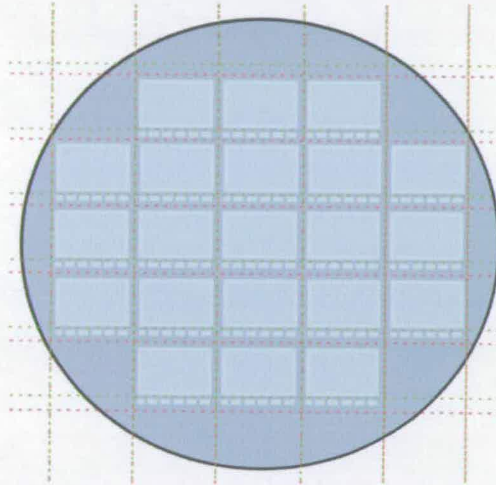


Figure 3.12: Typical scribe patterns employed to separate individual microdisplay devices from the laminates (green for glass and red for silicon).

Scribing of the substrates is often preferred to partial sawing as the cooling fluid associated with the later constitutes a potential source of contamination and is likely to require cleaning. In addition, sawing typically “sacrifices” a large area of material compared to scribing due to the requirements for the width of the blade. The larger singulation channels necessary in that case translates directly in wasted silicon space and potentially in fewer devices per wafer.

Breaking the scribed laminate is done using dedicated equipment, which relies on the application of mechanical pressure above the scribe lines to achieve breaking in a controlled fashion. Systems applying three point pressure to induce localised bending of the laminate can be used. Alternatively systems based on the use of impact bars are also available.

3.4.2 Die scale processing

3.4.2.1 Liquid crystal filling

Following singulation, individual cells are filled with liquid crystal material. Two main approaches can be employed to this effect.

The small amount of liquid crystal can be brought in contact with the cell in the vicinity of the fill hole. Alternatively, the cell can be dipped into a volume of liquid crystal material.

Traditionally the cells and the liquid crystal material will be evacuated in vacuum prior to filling to avoid air being trapped in the cell. The liquid crystal material and the cell are heated so that the material is allowed to flow into the cell in its isotropic phase. Following filling the cell is allowed to cool down slowly to promote the liquid crystal alignment induced by the alignment layers.

Once filling is complete and the cell is at room temperature, it is often necessary to clean the excess of liquid crystal material which has deposited onto the unwanted surfaces of the displays. The fill hole can then be sealed. The plug material typically is a UV curable adhesive as heating of the cell once filled is to be limited to the operating range of the display. Again the material employed must not react with the adjacent liquid crystal.

3.4.2.2 Electrical connection and packaging

The first process step of the LCoS packaging sequence, know as die-attach, consists of mounting the cell onto a carrier board. Over the last decade, flexible printed circuit board have become popular with LCoS manufacturers due to their versatility with respect to integration in customer applications.

LCoS cells can be bonded onto carriers using traditional paste die-attach adhesives or using tape materials. Again the process temperature restrictions on filled devices make the latter option more favourable. Whatever technique is used the die-attach method should not generate excessive stress which could induce deformation of the LCoS cell. In addition, the link between the display and the carrier should exhibit uniform thermal performance.

Interconnection between the carrier board and the LCoS cell is commonly achieved by wire bonding with the process temperature restrictions favouring aluminium wedge technology over gold ball bonding. Wedge bonding is typically applied to the interconnection of LCoS devices using 25-50 μm wires. Following wire bonding it is common practice to encapsulate the fragile bonds to improve the robustness of the resulting connection.

Electrical connection between the ITO coated glass electrode and the carrier is also required. Soldering and the use of electrically conductive adhesives are available for this purpose with the former option presenting obvious throughput.

Chapter 4. Developments in FLCoS backplane processing

4.1 Introduction

This chapter presents developments in the methodology for the post-processing of silicon backplanes. The work is a continuation of the pioneering work carried out in the mid-nineties by the Applied Optics Group at the University of Edinburgh [87,99,100,101].

Developments in dielectric planarisation by CMP presented in section 4.2.1 have been exploited by the author to prepare sample devices for the study of the alignment of SSFLCs. They are the fruit of the research work carried out by D. Calton [102].

Developments of the pixel layer fabrication method presented in section 4.2.2 are the results of collaboration between the various members of the Applied Optics group including the author [103].

The work on the fabrication of integrated spacer structures presented in section 4.3 and the work on flattening of silicon backplanes [104] presented in section 4.4 were carried out by the author. It was inspired by discussion during weekly meetings of the members of the Applied Optics Group. These include D. Calton, G. Bodammer, K. Seunarine, A. Ross, I. Underwood, W. Hossack and D. Vass to name a few.

4.2 Advances in backplane post-processing

4.2.1 Advances in dielectric planarisation

The main challenge associated with the application of CMP to the planarisation of LCoS silicon backplanes is the difference in topography existing across microdisplay devices.

Figure 4.1a shows the surface profile of a 512x512 DRAM silicon backplane after the deposition of 1.5μm of silicon oxide and before planarisation by CMP. The planarisation oxide was deposited by Electron-Cyclotron-Resonance (ECR) Plasma-Enhanced-Chemical-Vapour-Deposition (PECVD). This technique was selected for this application due to its ability to fill gaps such as those existing at the surface of the raw circuitry of silicon microdisplay backplanes [105].

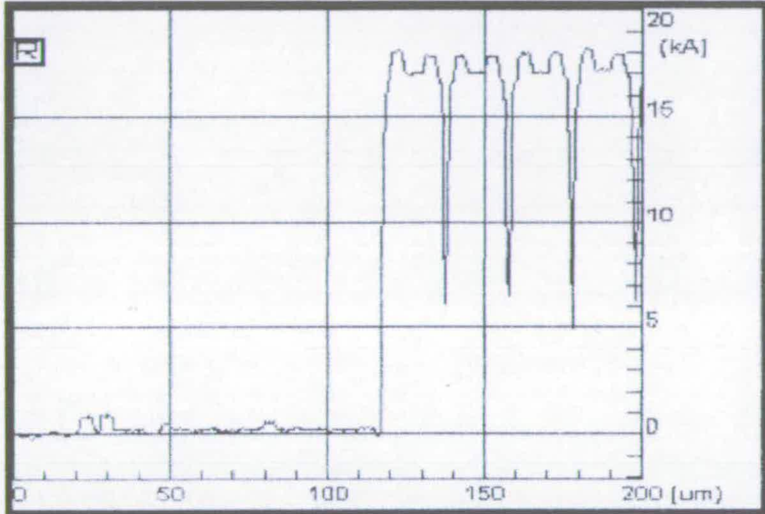
Oxide deposition was carried out using an Oxford Plasma Technology deposition systems using the parameters listed in table 4.1.

N_2O flow rate	35 sccm
SiH_4 flow rate	100 sccm
Substrate temperature	45 °C
Process pressure	5.0 mTorr
Microwave power (2.45 GHz)	280 W
DC Bias	-200 V

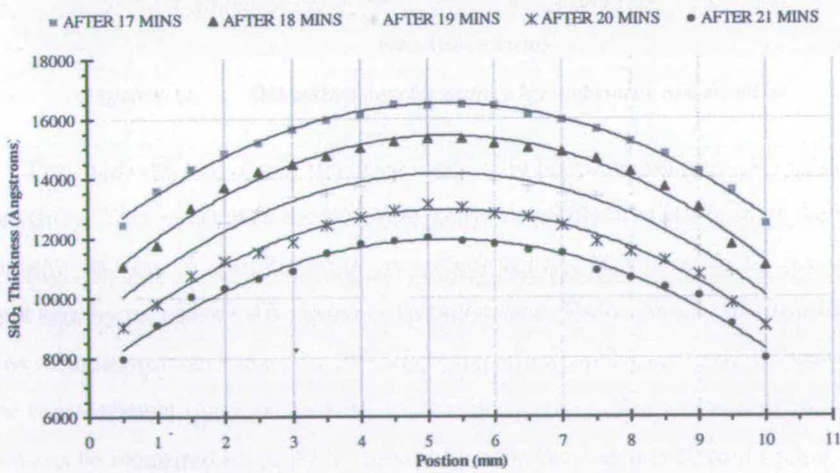
Table 4.1: Process parameters for deposition of planarisation oxide by ECR-PECVD.

As illustrated in figure 4.1b, the straight application of CMP to the topography resulting from the deposition of the dielectric layer onto the raw circuitry results in a poor level of global planarisation. The "doming" above the pixel array is caused by the difference in pattern density existing between the pixel array and its periphery. The higher pattern density above the array results in a lower polishing rate so that more oxide remains following polishing [102,106]. The induced variation in the planarising dielectric layer thickness will in turn result in cell gap non-uniformity across the active area of the microdisplay. The profile of oxide thickness across the

backplane is created at the early stage of the CMP process and remains as polishing progresses. Longer polishing results in a thinner and not flatter oxide layer (see figure 4.1b). CMP for this work was carried out using a Presi Mecapol E460 Polishing machine. The parameters employed for silicon oxide planarisation are listed in table 4.2.



(a)



(b)

Figure 4.1: Surface profile of an unplanarised 512x512 DRAM backplane showing the difference in pattern density between the pixel array (right) and its periphery (left) (a). Oxide thickness profiles obtained after CMP of the dielectric layer deposited onto a 512x512 DRAM backplane (b). [Courtesy of D. Calton]

A technique known as pre-CMP etch back was developed in order to solve the issue discussed above [102,104,107,108]. It consists of reducing the oxide thickness in the region exhibiting lower polishing rate to account for the difference in removal rate. As shown in figure 4.2a, this is achieved by patterning a photoresist layer to cover the periphery of the microdisplay backplane allowing etching of the oxide on top of the pixel array.

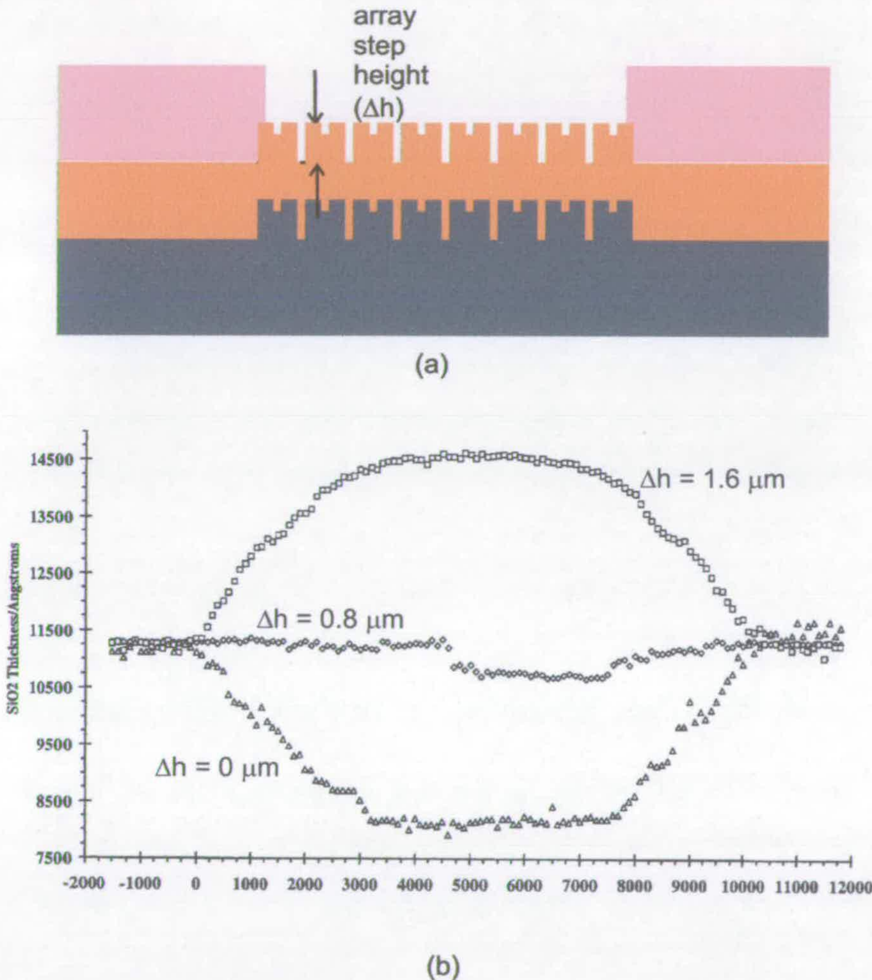


Figure 4.2: The array step height is reduced by conventional etching prior to CMP (a). Oxide thickness profiles obtained brought by the application of CMP to devices with various oxide array step heights (b). [Courtesy of D. Calton]

Figure 4.2b shows the oxide thickness profiles resulting from the polishing of devices with various step heights between the array and its periphery. As mentioned previously, polishing of the devices immediately after oxide deposition (array step

height = 1.6μm) results in doming. Etching away the oxide above the array so that it is level with the surrounding area (array step height = 0 μm) causes dishing. Reducing the step height to 0.8μm enabled a very high level of planarisation to be achieved across the surface of the devices despite the difference in topography. Etching of silicon oxide was carried out using a Plasmatherm PK2440 system. The etch recipe is detailed in table 4.3.

	Blanket SiO_2 CMP	Oxide Buffing	Al CMP
Head Pressure	0.6 bar	0.5 bar	0.4 bar
Head Speed	60 rpm	30 rpm	15 rpm
Platen Speed	60 rpm	30 rpm	10 rpm
Back Pressure	0.2 bar	0.15 bar	0.2 bar
Slurry	Klebasol 30H50	Klebasol 30H50	Rodel QCT1010
Pad	Rodel IC14000	Rodel IC14000	Rodel IC14000

Table 4.2: Process parameters for the various polishing steps involved during the post-processing of silicon backplanes.

4.2.2 Advances in pixel layer fabrication

4.2.2.1 Limitations of conventional post-processing procedure

As mentioned previously in chapter 3, a post-processing procedure was developed in the early nineties to increase the fill factor of silicon backplanes for LCoS applications. The procedure is summarised in figure 4.3. A conformal silicon oxide layer is planarised by CMP. Via holes are etched to allow for electrical contact between the microdisplay driving circuitry and the pixel layer subsequently deposited. Reactive Ion Etching (RIE) of planarised silicon oxide was carried out using a Plasmatherm PK2440 system (see table 4.3). A Balzers BAS450 dc-magnetron sputtering system was employed for aluminium deposition. The metallization process parameters are listed in table 4.4.

Etching of the aluminium layer was carried out using a STS Multiplex Load Locked RIE system using the parameters listed in table 4.5.

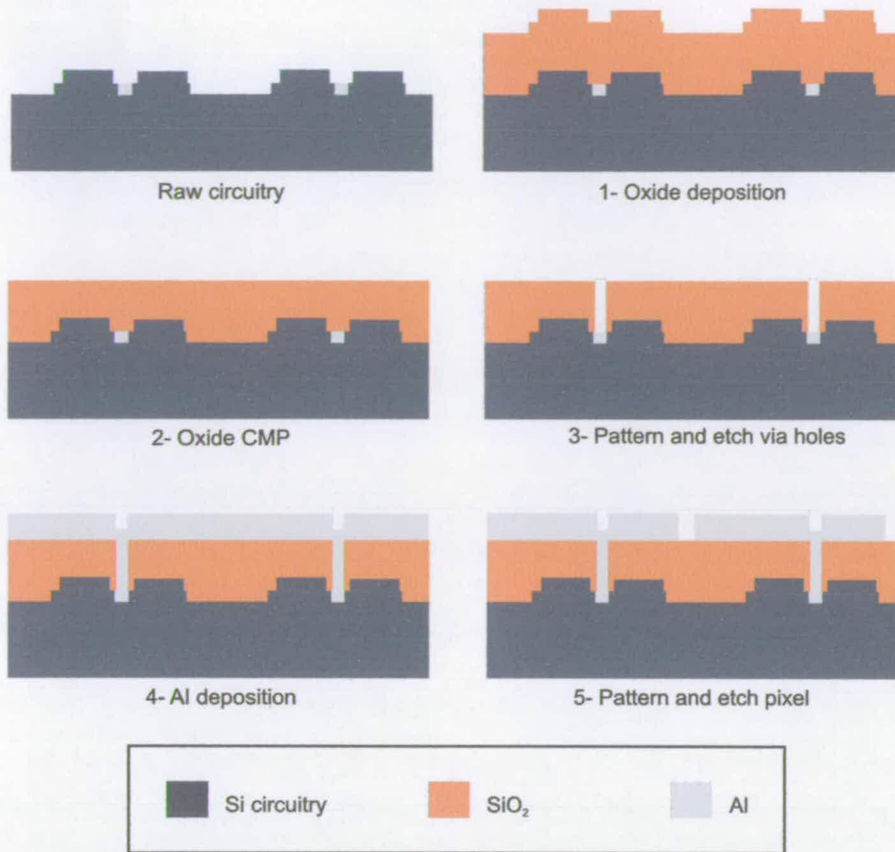


Figure 4.3: Process flow used for conventional post-processing of silicon backplanes

CHF_3 flow rate	75 sccm
He flow rate	15 sccm
RF power (13.56 MHz)	750W
Process pressure	1 mTorr

Table 4.3: Process parameters for etching of silicon oxide using the Plasmatherm PK2440 RIE system.

As illustrated in figure 4.4, this approach produces rough mirror surfaces. The roughness of the pixel layer resulting from the conventional post-processing procedure is caused by both the thickness of material deposited and the deposition conditions employed. In order to fill the opening in the dielectric layer (typically 1 μm thick after CMP) a 1.5 μm metal layer is deposited. Sputtering using high power settings is required to achieve satisfactory filling of the vias (see table 4.4).

	Thick mirror deposition	Thin mirror deposition
Power	2000 W	1000 W
Process pressure	2 mbar	2 mbar
DC bias	- 800V	- 600V

Table 4.4: Aluminium deposition of the aluminium pixel layer using the Balzers BAS 450 system.

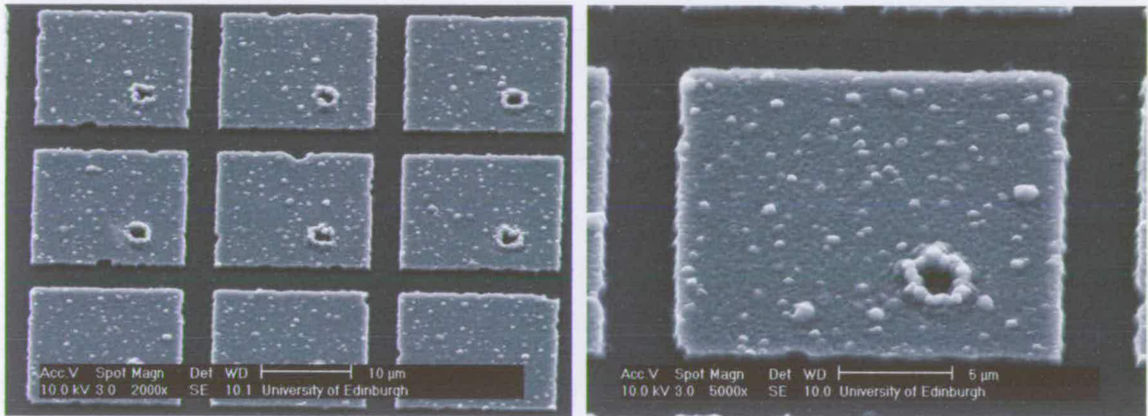


Figure 4.4: SEM images showing the topography of the pixel layer resulting from the conventional post-processing procedure.

The roughness of the mirror layer reduces the amount of light reflected by the backplane. It has been shown to affect the flow of liquid crystal during the filling process [109]. The effect of the roughness of the pixel layer on the alignment of FLCs will be discussed later in chapter 5.

$SiCl_4$ flow rate	37 sccm
Cl_2 flow rate	15 sccm
Process pressure	100 mTorr
RF Power (13.56 MHz)	125 W

Table 4.5: Process parameters for the etching of the aluminium pixel layers using the STS Multiplex system.

4.2.2.2 Enhanced post-processing procedure

A new post-processing sequence was developed to improve the surface of the pixel layer. It relies on the separation of the metallization steps used to connect the circuitry to the pixel and used to define the pixel layer. This is made possible by the introduction of a metal CMP step between the two metallization steps. The process flow of the enhanced post-processing procedure is illustrated in figure 4.5.

Following the oxide planarisation step by CMP, via holes are fabricated and filled with aluminium as in the conventional approach. A metal CMP step is introduced to remove the rough metal layer leaving the via holes filled with metal. The pixel layer can now be fabricated by sputtering a much thinner aluminium layer (0.1 μm) using lower power settings. Faster metal polishing rates at the edge of the wafer have been found to result in scratching of the oxide layer in this region [102]. A CMP oxide buffing step is introduced between the two metallization steps to counter this effect.

The process parameters for the aluminium polishing and oxide buffing steps are listed in table 4.2.

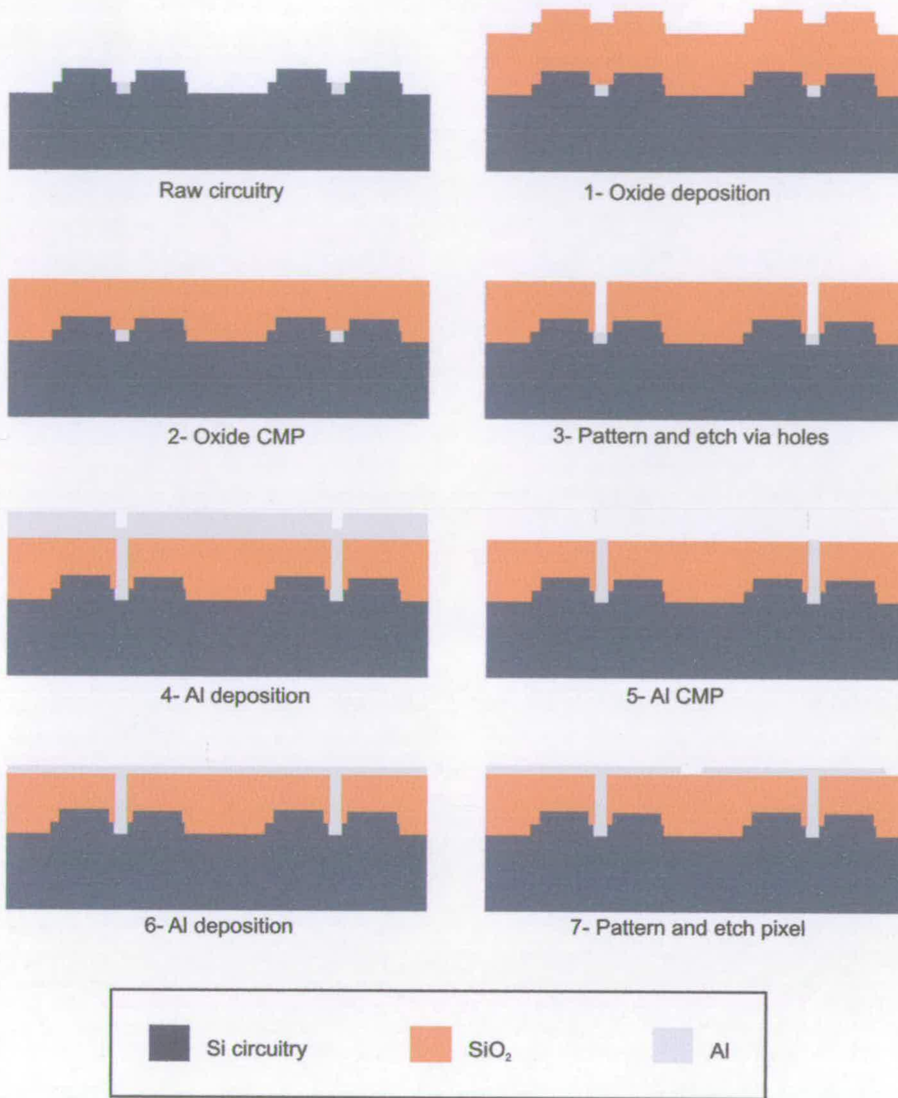


Figure 4.5: Process flow used for enhanced post-processing of silicon backplanes.

Figure 4.6 shows the enhanced post-processing procedure results in a much smoother pixel layer. Figure 4.7 shows the resulting improvements in terms of reflectivity across the visible spectrum. The reflectance values presented are relative to that of a 100nm thick aluminium layer deposited onto bare silicon by thermal evaporation. The reflectivity was measured on blanket layers (i.e. prior to lithography for pixel etching) in order to avoid discrepancies due to a difference in fill factor brought by the etching of different thickness. The effect of the improved pixel topography on the alignment of FLCs will be discussed in more details in chapter 5.

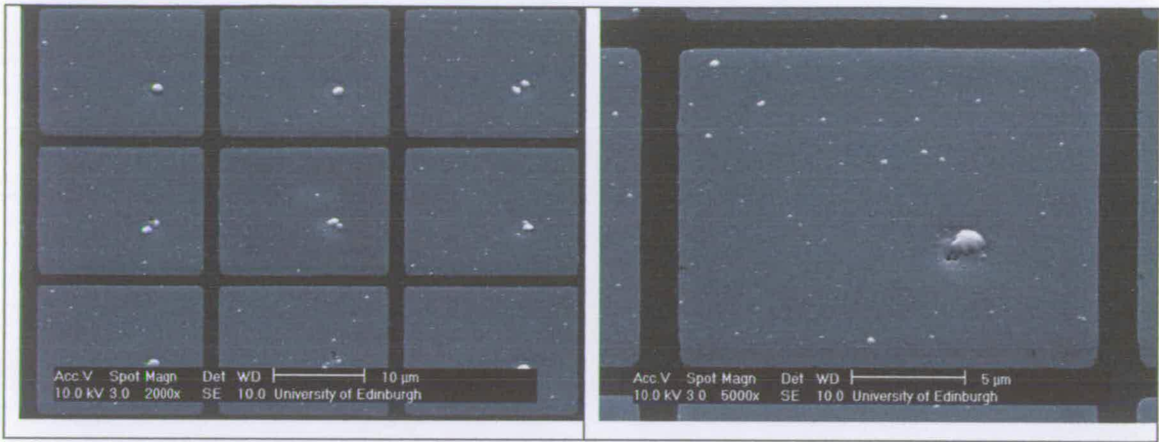


Figure 4.6: SEM images showing the smoother topography of the pixel layer resulting from the enhanced post-processing procedure.

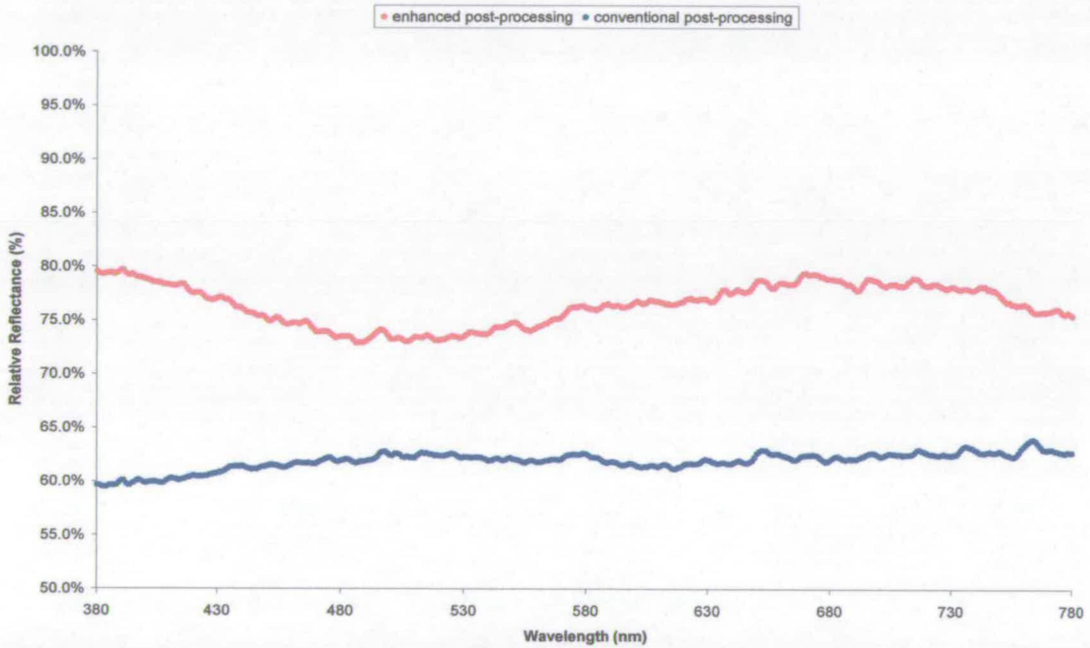


Figure 4.7: Reflectivity spectra in the visible region from blanket pixel layers fabricated using the conventional (1.5µm thick) and the enhanced post-processing procedure (0.1 µm thick).

4.2.2.3 Embedded pixel technology

The improved post-processing procedure presented above leads to significant improvement in pixel optical properties but still sees recessed inter-pixel gap. Work was carried out to develop a technique which would permit the dielectric layer between the pixels to be level with the surrounding surfaces in an effort to reduce impact of the addressing circuitry onto the liquid crystal layer.

The damascene approach illustrated in figure 4.8 relies entirely on metal CMP to level the pixel mirror with the inter-pixel gap dielectric. While being theoretically the simplest method, the damascene process sequence was found in practice to lead to significant amount of pixel dishing [102]. In addition, scratching and post-CMP cleanliness were found to be potential issues towards the production of backplanes of high optical quality using the damascene process.

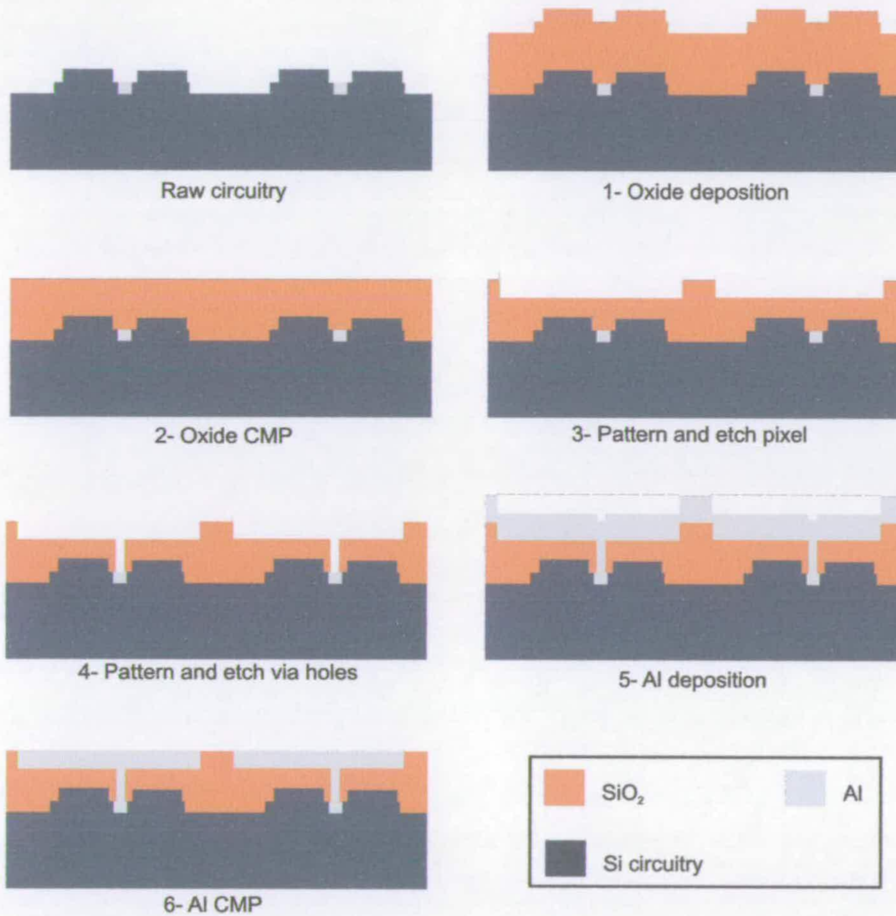


Figure 4.8: Process flow for damascene process used to produce embedded pixels on microdisplay backplane.

An alternative method, known as Self Aligning Insulator Filled Trench (SIFT) process was developed in an attempt to fabricate backplanes with level inter-pixel gap. As shown in figure 4.9, it consists of exploiting the photoresist layer employed to define the pixel electrode in order to selectively deposit dielectric material between the pixels. Deposition via thermal evaporation combined with photoresist

removal by ultrasonic immersion in acetone were found to give the best results [102]. Filling of the inter-pixel gap brought by the SIFT process resulted in improvements in liquid crystal flow [109]. The effect of the filling of the inter-pixel gap on the alignment of FLCs will be discussed in chapter 5.

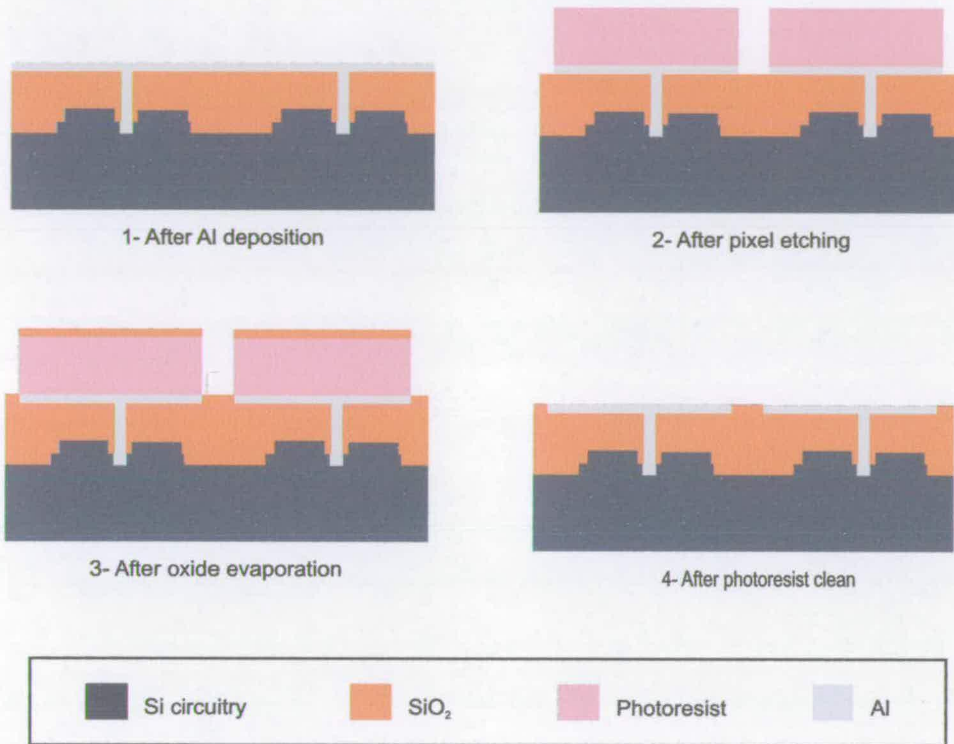


Figure 4.9: Process flow for SIFT process where silicon oxide is deposited between the pixels.

4.3 Integrated spacers

4.3.1 Peripheral glue guide spacer

Particulate type spacers have been traditionally used to control the cell gap of liquid crystal displays. Their use has several disadvantages. As illustrated in figure 4.10, hard particulate spacer made of silica can become embedded into the softer aluminium pixel layer during cell assembly. Particulate spacers are also challenging to handle in cleanroom environments and are not available in all sizes. Agglomeration of spacer particles in the active area of microdisplay devices is also problematic due to the magnification required to view images from LCoS

microdisplay devices. Finally, FLCs are known to be very sensitive to the presence of spacer structure [110,111]. Results from work on the interaction between spacers and FLCs will be presented in the following chapters.

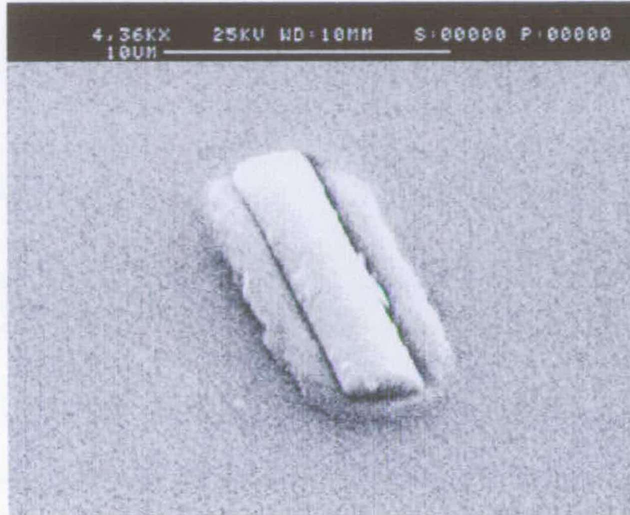
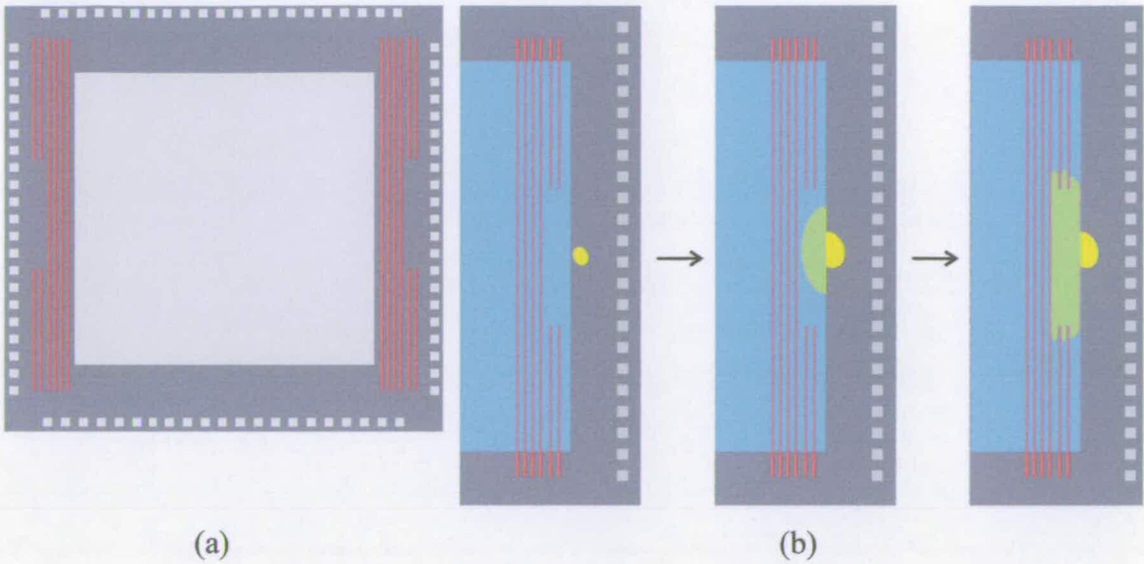


Figure 4.10: SEM image of a silica spacer particle embedded into the aluminium pixel layer [courtesy of M. Begbie].

The design of the 512x512 DRAM device is such that bond pads are present on its four sides. This feature makes wafer-scale lamination impractical. An integrated spacer structure was developed for the 512x512 device. As illustrated in figure 4.11a, its geometry is limited to the periphery of the pixel array.

In addition to providing cell gap control it was designed to act as glue guide to facilitate die-scale device assembly. Channels were used to control the spread of glue in the direction parallel to the long axis of the spacer structure.



(a) (b)

Figure 4.11: Schematic illustration of the peripheral spacer structure designed for the 512x512 DRAM device (a). The channels of the spacer structure guide the glue away from the pixel array during assembly (b).

In practice a 30 Gauge needle was employed to dispense a small volume of UV curable adhesive at the edge of the cover glass. Norland NO68 adhesive was selected for this application due to its suitable viscosity (see Appendix A). The cover glass was held mechanically against the spacer structure using spring loaded clips. After the initial spread of the glue brought the material in contact with the edge of the cell, capillary forces were found to accelerate the spread of glue within the cell. After the amount of adhesive which penetrated the cell was judged sufficient to provide a suitable level of adhesion between the silicon chip and the cover glass, the edge of the cell were exposed to UV light in order to cure the glue.

4.3.2 Spacer fabrication

The lift-off approach has been employed in the past to fabricate spacer structures onto silicon backplanes [112]. As illustrated in figure 4.12, this technique relies on photoresist to limit were a material is deposited as opposed to where it is removed in case of a standard etching process. The motivation behind the use of this method is to avoid exposing the dielectric material in the inter-pixel gap to the etching conditions.

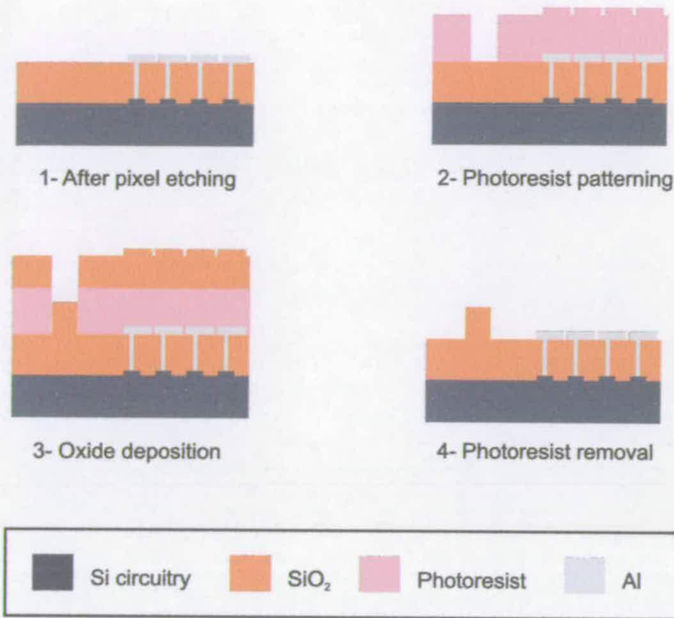


Figure 4.12: Process flow for fabricating the spacer structure using the lift-off method.

This section discusses an alternative approach by which spacer structures can be manufactured on the periphery of the pixel array of silicon backplanes using a standard etching process (i.e. where material is removed depending on the overlying photoresist pattern). As illustrated in figure 4.13, the spacer layer is patterned over the blanket pixel layer. The latter is subsequently wet etched to define individual pixels. The reduced thickness of the pixel layer brought by the enhanced post-processing procedure makes it possible for wet aluminium etching to be used. Isotropic etching of thicker layers would results in large lateral over-etch.

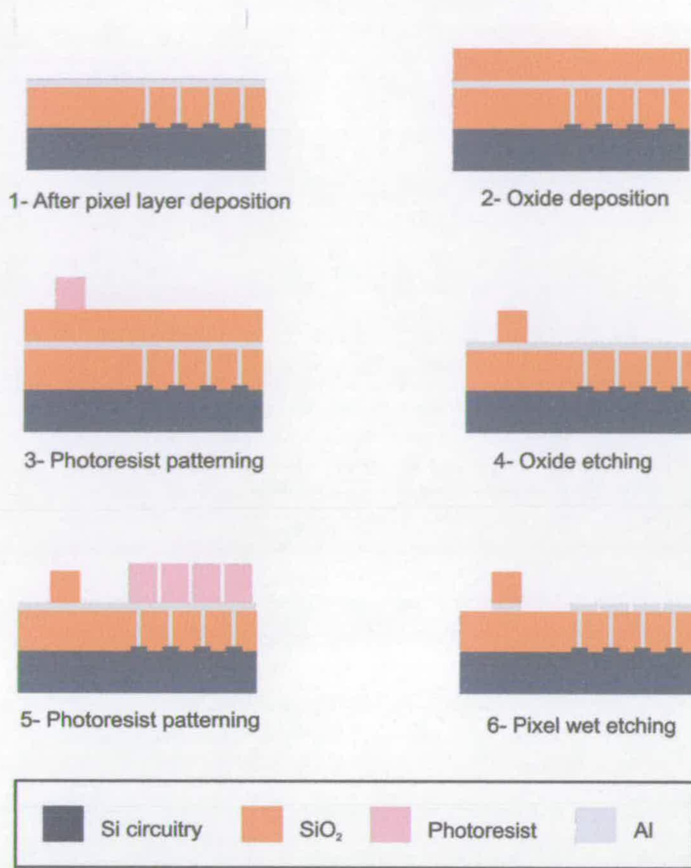


Figure 4.13: Process flow for the alternative method to fabricating peripheral spacer structure using a standard etching approach.

Samples were prepared by sputtering 0.1 µm aluminium onto thermally oxidised silicon wafers to simulate the pixel layer. A 2.4 µm thick silicon oxide was deposited by ECR-PECVD to form the spacer layer which was subsequently patterned by a standard photolithography process followed by RIE as described previously. Finally a second photolithography process was carried out to allow for the patterning of individual pixels in the aluminium layer by wet etching.

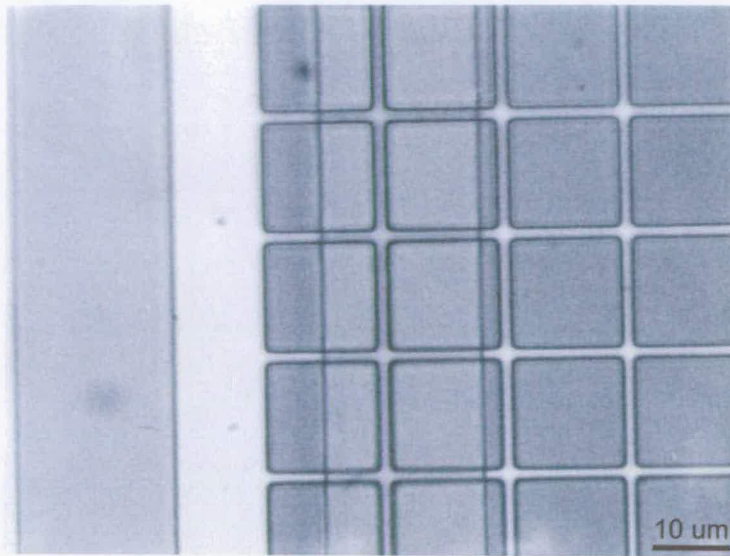


Figure 4.14: Micrograph of spacer structure with offset pixel photoresist pattern.

In order to verify the limited impact of the presence of the spacer onto the lithography step used to etch the pixel electrodes, the photoresist pattern was deliberately printed to overlap with one of the channels of the spacer structure. As can be seen in figure 4.14, photoresist patterns for pixel etching can be produced successfully in close proximity to the spacer structure.

The impact of the spacer structure on the coating of the alignment layer was assessed in a similar fashion. A substrate with 2.4 μm thick spacer channels was coated with a 50 nm thick polyimide alignment layer and subsequently rubbed in a direction parallel to the long axis of the spacer structure to promote liquid crystal alignment. A cell was prepared using 3.1μm spacer particles so that the top of the silicon oxide structure did not contact the cover glass. Figure 4.15 shows the resulting alignment of FLC material CS 1031 (Chisso Corporation). The spacer structure does not appear to disrupt the aligning properties of the polyimide film. The details of the test cell preparation, alignment layer coating and rubbing will be presented in more details in chapter5.

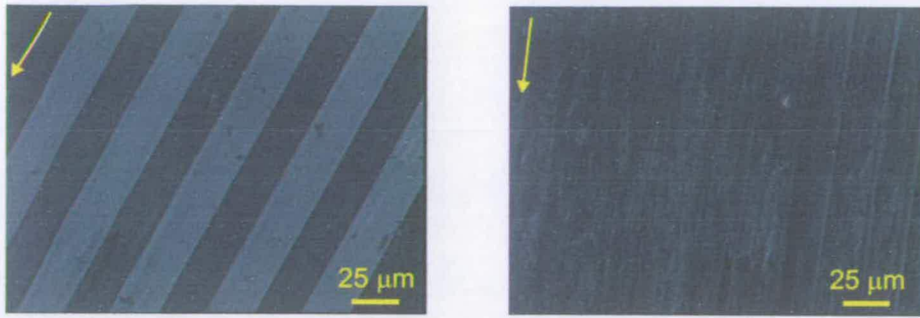


Figure 4.15: Micrographs showing the FLC alignment achieved by rubbing of a polyimide film spin coated above the spacer structure. The arrows indicate the rubbing direction.

The effect of the silicon oxide etch conditions on the topography of pixel surface was investigated by Atomic Force Microscopy (AFM). 0.1µm thick aluminium was sputtered on thermally oxidized silicon wafer using the parameters listed in table 4.4. Five 5x5 mm dies from the wafer samples were imaged after the deposition and after 5, 10, 20 and 40 mins exposure to the etching environment described in table 4.3. For each sample the roughness was measured across a 1x1µm area. As illustrated in figure 4.16, the oxide etch chemistry does not affect the aluminium surface dramatically. Some form of pitting could however be observed after 20 mins which become more obvious after 40 mins. Roughness measurements presented in figure 4.17 confirmed the AFM observations with a slight increase in RMS after 20 mins. The experimental work suggests that the aluminium pixel layer can be safely used as etch-stop for etching of the spacer layer as long as the overetch period is kept below a maximum of 10 mins. This translates in a 15% overetch for a 1µm thick oxide layer etch at a rate of 30 nm/min under the conditions described in table 4.3.

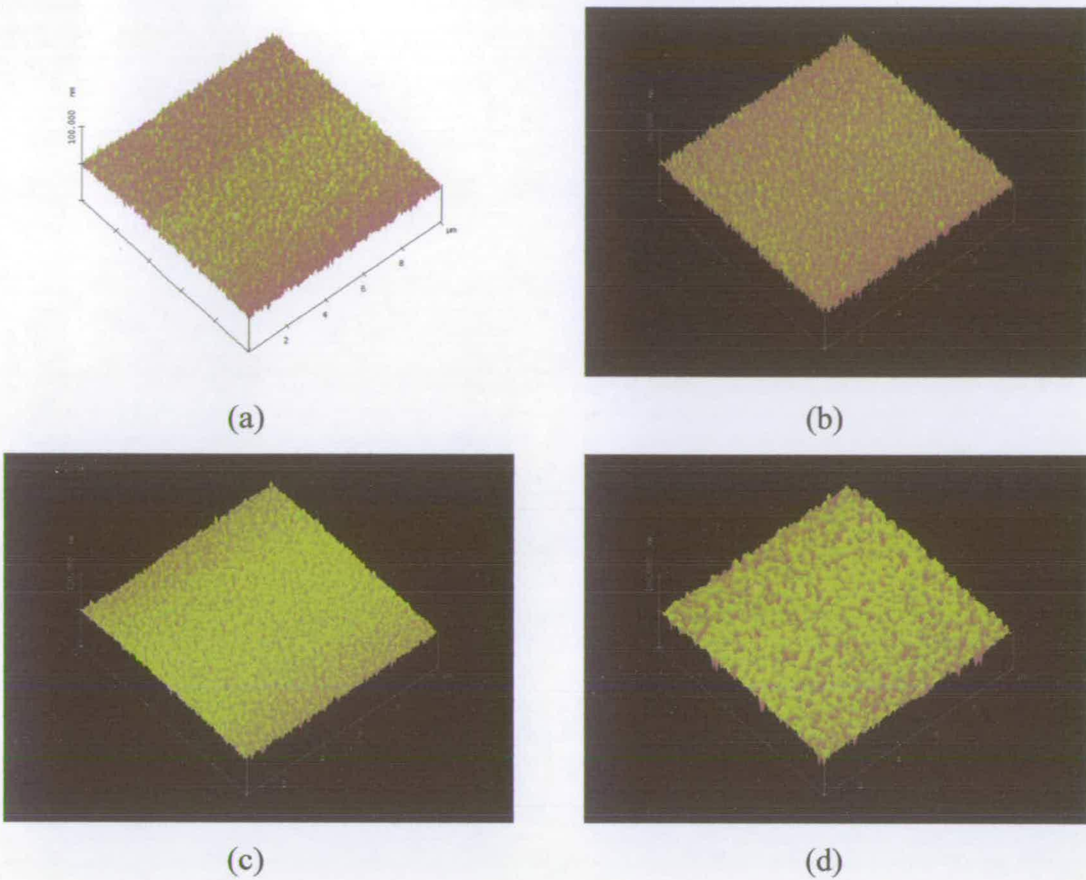


Figure 4.16: AFM images showing the effect of the oxide etch chemistry on the topography of the aluminium pixel surface. 0.1 µm as deposited (a), after 5mins (b), 10 mins (c) and 40 mins (d) exposure to the oxide etch conditions detailed in table 4.3.

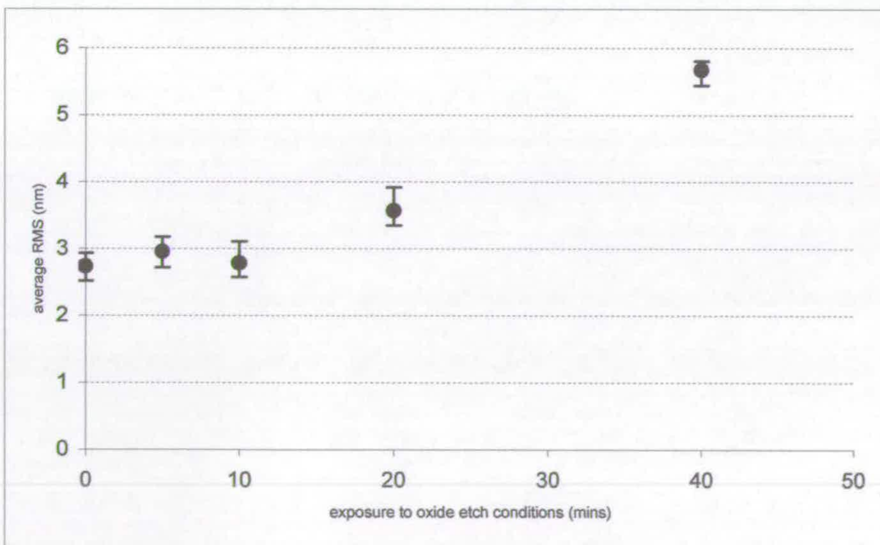


Figure 4.17: Graph showing the variation in roughness (measured by AFM) brought by exposure to oxide etch conditions detailed in table 4.3.

4.4 Backplane flattening

4.4.1 Flatness of LCoS backplanes

As mentioned previously the flatness of silicon backplanes used in LCoS is very critical to their performance. This is particularly true in the case of FLCoS technology where small cell gap requirements and the electro-optical properties of the SSFLC layer combine to make the performance of such devices very sensitive to variations in cell gap.

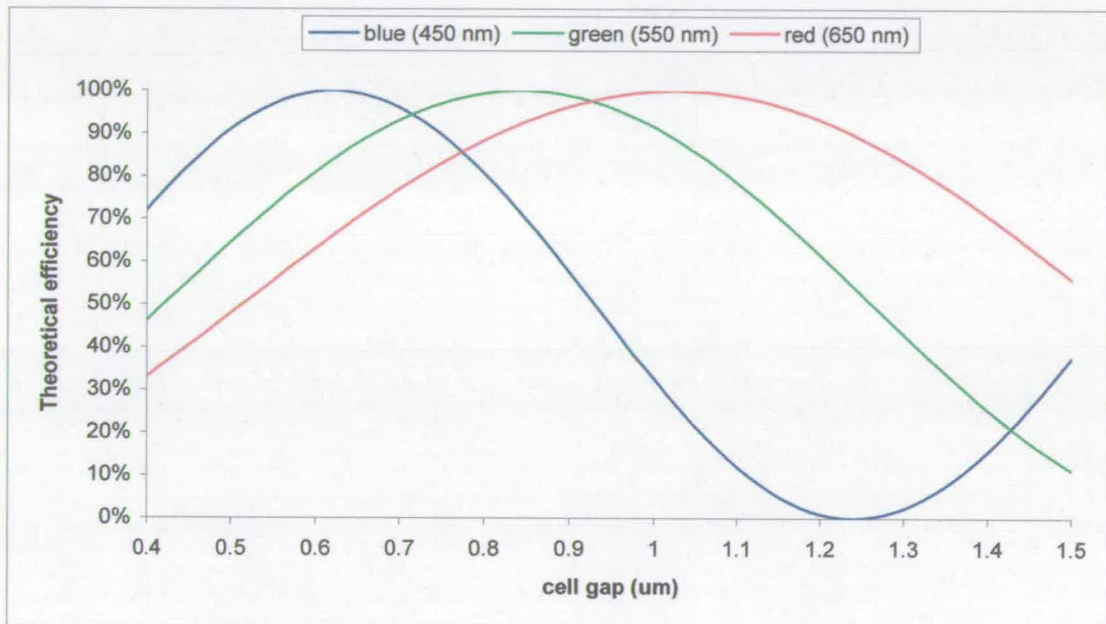


Figure 4.18: Graph showing the effect of cell gap on the theoretical electro-optical efficiency of a reflective SSFLC cell assuming 45° switching angle for red (650nm), green (550nm) and blue (450nm) light.

Figure 4.18 shows the theoretical electro-optical efficiency in reflection of a SSFLC layer as function of its thickness for the liquid crystal material FELIX 015-100 used in this work (see Appendix A). The plot is derived from equation 2.2 assuming an ideal tilt angle of 22.5°. The variation of the birefringence of the FLC with wavelength was estimated by fitting the experimental data provided by the FLC supplier to a polynomial as shown in figure 4.19.

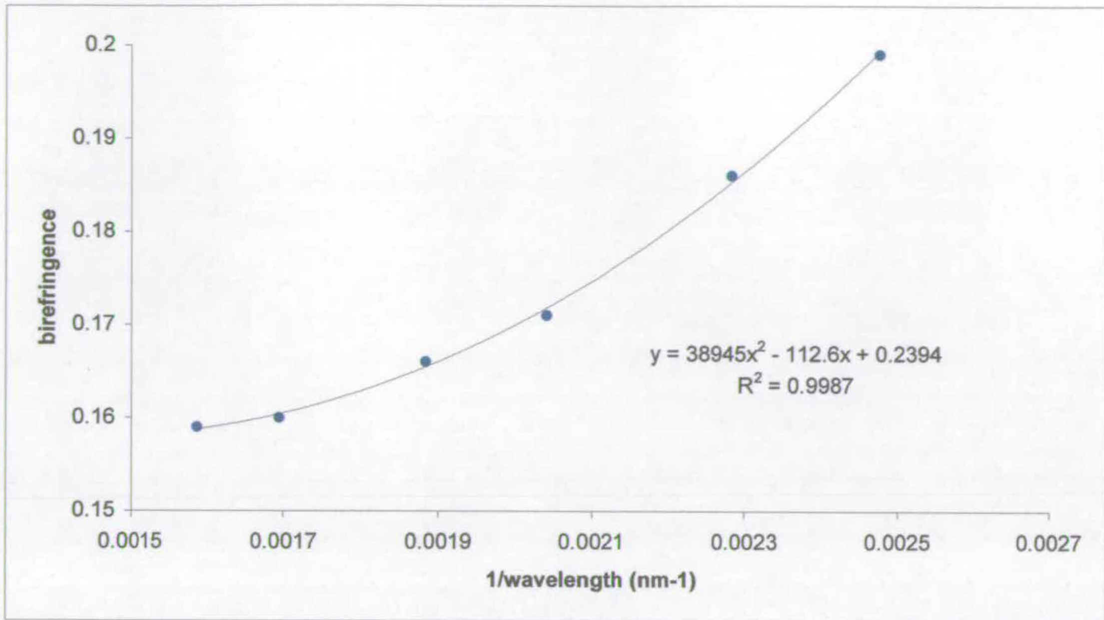


Figure 4.19: Experimental data and polynomial fit for the variation of the FLC birefringence with wavelength.

Bodammer highlighted the impact of the presence of CMOS circuitry on the flatness of LCoS silicon backplanes by comparing their shape before and after removing the circuitry by etching [113]. Thermal stresses caused by difference in coefficient of thermal expansion between two materials increase with temperature. High temperature processes involved in the manufacturing of transistors such as ion implant anneal and thermal oxidation have been known to cause plastic deformation of silicon wafers [114]. In addition the strain induced by lattice mismatch in diffusion regions [115] and nitride layer deposition [116] will also result in stress build up which will participate the overall deformation of silicon substrates. While the stress forces can be minimized by optimisation of the processing parameters, one must note that warpage will always results from processing.

4.4.2 Backplane flatness measurement

A technique known as scanning white light interferometric microscopy was used to assess the deformation of silicon substrates in this work. It relies on the Frequency Domain Analysis (FDA) analysis of the interference patterns resulting from the optical path difference between the light reflected from the sample surface and that

of a reference beam. As illustrated in figure 4.20, white light is directed to a Michelson interferometer objective which is moved in the z-direction using a precision piezoelectric transducer. The resulting series of interferograms are collected by a camera sensor and transferred to PC for analysis. The sample surface is positioned onto a XY stage to allow for mapping of areas larger than the field of view of the objective. This very powerful technique outputs 3D maps of the sample surface and calculates the radius of curvature of the surface analysed.

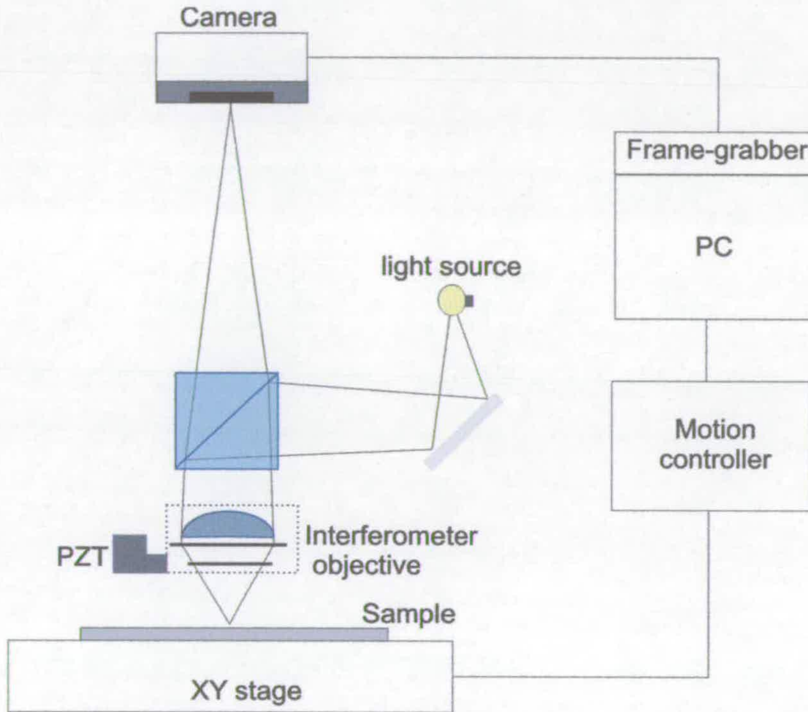


Figure 4.20: Schematic illustration of the Zygo NewView 100 system used to measure the deformation of silicon backplanes.

Figure 4.21 shows the surface profile from a singulated 512x512 DRAM silicon backplane after post-processing. As can be seen, the chip exhibits a significant degree of bow with the centre of the array being higher than the surrounding area. Attempts to analyse singulated non-planarised 512x512 backplanes by scanning white light interferometry proved unsuccessful due to reduced reflection and strong scattering. As illustrated in figure 4.22a, stylus based surface profilometry using a DEKTAK Model IIA system revealed that the intrinsic stress of the circuitry did

cause the backplane to bow in a concave fashion (i.e. with the edge of the array higher than its centre).

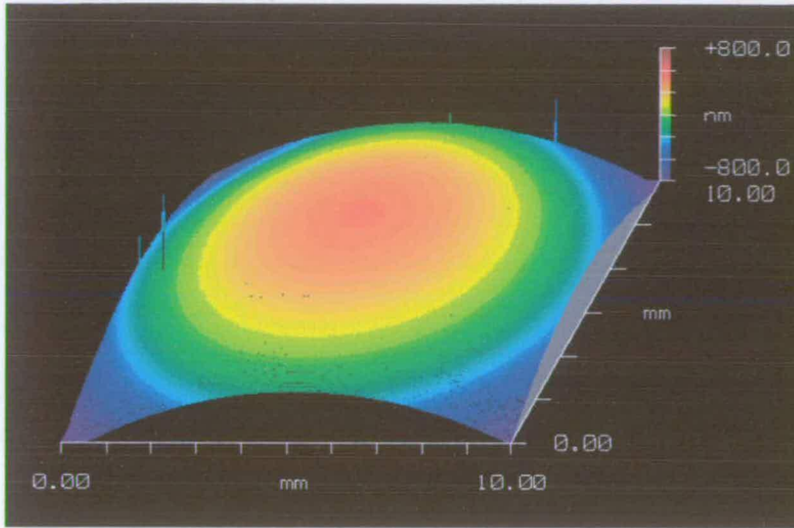
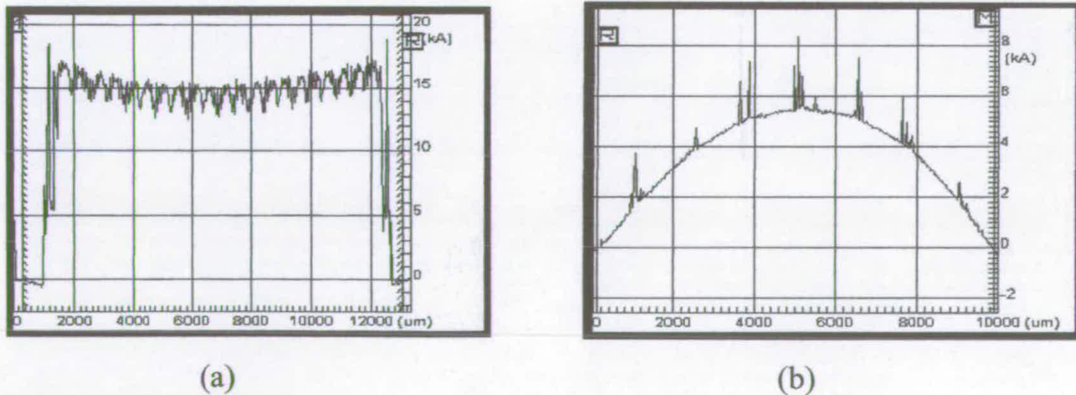


Figure 4.21: Altitude map (from ZYGO NewView 100) of a post-processed 512x512 device showing a convex bow.

To rule out any discrepancy regarding the direction of bow due to the difference in measurement methods, a post-processed device was measured using the DEKTAK system. As shown in figure 4.22b, stylus profilometry results were in agreement with white light interferometry measurements showing that the post-processing procedure causes the backplanes to become convex. Among the various causes of stress comprised in the post-processing procedure, the planarisation oxide layer was the first "suspect".



(a) (b)

Figure 4.22: Surface profile (from DEKTAK Model IIA) of a 512x512 DRAM backplane before (a) and after (b) post-processing.

Films of various thicknesses of silicon oxide were deposited by ECR-PECVD on the back of silicon dies singulated from a 380 um thick Si(100) wafer. The curvature of the front of the dies (polished side) was measured using the ZYGO system described above before and after deposition. Figure 4.23 shows the change in curvature (k=1/R) for increasing film thickness.

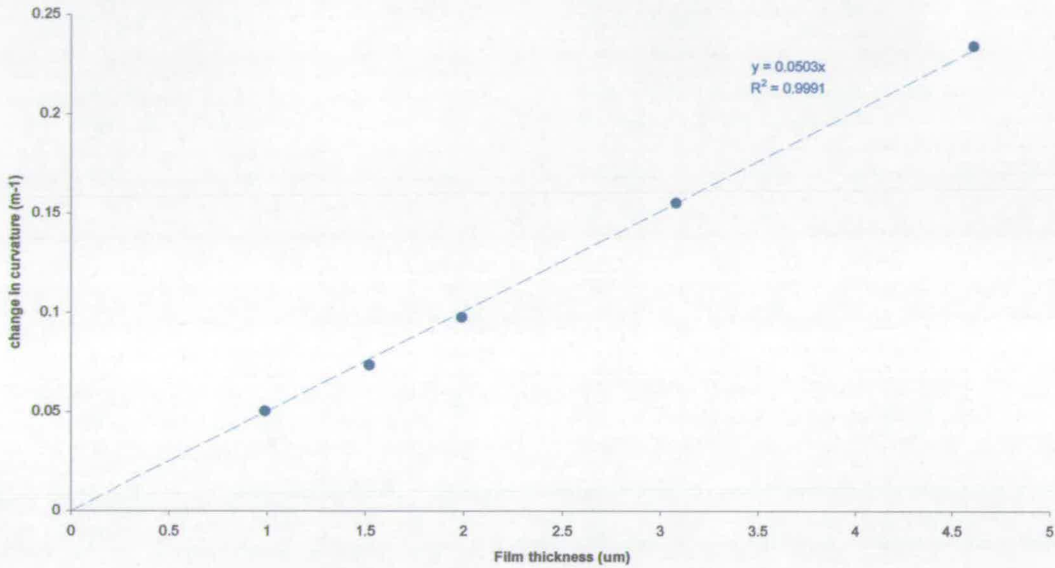


Figure 4.23: Graph showing the change in curvature brought by ECR-PECVD oxide films.

Equation 4.1 below derived from Stoney's formula [117] describes the relationship between the film stress σ and the radius of curvature of the substrate. It was used to calculate the stress of the ECR-PECVD film to be around 215 MPa assuming a biaxial modulus of 180 GPa for Si(100) [118].

$$\sigma = \left(\frac{1}{R_2} - \frac{1}{R_1}\right)\frac{E_s}{(1-\upsilon_s)}\frac{t_s^2}{6t_f} \quad (4.1)$$

with: E_s the Young's modulus of the substrate material

t_f the film thickness

t_s the substrate thickness

υ_s the Poisson's ratio of substrate material

R_1 the radius of curvature of the substrate before film deposition

R_2 the radius of curvature of the substrate after film deposition

Despite the deposition process taking place near room temperature, the resulting oxide film exhibits a high level of compressive stress which in turn causes significant substrate bow. As an indication, each μm of ECR-PECVD SiO_2 will result in a difference in altitude of 0.32 μm between the centre and the edge of a 10x10 mm silicon die.

4.4.3 Flattening of silicon backplanes

The investigation of the stress properties of the planarisation oxide layer and its effect of the bow of silicon substrate inspired a flattening method known Film Stress Compensation (FSC). It relies, rather simply, on the deposition of thin films on the backside of silicon backplanes to compensate for the bow caused its intrinsic stress (caused by CMOS circuitry fabrication and post-processing procedure).

The advantages of this approach over other strategies [112,107 ,119] include the absence of a need for supporting/flattening substrate, low sensitivity to particulate contamination, good uniformity and repeatability.

The high degree of linearity in figure 4.23 indicates that the stress properties of oxide films deposited by ECR-PECVD show little variation against thickness or deposition time. ECR-PECVD oxide is therefore suitable for correcting large backplane deformation.

In addition, silicon nitride films deposited by ECR-PECVD (see table 4.6) were found to exhibit tensile stress properties (E = 130 MPa) making them suitable for flattening of "bowl" shaped backplanes by the FSC method.

Flow rate N_2	1960 sccm
Flow rate SiH_4	40 sccm
Flow rate HN_3	55 sccm
Substrate temperature	300 °C
Process pressure	900 mTorr
RF power (13.56 MHz)	20 W

Table 4.6: Process parameters for the deposition of silicon nitride by ECR-PECVD using the Oxford Plasma Technology system.

For the reasons above silicon backplane flattening by the deposition of blanket oxide or nitride films is a very promising method. However its efficiency is limited by the need to have a symmetrical bow to achieve high level of flatness in all directions. As shown by Bodammer [113] the bow symmetry is not always guaranteed for LCoS silicon backplanes. Figure 4.24 shows the curvature profiles of a post-processed 512x512 device exhibiting bow symmetry of 0.8.

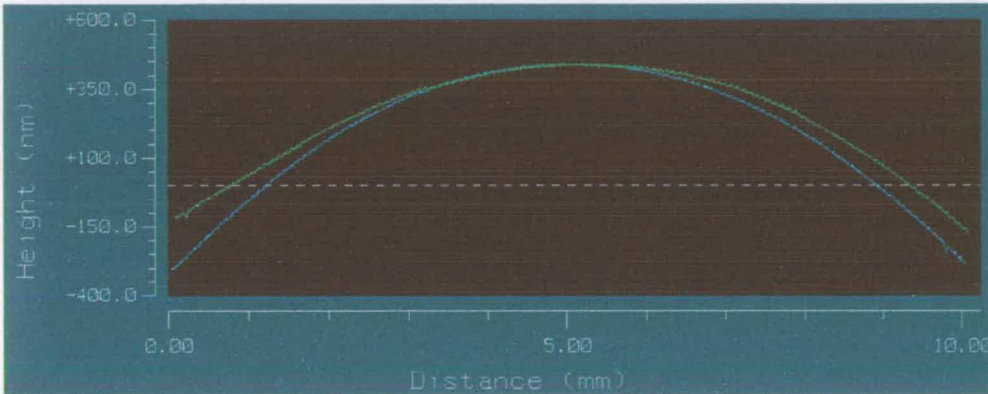


Figure 4.24: Curvature profiles in X (green) and Y (blue) of a post-processed 512x512 device showing unsymmetrical bow.

Experimental work was carried out to evaluate the effect of patterning the oxide/nitride films on the backside of the silicon backplanes in order to control the symmetry of the resulting stress. Breakdown of the ECR-PECVD deposition system required the use an alternative PECVD system (see table 4.7). Due to higher deposition temperatures oxide films produced were found to exhibit compressive stress values around 320 MPa.

Flow rate N_2	392 sccm
Flow rate SiH_4	10 sccm
Flow rate N_2O	1420 sccm
Substrate temperature	300 °C
Process pressure	900 mTorr
RF power (13.56 MHz)	30 W

Table 4.7: Process parameters for the deposition of silicon oxide by PECVD using the STS Multiplex PECVD system.

Oxide films of various thicknesses (t) were deposited on the back of 380 μm thick 3”diameter Si(100) wafers. Photolithography using a Cobilt 2020 contact printer system were carried out prior to etching using the Plasmatherm PK2440 RIE system (see process details in table 4.3). Three stripe patterns were fabricated with constant pitch and varying stripe width (see figure 4.25 and table 4.8). Areas of the wafers were also blanket etched to be able to evaluate the change in curvature brought by these patterns. Four dies for each type of pattern (stripes, blanket etch and blanket film) were singulated by sawing. The curvature of their front surface was measured using ZYGO NewView 100 system on an area of 5x5 mm. The radius of curvature was measure in a direction parallel (R_x) and perpendicular (R_y) to the axis of the stripes.

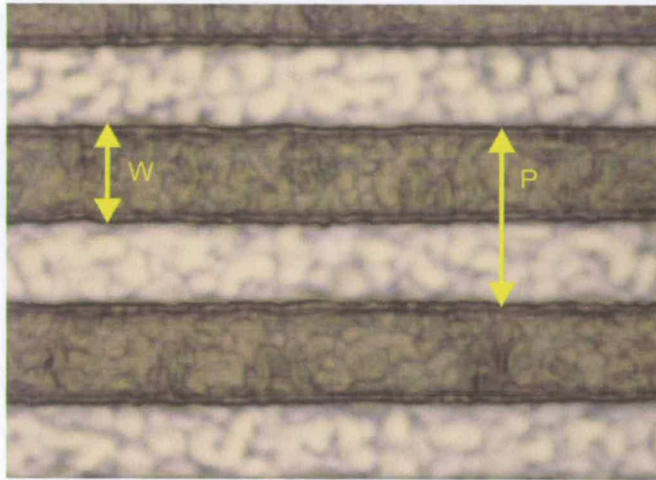
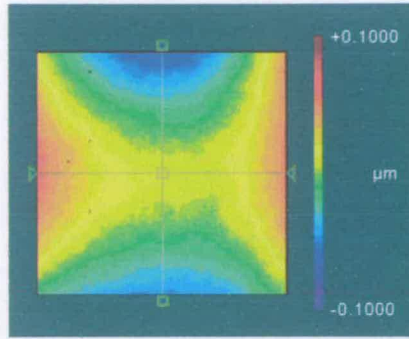


Figure 4.25: Micrograph of one of the stripe pattern employed to evaluate the effect of etching the film on the backside of silicon wafers.

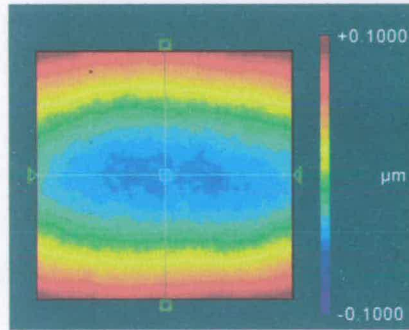
Pattern	Stripe pitch (μm)	Oxide width (μm)
A	30	10
B	30	15
C	30	20

Table 4.8: Dimensions of the three stripe patterns fabricated on the back of silicon wafers.

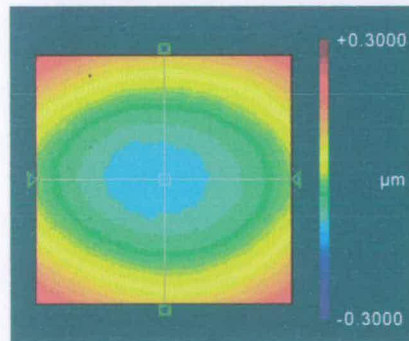
As illustrated in figures 4.26 and 4.27, etching stripes into the oxide film on the backside of silicon substrates greatly affects the symmetry of their curvature.



(a)

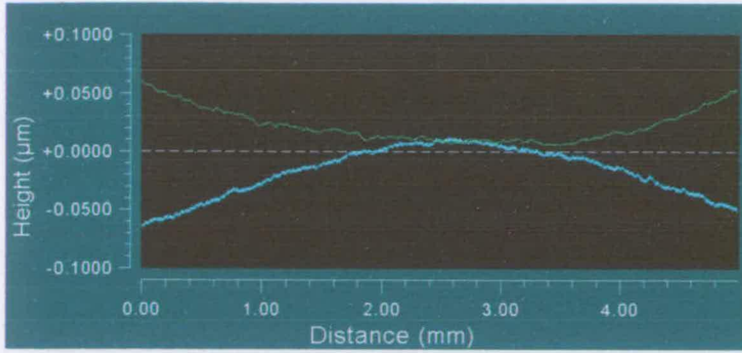


(b)

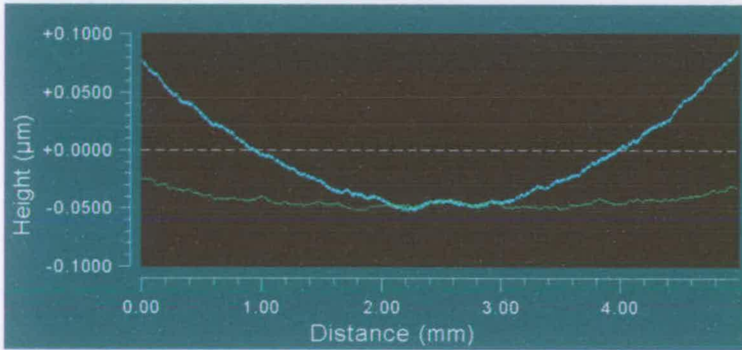


(c)

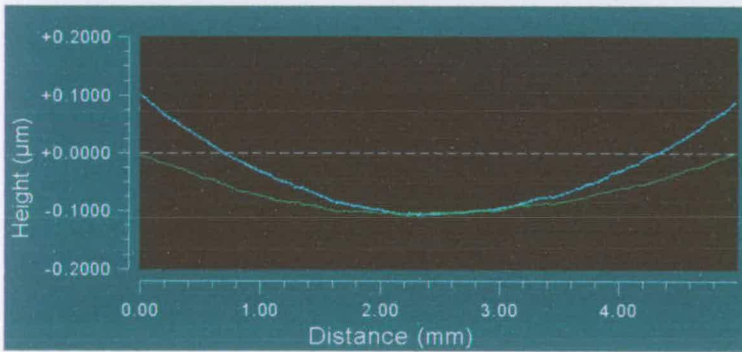
Figure 4.26: Altitude maps of silicon dies with stripe patterns A (a), B (b) and C (c) etched in a 2μm thick oxide layer. The plots are oriented so that the stripe axis is horizontal.



(a)



(b)



(c)

Figure 4.27: Curvature profiles of silicon dies with stripe patterns A (a), B (b) and C (c) etched in a 2µm thick oxide layer. The green and blue plots correspond to the direction parallel and perpendicular to the stripe axis respectively.

The results of the curvature measurements are in agreement with experimental work and numerical analysis by Shen et al. [120]. Silicon substrates with stripe patterns exhibit lower curvature than substrates with blanket films of the same thickness. This results from the absence of material in the etched region. The change in curvature brought by the stripe patterns is more pronounced in the direction parallel to the stripes (i.e. $\Delta K_x/\Delta K_y < 1$).

The change in curvature induced in the direction parallel to the stripes was found to be proportional to the film thickness in the range investigated (see figure 4.28). As shown in figures 4.29 and 4.30, the bow symmetry is not only dictated by the stripe pattern but is also dependant on the thickness of the film. As reported by Shen et al. the bow symmetry decreases rapidly as the ratio t/w increases.

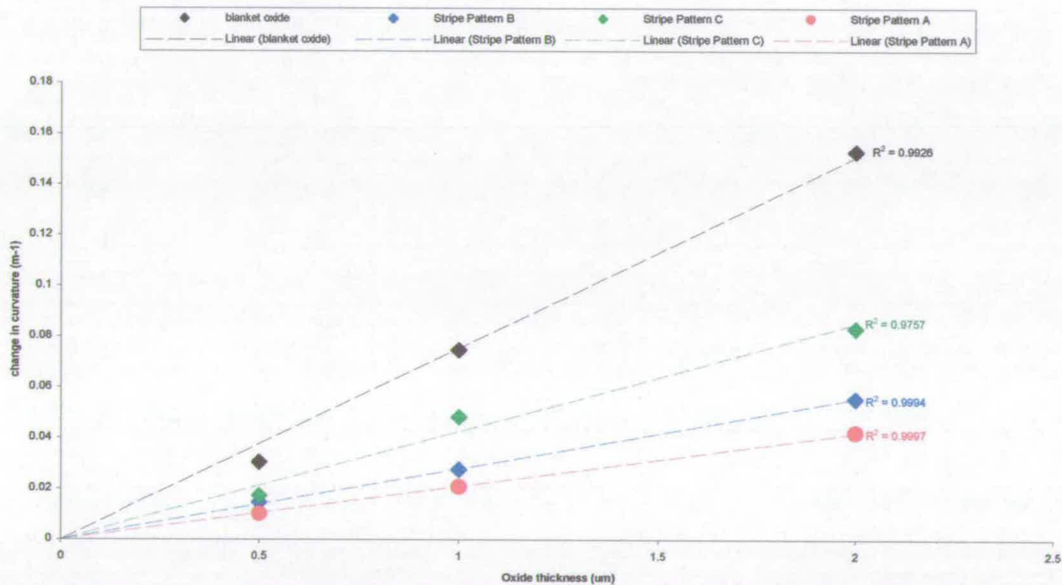


Figure 4.28: Graph showing the change in curvature induced by the stripe pattern in the direction parallel to the stripe patterns.

Experimental work using stripe patterns suggests that it is possible to control the symmetry of the change in curvature brought by the FSC flattening method. It will require careful selection of the film thickness and dimensions of the stripe pattern.

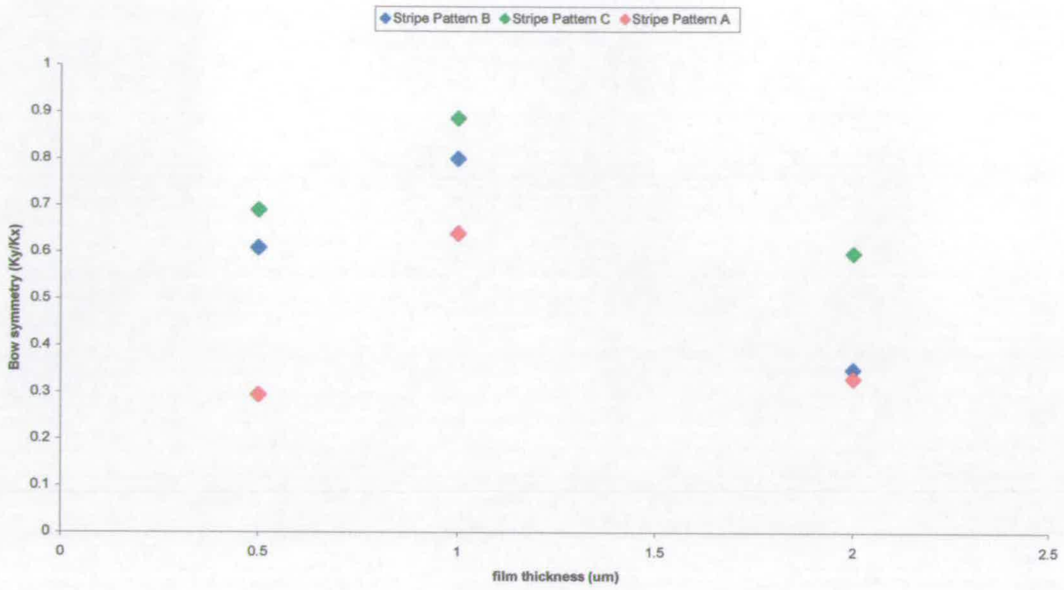


Figure 4.29: Graph showing the curvature symmetry against film thickness for the various stripe patterns.

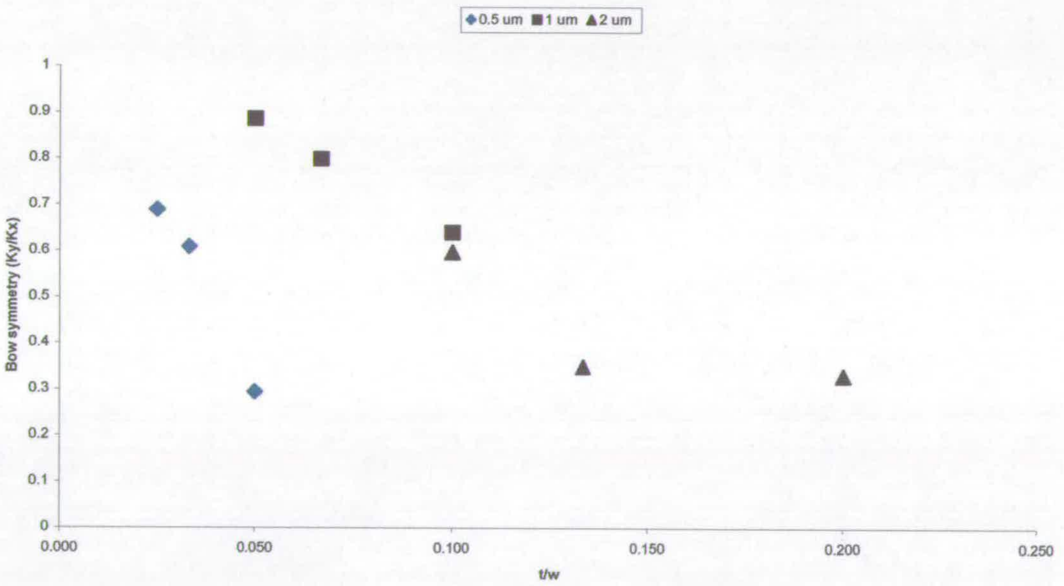


Figure 4.30: Graph showing the curvature symmetry against the film thickness to stripe width ratio.

4.5 Summary

Developments in post-processing of silicon backplanes have led to the fabrication of high optical quality chip for LCoS applications. Both advances in CMP and a better appreciation of the impact of the metallization steps onto the optical properties of the devices have been combined successfully.

A new methodology was also proposed to integrate the fabrication of integrated spacer structures into the post-processing sequence. While such spacer structures were designed for die-scale assembly, there is no reason for that approach not to be used to fabricate wafer-scale compatible spacers

The additional backplane bow brought by the deposition of planarisation oxide has been identified. The effect inspired non-contact flattening technique which sees thin films deposited on the backside of the silicon backplane to compensate for the existing bow. Patterning of the same films offers a unique opportunity to control the symmetry of the induced change in curvature. This elegant method is therefore applicable to a wide range of backplanes designs. Its implementation on real devices (with the help of scanning white light interferometry) is anticipated to be rapid and relatively inexpensive.

Chapter 5. Alignment of SSFLCs

5.1 Introduction

This chapter presents work on alignment of SSFLCs in view of implementation in FLCoS microdisplays. The alignment method most commonly employed in the LCD industry, based on the use of rubbed polyimide films is investigated. The effect of substrate topography on the cosmetic aspects of the alignment will be discussed. The results from the measurement of the electro-optical properties of SSFLC systems produced by the rubbed polymer method will be presented.

The suitability of non-contact photo-alignment methods for aligning SSFLCs has also been explored and the findings presented below. The electro-optical properties of SSFLC systems fabricated using a new generation of photo-polymer films are compared to that brought by rubbing.

5.2 Experimental

5.2.1 Substrates, test cells and FLC

Both silicon backplanes and ITO coated glass dies were employed for fabricating test cells in order to study the alignment of SSFLCs and their electro-optical properties.

For glass substrates, square dies (12x12 mm in size) were sawn from larger sheets supplied by the manufacturer (Delta Technologies).

In order to study the effect of backplane topography on the alignment of FLCs, an attempt was made to fabricate switchable "dummy backplanes" by following the procedure illustrated in figure 5.1.

Unfortunately, inefficient cleaning following via-polishing (step 6 in figure 5.1) resulted in open circuit between the via filling aluminium layer and the pixel layer. As a result, the measurement of the electro-optical performance of the SSFLC systems studied in this work had to be carried out in transmissive cells made by assembling two glass substrates. The reflective cells were used to study the effect of surface topography on the cosmetic aspects of the alignment of SSFLC systems.

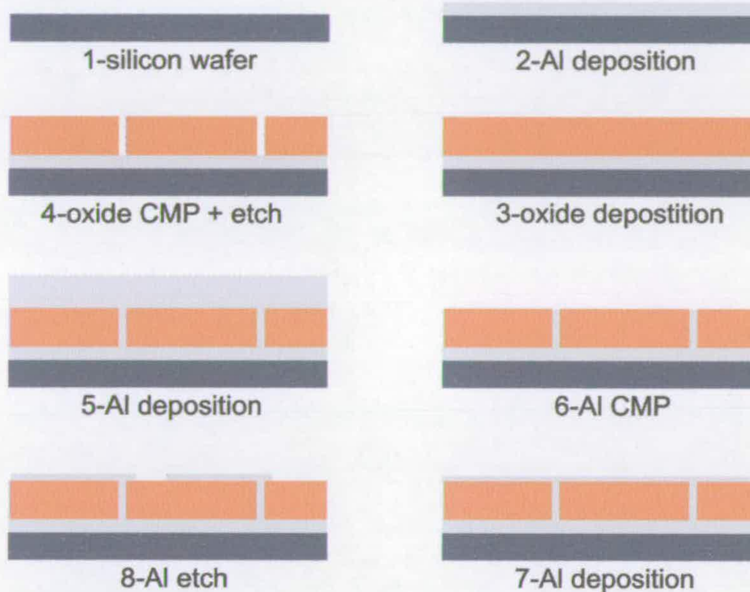


Figure 5.1: Schematic illustration of the process sequence used to fabricate dummy switchable backplanes.

5.2.2 Substrate cleaning

Silicon backplanes fabricated in house were spin-coated with thick photoresist material in order to protect the surface from contamination during the sawing process carried out to singulate the wafers into individual dies. The photoresist material was then removed by immersion in acetone with ultrasonic agitation. In order to prevent the formation of drying marks, silicon dies were rinsed with Isopropyl Alcohol (IPA) immediately upon their removal from the acetone bath. The IPA was subsequently dried using a nitrogen gun prior to cell assembly

In a similar fashion to silicon wafers ITO coated glass sheets were covered with spray-on resist prior to be sawing and the protective layer removed in the same manner as described above.

Further cleaning was carried out as follows. First the glass dies were cleaned in a solution of Neutracon cleaning agent dissolved in distilled water. Glass dies were held with the ITO coated side up (to prevent mechanical damage to the conductive surface) for 30 mins in the solution held at around 50°C under ultrasonic agitation. Efficient rinsing was achieved by removing individual glass dies from the detergent solution and immediately rinsing under a jet of distilled water followed by another ultrasonic bath at 50°C in pure distilled water under ultrasonic agitation. Upon removal from that bath, glass dies were dried using a nitrogen gun and stored in IPA. As for silicon dies, glass dies were held immersed in the IPA solution until cell assembly when they were dried using a nitrogen gun.

5.2.3 Cell assembly

0.81 μm spacer particles (Bang) were employed to control the cell gap of test cells constructed in this work. All cells were assembled with parallel pretilt conditions. Reflective cells were assembled using the procedure illustrated in figure 5.2. Spacer particles were mixed in UV curable adhesive NOA68 from Norland (see Appendix B). The mixture was then dispensed on the corner of the glass die prior to bringing it in contact with the silicon chip. The adhesive material was selected for its viscosity which prevents its rapid flow within the empty cell due to capillary forces. Small pressure was subsequently applied to the corners of the glass die in order to achieve a uniform cell gap. Upon obtaining a satisfactory cell gap, the edges of the cells were exposed to UV light for a short period in order to "freeze" the substrates into position. UV adhesive NOA81 was applied to the edge of the cells. The material with its lower viscosity was allowed to flow within the cell over a short distance to create a suitable seal. A short exposure to UV light for a few seconds after dispense was employed to stop the progression of the adhesive into the cells. Finally, the whole cell was exposed to UV light[5] for 20 mins in order to cure the glue so that it retains

[5] The intensity of the UV light employed to assemble the cells was measured to be around 20 mW/cm^2 at 365 nm.

its mechanical strength during the thermal cycling necessary for filling the cell and does not react when in contact with the liquid crystal.

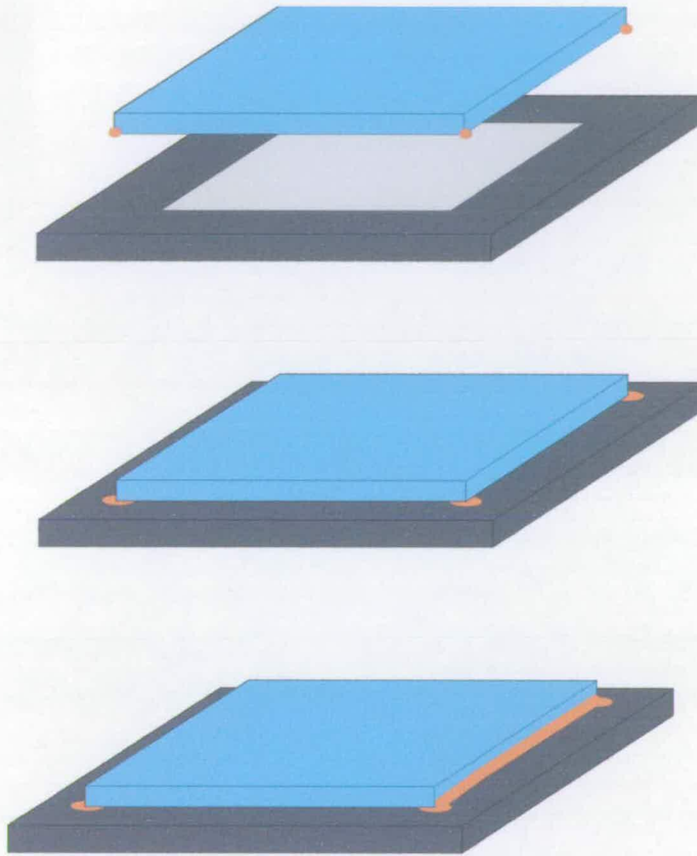


Figure 5.2: Schematic illustration of the method employed for assembling reflective cells with spacers mixed in the glue.

As illustrated in figure 5.3, in the case of the assembly of transmissive cells, the substrates were offset in the x direction to allow bonding and in the y direction for filling and electrical connection. Again, spacers mixed in adhesive were used to control the cell gap. Using clamps, the two substrates were held together, while UV adhesive NOA81 was dispensed at the edge of the cells to form a seal in a similar fashion to that carried out on reflective cells. Again the cells were exposed to UV light for 20 mins.

In order to investigate the effect of spacer particles on the alignment of SSFLCs, some cells were fabricated by spin coating a solution of spacer particles in methanol onto one of the two glass substrates immediately prior to bringing them together. In that case, no adhesive was dispensed at the corners and only adhesive material NOA 81 was used to seal the edges.

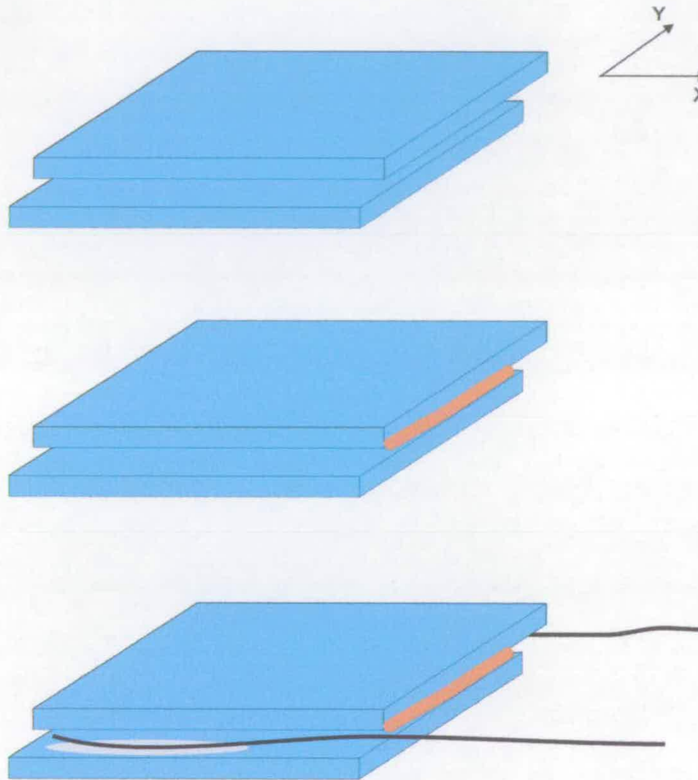


Figure 5.3: Schematic illustration of the methods employed for assembling transmissive cells after spin coating of the spacer in methanol solution.

Achieving a uniform cell gap proved to be very difficult. More often than not, particles larger than the desired cell gap were trapped between the substrates causing unacceptable level of cell gap variation. Whilst building test cells, their cell gap uniformity could be assessed by observing the fringes resulting from destructive interference. It was observed that the achievable cell gap uniformity was significantly increased by carrying out the assembly of the cells on Monday mornings whilst the number of occupants of the cleanroom remained low.

5.2.4 Liquid crystal filling and electrical connection

Liquid crystal filling was carried out by placing the empty cells onto a hotplate held at 110°C. After a delay period of a few minutes to ensure that the cells temperature approaches that of the hotplate, liquid crystal material was brought in contact with the substrates and allowed to fill the cell by capillary action. The hotplate was subsequently set to cool to 30 degC at the rate of around 0.5 degC/min.

The liquid crystal materials used in this work are FELIX 015-100 and FELIX 017-000 from Clariant and CS1031 from Chisso Corporation. Their properties are detailed in Appendix A. Following filling of the cells, the excess liquid crystal material present on exposed areas of the substrates was cleaned with the help of acetone dampened swab. A wire was then attached to the ITO coated surface using a silver filled adhesive (see figure 5.3).

5.2.5 Electro-optical properties appraisal

5.2.5.1 Apparatus

Measurement of the electro-optical properties of the test cells were carried out using the setup illustrated in figure 5.4. The optical setup was based on the used of an Olympus BH-2 polarizing microscope. The sample cells were placed onto a heating stage (LINKAM LTS350) linked to a temperature controller (LINKAM TMS94). A waveform generator (WAVETEK model 75) was used to supply to driving voltage to the test cells. A fast response photodiode (FLCE PIN20) was connected to the camera port of the microscope to measure the intensity of the light passing through the cell with the microscope setup in crossed polarizers configuration. The response time of the photodiode was set to 200 ns using the sensitivity adjustment resistance (see Appendix E). A digitizing oscilloscope (HP 51510A) was employed to record both the electrical response from the photodiode and the cell driving signal. Communication between the computer, the waveform generator and the oscilloscope was achieved via a GPIB interface.

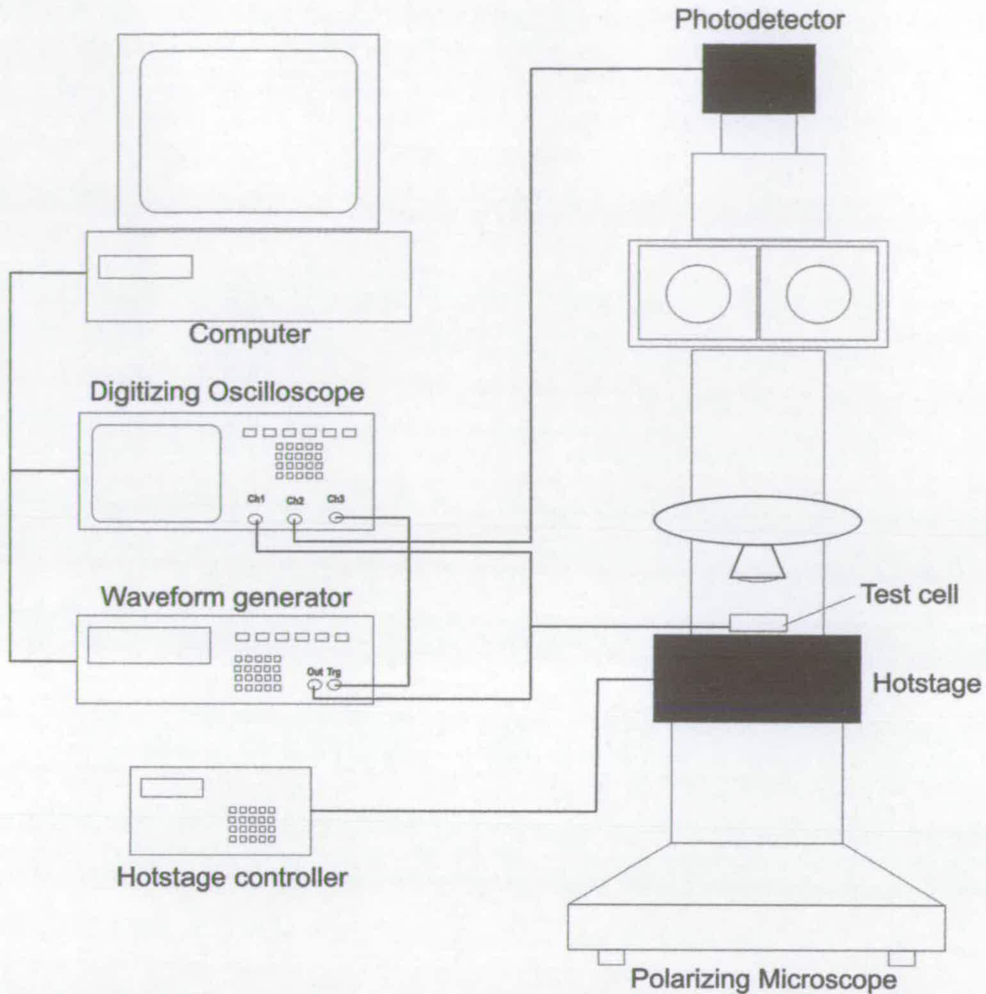


Figure 5.4: Schematic illustration of the setup employed to measure the electro-optical properties of transmissive test cells.

5.2.5.2 Electro-optical properties measurement

As mentioned previously in chapter 2, the efficiency of the binary amplitude modulation achievable with a given SSFLC system is dependent on the thickness of the liquid crystal layer and the angle between the two driven orientation states, also known as Dynamic Switching Angle (DSA). From an application perspective these two parameters will greatly affect the contrast and brightness of the display based on that SSFLC system. Switching times between the driven states will affect the achievable frame rate and numbers of grey levels or colours achievable with that display.

While used in the past to assess the electro-optical performance of SSFLC test cells [65] the measurement of the contrast ratio was judged to be irrelevant to this work

for two main reasons. The cell gap target of 0.8 μm for the transmissive test cells was selected to imitate that of reflective devices. Optically it corresponds to a quarter waveplate situation so that the constrast achieved is not representative of that of a reflective microdisplay device. Also the contrast ratio is very dependent on the cell gap. As a result, comparison of two cells or devices in terms of their contrast ratio is therefore only valid if their cell gap is identical. The SSFLC systems fabricated in this work were characterized in terms of their dynamic switching angle rather than contrast.

Figure 5.5 shows the effect of cell orientation on the light intensity level measured for the two switched states of a SSFLC cells subjected to bipolar pulses. The dynamic switching angle can be simply measured by measuring the cell rotation angle required to achieve extinction for the two polarities of the driving voltage. This method however is rather inaccurate due to the low change in light intensity around the extinction point and the dark voltage value of the photodiode. A more precise method was employed to measure the dynamic switching angle of the SSFLC systems in this work. Rather than using the extinction position, the cell was rotated to achieve a light level at mid-point between the maximum and minimum intensity resulting from bipolar switching. In this region, the relationship between transmitted light intensity and the cell orientation angle is steeper and therefore allows to position the cell more accurately with the reference mid-point for both polarity which results in more accurate switching angle measurement.

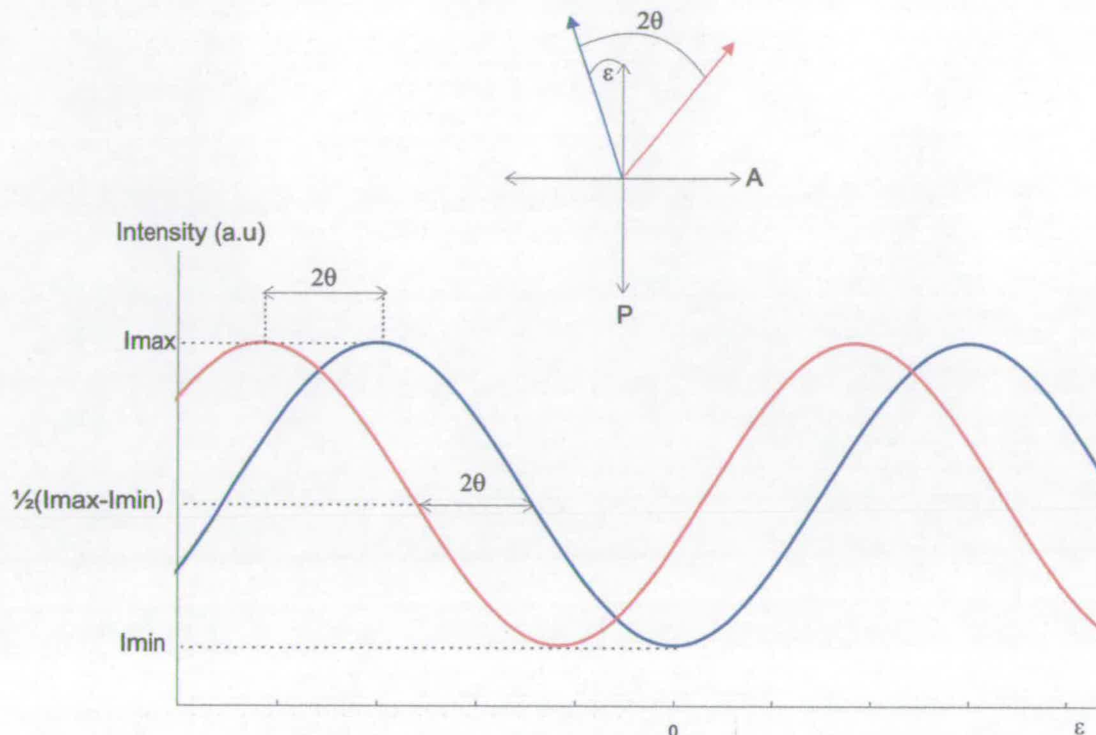


Figure 5.5: Schematic illustration of the relationship between cell orientation and the electro-optical response to a bipolar driving waveform.

The switching time was calculated as the average between the rise and fall time of the photodiode output signal with the cell driven by a 500Hz square waveform. The rise and fall times were measured using the oscilloscope's in-built function with the data averaged over 128 periods. As shown in figure 5.6, the rise and fall times corresponds to the time for the signal to change from 10% to 90% of the total signal step. The cell orientation for switching time measurement was set by rotating the cell 22.5° from the orientation leading to equal transmission for both polarities. The results from the switching time measurements carried out in this work will be presented in sections 5.3.4 and 5.4.2.

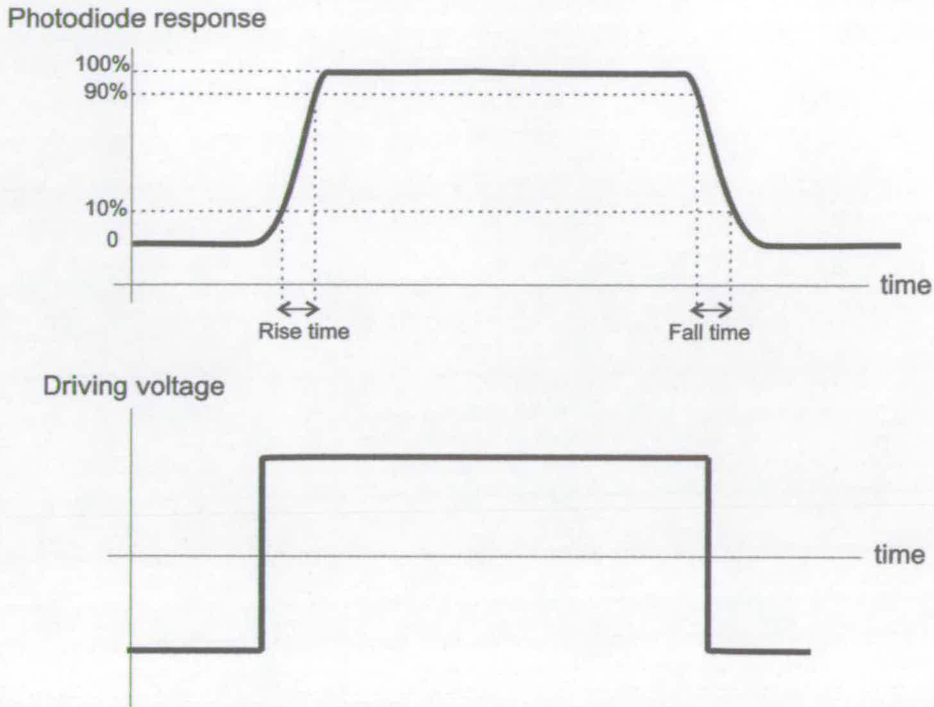


Figure 5.6: Schematic illustration of the switching time measurement.

5.3 Alignment of SSFLCs on rubbed polymers

Test cells were fabricated to evaluate the quality of the alignment of FLCs between rubbed polyimide alignment layers (see figure 2.5). This section presents the experimental details for the fabrication of such devices. Emphasis is brought on the topography of the rubbed polymer surfaces. Results from the electro-optical measurements described earlier are also presented.

5.3.1 Preparation of rubbed polyimide film

Polyimide material SE610 (Nissan Chemicals) was deposited onto the silicon and glass substrates by spin coating. The original polyimide solution was diluted in N-Methyl-Pyrrolidone and dispensed onto the substrates placed on the vacuum chuck of a Laurell WS-400B spin coater system. The solution was manually dispensed through a 0.2μm PTFE filter in order to cover the whole area of the substrate. Immediately after dispense the substrates were accelerated to 3000 rpm at 500 rpm/s and held at that rotating speed for 90 s. Various film thicknesses were obtained by varying the solution concentration (see figure 5.7).

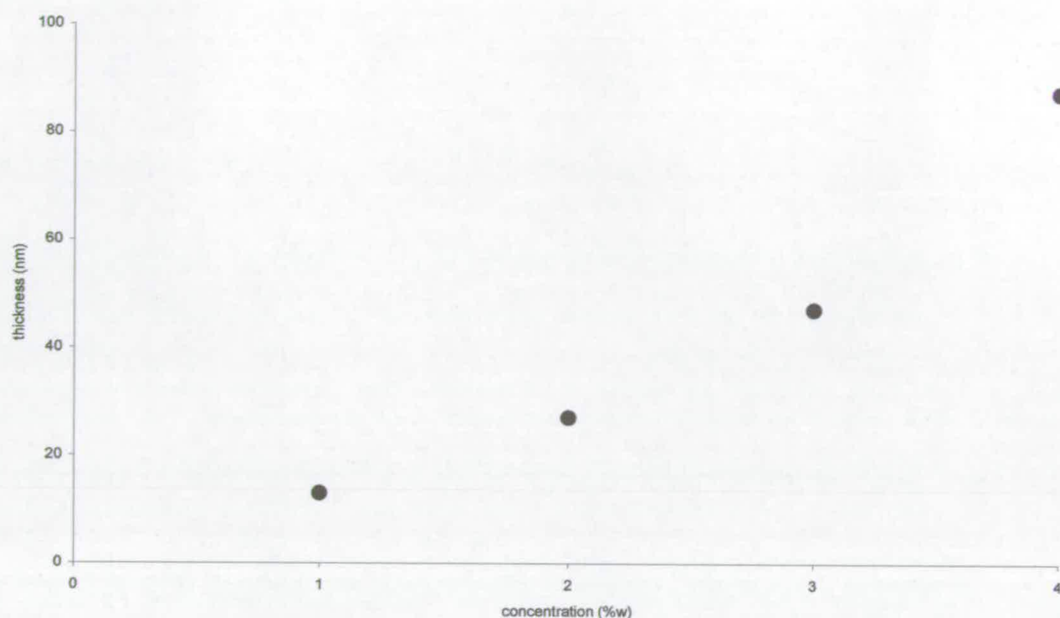


Figure 5.7: Graph showing the relationship between the polyimide solution concentration and the resulting film thickness produced by spin coating at 3000 rpm.

Immediately after spin coating the substrates were placed onto a hotplate pre-heated at 100°C and held at that temperature for a minimum of 30 mins. The temperature of the hotplate was then raises to 250°C at 5°C/min and held at that temperature for one hour.

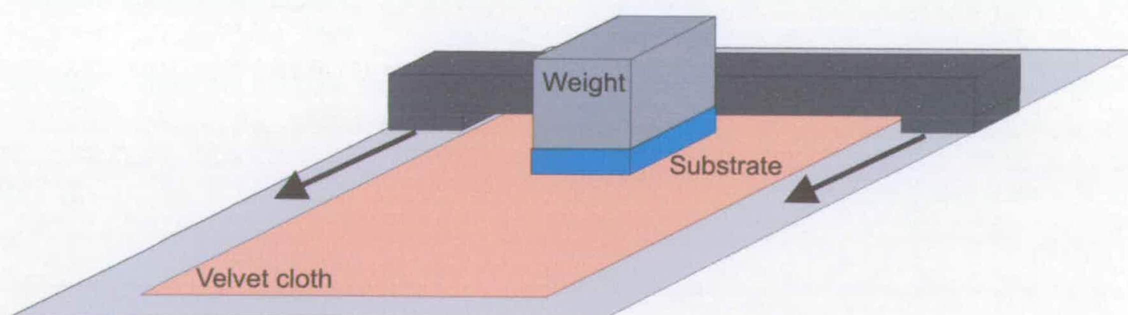


Figure 5.8: Schematic illustration of the setup employed for rubbing polyimide films.

Rubbing was achieved by moving the substrate, face down, in a straight line onto a velvet cloth. The speed of motion was controlled by the use of an old X-Y plotter.

The pressure applied to the substrate was controlled simply by the use of custom made metal weights matching the dimensions of the substrate.. The process was repeated in order to achieve rubbing distances larger than the velvet cloth.
Failing to source specialised rubbing cloth material, velvet pad designed for polishing purposes was employed. Following a series of simple trials using a range of cloth materials "Vel-cloth" pads (Allied High Tech) were selected as rubbing cloth for this work.

5.3.2 The rubbing process

Unlike roller based rubbing machines, the setup employed in this work permits to apply a very little amount of rubbing pressure to the polyimide layer. As a result, some insight could be gained onto the dynamics of the rubbing process.
Figure 5.9 shows the alignment of FLC material 015-100 obtained between lightly rubbed polyimide films. As can be seen the alignment of the FLC is not uniform across the whole substrate area but rather takes place in elongated streaks parallel to the rubbing axis. The surface area of orientated material for a given rubbing distance increases with increasing rubbing pressure and decreasing rubbing speed. For given speed and pressure conditions, rubbing the substrate over a longer distance results in the bands of aligned material to increase in size and coalesce. These observations are in agreement with results from work by Paek et al. [121] and Geary et al. [122].

Two main mechanisms have been accepted by liquid crystal technology scientists to explain the alignment of liquid crystal molecules above rubbed polymer surfaces. Berreman [123,124] suggests that LC alignment relies on grooves created by rubbing on with the liquid crystal molecules lying with their long axis parallel to the groove axis. Geary et al. [122] argue that such reasoning does not explain why certain polymers do not promote alignment of liquid crystals when rubbed. Interestingly they also comment that it is unlikely for alignment brought by weak rubbing to be due to the presence of grooves. Another concept suggested by Castellano [125] relies on the orientation of the polymer chains by the rubbing process which in turn leads to the alignment of the adjacent liquid crystal molecules by an epitaxial like process.

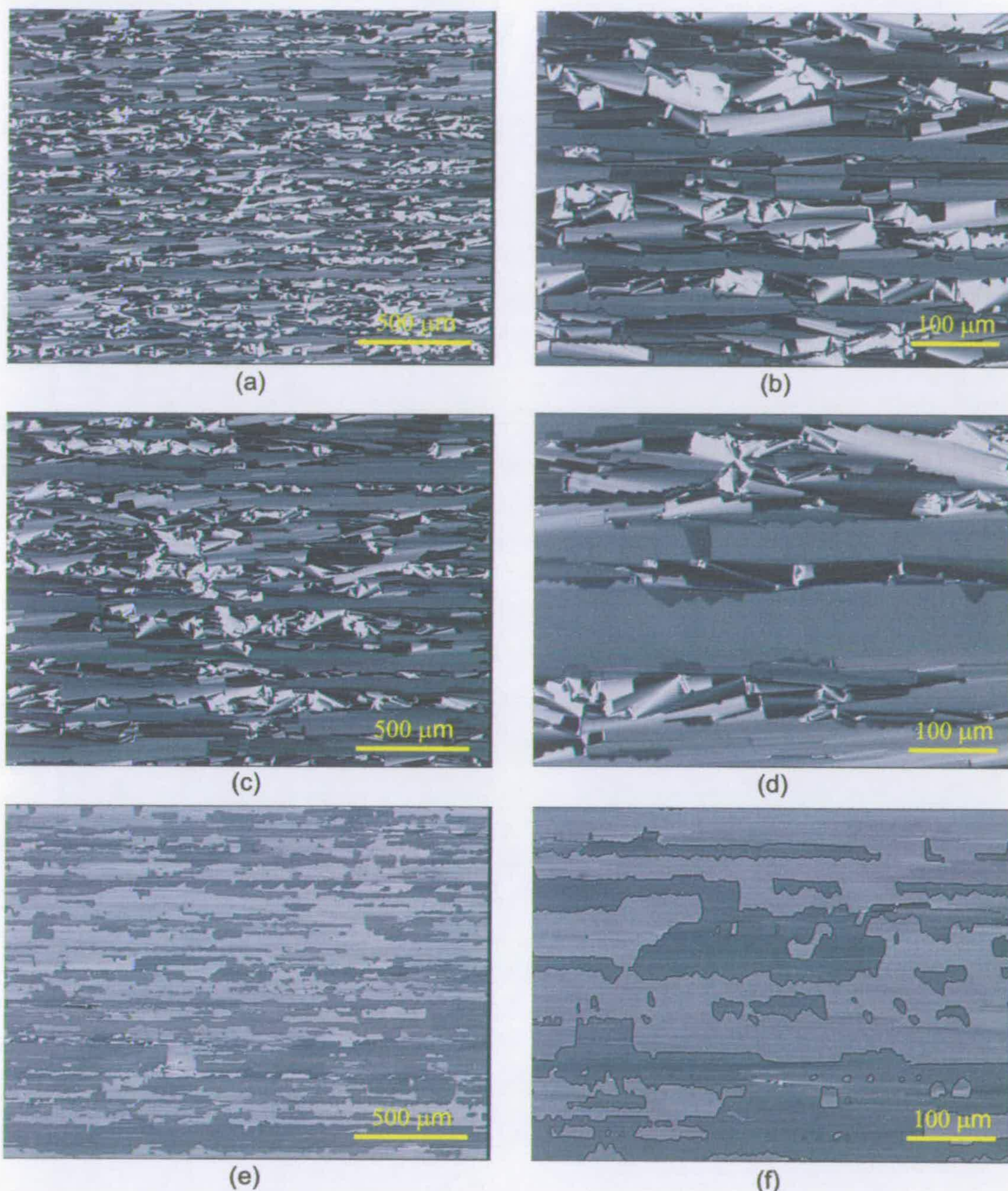


Figure 5.9: Micrographs of the alignment of FLC 015-100 on rubbed polyimide for the following rubbing conditions: (a,b) speed = 1cm/s, distance = 15cm, pressure = 0.5 g/cm2 (c,d) speed = 0.2 cm/s, distance = 15cm, pressure = 0.5 g/cm2 (e,f) speed = 1cm/s, distance = 15cm, pressure = 5 g/cm2. Rubbing direction for all micrographs is horizontal from left to right.

A study of the topography of alignment layers was conducted by AFM. As shown in figure 5.10, the polyimide layer around 50 nm thick provides a significant degree of

planarisation reducing the intrinsic roughness of the substrates resulting from the polycrystalline nature of the ITO films.

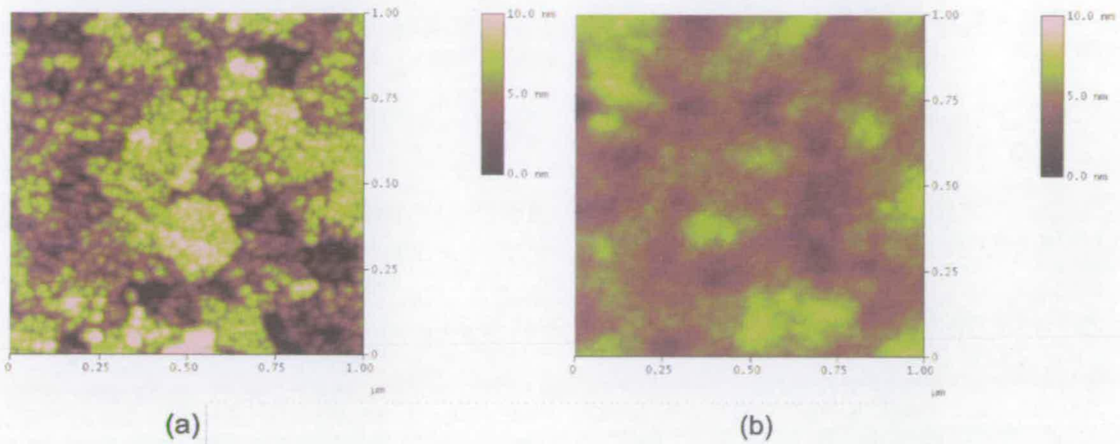
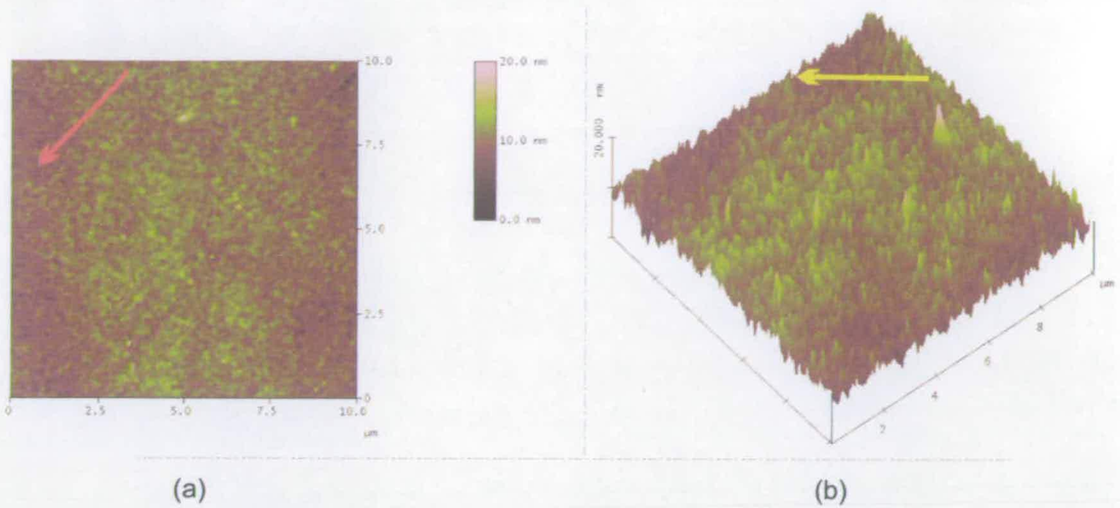


Figure 5.10: AFM images of ITO coated glass surface before (a) and after coating (b) with a 50 nm thick polyimide layer.

As can be seen in figures 5.11 and 5.12, the topography of rubbed polyimide films prepared using the setup described in section 5.3.1 were found to differ greatly from that obtained using roller machines [108]. It is thought that the weaker rubbing conditions do not promote the formation of grooves across the whole surface area of the substrate and that the streaks of alignment liquid crystal observed in "partially" rubbed cells corresponds to areas where the polymer chain have aligned parallel to the rubbing direction.



(a) (b)

Figure 5.11: AFM images (A) and oblique plot (B) of glass surface coated with a 50 nm thick SE610 polymide layer subjected to weak rubbing with the following conditions: speed = 1 cm/s, pressure = 2 g/cm2, speed = 1 cm/s.

It is well accepted that the orientation of the polyimide chains parallel to the rubbing axis results from the local heating due to friction between the polymer surface and the fibres of the rubbing cloth under linear motion. It remains however unclear if local melting of the polymer takes place as favoured by Mada et al. [126] or if a softening of the material with local temperature approaching that of its glass transition temperature is responsible for the alignment of the polymer chains as suggested by Pidduck et al. [127].

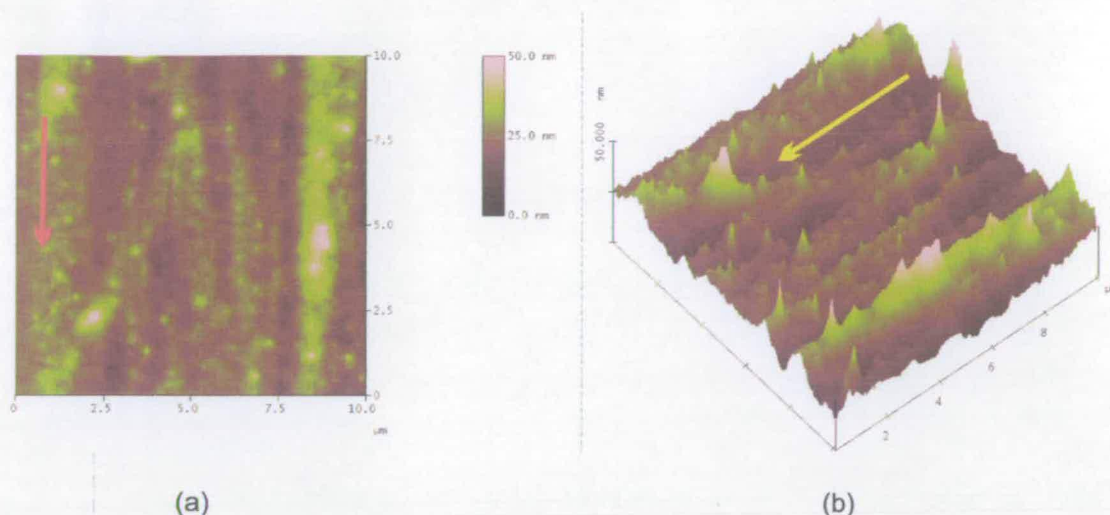


Figure 5.12: AFM images (A) and oblique plot (B) of glass surface coated with a 100 nm thick polyimide layer subjected to strong rubbing using a roller based rubbing machine **[Error! Bookmark not defined.]**.

5.3.3 Alignment brought by rubbing

The rubbing pressure was found to have on effect on the uniformity of the alignment for FLCs employed in this work. As shown in figure 5.13a, a pressure of 0.5 g/cm^2 did not promote uniform contact between the substrate and the cloth which resulted in linear streaks where it is thought that the liquid crystal molecules exhibit slightly different orientation. A minimum pressure of 2g/cm^2 was found to be necessary to promote uniform orientation of the liquid crystal molecules across the whole area of the substrate. At this pressure, samples were rubbed over a total distance of 100 cm at 1 cm/s. Under such conditions, as shown in figure 5.13b, some backplanes exhibited large scale non-uniformity. The frequency of such defects was low and at most affected 20% of samples. It is thought that contamination of the cloth by particulates or entangling of individual fibres could be at the origin of such defects.

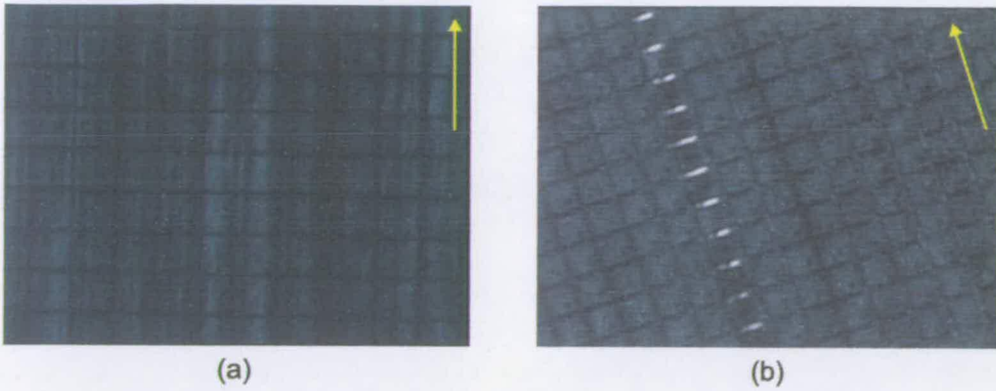


Figure 5.13: Micrographs showing regions of non-uniform rubbing observed on silicon backplanes for a rubbing pressure of 0.5 g/cm2 (a) and 2 g/cm2 (b). The arrows indicate the rubbing direction. The pixel pitch equals 20 μm.

Both FLC materials exihibited a C2 chevron orientation (see figure 2.7) over the rubbed polyimide films. As illustrated in figure 5.14, the orientation of the chevron structure could be identified by the presence an hairpin defect near the edge of the glass substrate. The origins of such features are not clear. The difference in film surface properties due to turbulence associated with the spin coating of square substrates could be responsible.

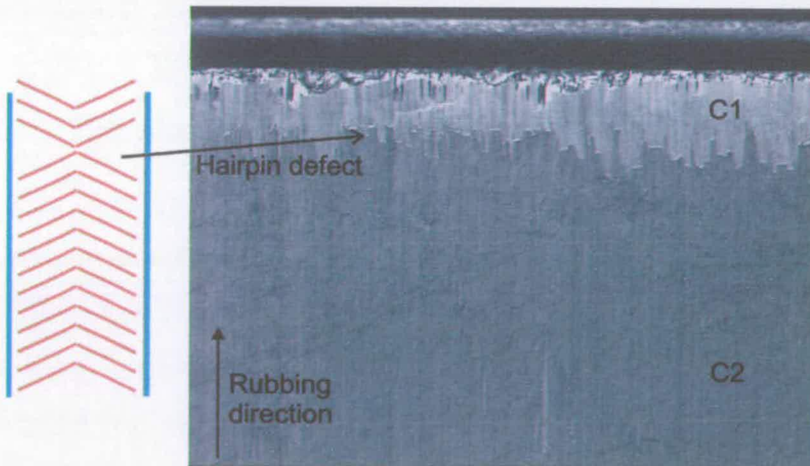


Figure 5.14: Micrograph showing the alignment of FELIX 015-100 with a majority C2 chevron orientation put in evidence by hairpin defect at the edge of the cell.

The low pretilt angle conditions[6] brought by the polyimide employed are compatible with the existence of both C1 and C2 chevron orientations. As it will be discussed later in section 5.4.2, the high anchoring energy conditions induced by rubbing favors the existence of C2 orientation rather than C1.

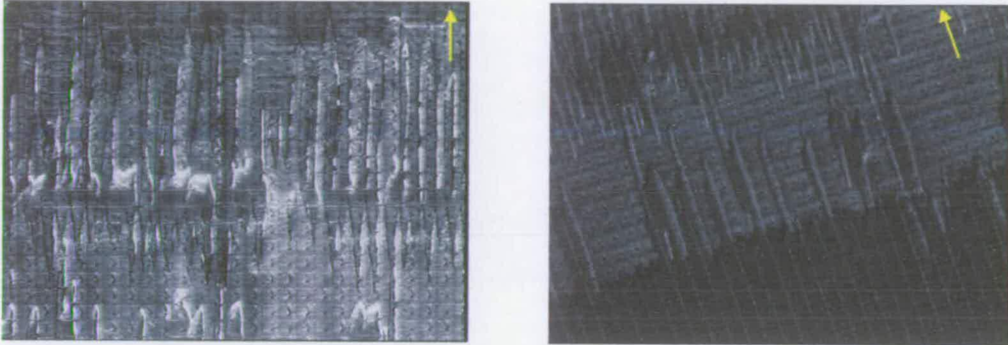


Figure 5.15: Micrographs showing the alignment of FELIX 015-100 obtained by rubbing on backplanes with thick pixel layer. The arrows indicate the rubbing direction. The pixel pitch equals 20 μm.

As illustrated in figure 5.15 and 5.16 backplanes with a thick pixel layer exhibited a significantly higher density of zigzag defects across the active area of the device than backplanes with thin pixel layer. This was found to be true for both FELIX 015-100 and FELIX 017-000 materials.

Silicon backplanes with a thin pixel layer showed very few isolated chevron defects which form islands of C1 chevron orientation in a majority of C2 orientation. Glass test cells were found to show less defects compared to reflective samples.

[6] A pretilt value of 5° at low rubbing strength is specified by the manufacturer.

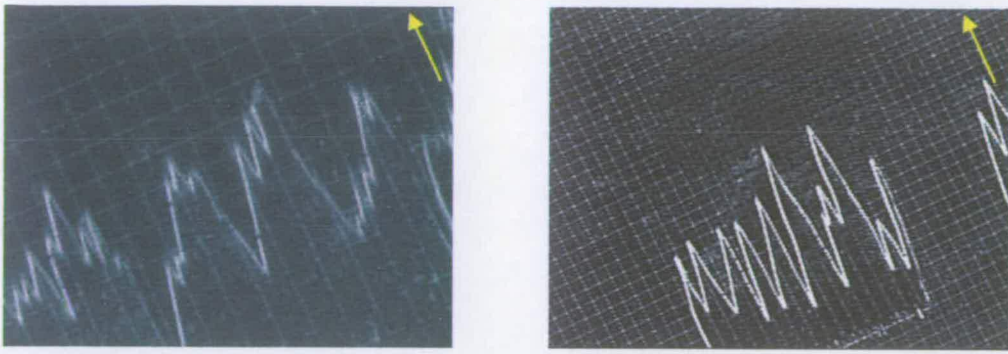


Figure 5.16: Micrographs showing the alignment of FELIX 015-100 obtained by rubbing on backplanes with a thin pixel layer. The arrows indicate the rubbing direction. The pixel pitch equals 20 μm.

These observations are in agreement with that of Watson et al. [128,129] and Furue et al. [130] who have shown that the density of chevron defects increases with the roughness of the substrate and/or alignment film. As shown in section 4.2.2 the thicker pixel layer exhibits a much rougher topography.
As illustrated in figure 5.17, the geometric requirements for the existence of the two chevron structures are as follows:

C1 structure is allowed if $0 < \alpha < \delta+\theta$,

C2 structure is allowed if $0 < \alpha < \theta-\delta$,

with α, δ and θ the pretilt angle, chevron angle and cone angle respectively.

While both chevron orientations are possible at low pretilt conditions, C2 chevron structure cannot exist if $\alpha > \theta-\delta$ and therefore C1 orientation will take place. It is the author's view that the surface of thicker pixels contains numerous sites which will promote higher pretilt conditions and therefore prohibit the existence of C2 orientation. At the boundary lie zigzag defects which are detrimental to display operation because of the light leakage associated. Work by Hatoh et al. [131] revealed that the presence of small projections at the surface can increase the pretilt depending on their shape and its relationship with the rubbing direction.

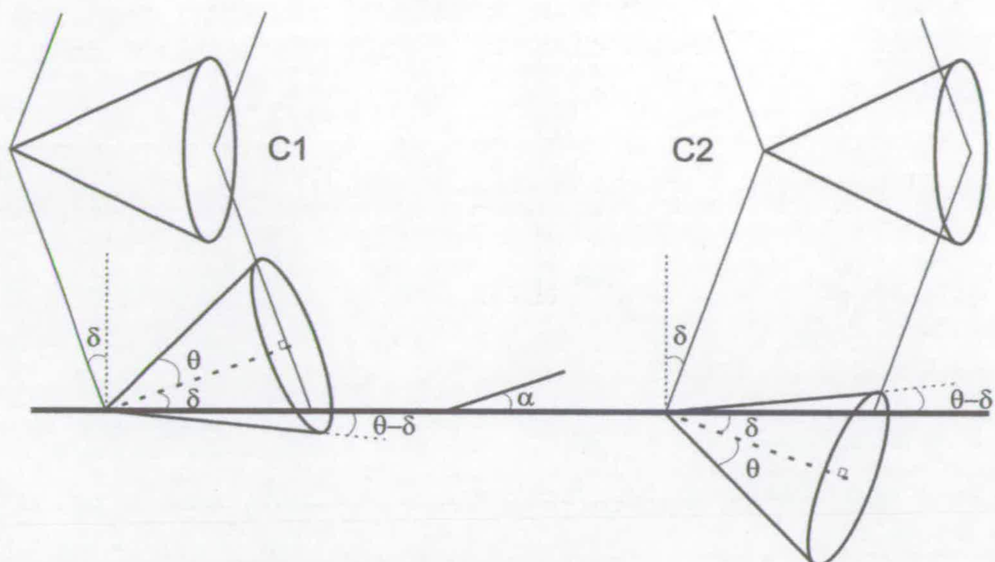


Figure 5.17: Schematic illustration showing the geometric relationship between the chevron angle δ, the pretilt angle α and the cone angle θ.

Surprisingly, the absence of inter-pixel gap on backplanes with embedded pixels (see section 4.2.2.3) was not found to reduce the chevron defect density further. This indicates that the pixel edge does not act as a seed for chevron defects. Furthermore the location of zigzag defects observed on silicon backplanes was never observed to coincide with any pixel scale topographical features. Even over thick pixels, areas of defect-free alignment could be observed over several pixels.

Glass test cells prepared with very thin alignment layers (thickness < 10 nm) obtained by spin coating a 0.5% polyimide solution at 3000 rpm exhibited a high density of chevron defects as illustrated in figure 5.18. It is expected that the reduced planarisation effect of thin alignment layers will result in increased surface roughness. Unfortunately, AFM analysis of the samples with thinner alignment layer to illustrate this phenomenon could not be carried out due to equipment breakdown. The above observations strongly indicate that surface roughness rather than larger topographical features such as pixel step has a strong impact on the formation of chevron defects.

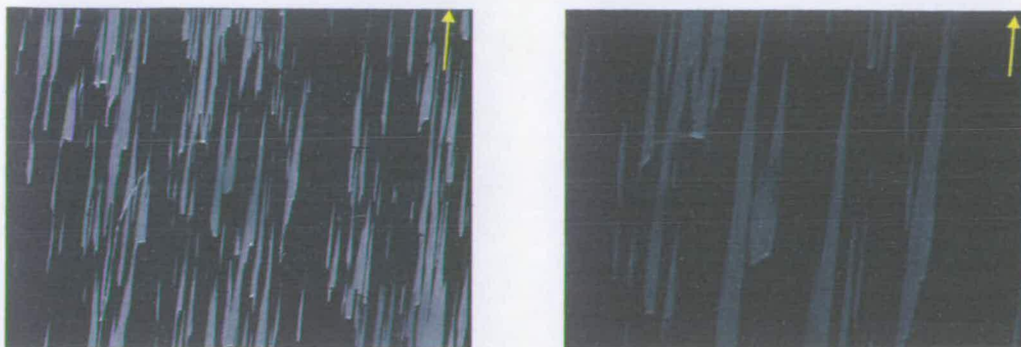


Figure 5.18: Micrographs showing the high chevron defect density obtained with FELIX 015-100 over thin alignment layer (< 10 nm). The arrows indicate the rubbing direction.

As illustrated in figures 5.19 and 5.20 glass test cells containing spherical spacer particles in the active area exhibited so-called needles defects. Cells filled with FELIX 017-000 were found to be more prone to developing such feature than samples made with FELIX 015-100. Unlike spacers related defects described by Kanbe et al. [132], no hairpin defect was found to be associated with such feature. The needles defects observed were very similar in appearance to that observed by Wang and Bos [110] around spacers in SSFLC systems aligned using obliquely evaporated silicon oxide.

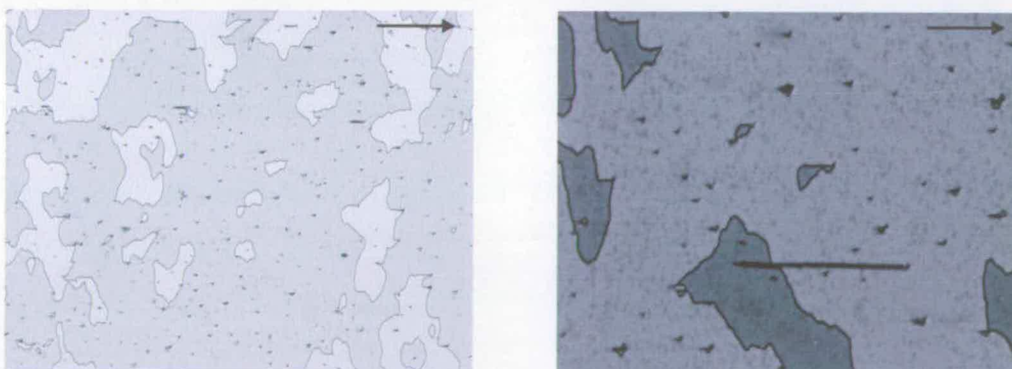


Figure 5.19: Micrographs showing the limited effect of silica spacer spheres on the alignment of FLC FELIX 015-100 on rubbed polyimide. The arrows indicate the rubbing direction.

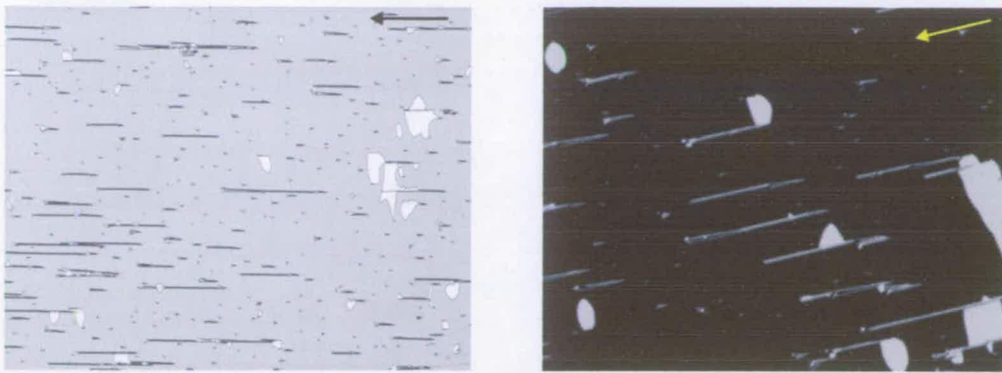


Figure 5.20: Micrographs showing the high density of spacer induced needles defects associated FLC FELIX 017-000 on rubbed polyimide. The arrows indicate the rubbing direction.

It is thought that the spherical silica particles employed as spacer force locally an inversion of the orientation of the chevron. As illustrated in figure 5.21, away from the spacer particle the orientation of the chevron is affected by the surface conditions so that the chevron switches back to its preferred C2 orientation.

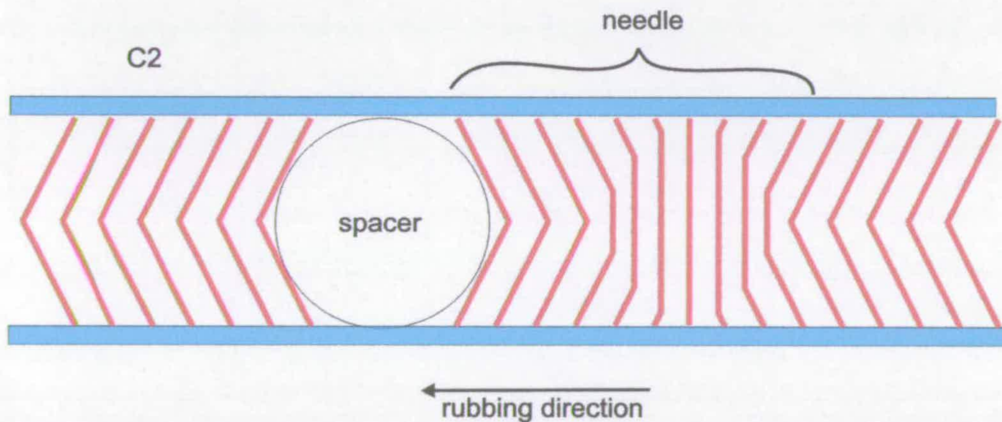


Figure 5.21: Schematic illustration of the layer structure of the needle defect associated with spacer particles.

As illustrated above light leakage in the dark state induced by the existence of defects associated with spacer spheres is unsuitable for microdisplay operations.

Reflective cells were assembled after exposing the backplanes for 10 mins to oxide etch conditions listed in table 4.3. In agreement with the roughness measurement by AFM, no increase in chevron defect density was observed in these samples confirming that the spacer fabrication method presented earlier in this thesis is suitable for the fabrication of FLCoS microdisplays.

5.3.4 Electro-optical properties of SSFLCs aligned by rubbed polyimide

Electro-optical measurements of the properties of the SSFLC systems prepared using rubbed polyimide highlighted the importance of the liquid crystal materials ultimately has on the performance achievable.

The properties exhibited by cells filled with FELIX 015-100 are very promising with a high dynamic switching angle and a low switching time (see figure 5.22). The lower spontaneous polarisation of FELIX 017-000 results in a much slower switching time despite a lower rotational viscosity (see figure 5.23).

Switching time measurements found the rise and fall times to be similar. This was expected due to the fact that glass test cells are made of two identical substrates. The switching time measurements were very close to calculations using equation 2.4.

The manufacturer specifies a similar switching angle of around 51° for both materials under an electric field ± 15V/μm. Under a much more moderate field of the order of ± 3 V/μm such as the one used in this work, FELIX 015-100 showed a significantly higher dynamic switching angle than FELIX 017-000. It is thought that in low electric field regime, the switching angle exhibited by this material was affected by the low value of its low spontaneous polarization.

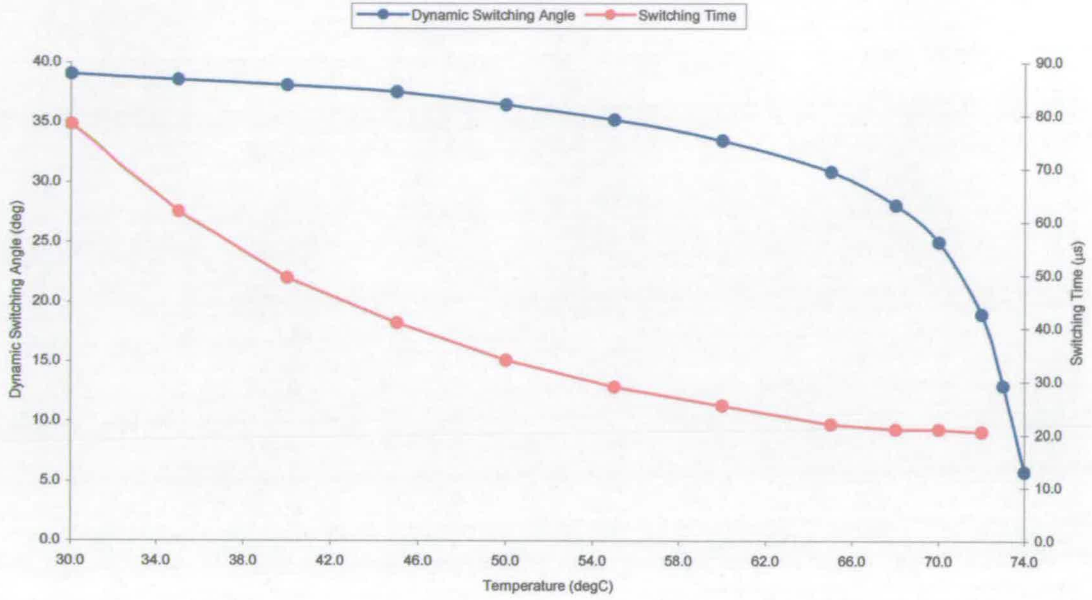


Figure 5.22: Graph showing the effect of temperature on the dynamic switching angle and switching angle of FELIX 015-100 on rubbed polyimide (thickness: 47 nm).

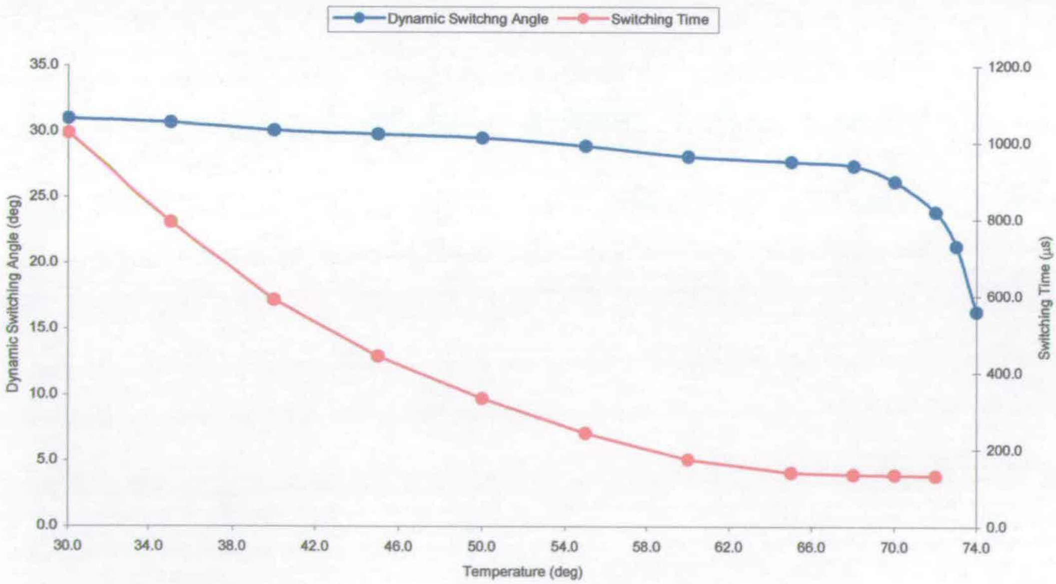


Figure 5.23: Graph showing the effect of temperature on the dynamic switching angle and switching angle of FELIX 017-000 on rubbed polyimide (thickness: 47 nm).

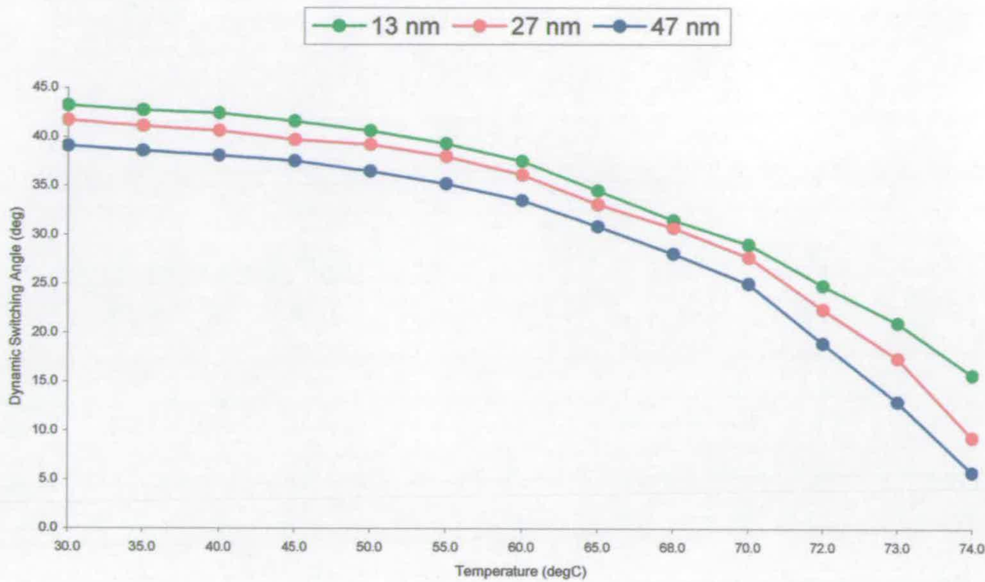


Figure 5.24: Graph showing the effect of temperature on the dynamic switching angle of FELIX 015-100 on rubbed polyimide for various alignment layer thicknesses.

Reducing the thickness of the polyimide alignment layer was found to result in an increase in a dynamic switching angle (see figure 5.24) without affecting significantly the switching time (see figure 5.25). At 30°C reducing the thickness of the alignment layer from 47 nm to 13 nm resulted in a dynamic switching angle increase of 2.3°. This change would translate in a 5% gain in electro-optical efficiency.

Whilst the impact of layer thickness on the bistable memory of SSFLCs is well documented [133,134,135], to the author's best knowledge no published reference describes the effect of layer thickness on the dynamic switching angle. Some insight was however gained during work towards the development of an improved SPICE model to describe FLCoS devices [136,137]. Results from experimental work by Macartney [138] were found to be in agreement with results presented above.

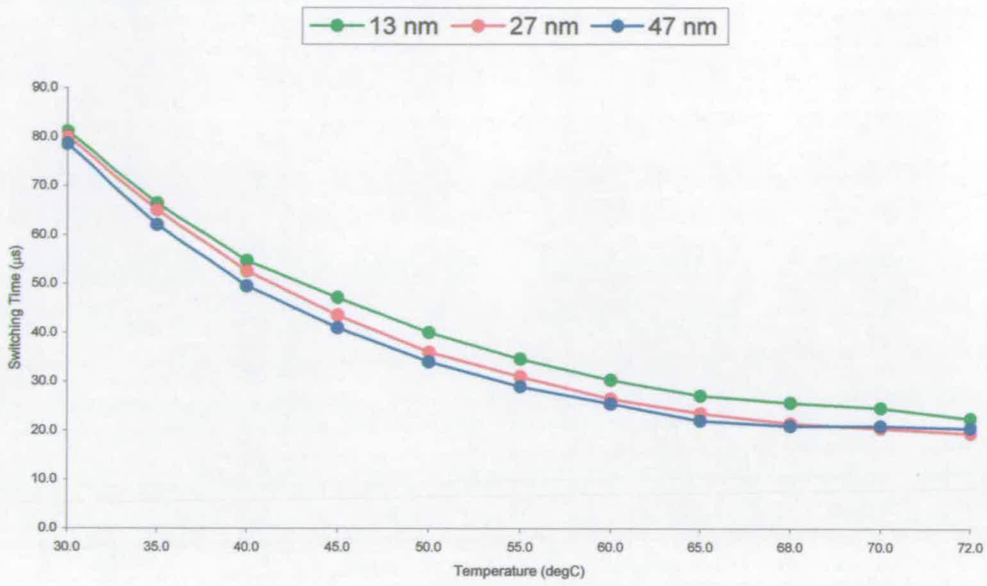


Figure 5.25: Graph showing the effect of temperature on the switching time of FELIX 015-100 on rubbed polyimide for various alignment layer thicknesses.

5.4 Photo-alignment of SSFLCs

5.4.1 Bulk photo-alignment

In the early nineties a number of researchers reported on the possibility of inducing homogeneous alignment of nematic [139,140] and smectic [141,142] liquid crystals without the use of alignment layers. The method known as bulk photo-alignment consists of exposing a mixture of liquid crystal and photopolymer to linearly polarised ultra violet (LPUV) light. The potential benefits of not requiring alignment layers were too attractive to be ignored and experimental work was carried out to investigate the feasibility of this method.

Smectic liquid crystal material CS 1031 from Chisso Corporation (see Appendix A) was mixed with a small amount (0.2% by weight) of poly(vinyl-4-methoxy cinnamate) (PVCi) in a solution of chloroform. The solvent was subsequently allowed to evaporate at room temperature for 48 hours.

Glass cells were filled with the FLC+PVCi mixture at 120°C. Upon complete filling, the cells were exposed to LPUV light. The cell temperature was maintained at 120°C during the whole exposure process. The cells were cooled to room temperature at a rate of 0.5°C/min.

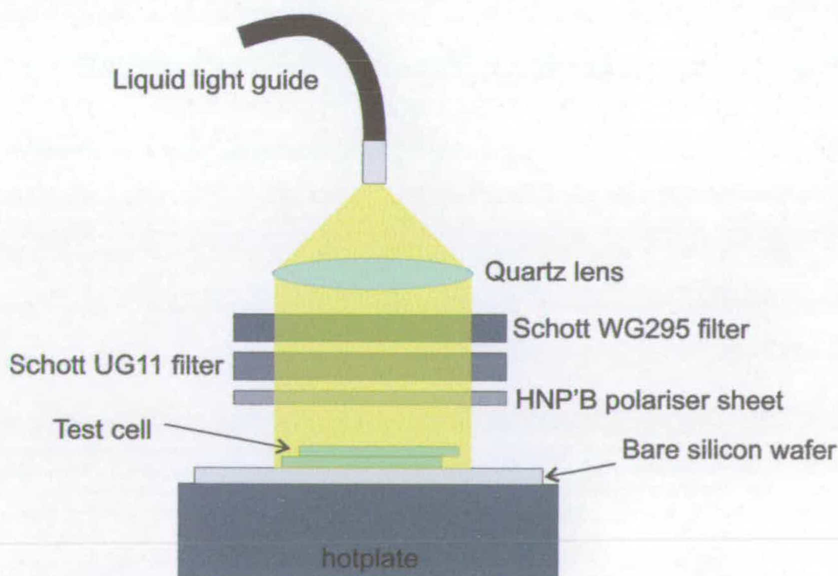


Figure 5.26: Schematic representation of the setup employed for exposing samples to LPUV light.

As illustrated in figure 5.26, the UV light from a 50W Mercury lamp was collected via a liquid light guide and collimated using a quartz lens. A cut-off filter (Schott WG295) and band-pass filter (Schott UG11) were employed to protect the polaroid type UV polariser sheet (HNP'B). The transmission spectra for the filters employed are shown in Appendix C. The intensity of the light striking the cell was measured to be 5 mW/cm^2 at 365nm.

Exposure to LPUV light gave rise to planar alignment of the FLC material. As shown in figure 5.27 the quality of the alignment observed in the central region of the test cells was found to increase with the LPUV energy. This was true up to a value around 18 J/cm^2. Further exposure failed to improve the alignment further and unfortunately it was impossible to obtain a perfect alignment. The texture exhibited a large number of sites non-aligned FLC material remaining.

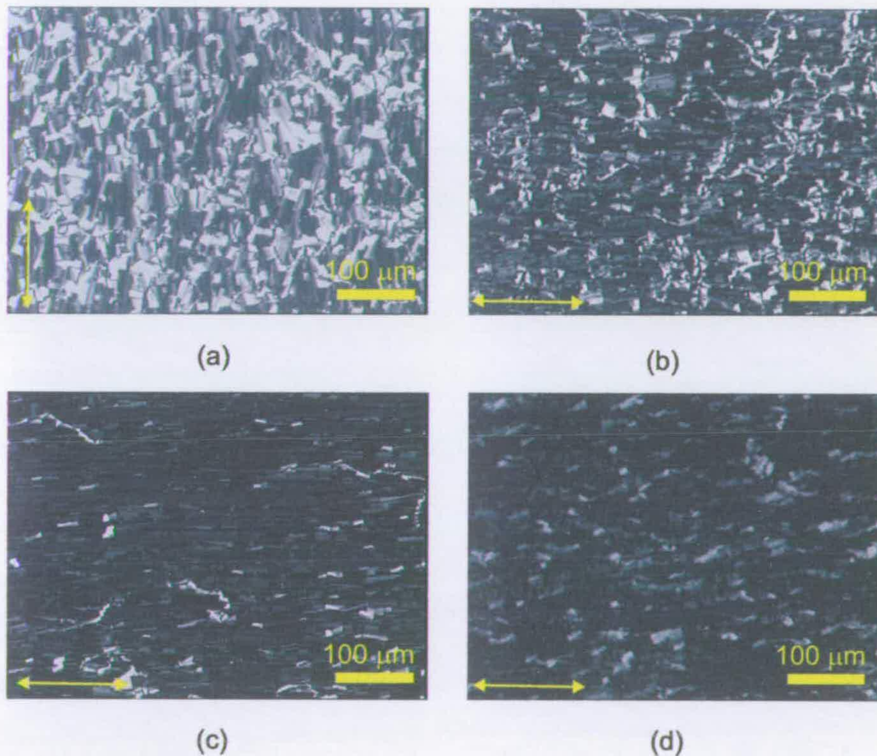


Figure 5.27: Micrographs showing the effect of exposure energy on the alignment obtained in the central region of the test cells by the bulk-photo-alignment method. (a) 4.5 J/cm2 (b) 9 J/cm2 (c) 18 J/cm2 (d) 36 J/cm2. The arrows indicate the direction of polarization of the LPUV light.

The mechanism of alignment was investigated by Sukhmal et al. [142] who demonstrated the formation of a thin layer of oriented photopolymer material on surface of the substrates of the cell, rather than a network of polymeric material spreading across the bulk of the cell as observed in blends with higher concentration of polymer [143].

A difference in texture could be observed between the region situated at the "entrance" of the cell (i.e near the filling edge) and the remaining area. This feature was also observed in cells cooled to room temperature without exposure to LPUV light. As shown in figure 5.28, in such areas the FLC was found to be fairly well aligned. It is thought that the filling process is responsible for such feature. A possible explanation is for the flow to cause the photopolymer molecules to orientate themselves in a way which causes the adjacent FLC molecules to align parallel to the direction of flow.

Figure 5.28: Micrographs showing the difference in texture between the central area of the cell (a) and region adjacent to the filling edge (b) observed in cells filled with the FLC+PVCi mixture. The textures were obtained just by cooling slowly to room temperature after filling without exposure to LPUV light.

In light of the results described above it was estimated that bulk-photo-alignment was not a method that could yield alignment of FLCs of sufficient quality for use in microdisplays. The next section presents alignment work carried out using photopolymers but this time alignment layers are deposited on the inner surfaces of the cell and exposure to UV light replaces the rubbing process.

5.4.2 Alignment on linearly photo-polymerizable polymers

Two experimental linearly photopolymerizable (LPP) materials (Rolic Technologies) were assessed in terms of their suitability for aligning FLCs. Because of the small amount of material available all experimental work was carried out on glass test cells. In the remaining of this thesis the two materials were be referred to as LPP1 and LPP2.

Coatings were prepared on ITO coated glass by spin coating. As for polyimide alignment layers the solution was dispensed through a 0.2 μm PTFE filter onto the substrate as to cover its whole surface area. The substrates were then spun at 3000 rpm for one minute with an acceleration of 500 rpm/s. Immediately after spin coating, substrates coated with LPP1 were placed onto a hotplate and held at 130°C for 15 minutes. The hotplate temperature was then raised to 200°C at a rate of about 5°C/min and held at this value for 60 mins. Films of LPP2 material were simply baked immediately after coating on a hotplate held at 150°C for 15 mins. The thickness of the resulting films was measured by be around 50 nm for both materials.

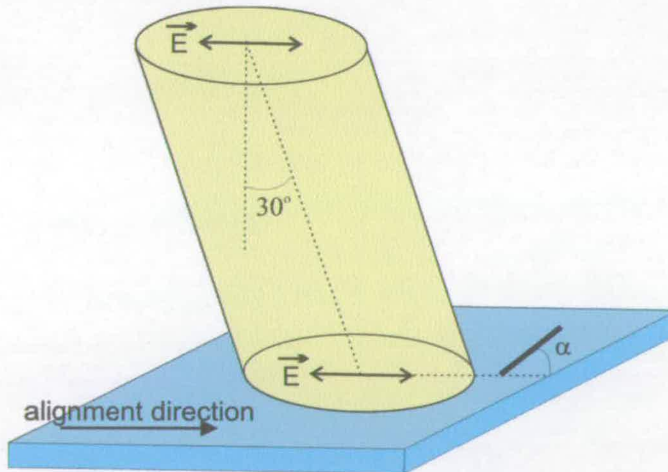


Figure 5.29: Schematic illustrations of the principle of exposure of LPP coatings with LPUV light.

Samples were exposed to LPUV light using the same illumination setup as that used for bulk-photo-alignment experiments. The substrates were held obliquely with respect to the axis of illumination. Figure 5.29 shows the relationship between incidence angle, polarisation direction (defined as electric field vector direction) and

pretilt angle. Whilst bulk-photo-alignment samples were held on a reflective silicon surface, LPP coated substrates were held onto a Perspex holder to avoid any unwanted reflection. The limited amount of material available forced the incidence angle to be kept constant at 30° throughout this work. The effect of the exposure energy on the alignment of FELIX 015-100 over the two LPP materials is discussed below. The cells were assembled with both substrates orientated as to see their pretilt angle point in the same direction. The alignment direction defined in figure 5.29 is equivalent to the rubbing direction employed previously in this thesis to provide information about the direction of alignment. The cross-linking mechanisms at the origin of the alignment of liquid crystals on LPP materials is discussed in the literature [144].

Ten minutes exposure equivalent to an energy of 3 J/cm^2 was found to be necessary to achieve fine scale alignment of FELIX 015-100 over LPP1 films. As shown in figure 5.30, smaller doses resulted in poor alignment even if some degree of orientation could be observed. Films obtained after 10 minutes exposure showed zigzag defects indicating the coexistence of C1 and C2 chevron orientations. As can be seen in figure 5.30c boat shaped domains could be observed in the area of C1 orientation. As the dose was increased to 6 J/cm^2, the whole area of the substrate was occupied with C1 chevron orientation. Boat shaped domains could be seen across the cell. The size and frequency of these domains was found to decrease when the exposure energy was increased to 9 J/cm^2 corresponding to a 30 mins exposure period.

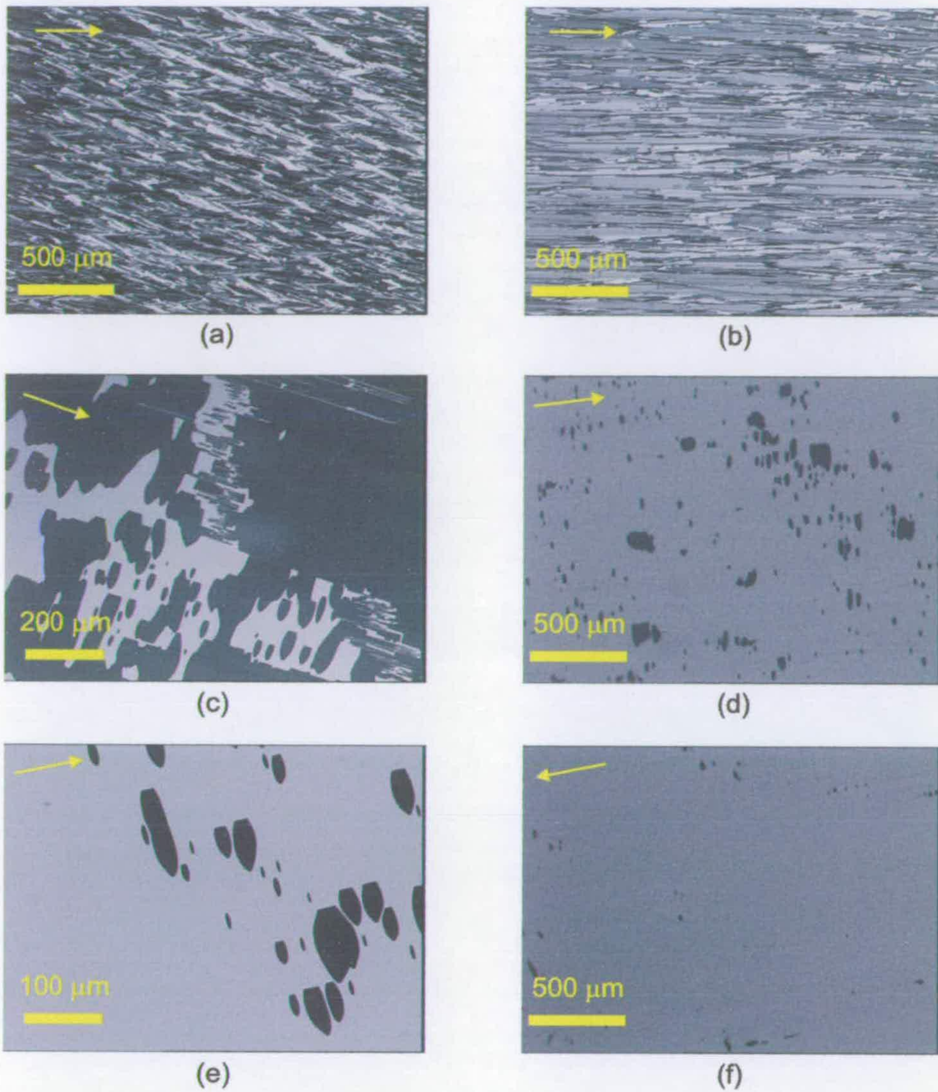


Figure 5.30: Micrographs showing the effect on exposure energy on the alignment of FELIX 015-100 over coatings of LPP1 material. (a) 0.3 J/cm2 (b) 1.5 J/cm2 (c) 3 J/cm2 (d,e) 6 J/cm2 (f) 9 J/cm2. The arrow indicates the alignment direction.

The quality of the alignment of FELIX 015-100 over material LPP2 was found to be independent of exposure energy. Fine alignment necessitated far less energy as complete alignment could be obtained after 60 seconds exposure (0.3 J/cm^2). Increasing the energy was not found to improve the alignment quality further. As in the case of LPP1 the large majority of the cells area was found to be in C1 orientation.

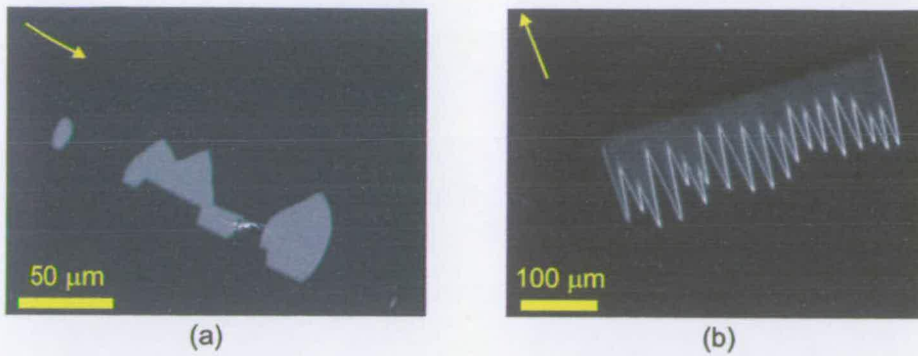


Figure 5.31: Micrographs showing the alignment of FELIX 015-100 over LPP1 material after 9 J/cm2 exposure (a) and over LPP2 material after exposure to 0.3 J/cm2 (b). The arrows indicate the alignment direction.

Alignment of FELIX 015-100 over LPP1 after 20 mins exposure to LPUV light was the best alignment obtained throughout the whole of the work carried out on alignment of SSFLCs. Repeatedly, cells produced using those material and exposure conditions did not contain any chevron defects. Defect free alignment over LPP2 could not be obtained. As shown in figure 5.31b, very small C2 islands enclosed in zigzag defect loops could be observed. As illustrated figure 5.31a, rather than zigzag defects boat shaped domain breakdown could be found in the vicinity of coating defects.

While C2 chevron orientation was induced by rubbed polyimide alignment layers, LPP films caused C1 chevron structure. Similar findings were reported by Kurihara et al. [145, 146] which interestingly compared the alignment of FLCs above the same material subjected to in one case to rubbing and the other to exposure to LPUV light. Numerical analysis recently explained such behaviour [147, 148]. Theoretical calculations of the free energy for the two chevron orientation have shown that low azimuthal anchoring conditions such as the one associated with photo-alignment will promote C1 orientation rather than C2. The behaviour of FELIX 015-100 over films of LPP1 material exposed to low doses of LPUV light (see figure 5.30) suggests that the anchoring between the alignment layer surface and the FLC molecules is weak and does increase with increasing the exposure time. Very low anchoring conditions, would explain why defect free C1 alignment could be achieved over LPP1 films.

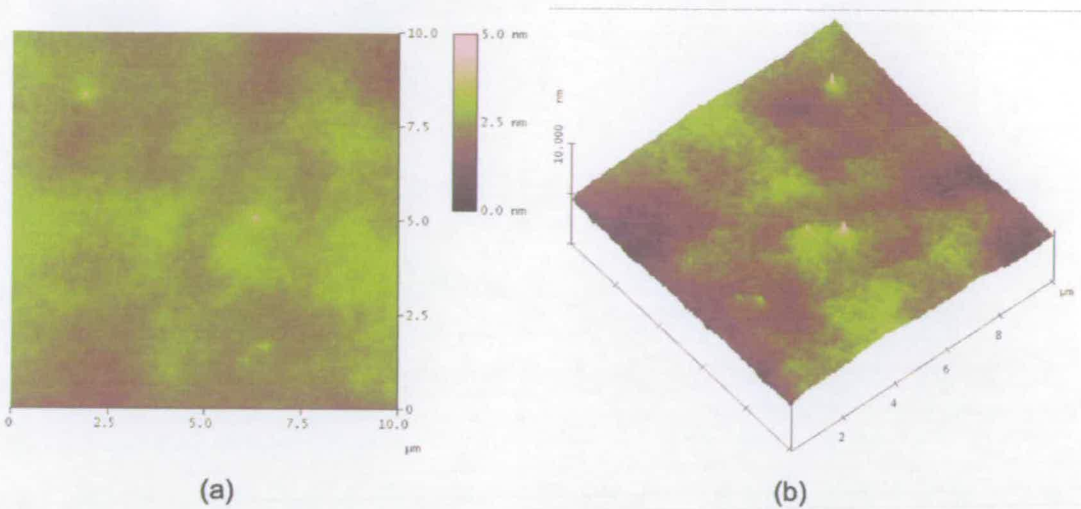


Figure 5.32: AFM images (a) and oblique plot (b) of glass substrate coated with 50 nm LPP2 material.

Calculations have also shown that there exists a critical azimuthal anchoring value at above which C2 orientation will be more stable than C1. This threshold value is dependent on pretilt. Therefore the topography of LPP films is also important to promote chevron defect free alignment. AFM analysis revealed that the topography of LPP films was similar to that of polyimide films prior to rubbing (see figure 5.32 and table 5.1). As mentioned before this is clearly an advantage when fabricating SSFLC systems.

Substrate	RMS roughness (nm)	
	5 µm x 5 µm scan	10 µm x 10 µm scan
Bare ITO	2.66	3.07
47 nm SE610 on ITO (unrubbed)	0.39	0.56
47 nm SE610 on ITO (rubbed)	1.01	1.02
51 nm LPP2 on ITO	0.43	0.48

Table 5.1: Roughness for various alignment layers used in this thesis as measured by AFM.

As shown in figure 5.33, the application of a square waveform (5Vpp, 500 Hz) to the glass cells fabricated using LPP1 films and filled with FELIX 015-100 gave rise to so called field lines or boat wake defects. Such defects are caused by the local rotation of the smectic layers [149,150,151] and are not reversible upon field removal. Unfortunately such defects are associated with light leakage and therefore are not desired in SSFLC systems for microdisplay applications.

Boat wakes defects were not observed in cells aligned with LPP2 material. It is possible that the presumed lower anchoring exhibited between LPP1 and FELIX 015-100 reduces the stress requirements for layer deformation.

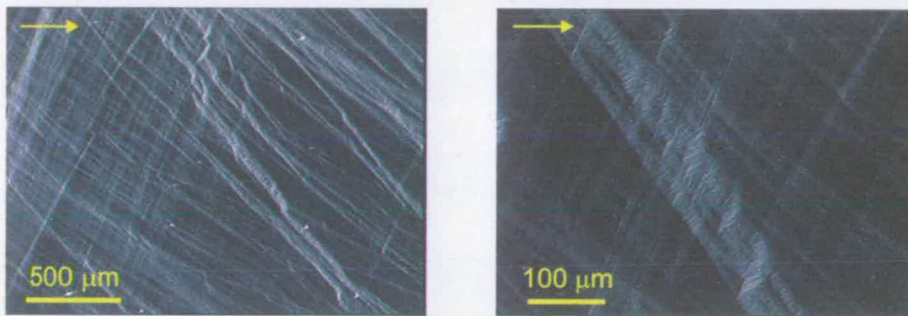


Figure 5.33: Micrographs showing boat wake defects forming when an electric field is applied to cells aligned with LPP1 material. The arrows indicate the alignment direction.

The electro-optical properties of the cells aligned with LPP2 and filled with FELIX 015-100 were measured and are shown in figure 5.34. Cells aligned using LPP films exhibited a slightly smaller dynamic switching angle compared to that measured in cells with rubbed polyimide alignment layers. At 30°C, a dynamic switching angle of 36.2° was measured on the LPP films compared to 39.1° on rubbed polyimide. Switching time measured in cells with the two types of alignment layers were found to be very similar.

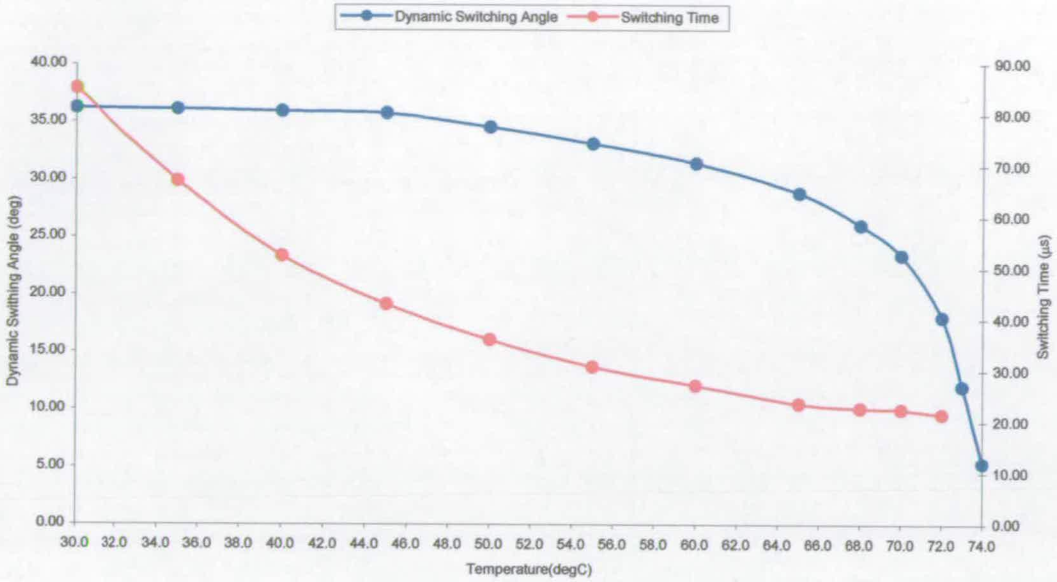


Figure 5.34: Graph showing the effect of temperature on the dynamic switching angle and switching time of FELIX 015-100 aligned over LPP2 films.

5.5 Summary

Alignment of SSFLCs with C2 chevron orientation was achieved over polyimide films subjected to low pressure rubbing. Under such conditions it is thought that the orientation of polymer chains induced by the rubbing process is responsible for alignment rather than the creation of groove as observed when using high rubbing pressure with roller based systems.

The topography of the substrates was found to have a strong effect on the appearance of zigzag defects. Reflective cells with thin pixel layers exhibited significantly better alignment with only a very low chevron defect density being observed. Filling of the inter-pixel gap did not seem to improve the alignment further.

Spacer particles were found to be associated with needle defects with one FLC material showing greater sensitivity than the other. The exposure of the pixel surface to oxide etch conditions which is at the heart of a simplified fabrication procedure for integrated peripheral spacer structures was not found to cause additional problems in terms of alignment.

FLC material FELIX 015-100 was found to be very suitable for use in microdisplay devices with a fairly large DSA (39° at 30°C and 5Vpp) and a switching speed inferior to 100 μs.

Reducing the alignment layer thickness caused an increase in DSA with very little effect on the switching time. The increase in roughness associated with the use of much thinner layers could however be problematic by increasing the likelihood of occurrence of zigzag defects.

Bulk photo-alignment of FLC material CS1031 was demonstrated. However the quality of the alignment was judged disappointing compared to that obtained between rubbed polyimide layers.

New photopolymers materials proved very promising with respect to aligning FLCs. Defect free alignment of FELIX 015-100 with a C1 chevron orientation was achieved. Unfortunately electric field induced defects were observed when driving the cell. Very high quality and stable alignment could be obtained on another LPP material even if small zigzag defects could not be avoided on the substrates employed in this work. The resulting electro-optical properties were found to be close to that obtained on rubbed polyimide films.

Chapter 6. Conclusion

6.1 Results summary

Advances in CMP of silicon oxide have made possible the degree of planarisation necessary to meet the unique cell gap requirements associated with FLCoS technology. It has also proved to be the first step towards high optical quality microdisplay backplanes. The application CMP, this time to aluminium, has also made possible the fabrication of a thinner, smoother and more reflective pixel electrode layer.

A low cost process sequence was developed to fabricate an integrated peripheral spacer structure in order to control the cell gap of LCoS displays. The absence of spacers in the active area of the device, although expected to be beneficial in terms of liquid crystal alignment quality, will necessitate stricter control of the curvature of the backplane.

A method exploiting the intrinsic stress of thin films deposited by PECVD to flatten silicon backplanes was demonstrated. Films deposited at the back of silicon wafers have been used to compensate the stresses resulting from the IC fabrication process. Patterning the stress compensation has been proposed to allow for the flattening of the backplanes exhibiting asymmetrical warpage due to the chip design.

Alignment of SSFLCs in the C2 chevron orientation with very low chevron defect density was achieved in glass test cells and in microdisplay envelopes using low pressure rubbing of polyimide films. AFM investigation suggests that under such rubbing conditions alignment is caused by the orientation of the polymer chains due to the rubbing process. Investigation of the dynamics of the same rubbing process revealed that the orientation of the polymer chains does not take place uniformly across the substrate surface but that elongated regions of material become oriented and that these areas eventually merge as the rubbing distance is increased. Decreasing the rubbing speed and increasing the rubbing pressure was found to favour the orientation of the polymer chains.

Some evidence of the intermediate stages of polymer orientation could be found when the rubbing pressure was very low. In the case of the polyimide and cloth employed in this work a minimum pressure of 2 g/cm^2 was found to be necessary to achieve uniform alignment.

Surface roughness was found to have a strong effect on the occurrence of chevron defects in SSFLCs. The density of these defects was greatly reduced on the thin pixel layer produced using the advanced post-processing procedure compared to the thicker layer resulting from the conventional process sequence.

Surprisingly the presence of the inter-pixel gap was not found to be at the origin of chevron defects. The processing steps aimed at filling the gap between the pixels during the preparation of the silicon backplanes do not appear necessary in the case of SSFLCs aligned on rubbed polymers.

The compatibility of the oxide etch process step involved in the fabrication of integrated spacer structure with the liquid crystal alignment, already put in evidence by AFM , was confirmed by alignment trials on rubbed polyimide.

Appraisal of the electro-optical properties of the SSFLC systems aligned over rubbed polyimide revealed that FELIX 015-100 (Clariant) is a suitable candidate for use in

FLCoS midrodisplay devices. The lower spontaneous polarisation of an alternative material resulted in a longer switching time unsuitable for use in microdisplay.
Interestingly it was observed that a reduction of the alignment layer thickness can lead to an increase in the dynamic switching angle. Alignment trials revealed that there is a critical aligment layer thickness below which the associated increase in surface roughness will introduce chevron defects.

Spacer particles were found to cause alignment defects. Different FLC materials appeared to be affected to a different degree by these. The work aimed at fabricating an integrated peripheral spacer structure is therefore relevant to the case of SSFLCs aligned on rubbed polymers.

Rubbing marks observed in a certain number of samples reinforced the appeal of having a clean non-contact alignment method.
Planar alignment of FLC material CS1031 (Chisso) was achieved by the bulk photo-alignment method. Unfortunately, the cosmetic quality of the SSFLC layer obtained was judged to be too poor in comparison to that achievable on rubbed polyimide films.

LPP materials (Rolic Technologies) proved very promising for aligning FLCs. Defect free alignment in the C1 chevron orientation could be obtained over one such material. Unfortunately, the alignment achieved proved to be damaged during switching. Another material gave rise to similar alignment which was stable under the application of an electric field compatible with FLCoS technology. Very few cosmetic defects were found to be associated with such system. It is the author's belief that the alignment achieved using LPP is close to commercial quality and that it could probably be improved by the use of substrates with a very smooth topography.
The electro-optical properties of the FELIX 015-100 material aligned with LPP films was measured to be close to that obtained on rubbed polyimide layers.

6.2 Concluding remarks and proposal for further work

The work presented in this thesis was mostly carried out on test structures and cells. Fabrication of functional microdisplay devices will be necessary to appreciate the benefits in terms of device performance.

While work towards developing a satisfactory post-CMP cleaning procedure is still required, it is the author's view that the developed methodology for post-processing of silicon backplanes (including the fabrication of integrated peripheral spacer structure) is ready to be applied to more expensive "product" substrates.

Since, as it was shown in this thesis, the molecular structure of SSFLCs make the use of particulate spacers unsuitable, efforts should also be made to implement the proposed flattening method to real devices. It is believed that die scale experimental work on product backplanes will allow a recipe to be developed relatively cheaply.

Fabrication of a series of benchmark microdisplay devices to measure the electro-optical performance brought about by the use of FELIX 015-100 on rubbed SE610 polyimide films is also suggested. More information on this reference system could be gained by measuring the pretilt and anchoring properties of the alignment layer in question.

The promising results obtained by using photopolymer alignment layers commend further work in this area. Other LPP materials as well as alternative commercial chemistries should be evaluated in terms of their suitability for aligning FELIX 015-100. Investigation of the effect of exposure parameters (incidence angle and energy) on the pretilt and anchoring properties of LPP films (and any suitable alternative material) should also be carried out for reflective and transparent substrates.

In addition to cosmetic and electro-optical aspects, the alignment achieved on LPP materials (and any suitable photoalignment alternative) should be assessed in terms of its stability to high light flux in order to judge its suitability for implementation in devices for projection applications.

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Appendix A

FLC materials

	CS1031	FELIX 015-100	FELIX 017-000
Supplier	Chisso	Clariant	Clariant
I - N phase transition temperature (°C)	97	86	87
N - S_A phase transition temperature (°C)	85	83	76
S_A - S_C phase transition temperature (°C)	60	72	70
S_C - X phase transition temperature (°C)	-12	-12	-26
Birefringence	0.170	0.160	0.172
Spontaneous polarization at 25°C ($nC.cm^{-2}$)	-28.1	+33	+9.5
Helical pitch (μm)	3	>100	32
Rotational viscosity at 25 °C (mPa.s)	265	80	47

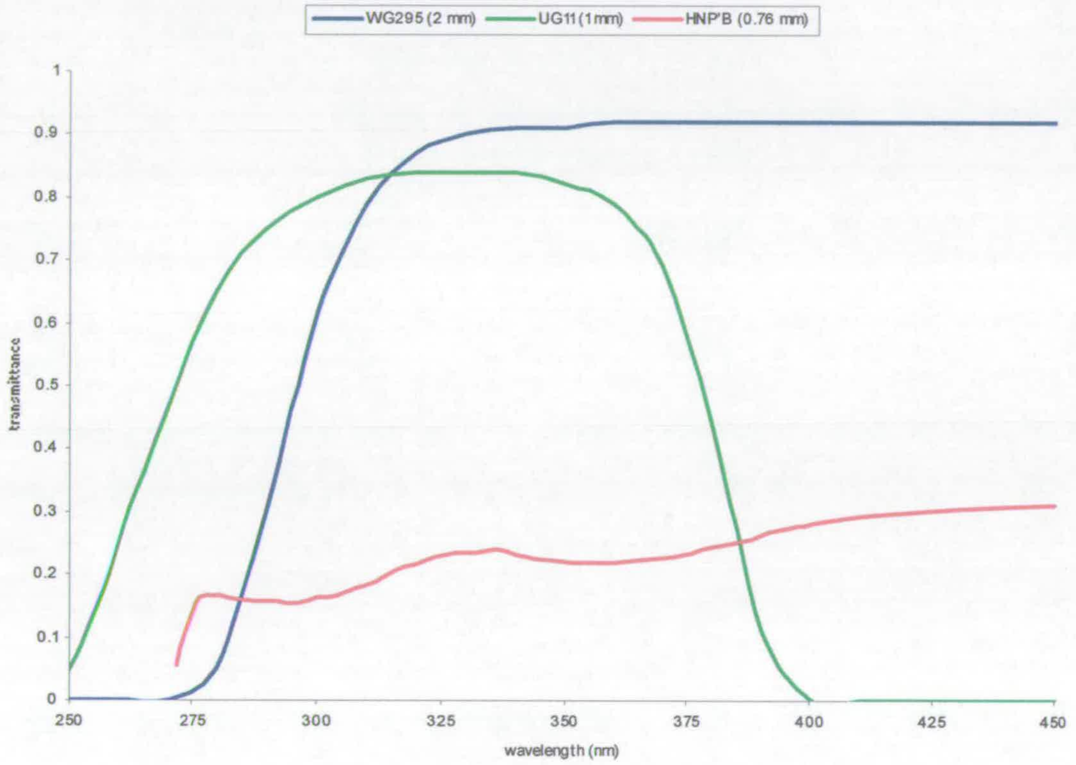
Appendix B

Norland Optical Adhesives

	NOA68	NOA81
Viscosity at 25°C (cPs)	5000	300
Refractive index of cured material	1.54	1.56
Elongation at failure (%)	80	25
Modulus of elasticity (psi)	20000	200000
Tensile strength (psi)	2500	4000
Hardness – Shore D	60	90

Appendix C

Filters



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