3D Representation and Characterisation

of IC Topography

Thesis submitted by

Jane Elliott

for the degree of

Doctor of Philosophy

Silicon Technology Research Group

The University of Edinburgh

1998

Abstract

Two trends are apparent in integrated circuit (IC) technology – a decrease in minimum feature size and an increase in die size. When combined, these trends lead to an increase in the number of transistors on a die, and therefore to a requirement for increasing numbers of interconnections. Due to decreasing track width and increasing use of multi–layer metal, interconnect has become more densely packed, both in the horizontal and vertical planes.

IC interconnect has associated with it both resistance and capacitance, and therefore always has some effect on circuit performance. As the density of interconnect on ICs increases, this effect becomes ever more significant. Highly accurate simulations are required to predict the value of the electrical properties of interconnect, with the most rigorous method being to simulate the interconnect in three dimensions. Due to the increasingly complex topography of ICs, creating a three–dimensional description of the interconnect for use with 3D simulation tools is not straightforward. This thesis presents a software tool, 3DTOP, which produces an appropriate three–dimensional description of circuitry using mask layout and selected process parameters.

In this thesis, various 3D representations of IC topography produced using 3DTOP are described, and the effect of the choice of 3D representation on extracted interconnect capacitance values is shown to be significant. In addition, the importance of considering interconnect capacitances when investigating circuit performance is illustrated, and a comparison of conventional and 3D extraction techniques is presented.

A further implication of the increasing complexity of IC topography is that as feature sizes continue to reduce, new processing techniques are required to reduce IC topography by planarisation. A test structure is described which uses inter–layer capacitance to determine the degree of planarisation of a wafer, and both simulated and experimental results are presented.

Declaration

I declare that all the work in this thesis is entirely my own unless otherwise indicated.

Jane Elliott

Acknowledgements

Contents

List of Figures

xiv

List of Tables

Chapter 1

Introduction

Integrated circuits (ICs) have become a part of everyday life in the developed world. It would be difficult now to find any electronic equipment currently in production which does not contain an IC of some description, and their use has become so prevalent that it is easy to forget that they have been in existence for less than forty years. In this introductory chapter, a brief historical background to the IC is given, and its development from the first 'solid circuit' to present day devices consisting of millions of transistors charted.

In order for current trends in the IC industry to continue, one of the hurdles which must be overcome is the problem of the increasing demands on the wires that connect together components on an IC, the *interconnect*. In section 1.3, an introduction to resistive and capacitive properties of interconnect is given, and the effect of scaling on interconnect discussed in section 1.4. Finally, the motivation for the work presented here and an outline of the thesis are included.

1.1   Historical Background

Prior to the invention of the transistor, the device used to amplify an electrical signal was the *valve* or *vacuum tube*. From 1942 to 1945, 17 000 of these devices were used
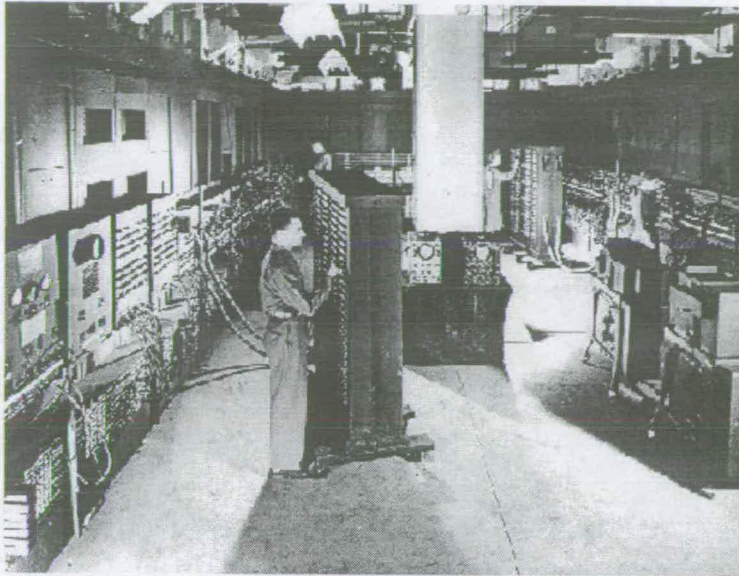
Figure 1.1: The first digital electronic computer, ENIAC.

to build the first digital computer, which occupied 1 500 square feet of floorspace and consumed around 174kW of power [1] (see figure 1.1). In 1945 therefore, technology was sufficiently advanced to produce a computer based on electronic devices. Clearly something revolutionary must have occurred to lead to the current state of electronic technology, where a pocket calculator can demonstrate superior computing power to the 30–ton ENIAC.

The revolution began in 1947, when Bardeen, Brittain and Shockley demonstrated the first solid–state amplifying device, or transistor [2]. The next leap of imagination was made by G. W. A. Dammer in 1952, when he suggested the idea of integrating electronics into a 'solid block with no connecting wires' [3]. Kilby set out to realise this idea, and in 1958 produced the first IC or 'solid circuit', a flip–flop built on a germanium substrate. From these beginnings, integration has increased to a degree that Kilby is unlikely ever to have imagined, and ICs have become the key technology for the 'information age'.

1.2 Integration and Moore's Law

The primary motivation behind integrating electronic components is an economic one. Since ICs can be manufactured using *batch processing*, with hundreds of die on an individual wafer and hundreds of wafers in each batch, the unit cost of each IC is small. Connecting components becomes straightforward and reliable, since it can form part of the process used to manufacture the components themselves. In addition to decreased cost, advantages of integration are reduced power consumption, increased reliability and increased speed.

Trends in the semiconductor industry are towards increasing wafer size, increasing die size, increasing circuit complexity and decreasing feature sizes. These latter three trends lead to increased integration, i.e. the inclusion of ever increasing numbers of transistors on a single IC, leading to increased functionality. This can be illustrated by examining one of the main applications of IC technology, the microprocessor. In 1975, Intel introduced their 8080 microprocessor, which contained 4 500 transistors (see figure 1.2). The 8086, which was introduced just three years later, had a transistor count of 29 000, and was followed by a succession of microprocessors, each one demonstrating a vastly increased degree of integration and functionality compared to the last. In 1995, the Pentium Pro was introduced, comprising a staggering 5.5 million transistors. In the space of 20 years, the number of transistors on a microprocessor increased over 1 000 times!

This increase in integration with time was investigated by Gordon Moore in the mid 1960s. He realised that there was a definite trend in the rate of integration, and put forward 'Moore's Law' based on his observations, which is now often used to predict future degrees of integration. He initially suggested that technology would develop such that the number of transistors which could be fabricated on a single IC would double each year [4]. In 1975, Moore suggested a change to his original law, to reflect the fact that innovations in increasing both die size and device density were less frequent [4]. The modified Moore's Law stated that doubling the number of transistors per IC would

3
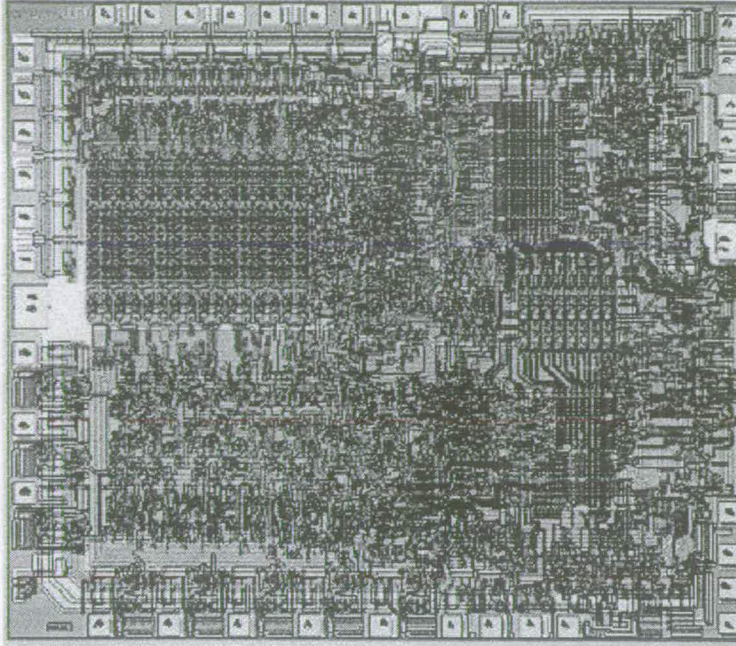
Figure 1.2: Intel's 8080 microprocessor, introduced in 1975.

take an increasing amount of time, perhaps even as much as two years. This is the situation in which Moore believes the IC industry is now [4]. Figure 1.3 graphically illustrates Moore's Law, in the period 1960 to 1990 [5], with the change in the law clearly visible as the gradient of the graph changes.

Since the early 1970s the rate of integration has followed a fairly constant and predictable trend. Figure 1.4 shows the degree of integration from 1970 to 1996, with microprocessors and memory marked on the graph, and illustrates a very good correlation between Moore's law and manufactured ICs over this period [6]. Predictions based on Moore's Law suggest that by the year 2015, microprocessor ICs containing 1 billion transistors will exist [4]

1.3 Effect of Interconnect on IC Performance

Historically, the driving force behind IC technology development has been scaling of the transistor. The motivation for this has been to gain improvements in IC packing density and performance [7]. The drive towards device miniaturisation is still very much in

4
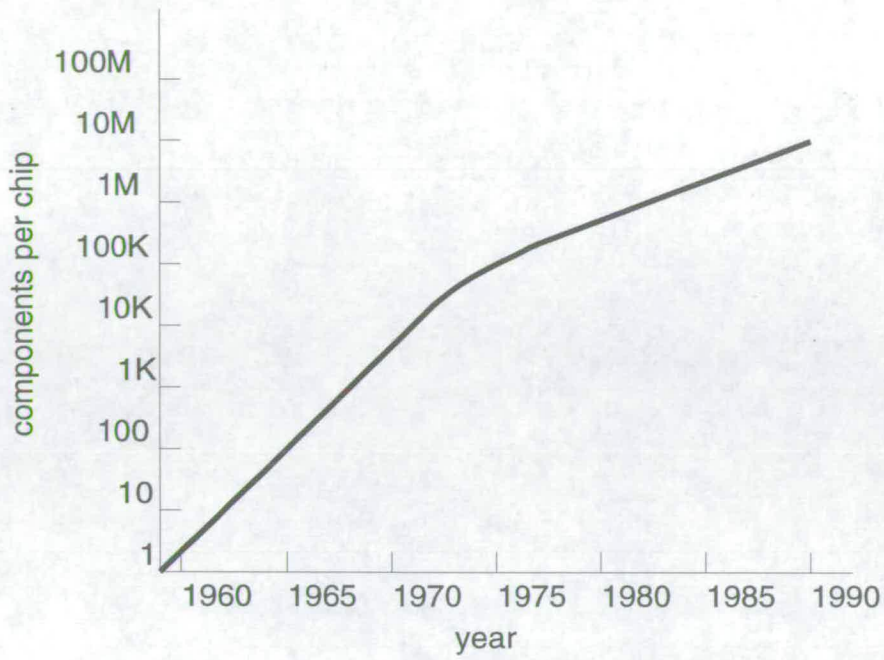
Figure 1.3: Components per chip vs year, illustrating Moore's Law.
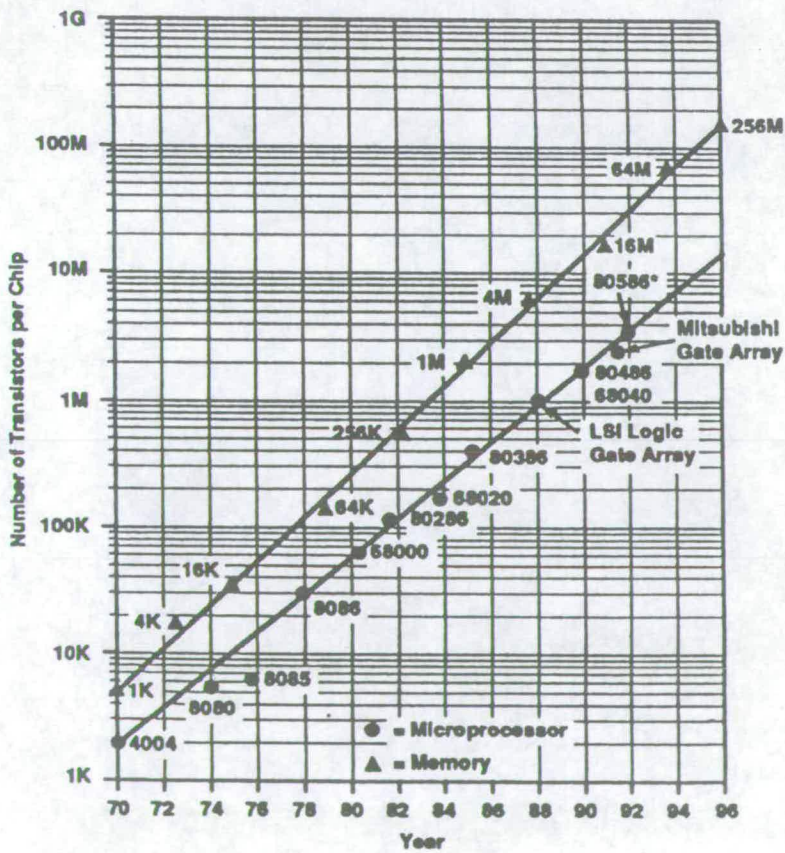
Figure 1.4: Density trends of microprocessors and DRAM memories.

evidence, with research into devices with channel lengths as short as $0.1\,\mu\text{m}$ reported [7]. However, considerable attention is now being focussed on scaling of interconnect. The reasons for this are twofold. Firstly, as the size of devices decreases, ICs become increasingly *interconnect limited*. This situation arises when the area required to connect devices together exceeds the area occupied by the devices themselves [6]. Possible solutions to this problem are to decrease interconnect pitch and to increase the number of layers of interconnect, leading to multi–layer metallisation (MLM) [8]. The second reason for increased concern about interconnect is that as it scales along with devices, the effect it has on IC performance becomes more significant [9].

Interconnect can be divided into four categories, depending on its function. *Local interconnects* are used to connect basic elements together to form gates or sub–circuits, and tend to be relatively short. *Global interconnects*, on the other hand, are used to connect these gates and sub–circuits together to form larger circuits or systems. Their length is limited only by the size of the chip. The two remaining types of interconnect are those carrying power to the various regions of the chip, and those which interface with the chip's packaging. These latter consist of either bonding pads or solder bumps [10].

An IC interconnection can be modelled as a distributed RLC network [6, 11], where R is resistance, C capacitance and L inductance. Typically in silicon ICs the effects of resistive and capacitive interconnect parasitics dominate those of inductive parasitics [9, 12]. This simplification becomes less acceptable where high currents, high frequencies (1–2 GHz) or long wires are concerned [9, 12]. In the following discussion, MOS technology and local interconnects are assumed, so the effects of inductance are ignored.

The RC delay of a wire is a very important parameter, since it determines the speed at which voltages can be transferred. Since MOS ICs are often *clocked*, i.e a global signal acting as a system clock is used to control the timing of the circuitry, an unexpectedly large RC delay on a node could cause incorrect operation of the circuit. Hence the RC delay on various key interconnections determines the maximum possible speed at

which the IC can be operated [8]. The value of capacitance is also important in its own right, since it can cause crosstalk between a node and surrounding wires [9]. The value of resistance determines the current for a given voltage across the wire, and therefore affects current density. This is a very important parameter, since it in turn affects the susceptibility of the wire to *electromigration* [13]. This is a phenomenon in which electrons forming the current in the wire collide with metal atoms, causing them to 'flow' in the opposite direction to the current. This can result in *voids*, which increase resistance of the wire and eventually cause it to break, and *whiskers*, which lead to the possibility of shorts between metal lines [14].

1.3.1 Dependence of Interconnect Resistance and Capacitance on Geometry and Materials

Resistance

The overall resistance of a wire as shown in figure 1.5 is determined by its physical dimensions and its resistivity, ρ (Ωm^{-1})

$$R = \frac{\rho l}{tw} \tag{1.1}$$

where

R = the total resisitance of the line (Ω)

l = the length of the line (m)

t = the thickness of the line (m)

w = the width of the line (m)

If the thickness of the conductive layer, t, is constant, and $l = w$, i.e. the area of conductor being considered is square, the resistance R between two opposite sides of
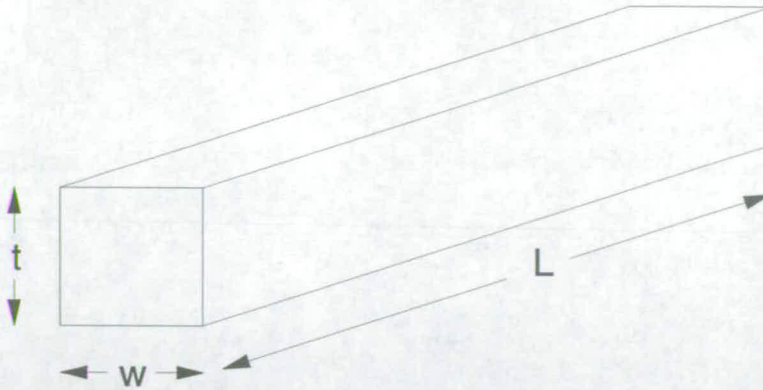
Figure 1.5: Small section of interconnect showing dimensions used to calculate resistance.
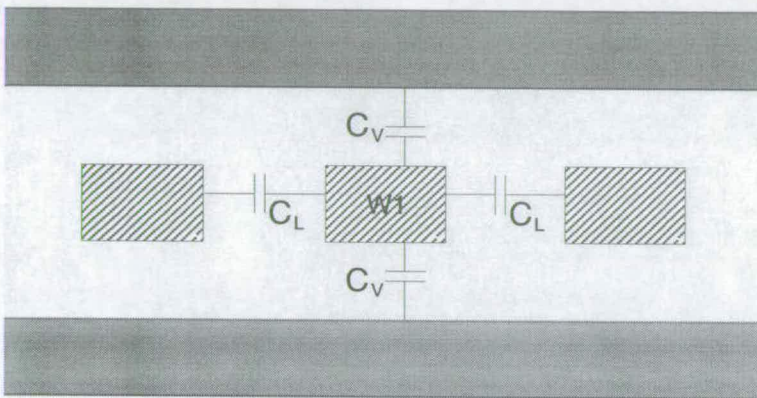
Figure 1.6: Cross section showing vertical and lateral capacitances (C_V and C_L) between interconnection W1 and surrounding interconnect in an orthogonal wiring array.

the square is a constant. This parameter is often used to define resistance in terms of ohms–per–square.

Capacitance

The overall capacitance of a wire is determined by the sum of all the capacitances between that node and those surrounding it. It comprises lateral capacitance, C_L, between the interconnection and those to either side of it on the same layer, and vertical capacitance, C_V, between the interconnection and those above and below it on other layers [8]. These capacitances are shown in figure 1.6, in which a simple orthogonal wiring structure with planarised inter–layer dielectrics is assumed. Using

8

a one–dimensional approximation, each component of the total capacitance can be represented by the well–known equation [8]

$$C = \frac{\epsilon_r \epsilon_o A}{d} \qquad (1.2)$$

where

C = capacitance between two conductors (F)

ϵ_r = the relative permittivity of the dielectric separating the two conductors (dimensionless)

ϵ_o = the permittivity of free space (F/m)

A = the area of overlap of the two conductors (m^2)

d = the distance separating the two conductors (m)

It can be seen from equation 1.2 that the total capacitance on the wire W1 is affected by the distance between it and adjacent wires both laterally and vertically, and by the value of the dielectric constant of the material between the wires.

From this simple analysis, it can be seen that the RC delay of a wire is affected by both the materials which form the IC and by the physical dimensions of the wire and surrounding interconnect. The way in which changes in these dimensions affect the resistance and capacitance of interconnect as feature sizes are scaled is discussed in the next section.

1.4   Scaling

Throughout the short history of semiconductor manufacturing, the trend has been towards the reduction of physical dimensions of all components on an IC, a process known as *scaling*. A simple strategy for investigating the effects of scaling was introduced

parameter	scaling factor (ideal scaling)	scaling factor (constant voltage)
feature size	$1/k$	$1/k$
doping concentration	k	k^2
voltage	$1/k$	1
current	$1/k$	k
power/gate	$1/k^2$	k
power density	1	k^3
device delay	$1/k$	$1/k$
local interconnect		
interconnect capacitance	$1/k$	$1/k$
interconnect resistance	k	k
interconnect RC delay	1	1
global interconnect		
interconnect capacitance	1	1
interconnect resistance	k^2	k^2
interconnect RC delay	k^2	k^2

Table 1.1: Scaling factors of some device and interconnect properties.

by Dennard et al in 1974 [15], and has become widely accepted [8, 9]. The strategy was introduced mainly to deal with scaling of MOS devices, although the effects on interconnect were also considered. Scaling has also been developed for bipolar ICs [10], but will not be discussed here.

Dennard at al introduced a dimensionless scaling constant, k, where all horizontal and vertical dimensions are assumed to scale by this factor. The supply voltage is also reduced by the factor k, and in order to maintain constant electric fields, the doping levels are increased by k [10]. This is known as *ideal scaling*, and results in the scaling factors shown in the second column of table 1.1. The die dimensions are assumed not to change, although in reality a decrease in feature size will often be accompanied by an increase in circuit functionality such that die size increases. The scaling factors are different for local and global interconnects, since local interconnects are expected to scale with the feature sizes, whereas global interconnects will have a length determined by the size of the die, which in this case will remain constant. This is reflected in the lower part of table 1.1.

There are two problems with this ideal scaling theory. Firstly, it assumes that supply voltage will scale as dimensions scale. This is not necessarily the case, since supply voltages are normally fixed at a standard value, such as 5V or 3.3V. Furthermore, scaling the supply voltage may not be desirable since it will reduce the noise margin on the threshold voltage of the devices. The scaling factors associated with *constant voltage* scaling are shown in column three of table 1.1. Note that the power per gate in this case now scales as k rather than $1/k^2$ in the ideal case. Therefore, with a constant die size and an increase in the number of devices on a die of k^2, the power dissipation per IC increases to k^3 rather than remaining constant in the ideal case. This implies that scaling devices without scaling voltage to some degree will lead to significant increases in power dissipation.

The second problem with simple scaling theory is that it assumes that vertical dimensions scale to the same degree as lateral dimensions. This is not true, particularly in the case of interconnect layers and inter–layer dielectrics, where the vertical thicknesses are generally accepted to scale as approximately $\sqrt{k}$ [9, 16]. Interconnect layer thicknesses are not scaled with k in order to prevent a large rise in resistance [17], which limits the increase in current density and therefore the susceptibility to electromigration [10, 14]. Therefore, interconnect resistance does not increase by the amount predicted by ideal scaling theory. Inter–layer dielectrics are not scaled to the same degree as feature sizes, since this can lead to reliability and yield problems, and will also cause an increase in the value of overlap capacitance between interconnect layers. This leads to a scaling factor for capacitance of less than the $1/k$ predicted. However, increasing the aspect ratio of interconnect tracks tends to increase the lateral capacitance on a node, since more electric field lines from each track terminate on adjacent tracks, rather than those above and below [16].

The effect on interconnect resistance and capacitance of non–ideal vertical scaling, and the increasing significance of lateral capacitance as feature sizes reduce, can be seen in figures 1.7 and 1.8, where capacitance and resistance per unit length are plotted against track width [16]. In figure 1.7, ideal scaling is assumed, so all dimensions
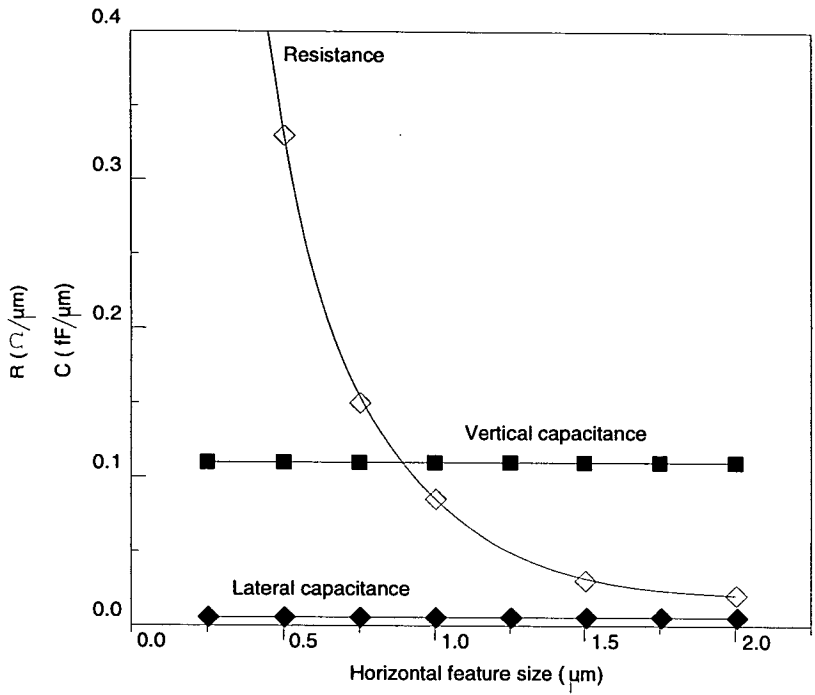
Figure 1.7: Parasitic capacitances and resistances of an aluminium interconnection and oxide dielectric system when all dimensions are scaled by k.
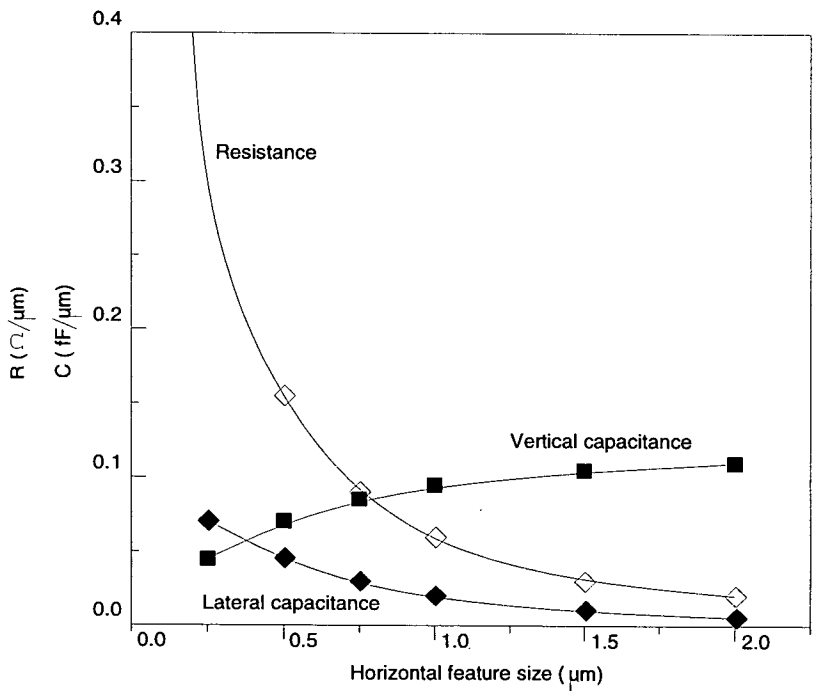
Figure 1.8: Parasitic capacitances and resistances of an aluminium interconnection and oxide dielectric system where lateral dimensions are scaled by k and vertical dimensions by the square root of k.

12

scale by the same amount. Since in this case there is no change in the distribution of electric field lines between interconnect tracks, both C_V and C_L remain constant [16]. Furthermore, since the value of resistance is proportional to the cross section of the track (see equation 1.1), resistance will increase as a function of k^2 as feature sizes scale. The more realistic situation, in which vertical dimensions are scaled by $\sqrt{k}$, is shown in figure 1.8. Resistance now increases as a function of $k^{3/2}$ [16], and lateral capacitance starts to increase compared to vertical capacitance.

A quantitative example of the increasing significance of interconnect delay is provided by Taur et al [7], in their investigation into CMOS device scaling to $0.1\mu m$. They quote a measured gate delay of approximately 50pS for a $0.25\mu m$ CMOS process operated with a 2.5V power supply. Compare this with the expected RC delay along a 4mm length of $1\mu m$ by $1\mu m$ aluminium interconnect of around 100pS [7], and the significance of interconnect delay becomes readily apparent.

The increasing significance of interconnect as devices are scaled is apparent from the results in table 1.1. Whichever type of scaling is used, whether ideal or constant voltage, whilst device delay is reduced, interconnect delay is not, i.e. *interconnect delay does not scale*. If vertical dimensions are assumed to scale as $\sqrt{k}$, the situation is not as bad as predicted by Dennard et al's scaling strategy [10]. However, a significant problem is still posed by the fact that interconnect delays do not scale at the same rate as device delays, leading to the need to develop new materials and processes, and to determine accurately the electrical characteristics of interconnect.

1.5 Motivation

With the trend towards increasing integration, as demonstrated by Moore's Law, the amount of interconnect required to connect the components on an IC increases. Furthermore, as scaling of devices and interconnect continues, the effect that interconnect has on circuit performance becomes more marked. For these reasons it is necessary

to accurately determine the electrical properties of interconnect. As the topography of ICs becomes more complex with increasing use of multi–layer metal, and with the increasing significance of lateral capacitance between interconnect tracks, it is necessary to recognise the three–dimensional nature of interconnect.

Three dimensional simulators exist which can determine the electrical properties of interconnect, and which require input data describing the IC layout in three dimensions. When creating such a three–dimensional representation, it is important that the data represents the true topography of the IC as closely as possible, since this has a significant effect on the interconnect's electrical properties. To produce such data by hand is a time–consuming and error–prone task, and is therefore unlikely to be accepted into a circuit designer's routine. There is therefore a requirement for a means of creating three–dimensional data which represents the topography of the IC directly from a readily available source, such as IC layout. The 3DTOP software presented in this thesis meets this requirement.

Since the topography of an IC is important in determining the characteristics of interconnect, it is necessary to assess its degree. This can be achieved by sectioning, surface profiling, or by using a test structure. Sectioning an IC is a difficult process, and destroys the sample. Surface profiling is time consuming, can only accurately determine the topography of features with smaller dimensions than the stylus tip, and provides no information on the topography of layers below the surface. An electrical test structure, however, can provide a means of efficiently determining the topography of a particular layer in an IC. Such a test structure has been developed and is presented in this thesis.

1.6   Thesis Outline

Chapter 2. The importance of considering interconnect capacitance in three dimensions is demonstrated, and strategies for accurately determining the value of interconnect

capacitance are discussed. Trends in IC processing which address problems created by the increasing demands on interconnect are outlined.

Chapter 3. The importance of technology computer aided design (TCAD) is outlined. Process simulation and process emulation are defined, and their suitability for producing a three–dimensional representation of IC topography is investigated.

Chapter 4. Software which produces a three–dimensional representation of IC layout, 3DTOP, is described. The data produced by 3DTOP and the procedure for running the software are presented. The creation of conformal and semi–conformal three–dimensional representations of IC topography is described in detail, and examples presented.

Chapter 5. Some applications of the 3DTOP software are described. 3DTOP is used to compare the results of three–dimensional capacitance simulations using different IC topography representations. Three–dimensional capacitance extraction techniques are compared with conventional capacitance extraction techniques, using a single transistor spatial light modulator pixel as an example. The applications of 3DTOP in the field of microelectromechanical structures are outlined.

Chapter 6. A test structure for use in characterising the degree of topography of an inter–layer dielectric following planarisation by chemical mechanical polishing is presented. Experimental work is described, and experimental results compared to those obtained by simulation.

Chapter 7. The work presented in the the thesis is summarised, and conclusions drawn. Suggestions for further work are made.

Chapter 2

The Three–Dimensional Nature of Interconnect – Simulation and Processing

The parasitic electrical characteristics associated with interconnect are becoming increasingly significant as feature sizes reduce, and must therefore be accurately determined. Since the need to consider parasitic capacitance in three dimensions is particularly important due to the increasing significance of lateral capacitance, C_L, simulation of interconnect capacitance in three dimensions is becoming necessary. In section 2.1, the need to treat the extraction of parasitic interconnect capacitance as a problem to be solved in three dimensions is discussed, and in section 2.2 various methods of approaching the problem of three–dimensional simulation are described.

The increasing complexity of interconnect in three dimensions poses several challenges which must be addressed by semiconductor processing. Firstly, there is a need to reduce the electrical parasitics associated with interconnect by means of introducing new materials and processing techniques. Secondly, the increase in metal track, via and contact aspect ratios as dimensions scale faster in horizontal dimensions than in vertical dimensions causes problems in the areas of electromigration and filling of vias and contacts. Finally, the use of increased numbers of interconnect layers, i.e. multi–level metallisation, raises further processing issues. The processing trends which address

these areas are briefly discussed in section 2.3.

2.1 Determining the Value of Parasitic Capacitance in Three–Dimensional IC Interconnect

As interconnect tracks become narrower and more closely spaced, and as the use of multi–layer metal increases, it becomes increasingly unrealistic to treat the extraction of interconnect parasitics as a problem which can be solved by considering the structure in either one or two dimensions. It is necessary either to treat the problem as one to be solved entirely in a three–dimensional solution space [18, 19], or to divide it into a well–specified set of smaller two–dimensional or three–dimensional problems which can later be combined to provide a total solution [20, 21]. Resistance, inductance and capacitance are important electrical properties of interconnect, as explained in section 1.3. However, we will limit our discussion here to the effects of the three–dimensional nature of interconnect on capacitance.

In order to demonstrate the issues involved in determining capacitance, we will consider a *crossover* structure as shown in figure 2.1. This structure, where one inter-connect track crosses another, occurs widely in ICs. For the sake of simplicity in this discussion, we assume perfect planarity of the inter–layer dielectric.

The simplest approach to finding the capacitance betweeen nodes n1 and n2 is to find the *parallel plate* capacitance, using equation 1.2, which is repeated below.

$$C_{pp} = \frac{\epsilon_r \epsilon_o A}{d} \qquad (2.1)$$

This can be thought of as a one–dimensional approach, since it it does not take any account of *fringing fields*. In reality, the electrical field lines between the two tracks do not all run parallel to the z–axis. Figure 2.2 shows the cross–section of figure 2.1(c) with the electrical field lines in the form assumed for a simple parallel–plate capacitance (fig-ure 2.2(a)), and a more realistic representation showing fringing field lines(figure 2.2(b)).
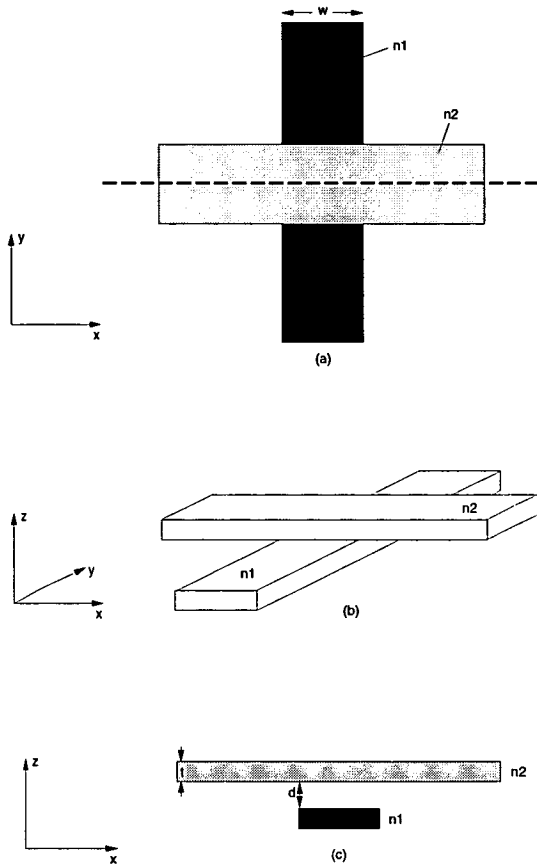
Figure 2.1: (a) plan view of crossover, (b) crossover (c) cross–section of crossover, in position indicated by dotted line in (a).
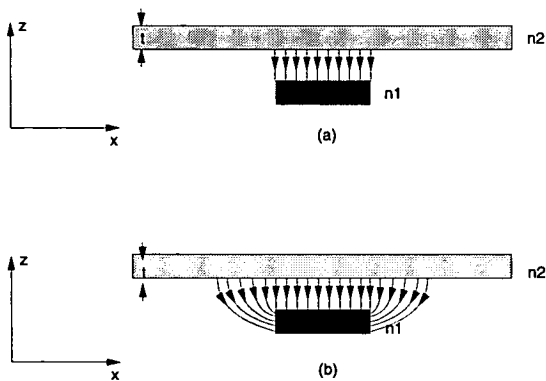
Figure 2.2: (a) Parallel–plate field lines (b) fringing field lines added.

18

If an accurate value for inter–layer capacitance is to be found, the fringing field must be accurately accounted for [22].

There are two possible approaches to finding the inter–layer capacitance in this situation which ensure that the fringing field is accounted for. Firstly, a value can be found for capacitance per unit length of the perimeter of the overlap between particular layers by either numerical simulation, test–structure measurement or analytical methods. The overlap perimeter of the structure of interest can then be found and multiplied by this parameter to give a value for the total fringing capacitance between two layers [22]. This value can then be added to the value found for the parallel plate capacitance to find the total inter–layer capacitance. The second approach is to perform a three–dimensional numerical simulation of the entire structure. This is more computationally intensive, but includes fewer approximations and therefore yields a more accurate result.

2.1.1   Increasing Importance of Fringing Capacitance with Reducing Feature Sizes

The importance of determining the fringing capacitance accurately depends on the proportion of the overall capacitance which is attributable to the fringing fields. The increasing significance of the fringing fields as feature sizes reduce will now be demonstrated. This discussion is based on an examination of a range of crossover structures. Figure 2.3 shows cross–sections of three crossover structures with varying track widths $w1$, $w2$ and $w3$, but a constant layer thickness. The cross–sections show a representation of electrical field lines drawn between the two nodes. These fields are shown in two dimensions for clarity, but exist in three dimensions in the crossover structure. We assume that the track forming n2 is infinitely long, and that the vertical distance separating the nodes, and the thickness of the layers, is constant. As track width decreases the contribution of the fringing capacitance to the total capacitance between nodes will increase, as shown below.

We assume that the total fringing capacitance, C_f, is directly proportional to the

(a)

(b)

(c)
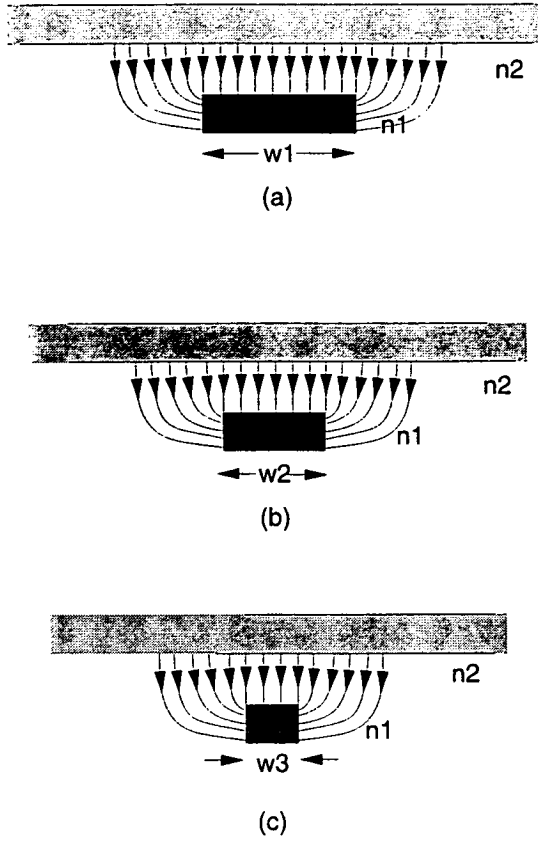
Figure 2.3: Cross–sections of three crossover structures with varying track widths.

perimeter of the overlap, P, i.e.

$$C_f \propto P \tag{2.2}$$

This does not take account of any effects at the corners of the overlap area, but the capacitance due to these effects is assumed to be constant for each of our three crossover structures, and so can be ignored in this case. We also know from equation 2.1 that since ϵ_r and d are constant, the parallel plate proportion of the capacitance, C_{pp} is proportional to the overlap area A, i.e.

$$C_{pp} \propto A \tag{2.3}$$

Since A is proportional to w^2, and P is proprtional to w, C_{pp} scales as w^2, and C_f scales as w. So as w reduces, C_f becomes increasingly significant in determining the total capacitance value, and the importance of obtaining an accurate value for the fringing capacitance increases.

Further illustration of the increasing contribution of fringing capacitance as feature

conductor width (μm)	conductor thickness (μm)	C_{total} (pF)	C_f (pF)	C_{pp} (pF)	% C_{total} due to C_f	% C_{total} due to C_{pp}
5	0.79	3.086	1.996	1.090	65	35
3	0.61	1.680	1.170	0.510	70	30
2	0.5	0.974	0.698	0.276	72	28
1.5	0.43	0.767	0.586	0.181	76	24
1	0.35	0.444	0.345	0.099	78	22
0.75	0.31	0.328	0.265	0.063	81	19
0.5	0.25	0.214	0.179	0.035	84	16

Table 2.1: Contribution of C_f and C_{pp} to C_{total} in a crossover structure with decreasing feature sizes

sizes reduce is provided by table 2.1. Here, the contribution to total capacitance between two orthogonal conductors made by C_f and C_{pp} is tabulated for conductors of decreasing feature size. The thickness of the conductors and inter–layer dielectric is not kept constant, but is scaled by $\sqrt{k}$, where the horizontal feature size is scaled by k. It is apparent from this table that, as interconnect is scaled, the contribution to capacitance made by C_f increases.

As feature sizes reduce it becomes grossly inaccurate to rely simply on the parallel plate capacitance, and this is illustrated further by van der Meijs [22]. Some texts propose the use of a factor by which C_{pp} should be multiplied to account for fringing capacitance [23], but this is clearly not acceptable since it treats fringing capacitance as if it is proportional to w^2, whereas it has been shown that it is much more closely proportional to w. A more accurate method in which the perimeter is multiplied by a factor found using analytical formulas [22] is an improvement on either of these approaches, but is still shown to yield significantly different results from those achieved using a full three–dimensional simulation [22].

The previous discussion has illustrated that even in a very simple structure, comprising only two conductors and in which perfect planarisation of the inter–layer dielectric is assumed, there are various approaches to determining capacitance, and that the accuracy of each approach is affected by the physical dimensions of the conductors involved.
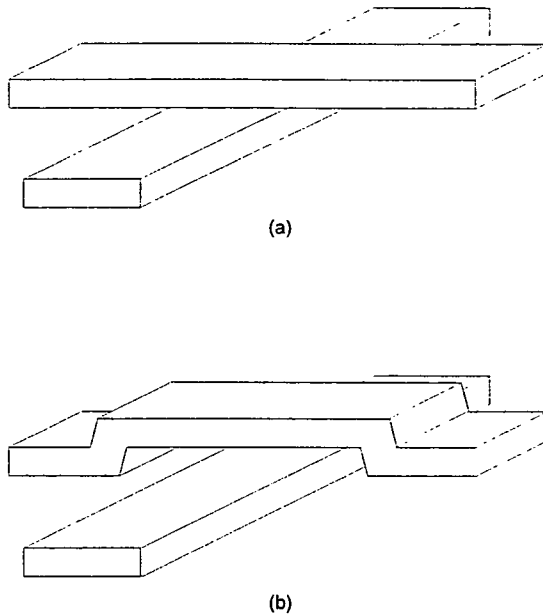
Figure 2.4: (a) Planar and (b) non–planar crossover structures.

The approach which requires the fewest approximations and which is therefore the most accurate across a range of structure dimensions is full three–dimensional simulation. Two further reasons can be put forward for considering such an approach. Firstly, if the process does not include perfect planarisation of the inter–layer dielectric, the structure itself becomes more complex in three–dimensional space, as illustrated in figure 2.4. The inter–layer capacitance, when the inter–layer dielectric is perfectly planar, (figure 2.4(a)) will differ from that when it is non–planar (figure 2.4(b)). Edelstein et al suggest that the difference may be greater than 20% [24]. This situation is investigated in detail in chapter 5 of this thesis, where the significance of the effect of dielectric planarity on interconnect capacitance is confirmed.

A second incentive to investigate any interconnect structure in three dimensions is based on the fact that crossover structures such as that illustrated will almost certainly not be isolated, i.e. other interconnect tracks may exist above and below, and to either side of the structure. Even if these surrounding tracks are of no interest in the problem under consideration, they may have a significant effect on the capacitance between the nodes of the structure, and failure to consider their effect may lead to an inaccurate solution [25].

In summary, this section has shown that as feature sizes reduce, the importance of finding an accurate value of fringing capacitance increases. It has been stated with reference to the literature that a one– or two–dimensional approximation to inter–layer capacitance in a crossover structure does not provide a sufficiently accurate solution. These solutions do not take account of non–planar IC topography, nor do they account for the influence of neighbouring wiring. For these reasons, a three–dimensional approach is required if accurate computed values of capacitance are to be obtained.

2.2   Extraction of Parasitic Electrical Properties

The majority of current research accepts the need to treat the extraction of parasitic interconnect capacitance as a three–dimensional problem [12, 18, 20, 22, 25, 26, 27]. The range of research on extraction of parasitic capacitances implies two major scenarios which require the extraction of parasitic electrical parameters due to IC interconnect. Firstly, a designer may wish to determine the properties of a wire used for a global connection, i.e. a wire which is common to many gates and subcircuits. An example of such a wire would be a system clock or a row or column driver. Alternatively, a localised and detailed study of a relatively small subcircuit may be required. In this case the designer would generally be more interested in capacitance than resistance, and would require a matrix of accurate values of the property of interest between each pair of electrical nodes in the subcircuit. Several approaches can be used to provide a solution to each situation.

The main motivation behind the choice of extraction technique at a system level is the provision of a reasonably accurate result whilst keeping the requirement for computing resources to an acceptable level. There are two schools of thought on how best to achieve this. Analytical methods, in which the capacitance between nodes is found by making use of an equation or a set of equations is an approach favoured by some [25, 28]. Kurosawa [25] claims an agreement between measured results and those found using his analytical technique to be of the order of 20% in many cases. Novel

analytical approaches are to be found in the literature, although some of these consider only very specific cases [29, 30].

An alternative to the analytical approach is to produce data pertaining to a wide range of specific situations using numerical simulations or practical experimentation, and to store the information as a model library. This is the approach favoured by Arora et al [20], in which agreements are quoted between extracted and measured values of 10–15%, although the examples used to produce these figures are fairly simple, consisting of no more than 5 electrical nodes. A similar approach is proposed by Aoyama et al [21], where instead of a model library a set of design charts is produced, again using numerical simulations. The disadvantage of these 'look–up–table' approaches is the necessity to produce a separate design chart or model library for each process. All of these system approaches appear to assume perfect planarity of inter–layer dielectrics, and no comment is made on the effects of a non–planar IC topgraphy. The parasitic extraction capability of the widely used Cadence software [31] uses pre–determined capacitance values per unit area or perimeter relating to specific combinations of mask layers. These are used along with physical dimensions derived from the layout to determine the required capacitance values, using equations provided in a technology file relating to a specific process. Further information on the Cadence parasitic extraction technique is given in section 5.3.2.

When smaller problems requiring highly accurate extracted values are considered, full three–dimensional numerical solutions become feasible. The algorithms used in these numerical solutions normally fall into one of four categories – finite difference, finite element, boundary element and multipole algorithms [20]. Many published algorithms exist [19, 26], some of which contain novel strategies for reduction in computing requirements [18].

The main benefit of analytical and look–up table solutions compared with fully three–dimensional numerical solutions is a reduction in the required computing resource. However, when the problem under consideration is fairly small, the use of

24

numerical simulation poses less of a problem. Numerical methods have several advantages over analytical and look–up table methods. The results are more accurate, and far more flexibility is possible. Provided that data is available in the correct format, in general any process can be considered using numerical simulators, with any combination of dielectrics, layer thicknesses and planarities. This allows a designer to consider the effect of changes in the process on a design without having to produce a new set of values for a look–up table. However, one of the problems of using this approach is that the data preparation of the three–dimensional coordinates required to fully describe the circuit to be analysed can be difficult and time–consuming. This thesis addresses this issue, and in Chapter 4 describes a means of obtaining these coordinates using the software 3DTOP.

The two numerical solution packages used in this thesis are Raphael [32] and FastCap [33], which use finite difference and boundary element algorithms respectively. The equation on which these simulators are based is Laplace's equation,

$$\nabla^2 V = 0 \qquad (2.4)$$

where ∇^2 is the divergence of the gradient of V, the potential. Equation 2.4 can be used to produce three–dimensional maps of field lines and equipotential surfaces describing any electric or magnetic field. Since capacitance between two objects can be described in terms of the potential distribution between them, this is an appropriate approach to determining capacitance.

Electric and magnetic field configurations depend on the boundaries of the field, so the type of 3D coordinate system chosen to solve the equation depends on these boundaries. For example, distribution of fields contained within rectangular boundaries will be solved for using rectangular coordinates. Many practical problems do not lend themselves to being expressed in any one coordinate system, so methods other than straightforward mathematical ones must be used. Most simulators use iterative methods, in which the area of interest is divided into a grid of points in space. A solution is aimed for in which the potential at any point is the average of the potentials at the six orthogonal surrounding points (for a 3D problem). This method is approximate, but

can be made sufficiently accurate by increasing the number of points in the grid [94].

2.3   Trends in Interconnect Processing

The main issues relating to interconnect that need to be addressed when developing processes are reduction in the resistance and capacitance of interconnect wires, reduction of electromigration, dealing with the increasing via and contact aspect ratios, and development of processes for multi–layer metallisation. Strategies for dealing with these issues will now be described.

2.3.1   Decreasing Resistance and Susceptibility to Electromigration

Since the 1960s, aluminium, often alloyed with a small percentage of copper and silicon, has been used as a material for metal interconnect [17]. The addition of copper, with its high resistance to electromigration, has gone some way to decrease the susceptibility to electromigration of aluminium interconnect lines. The addition of silicon helps to prevent spiking where aluminium and silicon come into contact [13]. Since copper has the second lowest resistivity of all metals (after silver) [34], this suggests that copper itself would be a good material from which to form interconnect, and in fact much research is centred on developing processes to allow successful depostion and etch of copper. Initial results are encouraging, with copper exhibiting good step–coverage and successful low–temperature deposition [34]. The main drawback of copper, in a highly competitive industry where strategic mistakes can be highly costly, is that it is a relatively unknown quantity, and its introduction would involve radical changes in manufacturing processes [13]. Aluminium–copper alloy has been used for decades, and whilst it will eventually fail to satisfy the industry's need for increased speed, evolutionary improvements in its performance are still being made [34].

One such improvement is the use of a thin titanium/titanium nitride contact, ad-

hesion and barrier layer at the top and bottom of each layer of aluminium alloy [13]. These layers have the effect of reducing contact resistance, and of providing a thin layer of conductive material forming part of the interconnect which is not susceptible to electromigration [17]. Thus, if voids form in the aluminium alloy as a result of electromigration, the resistance of the line will increase but a short is not created, and the possibility remains that the void will be repaired over time as a result of further electromigration.

2.3.2   Reduction in Capacitance

As interconnect pitch reduces, the amount of dielectric separating adjacent wires on the same layer decreases, leading to an increase in lateral capacitance, C_L (see figure 1.6). If the proximity of wires of a fixed vertical thickness is increased, the only way to counter the increase in capacitance between them is to decrease the relative permittivity, ϵ_r, of the dielectric material between them. Currently, the most commonly used dielectric material is silicon dioxide (SiO_2), which has a relative permittivity of 3.9. Much research activity is focussed on developing low–ϵ_r dielectrics [34]. Although numerous low–ϵ_r candidates exist, a dielectric for use in IC manufacturing must also exhibit suitable thermal and mechanical characteristics. More specifically, the material must be able to withstand the temperatures required for subsequent processing steps. Of particular concern are the thermal expansion coefficient of the material, which should be as low as possible, and the degree to which it softens at high temperatures. Some softening is beneficial from the point of view of step coverage and planarisation, but too much can lead to degradation of the pattern formed by the dielectric. The mechanical properties of the material should be isotropic, and the material should have the strength to suppress hillock formation in underlying metal layers. Currently, fluorine–doped SiO_2, polymers and aerogels are being investigated [8], but no one material has yet gained widespread acceptance.

2.3.3 Dealing with Increased Via and Contact Aspect Ratios

As discussed in section 1.3, feature sizes are reducing at a greater rate than inter–layer dielectric thickness. This results in ever higher aspect ratios of contacts and vias, which require filling with a conductive material to connect successive layers of interconnect. Historically, the aluminium alloy used to create interconnects has been used to fill contact and via holes. However, as aspect ratios increase, it is no longer feasible to use the standard aluminium sputtering process to fill contacts and vias, as the top becomes 'pinched off', leaving a highly resisitive and possibly open–circuiting void [13]. The industry standard method of dealing with this is to use tungsten deposited using chemical vapour depostion (CVD), with a titanium/titanium nitride contact, adhesion and barrier layer typically deposited prior to the tungsten [13].

An alternative to tungsten plugs is *forcefill aluminium* [35]. This technique involves sputtering aluminium onto the dielectric containing the contact or via holes, and then applying pressure ($\sim$60MPa) at high temperature ($\sim$400°C) to push the aluminium into the holes and fill them completely. This approach is expected to be manufacturable, but is not widely used.

2.3.4 Multi–level Metallisation

Multi–level metallisation (MLM), has been presented in section 1.3 as a solution to the problem of ICs becoming increasingly interconnect–limited. However, as the number of layers used in the manufacture of an IC increases, new problems arise. The main issue is the increasing complexity of the topography of the IC surface, and the demands that this makes on lithography tools and on deposition of interconnect materials [6]. A reduction in feature size leads to a reduced depth–of–focus in lithography tools, so vertical variations in IC surface topography cause difficulties as they approach or exceed the depth–of–focus. Similarly, a complex IC surface topography puts increasing demands on deposition processes, since reliable step–coverage becomes more difficult

28

to achieve [6]. Therefore, processes have been developed to ensure that the inter–metal dielectric shows very little topographical complexity, i.e. that it is *planar*.

Two main approaches exist to obtaining planar inter–layer dielectrics. Firstly, the inter–metal dielectric can be planarised during or following deposition over a patterned and etched metal layer. This can be achieved in several ways, including thermal flow, bias–sputtered dielectrics, etchback, spin–on–glass, and chemical mechanical polishing (CMP) [36] (see chapter 6). Whatever method is used, the aim is to produce global planarity across the wafer. The following metal layer can then be deposited, patterned and etched on this nearly flat surface [6].

An alternative to this approach is to use *damascene* processing. In this case, a layer of dielectric is deposited, and is then etched to form trenches. Metal is deposited over the entire wafer, filling the trenches, and is then polished back so that only metal inlaid in the trenches remains. Further oxide is then deposited to produce a planar surface ready for the next proces step [37].

A further development of damascene processing is the *dual–damasacene* approach. This involves patterning and etching the dielectric into which the metal is to be inlaid twice, to produce trenches for both interconnect tracks and vias to the underlying layer [13]. The main issue faced by dual–damascene processing is the difficulty of filling deep, high aspect–ratio holes in the dielectric, but since CVD processes currently exist to enable deposition of both aluminium and copper [13], this should not be an insurmountable problem. The attraction of the dual–damascene process lies in its simplicity and repeatability [37].

In summary, this discussion has highlighted developments in semiconductor pro-cessing technology which aim to reduce the effect of IC interconnect on circuit perform-ance. It should be noted, however, that many ICs are still produced using less advanced processes than those outlined here. It is generally agreed that future generations of ICs will be manufactured using planarising MLM schemes, with the introduction of copper

and low permittivity dielectrics occurring when no further progress can be made with these MLM processes [8, 17, 34].

2.4   Summary

In this chapter, the importance of treating the extraction of interconnect capacitance as a three dimensional problem has been discussed, with reference to fringing fields, non–planarity of the inter–layer dielectric and the effects of neighbouring interconnect lines. Furthermore, it has been shown that as feature sizes reduce, the significance of fringing fields, and hence the need to treat capacitance extraction as a three dimensional problem, increases.

Strategies for extracting interconnect capacitance in three dimensions at system level and at sub–circuit level have been described, with numerical 3D solutions being put forward as the most appropriate technique in smaller layouts. The necessity of producing appropriate data representing IC layout in three diemsions for use with 3D numerical simulators has been pointed out.

Trends in semiconductor processing which aim to address problems posed by the increasingly three–dimensional nature of interconnect, and to reduce the effects of interconnect on circuit performance, have been outlined.

Chapter 3

TCAD, Process Simulation and Process Emulation

In all aspects of IC design and manufacture, simulation tools are available to aid the designer or process engineer. For example, an IC designer may wish to determine circuit performance, and may therefore turn to a circuit simulator. A process engineer may wish to simulate the effect of a change in a particular process parameter on the physical structure of the circuit when it is manufactured, whereas a device engineer may wish to simulate the effects of that same parameter change on the properties of an individual device. The changes in the device parameters will then affect the results of the circuit simulation. Put simply, engineers regularly use simulators to help them design circuits, processes and devices, and each area of design interacts with the others. TCAD systems aim to provide a range of simulators which meet the needs of engineers in all areas of IC design and manufacture, and ideally allow easy and efficient data transfer between these tools.

All of the many different types of simulator required can be collected under the heading of technology computer aided design, or TCAD. In this chapter, a general overview of TCAD will be given. This will be followed by descriptions of two specific TCAD system components, process simulation and process emulation, with a view to demonstrating their suitability for generating data for interconnect analysis.

3.1 TCAD

TCAD systems are currently being developed at various academic and industrial sites [38, 39, 40]. These systems comprise different elements, but the aim of each system remains the same – to provide the capability to simulate processes, devices and circuits [40]. The main motivation for TCAD is the need to find ways of improving performance, reliability and yield of IC technologies accurately and efficiently, and to reduce the need for time–consuming experimental work, thus minimising the time to market [38]. A frequently stated aim is that all elements within a TCAD system should be fully integrated [39, 40, 41, 42], so that they can be used effectively as a whole, and due to developments in this area and improvements in the user–interface, the use of TCAD within the semiconductor industry is becoming more widespread [43].

TCAD systems can be described in terms of process simulation, device simulation, parameter extraction, interconnect simulation and circuit simulation [39]. Each of these areas is important, but in this chapter we will concentrate on specific aspects of TCAD which involve the production of structural representations of IC interconnect, since the relevance of the 3DTOP software presented later in this thesis can best be seen against this background. The application of the 3DTOP software is largely in the field of a further component of TCAD, namely interconnect simulation, which was discussed in the previous chapter.

3.2   Process Simulation and Emulation

In this section, two distinct approaches to producing data describing the physical structure of an IC are described, with a view to assessing their suitability for interconnect analysis. It is becoming increasingly necessary to analyse interconnect in three dimensions (see Chapter 2), so the three–dimensional capabilities of process simulation and process emulation are of particular interest here.

Process simulators, which involve the use of numerical equations based on physical models to simulate all aspects of silicon manufacturing technology, are widely available, and will be described in section 3.2.1. Their solution space is generally in one or two dimensions, although three–dimensional simulators are now being developed. Due to the complex models used by process simulators, they require significant computing resources and produce fairly accurate results. Process emulators, described in section 3.2.2, are based on empirical models, and as such are less resource–intensive than process simulators, although this dictates that they are also less accurate. The solution space of process emulators is usually three–dimensional, since the complex models which hinder the development of three–dimensional process simulators are not required.

3.2.1   Process Simulation

Process simulation involves the numerical solution of equations describing the physics of specific steps in the manufacturing process, namely diffusion, oxidation, lithography, ion implantation, deposition and etch. The result of a set of these simulations is an accurate description of the geometry and doping profiles of the specified area of the IC or device [42]. The methods used in performing the simulations, the degree of integration with other simulation and visualisation tools and the number of dimensions in the simulation space vary from simulator to simulator. A brief overview of some available process simulation tools is now presented, followed by an outline of some of the problems encountered in their use, an explanation of their applications and an assessment of their suitability for describing interconnect in three dimensions. The solution space of process simulators may be in one, two or more recently three dimensions. Three–dimensional simulators are not widely available, so to adequately describe process simulation, two–dimensional as well as three–dimensional simulators will be referred to here.
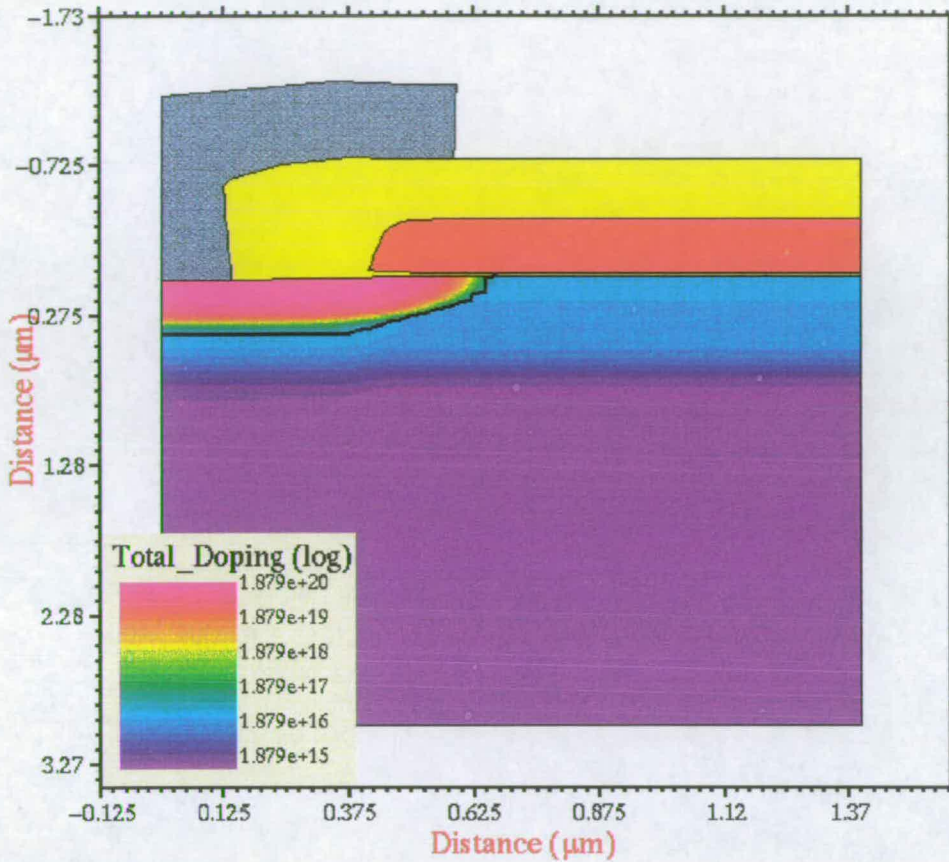
Figure 3.1: Simulation output from TSUPREM4, showing cross section and doping profiles of part of a 1.2μm NMOS device.

Two Dimensional Process Simulation

A widely used two–dimensional process simulator is TMA's TSUPREM4 [44], which covers a whole range of processing steps. Figure 3.1 shows the output of a TSUPREM4 simulation of a 1.2μm NMOS device, in which both the cross–sectional topography of the device and the doping profiles within the silicon are shown. In this case, doping and diffusion processes, and topographically important deposition, growth and etch processes are all incorporated. Several other process simulators exist which have similar capabilities to TSUPREM4, such as SUPREM3 [45], SUPREM4 [46] and SSUPREM4 [46].

The simulation of implantation and diffusion is of little interest in the field of

34
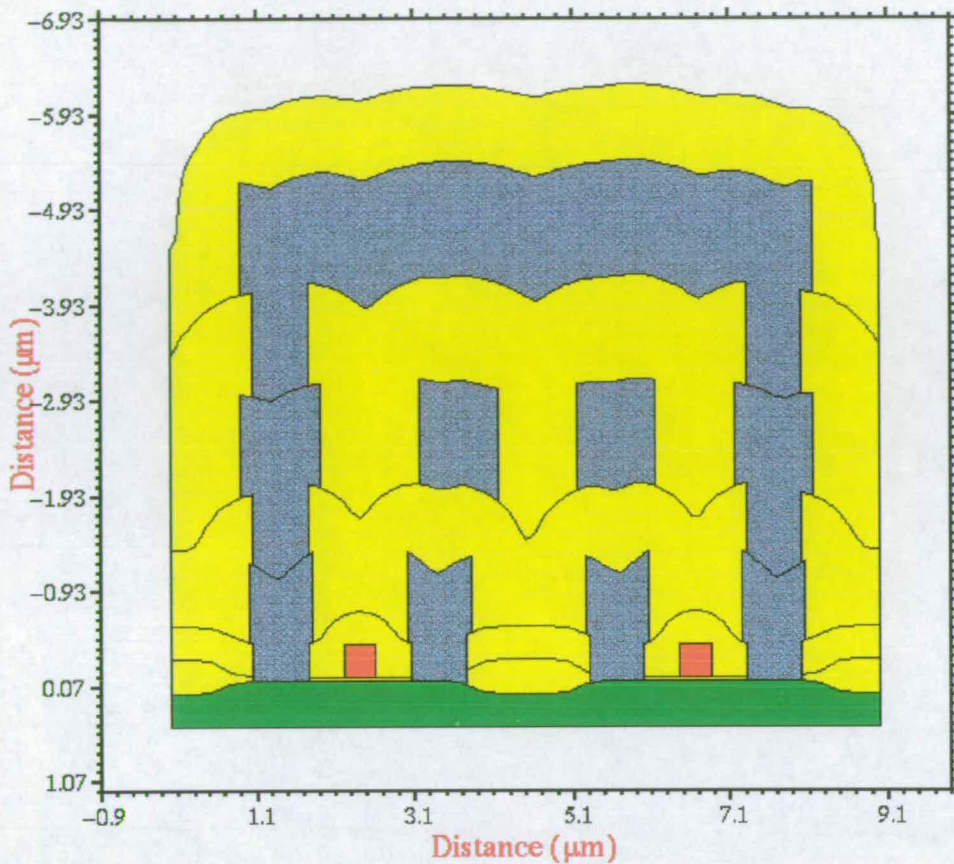
Figure 3.2: Sample output from TMA's deposition and etch simulator, TERRAIN.

interconnect, and will not be discussed further here. Of more interest are simulators, algorithms and models dealing with deposition [47, 48, 49, 50, 51], etch [52, 53, 54], lithography [55, 56], and combinations of these processes [57, 58, 59, 60].

Simulators exist which deal with both deposition and etch. For example, TMA's TERRAIN [61] and Silvaco's ELITE [62], can both be used to perform two–dimensional deposition and etch simulations. Figure 3.2 shows the output from a two–dimensional TERRAIN simulation, involving a series of conformal deposition and etch steps. Two–dimensional deposition simulators can also be used to simulate the deposition of metals in vias, as shown in figure 3.3.

Photolithography, whilst not directly contributing to IC topography in the same way as deposition, which adds material, and etch, which removes material, is nevertheless
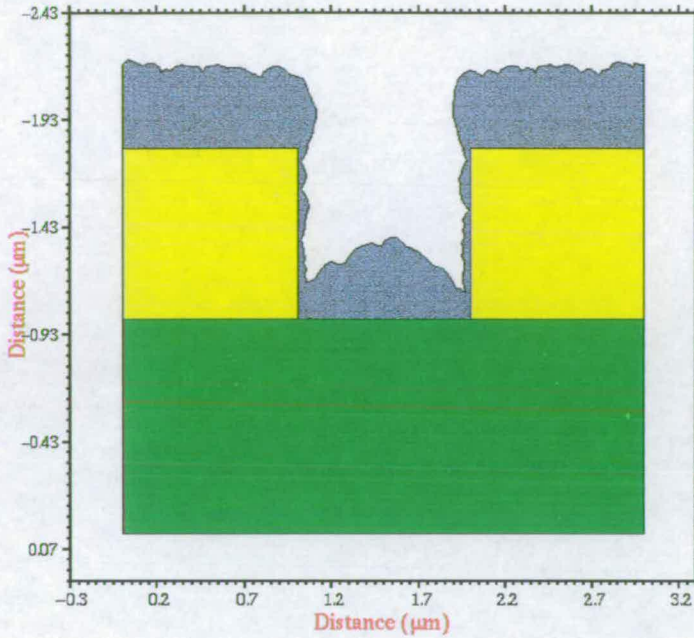
Figure 3.3: TERRAIN simulation of metal deposition in a via.

important in defining topography since it determines which areas of the IC will be affected by the following processing step. A lithography simulator such as TMA's DEPICT [55] determines in two dimensions how the mask pattern will be transferred onto the photoresist, and allows analysis to determine the printability of a pattern with a specified type of stepper. Figure 3.4 shows an example of an area of a mask overlaid with a DEPICT simulation of the expected pattern.

Three Dimensional Process Simulation

In recent years, considerable effort has been concentrated on developing three–dimensional process simulators [48, 49, 51, 52, 54, 57, 63]. This involves an increase in computing resource and time required compared to one– and two–dimensional process simulators, although this problem is widely recognised and is often dealt with to some extent by ensuring that the algorithms employed are as efficient as possible [57]. Three–dimensional etch and deposition simulators include SAMPLE–3D [57, 60] and Silvaco's HIPEX [64], both of which simulate lithography, deposition and etch in three dimensions. TMA's TERRAIN [61] can also be used to perform three–dimensional

36
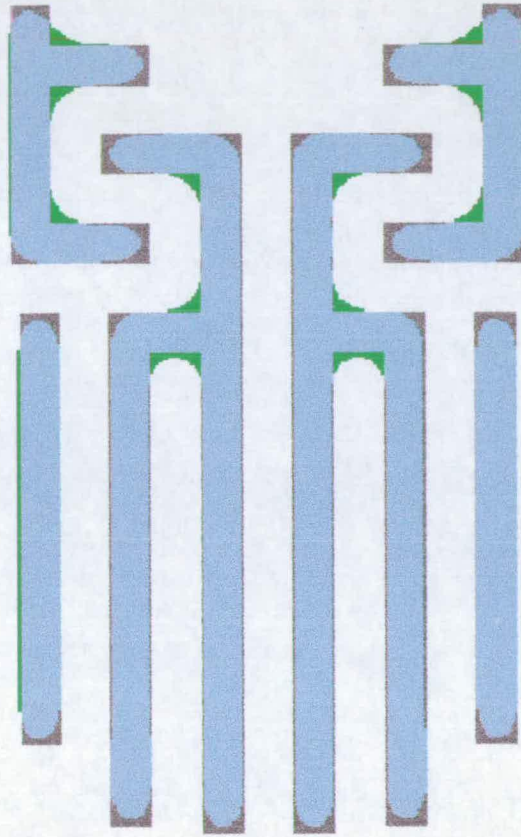
Figure 3.4: Drawn mask data overlaid with DEPICT simulation of the expected pattern transferred to photoresist.
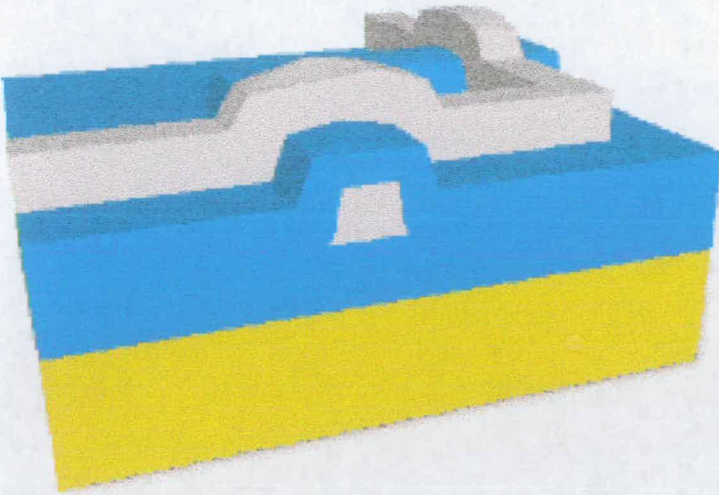
Figure 3.5: HIPEX representation of an area of interconnect.

etch and deposition simulations. Figure 3.5 shows a representation of an area of IC interconnect created by HIPEX. Figure 3.6 shows the output of a SAMPLE–3D lithography and etch process on a polysilicon elbow, along with the original structure and the mask used [60].

A problem encountered in process simulation, whether in two or three dimensions, is a lack of good models of the process steps [63]. Accurate models are essential to process simulation [38, 39], but are difficult to develop since the required data can only be obtained indirectly [38, 43]. As new materials and technologies emerge, further models must continually be developed [43].

The data produced by process simulators can be used in several ways. Visualisation of the physical structures predicted by the simulator can aid in understanding the effects of certain process parameters without the need for extensive practical experimentation [50, 59]. The results from a process simulation may also be used as input to a device simulator [40], which can be used to determine the electrical characteristics of single devices [39].

Process simulators are generally used to look at small sections of layout in great detail. Their complexity dictates that the resource requirements when considering
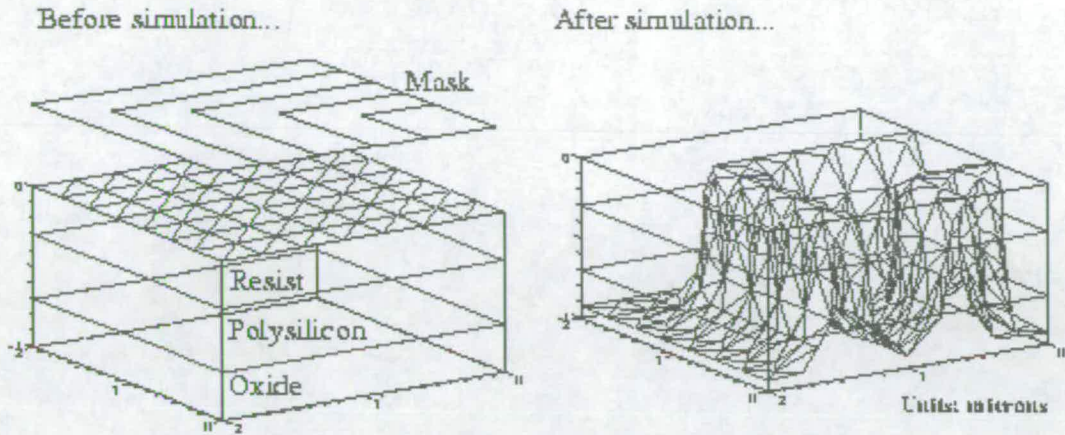
Figure 3.6: Three dimensional IC structure, before and after a SAMPLE–3D lithography and etching process.

anything other than a small area of layout would become prohibitive, particularly if a three–dimensional solution were required. When performing interconnect analysis, the area under consideration will often be of a size that a process simulator could not reasonably be expected to deal with. Furthermore, process simulators will produce a more accurate representation than is generally required for interconnect analysis.

Due to the increasing complexity of interconnect analysis, and the move towards performing the analysis in three dimensions, a three–dimensional representation of the interconnect structure will often be required. It is therefore apparent that a tool is required which can quickly produce a three–dimensional representation of the physical structure of an appropriate area of an IC. In this case, some accuracy of the representation may be sacrificed in order to reduce the required resources. Process emulators, described in the next section, fit this description.

3.2.2 Process Emulation

The process simulation tools described in the previous section aim to produce a highly accurate representation of a small area of an IC by the solution of numerical equations.

When considering the structure of IC interconnect, such a rigorous approach is not always necessary. In this situation, a *process emulator*, which requires much reduced computational resources compared with a process simulator will often suffice [39]. Process emulation as defined in this thesis involves the production of a structural description of an area of an IC based on an empirical approach. Due to the reduced computational resource involved, and the fact that there is no requirement for complex models, there are fewer barriers to considering the area of IC of interest in three dimensions when using process emulation than when using process simulation, as demonstrated by the availability of process emulation tools which use a three–dimensional solution space [39, 65, 66].

The feasability of three–dimensional process emulation as a tool for use in representing and analysing ICs was first demonstrated by Koppelman and Wesley in 1983, using OYSTER (Off–line Yorktown System for Three– dimensional Emulation of VLSI Research) [65]. This initial study explored the possibilities of two approaches, one based on physical processes, in which the system has 'knowledge' of VLSI manufacuring processes, and the other based on the observed results of processes on the IC structure. The former approach is analagous to the process simulation described in the previous section, while the latter fits our definition of process emulation.

Koppelman's system is based on a solid geometric modelling approach, of the type often used in mechanical engineering. The IC is represented by a set of three–dimensional solid objects, which are altered as processing steps are performed. The sequence of processing steps applied to the geometric data–base is identical to those to which the IC is subjected, and involves steps such as *grow oxide*, *deposit material*, *apply photoresist*, *expose*, *develop*, *wash*, *etch*, *lift–off* and *implant*. The areas affected by each step are determined by data describing the masks used in the IC manufacture.

The OYSTER feasability study [65] involves the creation of a three–dimensional representation of a field–effect transistor (FET) and the use of a capacitance simulation tool, which implies that appropriate uses of OYSTER would be in IC structure visual-

40
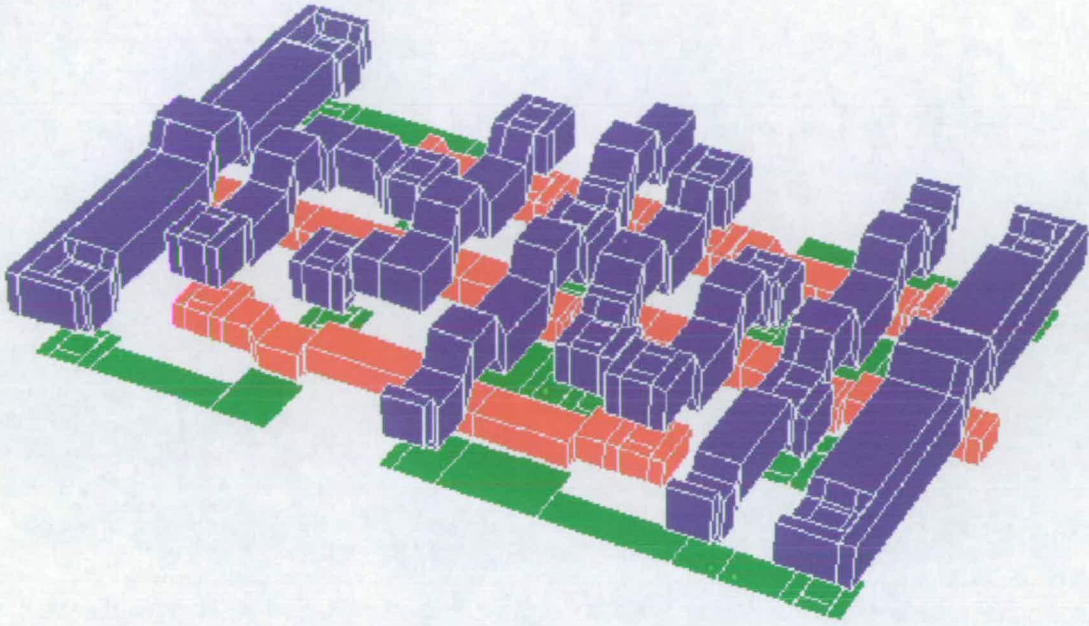
Figure 3.7: Three dimensional interconnect structure created by the SPACE 3D layout–to–circuit simulator.

isation and interconnect simulation. A further possible application of OYSTER is in the representation and design of microelectromechanical structures (MEMS) [67].

The availability of process emulation tools is much less than that of process simulation tools. AT&T have a process emulation tool, EASI, which forms part of their TCAD suite [39]. It is intended for use with AT&T's interconnect simulators, and produces a three–dimensional representation of metal, polysilicon and insulator using a process recipe and mask information. Process emulation also forms part of the TRICEPS tool [66], which takes in information relating to mask and processing data, produces a simulation space in three dimensions, and calculates capacitance between wires. This tool is somewhat limited in that it can only accept straight wires parallel to the x and y axes, and does not interface with other visualisation and simulation tools. Similarly, process emulation forms a part of the SPACE three–dimensional layout-to-circuit extractor [12, 27], in which orthogonality of the conductors to the x– and y–axes is assumed. Figure 3.7 shows a representation of interconnect in three–dimensions

generated by the SPACE tool.

The process emulators described in this section are all incorporated into specific tools or TCAD suites, which limits their flexibility. There is therefore a need for a generic process emulation tool which interfaces with a range of interconnect simulation tools, and makes no simplifying assumptions regarding dielectric planarity and orthogonality of interconnect to the axes.

3.3   Summary

In this chapter, the constituent parts and applications of TCAD have been described. The roles of process simulation and process emulation within the TCAD environment have been outlined, and a brief overview of simulation and emulation tools given. The relatively small number of available process emulation tools compared with process simulation tools has been mentioned, as has the trade–off between accuracy of representation and resource requirements. Process emulation tools have been shown to be suitable for providing data for use with three–dimensional interconnect analysis tools, and the need for a generic, non–process–specific, three–dimensional process emulator demonstrated. In Chapter 4, the 3DTOP software will be shown to make considerable progress towards fulfilling this need.

Chapter 4

3DTOP

4.1 Introduction

As IC feature sizes reduce and the number of layers of interconnect increases, circuit
designers are increasingly interested in the parasitic interconnect capacitances in their
designs. Currently, the most accurate means of determining interconnect parasitics by
simulation is to use a 3D simulator. Two of the most widely used software packages
which can simulate interconnect capacitances in three dimensions are Raphael [32] and
FastCap [33]. The Raphael software is based on the finite difference method, and takes
its input in the form of 3D shapes. It creates a rectangular mesh, with the number
of points specified by the user, and produces a capacitance matrix as output. FastCap
uses an algorithm based on the boundary element technique, and requires its input in
the form of 2D boundaries which represent 3D shapes. It requires the user to provide
these boundaries already discretised. FastCap produces both a capacitance matrix and
a postscript file for visualisation of the structure.

In order to make use of these 3D simulation packages, a description of the layout
in three dimensions is required. Producing such data by hand is a time–consuming
and error–prone process for anything but the smallest layouts, so an automatic method
of creating the data is required. The 3DTOP software described in this chapter has

43

been developed to meet this need by creating a 3D representation of layout directly from the 2D mask data. Whilst many current solutions to this problem assume perfect planarisation for each layer, 3DTOP can be used to produce planar, semi–conformal and completely conformal 3D representations. This allows the engineer to choose the most appropriate representation for any process, and so leads to improved accuracy. The difference between these types of representation is explained in the following section. 3DTOP can create data for use with the 3D capacitance simulators FastCap and Raphael, and with the ray-tracer POV–Ray [68], which can be used for visualisation of ICs in three dimensions to enable designers to gain invaluable insight into the 3D nature of their design. Since these are widely used simulators, 3DTOP is likely to be easily incorporated into an engineer's routine.

In this chapter, the output formats of 3DTOP are described, as is the required input data. The major algorithms implemented in the 3DTOP software are described, along with important data structures. IC layout examples are used to demonstrate 3DTOP's capabilities.

4.2   Data Produced by 3DTOP

3DTOP can be used to automatically produce a planar, semi-conformal or conformal 3D representation of an IC layout from the 2D mask data. These three types of representation will be described with reference to the simple 2D example layout shown in figure 4.1. Planar, semi-conformal and conformal 3D representations of this simple layout are shown in figures 4.2, 4.3, and 4.4 respectively.   The 3D data in these figures is in the boundary format, which will be described in more detail in section 4.4.7. Notice that in the planar representation the structure of each layer is unaffected by the topography of layers underneath it. In the semi-conformal representation the topography of underlying layers does have an effect on following layers, but is not followed exactly, since some smoothing occurs as successive layers are created. In the conformal representation each layer's topography directly reflects the topography of the layers beneath

44
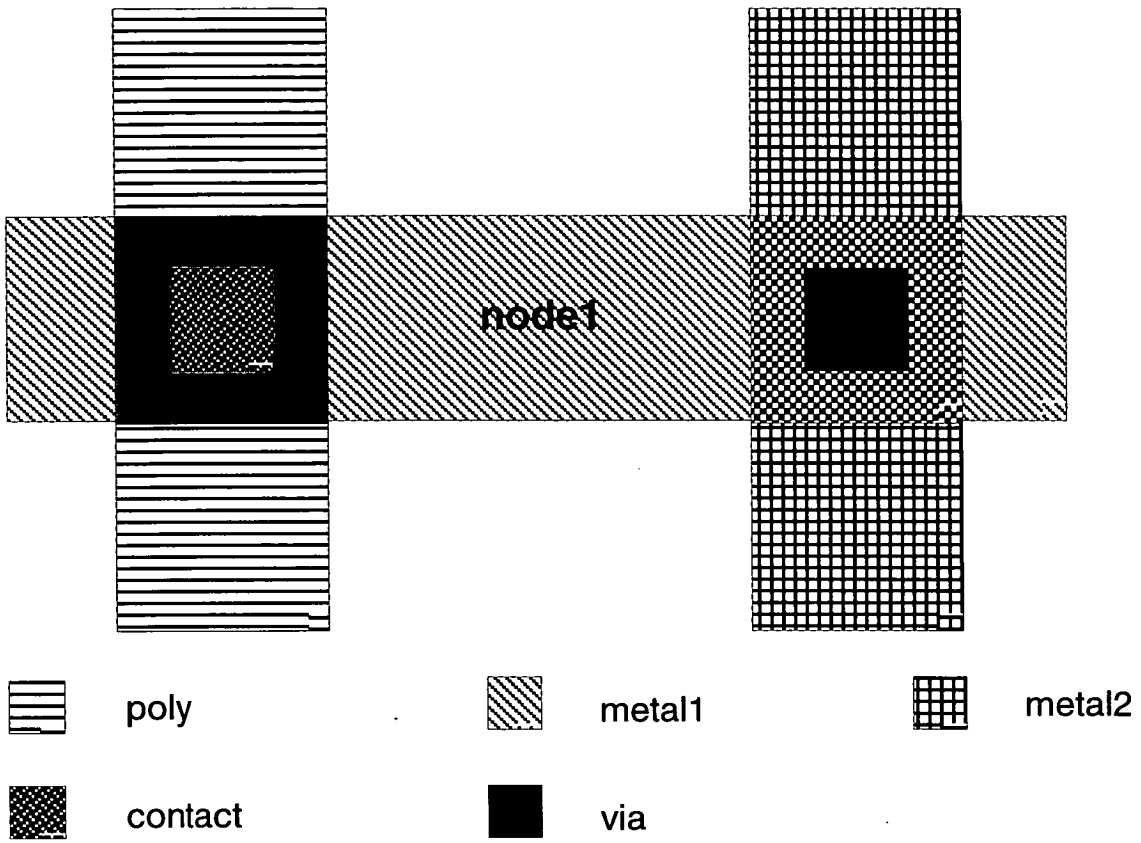
Figure 4.1: 2D example layout.
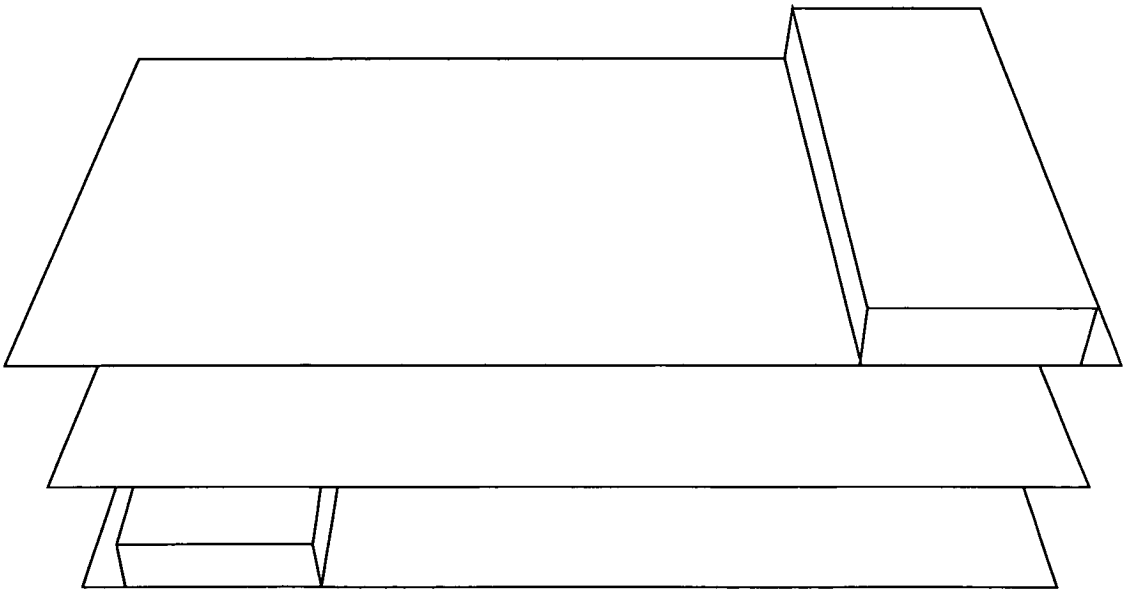
Figure 4.2: 3D planar representation of layout shown in Figure 4.1.

45
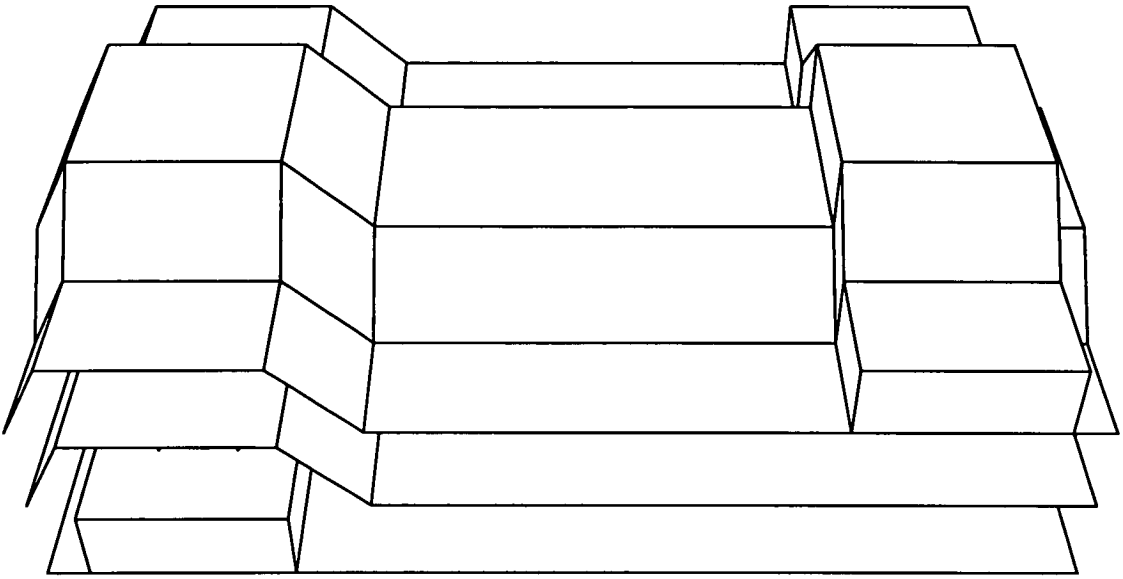
Figure 4.3: 3D semi-conformal representation of layout shown in Figure 4.1.
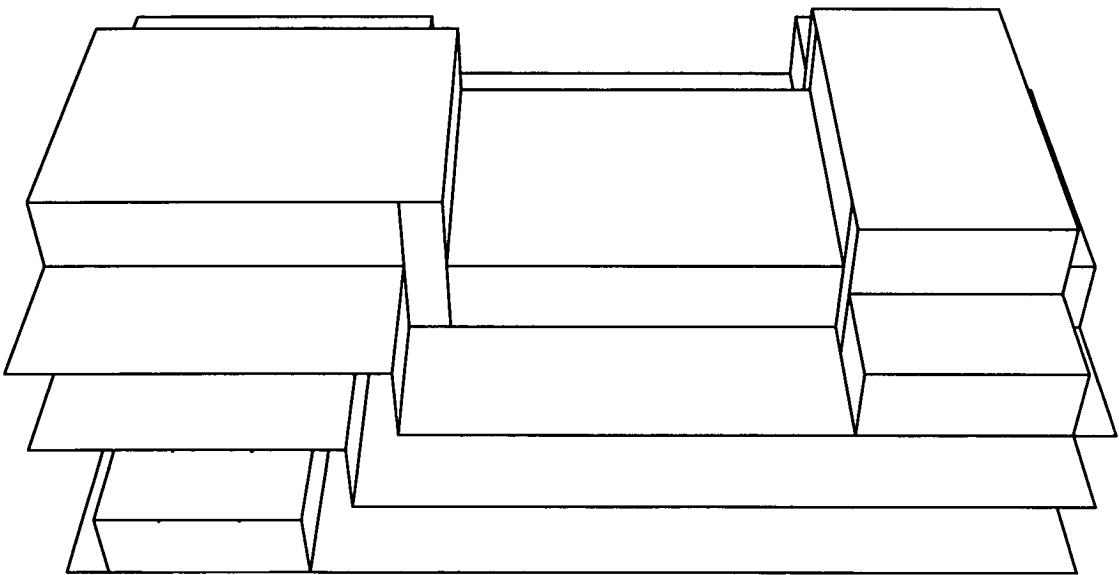
Figure 4.4: 3D conformal representation of layout shown in Figure 4.1.

it. In all cases etching is assumed to be anisotropic, so all layer edges are vertical.

3DTOP produces data in 2 different formats – as 3D shapes, a format compatible with Raphael, and as 2D boundaries representing 3D shapes, a format compatible with FastCap, making it easy to use with either simulator. Both data formats can be used in conjunction with all three 3D representations with the exception a semi–conformal representation in the format of 3D shapes. This combination is not supported since many of the shapes created are not accepted by Raphael, rendering the data useless in this context.

4.3   Running 3DTOP

3DTOP requires two files as input – a *mask description file* which describes the IC layout in two dimensions, and a *control file* which contains data relating to the process and the required representation. There follows an example of a mask description file, which has been created from a GDSII [31] file using conversion software. The GDSII file can be created using a layout editor (in this case Cadence).

```
11 P 4 40 0 240 0 240 600 40 600
16 P 4 100 260 180 260 180 340 100 340
17 P 4 0 200 1000 200 1000 400 0 400
18 P 4 820 260 900 260 900 340 820 340
19 P 4 760 0 960 0 960 600 760 600
T node1 500 300
```

The mask description file describes the layout in terms of 2D boxes as shown in figure 4.1. The first character in each line defines the layer number, and is followed by P or B to specify a polygon or a box. A list of coordinates is given, preceded by a figure specifying the number of vertices if the data is in the form of a polygon. The text on the layout is included, with coordinates specifying its position.

The control file contains a list of instructions regarding the type of representation and format required, and parameters relating to physical and electrical properties of

each layer. The control file can be divided into six parts, with the following functions:

1. define parameters

2. read in mask information and assign properties to layers

3. create non–mask layers

4. assign electrical characteristics

5. create 3D representation

6. specify output

Each of these functions is now described in detail, along with an example of syntax taken from the control file which was used to create 3D data from the example mask description file.

Define Parameters. Parameters relating to layer thickness, step coverage, dielectric constant in the case of dielectric materials and resistivity in the case of conducting materials are defined. These are used to assign properties to layers as they are read from the mask description file. It is not essential to use parameters, since absolute values may be assigned directly to layer properties, but the use of parameters ensures readability of the control file, and minimises the risk of incorrect data entry.

```
#poly_thickness = 80
#poly_step = 40
#poly_rho = 0.5
#dielectric1_thickness = 100
#dielectric1_step = 50
#dielectric1_diel = 3.9
#metal1_thickness = 80
#metal1_step = 40
#metal1_rho = 0.01
```

Read in mask information and assign properties to layers. The mask description file from which the mask data is to be read is defined. Each 2D mask layer, which is identified by a number in the mask description file, is assigned a name, a thickness (-t),

48

a step–coverage (-s), a type (-T) and an electrical characteristic (-v). The type field will be either C if the layer is to be treated as a conductor, D for a dielectric or V for a contact or via mask. The electrical characteristic will either be the material's resistivity or its dielectric constant. The following syntax takes data from file example4out, and reads in and assigns characteristics to layers poly, contact, metal1, via and metal2.

```
load ( 'example4out' ,
11 , poly -t #poly_thickness -s #poly_step -T C -v
#poly_rho ,

16 , contact -t #dielectric1_thickness -s
#dielectric1_step -T V -v #dielectric1_diel,

17 , metal1 -t #metal1_thickness -s #metal1_step
-T C -v #metal_rho ,

18 , via -t #dielectric2_thickness -s
#dielectric2_step -T V -v #dielectric2_diel ,

19 , metal2 -t #metal1_thickness -s #metal1_step
-T C -v #metal_rho )
```

Create non-mask layers. Not all 3D layers to be created are defined directly in the mask description file. These layers can be defined by way of boolean polygon operations on mask layers and on the layer substrate, which is created automatically by 3DTOP and encompasses the area of all mask layers read in to the program. Layer properties are defined as in the previous section. The following syntax defines the layers contact_dielectric, via_dielectric and passivation using boolean operations on the substrate layer and the contact and via masks.

```
contact_dielectric -t #dielectric1_thickness -s
#dielectric1_step -T D -v #dielectric1_diel =
substrate andnot contact

via_dielectric -t #dielectric2_thickness -s
#dielectric2_step -T D -v #dielectric2_diel =
substrate andnot via

passivation -t #dielectric3_thickness -s
#dielectric3_step -T D -v #dielectric3_diel =
substrate
```

Assign electrical characteristics. Electrical connectivity of layers is defined using the connect statement. Layers which will be electrically connected when they overlap are specified. For example, poly, contact and metal1 should be connected when all three coincide. In the following syntax, these layers are referred to by their numbers, 11,16 and 17, rather than by their names.

```
connect ( 11 , 16 , 17 )
```

Absolute voltage values may be assigned to nodes by using the set command followed by the electrical node name as it appears in the layout and the appropriate voltage value. An example of 3DTOP's handling of electrical nodes can be found in section 4.5.

```
set ( node1 , 5 )
```

Create 3D representation. One of three commands may be used depending on the representation required, and these are shown in the following example of syntax. The first two commands are commented out here using the $ character, since only one type of data may be created at any one time. Createlayers produces planar or conformal 3D shapes, createslopes produces a semi–conformal boundary representation and createboundaries produces a planar or conformal boundary representation. All of the create commands are followed by a list of layers in the order in which they are to be created, so some basic knowledge of the process is required. The createboundaries and createslopes commands are followed by the name of

50

the FastCap list file in which the FastCap data files produced by 3DTOP and containing data describing each created layer will be listed. Numbers specifying the required scaling factor and degree of discretisation are also included.

```
$createlayers ( substrate ,
$createboundaries "eg3bound" 0 0 ( substrate ,
createslopes "eg4slopebound" 0 0 ( substrate ,
poly ,
contact ,
contact_dielectric ,
metal1 ,
via ,
via_dielectric ,
metal2 ,
passivation )
```

If a planar representation is required, the user must produce extra layers which are the boolean *not* of the mask layers. This is easily achieved in the **create non–mask layers** section of the control file. These layers should be included in the list of layers to be created. If a 3D block format is required, these extra layers should be created as if they were dielectrics. In a boundary format, they should be created as dielectrics with zero step–size, but should not be included in the output as this would lead to duplicated boundaries.

Specify output. The command `povprint` produces input data for POV–Ray, `rprint` produces input data for Raphael, and `printps` produces a postcript file. In each case, the name of the output file must be given, along with the layers to be written to it. Data for use with FastCap is automatically produced as the program runs if the `createboundaries` or `createslopes` commands are used. The two commands in the following syntax illustrate the creation of data describing the layers `poly`, `metal1` and `metal2` for use with POV–Ray and Raphael respectively.

```
povprint ( "example3pov" , poly,metal1,metal2)
rprint ( "example3raph" , poly,metal1,metal2)
```

4.4 Creation of Conformal 3D Representations

In this section, concepts which are relevant to the creation of all three types of 3D representation are presented, along with the algorithm which describes the creation of conformal 3D data. The following sections contain detailed descriptions of the creation of block and boundary data, along with simple examples to show the creation of successive layers, and a more complex example to demonstrate fully 3DTOP's capabilities. The algorithm used to create semi–conformal data is presented in section 4.5.

4.4.1 Manipulation of Data in Two Dimensions

3DTOP is primarily intended to be used to create 3D representations of ICs in which the underlying topography has an effect on succeeding layers. Since this involves coverage of steps by layers of a finite thickness, data must be manipulated in the x and y directions as well as in the z direction. This manipulation of data in the horizontal plane is achieved using a set of polygon operations based on a scanline algorithm developed by Lauther [69]. The development and C++ coding of these algorithms as used in the 3DTOP software was carried out by Dr Gerard Allan of the University of Edinburgh. These 2D polygon manipulation algorithms also form the basis of the successful EYES tool for measuring the defect sensitivity of IC layout [70, 71]. Specifically, the operations used are *bloat*, which increases the dimensions of a polygon by a given amount, and the boolean operators *and, andnot* and *or*.

4.4.2 Manipulation of Data in Three Dimensions

Now that the manipulation of data in the horizontal plane has been described, 3D concepts will be introduced. An important concept developed during this work and used in the creation of 3D representations is the *topsurface*. This is a description of the uppermost surface of the 3D representation, which is stored as a list of planes and is

52
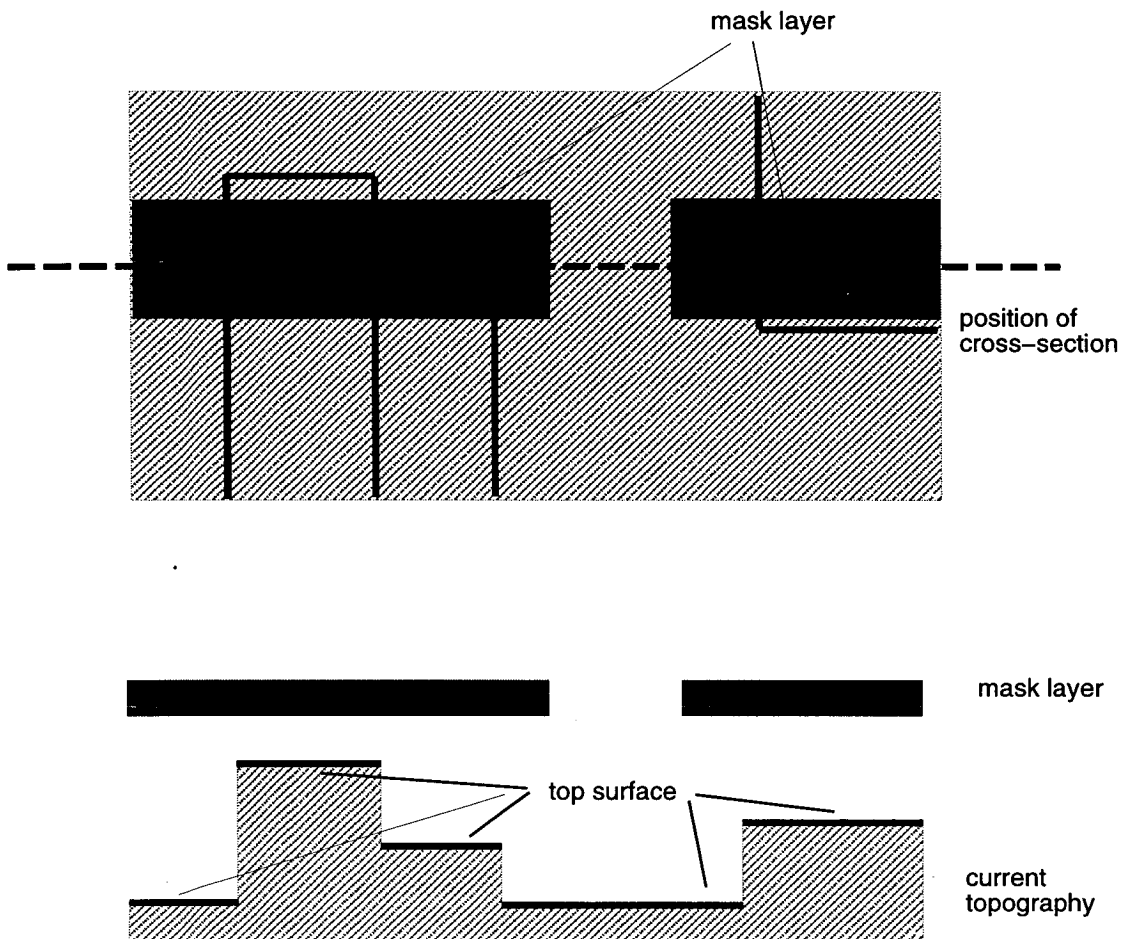
Figure 4.5: Current topography and mask layer.

updated each time a 3D layer is created. These planes contain the height information required to build up the 3D representation. The algorithm which is central to the creation of the conformal 3D representation, and which also forms the basis of creation of the semi–conformal 3D representation, is the *bloat* and *and* algorithm, which is described with the help of figures 4.5 to 4.8. Each of these figures shows both a plan view and a cross-section of a small piece of IC layout, along with the mask layer whose 3D representation is being created.

In figure 4.5, the mask layer is shown with a finite thickness, along with the current 3D topography of the layout. The *top–surface* is indicated by the thick black line.
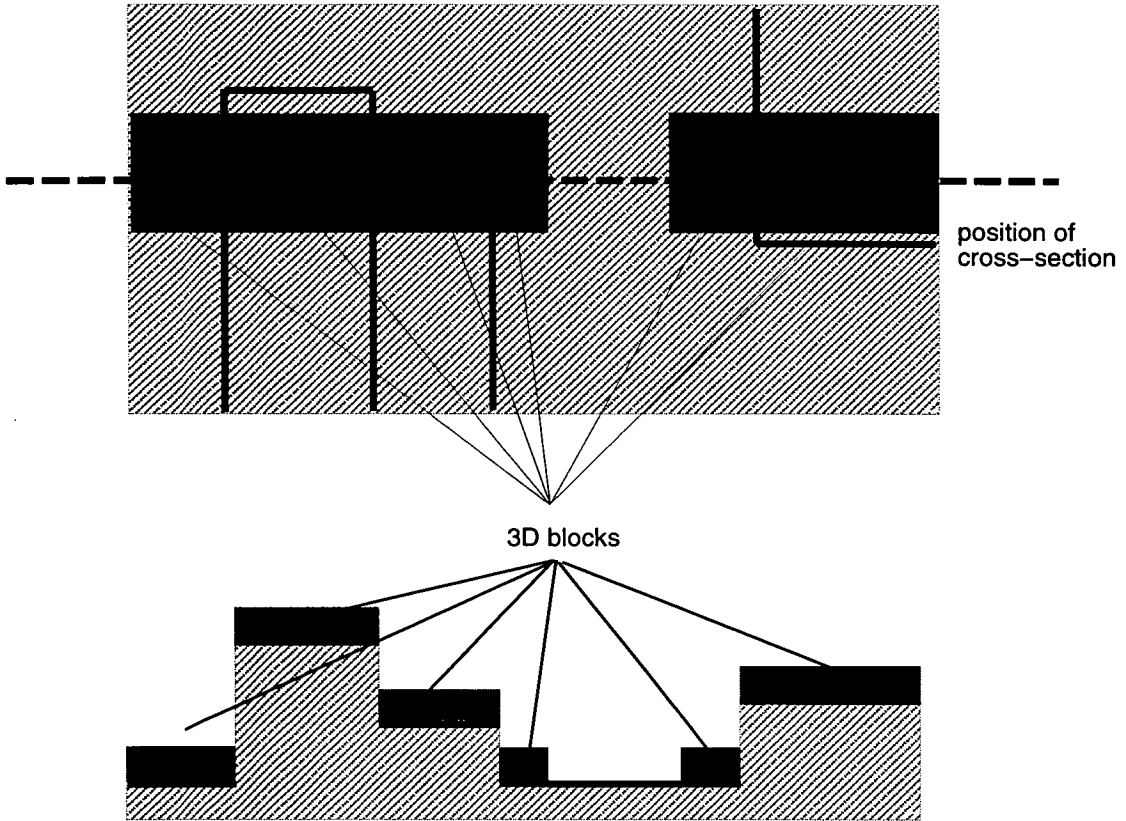
Figure 4.6: Creation of 3D blocks.

Figure 4.6 shows the mask layer being *and*ed with the top surface to create 3D blocks, whose thickness is determined by the user–defined parameter in the control file and whose height is determined by the height of the top surface. This produces a discontinuous 3D layer.

position of
cross–section

creating steps
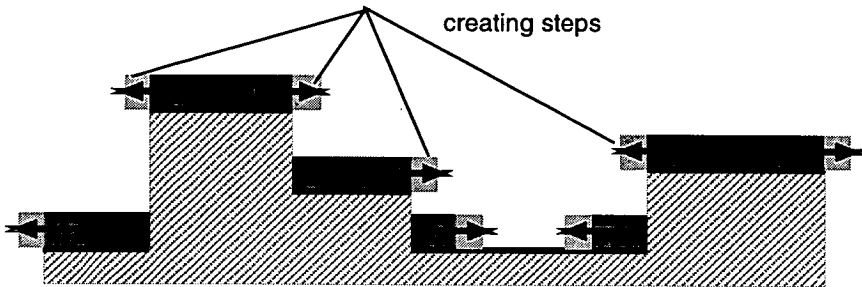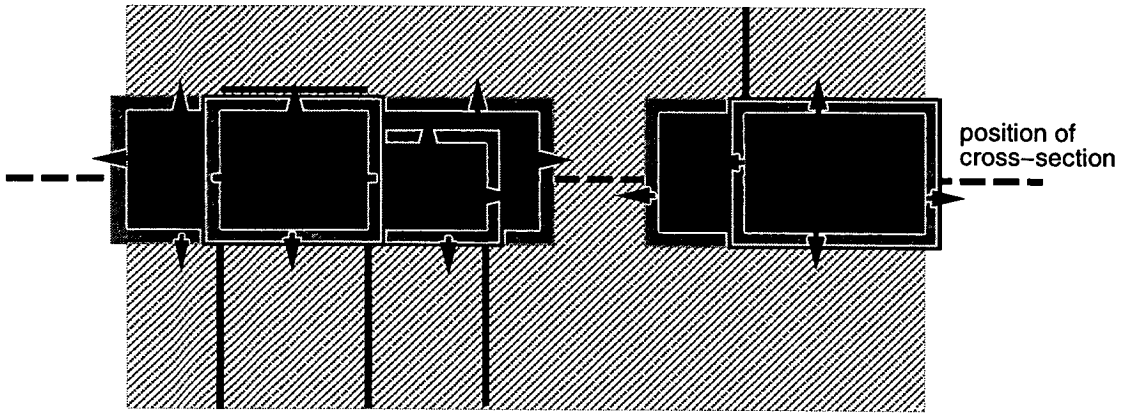
Figure 4.7: Creation of steps.

The next stage is to create steps to link the 3D blocks and create a continuous 3D
layer. Each group of blocks at a particular height is taken in order of increasing height,
and bloated by the user–defined step–size parameter as shown in figure 4.7. An *and* is
then performed on each bloated layer with any blocks or steps beneath it, to produce a
new step. The base height and the thickness of the step are determined by the blocks
and steps involved in the *and* operation.
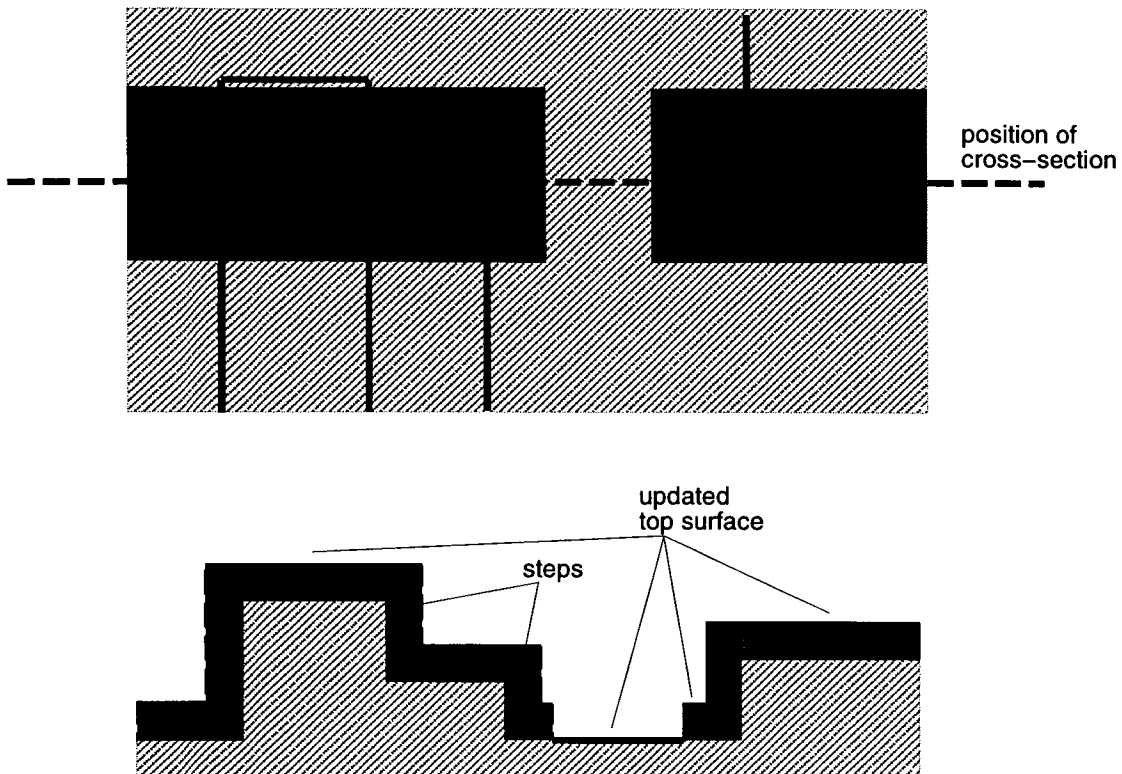
Figure 4.8: Newly created 3D layer and updated top surface.

Finally the top surface is updated to account for the newly created layer, as shown in figure 4.8.

4.4.3 Block Format

Data created in the 3D block format can be used with both TMA's Raphael software and with the ray tracer POV–Ray. In this section the required input formats for Raphael and POV–Ray will be described. A simple example is used to illustrate creation of the data, and a more complex example is used to fully demonstrate 3DTOP's capabilities. This more complex example layout is used to demonstrate creation of data for Raphael in order to produce a capacitance matrix, and for POV–Ray for purposes of visualisation.

4.4.4 Raphael and POV–Ray

Raphael can take various structures as input such as cylinders, spheres and blocks, but the 3DTOP–Raphael interface is restricted to one structure, `poly3d`. This 3D block is specified by means of a list of x and y coordinates which define the base of the block, a vector specifying the origin of the local coordinate system used to define the block's base, and the height of the block. 3DTOP also produces data to fill the fields name, which contains the electrical node name of the block, and either `volt` or `diel`, defining the voltage on the node or its dielectric constant depending on whether the block forms part of a conductor or a dielectric layer. In addition to describing each 3D block, 3DTOP automatically produces further data required by Raphael, i.e. a `window3d` statement describing the extent and dielectric constant of the simulation window, and an `options` statement containing an arbitrary number of grid points, which may later be modified by the user, and an instruction to produce a capacitance matrix. Part of the Raphael input file created from the layout shown in figure 4.1 follows. `Poly3d` statements describing the substrate and polysilicon layers are shown.

```
$RC3 Input file for layer example4raph

poly3d name=substrate; +
coord="1000,0;1000,600;0,600;0,0;" +
v1=0,0,200; height=80; volt=1;

$ layer = poly
poly3d name=node1; +
coord="240,0;240,600;40,600;40,0;" +
v1=0,0,200; height=80; volt=1;

window3d v1=0,0,0; v2=1000,600,460; diel=1;
options set_grid=10000;
capacitance
```

POV–Ray [68] can also take data in many formats, but the method chosen to interface with 3DTOP is to describe data in terms of 2D triangles which form the faces of 3D blocks. This was chosen as a method which could be used with all types of 3D data representation created by 3DTOP, since any block or boundary that 3DTOP produces

may be represented by triangular faces. 3DTOP automatically defines the location and viewing angle of the camera, and defines a light source in an appropriate position. The surface colour and texture of triangles describing each layer is also defined automatically for commonly used layers. A POV–Ray file describing the 3D polysilicon layer created from the layout shown in figure 4.1 follows.

```
#include "colors.inc"
#include "shapes.inc"
#include "textures.inc"
camera
location <500, 750, -600>
look_at <500, 0, 300>

//current layer is poly
triangle  <40,200,0>,<40,280,0>,<240,200,0>
texture ICpoly
triangle  <40,280,0>,<240,280,0>,<240,200,0>
texture ICpoly
triangle  <40,200,0>,<40,200,600>,<240,200,600>
texture ICpoly
triangle  <40,280,0>,<40,280,600>,<240,280,600>
texture ICpoly
triangle  <40,200,600>,<40,280,600>,<240,200,600>
texture ICpoly
triangle  <40,280,600>,<240,280,600>,<240,200,600>
texture ICpoly
triangle  <40,200,0>,<240,200,600>,<240,200,0>
texture ICpoly
triangle  <40,280,0>,<240,280,600>,<240,280,0>
texture ICpoly
triangle  <240,200,600>,<240,280,600>,<240,200,0>
texture ICpoly
triangle  <240,280,600>,<240,280,0>,<240,200,0>
texture ICpoly
light_source  <500, 375, 75 > color red 1 green 1
blue 1
area_light <3000,0,0>,<0,0,3000>,5,5
adaptive 1
jitter

background  color White
```

4.4.5 Production of Data in Block Format

3D blocks are created using the *bloat* and *and* algorithm described in section 4.4. Contacts and vias are not explicitly created – rather, dielectrics are modified in the *create non mask layers* section of the control file (see section 4.3), such that they have gaps where the contacts or vias would be. The *bloat* and *and* algorithm causes these gaps to be filled by the following layer to an extent determined by the layer thicknesses and step–coverages. Figures 4.9 to 4.12 show the creation of the 3D block representation of the substrate, polysilicon, contact dielectric and metal1 of the layout shown in figure 4.1. The contact dielectric in figure 4.11 is created using a 2D mask layer which is the result of a boolean *andnot* on the substrate and contact mask layers, so that the contact is already 'etched' into the dielectric. In this case, the metal1 layer shown in figure 4.12 completely fills this contact hole due to the user–defined values of layer thickness and step coverage. A pseudo–code description of the algorithm used to create the 3D block representation can be found in Appendix A.

4.4.6 Example – Conformal 3D Data in Block Format

The layout used to fully demonstrate the creation of 3D blocks for Raphael and POV–Ray is shown in figure 4.13. This layout has been chosen since it includes various combinations of Manhatten and $45°$ interconnect tracks. The ray traced image created using the POV–Ray input file is shown in figure 4.14, with dielectrics removed for clarity. The Raphael file was used to create both a capacitance matrix and a 3D image of the layout. The capacitance matrix is shown in table 4.1. The capacitance values on the diagonal of the matrix show the total capacitance on each individual node.
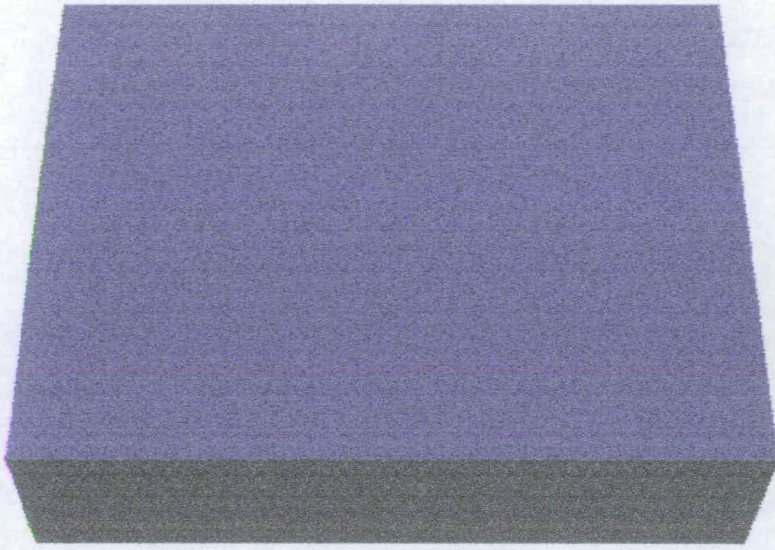
Figure 4.9: 3D block description of substrate layer, created using 3DTOP and POV–Ray.
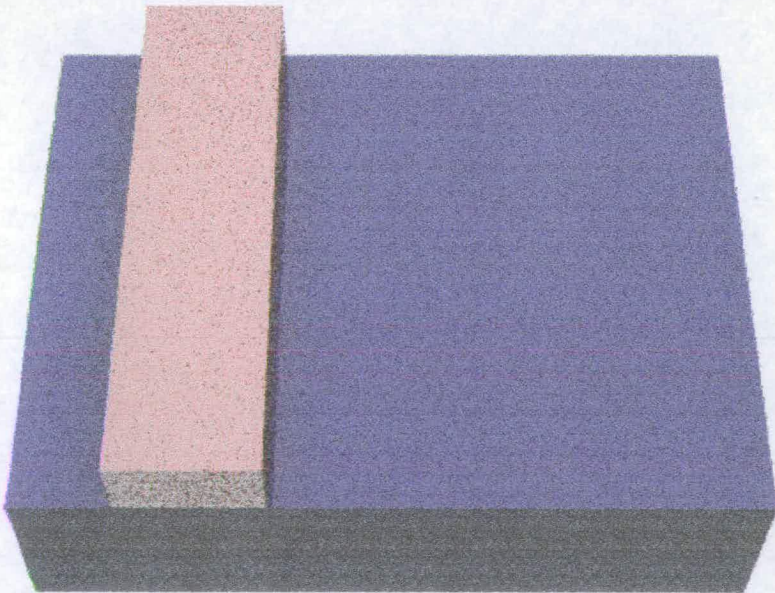
Figure 4.10: Polysilicon layer added.
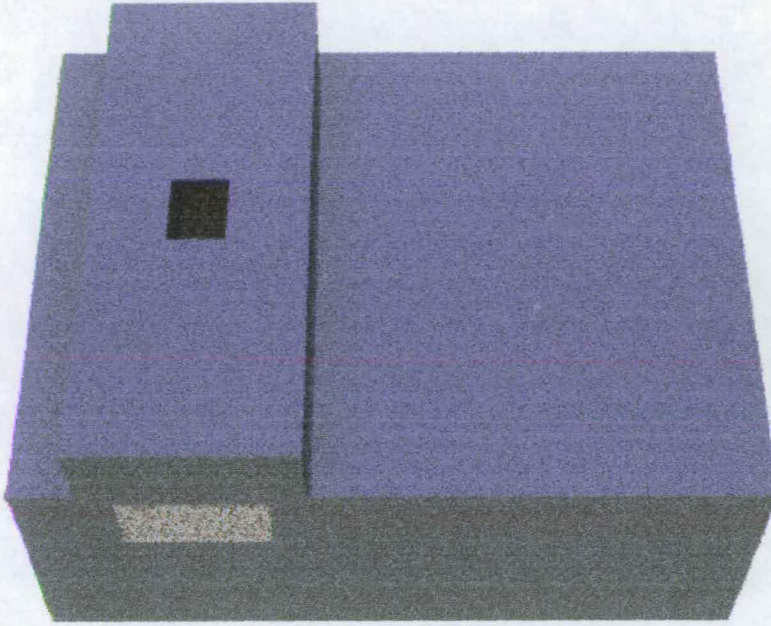
Figure 4.11: Contact dielectric layer added.
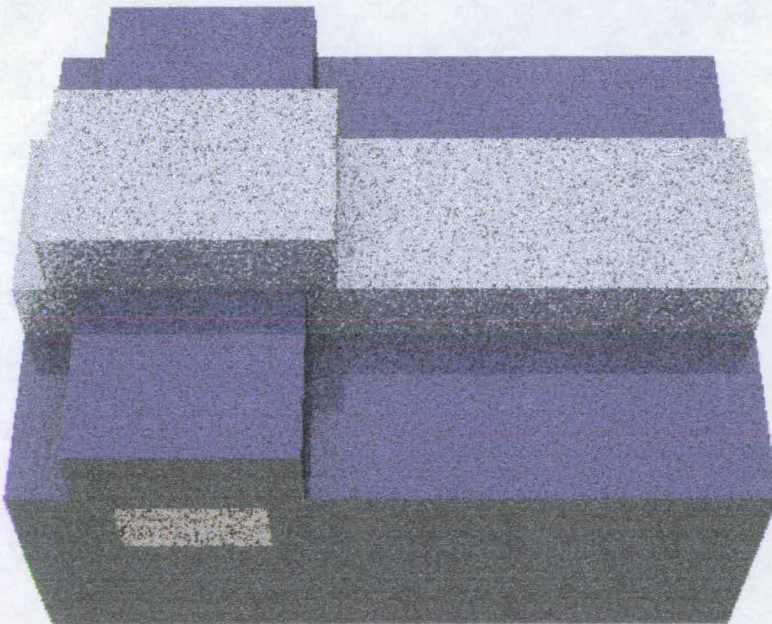
Figure 4.12: Metal1 layer added.
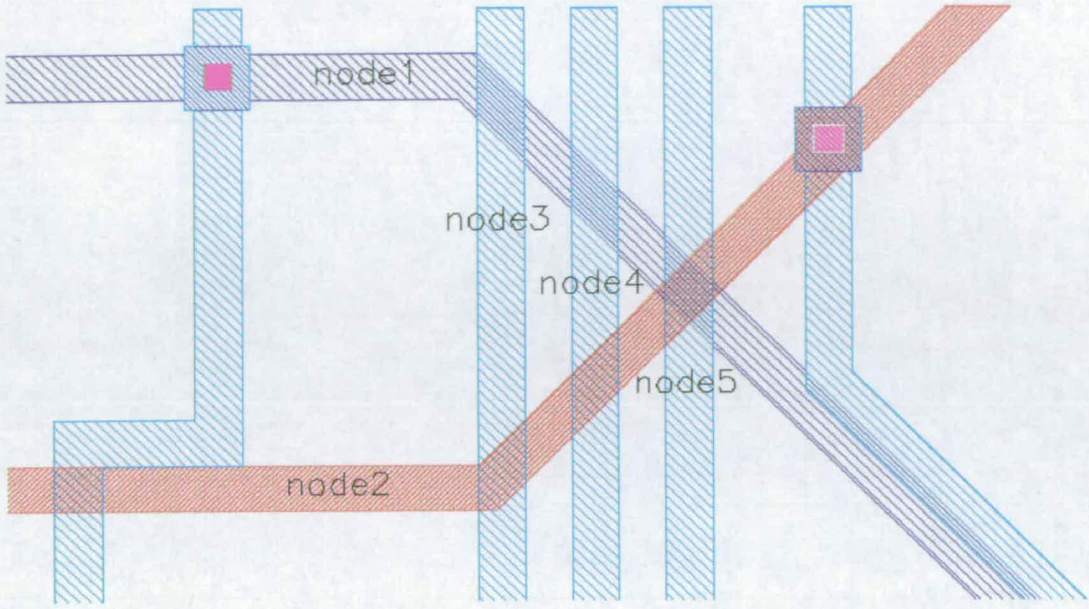
Figure 4.13: Simple layout, showing electrical node names.
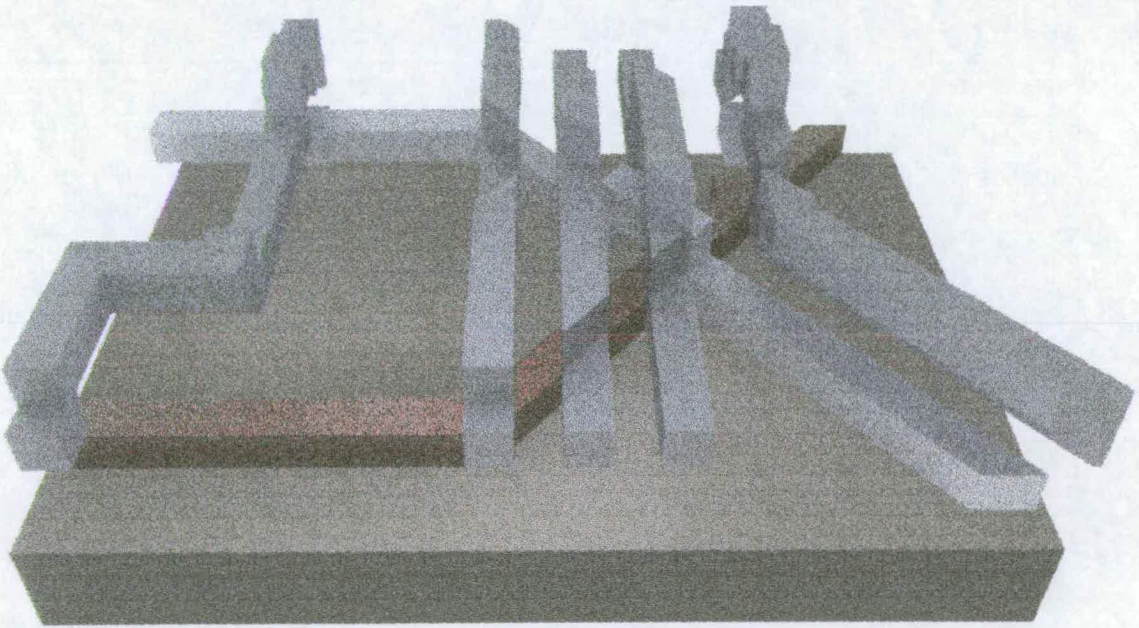
Figure 4.14: 3D block description of layout shown in Figure 3.13, created using 3DTOP and POV–Ray.

	node1	node2	node3	node4	node5
node1	251	118	50	39	44
node2	118	193	25	18	32
node3	50	25	111	33	3
node4	39	18	33	124	34
node5	44	32	3	34	113

Table 4.1: Capacitance matrix showing capacitances simulated using Raphael and 3D block description created from simple layout (all capacitances in nF).

4.4.7 Boundary Format

Data created in boundary format can be used with both the capacitance simulator FastCap and the ray tracer POV–Ray. In this section, the required input format for FastCap is described (the POV–Ray input format is described in section 4.4.4). Boundary format data can be used in conjunction with planar, conformal and semi-conformal 3D representations of layout. The creation of the conformal representation is described in this section, and is followed by an example. The creation of semi–conformal data is described in section 4.5.

4.4.8 FastCap

FastCap takes data in the form of 2D panels, which combine to describe 3D shapes. The panels may be either quadrilateral or triangular, each line of data beginning with either a Q or a T to specify the type of panel. This is followed by the electrical node name or number, and a list of vertices specified in terms of x, y and z. All panels defining the boundary between two specific layers are stored together in one file, and these files describing the inter–layer boundaries are then collected together in a list file. In this list file, the type of each boundary is defined – this may be either C to specify a boundary between a conductor and a dielectric, or D to specify a boundary between dielectrics. In each case, the appropriate dielectric constants are defined, as is the origin of the local coordinate system. In the case of the dielectric boundary, a reference point

is provided which defines the side of the boundary to which the first given dielectric constant applies.

3DTOP automatically produces separate files containing boundaries between conductors and dielectrics, and between dielectric layers. For example, panels forming the boundary between the base of a conducting layer and the dielectric below it will be stored in a different file from those describing the boundary between the top of the conducting layer and the dielectric above it. This allows for the situation in which the dielectrics above and below a conducting layer have different properties. The list file containing appropriate dielectric constants and reference coordinates is also created automatically. 3DTOP allows for basic discretisation of the data since FastCap requires that data be suitably discretised. 3DTOP can therefore be used to produce a complete set of 3D data from a 2D mask description entirely ready for use with FastCap.

The file containing panels describing the boundary between metal1 and the dielectric beneath it for the layout shown in figure 4.1, and the list file created by 3DTOP follow.

metal1–dielectric boundary file

```
0 metal1lower
Q 2 100E-8 200E-8 380E-8 0E-8 200E-8 380E-8 0E-8
400E-8 380E-8 100E-8 400E-8 380E-8
Q 2 180E-8 340E-8 380E-8 100E-8 340E-8 380E-8
100E-8 400E-8 380E-8 180E-8 400E-8 380E-8
Q 2 180E-8 200E-8 380E-8 100E-8 200E-8 380E-8
100E-8 260E-8 380E-8 180E-8 260E-8 380E-8
Q 2 290E-8 200E-8 380E-8 180E-8 200E-8 380E-8
180E-8 400E-8 380E-8 290E-8 400E-8 380E-8
Q 2 1000E-8 200E-8 300E-8 290E-8 200E-8 300E-8
290E-8 400E-8 300E-8 1000E-8 400E-8 300E-8
Q 2 290E-8 200E-8 300E-8 290E-8 400E-8 300E-8
290E-8 400E-8 380E-8 290E-8 200E-8 380E-8
Q 2 290E-8 200E-8 300E-8 290E-8 400E-8 300E-8
290E-8 400E-8 380E-8 290E-8 200E-8 380E-8
Q 2 290E-8 200E-8 300E-8 290E-8 400E-8 300E-8
290E-8 400E-8 380E-8 290E-8 200E-8 380E-8
```

list file

```
D substrate 1 3.9 0 0 0 500 300 0
C polylower 1 0 0 0
C polyupper 3.9 0 0 0
C contact 3.9 0 0 0
D contact_dielectric 3.9 4.1 0 0 0 500 300 0
C metal1lower 3.9 0 0 0
C metal1upper 4.1 0 0 0
C via 4.1 0 0 0
D via_dielectric 4.1 4 0 0 0 500 300 0
C metal2lower 4.1 0 0 0
C metal2upper 4 0 0 0
D passivation 4 1 0 0 0 500 300 0
```

4.4.9 Production of Data in Boundary Format

The algorithm used in creation of boundaries has similarities to that used to create 3D blocks in that it uses the *bloat* and *and* method described in section 4.4. However, since boundaries are being created rather than 3D blocks a slightly different approach is needed. It is important not to duplicate boundaries, since this is unacceptable to the simulator. A 3D block representation creates a boundary between layers more than once. For example, in the situation where a conducting track crosses a layer of dielectric, the boundary between the two will be represented by both the underside of the conductor and the top of the dielectric. In the boundary creation algorithm, the boundary between the two layers should be defined only once. For this reason, different types of layer, ie conductors, vias and dielectrics, are treated differently by the algorithm, in contrast to the creation of 3D blocks, where only conductors and dielectrics are explicitly created, and the algorithm used in each case is the same. Similarly, it is important not to create boundaries inside a node, since again this is an incorrect data representation for the simulator.

The algorithm will be explained with the use of a simple example, then a more complex example will be used to demonstrate 3DTOP's capabilities in the following section. The simple layout used is shown in Figure 4.1. Figure 4.15 shows the

65
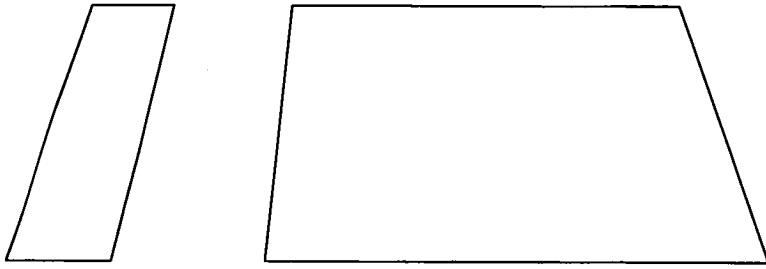
Figure 4.15: Boundary description of substrate layer, created using 3DTOP and FastCap.
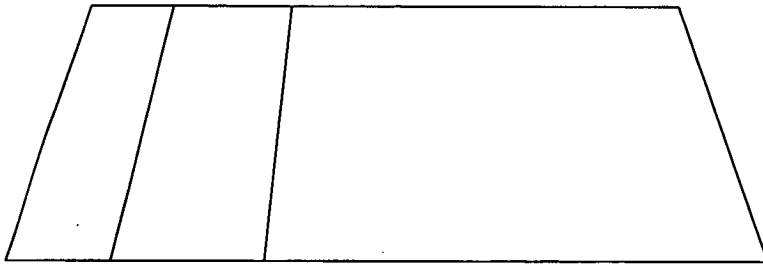
Figure 4.16: Lower polysilicon boundary added.
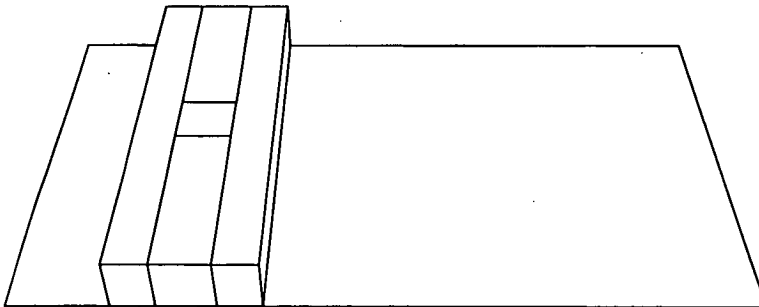
Figure 4.17: Upper polysilicon boundary added.
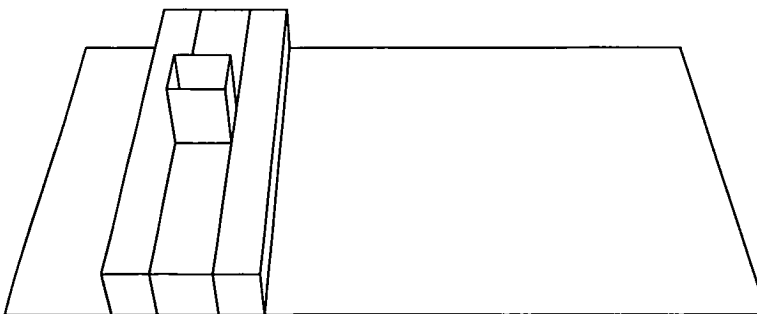
Figure 4.18: Contact added.
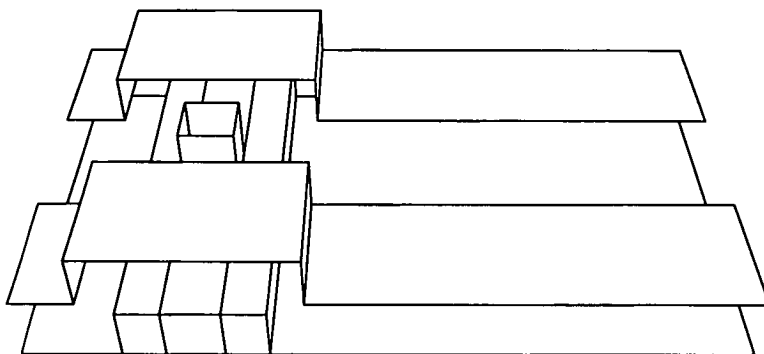
Figure 4.19: Dielectric plane added.
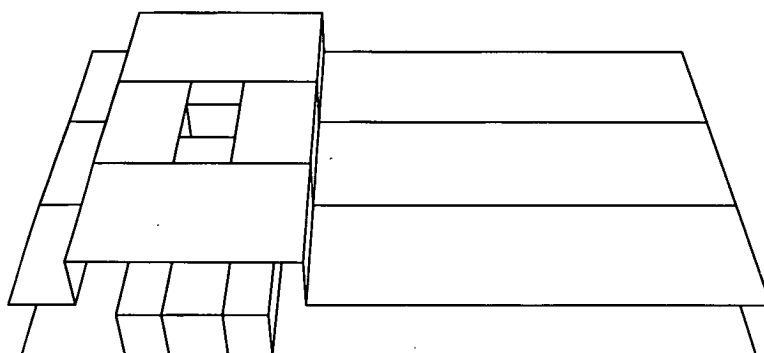
Figure 4.20: Lower metal1 boundary added.
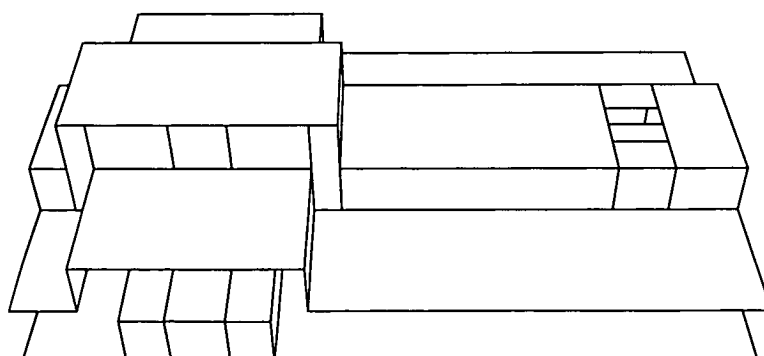
Figure 4.21: Upper metal1 boundary added.

initial boundary created, the substrate. Notice that there is a gap in this boundary which corresponds to the position the first conducting layer will occupy. The boundary between dielectric and conductor will be created as part of the conductor. Figure 4.16 shows the creation of the lower polysilicon boundary. Next, the upper polysilicon boundary is created using the *bloat* and *and* method, and boundaries are created between the polysilicon and the following dielectric. This is shown in Figure 4.17. This boundary has a gap where the next contact is positioned, so as not to create boundaries inside the conducting area. The contact between the polysilicon and metal1 is created, as shown in Figure 4.18. Only the side boundaries are created in this case, again to avoid creating boundaries inside the conductor. A dielectric interface is now added, as shown in Figure 4.19. Note that this again has a gap where the next conductor, metal1, is positioned. Figures 4.20 and 4.21 show the creation of the lower and upper metal1 boundaries, with gaps where previous and following contacts are positioned.

A pseudo-code description of the algorithm is included in Appendix A.

4.4.10   Example – Conformal 3D Data in Boundary Format

The example used to illustrate the creation of conformal boundaries is the same as that used in section 4.4.6. The 2D layout is shown in figure 4.13. Figure 4.22 shows a boundary representation of the conductors created from the example layout using 3DTOP, with the dielectric interface boundaries removed for clarity. The final dielectric boundary, the passivation, is shown in figure 4.23. This demonstrates the simple discretisation capability of the algorithm. Using the degree of discretisation shown in figure 4.23, a capacitance matrix was produced, which is shown in table 4.2. Note that the values are comparable to those created by Raphael, shown in table 4.1.
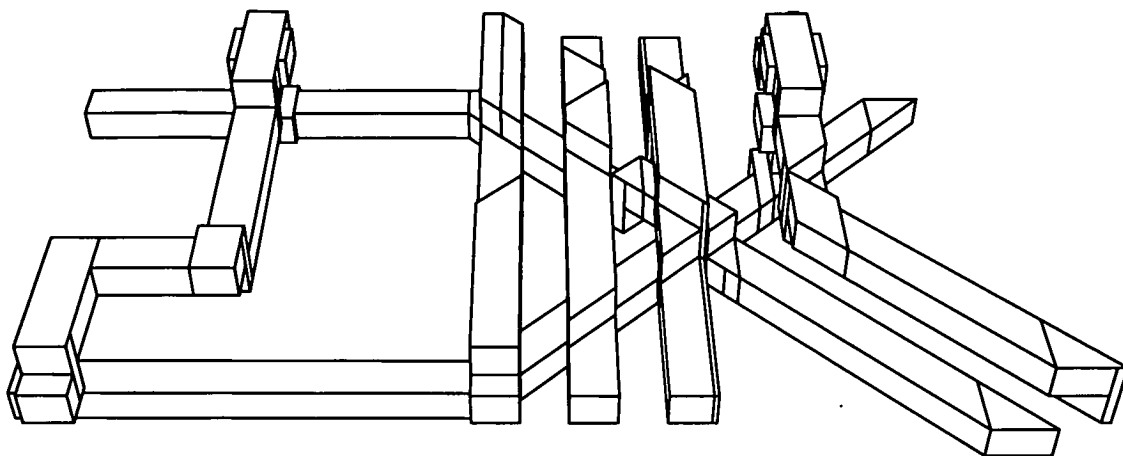
Figure 4.22: Boundary representation of conductors in layout shown in Figure 4.13.
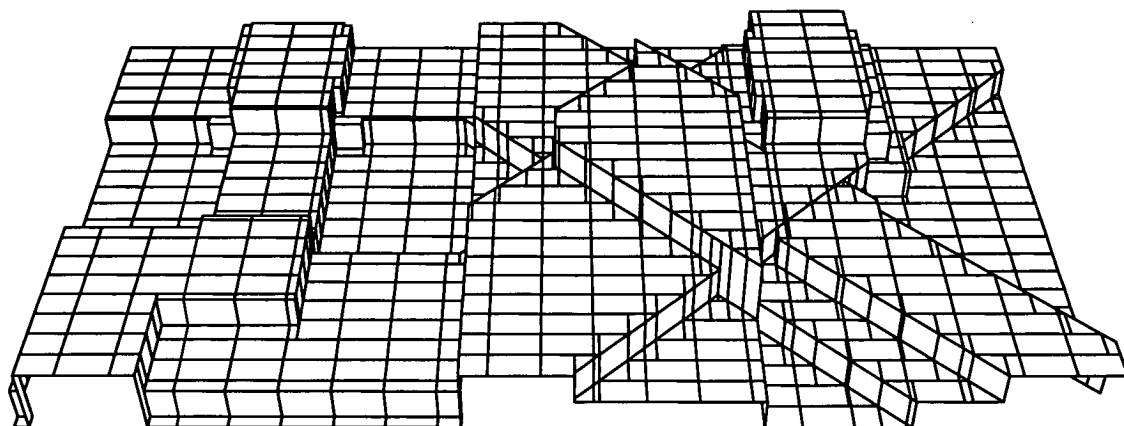
Figure 4.23: Gridded boundary representation of passivation.

	node1	node2	node3	node4	node5
node1	246	119	44	39	44
node2	119	194	24	19	32
node3	44	24	99	28	3
node4	39	19	28	115	29
node5	44	32	3	29	108

Table 4.2: Capacitance matrix showing capacitances simulated using FastCap with 3D boundary description created from simple layout (all capacitances in nF).

4.5 Creation of Semi–Conformal 3D Representations

Not all semiconductor processes result in 3D topography that can be represented using the planar or conformal formats previously described. In response to this, an algorithm has been developed to enable 3DTOP to produce a semi–conformal representation of an IC, allowing a wider range of processes to be represented.

The creation of semi–conformal boundary data is similar in many respects to the creation of conformal boundary data as described previously in this chapter. The data is produced in a format which can be used as input to the 3D capacitance simulator FastCap, so the same restraints apply regarding duplication of boundaries and removal of internal boundaries (see section 4.4.7). A significant difference is that whereas both conformal and planar boundary data are represented by only horizontal and vertical boundaries, semi–conformal boundary data will include some boundaries that are neither horizontal nor vertical. Such data may form parts of the *top surface*, so a means of storing and manipulating it is required.

The data structure which allows this is *Poly3D*, which is a polygon whose vertices are each described by means of x, y and z coordinates. The introduction of this new data structure as part of the top surface leads to the requirement for a method whereby 2–dimensional polygons describing a mask layer can take on the 3–dimensional nature of the underlying top surface. A *3dAND* operation has therefore been written to transfer 3D information from a *Poly3D* to a 2–dimensional polygon contained within it in x and y. The algorithm used to create semi–conformal boundary data will now be outlined with the aid of figures 4.24 to 4.28. There are some similarities with the *bloat* and *and* method described in section 4.4, but there are also significant differences.

70

position of
cross–section

mask layer

dielectric interface

previous layer
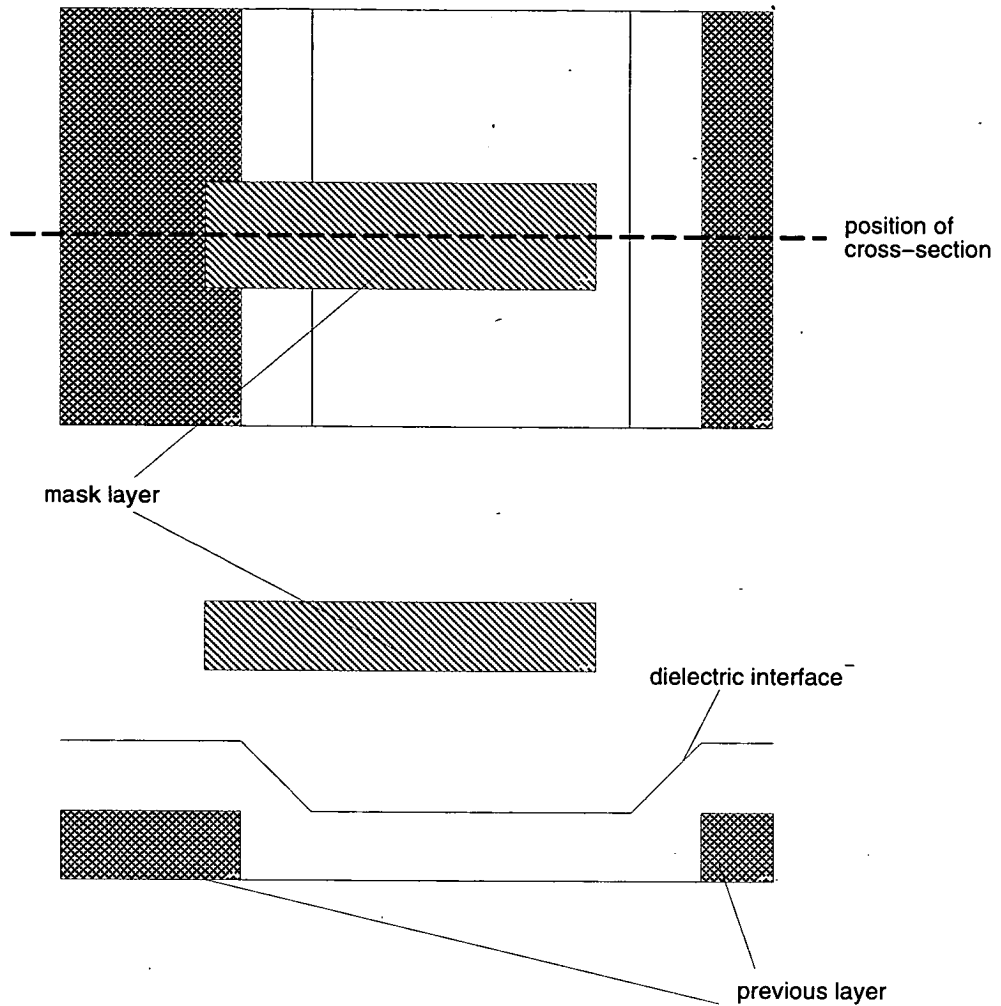
Figure 4.24: Current topography and mask layer.

Figure 4.24 shows a plan view and a corresponding cross–section through a small section of layout. The two conducting layers are shown as solid blocks for clarity, but would actually be represented by sets of 2–dimensional boundaries. The dielectric interface, which also forms the top–surface in this case, is shown as a group of 2D boundaries.
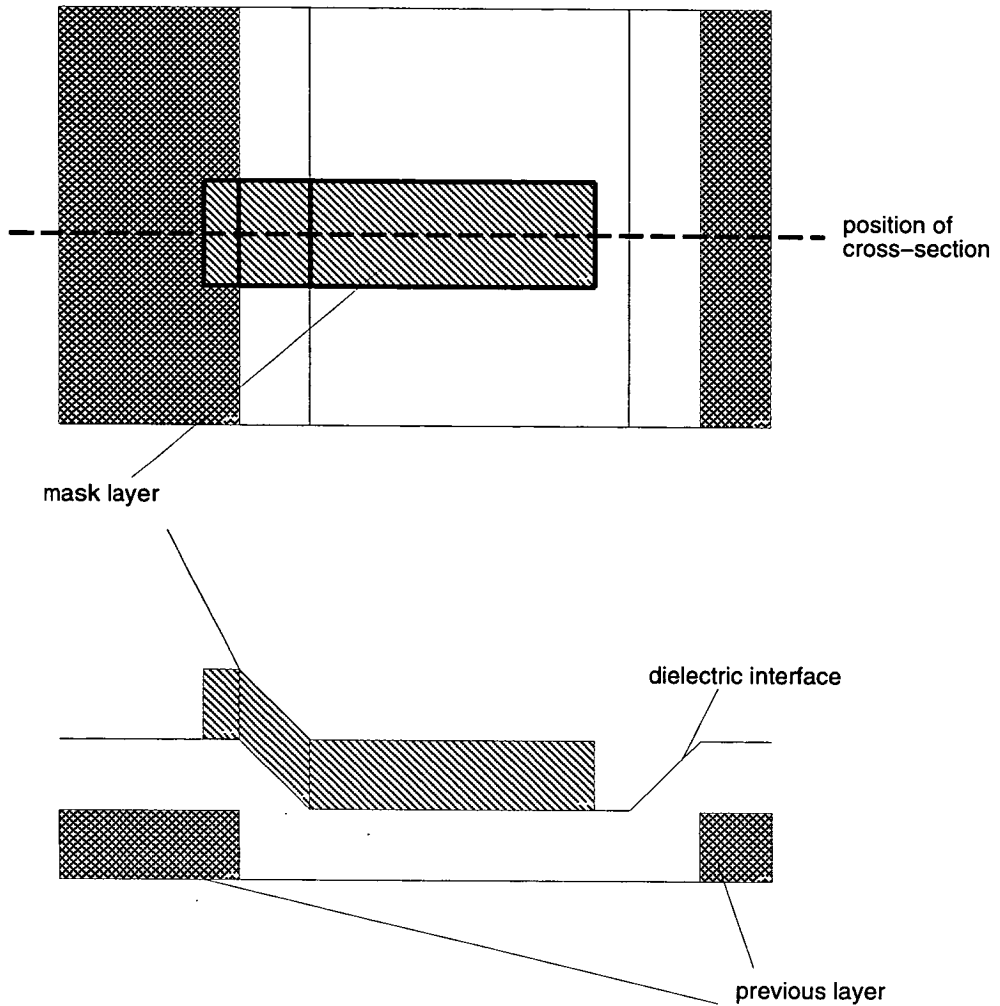
Figure 4.25: Mask layer is 'dropped' onto top–surface.

The mask layer being processed is 'dropped' onto the top–surface, as shown in figure 4.25. This operation divides the mask layer into 3 blocks, all described by a set of *Poly3D*s. Note that there is no need to perform a *bloat* and *and* to create the step, as is the case in conformal data creation, since no vertical steps need be produced. The requirement for the *Poly3d* data structure and the *3dAND* function is demonstrated by the middle block, whose representation must include boundaries which are neither horizontal nor vertical.
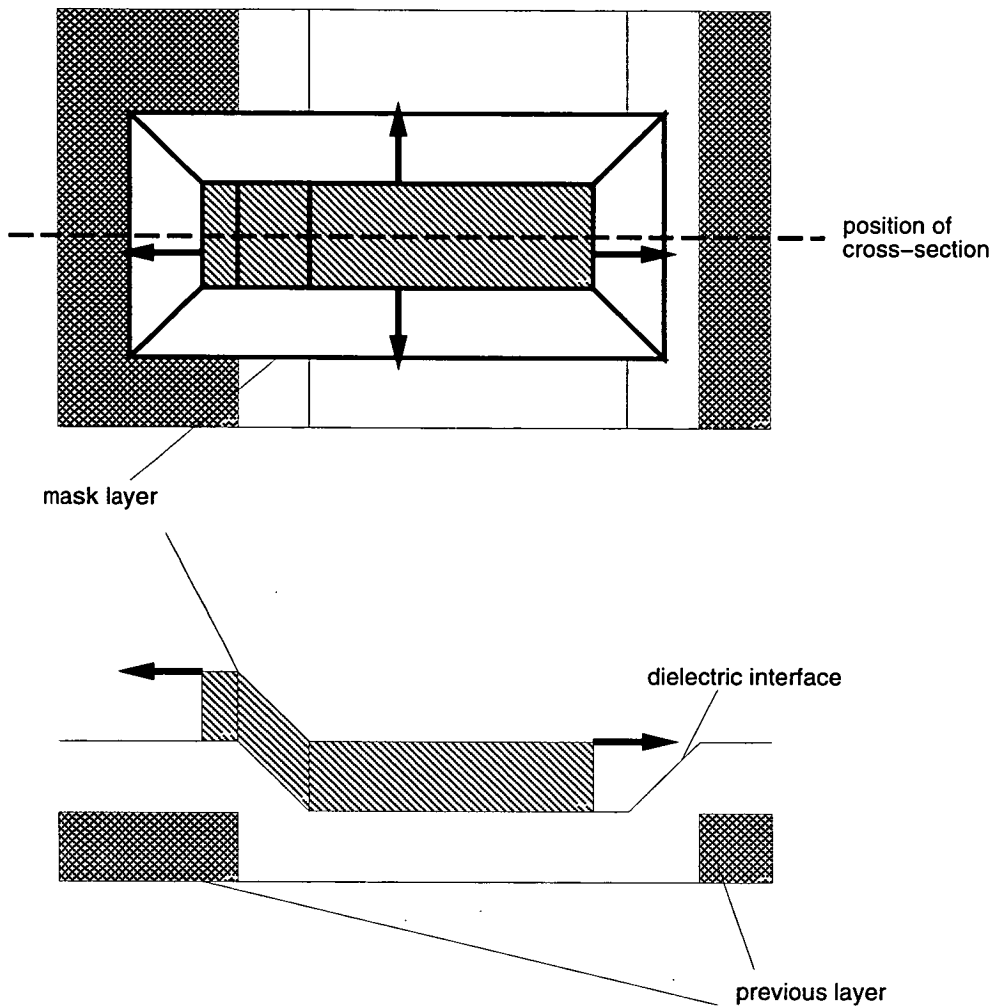
Figure 4.26: Creation of *collar* around conducting–layer polygons.

The semi–conformal description of the conducting layer has now been created. The next step is to create the following top–surface, which will be used to create the next dielectric interface and the next conducting layer. First, temporary polygons are created around the conducting layer, as shown in figure 4.26. The polygon describing the conducting layer is bloated by the user–defined step–size of the following dielectric layer, and the *collar* formed around the conducting–layer polygon is divided into quadrilaterals.

73

poly1

poly2

position of
cross-section

bb

cc

dd

ee

poly3

dielectric_step

B

thickness

A

C

D E
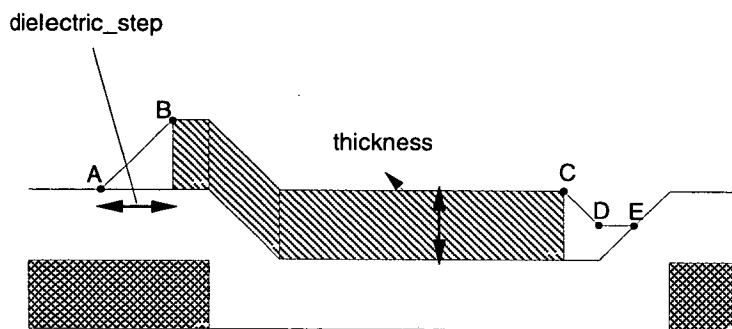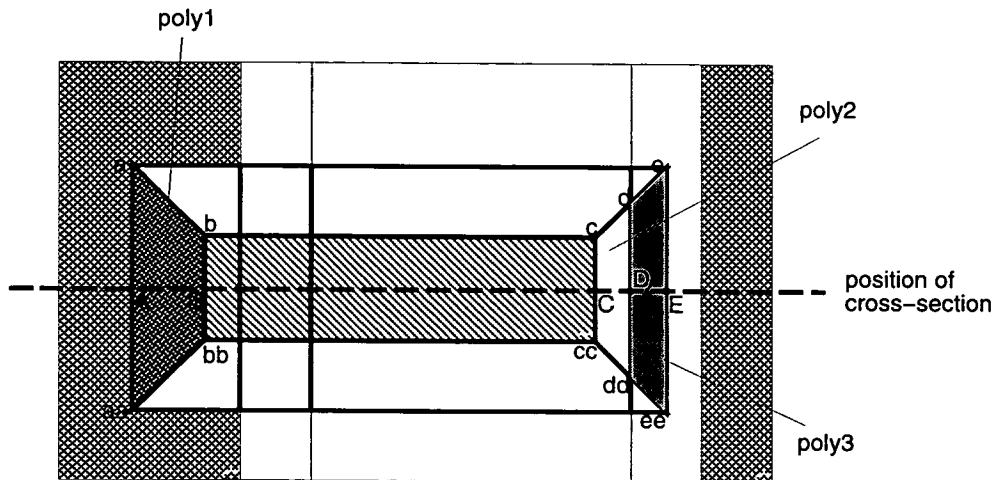
Figure 4.27: Creation of temporary slopes around conductor.

These *collar* polygons are used to create temporary slopes around the conducting layer, which will be used to produce the description of the following top surface. First a *3dAND* is performed on the collar polygons with the existing top–surface. The z–coordinates of the vertices of these *Poly3D*s are then altered depending on their distance from the original polygon describing the conducting layer. For example, if a collar–polygon vertex lies on the edge of the original polygon prior to bloat, its z coordinate will be increased by the thickness of the conducting layer. If it lies a full dielectric–step away from the original polygon, its z value is left unchanged. If it lies somewhere in between these two extremes, its z value will be increased by a percentage of the layer thickness depending on its distance away from the original polygon. The result of this operation is shown in figure 4.27.

In this case, vertices *a* and *aa* in poly3d *poly1*, and vertices *e* and *ee* in poly3d

74
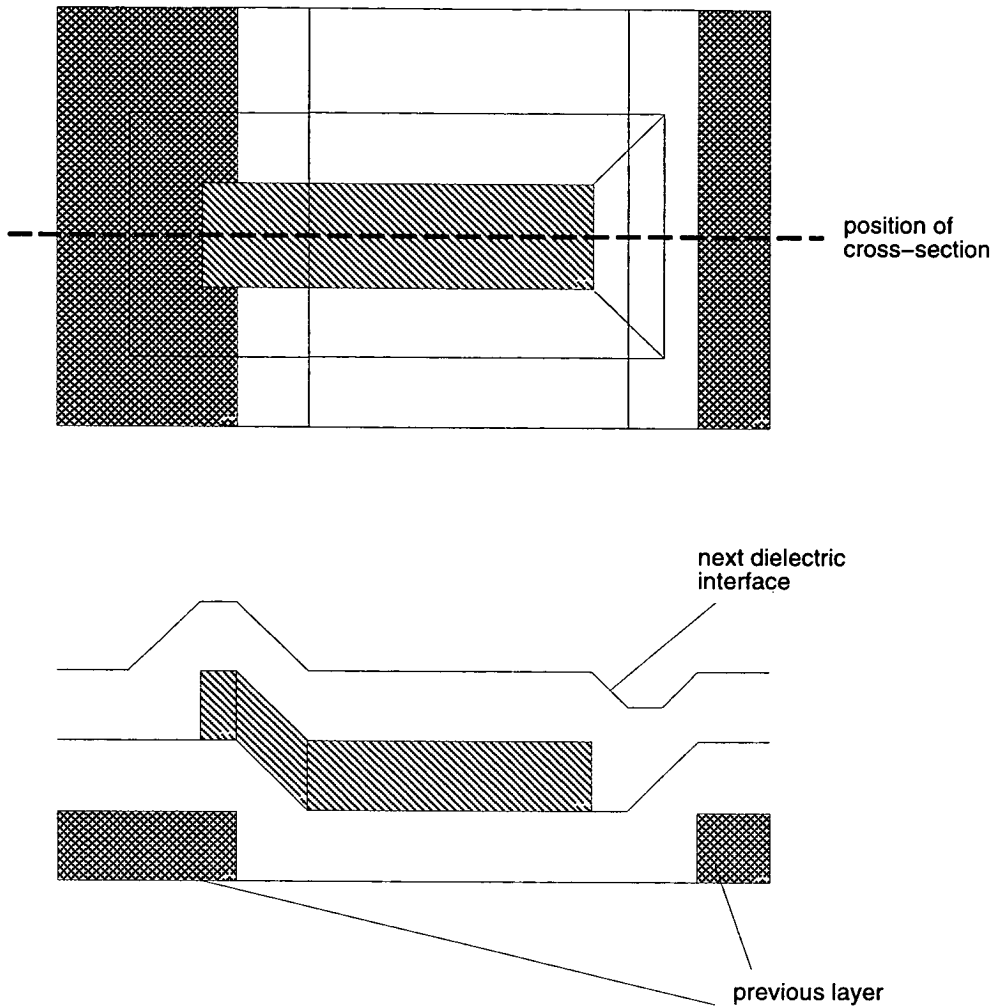
Figure 4.28: Creation of next dielectric interface.

poly3 remain unchanged, since they are a whole dielectric–step away from the original polygon. Vertices *b*, *bb*, *c* and *cc* in poly3ds *poly1* and *poly2* lie on the edge of the original polygon, so their z values are increased by the layer thickness. Vertices *d* and *dd*, which form part of poly3ds *poly2* and *poly3* lie a distance equal to half the dielectric–step away from the original polygon, and therefore have their z values increased by half the layer thickness. Section 4.5.1 contains a more detailed description of this procedure.

Finally, the new top–surface is created using the temporary slopes created in the previous step. The next dielectric layer is produced by simply increasing all the z values of this top surface by the user defined dielectric thickness, as shown in figure 4.28. A pseudo-code description of the algorithm is included in Appendix A.

75
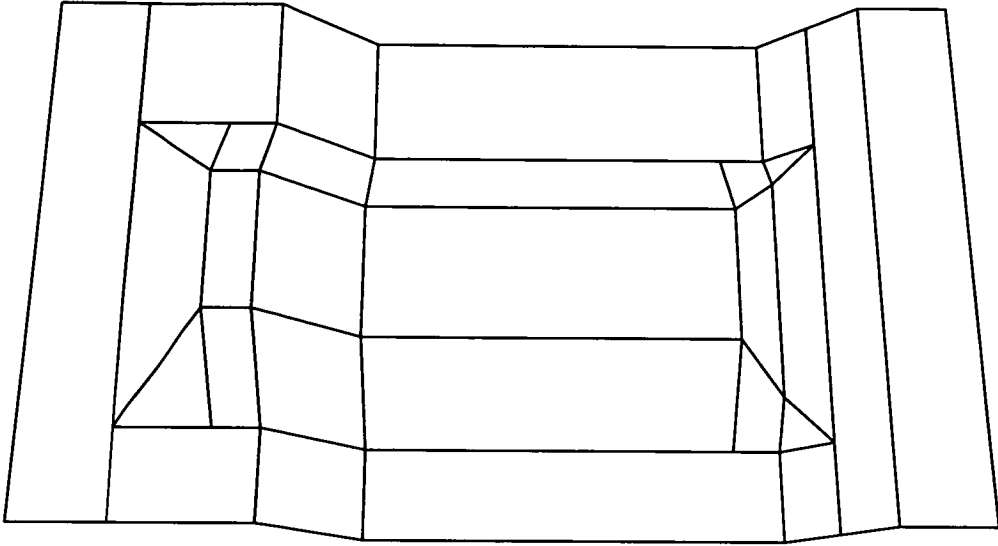
Figure 4.29: Top surface created by FastCap, viewed from above.
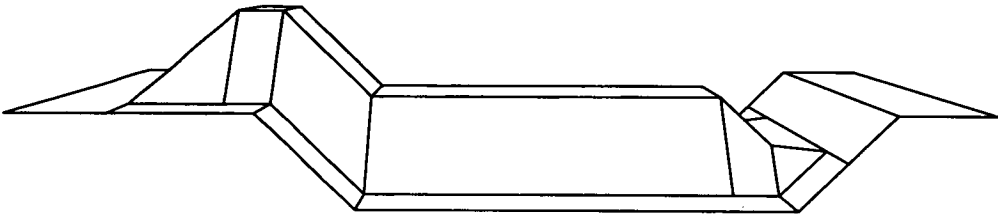
Figure 4.30: Top surface created by FastCap, viewed from the side.

To confirm that 3DTOP's semi–conformal boundary data creation does behave as described in figures 4.24 to 4.28, the layout shown in the plan view of figure 4.24 was used as input to 3DTOP. The output created by 3DTOP was used as input to FastCap, which was used to produce two views of the final top surface shown in figures 4.29 and 4.30.

Comparison of these figures with figure 4.28 confirms that the data created is as expected from the description of the algorithm. Any additional division of panels which has occurred in figures 4.29 and 4.30 is due to a polygon manipulation algorithm within the software which divides larger polygons into quadrialterals and triangles. Extra divisions sometimes occur, but this is not problematic, and is necessary to ensure the robustness of the algorithm.

76

4.5.1   Issues Arising from Creation of Slopes

Layout Constraints

When creating either planar or conformal data, 3DTOP will accept both Manhatten and 45° lines in the layout, due to the polygon manipulation algorithms used. As figure 4.26 demonstrates, during creation of semi–conformal data, 45° lines are introduced even though the layout is purely Manhatten. If 45° lines are included in the input in certain combinations with Manhatten lines, the creation of collars around conducting layers to produce temporary slopes as outlined in the algorithm description yields polygons containing lines which are neither 45° nor Manhatten. This situation is shown in figure 4.31. Manipulation of these polygons is not currently supported by the software, so 45° lines are not accepted as input when semi–conformal data is required.
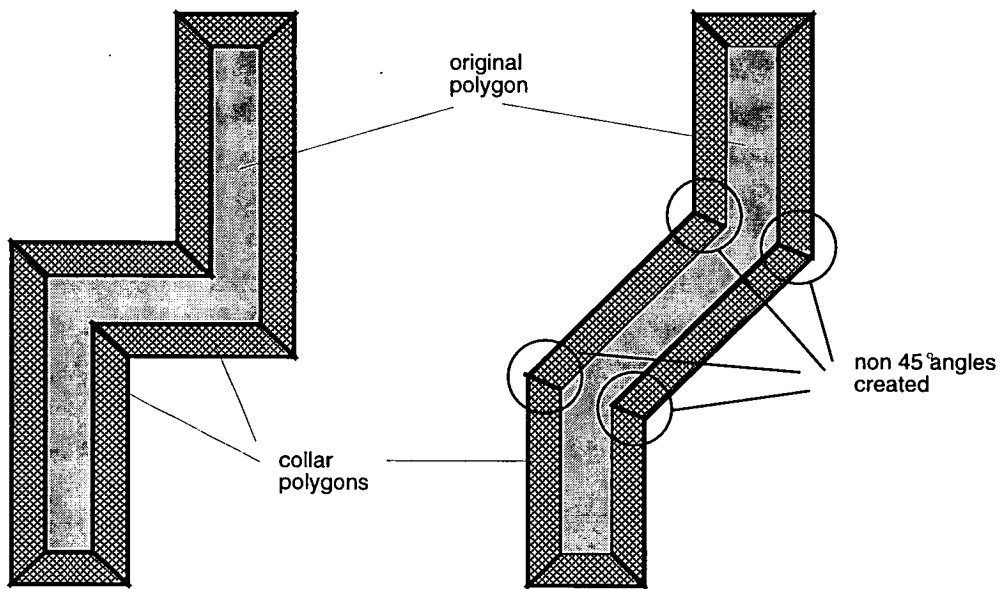
Figure 4.31: Creation of unacceptable polygons around polygon containing 45° lines.

Slopes over slopes

The situation which occurs when a sloping boundary forming a temporary *collar* around a conducting polygon is required to be created above existing sloping boundaries has been mentioned briefly in the algorithm description of section 4.5. This situation will now be described in more detail and some examples presented. Additional slopes are produced following the creation of a conducting layer, to define the following top–surface, as explained in section 4.5. The new slope may be created over a surface which slopes in a direction which is either the same as or opposite to that intended for the new slope. Furthermore, the underlying slope may form all of or just part of the top–surface directly underneath the slope being created. Whatever the case, the procedure is the same. Firstly, a *3dAND* is performed on the new collar polygon with the underlying top surface. Equation 4.1 is then used to find the new z values of each of its vertices. The variables used in this equation are shown in figure 4.32, which shows a cross–section through a conducting layer and the slope being created. The resulting slopes can now be used to create the following top–surface.

$$z = c - ((d/s) * t) \qquad (4.1)$$

z new z coordinate

c current z coordinate

d distance of vertex from originating polygon, in direction of bloat

s step–size of the next dielectric layer

t current layer thickness

Figures 4.33 to 4.38 show various situations in which slopes are created over other slopes. The data was created by 3DTOP and displayed using FastCap.

78
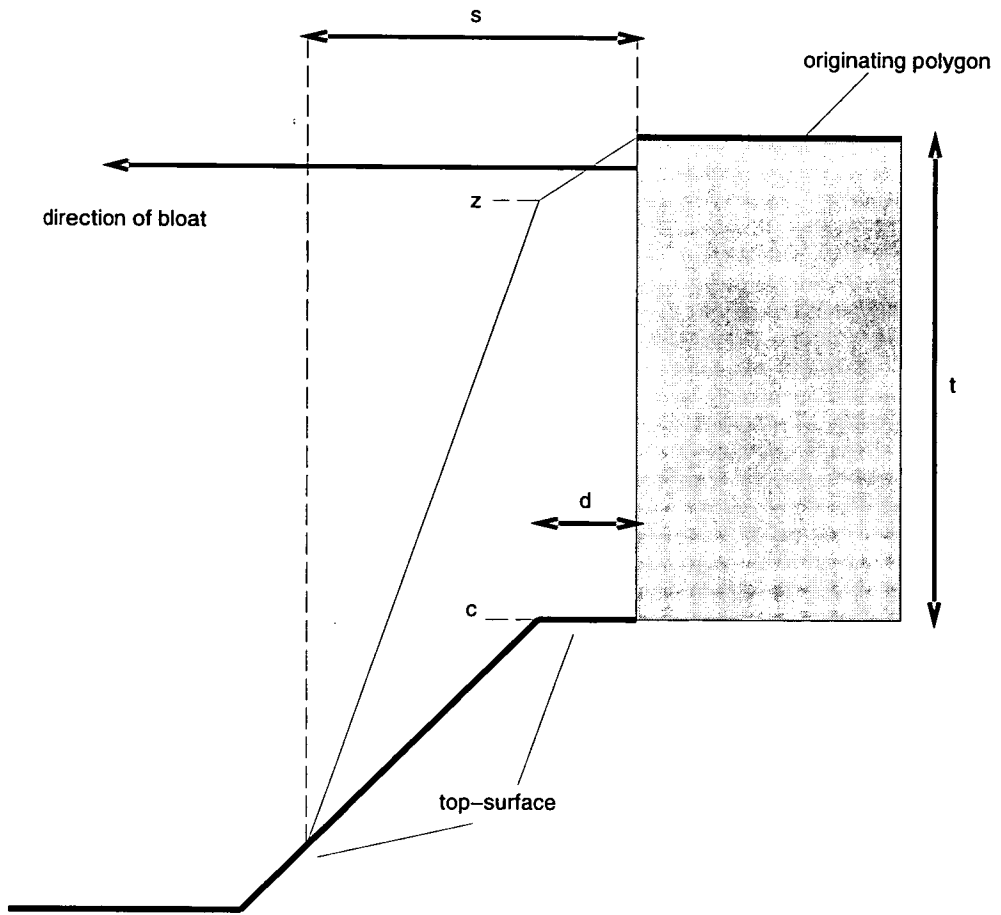
Figure 4.32: Cross section showing slope being created.
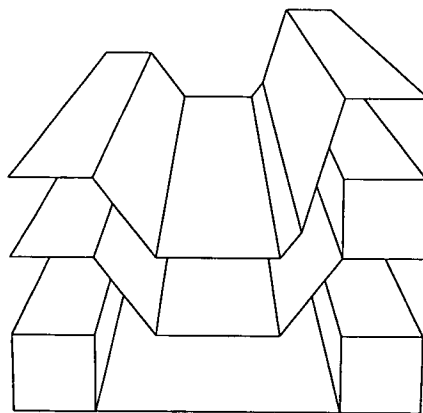
Figure 4.33: Slopes in same direction, dielectric2–step < dielectric1–step.
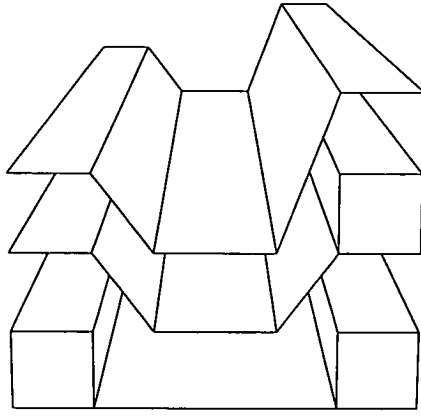
Figure 4.34: Slopes in same direction, dielectric2–step = dielectric1–step.
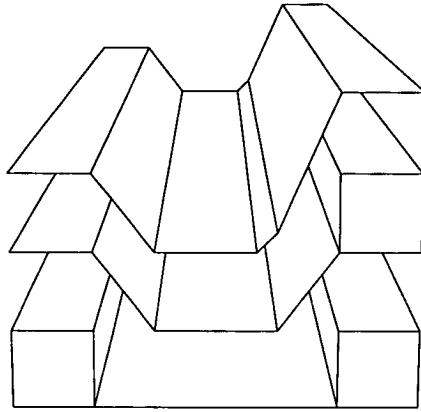
Figure 4.35: Slopes in same direction, dielectric2–step > dielectric1–step.
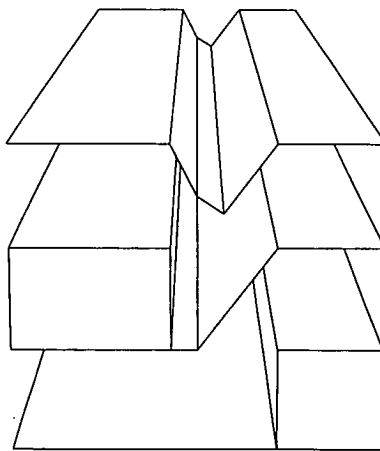
Figure 4.36: Slopes in opposite directions, dielectric2–step < dielectric1–step.
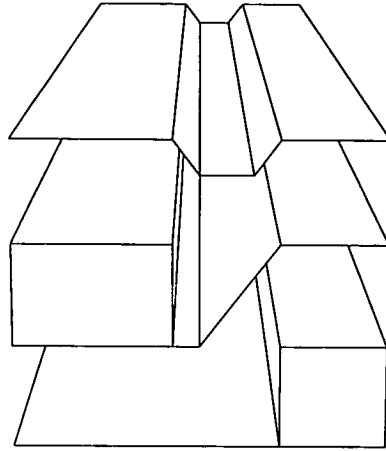
Figure 4.37: Slopes in opposite directions, dielectric2–step = dielectric1–step.
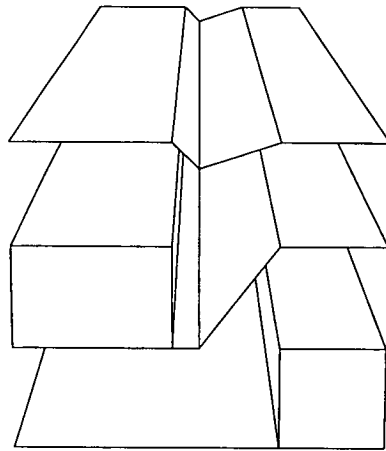
Figure 4.38: Slopes in opposite directions, dielectric2–step > dielectric1–step.

81
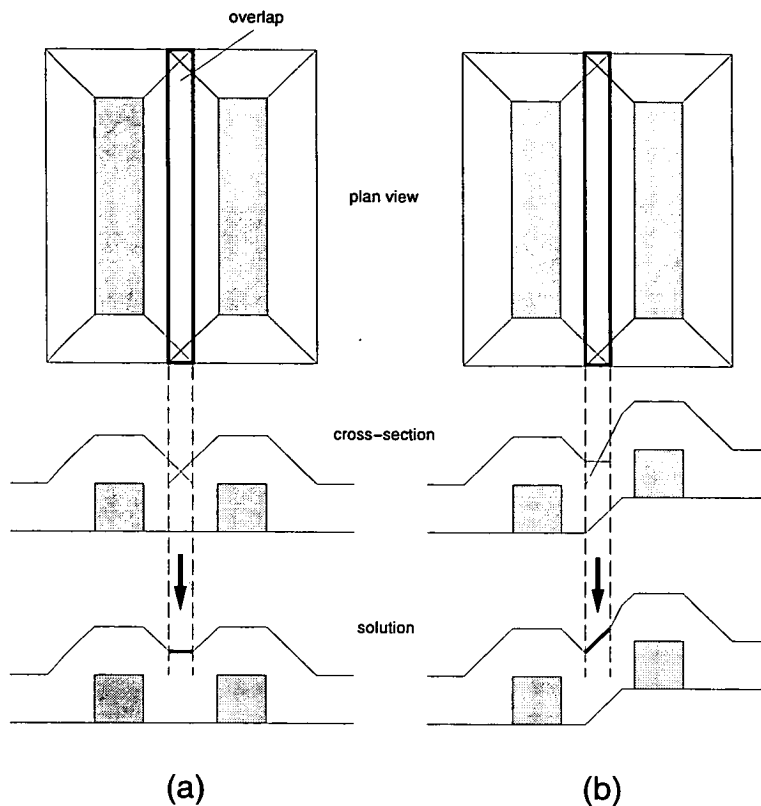
Figure 4.39: Intersecting slopes.

Intersecting slopes on the same layer

When creating slopes around separate polygons on a conducting layer, a situation may occur in which the slopes produced around two different polygons intersect. Two possible cases are shown in figures 4.39(a) and 4.39(b). This situation arises when the user–defined dielectric step–size is greater than half the separation between adjacent conducting–layer polygons. To deal with this situation and to introduce further smoothing of the dielectric layer, the following approach is taken.

Collar polygons around each conducting layer polygon are created as normal. An *andnot* is then performed on each collar polygon with all other collar polygons, and slopes created from the resulting polygons as normal. This results in gaps in the boundaries where the collar polygons overlapped. These areas are filled with polygons created by finding the overlap between collar polygons using an *and* operation. The overlap polygons have the z-values of their vertices set equal to those of the previously

82

created *Poly3D* vertices with which they are coincident in x and y. These overlap polygons are represented in figure 4.39 by the thick black line.

Figures 4.40 to 4.42 show situations in which the dielectric step–size varies from ·50% to 90% of the conducting layer polygon separation. These figures were created using 3DTOP and FastCap.
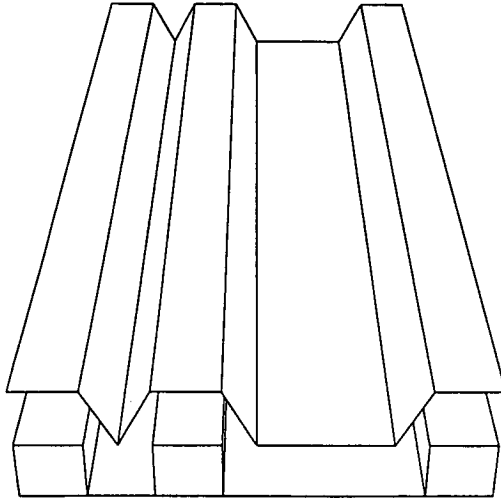
Figure 4.40: Dielectric stepsize = 50% of conducting layer polygon separation.

4.5.2 Semi–Conformal Boundary Example

Figure 4.43 shows the layout used to test the creation of semi–conformal boundaries as input to FastCap. This layout also serves to demonstrate 3DTOP's ability to read in text and deal with anomalies in node naming, as previously described in section 4.3.

In the control file, the `connect` statement,

```
connect ( 11 , 16 , 17 :   17 , 18 , 19)
```

specifies that when layers 11, 16 and 17 (polysilicon, contact and metal1), or layers 17, 18 and 19 (metal1, via and metal2) coincide, electrical connectivity is assumed. In the layout shown in figure 4.43, nodes 1 and 4 are connected, and in response to this, 3DTOP produces the following message:
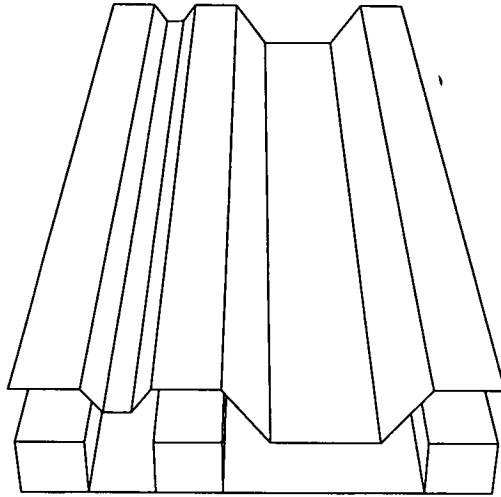
Figure 4.41: Dielectric stepsize = 70% of conducting layer polygon separation.
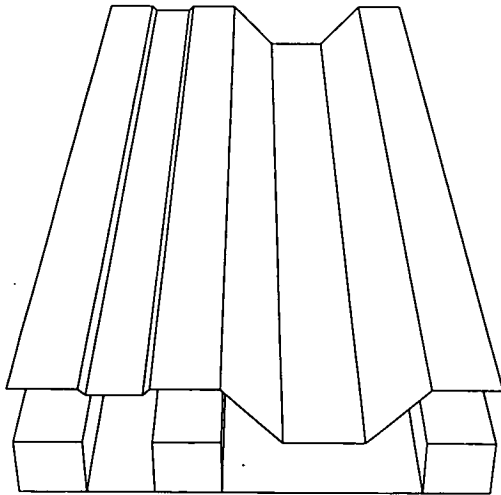
Figure 4.42: Dielectric stepsize = 90% of conducting layer polygon separation.

```
nodes node1 and node4 are connected.
combining node1 and node4 as node1
```

All polygons which were originally part of node4 are now reassigned to node1.

The files which 3DTOP creates to form input to FastCap attach an electrical node name as defined on the layout to each boundary. For example, the files describing the lower boundary of the polysilicon and of metal1 are as follows.

```
0 polylower
Q node1 0 0 200 0 3000 200 200 3000 200 200 0 200
Q node2 600 0 200 600 3000 200 800 3000 200 800 0
200

0 metal1lower
Q node3 1200 0 400 1200 3000 400 1400 3000 400
1400 0 400
Q node1 1800 0 400 1800 3000 400 2000 3000 400
2000 0 400
Q node1 0 1800 600 0 2000 600 200 2000 600 200
1800 600
```

Note that as expected the node names used to define the polysilicon are `node1` and `node2`, and those defining metal1 are `node1` and `node3`.

The boundary data is gridded by 3DTOP so as to produce suitable input data for FastCap. Figure 4.44 shows the gridded boundary data, and the results of the 3D capacitance simulation performed using this data are shown in table 4.3. Notice that in contrast to previous capacitance matrices presented in this thesis, the total capacitance on each individual node does not equal the sum of the capacitances between it and the other electrical nodes. This is due to the additional capacitance on each node to ground, due to the inclusion of a ground plane in this simulation. 3DTOP can also produce semi–conformal data as input to the ray–tracer POV–Ray. The POV–Ray output comprising the substrate and conducting layers is shown in figure 4.45.

	node1	node2	node3
node1	90	17	33
node2	17	48	11
node3	33	11	69

Table 4.3: Capacitance matrix showing capacitances simulated using FastCap, with 3D semi–conformal boundary description created from layout shown in Figure 4.43 (all capacitances in nF).
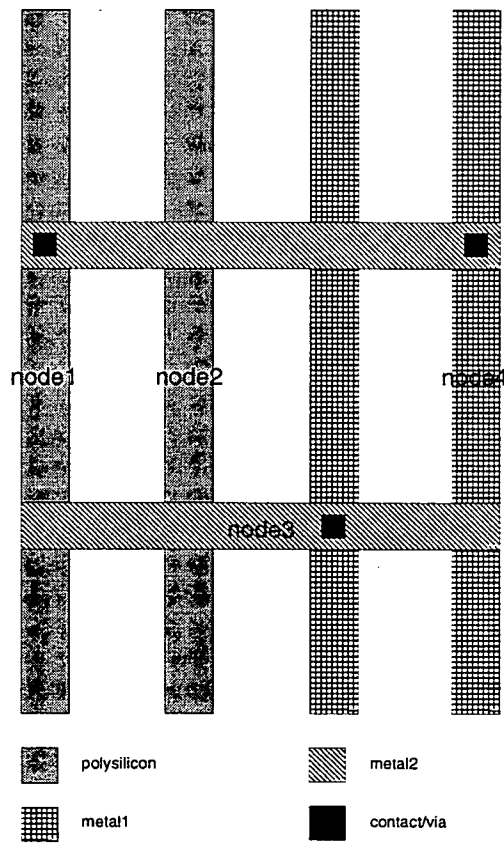
Figure 4.43: Layout used to create semi–conformal data for FastCap.
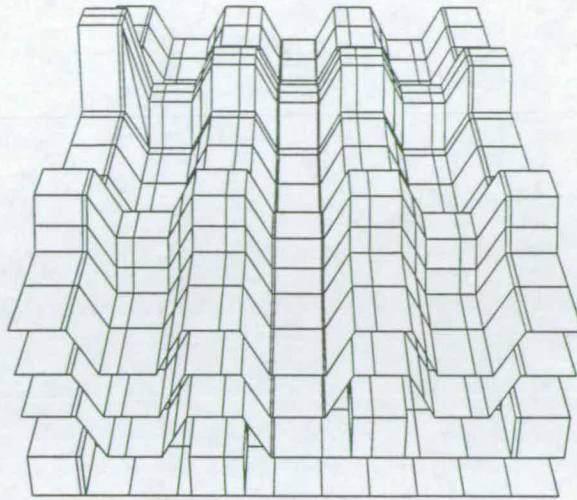
Figure 4.44: Semi–conformal gridded boundary data created from example layout shown in Figure 4.43 using 3DTOP and FastCap.
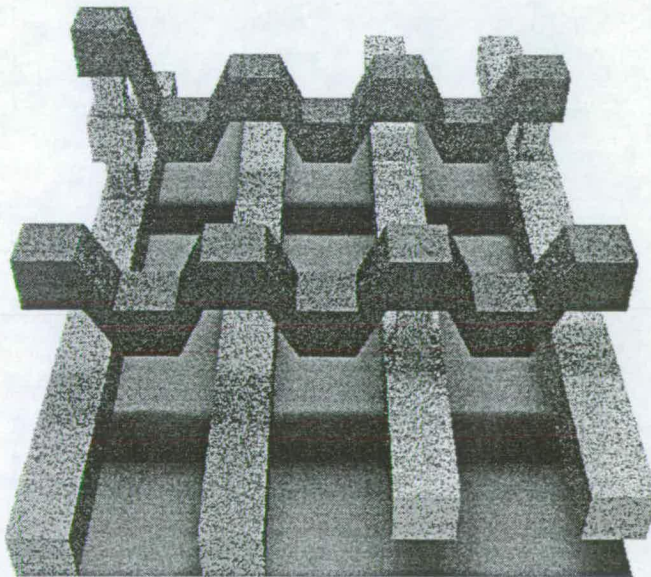
Figure 4.45: Semi–conformal description of substrate and conducting layers produced using 3DTOP and POV–Ray from example layout shown in Figure 4.43.
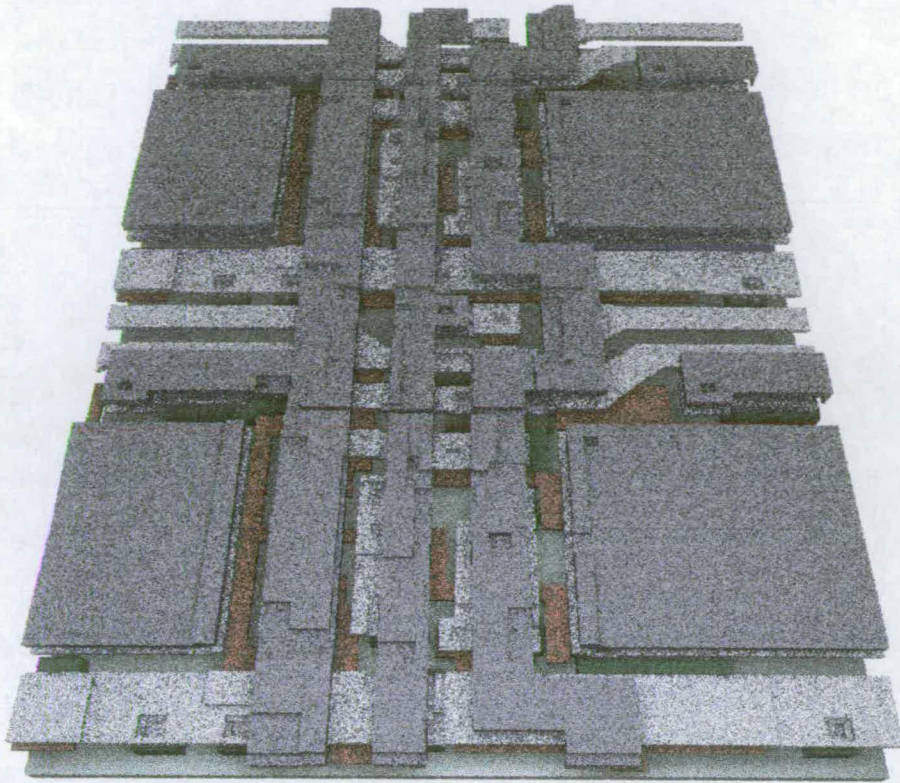
Figure 4.46: Representation of part of an array of SLM pixels created using 3DTOP and POV–Ray.
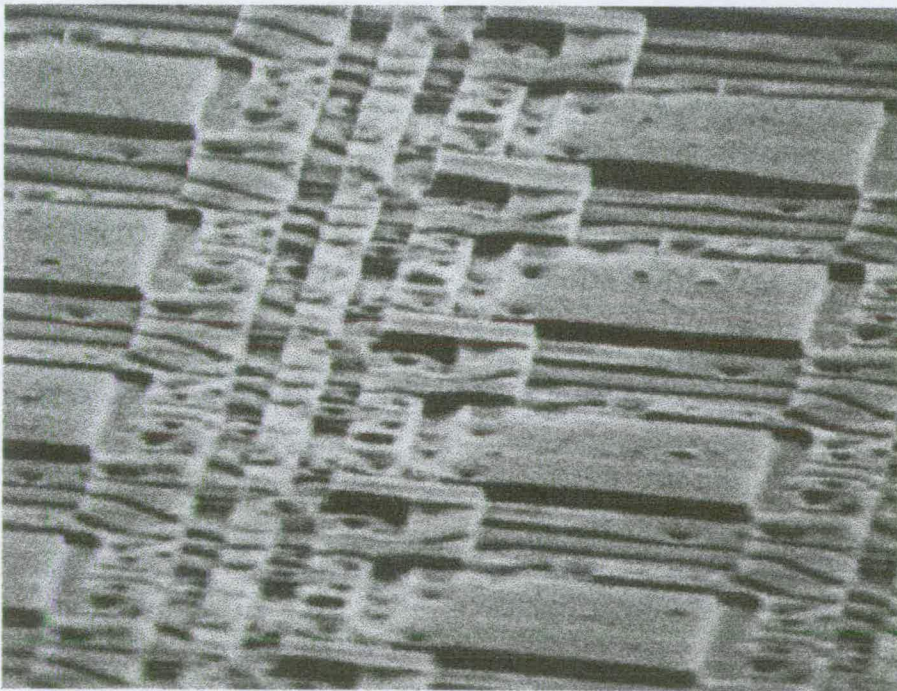
Figure 4.47: Scanning electron micrograph of part of the same array of SLM pixels.

4.6 Summary

In this chapter, the capabilities of 3DTOP have been presented. The flexibility of 3DTOP has been demonstrated by describing the three types of 3D representation that it can be used to produce, i.e. planar, semi–conformal and conformal. The algorithms used to produce each type of 3D representation have been explained, and examples presented. The input data describing the layout required by 3DTOP to produce these representations can be obtained easily from the widely used GDSII format, and a small area of an IC layout can be converted into a 3D representation in a matter of seconds.

3DTOP has the benefit of not being tied to any one type of capacitance simulator. It has been shown to interface with two widely used capacitance simulators, Raphael and FastCap, which use finite difference and boundary element solution techniques respectively. The capacitance matrices produced using the block and boundary representations in conjuction with Raphael and FastCap respectively have been shown to agree in general. Any small dissimilarities in the results produced are likely to be due to the different algorithms employed by the simulators.

3DTOP also interfaces with the ray tracing software POV–Ray for the purposes of visualisation. Figures 4.46 and 4.47, which show a representation of part of an array of spatial light modulator (SLM) pixels created using 3DTOP and POV–Ray along with a scanning electron micrograph of the same array, demonstrate the success of 3DTOP and POV–Ray as a means of representation and visualisation of IC topography.

The flexibility of 3DTOP in the data it produces and the software with which it interfaces leads to a wide range of applications, as desribed in the following chapter.

Chapter 5

Applications of 3DTOP

5.1 Introduction

3DTOP can be used to automatically create a planar, conformal or semi–conformal 3D representation of 2D layout, as described in the previous chapter. There are many software packages available which take data describing a structure in three dimensions and produce simulated values of a particular property. These properties may be electrical (resistance, capacitance and inductance for example), thermal, or even mechanical [32],[33],[72]. 3DTOP has potential to be used with many simulation packages which take 3D data as input, and can also be used in conjunction with visualisation software, in particular POV–Ray [68].

In this chapter, some applications of 3DTOP are described. In section 5.2, 3DTOP is used to demonstrate the importance of using an appropriate 3D representation when finding values of interconnect capacitance using a 3D capacitance simulator. Section 5.3 contains an investigation into the significance of parasitic interconnect capacitance in an example circuit, and compares a conventional extraction technique with a method which involves the use of 3DTOP. In section 5.4, the potential applications of 3DTOP in the simulation and visualisation of microelectromechanical systems (MEMS) are considered. Finally, the information presented in the chapter is summarised in section 5.5.

5.2 Comparison of 3D Data Representations

The representations created by 3DTOP are not intended to mimic exactly the processed IC topography - this is a job for a *process simulator* (see chapter 3). Process simulators provide very accurate topography representation, but their operation is not straightforward and their algorithms are slow, making their routine use by IC designers unlikely. 3DTOP *emulates* the manufacturing process and provides a good approximation to the IC topography. The type of 3D representation chosen when 3D simulations are to be performed on a structure forming part of an IC will depend on the process which is to be used in its manufacture. For example, if the process involves planarisation of some form, leading to an approximately planar topography, the obvious 3DTOP representation to use is the *planar* one. If the process does not involve planarisation, the resulting topography will in general be non–planar. The choice of which of the two non–planar representations to use will depend on the expected or observed step–coverage of existing topography by each layer as it is deposited. If the step coverage is in general fairly abrupt, as shown in figure 5.1(a), the conformal representation should be used. If it is less abrupt, as shown in figures 5.1(b) and 5.1(c), a semi–conformal representation should be used, with the user–defined step–coverage and layer–thickness parameters determining the step–coverage angle, α. The observed step–coverage is unlikely to match any of these situations exactly, so the representation which most closely approximates reality should be chosen. For example, if the step–coverage tends to take the form of a *bullnose* as shown in figure 5.1(d), the conformal representation would be the most appropriate one to use.

It is not currently possible to use 3DTOP to freely mix different types of representation for different layers. If the conformal representation is specified, all layers will be treated as conformal. If the semi–conformal representation is specified, all layers will be treated as semi–conformal, although there is flexibility as regards the angle α (see figures 5.1(b) and 5.1(c)), since specific step–coverage and layer–thickness parameters are defined for each layer individually in the 3DTOP control file. Planar representations can be mixed with conformal and semi–conformal representations to some degree. If
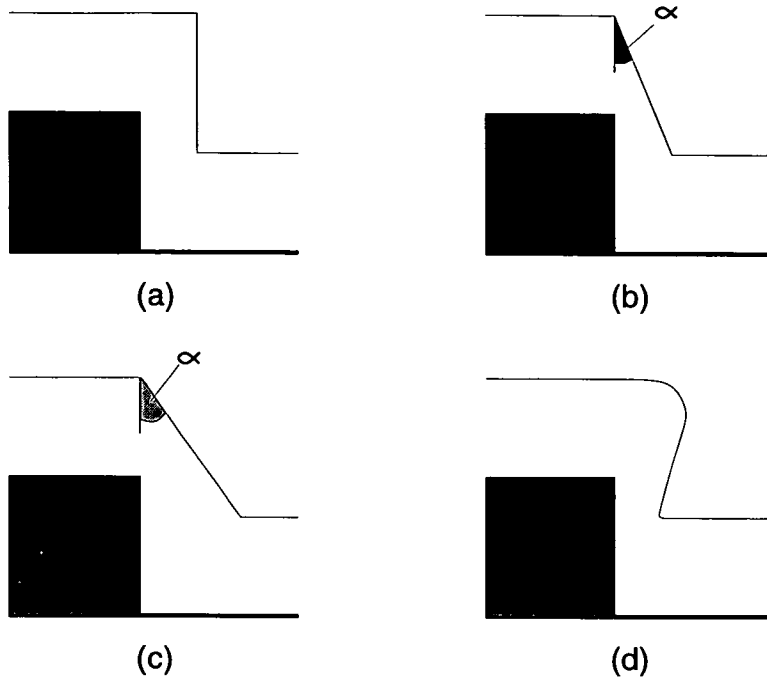
Figure 5.1: Possible step–coverage profiles.

all the planar layers lie beneath the conformal or semi–conformal layers, no problems will be encountered. However, due to the nature of the data–creation algorithm, in which each layer is laid down as a 'blanket' of a uniform thickness on top of the existing topography, layers cannot be successfully specified as planar after conformal or semi–conformal layers have been created. This situation can be easily dealt with by running 3DTOP more than once, including an offset of an amount equal to the sum of the thicknesses of all previous layers when creating the planar layers, and then simply combining all the data produced. In fact, this method is used when creating the 3D representation of the example circuit in section 5.3.

In this section, four example layouts will be used to demonstrate the significance of the type of 3D data representation used when extracting capacitance between interconnect tracks. The significance of the aspect ratio of the interconnect tracks, i.e. their thickness to width ratio, is also investigated. This is important since as IC feature sizes reduce, track width scales much more rapidly than track thickness, so aspect ratios increase.

5.2.1   Significance of Type of 3D Representation

Four example layouts, of low but increasing complexity, were used to investigate the significance of the type of 3D representation used when simulating capacitance. Layout 1, shown in figure 5.2, consists simply of two parallel metal1 tracks. Layout 2, shown in figure 5.3, is similar to layout 1, in that it contains two parallel metal1 tracks, but the complexity has been increased slightly by adding a wider polysilicon track underneath one of the metal1 tracks. Layout 3, shown in figure 5.4, consists of one straight polysilicon track with two parallel metal1 tracks crossing it. The final layout, layout 4, is shown in figure 5.5. A further polysilicon track has been added to layout 3, the metal1 tracks are now staggered, and a metal2 track has been added.

Each of these layouts was used to produce a GDSII file which was used as input to 3DTOP. The output format chosen was 2D boundaries representing 3D shapes, a format compatible with the 3D capacitance simulator FastCap [33], as all three types of data representation can be produced in this format. The user–defined layer–thickness parameters in the control file were all defined to be similar to the widths of the narrower tracks on the layout, leading to a maximum aspect ratio of approximately 1. The user–defined step–coverage parameters were defined to be half the value of the layer thicknesses. The 3D representations were all created with dielectric layers beneath the lowest interconnect layer and above the uppermost interconnect layer, and the relative dielectric constant of all dielectrics was defined as 3.9. All three types of representation were produced for each layout, 3D capacitance simulations were carried out on each set of data using FastCap, and images were produced using POV–Ray. The results for each of these sets of simulations are shown in tables 5.1 to 5.4. Layouts 1 and 2 are so simple that the images produced by POV–Ray are not included here, but the POV–Ray images of planar, semi–conformal and conformal data produced using layouts 3 and 4 are shown in figures 5.6, 5.7 and 5.8, and figures 5.9, 5.10 and 5.11.

In order to investigate the effect of a change in the aspect ratios of the interconnect tracks, a second set of 3D representations of layout 4 were produced, this time with the

93
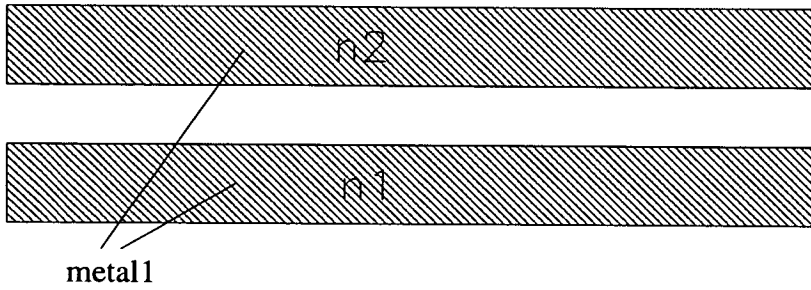
Figure 5.2: Layout 1.

nodes	capacitance (nF) for planar 3D data	capacitance (nF) for semi–conformal 3D data	capacitance (nF) for conformal 3D data	change in semi–conformal as a % of planar	change in conformal as a % of planar	change in conformal as a % of semi–conformal
n1,n2	3.927	3.924	3.927	0	0	0

Table 5.1: Results from simulations of layout 1 with interconnect track aspect ratios of one.

layer–thickness and step–coverage parameter values 1/3 of those previously used. The results of the 3D capacitance simulations are shown in table 5.5, and the images created using POV–Ray in figures 5.12 to 5.14.
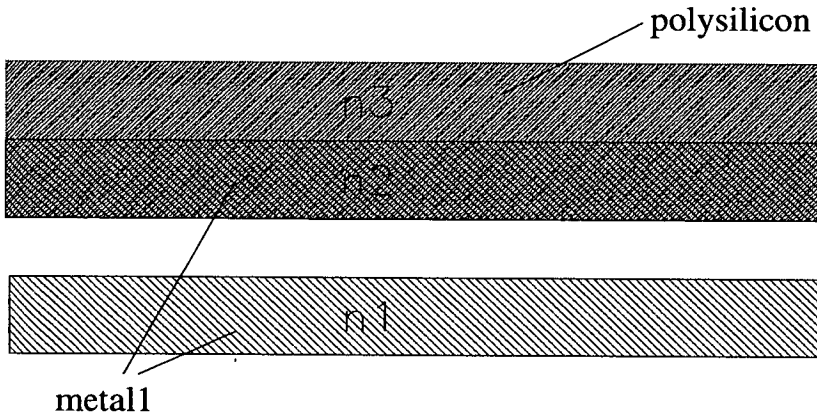
Figure 5.3: Layout 2.

nodes	capacitance (nF) for planar 3D data	capacitance (nF) for semi–conformal 3D data	capacitance (nF) for conformal 3D data	change in semi–conformal as a % of planar	change in conformal as a % of planar	change in conformal as a % of semi–conformal
n1,n2	3.254	2.407	2.376	-26	-27	-1
n1,n3	1.45	2.494	2.495	+72	+72	0
n2,n3	2.442	2.885	2.913	+18	+19	+1

Table 5.2: Results from simulations of layout 2 with interconnect track aspect ratios of one.
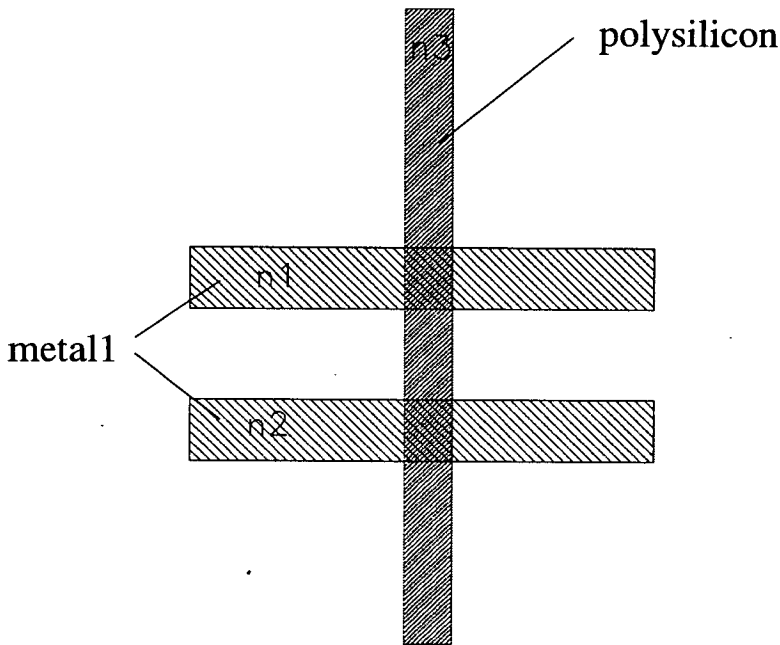
Figure 5.4: Layout 3.

nodes	capacitance (nF) for planar 3D data	capacitance (nF) for semi–conformal 3D data	capacitance (nF) for conformal 3D data	change in semi–conformal as a % of planar	change in conformal as a % of planar	change in conformal as a % of semi–conformal
n1,n2	1.518	1.514	1.683	0	-3	+3
n1,n3	1.339	1.938	1.86	+45	+39	-4
n2,n3	1.375	1.975	1.897	+44	+38	-4

Table 5.3: Results from simulations of layout 3 with interconnect track aspect ratios of one.
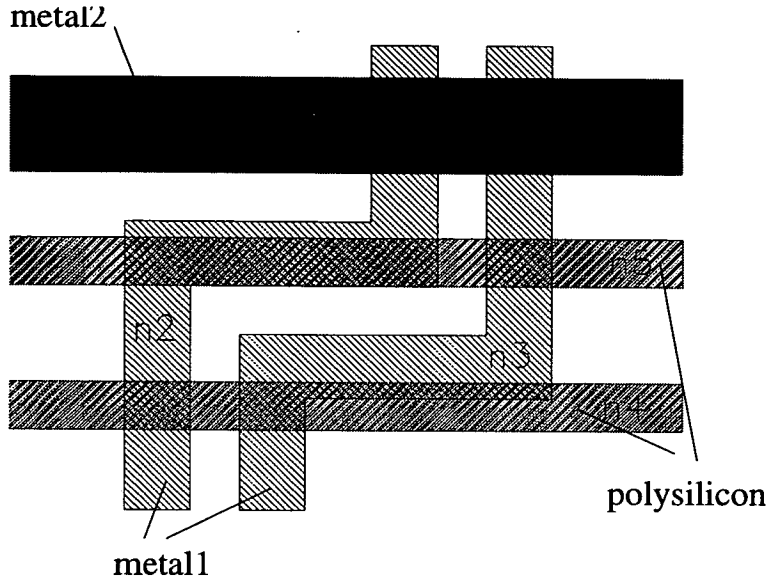
Figure 5.5: Layout 4.

nodes	capacitance (nF) for planar 3D data	capacitance (nF) for semi-conformal 3D data	capacitance (nF) for conformal 3D data	change in semi-conformal as a % of planar	change in conformal as a % of planar	change in conformal as a % of semi-conformal
n1,n2	1.783	3.079	2.962	+73	+66	-4
n1,n3	1.365	2.01	1.991	+47	+46	-1
n1,n4	0.234	0.2368	0.2656	+1	+13	+12
n1,n5	0.4135	0.754	0.8363	+82	+102	+11
n2,n3	2.54	2.406	2.939	-5	+16	+22
n2,n4	0.8502	1.326	1.226	+48	+37	-8
n2,n5	1.528	2.017	1.737	+32	+14	-14
n3,n4	1.509	2.62	2.403	+74	+59	-8
n3,n5	1.051	1.847	1.733	+76	+68	-6
n4,n5	1.7	1.317	1.342	-23	-21	+2

Table 5.4: Results from simulations of layout 4 with interconnect track aspect ratios of one.
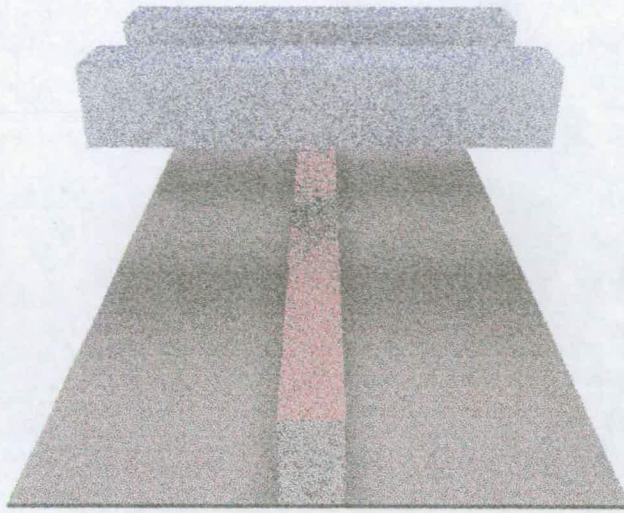
Figure 5.6: Planar representation of layout 3 (figure 5.4), with dielectrics removed for clarity.
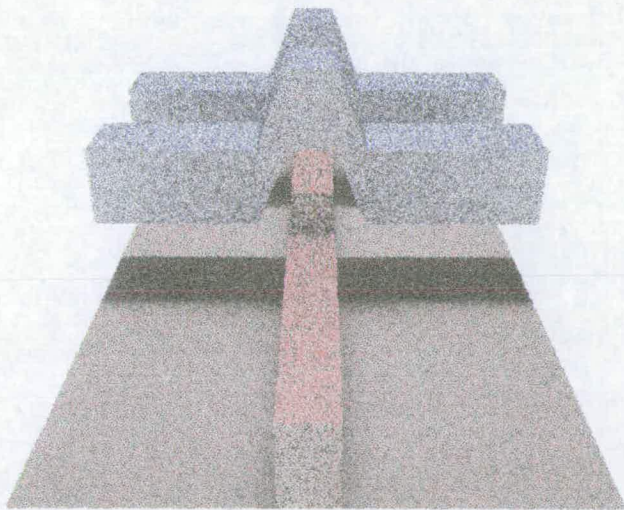
Figure 5.7: Semi–conformal representation of layout 3 (figure 5.4), with dielectrics removed for clarity.
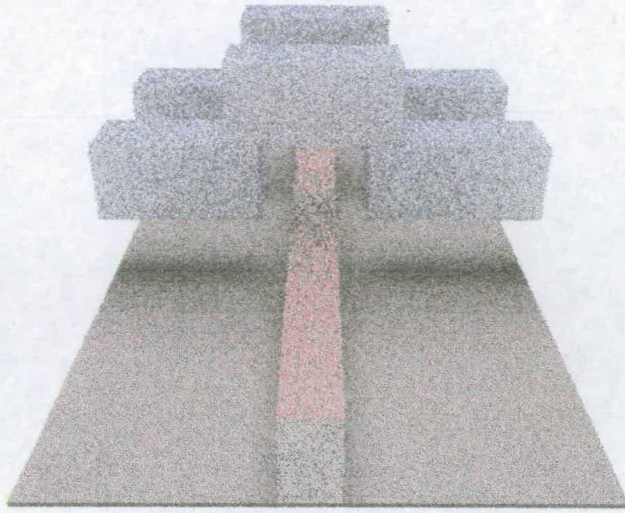
Figure 5.8: Conformal representation of layout 3 (figure 5.4), with dielectrics removed for clarity.
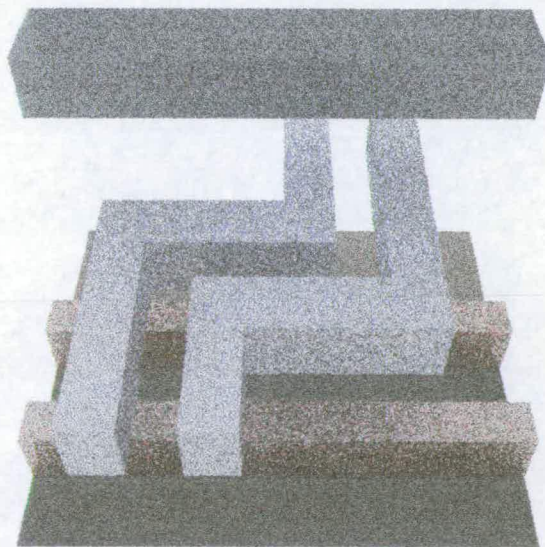
Figure 5.9: Planar representation of layout 4 (figure 5.5), with interconnect track aspect ratios of one.
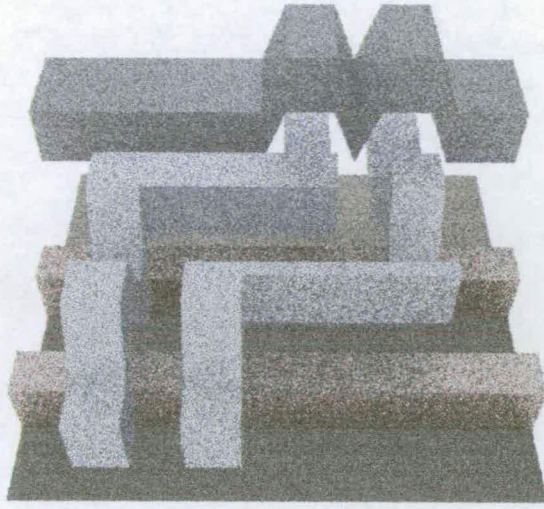
Figure 5.10: Semi–conformal representation of layout 4 (figure 5.5), with interconnect track aspect ratios of one.
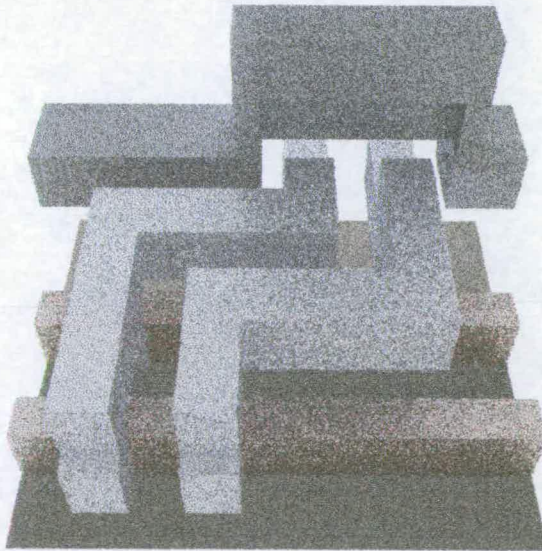
Figure 5.11: Conformal representation of layout 4 (figure 5.5), with interconnect track aspect ratios of one.
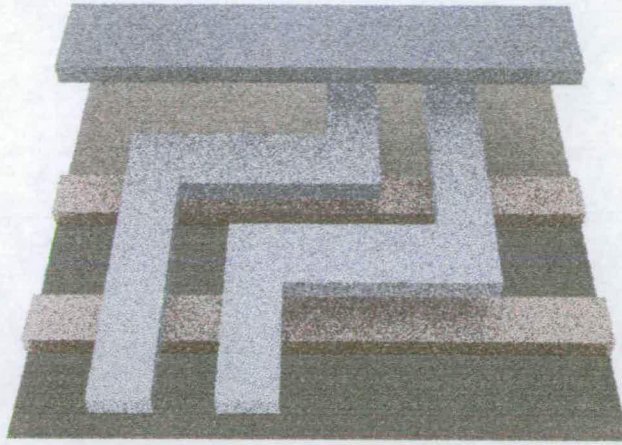
Figure 5.12: Planar representation of layout 4 (figure 5.5), with interconnect track aspect ratios of one third.
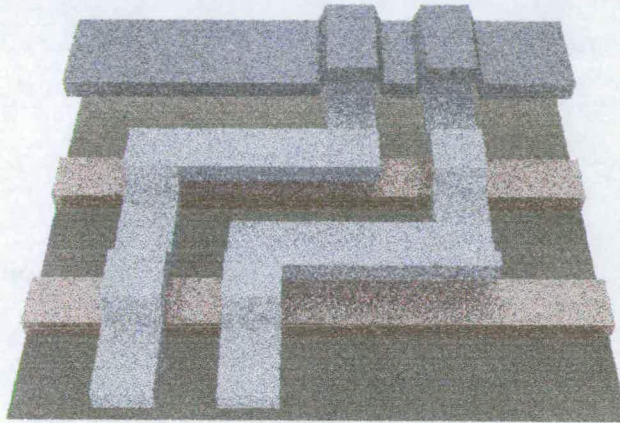
Figure 5.13: Semi–conformal representation of layout 4 (figure 5.5), with interconnect track aspect ratios of one third.

Figure 5.14: Conformal representation of layout 4 (figure 5.5), with interconnect track aspect ratios of one third.

nodes	planar (nF)	semi–conformal (nF)	conformal (nF)	change in semi–conformal as a % of planar	change in conformal as a % of planar	change in conformal as a % of semi–conformal
n1,n2	2.146	2.921	2.915	+36	+36	0
n1,n3	1.649	2.314	2.243	+40	+36	-3
n1,n4	0.2148	0.2051	0.1974	-5	-8	-4
n1,n5	0.634	0.7544	0.7493	+19	+18	-1
n2,n3	1.145	1.042	1.085	-9	-5	+4
n2,n4	1.229	1.693	1.633	+38	+33	-4
n2,n5	2.744	3.855	3.678	+40	+34	-5
n3,n4	2.461	3.619	3.48	+47	+41	-4
n3,n5	1.45	1.987	1.916	+37	+32	-4
n4,n5	0.7314	0.5877	0.5847	-20	-20	-1

Table 5.5: Results from simulations of layout 4 with interconnect track aspect ratios of one third.

5.2.2 Discussion

The results shown in table 5.1, relating to layout 1, show a virtually unchanged value of capacitance between the metal1 tracks regardless of the type of 3D representation used. This is to be expected, since only one layer is considered in this case, so there is no sequential build–up of topography. However, these results confirm that there are no unforseen anomalies introduced when producing the different types of data representation, and allow us to proceed with the following comparisons with reinforced confidence.

The results in table 5.2, relating to layout 2, exhibit a significant difference between the capacitance values obtained for the planar representation and the conformal and semi–conformal representations, although there is little difference between the values obtained for the conformal and semi–conformal representations. The largest difference in capacitance is between nodes n1 and n3. This result can easily be explained with reference to figure 5.15, which shows a cross–section through the three interconnect tracks in the planar (figure 5.15(a)) and conformal (figure 5.15(b)) cases. It is obvious from this
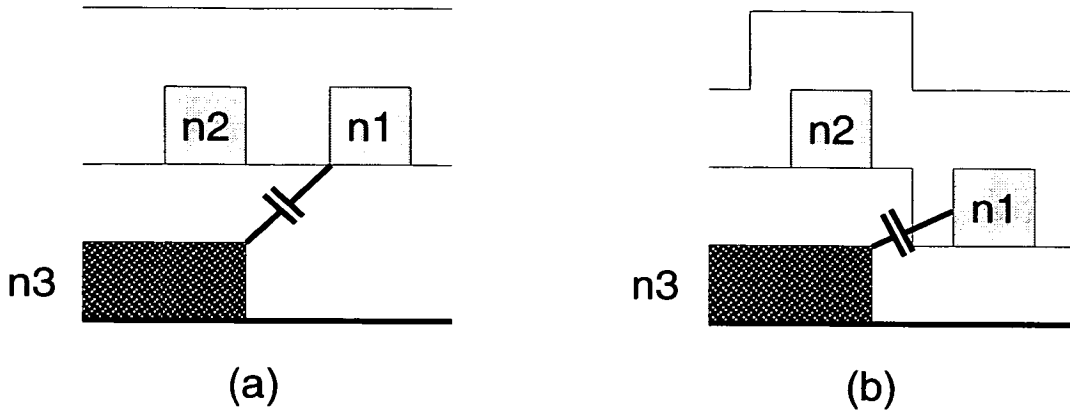
Figure 5.15: Cross sections of planar and conformal representations of layout 2.

figure that the capacitance between nodes n1 and n3 will be significantly higher in the conformal case than the planar case, which corresponds to the results obtained by simulation. This simple example serves to illustrate very clearly the importance of selecting an appropriate data representation when performing 3D capacitance simulations.

The results shown in tables 5.3 and 5.4 relate to layouts 3 and 4, where the 3D data was created assuming an interconnect track aspect ratio of approximately 1. The individual values obtained will not be discussed, but it is obvious from these results that the planar, conformal and semi-conformal representations can yield significantly different simulated capacitance values. Examination of figures 5.6, 5.7 and 5.8, and figures 5.9, 5.10 and 5.11 gives an insight into why these capacitance values are so variable.

The results shown in table 5.5 again relate to layout 4. However, in this case the 3D data was produced assuming an interconnect track aspect ratio of approximately 1/3. The average percentage differences in simulated capacitance values for this set of simulations and those carried out with the aspect ratio approximately equal to 1 are shown in table 5.6. These results clearly show that the type of data representation chosen has an increasing effect as the interconnect track aspect ratio increases. However, as IC feature sizes are reduced and aspect ratios continue to increase, the likelihood that the process will incorporate some kind of planarisation also increases [73], and the conformal and semi-conformal representations become less appropriate.

	aspect ratio =1	aspect ratio =3
average change in semi–conformal as % of planar	46.4	27.1
average change in conformal as % of planar	44.2	26.3
average change in conformal as % of semi–conformal	8.8	3

Table 5.6: Changes in simulated values for two track aspect ratios.

5.3 Conventional and 3D Capacitance Extraction of Single Transistor SLM Pixel

Parasitic capacitances can have various effects on any electronic circuit. They must be charged and discharged, leading to increased power dissipation and reduced speed of operation. Furthermore, parasitic capacitances between circuit nodes lead to crosstalk and the possibility of noise in the analog case and bit errors in the digital case. It is therefore important that where a circuit is expected to be sensitive to the effects of parasitic capacitances, the capacitance values are determined as precisely as possible.

In this section, a capacitance extraction will be performed on a circuit in which parasitic capacitances are expected to have a marked effect on performance. First, the example circuit is described, and its behaviour without the presence of parasitic capacitances explained. The location and expected effect on circuit performance of parasitic capacitances is then presented, and the method typically used to extract the parasitic capacitances outlined. As an alternative to this conventional extraction technique, 3DTOP is used to produce 3D data in block format, and this data is used to find values for the parasitic capacitances using Raphael, and to visualise the circuit using POV–Ray. The values obtained using the conventional and 3D extraction techniques are compared, and
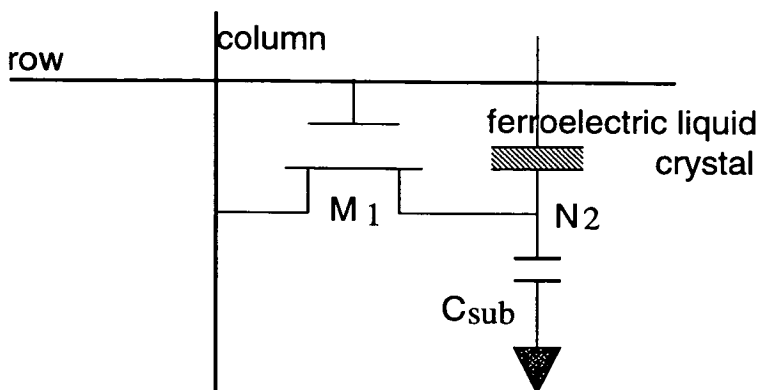
Figure 5.16: Single transistor pixel.

SPICE simulations used to show their effects on the performance of the circuit.

5.3.1 Single Transistor SLM Pixel Circuit

The example circuit used to demonstrate the effects of parasitic capacitances on circuit performance is a single transistor pixel for a ferroelectric liquid crystal over silicon spatial light modulator (SLM) [74]. This circuit is shown in figure 5.16.

This pixel forms part of a large array of identical pixels, which together form a miniature display. Referring to figure 5.16, when the row is high and the transistor M_1 is on, the value on the column is passed to node N_2. The value on this node, which determines the state of the ferroelectric liquid crystal above it, is stored by the capacitance C_{sub} after the node is isolated by the row voltage being driven low. C_{sub} is the depletion region capacitance between the transistor source and the substrate. The transistor source is made as large as possible to maximise this capacitance, which in this case is calculated to be 55fF [75].

The layout of an array of nine of these pixels is shown in figure 5.17, up to and including layer METAL2. The final device actually has 4 metal layers, the last two of which are added in a post–processing procedure [76]. Of these last two metal layers, METAL4 is used to form a top–level optically flat mirror to enhance the quality of the display, and METAL3 is a ground plane which complements METAL4 with a slight overlap

104
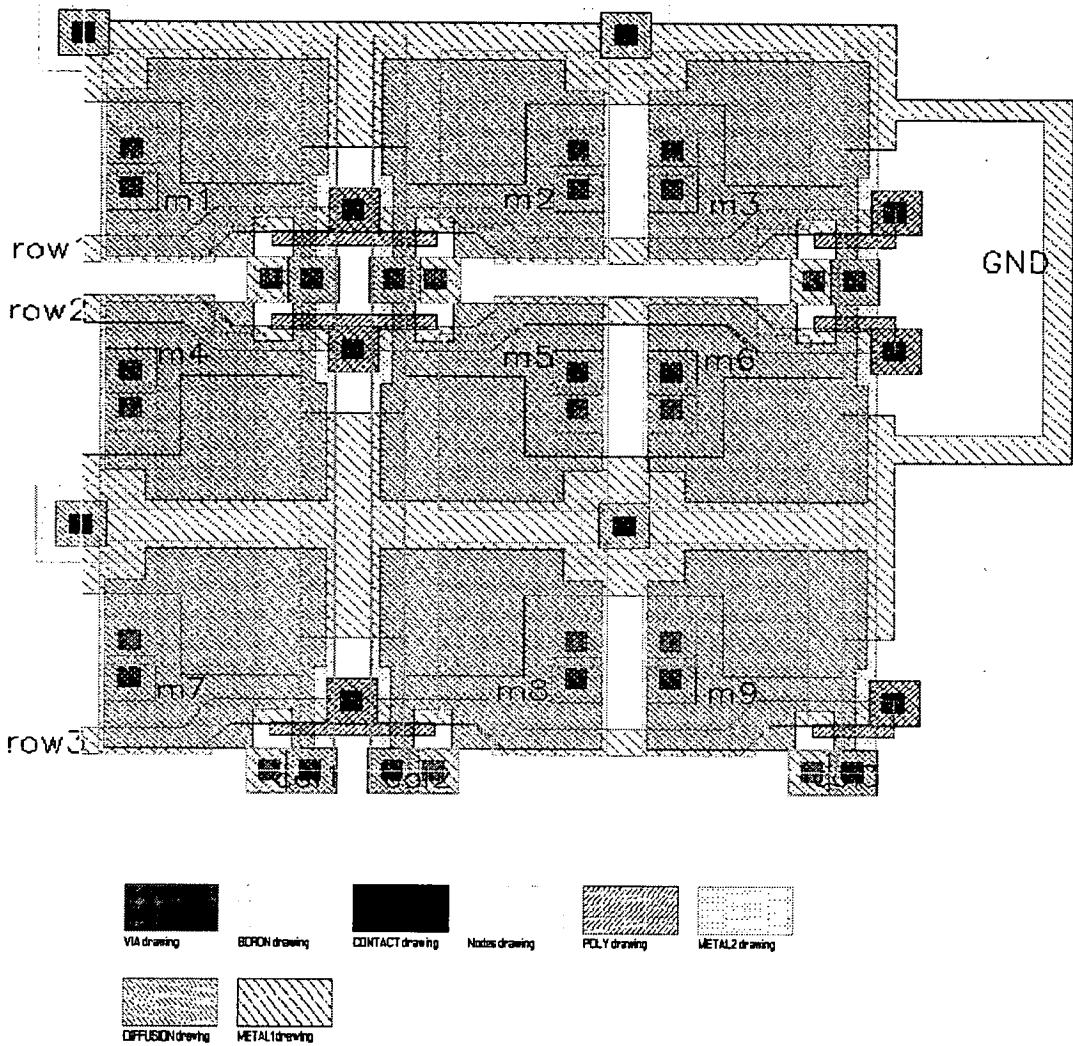
Figure 5.17: Layout of nine pixel transistors, up to layer METAL2.

in order to minimise the amount of light reaching the silicon substrate. Light reaching the substrate will cause the depletion–region capacitance C_{sub} to discharge. Layers METAL3 and METAL4 are shown in figure 5.18.

The procedure for writing a logic 1 onto the node N_2, also referred to as the mirror, will now be described. The column is driven high, then the row is driven high in order that the value on the column is passed to the mirror. Since the transistor M_1 is n–type, the value written to the mirror will be degraded by the transistor's threshold voltage, V_t. This occurs because as charge accumulates on capacitor C_{sub}, the voltage on the mirror, which is also the the transistor source, approaches the value on the gate, V_{row}. When the mirror voltage is equal to $V_{row} - Vt$, the transistor switches off, so the capacitor cannot be further charged [23]. This procedure is illustrated in figure 5.19, which shows the output of a SPICE simulation. Only the parasitic capacitances associated with the MOSFET device M_1, including the storage capacitor C_{sub}, are considered here. Note that after the row has been driven low, the value on the mirror remains virtually constant due to charge stored by C_{sub}.

Now that the behaviour of the circuit has been explained, the effects of parasitic capacitances can be presented. Figure 5.20 shows the circuit of figure 5.16 with the parasitic capacitances due to interconnect added. Capacitances C_1 and C_2 each act as a capacitive load on the row and column respectively. These capacitances will have little effect in the context of a single pixel, but when the effect of 1000 (on the row) and 700 (on the column) of these capacitances in parallel is considered, their effect is significant. Capacitances C_3 and C_4 act as coupling capacitors between the mirror node and the column and row respectively, and should be minimised as far as possible. Capacitance C_5, in parallel with C_{sub}, improves the charge storage on the mirror node, and should be maximised.

More specifically, the effect of capacitances C_3 and C_4 can be explained in terms of charge sharing. Consider the effect of C_4, the capacitance between the mirror and row, when the row is driven from a high to a low voltage, and capacitance C_{sub} is storing a
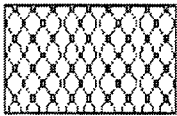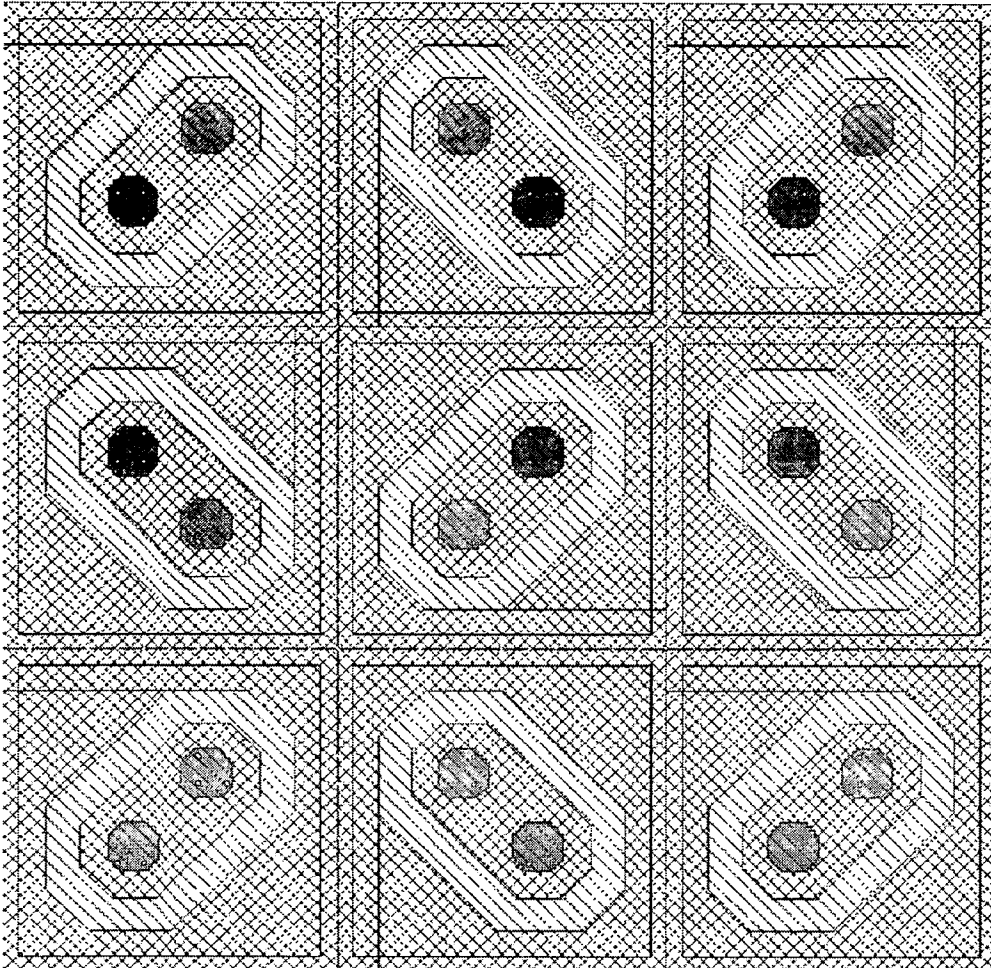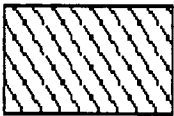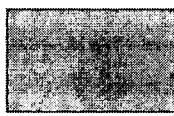
Figure 5.18: Layout of nine pixel transistors with post–processing layers only shown.
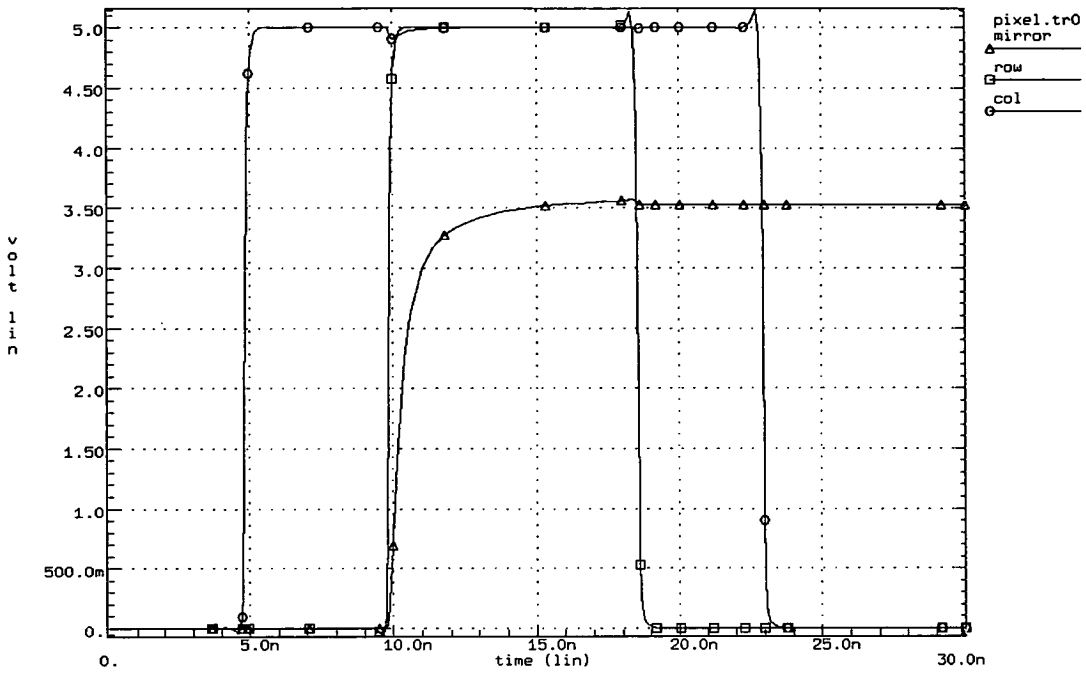
Figure 5.19: Simulation results showing pixel behaviour with no parasitic capacitances included in the circuit.
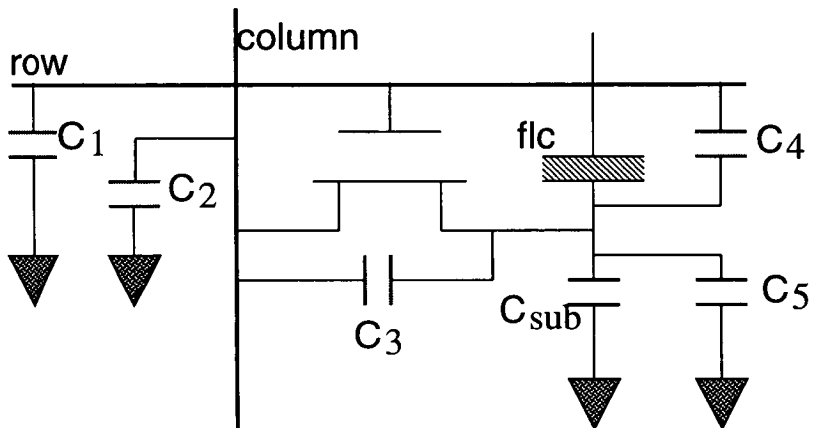
Figure 5.20: Single transistor pixel with parasitic interconnect capacitances shown.

108

time = t₁ Vrow high   time = t₂ Vrow low
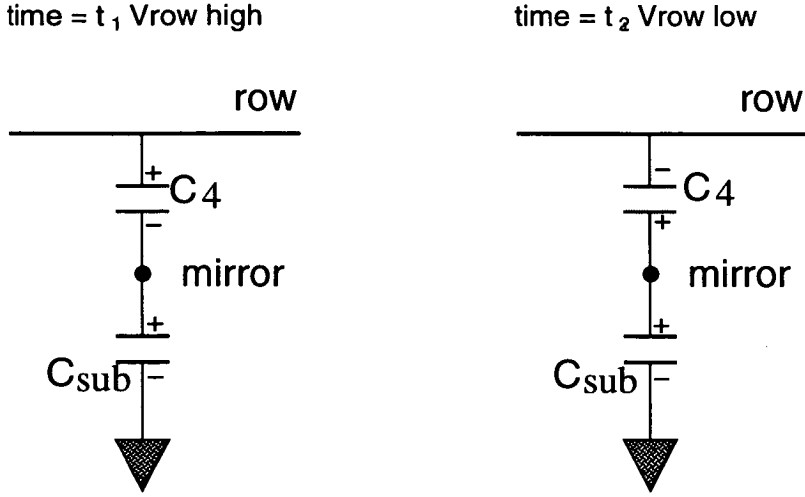
Figure 5.21: Capacitances C_4 and C_{sub} on the mirror node.

high voltage. This situation will be explained with reference to figure 5.21. The voltage on the row at time t_1, V_{row_1}, is high, and the charge on the mirror node, Q_{m_1} is given by

$$Q_{m_1} = C_{sub} * V_{mirror_1} - C_4 * (V_{row_1} - V_{mirror_1}) \qquad (5.1)$$

using Q=CV. When the row is driven low, at time t_2, the charge on the mirror node becomes

$$Q_{m_2} = C_{sub} * V_{mirror_2} + C_4 * V_{mirror_2} \qquad (5.2)$$

Since charge is conserved, $Q_{m_1} = Q_{m_2}$, so setting equations 5.1 and 5.2 equal gives

$$V_{mirror_1} * (C_{sub} + C_4) - V_{row_1} * C_4 = V_{mirror_2} * (C_{sub} + C_4) \qquad (5.3)$$

Therefore, the voltage V_{mirror_2} at time t_2, once the row has been driven low, is given by

$$V_{mirror_2} = V_{mirror_1} - (V_{row_1} * C_4)/(C_{sub} + C_4) \qquad (5.4)$$

i.e. the larger the value of C_4, the more the voltage stored on the mirror node will be degraded when the row switches low.

5.3.2   Conventional Parasitic Capacitance Extraction

Conventional parasitic capacitance extraction was carried out on this circuit using Cadence [31], an industry standard design and simulation suite. This required a GDSII

109

file and a *technology file,* which is produced to accompany a particular manufacturing process. The technology file includes various instructions and rules, including a set of rules relating to the extraction of parasitic capacitances. Boolean operations are carried out to find the overlaps between and coincident edges of specific mask layers. The results of these various operations are used along with unit capacitance values to find capacitances between the layers. The unit capacitance values may have been produced by hand calculation, simulation or measurement, and their accuracy is not under the designer's control.

The complexity of technology files varies. A file dealing with both overlap and fringing capacitance for 3 layers of interconnect along with two types of dielectric will contain around 70 equations. A section of the technology file used to extract capacitances from the pixel circuit follows, in which all numerical values have been replaced by 'C' in order to preserve confidentiality. This is a selection of equations which deal with the mask layer METAL1, and gives some idea of the complexity of the capacitance extraction.

```
(CAP = geomOr(DIFFUSION POLY))
(CmmT = measureParasitic(length
(METAL1 inside METAL2) Ce-17 two_net
))
(Cmmc = measureParasitic(length
(METAL1 coincident METAL2) Ce-17 two_net
))
(Cmmb = measureParasitic(length
(METAL1 butting METAL2) Ce-17 two_net
)) (Cm1C = measureFringe(METAL1
(calculate
((1 * Ce-17 * 1.00) / s)
)
(sep < 5) diffNet opposite
))
(Cm1P = measureParasitic(area
(METAL1 over bkgnd not_over CAP
not_over NTUB
) Ce-17 two_net
))
```

```
(CmwP = measureParasitic(area
(Cm1B = measureParasitic(length
(METAL1 outside CAP over bkgnd
not_over NTUB
) Ce-17 two_net
)) (METAL1 over NTUB not_over CAP) Ce-17 two_net
))
(CmwB = measureParasitic(length
(METAL1 outside CAP over NTUB) Ce-17 two_net
))
(CmPP = measureParasitic(area
(METAL1 over POLY) Ce-17 two_net
))
(CmPB = measureParasitic(length
(METAL1 inside POLY) Ce-17 two_net
))
(CmnP = measureParasitic(area
(METAL1 over ndiff) Ce-17 two_net
))
(CmpP = measureParasitic(area
(METAL1 over pdiff) Ce-17 two_net
))
(CmnB = measureParasitic(length
(METAL1 inside ndiff) Ce-17 two_net
))
(CmpB = measureParasitic(length
(METAL1 inside pdiff) Ce-17 two_net
)) (Cmnb = measureParasitic(length
(METAL1 butting ndiff) Ce-17 two_net
))
(Cmpb = measureParasitic(length
(METAL1 butting pdiff) Ce-17 two_net
))
```

Since layers METAL3 and METAL4, along with associated dielectric and via layers, were added during a post–processing procedure, the technology file supplied did not contain rules to extract parasitic capacitances for these layers. Two solutions to this problem were considered – to modify the technology file to include extraction rules relating to these layers, or to perform the extraction by hand. Both of these solutions involve considerable time and effort, and introduce the possibility of errors. It was decided that the most straightforward solution in this case was to perform the extraction using hand calculations. The results of this extraction are presented later in section 5.3.4.
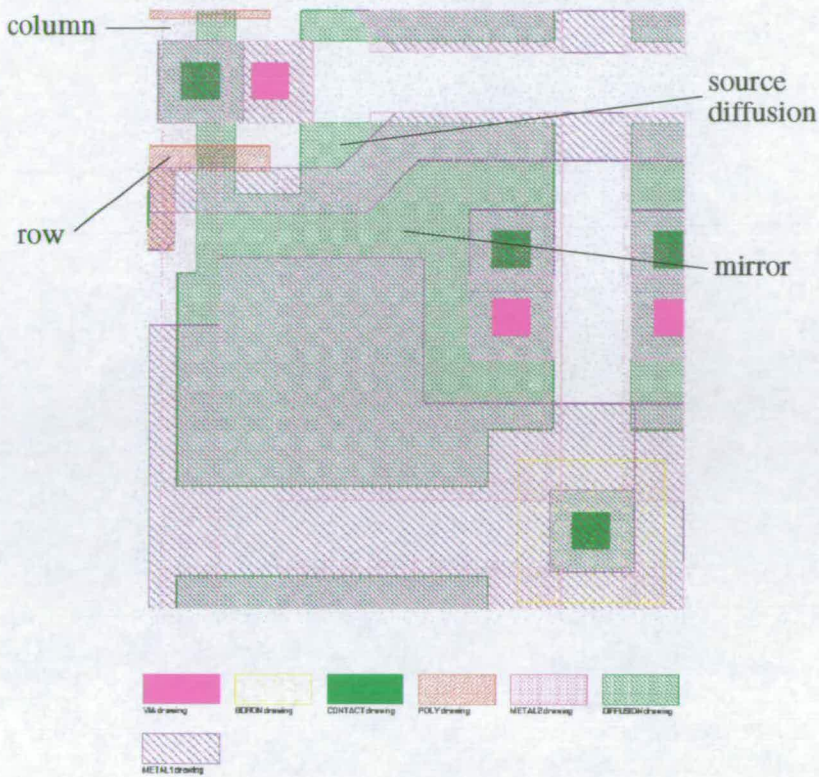
Figure 5.22: Cut down layout containing one pixel.

5.3.3 3DTOP Extraction

A parasitic capacitance extraction was performed on the example pixel circuit using 3DTOP. In order to reduce the amount of input data for 3DTOP, the layout shown in figure 5.17 was cut down to an area encompassing the central pixel, whilst retaining sufficient surrounding layout to extract capacitances between the central mirror and surrounding electrical nodes. This layout up to and including METAL2 is shown in figure 5.22.

In the post–processing procedure, the inter–layer dielectrics between layers METAL2 and METAL3, and between METAL3 and METAL4, are planarised. To take account of this situation, 3DTOP was run twice, first creating a conformal block description of the layers up to and including METAL2, then creating a planar block description of the remaining layers. An extra layer was included when creating layers METAL3 and METAL4 with a thickness equivalent to the combined thicknesses of layers up to and including

112
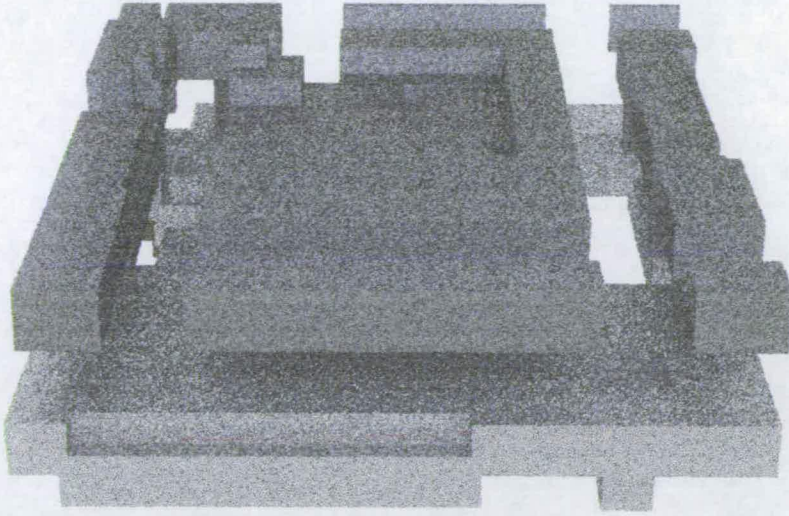
Figure 5.23: POV–Ray output showing conducting layers up to and including METAL2.
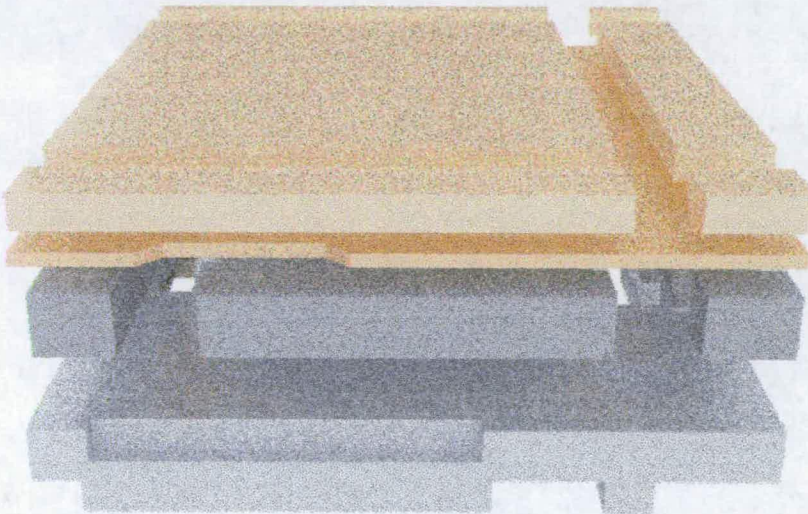
Figure 5.24: POV–Ray output showing conducting layers up to and including METAL4.

METAL2. The data produced by 3DTOP excluding the temporary layer included to ensure correct height information for layers METAL3 and METAL4 was collated into one Raphael input file, and the 3D capacitances simulated. POV–Ray compatible data was also produced, and the POV–Ray output showing conducting layers up to METAL2, and up to METAL4, is shown in figures 5.23 and 5.24.

113

node1	node2	capacitance (fF) extracted using conventional method	capacitance (fF) extracted using the 3DTOP method	% change
M_5	M_2	0.446	0.396	+11
M_5	M_6	0.744	0.766	+3
M_5	M_8	0.539	0.466	-14
M_5	$row2$	2.548	1.952	-23
M_5	gnd	13.627	16.595	+22
M_5	$col2$	0.604	0.643	6
$row2$	gnd	1.604	1.233	-23
$row2$	$col2$	0.778	0.812	4
$col2$	gnd	3.495	2.374	-32

Table 5.7: Capacitance between electrical nodes, obtained using conventional and 3DTOP extraction methods.

5.3.4 Results

The values obtained for parasitic capacitances using the conventional and 3DTOP methods are shown in table 5.7 – the nodes referred to are shown in figure 5.17. Values of capacitance between the central mirror, M_5 and mirrors M_2, M_6 and M_8 are shown. Capacitances between the central mirror and the other mirrors surrounding it are not shown since they are smaller than the tabulated capacitances by approximately a factor of ten, and as such were expected to have a negligible effect on the circuit performance. The performance of the example circuit with the addition of some of these capacitances will now be investigated. The stimuli to the circuit are identical to those described in section 5.3.1.

First, we will consider the effect of the loading capacitance to ground on the row and the column. The row and column are each driven by two consecutive inverters. Each row drives 1000 transistors, so the row–gnd capacitance shown in table 5.7 will be multiplied by 1,000. Similarly, each column is connected to the drain of 700 transistors, so the column–gnd capacitance shown in table 5.7 will be multiplied by 700. The specified clock rate for this circuit is 65MHz, so the row will be high for 1/130MHz, i.e. approximately 8ns. The effect of the conventionally and 3D extracted capacitances is

114
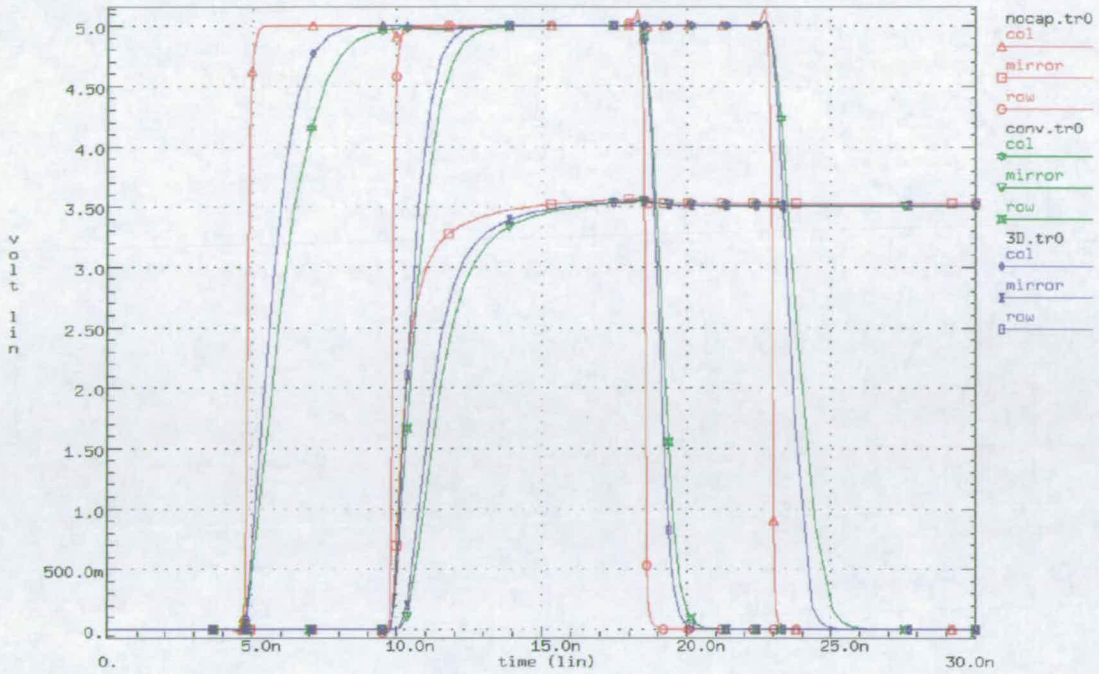
Figure 5.25: Behaviour of circuit with capacitances row–gnd and column–gnd obtained using conventional and 3D methods included.

shown in figure 5.25. The curves under the heading *nocap.tr0* in the legend, and shown in red, illustrate the behaviour of the circuit with no parasitic interconnect capacitances included in the SPICE file. The curves under the heading *conv.tr0*, shown in green, illustrate the behaviour of the circuit with parasitic interconnect capacitances extracted using conventional techniques, whilst those under the heading *3D.tr0*, shown in blue, illustrate the behaviour of the circuit with parasitic capacitances extracted using 3DTOP and Raphael. As expected, the inclusion of the parasitic interconnect capacitances has a marked effect on the rise and fall times of the row and column. The capacitance values found using conventional techniques are larger than those extracted using 3DTOP and Raphael, and therefore have a greater effect on these rise and fall times.

The SPICE input file used to generate these results follows.

115

```
SINGLE TRANSISTOR
.OPTIONS POST NODE NOPAGE


VIN ROWIN 0 PWL(0 0V 9NS 0V 10NS 5V 17.6NS 5V 18.6NS 0V 20NS 0V 30NS 0V)
VVDD VDD 0 5V

VVSS VSS 0 0V
VCOLIN COLIN 0 PWL(0 0V 4NS 0V 5NS 5V 22NS 5V 23NS 0V)
*MAIN CIRCUIT


M1 MIRROR ROW COL VSS NMOS L=0.7U W=1U
M2 NOTROW ROWIN VSS VSS NMOS L=1.2U W=12U
M4 ROW NOTROW VSS VSS NMOS L=1.2U W=24U
M3 NOTROW ROWIN VDD VDD PMOS L=1.2U W=20U
M5 ROW NOTROW VDD VDD PMOS L=1.2U W=40.2U
M6 NOTCOL COLIN VSS VSS NMOS L=1.2U W=12U
M8 COL NOTCOL VSS VSS NMOS L=1.2U W=24U
M7 NOTCOL COLIN VDD VDD PMOS L=1.2U W=20U
M9 COL NOTCOL VDD VDD PMOS L=1.2U W=40.2U

*CAPACITANCES
CCOL COL VSS 2447E-15F
CROW ROW VSS 1600E-15F
C1 MIRROR VSS 55E-15F

.TRAN 0.05NS 30NS
.PRINT TRAN V(ROW) V(MIRROR) V(COL)
```

The next parasitic capacitances to be considered are those between the mirror and row, and the mirror and column. The expected charge–sharing effect of these capacitances was discussed in section 5.3.1, and can clearly be seen in figure 5.26, which shows the SPICE output when these capacitances are included. Again, since the value of the mirror to row capacitance extracted using conventional techniques is greater than that found using the 3DTOP method, the charge sharing effect is more marked in the conventional case.

Quantitatively, the drop in voltage expected on the mirror node when the row is driven low can be found using equation 5.4 in section 5.3.1. In the 3D extraction case, C4, the capacitance between the mirror and row, consists of the extracted interconnect capacitance of 1.9fF in parallel with the parasitic gate–source capacitance of the n–type MOSFET. The SPICE model used in these simulations assumes a value of 0.35fF for
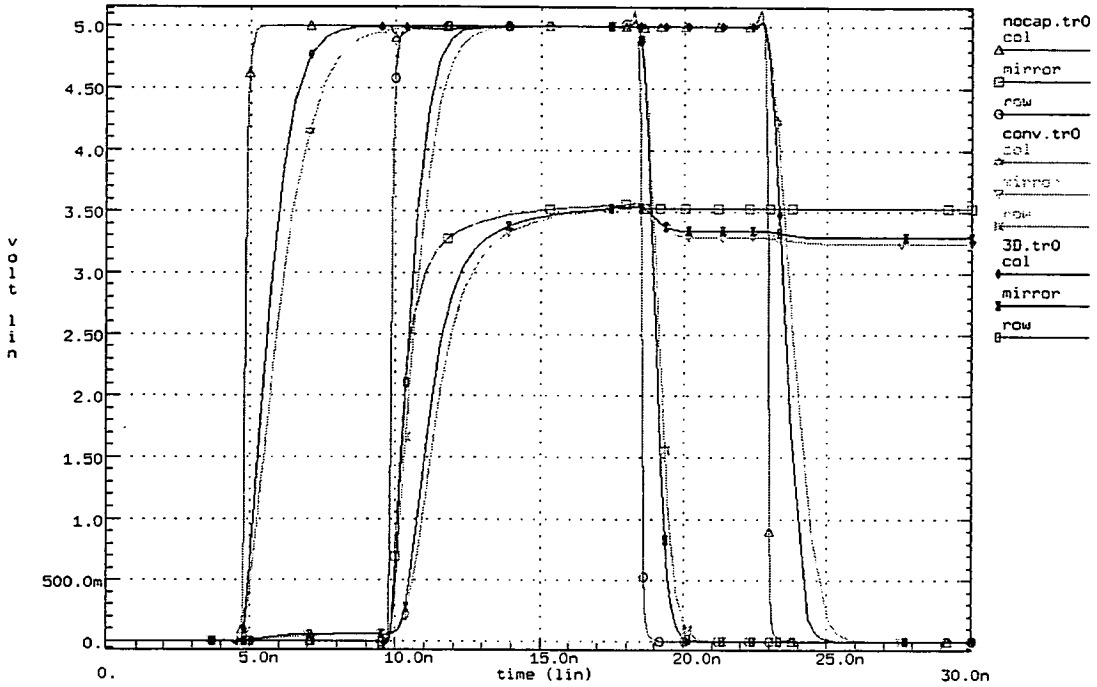
Figure 5.26: Behaviour of circuit with capacitances row–mirror and column–mirror obtained using conventional and 3D extraction methods included.

the gate–source capacitance, so the total capacitance between the mirror and row is the sum of these two capacitances, 2.25fF. Substituting the values C4 = 2.25fF, V_{mirror_1} = 3.55V, V_{row_1} = 5V and C_{sub} = 55fF in to equation 5.4 gives V_{mirror_2} = 3.35V. This corresponds exactly to the value to which the voltage on the mirror drops when the row is driven low in figure 5.26.

The parasitic capacitances between adjacent mirror nodes will lead to charge sharing when the value on one mirror changes whilst the adjacent mirror node's voltage is being held by its C_{sub}. This situation will never arise when transistors associated with the mirrors have a common gate connection, as the voltage on these mirrors will always be driven simultaneously, so the capacitance between nodes M_5 and M_6 need not be considered. The capacitances between nodes M_5 and M_2, and M_5 and M_8, will lead to charge sharing, although the effect will be significantly less than that caused by the mirror–row capacitance since the capacitance values involved are lower.

117

5.3.5 Discussion

In this section, SPICE simulations have been used to confirm that parasitic interconnect capacitances, even in a small circuit, can have a significant effect on circuit performance. This has been demonstrated using a single transistor circuit for an SLM pixel, for which values of parasitic interconnect capacitances were found using conventional and 3DTOP extraction methods. The values extracted using the 3DTOP method differed from those extracted using conventional methods by amounts ranging from -32% to +11%, although the effects on circuit performance of the two different sets of capacitances were not dramatically different. This indicates that this particular circuit is not highly sensitive to even fairly large changes in parasitic capacitance values, a fact largely due to the size of the storage capacitor, C_{sub}. In fact, from inspection of the graph shown in figure 5.26, it can be seen that the voltage held on the mirror once both the row and column driving it have been set low varies by only 0.1V (i.e approximately 3% of its final value), depending on which set of extracted parasitic capacitances are used. If the pixel size were to be reduced, leading to increased resolution capabilities of the pixel array, the size of C_{sub} would be expected to scale at a greater rate than the interconnect capacitances, so it would become increasingly important to accurately determine the values of the parasitic capacitances. In this case, the application of the 3D method has simply lead to increased confidence in the design.

The accuracy of the conventional extraction method depends on the origin of the technology file parameters and on the breadth of layer combinations allowed for in the extraction equations. However, even if the multiplication parameters are extremely accurate, the capacitance values extracted can at best only be approximate, due to the inherent generalisations involved in the technology file equations. In contrast, the 3D extraction method, incorporating the use of a 3D numerical simulator, considers the situation as a whole, so the influence of every part of the layout on every capacitance extracted is accounted for. The 3D extraction method is more versatile than the conventional method, since it allows the designer to change data relating directly to the process such as layer thicknesses. The use of 3DTOP also enables visualisation of the circuit

in three dimensions. This method is able to cope easily with non–standard situations, such as that involving post–processing layers as detailed in this section. However, when a standard manufacturing process is used and a complete technology file is available, the conventional method may be more convenient since it does not require process information. It also requires less time and computing resource than the 3D extraction method. Which of the two extraction methods is used will therefore depend on the accuracy required in the extraction, and the time, resources and information available to the designer.

5.4   Representation and Simulation of MEMS

Microelectromechanical Systems, or MEMS, are exactly what their name implies – systems comprising various microelectronic and micromechanical components. The mechanical components are created using *micromachining* techniques, such as bulk and surface micromachining on silicon, LIGA, silicon fusion bonding and Excimer laser micromachining [77], [78] and [79]. Of these, bulk micromachining is the most mature technology, and involves etching into a silicon wafer either isotropically or anisotropically, to create the required structure [77, 79]. LIGA (from the German Lithographie, Galvanoformung, Abformung), employs lithography, electroplating and moulding processes [77]. Silicon Fusion bonding (SFB) involves the atomic bonding of two silicon layers [77], whilst Excimer lasers are used to micromachine organic materials [78].

The method in which we are interested is *surface micromachining on silicon*. This involves the deposition and etching of thin–film materials, so the process used is very similar to a typical IC manufacturing process. Since 3DTOP can be used to create 3D representations of ICs, it can also be used to create representations of MEMS fabricated using this method. The data created can be used for visualisation using POV–Ray, and has potential to be used as input to various MEMS simulation packages. In fact, work has been carried out on the feasability and likely methods of integrating 3DTOP with a

particular MEMS simulator, SOLIDIS [72, 80].

Simulation of MEMS is a fairly complex undertaking, since both mechanical and electrical performance must be considered simulataneously [77]. Several tools exist to perform these simulations but often, as is the case with ICs, a large problem to be overcome is that of actually producing the 3D representation to form the input to this software. This problem has been addressed [67], [81] and [82], but the solutions offered often rely on the use of commercial software or only consider planar deposition. In some situations, the conformal data production capabilities of 3DTOP may not be of primary importance, since MEMS are often far more complex in the horizontal than the vertical plane. Also, due to the current limitation on 3DTOP that only Manhatten and 45° lines can be dealt with on the layout, microstructures such as gears and cogs cannot be dealt with at present. 3D representations of structures created using special techniques, such as atomic force microscope probe tips created using carefully controlled undercut in etch [77], cannot be produced using 3DTOP, but such structures generally form a small (although very important) part of any MEMS, and as such can easily be added by hand to the 3D data description. However, 3DTOP does undoubtedly provide a means of reducing the need for time–consuming and error–prone 3D data entry by hand.

By way of an example of 3DTOP's application in the representation of MEMS, figure 5.27 shows beams and springs forming an x–y translator [83]. 3DTOP and POV–Ray have been used to create this 3D representation from the mask data.

5.5   Summary

In this chapter, the importance of choosing an appropriate 3D representation when extracting parasitic capacitances has been demonstrated. It has been shown, using 3DTOP and FastCap, that even in very simple IC layouts the variation in extracted capacitance values between adjacent tracks can vary by over 100% depending on the representation chosen. This emphasises the need for a tool such as 3DTOP which
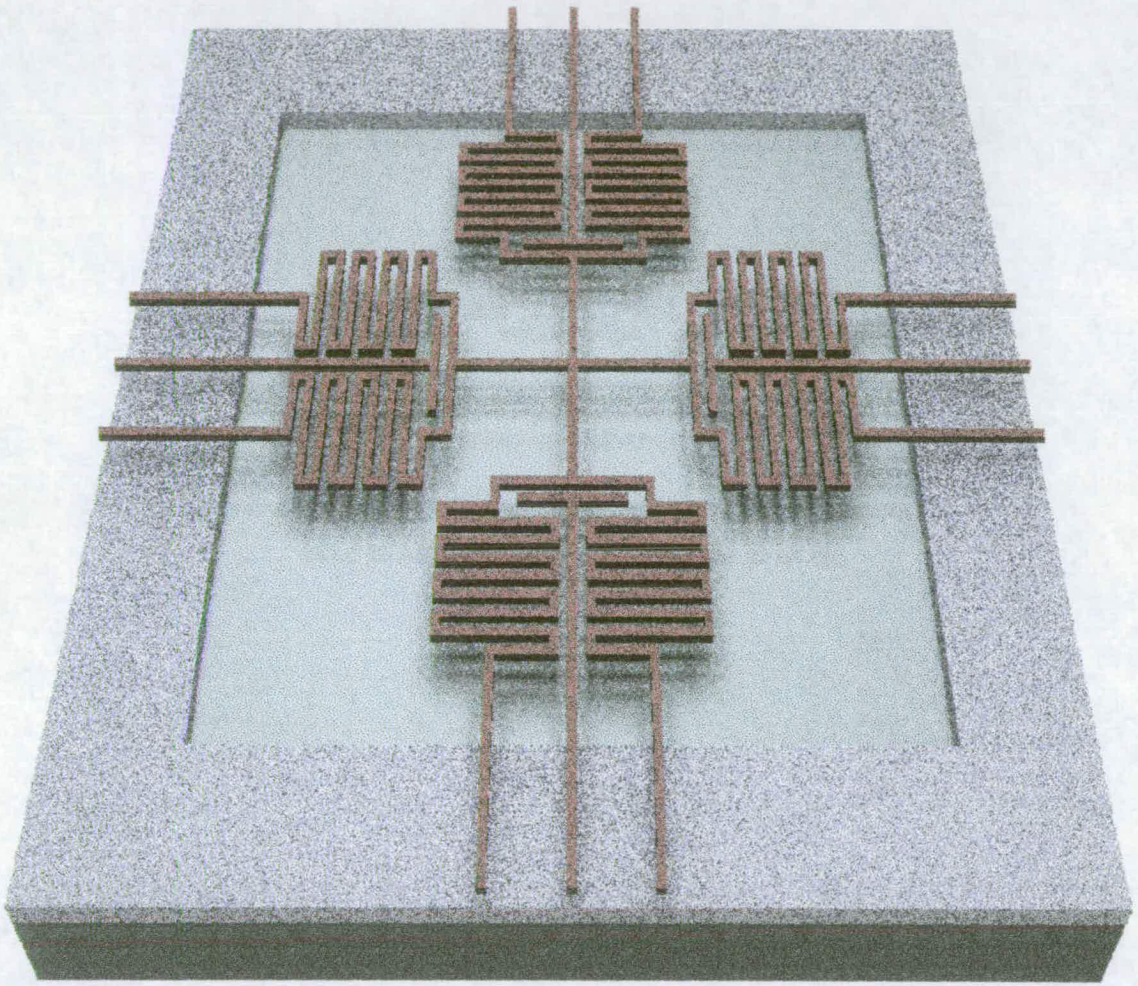
Figure 5.27: Representation of an x–y translator created using 3DTOP and POV–Ray.

can produce appropriate 3D representations of ICs manufactured using a particular process. The increasing significance of the choice of 3D representation as interconnect track aspect ratios increase was demonstrated, with the proviso that as aspect ratios continue to increase, IC processing will tend to involve more planarising steps, leading to increasingly planar IC topography.

The importance of determining parasitic capacitance values accurately has been further emphasised by demonstrating the effect that parasitic capacitances have on the behaviour of a simple circuit. The example circuit chosen was a single transistor circuit forming part of a spatial light modulator (SLM), which was expected to be particularly sensitive to parasitic interconnect capacitance. The effects of parasitic interconnect capacitances on its performance were explained, and conventional and 3D capacitance extraction techniques described and compared. In this case, whilst parasitic interconnect capacitances were shown to have a significant effect on circuit performance, the difference between the effects of capacitances extracted using conventional and 3DTOP techniques was not shown to be particularly significant, despite variation in extracted capacitance values of up to 32%. This was due to the large value of mirror charge storage capacitance designed into the circuit. However, the comparison of 3DTOP and conventional techniques highlighted the advantages and disadvantages of each. In particular, the 3DTOP technique is the more accurate approach, and allows for more flexibility than the conventional method. The conventional technique has the advantage of requiring less computing resource than the 3DTOP technique, and forms an integral part of an existing suite of design and simulation software. However, its accuracy depends on the complexity of the technology file used, and on the accuracy of the unit capacitance values.

Finally, 3DTOP has been shown to have applications in the field of visualisation and simulation of microelectromechanical structures, although further work is required to allow for MEMS which include structures such as cogs and gears, which must include lines in the x–y plane which are neither 45° nor Manhatten.

Chapter 6

Characterisation of Planarisation

6.1 Introduction

In the preceding chapters, the importance of topography in determining the character-istics of IC interconnect has been demonstrated. In the light of this, it is important to be able to practically assess the topography of an IC. Two methods commonly used to achieve this are *sectioning* and *surface profiling*. Sectioning involves breaking the sample along an appropriate axis and visually inspecting the exposed plane. This is a difficult process and obviously destroys the sample. Surface profiling involves using a stylus to measure the variation in surface height of a sample. Its use is limited to topo-graphies with horizontal feature sizes which are greater than the size of the stylus tip, and it provides no direct information regarding the the topography of layers below the surface. The drawbacks of these methods provide the motivation for the development of the test structure presented here, which can be used to determine the topography of an inter–layer dielectric (ILD) using electrical measurements.

Further motivation for the development of an electrical test structure to determine topography of certain layers is provided by the increasing importance of planarisation in IC manufacturing, since planarisation processes require characterisation. Planarisation decribes any process which results in the reduction of the severity of surface topography

of an IC. The method used here is planarisation of the ILD using chemical mechanical polishing (CMP). In this chapter, the benefits of planarisation are described, along with planarisation techniques. A description of the test structure is presented, along with simulation results, and the structure's robustness to poor global planarity is discussed. Experimental work is also described, and experimental results presented and compared with simulation results.

6.2 Planarisation

Planarisation involves the reduction of topography variations on the surface of a wafer. As feature sizes reduce, IC interconnect becomes increasingly dense, requiring smaller linewidths and increasing layers of metal. These developments lead to problems such as increasing difficulty in obtaining successful step coverage by deposited materials, increasingly significant interconnect parasitics and more stringent demands on photolithography tools. Planarisation of ILDs leads to improved step coverage and therefore increased circuit reliability, and also results in decreased interconnect resistance. Planarisation also prevents the formation of abrupt resist thickness variations, leading to greater tolerance of the decreasing depth of focus in lithography exposure tools [6]. Parasitic interconnect capacitances can also be reduced by planarisation [84] and this is of particular interest since the effect of interconnect capacitance on circuit performance has become much more important [21, 85] as device geometries have reduced.

There are several methods of planarisation, including thermal flow, bias–sputtered dielectrics, etchback, spin on glass and chemical mechanical polishing (CMP). CMP is emerging as the preferred method in industry [36, 73, 86], and is the technique for which the test structure described in this chapter has been developed.
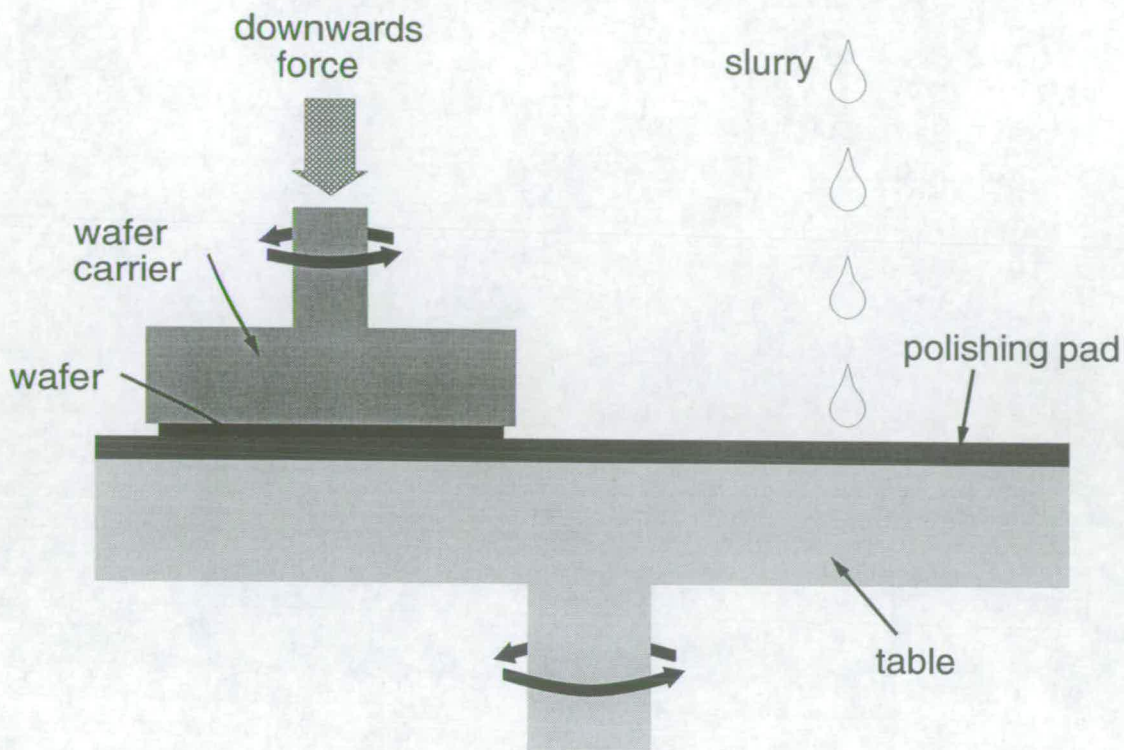
Figure 6.1: Schematic diagram of typical CMP tool.

6.2.1 Chemical Mechanical Polishing

CMP involves polishing away features on the surface of a wafer using a combination of mechanical abrasion and chemical reaction. A CMP tool usually comprises a rotating table and a rotating wafer carrier as shown in figure 6.1, although alternative designs are starting to appear [86]. A polishing pad is placed on the table and abrasive slurry is dripped onto the pad. The mechanical component of the process is contributed to by both the pad and the slurry, whilst the chemical component is a function of the slurry composition alone.

Two measurements are commonly used in connection with CMP. *Planarisation* refers to the local flatness of the wafer surface and is normally measured across a range of μm to mm. It indicates the flatness of a die. *Uniformity* refers to the variation in thickness of the dielectric across the entire wafer and is normally measured across a range of mm to cm [86]. The degree of planarisation can be defined as a percentage which relates to the amount by which the original topography has been reduced. For

example, 20% planarity describes a situation in which 20% of the original feature height has been removed by planarisation. Figure 6.2 shows increasing planarisation of an oxide layer.

Ideally, when a wafer is polished, the raised features on the wafer surface will be polished away eventually resulting in a completely flat surface, and the rate of removal of material will be constant across a wafer. In reality the situation is more complex since areas in between raised features may also be eroded. The raised features will normally be removed in preference to other areas, but this selectivity depends largely on the hardness of the polishing pad. Furthermore, the rate of material removal across the wafer is unlikely to be constant. Unfortunately, the equipment parameter requirements for successful local planarisation and across–wafer uniformity, both of which are desirable, conflict – good planarity requires a hard polishing pad, whereas good uniformity requires a soft pad. A compromise can be attained by using a combination of a hard pad with a soft pad underneath [86].

In addition to the hardness and the condition of the polishing pad, other variables can affect planarity and uniformity. These include the pressure with which the wafer is pressed onto the polishing pad, rotation speed of both the polishing pad and the wafer carrier, slurry composition and distribution across the pad, wafer carrier curvature, and temperature. The existence of so many variable parameters coupled with the fact that the state of the pad changes during its lifetime of between 200 and 1000 minutes of polishing [73] leads to difficulties in modelling the process.

6.2.2   Modelling, Characterising and Monitoring CMP

The effects of, and interactions between, the various parameters which affect the planarity and uniformity of the polished wafer are not yet fully understood [36, 87]. Research is being carried out to develop models for the process, but there is not as yet a complete and widely accepted model. Rather, industrial users of CMP tend to rely on characterisation and monitoring of the process. Characterisation normally takes the form

126

0%
planarity

increasing
planarity

100%
planarity
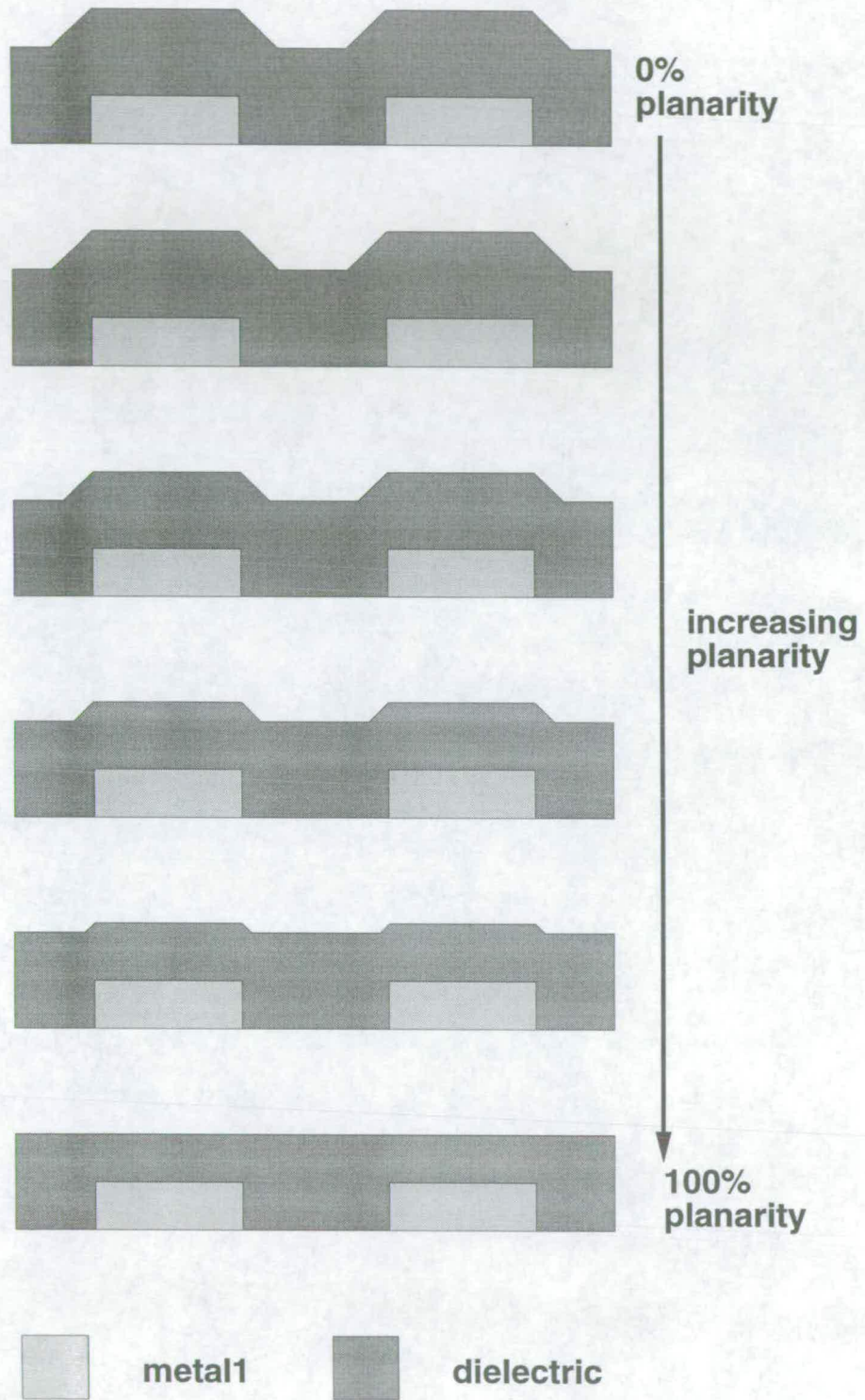
metal1   dielectric

Figure 6.2: Increasing planarity of dielectric over metal using CMP.

of physical surface measurements to determine planarity and layer thickness measurements to determine uniformity. It is now becoming common to monitor uniformity by measuring the remaining oxide thickness on the wafer during polishing, although such measurements can be distorted by the presence of both the slurry and the pattern on the wafer [86]. Measurements are normally taken at perhaps 9–13 sites to give a reliable measure of remaining oxide thickness and uniformity [73]. Planarity is not directly measured by this technique but its degree is sometimes inferred from oxide thickness, based on previously obtained data.

There is a need for some method of directly monitoring planarity rather than assuming a planarity based on the amount of oxide removed. The drawbacks of the commonly used techniques of sectioning and surface profiling were outlined in the introduction to this chapter. Some work has been done on determining planarity using an optical method [88], but is as yet inconclusive. The test structure described in this chapter can be used to monitor planarity of an ILD and has applications in characterisation of CMP processes. Determining ILD topography using this test structure is a non–destructive technique whose accuracy does not depend on the interconnect feature size, although it does require further processing following the CMP process step before measurements can be made.

6.3 Test Structure

The basic test structure which has been developed consists of two identical metal combs, separated by a layer of dielectric and offset from each other by a specific amount. The capacitance between the combs depends on their degree of overlap and the planarity of the inter–metal dielectric between them, and this property can be used to find the dielectric planarity if a set of structures of known and varying offset is available. The layout of a basic structure is shown schematically in figure 6.3 with an offset between the two combs of 1μm. Each comb has 100 teeth which are each 1mm long, 3μm wide and on a pitch of 6μm. To determine the degree of planarity of the dielectric

100 teeth per comb

1mm

3μ

1μ

3μ

■ metal1   ▦ metal2
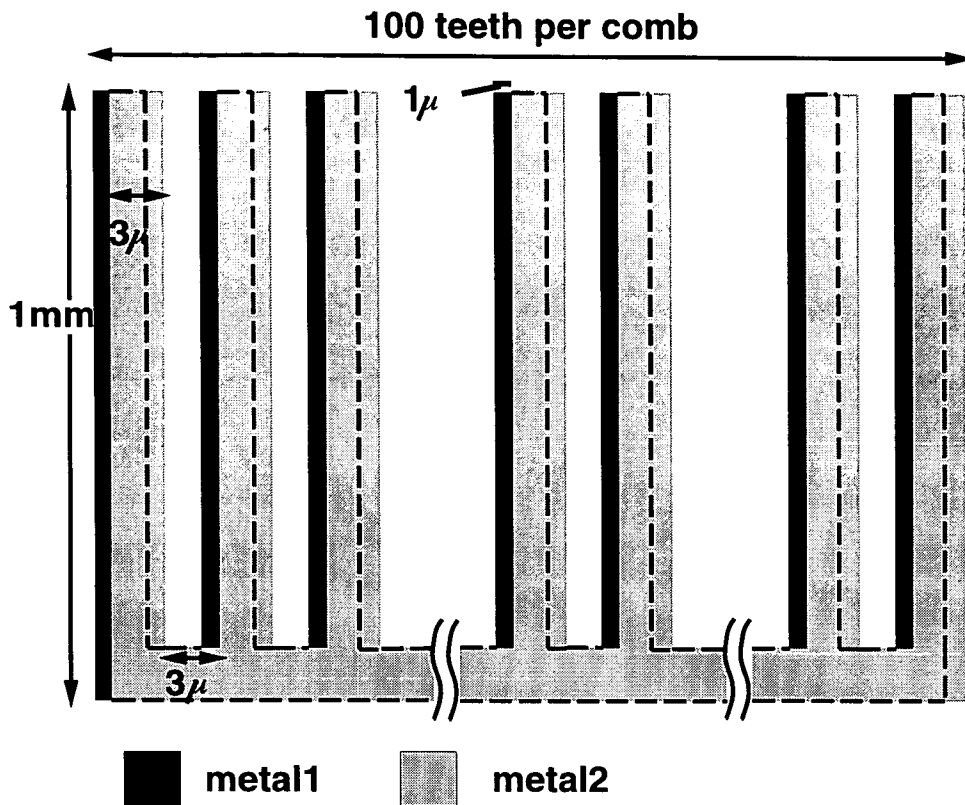
Figure 6.3: Schematic diagram of the basic test structure with an offset of 1μm between the two metal combs.

separating the two metal layers a set of such structures is required, with the upper comb progressively offset from the lower comb as schematically illustrated in figure 6.4. To be able to extract the planarity of the dielectric it is important to ensure that the offsets between the combs cover a range which encompasses both complete overlap and zero overlap.

Figure 6.5 shows the layout of an entire set of test structures for which the upper comb has been progressively offset from the lower comb by 0.2μm, covering the range from 0μm to 5.8μm. This range of offsets ensures that the measurement is robust to misalignments between metal1 and metal2, with the range of overlaps illustrated in figure 6.4 always available for measurement. Note that due to the 0.2μm increment and random nature of the misalignment between metal1 and metal2, the structures available for extracting the degree of planarity may be offset by up to 0.1μm from those shown in figure 6.4, but the range of overlaps required will still be encompassed.
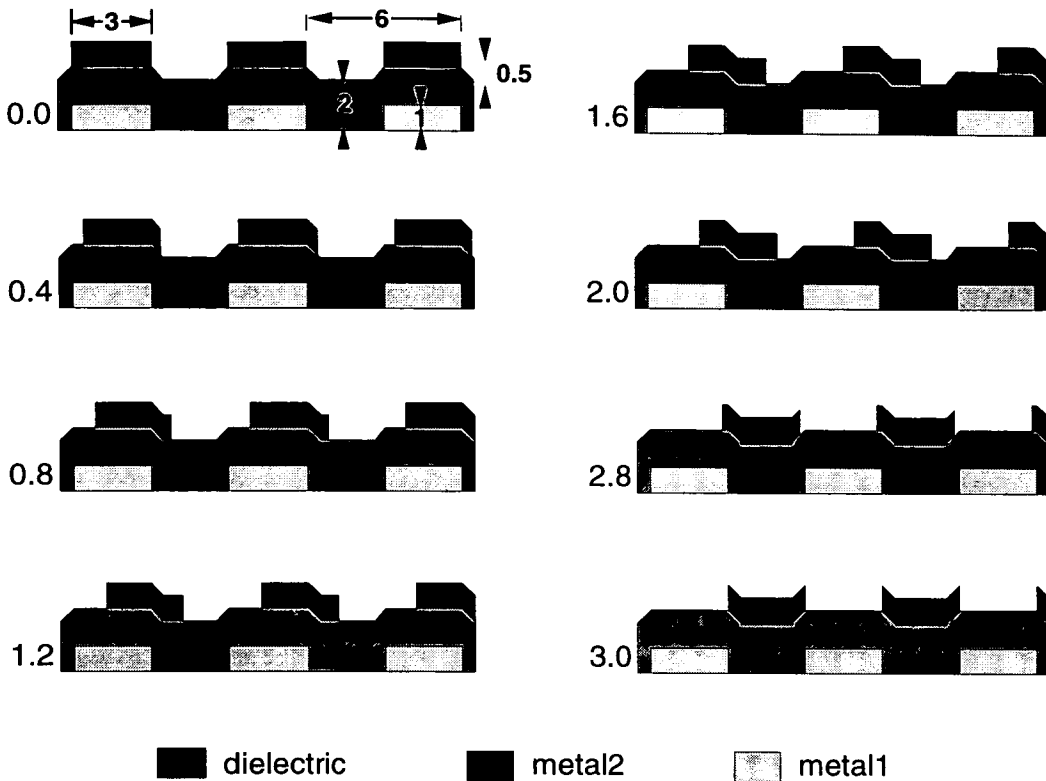
Figure 6.4: Cross sections of part of the structure showing increasing offset.

6.4   Simulation

In order to determine the effect that ILD topography would be expected to have on the capacitance between the metal comb structures, 2D simulations were performed to produce graphs of capacitance vs offset between the combs for dielectric planarities of 0% to 100% in increments of 10%. These simulations were performed using TMA's Raphael software, requiring 176 separate simulations to produce each set of curves. In order to reduce the time required to perform these simulations, a small section of the structure comprising a cross section of 10 teeth from each metal layer was simulated. The 2D simulations assume a third dimension of thickness 1 unit (in this case 1μm), so the results for this small section were multiplied by 1000 to account for the length of the teeth, and by 10 to account for the number of teeth in each comb (100). This approach did not take into account the effect of the bar connecting the teeth together on each comb, but the effect of this on capacitance was assumed to be negligible. Using this approach, the amount of time required to perform the simulations was greatly reduced

130

5.0	5.2	5.4	5.6	5.8
4.0	4.2	4.4	4.6	4.8
3.0	3.2	3.4	3.6	3.8
2.0	2.2	2.4	2.6	2.8
1.0	1.2	1.4	1.6	1.8
0.0	0.2	0.4	0.6	0.8

▨ **Probe pad to metal1**
■ **Probe pad to metal2**

Test structure – number indicates offset in microns
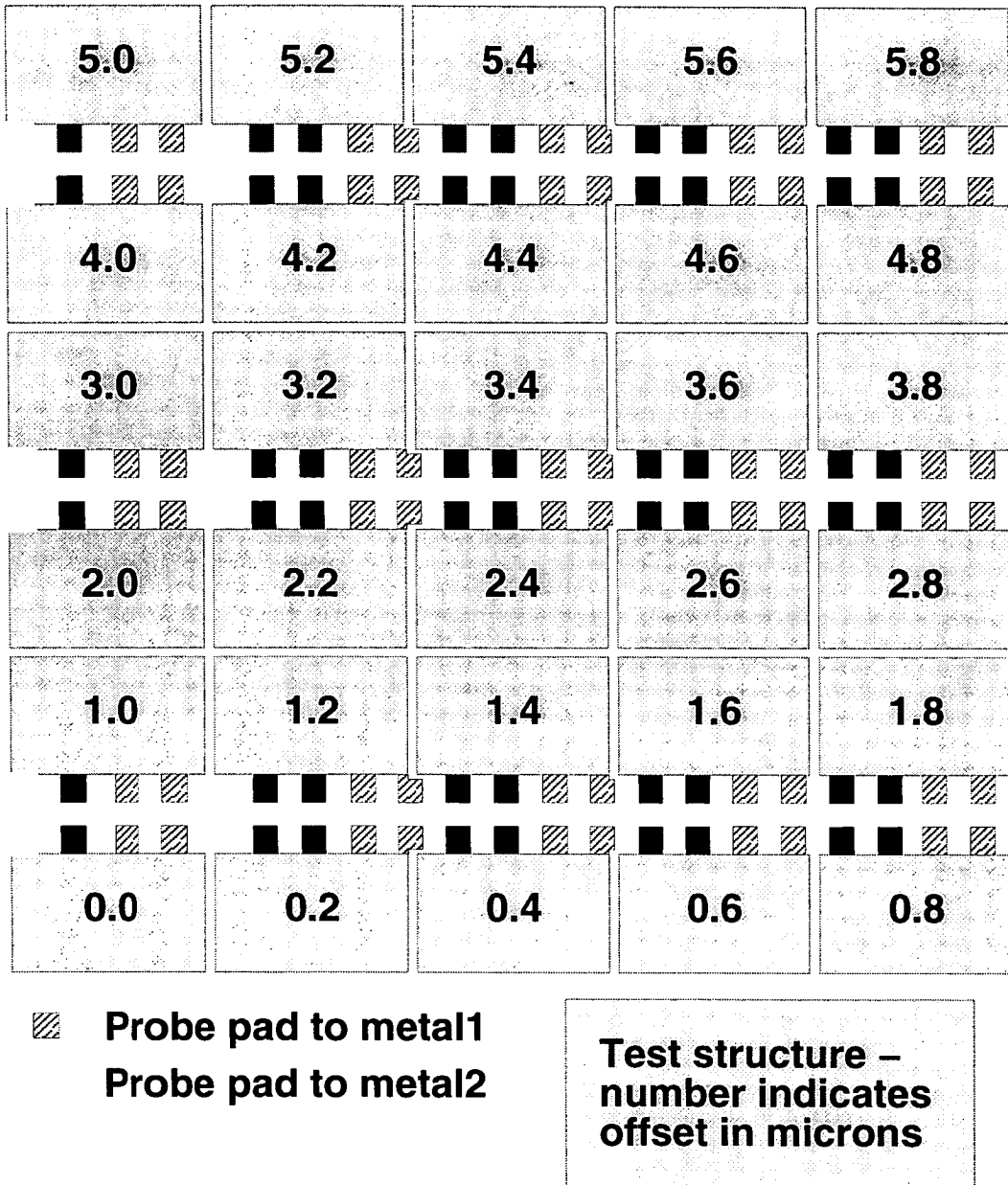
Figure 6.5: Layout of a complete set of test structures.

131
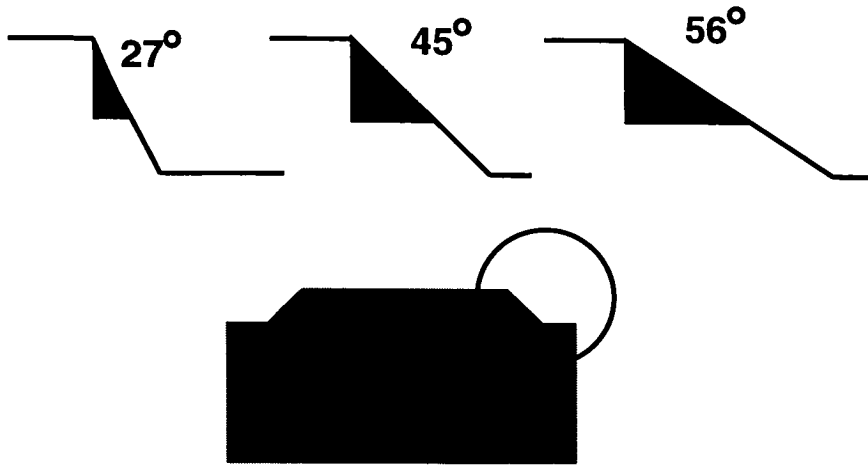
Figure 6.6: The three different slopes for which simulations were carried out.

– in fact, to simulate the capacitance of this smaller section required only 2 minutes on a Sun IPX workststation.

Data describing the structure being simulated was generated semi–automatically by using equations with variable parameters in the Raphael input file, with 15,000 gridpoints used in each simulation. The dielectric step coverage over the metal was assumed to have a constant slope. Simulations were performed for dielectric step slopes of $27°$, $45°$ and $56°$ to the vertical, as shown in figure 6.6. The results of these simulations are shown in figures 6.7, 6.8 and 6.9

The shape of these curves is readily explained. With increasing planarity, the oxide thickness directly above metal1 decreases as the raised oxide is polished away. This accounts for the change in capacitance at zero offset for different degrees of planarisation, and to a lesser degree for other offsets. However, the shape of the curves is dominated by the shape of the inter-metal dielectric, which is determined by the planarity. It can be seen from figures 6.7 to 6.9 that with increasing planarity, the gradient of the central part of the curves decreases progressively from a positive to a negative slope. The shapes of the curves vary slightly depending on the slope of the oxide step, but the general trend remains the same.

To emphasise the fact that the shape of the slope depends far more on the planarity

132
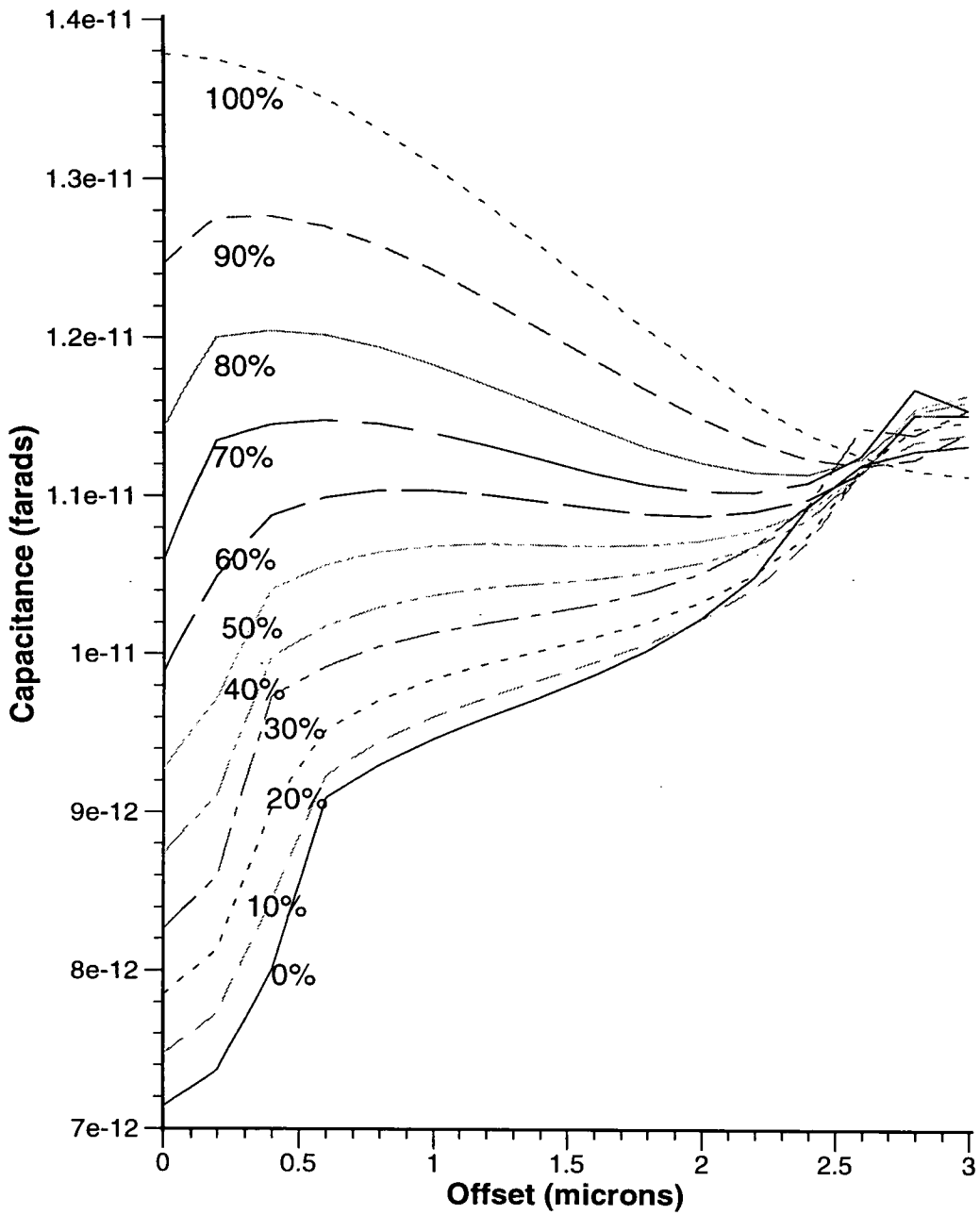
Figure 6.7: Set of curves showing capacitance vs offset for an oxide slope of 27°, with planarities ranging from 0% to 100%.

133
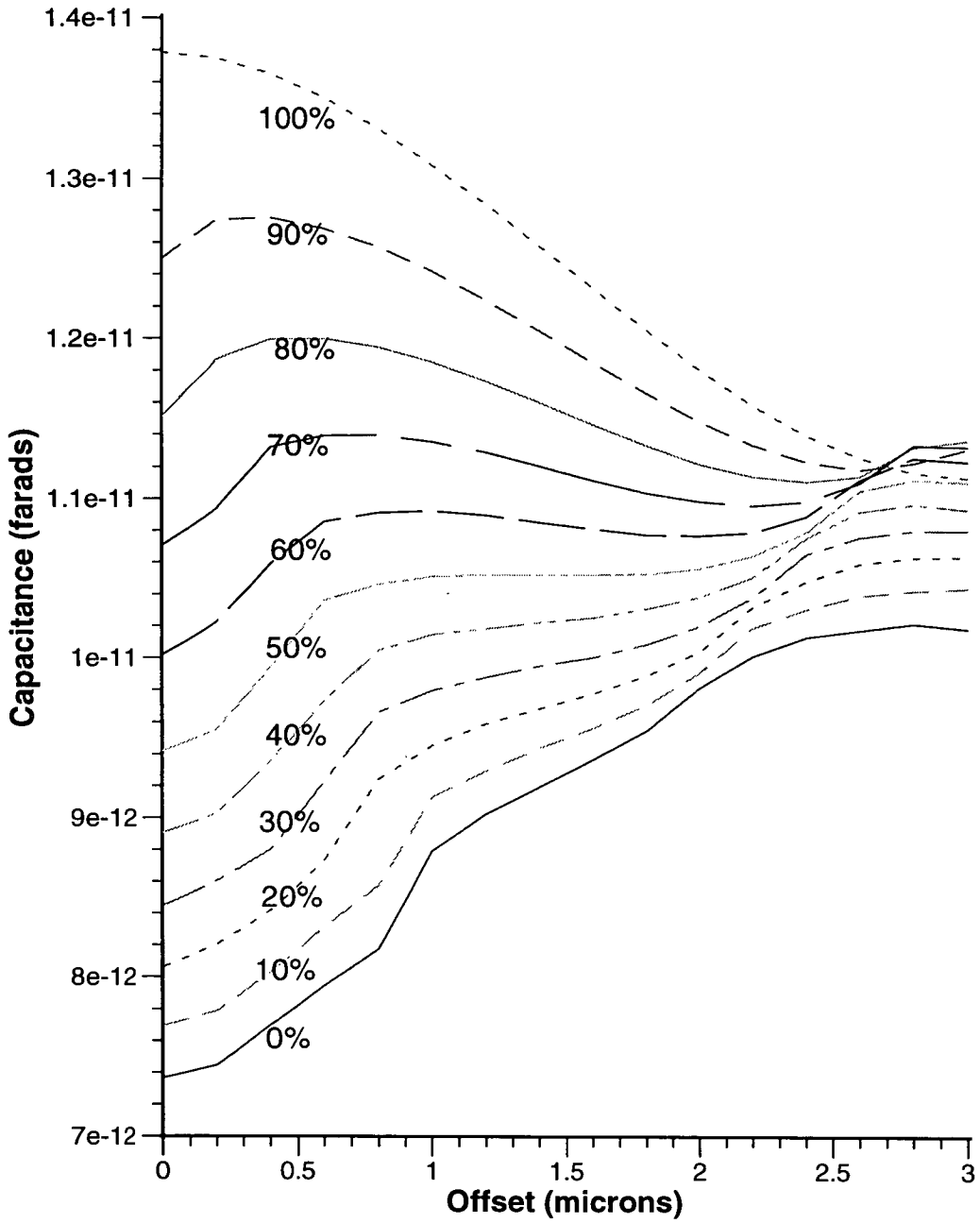
Figure 6.8: Set of curves showing capacitance vs offset for an oxide slope of 45°, with planarities ranging from 0% to 100%.
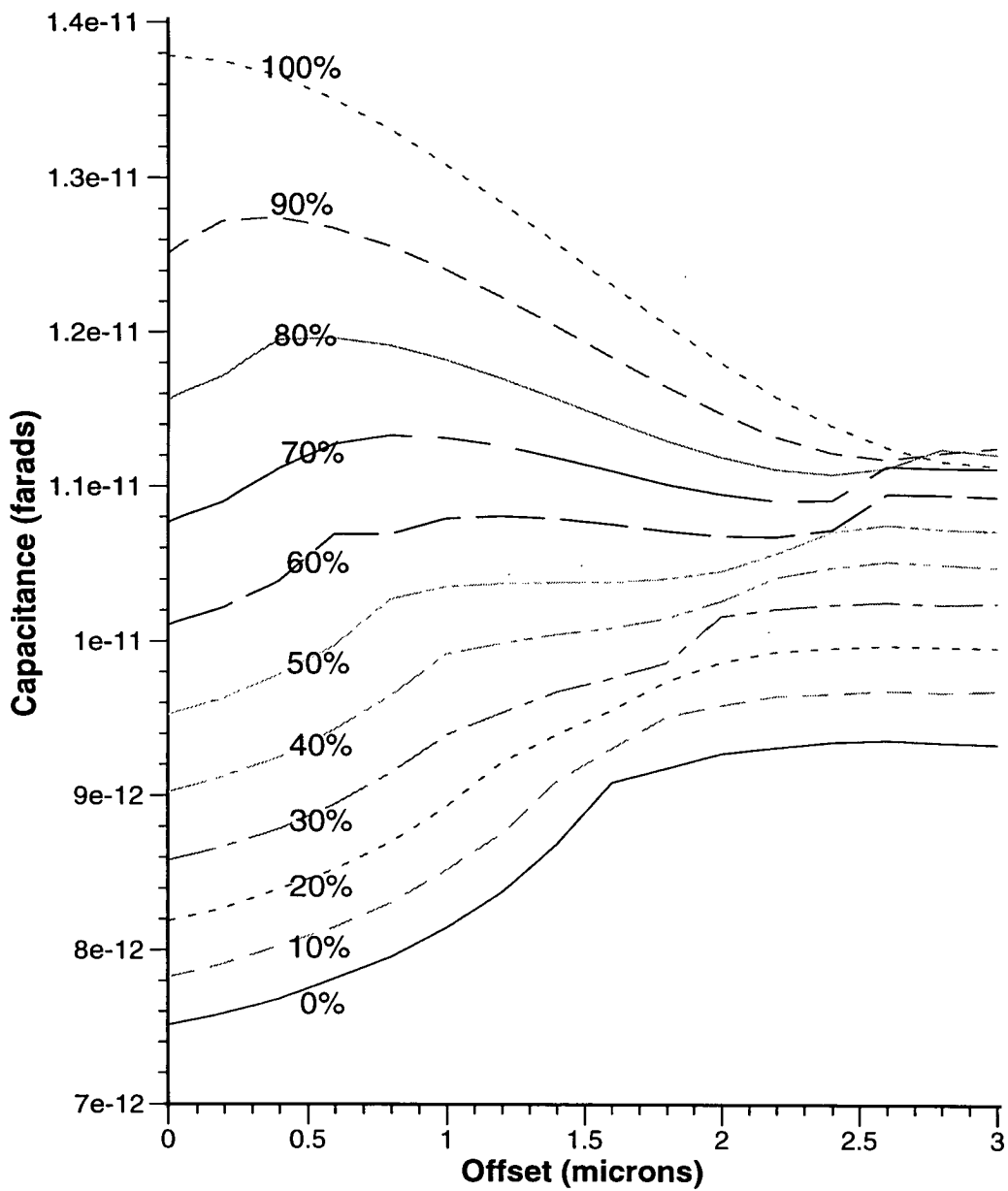
Figure 6.9: Set of curves showing capacitance vs offset for an oxide slope of 56°, with planarities ranging from 0% to 100%.
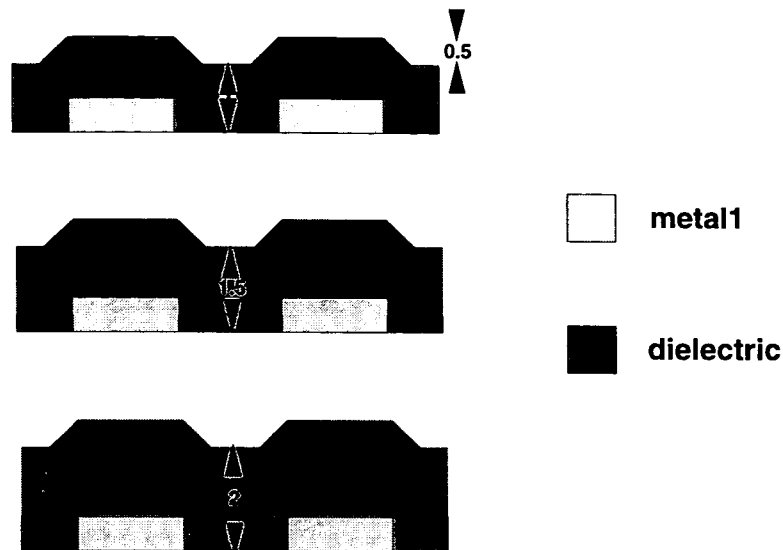
Figure 6.10: Three different oxide thicknesses, all 50% planar.

of the dielectric than on its thickness, curves have been plotted of capacitance vs offset for oxides of different thicknesses but a constant planarity as shown in figure 6.10. The resulting curves are shown in figure 6.11. Although the oxide thicknesses differ, the shapes of the curves are very similar. This ensures that the test structure can be used to develop processes where the oxide thickness is not known exactly.

6.5   Sensitivity to Oxide Thickness Variation

The test structure presented here has been developed with the intention of determining local planarity, and the assumption has been made that uniformity will be constant across a set of structures. However there will always be some degree of non–uniformity across a wafer, and therefore across a die, so it is important to know how robust the structure is to such variations.

In order to investigate the sensitivity of the structure to oxide thickness variation across a die, further simulations were performed. Oxides of thickness 1μm and 2μm were simulated with planarities of 0%, 50% and 100%. The oxide thickness was then varied by ±1% and ±5% whilst maintaining the planarities. The results of these
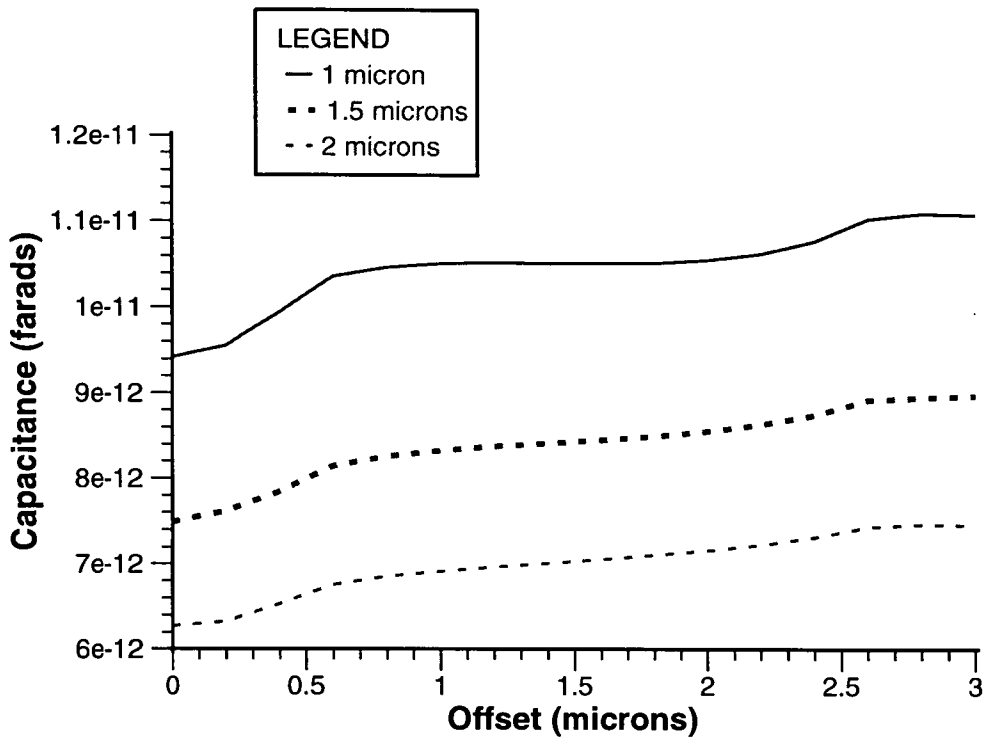
Figure 6.11: Capacitance vs offset for three oxide thicknesses, all 50% planar .

Planarity(%)	1μm$\pm1\%$	1μm$\pm5\%$	2μm$\pm1\%$	2μm$\pm5\%$
0	0.38	2.05	0.64	2.96
50	0.49	2.49	0.67	3.29
100	0.67	3.34	0.74	3.69

Table 6.1: Percentage change in capacitance with oxide thickness variations of 1% and 5%, for IC planarities of 0%, 50% and 100%.

simulations are shown in figures 6.12 to 6.17, and are summarised in table 6.1.

Typical uniformities quoted by polisher manufacturers are now less than 5% across a 200mm wafer with an exclusion area of 5 or 6mm around the wafer edge [86]. This translates to a uniformity of less than 0.2% across a 5mm by 5mm die containing all 30 structures.

Inspection of figures 6.12 to 6.17 indicates that the test structure is certainly tolerant of a variation in oxide thickness of up to 2% across a die, since any capacitance values

137
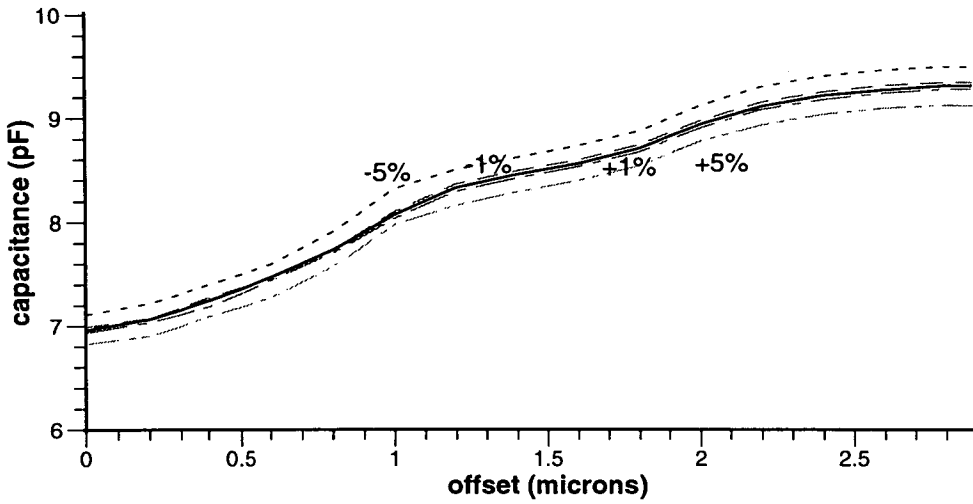
Figure 6.12: Simulated capacitance vs offset between combs for a 0% planar, 1μm thick oxide, with variations in oxide thickness of $\pm1\%$ and $\pm5\%$.
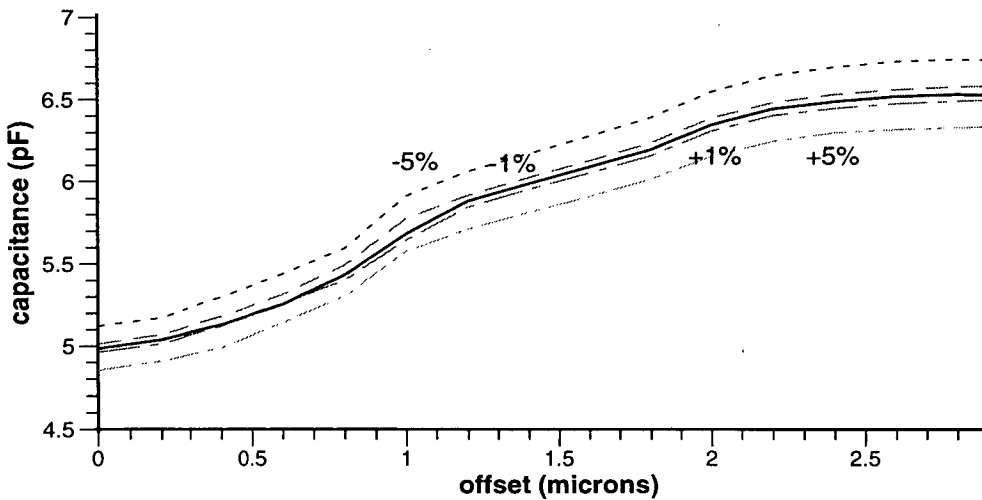
Figure 6.13: Simulated capacitance vs offset between combs for a 0% planar, 2μm thick oxide, with variations in oxide thickness of $\pm1\%$ and $\pm5\%$.

138
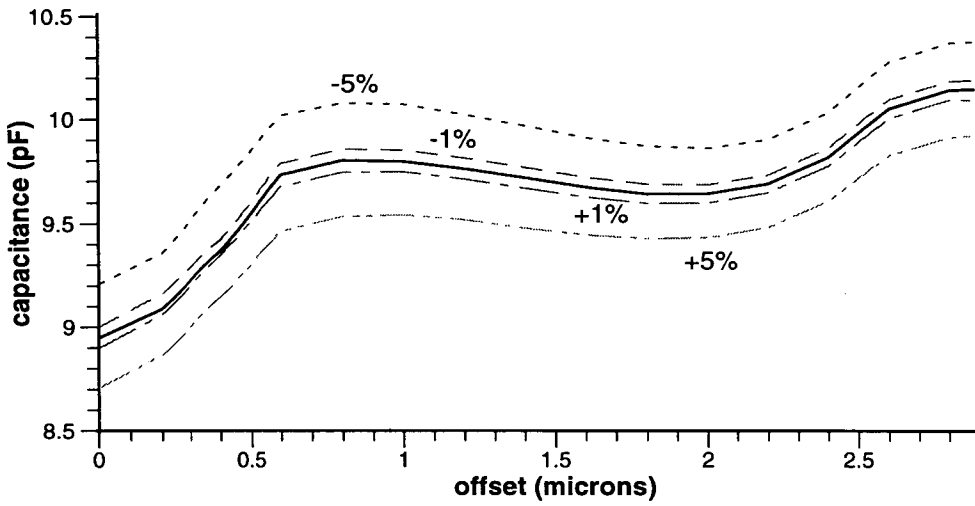
Figure 6.14: Simulated capacitance vs offset between combs for a 50% planar, 1μm thick oxide, with variations in oxide thickness of $\pm1\%$ and $\pm5\%$.
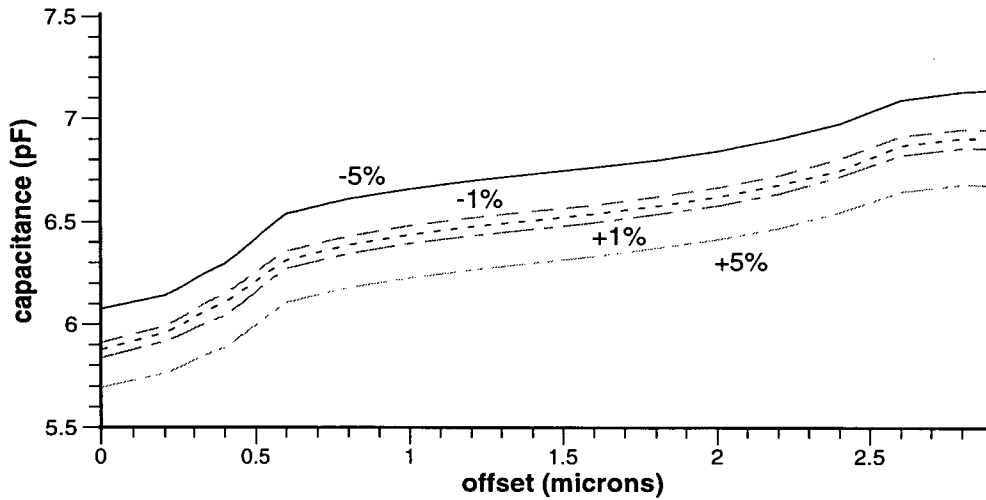
Figure 6.15: Simulated capacitance vs offset between combs for a 50% planar, 2μm thick oxide, with variations in oxide thickness of $\pm1\%$ and $\pm5\%$.
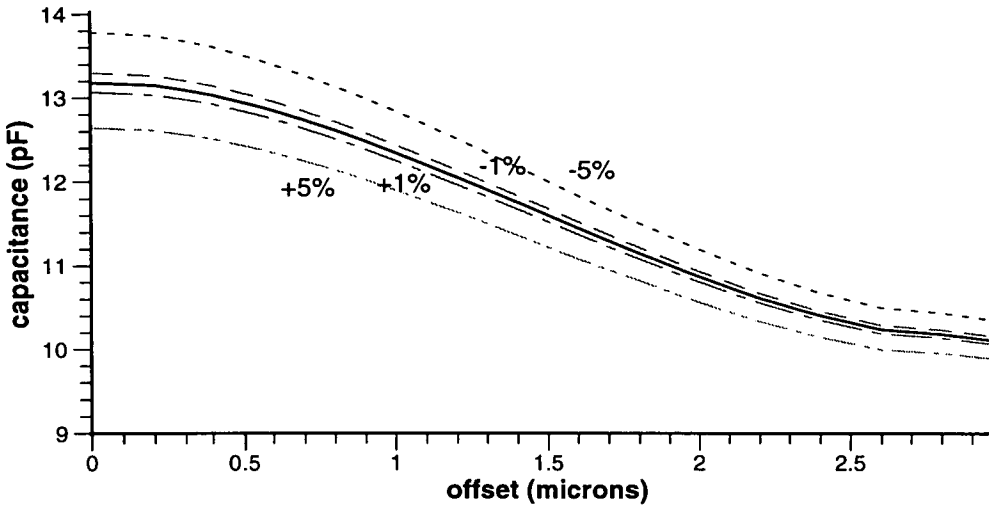
Figure 6.16: Simulated capacitance vs offset between combs for a 100% planar, 1μm
thick oxide, with variations in oxide thickness of $\pm 1\%$ and $\pm 5\%$.
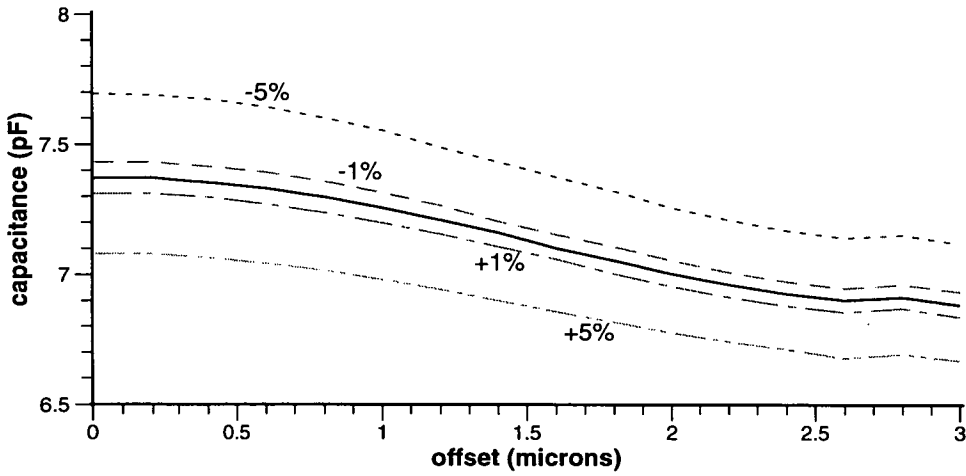
Figure 6.17: Simulated capacitance vs offset between combs for a 100% planar, 2μm
thick oxide, with variations in oxide thickness of $\pm 1\%$ and $\pm 5\%$.

varying between the +1% and -1% curves would produce very little variation in the overall shape of the graph. A variation in oxide thickness of 10% or even in some cases 5% could lead to a very different graph to that expected, but such a poor uniformity lies well outside the likely quoted values.

6.6 Experimental Work

In order to confirm the results obtained by simulation, experimental work was carried out. Five wafers with different degrees of planarisation were fabricated. Four of the wafers were processed conventionally, with planarities ranging from 0% to 100%. Due to the uncharacterised state of the polishing equipment, and non–uniform oxide deposition, obtaining a 100% planar sample whilst retaining an acceptable uniformity across the wafer proved to be impossible using conventional processing. An alternative approach was therefore taken to obtain the 100% planar sample, using damascene processing. These two approaches are described in the following sections.

6.6.1 Conventional Processing

For the four conventionally processed wafers, the procedure used is as follows. A layer of oxide was deposited on the bare silicon wafer, followed by a layer of silicon nitride. The nitride was used because of the high selectivity of etch between aluminium and nitride. Aluminium was deposited using a Balzers sputtering system, to a thickness of 1μm. The metal was then coated, patterned and etched back down to the nitride.

Next, oxide was deposited on the metal and nitride using Electron Cyclotron Resonance (ECR) [89]. This method was chosen since it produces a relatively uniform oxide deposition and does not involve any high temperature steps which could cause hillock formation in the aluminium. ECR deposition involves the creation of an intense plasma confined by two powerful electromagnets. The wafer is electrically isolated from the

141

rest of the system, and can be heated and RF biased [90]. When a bias is applied to the wafer, some of the deposited material is sputtered off during the deposition. This results in the removal of oxide deposited along the top edges of metal lines, which could develop into overhangs [91], and therefore allows void–free gap filling. It also results in a characteristic oxide topography above the metal lines, as sloping sides are formed above the underlying metal steps. As the deposition and sputtering time increases, the oxide topography changes as oxide is removed by sputtering, and the resulting sloping sides gradually approach each other to form first a point and eventually a completely planar surface [91]. If no bias is applied to the wafer, no sputtering occurs and a con-formal layer of oxide is deposited. This mode of deposition may result in the formation of voids in the trenches between metal lines [91], but the rate of oxide deposition is increased [90].

The conditions used for ECR deposition were chosen such that the trenches between the aluminium tracks would be completely filled, whilst ensuring a sufficiently thick oxide for the CMP step which followed. The oxide was first deposited in the *planar* mode, which involves sputtering, with pressure = 7mTorr, RF power = 280W and table height = 80cm. This table height, which corresponds to having the wafer as far from the plasma source as possible, was chosen to ensure that the oxide deposition was as uniform as possible. The *planar* deposition was followed by a 1 hour *non–planar* deposition, in which no sputtering occurs, to produce the required oxide thickness.

Following a via etch, 3 of the 4 wafers were polished using a Logitech PS2000 system, with a slurry of alkaline colloidal silica and an expanded polyurethane pad. The pad was rotated at 30 rpm with a downward pressure on the wafer of 0.0026 Kg/mm^2. The wafer carrier was not actively driven, but was left to rotate due to interaction with the rotating table and pad. Wafer 1 was not polished, wafer 2 received a 5 minute polish, wafer 3 a 10 minute polish and wafer 4 a 24 minute polish. After polishing, an interferometer (in this case a Nanospec instrument) was used to take oxide thickness measurements across each wafer to determine the global uniformity of the dielectric. These measurements were taken at the corner of each die as shown in figure 6.18.
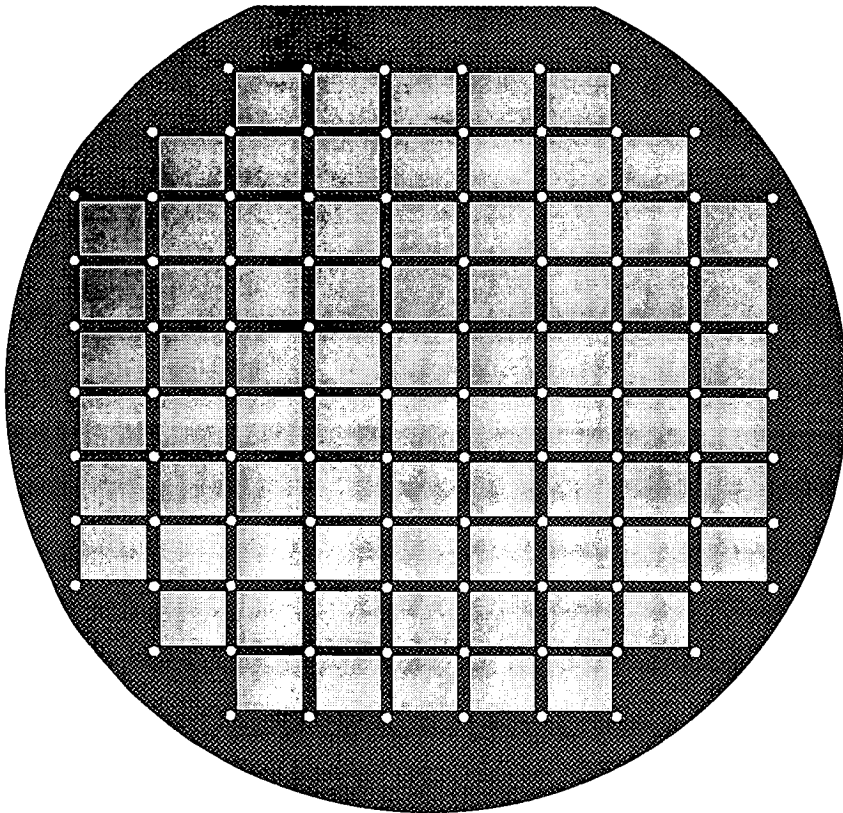
Figure 6.18: Wafer schematic - white dots show oxide thickness measurement sites.
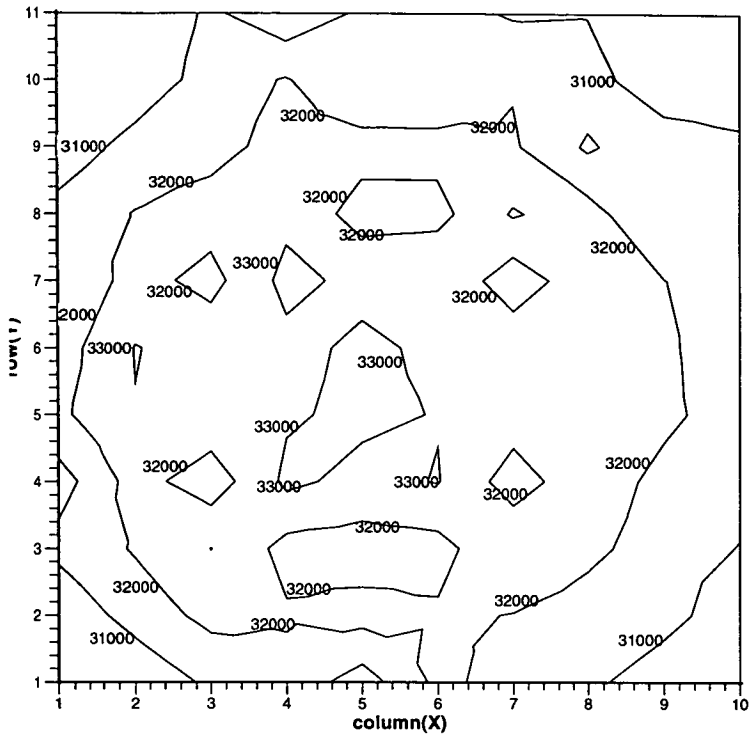
Figure 6.19: Oxide thickness contour map of wafer 1 (no polish).
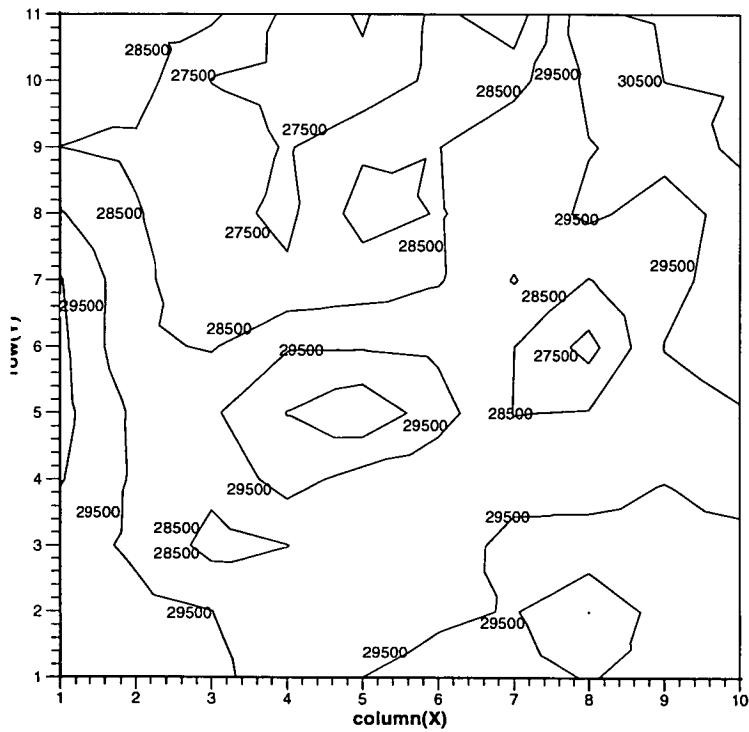
Figure 6.20: Oxide thickness contour map of wafer 2 (5 minute polish).
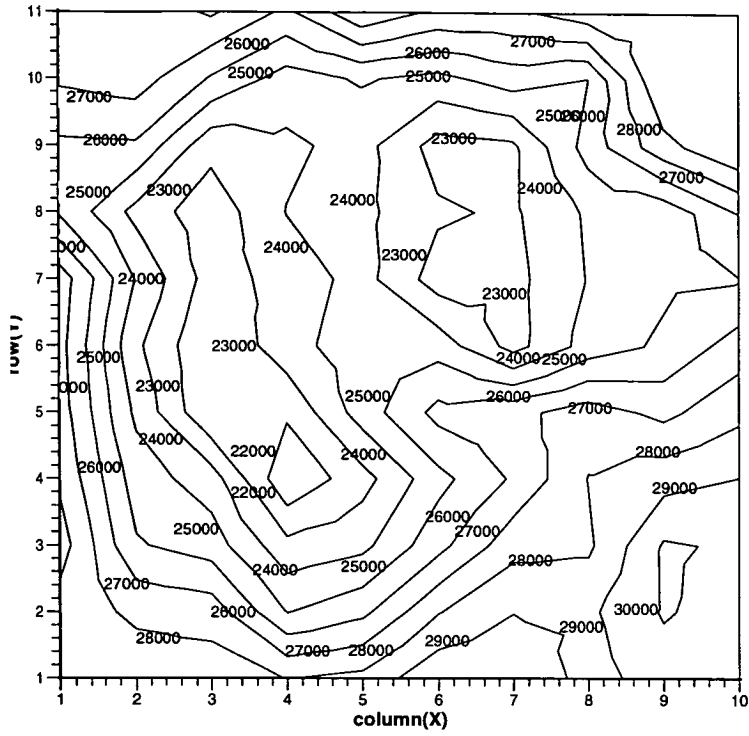
Figure 6.21: Oxide thickness contour map of wafer 3 (10 minute polish).
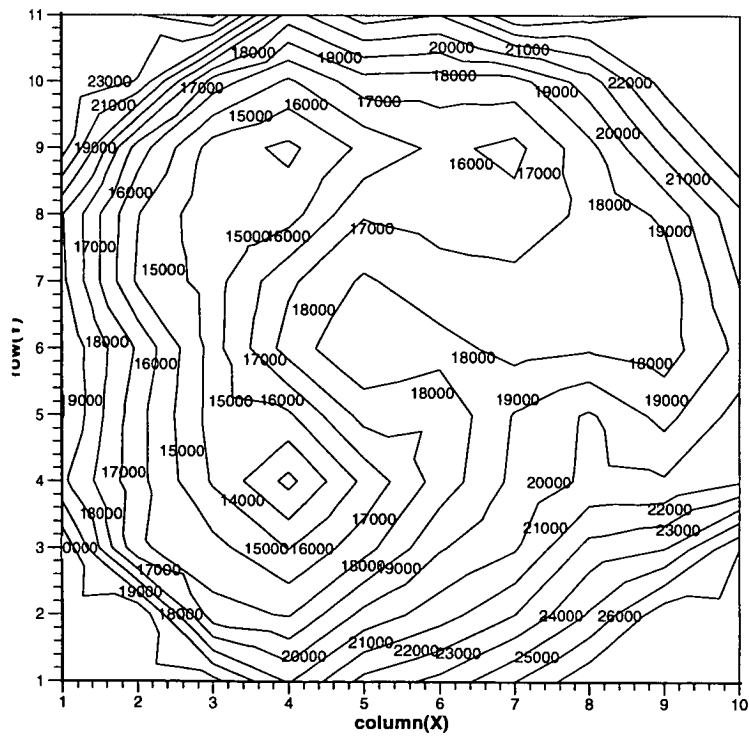
Figure 6.22: Oxide thickness contour map of wafer 4 (24 minute polish).

Figures 6.19 to 6.22 show oxide thickness contour maps produced using BBN/Cornerstone [92]. Contours are shown at every 1000Å (0.1μm). Figure 6.19 shows that the oxide is non–uniform after ECR deposition, prior to any polishing. Wafer 2's contour map has a different shape, but the uniformity is no worse than that on wafer 1. Wafer 3, which has had 10 minute's polishing shows worsened uniformity, and wafer 4 exhibits poor uniformity - only a very few sites exist where the oxide thickness variation across a die may be expected to be less than 5%, and in most cases it is in the region of 10%. These wafer maps indicate that the oxide is not being polished uniformly, with a maximum measured oxide thickness variation of 0.025μm on wafer 1, 0.35μm on wafer 2, 0.8μm on wafer 3 and 1.2μm on wafer 4. The rate at which oxide was removed was found to be greatest at the edges of the wafers. This is to be expected, and accounts for the 'exclusion zone' around the edge of a wafer when uniformities are quoted.

Topographical measurements of the wafer surface were made at individual sites, using a Dektak surface profiler, to assess the degree of local planarity. These measurements indicated that the maximum feature height on the wafers after polishing was 0.5-0.65μm on wafer 2, 0.2-0.5μm on wafer 3 and 0.02-0.06μm on wafer 4. The Dektak results are only useful as an indication of the relative planarity of the wafers since the 12μm stylus used was larger than the individual features on the wafer surface. Sample profiles obtained for wafers 2, 3 and 4 are shown in figures 6.23, 6.24 and 6.25.

Figures 6.23 and 6.24 indicate a metal line pitch of around 7μm, rather than the 6μm expected. This is likely to be caused by a Dektak scan which is not quite perpendicular to the metal tracks. Figure 6.25 shows trenches at half the pitch expected. This could be due to uneven polishing at the junction between the planar and non–planar deposited oxides, but it is difficult to properly investigate such small details with the relatively large Dektak stylus. The important information to be gained from this trace is the fact that the maximum feature height is very small, so the planarity is near to 100%.
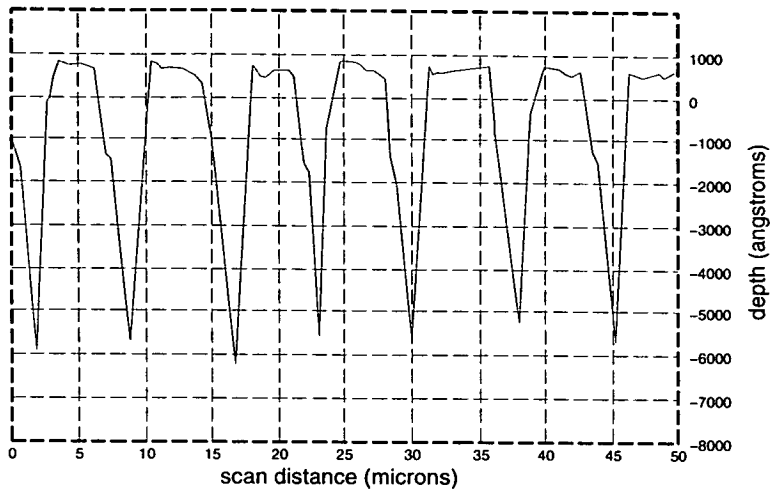
Figure 6.23: Dektak surface profile of oxide on wafer 2.
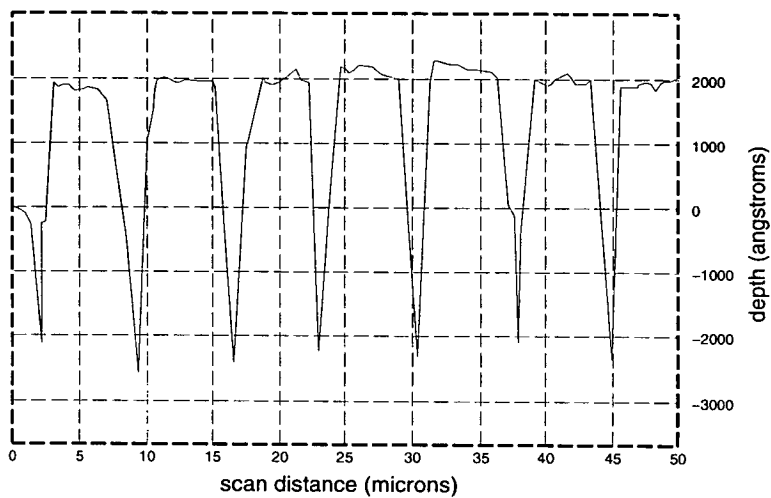
Figure 6.24: Dektak surface profile of oxide on wafer 3.
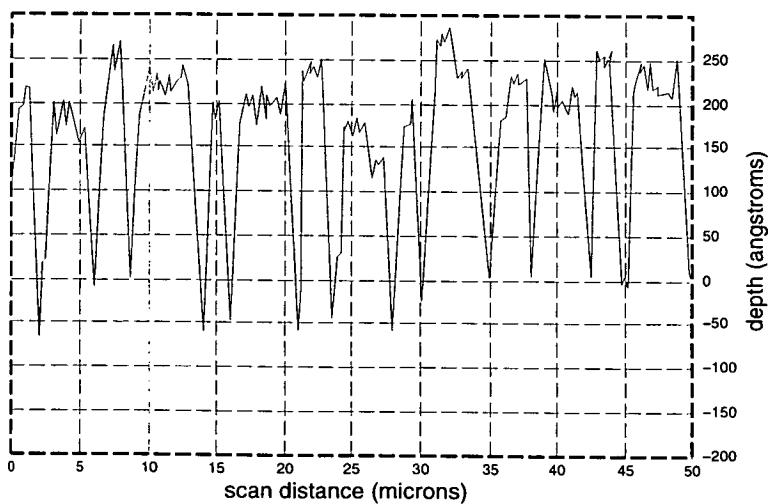
Figure 6.25: Dektak surface profile of oxide on wafer 4.

147

6.6.2 Damascene Processing

Due to the poor uniformity of wafer 4, processed using conventional processing, *damascene processing* was used in order to obtain a 100% planar sample with acceptable wafer uniformity. Damascene processing involves etching trenches into planar oxide, then depositing metal to fill the trenches completely. Metal which has been deposited on the oxide between the trenches is then polished away using CMP [6]. Further oxide is deposited on top of the metal filled trenches, producing the 100% planar situation shown in figure 6.2.

This approach should produce better uniformity across the wafer than the standard dielectric planarisation method previously described. Less time is required when polishing metal than is needed to produce a 100% planar oxide when polishing the ILD. In addition, the pressure applied to the wafer carrier is less for damascene processing than for dielectric planarisation, which improves uniformity across a die [36].

The damascene process used on wafer 5 will now be described. Starting with a bare silicon wafer, over 2μm of thermal oxide was deposited, followed by 0.5μm of non–planar mode ECR oxide. This was again deposited using a table height of 80cm to ensure that the deposition was as uniform as possible. The oxide was patterned with the inverse metal1 mask, and etched to a depth of 0.5μm. 1μm of aluminium was sputtered onto the wafer, filling the trenches and completely covering the oxide in between. The aluminium was polished back until level with the underlying oxide using the Logitech system, with a much reduced downwards force of 0.00065Kg/mm^2, a pad rotation of 30 rpm and a proprietary slurry.

Damascene processing is not without problems, which include *dishing* and *erosion*. Dishing refers to the situation where the softer metal in the trenches is removed below the level of the surrounding oxide, as shown in figure 6.26. Erosion occurs when the whole area of metal interconnect inlaid into oxide is polished away such that some oxide is removed along with the metal, resulting in a thinned oxide and shallower metal–filled

148
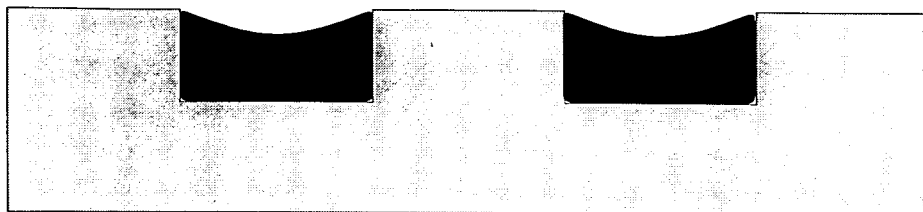
Figure 6.26: Metal tracks exhibiting *dishing*.
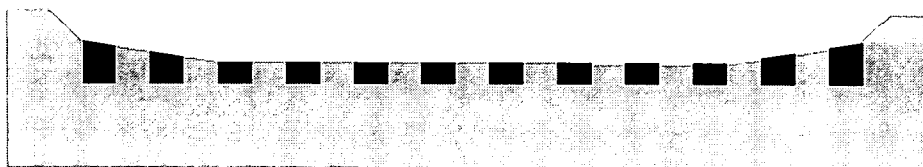
Figure 6.27: Metal tracks and oxide exhibiting *erosion*.

trenches, as shown in figure 6.27.

Both of these effects were minimised by reducing the downward pressure on the wafer during polishing. Furthermore, wafer 5 was polished until around 1/3 of the die on the wafer were completely clear of metal outside the trenches as shown in figure 6.28. This left the remaining die *under–polished*, in that some of the metal lying between the trenches remained as shown in figure 6.29. Although the number of die available for measurement was reduced, this approach ensured that those die which were clear of metal in between the trenches would not be over polished, minimising the probability of dishing and erosion occurring.

At this point, a further 0.5μm of ECR oxide was deposited, and vias patterned and etched. Measurements were taken using the Dektak to determine the extent of the dishing and erosion, both of which were found to be around 0.03μm. These measurements were taken after the deposition of the oxide so as not to damage the softer metal in the trenches with the Dektak stylus. Figure 6.30 shows a Dektak surface profile showing the extent of the dishing. Finally, 0.5μm of aluminium was deposited, patterned and etched to form the upper combs.
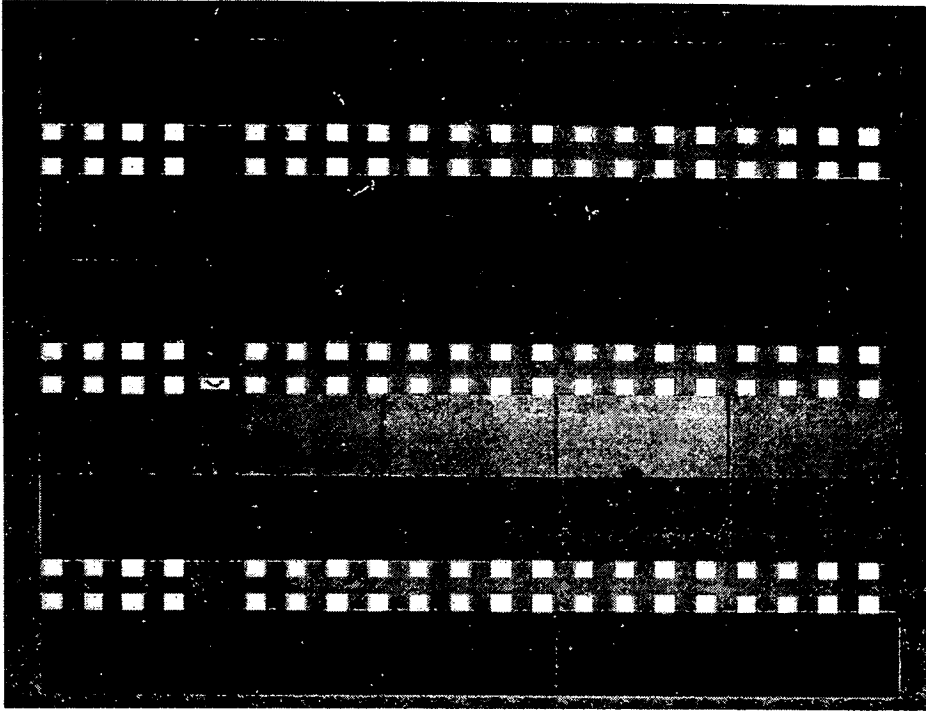
Figure 6.28: A die exhibiting complete removal of excess metal by CMP.
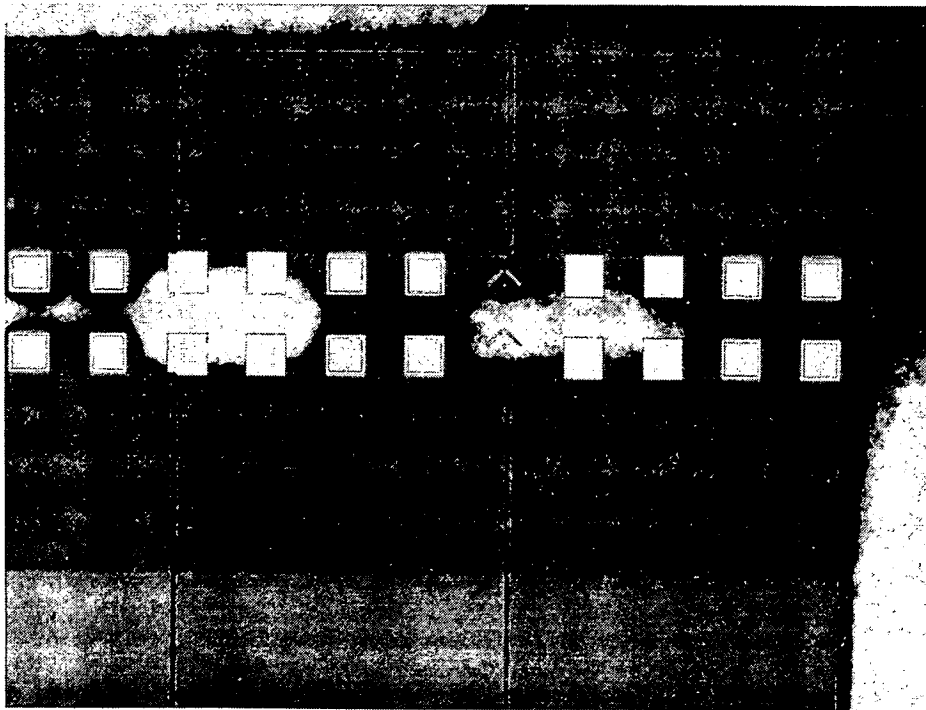
Figure 6.29: Part of a die showing residual metal1 due to under polishing.
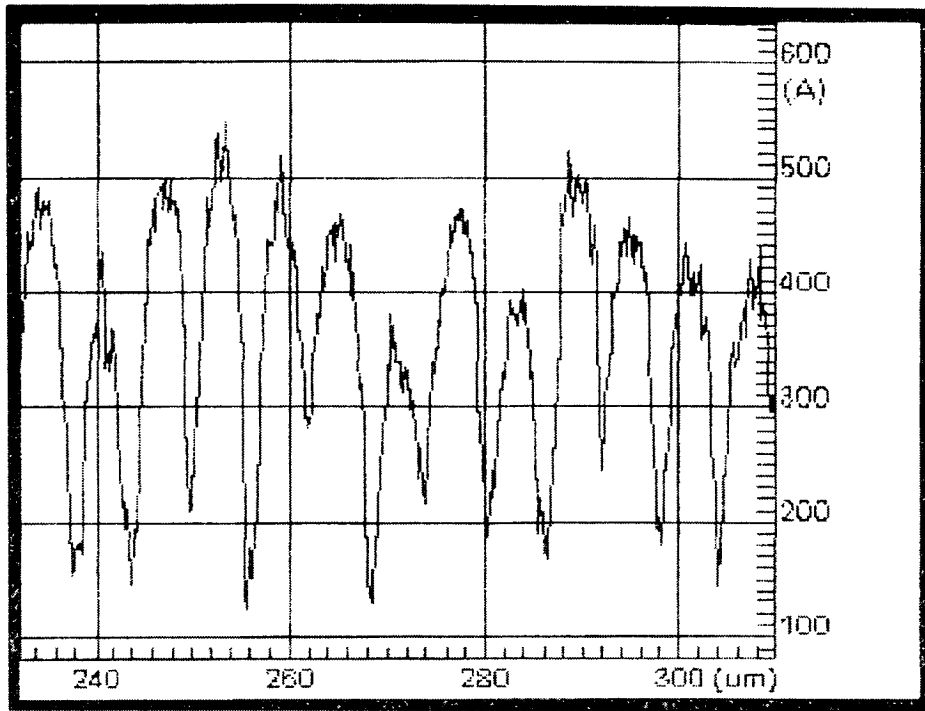
Figure 6.30: Dektak surface profile of slightly dished metal trenches.

6.7 Experimental Results

Using the oxide thickness contour maps produced prior to metal2 deposition, sites were chosen on wafers 1–3 where the oxide thickness variation across a die was acceptable. No such sites were available on wafer 4, since every die had an oxide thickness variation of at least 5%. The oxide thickness variation across the damascene–processed wafer 5 was assumed to be minimal, an assumption justified by the reduced amount of ECR deposition and less vigorous CMP applied to the wafer compared with wafers 1–4.

Using an HP4061A test system, the capacitance between the two layers of metal was measured for each set of test structures, and the relationship between offset and capacitance between combs plotted. To ease the comparison of the measured and simulated results, the point was determined about which each graph produced using experimental data was symmetrical, and the mean of the results to either side of this midpoint plotted. These results are shown in figures 6.31 to 6.34 with the corresponding wafer cross-sections shown in figures 6.35 to 6.38.

151

Inspection of the SEM cross-sections indicates that the 56° slope is a reasonable approximation to the fabricated structures, so the set of curves produced from simulations for this situation will be compared to the graphs obtained experimentally. Figure 6.31, obtained using measurements from wafer 1, shows a curve which indicates that the planarity is around 0%. Figures 6.32 and 6.33, obtained using measurements from wafers 2 and 3, appear similar to one another and an initial inspection indicates that they lie in the 30% to 50% planarity range. However, the graph shown in figure 6.32 maintains a shallow gradient over a larger number of offsets than that in figure 6.33, which when compared with simulated results indicates that the planarity of wafer 2 is less that wafer 3. Comparisons with the simulations suggest that the planarity of wafer 2 is around 30%, while that of wafer 3 is around 50%. The SEM cross-sections of wafers 1, 2 and 3 show a correlation between these results and the observed planarity. The value of capacitance at zero offset confirms that the longer the wafer is polished the more oxide is removed, since this value increases from wafer 1 to wafer 3.

Figure 6.34 shows the capacitance vs offset for the damascene–processed wafer 5, and has a negative slope as expected for a 100% planar inter-layer dielectric. The curve differs from the simulated results since the final thicknesses of the metal and the ILD do not correspond to those assumed in the simulations. The gradient is steeper than that for the simulation results, which is likely to be due to the fact that the first layer of aluminium was only $0.5\mu m$ thick, compared to the $1\mu m$ simulated. This would reduce the capacitance between the sides of the lower teeth and the base of the upper teeth, leading to a lower capacitance at larger offsets. Erosion of the patterned area will simply increase this effect, and dishing of the metal is not expected to significantly affect the results since the ILD will still have a constant thickness. In any case, the degree of dishing and erosion on the measured die was found to be slight. The actual values of capacitance are significantly higher than those on wafers 1–3, due to the thinner ILD on wafer 5.

It should be realised that the simulated structures are an approximation to the fabricated ones. The simulations assume $3\mu m$ wide teeth on a $6\mu m$ pitch with a
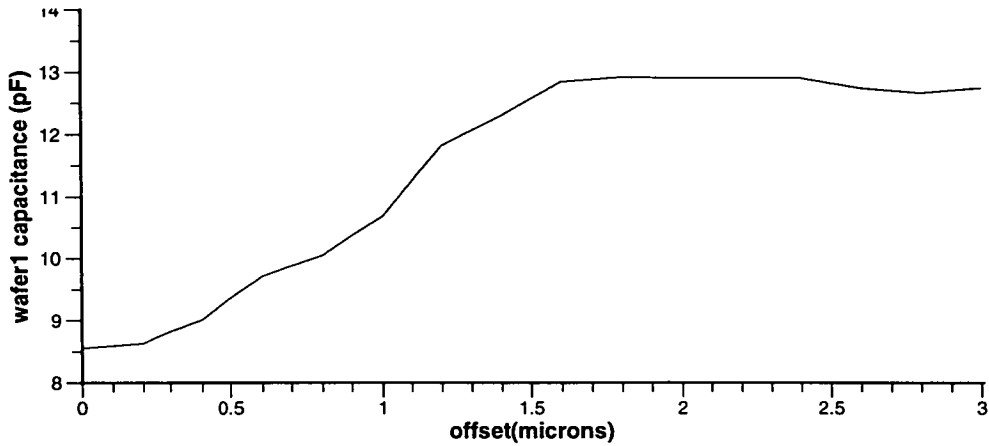
Figure 6.31: Measured capacitance vs offset between combs for structure on wafer 1.
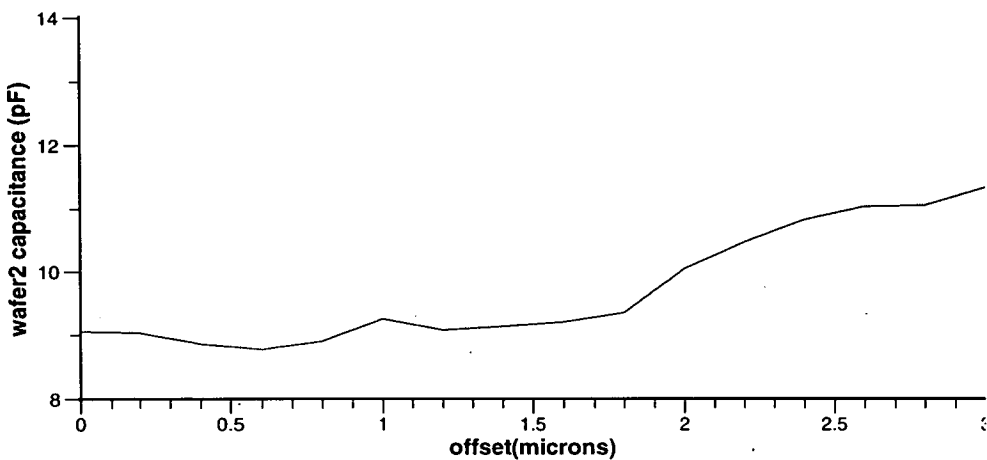
Figure 6.32: Measured capacitance vs offset between combs for structure on wafer 2.

dielectric slope of 56°. The shape of the slope is a fairly crude approximation to that on the fabricated structures, and the metal2 teeth are only 2.4μm wide on wafers 1–3 due to necessary over–exposure to clear the trenches of photoresist. Since on wafers 1–3, two layers of ECR oxide were deposited using different processes, the dielectric constant of the layers will be different. In fact the two layers can be identified in the cross-sections of figures 6.35, 6.36 and 6.37. As a consequence of this, the effective dielectric constant will change depending on the amount of polishing a wafer has received.

153
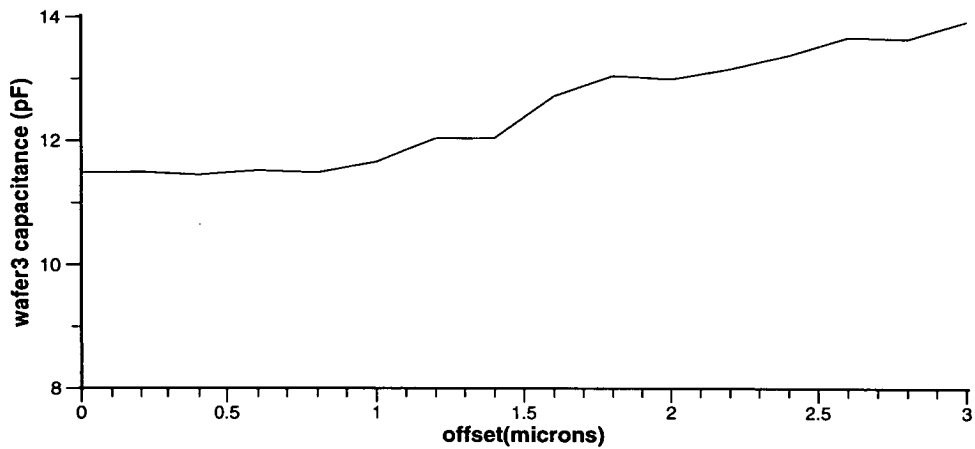
Figure 6.33: Measured capacitance vs offset between combs for structure on wafer 3.
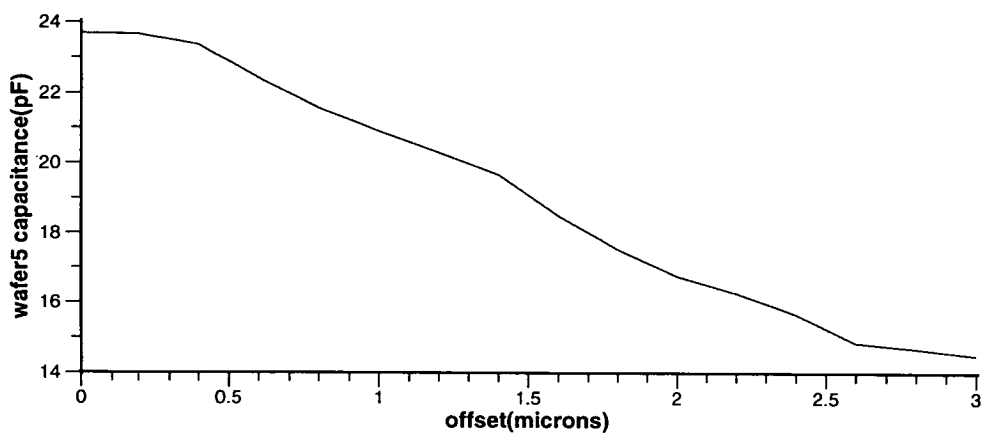
Figure 6.34: Measured capacitance vs offset between combs for structure on wafer 5.
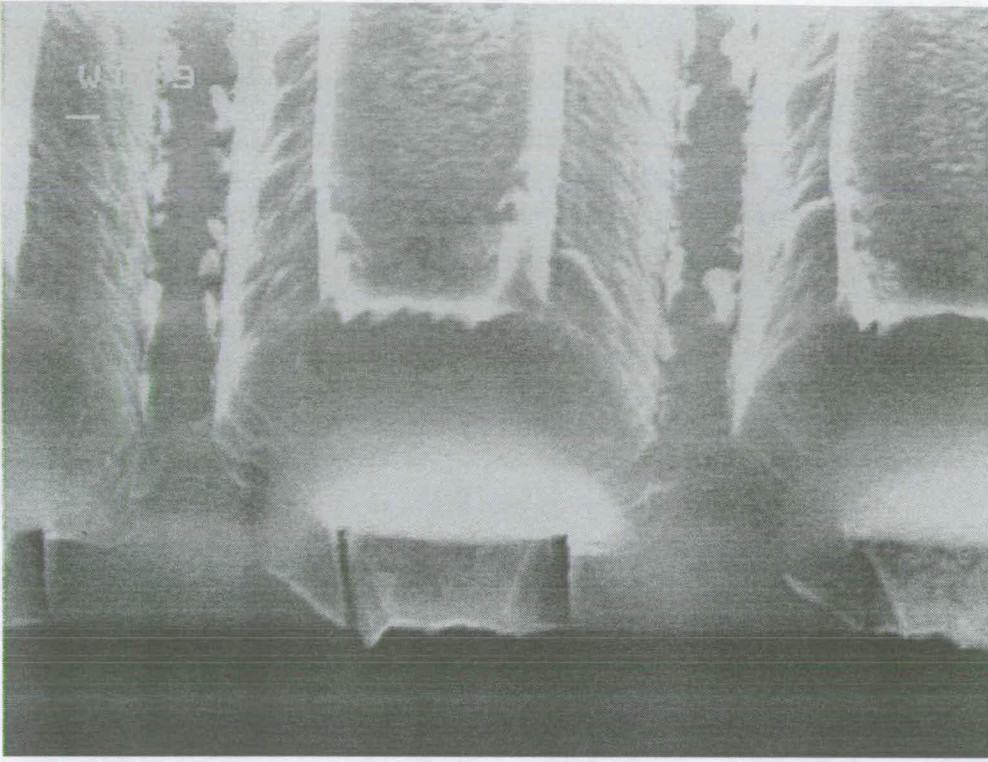
Figure 6.35: Cross–section of structure on wafer 1.
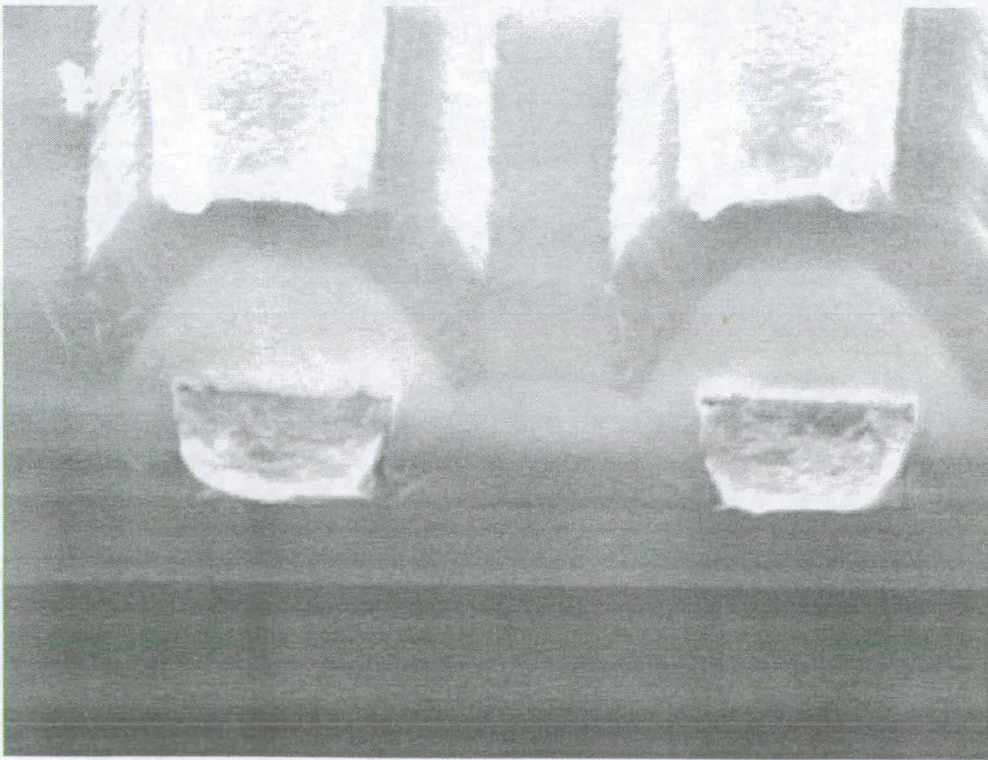
Figure 6.36: Cross–section of structure on wafer 2.

155
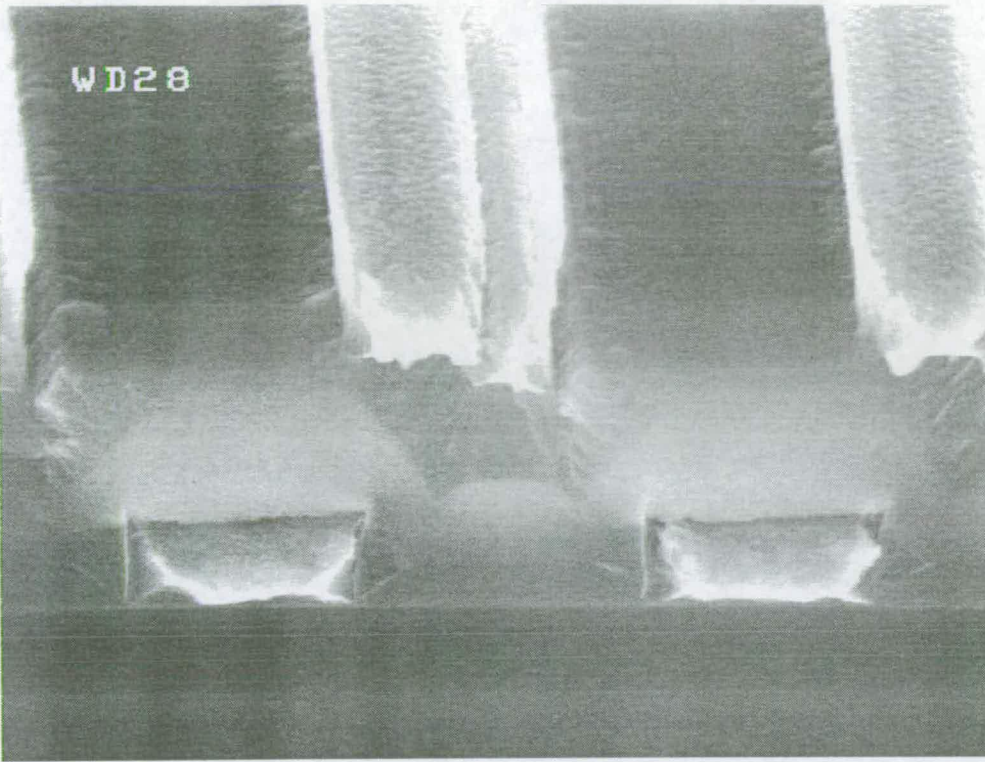
Figure 6.37: Cross–section of structure on wafer 3.
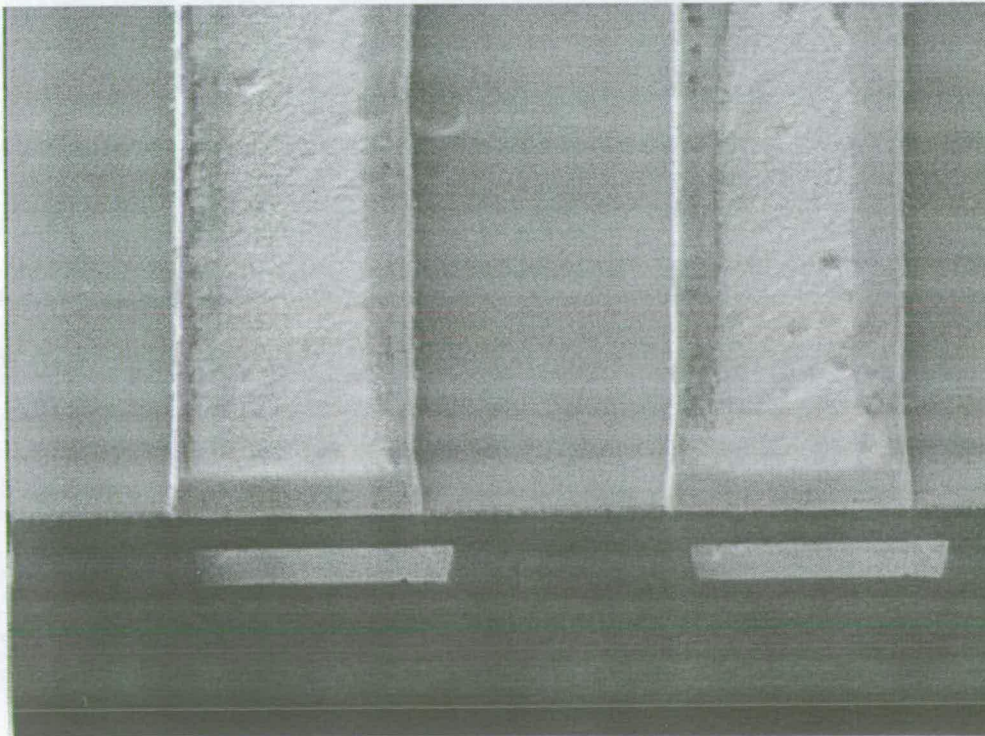
Figure 6.38: Cross–section of structure on wafer 5.

6.8 Discussion and Conclusions

The test structure presented here provides a means of electrically determining the degree of planarisation of an ILD. It depends on the fact that the capacitance between two metal combs will vary as the horizontal offset between them changes, and that this variation will depend on the topography of the oxide separating them. The gradient of a graph of capacitance between the combs as a function of offset can be used to estimate the degree of planarisation of the ILD, with negative gradients indicating planarisation greater than 70% (see figures 6.7, 6.8 and 6.9).

Simulations indicate that the structure is robust to likely oxide thickness variations. The experimental results bear this out, since although wafers 1–3 exhibit a degree of non–uniformity, the estimates of planarity obtained by comparing experimental results from these wafers with simulated results are confirmed by visual inspections of wafer cross–sections. The experimental results obtained for the damascene–processed wafer 5 broadly agree with the simulated results for the 100% planar situation, with any anomalies easily explained by the difference in fabricated and simulated layer thicknesses.

The structure described in this chapter has been designed to allow for a far higher misalignment between layers than would normally be experienced, and has a small incremental offset between the two layers. If space is at a premium it would be possible to reduce the number of individual structures by considering only offsets from $0.0\mu m$ to $3.0\mu m$, and one or two structures just outside this range to allow for some misalignment. The number of offsets considered within this range could also be reduced, further decreasing the number of structures required. The structure was designed such that the capacitance measured would be high in relation to noise introduced in the measurement system. If measurement equipment allows, the number of teeth per comb could be reduced, further decreasing space requirements. When characterising processes in which interconnect widths will be smaller than $3.0\mu m$, it is possible to scale the structure accordingly. Providing everything is scaled by the same amount in

157

both the horizontal and vertical directions, the shapes of the graphs of capacitance vs offset will be exactly the same as those for the structures presented here. The technique is applicable to situations where oxide and metal thicknesses scale differently to line widths, but in this case simulations should be rerun to determine the exact gradients expected for each degree of planarisation.

This test structure has applications in determining the severity of the topography of an ILD, information which is of direct relevance when considering the electrical characteristics of IC interconnect. It can also be used to characterise and monitor CMP, a planarisation process which is becoming increasingly widely used in the semiconductor industry.

Chapter 7

Review, Discussion and Future Work

The work described in this thesis is diverse, encompassing development of algorithms which represent the topgraphy of ICs in three dimensions, studies of the effects of topography on the electrical properties of interconnect, and experimental work to investigate the degree of IC topography. The motivation for all this work has stemmed from one source – the increasing impact that interconnect has on IC performance and manufacturing.

In this chapter, a review of the work presented in this thesis is given. Its significance is discussed, and some suggestions are made as to what further work could build on that which has been presented here.

7.1 Review

The operation of ICs is often thought of as being determined solely by the active devices from which the circuit is formed. However, with decreasing feature sizes and increasingly complex IC topography, the electrical effects of interconnect become ever more significant, and must be considered. The major trend in the IC industry, illustrated by the startling developments in both microprocessors and IC memory, and formalised by Moore's Law, is to increase the functionality obtainable on a single IC. This can be

achieved in two ways: by increasing the size of the IC, and by increasing the density of devices on the IC. Both of these trends result in increasing demands on IC interconnect. As the size of the IC increases, the length of the global interconnects, whose function is to connect together sub–circuits on the IC, also increases. The RC delay of these lines must therefore increase, and can be a limiting factor on the operating speed of the IC. As packing density increases, horizontal feature sizes must reduce. The pitch and width of interconnect tracks scale at the same rate as the devices which they connect. Layer thicknesses, whilst decreasing, do not scale to the same degree as the interconnect width and pitch, leading to an increase in track and via aspect ratios. This impacts on the electrical characteristics of the interconnect, since it results in an increase in fringing capacitance between wires and an increase in resistivity as track cross–sections decrease. Furthermore, modelling of interconnect becomes more complex, as the problem must be dealt with in three dimensions. Failure to do so can result in gross errors in extracted values of interconnect capacitance.

Increasing packing density, and the need to ensure that ICs do not become interconnect limited, results in the use of ever more interconnect layers. The use of multiple layers of metal, referred to as multi–level metallisation (MLM), adds to the three dimensional nature of the IC. This provides further motivation to perform simulations of electrical characteristics of interconnect in three dimensions. Furthermore, as the number of metal layers used increases, the topography of the IC becomes increasingly complex. If 3D simulations are to be accurate, an accurate representation of the IC, including the complex three–dimensional topography, is required.

There are two distinct methods of producing a three–dimensional representation of an IC, process simulation and process emulation. Process simulation involves the use of complex numerical equations which describe the actual physical processes involved in each manufacturing step. Process simulators exist which deal with all aspects of IC manufacturing, encompassing diffusion, photolithography, deposition and etch steps. The majority of process simulators produce representations of a small section of an IC in one or two dimensions. A few three dimensional process simulators

exist, but their use is very resource–intensive due to the complexity of the algorithms they employ. Although process simulators can produce representations of sections of circuitry in three dimensions, their usefulness in producing suitable data for input to 3D interconnect simulators is limited due to the resources that would be required to produce a representation of even a small sub–circuit. In any case, the representation produced would be more accurate than required.

Process emulators produce representations of ICs based on observed or empirical data, and generally support only deposition and etch steps. Their algorithms are not as complex as those used by process simulators, and they are correspondingly less resource intensive. This leads to there being fewer barriers to developing process emulators which produce three dimensional IC representations, although the representations are not as accurate as those produced by process simulators. The reduced complexity of process emulators compared to process simulators leads to their ability to produce representations of larger areas of circuitry. They are ideally suited to producing 3D representations of IC interconnect for use with 3D interconnect simulators. In fact, some process emulators are directly linked to particular interconnect simulators.

The requirement to accurately represent IC interconnect in three dimensions, and the limitations of existing process emulators, provided the motivation for the development of the software tool 3DTOP. Unlike many existing process emulators, 3DTOP is not linked to a particular 3D interconnect simulator. In fact, it can interface directly with two widely used interconnect simulators, Raphael and FastCap. 3DTOP can automatically produce three different types of 3D representation – planar, semi–conformal and conformal, which allows for accurate representations of ICs manufactured using a variety of processes. Data which interfaces with the ray tracing software POV-Ray can also be created by 3DTOP, which allows visualisation of the IC layout in three dimensions, providing valuable insight into the IC's structure. In order to use 3DTOP, in–depth knowledge of the process is not necessary, a feature common to most process emulators. 3DTOP simply requires a set of parameters related to the thickness and step–coverage of the layers to be created. Since this is such a limited set of data, the

effect of changes in the process can easily be investigated by altering a few parameters and re–running the software.

The importance of choosing an appropriate representation of an IC has been demonstrated using a set of very simple IC layouts. Planar, semi–conformal and conformal representations of each layout have been produced, and used as input to a 3D capacitance simulator, FastCap. The inter–node capacitances extracted for the three different representations, when compared, were found to differ significantly, in fact by up to 100% in some cases. The difference between the extracted capacitance values using the planar and conformal representations was found to be much greater than that between the extracted values found using semi–conformal and conformal representations. Furthermore, the difference between values of capacitance extracted using different 3D representations was found to become more significant as the width and pitch of the interconnect decreased.

The reason for accurately determining electrical parasitics due to IC interconnect is so that their effect can be accounted for during circuit design. It is especially important to find accurate values of capacitance due to interconnect when the circuit is expected to be particularly sensitive to parasitic capacitances. This has been demonstrated with reference to a circuit in which the storage of a logic value depends on capacitance on an electrical node. The behaviour of the circuit, a ferro–electric liquid crystal over silicon SLM, was first simulated without the inclusion of any parasitic capacitances. Parasitic capacitances between electrical nodes in the circuit were found using two methods: conventional techniques using Cadence extraction software and a proprietary technology file, and 3D extraction using 3DTOP and Raphael. Of these two methods, the latter was expected to yield the most accurate results, since it incorporates fewer approximations than the conventional technique. The capacitances extracted using conventional and 3D techniques were compared, and found to differ by up to 32%. The circuit was simulated with both sets of parasitic capacitances included. The results of these simulations were found to differ slightly from each other, whilst differing significantly from the results of the simulation in which no parasitic capacitances were

included. Due to an incomplete Cadence technology file for the manufacturing process, some of the conventional capacitance extraction was of necessity performed by hand. The simple input parameters required by 3DTOP ensured that no such problem was encountered in the 3D extraction.

Much research is currently focussed on microelectromechanical systems (MEMS). If their operation is to be adequately simulated, MEMS must be represented in three dimensions. Where standard IC processing is used to manufacture MEMS, 3DTOP can be used to create appropriate three dimensional data representations. This has been demonstrated with the creation of a 3D conformal representation of a simple x–y translator.

The topography of an IC has an effect on both the electrical properties of interconnect and on the success with which layers can be deposited and patterned. It is therefore important to be able to determine the degree of topography exhibited by particular layers forming the IC. This can be achieved by using a surface profiler at an appropriate point in the processing cycle, or by taking a cross–section. The former method has limited accuracy depending on the size of the stylus used, and can only provide information relating to the IC surface. The latter method is non–trivial and destroys the sample. The drawbacks of these techniques provided the motivation for the development of an electrical test structure for use in determining the severity of topography of an inter-layer dielectric (ILD). The test structure consists of a set of structures comprising two combs on consecutive conducting layers separated by the ILD whose topography is to be investigated. In each set of structures, the combs are progressively offset from each other, so that the whole range of offsets, from no offset to complete offset, is encompassed. The capacitance between each pair of combs can be measured and plotted against the offset between the combs. The shape and gradient of the resulting graph is determined by the planarity of the ILD. Experimental results were carried out and found to confirm the results obtained by simulation.

7.2 Discussion and Suggestions for Future Work

3DTOP has an important contribution to make in the context of Technology CAD (TCAD). It exhibits flexibility in both the type of 3D representation it can be used to produce and in the three dimensional simulation and visualisation tools with which it can interface. Since it is a process emulator rather than a process simulator, the representation it produces is an approximation to the actual topography of a manufactured IC. However, the benefit of producing a highly accurate representation of IC interconnect for use with 3D simulators is questionable. Interconnect simulation is likely to be required at sub–circuit level, and to produce a highly accurate 3D representation of the area occupied by even a small sub–circuit would be extremely resource intensive. Furthermore, the amount of data produced would result in the 3D simulator used for the interconnect analysis requiring increased computing resource, once the issue of interfacing a complex three dimensional description with the simulator had been addressed.

In any case, increasingly detailed 3D representations lead to diminishing returns in terms of the accuracy of the value of capacitance extracted. Increasing refinement of the 3D representation to include rounded corners for example would doubtless lead to more accurate capacitance extraction, but the gains in accuracy of extracted capacitance values would be small, whereas the increase in computing resources required would be significant. For this reason, further work on refining the representations produced by 3DTOP is not a priority. However, increasing flexibility in the allowable combinations of the three types of 3D representation would be advantageous, and would be a productive direction for further work. The ability to mix freely the three types of representation within the emulation of one process flow would enable the results of a wider range of manufacturing processes to be successfully represented. Currently, 3DTOP treats all layers in one process flow as either planar, semi–conformal or conformal, although variation of the step coverage of semi–conformal layers within one process flow is supported.

3DTOP, when used in conjunction with POV–Ray, has been shown to have applications in visualisation of ICs in three dimensions. The success of this has been demonstrated with reference to a 3DTOP and POV–Ray image of an array of spatial light modulators, which was compared to a scanning electron micrograph of the array in chapter 5, section 5.5. The visualisation opportunities created by 3DTOP have been recognised by the CAD company Mentor Graphics, who currently display a representation of a CMOS inverter created using 3DTOP and POV-Ray on their web site [93].

3DTOP has applications in the field of MEMS. This potential was noticed by the creators of the MEMS simulation package Solidis [72], which led to a successful undergraduate project investigating the creation of an interface between 3DTOP and Solidis [80]. However, in order that 3DTOP fulfill this potential, it must be able to accept 2D polygons which contain lines which are neither Manhatten nor $45°$, so that any MEMS, such as those containing cogs and gears, may be successfully represented. This would also remove the restriction on the semi–conformal data representation, which can currently only accept Manhatten layout if robustness is to be guaranteed (see section 4.5.1).

The wide ranging applications of 3DTOP have been described in this thesis. In order for it to fully achieve its potential, 3DTOP should be straightforward to use and should be seamlessly integrated into an IC designer's routine. As far as producing data for use with FastCap, Raphael and POV–Ray is concerned, 3DTOP fulfills this requirement, in that data files are created which can be used directly as input to these software packages. The production of data to form input to 3DTOP from 2D layout is not quite as simple, in that the 2D information must be streamed out from the layout into a GDSII text file before being converted using a simple software routine into *box* format for input to 3DTOP. Further work would include interfacing 3DTOP directly with the Cadence layout tool, such that the area of interest could be selected on screen, and a 3DTOP–compatible box description created automatically. As is the case for any software package, a manual detailing how to use 3DTOP should also be produced.

The electrical test structure presented in this thesis provides a means of determining the degree of planarity of an IC. Planarisation of some form is becoming increasingly widely used in semiconductor manufacturing. As its prevalence increases, the need to produce conformal representations of ICs, such as those created by 3DTOP, will reduce. However, complete planarisation of all layers in a process is common only in leading edge processes – many processes are still in use which do not planarise all layers. Even when planarisation does exist, the resulting topography is not always 100% planar. In future, 3DTOP could be modified to allow for the inclusion of a parameter which would define the *degree* of topography of the data created, in addition to its current ability to create data representing topography of a particular *type*. The test structure presented here could be used to determine this parameter for a particular process, so that interconnect capacitance could be accurately determined.

Chemical mechanical polishing is an important new processing technique and the mechanisms it involves are not fully understood. Characterisation and monitoring of CMP are important issues to IC manufacturers, and the test structure presented here provides a useful tool in this area. Further work on this test structure could be to confirm that the technique is applicable at smaller geometries.

Appendix A

Pseudo Code

A.1   Pseudo Code Description of 3D Block Algorithm

CREATE SUBSTRATE LAYER AND INSERT INTO *topsurface*

/* *topsurface* IS A LIST OF BLOCKS DESCRIBING THE UPPER SURFACE OF THE CIRCUIT. */

/* THE CONTENTS OF THE LIST ARE ORDERED BY INCREASING HEIGHT. */

FOR EACH LAYER TO BE CREATED {

    /* LISTS OF BLOCKS *planelist* AND *steplist* TOGETHER DESCRIBE 3D LAYER */

    FOR   EACH BLOCK IN *topsurface* {

        IF   (*currentlayer* AND *topsurface* BLOCK) IS TRUE

            INSERT RESULTING BLOCK INTO *planelist*

    }

    FOR EACH BLOCK IN *planelist* {

        BLOATEDBLOCK = CURRENT BLOCK BLOATED BY GIVEN STEPSIZE

        /* AND WITH STEPS ALREADY CREATED */ .

        FOR EACH BLOCK IN *steplist* {

            IF (BLOATEDBLOCK AND CURRENTSTEP) IS TRUE

                INSERT RESULTING BLOCK INTO *steplist*

        }

        /* AND WITH BLOCKS ALREADY CREATED */ .

```
        FOR EACH BLOCK IN LIST OF BLOCKS, storedlist {

            IF (BLOATEDBLOCK AND STOREDBLOCK) IS TRUE

                INSERT RESULTING BLOCK IN steplist

        }

        INSERT CURRENT planelist BLOCK INTO storedlist

    }

    */ UPDATE topsurface /*

    RENAME topsurface AS OLDTOPSURFACE

    FOR EACH OLD TOP BLOCK IN OLDTOPSURFACE {

        IF (OLD TOP BLOCK AND currentlayer) IS FALSE

            /* SURFACE IS UNAFFECTED BY NEW LAYER */

            INSERT OLD TOP BLOCK IN topsurface

    }

    IF steplist IS EMPTY

        INSERT ALL CONTENTS OF planelist INTO topsurface

    ELSE {

        FOR EACH BLOCK IN planelist {

            FOR EACH BLOCK IN steplist {

                IF UPPER LEVEL OF STEP BLOCK = UPPER LEVEL OF PLANE BLOCK

                    INSERT BLOCK IN sametoplist

                ELSE IF UPPER LEVEL OF STEP BLOCK > UPPER LEVEL OF PLANE BLOCK

                    INSERT BLOCK IN greatertoplist

            }

            NEWTOPBLOCK = sametoplist ANDNOT greatertoplist

            INSERT NEWTOPBLOCK INTO topsurface

        }

    }

}
```

A.2 Pseudo Code Description of Conformal Boundary Algorithm

CREATE LIST OF PLANES DESCRIBING GRID FOR USE IN FASTCAP DISCRETISATION

/* *topsurface* IS A LIST OF PLANES DESCRIBING THE UPPER SURFACE OF THE CIRCUIT. */

/* THE CONTENTS OF THE LIST ARE ORDERED BY DECREASING HEIGHT. */

createlist = LIST OF LAYERS TO BE CREATED

FOR EACH LAYER IN *createlist* {

    IF (*currentlayer* IS OF TYPE *conductor* OR *via*){

        /* WILL NEED TO SPECIFY ELECTRICAL NODES */

        SET PARAMETER *neednodes* = 1

        IF (*currentlayer* IS OF TYPE *conductor*)

            SET LAYER *latestconductor* = *currentlayer*

        IF (*currentlayer* IS OF TYPE *via*)

            SET LAYER *latestvia* = *currentlayer*

    }

    /* CREATE *lowerbound*, LIST OF PLANES DESCRIBING LOWER BOUNDARY OF *currentlayer* */

    FOR EACH PLANE IN *topsurface*{

        IF(*currentlayer* AND TOPPLANE) IS TRUE{

            INSERT RESULT IN *lowerbound*

        /* CREATE PLANES DESCRIBING UPPER BOUNDARY OF *currentlayer, upperbound* */

            IF (*currentlayer* IS OF TYPE *conductor*{

                BLOAT CURRENT LOWER BOUNDARY BY GIVEN STEPSIZE

                AND RESULT WITH *currentlayer*

                ANDNOT RESULT WITH PLANES ALREADY IN *upperbound*

                SET HEIGHT OF PLANE TO TOPPLANEHEIGHT + *currentlayer* THICKNESS

                INSERT IN *upperbound*

            }

            ELSE IF(*currentlayer* IS OF TYPE *via*{

                RAISE HEIGHT OF CURRENT LOWER BOUNDARY BY *currentlayer* THICKNESS

```
                INSERT IN upperbound

        }

    }

}
IF(currentlayer IS OF TYPE conductor {

        /* MODIFY LOWER BOUNDARIES TO ACCOUNT FOR VIAS BELOW */

        IF(latestvia STORED){

            IF(latestvia AND currentlayer) IS TRUE

                ANDNOT EACH LOWER BOUNDARY PLANE WITH latestvia

        }

        /* UPDATE topsurface */

        FOR EACH PLANE IN topsurface{

            ANDNOT CURRENT TOP PLANE WITH currentlayer

            INSERT ALL PLANES IN upperbound INTO topsurface

        }

        /* FIND FOLLOWING VIA AND DIELECTRIC CONSTANT */

        ITERATE THROUGH createlist

        ONCE currentlayer IS FOUND{

            LAYER nextvia = NEXT VIA LAYER IN createlist

            PARAMETER nextdielconstant = DIELECTRIC CONSTANT OF

            NEXT DIELECTRIC LAYER IN createlist

        MODIFY UPPER BOUNDARIES TO ACCOUNT FOR VIAS ABOVE */

        IF(nextvia SET){

            IF(nextvia AND currentlayer) IS TRUE

                ANDNOT EACH UPPER BOUNDARY PLANE WITH nextvia

        {

        /* AMEND EACH PLANE IN LOWER AND UPPER BOUNDARIES TO ACCOUNT FOR GRID */

        /* CREATE SIDE BOUNDARIES BETWEEN UPPER AND LOWER BOUNDARIES */

        AND LOWER AND UPPER BOUNDARIES WITH POLYGONS DESCRIBING GRID

        CREATE LIST OF PLANES CONTAINING ALL LOWER AND UPPER BOUNDARY PLANES

        PASS EACH LIST TO SIDE BOUNDARY CREATION ALGORITHM
```

170

WRITE RESULTS INTO UPPERBOUNDARY OUTPUT FILE

/* WRITE UPPER AND LOWER BOUNDARIES TO FILE */

FOR *lowerbound* AND *upperbound*{

    WRITE PLANES TO APPROPRIATE OUTPUT FILE

    PASS LIST OF PLANES TO SIDE BOUNDARY CREATION ALGORITHM

    WRITE SIDE BOUNDARIES TO APPROPRIATE OUTPUT FILE

}

INSERT OUTPUT FILES IN FASTCAP LIST FILE WITH APPROPRIATE DIELECTRIC PARAMETERS

}

IF(*currentlayer* IS OF TYPE *via*)

    AS FOR CONDUCTOR BUT CREATE ONLY EDGES BETWEEN UPPER AND LOWER BOUNDARIES

}

ELSE IF(*currentlayer* IS OF TYPE *dielectric*{

    /* DO NOT NEED TO SPECIFY ELECTRICAL NODES */

    SET PARAMETER *neednodes* = 0

    /* UPDATE *topsurface* */

    FOR EACH PLANE IN *topsurface*{

        BLOAT BY *currentlayer*'S STEPSIZE PARAMETER

        AND WITH *currentlayer*

        ANDNOT WITH PREVIOUSLY CREATED PLANES

        SET HEIGHT TO CURRENT HEIGHT + *currentlayer* THICKNESS

        INSERT IN NEW *topsurface*

    }

    /* FIND FOLLOWING CONDUCTOR */

    ITERATE THROUGH *createlist*

    ONCE *currentlayer* IS FOUND

        FIND NEXT CONDUCTOR AND SET *nextconductor*

    /* CREATE DIELECTRIC BOUNDARY PLANES */

    /* MODIFY *topsurface* TO ACCOUNT FOR FOLLOWING CONDUCTOR */

    IF(*nextconductor* STORED)

        ANDNOT EACH *topsurface* PLANE WITH *nextconductor*

```
        /* WRITE DIELECTRIC BOUNDARIES TO FILE */

        AND PLANES DESCRIBING DIELECTRIC WITH POLYGONS DESCRIBING GRID

        WRITE PLANES TO DIELECTRIC OUTPUT FILE

        PASS LIST OF PLANES TO SIDE BOUNDARY CREATION ALGORITHM

        WRITE SIDE BOUNDARIES TO DIELECTRIC OUTPUT FILE
    }

    INSERT OUTPUT FILES IN FASTCAP LIST FILE WITH APPROPRIATE DIELECTRIC PARAMETERS

}
```

A.3 Pseudo Code Description of Semi–Conformal Boundary Algorithm

CREATE LIST OF POLYGONS DESCRIBING GRID FOR USE IN FASTCAP DISCRETISATION

/* *topsurface* IS A LIST OF 3D POLYGONS DESCRIBING THE UPPER SURFACE

OF THE REPRESENTATION AT ANY PARTICULAR TIME */

createlist = LIST OF LAYERS TO BE CREATED

FOR EACH LAYER IN *createlist* {

    IF (*currentlayer* IS OF TYPE *conductor* OR *via*){

        /* WILL NEED TO SPECIFY ELECTRICAL NODES */

        SET PARAMETER *neednodes* = 1

        IF (*currentlayer* IS OF TYPE *conductor*)

            SET LAYER *latestconductor* = *currentlayer*

        IF (*currentlayer* IS OF TYPE *via*)

            SET LAYER *latestvia* = *currentlayer*

        /* CREATE *lowerbound*, A LIST OF 3D POLYGONS */

        /* DESCRIBING LOWER BOUNDARY OF *currentlayer* */

        FOR EACH 3D POLYGON IN *topsurface*{

            IF(*currentlayer* AND TOPPOLY3D) IS TRUE{

                TRANSFER 3D INFORMATION TO THE RESULTING POLYGON

                SET ELECTRICAL NODE INFORMATION

                INSERT RESULTING 3D POLYGONS IN *lowerbound*

            }

        }

        /* CREATE *upperbound*, A LIST OF 3D POLYGONS /*

        /* DESCRIBING UPPER BOUNDARY OF *currentlayer*/

        FOR EACH 3D POLYGON IN *lowerbound*{

            INCREASE ALL VERTEX Z–VALUES BY THE USER–DEFINED LAYER THICKNESS

            INSERT RESULT IN *upperbound*

        }

/* CREATE 3D POLYGONS FORMING SIDES */

/* BETWEEN UPPER AND LOWER SURFACES */

ITERATE THROUGH *lowerbound* AND *upperbound*

FOR EACH POLY3D{

    AND WITH GRID POLYGONS

    IF ONE OF THE RESULTANT POLYGON EDGES COINCIDES WITH A LAYER POLYGON EDGE

    INSERT EDGE IN EDGELIST *sideedges*

}   PASS *sideedges* TO SIDE BOUNDARY CREATION ALGORITHM

IF(*currentlayer* IS OF TYPE *via*){

    INSERT RESULTING 3D POLYGONS INTO *viabound*

    WRITE *viabound* 3D POLYGONS INTO VIA OUTPUT FILE

ELSE IF(*currentlayer* IS OF TYPE *conductor*){

    INSERT RESULTING 3D POLYGONS INTO *upperbound*

    /* CREATE SLOPES AROUND CONDUCTOR FOR

    USE IN CREATION OF FOLLOWING DIELECTRIC */

    /* FIND OVERLAPPING AREAS OF BLOATED POLYGONS

    WHERE SLOPES AROUND CONDUCTORS WOULD INTERSECT */

    BLOAT ALL POLYGONS BY USER–DEFINED *stepsize*

    AND ALL BLOATED POLYGONS

    INSERT RESULTS IN LIST OF POLYGONS, *overlappolys*

    /* CREATE LIST OF COLLARS AROUND POLYGONS */

    ITERATE THROUGH *lowerbound*

    FOR EACH 3D POLYGON{

        BLOAT 3D POLYGON BY *stepsize*

        ANDNOT RESULT WITH ORIGINAL POLYGON

        DIVIDE RESULTING *collar* INTO QUADRILATERALS, EACH WITH

        ONE SIDE DEFINED BY AN EDGE OF THE ORIGINAL POLYGON

        INSERT RESULT IN LIST OF POLYGONS, *collarpolys*

    }

    ITERATE THROUGH *collarpolys*

    FOR EACH POLYGON{

```
        /* CONVERT TO A 3D POLYGON */

        CALCULATE Z VALUE OF EACH VERTEX

        BASED ON DISTANCE FROM ORIGINAL POLYGON

    }

    ITERATE THROUGH overlappolys

    FOR EACH overlappoly{

        DETERMINE CORRECT Z VALUE OF EACH VERTEX

        BY COMPARISON WITH COLLAR POLYGONS

    }

    INSERT overlappolys INTO topsurface

    /*ENSURE NO POLYGONS OVERLAP IN X AND Y*/

    ANDNOT collarpolys WITH overlappolys

    INSERT RESULTING 3D POLYGONS INTO topsurface

    ANDNOT upperbound WITH collarpolys

    INSERT RESULTING 3D POLYGONS INTO topsurface

/* MODIFY LOWER BOUNDARIES TO ACCOUNT FOR VIAS BELOW */

IF(latestvia STORED){

    IF(latestvia AND currentlayer) IS TRUE{

        ANDNOT EACH LOWER BOUNDARY PLANE WITH latestvia

        AND RESULTING 3D POLYGONS WITH GRID POLYGONS

        WRITE RESULTS TO LOWER BOUNDARY OUTPUT FILE

    }

}

/* FIND FOLLOWING VIA AND DIELECTRIC CONSTANT */

ITERATE THROUGH LIST OF LAYERS TO BE CREATED

ONCE currentlayer IS FOUND{

    LAYER nextvia = NEXT VIA LAYER IN createlist

    PARAMETER nextdielconstant = DIELECTRIC CONSTANT OF

    NEXT DIELECTRIC LAYER IN createlist

}

MODIFY UPPER BOUNDARIES TO ACCOUNT FOR VIAS ABOVE */
```

```
IF(nextvia SET){

      IF(nextvia AND currentlayer) IS TRUE

            ANDNOT EACH UPPER BOUNDARY PLANE WITH nextvia

            AND RESULTING 3D POLYGONS WITH GRID POLYGONS

            WRITE RESULTS TO UPPER BOUNDARY OUTPUT FILE

      }

}

ELSE IF(currentlayer IS OF TYPE dielectric{

      /* DO NOT NEED TO SPECIFY ELECTRICAL NODES */

      SET PARAMETER neednodes = 0

      /* UPDATE topsurface */

      FOR EACH 3D POLYGON IN topsurface

            INCREASE ALL VERTEX Z VALUES BY LAYER THICKNESS

      /* FIND FOLLOWING CONDUCTOR */

      ITERATE THROUGH LIST OF LAYERS TO BE CREATED

      ONCE currentlayer IS FOUND

            FIND NEXT CONDUCTOR AND SET nextconductor

      ANDNOT topsurface WITH nextconductor

      AND RESULTING 3D POLYGONS WITH GRID POLYGONS

      WRITE 3D POLYGONS TO DIELECTRIC OUTPUT FILE

INSERT OUTPUT FILES IN FASTCAP LIST FILE WITH APPROPRIATE DIELECTRIC PARAMETERS

      }

}
```

Bibliography

[1] C. Dianne Martin. ENIAC: Press Conference that Shook the World. *IEEE Technology and Society Magazine*, 14(4), Winter 1995/1996.

[2] Junichi Nishizawa. The Transistor – a Look Back and a Look Ahead. *Solid State Technology*, pages 73–75, December 1987.

[3] Jack S. Kilby. The Invention of the Integrated Circuit. *IEEE Transactions on Electron Devices*, ED–23(7):648–654, July 1976.

[4] Ed Korczynski. Moore's Law Extended: The Return of Cleverness. *Solid State Technology*, pages 359–364, July 1997.

[5] S. M. Sze. *VLSI Technology*. McGraw-Hill, 1983.

[6] Syd R Wilson, Clarence J Tracey, and John L Freeman. *Handbook of Multilevel Metallization for Integrated Circuits*. Noyes Publications, 1993.

[7] Y. Taur, Y. J. Mii, D. J. Frank, H. S. Wong, D. A. Buchanan, S. J. Wind, S. A. Rishton, G. A. Sai-Halasz, and E. J. Nowak. CMOS Scaling into the 21st Century: $0.1\,\mu$m and Beyond. *IBM Journal of Research and Development*, 39(1/2):245–259, January/March 1995.

[8] Mark T. Bohr. Interconnect Scaling – the Real Limiter to High Performance ULSI. *Solid State Technology*, pages 105–111, September 1996.

[9] Soo-Young Oh and Keh-Jeng Chang. 2001 Needs for Multi–Level Interconnect Technology. *Circuits and Devices*, pages 16–21, January 1995.

[10] M. B. Small and D. J. Pearson. On–chip wiring for VLSI: Status and Directions. *IBM Journal of Research and Development*, 34(6):858–867, November 1990.

[11] Anthony J. Walton, Robert J. Holwill, and J. M. Robertson. Numerical Simulation of Resistive Interconnects for Integrated Circuits. *IEEE Journal of Solid–State Circuits*, 20(6):1252–1258, December 1985.

[12] N. P. van der Meijs. *Accurate and Efficient Layout Extraction*. PhD thesis, Delft University of Technology, 1992.

[13] Bruce Roberts, Alain Harrus, and Robert L. Jackson. Interconnect Metallization for Future Device Generations. *Solid State Technology*, pages 69–78, February 1995.

[14] J. R. Lloyd. Electromigration Failure in Thin Film Conductors. In *Proceedings of the 26th European Solid State Device Research Conference*, pages 839–846, September 1996.

[15] Robert H. Dennard, Fritz H. Gaensslen, Hwa-Nien Yu, V. Leo Rideout, Ernest Bassous, and Andre R. LeBlanc. Design of Ion–Implanted MOSFETs with Very Small Physical Dimensions. *IEEE Journal of Solid–State Circuits*, SC–9(5):256–267, October 1974.

[16] David Charles Thomas and S. Simon Wong. A Planar Interconnection Technology Utilizing the Selective Deposition of Tungsten – Multilevel Implemantation. *IEEE Transactions on Electron Devices*, 39(4):901–907, April 1992.

[17] J. G. Ryan, R. M. Geffken, N. R. Poulin, and J. R. Paraszczak. The Evolution of Interconnection Technology at IBM. *IBM Journal of Research and Development*, 39(4):371–381, July 1995.

[18] A. H. Zemanian, Reginald P. Tewarson, Chi Ping Ju, and Juif Frank Jen. Three–Dimensional Capacitance Computations for VLSI/ULSI Interconnections. *IEEE Transactions on Computer–Aided Design of Integrated Circuits and Systems*, 8(12):1319–1325, December 1989.

[19] Peter E. Cottrell and Edward M. Buturla. VLSI Wiring Capacitance. *IBM Journal of Research and Development*, 29(3):277–287, May 1985.

[20] Narain D. Arora, Kartik V. Raol, Reinhard Schumann, and Llanda M. Richardson. Modeling and Extraction of Interconnect Capacitances for Multilayer VLSI Circuits. *IEEE Transactions on Computer–Aided Design of Integrated Circuits and Systems*, 15(1):58–67, January 1996.

[21] Kimiko Aoyama, Kiyoshe Ise, Hisako Sato, Katsumi Tsuneno, and Hiroo Masuda. A New Characterisation of Sub-micron Parallel Multilevel Interconnects and its Experimental Verification. In *Proceedings of IEEE International Conference on Microelectronic Test Structures*, pages 63–66, March 1995.

[22] N. P. van der Meijs and J. T. Fokkema. VLSI Circuit Reconstruction from Mask Topology. *Integration–the VLSI journal*, 2(2):85–119, 1984.

[23] Neil Weste and Kamran Eshraghian. *Principles of CMOS VLSI Design*. Addison Wesley, 1985.

[24] D. C. Edelstein, G. A. Sai-Halasz, and Y. J. Mii. VLSI on–chip Interconnection Performance Simulations and Measurements. *IBM Journal of Research and Development*, 39(4):383–401, July 1995.

[25] Susumu Kurosawa. An Analytical Modeling of Three Primary Wiring Capacitance Components for Multi–Layer Interconnect Structure. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, E78–A(12):1793–1798, December 1995.

[26] T. Smedes, N.P. van der Meijs, and A. J. van Genderen. Boundary Element Methods for 3D Capacitance and Substrate Resistance Calculations in Inhomogeneous Media in a VLSI Layout Verification Package. *Advances in Engineering Software*, 20(1):19–27, 1994.

[27] T. Smedes, N. P. van der Meijs, A. J. van Genderen, P. J. H. Elias, and R. R. J. Vanoppen. Layout Extraction of 3D Models for Interconnect and Substrate Parasitics.

179

In *Proceedings of the 25th European Solid State Device Research Conference*, pages 397–400, September 1995.

[28] Umakanta Choudhury and Alberto Sangiovanni-Vincentelli. Automatic Generation of Analytical Models for Interconnect Capacitances. *IEEE Transactions on Computer–Aided Design of Integrated Circuits and Systems*, 14(4):470–480, April 1995.

[29] N. Delorme, M. Belleville, and J. Chilo. Inductance and Capacitance Analytic Formulas for VLSI Interconnects. *Electronics Letters*, 32(11):996–997, May 1996.

[30] Ganesh Shankar Samudra and Hsio Lin Lee. A Set of Analytic Formulas for Capacitance of VLSI Interconnects of Trapezium Shape. *IEEE Transactions on Electron Devices*, 41(8):1466–1467, August 1994.

[31] Cadence, San Jose River Oaks Campus, 555 River Oaks Parkway, San Jose, California, 95134, USA. *Cadence User's Manual*.

[32] Technology Modelling Associates, Inc., Third Floor, 300 Hamilton Avenue, Palo Alto, CA 94301, USA. *Raphael User's Manual*.

[33] K Nabors, S Kim, J White, and S Senturia. *Fastcap User's Guide*. Research Laboratory of Electronics, Massachusetts Institute of Technology, Cambridge, MA 02139, USA, September 1992.

[34] Pete Singer. New Interconnect Materials: Chasing the Promise of Faster Chips. *Semiconductor International*, pages 52–56, November 1994.

[35] David Butler. Options for Multilevel Metallization. *Solid State Technology*, pages S7–S10, March 1996.

[36] Iqbal Ali, Sudipto R. Roy, and Greg Shinn. Chemical-mechanical Polishing of interlayer dielectric: A review. *Solid State Technology*, pages 63–70, October 1994.

[37] T. J. Licata, E. G. Colgan, J. M. E. Harper, and S. E. Luce. Interconnect Fabrication Processes and the Development of Low–Cost Wiring for CMOS Products. *IBM Journal of Research and Development*, 39(4):419–435, July 1995.

[38] Robert W. Dutton and Ronald J. G. Goossens. Technology CAD at Stanford University: physics algorithms, software and applications. *Microelectronics Journal*, 26:99–111, 1995.

[39] Peter Lloyd, Colin C. McAndrew, Michael J. McLennan, Sani R. Nassif, Kishore Singhal, Kumud Singhal, Peter M. Zeitzoff, Mohammed N. Darwish, Ken Haruta, Janet L. Lentz, Hong-Ha Vuong, Mark R. Pinto, Conor S. Rafferty, and Isik C. Kizilyalli. Technology CAD at AT&T. *Microelectronics Journal*, 26:79–97, 1995.

[40] J. Ueda, S. Kuroda, K. Fukuda, K. Kai, and K. Nishi. Technology CAD at OKI. *Microelectronics Journal*, 26:159–175, 1995.

[41] Edward W. Scheckler, Alexander S. Wong, Robert H. Wang, Goodwin Chin, John R. Camagna, Andrew R. Neureuther, and Robert W. Dutton. A Utility–Based Integration System for Process Simulation. *IEEE Transactions on Computer–Aided Design*, 11(7):911–920, July 1992.

[42] Zakir H. Sahul, Kenneth C. Wang, Ze-Kai Hsisu, Eugene W. McKenna, and Robert W. Dutton. Heterogeneous Process Simulation Tool Integration. *IEEE Transactions on Semiconductor Manufacturing*, 9(1):35–47, February 1996.

[43] John D'Ignazio. TCAD Tools Leap Hurdles to Broader Use. *Semiconductor International*, pages 99–106, April 1996.

[44] Technology Modelling Associates, Inc., Third Floor, 300 Hamilton Avenue, Palo Alto, CA 94301, USA. *TSUPREM4 User's Manual*.

[45] Charles P. Ho, James D. Plummer, Stephen E. Hansen, and Robert W. Dutton. VLSI Process Modelling–SUPREM III. *IEEE Transactions on Electron Devices*, ED-30:1438–1453, November 1983.

[46] M. E. Law and R. W. Dutton. Verification of Analytic Point Defect Models using SUPREM–IV. *IEEE Transactions on Computer–Aided Design*, 2(2):181–190, February 1988.

[47] M. Karim Moallemi and Hui Zhang. A General Numerical Procedure for Multilayer Multistep IC Process Simulation. *IEEE Transactions on Computer–Aided Design of Integrated Circuits and Systems*, 13(11):1379–1390, November 1994.

[48] Ernst Strasser and Siegfried Selberherr. Three–Dimensional Simulation of Step Coverage for Contact Hole Metallization. In *Proceedings of the 24th European Solid State Device Research Conference*, pages 339–342, September 1994.

[49] E. Bar and J. Lorenz. 3–D Simulation of Low Pressure Chemical Vapour Deposition. In *Proceedings of the 24th European Solid State Device Research Conference*, pages 335–338, September 1994.

[50] Cameron Sorlie, Michael J. Brett, Steven K. Dew, and Tom Smy. Advanced Process Simulation of Metal Film Depostion. *Solid State Technology*, pages 101–107, June 1995.

[51] Eberhard Bar and Jurgen Lorenz. 3–D Simulation of LPCVD Using Segment–Based Topography Discretization. *IEEE Transactions on Semiconductor Manufacturing*, 9(1):67–73, February 1996.

[52] Kenny K. H. Toh, Andrew R. Neureuther, and Edward W. Scheckler. Algorithms for Simulation of Three–Dimensional Etching. *IEEE Transactions on Computer–Aided Design of Integrated Circuits and Systems*, 13(5):616–624, May 1994.

[53] Joachim Pelka, K. P. Muller, and Hermann Mader. Simulation of Dry Etch Processes by COMPOSITE. *IEEE Transactions on Computer–Aided Design*, 7(2):154–159, February 1988.

[54] Rudolf A. Buser and Nicholas F. de Rooij. ASEP*: a CAD Program for Silicon Anisotropic Etching. *Sensors and Actuators A*, 28:71–78, 1991.

[55] Technology Modelling Associates, Inc., Third Floor, 300 Hamilton Avenue, Palo Alto, CA 94301, USA. *DEPICT User's Manual.*

[56] Silvaco International, Inc., 4701, Patrick Henry Drive, Santa Clara, CA 95054, USA. *Optolith User's Manual.*

[57] Edward W. Scheckler and Andrew R. Neureuther. Models and Algorithms for Three–Dimensional Topography Simulation with Sample–3D. *IEEE Transactions on Computer–Aided Design of Integrated Circuits and Systems*, 13(2):219–230, February 1994.

[58] William G. Oldham, Andrew R. Neureuther, Chiakang Sung, John L. Reynolds, and Sharad Narayan Nandgaonkar. A General Simulator for VLSI Lithography and Etching Processes: Part II - Application to Deposition and Etching. *IEEE Transactions Electron Devices*, ED-27:1455–1459, August 1980.

[59] Keunmyung Lee and Andrew R. Neureuther. SIMPL–2:(SIMulated Profiles from the Layout – Version 2). *IEEE Transactions on Computer Aided Design*, 7(2):160–167, February 1988.

[60] John F. Sefler and Andrew R. Neureuther. Extracting Solid Conductors from a Single Triangulated Surface Representation for Interconnect Analysis. *IEEE Transactions on Semiconductor Manufacturing*, 9(1):82–86, February 1996.

[61] Technology Modelling Associates, Inc., Third Floor, 300 Hamilton Avenue, Palo Alto, CA 94301, USA. *TERRAIN User's Manual.*

[62] Silvaco International, Inc., 4701, Patrick Henry Drive, Santa Clara, CA 95054, USA. *Elite User's Manual.*

[63] H. Stippel, E. Leitner, Ch. Pichler, H. Puchner, E. Strasser, and S. Selberherr. Process Simulation for the 1990s. *Microelectronics Journal*, 26:203–215, 1995.

[64] Simulation Standard – Accurate Extraction of Interconnect Parasitics Based on 3D Back–End Process Simulation. Silvaco International Inc., 4701 Patrick Henry Drive, Santa Clara, CA 95054, USA, December 1996.

[65] George M. Koppelman and Michael A. Wesley. OYSTER: A Study of Integrated Circuits as Three–Dimensional Structures. *IBM Journal of Research and Development*, 27(2):149–163, March 1983.

[66] Reinhold H. Uebbing and Masao Fukuma. Process–Based Three–Dimensional Capacitance Simulation – TRICEPS. *IEEE Transactions on Computer–Aided Design*, CAD–5(1):215–220, January 1986.

[67] George M. Koppelman. OYSTER, a Three–Dimensional Structural Simulator for Microelectromechanical Design. *Sensors and Actuators*, 20:179–185, 1989.

[68] *Persistence of Vision Ray Tracer (POV-Ray) User's Documentation*, 1993.

[69] U. Lauther. An O(N log N) Algorithm for Boolean Mask Operations. In *Proceedings of 18th Design Automation Conference*, pages 555–560, 1981.

[70] G. A. Allan. *Yield Improvement of VLSI using Local Design Rules*. PhD thesis, University of Edinburgh, 1992.

[71] Gerard A. Allan and Anthony J. Walton. Efficient Critical Area Estimation for Arbitrary Defect Shapes. In *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, pages 20–28, October 1997.

[72] J. Funk, J. G. Korvink, G. Wachutka, and H. Baltes. Electro–Thermal–Mechanical Field Analysis using SESES. In *Proceedings of the 24th European Solid State Device Research Conference*, pages 347–350, September 1994. SESES later renamed SOLIDIS.

[73] W. Lee Smith, Kris Kruse, Karey Holland, and Randy Harwood. Film Thickness Measurements for Chemical Mechanical Planarization. *Solid State Technology*, pages 77–86, January 1996.

[74] Douglas J. McKnight. FLC/VLSI as a Smart Pixel Technology. In *Digest of the IEEE/LEOS 1996 Topical Meeting on Smart Pixels*, page 67, August 1996.

[75] M. W. G. Snook. personal communication, 1996.

[76] A. O'Hara, M. Begbie, I. D. Rankin, D. C. Burns, J. Gourlay, I. Underwood, and D. G. Vass. Protection of DRAM Spatial Light Modulators from Incident Light using a Multilevel Metallization Procedure. In *Proceedings of the 25th European Solid State Device Research Conference*, pages 277–280, September 1995.

[77] Janusz Bryzek, Kurt Petersen, and Wendell McCulley. Micromachines on the March. *IEEE Spectrum*, pages 20–31, May 1994.

[78] Danny Banks. Introduction to MicroEngineering. http://www.ee.surrey.ac.uk/Personal/D.Banks/umintro.html, 1994.

[79] Axel M. Stoffel. Micromachining and ASIC technology. *Microelectronics Journal*, pages 145–156, 1994.

[80] VincentNg. Project. Fourth year BEng project thesis, University of Edinburgh, 1996.

[81] J. R. Gilbert, P. M. Osterberg, R. M. Harris, D. O Ouma, X. Cai, A. Pfajfer, J. White, and S. D. Senturia. Implementation of a MEMCAD system for Electrostatic and Mechanical Analysis of Complex Structures from Mask Descriptions. In *Proceedings of the Sixth IEEE Workshop on Microelectromechanical Systems (MEMS)*, pages 207–212, February 1993.

[82] ISE Integrated Systems Engineering. 3D Solid Modeling and Process Emulation. Technical leaflet, 1995.

[83] J. Jason Yao, Susanne C. Arney, and Noel C. MacDonald. Fabrication of High Frequency Two–Dimensional Nanoactuators for Scanned Probe Devices. *Journal of Microelectromechanical Structures*, 1(1):14–22, March 1992.

[84] Jane P Elliott, Gerard A Allan, and Anthony J Walton. Automating the Calculation of 3D Interconnect Parasitics. In *Proceedings of IEE Colloquium on Advanced MOS and bi-polar Devices*, pages 15/1–15/2, February 1995.

[85] G J Gaston and I G Daniels. Efficient Extraction of Metal Parasitic Capacitances. In *Proceedings of IEEE International Conference on Microelectronic Test Structures*, pages 157–160, March 1995.

[86] Ruth DeJule. Advances in CMP. *Semiconductor International*, pages 88–96, November 1996.

[87] Michael A. Fury. Emerging Developments in CMP for Semiconductor Planarization. *Solid State Technology*, pages 47–54, April 1995.

[88] J. Paul Lesso. Endpoint Detection for Planarisation Process on Silicon Wafers. Fourth year BEng project thesis, University of Edinburgh, 1996.

[89] Stephen E. Lassig and James D. Tucker. Intermetal Dielectric Deposition by Electron Cyclotron Resonance Chemical Vapour Deposition (ECR CVD). *Microelectronics Journal*, 26(8):xi–xxiii, 1995.

[90] J. R. Hannah, R. J. Holwill, P. N. Kember, and R. Grimwood. Characterisation of a Production Single Step Planarisation Technique using ECR Deposition. In *Proceedings of Interconnection and Contact Metallization for ULSI Symposium*, October 1991.

[91] J. T. Pye, H.W.Fry, and W.J.Schaffer. High-density plasma CVD and CMP for 0.25-μm intermetal dielectric processing. *Solid State Technology*, pages 65–71, December 1995.

[92] BBN Software Products, 150 Cambridge Park Drive, Cambridge, MA 02140, USA. *BBN/Cornerstone User's Manual*.

[93] Mentor Graphics. http://www.mentor.com/xcalibre/datasheet.html.

[94] John. D. Kraus. *Electromagnetics*. McGraw-Hill, 1984.

Papers associated with this thesis

Jane P. Elliott, Martin Fallon, Anthony J. Walton, J. T. M. Stevenson, Anthony O'Hara and Alan M. Gundlach; 'An Electrical Test Structure for the Measurement of Planarization', IEEE Transactions on Semiconductor Manufacturing, Vol. 10, No. 2, pp242-249, May 1997.

J.P. Elliott, M. Fallon, A.J. Walton, J.T.M. Stevenson, A. O'Hara, C.M. Peyne, A. Shaffi, C.M. Reeves; 'Electrical Assessment of Planarisation for CMP and SOG Technologies', IEEE International Conference on Microelectronic Test Structures, pp85-90, March 1997.

J.P. Elliott, M. Fallon, A.J. Walton, J.T.M. Stevenson, A O'Hara; 'A Test Structure for the Measurement of Planarisation', IEEE International Conference on Microelectronic Test Structures, pp301-305, March 1996.

J.P. Elliott, M.W.G. Snook, I. Underwood, A.J. Walton, D.G. Vass; 'Visualisation, Extraction and simulation of Smart Pixel Circuits in Three Dimensions', IEEE/LEOS Smart Pixels, pp82-83, 7-9th August, 1996.

J.P. Elliott, G.A. Allan, A.J. Walton; 'The Automatic Generation of Conformal 3D Data for Simulation of IC Interconnect Parasitics and Representation of MEM Structures', ESSDERC, pp405-408, Sept 1995.

J.P. Elliott, G.A. Allan, A.J. Walton; 'The Automatic Generation of Conformal 3D Data for Interconnect Capacitance Simulation', VLSI Multi-Level Interconnect Conference, pp664-666, June 1995.

J.P. Elliott, G.A. Allan, A.J. Walton; 'Automating the calculation of 3D interconnect parasitics', IEE Colloquium on Advanced MOS and Bipolar Devices, No 1995/033, pp15/1-15/6, 14th Feb 1995.

An Electrical Test Structure for the Measurement of Planarization

Jane P. Elliott, *Member, IEEE*, Martin Fallon, Anthony J. Walton, *Member, IEEE*,
J. T. M. Stevenson, Anthony O'Hara, and Alan M. Gundlach

Abstract—This paper presents the simulation and experimental measurements of an electrical test structure that can be used to assess the degree of planarization of interlayer dielectrics. It consists of two sets of metal combs separated by a dielectric. For each structure the combs on the two layers overlap each other, with adjacent structures having the overlap in one direction progressionally offset by 0.2 μm. The capacitance of these structures is then measured, from which the degree of planarization can be assessed. This structure has potential applications for characterising chemical mechanical polishing (CMP) processes for multilevel very large scale integration (VLSI) applications.

I. INTRODUCTION

AS DEVICE dimensions have reduced, IC interconnect has become more dense requiring increased layers of metallization which, in turn, has made the planarization of interlevel dielectrics essential. Benefits of planarising dielectrics for multilevel metallization include improved step coverage, increased circuit reliability, and decreased interconnect resistance. Planarization also prevents the formation of abrupt resist thickness variations, leading to greater tolerance of the decreasing depth of focus in lithography exposure tools [1]. Parasitic interconnect capacitances can also be reduced by planarization [2], and this is of particular interest, since the effect of interconnect capacitance on circuit performance has become much more important [3]–[4] as device geometries have reduced.

This paper presents a test structure which can be used to help determine the degree of planarization using electrical measurements. This provides a means of electrically assessing planarization during the development of a process and for monitoring equipment performance once the process is in production.

II. PLANARIZATION

There are several methods of planarization. A widely used one is chemical mechanical polishing (CMP) [1], and the test structure described in this paper is ideally suited to evaluate this technology. CMP involves polishing away features on the surface of a wafer, using a mixture of mechanical abrasion and chemical reaction. In the ideal model, the raised features on the wafer surface will be progressively polished away, eventually resulting in a completely flat surface. This is illustrated in Fig. 1 where various degrees of planarization of an oxide
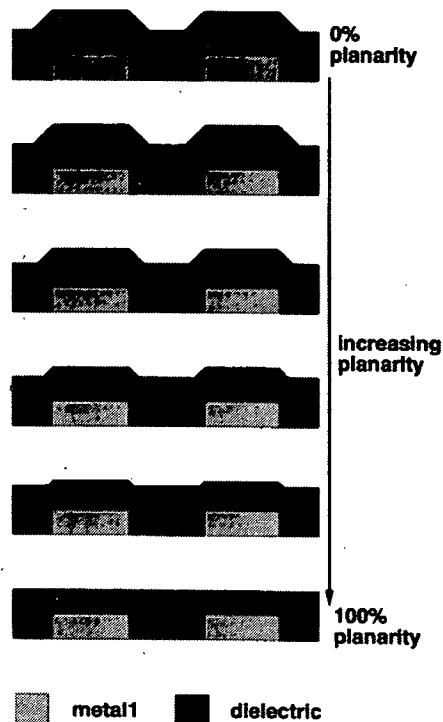

Fig. 1.   Increasing planarity of dielectric over metal using CMP.
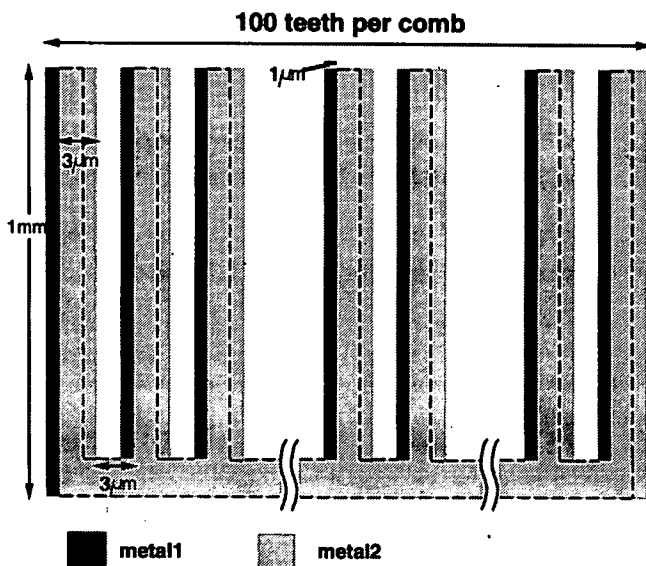

Fig. 2.   Schematic diagram of a test structure with an offset of 1 μm between the lower and upper combs.
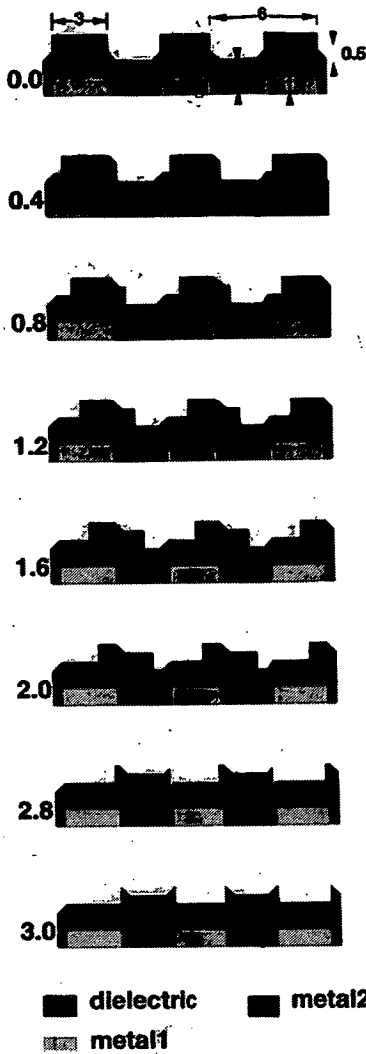
Fig. 3. Cross sections of a small part of the test structure showing increasing offset of metal2, with oxide planarity of 50%. The number to the left of each figure is the amount of offset. All measurements are in microns.

Fig. 4. Layout of the whole set of test structures.

Fig. 5. The three different step coverage slopes for which simulations were performed.

are shown. The degree of planarization can be defined as a percentage, which relates to the amount by which the original topography has been reduced. For example, 20% planarity describes a situation in which 20% of the original feature height has been removed by planarization.

In reality, the situation is somewhat more complex than in the ideal model in that not only will the tops of the features be removed by CMP, but the areas in between features will also be eroded. The tops of the raised features will normally be removed in preference to other areas, but this selectivity depends largely on the hardness of the polishing pad used.

Reliable characterization of CMP is not straightforward, and the degree of planarization achieved often varies across a wafer. This variation can depend on many factors, including the state of the polishing pad, the distribution of chemical slurry across the pad and wafer, the force with which the wafer is pressed onto the polishing pad, and the thickness and flexibility of the wafer itself. This test structure provides a means of electrically measuring planarization and consequently is ideally suited to wafer-mapping of planarity.
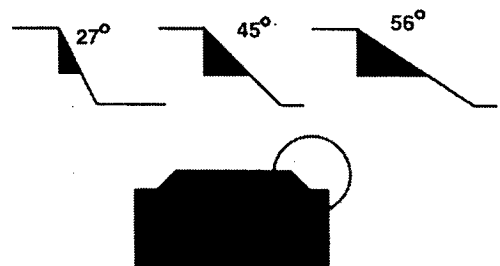
III. TEST STRUCTURE

The basic test structure consists of two identical metal combs, separated by a layer of dielectric [5]. The layout is shown schematically in Fig. 2 for a structure with an offset of 1 μm. To determine the degree of planarity of the dielectric separating the two metal layers a set of structures is required with the teeth progressively offset as schematically illustrated in Fig. 3. For each structure the capacitance between the teeth depends upon the degree of overlap and the planarity of the dielectric. To be able to extract the planarity of the intermetal dielectric it is important to ensure that the misalignment between the metal teeth traverses between complete overlap and zero overlap as shown in Fig. 3.

Fig. 4 shows an example of the layout of an entire set of test structures for which the upper comb has been progressively offset from the lower comb by 0.2 μm. In this design each structure has 100 teeth which are each 1000 μm long, 3 μm wide, and spaced 3 μm apart. The set of structures
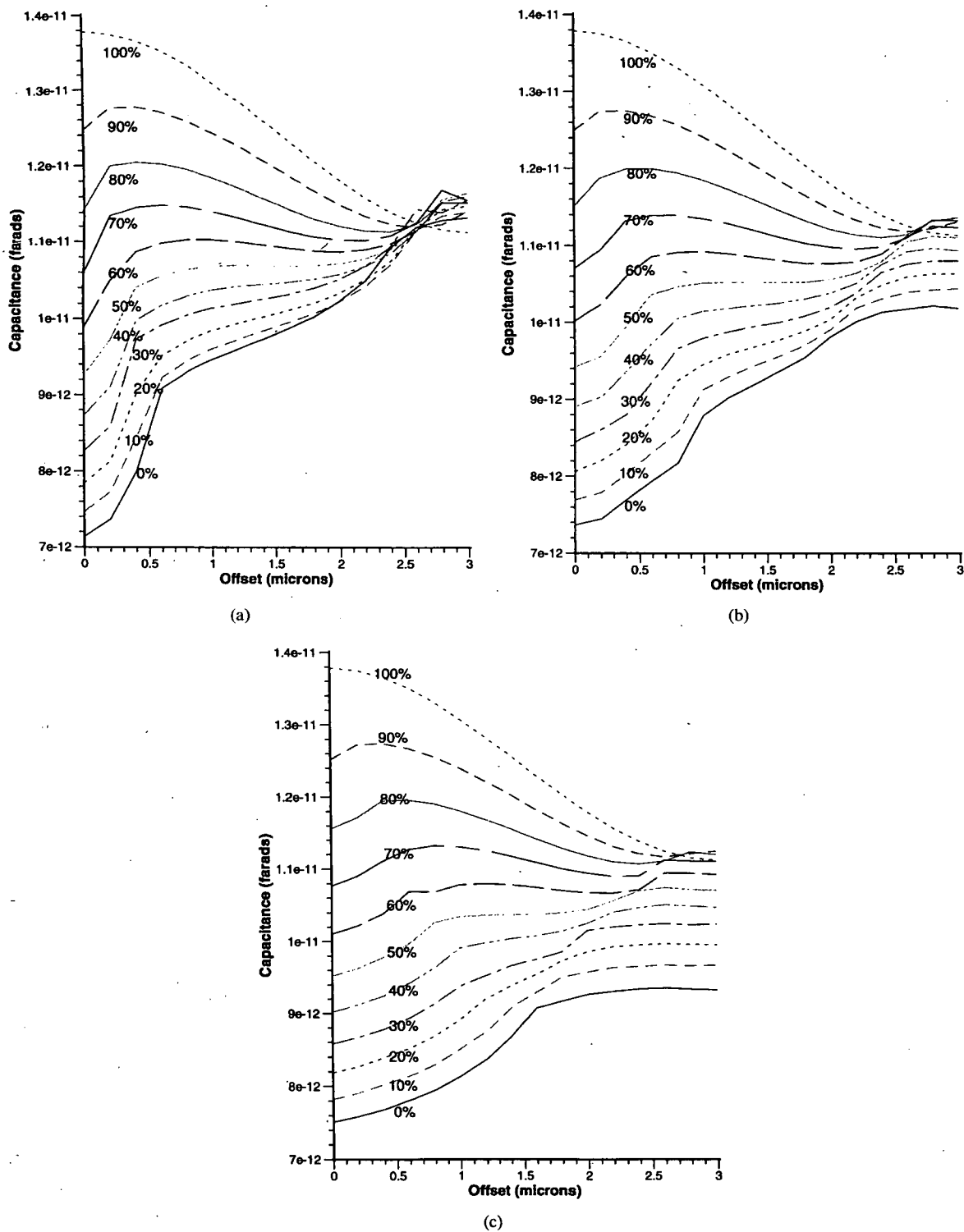
Fig. 6. (a) Capacitance as a function of offset for an oxide step of slope 27° for planarities ranging from 0% to 100%. (b) Capacitance as a function of offset for an oxide step of slope 45° for planarities ranging from 0% to 100%. (c) Capacitance as a function of offset for an oxide step of slope 56° for planarities ranging from 0% to 100%.

schematically shown in Fig. 4 consists of 30 pairs of combs, with offsets between the upper and lower level combs ranging from 0.0 to 5.8 μm. This range of structures ensures that the measurement is robust to expected misalignments between metal1 and metal2 with the range of overlaps illustrated in Fig. 3 always being available for measurement. Note that because of the 0.2 μm increment and random nature of the expected misalignment, the structures available for extracting the degree of planarity may be offset by up to ±0.1 μm from those shown in Fig. 3. However, since accurate alignment between the two metal layers is not a fundamental consideration this does not affect the measurement.

Fig. 7. Capacitance as a function of offset for three oxide thicknesses. The oxide is 50% planar in all three cases.

Fig. 8. Cross sections of oxide with thicknesses of 1.0, 1.5, and 2.0 μm and 50% planarity.

IV. SIMULATION RESULTS

Two-dimensional (2-D) capacitance simulations have been used to examine the relationship between the intercomb capacitance and a range of offsets for planarities ranging from 0% to 100%. The simulations were performed using TMA's Raphael software and were carried out for a small section of the structure comprising of ten teeth from each metal layer. Due to the repetition of this section within the whole structure, the capacitance between the complete combs could be determined by scaling the results for the smaller section by a factor of ten, thus greatly reducing the CPU time. Typical times to simulate the capacitance of this small section for a given offset were around 2 min on a Sun IPX workstation. The data describing the structure being simulated was generated semi-automatically by using equations with variable parameters in the Raphael input file. The number of grid points used in each simulation was 15 000.

Sets of simulations were performed for step coverages with slopes of $27°$, $45°$, and $56°$ as illustrated in Fig. 5. The slope of the dielectric step coverage over metal1 is assumed to be constant as shown in Fig. 5. Fig. 6(a) shows shows the relationship between the comb capacitance and the offset for a slope of $27°$ with Fig. 6(b) showing the variation for a $45°$ slope and Fig. 6(c) showing the results for a slope of $56°$.

With increasing planarity, the oxide thickness directly above metal1 decreases as the raised oxide is polished away. This accounts for the increase in zero offset capacitance as the dielectric is planarized. It can be observed that this increase in capacitance becomes smaller as the finger overlap reduces. However, the shape of the curves is dominated by the topography of the intermetal dielectric, which enables the degree of planarity to be extracted. It can be seen from Fig. 6(a)–(c) that with increasing planarity, the gradient of the central part of the curves decreases progressively from a positive to a negative slope. It can also be seen that the gradients of the curves for any given planarity are comparable for each of the oxide step angles.

Simulations indicate that the shape of the capacitance-offset slope depends far more on the planarity of the dielectric than on its thickness. Fig. 7 shows the relationship between the capacitance and offset for different oxide thicknesses with 50%
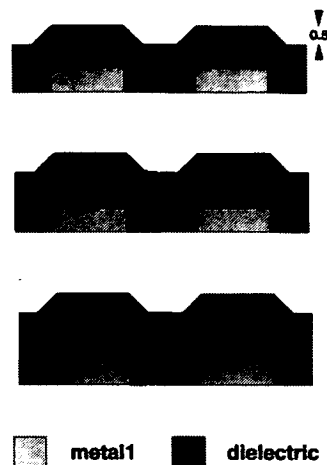
planarity as shown in Fig. 8. Although the oxide thicknesses differ, the shapes of the curves are very similar. This indicates that the test structure can be used to develop processes where the oxide thickness is not necessarily known. These results indicate that the test structure requires that the oxide thickness across a die is constant, although the oxide thickness across the wafer may vary.

V. EXPERIMENTAL WORK

Four wafers with different degrees of planarization were processed. Wafers 1 and 3 had a thin base layer of silicon nitride, while wafer 2 had a thicker layer of oxide covered by a layer of silicon nitride. The aluminum forming the lower teeth in the structures was 1 μm thick and the intermetal dielectric was deposited using electron cyclotron resonance (ECR). The conditions used for the ECR deposition were selected to ensure complete filling of the trenches between the metal1 teeth and a sufficient oxide thickness for the polishing step that followed. The ECR recipe consisted of an initial deposition using the "planar" mode (pressure = 7 mTorr, RF power = 280 W, and table height = 80 cm) to ensure that trenches would be filled. This was then followed by a 1 h deposition in the "nonplanar" mode, to produce the required oxide thickness.

Following the via etch, wafers 2 and 3 were polished, using a Logitech PS2000 system. The slurry used was alkaline colloidal silica, with an expanded polyurethane pad. The pad rotated at 30 rpm, with a downward pressure on the wafer of 0.0026 Kg mm^{-2}. Wafer 1 was not polished, wafer 2 received a 5-min polish and wafer 3 a 10-min polish. After polishing a Nanospec was used to produce a contour map of the oxide thickness of each wafer to determine the global uniformity of the dielectric. Topographical measurements of the wafer surface were also made at individual sites to determine the degree of local planarity using a Dektak surface profiler.

The wafer maps indicated that the oxide was not being polished at a constant rate with variations of 0.25 μm on wafer 1, 0.35 μm on wafer 2 and 0.8 μm on wafer 3. The rate at which oxide had been removed was found to be greatest at the edges of the wafers. It should be noted that there was a
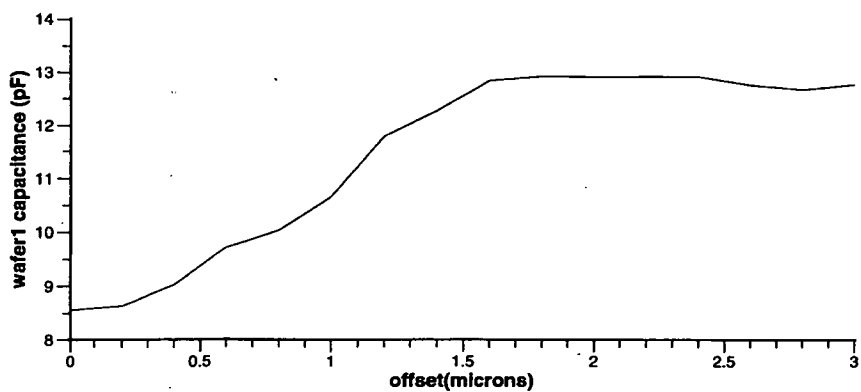
(a)
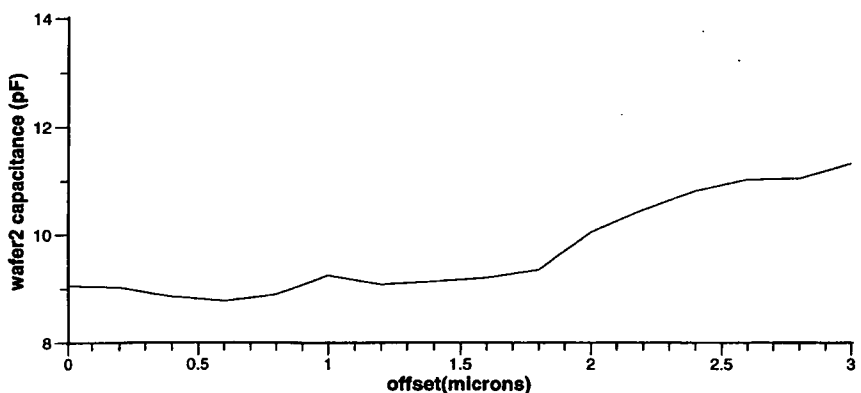
(b)
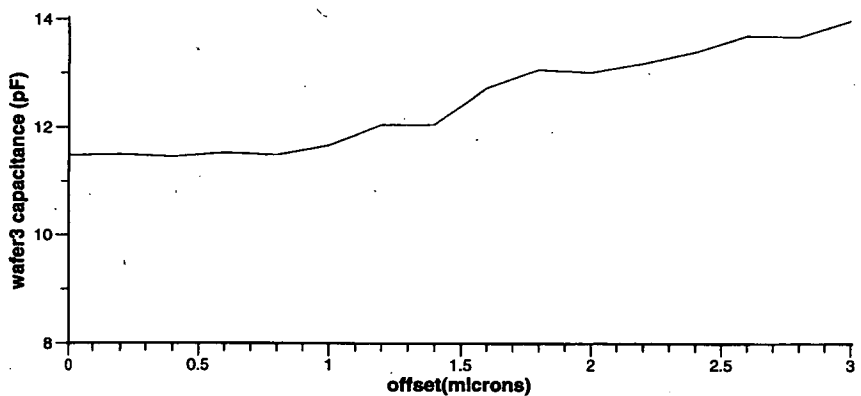
(c)
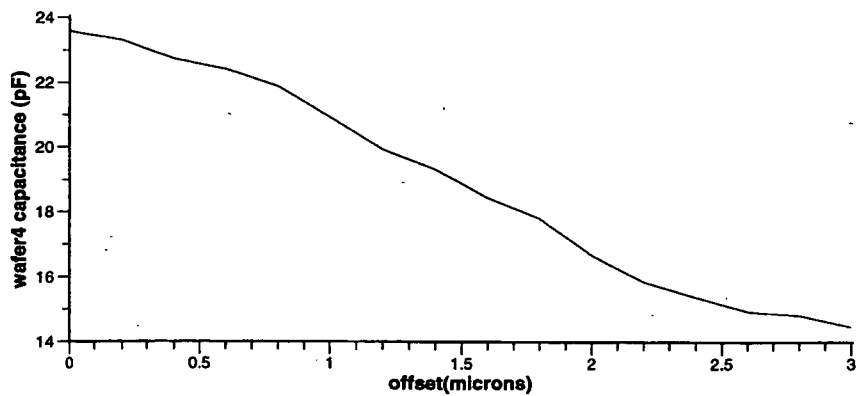
(d)
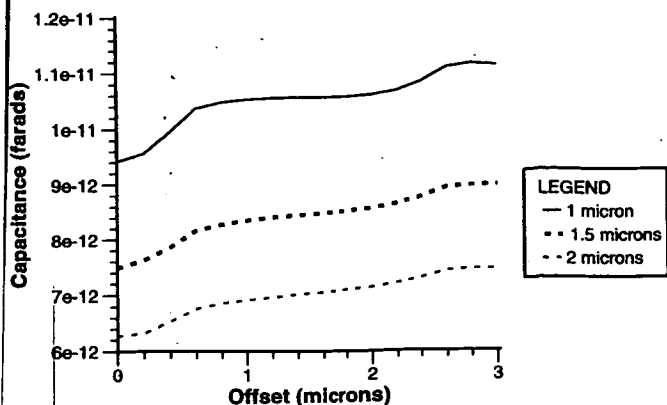
Fig. 9.   (a) Capacitance as a function of offset for structure on wafer 1. (b) Capacitance as a function of offset for structure on wafer 2. (c) Capacitance as a function of offset for structure on wafer 3. (d) Capacitance as a function of offset for structure on wafer 4.
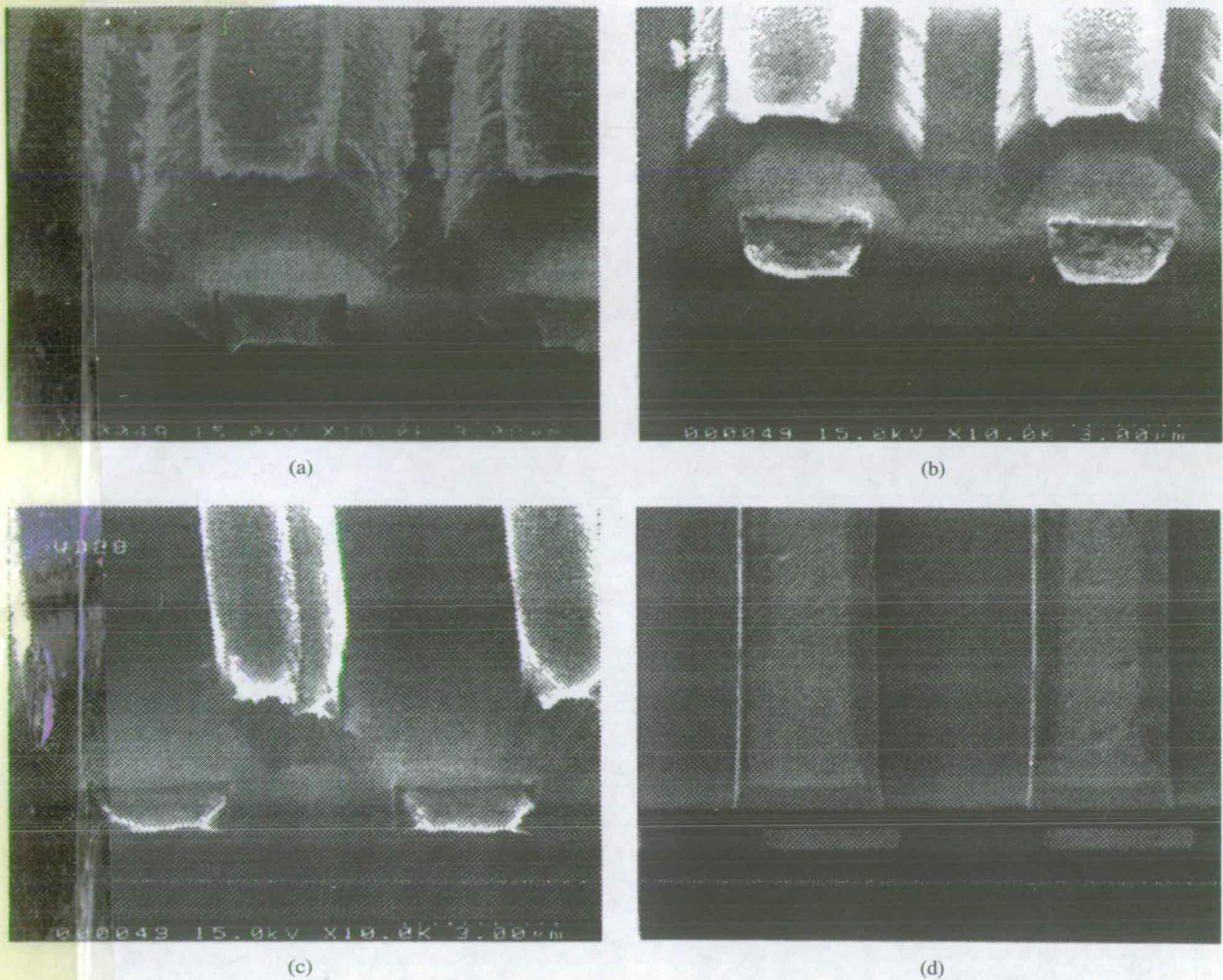
Fig. 10.   (a) Cross section of wafer 1. (b) Cross section of wafer 2. (c) Cross section of wafer 3. (d) Cross section of wafer 4.

variation in the ECR oxide thickness on the wafers prior to polishing. Local topographical measurements taken with the Dektak surface profiler indicated that the maximum vertical feature sizes of the wafers after polishing were 0.5–0.65 μm on wafer 2 and 0.2–0.5 μm on wafer 3. The Dektak results are useful only as an indication of the relative planarity of the wafers since the 12 μm stylus used was larger than individual features on the wafer surface.

After these measurements 1 μm of aluminum was deposited. When patterning this layer, the resist was deliberately overexposed to ensure that no resist remained in the oxide trenches, resulting in a reduced metal2 linewidth.

A different approach was taken with wafer 4. The aim was to produce the situation where the interlayer dielectric was 100% planar. With CMP, the more the interlayer dielectric is polished, the more nonuniform the resulting oxide thickness becomes. The structure reported in this paper requires that the oxide thickness across each die be as constant as possible. Typically, manufacturers of industrial polishers quote a global variation across a wafer of better than 5%. To ensure that the dielectric thickness across each die was as uniform as possible, while at the same time exhibiting 100% planarity, wafer 4 was fabricated using damascene processing.

ECR oxide was deposited to a thickness of 0.5 μm on top of 2.5 μm of thermal oxide, and 0.5, 0.5 μm deep trenches were etched. Then 1 μm of aluminum was deposited and polished back until level with the underlying oxide using the Logitech system with a downward force of 0.000 65 Kg mm^{-2}, a pad rotation of 30 rpm, and a proprietary slurry. Once the oxide was exposed, the polishing was stopped and another 0.5 μm of ECR oxide deposited. Vias were patterned and etched as for wafers 1–3.

Surface profiles taken with the Dektak indicated that any dishing and erosion were slight (less than 0.05 μm). Finally, 0.5 μm of aluminum was deposited, patterned, and etched to form the upper combs.

VI. Measurement and Experimental Results

Using the oxide thickness contour maps taken prior to metal2 deposition, sites were chosen on wafers 1–3 at which the oxide thickness was similar. The oxide thickness across wafer 4 was assumed to be constant. The capacitance between the two layers of metal was measured for each set of test structures, and the relationship between offset and capacitance plotted. To ease the comparison of the measured and simulated results, the point was determined where each graph was

ymmetrical, and the mean of the results to either side of this midpoint plotted. These results are shown in Fig. 9 with the corresponding wafer cross sections shown in Fig. 10.

Inspection of the SEM cross sections indicates that, of the slopes simulated, the angle of step coverage is closest to the 56° slope. Consequently this is the set of simulation curves with which the curve shapes in Fig. 9 have been compared in order to determine the degree of planarity. Inspection of Fig. 9(a) shows a curve which indicates that the planarity is around 0%. Fig. 9(b) and (c) appear similar to one another and an initial inspection indicates that they lie in the 30% to 50% planarity range. However, Fig. 9(b) reaches an increase in gradient at a higher offset than that in (c), indicating that the planarity of wafer 2 is less than wafer 3. Comparisons with the simulations suggest that the planarity of wafer 2 is around 30%, while that of wafer 3 is around 50%. The SEM cross sections of wafers 1, 2, and 3 show a correlation between these results and the observed planarity. Fig. 9(d) has a negative slope, as expected for a 100% planar interlayer dielectric. The gradient is steeper than that for the simulation results, which may be due to the fact that the first layer of aluminum was only 0.5 μm thick, compared to the 1 μm simulated. This would reduce the capacitance between the sides of the lower teeth and the base of the upper teeth, and lead to a lower capacitance at larger offsets. Provided dishing of the metal is slight, it is not expected to have a noticeable effect on the results, since the interlayer dielectric will still have a constant thickness. Fig. 10(d) shows that any dishing of the metal is negligible.

It should be realized that the simulated structures are at best an approximation to those fabricated. These assumed 3.0 μm teeth on a 6.0 μm pitch with a dielectric slope of 56°. The shape of the slope is a fairly crude approximation and the teeth on the fabricated structures were 2.4 μm wide on wafers 1–3. Since for wafers 1–3, two layers of ECR oxide were deposited using different processes the dielectric constant of the layers will be different [in fact the two layers can be identified in the cross sections of Fig. 10(a)–(c)]. As a consequence the effective dielectric constant will change depending on the amount of polishing a wafer has received.

VII. DISCUSSION AND CONCLUSIONS

The test structure presented provides a means of electrically testing the degree of planarization of interlayer dielectrics. It depends on the fact that the capacitance between two metal combs will vary as the horizontal offset between them changes, and that this variation will depend on the shape of the oxide separating them. The gradient of a graph of capacitance between the combs as a function of offset can be used to estimate the degree of planarization with negative gradients indicating planarization greater than 70%. Further work is required to fully quantify the effect of variations in oxide thickness across a set of structures although some indication is given in Fig. 7. It is expected that plate capacitors could be fabricated surrounding the structure to assist in this investigation.

The structure reported in this paper has been designed to allow for a far higher misalignment between layers than would normally be experienced, and has a small incremental offset between the two layers. If space is at a premium it would be possible to reduce the number of individual structures by considering only offsets from 0.0 μm to 3.0 μm, and one or two structures just outside this range to allow for some misalignment. The number of offsets considered within this range could also be reduced, thus reducing the number of structures required still further. The structure presented in this paper was designed such that the capacitance measured would be high in relation to noise introduced in the measurement system. If measurement equipment allows, the number of teeth per comb could be reduced, further decreasing space requirements. When characterising processes in which interconnect widths will be smaller than 3 μm, it is possible to scale the structure accordingly. Providing everything is scaled by the same amount in both the horizontal and vertical directions, the graphs of capacitance vs offset will be exactly the same as those for the structures presented in this paper. The technique is applicable to situations where oxide and metal thicknesses scale differently to line widths, but in this case simulations should be rerun to determine the exact gradients expected for each degree of planarization.

REFERENCES

[1] S. R. Wilson, C. J. Tracy and J. L. Freeman, Jr., *Handbook of Multilevel Metallization for Integrated Circuits*. New Jersey: Noyes, 1993, pp. 346–439.
[2] J. P. Elliott, G. A. Allan and A. J. Walton, "Automating the calculation of 3d interconnect parasitics," in *Proc. IEE Colloq. Advanced MOS and Bi-polar Devices*, Feb. 1995, pp. 15/1–15/2.
[3] G. J. Gaston and I. G. Daniels: "Efficient extraction of metal parasitic capacitances," *Proc. ICMTS*, Nara, Japan, Mar. 1995, pp. 157–160.
[4] K. Aoyama, K. Ise, H. Sato, K. Tsuneno and H. Masuda, "A new characterization of sub-micron parallel multilevel interconnects and its experimental verification," in *Proc. ICMTS*, Nara, Japan, Mar. 1995, pp. 63–66.
[5] J. P. Elliott, M. Fallon, A. J. Walton, J. T. M. Stevenson and A. O'Hara, "A test structure for the measurement of planarization," in *Proc. ICMTS*, Trento, Italy, Mar. 1996, pp. 301–305.

Jane P. Elliott (M'96) received the MEng degree in electronics in 1992 from the University of Edinburgh, U.K.

She spent two years working as an IC design engineer at Motorola, East Kilbride, U.K., before returning to the University of Edinburgh as a Research Associate. Her main research interests are in IC topography and parasitics, an area in which she is currently pursuing the Ph.D. degree.

Martin Fallon received the honors degree in physics and astronomy from the University of Glasgow, U.K.

He then joined General Instruments Microelectronics. In 1984, he took up a research post in the Edinburgh Microfabrication Facility and received the Ph.D. degree. In 1990, he was a Visiting Scientist at The ElectroTechnical Laboratory, Tsukuba, Japan, where he worked on the effects of ion implantation into dielectric materials. After a year teaching at Napier University, Edinburgh, U.K., he rejoined Edinburgh University in 1993 to work in R&D, particularly in the areas of simulation and experimental design. His areas of interest are in process and device modeling and back end test.

Anthony O'Hara received the B.Sc. degree in physics in 1985 from Heriot-Watt University, U.K. He joined the Medical Laser Unit and received the Ph.D. degree for research in laser physics in 1990.

He then started a research post at the University of Edinburgh where he developed a multilevel metallization process which included planarization using CMP. His research interests are CMP, damascene processing, and interconnect.

Anthony J. Walton (M'88), for a photograph and biography, see this issue, p. 195.

J. T. M. Stevenson received the B.Sc. degree in physics in 1967 and the M.Sc. degree in instrument design in 1969 from the University of Aberdeen, U.K.

He spent five years at Ferranti Ltd, Dalkeith, U.K., as a development engineer on moire measuring systems. In 1974, he joined the Wolfson Microelectronics Institute to work on the design of a pattern generator for the production of integrated circuits. In 1980, he was appointed to a research fellowship in the Edinburgh Microfabrication Facility, University of Edinburgh, from which he received the Ph.D. degree in 1988. His main research interests are in optical lithography and optical measurement techniques.

Alan M. Gundlach received the B.Sc. degree in physics in 1959 and the M.Sc. degree in 1965, both from the University of London, U.K.

He was employed in the semiconductor industry for 19 years from 1959, initially with A.E.I. Radio and Electronics Components Division and with Texas Instruments Ltd. working on the manufacture of bipolar discrete devices and integrated circuits and, latterly, with Elliott Automation Microelectronics Ltd. and with General Instrument Microelectronics Ltd. as MOS Process Development Manager. In 1978, he was appointed to a Senior Research Fellowship at the University of Edinburgh in the role of Operations Manager of the Edinburgh Microfabrication Facility in which capacity he has been responsible for designing and installing processes ranging from silicon machining to complete CMOS fabrication sequences.

Electrical Assessment of Planarisation for CMP

J.P. Elliott, M.Fallon†, A.J. Walton, J.T.M. Stevenson, A.O'Hara, A Shaffi†,
C.M. Reeves
Edinburgh Microfabrication Facility
Department of Electrical Engineering
Kings Buildings, University of Edinburgh
Edinburgh, EH9 3JL

Abstract

Experimental measurements of an electrical test structure for use in assessment of the degree of planarisation of inter-layer dielectrics are presented and compared with theoretical predictions. The test structure consists of two sets of metal combs separated by a dielectric. For each structure the combs on the two layers overlap each other by some degree, with adjacent structures having the overlap in one direction progressionally offset by $0.2\mu m$. It is demonstrated theoretically that the structure is robust to expected levels of oxide thickness variation.

1. Introduction

The trend towards reduced device dimensions has led to an increase in IC interconnect density, resulting in ever more layers of metallisation. Problems associated with this development are poor step coverage, increased interconnect resistance, poor circuit reliability and poor tolerance of the decreasing depth of focus in lithography exposure tools. Planarisation of inter-layer dielectrics can help to solve these problems [1], and can also decrease the value of parasitic interconnect capacitances [2].

This paper presents a test structure which can be used to determine the degree of planarisation using electrical measurements. Both simulated and experimental results are presented, along with an analysis of the sensitivity of the structure to oxide thickness variations.

2. Test Structure

The basic test structure consists of 2 identical combs, each with 100 teeth, on metal layers separated by a layer of dielectric [3,4]. The teeth are $1000\mu m$ long, $3\mu m$ wide and spaced $3\mu m$ apart. The dielectric separating the two sets of metal fingers is the layer whose degree of planarity is to be determined. The planarity of this layer is defined as a percentage which relates to the amount by which the original topography has been reduced. For example, 20% planarity describes a situation in which 20% of the original feature height has been removed by planarisation.

In order to be complete, a set of experimental results must cover offsets from $0\mu m$ to $3\mu m$ as shown in figure 1. The inter-layer dielectric in this case is 50% planar. A set of test structures consists of 30 pairs of combs, with offsets between the combs ranging from $0\mu m$ to $5.8\mu m$. This ensures that in spite of any misalignment between the upper and lower combs, the entire range of offsets required will be available to within $0.1\mu m$.

3. Simulation Results

Two dimensional capacitance simulations have been used to examine the relationship between the inter-comb capacitance and a range of offsets for planarities ranging from 0% to 100% [3,4]. The simulations were performed using TMA's Raphael software for a small section of the structure comprising 10 teeth from each metal layer. Due to the repetition of this section within the structure, the capacitance between the complete combs was determined by scaling the results for the smaller section by a factor of 10, thus greatly reducing the CPU time required. Typical times to simulate this small section for a given offset were around 2 minutes on a Sun IPX workstation. The data describing the structure being simulated was generated semi-automatically by using equations with variable parameters in the Raphael input file. The number of grid points used in each simulation was 15,000.

Simulations were carried out for oxide step slopes of 27°, 45° and 56°. These slopes were assumed to be constant, as shown in figure 2. Figure 3 shows the relationship between the comb capacitance and the offset for an oxide step slope of 56°. As the dielectric is polished, the thickness of the raised oxide directly above metal1 decreases, which accounts for the increase in zero offset capacitance as the dielectric is planarised. The reduction in the oxide thickness above the metal1 teeth has a diminishing effect on the simulated capacitance as the offset between the upper and lower teeth increases. The shape of the curves is dominated by the topography of the inter-metal dielectric, which enables the degree of planarity to be determined. It can be seen from figure 3 that with increasing planarity the gradient of the central part of the curve decreases progressively from positive to negative.

Figure 2. The three different step coverage slopes for which simulations were performed.
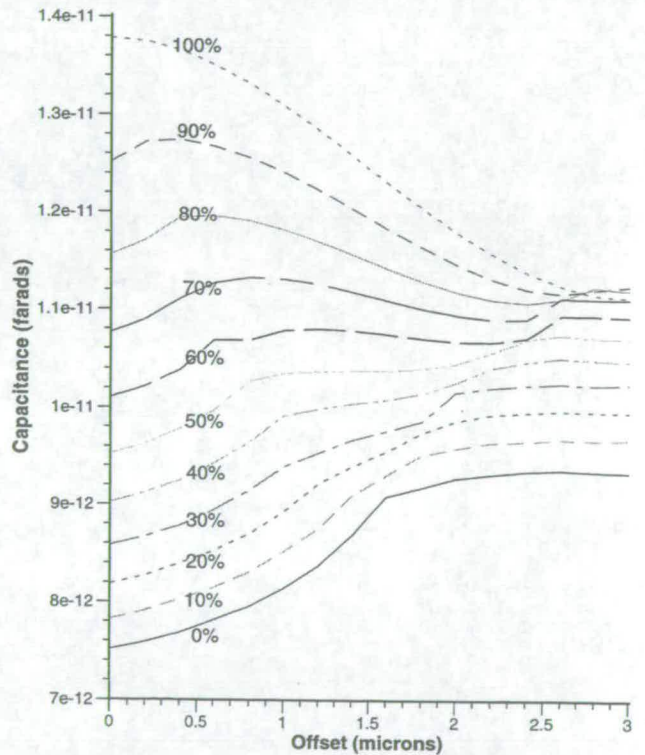
Figure 3. Capacitance as a function of offset for an oxide step of slope 56 ° for planarities ranging from 0% to 100%.
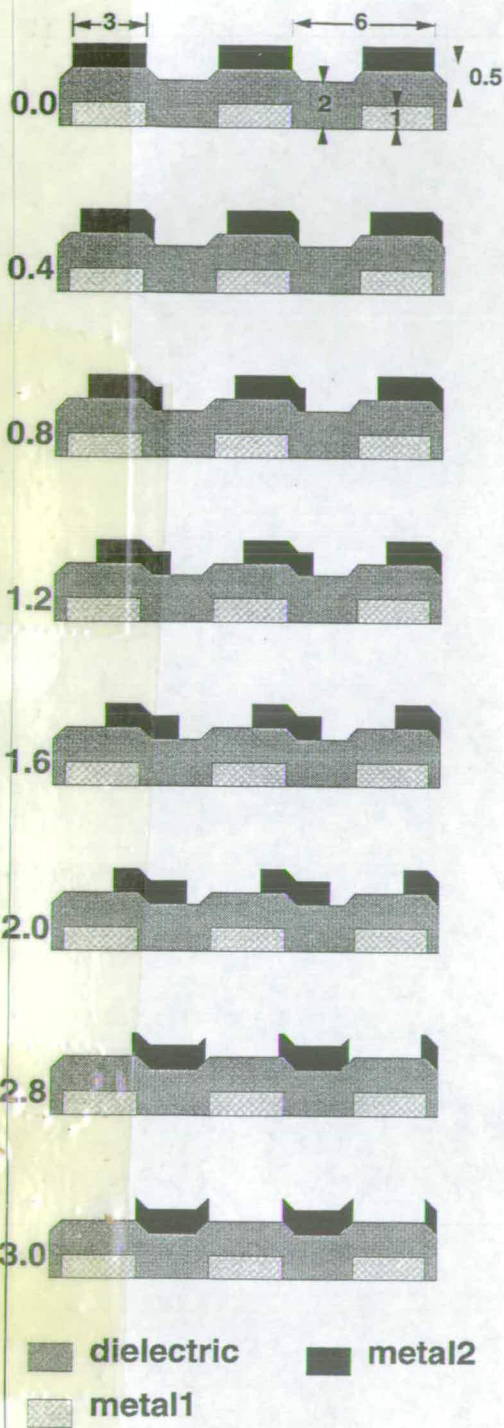
dielectric **metal2**

metal1

Figure 1. Cross sections of a small part of the test structure showing increasing offset of metal2, with oxide planarity of 50%. The number to the left of each figure is the amount of offset. All measurements are in microns.

4. Sensitivity to Oxide Thickness Variation

Ideally the offset of the upper teeth from the lower teeth will be the only variable across a set of structures. However, there will always be a degree of non-uniformity across a wafer, and therefore across a die. Typical uniformities quoted by polisher manufacturers are now less than 5% across a 200mm wafer with an exclusion area of 5 or 6mm around the wafer edge [5]. This translates to a uniformity of less than 0.2% across a die containing all 30 structures with a size of approximately 5mm by 5mm.

Figure 4(a). Capacitance as a function of offset for a 0% planar oxide of thickness 1μm, varied by 1% and 5%.

Figure 5(a). Capacitance as a function of offset for a 0% planar oxide of thickness 2μm, varied by 1% and 5%.

Figure 4(b). Capacitance as a function of offset for a 50% planar oxide of thickness 1μm, varied by 1% and 5%.
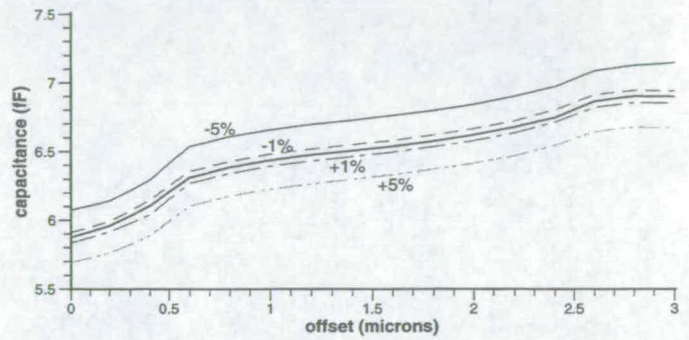
Figure 5(b). Capacitance as a function of offset for a 50% planar oxide of thickness 2μm, varied by 1% and 5%.

Figure 4(c). Capacitance as a function of offset for a 100% planar oxide of thickness 1μm, varied by 1% and 5%.

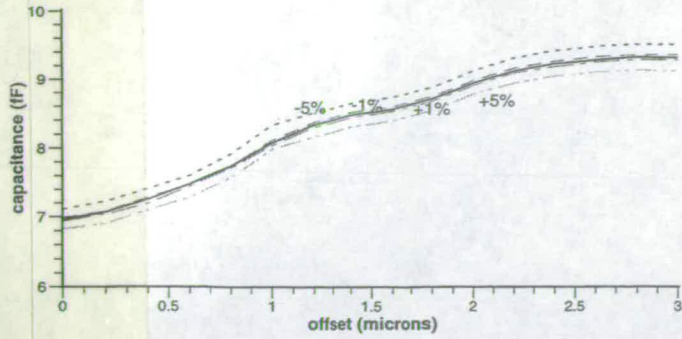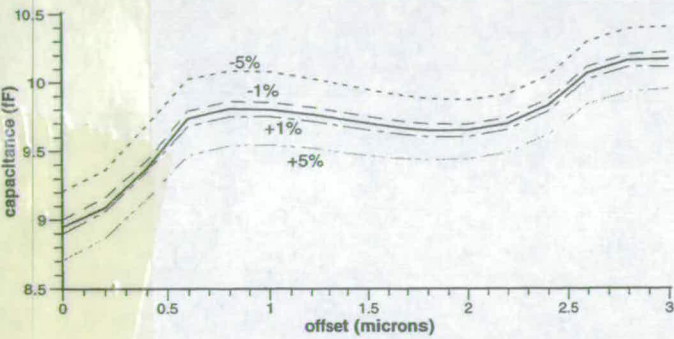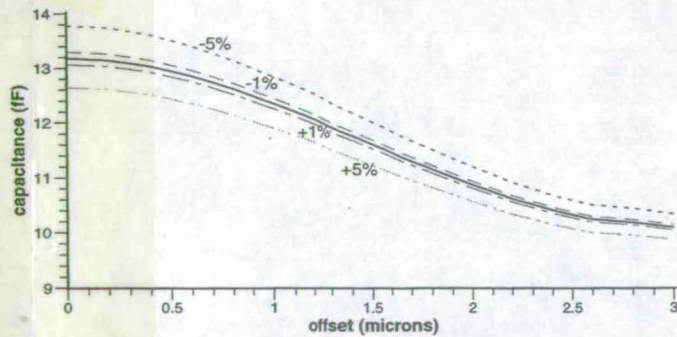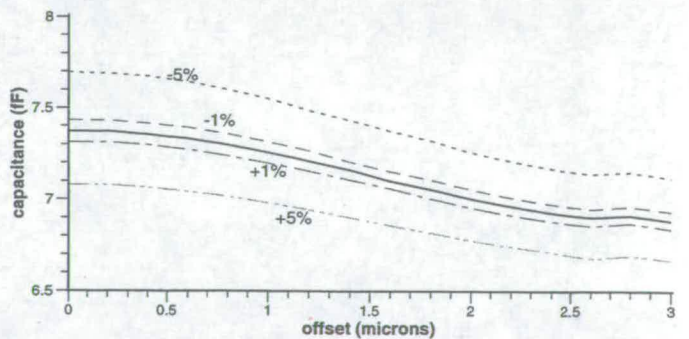Figure 5(c). Capacitance as a function of offset for a 100% planar oxide of thickness 2μm, varied by 1% and 5%.

Simulations were carried out to determine the sensitivity of the structure to oxide thickness variations. Oxide thicknesses of 1μm and 2μm with planarities of 0%, 50% and 100% were simulated. The oxide thickness was then varied by ±1% and ±5%. The results for the 1μm and 2μm thick inter layer dielectrics are shown in figures 4 and 5. From these curves it can be seen that if the oxide thickness varies by 2% (±1%), the shape of the curve remains very similar to the 1μm oxide thickness curve. An oxide thickness variation of 10% (±5%) could produce a very different curve, but such an extreme level of non-uniformity across a die would be very unlikely if a well calibrated polisher were used. Table 1 shows the percentage change in simulated capacitance for various oxide thickness

variations. These results and the curves shown in figures 4 and 5 indicate that the test structure is certainly robust to a uniformity in oxide thickness of 2%, which is well outside the likely quoted uniformity.

	1μm±1%	1μm±5%	2μm±1%	2μm±5%
0%	0.38	2.05	0.64	2.96
50%	0.49	2.49	0.67	3.29
100%	0.67	3.34	0.74	3.69

Table 1. Percentage variation of capacitance from original value when oxide thickness is varied by 1% and 5%.

5. Experimental Work

Five wafers with different degrees of planarisation were fabricated. Wafers 1 to 4 were conventionally processed, while a damascene process was used for wafer 5. For wafers 1 to 4, the aluminium forming the lower teeth in the structures was $1\mu m$ thick and the inter-metal dielectric was deposited using Electron Cyclotron Resonance (ECR). The conditions used for the ECR deposition were selected to ensure complete filling of the trenches between the metal1 teeth and a sufficient oxide thickness for the polishing step that followed. The ECR recipe consisted of an initial deposition using the 'planar' mode (with pressure = 7 mTorr, RF power = 280W and table height = 80 cm) to ensure the trenches were filled. This was then followed by a 1 hour deposition in the 'non-planar' mode, to produce the required oxide thickness.

Following the via etch, selected wafers were polished using a Logitech PS2000 system. The slurry used was alkaline colloidal silica, with an expanded polyurethane pad. The pad rotated at 30 rpm, with a downward pressure on the wafer of 0.0026 $Kg\ mm^{-2}$. Wafer 1 was not polished, wafer 2 received a 5 minute polish, wafer 3 a 10 minute polish and wafer 4 a 24 minute polish. After polishing, a Nanospec was used to produce a contour map of the oxide thickness of each wafer to determine the global uniformity of the dielectric. Topographical measurements of the wafer surface were also made at individual sites to determine the degree of local planarity using a Dektak surface profiler.

The wafer maps indicated that the oxide was not being polished uniformly, with variations of $0.025\mu m$ on wafer 1, $0.35\mu m$ on wafer 2, $0.8\mu m$ on wafer 3 and $1.2\mu m$ on wafer 4. The rate at which oxide had been removed was found to be greatest at the edges of the wafers. It should be noted that there was a variation in the ECR oxide thickness on the wafers prior to polishing. Local topographical measurements taken using the Dektak surface profiler indicated that the maximum feature height on the wafers after polishing was $0.5 - 0.65\mu m$ on wafer 2, 0.2-$0.5\mu m$ on wafer 3 and 0.02-$0.06\mu m$ on wafer 4. The Dektak results are useful only as an indication of the relative planarity of the wafers since the $12\mu m$ stylus used was larger than individual features on the wafer surface. After these measurements $1\mu m$ of aluminium was deposited. When patterning this layer, the resist was deliberately overexposed to ensure that no resist remained in the oxide trenches, resulting in a reduced metal2 linewidth.

Due to the poor global uniformity on wafer 4, a fifth wafer was processed using damascene processing to obtain reliable results for the 100% planar case. Over $2\mu m$ of thermal oxide was deposited, followed by $0.5\mu m$ of non-planar mode ECR oxide. This was deposited using a table height of 80cm, the lowest available, to ensure that the deposition was as uniform as possible. The oxide was then patterned with the inverse metal1 mask, and etched to a depth of $0.5\mu m$. $1\mu m$ of aluminium was sputtered onto the wafer, filling the oxide trenches and completely covering the oxide between the trenches. The aluminium was polished back until level with the underlying oxide using the Logitech system, with a much reduced
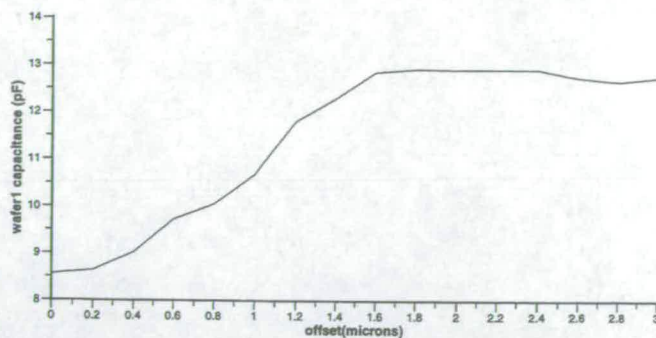

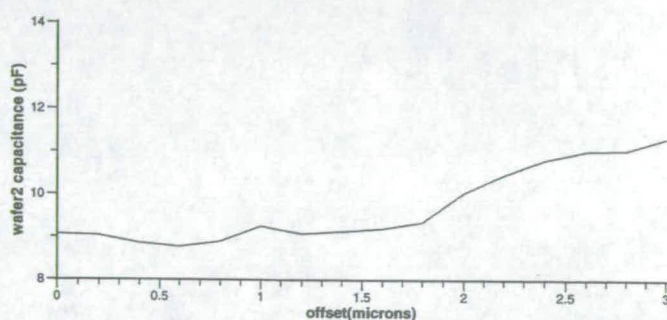Figure 6(a). Capacitance as a function of offset for structure on wafer 1.

Figure 6(b). Capacitance as a function of offset for structure on wafer 2.
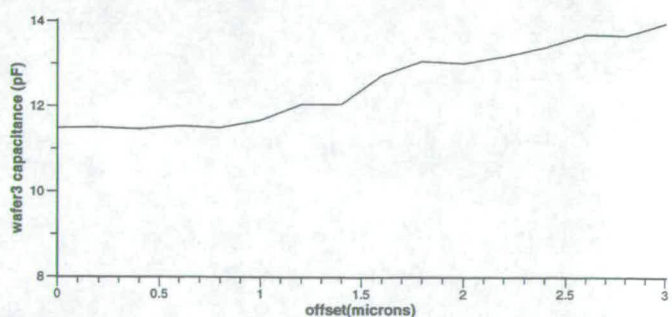
Figure 6(c). Capacitance as a function of offset for structure on wafer 3.
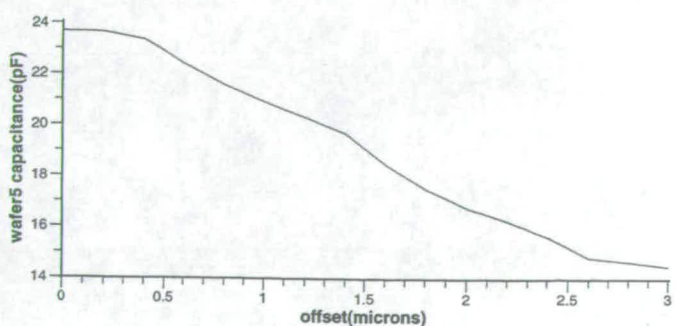
Figure 6(d). Capacitance as a function of offset for structure on wafer 5.
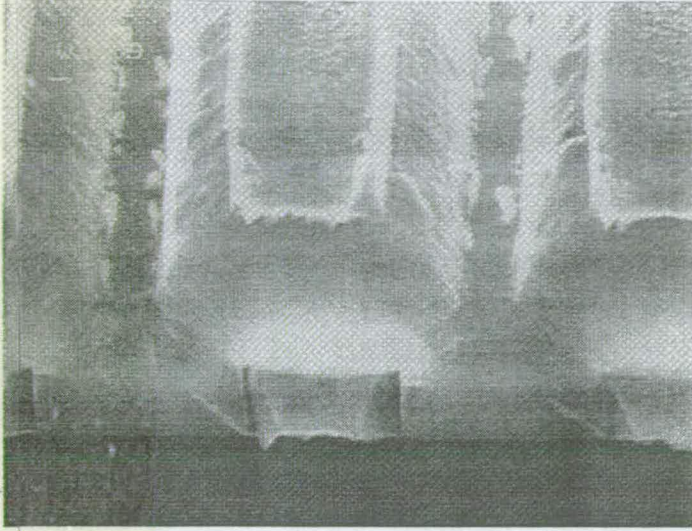
Figure 7(a).   Cross-section of wafer 1.
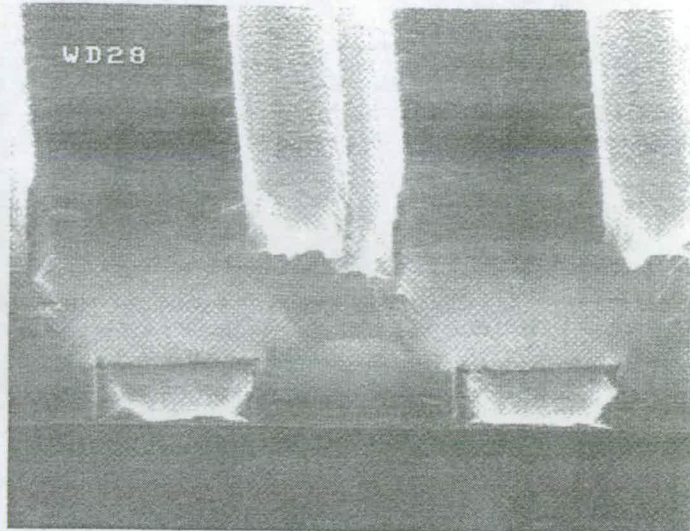
Figure 7(c).   Cross-section of wafer 3.
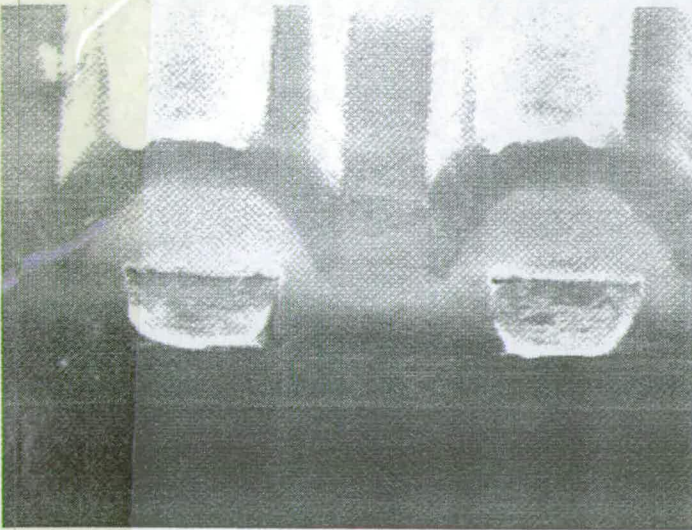
Figure 7(b).   Cross-section of wafer 2.
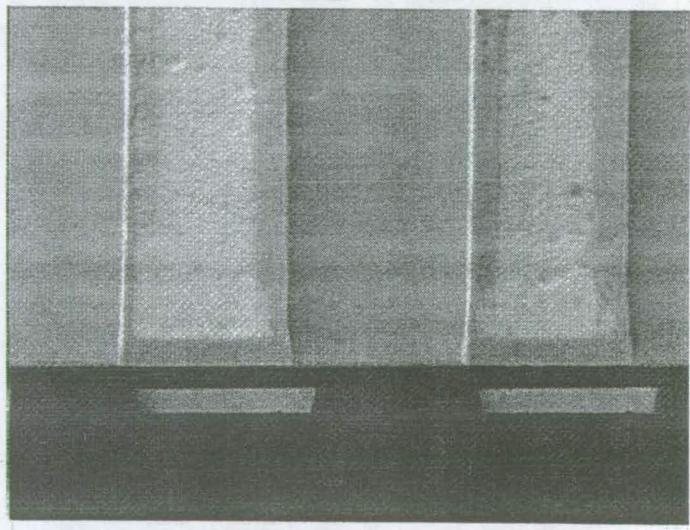
Figure 7(d).   Cross-section of wafer 5.

downwards force of 0.00065 $Kg\,mm^{-2}$, a pad rotation of 30 rpm and a proprietary slurry. All CMP conditions were chosen to minimise dishing and erosion, and polishing was stopped as soon as a good number of die had been sufficiently polished. This resulted in underpolishing of some die, but ensured that those which were sufficiently polished suffered from minimal dishing and erosion. A further 0.5μm of ECR oxide was deposited and vias patterned and etched. Measurements were taken using the Dektak to determine the extent of the dishing and erosion, both of which were found to be approximately 0.03μm. Finally, 0.5μm of aluminium was deposited, patterned and etched to form the upper combs.

6. Measurement and Experimental Results

Using the oxide thickness contour maps taken prior to metal2 deposition, sites were chosen on wafers 1 to 3 at which the oxide thicknesses were similar. The oxide thickness across wafer 5 was assumed to be constant. Wafer 4 was not used for measurements, since every die had an oxide thickness variation of greater than 5%. The effect of this degree of variation is shown in figure 5(c), where offset vs simulated capacitance is plotted for an oxide thickness of 2μm varying by 1% and 5%. This confirms that such a poor uniformity would yield unreliable results.

The capacitance between the two layers of metal was measured for each set of test structures, and the relationship between offset and capacitance plotted. To ease the comparison of the measured and simulated results, the point was determined where each graph was symmetrical, and the mean of the results to either side of this midpoint plotted. These results are shown in figure 6 with the corresponding wafer cross-sections shown in figure 7.

Inspection of the SEM cross-sections indicates that the 56° slope is a reasonable approximation to the fabricated structures, so this set of curves has been compared to the graphs obtained experimentally to determine the degree of planarity. Inspection of figure 6(a) shows a curve which indicates that the planarity is around 0%. Figures 6(b) and 6(c) appear similar to one another and an initial inspection indicates that they lie in the 30% to 50% planarity range. However, figure 6(b) reaches an increase in gradient at a higher offset than that in figure 6(c) indicating that the planarity of wafer 2 is less that wafer 3. Comparisons with the simulations suggest that the planarity of wafer 2 is around 30%, while that of wafer 3 is around 50%. The SEM cross-sections of wafers 1, 2 and 3 show a correlation between these results and the observed planarity.

Figure 6(d) has a negative slope, as expected for a 100% planar inter-layer dielectric. The gradient is steeper than that for the simulation results, which is probably due to the fact that the first layer of aluminium was only $0.5\mu m$ thick, compared to the $1\mu m$ simulated. This would reduce the capacitance between the sides of the lower teeth and the base of the upper teeth, leading to a lower capacitance at larger offsets. Provided dishing of the metal is slight it is not expected to have a noticeable effect on the results, since the inter-layer dielectric will still have a constant thickness. Figure 7(d) shows that any dishing of the metal is negligible.

It should be realised that the simulated structures are at best an approximation to those fabricated. These assumed $3.0\mu m$ teeth on a $6\mu m$ pitch with a dielectric slope of 56°. The shape of the slope is a fairly crude approximation to that on the fabricated structures, and the metal2 teeth were only $2.4\mu m$ wide on wafers 1 to 3. Since for wafers 1 to 3, two layers of ECR oxide were deposited using different processes, the dielectric constant of the layers will be different. In fact, the two layers can be identified in the cross-sections of figures 7(a), 7(b) and 7(c). As a consequence the effective dielectric constant will change depending on the amount of polishing a wafer has received.

Discussion and Conclusions

The test structure presented provides a means of electrically testing the degree of planarisation of inter-layer dielectrics. It depends on the fact that the capacitance between two metal combs will vary as the horizontal offset between them changes, and that this variation will depend on the shape of the oxide separating them. The gradient of a graph of capacitance between the combs as a function of offset can be used to estimate the degree of planarisation with negative gradients indicating planarisation greater than 70%. Simulations indicate that the structure is robust to likely oxide thickness variations.

The structure reported in this paper has been designed to allow for a far higher misalignment between layers than would normally be experienced, and has a small incremental offset between the two layers. If space is at a premium it would be possible to reduce the number of individual structures by considering only offsets from $0.0\mu m$ to $3.0\mu m$, and one or two structures just outside this range to allow for some misalignment. The number of offsets considered within this range could also be reduced, further decreasing the number of structures required. The structure presented in this paper was designed such that the capacitance measured would be high in relation to noise introduced in the measurement system. If measurement equipment allows, the number of teeth per comb could be reduced, further decreasing space requirements. When characterising processes in which interconnect widths will be smaller than $3\mu m$, it is possible to scale the structure accordingly. Providing everything is scaled by the same amount in both the horizontal and vertical directions, the graphs of capacitance vs offset will be exactly the same as those for the structures presented in this paper. The technique is applicable to situations where oxide and metal thicknesses scale differently to line widths, but in this case simulations should be rerun to determine the exact gradients expected for each degree of planarisation.

8. Acknowledgements

9. References

[1]. S.R. Wilson, C.J. Tracy and J.L. Freeman, Jr., "Handbook of Multilevel Metallization for Integrated Circuits", Noyes Publications, 1993, pp 346-439

[2]. J.P. Elliott, G.A. Allan and A.J. Walton, "Automating the Calculation of 3D Interconnect Parasitics", Proc. of IEE Colloquium on "Advanced MOS and bi-polar devices", Feb 1995, pp 15/1 - 15/2

[3]. J.P.Elliott,M.Fallon,A.J.Walton,J.T.M.Stevenson,A.O'Hara, "A Test Structure for the Measurement of Planarisation", Proc. ICMTS, Trento, Italy, March 1996, pp 301-305.

[4]. J.P.Elliott,M.Fallon,A.J.Walton,J.T.M.Stevenson,A.O'Hara, A.M.Gundlach,"An Electrical Test Structure for the Measurement of Planarisation", submitted to IEEE Trans Semiconductor Manufacturing

[5]. Ruth DeJule, "Advances in CMP", Semiconductor International, November 1996, pp 88-96

A Test Structure for the Measurement of Planarisation

J.P. Elliott, M.Fallon†, A.J. Walton, J.T.M. Stevenson, A.O'Hara
Edinburgh Microfabrication Facility
Department of Electrical Engineering
Kings Buildings, University of Edinburgh
Edinburgh, EH9 3JL

Abstract

This paper presents simulations of a test structure that can be used to assess the degree of planarisation of inter-layer dielectrics. It consists of sets of comb structures separated by a dielectric. For each structure the combs on the two layers overlap each other with adjacent structures having the overlap in one direction progressionally offset by 0.2μm. The capacitance of these structures is then measured from which the degree of planarisation can be assessed. This structure has potential applications for characterising Chemical Mechanical Polishing (CMP) processes for multi-level VLSI applications.

1. Introduction

As the density of IC interconnect increases and since the use of several layers of metal is now commonplace, planarisation of circuitry is becoming essential. Benefits of planarising dielectrics for multi-level metallisation include improved step coverage by layers deposited later in the process, increased circuit reliability, and decreased interconnect resistance [1]. Parasitic interconnect capacitances are also decreased by planarisation [2]. This is of particular interest, since interconnect capacitance is of increasing importance in circuit performance [3-4].

The objective of this work is to present a test structure which can be used to determine quickly and easily the degree of planarisation using electrical measurements. This provides a means of electrically assessing planarisation during the development of a process, and for monitoring the degree of planarisation once the process is in production.

2. Planarisation

There are several methods of planarisation. A widely used method is Chemical Mechanical Polishing (CMP) [1], and the test structure described in this paper is ideally suited to evaluate this technology. CMP involves polishing away features on the surface of a wafer, using a mixture of mechanical abrasion and chemical reaction. In the ideal model, the raised features on the
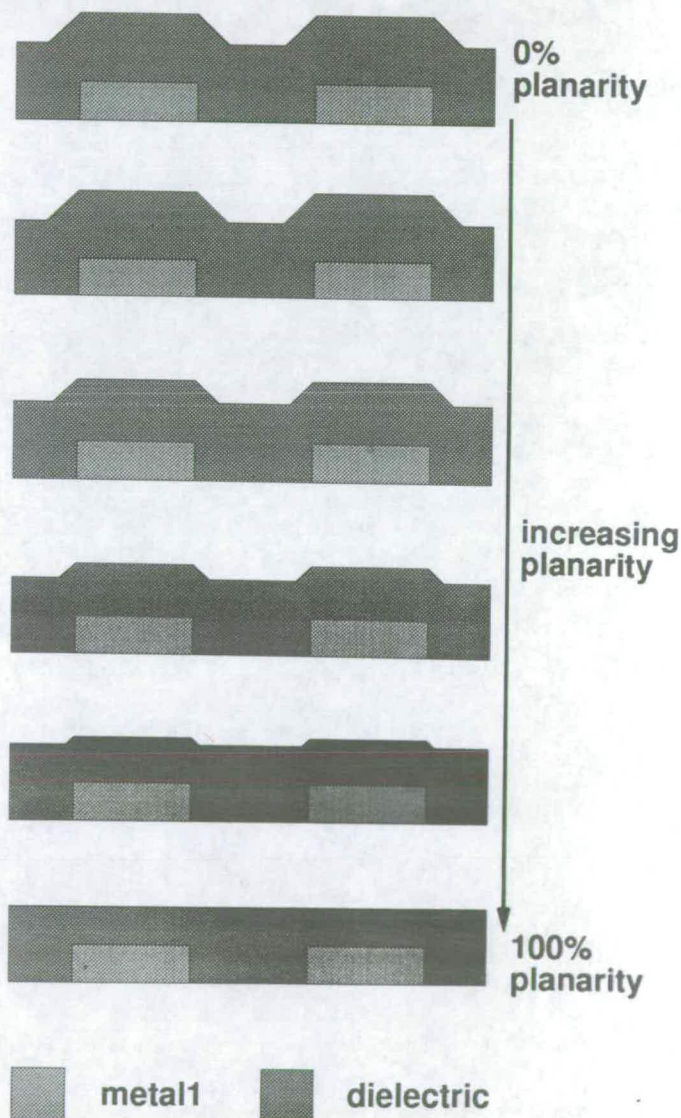
Figure 1. Increasing planarity of dielectric over metal using CMP.

wafer surface will be progressively polished away, eventually resulting in a completely flat surface. This is illustrated in figure 1 where various degrees of planarisation of an oxide are shown.

302

The degree of planarisation can be defined as a percentage, which relates to the amount by which the original topography has been reduced. For example, 20% planarity describes a situation in which 20% of the original feature height has been removed by planarisation.

In reality, the situation is somewhat more complex than in the ideal model in that not only will the tops of the features be removed by CMP, but the areas in between features will also be eroded. The tops of the raised features will normally be removed in preference to other areas, but this selectivity depends largely on the hardness of the polishing pad used on the machine.

Reliable characterisation of CMP is not straightforward, and the degree of planarisation achieved often varies across a wafer. This variation can depend on many factors, including the state of the polishing pad, the distribution of chemical slurry across the pad and wafer, the force with which the wafer is pressed onto the polishing pad, and the thickness and flexibility of the wafer itself. This test structure provides a means of measuring planarisation electrically, and can be used to wafermap planarity.

3. Test Structure

The basic test structure consists of 2 identical combs, each with 100 teeth, on metal layers separated by a layer of dielectric. The teeth are each 1000μm long, 3μm wide, and are spaced 3μm apart. The dielectric separating the two metal layers is the layer whose degree of planarity is to be investigated. A set of test structures has the upper comb progressively offset from the lower comb by 0.2μm. An entire set of test structures consists of 30 pairs of combs, with offsets between the combs ranging from 0μm to 5.8μm. This ensures that in spite of any
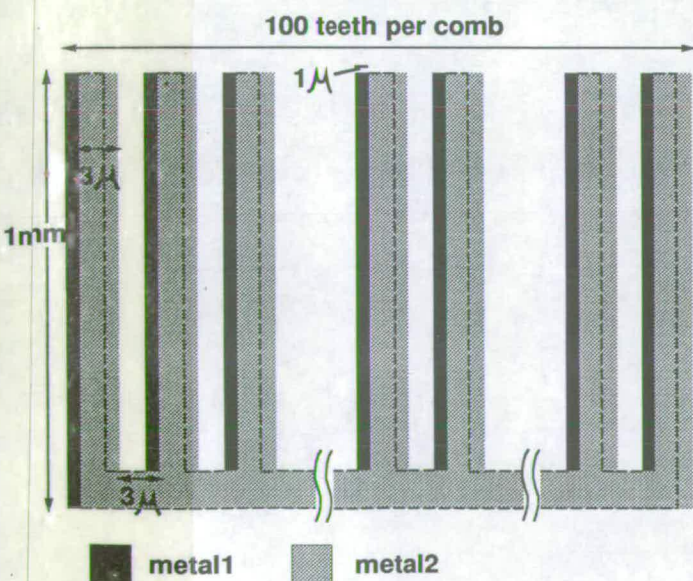
Figure 2. Schematic diagram of a test structure with an offset of 1μm between the lower and upper combs.
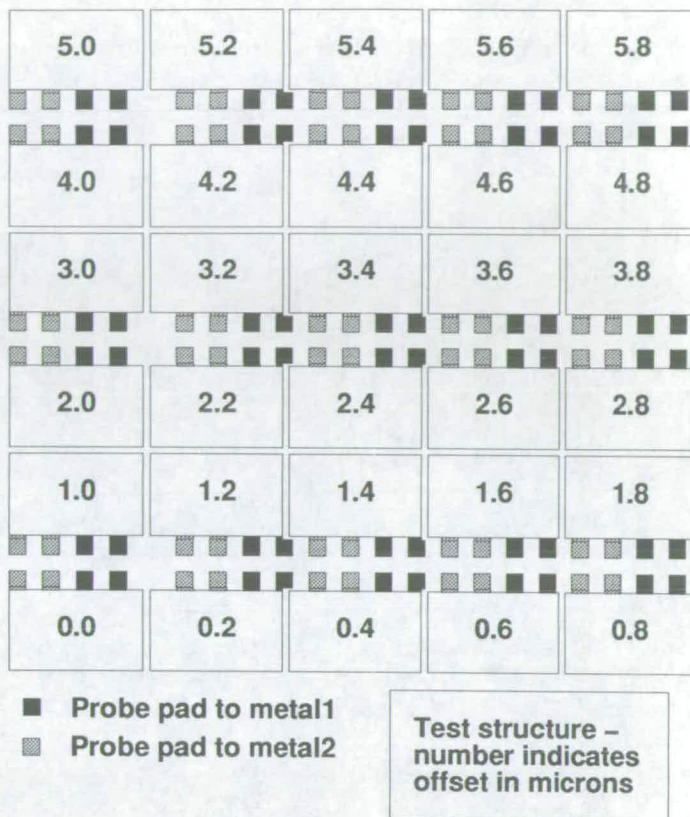
Figure 3. Layout of the whole set of test structures.

unintentional misalignment of the upper and lower combs which may have been introduced during processing, the entire range of offsets, from the teeth of the upper comb coinciding exactly with those of the lower comb to the teeth of the upper comb coinciding with the spaces between those of the lower comb, will be covered to within 0.1μm.

Figure 2 is a schematic diagram of a test structure with an offset of 1μm, whilst figure 3 shows the layout of the whole set of test structures. Figure 4 shows a cross section of three of the teeth for several degrees of offset.

4. Results

2D capacitance simulations have been used to extract the capacitance between the combs for each degree of offset for planarity ranging from 0% to 100%. These simulations were performed using TMA's Raphael software. Simulations were carried out for a small section of the structure which included 10 teeth from each metal layer. Due to the repetition of this section within the whole structure, the capacitance between the complete combs could be found by multiplying the results obtained for the smaller section by 10, thus greatly reducing the amount of time required to perform the simulations. In fact, to simulate the capacitance of this smaller section for a particular offset took around 2 minutes on a Sun IPX workstation. Data describing the structure being simulated was generated semi-automatically by using equations with variable parameters in the Raphael input file. The number of gridpoints used in each simulation was 15,000.
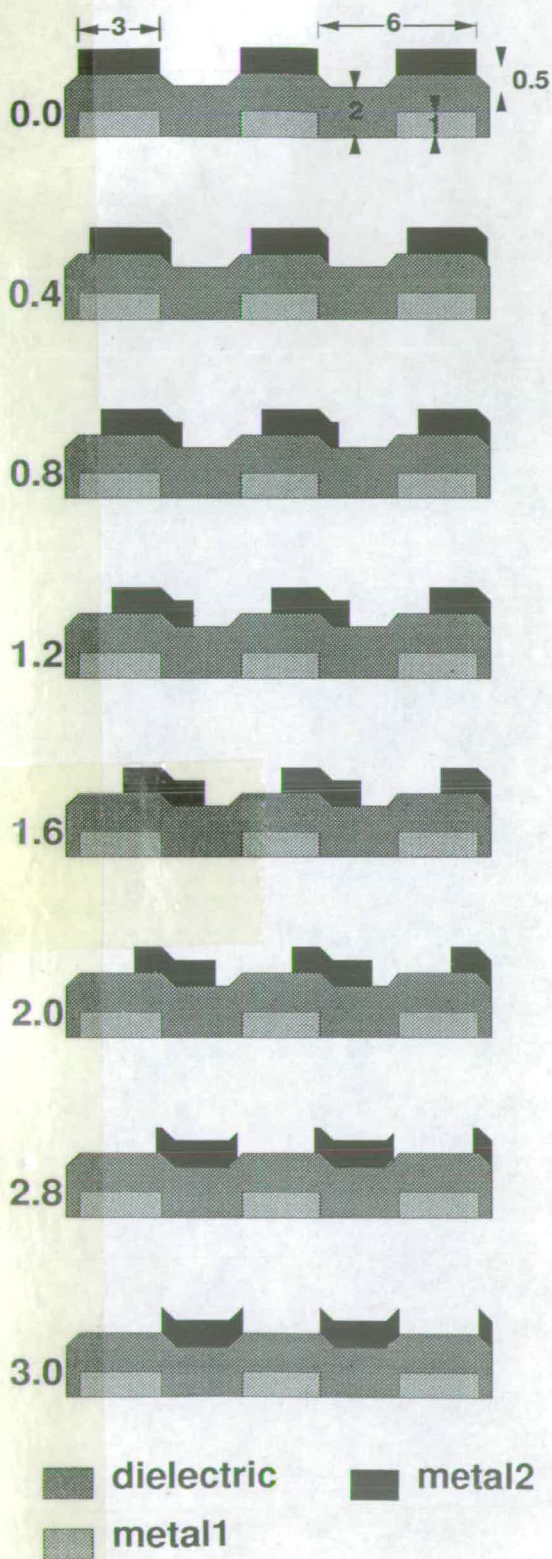
Figure 4. Cross sections of a small part of the test structure showing increasing offset of metal2, with oxide planarity of 50%. The number to the left of each figure is the amount of offset. All measurements are in microns.

The dielectric step coverage over the metal1 is assumed to be a constant slope as shown in figure 5. Sets of simulations were performed for step coverages with slopes of 27°, 45° and 56° (figure 5). Figure 6(a) shows capacitance between the combs vs the offset for a slope of 27° with figure 6(b) showing the variation for a 45° slope and figure 6(c) showing the results for a slope of 56°.
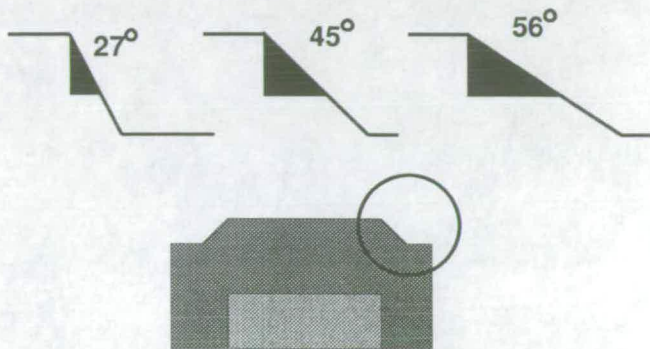
Figure 5. The three different step coverage slopes for which simulations were carried out.
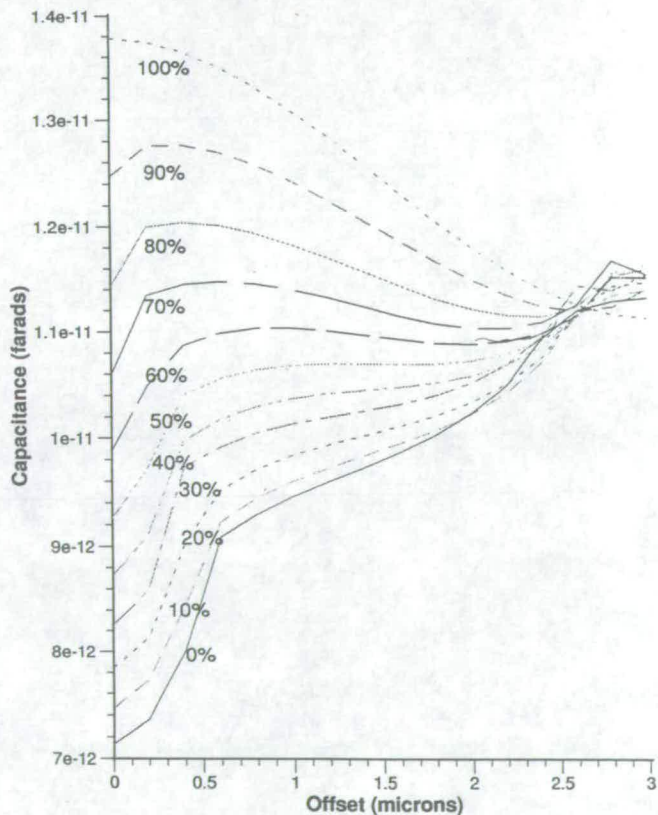
Figure 6(a). Capacitance as a function of offset for an oxide step of slope 27 degrees for planarities ranging from 0% to 100%.
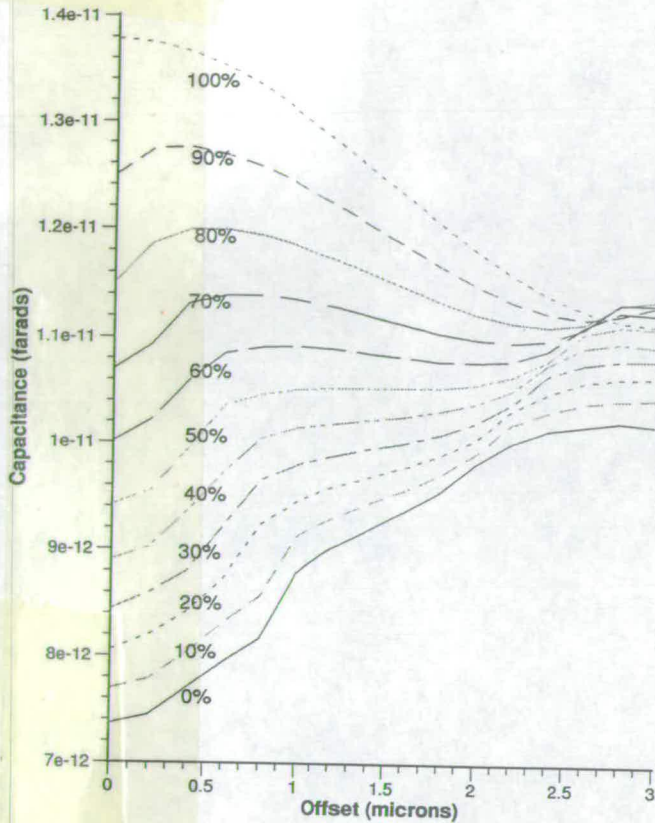
Figure 6(b). Capacitance as a function of offset for an oxide step of slope 45 degrees for planarities ranging from 0% to 100%.

Figure 6(c). Capacitance as a function of offset for an oxide step of slope 56 degrees for planarities ranging from 0% to 100%.

With increasing planarity, the oxide thickness directly above metal1 decreases as the raised oxide is polished away. This accounts for the change in capacitance for different degrees of planarisation with a zero offset and to a lesser degree for other offsets. However, the shape of the curves is dominated by the shape of the inter-metal dielectric, which is determined by the planarity. It can be seen from figures 6(a), (b) and (c) that with increasing planarity, the gradient of the central part of the curves decreases progressively from a positive to a negative slope. It can also be seen that the gradients of the curves for any given planarity are comparable for each of the oxide step angles.

To emphasise the fact that the shape of the slope depends far more on the planarity of the dielectric than on its thickness, curves have been plotted of capacitance vs offset for oxides of different thickness and with 50% planarity (figures 7 and 8). Although the oxide thicknesses differ, the shapes of the curves are very similar. This ensures that the test structure can be used to develop processes where the oxide thickness is not necessarily known.

Figure 7. Capacitance as a function of offset for 3 oxide thicknesses. The oxide is 50% planar in all 3 cases.

5. Conclusions

The test structure presented provides a means of testing electrically the degree of planarisation of inter-layer dielectric. It depends on the fact that the capacitance between two metal combs will vary as the horizontal offset between them changes, and that this variation will depend on the shape of the oxide separating them. The gradient of a graph of capacitance between the combs as a function of offset will indicate the degree of planarisation. The test structure is particularly suited to use with CMP.

metal1 **dielectric**
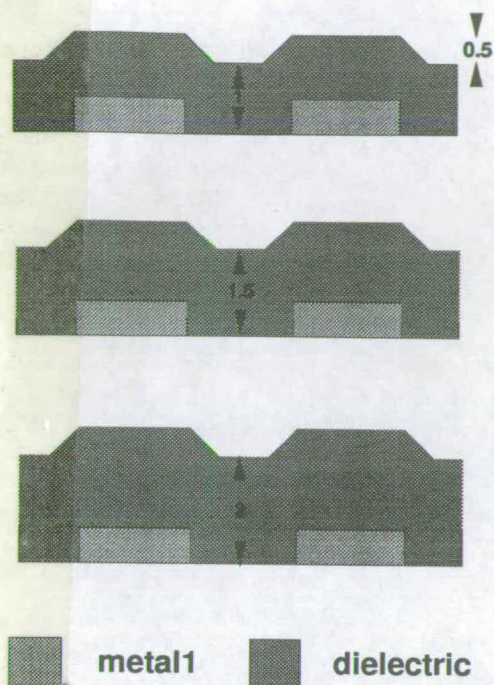
Figure 8. Oxide of 1, 1.5 and 2 micron thicknesses, 50% planar.

6. Acknowledgements

7. References

[1] Syd R. Wilson, Clarence J. Tracy and John L. Freeman, Jr., "Handbook of Multilevel Metallization for Integrated Circuits", Noyes Publications, 1993, pp 346-439

[2] Jane P. Elliott, Gerard A. Allan and Anthony J. Walton, "Automating the Calculation of 3D Interconnect Parasitics", Proc. of IEE Colloquium on "Advanced MOS and bi-polar devices", Feb 1995, pp 15/1 - 15/2

[3] G.J.Gaston and I.G.Daniels: "Efficient Extraction of Metal Parasitic Capacitances", Proc. of ICMTS, March 1995, pp 157-160

[4] Kimiko Aoyama, Kiyoshe Ise, Hisako Sato, Katsumi Tsuneno and Hiroo Masuda, "A New Characterization of Sub-micron Parallel Multilevel Interconnects and its Experimental Verification", Proc. of ICMTS, March 1995, pp 63-66.

Vizualization, extraction and simulation of smart pixel circuits in three dimensions

Jane P. Elliott, Mike W. G. Snook, Ian Underwood, Anthony J. Walton, David G. Vass†
The University of Edinburgh, Department of Electrical Engineering, (†Department of Physics,)
Edinburgh, EH9 3JL, UK, Tel. (+44) 131-650-5604, email jpe@ee.ed.ac.uk

Introduction

The effects of an increase in the parasitic capacitance on the performance of any electronic circuit are primarily two fold. Firstly, any such capacitances have to be charged and discharged leading to increased power dissipation. Secondly, any such capacitances between nodes lead to crosstalk and the possibility of noise (in the analog case) or bit errors (in the digital case). For VLSI circuits modern technology uitilises multiple metal interconnect layers (increasing the number of parasitic capaciors in a circuit) and operates at ever higher frequencies (increasing the value of each of the capacitors present). Thus there exists a requirement for precise capacitance extraction in order to allow the accurate modelling of circuit performance. This is particulary true for silicon based smart pixel technology.

As silicon based smart pixel technology has advanced, the three dimensional (3-D) topographic nature and complexity of the interconnect requirement has increased to the point where the technology has outstripped the capabilities of the conventional circuit extraction software. This is particularly true in at least two applications in which the authors are currently working. The first occurs where custom layers are added to a silicon wafer, as in the planarization of FLC/CMOS SLMs [1], or where different semiconductor technologies are combined, as in flip chip bonding of SEED/CMOS SLMs [2]. In each case the additional custom layers are not handled by the circuit extractor and yet can have a significant effect on circuit performance. The second occurs where "vulnerable" signals are present on nodes within a smart pixel circuit, and in particular where those nodes extend over several of the interconnect layers thus being exposed to parasitic capacitive coupling on several levels. Two extreme examples are (i) capacitive storage nodes at the output of a FLC/CMOS smart pixel [1]which, by definition extend from the bottom (active area) layer to the top (metal mirror) layer of the pixel circuit and (ii) nodes at the input of SEED/CMOS smart pixels [2] which have to conduct small, high frequency analogue signals through the layers of interconnect to the underlying high sensitivity amplifier circuit.

In this paper we briefly describe a custom software package which allows (a) the vizualization of microelectronic and micro-mechanical structures in 3-D, and (b) the accurate extraction of capacitances .We explore its initial application to a smart pixel circuit of type (i) as described in the previous paragraph.

3-D capacitance extraction

It is important in general to obtain as good an estimate as possible of the interconnect capacitances in a smart pixel. In order to achieve this, a 3-D capacitance simulator can be used, [eg, 3]. However, such software requires as input a description of the area of circuitry under consideration in a 3-D format. Furthermore, in order to achieve results which are realistic, the 3-D circuit description must be realistic. Specifically, for the process used in producing our pixel, the description of each layer should take account of the topography of underlying layers. Such a description can be acheived using software developed in-house at Edinburgh University - 3DTOP [4]. The software is designed for compatibility with a suite of industry standard device and circuit simulation software [5]. Figure 1 shows the 3D description of the circuitry up to and including layer metal 2. The circuitry is displayed without the inclusion of dielectrics for the sake of clarity. Any dielectrics used after this stage are planarised, so the effect of preceding layers on the topography of layers metal3 [M3] and metal4 [M4] is minimal - M3 and M4 are effectively flat.

Application Example

The example we use here is that of a single transistor pixel for a ferroelectric liquid crystal over silicon SLM. We choose this example because of the relatively simple nature of the circuit (if not its 3-D implementation). The circuit is shown in fig 2.

The final FLC/CMOS device has 4 metal layers. Metals 1 and 2 are used primarily for east-west and north-south bus lines respectively in the array; M4 is used for the top-level optically-flat mirror while M3 is a ground plane which complements M4 with a slight overlap in order to minimise the amount of light reaching the silicon substrate. M3 and M4 are applied in a custom post-processing technique. Conventional circuit extraction of parasitic capacitances is not available for M3 and M4 and is not sufficiently accurate for M1 and M2.

With regard to figure 2, several of the parasitic capacitances are key to the performance of the pixel and overall device. The role of Csub is well

known [1,6] as is the requirement to ensure that it stores sufficient charge in relation to the Ps of the FLC. C1 robs the mirror,M, of some of its charge as a falling edge on the row line pulls down the mirror potential at the same time as it isolates the mirror. C2 causes noise on the mirror node as the data bus line switches. C3 is a significant factor in determining the overall power dissipation of the device [7]. A typical design goal would be to maximise Csub while minimising C1 and C2.

Name	Conv'l	3D-TOP	Diff
	fF	fF	%
ΔCsub	4.85	5.61	16
C1	2.86	2.89	1
C2	0.70	1.29	84
C3	1.36	1.68	22

Table 1. Comparison of extracted parasitics for Conventional and 3-D TOP methods.

At the conference we will present further results of the capacitance extraction and simulations detailing the effect on circuit performance.
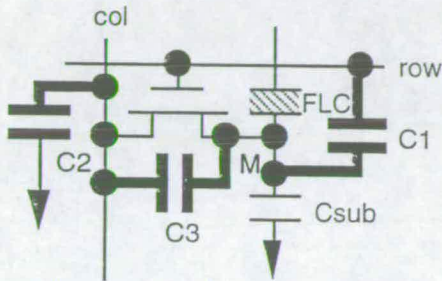
Figure 2. Pixel circuit schematic (parasitic capacitances in bold)

We carried out an analysis of a current single transistor pixel layout. We extracted the parasitic capacitances using the capacitance extraction routine available within our VLSI design suite and using 3D-TOP. The result, see Table 1, was that, in all cases 3D-TOP produced higher values of capacitance than the conventional extraction Results varied from 1% higher for essentially planar structures to 80% higher for complex topographic structures.

Conclusions
Table 1 shows that, by considering planar capacitances only, conventional extraction consistently underestimates parasitics. 3D-TOP takes full account of the 3-D nature of the circuit and is thus particularly suitable for use in smart pixel design for hybrid (SEED/CMOS and FLC/CMOS) technologies.

References
[1] Johnson et al, JQE Vol29, pp699-714.
[2] Goodwill et al, Smart Pixels '94 (invited)
[3] "Raphael User's Manual", Technology Modelling Associates Inc.
[4] Elliott et al, IEE Collq.,Feb 1995, pp 15/1-2.
[5] "Studio User's Manual" TMA Inc.
[6] Collings et al, Appl Opt Vol28, pp4740-7.
[7] McKnight et al, Appl Opt, Vol33, pp2775-84.
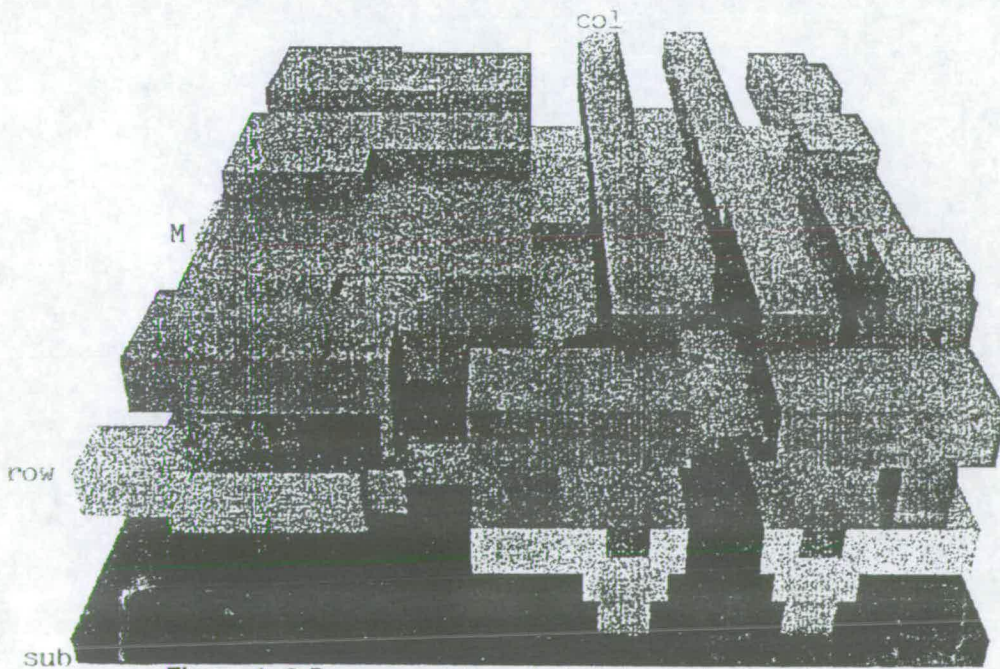
Figure 1. 3-D representation of pixel circuit obtained from 3D-TOP

THE AUTOMATIC GENERATION OF CONFORMAL 3D DATA FOR SIMULATION OF IC INTERCONNECT PARASITICS AND REPRESENTATION OF MEM STRUCTURES

Jane P.Elliott, Anthony J. Walton and Gerard A. Allan

Department of Electrical Engineering, University of Edinburgh, Mayfield Road,

Edinburgh, EH9 3JL, Scotland, UK

Abstract

A software tool which automatically generates planar, conformal and semi-conformal 3D representations of an IC direct from the 2D layout is reported. The basic concepts behind the algorithm used by the tool are described, and the creation of a semi-conformal description of a simple circuit illustrated. Results are presented that demonstrate the importance of using 3D capacitance extraction to accurately simulate circuit performance. The degree of success with which the 3DTOP software represents actual IC topography is illustrated. The application of the software tool in representation of MEMS is described.

1. Introduction

As IC feature sizes reduce and the use of multilayer metal increases, ever more dense and fast ICs are being manufactured. As a result, the effect of interconnect upon the overall circuit performance is becoming more important and must be considered during the design phase. Many software packages and algorithms are available for simulation of interconnect resistance and capacitance[1,2,3,4,5]. For present day technology, 3D simulation of circuit parasitics is essential. However the input to the software packages and algorithms available varies widely. For some it must be entered manually, others can take the input via CAD drawing packages, while some require the data to be in the form of descriptive text files. All of these are extremely time consuming and error prone processes and are not feasible for routine use except with the smallest elements of circuits.

2. 3DTOP

3DTOP is a software tool which automatically generates planar, conformal and the more realistic semi-conformal 3D representations of an IC direct from the mask layout. Both the planar and conformal data can be used as input to Raphael[2], a parasitic simulator based on the finite-element technique, whilst planar, conformal and semi-conformal data can be used as input to Fastcap[1], a simulator using the boundary-element technique. Figure 1 illustrates the difference between planar and conformal representations of an inverter, along with the layout from which the 3D data was created.

The 3DTOP software employs an algorithm which uses a set of basic polygon operations and Boolean operators[6]. A fundamental concept in this algorithm is the idea of a top surface, which is a topographical

description of the uppermost surface. This surface is used to determine the topography of each 3D layer as it is created. Figure 2 shows creation of a semi-conformal representation of a simple circuit. The top surface used to create each 3D conducting layer is shown.

(a)

(b)

(c)
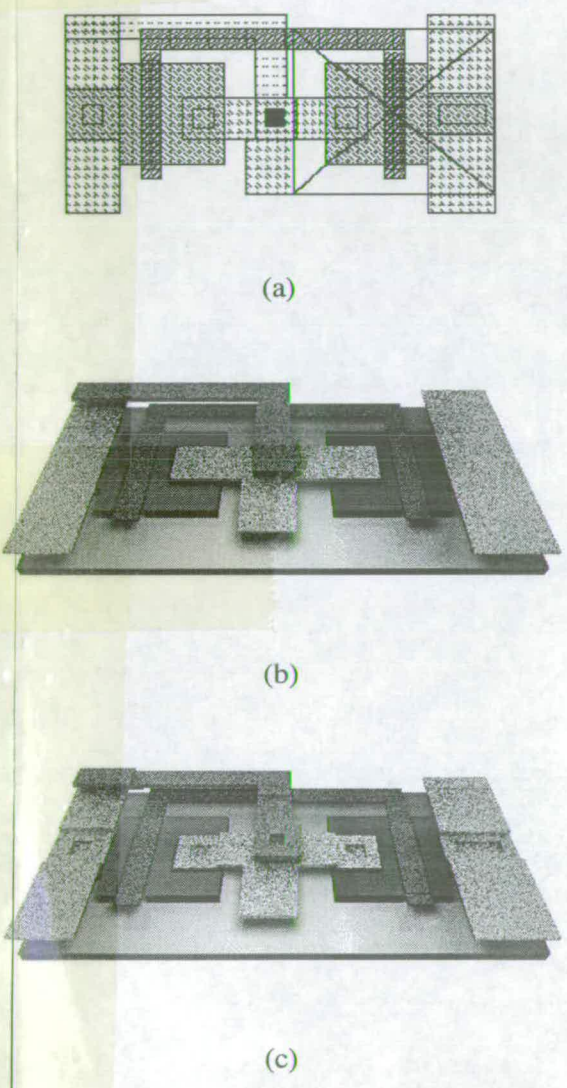
Figure 1. (a)Inverter layout (b)Planar 3D
inverter (c)Conformal 3D inverter

final top surface

metal2

top surface 3

metal1

top surface 2

poly

top surface 1
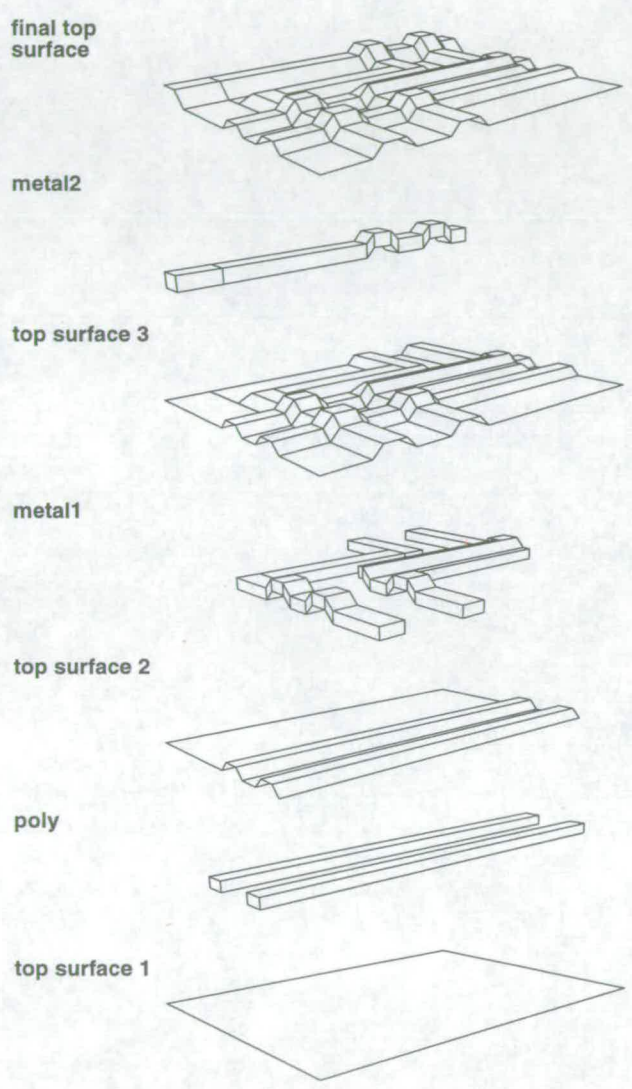
Figure 2. Creation of semi-conformal
representation of simple circuit

3. Parasitic Extraction

Simulations using 3D Data structures generated using 3DTOP were performed to determine the effect that the degree of conformality of the 3D data has on simulated capacitances and hence circuit performance.

Previous work has shown that the difference in capacitances simulated using conformal 3D data from those simulated using planar 3D data for even very simple structures can be as much as 30%, and increases with the complexity of the circuit[6]. The effect of these differences in simulated capacitance on circuit performance is illustrated by examining the delay through a string of 4 inverters. This delay was found with no interconnect

capacitances, and with those simulated using planar and conformal data. The results of the simulation are shown in Figure 3.
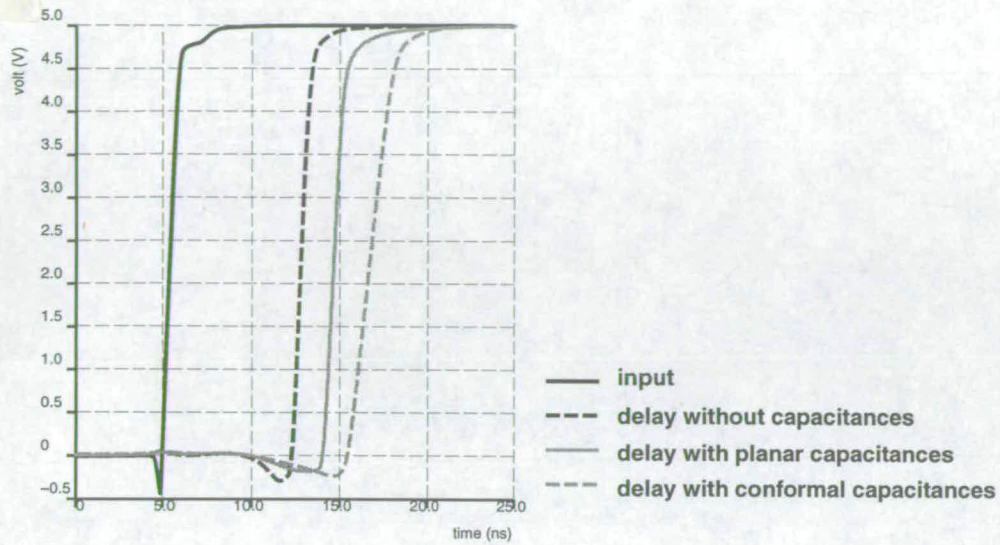
Figure 3. Delay through inverter string for inverters with no inter-connect capacitances, planar and conformal interconnect capacitances.

4. Success of Representation

The degree of success with which data generated using 3DTOP represents actual IC topography can be seen in Figure 4. Figure 4a shows an SEM photograph of part of an IC with the passivation removed[7], whilst Figure 4b shows a representation of the same area of circuitry generated by 3DTOP. The 3DTOP-generated data is displayed without dielectrics for clarity.
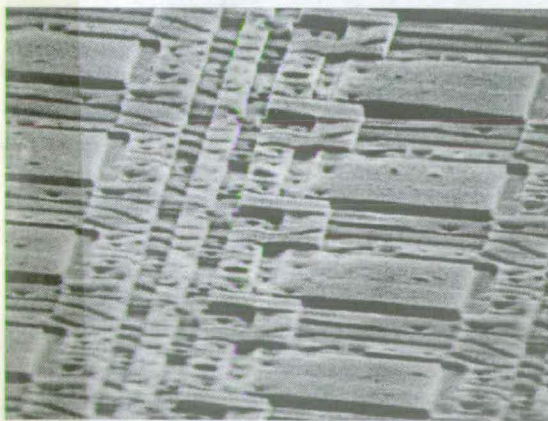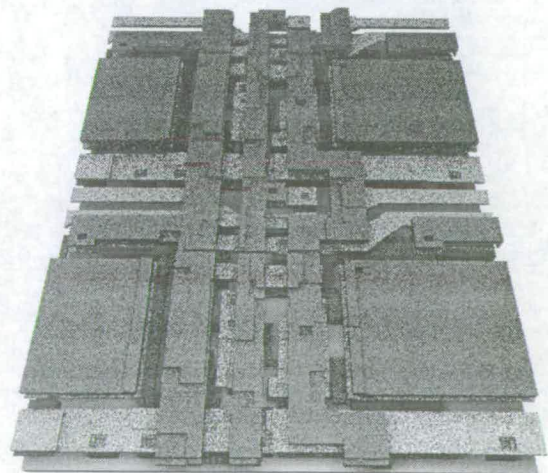
(a)   (b)

Figure 4 (a)SEM and (b)3DTOP depictions of part of an IC

5. Representation of MEMS

A further application of 3DTOP is the representation of microelectromechanical structures (MEMS). Since

3DTOP creates 3D data directly from the IC layout, representations of MEMS structures that are manufactured using the same fabrication process can be generated.
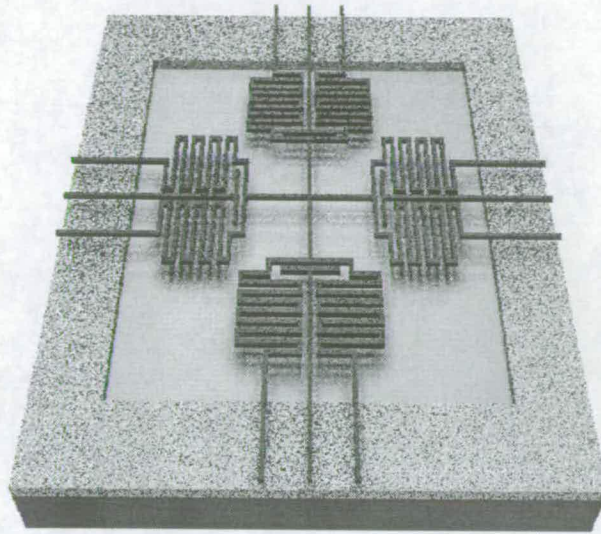
Figure 5 Representation of a simple MEM structure created using 3DTOP

5. Conclusions

Software has been described which automatically generates a planar, conformal or semi-conformal 3D description of an IC. It has been demonstrated that interconnect capacitances simulated using 3D conformal data have a significantly different effect on circuit performance than capacitances simulated using 3D planar data. 3D conformal data more accurately represents circuit topography than 3D planar data. Where accurate circuit simulation is important it is essential to use the capacitance data that is extracted from the more realistic conformal representation of the circuit.

References

[1] K.Nabors, S.Kim, J.White and S.Senturia: "FastCap User's Guide", 1992

[2] Technology Modelling Associates, Inc.: "Raphael User's Manual"

[3] R.H.Uebbing and M.Fukama: "Process-based three-dimensional capacitance simulation - triceps", IEEE Trans. on CAD, Vol 5, No 1 Jan 1986, PP 215-220

[4] A.H.Zemanian, R.P.Tewarson, Chi Ping Ju and Juif Frank Jan: "Three-dimensional capacitance computations for VLSI/ULSI interconnections",IEEE Trans on CAD, Vol 8, No 12 Dec 1989, PP 1319-1325

[5] S.Kumashiro, R.A.Rohrer and A.J.Strojwas: "Asymptotic waveform evaluation for transient analysis of 3-d interconnect structures",IEEE Trans. on CAD, Vol 12, No 7 July 1993, PP 988-996

[6] J.P.Elliott,G.A.Allan and A.J.Walton: "Automating the Calculation of 3D Interconnect Parasitics", IEE Colloquium on Advanced MOS and bi-polar devices, No 1995/033, February 1995.

[7] D.C.Burns: "Design and characterisation of a ferroelectric liquid crystal over silicon spatial light modulator", PhD Thesis, University of Edinburgh, 1994

THE AUTOMATIC GENERATION OF CONFORMAL 3D DATA FOR INTERCONNECT CAPACITANCE SIMULATION

Jane P. Elliott, Gerard A. Allan, Anthony J. Walton
Dept Electrical Engineering
University of Edinburgh
Edinburgh EH9 3JL
UK
+44 131 650 5602

EXECUTIVE SUMMARY

Software (3DTOP) is presented which can automatically create conformal 3D data directly from 2D mask data (GDSII file), and from simple process information such as layer thicknesses. It is shown that the difference between parasitic circuit capacitance values calculated using conformal and planar 3D data can be significant.

EXTENDED ABSTRACT

With reduction in IC feature sizes and the increased use of multilayer metal, ever more dense and fast ICs are being manufactured. As a result, the effect of interconnect upon overall circuit performance is becoming more important and must be considered during the design phase. Many software packages and algorithms are available for simulation of interconnect parasitics in 3D [1,2,3,4,5]. However the input to the software packages and algorithms available varies widely. For some it must be entered manually, others can take the input via CAD drawing packages, while some require the data to be in the form of descriptive text files. All of these are extremely time consuming and error prone processes, and are not feasible for routine use except with the smallest elements of circuits. Consequently a means of automatically producing representative 3D data from the circuit layout is becoming essential.

Conformal vs Planar

Current solutions assume perfect planarisation for each layer, a situation which is fairly unrealistic. In order to investigate the difference which exists between parasitic capacitances simulated using planar and conformal 3D circuit representations, a series of simple circuits of low but increasing complexity were considered. The 2D mask information was converted to planar 3D data using LORENZO [6], and to conformal 3D data using 3DTOP. Both sets of data were then used as input to RAPHAEL [2] to calculate the capacitance matrix.

The four circuits used are shown in figure 1. Circuit(a) consists of 2 parallel metal tracks, and was used to ensure that data created by LORENZO and 3DTOP was comparable. For circuit(b) the complexity was increased slightly by raising one of the metal tracks with relation to the other by placing a block of polysilicon underneath it. Circuit(c) has increased complexity, and finally the inclusion of a second polysilicon track and a third layer, metal2, in circuit(d) completes the set of test circuits. Figure 2 illustrates the difference between planar and conformal representations of

circuit(d). The complexity of the test circuits can be simply ordered as in figure 1. The calculated capacitance for the planar and conformal representations of each circuit have been compared and the percentage differences are shown in table 1. It can be observed that for these examples the difference increases with the complexity.
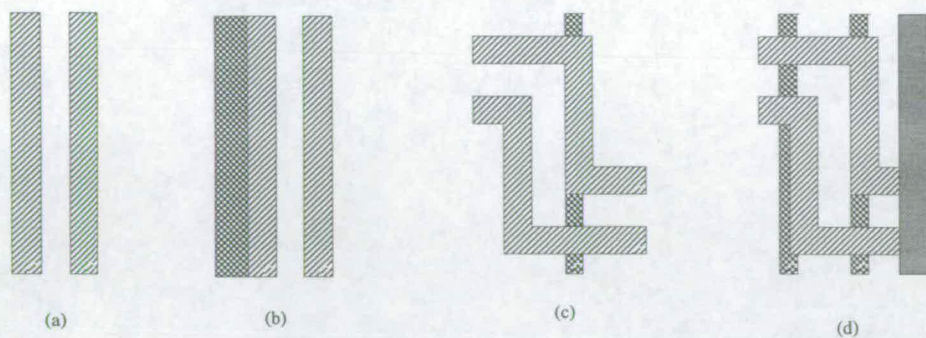

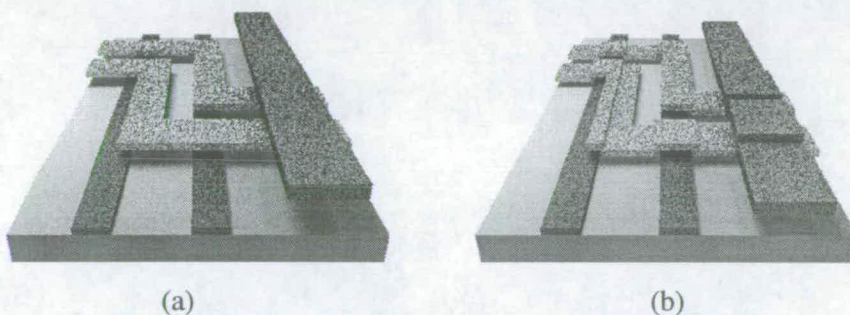(a)   (b)   (c)   (d)

Figure 1. Four simple test circuits.

(a)   (b)

Figure 2. Planar and conformal views of test circuit 4

test circuit	a	b	c	d
% increase in capacitance	0	1.6	11.3	29.6

Table 1. Percentage increase in parasitic capacitances in conformal data compared to planar data

The 3DTOP software

The 3DTOP software requires two files as input data. The first is a description of the 2D layout. The second consists of a control file containing instructions about which layers are to be electrically connected and any voltages associated with labelled nodes in the layout. It also contains parameters relating to layer and dielectric thickness, step coverage and electrical properties.

Example

The following example considers the delay through a string of four CMOS inverters. This delay is determined by several factors, including the interconnect capacitances which exist between electrical nodes within the circuit. In order to investigate this delay, a SPICE netlist was produced describing a string of four identical inverters. Interconnect capacitances were determined for both planar and conformal descriptions of the inverter using data generated using 3DTOP as an input to RAPHAEL. HSPICE simulations were performed on the inverter string for three cases: zero interconnect capacitance, interconnect capacitances simulated using planar data, and interconnect capacitances simulated using conformal data. Table 2 details the results.

| capacitance	none	planar	conformal
delay(ns)	6.5	9.0	11.5

Table 2. Delay through inverter string for no capacitance, planar 3D and conformal 3D capacitance.

Success and Limitations

The 3D data generated by 3DTOP gives a good representation of the actual topography of an integrated circuit. As an example, an array of Spatial Light Modulator (SLM) pixels is used[7]. Figure 3a shows a Scanning Electron Microscope (SEM) photograph of a section of the array, whilst figure 3b shows the corresponding data generated by the 3DTOP software. The data generated using 3DTOP is displayed without dielectrics.

Conclusions

A comparison of planar and conformal 3D circuit descriptions has shown that as circuit complexity increases, so too does the percentage increase in interconnect capacitance found using conformal data compared with that obtained using planar data. Software has been described which automatically generates a conformal 3D representation of an IC. An example of how the conformal 3D data might be used has been described, showing that parasitic interconnect capacitances can have an appreciable effect on circuit operation.
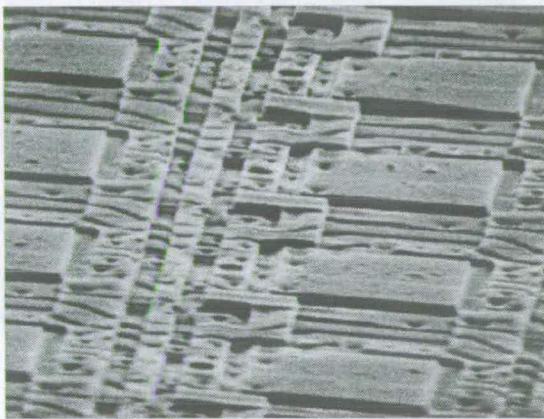
(a)
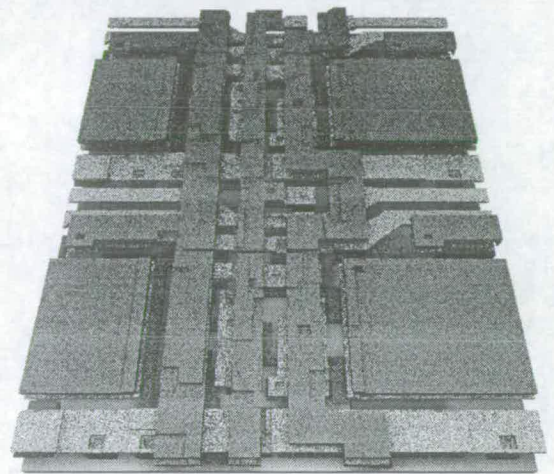
(b)

Figure 3. SEM and 3DTOP depictions of an array of SLM pixels

References

[1] K.Nabors, S.Kim, J.White and S.Senturia: "FastCap User's Guide", 1992

[2] Technology Modelling Associates, Inc.: "Raphael User's Manual"

[3] R.H.Uebbing and M.Fukama: "Process-based three-dimensional capacitance simulation - triceps", IEEE Trans. on CAD, Vol 5, No 1, Jan 1986, pp 215-220

[4] A.H.Zemanian, R.P.Tewarson, Chi Ping Ju and Juif Frank Jan: "Three-dimensional capacitance computations for VLSI/ULSI interconnections", IEEE Trans on CAD, Vol 8, No 12, Dec 1989, pp 1319-1325

[5] S.Kumashiro, R.A.Rohrer and A.J.Strojwas: "Asymptotic waveform evaluation for transient analysis of 3-D interconnect structures", IEEE Trans. on CAD, Vol 12, No 7, July 1993, pp 988-996

[6] Technology Modelling Associates, Inc.: "Lorenzo User's Manual"

[7] D.C.Burns: "Design and characterisation of a ferroelectric liquid crystal over silicon spatial light modulator", PhD Thesis, University of Edinburgh, 1994

AUTOMATING THE CALCULATION OF 3D INTERCONNECT PARASITICS

Jane P. Elliott, Gerard A. Allan and Anthony J. Walton [1]

Introduction

As IC feature sizes reduce and the use of multilayer metal increases, ever more dense and fast ICs are being manufactured. As a result, the effect of interconnect upon overall circuit performance is becoming more important and must be considered during the design phase. Many software packages and algorithms are available for simulation of interconnect resistance and capacitance [1,2,3,4,5]. For present day technology, 3D simulation of circuit parasitics is essential. However the input to the software packages and algorithms available varies widely. For some it must be entered manually, others can take the input via CAD drawing packages, while some require the data to be in the form of descriptive text files. All of these are extremely time consuming and error prone processes, and are not feasible for routine use except with the smallest elements of circuits.

A means of automatically producing representative 3D data from the circuit layout is essential. Current solutions assume perfect planarisation for each layer, a situation which is fairly unrealistic. This paper describes software which automatically creates 3D data from 2D mask information (by way of a GDSII file), and from simple process information (layer and dielectric thickness and step-coverage parameters). The algorithm employed takes into account the topography of any underlying layers. The parasitic capacitances of conformal and planar descriptions of some simple circuits are compared, and a description of the algorithm is followed by an example of how the software might be used in a design environment. Finally, the success of the software in truly representing the 3D nature of an IC is examined.

Conformal vs Planar

Before further consideration of the generation of conformal 3D data, it is appropriate to examine how significant the difference is between a planar and conformal representation. It is obvious that for a circuit of any real complexity, the capacitance between various conducting tracks will be different in the conformal and planar cases. Furthermore since the conformal case can be said to be a closer representation of the true topography of an IC, the capacitances resulting from a 3D simulation using the conformal data should more closely represent the true circuit parasitic capacitances.

In order to investigate the difference which exists between parasitic capacitances simulated using planar and conformal 3D circuit representations, a series of simple circuits of low but increasing complexity were considered. The 2D mask information was converted to planar 3D data using TMA's LORENZO software [6], and to conformal 3D data using the 3DTOP software. Both sets of data were then used as input to TMA's RAPHAEL software [2] to calculate the capacitance matrix.

The 4 circuits used are shown in figure 1. Circuit a (fig 1a) consists of 2 parallel metal tracks, and was used to ensure that data created by LORENZO and 3DTOP was comparable, since the results found using this circuit should be identical. For circuit b (fig 1b) the complexity was increased slightly by raising one of the metal tracks with relation to the other by placing a block of polysilicon underneath it. Circuit c (fig 1c), although still consisting only of 2 metal tracks and 1 polysilicon track, has increased complexity due to its layout, and finally

---

[1]Dept. of Electrical of Engineering
University of Edinburgh, Mayfield Road, Edinburgh. EH9 3JL

the inclusion of a second polysilicon track and a third layer, metal2, in circuit d (fig 1d) completes the set of test circuits. Figure 2 illustrates the difference between planar (fig 2a) and conformal (fig 2b) representations of circuit d.

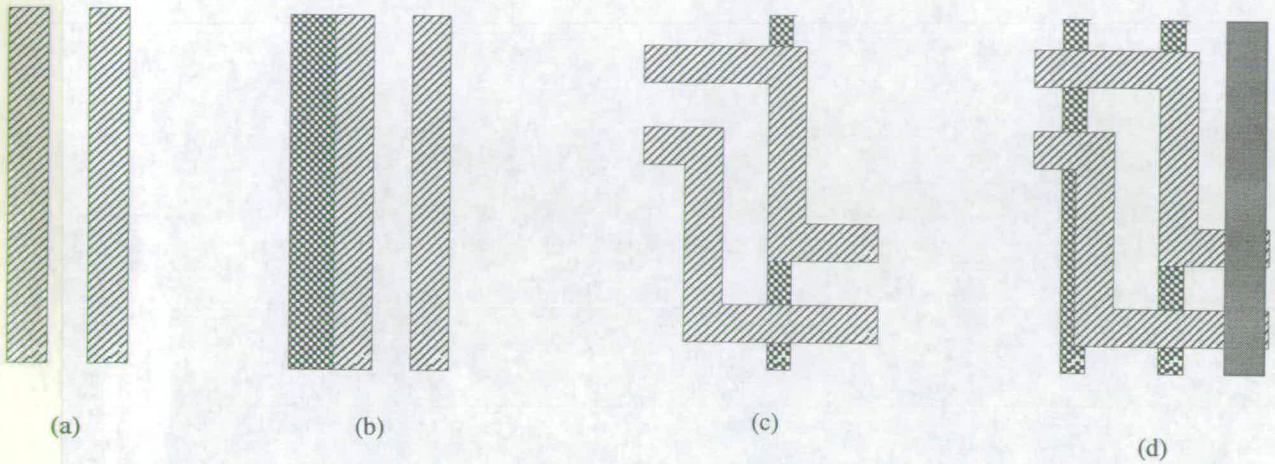(a)   (b)   (c)   (d)
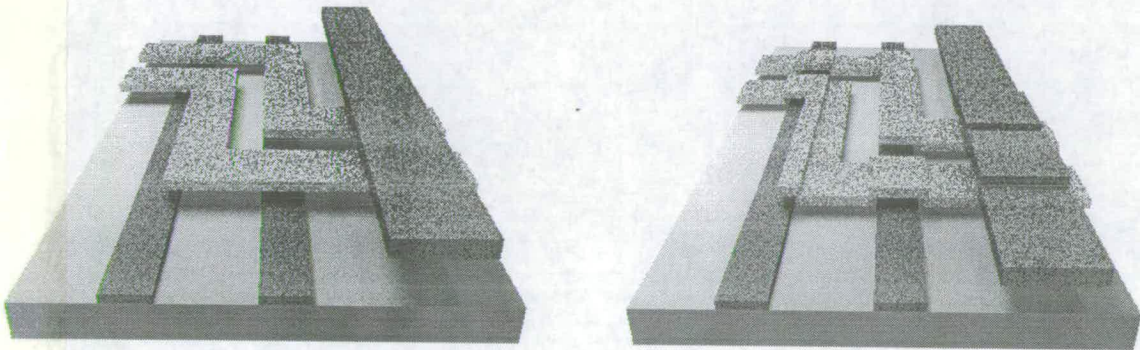
Figure 1. Four simple test circuits.

Figure 2. Planar and conformal views of test circuit 4

The complexity of the test circuits can be simply ordered as in figure 1. The calculated capacitance for the planar and conformal representations of each circuit have been compared. The percentage differences are shown in table 1, and it can be observed that for these examples the difference increases with the complexity. It can also be observed that the capacitance is always greater in the conformal case.

test circuit	a	b	c	d
percentage increase	0	1.6	11.3	29.6

Table 1. Percentage increase in parasitic capacitances in conformal data compared to planar data

The 3DTOP software

The 3DTOP software requires 2 files in order to run. The first is a description of the 2D layout in the form of boxes and polygons. The second consists of a control file containing instructions about which layers are to be electrically connected, any voltages associated with labelled nodes in the layout, and parameters relating to layer and dielectric thickness, step coverage and electrical properties. The 2D description is obtained by converting the GDSII file to CIF format, and then using CIF to boxes conversion software.

The software first loads in the specified layers from the data file and then creates electrical nodes, taking into account the electrical connectivity of the layers. The 2D to 3D conversion algorithm then uses a set of polygon operations, i.e. BLOAT, which increases the dimensions of a polygon by a given amount, and the Boolean

operators AND, ANDNOT and OR. A fundamental concept in this algorithm is the idea of the top surface, which is a topographical description of the uppermost surface of the circuit. This surface is stored as a list of planes and is used to determine the topography of each 3D layer as it is created. The top surface is updated after the creation of each 3D layer. The algorithm is described below.

```
CREATE BASE LAYER AND INSERT INTO TOPSURFACE
FOR EACH LAYER TO BE CREATED {
    /* PLANELIST AND STEPLIST TOGETHER DESCRIBE 3D LAYER */
    FOR  EACH TOPPLANE IN TOPSURFACE {
        IF    (CURRENTLAYER AND TOPPLANE) IS TRUE
            INSERT RESULTING PLANE IN PLANELIST
    }
    FOR EACH PLANE IN PLANELIST {
        BLOATEDPLANE = CURRENTPLANE BLOATED BY GIVEN PARAMETER
        FOR EACH STEP IN STEPLIST {
            IF (BLOATEDPLANE AND CURRENTSTEP) IS TRUE
                INSERT RESULTING STEP IN STEPLIST
        }
        FOR EACH PLANE IN STOREDLIST { */ CONTAINS PLANES OF THIS LAYER ALREADY CREATED */
            IF (BLOATEDPLANE AND STOREDPLANE) IS TRUE
                INSERT RESULTING STEP IN STEPLIST
        }
        INSERT CURRENTPLANE IN STOREDLIST
    }
    */ UPDATE TOPSURFACE /*
    RENAME TOPSURFACE AS OLDTOPSURFACE
    FOR EACH OLDTOPPLANE IN OLDTOPSURFACE {
        IF (OLDTOPPLANE AND CURRENTLAYER) IS FALSE
            INSERT OLDTOPPLANE IN TOPSURFACE
    }
    IF STEPLIST IS EMPTY
        INSERT ALL CONTENTS OF PLANELIST IN TOPSURFACE
    ELSE {
        FOR EACH PLANE IN PLANELIST {
            FOR EACH STEP IN STEPLIST {
                IF UPPER LEVEL OF STEP = UPPER LEVEL OF PLANE
                    INSERT STEP IN SAMETOPLIST
                ELSE IF UPPER LEVEL OF STEP > UPPER LEVEL OF PLANE
                    INSERT STEP IN GREATERTOPLIST
            }
            NEWTOPPLANE = SAMETOPLIST ANDNOT GREATERTOPLIST
            INSERT NEWTOPPLANE IN TOPSURFACE
        }
    }
}
```

Example

The example considers the delay through a string of 4 CMOS inverters. This delay is determined by several factors, including the interconnect capacitances which exist between electrical nodes within the circuit. In order to investigate this delay, a SPICE netlist was produced describing a string of 4 identical inverters. If it is assumed that the layout of this string of inverters is such that each inverter has an identical layout, and that parasitic

capacitances between the individual inverters are negligible, parasitic interconnect capacitances need only be determined for one inverter, and these values included in the inverter SPICE subcircuit. The planar and 3D representations of the inverter circuit are shown in figure 3.
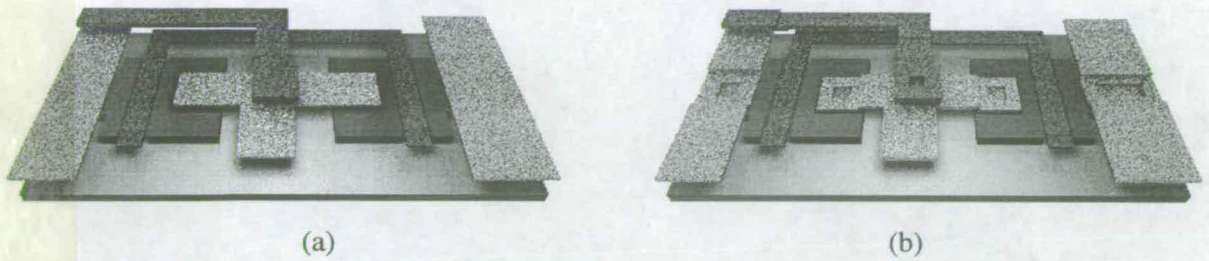

(a)   (b)

Figure 3. (a) Planar and (b) conformal representations of inverter with dielectrics removed for clarity

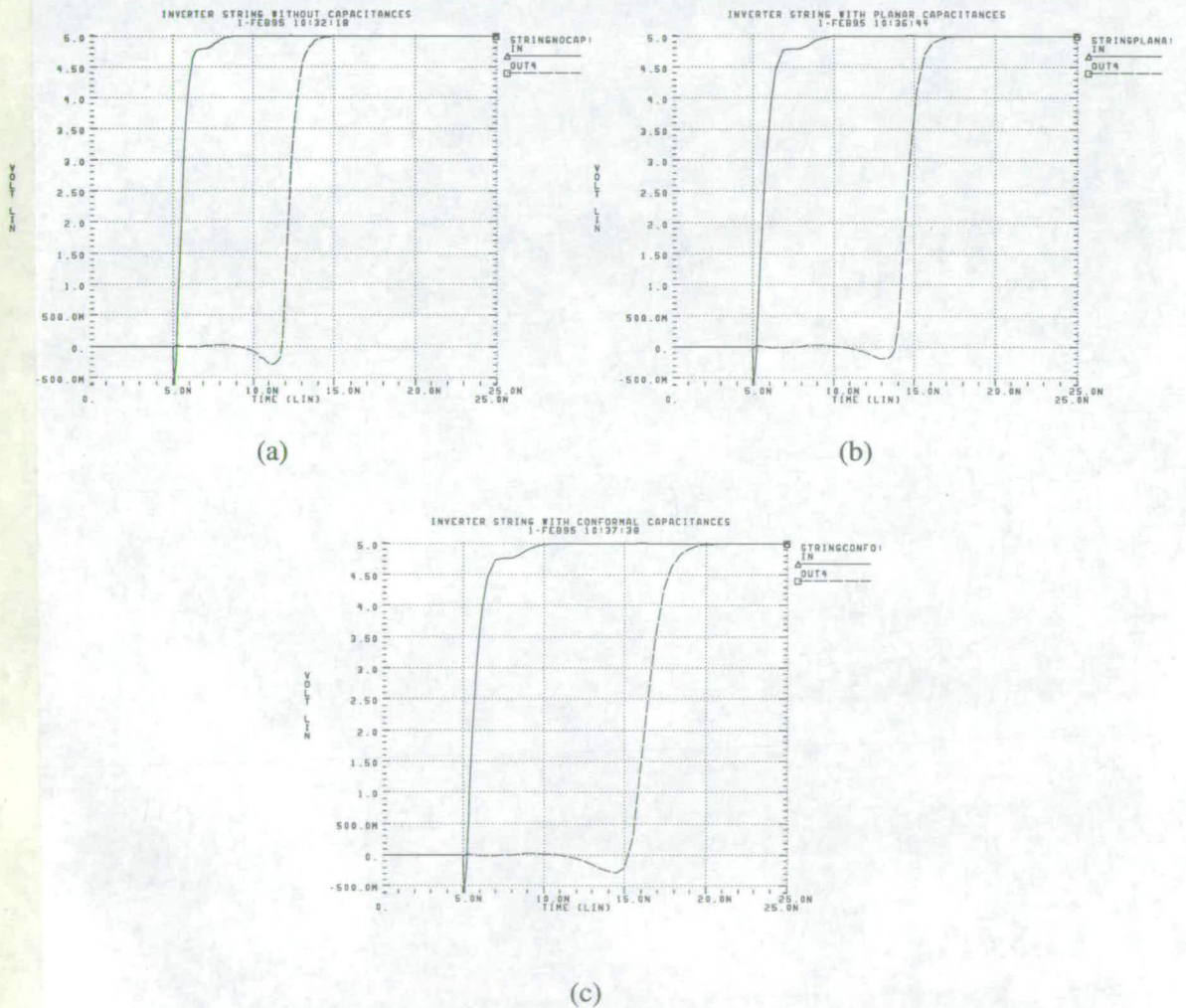(a)   (b)

(c)

Figure 4. Input and output of inverter string: (a) no capacitances, (b) planar capacitances, (c) conformal capacitances

Interconnect capacitances were determined for both planar and conformal descriptions of the inverter, using data generated using 3DTOP as an input to RAPHAEL. HSPICE simulations were performed on the inverter string for three cases: zero interconnect capacitance, interconnect capacitances simulated using planar data, and interconnect capacitances simulated using conformal data. Plots for these 3 cases showing the input to the

inverter string (solid line) and the output (dashed line) are shown in figure 4.

It can be seen from figure 4 that the delay through the inverter chain is increased by the inclusion of interconnect capacitances, and that this increase is greater for the capacitances resulting from simulation using the conformal data than for those resulting from simulation using planar data.

This example demonstrates the effect of interconnect capacitances on circuit performance. The production of representative 3D data for input to a capacitance simulator is straightforward using 3DTOP software. This makes it feasible for a designer to easily investigate the effect of layout changes on circuit performance, as a new set of 3D data can be readily obtained from any GDSII file. It is also possible to predict the performance of a circuit when fabricated using different processes, as the process information can easily be altered in the 3DTOP control file.

Success and Limitations

The 3D data generated by 3DTOP gives a good representation of the actual topography of an integrated circuit. As an example, an array of Spatial Light Modulator (SLM) pixels is used[7]. Figure 5a shows a Scanning Electron Microscope (SEM) photograph of a section of the array, whilst figure 5b shows the corresponding data generated by the 3DTOP software. Even a simple comparison (figure 5) shows many topographical similarities. There are differences however, the major one being the fact that the 3DTOP data consists of flat planes and sharp corners, whereas the actual circuit topography is more rounded and smooth. The data generated using 3DTOP is displayed without dielectrics, which explains some discrepancies in its appearance compared to the SEM photograph.
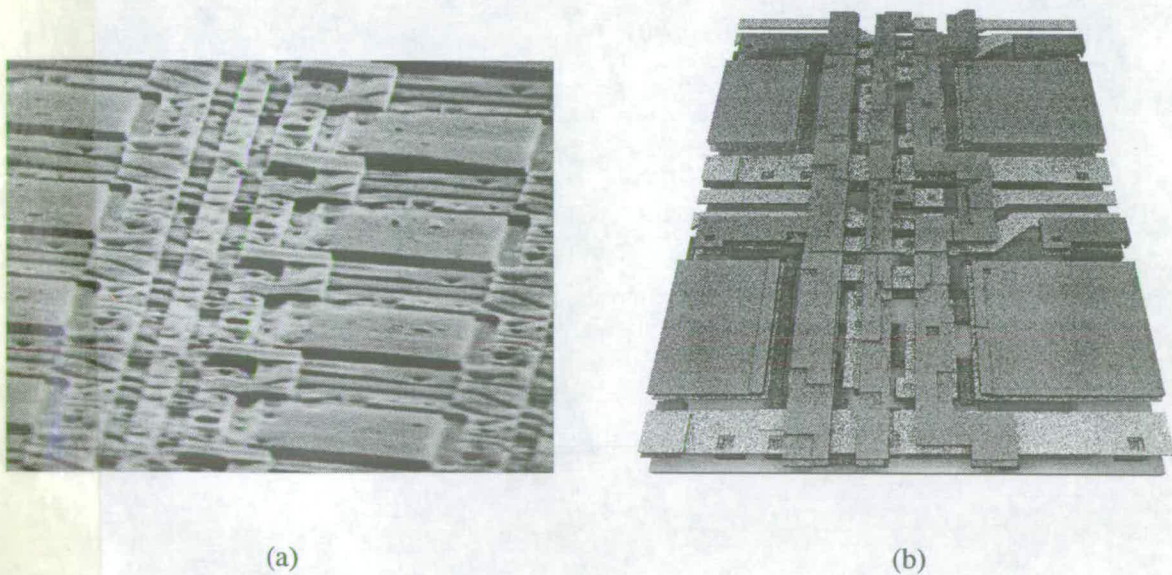

(a)   (b)

Figure 5. SEM and 3DTOP depictions of an array of SLM pixels

Conclusions

A comparison of planar and conformal 3D circuit descriptions has shown that as circuit complexity increases, so too does the percentage increase in interconnect capacitance found using conformal data compared with interconnect capacitance found using planar data. Software has been described which automatically generates a conformal 3D representation of an IC. An example of how the conformal 3D data might be used has been described, showing that parasitic interconnect capacitances can have an appreciable effect on circuit operation. The 3DTOP software has been shown to be successful in representing IC topography. Further work is being done to achieve a more realistic topographical description.

References

[1] K.Nabors, S.Kim, J.White and S.Senturia: "FastCap User's Guide", 1992

[2] Technology Modelling Associates, Inc.: "Raphael User's Manual"

[3] R.H.Uebbing and M.Fukama: "Process-based three-dimensional capacitance simulation - triceps", IEEE Trans. on CAD, Vol 5, No 1 Jan 1986, PP 215-220

[4] A.H.Zemanian, R.P.Tewarson, Chi Ping Ju and Juif Frank Jan: "Three-dimensional capacitance computations for VLSI/ULSI interconnections",IEEE Trans on CAD, Vol 8, No 12 Dec 1989, PP 1319-1325

[5] S.Kumashiro, R.A.Rohrer and A.J.Strojwas: "Asymptotic waveform evaluation for transient analysis of 3-d interconnect structures",IEEE Trans. on CAD, Vol 12, No 7 July 1993, PP 988-996

[6] Technology Modelling Associates, Inc.: "Lorenzo User's Manual"

[7] D.C.Burns: "Design and characterisation of a ferroelectric liquid crystal over silicon spatial light modulator", PhD Thesis, University of Edinburgh, 1994