On Chip Control Techniques for Single Chip CMOS Video Cameras

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Abstract

MOS technology permits the inclusion of image sensor with other control and processing functions on the same silicon substrate, allowing low-cost miniature cameras and vision application systems to be made.

The objective of this project has been to develop design techniques to integrate basic control and processing functions on chip to achieve monochrome and colour single chip video cameras. Such functions include automatic exposure control, automatic gain control, composite video formatting, and automatic colour balance etc.

In this thesis, following an introduction, the fundamentals and basic structures of the sensor array, colour cameras, and camera control techniques are reviewed. Automatic exposure & gain control are covered in Chapter 3 and automatic colour balance is covered in Chapter 4. Chapter 5 then describes other control techniques such as video timing format, black level calibration, optical centre registration, and camera digital control interface. A monochrome single chip video camera chip named ASIS-1011 and a colour device named ASIS-3000 are reported in Chapter 6. Proposed future research work and conclusions are given in the final chapter.

The work reported here has shown that, by integrating control functions on chip, vision applications will certainly enjoy greatly reduced size, power consumption, and cost.

Declaration

Unless otherwise stated, the material contained herein was researched and composed entirely by myself in the Department of Electrical Engineering, University of Edinburgh between February 1989 and May 1994.

Mingying Lu (M. Lu)

Acknowledgements

I would like to record my gratitude to my supervisors, Dr. D. Renshaw and Professor P. B. Denyer, for their constant support and encouragement during the course of this work. I would particularly like to thank Dr. D. Renshaw for his endless patience and consideration.

I also wish to thank Dr. G. Wang for his invaluable cooperation in the development of this project and Mr. D. Henry for his valuable assistance with the colour balance experiments.

I conclude with acknowledgement to SERC, the University of Edinburgh, and VLSI Vision Ltd., for their funding and financial support.

Contents

Chapter1 Introduction

1.1 Project background

Over the years considerable research has been conducted in the area of image sensing and image processing. As we progress through the 1990's, the demands of the information age are spurring such applications. However, a great many application systems require massive processing power, and the hardware appears both expensive and cumbersome. This limits the range of practical systems which can be implemented.

Functioning as "eyes" for many of the systems, solid state image sensors have emerged as critical path technologies to move electronic image forward. Fabricated on silicon chips, these photosensitive semiconductors translate light intensity into corresponding electrical values, which can be displayed, stored, processed, or transformed.

Solid state image sensors are classified into three main categories: CCD (Charge Coupled Device), MOS (Metal Oxide Semiconductor), and CID (Charge Injection Device). All these sensors use the p-n junction as the photoreceptor. The difference among them is in the read-out techniques utilized. The majority of solid state cameras today use CCD technology, which over two decades has been highly refined to epitomize functions. A major disadvantage of CCD sensors and most commercially available image sensor chips is their requirement for off-chip sense and/or amplification circuitry, for off-chip digital control circuitry, and for multiple supply voltage levels.

On the other hand, MOS technology allows integration of processing logic together with a sensor array on the same substrate. Therefore, it will be possible to implement smart single chip vision application systems, with the advantages of solid state image sensors and VLSI processing ability. Many research efforts have been concentrated on this area [Lyon,1981; Tanner, 1984; Forchheimer 1990; Gibertoni, 1991; Anderson, 1991; Fossum, 1994; Mendis, 1994; Ricquier, 1994], of which, the recent development in our group is of significance. Based on the structure proposed by P. B. Denyer and the noise compensation technique developed afterwards, good quality image sensors can be fabricated using unmodified CMOS ASIC technology [Denyer, 1989; Renshaw, 1990; Wang, 1991].

To achieve smart application systems, more research is needed to integrate those basic camera functions which are usually implemented off-chip electronically or mechanically. Such functions include automatic exposure control, gain control, black level calibration, and composite video formatting, etc.

There are appreciable advantages to be gained by building a colour imaging system using solid state sensors instead of vacuum tubes. In most colour cameras using vacuum tubes the incident light from the scene is separated into the red, green, and blue components by a prismatic assembly located behind the lens. The three colour components are then sensed separately by three tubes, which need strict alignment. Solid state sensors have the advantage of making colour arrays on the same substrate without worrying about the alignment of arrays. Solid state sensors also have the advantage of geometric scan accuracy. This makes it possible to make compact colour sensors only using one sensor array. This is achieved by depositing colour stripes or mosaic directly onto the photo array, making three neighbour pixels produce different colour information.

While we have demonstrated the viability of CMOS ASIC for monochrome image applications, it is desirable to extend this research to colour applications. The control functions of automatic exposure control and gain control for colour cameras will be more complicated than those of monochrome cameras. There are also new functions such as colour balance which needs to be developed.

1.2 Project review

I have taken part in the project since the March of 1989. The research was initially supported by University of Edinburgh Quantum Fund and the Science & Engineering Research Council (Grant GR/F 36538 IED2/1/1159, Augest/1989-July/1992) with Dr. D. Renshaw and Professor P. B. Denyer as principal investigators [Renshaw, 1992]. The research has since been supported by VLSI Vision Ltd. I registered as a part-time Ph.D. student in October, 1990 with Dr. D. Renshaw and Professor P. B. Denyer as supervisors.

The objective of my project has been to develop on chip control techniques to achieve single chip monochrome video cameras, and then colour video cameras, in unmodified

CMOS processes. Another researcher concentrated on the analogue block, including sensor structure and associated amplifying circuitry. My supervisors have given many informative instructions.

We started with monochrome video cameras. Six different designs have been completed during the past 4 years, including 3 commercial products. These designs have proven that the integration of sensor array together with on chip control functions will result in unprecedented reductions in size, cost and power consumption.

The main control functions are summarized as follows:

- Automatic exposure control has been implemented on chip, enabling the use of a single, fixed-aperture lens. Control is achieved by varying the integration time, in response to the live image of the sensor array. One device has achieved a total exposure range to 40,000:1, wider than that of most commercial cameras.

- Gain control is implemented through putting a digitally controlled MDAC (Multiplying Digital to Analogue Converter) as an adjustable load. It extends sensitivity in low ambient light so that a dim image can became more visible on a monitor and more detail is retained in data conversion.

- Digital control logic such as TV-formatting, photoarray driving, have been integrated on the same substrate to implement single chip video cameras.

- Other technical features include auto-calibrated video black level and a simple method for wafer stage test.

The primary goal for colour cameras is to maintain the existing advantages of economy, size, and power consumption whilst extending the monochrome capability to full colour reproduction. We believe these goals can be achieved, and indeed that the colour form of this technology may exhibit even greater advantages in these criteria than in the monochrome case.

Contemporary consumer cameras use a single lens and sensor, but the sensor surface is covered with a mosaic of grid of colour filters. Pixels of different colours are demultiplexed at the sensor output and interpolated to form synchronous parallel colour signals. This is well-suited to volume production as the surface colour mosaic can be fabricated as an extension of the semiconductor wafer fabrication process. However, this technology tends to be captive to the existing colour CCD camera manufacturers, and we did have difficulty to find a foundry service who were willing to make surface colour mosaic for us.

An alternative approach was then proposed by Professor P B Denyer. This approach builds three sensor arrays on one chip. Each array has its own lens, and contain a different colour filter. The obvious disadvantages of such a solution are parallax and alignment errors between physically separate sensor arrays. It has been shown that the parallax error can be made acceptably small for small sensor geometries [Denyer, 1992; Henry, 1992], and the potential problem of alignment is greatly eased by fabricating the three sensors on the same chip substrate. This ensures that the cameras all lie in the same plane and have the same rotational orientation. Assuming lenses can be accurately assembled in a parallel plane, the only possible alignment errors are simple orthogonal translations in the form of vertical and horizontal errors in the centres of the optical axes. It is easy to calibrate these cameras after assembly and to electronically correct for these translations.

The design and fabrication of such a device was sponsored. It took 18 man/months to complete the chip design, of which, 6 man-months were for the analogue part (undertaken by another researcher) and 1 man-year was for the research and implementation of digital circuits carried out by me. The design intended to use 0.8μm, 2 level metal CMOS technology of VLSI Technology, and actually has passed the pre-sign-off procedure with the foundry. However the design did not go to fabrication because of perceived problems in manufacturing the triple lens with 2-elements per lens. Single-element plastic lenses can not deliver the required (320 × 240) pixel resolution. The funding of the fabrication was then cancelled.

Although the chip hasn't been fabricated, the design itself has been completed and innovative control functions have been incorporated:

- Automatic exposure control has been implemented on chip, enabling the use of fixed-aperture lens. The integration time was varied uniformly so that exposure setting for all sensors are the same. The exposure is judged by counting number of "well exposed colour pixels" and "over-exposed colour pixels". The total exposure range is 3,000:1.

- Gain control is implemented through putting a digitally controlled MDAC as an adjustable load to each colour channel. The nominal resistor value of load transistors have been made different to compensate the sensitivity difference of three primary colour pixels. The gain is also judged by counting number of "well exposed colour pixels" and "over-exposed colour pixels". The gain control range is 20 dB.

- colour balance is required to correct inequality in the response of the three colour channels. A novel colour balance control scheme has been developed to use the colour information from the main sensor array. Instead of an analogue signal processing, the scheme uses a pure digital signal processing method. The scheme has made it possible to integrate the colour balance function together with the main sensor array on same chip. The colour balance function can compensate for spectral variation of ambient light, covering the colour temperature of light sources from 3,000K to 9,000K.

- Digital control logic is included for TV-formatting, delivering EIA-standard R, G, B video outputs. A composite colour NTSC video signal can be produced using the AD720 RGB to NTSC encoder device.

- A serial interface has been included to allow a host computer to set operational parameters and to control exposure and gain values. The host can also interrogate the camera to determine the camera capability and current state.

- Automatic black level calibration maintains stability of the image output, obviating the need for externally-adjustable components.

By implementing the above functions on chip and completing the design with circuit details, I have greatly built up the knowledge, skill and experience. Moreover, most techniques and component circuits can be directly used in a range of new colour sensor devices in future.

Other than designs mentioned above, eight technical papers have been published [see publications], of which one paper entitled "On-chip Automatic Exposure Control Technique" won the "Best Paper Award" in the conference of ESSCIRC'91. Another paper entitled "CMOS Video Cameras", won the "Best Circuit Award" in the conference of EURO ASIC 91. There was also an "Award for Innovative Technology", at the International Fire and Security Conference at Olympia in 1992, granted for a remote alarm verification system which is based on a customized image sensor chip developed by us [Watts, 1992; Wang 1990].

The principal achievements and novel contributions made by the author of this thesis in the research reported here are:

- on chip automatic exposure and gain control technique
- on chip digital automatic colour balance control technique
- implementation of these digital functions in CMOS single chip video cameras.

The digital automatic colour balance control technique is an entirely new method, no similar method has been seen in this field or other relevant areas. It may be suitable for other digital colour image systems as well. The on chip automatic exposure and gain control were the first reported in the world. All of these successfully implemented control functions were important steps in realizing commercial products from the research reported here and in [Wang, 1993].

The most immediate commercial benefit and probably the most significant outcome of this research has been that it has successfully engendered a new line of business, with

the foundation of VLSI Vision Ltd. This is a company set up by Prof. Denyer and Dr. Renshaw to trade in CMOS image sensor and sensor-processor designs and techniques. In 1993 the company won a Scottish Innovation Award of 1993 (The John Logie Baird Award For innovation).

1.3 Thesis structure

In this thesis, following the first chapter of introduction is a chapter of overview which reviews the evolution and present status of research and development in the field of solid state image sensors, with focus on the control techniques and colour cameras. The basic architecture of CMOS sensors and the fundamental of colour sensor structures are introduced.

Automatic exposure control (AEC) and automatic gain control (AGC) are common camera features required to improve dynamic range. The third chapter will discuss how to electronically adjust the exposure, how to adjust gain, and how to implement on chip control functions for both monochrome and colour cameras. The circuitry, principles, and block diagrams will be presented.

The fourth chapter will discuss colour balance which is required to correct inequality in the response of the three colour channels. The fundamental of colour science related to TV system will be introduced first. The novel scheme of colour balance judgement will be described. The experimental results using Macintosh computer and detailed on chip implementation will all be covered.

The fifth chapter will discuss other techniques such as the on-chip video timing, black level calibration, optical centre registration etc.The sixth chapter will present two design examples. One is a single chip monochrome video camera, named ASIS-1011, which we believe is the smallest commercial video camera in the world. The design, the features, and the characterization will be covered. Another example is a highly integrated colour camera, named ASIS-3000, which has on chip control functions such as auto exposure and gain control, colour balance, black calibration, and TV formatting, et. al. The design, the main functions, and features will be covered. The last chapter will contain discussions on remaining problems, recommendations for future work, and conclusions.

Chapter2 MOS Image Sensors and Colour Cameras: An Overview

2.1 Introduction

Work on solid state image sensors was started in 1960s. Since then, it has experienced a tremendous amount of development due to its advantages over vacuum tube image sensors. These advantages are: the much greater compactness, the low voltage and power reduction, the reliability and expected cost reduction. Also, digital scanning provides a geometric accuracy of scan and a versatility of addressing. These advantages could introduce many new applications which were not feasible for vacuum image devices, such as pick up tubes, which require the large amount of space for the electronics and coils, and large power consumption.

There are appreciable advantages to be gained from building colour image sensors by using solid state sensors instead of vacuum tubes. In colour cameras using vacuum tubes, the incident light from the scene is separated into the red, green and blue components by a prismatic assembly located immediately behind the camera lens. The three colour components are then sensed separately by three tubes. Great care has to be taken to ensure that the three beams sweep with nearly perfect mutual registration. In replacing these tubes with solid state sensors, the discreteness and precision geometry of the integration sites and the clock controlled readout can automatically ensure linear and mutually aligned tracking of the scan in all three sensors, once the initial mechanical positioning has been done.

Solid state image sensors have the advantage of geometric scan accuracy. This makes it possible to make compact colour cameras only using one sensor array. This is achieved by depositing colour pattern filter directly onto the photo-array, making 3 neighbour pixels produce different colour information. The resolution of the array for the use of colour cameras is 3 times that of monochrome cameras. The reduction in yield associated with larger devices and problems with the fabrication of the colour filter have been solved. Today, colour solid state cameras with TV broadcasting

standard resolution are in wide use.

Solid state image sensors come in several technologies, including CCD (Charge Coupled Device), MOS (Metal Oxide Semiconductor), and CID (Charge Injection Device). All these sensors use the p-n junction as the photoreceptor. The difference among them is in the readout techniques utilized [Weckler, 1965; Tseng, 1965; Chamberlain, 1986]. The majority of solid-state cameras today use CCD technology which, over two decades, has been highly refined to optimize its performance. However, cameras and vision systems addressed by today's CCD technology are still power-hungry and expensive, and fall short of the highest level of integration.

On the other hand, MOS technology, as a popular VLSI technology, is very attractive for achieving low-cost miniature cameras. Another important factor is that MOS technology, especially CMOS, permits the inclusion of the sensor with other control and processing functions on the same chip. Therefore MOS technology is the most suitable if not the only technology which can be used to achieve single chip video cameras, which require on-chip processing such as TV formatting, exposure control, gain control, and colour balance for colour applications.

2.2 MOS image sensors

2.2.1 Fundamentals

It is well known that silicon can act as an excellent photoreceptor over the visible spectrum. One of the most significant developments leading to the realization of a practical solid state image sensor was the utilization of the p-n junction photodiode in an integration mode. Charge-storage operation is based on the principle that, if a p-n junction is reverse-biased and then isolated, the charge stored on the depletion layer capacitance decays at a rate proportional to the incident illumination level [Sze, 1981; Middelhoek, 1989; Haskard, 1988; Sequin, 1975]. Therefore, a photodiode array can be used to produce electronic signals corresponding to the focused image. To electronically "read" this picture, each pixel on the array is selected in the sequence, controlled by the scan circuitry along both y-direction and x-direction. The image, in

the form of electronic charge, can be restored by display devices such as TV monitor and computer terminal.

Solid state image sensors are classified into three main categories: CCD (Charge Coupled Device), MOS (Metal Oxide Semiconductor), and CID (Charge Injection Device). All these sensors work on the principle of charge storage, utilizing essentially the same photodiode structure to sense incident light and convert it into an electric signal. The main difference is in the way they read out signals. CCD devices transfer the signal charge by manipulation of MOS potential wells. It shifts the signal charge in series to an output sensing node. CID devices transfer the collected signal charge within an individually addressed pixel, and sense displacement values across the electrodes at the site. MOS devices transfer the signal charge by multiplexer the photoarray, using digital scanner, in the way similar to RAM readout [Weckler, 1965; Tseng, 1985; Chamberlain, 1986; Hobson, 1978; Sun, 1988; Tompsett, 1973].

The majority of solid-state cameras today use CCD technology which over two decades, has been highly refined to optimize performance. On the other hand, the attraction of MOS sensors is that it is the dominant technology for VLSI chips. Therefore, this technology is more easy-access and cost effective. More importantly, this technology has the advancing capability, permitting the integration of control and process logic on the same substrate. A smart vision system may be implemented on a single chip with the advantages of both solid state image sensors and VLSI systems.

Other virtues of MOS sensors include the full inherent sensitivity, low voltage driving, custom pixel structure, and flexible readout scheme. Unlike CCD or CID pixel structure, MOS sensors require no surface electrode on the top of discrete photodiode so that there is no interference pattern or light loss. Like all MOS devices, The sensors only require a single low voltage driving (normally 5 volt).

Other than a photodiode and an access transistor on each pixel, extra transistors can be put in to enhance the function of the pixel. For example, a transistor connecting the photodiode to ground may be added to increase the anti-blooming ability [Renshaw, 1991]. Another example is APS (active pixel sensor) structure which is defined as a

detector array that has at least one active transistor within the pixel unit cell. The investigation on APS technology has been reported and reviewed [Fossum, 1993]. Toshiba use "double-gate floating surface transistor" as output amplifier in pixel cell [Yamashita, 1988; Matsunaga, 1991]. Jet Propulsion Laboratory reported several kinds of pixel structures to increase sensitivity of the sensor [Mendis, 1994] in order to be suitable for scientific applications. This technology is suitable for further on-chip integration of control timing, control logic with image sensor.

The sensor array can be read out in the normal sequence or in other scan out schemes. One example of alternative scan scheme is a CMOS image sensor chip for fingerprint verification [Anderson, 1991]. The addressing and read out circuits have been modified to allow local two dimension smoothing (3×3) to take place as the image data is scanned out. Just by changing the readout scheme, the required low-pass filtering is implemented without any hardware overhead.

However, normal MOS sensors suffer a significant problem: high noise. The large video line capacitance results in high random noise. Process nonuniformity results in the fixed pattern noise. These are limitations which hamper the huge potential application and market of MOS image sensors. The main concern has been concentrated on reducing noise and improving picture quality [Wang, 1993].

2.2.2 Structures

The predecessor of the MOS image sensor can be dated back to 1965 when the first monolithic integrated photodiode array structure was announced [Weckler, 1965]. It consisted of 200 photodiodes, each associated with a MOS FET. The gates of the MOS FETs are individually driven by an external scan generator. However, this structure wasn't developed further at that time because MOS technology was in its infancy. Instead, a phototransistor structure was pursued. It was thought to be better due to the transistor gain. The major disadvantages and factors which eventually returned the photodiode to favour, were the random variations in transistor gain and the low level threshold due to the emitter offset. Only after MOS technology was developed (in particular silicon gate technology), and the marriage between MOS technology and the

photodiode array operating in storage mode resulted in today's MOS image sensor.

MOS sensors use a digital scanner to multiplex signal charges from photo pixels to the output, in the way similar to RAM readout. A typical structure of MOS sensors has been shown in Figure 2.1.

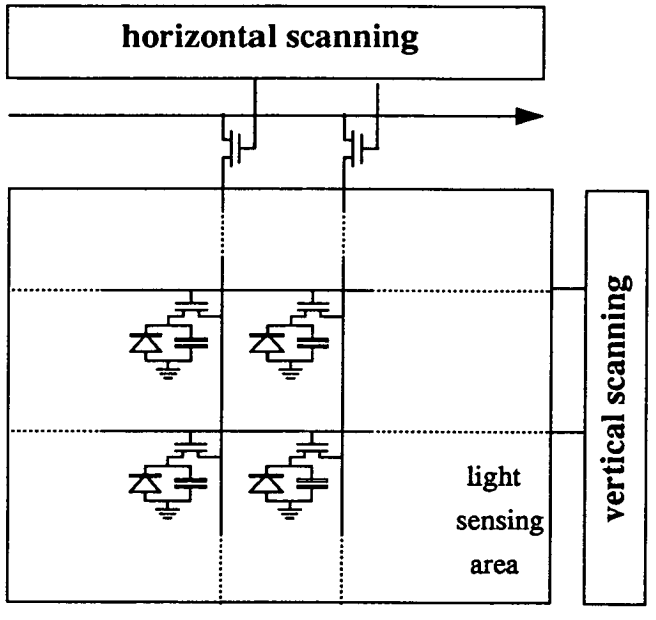

Figure 2.1. Normal structure of MOS sensors.

The light sensing area consists of a diode array matrix, schematically indicated by the columns and rows of individual photo-pixels. The photodiodes are pre-charged to a fixed bias voltage and then isolated. This results in a fixed charge being stored on the associated junction capacitance. The photodiodes are then left isolated for a suitable exposure time. During this time, incident light upon each pixel partially discharges the junction capacitance. The rate of discharge is proportional to the incident light level. The final charge retained on the capacitor, after a fixed time interval, will represent the light intensity at that point of the image. The pixel signal is read out by opening the gate, connecting the photodiode to the MOS transistor drain. All of the drains in each column are connected in common and only one row is read at any time. The column lines are

then gated through an analogue multiplexer to a single external charge sense amplifier.

Hitachi is a leading company which developed MOS sensors. It introduced colour video cameras in 1981 and camcorders in 1985 [Noda, 1986; Asano, 1988]. A array structure called TSL (Transversal Signal Line) structure, as shown in Figure 2.2 was developed by the company.

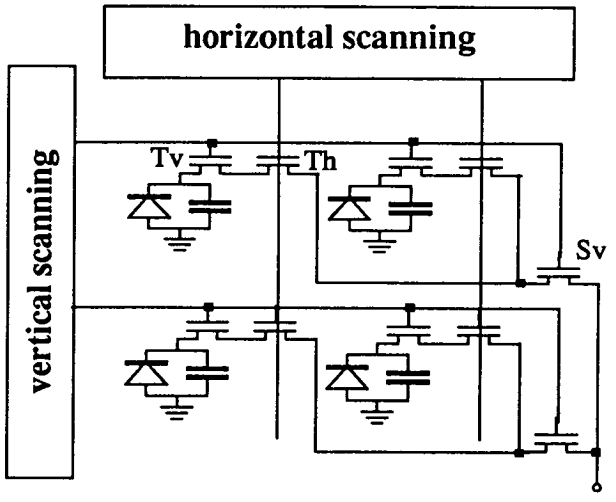

Figure 2.2. TSL structure.

Comparing with the normal structure of Figure 2.1, a new MOS switch is added to each pixel and the signal readout line is laid out horizontally. The information stored in each photodiode is read out in the following manner: the vertical shift register turns on the Tv and readout transistor (Sv), and the horizontal shift register turns on Th by transferring information to the external. The essence of this structure is that electric charge from each pixel stays only a short time on the signal line so that smear noise is suppressed. Normal structure may suffer from smear noise from overcharging of the vertical signal lines during the horizontal scanning period.

In the MOS sensor structures shown above, the signal charge is usually read out through the column line with large parasitic capacitance. Commonly, the column lines are gated through an analogue multiplexer to a single external charge sense amplifier. The

requirements of this amplifier are daunting considering that wide dynamic range and high-speed must be achieved from a charge packet in the pixel which may be of the order of fC.

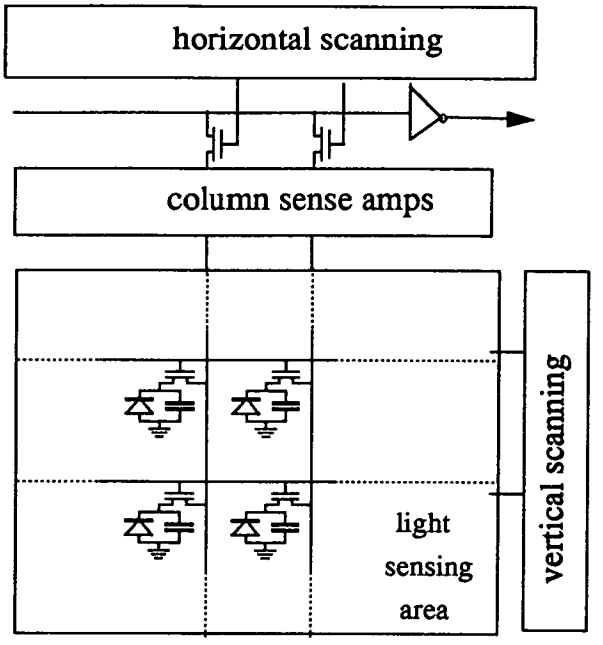

Figure 2.3. A new structure of MOS sensors.

Accordingly a scheme was proposed to overcome this problem [Denyer, 1989; Renshaw 1990]. The novel feature of the scheme is the integration of analogue CMOS charge sensing amplifiers at the top of every bit line, as shown in Figure 2.3. The benefits are that these amplifiers need not work so quickly, since their activation frequency is equal to the line rate rather than the pixel rate; and they are situated as close as possible to the pixel array so the line capacitance is reduced.

Experimental work has shown that, with sense amplifiers on the top of the array, the readout of the signal charges becomes easier. The random noise is reduced. However, the design of sensor amplifiers is a challenge. The amplifiers should have enough gain, be physically pitch-matched, and be insensitive to the mismatches caused by parameter variations [Wang, 1993].

The threshold voltage variation of sense amplifiers is a major cause of fixed-pattern noise. This pattern repeats every line, shown as vertical stripes on the screen of the display device. In order to compensate this noise, a sense amplifier structure was reported [Wang, 1993], as shown in Figure 2.4.

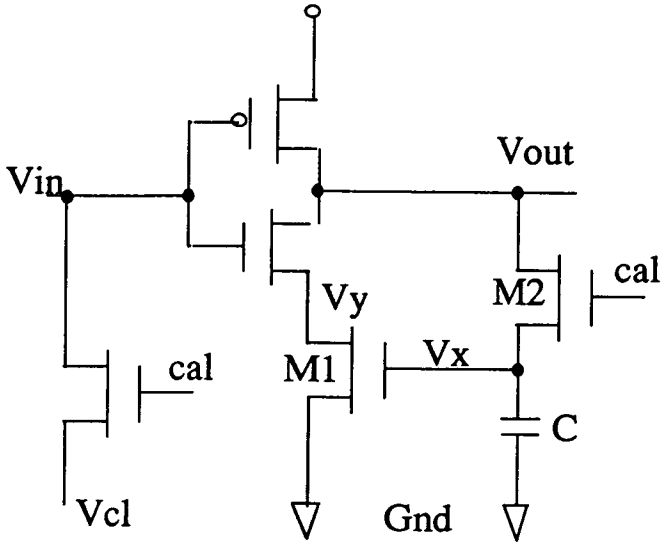

Figure 2.4. Calibrated sense amplifier.

Each amplifier is calibrated to give zero offset during the idle interval between line readout. An n-channel MOS transistor is connected in series with the Gnd power connection of the inverter. The drain voltage V_y of this transistor effectively becomes the new ground voltage reference for the inverter. Accordingly, the transfer characteristic of the inverter is dependent upon V_y and generally the switching threshold will vary in some proportionate relationship to V_y, which is in turn determined by V_x.

To achieve automatic adjustment of the inverting amplifier switching threshold to approach a given reference voltage, an external reference voltage V_{cl} is supplied to the inverter input. At the same time transistor M2 is enabled thereby connecting the gate of

M1 to the inverter output. This is a configuration of negative feedback and for suitable design values the circuit will settle to a stable value of V_x such that the switching threshold is achieved at an inverter input voltage of V_{cl}. This is the desired operating point. Once this condition has been reached M2 may be turned off, thereby breaking the feedback loop but leaving the correctly adjusted value of V_x held on capacitor C. The inverter may now be used in its normal capacity and will exhibit a switching threshold approximately equal to the programmed value V_{cl}.

With the calibrated sense amplifiers at the top of the array, both random noise and fixed-pattern noise are reduced to a level so that MOS sensor performance can approach that of CCD cameras. This is an important development for MOS image sensor structures.

2.2.3 Smart MOS sensors

Most commercial MOS cameras (such as Hitachi's) at present do not integrate control logic together with the sensor array. They usually consist of a X-Y addressable MOS photoarray chip, along with boards of components. One reason is that MOS sensors are so noisy that complicated off-chip sense and amplification circuits are needed. Another reason is that, although the digital circuitry can be put on chip, the digital interference causes a big problem. The cameras assembled in this way do not enjoy the real virtue of the MOS technology. They can not compete with CCD cameras because of the inherent high noise.

Other works have recognised the attraction of implementing sensors in an unmodified CMOS process, permitting the inclusion of the sensor with other control and processing functions on the same chip [Lyon, 1981; Tanner, 1984; Forchheimer 1990; Gibertoni, 1991; Anderson, 1991]. Even though the image quality is not as good as that of CCD, it is still very attractive to include a sensor array with other control and processing functions on the same chip. There are many applications where the image quality may not be so crucial but other matters such as cost, volume, power consumption, and

system integration are more important.

One early example is a one-dimensional motion detector [Tanner, 1984] which consists of an array of photodiodes for detecting the light pattern, a storage array for the image, circuitry to compute the correlation between the stored image and the current one, decision circuitry to determine where the correlation is greatest, and a self timed controller to sequence the entire system.

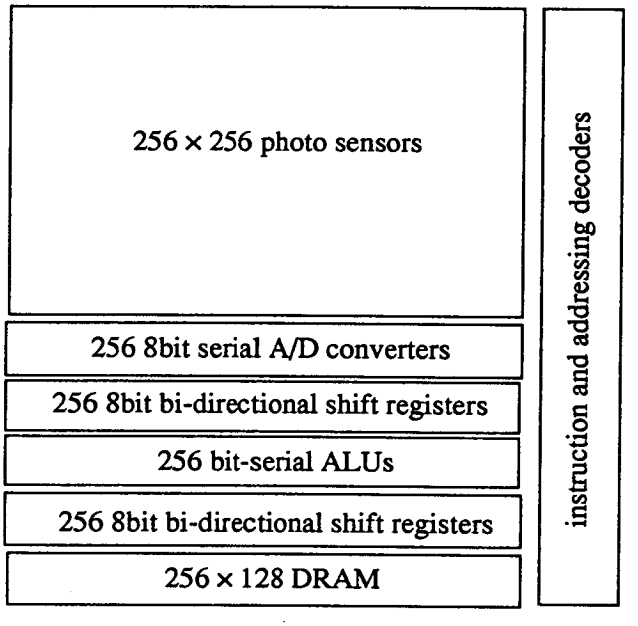

Figure 2.5. A matrix array picture processor.

Another example is a matrix array picture processor which can handles image processing tasks such as sensing, digitization and data reduction. [Forchheimer, 1990]. The device contains a 256 × 256 photosensor array, 256 8-bit serial A/D converters, 256 bit-serial processors and a 256 × 128 memory. Two 256 × 8 bidirectional shift registers are used for communication between processor elements and I/O (Figure 2.5). This chip is aimed at pre-processing of gray level images and binary images, eliminating the bottleneck of sequential image read-out that characterizes conventional systems. It is

suitable in applications demanding high-frame rate digital image processing with greatly reduced I/O bandwidth, complexity and system cost. [Gibertoni, 1991] also reported a smart image sensor for computer vision. The chip comprises a grid of light sensitive pixels and a set of processors operating in parallel.

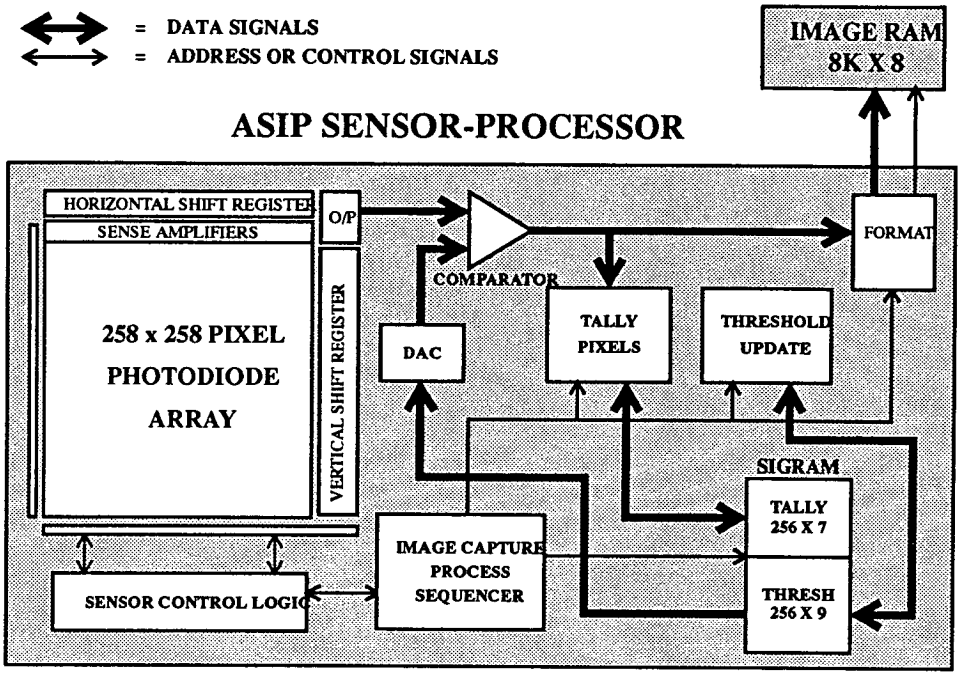

Figure 2.6. A sensor chip for fingerprint verification.

[Anderson, 1991] reported a smart image sensor chip for fingerprint verification. Other than a 258 × 258 pixel array, it includes image preprocessing and quantisation circuitry to form a normalised binary image, 64-cell 2000 M op/sec correlator array, post-correlation decision logic, 16K bits RAM, and 16K ROM (Figure 2.6). With the aid of two external devices (one 64Kbit RAM and one 8052 microcontroller), this device performs all of the image sensing and processing functions necessary to capture and verify a fingerprint against a stored reference print within one second. It shows that challenging imaging applications, such as fingerprint verification, can become possible in a system about the size of a credit card, consuming a few watts of power if MOS

technology is used. This is a good example to show how powerful a single chip MOS vision system can be.

2.3 Colour camera

2.3.1 Historic review

Research on colour reproduction can be dated back to 140 years ago. James Maxwell demonstrated a colour picture in 1861, in Edinburgh! He took three photographs for one picture through different filters of red, green, and blue. A colour picture was reproduced by projecting the three photos through filters again on a white screen simultaneously. This experiment is fundamental to all the following development of colour reproduction techniques, in the field of photography, printing, and television. Today, the principle of Maxwell's method is still universally used.

The development of TV cameras tube (Icono scope) can be dated back to the 1930's. Monochrome TV cameras were then produced since 1940's, using Orthicon tubes, which have good image quality but are too big and heavy to be used by colour cameras. A new generation of camera tubes called Plumbicon tube appeared during the 1960's [Sun, 1988]. This tube using a diode gun could be made smaller. The diameter of the tube can be as small as one inch. This smaller size tube made colour TV camera possible. The system of colour cameras is much more complicated than that of monochrome camera, considering that colour cameras need to generate three primary colour signals.

The first issue is a complicated optical system. An extra optical system which can separate colour image into three primary monochrome images is required, either using a dichroic prism or colour filter.

The second issue is the complicated electrical system. These three primary images are split by the dichroic prism or separated by colour filters have much lower luminance than that of full colour images, resulting in the requirements of high sensitivity and lower N/S ratio of the tube.

The third issue is the complicated control system. Three RGB channels electrical parameters must be balanced. The colour signals, L (luminance), Cr and Cb (two chrominances) need to be modulated to form composite colour TV signal.

Solid state image sensors provided a new technology to make video cameras. The size and weight of the camera can be greatly reduced. Other advantages include long life, small power consumption and no damage from strong oscillation, etc. The colour video camera with solid state sensor appeared commercially in the early 80's [Aoki, 1980; Nabeyama, 1981], followed by the appearance of camcorders in several years later.

2.3.2 Colour camera structure

Electronic colour cameras classically use following approaches for forming colour images:

(1). 3-tube cameras

Typically pre-CCD colour cameras use a single lens followed by a dichroic prism which forms three R,G,B images. Three tubes are used to simultaneously detect these images. Three tubes must be accurately aligned, and then a high quality colour picture can be achieved. However the tubes' assembly and alignment with the dichroic prism and lens are very difficult for volume manufacturing processes. This technique is therefore used exclusively in broadcast-quality equipment.

(2). Single tube cameras

Single tube colour cameras use colour filter stripe covering on the surface of sensor. Some advantages are obvious in this structure. It has smaller size and no alignement difficulty for camera assembly. This structure is easier to build than that of the three tubes, but further development is needed at separating R,G,B signals from the output of the tube, as are increasing resolution and improving sensitivity. The output of the tube with electronic beam scan is a continuous waveform with the three colour signals mixed together. The research on single tube cameras focused on "frequency separation" [Kell, 1956; Briel, 1970; Boyd, 1973] or "phase separation" [Kubota, 1972] techniques to

separate three primary signals.

In the 1970's single tube colour camera products were mainly represented by the Kell system cameras that used frequency separation mode. In the 1980's Sony's products were representative of the single tube colour camera using phase separation mode.

With CCD image sensor technique development, the single chip with colour filter stripe found its place. Every pixel in a CCD image sensor array is discrete sample point. Three primary colour signals are very easy to separate from output of the CCD sensor just by using digital demulplexing circuits.

(3). Colour mosaic cameras

Pixel structures of CCD sensors make it easy to build single chip colour cameras. Pixels of different colour are demultiplexed at the sensor output and interpolated to form synchronous parallel colour image signals. This is well-suited to volume production as the surface colour mosaic can be fabricated as an extension of the semiconductor wafer fabrication process.

Pixel-pitch colour filter patterns of single chip cameras vary from maker to maker because people seek better resolution, better sensitivity solutions. Research has found that peoples' eyes have higher sensitivity to green light than that to red and blue. If the colour filter pattern assign more green pixels than to red or blue pixels, it can increase the resolution of the camera without increasing the gross pixel number. The basic structure of colour mosaic filter patterns is a chequer board pattern, shown in Figure 2.7 [Bayer, 1976; Dillon,1978]. This structure is called Bayer filter which increases the number of green pixels to half of total, and reduces the number of the red and blue to a quarter so that the green signal frequency is increased, and the colour uniformity of the images is kept.

Apart from using R,G,B colour elements for colour mosaic filters some makers use other colour elements, such as W(white), Ye (yellow), Cy (cyan) colours [Fairchild], shown in figure 2.8. R, G, B, L (luminance) can then be produced by sums of W, Ye, Cy according to the following relationship:

$R = W - Cy; \quad G = Cy + Ye - W; \quad B = W - Ye; \quad L = Cy + Ye + 0.66aW$

where a is an adjustable quantity near unity.

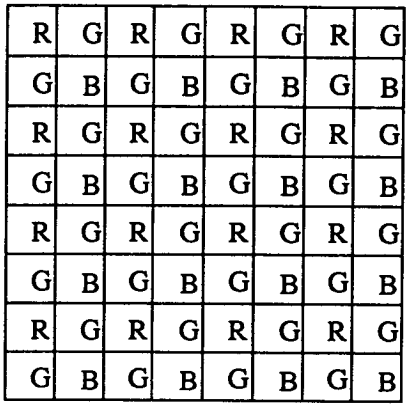

Figure 2.7. Bayer RGB colour mosaic filter structure.

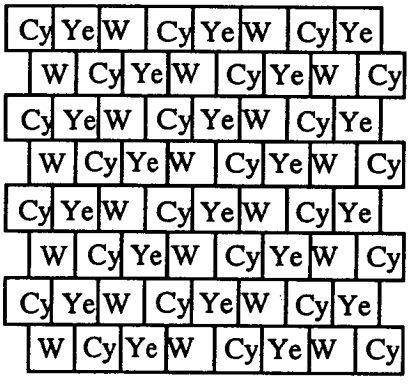

Figure 2.8. Staggered colour filter pattern using white, yellow, Cy elements.

(4). Tri-Sensor cameras

Based on our CMOS VLSI monochrome camera techniques, Prof. P.B. Denyer

proposed an approach to colour cameras [Denyer, 1992]. The primary goal is to maintain the existing advantages of economy, size and power consumption whist extending the monochrome ability to full colour reproduction.

In this approach three separated sensors are integrated on one chip, each with its own lens and one colour filter on the sensor array. It looks like that three single monochrome cameras are built on the chip. The obvious disadvantages of this approach are parallel and alignement errors between physically separated cameras. Calculation [Henry, 1992] shows the parallax error can be made acceptably small for small camera geometry, and the potential problem of alignement is greatly eased by fabricating the three sensor on one chip. This ensures that the cameras all lie in the same plane and have the same rotation orientation. Assuming lenses can be accurately assembled in a parallel plane, the only possible alignment errors are simple orthogonal translation in the form of vertical and horizontal errors in the centres of the optical axes. It is easy to calibrate these cameras after assembly and to electronically correct for these translations.

The advantage of the approach is that it avoids the use of colour mosaic filter technology which is not an easy-access foundry service.

2.4 Control techniques for cameras

In order to enhance functions of video cameras, electronic control techniques have been developed with the progress of video cameras. These control techniques include automatic exposure control [Asano, 1988], auto-iris, auto-focus[Toyoda,1986], auto black calibration, auto white balance[D'Luna,1991], automatic optical registration [Woad, 1971; Critchley, 1972], auto high gain etc. Since the 80's microcomputers have been widely used for the automatic control or programmable control [Sanderson, 1981].

However, all above control functions are implemented off the chip of sensor devices. Most commercial solid state sensor cameras (such as Sony's CCD and Hitachi's MOS) at present need a sensor device along with boards of components. The cameras assembled in this way do not enjoy the real virtue of the advanced VLSI technology,

integration. It is a real limitation for a lot of vision applications although it has been so successful in the camcorder market.

The following sections review some of common camera control techniques.

2.4.1 Automatic exposure control

The exposure parameters comprise the diameter D of the iris and electronic shutter time of Camera (with CCD sensors) or integration time (in MOS sensors). The iris control is usually driven by a motor that can rotate forward or backward. According to the brightness information detected by sensor, the iris D will be bigger for more light to come in or smaller for less light. The shutter time or integration time of the sensor is mostly controlled by electronic circuits. For TV cameras, the electronic shutter time could be as long as one frame period, or as short as one line period [Asano, 1988].

In CCD devices all pixels of the array are exposed to light simultaneously, so that the exposure time is similar to the shutter time of ordinary film camera. In MOS devices pixels of the array are operated sequentially row by row, so the integration time is counted as the interval from the pixel reset to pixel sample. The sample timing of the pixels is usually fixed, and the integration time can be varied by moving the timing of reset.

2.4.2 Automatic white balance control

When the ambient light sources change, the light intensity and spectral energy distribution of the ambient light could change. The light intensity variation can cause the brightness of the images to change, which then could be compensated with varying exposure parameters. The spectral distribution energy change will cause the loss of colour fidelity, which then could be compensated by varying the gains of the three signal channels. In order to maintain colour consistency of an object viewed at different light sources by the colour camera, auto white balance control technique is needed, which emulates the human eye and brain function to control the gains of the three channels automatically.

A simple automatic white balance control equalizes RGB signals for a white target under existing illumination conditions[D'Luna,1991]. This auto white balance control estimates the colour corrections from image data directly, but it is not a real-time controller.

Hitachi [Imaide, 1990] reported their auto white balance (AWB) control technique in 1990. The control circuits include both analogue and digital signal processing and a white centre detector. The AWB can cover colour temperature variation (2500K-10000K) with a 20% softness (tolerance), because they thought the images with some under-balance situations are subjectively better than images which are over-balanced.

2.4.3 Automatic black balance control

If an image is white balanced but without being black balanced, the image may still not be correctly colour balanced because the signal level of the image could cover the whole range of output signal. Only when the white level and black level are both balanced can the camera give colour balance in the full range [Sun, 1988].

Black balance is a shift of each black level of the three primary R,G,B signals to a same level. The purpose of this black level clamping is to establish a stable black reference value, which is equal to the average sensor dark current under actual operating conditions for the image. The dark value can be determined by averaging some black pixels located at the board area of the image sensor [D'Luna,1991].

In PAL video systems the black level equals blanking of the video signal. In NTSC video system the black level is at above 7.5% over the blanking level while peak white level is at 100% and blanking at 0.

2.4.4 Automatic focus control

Current automatic focusing system measure the distance between camera and object and then adjust the focus. Most cameras use Infra-red to detect the distance of the objector. Infra-red rays emitted by LEDs are reflected by the objector and return to the

photodetector. The distance of an objector [Toyoda, 1986], D, is then given by the following formula:

$$D = R\ f/x$$

where, R is the distance from sensor centre to the infra-red detector, f is focal lens, x is height of the objector in image. The result of the measured distance is used to adjust the focal lens in the lens unit.

2.5 Chapter summary

The evolution and present status of solid state image sensors, especially MOS sensors, have been reviewed. Although CCD image sensors represent a more mature technology, MOS sensors have a great potential to implement smart vision application system with higher scale of integration and a lower cost.

The different structure of colour cameras were then reviewed. The mosaic colour filter structure is widely used at present but the technology is not an easy-access foundry service. An alternative structure is to integrate three separated sensors on one chip and each sensor has its own lens and colour filter. The MOS sensors with this structure can be fabricated using standard VLSI technology but the lens and filter have to be specially designed.

Common camera control techniques have also been reviewed. Most commercial video cameras need boards of components to implement control functions. With the progress of MOS sensors described in Section 2.2.2, it has become possible to integrate most of camera control functions on the same chip with sensor array. This is an area worthy further research effort.

Chapter3 Automatic Exposure & Gain Control

3.1 Introduction

Automatic exposure control (AEC) and automatic gain control (AGC) are common camera features required to improve dynamic range. This chapter describes on-chip solutions to implement these features.

3.1.1 Automatic exposure control

Normally in good lighting it is necessary to control the exposure so that the distribution of grey levels within the image is reasonably well balanced. Over-exposure (e.g. in bright lighting) can push the grey level distribution mostly towards the white extreme, causing loss of useful contrast, saturation, and possibly blooming. Under-exposure results in similar loss of contrast as the majority of the image is compressed into the black end of the range.

On-chip automatic exposure control is of significance to avoid mechanical iris control in electronic vision systems. To achieve this, two related problems have to be solved.

1. How to electronically set and vary exposure instead of using a mechanical iris.

2. How to automatically determine the current exposure setting.

The solution to the first problem is to adjust exposure setting by varying the light integration time of photo pixels. Thus a longer integration time will have the same effect as if a bigger iris is used and a shorter integration time will have the same effect as if a smaller iris is used. The exposure setting implemented in this way can be referred as Electronic Aperture. In the following sections, two schemes of such electronic aperture will be presented.

For a TV camera, the integration time can be as long as one field, or as short as a few

cycles of pixel clock (3 cycles for our sensors). In this way, a very wide range of 40,000:1 can be achieved.

The solution to the second problem is that we alter the exposure setting in response to the monitored image. Hardware for auto-exposure is put on-chip to analyse the present picture and then set a more accurate integration time for next field. The analysis is based on estimating the fraction of each picture for which pixel values are over some threshold values and then judging whether the picture contrast is acceptable, or too bright, or too dark. If necessary, the exposure time is then changed in the appropriate direction.

For monochrome cameras, it is quite straightforward to implement such a control function. The histogram of the judgement algorithm and the control logic for monochrome cameras will be presented in this chapter. However, the control algorithm for colour cameras is not so straightforward because the brightness of colour pictures has a different meaning from that of monochrome cameras.

Following the discussion of the monochrome case, we will discuss in detail how to analyse colour pictures to judge the exposure. A new algorithm is then proposed.

3.1.2 Automatic gain control

Under dim lighting conditions exposure tends to be set at maximum and as the image reduces further in intensity the grey level distribution again shifts towards black. Although useful picture content remains, the information may not remain visible on a TV monitor and where A/D conversion is used, useful information may be lost within the quantisation step size. It is common practice to compensate for these effects by providing electronic gain within the output stage to restore the image amplitude. Of course the reduced dynamic range of the dim image is not improved, but the signal becomes more visible on a monitor and more detail is retained in data conversion.

The realization of on-chip automatic gain control is related to two following issues.

1. How to electronically set the gain.

2. How to automatically control the gain setting.

The solution to the first issue is that several load devices, instead of one, are used as a digitally controllable gain stage. These devices operate in their linear regions and form a binary-ratioed series. The total conductance of the load is G.D, where G is the conductance of the smallest device in the binary series and D is the digital word formed by the control bits applied to the series of gates.

For a seven bit load device, a gain setting range of 1 to 128 can be achieved. A detailed circuit for such a digitally controllable gain stage will be described later.

Similar to the exposure control, automatic gain control is achieved by monitoring the image pixel stream and estimating the fractions of each picture which are very white and very black. On the basis of this information, the device decides whether the picture contrast is acceptable, or too bright, or too dark. If necessary, the gain setting is then adjusted in the appropriate direction. We can view AGC function as a extension of AEC function at the dark end although they work on different principles. Actually, the algorithm and control logic of both functions have many common features.

Again, the AGC is more complicated for colour cameras because it is related to *colour balance*, which will be discussed in next chapter. In this chapter we will only be concerned with common gain control, which turns out to be the gain of the green channel; the gain of the red and blue channels is some multiple of this green channel gain.

3.2 Electronic aperture

3.2.1 Integration time of the pixels

The architecture of the MOS image sensor is shown in Figure 6.3. The light sensing area consists of a photodiode array. The line connected to the gate of transistors of a row is called the word line. The line connected to the drain of the transistors of a column is called the bit line. The word line controls pixels in row to be reset, isolated and

sampled. The pixels are reverse charged to a bias voltage when reset. After the pixels have been isolated for some time while being discharged by incident light, the charge left on the photodiodes is sampled along the bit line to capacitors at the top of the array. The time between reset and sample is called the integration time. The electronic aperture can be implemented by a circuit which varies the integration time, i.e., adjust the time interval between sample and reset.

An on-chip electronic aperture, equivalent to eight stops of a mechanical system has been reported before [Asano, 1988]. It uses two vertical shift registers, one for readout (sample) and another for reset (Figure 3.1).

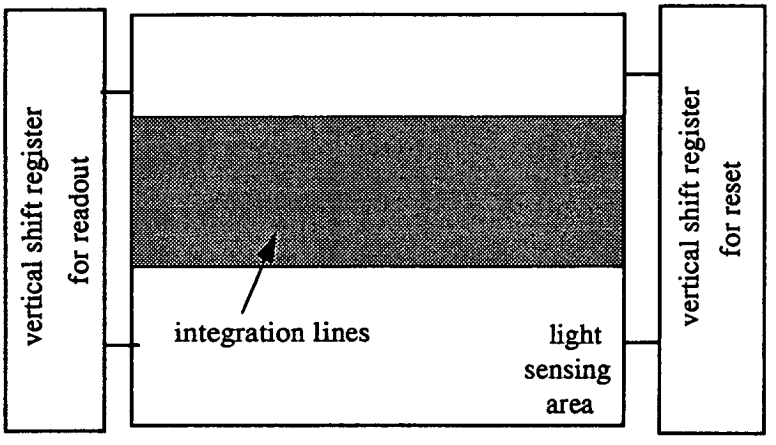

Figure 3.1. A sensor array with two vertical shift registers.

This scheme only allows exposure adjustment on the basis of line time.

A novel scheme [Lu, 1991] has been developed for our designs, which enables exposure adjustment not only on the basis of line time, but also on the pixel time. We refer to the line time adjustment as coarse adjustment and pixel time adjustment as fine

adjustment. This scheme allows a much wider adjustment range. For a shortest integration time of 3 pixel clock periods, the range can be 40,000:1, equivalent to 15 stops of a mechanical system. Another advantage is that with fine adjustment, oscillation will be less likely to happen for automatic exposure control schemes.

Our scheme is to define the integration time T_{int} to be the sum of a variable number m of line intervals plus a variable number n of pixel clock intervals:

$$T_{int} = m \times t_{line} + n \times t_{pclk};$$

where t_{pclk} is the pixel clock and t_{line} is the line period. We refer $m \times t_{line}$ as coarse settlement, and $n \times t_{pclk}$ as fine settlement.

Coarse settlement: Our schemes use a signal FI (input to the vertical shift register) to set integration line numbers as shown in Figure 3.2. The duration of FI defines a consecutive group of lines ahead of the line to be read, which are prohibited from resetting, i.e., they are integrating. The rising edge of FI therefore determines the coarse integration time in line periods, up to the falling edge. Figure 3.2 shows that, at a particular line time, row i is being sampled and then reset, rows i+1 through i+m are integrating and all other rows are being reset during the line period.

The minimum value of the coarse settlement is one line period, but the integration time may be further shortened by the reset pulse: RST.

Fine settlement: Fine settlement is achieved by varying the width of the reset pulse RST, which resets all lines of pixels which are not currently integrating. The starting edge of RST is fixed, the falling edge of RST therefore defines the start of the integration period. The reset time can range between a few pixel clock cycles and nearly one line time. The fine settlement is not important when the coarse number m is big. Only as the coarse number is reduced to zero, does the fine number dominate the exposure.

Fine and coarse settlements may be mixed to allow accurate control of integration time

above one line.

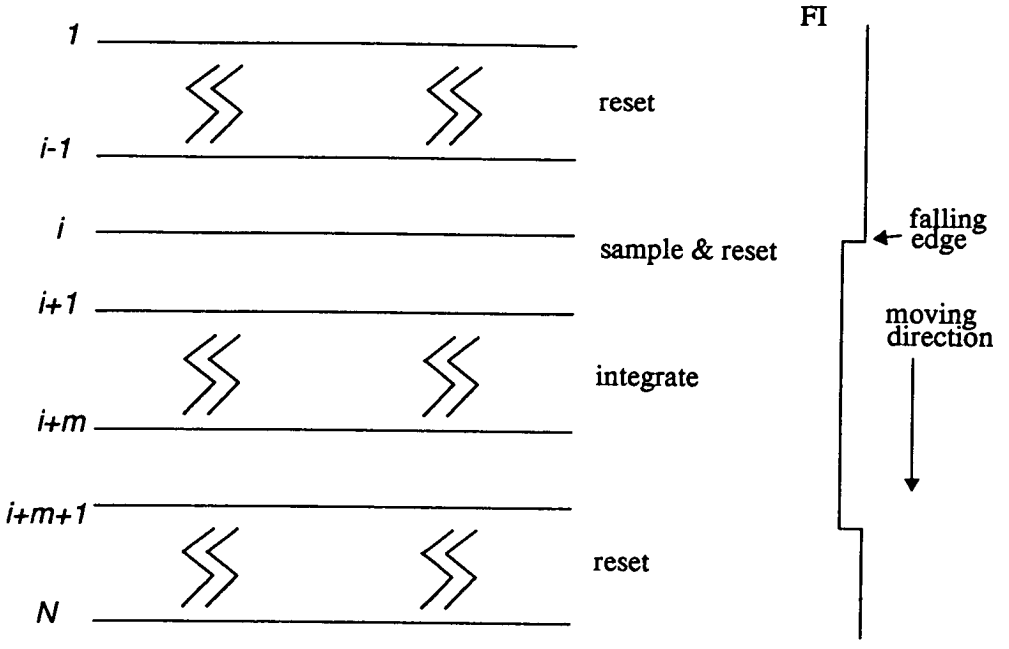

Figure 3.2. Exposure function at each row.

3.2.2 Structure of the electronic aperture

scheme1:

Figure 3.3 shows a cell of the v.s.r. with the decoder attached. The decoder takes d(i+1) and d(i) as inputs with control signals to form a proper operation sequence to sample and reset lines in the sensor array. The coarse exposure is set by the waveform of FI. Its high level represents the integration operation on the lines, and its low level represents the reset operation, while its falling edge represents the sample operation. When FI is shifted in the v.r.s (one bit forward in period of one field, controlled by clock signal cv), it bring these operation to each row sequentially.

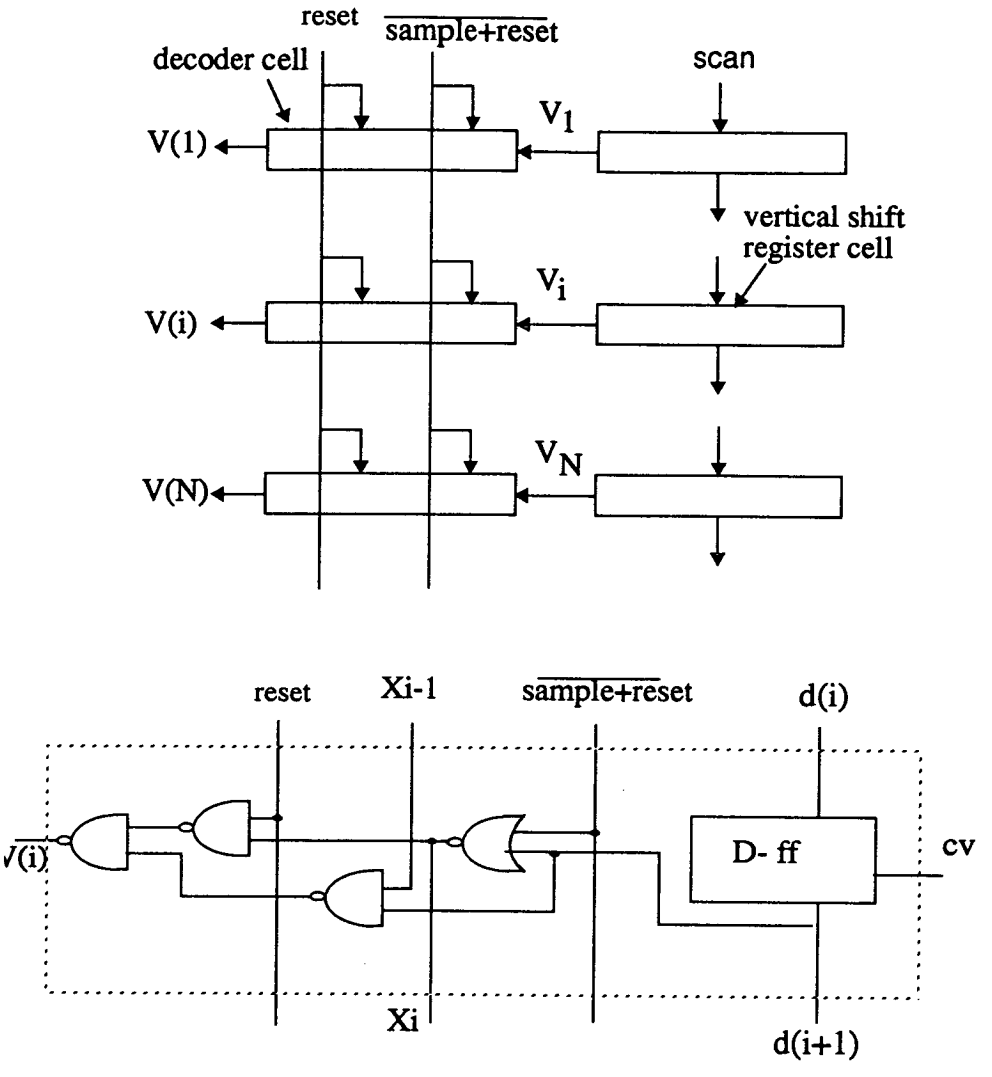

Figure 3.3. Vertical shift register with decoding.

This structure was used in several of our monochrome camera devices. It achieved electronic exposure setting over wide range. However, it had noise breakthrough into the image. When the picture is dark, a variable single bright vertical bar appears. The cause of this bright bar is the turn over of the driving gates of the decode cells. When the lighting condition is bright, the exposure will be in its fine settlement, and all lines

will be reset simultaneously and the reset can finish at any time during line time. When reset finishes (RST's falling edge), all driving gates of the vertical shift register will turn off, causing a voltage drop on the analogue power. This drop will make a particular pixel value lower than other pixels when it goes through the output sensing stage. This is repeated for every line, causing a bright vertical bar.

Scheme 2:

The cure for this vertical bar is to avoid turn over of all driving gates simultaneously at the line time. To do so, only one line (the last reset line, i+m+1, Figure 3.2) is allowed to finish its reset during line time. The reset for all other lines has to continue beyond the line time. Therefore, the turn over of all driving gates will occur during the idle period and will not effect any pixel values. Figure 3.4 shows the new structure. Using this structure the reset current switched by the RESET signal is expected to be reduced to 1/n, where n is the number of lines which need to be reset each time. Thus the vertical bar will not be noticeable in the picture.

This scheme has been used for our CMOS sensors to replace Scheme 1. The first prototype using this method has shown that this scheme has successfully got rid of the bright moving vertical bar, meanwhile achieving the same functions of a electronic aperture as scheme 1.

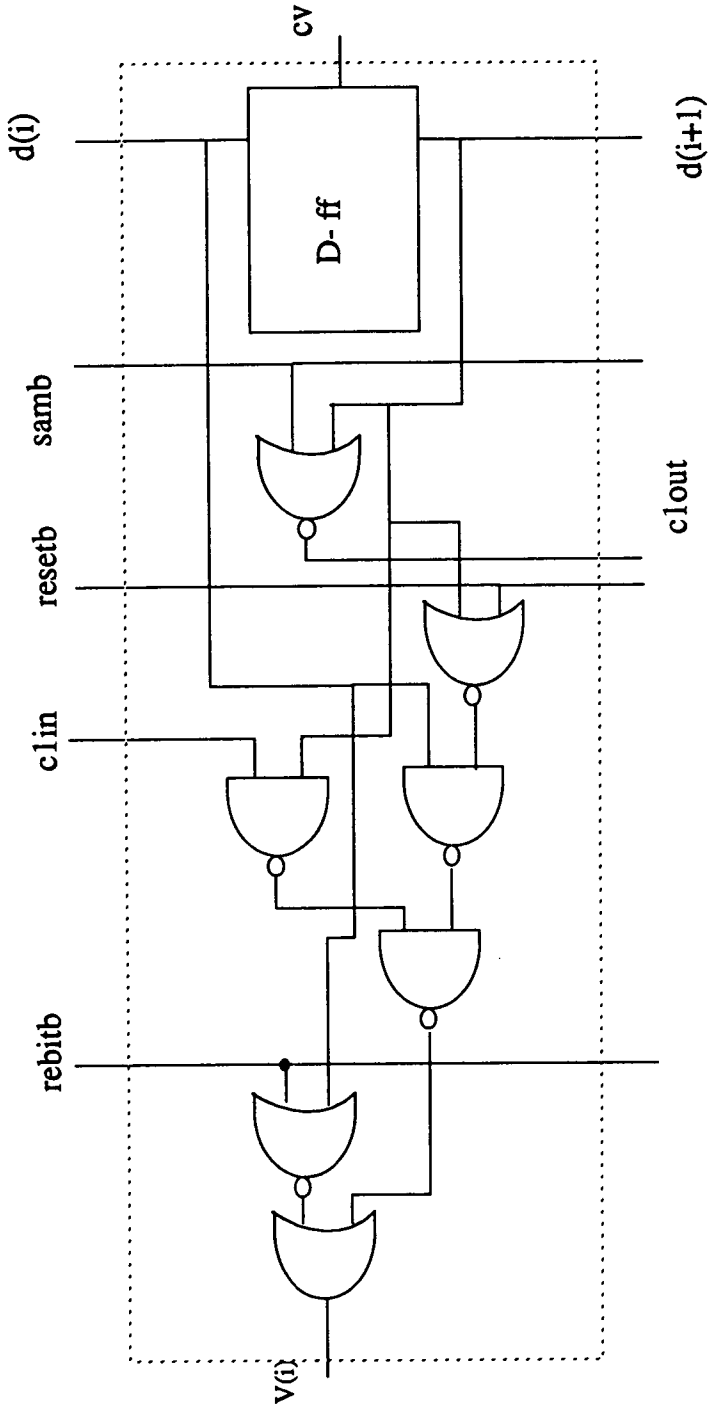

Figure 3.4. The new structure of the vertical shift register with decoding.

3.3 Electronic exposure control

The task of the exposure control is to provide all control signals, such as FI, Sample, and Reset, to set electronic aperture, in response to the live image of the sensor array. Let us consider a monochrome picture first, then extend the concept and method to a colour one.

3.3.1 Exposure control for monochrome pictures

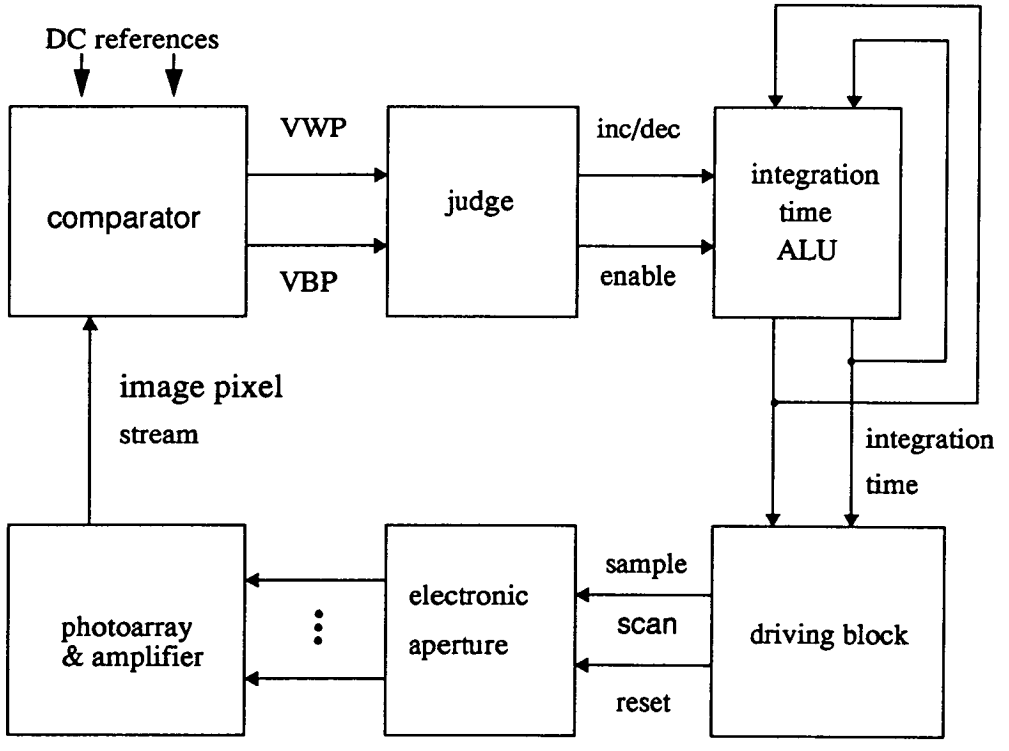

Figure 3.5. Block diagram for the exposure control of monochrome pictures.

Figure 3.5 is a block diagram for the exposure control of monochrome pictures. The image pixel output stream is monitored. Each pixel value is compared with two DC reference levels to pick up "very white pixels"(VWP) and "very black pixels"(VBP). A

very black pixel has its signal below a so called black reference level. A very white pixel has its level above a white reference. These occurrences are counted, and a group thresholds are set to judge the exposure of the current picture.

Figure 3.6 shows a typical histogram of the judgement algorithm based on the numbers of very white pixels and very black pixels. If the numbers fall in the middle area the picture is thought to be well-exposed and the previous exposure setting is kept. If the numbers fall in left side (shaded area marked by increase) the picture is thought to be too dark and then the integration time of pixels for next frame will be increased. On the other hand, if the numbers fall in the right area (shaded area marked by decrease) the picture is thought to be too bright and then the integration time of pixels will be decreased.

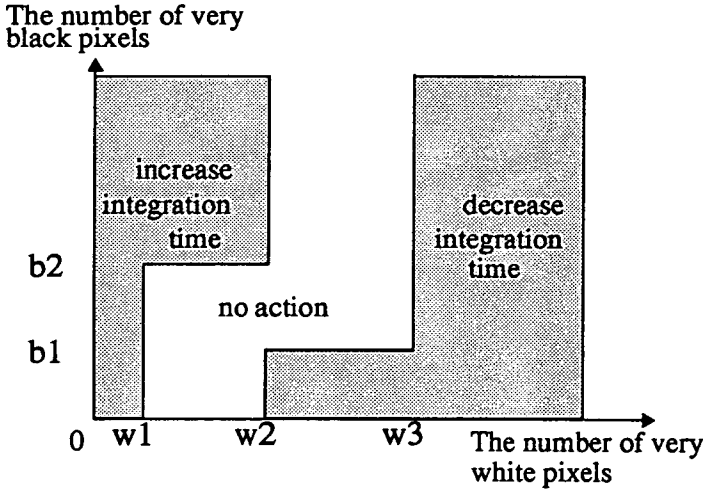

Figure 3.6. The algorithm of the exposure judgement for monochrome pictures.

The new integration time is calculated according to the following formula:

$$T_{new} = T_{pre} \times (1 \pm step) \qquad \text{if exposure is increased/decreased;}$$

$= T_{pre}$ if no action.

where T_{new} is new integration time for the next frame, T_{pre} is the current integration time. The step size could be 25%, 12.5%, or 6.25% according to the convergence speed requirement.

3.3.2 Exposure control for colour pictures

There are three sensing channels, corresponding to three primary colour (Green, red, and blue, or their combination). The exposure setting for each channel should be kept same. The question then is how to judge the exposure. We know that the luminance of a colour picture is decided by three primary colour [Hutson, 1989]:

$$\text{Luminance} = 0.59G + 0.3R + 0.11B$$

Thus, we can derive the luminance from the pixel stream of each channel.

Various strategies for setting exposure can be considered. For example we could only count one channel, say Green, to judge exposure, because Green is the most important colour component in the luminance formula.

Another choice is to count each channel separately and then OR them together. Or we could judge exposure based on the derived luminance.

To compare the above judgement schemes, we analyse several of the main saturated colours, white, yellow, cyan, green, magenta, red, blue, and black, as shown in the following tables. A value of 1 means full scale of the range, i. e. ideal signal amplitude; a value below 1 means under exposure; a value grater than 1 means over exposure.

Table 3.1: RGB and Luminance signal levels in well-exposure condition

right exposure	B	G	R	Luminance	E=OR(B,G,R)
White	1	1	1	1	1
Yellow	0	1	1	0.89	1
Cyan	1	1	0	0.70	1
Green	0	1	0	0.59	1
Magenta	1	0	1	0.41	1
Red	0	0	1	0.3	1
Blue	1	0	0	0.11	1
Black	0	0	0	0.0	0

Table 3.2: RGB and Luminance signal levels in over-exposure condition

over exposure	B	G	R	Luminance	E=OR(B,G,R)
White	1.2	1.2	1.2	1.2	1.2
Yellow	0	1.2	1.2	1.07	1.2
Cyan	1.2	1.2	0	0.84	1.2
Green	0	1.2	0	0.71	1.2
Magenta	1.2	0	1.2	0.49	1.2
Red	0	0	1.2	0.36	1.2
Blue	1.2	0	0	0.13	1.2
Black	0	0	0	0.0	0

Table 3.3: RGB and Luminance signal levels in under-exposure condition

under exposure	B	G	R	Luminance	E=OR(B,G,R)
White	0.8	0.8	0.8	0.8	0.8
Yellow	0	0.8	0.8	0.71	0.8
Cyan	0.8	0.8	0	0.56	0.8
Green	0	0.8	0	0.47	0.8
Magenta	0.8	0	0.8	0.33	0.8

Table 3.3: RGB and Luminance signal levels in under-exposure condition

under exposure	B	G	R	Luminance	E=OR(B,G,R)
Red	0	0	0.8	0.24	0.8
Blue	0.8	0	0	0.09	0.8
Black	0	0	0	0.0	0

From these tables we conclude that:

(1) Exposure monitored via luminance will be incorrect for most colours except white and black. In fact, the luminance level only represents the brightness of a monochrome picture, where all other colours become grey.

(2) Exposure monitored via the green will be correct for some colours, but will be incorrect for images which are predominantly Magenta, Red or Blue.

(3) The expression of E = OR(B, G, R) works well for all colours. E will be greater than 1 for the overexposure of any colour, and will be less than 1 for the under-exposure of any colour.

We can use this expression to judge exposure of pixels. To make the following discussion clear, we will use the terms "colour pixel" and "primary pixels". A "colour pixel" physically consists of three "primary pixels" (such as G, B, and R). The exposure judgement will be based on counting the over-exposed colour pixels and the well-exposed colour-pixels.

1). Compare primary pixels with a common "very bright" threshold(1, in full scale) and label the comparator outputs as gr[3],red[3] and blue[3] respectively. The outputs will be logic 1 if the primary pixel value is greater than the threshold. Combining gr[3],red[3] and blue[3] by an OR gate gives a net judgement, n1, for the colour pixel. The colour pixel is over-exposed if n1 is 1. Count n1's to derive the number of over-exposed colour pixels, N1, in the image.

2). Instead of picking up "very black" pixels as we did for monochrome pictures, we set another threshold level close to the "very bright" threshold level (approximate 0.92). Compare primary pixels with this new common threshold (we refer to it as the "well-exposed" threshold) and let the comparator output be gr[2], red[2], and blue[2]. The outputs will be logic 1 if the primary pixel value is greater than the "well-exposed" threshold. Combine gr[2], red[2], and blue[2] by an OR gate to give a net judgement, n2, for the colour pixel. A colour pixel is judged as well-exposed if its net judgement is that n1=0, n2=1.

To a colour image, we expect a good picture to have colour pixel distribution from black to the "well-exposed" region. If there are no colour pixels in the well exposed region, the picture will be too dark. Arithmetically, the picture is judged as under exposed if the number of well-exposed colour pixels, N2, is less than 1% of the total pixel number, and the exposure will be increased. On the other hand, we should limit the number of over exposed colour pixels. Arithmetically, a colour picture is thought to be over exposed if N1 is bigger than 2% of total pixel number, and the exposure will be decreased.

The thresholds of N1 and N2 are chosen as, respectively, 2% and 1% of the number of all pixels of the image. These values are not very sensitive in certain range, say from 1% to 3%. But from watching on Figure 3.7(b) we would see some potential problems if these thresholds are in wrong places. For example if N2 > N1, it may cause oscillation on some images. If N1 >> N2, it may cause some images over-exposed and less responsive control.

The step size of the exposure increase or decrease is about +/-6.25% of the original exposure value, the same as for the monochrome cameras. The step size is less than the gap of the threshold levels, 8%, between over-exposed and well-exposed. This is necessary to guarantee no oscillation under control of this algorithm. The algorithm of the exposure controller is shown in Figure 3.7.

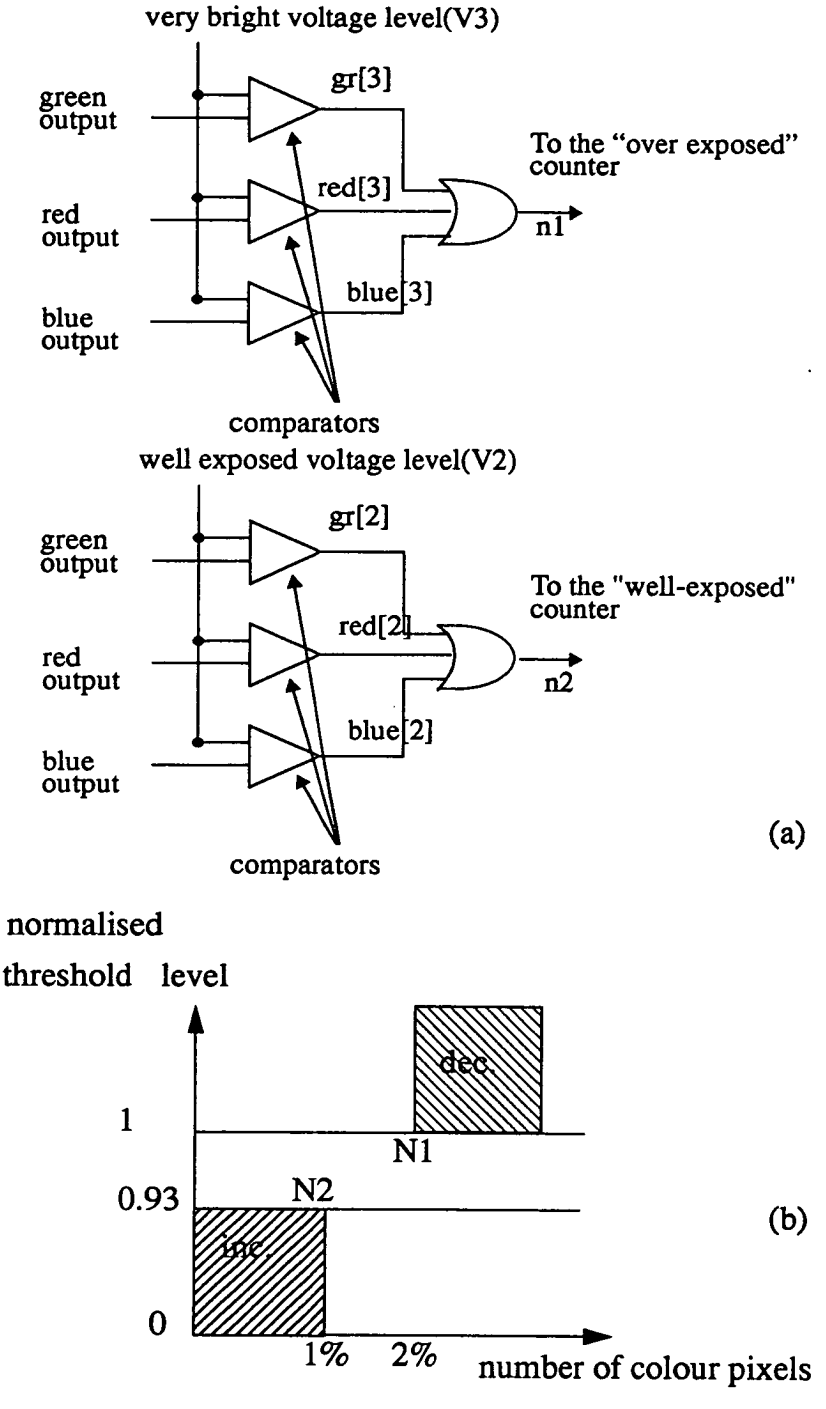

Figure 3.7. (a). The definition of the very bright and well-exposed pixels. (b). Exposure control algorithm for colour pictures.

3.4 Automatic gain controller

Auto gain control is needed when exposure reaches its maximum value. This section describes a controllable gain stage and the principle of such control.

3.4.1 The digital controllable gain stage

A digitally controlled MDAC (Multiplying Digital to Analogue Converter) is shown in Figure 3.8. It has a 7 bit of N-type MOS parallel transistor load. All these transistors work in the linear region and their sizes (ratio of the width to the length, W/L) increase by a factor of 2 in sequence from the least significant bit to the most one to form a binary-ratioed series. The conductance of the load is G.D, where G is the conductance of the least bit transistor in the binary series and D is the digital number applied to the transistors of the load. The input current is then converted into a voltage value (on the node A) that equals to Iv/G.D.

For the gain control purpose, this MDAC is working as a current load, as shown in Figure 3.8. The image signal is first converted to a current through M1. M2 provides a constant current source Imax. Imax is set via a procedure called black level calibration (Section 5.3) so that it equals to the greatest current expected from M1. This ensures the free offset of the black level. For an arbitrary value of Vin, which converts to Iin through M1, the residual current Iv = (Imax - Iin) flows out of this stage, through the load of MDAC to ground. The gain of this stage is adjusted by the 7 bit digital number.

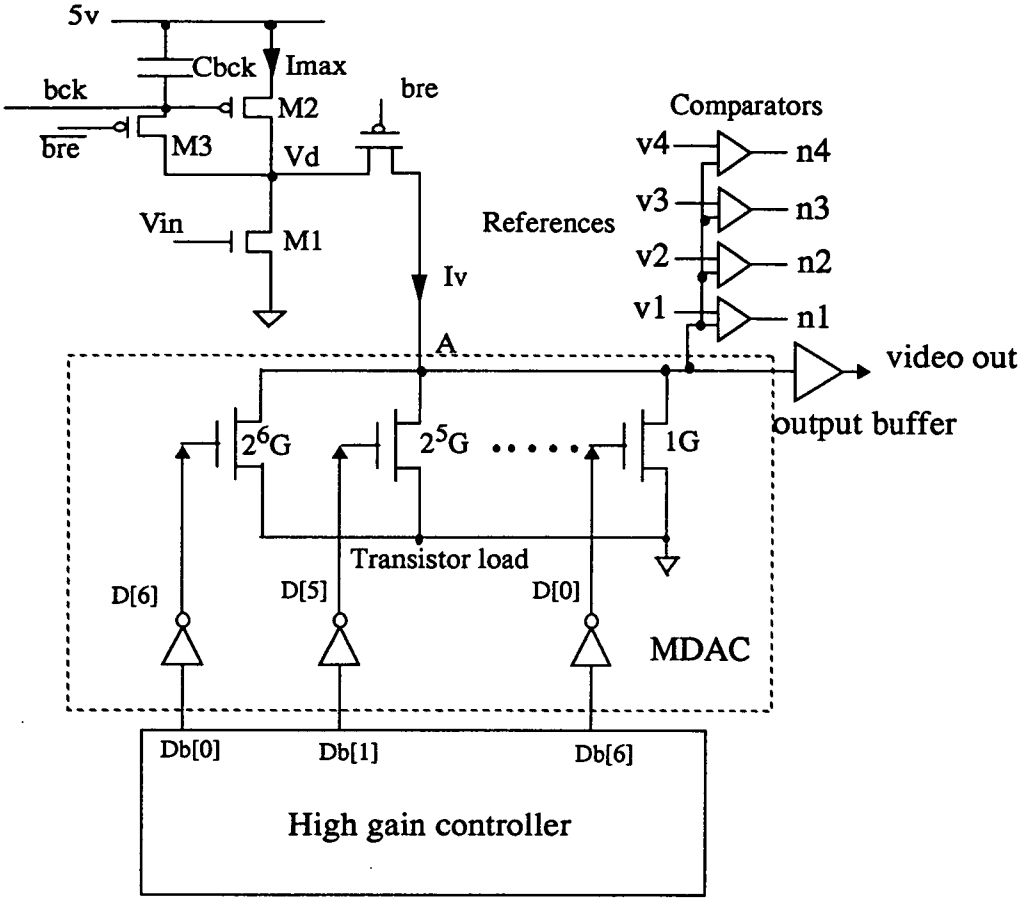

Figure 3.8. Gain setting and comparators circuitry.

3.4.2 Auto-gain control for monochrome cameras

The task of the gain control is to provide the 7 bit digital number to the MDAC, in response to the live image of the sensor array. The block diagram of auto-gain control is shown in Figure 3.9. Let us consider a monochrome picture first, then extend the concept and method to the colour one.

Similar to the exposure control, gain control is implemented by monitoring the image

pixel stream and counting both "very white pixels" and "very black pixels". The device then judges whether the gain is too low, too high, or acceptable. If the gain value is not acceptable, action will be taken to adjust it in the appropriate direction.

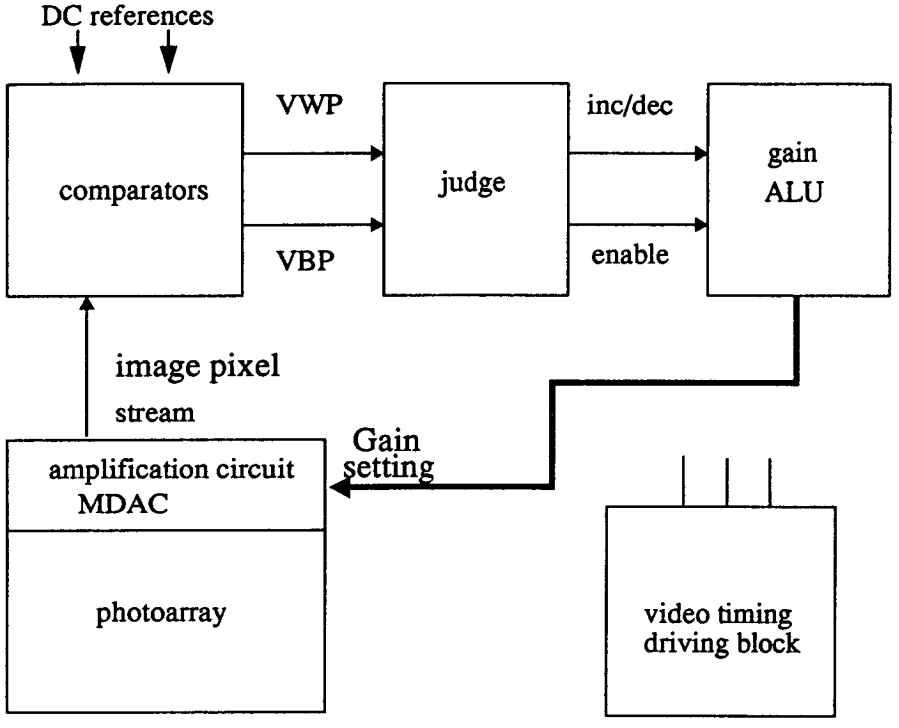

Figure 3.9. The block diagram of auto-gain control.

The new gain setting (7-bit digital number) is calculated according to the following formula:

$$S_{new} = S_{pre} \pm 1 \quad , \qquad \text{if Gain is decreased/increased;}$$

$$= S_{pre} \qquad \text{if no action.}$$

where, S_{new} is new conductance of the load for the next frame, S_{pre} is the present conductance.

Please note that for convenience of calculation, the conductance value is calculated instead of the resistance value. Therefore, there is a non linear relation between the gain and digital number calculated.

The AGC will turn off when gain returns to minimum (or nominal) and the picture is still too bright. Then the sensor will come back to normal AEC mode.

3.4.3 The digitally controllable gain stage for the colour camera

Colour cameras have three amplification channels. Each channel has one MDAC. The question is how to set the gains: Should these MDACs be identical? Should the gain setting for each of the three channels be the same?

The answer to the first question is NO because the optical response, i. e., sensitivity to three primary colours in each channel is quite different.

Factors causing the sensitivity difference are different transparency coefficients of the spectral responses of the colour filters, absorption and wavelength dependence of the silicon substrate, effects of manufacturing variations [Denyer, 1992].

The sensitivity difference should be compensated. It can be done by varying either exposure setting, or gain setting. We choose to vary gain and keep the exposure the same.

The different gain factors can be implemented in various stages from pixel to the output. Then the question is which amplification stage in the sensor is suitable to be given different gains for each channel? We choose to vary gains in the MDAC stages while keep the previous amplifier stages the same. The reason to do so is to keep the black calibration scheme unchanged. The MDAC is the stage following black calibration. The MDAC in the colour channels is designed with the same structure as the monochrome cameras, shown in Figure 3.8, but with different size in the load transistors to give the different gain.

Experiments have been carried out to measure the energy responses of three primary

colours, using a set of assembled filters and lens. The response ratio of R,G,B is 1/1.25: 1: 1/2 [Herry,1993]. Therefore, the ratio of the gain of the R, G, B channels is set to 1.25: 1: 2, realized by varying the sizes of the transistors.

The effective gain setting range of Db[0:6] is from lowest gain 0 (0000000) to highest gain 112(1111000). The lowest gain, Db[0:6] = 0, turns all 7 transistors on, the conductance is 127G. The highest gain could be Db[6:0] = 127(1111111) but the load resistor becomes infinite, thus this number is illegal. As the number, Db[6:0], gets larger, the gain step also increases. This finally leads to too large a gain step to be able to stabilize the output signal. So in practice Db[0:6] is limited to 112, with a conductance of 15G. Therefore the controllable gain range is 18.5dB(= 20log(127G/ 15G)).

Now, we come to the second question: Should the digital gain value settings be the same?

As the required gain difference has been implemented in the different MDACs the answer is yes. We can use same digital number setting for each MDAC. But in response to colour change of live image caused by changing of ambient lights, the digital gain settings could be different. In the following chapter on colour balancing, we will discuss how to control the gain setting to compensate the colour change of live images caused by changing ambient light.

3.5 On chip implementation of AEC/AGC for monochrome sensors

As discussed previously, the AGC will turn on when exposure has reached a maximum and the picture is still too dark. From this point of view, AGC is an extension of AEC, as shown in Figure 3.10, although the high gain does not increase the dynamic range and both functions work on different principles. Therefore, AEC and AGC can be controlled by the same exposure judgement algorithm, as described previously. For on chip implementation, these functions can share most cells, such as the comparators and judgement, as shown in Figure 3.5 & Figure 3.9. We then need a switching procedure

which judges the state of the exposure value and the gain value, and switches between the AEC or the AGC accordingly. Figure 3.11 shows the switching algorithm.

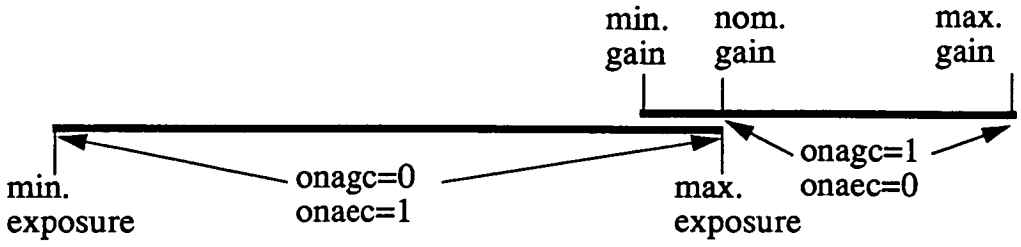

Figure 3.10. AGC is an extension of AEC.

Figure 3.12 shows the block diagram of control circuitry. It consists of comparators, judgement algorithm, switching block, integration time ALU, gain ALU and integration time encoder blocks. The operation sequences are controlled by video timing generator. Each block is described as follows.

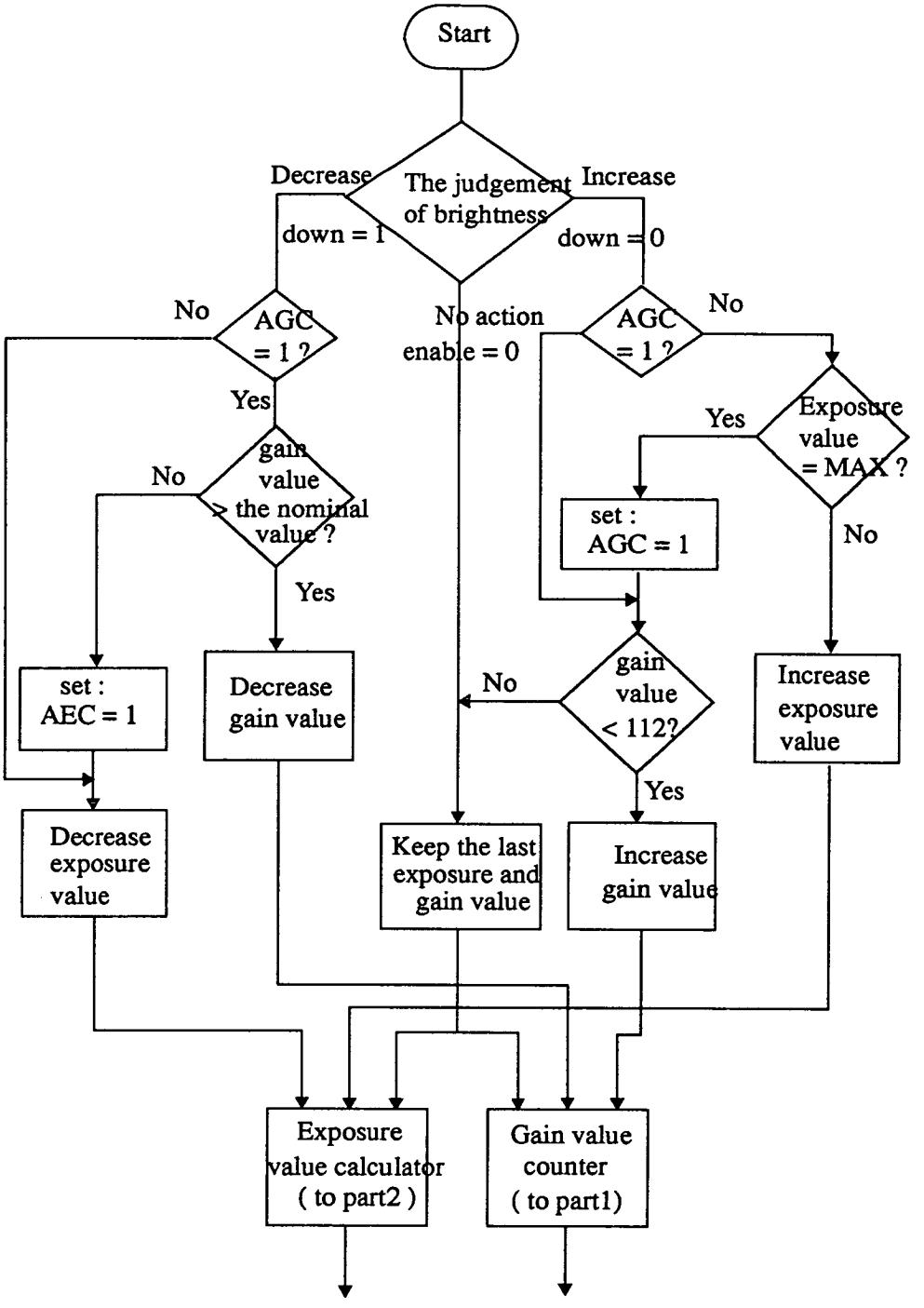

Figure 3.11. The switching algorithm between the auto-exposure and the auto-gain.

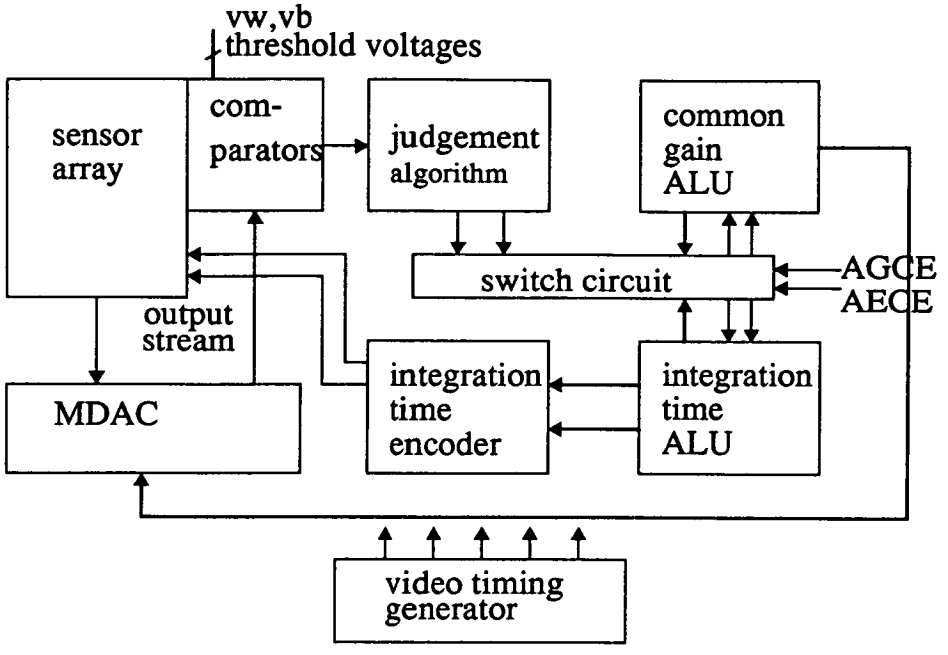

Figure 3.12. The block diagram of the exposure controller and high gain controller of the monochrome camera.

3.5.1 Comparators

There are two comparators which compare the video analogue output pixel stream with two reference voltages, one is called the white reference level, one is called the black reference level. The white reference level is near the top level of the range of video signal, the black reference level is near the bottom level. If a pixel's level is higher than the white level, the output of the white comparator is one, which represents a very white pixel. If the pixel's level is lower than the black level, the output of black comparator is one, which represents a very black pixel.

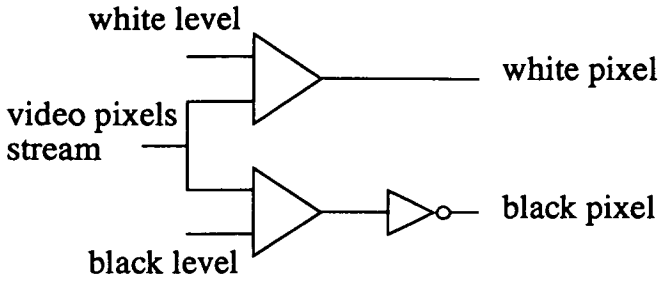

Figure 3.13. Comparators.

3.5.2 Exposure algorithm block

This block consists of two counters, one counts the number of the very black pixels, one counts the number of very white pixels. When one field scan finishes, the number of the white and black pixels are loaded into the judgement circuit, which finally sends two signals: enable and down/up.

The counters sample very white and very black pixels on PV's rising edge. When the state of the w1, w2 or w3, b1 or b2 is changed, this means the number is over the threshold settings as shown in Figure 3.6. An RS-ff latches the state and keep it until the next FS (field start) signal comes to reset it. The judgement decision is an implementation of the algorithm in Figure 3.6.

Enable=1 indicates that the exposure/gain data should increase or decrease, Down/up=1 decreases the exposure/gain data from the previous value, Down/up=0 increases the exposure/gain data. Enable=0 indicates that the exposure/gain data should keep unchanged from the previous value.

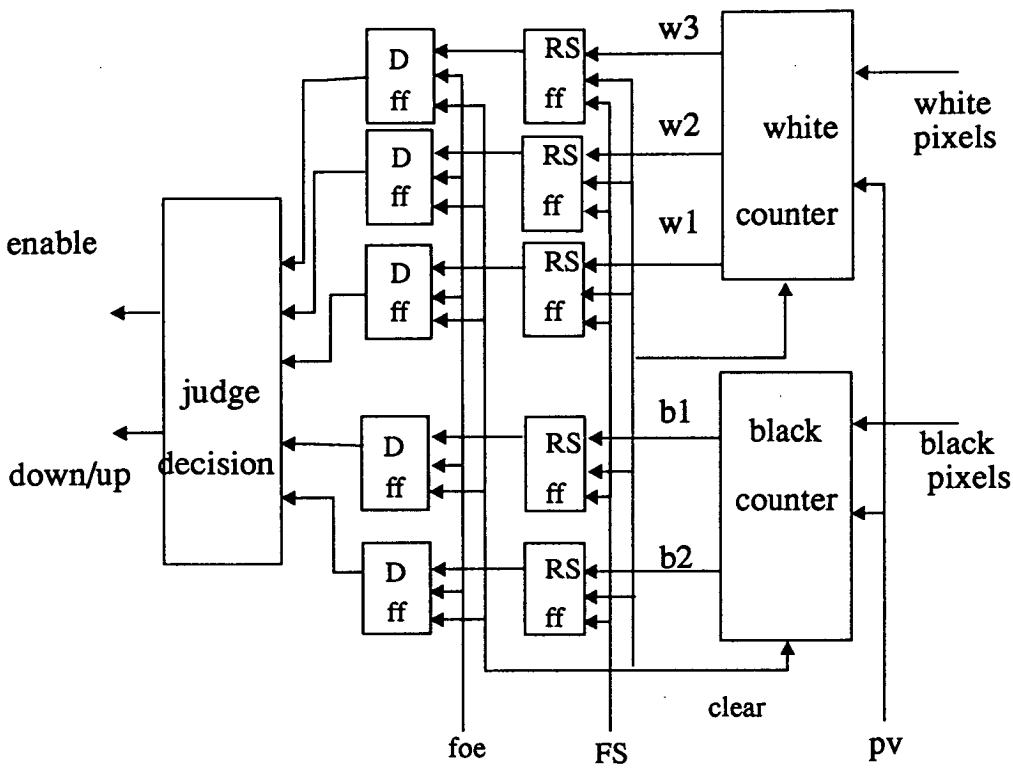

Figure 3.14. The block diagram of the exposure judgement.

3.5.3 Integration time ALU

The integration time ALU block consists of a 20 bit adder/ subtracter, registers, a times three multiplier and some decoders. We use fixed-point arithmetic circuits in the design of the calculation of the integration time. The block diagram is shown in Figure 3.15.

This block works at frame rate and always uses the previous integration time as a reference value from which to form the new one. The previous values are stored in the registers, and feed back directly to the input a[19:0], and to the input b[19:0] by shifting right by 4bit to form the step size, 1/16th of the previous value. One difficulty existed originally in the calculation was how to deal with the carry from the fine (exp[8:0]) to the coarse number (exp[17:9]). The number 384 in the fine data equals one in the coarse data. Because 384 is not a power of 2, we could not simply put the two numbers

calculated together.

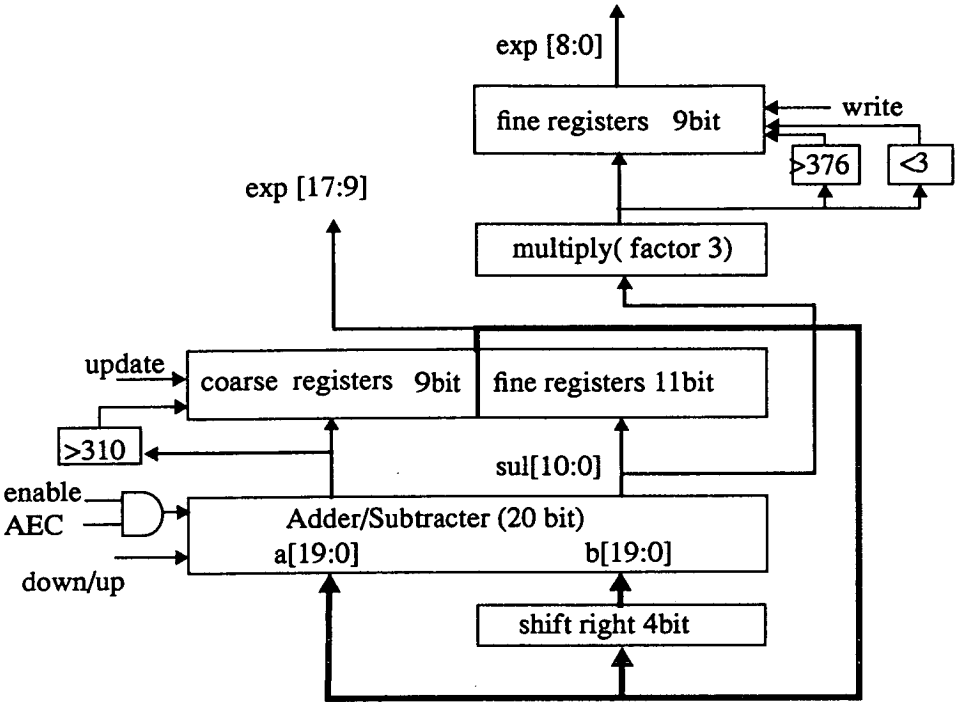

Figure 3.15. The logic structure of the integration time ALU.

To solve this problem, instead of using 384 we use 128 (2^7) as a carry between the fine and coarse number at the adder/sub stage, and then the output of the fine one is finally formed by multiplying by 3. Before the number is written to the fine register, the range of the number is further clamped to 3 - 376 according to the operation sequence of the sensor array. There are two decoders to detect the number overflowing out of this range, and then resetting the number in the range before it is written into the registers. This is a smart solution to convert a non base 2 arithmetic function back to base 2 arithmetic.

Another decoder is used to monitor the coarse number going out of the range(>310) and clamp it to 310 in the coarse register.

3.5.4 Gain value ALU

Figure 3.16 shows the diagram of the auto-gain controller logic block. This part consists of a nominal value register, an up-down counter, decoders and some control gates.

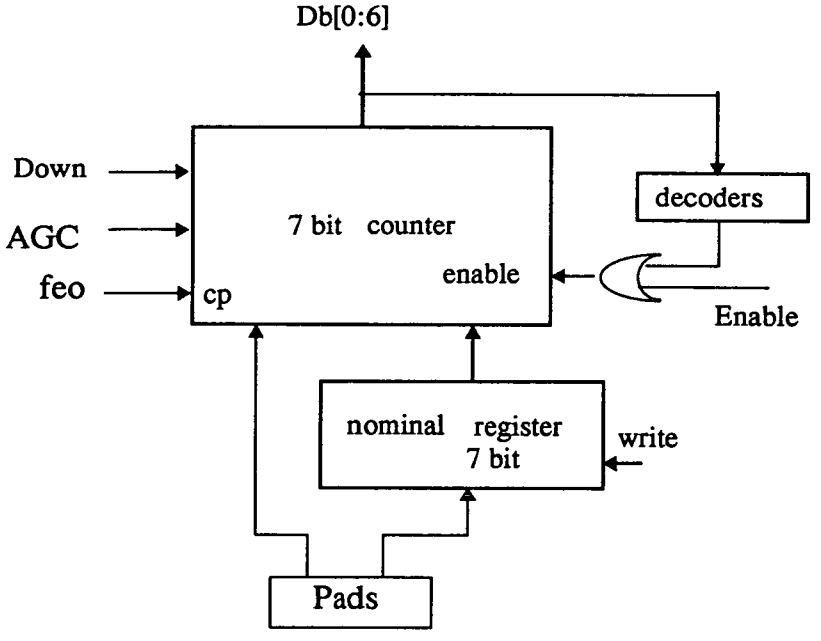

Figure 3.16. The gain value ALU block.

A 7 bit nominal register is used to store the nominal gain value, its default value is sets to 24 internally. If the internal nominal gain value does not provide a suitable gain to the MDAC stage in normal lighting conditions, a new nominal gain can be set externally through pads.

The 7 bit up-down counter is used for providing the gain value, the step size is +/-1 for every increment or decrement action. It is controlled by the two signals, Down/up and Enable. The Enable signal is used to increase/decrease the gain when the data is out of range or disable increase/decrease when no action is needed according to the exposure judgement or AGC function inhibition. The range of the gain value Db[6:0] is from the

nominal to 120 (maximum).

In good light conditions before the integration time reaches maximum the counter always loads the gain value from the nominal register. When a higher gain is needed in dim lighting conditions, the number in the counter goes up until the exposure judgement indicates no further action. The number can go down if the light condition becomes better.

3.6 On chip implementation of AEC/AGC for colour cameras

Three terms are defined below before discussion:

- Nominal gain: a nominal gain is a gain setting of MDAC at initialization and remains so for normally good lighting before the AGC turns on. Please note that nominal gains are different for the three channels although the nominal settings are the same.

- Common gain: a common gain is the gain value controlled by the AEC/AGC controller, which could be the nominal gain (before AGC turns on) or a higher gain value (after AGC turns on).

- Offset gain values: an offset gain value is the difference between either the red or blue channels and the green channel. The offset gain value is controlled by the colour balance controller according to its judgement to weight the RGB signals.

- Real gain value: the real gain of the green channel is the same as its common gain value. The real gains of the red and blue channels are the sums of the common gain and the offset gain value.

As with monochrome cameras, the AGC is an extension of AEC (Figure 3.10). The switch algorithm is the same as shown in Figure 3.11. Both functions will also share most circuitry.

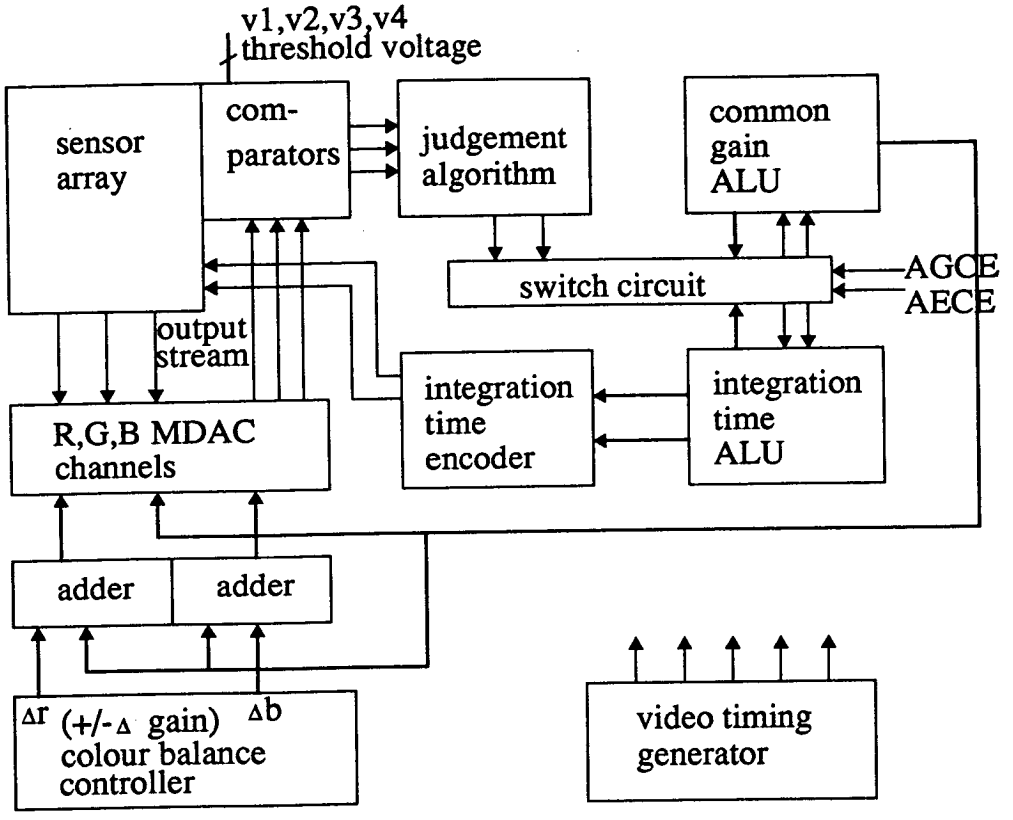

Figure 3.17. The block diagram of the exposure controller and high gain controller of colour cameras.

The AEC and AGC block diagram for colour cameras is shown in Figure 3.17. It consists of an judgement block, an integration time ALU block, an integration time encoder block and a common gain ALU block. It takes the pixel stream of the image signals from the sensor array, through the comparators, the analogue image signals become desired digital signals. The digital signals are processed in the judgement block, which indicates the direction of the integration time changing or the common gain changing. The integration time ALU and the gain ALU provide proper values for the sensor array.

The common gain value is sent only directly to the green channel's MDAC. The red

and the blue channels's gain are the sums of the common gain and the compensation gain which could be a positive negative or zero value under the control of the colour balance circuitry. AECE and AGCE are external enable signals to inhabit AEC and AGC functions.

3.6.1 Comparators

The comparator structure is shown in Figure 3.7(a). Every channel has two comparators, one is called the very bright comparator, the other is called the well exposed comparator. An OR gate combines the outputs of gr[3], red[3], blue[3] into n1, whose state "1" represents an over-exposed colour pixel. Another OR gate combines the outputs of gr[2], red[2], blue[2] into n2, whose state "1" represents a well-exposed colour pixel.

3.6.2 Exposure judgement

The exposure judgement block takes the two outputs combined by ORing the outputs of the comparators. Two pixel number counters, record the pixel numbers over-exposed and well-exposed, N1 and N2, respectively. The RS-ffs latch the states of N1 and N2 if their state changes to one. At the end of each field, the FOE signal loads the counting results into D-ffs, then the new judgement results are available on nodes Enable and Down/up.

Since the judgement block did not indicate which of, the integration time ALU or the gain ALU should change its value for the next frame, we build a switch state machine according to the switching algorithm in Figure 3.10 to indicate the working procedure.

Figure 3.19 gives the truth table of enable and down vs. N1 & N2.

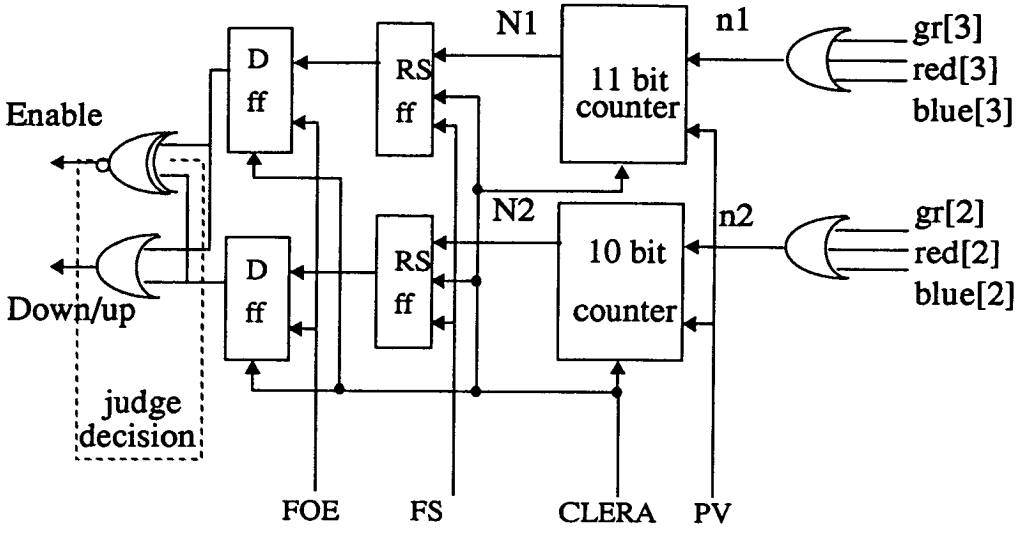

Figure 3.18. The block diagram of the exposure judgement for the colour camera.

N2 \ N1	0	1
0	1	x
1	0	1

enable

N2 \ N1	0	1
0	0	x
1	x	1

down

Figure 3.19. The truth table of the exposure judgement.

3.6.3 Integration time ALU

The structure of the integration time is the same as used in the monochrome cameras, but the figures are different because the video standard is NTSC for colour, CCIR for monochrome.

The range of the coarse number of the integration time is 0 - 260. The range of the fine figure is 37-356.

Another difference in the blocks is that the data can be user over written. In the colour implementation the AEC function can be inhibited through the I^2C interface, the integration time can then be read out and altered to an external setting through the bus line and I^2C interface.

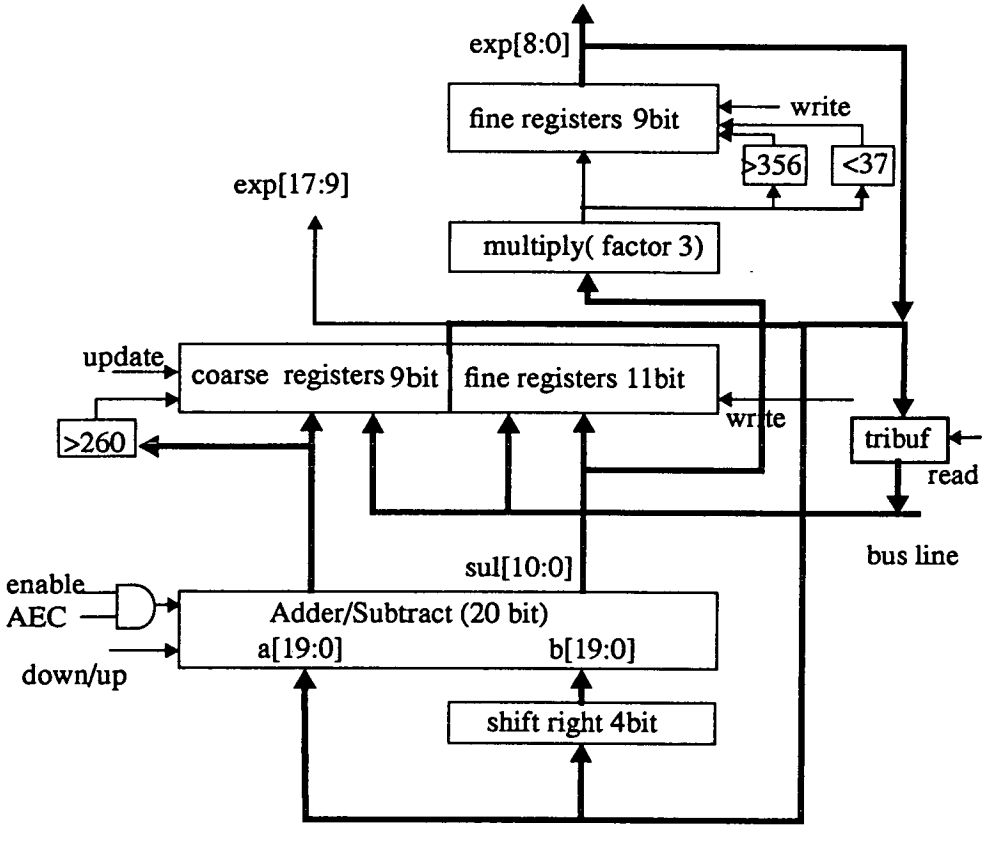

Figure 3.20. The logic structure of the integration time ALU.

3.6.4 Common gain ALU

The structure of the common gain ALU is the same as the gain ALU in the monochrome camera. The range of common gain is from the nominal value to 112. The nominal value is set to 80, near to the mid value of the common gain range, in order to give a

symmetrical range for the red and blue offset values to increment or decrement. The maximum gain is set to 112 because we want to limit the step change to less 6.5%.

The auto gain function can be inhibited and the gain value can be written in and read out through the bus line and the I^2C interface.

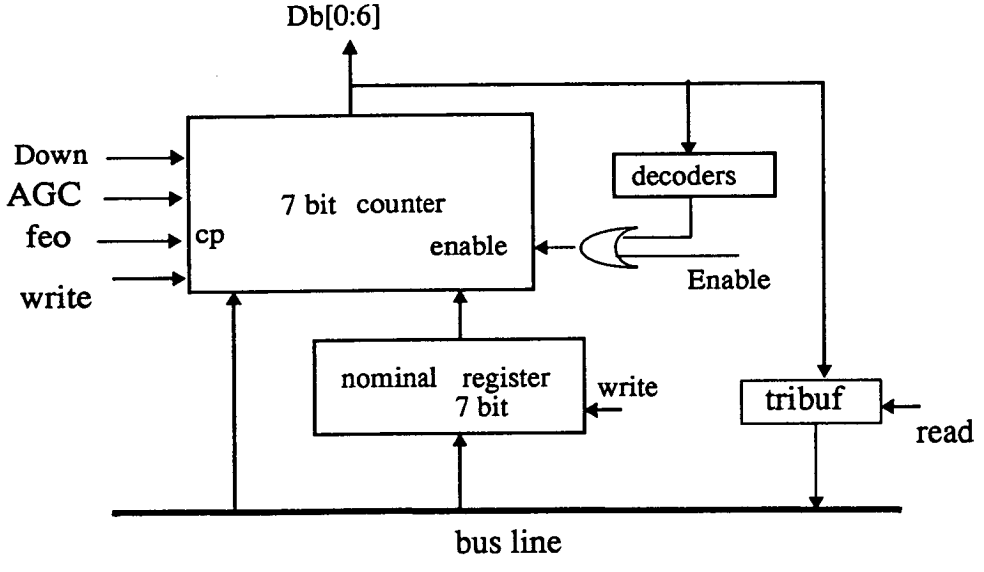

Figure 3.21. The gain value ALU block.

3.7 Chapter summary

The details of the electronic aperture, and the digitally controllable gain stage, as well as their automatic controllers have been described in this chapter, giving the control concept, the algorithm, and the circuit structure to implement the logic. Both monochrome and colour cases are covered. A special character of the controllers is that they are implemented using purely electronic circuits on the chip with the CMOS sensor.

For colour, there is a further requirement to control the gain setting to compensate the colour change of live images caused by changing ambient light. This can be combined with AGC for each channel and will be covered in the following chapter.

Chapter4 Colour Balance Control

4.1 Introduction

In TV or for monitor display systems the additive principle of trichromatic colour reproduction is used, the colour picture is reproduced by mixing RGB signals according fixed rules. In the camera colour the fidelity of images is controlled by weighting the R,G,B signals. Theoretically and practically, colour pictures taken by cameras should be balanced. Colour balance means that the R, G, B primary signals have equal energy levels in any grey scenes from black to white, which makes colour cameras behave in a similar way to human eye and brain function, and of being tolerant to changing light conditions.

In general this approach is called colour balance control. Modern commercial colour cameras use automatic white balance (AWB) to implement colour balance control. AWB uses a separate sensor containing relative few pixels which receives diffused light direct from a standard white object so as to provide a white image. This is the method which is widely and successfully used in modern video cameras.

This method does however have the disadvantages of requiring a separate additional sensor, a white object and the associated analogue signal processing to transfer colour balance information to the main image sensor. This results in additional manufacturing complexity and cost.

In contrast to this approach, a novel colour balance technique has been developed to avoid and minimize the disadvantages of the conventional method of the colour balance control. Instead of obtaining colour information from a separate sensor, the technique uses the colour information from the main sensor array. Instead of analogue signal processing, the technique uses a pure digital signal processing method. Therefore it is possible for it to be integrated with the main sensor array on the same chip substrate.

To present this new technique, the general colour science of TV display systems is reviewed first in Section 4.2 - 4.4. Colour matching colour coordinates systems, effects

on colour reproduction, and commodity colour balance techniques are discussed. This provides background knowledge relating to colour balance.

Section 4.5 describes the details of our colour balance technique. This digital technique not only compensates for variation of colour illuminance of the ambient light, covering colour temperature of light sources over a wide range, but also automatically accommodates systematic and manufacturing imbalance in the three channels.

The colour balance technique is suitable for integration. In Section 4.6, on chip implementation of the colour balance controller with design details is described. This controller only costs 2,500 logic gates.

4.2 Colour matching and coordinates for television system

H. Grassman set up eight colour matching rules [Sun,1984, Jain, 1989, Sproson, 1983], which lay the foundation of colour measurement and is called Grassman's Law. Here we list three of these rules related closely to our subject:

(1). Any colour can be matched by mixing at most three coloured lights.

$$C(c) = M(m) + N(n) + P(p).$$

where C(c) is any colour, '+' means additive mixing, M(m), N(n), and P(p) represent three primary light sources.

(2). The luminance of a colour mixture is equal to the sum of the luminance of its components.

(3). A colour match at one luminance level holds over a wide range of luminance values.

According to rule (1) any colour can be described in colour coordinates, by using three primary lights as attributes. By means of colour coordinates colour definition and calculation become clear and quantitative.

4.2.1 Colour coordinates

Several colour coordinate systems for colour calculations have been proposed, for example C.I.E RGB, C.I.E. XYZ, NTSC RGB, NTSC IQY, PAL RGB, etc. Of these colour coordinate systems, we are specially interested in C.I.E. RGB, C.I.E. XYZ, NTSC RGB, and PAL RGB systems.

Each of the systems chooses its own primaries and, therefore has its own colour matching curves. C.I.E. (Commission International d'Eclairage) established standards for tri-colour matching and calculation in 1931, which are called C.I.E RGB and XYZ [Grum, 1980]. NTSC and PAL systems were developed for TV display.

4.2.2 C.I.E. RGB and XYZ

C.I.E. chooses three monochromatic primary stimuli in the RGB system: P1, red = 700nm; P2, green= 546.1nm; P3, blue=435.8nm. Reference white has a flat spectrum over the visible wavelength band, and the RGB energy equal each other under white light. The spectral matching curves are shown in Figure 4.1. There is a negative lobe on the red curve. This means some colours can not be obtained by additive mixture of this red, green and blue. If, however, the red primary is added to the colour in suitable quantity, it is then found to be possible to match this in slightly desaturated colour with a mixture of primaries blue and green. Negative light flux of course is physical impossible, but fortunately using a matrix transfer equation we can easily generate a negative lobe in the matching curve of RGB [Sproson, 1983; Hunt,1987].

No practical set of three primaries has been found that can produce all colours, some negative value is inevitable on the matching curve of the primaries. However in order to have a convenient coordinate system for colour calculation, the C.I.E. XYZ system has been developed in which the matching value of special tristimuli are all positive, here XYZ are not practical primaries.

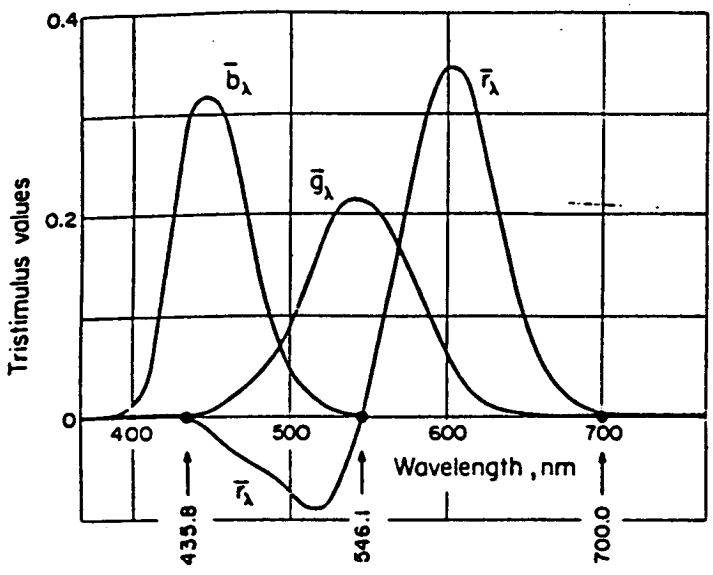

Figure 4.1. Spectral matching curves of CIE RGB.

The three primaries in colour coordinates are not independent because the three have equal energy under the standard white. Therefore three dimensional colour coordinates can be projected on a plane. This is called a chromaticity diagram. Figure 4.2 shows the chromaticity diagram of the C.I.E. XYZ coordinate system [Sproson, 1983]. The tongue shape is called colour gamut area.

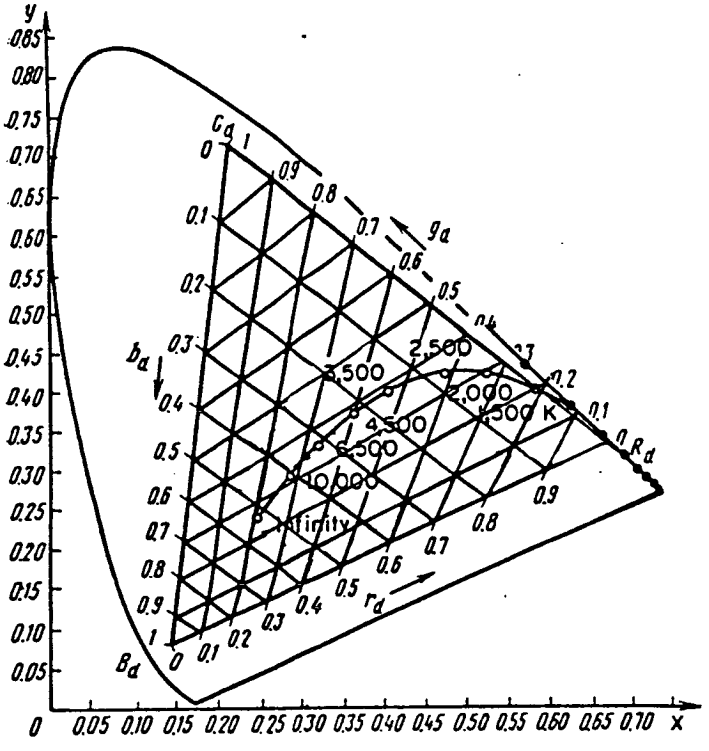

Figure 4.2. The chromaticity diagram of the C.I.E. XYZ colour coordinates system [Sproson, 1983] and a grid of trilinear coordinates for NTSC receiver primaries [Novakovsky, 1975].

4.2.3 NTSC RGB and PAL RGB

These two systems have been developed for NTSC and PAL television receivers. NTSC has adopted three phosphor primaries that glow in the red, green and blue band of the visible spectrum. The reference white was chosen as the illuminance C or D65 (day light at the temperature of 6500K) for which RGB energy equal each other. The grid of trilinear coordinates in Figure 4.2 expresses the colour gamut area of NTSC RGB systems, using the reference white of illuminant D65 [Novakovsky, 1975]. PAL

RGB has its phosphor primaries and matching curves slightly different from those of NTSC RGB [Hunt,1987].

4.3 Effects on colour reproduction

To achieve colour fidelity in the colour camera, we need to consider all processes involved, from optical component to silicon technology, which will have some effects on colour reproduction. According to experiment and analysis there are three major processes: the colour filter, the silicon opt-electronic properties from the manufacturing processes, and the ambient light condition.

4.3.1 Colour filter

It is most important that colour cameras have good quality colour filters, as they directly affect the spectral response of the camera, and colour reproduction.

The filter should have the following characteristics:

(1). High transmission over its transparent spectrum band and a very low transmission over other parts of the spectrum.

(2). The response curve shape of filters should match as closely as possible those of the NTSC/PAL receiver primary phosphorus.

(3). The filters should be very reliable and not fade away with time & exposure to strong light.

Multilayer dielectric filters have the best characteristics to meet the requirements of colour cameras [Sproson, 1983]. Our experiment [Henry,1992] shows the response spectrum curves of the filters, which are produced by OCLI. The filters are suitable for both NTSC and PAL system colour cameras, if cameras analysis is confined to only positive responses.

4.3.2 Silicon spectral response

The silicon spectral response characteristic is related to the electrical properties of the silicon substrate material and the manufacturing technology.

Silicon is responsive to radiation around the visible region of the electromagnetic spectrum. It covers the spectrum response of the human eye but is wider and higher at the long wavelength end. The spectrum response of the human eye and that of ASIS-1011 are shown in Figure 4.3 and Figure 4.4.

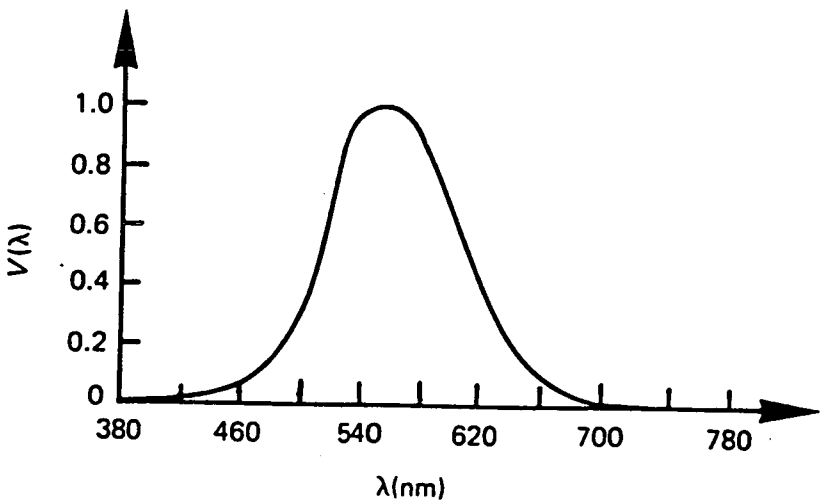

Figure 4.3. The spectrum response of human eye.

The photodiode is a PN junction diode, to which a reverse-bias voltage is applied to generate a depletion region stretching across two sides of the physical PN junction. Under incident light photons with sufficient energy stimulate electron-hole generation in the silicon. Then electrons and holes in the depletion region drift to two sides of the region under the influence of the electric field. In the area of neutral N and P the generated electrons and holes will diffuse from a higher density area to a lower density area.

Light is absorbed along the depth of the silicon substrate. The energy remaining at distance X is:

$$E = e^{-cx}$$

C is absorption coefficient which is related to the wavelength of incident light [Sze,1981]. Short wavelength light has a large value C, so the radiation is absorbed very near the surface where the recombination time of electron and hole is short. The electrons and holes thus can recombine before they are collected in the PN junction. Long wavelength light has a low value of C so the radiation is absorbed at a relatively longer distance but the longer the wavelength, the lower energy of the photon. Photons with energy less than 1.1ev will not generate electron hole pairs in silicon.

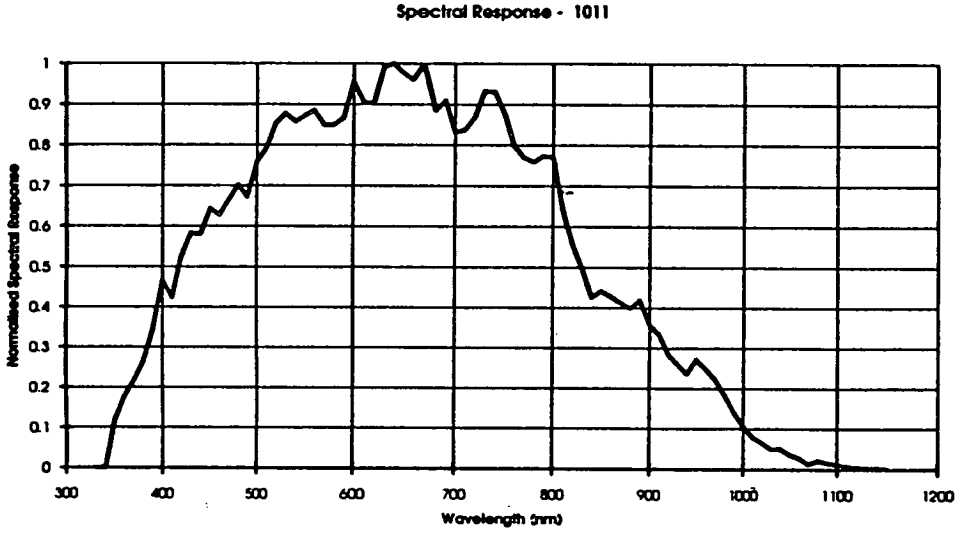

Figure 4.4. Spectral response of CMOS sensor of ASIS-1011 device.

Figure 4.4 shows the measured spectral response of CMOS sensor of ASIS-1011 using 1.5μm technology. For colour cameras the worst feature of the spectral response is the attenuation over the blue region of the spectrum, from 400-500 nm. This may be improved by using a process with a shallower junction depth.

4.3.3 Light sources

There are three kinds of light source that are widely used. One is Tungsten lamps which are referred to as warm light. One is daylight which is the most colorful light source. The other is fluorescent lamps which are referred to as cold light. The different light sources have different spectral power distribution shapes, which severely affect the energy distribution of the RGB signals, and therefore colour reproduction.

4.3.3.1 Tungsten lamps

Figure 4.5 shows the spectral power distribution of tungsten lamps.The spectral power distribution is higher at long wavelengths and lower at short wavelengths. The character of the power distribution of the light sources can be described using colour temperature [Hunt, 1987]. The spectral power distribution of tungsten lamps is nearly identical to that of full radiators. The colour temperature of tungsten filament lamps lie in a range from 2500K - 3400K for commonly used lamps.

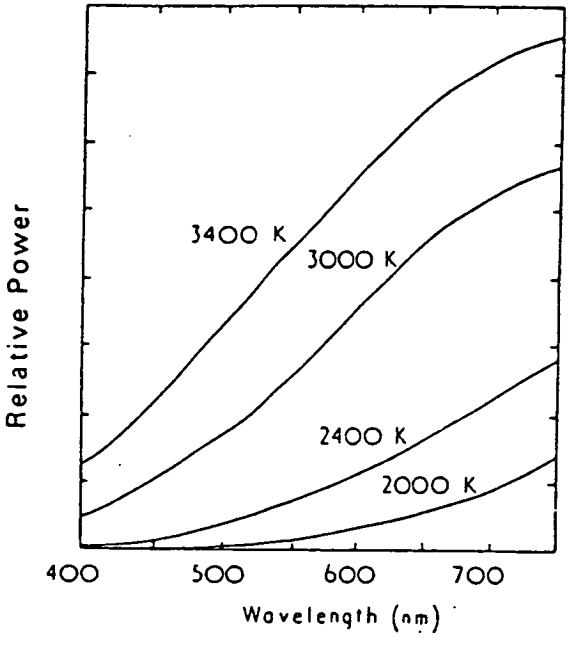

Figure 4.5. The spectral power distribution of tungsten lamps [Hunt, 1987].

4.3.3.2. Daylight

Figure 4.6 shows some spectral power distributions for daylight conditions. Daylight is the most important and the most variable and colourful light source. The spectral distribution of day light is a considerable departure from that of full black body radiation because the light passes through the atmospheres of both the sun and the earth, which are neither neutral nor constant in their spectral absorption. A term called correlated colour temperature is used to describe the colour of daylight. Standardized spectral power distribution curves have been drawn up by the CIE to represent daylight for correlated colour temperatures from 4000 to 25000K [Hunt, 1987], and are known as Standard Illumination D, in which D65 is used as a standard light source in TV systems.

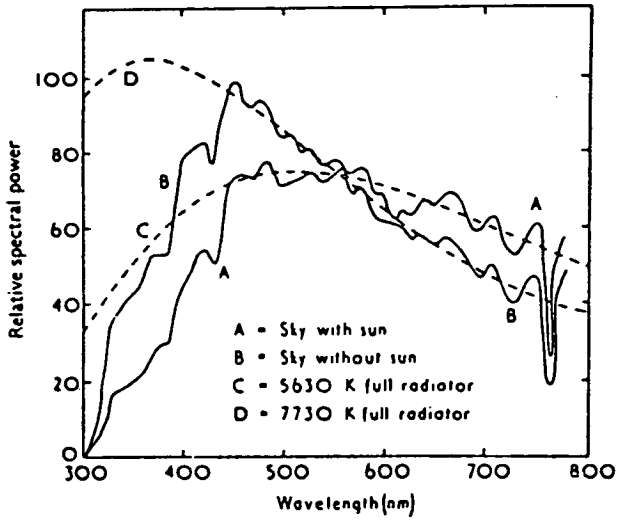

Figure 4.6. Some spectral power distributions of daylight conditions [Hunt,1987].

4.3.3.3. Fluorescent lamps

Fluorescent lamps have spectral power distributions that are mixtures of those of various fluorescent powders and that of the mercury vapour spectrum. Figure 4.7 shows some examples. The spectral power distribution of the fluorescent lamps is also considerable departure from that of full black body radiation. The illuminance colour

of fluorescent lamps can be described by correlated colour temperature.

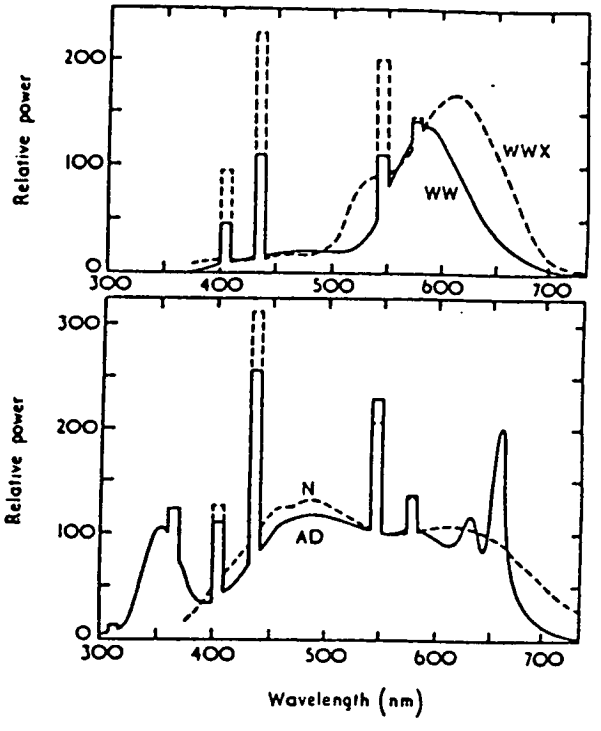

Figure 4.7. The spectral power distributions of fluorescent lamps [Hunt, 1987].

4.3.3.4. The colour temperature of light sources

Figure 4.2 shows the chromaticity of full radiators lying along a curve in the CIE 1931 x, y chromaticity diagram. This figure shows that the green component in full radiators has relatively stable power distribution with change of colour temperature of the light source over wide range. The red component decreases with increasing colour temperature. The blue component increases with increasing colour temperature.

The spectral power distribution of light sources (Figure 4.6 and 4.7) shows quite a big difference from that of full radiators, but the chromaticity of the correlated colour

temperature and colour temperature of full radiators is quite close [Hunt,1987]. So the full colour temperature line can be used, approximately, to represent the chromaticity of light sources.

Table 4.1 gives the energy levels of RGB after normalizing the green to one at the colour temperature 6500K. R, G and B levels are read from Figure 4.2. G*, R* and B* values are normalised from G, R and B respectively. When the colour temperature of the ambient light sources deviates from 6500K, the ratios of the red to the green, and the blue to the green deviate as well. However, the stable energy level of the green component is a very useful feature. We make use of this to develop a new colour balance technique.

Table 4.1. Energy levels of RGB against light source colour temperature deviation from D65.

	2500	3500	4500	5500	6500	7500	9000	10000
G	0.34	0.36	0.36	0.35	0.33	0.34	0.33	0.32
R	0.58	0.47	0.40	0.36	0.33	0.31	0.29	0.28
B	0.08	0.15	0.23	0.28	0.33	0.35	0.38	0.40
G*	1.03	1.09	1.09	1.06	1.00	1.03	1.00	0.97
R*	1.76	1.42	1.21	1.09	1.00	0.94	0.88	0.85
B*	0.24	0.45	0.70	0.93	1.00	1.06	1.15	1.23

4.3.4 Summary of the effects

Summarizing the effects of these processes on the colour reproduction of the images, we conclude as shown in Table 4.2. Colour filter, silicon parameters and technology processes have quite stable effects so that we can obtain coefficients of the effects from experiment and provide compensation in the design in advance. Light sources vary from time to time so that we have to have a real-time colour balance controller to monitor light source variation and feed back gain adjustment. We describe this in the next section.

Table 4.2. summary of effects

process	effects
colour filters	fixed with some tolerance from wafer to wafer
silicon parameters	fixed with some tolerance from batch to batch
technology process	fixed with some tolerance from batch to batch
light sources	varies from time to time

4.4 Colour balance control techniques

Variation in colour illuminance of light sources causes the colours of images to look differently from the original. Colour balance is a control process to achieving a fidelity on colour reproduction by adjusting the gains of the different channel. Conventional colour balance techniques include white balance (used in video camera) [Imaide, 1990; D'luna,1991; Teleview,1993] and integrating to grey (used in photograph development) [Evans, 1951; Bartleson, 1956; Hunt,1960; Pearson, 1978]. The objectives of colour reproduction and the conventional colour balance techniques are reviewed in this section.

4.4.1 Objective of equivalent colour reproduction

There are six kinds objectives in colour reproduction which were defined by Dr. Hunt [Hunt, 1987]. These are 1. Spectral Colour Reproduction; 2. Colorimetric Colour Reproduction; 3. Exact Colour Reproduction; 4. Equivalent Colour Reproduction; 5. Corresponding Colour Reproduction; 6. Colorimetric Colour Reproduction as a Practical Criterion.

The objective in TV system is chosen to be Equivalent Colour Reproduction [Hunt, 1987]. This objective makes allowance for:

argued that, because any colour reproduction will tend to adapt the eye towards its average colour balance, it would be an advantage if the light from the print, when integrated, appeared grey in colour, because then the eye would immediately be adapted to it. In this way, prints can be made rapidly by automatic printing methods to a consistently high standard of acceptance. A proportion will require special treatment, because of unusual subject matter but this is a surprisingly small proportion of pictures. This method has been applied in various ways [Bartleson, 1956; Hunt, 1960]. Automatic methods of adjusting the colour balance of video cameras have also been devised [Hunt,1987].

According to experimental results from 100 varied images, sampled by us using Adobe Photoshop [Lu, 1992], the proportion of marginal (unbalanced images) and failed images (subjectively unacceptable results judged by eye) after processing using the integrating to grey method was 18%. All case were identifiable as strongly colour biased or illuminated by flashlight. For most applications for internal scenes, such as videophone, the proportion of failed images may even go higher, so that we are not satisfied with this method.

As a result of the above investigation we set ourselves the aim of developing a digital automatic colour balance control technique, and this became a major part of the work of my Ph.D project. The proprietary method is described in the following section.

4.5 Automatic colour balance control on RGB peaks

The technique was developed for achieving the objective of equivalent colour reproduction; therefore its working principle is quite similar to the white balance technique. This technique does not only keep the advantages of the white balance technique, but it also enlarges the balance reference from white to also including yellow, cyan and green. Thus it does not need a white reference. It works directly on the colour images to save any secondary operation, or separated sensor and apparatus. It is implemented by digital logic and is suitable to be integrated on chip with the CMOS sensor. The extra chip area for the control logic is quite small so there is almost no extra cost.

4.5.1 The essential information of judging colour balance

What is the essential information used for judging the colour balance of a picture using objectively equivalent colour reproduction? Maybe the answer is "White", according to the objective of equivalent colour reproduction and other people's practice. By going through the details of the objective of the equivalent colour reproduction, I found that the correct answer should be the "RGB primary colour signals themselves."

This is not a trivial difference because it leads to the new colour balance technique based on the green peak.

From Table 4.3 we notice the RGB are weighted differently for different colours. The RGB can be picked out, not only from white, but also from other colours, such as the red from yellow, purple and red; the blue from cyan, purple and blue; the green from yellow, cyan and green. A colorful image could consist of many colours, saturated or not saturated, of which some colours are mixtures of two or three of the RGB primaries. Most of colourful images contain all RGB primaries. This fact hints to us, that if we could find a way of picking out the RGB signal levels which represent colour balance information for most colorful images with or without a white spot, then white no longer needs to play the key role in colour balance. If the colour balance judgement does not rely on the white reference then it could work on the image signal outputs in real time without using the white reference.

The next questions are how to pick out the critical levels of the primaries in the image monitored and how to judge whether the colour of the image is balanced. We present the solutions of these two problems in following two sections.

4.5.2 Algorithm of picking the peak levels of the RGB

Developing a proper algorithm for picking out correctly represented levels of the RGB signals directly from the output of images is a critical step for judging colour balance.

A key and novel contribution of the author of this thesis to knowledge and practice in this field has been the development of an entirely new method of colour balance based on the peak green signal in the image.

We reckon that the correctly presented level of the RGB in the image should be their peak levels. The algorithm for picking the peak levels of the RGB includes following steps:

Step one: We use green as a reference signal and find the peak level of green, Gpw, over the whole image.

The reasons for doing this are:

(1). in Figure 4.2 the green signal has shown a relatively stable energy level with changing colour temperature of ambient light source.

(2). green is a component in white, yellow, cyan, and green colours. These colours are usually brighter than other colours in images. Almost all images have at least one of these highlighted colours, therefore the green is the most important component in images.

These features of green mean that it can play an important role in colour balance.

Step two: We pick the peak levels of red and blue, Rpg and Bpg, in the area of the pixels where the green has its peak level. Rpg and Bpg are regarded as the first source of the peak levels of the red and blue for colour balance judgement.

The reasons for doing this are: the peak green areas are highlight areas in images, these areas could be white, yellow, cyan, or green in colour, from which there is big probability of picking the correct representative peak levels of the red or blue or both.

Step three: we pick the peak levels of red and blue over the whole image again, Rpw and Bpw. These are used as a second source of peak levels for red and blue for colour balance judgement.

The reason for doing this is to prevent an incorrect representation of Rpg or Bpg, which are picked in the green highlight areas. For example if the green highlight areas are only yellow, Rpg is correct representative but Bpg is not because yellow = red + green. If the area is only cyan, Bpg is correct representative but Rpg is not because cyan = green + blue. So, in the process of the colour balance judgement, the second sources of Rpw and

Gpw are needed and are used to replace Rpg and Gpg in above circumstances.

These five peaks should be recorded simultaneously in the same image. The implementation is described in Section 4.6.

4.5.3 Algorithm of colour balance judgement

In general the green peak level, Gpw, is the reference signal. The red and blue peak levels, Rpg and Bpg, are compared with Gpw respectively. They are equal to each other under colour balance. If they are not equal to each other, colour is unbalanced. However, if Rpg and Bpg are not picked from a white area, as mention above, this judgement may be incorrect.

To solve this problem we go through following sequences to work out a more successful colour balance judgement procedure. That is shown in Figure 4.8. While the image is scanned out, the five peaks, Gpw, Rpg, Bpg, Rpw and Bpw are recorded in parallel. The exposure controller has a high priority to examine exposure first which brings the RGB levels to the right range. The colour balance judgement procedure occurs during field synchronization. The first set of comparison is between Gpw and Rpg, and Gpw and Bpg. Only if Rpg or Bpg or both of them are greater than Gpw, is the image judged as unbalanced, the action is to reduce the gain of the corresponding R or B or both channels. If Gpw is greater than Rpg or Bpg the result will trigger the second set of comparison. This procedure can avoid a possible wrong action that the gain of the red channel would be increased by the judgement that Rpg is lower than Gpw, when a lower Rpg is caused by shortage of red in the green highlight areas, such as in cyan. The same circumstances can happen for Bpg, such as in yellow.

Obviously the first step of the judgement and action only improve the image in one direction, this is not enough. So we introduce the second comparison step in the colour balance judgement. If Rpg is lower than Gpw in the first comparison then this result brings about the second comparison. Instead of using Rpg, Rpw is used for comparison with Gpw. Rpw also has a big possibility of representing a correct level in the image. If Rpw is still lower than Gpw, the image is judged as unbalanced and the required

action is to increase the gain of the red channel. The same principle applies for the blue signal and the gain of the blue channel.

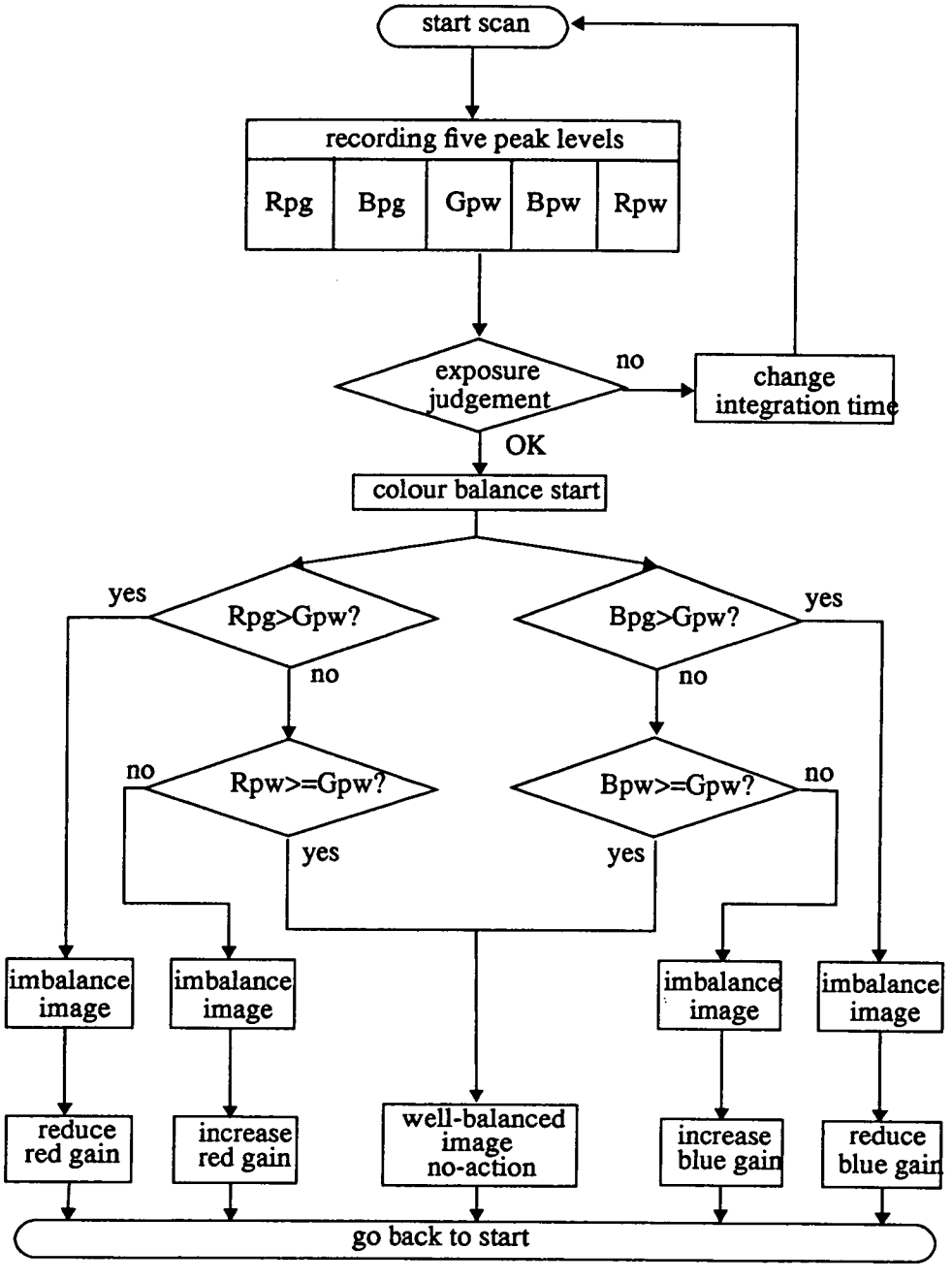

Figure 4.8. The flow chart of the colour balance scheme.

It is worth pointing out that the algorithm not only compensates for variation of colour temperature in the ambient light source over a wide range, but also automatically accommodates the systematic and manufacturing imbalances between the three channels. If the peak of red and blue are both bigger (smaller) than that of green, the gain of the red and blue channels could be reduced (increased) simultaneously.

Figure 4.9. shows various colour imbalance cases, expressed in four phases of the plane. The centre point represents the balanced colour position. No matter which case of colour imbalance the algorithm can judge it and then have a corresponding action until the well-balanced case has been reached.

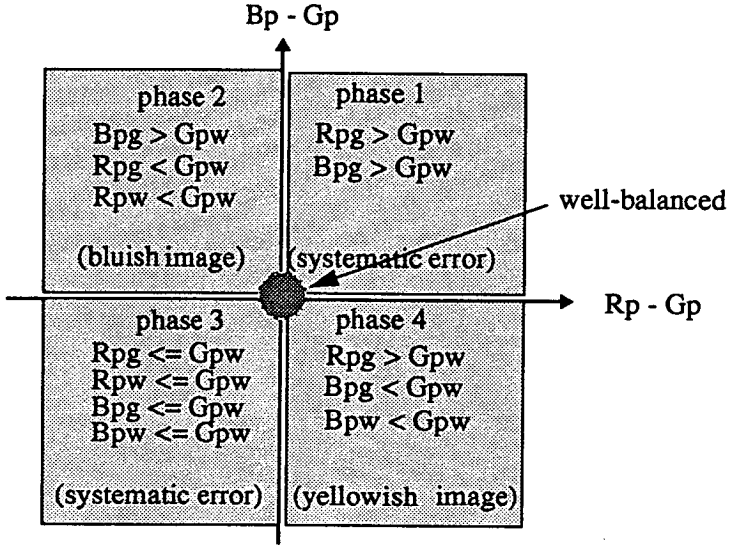

Figure 4.9. Five cases of the colour balance judgement.

4.5.4 Experiment

Experiments were carried by myself and D. Henry, an optical engineer. Two algorithms, the colour balance on green peak and the integrating on grey, were tested. The test colour images included a wide variety of scenes taken by a commercial still camera (the Canon Ion).

The colour balance on green peak algorithm was coded in C language (Appendix 3).

We deliberately imbalanced some of the test images by changing the amplitude of the green, red and blue signals using Adobe Photoshop (an image processing software package) on an Apple Macintosh computer. We then applied the algorithm to process these images and limit the balance tolerance to be less than or equal to 10%.

The experiment shows a high degree of success, 97% of the images are of good colour reproduction. Some images (3%) failed to achieve good colour reproduction. The reason is that the images are composed of only one strong primary colour, green, red or blue. The resulting reconstructed colour images look less saturated than original images because the balance processing increases the amplitude of the other primary signals which are weak or absent in the original images. Even the failed images are acceptable to the eye although colour fidelity is lost.

The colour balance algorithm of "integrating on grey" was tested using Adobe Photoshop either. We analysed the set of the test images for colour balance by noting the mean value of each colour channel. We characterised the colour balance for each picture as two parameters, which are the ratio of the red and blue means to the green mean. For confirmation of the integrating to grey algorithm, we look for a concentration of points around coordinate 1.0, 1.0, and qualify all images with a tolerance of 0.1 as well balanced. The test results show: 36% of the images meet acceptance criterion; 45% of the images are rebalanced with subjectively acceptable result; 18% of the images are rebalanced with unacceptable result.

The experimental results shows that the proportion of failed images (3%) of our proprietary algorithm is much lower than that (18%) of the integrating to grey algorithm.

4.6 Implementation of the colour balance controller

Using the colour balance algorithm detailed above, we have built a colour balance controller. The block diagram of the colour balance controller with the sensor and the exposure block is shown in Figure 4.10.

The colour balance controller is a digital signal processor, it includes groups of comparators, a colour balance judgement controller and two offset gain arithmetic units. It can easily be merged with the video format circuit, exposure controller and integrated with CMOS sensor on a single chip.

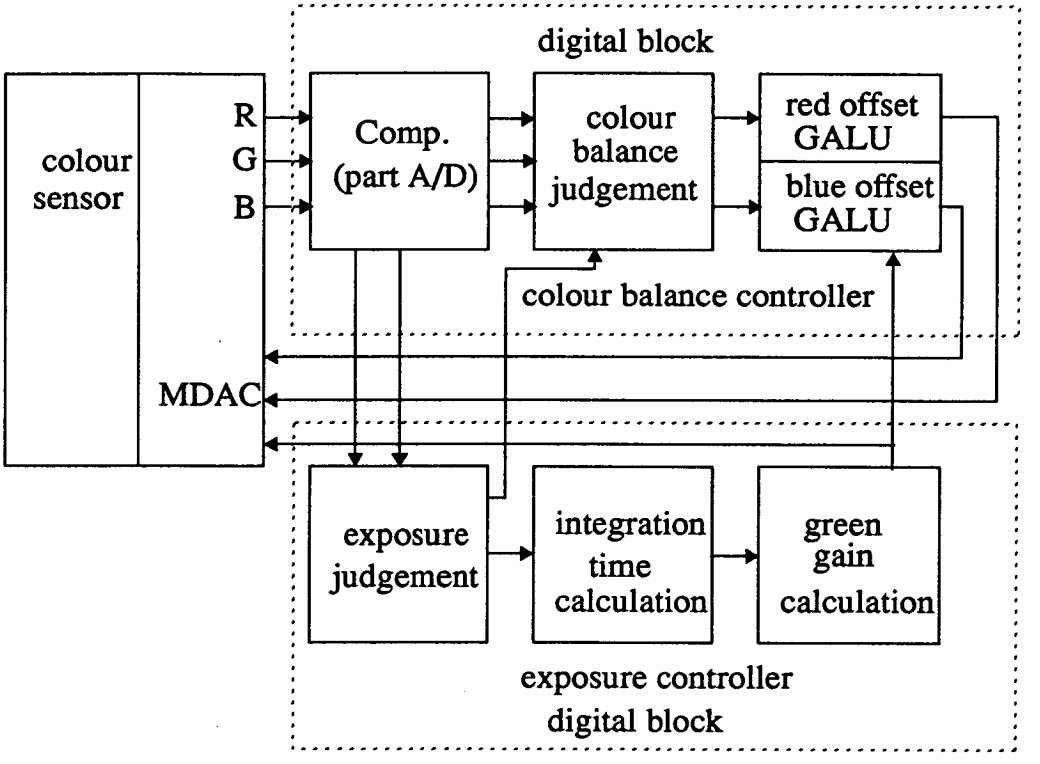

Figure 4.10. The block diagram of the colour balance controller and the exposure controller.

4.6.1 Thresholds of the comparators

The colour balance judgement decision depends on the RGB signal levels whose positions are in the upper part of the signal range, thus we do not need a full range ADC to implement the conversion of the analogue signal. We use only four comparators to categorize the value of the pixels into five coarse bands for each channel, as shown in Figure 4.11. The goal of colour balance is to adjust the gain of the three channels until

the RGB peak levels of the three colour signals fall into same band (band2). The width of this band (7% of the whole range) represents a tolerance on the colour reproduction. From the results of the experiment using the Macintosh computer we feel that images are subjectively good within a tolerance of 10%.

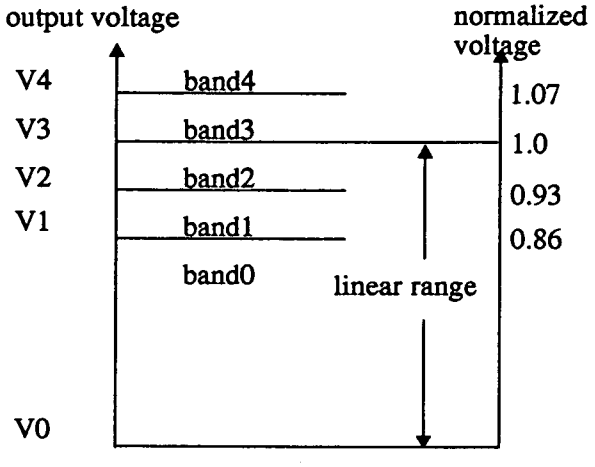

Figure 4.11. The bands of the output voltage.

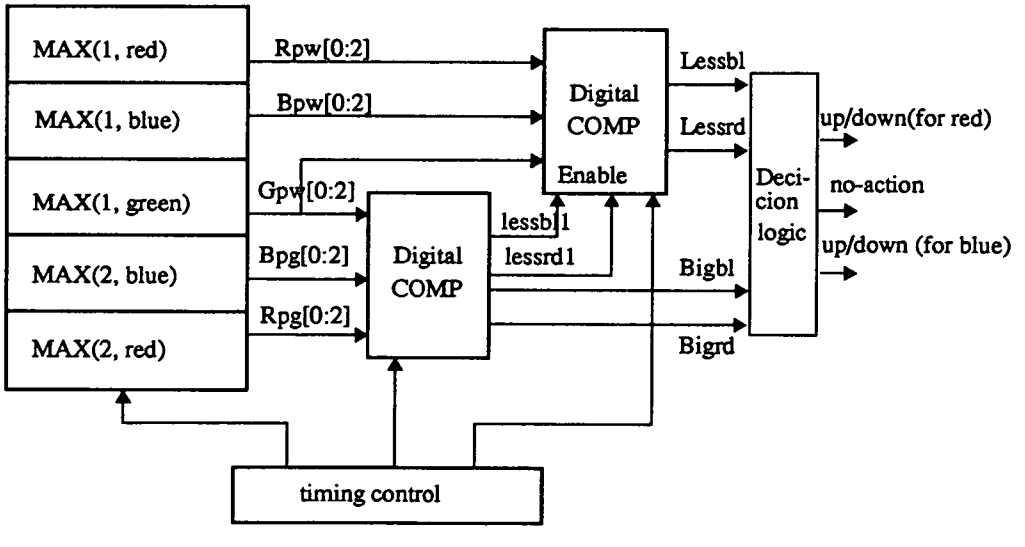

Figure 4.12. The block diagram of the colour balance judgement.

4.6.2 Colour balance judgement

The colour balance judgement controller includes two parts, one consists of five peak level recorders, called MAX blocks, the other consists of two digital comparators and a decision block. Figure 4.12 shows the block diagram for colour balance judgement.

4.6.2.1 Picking and recording the peak levels

The digitized output level of the pixels from the comparators is further processed by the MAX blocks. Each one implements the function of picking and recording the peak level of the pixels in each channel. Two kinds of MAX cell, MAX(1) and MAX(2), have been designed. MAX(1) is used for picking and recording the peak level of the pixels over whole image. MAX(2) is used for picking and recording the peak level of the pixels in the green peak areas. Figure 4.13 shows the detailed logic block diagrams of MAX(1) and MAX(2).

MAX(1) consists of an encoder, a digital peak level comparator, a 3bit peak level register and a pixel number counter. The encoder converts 4bit Gr[4:1] (output from the four analogue comparators) into a 3bit value Gren[2:0], whose 000(0) to 100(4) values represent the levels in the five bands. The counter is used to count the number of pixels having the peak level. We specify the number must be more than 64 in order to eliminate possible noisy in the video output stream. If the number is less than 64 at the end of field scanning, the value of the peak level in the registers will be reduced one.

The present pixel level, Gren[2:0], is always compared with the level in the peak registers. The present pixel level is sorted into three cataloguers, Bigger, Equal, Lower. If the present value is the "Bigger", it indicates that the value in the peak register should be updated and the number in the pixel counter should be cleared to 1. If the result is the "Equal" it indicates the number in the pixel counter should be increased by one. If the result is "Lower" nothing is done by MAX(1). At the end of field, Eq64 = 1 if the number of the counter is bigger than 64. Eq64, Bigger, Equal, Lower are used to control the operation of MAX(2) for picking Rpg and Bpg.

The function of MAX(2) is similar to that of MAX(1), but some differences exist, as

following explanation using MAX(2) for red as example.

(1). it finds two peak values, Rdg and Rdlog. Rdg is the red peak level in the peak green area, Rdlog is the red peak level in area of green level in next lower band. The Rdlog is used to provide Rpg if Eq64 is zero.

(2). operation is controlled by the sort results of MAX(1) for green.

In MAX(2) we use two registers for Rdg and Rdlog respectively, which is called Peakreg and Lowpkreg. Two digital comparators are used to sort the present pixel level, by comparing with the values in the two registers. The signal bigpix(1) and bigpix(2) indicate the present pixel level is bigger. Table 4.4 lists the updating condition of the peak registers.

At the end of odd field Foe signal (field-odd end) loads the five peak levels to the colour balance judgement block and switches on the judgement operations. Fst (field start) clears the all values in the registers after the five peak levels have been taken, to be ready for the next field.

Table 4.4. the update condition of the peak register in MAX(2) block

bigpix(1)	bigpix(2)	Equal	Big-ger	Low-er	update peakreg	update lowpkreg
True	*	True	*	*	yes	no
True	*	*	True	*	yes	no
*	True	*	*	True	no	yes
*	True	*	True	*	no	yes

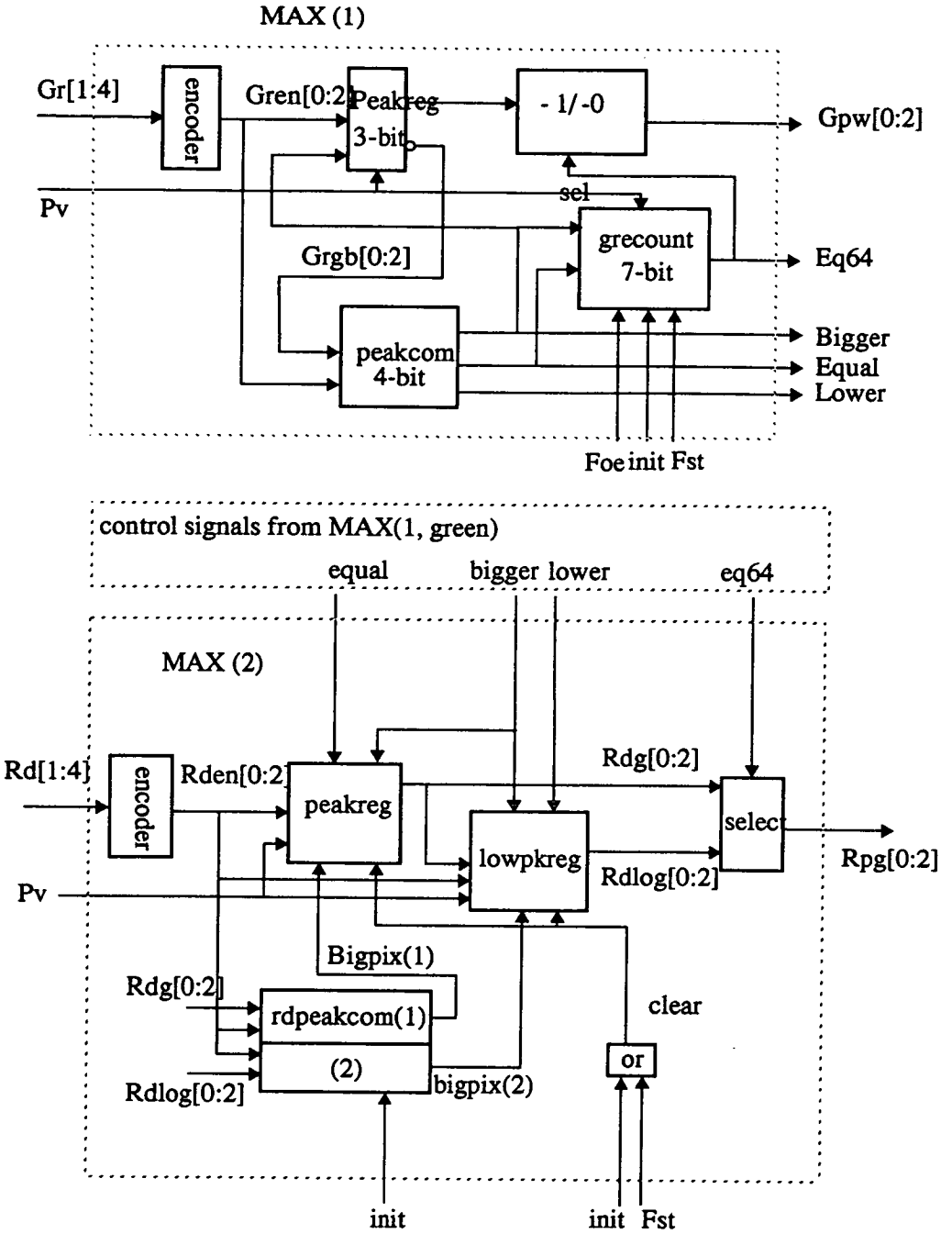

Figure 4.13. The logic diagram of the MAX(1) and MAX(2) block.

4.6.2.2 Colour balance judgement

The operations of colour balance judgement occur during the field synchronization period which is switched on by the Foe signal. The procedure of colour balance includes the following two steps, as shown in Figure 4.12:

(1). the Gpw compares with the Rpg and the Bpw respectively. If the Rpg is greater than the Gpw, then the Bigrd is true, the result indicates the gain of the red channel should be reduced by one step in next field.

(2). if the Rpg is smaller or equal than the Gpw in the first step of the comparison, the result brings the second step of the comparison into operation. Gpw is compared with Rpw once again. When Rpw is also smaller than Gpw, Lessrd become true to indicate an increasing gain action in next field.

Exactly the same judgement operations happen for processing the blue channel. After the two steps of comparison, the four signals, Bigrd, Lessrd, Bigbl, Lessbl, represent the result of the colour balance judgement. The four signals are further combined in the decision logic block to generate the up/down and no-action commands for Offset GALU blocks.

4.6.3 GALU for red and blue channels

Figure 4.14 shows the GALU block diagram. The GALU consists of an offset GALU, an adder and a register. The red gain value settings is expressed as the 7 bit digital numbers, Drd[7:1], which is calculated in GALU. The offset GALU is a up-down counter which forms an offset gain value. Its step size is one up or down. The adder sums the offset gain and the common gain values. The register stores the gain value for red channel.

The 8bit up-down counter operates from -127 to +127 that is expressed by 2's complement numbers. The Cbe signal stops the counter from incrementing or decrementing when not true and the number is then held.

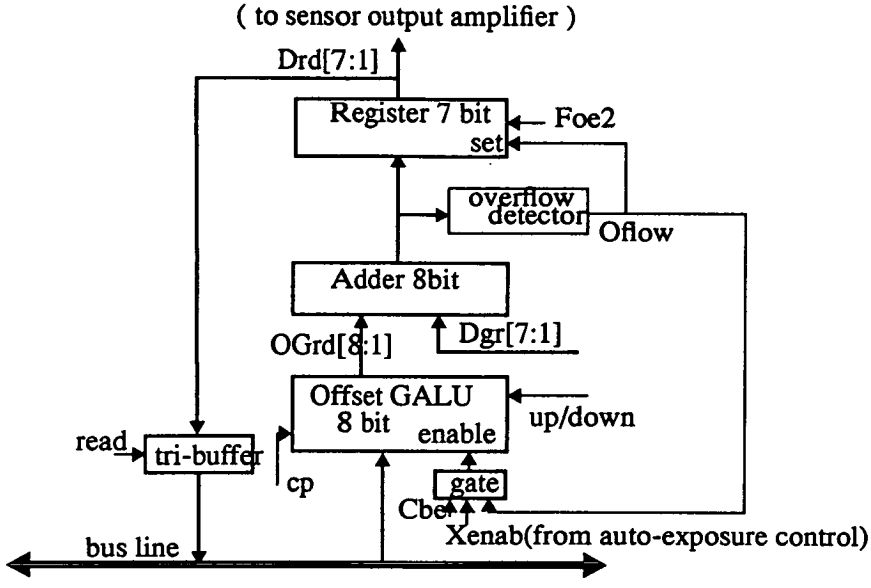

Figure 4.14. The block diagram of the red gain ALU(GALU).

The adder is 8 bit wide. The highest bit is the sign bit. The two addends are: the common gain value, Dgr[7:1], and the red offset gain value OGrd[8:1]. The range of the gain values required by the MDAC for each channel is 0-112. If the number from the adder is out of range, then the number should be clamped before it goes to the register stage. Two decoders are designed to detect overflow from the adder, the output is called Oflow. Oflow informs the up-down counter to stop further action in that direction and reset the number in the register to be in the range.

The external access allows GALU to receive an offset gain from the bus line and send its auto-calculated gain through tri-buffers to the bus line. When CBE is set to zero (inhibits automatic colour balance controller), it breaks the feedback of toggle cells in the counter and opens an access for an external offset gain value from the bus line. The counter behaves like a register in this mode.

When the master computer enquires the red gain value, the value in the registers can be sent out from the tri-buffer through the bus lines and the serial interface. The output of

the tri-buffer gates is high Z state if no enquiry comes.

4.7 Chapter summary

This chapter concentrated on the issues relating to colour reproduction in colour cameras. Some fundamentals about colour calculation are reviewed, including colour coordinates, primary matching curves, and objectives of equivalent colour reproduction. The factors that affect the quality of colour reproduction are examined, and the conventional white balance techniques are reviewed.

Our own proprietary colour balance technique, colour balance on RGB peaks, is presented, covering all aspects of the concept, algorithm, experiment and hardware implementation. It meets not only the objective of equivalent colour reproduction used for colour TV display systems but also has some advantages over the conventional white balance techniques.

These advantages are:

- it works directly on the output of the RGB signals;
- it realizes an automatic and real time colour balance controller on the same chip with colour sensors;
- it is implemented digitally by only 2,500 gates;
- it involves no extra hardware cost.

The experiments using the Macintosh computer have shown the algorithm of the controller to work effectively for 97% of the benchmark images, compared with 82% using conventional integration to grey.

Chapter5 Other Control Techniques

This chapter describes some other control circuits for on-chip solutions, such as video timing generator, exposure data encoder, black level calibration, optical centre registration, camera control interface, etc.

5.1 Video timing generator

This part of the logic generates the operational timing signals for the sensor to provide composite video format.

5.1.1 Timing consideration

The NTSC and PAL composite video systems have 525/60 and 625/50 standard interlaced scanning rates respectively. To realize a medium resolution image with standard video format we apply a non-interlaced scan mode in the vertical direction of the sensor array. Then the odd and even fields of the video signal are traced out on the same lines. So the vertical resolution of the sensor array is half of full video resolution. This is 240 or 287 lines in NTSC or PAL modes.

The resolution of the array can be chosen around 300 - 400 pixels in the horizontal direction to make the resolution approximately equal in vertical and horizontal directions. The pixel sample frequency is then around 6MHz, which is derived from pixel number divided by the visible duration of per video line (52μs for PAL and 52-53.4μs for NTSC).

The line frequency of the video signal, Fh, is 15.625KHz for PAL and 15.734KHZ for NTSC. Fh does not need to be very accurate for monochrome video. For colour video Fh must be accurate and stable because the colour subcarrier frequency Fsc in the NTSC system has been strictly specified to avoid interference on the screen. Fsc, 3.579545MHz, is the 455th harmonic of the Fh/2. To meet this specification we choose an external clock frequency Fclk as four times high as the Fsc, i.e., 14.31818MHz. Then Fh is derived from Fclk by division 910, which gives 15,734.264Hz. The pixel clock

Fpclk is then 5.727272MHz, which is divided by 2.5 from Fclk. Table 5.1 shows the external clock, pixel clock, resolution of the array, pixel size etc. parameters of two designs (ASIS-1011 and ASIS-3000), which will be presented in Chapter 6.

Table 5.1: Pixel clock and resolution of two sensors

camera device	TV system	external clock (MHz)	pixel clock (MHz)	resolution	visible time (μs)	pixel size (μm^2)	array aspect
ASIS-1011	PAL	12	6.0	312 x 287	52	19.6 x 16	4:3
ASIS-3000	NTSC	14.318	5.7272	305 x 240	53.4	10.5 x 10	4:3

5.1.2 Video timing generator

Figure 5.1 shows a logic diagram of the video timing generator. According to the video signal characters and the operation timing requirement of the sensor, we generally build two counters to give a line and a frame period. They are both synchronous counters with a serial carry. The counting ranges are 0-N1 (Number of pixels clock cycles per line) for the line counter and 0- N2 (number of lines per frame) for the frame counter.

The outputs of the counters, q[8:0] and q[18:9], are sent to the decoders in next stage. Static decoders are used for fixed number decoding, dynamic decoders are used for a changing number decoding. The dynamic decoding number is represented by Sf[8:0] and Sc[17:9]. When q[8:0] equals the Sf[8:0], the output of the dynamic decoder is one. Otherwise it is zero.

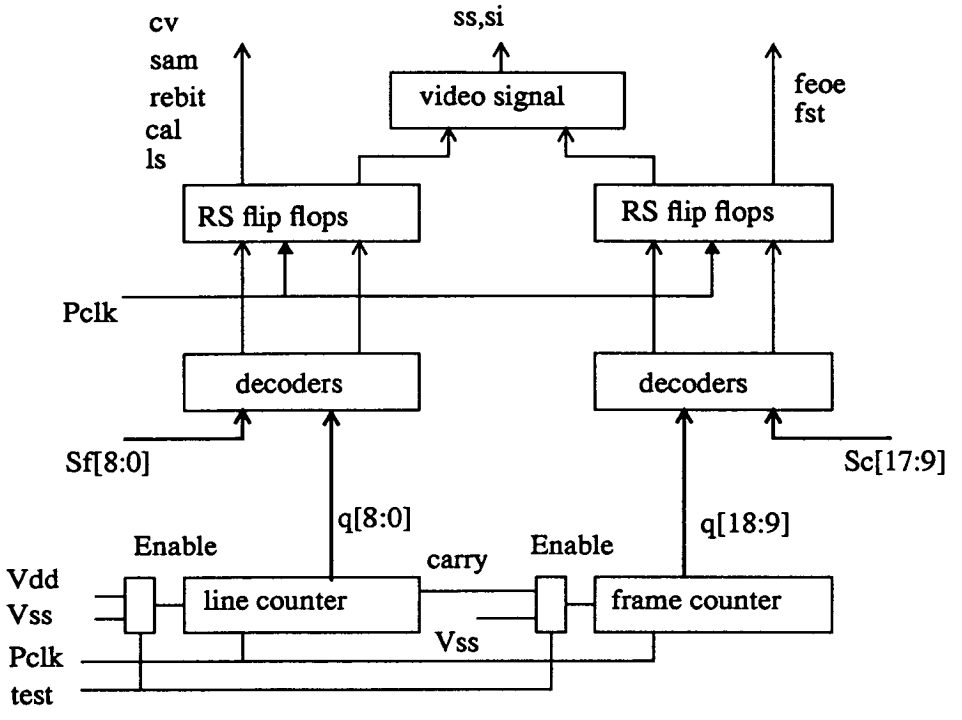

Figure 5.1. The block diagram of the video timing generator.

The next stage comprises RS flip flops whose set and reset nodes are connected to the decoders' outputs. Desired width of pulses of the line operational signals are obtained from the output of the RS flip flops, such as CVI, SAM, CAL, RST, REBIT and LS. The frame operational signals, FI, feoe (flag of the odd/even fields), fst (field start), are obtained from the frame's RS-ffs.

SI, SS are line video output and line synchronization level enable signals, their waveform changes are related to the video scanning sequence. We produce them by combining the line and frame pulse signals together. On the line side three different width of synchronous pulses are generated, the frame signals select one from three appearing at the output of the SS signal according the line sequence in the frame. SI is switched off during the field synchronization period. SS, SI are applied to an analogue multiplexer to select different voltage levels to form the video output signal from the camera device. SS, SI, and video output waveform are shown in Figure 5.2(b).

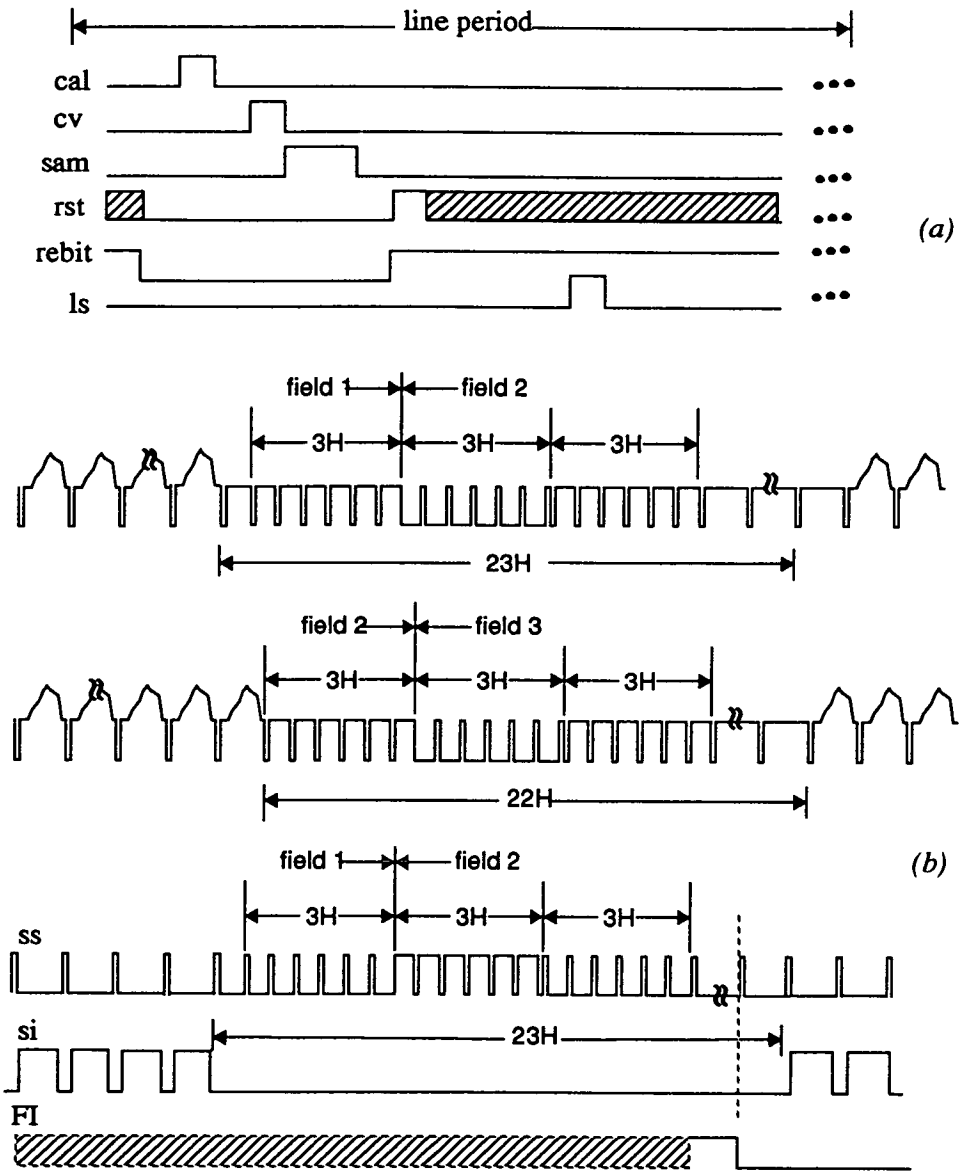

Figure 5.2. (a). The generated line operation signals. (b). The NTSC video frame signals.

5.2 Exposure data encoder

FI and RST are two signals whose waveforms are related to the control of pixels'

integration time. In Chapter 3 the exposure data generated by the exposure controller, exp[17:9] and exp[8:0], need to be encoded to the waveforms of FI and RST to control the integration time.

We define FI's zero period as resetting pixels to bias voltage and its one period as the coarse integration time of the pixels, therefore the width of the pulse of FI changes with the exposure data, exp[17:9]. FI's falling edge selects a read line, in which the charges of the pixels are sampled to the sense amplifiers. FI's falling edge timing must be matched with the beginning of video display window. FI's rising edge is encoded with the coarse exposure value to control the integration time of the pixels, so that the rising edge goes backward with increasing the exp[17:9]. Figure 5.2(b) shows the waveform of FI.

RST is the pixels' reset signal. Its one period is used to reset bias voltage to the pixels and its zero periods represent a fraction of line period of the integration time. The width of the zero period varies with the fine exposure value, exp[8:0]. RST's rising edge is fixed, its falling edge is encoded with the exp[8:0], shown in Figure 5.2, so that the falling edge of RST goes forward with increasing exp[8:0].

The implementation of logic to achieve a changeable waveform for FI and RST is shown in Figure 5.3. Each part comprises an adder, a dynamic decoder and an RS flip-flop. The adders are used to transfer the exposure value exp[17:9] and exp[8:0] to data Sc[17:9] and Sc[8:0] that relate to the position of the rising edge of FI and the falling edge of the RST. A, B are constant. The one dynamic decoder compares Sc[17:9] with q[19:11] (the output from the frame counter). When Sc[17:9] is as same as q[19:11], the output of the dynamic decoder is 1. It then sets FI to one. The output of the static decoder resets FI back to 0 at the fixed timing. The same circuit is used for generating RST.

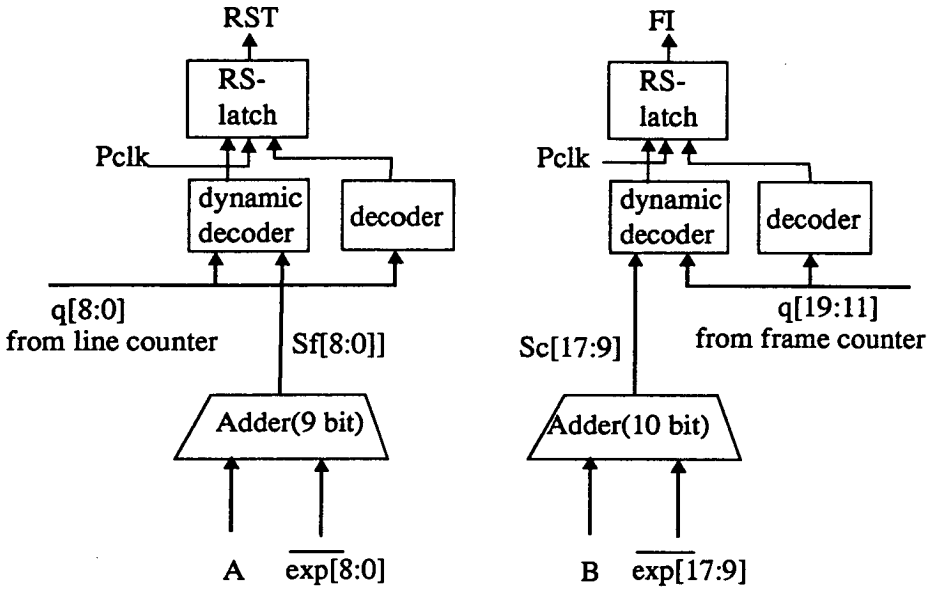

Figure 5.3. The implementation of the exposure data encoder.

5.3 Black level calibration

It is important to have a constant black level to get the right TV format and good picture quality. There will be a synchronization problem if the black level is too low (lower than the blanking level). On the other hand, the black contents will look less than black if the level is too high. Data conversion also needs a constant black level. However, ASIC processes cannot guarantee a constant level across different batches, because electric parameters will vary (such as the value of threshold voltage). Variation in operating temperature will also result in a shift in black level.

5.3.1 Black calibration in monochrome cameras

In monochrome cameras an auto-black calibration function has been successfully implemented in the output amplifier stage of the sensor [Wang, 1993]. Please refer to Figure 3.8 for the following describtion.

The input Vin (= Vblack - Vv) is an inverted video output stream from previous amplifiers. M2 provides a constant current source Imax, of value equal to the greatest current from M1 when Vin = Vblack. For an arbitrary value of Vin, which converts to Im1 through M1, the residual current Iv (= Imax - Im1) flows out of this stage, through M4 and the load devices of MDAC to ground. As has been explained in Chapter 3, this MDAC provides an adjustable gain. The output becomes:

$$Vout = Iv/GD[6:0]$$

The black calibration is enabled by a signal called Bre, which turns on M3 and turns off M4. Meanwhile, a line of black pixels is read out as black level reference. The black line is put on the bottom of the photo array and is shielded by a third layer metal. In this case, Vin equals Vblack, and the current of M2 equals Imax. The resulting voltage value is stored in the capacitor of Cbck and will be kept for one video field until the calibration process can be repeated.

Vout equals zero when black calibration is carried on, and will be zero for any black pixels.

5.3.2 Black calibration in colour cameras

Black levels in three channels should be at the same level to achieve black level balance. We may have black lines in each colour array but, because the need for optical registration the timing of the Red and Blue array's black pixels is not in fixed position, so it is not practical to use them to get black level calibration. One solution is that the black pixel line in the Green array is used for calibrating the black level for the three channels by assuming the pixel array and, the sensor amplifier circuits have exactly same physical size and electrical parameters. We remove the M3 transistor in the red and blue channels but keep the Cbck capacitor, M1 and M2 in the circuit. The Cbck in the Red and Blue channel is connected to Cbck in the Green channel. When doing black level calibration in the green channel, the BCK voltage is shared between the three channels. The current Imax in the three channels are then equal to each other so that the purpose of the black level calibration and balance can be achieved for the colour

camera.

5.4 Optical centre registration

ASIS-3000 (details in Chapter 6) has a programmable optical centre registration function. It is designed for accommodating the systematic parallax error that will be caused by the triple lens assembly. The optical centre x, y of the red and blue arrays is designed to be able to move 7- 8 pixels in all directions from the geometric centre(0,0) of the array by external settings through the serial interface.

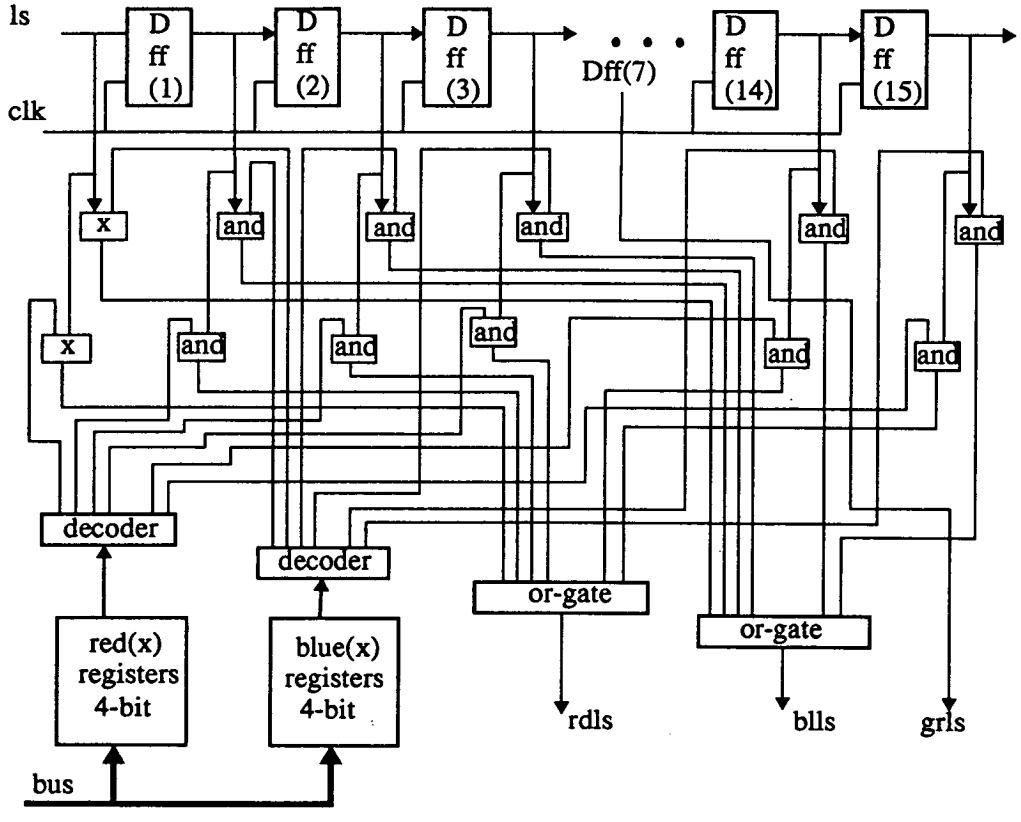

Figure 5.4. The optical registration circuit.

LS and FI are inputs to start horizontal and vertical scan in the sensor arrays. LS and FI's pulse timing are programmed to cope with requirement of the moving of the optical area of the sensor array. Figure 5.4 shows a 15-bit shift register that is used to delay LS

to GRLS (for green array), RDLS (for red array), BLLS (for blue array). The external settings X(blue) and X(red), loaded in through the serial interface, select different decoder gates to program the RDLS and BLLS's timing position relatively to GRLS's. The output of GRLS is fixed in the middle of the shift register position, RDLS, BLLS' position can be moved backward or forward from the position of GRLS. So the optical area of the red and blue array are moved with the X numbers in the horizontal direction

Another 15-bit shift register with decoders is used to delay FI to GRFI, RDFI, BLFI. GRFI's position is fixed as no extra lines in the green array. RDFI and BLFI's positions can be moved +/- 8 lines according different Y settings. So the optical area of the red and blue can be moved with Y numbers in the vertical direction.

Figure 5.5 shows the optical centre of the red and blue array moving in both horizontal and vertical directions with different settings.

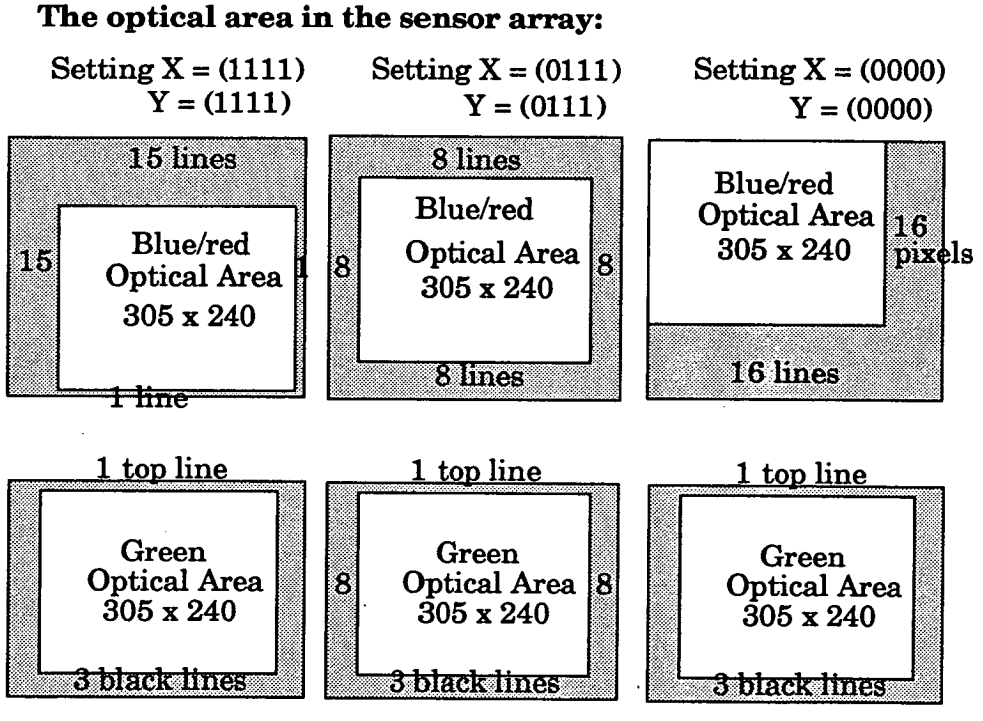

Figure 5.5. The optical area movement with the X and Y settings.

5.5 Camera digital interface

Digital video interactive (DVI) technology has been rapidly developed in recent years to meet the requirement of video information processing. Bringing together video and personal computing creates a system, which fulfils a large number of needs. This system is user-friendly and can deliver many types of presentation to the user.

In order to develop a communication channel between the PC and the camera, a serial interface circuit has been designed for this purpose. A host computer can set operation parameters and control exposure, gain values and optical registration etc. The host can also interrogate the camera for all operation parameters via the interface.

Figure 5.6 shows the host computer connections to the camera and the interactive operation of the camera. All automatic controllers can be switched off individually and then an external control can be set up by sending control parameters via the interface. The output of the camera connects to the RS232 interface of a PC. The video image data can be processed and displayed on PC.

5.6 Chapter summary

Control techniques for the video timing generator, exposure data encoder, black calibration, optical registration and camera interface have been presented in this chapter.

Again, all control techniques in this chapter are implemented on chip. Each function will benefit applications further, but only cost extra hundreds gates.

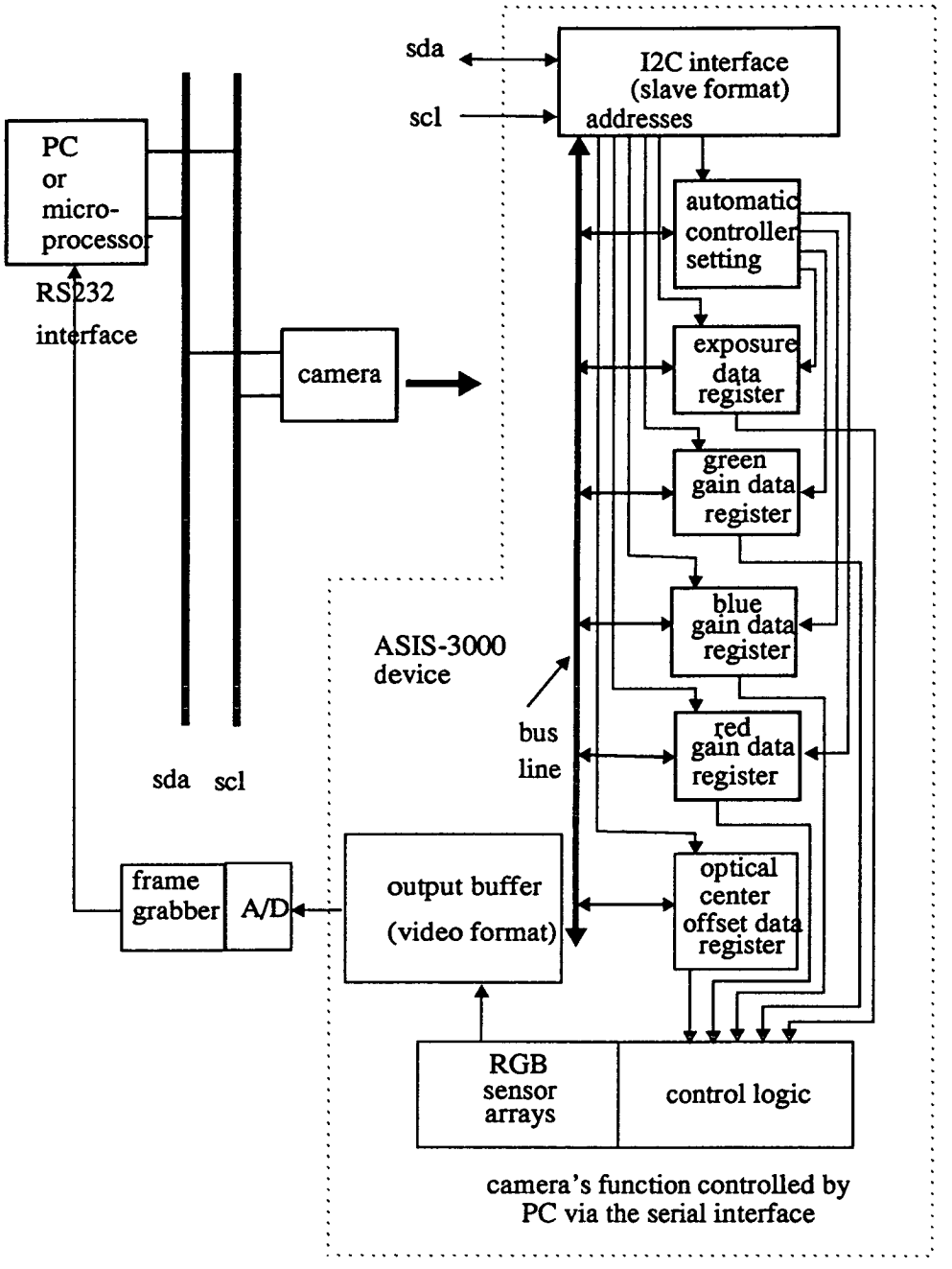

Figure 5.6. The camera interactive block diagram.

Chapter6 Implementations: ASIS-1011 and ASIS-3000

6.1 Introduction

In order to test the techniques described in the previous chapters, several single chip video camera devices have been designed. In all 9 chip designs were completed by the author of this thesis and 2 designs by other engineers adopting the techniques developed here. Appendix 5 lists some of these devices in which the control techniques described in this thesis have been used. This chapter describes two of them in detail.

One design, named ASIS-1011, is a highly-integrated monochrome video camera device, which has pixel resolution of 312 × 287. It includes all the necessary circuitry to drive and sense the array, delivering CCIR 625/50 formatted composite video signal with on chip control functions such as automatic exposure and gain control, auto black calibration.

ASIS-1011 features automatic electronic exposure control over a wide range (40,000 : 1), enabling the use of a fixed-aperture lens. Automatic gain control (AGC) provides up to +10dB gain boost at low light levels. Black-level calibration maintains image stability, obviating the need for externally-adjusted components.

The die measures 7.95 × 7.05 mm^2, using the 1.5 μm, 2 level metal CMOS technology of ES2 (European Silicon Structure).

A miniature PCB integrates the chip with all necessary components to implement a complete CCIR-standard video camera, requiring a single unregulated DC voltage supply to produce a buffered composite video output capable of driving a 75 ohm load at 1 volt peak-to-peak. These components are:

- a 12 MHz crystal or ceramic resonator as clock source;

- a 5v regulator for stabilizing the power supply;

- a bipolar transistor for buffering video output;

- a few resistors and capacitors for biasing and decoupling.

The PCB, including chip and all other components weighs 50g, measures 30 mm diameter, and consumes 150 mW. Figure 6.1 shows the photograph of a chip, a PCB, and miniature cameras.

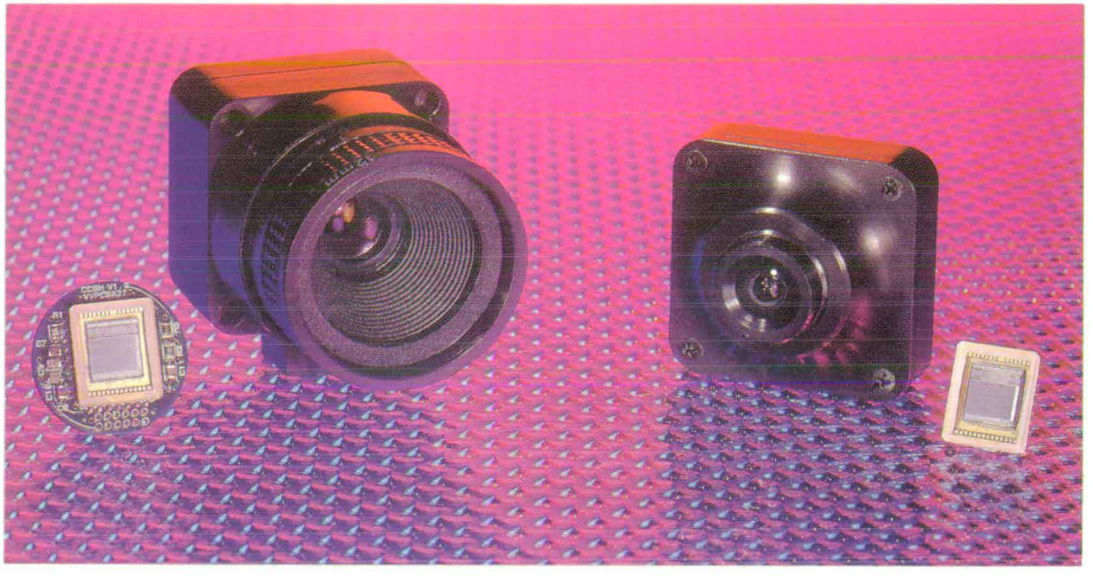

Figure 6.1. The photograph of a chip, a PCB, and miniature cameras.

Another design, named ASIS-3000 is a highly-integrated colour video camera device. It has three 305 × 240 pixels image sensor arrays, one for each primary colour: Red, Green, Blue. It includes all necessary circuitry to drive and sense the arrays, delivering three EIA 525/60 formatted monochrome video signals. To form a full-formatted composite colour NTSC video signal, an encode device (AD720 RGB to NTSC) is needed.

ASIS-3000 features automatic electronic exposure control over a wide range (3,000 : 1). It requires a special-purpose (custom designed) fixed-aperture fixed-focus triple colour lens. Automatic gain control enhances image contrast under low level lighting conditions. Automatic colour balance controls gains to compensate for spectral

variation of ambient light covering colour temperature of light sources over a wide range. Automatic black level calibration maintains stability of the image output, obviating the need for externally-adjustable components.

A serial interface allows a host computer to set operational parameters and to control exposure and gain values directly. The host can also interrogate ASIS-3000 via the serial interface to determine the camera capability and current state.

The design, using 0.8μm 2 level metal CMOS technology of VTI (VLSI Technology Inc.), was completed and passed the pre-sign-off procedure with the foundry, but didn't go fabrication for the reason explained in the first chapter. However, I have built up the knowledge of the colour camera system and experience from the algorithm experiment and design implementation. The techniques developed for ASIS-3000 are valuable and most of control blocks can be used in new colour devices in the future.

6.2 Main functions and features of ASIS-1011

The architecture of ASIS-1011 is shown in Figure 6.2.

The next section will briefly explain the analogue block (Figure 6.3) which was designed by another researcher [Wang, 1993]. The digital control functions are explained in the follow sections.

6.2.1 Analogue block

The light sensing area consists of a 312 × 287 pixel array, which are accessible on the basis of sequential selection of each row through a vertical shift register. At the top of each column is a sense amplifier. The sensed information is read out sequentially along the x-direction under control of a horizontal shift register. At the end of the path there is an output amplifier followed by an output buffer.

The photodiode is implemented by extending the source region of MOS transistor. This may be reset and then isolated under control of the MOS transistor gate. All of the gates

in each row are driven in common. Once reset, the reverse-biased diode converts incident light into a small photocurrent which gradually discharges the photodiode capacitance. The pixel is read by opening the gate, connecting the photodiode to the MOS transistor drain. All of the pixel transistor drains in each column are connected in common and only one row is read at the time. At the top of every column line a sense amplifier is integrated. These sense amplifiers need not work so quickly, since their activation frequency is equal to the line rate rather than the pixel rate and they are situated as close as possible to the pixel array. Their sole constrains are the need to achieve a good dynamic range and to be realised within the pixel pitch. The read time is approximately 0.5μs.

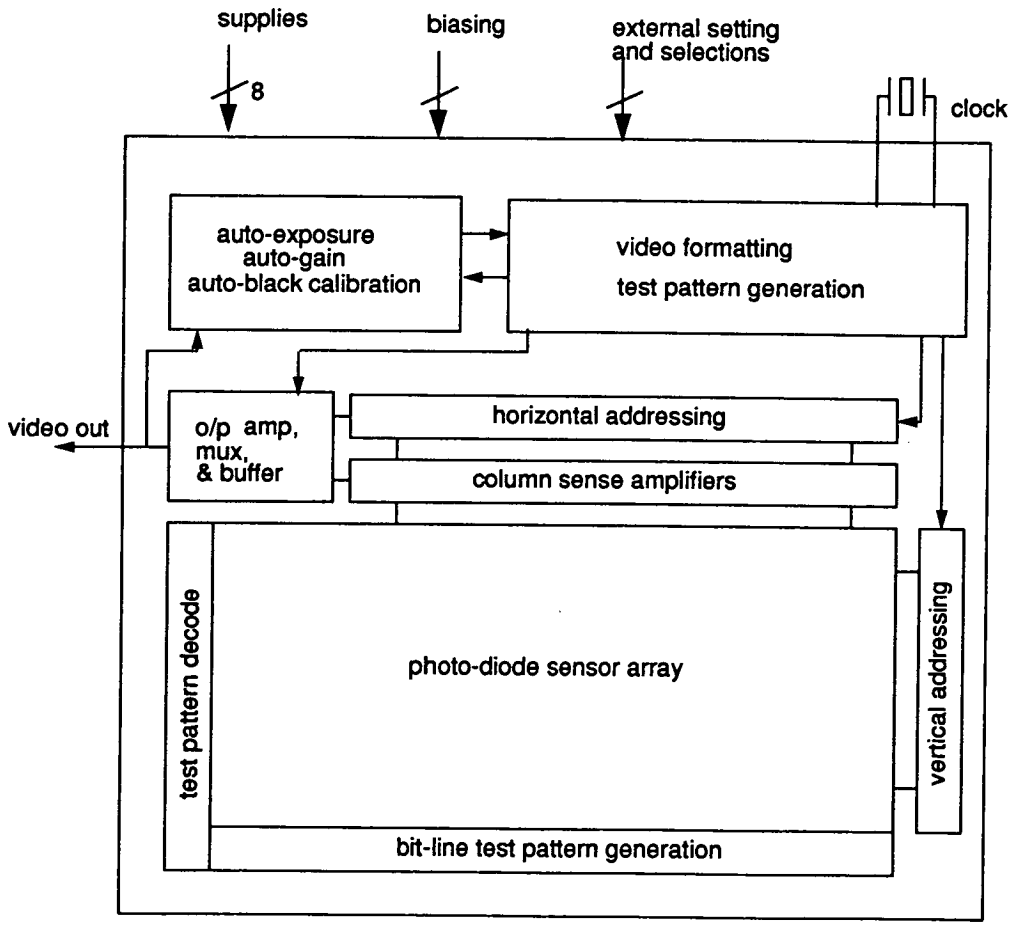

Figure 6.2. The architecture of ASIS-1011.

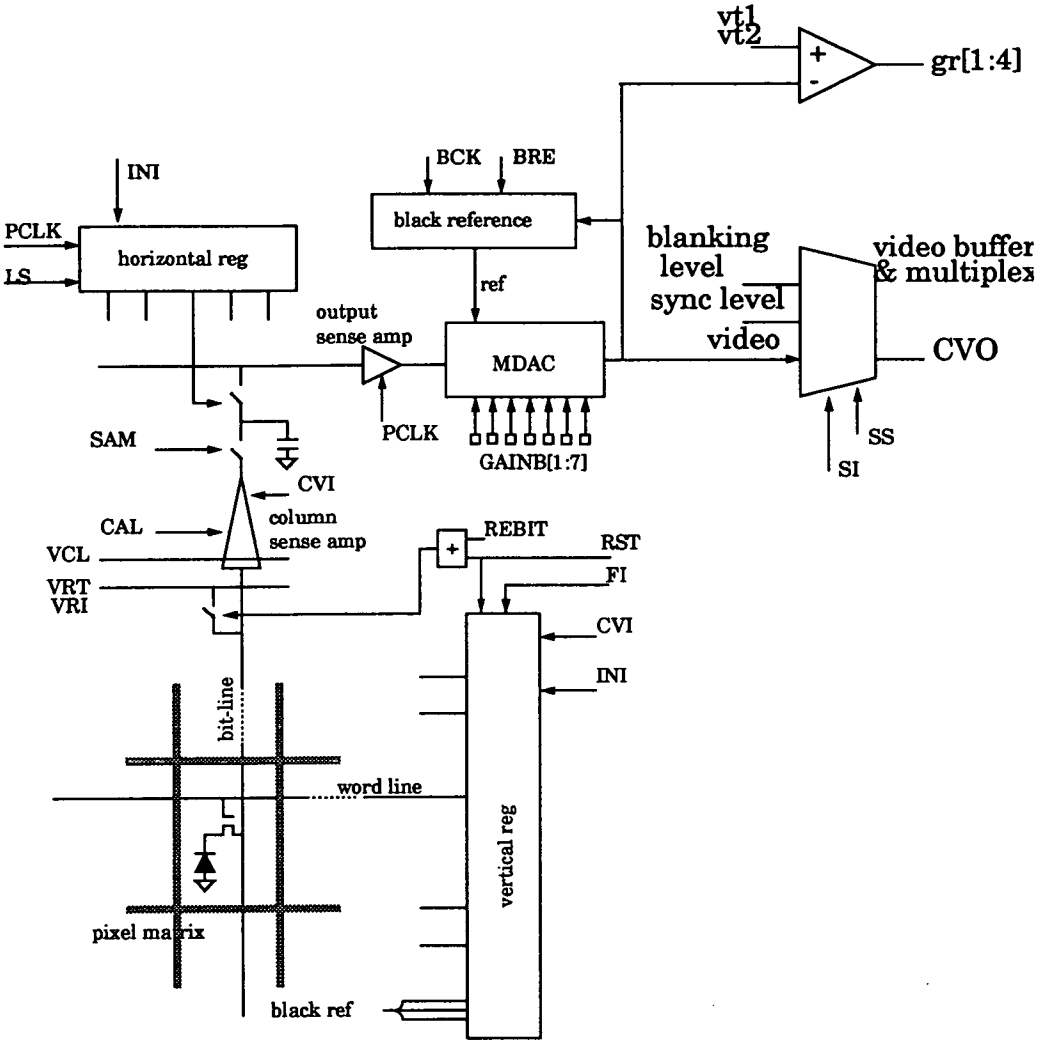

Figure 6.3. The architecture of the sensor array.

6.2.2 On chip composite video formatting

Approximately 1,000 gates implement the video timing block to deliver a fully-formatted composite video signal and driving timing signals for on-chip microcontrollers. The details of the video timing block have been described in Chapter 5. The image data stream is then multiplexed with the sync-level and blanking-level,

controlled by timing signals. Figure 6.4 shows the composite video signals. Apart from generating all necessary signal for internal requirement of the camera, the video timing block also provides two signals for external frame grabber sampling the image from ASIS-1011 device. One is FST, indicating a new field of image beginning. The other is PVB, indicating the pixel valid when pixels are to be sampled (for ADC).

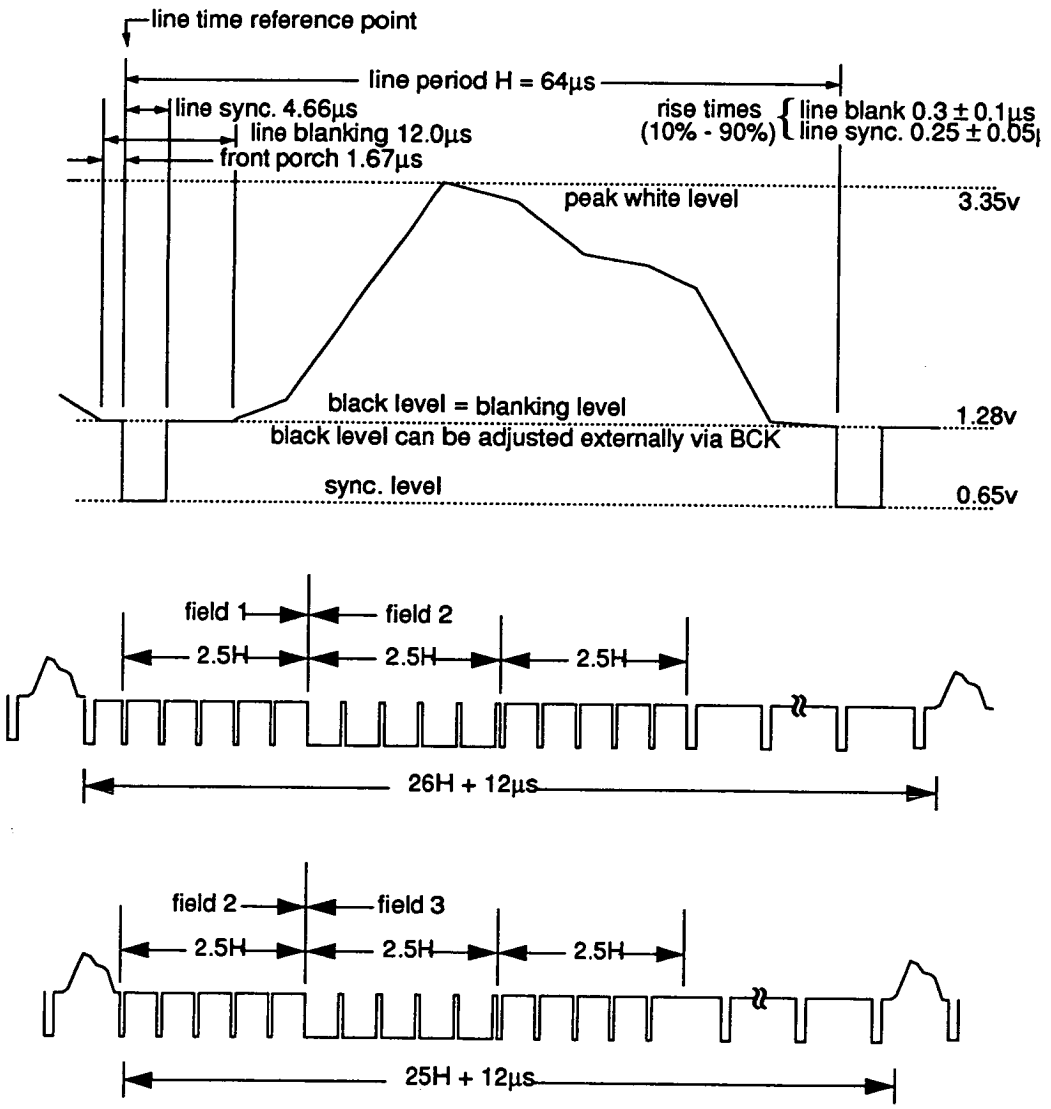

Figure 6.4. Video signal format of ASIS-1011 devices.

6.2.3 Automatic exposure control

The device automatically controls its exposure over a range of 40,000:1 using the scheme described in Chapter 3. This is the main mechanism for adjusting sensitivity to track varying picture conditions. The integration time can be as long as one field, or as short as three cycles of the pixel clock. The exposure is set by monitoring the video stream and estimating the fraction of each picture which is very white (above VWT) and very black (below VBT). VWT and VBT are pins which set white and black threshold levels. On the basis of this information the device decides whether the picture is too white, too dark, or OK.

The exposure time is varied if necessary, in steps of 6.25%, in the appropriate direction until the correct exposure for the scene is obtained.

6.2.4 Automatic gain control

The output gain of the device is controlled by the scheme described in Chapter 3. A 7bit MDAC has been implemented on chip. In theory, it can provide gain adjustment of more than 100 times. However, in practice, we should put margins on both ends when doing the design. We can not use minimum gain as normal setting because it may cause trouble if the gain is still high. This could be caused by technology variations. Therefore, the normal gain is set higher and the setting can then be adjusted by external pull-up and pull-down of pins. At the other end, we don't use the very high gain settings because a single step there actually means a big gain change. Thus, we use the middle range of the setting and expect 10 times (20dB) gain control for this design.

AGC function is optional. When pin AGC is pulled low, the device automatically increases the gain of its output stage when the exposure is maximum and the picture is still too dark. Otherwise gain is maintained at its normal value which can be set externally by pins GS5, GS6 and GS7.

The gain control works well over the expected range for the nominal gain setting. However, the PCB tuning changes a few of the bias values (such as BCK) in order to

get a better picture. The gain setting then has to follow those bias changes. The actual normal setting was more than 2 times higher than expected setting, reducing the gain adjustment to about 10dB.

6.2.5 Automatic black-level calibration

This circuit automatically calibrates the video black level using the method described in Chapter 5. Three extra lines of "black pixels" are added on the bottom of the photo array, of which, the second line is used for calibration. The reason to put three extra lines is to avoid leakage from neighbouring non-black pixels. Calibration occurs every field. It can be inhibited by setting the pad IBC = 1, in which case an internal bias voltage sets a nominal black level. This bias voltage can be overridden externally on pin BCK for fine adjustment.

6.2.6 Simple solution for test

Special consideration has been given to make it possible to carry out digital wafer test which is as complete as possible within the limited test vector length available. The digital counters in the video timing block are sped up by switching a test signal through a pad. The exposure and gain control blocks are auto tested by running the datapath internally, which is controlled by a pad as well. The connection signals between sensor and driving logic are observed through bidirectional pads.

The analogue parts are also tested by making them produce digital outputs, so avoiding a requirement for full analogue test. The test includes bit-line tests, word-line tests and chequer board tests. The individual photo pixels may be tested using chequer board test if a sufficiently long vector set is allowable. The chequer board test can also be used to check for excess column leakage. The self-generated chequer board pattern which may be displayed on a monitor screen, or captured by a frame grabber.

The test vectors have a toggle coverage over 98.8% of the all of nodes.

6.2.7 Main features

Here is a summary of ASIS-1011 main features:

- 312 × 287 pixel array
- 7.97 × 7.05 mm^2 die size
- automatic black-level calibration
- automatic exposure control (range 40,000:1)
- automatic gain control (up to +10 dB)
- field-start and pixel clock outputs to facilitate frame grabbing
- 0.5" format lens-compatible
- CCIR 625/50 format composite monochrome video output.
- 8 lux operation (measured at sensor surface with a IR cutoff filter)
- power consumption < 150mW

Appendix 1 lists all pads of ASIS-1011.

6.3 Main functions and features of ASIS-3000

The architecture of ASIS-3000 is shown in Figure 6.5. The design consists of two parts. One part is the full-custom layout designed sensor arrays. It includes three sensor arrays, in which each has its own photodiode array, sensor amplifiers, output amplifier incorporating a MDAC stage for implement a high gain performance, horizontal and vertical shift registers with decoding circuit formed a electrical aperture. Each array behaves like a single monochrome sensor array. The other part is a logic circuit, in

which all necessary circuits to drive and control the sensors are designed. This part includes a timing block, two microcomputers for AEC, AGC and ACB control, and a serial interface for communication between a host computer and the camera. These two parts form a self-contained colour video camera system.

Figure 6.6 shows the layout of the design. There are 29 pads line up at two narrow side of the chip. At the left and right side are full of ground pads to offer the triple lens assembly. There are 49 internal connections between the sensor arrays and the logic parts.

6.3.1 Sensor arrays

There are three sensor arrays in the analogue part. Each array is used to convert one of the primary colours (green, red and blue) into corresponding electrical signal.The three arrays have the same architecture, as ASIS-1011. The light area in each array consists of 305 × 240 photodiodes, schematically indicated by columns and rows of individual photodiodes. The pixel size is 10.5 × 10 μm^2, giving a light sensing area of 3.20 × 2.40 mm^2.

There are 321 × 244 pixels in the green sensor array. The bottom three lines are black pixels; we use the middle line for black calibration. At the top of the array we put an extra line pixels to minimise edge effects. There are eight extra pixels at the left and right sides of the array. The light sensing area of the green array is 305 × 240 pixels in the middle array.

There are 321 × 256 pixels in the red and the blue sensor array. The light sensing area of both is the same as that in the green, but can be programmably moved in four directions. The extra pixels are used to provide the required extra space.

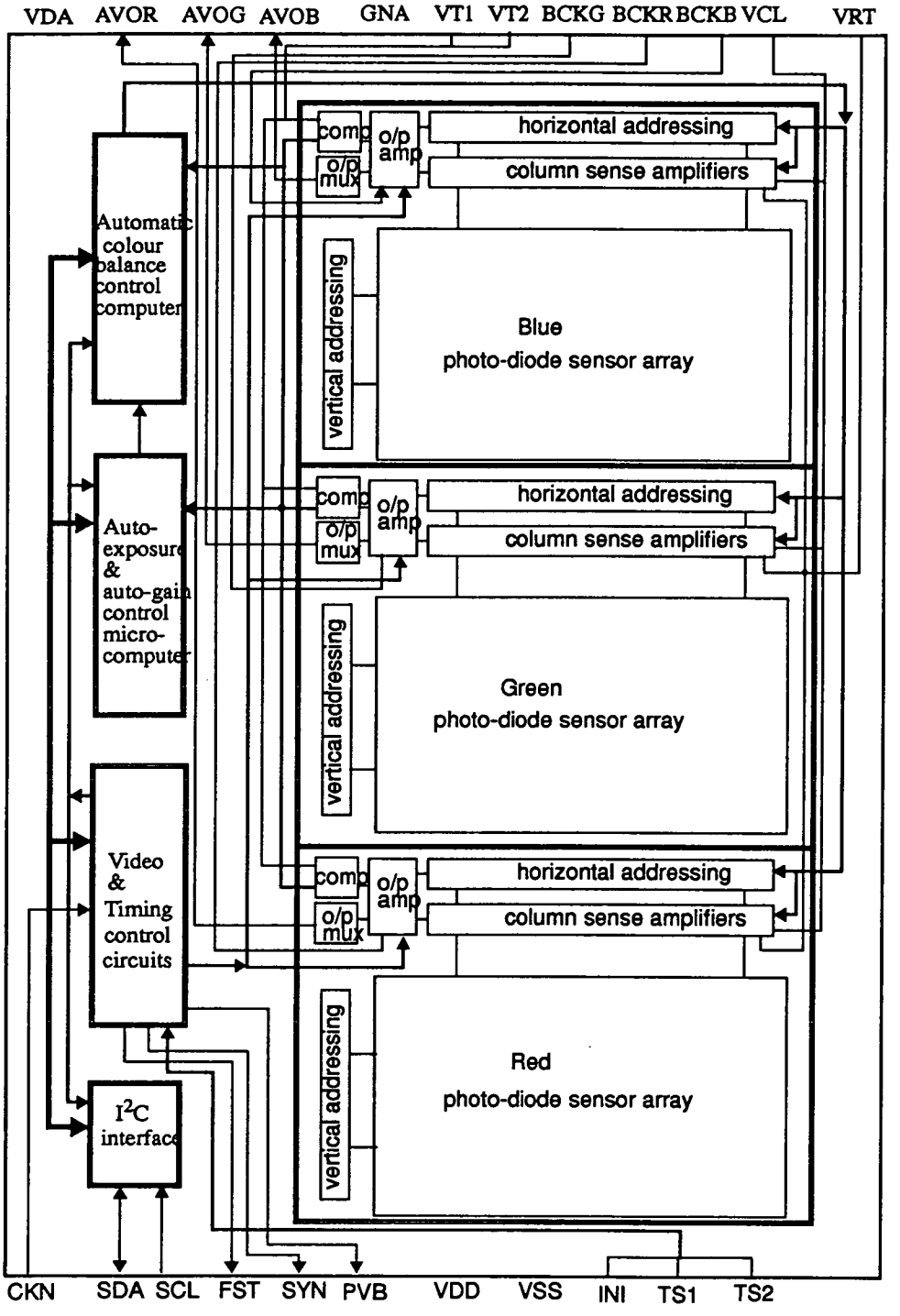

Figure 6.5. Architecture of ASIS-3000 colour camera devices.

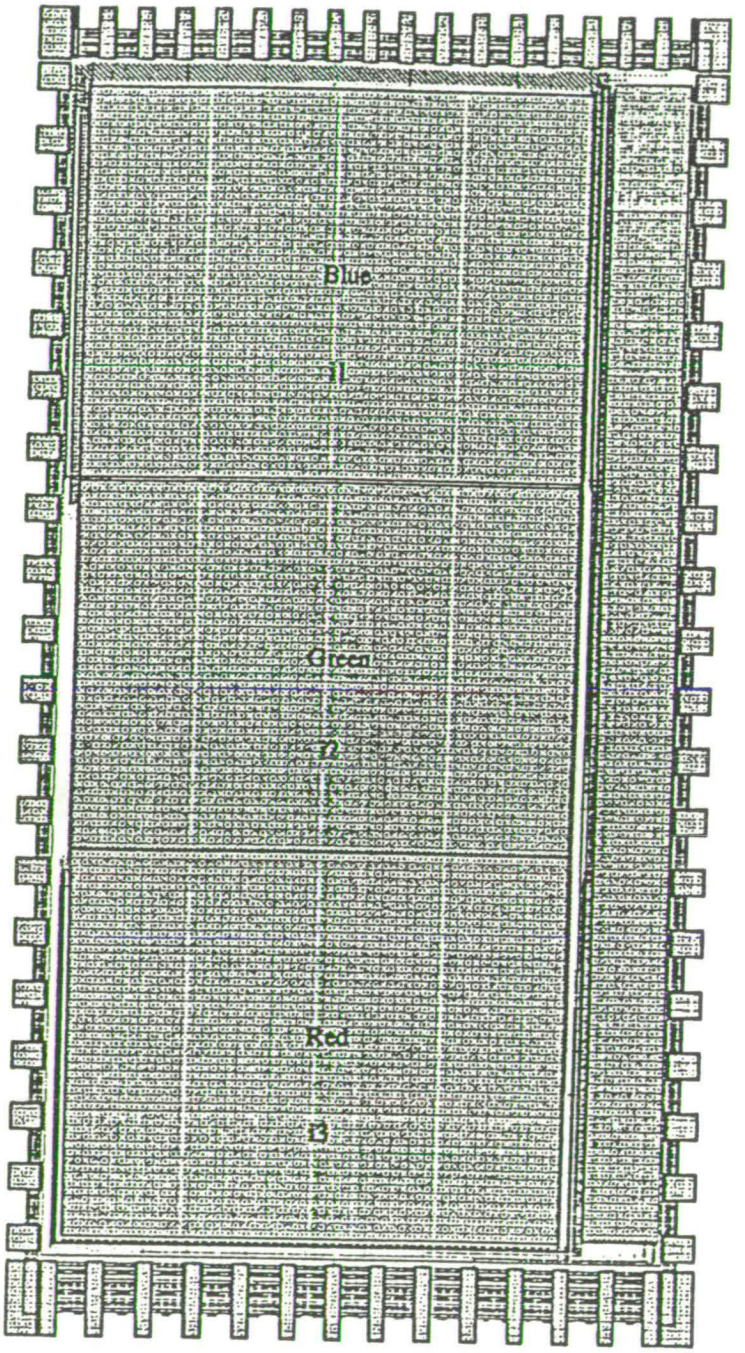

Figure 6.6. Layout of ASIS-3000 colour camera devices.

6.3.2 Video timing generator block

This part generates the operational timing requirement for the three sensors and the automatic controllers. Each of the RGB signals is individually output as a monochrome EIA 525/60 video formatted signal. The optical centre registration function is included in the video timing block. The logic function was implemented using about 1500 gates in this block. The detailed logic circuit has been described in Chapter 5.

6.3.3 Automatic exposure & gain Control

The device has automatic exposure control over a range 3000 : 1. The maximum integration time of the pixels can be as long as one field period, or as short as 6μs. Under low light conditions, after the integration time has reached to the maximum, if the picture is still judged to be too dark, then the controller starts to increase gain. The gain value can be varied from the nominal value up by a further 10dB. Therefore the auto-gain function is a further extension of dynamic range.

The control algorithm for auto-exposure and auto-gain, described in Chapter 3, works by monitoring the video stream of colour pixels, combined by oring R,G,B primary pixels whose level is over threshold voltages, V2 and V3. V2 is the "under exposure threshold", V3 is the "very bright exposure threshold". If the number of very bright colour pixels is more than 2% of total pixel number, the exposure controller decreases the integration time of the arrays. If the number of under exposure colour pixel is less than 1% of total pixel number, the exposure controller will increase the integration time.

The integration time is varied if necessary, in steps of 6.25% in the appropriate direction until correct exposure is obtained. In order to cooperate with the colour balance controller, the exposure controller is always given higher priority to act first if the both controllers want to have action.

V2 and V3 thresholds can be adjusted externally to offer more flexibility over the control function during characterising the device.

Both AEC and AGC functions are optional. The functions can be switched off by writing configuration bits to the device through the serial interface. New integration time and gain can also be set externally through the interface.

6.3.4 Automatic colour balance controller

Automatic colour balance control is expected to cover a range from 3000k to 10,000K colour temperature of light sources, as calculated in Chapter 4. This is a mechanism for correcting colour distortion of the picture caused by spectral variation of the light source. The colour balance judgement algorithm works by monitoring the top level of each primary pixel stream. Using the peak level of the green pixels as a comparison reference if the peak levels of the red or blue pixels are higher than the green, the controller will decrease offset gain of the red or blue channel. If the peak level of the red or blue is lower than the green, the controller will increase the offset gain of the channel until the peak level of the three primary signals are equal each other. The colour picture is judged as well-balanced if the peak levels of the three primaries are equal to each other, in the same band. The offset gain is varied if necessary, in steps of less than 7%, in the appropriate direction and channels.

Tolerance of the colour balance is set less than 8% internally. Externally the several threshold voltages can be adjusted to change the tolerance value and offer more flexibility in auto-colour balance control.

6.3.5 Automatic black calibration

The device automatically calibrates the video black level using the method described in Chapter 5. It is very important to obtain black balance in the three channels, that is, equal black level. Three extra lines of "black pixels" are added at the bottom of the green photo array, of which the middle line is used for calibration. The black pixels are shielded by a third layer metal on the surface of the chip. Calibration occurs every field. The calibrated black voltage is actually shared between the three channels to make the black levels of the three channels identical.

The black calibration function can be switched off by pulling pin IBC to ground. The black voltage level of the three channels can then be set individuality by adjusting the voltage on pins BCKG, BCKR, BCKB.

6.3.6 Camera interface

The camera interface is realized by a serial interface which allows a host computer or a micro-processor to interact with camera devices. The functions which can be inhibited by host computers include AEC, AGC, ACB.

Then the exposure value and gain value for each individual channel can be written into the camera device through the serial interface. The data format and address are shown in Figure 6.7.

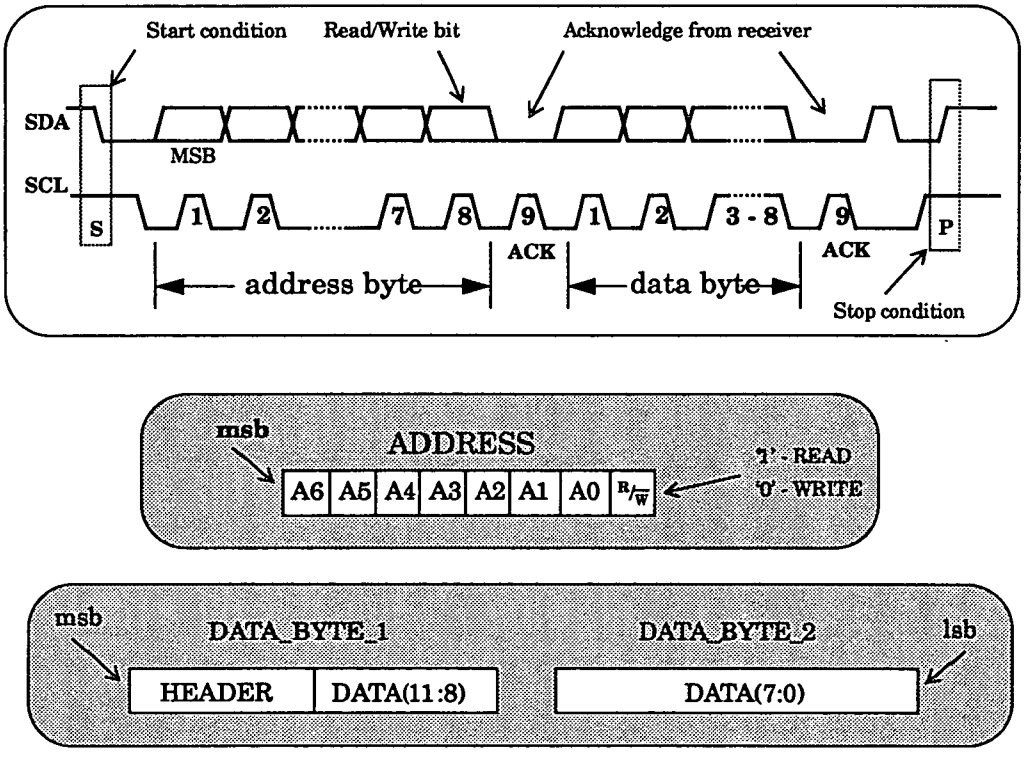

Figure 6.7. The format of the serial interface.

The address, 20H, is hardwired into the camera logic. The write data is formed into two bytes. A 4 bit header in the first byte is used by the camera to determine the destination of the 12 bit message following the header. Figure 6.8. shows the camera's interpretation of the header code and the set-up code message. Defaults for each control bit are built in to the camera's initialisation cycle, and may be changed on-the-fly under host control. The range of value following header is shown in Figure 6.9.

Header Code

Table 1:

Header	Interpretation
0000	(free)
0001	Set up code to follow
0010	Exposure value to follow
0011	Gain value to follow
0100	Red gain offset value to follow
0101	Blue gain offset value to follow
0110	Blue & red centre X offset value to follow
0111	Blue & red centre Y offset value to follow
1xxx	(free)

Set-Up Code

Table 1:

Bit	Function
0	free
1	free
2	AGC on/off
3	free
4	AEC on/off
5	Ch'q board on/off
6	free
7	free
8	free
9	AWC on/off
10	free

Figure 6.8. The header code and set up code.

Header	Data (12-bit)			
0010	0 - 260 (9-bit)		0 - 5 (3-bit)	exposure value: coarse / fine
0011	free (4-bit)	free	0 - 112 (7-bit)	green gain value
0100	free (4-bit)	sign bit	0 - 112 (7-bit)	red gain offset
0101	free (4-bit)	+ / - 0 / 1	0 - 112 (7-bit)	blue gain offset
0110	free (4-bit)	0-15(4-bit)	0-15(4-bit)	blue, red centre x offsets
0111	free (4-bit)	0-15(4-bit)	0-15(4-bit)	blue, red centre y offsets

Figure 6.9. The range of the parameters of the camera control.

This function make ASIS-3000 camera devices more flexible to apply different AEC, AGC, ACB control algorithms afterward.

6.3.7 Main features

Main features of the chip are:

- three arrays of 305 x 240 pixels
- aspect ratio 4:3
- 10.5 x 10 μm^2 pixel size
- automatic exposure control (dynamic range 3000:1)
- automatic gain control (up to 10 dB)
- automatic colour balance control

- automatic black calibration
- NTSC-standard RGB video output
- camera interactive
- power consumption < 500mw

Apendix 2 lists pads of ASIS-3000.

6.4 Chapter summary

The two main implementations of single chip camera devices have been described in this chapter.

The single chip monochrome camera device with medium resolution has been assembly with a few off-chip components on a printed circuit board of 30 mm diameter to form a "peach" miniature video camera product.

The single chip colour camera device was designed as a prototype to demonstrate how our CMOS VLSI camera techniques transfer from the monochrome solution to a colour solution. The design did not go to fabrication because of perceived problems in manufacturing the triple lens with 2-elements per lens. Single-element plastic lenses can not deliver the required (320 x 240) pixel resolution.

Most techniques developed for this colour chip are useful and transferable to the alternative colour camera structure -- single sensor array with colour mosaic filters covering the pixels. This structure will be described in the next chapter.

Chapter7 Future Research Opportunities and Conclusions

From the characterization of ASIS-1011, and the design review of ASIS-3000, it is obvious that further research is required. This chapter discusses possible improvement for exposure judgement algorithm. A new scheme to implement single chip colour camera devices will also be discussed.

7.1 Improvement on exposure judgement algorithm

The exposure algorithm introduced in Chapter 3 works quite well, as ASIS-1011 has shown. However, there are two problems.

The first problem is oscillation on flat grey scenes. The pixel output level of flat grey scenes is in a very narrow band of the normal output range. The images will be judged as over-exposed if this narrow band is above the white pixel threshold voltage and as under-exposed if the narrow band is below the white threshold. Thus flat grey scenes have difficulty to come into the stable area in the exposure algorithm of Figure 3.7.

The second problem is the slow convergence following a major light intensity change. Because the exposure step size is fixed at 1/16 it takes 7 seconds to change exposure setting from the minimum to the maximum.

Improvements can be achieved by the following methods:

1. An oscillation detector can be added to detect the occurrence of oscillation (from under-exposure to over-exposure in adjacent frames) and set the step size smaller than normal, then the stable area in Figure 3.7 can be more easily reached. A release of the special state can be triggered if the over-exposure to under exposure state is detected in adjacent frames.

2. In some applications, there may be a requirement for fast convergence if the light intensity suddenly varies by more than 10 times. To cope with this requirement, we

need to partition the brightness of the image into more complex ranges, instead of only having three results: under-, over-, and right-exposure. Adaptive step size for changing exposure can be taken according to the ranges.

For example, an algorithm based on controlling the median of the image (the threshold at which the image would be half black and half white) has been proposed [Denyer, 1993]. By experiment the median of a well exposed image lies close to the 50% of white level, we use it as target level. This target is combined with an adaptive step size which is linked to the error of the current median. Values which are far from the target level cause larger steps to be used in changing exposure.

7.2 Single chip digital colour video camera device

The three sensor array colour scheme has been abandoned because of cost and difficulty of manufacturing the triple lenses.

A real solution for achieving colour sensors for CMOS vision technology is to use a single array with colour mosaic filters to cover the surface of the sensor. Full RGB colour data for every pixel can then be restored by colour interpolation [Parulski, 1991]. By means of A/D conversion, image processing can be implemented much more easily in digital mode than in analogue mode. At the final stage, the colour image data is converted back to analogue signals using D/A data convertors.

A diagram of proposed architecture for digital colour video camera devices is shown in Figure 7.1. The following sections cover the main technical points.

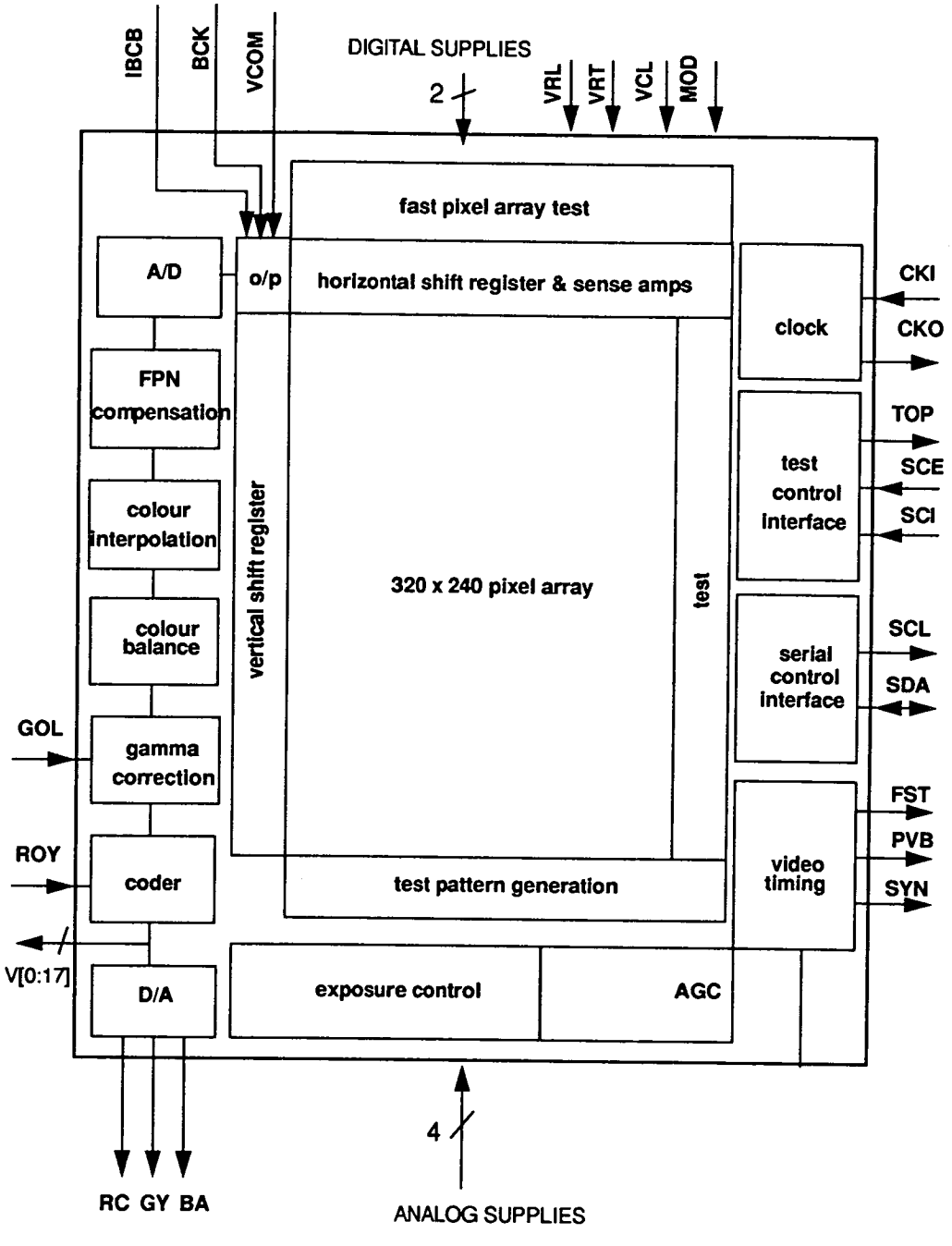

Figure 7.1. Architecture of ASIS-3010 camera device.

7.2.1 Single pixel colour array with colour mosaic filter

Most commercial solid state colour cameras use this scheme but with different arrangements & choices of colour filters. For example White, Yellow, Cyan colour filters can transmit more light intensity than R, G, B filters but more circuitry is needed for signal processing.

Since our proprietary colour balance algorithm chooses the green signal as the reference for balance judgement, as explained in Chapter 4, we have to chose RGB colour filters. Fortunately filter material for making RGB colour filter is commercially available now. The filter layers can be developed on wafer after the completion of the CMOS process.

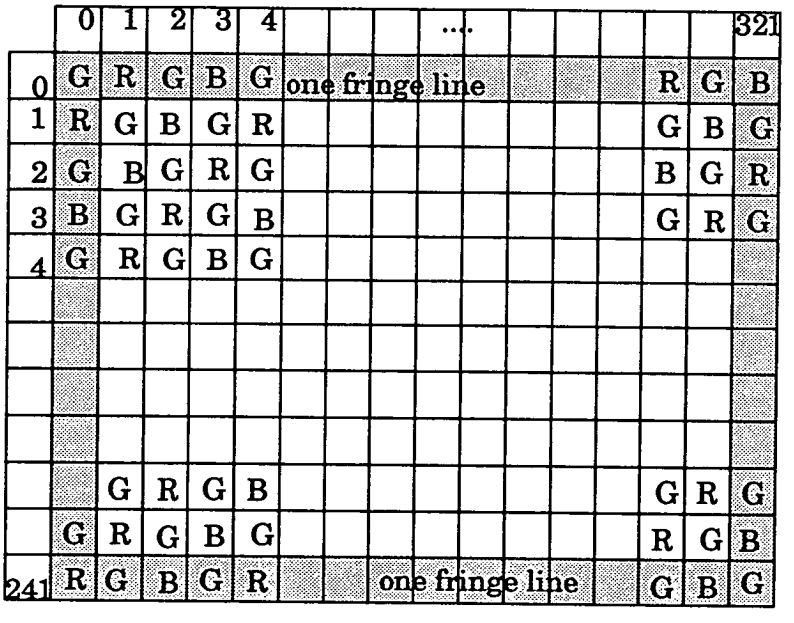

Figure 7.2. The proposed colour mosaic filter structure.

The RGB colour filter structure has been investigated here [Henry, 1994]. It is one alternative version of the Bayer colour filter structure. Half of pixel array is populated

with green pixels, with the remainder of the array being split between red and blue. Figure 7.2 shows the proposed colour filter structure.

7.2.2 Video speed A/D convertor

Digital signal processing is a much more desirable way to achieve a stable and repeatable result of video signal processing. For the new digital colour camera solution we need a on chip 6MHz 7bit A/D convertor.

Video speed A/D convertors can be implemented using the parallel or flash architecture, to achieve short conversion times. The ultimate conversion speed is one pixel clock cycle, 170ns for ASIS-3010, which would typically consist of a set-up and convert phase. There could be compromise between the speed and area. Another method of improving the speed of the converter is to increase the speed of the individual components.

7.2.3 Colour array interpolation technique

The colour array interpolation technique is used to restore three colour image array data from the single filtered colour image array. Generally adjacent pixels are always used for interpolating missing pixels. Interpolation of missing pixels could be formed by averaging the levels of the adjacent pixels or assigning a neighbouring pixel level to the missing one. The objective here is to satisfy the eye and be able to be relatively easily implement the hardware by digital signal processing.

7.2.4 Colour balance controller

In order to suit a purely digital signal processing method the colour balance controller hardware implementation needs to be modified. In ASIS-3000 the gain of the red and blue channels controlled by the colour balance algorithm is performed by the gain in the MDAC stage of the output amplifier. In ASIS-3010 the MDAC of the single array is used for high gain control so that the offset gain should be implemented in an alternative way. Figure 7.3 shows a proposed block diagram of the colour balance

controller. The gain setting is implemented by employing a multiplier. A linear gain control can be achieved in this way.

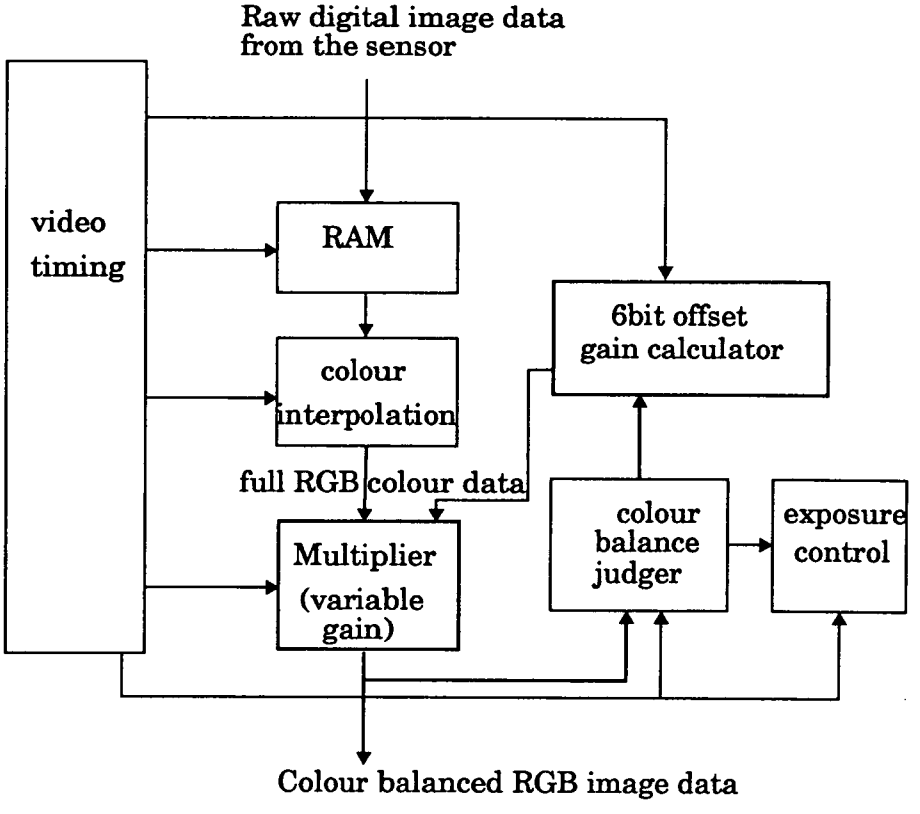

Figure 7.3. Digital colour balance controller block.

7.2.5 Gamma correction

In the previous single chip camera devices an analogue gamma correction circuitry was used [Wang, 1993]. It is a simple solution but does not match well with video standards.

Gamma correction can be more accurately done again by using digital processing. For example, an on-chip ROM look-up table can be used in a straight forward way to give the gamma I/O curve [Trundle, 1987]. The three RGB data can share one ROM look-up table by an time division modulator (TDM).

7.2.6 Fixed pattern noise compensation

Fixed pattern noise is the most serious problem in the image produced by component mismatches in the sense amplifiers. It looks as if some brighter or darker stripes are added on to an uniform image picture. An analogue method has been used to reduce FPN [Wang, 1991], which did reduce the ratio of the N/S but it is still not good enough.

A digital FPN compensation scheme can be used to reduce FPN further (Figure 7.4). Basically it may be implemented by a RAM and an adder. The RAM is used to store the digital data for column compensation. The stored digital value is written into the RAM after a post-characterisation procedure for each individual device. Then when a row of pixels is read out from the output of the A/D, the level of the pixel is added to a corresponding stored digital number, which will make the stripes of the image finally disappear. The compensation digital number of the RAM can be written through serial interface from a microprocessor chip.

With a digital FPN compensation scheme, we aim to achieve -50dB on N/S ratio.

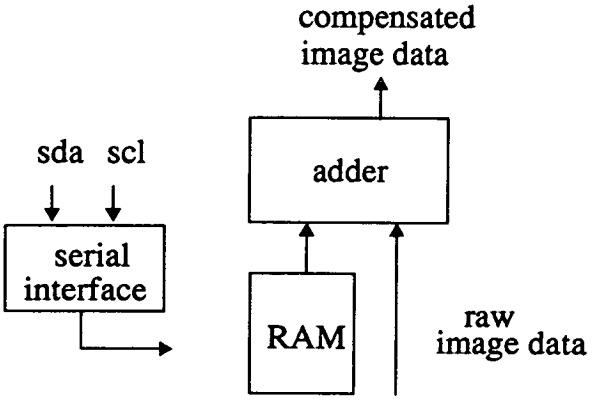

Figure 7.4. Digital compensation to reduce FPN.

7.3 Conclusions

This thesis has presented basic techniques to include control functions on chip together with a sensor array. These main control functions include:

- automatic exposure control
- automatic gain control
- composite TV signal formatting
- automatically colour balance
- serial interface.

The main achievements and original contributions of the author were:

- on chip automatic exposure and gain control technique
- on chip digital automatic colour balance control technique
- implementation of digital functions in CMOS single chip video cameras.

The digital automatic colour balance control technique is an entirely novel method in this field, no similar method has been seen reported before. The on chip automatic exposure and gain control provide both maker and user of video cameras an easier way to have these functions without any extra cost. All of these successfully implemented control functions were important steps in realizing commercial products from the research reported here and in [Wang, 1993].

Several monochrome single chip cameras have been implemented with most of the above functions. One such cameras, named ASIS-1011, has been presented. All on chip control logic only occupies 15% of the chip area.

A high level integrated colour video chip, named ASIS-3000, has been designed. This device, which also includes all the above functions was not fabricated, because of the problem of lens production. However, experiment has shown the colour balance algorithm works better than some commercial available colour cameras; simulation has confirmed all the expected waveforms, and the layout work has been completed. This shows that all on chip control logic only occupies about 10% of the chip area.

This thesis then proposed a modified scheme to achieve a single chip digital colour video camera. This device named ASIS-3010 will use a single photodiode array covered by mosaic colour filters. Therefore, there is no requirement for a special lens. The device will also perform most control functions digitally.

Based on these facts:

- most control functions listed above have been integrated and proven to work well,
- all the above functions can be put in one chip and only occupy a small fraction of chip area,
- such controls functions can be further enhanced by a proposed digital processing scheme,

we can conclude that:

more powerful vision application systems can be highly integrated using CMOS technology. These applications will certainly enjoy

- greatly reduced size,
- greatly reduced power consumption,
- greatly reduced cost.

These advantages are relevant to many applications in the vision marketplace, but nowhere so much as in personal computing and telecommunications, where multi-media applications are growing.

We see a new capability that extends the CMOS ASIC marketplace in a sector of high growth rates, and expect it to be substantial and likely to change the nature of the vision market fundamentally.

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Appendix 1

ASIS-1011 pads List

VDD	Digital power.
VD1	Analogue power (array and column sense amplifiers).
VD2	Analogue power (output amplifier and buffer).
VD3	Analogue power (row access drivers).
GND	Digital ground.
GN1	Analogue ground (array and column sense amplifiers).
GN2	Analogue ground (output amplifier and buffer).
GN3	Analogue ground (row access drivers).
VRT	Pixel reset level. Drive externally.
CVO	Composite video output.
PVB	Pixel valid (bar) clock output. Used for external image capture. Video signal should be sampled on falling edge of PVB. (Valid over 312 x 287 pixels).
HLD	Input pad to hold exposure. Freezes the current internal exposure value. HLD=1 to enable continuous automatic exposure evaluation.
AGC	Input pad to enable AGC circuit. AGC = 0 to inhibit AGC function. The AGC circuit requires automatic black-level calibration for correct operation.
FST	Field-start output. Used for frame grabbing.
ITS	Input pad to select integration threshold. Controls sensitivity parameter in automatic exposure control algorithm. Typically ITS = 0, selecting the larger gap in the integration threshold algorithm.
CPE	Input pad to enable central 256 x 256 pixel output clock on TAE pad when CPE = 0.

TAE	Test output from auto-exposure and gain computer when CPE = 1. Central pixel output clock when CPE = 0.
SYN	Frame synchronization input, active on falling edge.
CKI	Oscillator input pad.
CKO	Oscillator output pad.
MAX	Input pad to force maximum exposure when MAX = 1.
IBC	Input pad to inhibit black-level calibration when IBC = 1. Auto black-level calibration must not be inhibited if AGC circuit is in operation.
VCL	Analogue input pad to provide sense amplifier calibration voltage.
ITT	Precharge word line test input. Active low.
TOP	Word line test output.
TS1	Input pad enable bit line test vector 1 (101010... is forced onto bit lines).
TS2	Input pad to enable bit line test vector 2 (010101... is forced onto bit lines).
INI	Input pad to initialises the device when high.
PCLK	Pixel clock input for horizontal shift register.
LS	Input to horizontal shift register. Starts horizontal scan.
CVI	Line clock input (to vertical shift register), also balances column sense amplifiers.
FI	Input to vertical shift register. Duration determines coarse exposure time.
RST	Resets photodiodes in selected row(s). Duration determines fine exposure time.
SAM	Control input to sample column sense amplifiers.
REBIT	Resets bit-lines to alleviate antiblooming outside sensing period.

CAL Input enables calibration of column sense amplifiers.

GB[1:7] MDAC input coefficient in output stage. Active low. MSB is GS7.

SS Input selects sync level at AVO.

SI Input selects sensor output (video) at AVO.

N.B. Blanking level appears at AVO when SS,SI = 0.

BRE Input enables automatic black-level calibration.

IBC Inhibit automatic black level calibration, use BCK instead.

BCK Analogue black level adjustment. Nominal value (1.5 v) set within part 1, but may be overidden externally when IBC = 0.

LOG Selects linear analogue output characteristic (1 -> gamma = 1.0) or gamma-corrected (0 -> gamma = 2.1).

VWT Threshold for very white pixels. Nominal value (2.15 v for gamma, 1.6 v for linear) set within part 1, but may be overidden externally.

VBT Threshold for very black pixels. Nominal value (1.86 v) set within part 1, but may be overidden externally.

CPO Very white pixel comparator output. CPO=1 when sensor output > VWT.

VBP Very black pixel comparator output. VBP=1 when sensor output < VBT.

GC1 Gain control for the first sensing stage.

GC2 Gain control for the second sensing stage.

Appendix 2

ASIS-3000 pads list

VDDC	power	Digital power for core.
GNDC	power	Digital ground for core.
VDDP	power	Digital power for pads.
GNDP	power	Digital ground for pads.
GNG	grnd	lens support (connect to ground)
GNO	grnd	optical shield (connect to ground)
CKN	clock	Clock input. Nominal frequency = 14.31818MHz (4 x fsc).
SCL	I^2C	Serial bus clock (input only)
SDA	I^2C	Serial bus data (bidirectional, open drain)
FST	OD[1]	Field start. Synchronises external image capture for image capture purposes.
PVB	OD	Pixel valid (bar) clock. Qualifies video output for external image capture. Video signal should be sampled on falling edge of PVB.
SYNC	OD	Synchronization output. Connects to SYNC pin on AD 720 colour encoder device
TS1	ID	Chip test code.
TS2	ID	Chip test code. Normal operating when ts1 =1, ts2 = 1.
INI	ID	Initiation of the chip.
VDA	power	Analogue power.

1. OD: digital output pad 2. ID: digital input pad. 3. A: analogue bias pads 4. clock: clock input.

GNA	power	Analogue ground.
VT1	A	Threshold 1. Bias generated on chip, nominal value 2.78v.
VT2	A	Threshold 2. Bias generated on chip, nominal value 2.68v.
BCKG	A	Black Reference storage point. Requires external 1 nF ceramic decoupling capacitor.
BCKB	A	Black Reference storage point. Requires external 1 nF ceramic decoupling capacitor.
BCKR	A	Black Reference storage point. Requires external 1 nF ceramic decoupling capacitor. BCKG, BCKR and BCKB are connected togather externally when auto-balck calibration function is in use. BCKG, BCKR, BCKB are also able to be set externally by providing an adjustable DC voltage to each of them, nominal value is 1.85v.
VRT	A	Sensor array reset voltage. Generated on chip by setting the value of VRI. Requires external decoupling capacitor.
VCL	A	Sense amplifier calibration voltage. Generated on chip, nominal value = 2.20v. Requires external decoupling capacitor.
CVOG	OA	Analogue composite video gamma output of the green channel.
CVOR	OA	Analogue composite video gamma output of the red channel.
CVOB	OA	Analogue composite video gamma output of the blue channel.

Appendix 3

Colour balance & exposure algorithm in C program

```
#include <stdio.h>
#include <stdlib.h>
#include <math.h>
#include "defs.h"
#include "image.h"

FILE *ifile;
FILE *ofile;

byte R[ROWS][COLS];
byte G[ROWS][COLS];
byte B[ROWS][COLS];
int Rpeakpos[2];
int Gpeakpos[2];
int Bpeakpos[2];

byte trunc(int x)
/* Clips numbers to within the range [0,255]      */
/*  If x > 255 then x is set to 255               */
/*  If x < 0 then x is set to 0                   */
{
        if (x>255) x=255;
        if (x<=0)  x=0;

        return(x);
}

void exposure ()
/* Performs autoexposure algorithm */
{

        byte exp_ok;        /*Indicates correct  exposure(1) or not (0) */
        int N1, N2, r, c, i;
        double expinc;                          /*Exposure increment/
decrement */

        expinc = 0.06;                          /*Set exposure inc/
decrement*/
        i=0;                                            /*Count
loops*/
```

```
do {
                exp_ok = 1;                    /*Assume exposure is
OK, unless algorithm decides not*/
                N1 = 0;        /*Histogram Binning */
                N2 = 0;
                for( r = 0; r < ROWS; r++ ) {
                for( c = 0; c < COLS; c++ ) {
                                                if ( (R[r][c]>246) ||
(G[r][c]>246) || (B[r][c]>246) ) N1++;
                                                if ( (R[r][c]>227) ||
(G[r][c]>227) || (B[r][c]>227) ) N2++;
                }
                }
                if (N1>768) {
                /* Overexposed */
                                for( r = 0; r < ROWS; r++ ) {
                                for( c = 0; c < COLS; c++ ) {        Decrease
exposure */
                                                                R[r][c] =
trunc( (1-expinc)*(int)R[r][c]);
                                                                G[r][c] =
trunc( (1-expinc)*(int)G[r][c]);
                                                                B[r][c] =
trunc( (1-expinc)*(int)B[r][c]);
                                                                exp_ok =
0;
                                }
                                }
                }
                else if (N2<768) {
                /* Underexposed */
                                for( r = 0; r < ROWS; r++ ) {
                                for( c = 0; c < COLS; c++ ) {        Increase
exposure */
                                                                R[r][c] =
trunc( (1+expinc)*(int)R[r][c]);
                                                                G[r][c] =
trunc( (1+expinc)*(int)G[r][c]);
                                                                B[r][c] =
trunc( (1+expinc)*(int)B[r][c]);
                                                                exp_ok =
0;
                                }
                                }
                }
                printf("  Exposure loop %d \n",++i);
```

```
        } while (!(exp_ok));
}

byte band( byte x)
/* Determines which histogram band the pixel value (x) is in */
{
        byte retval;

        if (x<208)
                retval = 1;
        else if ((x>=208) && (x<227))
                retval = 2;
        else if ((x>=227) && (x<246))
                retval = 3;
        else if ((x>=246) && (x<255))
                retval = 4;
        else
                retval = 5;

        return(retval);
}


void peak ( byte (*RGBarray)[ROWS][COLS], int (*RGBpos)[2])
/* Locates peak value in array <*RGBarray>, and writes row and */
/* column value of this peak to <*RGBpos>                      */
{
        byte peakval;
        int rowpos, colpos, r, c;

        peakval = 0;

        for (r=0; r<ROWS; r++) {
                for (c=0; c<COLS; c++) {
                        if ((*RGBarray)[r][c] > peakval) {
                                peakval =
(*RGBarray)[r][c];
                                rowpos = r;
                                colpos = c;
                        }
                }
        }

        (*RGBpos)[0] = rowpos;
        (*RGBpos)[1] = colpos;
```

```
}


main(int argc, char *argv[] )
{
        long count;
        char infilename1[100];
        int arg, r, c, i;
        byte bal_ok;                                    /*
Indicates correctly balanced image (1) or not (0) */
        byte Gpeak, Rpeak, Bpeak;   /* Peak values in RGB arrays */
        byte R_Gpeak, B_Gpeak;                  /* Values of R and B at
green peak pixel */
        double colinc;                                  /* Colour
balance increment/decrement */

/* Check that one argument is given */
        if (argc != 3) {
                printf("Usage: cb1 <input image> <output image>\n");
                exit(1);
        }
/* Check that file exists; if it does read data into RGB arrays */
        arg = 1;
        strcpy(infilename1,argv[arg]);

        if( (ifile = fopen( infilename1, "r" )) == NULL ) {
                printf(" cb1: failed to open %s - Exiting\n", infilename1
);
                exit(1);
        }
        else
                printf(" cb1: %s opened OK\n", infilename1 );

        count = fread( R, 8, (long)ROWS*(COLS/8), ifile);
        count = fread( G, 8, (long)ROWS*(COLS/8), ifile);
        count = fread( B, 8, (long)ROWS*(COLS/8), ifile);

        count = count * 8 * 3;
        printf(" cb1: read %lu bytes from %s\n", count, infilename1);
        fclose(ifile);

/* Perform colour balance algorithm */
        printf(" cb1: performing colour balance algorithm\n");

        colinc = 0.25;
        i=0;
```

```
                                        /*Count loops*/
            do {
                        bal_ok = 1;
                        /*Assume colour balance OK*/
                        exposure();
                        peak (&G, &Gpeakpos);
            /*Find Green Peak */
                        Gpeak = G[ Gpeakpos[0] ][ Gpeakpos[1] ];
                        R_Gpeak = R[ Gpeakpos[0] ][ Gpeakpos[1] ];/*Note R
at Green Peak*/
                        B_Gpeak = B[ Gpeakpos[0] ][ Gpeakpos[1] ];/*Note B
at Green Peak*/
                        if ( (band(B_Gpeak)>band(Gpeak)) &&
(band(R_Gpeak)>band(Gpeak)) ) {
                                    for( r = 0; r < ROWS; r++ ) {
                                                for( c = 0; c < COLS; c++
) {
                                                            R[r][c] =
trunc((1-colinc)*(int)R[r][c]);
                                                            B[r][c] =
trunc((1-colinc)*(int)B[r][c]);
                                                }
                                    }
                                    bal_ok = 0;
                        }
                        else if ( (band(B_Gpeak)>band(Gpeak)) &&
(band(R_Gpeak)<=band(Gpeak)) ) {
                                    for( r = 0; r < ROWS; r++ ) {
                                                for( c = 0; c < COLS; c++
) {
                                                            B[r][c] =
trunc((1-colinc)*(int)B[r][c]);
                                                }
                                    }
                                    peak (&R, &Rpeakpos);
                                    Rpeak = R[ Rpeakpos[0] ][ Rpeakpos[1]
];
                                    if (band(Rpeak)<band(Gpeak)) {
                                                for( r = 0; r < ROWS; r++
) {
                                                            for( c = 0; c
< COLS; c++ ) {

            R[r][c] = trunc((1+colinc)*(int)R[r][c]);
                                                            }
                                                }
```

```
                                        }
                                        bal_ok = 0;
                                }
                                else if ( (band(B_Gpeak)<=band(Gpeak)) &&
(band(R_Gpeak)>band(Gpeak)) ) {
                                        for( r = 0; r < ROWS; r++ ) {
                                                for( c = 0; c < COLS; c++
) {
                                                        R[r][c] =
trunc((1-colinc)*(int)R[r][c]);
                                                }
                                        }
                                        peak (&B, &Bpeakpos);
                                        Bpeak = B[ Bpeakpos[0] ][ Bpeakpos[1]
];
                                        if (band(Bpeak)<band(Gpeak)) {
                                                for( r = 0; r < ROWS; r++
) {
                                                        for( c = 0; c
< COLS; c++ ) {

                B[r][c] = trunc((1+colinc)*(int)B[r][c]);
                                                        }
                                                }
                                        }
                                        bal_ok = 0;
                                }
                                else if ( (band(B_Gpeak)<=band(Gpeak)) &&
(band(R_Gpeak)<=band(Gpeak)) ) {
                                        peak (&R, &Rpeakpos);
                                        peak (&B, &Bpeakpos);
                                        Rpeak = R[ Rpeakpos[0] ][ Rpeakpos[1]
];
                                        Bpeak = B[ Bpeakpos[0] ][ Bpeakpos[1]
];
                                        if (band(Bpeak)<band(Gpeak)) {
                                                for( r = 0; r < ROWS; r++
) {
                                                        for( c = 0; c
< COLS; c++ ) {

                B[r][c] = trunc((1+colinc)*(int)B[r][c]);
                                                        }
                                                }
                                        bal_ok = 0;
                                        }
```

```
                                        else if (band(Rpeak)<band(Gpeak)) {
                                                for( r = 0; r < ROWS; r++
) {
                                                                for( c = 0; c
< COLS; c++ ) {

                R[r][c] = trunc((1+colinc)*(int)R[r][c]);
                                                                }
                                                }
                                        bal_ok = 0;
                                        }
                        }
                        printf("   Colour Balance Loop %d\n\n",++i);
                } while (!(bal_ok));


/* Output RGB data to file */
                printf(" cb1: writing RGB arrays to file\n");
                ofile = fopen (argv[2], "w");
                for( r = 0; r < ROWS; r++ ) {
                        for( c = 0; c < COLS; c++ ) {
                                fprintf(ofile, "%c",R[r][c]);
                }
                }
                for( r = 0; r < ROWS; r++ ) {
                for( c = 0; c < COLS; c++ ) {
                                fprintf(ofile, "%c",G[r][c]);
                }
                }
                for( r = 0; r < ROWS; r++ ) {
                for( c = 0; c < COLS; c++ ) {
                                fprintf(ofile, "%c",B[r][c]);
                }
                }
                fclose(ofile);

/* Exit */
                exit(0);
}
```

Appendix 4

Publications and patents

Publications:

1. M. Lu, G.Wang, D.Renshaw, and P.B.Denyer, "On-chip Automatic Exposure Control Technique", *Proc. ESSCIRC'91*, pp.281-284.

   This paper won the "*Best Paper Award*" in the conference.

2. P.B.Denyer, D.Renshaw, G.Wang, and M.Lu, "CMOS Image Sensors for Multimedia Applications", *Proc. IEEE CICC 93*, San Diego, 11.5.1

3. G.Wang, P.B.Denyer, D.Renshaw, and M.Lu, "A Simple Solution for Image Sensor Test", *Proc. ISIC-91*, Singapore, pp.202-205.

4. G.Wang, P.B.Denyer, D.Renshaw, and M.Lu, "CMOS Video Cameras", *Proc. EURO ASIC 91*, Paris, pp.100-103.

   This paper won the "*Best Circuit Award*" in the conference.

5. D.Renshaw, P.B.Denyer, M.Lu, and G.Wang, "A Single-chip Video Camera with On-chip Automatic Exposure Control", *Proc. ISIC-91*, Singapore, pp.346 -349.

6. P.B.Denyer, D.Renshaw, G.Wang, M.Lu, and S.Anderson, "On-chip CMOS Sensors for VLSI Imaging Systems", *Proc. VLSI 91*, Edinburgh, pp.4b1.1-1.10

7. D. Renshaw, P.Denyer, G.Wang, & M. Lu, "ASIC Vision", *Proc. IEEE Custom Integrated Circuits Conference*, 1990, pp 3038-3041.

8. D. Renshaw, P.Denyer, G.Wang, & M. Lu, "ASIC Image Sensors", *Proc. IEEE International Symposium on Circuits and Systems*, 1990, pp 7.3.1-7.3.4.

Patents:

1. M. Lu, P. B. Denyer, "Colour Balance", British Application NO: 932 1334.6.

2. P. B. Denyer, D. Renshaw, G. Wang, M. Lu, "Solid State Imaging Device", International Application Number: PCT/GB92/01522, International Publication Number: WO 93/04556, Publication Date: 04.03.93.

Appendix 5

Single chip camera devices list

Single chip camera devices, in which the control techniques described in this thesis have been used, are listed:

- ASIS-1011, 312 x 287 resolution with PAL video format, has been used for VVL's Peach camera series and Imputer.

- ASIS-1021, 160 x 100 resolution with PAL video format, has been used for the TVX security system for instant visual alarm verification by ASH PLC. Figure 1 shows the ASIS-1021 chip with LLCCC package, photo-micrograph of chip and TVX camera board.

- ASIS-1030, 128 x 128 resolution with anti-blooming pixel structure, has been used for aerospace experiments. Figure 2 shows the photo-micrograph of ASIS-1030 chip.

- ASIS-1031, 312 x287 resolution with anti-blooming pixel structure, has been used for aerospace experiments.

- ASIS-1060, 768 x 584 resolution with NTSC and PAL video format, which is being fabricated at TSMC, will be used for the pilot helmet project and for VVL's high resolution cameras. Figure 3 shows the layout of ASIS-1060 with a 84 LDCCC chip carrier.

- ASIS-3000, 305 x 240 resolution with NTSC video format, was designed for VVL's colour version camera. The new version of the design has been called ASIS-3010 because the scheme of colour sensors was changed,.

- ASIS-3010, 320 x240 resolution with NTSC video format, is being designed for VVL's colour camera.

- ASIS-3030, 369 x 287 resolution with PAL video format, is being designed for VVL's colour camera.

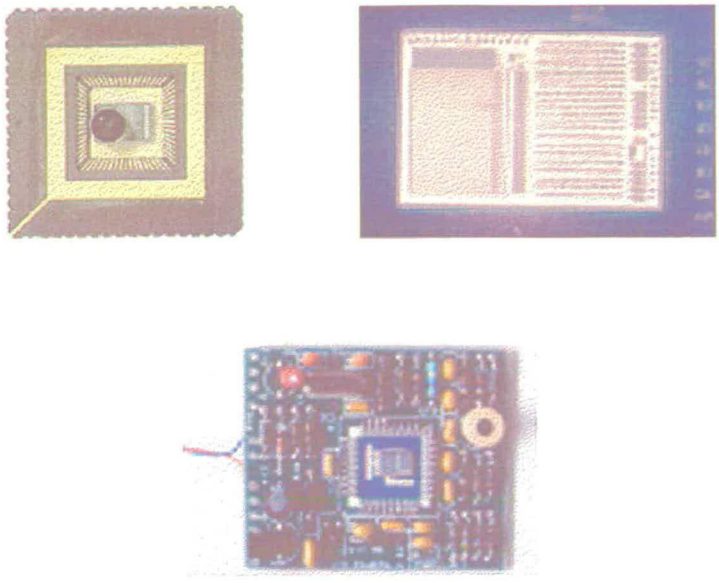

Figure 1. (a) *ASIS-1021 chip with LLCCC package*
(b) *photo-micrograph of ASIS-1021 chip*
(c) *TVX camera board*

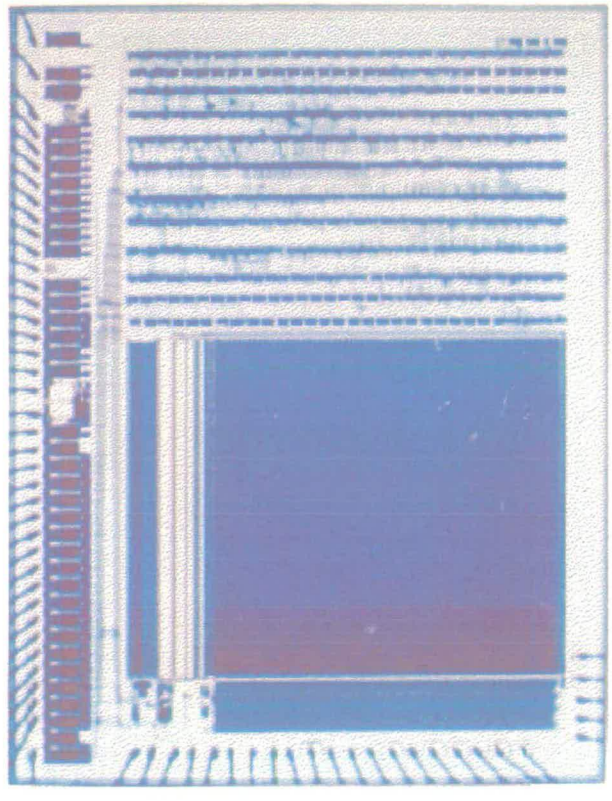

Figure 2. *photo-micrograph of ASIS-1030 chip*

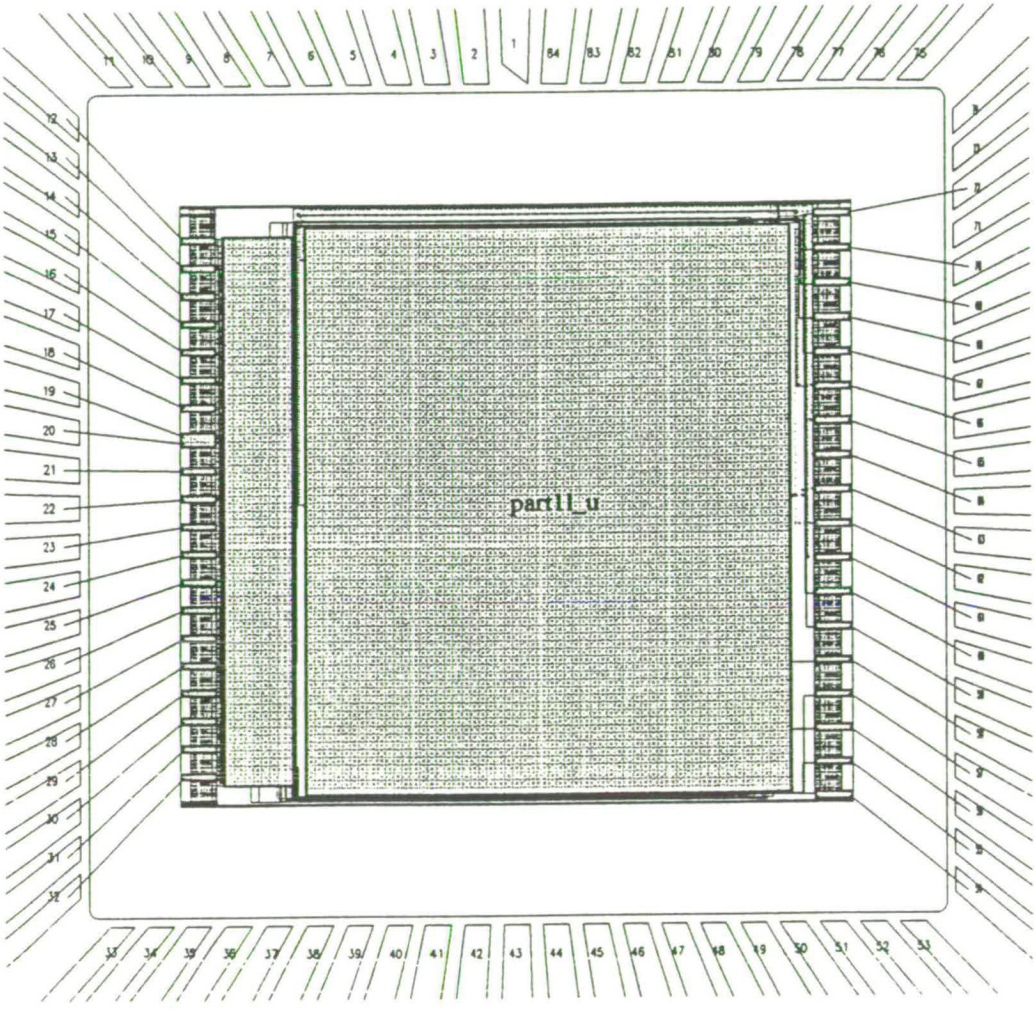

Figure 3. layout of ASIS-1060 with a LDCCC chip carrier.