Investigation of Voltage Injection Control for Power Supplies in Radar Applications

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Abstract

In radar applications, system performance depends strongly on the dynamic performance of its power supplies. The operations of the transmitter causes a step-current to be drawn from its power supply, leading to a transient voltage drop. The voltage must settle to within pre-specified limits, before the arrival of the echoed pulse signals from the target, to ensure the correct functionality of the radar receiver; otherwise, some of these pulses have to be rejected. Rejected pulses reduce the accuracy of the information of the target, causing system performance to deteriorate. It is therefore vital that radar power supplies have a very robust dynamic performance to load changes.

Although the transient requirements of a radar power supply are stringently specified, the precise timing of the load application is known in advance, allowing advance compensation to be made. The anticipated effect of the connection of load can be alleviated by increasing the pulse width of the converter before the load is applied, by the injection of a small voltage into the control loop. With a suitable injected voltage, significant improvement in transient response is achieved. Based on this principle, Voltage Injection Control (VIC) is proposed and investigated in this thesis.

In the thesis, the implementation and design considerations of VIC are described. Timedomain optimisation using HSPICE is proposed to select a suitable injected voltage to meet the specified transient performance. Both experimental and simulated results are presented, demonstrating the robustness of the technique. Utilisation of this technique in distributed power systems for future phased-array radar systems and in other possible applications is also discussed.

During the course of this research, HSPICE optimisation has been applied effectively to design the control loop error amplifier compensation circuit in the time-domain, overcoming some of the limitations of the traditional frequency-domain approach.

Declaration of originality

I hereby declare that this thesis is my own work, unless otherwise stated.

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Abbreviations

- CCM Continuous Current Mode
- CPS Central Power Systems
- CPU Central Processing Unit
- **DCM** Discontinuous Current Mode
- **DPS** Distributed Power Systems
- DSP Digital Signal Processor
- ESR Equivalent Series Resistance
- PCB Printed Circuit Board
- **PMU** Power Management Unit
- **PRF** Pulse Repetition Frequency
- **PWM** Pulse Width Modulation
- SMPS Switched Mode Power Supplies
- VIC Voltage Injection Control

Note:

In this thesis the symbol V_e is used to represent a compensated error voltage. In some texts, V_e represents an uncompensated error voltage.

Chapter 1

Introduction

Switched Mode Power Supplies (SMPS) are widely used as the DC power source in the majority of modern electronic systems, ranging from modern office equipment (e.g. personal computers, printers, fax machines, etc.) to highly sophisticated systems (e.g. radar systems, space shuttle power systems, etc). The increasing complexity of electronic systems has resulted in ever more demanding requirements being placed on their power supplies, particularly in terms of power density, efficiency, electromagnetic compatibility, and output voltage control. The trend towards lower operating voltage for integrated circuits (e.g. from 5 to 3.3V in the pentium processor chip) has further increased the burden on power supply designers.

SMPS employ feedback control to regulate the output voltage, which must be kept within desired limits throughout the whole operating range to ensure correct functionality of the load. For example, a power supply for the Pentium processors must be capable of providing output voltage regulation of $\pm 5\%$, regardless of the processor operating conditions in which load current can slew from a minimum value of less than 1A to a maximum value of about 10A within a few hundreds nanosecond, during the transition of processor operation from sleep to fully active modes. Therefore to meet both steady state and transient output voltage requirements in this application, a control method must be appropriately selected and well designed. Several output voltage control methods are available, some of which are reviewed later in this chapter. In an airborne radar system, due to the nature of its operation, radar performance is strongly determined by the dynamic performance of its power supply. In particular, it is critical that the radar power supply has a robust performance against sudden load current changes. The output voltage transient period must be minimised during the radar operation to prevent deterioration of system performance. This thesis investigates a new control technique for radar power supplies to meet this requirement.

This chapter begins by reviewing the basic concept of SMPS and the voltage control methods currently available. The problems inherent in SMPS in radar systems, together with the rationale and the objectives of the present research are then discussed.

1.1 Overview of Switched Mode Power Supplies

Unlike traditional linear power supplies, the DC-to-DC conversion process in SMPS is achieved using switching techniques in which a solid-state device (bipolar transistor, MOSFET or IGBT, etc.) is employed as an electronic switch operating at high frequency, usually above 20kHz, to convert the DC voltage from one level to another. Through this high frequency switching technique, the device conduction losses are minimised and hence much greater efficiency can be realised, typically 80-90% as opposed to 30-40% for linear units [1]. With high frequency operation, the size of wound components as well as the overall weight are significantly reduced. Recent advances in semiconductor technology have resulted in power devices with increased switching speed, high power rating, and a relatively low cost, such that switched mode power supplies now dominate the power supply market.

Figure 1.1 shows a simplified block diagram of a typical off-line SMPS. The input voltage from the AC mains supply is rectified into an unregulated DC voltage by a diode bridge rectifier circuit with an output smoothing capacitor. In the DC-to-DC conversion, the inverter chops the DC voltage at high frequency, producing an AC voltage across the isolation transformer. The secondary voltage is rectified and filtered by the L-C low-pass filter to produce a smooth DC output voltage



Figure 1.1: Block diagram of an off-line SMPS

 V_o . V_o is regulated by means of feedback control which adjusts the pulse width of the switching device in the inverter block.

The following sections are intended to provide a brief background on SMPS, where only common features such as circuit topologies and operating modes are covered. More details on system characteristics and operations and other essential features can be found in most power electronics textbooks [1,2].

1.1.1 Basic PWM DC-to-DC converter circuits

The isolated DC-to-DC conversion stage in figure 1.1 is usually a derivation from one of the three basic DC-DC converters shown in figure 1.2. The operation of these circuits is based on the alternate conduction of a transistor and diode within each switching cycle. In the buck circuit, during the interval when the MOSFET is on, the diode is reverse biased and the power is transferred from the input to the load through the inductor. During the interval when the switch is off, the diode takes over the conduction of the inductor current, transferring some (or all) of the stored energy in the inductor to the load. The output voltage of the buck converter ideally depends only on the input voltage and the duty ratio $(d = \frac{t_{on}}{T})$ and is always lower than the dc input voltage.



Figure 1.2: Three basic DC-DC converters

The boost and buck-boost converters achieve the DC-to-DC conversion through a similar principle of inductor energy transfer. As seen in figure 1.2, the output voltage of the boost converter is always higher than the input voltage, and the output voltage of the buck-boost converter can be either higher or lower than its input voltage, but with opposite polarity.

1.1.2 Continuous and discontinuous conduction mode

The converters mentioned above may operate either in the continuous or discontinuous conduction mode. This implies that the current in the filter inductor either never falls to zero (in the continuous case), or for the last part of the switching cycle has no current flowing in it (in the discontinuous case). Both conduction modes are illustrated in figure 1.3.

The conduction mode of a converter is determined by the value of load current, inductor and switching frequency. For a converter operating in the continuous



Figure 1.3: Inductor current waveforms of DC-DC converters operating in continuous, boundary and discontinuous modes

mode, the following expression must be satisfied [3]:

$$k = \frac{2Lf_s}{R} > K_{critical}$$
 Equation: (1.1)

where R is the effective load resistance, f_s is the switching frequency, and $K_{critical}$ is a function of duty ratio and is equal to 1 - d, $d(1 - d)^2$, and $(1 - d)^2$ for buck, boost and buck-boost converters respectively. For operation at the boundary $k = K_{critical}$, and $k < K_{critical}$ for discontinuous mode operation. From equation (1.1), the trend towards discontinuous mode can be realised by either decreasing L or f_s , or increasing R.

The advantages of continuous mode of operation over the discontinuous are summarised below:

- Lower peak current through the transistor, diode and output capacitor, for the same average load current. This reduces stress on these devices and does not require components with high current capability.
- 2. Good open loop load regulation.

The disadvantages associated with continuous mode of operation are:

- 1. Slower dynamic response. Due to the continuous flow of the inductor current, a rapid response to disturbances cannot be accomplished; whereas in the discontinuous mode the inductor current starts from zero at the beginning of every cycle, and can accommodate the changes more quickly.
- 2. Requires a larger inductor and, thus, occupies more space.

1.2 Output Voltage Control Methods

1.2.1 Standard control methods

The discussion of PWM control schemes in this section is restricted to the control methods based on constant frequency operation. Three standard control methods in this category are voltage-mode control (or direct-duty control), current-mode control and voltage feedforward control, all of which are analogue-type control techniques. The circuits implementing these control methods are available in Integrated Circuit (IC) chips, which usually incorporate a precision reference voltage source, an error amplifier, a voltage comparator, and a driver circuit. The integration of all of these components into a single IC offers the advantages of compactness, greater reliability, and increased performance.

1.2.1.1 Voltage-mode control

Direct duty control is the simplest method used in SMPS control. Its control principle is illustrated in figure 1.4(b). The output voltage V_o is compared with a reference voltage V_{ref} by the error amplifier. By comparing the error signal V_e to the fixed-frequency sawtooth voltage V_s , the resulting duty cycle signal is used to drive the MOSFET to maintain a constant output voltage. Any change in the output voltage is reflected by an excursion in V_e . The length of the transient period depends on the magnitude of the disturbance and the bandwidth of the system. UC3524 [4], from Unitrode Corporation, is an example of a direct-duty control IC chip.



Figure 1.4: (a) Buck regulator (b) Direct duty control strategy (c) Voltage feedforward control strategy

1.2.1.2 Voltage feedforward control

The direct duty control described in the last section has a poor closed-loop transient response to changes in the input voltage V_i , because the correction mechanism does not take place until the effect has propagated to the output, causing the output voltage to change. This problem is overcome by voltage feedforward control [2,5,6]. In this scheme, the input voltage is fed-forward to the control circuit which possesses a modulation strategy similar to direct duty control, except that the magnitude of the sawtooth signal is proportional to the input voltage. As indicated by the dash line in figure 1.4(c), an increasing input voltage is instantly corrected by decreasing duty ratio, resulting in excellent line regulation.

The voltage feedforward control provides full compensation for line voltage changes only in buck-type (continuous mode) and flyback (discontinuous mode) regulators, while it provides just a partial compensation in other types of regulator. However, the newly proposed voltage feedforward control scheme in [7] in which the control signal V_e , instead of the input voltage, is used to control the magnitude of sawtooth signal results in excellent line regulation in boost converters.

1.2.1.3 Current-mode control

Current-mode control is the most common method currently used in SMPS control. It was first reported in 1978 [8] and ever since has received a great deal of attention. Various analysis methods as well as equivalent circuit models of current-mode controlled converters [9–12] have been developed to tackle design issues such as system dynamic characteristics and stability. The current mode control technique is now mature and well understood.

The operating principle of current-mode control is depicted in figure 1.5(a). The



Figure 1.5: A buck regulator with: (a) Peak current mode control (b) Average current-mode control

duty cycle is derived by comparing V_e to the switch current (or inductor current) waveform V_s . The feedback of switch current forms a second inner current control

loop in addition to the main voltage control loop. The switch is turned on at the beginning of each switching period by the clock signal, and turned off when V_s reaches V_e . The switch remains off until the beginning of the next switching cycle when the next clock signal restarts and the process is repeated.

A converter employing current-mode control is known to be unstable above 50% duty cycle. Some form of compensation is required to extend the stability range: in practice, this is achieved by adding a stabilising ramp signal to V_e or V_s (described further in section 3.4). This slope compensation also prevents sub-harmonic oscillations [13].

Current-mode control has the following advantages over direct duty control:

- 1. Current limit since the switch current is directly controlled by V_c , current limiting to prevent excessive switch current can be easily accomplished by putting an upper limit on the control voltage V_e .
- 2. One pole frequency characteristic as the inductor current is being controlled directly, the converter virtually exhibits single-pole frequency characteristics (a pole due to the inductor is removed), thus simplifying the control-loop compensation.
- 3. Inherent voltage feedforward control a change in the input voltage is instantly reflected in the inductor current and hence duty ratio.
- 4. Modular design parallel connection of identical SMPS modules with equal current sharing can be achieved by feeding the same control voltage V_c to each module.

1.2.1.4 Average current-mode control

The original thought in the proposal of current-mode control described above was to transform a converter's output characteristic into a perfect current source, where the output current (the average of inductor current) is directly controlled by the control voltage in the outer voltage loop, resulting in better output voltage dynamic performance. Because the conventional current-mode control uses the peak inductor current feedback instead of its average value, accurate output current control will be achieved (or the peak-to-average current error will be less) if the current-loop gain is sufficiently high. In current-mode control, the current-loop gain is normally not high enough to correct this error. In addition to this problem, the peak current-mode control has the following drawbacks [14,15]:

- Poor noise immunity. Any noise spike on the peak current waveform can cause instability.
- Slope compensation required.

These limitations are eliminated by the use of average current-mode control as shown in figure 1.5(b) [15]. In this control scheme, a current amplifier is introduced into the current loop which compares the inductor current to its desired level (represented by the error voltage), giving the current error signal at its output. The PWM switching voltage is then derived by comparing the current error signal with a sawtooth waveform. The incorporation of the current amplifier with appropriate compensation allows a much higher current loop gain to be realised than is obtained in peak current-mode control. The substantial increase in the current loop gain makes the inductor current track closely its desired level, eliminating peak-to-average error problems. Due to this tracking ability, average current-mode technique is commonly used to shape the line input current in power factor correction applications.

1.2.2 Modern control methods

In addition to the standard control methods reviewed in the preceding sections, numerous control strategies have recently been proposed with the common aim to improve converter performance (both dynamic and steady state), some of which are examined in this section.

1.2.2.1 Function control

Function control [16–18] is a novel control strategy whose control law is synthesised from equations governing the averaged behaviour of the power circuit. The control law is formulated such that the output voltage is theoretically independent of both line voltage and load current, accomplishing zero voltage regulation¹. A buck converter with function control is shown in figure 1.6. For robust per-



Figure 1.6: Function control of a buck converter

formance, the control law is implemented employing four feedback variables: the output voltage (V_o) , a low-frequency component of inductor voltage (V'_L) , the input voltage (V_i) , and the rate of change of output voltage (proportional to I_c).

As illustrated in [18], function control exhibits superb dynamic performance to both line voltage and load current variations. Nevertheless, it is subjected to the following limitations:

• The control circuit is complicated, requiring a circuit to retrieve a low frequency component of the inductor voltage (V'_L) . Additionally, the control law for other types of converters, such as boost or buck-boost, would have a more complicated form which requires more elaborate control circuits.

¹Because of the non-ideality of the switching device and circuit components, zero voltage regulation would never be attained in practice.

 System stability is ensured only when a properly design proportional-derivat ive (PD) controller is used in the output voltage (V_o) loop. Function control is unstable with both proportional and proportional-integral (PI) controllers.

1.2.2.2 One cycle control

One-cycle control [19-21] is a non-linear control technique proposed by Professor Cuk of California Institute of technology. The technique demonstrated with the buck converter is shown in figure 1.7, with the operating principle described as follows.



Figure 1.7: A buck converter with one-cycle control

A constant frequency clock turns on the transistor at the beginning of each switching period. The voltage across the diode V_s is integrated and compared with a reference voltage V_{ref} . As soon as the integration result (V_{int}) reaches V_{ref} , the comparator changes its state, turning off the transistor and, at the same time, resetting the output voltage of the integrator to zero ready for the operation in the next switching cycle.

The integration of V_s in each switching cycle represents the averaged value of V_s (which is equal to the output voltage) and follows closely the reference voltage V_{ref} . Therefore, with constant V_{ref} , the output voltage is also constant. One

cycle control eliminates the effect of input voltage perturbation within a switching cycle, but suffers badly from poor load regulation due to no output voltage feedback. The technique is thus not suitable for power supply regulation, but is often used in power factor correction applications [22].

1.2.2.3 Digital control

In recent years, there has been much research on digitally controlled switched mode power supplies [23–26]. The digital controller may be a computer, a microprocessor or a Digital Signal Processor (DSP), performing control algorithms which can range from simple direct duty control [23,24] to averaged current mode control [25]. Using software control, the control strategy can easily be changed without changes in hardware. The digital controller is also less sensitive to noise and to changes in environment such as temperature, ageing components, etc. Because the implementation of digital control is normally far more expensive than its analogue counterparts, it is only favoured in high performance applications, in which some auxiliary functions may be necessary and can be easily implemented with the digital controller, e.g. in a battery charger in satellite systems [26].

The main limitations of digital control are summarised below:

- 1. Errors are rounded as the digital controller is only capable of processing data with a finite wordlength. As a result, the variation of duty cycle is limited to a specific resolution (not continuously variable).
- 2. It is slower in comparison to the analogue type due to the processor computation time.

1.2.2.4 Artificial neural networks control

Artificial Neural Networks (ANN) are well-known for their learning and selforganising abilities which allow them to adapt to changes or any uncertainties that may develop in the system. These attributes are found to be useful in



controlling non-linear systems. A simplified structure of an ANN controller [27] is shown in figure 1.8. The input and output of the controller are connected

Figure 1.8: A simplified ANN controller

through layers of similar processing elements called neurons. Each neuron has multiple inputs and one output and is connected to other neurons through the connection weighting. Changing the weighting will alter the behaviour of the element and hence the behaviour of the whole network. The goal in designing the controller is to adjust the weightings of the network to result in a desired input/output relationship. This process is known as *training* the network.

The application of ANN to control DC-DC converters has been recently reported in [27-31]. Except [31], all works are solely computer simulations. The on-line trained neuron ANN boost converter implemented in [31] suffers from a very poor dynamic performance, as it takes approximately 10 seconds for the controller to track correctly changes in reference voltage. Additionally, the cost associated with this implementation is high as it requires a fast, high performance DSP chip as well as peripheral systems to realise the operation at high switching frequency. This indicates that at present ANN controllers are not yet suitable for power supply voltage control applications.

1.2.2.5 Fuzzy logic control

Fuzzy Logic Control (FLC) employs heuristic reasoning based on human experience of the system to construct the control strategy. Such experience is collected in the knowledge base (or rule base) in the form of linguistic rules using an *if-then* conditional statement. Based on the qualitative description of the system to be controlled, FLC is suitable for controlling a complex and ill-defined system without requiring its detailed mathematical model. The major drawback of FLC is that there are no precise criteria to synthesise the control rules and select membership functions [32].

In recent years, some researchers have introduced FLC to control DC-DC converters. As with neural networks, the application of FLC in DC-DC converters is just in its early phase and most of the work [32-34] is mainly based on computer simulation. The hardware realisation of fuzzy logic control DC-DC converter has been recently described in [35,36]. So et. al. [35] use a fast, powerful TMS320C50



Figure 1.9: The functional structure of FLC DC-DC converter

DSP chip to implement FLC shown in figure 1.9. With an execution time of 50ns per single instruction and a converter switching frequency of 100kHz, only 200 single instructions are permitted to complete all essential computation in each switching cycle. This is just adequate for a primitive algorithm, but not for more sophisticated control. The computation power of the FLC implementation in [36] is even more limited as a slower microcontroller is used. Above all, the implementation of FLC reported in these two papers is complicated and expensive, yet it does not give a better dynamic performance than conventional analogue control.

1.2.3 Brief summary of existing control strategies

In summary, the modern control strategies reviewed in the previous section either are still in the very early stages of development e.g. fuzzy logic control and artificial neural networks, or have their usage confined to a very limited number of applications, e.g. digital control and one-cycle control. At present, voltage-mode control and in particular current-mode control (described in section 1.2.1) are the two control methods currently used in almost all commercial power supplies.

It is well-known that current-mode control has a generally superior performance over its voltage-mode counterpart, and for most applications a well designed power supply incorporating current-mode control yields satisfactory performance. Nevertheless, in some applications, such as in radar systems, system performance is severely limited by the dynamic response of the power supply to sudden load changes.

In this project, a new control technique specifically for radar power supplies is investigated. In order to have a clear understanding of the concept of the proposed technique, it is useful first to describe the radar system operation and the load characteristics of the power supply in this application.

1.3 Airborne Radar Systems

1.3.1 Brief operation overview

The simplified diagram of a radar system consisting of a transmitter/receiver unit, a power supply unit and a radar processor is shown in figure 1.10(a). Controlled by the radar processor, the system operation is primarily based on transmission of a high power pulse signal (by the transmitter) into space and detection of the reflected signal from the target (by the receiver) from which information concerning the target's location, direction and velocity can be derived. The frequency at which the pulse signal is transmitted is called the *pulse repetition frequency* (PRF). The receiver can only accept target echoes during the interpulse period



Figure 1.10: (a) Simplified block diagram of radar systems (b) Pulse current drawn during PRF transmission (c) Equivalent circuit of PRF transmission

i.e. target echoes arriving within the duration of the transmitted pulse will not be seen. As a result, a range of pulse widths and PRFs are required in different modes, to ensure that the target is not lost.

The range of frequencies and pulse widths typically used in low, medium and high PRF operation is listed in Table 1.1^2 . The control technique investigated in

Operation	Frequency range	Pulse widths
High PRF	80 - 200kHz	150 - 500ns
Medium PRF	10 - 25kHz	1 - $3\mu { m s}$
Low PRF	less than 10kHz	5 - 50µs

Table 1.1: The range of frequencies and pulse widths in different PRF regimes

this project is aimed to be used in radar systems operating in the medium and high PRF regimes.

²This information is obtained from Mr. Frank Fisher, the chief engineer of the Power Conversion Division at GEC-Marconi Ltd., Edinburgh.

1.3.2 Load characteristics of radar power supplies

The transmission of each RF pulse causes a high-peak pulse current to be drawn from the power supply. Fortunately, the period of the pulses is very short, a maximum of 3μ s in a typical medium PRF system. The resulting voltage drop during such a short period is negligible and not detrimental to system operation. On the contrary, the voltage drop due to the averaged current drawn by a series of these current pulses (typically several thousand pulses per operation) could affect system operation.

The operation at a different PRF represents a different load condition for a fixed pulse width to the power supply; the higher the PRF, the more average current is drawn as shown in figure 1.10(b). This is analogous to having a bank of loads (figure 1.10(c)) connected across the output of the power supply, where the selection of load is controlled by the radar processor. With n loads in parallel, $2^n - 1$ load conditions (or PRF values) are possible.

Figure 1.11 illustrates how the overall performance of radar systems can be reduced by using a power supply with limited dynamic performance. Transmission



Figure 1.11: Illustration of how system performance is limited by SMPS dynamic performance

at a new PRF at time t_0 draws an increased averaged current, causing the output voltage drop. To ensure the correct operation of the receiver, the output voltage must return to the specified level before the return of the echo pulses time t_d later; otherwise, the first few returning pulses would have to be rejected. The more rejected pulses means the less accurate target information. Assuming the target was 20 miles away from the radar, the output voltage settling time of the power supply should be less than 213μ s (time used by the signal travelling to and returning from the target) in order that no pulses are missed. It is therefore critical that the radar power supplies have excellent dynamic performance against the load disturbances.

Conventional current-mode control does not yield satisfactory load transient response (as a result many returning pulses have to be abandoned). A new control technique for radar power supplies which is capable of giving better transient performance is essential.

1.4 The New Voltage Injection Control (VIC)

Since the radar processor (a computer) knows precisely when the transmission of the PRF pulse stream will take place, a warning signal (shown by the dash line in figure 1.10(a)) can be sent in advance to the power supply control circuit to initiate a compensation mechanism, in an attempt to minimise transient effects when the load change occurs. The compensation can be achieved by forcing the output voltage to increase by injecting a small voltage into the power supply's control loop (thereby increasing the pulse width of the converter), at some point before the load application. The proposed technique is therefore named Voltage Injection Control (VIC).

The principle of VIC illustrated for PWM voltage-mode control is shown in figure 1.12. In figure 1.12(a), after load application, the pulse width of the converter is increased by the feedback mechanism, in an attempt to bring the output voltage back to nominal value. With the advanced knowledge of load application, a small voltage can be injected into the control loop to increase the pulse width of the converter waiting for the subsequent load application (figure 1.12(b)). When appropriately performed, VIC will result in a significant improvement in the output voltage transient response.

VIC is considered as a disturbance feedforward technique in the sense that the



Figure 1.12: (a) Conventional technique: the PWM pulse widens after load application (b) With VIC, the PWM pulse widens by before load application

compensation mechanism is initiated upon receiving the advance warning signal of load disturbance from the radar processor. Similar feedforward compensation techniques based on predictable disturbances to improve plant performance are also found in industrial processes [37] and data storage systems [38,39]. The VIC technique will be discussed in detail in Chapter 2.

1.5 Aims of the Research

This research is to investigate the voltage injection control technique. Aims of the research are as follows:

- 1. To study the feasibility of VIC. The principle objective of this study is to assess how much improvement in transient response can be achieved with this technique, compared to that given by standard control methods.
- 2. To develop a VIC prototype system so that experiments can be conducted to validate the objective (1).

- 3. To establish the VIC design methodology. In order to obtain an improved transient response, the magnitude and shape of the injection voltage, and when it should be applied, are parameters that must be appropriately selected. A systematic procedure for computing these parameters is therefore needed.
- 4. To exploit the advantages of computer simulation in the design and analysis of a switching converter with VIC.

This project was carried out with cooperation from GEC-Marconi Avionics³, Edinburgh. The use of the VIC technique to real radar systems is envisaged by the company.

1.6 Thesis Structure

The remainder of this thesis is organised into seven chapters:

Chapter 2 - Voltage Injection Control (VIC) Technique - The principle and implementation of voltage injection control are explained in detail. It is important that VIC implementation should not affect the pre-defined loop-gain characteristics and system stability. This issue is also considered in this chapter.

Chapter 3 - Prototype Design and Development - The operation of the VIC prototype system, consisting of a personal computer (as a radar processor), a power supply unit, a programmable switched load and a computer based oscilloscope, are described. The detailed design and construction of the power supply and programmable load units is also given in this chapter.

Chapter 4 - Simulation and Modelling - The development of the state-space averaged model of a buck converter with VIC and its SPICE equivalent circuit model are explained. Also developed in this chapter is the switched model for SPICE "brute-force" simulation. Issues concerning SPICE convergence problems in brute-force simulation and the appropriate remedies are also considered.

³The company is a major radar manufacturer in the UK.

Chapter 5 - V_{inj} Optimisation - In this thesis, optimisation is employed to perform two tasks: to design a suitable injection voltage (V_{inj}) for each load change, and to design the power supply compensation circuit. Each of these applications is discussed in this chapter.

Chapter 6 - Results - Results of VIC investigation are presented, including those from optimisation design of the power supply compensation circuit.

Chapter 7 - Discussion - This chapter evaluates the advantages and disadvantages of VIC. The discussion on simulation and modelling, and optimisation are given. The use of VIC in a power supply system for a future phased array radar, and also in other possible applications, is reviewed.

Chapter 8 - Conclusion - The outcomes of the research are summarised and possible future work suggested.

Chapter 2

Voltage Injection Control (VIC) Technique

As stated in section 1.5, the objective of this work is to propose and investigate Voltage Injection Control (VIC), a technique to enhance dynamic response due to load change of power supplies in radar applications. Using prior knowledge of the forthcoming load condition, the controller increases the pulse width of the converter an appropriate number of cycles in advances of the load application, allowing considerable improvement in system performance to be achieved.

By the definition given in [40], VIC is classified as an open-loop disturbance feedforward control, illustrated in figure 2.1. In addition to the existing feedback



Figure 2.1: A simplified diagram of a switching converter incorporating disturbance feedforward control

control loop, the feedforward path is provided for a prior warning signal to be

sent to notify the controller of the arrival of a load disturbance, so that it can start the appropriate compensation for the anticipated effect of that load. The VIC prototype realising the system shown in figure 2.1 is detailed in Chapter 3.

This chapter describes features concerning the operating principles, implementation, and design considerations of VIC.

2.1 Voltage Injection Control

A buck converter with the proposed VIC control circuit is illustrated in figure 2.2. An external summing block has been added to the standard voltage-mode control





loop, allowing an externally controlled voltage to be injected into the control loop, thereby increasing the pulse width of the converter. The injection of the external voltage into the control loop causes a disturbance in the system, which is used to compensate for the disturbance caused by a sudden load change. For this reason, VIC is considered as a disturbance feedforward compensation technique.

2.1.1 Principle of operation

2.1.1.1 System characteristics under a sudden load change

When a load is applied, in a conventional system (figure 2.2 with $V_{inj}=0$), the extra current demanded by that additional load is initially drawn from the discharging current of the output capacitor, as current cannot be immediately increased from the input due to the presence of the filter inductor. The output voltage hence drops below its regulated value, and the error signal, V_e , as well as the control signal, V_c , will increase (in this case, $V_e = V_c$). V_c is compared to the sawtooth signal at the comparator stage which will consequently widen the PWM pulse in an attempt to reduce the output voltage error.

After passing through the transient state, the converter eventually settles to a new steady state and the output voltage is brought back to its regulated value, as shown in figure 2.3.¹ The dynamic response is dictated by the loop gain bandwidth, and normally a large number of switching cycles is required before the steady-state is regained.

2.1.1.2 System characteristics under voltage injection (with constant load)

When the injected voltage, V_{inj} , is applied into the control loop, it is added to V_e so that the input to the comparator, V_c , is:

 $V_c = V_e + V_{inj}$ Equation: (2.1)

A rise in V_c increases the pulse width and forces the output voltage to rise. V_e hence decreases, and from equation (2.1), V_c also decreases as V_{inj} remains constant, resulting in a narrowing of the pulse width of the converter in an attempt to reduce the output voltage (as now it is increasing above the regulated value).

¹All waveforms presented in this chapter are generated by HSPICE simulating the converter's switched model described in chapter 4.



Figure 2.3: Dynamic response to a 3A load change (switching frequency = 100kHz)

After passing through the transient state, the previous steady state of the converter, before the voltage injection, is reinstalled, as the output voltage is brought back to its regulated value. V_c reverts to its previous steady-state value, but at the expense of V_e being compensated by V_{inj} , as shown in figure 2.4. The duration of the transient is again dictated by the loop gain bandwidth.

2.1.1.3 System characteristics under a sudden load change with VIC

If the timing and magnitude of load application is known in advance, this information can be used to start a compensation mechanism, the voltage injection (figure 2.4), before that load is applied. By injecting an appropriate value of V_{inj} in advance of the load application, significant improvement of transient response will be obtained. An example of such improvement is shown in figure 2.5, which is a simulated result of injecting a voltage of 0.1755V, 60μ s in advance of a 3A load change. The converter's switching frequency is 100kHz. Compared with


figure 2.3, the transient performance has been significantly enhanced.

Figure 2.4: Dynamic response to voltage injection (constant load)



Figure 2.5: Dynamic response to a 3A load change enhanced by VIC For a load rejection (opposite to the load application of figure 2.3), similar im-

provement will be obtained if V_{inj} is removed 60μ s in advance of the load rejection. Consequently, the subsequent study and discussion of VIC will be confined only to the load application case: similar conclusions can easily be drawn for load rejection by considering it as a mirror image of the application of load.

2.1.2 Control circuit realisation

The summing circuit in figure 2.2 includes summing and inverting amplifiers as depicted in Figure 2.6. The summing amplifier adds V_{inj} to V_e , as in equation



Figure 2.6: Circuit Realisation of VIC

(2.1) $(R_1=R_2)$, but with an inverted polarity. Thus, it has to be followed by an inverting amplifier. The injection of V_{inj} is controlled by a computer which embraces both timing and amplitude control. This is discussed in more detail in Chapter 3.

2.1.3 Stability considerations

From the stability point of view, the implementation of VIC should not alter the pre-determined control-loop characteristics, otherwise it may lead to an unpredictable instability. However, the inclusion of the voltage injection circuitry (figure 2.6) into the control loop has the potential to change the converter loop gain characteristics as shown in figure 2.7. The portion surrounded by the dashed



Figure 2.7: Closed-loop control block diagram of VIC converter

box is newly introduced into the system block diagram due to the incorporation of the VIC circuit. The loop gain $(T_cT_mT_p)$ in figure 2.7 is now adjusted by the ratio $\frac{R_2}{R_1}$. If the control loop has already been well designed, this loop-gain alteration will alter the converter performance from the expected values, i.e. a sluggish dynamic response would be obtained if $\frac{R_2}{R_1}$ was low, whereas the system would exhibit considerable overshoot and ringing if $\frac{R_2}{R_1}$ was high, and if too high, the system would become unstable. To avoid these effects, a unity gain summing circuit is used $(\frac{R_2}{R_1} = 1)$, thus leaving the converter performance dependent solely on the initial design of the control loop.

2.2 The Injected Voltage

The injected voltage (V_{inj}) is a crucial parameter in determining the resulting transient response. If V_{inj} is well-suited to the load change, a stringent transient specification that cannot be achieved by standard feedback control can be attained with VIC.

 V_{inj} is described by three variables, its amplitude, injecting time, and shape. In mathematical terms, it is expressed as a function containing these variables:

$$V_{ini} = F(Amplitude, Injecting time, Shape)$$
 Equation: (2.2)

Each variable and its implication on the final response is described below.

2.2.1 Amplitude of the injected voltage

A higher injected voltage amplitude causes a higher maximum voltage rise and longer transient duration (see figure 2.4). As a result, the amplitude should increase with the magnitude of load disturbance. However, it must not be so high such that the resulting V_c exceeds the peak of the sawtooth signal, as this would make the control loop temporarily open (it will be permanent if the magnitude of V_{inj} was high enough to force V_e to its minimum value). Therefore, the maximum magnitude of V_{inj} must be confined to the difference between the peak sawtooth signal and the steady-state error voltage at minimum load current (V_{emin}), as shown in figure 2.8. For example, if the peak of sawtooth signal and the minimum



Figure 2.8: Maximum V_{inj} is determined from the error voltage at minimum load current to the peak of sawtooth signal

error voltage are 3.5V and 1V respectively, the maximum V_{inj} magnitude should be less than 2.5V. For a converter to have a good transient response at any possible load condition, the magnitude of V_{inj} is usually limited to the resultant change of V_e the converter would experience when it is subjected to that load without VIC.

In this project, V_{inj} is applied by a computer, the VIC controller, via a D/A converter. The value of V_{inj} is stored in the computer memory using 8-bit data format (see chapter 3). This finite word length sets the resolution of V_{inj} , therefore, the amplitude of V_{inj} is a discrete variable.

2.2.2 Injecting time of the injected voltage

The injecting time is the time interval between the instance of voltage injection and load application, as shown in figure 2.9. In this section, it is assumed that



Figure 2.9: Illustration of the injecting time definition

load is applied during the ON period of cycle *i*. The pulse width can be increased one cycle in advance of the load switching by injecting the voltage at the point indicated by the arrow in the i - 1 cycle, or two cycles in advance by injecting the voltage at the point indicated by the arrow in the i - 2 cycle, and so on. Therefore, the injecting time expressed in term of a switching cycle is a positive integer:

It should be noted that V_{inj} can, in fact, be applied anywhere in the region labelled by A (or B) for two-cycle (one-cycle) advance compensation, while the eventual result is still the same. Here, the definition of injecting time indicated by the arrow in figure 2.9 is used.

Although the preceding definition of the injecting time assumes that the load is applied during the ON period, it also holds true for when load is applied during the OFF period. However, a slightly discrepancy does exist between the worst case scenario, when the load is applied at the beginning of the OFF period, and the optimistic one, when the load is applied near the end of the ON period. This discrepancy is examined in detail in section 6.2.4.

The voltage injection is usually not permitted to take place long before the load application, otherwise the initial output voltage rise will become excessive as shown in figure 2.10. This rising voltage is named the spike voltage, a transient



Figure 2.10: High spike voltage due to long injecting time

specification newly introduced by VIC. Despite a higher spike voltage, the long injecting time is likely to result in a smaller voltage drop after load application. This demonstrates one of the trade-offs in the process of selecting a suitable V_{inj} for any specific load condition, to meet the transient requirements. A compromise between these transient specifications has to be reached in the V_{inj} design, and is further discussed in Chapter 5.

2.2.3 Shape of the injected voltage

The two V_{inj} waveforms shown in figures 2.11 and 2.12 had been conceived in this project, a ramp and a step. In figure 2.11, V_{inj} increases linearly from 0 to the

required value over the injecting time interval (slope $= \frac{amplitude}{injecting time}$) causing the output voltage to build up at a slower rate than in figure 2.12, hence resulting in a smaller spike voltage. However, it produces a larger voltage drop after load is applied.

The step V_{inj} was selected and used throughout this work as it is easier to generate and control. It should be noted that the result in figure 2.11 can also be achieved using a step voltage with a lower magnitude. Therefore, equation (2.2) is now redefined as a step function of two variables, the amplitude and injecting time:

$$V_{ini} = Step - function(amplitude, injecting time)$$
 Equation: (2.4)

The problem of selecting an appropriate V_{inj} in order that the desired transient requirement is met for each load condition is associated with the optimisation of equation (2.4). Before the optimisation is discussed, the mathematical model of VIC is required and is derived in Chapter 4. The developed model is then used in Chapter 5 for carrying out the optimisation of V_{inj} .



Figure 2.11: Dynamic response of the linearly increased V_{inj}



Figure 2.12: Dynamic response of the step V_{inj}

Chapter 3

VIC Prototype Design and Development

3.1 VIC Experimental Set Up

This chapter details the design and development of a prototype power supply implementing the concept of VIC described in Chapter 2. The system configuration shown in figure 3.1, whose components include a microcomputer, a switching load unit, a SMPS unit, and a computer oscilloscope (HS508), is proposed. It is intended to imitate the operating environment of a power supply in a radar system (section 1.3), in which the application/rejection of a chosen load in the switched load unit represents the beginning/ceasing of the transmission of pulses at a specific PRF.

The microcomputer is employed as a central control unit, controlling both the switching load unit and the injection of V_{inj} with appropriate magnitude and timing for the selected load. The operation of the prototype is best described by the flowchart of figure 3.2.

Design considerations and the construction of each unit in the prototype are described in the following sections.



Figure 3.1: Experimental set up to investigate VIC technique

3.2 Computer

3.2.1 Hardware

The microcomputer used is an 80486, 33MHz Personal Computer (PC). The interface to the outside world is facilitated by a programmable I/O card based on an Intel 8255 chip [41,42]. The card provides three 8-bit ports (A, B, and C) each of which can be configured to be either an input or output port by a user programme. The card is plugged into one of the vacant slots available on the PC motherboard, and obtains power, control, addressing and data signals from the computer expansion bus. The outputs from the card (24 I/O lines, 5V and ground) are connected to a 37-way male D-type connector to facilitate connection with the outside world.

The computer accesses the interfacing card by its addresses, in which the addresses of ports A, B, C and a control register are designated to 300h to 303h respectively, as shown in figure 3.3. These ports are programmed to perform the intended functions by writing the corresponding 8-bit control word to the control register. The bit description of the control word can be found in the technical



Figure 3.2: The prototype operation flowchart

manual in reference [41]

In this work, only ports B and C are used; these are assigned to do the following functions:

- Port B is an output port to control voltage injection, and is connected to the D/A converter of the voltage injection circuit.
- Port C is an output port to control the switched load.

3.2.2 Software

As seen in the flowchart in figure 3.2, the communication between the computer and the interfacing card is a major part of the programme, as both voltage injection control and switched load control require data to be sent from the PC



Figure 3.3: Simplified diagram of the I/O interfacing card

through the card. The assembly language¹ routines have been written to facilitate this low level I/O interfacing, and is incorporated into the main C programme written to perform the user interfacing tasks. The compiler used, Borland C++ 4.0 [43], allows assembly code to be compiled separately from the main C code by the Turbo assembler [44]. The resulting assembly language object code is then combined with the C language object code into one working programme during the linking process. The control programme is listed in appendix A.

Brief control programme description

Before the operations in figure 3.2 can begin, the interfacing card must first be initialised by writing a control word to the control register:

mov dx, 303H mov al, 80H out dx, al

This configures ports A, B, and C as output ports.

The following is a brief description of the assembly code which performs the control algorithm in figure 3.2

¹This is a *low-level* (or *machine-level*) programming language and is very powerful for computer hardware control and interfacing.

• V_{inj} is issued through port B by the execution of the following code:

mov dx, 301H mov al, 0dH out dx, al

• The injecting time is set by the execution of a time delay loop:

mov cx, 100

AA: nop

nop

loop AA

The value loaded into the register \mathbf{cx} is calculated from the following formula (derived from the execution time of each instruction):

$$t_{inj} = \frac{1}{f_{sys}}(8n+1)$$
 Equation: (3.1)

where:

 t_{inj} is the injection time (in μ s),

 f_{sys} is the clock speed of the computer (in MHz), which is equal to 33MHz in this case,

n is the number required for the register cx.

• After the injecting time, a signal is sent through port C to the switching load control circuit:

mov dx, 302H mov al, 50H out dx, al

• The duration of the existence of the switched load is controlled by the following time delay loop:

ы, 0 mov ы, 1 **BB**: cmp \mathbf{exit} je 0fffH mov cx, CC: nop nop loop CCbl inc BB jmp

• For load rejection to be controlled in a similar way, V_{inj} is removed in advance of the load rejection:

301H dx, exit: mov 0 mov al, dx, al \mathbf{out} cx, 100mov DD: nop nop DD loop 302H dx, mov 0 mov al, al dx, out

In radar systems, the computational power of the radar processor is mostly spent on processing the received signal, and therefore the available computing power is limited. To incorporate the voltage injection control routine into the radar control programme, it is very important that the length of the routine is kept as short as possible. With the assembly language, the length of the voltage injection control routine can be easily optimised.

3.3 Power Supply Unit: Voltage Mode Control

In chapter 2, VIC has been demonstrated in a converter employing voltage-mode control; nevertheless the principle may equally well be applied to a power supply

using current-mode control. Although the main emphasis in this project is an investigation of VIC in a system using voltage-mode control, the prospect of applying VIC with current-mode control is also examined.

Hence, two prototypes, one based on each control method, have been developed and are detailed in this section.

3.3.1 Power circuit board

The buck converter in figure 3.4 operating in Continuous Current Mode (CCM) was designed to meet the following specifications:

Input voltage, $V_{in} = 30V \pm 10\%$, Output voltage, $V_o = 15V$, Maximum output ripple, $V_{ripple} < 100mV$ Minimum output current, $I_{omin} = 0.75A$, Maximum output current, $I_{omax} = 5A$.

A switching frequency (f) of 100kHz was chosen.



Figure 3.4: Buck power circuit of VIC with voltage-mode control

For a converter to operate in CCM, the value of inductor must satisfy the following condition [45]:

$$L > \frac{V_o^*(1 - D_{min})}{I_{ripple}f}$$
 Equation: (3.2)

where:

 V_o^* is an effective output voltage, equal to an output voltage plus a voltage drop in the circuit; the value of 15.7V is assumed in the design.

 I_{ripple} is the ripple current in the inductor which is equal to $2I_{omin}$.

Thus, the value of inductance must be greater than 49μ H. The chosen filter inductor L=50 μ H satisfies the above condition, and is fabricated using a Ferroxcube ETD core.

The filter capacitor is calculated following the formula:

$$C > \frac{V_o T^2 (1 - D_{min})}{8V_{ripple}L}$$
 Equation: (3.3)

Thus, a capacitance greater than $20\mu F$ is required.

The capacitor has an Equivalent Series Resistance (ESR), whose value is determined from:

$$ESR < \frac{V_{ripple}}{I_{ripple}}$$
 Equation: (3.4)

Thus, an ESR less than $66m\Omega$ is required.

The chosen 470μ F, ESR=0.027 Ω low impedance electrolytic capacitor satisfies both equations (3.3) and (3.4).

The semiconductor devices were deliberately overrated to give reliable operation: an IRF740 (400V,10A) power MOSFET and a MBR1045 (45V,10A) diode were chosen.

The input voltage to the circuit is taken from a variable DC voltage power supply (0-35V, 8A) and is set to 33V. The output resistor is 20 Ω , thus establishing a standing load current of 0.75A.

The circuit is assembled on a double-side PCB which was designed to ensure minimum connection length between circuit components. A large copper area

was left on both side of the board as a ground plane to attenuate noise in the circuit.

3.3.2 Control circuit board

A full circuit diagram of the control board consisting of control (figure 3.5(a)) and driver (figure 3.5(b)) stages is depicted in figure 3.5. Similar to the power circuit board, the circuit is built onto a double-side PCB with a large ground plane on both sides. The functional details of each stage are described below:

Control stage

Voltage-mode control is implemented using a UC3524A, a voltage-mode control chip from Unitrode [4]. The converter switching frequency is programmed by R_t and C_t connected respectively at pins 6 and 7 of the chip according to the approximate formula:

$$f = \frac{1.18}{R_t C_t}$$
 Equation: (3.5)

where R_t , C_t and f are in k Ω , μ F, and kHz respectively.

To implement voltage injection control, a summing circuit is included between the error amplifier and the voltage comparator. This is done by disabling the error amplifier inside the chip (by connecting it as a unity gain buffer, with pin 1 connected to pin 9 and pin 2 connected to ground), and instead, using an external error amplifier (LM741). The converter's output voltage is fed back to the error amplifier through a resistive divider chosen to give a gain of 0.16. This implies the reference voltage must set to 2.4V in order to achieve a regulated output voltage of 15V. The error amplifier is compensated by a two-pole, two-zero compensation circuit, with component values selected by the optimisation design described in Chapter 5, in order to give a good dynamic response to load changes.

Receiving its input from port B of the interfacing card, the 8-bit D/A converter (ZN428E-8) converts the digital V_{inj} to the equivalent analogue value. V_{inj} is





Figure 3.5: VIC with voltage-mode control board: (a) Control circuit (b) Driver circuit

then fed into one of the inputs of the summing circuit, comprising a summing amplifier (LM741) and an inverting amplifier (LM741). The resolution² of the D/A converter is 19.5mV, and the control range of V_{inj} is available from 0 to 4.9725V.

The output from the summing circuit (V_c) is connected to the comparator inside the UC3524A through pin 9, and the output PWM signal is obtained at pin 13.

Driver stage

As shown in figure 3.5(b), the complementary buffers (CD4049 and CD4050) are employed to drive the power MOSFET through a 1:1 isolation transformer. The buffers increase the current capability of drive signal to a level sufficient to supply the gate current required by the MOSFET gate-source capacitance at switch-on and switch-off.

On the transformer secondary, further components are necessary to create a satisfactory switching waveform at the MOSFET gate [46]:

- 1. 150 Ω resistor across the gate-source of the MOSFET to attenuate ringing - at the gate, due to resonance with the lead inductance.
 - 2. Two Zener diodes back-to-back provide protection against transient voltage spikes from punching through the gate-source junction of the MOSFET.
 - 3. 10Ω resistor in series with the gate to dampen ringing with the secondary of the pulse transformer.

The gate drive signal is shown in figure 3.6.

 $^{^{2}}$ The resolution of a D/A converter is defined as the difference between any two consecutive values at the output, or equal to the LSB.



Figure 3.6: PWM gate drive signal

3.4 Power Supply Unit: Current Mode Control

The prototype is adapted from the voltage-mode control board by incorporating features essential in current-mode control i.e. a current sensing resistor in the power circuit, a stabilising ramp signal, and the current-mode control chip. Hence, in this section, these extra features are emphasised.

3.4.1 Power circuit board

A buck converter operating in CCM with the following specifications was built to validate the capability of VIC in a system using current-mode control (figure 3.7):

Input voltage, $V_{in} = 20V \pm 10\%$, Output voltage, $V_o = 5V$, Maximum output ripple, $V_{ripple} < 100mV$, Minimum output current, $I_{omin} = 1.25A$, Maximum output current, $I_{omax} = 5A$. A switching frequency of 50kHz was chosen.



Figure 3.7: Buck power circuit of VIC with current-mode control

Following the same criterion used in designing the power circuit board in section 3.3.1, the MOSFET, diode and output filter were chosen as illustrated in figure 3.7. The standing load current is fixed at 1.25A by a 4 Ω output resistor. The switch current is sensed by a 0.1 Ω resistor, which was chosen to give a large sensed voltage (for noise immunity) while minimising power losses.

Because of the position of the sensing resistor, the signal ground³ must be at the output, instead of at the input as previously used in the power circuit board of the voltage-mode system (section 3.3.1).

3.4.2 Control circuit board

The voltage injection and driver circuits used are similar to those in the voltagemode control board. The current-mode control board, however, employs a different control chip and error amplifier compensation scheme, and requires slope compensation to prevent instability for duty ratios greater than 0.5 and subharmonic oscillations. These extra features are shown in figure 3.8.

The current-mode control is established using a UC3846, a peak current-mode control chip from Unitrode. The converter switching frequency is programmed

³Signal ground is a reference signal for various signals in the control circuit



Figure 3.8: VIC with current-mode control board: (a) Current-mode control chip, switch current inverter and slope compensation circuit (b) Error amplifier and compensation circuit

by R_t and C_t connected at pins 8 and 9 of the chip respectively according to the approximate formula:

$$f = \frac{2.2}{R_t C_t}$$
 Equation: (3.6)

where R_t , C_t , and f are in k Ω , μ F, and kHz respectively.

The sensed switch current (V_s) is fed back to the current sense amplifier inside the chip (pins 3 and 4) through an inverting amplifier, forming an inner current loop (in addition to the main voltage loop). The inverting amplifier is required to invert V_s , which is negative due to the position of the signal ground before feeding it to the current sense amplifier. A small RC filter at the output of the inverter amplifier is employed to reduce any noise in the sensed current waveform to an acceptable level [47].

The slope compensation signal is generated from the oscillating ramp signal at pin 8 of UC3846. By feeding the signal to a buffer transistor (2N2222), an adjustable slope signal controlled by the variable $1k\Omega$ resistor is obtained at the collector of the transistor. This slope signal is then added to the sensed switch current at pin 4 of the UC3846, accomplishing the slope compensation scheme and thus extending the stability range of the converter to above 50% duty cycle [9,11,48,49].

Unlike voltage-mode control, the power stage of the switching converter employing current-mode control exhibits a single-pole frequency characteristic, hence easing the control loop compensation. In theory, closing the loop will produce a stable system with no additional compensation: however, in practice the excess gain at half the switching frequency can cause subharmonic oscillation. Therefore, the pole-zero network consisting of $R=10k\Omega$ and $C=0.033\mu$ F is used to reduce slightly the high frequency gain and cross-over frequency to ensure system stability.

3.5 Switching Load

The circuit configuration of the load is depicted in figure 3.9. Three resistive



Figure 3.9: Switched load circuit configuration

loads, each of which is in series with an IGBT, are connected in parallel across the output terminals of the converter. The IGBT acts as an electronic switch, and is turned ON by applying an appropriate voltage to its gate terminal.

The switching load is controlled by the PC through the control circuit shown in figure 3.10. The load selecting signal sent by the PC through the three uppermost bits of port C of the interfacing card (PC5,6,7) is first decoded by a 3-to-8 decoder circuit (74LS138 and 74LS04). The decoded signal is then mapped to the selected loads by the circuits comprising OR gates (74LS32's) and AND gates (74LS08's), giving a TTL high-level voltage to the target driver circuits. This high-level voltage is boosted to 15V by the buffer (74LS17) and input to the high current driver chip (HV500), which produces a voltage of approximately 9V at the output, high enough to drive the IGBT into hard saturation.

Regarding the arrangement shown in figure 3.9, seven different load combinations (excluding no load) are possible, and are listed along with their associated control code in Table 3.1.

3.6 Transient Waveform Recorder HS508

In this project, all waveforms obtained from experiments are captured by HS508, a computer oscilloscope from TiePie Engineering [50]. Connected to a PC printer



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Load	Bit 7,6,5 of port C
A	001
В	010
С	011
A & B	100
A & C	101
В &С	.110
A & B & C	111

Table 3.1: Switched load and the selecting code

port, the oscilloscope working under software control can perform four measuring functions: a storage oscilloscope, a spectrum analyser, a voltmeter and a transient recorder. Measured waveforms are displayed on the computer screen and are controlled by various display control options at the bottom of the screen as shown in figure 3.11.



Figure 3.11: Computer display using the HS508

Experimental results given in Chapter 6 are measured using the oscilloscope operating in the storage mode. In this mode, a waveform is sampled at a frequency determined by the following formula:

Sampling frequency =
$$\frac{50}{\text{selected time base}}$$
 Equation: (3.7)

This gives 15,000 samples of data that can be saved into a file.⁴ The waveform displayed on the computer screen is reconstructed from this data by drawing a line between the adjacent samples. The range of the time base is from 0.2sec/div to 2μ s/div (18 values) i.e. the sample is taken at every 4ms interval (the sampling frequency = 250Hz), if the time base is set to 0.2sec/div.

Due to the digital sampling, aliasing can occur when too low a sampling rate is chosen. To avoid this, the sampling frequency must be at least twice the maximum frequency of the input signal as stated by the sampling theorem [51]. For example, to capture the output voltage containing a 100kHz ripple, the time base selected must be no more than $\frac{50}{200kHz}=0.2\text{ms/div}$.

The photographs of the prototype power supply including VIC with voltage-mode control and that with current-mode control are shown in figures 3.12 and 3.13 respectively.

⁴The file contains 15,000 lines and 4 columns of data (No. of samples, x-axis, channel 1, and channel 2). A result is obtained by plotting data in channel 1 (or 2) against the x-axis using plotting packages such as Excel, Gnuplot.



Figure 3.12: Prototype VIC with voltage-mode control



Figure 3.13: Prototype VIC with current-mode control

Chapter 4

Simulation and Modelling

This Chapter discusses two modelling approaches, an averaging method and a state-space representation method, that have been adopted to model the VIC converters in this project. In the averaging method, the converter power circuit as well as its voltages and currents are averaged to produce an averaged circuit model. Hence, any prediction from the averaged model represents only the averaged behaviour of the converter, and disregards high frequency ripple information contained in the real voltage and current waveforms resulting from switching. The averaged model provides fast and efficient means of simulation and is most favourable in the study of the converter overall performance (e.g. transient performance).

On the other hand, the state-space representation method (simulation using this technique often known as *brute-force* simulation) regards the switching converter as a time-varying linear system, in that the power circuit configuration of the converter changes as a function of time and is described by a set of linear differential equations in each topological mode. During the simulation process, the task of the simulator includes the determination of the switching instant and the solution of linear differential equations associated with each topological mode. Because instantaneous voltage and current values in the circuit are being tracked, the resulting voltage and current waveforms contain high frequency switching ripple resembling that obtained from the real converter. However, the state-space method is computationally intensive and yields excessive simulation time compared to the averaged model. Thus, it is preferred only in the analysis

where detailed cycle-by-cycle information is of importance (e.g. snubber circuit design).

In this work, the mathematical model of switching converters with VIC for use in V_{inj} optimisation is developed following the averaging approach, whilst the model developed for brute-force simulation¹ is used to study the response discrepancy due to the voltage injection at different timepoints in a particular cycle (discussed in Chapter 6). In this Chapter, the averaged model of buck VIC regulators using both voltage- and current-mode control are derived using the state-space averaging technique, as well as their SPICE equivalent circuit implementations. The development of state-space model for brute-force simulation and its SPICE implementation is covered in the later part of this Chapter.

4.1 Averaged Model

Averaging techniques are broadly categorised into two main classes following the procedures used in the derivation of the model. The first category of averaging methods is based on the direct average of a set of state-space equations that describes a system behaviour over a switching period. Briefly, the averaged model is obtained by taking a weighted average of the system matrices, where the weighting factor is a function of the duty ratio. Examples of this class are the state-space averaging technique [3,52] and its derivatives [53–59]. Reference [54,55] gives a rigorous mathematical background of averaging theory. It should be noted that the state-space averaging technique can be applied to model only PWM switching converters; for modelling a converter employing other switching techniques, such as soft switching, the averaging technique given in reference [57] is suitable.

Another approach, namely a circuit-oriented approach, is based on the identification of a three-terminal non-linear block in the converter power circuit, and the replacement of this circuit block by its equivalent averaged model established from the mathematical relation of the averaged currents and voltages between the three terminals. The PWM switch model [60-62] as well as its derivatives [63-66]

¹Note that all waveforms illustrated in Chapter 2 are results given by the state-space model.

and the switched inductor model [67,68] are examples of this class of averaging technique. The PWM-switch averaged model of a buck converter is illustrated in figure 4.1 (for the switched inductor model, the inductor is included in the nonlinear circuit block).



Figure 4.1: PWM-switch averaged model of buck converter

When properly implemented, these two averaging approaches lead to models that produce identical results [64, 67, 69]. The state-space averaging approach is, however, preferred in this project because it offers a more systematic way to achieve the final averaged model.

4.2 State-space Averaging Technique

The state-space averaging technique has been widely used in DC-to-DC converter modelling since it was first published by Middlebrook and Cuk in 1976 [52]. In essence, the technique entails the transformation of a converter which is nonlinear because of the switching action in the circuit, into an eventual linear circuit model through the modelling process illustrated in figure 4.2. It can be concisely described as follows:

For a converter operating in CCM, there exists two different power circuit topologies within a switching cycle: one is when the main switch is conducting (ON state), and the other when the diode is conducting (OFF state). The state equations governing the behaviour of each circuit state must first be written (figure 4.2(a)).



Large-signal averaged model $\dot{x} = Ax + Bv_i$ $y = C^T x$ $A = dA_1 + d'A_2$ $B = dB_1 + d'B_2$ $C^T = dC_1^T + d'C_2^T$ b

```
Small-signal purturbation

d = D + \hat{d}
d' = D' + \hat{d}'
x = X + \hat{x}
y = Y + \hat{y}
v_i = V_i + \hat{v}_i
```





Figure 4.2: State-space averaging procedure for switching converters operating in Continuous Conduction Mode (CCM)

- 2. These two sets of state equations are then averaged over a switching period (T) by weighted averaging the ON and OFF state matrices using the duty ratio as shown in figure 4.2(b). The result is a single set of state equations: a large-signal averaged model, which represents the averaged property of the two switching networks.
- 3. By introducing signal perturbations (figure 4.2(c)) into the large-signal model (figure 4.2(b)), and assuming the small-signal variation (magnitude of the pertubating variables is negligible compared to their DC values), the resulting equations become linear (figure 4.2(d)) (after neglecting the non-linear term). The steady-state and dynamic characteristics of the converter are described by the steady-state and small-signal model respectively. These two models are very useful in feedback control loop design.
- 4. From the AC small-signal model, a linear equivalent circuit denoting the canonical circuit model (figure 4.2(e)) can be derived. The equivalent circuit is unified for all three basic converters (buck, boost and buck-boost), but has different circuit parameters.

The justification of representing the switched networks (figure 4.2(a)) by the averaged model (figure 4.2(b)) relies on the effective output filter pole (f_c) being much lower than the switching frequency (f_s) . In other words, the averaged model will accurately represent the averaged behaviour of the converter when its output ripple voltage is very low [52], as:

$$\Delta V_o = \frac{\pi^2 V_o}{2} \left(\frac{f_c}{f_s}\right)^2 \qquad (4.1)$$

In SMPS design, it is normally desirable to have a low output ripple voltage; for example an output ripple voltage less than 1% of the nominal value is commonplace. Replacing the converter by its averaged model is therefore justified.

The large-signal averaged model in figure 4.2(b), together with the mathematical model of the control law developed in sections 4.3.2 and 4.3.3, form an averaged model of closed-loop converters which is used for the V_{inj} optimisation addressed in Chapter 5.

4.3 Formulation of Mathematical Model of a Buck Converter With VIC

4.3.1 Power stage

The buck converter (including circuit parasitics) shown in figure 4.3 (a) is assumed to be operating in CCM. With $R \gg r + r_L$, r and r_L can be approximated by R only. Since the converter is a second order system, two state variables are necessary in formulating the state equations: here, capacitor voltage (v) and inductor current (i) are chosen.



Figure 4.3: (a) Buck power circuit including parasitics (b) ON-state buck power circuit (c) OFF-state buck power circuit

Following the procedure outlined in figure 4.2(a), the state equations for the ON and OFF state conditions must be formulated.

For the ON state (the circuit in figure 4.3(b)):

$$\begin{bmatrix} \frac{di}{dt} \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(r+r_L)}{L} & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{CR} \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_i \qquad \text{Equation:} \quad (4.2)$$

$$V_o = \begin{bmatrix} r & 1 \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} \qquad \text{Equation:} \quad (4.3)$$

And, for the OFF state (the circuit in figure 4.3(c)):

$$\begin{bmatrix} \frac{di}{dt} \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(r+r_L)}{L} & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{CR} \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \end{bmatrix} V_i \qquad \text{Equation:} \quad (4.4)$$
$$V_o = \begin{bmatrix} r & 1 \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} \qquad \text{Equation:} \quad (4.5)$$

Equations (4.2) and (4.3) can be rewritten in the standard state-space form as:

- $\dot{x} = A_1 x + B_1 V_i$ Equation: (4.6)
- $V_o = C_1^T x Equation: (4.7)$

Similarly, the standard form of equations (4.4) and (4.5) are:

- $\dot{x} = A_2 x + B_2 V_i$ Equation: (4.8)
- $V_o = C_2^T x Equation: (4.9)$

where,

$$A_1 = A_2 = \begin{bmatrix} \frac{-(r+r_L)}{L} & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{CR} \end{bmatrix}$$
 Equation: (4.10)

$$B_{1} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix}$$
 Equation: (4.11)

$$B_{2} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$
 Equation: (4.12)

$$C_{1}^{T} = C_{2}^{T} = \begin{bmatrix} r & 1 \end{bmatrix}$$
 Equation: (4.13)

Next, equations (4.6) to (4.9) are averaged over a switching period (T), following the procedure in figure 4.1(b):

$$\dot{x} = (dA_1 + d'A_2)x + (dB_1 + d'B_2)V_i$$
 Equation: (4.14)

$$v_o = (dC_1^T + d'C_2^T)x$$
 Equation: (4.15)

Substituting equations (4.10) to (4.13) into equations (4.14) and (4.15) with d + d' = 1, a large-signal state-space averaged model of a buck converter eventually results:

$$\begin{bmatrix} \frac{di}{dt} \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(r+r_L)}{L} & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{CR} \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} dV_i \qquad \text{Equation:} (4.16)$$

$$Vo = \begin{bmatrix} r & 1 \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} \qquad \text{Equation:} (4.17)$$

Equations (4.16) and (4.17) are a non-linear continuous time model representing the average behaviour of the networks depicted in figures 4.3(b) and 4.3(c). The equations are non-linear because they contain the product of d and V_i , both of which are dynamic variables. The solution of equations (4.16) and (4.17) simulated by HSPICE [70] is illustrated in figure 4.4, where the multiplication


Figure 4.4: Simulation of buck power stage using SPICE

of two dynamic variables is handled by the use of non-linear controlled sources. The SPICE-based implementation for simulating the converter performance is described in detail in section 4.4.

In closed-loop simulation, the variable d is determined by the control law which relates d to the output voltage and some variables in the control loop discussed in the next section.

4.3.2 VIC with voltage-mode control

The mathematical model of VIC in a SMPS with voltage mode control is derived from the mathematical relationship between various elements in the control loop as illustrated in figure 4.5(a). In the figure, the power stage is now represented by equations (4.16) and (4.17), and the output voltage (equation (4.17)) is fed back through a gain block G_d , which practically can be a resistive divider, to scale V_o down to an appropriate value V'_o . Hence,

$$V_{a}' = G_{d}V_{a}$$
 Equation: (4.18)

The output of the error amplifier is given by:



Figure 4.5: (a) Mathematical model of closed-loop switching converter with VIC voltage-mode control (b) Injected voltage (c) Voltage-mode control PWM modulator

Equation:

(4.19)

$$V_e = rac{Z_2(s)}{Z_1(s)} (V_{ref} - V'_o)$$

where:

 $V_e = \text{error voltage.}$ $V_{ref} = \text{reference voltage.}$ $\frac{Z_2(s)}{Z_1(s)} = \text{gain of error amplifier.}$

It should be noted that the gain $\frac{Z_2(s)}{Z_1(s)}$ is given in the s-domain for ease of presentation. In the time-domain simulation, this value is automatically calculated by SPICE from the given compensation circuit component values.

 V_{inj} (previously defined in equation (2.4)) is mathematically a step function of two variables (figure 4.5(b)): amplitude, and injecting time, and is expressed as:

$$V_{inj} = Au(t - t_{inj})$$
 Equation: (4.20)

where,

 $u(t - t_{inj}) =$ a unit step function at time t_{inj} A = amplitude of V_{inj} t_{inj} is the injecting time defined previously in section 2.2.2

The output of the summing circuit, V_c , is thus equal to:

 $V_c = V_e + Au(t - t_{inj})$ Equation: (4.21)

The PWM modulator compares V_c to the sawtooth signal whose minimum and maximum values are E_o and V_m respectively, giving the duty ratio (figure 4.5(c)):

$$d = \frac{V_c - E_o}{V_m - Eo}$$
 Equation: (4.22)

Substituting equations (4.19) and (4.21) into equation (4.22), the VIC voltagemode control law is obtained as:

$$d = \frac{\frac{Z_2(s)}{Z_1(s)}(V_{ref} - V'_o) + Au(t - t_d) - E_0}{V_m - E_o}$$
 Equation: (4.23)

Equations (4.16), (4.17) and (4.23) therefore form a model of the closed-loop buck regulator with voltage injection control.

4.3.3 VIC with current-mode control

The diagram of a switching converter with VIC current-mode control law is illustrated figure 4.6(a). It is essentially similar to that in figure 4.5(a); thus the



Figure 4.6: (a) Mathematical model of closed-loop switching converter with VIC current-mode control (b) Current-model control PWM modulator

former equations (4.16) to (4.21) are applicable here. The mathematical model of the modulator block is, however, more complicated than the previous voltagemode control. It can be derived from figure 4.6(b) which relates the steady-state control signal V_c and sensed inductor current iR_s to the duty cycle d. It should be noticed that V_c is compensated by the slope signal M to ensure stability. From figure 4.6(b), the following relation is obtained [71]:

$$v_c - MdT - \frac{M_1dT}{2} = iR_s$$
 Equation: (4.24)

Or,

$$d = \frac{v_c - iR_s}{T(M + \frac{M_1}{2})}$$
 Equation: (4.25)

where:

 M_1 is the slope of the inductor current during the ON state, equal to $R_s\left(\frac{V_i-V_2}{L}\right)$ for a buck converter (in amp/second).

M is the slope of the slope compensation signal (in volt/second).

 R_s is the gain associated with current sensing.

The VIC current-mode control law is finally obtained by substituting equation (4.21) for V_c into equation (4.25):

$$d = \frac{\frac{Z_2(s)}{Z_1(s)}(V_{ref} - V_o) + Au(t - t_d) - iR_s}{T(M + \frac{M_1}{2})}$$
 Equation: (4.26)

In the next section, the development of SPICE equivalent circuit models of a closed-loop voltage-mode VIC converter (equations (4.16), (4.17), and (4.23)), and current-mode VIC converter (equations (4.16), (4.17), and (4.26)) are presented.

4.4 SPICE-based Implementation

SPICE, a standard circuit simulation program, is being used increasingly in modern electronic circuit design. With an appropriate circuit model, circuit performance can be accurately validated without requiring to breadboard a test circuit, thus facilitating the design process. Because of switching actions in the circuit, modelling power electronic systems normally results in non-linear/complex mathematical relations. Therefore, suitable modelling packages must provide an easy means for handling such tasks. With SPICE, non-linear modelling is facilitated through non-linear controlled sources, which are available in four different forms as illustrated in figure 4.7. These controlled sources define a function which can be either linear or polyno-



Figure 4.7: Four types of SPICE controlled sources

mial (non-linear). The polynomial functions are specified by a set of coefficients P_0 , P_1 , P_2 , ..., P_n . The meaning of each coefficient depends upon the dimension of the polynomial and is described in most SPICE text books [72,73]. An example of using controlled sources to model the multiplication of two variables is given in figure 4.8. Controlled sources are immensely useful for modelling the functions of analogue and digital blocks such as gain stages, operational amplifiers, power converters, and many others. The application of SPICE controlled sources to perform basic mathematical operations (e.g. division) and more complicated problems (e.g. transfer function modelling) is reported in [74-79].

Modelling the preceding mathematical formulas (equations (4.16), (4.17), (4.23) and (4.26)) using SPICE requires suitable selection of SPICE circuit components and their connection. The equivalent circuit model of the closed-loop VIC



Figure 4.8: Use of VCVS to model the multiplication of two variables

converters to be described next are adapted from the works in [80] and [81] respectively, by including the voltage injection control block into the original models.

4.4.1 SPICE model of the buck power stage

The SPICE equivalent circuit model of the buck power stage described by equations (4.16) and (4.17) is shown in figure 4.9. As a result of circuit averaging, the MOSFET and diode in the power circuit (figure 4.3(a)) are replaced by a fictitious DC-to-DC transformer whose function is to step down the input voltage V_i by the ratio d, presenting voltage dV_i to the output filter circuit. The SPICE circuit model of the fictitious transformer together with its associated netlist are illustrated in figure 4.9(b). The transformer action with a transfer ratio d is performed by the VCCS G1 and VCVS E1. The circuit netlist of the fictitious DC-to-DC transformer is written under the subcircuit named PWMBCK.

In order to achieve a realistic performance, the circuit component values used in figure 4.9 (see the netlist given in Appendix B2) must correspond with those in the prototype, i.e. the values of L, C, r_C , and R are measured values, and r_L is an approximated lump value including inductor resistance, the averaged value of the ON-state resistance of the MOSFET and diode, and circuit interconnection



Figure 4.9: (a): SPICE circuit model of the buck power circuit (b): Fictitious DC-to-DC transformer model

resistance. The value of the input stimulus V_i is the same as that used in the practical experiments.

4.4.2 SPICE model of VIC with voltage-mode control

The SPICE implementation of the VIC voltage-mode control described by equation (4.23) is realised by the circuit model shown in figure 4.10.

The error amplifier (the circuit surrounded by the dash line) is modelled by passive components (R's and C's), two diodes, and a non-linear controlled source, G_E . The current source G_E , which is controlled by the voltage difference between nodes 2 and 1, together with R_{EO} and C_{EO} define the error amplifier functions. Under DC operating conditions, the voltage at node 3 is given by:



Figure 4.10: SPICE circuit model of VIC voltage-mode control

$$V_3 = V_e = KR_{EO}(V_{ref} - V_o')$$
 Equation: (4.27)

where KR_{EO} is the error amplifier open-loop gain.

The error amplifier cut-off frequency is determined by R_{EO} and C_{EO} according to the formula:

$$f_{3dB} = \frac{1}{2\pi R_{EO}C_{EO}}$$
 Equation: (4.28)

Once a compensation circuit is connected, the error amplifier operation previously expressed by equation (4.27) becomes:

$$V_3 = V_c = \frac{Z_2(s)}{Z_{1(s)}} (V_{ref} - V'_o)$$
 Equation: (4.29)

where $\frac{z_2(s)}{z_1(s)}$ is the new error amplifier gain due to the compensation circuit and is automatically calculated by SPICE from the compensation circuit description.

The voltage excursion of V_3 is limited to a pre-defined band by the voltage limiter circuit, consisting of diodes and voltage sources, in which V_{EMIN} and V_{EMAX}

specify respectively minimum and maximum values of V_3 . The inclusion of the limiter circuit introduces non-ideality into the error amplifier model making it more realistic (the voltage excursion of a real operational amplifier is limited by its output capability and can be found from the data sheet).

The current source G_{PWM} , which has a current gain set to $\frac{1}{(V_m - E_o)}$, performs the addition of the voltage at node 11 (V_{inj}) to the voltage across R_C (equal to $V_c - E_o$). Hence, the voltage node 7, a product of current G_{PWM} and R_{PWM} , is equal to:

$$V_7 = R_{PWM}G_{PWM} = \frac{R_{PWM}[(V_c - E_o) + V_{inj}]}{(V_m - E_o)}$$
 Equation: (4.30)

The value of V_7 is bounded to the required range $(V_{OMIN} \text{ and } V_{OMAX})$ by the limiter circuit connected to node 7. Finally, a controlled voltage source E_D is employed to scale down V_7 by the ratio $\frac{1}{R_{PWM}}$, giving the duty ratio (d) equal to equation (4.23) at node 10.

The circuit netlist of VIC voltage-mode control is written under the sub-circuit named VICVM, which is included in the netlist in Appendix B1. The VICVM sub-circuit has external node connections as follows: nodes 1,2,3 are inverting, non-inverting and output pins of the error amplifier respectively, node 11 is an input for the injected voltage which is an independent pulse voltage source, and the output d is given at node 10.

The VICVM circuit model, together with the circuit model of the power stage in figure 4.9, complete the SPICE model of a closed-loop buck VIC converter shown in figure 4.11. In the figure, the resistors r_{d1} and r_{d2} form the resistive divider sensing the output voltage (the gain block G_d in figure 4.5). The chosen compensation circuit is constituted of passive components r_{c1} , r_{c2} , r_{c3} , c_{c1} , and c_{c1} , whose component values are designed in Chapter 6. The dash box containing a large inductor ($L_{ac}=1$ GH) and capacitor ($C_{ac}=1$ GF), and the AC stimulus source is included when performing an AC open-loop analysis e.g. the loop gain frequency response. Large values of L_{ac} and C_{ac} allow the AC analysis to be performed at the closed-loop DC operating point, and the loop gain frequency response is



obtained at node 12. The completed circuit netlist is given in Appendix B1.

Figure 4.11: SPICE model of a closed-loop buck converter with VIC voltagemode control

4.4.3 SPICE model of VIC with current-mode control

The SPICE equivalent circuit implementing VIC current-mode control (equation 4.26) is shown in figure 4.12. The error amplifier model is the same as that used previously in the voltage-mode control, thus the error voltage V_3 is expressed by equation (4.27). V_3 is added to V_{inj} from node 11 by the controlled source E_{SUM} , giving at node 6, $V_6 = V_3 + V_{11}$.

The switch current from the power circuit, equal to iR_{il} (R_{il} is the value of sensing resistor) is sensed through node 19, $V_{19} = iR_{il}$. With the UC3846 control chip,



Figure 4.12: SPICE circuit model of VIC current-mode control

the sensed current is amplified by three by the current sense amplifier inside the chip before comparing it to V_c at the comparator. This is accomplished by E_{CAMP} which multiplies V_{19} by three, such that at node 14, $V_{14} = 3iR_{il} = iR_s$, where $R_s = 3R_{il}$.

The numerator of equation (4.26) is produced by E_{NUM} which subtracts V_{14} from V_6 , hence at node 12:

$$V_{12} = V_6 - V_{14} = \frac{Z_2(s)}{Z_1(s)} (V_{ref} - V_o) + Au(t - t_d) - iR_s \quad \text{Equation:} \quad (4.31)$$

 E_{M1} multiplies the voltage between nodes 17 and 18, which is equal to $V_i - V_o$, by a gain $\frac{TR_s}{2L}$, yielding $V_{15} = \frac{TR_s(V_i - V_o)}{2L} = \frac{M_1T}{2}$, where $M_1 = \frac{R_s(V_i - V_o)}{L}$. Connected in series with E_{M1} is V_M , which is a DC voltage source with a constant value of MT. Thus at node 16 (the denominator of equation (4.26)):

$$V_{16} = MT + \frac{M_1}{2}T = (M + \frac{M_1}{2})T$$
 Equation: (4.32)

 G_{PWM} is set equal to the voltage across R_{DIV} (equal to $V_{12} - V_{10}V_{16}$), and at node 7, $V_7 = G_{PWM}.R_{PWM}$, where R_{PWM} is set to $100M\Omega$. V_7 is then scaled down by a factor of 100 by E_D , resulting in the duty ratio at node 10:

$$V_{10} = d = \frac{R_{PWM}}{100} (V_{12} - V_{10}V_{16}) = 10^6 (V_{12} - V_{10}V_{16})$$
 Equation: (4.33)

Or,

$$\frac{V_{10}}{10^6} = V_{12} - V_{10}V_{16}$$
 Equation: (4.34)

The term $\frac{V_{10}}{10^6}$ is then approximately zero. Substituting (4.31) and (4.32) into (4.34), the duty ratio, d, finally becomes (4.26).

The circuit netlist for VIC current-mode control is in the sub-circuit named VICCM and is listed in Appendix B3. Figure 4.13 illustrates the use of the VICCM model in closed-loop simulation, where the current sensing scheme is implemented by H_{il} at node 12.

Recently, the authors in [12] have refined the procedure for deriving the currentmode control law by using the transient relation of the control signal V_c and sensed inductor current iR_s depicted in figure 4.14, instead of the steady state relation (figure 4.6(b)). This results in a new current-mode control law:

$$v_c - MdT - \frac{dM_1dT}{2} - \frac{d'M_2d'T}{2} = iR_s$$
 Equation: (4.35)

which is valid for both steady-state and transient conditions.

The refined control law has resulted in a more accurate small-signal model of current-programmed converters which is reasonably accurate up to high frequency, whereas that employing equation (4.26) is valid only in the lower frequency regime. However, for large-signal conditions (time-domain simulation), there is little improvement in accuracy from the refined model compared to the steady state model [82]. Hence, the SPICE model of the current-mode control



Figure 4.13: SPICE model of a closed-loop buck converter with VIC currentmode control



Figure 4.14: Control voltage with stabilising ramp and the sensed inductor current waveforms during transient conditions

law described in this section is valid for most applications. The SPICE circuit model of the refined current-mode control law can be found in reference [82].

4.5 Direct Solution Technique

For a general DC-to-DC converter operating in CCM such as the buck converter in figure 4.3(a), the power circuit exhibits two topological modes (figure 4.3(b) and (c)) determined by the status of the switch and the diode. Because of the switching actions, these two linear networks are changing from one to the other. A system behaving as such can be described by a time-varying linear system of the form:

 $\dot{X} = A_i X + B_i U$ Equation: (4.36) $Y = C_i X + D_i U$ Equation: (4.37) i = 1, 2, ..., k

where A_i , B_i , C_i , and D_i are matrices composed of numerical constants derived from the *i* circuit topology, U is the vector of input variables, and X and Y are the state and output vectors respectively.

When this is applied to the considered buck converter, k is equal to two and the value of corresponding matrices A_1, B_1, C_1, A_2, B_2 and C_2 are readily given by equations (4.10)-(4.13) (note that $D_1 = D_2 = 0$). The input vector U is constant over the period of each topological mode, and is equal to V_i during the ON state and zero during the OFF state. The state vector contains capacitor voltage and inductor current, and the output vector is the output voltage of the converter.

The analytical solution of equation (4.36) can be expressed as [83]:

$$x(t) = e^{A_i(t-t_o)}x(t_o) + \int_{t_o}^t e^{A_i(t-\tau)}B_iU(\tau)d\tau \qquad \text{Equation:} \quad (4.38)$$

Or,

$$x(t_o + \delta t) = e^{A_i(\delta t)} x(t_o) + A_i^{-1} [e^{A_i} - I] B_i U$$
 Equation: (4.39)

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where: t_o is the initial time, δt is the time step, $x(t_o)$ is the initial value of the state vector. $e^{A_i(t-t_o)}$ is the state transition matrix for the *i*th topology.

A central issue in SMPS closed-loop simulation is not only to compute equation (4.38) but to determine when the converter moves into another configuration. This switching instant depends on the circuit operating conditions and the threshold conditions of some state variables, and hence is governed by complex relations. Once the solutions of the state vector are obtained, the output variables can then be calculated from equation (4.37).

4.5.1 Existing simulation tools

Several simulation algorithms based on the numerical techniques for solving the system described by equations (4.36) and (4.37) and their associated switching instant have been proposed by various groups of authors [83–86]. Some of these algorithms have been used in power electronics simulation programmes, commonly called *switched-circuit simulators*, such as SIMPLIS [83] and CAP [84]. The applications of the switched-circuit simulators to evaluate SMPS performances can be found in references [87–90].

Alternative to the state-space approach (equations (4.36) and (4.37)), the switching converter problems can be formulated in terms of nodal equations obtained by applying the Kirchoff Current Law (KCL) to the power circuit from which the admittance matrix can be formulated. The switching devices are constantly monitored by the control circuit simulator. Once conditions for change in circuit topology are met (switching action taking place), the admittance matrix is modified according to the new circuit configuration. This modification is usually made on some particular rows and columns of the admittance matrix, while most of the remaining parts of the matrix are still the same, since change in switch conduction state essentially affects only the two nodes connected to that switch. References [91,92] are examples of the methods based on this nodal approach. A good comprehensive overview of different power electronics simulation programs and analysis methods is reviewed in [93].

Although different solution approaches have been applied, these algorithms have in common the aim to improve the simulation time over that given by the standard circuit simulators such as SPICE or SABER, while maintaining the accuracy of the result. Excessive computation time of the standard circuit simulators are primarily caused by complex non-linear device models employed in detail-mode simulation (see section 4.5.2.1 for further details) and by the Newton-Raphson method of iteration used to solve the non-linear network in each time step. Convergence problems are also likely to occurred, most frequently due to fast changes in the circuit voltages and currents during switching transitions. The drastic difference between the time constant of the output filter and the switching period (a ratio of 1:1000 is commonplace), unique in power supply simulation, is also another major cause of convergence problems [94].

Despite these problems, SPICE is still preferred in this work because of the following reasons:

- 1. The availability and generality of the program.
- 2. Having been through several years of research and development, the software is mature and the numerical solution algorithms are robust. Furthermore, enhancement of simulation algorithms in the newer software versions yields faster simulation time and fewer convergence problems.
- 3. Recent versions of the software are equipped with features that facilitate behavioural modelling, such as ideal switches and non-linear dependent sources (behavioural-mode simulation is discussed further in section 4.5.2.2). With the behavioural approach, the simulation time and convergence problems are significantly reduced compared to when detailed-model simulation is used. The behaviour-mode simulation, coupled with the increasing performance of today's computers, makes SPICE brute-force simulation attractive.

4.5.2 Choices of simulation techniques

Two techniques, detailed-mode and behavioural-mode simulation, are available for studying the switching converter performance and are discussed below.

4.5.2.1 Detailed-mode simulation

Detailed-mode simulation uses detailed device models (or manufacturer supplied models) of semiconductor devices (e.g. MOSFETs and diodes), and the circuit to be simulated is constructed to resemble the actual circuit as closely as possible. The accuracy of the simulation depends on the models being used, and, in practice, it is very difficult to obtain exact device models [95]. Detailed-mode simulation therefore is limited and does not completely replace hardware prototyping.

Because the detailed device characteristics are usually described by a set of nonlinear equations, the simulation involves intensive calculations and often requires excessive simulation time particularly when the simulation extends over several hundreds cycles to allow for the output voltage to settle to its steady state from start-up. In this project, simulation of a buck regulator using detailed models of MOSFET, diode and operational amplifiers in the control loop has been tested, with a run-time of approximately 50 minutes by a SUN SPARC4 workstation before completion, not to mention the amount of time spent on fixing convergence problems. The problem becomes even worse as converter systems grow in size and complexity (e.g. in [94], detailed-mode simulation of a full-bridge converter (open-loop) takes about 10 minutes by a mainframe computer). For these reasons, detailed-mode simulation is impractical for use in concept verification.

However, simulation using detailed device models is still necessary in some cases such as in evaluating device power dissipation or optimising component selection.

4.5.2.2 Behavioural-mode simulation

In contrast, behaviour-mode simulation employs simplified device models (sometimes called macromodels) which represent only its external characteristics, omitting its detailed characteristics. For example, to simulate a switching converter in behavioural mode, the MOSFET can be modelled by an ideal switch which has zero on-state resistance and infinite (open circuit) off-state resistance. Replacing non-linear devices in the circuit with the appropriate macro-models greatly helps to accelerate the simulation and alleviate convergence problems, but with a trade-off of losing some accuracy. Behaviour-mode simulation is generally suitable for concept verification in SMPS design and analysis, and is preferred to detailed-mode simulation in this work.

4.5.3 Behavioural simulation options

To simulate the buck VIC converter in figure 4.3(a), the power MOSFET and the diode are modelled by suitable macro-models. The two behavioural modelling approaches shown in figure 4.15 are considered.

The switching function approach [95,96] in figure 4.15(a) models the block containing the main switch and the diode with controlled voltage and current sources. The switching function f(t) is a duty cycle, and $V_o(t) = f(t)V_i$ and $I_{in}(t) = f(t)i_L$ are the input voltage to the output filter and the input current of the buck converter respectively.

Another equivalent approach is illustrated in figure 4.15(b), where the individual solid-state switches are replaced by ideal switches controlled such that they are conducting alternately, simulating the converter operation. When correctly implemented, results given by these two approaches are identical, but the simulation time of the switching function method is slightly faster. The reason for this is that the switching function model results in an overall equivalent circuit with fewer circuit components and nodes. As an example, the simulation time of the buck converter in figure 4.3(a) from start-up to steady state (figure 4.16) using



Figure 4.15: Two behavioural models of a buck converter: (a) Switching function model (b) Ideal switch model

HSPICE running on a SUN SPARC4 workstation is about 4 seconds and 7 seconds for the switching function and ideal switch respectively. It should be noted the circuit parameters used in this simulation are the same as that specified in figure 4.4 and, hence, the simulated result in figure 4.4 is an averaged waveform of figure 4.16. For closed-loop simulation, the control circuit (described later in section 4.5.4) must be incorporated to regulate the output voltage and this will increase the simulation time. To simulate the start-up performance similar to that in figure 4.16 in closed-loop configuration, it takes 97 seconds and 125 seconds for the switching function and ideal switch respectively.

The major disadvantage of the switching function model is that it disguises the circuit from its original form, and results in an equivalent circuit in which the individual solid-state switches no longer exist. Therefore, it is not possible to monitor the voltage/current or conduction state of these switches. For this reason, coupled with the fact that the simulation time of these two methods is approximately the same, the ideal switch approach (figure 4.15(b)) is favoured in this project.



Figure 4.16: Start-up simulation of a buck power circuit employing switching function/ideal switch model

4.5.4 SPICE closed-loop brute-force simulation

Ideal switch model

The SPICE equivalent circuit model of an ideal switch [97,98] is shown in figure 4.17. It is constructed from controlled voltage sources and resistors which have been arranged such that the equivalent resistance across terminal A-B of the circuit is periodically varying between zero and infinity (practically a very high resistance), depending on the value of the control pulse $V_{in}(t)$ at node C.

By assigning the controlled source E_1 equal to the voltage across the resistor R_D , $V_1(t)$, the equivalent current I_{eq} through the circuit is:

$$I_{eq}(t) = \frac{V_1(t)}{R_D} = \frac{V(t) - E_g(t)}{R_D}$$
 Equation: (4.40)

The equivalent voltage at terminal A-B is:

$$V_{eg}(t) = E_g(t)$$
 Equation: (4.41)



Figure 4.17: Equivalent circuit model of the ideal switch

From equations (4.40) and (4.41), the equivalent resistance across terminal A-B is thus equal to:

$$R_{eq}(t) = \frac{V_{eq}(t)}{I_{eq}(t)} = \frac{E_g(t)R_D}{V(t) - E_g(t)}$$
 Equation: (4.42)

By substituting the switches SW1 and SW2 in figure 4.15(b) with the ideal switch model (figure 4.17) and using equation (4.42): $E_g(t) = V(t)[1 - V_{in}(t)]$ for SW1 and $E_g(t) = V(t)V_{in}(t)$ for SW2, $R_{sw1}(t)$ and $R_{sw2}(t)$ finally become:

$$R_{sw1}(t) = \frac{[1 - V_{in}(t)]R_D}{V_{in}(t)}$$
 Equation: (4.43)

And,

$$R_{sw1}(t) = \frac{V_{in}(t)R_D}{[1 - V_{in}(t)]}$$
 Equation: (4.44)

When $V_{in}(t)$ is a pulse signal with amplitude equal to one, it can be seen from equations (4.43) and (4.44) that $R_{sw1}(t)$ and $R_{sw2}(t)$ are periodically switching between 0 and ∞ , but with opposite conduction states; i.e. when $R_{sw1}(t) = 0$,

 $R_{sw2}(t) = \infty$ and vice versa, emulating the operation of the diode and MOSFET in the circuit.

The netlist of the ideal switch model is written under the sub-circuit named SW1 and SW2 listed in figure 4.17. In closed-loop simulation, $V_{in}(t)$ is a duty cycle and derived from the control circuit.

Control circuit model

Unlike the control circuit model used previously in the state-space averaged simulation which outputs a continuous duty ratio (section 4.4.2), the output of the control circuit in brute-force simulation (figure 4.18(a)) is a PWM duty cycle driving the ideal switches. The duty cycle output is obtained by direct comparison of the error amplifier output V_{ϵ} to a constant-frequency sawtooth waveform V_{saw} .

The error amplifier circuit model is the same as that previously used in the averaged model (section 4.4.2), therefore it is not described again here. The simplified SPICE circuit model of the comparator is illustrated in figure 4.18(b). The voltage across R_{comp} represents the comparison result of V_e to V_{saw} and is amplified by a thousand by the controlled source E_{comp} . The resulting positive and negative voltages are respectively clamped to between one and zero by the voltage limiter at the output stage.

The complete SPICE circuit netlist of a closed-loop buck converter for behavioural brute-force simulation is given in Appendix B4.

Convergence problems and remedies

The most serious problem associated with SPICE simulation of the above switched system is non-convergence of a result, which causes the simulation to cease prematurely. As mentioned in section 4.5.1, the cause of this problem is due to the fast changes in currents and voltages in the circuit occurring during switch transition and the great difference in time-constant between sub-systems. The probability of convergence problems arising is likely to increase with increased



Figure 4.18: (a) Voltage-mode control circuit used in behavioural-mode simulation (b) Comparator model

switching frequency.

Solving the convergence problem requires a good understanding of the models, experience with the software, and, to some extent, trial and error. From the author's experience, non-convergence associated with the error message *internal time step too small* arose most frequently during the course of simulations. Some effective procedures to overcome this and related convergence problems have been suggested in [99–101], in which attempts to alleviate the problem have been mainly focussed on the decrease of timestep used in the simulation², the appropriate se-

²A smaller timestep results in a longer simulation time.

lection of the numerical integration algorithm, and the relaxation of some error tolerances.

In the netlist given in appendix B4, the HSPICE control options have been carefully selected to minimise the convergence problems while retaining result accuracy, and have been proven after several trials with different operating conditions. These options are concisely described as follows:

- PIVOT=13 selects the best pivoting algorithm available in HSPICE. PIVOT is an algorithm for re-ordering matrix elements and is usually used to achieve convergence in circuits that produce hard-to-solve matrix equations such as switching regulator circuits, whose major circuit component values result in a large conductance matrix (L's and C's are in the order of 10⁻⁶).
- DVDT=2 allows the internal time step³ to be adjusted based on the node voltage rate of change. It is used in conjunction with ABSVAR=0.2, FT=0.2 and RELVAR=0.2, all of which specify the convergence criterion at each timepoint to generate very accurate results, with the trade-off of a somewhat longer simulation time [70].
- ACCT, PROBE and POST are general control options. ACCT allows run time statistics to be reported at the end of the output file. POST generates a post-processing file of the simulated results for displaying in the GSI environment, a waveform display programme. PROBE limits the postprocessor output just to the selected variables (by default HSPICE outputs all variables).

³The internal time step used during the computation is different from the timestep specified in .TRAN card.

Chapter 5

Optimisation of Injected Voltage

Using the mathematical model of the VIC converter developed in Chapter 4, optimisation of V_{inj} can now be carried out. The basic concepts of optimisation are reviewed at the beginning of this Chapter. Multi-objective optimisation, the approach taken to optimise V_{inj} , is then described, followed by a brief description of the operation of HSPICE optimisation and its related commands (statements) used in performing the optimisation.

In this project, although the principal application of HSPICE optimisation is to optimise the injected voltage, it has also been applied to assist in the design of the error amplifier compensation circuit. Design outlines and considerations associated with both of these applications are described in sections 5.4 and 5.5. All results are given in Chapter 6.

5.1 Overview of Optimisation

Optimisation is a numerical technique associated with the search for a set of allowed values of variables for which the objective function assumes an optimal value. It has been found to be very useful in solving problems in a wide variety of subject areas, including mathematics, applied science, engineering, economics, medicine and statistics. In control system design, optimisation can play an important role in assisting the designer to select optimal controller parameters to satisfy design requirements [102,103]. In mathematical terms, optimisation is essentially a problem of function minimisation (or maximisation), usually under conditions in which the input variables are subjected to constraints. For example, design of an RC network to meet simultaneously desired time constant and power dissipation specifications (design objectives) requires optimisation of the R and C values (input variables). The constraints in this optimisation arise from the fact that the components values cannot be negative and normally occupy only a particular band of values. The general form of optimisation problems may be represented by [104]:

 $egin{aligned} \hline minimise & F(x) \ x \in A \ & subject \ to & c_i(x) = 0, \ i = 1, 2, ..., m'; \ & c_i(x) \leq 0, \ i = m' + 1, ..., m. \end{aligned}$

Equation: (5.1)

where:

F is an objective function or a measure of goodness of the system under consideration, and relates in some way with a variable vector x. $x = [x_1, x_2, ..., x_n]$ represents a vector of variables. c_i is a constraint function that defines acceptable values of the variables A is an arbitrary domain, part of which includes all values of x.

From equation (5.1), any point x that satisfies all the constraints is said to be *feasible*, and the set of all feasible points is termed the feasible region. For instance, the feasible region of a two-variable function with the variable constraints of $x_1^2 + x_2^2 \leq 1$ and $x_1 + x_2 = 0$, would cover all points on the straight line inside the unit circle, including the values where these two curves intersect, as shown in figure 5.1.

In optimisation, the task of an optimiser is to search for a value of variables in the feasible region that gives a minimum (or maximum) value to the objective function. The optimiser is a computer program based on suitable mathematical optimisation algorithms. Many optimisation algorithms have been developed, usually made up of two main components [105]: the search for the values of variables that are likely to make the objective function minimum (or maximum), and



Figure 5.1: Feasible region of a function of two-variable constrained by $x_1^2 + x_2^2 \le 1$ and $x_1 + x_2 = 0$

the validation of these points. It is the method of selecting a suitable search direction that fundamentally distinguishes optimisation algorithms from one another. In general, the variable search for optimal values can be written, in recursive form, as:

$$x^{r+1} = x^r + \alpha^r d^r$$
 Equation: (5.2)

where,

 x^{\prime}

 x^{r+1} is a vector of new variable values.

 x^r is a vector of current variable values.

 d^r is a direction vector which indicates the current search direction.

 α^r is a scalar and determines how far to move in the current search direction.

The graphical interpretation of the above equation is illustrated by the search on the two-variable surface shown in figure 5.2, where the selected search direction $\alpha^0 d^0$ yields the reduced function value on the first iteration. Convergence to a minimum is usually achieved if at each iteration, $\alpha^r d^r$ is chosen to reduce the function value.

Using search strategies as a criterion [105], optimisation methods can be divided into the direct search method, where only a computed value of the objective



Figure 5.2: An example of search on a 2-variable surface

function is required to establish the search direction, and the gradient method, where the computation of first and/or higher derivatives of the objective function is required to determine a suitable search direction. Examples of optimisation algorithms that employ the direct search strategy are the simplex method and Powell's conjugate direction method, and that employ the gradient search strategy are the steepest descent method and Newton's method. More detail of various available optimisation algorithms can be found in most optimisation text books [104,105].

5.2 Multi-Objective Optimisation

In control system design, the design specifications and the constraints imposed on the design variables typically specify an acceptable design. These specifications are often in conflict and are likely to be competing with one another, such that an improvement in one specification leads to a degradation in at least one of the remaining specifications. For example, in SMPS control loop design, increasing the system loop-gain bandwidth will increase the speed of dynamic response, but at the expense of high voltage overshoot and ringing. Therefore, a compromise between these multiple competing objectives has to be reached in a way that satisfies all objectives.

When single-objective optimisation (equation (5.1)) is used, various design ob-

jectives are aggregated to form a single objective function before the optimisation is carried out [106]. However, as the design objectives are likely to be competing with one another, one cannot aggregate these objectives into a single-objective function until the relative importance of the objectives and their trade-offs are well understood [107]. In this case, problem formulation using equation (5.1) is not straightforward.

Multi-objective optimisation [108] is a suitable technique for formulating and solving this category of problem, and has the general form of:

$minimise \ x \in A$	$\underline{F}(x)$	
subject to	$c_i(x)=0,$	i = 1, 2,, m';
	$c_i(x) \leq 0,$	i = m' + 1,, m.

Equation: (5.3)

where,

 $\underline{F}(x) = [F_1(x), F_2(x), ..., F_m(x)]$ represents the n design objectives.

Conflict between some (possibly all) of the components of $\underline{F}(x)$ can result in the multi-objective problem having no unique optimal solution, but rather a set of non-inferior or compromised solutions, the solutions on the trade-off surface. The graphical illustration of non-inferior solutions can be seen in figure 5.3. The optimised variables and the correspondent value of objective functions are shown in figure 5.3(a) in which the variables k_1 and k_2 could be, for example, the magnitude of V_{inj} and the injecting time respectively, and the objective functions F_1 and F_2 could be the output voltage settling time and overshoot respectively. The conflict between two design objectives is seen between region C and D in figure 5.3(b), where the improvement in F_1 at point B ($F_{1B} < F_{1A}$) leads to a degradation in F_2 ($F_{2B} > F_{2A}$).

To find non-inferior solutions in multi-objective problems, equation (5.3) is usually reformulated into an appropriate single-objective problem, such that all the design objectives are taken into account simultaneously during optimisation, enabling any suitable single-objective optimisation algorithm to compute the solu-



Figure 5.3: (a) Mapping from the variables plane into the objective functions plane of the two-objective functions of two variables, (b) Showing the non-inferior solution set

tion. One such effective conversion method is goal attainment (also used in MAT-LAB optimisation toolbox [109,110]), which reformulates equation (5.3) into:

 $\begin{array}{ccc} \hline minimise & \lambda \\ x,\lambda \in A \\ subject \ to & F_i(x) - w_i\lambda \leq F_i^* \quad i=1,2,...,n \end{array}$

Equation: (5.4)

where:

 λ is a dummy scalar variable,

 F_i^* are the goal values of individual objectives,

 $w_i \geq 0$ are designer-selected weighting coefficients.

The dummy variable λ and the input vector x are the optimising variables, and all objectives are treated as constraints which have to be met in the optimisation. Minimisation of λ tends to force all specifications to meet their target value (goals). If λ is negative, then the goals have been over-attained (i.e. $F_i(x) < F_i^*$) and if λ is positive, then the goals have been under-attained (i.e. $F_i(x) > F_i^*$). Hence, the quantity $w_i \lambda$ represents the degree of under- or over-attainment. Although the concept of multi-objective optimisation is adopted in performing optimisation in this work, problem formulation in equation (5.3) or goal attainment method in equation (5.4) is not normally practical for optimising switching converter performance, because the objective functions $F_i(x)$ which relates design objectives to design variables is very complicated. The more viable approach to find optimised solutions is to use simulation/optimisation strategy - by iteratively simulating a circuit, evaluating its performance, and optimising the design variables on each iteration run until the design objective are met. By this way, optimisation reduces to the problem of minimising the error function that describes the difference between the desired goal value and the actual value.

Such an optimisation environment is supported in HSPICE [70], and also in newer versions of PSPICE (from Microsim Corp.) and IntuSPICE (from Intusoft Corp.). HSPICE is used in this work to perform optimisation of the injected voltage (equation (4.20)), and also to assist in designing the error amplifier compensation circuit in the prototype voltage-mode converter. The optimisation is carried out employing the SPICE circuit models developed in Chapter 4. The HSPICE optimisation environment and essential HSPICE commands (statements) for performing the optimisation are described in section 5.3.

5.3 Optimisation With HSPICE

HSPICE from Meta-Software Corporation is a SPICE-based circuit simulator developed from SPICE2 of the University of California Berkeley. Incorporating features from SPICE2 and other similar circuit simulation programs, the simulation algorithms used by HSPICE have been enhanced to give superior convergence. With features such as Graphical Simulation Interface (GSI) and a circuit optimiser, the HSPICE package provides an efficient design environment. GSI is the environment for interactive waveform graphing from multiple simulations, similar to SCOPE of IntuSPICE or PROBE of PSPICE.

The optimisation design scheme in HSPICE (illustrated in figure 5.4) is an iterative design environment embracing circuit simulation, performance evaluation, and design variable optimisation until either convergence is declared, or no solu-



Figure 5.4: Optimisation design scheme in HSPICE

tion is found after a pre-defined maximum number of iterations. To perform the optimisation, information concerning the optimisation task (e.g. design variables and objectives) must be stated in the netlist as shown in figure 5.5, in addition to the circuit description.

The optimisation is set up by the .MODEL statement with keyword OPT, which allows optimisation control options (e.g the convergence criterion, the optimisation algorithm, etc.) to be selected. For example,

.MODEL Vinj-opt OPT ITROPT=25 RELIN=1e-3 RELOUT=1e-3

This assigns Vinj-opt as the optimisation reference name, ITROPT=25 limits the maximum number of iterations to 25, and RELIN=1e-3 and RELOUT=1e-3 specify that convergence be declared when either all input variables or all results vary by no more than 0.1% from one iteration to the next.

The design variables are defined through the .PARAM statement in which the



Figure 5.5: Structure of HSPICE optimisation netlist

initial guess, minimum and maximum values are specified. For example,

.PARAM Vinj-amplitude optval(0.234,0,0.39)

assigns Vinj-amplitude a design variable with the initial guess, minimum and maximum values of 0.234, 0, and 0.39 respectively. **optval** is a unique reference name and is referred to by the analysis statement (.TRAN, .AC, or .DC with the keyword **OPTIMIZE**) to permit optimisation of this variable.

The design objectives (the desired specifications) are stated through the .MEAS-URE statement. For example,

.MEASURE tran tset trig at=100us targ V_{out} val=14.9V RISE=1 goal=1ms

specifies tset as the variable being evaluated, and that the value of 1ms (goal=1ms) is being sought. The measurement is started at the timepoint $100\mu s$ (trig at=100us) and ended when the output voltage first reaches 14.9V (V_{out} val=14.9V

RISE=1). In other words, the above .MEASURE statement states that an output voltage transient response with a settling time of 1ms is being sought in the optimisation. This form of .MEASURE statement is suitable for the optimisation of time-related variables e.g. rise time, settling time etc. Another form of the .MEASURE statement found useful in this work is:

.MEASURE tran overshoot max V_{out} from=250us to=1ms goal=15.075V

This specifies the variable **overshoot**, the maximum output voltage between the time 250μ s and 1ms, with a maximum value of 15.075V being sought. For multi-objective optimisation, individual objectives are each given by a separate .MEASURE statement.

The iterative simulation and optimisation environment in figure 5.4 is completed by HSPICE optimisation analysis statements (.DC, .AC, or .TRAN with the keyword **OPTIMIZE**). For example,

.TRAN 10u 2m SWEEP OPTIMIZE=optval RESULTS=tset MODEL=Vinj-opt

specifies that iterative transient analysis and optimisation of the design variable **Vinj-amplitude (OPTIMIZE=optval)** be carried out, until either the design objectives are achieved or the maximum number of iterations is reached. The latter is defined by the keyword **ITROPT** in the .MODEL statement; if not specified, the default value of 20 is used. The analysis is started at timepoint 0 and ended at timepoint 2ms, with a timestep of $10\mu s$. **RESULTS=tset** passes the simulated results of tset to the .MEASURE optimisation statement for evaluating if the goal has been met. **MODEL= Vinj-opt** notifies HSPICE that it should adopt the optimisation control options specified in .MODEL statement (with the keyword **OPT**).

Detailed usage of these statements is explained in the HSPICE manual [70]. In the following sections, the application of HSPICE optimisation to design the compensation circuit and to optimise the injected voltage is described, using the SPICE circuit models developed in Chapter 4.

5.4 SMPS Control Circuit Design

5.4.1 Design in the frequency domain

Design of linear time-invariant Single Input Single Output (SISO) control systems is normally carried out in the frequency domain. In SMPS, the error amplifier compensation circuit is usually designed using a Bode plot, from which the required compensation circuit frequency characteristic is obtained by subtracting the control-to-output frequency characteristic of the converter from the required loop-gain frequency characteristic. The desired circuit component values can then be calculated.

In the following sections, the frequency response design method, considerations and limitations are examined.

5.4.1.1 Design overview

Figure 5.6 shows the basic block diagram of a SMPS from the control system point of view, consisting of the power circuit, PWM modulator, and error amplifier with the compensation circuit (compensator), with transfer functions T_{pw} , T_{mod} , and T_{err} respectively. There is an additional, inner current loop for systems using current-mode control. The frequency characteristics of transfer functions T_{mod}



Figure 5.6: SMPS closed-loop block diagram

and T_{pw} are pre-determined by the choice of control strategy and power circuit
topology respectively. As a result of many years of research in switching converter modelling, the frequency characteristic of the product $T_{mod}T_{pw}$, often known as the small-signal control-to-output transfer function, is well understood for both voltage-mode and current-mode converters (e.g: [52] discusses converters with voltage-mode control, and [9] discusses converters with current-mode control). Hence, the remaining task is to define T_{err} to give the desired open-loop frequency characteristic ($T_{pw}T_{mod}T_{err}$) and thus obtain the desired converter performance, while maintaining a stable system.

5.4.1.2 Stability considerations

For a system to be stable, the phase lag of the open-loop transfer function at the crossover frequency, f_c (the frequency at which the gain on the Bode plot crosses 0 dB), must not exceed 180° (in addition to the normal 180° phase shift associated with a negative feedback). However, according to Nyquist's stability criterion, the phase lag is permitted to be greater than 180° at frequencies below f_c . If this is the case, the system is said to be conditionally stable; however, it is not good practice to have a conditionally stable system because it is prone to becoming unstable.

Two importance parameters for indicating system stability are the phase and gain margins. The phase margin is defined as the phase shift from 180° at f_c , and the gain margin is the amount of gain (below unity) when the total phase shift is 180° (figure 5.7). In system stability prediction, the phase margin is more often used than the gain margin because it is a more intuitive indicator; for instance, a system with a small phase margin (where total phase shift is close to 360°) will exhibit considerable overshoot and ringing.

5.4.1.3 Design objectives

The design objective is to design a compensation circuit that results in an overall open-loop frequency characteristic with a high gain out to high frequencies (i.e.



Figure 5.7: Graphical illustration of phase and gain margins

large loop-gain bandwidth), while maintaining a sensible value of phase margin and avoiding conditional stability. Ideally, one would wish to select f_c as high as possible, so that the system can respond more rapidly. However, the phase lags of various elements in the control loop increase with frequency, limiting f_c to a value for which the phase lag is still manageable. Typically, a phase margin of at least 45° with f_c limited to maximum one third of the switching frequency is required for a stable system [111].

The open-loop frequency characteristic is related to both steady state and dynamic performances in the time domain as follows:

- High loop gain at low frequency provides good steady state regulation.
- Large loop-gain bandwidth (high f_c) indicates a system with a fast dynamic response.
- A system with a small phase margin exhibits response with considerable overshoot and ringing.

5.4.1.4 Limitations

Design with the frequency response technique essentially involves the graphical subtraction/addition of the Bode plots of the components that constitute the closed-loop system. Asymptote lines are usually used in constructing the plots to simplify the design process, which introduce small errors. After the desired frequency characteristic of the error amplifier block (T_{err}) has been identified, compensation circuit component values are calculated from the location of the poles and zeros on that plot (the application of this technique to the design of a SMPS compensation circuit is demonstrated in Chapter 6).

Although it is relatively simple, the frequency domain method has the following limitations:

- The power supply is assumed to be linear with small-signal perturbations around the operating point; whereas in practice, a converter can be subjected to large signal disturbances, either from line or load changes.
- The design is carried out in the frequency-domain, whereas the target specifications are time-domain parameters (voltage regulation, maximum deviation from nominal and recovery time under transient conditions). There is no simple quantitative relation between the open-loop frequency characteristics and the time-domain performances. Therefore, it is common that the desired specifications are not met at the first attempt, with fine-tuning required, usually on a trial-and-error basis.
- The effect of circuit/device parasitics are usually omitted to simplify the design process.

5.4.2 A new optimisation based design

The above limitations of design in the frequency domain were identified during the development of the prototype control board. The quest for an alternative design method which can overcome these limitations is therefore required and has led to the proposal of a new Computer Aided Design (CAD) method, namely optimisation design using HSPICE [112].

5.4.2.1 Related work on using CAD to design SMPS compensation circuits

Circuit simulation programs such as SPICE and SABER are being used increasingly in SMPS design to validate accurately the initial design results. In [113], the author shows how SPICE can be used to evaluate both frequency- and timedomain performances without the necessity of breadboarding a circuit. The SMPS design environment in [114] carries out the compensation circuit design by repeatedly simulating the circuit using an averaged model and validating its performance, until a satisfactory result is met. Because a trial-and-error approach is used to adjust the circuit component values for each simulation run, it can be very time consuming, particularly when designing for stringent specifications.

MATSPICE, a compensation circuit design environment using optimisation, has been proposed in [115, 116]. The package uses MATLAB for carrying out optimisation and result evaluation, and PSPICE for simulating the converter performance: communication between the two programs is facilitated by C interfacing routines. Even though MATSPICE yields improved design results compared with conventional design methods, the authors mention that the execution time of the program is slow, owing to the considerable amount of data being transferred between MATLAB and PSPICE for each optimisation iteration, preventing it from being an efficient design tool.

Although the approach taken is similar to MATSPICE, HSPICE optimisation design is superior in term of speed, as with a built-in optimiser there is no unnecessary time lost in data transfer between packages. The execution time of HSPICE optimisation depends only on the complexity of the optimisation problem.

With HSPICE optimisation, all essential attributes lacking in frequency response design are fulfilled:

- A non-linear, large-signal averaged model (sections 4.4.1 and 4.4.2) is used, instead of a linear small-signal model.
- The design is carried out directly in the time-domain and automatic finetuning of the design is accomplished through iterative simulation and optimisation (figure 5.4).
- The circuit parasitics can easily be incorporated (section 4.3.1)

The application of optimisation to the design of an error amplifier compensation circuit is demonstrated in Chapter 6.

5.5 V_{ini} Optimisation

Optimisation of V_{inj} (equation (4.20)) to achieve the desired transient performance to load changes is characterised as a multi-objective optimisation problem. The desired performance is specified by a set of transient specifications, i.e. settling time, voltage overshoot, maximum voltage deviation and spike voltage. There usually exists a set of non-inferior solutions for V_{inj} that do not violate the specifications. The number of possible solutions for V_{inj} is dependent on the stringency of the imposed specifications and the resolution of the amplitude of V_{inj} . From these non-inferior solutions, the trade-off between these conflicting objectives can be studied.

5.5.1 Optimising variables and constraints

The magnitude of V_{inj} and the number of cycles in advance of load switching that V_{inj} is applied must both be optimised (equation (4.20)) to achieve the desired transient performance. As mentioned before in section 2.2.1, the amplitude of the injected voltage is a discrete variable due to the finite word length used to store the value of V_{inj} . The resolution of the D/A converter, which dictates the difference between any two consecutive values of V_{inj} and is set to 19.5mV, poses the following variable constraint in the optimisation:

 $A_{i+1} - A_i = 0.0195, \quad i = 0, 1, 2, ..., 255$ Equation: (5.5)

where, A is the amplitude of V_{inj} . It should be noted that the 8-bit word length used limits the maximum value of i to 255.

By the definition given in section 2.2.2 (see also figure 2.9), the injecting time (t_{inj}) is the number of cycles in advance of the load application and, thus, is a discrete variable whose feasible values are restricted to positive integers (I^+) . This introduces another variable constraint into the optimisation:

 $t_{inj} \subset I^+$ Equation: (5.6)

The above equation defines t_{inj} as a subset of I^+ .

5.5.2 Design objectives

The stringent transient performance specifications in table 5.1 are chosen as the design objectives for the optimisation. The voltage overshoot as well as the

Load transient performance	desired value
maximum voltage overshoot	15.075 volts
maximum spike	15.075 volts
settling time	250 microseconds

Table 5.1: Desired transient performance under various load changes

spike voltage must not exceeded 0.5% of the nominal output voltage (15V for the voltage-mode prototype converter), while the settling time, taken to be when the response has settled to within $\pm 0.5\%$ of the nominal value, must be satisfied. The maximum voltage deviation is not included as it is not normally a critical parameter for power supplies in radar applications. However, in other applications this might be a critical parameter which would need to be included. It is required that all specifications in table 5.1 must be satisfied under all possible load conditions. To demonstrate the conflict between transient specifications in SMPS design, simulation of the switching converter subjected to a step-load change with voltage injection control is shown in figure 5.8, using the averaged model developed in Chapter 4. When the magnitude of V_{inj} is increased with t_{inj} constant (figure 5.8(a)), the maximum voltage deviation is reduced substantially at the expense of increased voltage overshoot, while the spike voltage is insignificantly increased. In this case, the maximum voltage deviation and voltage overshoot are two conflicting objectives. On the other hand, when t_{inj} is increased and the magnitude of V_{inj} is kept constant (figure 5.8(b)), the spike voltage is increased rapidly, while both maximum voltage deviation and voltage overshoot are modestly reduced. This indicates the conflict between the spike voltage and the maximum voltage deviation, and voltage overshoot. In both cases, the settling time is dependent on how closely the optimum band has been specified.

Details of V_{inj} optimisation, the associated results, as well as the identification of the necessary trade-offs are given in the next chapter.



Figure 5.8: Illustration of competing design objectives: (a) The amplitude of V_{inj} is changed and the injecting time is constant, (b) The injecting time is changed and the amplitude of V_{inj} is constant

Chapter 6

Results

This chapter is organised into two main sections. The first section is dedicated to the error amplifier compensation circuit, where the detailed design procedures are given and the associated results presented. The capability of HSPICE optimisation as a powerful tool for the design of SMPS compensation circuits is illustrated in this section.

The second part of this chapter presents all relevant results obtained from the VIC investigation. These include V_{inj} optimisation results and the corresponding experimental and simulated results. The experimental results of the VIC current-mode converter is also presented.

6.1 Compensation Circuit Design

The design of the error amplifier compensation circuit in the prototype voltagemode control circuit is discussed in this section. The frequency response design method is first employed to obtain the preliminary compensation circuit component values. Then, the optimisation design using HSPICE described in section 5.5 is used to "fine-tune" the initial results.

6.1.1 Frequency response design

6.1.1.1 Design objectives

The two-pole, two-zero error amplifier compensation circuit in figure 6.1 is designed to satisfy the following objectives:

- 1. The required regulation limits are $\pm 0.5\%$ of nominal output voltage.
- 2. A settling time of no more than 1ms is required, when the converter is subjected to a 2.75A step-load change (68% of maximum step-load current).

6.1.1.2 Control-to-output frequency characteristic

The small-signal control-to-output transfer function $(T_{mod}T_{pw}$ in figure 5.6) of a buck converter operating in CCM is expressed as [117]:

$$\frac{\hat{V}_o}{\hat{V}_e} = \left(\frac{V_{in}}{V_s}\right) \left(\frac{1 + \frac{s}{w_z}}{1 + \frac{s}{w_oQ} + (\frac{s}{w_o})^2}\right)$$
Equation: (6.1)

where,

 $w_o = \frac{1}{\sqrt{LC}}$ is the second-order output filter pole. $w_z = \frac{1}{r_c C}$ is the zero due to the capacitor ESR. $Q = \frac{R}{w_o L}$ is the Q-factor.

 V_s is the peak of the sawtooth voltage and equal to 3.5V for the UC3524A control chip.

 V_{in} is the input voltage of the converter.

The power circuit parameters are: $C = 470 \mu F$, $L = 50 \mu H$, $r_c = 0.027\Omega$, and $R = 20\Omega$, and the input voltage is 33V. By substituting the corresponding parameters into equation (6.1), the Bode plot of the control-to-output transfer function, with an asymptote line assumption, is drawn as shown in figure 6.2(a), where:

Low frequency gain $G_1 = \frac{V_{in}}{V_s} = 19.5 \text{dB}$, Corner frequency $f_o = \frac{w_o}{2\pi} = 1040 \text{Hz}$, ESR zero $f_z = \frac{w_z}{2\pi} = 12.5 \text{kHz}$

Note that using the asymptote line approximation, the gain peaking at the corner frequency (f_o) determined by the Q factor is ignored. Also it results in small errors of 3dB and 5.7° at the location of poles and zeros in the gain and phase plots respectively.

6.1.1.3 Error amplifier compensation circuit frequency characteristic

The chosen compensation circuit has a gain frequency characteristic as shown in figure 6.1. Also included in the figure is the relation between the poles and zeros, and the circuit component values. The position of the poles and zeros is to be determined in the design process. It should be noted that in figure 6.1, the



Figure 6.1: An error amplifier with a two-pole, two-zero compensation circuit, together with its gain frequency response

asymptote line is again used and the error amplifier itself is assumed to be ideal.

6.1.1.4 Error amplifier compensation: first design attempt

As mentioned in section 5.4.1.3, the primary objective in error amplifier compensation is to design the compensation circuit such that it results in an open-loop frequency characteristic having a high gain out to high frequency, while remaining unconditionally stable. The following design procedure has been adopted from the method used in [117]. The Bode plot corresponding to the first design attempt is shown on the left-hand side in figure 6.2, with the design detail summarised below:

- 1. The crossover frequency (f_c) is chosen at a quarter of the switching frequency, thus $f_c=25$ kHz. In figure 6.2(a), the control-to-output gain at f_c is -29dB. Therefore, in order to result in a zero open-loop gain, the error amplifier gain required at f_c must be equal to 29dB.
- 2. The first pole (f_{p1}) of the error amplifier occurs at a very low frequency (less than 1Hz). This provides a sufficient open-loop gain at low frequency to give good regulation (practically, the gain is limited by the output capability of the error amplifier).
- 3. The second order filter pole (f_o) in figure 6.2(a) is compensated by the two zeros (f_{z1}, f_{z2}) placed together at $\frac{f_o}{2} = 519Hz$. This is to compensate for a rapid phase shift caused by the second order filter pole.
- 4. The error amplifier second pole f_{p2} cancelling the ESR zero (f_z) is normally placed at least five times above f_o to avoid adding more phase lag at f_o . In this first design attempt, it is set equal to f_z , thus $f_{p2} = f_z = 12.5 kHz$.
- 5. By adding the frequency response of the control-to-output gain (figure 6.2(a)) to that of the compensated error amplifier gain (figure 6.2(b)), the resulting open-loop gain frequency response is obtained as shown on the left-hand side of figure 6.2(c).

From figure 6.2(b), the compensation circuit component values are calculated as follows:

Let $R_{c2} = 4.7 \mathrm{k}\Omega$ $\underline{f_{z2} = 519 Hz}$: $C_{c1} = \frac{1}{2\pi f_{z2} R_{c2}} = 0.065 \mu \mathrm{F}$; $C_{c1} = 0.068 \mu \mathrm{F}$ is chosen $\underline{f_{p2} = 12500 Hz}$: $R_{c1} = \frac{R_{c2}}{(2\pi f_{p2} R_{c2} C_{c1} - 1)} = 194\Omega$; $R_{c1} = 220\Omega$ is chosen <u>Gain at 519Hz</u>: $R_{c3} = 1.2(R_{c1} + R_{c2}) = 5.9 \mathrm{k}\Omega$; $R_{c3} = 6.2 \mathrm{k}\Omega$ is chosen



Figure 6.2: Bode plots of the first design attempt (left-hand side) and second design attempt (right-hand side)

$$f_{z1} = 519 Hz$$
: $C_{c2} = \frac{1}{2\pi f_{zerr}R_{c3}} = 0.049 \mu F$; $C_{c2} = 0.047 \mu F$ is chosen

The transient response due to a 2.75A step-load change given by this preliminarily designed compensation circuit is simulated by HSPICE and shown in figure 6.3 (labelled 1st design). It can be seen that a rather slow transient response (settling



Figure 6.3: Transient responses to a 2.75A step-load change associated with the first and second design compensation circuits

time $\approx 2.7 \text{ms}$ and maximum voltage deviation $\approx 1.3 \text{V}$) is obtained, which does not meet the target specifications. The sizable voltage drop and sluggish settling time are caused by a low loop gain and low bandwidth. These must be further increased in the next design attempt, in order to achieve a better response.

6.1.1.5 Error amplifier compensation: second design attempt

The overall system loop-gain and bandwidth can be increased by increasing the error amplifier gain. However, in doing so, due care must be taken to prevent the resulting loop-gain bandwidth or phase lag at the crossover frequency becoming excessive; otherwise this will result in a highly oscillatory response such as that shown in figure 6.4, possibly leading to instability. Typically, the maximum cross-over frequency is limited to one third of the switching frequency, and the system phase shift from DC up to the crossover frequency must be maintained well above 180° (in addition to a 180° phase shift due to negative feedback) [111].



Figure 6.4: A very oscillatory transient response of a system with high loop gain

In the second design attempt using the frequency response technique, the error amplifier gain is increased by placing f_{p2} of the error amplifier at exactly five times above f_o , while retaining the same values of f_c , f_{z1} , and f_{z2} as those used in the previous design attempt. This redesign process is illustrated by the Bode plot on the right hand side of figure 6.2 with the following results obtained: $R_{c2} = 4.7 \mathrm{k}\Omega$, $C_{c1} = 0.068 \mu \mathrm{F}$, $R_{c1} = 470 \Omega$, $R_{c3} = 15 \mathrm{k}\Omega$, and $C_{c2} = 0.022 \mu \mathrm{F}$.

Compared with figure 6.2(b) on the left-hand side, the second design attempt results in an error amplifier with a higher gain, which raises the system loop gain and bandwidth (figure 6.2(c) on the right-hand side). The transient response to the 2.75A step load change given by these new component values is also shown in figure 6.3 (labelled 2nd design) for comparison. The response is improved as expected, but again the desired response has not yet been achieved and further trial-and-error tuning is needed, to attain satisfactory performance.

The preceding design process clearly demonstrates the pitfalls of the frequency response technique, particularly in the fine-tuning process where re-design of the compensation circuit is carried out on a trial-and-error basis. The main obstacle stems from the fact that there is no quantitative, but only a descriptive relationship between the required time-domain performance and the open-loop gain frequency characteristic.

6.1.2 Compensation circuit design using HSPICE optimisation

In this section, the application of optimisation to fine-tune the compensation circuit component values to achieve the desired specifications is illustrated. The circuit netlist of the averaged model in figure 4.11 (with the voltage source V_{inj} set to zero) is employed in the optimisation. In addition to the circuit description, information concerning optimisation must also be specified as follows.

6.1.2.1 Design objectives

In each iteration of optimisation, the simulation is started at 0s and ended at 3ms, and a 2.75A step load change is assumed to occur at the timepoint $100\mu s$.

The first design objective, a transient response with a settling time of 1ms (or less), is stated by the .MEASURE statement below:

.MEASURE tran tsetting trig at=100us targ V(4) val=14.925 RISE=1 goal=1ms

The second design objective, a steady state regulation of \pm 0.5% of nominal output voltage, is ensured by the following .MEASURE statements:

.MEASURE tran overshoot max v(4) from=100us to=3ms goal=15 .MEASURE tran min-limit min v(4) from=2ms to=3ms goal=14.925

The first .MEASURE statement dictates the output voltage (v(4)) should never be more than 15V after the instant of the load change $(100\mu s)$. The second .MEASURE statement ensures that after 2ms, the output voltage remains above the regulation limit (14.925V). These two statements together not only ensure that the regulation limits are secure, but also that the response has no voltage overshoot.

6.1.2.2 Design variable

The error amplifier gain can be tuned by just varying R_{c3} and C_{c2} , while keeping the rest of the components constant. Unless the specifications are very stringent, it is unnecessary to select all five compensation circuit components as design variables, and having too many design variables makes the optimisation more difficult and may cause convergence problems.

In the netlist, R_{c3} and C_{c2} are defined as follows, with the results from the second design attempt assigned as the initial guess:

.PARAM rx=optval(15k,10,100k) .PARAM cx=optval(0.022u,0.001u,0.2u)

6.1.2.3 Optimisation strategy configuration

The optimisation strategy given below has been configured to give a convergent result:

.MODEL opt1 opt relout=1e-3 relin=1e-3 itropt=30

relout=1e-3 and relin=1e-3 specify convergence of the solution is declared when either all of the optimising input parameters, or output results, vary by no more than 0.1% (1e-3) from one iteration to the next. itropt = 30 limits the maximum number of iterations to 30.

The complete HSPICE netlist for this design is given in appendix B1.

6.1.3 Results

HSPICE is run on a SUN SPARC4 workstation. After a few iterations of simulation and optimisation, the optimised solution is found with the results listed in column 2 of Table 6.1. Note that the optimised R_{c3} and C_{c2} in Table 6.1 are calculated from the optimised w_{z2} found by HSPICE, through $w_{z2} = \frac{1}{R_{c3}C_{c2}}$. It

Initial design values	Optimised values
$R_{c1} = 470\Omega$	$R_{c1} = 470\Omega$
$R_{c2} = 4.7 \mathrm{k}\Omega$	$R_{c2} = 4.7 \mathrm{k}\Omega$
$R_{c3} = 15 \mathrm{k}\Omega$	$R_{c3} = \underline{27} \mathrm{k}\Omega$
$C_{c1} = 0.068 \mu F$	$C_{c1} = 0.068 \mu F$
$C_{c2} = 0.022 \mu F$	$C_{c2} = \underline{0.01}\mu\mathrm{F}$

Table 6.1: HSPICE optimisation results

can be seen that the optimiser has met the design objectives by increasing R_{c3} and decreasing C_{c2} , thus increasing the error amplifier gain and subsequently the loop-gain and bandwidth. The improved performances in both time- and frequency-domain after optimisation compared with those before optimisation are illustrated in figure 6.5. Figure 6.5(a) shows the increase in system loop gain and bandwidth, while the phase shift at the crossover frequency is maintained in the vicinity of 90° (in addition to the 180° phase shift due to negative feedback) indicating a wide stability margin. As seen in figure 6.5(b), the improvement in transient response has been considerable and the design specifications have been satisfied. The optimised transient response to the 2.75A step-load change obtained experimentally is shown in figure 6.9, along with the simulated result for comparison. Close agreement between the two results is seen, confirming the accuracy of the averaged model in SMPS modelling.

The time spent on the simulation/optimisation process normally depends on the circuit complexity, the rigour of the objectives, the numbers of optimising variables and the closeness of the initial guess to the final solution. To achieve the optimised results in the above design example, the associated run time is usually less than 20s. This fast design cycle is due mainly to the use of the averaged model, and also the use of only two design variables with good initial guesses.



Figure 6.5: Performance comparison before and after optimisation: (a) Openloop gain and phase (b) Transient responses to a 2.75A step-load change

6.1.4 Discussion

The optimised solution in column 2 of Table 6.1 is just one set of non-inferior solutions that satisfies the design objectives. It is likely that there will be many other sets of non-inferior solutions which also satisfy these objectives, some of which may yield better transient responses (e.g. faster settling time with smaller overshoot) than that in figure 6.5. Such responses are illustrated in figure 6.6. The number of non-inferior solutions is strongly dependent on how closely the



Figure 6.6: Transient responses to the 2.75A step-load change of when (a) $R_{c3}=25k\Omega$ and $C_{c2}=8nF$ (b) $R_{c3}=16.4k\Omega$ and $C_{c2}=9.1nF$

design objectives are specified; more stringent specifications would result in fewer

non-inferior solutions and vice versa.

In using time-domain optimisation to design the compensation circuit, care must be taken to maintain system stability under all possible operating conditions [102]. In this design example, the possibility of picking parameters that lead to system instability has been prevented by the two .MEASURE statements specifying the steady state requirement.

For off-line power supply applications where an input voltage to a converter contains ripple at twice line frequency (e.g. the 100Hz ripple for the 50Hz line input) as a result of rectification, design of the error amplifier compensation circuit must result in high loop-gain at the ripple frequency to minimise its effect propagating to the converter's output [111] - a loop gain of 35dB is typically required at this frequency. With the proposed HSPICE optimisation, design in the time-domain and frequency-domain cannot be performed at the same time. Design to meet loop gain requirements at the ripple frequency, however, can be done at the initial design stage (before fine-tuning with HSPICE optimisation); for example, by placing the zero f_{z1} in figure 6.1 at the location that gives the desired loop-gain at the ripple frequency.

With HSPICE optimisation, it is possible that the convergence criteria (relin and relout) are met, causing the optimisation process to stop before the design objectives have been satisfied. This has been observed when poor initial guess values are used. From the author's experience, initial results from classical design methods provide an adequate initial guess for optimisation to occur within the pre-specified maximum number of iterations, normally set to 20-40 as recommended in [70]. If the solution has not converged within 40 iterations, it is unlikely to do so. Non-convergence is usually caused by either unrealistic design objectives or poor initial guesses.

6.2 Voltage Injection Control (VIC)

In this section, results obtained from the investigation of Voltage Injection Control are presented. Simulated and experimental results given by the prototype converter without VIC (standard voltage-mode control) are first presented, followed by those obtained with VIC.

6.2.1 Transient responses without VIC

Depicted in figures 6.7 to 6.10 are simulated and experimental transient responses to various step-load changes using standard voltage-mode control (without VIC). The experimental results are obtained by switching on a particular load in the programmable load block. The measurement is taken by the computer oscilloscope HS508 operating in storage mode and the resulting waveforms are plotted using Gnuplot [118]. Simulation is performed by HSPICE using the averaged model in figure 4.11, with V_{inj} assigned to zero. To achieve realistic results, all circuit parameters used in the simulation are measured values.

The transient performances of the results in figures 6.7 to 6.10 expressed in terms of settling time and maximum voltage drop are summarised in Table 6.2, where the values given in the parenthesis are the simulated results. The close agreement between the simulated and experimental results can be seen. It is worth noting that in Table 6.2, the settling time for the 2.75A step-load change is 1.1ms, slightly longer than the predicted value of 1ms. This is due mainly to variation of circuit components from their nominal values. In compensation circuit design, the nominal component values were assumed.

Load Change Condition	Settling time (ms)	Voltage drop (V)
1.50A step load	0.90 (1.00)	0.38~(0.37)
2.25A step load	1.05(1.14)	0.59~(0.56)
2.75A step load	1.10 (1.20)	0.74(0.67)
3.50A step load	1.20(1.28)	0.92~(0.85)

Table 6.2: Transient performance associated with figures 6.7 to 6.10

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Figure 6.7: Transient responses to a 1.5A step-load change (a) simulated (b) experimental



Figure 6.8: Transient responses to a 2.25A step-load change (a) simulated (b) experimental



Figure 6.9: Transient responses to a 2.75A step-load change (a) simulated (b) experimental



Figure 6.10: Transient responses to a 3.5A step-load change (a) simulated (b) experimental

6.2.2 HSPICE optimisation of V_{inj}

In each iteration of the optimisation, the simulation is started at 0 and ended at 2ms, and a step load change is assumed to occur at $100\mu s$.

6.2.2.1 Design objectives

The design objectives in Table 5.1 can be translated into multiple inequality constraints of the form:

$V_{overshoot}(amplitude, t_{inj})$	\leq	0.075 volt	Equation:	(6.2)
$V_{spike}(amplitude, t_{inj})$	\leq	0.075 volt	Equation:	(6.3)
$t_{settling}(amplitude, t_{inj})$	\leq	$250 \mathrm{x} 10^{-6}$ second	Equation:	(6.4)

In the above equations, the individual objective is written as a function of two design variables, and all of them must be simultaneously satisfied in the optimisation. These objective functions are respectively coded in the HSPICE netlist as follows:

.MEASURE tran t_setting trig at=100us targ v(4) val=14.925 RISE=1 goal=0.25ms

.MEASURE tran v_max1 max v(4) from=101us to=2ms .MEASURE tran overshoot param='v_max1-15' goal=0.075

.MEASURE tran v_max2 max v(4) from='tinj' to=100us .MEASURE tran spike param='v_max2-15' goal=0.075

The first .MEASURE statement specifies that a settling time of $250\mu s$ (or less) is sought in the optimisation. The settling time measurement is started at the timepoint $100\mu s$ (the instant of load application) and ended when the output voltage comes back to the lower regulated limit (14.925V) for the first time.

The second and third .MEASURE statements together implement the voltage

overshoot objective (equation (6.3)). In the second .MEASURE statement, the maximum voltage immediately after the load change $(t=101\mu s)$ to the end of the simulation (t=2ms) is measured and stored in a dummy variable **v_max1**. The third .MEASURE statement then defines the voltage overshoot as the difference between **v_max1** and the nominal voltage (15V) in which the value of 0.075V is sought. Similarly, the spike voltage requirement in equation (6.4) is stated by the fourth and fifth .MEASURE statements, with **v_max2** the dummy variable in this case.

6.2.2.2 Design variables

The two discrete optimising variables described in equations (5.5) and (5.6) are defined by the following .PARAM statements:

.PARAM tinj = optval(90us,100us,40us,10us) .PARAM amplitude = optval(0.039,0,0.39,19.5e-3)

The first .PARAM statement defines the injection time variable (tinj) with the initial guess value, lower and upper limits of 1, 0 and 6 cycles in advance respectively, given with respect to the instant of load change at $t=100\mu s$ (the switching period is $10\mu s$). The last number in the statement (10us) sets the incremental step to $10\mu s$, reflecting the constraint in equation (5.6).

The magnitude of V_{inj} (amplitude) is defined by the second .PARAM statement in a similar manner. In this case, the step size is set to 19.5mV and the initial guess value is set to 39mV (2x19.5mV). This initial guess value is used in the optimisation of V_{inj} for every step-load change.

6.2.2.3 Optimisation strategy

An example of control options used in optimising V_{inj} for a 2.75A step load condition is given below:

.MODEL opt1 opt relin=1e-4 relout=1e-4 itropt=30 close=10

These are very similar to those used in the previous control loop design, except that the convergence criteria (relin, relout) are more rigid and a new option CLOSE is introduced. CLOSE is an indication of how close the initial guess is to the final solution; a large value of CLOSE causes the optimiser to take large steps toward the solution, otherwise small steps are used. It is chosen on a trial-and-error basis and is different for each step-load condition.

6.2.3 Results

The optimisation of V_{inj} is carried out for the same four step-load conditions as those in figures 6.7-6.10. HSPICE optimisation is run on a SUN SPARC4 workstation, with the optimised results shown in Table 6.3. The netlists that produced these results are listed in Appendix B2. In all cases, it takes less than 15 iterations for the optimisation to converge (less than 10 seconds to run).

Step-load	Solution by HSPICE
1.50A	0.1775u(t-2cycles)
2.25A	0.2145u(t-2cycles)
2.75A	0.2925u(t-2cycles)
3.50A	0.3705u(t-1cycle)

Table 6.3: Optimised V_{inj} found by the HSPICE optimiser

Each solution in Table 6.3 represents just one possible solution for that step-load condition. A complete set of non-inferior solutions for each step-load change is symbolised by a circle shown in the charts in figures 6.11-6.14. These optimised solutions all result in transient responses that satisfy the desired performance described by the inequality (6.2) to (6.4). The cross symbol in each chart indicates the violated solutions, with those which yields similar category of violation being shaded with the same intensity. It should be noted here again that the maximum voltage deviation is not considered in this optimisation, as it is not a critical criterion in radar applications.



Figure 6.11: V_{inj} solution chart for a 1.5A step-load change

Step-load = 2.25A



Figure 6.12: V_{inj} solution chart for a 2.25A step-load change

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Figure 6.13: V_{inj} solution chart for a 2.75A step-load change

Step-load = 3.5A



Figure 6.14: V_{inj} solution chart for a 3.5A step-load change

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Experimental and simulated transient responses given by the V_{inj} solutions selected for each load condition are shown in figures 6.16-6.21. Compared with the results from standard control (figures 6.7-6.10), the transient responses have been significantly improved. In all cases, the experimental results are highly consistent with their simulated counterparts. This indicates that the proposed optimisation procedure is an accurate and effective tool for selecting an appropriate value of V_{inj} .

From figures 6.11 to 6.14, the following observations are drawn:

- 1. For the 1.5A and 2.25A load changes, the optimised V_{inj} solutions represented by black circles indicate the results that yield no transient response, i.e. a response that remains within regulation limits. Examples of such responses are illustrated in figures 6.16 and 6.17. This demonstrates the robustness of VIC for low step-load changes.
- 2. In each chart, the area on a left-hand side of the optimised solutions is denoted the under-compensated region, where the magnitude of V_{inj} is not adequate to give satisfactory settling time. An attempt to increase the injecting time leads to the violation of the spike voltage. On the other hands, the area on a right-hand side of the chart is considered as the overcompensated region, where the magnitude of V_{inj} is high resulting in an excessive voltage overshoot, with an attempt to increase the injecting time leading to the breach of the spike voltage specification.
- 3. The required magnitude of V_{inj} increases as the magnitude of load change becomes larger. At low step-load changes (1.5A and 2.25A), the low V_{inj} magnitudes cause a slower output voltage rise, and therefore a longer injection time (more numbers of cycles in advance) is possible without the spike voltage specification being violated. For example, at the 1.5A step-load change, an injecting time up to 5 cycles is permitted, whereas the maximum injecting time for the 2.75A and 3.5A step-load change is limited only to 2 cycles. Additionally, for high step-load change an attempt to increase the magnitude a step further (e.g. from 292.5mV to 312mV in the 2.75A load condition, or from 370.5mV to 390mV in the 3.5A load

condition) would result in a response with an excessive voltage overshoot. For these reasons, there are more solutions for low step-load changes.

4. The magnitudes of optimised V_{inj} at every step-load change are very close to the difference between the steady state error voltage, ΔV_e before and after load application, obtained from standard control (figure 6.15). The values of ΔV_e for each step-load change are given in Table 6.4. This suggests that



Figure 6.15: The excursion of the error voltage V_e in standard voltage-mode control (no V_{inj}) after a step load applied to the converter

Step-load change	$\Delta V_e(V)$
1.5A	0.149
2.25A	0.231
2.75A	0.277
3.5A	0.355

Table 6.4: ΔV_e for each step-load change

 V_{inj} optimisation can be reduced just to the selection of an appropriate injection time which can be easily found on a trial-and-error basis, without accessing the optimisation tool.

For any step-load condition, the imposed design objectives and the resolution of the magnitude of V_{inj} play an important role in determining the size of a noninferior solution set; relaxed objectives and fine V_{inj} resolution will give more non-inferior solutions and vice versa. During the course of the V_{inj} optimisation, convergence problems similar to those mentioned in section 6.1.4 were also encountered. These are further discussed in chapter 7.

The design trade-offs for the 2.75A step-load change are illustrated in figure 6.22 which depicts the plots of the non-inferior solutions of V_{inj} against the three design objectives. To facilitate the plots, the resolution of V_{inj} has been scaled down five times from its original value i.e. from 19.5mV to 3.9mV allowing more solutions to be obtained, and only those solutions with a constant injection time of 2 cycles are used in constructing these plots. From figure 6.22, it can be seen that as the amplitude of V_{inj} increases, the settling time decreases, but at the expense of larger voltage overshoot and spike voltage. The voltage overshoot increases more rapidly than the spike voltage and is the first objective to be violated. It is therefore identified as the main obstacle to any further transient response improvement.



Figure 6.16: Optimised transient responses to a 1.5A step-load change with V_{inj} of 156mV, 2 switching cycles in advance of the load application (a) simulated (b) experimental



gure 6.17: Optimised transient responses to a 2.25A step-load change with V_{inj} of 234mV, 3 switching cycles in advance of the load application (a) simulated (b) experimental


Figure 6.18: Optimised transient responses to a 2.75A step-load change with V_{inj} of 273mV, 2 switching cycles in advance of the load application (a) simulated (b) experimental



Figure 6.19: Optimised transient responses to a 3.5A step-load change with V_{inj} of 351mV, 2 switching cycles in advance of the load application (a) simulated (b) experimental



ure 6.20: Optimised transient responses to a 2.75A step-load change with V_{inj} of 273mV, 1 switching cycles in advance of the load application (a) simulated (b) experimental



Figure 6.21: Optimised transient responses to a 3.5A step-load change with V_{inj} of 351mV, 1 switching cycles in advance of the load application (a) simulated (b) experimental



Figure 6.22: V_{inj} design trade-off for a 2.75A step-load condition with a constant injecting time of 2 switching cycles in advance

6.2.4 Response discrepancy associated with the injecting time

This section examines in detail the transient response discrepancy mentioned in section 2.2.2. This investigation is carried out using simulation, as the user has full control over the relative timing between the instant of load change and voltage injection, while this is very difficult to do experimentally due to the lack of synchronisation between the computer and the prototype converter's switching frequency.

Figure 6.23 shows the relative position between voltage injection and load application, in the one-cycle in advance case, of the optimistic scenario (figure 6.23(a)) and the worse case one (figure 6.23(b)).



Figure 6.23: Timing diagram demonstrating (a) optimistic scenario (b) worse scenario in VIC

In the optimistic case, voltage injection at the end of the ON period instantly opens up the pulse width of the converter making the output voltage rise. It continues to rise for a switching cycle before the load application. On the other hand, in the worst case, voltage injection at the very beginning of the OFF period does not make the output voltage rise until the end of the following ON period. The output voltage has very little time to rise as the load application occurs immediately after this ON period is ended. (After sudden load application, the error signal as well as the control voltage V_c will rise in a step manner in response to a sudden voltage drop (see figure 2.5). Here, for convenience it is assumed in figures 6.23(a) and 6.23(b) that the control voltage V_c does not change.)

The simulated extreme scenarios in the 2.75A step-load change using an injected voltage of 0.273u(t-1cycle) are shown in figure 6.24(a) and 6.24(b) respectively. Note that in simulation of the worst case scenario, the instant of voltage injection was carefully chosen not to cause double pulses within a switching period. In a practical circuit, this is prevented by the double pulse suppression logic in the control IC chip.



Figure 6.24: Transient responses to a 2.75A step-load change, with $V_{inj} = 0.273u(t - 1cycle)$ (a) Optimistic case (b) Worst case

Comparing figures 6.24(a) and 6.24(b), the difference in maximum voltage drop is less than 0.3% of nominal output voltage, while the discrepancy in voltage overshoot and spike voltage are both less than 0.15%. Similar figures result for the increased numbers of cycles of advanced injection. These figures are the approximate performance tolerances of the experimental results in figures 6.16(b) to 6.21(b). Despite being relatively small, it must be ensured that the selected solution for V_{inj} still results in a satisfactory transient performance, after these tolerances have been considered.

The above transient response discrepancy is due to the fact that load application is allowed to take place anywhere in a switching cycle. It can be eliminated if the occurrence of load connection is always fixed at a particular point in the switching cycle. To realise this control scheme, load switching would need to be synchronised to the converter's switching frequency.

6.2.5 VIC experiment with current-mode control

Experimental results associated with the prototype current-mode controlled converter with and without VIC are illustrated in figure 6.25. The magnitude of the step-load change in both cases is 3A (75% of a maximum step-load current). In figure 6.25(a), without VIC the voltage drop is approximately 0.35V and the settling time is about 700 μ sec (assuming $\pm 2\%$ regulation limit). By injecting the V_{inj} of 136mV, 2 cycles in advance of the load application, the transient response shown in figure 6.25(b) is obtained, which is just within the regulation limit, showing considerable improvement. This clearly demonstrates the capability of VIC in a system employing current-mode control. For the design to achieve a target transient performance, an optimisation procedure for V_{inj} similar to that used in the voltage-mode control case can be applied using the current-mode converter model developed in section 4.4.3.

It is worth noting that the main voltage loop of the prototype current-mode controlled converter has not been optimised. One would expect to achieve a better transient response than that in figure 6.25(a) if the compensation circuit component values were well selected. To arrive at optimised values of these circuit components, the HSPICE optimisation procedure demonstrated in section 6.1.2 could be used. Noise seen in the waveforms at turn ON and OFF could have arisen from inadequate PCB layout and wiring.

In this project, the investigation of the VIC technique was mainly carried out for a converter employing voltage-mode control because of the simplicity of this control method, as well as the ease of its implementation. With voltage-mode control, no additional current feedback loop, which is very sensitive to noise pick up, and no stabilising ramp to avert problems associated with sub-harmonic oscillation and system instability beyond the duty ratio of 0.5 are required, thus reducing circuit complexity, design time, and time spent on troubleshooting. While the maximum magnitude of V_{inj} in the voltage-mode control case is limited to the value at which the minimum error signal (V_{emin}) differs from the peak of the sawtooth signal, in the current-mode control case, this value is restricted by a preset current limit value.

The VIC current-mode controlled prototype was designed and built with the intention to confirm experimentally the operation of the VIC technique in this control method (which is more popular in SMPS).



Figure 6.25: (a) Transient response to a 3A step-load change of the currentmode controlled prototype (a) without VIC (b) with V_{inj} of 136.5mV, 2 cycles in advance of the load application

Chapter 7

Discussion

The preceding chapters describe the technique, design and implementation of voltage injection control. In this chapter, the broader aspects of these issues and the outcomes of the VIC investigation are discussed. Simulation and modelling have played an important role in this work in both the design of V_{inj} and error amplifier compensation circuit. Issues concerning the justification in using the averaged model and the validation of its results are examined.

Also discussed are the prospects of the VIC technique in future phased array radar systems, as well as in other general applications.

7.1 VIC Technique - General Consideration

As described in Chapter 2 (figure 2.1), VIC is an open-loop technique which employs prior information of load to initiate appropriate advance compensation in an attempt to minimise the anticipated effect of the load disturbance. The implementation of VIC is therefore suitable for power supplies in systems where the load switching pattern is known in advance, and where there is a central system controller (processor) available to provide such information, for example in radar systems or maybe in the computer power management systems discussed in section 7.6.

To realise the VIC control scheme, the power supply control circuit (figure 2.2) includes an extra summing circuit to allow an injected voltage (V_{inj}) to be added

to the error signal (V_e) , enabling the pulse width of the converter to increase. It is preferable that the gain of the summing circuit is unity to prevent alteration of the control loop characteristics determined during the control loop design. Unity gain ensures that implementation of VIC does not affect control loop design.

In VIC, V_{inj} is a control parameter to be determined and is a function of three variables: amplitude, injecting time and shape. In this work, a linearly increased V_{inj} and a step V_{inj} were considered (section 2.2.3). It is found that these two shapes produce similar results, i.e. the linearly increased V_{inj} is replaceable by its step counterpart with a lower V_{inj} magnitude. The step V_{inj} is chosen as it is easy to generate and control, reducing V_{inj} to a step function of amplitude and injecting time as described by equation (2.4). The effect of amplitude and injecting time on the resulting transient response is described in section 2.2. To achieve the desired transient performance to load changes, V_{inj} must be optimised: in this project this was carried out by HSPICE optimiser. The discussion on optimisation of V_{inj} is given in section 7.2.2.

The primary aim of this research is to test the feasibility and capability of the VIC technique, with the outcomes discussed as follows.

7.1.1 Capability of VIC

As illustrated in figures 6.16 to 6.21, VIC results in significant improvement in transient response to load changes, such that stringent transient specifications can be met. The robustness of the technique is clearly demonstrated in the cases of 1.5A and 2.25A step-load changes (figures 6.16 and 6.17), where VIC results in the responses bounded within the steady state regulation limits. Substantial improvement is also obtained for higher step-load conditions; for the 3.5A step-load case, comparing figures 6.10 to 6.19 the maximum voltage deviation reduces from 0.95V to 0.15V, while an improvement in the settling time is approximately ten fold. A similar degree of achievement is also obtained in the system employing current-mode control (figure 6.25).

Due to advance voltage injection, VIC introduces a spike voltage to the resulting

response, which is undesirable in any application if it is too high. Results in figures 6.11-6.14 show that with injecting times of zero to two cycles in advance the spike voltage is acceptable for every tested step-load change. However, a value of up to five cycles in advance is possible in the case of a 1.5A step load, with the spike voltage still acceptable. This is due to the fact that the low magnitudes of V_{inj} associated with this load condition cause a slower output voltage rise. The output voltage rate of rise is also dictated by values of the filter inductor and capacitor.

7.1.2 Limitations of VIC

Despite being able to give a good transient response, the usefulness of VIC to broader applications is limited by the following considerations:

- Advance knowledge of a forthcoming load is a basic requirement for the implementation of VIC in any system. This limits the appeal of VIC to just certain applications.
- The requirements of a summing circuit and possibly a D/A converter add an extra cost to the power supply.
- It is only suitable for single-output power supplies, such as localised DC/DC converter supplying a group of sensitive loads in a distributed power system (see figure 7.4 for example). The distributed power system is described later in section 7.5. If VIC was used in multiple output power supplies, an attempt to compensate for a load disturbance in one output would result in a voltage rise on the remaining outputs which is undesirable.

7.2 Time Domain Optimisation With HSPICE

In this work, optimisation has been used to design the error amplifier compensation circuit and to select a suitable V_{inj} . In both cases, optimisation is performed by HSPICE in the time-domain. This is very relevant because the transient specifications are all time-domain parameters. Nevertheless, the frequency-domain design method is not totally ignored in this work; it was used to initially design the compensation circuit to result in a stable converter. The compensation circuit component values obtained from this initial design were used as the initial guess values for the error amplifier compensation circuit optimisation.

The HSPICE optimisation is an iterative process embracing simulation and optimisation. In each iteration run, the averaged circuit model is simulated and measurements taken from the simulated result. If the desired performance is not met, design variables are adjusted and the same process repeated for the next iteration, until either the solution is declared convergent or no solution is found after a prescribed maximum number of iterations. This iterative environment is shown by the flow chart in figure 5.4.

In this section, the use of HSPICE optimisation in these two applications is evaluated. Then, convergence problems associated with HSPICE optimisation are discussed and an effective remedy suggested. Finally, VIC converter design consideration is reviewed.

7.2.1 Optimisation of the error amplifier compensation circuit

Traditionally, design of the error amplifier compensation circuit is carried out in the frequency domain, using classical design tools such as the Bode plot method or the root locus method. These conventional tools are limited and inefficient mainly because of the lack of a quantitative relation between transient specifications which are time-domain parameters and design parameters in the frequency domain, hence making the fine-tuning tedious and difficult (other limitations were previously outlined in section 5.4.1.4).

With HSPICE optimisation, this problem is overcome as the fine-tuning is automatically performed by the optimiser in each iteration run, offering a more efficient means to design error amplifier compensation circuits and reducing significantly the design time. Moreover, unlike the frequency-domain design methods which rely on small-signal assumptions, the proposed HSPICE optimisation uses a large-signal averaged model of the converter with the effect of circuit parasitics included in the simulation, therefore producing very accurate results as can be seen by comparing simulated results to their experimental counterparts in figures 6.7 to 6.10.

Although HSPICE can optimise circuit performance simultaneously in both timeand frequency-domain, the proposed design technique only allows optimisation to be carried out for one particular domain at a time. This limitation arises from the averaged model employed in the simulation not being able to give meaningful results in both domains at the same time. To simulate converter performance in the frequency domain (AC analysis) using the averaged model, the AC stimulus together with a coupling L-C circuit must be inserted between the output of the sub-circuit VICVM and the input of the sub-circuit PWMBCK as shown in figure 4.11

An application for HSPICE optimisation may be in the control loop design of a power supply for high performance microprocessors such as Intel's Pentium Pro (P6). The new generation of microprocessors operate with a low power supply voltage in the range of 3.1V, and are "current thirsty" devices due to the large number of transistors in the circuit (over 5 million are used). The power management feature incorporated within these chips to resolve heat dissipation problems causes sections of circuitry inside the chip to come on and off line, imposing large load transients on the power supply. In the worst case, current requirements can slew from minimum (less than 1A) to full load ($\approx 10A$) within 360ns [119]. This severe load transient, coupled with the requirement for tight voltage regulation of $\pm 5\%$ for reliable operation, makes the design of power supplies for this application very challenging. Presently, the design problem is tackled by the careful selection of a low ESR output capacitor to limit the initial transient voltage deviation, and the use of a well-compensated control circuit (voltage-mode control or more normally current-mode control) to regulate the subsequent transient voltage excursion. HSPICE optimisation can readily be adopted to assist the designer in selecting compensation circuit component values to achieve the desired load transient performance.

7.2.2 Optimisation of V_{inj}

 V_{inj} is chosen to ensure that the resulting transient response meets the design specifications. These specifications are given in terms of the desired settling time, voltage overshoot, and spike voltage, all of which must be satisfied simultaneously. In applications other than for radar systems, maximum voltage deviation could be added to the above list.

If the appropriate value for V_{inj} is to be calculated analytically, equations (4.16), (4.17), and (4.23) must be manipulated to result in a single equation which expresses an output voltage as a time-varying function of step-load change and injected voltage, with the power circuit and feedback compensation parameters as constant. A great deal of effort is usually spent before such an equation is reached, and the equation itself would be very complex. Given a value of stepload change and injected voltage, the output voltage can be solved as a function of time. A "trial-and-error" approach to obtain the optimum V_{inj} becomes tedious and impractical, particularly when fine V_{inj} resolution is required or when stringent design objectives are sought.

Hence, a more effective and systematic design methodology must be established, with a CAD approach being preferable. HSPICE optimisation is thus proposed to fulfil these objectives. With HSPICE optimisation, equations describing converter behaviour are automatically formulated from an input circuit netlist. The optimisation problem then becomes the minimisation of the function that describes the error between the desired value and the measured value, instead of the minimisation of objective functions $F_i(x)$ (see equation (4.3)) described by the complex time-varying functions.

It is shown in table 6.3 that the use of HSPICE optimisation to design V_{inj} to meet the desired transient performance has been successful. From the charts in figures 6.11 to 6.14, there are more optimised V_{inj} solutions for the lower step-load conditions, i.e. for the 1.5A and 2.25A step-load changes than for higher steploads. This is due to the fact that the lower magnitudes of V_{inj} associated with these step-load conditions make the output voltage rise slower, therefore allowing longer injecting time without the spike voltage specification being violated, and is also due to the lower transient (i.e. the smaller voltage drop and the faster settling time) expected with a lower step load.

For each step-load change, the number of non-inferior solutions is influenced by the resolution of V_{inj} magnitude and the design objectives. A more refined V_{inj} magnitude resolution will give a larger set of non-inferior solutions, while stringent objectives will result in a reduced set of solutions. Despite being an independent variable, the injection time tends to play a less important role than the V_{inj} magnitude, in that it can be determined after obtaining the optimised V_{inj} magnitude. The magnitudes of optimised V_{inj} at every step load can be approximated by the steady state error voltage, ΔV_e before and after load application, obtained from standard control (without V_{inj}), as shown in figure 6.15 and table 6.4. Though the injection time can be any integer number of cycles, it is very unlikely that values above ten will be used as the resulting spike voltage would become too excessive for most applications.

In this project, the settling time, voltage overshoot and spike voltage were the three main targets considered in the optimisation. The maximum voltage deviation was omitted as it is not normally a crucial parameter for power supplies in radar applications. Though disregarded in the optimisation, the results in figures 6.16 to 6.21 show that the maximum voltage drop is maintained at acceptable levels for all step-load changes (for a 3.5A load change in figure 6.21, the maximum voltage drop is approximately 0.25V).

In other applications, the settling time may not be considered to be as important a parameter as the maximum voltage drop. For instance, in computer power supplies, the output voltage must be maintained within the prescribed regulation limits throughout the operating range [119], to prevent malfunction of some IC chips in the system.

7.2.3 Convergence problems and remedies

As mentioned before, one condition which will terminate the HSPICE optimisation process is when convergence is declared, i.e. when either the optimising variables or the results vary by no more than the values respectively specified by RELIN and RELOUT from one iteration to the next. It is possible that the optimiser establishes a search direction which causes the convergent conditions to be met, while some design objectives still have not yet achieved (i.e. some design objectives are under-attained), resulting in the optimisation process being prematurely terminated. This problem is prone to occur particularly when stringent design objectives are sought, more design objectives are stated, or when optimising parameters are assigned poor initial values.

The non-convergence of the optimisation (i.e. no solution found after the maximum number of iterations) is another problem that is likely to occur if poor initial guesses are being used or unrealistic objectives being sought. It is usually hard to determine whether the specified design objectives are realistic, as this requires experience with the system under consideration. Nevertheless, this question may be qualitatively answered by using knowledge gained from the achievable objectives. For instance, from Table 7.1 which lists the transient performance associated with each V_{inj} solutions for the 2.75A step-load change, one learns that a settling time of less than 100μ s is not an achievable objective, unless the allowed values of either voltage overshoot or spike voltage are increased (assuming the resolution of V_{inj} remains unchanged).

In solving these convergence problems, an option CLOSE can be used by the optimiser to estimate how close the initial guesses are to the final solution. Other control options such as RELIN and RELOUT and CUT^1 also influence the convergence, but their effects are not obvious. Changing the CLOSE value effectively establishes the new search direction, through which convergence may result. The CLOSE value used in the V_{inj} optimisation for each step-load change was chosen

 $^{^{1}}$ CUT acts as a scaling factor of the CLOSE value. If the last iteration was a successful descent toward the solution, CLOSE is decreased by CUT; otherwise CLOSE is increased by CUT squared.

Vinj	Settling time (μs)	Overshoot (V)	Spike (V)
0.2535u(t-1cycle)	247	0	0.015
0.2535u(t-2cycles)	242	0	0.042
0.2535u(t-3cycles)	239	0	0.074
0.2730u(t-0cycle)	195	0.034	0
0.2730u(t-1cycle)	179	0.023	0.016
0.2730u(t-2cycles)	155	0.013	0.046
0.2925u(t-0cycle)	158	0.069	0
0.2925u(t-1cvcle)	136	0.058	0.018
0.2925u(t-2cycles)	100	0.046	0.05

Table 7.1: V_{inj} solutions and associated transient performance for 2.75A stepload change

on a trial-and-error basis. To achieve an optimised V_{inj} in this project, CLOSE values between 10-20 were found to be suitable.

7.2.4 Design Procedure

If the summing circuit has unity gain, the loop-gain characteristic and system stability of a converter with VIC are the same as that with standard control, and are determined at the control loop design stage. In this project, control loop design is begun by selecting the initial compensation circuit component values to ensure system stability using the Bode plot method. HSPICE optimisation is then employed to fine-tune the initial design results by adjusting the error amplifier gain, subsequently the system loop gain and its bandwidth, until the desired specifications are met. Initial results from the frequency-response method provide a sufficient initial guess for optimisation to occur within the maximum number of iterations. Rough initial guess values can also be used to simplify the design process, but poorly chosen values may result in the convergence problems discussed in section 7.2.3.

As described in section 6.1.1.5, adjustment of the error amplifier gain (varying r_{c3} and c_{c2} , while keeping the rest of the compensation circuit components constant) can lead to instability if it results in the system bandwidth, the loop-gain crossover frequency f_c , being increased excessively. Using frequency response methods to

design the error amplifier compensation circuit, the value of f_c is normally limited to maximum one third of the switching frequency (f_s) to prevent instability [111]. In the time-domain, there is normally no easy means to predict system stability. Simulation of system response is probably the most practical way to verify this. With HSPICE optimisation, the prospect of obtaining solutions (compensation circuit component values) which lead to system instability can be avoided by always including the objectives stating the regulation limits (section 6.1.2.1).

Since optimisation can only be performed under one set of operating conditions at a time (for example in this project it was performed under the 2.75A stepload change, with constant input voltage of 33V), system stability must also be examined under other possible operating conditions. An AC analysis may be required to check the crossover frequency and phase margin under various extreme conditions in the system (e.g. by performing loop-gain measurement or using the averaged model in figure 4.11). From the resulting Bode plots, stability is well established if the phase margin is greater than 45° and the cross-over frequency less than a third of f_s .

7.3 VIC Test Facilities

The prototype VIC test facility shown in figure 3.1 was designed to simulate the operating environment of radar power supplies. The transmission of a pulse signal at a specific PRF which draws a step average current from a power supply is emulated by the connection of load from the switched load bank (seven different loads are possible). The personal computer (PC) duplicates the radar processor functions controlling both load application and voltage injection following the algorithm shown in figure 3.2.

Instead of the PC, other type of controllers such as a microcontroller or DSP cards could also be used to perform the control functions. However, the PC is preferred in this project because of its availability and flexibility. An interfacing card based on the Intel 8255 chip is used to facilitate the communication between the PC and the outside world. This is preferred to the PC parallel port as it is much easier to control. The card operates with 8-bit data and, hence, this dictates that V_{inj} is stored using an 8-bit data format. For a greater V_{inj} resolution, a longer wordlength (e.g. 16-bit) can be used, and if this is the case, more sophisticated interfacing cards which operate with the 16-bit data format such as [120] should be considered.

In the prototype, the resolution of V_{inj} is 19.5mV, with a control range from 0 to 4.9725V which is considered unnecessarily large. In voltage-mode control, the maximum V_{inj} magnitude is determined from the minimum error voltage to the peak of the sawtooth signal (refer to figure 2.8). The resolution of V_{inj} can be



Figure 7.1: Inclusion of a resistor divider to increase V_{inj} resolution

increased, while decreasing the control range, by connecting a resistive divider at the output of the D/A converter as shown in figure 7.1. With this configuration, the new V_{inj} resolution is defined by $\frac{4.9725}{255} \left(\frac{R_1}{R_1+R_2}\right)$ V and the control range is now reduced to 0 to $4.9725 \left(\frac{R_1}{R_1+R_2}\right)$ V.

The control program implementing the operation described by the flowchart in figure 3.2 has been written using an assembly language, as discussed in section 3.2.2. A serious disadvantage of this programme is that the injection time delay calculated from equation (3.1) is dependent on the computer clock frequency. Hence, this would need to be recalculated if the program was running on a system with a different clock speed. To eliminate this dependency, the control program could be written making use of the built-in timer and counter chip in the PC (8254), to assist the timing coordination [121, 122]. Fed from a constant clock frequency of 1.1932MHz regardless of system speed, the 8254 can be programmed

as a timer to provide very accurate injection time control.

7.4 Simulation and Modelling Considerations

Simulation and modelling have played a major role in this work, particularly in the V_{inj} design process. Clearly, an accurate circuit model is necessary for the simulation results to be meaningful. In addition, the circuit model for V_{inj} optimisation should require a sensible simulation time, as the total design time is largely determined by the time spent in the simulation.

The most accurate circuit model of a switching converter is constructed as a direct copy of the actual circuit (detailed-mode simulation). This method, however, is not normally feasible due to the non-availability of models of some devices. Even if they are available, this technique often yields an excessively long simulation time, due to the complex non-linear characteristics of the switching devices, and convergence of results is likely to be a major problem. Hence, the use of macromodels is often necessary in SMPS simulation. Though its accuracy is limited, the use of macro-models greatly reduces the simulation time.

One of the most successful macro-models for studying the behaviour of SMPS is the averaged model. Obtained by averaging the behaviour of the converter power circuit over a switching period, the averaged model gives a result which is an averaged quantity of the instantaneous waveform. This is illustrated in figure 7.2 which compares instantaneous output voltage and inductor current simulated by the brute-force simulation (using the ideal switch model described in section 4.5.4) to the same results simulated by the averaged model.

Simulation using the averaged model is usually preferred to brute-force simulation in evaluations where the detailed switching ripple is not of interest, such as the transient response to either line or load disturbances. Simulation using the averaged model results in a much faster simulation time because it involves only the computation of *continuous* variables, not going through the repetitive calculations in each individual switching cycle as in brute-force simulation. To simulate the transient response of the VIC converter in this thesis, the simulation time by



Figure 7.2: Comparison of steady state output voltage and inductor current resulted from average and brute-force simulations

the averaged model is less than 2 seconds, whereas using brute-force simulation it is about 120 seconds (both simulations were performed by HSPICE running on a SUN SPARC4 workstation). Thus, the averaged model is preferable for the optimisation of V_{inj} .

As mentioned above, to achieve a meaningful V_{inj} solution, an accurate circuit model must be used in the optimisation. Thus, all power circuit component values specified in the netlist (see appendix B2) are measured values rather than nominal values. In the control section, the error amplifier uses a macro-model of the LM324 operational amplifier and the compensation circuit component values are measured values.

It is also necessary to model the interconnection and parasitic resistances in the power circuit. The parasitic resistances, in this case, include the power MOSFET and the diode ON-resistances, and the inductor resistance. Measurement on the PCB is one way of quantifying the interconnection and parasitic resistance, but can be difficult to do. As suggested in [94], a more practical approach is to estimate these values based on an empirical basis.

In this work, the interconnection and parasitic resistances are lumped together and represented by a single resistor r_L , whose value is chosen such that the model prediction closely matches actual measurement. The value of r_L was found to be about 0.9Ω . It should be noted that in this circuit r_L represents a damping factor, i.e. a larger value of r_L results in a slower closed-loop response speed. This method has been proved to be effective by the closeness that all the simulated results match their experimental counterparts (figures 6.16 to 6.21).

Due to the nature of PWM modulation, a slight discrepancy can occur in the resulting transient response, depending on where in a switching cycle load is applied. This effect cannot be seen with the averaged model and was studied by the use of brute-force simulation in section 6.2.4. The result given by the averaged model represents the average of the worst and most optimistic cases. This is illustrated in figure 7.3 for a one-cycle advanced injection case. In this figure, the definition used for simulation of best and worse scenarios was illustrated in figure 6.23. It should be noted that the instant of voltage injection was chosen to avoid double pulses within a switching period.

7.5 Future Phased Array Radar Systems

Future developments of airborne radar systems may well see the traditional microwave tube being replaced by solid-state phased array devices for the transmit/receive function [123]. In this type of radar system, known as electronically scanned phased-array radar, the transmit function is combined with the receive function into an array of Transmit/Receive (T/R) modules mounted directly behind each slot of a phased-array antenna.

Each T/R module consumes typically, at the present state of the art, 20W of power and operates with a power supply voltage of between 5 and 10V. In practice, up to a thousand of these T/R units are used to produce a high power radar. A low voltage power supply capable of supplying currents up to 2000A is thus



Figure 7.3: The output voltage in optimistic and worse cases and that given by the averaged model in one-cycle advanced voltage injection

required to power such a system.

Due to this enormous current requirement, it is likely that a power supply with the Distributed Power Systems (DPS) architecture shown in figure 7.4 will be used (references [124,125] provide a good technical background of DPS). Unlike the traditional Centralised Power Systems (CPS) where a single multiple-output power supply feeds the entire system, in DPS, a group of loads is supplied by a localised DC-to-DC converter module fed from the front-end AC-to-DC converter. In this way, voltage regulation is accomplished close to the load eliminating the problem of voltage drop over a long cable at a heavy load current, experienced in CPS. DPS architectures are widely used in DC power supplies in telecommunication and avionic applications, and computer systems. Some advantages of DPS over CPS are briefly summarised below [126]:

- Good voltage regulation
- No cross-regulation problems.
- Flexibility easy to upgrade/uprate.



Figure 7.4: A distributed power supply system incorporating voltage injection control for phased array radar systems

• High reliability

The disadvantages of DPS are:

- Lower efficiency due to two stage conversion.
- Increased EMI problems due to having many converters in a system.

The dynamic requirements of each converter module will be extremely stringent for maximum radar performance to be achieved. With a pre-warning signal from the radar processor, the VIC technique could be incorporated into these individual localised power supplies to enhance their dynamic performance, and thus the overall system performance of phased array radars.

7.6 Possible Applications of the VIC Technique

Although it was primarily proposed for radar power supplies, voltage injection control may also be extended to power supplies in other applications, where load disturbance is predictable or periodic. Such applications include power supplies in laser and sonar systems whose operating principles are very similar to radar systems, i.e. they are based on pulsed transmitting and receiving signals under the control of a processor unit.

The technique may be also extended to power supplies in more general applications, where the transient voltage caused by some equipment may effect the functionality of another circuit connected to the same bus. Figure 7.5 shows a simplified diagram of a power supply whose output feeds a small motor, as well as other electronic circuits (e.g. the disk drive in a computer). The bus transient



Figure 7.5: A small motor and a sensitive electronic load fed from the same output voltage bus

voltage caused by the motor operation (to move the read/write head) may result in a voltage excursion beyond the tolerance of some sensitive devices fed from the same bus. In this case, a signal from the processor may be used to activate the voltage compensation mechanism, before the motor is activated.

Modern computer systems, such as an Intel Pentium processor PC mother board, have been designed with power management features for the efficient use of electricity. Interfacing with a CPU, the Power Management Controller (PMC) unit is a microcontroller programmed to administrate efficiently the CPU power consumption as well as that of peripheral devices, while retaining maximum system performance. In portable computers (e.g. a notebook computer), an efficient power management strategy not only helps to reduce energy consumption, but also to extend battery life and reduce the heat dissipation issues created by operating a high-clock-frequency microprocessor (e.g. pentium chip) in a confined space with limited air flow [127]. From a power consumption point of view, computer operations can generally be divided into three operating modes as follows [128]:

- Active mode The nominal power is consumed in this mode, as the CPU is running at full clock speed and all peripheral devices are powered up ready to accept data and commands.
- Intermediate (or power saving) mode The power consumption is reduced due to the disconnection of some inactive peripherals or the reduction of CPU clock speed (i.e. CPU is in an idle state).
- Sleep mode The power consumption is minimal because most peripherals are inactive.

In a modern desktop computer, the typical power requirements in the active, intermediate and sleep modes are approximately 140W, 50W and 10W respectively². The rapid transition between these operating modes can cause serious transients in the power supply voltage. This transition process is, however, controlled by the CPU through the PMC unit, and therefore it would be possible to incorporate the VIC technique into a PMC unit to alleviate this problem.

²This information is from Mr Richard Soh, the chief engineer at Minebea Electronics Ltd, Glasgow, UK.

Chapter 8

Conclusion and Future Work

8.1 Conclusions

In airborne radar systems, system performance is strongly affected by the dynamic performance of their power supplies. The operation of the transmitter draws a step current from the power supply causing the power supply output voltage to drop. It is vital that the output voltage returns to within prescribed limits as quickly as possible to ensure correct operation of the receiver when it receives the echoed pulse signals from the target. A slow power supply dynamic response will result in a number of returning pulses being disregarded, causing a deterioration in the accuracy of the target information and thus in the system performance as a whole.

In this thesis, it has been demonstrated that Voltage Injection Control (VIC) is feasible and capable of giving excellent transient response due to load changes. To achieve the desired performance at a particular load change, both the magnitude of V_{inj} and the time at which it is applied must be optimised. The optimisation was carried out using the circuit optimiser incorporate within HSPICE employing the averaged circuit model of the VIC converter.

Experimental and simulated results in figures 6.16 to 6.21 have shown that when an optimised V_{inj} is used, transient response is greatly improved, such that the desired specifications are met. However, improvement in recovery time (as well as maximum voltage deviation) is achieved at the expense of introducing a spike voltage to the resulting response, due to advance voltage injection. The robustness of the VIC technique was clearly demonstrated for the step-load changes of 1.5A and 2.25A in which some optimised V_{inj} solutions result in the output voltage never dropping outwith the specified band (figures 6.16 and 6.17). The experimental results also agree well with their simulated counterparts, confirming the capability of the proposed HSPICE optimisation for designing V_{inj} .

The technique has also been tested in a current-mode controlled converter, and performs equally well (figure 6.25). Despite not being investigated in this thesis, similar outcomes are expected in a converter operating with DCM.

However, the limitations of VIC are:

- The extra voltage injection circuitry adds more cost to a system.
- Precise timing of load application must be known in advance.
- It is advantageous only in single-output power supplies, e.g. in a localised DC-to-DC converter in a distributed power system.

In this research, additional achievement has been made in the area of the design of the power supply control loop, in that HSPICE optimisation has been used to design the error amplifier compensation circuit. The proposed technique carries out the design in the time-domain through an iterative simulation/optimisation process, overcoming many limitations of traditional frequency-domain design methods. Using HSPICE optimisation, a compensation circuit is accurately designed with automatic fine-tuning accomplished. This optimisation approach can readily be adopted to design a compensation circuit in applications where stringent transient requirements are imposed, such as a power supply for the Intel Pentium processor.

Although the voltage injection control has been developed primarily for use in radar power supplies, the technique may also be implemented in power supplies in other applications, provided that the load switching pattern is well-defined.

8.2 Future work

The main emphasis of this research was to examine the concept and capability of the VIC technique, and to develop a systematic procedure for designing the injected voltage. Several issues were not covered during the course of the research which require further work. These topics, as well as possible extension to the current work, are outlined below:

- 1. The prototype VIC setup could be further extended to include synchronisation of the computer operation to the power supply switching frequency, in order to eliminate the transient response discrepancy discussed in section 6.2.4. To achieve this, the computer would have to sample periodically a reference timing signal provided at the programmed-frequency capacitor, C_t , (pin 7 in figure 3.5). This timing signal occurs at the beginning of every switching cycle and could be used by the computer, as a reference point, to calculate the specific instant in a switching cycle for load application.
- 2. The development of the proposed VIC technique into an intelligent system is another interesting research area. In this project, optimisation of V_{inj} is performed off-line, i.e. V_{inj} was pre-determinded and stored in the computer memory in the form of a look-up table. In an intelligent system, the V_{inj} optimisation would be performed on-line. Based on the present measured transient performance, the computer would compute a new injected voltage, using an appropriate optimisation strategy, for use next time the same load condition is applied. This optimisation process would be repeated each time that load is applied, until the desired transient performance is attained. However, performing on-line optimisation demands heavy computation and usually a lengthy programming code. In practice, the radar processor is already involved in intense computation associated with signal processing, and the availability of spare computing power to implement this on-line optimisation scheme must be questioned.
- 3. The possible extension of VIC to other applications has been discussed in section 7.6. The potential of the VIC technique appears particularly promising in the computer power management application. Issues relating to this

subject, including the feasibility of integrating VIC into the Power Management Controller (PMC), deserve further investigation. Also, the suitability of this technique to a wider range of applications should be explored.

- 4. The digitally controlled switched mode power supply for radar applications was first investigated by Holmes¹ in 1991 [25] (the advantages of digital control were highlighted in section 1.2.2.3). Due to the limited computing power of DSP chips available at that time, the switching frequency as well as the system bandwidth of the power supply were rather limited, preventing digital control from being fully exploited in this application. Additionally, the cost associated with the implementation of this control scheme was very high compared to its analogue counterparts. Recent advance in microelectronics and microprocessor technologies has made the realisation of a sophisticated, inexpensive digitally controlled switch mode power supply more feasible [129,130]. With a powerful digital signal processor (DSP) capable of performing elaborate calculations at very high speed, system switching frequency and loop gain bandwidth can now be realised at rational values. As voltage injection is much easier to implement digitally (through software), the next stage in radar power supply development could be the integration of voltage injection control into a digitally controlled radar power supply.
- 5. In a power supply control loop design, the traditional frequency response approach (section 6.1.1) uses a near ideal power circuit to simplify the design process. Due to this assumption, the predicted system performance is not accurate enough for practical power supplies which usually incorporate an input filter circuit (e.g. an EMI filter, an input current harmonic filter). To avoid the interaction, the resonant frequency of the input filter should be kept at least one decade away from the resonant frequency of the output filter. The design guideline for this is briefly summarised in [131] which, to some extent, involves trial-and-error. The capability of HSPICE optimisation could be broadened to include the interaction with the input filter in the design of the error amplifier compensation circuit, by incorporating the input filter circuitry into the simulation model.

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Appendix A

Voltage Injection Control Test Programme

Below is listed the VIC test program implementing the operation shown by the flowchart in figure 3.2. The program is written using C language, with the embedded assembly code which performs the required control tasks (described in section 3.2.2). Step-load conditions, magnitudes of V_{inj} and injecting times are stored in the form of look-up table by functions load_table, vinj_table and tinj_table respectively.

#pragma inline // Call turbo assembler

#include <iostream.h>
#include <stdio.h>
#include <conio.h>
#include <stdlib.h>

#define N0_TEST 6

int vinj_table(int k); // Define function storing a table of Vinj magnitude int tinj_table(int l; // Define function storing a table of injecting time int load_table(int m); // Define function storing a table of load selection code void init(void); // Define interfacing card initialised function

int main(void) // Main function
{

```
char x;
int i=0;
int v_inj,t_inj,load;
init(); // Initialise the interfacing card
printf( "Type 'x' to halt \n");
while((x = getch()) != 'x')
{
v_inj = vinj_table(i);
t_inj = tinj_table(i);
load = load_table(i);
 \mathrm{cout} \ll \mathrm{``Index} = \mathrm{''} \ll \mathrm{i} \ll \mathrm{``\backslash n''};
 cout « "Injected Voltage : " « hex « v_inj « "h\n";
 cout « "Injecting Time : " « dec « t_inj « "\n";
 cout « "Step-load Change : " « hex « load « "h\n";
 asm{
  // Initiate Vinj
                 v_inj
           al,
   mov
                 301h
           dx,
   mov
           dx,
                 al
   out
  // Injecting time delay
        mov cx, t_inj
   ff:
        nop
        nop
        loop
               ff
   // Switch on load
                 load
           al,
    mov
                  302h
           dx,
    mov
           dx,
                  al
    \operatorname{out}
```

```
// Duration of load
                          0
          mov
                 bl,
                          1
 delay2:
          \operatorname{cmp}
                 bl,
                 exit
          je
                          0fffh
           mov
                 cx,
 delay3:
          nop
           nop
                 delay3
           loop
           inc
                  bl
                  delay2
           jmp
// Clear Vinj
 exit:
        nop
                     0h
        mov
               al,
                     301h
               dx,
        mov
                    al
               dx,
        out
// Injecting time delay
             cx, t_inj
       mov
  tt: nop
       nop
       loop tt
 // Remove load
         al,
              0h
  mov
              302h
         dx,
  mov
               al
  out
         dx,
 }
 i++;
 if(i == 6)
               i=0;
 printf("\nType 'x' to halt \n");
  }
 return(0);
  }
 int vinj_table(int k) // Function contains a table of Vinj magnitude
```

·

```
{
int Vinj[NO_TEST] = \{0,0x9,0,0xd,0,0xf\};
return(Vinj[k]);
}
int tinj_table(int l) // Function contains a table of injecting time
{
int tinj[NO_TEST] = \{0,90,0,90,0,90\}; // CX=90 - 2cycles advance
return(tinj[l]);
}
int load_table(int m) // Function contains a table of load selection code
{
int step_load[NO_TEST] = \{0x70, 0x70, 0x50, 0x50, 0x30, 0x30\};
// 0x70 - 1.50A step-load
// 0x50 - 2.25A step-load
 // 0x30 - 2.75A step-load
 return(step_load[m]);
 }
 void init(void) // Initialise the interfacing card
 {
 // initialise I/O card
 asm{
              303h
         dx,
  mov
               80h
         al,
  mov
         dx,
               al
  out
 }
 // Set upper-half of port C to zero
 asm{
               0 fh
   mov
         al,
               302h
         dx,
   mov
               al
          dx,
   out
  }
  return;
  }
```

Appendix B HSPICE Netlists

B.1 Control loop optimisation netlist

Below is listed the HSPICE netlist for performing optimisation of compensation circuit described in section 6.1.2. The circuit schematic in figure 4.11, with V_{inj} set to zero, is used. The functionality of PWMBCK sub-circuit (figure 4.9) and VICVM sub-circuits (figure 4.10) is explained in sections 4.4.1 and 4.4.2 respectively.

***OPTIMISATION STRATEGY .model opt1 opt relout=1e-3 relin=1e-3 itropt=30

***DESIGN VARIABLES .param rx=optval(15k,10,100k) .param cx=optval(0.022u,0.001u,0.2u)

***DESIGN OBJECTIVES

.meas tran tsetting trig at=100u targ v(4) val=14.925 RISE=1 goal=1ms .meas tran overshoot max v(4) from=100u to=3ms goal=15 .meas tran min_limit min v(4) from=2ms to=3ms goal=14.925 .meas tran w_z2 param='rx*cx' *******************

.options acct nomod post opts optlst=2 probe dvdt=3 .MODEL DSWIT D(RS=.01) .tran 5u 3m .tran 5u 3m sweep optimize=optval result=tsetting,overshoot,undershoot, w_z2 + model=opt1

***** *BUCK POWER CIRCUIT ***** Vi 50 0 DC 33 rin 50 1 0.2 X1 1 0 2 0 12 PWMBCK d2 0 2 DSWIT rl 2 3 0.75 L 3 4 50U rc 4 5 0.027 C 5 0 470U R 4 0 20 ISWITCH 4 0 PULSE 0 3 100u 1N 1N 5m 6m ***** *CONTROL CIRCUIT ***** rd1 4 6 125K rd2 6 0 25K rc1 6 7 470 rc2 7 8 4.7K cc1 7 8 0.068u rc3 8 9 rx cc2 9 10 cxVref 11 0 2.5 X9 8 11 10 12 13 VICVM Vinj 13 0 0 ***** *VICVM SUB-CIRCUIT *********

.SUBCKT VICVM 1 2 3 10 11

.param EP=3.5.param EO=0.7

RINJ 11 0 10G

REI 2 1 100K CEI 2 1 1PF

GE 0 3 2 1 1.5M

REO 3 0 5MEG

CEO 3 0 80PF

D1 4 3 DS

D2 3 5 DS

RC 3 6 1G

VO 6 0 DC 0.7

RPWM 7 0 1k

D3 8 7 DS

D4 7 9 DS

VOMIN 8 0 DC 4

VOMAX 9 0 DC 92

ED 10 0 7 0 .01

VEMIN 4 0 DC 0.6

VEMAX 5 0 DC 4

* NODE 1 IS INVERTING INPUT

* NODE 2 IS NONINVERTING INPUT

* NODE 3 IS ERROR AMP OUTPUT

* NODE 10 IS DUTY CYCLE OUTPUT

.MODEL DS D(TT=1NS CJO=1PF)

***ERROR AMPLIFIER STAGE

***PULSE WIDTH MODULATOR STAGE

GPWM 0 7 POLY(2) 3 6 11 0 œ; 0 '(0.1)/(EP-EO)' '(0.1)/(EP-EO)'

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* NODE 11 IS INJECTED VOLTAGE INPUT

.ENDS

```
*****
```

PWMBCK SUB-CIRCUIT

SUBCKT PWMBCK 1 2 3 4 5 *NODES 1 & 2 ARE INPUT TERMINALS *NODES 3 & 4 ARE OUTPUT TERMINALS *NODES 5 THE DUTY RATIO INPUT

.param RO = 0.15

RD 5 0 1MEG RO 6 3 RO G1 1 2 POLY(2) 6 3 5 0 0 0 0 0 '1/RO' E1 6 4 POLY(2) 1 2 5 0 0 0 0 0 1 .ENDS .END

B.2 Vinj optimisation netlist

Below is listed the HSPICE netlist for the V_{inj} optimisation described in section 6.2.2. The functionality of PWMBCK sub-circuit (figure 4.9) and VICVM (figure 4.12) subcircuit is explained in sections 4.4.1 and 4.4.2 respectively. The measured values of power circuit parameters and compensation circuit components are used for simulation accuracy.

.param step_load=3.5

***OPTIMISATION STRATEGY .model opt1 opt relout=1e-4 relin=1e-4 itropt=30 close=15 ***DESIGN VARIABLES

.param tinj=optval(90u,100u,40u,10u) .param amplitude=optval(0.039,0,0.39,19.5e-3)

***DESIGN OBJECTIVES

.meas tran tsetting trig at=delay targ v(4) val=14.925 RISE=1 goal=0.25msec .meas tran v_max1 max v(4) from=101u to=2ms .meas tran overshoot param='v_max1-15' goal=0.075 .meas tran v_max2 max v(4) from='tinj' to=100u .meas tran spike param='v_max2-15' goal=0.075

*OPTIMISATION SET UP FOR 2.75A STEP-LOAD

*.param step_load=2.75

***OPTIMISATION STRATEGY

*.model opt1 opt relout=1e-4 relin=1e-4 itropt=30 close=10

***DESIGN VARIABLES

*.param tinj=optval(90u,100u,40u,10u)

*.param amplitude=optval(0.039,0,0.39,19.5e-3)

***DESIGN OBJECTIVES

*.meas tran tsetting trig at=delay targ v(4) val=14.925 RISE=1 goal=0.25msec

*.meas tran v_max1 max v(4) from=101u to=2ms

*.meas tran overshoot param='v_max1-15' goal=0.075

*.meas tran v_max2 max v(4) from='tinj' to=100u

*.meas tran spike param='v_max2-15' goal=0.075

*OPTIMISATION SET UP FOR 2.25A STEP-LOAD

*.param step_load=2.25

*****OPTIMISATION STRATEGY**

*.model opt1 opt relout=1e-4 relin=1e-4 itropt=40 close=20

***DESIGN VARIABLES

*.param tinj=optval(90u,100u,40u,10u)

*.param amplitude=optval(0.039,0,0.39,19.5e-3)

***DESIGN OBJECTIVES

- *.meas tran tsetting trig at=delay targ v(4) val=14.925 RISE=1 goal=0.25msec
- *.meas tran v_max1 max v(4) from=101u to=2ms

*.meas tran overshoot param='v_max1-15' goal=0.075

- *.meas tran v_max2 max v(4) from='tinj' to=100u
- *.meas tran spike param='v_max2-15' goal=0.075

***OPTIMISATION SET UP FOR 1.5A STEP-LOAD**

*.param step_load=1.5

***OPTIMISATION STRATEGY

*.model opt1 opt relout=1e-4 relin=1e-4 itropt=30 level=1 close=5

***DESIGN VARIABLES

*.param tinj=optval(90u,100u,40u,10u)

*.param amplitude=optval(0.039, 0, 0.39, 19.5e-3)

***DESIGN OBJECTIVES

*.meas tran tsetting trig at=delay targ v(4) val=14.98 RISE=1 goal=0.08msec

*.meas tran v_max1 max v(4) from=101u to=2ms

*.meas tran overshoot param='v_max1-15' goal=0.075

*.meas tran v_max2 max v(4) from='tinj' to=100u

*.meas tran spike param='v_max2-15' goal=0.075

Appendix B : HSPICE Netlists

.options post probe nomod optlst=2 dvdt=3 .MODEL DSWIT D(RS=.01) .tran 10u 2m .tran 10u 2m .tran 10u 2m sweep optimize=optval result=tsetting,overshoot,spike model=opt1

***** *BUCK POWER CIRCUIT ****** Vi 50 0 DC 33 rin 50 1 0.2 CIN 1 0 197UF X1 1 0 2 0 12 PWMBCK d2 0 2 DSWIT rl 2 3 0.85 L 3 4 49.5U rc 4 5 0.033 C 5 0 449U R 4 0 20 ISWITCH 4 0 PULSE 0 step_load 100u 1N 1N 20 30 ***** *CONTROL CIRCUIT *********** rd1 4 6 99.6K rd2 6 0 19.7K rc1 6 7 475 rc2 7 8 4.68K cc1 7 8 87.3n

rc3 8 9 26.9k

cc2 9 10 10.569n

Vref 11 0 2.47583

X9 8 11 10 12 13 VICVM

Vinj 13 0 pulse 0 amplitude tinj 1n 1n 10 20

***PULSE WIDTH MODULATOR STAGE

RC 3 6 1G

REI 2 1 100K CEI 2 1 1PF GE 0 3 2 1 1M REO 3 0 100MEG CEO 3 0 10PF VEMIN 4 0 DC 0.6 D1 4 3 DS VEMAX 5 0 DC 4 D2 3 5 DS

RINJ 11 0 10G

.param EP=3.5 .param EO=0.7 .param T=10u .param TO=1u .MODEL DS D(TT=1NS CJO=1PF)

***ERROR AMPLIFIER STAGE

* NODE 11 IS INJECTED VOLTAGE INPUT

* NODE 10 IS DUTY CYCLE OUTPUT

* NODE 3 IS ERROR AMP OUTPUT

* NODE 2 IS NONINVERTING INPUT

* NODE 1 IS INVERTING INPUT

.SUBCKT VICVM 1 2 3 10 11

Appendix B : HSPICE Netlists

VO 6 0 DC 0.7 **PWM modulator taking account a dead time of the sawtooth signal GPWM 0 7 POLY(2) 3 6 11 0 0 '(0.1*(T-TO))/((EP-EO)*T)' + '(0.1*(T-TO))/((EP-EO)*T)' RPWM 7 0 1k VOMIN 8 0 DC 4 D3 8 7 DS VOMAX 9 0 DC 92 D4 7 9 DS ED 10 0 7 0 .01 .ENDS

*PWMBCK SUB-CIRCUIT ******

SUBCKT PWMBCK 1 2 3 4 5 *NODES 1 & 2 ARE INPUT TERMINALS *NODES 3 & 4 ARE OUTPUT TERMINALS *NODES 5 THE DUTY RATIO INPUT

```
.param RO = 0.15
```

RD 5 0 1MEG RO 6 3 RO G1 1 2 POLY(2) 6 3 5 0 0 0 0 0 '1/RO' E1 6 4 POLY(2) 1 2 5 0 0 0 0 0 1 .ENDS .END

B.3 Buck converter with current-mode control netlist

Below is listed the HSPICE netlist of the current-mode controlled regulator in figure 4.13. The functionality of PWMBCK sub-circuit (figure 4.9) and VICCM (figure 4.12) subcircuit is explained in sections 4.4.1 and 4.4.3 respectively.

Appendix B : HSPICE Netlists

.options post probe acct nomod dvdt=3 .tran 5u 2m .probe tran v(4) .MODEL DW D(RS=.01)

***CURRENT SENSE AMP. HIL 12 0 Vi 0.1

* VICCM SUB-CIRCUIT

SUBCKT VICCM 1 2 3 17 18 19 11 10 *PIN 1 INVERTING INPUT *PIN 2 NON-INVERTING INPUT *PIN 3 ERROR AMP. OUTPUT *PIN 17 INPUT VOLTAGE SENSE *PIN 18 OUTPUT VOLTAGE SENSE *PIN 18 OUTPUT VOLTAGE SENSE *PIN 19 SWITCH CURRENT SENSE INPUT *PIN 11 INJECTED VOLTAGE INPUT *PIN 10 DUTY RATIO OUTPUT

.model DS D(TT=1NS CJO=1PF)

***ERROR AMPLIFIER STAGE REI 2 1 100K CEI 2 1 1PF GE 0 3 2 1 1.5M REO 3 0 118MEG CEO 3 0 8.6PF VEMIN 4 0 DC 0.6 D1 4 3 DS VEMAX 5 0 DC 4 D2 3 5 DS

R_VIOSENSE 17 18 1G RINJ 11 0 1MEG

ESUM 6 0 POLY(2) 3 0 11 0 0 1 1 RSUM 6 0 1MEG \$ ESUM=V3+V11

RHIL 19 0 1MEG ECAMP 14 0 19 0 3 RCAMP 14 0 1MEG

Appendix B : HSPICE Netlists

```
***RAMP GENERATOR (M1 & M)
EM1 15 0 17 18 '(3*0.1*20)/(2*35)'
VM 16 15 '(3*0.1*5*20)/35'
RSLP 16 0 1G
4
***PULSE WIDTH MODULATOR STAGE
ENUM 12 0 POLY(2) 6 0 14 0 0 1 -1
RDIV 12 13 1G
EDENOM 13 0 POLY(2) 10 0 16 0 0 0 0 1
GPWM 0 7 12 13 1
RPWM 7 0 100MEG
VOMIN 8 0 DC 1
D3 8 7 DS
VOMAX 9 0 DC 99
D4 7 9 DS
 ED 10 0 7 0 0.01
 RD 10 0 1G
 .ENDS
```

*PWMBCK SUB-CIRCUIT ******

.SUBCKT PWMBCK 1 2 3 4 5 NODES 1 & 2 ARE INPUT TERMINALS NODES 3 & 4 ARE OUTPUT TERMINALS NODES 5 THE DUTY RATIO INPUT

.param RO = 0.15

```
RD 5 0 1MEG
RO 6 3 RO
G1 1 2 POLY(2) 6 3 5 0 0 0 0 0 '1/RO'
E1 6 4 POLY(2) 1 2 5 0 0 0 0 1
```

S ENUM = V6-V14

EDENOM = V10*V16

.ENDS .END

B.4 Brute-force simulation netlist

Below is listed the HSPICE netlist of the buck regulator for brute-force simulation using the ideal switch model described in section 4.5.4. The simulation option (.options) has been configured to give convergence results and is explained in section 4.5.4.

```
.options acct post probe pivot=13 rmin=1e-12 itl4=100 dvdt=2
+ lvltim=3 absvar=0.2 relvar=0.2 ft=0.2
.MODEL DIODO D(N=1M RS=1M)
.tran lu 3.5m uic
.probe tran Vout=v(5) Ve=v(11) Vc=v(14) Vinj=v(13)
```

.param amp=0.1755 .param delay=1946u

```
rc 5 6 0.027
```

```
C 6 0 470u ic=15
```

R 5 0 20

ISW 5 0 PULSE 0 3 2006u 1N 1N 20m 30m

*CONTROL CIRCUIT

******* rd1 5 7 125k rd2 7 0 25k rc1 7 8 470 rc2 8 9 4.7kcc1 8 9 0.068u rc3 9 10 27k cc2 10 11 0.01u xerr 9 12 11 ERRAMP vref 12 0 2.5 Vinj 13 0 pulse 0 amp delay 1n 1n 20m 30m esum 14 0 poly(2) 11 0 13 0 0 1 1 rsum 14 0 1meg xcomp 15 14 16 COMPARATOR vsaw 15 0 pulse 0.73.50 10
u0.001u0.0001u 10.0011
u rsaw 15 0 1meg edrive 3 0 16 0 1 .

*ERROR AMPLIFIER SUB-CIRCUIT *****

SUBCKT ERRAMP 16 19 4 *NODE 16 IS INVERTING INPUT *NODE 19 IS NON-INVERTING INPUT *NODE 4 IS ERROR AMPLIFIER OUTPUT

RERR_INP 16 19 100K CERR_INP 16 19 1P GERR_AMP 0 4 19 16 1.5M RERR_OUT 4 0 5MEG CERR_OUT 4 0 80P D1 5 4 DIODO VERR_MIN 5 0 0.5

Appendix B : HSPICE Netlists

D2 4 6 DIODO _VERR_MAX 6 0 5 .ENDS

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VREF1 1 0 0.5 D1 1 6 DIODO RREF1 6 12 10K D2 6 3 DIODO VREF2 3 0 3.8 D7 4 2 DIODO VREF3 4 0 0.5 RREF2 2 13 10K D8 2 7 DIODO VREF4 7 0 3.8 EPWM 10 0 6 2 1K D9 0 8 DIODO RPWMOUT 8 10 10K D10 8 11 DIODO VPWMOUT 11 0 1 ESEG1 12 0 15 0 1 ESEG2 13 0 14 0 1 .ENDS

 .SUBCKT SW1 1 4 5 E1 2 1 2 3 1 RD 2 3 1 EG 3 4 POLY(2) 2 4 5 0 0 1 0 0 -1 RIN 5 0 1 .ENDS

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Appendix C Publications

The work described in this thesis has been reported in the following publications:

- [†] C. Bunlaksananusorn, D.E. Macpherson and F. Fisher, "Voltage Injection Control for Power Supplies in Radar Applications", in Proceedings *EPE-97*, Trondheim, Norway, vol. III, pages 167-172, September, 1997.
- [†] D.E. Macpherson and C. Bunlaksananusorn, "Optimisation of Switch Mode Power Supply Control Circuit Using HSPICE", in Proceedings UPEC-97, Manchester, England, vol. II, pages 810-813, September, 1997.
- † Reprinted in this appendix.

VOLTAGE INJECTION CONTROL FOR POWER SUPPLIES IN RADAR APPLICATIONS

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<u>Abstract.</u> A new control method is proposed to enhance the dynamic response of power supplies that have a predictable load switching pattern, such as in radar applications. By injecting a small voltage into the control loop in advance of the load application, the dynamic response is greatly improved. Both experimental and simulated results are presented, demonstrating the robustness of the technique.

Keywords. Switch mode power supplies, SPICE, simulation, modelling

1. INTRODUCTION

Switched Mode Power Supplies (SMPS) are used as the DC power source in the vast majority of modern electronic systems. The DC output voltage is regulated by employing feedback control to modulate the pulse. Control of a SMPS to satisfy its dynamic and steady state performance specifications requires careful design of the feedback loop and proper choice of the control method. In recent years numerous works have been published on establishing new control strategies [1-4], with the common aim of improving the dynamic performance of the converter. However, these control strategies have not yet reached the stage where they can be implemented in commercial power supplies, and active research on these control strategies is ongoing.

The two standard control methods used in commercial SMPS are voltage-mode control and current-mode control. It is well-known that current-mode control has a generally superior performance over its voltage-mode counterpart [5,6], and for most applications a well designed power supply incorporating current-mode control yields satisfactory results. Nevertheless, in some applications such as in radar systems, system performance is severely limited by the dynamic response of the power supply to sudden load changes.

In a radar system, although the transient requirements of the power supply are closely specified, the load switching pattern is both regular and predictable. By knowing in advance precisely when load will be applied, a signal can be sent to the control circuit to increase the pulse width of the converter in advance of the load application, allowing considerable transient response improvement to be achieved, thus enhancing the performance of the radar system. This technique has led to the proposal of Voltage Injection Control (VIC) for radar power supplies and is described in this paper. The principle of voltage injection control is explained in Section 2. In Section 3, the mathematical model of a buck regulator with voltage injection control is developed. Optimisation of the injected voltage is addressed in Section 4, and all results are presented in Section 5.

2. VOLTAGE INJECTION CONTROL

A buck converter with the proposed VIC control circuit is illustrated in Figure 1. An external summing block has been added to the standard voltage-mode control loop, allowing an externally controlled voltage to be injected into the control loop, thereby increased the pulse width of the converter.



Figure 1. Buck converter with the proposed Voltage Injection Control

2.1 Principle Of Operation

In a conventional system (Figure 1 with $V_{inj}=0$), when load is applied, the output voltage will drop below its

regulated value and the error signal, V_e , will increase, hence increasing V_c . V_c is compared to the sawtooth signal at the comparator stage which will consequently widen the PWM pulse to reduce the error.

After passing through the transient state, the converter eventually settles to a new steady state and the output voltage is brought back to its regulated value, as shown in Figure 2.



Figure 2. Dynamic response to a load change

The duration of the transient is dictated by the loop gain bandwidth, and normally a large number of switching cycles is required before the steady-state is regained.

When the step injected voltage, V_{inj} , is applied into the control loop, the input to the comparator, V_c , is:

$$V_{e} = V_{e} + V_{ini} \tag{1}$$

A step change in V_c increases the pulse width and forces the output voltage to rise. Once applied, the injected voltage remains constant until the load is removed. The error signal will decrease, and from (1) the control signal, V_c , also decreases resulting in a narrowing of the duty ratio to reduce the error. After passing through the transient state, the previous steady state of the converter, before the voltage injection, is reinstalled, as the output voltage is brought back to its regulated value. V_c resumes to its previous value, but at the expense of V_e being compensated by V_{inj} , as shown in Figure 3. The duration of the transient is again dictated by the loop gain bandwidth.

If the timing and magnitude of load application/rejection is known in advance, this information can be used to start a compensation mechanism, the voltage injection, before load is applied. By injecting an appropriate value of V_{inj} , significant improvement of transient response can be obtained. By the definition given in [7], VIC is classified as a disturbance feedforward control.



Figure 3. Dynamic response to a voltage injection

2.2 Implementation

The summing circuit in Figure 1 includes summing and inverting amplifiers as depicted in Figure 4.



Figure 4. Summing circuit for voltage injection

The summing amplifier adds the injected voltage, V_{inj} , to the error signal, V_e , giving (1) but with an inverted polarity. Thus, it has to be followed by an inverting amplifier to invert the signal back to a required polarity. In this work, the control of the injected voltage, which embraces both timing and amplitude control, is accomplished by a computer and is discussed in more detail in Section 4.

From the stability point of view, the implementation of VIC should not alter the pre-determined control-loop characteristics [8,9], otherwise it may lead to an unpredictable instability. To avoid this, an unity-gain summing circuit is used, removing the effect of VIC implementation on the system stability and leaving it dependent solely on the initial design of the control loop.

3. MATHEMATICAL MODEL

In this section, a mathematical model of a converter employing VIC is developed and is used in the optimisation of the injected voltage described in Section 4. The state-space averaging modelling approach described in [10] is used, as it is capable of giving accurate results and is easily implemented for SPICE simulation [11].

The state-space averaged model of the buck power circuit depicted in Figure 1 can be formulated as:

$$\begin{bmatrix} \frac{di}{dt} \\ \frac{dv}{dt} \end{bmatrix} = \begin{bmatrix} \frac{-(r+r_{L})}{L} & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{CR} \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix} + \begin{bmatrix} \frac{V_{i}}{L} \\ 0 \end{bmatrix} d$$
(2)

$$V_{a} = \begin{bmatrix} r & 1 \end{bmatrix} \begin{bmatrix} i \\ v \end{bmatrix}$$
(3)

The error amplifier and its compensation circuit can be expressed as:

$$V_{e} = \frac{Z_{2}(s)}{Z_{1}(s)} (V_{ref} - V_{v})$$
(4)

Vinj is a step injected voltage function. Mathematically it can be written as:

$$V_{inj} = A u (t - t_d)$$
⁽⁵⁾

where

 $\begin{array}{ll} u(t-t_d) &= \text{ unit step function at time } t_d \\ t_d = 1,2,3,...,n \text{ is the injection time (number of switching , cycles in advance of load application)} \\ A = amplitude of the injected voltage (volts) \end{array}$

From (1), the output of the summing circuit is thus:

$$V_{c} = V_{c} + Au(t - t_{d})$$
⁽⁶⁾

The comparator compares the control voltage, V_c , with a reference sawtooth voltage (V_{saw}) to produce the duty ratio (d), and is represented by:

$$d = \frac{V_c}{V_m}$$
(7)

where $V_m = peak$ sawtooth voltage signal.

Substituting (4) and (5) into (7) gives the VIC control law:

$$d = \frac{\frac{Z_{1}(s)}{Z_{2}(s)}(V_{ref} - V_{o}) + Au(t - t_{d})}{V_{m}}$$
(8)

Equation (2), (3) and (8) thus form a model of the closed loop buck regulator with voltage injection control.

4. INJECTED VOLTAGE OPTIMISATION

The magnitude of V_{inj} , and the number of cycles in advance of load switching that V_{inj} is applied, must both be optimised (5) to achieve the desired transient performance. In this section, these optimising variables are discussed, together with a short description of HSPICE, a package used to carry out the optimisation.

4.1 Optimising Variables

The injected voltage amplitude is controlled by the computer through a D/A converter. The resolution, which is the amplitude difference between any two consecutive injected voltages, is set to 19.5mV. Therefore, the amplitude of the injected voltage is a discrete variable where:

$$A_{i+1} - A_i = 0.0195, i=0,1,2,...,255$$
 (9)

The injecting time is defined as the number of cycles in advance of the load application that V_{inj} is applied, as shown in Figure 5.



Figure 5. Illustration of the injecting time definition

It is assumed that a load is applied during an ON period of the cycle i of the gate drive signal. The pulse width can be increased one cycle in advance of the load switching by injecting the voltage at the point indicated by the arrow in the i-1 cycle, or two cycles in advance by injecting the voltage at the point indicated by the arrow in the i-2 cycle, and so on. Therefore, the injecting time is also a discrete variable and a subset to the positive integer domain:

$$t_d \subset I^+$$
 (10)
where $I^+ = 1, 2, 3, ...$

It should be noted that the injected voltage can in fact be applied anywhere in the region A (or B) for two-cycle (or one-cycle) advance compensation.

Although the preceding definition of the injecting time assumes that the load is applied during the ON period, it also holds true for when load is applied during the OFF period. However, a slightly discrepancy does exist between the worse case scenario, when the load is applied at the beginning of the OFF period, and the optimistic one, when the load is applied near the end of the ON period. However, it is beyond the scope of this paper to go into this in detail.

4.2 Multi-Objective Optimisation

The optimum transient response is usually specified by the desired performance specifications e.g. voltage overshoot, settling time, maximum voltage deviation and spike voltage (the latter is the voltage rise caused by V_{inj} in advance of load being applied). These performance specifications are likely to be competing with one another, such that an improvement in one specification leads to a degradation in at least one of the remaining specifications. Therefore, in the optimisation a compromise between these multiple competing objectives has to be reached in such a manner that all objectives are satisfied.

Multi-objective optimisation [12,13] is a suitable technique for formulating and solving this category of problem. In multi-objective optimisation, there is no unique 'optimal' solution, but rather a set of 'non-inferior' solutions, which are the solutions that yield no violation of any of the design objectives. From the non-inferior solutions, the trade-off between these conflicting objectives can be studied.

4.3 Optimisation using HSPICE

The optimisation is carried out making use of the mathematical model developed in Section 3. A SPICE netlist of the state-space average model given by equations (2), (3), and (8) is constructed, and the HSPICE [14] simulator which incorporates a circuit optimiser is used as the simulation-optimisation platform.

To perform optimisation in HSPICE, the keyname OPTIMIZE must be specified in the netlist analysis statement (.TRAN, .AC or .DC), and the keyname OPT must be given in the .MODEL statement. The .MODEL statement also allows optimisation control options such as the maximum number of iterations and the algorithm used etc., to be selected. The optimising variables and design specifications are specified through .PARAM and .MEASURE statements respectively. More details of these statements can be found in reference [14].

5. RESULTS

The buck converter shown in Figure 2 with the following specifications: L=50 μ H, C=470 μ F, R=20 Ω , V_i=35V, V_o=15V, f_s=100kHz, I_{omin}=1A, and I_{omax}=5A, has been built and used in this work. The desired transient specifications are stringently specified and shown in Table 1. The voltage overshoot as well as the spike voltage must not exceed 0.5% of the nominal output voltage, while the settling time, taken when the response settles to within ±0.5% of the nominal value (15 volts), must be satisfied. The maximum voltage deviation is not included as it is not normally a critical parameter for power supplies in radar applications. The power supply includes a carefully designed error amplifier compensation circuit in the feedback loop to improve the dynamic performance.

Load Transient Performance	Desired Value
maximum voltage overshoot	15.075 volts
maximum spike	15.075 volts
settling time	250µs

Table 1- Desired transient performance

Without VIC, when the power supply is subjected to a step load of 2.75A, the transient response shown in Figure 6 is obtained.



Figure 6. Transient response to a 2.75A step-load change without VIC (experimental)

It takes approximately 1.2ms for the transient response to settle, which is far too slow compared to the desired settling time. This result suggests that even with a well design control circuit, it is unlikely that the stringent specifications specified in Table 1 can be obtained using standard control techniques.

Using VIC, the optimisation of the injected voltage has been carried out by HSPICE for various step-load change conditions. The task of the optimiser is to optimise the two optimising variables, the amplitude and injecting time of the injected voltage, constrained by (9) and (10), to satisfy the desired objectives:

$$V_{overshoot} \le 0.075 \tag{11}$$

 $V_{spike} \le 0.075$ (12)

$$t_{set} \le 250E - 6$$
 (13)

Figure 7 shows the simulated optimised transient response, subjected to the same step-load condition as in Figure 6, given by one of the non-inferior solutions. The response is said to be optimum because all the specifications in Table 1 have been satisfied. The selected solution is 0.273(t-2cycles), i.e. a step voltage of 0.273V amplitude is applied 2 cycles in advance of The corresponding optimum the load application. transient response obtained experimentally is illustrated in Figure 8, which corresponds very closely with the simulated result. This not only confirms the accuracy of the state-space averaged model in switching regulator modelling, but indicates that it is an effective tool for calculating the injected voltage used in VIC. As can be seen by comparing Figures 6 and 8, there is a big improvement in performance by the introduction of VIC.



Figure 7. Optimum transient response to a 2.75A stepload change with VIC (simulated)

The design trade-offs for the 2.75A step-load change have also been studied and are depicted in Figure 9. The non-inferior solutions of V_{inj} in which the injecting time is constant and equal to 2 cycles are selected and plotted against the three design objectives. From Figure 9, it can be seen that as the amplitude increases, the settling time decreases, but at the expense of larger voltage overshoot and spike voltage. The voltage overshoot increases more rapidly than the spike voltage and is the first objective to be violated. It is therefore identified as the main obstacle to any further transient response improvement.



Figure 8. Optimum transient response to a 2.75A stepload change with VIC (experimental)



Figure 9. Design trade-offs for a 2.75A step-load change

6. CONCLUSION

Voltage Injection Control has been developed to improve the transient performance of power supplies in applications where the load switching pattern is predictable, such as in radar systems.

Systematic procedures to obtain the appropriate value of injected voltage to produce the desired transient performance have been accomplished by the use of multi-objective optimisation using HSPICE. The experimental and simulated results clearly demonstrate the advantages of the technique as the stringent specifications have been achieved.

Although in this paper the technique has been demonstrated in a switching regulator using voltage mode control, it has also been tested in a converter with the more popular current mode control, and performs equally well.

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OPTIMISATION OF SWITCH MODE POWER SUPPLY CONTROL CIRCUITS USING HSPICE

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ABSTRACT

This paper describes an optimisation technique, implemented using HSPICE and its incorporated circuit optimiser, to overcome the drawbacks inherent in available design methods and ease the task of designing the error amplifier compensation circuit. A design example is presented and compared with the results from a classical design technique. The validity of the optimised design is confirmed by experimental results.

1. INTRODUCTION

Switched Mode Power Supplies (SMPS) are a basic building block in all modern electronic systems ranging from the modern office equipment (e.g. personal computers, printers, fax machines, etc.) to highly systems systems, sophisticated (e.g. radar The increasing telecommunication systems, etc.). complexity of electronic systems has resulted in ever more demanding requirements being placed on their power supplies, particularly in terms of power density, efficiency, electromagnetic compatibility, and output voltage control. The trend towards lower operating voltage for integrated circuits has further increased the burden on power supply designers.

The output voltage is specified both in terms of steady state voltage regulation, and also its response to transient conditions (e.g. application/rejection of load). The SMPS regulates the output voltage by comparing it with a reference voltage, and using feedback control to modulate the pulse width of the switching transistor(s). To design the SMPS to meet both steady state and dynamic requirements requires careful design of the control circuit, in particular the compensation circuit around the error amplifier in the feedback loop.

1.1 Frequency Response Design

The design of linear time-invariant Single Input Single Output (SISO) control systems is normally carried out in the frequency domain using classical control theory[1]. Figure 1 shows the basic block diagram of a SMPS from the control system point of view, consisting of the power circuit, PWM modulator, and error amplifier with the compensation circuit, with transfer functions T_{pw} , T_{mod} , and T_{err} respectively. There is

an additional, inner current loop for systems using current mode control (used in most power supplies).





The design task is to define T_{err} to give the desired open-loop gain frequency characteristic $(T_{pw}, T_{mod}, T_{err})$, while not violating the stability criterion [2] (typically, a phase margin of at least 45° is required for a stable system). With the aid of a Bode plot, the design is carried out graphically in the frequency domain, simplifying the design process. However, the method has the following limitations:

- 1. The power supply is assumed to be linear with small-signal perturbations around the operating point; whereas in practice, a converter can be subjected to large disturbances, either from line or load changes.
- 2. The design is carried out in the frequency-domain, whereas the target specifications are time-domain parameters (voltage regulation, maximum deviation from nominal and recovery time under transient conditions). Therefore, it is common that the desired specifications are not met at the first attempt, with fine-tuning required, usually on a trial-and-error basis.

3. The effects of circuit/device parasitics are usually omitted to simplify the process.

1.2 Existing CAD Approaches

Circuit simulation programs such as SPICE and SABER are being used increasingly in SMPS design to validate accurately the initial design results. The SMPS design environment developed in [3] uses SPICE as a simulation platform for validating the design Using the averaged circuit model [4], the results. compensation circuit design is carried out by repeatedly simulating the circuit and validating its performance, until a satisfactory result is met. Because a trial-and-error approach is used to adjust the circuit component values for each simulation run, it can be very time consuming, particularly when designing for stringent specifications.

MATSPICE, a compensation circuit design environment using optimisation, has been proposed in [5]. The package incorporates MATLAB, PSPICE, and some C interfacing routines to implement the optimisation design environment. However, the authors mention that the execution time of the program is slow, owing to the considerable amount of data being transferred between MATLAB and SPICE for each optimisation iteration, preventing it from being an efficient design tool.

In this paper, optimisation using HSPICE [6] is proposed as a solution to overcome the drawbacks of the existing tools. With the proposed method, the limitations of conventional frequency response design are avoided, as the non-linear large-signal model (instead of a small-signal model) is used, and the circuit parasitics can easily be incorporated, and automatic fine-tuning of the design is accomplished through iterative simulation and optimisation. Unlike MATSPICE, the execution time of the HSPICE optimisation depends only on the complexity of the optimisation problem.

2. OPTIMISATION DESIGN USING HSPICE

The optimisation design scheme in HSPICE (illustrated in Figure 2) is an iterative design environment embracing circuit simulation, performance evaluation, and design variable (compensation circuit component values) optimisation until either the desired specifications are attained, or no solution is found after a pre-defined maximum number of iterations. In the input HSPICE netlist, the converter under design is modelled by the large signal state-space average model described in [4]. The selection of the model is justified because of its accuracy and fast simulation time [7]. In addition to the circuit description, information concerning the optimisation task must also be stated in the netlist.



Figure 2 Optimisation design scheme in HSPICE

The design variables are defined through the **.PARAM** statement in which the initial guess, minimum and maximum values are specified. The design objectives, the desired specifications (e.g. voltage overshoot, maximum voltage drop, settling time etc.) are stated through the **.MEASURE** statement. To perform optimisation in HSPICE, parameters in the analysis statements (**.TRAN**, **.AC** or **.DC**, with the keyname **OPTIMIZE**) must be given corresponding to those in the **.MODEL** statement. Also, the optimisation control options (e.g. the convergent criterion, and the algorithm used), are selected through the **.MODEL** statement. Detailed usage of these statements can be found in reference [6].

3. DESIGN EXAMPLE

The application of HSPICE optimisation to the design of a SMPS error amplifier compensation circuit is demonstrated by the design example of a simple buck regulator using voltage mode control depicted in figure 3.



Figure 3 A buck switching regulator

The buck converter has the following specifications: L=50 μ H, C=470 μ F, R=20 Ω , Vi = 35V, Vo=15V, Io(min)=1A, and Io(max)=5A, switching frequency fs=100KHz. The two-pole, two-zero compensation circuit surrounding the error amplifier is designed to satisfy the following objectives: 1. The required regulation limits are $\pm 0.05\%$ of nominal output voltage.

2. A settling time less than 1ms is required, when the converter is subjected to a 3A step load change (60% of maximum load current).

The compensation circuit was designed using classical frequency domain methods, resulting in the component values given in column 1 of Table 1. The associated transient response for a 3A load change is depicted in figure 4(a).

It can be seen that a rather slow response is obtained and the design target is not yet met. From the result, it is apparent that this sluggish response is caused by the low system loop-gain. The speed of the response can be enhanced to meet the desired specification, by optimising the error amplifier's gain (thus optimising the loop-gain).

It is unnecessary to select all five compensation circuit components as design variables, as the error amplifier can be tuned by varying R3 and C2, while keeping the rest of the components constant. Having too many design variables makes the optimisation more difficult and may cause a convergence problem. For these reasons, only R3 and C2 are selected as design variables, with the results from the frequency response design assigned as the initial values.

HSPICE is run on a SUN SPARC4 workstation. After a few iterations of simulation and optimisation, the optimised solution is found, with the results listed in column 2 of Table 1. It can be seen that the optimiser has met the specification by increasing R3 and decreasing C2, thus increasing the error amplifier gain. The simulated and experimental optimum transient responses are shown in figures 4(b) and 4(c) respectively. The simulated result behaves very closely to its experimental counterpart, confirming the accuracy of the averaged model in SMPS modelling.

It should be noted that in addition to the results in column 2 of Table 1 found by the optimiser, there exists a set of solutions that satisfy the design objective. Some of these solutions may yield better transient responses (e.g. faster settling time with small voltage overshoot) than that in figures 4(b). This set of solutions is called non-inferior solutions [8]. It is a task of a designer to carry out the existing trade-off between these solutions.



(a) Output voltage transient response due to a 3A load change, before optimisation (simulated)

(b) Output voltage transient response due to a 3A load change, after optimisation (simulated).

(c) Experimental result after optimisation
Frequency Response Design	HSPICE Optimisation Design
$R1 = 470\Omega$	$R1 = 470\Omega$
$R2 = 4.70k\Omega$	$R2 = 4.70k\Omega$
$R3 = 16k\Omega$	$R3 = 27k\Omega$
$C1 = 0.068 \mu F$	$C1 = 0.068 \mu F$
$C2 = 0.022 \mu F$	$C2 = 0.01 \mu F$

Table 1. Compensation circuit component values before and after optimisation

4. CONCLUSION

The application of the circuit optimisation feature in HSPICE to design SMPS compensation circuits has been described. Unlike traditional frequency response design, the proposed method carries out the design by means of iterative time-domain simulation and optimisation, automatically fine-tuning the design to meet the target specifications. The design example demonstrates the capability of this technique, with a significant improvement in the transient response such that the design target is met. It is suggested that the proposed method can be used to facilitate and speed up the compensation circuit design phase of SMPS.

5. REFERENCES

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