Single-Stage Power Factor Correction Converter Topologies for Low Power Off-Line Applications

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Abstract

Since January 2001 it has been necessary for equipment connected to the low voltage public distribution network in Europe and Japan to comply with IEC 61000-3-2. The regulation IEC 61000-3-2 specifies the level of current that can be drawn for particular harmonics. Much equipment today is fitted with a Switch Mode Power Supply (SMPS) at its input to interface between the line voltage and internal low voltage electronics. This SMPS must not only convert the line voltage, but also ensure that the input current to the device meets the IEC regulations.

To meet these regulations two methods are normally used, passive filtering using a large filter inductor or a boost converter cascaded with the main DC/DC SMPS converter with isolation. To try and reduce component count, cost and increase efficiency many new single-stage Power Factor Correction (PFC) topologies have been proposed. In a single-stage topology the output voltage regulation and meeting IEC 61000-3-2 are combined into a single power stage. Unfortunately very little is known about the behaviour or performance of these single-stage topologies.

In this thesis two of the more promising single-stage topologies: the bi-forward and CS S^2PFC converters are investigated further. A new topology using a low frequency switch (LFSPFC) is introduced. The topologies are analysed investigating input current shape and harmonic content, voltage variation on bulk capacitance and component stresses. Simulation in PSpice is used to confirm circuit operation.

Four 150W output power experimental circuits were built, bi-forward converter, CS S^2PFC converter, passive filtering cascaded with a forward converter and a boost pre-regulator cascaded with a forward converter. The converters operate from universal input voltage and have outputs at 5V and 12V. A 100W test circuit was built for the LFSPFC operating from 230V input voltage and with an output of 5V.

Experimental results are presented showing circuit behaviour and performance of the bi-forward, CS S^2PFC and LFSPFC converters. The bi-forward and CS S^2PFC converters are compared to the passive filter and boost converter cascaded with a forward converter. It is demonstrated that neither of these single-stage topologies are at present a viable replacement for either present method, but the LFSPFC could be a lighter weight and less bulky alternative to passive filtering.

Declaration

I declare this is thesis has been completed by myself and that except where indicated to contrary, the research documented is entirely my own work.

Edward Michael Lord

Dedication

In memory of Katie Lord

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Abbrevations

AC	Alternating Current
AC/DC	Alternating Current to Direct Current
BIBRED	Boost Integrated with a Buck Rectifier/Energy storage/Dc-dc converter
BIFRED	Boost Integrated with a Flyback Rectifier/Energy storage/DC-dc converter
BJT	Bipolar Junction Transistor
BS	British Standard
CCM	Continuous Conduction Mode
CS S^{2}PFC	Current Source Single-Stage Power Factor Corrector
DB	Diode Bridge
DCM	Discontinuous Conduction Mode
DC	Direct Current
DC/DC	Direct Current to Direct Current
EMI	Electro Magnetic Interferance
EN	European Standard
ESR	Equivalent Series Resistance
IC	Integrated Circuit
ICS	Input Current Shaping
IEC	International Electrotechnical Commission
IGBT	Insulated Gate Bipolar Transistor
LC	Inductor Capacitor
LFR	Loss Free Resistor
LFSPFC	Low Frequency Switch Power Factor Corrector
MOSFET	Metal Oxide Silcon Field Effect Transistor
PC	Personal Computer
PF	Power Factor
PFC	Power Factor Correction
PWM	Pulse Width Modulation
RCD	Resistor Capacitor Diode
RMS	Root Mean Squared
SMPS	Switched Mode Power Supply
SSIPP	Single-Stage Isolated Power-Factor-Corrected Power Supply
TV	Television
VMC	Voltage Mode Control
UK	United Kingdom

Symbols

A_c	Conduction of Input Current (LFSPFC)
D	Duty Ratio for Switch S_1
D_1	Duty Ratio for Switch S_1 when Operating from Bulk Capacitor (LFSPFC)
D_2	Duty Ratio for Switch S_1 during Period 2 (Bi-Forward)
	Duty Ratio for Switch S_1 when Supplied Direct from Input (LFSPFC)
D_3	Duty Ratio for Switch S_1 during Period 3 (Bi-Forward)
D_4	Duty Ratio for Switch S_1 during Period 4 (Bi-Forward)
D_{4A}	Duty Ratio for Switch S_1 during Period 4A (Bi-Forward)
D_{eff}	Effective Duty Ratio for L_2 (LFSPFC)
D_f	Duty Ratio for Fall of DCM Current in Inductor L_1 (CS S^2PFC)
	Duty Ratio for Fall of Current in Inductor L_1 (LFSPFC)
D_{f2}	Duty Ratio for Fall of DCM Current in Inductor L_1 during Period 2 (Bi-Forward)
D_{f3}	Duty Ratio for Fall of Current in Inductor L_1 during Period 3 (Bi-Forward)
D_{max}	maximum Duty Ratio (LFSPFC)
E_c	Energy lost by Bulk Capacitor
F	Line Frequency
F_{Dist}	Displacement Factor
F_{Dist}	Distortion Factor
f_s	Switching Frequency
I_1	RMS Fundamental Current
I_{2adif}	Difference between Current Rise and Fall in Inductor L_1 during Period 2A (Bi-Forward)
I_{2amin}	Minimum Current in Inductor L_1 during Period 2A (Bi-Forward)
I_{4min}	Minimum Current in Inductor L_1 during Period 4 (Bi-Forward)
I_{av}	Average Current in Inductor L_1 (LFSPFC)
I_{avc}	Average Current in Inductor L_1 during CCM (CS S^2PFC)
I_{avd}	Average Current in Inductor L_1 during DCM (CS S^2PFC)
I_{av2}	Average Current in Inductor L_1 during Period 2 (Bi-Forward)
I_{av2a}	Average Current in Inductor L_1 during Period 2A (Bi-Forward)
I_{av3}	Average Current in Inductor L_1 during period 3 (Bi-Forward)
I_{av4}	Average Current in Inductor L_1 during Period 4 (Bi-Forward)
I_{av4a}	Average Current in Inductor L_1 during Period 4A (Bi-Forward)
I_c	Current at which Diode D_5 Stops Conducting during CCM Operation of Inductor L_1 (CS S^2PFC)
I_o	Output Current
I_{p1}	Current in Inductor L_1 and Reflected Current in Inductor L_2 (LFSPFC)

I_{p2}	Current in Inductor L_1 and Reflected Current in Inductor L_2 Raises too (LFSPFC)
I_{pkd}	Peak current in Inductor L_1 when Operating in DCM (CS S^2PFC)
I_{pk2}	Peak Current in Inductor L_1 when Operating in DCM during Period 2 (Bi-Forward)
I_{pk2a}	Peak Current in Inductor L_1 during Period 2A (Bi-Forward)
I_n	RMS Current of Harmonic n
i_c	Bulk Capacitor Recharging Current
i_{dir}	Current Flowing Directly to the Output from the Input (Bi-Forward)
i_f	Current Flowing Directly to the Output from the Input (LFSPFC)
i_s	AC Line Current Drawn by Converter
n	Turns Ratio between Primary Windings
P_{in}	Input Power
P_o	Output Power
T	Time for a Half Line Period
T_s	Time for One Switching Cycle
t	Overall clock
t_1	Time after Zero Crossing that Inductor L_1 Enters DCM (CS S^2PFC)
t_2	Time after Zero Crossing that Inductor L_1 Enters CCM (CS S^2PFC)
t_3	Time after Zero Crossing that Inductor L_1 Enters DCM Again (CS S^2PFC)
t_4	Time after Zero Crossing that Inductor L_1 Stops Conducting (CS S^2PFC)
t_5	Time after Zero Crossing that Complete Cycle Ends (CS S^2PFC)
t_{2a}	Time after Zero Crossing that Inductor L_1 Enters Period 2A (Bi-Forward)
t_{3a}	Time after Zero Crossing that Inductor L_1 Enters Period 4A (Bi-Forward)
t_a	Zero Crossing Time (Bi-Forward, LFSPFC)
t_b	Time after Zero Crossing that Inductor L_1 Enters Period 2 (Bi-Forward) Time after Zero Crossing that Inductor L_1 Starts Conducting (LFSPFC)
t_c	Time after Zero Crossing that Inductor L_1 Enters Period 3 (Bi-Forward) Time after Zero Crossing that Inductor L_1 Stops Conducting (LFSPFC)
t_d	Time after Zero Crossing that Inductor L_1 Enters Period 4 (Bi-Forward) Half Line Period Zero Crossing Time (LFSPFC)
t_e	Time after Zero Crossing that Inductor L_1 Enters Period 3 Again (Bi-Forward)
t_f	Time after Zero Crossing that Inductor L_1 Enters Period 2 Again (Bi-Forward)
t_g	Time after Zero Crossing that Inductor L_1 Enters Period 1 Again (Bi-Forward)
t_h	Half Line Period Zero Crossing Time (Bi-Forward)
t_{off}	Time after Zero Crossing that S_2 is Turned Off (LFSPFC)
t_{on}	Time before Zero Crossing thst S_2 is Turned On (LFSPFC)
t_r	Time after Zero Crossing Bulk Capacitor Starts Recharging
V_1	RMS Fundamental Voltage
V_B	Average Bulk Capacitor Voltage
V_{co}	Switch Over Voltage
V_{D2}	Voltage Across Diode D_2
V_{D3}	Voltage Across Diode D_3
$V_{D5:5V}$	Voltage Across Diode D_5 on the 5V Output
V_{GS}	MOSFET gate to source voltage
V_{IN}	Input Voltage to Converter
V_{inmin}	Minimum Voltage that S_2 can turn on and off at (LFSPFC)
V_{min}	Minimum bulk Capacitor Voltage
V_{pk}	Peak of Line Voltage

V_o	Output Voltage of Converter
V_{S1}	Voltage Across Switch S_1
V_{SS}	Voltage Source Voltage
v_s	AC Line Input Voltage
ΔD	Duty Ratio for Rise of Current in Inductor L_D (CS S^{2}PFC)
	Duty Ratio for Rise of Current in Inductor L_1 (LFSPFC)
ΔD_3	Duty Ratio for Rise of Current in Inductor L_1 during Period 3 (Bi-Forward)
ΔD_4	Duty Ratio for Rise of Current in Inductor L_1 during Period 4 (Bi-Forward)
ΔD_{4A}	Duty Ratio for Rise of Current in Inductor L_1 during Period 4A (Bi-Forward)
ΔI_{2af}	Current Fall in Inductor L_1 during Period 2A (Bi-Forward)
ΔI_{2ar}	Current Rise in Inductor L_1 during Period 2A (Bi-Forward)
ΔI_4	Current Rise in Inductor L_1 during Period 4 (Bi-Forward)
ΔI_{4F}	Current Fall in Inductor L_1 during Period 4 (Bi-Forward)
ΔI_c	Current Rise in Inductors L_1 and L_D during CCM (CS S^{2}PFC)
ΔI_o	Current Ripple through L_2 (LFSPFC)
ω	Angular Line Frequency

Contents Summary

Contents

List of Figures

List of Tables

Chapter 1

Introduction

DC/DC Switched Mode Power Supplies (SMPS) are one of the most common methods to provide a DC power source for modern electronic equipment, ranging from office equipment such as personal computers, printers and fax machines to communications and radar systems. The increasing demands of modern electronic equipment for lower operating voltage, higher efficiency, and lower cost has led to a substanical increase in the use of SMPS. The increase in the use of DC/DC SMPS has led to the use of diode bridge rectifiers and capacitive smoothing to provide an unregulated DC voltage from the mains, which a DC/DC SMPS requires. The increase in SMPS usage has degraded line quality to the extent that regulations to control the harmonics of the current drawn by the power supply have been introduced.

This chapter reviews power factor, the need for power factor regulations, and the regulation itself.

1.1   The Need for Power Factor Regulations

SMPS are inherently a DC to DC converter and as such require a DC supply voltage to operate from. For converters operating from the AC mains supply a diode bridge rectifier and smoothing capacitor are used to give an unregulated DC supply as shown in figure 1.1. This also shows the voltage and current waveforms. For a reasonably smooth DC voltage the capacitance has to be large, so that the voltage sag across the capacitance is small. The

diodes will only conduct when the line voltage is greater then the capacitor voltage, and as the capacitor voltage does not sag very much, the capacitor is only recharged at the peak of the line voltage waveform. The current drawn, i_s, is a large spike as shown in figure 1.1, (often 5A or more) carrying all the energy required to recharge the capacitor. The current waveform shown in figure 1.1 has very poor power factor and is rich in harmonics.
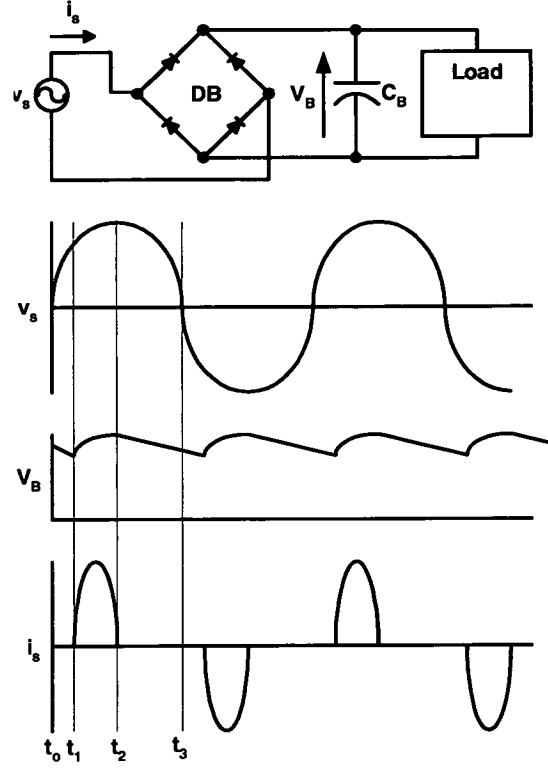
Figure 1.1: Diode bridge and capacitive rectification

1.1.1 Power Factor

Power Factor (PF) is a measure of useful line current supplied. It can be considered as the product of a distortion factor given by equation 1.1 [4], which is a measure of line current distortion, and a displacement factor given by equation 1.2 which is a measure of the line current lag from source voltage waveform at the fundamental frequency.

$$F_{Dist} = \frac{I_1}{\sqrt{I_1^2 + \sum\limits_{2}^{\infty} I_n^2}} \qquad (1.1)$$

2

where F_{Dist} is the distortion factor, I_1 is the RMS fundamental current, and I_n is the RMS current of harmonic n.

$$F_{Disp} = \frac{P_1}{V_1 I_1} \qquad (1.2)$$

where P_1 is the average input power from the supply, V_1 is the RMS fundamental supply voltage, and I_1 is the RMS fundamental supply current. F_{Disp} can be rewritten as:

$$F_{Disp} = \frac{V_1 I_1 \cos \phi}{V_1 I_1} \qquad (1.3)$$

where ϕ is the amount of phase lag between the current and voltage waveforms. From this the displacement factor can be reduced to:

$$F_{Disp} = \cos \phi \qquad (1.4)$$

Overall Power Factor (PF) is the product of the two factors:

$$PF = F_{Dist} F_{Disp} \qquad (1.5)$$

which is:

$$PF = \frac{I_1}{\sqrt{I_1^2 + \sum_{2}^{\infty} I_n^2}} \cos \phi \qquad (1.6)$$

The presence of higher order harmonics in the current and the amount of reactive power being drawn increases as PF decreases.

1.1.2 The Effects of Low Power Factor

It may seem that the effects on the AC distribution system of the circuit in figure 1.1 are negligible. This is no longer so as the use of sophisticated electronic equipment continues

to increase, and the number of low power quality loads attached to the line increases. There are a large number of capacitors being recharged at the peak of the line (as well as many other disturbances such as light dimmers, etc) and the cumulative effects of these low power factor loads causes a number of problems in the AC distribution system:

- Excessive neutral currents due to excessive reactive power

- Flattening of the peak of the sine wave voltage waveform

- Additional heating of distribution equipment

- Overvoltages due to resonances

Poor PF can also cause incandescent lights to flicker with variations in line frequency and RMS voltage. More seriously, a poor power factor can cause sensitive equipment to operate incorrectly or malfunction.

1.2   AC Power Quality Regulatory Standards: IEC 61000-3-2 [1, 2]

To reduce the problems caused by equipment with low PF, regulatory standards are being introduced around the world dictating the levels of harmonic current drawn by electrical equipment (not just SMPS). These regulations have been devised by the International Electrotechnical Commission (IEC), the worldwide organisation responsible for developing most electrical standards. The IEC develops standards for voluntary use, which can then be harmonised into regional or national standards.

IEC 61000-3-2 is the electrical standard for limits of harmonic current per phase. This document sets out the levels of current allowable for each harmonic and for different types of electrical equipment. IEC 61000-3-2 is mandatory in Europe (where it is known as EN 61000-3-2 or BSEN 61000-3-2 in United Kingdom), since January 1st 2001, and also in Japan.

1.2.1 IEC 61000-3-2

The regulations divide equipment into four different classes, known as classes A to D, for which different current harmonic levels are specified. There is no restriction on the phase of the current. Most SMPS will usually fall into either class A or class D and are outlined below. The remaining two classes are B and C. Class B covers portable tools and class C covers lighting equipment.

The IEC 61000-3-2 regulations only deal with the distortion component of PF, and even then current waveforms can still be non-sinusiodal as only the level of certain current harmonics is specfied. IEC 61000-3-2 does not specify anything to do with the displacement factor, so a current waveform could be completely out of phase with the voltage waveform (low PF), but still comply wth the regulations. Class D is discussed first.

Class D

In the latest amendment of IEC 61000-3-2 [2], in 2000, only two types of equipment fall into this category, with a power input of 600W or less:

- Personal Computers (PC) and personal computer monitors

- Television receivers

The harmonic regulations for class D limits are applied to the RMS level of the harmonic current for all odd harmonics from 3 to 39 and are scaled according to power. The class D limits are shown in table 1.1. The testing is carried out at nominal power input: the minimum power input specified, which has to comply with the regulations, is 75W. This may in the future be reduced to 50W, but this has not been decided yet.

For Japan the levels need to be multiplied by 2.3 to correct for the voltage difference between Japan (100V) and Europe (230V).

Class A

Class A harmonic regulations cover the following equipment [2]:

5

Harmonic Order, n	Maximum Permissible Current per watt, mA/W	Maximum Permissible Harmonic Current, A
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
$13 \leq n \leq 39$	$3.85/n$	See Class A

Table 1.1: Limits for class D equipment [1]

- Balanced three phase equipment

- Household appliances, excluding equipment named in class D

- Tools, excluding portable tools

- Dimmers for incandescent lamps

- Audio equipment

The limits for class A are absolute limits and apply to RMS current harmonic levels at odd and even harmonics up to 40. The limits are outlined in table 1.2 below. Again the same applies for Japan as for class D.

Harmonic Order, n	Maximum Permissible Harmonic Current, A
Odd Harmonics	
3	2.30
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
$15 \leq n \leq 39$	$0.15\frac{15}{n}$
Even Harmonics	
2	1.08
4	0.43
6	0.30
$8 \leq n \leq 40$	$0.23\frac{8}{n}$

Table 1.2: Limits for class A equipment [1]

For harmonics of the 21st order and above for both class A and D it is possible for the measured current to exceed the limits by 50% if the measured odd harmonic current does not exceed the partial harmonic current calculated from the limits and all RMS harmonic currents are equal to or less than to 150% of the limits.

1.3 Methods to Comply with IEC 61000-3-2

At present there are two basic methods used to build SMPS which comply with IEC 61000-3-2:

- Passive filtering using a large inductance to smooth current drawn by the bulk capacitors.

- Use of a two stage approach using a boost pre-regulator.

These two methods will be explained in more detail in chapter 2. It is generally considered that the two present methods are expensive, bulky and component intensive. In an attempt to reduce these disadvantages many new SMPS topologies have been suggested in the literature. These topologies are collectively known as single-stage power factor correctors. The majority of single-stage topologies combine the process of power factor correction (harmonic correction) and supplying DC output voltages into one activity, turning the SMPS into an AC/DC converter. There is very little known about these new topologies apart from all the benefits reported enthusastically in the literature.

1.3.1 Thesis and Contribution to Knowledge

Overall this project tests the hypothesis that: "Single-stage power factor correction topologies for low power SMPS off-line applications can meet the requirements of IEC 61000-3-2 and supply well regulated low voltage DC outputs".

Two single-stage power factor correction topologies known as the bi-forward and CS S^2PFC converters were selected from the literature and studied in further detail. For each topology the ability to meet IEC 61000-3-2, the variation of bulk capacitor voltage, the component stress and general operation were investigated using a combination of analysis, simulation

7

and experimental testing. Most of the analysis carried out has not been applied to these topologies before. To test the hypothesis of this thesis circuits were designed and built using the two single-stage power factor correction topologies and were compared with both a forward converter cascaded with a filter inductance and a forward converter cascaded with a Power Factor Correction (PFC) boost converter.

This thesis also presents a new single-stage power factor correction topology using a low frequency switch developed during the project. The low frequency switch is in series with the bulk capacitor of a forward converter. Analysis and experimental test results investigating the behaviour of this circuit and its ability to meet IEC 61000 classes A and D are presented.

1.4   Objectives of the Research

This research was to investigate the possiblity of single-stage power factor correctors being replacements for the current methods of PFC. The objectives of the research were as follows:

1. To determine the most promising topologies from the literature.

2. To study the the most promising topologies in detail so as to learn both the positive and negative aspects of these converters, as the literature normally only presents the positive aspects.

3. To compare the new promising topologies with the two existing PFC methods.

4. To suggest improvements to the new topologies, to improve performance.

5. To suggest alternative methods to meet IEC 61000-3-2.

This project was carried out with the cooperation and support of Minebea Electronics (UK) Ltd. The possibility of using single-stage PFC topologies as power supplies in personal computers was being considered by the company.

1.4.1 Typical Application

This research has been carried out with the PC power supply in mind. This application has been chosen as it will allow testing of the new topologies to the most demanding part of the regulations (class D) and to the tough specifications of a PC power supply. Other applications only have to meet class A regulations, but have similar output requirements to a PC power supply (low voltage, high current), so testing also considered class A testing.

Chapter 2

PC Power Supplies: The Present

Personal Computer (PC) power supplies are required to convert AC mains input voltage to controlled and isolated DC outputs. A typical power supply needs to operate from the "universal" voltage ranges of 90V to 130V and 180V to 265V, while supplying outputs at 12V, 5V, 3.3V and -12V. Output power can range from almost zero to full load powers ranging from 70W to 300W. Under IEC 61000-3-2 computing equipment [2] such as PCs is required to meet class D harmonic regulations.

In this chapter basic switched mode power topologies are reviewed, and the topologies currently used as the main converter and the two most common methods of Power Factor Correction (PFC) are briefly presented. The implications of IEC 61000-3-2 on PC power supplies are discussed.

2.1 Basic Switched Mode Power Supplies

In DC/DC SMPS a solid state device is used as a high frequency (20kHz+) electronic switch to convert one DC voltage to another. In figure 2.1 the three basic SMPS topologies are shown from which almost all other SMPS are derived.

In the buck converter, the power switch, S_1, is turned on and the diode, D_1, is reverse biassed and energy is tranferred from the supply to the output through the inductor, L_1. When the switch is turned off the current built up in the inductor freewheels through the diode. The output voltage of the buck converter is always lower than the supply voltage and

ideally only depends on the expression given in figure 2.1 where D is the ratio of the time that S_1 is conducting to the whole switching period. The boost and buck-boost converters operate on a similar principle of inductive energy transfer. In a boost converter the output voltage is always higher than the supply, and in the buck-boost the output voltage can be either higher or lower than the supply, but of the opposite polarity.

$$V_O = DV_{IN}$$

Buck Converter

$$V_O = V_{IN}\frac{1}{1-D}$$

Boost Converter

$$V_O = V_{IN}\frac{D}{1-D}$$

Buck-Boost Converter
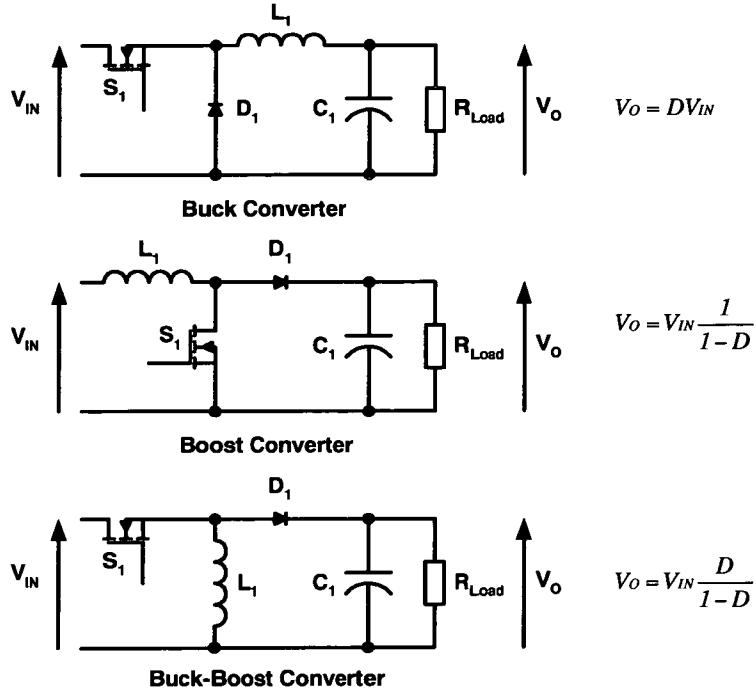
Figure 2.1: Basic switched mode power supply topologies

2.1.1 Continuous and Discontinuous Conduction Modes

The filter inductor of a SMPS can operate in either Continuous Conduction Mode (CCM) where the current in the inductor never falls to zero, or in Discontinuous Conduction Mode (DCM) where inductor current falls to zero and is not flowing for some of the switching cycle. The different modes of conduction are shown in figure 2.2. The conduction mode depends-on the load current, inductance value and switching frequency.

The benefits of continuous conduction mode are:

- Lower peak current through transistors and diodes than in DCM for the same load current. This results in lower stress on semiconductor components so reducing power
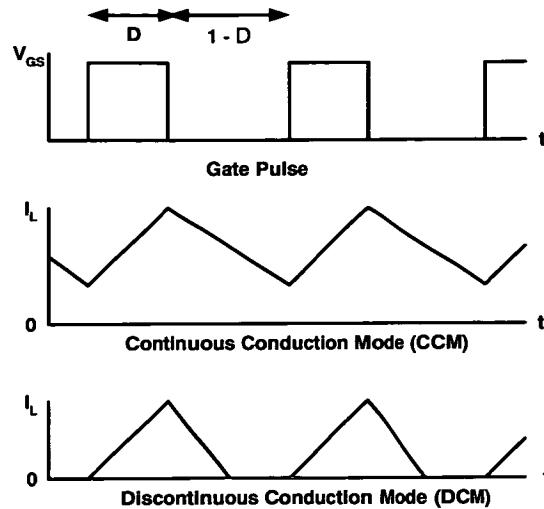
Figure 2.2: Different modes of inductor current

loss, size and cost.

- Good open loop regulation.

The disadvantages are:

- A larger inductor is required than with DCM.

- Poor closed loop response. It takes time for the current in the inductor to change in response to a disturbance. In DCM the current in the inductor can change on a cycle by cycle basis.

2.1.2 Output Voltage Control

There are a variety of control schemes:

1. Constant frequency Pulse Width Modulation (PWM). The switching frequency of the converter is fixed and the time of the on period (time the power switch is conducting) is varied to control the output voltage. The ratio of on time to switching period is the duty cycle (D). PWM is the most common method used, as fixed frequency enables magnetic components to be better utilized.

2. Variable frequency fixed pulse. Either the on or off time is kept constant while the other is varied to control the output voltage.

3. Frequency and pulse modulation. Both are varied to control output voltage.

2.2   Topologies Currently used as the Main Converter in PCs

There are three topologies that are commonly used as the main converter in personal computers. These are the

1. Single switch forward converter

2. Double switch forward converter

3. Half bridge converter

There is often also a small auxiliary converter, used for operation in sleep mode, which is normally based on the flyback converter. Typically the single switch forward is used at the lower end of the power range in supplies of up to 200W, while the double switch forward and half bridge are used for higher powers.

2.2.1   Single Switch Forward Converter
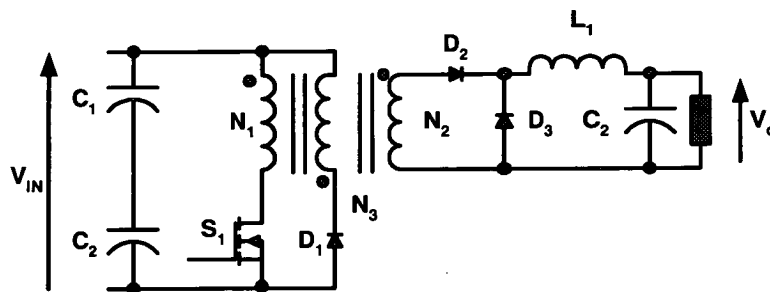
Figure 2.3: Single switch forward converter with tertiary reset winding

The forward converter shown in figure 2.3 is essentially a buck converter with transformer isolation. When the power switch S_1 is turned on current flows through the primary of the transformer transferring energy to the secondary. Current in the secondary will then flow via

13

diode D_2 charging up the inductor L_1. When S_1 is turned off diode D_3 becomes forward biassed and D_2 reverse biassed. The current in L_1 now freewheels via D_3. When S_1 turns off the transformer is reset by returning, to bulk capacitors C_1 and C_2, magnetising current built up during the on period via winding N_3.

A PC power supply is designed to operate in CCM for the majority of the time. With outputs supplying 20 to 30A this helps to reduce peak current stress in the semiconductor components as well as power loss. The usual method of output voltage modulation is fixed frequency PWM. The conversion ratio for a forward converter operating with PWM is shown in equation 2.1. Due to the need to reset the transformer the duty cycle, D, is restricted to 0.5 when $N_1 = N_3$. N_3 can be reduced to enable longer pulses, but this increases the voltage across the power switch. An alternative method of resetting the transformer, which is gaining popularity, is to use an Resistor Capacitor Diode (RCD) snubber.

$$D = \frac{V_o \cdot N_1}{V_{IN} \cdot N_2} \tag{2.1}$$

The main power switch is normally a Metal Oxide Silicon Field Effect Transistor (MOSFET); these are used as they can be switched at a high frequency without excessive power loss unlike the Bipolar Junction Transistor (BJT) or Insulated Gate Bipolar Transistor (IGBT). Unfortunately the MOSFET has to be rated for at least twice the bulk capacitor voltage (due to voltage induced in the primary during transformer reset) which is at least 750V when operating at the high end of the input voltage range. For a multiple output converter such as a PC power supply there will be multiple transformer secondaries or stacked secondaries. The output inductor L_1 will have multiple windings (one winding for each output) on a single core to improve cross regulation between the various outputs. The secondary side diodes are normally a mixture of Schottky diodes for the lower voltage outputs (5V and 3.3V) to reduce loss and normal fast recovery diodes for the 12V outputs.

2.2.2 Double Switch Forward Converter

The double switch forward converter shown in figure 2.4 is used in higher power converters (300W+) as the losses in the main switch become unmanageable in the single switch forward at higher powers. The basic operation is the same as the single switch forward.

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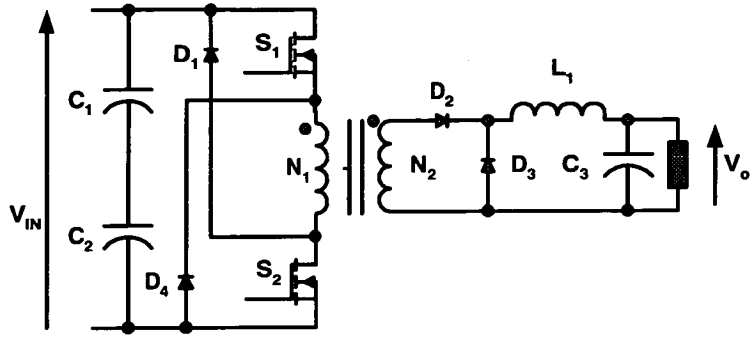
Figure 2.4: Double switch forward converter

The two MOSFETs are turned on and off together and the transformer is reset via the two diodes D_1 and D_4. The main difference is that during reset the voltage on the MOSFETs is only as high as the bulk capacitor voltage. This allows the use of lower voltage MOSFETs that are cheaper and have a lower on state resistance (R_{dson}). There is however an added complication, due to the need for transformer coupled drive for MOSFET S_1.

2.2.3 Half Bridge Converter
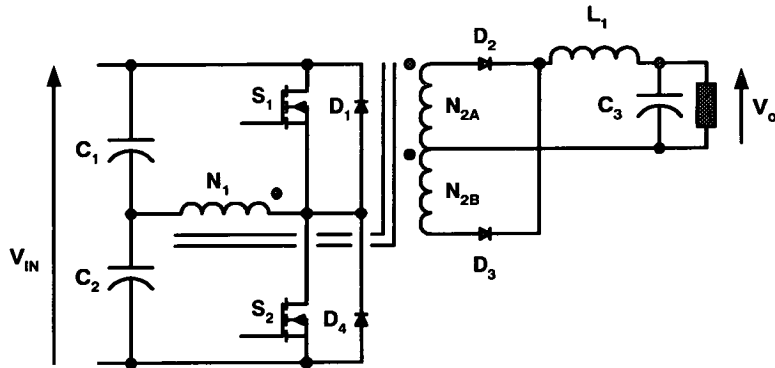
Figure 2.5: Buck based half bridge converter

The buck-based half bridge converter shown in figure 2.5 is used for power supplies supplying 200W or more. Requiring a centre-tapped (or full wave rectified) secondary on the transformer the operation of this topology is quite different to that of the forward converter. Considering a complete switching period, power switch S_1 is turned on and current flows through the transformer primary into the bulk capacitors. Energy is transferred into the top

half of the secondary winding, N_{2A}, and current flows through D_2 charging up inductor L_1. When S_1 turns off the magnetising current freewheels in the primary via D_1 or D_4 depending on its direction, as does current in L_1 through the secondary side diodes. Then S_2 is turned on and current flows through the primary of the transformer in the opposite direction from the bulk capacitors. This time the current in L_1 is increased via the other half of the secondary, N_{2B}. As there are two on-periods during a cycle the output filter L_1 and C_3 is operating at twice the switching frequency. The duty cycle for each switch is restricted to 0.5 to avoid shoot through (this occurs when S_1 and S_2 are on simultaneously).

2.2.4 Flyback Converter
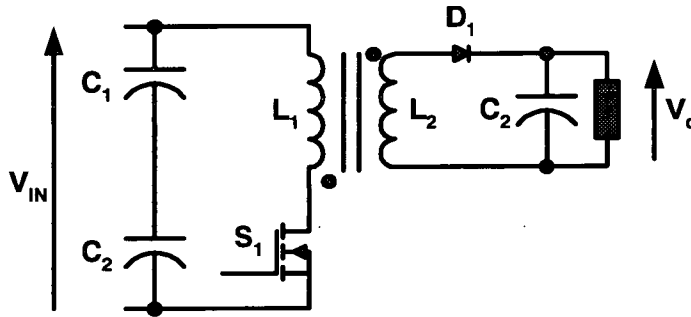
Figure 2.6: Flyback converter

The flyback converter, shown in figure 2.6, is generally considered a low power converter, but it is considered here as many new single-stage topologies are initially developed as a variation on the flyback. In this topology the transformer is operated as a coupled inductor. The current in the coupled inductor can flow either in CCM or DCM as shown in figure 2.2. When the power switch, S_1, is turned on current ramps up in L_1, either from zero in DCM or a non zero value in CCM. When S_1 is turned off the current built up in L_1 must keep flowing and the only route available is through L_2 (L_2 is wound on the same core as L_1) and D_1 to the the load.

2.3 Current PFC Techniques

The two most common methods of PFC in PC power supplies are the passive filter, which is used on converters of up to 200W, and the boost pre-regulator. Both methods are an extra

stage preceeding the main isolated power converter.

2.3.1 Passive Power Factor Correction
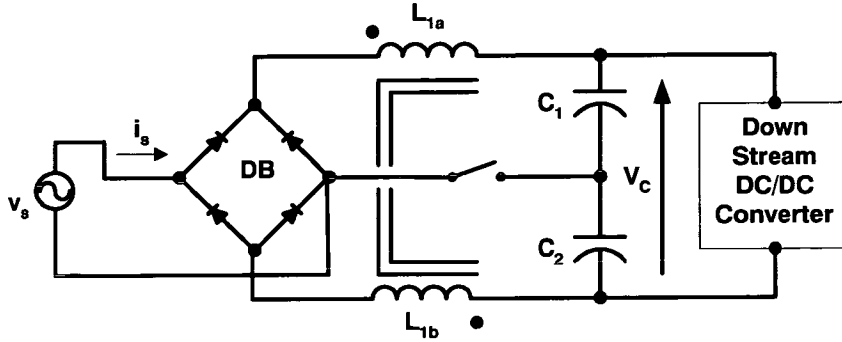
Figure 2.7: Passive filtering PFC

The normal method of carrying out passive PFC is shown in figure 2.7. The switch is a voltage selector which is open in the 230V range and closed when operating in the 115V range. This configuration doubles the voltage possible across the bulk capacitors when operating from low line, enabling the down stream SMPS to be more optimised. The inductor L_1 is wound on an iron laminated core as it is operating at low frequency (100/120Hz) and the inductance value is large (about 9mH to 40mH for a 150W output power supply, depending on whether the voltage selector switch is open). This method is only used for lower power supplies due to the bulky nature of the PFC choke.

When running from the 230V mains the two windings on the inductor are connected in series. During a half mains cycle the bulk capacitors C_1 and C_2 are partially discharged reducing the voltage across them, while supplying the converter. When the voltage of the supply rises above the voltage across the capacitors current starts to flow via L_{1a}, C_1, C_2 and L_{1b}, in a resonant manner. The resonance will stop when the current in L_{1a} and L_{1b} tries to go negative as the current is blocked by the diode bridge. The significant waveforms are shown in figure 2.8.

When running from the 115V range the selector switch is closed. The basic operation is the same as before. When operating with the selector switch closed the bulk capacitors are recharged individually. C_1 is recharged through L_{1a} during the positive half cycle and C_2 is recharged during the negative cycle via L_{1b}.

17
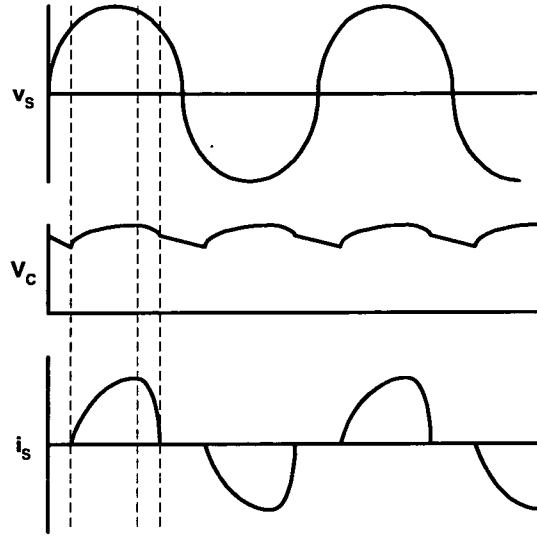
Figure 2.8: Passive filtering PFC waveforms

Further information on how to design and analysis a passive PFC filter can be found in [5, 6].

The passive PFC filter can exhibit sub-harmonic oscillation, see figure 8.5a taken from the prototype passive PFC circuit built for the comparison in chapter 8. The sub-harmonic oscillation is undesirable, but even with this phenomenon the circuit can still pass IEC 61000-3-2 for class D. Power supplies are sold exhibiting this feature.

2.3.2   Boost Pre-Regulator

The most common alternative to passive PFC is to have a boost converter pre-regulator supplying the main SMPS with a DC voltage source. This configuration is shown in figure 2.9. The boost converter can be controlled in such a manner as to draw nearly a perfect sine wave current from the line. It can supply a reasonably regulated DC voltage (stepped up to about 400V) for the main converter from a 90V to 265V input supply. L_1 can operate in either DCM, CCM or hysteresis mode. There are several different control schemes utilized for PFC boost converters including boundary mode and CCM mode.

The more popular method (which is used by Minebea Electronics UK Ltd) is the CCM PFC as shown in figure 2.9. Here the boost converter is operated at a fixed frequency and the current in L_1 is chopped to follow the input voltage waveform. This produces a 50Hz
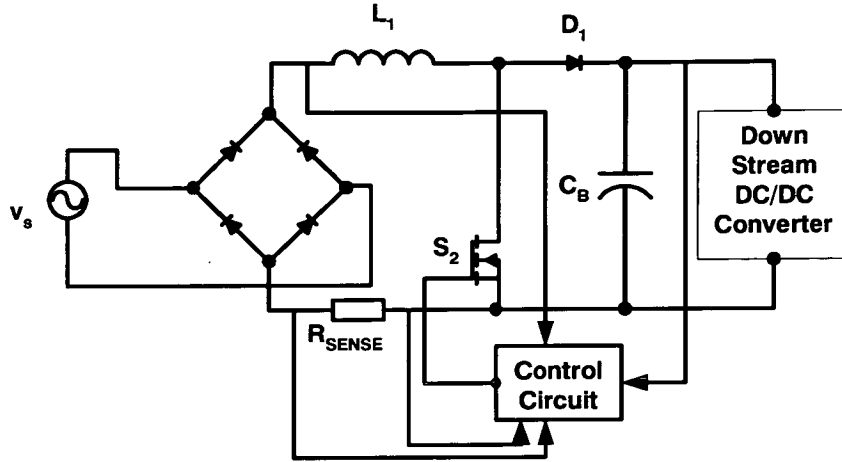
Figure 2.9: PFC boost pre-regulator operating in CCM

current sine wave with a high frequency ripple as shown in figure 2.10. The pulse width is determined by information from the bulk capacitor voltage (voltage feedback), input voltage (voltage feedforward) and average inductor current (average current mode control) (resistor R_{sense} is used to convert the current to a voltage signal for the controller).

For further information consult [7].
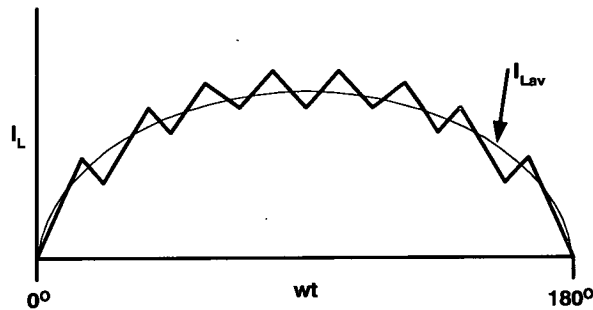
Figure 2.10: PFC boost pre-regulator operating in CCM current waveform

2.4 Advantages and Disadvantages of Current PFC Methods

The advantages and disadvantages of passive PFC and the two stage approach using the boost pre-converter are discussed below to provide a benchmark for evaluating single-stage topologies, as well as highlighting why single-stage PFC topologies are being proposed.

2.4.1 Passive PFC

Advantages:

- A very simple solution requiring just one additional component, the PFC choke.

- It produces a clean input current with no high frequency noise or ripple.

Disadvantages:

- The PFC choke is very large (manufactured on cores such as EI 38) and due to the iron laminated core, adds weight and takes valuable space in the power supply case.

- It can suffer from sub-harmonic oscillation.

- It can be difficult to design a passive choke to pass the class D regulations over a wide power range.

2.4.2 Two stage PFC with boost Pre-Regulator

Advantages:

- It produces an input current with a very high PF of about 0.99 across a wide power range.

- The boost converter and main isolating SMPS can be individually optimised to their own task.

- The boost converter is highly efficient.

- Due to the reasonably regulated output voltage from the boost converter, the isolated SMPS second stage can be designed to operate from a narrow input voltage range.

Disadvantages:

- There are a considerable number of additional components added to the basic DC/DC SMPS. This not only includes the power components, but also all its control circuitry

and heatsinking for the two extra semiconductors (boost MOSFET and diode). This requires additional space on the PCB and will add to the cost.

- The high voltage on the bulk capacitor will typically require the capacitor to be rated for 450V, which again is an additional cost.

- Improved inrush current limiting is required to avoid destroying the boost MOSFET.

- A slightly lower overall efficiency is expected as all power to the output is processed twice. Also the additional control circuitry needs powering.

The disadvantages listed above are enough to spur development of single-stage PFC topologies to overcome these difficulties.

2.5   The Regulations and the PC Power Supply

In chapter 1 it was mentioned that PCs must conform to class D of IEC 61000-3-2, the most stringent part. The reason for this is that PCs, PC monitors and TVs have been shown to have a significant effect on the supply system. The reasons in turn for this are [2]:

- The large number of these three appliances in use,

- The duration of use (many PCs are left on all the time),

- Their power consumption: although this is not high for individual items, collectively the power consumption is large,

- The harmonic spectrum of the input current.

It is possible for other equipment to be reclassified to class D if at a later date they fulfill the above critria.

A major problem when designing the PFC stage for a PC power supply is knowing the power to design for. Most PC manufacturers consider the power supply last, and normally heavily over-specify the power requirements. A typical PC will generally not require more than 60W of power, but most PC power supplies have to be able to supply 200W. The figure of 200W does allow for system upgrading, but when specifying the power supply output

21

ratings the PC manufacturers always build in a large margin of safety (another reason is that many cheap PC power supplies would have trouble supplying their full rated power). A PC power supply has to meet IEC 61000-3-2 class D:

- From 75W to full load,

- In Europe at 230V 50Hz,

- In Japan at 100V 50Hz, but not in the USA where the regulations have not been introduced.

Chapter 3

Review of Single-Stage PFC Topologies

Attempts to combine PFC and output voltage regulation into a simple, reliable and cheap single-stage converter to overcome the problems identified in Chapter 2 have been proposed since the early 1990s, but a single-stage does not necessarily mean the converter has to have just one power switch. The various circuits proposed tend to fall into two types:

- Converters that have a series power flow: this is where all the power to the output is processed by both the PFC part of the circuit and the output supply part. There is an energy storage element between the two parts of the circuit.

- Converters that have parallel power flow: this is where the majority of the power flows directly from the input to the output normally through the PFC stage of the circuit. The rest of the power flows on a parallel route via an energy storage element and conversion stage.

3.1 Series Single-Stage PFC Topologies

3.1.1 Differ PFC Converters

One of the earliest attempts was to make use of the differ effect. The conventional differ circuit shown in figure 3.1 was introduced in 1988 and is mentioned in [8]. The topology

23

is the integration of a buck-boost converter and a forward converter. When S_1 is turned on the output is supplied from C_B in the the conventional forward manner. At the same time L_1 is charged up from the supply. When S_1 turns off the current built up in L_1 freewheels and charges C_B via D_1. This circuit suffers from high voltage on the bulk capacitor when the input voltage is low. In [8] the input from the diode bridge is fed into a centre tapped primary which helps to control the voltage on C_B by reducing the voltage across L_1. A further differ rectifier based topology is proposed in [9] based on the integration of a boost converter and forward converter with a centre tapped secondary. To maintain a constant voltage on the bulk capacitor C_B, variable switching frequency (25kHz to 200kHz) control is employed with PWM to control output voltage, V_o.
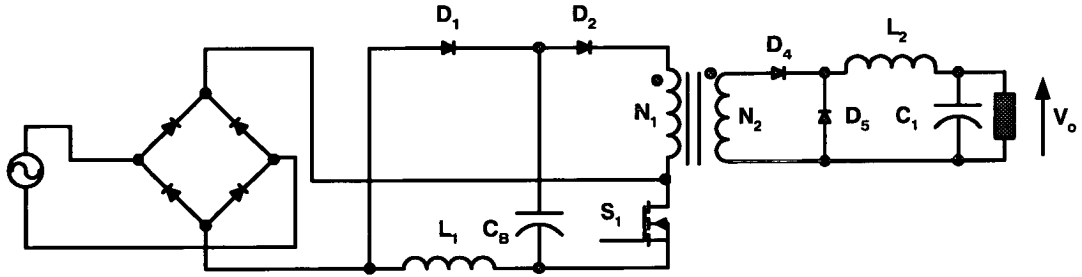
Figure 3.1: The differ single stage PFC topology

3.1.2 BIFRED and BIBRED

In 1992 in [10] the Boost Integrated with a Flyback Rectifier/Energy Storage/DC-DC converter (BIFRED) and Boost Integrated with a Buck Rectifier/Energy Storage/DC-DC converter (BIBRED) were developed, the first of many single stage topologies: shown in figures 3.2 and 3.3. The BIFRED is the integration of a DCM boost converter and a DC/DC flyback converter operating in either DCM or CCM, into one stage. The DCM boost converter operating with a fixed duty will emulate a resistor. The fixed duty is set in the steady state by controlling the output voltage. The energy storage element C_B is in series with the main power path. The same topology was produced in [11] by placing diode D_1 into a SEPIC converter.

The BIBRED is the integration of a DCM boost converter and buck converter operating in either DCM or CCM. The topology was re-produced in [12] by placing diode D_1 in a Cuk converter.
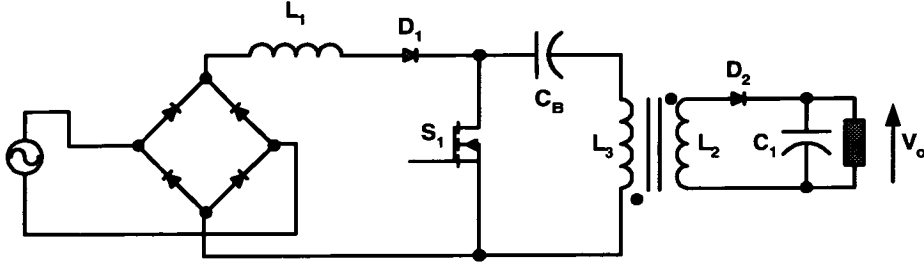
Figure 3.2: BIFRED converter
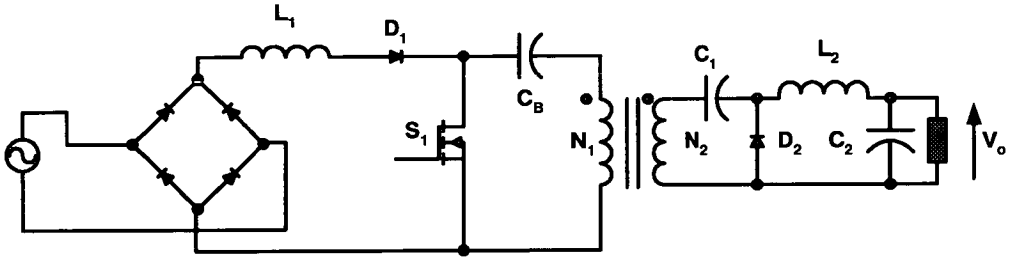
Figure 3.3: BIBRED converter

Unfortunately when operating with the output inductor L_2 in CCM the voltage on capacitor C_B is load dependant, and when operating at light CCM loads the voltage can be very high, especially when operating off the universal voltage range. To reduce the high voltage on C_B in [13] variable frequency control as well as the normal PWM control is applied. The alternative method is to operate the output inductor, L_2, in DCM as in [11], which also improves the input current waveform. [14] introduces a negative feedback winding wound on the transformer placed in series with L_1 in the BIFRED converter with L_2 operating in CCM. The winding is used to feedback the voltage on capacitor C_B (seen across the flyback transformer when S_1 is on) and reduce energy absorbed from the line by L_1. This helps to reduce the voltage on C_B at light loads. [15] uses a similar method on the BIBRED converter, but instead of using a transformer winding, a magnetic amplifier is used instead. To reduce the size of the BIFRED converter [16] integrates the three magnetic components onto one core. The integrated core has inherent ripple cancellation, which removes the need for a differential mode filter inductor on the input of the converter. In [17] a passive clamp is added to the BIFRED to protect the switch from voltage spikes caused by the leakage inductance of the transformer.

3.1.3 Single-Stage Isolated Power-Factor-Corrected Power Supply (SSIPP)

In [18] the energy storage element C_B is moved to be in parallel with the main energy path but all energy is still processed twice. The resulting topology is shown in figure 3.4 and is called the Single-Stage Isolated Power-factor-corrected Power supply (SSIPP). This topology is the integration of a DCM boost converter and a flyback (or forward) converter operating in DCM or CCM sharing the same switch. As with the BIFRED and BIBRED, if inductor L_2 operates in CCM then the voltage on bulk capacitor C_B is load dependant, hence it is advised to operate L_2 in DCM. When operating with L_1 and L_2 in DCM there is inherent energy balance, and the voltage on C_B is independant of load. The converter is controlled by PWM. In [19] the need to operate L_2 in DCM is reinforced and design curves are presented.
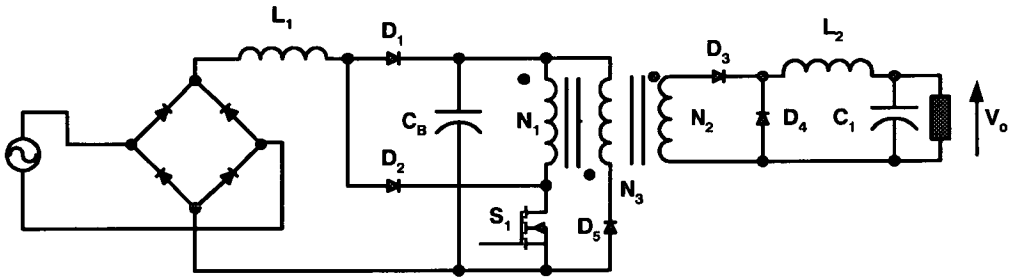
Figure 3.4: Single-stage isolated power-factor-corrected power supply(SSIPP)

Unfortunately it is undesirable to operate the output inductor L_2 in DCM for converters with high current outputs such as PC power supplies due to increased conduction losses and current stress in semiconductors: it is much preferred to operate the output inductor in CCM. In view of this there have been various attempts to overcome the problem of the high voltage on capacitor C_B when operating SSIPP converters with the output inductor in CCM. One approach has been to use voltage feedforward to vary the switching frequency as in [20]. PWM is still used to control the output voltage. The work in [20] is expanded in [21, 22] with the development of a control circuit and experimental results. The same group of authors also explore ways of making the SSIPP converter more efficient and in [23] on a DCM (L_2) version they implement a regenerative clamp to reduce voltage stress on the switching device due to leakage inductance and to increase efficiency. This is followed up by a CCM version in [24] where an active clamp and soft switching are implemented. Unfortunately in this paper the problem of the high voltage on C_B is not dealt with and is

still a problem. [25] adds synchronous rectifiers to the forward output on the secondary, to improve the overall efficiency.

[26] removes D_1 completely. The operation is the same as the SSIPP when S_1 is on, but when S_1 is off L_1 discharges its energy to C_B via the transformer primary N_1. [27] moves L_1 to the line side of the diode bridge rectifier. L_1 is operated in DCM mode and L_4 in CCM. [28] applies the SSIPP scheme to a soft-switched half bridge converter. In [29] the boost inductor is moved to the line side of the diode bridge and the switches are incorporated into the diode bridge. This scheme needs two primary windings. In [30] the input inductor L_1 is implemented as a flyback converter with the input current ramped up in the primary and delivered to C_B during the off time via the secondary winding of the flyback transformer.
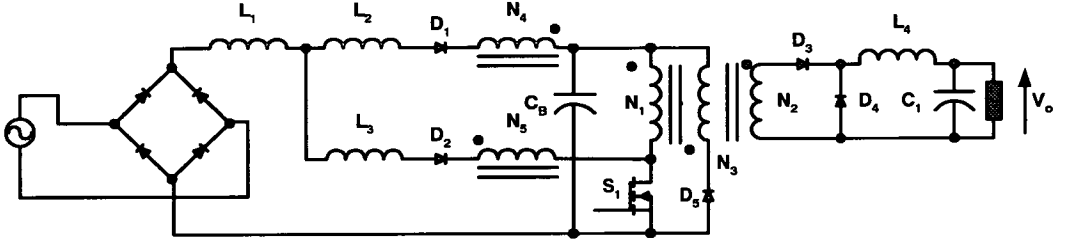
Figure 3.5: The SSIPP converter with possible topological variations

Further topological variations of the SSIPP have been proposed, most of which are some variation of the circuit shown in figure 3.5 (e.g. a topology may not have inductors L_2 and L_3). Most of the variations have been developed to allow L_4 and sometimes L_1 to operate in CCM without excessive voltage stress on C_B. Working with figure 3.5, the first of the many modifications to the basic SSIPP converter is presented in [31], with the addition of transformer winding N_5 connected between D_2 and S_1. The converter is operated with L_1 in DCM and L_2 in CCM. The additional winding N_5 has a positive voltage across it when switch S_1 is on, reducing the voltage across L_1 hence slowing down the current rise in L_1 and the amount of energy transferred to C_B during the off time. This scheme increases the distortion of the input current by introducing a dead time in the current during the zero crossing, but not enough to prevent the topology from meeting IEC 61000-3-2. It also prevents the voltage on C_B from rising above 450V enabling the converter to be used on the universal voltage range. A thorough analysis and design procedure for this scheme is presented in [32].

In [33] winding N_4 is also added to the converter. Winding N_4 comes into effect during the off period when the voltage induced across it during transformer reset is added to the voltage of C_B, causing current in L_1 to fall more quickly transferring less charge to C_B. This again helps to reduce the voltage on C_B and allow operation on the universal voltage range. The converter can be operated in the conventional manner with L_1 in DCM and L_2 can operate in CCM or DCM. As a further development this paper proposes the operation of L_1 in DCM near the zero crossing and in CCM when the input voltage is higher. CCM operation of L_1 will increase efficiency and again helps keep V_{CB} reasonable when L_2 is in CCM and the circuit is lightly loaded. [34, 35] extends the work in [33] by introducing a design optimisation. It also considers the effect of additional inductances L_2 and L_3 in series with both of the two extra windings. These inductances can either be transformer leakage inductances or external inductances. The topology is further altered, in [36], by incorporating windings N_4 and N_5 into the transformer primary where $(N_4 + N_5) < N_1$. This version still requires both diodes D_1 and D_2 and can operate with L_1 in CCM. The same paper also reduces D_1 and D_2 into one diode and feeding into a centre-tapped primary where $(N_4 + N_5) = N_1$, but this version can only operate with L_1 in DCM.

[37, 38] presents a variation with L_3 and N_5 added to the basic SSIPP converter. This scheme was developed from the concept of a loss-free resistor and a voltage source between the diode bridge and the bulk capacitor. The practical realisation is an input stage based on a forward converter output with an additional inductor to delay the turn off of the freewheel diode. The version mentioned here is a simplification of the loss free resistor scheme discussed in section 3.1.4. The input current is similar to that in [33] with L_1 being in CCM for most of the time. The voltage on C_B will still vary significantly with load when operating with the output inductor operating in CCM. To improve the current shaping performance when operating in the universal range, it is suggested that when operating on the 180V to 265V part of the range, the switching frequency be half that of when operating on the 90V to 130V part. Aspects of the design and operation are analysed in [39].

[40] comes up with a number of variations on the scheme, all operating L_1 and L_4 in CCM for most of the time. The first is a converter with just L_3 added with the current in L_1 operating in CCM, and then a design with just L_2 added to the basic SSIPP. The next modification is to feed the D_2 and L_3 branch into a centre-tapped primary winding (N_1) on the transformer. The centre-tapped version with L_3 is modified in [41] by the addition of a

low frequency switch across diode D_2 and the bottom half of the primary winding directly to switch S_1. The low frequency switch is turned on during the zero crossing periods. The scheme is also shown working on the version discussed in [31] where the switch is placed across N_5 and D_2. The low frequency switch is used to improve the current shape by allowing conduction of L_1 right up to the zero crossing which was lost (conduction of L_1 up to the zero crossings) in [31] and subsequent papers. Another method to remove the dead angle where L_1 does not conduct when operating L_1 in CCM is proposed in [42] where inductor L_2 and N_5 are fitted, and L_2 is coupled to L_1. The winding N_4 is moved to the L_1 side of the D_2 branch in [43] (L_1, L_2, L_3 and N_5 are not fitted). This reduces the major magnetic components onto one core. A small inductor is added to soft-switch diodes D_1 and D_2. Both the input and output inductors can be operated in CCM with reasonable voltage on the bulk capacitor C_B.
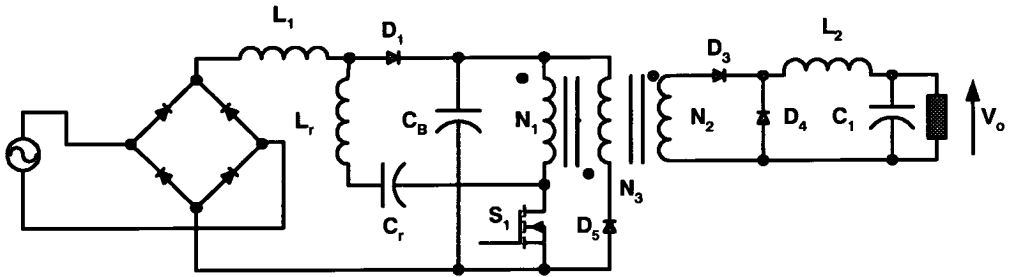
Figure 3.6: SSIPP converter with resonance based variations

Instead of using diodes, inductors and transformer windings to improve the SSIPP converter another method is to use resonant methods as shown in the circuit in figure 3.6 [40]. Another resonant version [44] uses the charge pump concept. The SSIPP version is shown in [45, 46] where L_r is not fitted. [45, 46] modifies the circuit with the addition of an extra diode and capacitor. Half bridge versions are shown in [47, 48]. This topology is mainly for use as a fluoresent lamp ballast. [49, 50] proposes a LC resonant half-bridge converter also based on electronic ballasts with PFC.

3.1.4 Two Terminal SSIPP

The topologies discussed so far have what is known as a three terminal ICS (Input Current Shaping) cell [51]. The branch connected in series with S_1 (the branch with D_2 on it in

figure 3.5) is the charging branch for L_1 and the branch connected to C_B (the branch with D_1 on it) is the discharging branch for L_1. There is another type known as a two terminal ICS cell where the charging and discharging paths are in parallel with each other between L_1 and C_B. In [51] rules are developed to convert between ICS cell types.

The magnetic-switch power supply [52] shown in figure 3.7 uses the transformer winding N_4 on the input to control the current in L_1. L_1 is operated in DCM and L_2 in CCM. When S_1 is on the voltage on N_4 is positive (dot notation) and adds onto the input voltage, causing the current in L_1 to ramp up. When S_1 turns off the voltage on N_4 reverses causing the current in L_1 to fall. In [53] a soft switching scheme is added. A similar layout is developed in [54], but with quite a different operating sequence where the current in L_1 is ramped up and down during the off period of S_1.
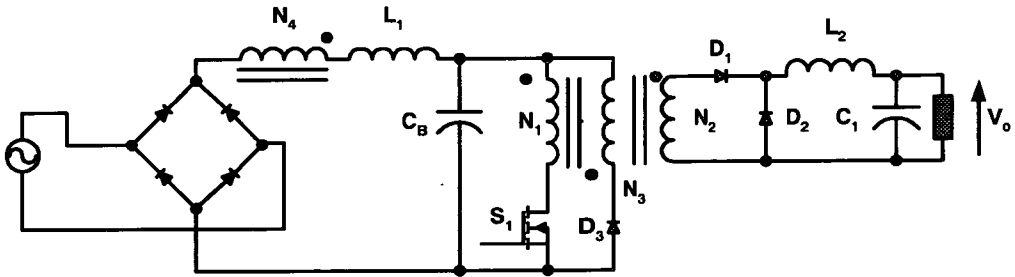
Figure 3.7: Magnetic-switch power supply
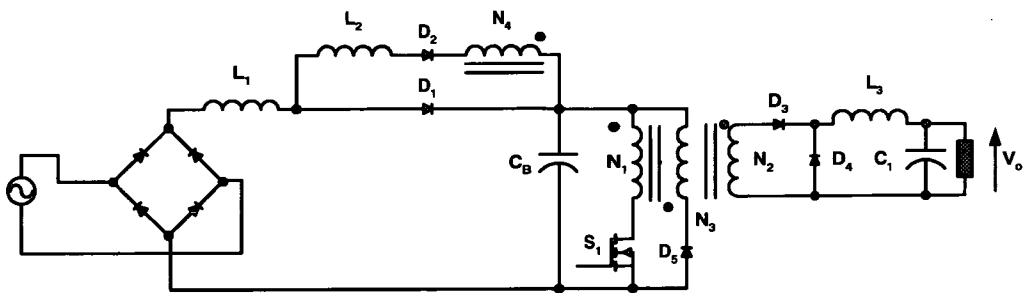
Figure 3.8: Loss free resistor and voltage source PFC converter

The first converter to have the arrangement shown in figure 3.8, in [55], does not have inductor L_2. Without this inductor the input current shaping circuit is a forward style output placed on the input current path. The current in L_1 is designed to be in DCM so that it will draw a sinusiodal shape automatically with steady state PWM. The output inductor L_3 is operating in CCM, so to keep the voltage of C_B reasonable variable frequency control is

also used applying a voltage feedforward signal. Futher work in [56, 57] operates L_2 in DCM and without variable frequency control, so the voltage on C_B is not a problem, but the converter in this paper has a high voltage (54V) low current (3A) output whereas [55] was a 5V 10A output.

The complete configuration shown in figure 3.8 is introduced in [37, 38] and uses the concept of a loss free resistor and a voltage source between the diode bridge and the bulk capacitor. As mentioned earlier the practical realisation is an input stage based on a forward converter output with an additional inductor to delay the turn off of the freewheel diode. The input current is similar to that in [33] being in CCM for most of the time. [58] compares several designs of the basic converter. [59] implements the current shaping scheme on a complementary controlled half bridge with synchronous rectifiers on the output rectifier. In [60, 61] the scheme is implemented on a non-isolated buck converter. In [62, 63] the steady state analysis is carried out on a variety of topologies with the current shaper on the front end; these are the flyback, forward, SEPIC, Cuk, half-bridge, full-bridge, push-pull buck, boost and buck-boost converters. [64] alters the the input current shaping circuit to operate with converters with symmetrically driven transformers such as the full bridge and half bridge. [65] adds synchronous rectifiers to the output of [64]. In [66] the design principles developed in earlier papers are re-appraised with the introduction of the 2000 amendment to IEC 61000-3-2 where PCs and TVs need only comply with class D, and the removal of the class D shape. In [67] the D_2 branch in figure 3.8 is moved so that it is connected across the diode bridge on the DC side, and diode D_1 is removed.

The circuits discussed so far can be based on most DC/DC topologies such as the forward converter shown in the figures or using the flyback converter. In [68] an interleaved version of the SSIPP is introduced. This topology, shown in figure 3.9, requires a symetrically driven transformer so is constucted from a half-bridge converter. The two inductors L_1 and L_2 are both operated in DCM but are 180° out of phase due to the opposite wound windings N_1 and N_2 ($N_1 = N_2$), but due to the interleaving the input current seems continuous.

[69, 70, 71, 72] presents the SSIPP type converter shown in figure 3.10. The power switch of the converter has been moved to the boost position and and the primary of the transformer has been split into two parallel primaries. The new transformer capacitor arrangement removes the voltage spike caused by the leakage inductance of the transformer. Both L_1 and flyback transformer inductors N_{1A}, N_{1B} and N_2 are operated in DCM so voltage on the
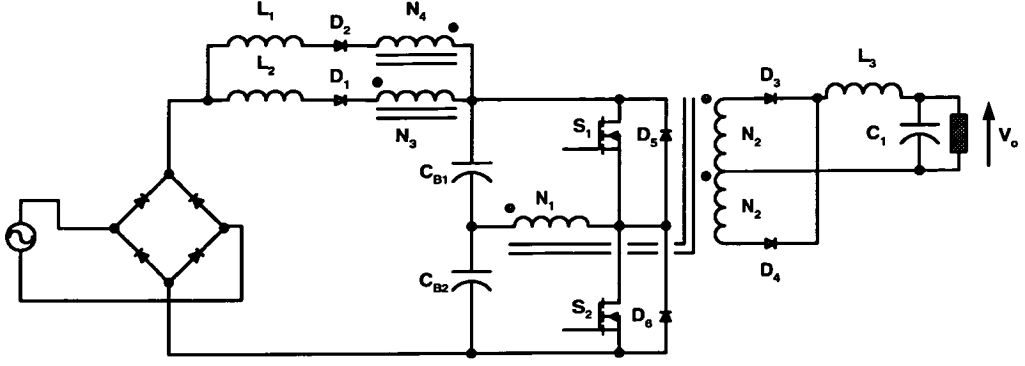
Figure 3.9: DCM interleaved SSIPP converter

two capacitors C_{B1} and C_{B2} is not a problem. The inductors L_{2A} and L_{2B} are replaced by diodes in [73]. Another topology is generated in [74, 75] by the combination of a boost PFC cell and an aysmmetrical half-bridge.
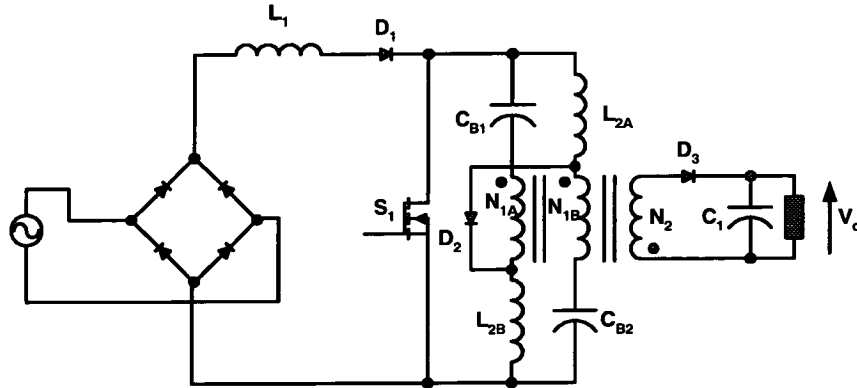
Figure 3.10: Double primary Winding SSIPP converter

3.2 Parallel PFC Converters

The concept of parallel PFC was introduced by Jiang [76] in 1993. The scheme proposed is shown in figure 3.11. Conversion stage 1 delivers 68% of the total output power and stage 2 the remaining 32%. Figure 3.12 shows the power waveforms for a line period. Ideally input power $P_{O.PFP}$ is a $\sin^2$ function, and output power P_{OUT} is a constant power. As can be seen $P_{O.PFP}$ can be anything between 0 and twice P_{OUT}, hence $P_{O.PFP}$ cannot be delivered directly to P_{OUT} all the time. When $P_{O.PFP}$ is greater than P_{OUT} (assuming

efficiency of 100%) the output is supplied directly by the stage 1 converter and the excess input power, P_{STO}, is sent to the energy storage element, bulk capacitor C_B. When $P_{O.PFP}$ falls below P_{OUT} then C_B releases its stored energy to the load via stage 2, P_{AUX}, to maintain P_{OUT} constant. It is believed that since 68% of the power is delivered directly to the load this method is more efficient than the two stage approach. In [76] Jiang feels this method is more suitable for high power and shows a practical realisation based on a boost full-bridge.
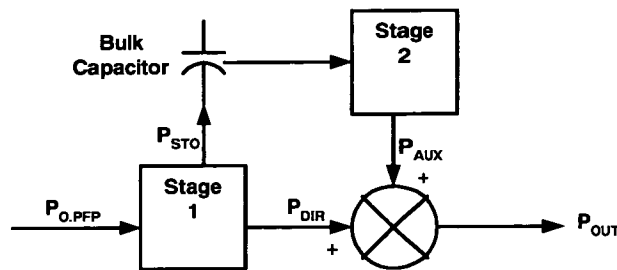
Figure 3.11: Parallel PFC power flow
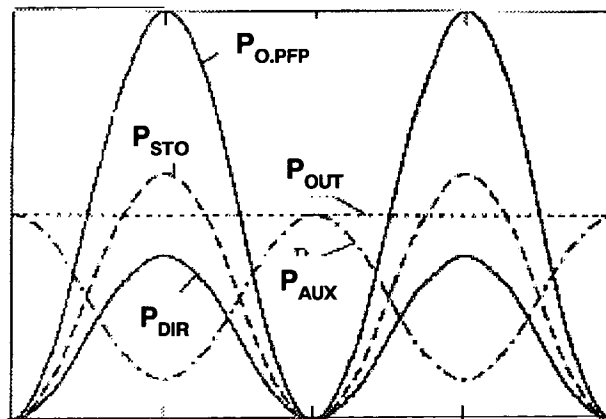
Figure 3.12: Powerflow in a line period [3]

The concept is developed further in [77] with a change to how the power is processed. The improved scheme is shown in figure 3.13. The main difference to that of [76] is that there is only one power stage. The single power stage processes all the power at least once with about 68% going directly to P_O and the remainder stored on C_B. When P_{IN} falls below P_O the same stage reprocesses the energy from C_B to keep P_O constant. This improved scheme produces a simpler converter topology. It is implemented as a flyback converter with two extra switches and a boost converter.

33
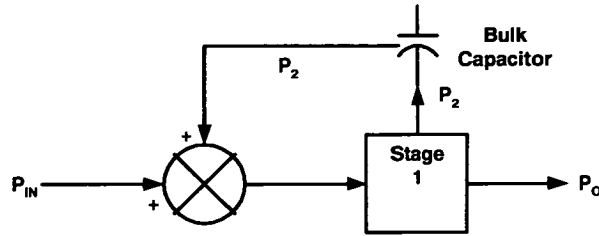
Figure 3.13: Parallel PFC with altered power flow

[78] presents a topology based on a flyback converter with a transformer with two secondary windings for the output. When input power is higher than the output power the excess power is stored in the capacitive element of the second output, and when input power is lower than the output power the deficiency is made up by taking power from that capacitor. [79] introduces, with subsequent work presented in [80, 81], a parallel PFC topology based on the forward converter operated in DCM. The converter makes use of the magnetising energy of the transformer to reduce the output voltage ripple at 100/120Hz. Instead of a reset winding on the primary the converter has a second secondary winding for the output based on the flyback output. Following this output is a second switch which is used to compensate the output voltage ripple.

In [82] both parts of the converter (the main converter and the auxiliary converter) are moved to the primary side of the converter. The topology consists of a buck-boost converter which supplies energy to a storage capacitor (when the input voltage is high enough). This is followed by a forward converter which is fed by the mains connected in series with the storage capacitor, so even during the mains zero crossing there will be an input supply for the forward converter. [83] has two flyback converters in parallel both supplying power to the output (about 1/2 each). The first is fed from the bulk capacitor and its prime function is to regulate the output voltage. The second performs the PFC function and regulates the voltage on the bulk capacitor. [84] presents a converter with a flyback converter with two output diodes, one supplying the load and the other an auxiliary boost converter on the secondary side of the transformer.

34

3.2.1 Parallel Single-Stage PFC using Pre-Regulator with Two Output Capacitors and Auxiliary DC/DC Converter

Another family of parallel PFC topologies is introduced by Garcia in [3]. The scheme is shown in figure 3.14. The first module is the power factor correction circuit which has two capacitors C_1 and C_2 in series on its output. Capacitor C_1 is the output capacitor and is in parallel with the load. Capacitor C_2 is the main energy storage element and is in series with the load (C_1 is floating so the voltage across C_1 and the load is constant, but C_1 and the load will be sitting on the ripple). A second stage or auxiliary module is supplied with C_2 as its input and supplies the load as well. A low frequency ripple (100/120Hz) will appear across C_2. The basic power management is the same as in [77], where the main module has to process all the power, P_O with about 1/2, P_{DIR}, going to the load and the rest, P_{STO}, being stored in C_B. The auxiliary module will supply the additional load power, P_{AUX}, that the main module is unable to supply, and provides fast regulation of the output voltage. $P_{OUT} = P_{AUX} + P_{DIR}$. Each module has its own control circuit, with the main module including isolation if required. The main module can be almost any converter, a PFC converter such as a boost or flyback or even a forward. The auxiliary module has a requirement that the negative input terminal will be connected to the positive output terminal or vice versa. This limits the choice of converter to buck-boost, cuk or an isolated topology. The input current waveform is almost sinusoidal.
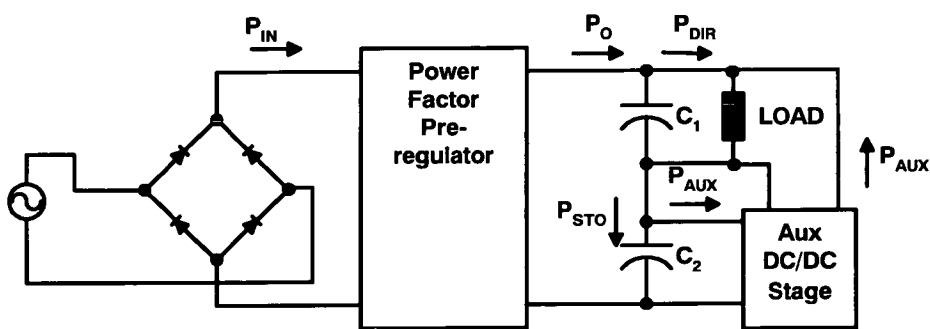
Figure 3.14: Parallel single-stage PFC using pre-regulator with two output capacitors and auxilary DC/DC converter

In [85] the concept is reapplied to a low output voltage (3.3V) power supply using synchronous rectifiers.

The concept is slightly modified in [86] with a slight change to the configuration of C_1 and
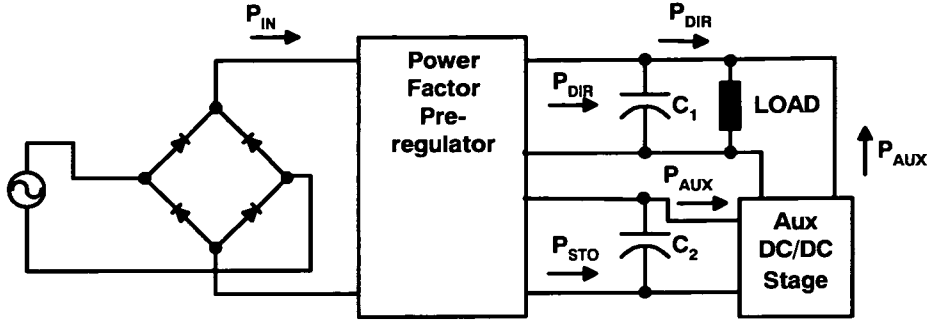
Figure 3.15: Parallel single-stage PFC using pre-regulator with two output capacitors, with different connection, and auxilary DC/DC converter

C_2 as shown in figure 3.15. The advantage of this new configuration is that the voltage on C_2 becomes a degree of freedom and can be designed to improve aspects of performance such as hold up time or efficiency. To implement this method the main module has to have two windings on the transformer for each output if it has an LC filter output stage, or if using a flyback then two transformers in parallel. The main module should work in DCM. The auxiliary module can be any converter operating in DCM or CCM. Both modules are again individually controlled. The input current is nearly sinusoidal.

[87] takes the first version of the scheme in figure 3.14 and implements it using a single control stage driving both modules with the same gate signal. This reduces the component count. The scheme is implemented with a flyback as the main module and a buck-boost as the auxiliary module [87]. The main module should operate in DCM and the auxiliary module in DCM or CCM. When operating with the auxiliary module in CCM the voltage on C_2 becomes load dependant and at light load and high line it becomes very high (as with the series circuits). When operating with both modules in DCM the distortion of the input current is dependant on the voltage on C_2, V_{C2}, and the harmonics decrease as the input voltage, v_{IN}, increases. The input current is no longer sinusoidal. The voltage on C_2 limits operation on the universal voltage input range.

[88] considers both versions of the scheme and applies a single control stage to both versions. To improve energy management a trade-off between input current harmonics and the percentage of power processed once is made (ie increase power delivered directly to above 50% as it is in the previous papers) up to a maximum of 70% when working with both modules in DCM. When operating with the auxiliary module in CCM P_{DIR} can only be 50%.

36

In [89] another variation is proposed where a forward type output is placed at the input of the auxiliary module. The main module is a converter that has an inductor at its input such as a boost or flyback. The auxiliary module can be any topology. The inductive front end and the inductor in the forward stage change the way the scheme takes energy from the supply. Different control methods are investigated to see their effect on the input current, but no prototype circuits were presented.

3.2.2 Single Switch Parallel PFC Topologies

Bi-Flyback and Bi-Forward
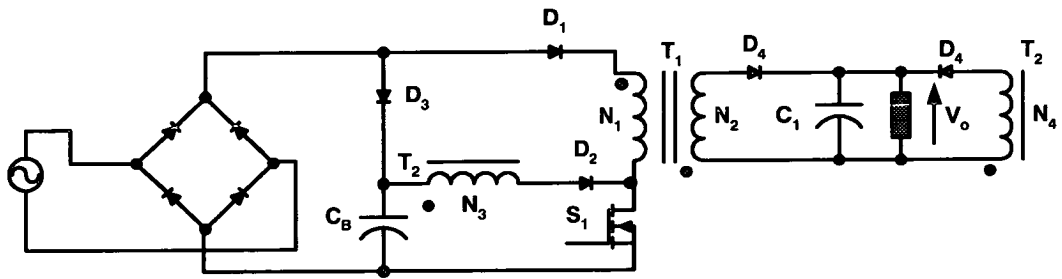
Figure 3.16: Bi-Flyback converter
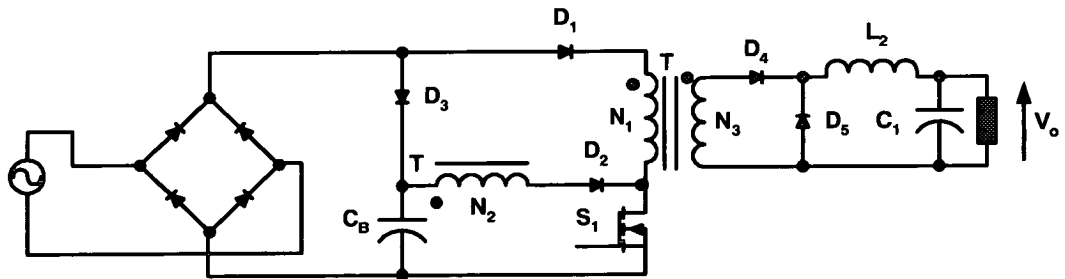
Figure 3.17: Bi-Forward converter with single transformer

The bi-flyback converter was proposed in [90] and is shown in figure 3.16. The output is fed directly from the line and from C_B. When S_1 is turned on the current in N_1 and N_3 ramps up. When S_1 turns off the energy is delivered to the load from both transformers. The ratios of the transformers determine how much of the output power it transfers. It should be designed so that most of the power goes via N_1 and N_2 so that as much power as possible is processed once. A good feature of this converter is that the capacitor C_B is peak charged

and hence the voltage on it does not rise above the peak of the line, even when operating in CCM. The current wavefrom (similar waveform to that shown in figure 4.3) is far from ideal and the authors only design the converter to meet the class A part of IEC 61000-3-2. In [91] the idea is extended to the forward converter and design curves are presented. [92] evalutes the different conduction modes that the two transformers in the bi-flyback can work in (any combination except both in CCM) and their effect on the line current. The bi-forward converter has the transformer integrated into single device as shown in figure 3.17. Doing this changes the way the converter operates. Now N_1 is the primary when the input voltage is high. When the input voltage falls during the zero crossings N_2 becomes the primary winding. The point when N_2 takes over the power transfer is determined by the turns ratio. Again the converter is only designed to meet class A. In [93] design curves and guidelines are developed for the version in figure 3.17 of the bi-forward. [94] uses the bi-flyback as a small AC/DC adapter. In [95] the final version is shown to be just able to meet the class D regulation. The authors suggest the addition of the inductor L_1 in figure 3.18. The transformer is also converted to be centre-tapped to reduce the number of windings. The addition of L_1 improves the current shaping ability and the topology is able to meet class D with ease.
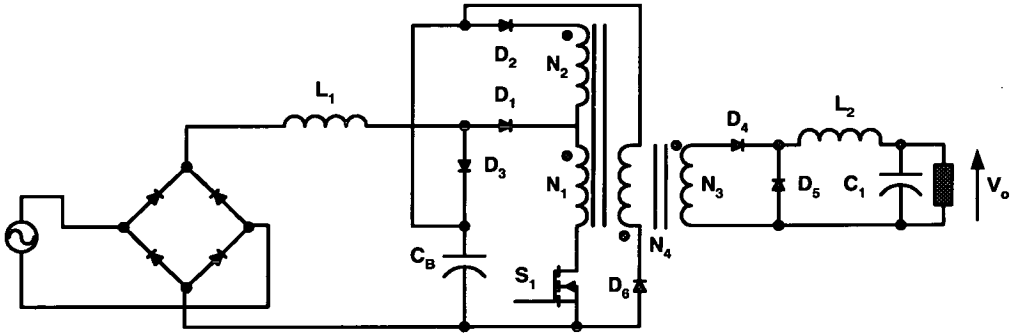
Figure 3.18: Bi-Forward converter with centre tapped primary winding and boost type input inductor

Bi-Flyback 2: A Different Topology with the same Name

Another topology which integrates two flyback converters operating in DCM into a topology with one switch is presented in [96], and the basic topology is shown in figure 3.19. A similar topology is presented in [97] which was developed from the BIFRED. The input
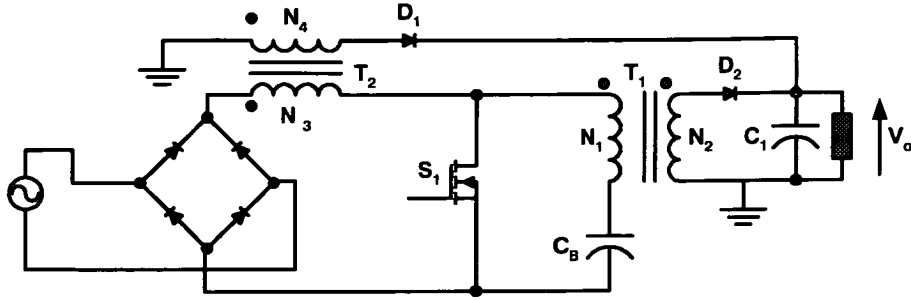
Figure 3.19: The other bi-flyback converter

flyback transformer T_2 is operated under DCM and the output flyback transformer T_1 in CCM. When the input voltage is low (during the zero crossing) both transformers operate as flyback converters, both supplying the output. When the input voltage is high the transformer T_1 still operates as a flyback and supplies all the power to the output. The other transformer T_2 operates as a boost inductor (N_4 is not used). The converter is operating in a similar manner to the BIFRED during this period. [98] implements the converter with an active clamp with a modified control scheme. [99] applies the PFC scheme to the asymetrical half bridge. [100] applies the scheme to the converter proposed in [73], and in [101] additional boost inductance is added in series with N_1 and a lossless snubber is added to the basic topology. [102] converts the input PFC cell (transformer T_2) into a "flyboost" with the addition of a diode in series with N_1. The operating principle is very much the same as the topology in [97]. A converter with similar operating principles but based on a flyback current fed push-pull converter is introduced in [103], where the converter operates in boost mode during the zero crossings of the input voltage and buck mode when the input voltage is high.

3.3 Operation of Conventional Converters as Single-Stage PFC Converters

Another method of achieving single-stage PFC is to use an existing converter, but operate it so that it carries out both current shaping and output voltage control. Topologies suitable for this are ones that have an inductor on the front end such as the boost, flyback and Cuk converters. The Cuk converter in [104] is operated with DCM inductors and with normal

39

voltage feedback, hence the Cuk converter automatically draws almost sinusoidal current. The converter also features integrated magnetics. [105] uses coupled inductor SEPIC and Cuk converters with non-linear charge carrier control as single-stage PFC circuits, and [106] presents a PFC SEPIC converter with multiple outputs. In [107] a flyback converter using charge control is presented as being able to operate as a PFC converter while operating in CCM. A digital control scheme for a PFC flyback converter is presented in [108]. In [109] an active clamp flyback converter for PFC in distributed power systems is presented. The Sheppard-Taylor topology (which can be considered as a modified boost and a buck converter sharing the same switch) is used as a single stage PFC topology in [110]. [111] uses quasi-resonant flyback converters for PFC. The converter can be operated with the input inductor in DCM and the output inductor in CCM using PWM, or with the input inductor operating in CCM and the output inductor operating in DCM using frequency modulation to control the output voltage. When operated in the latter case the input current suffers negligible distortion. In [112] a class D series resonant half bridge converter with fixed frequency with close to unity power factor is presented. In [113] discontinuous capacitor voltage mode converters for single stage PFC are presented. The discontinuous capacitor voltage mode converters are derived from the conventional DCM buck, buck-boost and boost converters. Unfortunately they do not build any of the converters presented. [114] applies the principle to a flyback converter, but with experimental results. In [115] isolated capacitive idling converters operating in DCM for PFC are presented. The capacitive idling converters shown are based on the flyback, Cuk, SEPIC and inverse SEPIC. In [116] a SEPIC capacitive idling converter operating in CCM and an auxiliary switch network is developed. A new current shaping technique in CCM is shown in [117] using inductor voltage sensing in the isolated Cuk, SEPIC and flyback converters.

3.4   Selection of the Most Promising Topologies

Keeping in mind that the topologies selected are to be considered as being used as PC power supplies, they will need to be simple and cost effective. Since there are two broad families (the series power delivery and parallel power delivery) of single stage converters then the most promising from each family is selected for further study.

Most of the parallel based topologies with more than one converter are not suitable for the

application of PC power supply. As most of the auxiliary converters are on the secondary of the transformer and a PC power supply has multiple secondaries this option will be expensive due to a large increase in components. Also complexity is increased. The second bi-flyback was unfortunately proposed too late to be considered for study, but may still suffer from the same variable voltage on the bulk capacitor as the BIFRED does. The one converter that stands out in this group is the bi-forward shown in figures 3.17. The bi-forward does not suffer from load dependant voltage stress when the output is operating in CCM as the series PFC circuits do. The basic converter has a simple operation, only requiring the addition of an extra transformer winding and three diodes on the basic forward converter. It should also have no problems with multiple outputs. Even though the topology is only designed to meet class A in [92] it may be possible to redesign it for class D. If that is not possible the addition of inductor L_1 in figure 3.18 can be implemented with little detrimentral effect (it is claimed that adding L_1 in [95] will not cause the voltage on the bulk capacitor to change appreciably).

From the series PFC topologies it was decided to study the topology in figure 3.8 introduced in [37]. This topology is considered promising as it operates with the output inductor in CCM, but also as the input inductor operates in CCM for some of the time input filtering requirements are reduced. Also it was considered that this topology deals with the bulk capacitor voltage problem to a reasonable extent, allowing the use of the converter on the universal voltage range. Most of the other options do not deal with the voltage on the bulk capacitor satisfactorily. It is undesirable to operate with a variable frequency due to increased complexity or to operate the output inductor in DCM since the output currents are quite high. Other topologies were considered to be too complicated for this application.

41

Chapter 4

Bi-Forward Converter

4.1 Introduction

The simplest version of the bi-forward is presented in [92] and [93]. This version has a single transformer core wound with two primary windings as shown in figure 4.1. The converter can be made more compact by integrating the two primary windings into one with a centre tap as shown in figure 4.2. This version was presented in [95]. Converting the primary windings into a single winding with a centre tap does not change the basic operation of the converter. In the centre tapped version $N_{1A} + N_{1B}$ is equal to N_{1A} of the the version in figure 4.1.
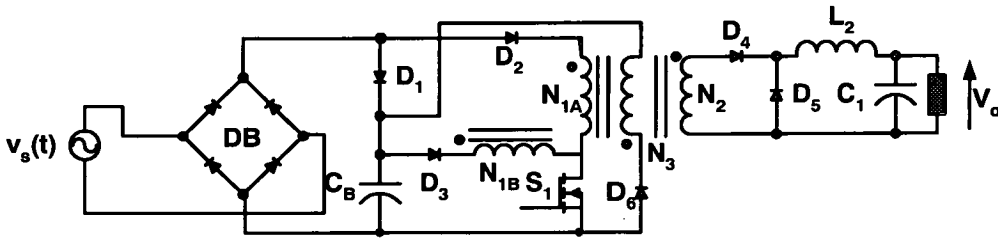
Figure 4.1: Bi-Forward converter with two primary windings

The original bi-forward and bi-flyback presented in [92] were only designed to pass the class A part of IEC 61000-3-2. The version with the centre tapped transformer in [95] is claimed to pass the class D regulations at low line with only a 60W output. These statements indicate that the basic converter will find it very difficult to pass the class D regulations, but

42
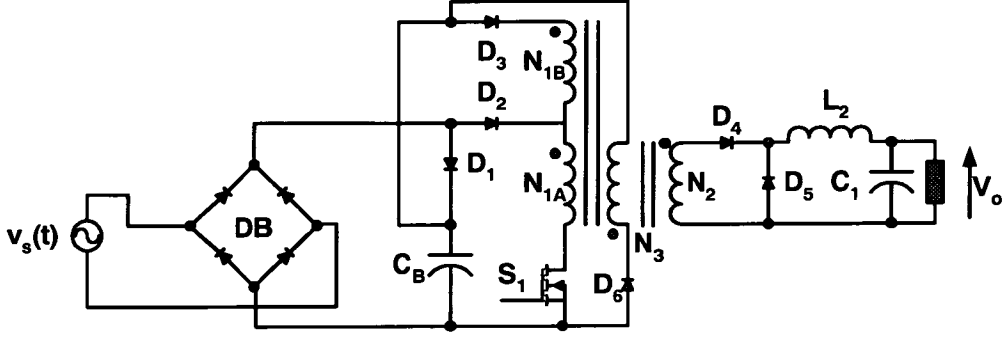
Figure 4.2: Bi-Forward converter with centre-tapped primary winding

not necessarily impossible. If the basic bi-forward is shown to be unable to meet class D regulations then it can be modified along the lines in [95] with the addition of an inductor placed between the diode bridge and the $D_1 D_2$ junction. The main reason that makes this topology worth investigating is that the bulk capacitor voltage is independent of the load, normally being charged to the peak of the mains input.

4.2 Operation

The converter operation of the circuit in figure 4.2 is simple; the output is supplied either from C_B via $N_{1A} + N_{1B}$ when the input voltage is low or from the input voltage source $v_s(t)$ via N_{1A} when the input voltage is high. The bi-forward operates in the same fashion as an ordinary forward converter, which is either being fed from C_B or $v_s(t)$ depending on the line voltage level. When operating from $v_s(t)$ the duty cycle has to alter to keep V_o constant as $v_s(t)$ changes. The bulk capacitor is recharged by peak charging.

The change over between feeding the output from C_B to $v_s(t)$ or vice versa is controlled by the primary of the transformer. When operating from $v_s(t)$ the instantaneous voltage of $v_s(t)$ is applied across N_{1A} when S_1 is turned on. A voltage is thus induced in winding N_{1B}; if the voltage across $N_{1A} + N_{1B}$ is higher than the bulk capacitor voltage then diode D_3 is reverse biassed and the output is still supplied from $v_s(t)$ via D_2. If the voltage across $N_{1A} + N_{1B}$ is lower than V_B then the output is supplied from C_B. When C_B is supplying the load the voltage across N_{1A} will be higher than the input voltage $v_s(t)$, reverse biassing D_2. The diode D_1 only conducts during bulk capacitor recharge, and is there to disconnect C_B from N_{1A} and prevent it from supplying the load via N_{1A} instead of $v_s(t)$. The typical

43

input current waveform is shown in figure 4.3.
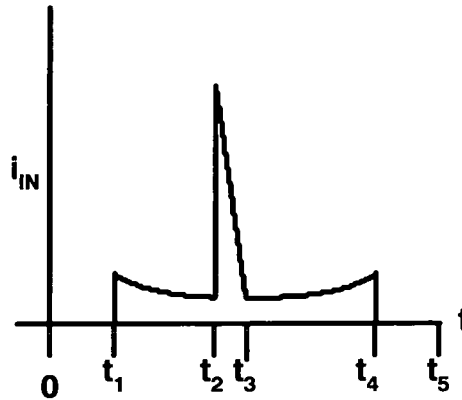
Figure 4.3: Typical input current waveform for a half line period showing the conduction periods

4.3 Analysis And Design

The main parameter in the design of a basic bi-forward converter is the turns ratio between N_{1A} and N_{1B}. This turns ratio has several important effects:

1. It determines the conduction angle of the input current (length of time $v_s(t)$ supplies the output directly).

2. Following on from the conduction angle, the turns ratio also determines the conduction angle of C_B. If the mains conduction angle is long then the bulk capacitor has to supply the output for a short time and the recharging current is low and vice versa.

3. It determines the current and voltage stress across S_1.

Points 1 and 2 affect the level of the input current harmonics which must meet the regulations, but point 3 should not be neglected.

To examine the bi-forward converter, a test circuit was designed and built.

44

4.3.1 Specification

The specification for the test circuit is a simplified representation of a PC power supply specification and is outlined below;

- Operate from 90 - 130V_{RMS} and 180 - 265V_{RMS} at 47 - 63Hz

- Output power of 0 - 148W at 5V, 0 - 20A and 12V, 0 - 4A

- Efficiency of over 65%

- Meet IEC 61000 -3-2 Class D and A at 100V_{RMS} and 230V_{RMS} at 50Hz

- Switching frequency of about 100kHz

The bi-forward is loosely based on a 150W forward converter PC power supply designed and manufactured by Minebea Electronics (UK) Ltd. The bi-forward does not have a voltage doubler front end (a scheme was later suggested in [95] after the converter was built) so the converter must be designed to operate from 90V_{RMS} to 265V_{RMS} as a single range.

4.3.2 Assumptions

The following assumptions were made during the analysis and design of the bi-forward and are also used in chapters 5, 6 and 7:

1. Switching frequency is 100kHz.

2. Semiconductors are ideal. That is, they have zero voltage drop and resistance when conducting, infinite resistance when off and instantaneous switching transitions.

3. Magnetising inductance is infinite so magnetising current is zero and leakage inductance is zero.

4. All inductances, capacitances and resistances are ideal with no parasitic elements .

4.3.3 Analysis

All the analysis and design calculations were carried out using MathCad 2000. The analysis carried out follows that presented in [92, 93], so most of it is not presented.

The input voltage is defined as:

$$v_s(t) = V_{pk} \cdot \sin(\omega \cdot t) \tag{4.1}$$

and the turns ratio between N_{1A} and $N_{1A} + N_{1B}$ is defined as:

$$n = \frac{N_{1A} + N_{1B}}{N_{1A}} \tag{4.2}$$

If power, P_o, is supplied, then the energy lost (E_c) by C_B supplying the load during the zero crossings is:

$$E_c = P_o \cdot (2 \cdot t_1) \tag{4.3}$$

where t_1 is the time from the start or stop of conduction to the zero crossing point.

Considering the energy loss across C_B in equation 4.4, the voltage C_B falls to (V_{min}) can be found.

$$E_c = \frac{1}{2} \cdot C_B \cdot \left(V_{pk}^2 - V_{min}^2 \right) \tag{4.4}$$

The recharge current for C_B is:

$$i_c(t) = C_B \cdot \frac{dv_s}{dt} = C_B \cdot V_{pk} \cdot \omega \cdot \cos(\omega \cdot t) \tag{4.5}$$

The recharging of C_B starts when $v_s(t) = V_{min}$ which gives a recharge start time of t_r (equation 4.6) after the zero crossing of the input voltage. C_B has been chosen to be 165μF formed from two 330μF capacitors in series. This value was chosen since it is the com-

46

bination being used in the 150W power supply produced by Minebea. When the design procedure was started C_B was initially chosen to be 470μF, but this is large and expensive hence the change to 165μF. The implications of this change are mentioned in section 4.4.1.

$$t_r = \frac{\sin^{-1}\left(\frac{V_{min}}{V_{pk}}\right)}{\omega} \tag{4.6}$$

The input current waveform can now be constructed. The current, $i_{dir}(t)$, supplied directly to the output from the input can be considered as:

$$i_{dir}(t) = \frac{P_o}{v_s(t)} \tag{4.7}$$

Using figure 4.3 the input current, $i_s(t)$, for a half period of the input voltage can be considered as:

$$i_s(t) = \begin{array}{ll} 0 & 0 < t < t_1 \quad t_4 < t < t_5 \\ i_{dir}(t) & t_1 < t < t_2 \quad t_3 < t < t_4 \\ i_{dir}(t) + i_c(t) & t_2 < t < t_3 \end{array} \tag{4.8}$$

If the bi-forward is built with a tertiary transformer reset winding then N_3 has to at most, equal N_{1A} to ensure that the transformer will reset during the S_1 off time. The reset winding can only be placed across C_B, thus during transformer reset the voltage seen across S_1, V_{S1}, is:

$$V_{S1} = V_B + \frac{N_{1A} + N_{1B}}{N_3} \cdot V_B \tag{4.9}$$

Since $N_3 = N_{1A}$, then

$$V_{S1} = V_B + n \cdot V_B \tag{4.10}$$

When operating from 265V$_{RMS}$ the peak voltage on C_B is 375V. S_1 is realized as a MOS-FET (normal practise in current PC power supplies), and MOSFETs are only produced up to a maximum voltage of 1500V. At this voltage the devices are expensive and the range

47

limited. 1200V devices are also manufactured and are slightly more common. It is thus desirable that the voltage on S_1 should be kept below 1200V. From equation 4.10, n has to be kept below $n_{max} = 2.2$ to be able to build a prototype. n was chosen as 2, 1.3, 1.57 and 1.16 so that design curves could be plotted.

The rms harmonic currents of the input current can be found from the Fourier series for $i_s(t)$.
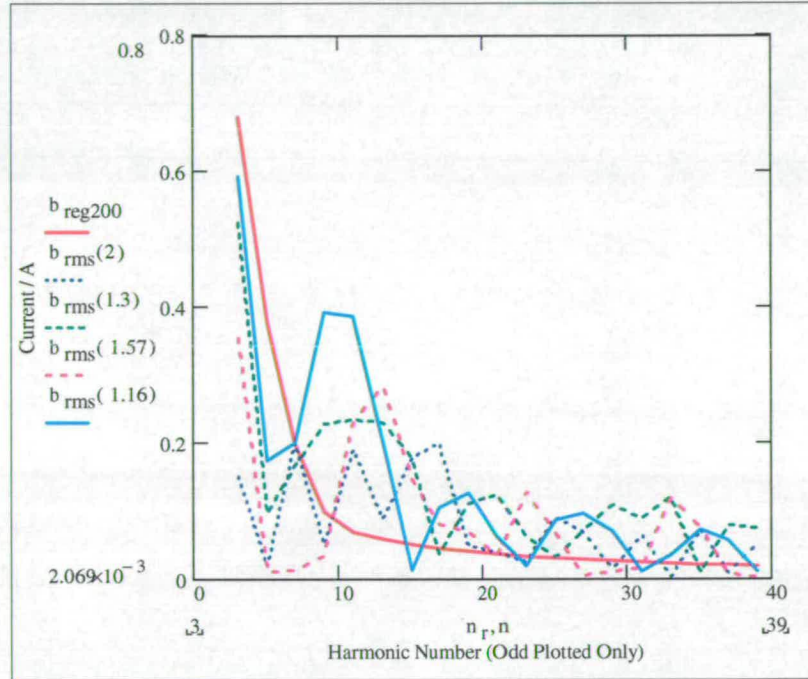
Figure 4.4: RMS input current harmonics compared to class D (b_{reg200} curve) for 230V input with an input power of 200W with n as 2, 1.3, 1.57 and 1.16. Traces are listed by side of graph.

Shown in figures 4.4 and A.1 (in appendix A as both the plots look similar) are the harmonic plots at 200W (assuming about 70% efficiency) input power at 230V and 100V compared to the class D regulation values. Figures 4.4 and A.1 show that all four of the design curves are exceeding the class D limits at 200W at both 100V and 230V for a large number of the odd harmonics. Similar curves produced for 75W input power show a similar behaviour. Figures 4.5 and A.2 (in appendix A) show plots for harmonic levels to class A at 230V and 100V, but only at full expected input power. At 100V in figure A.2 all the design curves are below the regulation values. For 230V in figure 4.5 the design curves are very close to the class A limit, but they are still just exceeding it, but are close enough to possibly pass in practice. The effect of the value of C_B on the input current harmonics is shown in appendix
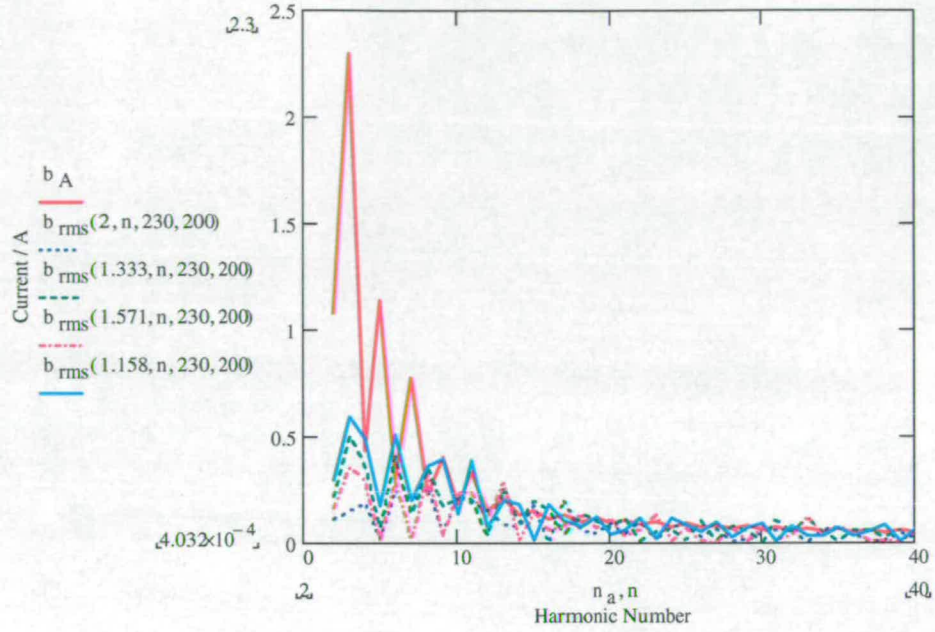
Figure 4.5: RMS input current compared to class A (curve b_A) for 230V input with an input power of 200W with n as 2, 1.3, 1.57 and 1.16. Traces are listed by side of graph: 1st value is n, 2nd value is the input voltage and 3rd value is the power.

B.

From figures 4.5 and A.2 values of n around 2 seem to produce realisable designs which has the best chance to meet class A. The 8th, 10th, 12th, 15th, 17th, 20th, 22nd, 32th, 34th, 35th are the harmonics it fails on at 230V. The even harmonics are expected to be low (see the simulation results in section 4.4.1). Thus $N_{1A} = N_{1B}$ appears to be the best design to pursue. It would appear to be impossible to meet class D with any value of n. Even though it is shown in figure 4.5 that some harmonics are just exceeding the limits, it is likely that in a prototype converter that they could meet the class A regulation as the current shape will not be as sharp as shown in figure 4.3.

Design of Transformer Turns and Output Filter

It was decided to use the same output filter design for the bi-forward as is used in a Minebea 150W supply. That is

$L_{2:5V}$		$15.4\mu\text{H}$
$L_{2:12V}$		$64\mu\text{H}$
$C_{1:5V}$	$2200\mu\text{F}$ (changed from $1800\mu\text{F}$ as this is rare part to find)	
$C_{1:12V}$		$470\mu\text{F}$

Since the transformer for the bi-forward has a different structure to a conventional forward converter transformer it was decided to design a completely new one. When the converter is supplying the output directly from the mains the minimum voltage across N_{1A} is 63.5V when $n = 2$, and when the converter is operating from C_B via $N_{1A} + N_{1B}$ the minimum voltage is 86V. When the converter is operating from 265V_{RMS} the maximum voltage across $N_{1A} + N_{1B}$ or N_{1A} is only 375V. Considering this, $N_{1A} + N_{1B}$ was chosen to be 44 turns, with N_{1A} and N_3 as 22 turns for $n = 2$. The number of secondary turns were chosen to be 5 turns on the 5V output and 11 turns on the 12V output, which are just large enough to ensure that the secondary transformer voltage would be high enough to still produce the desired output voltages when running from C_B at 127V with the existing output LC filters. The transformer was designed and built for the case where C_B is $470\mu\text{F}$ and the drop in voltage is only to about 100V. When C_B was changed to $165\mu\text{F}$ the voltage dropped to 86V. This late design change is shown later to cause a slight problem with a loss of output voltage regulation at 90V input voltage when suppling the output from C_B and is discussed in section 4.4.1.

When operating from C_B the duty cycle is given by

$$D = \frac{V_o \cdot N_2}{V_B \cdot (N_{1A} + N_{1B})} \tag{4.11}$$

and when operating from the input supply $v_s(t)$

$$D = \frac{V_o \cdot N_2}{v_s(t) \cdot N_{1A}} \tag{4.12}$$

Figure 4.6 shows how the duty ratio varies over a half-mains period for 90V and 265V_{RMS}. The duty ratio is below 0.5 for the 90V_{RMS} and not too low at 265V_{RMS} so that the control IC has problems turning S_1 on properly.
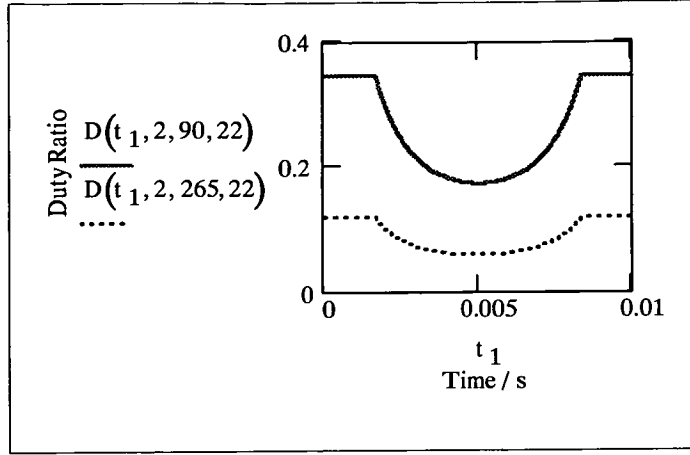
Figure 4.6: Variation of duty cycle over a line half period at 90V and 265V input with n as 2. Traces are listed by side of graph, 1st value is n, 2nd value is the input voltage and 3rd value is the number of turns on N_{1A}.

Sizing of Semiconductors

Design equations are presented in general terms so that they can be used for different values of n. Devices used are heavily over-rated to reduce the risk of component failure on the prototype converter.

MOSFET (S_1)

The voltage across the MOSFET for $n = 2$ is 1125V. Following the method outlined in [118] the RMS current through S_1 at 90V is 2.73A. The peak current from inspection in S_1 is 7.33A, when the converter operates from 265V input voltage. For this application the APT1201R2BLL, a 1200V 12A 1.2Ω R_{dson} device was selected. A small 1200V diode, the BYD33U, was chosen for the reset winding N_3.

Secondary Diodes ($D_{4:5V}$, $D_{5:5V}$, $D_{4:12V}$ and $D_{5:12V}$)

The 5V diodes have a total average current of 20A through the pair $I_{D4:5V} + I_{D5:5V}$, so a 20A (average) diode was used for each since the average current in each diode will be below 20A.

When operating from a 265V mains input the voltage seen across the diode $D_{5:5V}$, $V_{D5:5V}$,

is expressed in equation 4.13 and is calculated to be 86V when $n = 2$, and a BY51-200, a 200V 20A device was chosen. This means that ordinary diodes are used instead of Schottky diodes on the low voltage high current output which will have a noticeable effect on efficiency (voltage drop across ordinary diodes is approximately twice that of Schottky diodes).

$$V_{D5:5V} = V_{pk} \cdot \frac{N_{2:5V}}{N_{1A}} \tag{4.13}$$

Applying equation 4.13 to the 12V secondary the voltage across the diodes is expected to yield 188V with $n = 2$. The 12V diodes have a total average current of 4A through the pair $I_{D4:12V} + I_{D5:12V}$, so the BYT08P-400, an 8A (average) diode was used for each (8A diodes were the easiest/cheapest to use).

Diodes D_1, D_2 and D_3

The voltage seen across D_3, V_{D3}, is expressed in equation 4.14. The worst condition is if C_B is completely discharged and the input voltage is at its maximum of 375V. This gives V_{CB} as a possible 750V with $n = 2$. Again following the methods in [118] the average current in D_3 at 90V is 0.378A. From inspection of the current waveform the peak current through D_3 is 3.64A at 265V input.

$$V_{D3} = v_s(t)\left(1 - \frac{N_{1B}}{N_{1A}}\right) - V_B \tag{4.14}$$

A similar procedure is used for D_2 and the average current is calculated to be 0.949A with $n = 2$ at 90V input. The peak current for D_2 is the same as for S_1 when operating from N_{1A} which is 7.33A for $n = 2$. The voltage across D_2, V_{D2}, can be deduced from equation 4.15. The worst case scenario for this diode is when the input voltage $v_s(t)$ is zero and the bulk capacitor voltage is at its maximum. This gives V_{D2} as 750V when $n = 2$.

$$V_{D2} = V_B \cdot n - v_s(t) \tag{4.15}$$

Diode D_1 only conducts when the bulk capacitor C_B is being recharged and thus the average current through D_1, $I_{av:D1}$, is:

$$I_{av:D1} = \frac{1}{T} \cdot \int_{t_r}^{\frac{T}{2}} C_B \cdot V_{pk} \cdot w \cdot \cos{(w \cdot t)} dt \qquad (4.16)$$

This is calculated to be 0.439A with $n = 2$. The maximum voltage seen across D_1 is the bulk capacitor voltage which is 375V.

Diode Bridge

The voltage seen across the bridge diodes is $v_s(t)$, and the average current is the average of $i_s(t)$. These are calculated to be 375V for $265V_{RMS}$ input and 0.968A when the input voltage is $90V_{RMS}$. The GBU6J was chosen, which is a 600V, 6A device.

Control Circuit

Single stage PFC topologies such as the bi-forward are designed to perform current shaping as part of regulating the output voltage (ie it is a by-product). Since this is the case, the simple method of output voltage regulation was chosen which is fixed frequency PWM with voltage mode control. The UC 3524 control IC was used.

4.4 Simulation of the Bi-Forward Converter

To confirm the operation, and to check that the design produced would work, the bi-forward was simulated using PSpice. As in this case simulation is only used as a confirmation tool and not a detailed design method, the models used in the simulation are the more basic ones. Figure 4.7 shows the circuit schematic entered into the schematic editor of PSpice.

To speed up simulation times the two outputs have been reduced to one 5V output operating with the full output power (148W). The transformer is made up from inductances L_1 to L_4 which are coupled using linear coupling coefficients K_1 to K_6. The coupling coefficients of K_1 to K_6 are set to 1 which represents ideal coupling. For a SMPS transformer a typical coupling coefficient is 0.999, since this is so close to 1 it was rounded up to make the simulations run more efficiently. The magnetising inductance of the primary is approximately the inductance value of the inductor L_1. The inductance value of L_1 is chosen as the value
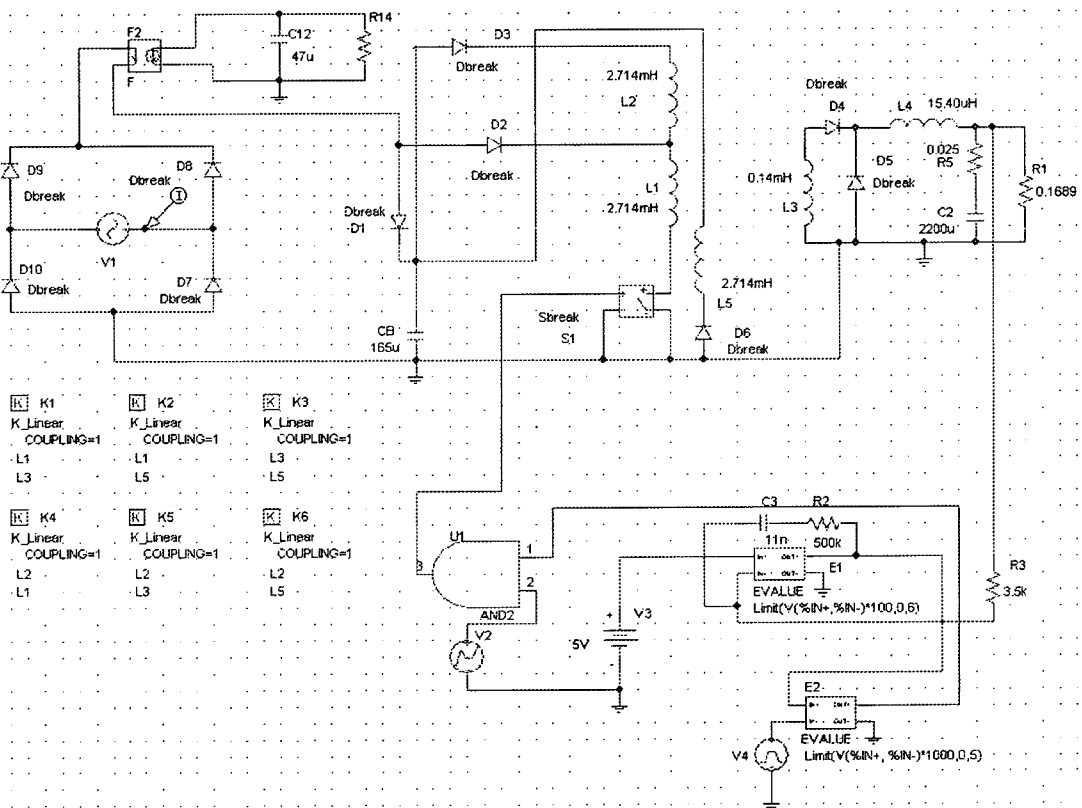
Figure 4.7: PSpice circuit schematic

measured from a standard PC power supply transformer. The turns ratio is set by the inductance ratios as shown in equation 4.17. The diodes are the simple Dbreak models (with the area set to 500 for D_1 to D_5). The MOSFET (S_1) is represented by a voltage controlled switch.

$$L_2 = \left(\frac{N_2}{N_{1A}}\right)^2 \cdot L_1 \qquad (4.17)$$
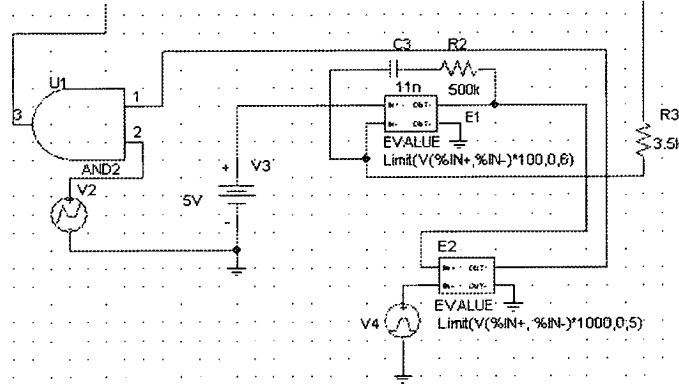
Figure 4.8: PSpice voltage mode controller

The bi-forward needs to have a feedback loop to keep the output voltage constant when operating directly from the line (an ordinary forward converter could be simulated with D set to a constant value and produce a constant voltage output). In figure 4.8 the feedback and gate driving pulse generator part of the simulation circuit is highlighted. The first EVALUE box E_1 is used as an error amplifier. The output voltage is fed back to the negative input and the positive is connected to the reference voltage, which in this case is set to be the required output voltage. The resistor and capacitor network (R_2 and C_3) provides error compensation. The values of R_2 and C_3 were determined by trial and error. The limit term specifies the open loop gain of the amplifier (100, set low to avoid convergence errors) and the maximum and minimum output voltages. The second EVALUE box E_2 is used as a comparator. The two inputs are the output of the error amplifier and a clock signal. The clock signal is a modified ramp from 0 to 5V at 100kHz. The signal ramps up for half of a cycle and then sits at 5V until the start of the next cycle; this is used to limit the duty ratio to 0.5. The limit term is set up in the same manner as for E_1. The output of E_2 is a square wave driving signal. The AND gate and voltage source V4 are included to avoid convergence problems when the simulation starts by delaying the application of the driving

signal to the voltage controlled switch.

The part of the schematic in figure 4.7 formed from F_2, C_{12} and R_{14} is used to produce an averaged version of the input current, as otherwise all that is seen is a set of high frequency DCM current pulses giving no clue to the overall waveform shape. The component F_1 is a current controlled current source and C_{12} and R_{14} form a filter.

The simulations are carried out with the accuracies in PSpice set as shown in table 4.1, so that the simulations are not too slow and can reach a steady state result in a reasonable time. The capacitors and inductors have been set with initial conditions close to expected operating conditions so that the simulation will quickly reach a steady state. This also reduces the transient effects of the first cycle which may have a bearing on the measured current harmonics. The simulations were carried out at 90V, 100V, 230V and 265V RMS. The simulations at 100V and 230V are to examine the input current, and the 90V and 265V simulations are to check current and voltage stresses. 10% or better agreement is hoped for between simulation results and analysis predictions.

Setting Name	New Setting
ABSTOL	$10\mu A$
ITL2	50
ITL4	500
LIMPTS	10k
RELTOL	0.005
VNTOL	0.1mV

Table 4.1: PSpice settings that have been changed

4.4.1   Simulation Results

Tables F.1 and F.2 in appendix F show the current harmonics for full power input at 230V and 100V compared to the regulation values for class D and A. The input power was calculated in PSpice. From table F.1, PSpice predicts that the topology at 230V will only pass class D for the 3rd and 5th harmonic (Mathcad for 200W predicts passes at the 3rd, 5th, 7th, 9th, 11th, 25th, 27th, 29th, and 33rd), and fails class A at the 15th, 17th, 23rd, 31st and 37th harmonics (Mathcad predicts 8th 10th, 12th, 15th, 17th, 20th, 22nd, 32th, 34th, 35th). For 100V in table F.2 Pspice predicts that the bi-forward will only pass the 3rd, 5th, 7th, 15th, 25th and 31st harmonics for class D (Mathcad predicts 3rd, 5th, 7th, 9th, 11th, 25th, 27th,

29th, and 33rd) and completely passes class A (as does Mathcad for 200W).

Table 4.2 shows the peak voltages and currents (ignoring spikes) for the semiconductors as predicted by PSpice with a $265V_{RMS}$ input voltage. When comparing the average and RMS currents for $90V_{RMS}$ input calculated in Mathcad in section 4.3 and predicted by PSpice, the difference between them was found to be above the desired 10%. The calculations were redone, but considering diode voltage drops, switch losses, the same input power as PSpice and considering the discharging of the bulk capacitor C_B while it was supplying the output, the results of which are shown in table 4.3, but not including the values calculated in section 4.3. These modifications brought the calculated values to within 10% of the simulated values. The diode voltage drops when conducting were measured to be 0.705V for D_1 to D_5 in PSpice and D_7 to D_{10} as 1.5V. The voltage across S_1 was measured to be 3.3V when D_3 was conducting and 6.8V when D_2 was conducting in PSpice. These were the values used in the recalculation. The voltage on the capacitor was calculated to fall from 125.6V to 84.8V with a 90V input. The peak voltages for D_1 to D_3 were recalculated for normal operating conditions. When simulating at 90V the output voltage fell from 5V to 4.7V when the output was supplied from C_B. This is due to C_B becoming discharged to below a voltage where the duty cycle cannot open up any more (duty is limited to 0.5), to maintain output voltage. This happens as the circuit was originally designed to operate with C_B as 470μF where V_{CB} was only expected to fall to 110V. The problem could be solved by reconnecting the two 330μF capacitors in parallel when operating from the low line, but as this is only a minor defect they are left in series.

Device	Peak Voltage/V		Peak Current/A	
	PSpice	Mathcad	PSpice	Mathcad
S_1	1183	1122	7.12	7.33
D_1	213	375	3.87	–
D_2	372	375	7.15	7.33
D_3	363	375	3.55	3.64
$D_{4:5V}$	84	86	N/A	N/A
$D_{5:5V}$	84	86	N/A	N/A

Table 4.2: Peak voltage and current on key components at 265V measured in PSpice compared to Mathcad predictions

57

Device	Average or RMS Current/A	
	PSpice	Mathcad
S_1	3.22A$_{RMS}$	3.11A$_{RMS}$
D_1	0.491A	0.545A
D_2	1.30A	1.21A
D_3	0.490A	0.521A
DB	0.853A	0.968A

Table 4.3: Average or RMS currents in key components at 90V measured in PSpice compared to Mathcad predictions including device voltage drops
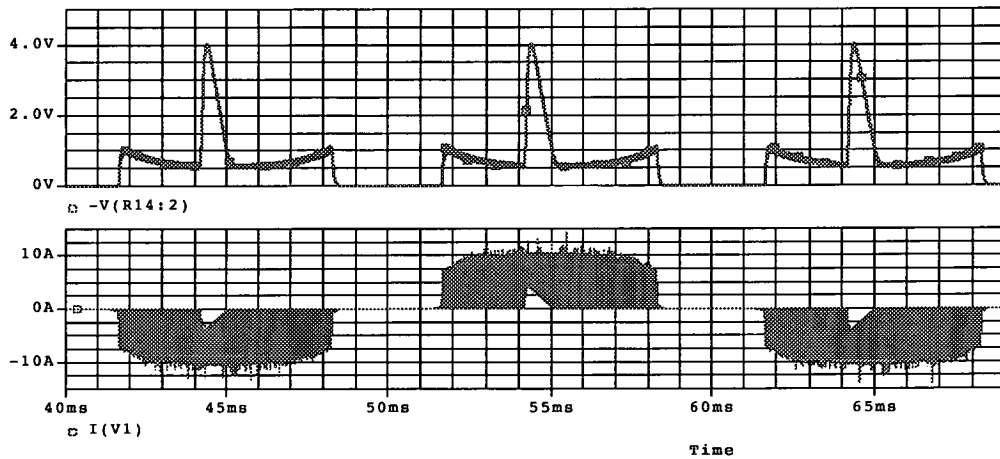
Figure 4.9: Line frequency waveforms produced by PSpice at 230V input voltage and 150W output power. Top trace) averaged input current seen as a voltage across R_{14} and, bottom trace) unaveraged input current

58

4.4.2 Simulation Waveforms

Figure 4.9 shows the unfiltered input current at line frequency of the bi-forward for $n = 2$ at $230V_{RMS}$ input which is just 100kHz current pulses superimposed onto the recharging of C_B (the triangular section). The top trace is the averaged current displayed as the voltage across R_{14}. This is very similar in shape to the predicted shape from equation 4.8. The waveforms for 100V and 75W input are not shown as they are very similar.
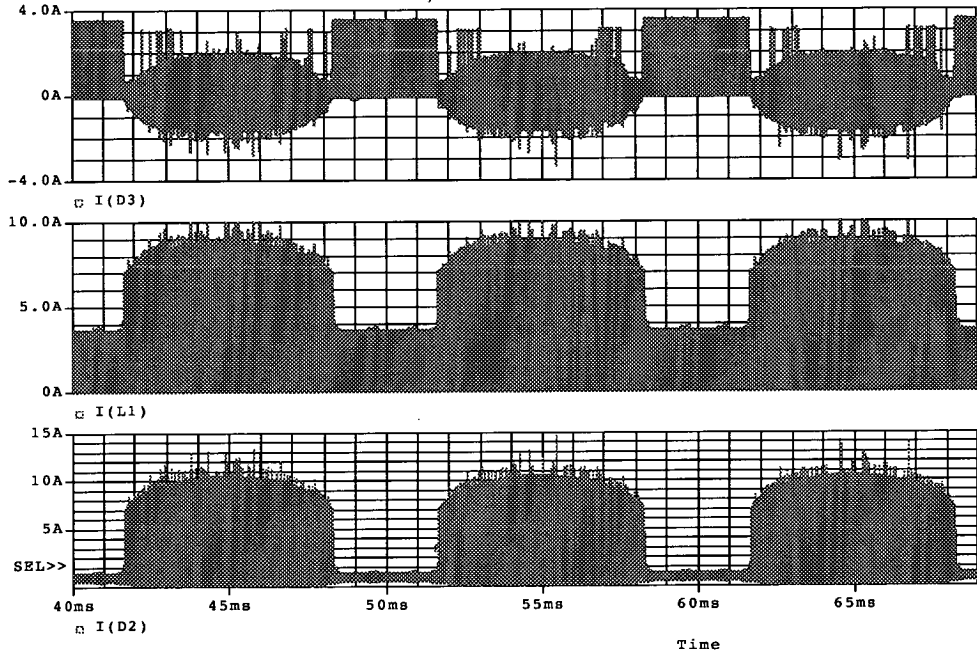
Figure 4.10: Simulated line frequency current through diode D_3 (top trace), inductor L_1 and S_1 (middle trace) and diode D_2 (bottom trace) for 230V and full load output at line frequency

Figure 4.10 shows the line frequency waveforms for the current through D_3, L_1 and D_2. They show D_3 only conducts during the zero crossings (the part between conduction periods is pulses which occur on the switching transitions). A similar effect can be seen for D_2 which is conducting when the input voltage is high. The current in L_1 and S_1 is a combination of both. The current waveforms for D_3, L_1 and D_2 at switching frequency are very similar to CCM current waveforms in a normal forward converter.

4.5 Experimental Results

The prototype circuit could be run from either an isolation transformer and variac or a transformer coupled AC source. When running via the isolation transformer and variac the input voltage waveform to the circuit had a flattened peak due to a distorted mains voltage waveform in the laboratory. Shown in figure 4.11 is the final circuit schematic for the circuit that was tested and in figure 5.20 is a photograph of the experimental circuit with an input inductor. Table G.1 in appendix G lists the components.
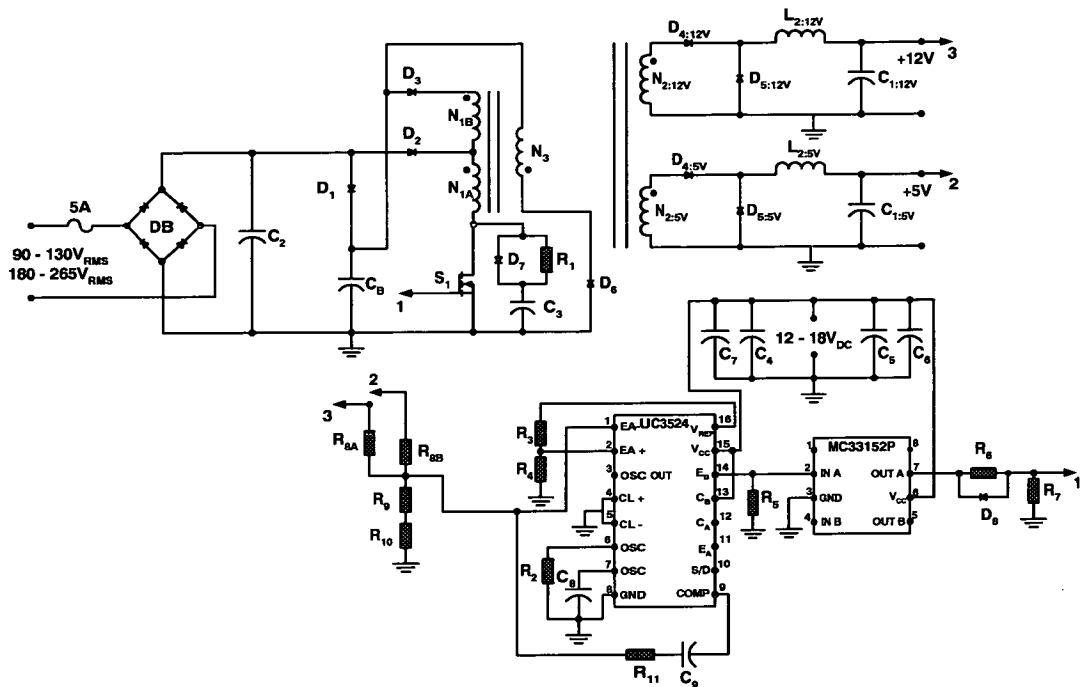
Figure 4.11: Final and complete circuit schematic for the bi-forward converter

4.5.1 Changes to the Prototype

To improve the current waveform drawn by the converter a $1\mu F$ capacitor, C_2 was placed across the diode bridge rectifier. This helps to stabilise the voltage on the DC side of the bridge. The other change was to place a RCD snubber across MOSFET S_1 to reduce turn off losses, as S_1 was suffering from thermal run away at high voltage and power. The snubber circuit is shown in figure 4.11. The snubber was designed following the procedure in [119].

4.5.2 Harmonic Tests

The harmonic tests were carried out at 75W and full load input power, both at 100V and 230V, but not at 230V and full load as the converter was operating incorrectly. The tests were carried out using a Hewlett Packard AC source and harmonic measuring program at Minebea Electronics. The results are shown in figures 4.12, 4.13 and 4.14. These figures show that the converter is unable to meet class D, particularly at 75W where the converter fails at almost every odd harmonic apart from the 3rd and 5th at 230V and a large number at 100V. At full load the performance is better, only failing at the 11th, 13th, 15th, 35th and 37th at 100V. Many of the class D harmonic limits are exceeded by a large margin. These results compare well with the PSpice results in table F.2 and the results from the Mathcad analysis shown in figures A.1 and A.2. At 100V full load the converter passes the class A regulations. This is the same as predicted by both PSpice and the analysis.
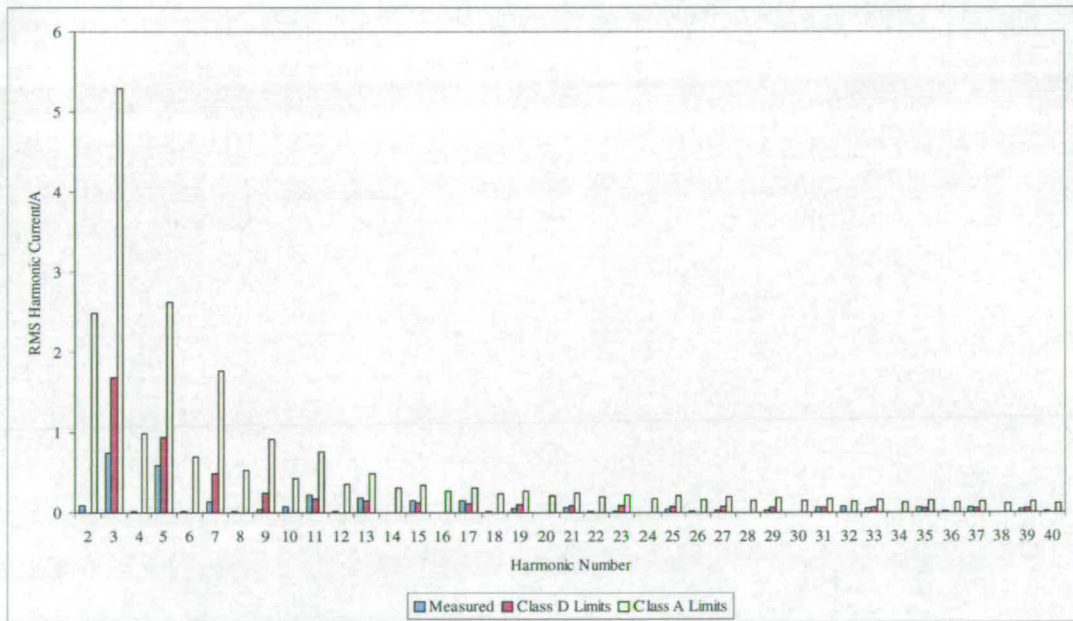
Figure 4.12: Measured RMS input current harmonics at 100V and full load compared to class D and A

4.5.3 Voltage Stress on MOSFET S_1

The voltage on S_1 was measured to be 845V at 265V input. This is lower than expected from PSpice and the analysis, both of which predicted over 1100V. The reason this voltage is lower is because the MOSFET snubber circuit is resetting the transformer instead of the
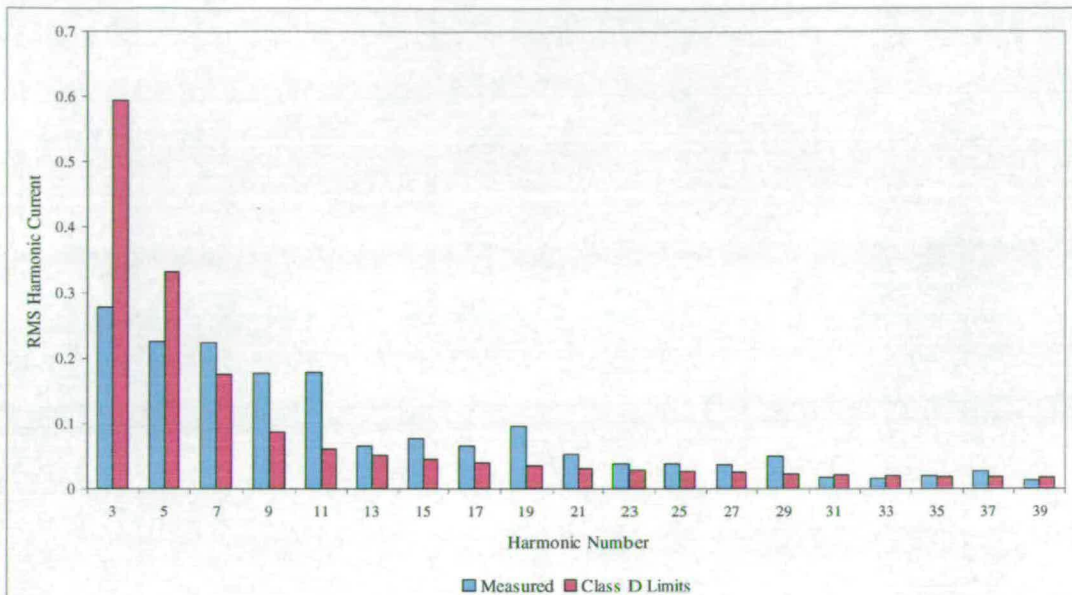
Figure 4.13: Measured RMS input current harmonics at 100V and 75W input power compared to class D
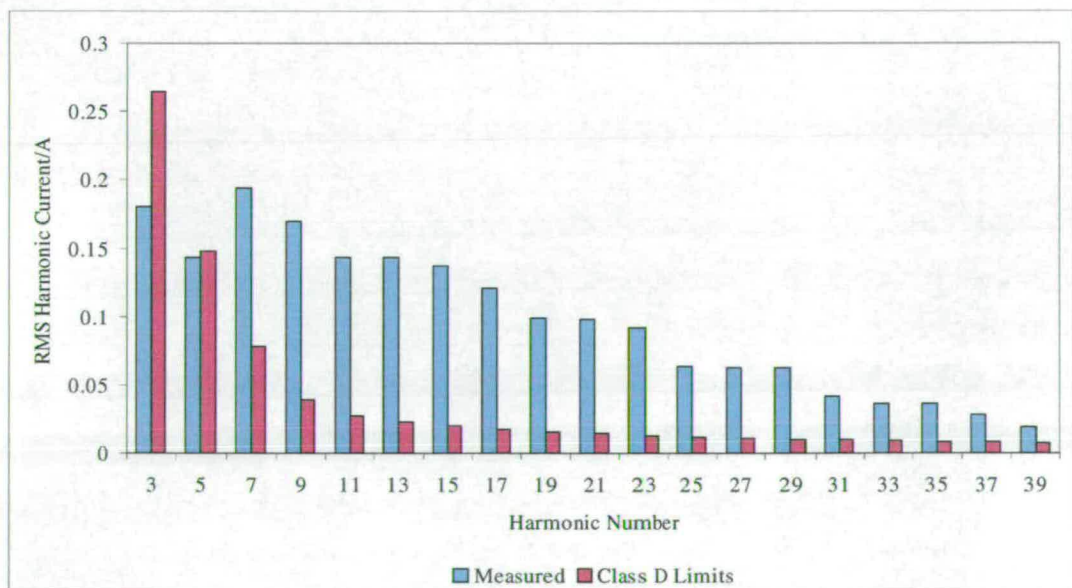
Figure 4.14: Measured RMS input current harmonics at 230V and 75W input power (77W) compared to class D

tertiary winding N_3. This was proven, since when the voltage across the reset winding diode D_6 was measured it never became forward biassed. This occured across the whole input voltage range. The snubber primary purpose is as a switching aid and not to reset the transformer. In [93] a RCD snubber is used to reset the transformer and the reset winding, N_3, is removed.

4.5.4 Efficiency

Efficiency readings taken during harmonic tests are given in table 4.4

Input Voltage/V	Output Power/W	Input Power/W	Efficiency/%
100V	57.8	76	76
100V	143	214	66.8
230V	56.6	77.7	72.9

Table 4.4: Efficiency measurements for the bi-forward converter at 100V and 230V

4.6 Conclusion

This study shows that the bi-forward converter is not as attractive as was expected. It was not expected to pass the class D regulations, but it was expected to meet the class A regulations, and was predicted to have difficulties at 230V full load. The use of an RCD MOSFET snubber was found to be useful in that it was resetting the transformer at a lower voltage than expected, meaning that a lower voltage device could be used. Using an RCD snubber would also allow the duty cycle to extend beyond 0.5. The efficiency reading at full load is dissapointing. This is due to the use of ordinary diodes on the 5V output instead of Schottky diodes normally used in this sort of application.

In light of the fact that the basic bi-forward converter is not able to pass class D, and since it is class D which PC power supplies need to pass, it was decided not to do any more tests on this version and to work on the modified version to be described in the next chapter and showing more promise. The basic bi-forward is most likely ideal for use in low power applications (100W or less output) which only have to meet class A.

Chapter 5

Bi-Forward Converter with Input Inductor

5.1   Introduction

In chapter 4 the bi-forward converter was investigated. It was found to be unable to pass the class D regulations and only just meet the class A regulations at low powers (200W at 100V). In spite of this the bi-forward converter in chapter 4 has a simple operation, and the voltage on the bulk capacitor does not rise above the peak voltage of the line. To improve the PFC performance of the bi-forward converter an inductor, L_1, was added to the converter as shown in figure 5.1, by Zhao in [95]. The inductor changes the current shape and increases the conduction period of the input current. With the addition of L_1 the converter in [95] was able to meet class D with ease and with little detriment to the voltage level on C_B (it rises a small amount above the peak of the line).

5.2   Operation

In figure 5.2 the input current waveform is shown for a half line period: the dashed lines are transitions between different conduction methods that occur.
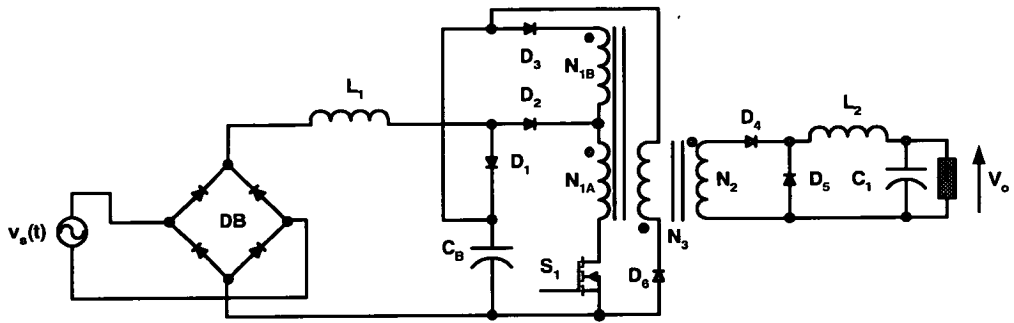
Figure 5.1: Bi-Forward converter with input inductor L_1
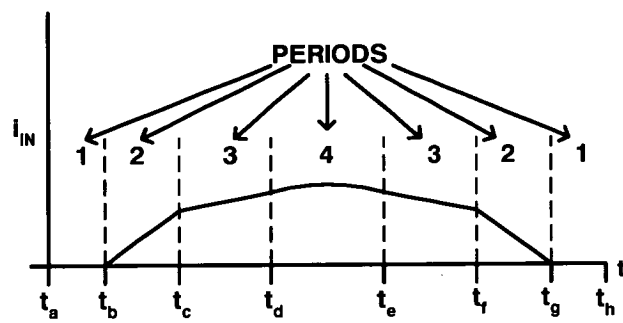
Figure 5.2: Typical input current waveform for a half line period showing the different conduction periods of L_1

65

Period 1: t_a to t_b and t_g to t_h

During the zero crossings from t_a to t_b and t_g to t_h the output is supplied entirely from C_B and no current is flowing through the input part of the circuit.

Period 2: t_b to t_c and t_f to t_g
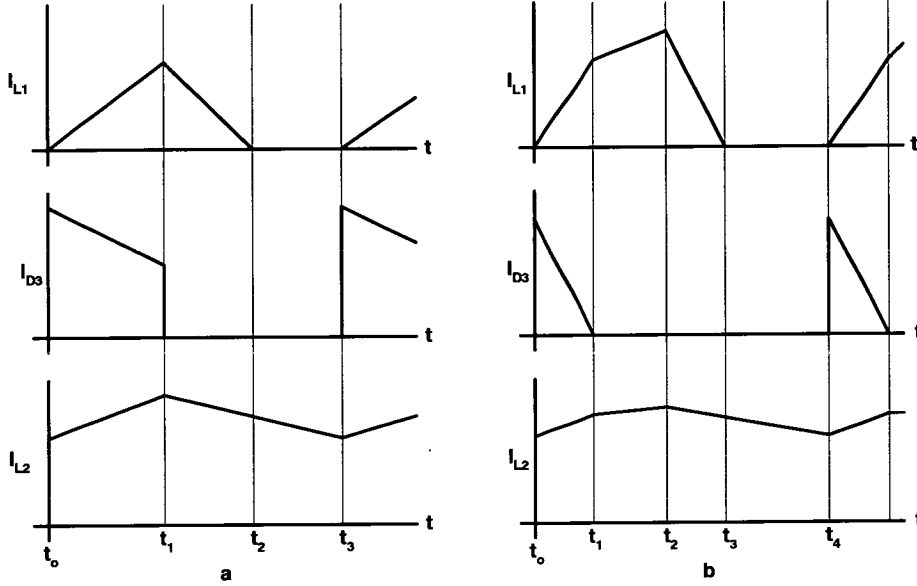
Figure 5.3: a: Current waveforms for L_1, D_3 and L_2 when input voltage is low between t_b to t_c and t_f to t_g, b: Current waveforms for L_1, D_3 and L_2 when input voltage is higher between t_c to t_d and t_e to t_f.

At low input voltages from t_b to t_c and t_f and t_g in figure 5.3a L_1 is in DCM. Shown in figure 5.3a are the key switching frequency waveforms for this period. The device S_1 is turned on at t_0 and the current in L_1 ramps up from zero. This current also flows in N_{1A} of the transformer supplying the output. This is topped up by supplying the remaining output power from the capacitor C_B via diode D_3 and both parts of the transformer primary. The current in L_2, I_{L2}, is formed from

$$I_{L2} = (N_{1A}/N_2) \cdot I_{L1} + ((N_{1A} + N_{1B})/N_2) \cdot I_{D3} \qquad (5.1)$$

As the voltage across L_1 is small the current never rises high enough to supply the output on its own. At t_1, S_1 is turned off and the current in L_1 is discharged into C_B until t_2. At

t_3 the cycle repeats.

Period 3: t_c to t_d and t_e to t_f

Further on in the cycle from t_c to t_d and t_e to t_f the switching frequency behaviour is now as shown in figure 5.3b. The current in L_1 ramps up quickly from t_0 when S_1 is turned on as the voltage across L_1 is higher. Again the output current is topped up by current from C_B. At t_1 the current in L_1 equals the current in L_2 (seen through the transformer by turns ratio $N_2 : N_{1A}$) and the two connect in series supplying the complete output power directly from the input. At t_2, S_1 is turned off and L_1 discharges into C_B until t_3. At t_4 the cycle repeats.

Period 4: t_d to t_e
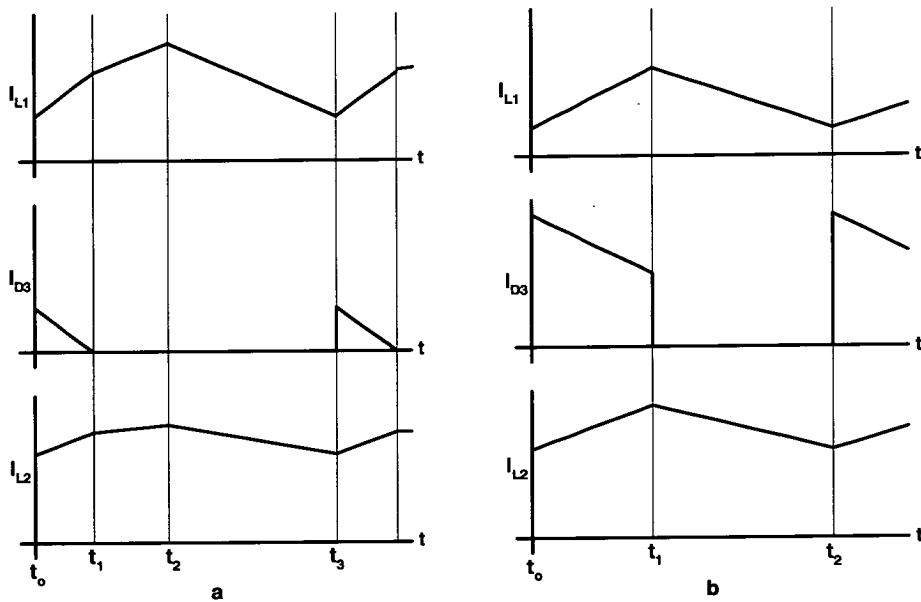
Figure 5.4: a: Current waveforms for L_1, D_3 and L_2 when input voltage is high between t_d to t_e, b: Current waveforms for L_1, D_3 and L_2 when converter enters period 2A.

Across the peak of the line from t_d to t_e the converter enters a fourth operating condition where the current in L_1 is in CCM. The switching frequency waveforms are shown in figure 5.4a. When S_1 turns on at t_0 there is already current flowing in L_1. The current in L_1 now starts to ramp up. The current is topped up by current from C_B. At t_1 the current in

L_1 equals the current in L_2 (seen through the transformer) and the two connect in series supplying the complete output power directly from the input. At t_2 S_1 turns off and the current in L_1 discharges into C_B until t_3 when S_1 is turned on again for the next cycle.

Period 2A

While carrying out the analysis it was found that there was another possible operating mode for L_1 during period 2. This is where L_1 goes into CCM, but the current has not reached the reflected secondary current, so the output is also supplied from C_B for the whole of the on period. Shown in figure 5.4b is the switching frequency waveforms for this period. It is possible from this period to enter period 4 directly.

At t_0 S_1 is turned on. The current in L_1 is already flowing and will now start to ramp up. At t_1 S_1 will turn off and the current in L_1 will ramp down until t_3 when the cycle repeats itself. The current in L_1 never reaches the reflected secondary current so the output is also supplied from C_B for the whole period. If the current in L_1 reaches the reflected secondary current during the on time of S_1 then the converter will enter period 4.

5.3   Analysis

All the analysis and design calculations were carried out using MathCad 2000.

5.3.1   Assumptions

In addition to the assumptions in section 4.3.2 the following assumptions were made:

1. The secondary current is assumed to be a constant dc value without any inductor ripple on L_2 when seen from the primary side of the transformer. This makes the equations developed solvable for the period t_c to t_h, which they are not if the inductor L_2 current ripple is considered.

2. The voltage on the bulk capacitor is constant during a line cycle.

3. During a switching cycle the input voltage is constant.

68

5.3.2 Analysis at Switching Frequency

The input voltage is defined as:

$$v_s\left(t\right) = V_{pk} \cdot \sin\left(\omega \cdot t\right) \tag{5.2}$$

Period 1: t_a to t_b and t_e to t_f

The output is supplied completely from C_B and the input current is zero. The converter is operating just like an ordinary forward converter.

Period 2: t_b to t_c and t_f to t_g

During this period the output is supplied by both the input and C_B jointly for the complete duty cycle as shown in figure 5.3a. The duty ratio, D_2, is set by the bulk capacitor, C_B, where the voltage on C_B is V_B.

$$D_2 = \frac{(N_{1A} + N_{1B}) \cdot V_o}{N_2 \cdot V_B} \tag{5.3}$$

The inductor L_1 is operating in DCM. Applying $v = L \cdot \frac{di}{dt}$ during the on time of S_1 gives:

$$v_s\left(t\right) - \frac{N_{1A}}{N_{1A} + N_{1B}} \cdot V_B = \frac{L_1 \cdot I_{pk2} \cdot f_s}{D_2} \tag{5.4}$$

where f_s is the switching frequency.

When S_1 turns off L_1 discharges into C_B until the current reaches zero and is blocked by diode D_1. The discharge equation for L_1 is

$$V_B - v_s\left(t\right) = \frac{L_1 \cdot I_{pk2} \cdot f_s}{D_{f2}} \tag{5.5}$$

Equating 5.4 and 5.5 the fall time duty ratio, D_{f2}, can be found:

$$D_{f2} = \frac{\left(v_s\left(t\right) - \frac{N_{1A}}{N_{1A}+N_{1B}} \cdot V_B\right) \cdot D_2}{V_B - v_s\left(t\right)} \qquad (5.6)$$

The peak current, I_{pk2}, in L_1 for one switching cycle is:

$$I_{pk2} = \frac{\left(v_s\left(t\right) - \frac{N_{1A}}{N_{1A}+N_{1B}} \cdot V_B\right) \cdot D_2}{L_1 \cdot f_s} \qquad (5.7)$$

The average current, I_{av2}, in L_1 during one switching cycle of this period is:

$$I_{av2} = \frac{D_2 + D_{f2}}{2} \cdot I_{pk2} \qquad (5.8)$$

This period will begin when the input voltage $v_s\left(t\right)$ is higher than the voltage at the centre tap of the transformer primary windings:

$$v_s\left(t\right) > \frac{N_{1A}}{N_{1A} + N_{1B}} \cdot V_B \qquad (5.9)$$

Period 3: t_c to t_d and t_g to t_h

This period is when L_1 is still operating in DCM, but the current in L_1 reaches the reflected load current and takes the complete throughput load current causing C_B to stop conducting (see figure 5.3b).

The period will start and end when the current ramping up in L_1 reaches the reflected current in L_2 (current in L_2 is I_o) seen through winding N_{1A} at time t_1 (figure 5.3a). Rearranging equation 5.4 and solving for t when I_{pk2} is the reflected average current in L_2 gives:

$$t_c = \frac{\sin^{-1}\left[\frac{\frac{N_2}{N_{1A}} \cdot I_o \cdot L_1 \cdot f_s}{D \cdot V_{pk}} + \frac{N_{1A} \cdot V_B}{\left(N_{1A}+N_{1B}\right) \cdot V_{pk}}\right]}{\omega} \qquad (5.10)$$

From figure 5.3b the current in L_1 will ramp up from zero to the reflected current of L_2 through N_2/N_{1A} from t_0 to t_1. This period is considered as a small part of the duty cycle ΔD_3. Taking account of assumption 1 (section 5.3.1), ΔD_3 is calculated to be:

$$\Delta D_3 = \frac{\frac{N_2}{N_{1A}} \cdot I_o \cdot L_1 \cdot f_s}{v_s\left(t\right) - \frac{N_{1A}}{N_{1A}+N_{1B}} \cdot V_B} \tag{5.11}$$

Following the same assumption the duty D_{f3} for the discharge of L_1 into C_B during the switch S_1 off period is calculated to be:

$$D_{f3} = \frac{\frac{N_2}{N_{1A}} \cdot I_o \cdot L_1 \cdot f_s}{V_B - v_s\left(t\right)} \tag{5.12}$$

Equations 5.11 and 5.12 are formed from applying $v = L\frac{di}{dt}$ to L_1 over the relevant period. During the remaining conduction period between t_1 and t_2 $((D_3 - \Delta D_3)$ expressed as a duty) the current in L_1 is considered constant as:

$$I_{L1} = \frac{N_2}{N_{1A}} \cdot I_o \tag{5.13}$$

The overall duty cycle D_3 for S_1 during this period can be calculated from the flux balance for L_2 shown in equation 5.14:

$$\frac{V_o\left(1 - D_3\right)}{L_2} = \frac{\left(\frac{N_2}{N_{1A}} \cdot v_s\left(t\right) - V_o\right) \cdot \left(D_3 - \Delta D_3\right)}{\left(\frac{N_{1A}}{N_2}\right)^2 \cdot L_1 + L_2} + \frac{\left(\frac{N_2}{N_{1A}+N_{1B}} \cdot V_B - V_o\right) \cdot \Delta D_3}{L_2} \tag{5.14}$$

Equation 5.14 is rearranged to give D_3,

$$D_3 = \frac{\frac{V_o + \left(V_o - \frac{N_2}{N_{1A}+N_{1B}}\right) \cdot \Delta D_3}{L_2} + \frac{\left(\frac{N_2}{N_{1A}} \cdot v_s(t) - V_o\right) \cdot \Delta D_3}{\left(\frac{N_2}{N_{1A}}\right)^2 \cdot L_1 + L_2}}{\frac{\frac{N_2}{N_{1A}} \cdot v_s(t) - V_o}{\left(\frac{N_2}{N_{1A}}\right)^2 \cdot L_1 + L_2} + \frac{V_o}{L_2}} \tag{5.15}$$

The average current, I_{av3}, in L_1 during this period is calculated to be:

$$I_{av3} = \frac{N_2}{N_{1A}} \cdot I_o \cdot \left(2 \cdot D_3 + D_{f3} - \Delta D_3\right) \tag{5.16}$$

71

Period 4: t_d to t_e

Period 4 will be entered if:

$$1 = D_3 + D_{f3} \tag{5.17}$$

This equation can be solved to give the time after the zero crossing that period 4 is entered by substituting from equations 5.15, 5.12 and 5.11 for D_3, D_{f3} and ΔD_3. During this period assumption 1 (section 5.3.1) is still valid. The current rise, ΔI_4, in L_1 will be from a non zero value to the reflected secondary current. This is expressed in equation 5.18 where assumption 1 is still valid. This is shown in equation 5.18:

$$\Delta I_4 = \frac{\left(v_s \left(t \right) - \frac{N_{1A}}{N_{1A} + N_{1B}} \cdot V_B \right) \cdot \Delta D_4}{L_1 \cdot f_s} \tag{5.18}$$

where ΔD_4 is the duty ratio for the rise of current in L_1 from the turn on of S_1 to the reflected secondary current from t_0 to t_1 in figure 5.4a.

The current fall in L_1 during the off time (t_2 to t_3) is similarly expressed in equation 5.19:

$$\Delta I_{4F} = \frac{\left(V_B - v_s \left(t \right) \right) \cdot \left(1 - D_4 \right)}{L_1 \cdot f_s} \tag{5.19}$$

It is assumed that during one switching cycle the current in L_1 will make one full excursion and return to the current at the start of the cycle, ie the flux balances. Duty cycle D_4, the overall duty ratio for S_1, can be expressed in the same way as the duty D_3 in equation 5.15. Equations 5.18 and 5.19 can be equated to give D_4, as in equation 5.20.

$$D_4 = \frac{\left(v_s \left(t \right) - \frac{N_{1A}}{N_{1A} + N_{1B}} \cdot V_B \right) \cdot \Delta D_2 + v_s \left(t \right) - V_B}{v_s \left(t \right) - V_B} \tag{5.20}$$

Equating equations 5.15 and 5.20 gives ΔD_4 to be:

72

$$\Delta D_4 = \cfrac{\cfrac{(v_s(t)-V_B)\cdot\left(\frac{N_2}{N_{1A}}\cdot v_s(t)-V_o\right)}{\left(\frac{N_2}{N_{1A}}\right)^2\cdot L_1+L_2}}{\frac{1}{L_2}\cdot\left(\left(V_o-\frac{N_2}{N_{1A}+N_{1B}}\cdot V_B\right)\cdot(v_s(t)-V_B)-V_o\cdot\left(v_s(t)-\frac{N_{1A}}{N_{1A}+N_{1B}}\cdot V_B\right)\right)} +$$

$$\cfrac{\cfrac{(v_s(t)-V_B)\cdot\left(\frac{N_2}{N_{1A}}\cdot v_s(t)-V_o\right)}{\left(\frac{N_2}{N_{1A}}\right)^2\cdot L_1+L_2}}{\cfrac{\frac{N_2}{N_{1A}}\cdot v_s(t)-V_o}{\left(\frac{N_2}{N_{1A}}\right)^2\cdot L_1+L_2}\cdot\left(1-v_s(t)+\frac{N_{1A}}{N_{1A}+N_{1B}}\cdot V_B\right)} \tag{5.21}$$

ΔD_4 can then be substituted to give D_4 in equation 5.15. The current in L_1 at the beginning (I_{4min}) and end (I_{4max}) of the switching cycle is:

$$I_{4min} = \frac{N_2}{N_{1A}}\cdot I_o - \Delta I_4 \tag{5.22}$$

The average current, I_{av4} in L_1 during a switching cycle for period 4 is:

$$I_{av4} = \frac{N_2}{N_{1A}}\cdot I_o - \frac{\Delta I_4}{2}\cdot(1-\Delta D_4 + D_4) \tag{5.23}$$

Period 2A

This is when L_1 is operating in CCM but the current in L_1 has not reached the reflected secondary current. This operation mode will occur when the duty cycle, D_2 (set by C_B), and the fall duty cycle, D_{f2}, together are greater than 1. From equation 5.24 the time t_{2A} after the zero crossing that period 2A occurs is;

$$t_{2a} = \frac{\sin^{-1}\left(\frac{V_B}{V_{pk}}\cdot\left(1-D_2+\frac{N_{1A}}{N_{1A}+N_{1B}}\cdot D_2\right)\right)}{w} \tag{5.24}$$

where D_2 is as expressed in equation 5.3. During the on time the current in L_1 will rise by:

$$\Delta I_{2Ar} = \frac{\left(v_s(t)-\frac{N_{1A}}{N_{1A}+N_{1B}}\cdot V_B\right)}{L_1\cdot f_s} \tag{5.25}$$

The current in L_1 during the off time will fall by:

$$\Delta I_{2Af} = \frac{(V_B - v_s(t)) \cdot (1 - D)}{L_1 \cdot f_s}$$

(5.26)

The current rise ΔI_{2Ar} and fall ΔI_{2Af} are not equal since the duty cycle is set by the flux balance on L_2 and not L_1. This means that the current in L_1 at the end of a switching cycle is not the same as at the beginning. The difference between the two is

$$I_{2Adif} = \Delta I_{2Ar} - \Delta I_{2Af}$$

(5.27)

The peak current, I_{pk2A}, during a switching cycle in L_1 will be:

$$I_{pk2A} = 2 \cdot \Delta I_{2Ar} - \Delta I_{2Af}$$

(5.28)

The average current, I_{av2A}, for a switching cycle during this period in L_1 is approximated by:

$$I_{av2A} = I_{2Adif} + \frac{\Delta I_{2Ar}}{2}$$

(5.29)

Period 4A

The period 4 style conduction following period 2A is considered slightly differently to period 4 when entered from period 3. Because of this it is renamed period 4A.

Period 4A conduction will be entered when the current in L_1 reaches the reflected secondary current which is as assumed in assumption 1 in section 5.3.1. From equation 5.28 solved for when the peak current in L_1 is $\frac{N2}{N1A} \cdot I_o$, this occurs at t_{3A} after the zero crossing and is as shown in equation 5.30:

$$t_{3A} = \frac{\sin^{-1}\left(\frac{L_1 \cdot f_s \cdot I_o \cdot \frac{N2}{N_{1A}} + V_B \cdot \left(2 \cdot D_2 \cdot \frac{N_{1A}}{N_{1A}+N_{1B}} - D_2 + 1 \right)}{(1-D_2) \cdot V_{pk}} \right)}{\omega}$$

(5.30)

74

As for period 2A, period 4A is considered to not have the flux on L_1 balance during a switching cycle as the the duty cycle is again set by the flux balance of L_2 and the current in L_2 at the end of the cycle will not be the same as at the start. Using the minimum value of the current in L_1 calculated for period 2A, the duty ratio for the rise in current in L_1 up to the reflected load current is ΔD_{4A} and is expressed as:

$$\Delta D_{4A} = \frac{\left(\frac{N_2}{N_{1A}} \cdot I_o - I_{2Amin}\right) \cdot L_1 \cdot f_s}{v_s\left(t\right) - \frac{N_{1A}}{N_{1A}+N_{1B}} \cdot V_B} \tag{5.31}$$

where

$$I_{2Amin} = I_{pk2A} - \Delta I_{2Af} \tag{5.32}$$

This value of ΔD_{4A} can be substituted into equation 5.15 to give the on time duty cycle D_{4A}. During the off period the current in L_1 is assumed to fall back to I_{2Amin}.

The average current in L_1 during this period is approximated to:

$$I_{av4A} = \frac{\frac{N_2}{N_{1A}} \cdot I_o + I_{2Amin}}{2} \cdot (1 + \Delta D_{4A} - D_{4A}) + \frac{N_2}{N_{1A}} \cdot (D_{4A} - \Delta D_{4A}) \tag{5.33}$$

5.3.3 Analysis over a Half Line Period

Depending on the output power and the size of L_1 the converter will not necessarily work in all the four periods. If the current in L_1 is unable to meet the reflected load current at all during the on time of S_1 during a half mains cycle, the converter will only operate in periods 1 and 2, and the input current, $i_s\left(t\right)$ is defined as:

$$i_s\left(t\right) = \begin{array}{ll} 0 & t_a < t < t_b \quad t_g < t < t_h \\ I_{av2}\left(t\right) & t_b < t < t_g \end{array} \tag{5.34}$$

If the current in L_1 is able to meet the reflected secondary then the converter will also operate in period 3 as well, but if the current in L_1 always falls to zero before the start of

the next switching cycle it will not enter period 4. The input current for this operation state is:

$$
i_s(t) = \begin{array}{lll}
0 & t_a < t < t_b & t_g < t < t_h \\
I_{av2}(t) & t_b < t < t_c & t_f < t < t_g \\
I_{av3}(t) & t_c < t < t_f &
\end{array}
\tag{5.35}
$$

All four periods will occur if L_1 enters CCM. The input current will then be defined as:

$$
i_s(t) = \begin{array}{lll}
0 & t_a < t < t_b & t_g < t < t_h \\
I_{av2}(t) & t_b < t < t_c & t_f < t < t_g \\
I_{av3}(t) & t_c < t < t_d & t_e < t < t_f \\
I_{av4}(t) & t_d < t < t_e &
\end{array}
\tag{5.36}
$$

If the converter does enter period 2A conduction, but not period 4A conduction, then the input current is:

$$
i_s(t) = \begin{array}{lll}
0 & t_a < t < t_b & t_e < t < t_f \\
I_{av2}(t) & t_b < t < t_c & t_d < t < t_e \\
I_{av2A}(t) & t_c < t < t_d &
\end{array}
\tag{5.37}
$$

If the converter enters periods 2A and 4A the input current is expressed as:

$$
i_s(t) = \begin{array}{lll}
0 & t_a < t < t_b & t_g < t < t_h \\
I_{av2}(t) & t_b < t < t_c & t_f < t < t_g \\
I_{av2A}(t) & t_c < t < t_d & t_e < t < t_f \\
I_{av4A}(t) & t_d < t < t_e &
\end{array}
\tag{5.38}
$$

The input power to the converter can also be expressed in five different ways depending on the number of operation periods the converter is operating in.

For operation in periods 1 and 2.

$$
P_{in} = \frac{2}{T} \cdot \int_{t_b}^{\frac{T}{2}} I_{av2}(t) \cdot v_s(t) \, dt
\tag{5.39}
$$

76

where T is the half line period.

For operation in periods 1, 2 and 3.

$$P_{in} = \frac{2}{T} \cdot \int_{t_b}^{t_c} I_{av2}(t) \cdot v_s(t)\, dt + \frac{2}{T} \cdot \int_{t_c}^{\frac{T}{2}} I_{av3}(t) \cdot v_s(t)\, dt \qquad (5.40)$$

For operation in periods 1, 2, 3 and 4.

$$P_{in} = \frac{2}{T} \cdot \int_{t_b}^{t_c} I_{av2}(t) \cdot v_s(t)\, dt + \frac{2}{T} \cdot \int_{t_c}^{t_d} I_{av3}(t) \cdot v_s(t)\, dt + \frac{2}{T} \cdot \int_{t_d}^{\frac{T}{2}} I_{av4}(t) \cdot v_s(t)\, dt$$
$$(5.41)$$

For operation in periods 1, 2 and 2A.

$$P_{in} = \frac{2}{T} \cdot \int_{t_b}^{t_c} I_{av2}(t) \cdot v_s(t)\, dt + \frac{2}{T} \cdot \int_{t_c}^{\frac{T}{2}} I_{av2a}(t) \cdot v_s(t)\, dt \qquad (5.42)$$

For operation in periods 1, 2, 2A and 4A.

$$P_{in} = \frac{2}{T} \cdot \int_{t_b}^{t_c} I_{av2}(t) \cdot v_s(t)\, dt + \frac{2}{T} \cdot \int_{t_c}^{t_d} I_{av2a}(t) \cdot v_s(t)\, dt + \frac{2}{T} \cdot \int_{t_d}^{\frac{T}{2}} I_{av4a}(t) \cdot v_s(t)\, dt$$
$$(5.43)$$

The RMS current harmonic levels can be calculated from the Fourier series for the waveform and compared to the IEC 61000-3-2 regulation values.

5.4 Converter Design

This version of the bi-forward (with input inductor L_1) is a modified version of the basic bi-forward converter of chapter 4 with the addition of input inductor L_1. This reduces the number of design parameters to just one, which is the inductance value of L_1 (the only additional component). If the converter was being designed from scratch then the important design parameters would be

- The value of L_1

- Transformer turns ratio - in particular between N_{1A} and N_{1B}

- The value of L_2

The specification for this circuit is the same as in section 4.3.1.

5.4.1 Effect of Inductance Value of L_1 on Input Current RMS Harmonics

In [95] the value of inductance for L_1 is low at only 20μH, hence low values of L_1 around that area are investigated. An efficiency of about 70% is assumed so when the converter is working at full output power the input power will be about 200W. L_1 was set to be 10, 20, 50, and 100μH.

Shown in figure 5.5 is the odd harmonic spectrum for 230V and 200W input power. Harmonic 27 for 20μH is very large (exceeding the regulations) and is most likely just an anomaly due to the current waveform being too ideal, or a Mathcad calculation error. 50μH just exceeds the regulations at the 9th and 11th harmonics. All the rest of the current harmonics are below the class D regulation values for all values of L_1. The plot for 10μH is operating in periods 1, 2 and 3, the plot for 20μH is operating in just periods 1 and 2 and the plots for 50μH and 100μH are both operating in periods 1, 2 and 2A. Similar curves for 75W input power show all the current harmonics are below the class D regulation values for all values of L_1, but have not been included in the thesis. At 75W the curves for 10 and 20μH are operating in periods 1, 2 and 3, the curve for 50μH is operating in just periods 1 and 2 and the curve for 100μH is operating in periods 1, 2 and 2A.

Shown in figure 5.6 is the odd harmonic spectrum for 100V and 200W input power. All three values of L_1 (10, 20 and 50μH) shown pass the class D regulation. The plot for 10μH is operating in periods 1, 2 and 3, the plot for 20μH is operating in periods 1, 2, 2A and 4A and the plot for 50μH is operating in periods 1, 2 and 2A. The plot for 100μH is not shown as the voltage on the bulk capacitor C_B was calculated to be less than the peak of the line which would cause C_B to peak charge and distort the current waveform. A similar set of curves for 75W indicated that all values of L_1 (10, 20, 50 and 100μH) passed the class D regulation. The curves observed for 10 and 20μH are operating in periods 1, 2 and 3, the

78
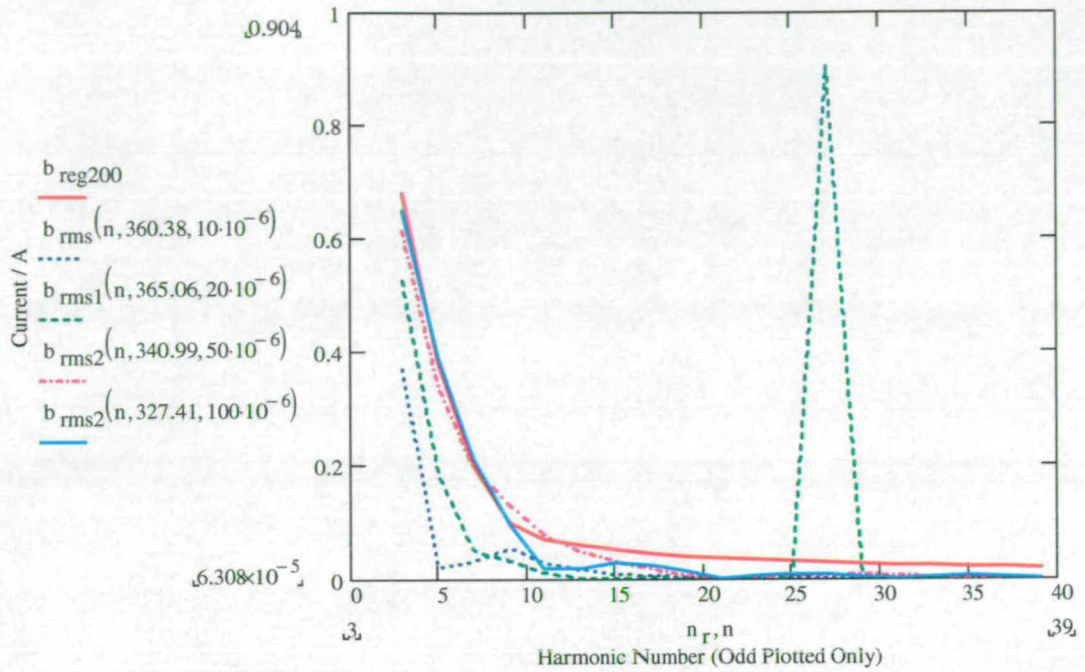
Figure 5.5: Input current class D (trace b_{reg200}) harmonics for 230V input with an input power of 200W with L_1 as 10, 20, 50 and 100μH. Traces are listed by side of graph, 1st value is the voltage on C_B and the 2nd value is the value of L_1.

curve for 50μH is operating in periods 1, 2, 2A and 4A and the curve for 100μH is operating in periods 1, 2 and 2A.

Shown in figures 5.7, 5.8, 5.9, 5.10 and 5.11 are predicted (filtered) current waveforms for the different possible conduction periods the converter operates in. These figures show the variety of different current waveform shapes the converter could draw depending on the power, input voltage and size of L_1. Figures 5.7 (operation in periods 1, 2 and 3), 5.8 (operation in periods 1 and 2) and 5.9 (operation in periods 1, 2 and 2a) are all at 230V and 200W input and show the different current waveforms possible depending on the size of L_1. Figures 5.10 and 5.11 are included to illustrate the current waveform in the remaining two periods 4 and 4A. When the converter enters period 3 (in figures 5.7 and 5.10) the current waveform takes on a much shallower slope due to the output current being fed from the input. In 5.10 the slope of the current increases again when period 4 is entered.
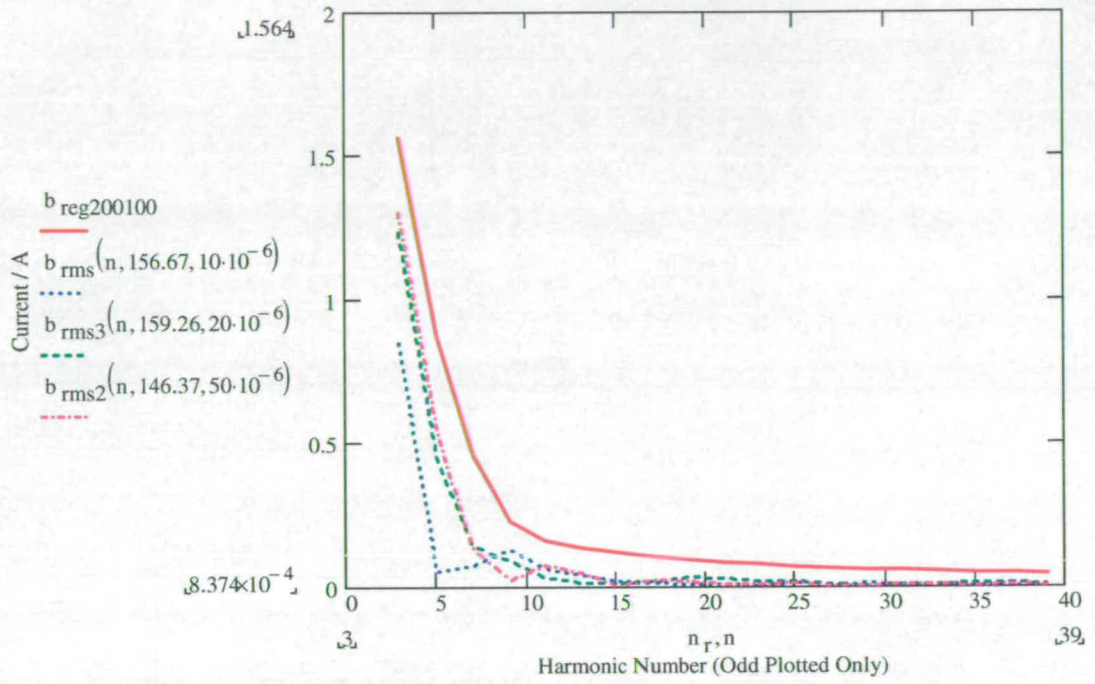
Figure 5.6: Input current class D (trace $b_{reg200100}$) harmonics for 100V input with an input power of 200W with L_1 as 10, 20 and 50μH. Traces are listed by side of graph, 1st value is the voltage on C_B and the 2nd value is the value of L_1.
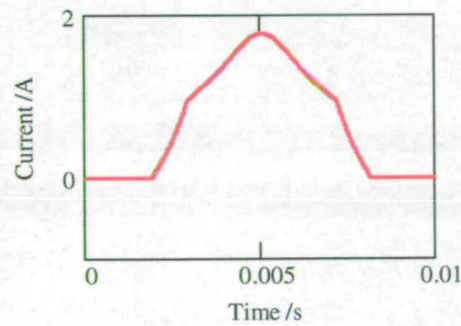
Figure 5.7: Predicted input current waveform at 200W input power at 230V with L_1 as 10μH. The current is flowing in periods 1, 2 and 3. V_B is 360V.
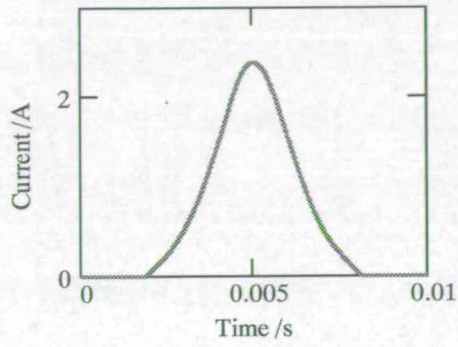
Figure 5.8: Predicted input current waveform at 200W input power at 230V with L_1 as 20μH. The current is flowing in periods 1 and 2. V_B is 365V.
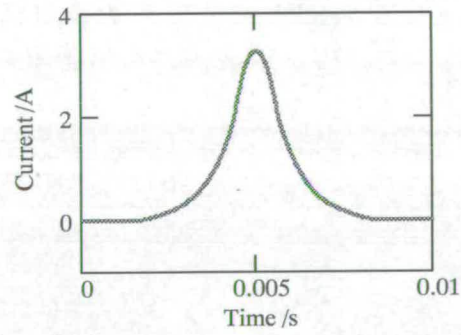
Figure 5.9: Predicted input current waveform at 200W input power at 230V with L_1 as 50μH. The current is flowing in period 1, 2 and 2a. V_B is 341V.
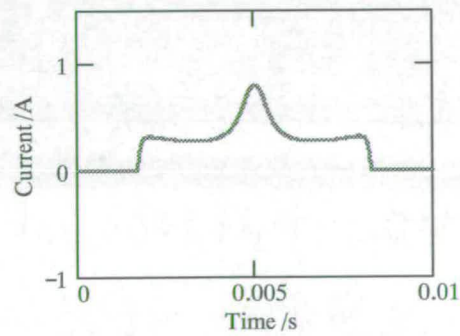
Figure 5.10: Predicted input current waveform at 25W input power at 90V with L_1 as 10μH. The current is flowing in period 1, 2, 3 and 4. V_B is 128V.
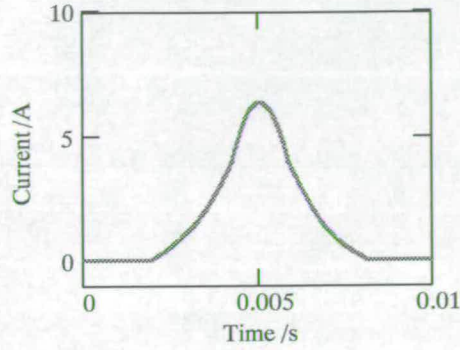
Figure 5.11: Predicted input current waveform at 25 W input power at 100V with L_1 as 20μH. The current is flowing in period 1, 2, 2a and 4a. V_B is 159V.

5.4.2 Effect of Inductance Value of L₁ on the Bulk Capacitor Voltage

Figures 5.12, 5.13, 5.14 and 5.15 show how the bulk capacitor voltage varies with power for L_1 equal to 10, 20, 50 and 100μH with input voltages of 90V, 115V, 230V and 265V respectively. The way the bulk capacitor voltage varies is different for each value of L_1 because of the different periods the converter operates in.

In all four figures (5.12, 5.13, 5.14 and 5.15), when L_1 is 10μH the voltage on V_B rises as the throughput power rises. When L_1 is 10μH, L_1 is operating in conduction periods 1, 2, and 3, except at 90V and 25W input where L_1 just enters period 4 as well. The voltage on bulk capacitor C_B is rising so as to keep the input and output charge from C_B equal during the line cycle. Charge is taken from C_B during the whole line period. This charge is replaced by an equal amount from L_1 discharging during the off periods. At light loads most of the charge to the output is delivered directly from the input, L_1 is in period 2 for a short period and ΔD is also short, but C_B is still supplying the output completely during period 1. To balance the input and output charge from C_B, the voltage on C_B at low powers falls to give L_1 a long discharge time (D_f and D_{f2}), as the peak current level is low. At higher powers the reflected output current flowing in L_1 is much higher. Therefore to deliver the charge C_B needs to keep the output supplied, a shorter discharge time is possible as the current starts much higher, so the overall charge delivered to C_B is much more than at low power. The only way then to balance the charge in and out of C_B over a line cycle is for the voltage on C_B to rise as power increases.

When L_1 is 20 and 50μH the voltage on C_B rises as power increases and then falls again

at higher power. At low power they are operating in periods 1, 2 and 3 so the voltage is rising when the power goes up. When L_1 is at 50μH it leaves conduction period 3 at about 50W and just operates in periods 1 and 2, plus sometimes 2A and possibly 4A. At this point the voltage will level off and start to fall as power goes up. When L_1 is 20μH operation in period 3 is lost much higher in the power range and a drop in voltage only starts to appear around 200W.
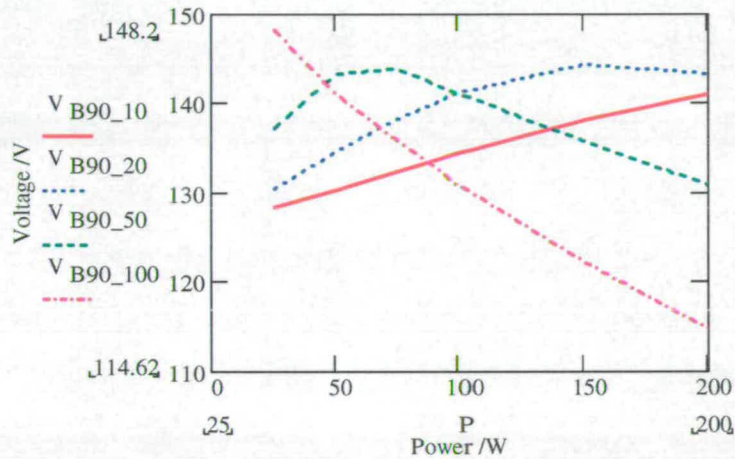
Figure 5.12: Predicted voltage on bulk capacitor C_B at 90V input for $L_1 = 10$, 20, 50 and 100μH. Traces are listed by side of graph. 1st value is the input voltage and the 2nd value the value of L_1.
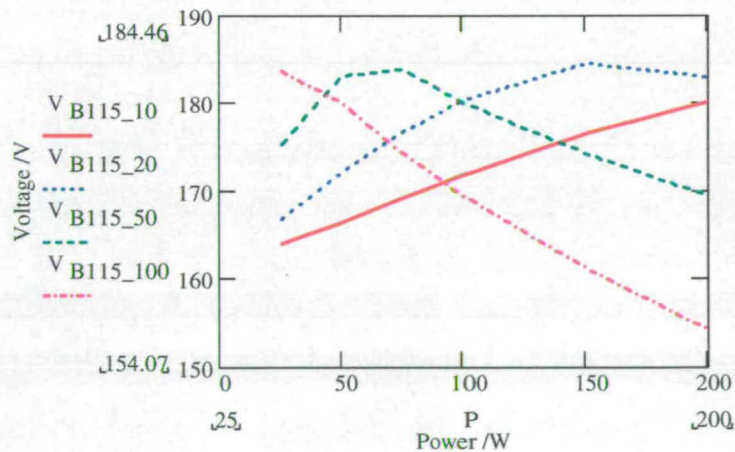
Figure 5.13: Predicted voltage on bulk capacitor C_B at 115V input for $L_1 = 10$, 20, 50 and 100μH. Traces are listed by side of graph. 1st value is the input voltage and the 2nd value the value of L_1.

When direct conduction from the input to the output occurs, the charge balance on C_B
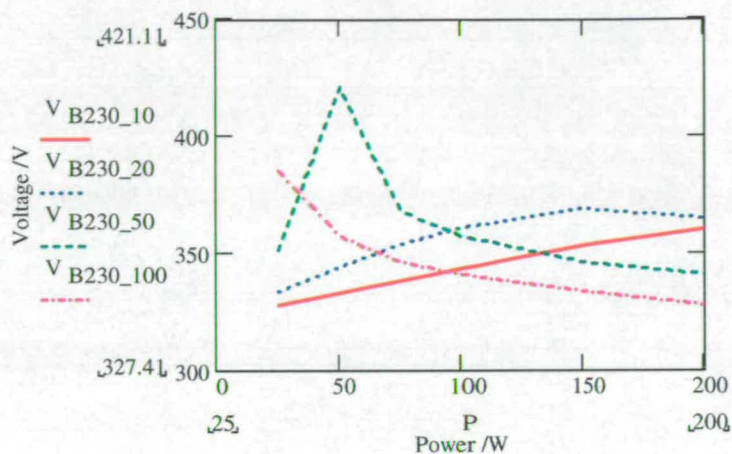
Figure 5.14: Predicted voltage on bulk capacitor C_B at 230V input for $L_1 = 10$, 20, 50 and 100μH. Traces are listed by side of graph. 1st value is the input voltage and the 2nd value the value of L_1.
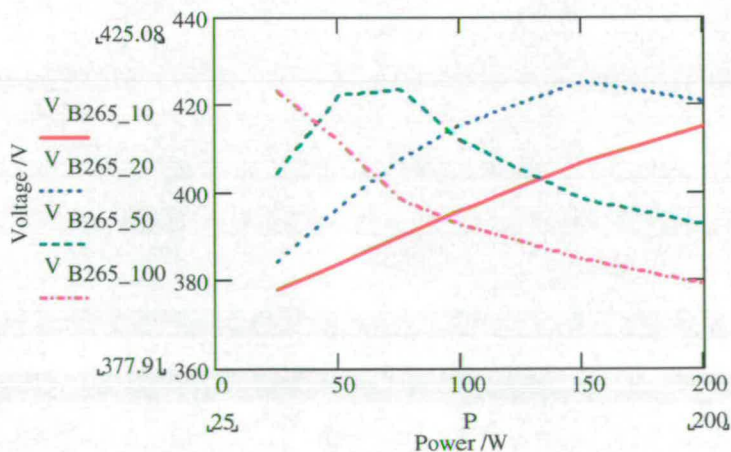
Figure 5.15: Predicted voltage on bulk capacitor C_B at 265V input for $L_1 = 10$, 20, 50 and 100μH. Traces are listed by side of graph. 1st value is the input voltage and the 2nd value the value of L_1.

causes voltage to rise as power goes up. When direct conduction does not occur it causes the voltage on C_B to fall as power goes up. When direct conduction occurs the duty cycle is only affected by the voltage on C_B by a small amount, hence the only way to control the charge balance on C_B is with the discharge of L_1. When C_B is conducting significantly during a line cycle, duty cycle can be used to balance the charge in and out of C_B. This causes the voltage on C_B to fall as power goes up to deliver the required charge to the output, or to cause the voltage to rise at low power to reduce charge taken from C_B.

The voltage on C_B when is L_1 equal to 100μH is falling across the whole power range, as the converter is operating almost all the time in periods 1, 2 and 2A, where there is no direct conduction between the input and output.

5.4.3 Duty Cycle Variation
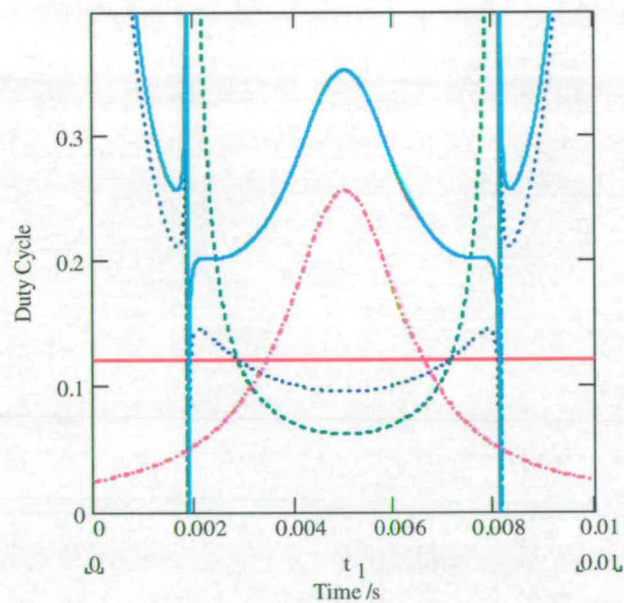
Figure 5.16: Predicted duty cycle variation for 100V 200W input over a half line cycle. Red trace is D_2 the duty cycle when supplied from C_B, blue dot trace is D_3 the on duty cycle for S_1, green dash trace is ΔD_3 the duty of the period where L_1 is charged up to the load current, lilac dash-dot trace is D_{f3} the duty for the fall of current in L_1 to zero and light blue trace is $D_1 + D_{f2}$ the overall condution duty for L_1 with V_B at 361V and L_1 equal to 10μH.

Shown in figure 5.16 is the plot of the different duty ratios that occur when operating in periods 1 to 3 plotted to show how they vary over a half line cycle. The three most important

lines are the red line for duty cycle for D_2 (duty cycle when the output is supplied from C_B for the whole of the on time), the blue dot curve for D_3 (duty cycle when operating in period 3) and the green dash curve for ΔD_3 (the duty for the rise of current in L_1 in period 3). The converter will operate with duty D_2 until the point where the curves for D_2, D_3 and ΔD_3 all intersect. In figure 5.16 this occurs after about 0.002s where D_3 and ΔD_3 gently fall through D_2: from this point the converter will operate with duty cycle D_3 and is in period 3. At the same intersection ΔD_3 falls below D_3. ΔD_3 is the charging up duty cycle for L_1 and has to be below D_3 when in period 3. At the similar crossing point just before 0.008s the converter again reverts to operating with D_2. D_{f3} is shown for completeness. $D_3 + D_{f3}$ is shown to check if the converter will enter period 4: this occurs when the curve exceeds 1. If the D_3 and ΔD_3 curves do not fall below the D_3 curve the converter will not enter period 3.

5.4.4 Selection of L_1

From the harmonic plots and voltage on C_B plots it was decided to set L_1 to be 10 or 20μH. When operating in the low voltage range of 90V to 130V the 100μH inductance produced a voltage on C_B lower than the peak of the mains at 200W which will cause peak charging, and distort the input current waveform. Also the converter does not enter period 3 very often as it should do. Because of these two reasons 100μH was considered to be too high. With L_1 at 50μH the class D regulation was exceeded at 230V 200W. Looking at the bulk capacitor voltage figures 5.15 and 5.14, the voltage goes very high to 423V with a 265V input (it does with all the other values of L_1, but it also goes that high (421V) when operating from 230V input, whereas it does not with the other values). Due to these two reasons a value for L_1 of 50μH was also considered too high.

It was decided to test the prototype using L_1 set to 10 or 20μH (it only requires the removal of a couple of turns of the L_1 inductor to change its value from 20 to 10μH). These two values were considered to give the best design based on what had been investigated because

- It would appear that they will pass class D regulations from 75W to 200W at both 100V and 230V.

- They both operate mainly with period 3 type conduction.

86

All four values for L_1 have very high peak voltages shown in table 5.4.4 and figure 5.15 There is very little difference between them, all being around 420V, but L_1 equal to $10\mu H$ gives the lowest at 415V. Since they are all similarly high this has very little effect on which value to use, but there is a slight benefit of using L_1 equal to $10\mu H$.

Inductance/μH	Voltage/V
10	415
20	425
50	423
100	423

Table 5.1: Peak voltage seen on the bulk capacitor C_B with 265V input

5.4.5 Sizing of Semiconductors

It is expected that the current stresses in this version of the bi-forward will be about the same as in the bi-forward converter in chapter 4. The only concern converting from the bi-forward converter to this version with input inductor L_1 is the voltage seen across certain components due to the increase of peak voltage on C_B from 375V to 425V.

The diodes D_1 to D_3 are already rated for 1000V, so the slight increase in bulk capacitor voltage will not affect these three devices. The voltages across the MOSFET S_1 and the secondary diodes $D_{4:5V}$, $D_{5:5V}$, $D_{4:12V}$ and $D_{5:12V}$ are the ones that need checking.

MOSFET S$_1$

Using equation 4.10 the voltage across S_1 (when there is no snubber across S_1) is 1275V when V_B is at its peak of 425V (L_1 is $20\mu H$), which is 75V higher than what the MOSFET for S_1 is rated for. The snubber which is fitted to the bi-forward converter in chapter 4 must therefore, be left across S_1 to reduce the reset voltage of the transformer. In chapter 4 it reduced the voltage across S_1 from an expected 1120V to 845V and it was expected to have a similar effect on this variation of the topology. It was measured as 830V.

Secondary Diodes

Using equation 4.13 the voltage across the secondary diodes without a snubber across S_1 was calculated to be:

$$D_{4:5V}, D_{5:5V} \quad 96\text{V}$$
$$D_{4:12V}, D_{5:12V} \quad 213\text{V}$$

The diodes used for the 5V output are already rated for 200V and for the 12V output they are rated for 400V. There should be no danger of these voltage ratings being exceeded.

5.5   Simulation

Figure 4.7 shows the simulation schematic used in PSpice, with an inductor called L_{12} added between F_2 and the D_1 and D_2 junction. The simulation was carried out in the same manner as in chapter 4. Again the output voltage is 5V and the transformer was made up of coupled inductors with values set to give the correct turns ratio. The network formed from F_2, C_{12} and R_{14} was used to see the averaged input current shape as in section 4.4.

5.5.1   Simulation Results

In tables F.3 and F.4, in appendix F, are the RMS harmonic currents measured in PSpice for a 150W output power at 100V and 230V respectively. For L_1 equal to 10 and 20μH the simulation results at full output power show the converter passing class D at both 100V and 230V. The class D harmonics shown are for the simulation with lowest input power. This does not change any harmonic that would have passed into one that fails for the other simulations, as the measured RMS harmonic currents are far smaller than the regulation's values. There is only a couple of watts between the higher powered simulation and lower power simulation. This is a similar prediction to the Mathcad analysis of the two designs passing class D (without the large harmonic current seen for the 27th harmonic in some of the analysis).

The simulations were also run at 265V input with 150W output to find the capacitor bulk voltage and the voltages across S_1, D_4 and D_5 without a MOSFET snubber. The results are shown in table 5.2. These results confirm that the snubber across the MOSFET will be

required to keep the transformer reset voltage below 1200V.

Device	Voltage/V
$L_1 = 10\mu\text{H}$	
C_B	413
S_1	1238
D_4	93
D_5	65.6
$L_1 = 20\mu\text{H}$	
C_B	432
S_1	1298
D_4	97.6
D_5	56.5

Table 5.2: Simulated voltage on key components with 265V input and 150W output

5.5.2 Simulation Waveforms

In figure 5.17 are shown the waveforms of the input current for an output of 150W with a 100V input and L_1 equal to $10\mu\text{H}$. The "averaged current" seen across resistor R_{14} is similar in shape to the predicted averaged current in figure 5.7. The slight lean to the left of the waveform is due to the voltage on the bulk capacitor changing during the line cycle (charging up). The current in L_1 is entering period 3. The lower trace shows how the current will look before filtering. It is noted that the switching frequency current always returns to zero.

In figure 5.18 is the same set of waveforms but for L_1 equal to $20\mu\text{H}$. In this case the converter is only operating in periods 1 and 2. Due to this the averaged waveform is slightly different, but is still similar in shape to the predicted waveform in figure 5.8. Again the unfiltered switching waveform is returns to zero.

Figure 5.19 shows the switching frequency waveforms for operation in period 3 when operating at 100V with L_1 as $10\mu\text{H}$. The bottom trace is the current in L_1 and shows the current ramping up from zero to the reflected secondary current where the up-slope changes and then the discharge into C_B; the top trace shows the current in N_{1B}, the current supplied from C_B: this is a falling ramp as L_1 takes more of the output current. This current stops flowing when the current in L_1 reaches the reflected secondary current. The middle trace shows both currents added together flowing through S_1. Simulating at 230V and

89
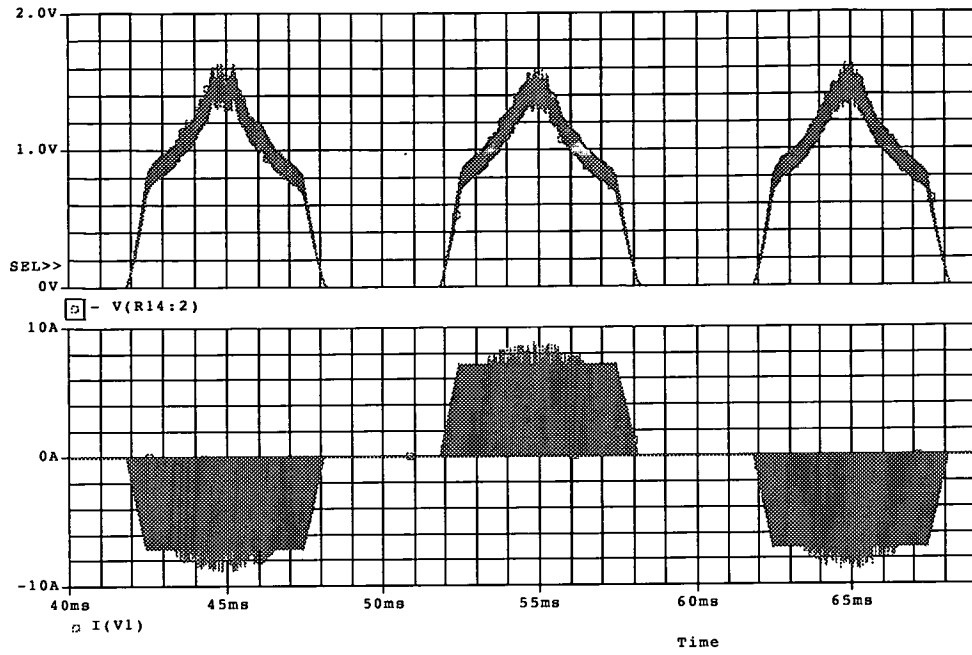
Figure 5.17: Simulated averaged and non average input current waveforms for 230V and $L_1 = 10\mu H$. The converter is operating in periods 1 to 3. The top trace is the averaged current shown as a voltage across R_{14} and the bottom trace is the non averaged current shown as a current.
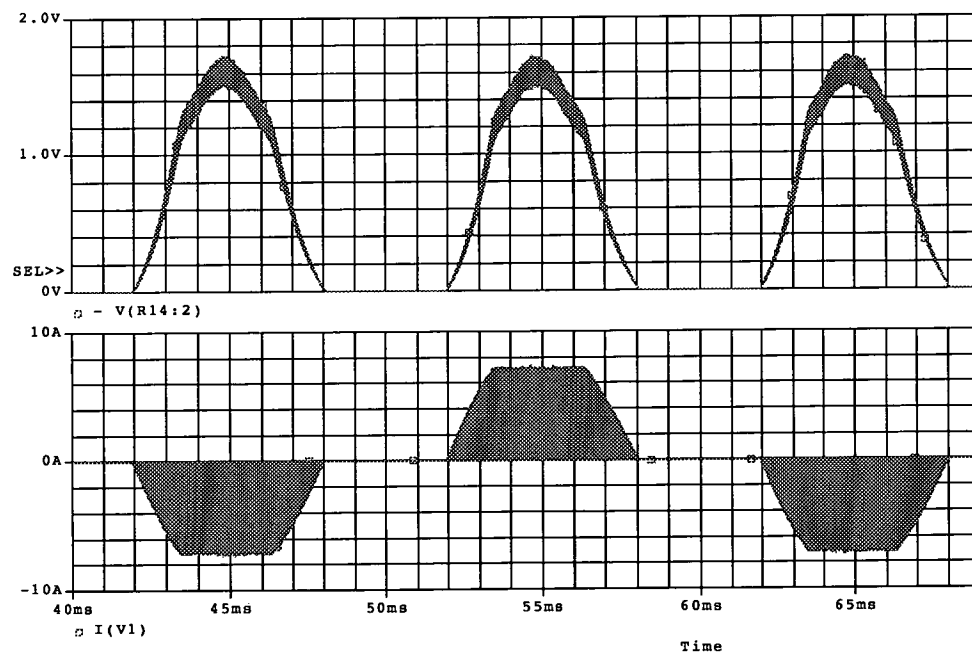
Figure 5.18: Simulated averaged and non averaged input current waveforms for 230V and $L_1 = 20\mu H$. The converter is operating in periods 1 and 2. The top trace is the averaged current shown as a voltage across R_{14} and the bottom trace is the non averaged current shown as a current.

L_1 =20μH, period 2 switching frequency waveforms were observed as was period 4A switching frequency waveforms when simulating at 100V and L_1 =20μH.
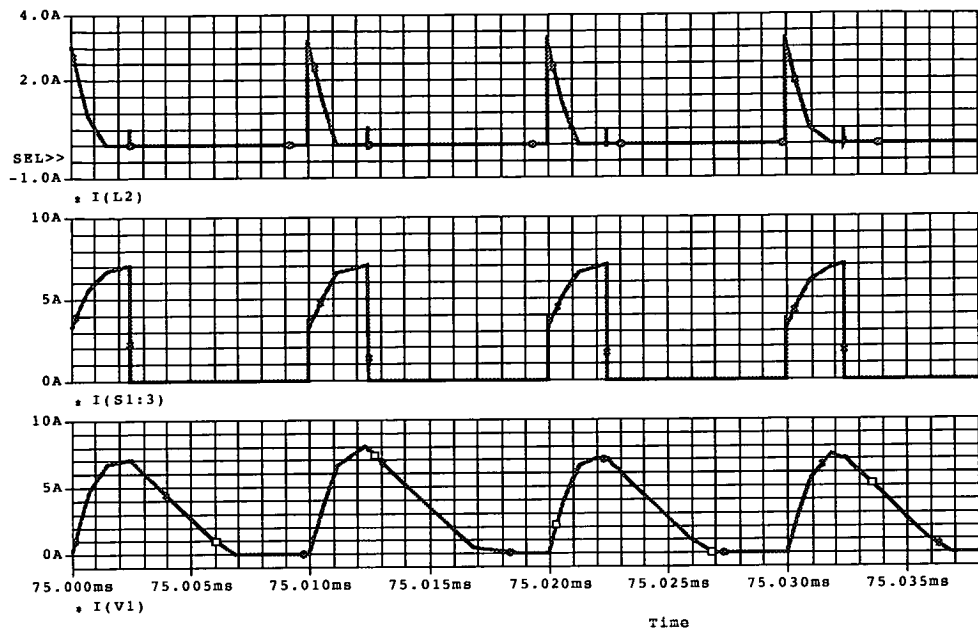
Figure 5.19: Switching frequency simulation results showing period 3 conduction for 100V and $L_1 = 10\mu$H. Top trace is the current in N_{1B} (or L_2 in the simulation), the centre trace is the current in S_1 and the bottom trace is the current in L_1.

The switching frequency current waveforms seen in the simulations are of the expected amplitude for a 150W output, as are the voltages measured at 265V. The voltages on the bulk capacitor are also similar to the predicted values as in table 5.3. Since the predicted voltages are for 100% efficiency and the simulation is not 100% efficient, the predicted values will be slightly different (but still within 10%) to those shown as the predicted values for 150W input and output power.

Through power/W	PSpice input power/W	Voltage MathCad/V	Voltage Pspice/V
$L_1 = 10\mu$H			
150W	168	353	354
$L_1 = 20\mu$H			
150W	170	369	369

Table 5.3: Predicted and simulated bulk capacitor voltages for 150W throughput power at 230V

91

5.6 Experimental Results

Figure 4.11 shows the final and complete circuit schematic tested, inductor L_1 is added between C_2 and the D_1 D_2 junction. The actual components used are listed in table G.1 in appendix G except L_1 which is $20\mu H$, and a photograph of the final circuit is shown in figure 5.20
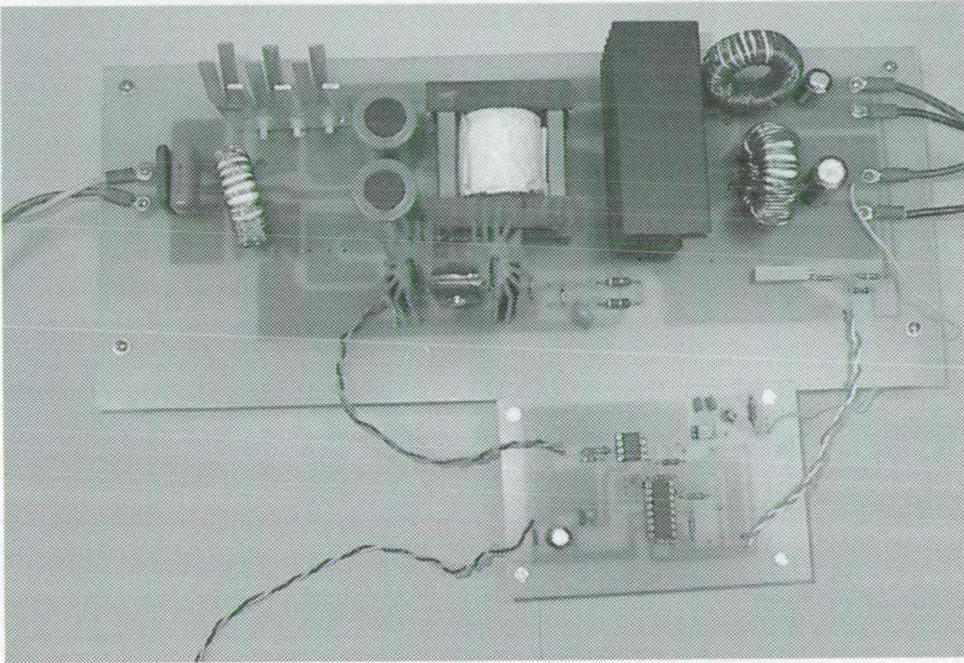
Figure 5.20: Photograph of the bi-forward converter with L_1

5.6.1 Changes Made to the Prototype Circuit

To see if the voltage seen across S_1 could be lowered a second transformer was wound during testing, after the design work was done, with $N_{1A} = 32$ and $N_{1B} = 12$ ($N_{1A} + N_{1B}$ is still 44 turns in total). The voltage expected across S_1 with this transformer would be lower as the total primary turns are only 12 turns more than the tertiary reset winding N_3. With the voltage on C_B going up to 425V this reduces the voltage seen on S_1 without a snubber to 1009V (which is below the MOSFET rating). Design curves are shown in appendix C.

5.6.2 Harmonic Tests

Shown in figures 5.21, 5.22, 5.23 and 5.24 are the harmonic plots compared to the class D regulations. The three different designs, L_1 equal to 10μH and 20 μH as well as 20μH with the alternative transformer design are all plotted together. The class D regulation values are compared to the values calculated for the converter with $L_1 = 20\mu$H and $N_{1A} = N_{1B} = 22$ turns. It was checked that doing this would not alter a pass or fail reading for the other two variations.
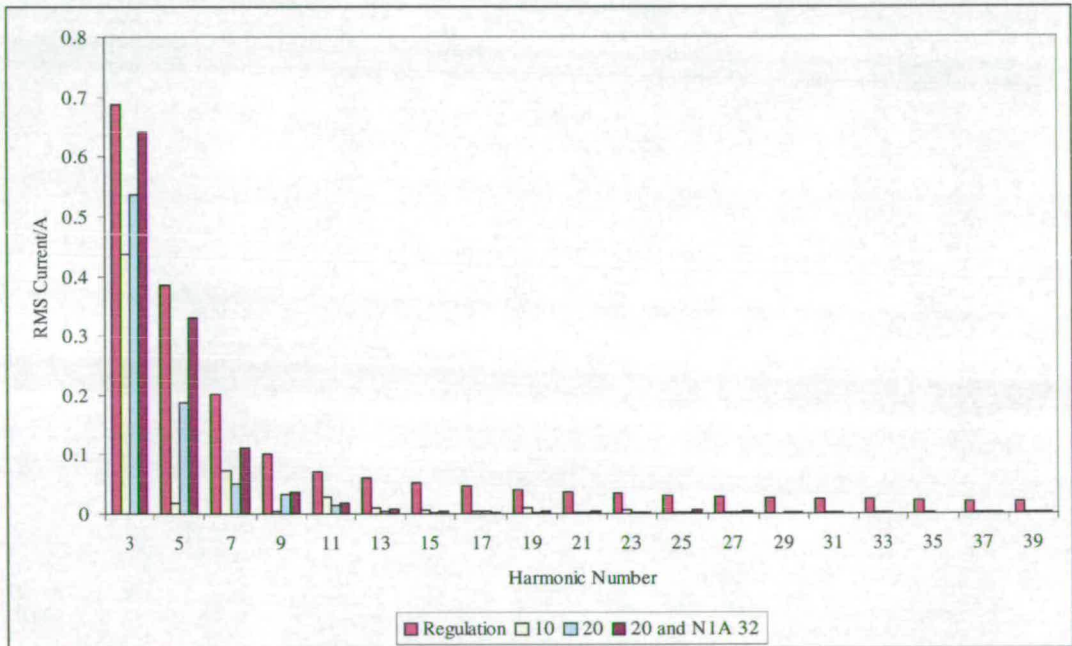
Figure 5.21: Measured RMS current harmonic levels for 230V and full load output compared to class D

At 230V and full load (150W output power) all three design variations are below the class D harmonic levels. At 230V and 75W input power (figure 5.22) with L_1 as 10μH the class D level for the 9th harmonic is exceeded by 0.0188A (class D is 0.039). The version with $N_{1A} = 32$ turns failed on the 9th, 11th and 13th harmonics by a considerable amount. The version with L_1 as 20μH was below all the class D levels.

In figure 5.23 the versions with L_1 as 10 and 20 μH at 100V and full load, the measured harmonics are below the class D values. With the transformer changed to $N_{1A} = 32$ turns the converter failed on the 9th, 11th, 13th and 15th harmonics.

In figure 5.24 for 100V and 75W input power all three variations were below the class D

93
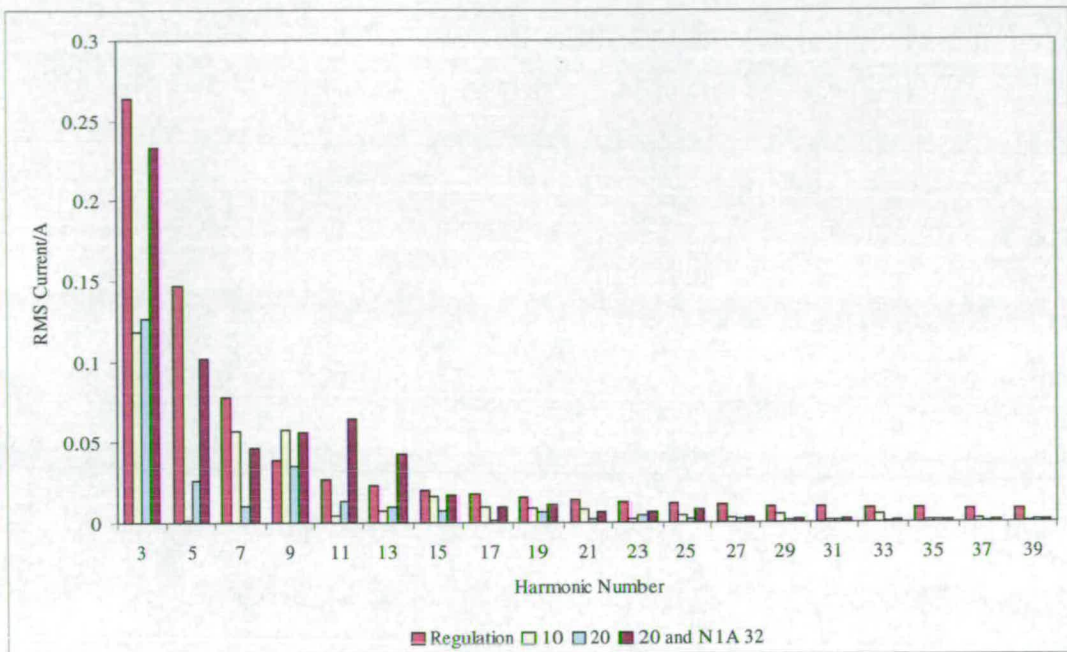
Figure 5.22: Measured RMS current harmonic levels for 230V and 75W input power compared to class D
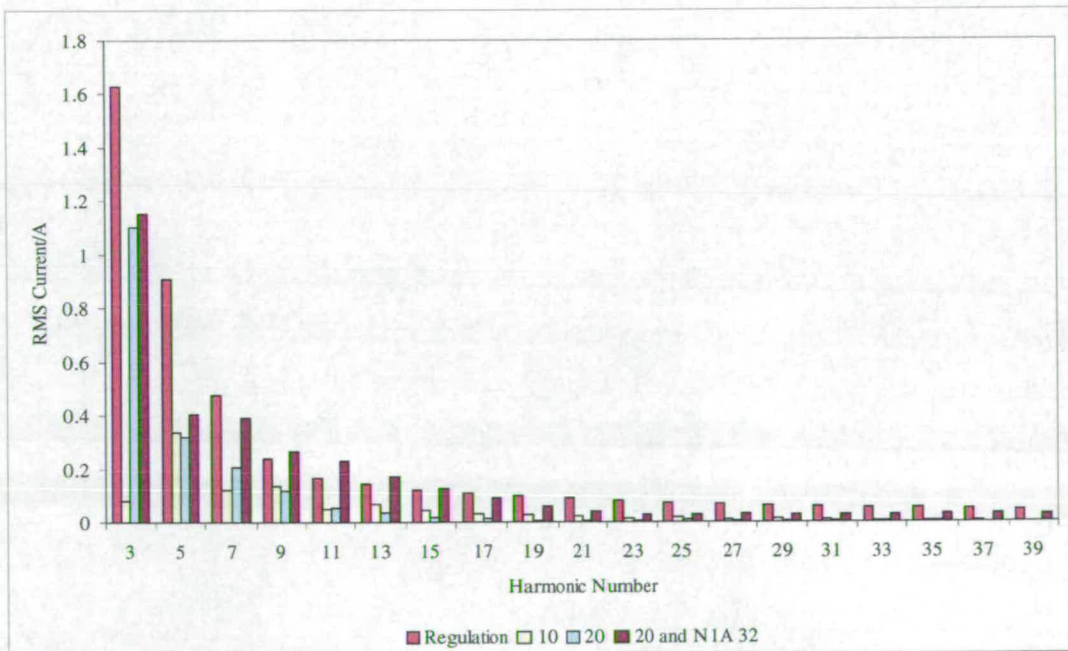
Figure 5.23: Measured RMS current harmonic levels for 100V and full load output compared to class D

regulation values.
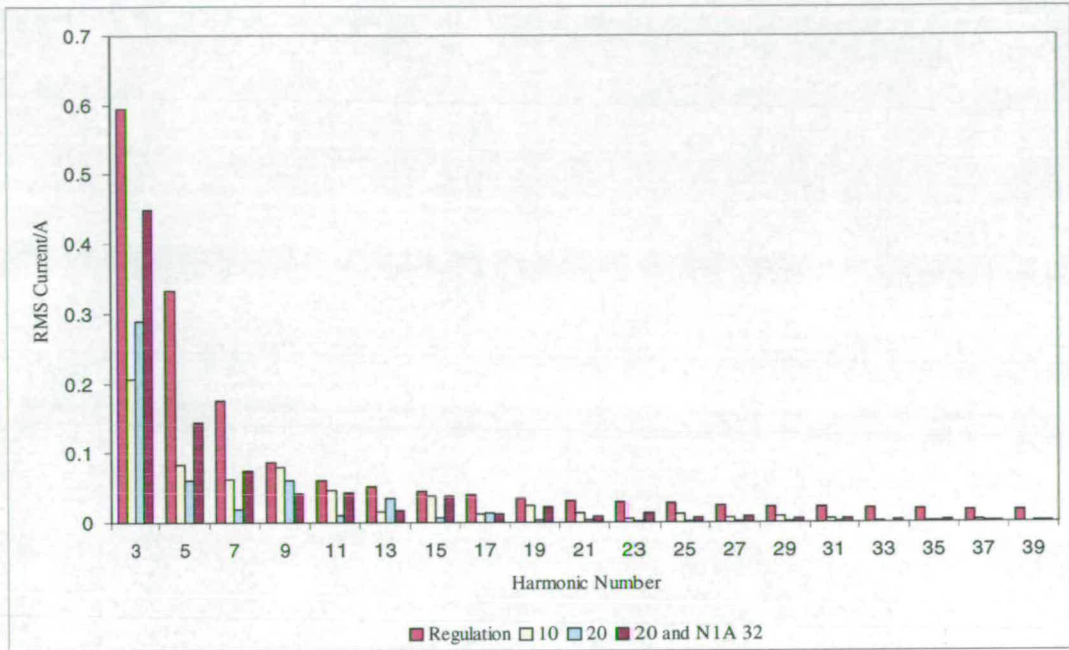
Figure 5.24: Measured RMS current harmonic levels for 100V and 75W input power compared to class D

The version with $N_{1A} = 32$ turns and $N_{1B} = 12$ turns failed the harmonic tests. This was because the conduction period of the input current is shorter since the input voltage at which period 2 starts is higher due to the turns ratio between N_{1A} and $N_{1A} + N_{1B}$ decreasing.

The only design that passes at both 75W and full load input power at both 100V and 230V is L_1 equal to $20\mu H$ with N_{1A} and N_{1B} equal to 22. Since this was the only version that passed the harmonic testing completely, it was decided to only test this design completely, even though the version with L_1 as $10\mu H$ only failed on one harmonic at 230V 75W input power. All 3 versions pass class A.

5.6.3   Input Current Waveform

Shown in figure 5.25 are the input current waveforms for L_1 equal to $20\mu H$ at 100V and 230V input voltage. The input current has had the switching frequency currents filtered out by the output transformer of the AC source, leaving only the line frequency current showing. In 5.25a is the input current at full load output power and 230V. From inspection of the current in L_1 (this is shown in figure 5.26a) the converter is operating only in periods

95

1 and 2. This is the same behaviour predicted in the simulation and the analysis. In 5.25b the input voltage is 230V with 75W input power. The shape of the current waveform (figure 5.25b) suggests the converter operated in periods 1, 2 and 3: this would also back up the analysis in section 5.4, which predicts the converter operating in these three periods with a 75W input power. Inspection of the current in L_1 at 83W confirmed operation in periods 1, 2 and 3. In 5.25c is shown the input current at full load and 100V input voltage. Investigating the L_1 current at 115V (not shown) shows the converter operating in periods 1, 2 and 2A modes. The waveform was similar in shape to that predicted by simulation and analysis for operation up to period 2A or 4A. The waveform leans to the left due to the bulk capacitor charging up. Figure 5.25d shows the input current at 100V with 75W input power. The waveform shape suggests operation in periods 1, 2 and 3, which the analysis backs up. Looking at the current in L_1, but at 115V, confirms that the converter is operating with period 3 conduction, but not period 4.

In figure 5.26 are shown switching frequency waveforms taken over the peak of the input voltage. In 5.26a (taken at full load and 230V) the current in L_1 can be seen to rise during the on time (shown in the top trace for V_{ds}) and then fall back to zero, before the next switching cycle starts. This shows that the converter is operating in period 2 and will not enter period 3. In 5.26b are the same waveforms but for a 75W input at 115V. In this case the current in L_1 is seen to rise from zero, until about halfway through the on period (shown in the top trace for V_{ds}) when it reaches the reflected load current and the slope becomes less steep. After turn off of S_1 the current in L_1 falls back to zero long before the next cycle starts. The converter is then operating in period 3. When the current in L_1 reaches the reflected load current, the current in L_1 actually falls for $3.96\mu s$, before it starts rising for 960ns when in series with L_2. Looking at the voltage waveform for D_1 (trace 3) it seems that D_1 becomes forward biassed (raising the voltage at that end of L_1 to the bulk capacitor voltage, hence current starts to fall) and on checking the current in D_1 (not shown), there is a small amount of current flowing through it (small ramp down from about 0.78A). This could be a resonance.

5.6.4   Voltage on the Bulk Capacitor C_B and Efficiency

In table H.1 in appendix H are the measured input and output powers, efficiency and bulk capacitor voltages. The efficiency and bulk capacitor voltage are plotted in figures 5.27 and
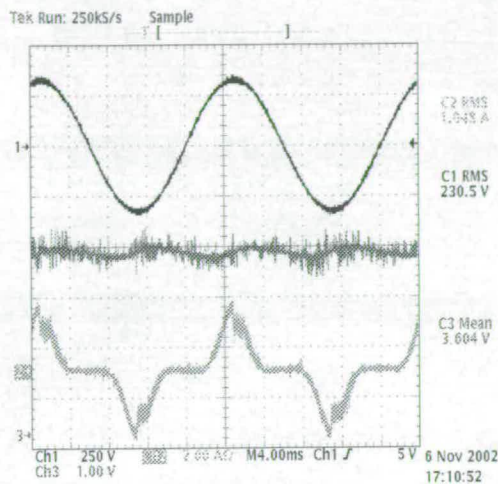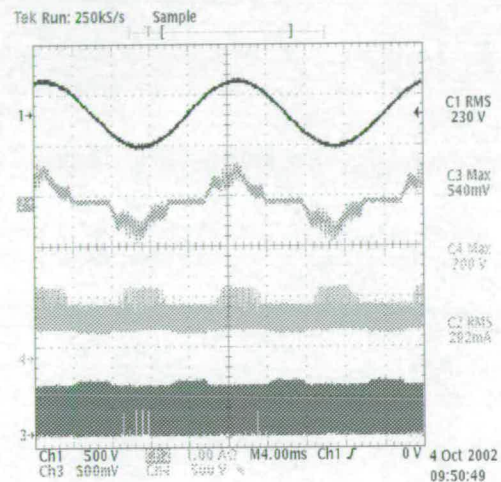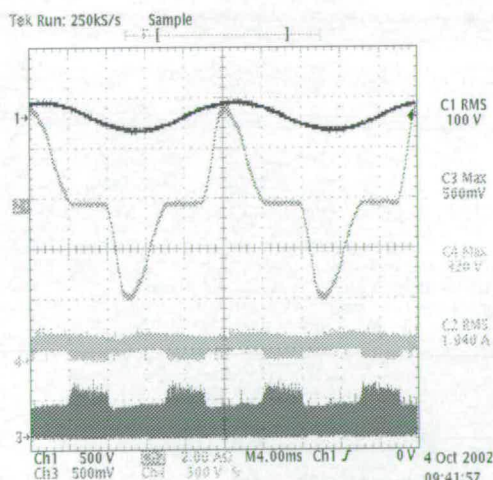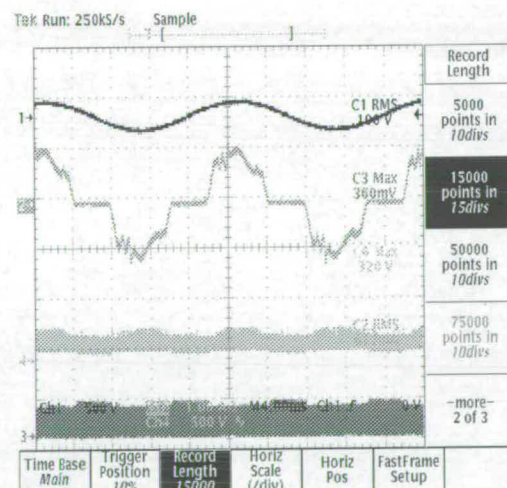
Figure 5.25: Measured a) filtered input current at full load and 230V, b) filtered input current at 75W and 230V, c) filtered input current at full load and 100V and d) filtered input current at 75W and 100V for L_1 as 20μH. Top trace input voltage, 2nd trace down input current (except a) where it is the voltage on C_B), 3rd trace down voltage across D_6 (except a) where it is input current) and bottom trace voltage across S_1.
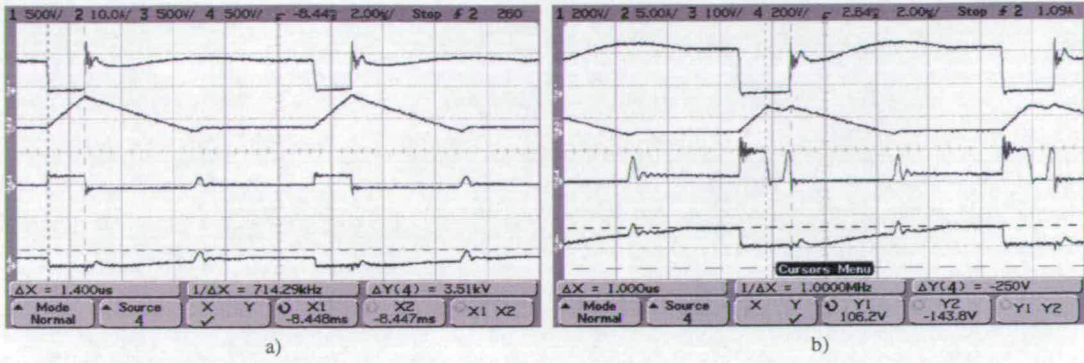
Figure 5.26: Measured a) Current in L_1 at full load and 230V, b) Current in L_1 at 75W and 115V taken over the peak of input voltage. Top trace: V_{ds} of S_1, 2nd trace down: I_{L1}, 3rd trace down: V_{D1} and the bottom: V_{D2}.

5.28 respectively.
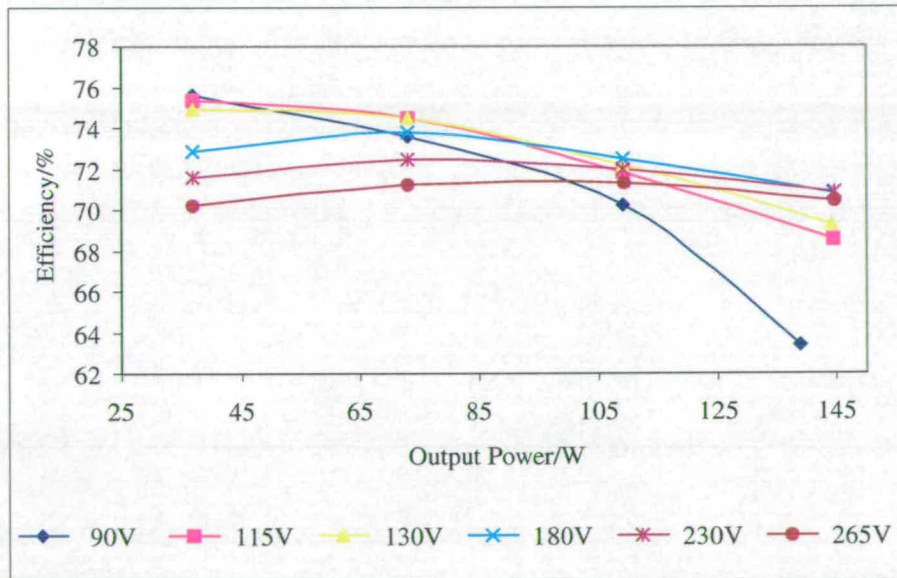
Figure 5.27: Efficiency of the bi-forward converter with input inductor L_1

At 90V input the efficiency falls from about 76% at 37W output to about 63% at 138W output. The final output power at 90V is low as the converter loses output regulation (duty cycle hits 0.5) towards the end of period 1 when C_B has been discharged. This can be solved by increasing the bulk capacitor value up from $165\mu F$ (two $330\mu F$ in series). Changing the bulk capacitor capacitance will not have a large effect on the average voltage seen across the bulk capacitor, as the voltage is determined by the balance of energy in and out of the capacitor, not its capacitance. A similar behaviour is seen at 115V and 130V where the

efficiency falls from about 75% at 37W output to 68% at 144W output. At 100V input and above the voltage on C_B does not fall sufficently low for the converter to lose regulation. When operating in the high voltage range the efficiency of the converter is just above 70%, being slightly lower at high output power and low output power. The efficency is acceptable, but a little low as ordinary fast recovery diodes have been used on the 5V output, instead of Schottky diodes which are normally used, due to the need to withstand higher voltages than in a normal forward converter.
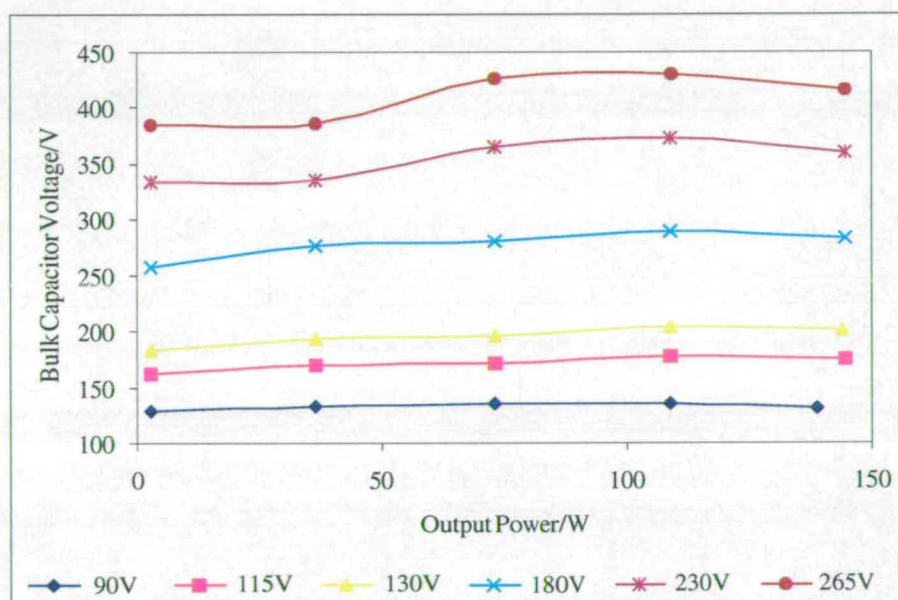
Figure 5.28: Variation of bulk capacitor voltage with output power at various voltages

The bulk capacitor voltage shown in figure 5.28 rises with input voltage, as expected. The peak value measured was 430V at 109W output at 265V input. The trend for variation of bulk capacitor voltage with power is a rise from low power and then a drop at full output power (about 144W). The reason for this is explained in section 5.4.3.

In figures 5.29 and 5.30 the measured bulk capacitor voltage is compared to the predicted voltage from MathCad. From 5.29 the predicted values are higher than the measured values for both 90V and 115V, with the difference increasing as the input power goes up. The difference between the predicted values and measured values is less than 10%, except for full input power at 115V where it is 11%. This is considered to be reasonable estimation of the bulk capacitor voltage on the low input voltage range. Shown on 5.30 the predicted values are lower at high input power (about 200W) and low input power (about 50W). In
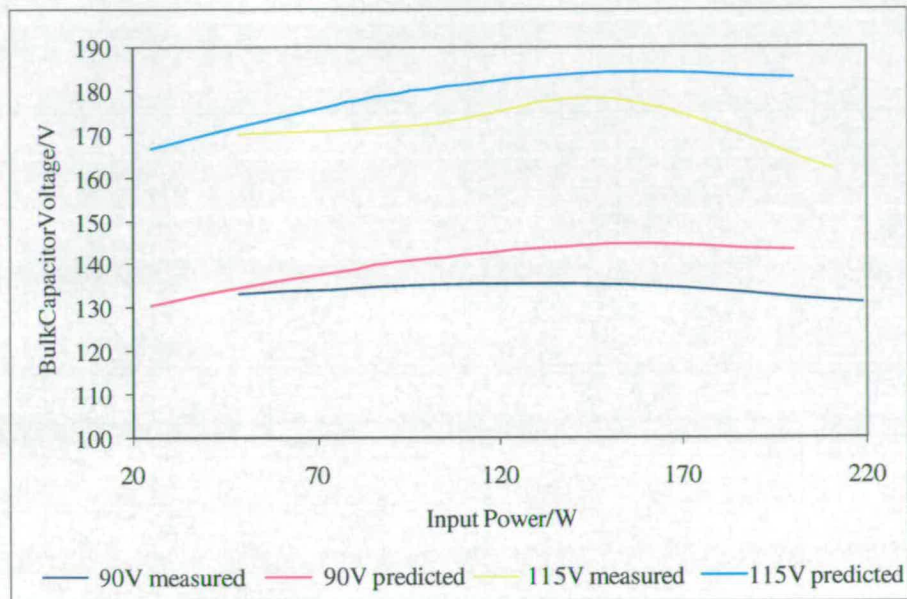
Figure 5.29: Variation of bulk capacitor voltage with input power on the low voltage range compared to predicted bulk capacitor voltage
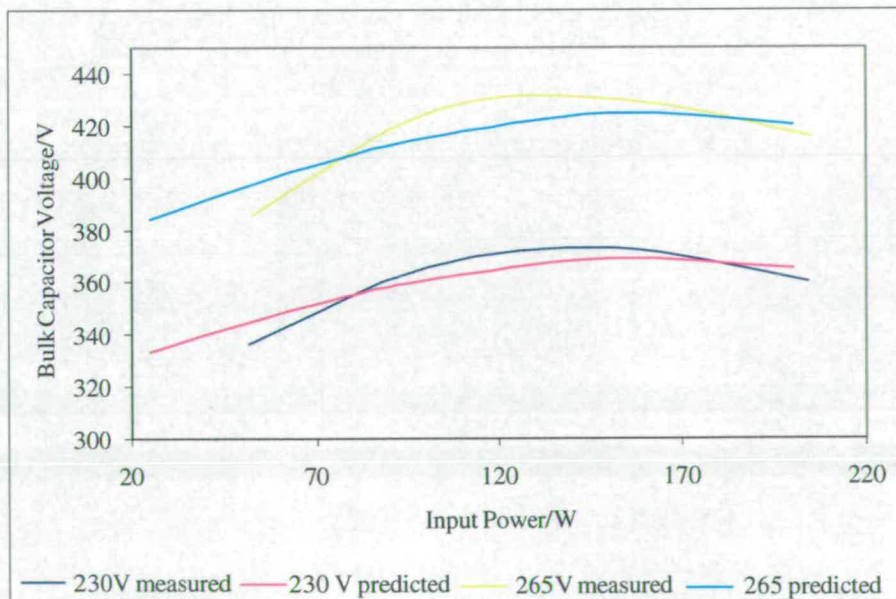
Figure 5.30: Variation of bulk capacitor voltage with input power on the high voltage range compared to predicted bulk capacitor voltage

the middle of the power range the predicted voltage values are higher than the measured values. The shape of the predicted voltage and measured voltage curves are similar. The difference between predicted bulk capacitor voltage and measured bulk capacitor voltage is less than 3%, which is again considered acceptable.

In table 5.4 are the voltages measured on C_B for $L_1 = 10\mu H$ and $N_{1A} = 32$ turns taken while carrying out the harmonic level measurements. These measurements are to show that the other two designs, while not passing all the current harmonic tests, could have lower voltage stress on the bulk capacitor and hence other components in the circuit. For L_1 equal to $10\mu H$ the voltage for full load at 230V is actually higher than for L_1 equal to $20\mu H$ by about 13V. If the graph in figure 5.14 is extended, it would predict a similar result. At about 75W input the voltage on C_B is lower (this is also seen in figure 5.14).

For the version with N_{1A} equal to 32 turns the voltage seen on C_B is lower than that with N_{1A} equal to 22 turns by about 20V to 30V. In the version with $N_{1A} = 32$ turns the reflected secondary current is lower so the converter is more likely to operate in period 3 and a lower amount of energy is delivered to C_B during the off periods since the current is not so high.

Setting	Voltage/V
$L_1 = 10\mu H$	
100V 72.98W in	149
100V 211W in	150
230V 75.7W in	338
230V 212W in	376
$L_1 = 20\mu H$ $N_{1A} = 32$	
100V 75.3W in	136V
100V 192W in	131V
230V 82W in	322V
230V 188.7W in	332V

Table 5.4: Voltage measured across bulk capacitor C_B with $L_1 = 10\mu H$ and with $L_1 = 20\mu H$ and $N_{1A} = 32$

5.6.5 Hold Up Time and Output Voltage Ripple

Hold Up Time

Hold up time is how long the converter can operate until the loss of output voltage regulation after the loss of the input voltage. This was measured from the loss of the input supply until

the point that the 5V output voltage started to drop at full output load of 5V 20A and 12V 4A. It was not possible to control the precise point that the input voltage was lost so these numbers are approximate. The ideal test point for this is just before the bulk capacitor starts recharging. Hold up time is normally at least 10ms for a PC power supply.

Input Voltage/V	Hold up time/ms
115	8.6
230	48.6

Table 5.5: Hold up times for 115V and 230V

Hold up time is short at 8.6ms for 115V input as the voltage on C_B does not have to fall far before regulation is lost. The opposite is true for the 230V reading. Increasing the size of the bulk capacitor will improve the hold up time for low line.

Output Voltage Ripple

The output voltage ripple was measured on both the 5V and 12V output at both 75W output load and full output load (150W) at the same input voltages as for the efficiency measurements.

The output voltage ripple seen on the two outputs are shown in table 5.6. Some are higher than normally specified for a PC power supply (50mV peak to peak maximum on the 5V output and 120mV peak to peak on the 12V output), but then this was not an important design consideration for the prototype converter. The 100kHz ripple on the 5V output ranges from about 45mV to 65mV on the 5V output and from 109mV to 165mV on the 12V output. This is not the only ripple seen at the output of the converter as there is also a 100Hz ripple ranging from about 15mV to 50mV on the 5V output and 47mV to 115mV on the 12V output. This ripple appears partly from the control loop being overdamped and partly from having the two different voltage sources, $v_s(t)$ and C_B.

5.6.6 Voltage seen on key devices

The voltages on S_1 and the various diodes are shown in table 5.7, measured at 265V.

The voltage seen across S_1 is only 830V, much lower than the possible 1275V that could

Output Combination	5V 100kHz p-p Ripple /mV	5V 100Hz p-p Ripple /mV	12V 100KHz p-p ripple /mV	12V 100Hz p-p Ripple /mV
Input Voltage: 90V				
5.17V 10.2A, 11.54V 1.9A	45	50	109	115
4.96V 19.9A, 11.78V 3.9A	33	938	90.6	2.18
Input Voltage: 115V				
5.17V 10.4A, 11.57V 2A	62	45.3	109	87.5
5.05V 19.4A, 12.02V 3.9A	45.3	28.1	112	75
Input Voltage: 130V				
5.17V 10.2A, 11.56V 1.9A	42.2	40.6	103	87.5
5.05V 19.4A, 11.56V 1.9A	50	29.7	112	59.4
Input Voltage: 180V				
5.16V 10.2A, 11.54V 2A	68.8	50	116	100
5.01V 20.4A, 11.97V 3.9A	48.4	31.3	115	59.4
Input Voltage: 230V				
5.15V 10.2A, 11.51V 2A	48.4	35.9	115	78.1
5.04V 20.4A, 12.00V 3.9A	90	15.6	165	46.9
Input Voltage: 265V				
5.14V 10.2A, 11.52V 2A	53.1	28.1	109	53.1
5.04 20.4A, 11.99V 3.8A	65.6	15.6	156	56.3

Table 5.6: Peak to peak ripple voltage on output voltages

Device	Voltage/V
S_1	830
D_1	188
D_2	438
D_3	469
$D_{4:5V}$	25
$D_{5:5V}$	89
$D_{5:12V}$	222

Table 5.7: Voltage measured across key semiconductor components with 265V input voltage

occur. This is due to the MOSFET snubber (figure 4.11) resetting the transformer instead of the tertiary winding N_3. At low voltages of around 100V input and higher power (144W output) the reset winding is still resetting the transformer instead of the snubber. The voltage seen across $D_{5:5V}$ at 89V is lower than the predicted 96V and across $D_{5:12V}$ at 222V is higher than the predicted 213V, but both are within 10% of the predicted value. $D_{4:5V}$ has only 25V across it (maybe allowing the use of a Schottky diode). The blocking voltages for D_1 to D_3 were not calculated for this version of the bi-forward as 1000V diodes were already being used, and the voltage was never expected to go that high.

5.7 Conclusions

Analysis has been produced that predicts the bulk capacitor voltage, input current shape and input current harmonics reasonably well. It can be used to test designs with different values of L_1, different turns ratios and any power where L_2 is in CCM. PSpice simulation of the circuit has been carried out, to confirm the analysis.

A prototype converter has been built with L_1 as 20μH that passes class D with acceptable efficiency. However V_{CB} is very high and the circuit will not operate in all the conduction modes mentioned in [95]. The same prototype, but with L_1 as 10μH produced a more satisfactory input current waveform with more consistent operation periods, but failed on just one harmonic setting at 100V and 75W input power. A final design to see if bulk capacitor voltage could be lower with N_{1A} as 32 and N_{1B} as 12 performed badly on the harmonics but had a lower bulk capacitor voltage. The design with L_1 as 20μH and $N_{1A} = N_{1B} = 22$ was investigated further and voltage on the bulk capacitor was found to rise to 430V and the voltage across S_1 was 830V, $D_{5:5V}$ was 89V and $D_{5:12V}$ was 222V. The efficiency was found to be above 68% when operating properly. It was also found that 100Hz ripple appeared on the output voltage. To meet hold up time requirements and to operate correctly at 90V the size of the bulk capacitor needs to be increased.

When power is increased it is difficult to produce a design that has low voltage on C_B and will operate in period 4 in the way [95] intended and meet IEC 61000-3-2 class D. Due to this the behaviour of the circuit, when operating in particular combinations of conduction of L_1, has been investigated and the effects on current harmonics and bulk capacitor voltage shown. In particular it is noted that when not operating in period 4 the voltage on the bulk

capacitor rises to a very high level.

The use of snubber transformer reset, instead of a tertiary winding, where the voltage seen by S_1 is up to three times V_{CB}, is advised as this allows the use of a lower voltage MOSFET for S_1 even when the bulk capacitor voltage is high.

Chapter 6

High Frequency Current Source Single-Stage PFC Converter (CS S^{2}PFC)

6.1 Development of the High Frequency Current Source Single-Stage Converter

In an attempt to produce an off-line converter with low cost and high efficiency with an input current harmonic content which can meet IEC 61000-3-2, Sebastian et al in [120] introduced a single stage PFC converter based on the concept of the series connection of a loss free resistor and a voltage source.

6.1.1 The Series Connection of a Loss Free Resistor and a Voltage Source Concept

In figure 6.1 is shown the concept of a Loss Free Resistor (LFR) in series with a voltage source. If the input voltage $v_s(t) < V_B - V_{SS}$, which will occur around the zero crossing area, then the diode bridge DB will be reverse biased and no input current will flow. When $v_s(t)$ has risen to $v_s(t) = V_B - V_{SS}$ the diode will just be able to start conducting. When $v_s(t) > V_B - V_{SS}$ the diode bridge is conducting and the input current is:
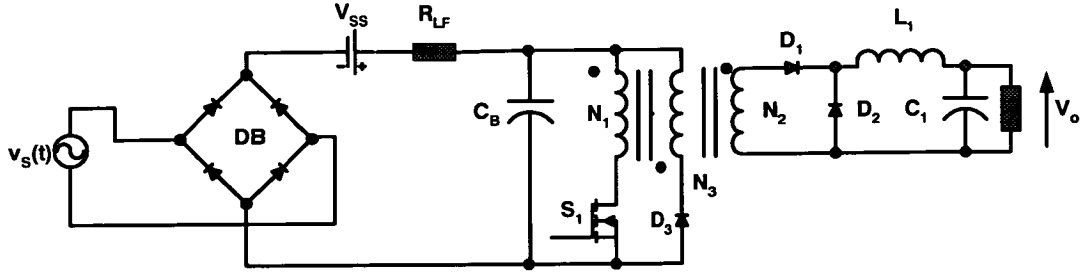
Figure 6.1: Loss free resistor and voltage source PFC converter

$$i_s\left(t\right) = \left(v_s\left(t\right) + V_{SS} - V_B\right)/R_{LF}.$$

6.1.2 The Practical Implementation of the Series Connection Loss Free Resistor and a Voltage Source

The practical implementation of the series connection of a loss free resistor and a voltage source applied to the forward converter is shown in figure 6.2. It is basically a forward output stage operating mainly in CCM with an additional inductor L_D in series with the forward diode D_4 placed on the input of the converter. The inductor L_D is used to extend the freewheeling time of diode D_4. This configuration produces an input current similar to that of the LFR.
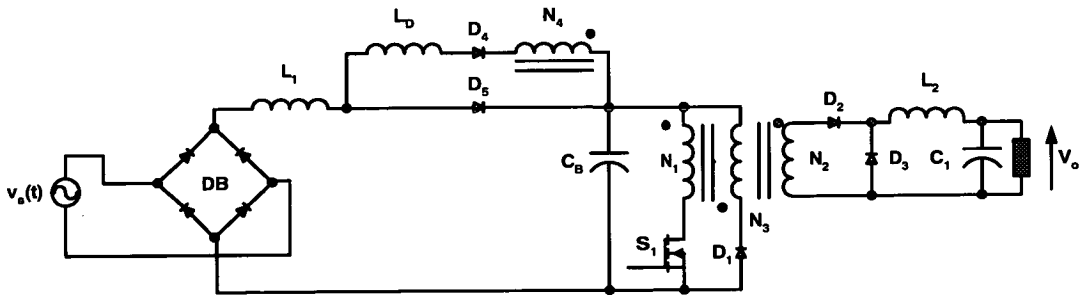
Figure 6.2: Loss free resistor and voltage source PFC converter or Current Source Single Stage PFC Converter (CS S^{2}PFC)

The CS S^{2}PFC converter proposed in [120] is designed to operate with the input and output inductors L_1 and L_2 in CCM. This means that the voltage on C_B is expected to rise as the input voltage goes up and as the load goes down, but it does appear the voltage on C_B can be maintained at a reasonable level.

6.1.3 Application of a Voltage Doubler Scheme

A voltage doubler is considered desirable as this gives a smaller voltage range across the bulk capacitors when operating from 115V range. This means the transformer can be designed to operate over a smaller voltage range leading to a more optimised design with smaller duty cycle range. An advantage for the PFC circuit is that a doubler circuit can be included, thus it will be able to perform reasonably well on both input voltage ranges.

In [120] to enable the converter to operate from both the 90V-130V and 180V-265V ranges and still have an input current that meets IEC 61000-3-2, the switching frequency is halved on the high line range.
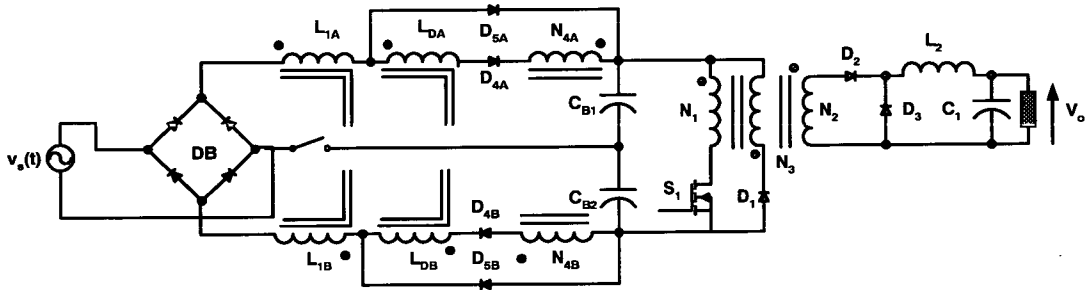
Figure 6.3: CS S^{2}PFC converter with voltage doubler

Based on the scheme presented in [121], [122] produced the version of the converter seen in figure 6.3. When the switch is open the converter is operated from the high voltage range of 180V to 265V. The A and B sides of the PFC circuit connect in series and operate together. As the A and B side inductors are coupled the inductance of the complete winding is four times higher than either L_{1A} or L_{1B} or L_{DA} or L_{DB}. When the switch is closed the A and B side inductors work independently. When the line voltage is positive the A side functions delivering energy to just C_{B1}. When the line voltage is negative the B side functions delivering charge to C_{B2}.

It was decided to investigate and build the voltage doubler version of the CS S^{2}PFC converter. This version was chosen as it is more likely to meet the harmonic regulations at both 100V and 230V and because of the advantages of the voltage doubler mentioned above.

6.2 Operation of the High Frequency Current Source Single-Stage Converter

6.2.1 Operation at Line Frequency

Shown in figure 6.4 is a conceptual average input current waveform over a half line cycle drawn by the circuit in figures 6.2 (or 6.3). The waveform shown is produced whether the converter is operating in voltage doubler mode or normal mode.
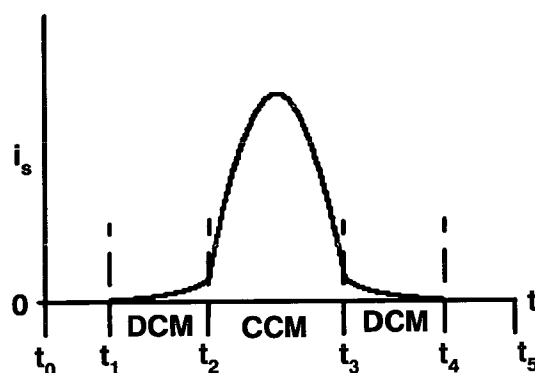
Figure 6.4: Conceptual average input current

From t_0 to t_1 and t_4 to t_5 the current in L_1 is zero and hence the input current is also zero. Inspecting figure 6.2 the current in L_1 can only rise when the voltage at the D_4 end of N_4 in figure 6.2 (when S_1 is turned on) is lower than the input voltage $v_s(t)$. During the zero crossing area the input voltage $v_s(t)$ is lower than that at the D_4 N_4 point. From t_1 to t_2 and t_3 to t_4 the current in L_1 is operating in DCM. $v_s(t)$ is now higher than the voltage at the D_4 N_4 point so current in L_1 (and L_D) can rise, but since the voltage across the inductors is low the current does not rise very far and can reset before the next switching cycle. From t_2 to t_3 the current in L_1 is operating in CCM. Now $v_s(t)$ and the load are high enough so, that the current in L_1 cannot fall to zero in a switching cycle. Operation in the DCM and CCM periods is described in detail in the next section.

6.2.2 Operation at Switching Frequency

DCM

Shown in figure 6.5 are important waveforms for when the input current shaper is operating in DCM.
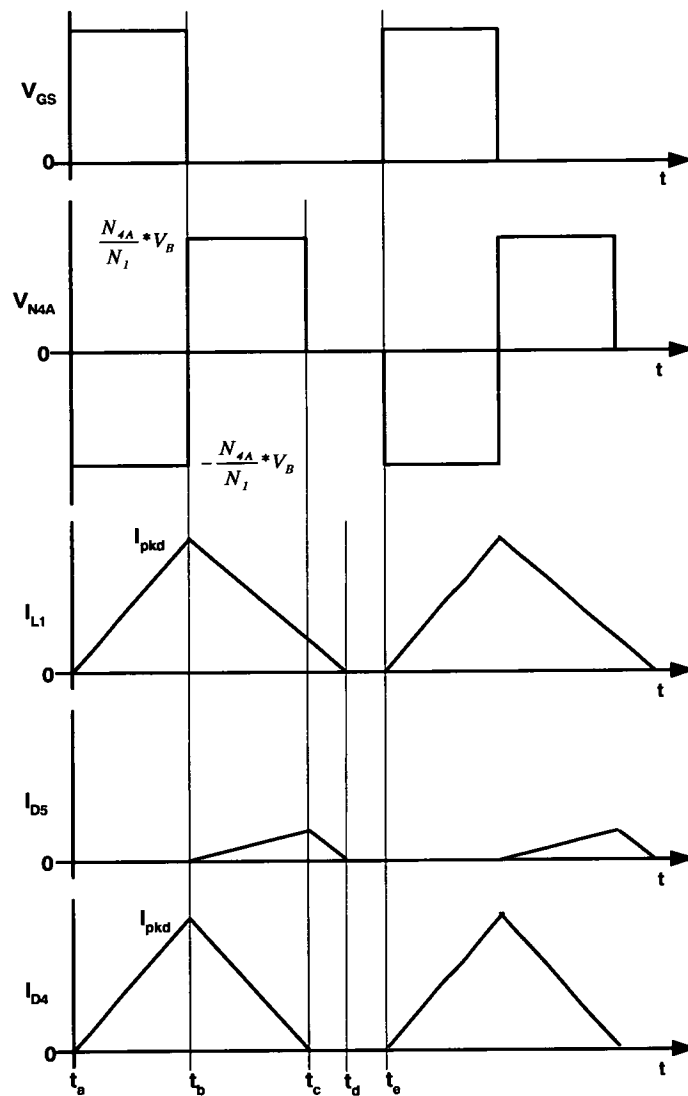
Figure 6.5: Waveforms in the current shaper at switching frequency when operating in DCM

t_a to t_b

At t_a S_1 is turned on. The secondary and the load are supplied from C_B via N_1. A negative voltage is applied across N_4 reducing the voltage at the D_4 end to $V_B - V_{N4}$. The input voltage $v_s(t)$ is higher than this, so current in L_1 and L_D in series ramps up from zero.

t_b to t_c or t_d

At t_b S_1 is turned off. The current in the secondary now freewheels.

t_d to t_e

All the primary current has reset to zero. Only the secondary freewheeling current is flowing.

CCM

Shown in figure 6.6 are important waveforms for the input current shaper when operating in CCM.

t_a to t_b

At t_a, S_1 is turned on. The secondary and the load are supplied from C_B via N_1. A negative voltage is applied across N_4 reducing the voltage at the D_4 end to $V_B - V_{N4}$. The current in L_1 is freewheeling (decreasing) via D_5 to C_B, hence the voltage at the L_1 and L_D junction is at V_B. Current in L_D starts to ramp up from zero. The current flowing in D_5 starts to commutate to the D_4 branch as the current in L_D increases.

t_b to t_c

At t_b the current in L_D has risen to that in L_1 and D_5 stops conducting. L_1 and L_D connect in series and the current in the pair now ramps up. The charging current in L_1 has effectively shortened the "on" time of L_1 by $t_b - t_a$.
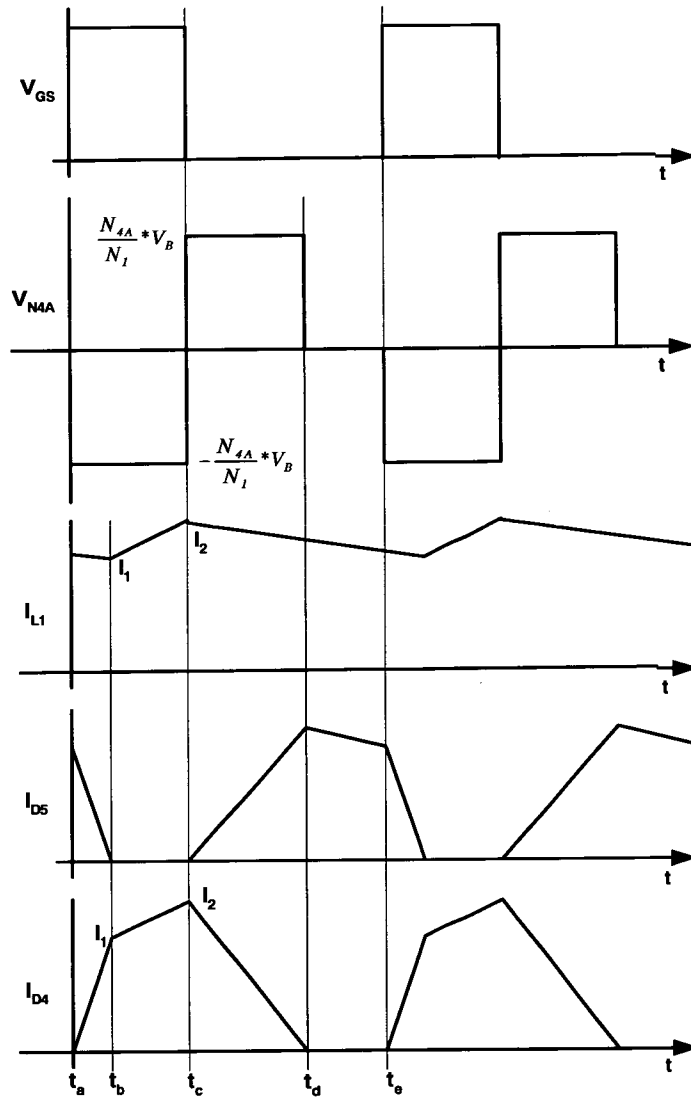
Figure 6.6: Waveforms in the Current Shaper at Switching Frequency when operating in CCM

112

t_c to t_d

At t_c S_1 is turned off. The secondary current is now freewheeling. An opposite voltage is induced across N_4 as the transformer resets, raising the voltage at D_4 above the capacitor voltage V_B. This voltage is also higher than $v_s(t)$ and the current in L_1 and L_D starts to ramp down, but at a different rate. D_5 has now become forward biassed: the voltage across L_1 is $v_s(t) - V_B$ and that across L_D is V_{N4}. The current in L_1 is split between the D_5 and D_4 paths. L_D reaches zero at t_d and stops conducting. The current in L_1 keeps on freewheeling via D_5.

t_d to t_e

The current in L_1 and on the secondary keep on freewheeling. At t_e the next cycle starts when S_1 is turned on again and the process repeats.

L_1 and L_D in CCM

If L_D is too large it will enter CCM over the peak of the mains. It is undesirable to operate the converter in this condition as the current waveform becomes distorted and reduces its chance of passing the class D harmonics. The design should avoid this if possible.

6.3   Analysis

In [120] and [39] analysis was carried out by Sebastian based on the loss free resistor and voltage source, but when this method was attempted, it was not able to produce the design shown in the later work of Zhang in [122]. The loss free resistor method was producing designs with values of inductance in mH, not in μH which the work in [122] was using. Because of this the following analysis was carried out.

To further understanding, and to assist with the design of a prototype of the circuit, a detailed analysis was carried out. When carrying out the analysis for operation in normal mode (switch open, high voltage range) the A and B PFC cells can be combined and considered as a single unit. Hence the inductances L_{DA} and L_{DB}, L_{1A} and L_{1B} and the turns on the

113

transformer N_{4A} and N_{4B} can be combined into single values. In voltage doubler mode, when the A and B cells operate alternately on either the positive or negative part of the cycle, only a single cell needs considering. The analysis only considers the converter with a single output. In this topology this does not matter as the PFC current and the output current do not interact.

In addition to the assumptions made in section 4.3.2 the following assumptions are made:

1. Bulk capacitor voltage is constant over a mains cycle.

2. The input voltage is constant over a switching cycle.

For the analysis when operating in normal mode with the switch open, the inductances L_D and L_1 can be considered to be as in equations 6.1 and 6.2. The times four factor is due to the A and B inductances being coupled. The A and B turns add up as in equation 6.3.

$$L_D = 4 \cdot L_{DA} = 4 \cdot L_{DB} \tag{6.1}$$

$$L_1 = 4 \cdot L_{1A} = 4 \cdot L_{1B} \tag{6.2}$$

$$N_4 = 2 \cdot N_{4A} = 2 \cdot N_{4B} \tag{6.3}$$

When operating in voltage doubler mode L_1, L_D and N_4 are:

$$L_D = L_{DA} = L_{DB} \tag{6.4}$$

$$L_1 = L_{1A} = L_{1B} \tag{6.5}$$

$$N_4 = N_{4A} = N_{4B} \tag{6.6}$$

Since the CS S^2PFC is a forward converter and it is the capacitor voltage V_B that is seen across the transformer primary, the duty ratio D is:

$$D = \frac{N_1}{N_2} \cdot \frac{V_o}{V_B} \tag{6.7}$$

where V_B is the bulk capacitor voltage.

The input voltage $v_s(t)$ is assumed to be sinusoidal and is expressed in equation 6.8.

$$v_s(t) = V_{pk} \cdot \sin(\omega \cdot t) \tag{6.8}$$

where

$$\omega = 2 \cdot \pi \cdot F \tag{6.9}$$

and F is the line frequency.

6.3.1   Analysis when Operating in DCM for One Switching Cycle

From examining figure 6.4, the current in L_1 (unfiltered input current) is discontinuous from t_1 to t_2 and t_3 to t_4. If the input current is low (ie low power throughput) then L_1 will not enter CCM. Looking at figures 6.5 and 6.2 when S_1 is on (t_a to t_b), applying the inductor equation ($v = L \cdot \frac{di}{dt}$) to L_1 yields:

$$v_s(t) - \left[1 - \frac{N_4}{N_1}\right] \cdot V_B = \frac{(L_1 + L_D) \cdot I_{pkd} \cdot f_s}{D} \tag{6.10}$$

Rearranging equation 6.10 to give the peak current, I_{pkd}, in L_1 gives:

$$I_{pkd} = \frac{\left[v_s(t) - \left(1 - \frac{N_4}{N_1}\right) \cdot V_B\right] \cdot D}{(L_1 + L_D) \cdot f_s} \tag{6.11}$$

When S_1 turns off the current in L_1 and L_D falls to zero. Considering the inductor equation for L_1

$$v_s(t) - V_B = \frac{-I_{pkd} \cdot L_1 \cdot f_s}{D_f} \qquad (6.12)$$

where f_s is the switching frequency.

Rearranging 6.12 to give the current fall duty ratio D_f for L_1:

$$D_f = \frac{L_1 \cdot I_{pkd} \cdot f_s}{V_B - v_s(t)} \qquad (6.13)$$

The average current in L_1, I_{avd}, during DCM is:

$$I_{avd} = \frac{D + D_F}{2} \cdot I_{pkd} \qquad (6.14)$$

The DCM period starts at t_1 after a period of no conduction during the zero crossing. The period of no conduction occurs while:

$$v_s(t) \geq \left(1 - \frac{N_4}{N_1}\right) \cdot V_B \qquad (6.15)$$

The moment $v_s(t)$ rises above $\left(1 - \frac{N_4}{N_1}\right) \cdot V_B$ the DCM period can start, hence the time t_1 can be found from:

$$t_1 = \frac{\sin^{-1}\left[\frac{V_B}{V_{pk}} \cdot \left(1 - \frac{N_4}{N_1}\right)\right]}{w} \qquad (6.16)$$

6.3.2 Analysis when Operating in CCM For one Switching Cycle

In figure 6.4 the current in L_1 enters the CCM stage at t_2. Looking at figures 6.6 and 6.2 the current in L_1 keeps falling until the current in L_D ramps up to meet it. From t_a to t_b the inductor equation for L_D is expressed in equation 6.17. ΔD is the ratio of $(t_b - t_a)/(t_e - t_a)$ or the duty cycle of that part of the cycle.

$$\frac{N_4}{N_1} \cdot V_B = \frac{I_c \cdot L_D \cdot f_s}{\Delta D} \qquad (6.17)$$

Rearranging this gives the current, I_c, at which L_1 and L_D have the same current flowing in them:

$$I_c = \frac{N_4 \cdot V_B \cdot \Delta D}{N_1 \cdot L_D \cdot f_s}$$

(6.18)

At t_b L_1 and L_D connect in series and the overall inductor equation is:

$$v_s(t) - \left(1 - \frac{N_4}{N_1}\right) \cdot V_B = \frac{(L_1 + L_D) \cdot \Delta I_c \cdot f_s}{D - \Delta D}$$

(6.19)

Rearranging gives ΔI_c, the current rise in L_1 from t_b to t_c:

$$\Delta I_c = \frac{\left[v_s(t) - \left(1 - \frac{N_4}{N_1}\right) \cdot V_B\right] \cdot (D - \Delta D)}{(L_1 + L_D) \cdot f_s}$$

(6.20)

From t_c to t_b on the next cycle the current in L_1 is freewheeling and this is governed by the inductor equation:

$$v_s(t) - V_B = \frac{-\Delta I_c \cdot L_1 \cdot f_s}{1 - D + \Delta D}$$

(6.21)

If 6.19 and 6.21 are equated then ΔD can be found.

$$\frac{\left[v_s(t) - \left(1 - \frac{N_4}{N_1}\right) \cdot V_B\right] \cdot (D - \Delta D)}{L_1 + L_D} = \frac{(V_B - v_s(t)) \cdot (1 - D + \Delta D)}{L_1}$$

(6.22)

Rearranging 6.22:

$$\Delta D = \frac{D \cdot L_1 \cdot \left[v_s(t) - \left(1 - \frac{N_4}{N_1}\right) \cdot V_B\right] + (L_1 + L_D) \cdot [v_s(t) - V_B + D \cdot (V_B - v_s(t))]}{\left[v_s(t) - \left(1 - \frac{N_4}{N_1}\right) \cdot V_B\right] \cdot L_1 + (L_1 + L_D) \cdot (V_B - v_s(t))}$$

(6.23)

For L_1 to enter CCM, ΔD has to be greater than zero. This condition is fulfilled when the numerator of 6.23 is greater than zero. Rearranging the numerator of 6.23 gives:

$$v_s\left(t\right) \geq \frac{V_B \cdot \left[D \cdot L_1 \cdot \left(1 - \frac{N_4}{N_1}\right) + \left(L_1 + L_D\right) \cdot \left(1 - D\right)\right]}{\left(L_1 + L_D\right) - D \cdot L_D} \qquad (6.24)$$

This equation can then be solved to give t_2 (figure 6.4):

$$t_2 = \frac{\sin^{-1}\left[\frac{V_B}{V_{pk}} \cdot \frac{D \cdot L_1 \cdot \left(1 - \frac{N_4}{N_1}\right) + \left(L_1 + L_D\right) \cdot \left(1 - D\right)}{\left(L_1 + L_D\right) - D \cdot L_D}\right]}{w} \qquad (6.25)$$

The average current in L_1, I_{avc}, for one switching cycle is:

$$I_{avc} = I_c + \frac{\Delta I_c}{2} \qquad (6.26)$$

6.3.3 Analysis at Line Frequency

At line frequency the input power and input current of the converter needs to be considered.

The input power, P_{in}, is:

$$P_{in} = \frac{2}{T} \cdot \int_{t_1}^{t_2} I_{avd}\left(t\right) \cdot v_s\left(t\right) dt + \frac{2}{T} \cdot \int_{t_2}^{\frac{T}{2}} I_{avc}\left(t\right) \cdot v_s\left(t\right) dt \qquad (6.27)$$

where T is the half line period.

When the input power is low L_1 only operates in DCM, and the input power can be expressed by:

$$P_{in} = \frac{2}{T} \cdot \int_{t_1}^{\frac{T}{2}} I_{avd}\left(t\right) \cdot v_s\left(t\right) dt \qquad (6.28)$$

The input current can be formed piecewise from the various current modes of L_1. For a half cycle of the mains the input current is defined in equation 6.29 and in equation 6.30 for operation in just DCM.

118

$$i_s(t) = \begin{cases} 0 & 0 < t < t_1 \quad t_4 < t < t_5 \\ I_{avd}(t) & t_1 < t < t_2 \quad t_3 < t < t_4 \\ I_{avc}(t) & t_2 < t < t_3 \end{cases} \qquad (6.29)$$

$$i_s(t) = \begin{cases} 0 & 0 < t < t_1 \quad t_4 < t < t_5 \\ I_{avd}(t) & t_1 < t < t_4 \end{cases} \qquad (6.30)$$

The RMS current harmonics can be found by analysing the Fourier series for $i_s(t)$.

6.4 Design Procedure

The specification for this converter is the same as for the bi-forward converter specified in section 4.3.1.

6.4.1 Converter Design

It was decided to keep the primary turns on the transformer the same as the total number of primary turns (44) for the bi-forward converters.

Design of the PFC Stage

The key design parameters are L_{1A} and L_{1B}, L_{DA} and L_{DB} as well as the number of turns on N_{4A} and N_{4B}. These need to be determined for the best design compromise which will meet IEC 61000-3-2 and keep the bulk capacitor voltage reasonable at below 500V, but preferably closer to 400V. The diodes D_{4A}, D_{4B}, D_{5A} and D_{5B} can then be sized. For design purposes the converter is assumed to be about 75% efficient, hence the maximum input power will be about 200W. Before the PFC stage can be designed the turns ratio $N_2 : N_1$ should be chosen, as this determines the duty cycle of the converter (equation 6.7) and it also affects the operation of the PFC stage. The converter in [122] has transformer turns as $N_1 = 52$ and $N_2 = 3$ (5V output) which gives a lower turns ratio than normal for this sort of design where $N_1 = 34$ is common. The primary turns have been increased so as to increase the duty ratio of the converter and give a longer period for the processes shown

119

in figure 6.6 to occur. Following on from this example the number of secondary turns (as used in the other converters) was reduced from 5 to 3 for $N_{2:5V}$ and from 11 to 7 for $N_{2:12V}$.

[122] shows that the value of L_{1A} and L_{1B} does not affect the level of the input current harmonics, particularly when they test a 200W output CS S^{2}PFC circuit with L_{1A} set at values between $45\mu H$ and $190\mu H$. The same paper shows that higher values of L_{1A} produce converters with lower levels of V_B, but V_B is only reduced by 10V between L_{1A} equal to $78\mu H$ and $178\mu H$. As L_{1A} and L_{1B} have only a minor effect on the converter performance, it was decided to set them to $100\mu H$. The value of L_1 will determine how much switching frequency ripple will need to be filtered on the input of the converter, but this not a concern for this study.

Evaluating equation 6.27, it is possible to plot power against bulk capacitor voltage for different values of L_{DA} and L_{DB}, and N_{4A} and N_{4B}. Initially considering the input voltage as $230V_{RMS}$, power vs V_B plots were produced for:

L_{DA}/L_{DB} 10, 30, 50, 70μH

N_{4A}/N_{4B} 6, 12, 18 turns

$\frac{N_{4A}}{N_1}$ 0.136, 0.27, 0.41

These particular values were chosen based on the work in [122]. The plots are displayed in figure 6.7. Other designs can be deduced from these curves.

The point where slope of the curves changes dramatically is where the input power has dropped low enough for L_1 to operate only in DCM. From figure 6.7 it is possible to see that curves around N_{4A} and $N_{4B} = 6$, with L_{DA} and L_{DB} at 30-70μH, as well as N_{4A} and $N_{4B} = 12$ with L_{DA}/L_{DB} at 50-70μH are not acceptable, as the voltage V_B is too low at high power (below the peak of the supply voltage). The voltage on C_B should be above the peak of the mains (325V with 230V_{RMS} input) at full load input power, as otherwise the action of the PFC stage is lost and the bulk capacitors peak charge via L_1 distorting the current shape (the peak charging was not predicted in the analysis carried out, but a lower average voltage was). At low power the bulk capacitor voltage was high so as to limit the amount of energy being taken to and from the bulk capacitors. As the voltage rises the duty cycle becomes narrower, reducing the amount of energy taken from C_B as the output power reduces. The narrowing of the duty cycle also reduces the amount of energy delivered to C_B via L_1 so balancing the energy in and out of C_B. At high output power a large amount

The legend entries (left side of graph):

- $P(V_B, 10 \cdot 10^{-6}, 6)$
- $P(V_B, 30 \cdot 10^{-6}, 6)$
- $P(V_B, 50 \cdot 10^{-6}, 6)$
- $P(V_B, 70 \cdot 10^{-6}, 6)$
- $P(V_B, 10 \cdot 10^{-6}, 12)$
- $P(V_B, 30 \cdot 10^{-6}, 12)$
- $P(V_B, 50 \cdot 10^{-6}, 12)$
- $P(V_B, 70 \cdot 10^{-6}, 12)$
- $P(V_B, 10 \cdot 10^{-6}, 18)$
- $P(V_B, 30 \cdot 10^{-6}, 18)$
- $P(V_B, 50 \cdot 10^{-6}, 18)$
- $P(V_B, 70 \cdot 10^{-6}, 18)$
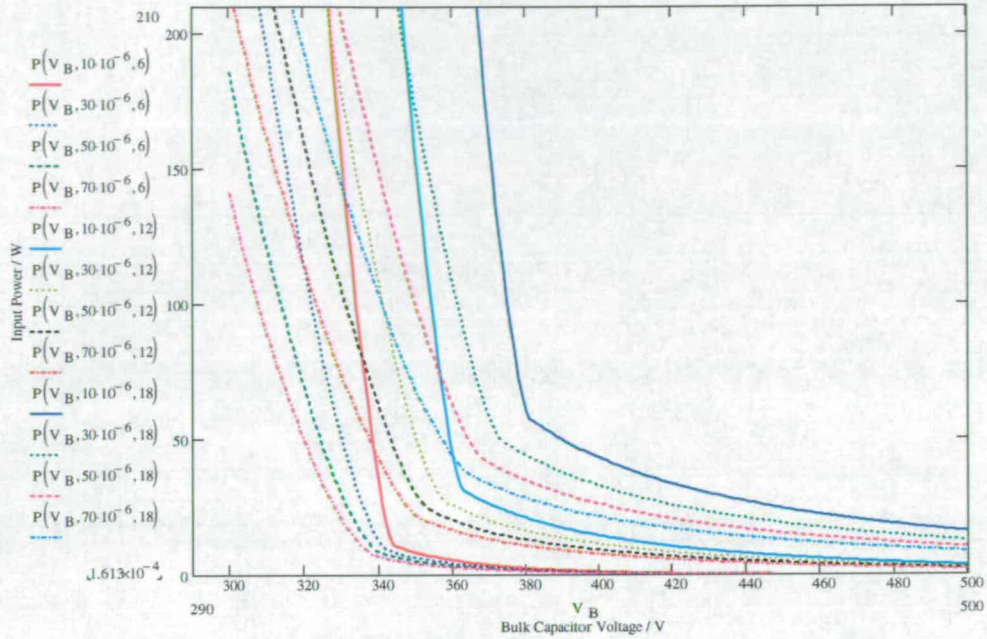
Figure 6.7: Graphs showing power against bulk capacitor voltage for 230V_{RMS} input for $L_{DA}/L_{DB} = 10, 30, 50, 70\mu\text{H}$ with N_{4A} and N_{4B} as either 6, 12, or 18 Turns. Traces are listed by side of graph, 1st value is the value of L_{DA} and L_{DB} and 2nd value is the number of turns on N_{4A} and N_{4B}.

of energy needs delivering to the output: to get an equivalent amount of energy into the bulk capacitor the duty cycle needs to be wider to get the energy through the PFC network. To balance the input and output energy from C_B the duty cycle needs to be wider to get the required energy in and out of C_B; this can only occur if the bulk voltage is low.

The input current $i_s(t)$ can be constructed as in equation 6.29 and can be evaluated to see if they meet IEC 61000-3-2 class D at 200W and 75W.

Figure 6.8 shows the odd harmonic spectrum for the remaining design curves at 200W input power. Figure 6.8 shows that the curves for L_{DA} and $L_{DB} = 10\mu\text{H}$ and N_{4A} and $N_{4B} = 6$, 12 or 18 all exceed the class D regulation for 230 V 200W input by a considerable margin. The other curves for L_{DA} and $L_{DB} = 30, 50$ or $70\mu\text{H}$ and N_{4A} and $N_{4B} = 12$ or 18 (only one for 12) are either very close to the regulation curve or below it. A similar set of curves for 75W input power showed that all the design curves are exceeding the class D regulation at 75W with the two curves for L_{DA} and $L_{DB} = 10\mu\text{H}$ and N_{4A} and $N_{4B} = 6$ or 12 being the worst. From figure 6.8 and its 75W counterpart it was decided that curves for L_{DA} and $L_{DB} = 10\mu\text{H}$ and N_{4A} and $N_{4B} = 6$, 12 or 18 all exceeded the regulation curves by far too
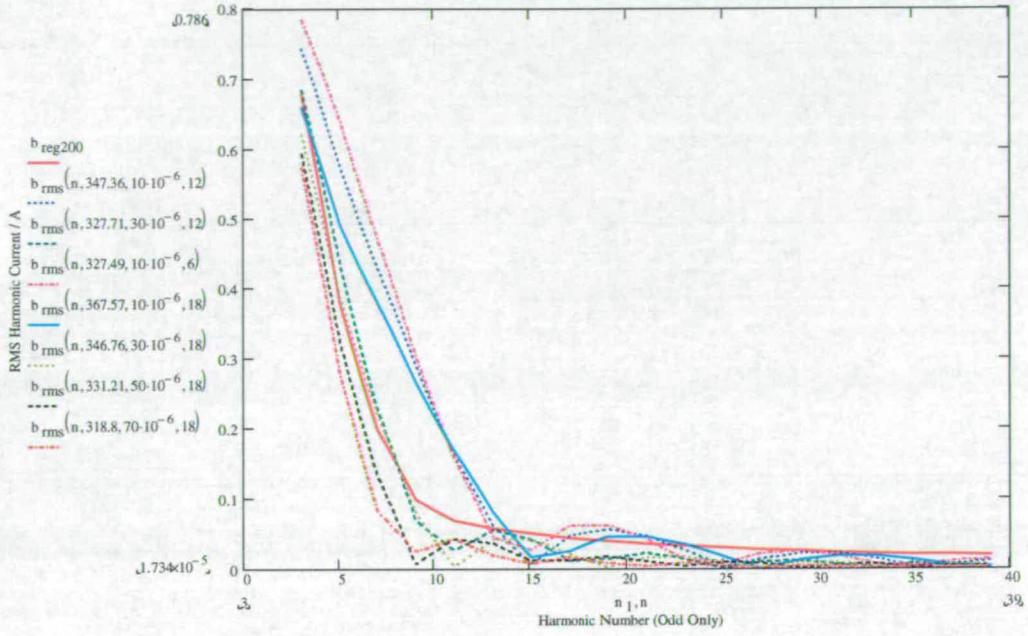
Figure 6.8: Odd harmonic spectrum for input power and voltage of 200W 230V$_{RMS}$ for the remaining curves (only odd harmonics are plotted). The red trace (b_{reg200}) is the class D limits for 200W. Traces are listed by side of graph: 1st value is the voltage on C_B, 2nd value is the value of L_{DA} and L_{DB} and 3rd value is the number of turns on N_{4A} and N_{4B}.

large a margin to be considered and were thus rejected. The other designs were considered close enough to the design curve (even if they exceeded it by a small amount) that if they were built it is likely that they would meet the class D regulations at least at full input power (about 200W).

The remaining design possibilities (4) were checked at 265V$_{RMS}$ input to see how high the bulk capacitor voltage would go. The plot of power against V_B for 265V$_{RMS}$ input is shown in figure 6.9. The line P_{od} is a plot of the CCM/DCM boundary for the output inductors $L_{2:5V}$ and $L_{2:12V}$ and is defined by equation 6.31.

$$P_{od} = \frac{0.5 \cdot V_{o:5V}{}^2 \cdot (1 - D(V_B))}{L_{2:5V} \cdot f_s} + \frac{0.5 \cdot V_{o:12V}{}^2 \cdot (1 - D(V_B))}{L_{2:12V} \cdot f_s} \tag{6.31}$$

Where this curve intersects the design curves is the highest bulk capacitor voltage that the design will experience. At this point the output inductor is in DCM and the bulk capacitor voltage is no longer dependent on power. The curve for L_{DA} and L_{DB} as 30μH and N_{4A} and N_{4B} as 12 has a peak voltage of about 438V which is under a desired maximum voltage

122

$P\left(V_B, 30 \cdot 10^{-6}, 12\right)$

$P\left(V_B, 30 \cdot 10^{-6}, 18\right)$

$P\left(V_B, 50 \cdot 10^{-6}, 18\right)$

$P\left(V_B, 70 \cdot 10^{-6}, 18\right)$

$P_{od}\left(V_B\right)$
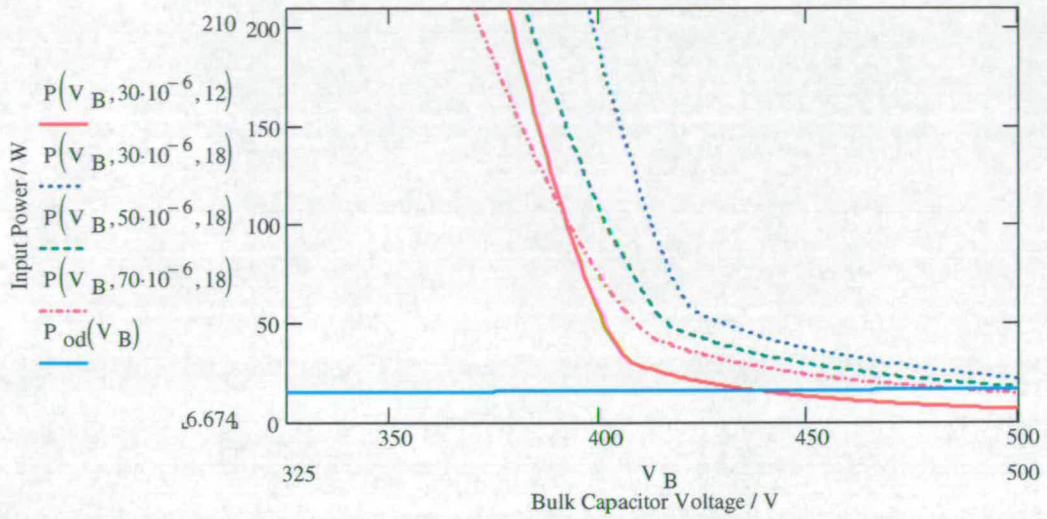
Figure 6.9: Graphs showing power against bulk capacitor voltage for $265V_{RMS}$ input for L_{DA} and $L_{DB} = 30\mu H$ with N_{4A}/N_{4B} as 12 and L_{DA} and $L_{DB} = 30$, 50 and $70\mu H$ with N_{4A}/N_{4B}. Traces are listed by side of graph: 1st value is the value of L_{DA} and L_{DB} and 2nd value is the number of turns on N_{4A} and N_{4B}.

of 450V. The other remaining design curves have a higher peak voltage, but L_{DA} and L_{DB} as $70\mu H$ and N_{4A} and N_{4B} as 18 gives about 486V, which is still acceptable if two 250V capacitors are used. With L_{DA} and L_{DB} as $30\mu H$ and N_{4A} and N_{4B} as 18 the peak voltage expected is 538V, and for L_{DA} and L_{DB} as $50\mu H$ and N_{4A} and N_{4B} as 18 the peak voltage is 511V, both of which are too high if two 250V capacitors are to be used. If the output filter inductors $L_{2:5V}$ and $L_{2:12V}$ were redesigned so that they entered DCM at a higher current, then designs based on other curves would be possible (in this case they are not redesigned as they were kept the same as the other converters). It was decided that the two design curves with the bulk capacitor below 500V (that is L_{DA} and L_{DB} as $30\mu H$ and N_{4A} and N_{4B} as 12, and L_{DA} and L_{DB} as $70\mu H$ and N_{4A} and N_{4B} as 18), were the most likely to be worth pursuing, but the other two could not be neglected at this stage. These remaining designs were checked to see if they meet the regulation at $100V_{RMS}$ input voltage in the same manner as for 230V. The graphs are shown in figures 6.10 and 6.11.

Figure 6.10 shows the variation of bulk capacitor voltage with power for one bulk capacitor and for 100V input voltage. It is noticed that all four design curves have an average bulk capacitor voltage below the peak of the line voltage (141V) at full load input power of 200W. To see how a curve which does have a bulk capacitor at full power above the line
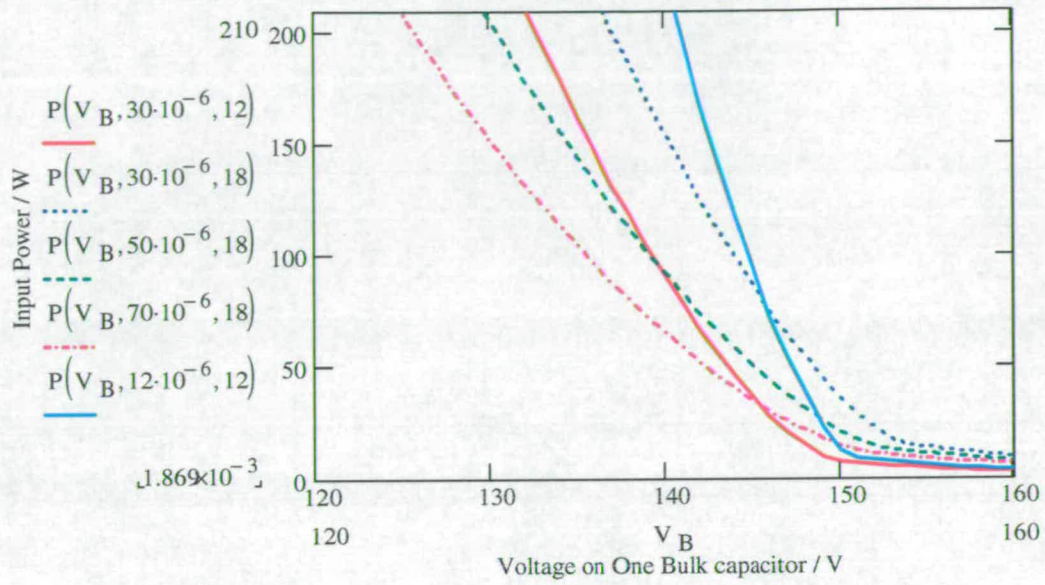
Figure 6.10: Graphs showing power against bulk capacitor voltage for $100V_{RMS}$ input for L_{DA} and $L_{DB} = 30\mu H$ with N_{4A} and N_{4B} as 12 and L_{DA} and $L_{DB} = 30, 50$ and $70\mu H$ with N_{4A} and N_{4B}. Traces are listed by side of graph: 1st value is the value of L_{DA} and L_{DB} and 2nd value is the number of turns on N_{4A} and N_{4B}.
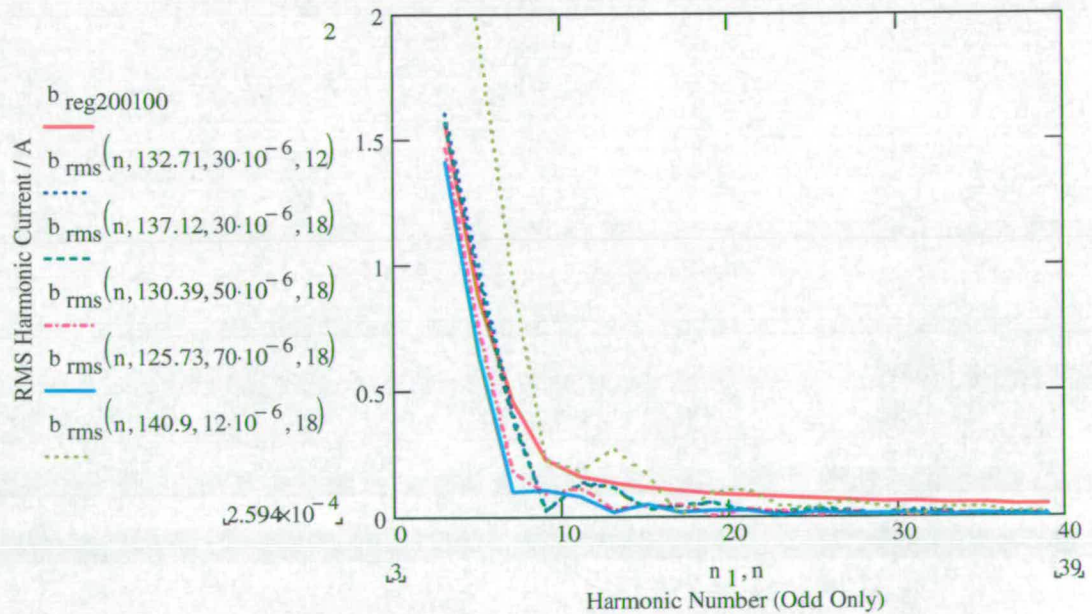
Figure 6.11: Odd harmonic spectrum for input power and voltage of 200W $100V_{RMS}$ for the remaining curves (only odd harmonics are plotted). The red trace ($b_{reg200100}$) is the class D limits for 200W. Traces are listed by side of graph: 1st value is the voltage on a single C_B, 2nd value is the value of L_{DA} and L_{DB} and 3rd value is the number of turns on N_{4A} and N_{4B}.

voltage peak, a fifth design curve has been iterated and is L_{DA} and L_{DB} as 12μH and N_{4A} and N_{4B} as 12. Figure 6.11 shows the RMS current harmonics compared to class D at 200W input, and again four of the curves are very close to the class D limits, the exception being L_{DA} and L_{DB} as 12μH and N_{4A} and N_{4B} as 12. A similar plot for 75W input power showed all the design curves are above the class D limit (most are just above) for the low harmonics below about the 11th harmonic. The worst offender is L_{DA} and L_{DB} as 12μH and N_{4A} and N_{4B} as 12.

From the final five design curves left it was decided to construct a prototype converter based around the L_{DA} and L_{DB} as 30μH and N_{4A} and N_{4B} as 12 curve. L_{DA} and L_{DB} as 30 and 50μH and N_{4A} and N_{4B} as 18 have already been shown to have a peak bulk capacitor voltage in excess of 500V, which is far too high. L_{DA} and L_{DB} at 12μH and N_{4A} and N_{4B} at 12 would most likely not have any chance of meeting the regulations at any power or voltage. L_{DA} and L_{DB} at 70μH and N_{4A} and N_{4B} at 18 has a bulk capacitor voltage which is too low at 100V input for the converter to operate in the proper and expected manner, even when considering that the calculated figures for bulk capacitor voltage should be within 10% of the values seen on a prototype. It is felt a design around L_{DA} and L_{DB} as 30μH and N_{4A} and N_{4B} as 12 gave the best compromise in ability to meet the class D harmonic regulations and for voltage seen across the bulk capacitor. The RMS current harmonics calculated were close to the class D regulation curves. The peak voltage at 265V input was the lowest, and the average voltage at 100V was below the peak of the line voltage but it was higher than L_{DA} and L_{DB} as 70μH and N_{4A} and N_{4B} as 18, and voltages within 10% of these would be above the peak of the line voltage. Figure 6.12 shows the predicted input current at 230V and 100V.

The final choice was:

- L_{DA}/L_{DB} 33μH, later changed to 43μH during testing.

- N_{4A}/N_{4B} 11 turns

6.4.2 Sizing of Semiconductor Components

The average or RMS current through the components cannot yet be calculated, as at 90V input voltage the analysis predicts the bulk capacitor voltage to be below the peak of the line

125
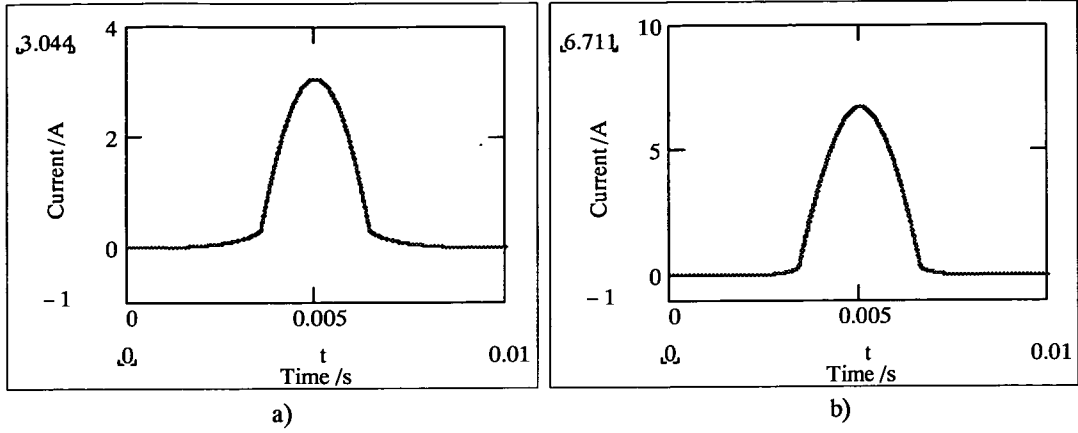
Figure 6.12: Predicted input current waveforms for 200W input power at a) 230V and b) 100V input voltage with L_{DA} and $L_{DB} = 33\mu$H and N_{4A} and $N_{4B} = 11$

voltage. This causes some of the current change to slope in the wrong direction. Instead the currents predicted by PSpice in table 6.2 are used. The analysis was only written for when the bulk capacitor voltage is above the peak of the line voltage.

When operating at 265V input voltage the peak bulk capacitor voltage was measured in figure D.3 as 423.76V when the output inductors $L_{2:5V}$ and $L_{2:12V}$ go into DCM.

Switch S_1 and Reset Winding Diode D_1

When the transformer is being reset the voltage seen across S_1, V_{S1}, is

$$V_{S1} = V_B + \frac{N_1}{N_2} \cdot V_B \tag{6.32}$$

Since N_1 and N_2 are the same the peak voltage seen across S_1 is 847V: to provide a reasonable safety margin a 1000V MOSFET is used. Heavily over-designing for survivability the IXFH12N100, a 1000V 12A device, was used.

The same voltage is seen across diode D_1 when S_1 is on. In the bi-forward of chapters 4 and 5 the BYD33U diode was used, but this only has an average current rating of 1.26A. In this topology the tertiary winding N_3 will carry more than just magnetising current, as transformer windings N_{4A} or N_{4B} will also be carrying current during the off-time of S_1, and this current will be transferred to the tertiary winding N_3 while the transformer is

126

resetting. Due to this, D_1 is replaced by the plentiful and over-rated BY329-1000 (1000V 8A diode).

Secondary Diodes $D_{2:5V}$, $D_{3:5V}$, $D_{2:12V}$ and $D_{3:12V}$

The peak voltage seen across the secondary diodes, V_{D2}, is:

$$V_{D2} = \frac{N_2}{N_1} \cdot V_B \qquad (6.33)$$

For the 5V output ($N_2 = 3$) this is calculated to be 28.9V and for the 12V output ($N_{2:12V} = 7$) this is calculated to be 67.4V. The total average current in the 5V diodes is 20A and the total average current in the 12V diodes is 4A. For the 12V output, where diode losses are not so severe, the BYT08P-400 (400V 8A device) is used. For the 5V output where the losses are higher, 20A Schottky diodes are used to reduce losses, as the voltage is now low enough to allow their use. The device chosen was a STPS20H100CT (100V 20A).

Diodes D_{4A}, D_{4B}, D_{5A} and D_{5B}

During normal operation the peak voltage seen across D_{4A} or D_{4B}, V_{D4}, is:

$$V_{D4} = \frac{V_B + \frac{2 \cdot N_{4A}}{N_3} \cdot V_B - V_{cin}}{2} \qquad (6.34)$$

This situation occurs across the zero crossing. The voltage V_{cin} is the voltage across capacitors C_{2A} and C_{2B} in figure 6.16 that are fitted across the DC side of the diode bridge rectifier. During the time when current is flowing through the input of the circuit these capacitors have the input voltage across them. However, during the zero crossing when no current is flowing through the input of the converter the voltage on the capacitors remains at the instantaneous supply voltage that L_{1A} or L_{1B} stopped conducting, this the input voltage (V_{cin}) at time t_1. V_{cin} for this case is 212V when the input voltage is 265V. This gives a normal operating peak voltage across D_{4A} or D_{4B} of 212V. To cover for the situation where there is no voltage at the input and if one of the diodes D_{4A} or D_{4B} turns off slower than the other, then the voltage, V_{D4E}, across the diode will be:

$$V_{D4E} = V_B + \frac{N_{4A}}{N_3} \cdot V_B \qquad (6.35)$$

In this situation the voltage across D_{4A} or D_{4B} is 530V.

During normal operation the voltage, V_{D5} seen across D_{5A} or D_{5B} is

$$V_{D5} = \frac{V_B - V_{cin}}{2} \qquad (6.36)$$

This calculates to be 106V. Again, to cover the same situation as mentioned for D_{4A} or D_{4B} the maximum possible voltage is the bulk capacitor voltage of 424V.

The diode used for D_{4A}, D_{4B}, D_{5A} and D_{5B} is the BY329-1000 as there was a plentiful supply and they had ratings well in excess of what was required, again building in survivability.

6.5   Simulation

In figure 6.13 is the PSpice simulation schematic. The simulation settings are the same as used for the bi-forward converters in chapters 4 and 5. The averaging circuit shown in figure 4.7 is not included in this simulation as the input current is mainly in CCM and the filtered (averaged) shape of the input current can be seen without it. To convert the schematic for simulation on the 90 to 130V input voltage range an additional bulk capacitor is added in series with C_B and their values are changed to 330μF. Also a connection is made between the bulk capacitors and diodes D_7 and D_8. When simulating at 265V input voltage, to find the voltage across the semiconductors a capacitance of 1μF is put across the DC side of the diode bridge to stabilize the voltage when the diode bridge is not conducting (this capacitor is fitted to the prototype converters at all voltages). This capacitor does not effect the working of the rest of the simulation. The simulation was run in the same way as in chapters 4 and 5.
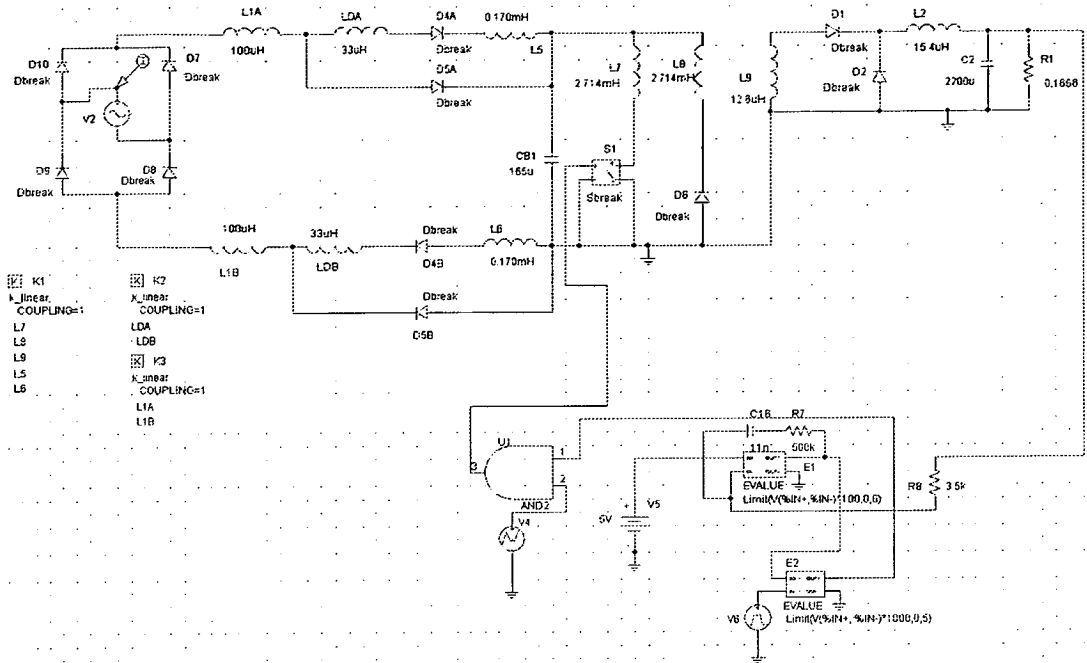
Figure 6.13: PSpice schematic for simulation on the 180 to 265V Range

6.5.1 Simulation Results

Table F.5 in appendix F shows the input current harmonics for 230V input voltage and 150W output power (174W input power) compared to class D. The simulation waveform fails on the 5th and 7th harmonics, by a small amount, which is the same two harmonics predicted by Mathcad in figure D.1.

Table F.6 in appendix F shows the input current harmonics for 100V input voltage and 150W output power (174W input power) compared to class D. The simulation waveform passes on all the odd harmonics, whereas the Mathcad prediction in figure D.2 shows that the waveform just exceeds the class D regulation for 200W on the 3rd and 5th harmonics; again they are close.

Table 6.1 shows the voltage across the semiconductors measured in PSpice. They are slightly lower (but within 10%), than that predicted in the analysis, as the bulk capacitor voltage is lower at 400V instead of 424V.

The average current in the semiconductor components is shown in table 6.2. These are sensible values for a converter with a 150W ouput power and for the particular transformer

129

Device	Voltage/V
S_1	802
D_1	26.6
D_2	26.5
D_{4A}/D_{4B}	199
D_{5A}/D_{5B}	97.3
D_6	800
D_B	374

Table 6.1: Peak voltage across key semiconductors at 265V input and 40W output measured in PSpice. Average voltage across C_{B1} and C_{B2} was 400V.

turns ratios used.

Device	Average or RMS Current/A
S_1 RMS	1.44
S_1 AV	0.84
D_{4A}/D_{4B} per diode	0.306
D_{5A}/D_{5B} per diode	0.509
D_6	0.00926
D_B per diode	0.811

Table 6.2: RMS or average current through key semiconductors at 90V input and 150W output (176W input) measured in PSpice

6.5.2 Simulation Waveforms

The lower trace in figure 6.14 shows the input current waveform predicted by PSpice at 100V input voltage. The shape is similar to that predicted in analysis shown in figure 6.12b, but the PSpice waveform has a slight lean to the left due to the charging and discharging of the bulk capacitor causing its voltage to change. The top trace shows the current in L_{1A} (this current only flows every other half line cycle due to the voltage doubler switch being closed). The inductor L_{1B} is conducting during the half line periods that L_{1A} is not. The peak of the input current is just under 6A. The waveform predicted by the analysis in figure 6.12b has a peak of 6.77A. They are different to the analysis above, as the power used in Mathcad was 200W.

Figure 6.15 shows switching frequency current waveforms for L_{1A}, D_{4A} and D_{5A} at 230V input voltage and 150W output when L_{1A} is operating in CCM. It can be seen that at turn
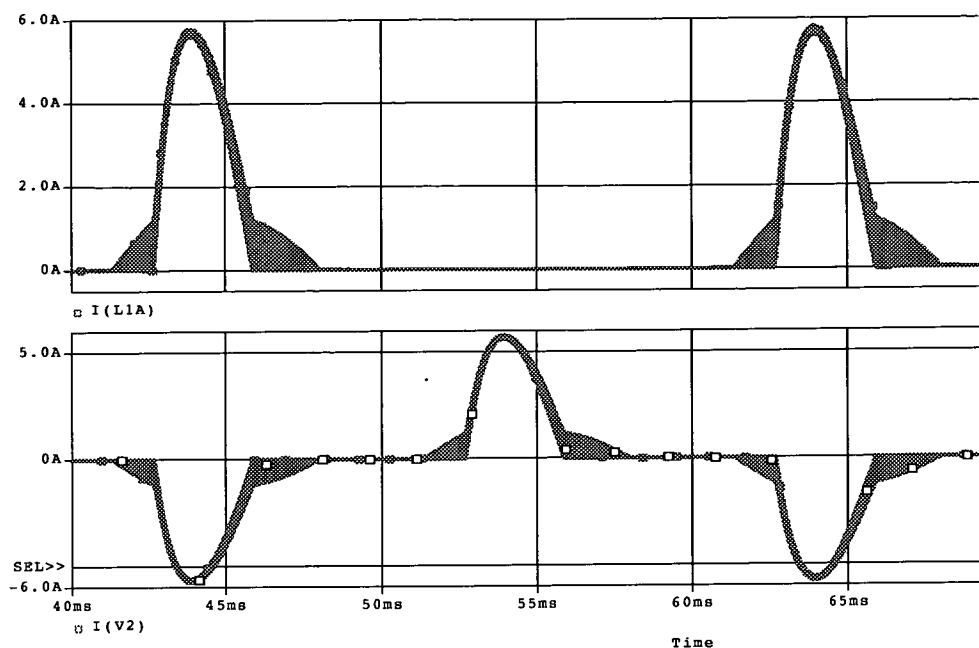
Figure 6.14: Input current at 150W output and 100V input measured in PSpice (bottom trace) and current in L_{1A} (top trace). The input power is 177W.

on of S_1 the current in D_{4A} (and L_{DA}) ramps up from zero and the current in D_{5A} is commutating to D_{4A}; at the same time the current in L_{1A} is still falling as the voltage across L_{1A} has not changed. The current in L_{1A} starts rising when the current in D_{4A} reaches that in D_{5A}, and D_{5A} stops conducting. The voltage across L_{1A} is now positive so current rises. At turn off of S_1 the current in D_{4A} slowly commutates to D_{5A} and the current in L_{1A} starts falling again. This is most obvious in the last cycle shown.

6.6 Experimental Results

Figure 6.16 shows the final and complete circuit schematic tested. The components used are listed in table G.2 in appendix G and a photograph of the final circuit is shown in figure 6.17.

131
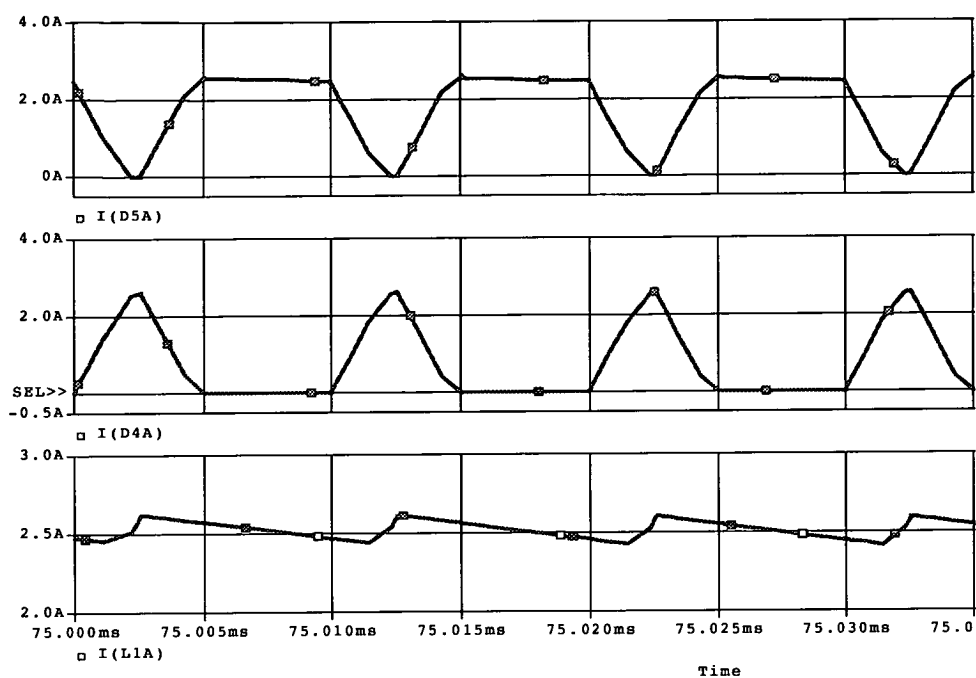
Figure 6.15: Switching frequency current in inductor L_{1A} (bottom trace), D_{4A} (middle trace) and D_{5A} (top trace) across the peak of the line input voltage at 230V input measured in PSpice
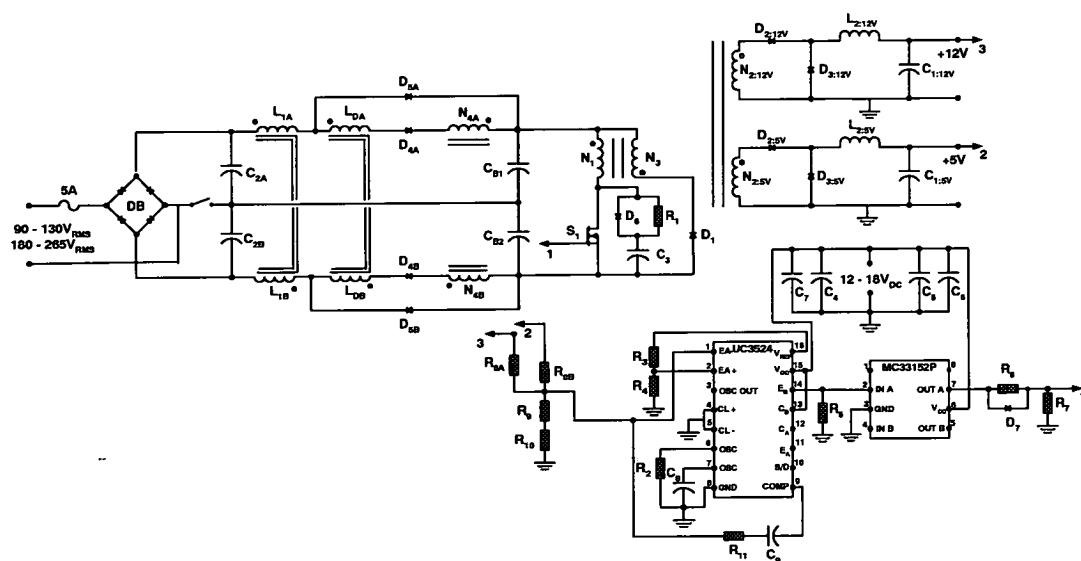
Figure 6.16: Final and complete circuit schematic for the CS S^2PFC converter

132
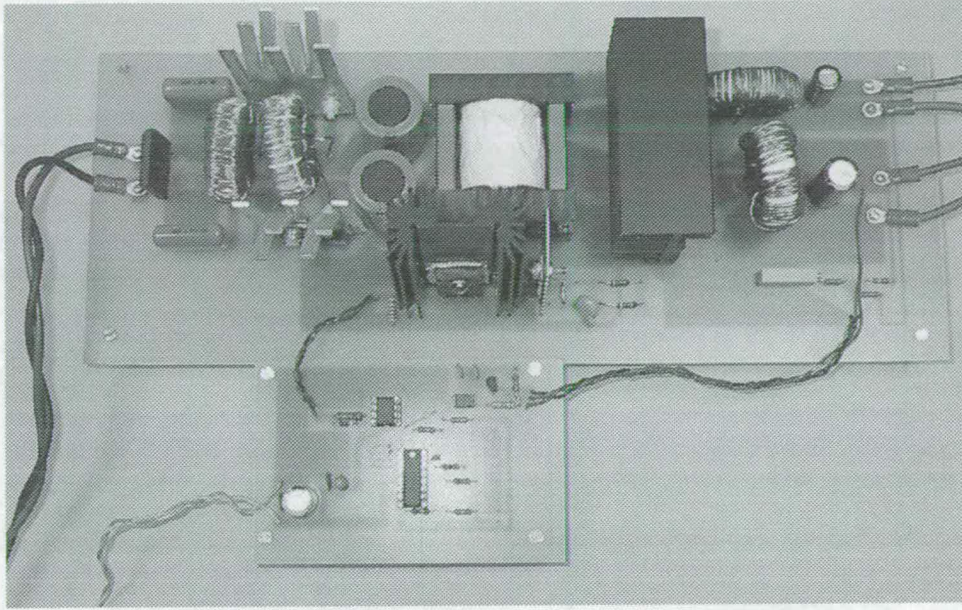
Figure 6.17: Photograph of the CS S²PFC converter

6.6.1   Changes Made to Prototype Circuit

The value of L_D was varied to try and make the converter pass the class D harmonic regulations at 75W input power. The values tried were 33, 22, 43, 37μH.

All values of L_D tried failed class D at 75W input power at both voltages. In the end 43μH was used because it produced a lower bulk capacitor voltage.

A MOSFET turn-off snubber shown in figure 6.16 was fitted early during testing.

6.6.2   Harmonic Tests

Figures 6.18, 6.19, 6.20 and 6.21 show the measured input RMS current harmonics compared to class D. In figures 6.18 and 6.20 the converter is shown to meet class D at full power at 100V and 230V. This is better than that predicted by PSpice and in the analysis, both of which predicted slight failure at 230V on the low harmonics. At 100V PSpice predicted a pass and the analysis a slight failure at the low harmonics. At 75W input power the converter failed to meet the regulation for the 7th, 9th, 11th and 13th harmonics at 230V (figure 6.19) and for the 7th and 9th harmonics at 100V (figure 6.21). Further testing found that the lowest power that the converter would comply with the class D limits was at 97W

for both 100V and 230V input voltage. The converter passes class A.
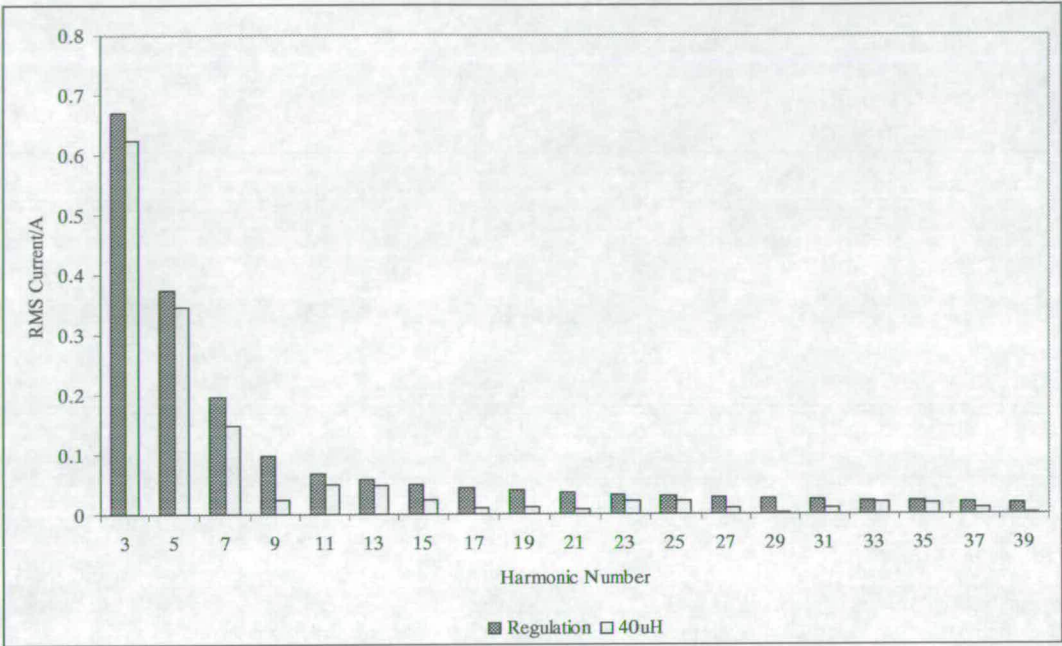
Figure 6.18: Measured RMS current harmonic levels for 230V and full load output power with L_D as $43\mu H$ compared to class D: input power is 197W

6.6.3 Input Current Waveform

Figure 6.22 shows the input current waveform at: a) 230V full load where the converter meets class D, b) 230V 75W input where the converter failed class D, c) 100V 97W input where the converter started to meet class D and d) 100V full load where the converter meets class D. In 6.22a and c, with the two waveforms at full power, it is noticeable that the peak of the current waveform is flattened. Otherwise their basic shapes are very similar to each other. It is possible to see the DCM part of the waveform at the beginning and end of the current waveforms, where the slope is shallow.

There is possibly some distortion in figure 6.22c due to peak charging of C_{B2} during the negative parts of the cycle (this is hard to see). This does not seem to have affected the current harmonics much.

It is not possible to show switching frequency waveforms which clearly show the operation of the converter as resonances were present on the waveforms, hiding the actual power transfer voltages and currents. The resonances did not seem to hinder or change the operation of

134
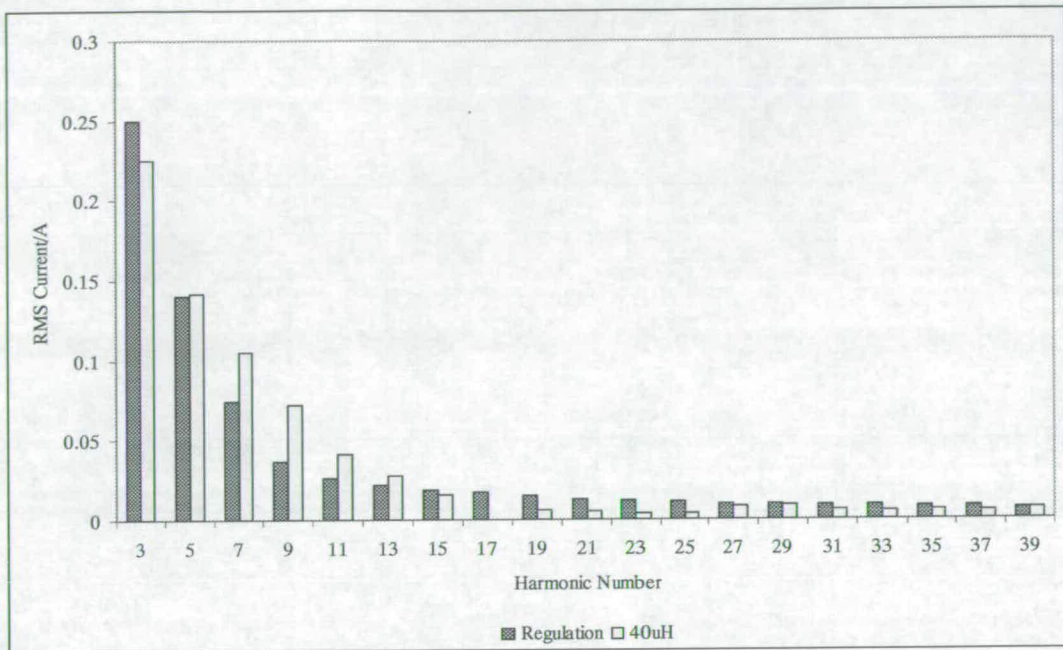
Figure 6.19: Measured RMS current harmonic levels for 230V and 75W input power with L_D as 43μH compared to class D: input power is 74W
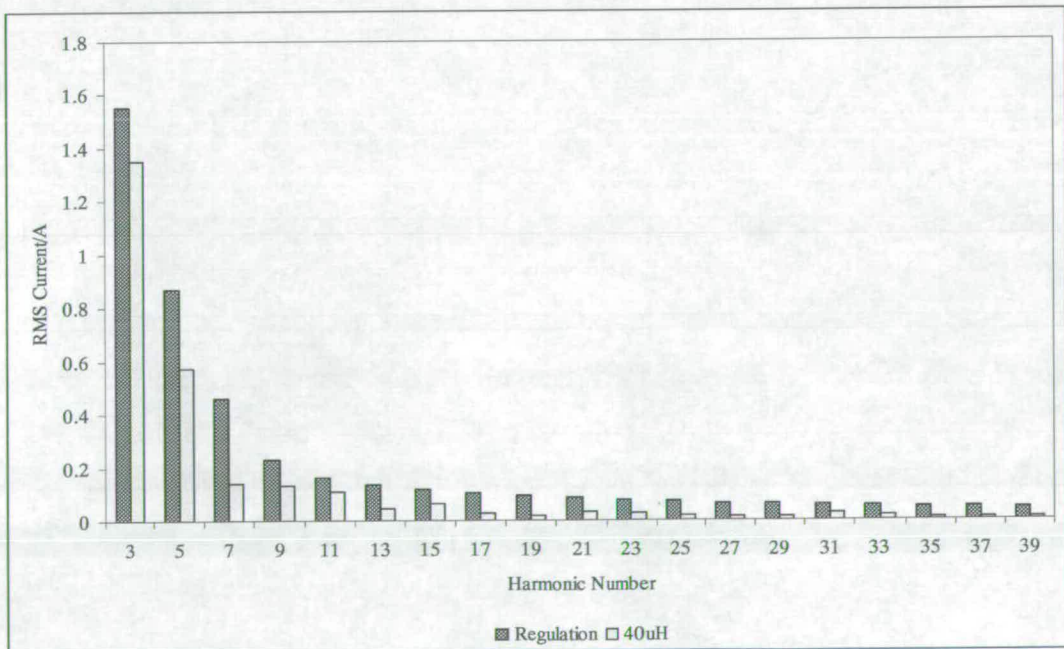
Figure 6.20: Measured RMS current harmonic levels for 100V and full load output power with L_D as 43μH compared to class D: input power is 199W
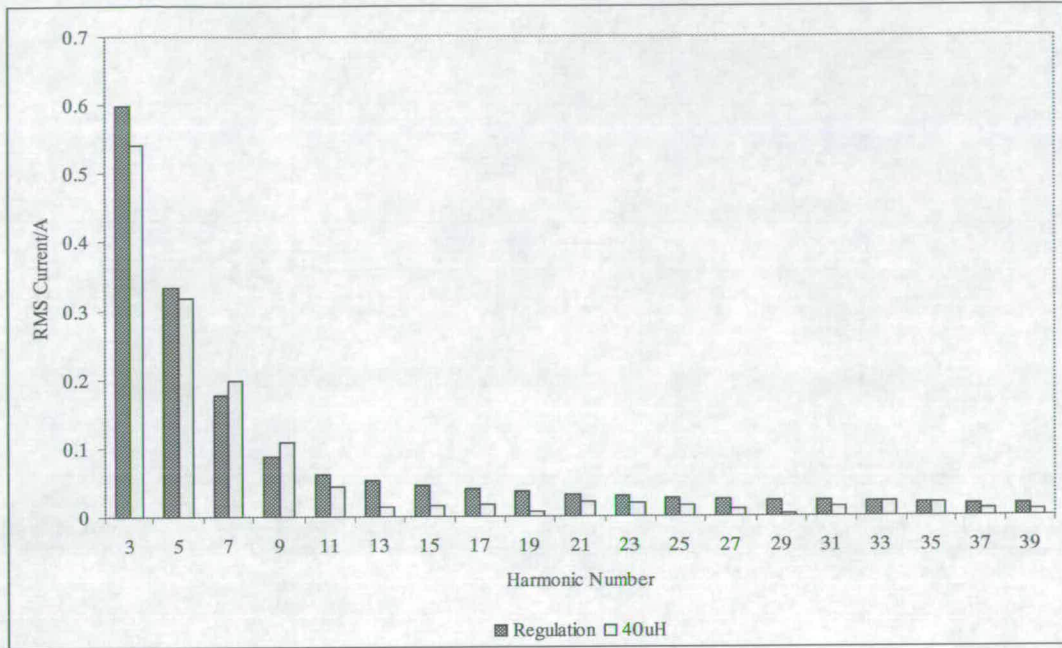
Figure 6.21: Measured RMS current harmonic levels for 100V and 75W input power with L_D as 43μH compared to class D: input power is 76W

the converter.

6.6.4 Efficiency and Voltage Across the Bulk Capacitors, C_{B1} and C_{B2}

In table H.2 in appendix H are presented the measured input and output powers, efficiency and bulk capacitor voltages. The efficiency and bulk capacitor voltages are plotted in figures 6.23 and 6.24. The efficiency is very good, ranging from 72% at about 40W output power with 265V input voltage to 78% at 74W output power at 180V input voltage. Most of the efficiency readings are in the mid-70s. When dividing the low line bulk capacitor voltages by two to give an indication of the voltage across a single capacitor, the voltage given is below the peak of the line voltage and checking the waveforms recorded for when the output was 150W for all three voltages (90V, 115V and 130V) peak charging is observed, but different amounts are occurring on the positive and negative parts of the cycle.

The voltage across both bulk capacitors is shown in figure 6.24 ranging from 230V to 408V. The range is narrower than the line voltage range due to the voltage doubler. This can be seen since the bulk capacitor voltage at 130V is close to that seen at 265V, the 115V bulk capacitor voltage is close to that of 230V, and the 90V bulk capacitor voltage is close to
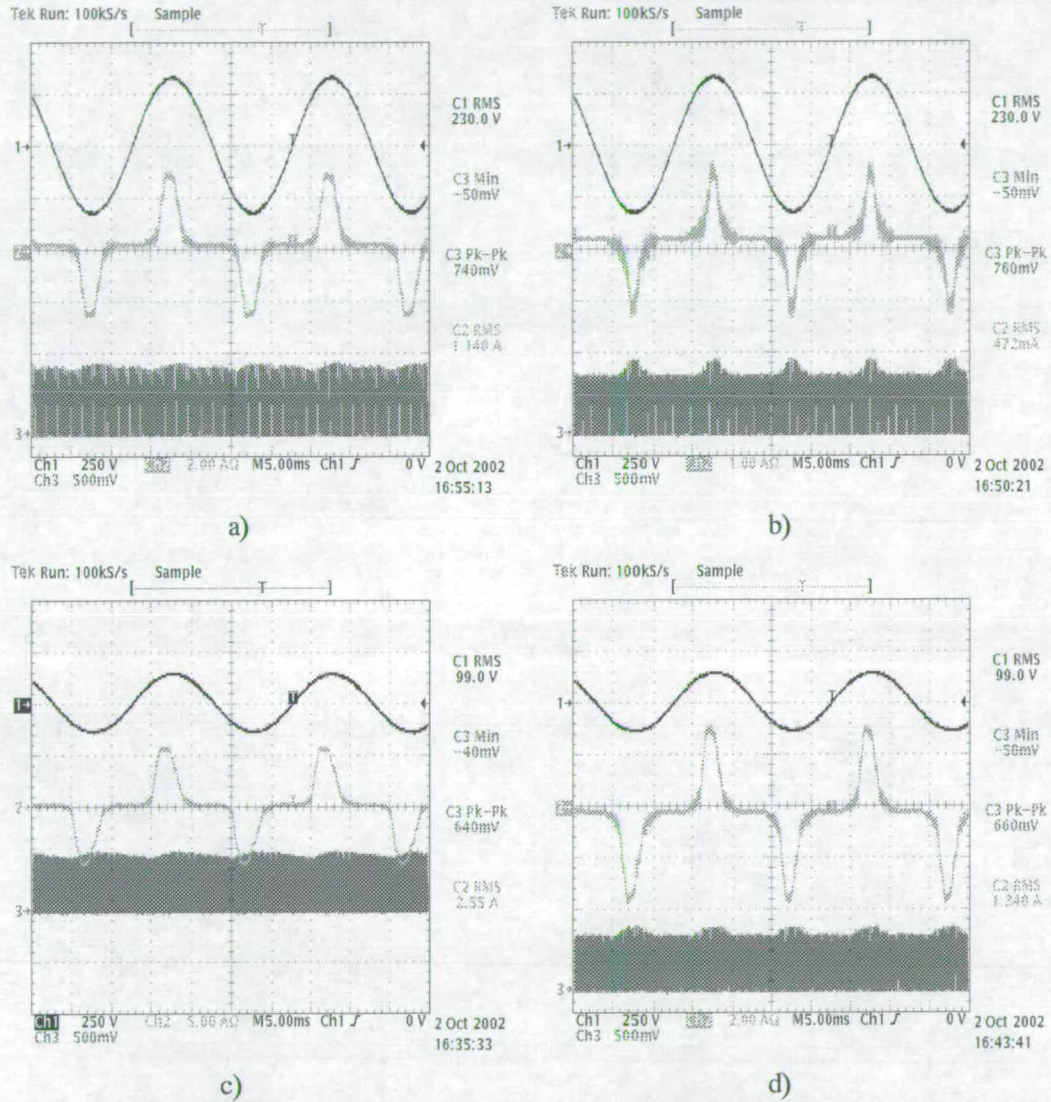
Figure 6.22: Measured a) Input current at 230V and full load, b) Input current at 230Vand 75W input power, c) Input current at 100V and full load and d) Input current at 100V and 97W input power. All have L_D as $43\mu H$. Top trace is input voltage, middle trace is input current and the bottom trace is the drain-source voltage of S_1.
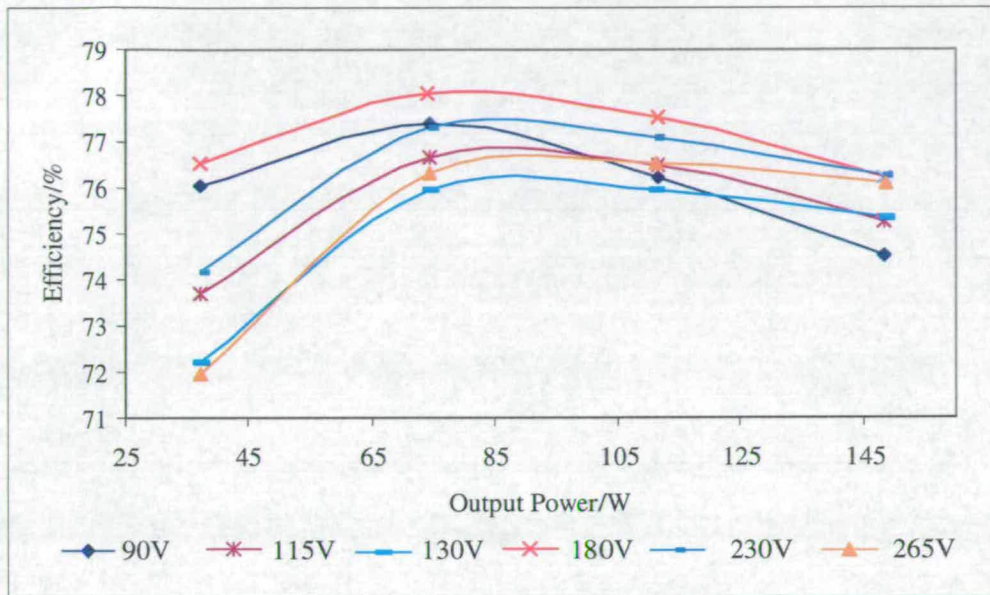
Figure 6.23: Efficiency of the CS S^{2}PFC across the input voltage range

that of 180V. Figure 6.25 compares the bulk capacitor voltage measured at 265V with that predicted for 265V. The measured voltage is higher than the predicted voltage for the same input power by about 20V, but it is following the same shape, except when the input power is low (at 8W). Even with a 10V difference predicted voltages are still within 10% of the measured voltages.

6.6.5 Hold Up Time and Output Voltage Ripple

Hold Up Time

Hold up is measured in the same way as in section 5.6.5. The results for 115V and 230V are shown in table 6.3 and both are acceptable, being above 10ms.

Input Voltage/V	Hold up time/ms
115	18.4
230	27.6

Table 6.3: Hold up time for 115V and 230V
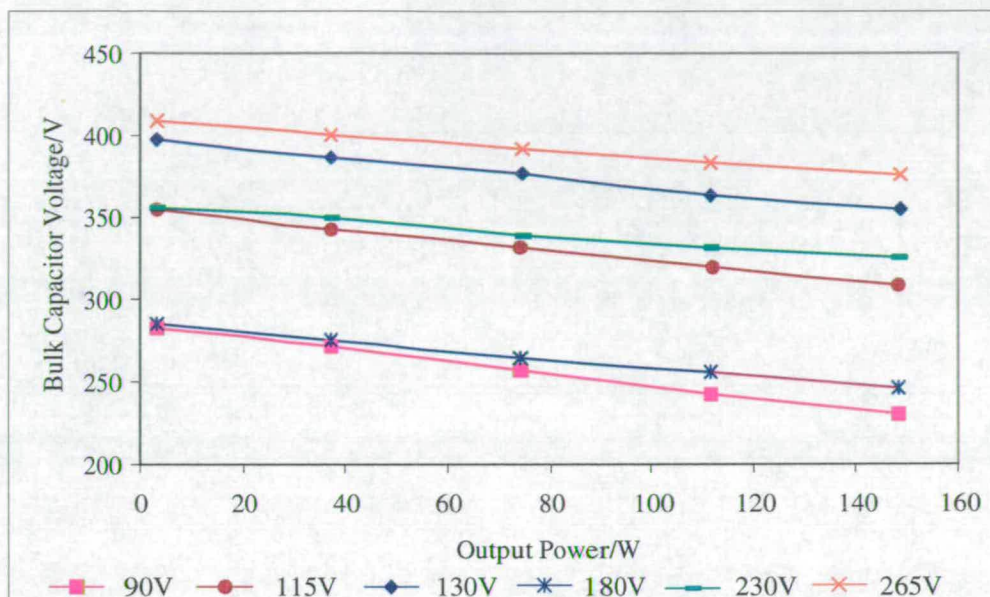
Figure 6.24: Variation of bulk capacitor voltage with output power across the input voltage range
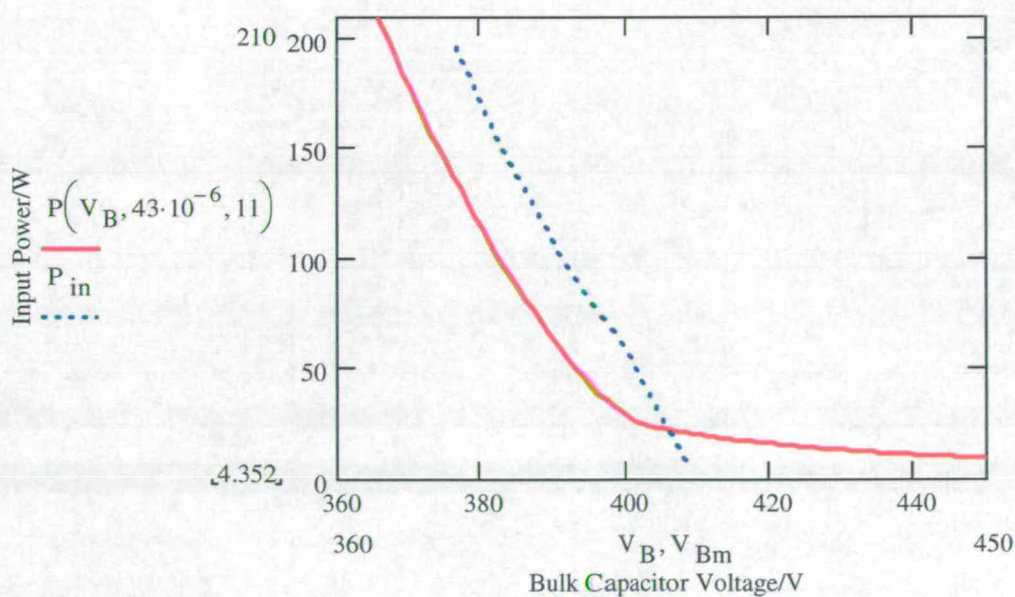
Figure 6.25: Variation of bulk capacitor voltage with input power at 265V (dot trace) compared to the Mathcad prediction

Output Voltage Ripple

Table 6.4 shows the 100kHz and 100Hz ripple on both outputs at 75W and full load output power. The 100kHz ripple on the 5V output ranges from 12.1mV to 20.3mV and on the 12V output from 81.3mV to 181mV. The 12V ripple voltages are higher than that normally specified for a PC power supply (50mV on the 5V output and 120mV on 12V output). The 100Hz ripple on the 5V output ranges from 28mV to 40.6mV and from 93mV to 131mV on the 12V output.

Output Combination	5V 100kHz p-p Ripple/mV	5V 100Hz p-p Ripple/mV	12V 100kHz p-p Ripple/mV	12V 100Hz p-p Ripple/mV
Input Voltage: 90V				
5.05V 10A, 12.71V 2.1A	15.6	28	125	106
Input Voltage: 115V				
5.07V 10.1A, 12.75 2.1A	15.6	35.9	112	112
4.98V 19A, 13.19V 4.2A	18.8	31.3	156	118
Input Voltage: 130V				
5.06V 10A, 12.73V 2.15A	14.1	34.4	118	100
4.98V 19A, 13.17V, 4.2A	17.2	40.6	168	131
Input Voltage: 180V				
5.06V 10.2A, 12.78V 2.1A	20.3	29.7	137	106
4.99V 19A , 13.2V 4.2A	18.8	26.6	181	93
Input Voltage: 230V				
5.08V 10A, 12.71V 2.15A	15.6	34.4	81.3	103
4.98V 19.1A, 13.2V 4.2A	20.3	34.4	121	112
Input Voltage: 265V				
5.07V 10.2A, 12.73V 2.15A	12.1	35.9	87.5	103
4.99V 19.2A, 13.17V 4.2A	20.3	34.4	140	109

Table 6.4: Ripple voltage seen on the 5V and 12V outputs at 100kHz and 100Hz across the input voltage range

6.6.6   Voltage seen on Key Devices

Measured at 265V input, the voltages on S_1 and the diodes are shown in table 6.5.

The voltage measured across S_1 was about 813V, which is about the expected value for a bulk capacitor of 408V. The 5V diodes at 25V are close to their expected voltages of 28V for a bulk capacitor voltage of 408V, as are the 12V diodes at about 57V when their expected voltage is 65V (more than 10%). The voltage measured across D_{4A} or D_{4B} and D_{5A} or

Device	Voltage/V
S_1	813
$D_{2:5V}$	25.6
$D_{3:5V}$	25
$D_{2:12V}$	57.8
$D_{3:12V}$	56.3
D_{4A}/D_{4B}	312
D_{5A}/D_{5B}	231

Table 6.5: Voltage measured across key semiconductor components with 265V input voltage

D_{5B} is about 100V higher than what would be expected (202V for D_4 and 100V for D_5) due to the resonance on the voltage seen across them.

6.7 Conclusion

Analysis has been produced that predicts bulk capacitor voltage, and input RMS current harmonics at an acceptable level. The analysis can be used to test designs with different values of inductances and turns ratios. The analysis needs further work to add an improved method of calculating current when the bulk capacitor voltage is below the line voltage peak, when the bulk capacitors may be peak charged.

The converter was simulated at 100V and 230V with a 150W 5V output to check the harmonics. At 90V the converter was simulated to find the RMS or average current in the semiconductor devices and at 265V to find the peak voltage across the devices.

A prototype converter was built and tested. This converter has good efficiency percentage around the mid 70s. The converter passed class D at full load (150W output) at 100V and 230V, but not down at 75W input power. The lowest input power that it passed at was 97W. The bulk capacitor voltage rises to 408V. This has the knock-on effect, requiring a 1000V MOSFET to be used, which is expensive.

Chapter 7

Forward Converter with Low Frequency Switch - LFSPFC

7.1 Introduction

The bi-forward converter in both forms (with and without input inductor) and the CS S^2PFC converter have a number of undesirable characteristics which have been highlighted in the previous three chapters. The bi-forward suffers from:

- Variable and high voltage on the bulk capacitor when operated with the input inductor

- High voltage stress across MOSFET S_1 (up to 1100V) and the secondary diodes due to the centre tapped primary winding on the transformer

- High current stress in the MOSFET S_1 when operating via the lower tap of the primary winding

Due to these three problems the bi-forward has low conversion efficiency and a high cost. The CS S^2PFC suffers from:

- Variable and high voltage on the bulk capacitor

- High voltage stress across MOSFET S_1 (up to 1000V)

- Does not meet IEC 61000-3-2 at lower powers

- High cost

It would be advantageous if a 800V/900V MOSFET could be used for S_1: this would reduce both cost and losses. Further benefit could be gained by the use of Schottky diodes on the 5V output (bi-forward), giving a much needed increase in efficiency.

The main cause for the problems in the bi-forward is the centre tapped primary transformer winding, but this winding is important as it performs most of the current shaping and power management. It would be useful if there was some other method of performing exactly the same task as the centre tapped primary winding (as in the bi-forward without L_1), but allowing the primary winding of the transformer to reduce back to its usual forward converter form. This would reduce the current and voltage stress on the power MOSFET.

7.2 The LFSPFC Converter

In figure 7.1 is shown the schematic for the LFSPFC converter. This converter was developed in this project as an attempt to solve the problems of the bi-forward and CS S^2PFC dicussed above. A converter based on the flyback topology with a similar switch and diode arrangement has just been presented in [123], but this converter is operating in a very different manner to the one proposed here.
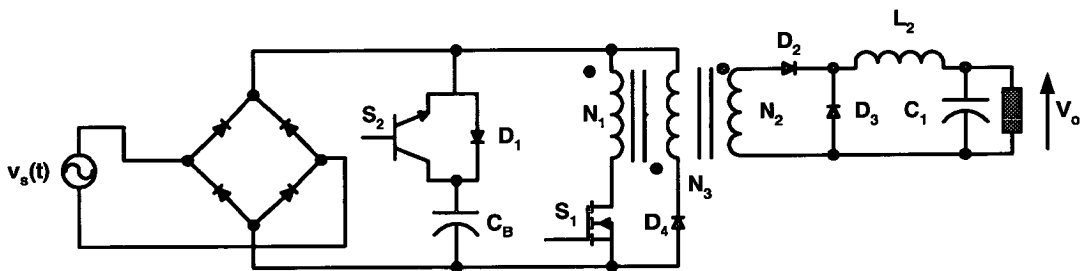
Figure 7.1: Forward converter with auxiliary switch and diode in series with the bulk capacitor C_B

7.2.1 Operation

The switch S_1, transformer and secondary side form an ordinary forward converter that operates in the normal manner, such as voltage mode control with fixed frequency PWM

143

with duty adjusted to keep the output voltage V_o constant. When the input voltage is high the auxiliary switch S_2 is turned off and the output is supplied directly from the converter's input at the main high switching frequency of S_1, in the same manner as the bi-forward in chapter 4 does. The duty cycle is adjusted to keep the output voltage V_o constant as the input voltage $v_s(t)$ changes. When the input voltage is low S_2 is on and the output is supplied from C_B via S_2 in the ordinary manner of a forward converter fed from a capacitor. S_2 is left on all the time when the voltage is low. The bulk capacitor C_B is peak charged through D_1. All that has happened is that the power processing function of the centre tapped primary winding of the bi-forward is now done by switch S_2.

7.2.2 Input Current Waveform

The input current waveform is exactly the same as in the bi-forward converter discussed in chapter 4 (and which is shown in figure 4.3) because the converter is drawing current directly from the supply in the same manner as the bi-forward converter. This means that the converter as it stands should not pass class D and should only just meet class A.

7.2.3 Advantages and Disadvantages of the LFSPFC

The advantages over the bi-forward are:

- The voltage seen across S_1 is only twice the bulk capacitor voltage as in a conventional forward converter.

- The current stress in S_1 is similar to that of a conventional forward converter and not double as in the bi-forward when operating from just the lower tap.

- These two points allow the use of a 800V/900V MOSFET for S_1 giving a significant reduction in overall cost (including the auxiliary switch and its control and drive circuitry).

- A probable increase in efficiency over the bi-forward.

The disadvantages of this converter are:

144

- It draws the same shape current as the conventional bi-forward converter which will not meet class D (but will meet class A).

- It still has a sharp change in input current, which is still discontinuous.

- There is a step change in duty cycle.

7.2.4 Operation of the Auxiliary Switch S_2

Figure 7.2 shows a method of controlling switch S_2. This is based on a simple comparator (eg LM311) which compares the input voltage seen through the voltage divider R_1 and R_2 at the negative input of the comparator, with the reference voltage set by voltage divider R_3 and R_4 from the control IC and gate drive supply for S_1. When the input voltage seen at the negative input falls below the voltage at the positive input of the comparator, S_2 is turned on. When the input voltage seen at the negative terminal rises above that at the positive terminal then S_2 will turn off.
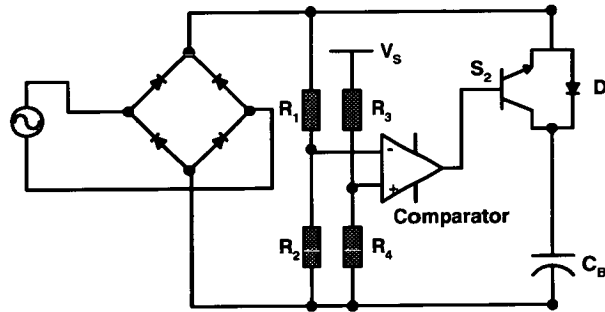
Figure 7.2: Comparator control of auxiliary switch S_2

This arrangement will also turn S_2 on if there is a loss of line voltage, allowing the output to be supplied from C_B. The input voltage at which S_2 turns on and off can be adjusted so as to give the best current harmonics once a circuit is built by making, say, R_4 a variable resistor.

The gate drive for the auxiliary switch S_2 can be implemented using several methods such as a gate drive transformer or a level shift gate drive IC. If the topology is used in an application such as a PC power supply there is an auxiliary converter supplying isolated outputs to the drive circuitry and to the PC. An extra winding on this converter could be used to supply power for the gate drive of S_2 and an opto-coupler, or level shift IC, could be used to level

145

shift the gate drive signal.

7.3 The LFSPFC Converter with Input Inductor

To try and improve the input current shape and ability of the circuit to meet class D regulations the familiar technique of adding an input inductor is used, as shown in figure 7.3. This looks similar to the circuit in [123], but it operates differently with auxiliary switch S_2 operating at a low frequency unlike the same switch in [123] which operates at a high frequency (the same as S_1).
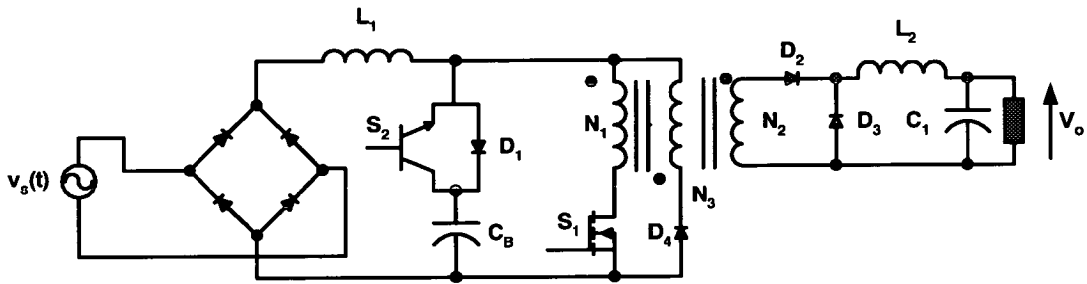
Figure 7.3: Forward converter with auxiliary switch and diode in series with the bulk capacitor C_B with input boost type inductor L_1

7.3.1 Operation

The switch S_2 is operated in the same way as described in section 7.2.4. When the input voltage is low the forward part of the converter is fed from C_B and operates just like an ordinary forward converter as described in section 7.2.1.

Shown in figure 7.4 are the switching frequency waveforms for the current in L_1, S_1 and D_1 when S_2 is off. The current in L_2 is operating in CCM and in L_1 it is DCM. When S_1 is turned on at t_0 the inductor L_1 has applied across it the full line voltage, as turning on S_1 connects the right hand end of L_1 to zero voltage. The current in L_1 starts to ramp up from zero to the reflected load current as seen through the transformer. While the current in L_1 is ramping up the current in L_2 will keep on free wheeling via diode D_3. At t_1 the current in L_1 has ramped up to the current in L_2 seen through the transformer and the current in L_2 stops free wheeling and starts to rise via diode D_2. At this point L_1 and L_2 also connect in

146
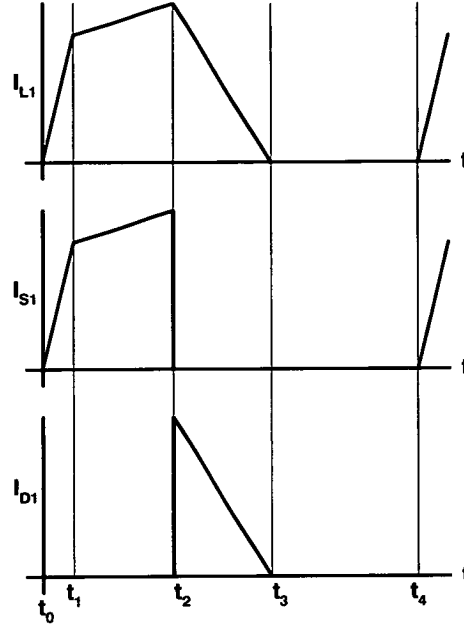
Figure 7.4: Switching frequency waveforms for when S_2 is off

series through the transformer and the current in the pair rises together supplied from the input source $v_s(t)$. At t_2 switch S_1 is turned off. The current in L_2 again freewheels via diode D_3. The current in L_1 is discharged into C_B via diode D_1. At t_3 the current in L_1 reaches zero and stops flowing. At t_4 the cycle is repeated.

7.4   Development of a Prototype Converter

To test if the basic concept of the LFSPFC converter and the LFSPFC converter with input inductor work in practice a test circuit was built which could operate with or without the input inductor L_1. The specifications are;

- Up to 100W output at 5V and 0A to 20A

- Input voltage is $180V_{RMS}$ to $265V_{RMS}$

- Conform to EN 61000 -3-2 class A at full load

- Conform to EN 61000 -3-2 class D at full load

- Switching frequency of 100kHz

The converter is based on the normal forward converter built for the comparison in chapter 8. The basic details are;

- Transformer turns; N_1, N_3: 44 turns, N_2: 5 turns

- Secondary filter L_2: 15.4μH and C_1: 1800μF 16V electrolytic

- Voltage mode control using the UC3524 IC

- D_2 and D_3 are STPS20H100CT, 20A Schottky diodes with a forward voltage drop of 0.71V

- S_1 is the 2SK2611 and is a 900V 9A device with an R$_{dson}$ of 1.1Ω

- D_4 is a BYD33U 1200V diode and DB is the GBU6J

As for the other single stage topologies built there was a RCD snubber across the MOSFET S_1 to the design shown in figure 7.19.

The drive and control for S_2 is shown in figure 7.19 and was implemented using the common LM311 comparator and a signal level shift IC.

The two main design parameters left were the input voltage at which S_2 is turned on and off at and the inductance of L_1 (for the version with input inductor). Another parameter to consider if the converter is designed from scratch and not adapted from an existing design would be the transformer turns ratio, as this determines the amplitude of the reflected secondary current and the charging up time of L_1 and the amount of energy transferred to C_B when L_1 is discharged.

7.5 Analysis

7.5.1 Assumptions

The following assumptions are made in addition to those made in section 4.3.2:

1. During a switching cycle the input voltage is assumed constant.

2. Bulk capacitor voltage for the LFSPFC with input inductor is constant over a half line cycle.

7.5.2   Basic LFSPFC

The input voltage is defined as:

$$v_s(t) = V_{pk} \cdot \sin(\omega \cdot t) \tag{7.1}$$

Turn On and Turn Off Voltage of Switch S_2 for the Basic LFSPFC

The lowest voltage at which S_2 can be turned on or off, V_{inmin}, is determined by the maximum duty ratio possible, D_{max}, and can be expressed as:

$$V_{inmin} = \frac{N_1 \cdot V_o}{N_2 \cdot D_{max}} \tag{7.2}$$

For the UC3524 the maximum duty is 0.45, so the lowest voltage at which S_2 can be turned on and off is 98V rising to the peak of the line voltage.

For a particular turn on/off voltage, V_{S2}, the time after input voltage zero crossing that S_2 turns off is:

$$t_{off} = \frac{\sin^{-1}\left(\frac{V_{S2}}{V_{pk}}\right)}{\omega} \tag{7.3}$$

and it turns back on again at:

$$t_{on} = \frac{T}{2} - t_{off} \tag{7.4}$$

where T is a half line period

The conduction angle of the input current is expressed (in degrees) as:

$$A_c = \left(\frac{T}{2} - t_{off}\right) \cdot \frac{180 \cdot \omega}{\pi} \tag{7.5}$$

Equation 7.5 is plotted in figure 7.5 for 230V input for different values of turn on/off voltage down to 98V where the converter would lose regulation of the output voltage.
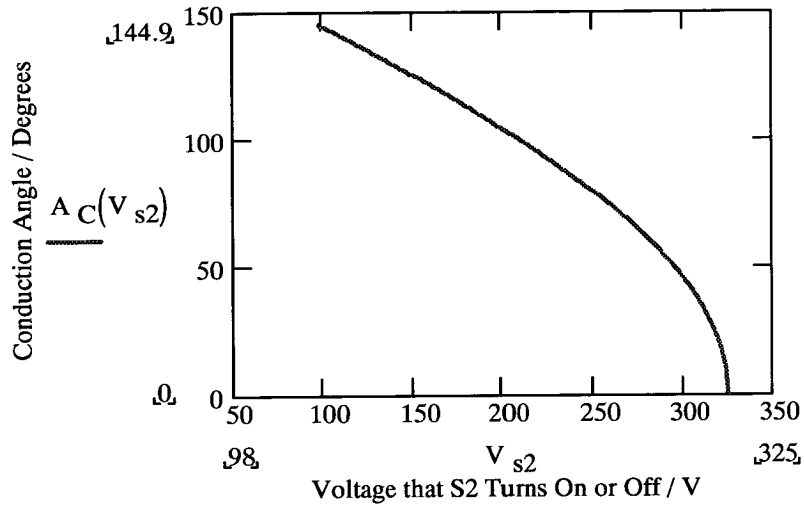
Figure 7.5: Graph of conduction angle of input current against switch S_2 turn on/off voltage

Duty Cycle Variation

When operating from C_B when S_2 is on, the duty cycle is:

$$D_1 = \frac{N_1 \cdot V_o}{N_2 \cdot V_B} \tag{7.6}$$

where V_B is V_{pk}.

When the converter is operating directly from the line the duty cycle is:

$$D_2 = \frac{N_1 \cdot V_o}{N_2 \cdot |v_s(t)|} \tag{7.7}$$

For a half line period the duty can be defined as:

150

$$D = \begin{array}{ll} D_1 & 0 < t < t_{off} \quad t_{on} < t < T \\ D_2 & t_{off} < t < t_{on} \end{array} \tag{7.8}$$

Equation 7.8 is plotted in figure 7.6 for 230V. This plot is slightly different to that for the bi-forward converter shown in figure 4.6 where the duty change between operating from C_B and $v_s(t)$ is smooth: in this converter it is a step change. This is due to there only being one primary winding from which both conduction paths supply the output.
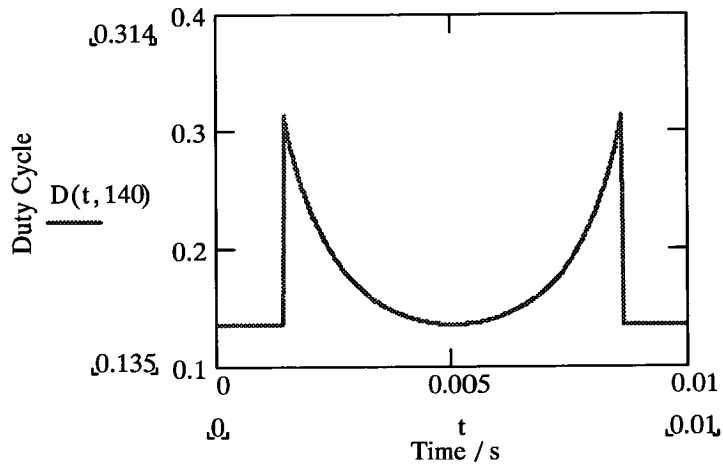
Figure 7.6: Variation of duty cycle over a line half cycle for 230V

Bulk Capacitor Recharge

This is exactly the same as for the bi-forward converter discussed in section 4.3.3.

Overall Input Current

The averaged switching frequency current drawn by the converter from the line can be assumed to be:

$$i_f(t) = \frac{P_o}{v_s(t)} \tag{7.9}$$

and the input current for a half line period is:

151

$$i_s\left(t\right) = \begin{array}{ll} 0 & 0 < t < t_{off} \quad t_{on} < t < \frac{T}{2} \\ i_f\left(t\right) & t_{off} < t < t_r \quad \frac{T}{4} < t < t_{on} \\ i_f\left(t\right) + i_c\left(t\right) & t_r < t < \frac{T}{4} \end{array} \qquad (7.10)$$

Figure 7.7 shows the current waveform produced by equation 7.10. Comparing it to the waveforms shown in figure 4.3, the shape is identical to that drawn by the bi-forward converter. Changing the size of the bulk capacitor will change the height of the recharging peak, as will changing the turn on or turn off voltage of S_2 (as was the case for the bi-forward in appendix B).
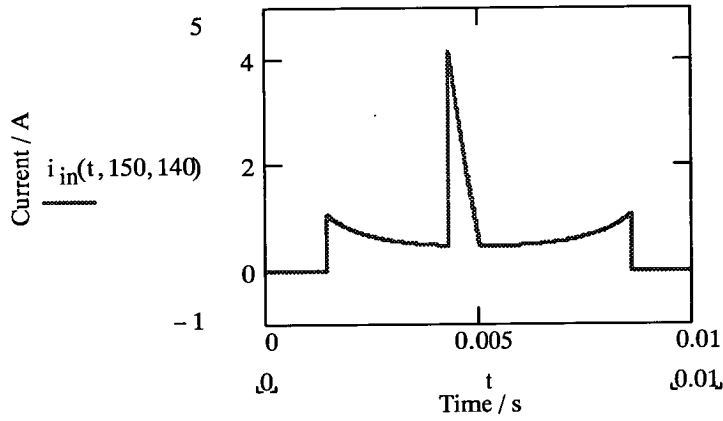
Figure 7.7: Predicted input current waveform for 150W input power at 230V with C_B as 165μH and turn on/off of S_2 at 140V

From equation 7.10 the RMS current harmonics can be calculated from the Fourier series.

Input Current Harmonics to Class A

For this converter the only variable is the turn on/off voltage of S_2. The bulk capacitor capacitance is left at 165μF, the same as is used in the bi-forward and forward converter used elsewhere, but this would be another possible variable when trying to reduce the converter's harmonics below the regulation values. Since the converter will draw the same current shape as the bi-forward converter it is pointless looking at class D as it has already been shown in figure 4.4 as well as in the simulation results shown in table F.1 that the current waveform will not meet class D. Since the other converters (the passively filtered forward converter, the two stage cascaded boost and forward converters, the SS S^{2}PFC converter and

152

bi-forward converters) have already been tested, it was decided to assume an efficiency of 75% giving an input power of 133W. Figure 7.8 shows various turn on/off voltage designs compared to the class A limit.
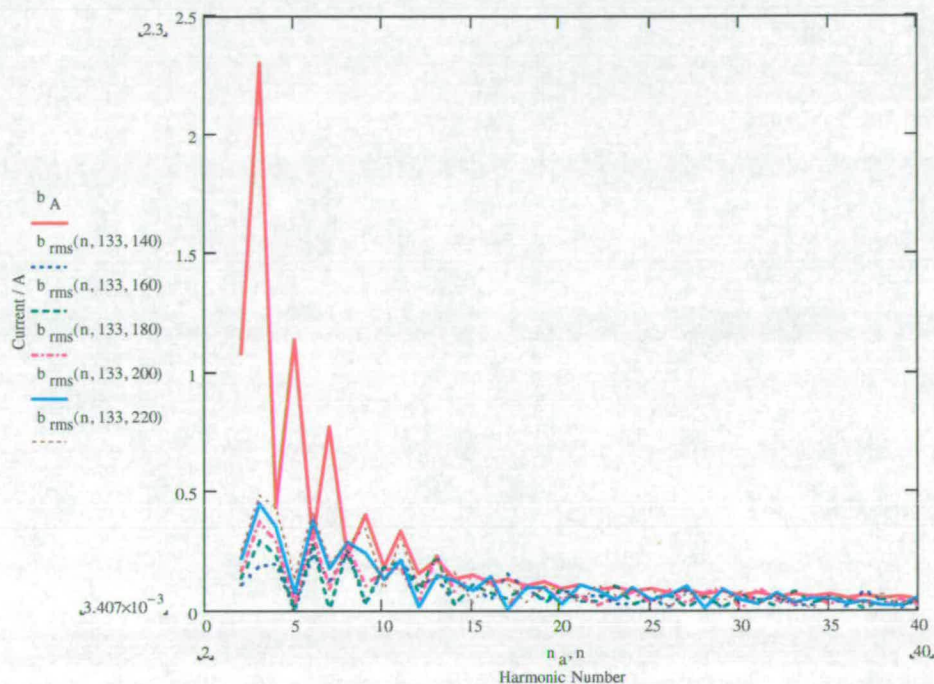
Figure 7.8: RMS input current harmonics compared to the class A (trace b_A) limits for 230V input with the turn on/off voltage of S_2 as 140, 160, 180, 200 and 220V. Traces are listed by side of graph: 1st value is power and 2nd value is the turn on/off voltage for S_2.

Since the input power is lower, this converter is better able to meet the class A regulation than the bi-forward shown in figure 4.5 All five of the different values of S_2 turn on/off voltage just exceed the regulations a little (barely noticeable) from above the 17th harmonic. If the input power of the converter was a little lower, at about 100W, then it will pass class A with ease for all five values. It is likely that when a prototype converter is tested it will pass class A with a 100W output, since the bulk capacitor recharging current will be more smooth, as will the smaller peaks at the start and end of the waveform. The input power may also be lower (similar to the bi-forward of chapter 4). It was decided to turn S_2 on/off at 140V. This value has the lowest harmonic levels with only the 21st harmonic exceeding the class A limit and will give the best chance of meeting the class A limits in practice. If 140V exceeds the limits it will be easy to change the voltage at which S_2 turns on/off by fitting a variable resistor in the voltage divider on the reference leg of the comparator.

Component Stress

The method used was similar to that used in chapters 4, 5 and 6. The predicted values are shown in tables 7.1 and 7.2 on pages 164 and 165 together with simulation values for component stress.

7.5.3   LFSPFC with Input Inductor L_1

The analysis for the turn on and off for S_2 is the same as in section 7.5.2.

Operation of Converter During S_2 off time

From figure 7.4 and applying $v = L \cdot \frac{di}{dt}$ the inductor equation for the time t_0 to t_1 is:

$$v_s(t) = \frac{L_1 \cdot I_{p1} \cdot f_s}{\Delta D} \tag{7.11}$$

where I_{p1} is the current in L_1 and the reflected current in L_2 at t_1 (both the same) and f_s is the switching frequency.

At t_1 the current in L_1 reaches the reflected current in L_2 and the two connect in series. The equation becomes:

$$v_s(t) - \frac{N_1}{N_2} \cdot V_o = \frac{\left(L_1 + \left(\frac{N_2}{N_1}\right)^2 \cdot L_2\right) \cdot (I_{p2} - I_{p1}) \cdot f_s}{D_{eff}} \tag{7.12}$$

where I_{p2} is the peak current in L_1 and the reflected current in L_2 rises to between t_1 and t_2. D_{eff} is defined as

$$D_{eff} = D - \Delta D \tag{7.13}$$

D_{eff} is the effective duty ratio for the current in L_1, D is the duty ratio of S_1 and ΔD is the duty ratio for the rise of current in L_1 from zero.

When S_1 turns off at t_3, L_1 discharges into C_B. This is defined by:

154

$$V_B - v_s\left(t\right) = \frac{L_1 \cdot I_{p2} \cdot f_s}{D_f} \tag{7.14}$$

Now considering L_2, the up ramp for the current is defined by:

$$\frac{N_2}{N_1} \cdot v_s\left(t\right) - V_o = \frac{\left(L_2 + \left(\frac{N_2}{N_1}\right)^2 \cdot L_1\right) \cdot \Delta I_o \cdot f_s}{D_{eff}} \tag{7.15}$$

and the down ramp, ΔI_o, for L_2 is defined by:

$$V_o = \frac{L_2 \cdot \Delta I_o \cdot f_s}{1 - D_{eff}} \tag{7.16}$$

Considering the flux balance across L_2, equations 7.15 and 7.16 can be equated and solved to give D_{eff} as:

$$D_{eff} = \frac{V_o \cdot \left(L_2 + \left(\frac{N_2}{N_1}\right)^2 \cdot L_1\right)}{\left(\frac{N_2}{N_1} \cdot v_s - V_o\right) \cdot L_2 + V_o \cdot \left(L_2 + \left(\frac{N_2}{N_1}\right)^2 \cdot L_1\right)} \tag{7.17}$$

ΔI_o can be found by substituting D_{eff} into equation 7.16 or 7.15. From ΔI_o the peak and minimum values of the ripple current can be found and transferred to the primary as:

$$I_{p1} = \frac{N_2}{N_1}\left(I_o - \frac{\Delta I_o}{2}\right) \tag{7.18}$$

$$I_{p2} = \frac{N_2}{N_1}\left(I_o + \frac{\Delta I_o}{2}\right) \tag{7.19}$$

where I_o is the average output current.

Substituting I_{p1} into equation 7.11 the duty ΔD can be found, and substituting I_{p2} into equation 7.14 the fall duty, D_f, can be found.

Figure 7.9 shows how the various parts the duty cycle change when operating from $v_s\left(t\right)$. ΔD is very small which in turn makes the difference between D and D_{eff} also very small.

155
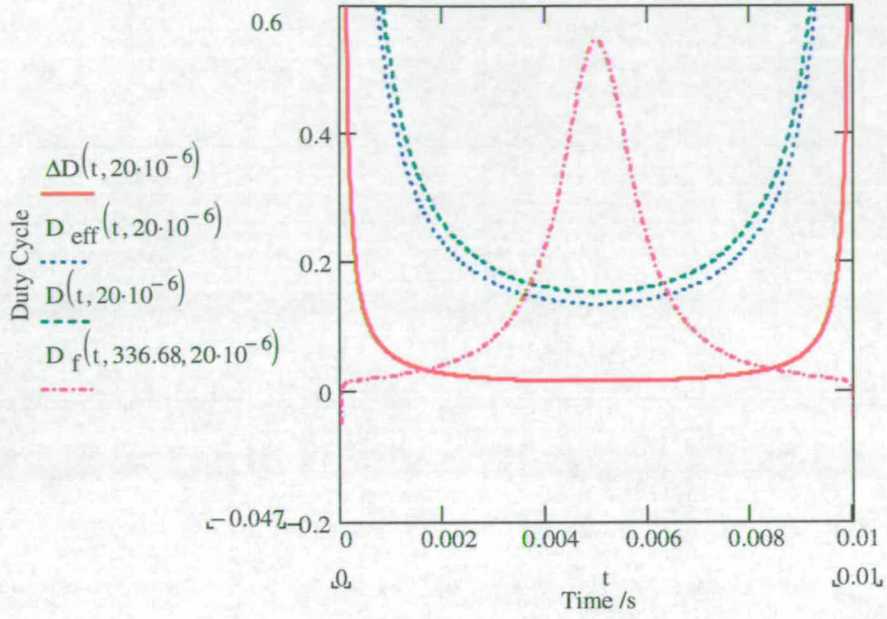
Figure 7.9: Duty cycle variation over a half line period showing ΔD, D_{eff}, D and D_f for L_1 as $20\mu H$ and V_B as $336.68V$ (Value of V_B for a turn on/off voltage of $220V$ at an input power of $133W$)

This is different to the bi-forward with input inductor where ΔD is much longer (see figure 5.16).

The average current, I_{av}, in L_1 during this period is considered as:

$$I_{av} = \frac{\Delta D \cdot I_{p1}}{2} + \frac{D_{eff} \cdot (I_{p1} + I_{p2})}{2} + \frac{D_f \cdot I_{p2}}{2} \tag{7.20}$$

The complete input current, $i_s(t)$, to the converter is:

$$i_s(t) = \begin{array}{ll} 0 & t_a < t < t_b \quad t_c < t < t_d \\ i_{av}(t) & t_b < t < t_c \end{array} \tag{7.21}$$

The input power, P_{in}, is:

$$P_{in} = \frac{2}{T} \cdot \int_{t_{off}}^{t_{on}} v_s(t) \cdot i_{av}(t) \, dt \tag{7.22}$$

156

The RMS current harmonics can be worked out from the Fourier series.

RMS Input Current Harmonics

Figures E.1, E.2 and E.3 in appendix E show the current harmonics for S_2 turned on/off at 140, 160, 180, 200 and 220V with L_1 as 10, 20 and 30μH respectively for an input power of 133W. Figure E.1 shows all the curves are exceeding the class D limit (different harmonics for each curve). For L_1 at 20μH (figure E.2) all the curves still exceed the class D limits, but they are now closer to the class D limit. The black curve, which is for a 220V turn on/off voltage, looks to be the closest to the class D limit. Similarly, for L_1 at 30μH (Figure E.3) the curves exceed the class D regulation values for certain harmonics, but the curves have become closer to the class limit, and the black curve for 220V turn on/off of S_2 seems closest to them. The light blue curve (turn on on/off voltage of 200V) in figure E.2 has what is likely to be an anomaly for the 27th harmonic, as it is very large.

From figures E.1, E.2 and E.3 the 220V curve gives a result closest to the class D limit at 133W input. Further investigation around this figure showed that a turn on/off voltage for S_2 of 230V performed far better harmonically. This is shown in figures 7.10 for 133W input power where the turn on/off voltage is 230V with L_1 at 10, 20, 30 and 35μH. With an input power of 133W the curves for 20, 30 and 35μH are almost the same as the class D regulation curve (except 20μH on the 9th harmonic). The low harmonics of the 3rd, 5th and 7th are below the regulation curve. With L_1 at 10μH the harmonic levels are still exceeding the class D Limit by a large margin.

The addition of the inductor reduces the harmonic level considerably, but not enough to meet the class D regulations. It is worth comparing the RMS harmonic levels with class A as well. This is shown in figure 7.11 for L_1 at 10μH for an input power of 133W. 10μH was shown to have harmonic levels in excess of class D in figure E.1, but when compared to class A with the same set of turn on/off voltages curves are all below the class A limits. A similar result is seen for L_1 at 20μH and 30μH. This is quite an improvement over the basic LFSPFC and the basic bi-forward, where it is possible that the design (turn on/off as 140V) with the lowest harmonic levels for 133W may not pass class A.
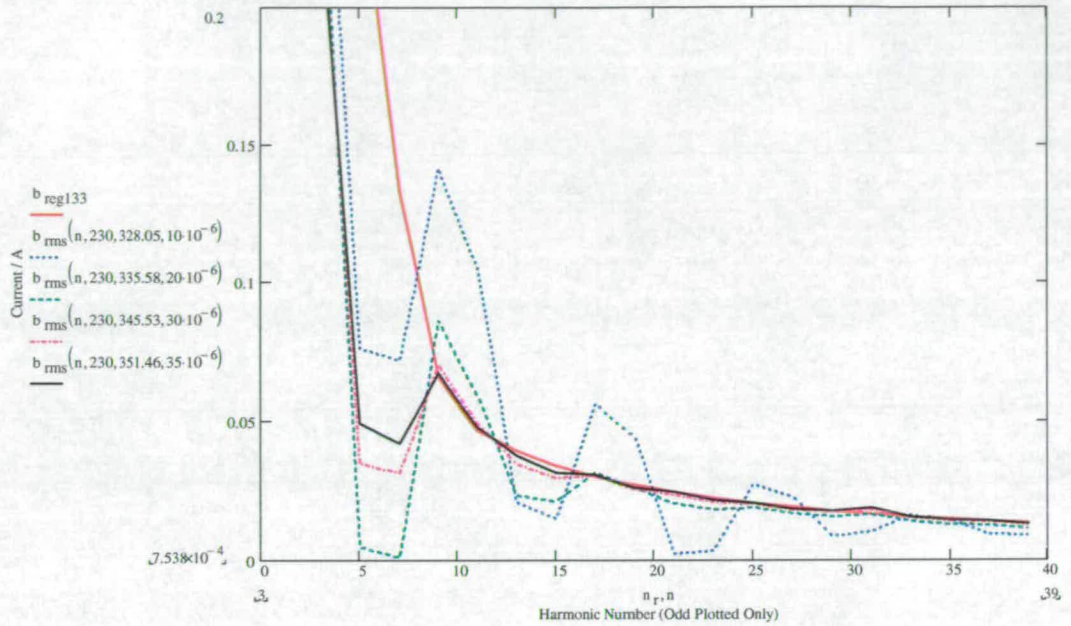
Figure 7.10: RMS input current harmonics compared to the class D (trace b_{reg133}) limits for 230V, 133W input with the turn on/off voltage of S_2 at 230V with L_1 as 10, 20, 30 and $35\mu H$. Traces are listed by side of graph: 1st value is the turn on/off voltage for S_2, 2nd value is the voltage on C_B and 3rd value is the value of L_1.
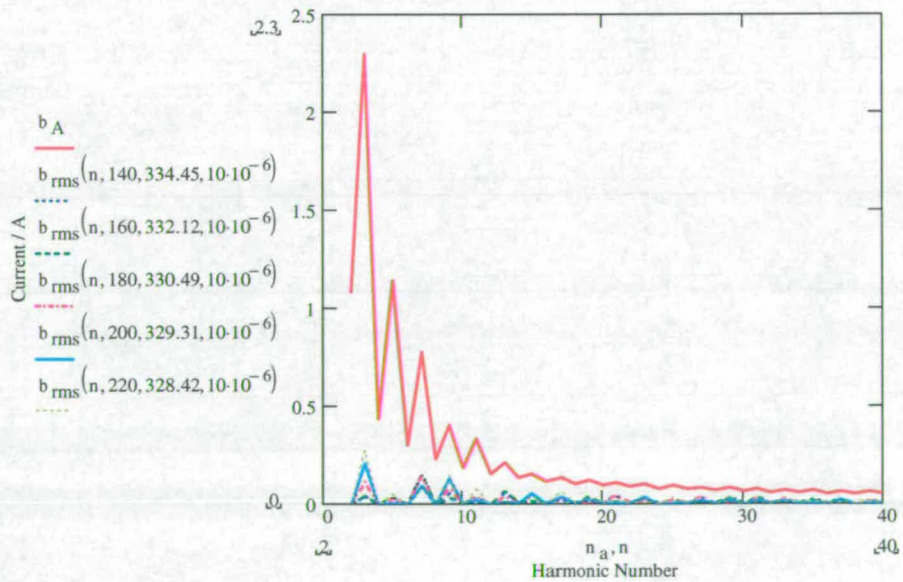
Figure 7.11: RMS input current harmonics compared to the class A (trace b_A) limits for 230V, 133W input with the turn on/off voltage of S_2 as 140, 160, 180, 200 and 220V and L_1 as $10\mu H$. L_1 as $20\mu H$ and $30\mu H$ produce a similar result. Traces are listed by side of graph: 1st value is the turn on/off voltage for S_2, 2nd value is the voltage on C_B and 3rd value is the value of L_1.

Voltage on the Bulk Capacitor C_B

Figures 7.12, 7.13 and 7.14 show the variation of bulk capacitor voltage for turn on/off voltages of 140, 160, 180, 200, 220 and 230V with L_1 at 10, 20 and 30μH. All the curves for the different turn on/off voltages with different inductance values follow the same shape, which is a rise in voltage as the power increases. Bulk capacitor voltage also rises as the the turn on/off voltage falls. So for each set of L_1 the turn on/off voltage of 140V always has the highest voltage across the bulk capacitor and the 230V curve the lowest. This is good because a turn on/off of 230V also has the lowest harmonic content, giving the best current shape with the lower bulk capacitor voltages. The reason for this behaviour is similar to that for the bi-forward with input inductor. Over a half line cycle the energy (charge) into and out of the bulk capacitor will balance. At low output power this balance is achieved at a lower bulk capacitor voltage.

Remembering that S_1 is a 900V MOSFET, the voltage across the bulk capacitor should not exceed much more than 400V. In figure 7.12 where L_1 is 10μH the voltage across the bulk capacitor is below 400V for all the turn on/off curves, with the highest being 390V for 140V turn on/off. In figure 7.13 where L_1 is 20μH, the maximum voltage is 428V which is again for the 140V on/off curve. This is too high, as is the 414V for the 160V curve. The lowest maximum is 392V from the 230V curve. In figure 7.14 where L_1 is 30μH all the maximum voltages are above 400V. The curve for 230V turn on/off is just acceptable at 410V. The curves for 220 ($V_B = 414$V), 200 ($V_B = 424$V), 180 ($V_B = 438$V), 160 ($V_B = 458$V) and 140V ($V_B = 489$V) have bulk capacitor voltages that are too high.

From figures 7.12, 7.13 and 7.14 and cross-referencing with the RMS harmonic level graphs E.1, E.2, E.3, 7.10, and 7.11, then:

- A turn on/off voltage of 230V and L_1 as 10μH should meet class A with the lowest bulk capacitor voltage.

- A turn on/off voltage of 230V with L_1 as 20μH or 30μH may meet class D with the lowest bulk capacitor voltage.

Figure 7.15 shows the predicted input current waveform.
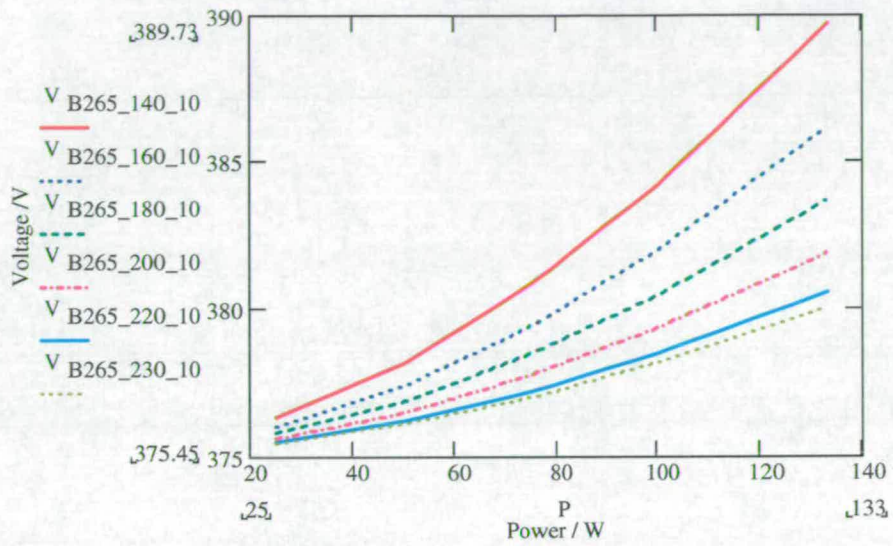
Figure 7.12: Voltage on bulk capacitor C_B against power with L_1 as 10μH with turn on/off voltages for S_2 of 140V, 160V, 180V, 200V, 220V and 230V. Traces are listed by side of graph: 1st value is the input voltage, 2nd value is the turn on/off voltage for S_2 and 3rd value is the value of L_1.
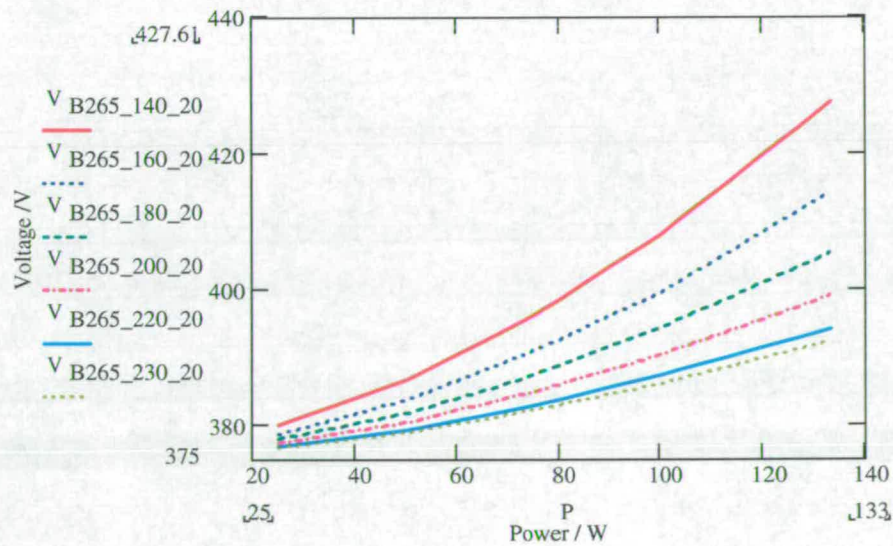
Figure 7.13: Voltage on bulk capacitor C_B against power with L_1 as 20μH with turn on/off voltages for S_2 of 140V, 160V, 180V, 200V, 220V and 230V. Traces are listed by side of graph: 1st value is the input voltage, 2nd value is the turn on/off voltage for S_2 and 3rd value is the value of L_1.
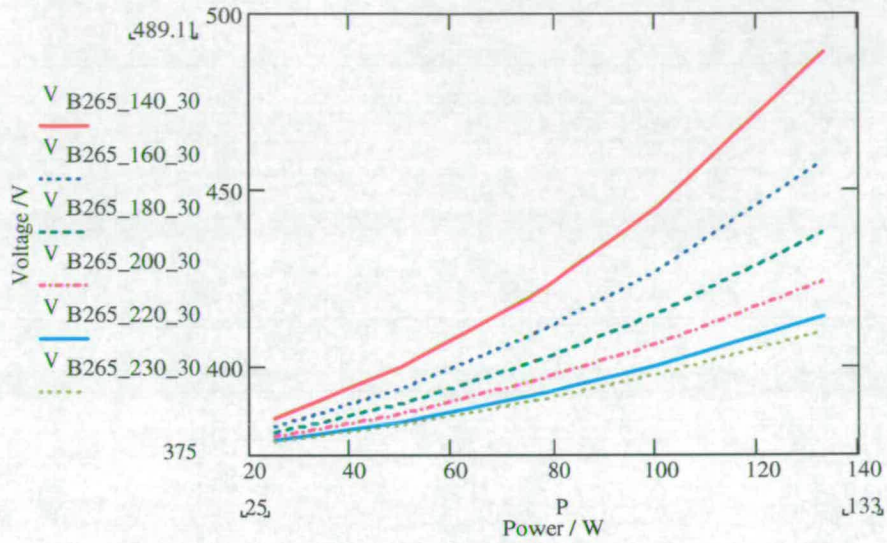
Figure 7.14: Voltage on bulk capacitor C_B against power with L_1 as 30μH with turn on/off voltages for S_2 of 140V, 160V, 180V, 200V, 220V and 230V. Traces are listed by side of graph: 1st value is the input voltage, 2nd value is the turn on/off voltage for S_2 and 3rd value is the value of L_1.
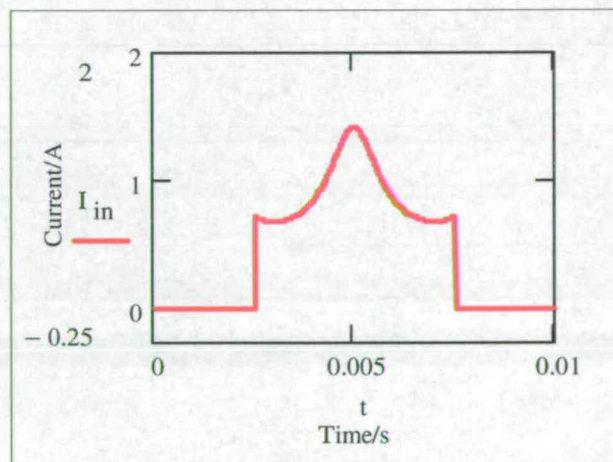
Figure 7.15: Predicted input current waveform with a turn on/off voltage of 230V and L_1 as 20μH for 133W power

161

Component Stress

Following the same procedure as for the basic LFSPFC, the peak voltage across the semi-conductors are shown in table 7.1 on page 164 for an input voltage of 265V. Also following the same method as for the basic LFSPFC, the average or RMS currents for the semicon-ductor components are given in table 7.2 on page 165 for an input voltage of 180V. The current through S_1 is assumed not to contain the ramp up from zero during time t_1 to t_2, which is a small part of the current waveform.

At 180V input voltage the analysis shows that L_1 will enter CCM. The analysis for when L_1 is operating in CCM has not been investigated thoroughly as the intention is to operate L_1 in DCM at 230V input voltage where the converter has to meet IEC 61000-3-2. This is why the current in D_1 is not calculated and the current rise in S_1 is not considered. They are checked in simulation.

For diode D_1 the BY329-1000, 1000V 8A diode is used and for S_2 the IRG4BC30W a 600V IGBT is used.

7.6 Simulation

Figure 7.16 shows the PSpice simulation schematic used without L_1. The input inductor L_1 is placed between C_4 and D_5 when required. Diode D_5 is added to make the simulation run more quickly. For the basic LFSPFC, simulation was carried out with a turn on/off voltage for S_2 of 140V. For the LFSPFC converter with input inductor, simulation was carried out with L_1 at $20\mu H$ and a turn on/off voltage for S_2 of 230V.

7.6.1 Simulation Results

Table F.7 in appendix F shows the simulated input RMS current harmonics compared to class A and D for an input power of 115W (output power is 100W). For class A all the simulated harmonics are below the regulation values for the converter with and without L_1. For class D the 9th, 11th, 23rd, 27th, 35th and 39th harmonics exceed the regulation for the converter with L_1. The analysis predicts failure on the 9th, 11th and 17th harmonics so there is some agreement. All of the simulated failures apart from the 9th and 11th harmonics are

Figure 7.16: PSpice schematic

	LFSPFC		LFSPFC with L_1	
Device	PSpice Voltage/V	Mathcad Voltage/V	PSpice Voltage/V	Mathcad Voltage/V
S_1	746	749	769	785
S_2	233	235	143	162
D_1	232	235	143	162
D_2	41.6	42.6	42.9	44.6
D_3	41.3	42.6	42.7	44.6
D_4	743	750	–	–
D_B	374	375	374	375

Table 7.1: Peak voltage across key devices predicted by PSpice simulation and compared to predicted voltages from the analysis for an input voltage of 265V at 100W output (about 115W input). L_1 is 20μH.

within 10% of the regulation level for that harmonic, so there is a possibility it could pass class D. Without L_1, and with an on/off voltage for S_2 of 140V the converter fails class D from the seventh harmonic onwards by a considerable margin.

Table 7.1 shows the peak voltages predicted by PSpice simulation compared to that calculated in the analysis. All figures are within 10% of each other giving reasonable agreement. The PSpice voltages for S_1, S_2 and D_1 for the converter with L_1 are about 20V below the calculated values: this is due to the average bulk capacitor voltage in the simulation being about 10V (384V) lower than that predicted in the analysis (393V). This partly is due to the analysis figures being produced at an assumed input power of 133W instead of the 114W of the simulation. The voltage stresses in this converter are reasonable and allow the use of cheaper, lower rated devices.

Table 7.2 compares the average or RMS current through the semiconductors at 180V input voltage predicted by PSpice with that predicted by analysis both considering and not considering semiconductor losses. The losses considered are the diode forward bias voltage and switch on-state voltage. The simulated results agree well with the results from the analysis considering losses and are within 10% of each other. The analysis results not considering losses are outside of 10% of the simulated results for S_1, S_2 and D_2 with L_1 in the converter.

Device	PSpice average or RMS Current/A	Mathcad average or RMS Current/A	Mathcad average or RMS Current/A including Diode/ Switch drops
Basic LFSPFC Converter			
S_1 (RMS)	1.12	1.01	1.10
S_2 (RMS)	0.654	0.576	0.632
S_2 (Av)	0.183	0.146	0.176
D_1	0.170	0.148	0.178
D_2	4.69	3.94	4.66
D_3	15.1	16.1	15.3
D_4	16.3m	—	—
D_B(per diode)	0.286	0.225	0.253
LFSPFC Converter with L_1			
S_1 (RMS)	1.06	0.95	1.05
S_2 (RMS)	0.892	0.798	0.885
S_2 (Av)	0.346	0.28	0.344
D_1	0.336	—	—
D_2	4.32	3.49	4.22
D_3	15.5	16.5	15.8
D_B(per diode)	0.269	—	—

Table 7.2: Average or RMS current in key devices predicted by PSpice for an output power of 100W and an input power of 116W compared to predicted average or RMS current for 100W throughput power in the analysis, and predicted values from analysis including diode and switch voltage drops for a throughput power of 100W.

7.6.2 Simulation Waveforms

Figure 7.17 shows the input current, the averaged input current and the gate driving voltage of switch S_2 showing when it is on and off for the LFSPFC converter without L_1 and a turn on/off voltage for S_2 of 140V. The input current (bottom trace) unless filtered will be formed of 100kHz current pulses. The triangular part of the waveform is the bulk capacitor being recharged. The middle trace shows the averaged or filtered input current waveform represented as a voltage across R_{14}. This waveform is the same shape as that drawn by the basic bi-forward shown in figure 4.9.
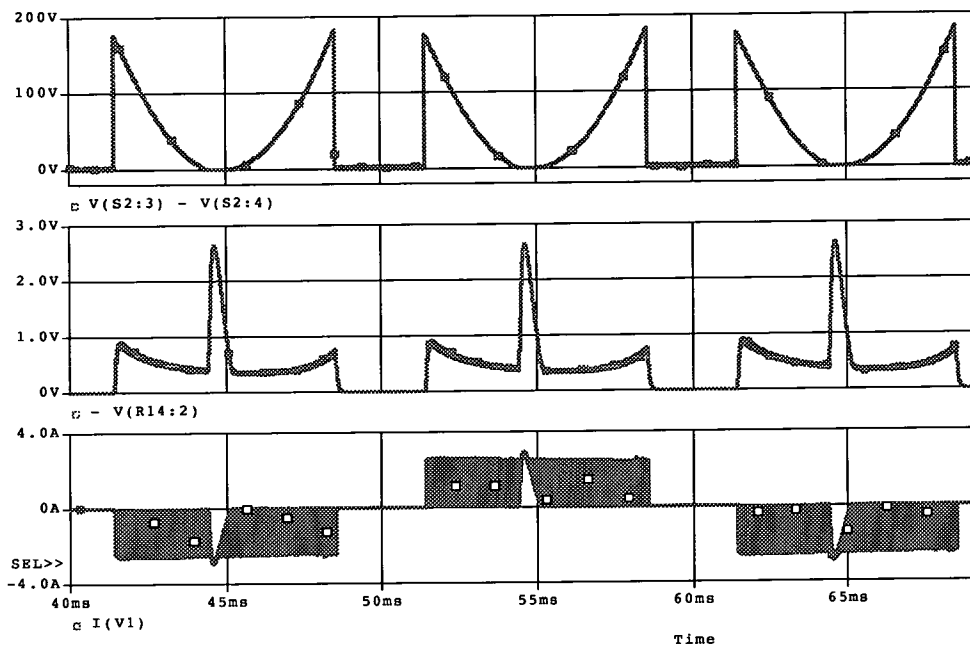
Figure 7.17: Simulated input current at 230V input and 100W output power for a turn on/off voltage of 140V. Top trace: Gate voltage of switch S_2. Middle trace: averaged current seen across as a voltage across R_{14}. Bottom trace: Input current.

Figure 7.18 shows the input current, the averaged input current and the turn on/off of S_2 for the LFSPFC converter with L_1. The input current (bottom trace) is again made up of 100kHz pulses, but this time there is no continuous bulk capacitor recharging current as it is charged at 100kHz after each switching cycle. The averaged or filtered input current (middle trace) shows a similar shape to that predicted in the analysis in figure 7.15, but leaning to the left due to the change in voltage on the bulk capacitor over a line half period.

166
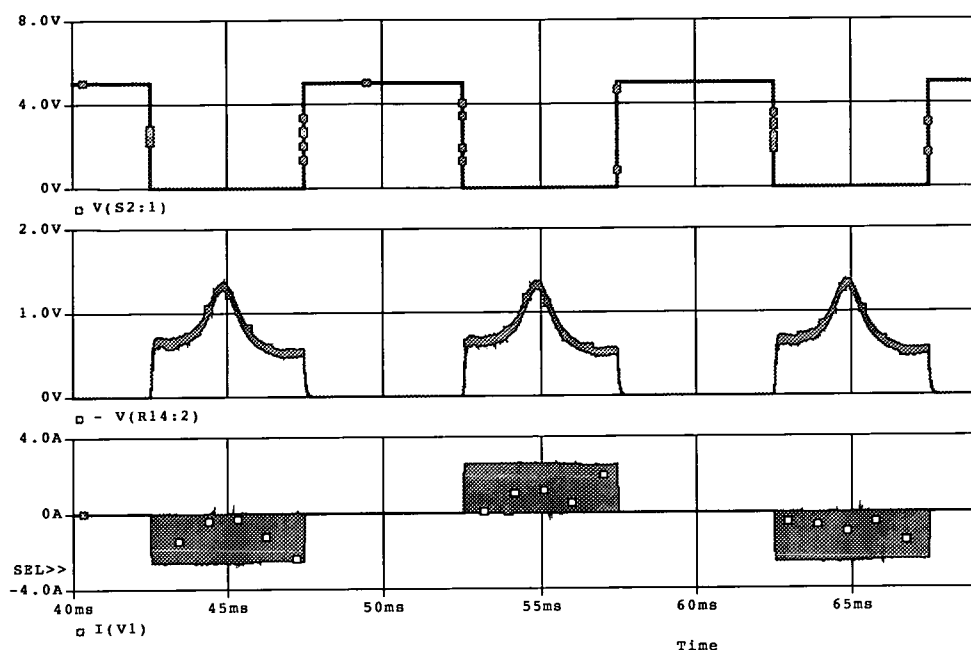
Figure 7.18: Simulated input current at 230V input and 100W output power. Top trace: gate voltage of switch S_2. Middle trace: averaged current seen across as a voltage across R_{14}. Bottom trace: Input current with L_1 as $20\mu H$ and a S_2 turn on/off voltage of 230V.

7.7 Experimental Results

Figure 7.19 shows the final and complete circuit schematic tested. The actual components used are listed in table G.3 in appendix G and a photograph of the final circuit is shown in figure 7.20.

This converter was developed after the tests on the other converters were completed and the test equipment used previously was not available. Thus testing was carried out using an isolation transformer and auto-transformer for the input voltage. As the supply voltage waveform in the laboratory is not very sinusoidal an LC tuned filter was used on the output of the transformers to produce a more sinusoidal voltage source when carrying out the input current harmonic measurements.

The test equipment previously used either filtered the input current or displayed what the averaged input current looked liked. The transformers achieved a similar effect, apart from when using the LC tuned filter. To see the current shape an additional LC current filter was added on the input of the converter (see figure 7.21). This filter also helped give an idea of
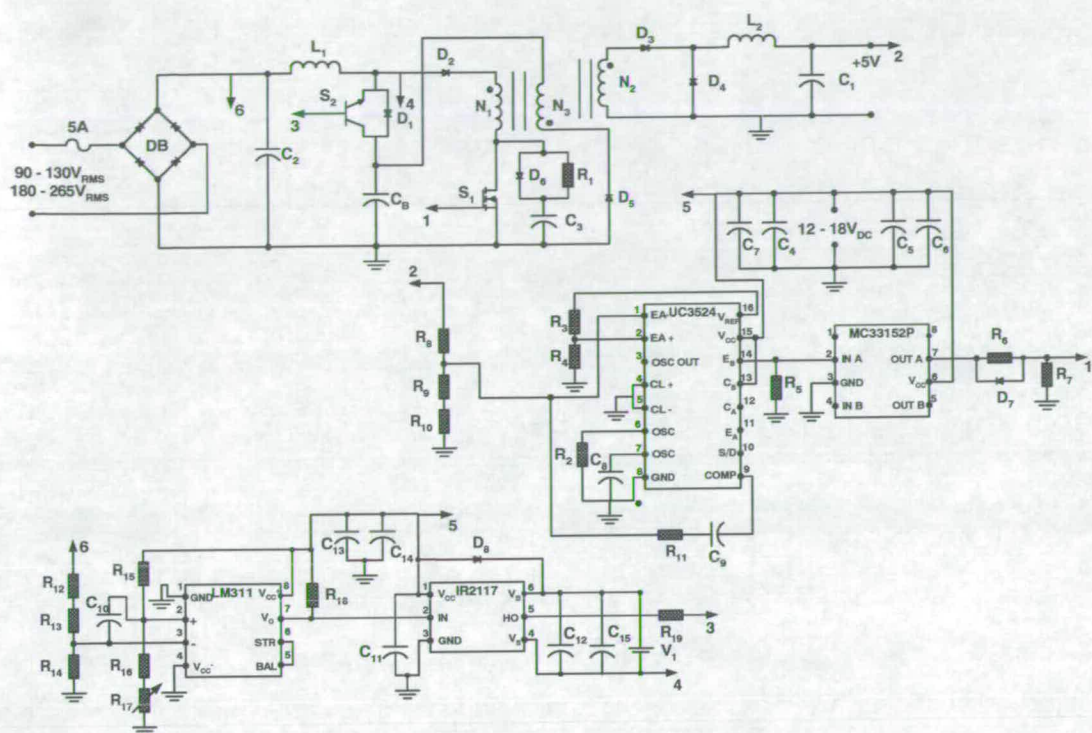
Figure 7.19: Final and complete circuit schematic for the LFSFPFC converter with L_1
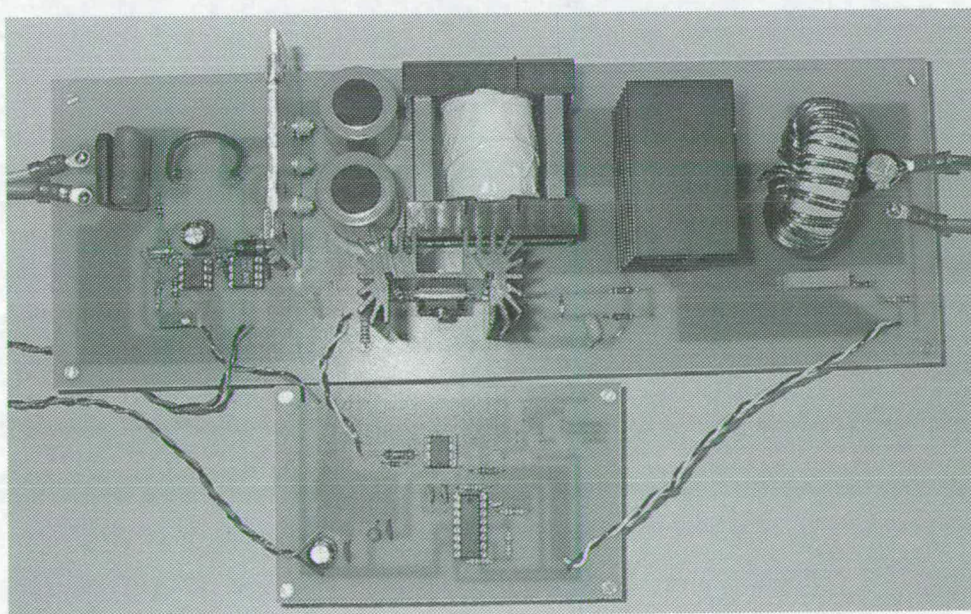
Figure 7.20: Photograph of the LFSFPFC converter without L_1

the filtering requirements of this converter and the bi-forward converter.
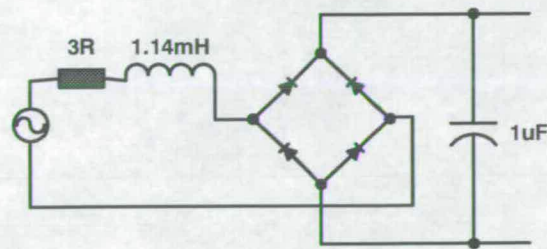
Figure 7.21: Input current filter to filter switching frequency current. Set to a resonant frequency of 4.7kHz

The LFSPFC converter with input inductor was built with L_1 as $20\mu H$ and an S_2 turn on/off voltage of 230V. To show the effect of adding L_1 to the converter, the power supply was also tested without L_1 with a turn on/off voltage of S_2 as 230V. The main testing for the LFSPFC converter without L_1 was done with a turn on/off voltage for S_2 of 140V.

7.7.1 RMS Input Current Harmonic Levels Compared to Classes A and D

Figure 7.22 shows the RMS input current harmonics for a 230V input voltage compared to class A. Only the odd harmonics are shown as all the even harmonics are well below the class A limits. The input filter was fitted. Figure 7.22 shows that all the harmonics are well below the class A limits for all three versions tested. The version without L_1 and a turn on/off voltage for S_2 of 140V shows a better performance than predicted by Mathcad and PSpice. The main reason for this is the smoothed bulk capacitor recharging peak which in Mathcad and PSpice is shown as sharp and short; in practise it is filtered slightly by circuit parasitics and filtering.

Figure 7.23 shows the RMS input current harmonics for a 230V input voltage compared to class D for the converter with and without L_1. The input filter was fitted. The version of the converter without L_1 and a turn on/off voltage of 230V exceeded the class D regulations for the 11th, 13th, 15th, 17th, 19th, 21st, 23rd, 25th, 27th and 29th harmonics. While the version with a turn on/off voltage of 140V exceeded class D on the 7th, 9th, 11th, 15th, 17th, 19th, 23rd, 29th and 31st harmonics. When L_1 is fitted the converter only exceeds on the 13th harmonic by about 50% and 23rd harmonic by about 19%. Both PSpice and Mathcad did not predict failure on the 13th harmonic, but did predict a failure on the 11th. Even
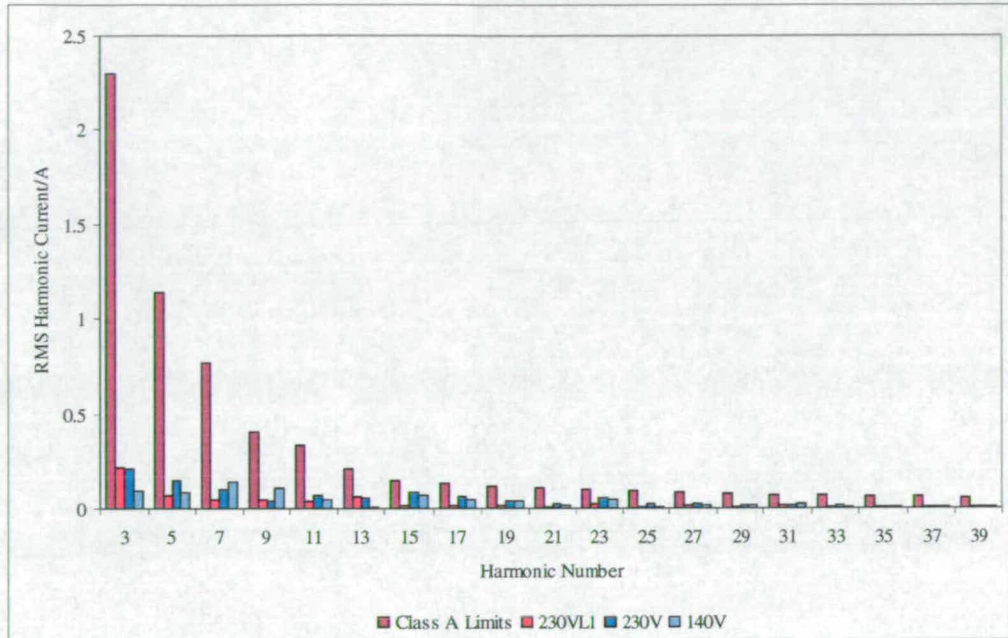
Figure 7.22: Odd harmonics compared to the class A limits for a full load input power of 127W at 230V and a turn on/off voltage for S_2 of 140V and 230V with and without L_1 (20μH)

though this is not a pass at class D, it is a considerable improvement. The 23rd harmonic is not a serious concern if a method can be found to reduce the 13th harmonic, such as increasing the size of L_1 or changing the turn on/off voltage of S_2. Harmonics above the 21st can exceed the regulation by 50% if certain conditions are met [2].

7.7.2   Waveforms

Figure 7.24 shows the filtered input current waveform for a switch on/off voltage for S_2 of 140V.

Figure 7.25 shows the input current waveform with L_1 in the circuit at full output load and with the input current filter fitted, and figure 7.26 shows the same converter input current waveform without L_1. They are not dissimilar, but the waveform in figure 7.25 is smoother.

Investigating the current in L_1, without the input current filter, the current flows in DCM at 230V$_{RMS}$, but at 180V$_{RMS}$ the current in L_1 was entering CCM from about half load and higher. With the input current filter fitted the current in L_1 also operates in CCM at 230V$_{RMS}$ but not at full load.
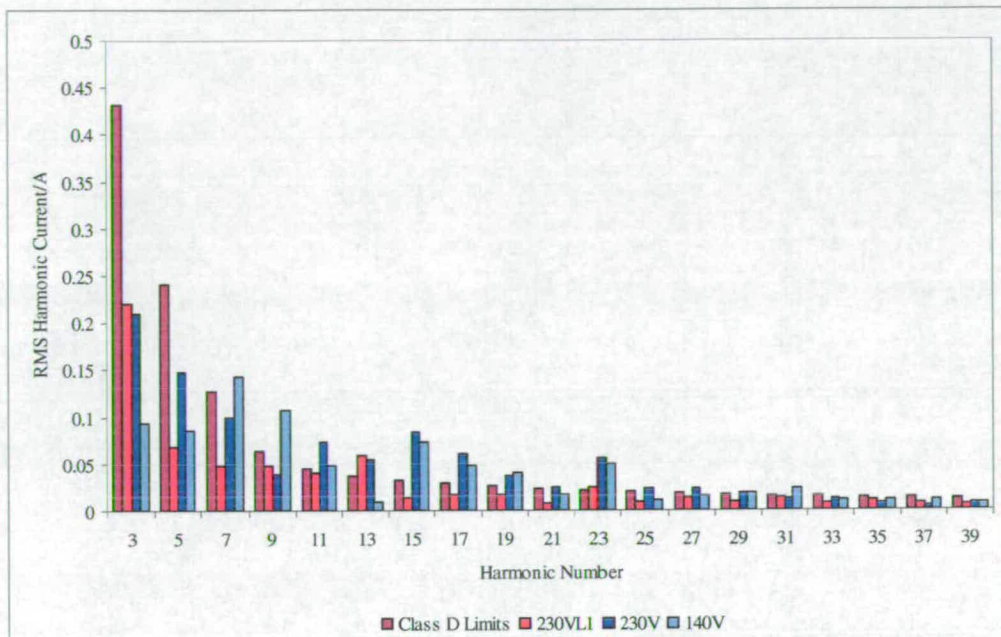
Figure 7.23: Odd harmonics compared to the class D limits for a full load input power of 127W at 230V and a turn on/off voltage for S_2 of 140V and 230V with and without L_1 (20μH)
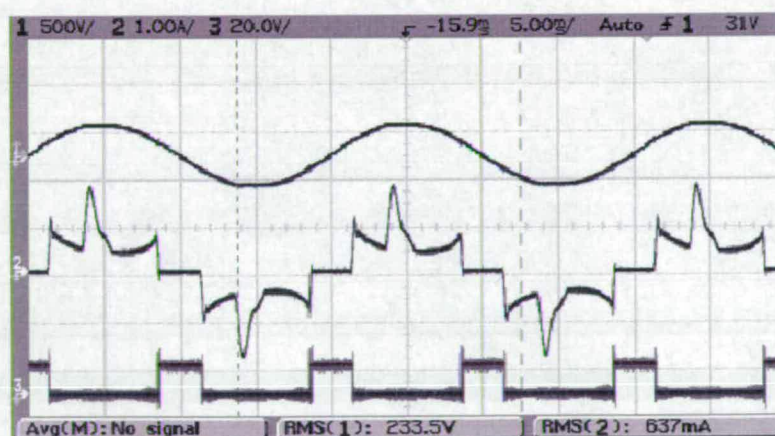
Figure 7.24: Input current without L_1 and a turn on/off voltage for S_2 of 140V. Top trace: Input voltage. Middle trace: Input current. Bottom trace: Output voltage from the comparator.
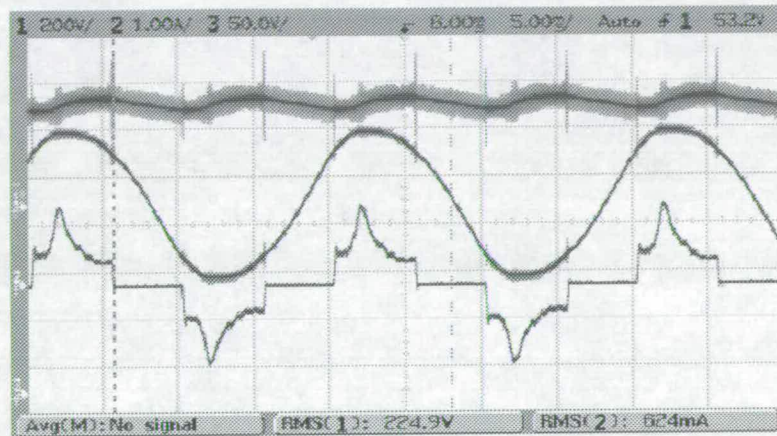
Figure 7.25: Input current with L_1 as 20μH and a turn on/off voltage for S_2 of 230V. Top trace: Bulk capacitor voltage. Middle trace: input voltage. Bottom trace: input current.
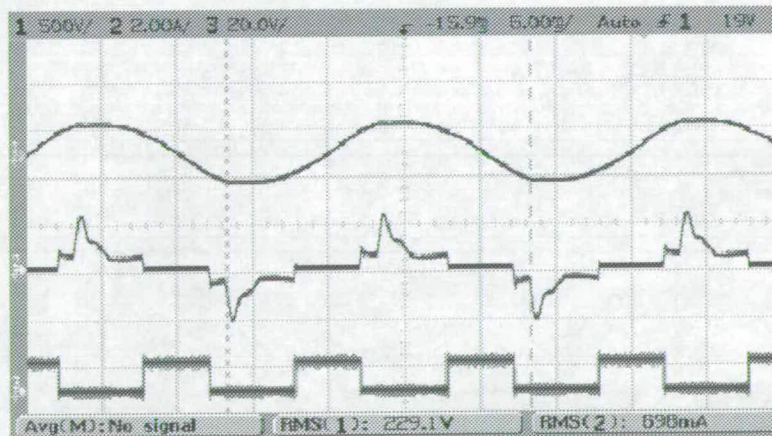
Figure 7.26: Input current without L_1 and a turn on/off voltage for S_2 of 230V. Top trace: input voltage. Middle trace: input current. bottom trace: output voltage from the comparator.

7.7.3 Efficiency and Bulk Capacitor Voltage

The efficiency and bulk capacitor voltage were measured without the input current filter fitted and are displayed in table H.3 for a turn on/off voltage of 140V and table H.4 for a turn on/off voltage of 230V with L_1, both tables are in appendix H.

Figure 7.27 shows the efficiency across the output power range for $180V_{RMS}$ and $230V_{RMS}$ input voltage. The efficiency is good at around the high seventies and low eighties for a turn on/off voltage of S_2 of 140V without L_1. For a turn on/off voltage of S_2 of 230V with L_1 the efficiency is also good with similar values. With the addition of the input current filter the efficiency was observed to drop to about 76% at full output power of about 100W.
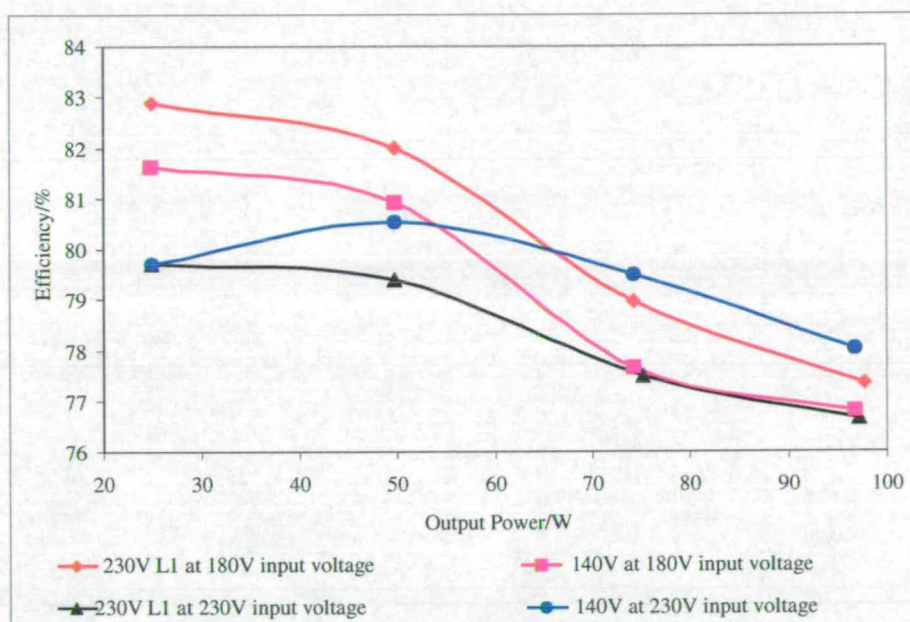
Figure 7.27: Efficiency across the power range without L_1 fitted and a turn on/off voltage for S_2 of 140V. Efficiency across the power range with L_1 as 20μH and a turn on/off voltage of 230V.

Figure 7.28 shows the bulk capacitor across the output power range for a $230V_{RMS}$ input voltage with an input voltage peak of 312V for a turn on/off voltage of 230V and with L_1 fitted. The bulk capacitor voltage rises from 320V at about 25W output power to 325V at full load. As the input voltage is not sinusoidal the result cannot be compared easily with Mathcad predictions. For a turn on/off voltage of 140V without L_1 fitted, the average bulk capacitor voltage stays constant at 306V across the power range, with a peak input voltage of 313V for a RMS input voltage of 230V.
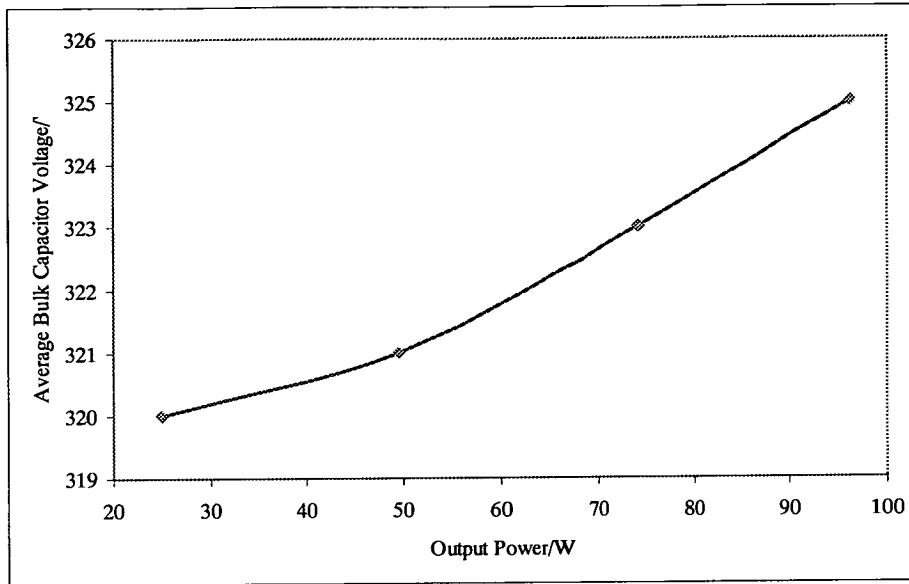
Figure 7.28: Voltage across the bulk capacitor over the output power range with a peak input voltage of 312V for a turn on/off voltage of 230V and L_1 at $20\mu H$

7.7.4 Semiconductor Voltage Stress

Table 7.3 shows the voltage stress on the semiconductors, measured without the input filter and with the peak of input the voltage at 306V or 313V. The values are lower than predicted due to non-ideal input voltage waveform with a depressed peak voltage. Simulation and analysis values are for a peak voltage of 375V. Recalculation with a non-ideal input voltage predicts that S_1 has a voltage of 612V.

Device	Voltage/V Basic	Voltage/V with L_1
S_1	625	656
S_2	140	362
D_1	175	325
D_2	39.1	28.1
D_3	32.8	35.9

Table 7.3: Voltages measured across key semiconductors with a peak input voltage of 306V for the basic LFSPFC converter without L_1 and 313V for the LF-SPFC converter with L_1.

	Basic LFSPFC		LFSPFC with L_1	
Output	100kHz Voltage p-p Ripple/mV	100Hz Voltage p-p Ripple/mV	100kHz Voltage p-p Ripple/mV	100Hz Voltage p-p Voltage/mV
Input Voltage: 230V				
5.13V 10A	78	484	75	250
5.1V 19.6A	94	484	65.6	281
Input Voltage: 200V				
5.13V 10A	94	406	68.8	168
5.1V 19.4A	94	391	93.8	187
Input Voltage: 180V				
5.15V 10A	94	359	75	100
5V 19.6A	78	344	87.5	112

Table 7.4: Ripple on the output voltage at 100kHz and 100Hz

7.7.5 Output Voltage Ripple

Table 7.4 shows the measured voltage ripple on the output voltage. For the LFSPFC converter without L_1 the 100kHz ripple maximum was 94mV. This ripple is mainly determined by the ESR of capacitor C_1. The 100Hz ripple on the output voltage ranges from 359mV to 484mV. This ripple is caused by the switching on and off of switch S_2. The switching of S_2 causes a step-change in input voltage being applied at the transformer (either a change from instantaneous line voltage to bulk capacitor voltage or vice-versa). As there is a step input in the voltage the control circuit has to deal with the disturbance. Voltage mode control is used, and as the voltage feedback loop is slightly over-damped this exaggerates the effect of the disturbance seen on the output voltage. The use of a control strategy such as peak current mode would be more appropriate as this can respond to an input voltage disturbance in one switching cycle. The same comments apply for the version with L_1, but the 100Hz ripple is lower in this version at a maximum of 281mV. This is because the switch S_2 is turned on/off at a higher voltage and hence the voltage change at the transformer when switching between line and bulk capacitor is smaller, producing a smaller disturbance. The values of ripple are a lot higher than that specified for a PC power supply (50mV on a 5V output), but this can be reduced by adding an additional stage of filtering on the output or by using current mode control to reduce the response time to the disturbances.

7.8 Conclusion

A new single-stage PFC converter using a low frequency switch has been introduced. The proposed converter can be built with or without a boost style input inductor depending on how low the input current harmonics need to be. The technique and operation has been explained. Analysis has been carried out on the duty cycle variation, input current wave shape and input current harmonics for the converter without an input inductor. In addition the behaviour of the bulk capacitor voltage has been explored for the version with an input inductor. The analysis has been carried out for operation in DCM and will need extending to CCM. Simulation has also been carried out as have some practical measurements.

A 100W prototype was built and tested with and without the input inductor. The converter with and without the input inductor will pass class A, but without the input inductor there is little chance of passing class D. The converter with the input inductor is close to passing class D. With the input inductor the voltage on the bulk capacitor behaves in a similar manner as predicted in the analysis. The efficiency of both versions was in the high seventies and component stress was reasonable.

From the analysis and testing so far it is desirable to have the turn on/off voltage of switch S_2 as high as possible. This will still meet the input current harmonic regulations, and reduces the disturbance when turning S_2 on/off, and when fitted with an input inductor keeps the bulk capacitor voltage low.

This converter could be a possible alternative to the use of passive filtering to meet IEC 61000 -3-2 as the semiconductor components suffer a similar voltage stress and the auxiliary switch arrangement will take less space and be lighter than a PFC choke.

Further testing with a more sinusoidal input supply is needed and investigation for operation of the input inductor operating in CCM is required.

Chapter 8

Comparison

8.1 Introduction

In the previous chapters three single-stage PFC topologies, the bi-forward, bi-forward with input inductor and the CS S^2PFC have been investigated. Also a new single stage PFC topology has been presented, the LFSPFC. The basic bi-forward was found to only meet the class A regulations, which lead to the study of the bi-forward with input inductor which met the class D regulations. The LFSPFC has only just been developed and further testing is necessary for this topology.

To determine if the bi-forward with input inductor or the CS S^2PFC are as attractive as described in the literature, in this chapter the pair will be compared with two current PFC solutions; a forward converter with a passive filter on the input shown in figure 2.7 and a boost pre-regulator cascaded with a forward converter shown in figure 2.9. This is to determine if the bi-forward or CS S^2PFC would be a suitable replacement for either the passive PFC or boost pre-regulator methods. The comparison will also show how well the two single-stage topologies generally perform in comparison to current methods of meeting IEC 61000-3-2. So far the results have only been shown separately and give no comparative indication as to how well the topologies performs. The specification used for all four converters is

- Operate from 90 - 130V$_{RMS}$ and 180 - 265V$_{RMS}$ at 47 - 63Hz

- Output power of 0 - 148W at 5V, 0 - 20A and 12V, 0 - 4A

- Meet IEC 61000-3-2 class D at 100V$_{RMS}$ and 230V$_{RMS}$ at 50Hz from 75W input power to full load

In addition to this the following is standardized between the four topologies:

Switching frequency	100kHz
Control method	voltage mode using the UC3524
5V Output filter	$L_{2:5V} = 15.4\mu H$, $C_{1:5V} = 1800\mu F$
12V Output filter	$L_{2:12V} = 64\mu H$, $C_{1:12V} = 470\mu F$
12V Diodes $D_{1:12V}$ and $D_{2:12V}$	BYT08P-400 400V 8A
Input Diode Bridge	GBU6J 600V 6A
Transformer	ETD44 using ferroxcube ferrite material 3C90
Core for $L_{2:5V}$ and $L_{2:12V}$	MMG Sailcrest G56VH

Also the same design of heat sink is used for the secondary side diodes in all the converters and the switch S_1.

This study has been carried out with the end application of a PC power supply in mind, which has to meet the class D regulation. Because of this the basic bi-forward converter is not considered as it does not meet class D at all. The LFSPFC with input inductor is considered where it is possible to make some form of comparison, as it is only a single 5V output 100W converter operating from 180V to 265V.

8.2 Passive Filter Inductor Cascaded with a Forward Converter

This was introduced in section 2.3.2.

The PFC inductor is made up of two 9mH windings on an EI42 iron laminated core and the two bulk capacitors are $330\mu F$ 250V components. The remaining aspects of the design are outlined below:

Switch S_1	2SK2611 900V 9A MOSFET
5V diodes $D_{1:5V}$ and $D_{2:5V}$	STPS20H100CT 100V 20A Schottky diodes
Transformer turns	$N_1 = N_3 = 44$turns; $N_{2:5v} = 5$turns; $N_{2:12V} = 11$turns
Diode D_3	BYD33U 1200V 1.26A

The converter passed the class D regulations at 75W and full load input power at both 100V

178

and 230V. Table H.5 in appendix H shows the measured input and output power, efficiency and bulk capacitor voltage for this converter.

8.3 Two Stage Active PFC using a Boost Pre-Regulator Cascaded with a Forward Converter

This was introduced in section 2.3.3. The boost converter operates with fixed frequency PWM at 100kHz and inductor L_1 operates in CCM. The boost converter was produced by following [7].

The forward converter part of the circuit is identical to the forward converter used with the passive filter inductor in section 8.2. The boost converter is constructed using the following components:

Switch S_2	STW20NB50 500V 20A
Diode D_4	STTH806TTI 600V 8A
Diode D_5	BYV28-600
Control IC	UC3854A
Boost Inductor L_1	1mH on a G56VH core
Bulk capacitor C_B	100μF 450V
Capacitor C_3	1μF

On top of this are the resistors and capacitors required around the control IC to make it function. Also required is some soft start and start up current limiting circuitry to ensure the converter does not destroy it self during starting.

The converter passed the class D regulations at 75W and full load input power at both 100V and 230V. Table H.6 in appendix H shows the measured input and output power, efficiency and bulk capacitor voltage for this converter.

8.4 Comparison

8.4.1 PFC Method

On top of a basic forward converter additional components have been added to carry out the input current shaping. The additional components are outlined in table 8.1.

Passive	2 x 9mH PFC inductance windings wound on EI42 iron laminated core
Boost	1mH boost inductor 500V 20A MOSFET 600V 8A diode Control IC and associated components
CS S^{2}PFC	2 x 100μH windings on the same core 2 x 43μH windings on a second core 2 x 11 turns extra on the transformer 4 x 1000V 8A diodes
Bi-forward	20μH inductor Centre tapped transformer primary winding 3 x 1000V 8A diodes
LFSPFC	20μH inductor 1 x 1000V 8A diode 1 x 600V IGBT Comparator and gate drive components

Table 8.1: Additional components added to a forward converter to achieve PFC

In the single-stage converters some parts of the forward part of the converter had to be altered; these are shown in table 8.2.

Converter	MOSFET	5V Diode
Passive	900V 9A	100V 20A Schottky
Boost	900V 9A	100V 20A Schottky
CS S^{2}PFC	1000V 12A and snubber	100V 20A Schottky
Bi-forward	1200V 10A and snubber	200V 20A fast recovery
LFSPFC	900V 9A* and snubber	100V 20A Schottky

Table 8.2: Components altered in the forward converter. * Only 100W converter.

The passive PFC method only requires the addition of one extra component, the PFC choke. A disadvantage is that the PFC choke is heavy and bulky, but no other modification is required.

The two stage approach using a boost converter certainly adds the most components to the basic forward converter, as a full extra converter is added. The advantages of this method are the very good input current waveform, and that the forward converter can be operated from a narrow voltage range. This method also allows each converter to be optimised to its task. Again the forward converter requires no modification.

The single stage converters offer a compromise between the passive and the two stage methods, as they do not have the large number of components of the two stage or the large and heavy PFC choke of the passive. The CS S^2PFC has two small inductor cores (with four inductors on them) and four diodes added and the bi-forward has one small inductor and three diodes added. The gain made in component number and weight is lost in component stress and cost as both converters require high voltage MOSFETS which are expensive; this is illustrated in section 8.4.7. The LFSPFC requires the addition of some simple and common components which do not significantly increase cost for a 100W converter. If power is increased then from figures 7.12, 7.13 and 7.14, a high voltage MOSFET like the bi-forward and CS S^2PFC will be required.

8.4.2 Measured Harmonic Content to Class D

Figures 8.1, 8.2, 8.3 and 8.4 show the harmonic content for the four topologies at 230V full load, 230V 75W input power, 100V full load and 100V 75W input power compared to the class D regulation values for that setting. Only harmonics up to the 19th are shown for clarity. All harmonics above the 19th pass with a large margin. The measured harmonics were measured at slightly different powers and have been adjusted to be at the same power. For the 75W readings all the measurements for the four converters were adjusted to 75W. At full load the values have been adjusted to the input power of the passive converter.

At full load at both 100V and 230V all four topologies met the class D regulations. At 75W input power the passive, two stage and bi-forward converters met the class D regulations at both 100V and 230V. The CS S^2PFC failed the 75W harmonic tests at both 100V on the 7th and 9th harmonics and 230V from the 5th to the 13th harmonics. It started to pass the regulations at about 100W input power. All the results for the two stage method show very low harmonic content well below the class D limits (they can hardly be seen in figures 8.1, 8.2, 8.3 and 8.4). The harmonic levels for the passive solution are sitting just below the class

D limits in particular for the 3rd and 5th harmonic. The bi-forward converter has harmonic levels that are lower than the passive, but still much higher than the two stage approach. At full load the harmonic levels for the CS S^{2}PFC are between the levels for the bi-forward converter and the passive PFC and forward converter. The LFSPFC converter with input inductor at 127W input power exceeded the class D harmonic levels for the 13th and 23rd harmonics, but passes class A.

The passive, bi-forward, and CS S^{2}PFC all have measured harmonics which are close to the class D limits. This may cause problems if the regulations are tightened.
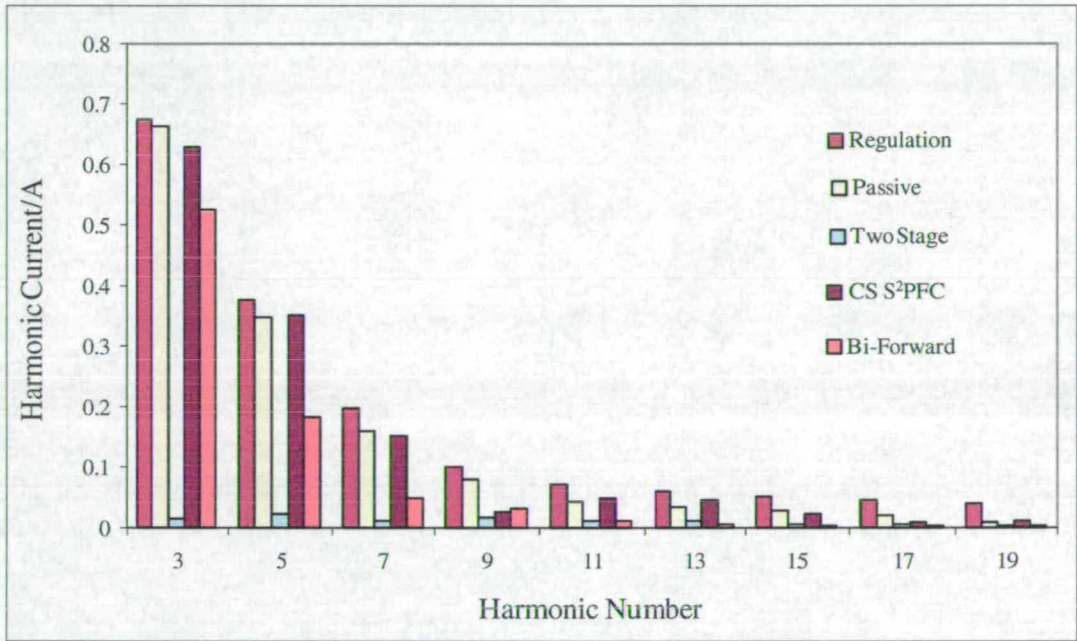
Figure 8.1: Harmonic content at full load input power (about 198W) at 230V compared to class D

8.4.3   Input Current Waveform

Figures 8.5A, 8.5B, 8.5C and 8.5D show the input current waveforms at 230V and full power. As can be seen the current waveform does not have to look particularly sinusoidal to pass the class D regulation. The two stage with the boost pre-regulator has the best current shape, shown in figure 8.5B, and is virtually sinusoidal. The passive method in figure 8.5A has quite a narrow conduction angle and is suffering from a sub-harmonic oscillation. Even when suffering from this oscillation the converter still passes class D and they are
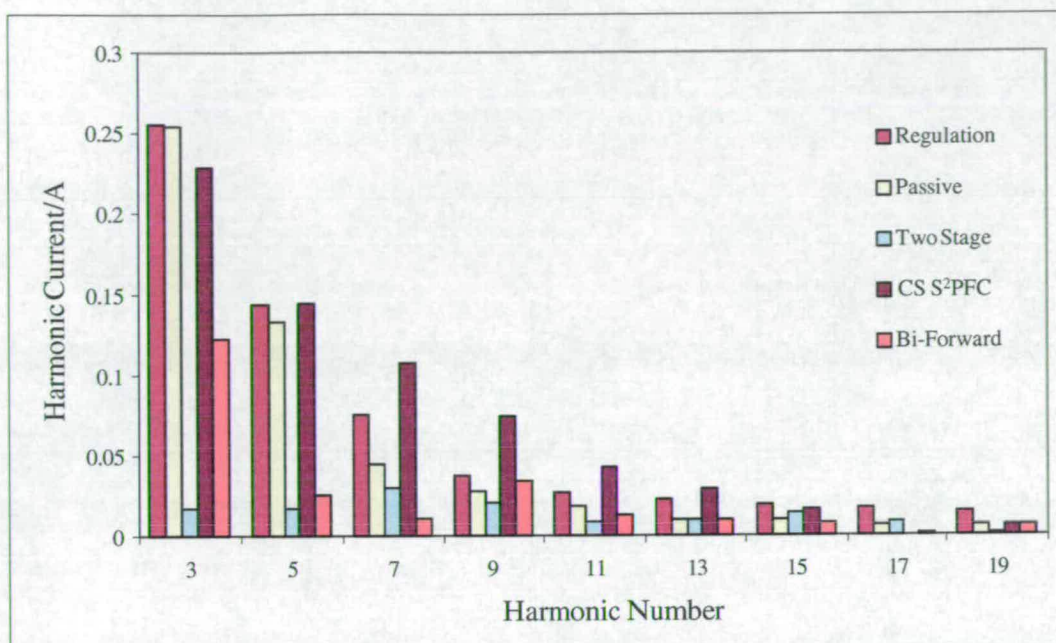
Figure 8.2: Harmonic content at 75W input power at 230V compared to class D
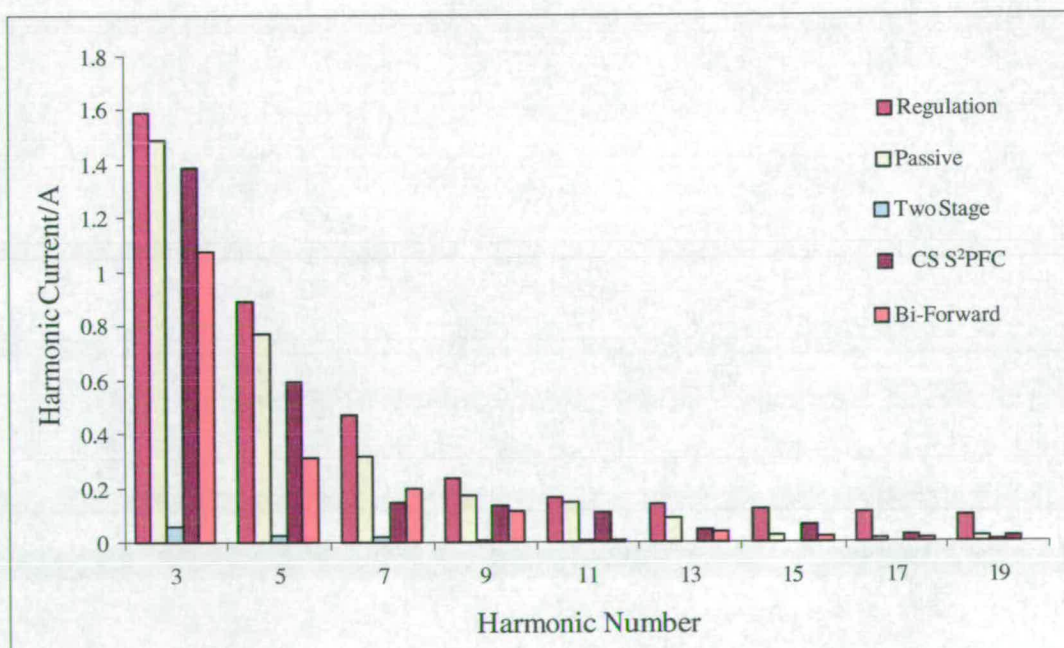
Figure 8.3: Harmonic content at full load input power (about 203W) at 100V compared to class D
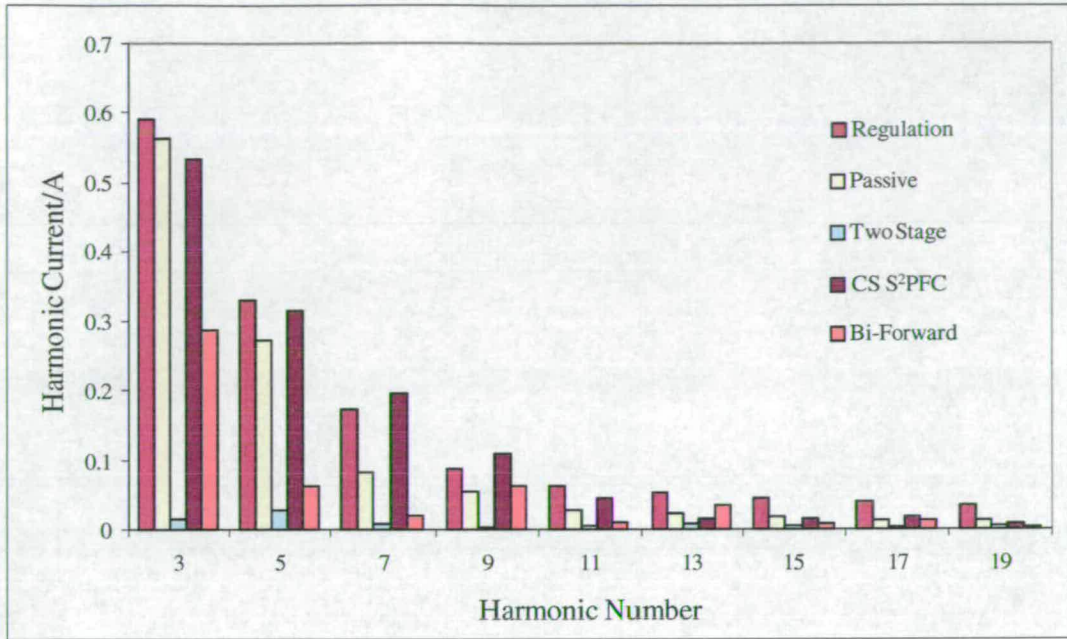
Figure 8.4: Harmonic content at 75W input power (about 198W) at 230V compared to class D

sold exhibiting this behaviour. The CS S^2PFC current waveform shown in figure 8.5C also has a narrow conduction angle, but does have a slight similarity in basic wave shape with the passive in figure 8.5A. It is possible to see the DCM part of the waveform at the beginning and end of the current waveform. The bi-forward converter input current waveform shown in figure 8.5D has a wider conduction angle and is somewhere between the passive waveform and the two stage waveform. The waveform has a slight triangular shape. Figure 7.25 shows the input current of the LFSPFC converter and the waveform is quite different to that of the CS S^2PFC and bi-forward with sharp rises in current at the start and end of conduction. Other than that the shape has the same rise to a peak in a rounded triangular type shape.

8.4.4 Efficiency

Figures 8.6 and 8.7 shows the measured efficiency across a wide output power range from about 37W to 150W output power at 230V and 115V. The passive filter PFC and forward converter exhibited the highest efficiency of around 80%. The CS S^2PFC and the two stage are both showing efficencies of around 75%. This confirms the result in [124]. The bi-
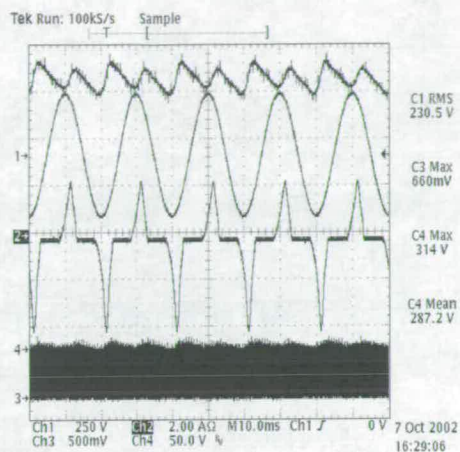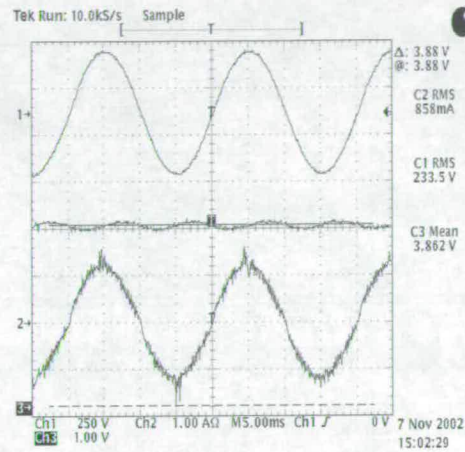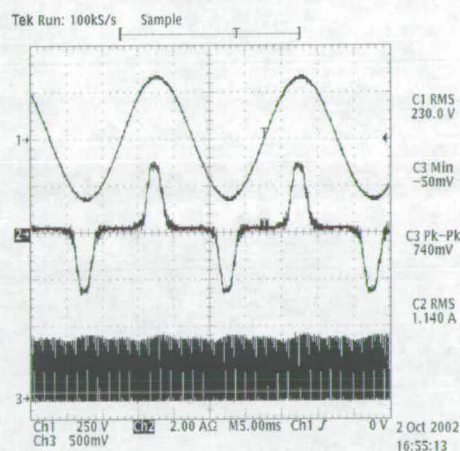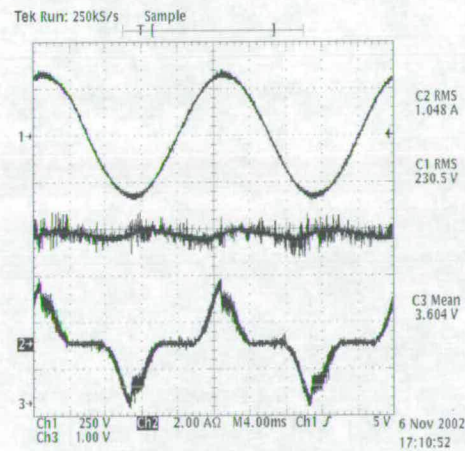
Figure 8.5: A) Measured full load bulk capacitor voltage top trace, input voltage (2nd from top), input current (3rd from top) and voltage drain source of the MOSFET (bottom) at 230V input for the passive filter circuit. B) Measured full load input voltage (top), input current (bottom) and bulk capacitor voltage (middle) at 230V input for the two stage circuit. C) Measured full load input voltage (top), input current (middle) and gate drive signal (bottom) at 230V input for CS S^2PFC circuit. D) Measured full load input voltage (top), input current (bottom) and bulk capacitor voltage (middle) at 230V input for the bi-forward circuit.

forward converter is showing an efficiency of about 70%. The reason for the lower efficiency is the use of standard fast recovery diodes on the 5V output instead of Schottky diodes used in the three other converters. Normal diodes have to be used in the bi-forward as the voltage seen across them is higher due to the centre tapped primary winding on the transformer and the high bulk capacitor voltage. If Schottky diodes could be used in a future design of the bi-forward converter then the efficiency would be more comparable with the CS S^{2}PFC and two stage approaches. It should be noted that the two single-stage topologies are fitted with RCD snubbers to reduce MOSFET turn off losses.

Table 8.3 compares the efficiency of the LFSPFC at 100W with the other converters. The single output LFSPFC converter at 100W output power has an efficiency of about 77%. This makes it comparable to the CS S^{2}PFC and two stage method at that power. Ranking them by efficiency the passive leads, followed by the CS S^{2}PFC (and LFSPFC) then the two stage and finally the bi-forward.

The efficiency of all four converters is highest at about 75W. This is due to some aspects of their design coming from production PC power supplies which are rated at 150W or more, but operate most of the time at between 60W and 70W, so the converters are designed to be most efficient at that output power.
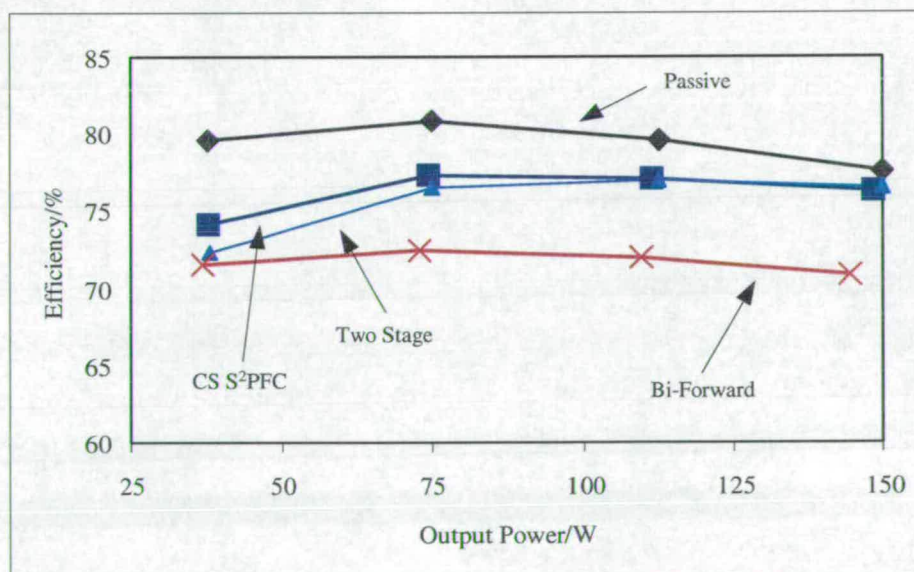
Figure 8.6: Measured efficiency with input voltage as 230V
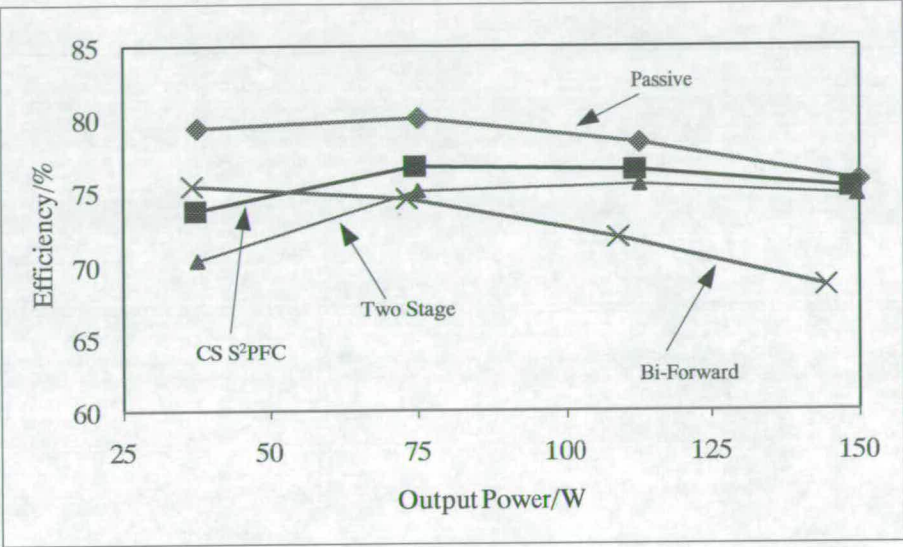
Figure 8.7: Measured efficiency with input voltage as 115V

Topology	Efficiency/%
LFSPFC	77
Passive	80
Two Stage	77
CS S^{2}PFC	77
Bi-forward	72

Table 8.3: Measured efficiency at 100W compared to measured efficiency of the LF-SPFC

8.4.5 Voltage Across the Bulk Capacitor

Figure 8.8 shows the measured variation of bulk capacitor voltage with power at 265V input voltage. The two stage method has a bulk capacitor voltage which is virtually constant, only varying across a 10V range from 395 to 385V as the throughput power goes up. The passive and forward converter has the lowest bulk capacitor voltage from 366V at almost no output to 355V at 150W output power. The voltage across the CS S^2PFC falls from 408V at almost no load to 376V at 149W output power. The bi-forward has the highest bulk capacitor voltage at 430V. The voltage across the bulk capacitors in the bi-forward varies between 386V and 430V. The results for the LFSPFC do not allow comparison [1], but the analysis predicts the voltage to rise from 375V to 392V at 133W. Table 8.4 shows the bulk capacitor voltage at about 112W for the measured circuits at 265V compared to expected bulk capacitor voltage for the LFSPFC.

The reasons for the variation of bulk capacitor voltage for the CS S^2PFC and the bi-forward with input inductor have been explained in their respective chapters. The voltage across the bulk capacitors in the passive converter is set by a combination of the load and the resonant circuit conditions between L_1 and C_{B1} and C_{B2}. The voltage on C_B in the boost pre-regulator is reasonably well regulated.

Topology	Bulk Capacitor Voltage/V at 112W Output	Bulk Capacitor Voltage/V at 37W Output
LFSPFC	392	378
Passive	389	355
Two Stage	389	394
CS S^2PFC	383	400
Bi-forward	430	386

Table 8.4: Measured bulk capacitor voltage compared to predicted bulk capacitor voltage for LFSPFC at 265V input

Figure 8.9 shows the bulk capacitor voltages at the other end of the input voltage range at 90V. This figure shows that the voltage across the bulk capacitor in the two stage is the same at 90V as it is at 265V at just below 400V. The bi-forward has the lowest bulk capacitor voltage at just above the peak of the input voltage (the peak of the input voltage is 127V). This is because the bi-forward has the widest bulk capacitor voltage range as it

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[1] the equipment used would not supply voltage up to 265V and as the input voltage peak was flattened
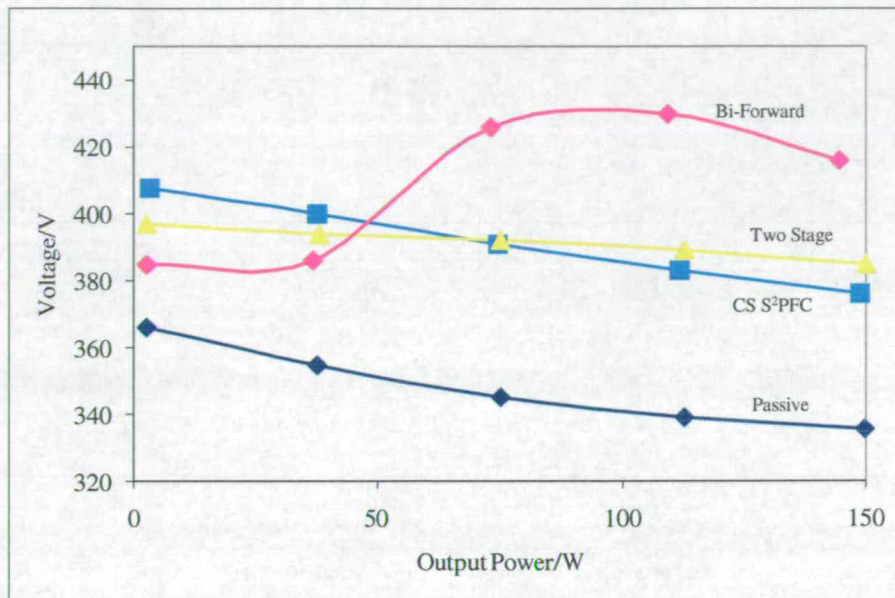
Figure 8.8: Measured bulk capacitor voltage with input voltage as 265V

does not have any method of raising the capacitor voltage at low input voltage. The passive and CS S^{2}PFC both have similar voltages of about 250V across the bulk capacitor, though the CS S^{2}PFC is slightly higher due to the boost nature of L_1. These two converters are both operating in voltage doubler mode. The LFSPFC was not designed to work on the low voltage range.

8.4.6 Voltage Measured Across Components

Table 8.5 compares the voltage stress across some of the forward converter components at 265V input voltage. The voltage across switch S_1 is not as high as expected (1200V) in the bi-forward converter due to the MOSFET snubber resetting the transformer core at 830V. This makes the voltage across S_1 105V higher than that in the passive and forward converter method. If the snubber was designed for resetting the core it could be used to reduce the voltage of the bi-forward and CS S^{2}PFC to a similar level as observed on the switch S_1 in either the passive or two stage methods. The voltage across the secondary diodes on the 5V and 12V output in the CS S^{2}PFC are both very low compared to the other converters: this is due to the lower turns ratios used. Schottky diodes could be used on both outputs, but have only been used on the 5V output. The passive and the two stage methods produce higher voltages across both sets of diodes, requiring normal fast recovery diodes to be used on the

189
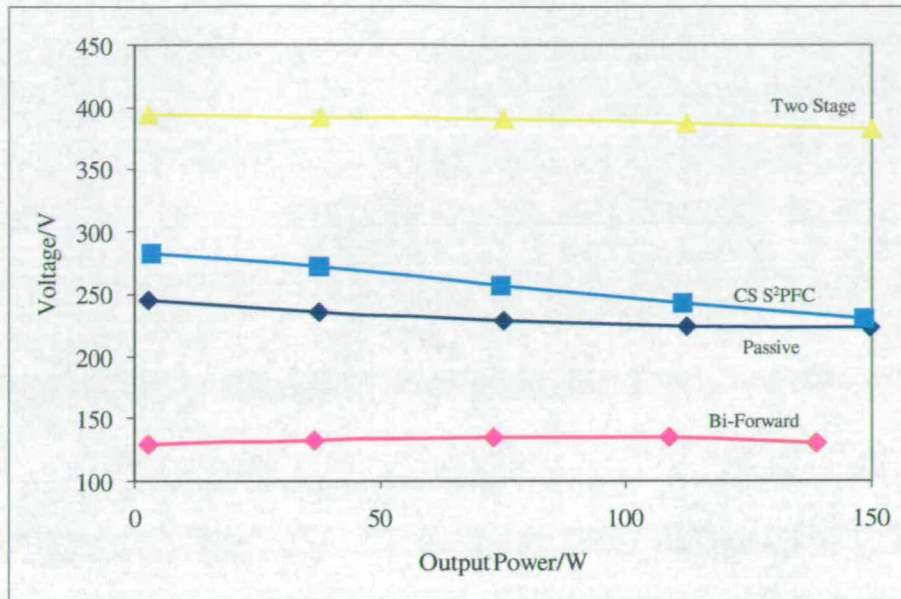
Figure 8.9: Measured bulk capacitor voltage with input voltage as 90V

12V output. The bi-forward has the highest voltage across both the 5V and 12V diodes. At 89V, across one of the 5V diodes, this requires that ordinary fast recovery diodes have to be used for the 5V output. This value is almost five times that across the same diode in the CS S^{2}PFC and twice that in the passive and two stage. The same is seen for the 12V output diodes.

Device	Passive	Boost	CS S^{2}PFC	Bi-forward
Switch S_1	725	800	850	830
5V diodes	37.8	31.3	25	89
12V diodes	84.4	107	57	222

Table 8.5: Voltages measured across S_1, 5V diodes and 12V diodes at 265V input voltage

8.4.7 Cost

Table 8.6 shows the normalised cost of the converters with the passive PFC and forward converter as the base value of one.

The passive PFC method was found to be the cheapest, with the boost converter second even with all the additional components. The two single-stage topologies were the most ex-

Converter	Cost	Single-Stage Cost with 900V MOSFET
Passive	1	1
Boost	1.39	1.39
CS S^{2}PFC	1:46	1.14
Bi-Forward	1.455	1.03

Table 8.6: Costs of the converters compared to the passive filtering with forward converter

pensive with the CS S^{2}PFC being marginly more expensive. The reason for the bi-forward and the CS S^{2}PFC being the most expensive was the cost of the 1000V or 1200V MOSFET. The cost of a 1000V MOSFET compared to a 900V MOSFET is considerably greater even though the voltage difference between them is only 100V. Using an RCD snubber instead of the tertiary winding to reset the transformer will lower the reset voltage of the transformer to a level low enough to allow the use of a 900V MOSFET in the bi-forward or CS ^{2}PFC making their cost more comparable to the passive with forward converter method, this is illustrated in the final column of table 8.6.

8.4.8   Hold Up Time

Table 8.7 shows the hold up times at 115V and 230V. For the two stage and passive models the hold up time at 115V and 230V are similar. This is because the voltage across the bulk capacitors is similar at 115V and 230V: in the two stage the boost converter is controlled to give an output voltage of 400V from both input voltages, and a voltage doubler is used in the passive PFC. The two stage has the second longest hold up time at 39ms as the bulk capacitor is charged to 400V and the forward converter will not lose regulation until the bulk capacitor voltage reaches 100V. The passive is only falling from 287V at 230V and 291V at 115V, but the capacitance is 65μF higher. The CS S^{2}PFC has hold up times similar to that of the passive with forward converter (at 115V it is lower and at 230V it is higher). At 115V the voltage across the bulk capacitors is 309V and 230V it is 326V, but the converter loses output voltage regulation at a bulk capacitor voltage of 163V due to the lower number of secondary turns. The passive, two stage and CS S^{2}PFC all have hold up times at both input voltages above that typically set for a PC power supply of 10ms. At 115V the bi-forward converter has a hold up time of only 8.6ms: this converter does not have a voltage doubler arrangement and the bulk capacitor voltage only has to fall from 176V to 100V

before regulation is lost. At 230V the bi-forward has the longest hold up time of 48ms; this is a fall of bulk capacitor voltage from 360V to 100V, but the capacitance is $65\mu F$ higher than that in the two stage.

Converter	Hold Up Time at 115V /ms	Hold Up Time at 230V /ms
Passive	23.8	25.2
Two stage	38	39.2
CS S^{2}PFC	18.4	27.6
Bi-Forward	8.6	48.6

Table 8.7: Hold up time of the converters at 115V and 230V input voltage at 150W output power

8.4.9 Output Voltage Ripple

Table 8.8 compares the ripple on the output voltages of the four converters. The passive and two stage have hardly any 100Hz ripple appearing on the output voltages. This is due to the PFC stage of the converter being separated from the part of the converter that controls the output voltage. On the bi-forward the maximum 100Hz ripple on the 5V output is 50mV and 115mV on the 12V output, and for the CS S^{2}PFC it is 40mV on the 5V output and 131mV on the 12V output. The LFSPFC has 281mV of ripple on its output. This is not as bad as it seems as typically a PC power supply is allowed ripple within 1% of the 5V and 12V output, which these figures meet except for the LFSPFC. 100Hz ripple appears on the output voltages as the output voltage controlling part of the circuit is also shaping the input current (they are only controlled to keep output voltage constant). In the bi-forward the ripple appears due to the step change in transformer turns transferring energy to the output. A similar reason causes the same to happen with the LFSPFC where the duty ratio will suddenly change when switch S_2 turns on/off. In the CS S^{2}PFC the ripple appears as there is PFC stage current flowing in the transformer while it is supplying the output.

Additional output filtering or post regulation would remove the 100Hz ripple. The voltage ripple seen on the output voltage is produced from two sources; the voltage on the output capacitor changing as it charges or discharges, and from the current to and from the capacitor flowing through the capacitor equivalent series resistance (ESR). The voltage across the ESR is the main contributer to voltage ripple and this is linked to the inductor ripple current.

192

At 100kHz the two stage has a ripple over a small range, from 28.1mV to 39.3mV on the 5V and on the 12V from 90.6mV to 125mV. This small range is to be expected as the voltage on the bulk capacitor is regulated and so a fairly constant voltage is seen across the secondary inductors $L_{2:5V}$ and $L_{2:12V}$ between each switching cycle. The passive ranges from 42.5mV to 76.6mV on the 5V and on the 12V from 103mV to 137mV at 100kHz. The CS S^{2}PFC ranges from 15.6mV to 20.3mV on the 5V output and on the 12V output from 81.3mV to 125mV. The ripple on the CS S^{2}PFC is lower than the other converters due to the lower turns ratios on the transformer which produce a lower voltage on the secondary windings and makes the duty cycle longer. The bi-forward 100kHz ripple ranges from 45mV to 90mV on the 5V output, a similar value appears on the LFSPFC converter, and from 90.6mV to 165mV on the 12V output. The bi-forward converter operates over a wide voltage range and with two different sets of transformer turns ratios, so a wide range is not unexpected, but it is not much wider than the passive circuit.

The 100kHz ripple can be improved by additional filtering or post regulation. Care would have to be taken when changing the inductance of L_2, as in the bi-forward and LFSPFC this forms part of the PFC action of the circuit and will modify the current shaping behaviour and the voltage across the bulk capacitors, as it would in the CS S^{2}PFC as L_2 sets where the output goes into DCM.

Converter	5V 100kHz p-p Ripple/mV	5V 100Hz p-p Ripple/mV	12V 100kHz p-p Ripple/mV	12V 100Hz p-p Ripple/mV
Passive	76.6	0	137	0
Two stage	39.3	3.13	125	7.8
CS S^{2}PFC	20.3	40.6	181	131
Bi-Forward	90	50	165	115
LFSPFC	93.8	281	–	–

Table 8.8: Maximum Output Voltage Ripple, not considering the bi-forward at 90V input voltage and full load

8.5 Discussion

The bi-forward with or without input inductor and the CS S^{2}PFC both exhibited that what was gained in losing a stage was lost elsewhere in the converter, and some of this is reflected in the performance of the converter. The loss from going to a single-stage in all topologies

was an increase in voltage stress. Single-stage converters such as the CS S^2PFC and bi-forward with input inductor converters both suffered from high bulk capacitor voltage in excess of 400V when operating from 265V input voltage, and this appears in all single stage topologies (including the LFSPFC) with a boost converter style inductor on the input when operating with the output inductor in CCM. This occurs as it is the only way the converter can balance input and output power. This high voltage requires the use of a MOSFET capable of withstanding 1000V or more as the power switch (tertiary reset forward); these are very expensive, losing the assumed cost saving of the converter when compared to either two stage approach. The problem of a high voltage MOSFET can be removed, but with an increase of components by using a two switch forward converter or snubber transformer reset (more common now). Another method is to try changing the PFC part of the converter so that it keeps the bulk capacitor voltage lower.

One thing that may make the bi-forward and the CS S^2PFC more desirable is the fall in cost of high voltage MOSFETS. For the bi-forward, the development of higher voltage Schottky diodes would help with the bi-forward's lower efficiency. At the moment the passive filtering or boost pre-regulator and ordinary forward converter are conventional. Due to this the components they are constructed from are popular and used in high quantities, which makes them cheap and more likely to have been subject to development to reduce factors such as R_{dson} in 900V MOSFETs. On the other hand 1000V and 1200V MOSFETS are not used in high quantities, and as such they have had less development and are more expensive.

The present single-stage topologies are at the moment unlikely to be viable as a PC power supply. The main reason from the view of a manufacturer is that they are too expensive. From a more engineering point of view the bi-forward and CS S^2PFC present little benefit over the two current methods studied. They suffer from high voltage stress on the switch S_1 and the bulk capacitor. They do not reduce the amount of space a converter needs when compared to the passive filtering method, and will require additional filtering to remove switching frequency currents on the input. A clear reason that the CS S^2PFC is unlikely to be used is that it does not meet the class D regulations at the lower end of the power range. Also 100Hz ripple is appearing on the output voltages, which does not occur with either two-stage circuit. The efficiency of all the four topologies studied was at an acceptable level for a PC power supply.

In [94] the flyback version of the basic bi-forward converter is presented as being a possible

converter in a low power AC/DC adapter with the benefit of reduced bulk capacitance. There is a possibility that there could be some advantage in using either the CS S^2PFC or the bi-forward with input inductor converters in particular applications where only class A has to be met (almost anything else apart from PCs) and where the output power does not vary over a wide range. The bi-forward in the form investigated is more suitable for use on a single input voltage range. For the bi-forward an input inductor is required even to meet class A once output power is above 100W. The basic version has difficultly meeting class A at higher power. To meet class A the bi-forward's transformer turns ratios can be made so as to reduce the voltage seen across the switch S_1 (if L_1 is fitted also reduce the voltage across the bulk capacitors).

The bi-forward converter with input inductor is more suitable for low power of around 100W or less, as the converter is more likely to operate in the intended manner. At low power the bulk capacitor voltage is lower for a particular input voltage and the efficiency is slightly better.

The CS S^2PFC converter, on the other hand, is likely to be more suitable for medium powers of around 200W. At this level it should have no problem meeting class D if needed and the bulk capacitor voltage should be close to the peak of the mains.

The LFSPFC converter has been briefly compared with the other topologies where it is possible as the converter was only designed to operate at 100W on a 5V output from the high volage range, but also due to the poor quality voltage supply available in the laboratory. It has been found to have reasonable bulk capacitor voltage (predicted) up to 133W when compared to the bi-forward and CS S^2PFC converters. It is expected that the if throughput power is increased then the bulk capacitor voltage will rise to a higher value. Hence it is expected that a high voltage MOSFET similar in rating to that used in the bi-forward and CS S^2PFC converters is required for a 150W output. The efficiency was comparable with the two stage method and CS S^2PFC converter. Cost has not been investigated, but with a 100W output it will be close to the passive method as the additional components are cheap. It is felt that this converter is most suited to lower powers of about 100W where voltage level is not a problem, and could with some work be a lighter, less bulky replacement for the passive method at those lower powers and with comparable cost.

8.6 Conclusion

Table 8.9 summarises the vices and virtues of the various topologies [2]. It would seem that the passive and forward combination has the best efficiency, lowest cost and is able to meet the class D regulations at 150W output.

Characteristic	Topology			
	Passive	Two Stage	CS S^2PFC	Bi-Forward
Additional Components	1	9+	8	5
Regulations	Pass	Pass	Fails 75W	Pass
Average Efficiency at 230V/%	79.4	75.6	76.2	71.7
Average Efficiency at 115V/%	78.3	73.9	75.5	72.6
Cost	1	1.39	1.46	1.455
Highest Voltage on C_B/V	366	397	408	430
Shortest Hold Up Time/ms	23.8	38	18.4	8.6
Highest 5V Output Voltage Ripple at 100kHz/mV	76.6	39.3	20.3	90
Highest 5V Output Voltage Ripple at 100Hz/mV	0	3.13	40.6	50

Table 8.9: Summary of topology performance

If an RCD transformer reset was to be used with the bi-forward converter and on the CS S^2PFC this would reduce the voltage seen across switch S_1 during transformer reset, allowing the use of a cheaper device and making the converters more comparable on cost to the passive and forward converter. Re-design may also bring the bulk capacitor voltage down to a lower level, ideally 400V or less, and in the bi-forward allow the use of Schottky diodes on the 5V output. This would increase the efficiency of the bi-forward to be more comparable to the other three converters.

It is believed that the CS SS^2PFC converter is more suited to applications where meeting the class D regulation is only required at a single power and that the bi-forward is more suited to low power applications.

The LFSPFC had the highest ripple, but did have reasonable efficiency and bulk capacitor voltage for a 100W output converter. It is felt that 100W is about the maximum power output that this converter can work up to. It could, with some more work, be a possible lighter weight replacement for the passive method in some applications.

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[2] except the LFSPFC as the results for this converter are limited due to using different test equipment

Overall the passive filtering and forward converter solution would still seem the most attractive choice of converter to use.

Chapter 9

Conclusions and Further Work

In addition to the conclusions drawn at the end of the preceeding chapters the following final conclusions can be drawn.

9.1   Final Conclusions

The project has shown that the bi-forward with input inductor and the CS S^2PFC converters are not suitable replacements for passive filtering or a boost converter cascaded with a forward converter for a 150W output power supply operating on an universal input voltage and able to meet IEC 61000-3-2 class D. It was found that the passive, boost pre-regulator and bi-forward methods met IEC 61000-3-2 class D at 100V and 230V from 75W input power to full load power, but the CS S^2PFC would not pass at input powers lower than about 100W. The test results showed that both converters suffered from high voltage on the bulk capacitor which had knock-on effects when compared to the passive and two stage methods. The high bulk capacitor voltage (and the centre tap primary on the bi-forward) required the bi-forward and CS S^2PFC converters to have MOSFETs rated for 1000V and above, which made their costs much higher than either the passive method or boost pre-regulator. The high voltage due to the the centre-tapped primary in the bi-forward converter made it the least efficient converter as it required normal fast recovery diodes on the 5V output and not Schottky diodes as in the other converters, but the CS S^2PFC had an efficiency comparable to the boost pre-regulator method. Both the bi-forward with input inductor and CS S^2PFC had noticeable 100Hz ripple on the output voltage since a large mains frequency component

is seen in the main converter. The only immediate benefit of using the bi-forward with input inductor or the CS S^2PFC converters is a saving in space or weight. It was found that the passive filtering with forward converter method was the cheapest, most efficient, had output voltages with minimal 100Hz ripple and met class D at both 100V and 230V from 75W input power to full load at 150W output power. If the regulations were to be tightened up then the all the converters studied except the boost pre-regulator could have problems meeting the improved regulations.

The basic bi-forward converter as described in the literature is only able to meet class A, but a MOSFET rated up to 1200V may be needed due to increased voltage seen across the transformer primary side during core reset. It was found that cost could be reduced if snubber transformer resetting circuits were used allowing a lower voltage MOSFET. This topology is suitable for low power (100W or less) operating from just one voltage range (230V or 115V).

For bi-forward converter with input inductor the performance was quite different to that presented in [95]. It was difficult to produce a converter that operated with the input inductor in CCM, but the converter could pass class D with the input inductor operating in DCM. It was found the converter could operate in five different ways depending on the value of input inductance and output power. The way the converter operated also determined how the bulk capacitor voltage varied with power. The peak bulk capacitor voltage was found to be 430V which was the highest recorded. It was found that a snubber to reset the transformer was essential as otherwise the voltage would exceed the rating of a 1200V MOSFET. This topology is probably suitable for low power (100W or less) operating from just one voltage range (230V or 115V) for an application that has to meet class D.

The CS S^2PFC converter performed fairly well, in line with what was reported in [122]. It was found that the converter can meet class D at full load when bulk capcitor voltage is below the peak of the line and some of the current shaping action is lost. This converter is suitable for applications where compliance with class D is not required across a wide power range. Its cost could be reduced if snubber transformer resetting circuits were used allowing a lower voltage MOSFET.

In chapter 7 a new topology, the LFSPFC converter was introduced. This converter has a low frequency switch in series with the bulk capacitor of a forward converter controlled by a comparator looking at the rectified input voltage of the converter. This converter can

be built with or without an input inductor. The 100W converter built operates as expected with and without input inductor, proving the concept to work. With or without an input inductor the converter passes class A with ease and has reasonable efficiency of about 77%. Without a low value input inductor, the converter fails class D on many harmonics, but with the inductor in it only fails on two harmonics, the 13th and 23rd. Using an input inductor analysis showed that the bulk capacitor voltage should stay below 400V with careful design. With the input inductor the bulk capacitor voltage is higher when the low frequency switch is turned on at lower voltages for a given power, and that the voltage rises with power. Extrapolating the plots of bulk capacitor voltage against power it is likely that at 150W output power the bulk capacitor voltage will be high as in the bi-forward with input inductor or CS S^2PFC converters requiring an expensive high voltage MOSFET, hence this converter should only be used up to about 100W. This converter could be a possible lighter and less bulky replacement for the passive method at about 100W output power.

9.2 Further Work

To further this study there are several areas which should be explored. The first would be further investigation into filtering the input current so as to remove the switching components of the current waveform. Along with this the EMI filtering requirements for a single-stage converter, such as the ones studied, should be considered along with the input current filtering as the two may be combinable.

Other areas of investigation for the bi-forward converters and CS S^2PFC converters would be

1. The use of a snubber for transformer reset.

2. Operation and design of the converters with different transformer turns ratio, output filters and input inductances.

3. Circuit optimisation could also be carried out.

Another area which needs further work (this applies to the LFSFPFC as well) is the use of more advanced control methods such as current mode control.

The LFSFPFC converter needs to be studied with operation of the input inductor in CCM. Also further work will be required to enable the converter to comply with the class D limits. Expansion to other converter types could also be tried.

In the analysis, further work should be done to investigate the effects of the charging and discharging of the bulk capacitor and its effect on the input current shape and harmonics. Prediction of losses and converter efficiency is another area of interest and will highlight areas where the most losses occur.

Appendix A

Predicted Harmonic Content at 100V for the Bi-Forward Converter

Shown in figures A.1 and A.2 are the harmonic plots at 100V and 200W input power for the bi-forward converter for class D and A respectively.
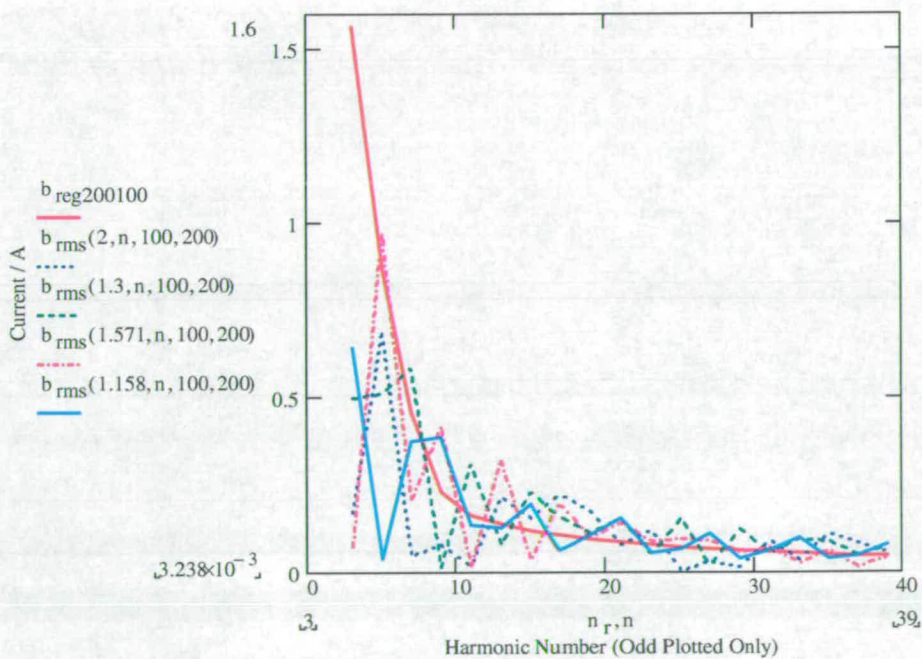
Figure A.1: RMS input current compared to class D (trace $b_{reg200100}$) for 100V input with an input power of 200W with n as 2, 1.3, 1.57 and 1.16. Traces are listed by side of graph, 1st value is n, 2nd value is the input voltage and 3rd value is the power.
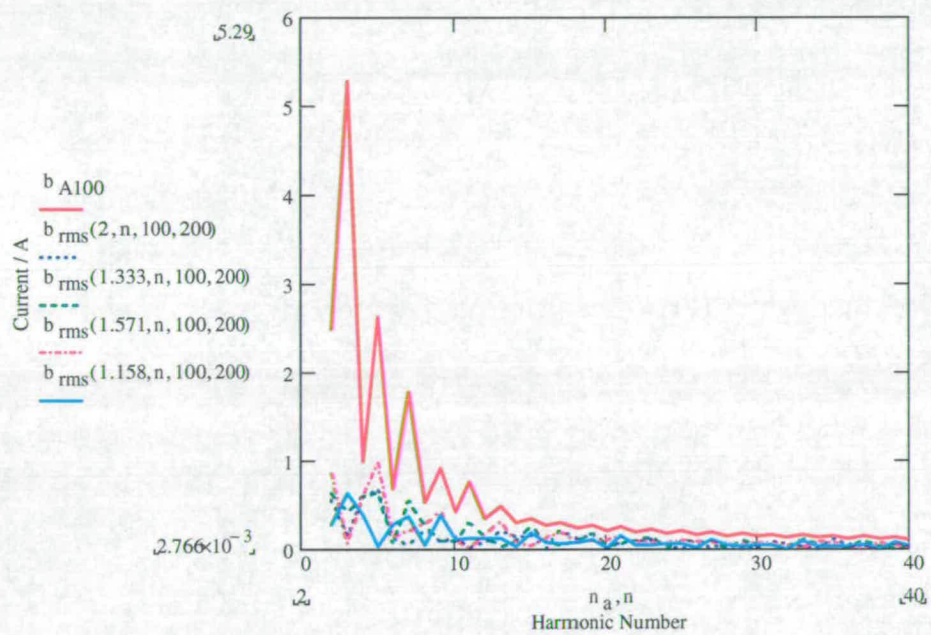
Figure A.2: RMS input current harmonics compared to class A (curve b_{A100}) for 100V input with an input power of 200W with n as 2, 1.3, 1.57 and 1.16. Traces are listed by side of graph, 1st value is n, 2nd value is the input voltage and 3rd value is the power.

Appendix B

Effect of Bulk Capacitance Value on the Bi-Forward

To demonstrate the effect that the value of C_B has on the harmonics shown in figures B.1, B.2, B.3 and B.4 show harmonic plots for C_B at values of $165\mu F$, $220\mu F$, $330\mu F$ and $470\mu F$ at 100V and 230V with a 200W input. From these figures it can be seen that $165\mu F$ gives the lowest harmonics for class A and D at both voltages. This is because the bulk capacitor is recharging over a longer period.
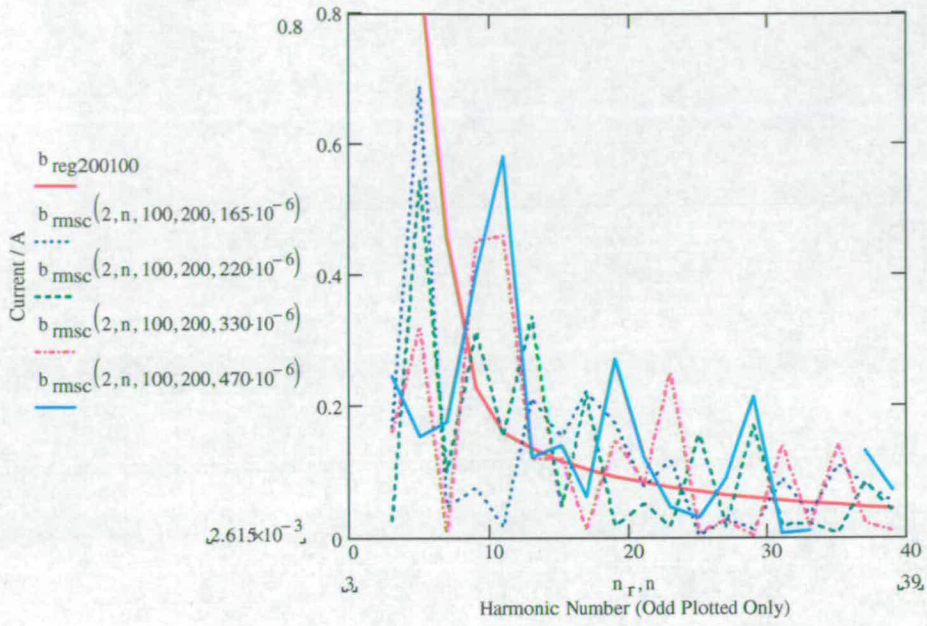
Figure B.1: RMS input current harmonics compared to class D (curve $b_{reg200100}$) for 100V input with an input power of 200W with n as 2 and C_B as 165μF, 220μF, 330μF and 470μF. Traces are listed by side of graph, 1st value is n, 2nd value is the input voltage, 3rd value is the power and 4th the capacitor value.
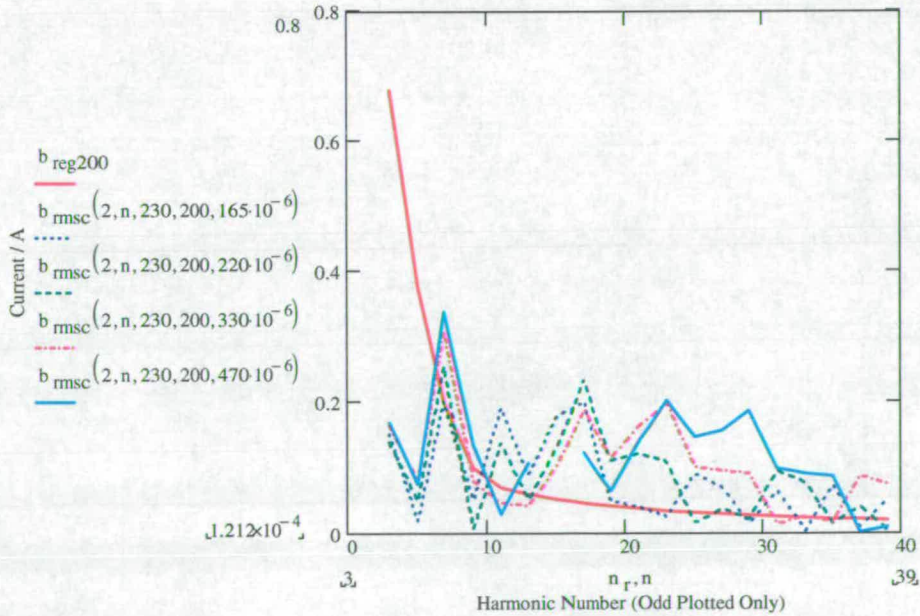
Figure B.2: RMS input current harmonics compared to class D (curve b_{reg200}) for 230V input with an input power of 200W with n as 2 and C_B as 165μF, 220μF, 330μF and 470μF. Traces are listed by side of graph, 1st value is n, 2nd value is the input voltage, 3rd value is the power and 4th the capacitor value.

205
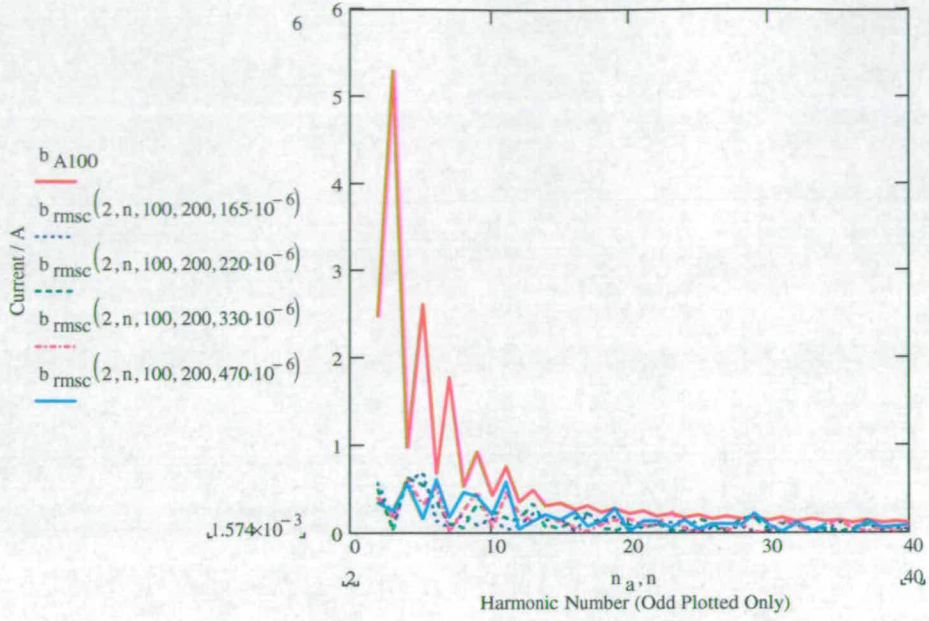
Figure B.3: RMS input current harmonics compared to class A (curve b_{A100}) for 100V input with an input power of 200W with n as 2 and C_B as 165μF, 220μF, 330μF and 470μF. Traces are listed by side of graph, 1st value is n, 2nd value is the input voltage, 3rd value is the power and 4th the capacitor value.
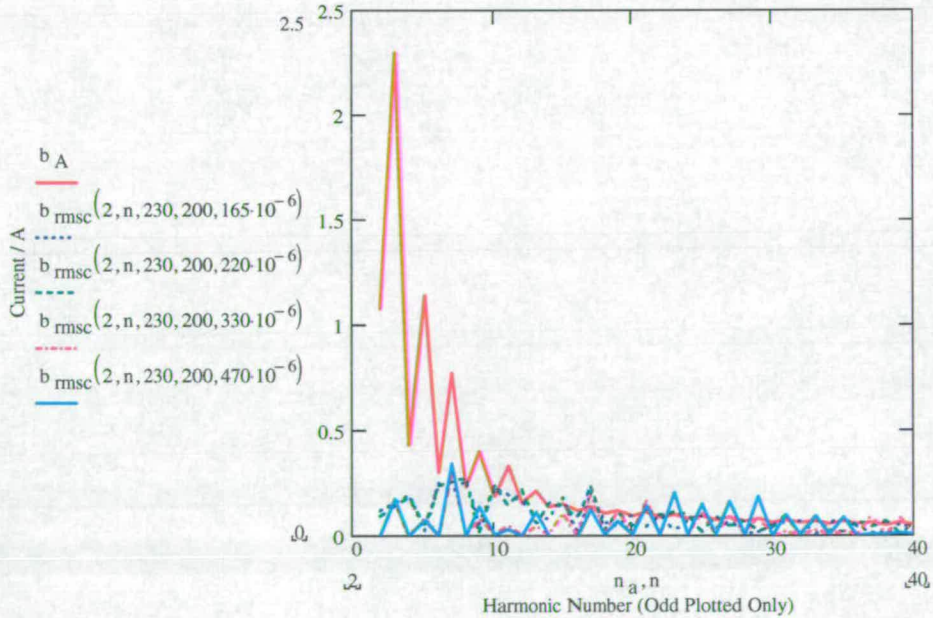
Figure B.4: RMS input current harmonics compared to class D (curve b_{200100}) for 100V input with an input power of 200W with n as 2 and C_B as 165μF, 220μF, 330μF and 470μF. Traces are listed by side of graph, 1st value is n, 2nd value is the input voltage, 3rd value is the power and 4th is the capacitor value.

Appendix C

Predicted Results for N_{1A} as 32 and N_{1B} as 12 for the Bi-Forward with Input Inductor

Shown in figure C.1 is the predicted bulk capacitor voltage for 265V input for N_{1A} =32 and N_{1B} =12. The peak voltage is about 386V which much lower than the 430V predicted for $N_{1A} = N_{1B} = 22$.
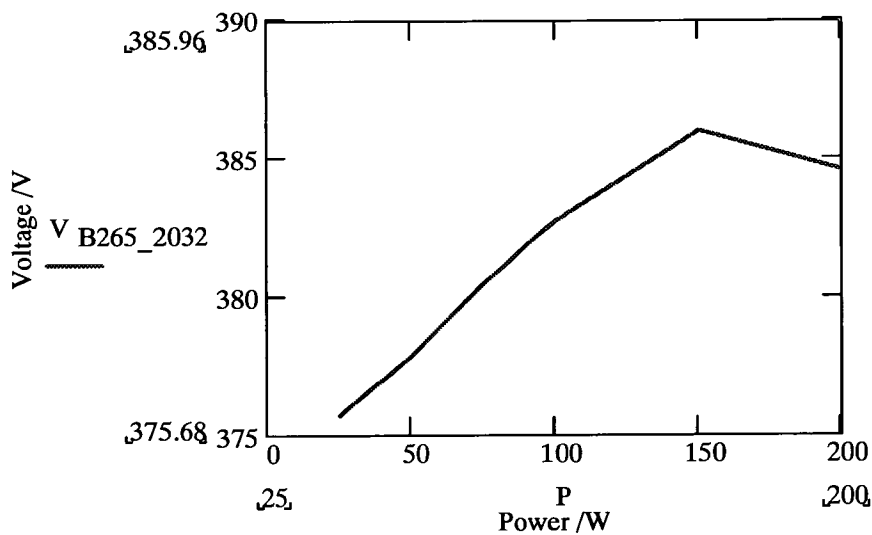
Figure C.1: Predicted voltage on bulk capacitor C_B at 265V input for $L_1 = 20\mu$H and $N_{1A} = 32$ and $N_{1B} = 12$

As shown in figure C.2 for 100V and 75W, input the converter is predicted to meet the class D regulation. This is the same as for the measured result for $N_{1A} = 32$ turns in figure 5.24. The analysis shows that the converter will operate in periods 1, 2, 3 and 4.
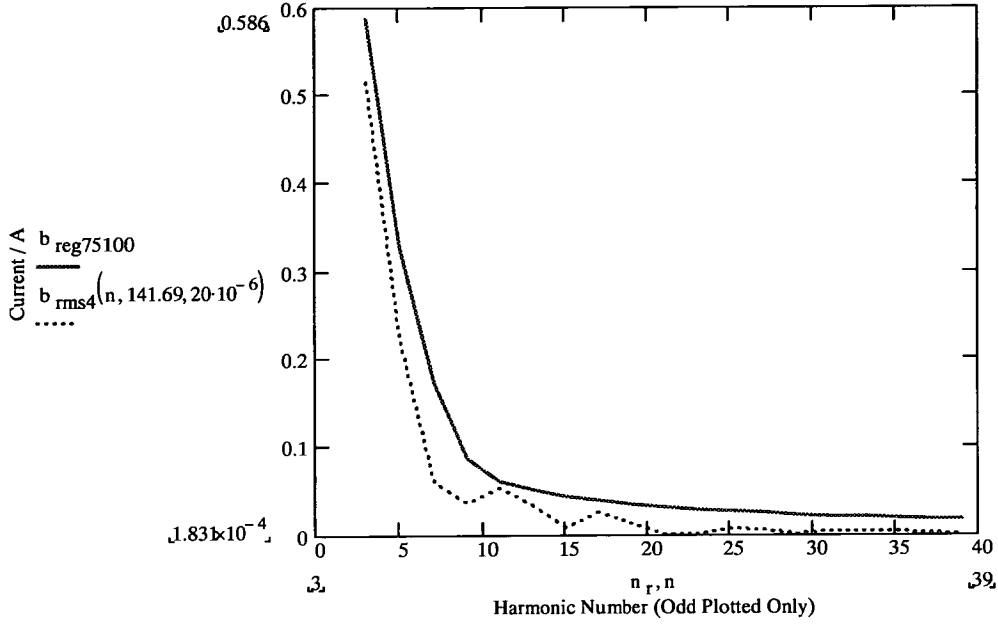
Figure C.2: Input current class D (trace $b_{reg75100}$) harmonics for 100V input with an input power of 75W with L_1 as 20μH and N_{1A} as 32 turns and N_{1B} as 12 turns (other trace, 1st value is voltage on C_B and 2nd value is the value of L_1)

Figure C.3 shows that the converter with $N_{1A} = 32$ turns will fail on the 3rd, 5th and 7th harmonics for 100V and 200W input. The measured results shows failure on the 9th, 11th, 13th and 15th harmonics. These are not the same harmonics, but both are failures. The analysis shows the converter operating in periods 1, 2 and 2A.

Figure C.4 shows that the converter with $N_{1A} = 32$ turns will fail on the 11th and 13th harmonics for 230V and 75W input. The measured results shows failure on the 9th, 11th and 13th harmonics. These are more or less the same harmonics and both are failures. The analysis shows that the converter operates in periods 1, 2 and 3 and 4.

Figure C.5 shows that the converter with N_{1A} as 32 turns will fail on the 3rd, 5th, 7th, 9th, 11th, 13th and 15th harmonics for 230V and 200W input. The measured results showed that all the harmonics measured were below the class D limit. The prediction shows that the design will not meet class D, but in practice it did. This is the first case where the predicted RMS harmonic current did not produce a result close to measured RMS harmonic current

208

The graph shows plots labeled with:

$\frac{b_{reg200100}}{b_{rms2}(n, 144.34, 20 \cdot 10^{-6})}$

Current / A

y-axis values: 2, 1.5, 1, 0.5, 0 with 1.599 at top and 2.606×10^{-3} near bottom

x-axis: 0, 5, 10, 15, 20, 25, 30, 35, 40 with 3 and 39 marked

n_r, n

Harmonic Number (Odd Plotted Only)
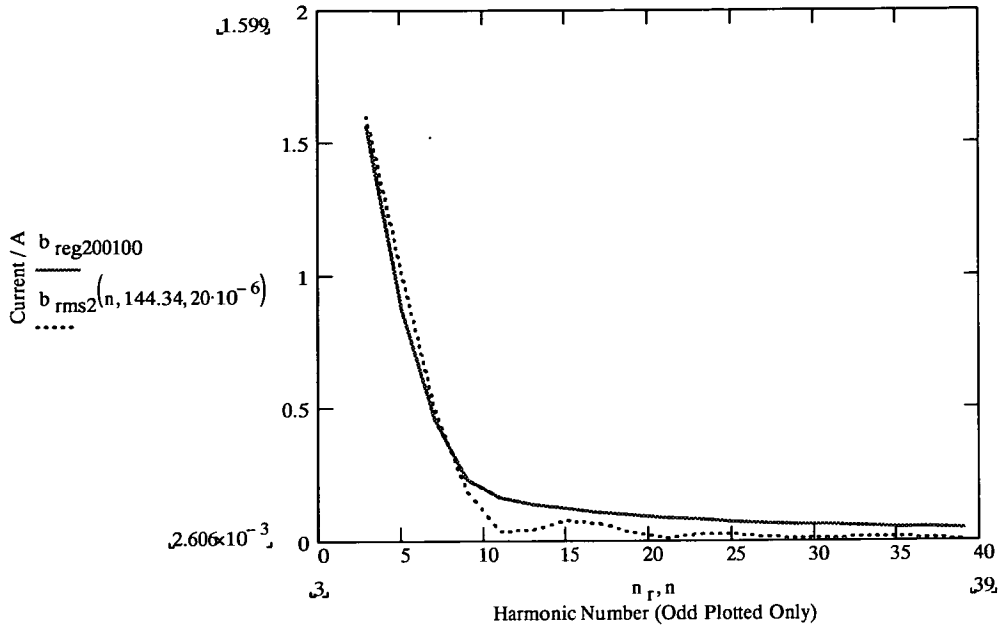
Figure C.3: Input current class D (trace $b_{reg200100}$) harmonics for 100V input with an input power of 200W with L_1 as $20\mu H$ and N_{1A} as 32 turns and N_{1B} as 12 turns (other trace, 1st value is voltage on C_B and 2nd value is the value of L_1)

The graph shows plots labeled with:

$\frac{b_{reg75}}{b_{rms}(n, 330.22, 20 \cdot 10^{-6})}$

Current / A

y-axis values: 0.3, 0.25, 0.2, 0.15, 0.1, 0.05, 0 with 0.255 at top and 2.145×10^{-5} near bottom

x-axis: 0, 5, 10, 15, 20, 25, 30, 35, 40 with 3 and 39 marked

n_r, n

Harmonic Number (Odd Plotted Only)
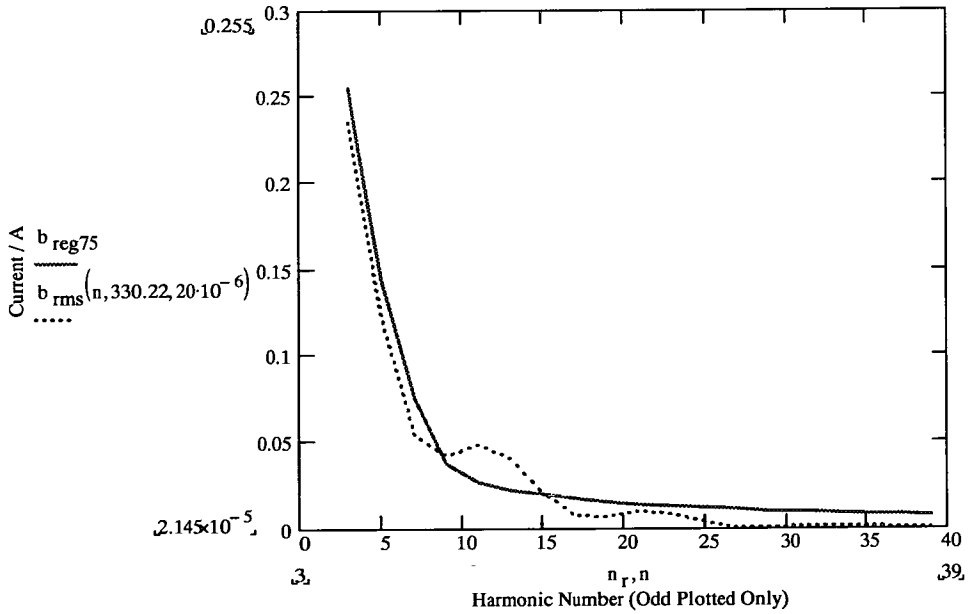
Figure C.4: Input current class (trace b_{reg75}) D harmonics for 230V input with an input power of 75W with L_1 as $20\mu H$ and N_{1A} as 32 turns and N_{1B} as 12 turns (other trace, 1st value is voltage on C_B and 2nd value is the value of L_1)

209

values. The analysis shows the converter operating in periods 1, 2 and 2A.
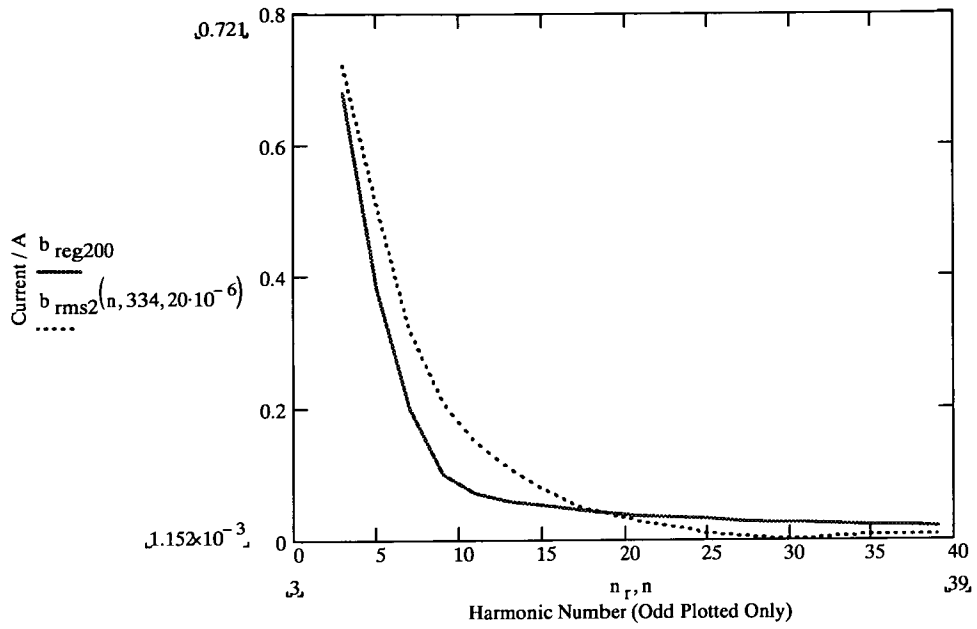
Figure C.5: Input current class D (trace b_{reg200}) harmonics for 230V input with an input power of 200W with L_1 as $20\mu H$ and N_{1A} as 32 turns and N_{1B} as 12 turns (other trace, 1st value is voltage on C_B and 2nd value is the value of L_1)

Appendix D

Predicted Performance of Final CS S^{2}PFC Designs

To give some idea of the performance of the final converter design and altered converter design, figures D.1 and D.2 show their predicted harmonic content for 200W input power at 100V and 230V and figure D.3 shows how the bulk capacitor voltage varies with power at 265V input. Figures D.1 and D.2 both show that harmonics for L_{DA} and L_{DB} as 33 or 43μH are very close to the class D harmonic limit at 100V, just exceeding the 3rd and 5th harmonics and at 230V just exceeding the limit on the 5th and 7th harmonics for 200W input power (assuming 75% efficiency) and thus has a good chance of passing class D at full load. For both of these designs the average bulk capacitor voltage is lower than the peak of the line voltage, but are within 10% of the line voltage peak. In figure D.3 the peak bulk capacitor voltage is shown to be about 430V for both designs. The predicted input current waveform at 230V and 100V and 200W input are shown in figures 6.12a and 6.12b. The obvious difference is that the 100V current waveform has a higher peak current, but more subtle is that L_1 spends less time in DCM at 100V.
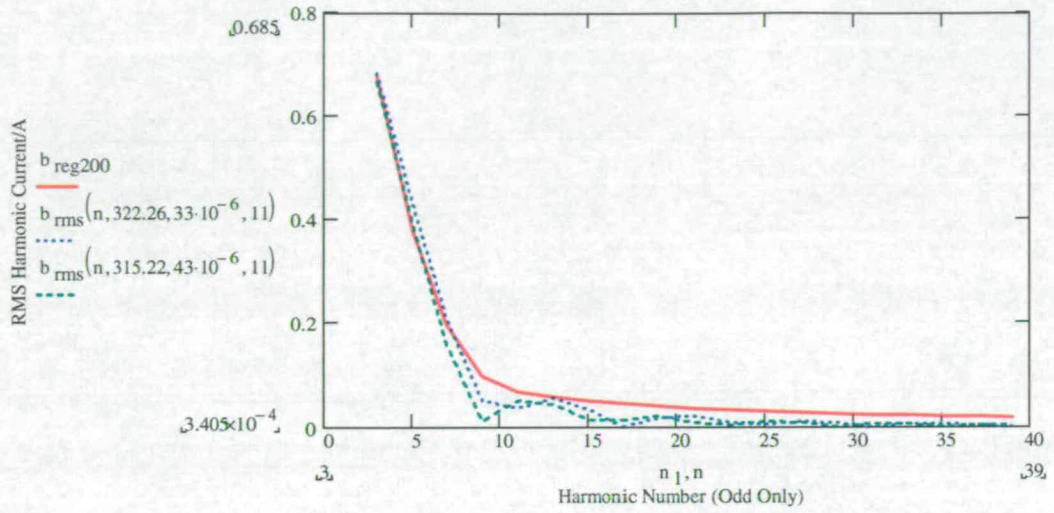
Figure D.1: Odd harmonic content of L_{DA} and $L_{DB} = 33\mu H$ with N_{4A} and $N_{4B} =$ 11 and L_{DA} and $L_{DB} = 43\mu H$ with N_{4A} and $N_{4B} = 11$ at 200W input power and 230V input voltage compared to class D limits (b_{reg200}). Traces are listed by side of graph, 1st value is the voltage on C_B, 2nd value is the value of L_{DA} and L_{DB} and 3rd value is the number of turns on N_{4A} and N_{4B}.
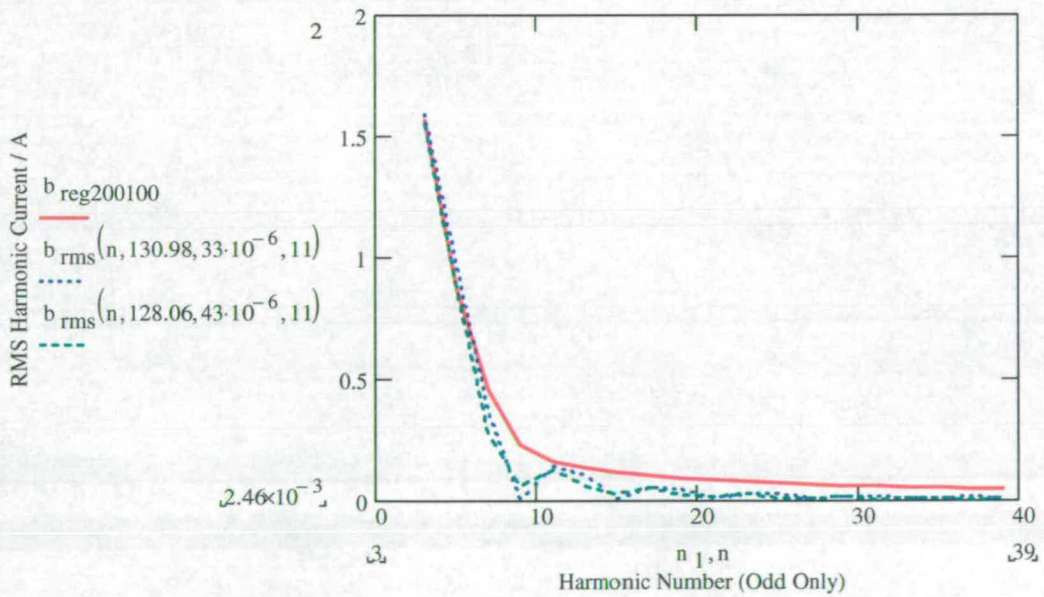
Figure D.2: Odd harmonic content of L_{DA} and $L_{DB} = 33\mu H$ with N_{4A} and $N_{4B} =$ 11 and L_{DA} and $L_{DB} = 43\mu H$ with N_{4A} and $N_{4B} = 11$ at 200W input power and 100V input voltage compared to class D limits ($b_{reg200100}$). Traces are listed by side of graph, 1st value is the voltage on C_B, 2nd value is the value of L_{DA} and L_{DB} and 3rd value is the number of turns on N_{4A} and N_{4B}.

212
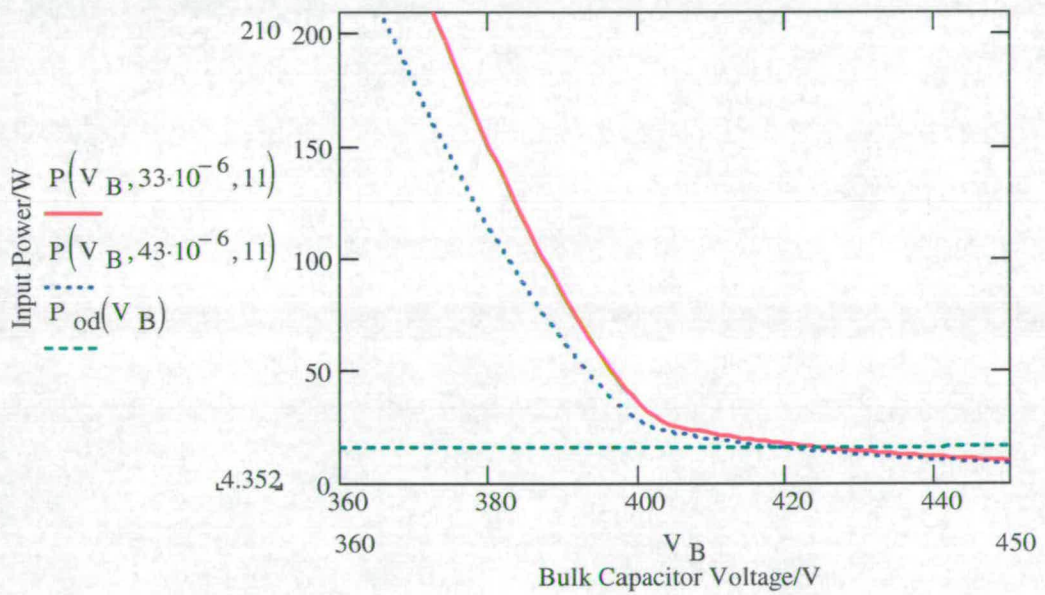
Figure D.3: Power against bulk capacitor voltage for $100V_{RMS}$ input for L_{DA} and $L_{DB} = 33\mu H$ with N_{4A} and $N_{4B} = 11$ and L_{DA} and $L_{DB} = 43\mu H$ with N_{4A} and $N_{4B} = 11$. Traces are listed by side of graph, 1st value is the value of L_{DA} and L_{DB} and 2nd value is the number of turns on N_{4A} and N_{4B}.

Appendix E

Predicted Harmonic Content at 230V for the LFSPFC Converter

Shown in figures E.1, E.2 and E.3 are the harmonic plots compared to class D at 230V and 133W input power for the LFSPFC converter for input inductances of 10, 20 and $30\mu H$ respectively.
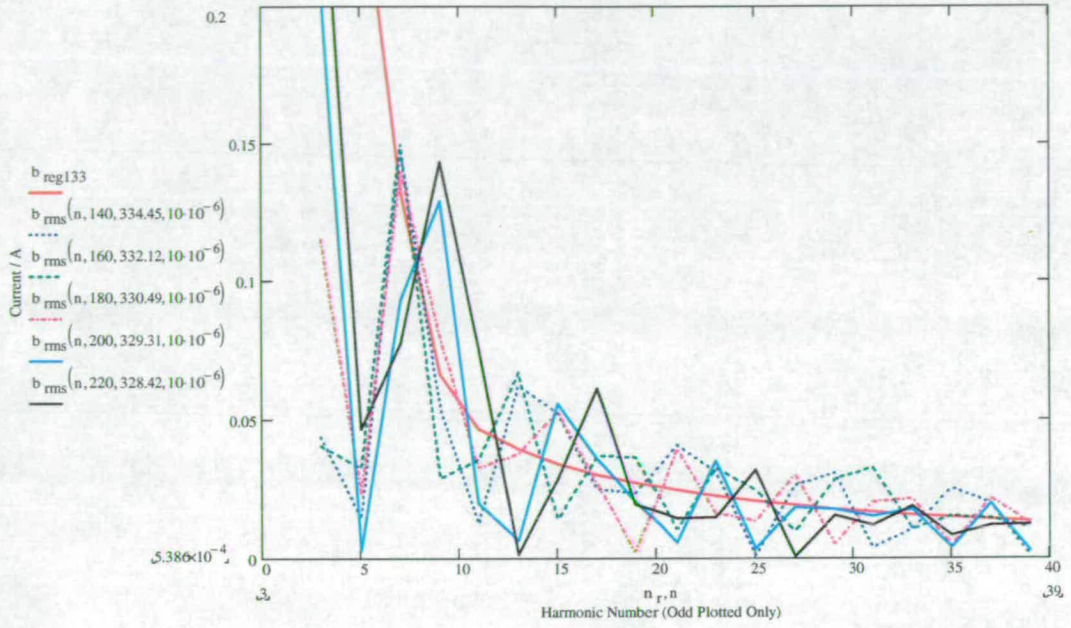
Figure E.1: RMS input current harmonics compared to the class D (trace b_{reg133}) limits for 230V, 133W input with the turn on/off voltage of S_2 as 140, 160, 180, 200 and 220V and L_1 as 10μH. Traces are listed by side of graph: 1st value is the turn on/off voltage for S_2, 2nd value is the voltage on C_B and 3rd value is the value of L_1.
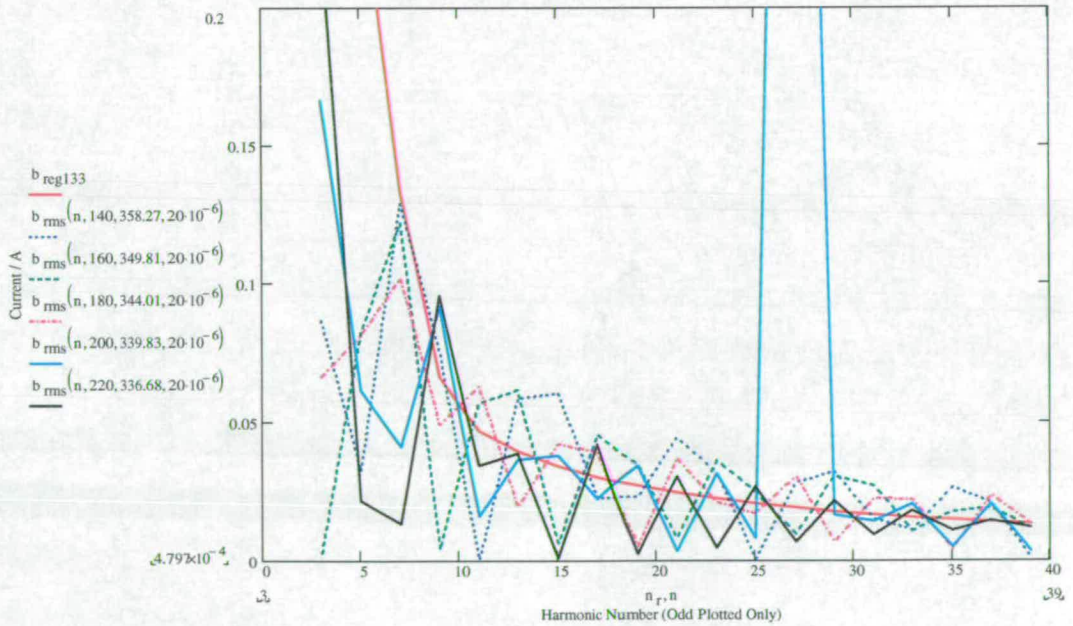
Figure E.2: RMS input current harmonics compared to the class D (trace b_{reg133}) limits for 230V, 133W input with the turn on/off voltage of S_2 as 140, 160, 180, 200 and 220V and L_1 as 20μH. Traces are listed by side of graph: 1st value is the turn on/off voltage for S_2, 2nd value is the voltage on C_B and 3rd value is the value of L_1.
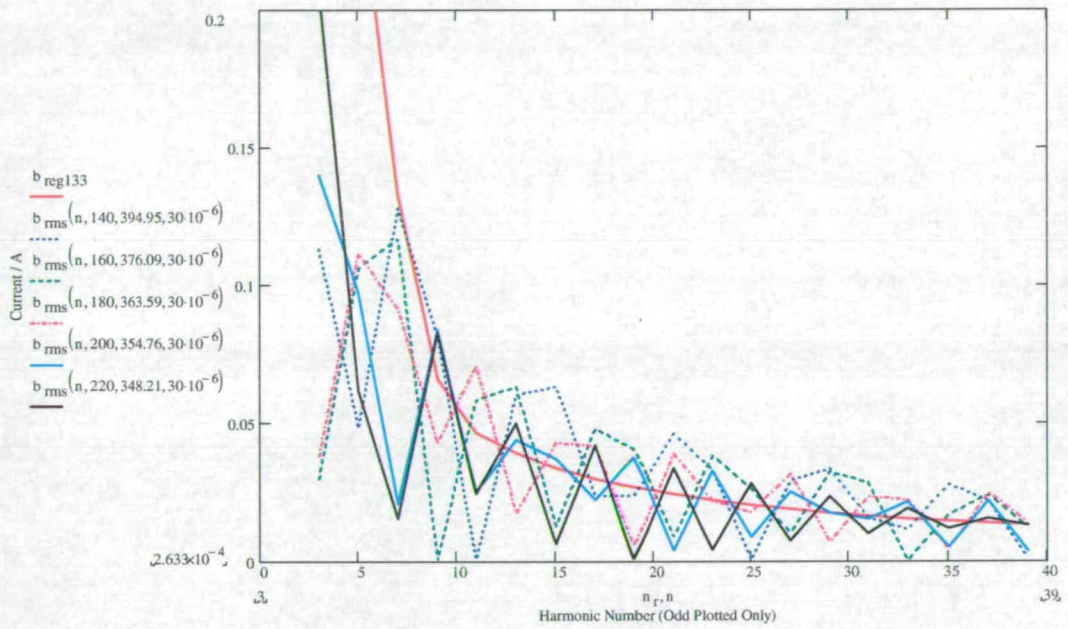
Figure E.3: RMS input current harmonics compared to the class D (trace b_{reg133}) limits for 230V, 133W input with the turn on/off voltage of S_2 as 140, 160, 180, 200 and 220V and L_1 as 30μH. Traces are listed by side of graph: 1st value is the turn on/off voltage for S_2, 2nd value is the voltage on C_B and 3rd value is the value of L_1.

Appendix F

RMS Harmonic Currents Measured in PSpice

F.1   Bi-Forward Converter

Tables F.1 and F.2 show current harmonics measured in PSpice for full input power at 230V and 100V respectively.

F.2   Bi-Forward Converter with Input Inductor

Tables F.3 and F.4 show current harmonics measured in PSpice for full input power at 100V and 230V respectively.

F.3   CS S^2PFC Converter

Tables F.5 and F.6 show current harmonics measured in PSpice for full input power at 230V and 100V respectively.

Harmonic Number	RMS Harmonic Current/A	Class A Limits/A	Class D Limits/A
2	1.793m	1.08	
3	0.175	2.3	0.5882
4	1.758m	0.43	
5	0.166	1.14	0.3297
6	1.783m	0.3	
7	0.308	0.77	0.173
8	1.875m	0.23	
9	0.214	0.4	0.0865
10	1.764m	0.184	
11	0.214	0.33	0.06055
12	1.706m	0.153	
13	0.163	0.21	0.0512
14	1.819m	0.131	
15	0.158	0.15	0.0444
16	1.850m	0.115	
17	0.258	0.182	0.0392
18	1.729m	0.102	
19	0.0742	0.118	0.0351
20	1.693m	0.092	
21	0.0976	0.107	0.0317
22	1.845m	0.0836	
23	0.115	0.0978	0.029
24	1.934m	0.0766	
25	0.0668	0.09	0.0266
26	1.708m	0.0708	
27	0.0623	0.0833	0.0247
28	1.694m	0.0657	
29	0.0430	0.0776	0.0230
30	1.692m	0.0613	
31	0.0757	0.0726	0.0215
32	1.68m	0.0575	
33	0.0534	0.0682	0.0202
34	1.594m	0.0541	
35	0.0327	0.0643	0.01903
36	1.562m	0.0511	
37	0.0623	0.0608	0.0180
38	1.701m	0.0484	
39	0.0474	0.0577	0.0171
40	1.672m	0.046	

Table F.1: RMS current harmonics measured for the bi-forward converter in PSpice for 230V at full Load with an input power of 173W for classes A and D.

218

Harmonic Number	RMS Harmonic Current/A	Class A Limits/A	Class D Limits/A
2	3.575m	2.484	
3	0.515	5.29	1.392
4	2.792m	0.989	
5	0.545	2.622	0.778
6	2.398m	0.69	
7	0.215	1.771	0.4094
8	2.727m	0.529	
9	0.330	0.92	0.2047
10	3.429m	0.4252	
11	0.248	0.759	0.1433
12	3.818m	0.352	
13	0.312	0.483	0.1212
14	3.495m	0.3013	
15	0.0961	0.345	0.1051
16	2.828m	0.2645	
17	0.137	0.3036	0.0927
18	2.160m	0.2346	
19	0.0668	0.2714	0.0830
20	2.534m	0.2116	
21	0.130	0.2461	0.0751
22	3.412m	0.1923	
23	0.0926	0.2249	0.0685
24	3.165m	0.1762	
25	0.170	0.207	0.0630
26	3.459m	0.163	
27	0.0594	0.192	0.0584
28	2.832m	0.151	
29	0.0742	0.1785	0.0544
30	1.099m	0.141	
31	0.0308	0.1670	0.0508
32	2.202m	0.1323	
33	0.0813	0.1569	0.0478
34	2.980m	0.1244	
35	0.0482	0.1479	0.0450
36	3.369m	0.1175	
37	0.111	0.1398	0.0426
38	3.324m	0.1113	
39	0.0519	0.1327	0.0404
40	2.699m	0.1058	

Table F.2: RMS current harmonics measured for the bi-forward converter in PSpice for 100V at full Load with an input power of 178W for classes A and D

219

Harmonic Number	RMS Harmonic Current for $L_1 = 10\mu$H /A	RMS Harmonic Current for $L_1 = 20\mu$H /A	Class D Limits/A
3	0.6453	0.9023	1.381
5	0.2248	0.2040	0.772
7	0.06305	0.1706	0.406
9	0.1335	0.0630	0.203
11	0.04079	0.02483	0.1422
13	0.0927	0.04451	0.1203
15	0.05192	0.01939	0.1043
17	0.04821	0.01124	0.092
19	0.02799	0.01267	0.0823
21	0.01517	0.01393	0.0745
23	0.01739	0.0094	0.0680
25	0.01604	0.01014	0.0626
27	0.01541	0.0097	0.0579
29	0.01541	0.0064	0.0539
31	0.0014	0.0049	0.0504
33	0.002	0.0049	0.0474
35	0.0088	0.0024	0.0447
37	0.0027	0.0006	0.0423
39	0.0048	0.0022	0.0401

Table F.3: Class D harmonics measured for the bi-forward converter with input inductor in PSpice for 100V 150W output for L_1 as 10μH (input power measured as 179W) and 20μH (input power measured as 177W). Class D harmonics are calculted for $L_1 = 20\mu$H input power, since those for $L_1 = 10\mu$H are similar.

Harmonic Number	RMS Harmonic Current for $L_1 = 10\mu$H /A	RMS Harmonic Current for $L_1 = 20\mu$H /A	Class D Limits/A
3	0.2596	0.3828	0.5725
5	0.05487	0.04895	0.3199
7	0.00757	0.04747	0.1684
9	0.07418	0.00899	0.0842
11	0.00013	0.01018	0.05894
13	0.03116	0.00713	0.04987
15	0.01335	0.00919	0.04322
17	0.01632	0.00563	0.03814
19	0.01114	0.00507	0.03412
21	0.00791	0.00661	0.03087
23	0.00058	0.00255	0.02819
25	0.00095	0.00022	0.02593
27	0.003	0.0019	0.02401
29	0.0011	0.00355	0.02236
31	0.00087	0.00123	0.02091
33	0.00156	0.00198	0.01965
35	0.00022	0.00187	0.01852
37	0.00347	0.00106	0.01752
39	0.00105	0.00061	0.01662

Table F.4: Class D harmonics measured for the bi-forward converter with input inductor in PSpice for 100V 150W output for L_1 as 10μH (input power measured as 168W) and 20μH (input power measured as 170W). Class D harmonics are calculated for $L_1 = 20\mu$H input power since those for $L_1 = 10\mu$H are similar.

Harmonic Number	RMS current/A	Class D Limits/A
3	0.593	0.593
5	0.377	0.331*
7	0.199	0.174*
9	0.0682	0.0872
11	0.0252	0.0611
13	0.0460	0.0517
15	0.0371	0.0448
17	0.0134	0.0395
19	0.0107	0.0353
21	0.0178	0.0320
23	0.0134	0.0292
25	0.00375	0.00269
27	0.00735	0.0249
29	0.0101	0.0232
31	0.00634	0.0217
33	0.00139	0.0204
35	0.00542	0.0192
37	0.00570	0.0182
39	0.00266	0.0172

Table F.5: Class D harmonics measured for the CS S^2PFC converter in PSpice for 230V 150W output for L_D as 33μH (input power measured as 174W). * indicates harmonics that exceeded the regulation.

Harmonic Number	RMS current/A	Class D Limits/A
3	1.320	1.383
5	0.735	0.773
7	0.297	0.407
9	0.104	0.203
11	0.134	0.142
13	0.0926	0.120
15	0.0334	0.104
17	0.0482	0.0921
19	0.0445	0.0824
21	0.0181	0.0746
23	0.0234	0.0681
25	0.0256	0.0626
27	0.0128	0.0580
29	0.0125	0.0540
31	0.0171	0.0505
33	0.0087	0.0474
35	0.00728	0.0447
37	0.0107	0.0423
39	0.00676	0.0401

Table F.6: Class D harmonics measured for the CS S^2PFC converter in PSpice for 100V 150W output for L_D as 33μH (input power measured as 177W)

F.4 LFSPFC Converter

Table F.7 shows current harmonics measured in PSpice for full input power at 230V.

Harmonic Number	RMS Harmonic Current/A Basic	RMS Harmonic Current/A with L_1	Class A Limits/A	Class D Limits/A
2	26m	0.208m	1.08	
3	0.0714	0.245	2.3	0.390
4	2.16m	0.0843m	0.43	
5	0.0863	0.0346	1.14	0.218
6	1.61m	0.134m	0.3	
7	0.21*	0.0148	0.77	0.115
8	1.56m	0.224m	0.23	
9	0.109*	0.0801*	0.4	0.0574
10	0.71m	0.214m	0.184	
11	0.109*	0.0623*	0.33	0.0402
12	0.529m	0.157	0.15	
13	0.131*	0.0208	0.21	0.0340
14	0.226m	0.0842m	0.131	
15	0.117*	0.0208	0.15	0.0295
16	0.438m	0.0258m	0.115	
17	0.0877*	0.0257	0.132	0.0260
18	0.314m	0.105m	0.102	
19	0.0813*	0.0267	0.118	0.0233
20	0.595m	0.0878m	0.092	
21	0.106*	0.0158	0.107	0.0210
22	0.707m	0.0152m	0.0836	
23	0.0504*	0.0198*	0.0978	0.0192
24	0.162m	0.0839m	0.0766	
25	0.0554*	0.0119	0.09	0.0177
26	0.39m	0.0332m	0.0708	
27	0.0778*	0.0178*	0.0833	0.0164
28	0.192m	0.101m	0.0657	
29	0.0257*	0.00989	0.0776	0.0152
30	0.335m	0.208m	0.0613	
31	0.0425*	0.00168	0.0726	0.0143
32	0.079m	0.205m	0.0575	
33	0.0455*	0.00791	0.0682	0.0134
34	0.509m	0.09971m	0.0541	
35	0.0337*	0.0138*	0.0643	0.0126
36	0.371m	0.0936	0.0511	
37	0.0257*	0.00707	0.0608	0.0119
38	0.13m	0.175m	0.0484	
39	0.0238*	0.0119*	0.0577	0.0113
40	0.238m	0.170m	0.046	

Table F.7: RMS current harmonics measured for the LFSPFC converter in PSpice for 230V at full load compared to class A and D harmonic levels. The basic LFSPFC converter has an input power of 116W and the LFSPFC converter with input inductor has an input power of 115W and L_1 as 20μH. Class D values are for 115W.* indicates measured harmonics that exceed the regulation for class D.

Appendix G

Components Used in Test Circuits

G.1 Bi-Forward and Bi-Forward with Input Inductor Converters

Table G.1 shows the components used to build the bi-forward converter.

G.2 CS S^{2}PFC Converter

Table G.2 shows the components used to build the CS S^{2}PFC converter.

G.3 LFSPFC Converter

Table G.3 shows the components used to build the LFSPFC converter.

Device	Component
S_1	APT1201R2BLL
D_1, D_2, D_3	BY329-1000
$D_{4:5V}, D_{5:5V}$	BY51-200
$D_{4:12V}, D_{5:12V}$	BYT08P-400
D_6, D_7	BYD33U
DB	GBU6J
C_B	$2 \times 330\mu$F 250V Electrolytic
$C_{1:5V}$	2200μF 16V Electrolytic
$C_{1:12V}$	470μF 25V Electrolytic
C_2	1μF 400V Polyester
C_3	$47p$F 1500V Polyester
R_1	$2 \times 470\Omega$ 2W
$L_{2:5V}$	15μH
$L_{2:12V}$	64μH
Transformer	ETD44 3C90 Material
	$N_{1A} = N_{1B} = N_3 = 22$
	$N_{2:5V} = 5 \ N_{2:12V} = 11$
UC3524	VMC Controller
MC33152P	MOSFET Driver
D_8	1N4148
C_4	100μF 35V Electrolytic
C_5	47μF 35V Tantalum
C_6, C_7	1μF Ceramic
C_8	$2.2n$F Ceramic
C_9	$44n$F Ceramic
R_2, R_3, R_4	2.7kΩ
R_5	10kΩ
R_6	10Ω 0.5W
R_7	12kΩ
R_{8A}	39kΩ
R_{8B}	3.9kΩ
R_9	1kΩ
R_{10}	2.9kΩ
R_{11}	18kΩ

Table G.1: Components used in the bi-forward converter and its control circuit

Device	Component
S_1	IXFH12N100
$D_1, D_{4A}, D_{4B}, D_{5A}, D_{5B}$	BY329-1000
$D_{2:5V}, D_{3:5V}$	STPS20H100
$D_{2:12V}, D_{3:12V}$	BYT08P-400
D_6	BYD33U
DB	GBU6J
C_{B1}, C_{B2}	330μF 250V Electrolytic
$C_{1:5V}$	2200μF 16V Electrolytic
$C_{1:12V}$	470μF 25V Electrolytic
C_{2A}, C_{2B}	1μF 400V Polyester
C_3	$47p$F 1500V Polyester
R_1	$2\times470\Omega$ 2W
L_{DA}, L_{DB}	43μH on the same core
L_{1A}, L_{1B}	100μH on the same core
$L_{2:5V}$	15μH
$L_{2:12V}$	64μH
Transformer	ETD44 3C90 Material
	$N_1 = N_3 = 44$
	$N_{2:5V} = 3\ N_{2:12V} = 7$
	$N_{4A} = N_{4B} = 11$

Table G.2: Components used in the CS S^2PFC converter. The control circuit components are the same as listed in table G.1 for the bi-forward converter

227

Device	Component
S_1	2SK2611
S_2	IRG4BC30W
D_1, D_2	BY329-1000
D_3, D_4	STPS20H100CT
D_5, D_6	BYD33U
DB	GBU6J
C_B	$2\times330\mu$F 250V Electrolytic
C_1	2200μF 16V Electrolytic
C_2	1μF 400V Polyester
C_3	$47p$F 1500V Polyester
R_1	$2\times470\Omega$ 2W
L_1	20μH
L_2	15μH
Transformer	ETD44 3C90 Material
	$N_1 = N_3 = 44\ N_{2:5V} = 5$
UC3524	VMC Controller
MC33152P	MOSFET Driver
D_8	1N4148
C_4	100μF 35V Electrolytic
C_5	47μF 35V Tantalum
C_6, C_7	1μF Ceramic
C_8	$2.2n$F Ceramic
C_9	$44n$F Ceramic
R_2, R_3, R_4	2.7kΩ
R_5	10kΩ
R_6	10Ω 0.5W
R_7	12kΩ
R_{8A}	2.7kΩ
R_9	1kΩ
R_{10}	2kΩ
R_{11}	18kΩ
LM 311	Comparator
IR2117	Signal Level Shifter
D_8	UF5407
C_{10}	$100p$F Polyester
C_{11}, C_{13}	100μF 35V Electrolytic
C_{12}	47μF 35V Electrolytic
C_{14}, C_{15}	1μF Ceramic
R_{12}	1MΩ
R_{13}	100kΩ
R_{14}	39kΩ
R_{15}	12kΩ
R_{16}	3.9kΩ
R_{17}	10kΩ
R_{18}	10kΩ
R_{19}	47Ω 0.5W
V_1	16V

Table G.3: Components used in the LFSPFC converter and its control circuit

Appendix H

Measured Efficiency and Bulk Capacitor Voltage

H.1   Bi-Forward Converter with Input Inductor

Table H.1 presents the measured efficiency and bulk capacitor voltage for the bi-forward converter with input inductor.

H.2   CS S^{2}PFC Converter

Table H.2 presents the measured efficiency and bulk capacitor voltage for the CS S^{2}PFC converter.

H.3   LFSPFC Converter

Table H.3 presents the measured efficiency and bulk capacitor voltage for the LFSPFC converter with a turn on/off voltage of 140V and table H.4 presents the measured efficiency and bulk voltage for the LFSPFC converter with input inductor and a turn on/off voltage of 230V.

Output Power/W	Input Power/W	Efficiency/%	Bulk Capacitor Voltage/V
Input Voltage: 90V			
2.73	5	54.6	129
36.68	48.41	75.62	133
72.82	99.02	73.54	135
108.89	155.02	70.24	135
138.62	218.6	63.41	131
Input Voltage: 115V			
2.72	5	54.33	162
36.68	48.64	75.41	170
72.82	97.85	74.52	172
108.89	151.57	71.84	178
144.43	210.77	68.53	176
Input Voltage: 130V			
2.72	5	54.33	183
36.68	48.93	74.97	194
72.82	97.72	74.52	196
108.89	150.82	72.20	204
144.03	207.86	69.29	201
Input Voltage: 180V			
2.72	6	45.28	257
36.68	50.34	72.87	277
72.82	98.66	73.81	281
108.89	150.21	72.49	290
144.43	203.9	70.83	283
Input Voltage: 230V			
2.7	8	33.74	334
36.68	51.24	71.59	336
72.82	100.53	72.44	366
109.04	151.48	71.98	373
144.63	204.14	70.85	360
Input Voltage: 265V			
2.7	8	33.61	385
36.73	52.3	70.23	386
72.92	102.35	71.25	426
109.19	153.1	71.32	430
144.63	205.04	70.41	416

Table H.1: Measured efficiency and voltage on the bulk capacitor for the bi-forward with input inductor for $L_1 = 20\mu H$ across the input voltage range

Output Power/W	Input Power/W	Efficiency/%	Bulk Capacitor Voltage/V
Input Voltage: 90V			
3.25	6	54.09	283
37.36	49.14	76.03	272
74.35	96.08	77.38	257
111.63	146.5	76.20	243
148.46	199.2	74.53	230
Input Voltage: 115V			
3.21	8	40.08	355
37.36	50.71	73.68	343
74.35	97.00	76.65	332
111.78	146.20	76.46	320
148.46	197.2	75.28	309
Input Voltage: 130V			
3.21	8	40.07	398
37.42	51.82	72.20	387
74.45	97.99	75.96	377
111.48	146.75	75.96	364
148.66	197.3	75.34	355
Input Voltage: 180V			
3.25	6	54.09	285
37.36	48.82	76.53	276
74.15	94.98	78.06	275
111.63	144	77.53	256
148.46	194.8	76.21	246
Input Voltage: 230V			
3.23	8	40.39	356
37.47	50.5	74.17	350
74.45	96.3	77.31	339
111.48	144.6	77.09	332
148.46	194.7	76.25	326
Input Voltage: 265V			
3.21	8	40.1	408
37.36	51.93	71.95	400
74.45	97.57	76.30	391
111.48	145.66	76.53	383
148.66	195.38	76.09	376

Table H.2: Measured efficiency, input and output power and bulk capacitor voltage across the input range for the CS S^2PFC converter

Output Power/W	Input Power/W	Efficiency/%	Bulk Capacitor Voltage/V	Peak of Supply Voltage/V
Input Voltage: 180V				
24.9	30.5	81.64	242	250
49.7	61.4	80.94	237.5	243
74.25	95.6	77.67	237.5	243
96.628	125.8	76.81	237.5	243
Input Voltage: 200V				
24.9	30.4	81.91	265	266
49.7	60.7	81.88	265	266
75.24	95.1	79.12	270	266
97.614	125.3	77.90	268	266
Input Voltage: 230V				
24.95	31.3	79.71	306	313
49.7	61.7	80.55	306	313
74.25	93.4	79.5	306	313
96.628	123.8	78.05	306	313

Table H.3: Measured efficiency, input and output power and bulk capacitor voltage across the available input voltage range for the LFSPFC converter without L_1 and a S_2 turn on/off voltage of 140V

Output Power/W	Input Power/W	Efficiency/%	Bulk Capacitor Voltage/V	Peak of Supply Voltage/V
Input Voltage: 180V				
24.95	30.1	82.89	240.6	237
49.7	60.6	82.01	240.6	237
74.25	94	78.99	239.1	237
96.614	126.2	77.35	239.3	237
Input Voltage: 200V				
24.451	29.1	81.78	276.7	268.7
49.7	62.5	79.52	277.6	268
75.735	97.7	77.52	277.3	268.7
95.642	123.6	77.38	276.6	268.7
Input Voltage: 230V				
24.95	31.3	79.71	320	312
49.7	62.6	79.39	321	312
75.24	97.1	77.49	323	312
97.121	126.7	76.65	325	312

Table H.4: Measured efficiency, input and output power and bulk capacitor voltage across the available input voltage range for the LFSPFC converter with L_1 and a S_2 turn on/off voltage of 230V

H.4 Pasive Filter and Forward Converter

Table H.5 presents the measured efficiency and bulk capacitor voltage for the passive filter and forward converter.

H.5 Two Stage Active PFC

Table H.6 presents the measured efficiency and bulk capacitor voltage for the boost converter cascaded with a forward converter method.

Output Power/W	Input Power/W	Efficiency/%	Bulk Capacitor Voltage/V
Input Voltage: 90V			
2.83	5	56.6	245
37.64	46.18	81.51	236
74.98	93.54	80.16	228
112,49	146.23	76.93	224
149.78	205.4	72.92	223
Input Voltage: 115V			
2.74	6	45.6	313
37.64	47.42	79.37	306
74.94	93.72	79.97	298
112.55	143.73	78.31	293
149.86	197.9	75.73	291
Input Voltage: 130V			
2.76	6	45.94	360
37.64	48.31	77.91	349
74.94	94.25	79.51	340
112.37	143.3	78.42	335
149.75	195.83	76.47	332
Input Voltage: 180V			
2.82	6	47.08	247
37.5	45.91	81	234
72.96	92.16	79.16	225
112.7	142.32	78.95	221
150	199.9	75.04	222
Input Voltage: 230V			
2.74	7	39.12	318
37.5	47.11	79.6	305
74.94	92.71	80.84	296
112.55	141.49	79.55	290
150.04	193.6	77.5	287
Input Voltage: 265V			
2.76	7	39.43	366
37.5	48.24	77.73	355
74.94	93.54	80.11	345
112.52	141.71	79.40	339
149.77	192.51	77.8	336

Table H.5: Measured efficiency, input and output power and bulk capacitor voltage across the input range for passive PFC method

Output Power/W	Input Power/W	Efficiency/%	Bulk Capacitor Voltage/V
Input Voltage: 90V			
2.85	7	40.67	394
37.69	54.16	69.58	392
74.94	101.14	74.1	390
112.64	151.60	74.3	387
149.85	204	73.46	382
Input Voltage: 115V			
2.85	8	35.58	394
37.74	53.7	70.27	392
75.02	100	75.02	390
112.58	149.13	75.49	387
149.81	200.43	74.75	383
Input Voltage: 130V			
2.85	11	25.88	394
37.74	53.57	70.44	392
75.02	99.66	75.23	390
112.58	148.41	75.86	387
149.81	199.22	75.2	383
Input Voltage: 180V			
2.85	13	21.9	395
37.74	52.22	72.26	393
75.02	98.98	75.80	391
112.58	147.11	76.53	387
150.01	197.1	76.11	384
Input Voltage: 230V			
2.85	14	20.33	397
37.74	52.14	72.38	394
75.02	97.98	76.57	391
112.58	146.35	76.93	388
150.01	195.97	76.55	385
Input Voltage: 265V			
2.85	7	40.67	397
37.74	51.41	73.40	394
75.02	97.37	77.05	392
112.58	145.54	77.35	389
150.01	195.16	76.87	385

Table H.6: Measured efficiency, input and output power and bulk capacitor voltage across the input range for boost converter cascaded with a forward converter method

Appendix I

Publications

1. Comparison of Two Single-Stage PFC Topologies with Conventional PFC Solutions for Low Power Isolated Supplies, E.M. Lord and D.E. Macpherson. Presented at EPE 2003 in Toulouse France.

2. A New Single-stage PFC Converter Based on the Forward Converter with a Low Frequency Switch, E.M. Lord and D.E. Macpherson. Presented at PEMD 2004 in Edinburgh Scotland.

Comparison of Two Single-Stage PFC Topologies with Conventional PFC Solutions for Low Power Isolated Supplies

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Keywords

Converter circuits, DC power supplies, Power Factor Correction, Switch mode power supplies.

Abstract

The comparison of two promising single-stage PFC topologies, the bi-forward and high frequency current source single stage power factor corrector, with conventional power factor correction (PFC) solutions is presented. The two new topologies are briefly introduced. The comparison considers efficiency, component stress, cost, and ability to meet IEC1000-3-2 class D.

Introduction

In Europe and Japan it is now a requirement for a SMPS connected to the line, to meet EN 61000-3-2 [1] standard and it's Japanese equivalent. The standard sets strict limits for harmonic content of the input current of a power supply. The strictest part of the regulation is for equipment such as personal computers (PC), which are specifically classified as class D [2]. To meet the regulation, normally either passive filtering using a large inductance as in figure 1 or a boost pre-regulator as in figure 2 is placed in front of the main converter. These two methods are either bulky or component intensive and are often considered expensive. Recently many single-stage PFC topologies have been proposed in an attempt to address these problems, with varying degrees of success. Two of the more promising single-stage PFC topologies, the bi-forward and CS S²PFC converters, have been selected and examined, and compared to the two conventional PFC solutions. Areas of interest are efficiency, ability to meet EN 61000-3-2, component stresses and cost. The comparison is carried out with the application of a 150W forward converter based PC power supply in mind.

Passive Filtering PFC
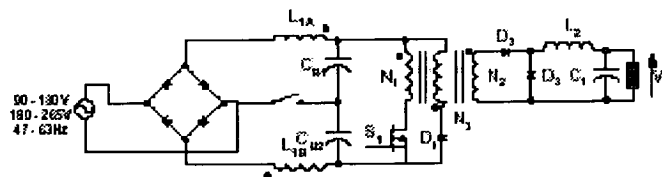
Figure 1: Passive PFC using a large smoothing choke and a forward converter

Shown in Figure 1 is a passive PFC scheme. When operating from the low voltage range the switch is closed and when operating from the high voltage range the switch is open. Inductor L_1 increases the charging time of the bulk capacitors C_{B1} and C_{B2}. The inductor L_1 is normally constructed on an iron laminated core. For a 150W output power supply typically each winding of L_1 is 9mH and the core size is an EI42. This method can only just meet the regulations and is bulky, but it is simple and inexpensive.

Two Stage PFC
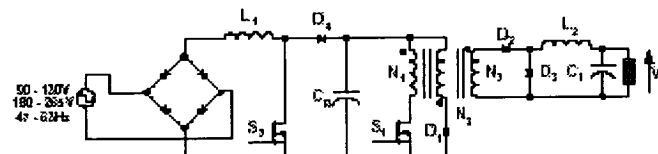
Figure 2: Forward Converter with PFC Boost Pre-Regulator

The two stage scheme is shown in figure 2 implemented using a boost pre-regulator for current shaping cascaded with a forward converter to control the output voltage. The inductor L_1 is typically operated in continuous conduction mode (CCM) and is controlled so that the input current follows the input voltage, hence producing an input current which is nearly sinusoidal with low harmonic content. The voltage on C_B is moderately regulated at about 400V, unlike many single stage topologies. Unfortunately this method requires the addition of an additional converter with many extra components such as S_2, L_1, D_4 and associated control circuitry increasing cost. Efficiency is also reduced as the throughput power is processed twice, even though each stage is highly efficient (80% to 90%) and can be optimised to its own task.

Bi-Forward Converter
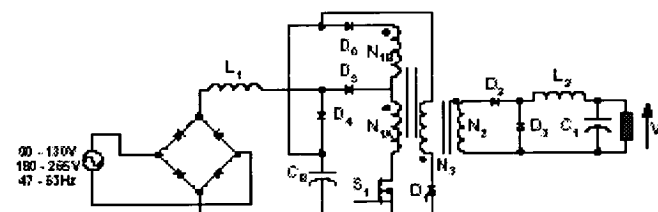
Figure 3: Bi-Forward Converter

The concept for the bi-forward, shown in figure 3 (without L_1), was initially proposed in [3] based on a flyback converter. The bi-forward was developed and improved upon in [4, 5]. The basic idea is that there are two conversion paths. One is from the input directly to the output via winding N_{1A} and is used to supply the output when the input voltage is high. When the input voltage is low (close to the zero crossings) the output is supplied from the bulk capacitor C_B via windings N_{1A} and N_{1B}. Capacitor C_B is peak charged. The percentage of energy delivered directly to the load is determined by the turns ratios between N_{1A} and N_{1B}. The converter proposed was not designed to meet class D regulations.

Improvements to the current shaping performance were suggested in [6] with the addition of an inductor L_1 after the diode bridge, which enabled the converter to meet the class D regulations with greater
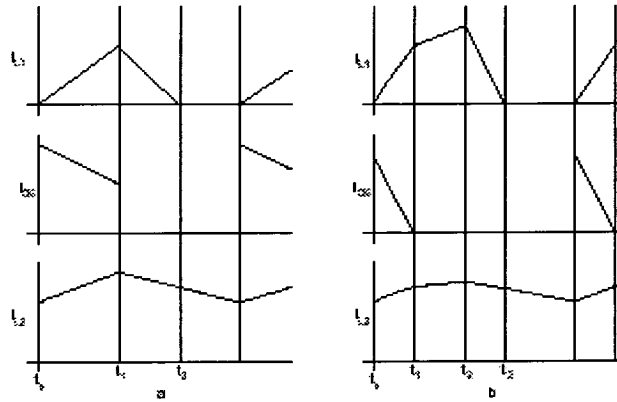
Figure 4: A: Current waveforms when input voltage is low, B: Current waveforms when input voltage is low

ease. [6] also converts the primary transformer windings into a single winding with a centre tap. This final version is shown in figure 3. The addition of L_1 changes the way the power to the output is delivered. During the zero crossings the output is supplied entirely from C_B. At low input voltages, as shown in figure 4A the device S_1 is turned on at t_0 and the current in L_1 ramps up from zero. This current also flows in N_{1A} of the transformer suppling the output. This is topped up by supplying the remaining output power from the capacitor C_B via diode D_6 and both parts of the transformer primary. $I_{L2} = (N_{1A}/N_2) \times I_{L1} + ((N_{1A} + N1B))/N_2 \times I_{D6}$. As the voltage across L_1 is small the current never rises high enough to supply the output on its own. At t_1, S_1 is turned off and the current in L_1 is discharged into C_B until t_2.

In figure 4B the input voltage is high. The current in L_1 ramps up quickly from t_0 when S_1 is turned on. Again the output current is topped up by current from C_B. At t_1 the current in L_1 equals the current in L_2 (seen through the transformer) and the two connect in series supplying the complete output power directly from the input. At t_2 S_1 is turned off and L_1 discharges into C_B until t_3. In [6] there is a third operation stage where L_1 goes into CCM, but the converter that was built for this investigation does not operate in this mode. The expected input current shape is shown in figure 5 which was measured when the converter was operating at 130V input.
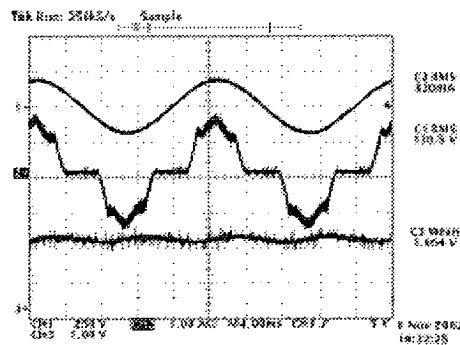
Figure 5: Measured half load input voltage (top), input current (middle) and bulk capacitor voltage (bottom) at 130V input for the bi-forward circuit

239

This topology is attractive as it maintains the voltage on C1 at a reasonable level close to the peak of the mains and as PFC is achieved as a consequence of supplying the output directly from the line input. A further advantage is the small number of additional components required: three diodes, a small inductor and a redesigned transformer primary to include a centre tap. No additional control circuitry is necessary.

Current-Source Single-Stage PFC Converter (CS S²PFC)
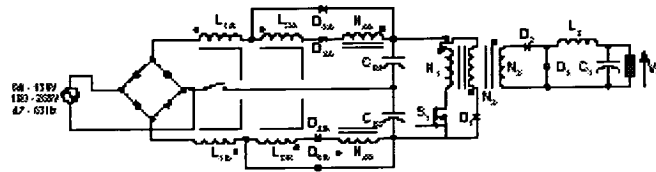
Figure 6: Forward Based CS S²PFC Converter with Voltage Doubler Input

The basic scheme for the CS S²PFC converter without voltage doubling was introduced in [7, 8]. The scheme is the practical implementation of a loss free resistor and a voltage source. The voltage doubler scheme is added in [9] and the complete converter is shown in figure 6. When the switch is open the A side is in series with the B side and is operated off the high voltage range. When the switch is closed the two sides work independently and the converter is supplied from the low voltage range. When S_1 is turned on there is already a current flowing in L_1. A negative voltage is applied across N_4, causing the current in L_D to rise (at the same time current in D_5 falls). When the current in L_D reaches the current in L_1 the two connect in series and all the current flows in the L_D path. When S_1 is turned off the current in L_D starts to fall and the current in L_1 commutates back into D_5 (L_D path and the D_5 path share current until the current in L_D reaches zero). This procedure reduces the duty ratio seen by L_1 and so helps to keep the voltage on the bulk capacitors reasonably low at about 400V at light load.

The advantages of this topology are that the voltage on the bulk capacitors remains reasonable over a wide power range and it produces an acceptable input current waveform. Also the voltage doubler input allows the transformer to operate with a narrow primary voltage range. The CS S²PFC converter is also shown to be promising in [10] where it is compared to a CCM boost pre-regulator scheme at 450W.

Experimental Circuit Specification

To enable the comparison to be carried out the two single-stage topologies, the bi-forward and CS S²PFC, as well as a conventional forward with either a passive or active-boost pre-regulator have been tested. The test circuits were developed using a mixture of analysis to determine values for key circuit parameters and simulation to verify operation. The specifications for the test circuits are:

- Up to 150W output at 5V 20A and 12V 4A.

- Input supply is both the 90 to 130V and 180 to 265V ranges.

- Ability to conform to IEC1000-3-2 class D from 75W input to full load input power (when supplying 150W output).

- Circuits are as similar as possible.

In the passive PFC and two stage PFC circuit the values of the key forward converter components are: transformer N_1, N_3 - 44 turns, N_2 5V output - 5 turns, N_2 12V output - 7 turns; Semiconductor

devices S_1 - MOSFET 900V; D_2, D_3 5V output - 100V 20A Schottky diodes; D_2, D_3 12V output - 400V 8A diodes. The passive filter for the passive PFC circuit consists of C_{B1}, C_{B2} - 330μF 250V and a 9mH per winding(L_{1A} or L_{1B}) PFC inductor on an iron laminated E142 core. The boost pre-regulator consists of C_B - 100μF 450V; L1 - 1mH; S_2 - MOSFET 500V; D_4 - 600V 8A.

The differences in the bi-forward are N_{1A}, N_{1B}, N_3 - 22 turns; S_1 - MOSFET 1200V; D_2, D_3 5V output - 200V 20A diodes; C_B is made up from two 330μF 250V capacitors connected in series; with additional components D_4, D_5, D_6 -1000V 8A diodes and L_1 - 20μH. The differences in the CS S^{2}PFC are N_2 5V output - 3 turns; N_2 12V output - 7 turns; S_1 - MOSFET 1000V; with additional components L_{1A} and L_{1B} - 100μH each on the same core; L_{DA} and L_{DB} - 40μH each on the same core; D_{4A}, D_{4B}, D_{5A}, D_{5B} - 1000V 8A diodes; additional transformer turns N_{4A}, N_{4B} - 11 turns.

All circuits are operated at a switching frequency of 100kHz.

Normally the boost pre-regulator, bi-forward and the CS S^{2}PFC would require a filter on the input to remove switching frequency noise, but since the test circuits are being operated from a transformer isolated AC source, the transformer and a 1μF on the DC side of the diode bridge rectifier is used instead. The two single stage topologies also have a RCD snubber across the MOSFET to reduce turn off losses.

Design Considerations

The following considerations were used to design the single stage converters. The basic forward converter design from above was used as the start point for the designs.

Bi-Forward

The bi-forward design was initially produced for the version of the converter without L_1 (this was to see if that version was able to meet the regulations, L_1 was added after it was confirmed the circuit would not comply). Transformer primary turns N_1 for the forward converter is 44. This was split in half so that $N_{1A} = N_{1B} = N_3 = 22$ turns (simulation in PSpice was used to confirm that this design would produce a reasonable input current). This design means that the change over between direct power transfer from the supply and the bulk capacitor occurs when the input is at 163V (input voltage 230V) or 188V when operating of 265V mains. This gives a total voltage of about $3 \times 375V = 1125V$ (peak of the mains at 265V input) across the MOSFET during transformer reset requiring the use of a 1200V device. When supplying the output directly from the mains the voltage seen across the freewheel diode D_3 is $N_3/N_{1A} \times 375V = 85V$. This is high, so it was decided to use 200V normal diodes for the 5V output for safety, instead of the 100V schottky diodes as used for the forward converter. This will increase loss. The maximum voltage seen across D_4 and D_6 is the bulk capacitor voltage, about 375V (during the zero crossings). The maximum voltage seen by D_5 is $2 \times V_{CB}$ when the input voltage is zero giving about 750V. Due to this high voltage on D_5 1000V 8A diodes were used for all three. Using these over rated diodes will not have much effect on cost or efficiency. From a cost point of view the high voltage MOSFET is a key factor and the use of normal diodes on the 5V output is a key factor from an efficiency point of view.

CS S^{2}PFC

To allow L_D to have enough time to ramp up to the current in L_1 the turns on the transformer secondaries were reduced to 3 turns on the 5V output and 7 turns on the 12V output so as to increase the duty cycle. The voltage across C_{B1} and C_{B2} is expected to be about 420V at worst, hence the MOSFET will need to be rated for at least twice that, 850V, a 1000V device was used. The possible voltage across the D_5s is the bulk capacitor voltage of about 420V. The voltage on the D_4's is $V_{CB} + V_{CB} \times (N_{4A}/N_1)$, which is about 525V. Since 1000V diodes were already available these were used for D_{4A} through to D_{5B}. L_D was chosen following the method set out in [9] which produced a value of 25μH, this was increased to 40μH from experimentation. L_1 was set to 100μH.

The boost pre-regulator was developed following an Unitrode application note [11] and the passive filter inductor was taken from a 150W commercial power supply.

Comparison of Results
Harmonic Content

Shown in figures 7A, 7B, 7C and 7D is the harmonic content for the four circuits at 230V and 100V at full load input power, and 230V and 100V at 75W input power. At full input power all four circuits pass at both voltages, but at 75W the CS S^2PFC circuit exceeded the regulation limits from the 5th to 13th harmonics at 230V input and on the 7th and 9th harmonic at 100V input. The lowest input power at which the CS S^2PFC circuit complied was at 100W input power at 230V and at 97W input power at 100V input. The two stage circuit passes each harmonic with very low harmonic current, whereas the other topologies are much closer to the harmonic limit.
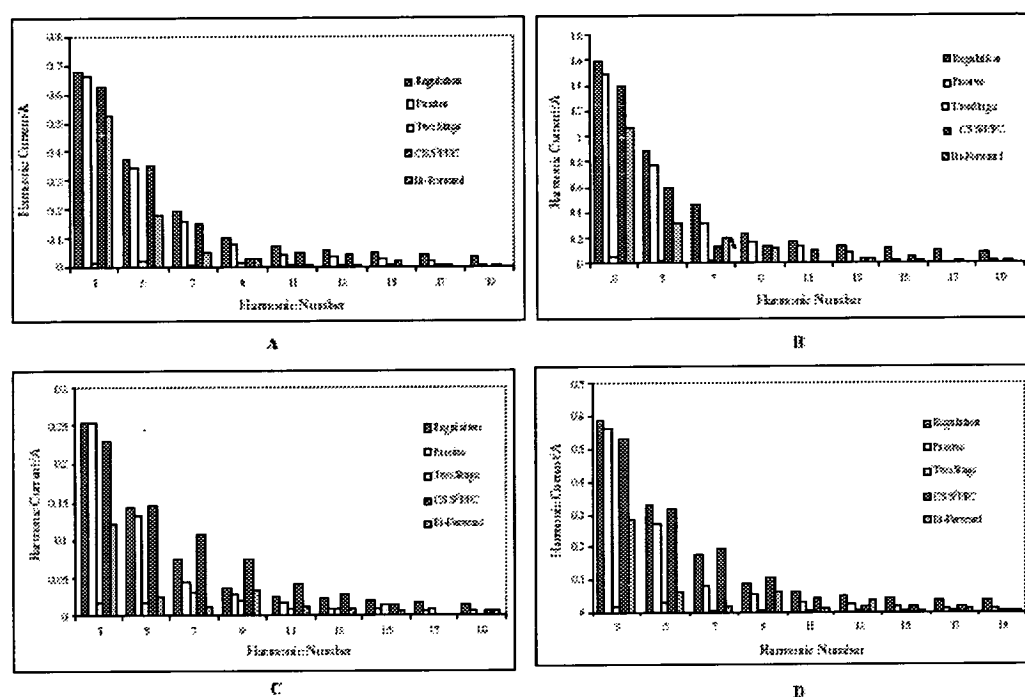
Figure 7: A: Harmonic content at full load (about 198W) input power at 230V, B: Harmonic content at full load (about 203W) input power at 100V, C: Harmonic content at 75W input power at 230V, D: Harmonic content at 75W input power at 100V.

Current Waveform

In figures 8A, 8B, 8C and 8D are shown the input current waveforms at 230V and full power. As can be seen the current waveform does not have to be particularly sinusoidal to pass the class D regulation. The two stage with boost converter pre-regulator has the best current shape, shown in figure 8B, which is almost sinusoidal. The passive solution, shown in figure 8A has quite a narrow conduction angle and as can be seen is suffering from a subharmonic oscillation. Even with this it still passes the regulations. The CS S^2PFC waveform is shown in figure 8C and is again showing a fairly narrow conduction angle. It is also possible to see the different conduction modes of the input current mentioned in [9]. The DCM part is at the beginning and end of the current waveform where the slope is shallow and the CCM part is the main part of the waveform. The bi-forward input current waveform is shown in 8D

242

and has a wider conduction angle. The waveform is slightly triangular in shape. This was different to what was expected. The current waveform shown in figure 5 is similar to the waveshape predicted for the inductor smoothed bi-forward: as power and voltage increased the waveshape became more triangular, but the converter was still able to meet the class D regulation. The reason for the change in shape is that reflected secondary current seen by N_{1A} is quite high (6-7A) at higher powers and at high voltage the duty is very narrow. This meant that the current in L_1 was not able to reach the reflected load current, hence the change in shape.

A

B

C

D
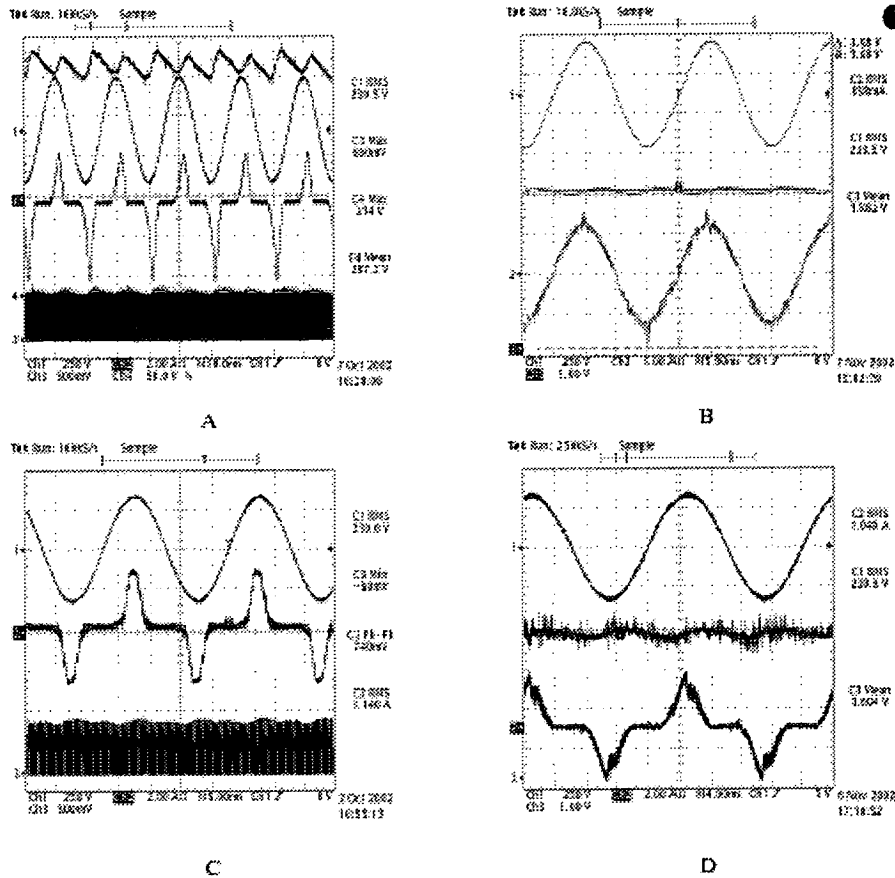
Figure 8: A: Measured full load bulk capacitor voltage top trace, input voltage (2nd from top), input current (3rd from top) and voltage drain source of the MOSFET (bottom) at 230V input for passive filter circuit, B: Measured full load input voltage (top), input current (bottom) and bulk capacitor voltage (middle) at 230V input for the two stage circuit, C: Measured full load input voltage (top), input current (middle) and gate drive signal (bottom) at 230V input for CS S²PFC circuit, D: Measured full load input voltage (top), input current (bottom) and bulk capacitor voltage (middle) at 230V input for the bi-forward circuit.

Efficiency

Figures 9A and 9B show the efficiency of the four converters across a wide output power range from about 37W output to 150W output for input voltages of 115V and 230V. The passive filter PFC and forward converter shows the best efficiency of around 80% for both voltages. The CS S²PFC and the two stage are both showing efficiencies of about 75%. This result confirms the result from [10] that

243

the CS S^{2}PFC and the two stage will have similar efficiencies. The bi-forward is showing an efficiency of about 70%. The reason for this is the use of standard diodes on the 5V output instead of schottky diodes which are used in the other circuits. The reason for using normal diodes was explained in the design considerations section. If schottky diodes could be used in a future design the efficiency would be comparable with the CS S^{2}PFC and two stage approach. It is worth remembering that the two single stage topologies are fitted with RCD snubbers to reduce MOSFET turn off losses.

A   B
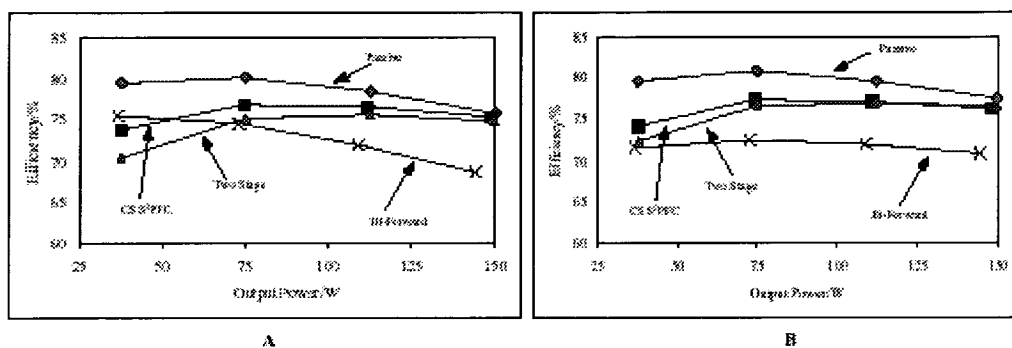
Figure 9: A: Measured efficiency with input voltage at 115V, B: Measured efficiency with input voltage at 230V.

Bulk Capacitor Voltage

In figure 10 the variation of voltage across the bulk capacitors as the power increases is shown. The two stage bulk capacitor voltage stays virtually constant in a 10V range between 395V and 385V, showing a small decrease as the converter is loaded up. The passive PFC has the lowest bulk capacitor voltage range from 366V at light load to 355V at full load. This variation happens as the resonant circuit conditions between L_1 and C_{B1} and C_{B2} change as the load increases. The CS S^{2}PFC voltage ranges from 408V at light load to 376V at full load which is close to expectation. The bi-forward has a voltage of about 386V from virtually no load to 37W output; the voltage then jumps to 426V at half power reaching a maximum of 430V at 3/4 of full load falling slightly at full load. The bulk capacitor voltage for the bi-forward was expected to stay close to the peak of the mains at about 380V. This is due to the same reason as explained in the current shape section. An alternative design with N_{1A} set to 32 turns and N_{1B} set to 12 turns was also tried out. This design did have bulk capacitor voltage close to the peak of the mains at 330V when operating with a 230V input, but it did not meet all of the harmonic tests.
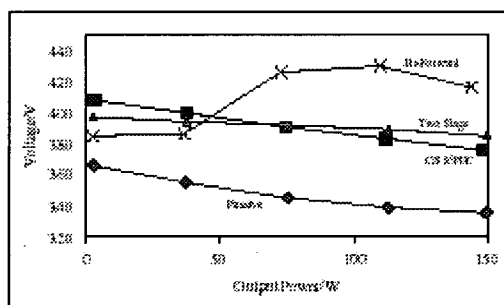
Figure 10: Measured bulk capacitor voltage with input voltage at 265V

Component Stress

Shown in table I are the measured voltage stresses for the MOSFETS and diodes. The voltage on the switches in the bi-forward is lower than expected as the MOSFET snubber circuits were resetting the transformer instead of the tertiary winding. The snubber circuit was also resetting the transformer in the CS S^2PFC. The 5V diode voltage for the bi-forward is slightly higher than expected (85V) since the bulk capacitor voltage is higher than expected.

Device	Bi-forward	$CS\,S^2PFC$
S_1	830	850
5V diodes	100	29

Table I: Voltage stress on key semiconductor components

Cost

Shown in table II is the normalised cost of the four converters, the passive with forward converter is the base value at one, the rest are compared to this.

Converter	Cost
Passive	1
Boost	1.39
CS S^2PFC	1.46
Bi-Forward	1.455

Table II: Costs of the converters compared to the passive filtering with forward converter

The passive solution came out cheapest, with the boost converter second even with all those extra components. The two single stage topologies are about the same and are the most expensive. The main reason they are the most expensive is that they both have high voltage MOSFETs (1000V and 1200V compared to the 900V device in the forward converter). If RCD snubber transformer reset is used instead of tertiary winding reset then the same MOSFET as in the normal forward converter could be used and there cost would be comparable to the passive with forward converter method.

Conclusion

From the results it seems that the passive with forward converter has the best efficiency and lowest cost and is able to meet the class D regulations. The boost pre-regulator scheme is most likely to complicated for a 150W power level. The two single stage topologies have come out worse being the most expensive, the bi-forward least efficient and the CS S^2PFC not able to meet the regulations over a wide power range. If the two single stage topologies were built using snubber transformer reset and with minor redesign to keep capacitor voltage lower they would most likely start being competitive with the passive with converter solution. Single stage topologies with the improvements are also better suited to applications where compliance with the regulations is only required at certain power and not a wide power range.

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245

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246

A NEW SINGLE-STAGE PFC CONVERTER BASED ON THE FORWARD CONVERTER WITH A LOW FREQUENCY SWITCH

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Abstract

In this paper a new single-stage PFC topology, to meet IEC 61000 -3-2, based on the forward converter with a low frequency switch is presented. The proposed converter is simple and suffers from lower component stresses than other single-stage PFC converters. Due to this it is expected that the converter will operate with higher conversion efficiency and lower cost. The harmonic content of the input current, efficiency and component stress are investigated.

1 Introduction

In recent years many new so-called single-stage PFC topologies have been introduced. The aim of these converters is to meet IEC 61000 -3-2 and supply the output load with good output voltage regulation in a single power stage. These types of converter are intended for low/medium power supplies.

One of the more promising topologies is the bi-forward introduced in [1], but this could only meet the class A part of the regulations. Also it suffers from high voltage and current stress (when compared to a forward converter) on the the mains switch possibly requiring the use of a MOSFET rated up to 1200V. Such a highly rated device is required when using tertiary winding transformer reset as the primary winding in the transformer is centre tapped, hence during reset three times the bulk capacitor voltage will be seen across the switch if all three windings have the same number of turns. In [3] an inductor was added onto the front end of the converter, which enabled it to pass the class D regulations, but in [2] this was shown to suffer from high voltage stress on the bulk capacitor and main switch.

To try and improve on this poor voltage and current stress performance a new converter topology, shown in figure 1, is pro-
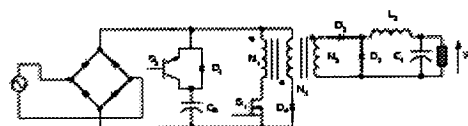
Figure 1: Forward converter with additional low frequency switch in series with the bulk capacitor. S_2 can also be an IGBT.

posed in this paper using a low frequency switch added onto a forward converter. The aim of the low frequency switch (or the additional transformer winding in [1]) is to provide a method of releasing energy stored in CB to the output when the input voltage is low. This converter should have the same ability to meet IEC 61000 -3-2 as the bi-forward in [1] and only meet class A.

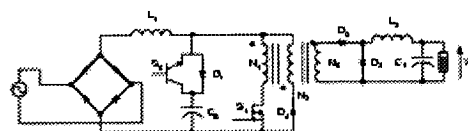Figure 2: Forward converter with additional low frequency switch in series with the bulk capacitor and an input inductor. S_2 can also be an IGBT.

Figure 2 shows the proposed converter with additional input inductor L_1. This version is expected to meet class D.

2 Operation

2.1 Operation of Low Frequency Switch S_2

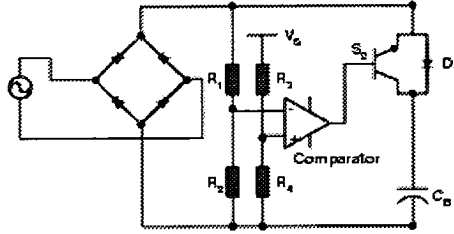Switch S_2 is turned on and off by a comparator looking at the

Figure 3: Control of the low frequency switch using a simple comparator

input voltage of the converter as shown in figure 3. When the input voltage is low, S_2 is on and the output is supplied completely from C_B. Switch S_1 is switching at a high frequency (e.g. 100kHz), and high frequency current pulses flow through S_2, but S_2 stays on all the time. When the voltage at the input rises above the voltage set for the comparator, S_2 will turn off. The output load is now supplied directly from the line. The duty cycle for S_1 will reduce as the line voltage rises to keep the output voltage constant.

2.2 Operation of the Converter with Input Inductor L_1

If L_1 is not fitted the bulk capacitor C_B is peak charged in the normal manner of a capacitor smoothed diode bridge rectifier and the converter draws the same shape current as the bi-forward in [1]. With the addition of L_1 the recharging of C_B is spread out across the whole period that S_2 is turned off. Figure 4 shows the current waveform for L_1 operating in discontinuous conduction mode (DCM) with L_2 operating in continuous conduction (CCM), during the off period of S_2. L_1 could also be operated in CCM.

At t_a S_1 is turned on, the full line voltage is applied across L_1 and the current ramps up. At t_b the current in L_1 reaches the reflected current in L_2 and the two inductors connect in series through the transformer and energy is transferred to the secondary side of the circuit. At t_c S_1 is turned off and L_1 discharges into C_B until t_d when the current in L_1 reaches zero.

3 Design Considerations

3.1 Basic Converter

The main design parameter for setting the conduction time of the input current and the magnitude of the bulk capacitor recharging current is the turn on and off voltage of switch S_2. Another is the turns ratio of the transformer which will deter-
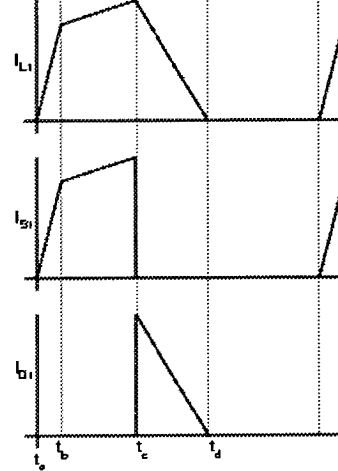
Figure 4: Current in L_1, S_1 and D_1 for one switching cycle

mine the voltage and current stresses in key components and the duty cycle.

The minimum voltage V_{S2min} that S_2 can be properly operated is

$$V_{S2min} = \frac{N_1 \cdot V_o}{N_2 \cdot D_{max}} \qquad (1)$$

where D_{max} is the maximum duty cycle (normally 0.5 for a forward converter).

Figure 5 shows how the duty cycle of the converter changes over a half line cycle. Where the plot is flat the output is supplied from C_B and the curved part is where the output is supplied direct from the line. It is noted that there is a jump in the duty cycle at the switching of S_2, due to a sudden change in voltage seen at the transformer, which the converter's controller has to respond to quickly to keep the output voltage in regulation. In figure 5 the turn on and off voltage is 140V; if the turn on and off voltage is increased the jump in duty cycle will be reduced as the difference between bulk capacitor voltage and input voltage at turn on and off is reduced.

Figure 6 shows that as the turn on and off voltage for S_2 increases input current conduction angle decreases. This can be translated to give an indication of the filtered input current shape as shown in figures 7 and 8.

248
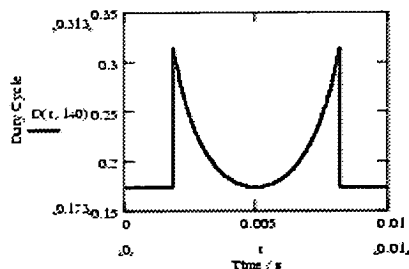
Figure 5: Duty cycle variation over a line half cycle for a turn on and off voltage of 140V for S_2
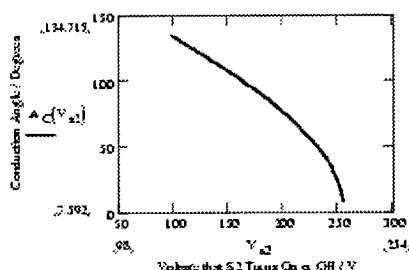
Figure 6: Conduction angle of the input current as the turn on and off voltage of S_2 increases

In figure 7 where the input current conduction angle is long (113°) the conduction angle for supplying the output from the bulk capacitor is low (67°) which reduces the peak of the bulk capacitor recharging current. When the turn on and off voltage is high (200V) as in figure 8 the input current conduction angle is reduced (76°) and the bulk capacitor supplies the output for longer making the peak of its recharging current higher.

3.2 Converter with Input Inductor L_1

In addition to the considerations for the basic converter the effect of adding inductor L_1 needs to be considered. Figure 9 shows how various parts of the duty cycle change over a half line cycle when the converter is supplied from the line input.

One of the effects of adding inductor L_1 is that the bulk capacitor C_B is no longer peak charged and hence the voltage requires analysis to predict its average value. Figure 10 shows how the calculated bulk capacitor voltage varies. The voltage rises as the output power increases.

Figure 11 shows the predicted current shape for a turn on and
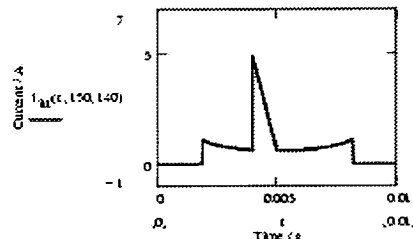
Figure 7: Input current waveform for 150W with S_2 turned on and off at 140V
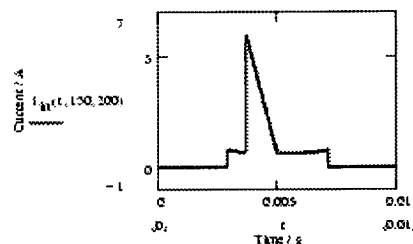
Figure 8: Input current waveform for 150W with S_2 turned on and off at 200V

off voltage for S_2 of 230V and L_1 as 20μH. Compared to figures 7 and 8 the waveform is smoothed out and more balanced about the centre of the time period. The peaks at the ends of the waveform in figures 7 and 8 will appear if the turn on and off voltage of S_2 is reduced.

3.3 Driving of Switch S_2

The switch S_2 can be driven using several different methods, such as using a level shift IC, gate pulse transformer or opto-isolator with an independent power supply. The use of a separate power supply is not a problem as most converters in practice have an auxiliary power supply to power items such as the control circuits. For the prototype converter presented in the next section switch S_2 is driven using a signal level shift IC and a bench supply to power the floating side to represent an auxiliary power supply.

4 Experimental Verification

A prototype converter with the following specifications has been built and tested.

• Output power 150W

249
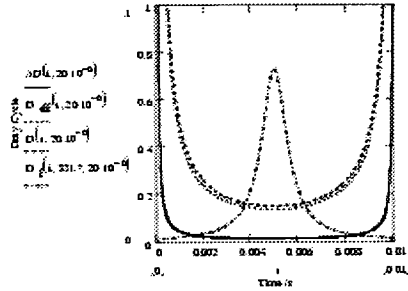
Figure 9: Variation of duty cycle for S_2 turned on and off at 230V with L_1 as 20μH. ΔD is the duty for the period t_a to t_b, D_{eff} is the duty for the period t_b to t_c, D is the overall on duty for S_1 from t_a to t_c and D_f is the discharge duty for L_1 from t_c to t_d.
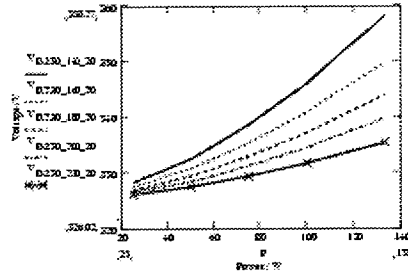
Figure 10: Variation of bulk capacitor voltage with load, for different turn on and off voltages for S_2 of 140V, 160V, 180V, 200V and 230V (L_1 as 20μH)

● Output voltage and current 5V, 0A-20A

● Input voltage 180V-265V

The key component values are; for the transformer $N_1 = N_3 = 44$ and $N_2 = 5$; the inductors $L_1 = 20\mu$H and $L_3 = 15\mu$H. The switch S_1 is a MOSFET rated for 900V and S_2 is an IGBT rated for 500V. The diodes D_2 and D_3 are schottky diodes.

The prototype converter can be configured with or without the input inductor L_1, and the input voltage at which S_2 turns on and off can be adjusted using a variable resistor on the positive input voltage divider of the comparator. The following set ups were tested;
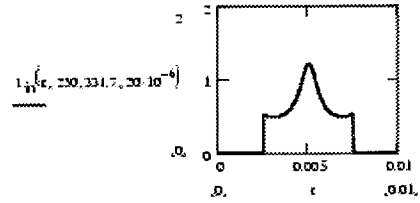
Figure 11: Input current waveform for 100W with S_2 turned on and off at 230V with L_1 as 20μH

● S_2 turn on/off voltage at 230V, and with L_1

● S_2 turn on/off voltage at 230V, and without L_1

● S_2 turn on/off voltage at 140V, and without L_1

On the input of the prototype converter a filter formed from a 1.14mH inductance and 1mF capacitance have been added to filter out the discontinuous switching frequency current pulses.

4.1 Harmonic Content of Input Current

Figure 12 shows the input RMS current harmonic levels for the odd harmonics up to the 19th harmonic compared to class A. The even harmonics for all three converters was very low and hence they are not shown. All three versions of the converter passed all the class A limits by a wide margin as figure 12 shows.
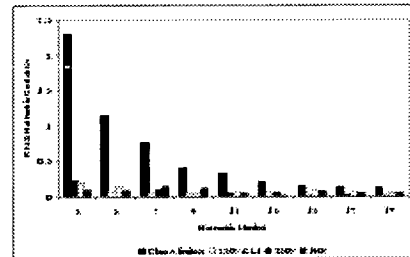
Figure 12: Input current odd harmonics up to the 19th harmonic for the three converter variations compared to the class A limits

Figure 13 shows the input RMS current harmonic levels for the odd harmonics up to the 19th harmonic compared to class D for an input power of 127W. The harmonics for the two versions without L_1 are shown to compare them to the version with L_1.

250

The converter with the turn on and off of S_2 as 140V fails class D on the 7th, 11th, 15th, 17th, 19th, 23rd and 29th harmonics and the version with a S_2 turn on and off at 230V failed class D on the 11th, 13th, 15th, 17th, 19th, 21st, 23rd, 25th, 27th and 29th. Once L_1 has been added to the version with a S_2 turn on and off voltage at 230V the converter only fails class D on the 13th and 23rd harmonics. Further investigation is needed to reduce the level of the 13th harmonic (harmonics above the 21st are allowed to exceeded the regulation value by 50% if certain other conditions are met). This maybe achieved by increasing the size of L_1 and/or changing the turn on and off voltage of S_2.
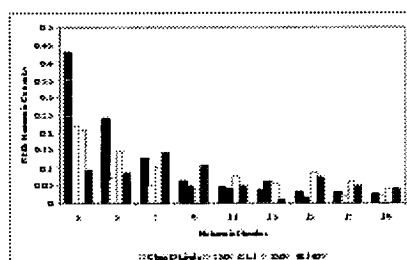
Figure 13: Input current odd harmonics up to the 19th harmonic for the three converter variations compared to the class D limits for an input power of 127W

The addition of even a small inductance (only 20μH was added) on the front end of the converter reduces the levels of the current harmonics quite considerably. The inductance is just extending the conduction time of each switching cycle by adding the charging and discharging of itself on to the current being transferred to the output flowing through L_1.

4.2 Input Current Waveforms

Figure 14 shows the filtered input current waveform for the converter with L_1 and a turn on and off voltage for S_2 of 230V, and figure 15 shows the same converter, but without L_1. The current waveform in figure 14 is smoother than that in figure 15 and does not suffer from rises in current close to turn on or off to the same extent. Figure 16 where turn on or off is 140V shows this effect more clearly. Also the peak part of the waveform is more spread out when L_1 is fitted. Figure 16 when compared to the waveform drawn by the bi-forward is very similar in shape.

4.3 Efficiency and Component Stress

Figure 17 shows the efficiency for the converter with S_2 turn on and off voltage at 230V with L_1 and figure 18 shows the efficiency for the converter without L_1 with a S_2 voltage of 140V.
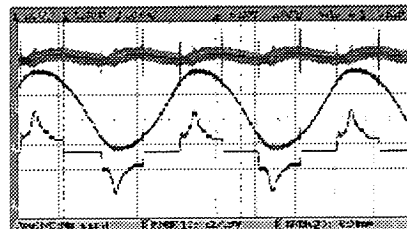
Figure 14: Input current with L_1 and a turn on and off voltage for S_2 of 230V. Top trace: bulk capacitor voltage, middle trace: input voltage and bottom trace: input current.
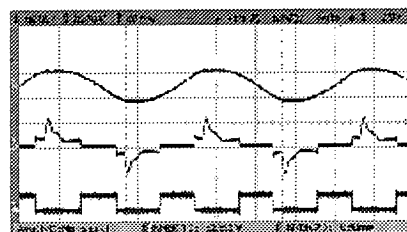
Figure 15: Input current without L_1 and a turn on and off voltage for S_2 of 230V. Top trace: bulk capacitor voltage, middle trace: input voltage and bottom trace: output voltage from comparator.

The measured efficiency is reasonable being around about 77% at full load and normal input voltage of 230V for both versions of the converter with and without L_1. This could be improved with optimisation of the converters.

The inductor L_1 acts like an inductor in a boost converter raising the bulk capacitor voltage above the input voltage. Unlike a boost converter the bulk capacitor voltage is uncontrolled. Figure 19 shows how the bulk capacitor voltage varies with output power for the maximum input voltage available from the test supply. Analysis carried out predicts the peak voltage across C_B to be 394V when operating from a 265V input. This value is acceptable, being similar to that typically seen on the bulk capacitor in a PFC boost pre-regulator. In the versions without L_1 the bulk capacitor is only ever charged up to the peak of the supply voltage.

The bulk capacitor voltage rises as the output power increases. This is the opposite to most single-stage PFC topologies with a boost style inductor where the voltage on the bulk capacitor rises increases at low power. The bulk capacitor voltage
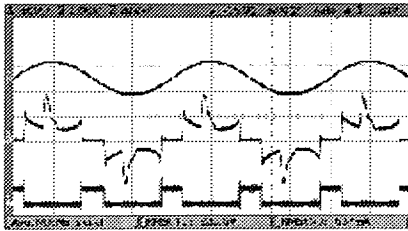
Figure 16: Input current without L_1 and a turn on and off voltage for S_2 of 140V. Top trace: input voltage, middle trace: input current and bottom trace: output voltage from the comparator
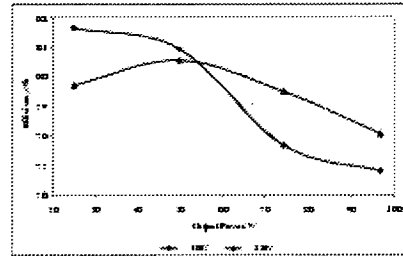
Figure 18: Efficiency across the output power range without L_1 fitted and a turn on and off voltage for S_2 of 140V
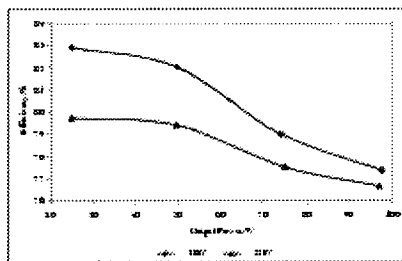

Figure 17: Efficiency across the output power range with L_1 fitted and a turn on and off voltage for S_2 of 230V
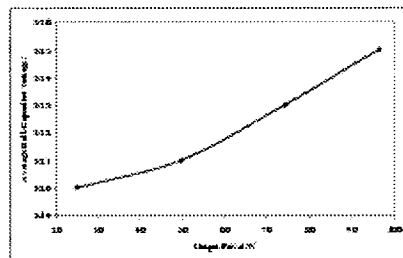
Figure 19: Bulk capacitor voltage measured with an input voltage peak of 313V for the converter with L_1

changes so as to balance the energy in and out of the capacitor over a half line cycle.

5 Conclusions

A single-stage PFC topology with a simple operation has been presented. The converter will pass class A and is very close to passing class D with an input inductor fitted. The converter has a reasonable bulk capacitor voltage and efficiency. The converter could be used instead of passive filtering, reducing weight and volume of a power supply.

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