THE UNIVERSITY
of EDINBURGH

This thesis has been submitted in fulfilment of the requirements for a postgraduate degree (e.g. PhD, MPhil, DClinPsychol) at the University of Edinburgh. Please note the following terms and conditions of use:

This work is protected by copyright and other intellectual property rights, which are retained by the thesis author, unless otherwise stated.
A copy can be downloaded for personal non-commercial research or study, without prior permission or charge.
This thesis cannot be reproduced or quoted extensively from without first obtaining permission in writing from the author.
The content must not be changed in any way or sold commercially in any format or medium without the formal permission of the author.
When referring to this work, full bibliographic details including the author, title, awarding institution and date of the thesis must be given.

Development of a High Temperature Sensor Suitable for Post-Processed Integration with Electronics

Aleksandr Tabasnikov

A thesis submitted for the degree of Doctor of Philosophy
The University of Edinburgh
2016

Declaration of originality

I declare that this thesis has been composed by me, the work is my own, and it has not been submitted for any other degree or professional qualification. Research recorded was carried out by me except as specified below:

X-ray diffraction measurement results obtained using X-ray diffractometer Siemens D5000 were collected by Richard Yongqing Fu and his students Jimmy Zhou and Chao Zhao at the University of West of Scotland. Measurement results are analysed in section 4.4.6 of Chapter 4 and have been jointly published in 2014 (DOIs: 10.1109/ICMTS.2014.6841491).

Aleksandr Tabasnikov

Abstract

Integration of sensors and silicon-based electronics for harsh environment applications is driven by the automotive industry and the maturity of semiconductor processes that allow embedding sensitive elements onto the same chip without sacrificing the performance and integrity of the electronics. Sensor devices post-processed on top of electronics by surface micromachining allow the addition of extra functionality to the fabricated ICs and creating a sensor system without significant compromise of performance. Smart sensors comprised of sensing structures integrated with silicon carbide-based electronics are receiving attention from more industries, such as aerospace, defense and energy, due to their ability to operate in very demanding conditions.

This thesis describes the design and implementation of a novel, integrated thin film temperature sensor that uses a half-bridge arrangement to measure thin film platinum sensitive elements. Processes have been developed to fabricate temperature insensitive thin film tantalum nitride resistors which can be combined with the platinum elements to form the temperature transducing bridge. This circuit was designed to be integrated with an existing silicon carbide-based instrumentation amplifier by post-CMOS processing and to be initially connected to the bond pads of the amplifier input and output ports. Thin films fabricated using the developed TaN and Pt processes have been characterized using resistive test structures and crystallographic measurements of blanket thin film layer samples, and the relationship between the measurement results obtained has been analyzed.

An initial demonstration of temperature sensing was performed using tantalum nitride and platinum thin film resistor element chips which were fabricated on passivated silicon substrates and bonded into high temperature packages. The bridge circuit was implemented by external connections through a printed circuit board and the bridge output was connected to a discrete instrumentation amplifier to mimic the integrated amplifier. The temperature response of the circuit measured at the output

of the amplifier was found to have sensitivity of 844 $\mu V \cdot °C^{-1}$ over the temperature range of 25 to 100 °C.

Two integrated microfabrication process flows were evaluated in this work. The initial process provided a very low yield for contact resistance structures between TaN and Pt layers, which highlighted problems with the thin film platinum deposition process. Multiple improvement options have been identified among which removal of the dielectric layer separating TaN and Pt layers and thicker Pt film were considered and a redesign of both layout and the process flow has resulted in improved yield of platinum features produced directly on top of TaN features.

Temperature sensitivity of the integrated sensor devices was found to depend significantly on parasitic elements produced by thin film platinum step coverage, the values of which were measured by a set of resistive test structures. A new microfabrication design has enabled the production of a group of integrated temperature sensors that had a sensitivity of 150.84 $\mu V \cdot °C^{-1}$ in the temperature range between 25 and 200 °C on one of the fabricated wafers while the best fabricated batch of sensors had a sensitivity of 1079.2 $\mu V \cdot °C^{-1}$.

Lay summary

Producing sensors on silicon-based integrated circuits enables additional sensing functions on the same chip without reduction in the performance of the electronics. Silicon carbide (SiC) dramatically lifts the fundamental temperature limitation of silicon electronics (125 °C) to at least 300 °C and producing sensors with electronics based on this new material is a challenge as well as a new research area. Sensor devices fabricated on top of SiC electronics would create a sensor system able to perform in extreme conditions, and this perspective was the key motivation behind this work.

This thesis describes the design and implementation of an integrated, thin film temperature sensor based on temperature insensitive, thin film tantalum nitride (TaN) resistors and thin film platinum (Pt) temperature sensitive elements. These films as well as the insulating layers separating them were produced using production processes that would be safe to perform on SiC integrated circuits. Electrical resistance parameters, physical structure and stability of thin film Pt and TaN have been measured, and fabrication processes have been developed step by step to form a temperature transducing circuit.

The temperature sensor was demonstrated in two implementations, both of which produced sufficiently high sensitivity to temperature. The first implementation used external connections between separate TaN and Pt resistor chips, and a commercial instrumentation amplifier that was not exposed to high temperatures. An integrated bridge implementation was later produced by a microfabrication process flow that potentially enabled the sensor to be integrated with a SiC instrumentation amplifier and was measured up to 200 °C. This points the way towards future integration of sensors for extreme environments such as wind turbines, gas turbines, oil drills, geothermal wells and other demanding industrial applications.

Acknowledgments

I gratefully acknowledge the financial support by UK EPSRC through the FS/01/02/10 IeMRC Flagship Project on Smart Microsystems.

I would like to thank my supervisor Dr. Stewart Smith for supporting and guiding me through my PhD, spending days of his time on discussions of my work and initiating me to many insights of microfabrication and test. I am extremely grateful to my second supervisor Professor Anthony Walton for his advice, help and direction throughout the project and thesis write-up stages, and also for the opportunity given to me to work at the facilities and with specialists of Scottish Microelectronics Centre. My major thanks go to Stewart Ramsay, Ewan MacDonald, Richard Blair, Brian Neilson and Hugh Frizell as well as Andrew Bunting and Tom Stevenson for their immense technical help and assistance for the duration of this work. I also want to thank Jonathan Terry, Gerard Cummins, Jeremy Murray, Atif Syed, Yifan Li, Peter Lomax, Ross Walker, Evgeny Sirotkin, Ewan Blair and Ilka Schmueser for their assistance and groundwork that influenced this research.

I gladly appreciate help and communication from Richard YongQing Fu, Khelil Sefiane and their PhD students who provided the required measurement setups in critical times. I would also like to express my gratitude to the staff of electronic and mechanical workshops, School of Biological Sciences and School of Physics for their support in building parts of different experimental setups, producing experimental samples and other deliverables.

I am especially grateful to my friends and relatives for their encouragement and most importantly I would not go far without love and support from my mother, father and my wife Irina who never lost faith in me.

Table of contents

Declaration of originality II

Abstract III

Lay summary V

Acknowledgments VI

Table of contents VII

List of figures XI

List of tables XIX

Abbreviations XX

Publications XXV

1 Introduction 1

1.1 Background 1

1.2 Thesis structure 4

References 6

2 High temperature sensing technologies 9

2.1 Introduction 9

2.2 Pressure and strain sensors 11

2.2.1 Piezoelectric sensors 11

2.2.2 Piezoresistive sensors 14

2.3 Temperature sensors 16

2.3.1 Integrated circuit-based thermometers 17

2.3.2 Thermoelectric sensors: thermocouples 18

2.3.3 Thermoresistive sensors: resistance thermometers and thermistors 22

2.3.4 Infrared radiation sensors: infrared thermometers 29

2.3.5 Fibre optic sensors: fibre optic-based thermometers 34

2.4 High temperature thin film elements 39

2.4.1 Thin film material selection 40

2.4.2 Thin film tantalum nitride phase content adjustment approaches 42

2.5 Summary 44

References 47
3 Design of temperature transducer bridge 55
3.1 Introduction 55
3.2 Integrated temperature sensing system produced by post-processing 55
3.3 Resistance bridge circuit numerical analysis 58
3.3.1 Effect of specified electrical parameters 59
3.3.2 Element mismatch 64
3.3.3 Deviation from designed sensor circuit component values 70
3.3.4 Comparison with most popular types of thermometer 73
3.4 Conclusions 74
References 76
4 Development of thin film materials 77
4.1. Introduction 77
4.2. Crystallographic measurements 78
4.2.1 Motivation 78
4.2.2 Basic features of XRD measurement 80
4.2.3 Experimental setup and sample fabrication 83
4.2.4 Example measurements 83
4.3 Electrical measurements 85
4.3.1 Measurement basics 86
4.3.2 Test structures for electrical thin film characterization 89
4.3.3 Experimental setup 90
4.4 Development of tantalum nitride process 93
4.4.1 Introduction 94
4.4.2 Preparation and characterization of initial tantalum nitride samples 95
4.4.3 Thin film tantalum nitride patterning 96
4.4.4 Environment- and temperature-related effects on thin films 98
4.4.5 Phase content control and characterization 102
4.4.6 Summary of results 111
4.5 Development of platinum process 111
4.5.1 Introduction 112
4.5.2 Thickness-related issues 112

4.5.3 Adhesion layer for thin film platinum 116
4.5.4 Summary of results 120
4.6 Conclusions 120
References 123
5 Development of integrated temperature transducer bridge 129
5.1 Introduction 129
5.2 Hybrid bridge-based temperature sensor 130
5.2.1 Fabricating and combining elements into a bridge 130
5.2.2 Experimental setup 133
5.2.3 Demonstration of temperature sensing capabilities 135
5.2.4 Conclusions 138
5.3 Integrated bridge-based design 139
5.3.1 Integrated sensor device design 139
5.3.2 Supplementary test structure design 144
5.4 Fabrication 147
5.5 Measurement setup and results 157
5.5.1 Experimental setup 157
5.5.2 Test structure measurement results 159
5.5.3 Conclusions 162
5.6 Temperature sensitive layer improvement options 163
5.7 Conclusions 165
References 167
6 Integrated bridge improvement and results 169
6.1 Introduction 169
6.2 Design improvements 170
6.2.1 Improvement of sensor design elements 170
6.2.2 Test structures to characterize additional resistive elements 172
6.2.3 Optimization of microfabrication processes 177
6.2.4 Test design improvements 178
6.3 Fabrication 181
6.4 Measurement results 188
6.4.1 Step coverage resistance measurements 189

6.4.2 Contact resistance measurements using TLM and chain structures........194
6.4.3 Contact resistance measurements using CBKR structures......................196
6.4.4 Sensor measurements 197
6.5 Conclusions 209
References 212
Chapter 7 Conclusions and further work 213
7.1 Summary of results..213
7.2 Conclusions 214
7.2.1 High temperature thin film materials 214
7.2.2 High temperature sensors produced from thin films 216
7.3 Future work 218
7.3.1 Solution of platinum sidewall coverage problem...................................218
7.3.2 Improvement of thin film electrical parameters 220
7.3.3 An outline fabrication process for integration on SiC electronics 221
7.4 Final conclusions...223
References 224
Appendix A Runsheets of initial microfabrication process flow 225
Appendix B Runsheets and measurement results of devices produced by improved microfabrication process 231

List of figures

Figure 2.1.1 Illustration of temperature distribution in multilayer solid acting as a source of heat that is transferred by different mechanisms 9

Figure 2.2.1 Illustration of piezoelectric effect 12

Figure 2.2.2 a) Schematic layout of a strain sensor; Schematic construction of pressure sensor: b) side-view illustration, c) top-view layout 16

Figure 2.3.1 Illustration of thermoelectric effect 19

Figure 2.3.2 Illustration of thermoelectric measurement circuit using conductors from three different materials 19

Figure 2.3.3 Insulated and sheathed thermocouple construction example................ 21

Figure 2.3.4 Simplified construction of platinum resistance thermometer probes .. 25

Figure 2.3.5 Simplified construction of platinum resistance thermometer devices.. 25

Figure 2.3.6 Wheatstone bridge used to measure temperature sensitive elements ... 26

Figure 2.3.7 Four-wire connection used to measure RTD element 26

Figure 2.3.8 Examples of linearization circuit effects on sensitivity of temperature response.. 29

Figure 2.3.9 Schematic construction of automatic pyrometer 33

Figure 2.3.10 Typical arrangement of Fabry-Perot fibre thermometer..................... 37

Figure 2.3.11 Example spectrometric distributed thermometer sensing and detection diagram 39

Figure 3.2.1 Full-scale deviation from linear response produced by a Wheatstone bridge circuit measuring a single RTD element 57

Figure 3.2.2 Bridge with two RTD elements used as a temperature transducing circuit 57

Figure 3.3.1 Expected full-scale temperature response for different resistor ratios . 60

Figure 3.3.2 Reference sensor output against designed resistor ratio 61

Figure 3.3.3 Temperature sensitivity against designed resistor ratio........................ 61

Figure 3.3.4 Full-scale deviation from linear response at different temperatures.....62
Figure 3.3.5 Expected temperature sensitivity against designed resistor ratio..........63
Figure 3.3.6 Full-scale deviation from linear response at different temperatures (a) α_{Pt} = 2500 ppm/°C; (b) α_{Pt} = 1500 ppm/°C..63
Figure 3.3.7 Expected temperature sensitivity with changing TaN TCR..................64
Figure 3.3.8 Illustration of mismatch cases affecting the half-bridge circuit............65
Figure 3.3.9 Expected reference sensor output with different degree of diagonal mismatch 67
Figure 3.3.10 Expected sensitivity to temperature with different degree of diagonal mismatch 67
Figure 3.3.11 Expected reference sensor output and temperature sensitivity against degree of horizontal mismatch 68
Figure 3.3.12 Expected reference sensor output and temperature sensitivity against degree of vertical mismatch 68
Figure 3.3.13 Expected change of temperature response sensitivity and maximum non-linearity error when mismatch values d increase to 20%...........................69
Figure 3.3.14 Expected temperature sensitivity against TCR of TaN elements with different diagonal mismatch (α_{Pt} = 3850 ppm/°C) 71
Figure 3.3.15 Expected temperature sensitivity against TCR of TaN elements with different diagonal mismatch (a) α_{Pt} = 2500 ppm/°C; (b) α_{Pt}= 1500 ppm/°C......71
Figure 3.3.16 Expected value of temperature response non-linearity error against TCR of TaN elements with different α_{Pt} (R_{Pt}:R_{TaN} = 0.03)...............................72
Figure 3.3.17 Expected value of temperature response non-linearity error against TCR of TaN elements with different α_{Pt}: R_{Pt}:R_{TaN} = (a) 0.03; (b) 0.09 73
Figure 4.2.1 Illustration of (a) X-ray diffraction, (b) resultant Debye-Scherrer representation and (c) equivalent XRD diffractogram, (d) out-of-plane GIXRD measurement...81
Figure 4.2.2 Illustration of tension effect on the XRD plot of a crystalline sample .82
Figure 4.2.3 XRD measurement result of an oxidised silicon wafer sample 84
Figure 4.2.4 XRD sample measurement results 85
Figure 4.3.1 Schematic illustration of geometrical relationship of resistivity-related electrical parameters..86

Figure 4.3.2 Illustration of four-point probe measurement 87
Figure 4.3.3 Illustration of Greek Cross structure 88
Figure 4.3.4 Illustration of Cross-Bridge measurement 88
Figure 4.3.5 Designed (a) Greek Cross and (b) Cross-Bridge test structures 90
Figure 4.3.6 Test setup designed to characterize developed thin films 91
Figure 4.3.7 Temperature calibration plot 92
Figure 4.3.8 Block diagram of virtual instrument functional flow 93
Figure 4.4.1 Tantalum-Nitrogen phase diagram 95
Figure 4.4.2 Example etch profiles: isotropic profile of wet etch process and anisotropic profile produced by dry etch process 97
Figure 4.4.3 Illustration of visual nitridation effect on tantalum nitride films 100
Figure 4.4.4 XRD measurement of samples annealed in nitrogen ambient at 450 and 500 °C for 30 minutes, 600 °C for 5 hours 102
Figure 4.4.5 Effect of vacuum annealing process temperature on 210 nm thick TaN samples produced using a 10% process 103
Figure 4.4.6 XRD measurement results of samples annealed for total of 7.5 hours at temperatures of 450 to 600 °C 104
Figure 4.4.7 Effect of vacuum annealing process performed at 600 °C on different thickness films produced using 10% process 105
Figure 4.4.8 Effect of vacuum annealing process performed at 600 °C on sheet resistance of thin films sputtered for 90 minutes in different N_2 flow ratios ... 106
Figure 4.4.9 Effect of vacuum annealing at 600 °C on TCR of films produced by 90 minute processes using different nitrogen flow ratios 107
Figure 4.4.10 Sheet resistance of as-deposited 190-210 nm samples and the change in resistance of these films after a 6 hour vacuum annealing process 108
Figure 4.4.11 XRD measurement results of as-deposited samples produced by different nitrogen flow ratio processes 109
Figure 4.4.12 XRD measurement results of samples annealed at 600° C for 6 hours produced by different processes: 10% and 12% N_2 flow ratio for 90 min 109
Figure 4.4.13 XRD measurement of samples produced by 12% process annealed at 600 °C for total of 6 and 12 hours 110
Figure 4.5.1 TCR measurement of as-deposited 100 nm Pt film: Ti adhesion 115

Figure 4.5.2 TCR measurement of annealed 100 nm Pt film: TaN adhesion 115
Figure 4.5.3 XRD sample measurements: annealed and as-deposited Ta on thermal SiO_2 117
Figure 4.5.4 XRD sample measurements: annealed and as-deposited Ta on TaN adhesion layer..........118
Figure 4.5.5 XRD sample measurements: annealed and as-deposited Pt on TaN adhesion layer; annealed and as-deposited Pt on TiN adhesion layer.............119
Figure 5.2.1 Schematic diagram of the half-bridge used as a temperature transducing circuit..........130
Figure 5.2.2 Layout of discrete element chips 131
Figure 5.2.3 Test setup designed to measure hybrid bridge temperature response.134
Figure 5.2.4 Block diagram of created virtual instrument functional flow 135
Figure 5.2.5 Estimation of parasitic effects on balancing circuit..........137
Figure 5.2.6 Measured temperature response of implemented bridge 138
Figure 5.3.1 Designed bridge to be integrated with SiC electronics and used as a standalone sensor with extra space for test structures..........141
Figure 5.3.2 Layout of a bridge to be integrated with SiC electronics and measured using the probe array: interconnect in TaN layer..........142
Figure 5.3.3 Layout of a bridge to be integrated with SiC electronics and measured using the probe array: interconnect in Al layer 143
Figure 5.3.4 Illustration of CBKR measurement and error sources in the contact resistance measurement..........145
Figure 5.3.5 Layout of Cross-Bridge Kelvin Resistor test structures..........146
Figure 5.3.6 3” wafer layout of chips..........147
Figure 5.4.1 Illustration of sensor device and test structure forming layers 148
Figure 5.4.2 The microfabrication process flow for Process 1..........150
Figure 5.4.3 Fabricated standalone bridge designed to be integrated with SiC electronics with sheet resistance test structures on the chip..........151
Figure 5.4.4 Fabricated standalone bridge with TaN interconnect designed to be integrated with SiC electronics and measured using the probe array..........151
Figure 5.4.5 Fabricated CBKR test structure with resist patterned for lift-off and metal lifted off..........153

Figure 5.4.6 Mask that was used to produce cross-section samples for SEM analysis: layout of a 4” mask and magnified view of used lines 153
Figure 5.4.7 Illustration of vertical TaN sidewall and over-etching depth into the thermal oxide: cross-section view from SEM tool 154
Figure 5.4.8 Illustration of smooth angular LF SiO2 sidewall and sputtered gold coverage failure: cross-section view from SEM tool...................................... 155
Figure 5.4.9 Illustration of resist remainders after 60-minute barrel asher process on 500 nm-thick PECVD oxide sample: top-down view from light microscope. 155
Figure 5.4.10 CBKR test structures at the stage of resist patterning on wafer used with evaporated (left) and sputtered (right) thin film platinum 156
Figure 5.5.1 Test setup used to measure integrated bridge circuits, sheet resistance and contact resistance test structures 158
Figure 5.5.2 Block diagram of VI functional flow 158
Figure 5.5.3 Measured contact resistance against inverse of designed contact area for annealed 100 nm Pt sample.. 160
Figure 5.5.4 Measured contact resistance against inverse of designed contact area for non-annealed 200 nm Pt sample 161
Figure 5.5.5 Measured contact resistance against inverse of designed contact area for non-annealed 200 nm Pt sample fabricated by improved lift-off process 161
Figure 5.5.6 Measured contact resistance against inverse of designed contact area for non-annealed 200 nm TaN sample fabricated by improved etching process .. 162
Figure 5.6.1 TCR measurement of 200-nm thick sputtered platinum film............. 163
Figure 5.6.2 Measured resistance for different contact resistance test structures between 200 nm sputtered platinum layer and TaN 164
Figure 5.6.3 Measured resistance for different contact resistance test structures between 200 nm evaporated platinum layer and TaN...................................... 165
Figrue 6.2.1 Illustration of layout improvements around contact areas in the integrated bridge 170
Figure 6.2.2 Improved temperature transducer bridge design to be integrated with SiC electronics and used as a standalone sensor.. 171
Figure 6.2.3 Designed bridge to be integrated with SiC electronics and measured using the probe array.. 172

Figure 6.2.4 (a) Bridge resistor test structure used to measure step coverage resistance. (b) Cross-section through the resistive track indicating the resistive elements introduced by the step 173
Figure 6.2.5 Modified TLM test structures used to measure contact resistance with contact spacing values of 20-80 μm and 80-320 μm 174
Figure 6.2.6 Contact chain test structure used to measure integrity of multiple contacts between two layers 175
Figure 6.2.7 Layout of cross-bridge Kelvin contact resistance test structures 176
Figure 6.2.8 Integrity check blocks for step resistance and contact chain test structures 178
Figure 6.2.9 Integrity check blocks for TLM and CBKR test structures 178
Figure 6.2.10 Example integrity check for blocks with all positive and all negative results 179
Figure 6.2.11 Block diagram of test structure-related VI functional flow 179
Figure 6.2.12 Block diagram of sensor-related VI functional flow 180
Figure 6.3.1 Improved design of microfabrication process flow 182
Figure 6.3.2 Fabricated bridge devices: (left) standalone temperature sensitive element designed to be integrated directly with SiC electronics; (right) device to be integrated with SiC electronics and measured using the probe array 183
Figure 6.3.3 Examples of fabricated test structures: (a) Step resistance test structure; (b) Contact chain test structure; (c) TLM-type test structure designed to measure contact resistance; (d) CBKR-type contact resistance test structures 183
Figure 6.3.4 Re-fabricated standalone bridge elements designed to be integrated with SiC electronics with sheet resistance test structures on chips 184
Figure 6.3.5 Re-fabricated standalone bridge with TaN interconnect designed to be integrated with SiC electronics and measured using the probe array 184
Figure 6.3.6 Step coverage resistance test structure, where conductive platinum layer was used on top of patterned PECVD oxide mesas. Test structure segment with 4×5 μm mesa overlap 185
Figure 6.3.7 Illustration of PECVD sidewall coverage by annealed platinum film: tilted cross-section view from SEM tool 185

Figure 6.3.8 Illustration of PECVD sidewall coverage by as-deposited platinum film: tilted cross-section view from SEM tool 186
Figure 6.3.9 Illustration of TaN sidewall coverage by platinum film, tilted view from SEM tool: (left) annealed platinum covering TaN sidewall; (right) as-deposited platinum covering TaN sidewall 187
Figure 6.3.10 Illustration of fabricated features, top-down view from light microscope: blanket Pt layer on TaN features (left); blanket Pt layer on PECVD oxide features (right) 187
Figure 6.3.11 Fabricated bridge devices using 240 nm-thick Pt: standalone device designed to be integrated directly with SiC electronics (left); device to be measured using the probe array (right) 188
Figure 6.3.12 Fabricated test structure array and contact chain resistance and TLM-type contact resistance test structures between Pt and TaN 188
Figure 6.4.1 Measured resistance value validation maps 191
Figure 6.4.2 Resistance change with increasing step count 192
Figure 6.4.3 Resistance change with increasing layer overlap 192
Figure 6.4.4 Resistance as a function of contacts spacing in TLM structures: measurements from test structures with L = 20 to 320 μm............................. 194
Figure 6.4.5 Resistance as a function of distance between contacts in TLM structures: measurements from test structures with L = 20, 40 and 80 μm 195
Figure 6.4.6 Measured resistance change against inverse of contact area of CBKR test structures on annealed sample with 200 nm Pt 196
Figure 6.4.7 Measured resistance change against inverse of contact area of CBKR test structures on annealed sample with 400 nm Pt without $LFSiO_2$ 197
Figure 6.4.8 Output voltage as a function of designed resistor ratio measured at 50 °C on devices on wafer 1 199
Figure 6.4.9 Measured temperature sensitivity against designed resistor ratio of devices on wafer 1 199
Figure 6.4.10 Wafer maps of measured start of output range and sensitivity values demonstrated in Fig. 6.4.8 and 6.4.9 200
Figure 6.4.11 Output voltage as a function of designed resistor ratio measured at 50 °C on devices on wafer 2 201

Figure 6.4.12 Measured temperature sensitivity against designed resistor ratio of devices on wafer 2 201
Figure 6.4.13 Wafer maps of measured start of output range and sensitivity values demonstrated in Fig. 6.4.11 and 6.4.12 202
Figure 6.4.14 Output voltage as a function of designed resistor ratio measured at 25 °C on devices on wafer 3 203
Figure 6.4.15 Measured temperature sensitivity against designed resistor ratio of devices on wafer 3 203
Figure 6.4.16 Wafer maps of measured start of output range and sensitivity values demonstrated in Fig. 6.4.14 and 6.4.15 and detailed in Table B.2.1 204
Figure 6.4.17 Output voltage as a function of designed resistor ratio measured at 25 °C on devices on wafer 4 205
Figure 6.4.18 Measured temperature sensitivity against designed resistor ratio of devices on wafer 4 206
Figure 6.4.19 TCR measurement of annealed 240 nm-thick evaporated Pt covered by PECVD oxide 206
Figure 6.4.20 TCR measurement of annealed 200 nm-thick sputtered TaN covered by PECVD oxide 207
Figure 6.4.21 Wafer maps of measured start of output range and sensitivity values demonstrated in Fig. 6.4.17 and 6.4.18 and detailed in Table B.2.2 207
Figure 7.3.1 Integrated process: platinum is deposited first on a planar surface 219

List of tables

Table 2.2.1 Comparison of piezoelectric coefficient d_{33} and dielectric constant ε_{r33} values for example materials 13

Table 2.3.1 Comparison of emf at 100 °C for different materials referred to Pt 20

Table 2.3.2 Resistivity and TCR of example metal materials.................................. 23

Table 2.3.3 Comparison of pyroelectric coefficient and Curie temperature values for example materials 32

Table 2.4.1 Comparison of reviewed materials' high temperature properties 40

Table 3.3.1 Considered mismatch cases and mismatch effect on each element 66

Table 3.3.2 Temperature sensing performance of comparable thermometer types .. 74

Table 4.4.1 Comparative measurement of tantalum nitride thin films affected by annealing in nitrogen for 30 min.. 101

Table 4.4.2 Comparative measurement of tantalum nitride film resistance before and after annealing at 600 °C in vacuum 105

Table 4.4.3 Comparative measurement of tantalum nitride phase content before and after annealing in vacuum; comparison with result from the literature source 110

Table 5.2.1 List of geometrical parameters and resultant resistance of designed thin film resistive elements 131

Table 5.3.1 List of design elements and parameters of designed transducers 144

Table 5.3.2 List of designed resistive test structures according to cell name 144

Table 5.5.1 Summary of measured contact resistance values for different thickness of evaporated platinum according to designed contact areas.......................... 159

Table 6.2.1 Design parameters for different mesa structures................................. 173

Table 6.4.1 Step resistance values measured on all chips...................................... 189

Table 6.4.2 Step resistance test structure data validated using Eq. (6.9) 191

Abbreviations

Chapter 1

CMOS	Complementary metal–oxide–semiconductor
CVD	Chemical vapour deposition
PECVD	Plasma-enhanced chemical vapour deposition

Chapter 2

CGG	Calcium gallium germanate
CMOS	Complementary metal–oxide–semiconductor
CVD	Chemical vapour deposition
EOM	Electro-optical modulator
FBG	Fiber Bragg grating
FP	Fabry-Perot
FPI	Fabry-Perot interferometer
GF	Gauge factor
HPHT	High pressure, high temperature
IEC	*International Electrotechnical Commission*
IR	Infrared
NTC	Negative temperature coefficient
PCF	Photonic-crystal fiber
PIR	Passive infrared
PRT	Platinum resistance thermometer
PTC	Positive temperature coefficient
PZT	Lead zirconate titanate
RMS	Root mean square

RTD	Resistance temperature detector
sccm	Standard cubic centimetres per minute
SPRT	Standard platinum resistance thermometer
TCR	Temperature coefficient of resistance
UV	Ultraviolet
XRD	X-ray diffraction

Chapter 3

IC	Integrated circuit
NTC	Negative temperature coefficient
RTD	Resistance temperature detector
SPRT	Standard platinum resistance thermometer
TCR	Temperature coefficient of resistance

Chapter 4

a-TaN	Amorphous tantalum nitride
AES	Auger electron spectroscopy
BNC	Bayonet Neill–Concelman connector
CMOS	Complementary metal–oxide–semiconductor
DC	Direct current
EDX	Energy-dispersive X-ray spectroscopy
GIXRD	Grazing incidence X-ray diffraction
PC	Personal computer
PDF	Powder diffraction file
PECVD	Plasma-enhanced chemical vapour deposition
PID	Proportional–integral–derivative
RF	Radio frequency
RIE	Reactive ion etching

sccm	Standard cubic centimetres per minute
SMC	*Scottish Microelectronics Centre*
TCR	Temperature coefficient of resistance
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction

Chapter 5

BNC	Bayonet Neill–Concelman connector
CBKR	Cross-bridge Kelvin resistor
CMRR	Common-mode rejection ratio
DC	Direct current
DI	Deionized
GPIB	General Purpose Interface Bus
LF	Low frequency
PC	Personal computer
PCB	Printed circuit board
PECVD	Plasma-enhanced chemical vapour deposition
RIE	Reactive ion etching
RTD	Resistance temperature detector
SEM	Scanning electron microscopy
SMC	*Scottish Microelectronics Centre*
SMU	Source-measurement unit
TCR	Temperature coefficient of resistance
USB	Universal serial bus
VI	Virtual instrument

Chapter 6

CBKR	Cross-bridge Kelvin resistor

CFR	Contact front resistance
CMOS	Complementary metal–oxide–semiconductor
PECVD	Plasma-enhanced chemical vapour deposition
RIE	Reactive ion etching
SEM	Scanning electron microscopy
SMU	Source-measurement unit
TCR	Temperature coefficient of resistance
TLM	Transmission line model
VI	Virtual instrument
VMU	Voltage monitor unit

Chapter 7

CBKR	Cross-bridge Kelvin resistor
CMOS	Complementary metal–oxide–semiconductor
GIXRD	Grazing incidence X-ray diffraction
PECVD	Plasma-enhanced chemical vapour deposition
PVD	Physical vapour deposition
SEM	Scanning electron microscopy
TCR	Temperature coefficient of resistance
TLM	Transmission line model
XRD	X-ray diffraction

Appendices

DI	Deionized
HMDS	Hexamethyldisilazane
IPA	Isopropyl alcohol
PECVD	Plasma-enhanced chemical vapour deposition
RIE	Reactive ion etching

SEM	Scanning electron microscopy
TCR	Temperature coefficient of resistance
TLM	Transmission line model
TMAH	Tetramethylammonium hydroxide

Publications

[1] A. Tabasnikov, A. S. Bunting, J. G. Terry, J. Murray, G. Cummins, C. Zhao*, et al.*, "Characterization and development of materials for an integrated high-temperature sensor using resistive test structures," *Microelectronic Test Structures (ICMTS), 2014 International Conference on,* pp. 188-193, 2014.

http://dx.doi.org/10.1109/ICMTS.2014.6841491

[2] A. Tabasnikov, A. J. Walton, and S. Smith, "Combined transmission line measurement structures to study thin film resistive sensor fabrication," *Microelectronic Test Structures (ICMTS), 2015 International Conference on,* pp. 175-180, 2015.

http://dx.doi.org/10.1109/ICMTS.2015.7106136

Chapter 1 Introduction

1.1 Background

The idea of integrating sensors and transducers with electronics, to provide amplification of their response to the measured parameter or signal processing, has been in focus of many research groups since the early 1980s [1]. The ability to combine sensors with integrated electronic circuits using microfabrication approaches is now strongly associated with the concept of a “smart sensor” [2]. The aim of which is to condition and process the measured analogue signal from the sensor, convert the output into the digital domain for further transmission and communication with electronics as close to the sensor as possible. The technological advancement of smart sensors is supported by a high value market driven by automotive, aerospace and energy applications and thus attracts a lot of research interest [3-6].

Complementary metal oxide semiconductor technology (CMOS) electronics are accessible to small and medium-sized enterprises such as the Scottish Microelectronics Centre, which can add value through post-CMOS processing of add-on layers allowing integration with new materials and addition or increase of the sensor systems functionality [3, 7, 8]. Functional diversification of integrated systems does not necessarily follow the scaling of electronics governed by Moore’s law and hence is following “More than Moore” concept.

The same materials and processes that are commonly used to produce integrated circuits can also be used to fabricate sensor systems, and this has driven the

development of certain types of integrated sensors [3]. Fabrication of non-semiconductor sensor structures can be made CMOS-compatible and as a result an integrated smart sensor can be produced using an integrated process. Bulk micromachining production methods for building sensors, which involve etching of the substrate, are not always economically justified on costly materials, such as for example, hexagonal silicon carbide [9].

Surface micromachining fabrication methods were used to integrate electronics with sensors such as for example pressure sensors [10], acceleration sensors [11], temperature sensors [12], gas sensors [12] and biochemical sensors [13]. Post-CMOS processing of add-on layers, where processing of sensors would be performed with minimal risk of damage the underlying circuitry, has been used to produce some integrated devices [14-16]. However, the drawback of such an approach is, a limited maximum temperature exposure, which is ~450 °C for silicon CMOS circuits with aluminium metallization layers. On the other hand, CMOS-compatible processes such as plasma-enhanced chemical vapour deposition (PECVD), sputtering and evaporation can be used to deposit sensor materials and dry or wet surface micromachining processes can be used to produce the required patterns [3]. Bulky transducers for most physical quantities can currently be replaced with micro-miniaturised equivalents with minimal trade-offs which provide similar functionality and a comparable level of reliability [17]. The initial integration attempts described in the literature to achieve miniaturisation were met by reliability problems, but they are no longer the main issue due to current maturity of deposition and patterning processes as well as the effort put into chemical and mechanical matching of materials [3]. Furthermore, new materials suitable for microengineering have appeared decreasing the size of devices and rendering them more cost-efficient through density improvement [18].

Unfortunately, the most abundant silicon-based integrated circuits do not offer the required reliability and performance in harsh environments. Compound semiconductors such as gallium nitride and silicon carbide (SiC) are currently being developed to fill in the technology gap in electronics and smart sensors for harsh environment operations [19]. Integrating sensors with SiC electronics and improving

the ability of smart sensors to operate at extremes of temperature, corrosion and radiation is a focus of multiple research groups [20-23]. Cubic silicon carbide (3C-SiC) is usually used to produce sensor structures by bulk micromachining while hexagonal 4H- or 6H-silicon carbide is usually employed to produce electronics. It is more practicable to produce sensors using materials other than cubic SiC (which is grown using CVD) on top of the electronics fabricated in hexagonal SiC to decrease the temperature of processes used to fabricate the sensor. This work will detail the investigation and development of a high temperature half-bridge based sensor that uses thin film platinum as sensing elements, the response of which is expected to be measured by a SiC instrumentation amplifier of a target design.

In parallel with the research efforts on post-processing and smart sensor integration, the development of fabrication processes for creating active devices with integrated passive components or networks of those takes place [24-30]. Microengineering of film materials, such as platinum, palladium, indium tin oxide, titanium nitride or tantalum nitride, increases the degree of system-level integration even further, reduces the device area requirements and decreases the amount of parasitics introduced by discrete electronic components [3]. These passive components can be post-processed by surface micromachining techniques that allow the integration of sensor elements into the backend fabrication process, when electronic circuits are protected from the effect of further processes required to produce the passive components and interconnect.

Advancements in thin film deposition and patterning on arbitrary surfaces allow the deposition of multiple sensing devices directly onto the structural and functional elements of transport vehicles, such as gas turbine engine compressor blades [31, 32]. The application areas of these devices are specific, but such a fabrication approach attracts increased interest from automotive, aerospace, energy and environmental monitoring industries. Although in the case of this work the effort is not focussed on miniaturisation, the research of thin film materials for these devices is fundamental because devices measuring one parameter need to have as little as possible cross-sensitivity to other parameters as for example – low temperature sensitivity for a strain gauge [33].

Sensors produced using metal thin films have the potential to provide the required stability in harsh environments while sensors produced using CMOS-compatible processes enable both better process integration and lower temperature deposition and processing budgets [3]. Monolithic integration of sensors and electronics results inherently in better device test integration as well as smaller packaging of integrated devices. This does not affect the system performance and creates less parasitic effects [18].

1.2 Thesis structure

This section briefly outlines the contents of the thesis. Chapter 2 reviews current high temperature sensor technologies while Chapter 3 introduces the concept of the high temperature sensor developed during this project, describes its application and provides sensitivity analysis of the circuit. Chapters 4 to 6 describe the development and implementation of the integrated high temperature sensor, in particular high temperature thin film material development, demonstration of a hybrid temperature sensor and its further development into an integrated architecture. Chapter 7 outlines the conclusions drawn from fabrication and measurement results in previous chapters and suggests the focus of future work.

Chapter 2: High temperature sensing technologies. This chapter introduces the reader to examples of transduction methods that are most relevant to high temperature sensing and sensor technologies. It then reviews electronic temperature measurement technologies with a focus on available materials and the possibility of application at high temperatures.

Chapter 3: Design of temperature transducer bridge. This chapter describes the application of the designed sensor and details the working principles of the selected half-bridge measurement circuit. Circuit elements that are required to implement the integrated temperature measurement capability are examined, the choice of materials to produce the resistive elements is justified, and sensitivity analysis of the resultant circuit is presented.

Chapter 4: Development of thin film materials. This chapter describes the development of thin film platinum and tantalum nitride materials that are used to fabricate the temperature sensor. This is supported by crystallographic and electrical measurements using microfabricated test structures. The development of the main fabrication processes is described in detail, and the relationship between process parameters and measurement results is demonstrated.

Chapter 5: Development of integrated temperature transducer bridge. This chapter presents the development of an integrated sensor design. The first part demonstrates a hybrid temperature sensor that is based on the thin film materials developed in Chapter 4. The second part describes the design, fabrication and measurement of contact resistance test structures produced by an integrated combination of these fabrication processes. Suggestions are provided for the solution to a problem which arises when thin films are deposited one after another and are contacted through a passivation layer.

Chapter 6: Integrated bridge improvement and results. This chapter presents the improvement of layout and fabrication processes for the high temperature sensor devices following from issues encountered during development of an integrated process design. The measurement results obtained using devices fabricated by variations of improved integrated process are presented and discussed. It also details the design and measurement of test structures that assist in understanding the influence of parasitic elements introduced during integrated sensor fabrication.

Chapter 7: Conclusions and further work. This chapter summarizes the results and conclusions of thesis. Suggestions for further improvement and process optimisation are given with a focus on alleviating or eliminating issues with the integrated process combining TaN and Pt resistors to build the sensor circuit.

References

[1] R. S. Muller, "Integrating sensors and electronics - New challenges for silicon," *Electron Devices Meeting, 1984 International,* pp. 206-209, 1984.
[2] G. Meijer, "Smart Sensor Systems: Why? Where? How?," in *Smart Sensor Systems*, G. Meijer, Ed. Chichester, UK: Wiley, 2008, pp. 1-22.
[3] O. Brand, "Fabrication Technology," in *CMOS - MEMS*, H. Baltes *et al.*, Eds., (Advanced Micro & Nanosystems, no. 2), Weinheim, Germany: Wiley-VCH, 2005, pp. 1-68.
[4] R. Czichy, "Aerospace Sensors," in *Micro- and Nanosensor Technology/Trends in Sensor Markets*, H. Meixner and R. Jones, Eds., (Sensors: A Comprehensive Survey, no. 8), Weinheim, Germany: Wiley-VCH, 1995, pp. 365-412.
[5] P. Cockshott, "Automotive Sensors," in *Micro- and Nanosensor Technology/Trends in Sensor Markets*, H. Meixner and R. Jones, Eds., (Sensors: A Comprehensive Survey, no. 8), Weinheim, Germany: Wiley-VCH, 1995, pp. 491-524.
[6] J. W. Knutti and H. V. Allen, "Trends in MEMS Commercialization," in *Enabling Technologies for MEMS and Nanodevices: Advanced Micro and Nanosystems* Wiley Online Library: Wiley-VCH, 2008, pp. 21-47.
[7] M. Hiroki, M. Shinichiro, I. Hiromu, and M. Katsuyuki, "Integrated CMOS-MEMS technology and its applications," *Solid-State and Integrated-Circuit Technology, 9th International Conference on,* pp. 2460-2463, 2008.
[8] W. Arden, M. Brillouët, P. Cogez, M. Graef, B. Huizing, and R. Mahnkopf, "More-than-Moore," ed. http://www.itrs2.net/uploads/4/9/7/7/49775221/irc-itrs-mtm-v2_3.pdf: International Technology Roadmap for Semiconductors, 2010.
[9] R. Cheung, *Silicon Carbide Microelectromechanical Systems for Harsh Environments*. London, UK: Imperial College Press, 2006.
[10] O. Paul and H. Baltes, "Novel fully CMOS-compatible vacuum sensor," *Sensors and Actuators A: Physical,* vol. 46, no. 1-3, pp. 143-146, 1995.
[11] A. A. Seshia *et al.*, "A vacuum packaged surface micromachined resonant accelerometer," *Journal of Microelectromechanical Systems,* vol. 11, no. 6, pp. 784-793, 2002.
[12] F. Udrea *et al.*, "Three technologies for a smart miniaturized gas-sensor: SOI CMOS, micromachining, and CNTs - challenges and performance," *2007 IEEE International Electron Devices Meeting,* pp. 831-834, 2007.
[13] C. Vancura, Y. Li, K. U. Kirstein, F. Josse, A. Hierlemann, and J. Lichtenberg, "Fully integrated CMOS resonant cantilever sensor for bio-chemical detection in liquid environments," *The 13th International Conference on Solid-State Sensors, Actuators and Microsystems,* vol. 1, pp. 640-643, 2005.
[14] J. M. Bustillo, G. K. Fedder, C. T. C. Nguyen, and R. T. Howe, "Process technology for the modular integration of CMOS and polysilicon microstructures," *Microsystem Technologies,* vol. 1, no. 1, pp. 30-41, 1994.

[15] M. Wycisk, T. Tönnesen, J. Binder, S. Michaelis, and H. J. Timme, "Low-cost post-CMOS integration of electroplated microstructures for inertial sensing," *Sensors and Actuators A: Physical,* vol. 83, no. 1-3, pp. 93-100, 2000.
[16] A. E. Franke, J. M. Heck, K. Tsu-Jae, and R. T. Howe, "Polycrystalline silicon-germanium films for integrated microsystems," *Journal of Microelectromechanical Systems,* vol. 12, no. 2, pp. 160-171, 2003.
[17] G. Ciuti, L. Ricotti, A. Menciassi, and P. Dario, "MEMS sensor technologies for human centred applications in healthcare, physical activities, safety and environmental sensing: a review on research activities in Italy," *Sensors (Basel),* vol. 15, no. 3, pp. 6441-68, 2015.
[18] A. C. Fischer *et al.*, "Integrating MEMS and ICs," *Microsystems & Nanoengineering,* vol. 1, p. 15005, 2015.
[19] J. Watson and G. Castro, "A review of high-temperature electronics technology and applications," *Journal of Materials Science: Materials in Electronics,* vol. 26, no. 12, pp. 9226-9235, 2015.
[20] M. Wijesundara and R. Azevedo, *Silicon Carbide Microsystems for Harsh Environments*. New York, USA: Springer, 2011.
[21] G. Hunter *et al.*, "An Overview of Wide Bandgap SiC Sensor and Electronics Development at NASA Glenn Research Center," *ECS Transactions,* vol. 11, no. 5, pp. 247-257, 2007.
[22] D. G. Senesky, B. Jamshidi, C. Kan Bun, and A. P. Pisano, "Harsh Environment Silicon Carbide Sensors for Health and Performance Monitoring of Aerospace Systems: A Review," *IEEE Sensors Journal,* vol. 9, no. 11, pp. 1472-1478, 2009.
[23] R. Maboudian, C. Carraro, D. G. Senesky, and C. S. Roper, "Advances in silicon carbide science and technology at the micro- and nanoscales," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 31, no. 5, p. 050805, 2013.
[24] T. Remmel *et al.*, "Integration of Thin-Film Capacitors and Resistors into ULSI Technology for Wireless Applications," *Passive Component Industry,* no. January/February 2001, pp. 24-32 2001.
[25] R. Henderson *et al.*, "Tantalum nitride thin film resistors for integration into copper metallization based RF-CMOS and BiCMOS technology platforms," *Silicon Monolithic Integrated Circuits in RF Systems,* pp. 71-74, 2001.
[26] R. F. Kopf *et al.*, "Thin-film resistor fabrication for InP technology applications," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 20, no. 3, p. 871, 2002.
[27] J. Yang *et al.*, "Low Energy Sputter Deposition and Properties of NiCr Thin Film Resistors for GaAs Integrated Circuits," in *International Conference on Compound Semiconductor Manufacturing Technology*, 2005.
[28] A. Malmros, M. Südow, K. Andersson, and N. Rorsman, "TiN thin film resistors for monolithic microwave integrated circuits," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 28, no. 5, p. 912, 2010.
[29] M. J. Martinez *et al.*, "TaN Resistor Process Development and Integration," *International Conference on Compound Semiconductor Manufacturing Technology,* 2010.

[30] O. Arenas *et al.*, "Integration of Micro Resistance Thermometer Detectors in AlGaN/GaN Devices," *IEEE Journal of the Electron Devices Society,* vol. 2, no. 6, pp. 145-148, 2014.
[31] J. Yang, "A silicon carbide wireless temperature sensing system for high temperature applications," *Sensors (Basel),* vol. 13, no. 2, pp. 1884-901, 2013.
[32] R. D. Meredith, J. D. Wrbanek, G. C. Fralick, L. C. Greer, G. W. Hunter, and L. Chen, "Design and operation of a fast, thin-film thermocouple probe on a turbine engine," *50th AIAA/ASME/SAE/ASEE Joint Propulsion Conference, Propulsion and Energy Forum,* 2014.
[33] J. D. Wrbanek, G. C. Fralick, J. M. Gonzalez, and K. L. H. Laster, "Thin Film Ceramic Strain Sensor Development for High Temperature Environments," *NASA: Aging Aircraft 2008,* 2008.

Chapter 2 High temperature sensing technologies

2.1 Introduction

Temperature is a physical property that describes the average kinetic energy of random motions of electrons, atoms and molecules that move freely within solid materials, liquids or gas media. These motions have effects on material properties and integrity as well as on the performance of physical and chemical processes, therefore it is important to measure this parameter. Properties such as density, vapour pressure and electrical conductivity are affected significantly by temperature, and as a result these quantities can be used to infer the temperature value [1, 2].

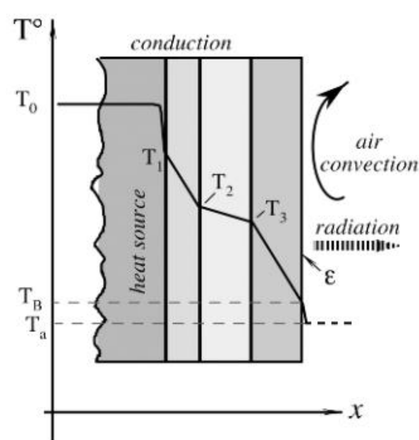

Figure 2.1.1: *Illustration of temperature distribution in multilayer solid acting as a source of heat that is transferred by different mechanisms [1].*

The average kinetic energy of agitated particles is represented by the absolute temperature. This is measured in Kelvin, meaning that at 0 K particles have no thermal energy [2]. The measure of thermal energy is heat, which can be transferred from hotter to colder objects or regions by three mechanisms: conduction, convection and radiation, the illustration of which is depicted in Fig. 2.1.1 [1]. Heat conduction takes place through physical contact between thermally conductive surfaces at different temperatures and the heat flow rate is proportional to their surface area, thermal contact resistance, thermal conductivity and thermal gradient. Thermal convection involves movement of fluid that takes the heat away from a hot surface and the rate of this process depends on surface area and convection type. Thermal radiation is electromagnetic in nature and is generated in a spectrum range that is dependent on the temperature; the amount of emitted radiation depends on surface area and its thermal radiation effectiveness.

This chapter will review high temperature thermometers and transduction methods that pertain to sustained operation at high temperature. There is a focus on the ability to read the measured parameter electrically because this aligns with the overall objectives of this work. It will begin by briefly describing piezoelectric and piezoresistive transduction methods, which can be employed to measure pressure and strain and, given suitable construction and selection of materials, perform these measurements at high temperatures. Sensors have different operational capabilities depending on the deployment environment, the method of transduction of the physical parameter into an electrical signal and the measurement principle of this signal. There are generally two – direct and indirect – measurement methods, which define whether the object of measurement is measured directly or the value is inferred from measuring a property that is affected by the object of measurement. The examples of indirect sensors are piezoresistive and thermoresistive sensing elements, which require an excitation current source and rely on resistance coefficients, while piezoelectric and thermoelectric sensors actively generate a voltage which is directly related to the according measured parameter. Infrared radiation can be measured using indirect techniques based on different electronic sensitive elements that are constructed in such a way that absorbs the heat radiation

in the infrared range of electromagnetic spectrum [3]. Optical fibers can be used to measure the change in response to excitation signal fed into the fiber due to changes in strain or temperature or used as a guide for thermal radiation [4].

2.2 Pressure and strain sensors

Sensor devices based on piezoelectric and piezoresistive transduction methods rely on sensitivity to deformation and creep of measured structures through temperature-dependent piezo-coefficients of materials. Measuring pressure and strain in harsh environments is challenging from the perspective of both materials and measurement instrumentation. However, monitoring these parameters reliably is as critical a task in many applications as measuring fundamental properties such as temperature. This section will describe piezoelectric and piezoresistive transduction methods, cover different designs and manufacturing characteristics and summarise materials that relate to high temperature environment applications.

2.2.1 Piezoelectric sensors

Operation of a piezoelectric sensor is based on a fact that deformations in piezoelectric material crystal due to applied force result in accumulation of an electrical charge Q that is proportional to the force. Some of the best examples of sensors using piezoelectric effects are dynamic pressure sensors, where the active area of a diaphragm converts a difference in pressure into a force that acts on the piezoelectric sensing element [5]. The direct piezoelectric effect that describes the accumulation of charge due to applied stress can be expressed using the following equation:

$$D = \varepsilon E + d_{xy}\sigma, \ (\mathrm{C\cdot m^{-2}}) \ [6] \qquad (2.1)$$

where D is the electric displacement field, ε is the electric permittivity (the product of vacuum and relative permittivity values ε_0 and ε_r), d_{xy} is the material piezoelectric coefficient in the measured direction ($\mathrm{C\cdot N^{-1}}$), E is the electric field strength and σ denotes the applied stress. Piezoelectric properties are anisotropic, hence the

orientation of crystalline planes in piezoelectric material is highly important. Depending on how the crystal structure is oriented towards the applied mechanical load in the sensitive elements, different operational modes are possible. The most widely utilized are longitudinal and transverse operational modes, which produce different orientation of polarization in response to applied force, with illustration of transverse piezoelectric effect demonstrated in Fig. 2.2.1.

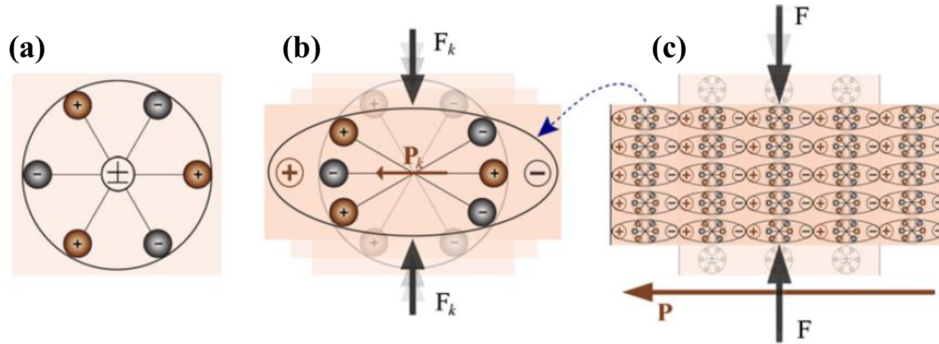

Figure 2.2.1: *Illustration of piezoelectric effect: (a) molecule with no piezoelectric effect, (b) polarization of molecule through direct piezoelectric effect due to applied force, (c) transverse piezoelectric effect in material due to compressive force [6].*

The longitudinal piezoelectric effect is described using Equation 2.2, where the electrical charge Q_L is independent of the geometry of the sample and is proportional to the applied force F and the longitudinal piezoelectric coefficient d_{33}. The charge induced by transverse effect (Q_T) depends on the sample geometry, as shown in Eq. (2.3), where l and t are the length and thickness of a piezoelectric material slice [5].

$$Q_L = d_{33}F, \text{ (C) [5]} \tag{2.2}$$

$$Q_T = d_{11}F\frac{l}{t}, \text{ (C) [5]} \tag{2.3}$$

Many piezoelectric materials offer a wide operating temperature range and are usually limited by the Curie temperature T_C at which point the material loses its piezoelectric properties and becomes a dielectric. For example, quartz (SiO_2) which is typically used in pressure sensors, can be used up to 400 °C and be produced at low cost, but is not ready to be integrated into a CMOS process in a single-crystal structure [5]. Gallium phosphate ($GaPO_4$) has the same crystalline structure as quartz, but offers a practically constant sensitivity to force that is twice that of quartz

up to 500 °C, however its crystals are difficult to fabricate [5]. Lead based materials like PZT ($PbZr_xTi_{(1-x)}O_3$) and lead metaniobate ($PbNb_2O_6$) have very large piezoelectric sensitivity, but long-term degradation and a huge pyroelectric effect limit their applications [5]. Bismuth titanate-based piezoceramics can be used up to 600 °C, but suffer from similar problems. CGG group piezoelectric materials (for example, lanthanum gallium silicate, $La_3Ga_5SiO_{14}$) are strictly piezoelectric and have no phase transition up to their melting point (in excess of 1000 °C), but are limited in usage to 1000 °C due to evident temperature dependence of resistivity [7, 8].

Some piezoelectric materials, for example PZT and lead metaniobate, can be ferroelectric, which means that they have randomly oriented dipoles and the piezoelectric effect will not naturally occur in them. These materials can be poled artificially at temperatures slightly below their Curie point when placed into a strong electric field. As a result, dipoles are oriented along the lines of an electric field, which is maintained while the material is gradually cooled down to room temperature, until the electric field is finally removed [9]. The poled ferroelectric material will then retain its polarization as long as it stays below the Curie temperature.

An example list of materials that exhibit piezoelectric properties is given in Table 2.2.1, where coefficients d_{33} for longitudinal piezoelectric effect are given for different forms that materials can be fabricated in [10-12].

Table 2.2.1 *Comparison of piezoelectric coefficient d_{33} and dielectric constant ε_{r33} values for example materials.*

Material	*Form*	Piezoelectric coefficient d_{33}, 10^{-12} C·N^{-1}	Dielectric constant ε_{r33}
SiO_2	*Single crystal*	2.3	4.5
AlN	*Oriented film*	5	9
$LiNbO_3$	*Polycrystalline*	23	28
$BaTiO_3$	*Polycrystalline*	190	1700
ZnO	*Polycrystalline*	246	1400
$PbZr_{0.6}Ti_{0.4}O_3$	*Polycrystalline*	370	1700
$Pb_{0.925}La_{0.5}$-$Zr_{0.56}Ti_{0.44}O_3$	*Polycrystalline*	545	1500

2.2.2 Piezoresistive sensors

Piezoresistive sensors convert applied strain to a difference in measured resistance. There are geometric and resistive components of piezoresistive effect in most materials that come from the facts that strained sensitive elements change their dimensions, which results in an increase in length to cross-section ratio, and strained piezoresistive materials have significantly different resistivity which depends on crystal orientation [5]. The relative change in resistance of a wire with circular cross section due to applied force can be expressed as:

$$\frac{\Delta R}{R} = \frac{\Delta \rho}{\rho} + \frac{\Delta L}{L} - \frac{2\Delta D}{D}, \text{ [13]} \tag{2.4}$$

where R is initial metal wire resistance, L and D are accordingly wire length and diameter, ρ is resistivity of metal in unstressed condition. Gauge factor (GF) is defined as the ratio of change of electrical resistance in response to mechanical strain $\varepsilon = \frac{\Delta L}{L}$:

$$GF = \frac{\Delta R / R}{\Delta L / L} = \frac{\Delta \rho / \rho}{\Delta L / L} + 1 - 2\frac{\Delta D / D}{\Delta L / L}, \text{ [13]} \tag{2.5}$$

Since the last term is governed by Poisson effect, which states that longitudinal expansion of a wire results in contraction in transverse direction, replacing $-\frac{\Delta D / D}{\Delta L / L}$ by Poisson ratio υ in Eq. 2.5 yields:

$$GF = 1 + 2\upsilon + \frac{\Delta \rho / \rho}{\Delta L / L} = 1 + 2\upsilon + \frac{\Delta \rho / \rho}{\sigma}\frac{\sigma}{\varepsilon} = 1 + 2\upsilon + \pi E, \text{ [13]} \tag{2.6}$$

where π is piezoresistive coefficient that defines the change in resistivity in response to applied stress and E stands for Young's modulus of metal, which defines a proportion between applied strain and resultant stress. Finally, the change in resistance in a wire with cross-section area of A with applied force F can be expressed in terms of fundamental material properties using:

$$\frac{\Delta R}{R} = \frac{F}{A}\frac{GF}{E}, \text{ [13]} \tag{2.7}$$

Equation 2.7 shows that materials with a large gauge factor and small Young's modulus are preferable in order to improve the sensitivity of piezoresistive sensors.

The value of gauge factor depends on the material properties and conduction mechanism, for example, metal foil strain gauges have gauge factors between 2 and 5 [14]. The most common measurement of piezoresistive strain gauges, an example of which is shown in Fig. 2.2.2(a), is performed using a Wheatstone bridge circuit to maximize the sensitivity to applied mechanical strain or pressure because the full-scale change of resistance can be as low as 1%. Common technologies that are used to produce the piezoresistive sensitive elements are doped silicon, polysilicon thin films, metal foils that are fixed to the measured structure and deposited metal films.

The gauge factor of single crystal doped silicon strain gauges is couple of orders higher than of metal strain gauges ($GF_{\mathrm{Si}} \approx$ 100-150). This is fully employed in pressure sensors that are based on measurement of piezoresistive bridge comprised of elements embedded into a diaphragm that is subjected to pressure [5]. Using silicon as a diaphragm material offers better elasticity when compared to the other materials typically used to create diaphragms. Furthermore, the integrated silicon piezoresistive elements do not experience bonding and creep issues that are typical for piezoresistors bonded to metallic diaphragms [15].

The silicon piezoresistive sensor can be produced by ion implanting four piezoresistors into the silicon to create sensitive elements, etching the backside of the substrate to produce the diaphragm (creating a structure depicted in Fig. 2.2.2(b,c)) and bonding a second substrate to create the reference chamber which may be sealed or include a port to set the reference. The thickness of the diaphragm defines the sensitivity and pressure input range of the piezoresistive sensor. Pressure sensors can be categorized by the pressure value that they are referenced to. Gauge pressure sensors are zero-referenced against pressure in a reference chamber that is open to atmosphere, while differential pressure sensors measure the difference in pressures between two pressure ports. Absolute pressure sensors measure the value with respect to a vacuum reference, which means that chamber under the diaphragm is sealed at near vacuum pressure (25 mTorr). Vacuum gauge pressure sensors measure a vacuum supplied against an external atmospheric pressure.

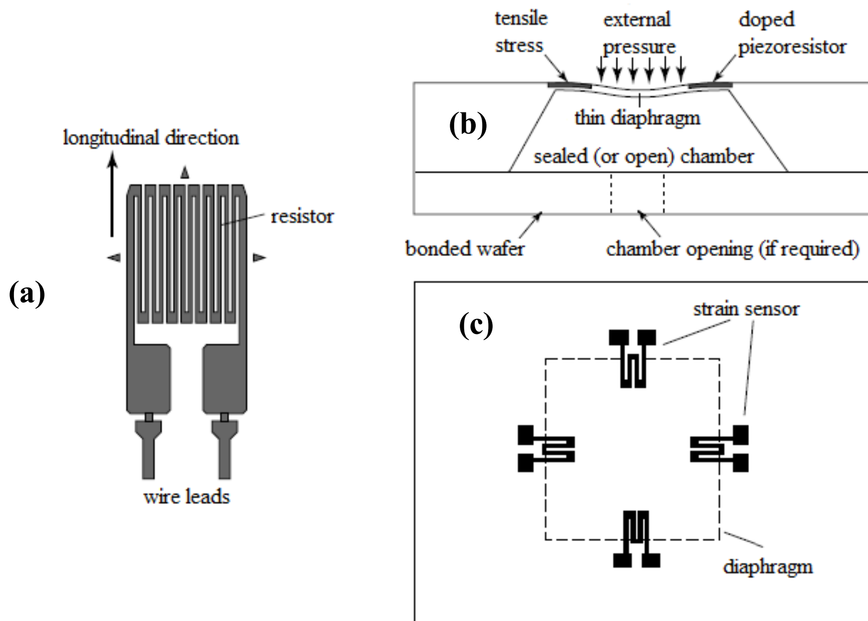

Figure 2.2.2: *(a) Schematic layout of a strain sensor; Schematic construction of pressure sensor: (b) side-view illustration of pressure effect on sensitive elements, (c) top-view layout of sensitive elements around diaphragm. Adapted from [16].*

The useful temperature range of semiconductor piezoresistive elements is limited, for example, most popular silicon elements are usable to around 300 °C because they gradually lose sensitivity to strain (sensitivity drift) and change nominal resistance value (zero drift) due to their temperature dependence. However, some sensing elements, such as for example 6H-SiC and 4H-SiC piezoresistors, are able to work at temperatures of 600 °C [17, 18]. Thin film piezoresistors have had increased attention from the research community recently with materials such as In_2O_3-SnO_2 and Pd-Cr operating at temperatures in excess of 1100 °C [19, 20].

2.3 Temperature sensors

In order to measure temperature, devices called thermometers either contact the measured object or medium directly so that they have nearly the same temperature, or they receive a portion of electromagnetic radiation emitted from the measured object and measure the amount of thermal radiation using an electronic temperature sensing element [1]. The first of these approaches is contact temperature

measurement and requires the sensor to be in direct contact with the sensed medium or object. Non-contact measurement detects the temperature by estimating the energy emitted in the infrared range of the electromagnetic spectrum [21]. This measurement type requires specific construction of the optical system and engineering of optical parameters of the measured surface and can be performed at distance by directing the focusing optical lens (and the sensitive element) towards the radiation source.

The important effects of temperature are changes in the properties of the material including density, vapour pressure and stress, all of which require a secondary transduction to be measured electrically. These are employed in devices such as liquid-in-glass thermometers, manometric thermometers and various mechanical thermometers based on bimaterial strips or shape-changing indicators [2, 9]. This section will provide a review of widely used thermometers in which temperature is measured electrically, with a focus on the temperature range of their applications, selection of materials, production methods and constructions that enable sustained operations at high temperatures and have a potential integration possibility.

2.3.1 Integrated circuit-based thermometers

A p-n junction is formed at the interface between volumes of semiconductor doped with acceptor (p-type) and donor (n-type) atoms [22]. A semiconductor junction temperature sensor is based on the fact that the forward voltage of a p-n junction is temperature-dependent as described approximately by following equation:

$$V_F = m\frac{kT}{q}\ln\left(\frac{I_F}{I_S}\right), \text{ (V)} \tag{2.8}$$

where m is ideality factor, k is Boltzmann constant, q is electron charge, I_F is forward current and I_S is reverse saturation current. Because saturation current increases exponentially with higher temperatures, to eliminate additional variation due to the temperature, a bandgap reference is usually utilized to produce voltage that is proportional to the temperature only [2]. By comparing bandgap voltages of two identical bipolar junction transistors at the same temperature, but at two different

currents, voltage produced between base and emitter of the transistor is linearly proportional to absolute temperature and is controlled by a ratio of forced collector currents I_{C1} and I_{C2}:

$$\Delta V_{BE} = m\frac{kT}{q}\ln\left(\frac{I_{C1}}{I_{C2}}\right), \text{ (V)} \tag{2.9}$$

Evident benefits from such thermometers, such as implementations using standard integrated diodes or diode-connected bipolar transistors and monolithic integration with measured power devices, are inherited from well-defined semiconductor processes and technology [2]. The drawback of integrated circuit-based temperature sensors is their application temperature range, for example, devices fabricated using silicon technology are typically used up to 150 °C, gallium arsenide technology – in cryogenic temperatures and up to the room temperature [22, 23]. Wider bandgap semiconductors, such as silicon carbide or gallium nitride, can be used to decrease the saturation current and hence increase the useful temperature range [24].

2.3.2 Thermoelectric sensors: thermocouples

Thermoelectric sensors are based on measuring a temperature-dependent voltage that results from the thermoelectric effect. The thermoelectric effect defines the function of temperature-sensing thermoelectric devices and describes how electrons diffuse from the hot end towards cold end of a conductor. Charge carriers will accumulate in the cold region, as illustrated in Fig 2.3.1, and when the conductor is in open-circuit condition the electric potential (or electromotive force) will be formed between hot and cold ends. The quantitative expression that describes the voltage gradient between hot and cold boundaries in the conductor is shown in Eq. (2.10) below:

$$\nabla E = -S(\Delta T)\nabla T, \text{ (V) [25]} \tag{2.10}$$

where S is the approximated Seebeck coefficient value between two temperatures. The Seebeck coefficient, usually expressed in $\mu V \cdot C^{-1}$, defines the potential difference induced by thermoelectric effect. Two features of the thermoelectric effect

describe the benefits as well as the requirements for the entire thermoelectric transducer-based temperature measurement setup [25]:

- If the material is homogeneous, then the generated voltage only depends on the difference between hot and cold end temperatures;
- If the temperature gradient does not exist the Seebeck voltage is zero.

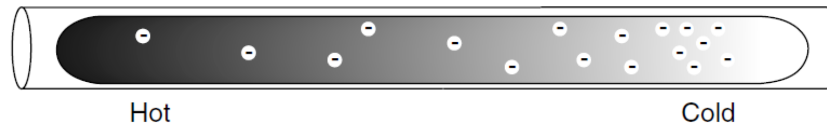

Figure 2.3.1: *Illustration of thermoelectric effect [25].*

Thermoelectric principles are applied to cases when two and more materials are used as conducting wires, for example, when the thermoelectric voltage between cold junctions of materials *A* and *B* forming a thermocouple is measured at some distance away from the junctions. Identical wires made of another material (*C*) can be used to extend the measurement circuit to voltmeter inputs (as illustrated in Fig. 2.3.2) without affecting the measured value if the contacts at the reference junction and the voltmeter terminals are at the same temperature.

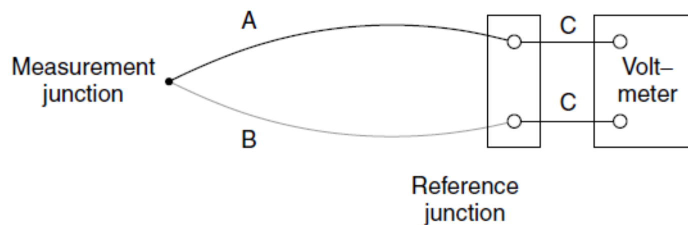

Figure 2.3.2: *Illustration of thermoelectric measurement circuit using conductors from three different materials [25].*

Table 2.3.1 summarises the emf experienced in different pure metals and metal alloys (as for example, material A in Fig. 2.3.2) when using a junction at 100 °C with platinum (material B) and maintaining the reference junction at T_{REF} = 0 °C [26]. The expected emf values between any two materials from the table for the same conditions can be found using subtraction, for example, the Type K thermocouple

junction (90% Ni-Cr – Ni-Al-Mn-Si) will generate a thermoelectric potential of 4.1 mV at 100 °C.

Table 2.3.1 *Comparison of emf at 100 °C for different materials referred to Pt.*

Material	*emf, mV*	*Material*	*emf, mV*
Co	-1.33	*55% Ni, 45% Cu*	-3.51
Pd	-0.57	*Ni*	-1.48
Al	+0.42	*95% Ni, 2%Al, 2% Mn, 1% Si*	-1.29
Pb	+0.44	*94% Pt, 6% Rh*	+0.61
Ir	+0.65	*90% Pt, 10% Rh*	+0.645
Ag	+0.74	*70% Pt, 30% Rh*	+0.647
Cu	+0.76	*Rh*	+0.70
Zn	+0.76	*W*	+1.12
Au	+0.78	*Fe*	+1.98
Mo	+1.45	*90% Ni, 10% Cr*	+2.81

Preferable properties of materials used to produce thermocouples are [2]:

- Low thermal conductivity to limit the heat transfer across the circuit to maintain a large temperature gradient.
- Low resistivity and temperature coefficient of resistance values to minimise Joule heating and make heating constant at different temperatures.
- High and linear Seebeck coefficient over a wide temperature range to improve the sensitivity to temperature.
- Thermal stability of the junction in the specified temperature range for the combination of materials and chemical resistance of each material to environmental effects.

Three categories of thermocouples exist, most of which have become industrial standards: base metal standard thermocouples, rare metal standard thermocouples and non-standard thermocouples [25]. Base metal thermocouples use nickel as alloy base metal and therefore oxidise easily, in particular *Type E* uses Ni-Cr and Ni-Cu alloys, *Type J* – Fe and Fe-Ni alloy, *Type K* – Ni-Cr and Ni-Al-Mn-Si alloys, *Type N* – Ni-Cr-Si-Mg and Ni-Si-Mg alloys, and finally, *Type T* uses Cu and Cu/Ni alloy. These combinations result accordingly with different performance in harsh environments [25]. Rare metal thermocouples do not readily undergo significant

changes at high temperatures because they use Pt and Pt-Rh alloys. The evident drawback of thermocouples with such metal systems is rather low sensitivity of up to 10 $\mu V \cdot °C^{-1}$ [25]. Thermocouples that use W-Rh alloy are an example of non-standard thermocouples, which provide reliable temperature measurements up to 2400 °C, but at the same time are not usually used below 400 °C due to low Seebeck coefficient values at the lower temperature range [25].

Thermocouples that use materials which are a problem in harsh environments can be protected by sheaths and insulating materials that demonstrate improved performance, as illustrated in Fig. 2.3.3, which increases the device size [25]. Protecting sheaths can be metal, ceramic, porous ceramic or composites of ceramic and metal (cermet). Cermets are most optimal as insulating materials because they offer reasonable mechanical strength, high resistance to thermal shock and are robust at high operating temperatures [26].

There are also thin-film miniaturized thermocouple variants that are produced using metal evaporation or sputtering. They allow high speed temperature measurements where standard thermocouples would exhibit thermal lag, while providing an option to have the thermocouple device deposited or attached directly on the measurement surface [9, 27]. However, since Seebeck coefficient is entirely dependent on performance and integrity of materials, thin-film thermocouples have issues with long-term measurement stability and repeatability [28]. Also due to the limited area a reference junction cannot be implemented on chip in thin-film thermocouples because temperature would be practically the same across the chip.

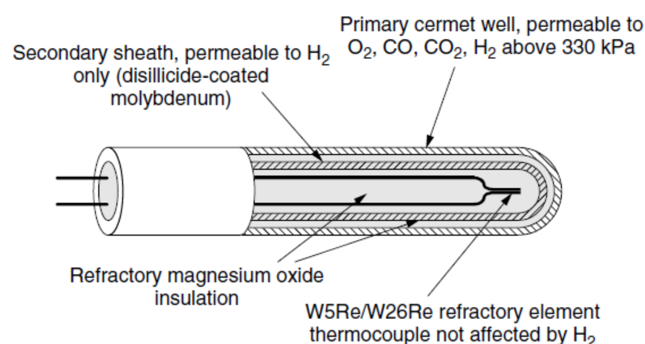

Figure 2.3.3: *Insulated and sheathed thermocouple construction example [25].*

Due to the principles of temperature measurement using thermocouples, the requirement for a reference junction can be fulfilled in several ways [2, 25, 26]. The actual reference temperature is not required to be 0 °C because it is possible to compensate the absence of cold junction numerically or electrically. When a single reference junction is applied it is required that it stays at the same temperature, while thermocouple readers usually create a dual reference junction where the temperature of the most distant reference is measured internally, and the according electromotive force difference between measured temperature T_R and designed reference T_0 is compensated for [2, 25].

2.3.3 Thermoresistive sensors: resistance thermometers and thermistors

Thermoresistive sensors are based on measuring a change of electrical resistance from a nominal value in response to temperature. The usual measurement of a thermoresistive sensor involves applying a constant current and measuring the resulting potential difference [2]. This applies to both types of thermoresistive devices – resistance thermometers and thermistors.

Metals are good electrical conductors because of the presence of free electrons that can drift readily in a response to applied electric field. There are two basic electron scattering mechanisms that increase the resistance of metallic materials to electron flow. The atoms that constitute the crystal lattice constantly vibrate around their positions in the lattice and drifting electrons collide with them, this is a phenomenon termed lattice scattering [29]. The amount of these vibrations and resultant resistance to flow of electrons is a function of temperature and changes in proportion to the absolute temperature value. Another mechanism is impurity scattering, where defects and impurities present in the crystal lattice cause additional resistance to electron flow [29]. A rule that describes the effect of many scattering sources on electron mobility, termed the Matthiessen's rule, provides a very close general approximation of mobility value in following equation [2]:

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_{temperature}} + \frac{1}{\mu_{defects}} + \frac{1}{\mu_{impurities}}, \ (\mathrm{V \cdot s \cdot m^{-2}}) \tag{2.11}$$

A large proportion of defects can be eliminated by annealing, i.e. heating the material to a specific temperature and then cooling in a controlled manner, but key to reducing scattering effects down to a temperature-only dependence are proper material selection and fabrication methods. The resistivity of metal ρ, which is defined by charge elementary value q, concentration n and mobility μ, can then be approximated as [2]:

$$\rho = \frac{1}{qn\mu} = \rho_0(1 + \alpha\Delta T),\ (\Omega\cdot\text{m}) \tag{2.12}$$

where ρ_0 is the resistance at the reference temperature T_0, α is the linear temperature coefficient of resistivity (defined specifically for T_0) and ρ is the resistivity at $T = T_0 + \Delta T$. Table 2.3.2 shows the resistivity and temperature coefficient of resistivity of some pure metals, which could be potentially used as temperature sensitive materials [30].

Table 2.3.2 *Resistivity and TCR of example metal materials.*

Material	*Resistivity at 20 °C, 10^{-8} Ω·m*	*TCR, 10^{-3} °C^{-1}*
Ag	1.6	4.1
Al	2.7	4.5
Au	2.2	4.0
Cu	1.7	4.3
Fe	10.1	6.5
Ni	6.9	6.8
Pb	20.6	4.2
Pd	10.8	4.2
Pt	10.6	3.9
Sn	12.6	4.6
Ta	13.5	3.5
W	5.4	4.8
Zn	6.0	4.2

Resistance temperature detectors (RTD) are essentially temperature-sensitive resistors with a highly linear relationship between temperature and measured resistance [2]. RTDs are usually fabricated from high-purity wires and films of platinum, nickel and copper, but because of different material resistivity and application temperature ranges, devices usually have different nominal values from

9 to 1000 Ω [31]. Constant current of an order of 1 mA is usually applied through RTDs and temperature is measured through the millivolt-order change of measured voltage. Curve-fitting equations can be used to establish the temperature value. Nickel possesses the highest temperature coefficient of resistance ($\alpha_{Ni} \approx$ 6720 ppm °C^{-1}), but its application temperature is limited to 300 °C due to eventual non-linearity of TCR, and copper has a higher TCR ($\alpha_{Cu} \approx$ 4270 ppm °C^{-1}) than that of platinum ($\alpha_{Pt} \approx$ 3850 ppm °C^{-1}). Copper RTD wire is used up to 150 °C respectively due to its susceptibility to oxidation and as a result worse resistance tracking and TCR degradation. Platinum is considered an indispensable material for manufacturing RTDs, which operate at temperatures up to 650 °C providing a long-term, nearly linear response to the temperature.

Different applications for platinum resistance thermometers have specific requirements for precision, temperature range and deployment, and therefore there are several types of RTDs with different constructions. Standard platinum resistance thermometers (SPRT) are very accurate reference devices, usually made from loosely wire-wound elements on a cross-shaped support (similar to Fig. 2.3.4(a)) with maximum possible and reproducible TCR values ($\alpha_{Pt} \approx$ 3926 ppm °C^{-1}) allowing operation up to 1000 °C. Secondary SPRTs have a similar construction and are produced using a one grade lower platinum wire ($\alpha_{Pt} \approx$ 3916 ppm °C^{-1}) and are able to operate up to 500 °C. Industrial PRT devices allow maximum durability of all sensor types while protecting from undesirable environmental effects, with coiled high purity platinum wire ($\alpha_{Pt} \approx$ 3850 ppm °C^{-1}) sensor construction (refer to Fig. 2.3.4(b)) allowing highest possible temperature range of 650 °C [2, 29].

The RTD devices described above use larger footprint size constructions and they can be miniaturised further at the cost of precision. As shown in Fig. 2.3.5(a), flexible wire-wound RTDs can be embedded between non-conductive foil, which can be applied directly to shaped measured surfaces and used in a temperature range of higher than 200 °C [32]. Thin film PRTs, as shown in Fig. 2.3.5(b), are deposited onto suitable substrates allowing temperature measured in a range of up to 600 °C [32]. Thin-film platinum RTD devices have nominally higher resistances, but the

increased strain and sub-micron thickness of platinum have a negative effect on RTD resistance and TCR as described in literature sources [33, 34].

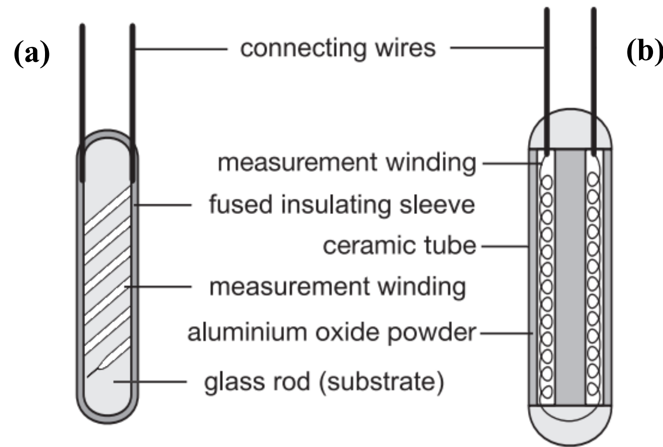

Figure 2.3.4: *Simplified construction of platinum resistance thermometer probes: (a) with wire-wound sensitive element; (b) with coiled sensitive element. Adapted from [32].*

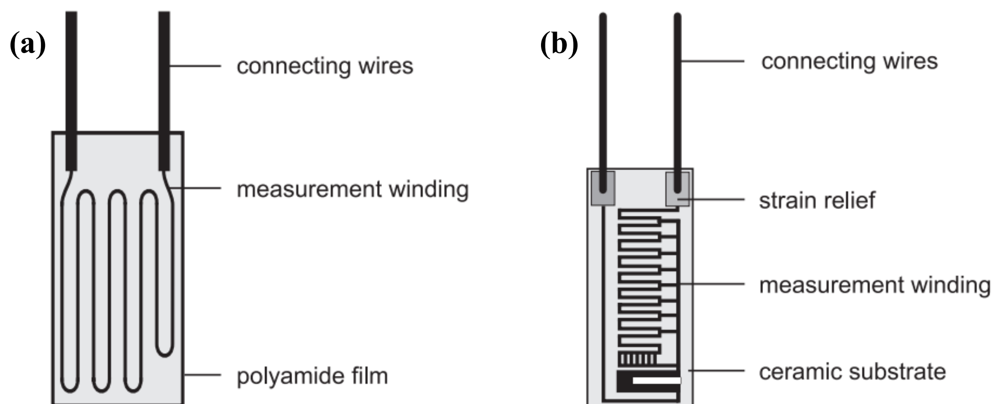

Figure 2.3.5: *Simplified construction of platinum resistance thermometer devices: (a) wire-wound sensitive element in foil; (b) thin film sensitive element [32].*

Platinum RTDs in high temperature environments can be measured remotely using two-wire, three-wire or four-wire circuits [21]. When the sensitive element is measured using a circuit similar to that depicted in Fig. 2.3.6(a), the additional resistance of the connecting wires, which also have their own TCR, is introduced. This results in a higher measured and interpreted temperature value and, at the maximum of temperature range, a significant error in measured value. Three-wire measurement, as shown in Fig. 2.3.6(b), uses an additional identical wire to measure voltage at node B which balances the effect of connecting wires (parasitic wire

resistance and its TCR) between the upper and lower resistances of a bridge arm that contains the RTD element.

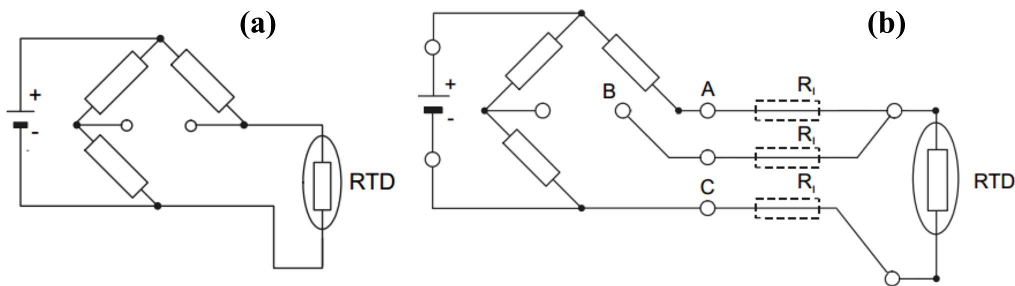

Figure 2.3.6: *Wheatstone bridge used to measure temperature sensitive elements using: (a) two-wire; (b) three-wire connection [35].*

Since the circuit that is used to measure the temperature response of the sensitive element is one of most important sources of inaccuracy in the measurement, and temperature uniformity and identical lead resistance requirements cannot be always satisfied, usually the four-wire measurement is employed to measure a single RTD accurately [29]. Four-wire measurement (Fig. 2.3.7) is effectively a Kelvin measurement, which allows to force the current through a circuit with the RTD and measure the voltage drop pertaining only to the resistance of the sensitive element (there is no current passing through the voltage taps) [35].

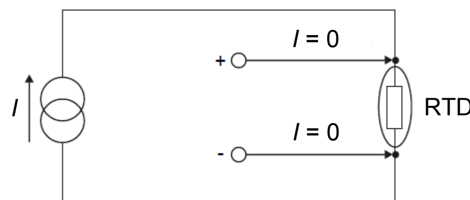

Figure 2.3.7: *Four-wire connection used to measure RTD element [35].*

Unlike resistance thermometers based on metals, thermistors are semiconductor bulk effect devices and as a result they have larger temperature coefficient of resistance (TCR) that resistance temperature detectors (RTD) [9]. Thermistors are classified into two categories describing the sign of their temperature coefficient, namely, positive (PTC) and negative (NTC) temperature coefficient thermistors [21]. Normally thermistors are expected to have higher rated resistance values than that of

RTDs. This results in better resolution of measured temperature, but the conversion of the measured resistance value is not as straightforward because its dependence on temperature is non-linear. Also there are no standard resistance characteristics and each thermistor model will usually have its own calibration curve [2, 21].

NTC thermistors are fabricated from mixtures of different compound oxide semiconductors based on Co, Cu, Fe, Mn, Ni, Ti and Zn (for example, $NiMn_2O_4$), and the resistance-temperature characteristics of these materials approximate the behaviour of intrinsic semiconductors. They have a nearly logarithmic response to the inverse of absolute temperature, which means that the coefficient of resistance is not constant across the complete temperature range and such thermistors have to be compensated [2, 23]. Usually the high temperature range of NTC thermistors does not exceed 300 °C because the thermistor resistance reaches the limiting value and it becomes insensitive to temperature, but tin oxide thick film processes have been shown to produce NTC thermistors that are able to withstand the temperatures of up to 1000 °C [36]. The approximate NTC thermistor resistance value will follow the exponential form:

$$R = R_0 e^{\frac{\beta}{T}}, \ (\Omega) \tag{2.13}$$

where R is the resistance at temperature T, and β is a material-dependent constant specific for the reference temperature value T_0 at which resistance is equal to R_0. Hence, parameter β can be expressed as:

$$\beta = \frac{T_0 T}{T_0 - T} \ln\left(\frac{R}{R_0}\right), \ (\text{°C}) \tag{2.14}$$

From Eq. (2.13), the temperature coefficient α for a thermistor device can be written down as [9, 29, 37]:

$$\alpha = \frac{1}{R}\frac{\Delta R}{\Delta T} = \frac{-\beta}{T^2}, \ (\text{°C}^{-1}) \tag{2.15}$$

yielding another expression for the measured resistance:

$$R = R_0 e^{\alpha \Delta T \left(\frac{T_0}{T}\right)}, \ (\Omega) \tag{2.16}$$

Silicon PTC thermistors rely on bulk properties of the semiconductor, producing an approximately linear response to temperature [2]. Doped silicon PTC thermistors

(silistors) can have a fairly linear temperature response of 7000 to 8000 ppm °C^{-1} and rely on the bulk properties of doped silicon [2]. A typical silistor application temperature range is up to 150 °C, with some examples of silistor devices able to perform at 300 °C. Higher temperature ranges of up to 450 °C can be provided by thermistors fabricated using silicon carbide polycrystalline film, which has a large, negative temperature coefficient of resistance [38].

Another type of PTC thermistors has resistance-temperature characteristics with negative TCRs of order of –10000 ppm °C^{-1} over most of the operable temperature range which can only be useful as a high resolution thermometer only in a limited temperature range (starting with a 'switch' temperature), where its TCR becomes positive with a value of as high as 1-2 °C^{-1} [2]. This thermistor type is usually fabricated using ceramic barium, lead and strontium titanates, which are doped to become semiconductive and are ferroelectric [23]. The mechanism behind a sudden increase of TCR in switching thermistors lies in the decrease of dielectric constant in ferroelectric compound oxides with increasing temperature when the Curie temperature is exceeded [9]. The typical temperature range of such devices does not exceed 150 °C, whereas TCR and temperature range values will vary depending on the composition of ceramic, which makes it less practical to use such a PTC type for wide temperature range measurements [2].

A standard approach for measuring temperature using thermoresistive sensing elements is to apply a constant current to a linear resistive element and measure a linear response to temperature [2]. The evident drawback of thermistor devices when used as a thermometer is their non-linear α coefficient across the temperature range. The red line in Fig. 2.3.8 illustrates the temperature response characteristic produced by an NTC thermistor, which is created using a 10 μA excitation current. The example NTC is specified to have a resistance of 10 kΩ at 25 °C and knowing specific values around temperature range of interest enables sensitivity and response linearity compensation through addition of precision resistors in series or parallel with the thermistor (as for example 10 kΩ resistor in Fig. 2.3.8(a)) [2, 39]. Further linearization is carried out by creating a network of identical thermistors (similar to

Fig. 2.3.8(b)), which will further decrease the effect of each of thermistors on designed sensitivity plot and maxima in the circuit's temperature response.

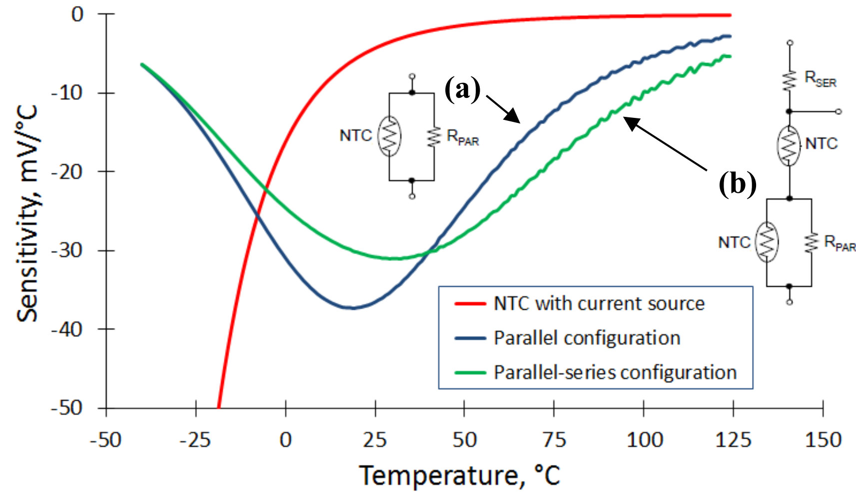

Figure 2.3.8: *Example of linearization circuit effects on sensitivity of temperature response produced by (a) parallel and (b) parallel-series configuration. Adapted from Baker in [40].*

2.3.4 Infrared radiation sensors: infrared thermometers

Infrared light is electromagnetic radiation (700 nm to 1 mm) with a longer wavelength than light in the visible spectrum but shorter than microwave radiation [2]. IR light can be reflected, filtered, absorbed etc. according to laws of optics. Since temperature is a measure of average kinetic energy, it is possible to determine the temperature of a remote surface from the intensity and wavelength of thermal infrared radiation (0.7 to 15 μm).

The relationship between intensity of infrared radiation at particular wavelength λ and temperature T is described by Planck's radiation law, where the power of electromagnetic radiation per unit wavelength is expressed as:

$$W_{\lambda} = \frac{\varepsilon(\lambda) C_1}{\pi \lambda^5 \left(e^{C_2 / \lambda T} - 1 \right)}, \text{ (W·m}^{-2}\text{·μm}^{-1}\text{) [2]} \qquad (2.17)$$

where $\varepsilon(\lambda)$ is emissivity of the object, $C_1 = 3.74 \cdot 10^{-12}$ W·cm^{-2} and $C_2 = 1.44$ cm·K. The emissivity ε in Eq. (2.17) describes the effectiveness of the surface of an object

in emitting thermal radiation as compared to an ideal emitter (black-body) at the same temperature. According to Kirchhoff law, it is related to other two basic properties reflectivity ρ and transmissivity τ through:

$$\varepsilon + \rho + \tau = 1, \qquad (2.18)$$

and since most of objects used in radiation thermometry are opaque to IR radiation, τ can be zero. Integrating Eq. (2.17) from λ_1 to λ_2 gives the equation expressing power radiated from object with surface area A described by the Stefan-Boltzmann law, where emissivity ε is independent of wavelength, but is less than unity:

$$P = A\varepsilon\sigma T^4, \text{ (W)} \qquad (2.19)$$

where Stefan-Botzmann constant σ = 5.67 · 10^{-8} W·m^{-2}K^{-4} and T is absolute temperature.

An approximation of Eq. (2.17), which is known as Wien's law, leads to the expression of the midpoint of spectral response of an infrared thermometer device, which is termed Wien's displacement law:

$$\lambda_{\max} = \frac{2898}{T}, \text{ (µm)} \qquad (2.20)$$

It is evident from Eq. (2.20) that the hotter the object is, the shorter is the central wavelength of infrared emissions by it.

Different types of infrared thermal detectors exist, which are based on a variety of transduction effects, although they do not necessarily exhibit direct conversion of infrared radiation into an electrical signal. Electronic thermal radiation detectors react to thermal radiation that the surface of the sensing element is exposed to. This increases the surface temperature and this increase becomes a measure of thermal radiation coming from the measured object [2]. Thermal transducers can be based on thermoelectric (thermopile) or pyroelectric (pyroelement) effects [3, 41]. Thermal sensors used for IR detection can be thermoresistive (RTD or thermistor bolometer), piezoresistive (strain gauge), or opto-acoustic (Golay cell), and can also be based on semiconductor junction temperature sensing principles (bolometer) [41]. The majority of infrared detectors measure the difference between the radiated power from the black-body being measured and the detector, which by applying Eq. 2.19 can be expressed as:

$$P_m = A\varepsilon_B\varepsilon_D\sigma\left(T_B^4 - T_D^4\right), \text{ (W) [2]} \qquad (2.21)$$

where A is the area of detector, and σ is the Stefan-Boltzmann constant, while ε_B,ε_D and T_B,T_D are respectively the emissivity and temperature values of the detector and the measured black-body. Equation 2.21 shows that any energy absorbed in the infrared spectrum causes a response at the detector; hence any difference from detector temperature should be measurable [21]. The expression of temperature measured by passive IR detectors can be found by manipulating Eq. (2.21) into Eq. (2.22). In order to measure the temperature of a blackbody, T_B, active IR sensors keep the temperature of the sensor element T_D constant at a value which is ΔT above ambient, through heat transfer from a heater element with electrical resistance R, produced by an applied voltage V, performed with a loss of heat due to loss factor α_S:

$$T_B = \sqrt{T_S^4 - \frac{1}{A\sigma\varepsilon_B\varepsilon_D}\left(\frac{V^2}{R} - \alpha_S\Delta T\right)}, \text{ (°C) [2]} \qquad (2.22)$$

Bolometers are miniature RTD or thermistor devices which are generally used for measuring RMS values of electromagnetic radiation over a very broad spectral range [2]. External power needs to be applied to convert resistance changes to voltage changes. It is advantageous to use miniature thermistors due to their higher sensitivity to temperature as compared to RTDs. For example, polysilicon is an attractive material due to its additional compatibility with CMOS processing, but some infrared thermometers use thin film nickel chromium or platinum resistor elements as detectors [9]. Thermopiles and pyroelectric elements are commonly used as detectors in IR thermometers [3]. Thermopile sensors are based on the thermocouples electrically connected in series, providing multiple junction pairs and increasing the response to temperature [2, 9]. An efficient and reliable thermopile sensor usually incorporates a semiconductor (for example, Si) as the thermoelectric material. The transduction from radiation to heat is carried out by a blackbody absorber and black coating for infrared detectors can be produced using silicon dioxide or nitride processes. Alternatively, porous thin metal coatings can be fabricated using modified thin film deposition processes [2].

Pyroelectric sensing elements are based on measuring the value of a capacitor which is charged by an influx of heat. Contrary to thermoelectric effect, which

produces a constant voltage at a measurement junction that is kept at certain temperature, the pyroelectric effect produces a charge in response to a change of temperature (e.g. when the sensor is heated or cooled). Pyroelectric materials are used as thin slices of crystalline material or as films to produce the detector [1]. Some pyroelectric materials are ferroelectric and therefore have to be poled in order to become useful for pyroelectric applications in a similar way to piezoelectric applications [2]. Typical pyroelectric materials used for PIR measurements involve PZT, lithium niobate and lithium tantalate, with the latter being preferable because of a combination of significantly high Curie temperature and high pyroelectric coefficient values [21, 42]. Table 2.3.3 summarizes the pyroelectric coefficients for a number of example materials, where the given values are a combination of a primary pyroelectric effect and a contribution of piezoelectricity due to thermal expansion and strain, as most pyroelectric materials have some degree of piezoelectric properties [43].

Table 2.3.3 *Comparison of pyroelectric coefficient and Curie temperature values for example materials.*

Material	*Form*	Pyroelectric coefficient, 10^{-3} C·m^{-2}K^{-1}	Curie temperature, °C
$(NH_2CH_2COOH_4)_3$-H_2SO_4	*Single crystal*	0.35	49
$LiTaO_3$	*Single crystal*	0.2	618
$BaTiO_3$	*Polycrystalline*	0.4	120
$(CF_2CH_2)_n$	*Polycrystalline*	0.04	205
$PbZr_{0.6}Ti_{0.4}O_3$	*Polycrystalline*	0.042	340
$PbTiO_3$	*Polycrystalline*	0.23	470

A basic type of radiation thermometer – disappearing filament pyrometer – is based on one of oldest, manual pyrometry principles, but is still considered as an accurate thermometer for temperatures exceeding 700 °C [2, 3]. Its working principle is based on comparing the radiance of a measured object and that of a tungsten filament that is heated controllably by electric current to a temperature that makes it glow. The value of electric current measured when the filament becomes indiscriminable from the observed surface is used to provide an estimation of

measured surface temperature [2]. The evident drawbacks of this method lie in the facts that measurement results depend on the subjectivity of the operators' colour perception and also that tungsten filaments can only be used up to 1400 °C [44]. Red and neutral density filters are used to solve these problems by limiting the observed wavelength and decreasing the radiance, thus decreasing the minimum possible measured temperature to its lowest possible value and extending the measured temperature range up to 4000 °C [45]. A ratio pyrometer is based on estimation of spectral radiance at two different wavelengths. A two-colour red-green filter is adjusted until the measured surface appears to be grey so that eventually, with an increase of temperature, the relative radiance at the green wavelength is increasing [45]. Colour temperature is read from a measurement scale, which usually covers the range from 700 to 2200 °C. The operator can be replaced with photoelectric detectors followed by improvements in device construction, which increases the temperature range up to 3100 °C [2].

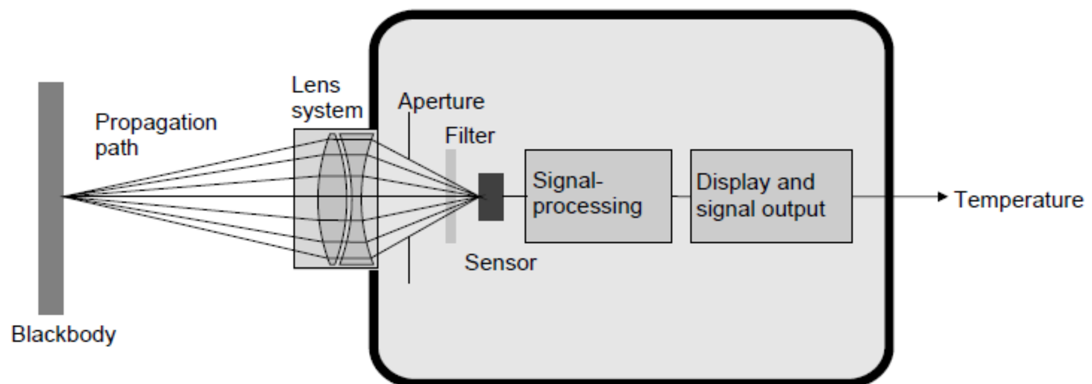

Figure 2.3.9: *Schematic construction of automatic pyrometer [3].*

More than one type of automatic pyrometer exists, but the usual structure of automatic thermometers based on pyrometry is as demonstrated in Fig. 2.3.9 [3]. The majority of automatic pyrometers are based on spectral band thermometry [45]. A pyrometer based on this principle measures the radiance over a narrow band of wavelengths providing a radiance temperature value that gives the temperature of an ideal blackbody (which is also wavelength dependent), while the wavelength range is determined by filters [46]. There are scenarios when the measured surface becomes

unreachable for a bulky pyrometer and there is an option to use optical fibres as a medium for radiance propagation [45]. With the use of appropriate material (such as artificial sapphire) this approach offers a measurement range of 250 to 2000 °C, as with pyrometer alone. An alternative infrared thermometer is a band radiation pyrometer, which is similar, but detects the radiance in a wider band, improving the temperature measurement capabilities to 3000 °C [45]. Multiple wavelength pyrometers compensate for limitations of most pyrometer types and make it possible to measure surfaces with low emissivity. They detect the radiant temperature at multiple wavelengths to produce a better approximation of measured temperature, but this limits the application temperature to 1700 °C. Finally, a total radiation pyrometer, which uses electronic thermal detectors (as opposed to photoelectric detectors) can be used to measure temperatures as low as 0 °C and up to 2000 °C, but not as precisely as other mentioned automatic pyrometers [45].

2.3.5 Fibre optic sensors: fibre optic-based thermometers

Maxwell's equations describe the nature of the propagation of electromagnetic waves and serve as groundwork for expression of the phase velocity of light waves in a medium:

$$c = \frac{1}{\sqrt{\mu_0 \varepsilon_0 \mu_r \varepsilon_r}}, \ (\text{m} \cdot \text{s}^{-1}) \tag{2.23}$$

where $\mu_0 = 4\pi \cdot 10^{-7}$ H·m^{-1}, $\varepsilon_0 = 8.854 \cdot 10^{-12}$ F·m^{-1}, the ideal vacuum magnetic permeability and electric permittivity while μ_r, ε_r are respectively the, dimensionless, relative permeability and permittivity [1]. The refractive index n is used to describe the ratio of velocity of light in a perfect vacuum c_0 to that of a medium with different relative electromagnetic parameters:

$$n = \frac{c_0}{c} = \frac{1}{\sqrt{\mu_r \varepsilon_r}} \tag{2.24}$$

This is a wavelength-dependent property, which is observed through a phenomenon termed dispersion. An optical waveguide can be used to transfer electromagnetic waves that are confined in a higher refractive index core by means

of total internal reflection from the surrounding material when the angle of refraction is higher than the critical ϑ_c value that is described by the following solution of Snell's law:

$$\vartheta_c = \arcsin\left(\frac{n_2}{n_1}\right), \ (°) \tag{2.25}$$

where n_1 is refractive index of the core and n_2 is lower refractive index of surrounding material.

Optical fibre is a dielectric light guide with a circular cross-section, which structurally consists of a core and a lower refractive index cladding, which is commonly used for wavelengths in the range from near-UV to near-IR (380 to 2500 nm) [47]. Optical fibres can be used for sensing because factors of the environment such as force and temperature applied to the fibre can change the propagation of light within the fibre [47]. Optical fibres can be utilized for sensing in two modes: the first mode uses the same fibre to transmit the excitation signal and collect the response signal and another mode has separated transmitting and receiving fibres [9]. Fibre optic sensors are categorized by the purpose of the optic fibre – when it is used as a medium for signal transfer from the sensor to electronics, an optical sensor is considered to be extrinsic, and when the measured environment affects the light beam while it is in the fibre, i.e. the latter serves as a sensitive element, it is called an intrinsic sensor [4]. Extrinsic sensors can be based on phenomena such as absorption, reflection, optical interference, thermal radiation or fluorescence [4, 47]. Intrinsic sensors are usually based on optical scattering, interference, Fresnel reflection or change of refractive index [2].

Optical fibre is usually produced from quartz (SiO_2, $n \approx 1.45\text{-}1.7$) by modern vapour deposition techniques, which gradually decreases the cost of fabrication and allows fibre optic-based thermometers to enter the market. Modifications of refractive index in the core and sheaths used to protect the fibre from harsh environments are application specific [48]. Sheathed quartz optic fibre is able to withstand temperatures exceeding 1000 °C and artificial sapphire (Al_2O_3) can be considered as an alternative to quartz for temperature sensing due to improved corrosion resistance and higher melting point [49]. However, current growth methods

do not allow producing a single mode fibre or cladding. This makes the lower refractive index air serve as a cladding and results in making the fibre multimode.

One of the optic fibre thermometer types that benefited from using sapphire as an optical fibre was fiber Bragg grating-based spectrometric thermometer [49]. This thermometer type contains gratings formed in the optical fibre core in a pattern that creates a periodic variation of refractive index in the fibre core and as a result produces refraction around a specific wavelength (~1 nm bandwidth). The shift of response signal wavelength $\Delta\lambda_B$ can be used to measure the change of temperature ΔT, but it is also affected by strain through an increase of grating length Δl:

$$\Delta\lambda_B = 2\Delta l\left(\Lambda\frac{\partial n}{\partial l} + n\frac{\partial\Lambda}{\partial l}\right) + 2\Delta T\left(\Lambda\frac{\partial n}{\partial T} + n\frac{\partial\Lambda}{\partial T}\right), \text{ (nm)} \tag{2.26}$$

where Λ is the grating pitch and n is the refractive index of the core dielectric. Most stable at high temperatures are Type II gratings produced using femtosecond lasers, which enable measurements of temperature values as high as 1200 °C, while the measurement capability is physically limited by SiO_2 fibre brittleness at temperatures higher than 1000 °C [49, 50]. Using sapphire optical fibres facilitates measuring temperatures slightly higher than 1700 C° [49, 50].

Optical interference fibre optic sensors are often used to produce high-precision measurements of physical parameters that affect an external sensitive element [48]. Interference is a phenomenon during which two light waves superpose to produce a wave with different amplitudes depending on phase difference of incident waves [9, 47]. A most common example of such a device is the Fabry-Perot interferometer (FPI), in which interference takes place between the partially reflective cross-section end of a fibre (that creates a reference signal) and an external reflective medium (such as for example – another fibre) that creates a reflection related to sensed parameter. The number of interference fringes shifted, m, and the signal wavelength, λ, can be used to detect when the sensed parameter changes the effective cavity length s by Δs:

$$\Delta s = \frac{m\lambda}{2}, \text{ (nm)} \tag{2.27}$$

The extrinsic fibre optic thermometer based on a Fabry-Perot sensing element (as in Fig. 2.3.10(a)) can utilize the temperature dependence of the spectral reflection

coefficient of a monocrystalline silicon film. Such an FPI-based thermometer has been shown to operate up to 400 °C [47]. Intrinsic Fabry-Perot interferometers using internal mirrors produced by fusion splicing of optical fibres (in a setup similar to as shown in Fig. 2.3.10(b)) have been demonstrated to measure temperatures up to 1050 °C [51]. Furthermore, an FPI interrogated using a broadband light source (as opposed to narrowband laser light) has provided temperature measurement resolution as good as 0.025 °C in a temperature range of 25 to 800 °C [52].

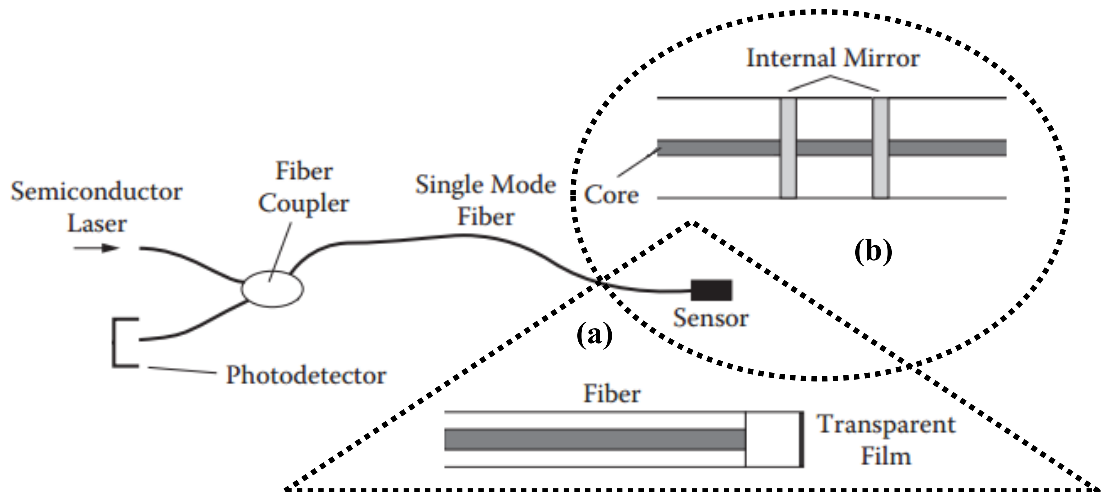

Figure 2.3.10: *Typical arrangement of Fabry-Perot fibre thermometer based on: (a) extrinsic FP sensitive element; (b) intrinsic FP sensor. Adapted from [53].*

Standard optical fibres that use a wide core impose the limitations on material selection for core and cladding, and also characteristics that are non-customisable for sensing applications due to specific refraction index profiles. This has led to emergence of photonic-crystal fibres (PCF). These are typically a pure SiO_2 filament which contains a periodic array of microscopic air holes in the entire length of filament, and as a result having a hollow or a solid core [54]. Such PCFs can be used as interferometric fibre optic thermometers, for example, in one application a solid silica core PCF was tapered to produce a section with no air holes that was exposed to the measured environment [55]. Interference peaks shifted to higher wavelengths with temperature increase and this characteristic was used to produce a response to temperature up to 1000 °C.

Light scattering is a process during which light changes trajectory due to, for example, non-uniformities of dielectric constant, diffraction from particles of different size and interaction with particle vibrations in propagation medium. Several scattering mechanisms are possible when light is propagated in a non-ideal dielectric medium [2, 56]. One example of elastic scattering, during which the frequency of light produced by scattering stays the same as in the original waves and does not transfer energy to the scattering medium, is Rayleigh scattering. This type of scattering is the main reason for light energy losses in optical fibres. Two main examples of inelastic scattering are Raman and Brillouin scattering, which both result in frequency shifts in the scattered light since one is a result of an interaction with molecular vibrations and another – of an interaction with acoustic vibrations of the medium.

The previously described inteferometric and spectrometric fibre optic thermometers are based on the requirement to measure localized temperature, hence they can be categorized as point sensors [4]. It is also possible to measure temperature using fibre optic over a significant distance by using a distributed thermometer consisting of a continuous temperature sensing element in an optic fibre as shown in Fig. 2.3.11 [57]. The response of this array to the modulated signal consists of a pulse frequency shift as a result of temperature change and pulse delay that provides sensing element positional information [56]. A good example of such a sensor was reported that detected the ratio of Raman backscattered and incident light portions while measuring the scattering distance using a reflectometer [47]. A quartz optical fibre protected by carbon and ceramic coating layers was used and as a result temperatures up to 500 °C have been detected at twenty positions along a 20-metre-long fibre. Alternatively, sensors based on Brillouin scattering can offer sensitivity to temperature variations (in a limited, 20 to 60 °C range) with resolution of the order of 1 m along a 50 km optical fibre [58].

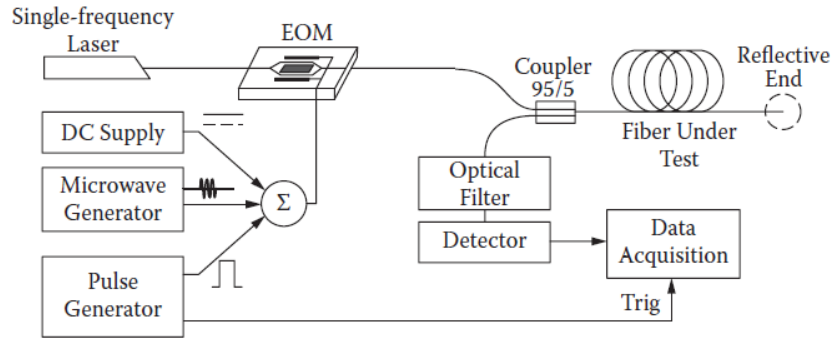

Figure 2.3.11: *Example spectrometric distributed thermometer sensing and detection diagram [57].*

2.4 High temperature thin film elements

The oilfield equipment company Schlumberger defines "high temperature" in the specification of the *ultra-HPHT* (high pressure, high temperature) as a temperature range that extends to 260 °C [59]. Temperatures of up to 315 °C are encountered in some geothermal wells and, rarely, in oil and gas wells [60]. It is problematic to produce resistive elements that would perform sustained operations in high temperature environments especially when coupled with corrosion and vibration [25]. Thin film platinum sensitive elements have numerous advantages over thermocouples and platinum resistance thermometer probes such as long-term stability and intrinsic resistance against vibration [22, 61]. Thin film device layouts are more space efficient, and the small footprint is beneficial for good matching between resistive elements. On the other hand, the values of thin film resistors are highly dependent on thickness as small changes can result in greater variability [62]. Thin film elements can be produced by means of vacuum deposition, and physical or reactive etching. Metallic films can be deposited using low temperature physical deposition while passivation layers can be produced by plasma-enhanced CVD processes at temperatures as low as 300 °C [63]. Table 2.4.1 provides a comparison between metals that can be fabricated as thin films and used for different applications as either temperature insensitive resistor elements or RTDs.

Table 2.4.1 *Comparison of reviewed materials' high temperature properties.*

Materials		*Temperature parameters*		*Ref.*
Purpose	*Name*	*Resistance coefficient* (ppm °C^{-1})	*Maximum temperature* (°C)	
Low TCR	*Ni, 20% Cr*	–50 – 200	350	[64-66]
	CrN	-185	-	[67]
	TaN	±190	-	[37, 68-75]
	TiN	–150 – 540	-	[76-80]
	ZrN	±200	-	[81, 82]
High TCR	*Cu*	4270	240	[83]
	Ni	6370 – 6720	250	[84]
	Pt	3300 – 4100	800	[85-89]

2.4.1 Thin film material selection

Tantalum nitride and platinum were selected for this application because, in addition to the fact that they are available and have the desired electrical characteristics, both materials have high corrosion resistance and overall thermal and chemical stability, as one is a refractory metal nitride compound and another is a noble metal. The success of using a combination of TaN and Pt in the current application depends on deposition results, in particular for TaN, and the resultant composition of films. Tantalum nitride will be produced by reactive sputtering from a pure target because a compound target, typically used in industry, is not available. This can result in inferior characteristics as compared to industrially produced TaN resistors and thin film characteristics can be expected to be different from examples in the literature. More attention should be given to the reproducibility of separate fabrication processes rather than the nominal resistor values because the circuit that combines the materials is ratiometric.

Temperature sensing elements will need to have as high as possible TCR, which is a problematic goal for a thin film implementation [34]. Platinum elements fabricated to a variety of standards have quoted α_{Pt} up to 3925 ppm °C^{-1} [2]. Such SPRTs are usually designed and fabricated to 100 and 1000 Ω standards. A widely

accepted equation based on Callendar-Van Dusen expression according to IEC 60751 standard gives the resistance at temperature T:

$$R(T) = R_0(1 + AT + BT^2) = R_0(1 + 3.9083 \cdot 10^{-3} \times T - 5.775 \cdot 10^{-7} \times T^2), \text{ [2]} \quad (2.28)$$

which remains true in a range between 0 °C (where the element has the rated value of R_0 = 100 or 1000 Ω) to 650 °C (end of maximum linearity range) [29]. When Pt elements are fabricated to this standard, they can be compared against reference tables and applicable tolerance errors can be found. Since every unique set of values of (α_{Pt}, α_{TaN}) and resistor ratio produces a different temperature response, the rated values of TaN and Pt elements are no longer important and it becomes practical to use the resistor ratio parameter. Commercial tantalum nitride and platinum elements are both precision thin film resistors, however, the resistance precision of a device batch can only be ensured by trimming certain devices should their rated values not satisfy the required tolerance distribution [90, 91]. As a result, the rated resistance value and its temperature performance can only be found by measuring each individual fabricated element in the specified temperature range. Commercial Pt RTD devices are required to have accuracy values of 0.06% (R_0 = 100 Ω ±0.06%, ±0.15 °C tolerance at 0 °C) according to Class A of this standard [29]. It is not required to produce such accurate devices during this research because, in addition to added cost of processing and possible manufacturability issues that may arise, the temperature transducer circuit is inherently non-linear. Each newly fabricated device will be specified using the independent linearity definition, which would characterise maximum deviation of measured values relative to a straight line obtained through a least squares fit. Measurement errors could be then estimated at start-, mid- and endpoints of the full-scale range, which by definition of linear least squares fit would be the points in the function with the highest linearity error values for a described bridge circuit. The determined temperature response functions would then be used to convert the measured transducer output value to temperature with a specified precision.

2.4.2 Thin film tantalum nitride phase content adjustment approaches

Tantalum nitride is well known for its stability at elevated temperatures [37, 92-94]. This metallic compound has gained recognition both in industry and research and its most successful application in the electronics area is thin film precision resistors [92, 95]. A TaN thin film has to consist of specific crystal phases i.e. have a certain composition in order to have the necessary properties [69, 96-98]. Reactively sputtered TaN does not have the required stability of electrical properties and is also usually highly amorphous when deposited at room temperature and therefore high-temperature treatment in vacuum has to be performed in order to recrystallize the film and ensure subsequent stability at lower temperatures [37, 95, 99]. Three tantalum nitride phases are considered as stable: hexagonal Ta_2N, hexagonal Ta_5N_6 and orthorhombic Ta_3N_5 and no further phase change is expected to take place after such phases have developed in the film [100]. Other crystalline TaN phases which can be recognised by X-ray diffraction (XRD) method are: cubic $TaN_{0.04}$ and $TaN_{0.1}$, orthorhombic Ta_4N, hexagonal $Ta_6N_{2.57}$, hexagonal $TaN_{0.8}$, cubic and hexagonal TaN, cubic $TaN_{1.13}$ and tetragonal Ta_4N_5. These phases are metastable and are expected to change at some critical temperature value, referred to as the recrystallization temperature.

Commercial tantalum nitride thin film resistors generally use a Ta_2N phase that is known to produce resistance profiles with a low and traceable TCR value. Based on limited information from Vishay Intertechnology, their precision thin film products use tantalum nitride with a sheet resistance value starting at 50 Ω/□ [101]. The TCR values may be positive or negative, but they are specified to be in the range of ±100 ppm $°C^{-1}$ and to be traceable.

A significant amount of information on how to adjust the electrical and structural properties of reactively sputtered tantalum nitride thin films is available in the literature. For example, Na et al. have characterised the properties of as-deposited single-layer and multilayer 200-nm thick tantalum nitride films, where the purpose of the multilayer deposition was to combine negative and positive TCR values of separate layers to produce a TCR close to zero [102]. They provided an example to

validate the approach, but the selection of phases used (β-Ta and Ta_3N_5) was suboptimal, leading to a TCR value of –284 ppm °C^{-1}.

Jiang et al. have shown results of resistance and XRD measurements of 30 to 280 nm-thick films, which were reactively sputtered at 600 °C [72]. A relation between sheet resistance, TCR and thin film thickness has been shown in that work. Riekkinen et al. have demonstrated phase evolution with increasing nitrogen content in film and provided the TCR value of α_{TaN} = –103 ppm °C^{-1} for 44 nm-thick polycrystalline Ta_2N film [68]. Remmel et al. have developed a thin film (R_s = 50 Ω/□) TaN resistor process for integration into a semiconductor fabrication process and have shown an example of an increasing resistivity trend with increasing nitrogen content with an exceptional region where resistivity became lower [103, 104]. The existence of such a region was attributed to a change of preferential crystal structure from tetragonal β-Ta to cubic α-Ta at nitrogen flow values that precede a process region of hexagonal Ta_2N [104]. Akashi et al. published another example of tantalum nitride resistor process integration, where the sheet resistance and TCR values of 110 nm-thick polycrystalline Ta_2N produced at 350 °C are mentioned (R_s = 20 Ω/□, α_{TaN} = 108 ppm °C^{-1}) [69, 105]. Finally, Grosser et al. provide a very useful review of phase evolution with increasing nitrogen gas flow ratio in reactive sputtering processes [106]. These papers, however, have not investigated the high temperature stability aspect of thin film produced by described processes.

Wang et al. have shown the effect of annealing at 400 °C for 2 minutes in an Ar atmosphere on the resistance and TCR of tantalum nitride samples [70]. In the experiment they describe, the TCR was observed to become more negative with an increasing nitrogen flow ratio, and that a region existed with a nitrogen flow ratio of ~11.76% (8:68 sccm), where the rate of change of resistivity and TCR decreased significantly. Chung et al. provided a very useful relationship between the TCR and temperature of a 1 hour vacuum annealing process, however the physical properties of the annealed samples were not measured and sheet resistance values were not documented [107]. It is difficult to fully evaluate the results described in these two papers because thin film thickness and/or deposition time values are not provided and, unfortunately, a comparison of XRD plots of as-deposited and annealed samples

is not available. Cuong et al. have shown in a series of papers an example of process development for a resistor with TCR close to zero, providing an exhaustive amount of data [73-75, 96]. In their first paper the relationships between TCR and the deposition temperature (25 to 400 °C) and phase content in 350 nm-thick films are described [96]. The second paper describes the effect of the temperature (450 °C to 600 °C) of a 3-hour vacuum annealing process on the TCR and the degree of crystallinity of a 350 nm-thick polycrystalline Ta_2N film deposited at 200 °C [73]. Their third paper examined the effect of film thickness (50 to 200 nm) on resultant TCR value of films produced by the same Ta_2N deposition process, which was followed by vacuum annealing at 550 °C for 4 hours [74]. The final paper in the series describes the electrical and structural properties of 50 to 200 nm-thick Ta_2N films produced by deposition at room temperature, followed by vacuum annealing at 525 °C for 4 hours [75]. These last two papers showed an example of how the degree of crystallinity was increasing with film thickness [74, 75]. The information from these papers was used to plan initial experiments related to TaN development.

The load-in and load-out temperatures are extremely important, as suggested by Auger electron spectroscopy measurements by Cuong et al. [75], because the effect of atmospheric gas diffusion may become an unavoidable part of the annealing process. However, most of papers reviewed either ignored this effect or did not describe the annealing process and related preparations in sufficient detail for conclusions to be drawn on the approach taken.

2.5 Summary

This chapter provides a review of high temperature sensing technologies with the focus on electronic thermometers, which are based on direct contact thermoelectric, thermoresistive and fibre optic as well as contactless infrared thermal radiation temperature transduction principles. It also briefly covers sensors employing piezoelectric and piezoresistive transducers of strain and pressure, which given the proper selection of materials can be employed in harsh environments.

The temperature range of piezoelectric sensors is limited by the Curie temperature, at which the material loses the piezoelectric effect. Piezoresistive sensors are usually limited to temperatures up to 300 °C due to decreasing piezoresistivity at high temperatures. The majority of available piezoelectric and piezoresistive sensors and materials are as a result limited in application temperature, but the development of thin film materials, for example, langasite and PdCr has improved the application temperature to at least 1000 °C [108, 109].

Sensors measuring temperature through infrared heat radiation are convenient due to a variety of applicable temperature detection methods and the ability to use any electrical temperature sensitive element as a blackbody sensor. This thermometer type can perform temperature measurements of surfaces as high as 3000 °C using a non-contact method, providing a possibility of measuring, for example, the temperature of molten metals. The evident disadvantages of such a thermometer are the inaccuracy of the measured value and the linear dependence on measured surface emissivity.

Fibre-optic based thermometers allow measuring temperatures of more than 1000 °C by applying spectrometric and interferometric techniques using standard optic fibres as well as using photonic-crystal fibres measured by interferometry. This thermometer type enables performing distributed sensing, where one fibre can act as a multiplexed sensing element at temperatures as high as 500 °C. Recent improvements in cost due to enhanced fibre fabrication processes make it a more feasible temperature sensing method and development of new fibres attracts significant research interest.

Thermocouples allow measuring temperature in excess of 1000 °C, while the temperature sensitivity of such thermometers is low and very non-linear. Another example of a non-linear thermometer is the thermistor, which can be used to register temperatures up to 300 – 450 °C. Resistance thermometers have the highest linearity in the temperature range of up to 650 °C when Pt sensitive elements are used. These three thermometer types have miniaturised implementations and have the best potential for integration, which is covered in examples from the research. Platinum RTDs are irreplaceable when maximum simplicity of measurement and highest

possible linearity is required, and thin film elements can be integrated with simple instrumentation to measure temperature reliably.

Platinum and tantalum nitride were selected as temperature transducer elements due to their promising temperature stability. Pt is selected as the temperature sensitive material while TaN can be used to give a very low temperature coefficient of resistance. Sub-micron thickness of platinum will result in less sensitivity to temperature as compared to bulk values achieved in resistance temperature thermometers used as industry standards. Necessary resistance parameter profile of TaN can be obtained through tuning of film composition as shown in the examples in the literature and temperature coefficient values of ±100 ppm $°C^{-1}$ should be achievable.

References

[1] J. Fraden, "Physical Principles of Sensing," in *Handbook of Modern Sensors*, 3rd ed., New York, USA: Springer-Verlag, 2004, pp. 37-150.
[2] J. S. Robert *et al.*, "Temperature Measurement," in *The Measurement, Instrumentation and Sensors Handbook*, J. G. Webster, Ed.: CRC Press, 1999, pp. 32.1-32.11.
[3] H. Budzier and G. Gerlach, "Thermal Infrared Sensors," in *Thermal Infrared Sensors: Theory, Optimisation and Practice*, Chichester, UK: John Wiley & Sons, 2011, pp. 103-148.
[4] E. Udd, "Overview of Fiber Optic Sensors," in *Fiber Optic Sensors*, S. Yin, P. Ruffin, and F. Yu, Eds., 2nd ed., Boca Raton, USA: CRC Press, 2008, pp. 1-34.
[5] G. Harman, "Pressure Sensors," in *Sensor Technology Handbook*, J. S. Wilson, Ed. Oxford, UK: Newnes, 2005, pp. 411-456.
[6] R. S. Dahiya and M. Valle, "Fundamentals of Piezoelectricity," in *Robotic Tactile Sensing*, Dordrecht, Netherlands: Springer, 2013, pp. 195-210.
[7] H. Fritze, S. Schmidtchen, M. Schulz, and D. Richter, "Langasite based high-temperature bulk acoustic wave sensors," *Sensors, 2011 IEEE,* pp. 600-605, 2011.
[8] S. Zhang, F. Yu, and D. J. Green, "Piezoelectric Materials for High Temperature Sensors," *Journal of the American Ceramic Society,* vol. 94, no. 10, pp. 3153-3170, 2011.
[9] J. Fraden, "Temperature Sensors," in *Handbook of Modern Sensors*, 3rd ed., New York, USA: Springer-Verlag, 2004, pp. 457-498.
[10] R. J. Brook, "Piezoelectrics Materials," in *Concise Encyclopedia of Advanced Ceramic Materials*, Cambridge, USA: MIT Press, 1991, pp. 351-354.
[11] N. Maluf and K. Williams, "Materials for MEMS," in *An Introduction to Microelectromechanical Systems Engineering*, 2nd ed., Boston, USA: Artech House, 2004, pp. 13-32.
[12] M. Zhang, J. Yang, C. Si, G. Han, Y. Zhao, and J. Ning, "Research on the Piezoelectric Properties of AlN Thin Films for MEMS Applications," *Micromachines,* vol. 6, no. 9, pp. 1236-1248, 2015.
[13] C. S. Lynch, "Strain Measurement," in *The Measurement, Instrumentation and Sensors Handbook*, J. G. Webster, Ed.: CRC Press, 1999, pp. 22.1-22.2.
[14] S. Beeby, G. Ensell, M. Kraft, and N. White, "Mechanical Transduction Techniques," in *MEMS Mechanical Sensors*, Norwood, USA: Artech House, 2004, pp. 85-112.
[15] K. H.-L. Chau, R. Goehner, E. Drubetsky, H. M. Brady, J. William H. Bayles, and P. C. Pedersen, "Pressure and Sound Measurement," in *The Measurement, Instrumentation and Sensors Handbook*, J. G. Webster, Ed.: CRC Press, 1999, pp. 26.1-26.3.
[16] C. Liu, "Piezoresistive Sensors," in *Foundations of MEMS*, Upper Saddle River, USA: Pearson Education, 2006, pp. 207-244.

[17] A. A. Ned, R. S. Okojie, and A. D. Kurtz, "6H-SiC pressure sensor operation at 600°C," *High Temperature Electronics Conference, Fourth International,* pp. 257-260, 1998.

[18] R. S. Okojie, D. Lukco, V. Nguyen, and E. Savrun, "4H-SiC Piezoresistive Pressure Sensors at 800°C With Observed Sensitivity Recovery," *IEEE Electron Device Letters,* vol. 36, no. 2, pp. 174-176, 2015.

[19] O. J. Gregory, Q. Luo, and E. E. Crisman, "High temperature stability of indium tin oxide thin films," *Thin Solid Films,* vol. 406, no. 1-2, pp. 286-293, 2002.

[20] J. Wrbanek, G. Fralick, and J. Gonzalez, "Developing Multilayer Thin Film Strain Sensors with High Thermal Stability," *42nd Joint Propulsion Conference and Exhibit,* 2006.

[21] J. Fontes, "Temperature Sensors," in *Sensor Technology Handbook*, J. S. Wilson, Ed. Oxford, UK: Newnes, 2005, pp. 531-562.

[22] T. Huynh, "Fundamentals of Thermal Sensors," in *Thermal Sensors: Principles and Applications for Semiconductor Industries*, C. M. Jha, Ed. New York, USA: Springer, 2015, pp. 5-42.

[23] L. Michalski, K. Eckersdorf, J. Kucharski, and J. McGhee, "Semiconductor Thermometers," in *Temperature Measurement*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 103-124.

[24] A. Elasser and T. P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems," *Proceedings of the IEEE,* vol. 90, no. 6, pp. 969-986, 2002.

[25] J. V. Nicholas and D. R. White, "Thermocouple Thermometry," in *Traceable Temperatures: An Introduction to Temperature Measurement and Calibration*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 295-342.

[26] L. Michalski, K. Eckersdorf, J. Kucharski, and J. McGhee, "Thermoelectric Thermometers," in *Temperature Measurement*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 37-84.

[27] Y. Heichal, S. Chandra, and E. Bordatchev, "A fast-response thin film thermocouple to measure rapid surface temperature changes," *Experimental Thermal and Fluid Science,* vol. 30, no. 2, pp. 153-159, 2005.

[28] J. Wrbanek, G. Fralick, S. Farmer, A. Sayir, C. Blaha, and J. Gonzalez, "Development of Thin Film Ceramic Thermocouples for High Temperature Environments," *40th Joint Propulsion Conference and Exhibit,* 2004.

[29] J. V. Nicholas and D. R. White, "Platinum Resistance Thermometry," in *Traceable Temperatures: An Introduction to Temperature Measurement and Calibration*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 203-253.

[30] E. A. Brandes and G. B. Brook, "Electrical Properties," in *Smithells Metals Reference Book*, 7th ed., Oxford, UK: Butterworth-Heinemann, 1992, pp. 19-1-19-10.

[31] "Specifying RTDs," ed. http://www.smartsensors.com/specrtds.pdf: Smart Sensors, 2003.

[32] M. Nau, "Resistance Thermometers," in *Electrical Temperature Measurement with Thermocouples and Resistance Thermometers*, 10th ed., Fulda, Germany, 2002, pp. 45-62.

[33] K. S. Gam, I. Yang, and Y. G. Kim, "Thermal Hysteresis in Thin-Film Platinum Resistance Thermometers," *International Journal of Thermophysics,* vol. 32, no. 11-12, pp. 2388-2396, 2011.
[34] F. Lacy, S.-I. Ao, M. A. Amouzegar, and S.-S. Chen, "Characterizing Nanometer Sized Platinum Films for Temperature Measurements," *World Congress on Engineering and Computer Science,* vol. 1007, pp. 128-139, 2008.
[35] F. Peeters, M. Peetermans, and L. Indesteege, "Temperature Sensors," in *Modern Sensors Handbook*, P. Ripka and A. Tipek, Eds., London, UK: ISTE, 2007, pp. 347-393.
[36] C. H. McMurtry, W. T. Terrell, and W. T. Benecki, "A Tin Oxide Thermistor for Temperature Sensing to 1800 °F," *IEEE Transactions on Industry and General Applications,* vol. IGA-2, no. 6, pp. 461-464, 1966.
[37] C. L. Au, W. A. Anderson, D. A. Schmitz, J. C. Flassayer, and F. M. Collins, "Stability of tantalum nitride thin film resistors," *Journal of Materials Research,* vol. 5, no. 06, pp. 1224-1232, 1990.
[38] K. Tominaga, H. Adachi, and K. Wasa, "Functional Thin Films," in *Handbook of Sputter Deposition Technology: Fundamentals and Applications for Functional Thin Films, Nanomaterials and MEMS*, K. Wasa, I. Kanno, and H. Katera, Eds., 2nd ed., Waltham, USA: Elsevier, 2012, pp. 361-520.
[39] L. Michalski, K. Eckersdorf, J. Kucharski, and J. McGhee, "Resistance Thermometers," in *Temperature Measurement*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 85-102.
[40] "Thermistors in Single Supply Temperature Sensing Circuits," ed. http://ww1.microchip.com/downloads/en/AppNotes/00685b.pdf: Microchip, 1999 [Revised 2004].
[41] J. Fraden, "Light Detectors," in *Handbook of Modern Sensors*, 3rd ed., New York, USA: Springer-Verlag, 2004, pp. 407-442.
[42] I. R. Sinclair, "Physical Principles of Sensing," in *Sensors and Transducers*, 3rd ed., Oxford, UK: Newnes, 2001, pp. 37-122.
[43] J. Fraden, in *Handbook of Modern Sensors*, 3rd ed., New York, USA: Springer-Verlag, 2004, pp. 557-577.
[44] L. Michalski, K. Eckersdorf, J. Kucharski, and J. McGhee, "Manually Operated Pyrometers," in *Temperature Measurement*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 163-176.
[45] J. V. Nicholas and D. R. White, "Radiation Thermometry," in *Traceable Temperatures: An Introduction to Temperature Measurement and Calibration*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 343-392.
[46] L. Michalski, K. Eckersdorf, J. Kucharski, and J. McGhee, "Automatic Pyrometers," in *Temperature Measurement*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 177-208.
[47] L. Michalski, K. Eckersdorf, J. Kucharski, and J. McGhee, "Fibre Optic Thermometers," in *Temperature Measurement*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 125-138.
[48] S. Tofighi, A. Bahrampour, N. Pishbin, and A. R. Bahrampour, "Interferometric Fiber-Optic Sensors," in *Optical Fiber Sensors: Advanced Techniques and Applications*, G. Rajan, Ed. Boca Raton, USA: CRC Press, 2015, pp. 37-78.

[49] S. Yin, C. Zhan, and P. B. Ruffin, "Femtosecond Laser-Inscribed Harsh Environment Fiber Bragg Grating Sensors," in *Fiber Optic Sensors*, S. Yin, P. Ruffin, and F. Yu, Eds., 2nd ed., Boca Raton, USA: CRC Press, 2008, pp. 164-200.
[50] D. Sengupta, "Fiber Bragg Grating Sensors and Interrogation Systems," in *Optical Fiber Sensors: Advanced Techniques and Applications*, G. Rajan, Ed. Boca Raton, USA: CRC Press, 2015, pp. 207-256.
[51] C. E. Lee, R. A. Atkins, and H. F. Taylor, "Performance of a fiber-optic temperature sensor from −200 to 1050°C," *Optics Letters,* vol. 13, no. 11, p. 1038, 1988.
[52] H.-S. Choi, H. F. Taylor, and C. E. Lee, "High-performance fiber-optic temperature sensor using low-coherence interferometry," *Optics Letters,* vol. 22, no. 23, p. 1814, 1997.
[53] H. F. Taylor, "Fiber Optic Sensors Based upon the Fabry–Perot Interferometer," in *Fiber Optic Sensors*, S. Yin, P. Ruffin, and F. Yu, Eds., 2nd ed., Boca Raton, USA: CRC Press, 2008, pp. 35-65.
[54] A. M. R. Pinto, "Photonic-Crystal Fibers for Sensing Applications," in *Optical Fiber Sensors: Advanced Techniques and Applications*, G. Rajan, Ed. Boca Raton, USA: CRC Press, 2015, pp. 125-150.
[55] D. Monzon-Hernandez, V. P. Minkovich, and J. Villatoro, "High-temperature sensing with tapers made of microstructured optical fiber," *IEEE Photonics Technology Letters,* vol. 18, no. 3, pp. 511-513, 2006.
[56] B. Srinivasan and D. Venkitesh, "Distributed Fiber-Optic Sensors and Their Applications," in *Optical Fiber Sensors: Advanced Techniques and Applications*, G. Rajan, Ed. Boca Raton, USA: CRC Press, 2015, pp. 309-358.
[57] Y. J. Rao and S. Huang, "Applications of Fiber Optic Sensors," in *Fiber Optic Sensors*, S. Yin, P. Ruffin, and F. Yu, Eds., 2nd ed., Boca Raton, USA: CRC Press, 2008, pp. 397-494.
[58] B. Glisic and D. Inaudi, "Distributed Fiber Optic Strain and Temperature Sensing for Structural Health Monitoring," *The Third Int'l Conference on Bridge Maintenance, Safety and Management,* 2006.
[59] A. Belani and S. Orr, "A Systematic Approach to Hostile Environments," *Journal of Petroleum Technology,* vol. 60, no. 07, pp. 34-39, 2008.
[60] C. Avant, B. K. Behera, and e. al., "Testing the limits in extreme well conditions," *Oilfield Review,* vol. 24, no. 3, pp. 4-19, 2012.
[61] "Platinum Temperature Sensors," ed. https://www.ist-usadivision.com/objects/media/brochures/temperature/platinum_temperature_sensor_catalog.pdf: Innovative Sensor Technology, 2012.
[62] K. Seshan, D. J. Schepis, and L. B. Rothman, "Organic Dielectrics in Multilevel Metallization of Integrated Circuits," in *Handbook of Thin Film Deposition*, K. Seshan, Ed. 2nd ed., Oxford, UK: William Andrew Publishing, 2002, pp. 513-594.
[63] O. Brand, "Fabrication Technology," in *CMOS - MEMS*, H. Baltes *et al.*, Eds., (Advanced Micro & Nanosystems, no. 2), Weinheim, Germany: Wiley-VCH, 2005, pp. 1-68.

[64] I. H. Kazi, P. M. Wild, T. N. Moore, and M. Sayer, "The electromechanical behavior of nichrome (80/20 wt.%) film," *Thin Solid Films,* vol. 433, no. 1-2, pp. 337-343, 2003.
[65] J. Yang *et al.*, "Low Energy Sputter Deposition and Properties of NiCr Thin Film Resistors for GaAs Integrated Circuits," in *International Conference on Compound Semiconductor Manufacturing Technology*, 2005.
[66] S. Das and J. Akhtar, "Comparative Study on Temperature Coefficient of Resistance (TCR) of the E-beam and Sputter Deposited Nichrome Thin Film for Precise Temperature Control of Microheater for MEMS Gas Sensor," in *Physics of Semiconductor Devices - 17th International Workshop on the Physics of Semiconductor Devices*: Springer, 2014, pp. 495-497.
[67] G.-S. Chung, W.-J. Lee, and J.-S. Song, "Characteristics of Chromium Nitride Thin-Film Strain Gauges," *Sensors and Materials,* vol. 13, no. 1, pp. 13-23, 2001.
[68] T. Riekkinen, J. Molarius, T. Laurila, A. Nurmela, I. Suni, and J. K. Kivilahti, "Reactive sputter deposition and properties of Ta_xN thin films," *Microelectronic Engineering,* vol. 64, no. 1-4, pp. 289-297, 2002.
[69] T. Akashi, S. Higashiyama, H. Takemori, and T. Koizmi, "A silicon optical bench incorporating a tantalum-nitride thin-film resistor," *Journal of Micromechanics and Microengineering,* vol. 14, no. 2, pp. 283-289, 2004.
[70] C. M. Wang, J. H. Hsieh, C. Li, Y. Fu, and T. P. Chen, "Effects of annealing on the microstructure and electrical properties of TaN-Cu nanocomposite thin films," *Surface and Coatings Technology,* vol. 193, no. 1-3, pp. 173-177, 2005.
[71] C. Gwiy-Sang and O. Chang-Min, "Fabrication of High Temperature Ceramic Pressure Sensor and Its Characteristics," *5th IEEE Conference on Sensors,* pp. 1111-1114, 2006.
[72] H. Jiang, C. Wang, W. Zhang, X. Si, and Y. Li, "Influences of Film Thickness on the Electrical Properties of TaN_x Thin Films Deposited by Reactive DC Magnetron Sputtering," *Journal of Materials Science & Technology,* vol. 26, no. 7, pp. 597-600, 2010.
[73] N. D. Cuong, N. M. Phuong, D.-J. Kim, B.-D. Kang, C.-S. Kim, and S.-G. Yoon, "Effect of annealing temperature on structural and electrical properties of tantalum nitride thin film resistors deposited on SiO_2/Si substrates by dc sputtering technique," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 24, no. 2, p. 682, 2006.
[74] N. D. Cuong, D.-J. Kim, B.-D. Kang, C.-S. Kim, and S.-G. Yoon, "Effect of film thickness on the electrical properties of tantalum nitride thin films deposited on SiO_2/Si substrates for Π-type attenuator applications," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 24, no. 3, p. 1398, 2006.
[75] N. D. Cuong, D.-J. Kim, B.-D. Kang, and S.-G. Yoon, "Structural and electrical characterization of tantalum nitride thin film resistors deposited on AlN substrates for π-type attenuator applications," *Materials Science and Engineering: B,* vol. 135, no. 2, pp. 162-165, 2006.
[76] N. D. Cuong, D.-J. Kim, B.-D. Kang, and S.-G. Yoon, "Effects of Nitrogen Concentration on Structural and Electrical Properties of Titanium Nitride for

Thin-Film Resistor Applications," *Electrochemical and Solid-State Letters,* vol. 9, no. 9, p. G279, 2006.
[77] N. D. Cuong, D.-J. Kim, B.-D. Kang, C. S. Kim, and S.-G. Yoon, "Characterizations of high resistivity TiN_xO_y thin films for applications in thin film resistors," *Microelectronics Reliability,* vol. 47, no. 4-5, pp. 752-754, 2007.
[78] N. D. Cuong, S.-G. Yoon, D.-J. Kim, and B.-D. Kang, "Ti(N) thin film resistors for 20dB Π-type attenuator applications," *Applied Physics Letters,* vol. 90, no. 18, p. 183506, 2007.
[79] A. Malmros, K. Andersson, and N. Rorsman, "Combined TiN- and TaN temperature compensated thin film resistors," *Thin Solid Films,* vol. 520, no. 6, pp. 2162-2165, 2012.
[80] Y. L. Cheng, B. J. Wei, F. H. Shih, and Y. L. Wang, "Stability and Reliability of Ti/TiN as a Thin Film Resistor," *ECS Journal of Solid State Science and Technology,* vol. 2, no. 1, pp. Q12-Q15, 2012.
[81] T. Nozawa and T. Suzuki, "Zirconium Nitride Thin-Film Resistors With High Thermal Durability," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology,* vol. 8, no. 4, pp. 512-516, 1985.
[82] K. Izumi, D. Masanobu, and H. Ariyoshi, "Properties of Zirconium Nitride Film Resistors Deposited by Reactive RF Sputtering," *IEEE Transactions on Parts, Hybrids, and Packaging,* vol. 11, no. 2, pp. 105-107, 1975.
[83] M. Imran and A. Bhattacharyya, "Effect of Thin Film Thicknesses and Materials on the Response of RTDs and Microthermocouples," *IEEE Sensors Journal,* vol. 6, no. 6, pp. 1459-1467, 2006.
[84] *Nickel Thin Film Temperature Sensor*, 2016.
[85] J.-S. Lee, H.-D. Park, S.-M. Shin, and J.-W. Park, "Agglomeration phenomena of high temperature coefficient of resistance platinum films deposited by electron beam evaporation," *Journal of Materials Science Letters,* vol. 16, no. 15, pp. 1257-1259, 1997.
[86] K. Tsutsumi, A. Yamashita, and H. Ohji, "The experimental study of high TCR Pt thin films for thermal sensors," vol. 2, pp. 1002-1005, 2002.
[87] R. M. Tiggelaar *et al.*, "Fabrication and characterization of high-temperature microreactors with thin film heater and sensor patterns in silicon nitride tubes," *Lab Chip,* vol. 5, no. 3, pp. 326-36, 2005.
[88] N. H. Kim, D. M. Na, P. J. Ko, J. S. Park, and W. S. Lee, "Electrical and Thermal Properties of Platinum Thin Films Prepared by DC Magnetron Sputtering for Micro-Heater of Microsensor Applications after CMP Process," *Solid State Phenomena,* vol. 124-126, pp. 267-270, 2007.
[89] G.-S. Chung and C.-H. Kim, "RTD characteristics for micro-thermal sensors," *Microelectronics Journal,* vol. 39, no. 12, pp. 1560-1563, 2008.
[90] J. Zhang, Y. Nagao, S. Kuwano, and Y. Ito, "Microstructure and Temperature Coefficient of Resistance of Platinum Films," *Japanese Journal of Applied Physics,* vol. 36, no. Part 1, No. 2, pp. 834-839, 1997.
[91] F. Zandman, P. R. Simon, and J. Szwarc, "Precision Resistors and Resistor Networks," in *Resistor Theory and Technology*, Malvern, USA: Vishay Intertechnology, 2002, pp. 153-180.

[92] F. Zandman, P. R. Simon, and J. Szwarc, "Resistive Materials," in *Resistor Theory and Technology*, Malvern, USA: Vishay Intertechnology, 2002, pp. 51-74.
[93] T. Lee *et al.*, "Characterization and reliability of TaN thin film resistors," in *Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International*, 2004, pp. 502-508: IEEE.
[94] G. I. Drandova and K. D. Decker, "TaN Resistor Reliability Studies," *International Conference on Compound Semiconductor Manufacturing Technology,* pp. 69-72, 2010.
[95] J. J. Licari and L. R. Enlow, "Thin Film Processes," in *Hybrid Microcircuit Technology Handbook: Materials, Processes, Design, Testing and Production*, 2nd ed., Westwood, USA: Noyes Publications, 1998, pp. 63-103.
[96] N. D. Cuong, D.-J. Kim, B.-D. Kang, C. S. Kim, K.-M. Yu, and S.-G. Yoon, "Characterization of Tantalum Nitride Thin Films Deposited on SiO_2/Si Substrates Using dc Magnetron Sputtering for Thin Film Resistors," *Journal of The Electrochemical Society,* vol. 153, no. 2, pp. G164-G167, 2006.
[97] T. Elangovan *et al.*, "Synthesis and high temperature XRD studies of tantalum nitride thin films prepared by reactive pulsed dc magnetron sputtering," *Journal of Alloys and Compounds,* vol. 509, no. 22, pp. 6400-6407, 2011.
[98] S. Noda, K. Tepsanongsuk, Y. Tsuji, Y. Kajikawa, Y. Ogawa, and H. Komiyama, "Preferred orientation and film structure of TaN films deposited by reactive magnetron sputtering," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 22, no. 2, p. 332, 2004.
[99] W. J. Ostrander, J. Verhoef, and L. W. Bos, "Processing and Performance of Tantalum Nitride Thin Film Resistor Networks with +-50 ppm/°C TCR," *IEEE Transactions on Parts, Hybrids, and Packaging,* vol. PHP-9, no. 3, pp. 155-160, 1973.
[100] C. Stampfl and A. J. Freeman, "Stable and metastable structures of the multiphase tantalum nitride system," *Physical Review B,* vol. 71, no. 2, 2005.
[101] W. Cuviello and D. Coulton, "Thin Film High-Density Interconnect (HDI) Design Guidelines," ed. http://www.vishay.com/docs/49271/hdi.pdf: Vishay Intertechnology, 2003.
[102] S.-M. Na, I.-S. Park, S.-Y. Park, G.-H. Jeong, and S.-J. Suh, "Electrical and structural properties of Ta–N thin film and Ta/Ta–N multilayer for embedded resistor," *Thin Solid Films,* vol. 516, no. 16, pp. 5465-5469, 2008.
[103] R. Henderson *et al.*, "Tantalum nitride thin film resistors for integration into copper metallization based RF-CMOS and BiCMOS technology platforms," *Silicon Monolithic Integrated Circuits in RF Systems,* pp. 71-74, 2001.
[104] T. Remmel *et al.*, "Integration of Thin-Film Capacitors and Resistors into ULSI Technology for Wireless Applications," *Passive Component Industry,* no. January/February 2001, pp. 24-32 2001.
[105] T. Akashi, "Fabrication of a Tantalum-Nitride Thin-Film Resistor with a Low-Variability Resistance," *IEEJ Transactions on Sensors and Micromachines,* vol. 125, no. 4, pp. 182-187, 2005.
[106] M. Grosser *et al.*, "Study on microstructural, chemical and electrical properties of tantalum nitride thin films deposited by reactive direct current magnetron sputtering," *Microsystem Technologies,* vol. 16, no. 5, pp. 825-836, 2010.

[107] G.-S. Chung, "Characteristics of tantalum nitride thin film strain gauges for harsh environments," *Sensors and Actuators A: Physical,* vol. 135, no. 2, pp. 355-359, 2006.

[108] R. Behanan *et al.*, "Thin films and techniques for SAW sensor operation above 1000°C," *2013 IEEE International Ultrasonics Symposium,* pp. 1013-1016, 2013.

[109] J. D. Wrbanek, G. C. Fralick, J. M. Gonzalez, and K. L. H. Laster, "Thin Film Ceramic Strain Sensor Development for High Temperature Environments," *NASA: Aging Aircraft 2008,* 2008.

Chapter 3 Design of temperature transducer bridge

3.1 Introduction

This chapter will briefly outline the approach used to produce a temperature sensor which can be integrated onto a silicon carbide-based integrated circuit. The answer to whether this approach will be effective and whether it will provide a reasonable application for the high temperature ICs lies in the temperature sensor performance characteristics. This chapter will describe the selection of thin film materials for sensors expected to perform sustained operations in high temperature environments and will also provide results of numerical analysis that show what effect the designed electrical parameters, element mismatch and deviation from rated parameters have on key characteristics of sensor temperature response.

3.2 Integrated temperature sensing system produced by post-processing

The aim of this project is to produce a temperature sensing system that can be co-fabricated with silicon carbide-based integrated circuits and eventually to enable monolithic integration of sensors with integrated circuits at the wafer level. Temperature sensors will provide an application for SiC-based instrumentation amplifiers which can operate at temperatures as high as 350 °C. A key advantage of this approach for SiC-based systems is reduced cost when compared to other

processing methods [1]. Another benefit of this solution is that no redesign of the SiC IC or additional packaging is required at this stage because the sensor is designed to be fabricated directly on top of the circuit, connecting to the existing power and input/output contacts.

The closest example of this approach can be seen in work by Wijngaards et al., where a low temperature coefficient of resistance (TCR) NiCr on-chip resistor and an on-chip temperature sensor based on high TCR Pt resistor were fabricated as separate elements using a post-processing strategy [2, 3]. Issues such as process compatibility and manufacturability were examined in that work stressing that the temperature budget of sensor microfabrication should not damage or affect the characteristics of underlying devices. From the perspective of a temperature sensor, the key requirement is that the performance of sensor remains stable for the specified amount of time in a given environment [4]. Alternative temperature sensing elements such as diode temperature sensors and thermistors that were produced by an integrated SiC process have been demonstrated in the literature [5-7]. In given examples temperature sensitivities reported were 3.5 $mV\cdot°C^{-1}$ for a 4H-SiC forward-biased p-n diode, 0.27 $\mu A\cdot°C^{-1}$ (biased at 1 V) for 4H-SiC p-type implanted NTC thermistor and $-0.17\%\cdot°C^{-1}$ for polycrystalline NTC thermistor post-processed on pressure sensor chip produced by cubic SiC on insulator process.

A popular and extremely effective temperature measurement approach utilizes resistance temperature detector (RTD) devices, and requires a current source to produce a measurement current and a differential amplifier to remove the common mode from the measured voltage [8]. At high temperatures these requirements become a problem because stable high temperature implementations of these circuits are required [9]. Using an RTD element in one arm of a Wheatstone bridge (as in Fig. 2.3.6(a)) gives no benefit in respect to the linearity of the resulting response to temperature (Fig. 3.2.2 against Fig. 3.3.4), and also requires balancing of the bridge so that $R_{TaN} = R_{Pt}$ at 0 °C and referencing the differential amplifier correctly [10].

Equation 3.1 describes the output of the described arrangement of Wheatstone bridge while Figure 3.2.1 demonstrates the linearity of temperature response from a circuit containing a single Pt element with TCR of α_{Pt} = 3850 ppm $°C^{-1}$:

$$V_{OUT} = V_{IN}\left(\frac{R_{Pt}}{R_{TaN} + R_{Pt}} - \frac{R_{TaN}}{2R_{TaN}}\right) = V_{IN}\left(\frac{R_{Pt}}{R_{TaN} + R_{Pt}} - \frac{1}{2}\right) \tag{3.1}$$

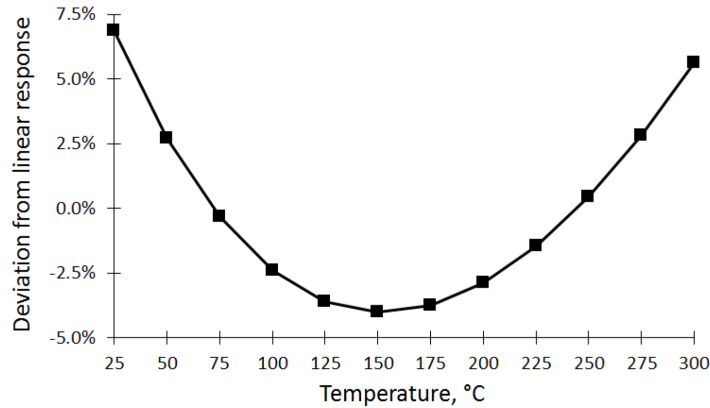

Figure 3.2.1: *Full-scale deviation from linear response produced by a Wheatstone bridge circuit measuring a single RTD element.*

A half-bridge that measures two RTD devices is a more linear temperature sensing system as shown in Figures 3.3.4 and 3.3.6, where well-matched balancing circuit elements comprised of TaN resistors that are insensitive to temperature, would result in the best possible performance (this is analysed in detail in section 3.4). Equation (3.2) describes the behaviour of the bridge circuit shown in Figure 3.2.2, with the assumptions of perfectly matched elements using TaN as a material with very low TCR and Pt as the temperature sensitive material.

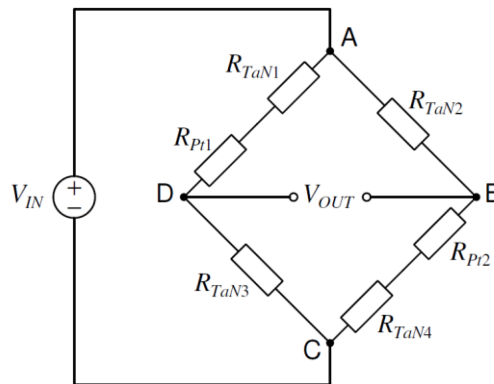

Figure 3.2.2: *Bridge with two RTD elements used as a temperature transducing circuit.*

$$V_{OUT} = V_{IN}\left(\frac{R_{TaN} + R_{Pt}}{2R_{TaN} + R_{Pt}} - \frac{R_{TaN}}{2R_{TaN} + R_{Pt}}\right) = V_{IN}\frac{R_{Pt}}{2R_{TaN} + R_{Pt}} \tag{3.2}$$

The sensor will be post-processed on top of a silicon carbide integrated circuit chip that contains two operational amplifiers and a single-ended (+15 V) rail-to-rail instrumentation amplifier with voltage-controlled gain (options of 1 and 10). The temperature specification and robustness of the SiC-based amplifier should allow measurement of temperatures of at least 300 °C using the half-bridge circuit. The instrumentation amplifier will be used to amplify the differential output V_{OUT} as described by (3.2) from the temperature sensor bridge, providing a gain G (where G = 1 or 10) to improve the temperature sensitivity of the bridge output:

$$V_{OUTina} = G \times V_{IN} \frac{R_{Pt}}{2R_{TaN} + R_{Pt}} \tag{3.3}$$

The voltage supplied to the IC power terminals (+15 V and 0 V in the current implementation) can be used for a bridge with a resistance of 15 kΩ to produce a current of the order of 0.5 mA flowing through each RTD device (7.5 mW dissipated power in each transducer arm, less than 1 mW dissipated on the sensitive element). The bridge circuit is practically insensitive to any additional resistance in the current path that remains a part of the balancing circuit as long as the effect is equal on all TaN resistors, and the instrumentation amplifier suppresses any common mode signal. Therefore, the bridge becomes essentially a ratiometric circuit that allows measurement of the temperature through the change of resistance ratio difference and the resulting change in the measured differential voltage [8].

3.3 Resistance bridge circuit numerical analysis

When a high-temperature amplifier is used at temperatures of the measured object, temperature-related parametric drift of input offset voltage, bias currents and gain figures can be expected. The response of the bridge sensor circuit in the temperature range up to 300 °C is expected to have a nearly linear dependence on designed nominal resistor values and temperature coefficients of resistance whereas non-idealities such as mismatch among temperature sensitive or balancing resistors will affect the sensitivity and linearity of the bridge response. In this section, three cases of symmetrical mismatch in bridge circuit are analysed, and the cumulative expected effects of worst case mismatch and deviation from specified resistance

parameters on key characteristics of the temperature response are demonstrated. An approximate model that describes the bridge response to temperature, ignores possible parasitic elements fabricated asymmetrically in the bridge arms and considers only α coefficients of materials is used to produce examples of circuit characteristics when it is affected by mismatch or different temperature coefficients of resistance than designed.

3.3.1 Effect of specified electrical parameters

Expected resistance and TCR values for each circuit element can be used to estimate the sensor response to temperature using Eq. (3.2). This estimate, however, does not cover variation of sheet resistance and TCR, which can change across the wafer and with each set of deposition and processing conditions that wafers are exposed to. To demonstrate the common principles of a bridge-based temperature transducer, equation 3.2 is modified to include the linear temperature dependence of both thin film materials α_{Pt} and α_{TaN}:

$$V_{OUT}(\Delta T) = V_{IN} \frac{R_{Pt}(1+\alpha_{Pt}\Delta T)}{2R_{TaN}(1+\alpha_{TaN}\Delta T)+R_{Pt}(1+\alpha_{Pt}\Delta T)}, \tag{3.4}$$

and further simplified into expression (3.5):

$$V_{OUT}(\Delta T) = V_{IN} \frac{A(1+\alpha_{Pt}\Delta T)}{2(1+\alpha_{TaN}\Delta T)+A(1+\alpha_{Pt}\Delta T)}, \tag{3.5}$$

where coefficient A denotes the ratio R_{Pt}/R_{TaN}.

The following trends are evident from Eq. (3.5):

- The TCR of Pt elements, α_{Pt}, defines the temperature sensitivity of the bridge when TCR of TaN elements is low;
- The TCR of TaN elements, α_{TaN}, affects both the sensitivity and the linearity of response to temperature;
- The ratio A and the bridge excitation voltage V_{IN} define the full-scale output range and linearity.

According to (3.5), significantly different output characteristics can be created by circuits with different resistor ratios. Figure 3.3.1 shows examples of simulated temperature response expected to be produced by 2% and 10% resistor ratio values.

The platinum TCR in this case is equal to 3850 ppm °C^{-1} and tantalum nitride TCR was varied from –250 to 250 ppm °C^{-1}. The negative TCR of tantalum nitride resistors results in improved sensitivity for any given resistance ratio, but on the other hand makes the full-scale output value larger. This becomes problematic for circuits with high resistor ratio and V_{OUT} values approaching 1.5 V, due to insuffiecient headroom for the instrumentation amplifier with a gain of 10× and a 15 V power supply.

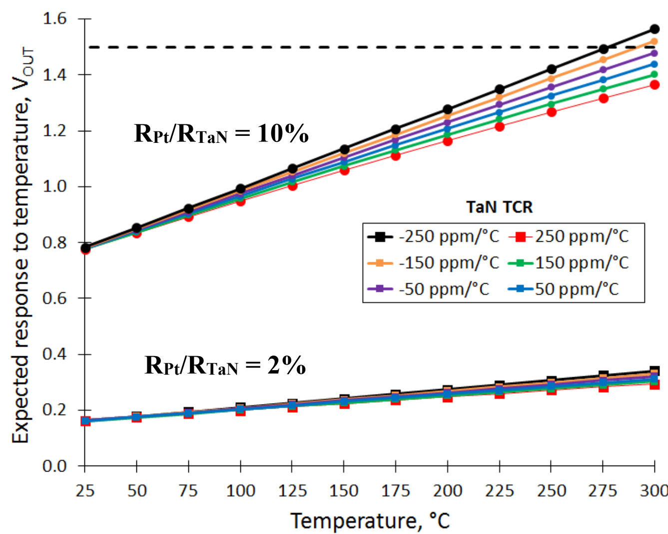

Figure 3.3.1: *Expected full-scale temperature response for different resistor ratios.*

The output of a particular temperature sensor circuit can be expressed in terms of two key response parameters:

- The reference output V_{REF}, i.e. the output voltage at the reference temperature of 25 °C;
- The sensitivity of temperature response $\Delta V_{OUT}/\Delta T$, expressed in mV·°C^{-1}.

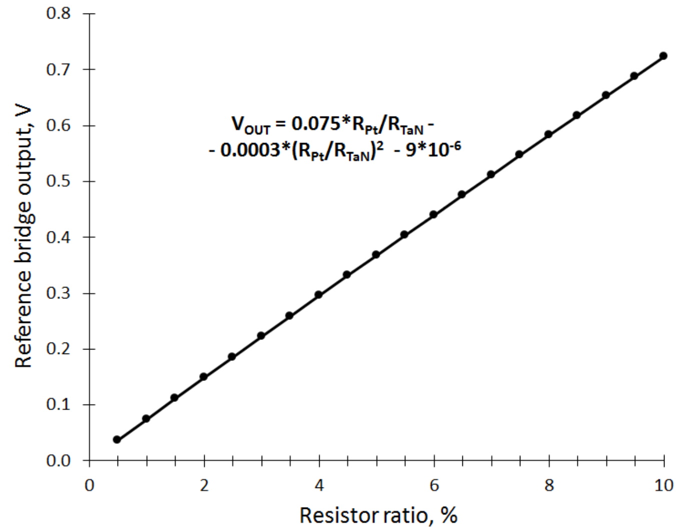

Figure 3.3.2: *Reference sensor output against designed resistor ratio.*

These can be used together to generate a calibration curve similar to those shown in Fig. 3.3.1. Figures 3.3.2 and 3.3.3 show respectively the calculated reference output and sensitivity plotted against resistor ratio, using Pt and TaN elements with ideal TCRs of 3850 and 0 ppm $°C^{-1}$ respectively. These plots are based on least squares fit values to the response characteristics for the temperature range of 25 to 300 °C similar to those shown in Fig. 3.3.1. It can be seen from the fitting functions that these characteristics have a second order dependence on the set resistor ratio.

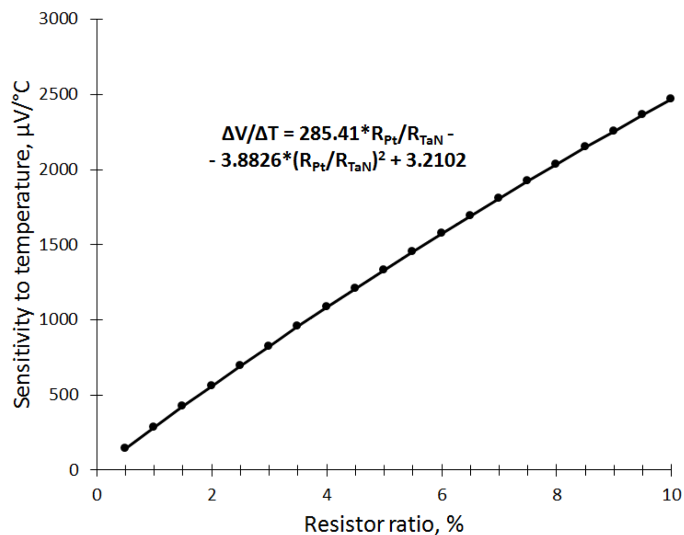

Figure 3.3.3: *Temperature sensitivity against designed resistor ratio.*

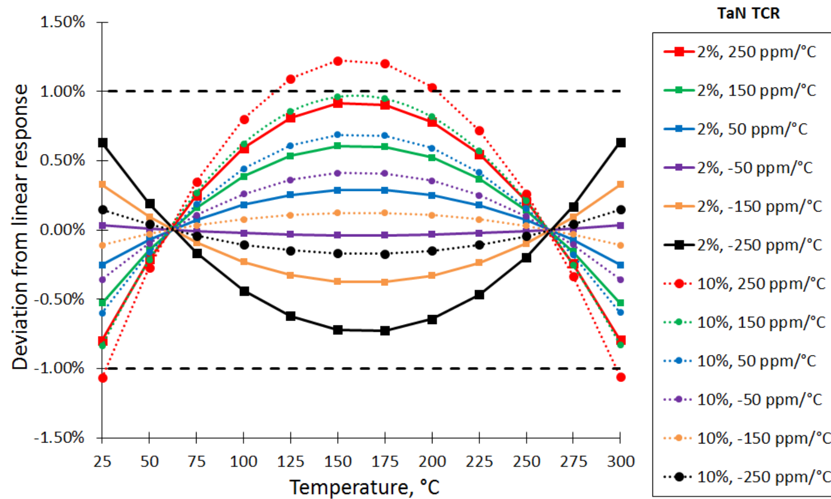

Figure 3.3.4: *Full-scale deviation from linear response at different temperatures: examples produced by 2% ratio (squares) and 10% ratio (circles)*

Figure 3.3.4 complements the previous set of graphs in Fig. 3.3.2 and 3.3.3 by showing the difference between the calculated least squares fit plots and the theoretical response to the temperature. As in Fig. 3.3.1, two families are produced that describe the expected temperature response from devices with 2% and 10% resistor ratios and different TaN TCR values. Fig. 3.3.4 depicts the full-scale non-linearity of response to temperature produced from each set of data shown in Fig. 3.3.1. It can be observed from Fig. 3.3.4 that for the given resistor ratio range the linearity and maximum deviation from linear response obtained by least squares fit is controlled by TaN TCR, where non-linearity is higher for positive TCR values.

When the TCR of the Pt resistors is significantly lower than the ideal value, the sensitivity of temperature response decreases proportionately and the only effective way to compensate for this is to increase the resistor ratio. Figure 3.3.5 shows sensitivity plots that could be expected from circuits built using Pt resistors with TCR values of 2500 and 1500 ppm °C^{-1} and TaN resistors with TCR equal to zero. Linearity plots shown in Fig. 3.3.6 (α_{Pt} = 1500 and 2500 ppm °C^{-1}), along with Fig. 3.3.4 (α_{Pt} = 3850 ppm °C^{-1}), demonstrate that more positive TaN TCR values and higher resistor ratios move the deviation to more positive values. Because these plots are describing least squares fit cases, the linearity of the response to temperature is similar regardless of the value of Pt TCR, and is generally within 1% in these examples.

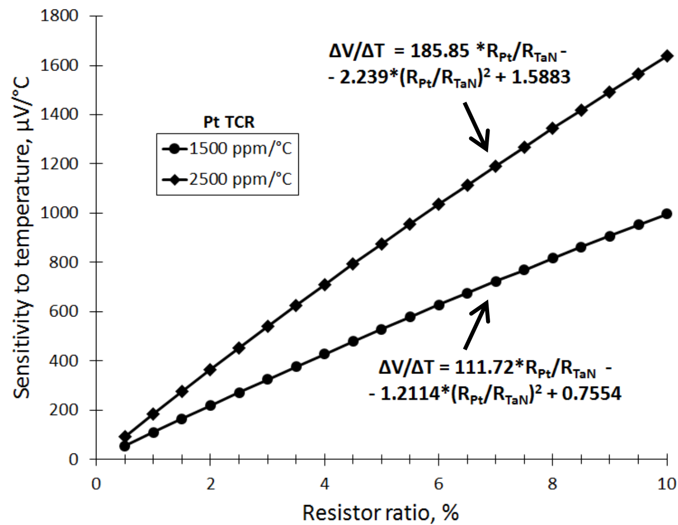

Figure 3.3.5: *Expected temperature sensitivity against designed resistor ratio.*

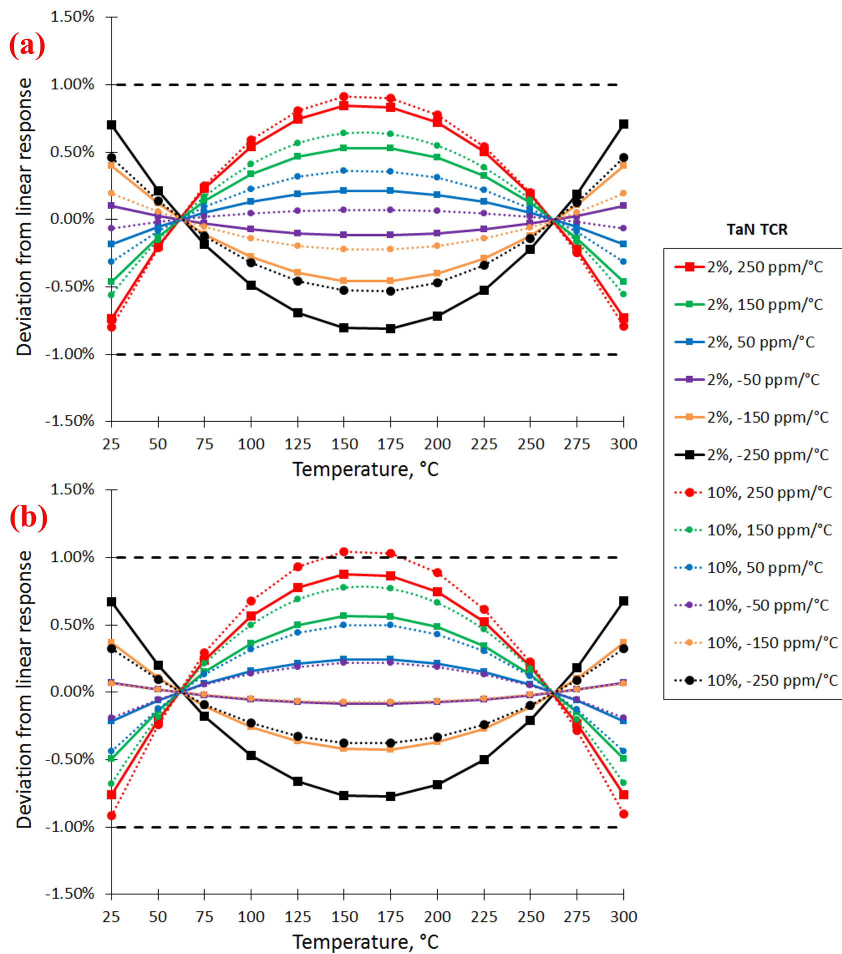

Figure 3.3.6: *Full-scale deviation from linear response at different temperatures, examples produced by 2% ratio (squares) and 10% ratio (circles): (a) α_{Pt} = 2500 ppm °C^{-1}; (b) α_{Pt} = 1500 ppm °C^{-1}.*

As shown in Fig. 3.3.1 – 3.3.6, in addition to an effect on the linearity of the sensor output, the TCR of TaN has an enormous effect on temperature sensitivity. As depicted in Fig. 3.3.7, for every 1 ppm °C^{-1} increase in the TaN TCR value, the temperature sensitivity of the sensor module is expected to decrease by at least 0.5 μV·°C^{-1} in circuits with a resistance ratio of 5% where α_{Pt} = 1500 ppm °C^{-1}. This should produce a sensitivity of 529 μV·°C^{-1} when α_{TaN} is zero so the change is ~0.1% for every 1 ppm °C^{-1} increase in TaN TCR. The effect of TaN TCR on sensitivity decreases with higher Pt TCR and this may be further used to increase the sensitivity by using more negative TCR of tantalum nitride elements. This might be required if the resistor ratio has to stay constant due to physical design constraints.

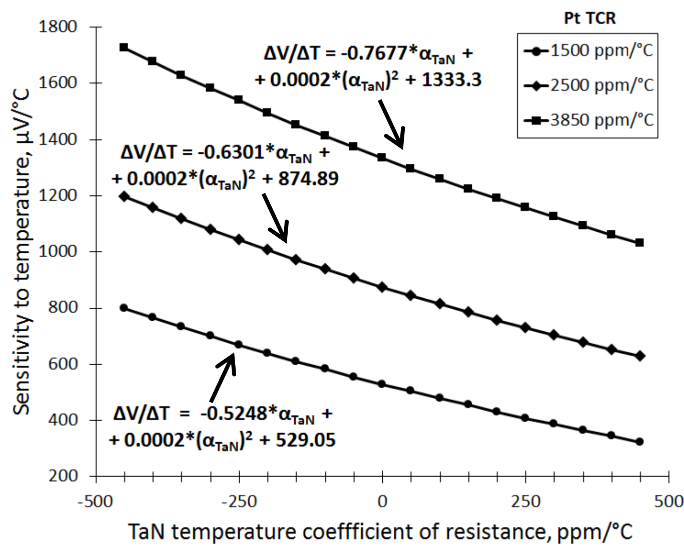

Figure 3.3.7: *Expected temperature sensitivity with changing TaN TCR.*

3.3.2 Element mismatch

The operation of a bridge sensor circuit is mostly affected by any mismatch between the balancing resistor elements. The probability of such mismatch increases with larger resistor footprint area due to effect of non-uniformities in the microfabrication processes. Other parasitic elements, such as contact resistances between different materials can also be present in the integrated sensor circuit [11].

The bridge sensor circuit output can be described using expressions such as Eq. (3.2) when all four TaN resistors are equal and both Pt resistors are equal. If simple mismatch-related effects dR that affect each of resistors are added, Eq. (3.2) changes to Eq. (3.7) to reflect all possible types of simplified mismatch:

$$V_{OUT} = V_{IN}\left(\frac{R_{TaN4} + dR_{TaN4} + R_{Pt2} + dR_{Pt2}}{R_{TaN2} + dR_{TaN2} + R_{TaN4} + dR_{TaN4} + R_{Pt2} + dR_{Pt2}}\right) - V_{IN}\left(\frac{R_{TaN3} + dR_{TaN3}}{R_{TaN1} + dR_{TaN1} + R_{TaN3} + dR_{TaN3} + R_{Pt1} + dR_{Pt1}}\right) \quad (3.7)$$

There are three major types of mismatch, each producing at least six cases in a combination of mismatch between four TaN (R_{TaN1}, R_{TaN2}, R_{TaN3} and R_{TaN4} in Fig. 3.2.3) and two Pt (R_{Pt1} and R_{Pt2}) resistors. The considered cases always include a mismatch between balancing TaN resistors and sometimes include equal degree of mismatch in temperature sensitive Pt resistors as shown in Table 3.3.1. General types that are considered for a circuit shown in Fig. 3.2.3 include mismatch of:

- Diagonally opposite balancing resistors (*'D'* cases such as in Fig. 3.3.8(a), when R_{TaN1} and R_{TaN4} are mismatched against R_{TaN2} and R_{TaN3});
- Horizontally opposite balancing resistors (*'H'* cases such as in Fig. 3.3.8(b), when R_{TaN1} and R_{TaN3} are mismatched against R_{TaN2} and R_{TaN4});
- Vertically opposite balancing resistors (*'V'* cases such as in Fig. 3.3.8(c), when R_{TaN1} and R_{TaN2} are mismatched against R_{TaN3} and R_{TaN4}).

For simplicity of explanation the value of mismatch effect is controlled by a single coefficient d and therefore mismatch cases have a symmetrical effect on balancing resistor values in the circuit.

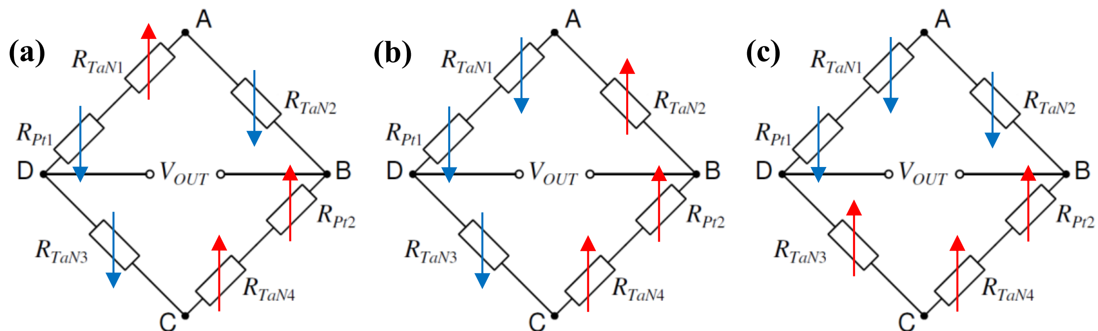

Figure 3.3.8: *Illustration of mismatch cases affecting the half-bridge circuit: (a) diagonal D1:1, (b) horizontal H1:1, (c) vertical V1:1.*

Table 3.3.1 *Considered mismatch cases and mismatch effect on each element.*

Mismatch		***Balancing circuit resistors***				***Temperature sensors***	
Direction	*Type: Case*	R_{TaN1}	R_{TaN2}	R_{TaN3}	R_{TaN4}	R_{Pt1}	R_{Pt2}
***D**iagonal*	***D**1:1*	+d	-d	-d	+d	-d	+d
	***D**1:2*	+d	-d	-d	+d	+d	-d
	***D**1:3*	+d	-d	-d	+d	0	0
	***D**2:1*	-d	+d	+d	-d	-d	+d
	***D**2:2*	-d	+d	+d	-d	+d	-d
	***D**2:3*	-d	+d	+d	-d	0	0
***H**orizontal*	***H**1:1*	-d	+d	-d	+d	-d	+d
	***H**1:2*	-d	+d	-d	+d	+d	-d
	***H**1:3*	-d	+d	-d	+d	0	0
	***H**2:1*	+d	-d	+d	-d	-d	+d
	***H**2:2*	+d	-d	+d	-d	+d	-d
	***H**2:3*	+d	-d	+d	-d	0	0
***V**ertical*	***V**1:1*	-d	-d	+d	+d	-d	+d
	***V**1:2*	-d	-d	+d	+d	+d	-d
	***V**1:3*	-d	-d	+d	+d	0	0
	***V**2:1*	+d	+d	-d	-d	-d	+d
	***V**2:2*	+d	+d	-d	-d	+d	-d
	***V**2:3*	+d	+d	-d	-d	0	0

If there is a symmetrical diagonal mismatch in a bridge circuit, the common-mode voltage at the output stays constant, but the differential voltage changes significantly. Fig. 3.3.9 and 3.3.10 show how diagonal mismatch from 0 to 20% is expected to affect devices built using 3850 and 0 ppm $°C^{-1}$ elements set at a ratio of 6%. As mismatch of resistors for a single device covering a footprint of 2.5×2.5 mm^2 should not be high, mismatch values of up to 20% are considered to include all non-idealities of the integrated bridge circuit, such as for example, contact resistance between the TaN and Pt films. Because the mismatch between Pt resistors does not have as strong influence on the output as compared to existing TaN resistor mismatch, all cases for different type of mismatch have been grouped to produce a single graph. Trends of reference output and sensitivity values are linear and opposite to one another for the diagonal mismatch cases considered here, and there is a considerable change of sensitivity and shift of full-scale output resulting from diagonal mismatch in the TaN balancing resistors.

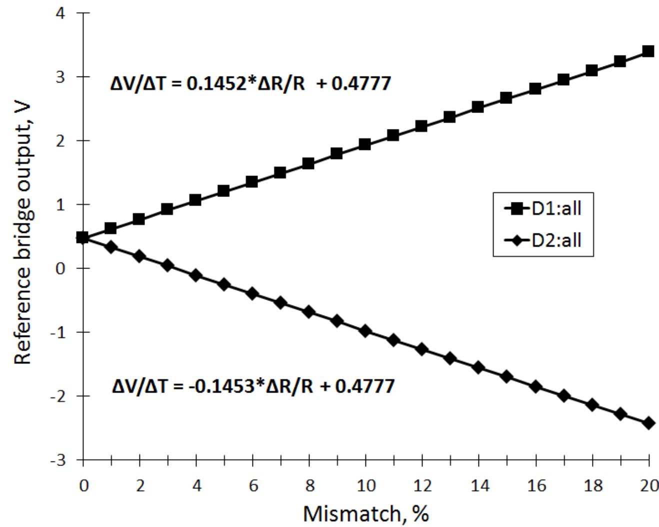

Figure 3.3.9: *Expected reference sensor output with different degree of diagonal mismatch.*

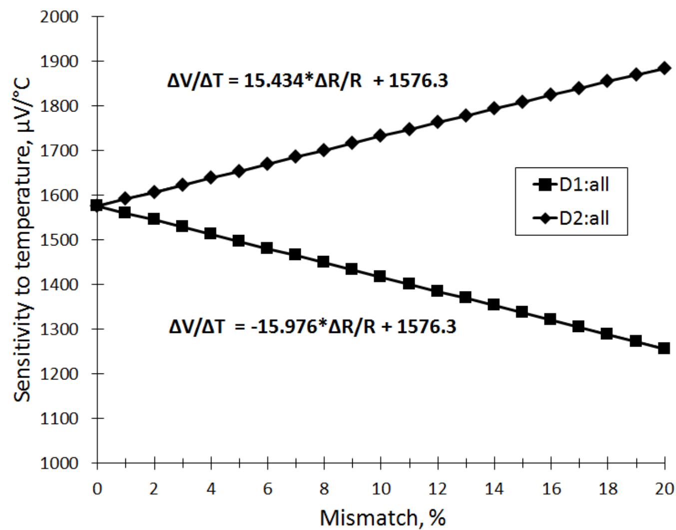

Figure 3.3.10: *Expected sensitivity to temperature with different degree of diagonal mismatch.*

In case of horizontal mismatch, the key characteristics of response to temperature are expected to change slightly as demonstrated in Fig. 3.4.11. Trends are similar for both reference output and sensitivity, and cases 'H1:1' and 'H2:2' (refer to Table 3.3.1) do not affect the characteristics because symmetrical change of resistance in each bridge arm does not affect values of common mode and differential voltages.

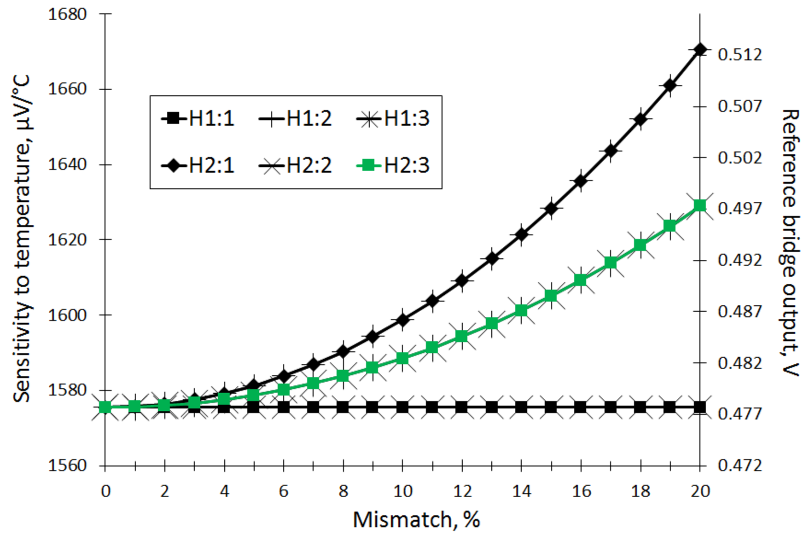

Figure 3.3.11: *Expected reference sensor output and temperature sensitivity against degree of horizontal mismatch.*

Vertical mismatch has a similar effect on key characteristics as compared to horizontal. As shown in Fig. 3.3.12, devices with 3850 and 0 ppm °C^{-1} elements with a ratio of 6% can lose or gain 3.8% in sensitivity due to a mismatch of 20%, where the rated sensitivity is 1575 µV·°C^{-1} with no mismatch. Cases such as 'V1:3' and 'V2:3' (refer to Table 3.3.1) do not affect the temperature sensing characteristics because the resistance of the Pt element is not changing.

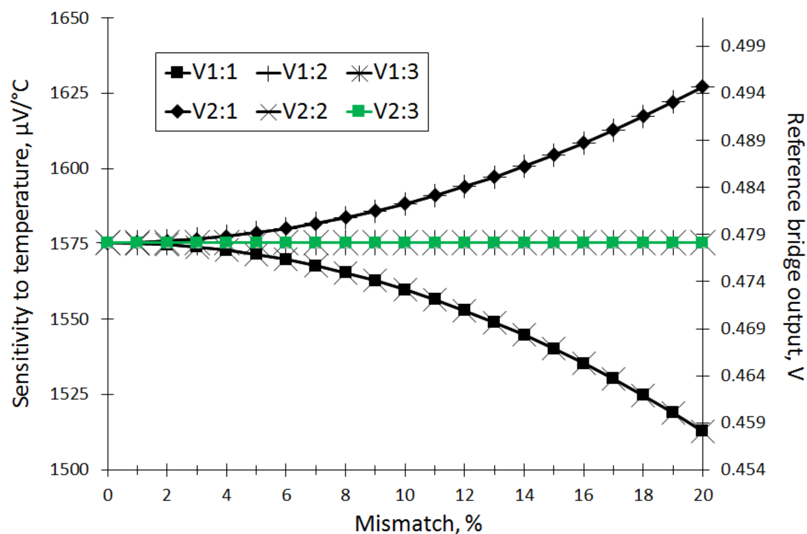

Figure 3.3.12: *Expected reference sensor output and temperature sensitivity against degree of vertical mismatch.*

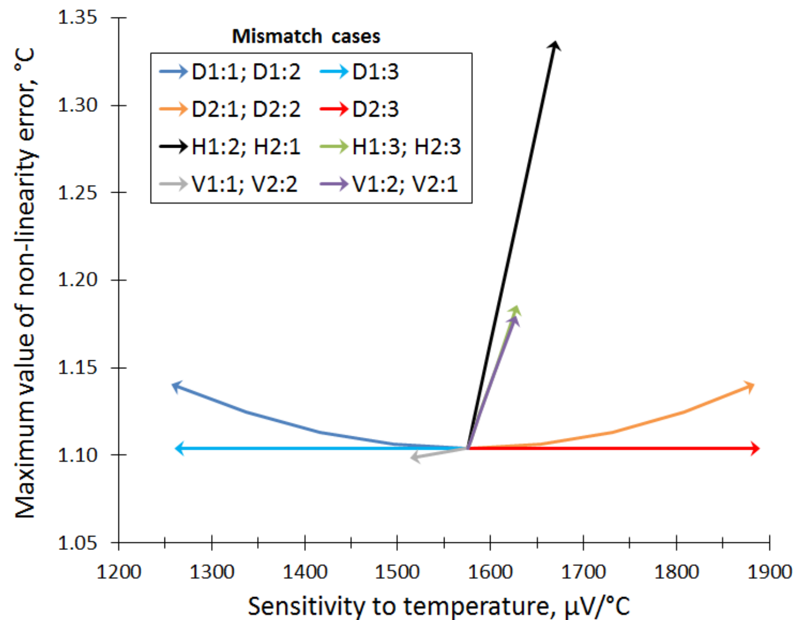

Figure 3.3.13: *Expected change of temperature response sensitivity and maximum non-linearity error when mismatch values d increase to 20%.*

Fig. 3.3.13 summarizes the sensitivity and linearity resulting from different mismatch cases, where examples expected to be produced by devices with 6% resistor ratio and α_{Pt} = 3850 and α_{TaN} = 0 ppm °C^{-1} are shown. On the graph each arrowhead represents a 20% mismatch of the particular type added to the circuit. It can be seen from horizontal mismatch plots (H1:2, H1:3, H2:1 and H2:3) that a significant non-linearity is added when both balancing and temperature sensitive resistor values are changing and misbalancing the circuit. Diagonal mismatch cases (D1:1, D1:2; D2:1, D2:2; D1:3 and D2:3) demonstrate that if platinum resistors are matched, the mismatch in the balancing circuit does not affect the linearity of the response to temperature. Although a 20% increase or decrease in the sensitivity due to diagonal mismatch in the balancing circuit does not require a significant trade-off with linearity, the reference output value is moved closer to zero (as shown in Fig. 3.3.9) and may become negative, which is unacceptable for the current application.

The modelled cases detailed in Table 3.3.1 all have mismatch that works symmetrically and changes linearly, and it should be expected that more complex

cases will result in inferior linearity of the sensor response. These examples, however, are comprehensive enough to give an idea of how mismatch between resistive elements affects the sensing performance of the circuit.

3.3.3 Deviation from designed sensor circuit component values

It has been demonstrated in section 3.3.1 that changing the R_{Pt}:R_{TaN} ratio leads to significant changes in the response to temperature and is an effective method of controlling the sensitivity of the bridge circuit. It has also been shown that deviation of TaN TCR from the ideal α_{TaN} = 0 ppm °C^{-1}, and certain cases of diagonal mismatch in the bridge also affect the sensitivity. This section will look at the cumulative effects of different types of variation of the component values, which can have a substantial impact on the temperature sensor performance.

The effect of variation of the expected material resistivities is straightforward and results in changes in the resistance ratio and bridge current. As shown in Fig. 3.3.7, the temperature sensitivity increases with a more negative value of TaN TCR and decreases with a more positive value. The combined effect of diagonal mismatch of up to 20% and TaN TCR in a range of –300 to 300 ppm °C^{-1} is demonstrated in Fig. 3.3.14, where the calculated sensitivity of a device using α_{Pt} = 3850 ppm °C^{-1} and a 6% resistor ratio is shown. Cases 'D1' and 'D2' cover examples when R_1 and R_4 resistor pairs increase and decrease in value, merging the cases for every diagonal mismatch type summarized in Table 3.3.1. Symmetrical platinum resistor mismatch for these cases has a negligible effect on characteristics of temperature response. Comparing the results in Fig. 3.3.14 with those in Fig. 3.3.3 and 3.3.5 it can be concluded that the cumulative effect of TaN TCR variation and mismatch in TaN balancing resistors may have as much effect as changing the resistor ratio by 3%. While mismatch in the TaN resistors can have a positive effect on sensitivity it should also be remembered that this will also have a significant effect on the full-scale differential output as shown in Fig. 3.3.9.

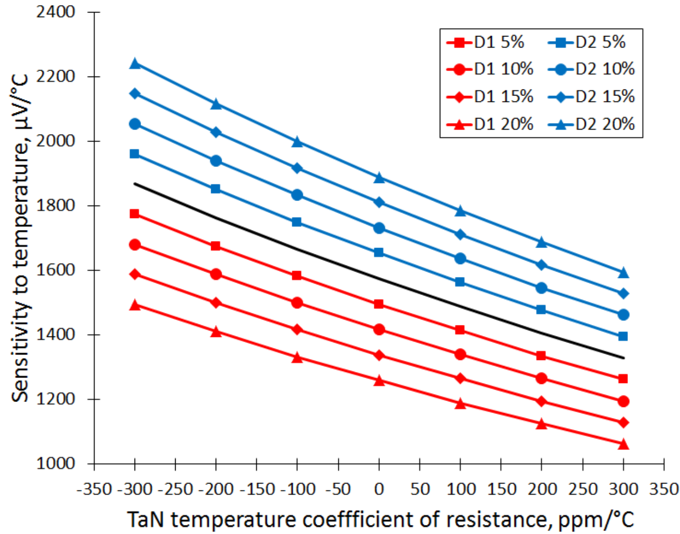

Figure 3.3.14: *Expected temperature sensitivity against TCR of TaN elements with different diagonal mismatch (α_{Pt} = 3850 ppm °C^{-1}, R_{Pt}:R_{TaN} = 0.06).*

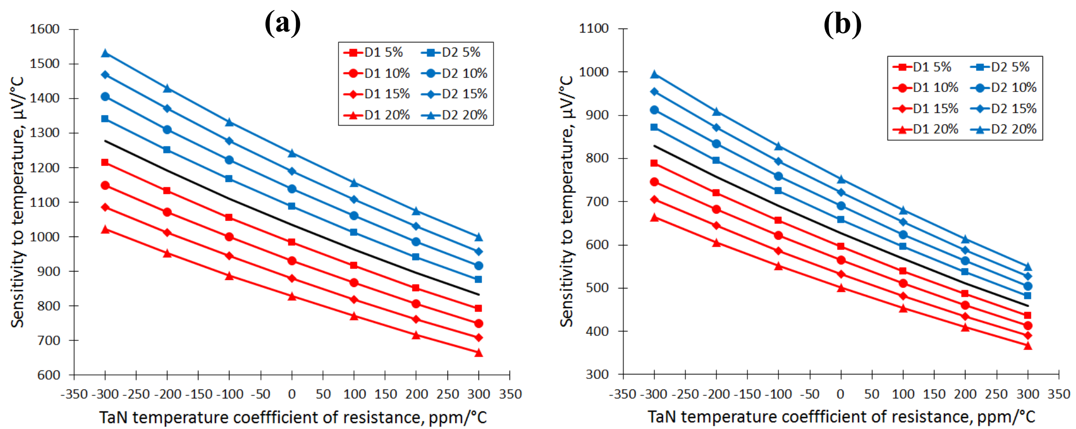

Figure 3.3.15: *Expected temperature sensitivity against TCR of TaN elements with different diagonal mismatch (R_{Pt}:R_{TaN} = 0.06):*
(a) α_{Pt} = 2500 ppm °C^{-1}; (b) α_{Pt} = 1500 ppm °C^{-1}.

Fig. 3.3.15 shows sensitivity plots expected to be produced when α_{Pt} is significantly lower than the ideal value. In can be seen from plots in Fig. 3.3.14 – 3.3.15 that expected values of sensitivity overlap between different combinations of mismatch and TaN TCR. Therefore, diagonal mismatch can be considered to produce the worst-case effects on temperature response characteristics while horizontal and vertical symmetric mismatch do not have such a pronounced effect on sensitivity. In

particular, certain types of horizontal mismatch have more effect on linearity than sensitivity as demonstrated in Fig. 3.3.13.

Figure 3.3.16 shows linearity-related characteristics of temperature response in cases summarized in Fig. 3.3.14 and Fig. 3.3.15, which describe maximum non-linearity error for an least squares fit plot. It can be seen from Fig. 3.3.16 that higher TCR of platinum elements results in more positive non-linearity error, therefore different combinations of α_{Pt} and α_{TaN} may result in more advantageous sensitivity and linearity characteristics.

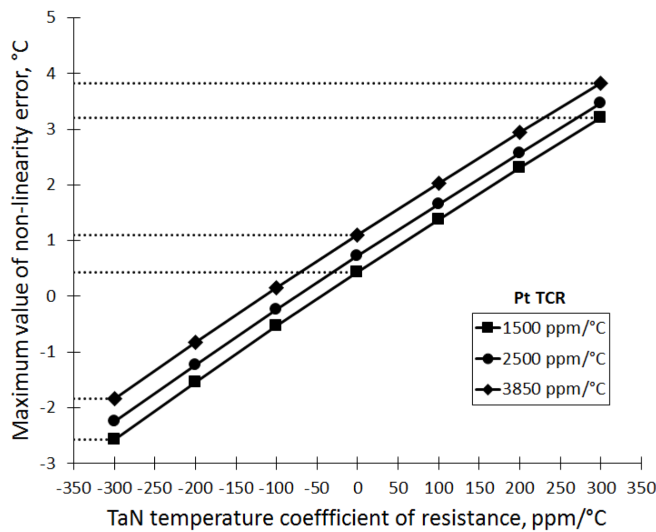

Figure 3.3.16: *Expected value of temperature response non-linearity error against TCR of TaN elements with different* α_{Pt} *(*R_{Pt}*:*R_{TaN} *= 0.06)*

Figures 3.3.17(a,b) show how changing the resistor ratio from 6% to 3% and 9% affects the linearity of response to temperature. Figures 3.3.16 – 3.3.17 demonstrate that TaN TCR has the largest effect on the non-linearity with higher positive values of TCR resulting in worse linearity while the resistor ratio and platinum TCR values lead to an offset in maximum non-linearity value.

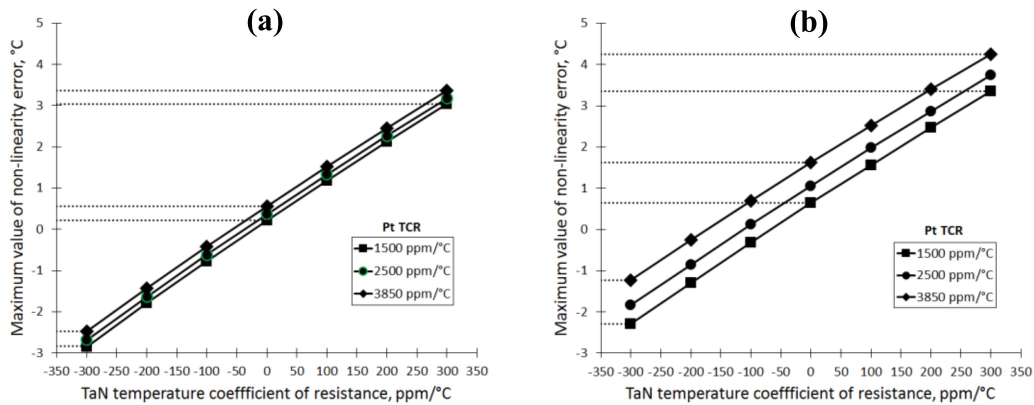

Figure 3.3.17: *Expected value of temperature response non-linearity error against TCR of TaN elements with different α_{Pt}:(a) $R_{Pt}:R_{TaN} = 0.03$; (b) $R_{Pt}:R_{TaN} = 0.09$.*

3.3.4 Comparison with most popular types of thermometer

Findings in sections 3.3.1 – 3.3.3 can be compared with the characteristics of popular temperature sensing methods in a temperature range of 25 to 300 °C. Characteristics of standard platinum resistance thermometer devices (for a 1 mA measurement current) and commonly used nickel and platinum-rhodium alloy thermocouples are summarized in Table 3.3.2 [4, 12, 13].

The sensitivity and linearity values (given in Table 3.3.2) of the temperature response from the Pt/TaN bridge circuit described in the current work are based on examples produced using a set of resistance ratios R_{Pt}/R_{TaN}, TCR values of 2500 ppm °C^{-1} for Pt and the range of TCR values for TaN given in Table 2.4.1. As shown in Fig. 3.3.5 the sensitivity to temperature is expected to be equal to at least 185 μV·°C^{-1} per percent of R_{Pt}/R_{TaN} when TaN TCR is zero, which will result in a value of higher than 1 mV·°C^{-1} for 15 V excitation voltage at a set resistor ratio value of 6%.

Table 3.3.2 *Temperature sensing performance of comparable thermometer types.*

Types		***Sensitivity***	***Largest error tolerance***	
Thermocouples				
Alloy base	*Type*	*dE/dT*	*Class 1*	*Class 2*
Ni	*E*	70.3 $\mu V \cdot {}^{\circ}C^{-1}$	± 1.5 °C	± 2.5 °C
	J	54.6 $\mu V \cdot {}^{\circ}C^{-1}$	± 1.5 °C	± 2.5 °C
	K	40.7 $\mu V \cdot {}^{\circ}C^{-1}$	± 1.5 °C	± 2.5 °C
	N	31.2 $\mu V \cdot {}^{\circ}C^{-1}$	± 1.5 °C	± 2.5 °C
	T	49.7 $\mu V \cdot {}^{\circ}C^{-1}$	± 0.5 °C	± 1.0 °C
Pt-Rh	*R*	8.1 $\mu V \cdot {}^{\circ}C^{-1}$	± 1.0 °C	± 1.5 °C
	S	7.8 $\mu V \cdot {}^{\circ}C^{-1}$	± 1.0 °C	± 1.5 °C
RTD-based thermometers				
Pure metal	R_0	dV_{RTD}/dT	*Class A*	*Class B*
Pt	*100 Ω*	385 $\mu V \cdot {}^{\circ}C^{-1}$	± 1.5 °C	± 2.5 °C
	1000 Ω	3850 $\mu V \cdot {}^{\circ}C^{-1}$	± 1.5 °C	± 2.5 °C
Current temperature transducer design				
Resistance ratio $R_{Pt}:R_{TaN}$	*TCR of balancing TaN elements*	dV_{OUT}/dT	*Maximum non-linearity error*	
3%	*150 ppm* C^{-1}	485.9 $\mu V \cdot {}^{\circ}C^{-1}$	± 1.85 °C	
	0 ppm C^{-1}	539.5 $\mu V \cdot {}^{\circ}C^{-1}$	± 0.4 °C	
	-150 ppm C^{-1}	602.7 $\mu V \cdot {}^{\circ}C^{-1}$	± 1.1 °C	
6%	*150 ppm* C^{-1}	933.8 $\mu V \cdot {}^{\circ}C^{-1}$	± 2.15 °C	
	0 ppm C^{-1}	1035.8 $\mu V \cdot {}^{\circ}C^{-1}$	± 0.75 °C	
	-150 ppm C^{-1}	1155.6 $\mu V \cdot {}^{\circ}C^{-1}$	± 0.75 °C	
9%	*150 ppm* C^{-1}	1347.1 $\mu V \cdot {}^{\circ}C^{-1}$	± 2.45 °C	
	0 ppm C^{-1}	1492.8 $\mu V \cdot {}^{\circ}C^{-1}$	± 1.1 °C	
	-150 ppm C^{-1}	1663.3 $\mu V \cdot {}^{\circ}C^{-1}$	± 0.35 °C	

3.4 Conclusions

A bridge-based temperature sensor can be built using tantalum nitride elements to produce a half-bridge balancing circuit and two platinum temperature sensitive resistors to provide high and linear sensitivity of response to temperature. The designed circuit is able to provide a linear response in a temperature range between 25 and 300 °C to serve as an application for a SiC-based instrumentation amplifier. It can also be expected that this temperature sensing circuit can be fabricated using

standard thin film, microfabrication post-processing on top of finished SiC integrated circuits.

The sensitivity to temperature of the bridge-based transducers is mostly defined by the temperature coefficient of resistance of thin film platinum. It is also expected to improve by increasing the platinum to tantalum nitride resistor ratio, which, in addition, governs the full-scale output range of the sensor. Sensitivity characteristics are notably affected by the temperature coefficient of the tantalum nitride film, where more negative values result in significantly better sensitivity at a cost of reducing the linearity of response. Different types of mismatch both in elements that constitute a balancing circuit and between temperature sensitive elements affect the sensitivity to an extent that is comparable with direct change of Pt TCR. From examples shown in this chapter it is evident that symmetric mismatch between diagonally opposite balancing resistors can produce an adverse effect on both sensitivity and output range. Linearity of temperature response is greatly affected by the TCR of TaN film resistors and it is therefore desirable to keep TCR of TaN close to zero or at a low negative value, which will result in lower expected non-linearity error.

A balance between resistor ratio and TCR values for each material has to be found depending on the obtained film parameters. It would be practical to design devices with multiple resistor ratios as possible change of sheet resistance values of according materials will invalidate the relation between intended resistor ratios and temperature response characteristics. It is expected that it should be possible to fabricate devices usable across the whole temperature range with sensitivity of the order of 750 $\mu V \cdot °C^{-1}$ in the worst case (allowing some mismatch in the balancing circuit) as compared to 385 and 70.3 $\mu V \cdot °C^{-1}$ values produced accordingly by 100 Ω SPRT resistors and type E thermocouple devices. The sensitivity value can be amplified by a factor of 10 using the instrumentation amplifier available on the SiC IC. Maximum non-linearity error can be expected to be better than error tolerance of Class A/Class 1 commercially available counterparts if balancing resistors have low negative to zero temperature dependence and will be comparable to Class B/Class 2 devices when TaN TCR is between 0 and 150 ppm $°C^{-1}$.

References

[1] M. Wijesundara and R. Azevedo, *Silicon Carbide Microsystems for Harsh Environments*. New York, USA: Springer, 2011.

[2] D. Wijngaards, M. Bartek, and R. F. Wolffenbuttel, "Silicon ic process compatible thin metal film post-processing module," *Sensors and Actuators A: Physical,* vol. 68, no. 1-3, pp. 419-428, 1998.

[3] D. D. L. Wijngaards and R. F. Wolffenbuttel, "IC fabrication-compatible processing for instrumentation and measurement applications," *IEEE Transactions on Instrumentation and Measurement,* vol. 50, no. 6, pp. 1475-1484, 2001.

[4] J. V. Nicholas and D. R. White, "Thermocouple Thermometry," in *Traceable Temperatures: An Introduction to Temperature Measurement and Calibration*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 295-342.

[5] N. Zhang, C.-M. Lin, D. G. Senesky, and A. P. Pisano, "Temperature sensor based on 4H-silicon carbide pn diode operational from 20 °C to 600 °C," *Applied Physics Letters,* vol. 104, no. 7, p. 073504, 2014.

[6] M. Berthou, P. Godignon, and J. Millan, "Monolithically Integrated Temperature Sensor in Silicon Carbide Power MOSFETs," *IEEE Transactions on Power Electronics,* vol. 29, no. 9, pp. 4970-4977, 2014.

[7] R. Ziermann *et al.*, "High temperature piezoresistive β-SiC-on-SOI pressure sensor with on chip SiC thermistor," *Materials Science and Engineering: B,* vol. 61-62, pp. 576-578, 1999.

[8] E. Haile, "Precision RTD Instrumentation for Temperature Sensing," ed. http://ww1.microchip.com/downloads/en/AppNotes/00001154B.pdf: Microchip, 2008 [Updated 2013].

[9] R. M. Stitt, "Implementation and Applications of Current Sources and Current Receivers," ed. http://www.ti.com/lit/an/sboa046/sboa046.pdf: Texas Instruments, 1990 [Updated 2000].

[10] "Signal Chain Design Guide - Devices For Use With Sensors," ed. http://www.microchip.com/stellent/groups/analog_sg/documents/devicedoc/en546110.pdf: Microchip, 2012.

[11] M. Braunovic, N. K. Myshkin, and V. V. Konchits, "Electronic Connections," in *Electrical Contacts: Fundamentals, Applications and Technology*, Boca Raton, USA: CRC Press, 2006, pp. 309-367.

[12] P. R. N. Childs, "Thermocouples," in *Practical Temperature Measurement*, Oxford, UK: Butterworth-Heinemann, 2001, pp. 98-144.

[13] J. V. Nicholas and D. R. White, "Resistance Thermometer Reference Tables," in *Traceable Temperatures: An Introduction to Temperature Measurement and Calibration*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 397-398.

Chapter 4 Development of thin film materials

4.1 Introduction

A combination of thin film materials, where each layer serves a different purpose, can produce an integrated temperature sensor system. In order to fit the sensor elements into a limited area a highly resistive thin film layer is required to produce balancing resistor elements, while the temperature sensing elements can be produced in a layer that is more conductive. Fabrication processes have to be designed with forethought to prevent affecting or damaging one layer while processing another, in addition to avoiding damage to underlying electronic circuitry. In this chapter, the development of thin film materials is described where the two layers are produced separately using processes that are compatible with monolithic integration.

Electrical properties of conductive metallic thin films depend strongly on fabrication processes that have been used to produce and process them. Different measurements need to be performed in order to evaluate whether the resultant films meet the required specifications. Of particular interest are measurements that allow tracking of how the electrical properties of a thin film layer have changed during processing, combined with measurements of physical quantities which support the understanding of why they have changed. This chapter will provide a description of measurements used, examine the interrelation between measurement results and show their practical value in terms of material development.

4.2 Crystallographic measurements

Crystallographic measurements are very important in material science because crystal structure defines the physical and electrical properties of metallic films [1-4]. The effect of crystal structure is even more pronounced in thin films, which are highly dependent on the fabrication method and deposition parameters used.

XRD identifies the parameters that are fundamental, which are crystal phase and degree of crystallinity [5]. Crystal phase can be found using the position of the peak on the intensity plot by comparison with the values supplied in powder diffraction files, while the degree of crystallinity may be evaluated by the sharpness of peak. Because these qualities of materials may change under working load or due to operating environment, it is very important to track these changes as they will directly affect the electrical characteristics.

4.2.1 Motivation

There are two types of restrictions which have to be addressed in order to produce a temperature sensing device that is reliable for a significant amount of time at elevated temperatures:

- *Operational stress*, which occurs to the device under the workload within the specified operational limits and within the designed temperature range [6].
- *Environmental stress*, which takes place when the device is exposed to the negative effects of elevated temperature, increased vibration, exposure to corrosion etc. [6].

The majority of effects related to operational stress will be diminished by correct layout of the temperature sensor, correct design of microfabrication processes, and well-judged specifications. For example, sensor element resistance values will be designed to be high enough to keep the electrical current low; therefore, the rate of current-induced degradation will be minimised [7]. This chapter will describe the development of thin films based on control of temperature and gas composition in the environment.

The changes to the film induced through exposure to different chemical environments or high vacuum at elevated temperatures during the fabrication stage are of interest in producing stable materials. The dominant threat to thin films is diffusion and distribution of contaminant atoms into the film, which have an irreversible effect and their rate increases with temperature [7]. There are two important effects produced by elevated temperatures in a high vacuum environment. The first effect is introduction of further physical stress and strain due to mismatch between the thermal coefficient of expansion of the thin film and that of the substrate that it is deposited on. The second effect is that it provides energy that can enable crystallization or recrystallization of thin film material.

There is no particular equation that could describe these three effects when they affect the film cumulatively. There is a good explanation, however, if these three effects are treated separately. The rate at which a thin film is affected by diffusion of contaminants and thermally-activated recrystallization at increasing temperature temperature in vacuum is well-studied and is usually expressed by the Arrhenius equation:

$$k = Ae^{-\frac{E_a}{RT}}, \qquad (4.1)$$

where A is constant, E_a is the activation energy, R is the ideal gas constant and T is the temperature [7-10]. The parameters A and E_a are constants specific to the particular process or reaction.

All metal thin films should preferably be deposited at elevated temperatures to decrease the amount of subsequent change in the film during annealing or later operational and environmental stress. However, such an option was not possible during this research due to the lack of high temperature metal deposition. In order to comprehend the crystallization phenomenon in metallic thin films, the following has to be considered:

- A minimum energy is needed to start thermally activated crystallization, and the most effective source of energy is temperature as governed by an Arrhenius-type expression [7].
- The solid phase film may change its structure from metal amorphous or metastable crystalline into an energetically more preferential one before a

unique, thermodynamically stable phase is formed [11]. The selection of phases is constrained in thin films because of the limited volume to surface area ratio.

- Lower temperatures are required for a post-deposition temperature treatment profile that uses a longer annealing time value [7]. Correct proportions of time may be estimated using Arrhenius equation (eq. 4.1).

The temperature at which recrystallization occurs depends both on the thin film composition and the previous history of exposure to high temperatures and different environments [7, 11]. As a general rule, if the thin film structure is stable at higher temperatures, it should stay stable at low temperatures unless it is under a larger effect of physical stress- or corrosion-related degradation [7]. Therefore, it is extremely important to track the crystal phase transition or recrystallization and make sure whether any of these processes have taken place or all of these processes have finished. In summary, if a film is required that can operate for extended periods in extreme conditions, it should be processed in such a way that it is in a highly thermodynamically stable state before it is used.

4.2.2 Basic features of XRD measurement

Each crystalline structure is unique, which results in specific intensities of X-ray beam diffraction from the measured sample when focussed at different angles [12]. Bragg diffraction law describes how the intensity pattern is produced by interference of waves scattered within the material of certain crystal structure. Fig. 4.2.1(a) illustrates an example of how X-rays penetrate into the sample and diffract from a plane and it can be shown that in order to satisfy the condition for diffraction maximum the path difference $\delta = n\lambda$ travelled by an X-ray beam needs to be a multiple of wavelength:

$$n\lambda = 2d_{hkl}\sin\theta, \qquad (4.2)$$

where d_{hkl} is interplanar spacing for a particular atomic arrangement and θ is the scattering angle [13].

When the incident beam diffracts in the sample containing multiple crystal orientations, a stereographic projection of detected X-rays creates circular patterns

called Debye-Scherrer rings such as shown in Figure 4.2.1(b). When the sample is slowly rotated in a single plane in reference to the detector, the measured diffraction intensity data are used to plot the diffraction pattern against the different measurement angles producing a diffractogram as shown in Fig. 4.2.1(c).

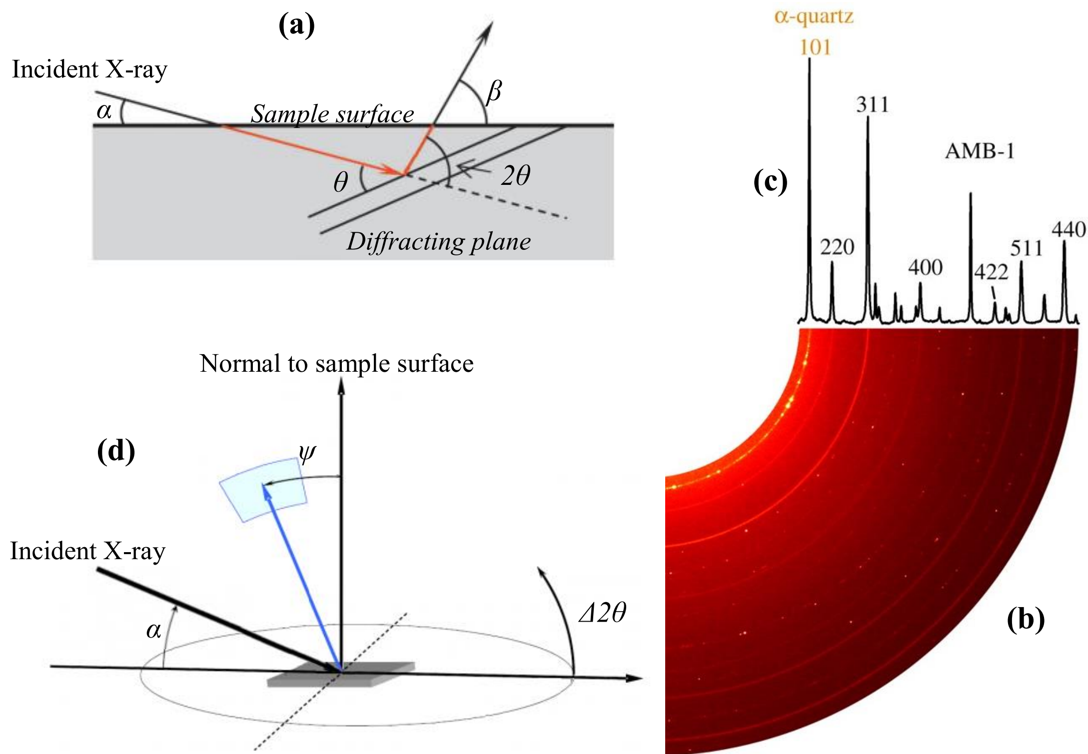

Figure 4.2.1: *Illustration of (a) X-ray diffraction, (b) resultant Debye-Scherrer representation and (c) equivalent XRD diffractogram, (d) out-of-plane GIXRD measurement. Adapted from Mitsunaga [14], Fischer et al. [15] and Inaba et al. [16].*

There are two different ways of measuring the crystal structure of a metal film using the XRD technique. In-plane XRD techniques are based on diffraction from planes that are normal to the sample surface whereas out-of-plane techniques are based on diffraction from crystalline planes that are parallel to the sample surface [17]. A conventional powder diffractometer using Bragg-Brentano configuration would not be suitable for analysis of a thin film that is deposited on a relatively thick substrate, because it results in domination of irrelevant background intensities and overwhelming diffraction from the substrate [14]. In order to overcome this drawback a grazing incidence XRD (GIXRD) technique is used, which allows increasing the diffraction intensity from the thin film material by decreasing the

X-ray penetration depth into the substrate [12, 14]. For out-of-plane measurements this approach is also termed as the asymmetrical technique [14]. The diffractometer keeps the small incident angle α constant while scanning the diffraction intensity across horizontal 2θ axis at speed of Δ2θ within the set radial limits and registering the diffraction intensities from the planes that are inclined to the sample surface across the mentioned axis. Angle values ψ_n are formed between the normal vectors of the sample and of the diffracting planes as shown in Fig. 4.2.1(d).

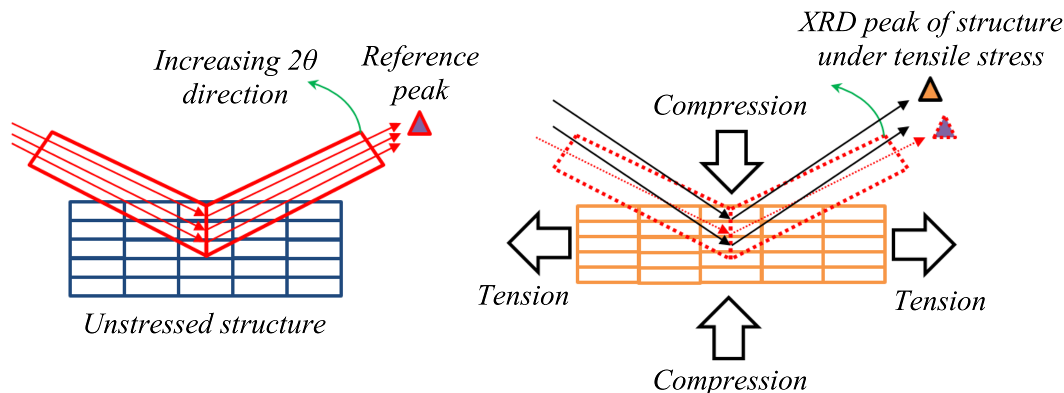

Figure 4.2.2: *Illustration of tension effect on the XRD plot of a crystalline sample.*

X-ray diffraction (XRD) is a powerful technique that allows identifying the crystalline structure of the measured sample and, when the list of chemical elements constituting the sample is known, XRD enables an estimation of the amount of defects in crystal structure, the order of crystallinity of material and also the degree of stress within the material. As a result, in addition to identifying the crystalline structure parameters, comparison of the observed diffraction peaks with those produced from reference samples stored in powder diffraction files (PDF) creates the possibility of studying effects of processes used to produce the measured sample on fundamental properties (such as mechanical and electromagnetic) of the material [5]. As a general observation, the height to width ratio of diffraction intensity peaks reveal the preferred crystalline orientation of thin film; therefore any change to this ratio refers to material recrystallization [13]. A large amount of background diffraction intensity with a pronounced pattern is usually regarded as diffraction from amorphous phases. Finally, any simultaneous change of detected peak width and its offset as compared to the well-studied value from a powder diffraction file may be

regarded as the contribution of added or reduced physical stress [13]. An example of the diffractograms produced by the samples affected by the increasing tensile stress in film (resulting in compressive stress in normal axis through Poisson effect) is shown in Figure 4.2.2.

4.2.3 Experimental setup and sample fabrication

During this research two different XRD tools have been used, which translated into slightly different measurement results and their accuracy. The first was a Siemens D5000, provided for use by the Thin Film Centre at the University of West of Scotland, and was set up to measure the diffraction data with a 2θ step of 0.02° across the range of 15° to 75°. The second tool was a Bruker D8 Advance, accessed through the School of GeoSciences at the University of Edinburgh, which allowed measurement of the diffraction pattern with a 2θ step of 0.03448° in a range of 10° to 74°. Both these tools were set up for thin film measurements by the respective institutions; therefore no other parameters affecting the diffraction measurements were changed from their active settings.

Both diffractometers required samples of 1×1 cm^2 to be produced to fit the sample holder. After the required fabrication processes were performed, the samples were cleaved from silicon wafers covered by a blanket layer of the metallic thin film to be studied. These were taken from the area closest possible to the center of the wafer and it is assumed that they are representative of the tested and developed processes.

4.2.4 Example measurements

A set of reference GIXRD measurements was performed on Si samples that did not contain any metallic thin films to understand the influence of the substrate on future thin film measurements. The observed peaks are useful to discriminate the metal thin film intensity peaks from substrate-related peaks. The first measurement was performed on a thermally oxidised (nominally 500 nm SiO_2) silicon wafer. Figure 4.2.3 shows a plot of the square root of diffraction intensity against the

measured diffraction angle 2θ, where two detected peaks can be seen. The peak with the highest intensity shows (400) silicon phase (69.13°, PDF#27-1402 [18]), which is an expected result when performing such a measurement on a cubic (100) silicon substrate [12]. Another peak that has been detected is related to (212) thermal SiO_2 phase (33.127°, PDF#47-1300 [18]). While thermal oxide is usually regarded as an amorphous material, it has been shown in the literature that there is a chance that some volume of thermally oxidised silicon can have a crystalline structure [19, 20]. Figure 4.2.3 also illustrates the point that it is impractical to show the silicon-related peak, because it completely overwhelms the graph.

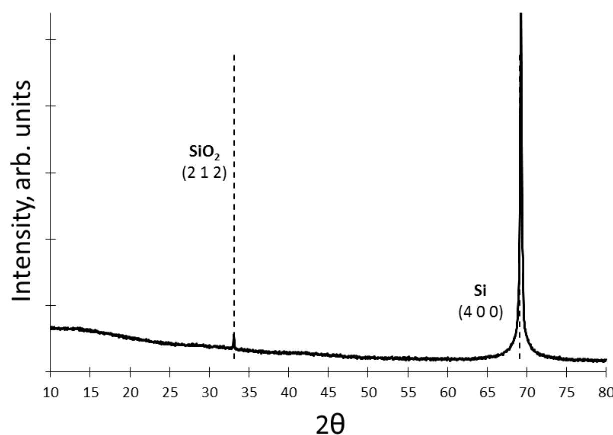

Figure 4.2.3: *XRD measurement result of an oxidised silicon wafer sample.*

More samples were fabricated using two thermally oxidised silicon wafers. One of the wafers was coated with low-frequency plasma-enhanced chemical vapour-deposited (PECVD) silicon oxide with a target thickness of 500 nm deposited over 12 minutes using an STS Multiplex PECVD tool. This type of oxide is known to be amorphous, which should be well indicated on the XRD intensity plot [21]. Following from this, both wafers were vacuum-annealed for 6 hours at 600°C. Two sets of measurements were performed on processed samples and as a result, each wafer sample was measured from both sides – polished (Figure 4.2.4(a,c)) and unpolished (Figure 4.2.4(b,d)). Measurement results of the backside are interesting in terms of finding out how processes affect the backside while processing the working surface of the wafer.

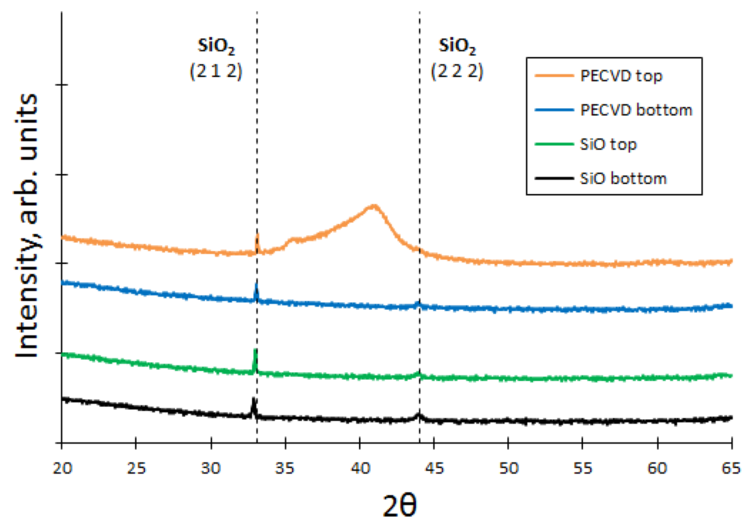

Figure 4.2.4: *XRD sample measurement results: Annealed oxidised silicon wafer covered by PECVD oxide: (a) frontside, (b) backside; Annealed oxidised silicon wafer: (c) frontside, (d) backside.*

Figure 4.2.4(a) shows that PECVD oxide is in fact amorphous because there are no visible peaks related to this layer, and the increased detected intensity is spread over at least 2θ = 5° range. As compared to Figure 4.2.2, the appearance of a new peak can be noticed on both sides of thermally oxidised silicon sample (Fig. 4.2.4(c),(d)) and also at a smaller scale on the backside of the sample that has been processed in PECVD tool (Fig. 4.2.4(b)). This (222) SiO_2 peak (44.005°, PDF#27-0605 [18]) may have appeared due to repeated temperature cycling of thermal oxide-silicon interface, and can be seen on both sides of the wafer.

4.3 Electrical measurements

Electrical measurements were required to track material properties before and after the thin film layer was affected by different processes. Development of metallic thin film materials was usually carried out in batches using film samples fabricated within a single deposition process. Samples have been measured electrically after deposition using the four-point probe. Following from that, different additional processes that affect thin film properties were performed on selected samples and

thin film properties of the latter were measured once again using the cleanroom equipment or equipment based in the test lab.

4.3.1 Measurement basics

Electrical resistivity ρ is a fundamental property of a conductor that describes the opposition of the material to electrical current. The relation between the electrical resistance R of a conductor with the constant rectangular cross section geometry shown in figure 4.3.1 is expressed using:

$$R = \rho \frac{L}{Wt}, \ (\Omega) \tag{4.2}$$

where L is the conductor length, W is the width and t is the thickness.

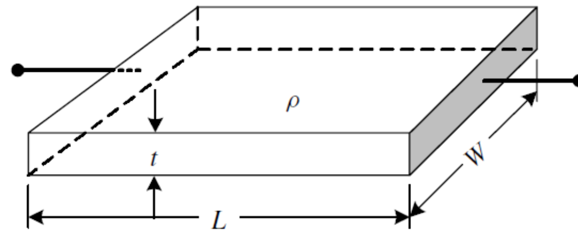

Figure 4.3.1: *Schematic illustration of geometrical relationship of resistivity-related electrical parameters [22].*

The resistivity of thin films considered to have a uniform thickness is usually expressed as a sheet resistance R_S which is related to the resistivity by:

$$R_S = \frac{\rho}{t}, \ (\Omega/\square) \tag{4.3}$$

The units of sheet resistance are Ohms per square, giving the resistance of any square segment (i.e., $W = L$) of a thin film with constant thickness. Henceforth, when providing electrical measurement results, the sheet resistance value for the particular film thickness will be used. To find the resistance of a conducting feature of length L and width W from the sheet resistance one can use:

$$R = R_S \frac{L}{W}, \ (\Omega) \tag{4.4}$$

Both blanket layer- and test structure-based tests have been used to characterize thin film materials. Three different types of measurements have been utilised, which are based on similar techniques:

- *Four-point probe* measurements, which are performed on blanket metallic thin film deposited on oxidised silicon wafers;
- *Greek Cross* measurements, which are performed using fabricated test structures;
- *Bridge* resistance test structure measurements, which are performed using fabricated patterned resistive lines or *Cross-Bridge* test structures.

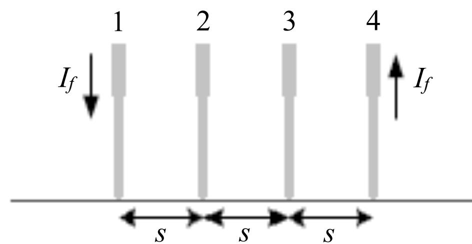

Figure 4.3.2: *Illustration of four-point probe measurement. Adapted from Schroder [22].*

Four-point probe technique is fundamental but straightforward and is based on the measurement of electrical potential difference in a longitudinal line where the electrical current is flowing. It uses four equally spaced probes (Figure 4.3.2), where current is forced from node 1 to node 4 while voltage is measured between 2 and 3. The resultant measured sheet resistance value may be expressed as:

$$R_S = \frac{\pi}{\ln(2)} \frac{V_{23}}{I_{14}}, \ (\Omega/\square) \tag{4.5}$$

which is correct whenever the measured thickness of material is less than or equal to half the distance between the probes. In this work this ratio will not come close to 1:1000.

Greek Cross measurement is a variant of four terminal measurement performed using the van der Pauw method [23]. The geometry of the test structure allows saving a significant amount of space while essentially performing the same measurement as described previously. Four measured nodes are arranged in a square (Fig. 4.3.3 left),

where current flows from node 1 to node 2 and voltage is measured between nodes 3 and 4.

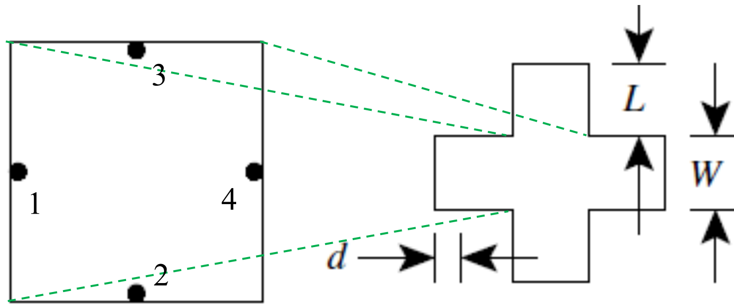

Figure 4.3.3: *Illustration of Greek Cross structure: (left) square sample geometry of test structure and (right) parameters of test structure that affect the accuracy of measured value. Adapted from Schroder [22].*

There is an error associated with the geometry of Greek Cross test structure, but its effect on the measurement can be brought to minimum provided that the current supply and voltage probe distance values d (see Figure 4.3.3 right) are more than or equal to twice the width W of the square measurement sample [24]. Similarly to four point probe measurement the measured sheet resistance value can be described using:

$$R_S = \frac{\pi}{\ln(2)} \frac{V_{34}}{I_{12}}, \ (\Omega/\square) \tag{4.6}$$

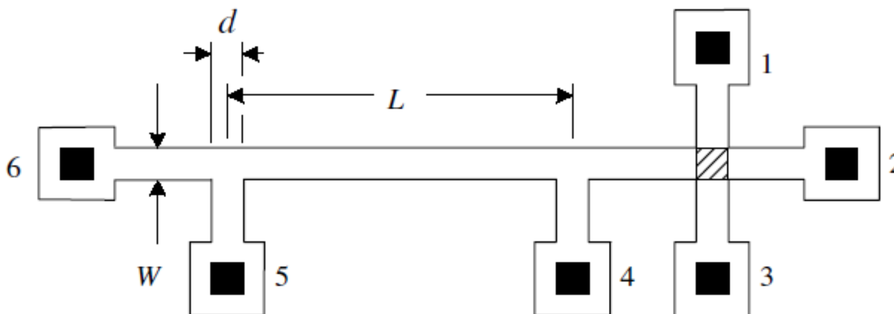

Figure 4.3.4: *Illustration of Cross-Bridge measurement [22].*

Bridge resistance test structures are usually used for measuring the electrical linewidth (as opposed to the designed linewidth). These structures were used to overcome the sensitivity limitations of the measurement setup used for material characterization described in this chapter. These structures allow measuring a

significant number of material square sheets (as opposed to the Greek Cross test structures, where a single square sheet is measured). This resulted in increased measured voltages, which was useful both in terms of measurement accuracy and precision. There is an error associated with the fact that voltage taps increase the effective width of the measured line (Figure 4.3.4). This can be minimised by making sure that voltage tap width d is less or equal to the line width W and the latter is at least 20 times narrower than the bridge length L [25]. The measured resistance value can be expressed using the following equation:

$$R = \frac{V_{45}}{I_{14}} = R_S \frac{L}{W}, \ (\Omega) \tag{4.7}$$

Kelvin measurement is a resistance measurement technique that uses separate pairs of current-forcing and voltage-sensing terminals, which results in elimination of lead and contact resistance from the measured electric circuit [22]. In any single Kelvin measurement there are errors associated with voltage offset at inputs and thermoelectric voltages, hence it is very practical to perform Kelvin measurements in all pertaining current paths and directions and take the average of measured values.

In order to measure temperature coefficient of resistance (TCR) any of the aforementioned measurements may be used provided that the measured structure is heated controllably. The change of resistance ΔR or sheet resistance ΔR_S due to a change in temperature of $\Delta T = T - T_0$ in the general case is expressed using the following formula:

$$\frac{\Delta R}{R} = \frac{\Delta R_S}{R_S} = \alpha \Delta T, \tag{4.8}$$

where R is the value measured at initial temperature and α denotes a linear TCR. Hence TCR can be found using following expression:

$$\alpha = \frac{\Delta R}{R \Delta T} = \frac{\Delta R_S}{R_S \Delta T}, \ (^{\circ}\mathrm{C}^{-1}) \tag{4.9}$$

4.3.2 Test structures for electrical thin film characterization

Greek Cross and Cross-Bridge test structures have been designed according to design rules mentioned in subsection 4.3.1. The layout of test pads has been selected

so that it would be compatible with a standard test setup that uses 4×2 arrays of probe needles with a 240 µm pitch to enable electrical measurements.

Figure 4.3.5(a) shows the layout of the designed Greek Cross test structures with arm widths of 10 µm, 15 µm and 20 µm. The arm length, before the first right angle, is at least $2W$ in each structure. Figure 4.3.5(b) shows the designed Cross-Bridge structures with geometric parameters (L/W) of 480 µm/20 µm and 480 µm/10 µm. Both test structure designs include the contact pads produced using a different material to protect the material under test from probing damage and to enable a better probing contact with the measured material.

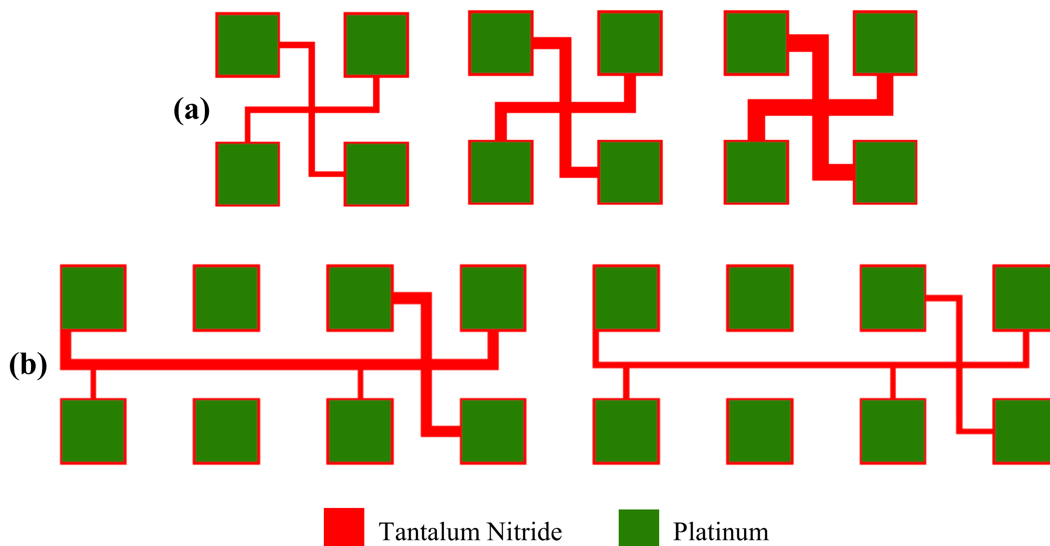

Figure 4.3.5: *Designed (a) Greek Cross and (b) Cross-Bridge test structures.*

4.3.3 Experimental setup

The test setup designed (see Fig. 4.3.6) for electrical experiments related to thin film development used a parametric semiconductor analyser HP4156B (2) to perform electrical measurements, a Micromanipulator 6200 manual prober (9) to provide electrical connection to the test structures and a HCP208SC hotplate (7) run by PID temperature controller HCP208SC-STC20U (4) to control the temperature of the sample under test. The temperature controller was connected to a LN2-P2UF2 liquid nitrogen pump (5) to allow cooling of the hotplate. The HP4156B was used to supply 1 mA current to the test structures and measure the resulting voltage using the ±2 V

range, which allowed 2 μV measurement resolution. The temperature controller allowed setting the chuck temperature with 0.1 °C precision up to 140 °C.

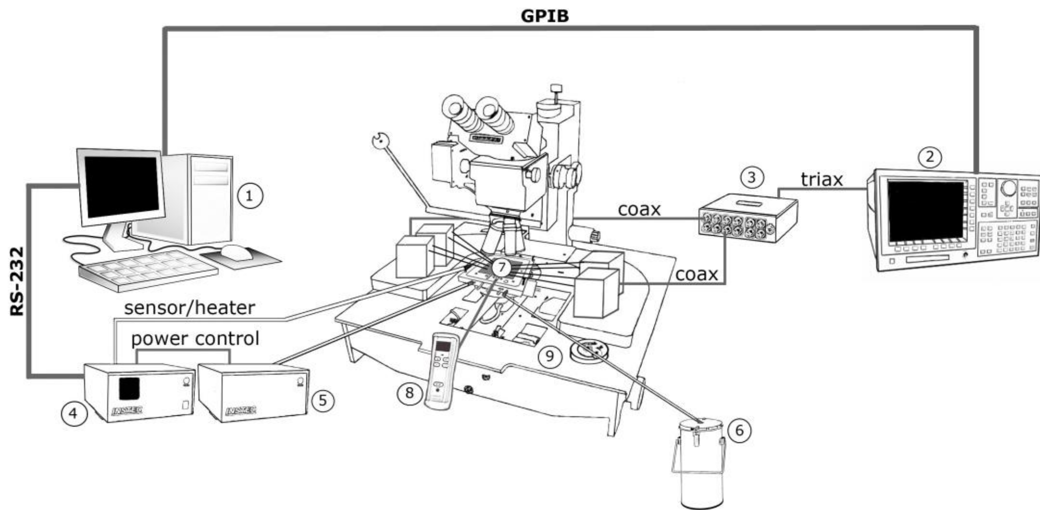

Figure 4.3.6: *Test setup designed to characterize developed thin films. 1: PC, 2: Parametric semiconductor analyser, 3: Coax-triax BNC box, 4: PID temperature controller, 5: Liquid nitrogen pump, 6: Nitrogen flask, 7: Hotplate, 8: Reference thermocouple reader, 9: Manual prober.*

Before starting a measurement session, temperature calibration was carried out because this is critical in order to set up a measurement environment that allows accurate determination of the TCR. The temperature controller PID values were first calibrated using a built-in auto-tune routine in order to set and stabilize the temperature precisely. Then the temperature measured by the PID controller was calibrated against measurements made using a Kane May KM3002 thermometer reading thermocouple soldered to the surface of a silicon wafer. This involved both ramping up to temperatures higher than 100 °C and cooling down below 10 °C.

An offset was observed between values measured by temperature controller and thermocouple, which grew linearly with increasing temperature (Fig. 4.3.7). Therefore, in this chapter the quoted temperature value will be the corrected value based on this calibration rather than the set point temperature from the controller. It was found that below the dew point a significant amount of condensate accumulates on the surface of both hotplate and wafer, which starts to crystallize into ice around

0 °C; hence the minimum temperature used was set to 25 °C. The maximum temperature was limited to 125 °C.

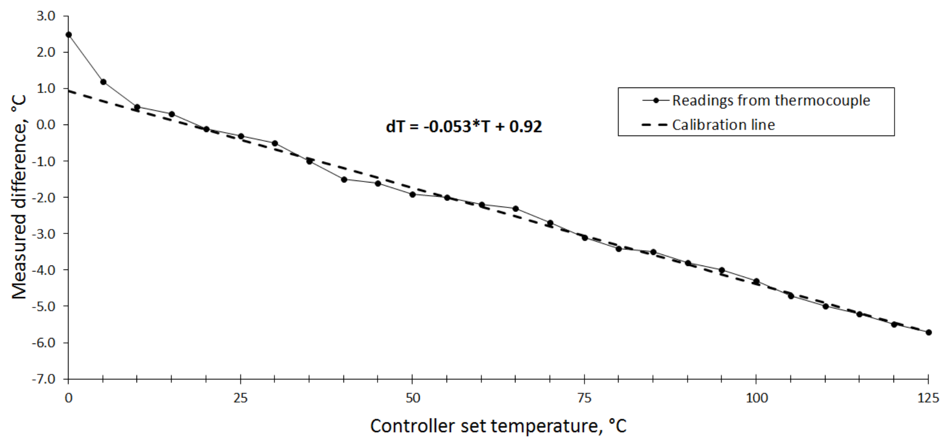

Figure 4.3.7: *Temperature calibration plot.*

LabVIEW software was used to create interfaces that control the temperature controller (STC-200) and the parametric analyser (HP4156B) in semi-automatic mode. The block diagram of main and device-related library virtual instruments is shown in Figure 4.3.8.

There were a number of significant physical limitations that existed in the test environment that could not be eliminated. The most important related to automatic range switching, which was interrupting the continuous measurement and increasing the time required to take a set of Kelvin-type measurements significantly. For example, if the probe contact to measured material resistance value was changing significantly, it was visible as a measured change of the voltage offset on the probes. The latter in particular was the primary reason why this test setup required manual decision making and additional input from the user (refer to Fig. 4.3.8).

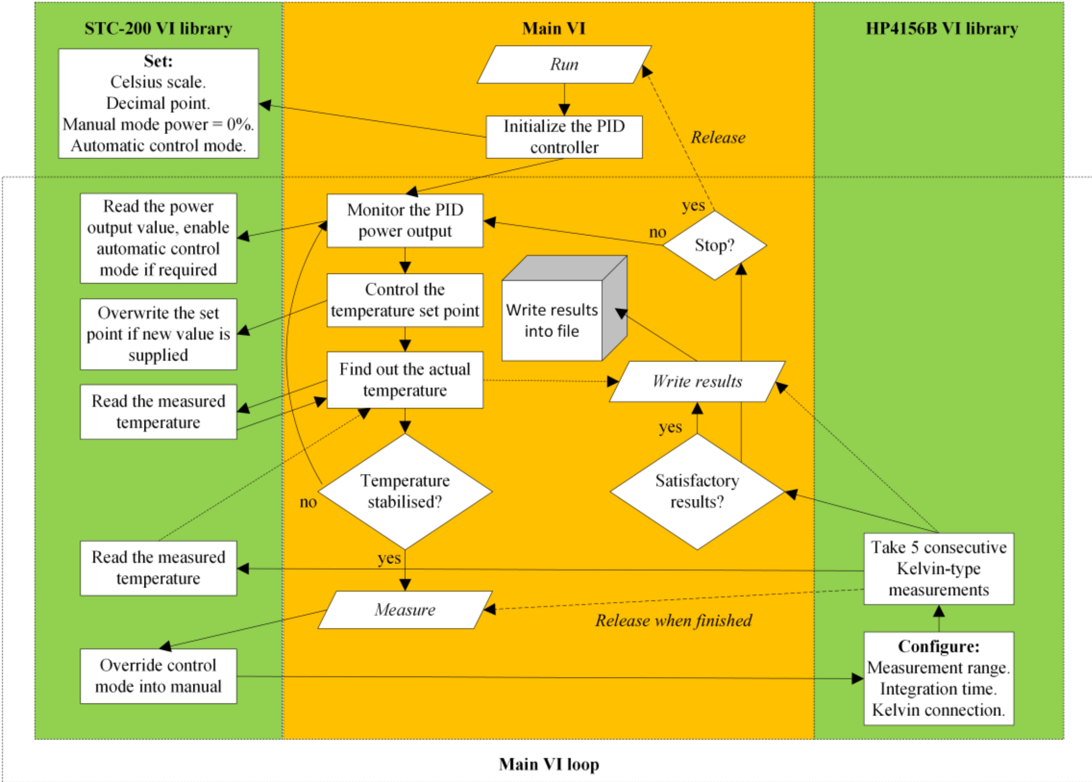

Figure 4.3.8: *Block diagram of virtual instrument functional flow.*

4.4 Development of tantalum nitride process

Tantalum nitride is a commercially accepted material for production of resistor elements that have a low dependence on temperature and are able to withstand harsh environment conditions. TaN is usually produced using thin film sputtering technology and it allows different electrical performance that is suitable for a variety of applications. It is a very attractive material for both research and industry because it has customisable resistance value as well as temperature coefficient of resistance value profiles, which depend on deposition and processing parameters and environment.

4.4.1 Introduction

The available thin film deposition method (DC magnetron sputtering) produces β-Ta phase, as shown in many examples in the literature [26-29]. This material has a tetragonal crystal structure and higher as-deposited resistivity ($\rho_{\beta\text{-Ta}} \approx 170 - 210\ \mu\Omega\cdot\text{cm}$) as compared to bulk α-Ta phase, which has a cubic crystal structure [30]. It is possible to craft tantalum compound resistors with TCR values that are incredibly stable over a wide temperature range by incorporation of nitrogen into the composition of thin film [31]. Thin films developed by the tantalum nitride process were required to have the following properties:

- Stability when exposed to environmental stress;
- TCR values that are close to zero and stay stable at elevated temperatures;
- Manufacturability using available deposition and post-deposition processes.

Thin films with such properties can be produced using the reactive sputtering deposition method in which a tantalum target is sputtered and the chemical reaction of tantalum and nitrogen occurs in argon gas at low pressure. Composition of the thin film can be modified by setting the ratio of nitrogen and argon gas flow values. The crystallinity of the resulting thin film is defined by the process parameters used in deposition and the subsequent annealing process. However, the possible crystalline phases are limited by the ratios of tantalum and nitrogen in the compound material. This principle is illustrated in a binary phase diagram (refer to Fig. 4.4.1), where for constant temperature and pressure values the resultant crystalline phase depends strongly on atomic composition of the film. Certain regions are expected to produce the mentioned tantalum nitride phases and in the neighbourhood of two regions it can be expected to result in a mixture of phases.

Primary criteria for selection of the correct fabrication process parameters were results from non-destructive measurements of microstructure using XRD (because thin film TaN atomic composition measurement techniques, such as X-ray photoelectron spectroscopy (XPS), energy-dispersive X-ray spectroscopy (EDX) or Auger electron spectroscopy (AES) were not available) in conjunction with electrical resistance measurements using different four-terminal methods. A combination of deposition and processing environment parameters can be used to produce thin films

with different resistance profiles and they can also adjust the phase content in the film compound [32].

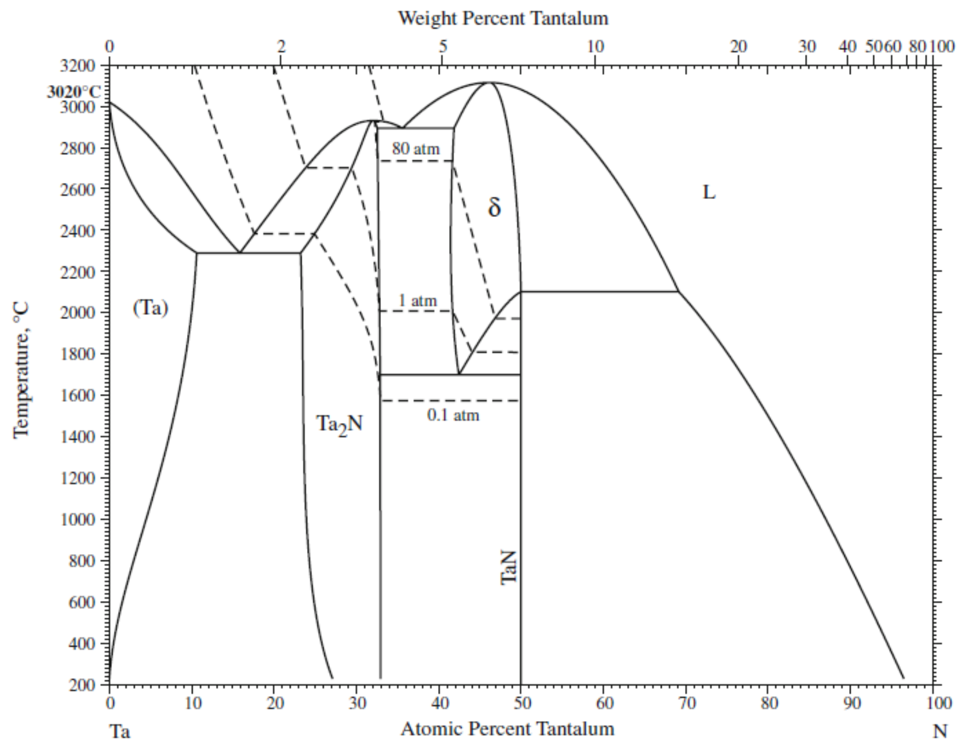

Figure 4.4.1: *Tantalum-Nitrogen phase diagram [33].*

Tantalum nitride can be etched by reactive ion etching using fluoride-based chemistry and a process has been developed to etch ~200 nm of thin film material. This process allows highly anisotropic etch profiles with sidewall angles of up to 90°, which improves matching and yield of thin film resistive elements.

4.4.2 Preparation and characterization of initial tantalum nitride samples

Several silicon wafers with 0.5 µm thermal oxide were prepared for initial thin film thickness measurements using a Dektak surface profilometer, and sheet resistance measurements using a Veeco FPP5000 four-point prober. Three wafers were patterned for lift-off using AZ5214E image reversal photoresist to be able to measure the thickness of deposited thin film produced by processes with three deposition time values as etching the film would most likely result in overetching into silicon dioxide layer.

Development of tantalum nitride started with deposition of thin films produced with the minimum possible N_2 flow setting available on OPT Plasmalab sputtering system. Values of 5 standard cubic centimetres per minute (sccm) for nitrogen gas and 45 sccm for argon gas were used (10% nitrogen flow ratio), the process pressure was set to 3 mTorr, tantalum target sputtering DC power was 500 W. 30 minute deposition steps with 5 minute breaks were used to produce thin films of different thicknesses with total deposition times of 30, 60 and 90 minutes. Sheet resistance was measured on blanket thin film samples while the thickness of deposited layer was measured on test structures produced by lift-off. The average measured sheet resistances of films produced by 30, 60 and 90 minute deposition runs were 36.9, 18.2 and 11.9 Ω/□ respectively. The lift-off process was performed using ACT CMI-S resist stripper with help of ultrasonic agitation. The average measured thicknesses for each deposition time were 67±3, 140±3 and 208±5 nm, which indicated an average deposition rate of 2.33 $nm \cdot min^{-1}$.

By comparison, a tantalum sputter deposition for 30 minutes without nitrogen gas (50 sccm Ar) produced a thin film with 24.6 Ω/□ sheet resistance, which comes both from the effect of lower resistivity and higher thickness as it leads to pure tantalum in the film and increased deposition rate. This indicated that film produced by 10% nitrogen flow ratio process is of quite high tantalum content as indicated by comparison with results from the literature [34-37]. It was found that the alignment of the wafer during the load stage is important for cross wafer uniformity control. Therefore, in all subsequent TaN deposition runs the wafers were loaded with the flat aligned at right angles to the radius of the rotating wafer carrier. One carrier wafer was used per one 3” wafer.

4.4.3 Thin film tantalum nitride patterning

There were three microfabrication processes available to produce patterned features in tantalum nitride thin film layers sputtered at room temperature: lift-off, dry etching and wet etching. Each of these methods has benefits and drawbacks which are critical for production of well-matched thin film resistive elements.

Lift-off is a method where the photoresist is patterned first and serves as a sacrificial layer for a thin film material that is deposited on top [38]. Lift-off is a patterning method that has ideal selectivity as there is typically no etching of the deposition substrate. However, the yield of integrated circuits produced in this way is relatively poor for reasons including defects in resist and low metal fill ratio which can increase retention of metal on the substrate and redeposition of lifted off metal particles in areas with high metal fill [38]. In contrast, a wet etching process would result in high yield, but produce an isotropic sidewall profile (as in Fig. 4.4.2 left), which would negatively affect the electrical linewidth of the produced features and also introduce further matching problems through etch bias effects [39].

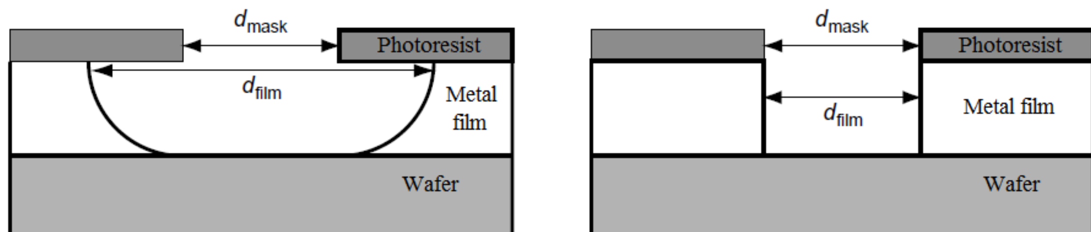

Figure 4.4.2: *Example etch profiles: (left) isotropic profile of wet etch process and (right) anisotropic profile produced by dry etch process [40].*

Dry etching has been selected in order to improve the thin film patterning process and minimise defects. Dry (reactive ion) etching using fluoride gas plasma allows outstanding anisotropy for thin TaN films (such as in example in Fig. 4.4.2 right), which is defined by observations of nearly vertical sidewalls (similar result reproduced in Fig. 5.4.7) [41]. As a result this will maximise the yield and improve matching of fabricated device elements.

The initial tantalum thin film dry etching process was attempted on 70 nm thick TaN film with a 1.5 µm thick Microposit SPR350 resist mask pattern. A JLS RIE80 reactive ion etching tool was used with following parameters: process pressure was set to 150 mTorr, RF power to 50 W, and gas flow controllers to 60 sccm for CF_4 and 3 sccm for O_2. The average measured height of steps produced by etching the 70 nm sample for 10 minutes was 80 nm, which indicated that the metal was over-etched and the silicon oxide was attacked. A separate run was performed on a thermally oxidised wafer, where the SiO_2 thickness was measured using a Nanospec

reflectometer, to find out that the thermal oxide was etched by this process at an average rate of 6.6 nm·min^{-1}. It was later found using SEM measurements that the sidewall angle created as a result of this SiO_2 etching process recipe was 67°. The estimated average etch rate of TaN film on a 3” wafer was greater than 8 nm·min^{-1}.

Subsequently a 210 nm thick TaN film was etched for 30 minutes using the same process parameters. A process time of 25 minutes was not sufficient because of evident non-uniformity of the etch process leading to some areas being clear of metal with other areas under-etched.

4.4.4 Environment- and temperature-related effects on thin films

A widely known tantalum nitride property is creation of a self-limiting Ta_2O_5 oxide passivation layer, which further improves the stability of the film as it protects the film from corrosion [8, 42]. In order to speed up oxidation and nitridation processes, the process temperature has to be increased significantly from the room temperature [7, 8, 42]. Heat treatment parameters will govern the resultant sheet resistance and temperature coefficient of the thin film and stability of these properties over time. One of the major factors of thin film stability at high temperatures is produced by thermally-activated recrystallization and the effect of the latter may be quantified using the Arrhenius equation. This phenomenon will affect the film texture and may lead to changes in structure of the material, which will influence the resistance and cause it to drift away from the initial value. For example, the Arrhenius-type equation provided by a passive electronic component manufacturer that describes the difference in temperature-related thin film electrical resistance drift for same electrical operating conditions but different temperature can be rewritten as:

$$\frac{\Delta R}{R(T)} = 2^{\frac{T-T_0}{30K}} \frac{\Delta R}{R(T_0)}, \tag{4.10}$$

where T is the hypothetical operating temperature and T_0 is reference temperature which is used to estimate the effect of temperature on electrical characteristics [43]. It is expected that an increase of temperature by 30 K will double the rate of change of electrical resistance of TaN thin films.

Tantalum/tantalum nitride is known to be affected significantly by nitrogen environment at elevated temperatures [44, 45]. This property can potentially be useful for thin film processing as the proportion of nitrogen and tantalum in the film defines the crystalline structure and resultant electrical resistance. The primary reason why processing of the film in a nitrogen environment needed to be explored was that the tantalum sputtering tool offered control of nitrogen flow ratio with only 2% step, hence it might not be possible to produce a thin film with the sought after characteristics because the composition of thin film produced by each step in N_2 flow ratio would be significantly different.

Therefore, a second experiment was designed to check whether nitrogen content in the TaN film can be adjusted reliably during high-temperature annealing in nitrogen ambient after deposition and produce an effect equivalent to a doping process in semiconductors. It was also important to find out whether a TaN film treated by such a process would be suitable to be used as a part of an electrical circuit. Researchers have tried annealing tantalum-based films in a nitrogen environment at temperatures higher than 500 °C, but unfortunately the resulting electrical resistance of the materials has not been disclosed [45, 46]. During this research the effect of annealing in a nitrogen environment was studied using samples deposited using the minimum possible nitrogen flow ratio of 10%.

Three wafers were produced using TaN deposition times of 30, 60 and 90 minutes. Thin film samples produced had thickness values of accordingly 67, 140 and 208 nm as measured earlier by Dektak 8 profilometer. Each wafer was cleaved into four shards and shards were measured (average values for shard groups of respective thicknesses were R_s = 36.8, 17.9 and 11.7 Ω/□) using the four point prober before performing any high-temperature treatment. The HITEC high-vacuum furnace was used to produce a 190 mTorr nitrogen environment at different temperatures. The furnace was set up to ramp up from 200 °C to the set temperature and back down again in the low pressure nitrogen environment at a rate of 5 °C per minute. The value of load temperature was selected to keep oxidation and nitration of the TaN thin film in the cleanroom atmosphere to minimum. Four point probe measurements were repeated to find out the value of thin film sheet resistance after

the samples have been processed. The relative change of measured sheet resistance values are given in Table 4.4.1 below.

The significant colour change of films has appeared after 30 minutes of annealing in nitrogen as shown in Fig. 4.4.3. This did not happen to any sample that was annealed in vacuum (described in subsection 4.4.5), which suggests that the colour change is related strictly to the creation of a thin film layer that passivates the film. Samples of all thicknesses annealed for 5 hours at 600 °C became completely passivated as indicated by drastic discolouration and a measured sheet resistance value of at least 450 kΩ/□ (which is the maximum sheet resistance range value of used four point probe device).

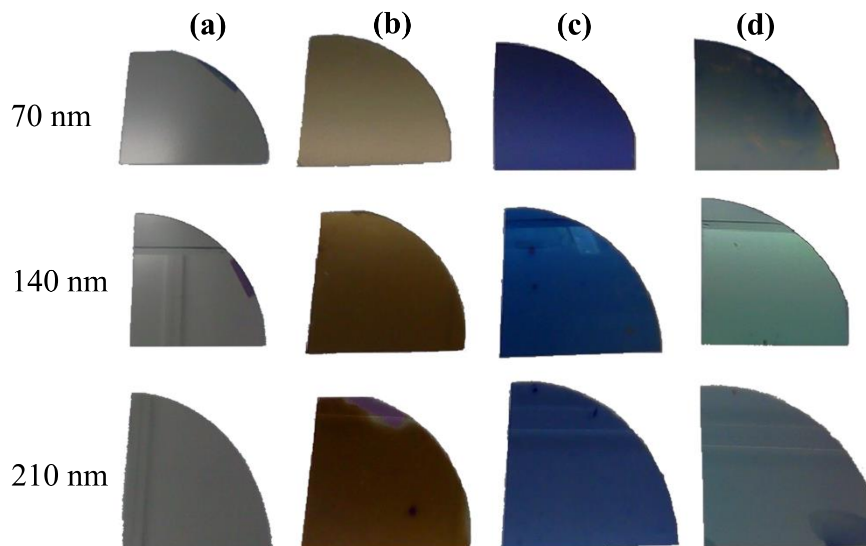

Figure 4.4.3: *Illustration of visual nitridation effect on tantalum nitride films. Loaded and unloaded at 200 °C: a) As-deposited TaN sample; b) Sample annealed at 450 °C for 30 min; c) Sample annealed at 500 °C for 30 min; d) Sample annealed at 600 °C for 300 min.*

The results of the resistance change from annealing at 450 and 500 °C are shown in Table 4.4.1. Relative change in resistance is shown because shards from the same wafer had a different measured sheet resistance due to its non-uniformity (2%) across the wafer. The non-reversible resistance change caused by a 30 minute process at 450 and 500 °C to a 70 nm TaN film suggested that the film produced by such a

process would not be suitable for a high-temperature electrical application; therefore, the planned experiments involving annealing in nitrogen were not continued.

Table 4.4.1 *Comparative measurement of tantalum nitride thin films affected by annealing in nitrogen for 30 min. Relative change of sheet resistance value is shown.*

Sample thickness (nm)	*Annealing temperature*	
	450 °C	*500 °C*
~70	+37%	+165%
~140	+14%	+6%
~210	-10%	-5%

The crystal structure of the annealed samples was evaluated using GIXRD (Fig. 4.4.4). The following peaks of the Ta_2N phase were detected in a range of 2θ = 20° to 65°: (100), (101), (102), (110) highly crystalline orientations (accordingly 33.968°, 38.73°, 50.764°, 60.968° in PDF#26-0985 [18]) with the highest diffraction intensity of (101) orientation of hexagonal tantalum nitride phase. Tetragonal Ta_2O_5 phase of (00(12)) orientation (29.554°, PDF#21-1199 [18]) was also found, which is likely to be located at the surface of the thin film because the diffraction intensity from it is relatively high. As suggested by the diffraction pattern, one of the possible explanations for the difference observed in samples annealed at 450 and 500 °C (Fig. 4.4.4) is that the originally polycrystalline TaN thin film, covered by a Ta_2O_5 layer, is damaged by nitrogen diffusion through the surface layer as indicated by disappearance of the Ta_2O_5-related peak. When annealing temperature and time are increased to 600 °C and 5 hours, only the substrate-related peak is visible, which means that the TaN film becomes completely disorganized.

It has been shown by the thin film colour change, sheet resistance and XRD measurements that annealing TaN in a nitrogen environment cannot introduce nitrogen, which would later distribute within the film thickness, to deposited TaN thin films, but rather creates passivation/low electrical conductance layers at the surface of the film. This effect becomes more pronounced with increasing temperature, hence it cannot be used as a method of reliable nitrogen content control.

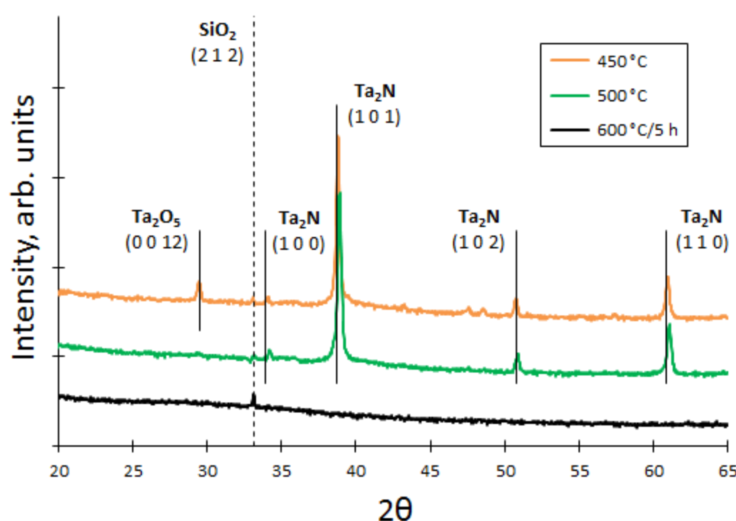

Figure 4.4.4: *XRD measurement of samples annealed in nitrogen ambient at 450 and 500 °C for 30 minutes, 600 °C for 5 hours.*

4.4.5 Phase content control and characterization

The purpose of the following set of experiments was not only investigate the stability of TaN sheet resistance, but also to evaluate the stability of the TCR, as this parameter is important to ensure the correct functionality of the temperature sensing circuit. The primary focus of these experiments was to find a relation between electrical and physical properties measured using XRD for both as-deposited and annealed film conditions. TaN thin film deposition was run on a tool where important parameters such as the configuration of sputtering target and deposition chamber, sputtering power and chamber pressure could not be changed without affecting other users. The only effective option was to change the relative nitrogen flow in 50 sccm total argon and nitrogen flow. The sputtering tool allowed the control of this ratio only with a precision of 2% (1 in 50 sccm), hence a lot depended on the composition of as-deposited films and not much could be changed by annealing. Results from initial depositions of tantalum nitride thin films, described in subsection 4.4.2, were comparable with results from the literature and indicated the production of films with composition close to one that produces a Ta_2N phase. Following the literature review, it was found that the targets for sheet resistance, TCR and stability properties are located within the range of Ta_2N to TaN [28, 35-37,

47, 48]. As this research is focussed on development of a temperature sensor that is planned to be produced by post-processing of SiC CMOS, the maximum annealing temperature was set to 600 °C due to the limited thermal budget of integrated circuits.

The three TaN samples with nominal thicknesses of 70, 140 and 210 nm produced using a 10% process were broken into four shards and each was annealed at temperatures of either 450, 500, 550 or 600 °C, iteratively, for 0.5, 1, 2, and 4 hours, with the last iteration resulting in an equivalent total annealing time of 7.5 hours. Load-in and load-out temperature in each case was 200 °C and the ramp rate was 5 °C·min^{-1}. Figure 4.4.5 shows that there is a significant change in the sheet resistance of the 210 nm-thick samples, and a greater change is produced by higher temperatures, whereas a much longer time is required to produce such a difference at 450 °C.

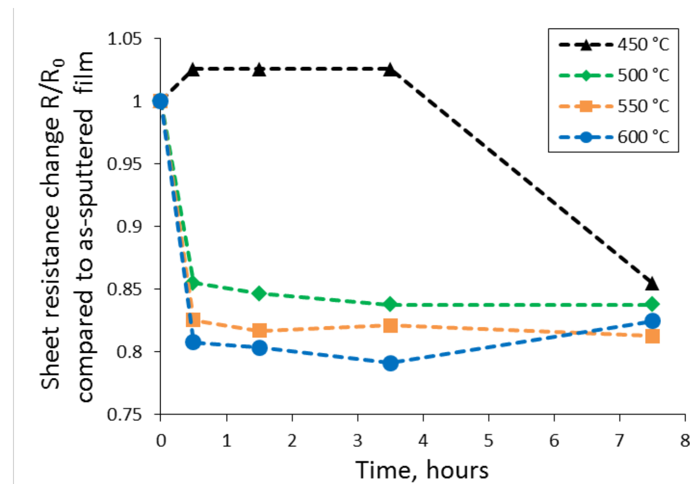

Figure 4.4.5: *Effect of vacuum annealing process temperature on 210 nm thick TaN samples produced using a 10% process.*

The crystal structure of samples with a nominal thickness of 210 nm, annealed for 7.5 hours has been measured using GIXRD (Fig. 4.4.6). Polycrystalline Ta_2N orientations of (100), (101), (102), (110) (accordingly 33.968°, 38.73°, 50.764°, 60.968° in PDF#26-0985 [18]) were found with (101) orientation being dominant in the diffraction data in a range of 2θ = 20° to 65°. A tetragonal Ta_2O_5 phase with orientation of (00(12)) is also present on the diffraction plot (29.554°, PDF#21-1199

[18]). Thinner film samples were measured electrically, but were not measured by XRD as they are expected to have lower crystallinity [49]. As suggested by the difference of diffraction patterns produced by samples annealed at 450 and 600 °C, the crystal orientation (101) in polycrystalline Ta_2N becomes more preferential whereas the diffraction from (110) decreases.

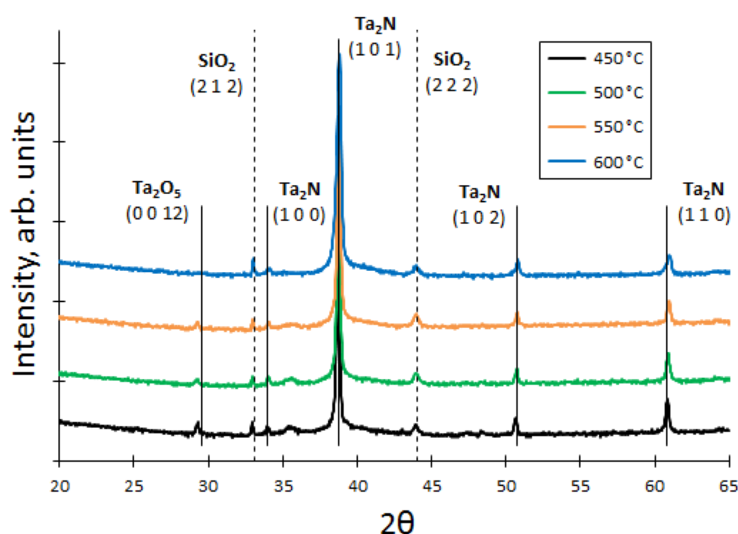

Figure 4.4.6: *XRD measurement results of samples annealed for total of 7.5 hours at temperatures of 450 to 600 °C.*

The resistance value change of Ta_2N sample measured by XRD and also thinner samples shown in Fig. 4.4.7 has indicated a change in trend at certain time value that is different for each annealing temperature. The reason for the transition in resistance trend from negative to positive was not confirmed by XRD plots in Fig 4.4.6, but can be explained by evolution of a different crystalline phase, similar to the β-Ta to α-Ta transition which is mentioned in many literature sources [30, 50-54]. This transition also suggests a low nitrogen content in the film, which results in a mixture of under-stoichiometric tantalum nitride and Ta_2N as opposed to single-phase polycrystalline Ta_2N [45, 51]. However, there was no direct evidence found through XRD measurements of thick samples (refer to Fig. 4.4.4 and 4.4.6).

An additional 24 hour, 600 °C annealing process was performed to check whether this hypothesis was correct – the results are shown in Fig. 4.4.7 and summarized in Table 4.4.2. A change in resistance trend took place within two hours for 70 nm samples and four hours for 140 and 210 nm samples, produced with a 10%

Ni process. Thinner samples are noticeably more affected by annealing as only the 210 nm sample provided reasonable stability with sheet resistance crossing the as-deposited value between 7.5 and 31.5 hours of annealing. The change from as-deposited state is around 8.98, 2.19 and 1.06 times for 70, 140 and 210 nm-thick samples annealed at 600 °C, five times for a total of 31.5 hours.

Table 4.4.2 *Comparative measurement of tantalum nitride film resistance before and after annealing at 600 °C in vacuum. Sheet resistance values are presented in Ω/□.*

Sample thickness, nm	*Annealing time, hours*					
	As-dep.	***0.5***	***1.5***	***3.5***	***7.5***	***31.5***
70	36.2	31.0	31.5	49.0	180	325
140	17.80	14.55	14.50	14.55	18.00	39.40
210	11.95	9.65	9.60	9.45	9.85	12.65

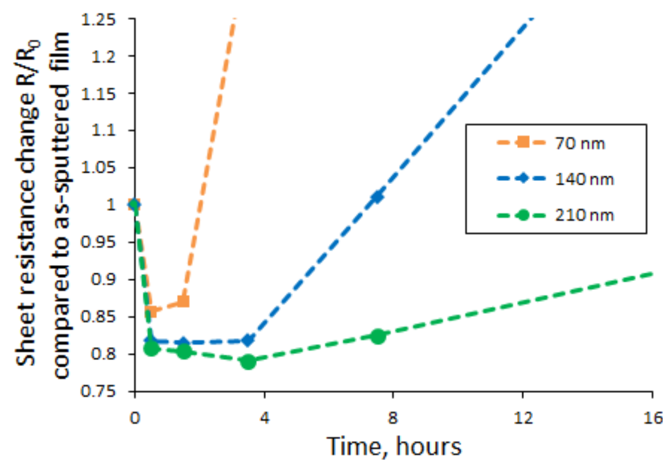

Figure 4.4.7: *Effect of vacuum annealing process performed at 600 °C on different thickness films produced using 10% process.*

Another set of experiments aimed at finding out electrical and physical properties of samples produced using different nitrogen flow ratio values was performed. All samples were prepared by 90 minute deposition runs in order to produce films thick enough to ensure long-term stability at elevated temperatures. The initial run involved film deposition using a 10% N_2 process and annealing in vacuum for either 5 or 8 hours. Wafers were patterned using the process described in subsection 4.4.3 and the TCR was measured using the 20 µm-wide cross-bridge test structures described in 4.3.2 and the test setup described in 4.3.3. Sheet resistances were

measured on blanket samples using a four point probe before and after annealing. The experiment continued with samples produced by 10%, 16% and 20% processes annealed for 6 and 7 hours. Samples fabricated using the 20% gas flow ratios produced a film with an average thickness of 190 nm as measured by Dektak 8 profilometer, hence the thickness of films in which test structures were fabricated was expected to be in the range of 190 to 210 nm. Finally, a 12% process was used to produce samples which were annealed for 5 and 6 hours. Sheet resistance and TCR of films produced using this process were measured using 20 µm-wide Greek Cross test structures (refer to subsection 4.3.2) and test setup described in subsection 5.5.1. TCR values of as-deposited and annealed (6 hours) samples produced by 10%, 16 and 20% processes were also confirmed by measurements performed using Greek Cross test structures.

Figure 4.4.8 shows how the sheet resistance of thin film tantalum nitride changed after different vacuum annealing processes run at 600 °C. There is a significant sheet resistance change between as-deposited and annealed samples; however, the value stabilizes after the first high-temperature treatment. Deposition processes that use 10% and 12% nitrogen flow ratios produce films with comparable stability of sheet resistance.

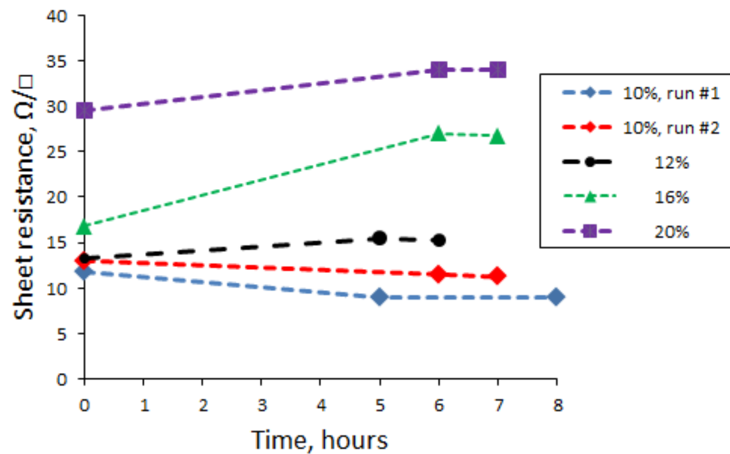

Figure 4.4.8: *Effect of vacuum annealing process performed at 600 °C on sheet resistance of thin films sputtered for 90 minutes in different nitrogen flow ratios.*

TCR (α) values were calculated using:

$$\alpha = \frac{\Delta R}{R\Delta T} = \frac{\Delta R}{\Delta T}\frac{1}{R} = \frac{m}{b}, \tag{4.11}$$

where m is the slope and b is the constant parameter of the linear equation calculated by linear regression fit to the resistance values measured in a temperature range of 25 to 125 °C:

$$R = mT + b \tag{4.12}$$

A summary of TCR measurement results is shown in Fig. 4.4.9. It can be seen from results measured on as-deposited samples produced by 10% and 12% processes that TCR is close to zero but becomes more negative with increasing ratio of nitrogen flow. Annealing causes the following changes in the TCR of these samples; with the 10% process TCR becomes more positive as it is annealed, crossing from a negative to a positive value after about 8 hours; meanwhile the TCR stays constant for the 12% process samples up to 6 hours of annealing; finally, those samples deposited with a 16% or 20% process show a TCR that becomes more negative with annealing.

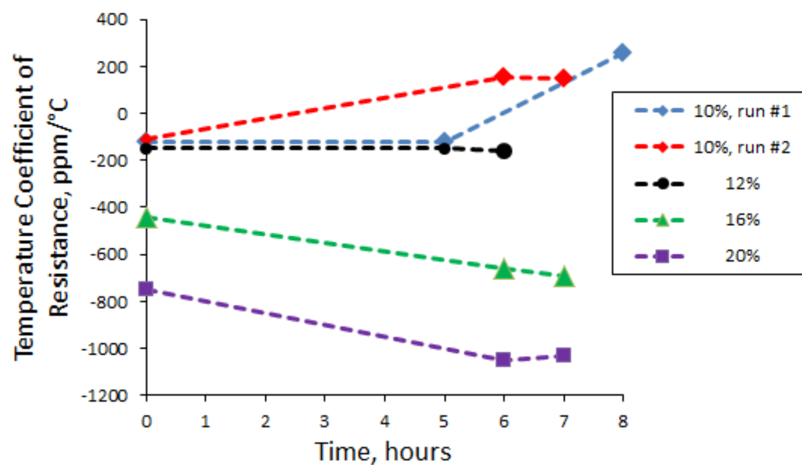

Figure 4.4.9: *Effect of vacuum annealing at 600 °C on TCR of films produced by 90 minute processes using different nitrogen flow ratios.*

As indicated in Figure 4.4.10, 90 minute reactive sputtering processes using 10% and 12% nitrogen flow ratio values offer comparable stability of thin film sheet resistance values. The TCR of a thin film produced by a 10% process is expected to cross zero within 8 hours of annealing, hence annealing for a shorter time will result

in a resistor that ages at operating temperatures in a way that brings the TCR closer to zero, until it becomes positive. The TCR of a TaN film deposited with a 12% process, on the other hand, is not expected to cross zero but has superior long term stability as the measured value stays around –150 ppm °C^{-1}. The trend in increase of TCR with increasing nitrogen content and annealing time shows that it would be unreasonable to choose any TaN film with higher nitrogen content than that produced by 12% process.

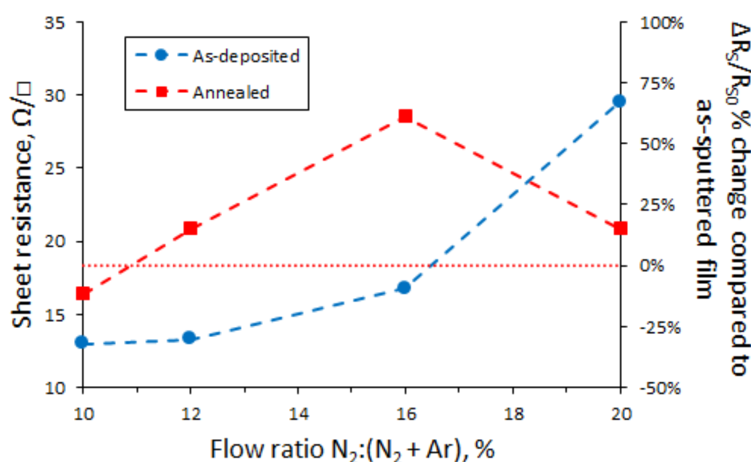

Figure 4.4.10: *Sheet resistance of as-deposited 190-210 nm samples and the change in resistance of these films after a 6 hour vacuum annealing process at 600 °C.*

A separate set of test wafers was produced to study phase transition in tantalum nitride films using XRD. A different tool (Siemens D5000) was used, which allowed comparison of measured data on similar thin film tantalum nitride samples (refer to Fig. 4.4.6 and 4.4.12). Four processes were used to produce films: 30 minute process without nitrogen addition and 90 minute processes using 10% and 12% flow ratios.

As shown in Fig. 4.4.11, the sputtered pure tantalum thin film (0%) consists of a single tetragonal Ta phase of (002) orientation as indicated by a sharp peak around 33.692° (PDF#25-1280 [18]). Another peak is related to native tantalum oxide Ta_2O_5 (29.554°, PDF#21-1199 [18]). In the case of the 10% process weak peaks measured from an as-deposited sample are related to under-stoichiometric $TaN_{0.1}$ (54.44°, PDF#25-1278 [18]), a (300) orientation of TaON (56.326°, PDF#20-1235 [18]) and, very likely, (002) orientation of Ta_2O_5 (47.647°, PDF#21-1199 [18]). No well-defined peaks were observed in results from sample produced with 12% process.

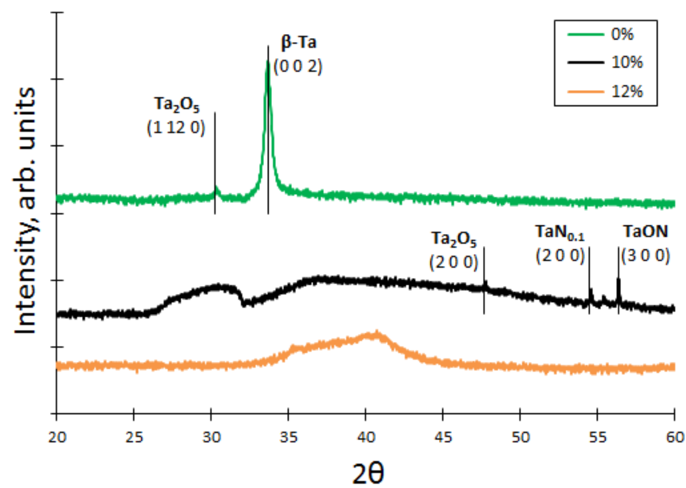

Figure 4.4.11: *XRD measurement results of as-deposited samples produced by different nitrogen flow ratio processes: 0% for 30 min., 10% and 12% for 90 min.*

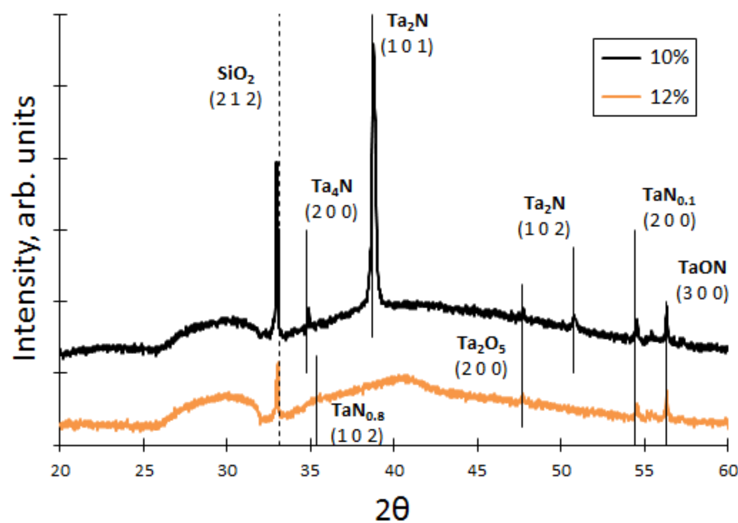

Figure 4.4.12: *XRD measurement results of samples annealed at 600° C for 6 hours produced by different processes: 10% and 12% nitrogen flow ratio for 90 min.*

Annealing of thin films is known to increase the crystallinity, therefore additional peaks appear on diffraction plots (Fig. 4.4.12). XRD patterns of annealed and measured samples produced by the 10% process show the appearance of (200) Ta_4N (34.728°, PDF#32-1282 [18]), (101) and (102) Ta_2N peaks (accordingly 38.73° and 50.764° in PDF#26-0985 [18]) in range of 2θ = 20° to 65°. The majority of detected phases in this sample are of higher stoichiometry, therefore it is likely that $TaN_{0.1}$ only exists in nitrogen-deficient layers. The annealed sample produced with the 12% process consists of a variably-oriented film with a weak indication of $TaN_{0.8}$ phase,

which was not directly observable due to the width of the increased diffraction intensity area. All these findings are related to phase development with increasing nitrogen content, which are quite similar to an example from the literature, where films were reactively sputtered at 300 °C, as summarized in Table 4.4.3 [55].

Table 4.4.3 *Comparative measurement of tantalum nitride phase content before and after annealing in vacuum and comparison with result from the literature source.*

Process: deposition time; N_2:(N_2+Ar)	*Phases obtained at film condition*		
	This work: as-deposited at RT	*This work: vacuum-annealed at 600 °C*	*Ref. [55]: as-deposited at 300 °C*
90 min; 10%	$TaN_{0.1}$, TaON, Ta_2O_5	Ta_2N, Ta_4N, TaON, $TaN_{0.1}$, Ta_2O_5	-
90 min; 12%	a-TaN	$TaN_{0.8}$, $TaN_{0.1}$, TaON, Ta_2O_5	-
30 min; 4%	-	-	Ta_2N, $TaN_{0.1}$
30 min; 10%	-	-	TaN, $TaN_{0.8}$, Ta_4N
30 min; 20%	-	-	TaN, $TaN_{0.8}$, $Ta_6N_{2.57}$
30 min; 30%	-	-	TaN, $TaN_{0.8}$

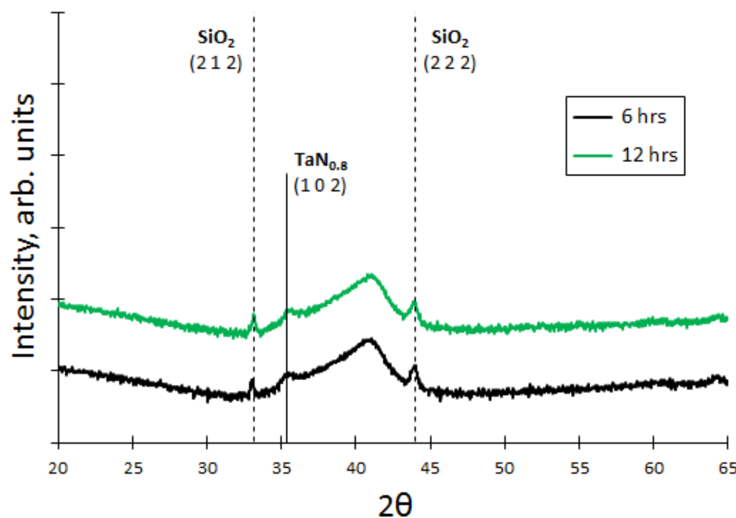

Figure 4.4.13: *XRD measurement of samples produced by 12% process annealed at 600 °C for total of 6 and 12 hours.*

A final test sample deposition was performed using 12% nitrogen flow ratio process for 90 minutes. The purpose of this run was to confirm whether a thin film produced by this process was indeed mostly amorphous after annealing. After the samples were deposited, one sample underwent the vacuum annealing process at 600 °C for 6 hours while another sample was annealed twice using this same process, i.e, for a total of 12 hours. The results of XRD measurement performed on these samples are shown in Fig. 4.4.13. The measured diffraction patterns are very similar for both annealing times, and the $TaN_{0.8}$ peak is more pronounced in both as compared to Fig. 4.4.12(b). This indicates that the annealing temperature is too low for complete recrystallization to take place, which partially explains why the TCR of films produced by this process (refer to Fig. 4.4.9) is unaffected by annealing.

4.4.6 Summary of results

A range of developed tantalum nitride deposition and annealing processes can be used to produce resistors with TCR close to zero. TCR control is performed through nitrogen flow ratio setting of reactive sputtering process performed at room temperature and annealing at different temperatures in vacuum. Deposition processes that used 10% and 12% nitrogen ratios produced a thin film with very low negative TCR, which was stabilised after vacuum annealing at 600 °C. The 12% nitrogen process offered a very stable TaN thin film with a TCR near –150 ppm $°C^{-1}$ when film was 200 nm thick. Variations of process in the range between 10% and 12% nitrogen flow ratio will allow tuning the TaN film TCR in the region between –150 and 200 ppm $°C^{-1}$. A thin film of approximately 210 nm thickness was dry etched controllably in plasma of $CF_4 + O_2$ to produce patterned structures.

4.5 Development of platinum process

Platinum is an industrially-recognized material due to its remarkable physical and chemical properties. Platinum-based elements are widely used in temperature sensing applications due to their high and linear value of TCR [56]. The thin film platinum

process available for this research used an e-beam evaporation deposition method without significant control of deposition parameters. This section will therefore focus on development of processes preceding and following the deposition of thin film platinum concerning such elements as adhesion layer selection, TCR stabilization and feature patterning.

4.5.1 Introduction

Physical vapour deposition of thin film platinum offers process simplicity while e-beam evaporation allows the deposition of platinum films with high purity [57]. However, there are problems related to this deposition method when it is required to produce elements which have to perform sustained operations at elevated temperatures. Evaporated platinum requires an adhesion layer when deposited on silicon substrates covered by a thermal oxide or deposited silicon nitride layer [58, 59]. The adhesion layer has to be carefully selected in order to ensure structural stability of platinum thin films in processing conditions and designed operational environment.

There is a clear difference between bulk and thin film platinum electrical characteristics [60, 61]. Most important for this research is the TCR value, which defines the temperature sensitivity. There is also an additional effect coming from a conductive adhesion layer which has its own resistivity and temperature dependence and this section will concern the trade-offs made to produce thin films with reasonable specifications.

4.5.2 Thickness-related issues

The temperature coefficient of resistance for bulk platinum quoted in the literature is close to 3850 ppm $°C^{-1}$. The electrical performance of thin films is typically inferior in many ways to the performance of elements produced using platinum with bulk properties and this fact results in implications for temperature sensing applications [60]. It has been shown that the TCR depends heavily on the deposited thin film thickness and there is a minimum value of thickness that is directly proportional to maximum exposure temperature in order to ensure that the

TCR stays linear and constant across the entire temperature range [60-63]. For example, platinum thickness of 800 nm can be expected to produce resistance temperature detector with TCR of 3850 ppm °C^{-1} [64].

For example, Lacy has provided an equation based on mathematical analysis and empirical values which describes the temperature (T_{max}) at which the TCR of thin film platinum with thickness t, changes suddenly to become much lower than expected [60, 63]:

$$T_{\max} = T_C + 0.009e^{0.1t}, \text{ (°C)} \tag{4.13}$$

T_C is a constant critical temperature which depends on the deposition process used, which was found to be 84 °C for the DC sputtering deposition process by Lacy [60, 63]. Rewriting Eq. 4.13, the minimum thickness required to ensure the linearity of TCR in the temperature range ΔT, where T_{max} = 300 °C and T_C = 84 °C:

$$t_{\min} = 10\ln\left(\frac{\Delta T}{0.009}\right) = 10\ln\left(\frac{216}{0.009}\right) \approx 100.9\ nm, \tag{4.14}$$

which means that samples thinner than 100 nm are likely to show a clear decrease in TCR at temperatures above 300 °C. Therefore, the minimum platinum thin film thickness considered as reasonable to be used for high-temperature applications is 100 nm. Using much thicker films, on the other hand, will unavoidably create deposition- and patterning-related problems. TCR of platinum thin film is inevitably lower than that of bulk platinum and vacuum annealing of thin film platinum at reasonable temperature is known, on one hand, to increase its TCR, but, on the other hand, also to adversely affect its structural stability [58, 65, 66]. Thicker films will have improved structural integrity after a high-temperature annealing process and can result in significant TCR increase [60, 62, 67].

From the perspective of the sensor element design, the sheet resistance of thin film platinum should be high enough for elements produced using this material to be laid out conveniently. The sought after sheet resistance value was 2 Ω/□ or higher and so a 100 nm thickness of Pt was selected as a trade-off between different design parameters, including the expected stability and an expected TCR value after vacuum annealing. A vacuum annealing process, which should be highly compatible with

TaN thin films, of 500 °C for 12 hours was selected after further examination of the literature [58, 66, 68].

TCR depends not only on the electrical conductivity-related mechanism, but also on any mechanical stress that is applied to the thin film [7]. Stress will change with temperature due to differences in thermal expansion between a thin film and the underlying substrate. Using XRD may be an effective measure to determine the effect of stress on films of different thicknesses and add to the explanation why TCR improves as a result of high-temperature treatment.

Ti and TaN adhesion layers were selected for comparisons of the TCR value and structural integrity of 100 nm-thick Pt films deposited on top. Thermally oxidised (500 nm) silicon wafers were used as a substrate. The sheet resistance value of an as-deposited 100 nm Pt/10 nm Ti sample measured using the four-point probe was 4.75±0.11 Ω/□ while TCR was 742.8 ppm $°C^{-1}$. The sheet resistance decreased to 4.07±0.05 Ω/□ after the sample was vacuum annealed at 500 °C for 12 hours. The sheet resistance of as-deposited 100 nm Pt/10 nm (10% flow ratio process) TaN was 7.74±0.31 Ω/□ and the sheet resistance increased significantly to 11.82±0.31 Ω/□ after annealing and TCR became 1342 ppm $°C^{-1}$.

Measuring the platinum thin film TCR using cross-bridge test structures and the setup described in subsection 4.3.3 turned out to be difficult because probes were damaging the film significantly. The annealed platinum sample that was deposited on top of the Ti adhesion layer was peeling off readily; hence it was decided to not continue the use of Ti adhesion layers for the rest of this research and TaN adhesion layers were used in later fabrication.

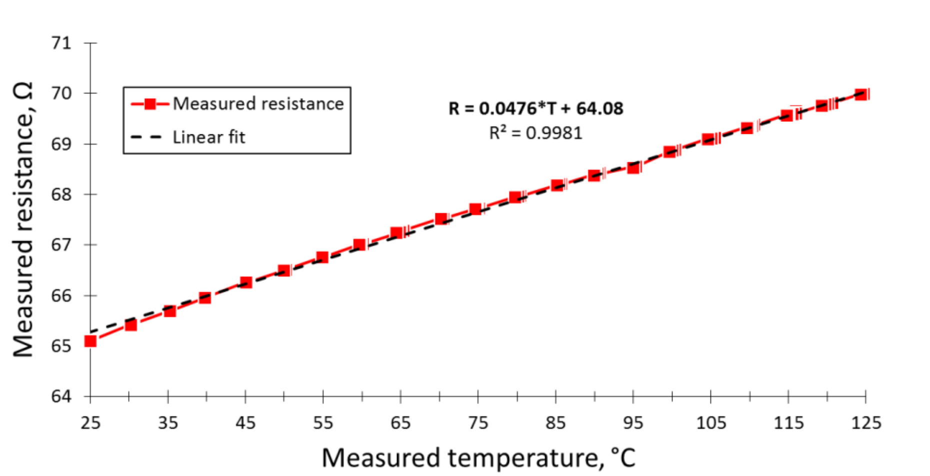

Figure 4.5.1: *TCR measurement of as-deposited 100 nm Pt film: Ti adhesion layer.*

From (4.9):

$$\alpha = \frac{\Delta R}{R\Delta T} = \frac{0.0476}{64.08} \approx 742.8 \text{ ppm °C}^{-1} \tag{4.14}$$

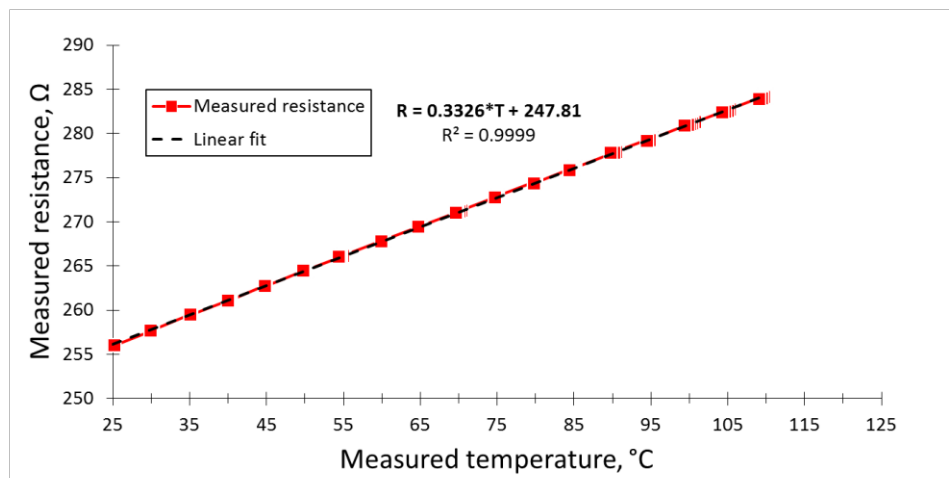

Figure 4.5.2: *TCR measurement of annealed 100 nm Pt film: TaN adhesion layer.*

From (4.9):

$$\alpha = \frac{\Delta R}{R\Delta T} = \frac{0.3326}{247.81} \approx 1342.2 \text{ ppm °C}^{-1} \tag{4.15}$$

TCR values measured were much lower than expected for both as-deposited and annealed samples, regardless of the adhesion layer used, which was a possible indication of the following:

- The TCR of evaporated thin film platinum is inferior to that of a sputtered film;

- Thin film platinum is under the effect of very high stress on Si/SiO_2 substrate;
- Platinum film crystallinity produced by such a process is poor and variable;
- The thin film platinum thickness varies significantly with each deposition run as indicated by variation of sheet resistance;
- The thin film contains a significant amount of impurities rather than pure Pt.

4.5.3 Adhesion layer for thin film platinum

Adhesion between evaporated platinum and oxidised silicon wafer substrate is poor without an adhesion layer [66, 69, 70]. Two refractory metals, titanium and tantalum, act well as adhesion materials for platinum, but these two materials in a pure form, however, have a tendency to form an oxidised protective surface layer when exposed to an atmospheric environment [66, 71]. As shown in multiple literature sources, titanium is not suitable for high-temperature applications on any conventional substrates [58, 66, 70, 72]. Tantalum is a better option at temperatures up to 650 °C as demonstrated by Tiggelaar et al. [58]. In order to increase the lifetime of the platinum elements deposited on the adhesion layer and to also make sure that platinum process would be highly compatible with TaN process developed earlier, an approach that uses TaN adhesion layer of same composition as TaN balancing resistors was selected. An electrically conductive adhesion layer was preferred in order to decrease the value of parasitic resistance in the device when further integrating platinum and tantalum nitride thin film processes.

As suggested by XRD results from section 4.4, in particular Fig. 4.4.11, there is chance that an oxidised surface layer develops on tantalum even before the sample has been exposed to a high-temperature treatment. This was one of the reasons Ta was ruled out as an adhesion layer despite high structural stability at high temperatures [58, 66]. Such a problem in fact exists even with a TaN adhesion layer produced by the 10% process if it is left open to the air for longer than two days. While this problem does not manifest itself during/after deposition or during etching of film, platinum comes off the adhesion layer during lift-off process performed at 50 °C in an ultrasonic bath. The only effective solution to solve this problem is to load wafers into the e-beam evaporator immediately after the adhesion layer has been

deposited. Another concern was the crystallinity of the extremely thin Ta adhesion layer. Trying to measure a very thin sputtered Ta film on a thick silicon substrate would be impractical and also the whole film may oxidise during the high-temperature annealing process, hence a 90 minute Ta deposition was run directly on oxidised wafers and wafers covered by TaN adhesion layer.

Figure 4.5.3 shows the result of XRD measurements performed on samples produced by these processes. There is a sharp (002) peak (33.692°, PDF#25-1280 [18]) of tetragonal β-Ta detected on the as-deposited sample. The measurements performed on the same film sample that was annealed for 6 hours at 600 °C shows that the height to width ratio of (002) Ta peak decreased significantly while another (311) Ta peak (32.387°, PDF#25-1280 [18]) appeared. This measurement also revealed an appearance of a pronounced (00(12)) peak of tetragonal tantalum pentoxide Ta_2O_5 (29.554°, PDF#21-1199 [18]) produced by the surface oxide.

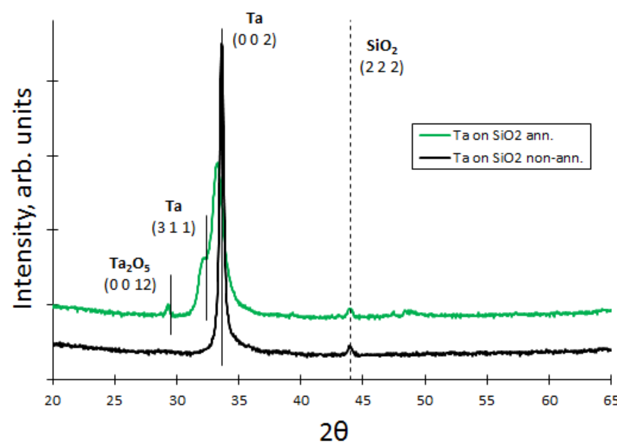

Figure 4.5.3: *XRD sample measurements: annealed and as-deposited Ta on thermal* SiO_2*.*

Figure 4.5.4 depicts XRD measurement results of a tantalum thin film deposited onto a TaN adhesion layer, which was produced by 5 minute reactive sputtering deposition with a 12% nitrogen flow ratio. Measurements of the as-deposited sample showed that there is the same (002) Ta phase present in the film, but this time at lower scale. Annealed Ta with TaN adhesion layer sample reveals that the phase changes taking place during annealing are similar to ones that are mentioned in the description of Fig. 4.5.1. In addition to that, a much stronger (202) Ta (38.200°,

PDF#25-1280 [18]) diffraction peak has appeared on the intensity plot of the measured as-deposited sample, which became less sharp after the sample has been annealed.

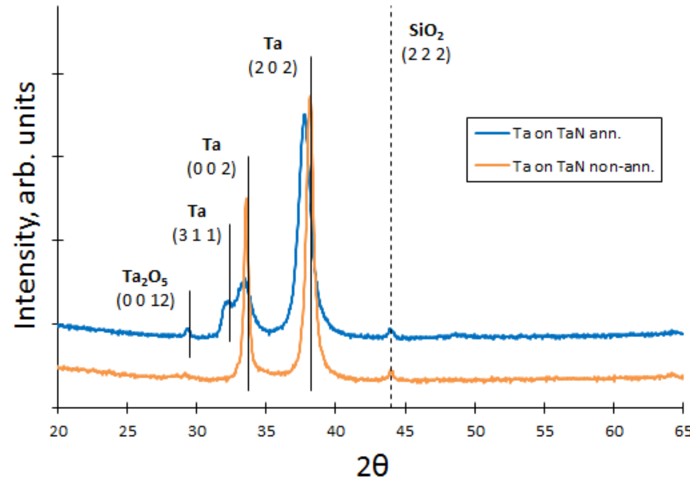

Figure 4.5.4: *XRD sample measurements: annealed and as-deposited Ta on TaN adhesion layer.*

There is a visible difference that has been introduced by TaN adhesion layer in terms of Ta phase stability, whereas tantalum without an adhesion layer has undergone significant phase changes (refer to Fig. 4.4.6 and 4.4.13 for comparison with TaN). Both measurements of annealed samples contained an offset of measured peak to lower values as compared to both PDF#25-1280 and as-deposited values, which is characteristic to films that are under higher compressive stress produced by incorporation of oxygen into the film [18]. This is also in agreement with the previous process development that has taken place at the SMC [73, 74]. Sheet resistance measurements were not performed in this case since tantalum is known to oxidise at elevated temperatures, and this changes the measured sheet resistance value and hence upsets conditions for a fair comparison.

As a result of criteria matching and elimination of materials that may become unstable during annealing, two metal adhesion layers were finally considered and compared:

- High nitrogen content *titanium nitride* produced by sputtering with a 44% nitrogen flow ratio;

- Low nitrogen content *tantalum nitride* produced by 10% or 12% processes developed in section 4.4.

A test deposition of platinum thin films has been performed to study the effect of different adhesion layers on the platinum properties. The titanium nitride was produced using 44% nitrogen flow ratio reactive sputtering for 15 minutes. The tantalum nitride adhesion layer was deposited using 12% nitrogen flow ratio reactive sputtering for 6 minutes in an attempt to produce the same film thickness as TiN (~10 – 15 nm). A blanket layer of 100 nm thick Pt was deposited in the same deposition process. The average, as-deposited, sheet resistance was 3.46 Ω/□ for Pt deposited on TiN and 3.35 Ω/□ for a TaN adhesion layer. Wafers were cleaved into halves before one half with each adhesion layer was annealed for 6 hours at 600 °C. Annealed samples had sheet resistances of 3.29 Ω/□ for TiN and 3.14 Ω/□ for TaN.

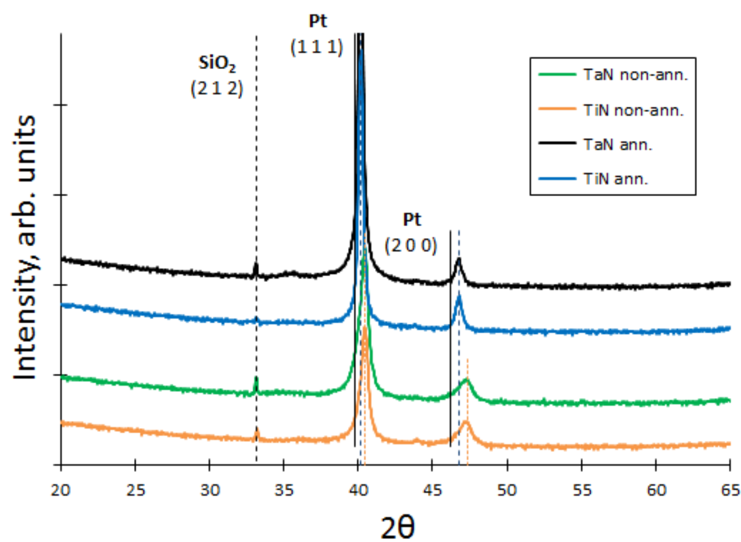

Figure 4.5.5: *XRD sample measurement: annealed and as-deposited Pt on TaN adhesion layer; annealed and as-deposited Pt on TiN adhesion layer.*

Figure 4.5.5 shows XRD measurement results of samples produced by these processes. Results of as-deposited and annealed samples are grouped for the convenience of presentation. As it can be seen from diffraction data, there is no particular benefit that the TiN adhesion layer offers (and otherwise) from the perspective of structural composition because both intensity plot groups look very similar for both annealed and as-deposited samples. As-deposited samples have

preferential platinum crystal orientation of (111) and (200) (accordingly 39.763° and 46.243°, PDF#04-0802 [18]), where the signal of the (111) is dominating in the intensity plot. The film is under significant tensile stress, which is indicated by the shift towards higher 2θ values as compared to the reference value. Annealing notably increases the crystallinity of the film as indicated by the significantly increased height-to-width ratio of the peaks and decreases the level of stress. Using the titanium nitride adhesion layer would decrease the effect of adhesion layer on the electrical resistance and hence contribute to an improved temperature coefficient of resistance, however it would not be practical to use it when trying to electrically connect elements using the developed tantalum nitride and platinum processes.

4.5.4 Summary of results

Evaporated thin film platinum is polycrystalline as deposited. Vacuum-annealing at 500 °C improved the preferential orientation and decreased the amount of tensile stress in the film, which resulted in improved TCR and sheet resistance values. TCR values in the range of 1000 ppm $°C^{-1}$ measured following the annealing process for as-designed 100 nm-thick film were lower than expected, which was an indication of process variability and potential contamination in the deposition chamber. The tantalum nitride process developed in section 4.4 was reused to produce a 10-15 nm adhesion layer for thin film platinum, which improved in sheet resistance value and remained stable following the vacuum-annealing process at 600 °C.

4.6 Conclusions

The scope of thin film development was narrowed due to constraints set by target specifications, availability of deposition tools and deposition parameter control. Described development of thin films has provided a significant groundwork for further development of a fabrication process that would enable the production of an integrated sensor. Thin films produced by deposition, patterning and annealing processes described here had reasonable stability of sheet resistance and temperature

coefficient of resistance. Therefore, it is highly likely that using the developed thin film processes can be used to produce a temperature sensor that would withstand high temperatures and it is only a matter of determining how these processes will be integrated to achieve the necessary result. As a general observation, it was possible to produce thin film tantalum nitride with the necessary TCR value that is close to zero while it was more problematic to fabricate platinum thin film resistors of comparable thickness and reasonable sheet resistance value with TCR close to that of a bulk material.

Two tantalum nitride deposition processes that offer TCR values close to zero have been developed. Process using 10% nitrogen flow ratio produced a thin film with very low negative TCR value that slowly changes to a low, positive value during vacuum annealing at 600 °C. The drawback of thin films produced by this process is that there is a demonstrable variation of sheet resistance that occurs in the same region. The primary reason for that is crystal structure change among a combination of stable Ta_2N and under-stoichiometric phases as showed in the XRD plots. This fact also suggests that the 10% process produces films with lower nitrogen content than is necessary to produce stable sheet resistance and TCR values. The 12% nitrogen process offered a very stable thin film with a constant TCR of approximately –150 ppm $°C^{-1}$. The most evident reason for such stability is the fact that the range of the temperatures and annealing times used were insufficient to create a change in the phase composition of the as-deposited, variably-oriented thin film. The nitrogen content in TaN can be changed by annealing in a nitrogen environment, however this causes passivation of the surface and does not lead to redistribution of nitrogen within the whole volume of thin film. Therefore, it is not a reliable method to control tantalum nitride film properties. Films produced using 14% and higher flow ratio processes would not have the sought after TCR values.

Thin film platinum produced by evaporation is polycrystalline with the (111) orientation being dominant in the film. Crystallinity of the film was improved after vacuum-annealing at 500 °C for 12 hours for any adhesion layer that is suitable for high-temperature operation. With the available deposition process, the TCR value could only be improved by increasing the thickness of the thin film, which would

have resulted in increased stress in the material. Annealing platinum thin films improved the TCR, however the values were lower than expected, probably due to the quality of platinum produced by the e-beam evaporator. Annealing also decreases the amount of stress in the film and therefore can be considered as the best way of stabilizing the values of sheet resistance and TCR. A tantalum nitride adhesion layer was chosen after thorough consideration and comparison to titanium, tantalum and titanium nitride. This gives the best trade-off between the TCR value of platinum deposited on the adhesion layer and the ability to make low resistance contact through the adhesion layer.

The relationships between electrical and physical properties were investigated for both tantalum nitride and platinum thin films. The GIXRD technique was extremely sensitive to any changes of crystal orientation in tantalum nitride thin films and, for example, helped in discovering that the reactively sputtered film contains some oxygen in a compound of tantalum and nitrogen. It has also been shown in this chapter that performing reference measurement of substrates is useful since the ambiguous peaks can be eliminated from analysis of peaks produced by thin films.

References

[1] I. Ayerdi, E. Castaño, A. García-Alonso, and F. J. Gracia, "Characterization of tantalum oxynitride thin films as high-temperature strain gauges," *Sensors and Actuators A: Physical,* vol. 46, no. 1-3, pp. 218-221, 1995.

[2] S. Tsukimoto, M. Moriyama, and M. Murakami, "Microstructure of amorphous tantalum nitride thin films," *Thin Solid Films,* vol. 460, no. 1-2, pp. 222-226, 2004.

[3] C.-C. Chang, J. S. Jeng, and J. S. Chen, "Microstructural and electrical characteristics of reactively sputtered Ta-N thin films," *Thin Solid Films,* vol. 413, no. 1-2, pp. 46-51, 2002.

[4] J. Zhang, Y. Nagao, S. Kuwano, and Y. Ito, "Microstructure and Temperature Coefficient of Resistance of Platinum Films," *Japanese Journal of Applied Physics,* vol. 36, no. Part 1, No. 2, pp. 834-839, 1997.

[5] A. Benediktovich, I. Feranchuk, and A. Ulyanenkov, "The Theory of X-Ray Scattering from Macroscopical Objects," in *Theoretical Concepts of X-Ray Nanoscale Analysis: Theory and Applications*, Berlin & Heidelberg, Germany: Springer-Verlag, 2014, pp. 53-70.

[6] "Guideline for the evaluation of European practices on the harsh environment qualification of electrical and IC equipment," European Commission, Luxembourg City, LuxembourgEUR 17563 EN, 1998.

[7] F. Zandman, P. R. Simon, and J. Szwarc, "Irreversible Phenomena Associated with Ohm's Law," in *Resistor Theory and Technology*, Malvern, USA: Vishay Intertechnology, 2002, pp. 33-50.

[8] A. O. Ibidunni, "The oxidation and resistance of tantalum-nitride thin films," *Oxidation of Metals,* vol. 40, no. 1-2, pp. 5-20, 1993.

[9] R. Haugsrud, "On the high-temperature oxidation of nickel," *Corrosion Science,* vol. 45, no. 1, pp. 211-235, 2003.

[10] D. J. Young, "Experimental Findings," in *High Temperature Oxidation and Corrosion of Metals*, (Elsevier Corrosion Series, no. 1), Oxford, UK: Elsevier, 2008, pp. 82-137.

[11] D. A. Porter and K. E. Easterling, "Crystal Interfaces and Microstructure," in *Phase Transformations in Metals and Alloys*, 2nd ed., London, UK: Chapman & Hall, 1996, pp. 62-184.

[12] A. Guinier, "Diffaction of X-Rays by Crystals," in *X-Ray diffraction in Crystals, Imperfect Crystals, and Amorphous Bodies*, San Francisco, USA: W. H. Freeman and Company, 1963, pp. 83-120.

[13] B. Fultz and J. M. Howe, "Diffraction and the X-Ray Powder Diffractometer," in *Transmission Electron Microscopy and Diffractometry of Materials*, Berlin-Heidelberg, Germany: Springer, 2008, pp. 1-59.

[14] T. Mitsunaga, "X-ray thin film measurement techniques II: Out-of-plane diffraction measurements," *The Rigaku Journal,* vol. 25, no. 1, pp. 7-12, 2009.

[15] A. Fischer, M. Schmitz, B. Aichmayer, P. Fratzl, and D. Faivre, "Structural purity of magnetite nanoparticles in magnetotactic bacteria," *Journal of the Royal Society Interface,* vol. 8, no. 60, pp. 1011-8, 2006 2011.

[16] K. Inaba, S. Kobayashi, K. Uehara, A. Okada, S. L. Reddy, and T. Endo, "High Resolution X-Ray Diffraction Analyses of (La,Sr)MnO_3/ZnO/Sapphire(0001) Double Heteroepitaxial Films," *Advances in Materials Physics and Chemistry,* vol. 03, no. 01, pp. 72-89, 2013.

[17] S. Kobayashi, "X-ray thin-film measurement techniques IV. In-plane XRD measurements," *The Rigaku Journal,* vol. 26, no. 1, pp. 3-11, 2010.

[18] Powder Diffraction Files by *International Centre for Diffraction Data*.

[19] A. Munkholm and S. Brennan, "Ordering in Thermally Oxidized Silicon," *Physical Review Letters,* vol. 93, no. 3, 2004.

[20] K. Nagata *et al.*, "Structural Analyses of Thin SiO2 Films Formed by Thermal Oxidation of Atomically Flat Si Surface by Using Synchrotron Radiation X-Ray Characterization," *ECS Journal of Solid State Science and Technology,* vol. 4, no. 8, pp. N96-N98, 2015.

[21] P. Song *et al.*, "PECVD Grown SiO2 Film Process Optimization," *2011 Symposium on Photonics and Optoelectronics,* pp. 1-4, 2011.

[22] D. K. Schroder, "Contact Resistance and Schottky Barriers," in *Semiconductor Material and Device Characterization*, 3rd ed., Hoboken, USA: Wiley-IEEE Press, 2006, pp. 127-184.

[23] L. J. Van der Pauw, "A method of measuring specific resistivity and Hall effect of discs of arbitrary shape," *Philips Research Reports,* vol. 13, pp. 1-9, 1958.

[24] J. M. David and M. G. Buehler, "A numerical analysis of various cross sheet resistor test structures," *Solid-State Electronics,* vol. 20, no. 6, pp. 539-543, 1977.

[25] Design Considerations for the Cross-Bridge Sheet Resistor by *National Bureau of Standards*, 82-2548, 1982.

[26] Y. M. Lu, R. J. Weng, W. S. Hwang, and Y. S. Yang, "Study of phase transition and electrical resistivity of tantalum nitride films prepared by DC magnetron sputtering with OES detection system," *Thin Solid Films,* vol. 398-399, pp. 356-360, 2001.

[27] S. K. Kim and B. C. Cha, "Deposition of tantalum nitride thin films by D.C. magnetron sputtering," *Thin Solid Films,* vol. 475, no. 1-2, pp. 202-207, 2005.

[28] N. D. Cuong, D.-J. Kim, B.-D. Kang, C. S. Kim, K.-M. Yu, and S.-G. Yoon, "Characterization of Tantalum Nitride Thin Films Deposited on SiO_2/Si Substrates Using dc Magnetron Sputtering for Thin Film Resistors," *Journal of The Electrochemical Society,* vol. 153, no. 2, pp. G164-G167, 2006.

[29] T. Elangovan *et al.*, "Synthesis and high temperature XRD studies of tantalum nitride thin films prepared by reactive pulsed dc magnetron sputtering," *Journal of Alloys and Compounds,* vol. 509, no. 22, pp. 6400-6407, 2011.

[30] L. A. Clevenger, A. Mutscheller, J. M. E. Harper, C. Cabral, and K. Barmak, "The relationship between deposition conditions, the beta to alpha phase transformation, and stress relaxation in tantalum thin films," *Journal of Applied Physics,* vol. 72, no. 10, p. 4918, 1992.

[31] F. Zandman, P. R. Simon, and J. Szwarc, "Resistive Materials," in *Resistor Theory and Technology*, Malvern, USA: Vishay Intertechnology, 2002, pp. 51-74.

[32] J. J. Licari and L. R. Enlow, "Thin Film Processes," in *Hybrid Microcircuit Technology Handbook: Materials, Processes, Design, Testing and Production*, 2nd ed., Westwood, USA: Noyes Publications, 1998, pp. 63-103.

[33] K. Frisk, "Analysis of the phase diagram and thermochemistry in the Ta–N and the Ta–C–N systems," *Journal of Alloys and Compounds,* vol. 278, no. 1-2, pp. 216-226, 1998.

[34] M. Grosser, M. Münch, H. Seidel, C. Bienert, A. Roosen, and U. Schmid, "The impact of substrate properties and thermal annealing on tantalum nitride thin films," *Applied Surface Science,* vol. 258, no. 7, pp. 2894-2900, 2012.

[35] S.-M. Na, I.-S. Park, S.-Y. Park, G.-H. Jeong, and S.-J. Suh, "Electrical and structural properties of Ta–N thin film and Ta/Ta–N multilayer for embedded resistor," *Thin Solid Films,* vol. 516, no. 16, pp. 5465-5469, 2008.

[36] H. Jiang, C. Wang, W. Zhang, X. Si, and Y. Li, "Influences of Film Thickness on the Electrical Properties of TaN_x Thin Films Deposited by Reactive DC Magnetron Sputtering," *Journal of Materials Science & Technology,* vol. 26, no. 7, pp. 597-600, 2010.

[37] T. Akashi, S. Higashiyama, H. Takemori, and T. Koizmi, "A silicon optical bench incorporating a tantalum-nitride thin-film resistor," *Journal of Micromechanics and Microengineering,* vol. 14, no. 2, pp. 283-289, 2004.

[38] "Lift-off Processes with Photoresists," ed. http://www.microchemicals.com/technical_information/lift_off_photoresist.pdf : MicroChemicals, 2013.

[39] S. Franssila, "Etching," in *Introduction to Microfabrication*, Chichester, UK: John Wiley & Sons 2004, pp. 119-132.

[40] J. Jessing, "CMOS Fabrication," in *The VLSI Handbook*, W.-K. Chen, Ed. 2nd ed., Boca Raton, USA: CRC Publishing, 2006, pp. 12-1-12-44.

[41] X. Kang, W. Wang, Q. Li, J. Li, and C. Yuan, "TaN Etch in CF4/CHF3 gas for MEMS/Sensor application," *Solid-State and Integrated Circuit Technology, 2010 10th IEEE International Conference on,* pp. 1413-1415, 2010.

[42] C. L. Au, W. A. Anderson, D. A. Schmitz, J. C. Flassayer, and F. M. Collins, "Stability of tantalum nitride thin film resistors," *Journal of Materials Research,* vol. 5, no. 06, pp. 1224-1232, 1990.

[43] "Drift Calculation for Thin Film Resistors," ed. http://www.vishay.com/docs/28809/driftcalculation.pdf: Vishay Intertechnology, 2013.

[44] W.-F. Wu, K.-L. Ou, C.-P. Chou, and C.-C. Wu, "Effects of Nitrogen Plasma Treatment on Tantalum Diffusion Barriers in Copper Metallization," *Journal of The Electrochemical Society,* vol. 150, no. 2, p. G83, 2003.

[45] N. D. Cuong, N. M. Phuong, D.-J. Kim, B.-D. Kang, C.-S. Kim, and S.-G. Yoon, "Effect of annealing temperature on structural and electrical properties of tantalum nitride thin film resistors deposited on SiO_2/Si substrates by dc sputtering technique," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 24, no. 2, p. 682, 2006.

[46] N. Terao, "Structure of Tantalum Nitrides," *Japanese Journal of Applied Physics,* vol. 10, no. 2, pp. 248-259, 1971.

[47] K. Radhakrishnan, N. Geok Ing, and R. Gopalakrishnan, "Reactive sputter deposition and characterization of tantalum nitride thin films," *Materials Science and Engineering: B,* vol. 57, no. 3, pp. 224-227, 1999.
[48] C. M. Wang, J. H. Hsieh, C. Li, Y. Fu, and T. P. Chen, "Effects of annealing on the microstructure and electrical properties of TaN-Cu nanocomposite thin films," *Surface and Coatings Technology,* vol. 193, no. 1-3, pp. 173-177, 2005.
[49] N. D. Cuong, D.-J. Kim, B.-D. Kang, C.-S. Kim, and S.-G. Yoon, "Effect of film thickness on the electrical properties of tantalum nitride thin films deposited on SiO_2/Si substrates for Π-type attenuator applications," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 24, no. 3, p. 1398, 2006.
[50] M. Grosser, M. Soldera, M. Munch, and U. Schmid, "Tantalum based multilayers for high temperature sensor applications," *2008 IEEE Sensors,* pp. 474-477, 2008.
[51] R. Hübner *et al.*, "Structure and thermal stability of graded Ta–TaN diffusion barriers between Cu and SiO_2," *Thin Solid Films,* vol. 437, no. 1-2, pp. 248-256, 2003.
[52] R. Hubner *et al.*, "Comparison of the annealing behavior of thin Ta films deposited onto Si and SiO_2 substrates," *Anal Bioanal Chem,* vol. 379, no. 4, pp. 568-75, Jun 2004.
[53] L. Liu, Y. Wang, and H. Gong, "Annealing effects of tantalum films on Si and SiO_2/Si substrates in various vacuums," *Journal of Applied Physics,* vol. 90, no. 1, p. 416, 2001.
[54] S. L. Lee, M. Doxbeck, J. Mueller, M. Cipollo, and P. Cote, "Texture, structure and phase transformation in sputter beta tantalum coating," *Surface and Coatings Technology,* vol. 177-178, pp. 44-51, 2004.
[55] K. Valleti, A. Subrahmanyam, S. V. Joshi, A. R. Phani, M. Passacantando, and S. Santucci, "Studies on phase dependent mechanical properties of dc magnetron sputtered TaN thin films: evaluation of super hardness in orthorhombic Ta_4N phase," *Journal of Physics D: Applied Physics,* vol. 41, no. 4, p. 045409, 2008.
[56] L. Michalski, K. Eckersdorf, J. Kucharski, and J. McGhee, "Resistance Thermometers," in *Temperature Measurement*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 85-102.
[57] M. Ohring, "Physical Vapor Deposition," in *The Materials Science of Thin Films*, United Kingdom Edition ed., London, UK: Academic Press, 1992, pp. 79-144.
[58] R. M. Tiggelaar, R. G. P. Sanders, A. W. Groenland, and J. G. E. Gardeniers, "Stability of thin platinum films implemented in high-temperature microdevices," *Sensors and Actuators A: Physical,* vol. 152, no. 1, pp. 39-47, 2009.
[59] V. Guarnieri, L. Biazi, R. Marchiori, and A. Lago, "Platinum metallization for MEMS application. Focus on coating adhesion for biomedical applications," *Biomatter,* vol. 4, p. e28822, 2014.
[60] F. Lacy, S.-I. Ao, M. A. Amouzegar, and S.-S. Chen, "Characterizing Nanometer Sized Platinum Films for Temperature Measurements," *World Congress on Engineering and Computer Science,* vol. 1007, pp. 128-139, 2008.

[61] F. Lacy, "Evaluating the Resistivity-Temperature Relationship for RTDs and Other Conductors," *IEEE Sensors Journal,* vol. 11, no. 5, pp. 1208-1213, 2011.

[62] F. Lacy, "Investigating Thin Films for Use as Temperature Sensors," in *Proceedings of the World Congress on Engineering and Computer Science*, San Francisco, US, 2007, pp. 441-444.

[63] F. Lacy, "Using Nanometer Platinum Films as Temperature Sensors (Constraints From Experimental, Mathematical, and Finite-Element Analysis)," *IEEE Sensors Journal,* vol. 9, no. 9, pp. 1111-1117, 2009.

[64] R. D. Baxter and P. J. Freud, "Thin film resistance thermometer device with a predetermined temperature coefficent of resistance and its method of manufacture," USA Patent US4375056, 1983.

[65] G.-S. Chung and S.-S. Noh, "The Study on Characteristics of Platinum Thin Film RTD Temperature Sensors with Annealing Conditions," *Journal of Sensor Science and Technology,* vol. 6, no. 2, pp. 81-86, 1997.

[66] S. L. Firebaugh, K. F. Jensen, and M. A. Schmidt, "Investigation of high-temperature degradation of platinum thin films with an in situ resistance measurement apparatus," *Journal of Microelectromechanical Systems,* vol. 7, no. 1, pp. 128-135, 1998.

[67] M. Kawamura, T. Mashima, Y. Abe, and K. Sasaki, "Formation of ultra-thin continuous Pt and Al films by RF sputtering," *Thin Solid Films,* vol. 377-378, pp. 537-542, 2000.

[68] F. Mailly *et al.*, "Anemometer with hot platinum thin film," *Sensors and Actuators A: Physical,* vol. 94, no. 1-2, pp. 32-38, 2001.

[69] J.-S. Lee, H.-D. Park, S.-M. Shin, and J.-W. Park, "Agglomeration phenomena of high temperature coefficient of resistance platinum films deposited by electron beam evaporation," *Journal of Materials Science Letters,* vol. 16, no. 15, pp. 1257-1259, 1997.

[70] U. Schmid and H. Seidel, "Effect of high temperature annealing on the electrical performance of titanium/platinum thin films," *Thin Solid Films,* vol. 516, no. 6, pp. 898-906, 2008.

[71] J. O. Olowolafe, R. E. Jones, A. C. Campbell, R. I. Hegde, C. J. Mogab, and R. B. Gregory, "Effects of anneal ambients and Pt thickness on Pt/Ti and Pt/Ti/TiN interfacial reactions," *Journal of Applied Physics,* vol. 73, no. 4, p. 1764, 1993.

[72] F. Yi, W. Osborn, J. Betz, and D. A. LaVan, "Interactions of Adhesion Materials and Annealing Environment on Resistance and Stability of MEMS Platinum Heaters and Temperature Sensors," *Journal of Microelectromechanical Systems,* vol. 24, no. 4, pp. 1185-1192, 2015.

[73] E. Mastropaolo, R. Latif, E. Grady, and R. Cheung, "Control of stress in tantalum thin films for the fabrication of 3D MEMS structures," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 31, no. 6, p. 06FD02, 2013.

[74] A. a. Al-masha'al, A. Bunting, and R. Cheung, "Evaluation of residual stress in sputtered tantalum thin-film," *Applied Surface Science,* vol. 371, pp. 571-575, 2016.

Chapter 5 Development of integrated temperature transducer bridge

5.1 Introduction

Processes developed in previous chapter need to be integrated in a way that produces a thin film temperature sensing circuit. Thin films produced by separately developed tantalum nitride and platinum processes provide reasonable stability of both sheet resistance and the temperature coefficient of resistance, both of which has been shown to be linear. In this chapter developments towards an integrated version of a temperature transducer bridge are shown, where the temperature sensing capabilities produced by a combination of materials are first demonstrated using a hybrid version that interconnects elements produced in different materials and then processes are evaluated for integrating the circuitry into a single microfabrication process batch.

This chapter will describe the issues experienced during development of an integrated temperature transducer fabrication process and will describe the non-idealities of the integrated design that effect the transducer characteristics where they deviate from the expected performance. Finally, process modifications are described and the resulting improvements of the integrated design are determined.

5.2 Hybrid bridge-based temperature sensor

At this stage the previously developed processes were used to produce resistive elements on chips that were designed, fabricated and wire-bonded to produce a half-bridge configuration. A demonstration of the temperature sensitive capabilities of designed circuit was performed using a set of selected platinum and tantalum nitride chips containing fabricated resistors.

5.2.1 Fabricating and combining elements into a bridge

The wafer layout was designed to enable the fabricated resistors to be later arranged into a half-bridge configuration (as in Fig. 3.2.2) by interconnecting platinum and tantalum nitride resistors off-chip as shown in Fig. 5.2.1. The layout contains 3×3 mm chips (Fig. 5.2.2(a,b)) that were designed to be mounted in 10-pin TO-8 packages and the bond connections are shown in Figure 5.2.2(c) and 5.2.2(d). Chips containing TaN balancing resistors and chips that have resistor pairs were designed to provide the Pt temperature sensing elements.

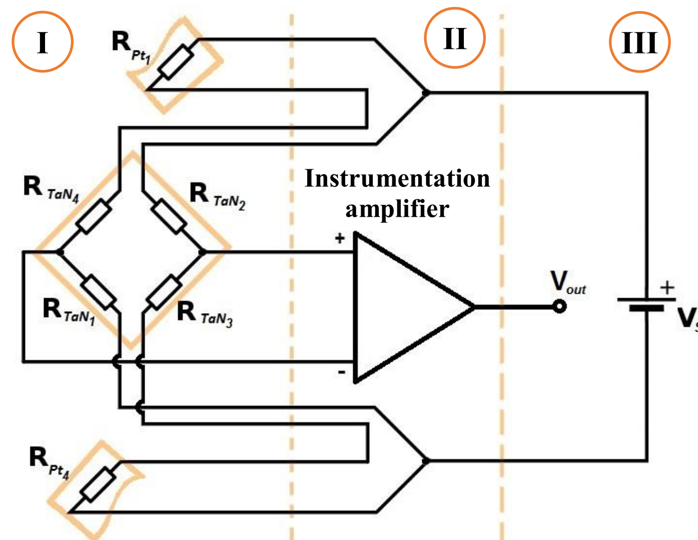

Figure 5.2.1: *Schematic diagram of the half-bridge used as a temperature transducing circuit. Section (I): TaN and Pt chips and circuit in TO-header socket assembly; section (II): PCB interconnect; section (III): external connections.*

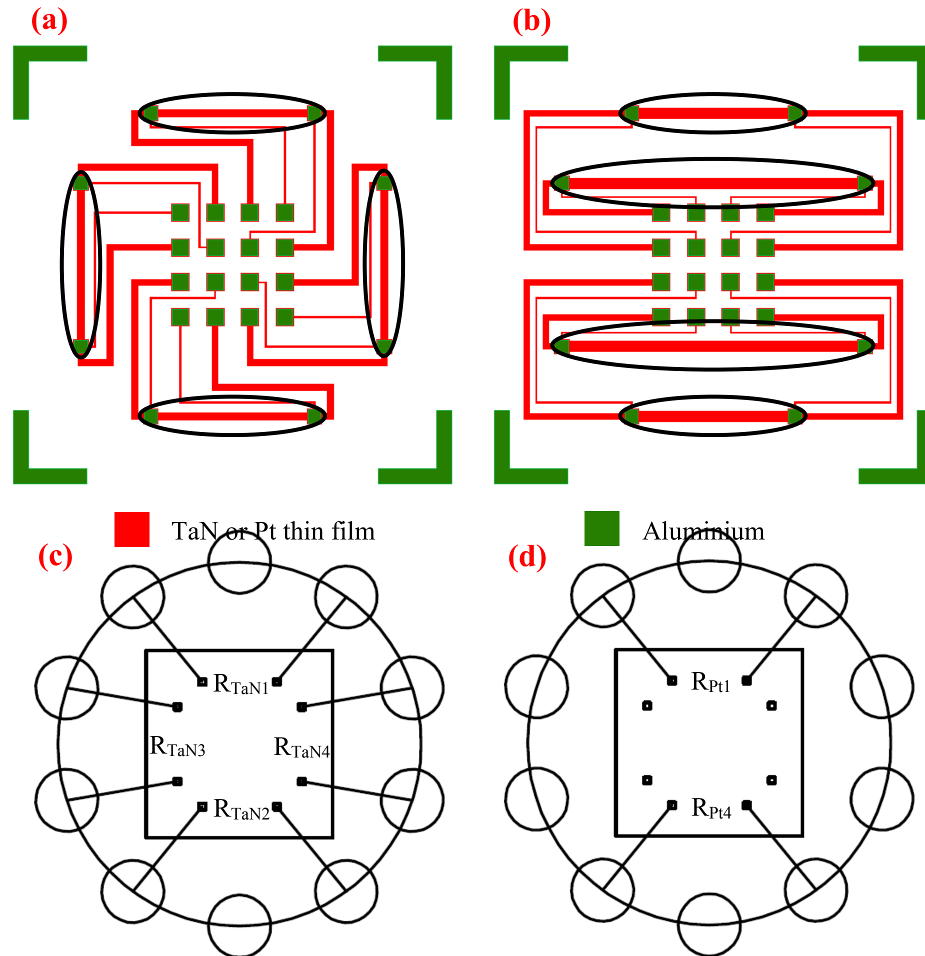

Figure 5.2.2: *Layout of discrete element chips: (a) TaN resistor layout; (b) Pt resistor layout; (c) bonding diagram for TaN chip; (d) bonding diagram for Pt chip.*

Table 5.2.1 *List of geometrical parameters and resultant resistance of designed thin film resistive elements.*

W, µm	*TaN resistors*		*Pt resistors*			
	Count	*R, Ω*	*Count*	*R, Ω*	*Count*	*R, Ω*
10	4	900-1500	2	300-500	2	600-1000
20	4	450-750	2	150-250	2	300-500
30	4	300-500	2	100-167	2	200-333
40	4	225-375	2	75-125	2	150-250
50	4	180-300	2	60-100	2	120-200
60	4	150-250	2	50-83.3	2	100-167
70	4	129-214	2	42.9-71.4	2	85.7-143
80	4	113-188	2	37.5-62.5	2	75-125
90	4	100-167	2	33.3-55.6	2	67-111

The drawback of this design was that the resistance of these elements was lower than that necessary for 15 V operation. This limitation was dictated by the restricted layout area of 3×3 mm per chip (including the area requirements of 4×4 probe pad with 240 μm pitch layout), and hence a much lower voltage was applied to demonstrate temperature sensing capabilities of the transducer. The layout provided the capability to measure the value of the fabricated resistors for element matching estimation. This was implemented by using an array of probe pads in the middle of chips. Aluminium bond pads were designed to ensure bond wires were of equal lengths and one Pt resistor pair was twice the size of the others with widths of 2000 and 1000 μm. The width of resistor element groups highlighted in Fig. 5.2.2(a,b) ranged between 10 to 90 μm in steps of 10 μm to produce resistors on different designed chips with values between (100 – 750; 900 – 1500) Ω for TaN (9 to 15 Ω/□) and (33.3 – 500; 600 – 1000) Ω for Pt (3 to 5 Ω/□). A summary of designed geometrical parameters and their resistance values are provided in Table 5.2.1.

Figure 5.2.3 shows the schematic layout of PCB that was designed to provide connections to the bridge (refer to Fig. 5.2.1), which creates a temperature transducer and instrumentation amplifier setup. The temperature transducer was designed to be used for DC operation and therefore the reference terminal of the instrumentation amplifier was set to 0 V with an 11 kΩ 1% resistor used to ensure that the gain of differential output from the bridge was 10.1× [1]. Amplifying the output from the bridge became a necessary step because the output produced by the temperature transducer (estimated without instrumentation amplifier gain) ranged between 0.1 to 0.5 V for the evaluated resistor element and transducer input voltage combinations. Hence, the temperature sensitivity of circuit was expected to be low.

TaN thin film resistors were fabricated using a 10% nitrogen flow ratio process for 90 minutes in order to produce TCR value of the material close to zero. Since the available test setup was capable of only short-term measurements in a limited temperature range, no drift of sheet resistance or TCR values was expected to be observed and this was the case. Hence, the 10% process was preferred at this stage to the 12% process. The deposited TaN was annealed for 6 hours at 600 °C, patterned

using 1.5 μm SPR350 resist and etched using CF_4 + O_2 plasma for 30 minutes (please refer to subsection 4.4.3 for more complete process details).

Pt resistive elements (100 nm target thickness) were deposited onto a 10 nm TaN adhesion layer (10% TaN process used for 4 minutes) covering the oxidised silicon wafer that was then transferred immediately from the sputterer into the e-beam evaporator. The resultant layers were vacuum annealed for 12 hours at 500° C. This thin film structure was patterned using 1.5 μm SPR350 using four 10 minute runs of argon milling in the STS Multiplex RIE tool set at 30 mTorr and 30 W power.

Next, in order to avoid etch damage to TaN or Pt both types of wafers were prepared for lift-off of aluminium, which was used as a contact material for the gold bonding wires. Around 1.5 μm-thick AZ5214E image reversal resist was deposited, soft baked, and exposed for 10 second in proximity contact mode using spacers. Then resist reversal bake was performed, and the wafer flood exposed for 50 seconds followed by a 90 seconds develop in AZ726MIF. Finally, the wafers were rinsed in DI water. Both types of wafers were covered by 500 nm aluminium produced by the ANS evaporator and the lift-off process was performed for 15 minutes at 50 °C in ACT CMI-S followed by rinsing in DI water.

Following inspection of the materials using an optical microscope, resistors were selected and assembled to create a half-bridge configuration for temperature sensing: two chips with 10 μm wide tantalum nitride resistors, and four platinum chips with resistor widths of 60, 70, 80 and 90 μm.

5.2.2 Experimental setup

A hybrid bridge temperature sensing capability was demonstrated using the test setup shown in Fig. 5.2.3. A parametric semiconductor analyser HP4145B was used to provide the voltage input to the bridge and also measure the output from the bridge amplified by an instrumentation amplifier. The bridge circuit mounted in a TO-package was connected to the PCB using a socket and the complete circuit board placed in a shielded BNC box. The temperature was controlled manually using a Heraeus conditioning oven T5028 with a Kane May KM330 digital thermometer

(K-type thermocouple) using a digital multimeter (HP34401A) for readout. The digital multimeter and parametric analyser were controlled using a netbook connected through a Prologix USB-GPIB converter. The HP4145B was used to supply 1 V input to the transducer (accuracy of 1.5 μV) and measure the voltage with 100 μV measurement resolution. The oven was only capable of precise temperature control in the temperature range of 25 to 100 °C so that was the range evaluated in this experimental study.

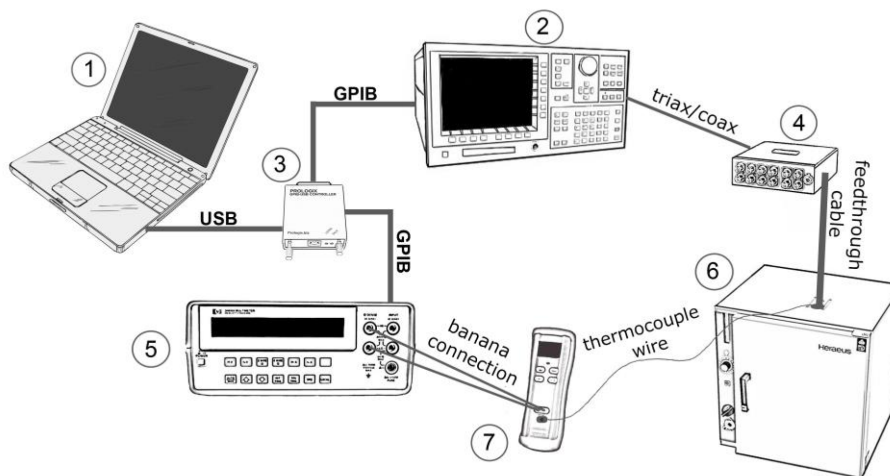

Figure 5.2.3: *Test setup designed to measure hybrid bridge temperature response. 1: Netbook, 2: Parametric semiconductor analyser, 3: USB-GPIB converter, 4: BNC box, 5: Digital multimeter, 6: Oven, 7: Digital thermometer.*

The thermocouple output was determined using a microvoltmeter calibrated using readings provided by thermocouple display. Limited oven power was applied during this stage and temperature range of 25 to 45 °C was used and no drift of thermocouple readings was observed. Any drift was most likely to be related to changes in the cold junction temperature because K-type thermocouples are known to have linear response to temperature with the compensation for cold junction temperature effect being implemented in the thermocouple reader [2]. This effect appeared as a systematic error at temperatures higher than 45 °C or when oven was heated quickly.

A LabVIEW VI library was created that controlled the multimeter (HP34401A) and the parametric analyser (HP4145B) in semi-automatic mode. A block diagram of designed virtual instruments is shown on Figure 5.2.4.

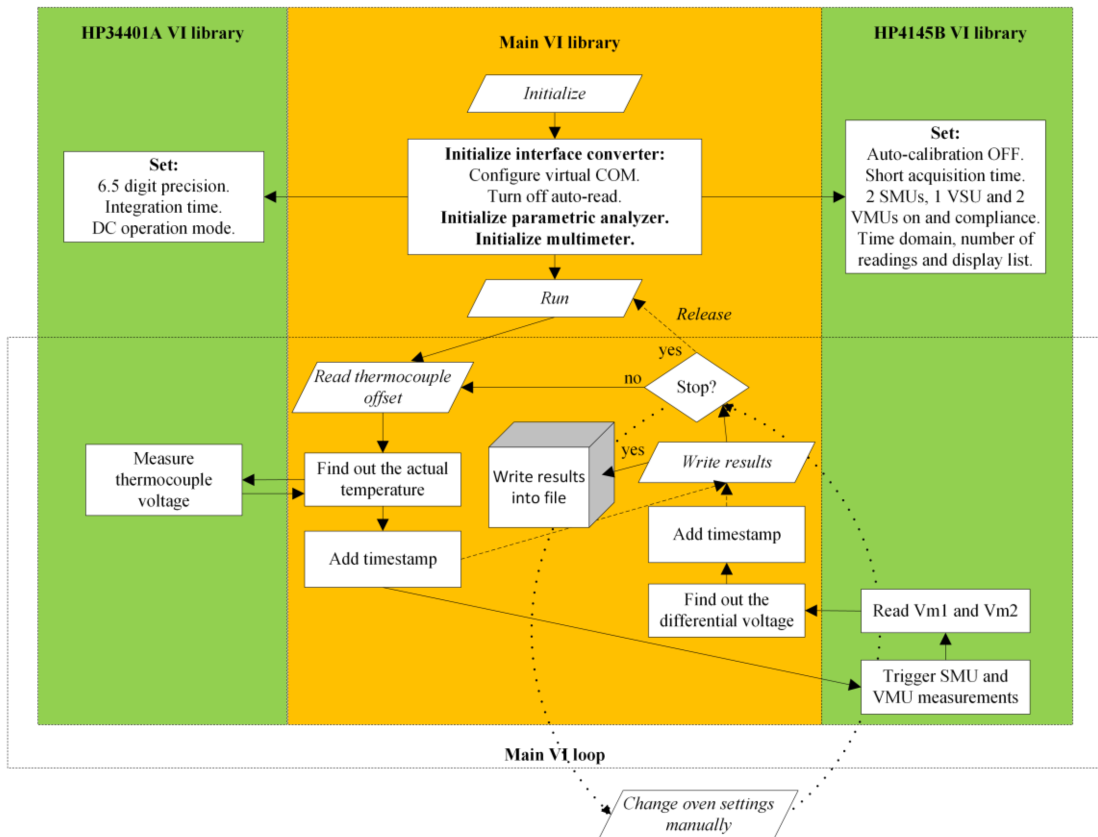

Figure 5.2.4: *Block diagram of created virtual instrument functional flow.*

5.2.3 Demonstration of temperature sensing capabilities

Before the assembled circuit was used as a temperature transducer, the effect of parasitic resistances in a balancing circuit consisting only of TaN resistors was estimated. Platinum resistors shown in Fig. 5.2.1 were replaced by wide cross-section aluminium wires. It was not possible to measure the unamplified output from the bridge and as a result the output from instrumentation amplifier was used to perform this test. The amplified output from the bridge contains both differential and common mode signal components. Typical CMRR at DC quoted in the instrumentation amplifier datasheet is 110 dB [1, 3]. As the reference voltage node V_{REF} was tied to 0 V the equations that describes the output from amplifier are:

$$V_{OUT} = V_{OUTdiff} + V_{OUTcm} = G \times (V_+ - V_-) + \frac{G \times V_{INcm}}{\log^{-1}\left(\frac{CMRR}{20}\right)} \qquad (5.1)$$

$$V_{OUT} = 10.1V_S \times \left(\frac{R_{TaN3} + R_{Pt4}}{R_{TaN2} + R_{TaN3} + R_{Pt4}} - \frac{R_{TaN1}}{R_{TaN4} + R_{TaN1} + R_{Pt1}} + \frac{V_{INcm}}{10^{5.5}} \right) \quad (5.2)$$

Since two bridge arms have nodes that are independent one from another and are only dependent on the voltage supplied V_S that is common for both arms while some parasitic elements due to leads, contacts etc. that are connecting the circuit to each of the TaN resistors are expected to exist, (5.2) may be rewritten into:

$$V_{OUTdiff} = 10.1V_S \times \left(\frac{R_1' + R_{Par1}' + R_{Pt}}{R_1'(1+A) + R_{Par1}'(1+C)} - \frac{R_2'}{R_2'(1+B) + R_{Par2}'(1+D)} \right) \quad (5.3)$$

$$V_{OUTcm} \approx 10^{-4.8} V_S \times \left(\frac{R_1' + R_{Par1}' + R_{Pt}}{R_1'(1+A) + R_{Par1}'(1+C)} + \frac{R_2'}{R_2'(1+B) + R_{Par2}'(1+D)} \right), \quad (5.4)$$

where for different bridge arms $A = \frac{R_{TaN2}}{R_{TaN3}}$ and $B = \frac{R_{TaN4}}{R_{TaN1}}$ are resistance proportions for TaN resistors in. and $C = \frac{R_{Pt4}}{R_{Par1}}$ and $D = \frac{R_{Pt1}}{R_{Par2}}$ are proportions of parasitic resistance to platinum element resistance. It can be recognized from (5.4) that the common mode term is negligibly small and is at least 1000 times lower in value than the differential term. If TaN resistors in Fig. 5.2.1 were swapped between bridge arms, the equation describing the differential term of amplifier output becomes:

$$V_{OUTdiff} = 10.1V_S \times \left(\frac{BR_2' + R_{Par1}' + R_{Pt}}{R_2'(1+B) + R_{Par1}'(1+C)} - \frac{AR_1'}{R_1'(1+A) + R_{Par2}'(1+D)} \right) \quad (5.5)$$

If parasitic resistances in both arms are equal or if the TaN resistors were perfectly matched, then the differential output voltages described by equations 5.3 and 5.5 would be equal while each of positive and negative outputs of the bridge would be different as shown by proportions in the equations. This is because only the common mode voltage changes in a response to essentially a different supply polarity, but the differential voltage stays the same. As parasitic resistance exists in both bridge arms and its scale is different, some mismatch in TaN resistors is expected, and the voltage response of circuits produced by TaN resistors pairs from the right and the left-hand side of the chip in Fig. 5.2.2(c) is shown in Fig. 5.2.5.

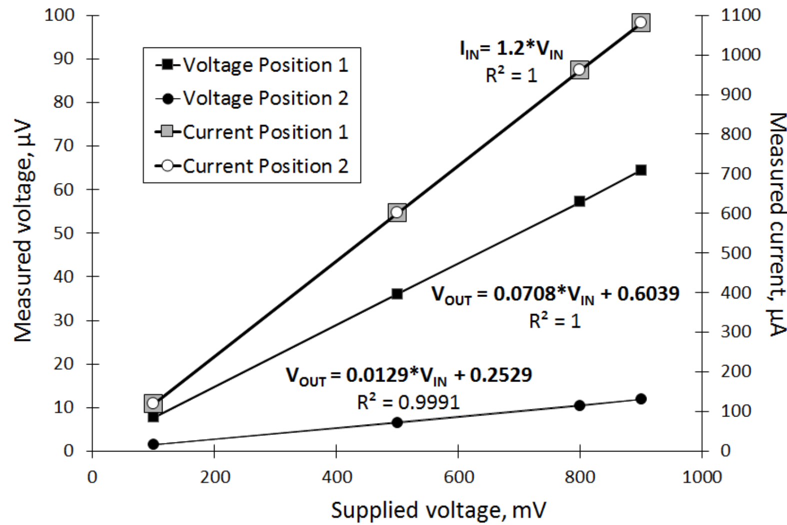

Figure 5.2.5: *Estimation of parasitic effects on balancing circuit in right-hand side (1) and left-hand side (2) positions.*

Measured current flowing into the bridge is identical for both balancing resistor array positions and is linearly proportional to the supplied voltage (1.2 $\mu A \cdot mV^{-1}$). This indicates an average single TaN resistor value of around 833 Ω. Differential outputs of 7.08 µV/V and 1.29 µV/V indicate that the mismatch between TaN resistors is less than 0.1% or 0.8 Ω with the parasitic resistance changes for different connections staying less than 0.1 Ω. TaN resistors were further used in left-hand side position to reproduce the same parasitic resistance conditions. Using 60 µm-wide Pt resistors meant that the resistance ratio between temperature sensing and balancing resistors would be a maximum of 6%, which is a reasonable value to demonstrate temperature sensitivity of the implemented circuit. A combination that used the TaN chip with 10 µm wide resistors and Pt chip with 60 µm wide resistors was finally selected for the temperature sensing demonstration. A convenient range of up to 0.1 V was estimated for the bridge output when 1 V is supplied to the bridge.

A platinum sensing element chip was fitted into the socket and temperature test was performed. There was no possibility to stabilize the temperature, therefore it was ramped up and held constant in 10 to 20 minute cycles to allow the platinum thin film elements and thermocouple to reach the same temperature. Measurement data was taken independently for temperature and sensor outputs at the fastest possible rate. Measured data points (red) plot in Fig. 5.2.6 were taken at the time when the

thermocouple voltage and sensor output reached local maxima within the cycle as there was a systematic delay in temperature as measured by the thermocouple and the response to temperature by the bridge circuit.

The temperature measured by the voltmeter only accounts for thermocouple sensitivity and offset values that were set before the temperature ramp started. As the total measurement period lasted for 90 minutes, a correction of systematic temperature measurement errors was undertaken and the result is shown as a corrected data (green) in Fig. 5.2.6.

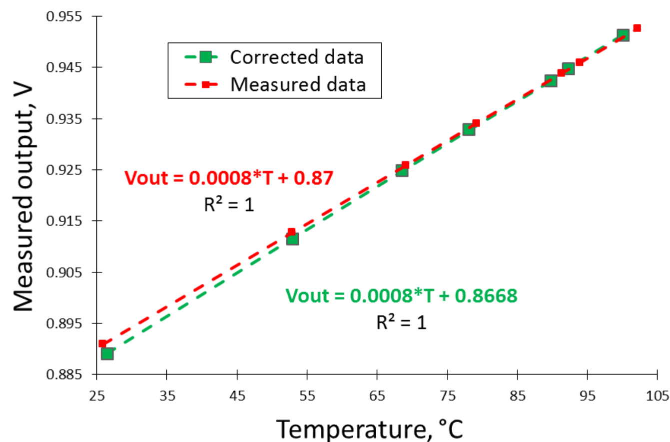

Figure 5.2.6: *Measured temperature response of implemented bridge.*

The measured sensitivity of the bridge was 844 μV·°C^{-1}, which is a reasonable value given that the sensitivity of platinum elements is rather low (1340 ppm °C^{-1}). This compares with a bulk value (3850 ppm °C^{-1}), and is acceptable for the purpose of a temperature sensing demonstration. The sensitivity value that was estimated using uncorrected time-temperature scale was 809 μV·°C^{-1}. Both temperature response plots are linear in the temperature range of 25 to 100 °C.

5.2.4 Conclusions

The assembled circuit has demonstrated the temperature sensing capabilities of the half-bridge built using discrete microfabricated resistor elements. Although the bridge configuration contains some parasitic elements of up to 0.1 Ω and there was a systematic problem related to the temperature difference of a thermocouple and

designed transducer half-bridge arrangement, the linearity of the measured response to temperature is very good. The sensitivity of the reported bridge was 844 $\mu V \cdot °C^{-1}$, which is mainly defined by the TCR of the fabricated platinum elements (1340 ppm $°C^{-1}$). The TCR of the TaN elements was close to zero as expected. It was not possible to estimate the mismatch between balancing resistors precisely using this setup, but this was estimated to be less than 0.1%.

5.3 Integrated bridge-based design

An integrated bridge design was devised that combined the processes developed in Chapter 4 and provided separation and electrical isolation between balancing and temperature sensing resistor layers. The purpose of this design was to demonstrate the integrity of the sensor produced by the microfabrication processes reported above and to provide an estimation of the parasitic circuit parameters which appear when two layers are connected together to produce a functional temperature transducer.

5.3.1 Integrated sensor device design

If the temperature transducer was built of tantalum nitride and platinum elements that had identical resistance values for each conductor material, then expression (5.6) describes the expected transducer output at any given temperature and (5.7) describes the output at elevated temperature T:

$$V_{OUT} = V_S \times \left(\frac{R_{TaN} + R_{Pt}}{2R_{TaN} + R_{Pt}} - \frac{R_{TaN}}{2R_{TaN} + R_{Pt}} \right) = V_S \frac{R_{Pt}}{2R_{TaN} + R_{Pt}} \tag{5.6}$$

$$V_{OUT}(\Delta T) = V_S \frac{R_{Pt}(1 + \alpha_{Pt}\Delta T)}{2R_{TaN}(1 + \alpha_{TaN}\Delta T) + R_{Pt}(1 + \alpha_{Pt}\Delta T)}, \tag{5.7}$$

where $\Delta T = T - T_0$ is the temperature difference between the elevated temperature and temperature T_0 at which resistor value was measured, and α is the first order temperature coefficient of resistance estimated across the temperature range.

As shown using these equations, the set ratio between platinum and tantalum nitride resistors at room temperature (or any other temperature T_0) defines the output range. Temperature transducers with different output range characteristics were designed using a range of calculated Pt to TaN resistor ratios. The resistance of each element depends on both the drawn geometrical parameters of features and the sheet resistance of the conducting layer at that point on the wafer. Scaling the resistors by increasing or decreasing resistance of both elements was absolutely impractical since increasing the resistance leads to an increased layout area and reducing it increases the transducer current. The drawn length of the tantalum nitride resistors was kept constant, the length of platinum resistors was modified to produce different ratios while the width of both resistors was 20 μm.

The process that used a 12% nitrogen flow ratio targeted a TaN layer with sheet resistance of 12 to 16 Ω/□ while the Pt target was a sheet resistance between 2 and 4 Ω/□ for thickness of 100 nm. The transducer features in both layers were produced by 20 μm-wide serpentine-shaped tracks, which were placed symmetrically across the design area to minimise mismatch in the resistors. The designed length of the tantalum nitride resistor for all sensor devices (Fig. 5.3.1, 5.3.2 and 5.3.3) was 870 squares, where 90 degree corners were counted as half a square according to accepted design rules [4]. Such a length of balancing resistors was selected according to a maximum power dissipation criterion. Eight different platinum resistor lengths were used to produce devices a range of different output values. A summary of designed device parameters is given in Table 5.3.1, where the device prefix given to each design indicates the closest ratio between designed temperature sensing and balancing resistors. Ratios were estimated in steps of 0.5% for room temperature and sheet resistance of 4 and 15 Ω/□ for Pt and TaN layers respectively.

Two different layouts of temperature transducer were designed that integrated the sensor with the instrumentation amplifier. A first design was planned to be used as a standalone sensor as shown on Figure 5.3.1. The insulation between conducting layers was provided by PECVD oxide and all necessary connections were fabricated using different masks. This design provided via connections directly to the instrumentation amplifier power and differential input terminals, with the differential

output being available at the instrumentation amplifier output terminals. The TaN resistor length in this case was calculated between instrumentation power terminal and connection to Pt resistor vias. Since the footprint of the transducer did not cover the whole chip area, extra space was used to create an array of test structures including Greek cross and cross-bridge test structures, which can be used to measure the sheet resistance of a layer in the particular area on the wafer.

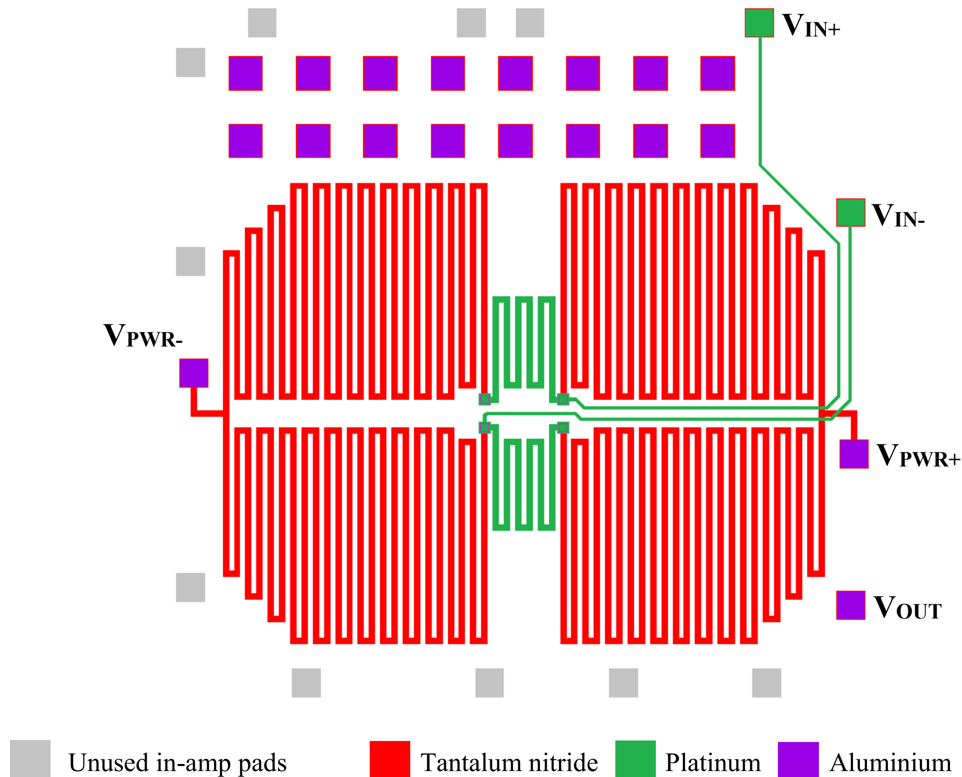

Figure 5.3.1: *Designed bridge to be integrated with SiC electronics and used as a standalone sensor with extra space for test structures.*

A second layout was designed to be measured using the semi-automatic prober using probe pad layout indicated in Fig. 5.3.2 and 5.3.3. The TaN resistor length was calculated between the probe pad and via to Pt resistor. Hence, each of the serpentine resistor parts was designed 128 squares shorter, which had to be compensated by 64 squares laid out in a path common to two parallel TaN resistors (difference between two designs highlighted in Fig. 5.3.2). Such a layout enabled the supply of different voltages to the instrumentation amplifier and temperature transducer bridge. Two

interconnect strategies to connect to the instrumentation amplifier were adopted for this design: one used TaN as interconnect metal and another used Al. The first type of interconnect (Fig. 5.3.2) enabled the fabrication of a fully functional temperature transducer without using the aluminium layer. The drawback of using TaN as interconnect metal was that the resistance of tracks that were each 68 squares long is rather high and would result in a significant drop in power supply voltage.

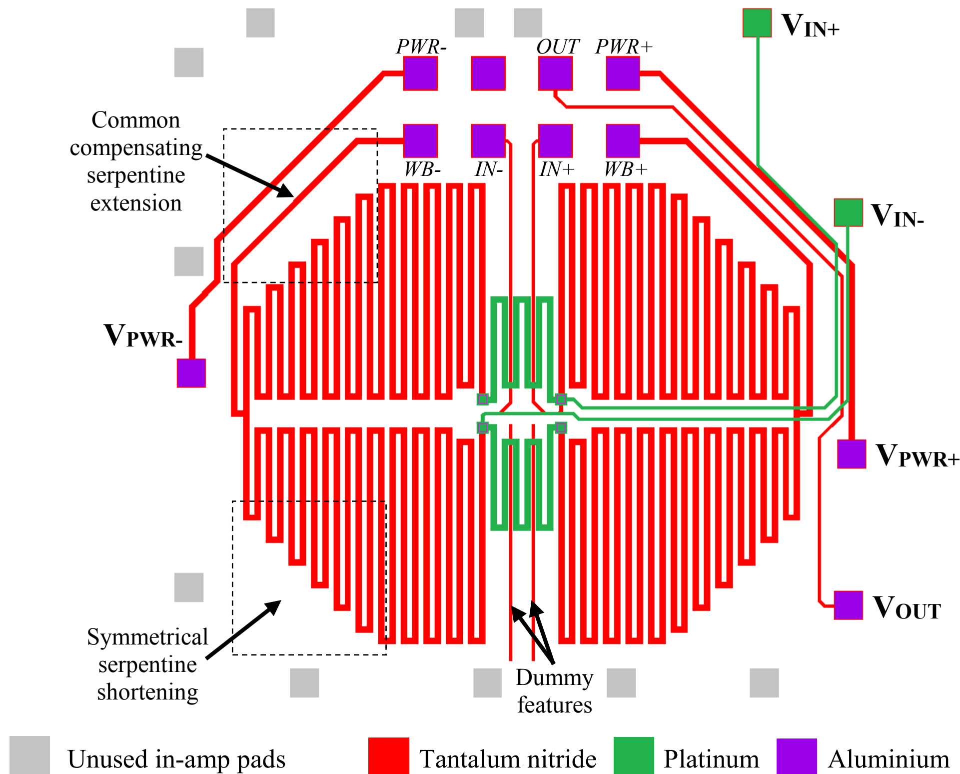

Figure 5.3.2: *Layout of a bridge to be integrated with SiC electronics and measured using the probe array: interconnect in TaN layer.*

The other approach (Fig. 5.3.3) used Al tracks to provide connections between probe pads and power and output terminals of instrumentation amplifier. Dummy TaN and Al tracks were added to provide similar stress conditions for Pt resistor tracks, where the former and the latter intersect.

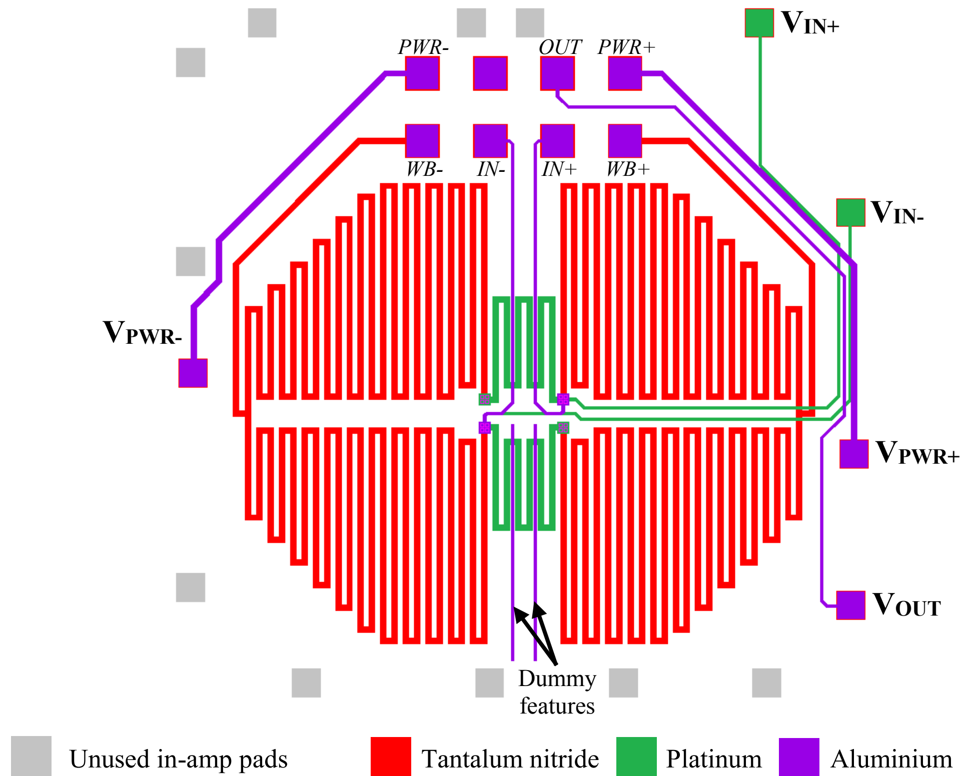

Figure 5.3.3: *Layout of a bridge to be integrated with SiC electronics and measured using the probe array: interconnect in Al layer.*

The maximum calculated power of the designed transducers at room temperature is 21.35 mW and 22.35 mW at 300 °C for the 15 V supply. The total number of sensor chips for each resistance ratio is 20, where 12 temperature sensors can be measured using bond pads and 8 are available via the probe pad arrays. It is important to note that Pt and TaN are materials which are an important part of the design because they define the sensor characteristics whereas Al is used as an interconnect metal for purpose of demonstration and can be replaced by any other comparable material with improved high temperature characteristics.

Table 5.3.1 *List of design elements and parameters of designed transducers.*

Bridge design parameters		
Device prefix	*Platinum resistor length, squares*	*Bridge resistance range, Ω*
3.0	97	10537 – 14114
3.5	115	10555 – 14150
4.0	133	10573 – 14186
4.5	151	10591 – 14222
5.0	169	10609 – 14258
5.5	189	10629 – 14297
6.0	207	10647 – 14333
6.5	225	10665 – 14369

5.3.2 Supplementary test structure design

Greek cross and cross-bridge structures have been added to each sensor chip layout depicted in Fig. 5.3.1. The summary of these structures is provided in Table 5.3.2, where the titles of designed cells stand for designed test structure count and material layer used.

Table 5.3.2 *List of designed resistive test structures according to cell name.*

Layer	*Cross-Bridges*	*Width, µm*	*Greek Crosses*	*Width, µm*
TaN	0	-	4	10, 15, 20, 25
TaN	1	20	2	10, 20
TaN	2	10, 20	0	-
Pt	0	-	4	10, 15, 20, 25
Pt	1	20	2	10, 20
Pt	2	10, 20	0	-

Cross-Bridge Kelvin Resistor (CBKR) contact resistance structures were added to wafer layout cells, designed specifically to accommodate the contact resistance structures. The latter were extremely important in order to evaluate the feasibility of tantalum nitride and platinum process integration. As shown in Figure 5.3.4 this structure is used to force the current in direction between terminals 1 and 2 while measuring the voltage across terminals 3 and 4.

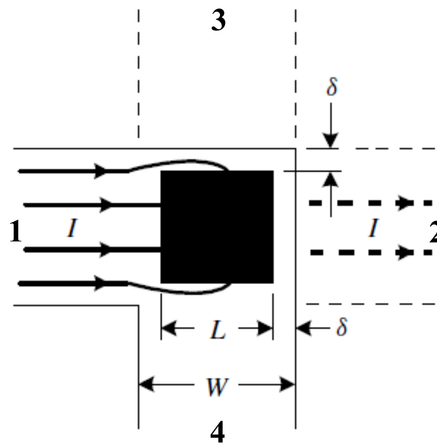

Figure 5.3.4: *Illustration of CBKR measurement and error sources in the contact resistance measurement. Adapted from [5].*

In the general case contact resistance may be determined using equation (5.8):

$$R_C = \frac{V_{34}}{I} \tag{5.8}$$

Errors associated with voltage and current measurement tools and probing conditions are eliminated by supplying forward and reverse current firstly between terminals 1 and 2 and then between terminals 3 and 4 and measuring voltage between the other two terminals. However, there is also an error associated with alignment collar δ (as shown in Fig. 5.3.4), defined by:

$$2\delta = W - L \tag{5.9}$$

The collar is required to ensure the contact is robust to the expected mask misalignment. The "electrical" error is associated with the fact that the current splits into a part that flows directly through contact and another part, which spreads around the contact area. This phenomenon is expected to take place in both layers and the task of error estimation becomes very complex, especially when there is a misalignment between two metals layers, and metal and via. Another drawback of such CBKR design is that there are always two contacts in the current path, which significantly increases the voltage supplied in order to provide the necessary current if contact resistance value is high. This also creates a voltage asymmetry if the via contact resistances are different.

Four CBKR structures with contact sizes 10×10, 15×15 and 20×20 μm^2 were used. The width of CBKR structure was 30 μm for both layers and the set of structures is shown in Fig. 5.3.5. For any contact resistance cell a total of twelve structures were designed to measure contact between Pt and TaN layers with the same number of structures designed to measure the contact resistance between aluminium and platinum. The characteristic resistance value may be determined with reasonable accuracy from three contact size values using (5.10), where possible non-linearity in the product plot can be explained by the measured contact resistance not scaling with area [6, 7]. The designed δ values were accordingly 10, 7.5 and 5 μm.

$$\rho_C = R_C A_C = R_{C10} \times 10^2\,\mu m^2 = R_{C15} \times 15^2\,\mu m^2 = R_{C20} \times 20^2\,\mu m^2 \qquad (5.10)$$

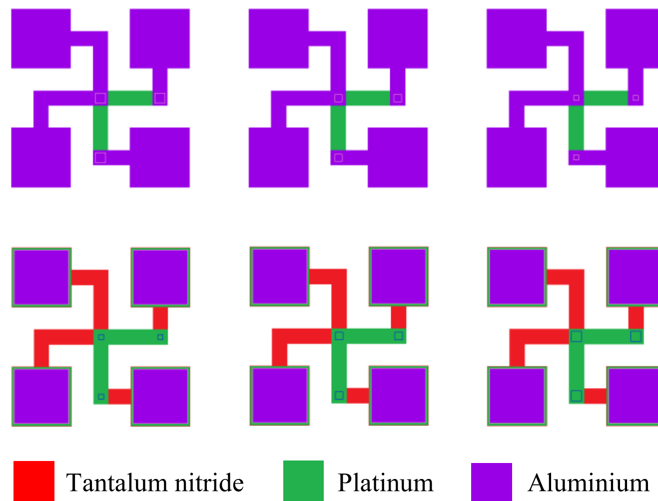

Figure 5.3.5: *Layout of Cross-Bridge Kelvin Resistor test structures:*
Top – CBKR structures between aluminium and platinum layers;
Bottom – CBKR structures between platinum and tantalum nitride layers.

A total of 68 dedicated contact resistance chips were added to the layout with 52 chips positioned near the 6 mm exclusion ring of a 3” wafer and 16 chips allocated closer to the wafer centre. The chip layout on the wafer for both integrated temperature sensors and different resistive test structures is depicted in Figure 5.3.6.

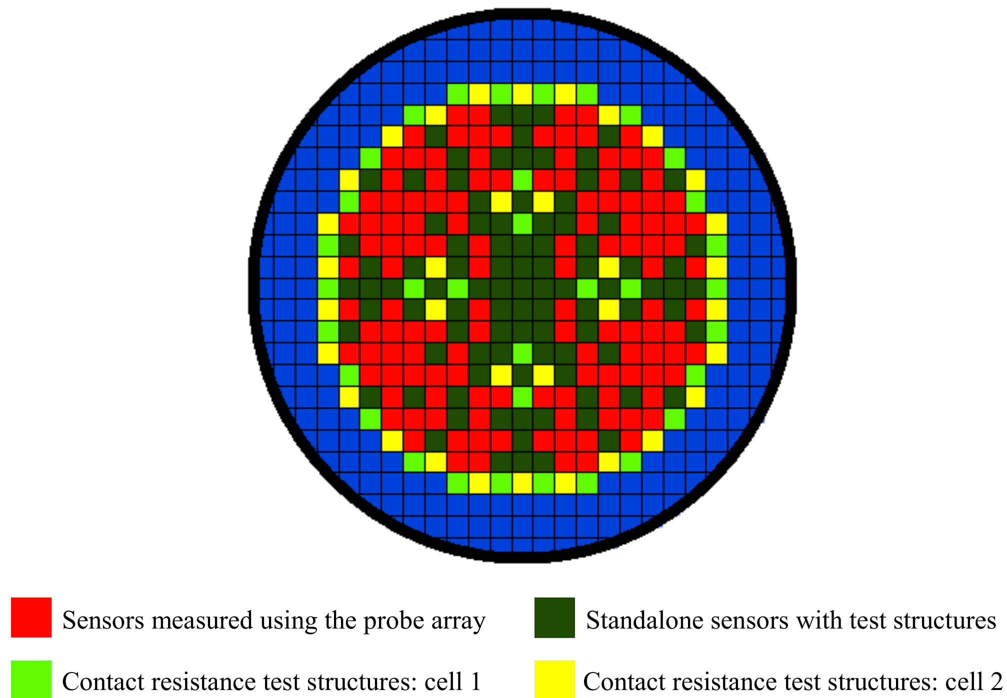

Figure 5.3.6: *3" wafer layout of chips.*

5.4 Fabrication

Before the integrated sensor fabrication process was undertaken, the successful deposition and etching processes of aluminium and PECVD oxide were performed on oxidised silicon wafers. A thin film aluminium interconnect layer was deposited on oxidised silicon wafers for 45 minutes using 1 kW DC power. The deposited aluminium thickness was around 250 nm using a sample with patterned lift-off resist. The '3SBD1' process was used for 15 minutes on STS Multiplex RIE system to completely remove Al in areas uncovered by resist. The aluminium thickness was increased to around 500 nm by two 45-minute deposition runs without breaking the vacuum to avoid Al target heating. Five seconds was determined as an optimum exposure time under chrome mask to produce patterns in 1.5 μm-thick SPR350 resist that were later used to produce 0.5 μm-thick aluminium features by dry etching. The '3SBD1' process was used for 25 minutes on STS Multiplex RIE system to completely remove Al in areas uncovered by resist.

PECVD oxide was deposited on oxidised silicon wafers covered by 200 nm of annealed TaN thin film to provide a similar combination of metal thin film and thin

film oxide to be used during target integrated fabrication process. The thickness of the PECVD oxide layer was expected to be close to 500 nm as it was produced by a well-characterised process run for 8 minutes. SPR350 resist was deposited and exposured for nine seconds which produced the best pattern of both vias that were etched. Dry etch processing was carried out using JLS RIE 80 tool in 100 W plasma produced by a combination of 17.7 sccm CHF_3 and 20 sscm Ar gases at a pressure of 30 mTorr for 35 minutes.

Initial integrated sensor fabrication process used a series of material deposition, resist patterning, material etching and resist removal steps. Sensor devices and related test structures consisted of four layers (Fig. 5.4.1):

- A 200 nm-thick tantalum nitride thin film (TaN) layer;
- A 500 nm-thick PECVD thin film oxide layer that was designed to separate features produced in TaN and the following layer;
- A 100 nm-thick platinum thin film layer (Pt) deposited on a 10 nm-thick TaN adhesion layer;
- Another 0.5 µm PECVD oxide (SiO_2) layer that insulates features fabricated in Pt and the following layer;
- A 500 nm-thick aluminium layer (Al).

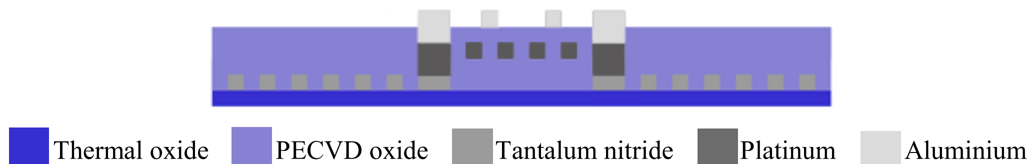

Figure 5.4.1: *Illustration of sensor device and test structure forming layers.*

The TaN thin film was vacuum-annealed for 5 hours at 600 °C while the platinum film was annealed for 12 hours at 500 °C immediately after film deposition. The aluminium interconnect layer was not annealed. Both TaN and Pt experienced heat treatment during fabrication steps other than their layer-specific annealing and these steps are described below:

- After TaN was annealed it was expected to experience elevated temperature effect during soft- and hardbake of resist patterning TaN, Pt and Al, and twice during bakes of resist patterning LF SiO_2. Wafers with the TaN thin film was

also exposed to 250 °C for 8 minutes during deposition of PECVD oxide firstly in a highly oxidising environment when the TaN film was exposed to the chamber environment and then, in a following process, when it was already covered by the PECVD oxide layer. Most importantly, the Pt annealing step introduced an extra 12 hour 500 °C treatment to the patterned TaN covered by PECVD oxide;

- The annealed Pt thin film experienced elevated temperature effects during resist bakes patterning Pt, Al and LF SiO_2 and was also exposed to 250 °C for 12 minutes during deposition of PECVD oxide.

These extra elevated temperature treatments may influence thin film to some extent; however, in the majority of cases they would be expected to have little to no effect on resultant thin film characteristics. The TaN thin film will be most affected by the PECVD oxide process when it is exposed to an oxidising environment and also during the 500 °C annealing step. However, TaN film will stay within the expected sheet resistance and TCR value range as indicated by values measured on films fabricated for the purpose of process control.

The final designed microfabrication process flow is depicted in Figure 5.4.2 and detailed in Table A.1 in Appendix A. For more process details refer to runsheet A.1.

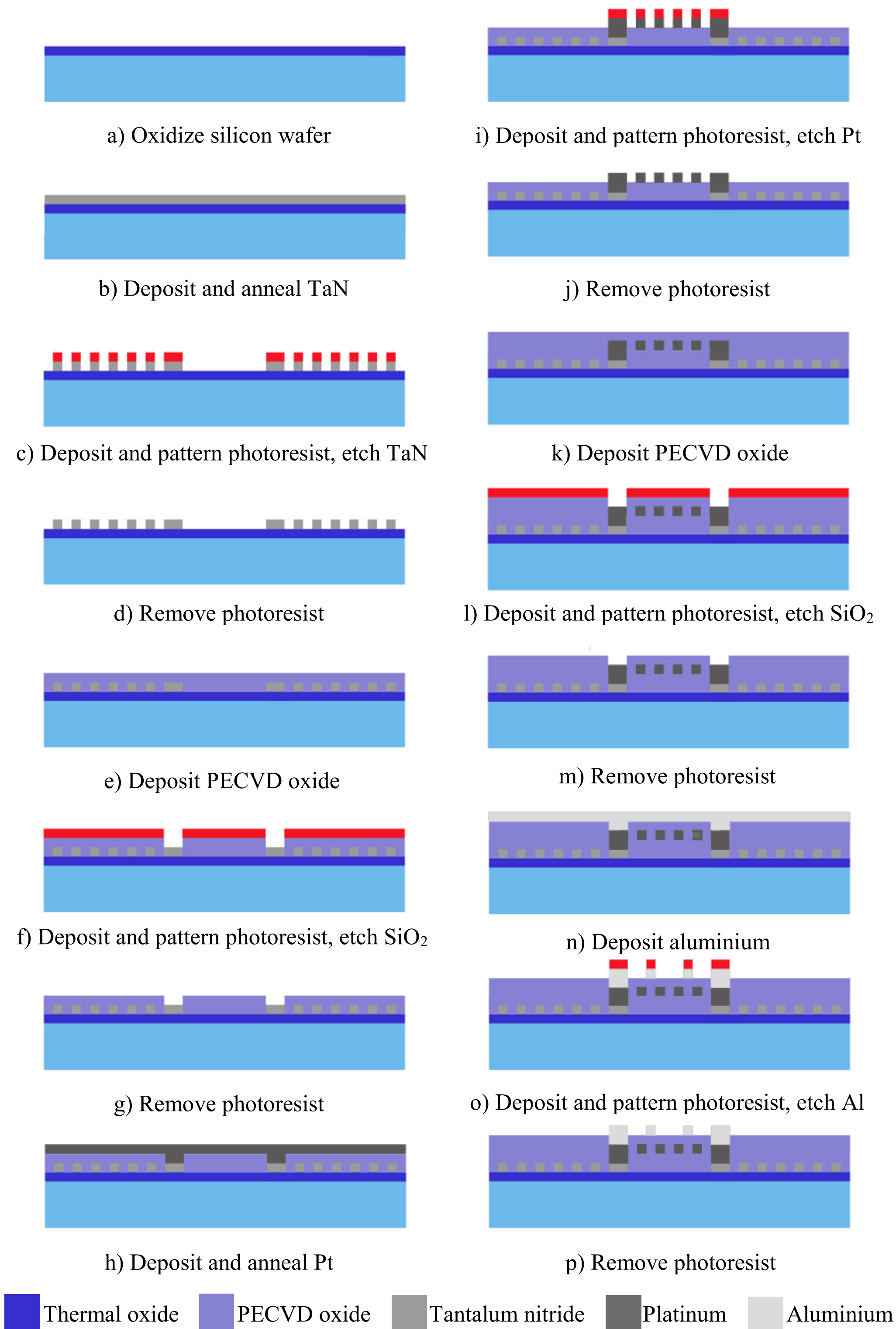

Figure 5.4.2: *The microfabrication process flow for Process 1.*

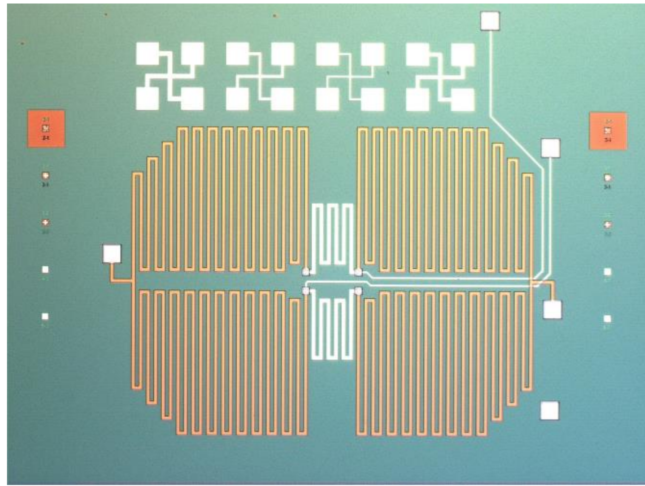

Figure 5.4.3: *Fabricated standalone bridge designed to be integrated with SiC electronics with sheet resistance test structures on the chip.*

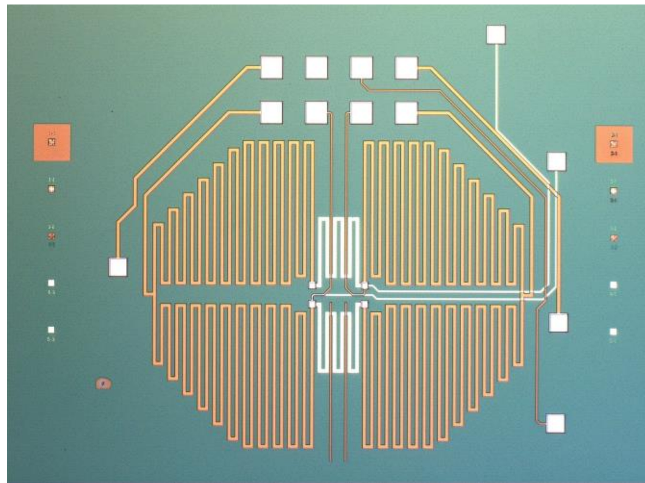

Figure 5.4.4: *Fabricated standalone bridge with TaN interconnect designed to be integrated with SiC electronics and measured using the probe array.*

Following from the initial integrated process fabrication efforts the specific contact resistance between aluminium and platinum layers was determined to be 69.4 $\Omega\cdot\mu m^2$, the average contact resistance extrapolated for infinite area was of the order of 0.1 Ω, and measured contact resistance was below 1 Ω for any structure of $10\times10\ \mu m^2$ contact area. The purpose of the aluminium layer was primarily to create voltage taps and as a result the Al to Pt contact test structures became unimportant both in terms of fabrication and measurement. A series of initial batches that used only TaN and Pt layers produced test structures with extremely poor yield and as a

result all fabrication effort was focussed on improving the yield. The integrated device-related batches (examples of fabricated devices are shown in Fig. 5.4.3 and 5.4.4) were primarily used to improve layer alignment, identify defects in features using light microscopy, determine visual structure differences between fabricated sensor structures and contact resistance structures (because the processes were run in parallel batches) and also to troubleshoot any systematic fabrication-related issues. Sheet resistance test structures were the only electrical measurements made for material-related process control.

When issues with Pt to TaN contact through a via in PECVD oxide were identified (discussed in subsection 5.5.2), a variety of fabrication approaches were undertaken to help resolve the source of the problem. The initial integrated fabrication flow involved etching Pt a STS RIE tool. Minor systematic changes in PECVD oxide etching and platinum deposition-related processes did not help with the top layer Pt and bottom layer TaN thin films still not making a robust electrical contact through a via. As an alternative it was decided to increase Pt thickness and use lift-off process to pattern the evaporated Pt layer to enable a comparison between different processes for batches that used 100 and 200 nm-thick Pt layer. An interest in using a lift-off process in these batches was that dry etching process time for 200 nm platinum increased to around 80 minutes. A set of batches was fabricated using this approach and an example of the structures produced is shown in Figure 5.4.5. Full details of the fabrication process are provided in runsheet A.2. Slight horizontal misalignment is evident in structures produced on this wafer; however both metal layer features and vias were fabricated correctly.

After wafers with platinum produced by lift-off were characterised and the contact resistance was found to remain high it was decided to run a batch designed specifically for SEM measurements. A different pattern was selected in order to enable the measurement of multiple cross-sections of material stacks from a single sample. Cross-sections were planned to be formed by cleaving rather than dicing using an existing lithography test mask that had been designed by another PhD student [8]. As illustrated in Figure 5.4.6, two sets of 42 cross-sections of 10 μm lines and 17 cross-sections of 20 μm lines were available in horizontal direction

when the wafer was cleaved along the blue lines. Two processes were used – one was designed to produce a cross-section of patterned 200 nm TaN and another was designed to fabricate features in 250 nm PECVD oxide on a blanket 200 nm TaN layer. Again a detailed microfabrication process runsheet A.3 is provided in Appendix A.

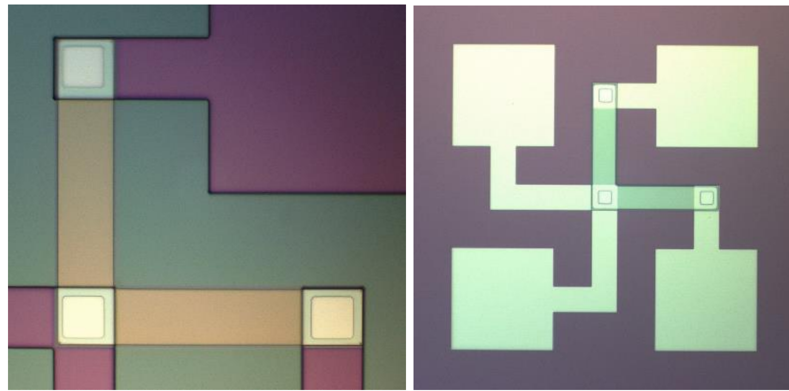

Figure 5.4.5: *Fabricated CBKR test structure with resist patterned for lift-off (left) and metal lifted off (right).*

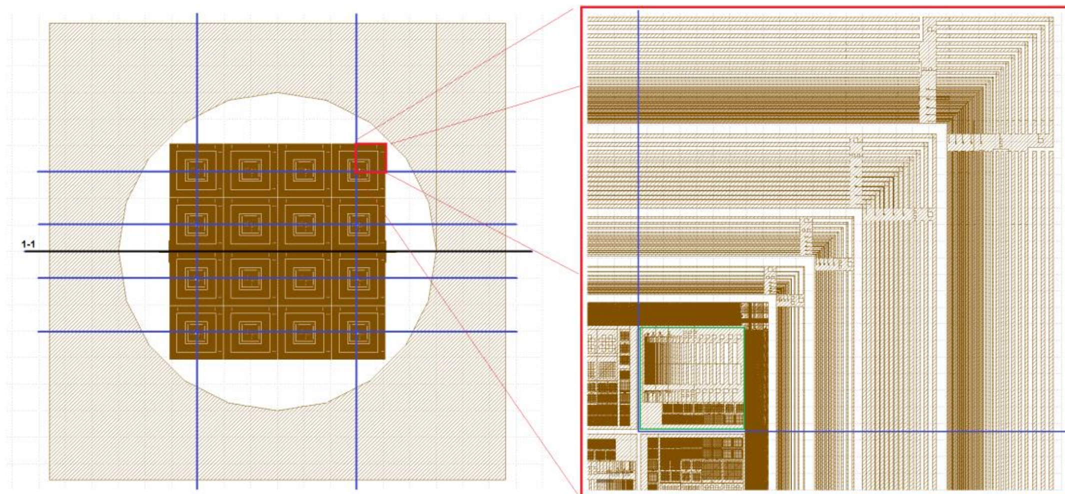

Figure 5.4.6: *Mask that was used to produce cross-section samples for SEM analysis: layout of a 4" mask (left) and magnified view of used lines (right).*

Prior to loading samples to the SEM chamber, samples were purposefully covered by sputtered gold to eliminate electrostatic charging of dielectric layers, such as silicon oxides (which are exposed during cross-section measurement), using a 5 minute process in an Edwards E306A coating system. A Hitachi 4700 FE-SEM

tool with a resolution of 12 Å was used to produce cross-section images and the results are shown in Figures 5.4.7 and 5.4.8.

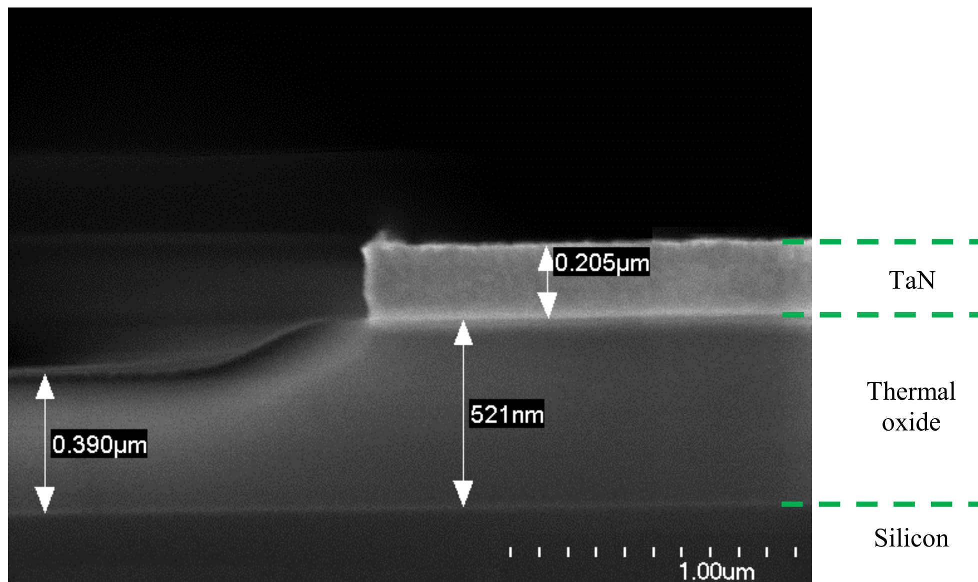

Figure 5.4.7: *Illustration of vertical TaN sidewall and over-etching depth into the thermal oxide: cross-section view from SEM tool.*

Figure 5.4.7 shows a well-developed TaN structure with vertical sidewall produced by CF_4/O_2 dry etching process. However, the over-etched depth is of the order of 100 nm, which is not acceptable in structures fabricated for this integrated process. As is evident from Fig. 5.4.8, the PECVD oxide CHF_3/Ar dry etching process also removes TaN and this cannot take on the role of an etch stop layer. On the other hand, any existing surface tantalum oxide layer will be removed in a process that produces the vias to TaN, which is beneficial to the integrated process. Another potentially critical issue which was noted during SEM measurements was poor antistatic gold layer coverage on PECVD oxide due to the surface contamination by SPR350 etching post-products. As resist removal in the barrel asher and gold deposition steps were carried out during the same process instances on the samples shown on Fig. 5.4.7 and 5.4.8, this issue was found to be strongly related to etching of dense PECVD oxide features.

Such a problem could not be observed using light microscope on fabricated 250 nm-thick PECVD oxide SEM samples or wafers that contained integrated sensor

devices and test structures, where a 500 nm PECVD oxide was used to create vias. The primary reasons for that were most probably the lower etching time and less dense etched features. A single-step oxide etching process on 500 nm-thick PECVD oxide performed with the pattern used for SEM analysis revealed the severity of the problem as shown in Figure 5.4.9.

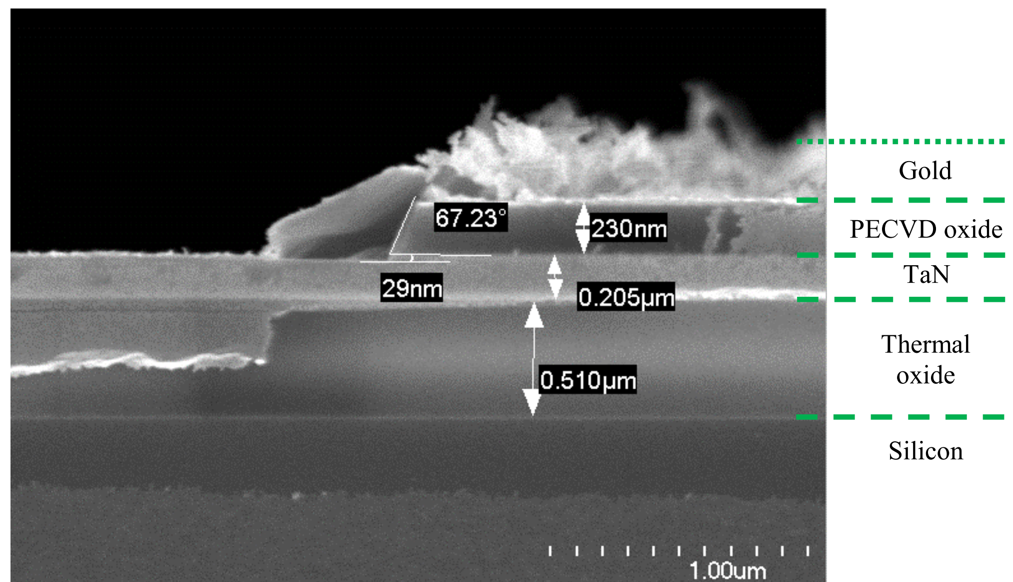

Figure 5.4.8: *Illustration of smooth angular LF SiO_2 sidewall and sputtered gold coverage failure: cross-section view from SEM tool.*

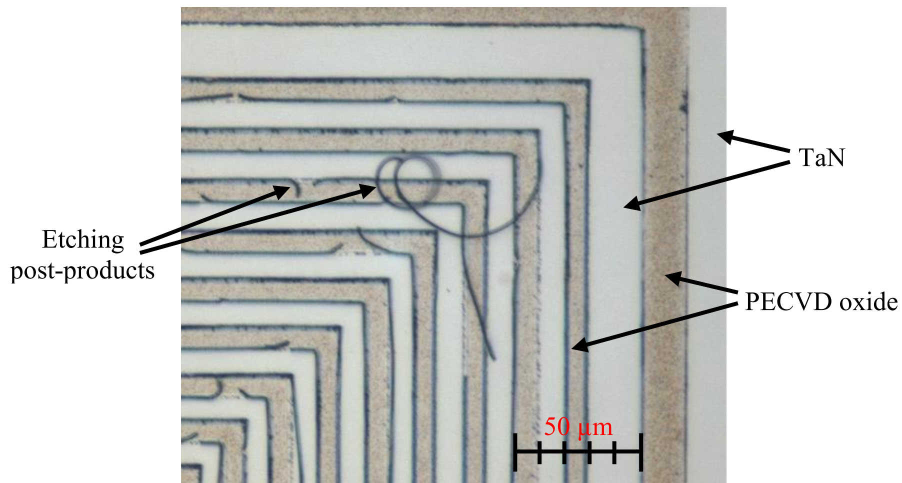

Figure 5.4.9: *Illustration of resist remainders after 60-minute barrel asher process on 500 nm-thick PECVD oxide sample: top-down view from light microscope.*

To make sure that a platinum coverage problem is not caused by PECVD oxide-related processing, another approach has been developed. This does not require any separation layer between TaN and Pt, with the Pt being patterned by lift-off. A 10 minute argon mill step was included as part of the TaN adhesion layer process, which was expected to remove up to 30 nm of underlying patterened TaN. As no via was present, all structures designed to have a different contact area were becoming essentially CKBR structures with 30×30 μm^2 overlap areas. At this point any break in electrical path would be related strictly to platinum step coverage because all other options were eliminated by process design. A sputtered platinum sample was processed in parallel using the same approach, which has enabled the comparison between yields produced by sputtered and evaporated platinum films of same designed thickness as the former is known from the literature sources to have better step coverage characteristics [9, 10]. The platinum film was not annealed in this process because samples with sputtered Pt were probably contaminated by gold in the Pt deposition tool. More processing details are presented in a runsheet A.4.

Following from measurements performed on fabricated samples, a significant redesign of the integrated process was considered because the source of problems was tracked down to the areas highlighted in green and yellow in Fig. 5.4.10, where the step in feature produced in Pt thin film layer takes place.

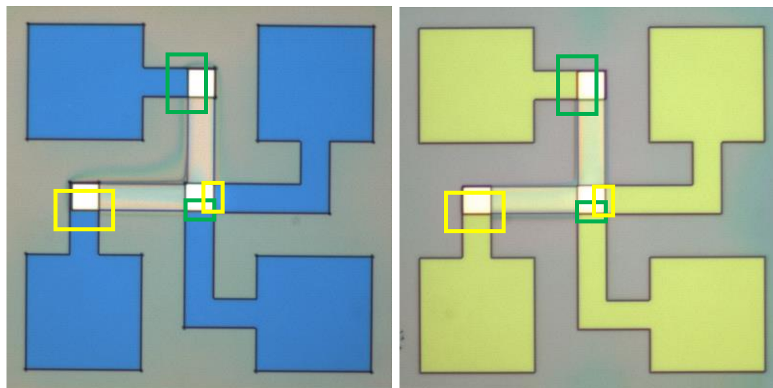

Figure 5.4.10: *CBKR test structures at the stage of resist patterning on wafer used with evaporated (left) and sputtered (right) thin film platinum. Green and yellow rectangles highlight vertical and horizontal current paths.*

5.5 Measurement setup and results

Measurements of fabricated batches related to first integrated design were focussed on determining the contact resistance, primarily between platinum and tantalum nitride layers. Therefore test setup and LabVIEW virtual instruments related to these measurements were based fundamentally on measurement of characteristics described in subsection 5.3.2.

5.5.1 Experimental setup

The test setup used to measure the CBKR test structures is shown in Fig. 5.5.1. A DC source/monitor (HP4142B) was used to provide 1 mA current input to the test structures and a digital multimeter (HP3458A) was used to measure the differential voltage produced by the current in the test structures over a ±2 V range. This provided a 2 μV measurement resolution, i.e. contact resistances of up to 2 kΩ could be measured with a 2 mΩ resolution. A Suss PA200 semi-automatic prober provided electrical contact to the test structures using a 2×4 probe card and heated chuck controlled by an A200 temperature controller. A switching matrix (HP4084B) was used to connect the necessary electrical voltage measurement and current supplies to the required probes. The temperature controlled chuck used a compressed air supply to enable cooling, which enabled the temperature to be set with 0.01 °C precision in a temperature range from 20 to 200 °C. Automatic control of all of these interfaces was implemented using a PC that was equipped with a camera attached to a light microscope.

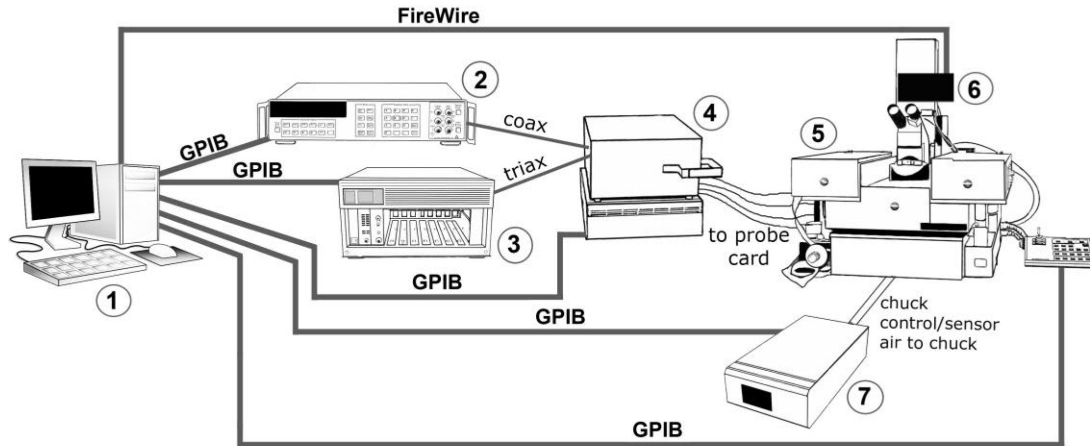

Figure 5.5.1: *Test setup used to measure integrated bridge circuits, sheet resistance and contact resistance test structures. 1: PC, 2: Digital multimeter, 3: DC SMU, 4: Switching matrix, 5: Semi-automatic prober, 6: FireWire camera, 7: Chuck temperature controller.*

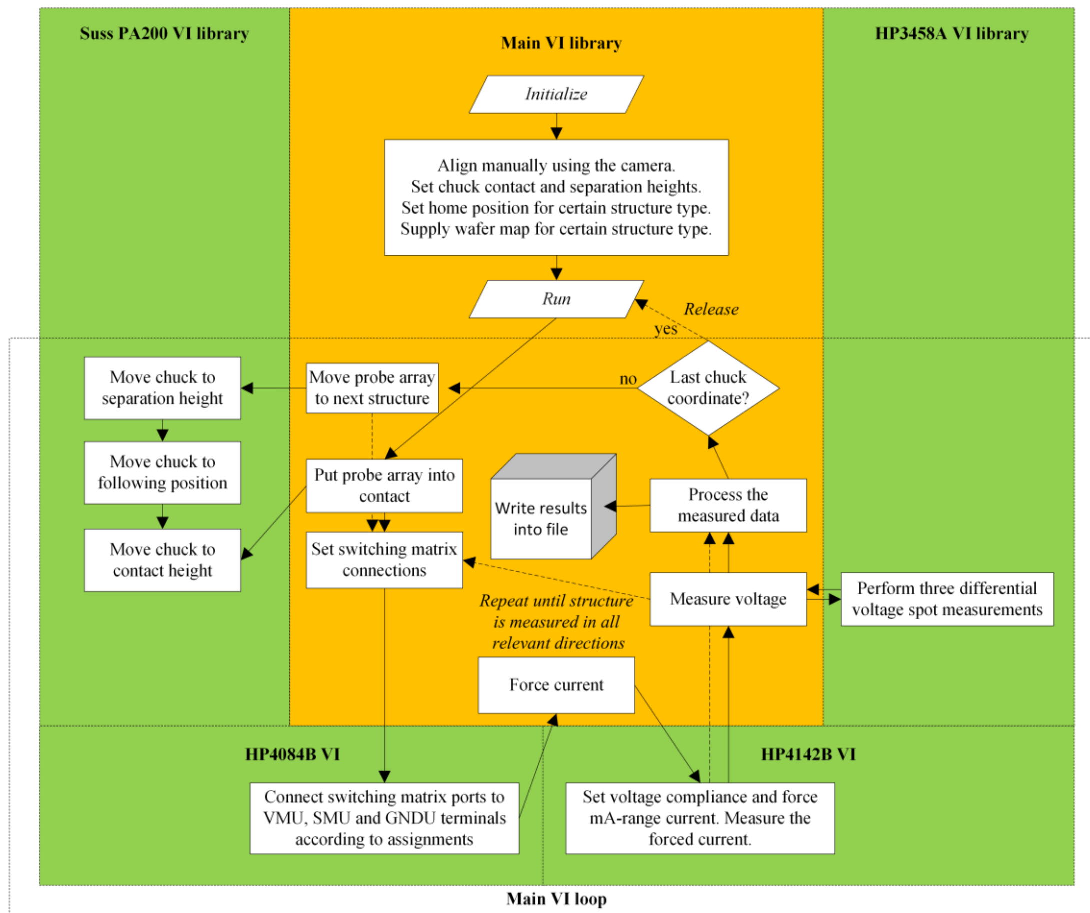

Figure 5.5.2: *Block diagram of VI functional flow.*

Initialization of each piece of equipment was undertaken before each measurement session to ensure that all devices were initialised to a known setting.

The LabVIEW code that performed contact resistance measurements was based on another PhD student's work that automated measurements across the whole wafer area [11]. All the contact resistance values were measured with the temperature controlled between of 24.95 and 25.05 °C. The virtual instrument flow is shown as a block diagram in Figure 5.5.2.

5.5.2 Test structure measurement results

The initial contact test structure measurements have shown an extremely poor yield of contact resistance structures (0.5%) when fabricated as part of an integrated process, or when fabricated using an initial process detailed in runsheet A.2, that connects layers of Pt and TaN. The yield of contact resistance structures was as low as 1 or 2 partially working structures out of 816 with current passing only in one path indicating contact resistance values higher 2 kΩ. With 10^{-3} A forced and 2 V compliance set, current measured was at noise level of 2×10^{-8} to 5×10^{-7} A.

The second batch of wafers with platinum to TaN CBKR test structures was produced using a lift-off process. The resulting measurements are presented in Fig. 5.5.3 and Fig. 5.5.4. The first set of results was measured on samples with annealed Pt and the second set was produced by samples which have not been annealed. A summary of the measured data set is provided in Table 5.5.1.

Table 5.5.1 *Summary of measured contact resistance values for different thickness of evaporated platinum according to designed contact areas.*

Sample	*Layers in contact*	*Mask contact area, μm²*	*Minimum value, Ω*	*Median value, Ω*	*Maximum value, Ω*	*Mean value, Ω*
Non-annealed	*100 nm Pt to 200 nm TaN*	*20×20*	13.69	66.22	153.94	65.50
		15×15	10.76	88.20	271.63	110.58
		10×10	2.60	69.69	224.59	89.21
Annealed	*100 nm Pt to 200 nm TaN*	*20×20*	3.60	72.82	160.54	78.03
		15×15	0.75	87.21	194.63	84.19
		10×10	1.99	16.00	757.50	84.88
Non-annealed	*200 nm Pt to 200 nm TaN*	*20×20*	5.19	22.32	192.00	67.67
		15×15	1.07	21.10	263.00	67.19
		10×10	4.86	55.79	243.35	84.65

As evident from Fig. 5.5.3 and Table 5.5.1, the annealed samples fabricated using the process described in section 5.4 and detailed in Appendix B.2 had average measured Pt to TaN contact resistance value of the order of 80 Ω for contact areas of 10×10 to 20×20 μm^2. It can be observed that the range of the measured results increases as the contact area reduces. The median values in each data set were close to average values with the range increasing as the contact area decreased. However, the minimum, median, mean and maximum values of measured resistance were larger for 15×15 μm^2 structures than those with contact area 10×10 μm^2. It is therefore suspected that the measured contact resistance in Fig. 5.5.3 is not related to the contact area or the specific contact resistance between two layers, but is most likely related to the integrity of platinum layer around the vias caused by poor step coverage of the evaporated platinum thin film.

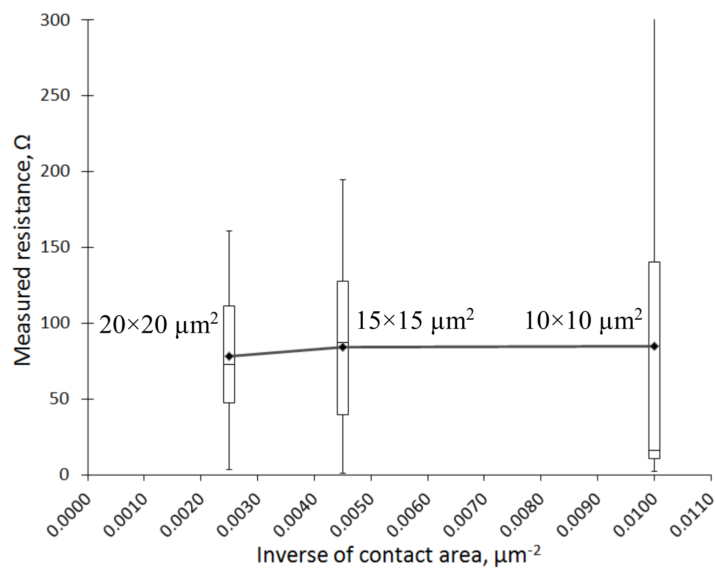

Figure 5.5.3: *Measured contact resistance against inverse of designed contact area for annealed 100 nm Pt sample.*

Contact resistance test structures fabricated using 200 nm platinum layer had mean measured value of the order of 70 Ω as depicted in Figure 5.5.4. These results are marginally better than the sample that used 100 nm Pt (refer to Fig. 5.5.3).

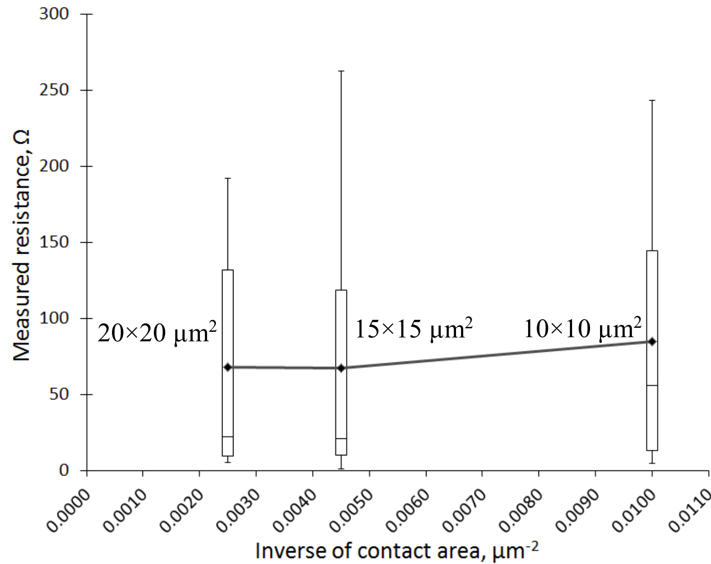

Figure 5.5.4: *Measured contact resistance against inverse of designed contact area for non-annealed 200 nm Pt sample.*

A process where 200 nm Pt was lifted off and 200 nm TaN was etched using a process detailed in runsheet A.5 (Appendix A) produced functioning contact resistance test structures. Contact resistance results measured on 200 nm platinum sample are shown in Fig. 5.5.5 and again the contact resistance does not scale with area to produce a linear dependence with the inverse of contact area as it is expected for contacts between a conductive metal compound (TaN) and a metal (Pt).

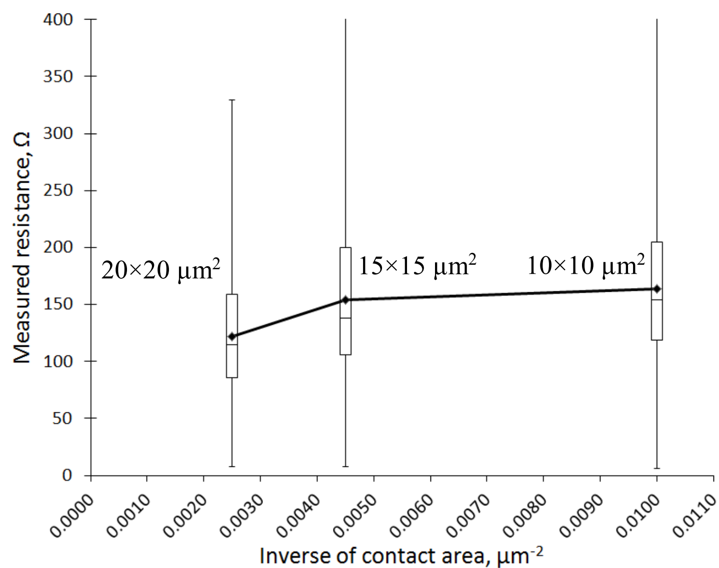

Figure 5.5.5: *Measured contact resistance against inverse of designed contact area for non-annealed 200 nm Pt sample fabricated by improved lift-off process.*

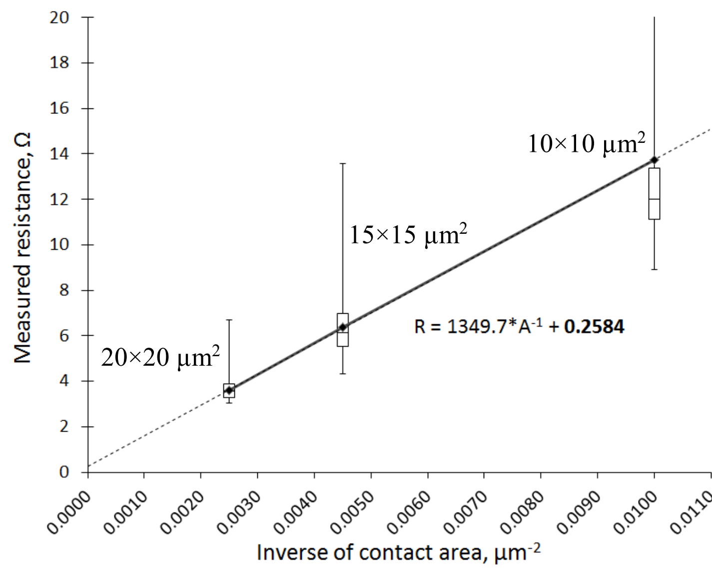

Figure 5.5.6: *Measured contact resistance against inverse of designed contact area for non-annealed 200 nm TaN sample fabricated by improved etching process.*

The results of contact resistance test structures fabricated to characterise a 200 nm-thick tantalum nitride layer contacting another TaN layer are shown in Fig. 5.5.6, and these scale with area as expected. The average contact resistance extrapolated at $A \to \infty$ was 258 mΩ while specific contact resistance was 1349.7 $\Omega \cdot \mu m^2$.

5.5.3 Conclusions

Fabricated contact resistance test structures provide information on the contact resistance between platinum and tantalum nitride thin films and the integrity of platinum layer that covers the sidewalls of vias, which make a contact with the bottom tantalum nitride film. Due to poor step coverage around half the wafers in batches related to evaporated platinum failed to produce a measurable contact resistance to TaN.

Increasing platinum thickness marginally improved the platinum step coverage around vias. However, the problem of high measured values still persisted. Average

measured value of contact resistance between 100/200 nm Pt layer to TaN was of the order of 100 Ω for contact areas between 10×10 and 20×20 μm^2.

Test structures fabricated to measure the contact resistance between two layers of sputtered 200-nm thick TaN functioned as expected with measured average resistances extrapolated for infinite contact area of 258 mΩ and a specific contact resistance of 1349.7 $\Omega \cdot \mu m^2$.

5.6 Temperature sensitive layer improvement options

As a result of the above investigations there was a clear need to improve the contact between temperature sensitive material and the low TCR tantalum nitride thin film. Two options were considered to improve the step coverage, one of which was using a thicker (200 – 400 nm) evaporated platinum thin film.

Sputtered platinum (200 nm) was also evaluated as sputtered films tend to exhibit better step coverage compared with evaporation [9, 10]. Unfortunately, the sputtering tool located in the School of Physics was set up to be used with materials such as gold, therefore platinum deposited using this tool could not be further processed in the cleanroom as it was potentially contaminated by gold. The TCR of a 200 nm platinum sputtered film was measured and as shown in Fig. 5.6.1 is of the order of 1600 ppm $°C^{-1}$.

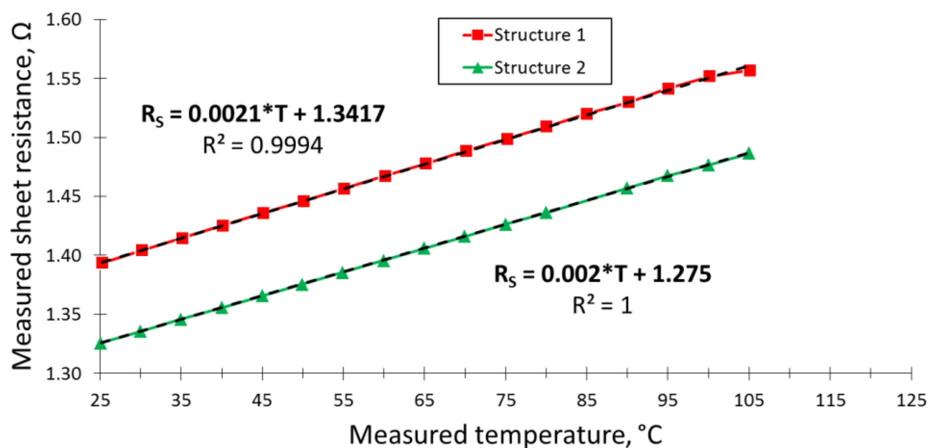

Figure 5.6.1: *TCR measurement of 200-nm thick sputtered platinum film.*

From (4.9):

$$\alpha_1 = \frac{2.086\times10^{-3}}{1.34166} \approx 1555.0\left[\frac{ppm}{°C}\right]; \qquad \alpha_2 = \frac{2.018\times10^{-3}}{1.27499} \approx 1582.7\left[\frac{ppm}{°C}\right] \tag{5.11}$$

A comparison of contact resistance structure yield and measurement results was performed by depositing 200 nm thick evaporated and sputtered Pt and, as the sputtered platinum sample could not be annealed, neither was the evaporated sample. At this stage the oxide layer between TaN and Pt had been dispensed with, which left no via in the structure and the latter was essentially becoming an overlap between 30×30 μm^2 corner sheets in Pt and TaN layer with actual contact area defined by the alignment between the two metal layers. Fig. 5.6.2 shows the measured contact resistance of sputtered Pt and TaN while Fig. 5.6.3 depicts the measured contact resistance between evaporated Pt and TaN. Inspection of Figures 5.6.2 and 5.6.3 indicated that sputtered platinum has a much lower median measured resistance (~20 Ω) than evaporated platinum test structures (~150 Ω).

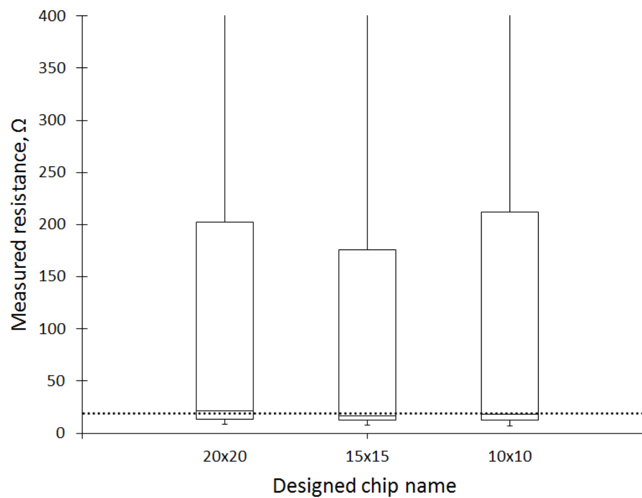

Figure 5.6.2: *Measured resistance for different contact resistance test structures between 200 nm sputtered platinum layer and TaN.*

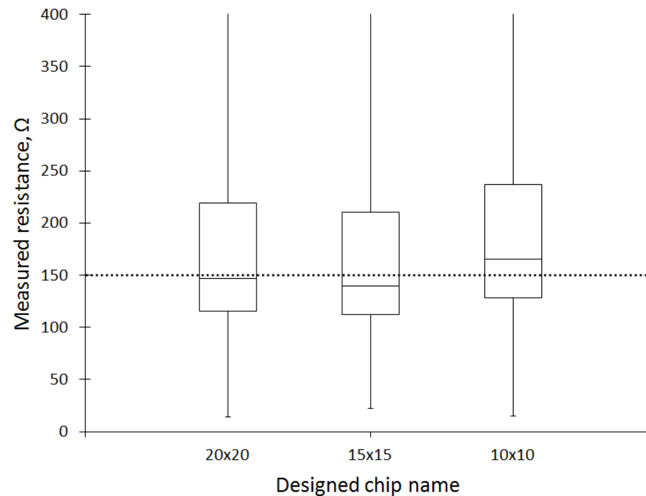

Figure 5.6.3: *Measured resistance for different contact resistance test structures between 200 nm evaporated platinum layer and TaN.*

These results led to conclusion that available sputtering tool was producing better contacts between platinum and tantalum nitride thin films as determined by the median of measured resistance values being of the same order with minimum values of those produced by evaporation tool. However, it would not provide sufficient uniformity to produce sensor devices with equal effect of parasitic resistance due to step coverage, or enable completing the fabrication of PECVD and aluminium layers and finishing the devices in the cleanroom environment.

5.7 Conclusions

A hybrid bridge was built using discrete microfabricated element chips that produced a circuit with a pair of parasitic interconnect elements (~0.1 Ω) in each bridge arm. The sensitivity of this circuit measured in a range of 25 to 100 °C was a reasonably high value of 844 $\mu V \cdot °C^{-1}$. This sensitivity was mainly determined by the TaN and Pt resistor values and proportions chosen for demonstration and TCR values of the Pt temperature sensitive elements (1340 ppm $°C^{-1}$). The TaN balancing resistors were fabricated with TCR close to zero and the estimated element of resistance value mismatch was less than 0.1%.

Development of an integrated bridge at this stage was focussed on contact resistance test structure measurements due to issues with the connection between platinum thin film and TaN for an integrated bridge circuit. The specific contact resistance between Pt and TaN could not be estimated probably due to poor step coverage of the layer of platinum around contacts down to the TaN (as illustrated in Fig. 5.4.10). This was indicated by the extremely poor yield of some wafers containing contact resistance structures and significant mismatch of measured resistance in different current paths in working structures.

One potential problem with the etching processes was identified by SEM measurements where a denser layout was to be patterned. A burnt photoresist residue remained on PECVD oxide after resist removal step, which could be addressed by a reduction in the etching time and also employing multiple runs with cooling times interspersed. This approach was applied to both TaN and PECVD etch processes as overetching into underlying layers by both processes was evident.

In an attempt to eliminate any negative effect of PECVD oxide-related processing on contact between Pt and TaN films the oxide layer was dispensed with which appeared to finally solve the test structure yield issue. As a result, Pt patterns were produced by lift-off directly on 200 nm-thick TaN features instead of making contact through vias in 500 nm-thick PECVD oxide. Such changes in process, on the other hand, did not improve measured contact resistance value which became higher than 100 Ω on average for evaporated platinum.

Possible approaches to improve contact between TaN and temperature sensitive thin films were identified and discussed. Among alternative deposition processes using thicker evaporated platinum film was finally considered. Performance of sputtered platinum in contact resistance structures was found to be better than that of evaporated platinum as demonstrated by measurements of the structures, where PECVD oxide layer was not used and Pt features were produced by lift-off. Median measured contact resistance values of sputtered and evaporated 200 nm-thick platinum films were around 20 Ω and 150 Ω respectively for the same data set size.

References

[1] "INA333 Micro-Power (50µA), Zero-Drift, Rail-to-Rail Out Instrumentation Amplifier," ed. http://www.ti.com/lit/ds/sbos445c/sbos445c.pdf: Texas Instruments, 2008 [Revised 2015].

[2] J. V. Nicholas and D. R. White, "Thermocouple Thermometry," in *Traceable Temperatures: An Introduction to Temperature Measurement and Calibration*, 2nd ed., Chichester, UK: John Wiley & Sons, 2001, pp. 295-342.

[3] E. Nash. (1998) A practical review of common mode and instrumentation amplifiers. *Sensors Magazine (July 1998)*. 26-33.

[4] "Applications and Design of Thin Film Resistors," ed. http://www.vishay.com/docs/61083/appsdes.pdf: Vishay Electro-Films, 2004.

[5] D. K. Schroder, "Contact Resistance and Schottky Barriers," in *Semiconductor Material and Device Characterization*, 3rd ed., Hoboken, USA: Wiley-IEEE Press, 2006, pp. 127-184.

[6] M. Ono, A. Nishiyama, and A. Toriumi, "A simple approach to understanding measurement errors in the cross-bridge Kelvin resistor and a new pattern for measurements of specific contact resistivity," *Solid-State Electronics,* vol. 46, no. 9, pp. 1325-1331, 2002.

[7] P. Zhang and Y. Y. Lau, "Scaling laws for electrical contact resistance with dissimilar materials," *Journal of Applied Physics,* vol. 108, no. 4, p. 044914, 2010.

[8] R. Walker, "Characterisation and integration of materials and processes for planar spiral microinductors with permalloy cores," Doctor of Philosophy Dissertation, University of Edinburgh, 2015.

[9] M. J. Madou, "Physical and Chemical Vapor Deposition - Thin Film Properties and Surface Micromachining," in *Manufacturing Techniques for Microfabrication and Nanotechnology*, 3rd ed., (Fundamentals of Microfabrication and Nanotechnology, no. 2), Boca Raton, USA: CRC Press, 2011, pp. 391-508.

[10] S. Franssila, "Thin-Film Materials and Processes," in *Introduction to Microfabrication*, Chichester, UK: John Wiley & Sons 2004, pp. 47-65.

[11] J. Murray, "The electrodeposition and characterisation of thin films for the fabrication of microinductors," Doctor of Philosophy Dissertation, University of Edinburgh, 2014.

Chapter 6 Integrated bridge improvement and results

6.1 Introduction

Developments in Chapter 5 identified problems related to the step coverage of platinum layer around the contact area. The fabrication process flow and parameters were modified to: (a) decrease the effect of the latter on the resultant integrity of the fabricated sensor devices, (b) to improve the uniformity and selectivity of etch processes and, finally, (c) integrate the two fabrication processes of functional layers to ensure compatibility with one another. As a result, a relationship between the integrity of the platinum layer and the resultant sensor performance in the temperature range of up to 200 °C was demonstrated.

This chapter will describe: (a) further improvements in the design of an integrated temperature transducer layout and process flow, (b) the design of test structures to study step coverage and contact resistance effects on parasitic resistance introduced to the integrated transducer circuit and (c) related improvements of measurement setup. Resistive test structures produced in two conductive layers and temperature sensitive circuits fabricated using the novel integrated process were measured and these results have been validated and analysed. This enabled measured resistance characteristics to identify apparent microfabrication effects and non-idealities.

6.2 Design improvements

Improvements in temperature transducer element design, test structure versatility and selection, and further development of common approaches to both microfabrication strategy and test design are described in following sections.

6.2.1 Improvement of sensor design elements

The design of the temperature transducer was improved based on the conclusions drawn in Chapter 5. Firstly, PECVD oxide layer between TaN and Pt was removed in the new design, which has decreased the thickness of material that Pt had to cover from 500 nm (PECVD oxide) to 200 nm (TaN). The 30×30 μm^2 contact through via elements were replaced with a 40×40 μm^2 overlap areas produced by direct contact of TaN and Pt thin films. Some step coverage related issues could still result, however this layout of Pt overlapped the TaN area with at least 5 µm and 10 µm alignment margins along X and Y axes to help address this. As a result, the TaN contact pad coverage perimeter increased from 120 µm to 170 µm. Figure 6.2.1 illustrates the layout improvements in the temperature sensor devices, where the area of most significant improvement is highlighted.

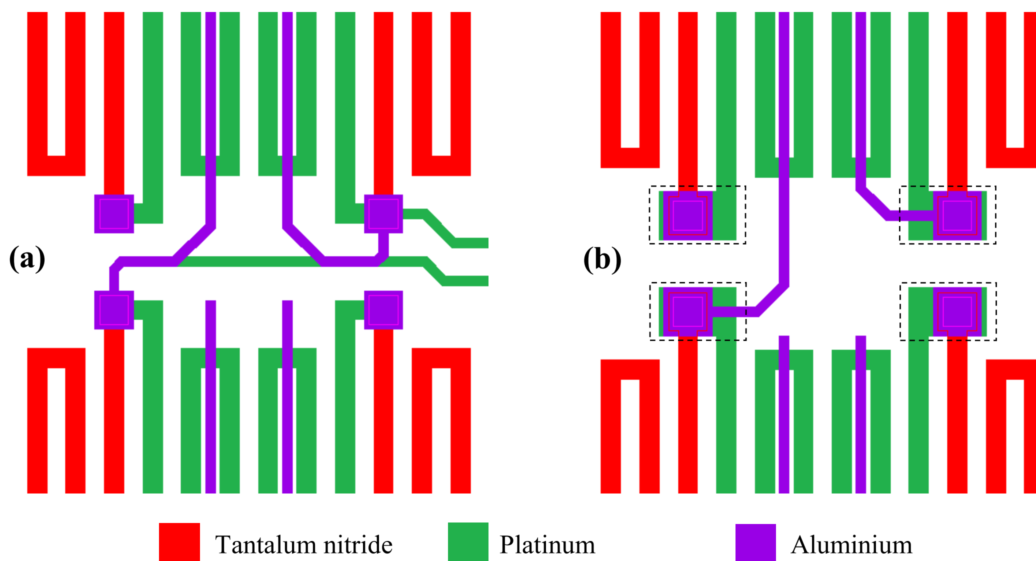

Figure 6.2.1: *Illustration of layout improvements around contact areas in the integrated bridge: (a) initial design revision and (b) improved design.*

The standalone sensor design was not much affected as illustrated on Figure 6.2.2, where connections to instrumentation amplifier terminals were moved to the Al layer. Only Al layer was now electrically separated from TaN and Pt by the PECVD oxide layer. The amplified/non-amplified differential output could now be measured using the instrumentation amplifier output terminal while controlling the gain and reference voltages accordingly using terminals V_{SEL} and V_{REF}.

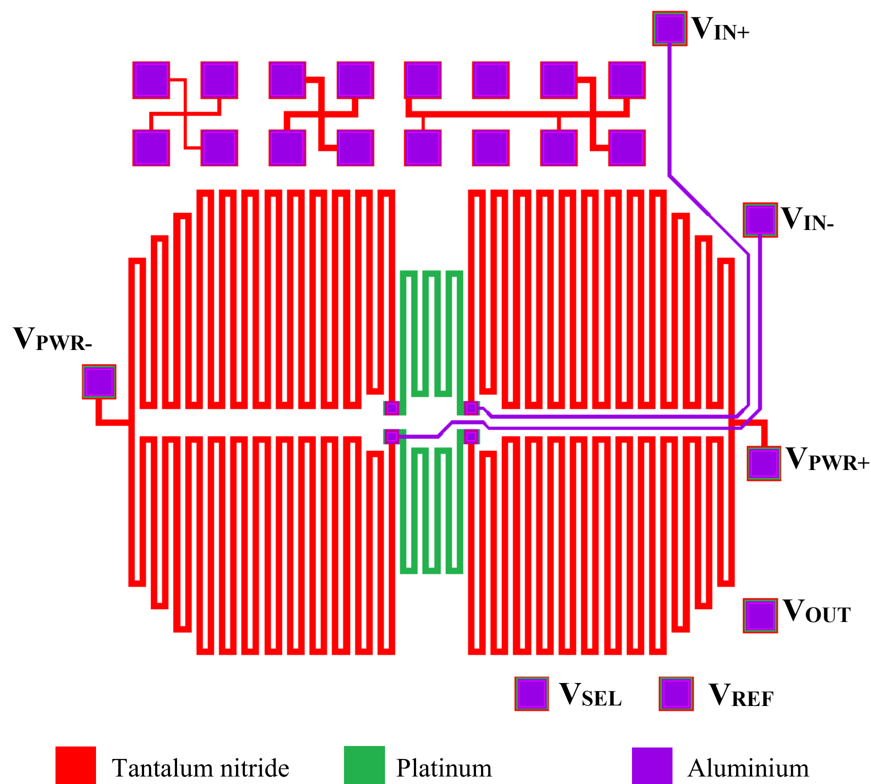

Figure 6.2.2: *Improved temperature transducer bridge design to be integrated with SiC electronics and used as a standalone sensor.*

The sensor devices to be measured have been improved accordingly by creating a single interconnect strategy, which now uses only aluminium as an interconnect metal. TaN and Pt serpentine lengths were rebalanced. However, the total values for each resistor have not been changed. Probe pads connected to tap to the bridge output have now been connected using vertical tracks and are also extended to connect to the input terminals of the instrumentation amplifier. The improved design for the device with external connections is shown in Fig. 6.2.3.

Platinum sheet resistance value in devices fabricated using the revised design were expected to be <3 Ω/□ as platinum film thicknesses of more than 200 nm have been considered. The geometrical parameters of the resistive elements were practically unchanged and the resistance values detailed in Table 5.3.1 were still correct for 200 nm-thick Pt films, and hence device labels were kept to reflect the designed ratio for this particular thickness.

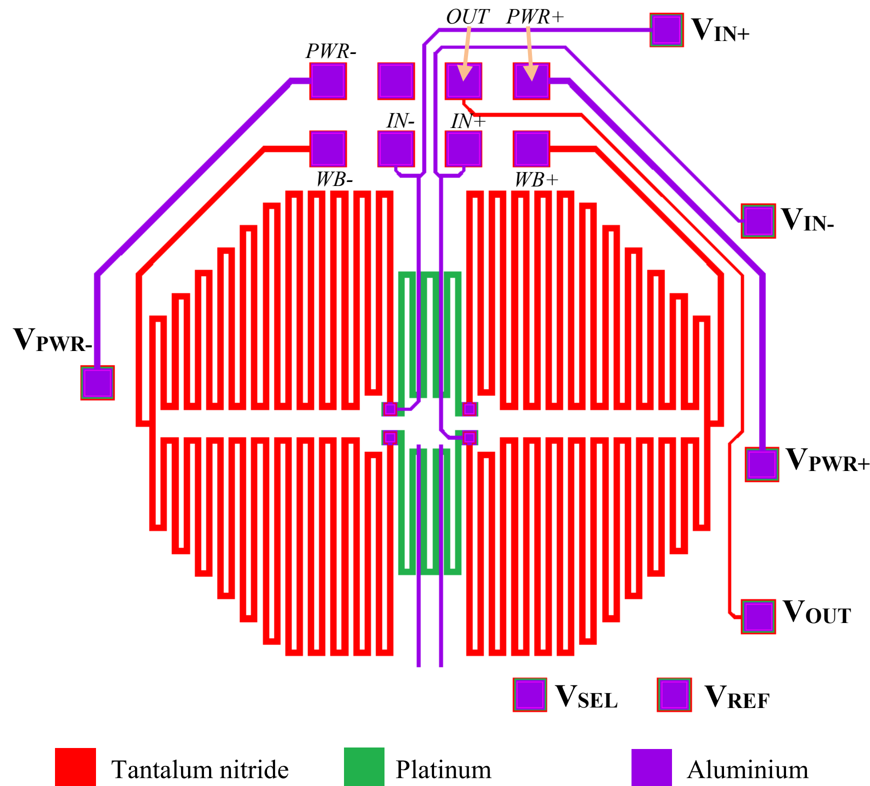

Figure 6.2.3: *Designed bridge to be integrated with SiC electronics and measured using the probe array.*

6.2.2 Test structures to characterize additional resistive elements

The resistance of tracks due to step coverage around areas of contact between platinum and tantalum nitride films will increase [1]. Test structure chips described in the revised design have been improved with a set of structures that enable the measurement of contact resistance between two thin film materials without using vias. The step resistance test structure is a new variation of a bridge structure, which consists of a track produced in the upper conducting layer (green, Pt) that crosses

over a series of mesas patterned in the bottom electrically conductive layer (red, TaN), as illustrated in Figure 6.2.4(a). Mesa features introduce one or more steps to evaporated platinum layer as indicated in Figure 6.2.4(b). The resistance of different track sections 1 to 5 is characterized by track length (which is 120 µm for all sections), overall overlap length between TaN mesa and Pt track, and by the number of steps that the track passes across. These parameters are summarized in Table 6.2.1 according to numbered sections in Figure 6.2.4(a).

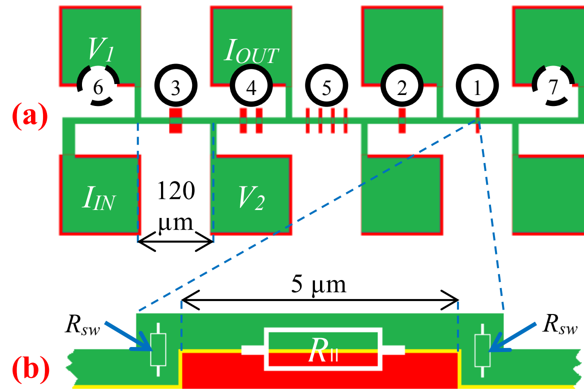

Figure 6.2.4: *(a) Bridge resistor test structure used to measure step coverage resistance. Green: Pt upper conducting layer; yellow: TaN adhesion layer; red: TaN lower conducting layer. (b) Cross-section through the resistive track indicating the resistive elements introduced by the step (not to scale).*

Table 6.2.1 *Design parameters for different mesa structures.*

Structure number	*Track length L_m, µm*	*Mesa overlap segments*	*Mesa overlap length L_{TS}, µm*	*Step count*
1	*120*	*1×5 µm*	5	2
2		*1×10 µm*	10	
3		*1×20 µm*	20	
4		*2×10 µm*		4
5		*4×5 µm*		8

The voltage measured between two adjacent voltage taps (for example, V_1 and V_2 in Fig. 6.2.4(a)) can be expressed as:

$$V_m = I_m\left(\frac{L_m - L_{TS}}{W} R_{S(Pt)} + R_{TS}\right), \tag{6.1}$$

where I_m is the applied current flowing from the pads I_{IN} to I_{OUT}, L_m is the track section length (120 µm for this design), L_{TS} is the lower layer mesa length, and W is

the upper layer track width (10 µm for this design), given that sheet resistance $R_{S(Pt)}$ is uniform across the whole track. R_{TS} is the resistance of section where the Pt track crosses the TaN mesa, which consists of step resistance elements $2R_{sw}$ in series with the parallel resistance of the upper and lower layers $R_{||}$ (refer to Fig. 6.2.4(b)). Measurement of individual bridge test structures with different numbers and widths of lower layer features enables the effect of individual steps and conductive layers overlaps on track resistance to be estimated.

A variation on a transmission line (or transfer length) model (TLM) test structure was designed to measure the contact resistance between two films. Conventional contact front resistance (CFR) test structure had to be modified in order to allow measurement using a probe card array [2]. This design used test structure elements with 20, 40, 80 and 80, 160, 320 µm contact spacing L to the 10 µm wide (W) bottom layer (red, TaN) track as shown in Figure 6.2.5. The 10 µm-wide taps in the upper layer (green, Pt) were used to force current and measure voltage in a set of four-terminal measurements.

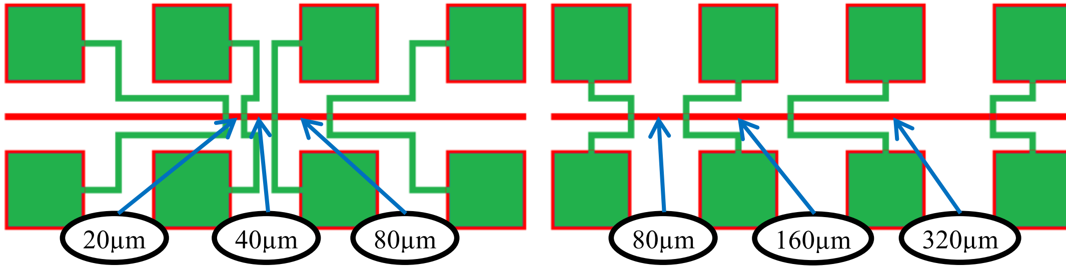

Figure 6.2.5: *Modified TLM test structures used to measure contact resistance with contact spacing values of (left) 20-80 µm and (right) 80-320 µm.*

The voltage measured between two taps is given by:

$$V_m = I_m \left(\frac{L}{W} R_{S(TaN)} + 2R_C \right) \tag{6.2}$$

where I_m is the current forced, $R_{S(TaN)}$ is the TaN layer sheet resistance and R_C is the contact resistance. The measured voltage inevitably includes voltage errors produced by the current spreading in the contact as identified in the literature [2-4]. This error had a minimal effect on the constant part of the equation (contact resistance term R_C) as it was assumed that it was constant for every single contact in the test structure

(across 150×10 μm area). Multiple Kelvin-type measurements using different paths and directions of current facilitate more precise measurement for every single contact spacing L structure element whereas multiple different contact spacing measurements enabled the estimation of contact resistance for a designed contact area of 10×10 μm^2.

Two more parameters can be estimated using the data sets from these test structures:

- The electrical linewidth (W) of the tantalum nitride track, which will be most accurate for the track section of L = 80 μm.

$$W = \frac{L}{R} R_{S(TaN)} \tag{6.3}$$

- The sheet resistance of the tantalum nitride track of known width W

$$R_{S(TaN)} = \frac{\Delta R_m}{\Delta L} W \tag{6.4}$$

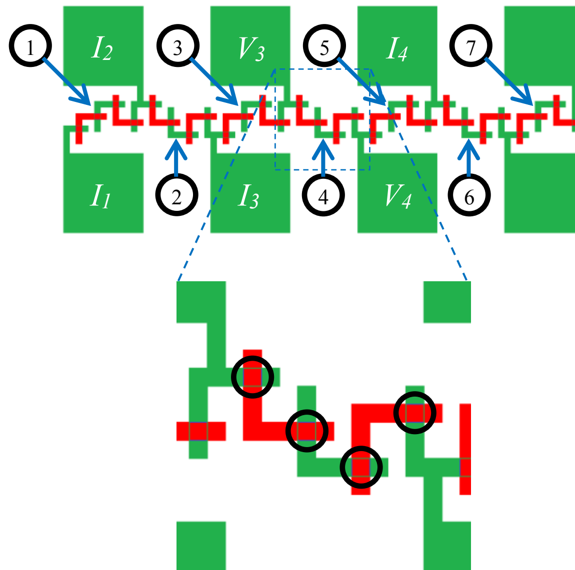

Figure 6.2.6: *Contact chain test structure used to measure integrity of multiple contacts between two layers. Numbers indicate separate contact chains.*

The integrity of platinum layer was also evaluated using contact chain structures, which consisted of a set of four 10×10 μm^2 contacts and four 10 μm-wide step resistance elements between each pair of pads, as shown in Fig. 6.2.6. There are

seven chains with 2 to 6 being configured for a four terminal Kelvin connection. The following two measurements were made to characterise the fabricated test structure:

- In order to investigate the continuity of the fabricated elements current was forced through a set of short conductive paths, for example I_1 to I_2 for segment 1 and I_2 to I_3 for segment 2 etc. as indicated on Fig. 6.2.6, and voltage compliance was checked.
- In order to measure the contact chain resistance value current was forced (for example, between I_3 and I_4) in a set of Kelvin type measurements, where a differential voltage across short conductive paths (V_3 to V_4) was measured. The resistance value of segment 4 can then be calculated using:

$$R_4 = \frac{V_3 - V_4}{I_3} \tag{6.5}$$

The final set of test structures were different variations on a CBKR structure. A total of twelve test structures with contact sizes of 10×10, 15×15 and 20×20 μm^2 were used to determine the contact resistance between Al and Pt, and Al and TaN contacts. The fabrication process involved a single PECVD oxide layer between aluminium and other conducting thin films. The designed W and δ values were identical to the previous design.

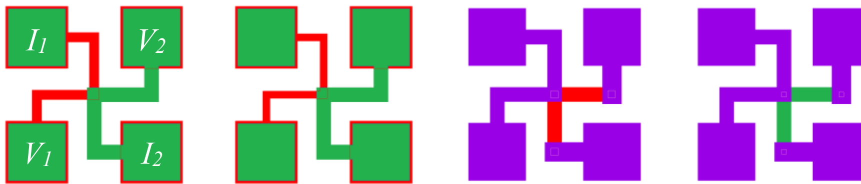

Figure 6.2.7: *Layout of cross-bridge Kelvin contact resistance test structures: Left – between platinum and tantalum nitride layers; Right – between Al and tantalum nitride, and Al and platinum layers.*

The contact resistance test structures between Pt and TaN layers had no dielectric via, as illustrated in Fig. 6.2.7 (left), which meant that contact area is determined by bottom layer track width (W = 15 and 20 μm) and alignment. On the other hand, such a structure uses a single contact in each conductive path combination instead of two, which improves the voltage compliance conditions. The final contact area in these

structures will clearly vary due to inevitable layer misalignment. However, an XY mirror copy of each structure existed on each of test structure chips to compensate for this effect. The contact resistance value measured in a particular direction determined by using:

$$R_{C1} = \frac{V_1 - V_2}{I_2} \tag{6.6}$$

and the average of four measurements was used to calculate the contact resistance for the fabricated test structure.

6.2.3 Optimization of microfabrication processes

Parameters related to microfabrication processes were optimised based upon the electrical and microstructural measurements described in Chapter 5. The most obvious change in the fabrication flow was that PECVD was dispensed with and the required design modifications were described in the preceding two subsections.

Following from this, the tantalum nitride and platinum thin films were now in direct contact one with another, and a single annealing step for 6 hours at 600 °C was performed after both thin films had been patterned. This decreased the complete fabrication flow duration by at least one day, which also resulted in the CMOS circuit experiencing a lower thermal budget when temperature transducer is fabricated by post-processing. Another aspect worth mentioning is the initial etching the PECVD oxide affected features produced in TaN layer in areas where vias were required.

To further improve etch uniformity and decrease the chance of over-heating the photoresist in a single etching step both the tantalum nitride and PECVD oxide processes were split into two steps. For the second step the wafers were rotated by 180°. The tantalum nitride etching total process duration was decreased to 20 minutes with 5 minute follow-up process, if necessary. Platinum patterning was now carried out using a newly developed AZ2070 lift-off photoresist process that allowed the use a negative photoresist instead of an image reversal resist. Finally, the aluminium etch time was decreased significantly to 15 minutes, which further reduced the processing time required to fabricate the integrated sensor devices.

6.2.4 Test design improvements

Separate LabVIEW VI libraries were created in order to measure the sensor devices and test structures. One supplied a voltage, measured current and differential voltage output across a temperature range. The other forced a current and measured the voltage in a four-terminal Kelvin measurement with an ability to perform such measurements at different temperatures. The measurement setup used is shown in Figure 5.5.1.

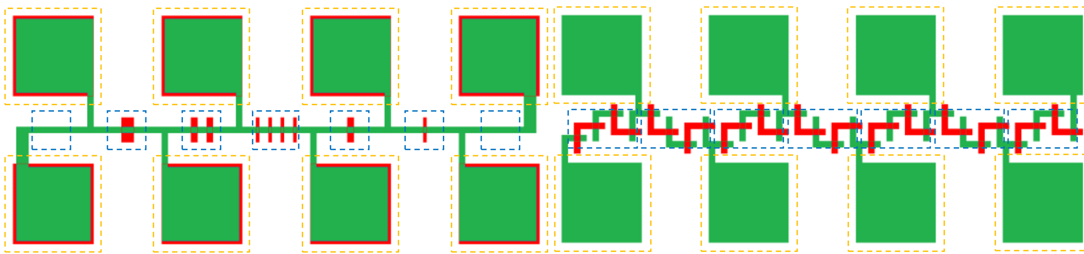

Figure 6.2.8: *Integrity check blocks for step resistance (left) and contact chain test structures (right).*

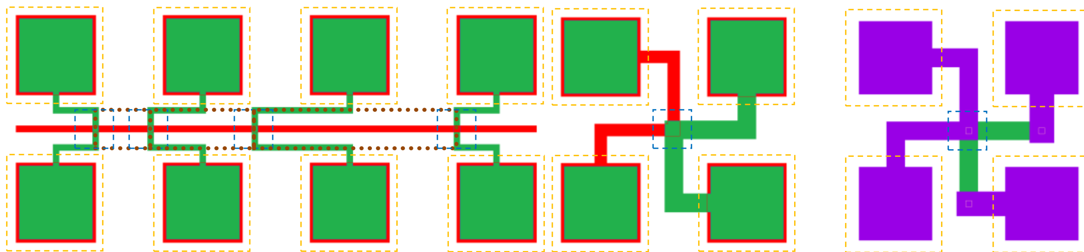

Figure 6.2.9: *Integrity check blocks for TLM (left) and CBKR test structures (right).*

The test structure measurement functions were enhanced to automatically analyse the results in the course of a measurement session and store information on the measured structures as both measured numerical and graphic data in binary format. The latter data reflected whether the measurement was reproducible (5%) and whether measured current was within accepted (1%) range using a 1 mA set current and 13 V compliance. This functionality enabled working test structure blocks as illustrated in Fig. 6.2.8 and 6.2.9 to be distinguished from blocks where resistance was higher than 13 kΩ, producing data in a format shown in Fig. 6.2.10.

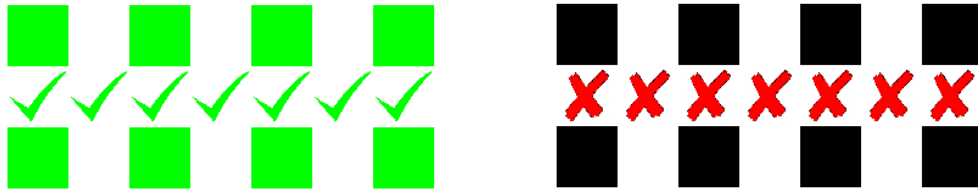

Figure 6.2.10: *Example integrity check for blocks with all positive (left) and all negative results (right).*

The test structure measurement was not completely automated with the chuck being manually controlled to navigate between different test structures using a separate LabVIEW VI user interface. All multilayer test structure resistance values were measured at a temperature between 24.95 and 25.05 °C. The virtual instrument measurement flow block diagram is depicted in Figure 6.2.11.

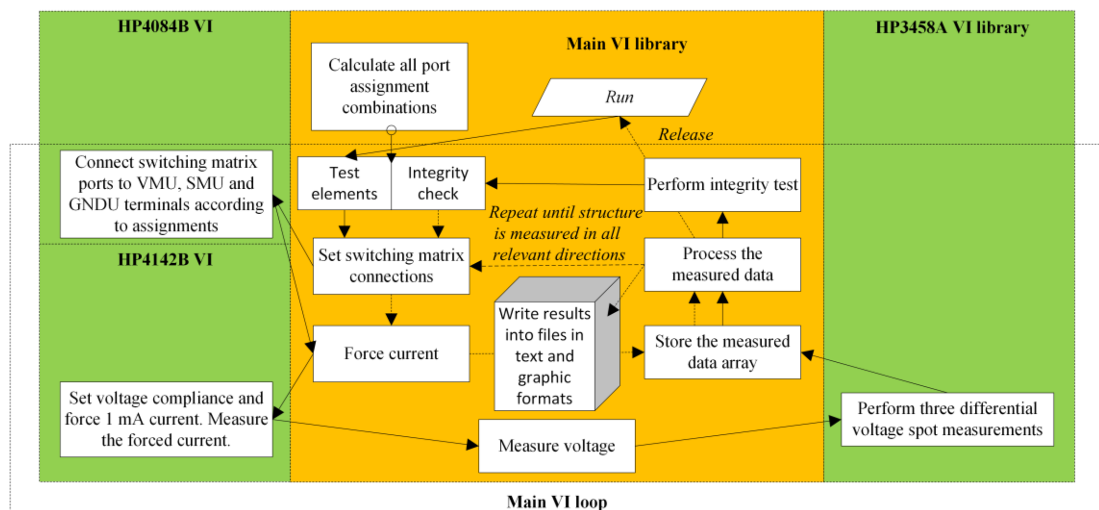

Figure 6.2.11: *Block diagram of test structure-related VI functional flow.*

The same test setup was used to measure the bridge devices by forcing 15 V with 5 mA compliance and measuring output voltage within ±2 V range with 2 μV resolution. Voltage was supplied to force current in forward and reverse directions while the output voltage was measured from *IN+* to *IN-* without swapping voltage terminals in order to keep track of the sign of the measured value. The drawback of this setup was that 15 V was supplied using connections of SMU1 and the GND

terminal in the switching matrix, which made the voltage delivered to the transducer inputs dependent on the contact, switch and lead resistance values, and this changed with each new assignment of the terminals. Therefore a potentially systematic effect existed with each bridge-related measurement.

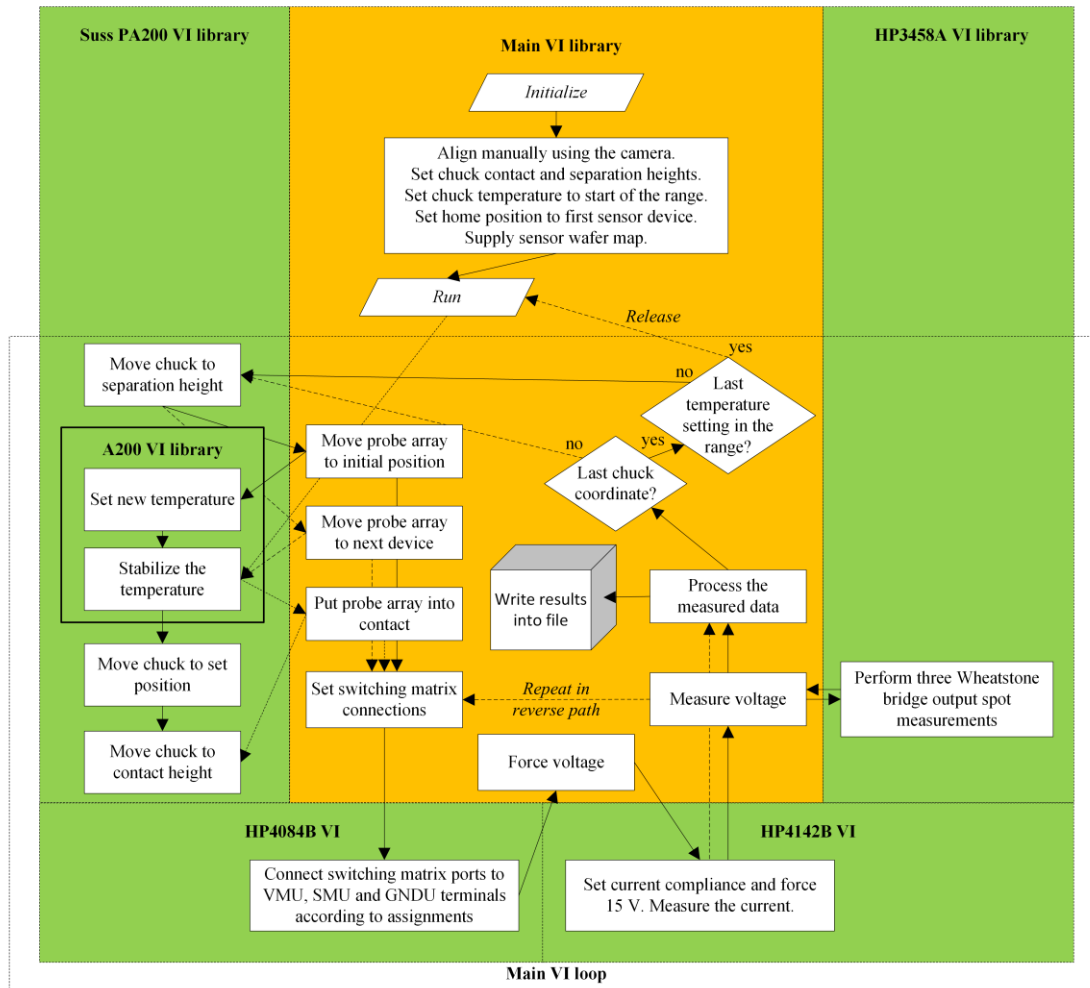

Figure 6.2.12: *Block diagram of sensor-related VI functional flow.*

The chuck temperature was controlled with ± 0.1 °C and measured with a 0.01 °C precision in the temperature range of interest (20 to 200 °C). Fully automated tests were performed for 128 sensor devices across this temperature range in a set of measurement sessions. The functional flow of the virtual instrumentation that enabled such operations is shown in Figure 6.2.12.

6.3 Fabrication

Layout design improvements were fabricated using a new set of photolithography masks. The microfabrication process flow used with the design revision detailed in section 6.2 is depicted schematically in Figure 6.3.1 and a detailed runsheet B.1.1 describing microfabrication steps is available in Appendix B.1.

Sensors and test structures of the same batch were fabricated during the same deposition runs of TaN, and Pt was deposited in separate runs according to the batch purpose. Examples of fabricated devices produced using the integrated processes ('Process 1') are shown in Fig. 6.3.2. The batch yield assessed using an optical microscope only identified one out of 256 devices on two wafers as having a visible defect in the aluminium interconnect.

The test structure-related batch was fabricated up to the PECVD oxide deposition step. This was not carried out at this stage so that the PECVD process did not affect the metallic thin films, in particular, to avoid a possible effect of elevated temperature and a change of stress during the addition of PECVD oxide layer onto the top of metallic thin film stack. This microfabrication processes ('Process 2') is described in full detail in a runsheet B.1.2 in Appendix B.1. Examples of the individual test structures fabricated are shown in Fig. 6.3.3.

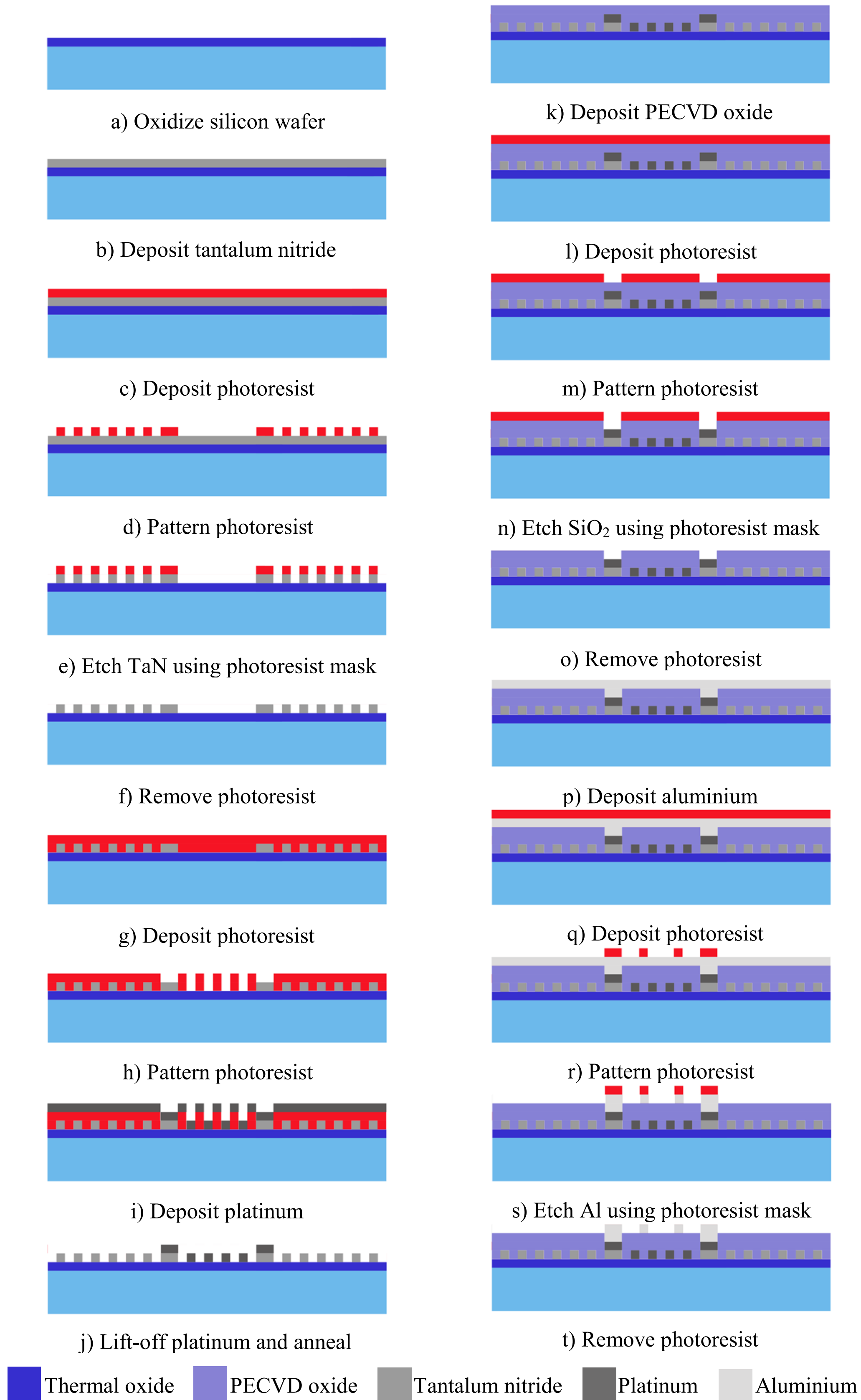

Figure 6.3.1: *Improved design of microfabrication process flow*

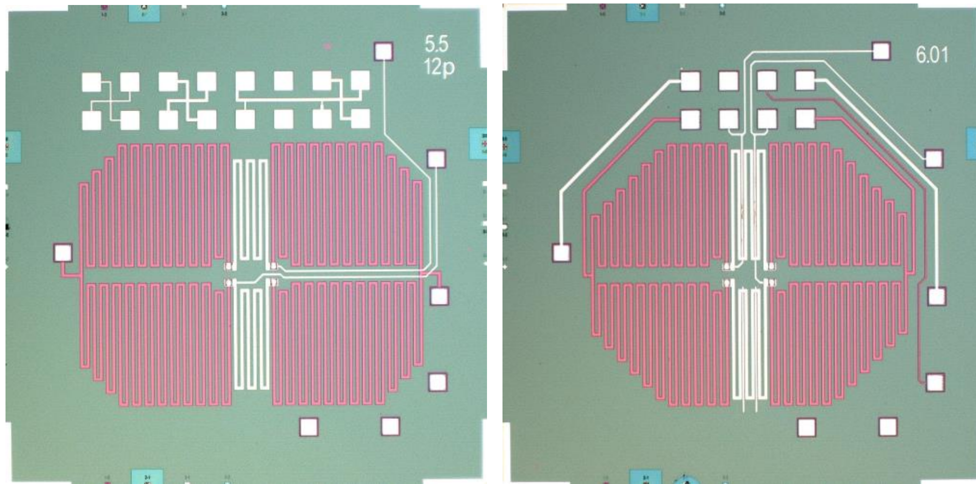

Figure 6.3.2: *Fabricated bridge devices: (left) standalone temperature sensitive element designed to be integrated directly with SiC electronics; (right) device to be integrated with SiC electronics and measured using the probe array.*

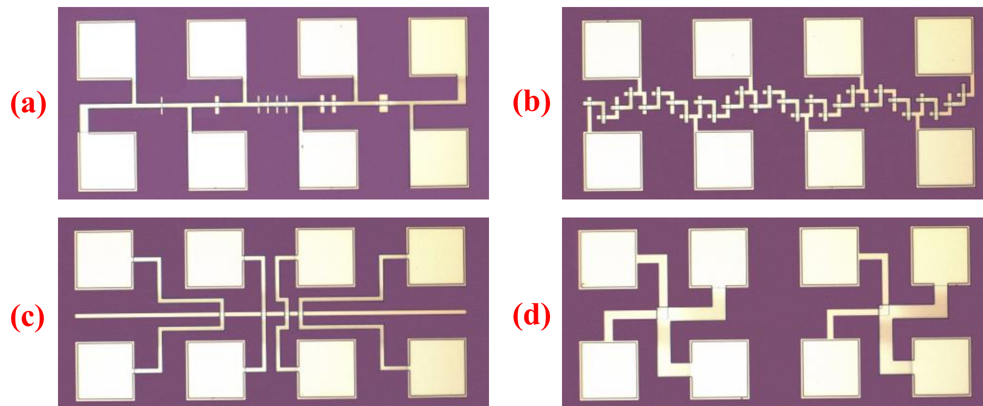

Figure 6.3.3: *Examples of fabricated test structures: (a) Step resistance test structure; (b) Contact chain test structure; (c) TLM-type test structure designed to measure contact resistance; (d) CBKR-type contact resistance test structures*

Unfortunately, samples with both annealed and as-deposited TaN and Pt films in temperature sensing devices produced by a full run of 'Process 1' had their interconnect damaged during the course of automated testing before the improved probing procedure was developed and as a result two wafers were rerun using the process detailed in runsheet B.1.1. Photographs of some resulting circuits are presented in Figs. 6.3.4 and 6.3.5. The yellow squares identify Pt debris, which appeared after the lift-off of Pt film on some devices. However, this was not a cause for concern provided they did not redeposit onto conductive structures and short neighbouring tracks or did not occupy areas around contact vias between Al and Pt

layers. This debris proved impossible to remove once the wafers were dry and was fixed in position after thin film structures were covered by the passivating PECVD oxide layer.

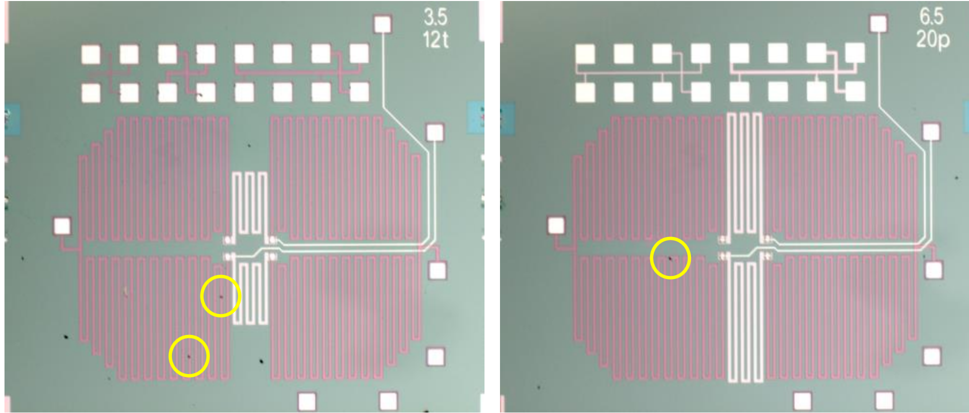

Figure 6.3.4: *Re-fabricated (Process 1) standalone bridge elements designed to be integrated with SiC electronics with sheet resistance test structures on chips. Yellow circles identify Pt debris.*

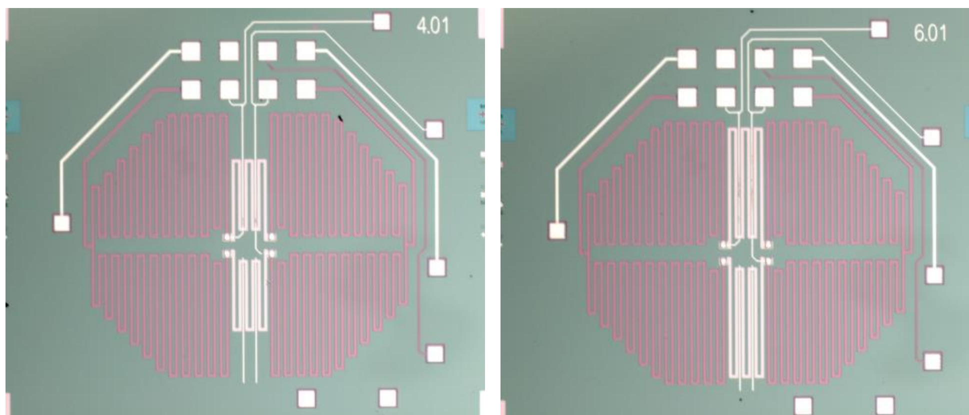

Figure 6.3.5: *Re-fabricated (Process 1) standalone bridge with TaN interconnect designed to be integrated with SiC electronics and measured using the probe array.*

Following the successful electrical measurements of the test structure wafer batch, another wafer was fabricated, where step-producing mesas were fabricated in PECVD oxide instead of TaN. The purpose of this wafer was to estimate the step coverage resistance of a platinum track that traversed across non-conductive features. The full microfabrication process ('Process 3') is detailed in runsheet B.1.3 in Appendix C and an example of a test structure produced by such process is shown in Fig. 6.3.6.

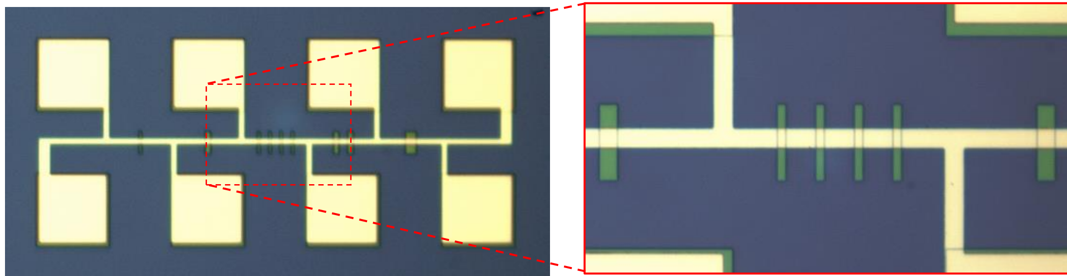

Figure 6.3.6: *(Left) Step coverage resistance test structure, where conductive platinum layer was used on top of patterned PECVD oxide mesas. (Right) Test structure segment with 4×5 μm mesa overlap.*

Following from measurements of test structures, where high step resistance and related parameter values were observed, samples with as-designed 200 nm-thick platinum film were prepared for SEM measurement utilizing the layout illustrated in Fig. 5.4.6. Two patterns were chosen to be covered by platinum – 250 nm-thick patterns produced in PECVD oxide layer and 200 nm-thick patterns in thin TaN film. Full details of the microfabrication process ('Process 4') used are provided in a runsheet B.1.4 in Appendix B. A blanket layer platinum was deposited during the same time as was the structure shown in Fig. 6.3.6.

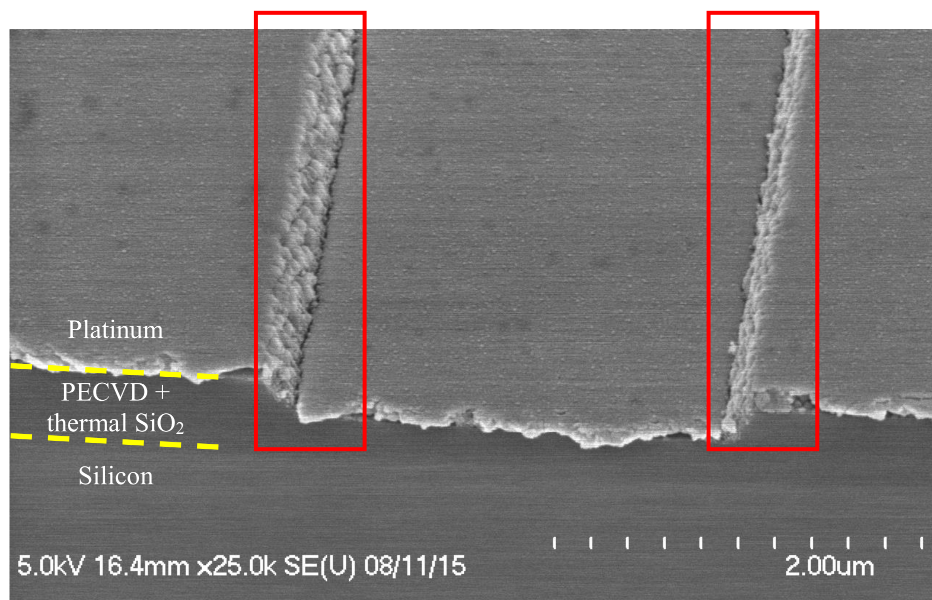

Figure 6.3.7: *Illustration of PECVD sidewall coverage by annealed platinum film: tilted cross-section view from SEM tool*

Figures 6.3.7 and 6.3.8 show how a blanket platinum layer covers features produced in PECVD oxide. The areas identified by the red boxes are of most concern as they appeared to be the reason for the high measured resistance in the test structure that used multiple metal layers. The platinum deposited onto the surface of a smooth RIE-etched sidewall is rough both when as-deposited (Fig. 6.3.8) and annealed (Fig. 6.3.7). It is also evident from these SEM images that platinum at the top of fabricated features appears to be probably not electrically connected with platinum at the bottom of trenches as cracks between these two levels of the structure are present in both as-deposited and annealed samples.

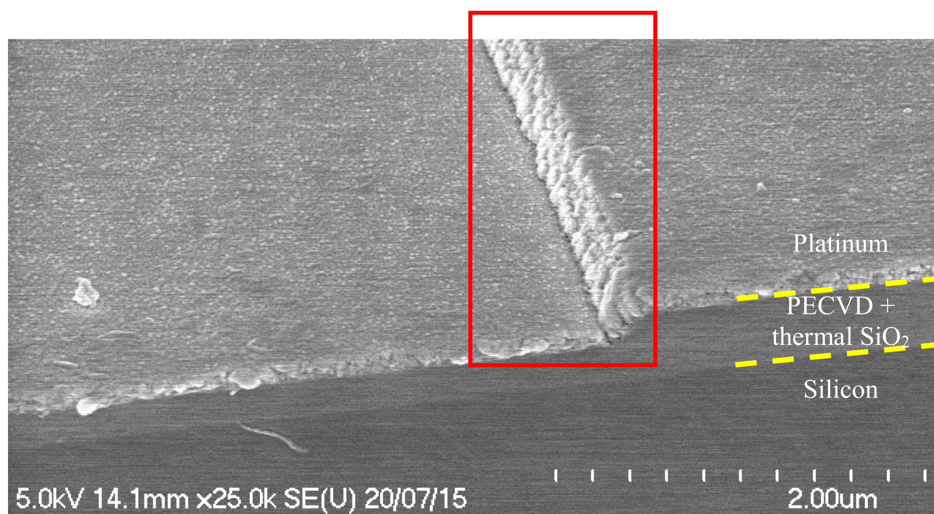

Figure 6.3.8: *Illustration of PECVD sidewall coverage by as-deposited platinum film: tilted cross-section view from SEM tool*

Samples, where Pt was deposited onto TaN had a similar issue with platinum thin film covering a vertical wall of the metallic features. The platinum film completely covers both thermal oxide and TaN horizontal surfaces. However, the sidewall coverage of the TaN is again extremely rough as highlighted by the red rectangle in Fig. 6.3.9 (left). Sample with as-deposited platinum blanket film on TaN features was also characterised and found to have cracks at the bottom of the sidewall as illustrated in Fig. 6.3.9 (right). Although Figure 6.3.9 is not conclusive proof, it is also likely that there are probably cracks in platinum layer at both top and bottom of sidewall of the TaN features. Figure 6.3.10 shows fabricated features as viewed with an optical microscope before the SEM samples were prepared.

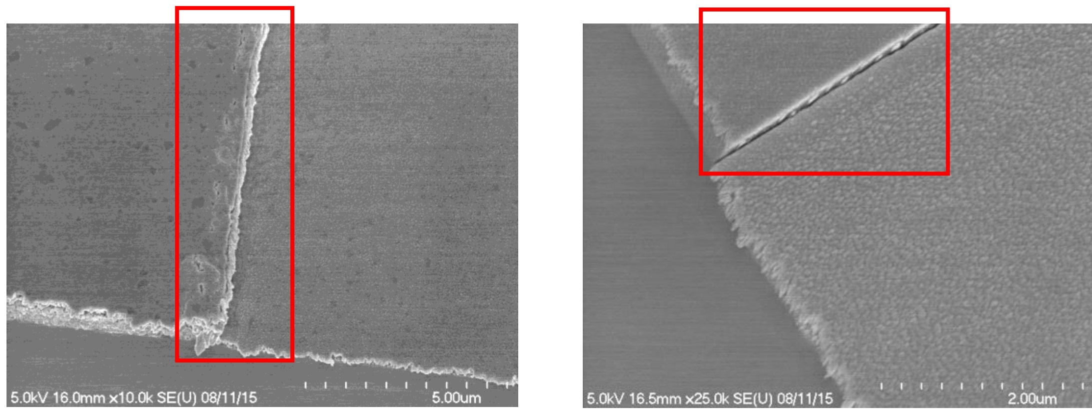

Figure 6.3.9: *Illustration of TaN sidewall coverage by platinum film, tilted view from SEM tool: (left) annealed platinum covering TaN sidewall; (right) as-deposited platinum covering TaN sidewall.*

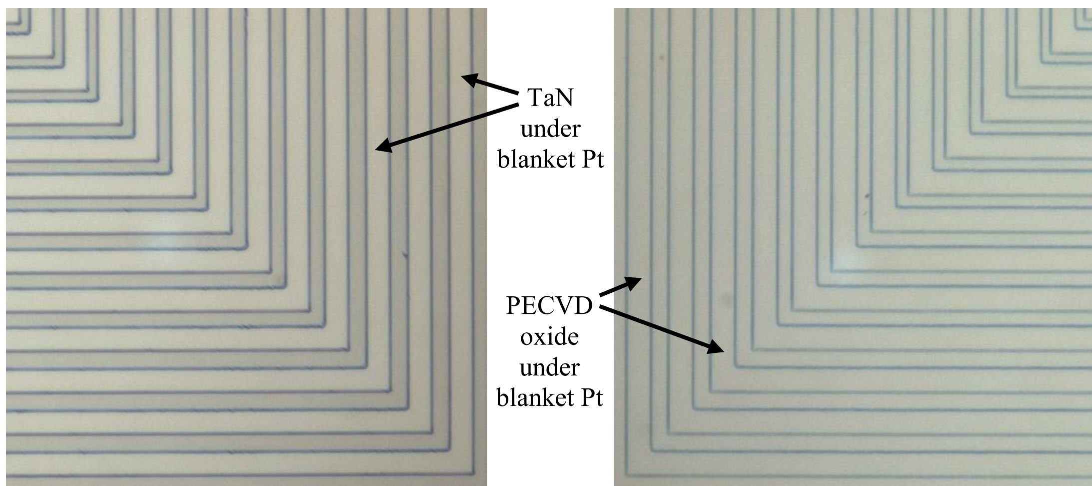

Figure 6.3.10: *Illustration of fabricated features, top-down view from light microscope: (left) blanket Pt layer on TaN features; (right) blanket Pt layer on PECVD oxide features.*

It is evident from images such as shown in Fig. 6.3.9 that the deposited platinum film was thinner than the TaN film, and therefore Pt thickness was re-measured utilizing Dektak 8000 profilometer on the wafers with test structures (refer to Fig. 6.3.6). The average measured film thickness was 135 nm.

A run with 400 nm target platinum film thickness was performed to produce two wafers with test structures and one wafer with both sensor devices and test structures, using the microfabrication flow ‘Process 5c’ detailed in Appendix B.1. Four new masks were required to produce this batch. The platinum thickness was measured using Dektak 8000 profilometer immediately after the lift-off of the platinum film

and was found to be 240 nm thick on average on two measured wafers. Figure 6.3.11 shows fabricated sensor devices while Figure 6.3.12 demonstrates the fabricated test structure arrays.

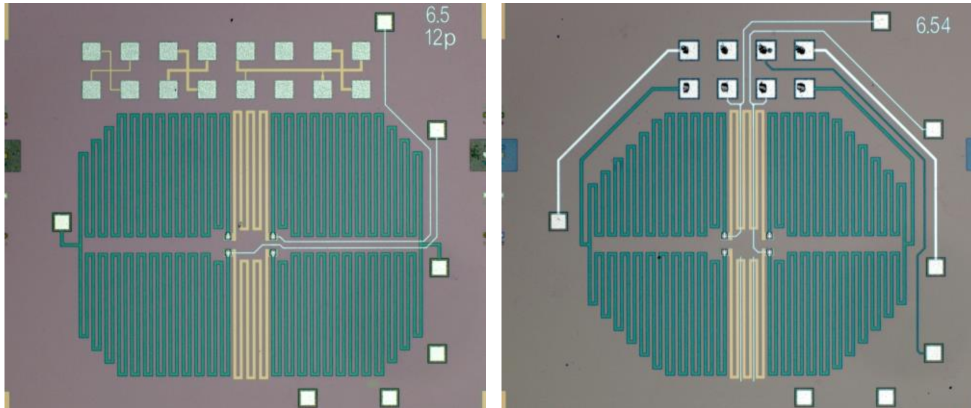

Figure 6.3.11: *Fabricated bridge devices (Process 5) using 240 nm-thick Pt: standalone device designed to be integrated directly with SiC electronics (left); device to be measured using the probe array (right).*

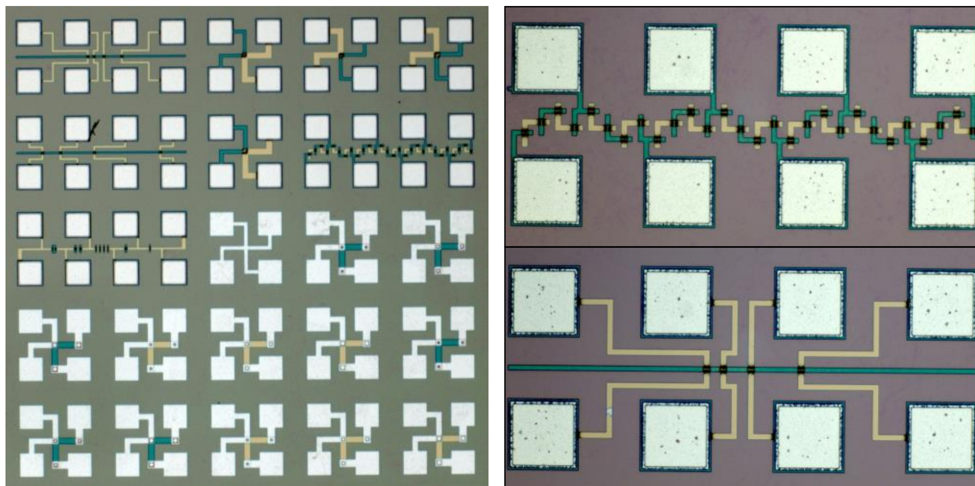

Figure 6.3.12: *Fabricated test structure array (Process 5) and contact chain resistance (left) and TLM-type contact resistance test structures between Pt and TaN (right).*

6.4 Measurement results

Characterisation of the batches fabricated using initial integrated microfabrication flow as described in section 5.4 was focussed on determining the

contact resistance, primarily between platinum and tantalum nitride layers. At this stage measurements of a set of newly designed test structures described in section 6.2.2 were undertaken manually using multiple wafers produced by a range of processes. Four temperature sensor device wafers were also measured using automated test procedures.

One test structure wafer produced by 'Process 2' was measured manually at the temperature of 25.03 °C. TCR measurements in the temperature range of 25 to 125 °C were performed on Pt and TaN films fabricated using microfabrication flow detailed in runsheet B.1.5. This was followed by measurement of all the sensor devices produced using the above combination of thin films across the maximum possible temperature range using a totally automated approach. Finally, randomly selected sensor devices were measured to help determine the effect of test setup non-idealities on the measured sensor characteristics.

6.4.1 Step coverage resistance measurements

A wafer with annealed thin film test structures fabricated by 'Process 2b' as described in runsheet B.1.2 was fully characterised providing measurements on 68 step coverage resistance test structures. This measured data is summarized in Table 6.4.1, where mesa overlap length L_{TS} values expressed in µm from Table 6.2.1 and equation (6.1) are replaced with the equivalent number of squares ($L_{TS□}$).

Table 6.4.1 *Step resistance values measured on all chips.*

Mesa structure			***Resistance values, Ω***				
Number	$L_{TS□}$	*n*	*Minimum value*	*Median value*	*Maximum value*	*Mean value*	*Standard deviation*
1	*0.5*	*2*	230	321	469	323.96	39.26
2	*1*	*2*	187	295	423	288.46	40.62
3	*2*	*2*	180	250	411	262.12	52.57
4	*2*	*4*	214	351	483	352.24	64.09
5	*2*	*8*	391	557	941	572.13	99.07

The measured resistance increased significantly with increasing step count *n* while decreasing the overlap length L_{TS} decreased the resistance of the measured

bridge segment. If we recognize that in Eq. (6.1) resistance R_{TS} of the mesa overlaps are a combination of the parallel resistance of upper and lower layers, and also a pair of resistance values $\bar{R}_{sw}$, which are introduced by steps in the upper layer metal (refer to Fig. 6.2.4b), then:

$$V_m = I_m\left(R_{S(Pt)}(L_{m\square} - L_{TS\square}) + R_{S_{||}}L_{TS\square} + n\bar{R}_{sw}\right) =$$
$$= I_m\left(R_{S(top)}L_{m\square} - L_{TS\square}\left(R_{S(top)} - R_{S_{||}}\right) + n\bar{R}_{sw}\right), \quad (6.7)$$

where $R_{S_{||}} = R_{S(Pt)}||R_{S(TaN)}$, $L_{m\square}$ is the track length in squares (12 for this design), and n is the number of steps. In addition, it is possible to define the following set of inequalities:

$$\begin{cases} R_{S\|} < R_{S(TaN)}, \\ R_{S\|} < R_{S(Pt)} \end{cases} \quad (6.8)$$

The mesa structures 1-3 were designed to determine the effect of different overlap lengths, while mesa structures 3-5 were used to estimate step resistance (refer to Fig. 6.2.4). At the same time, all measured values should obey (6.7) when compared with one another. The following set of inequalities should also be true for resistance values R_k measured using mesa structure number k:

$$\begin{cases} R_3 < R_2 < R_1, \\ R_3 < R_4 < R_5 \end{cases} \quad (6.9)$$

If these inequalities were not valid for a measured structure this implies that there is a yield issue on the chip and the results should be disregarded for either or both mesa structure groups 1-3 or 3-5. The conditions identified in Eq. (6.9) have been checked using validation maps shown in Figure 6.4.1. Measurement results that did not comply (red in Fig. 6.4.1) were eliminated from data set and the validated data is presented in Table 6.4.2, which shows that the variability of measured resistance values increases with increasing step count or decreasing overlap length. It is important to note here that increasing the step count means that the overlap length for each individual mesa is reduced while the pattern density of mesa features is increased.

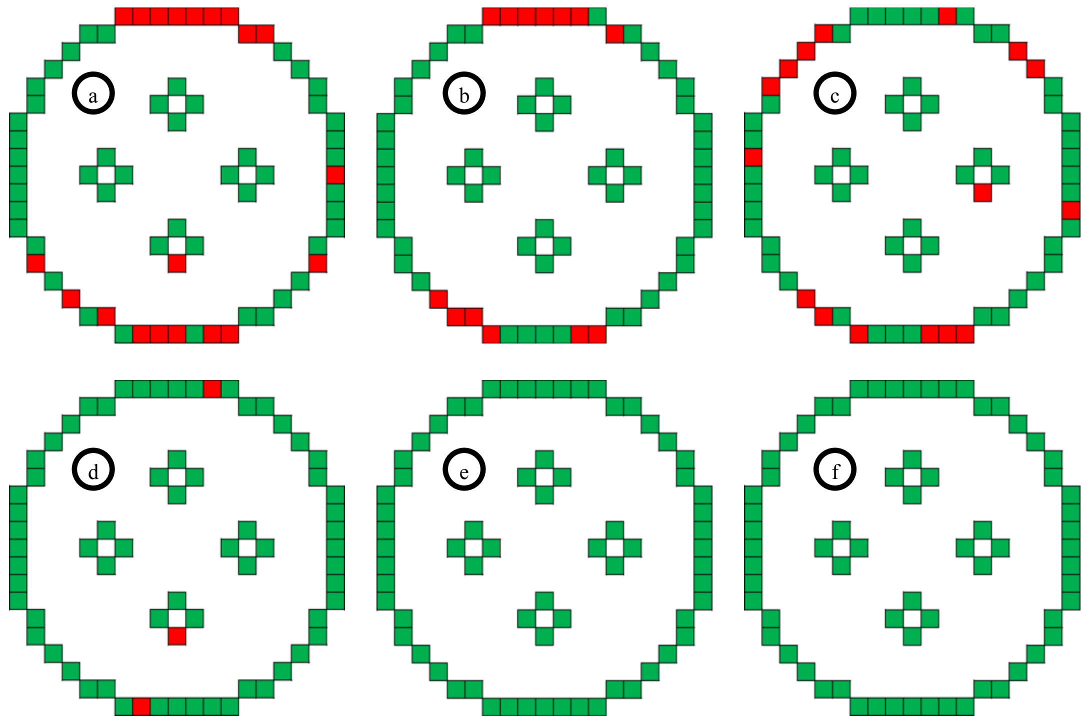

Figure 6.4.1: *Measured resistance value validation maps based on set of inequalities (6.9): (a) $R_3 < R_2$; (b) $R_3 < R_1$; (c) $R_2 < R_1$; (d) $R_3 < R_4$; (e) $R_3 < R_5$; (f) $R_4 < R_5$. Green denotes validated test structure groups.*

Table 6.4.2 *Step resistance test structure data validated using Eq. (6.9).*

Mesa structure			***Resistance values, Ω***				
Number	$L_{TS□}$	*n*	*Minimum value*	*Median value*	*Maximum value*	*Mean value*	*Standard deviation*
1	*0.5*	*2*	242	331	469	332.44	41.25
2	*1*	*2*	203	281	331	279.31	33.00
3	*2*	*2*	180	232	293	235.72	25.18
4	*2*	*4*	222	353	483	354.82	62.38
5	*2*	*8*	391	557	941	572.13	99.07

Figure 6.4.2 shows measured and validated values for mesa structures 3-5, where the step count *n* is 2, 4 and 8 respectively. The trend of average resistance is linear and the mean step resistance $\bar{R}_{sw}$ was 55.8 Ω. Figure 6.4.3 shows measured and validated values for mesa structures 1-3, where the overlap area $L_{TS□}$ was 0.5, 1 and 2 squares respectively. Each of these structures should have similar values of step resistance $2R_{sw}$ and different values for the resistance of the mesa overlap $R_{||}$. The

overall effect of increasing the overlap length in squares should be to decrease the track resistance by:

$$\Delta R = L_{TS\square}\left(R_{S(Pt)} - R_{||}\right) \tag{6.10}$$

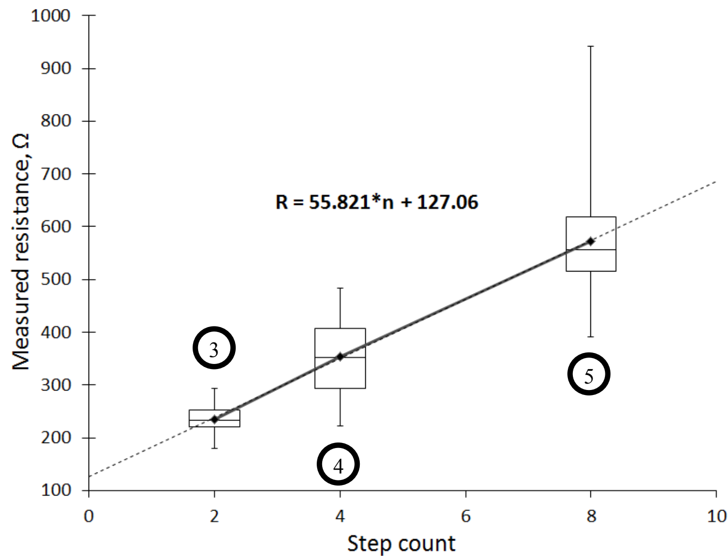

Figure 6.4.2: *Resistance change with increasing step count, using mesa structures 3, 4 and 5 in Fig. 6.2.4(a).*

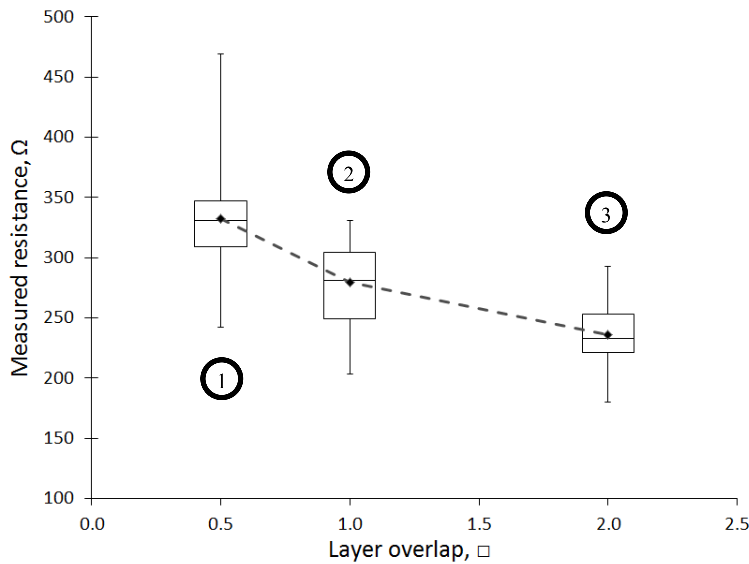

Figure 6.4.3: *Resistance change with increasing layer overlap, using mesa structures 1, 2 and 3 in Fig. 6.2.4(a).*

Based on the measured values of sheet resistance of platinum and tantalum nitride in this process (4.4 ± 0.1 Ω/□ and 14.0 ± 0.5 Ω/□ at 25 °C), the value of *ΔR*

should have a maximum value of around 1 Ω. However, the measured difference in resistance between a layer overlap of 0.5 and 1 square, and also between 1 and 2 squares was of the order of 50 Ω. This indicated that there was an additional effect from the fabrication, which was not covered by the model, most likely coming from platinum feature cracks and thinnings of platinum layer around walls of TaN features similarly to those identified by SEM and shown in Fig. 6.3.9.

Step coverage test structures were also measured on wafer with as-deposited TaN and Pt films produced by 'Process 2a'. In this measurement 30 out of 68 measured test structures were found to have an extremely high resistance (>13 kΩ) of test structure segments 1-5. The only segments that did not contain mesa features underneath the Pt tracks, such as 6 and 7, passed the verification test. As a result, it can be concluded that the yield of fabricated test structures was poor due to an effect produced by mesa features fabricated with TaN.

Test structures, which were created from PECVD oxide mesas and as-deposited platinum tracks using 'Process 3' as described in runsheet B.1.3, also had extremely poor yield with every segment failing the integrity test in 28 measured structures. The reason for poor integrity was related to both the increased height of mesa structure and cracks formed in platinum film at the bottom of mesa structures as identified by the SEM results (refer to Fig. 6.3.8).

Increasing the platinum thickness (to 240 nm as measured by a profilometer) and using 'Process 5a' to fabricate wafers as detailed in Appendix B.1.5 improved the average measured step resistance, but resulted in an inferior yield compared with the first set of data in Table 6.4.2. Samples with the as-deposited TaN and Pt, which were not covered by PECVD oxide, had every second test structure (26 out of 52 positioned near the wafer edge), and only 5 structures at the bottom of the wafer passed the integrity test of every segment in the structure. The average effect of a Pt track stepping over a TaN mesa in working structures was found to be 7.73 Ω, which is lower than the value previously reported in Fig. 6.4.2. Additionally, $R(n = 0)$ was 13.19 Ω, which was a reasonable value for 12 squares of the given sheet resistance platinum track ($R_{S(Pt)} = 1.25 \pm 0.02$ Ω/□).

Both tracks covered and not covered by PECVD with annealed thin films (produced accordingly using ‘Process 5b’ and ‘Process 5c’) had faulty step coverage in 10 µm-wide tracks, as 28 measured test structures (out of 68 total available) had every segment failing the integrity test.

6.4.2 Contact resistance measurements using TLM and chain structures

Modifications of transmission line model (TLM) and contact chain test structures were found to have similar issues as they were designed to have the same parasitic elements – the TLM-type structure had a set of two 10×10 µm^2 contacts and four 10 µm-wide step resistance elements between each pair of pads while contact chain test structure had two more contact elements.

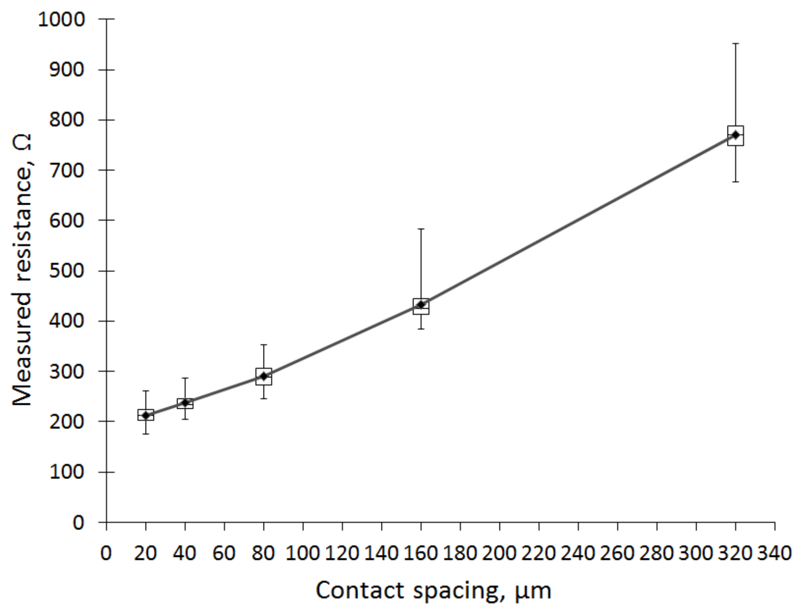

Figure 6.4.4: *Resistance as a function of contacts spacing in TLM structures: measurements from test structures with L = 20 to 320 µm.*

All 68 test chips with TLM test structures were measured on annealed samples produced by ‘Process 2b’ detailed in runsheet B.1.2. The measured resistance value becomes larger with increasing contact spacing as shown in Fig 6.4.4. The average value of measured contact resistance for the 10×10 µm^2 contact area in approximation of contact spacing L between 20 and 80 µm is 93.35 Ω as suggested

by measured value of $2R_C$ = 186.71 Ω illustrated in Fig. 6.4.5 when L is reduced to 0 µm. The slope value shown on the graph is related to R_S/W characteristic and from equation (6.3) the average measured linewidth W can be estimated as 10.85 µm ($R_{S(TaN)}$ = 14.0 Ω/□).

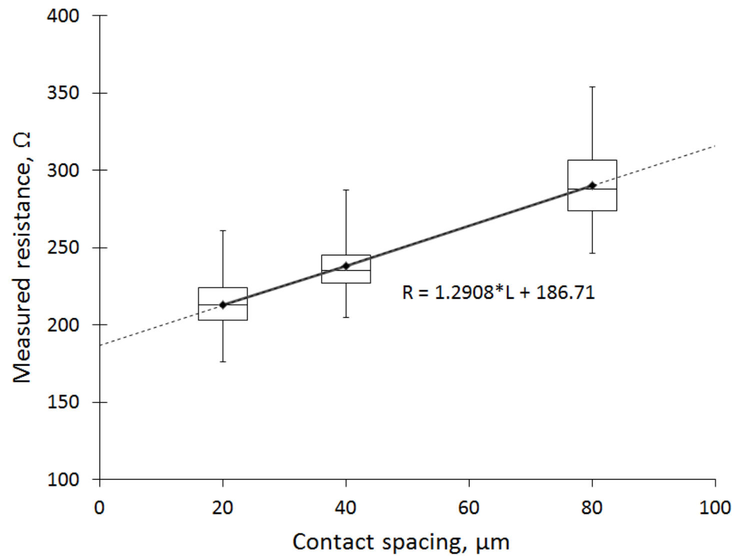

Figure 6.4.5: *Resistance as a function of distance between contacts in TLM structures: measurements from test structures with L = 20, 40 and 80 µm.*

The as-deposited sample produced by the same process ('Process 2a') had a significantly lower yield of TLM-type test structures, where it passed the integrity test on only 7 out of 26 test chips measured. From plots similar to Fig. 6.4.5, the average measured contact resistance value was found to be 7.49 Ω as indicated by a $2R_C$ value of 14.97 Ω.

An as-deposited sample fabricated by 'Process 5a' described in runsheet B.1.5 had better yield compared with the previously described sample with 14 test structure chips situated at the bottom of the wafer out of 26 measured which passed the integrity test. The value of $2R_C$ extrapolated at L = 0 was 64.6 Ω, which indicated an average measured value of 32.3 Ω for as-designed 10×10 µm^2 contact.

There was no opportunity to measure a reliable value from contact chain resistance structures as compliance limits were hit indicating open circuit or greater than 13 kΩ resistances most likely resulting from breaks in conductive paths due to issues with step coverage.

6.4.3 Contact resistance measurements using CBKR structures

Figure 6.4.6 shows data measured using CBKR-type structures (52 chips out of 68) on annealed sample from a batch produced by 'Process 2a' described in runsheet B.1.2. 20×20 μm^2 contact area structures had average measured resistance values of 90.1 Ω while 15×15 μm^2 structures had contact resistance of 104.6 Ω on average. The effect of misalignment was relatively small when compared to the variation in measured resistance, however it increased with decreasing contact area. The average values of measured contact resistance for the standard and mirrored test structures were 102.0 Ω and 107.0 Ω for 15×15 μm^2 contacts and 95.1 Ω and 85.7 Ω for 20×20 μm^2 contact areas while the distribution seemed to be completely dominated by contact resistance variation as partly indicated by results shown in Fig. 6.4.6.

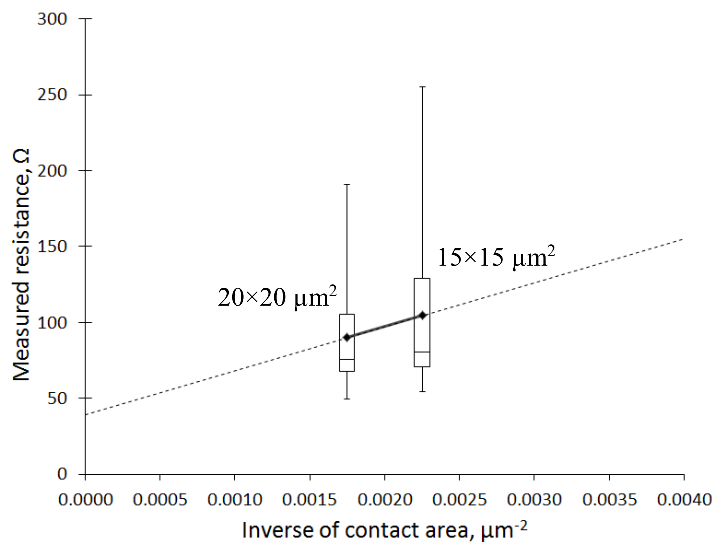

Figure 6.4.6: *Measured resistance change against inverse of contact area of CBKR test structures on annealed sample with 200 nm Pt.*

Sample fabricated by 'Process 5c' had 54 working test structures out of 136 fabricated in total for 15×15 μm^2 contact area and 60 measurable test structures with designed contact area of 20×20 μm^2. The average measured resistance values were 3.15 Ω for both types of test structures.

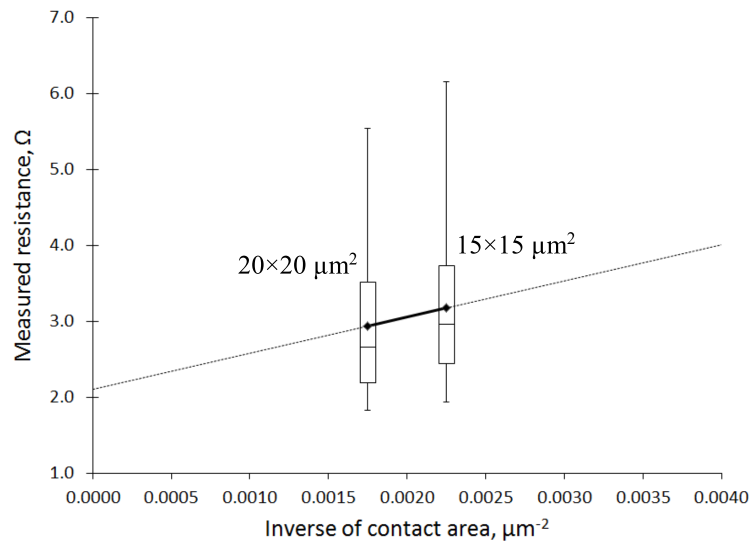

Figure 6.4.7: *Measured resistance change against inverse of contact area of CBKR test structures on annealed sample with 400 nm Pt without LFSiO$_2$.*

A different sample, which was processed in the same batch, but where processing was stopped before PECVD oxide deposition ('Process 5b') had 38 and 47 working test structures with designed contact areas of accordingly 15×15 and 20×20 μm^2. The measured results are shown in Figure 6.4.7, where 20×20 μm^2 contact area structures had average measured resistance of 2.94 Ω while 15×15 μm^2 structures had average contact resistance of 3.17 Ω.

6.4.4 Sensor measurements

Measurements of contact resistance test structures served as an efficient method of evaluating both contact resistance and the integrity of the step coverage that covers the sidewalls of underlying layer to make a contact. The yield of fabricated sensors was found to be higher than that of test structure chips and, unlike the case with test structures, did not solely depend on the position of sensor on the wafer. The key reason for this may be the fact that the coverage of TaN contact pads by Pt pads was better following from design improvement shown in Fig. 6.2.1.

In addition to the evident parasitic resistance caused by the contact resistance and step coverage issues, there was another issue caused by changing contact and switch

resistance with each measurement. Since sensitivity of the temperature circuitry is directly proportional to the excitation voltage, changing the resistance value that was added in series to the current path leads to a change in the measured output voltage of the order of millivolts. As a result, rather than being as simple as Eq. (5.6) and (5.7), the equation describing output of the bridge becomes:

$$V_{OUT} = V_S \times \left(\frac{R_{TaN3} + R_{Pt4} + R_{ParB3} + R_{ParC3}}{R_{TaN2} + R_{TaN3} + R_{Pt4} + R_{ParB2} + R_{ParB3} + R_{ParC2} + R_{ParC3}} - \right.$$

$$\left. - \frac{R_{TaN1} + R_{ParB1} + R_{ParC1}}{R_{TaN1} + R_{TaN4} + R_{Pt1} + R_{ParB1} + R_{ParB4} + R_{ParC1} + R_{ParC4}} \right), \qquad (6.11)$$

where R_{ParBx} denotes the value of parasitic resistance created by contact and step coverage resistances and R_{ParCx} is the term covering the resistance produced by non-idealities of test setup. The issue here was that R_{ParBx} elements were impossible to measure and hence it was problematic to estimate their TCR while R_{ParCx} were changing with every new contact made and did not have a dependence on temperature. As a solution to that, each measured data point of the response to temperature was validated by manually checking data points on both voltage and current plots.

First set of devices that consisted of thin films in as-deposited condition fabricated as detailed in runsheet B.1.1 ('Process 1a') was measured in the temperature range from 25 to 125 °C with 2.5 °C step. The measured response to temperature was validated only in the temperature range of 50 to 100 °C due to inappropriate contact conditions up to 45 °C and evident destruction of the interconnect between probe pads and sensors due to thermal expansion of probes starting at 95 °C. Measurement results are grouped according to geometrical parameters and two most important plots characterising fabricated sensors are shown in Fig. 6.4.8 and 6.4.9, namely, the start of the output range and sensitivity of response to the temperature. Full-scale output of sensors may be estimated utilizing these plots using the response to the temperature values produced by groups of different designed resistor ratio devices.

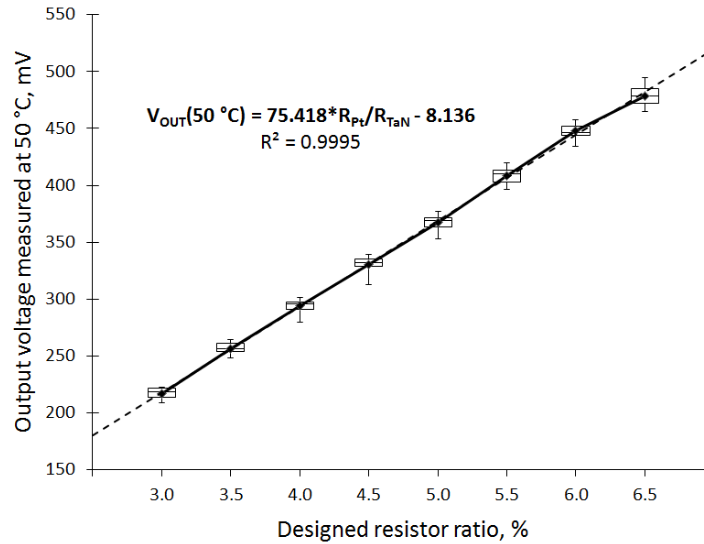

Figure 6.4.8: *Output voltage as a function of designed resistor ratio measured at 50 °C on devices on wafer 1 (Process 1a).*

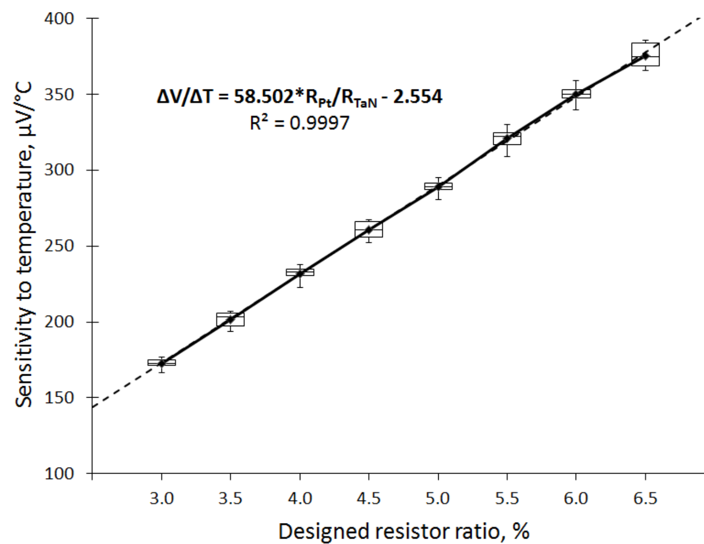

Figure 6.4.9: *Measured temperature sensitivity against designed resistor ratio of devices on wafer 1 (Process 1a).*

The measured output voltage at 50 °C was increasing proportionally to the designed resistor ratio as demonstrated in Fig. 6.4.8 for the designed resistor ratios of 3 to 6.5% as expected following from analysis provided in Chapter 3. Devices were wafer mapped according to their position on the wafer as shown in Fig. 6.4.10, where every distribution shown in Fig. 6.4.8 and 6.4.9 is grouped according to quartiles of values for according resistor ratios. Since devices are arranged symmetrically in

quadrants on the wafer, the grouping of results reveals that distribution of values depends on their position. The maximum values of mentioned characteristics in a set of 124 devices were gathered around first quadrant of the wafer whereas minimum value was measured on chips in the third quadrant. The reason for such distribution is the cumulative effect of parasitic resistances in devices and the fundamental characteristics of thin film from which they were fabricated, e.g. the distribution of Pt and TaN film sheet resistance and TCR on the wafer.

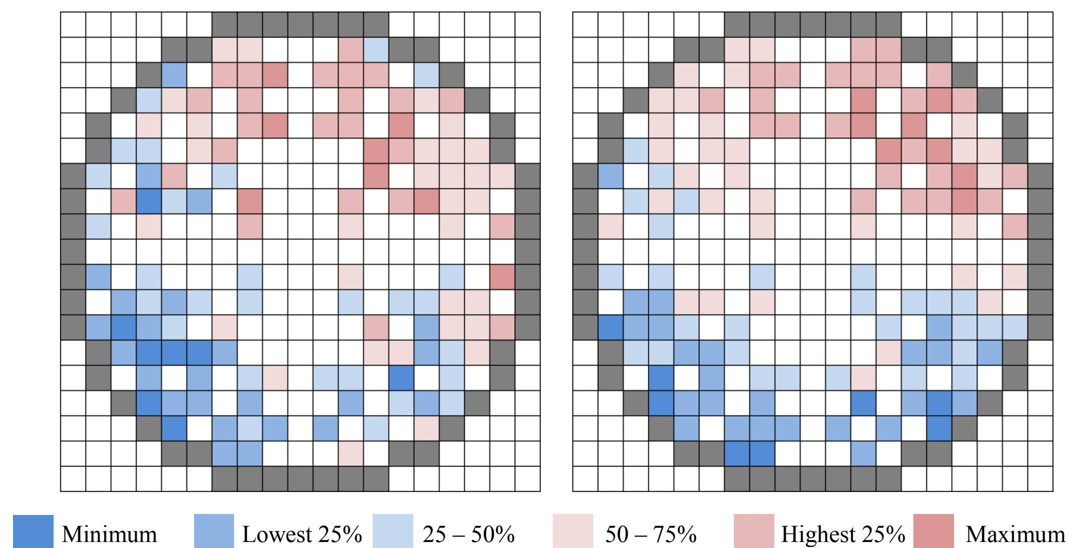

Figure 6.4.10: *Wafer maps of measured (a) start of output range and (b) sensitivity values demonstrated in Fig. 6.4.8 and 6.4.9.*

Devices on another wafer produced by 'Process 1b' with annealed thin films were measured from 25 to 100 °C. Measured data was validated between 45 and 80 °C due to problems with test setup and inability to make multiple measurements as a result of thermal expansion of the probes.

Processed data of key device characteristics measured on 109 working sensors are presented in Figs. 6.4.11 and 6.4.12. Compared to the wafer with non-annealed films in Figs. 6.4.8 and 6.4.9, the starting output has decreased while the sensitivity of the devices has increased. The distribution of starting values was biased towards higher voltage values while the distribution of the measured sensitivity was heavily biased towards lower voltage values. Devices producing skew into the distribution

are identified by the darker red colours in Fig. 6.4.13 (left) and with darker blue colours on the right-hand plot.

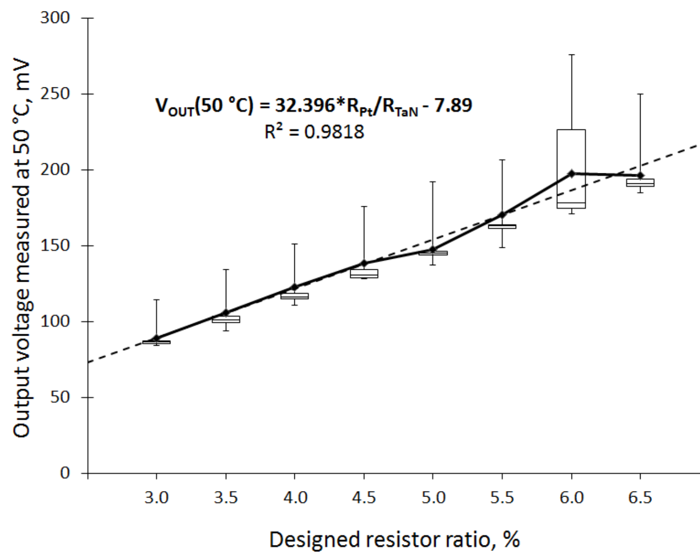

Figure 6.4.11: *Output voltage as a function of designed resistor ratio measured at 50 °C on devices on wafer 2 (Process 1b).*

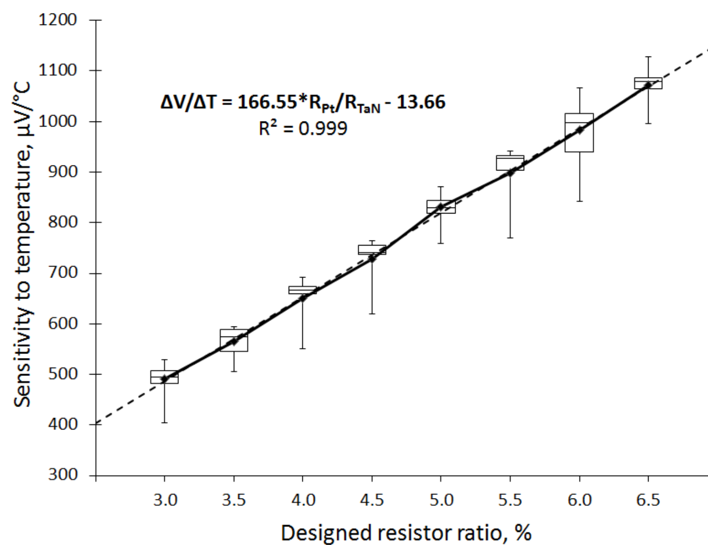

Figure 6.4.12: *Measured temperature sensitivity against designed resistor ratio of devices on wafer 2 (Process 1b).*

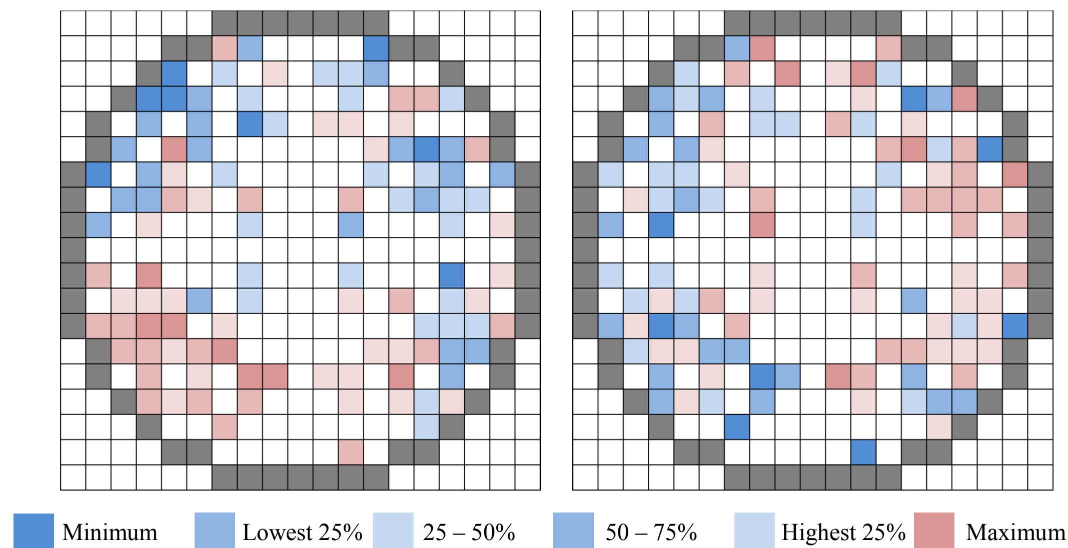

Figure 6.4.13: *Wafer maps of measured (a) start of output range and (b) sensitivity values demonstrated in Fig. 6.4.11 and 6.4.12.*

Although the difference in processing between two wafers was related to the annealing process and the different position of the wafers during the deposition of Pt, these measurements were unexpected and opposite of those demonstrated in Fig. 6.4.10. While there is still an apparent distribution of values from the first to the third quarter of the wafer, which is governed by uniformity of sheet resistance and TCR of Pt and TaN films across the wafer, it is less ordered compared with the previous set of results. Similarly to that demonstrated in subsection 3.3.2, when values of output voltage at the start of temperature range and sensitivity are opposite, it is a sign of diagonal mismatch in the balancing circuit (refer to Fig. 3.3.9 and Fig. 3.3.10). Such mismatch was most likely caused by an unexpected deviation of annealing process, which has changed the integrity of structures fabricated in the Pt film around contact to TaN features (similarly to Fig. 6.3.9).

Following from test setup improvements described in subsection 6.2.4, the measurement range was increased to 175 °C with no damage to the devices and validated the data over the whole measurement range. The measurement of devices produced by another iteration of 'Process 1a' detailed in runsheet B.1.1 was unsuccessful, yielding no useful devices evidently due to poor integrity of platinum film on the sidewall of TaN features. Wafer processed during the same deposition steps as the failed wafer produced by 'Process 1b' was effectively a reiteration of

previously attempted process with annealed films (refer to Fig. 6.4.11 and 6.4.12). Summary of validated data measured on 115 devices produced by such process is provided in Table B.2.1 separately for forward and reverse measurements while Fig. 6.4.14 and 6.4.15 show the data plots produced by averaging characteristics found by forward and reverse measurements.

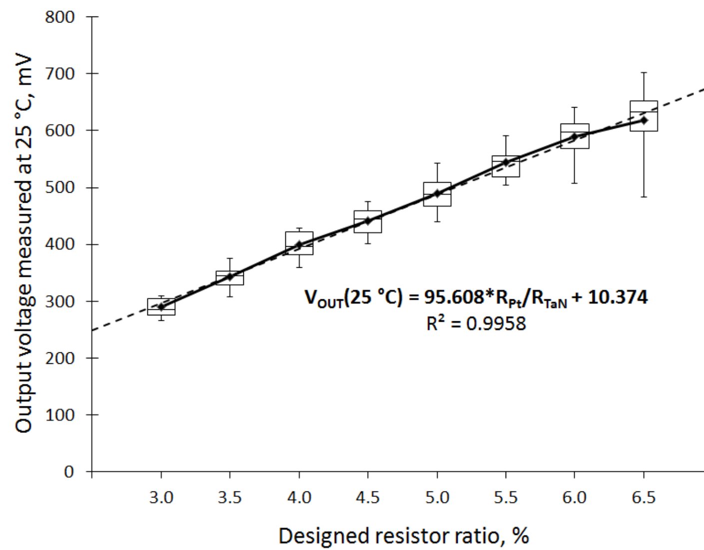

Figure 6.4.14: *Output voltage as a function of designed resistor ratio measured at 25 °C on devices on wafer 3 (Process 1b).*

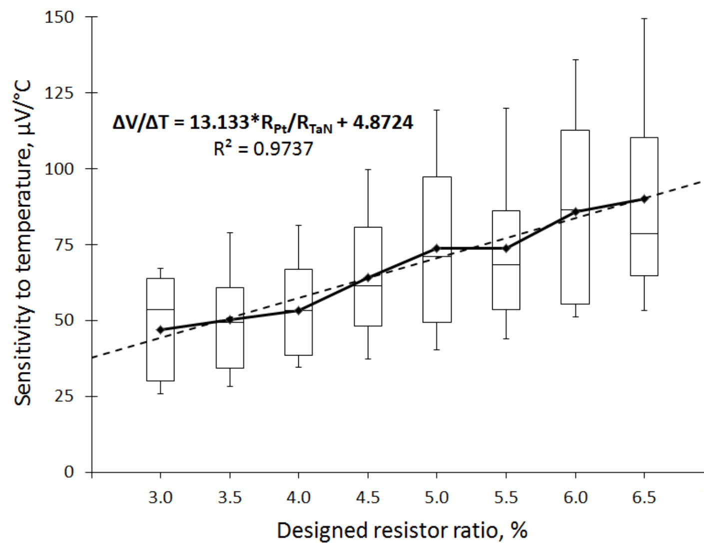

Figure 6.4.15: *Measured temperature sensitivity against designed resistor ratio of devices on wafer 3 (Process 1b).*

The effect of mismatch is more evident in fabricated devices when compared with Fig. 6.4.11 – 6.4.13. The sensitivity of devices produced on this wafer using effectively the same fabrication process has dropped from 166.55 μV·°C^{-1} per percent of ratio between temperature sensitive and balancing resistors to 13.13 μV·°C^{-1} as a result of apparent increased mismatch and the different sheet resistance and TCR values of Pt and TaN. Consequently, the full-scale output range has also narrowed, while starting values in the range have significantly increased. The systematic effect produced by measurement setup has not been eliminated completely. However, it will not affect the relative values which graphs such as that shown in Fig. 6.4.16 are based on. There is a more evident position-dependent key sensor characteristic distribution from the left to the right side of the wafer compared with the results presented in Fig. 6.4.13.

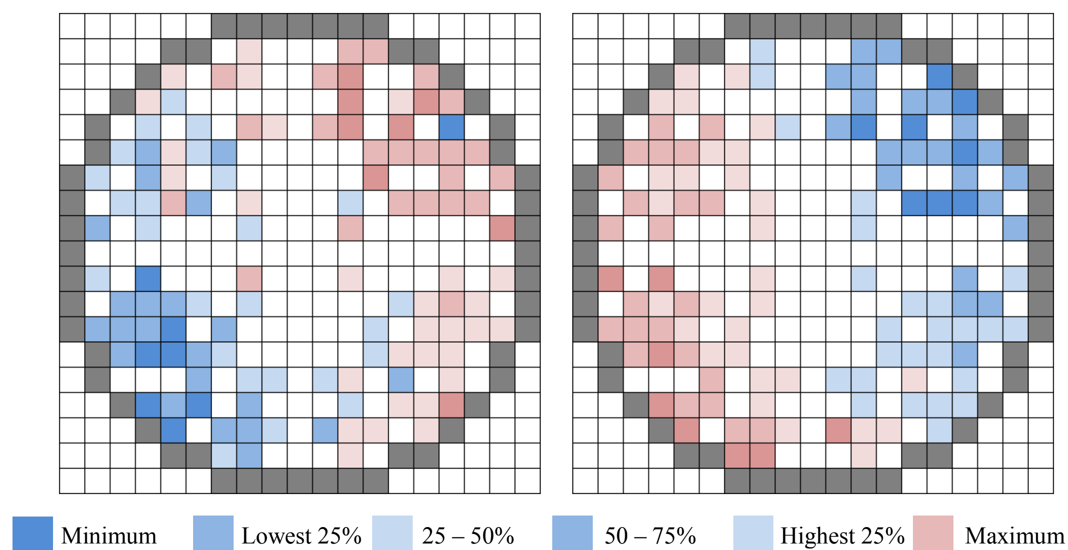

Figure 6.4.16: *Wafer maps of measured (a) start of output range and (b) sensitivity values demonstrated in Fig. 6.4.14 and 6.4.15 and detailed in Table B.2.1.*

A final measured device wafer was fabricated by 'Process 5c' described in runsheet B.1.5 and had nearly twice the thickness of platinum compared with previously described wafers. These measurements on 128 fabricated devices in a temperature range between 25 and 200 °C were validated and as a result 122 plot families were used to determine the response to the temperature characteristics summarised in Table B.2.2. The averages between plot families were used to produce

Figs. 6.4.17 and 6.4.18. The output range of the temperature response of these sensor devices has gone below 0 V in 29 out of 122 devices indicating enormous diagonal mismatch present in the balancing circuit, which not only minimised the starting value of the temperature response, but also significantly decreased the sensitivity to temperature.

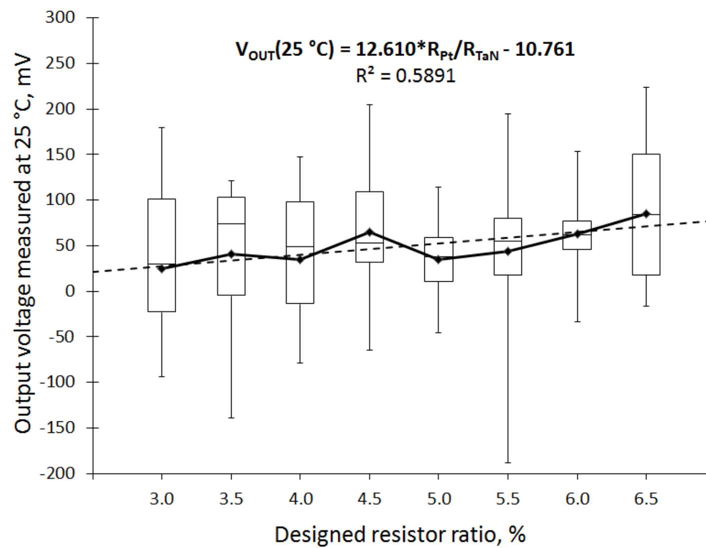

Figure 6.4.17: *Output voltage as a function of designed resistor ratio measured at 25 °C on devices on wafer 4 (Process 5c).*

The sensitivity increased from 13.13 μV·°C^{-1} to 21.44 μV·°C^{-1} when compared with the batch that produced results shown in Fig. 6.4.14 – 6.4.15, but is insignificant if compared with the first iteration of devices with as-designed 200 nm-thick annealed platinum. Devices measured on the current wafer had poorest of all shown distributions from both characteristics because of the diagonal mismatch, which resulted in both a decrease and increase of measured parameters for devices positioned on different chips across the wafer. Because sheet resistance test structures were accessible on this wafer, two test structures were measured for each film and the resulting plots are shown in Fig. 6.4.19 and 6.4.20.

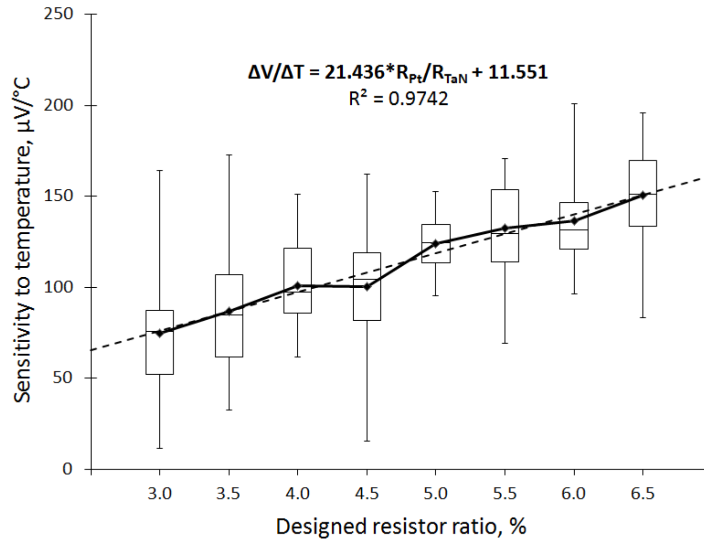

Figure 6.4.18: *Measured temperature sensitivity against designed resistor ratio of devices on wafer 4 (Process 5c).*

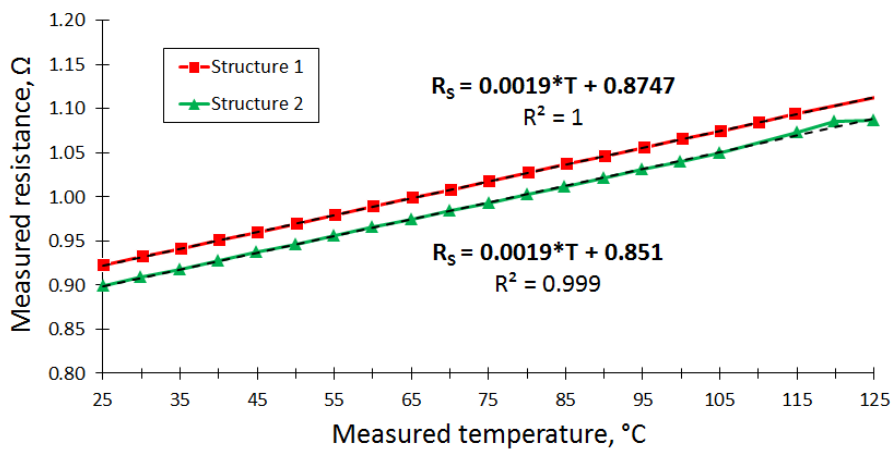

Figure 6.4.19: *TCR measurement of annealed 240 nm-thick evaporated Pt covered by PECVD oxide (Process 5c).*

From (4.9) the TCR of platinum thin film measured in two locations on the wafer was found to be:

$$\alpha_1 = \frac{1.906 \times 10^{-3}}{0.87470} \approx 2179.2 \left[\frac{ppm}{°C} \right]; \qquad \alpha_2 = \frac{1.907 \times 10^{-3}}{0.85104} \approx 2240.4 \left[\frac{ppm}{°C} \right] \tag{6.12}$$

for test structures positioned 6 mm from the centre of the wafer and spaced apart horizontally by 12 mm, as illustrated by the yellow squares in Fig. 6.4.21.

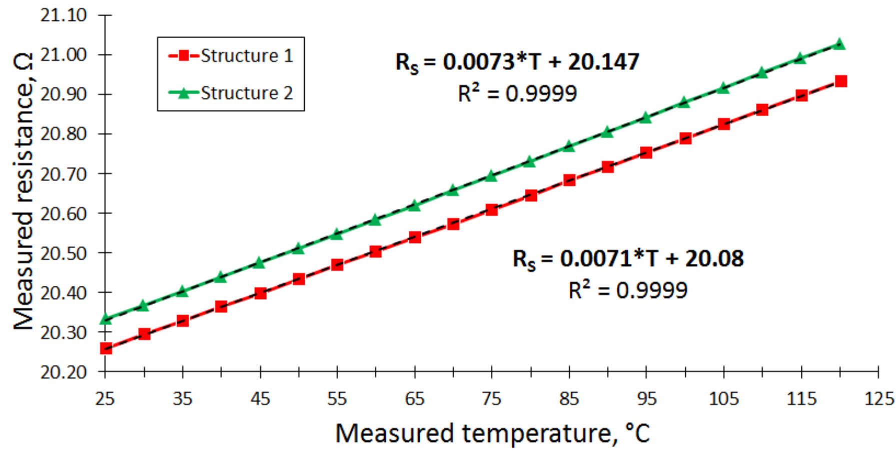

Figure 6.4.20: *TCR measurement of annealed 200 nm-thick sputtered TaN covered by PECVD oxide (Process 5c).*

Similarly,

$$\alpha_1 = \frac{7.104\times10^{-3}}{20.07958} \approx 353.8\left[\frac{ppm}{°C}\right]; \qquad \alpha_2 = \frac{7.344\times10^{-3}}{20.14648} \approx 364.5\left[\frac{ppm}{°C}\right] \qquad (6.13)$$

were measured TCR values of TaN film determined using test structures positioned 6 mm from the centre of the wafer and spaced apart vertically by 12 mm, as illustrated by the orange chips in Fig. 6.4.21.

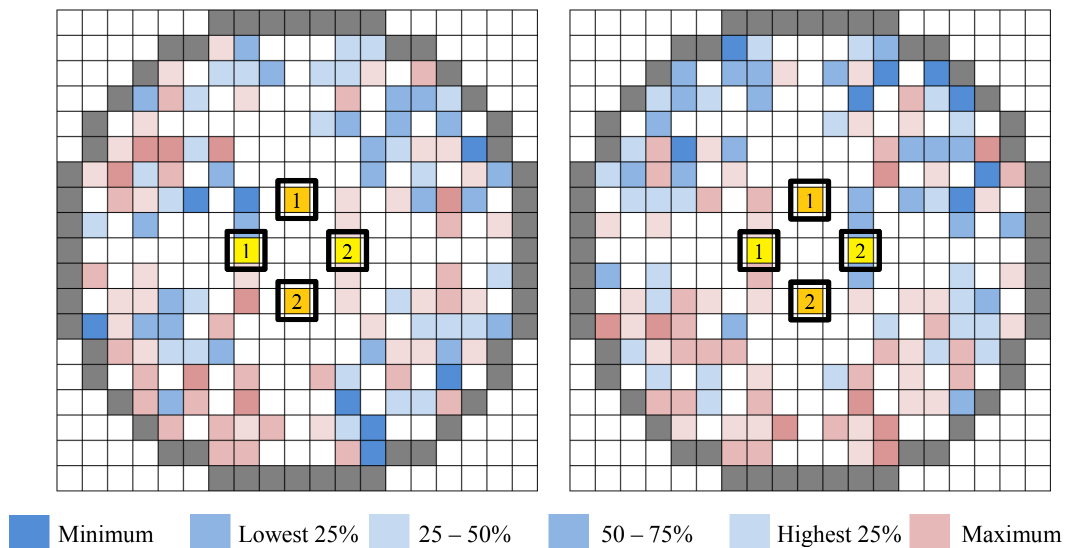

Figure 6.4.21: *Wafer maps of (a) measured start of output range and (b) sensitivity values demonstrated in Fig. 6.4.17 and 6.4.18 and detailed in Table B.2.2.*

The extracted platinum TCR was rather low because the measured 240 nm thickness was significantly lower than expected, with at least 10-15 nm of the stack produced by the TaN adhesion layer. The sheet resistance of TaN was much higher than expected as demonstrated in Appendix B.2.1 and TCR was positive, but fortunately, small. The reason for this was a deviation from expected outcome of the 600 °C vacuum annealing process. As a result, an increase in TCR of platinum film was counteracted by positive TCR of the TaN, which produced sensors with a lower sensitivity than expected. It is important to note here that the *'designed resistor ratio'* parameter targeted set sheet resistance values for both materials and a direct comparison between measured characteristics was used only for illustrative purposes.

As demonstrated by measurement data from devices on wafers that have been annealed, the sensor response to the temperature is affected, if not determined, by the platinum integrity (step coverage) because it produces parasitic resistive elements around steps over TaN features. Each sensor inevitably has two such elements in each arm of the bridge measurement circuit. Whereas parameters of thin films such as sheet resistance (which set the resistance ratio) and TCR define the most important characteristics of temperature response, any mismatch produced by parasitic elements affect the measured characteristics as identified by the shift of the output range towards negative values. The response of a significant number of measured sensor devices started with negative output voltage in the temperature range. An attempt to increase the thickness of Pt layer (from 135 nm to 240 nm as measured by profilometer) and decrease the importance of step coverage by platinum was unproductive.

Wafer map of measurements shown in Fig. 6.4.21, indicate there is not much demonstrable evidence that the sensor response to temperature depended on the position on the wafer. The temperature response of selected sensors (marked with circles on Fig. 6.4.21) is demonstrated and discussed in Appendix B.2.2.

6.5 Conclusions

Improved layout design of integrated temperature sensors and microfabrication process flow has resulted in improved yield of test structures formed between tantalum nitride and platinum layers and significantly decreased the processing time required to produce integrated devices. The most evident drawback of the redesigned integrated process that did not use a separation layer was inevitable redeposition of some Pt debris onto already-fabricated structures during lift-off process. The test setup used for characterisation has also undergone significant improvements reflecting the changes in the design of test structures and temperature sensors and also alleviating identified problems with reproducible probing to contact pad arrays across an increased temperature range.

The designed test structures that enabled the estimation of the degree of parasitic resistance introduced during fabrication of the integrated sensor were successfully measured. It was found that resistance values measured on fabricated test structures were primarily defined by the integrity of platinum layer covering features produced in 200-nm thick underlying TaN layer. With a target 200 nm for both conducting layers in annealed condition, it was found that the average effect of each step in the bottom layer on the measured Pt line resistance was 55.8 **Ω**. The effect of overlap between two conductors on the measured resistance could not be explained as a parallel combination of the two layers and was most likely related to cracks in Pt layer similarly to that identified by electrical and SEM measurements. Increasing the thickness of Pt also reduced the yield of step resistance test structures drastically, but also decreased the average measured step resistance to 7.73 Ω as measured on 5 working structures positioned at the bottom of wafer with TaN and Pt films in as-deposited condition.

It was found that measured contact resistance depends not only on the designed contact area, but again – on the step coverage of platinum layers covering TaN features near the contacts as demonstrated by the measured resistance values from both TLM-type and CBKR-type test structures. From measurements performed on different contact resistance structures it was identified that the measured resistance values were changing significantly with different platinum deposition runs. For

example, it was found using an annealed wafer with as-designed 200 nm thick Pt that the extrapolated contact resistance value in TLM-type test structures for 10×10 μm^2 designed contact area was 93.35 Ω while in CBKR-type test structures the average contact resistances were found to be 104.6 Ω for 15×15 μm^2 contact area and 90.1 Ω for 20×20 μm^2 contacts. When platinum thickness was increased to as-designed value of 400 nm wafers with annealed films have not produced any useful TLM test structures, but at the same time average contact resistance values obtained from CBKR test structures were significantly lower and were equal to 3.17 and 2.94 Ω for 15×15 μm^2 and 20×20 μm^2 test structures.

Measurements of test structures produced a lot of useful yield data. For example, measurements on CBKR test structures have demonstrated that their yield depended explicitly on step coverage performance of Pt track over the probe pad. An integrity check of TaN track passed 100% whereas a failed integrity check of the Pt track always resulted in inability to measure the test structure. Also the measured resistance on working contact resistance test structures did not have a large dependence on their designed area probably due to the different perimeter of step coverage. This assumption is also supported by demonstrated yield of test structures with different widths (27.9% and 39.1% for W = 15 against 34.6% and 43.5% for W = 20 µm).

The yield of fabricated sensors was extremely high given the low yield of the measured test structures. The primary cause for this most likely is longer sidewall perimeter and the fact that it is distributed in two planes for contact areas between TaN and Pt in sensor design. Although the level of parasitic resistance introduced into the balancing circuit at the point where Pt resistors are electrically connected to TaN resistors was rather high, every validated sensor response to temperature was within a predictable range of starting output voltage and sensitivity. The most successful set of sensor devices was produced during the initial run of the improved integrated microfabrication process, where sensor devices fabricated from annealed films had on average a sensitivity of 166.55 $\mu V \cdot °C^{-1}$ per percent of designed resistor ratio. As an example, an average sensitivity of 982.79 $\mu V \cdot °C^{-1}$ was measured on 15 devices (out of 16 fabricated) for 6% designed ratio, which is comparable with the

results produced by a hybrid bridge demonstrated in Chapter 5. A second attempt of the same process was not as successful, producing a sensitivity at least ten times less. Increasing the thickness of platinum did not help as mismatch evidently present in every device produced using annealed films has only increased, which was demonstrated by the starting voltage of output range taking negative values. As a result, it can be concluded that the mismatch of balancing resistors produced by parasitic resistance was more important for resultant device characteristics than the distribution of sheet resistance and TCR across the wafer. Nevertheless, parameters of response to the temperature can be tuned close to expected values if effects such as step coverage and integrity of evaporated platinum film on the resistance of balancing circuit in the bridge can be diminished.

References

[1] K. Seshan, D. J. Schepis, and L. B. Rothman, "Organic Dielectrics in Multilevel Metallization of Integrated Circuits," in *Handbook of Thin Film Deposition*, K. Seshan, Ed. 2nd ed., Oxford, UK: William Andrew Publishing, 2002, pp. 513-594.

[2] D. K. Schroder, "Contact Resistance and Schottky Barriers," in *Semiconductor Material and Device Characterization*, 3rd ed., Hoboken, USA: Wiley-IEEE Press, 2006, pp. 127-184.

[3] M. Bhushan and M. B. Ketchen, "Resistors," in *Microelectronic Test Structures for CMOS Technology*, New York, USA: Springer-Verlag, 2011, pp. 67-106.

[4] H. Lin, S. Smith, J. T. M. Stevenson, A. M. Gundlach, C. C. Dunare, and A. J. Walton, "An evaluation of test structures for measuring the contact resistance of 3-D bonded interconnects," *Microelectronic Test Structures (ICMTS), 2008 International Conference on,* pp. 123-127, 2008.

Chapter 7 Conclusions and further work

7.1 Summary of results

Processes for the deposition, annealing and patterning of tantalum nitride and platinum thin films have been developed. These have been demonstrated to produce films with the desired values of resistance and temperature coefficients of resistance. These values remained stable after subsequent annealing processes, once they have been vacuum annealed for at least 5 hours at 600 °C. As-deposited evaporated platinum thin films were polycrystalline while as-deposited reactively sputtered TaN films were amorphous, as determined by thin film X-ray diffraction (GIXRD). Annealed TaN thin films produced by a 10% nitrogen process consisted of a mixture of Ta_2N and under-stoichiometric phases, and these films were used to fabricate resistors on chips that were combined with platinum resistors on another substrate to produce a hybrid bridge temperature transducer. TaN thin films deposited with a 12% N_2 component in gas flow stayed amorphous after vacuum annealing and were used as a part of an integrated microfabrication flow because they exhibit better sheet resistance and TCR stability as compared to TaN film produced by different nitrogen flow ratio processes. This process was subsequently used to produce 10-15 nm TaN adhesion layers for evaporated platinum thin films for monolithically integrated sensors.

Pairs of thin film resistor chips containing two Pt and four TaN resistors with a designed resistor ratio of around 6% were packaged and arranged into a bridge configuration. The output from the hybrid bridge was measured using an

instrumentation amplifier with set gain of 10. This circuit produced a temperature response with a sensitivity of 844 μV·°C^{-1} in a measured range of 25 to 100 °C with a 1 V excitation voltage applied. An integrated process and layout were then designed, where platinum resistors contacted TaN resistors through vias in an interlayer silicon oxide dielectric. Contact resistance test structures were used to estimate the effect of the evaporated platinum process on the integrity of contacts and platinum layer step coverage issues were identified, which suggested improvements that were required in the integrated sensor design.

An improved layout design and microfabrication flow has enabled measurements of parasitic elements introduced by thin film platinum step coverage when it was deposited on top of TaN features. It was found using measurements of test structures that the performance of fabricated sensors would be heavily affected by parasitic resistances. Temperature sensors with 3% to 6.5% designed resistor ratio (R_{Pt}/R_{TaN}) were measured using a 15 V bridge excitation voltage. The initial improved run of the integrated process has produced temperature sensors with sensitivity values of respectively 58.5 and 166.6 μV·°C^{-1} (per percent of designed resistor ratio) when films were in non-annealed and annealed conditions. A second run of an identical process, where films have been annealed, has resulted in production of devices with temperature response of 13.13 μV·°C^{-1} (per percent of designed resistance ratio). Increasing platinum thickness did not solve the problem of manufacturability of Pt/TaN contacts and resulted in a measured sensitivity of 21.44 μV·°C^{-1} (per percent of designed ratio).

7.2 Conclusions

7.2.1 High temperature thin film materials

Thin film platinum and tantalum nitride microfabrication processes have been developed to produce sets of resistors which are respectively highly sensitive or practically insensitive to temperature. The temperature sensitivity of TaN affects the response of the half-bridge circuit with a more negative temperature coefficient of TaN resulting in a higher apparent sensitivity to temperature. Tantalum nitride was

produced from a pure tantalum target by reactive sputtering at room temperature and a thickness of 200 nm was found to be optimum for further development due to suitable sheet resistance values and increased stability during subsequent high temperature vacuum annealing. The nitrogen:argon flow ratio used for the sputtering process significantly affected the electrical characteristics of the TaN thin film, particularly since the ratio could only be controlled with a 2% precision.

Two TaN processes with flow ratio settings of 10% and 12% were developed that offered a TCR close to zero. Higher ratio films were shown to have more negative TCR values. The first process resulted in a film with a very low, negative TCR value that becomes a low, positive value during vacuum annealing at 600 C°. The drawback of thin films produced by this process was a demonstrable variation of sheet resistance that occurred during the annealing process. The 12% nitrogen process offered a very stable tantalum nitride thin film with a constant TCR of approximately –150 ppm $°C^{-1}$. As confirmed by XRD measurements, the range of the temperatures and times of the vacuum annealing process used were insufficient to create a change in the phase composition of the as-deposited, variably-oriented thin film.

Thin film platinum deposited by e-beam evaporation at room temperature was polycrystalline regardless of which adhesion layer was used in this study. This adhesion layer was needed because the adhesion of platinum to silicon oxide is poor. A TaN adhesion layer was conveniently found to be optimal and the TCR of a 100 nm thick Pt on TaN adhesion layer was observed to increase as a result of vacuum annealing process due to improved crystallinity of the platinum.

The development of TaN and Pt thin films detailed in Chapter 4 represents significant groundwork for further development of an integrated microfabrication process. The processes developed should be compatible with post-CMOS integration with the target instrumentation amplifier based on the temperature budget used. Annealing temperature values were selected due to the increased stability they offer, and as both TaN and Pt films would be expected to have better stability when deposited at higher temperatures, annealing processes could be optimised to further decrease the temperature budget of film processes.

7.2.2 High temperature sensors produced from thin films

A hybrid bridge device was built using discrete fabricated TaN and Pt element chips and connected to an instrumentation amplifier providing a gain of 10. The sensitivity, measured in a limited temperature range, was 844 $\mu V \cdot °C^{-1}$ and was mainly determined by the TaN and Pt resistor values and their TCR. TaN resistors were produced by a 10% nitrogen flow ratio process and a similar shorter process was used to deposit the adhesion layer for Pt. The TCR value of 100 nm-thick Pt temperature sensitive elements produced on TaN adhesion layer was around 1340 ppm $°C^{-1}$ while the TCR of TaN balancing resistors was close to zero.

The initial layout design used TaN and Pt thin film layers to build temperature sensing devices with an additional aluminium interconnect layer and interlayer dielectric layers of 500 nm of PECVD oxide. The integrated microfabrication process involved steps of deposition, patterning and processing of all layers, but this failed to produce reliable contacts between Pt (100 nm) and TaN (200 nm) layers, as demonstrated by numerous contact resistance test structure measurements. The specific contact resistance between Pt and TaN could not be estimated due to poor integrity of the layer of evaporated Pt surrounding vias down to the TaN. Sputtered 200 nm TaN produced better measurable contacts to lower layer TaN features through vias because these layers had specific contact resistance of 1349.7 $\Omega \cdot \mu m^2$ and extrapolated contact resistance as low as 258 mΩ when A tends to infinity. As a result of contact reliability improvement and process optimisation, the dielectric between TaN and Pt was removed and a lift-off process was developed to pattern a 200 nm-thick Pt film layer. Sputtered 200 nm Pt was also found to produce more reliable direct contact with TaN when compared to results produced using evaporated 200 nm Pt. Unfortunately, in the current process the wafers with sputtered Pt could not be annealed due to the possibility of contaminating the vacuum furnace.

The microfabrication process improvements required a re-design of the layout and the new design included test structures that helped in estimating the effect of parasitic resistive elements introduced by non-conformal platinum film coverage of steps produced by TaN elements. The improved process flow resulted in better yield

for test structures formed between tantalum nitride and platinum layers. The most evident drawback of the process without the dielectric layer was the redeposition of Pt film debris onto already-fabricated TaN structures. Test structures measured using improved test automation enabled the analysis of the thin film platinum process yield. For example, contact chain structures were measured on every fabricated wafer with accessible test structures, but the measured resistances (> 13 kΩ for a set of four step and four contacts) were much higher than expected. From measurements performed on TLM-type and CBKR contact resistance structures it was concluded that the measured resistance values were changing with different platinum deposition and vacuum annealing runs and that the test structure yield depended explicitly on step coverage performance of narrow Pt tracks over the TaN features. The effect of overlap between features in Pt and TaN layers in step resistance test structures could not be explained as a parallel combination of the two layers and was most likely related to cracks in Pt layer which were discovered later by SEM measurements.

The most successful set of sensor devices was produced during the initial run of the integrated microfabrication process, where sensor devices fabricated from annealed 200 nm TaN and 200 nm Pt films had, on average, a sensitivity of 166.55 $\mu V \cdot {}^{\circ}C^{-1}$ per percent of designed resistor ratio, which is a result that is comparable with that produced by the hybrid sensor. Another batch using exactly the same process has produced sensors which are at least ten times less sensitive. Increasing the platinum thickness to 400 nm was expected to produce a film that would completely cover 200 nm-thick TaN features. However, the inconsistency of the platinum process resulted in a measured thickness value below 250 nm and reduced the yield of step resistance test structures drastically. The yield of the sensors was high given the low yield for the multilayer test structures on the same wafer. Step coverage was apparently not as critical for sensor devices, however due to the variability of parasitic elements in the circuit, the mismatch in fabricated devices has increased and as a result the measured temperature sensitivity and full-scale output range suffered. The expected temperature sensitivity values should be obtained from devices produced by the integrated process if the issues with the quality of the platinum films can be improved.

7.3 Future work

The fabrication processes developed here have allowed the production of films that meet the required criteria for nominal resistance and stability, but they are not the most optimal processes that should be available using this deposition equipment. The platinum sidewall coverage issue was not resolved by decreasing the step height or increasing the platinum thickness. This resulted in significant parasitic effects in sensor devices, and the final option to be considered is platinum deposition by sputtering on a planar surface.

7.3.1 Solution of platinum sidewall coverage problem

It is clear that this issue needs to be solved, as indicated by the poor yield of electrical test structures designed to study step coverage as well as the measured temperature transducer characteristics. The most recent fabrication process used lift-off patterning that decreased the maximum step height from 500 to 200 nm and deposition of 400 nm (target thickness) platinum films, but the problems with step coverage by platinum still persisted. Many of the integration issues, such as platinum step coverage, would not have existed if a proper sputtered Pt process was available. If platinum can only be produced by evaporation the most effective solution would be to use a planar surface for platinum deposition. This would require a redesign of layout, but would allow deposition of platinum as the first layer in the stack with TaN. Depositing thin film tantalum nitride as a second layer has been demonstrated in section 5.5.2 to be a better option to provide connection with an underlying tantalum nitride thin film and would be expected to provide high yield connections. However, it would be practical to confirm this using the latest test structures described in section 6.2.2. The proposed fabrication process that should solve step coverage issues is illustrated in Fig. 7.3.1.

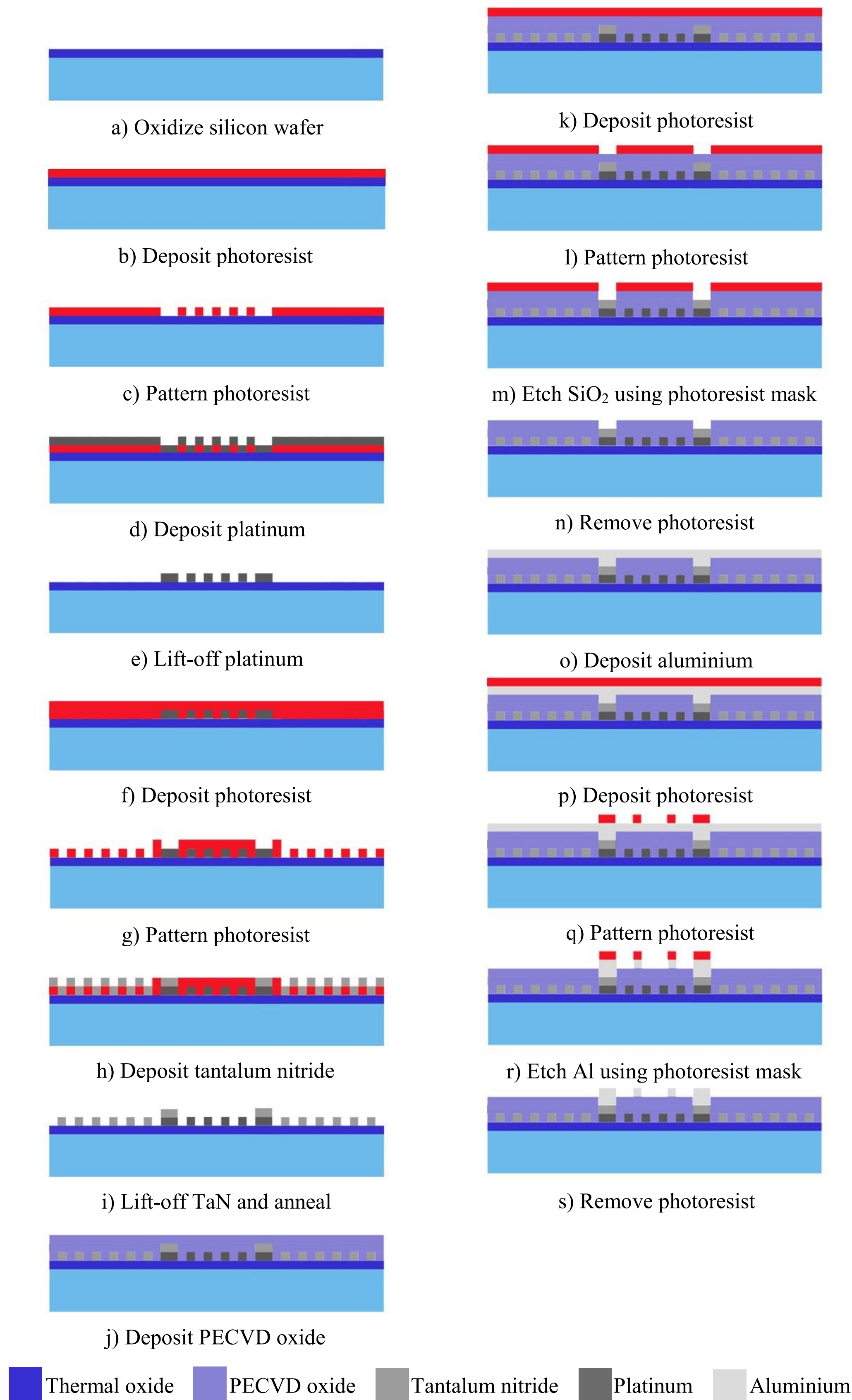

Figure 7.3.1: *Integrated process: platinum is deposited first on a planar surface*

Lift-off patterning of platinum and tantalum nitride may result in incomplete removal or debris of metal film, as shown in Fig. 6.3.4, and this can negatively affect the performance of produced devices. In this work lift-off was used for demonstration purposes only and is not considered as a semiconductor industry process, which may cause implications in integration of thin film patterning processes with those used to produce the integrated circuit. In order to avoid this, the two metal layers may be separated with a thinner, for example – 250 nm, PECVD oxide layer, similar to a process design proposed and evaluated in Chapter 5, and both films and the dielectric layer can then be dry etched. This would require redevelopment of the platinum etch process and that could also affect the characteristics of TaN films produced by the reactive sputtering process and would have to be evaluated by experiments similar to those detailed in Chapter 4.

7.3.2 Improvement of thin film electrical parameters

In addition to improvements suggested in section 7.3.1, both platinum and tantalum nitride deposition and annealing processes can be subject to further optimisation. The vacuum annealing process (600 °C, 6 hours) that was eventually applied to both films was developed to produce low temperature coefficient of resistance tantalum nitride and was primarily targeting sputtering processes with nitrogen flow ratio settings of 10% and 12%. X-ray diffraction measurements in Chapter 4 have revealed that annealing at 600 °C did not produce significant crystallographic changes in TaN films produced with the 12% process. Increasing temperature to study the effect of annealing at higher temperatures on TaN films would be of interest, but it would be impractical for integration due to increased process thermal budget and the expectation that platinum thin film characteristics would deteriorate [1-3]. Temperatures in the range of 500 to 550 °C were shown to be optimal for both metal films in some literature sources, and it may be possibly with further investigation to find temperatures and annealing times that better match the required effect on thin film electrical performance [3-6]. Additional experiments would be required to confirm how new annealing parameters affect the resistance, TCR and stability of thin film TaN. Furnaces can be set to start and end the annealing

process at room temperature to have a more controllable effect of thermal expansion as a part of the process.

Nitrogen flow for the reactive sputtering process was set with a precision of 1 sccm in 50 sccm total argon, with a minimum available setting of 5 sccm resulting in 10% expected flow ratio. It should also be possible to adjust the total flow value between 49 and 42 sccm which would result in finer control of the flow ratio (for 5 sccm nitrogen flow) between 10% and 12%. In addition, different chamber pressure settings would be expected to produce a variety of films with different deposition rates and resulting resistance parameters. As a result of further optimisation of TaN process parameters, films that better fulfil sheet resistance stability and low TCR criteria could be produced. It should also be ensured that platinum is produced from as pure grade material as possible in an evaporation process and confirmed by thin film chemical composition measurement and analysis tools. With the availability of high temperature probes for the semi-automatic prober, thin films can be characterised over a wider temperature range, with platinum film TCR being of particular interest due to possible non-linearities at higher temperatures [7]. Finally, a proper stability test to study the irreversible effects of corrosion on stability of produced devices can be performed. Once thin film deposition and processing parameters are optimised, a new sensor design can be produced that would be enhanced for new sheet resistance values and TCR. The wafer layout could then contain a single sensor design with necessary resistance ratio that would enable the fabrication of devices with characteristics which would only be affected by sheet resistance and TCR uniformity of metal thin film processes and some parasitic resistances.

7.3.3 An outline fabrication process for integration on SiC electronics

The results of measurements of the integrated sensors and test structures, along with the suggested improvements to the fabrication process, have been described in Chapter 6. These are capable of providing a sensor with the full-scale temperature response and sensitivity required for the desired applications. This subsection will concentrate on setting out a production process for an integrated sensor based on the

original application for post-processed high temperature sensor for SiC electronics. It is assumed at this stage that dry etching will be used to pattern all deposited layers, avoiding lift-off processes.

The first process step is deposition of platinum on the planarized surface of the foundry substrate. The substrate should be loaded at room temperature and ramped slowly to the deposition temperature. Thin film platinum should be preferably sputtered in argon at a temperature of around 340 °C [3]. Platinum evaporation may result in improved TCR but sputtering would be preferred when lower resistance drift and higher deposition uniformity are required, which would be most important selection criteria for this project [8]. The platinum thickness of around 200 nm should be easily etched by an argon mill process, similar to one developed for the current research project.

If the tantalum nitride is to be dry etched, there will be a requirement to protect the Pt from this process using an interlayer dielectric such as PECVD oxide. This layer can be as thin as 250 nm using a suitable design such as that shown in Fig. 6.2.2, where no intersections of Pt and TaN layers occur apart from where there are contacts. Contacts to Pt resistive elements through vias in PECVD oxide can be created using the CHF_3 + Ar RIE process described in Appendix A. Wafer should be ramped slowly from room temperature (ramp rates less than 5 $°C \cdot min^{-1}$) to the TaN deposition temperature of 300 °C and back again [9]. There is no requirement for a compound tantalum nitride target because it has been shown in this work that TaN with a low negative TCR can be produced through a reactive sputtering process, for example using a 12% nitrogen flow ratio process. TaN can be patterned by the CF_4 + O_2 dry etching process developed in this project.

Once TaN and Pt are deposited and patterned, a vacuum anneal in the temperature range of 450 – 500 °C should follow. Temperature ramping must be slow and uniform and performed from room temperature. Similar ramping conditions have to be ensured during deposition of PECVD oxide passivation, where the substrate temperature is ramped up to 250 °C. Once a protection layer is deposited, a vacuum annealing process at 300 – 350 °C for at least 2 hours can be used to further stabilise the films.

As a result of this integrated deposition, patterning and annealing process it can be expected that thin film elements with linear temperature sensitivity of the order of 2200 – 2500 ppm $°C^{-1}$ for platinum and between –200 and 100 ppm $°C^{-1}$ for tantalum nitride can be produced. Deposition at higher temperatures is expected to further decrease drift of sheet resistance and TCR values as compared to results obtained in this work.

7.4 Final conclusions

This study demonstrates how a combination of temperature sensitive and temperature insensitive material elements is utilized to produce an integrated half-bridge that can measure high temperatures. Thin film elements deposited in different layers are produced using PVD processes and a similar approach can be used to monolithically integrate the sensor with an instrumentation amplifier fabricated in underlying layers.

This thesis has described the development of thin film manufacturing and annealing processes using a variety of resistive test structures that produce elements with reasonable high temperature stability, as demonstrated both by resistance and crystallographic measurements. Initial demonstration of the temperature measurement principle was performed using a hybrid device consisting of bonded platinum and tantalum nitride chips. Issues identified with the manufacturability of platinum thin film elements on a non-planar surface were partially solved by producing platinum elements in direct contact with tantalum nitride thin film resistors. If the step coverage and integrity of evaporated platinum can be improved, it should be possible to bring the key parameters of the sensor response (sensitivity and reference output at T_{REF}) close to the expected design values. The advantages of this sensor as a miniaturised device capable of monolithic integration with high temperature electronics would then become clear.

References

[1] F. Mailly *et al.*, "Anemometer with hot platinum thin film," *Sensors and Actuators A: Physical,* vol. 94, no. 1-2, pp. 32-38, 2001.

[2] U. Schmid and H. Seidel, "Influence of thermal annealing on the resistivity of titanium/platinum thin films," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 24, no. 6, p. 2139, 2006.

[3] R. M. Tiggelaar, R. G. P. Sanders, A. W. Groenland, and J. G. E. Gardeniers, "Stability of thin platinum films implemented in high-temperature microdevices," *Sensors and Actuators A: Physical,* vol. 152, no. 1, pp. 39-47, 2009.

[4] N. D. Cuong, N. M. Phuong, D.-J. Kim, B.-D. Kang, C.-S. Kim, and S.-G. Yoon, "Effect of annealing temperature on structural and electrical properties of tantalum nitride thin film resistors deposited on SiO_2/Si substrates by dc sputtering technique," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 24, no. 2, p. 682, 2006.

[5] N. D. Cuong, D.-J. Kim, B.-D. Kang, C.-S. Kim, and S.-G. Yoon, "Effect of film thickness on the electrical properties of tantalum nitride thin films deposited on SiO_2/Si substrates for Π-type attenuator applications," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures,* vol. 24, no. 3, p. 1398, 2006.

[6] N. D. Cuong, D.-J. Kim, B.-D. Kang, and S.-G. Yoon, "Structural and electrical characterization of tantalum nitride thin film resistors deposited on AlN substrates for π-type attenuator applications," *Materials Science and Engineering: B,* vol. 135, no. 2, pp. 162-165, 2006.

[7] F. Lacy, "Using Nanometer Platinum Films as Temperature Sensors (Constraints From Experimental, Mathematical, and Finite-Element Analysis)," *IEEE Sensors Journal,* vol. 9, no. 9, pp. 1111-1117, 2009.

[8] J. J. Licari and L. R. Enlow, "Thin Film Processes," in *Hybrid Microcircuit Technology Handbook: Materials, Processes, Design, Testing and Production*2nd ed. Westwood, USA: Noyes Publications, 1998, pp. 63-103.

[9] N. D. Cuong, D.-J. Kim, B.-D. Kang, C. S. Kim, K.-M. Yu, and S.-G. Yoon, "Characterization of Tantalum Nitride Thin Films Deposited on SiO_2/Si Substrates Using dc Magnetron Sputtering for Thin Film Resistors," *Journal of The Electrochemical Society,* vol. 153, no. 2, pp. G164-G167, 2006.

Appendix A Runsheets of initial microfabrication process flow

Table A.1 *Detailed summary of initially designed microfabrication flow.*

Fabrication step	***Tool and parameters***		***Process consumables***	
	Name	*Process details*	*Name(s)*	*Process purpose*
1. Oxidize silicon wafers	Furnace 10	1400 °C, 40 min, 1.7 slm O_2, 3 slm H_2, 1 atm	O_2, H_2	Electrical passivation of silicon
2.1. Deposit thin film TaN	OPT Plasmalab System 400 sputterer	500 W, 44 sccm Ar, 6 sccm N_2, 90 min	Ar, N_2, Ta target	Temperature-insensitive layer
2.2. Anneal TaN	HITEC 8” tube nitride furnace	600°C, 5 hours, vacuum	–	Crystallization, phase transformation
2.3. Deposit and pattern resist	SVG 8600 and Karl Suss MA8	SPR 350, 1.5 µm, 7.5 sec exp.	HMDS, SPR350, TMAH	Etch selectivity to TaN features
2.4. Dry etch TaN	JLS RIE 80	150 mTorr, 50 W, 60 sccm CF_4, 3 sccm O_2, 30 min	CF_4, O_2	Develops features in TaN
2.5. Remove resist	Electrotech 508 Barrel Asher	60 min	O_2	Reveals non-etched TaN
3.1. Deposit PECVD oxide	STS PECVD tool	550 mTorr, 60 W, 392 sccm N_2, 1420 sccm N_2O, 12 sccm SiH_4	N_2, N_2O, SiH_4	Electrical separation of TaN and Pt features
3.2. Deposit and pattern resist	SVG 8600 and Karl Suss MA8	SPR 350, 1.5 µm, 9 sec exp.	HMDS, SPR350, TMAH	Etch selectivity to vias in PECVD oxide
3.3. Dry etch PECVD oxide	JLS RIE 80	30 mTorr, 100 W, 17.7 sccm CHF_3, 20.1 sccm Ar, 35 min	CHF_3, Ar	Vias between TaN and Pt features
3.4. Remove resist	Electrotech 508 Barrel Asher	60 min	O_2	Reveals non-etched SiO_2
4.1. Deposit thin film Pt	ANS Cluster Tool	100 nm	Pt pellets	Temperature-sensitive layer
4.2. Anneal Pt	HITEC 8” tube nitride furnace	600°C, 12 hours, vacuum	–	Recrystallization
4.3. Deposit and pattern resist	SVG 8600 and Karl Suss MA8	SPR 350, 1.5 µm, 7.5 sec exp.	HMDS, SPR350, TMAH	Etch selectivity to Pt features

4.4. Dry etch Pt	STS RIE	30 mTorr, 30 W, 25 sscm Ar, 40 min	Ar	Develops features in Pt
4.5. Remove resist	Electrotech 508 Barrel Asher	60 min	O_2	Reveals non-etched Pt
5.1. Deposit PECVD oxide	STS PECVD tool	550 mTorr, 60 W, 392 sccm N_2, 1420 sccm N_2O, 12 sccm SiH_4	N_2, N_2O, SiH_4	Electrical separation of Pt and Al features
5.2. Deposit and pattern resist	SVG 8600 and Karl Suss MA8	SPR 350, 1.5 µm, 9 sec exp.	HMDS, SPR350, TMAH	Etch selectivity to vias in PECVD oxide
5.3. Dry etch PECVD oxide	JLS RIE 80	30 mTorr, 100 W, 17.7 sccm CHF_3, 20.1 sccm Ar, 35 min	CHF_3, Ar	Vias between Pt and Al features
5.4. Remove resist	Electrotech 508 Barrel Asher	60 min	O_2	Reveals non-etched SiO_2
6.1. Deposit thin film Al	OPT Plasmalab System 400 sputterer	1000 W, 50 sccm Ar, 45 min	Ar, Al target	Demonstrational interconnect layer
6.2. Deposit and pattern resist	SVG 8600 and Karl Suss MA8	SPR 350, 1.5 µm, 5 sec exposure	HMDS, SPR350, TMAH	Etch selectivity to Al features
6.3. Dry etch Al	STS RIE	100 mTorr, 60 W, 37.5 sccm $SiCl_4$, 15 sccm Ar, 25 min	$SiCl_4$, Ar	Develops features in Al
6.4. Remove resist	Electrotech 508 Barrel Asher	60 min	O_2	Reveals non-etched Al

Runsheet A.1 *Runsheet for sensor devices and test structures: initial microfabrication design.*

Step	*Description*	Equipment	Parameters
0	*Processing starts with cleaned 3" wafers covered by thermal SiO_2*		
1.1.	**Metallization (TaN)**	**OPT Plasmalab**	**3×30 min, 3 mTorr, 500 W, 44 sccm Ar, 6 sccm N_2**
1.2.	**Cleaning**	**Wet bench**	**Clean with air gun**
1.3.	**Annealing**	**Furnace 3**	**5 hours, 600 °C, vacuum – Load at 200 °C**
1.4.	**Cleaning**	**Wet bench**	**Clean with air gun**
1.5.	**Photolithography: Metal dry etch**	**Mask 1**	
1.5.1.	Resist coat	SVG Track 1	Prime, spin-coat 1.5 µm SPR350, soft bake
1.5.2.	Resist expose	KS MA 8	Hard contact, 7.5 seconds exposure
1.5.3.	Resist develop	SVG Track 2	Develop resist and hard bake
1.6.	**Inspect**	**Microscope**	**Inspect developed features**
1.7.	**Metal etch**	**JLS RIE80**	**30 min, 150 mTorr, 50 W, 60 sccm CF_4, 3 sccm O_2**
1.8.	**Inspect**	**Microscope**	**Inspect resist condition**

1.9.	**Resist strip**	**Barrel Asher**	**Plasma etch for 60 minutes**
1.10.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**
2.1.	**Passivation (SiO_2)**	**STS PECVD**	**8 min, 500 nm *LFSiO***
2.2.	**Photolithography: Oxide dry etch**	**Mask 2**	
2.2.1.	Resist coat	SVG Track 1	Prime, spin-coat 1.5 μm SPR350, soft bake
2.2.2.	Resist expose	KS MA 8	Hard contact, 9 seconds exposure
2.2.3.	Resist develop	SVG Track 2	Develop resist and hard bake
2.3.	**Inspect**	**Microscope**	**Inspect developed features**
2.4.	**Oxide etch**	**JLS RIE80**	**35 min, 30 mTorr, 100 W, 17.7 sccm CHF_3, 20.1 sccm Ar**
2.5.	**Inspect**	**Microscope**	**Inspect resist condition**
2.6.	**Resist strip**	**Barrel Asher**	**Plasma etch for 60 minutes**
2.7.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**
3.1.	**Metallization (TaN)**	**OPT Plasmalab**	**4 min, 3 mTorr, 500 W, 45 sccm Ar, 5 sccm N_2**
3.2.	**Cleaning**	**Wet bench**	**Clean with air gun**
3.3.	**Metallization (Pt)**	**ANS**	**100 nm**
3.4.	**Cleaning**	**Wet bench**	**Clean with air gun**
3.5.	**Annealing**	**Furnace 3**	**12 hours, 500 °C, vacuum – Load at 200 °C**
3.6.	**Cleaning**	**Wet bench**	**Clean with air gun**
3.7.	**Photolithography: Metal dry etch**	**Mask 3**	
3.7.1.	Resist coat	SVG Track 1	Prime, spin-coat 1.5 μm SPR350, soft bake
3.7.2.	Resist expose	KS MA 8	Hard contact, 7.5 seconds exposure
3.7.3.	Resist develop	SVG Track 2	Develop resist and hard bake
3.8.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**
3.9.	**Dry etch**	**STS Al etcher**	**40 min, 30 mTorr, 30 W, 25 sccm Ar**
3.10.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**
4.1.	**Passivation (SiO_2)**	**STS PECVD**	**8 min, 500 nm *LFSiO***
4.2.	**Photolithography: Oxide dry etch**	**Mask 4**	
4.2.1.	Resist coat	SVG Track 1	Prime, spin-coat 1.5 μm SPR350, soft bake
4.2.2.	Resist expose	KS MA 8	Hard contact, 9 seconds exposure
4.2.3.	Resist develop	SVG Track 2	Develop resist and hard bake
4.3.	**Inspect**	**Microscope**	**Inspect developed features**
4.4.	**Oxide etch**	**JLS RIE80**	**35 min, 30 mTorr, 100 W, 17.7 sccm CHF_3, 20.1 sccm Ar**
4.5.	**Inspect**	**Microscope**	**Inspect resist condition**
4.6.	**Resist strip**	**Barrel Asher**	**Plasma etch for 60 minutes**
4.7.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**
5.1.	**Metallization (Al)**	**OPT Plasmalab**	**45 min, 3 mTorr, 1000 W, 50 sccm Ar**
5.2.	**Photolithography: Metal dry etch**	**Mask 5**	
5.2.1.	Resist coat	SVG Track 1	Prime, spin-coat 1.5 μm SPR350, soft bake
5.2.2.	Resist expose	KS MA 8	Hard contact, 5 seconds exposure
5.2.3.	Resist develop	SVG Track 2	Develop resist and hard bake
5.3.	**Inspect**	**Microscope**	**Inspect developed features**

5.4.	**Metal etch**	**STS Al etcher**	**25 min, 30 mTorr, 100 W, 17.7 sccm CHF_3, 15 sccm Ar**
5.5.	**Inspect**	**Microscope**	**Inspect resist condition**
5.6.	**Resist strip**	**Barrel Asher**	**Plasma etch for 60 minutes**
5.7.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**

Runsheet A.2 *Runsheet for test structures: improved microfabrication flow (without Pt or Ni annealing step) used to produce contact resistance test structures.*

Step	*Description*	Equipment	Parameters
0	*Processing starts with cleaned 3" wafers covered by thermal SiO_2*		
1.1. – 2.3.	*Same as in Runsheet A.1: 1.1.-2.3, but using masks 3 and 4 and annealing for 6 hours*		
2.4.	**Oxide etch**	**JLS RIE80**	**30 min, 30 mTorr, 100 W, 17.7 sccm CHF_3, 20.1 sccm Ar**
2.5.	**Inspect**	**Microscope**	**Inspect resist condition and repeat part of 2.4 if necessary**
2.6.	**Resist strip**	**Barrel Asher**	**Plasma etch for 60 minutes**
2.7.	**Inspect**	**Microscope**	**Inspect produced features, take pictures and repeat part of 2.6 if necessary**
3.1.	**Photolithography: Metal lift off**	**Mask 5**	
3.1.1.	Resist coat	SVG Track 1	Prime, spin-coat 1.5 µm AZ5214E manually, soft bake
3.1.2.	Resist expose	KS MA 8	Hard contact, 7.5 seconds exposure
3.1.3.	Resist reversal bake	SVG Track 1	Bake
3.1.4.	Resist expose	KS MA 8	Flood expose, 50 seconds exposure
3.1.5.	Resist develop	Dish	AZ726MIF for 60 seconds
3.1.6.	Resist rinse	Wet bench	Rinse with DI water and dry
3.1.7.	Inspect	Microscope	Inspect resist features
3.2.	**Metallization (TaN)**	**OPT Plasmalab**	**5 min, 3 mTorr, 500 W, 44 sccm Ar, 6 sccm N_2**
3.3.	**Cleaning**	**Wet bench**	**Clean with air gun**
3.4a.	**Metallization (Pt)**	**ANS**	**200 nm**
3.4b/c.	**Metallization (Pt)**	**ANS**	**100 nm**
3.5.	**Cleaning**	**Wet bench**	**Clean with air gun**
3.6.	**Metal lift-off**	**Wet bench**	**ACT CMIS, 15 mins, 50 °C in ultrasonic bath**
3.7.	**IPA rinse**	**Wet bench**	**IPA in ultrasonic bath, 1 min**
3.8.	**Inspect**	**Microscope**	**Inspect wafer and repeat 3.6/3.7 if necessary**
3.9.	**DI rinse**	**Wet bench**	**Rinse with DI water and dry**
3.10.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**
3.11c.	**Annealing**	**Furnace 3**	**12 hours, 500 °C, vacuum – Load at 200 °C**
3.12c.	**Cleaning**	**Wet bench**	**Clean with air gun**

Runsheet A.3 *Runsheet used to produce samples for SEM measurements.*

Step	*Description*	Equipment	Parameters
0	*Processing starts with cleaned 3" wafers covered by thermal SiO_2*		
1.1. – 1.4.	*Same as in Runsheet A.2: 1.1. – 1.4.*		
1.5a. – 1.10a.	*Same as in Runsheet A.2: 1.5. – 1.10, but using RW mask*		
2.1b.	**Passivation (SiO_2)**	**STS PECVD**	**4 min, 250 nm LFSiO**
2.1c.	**Passivation (SiO_2)**	**STS PECVD**	**8 min, 500 nm LFSiO**
2.2b/c.	**Photolithography**	**RW mask**	
2.2.1.	Resist coat	SVG Track 1	Prime, spin-coat 1.5 µm SPR350, soft bake
2.2.2.	Resist expose	KS MA 8	Hard contact, 9 seconds exposure
2.2.3.	Resist develop	SVG Track 2	Develop resist and hard bake
2.3b/c.	**Inspect**	**Microscope**	**Inspect developed features**
2.4b.	**Oxide etch**	**JLS RIE80**	**20 min, 30 mTorr, 100 W, 17.7 sccm CHF_3, 20.1 sccm Ar**
2.4c.	**Oxide etch**	**JLS RIE80**	**30 min, 30 mTorr, 100 W, 17.7 sccm CHF_3, 20.1 sccm Ar**
2.5b/c.	**Inspect**	**Microscope**	**Inspect resist condition**
2.6b/c.	**Resist strip**	**Barrel Asher**	**Plasma etch for 60 minutes**
2.7b/c.	**Inspect**	**Microscope**	**Inspect developed features and take pictures**
3.1.	**Cleaving**	**Scribe pen**	**Cleave along lines other than 1–1**
3.2.	**Cleaning**	**Wet bench**	**Clean with air gun**
3.3.	*Cover cleaved samples with evaporated gold in Edwards E306A for 5 minutes*		
3.4.	**Sidewall inspection**	**Hitachi 4700 SEM**	**Take pictures of sidewall cross-section**

Runsheet A.4 *Runsheet for fabricating test structures with direct contact between two layers.*

Step	*Description*	Equipment	Parameters
0	*Processing starts with cleaned 3" wafers covered by thermal SiO_2*		
1.1. – 1.10.	*Same as in Runsheet A.2: 1.1. – 1.10.*		
2.1.	**Photolithography: Metal lift-off**	**Mask 5**	
2.1.1.	Prime	SVG Track 1	Or use HMDS box for 10 minutes
2.1.2.	Resist coat	POLOS 150	Spin-coat 1.5 µm AZ2070
2.1.3.	Soft bake	Hotplate	90 seconds, 100 °C
2.1.4.	Resist expose	KS MA 8	Hard contact, 20 seconds exposure
2.1.5.	Post-Exposure Bake	Hotplate	60 seconds, 115 °C
2.1.6.	Resist develop	Dish	AZ726MIF for 90 seconds
2.1.7.	Resist rinse	Wet bench	Rinse with DI water and dry
2.1.8.	Inspect	Microscope	Inspect resist features
2.1.9.	Cleaning	Barrel Asher	Plasma etch for 2 minutes
2.2.	**Metallization (TaN)**	**OPT Plasmalab**	*1:* **10 min argon mill;** *2:* **5 min, 3 mTorr, 500 W, 44 sccm Ar, 6 sccm N_2**
2.3.	**Cleaning**	**Wet bench**	**Clean with air gun**
2.4a.	**Metallization (Pt)**	**Denton Desk 3**	**200 nm, without Cr adhesion layer**

2.4b.	Metallization (Pt)	ANS	200 nm, without Ti adhesion layer
2.5.	Metal lift-off	Wet bench	1165, 15 mins, 50 °C in ultrasonic bath
2.6.	IPA rinse	Wet bench	IPA in ultrasonic bath, 1 min
2.7.	Inspect	Microscope	Inspect wafer and repeat 2.5/2.6 if necessary
2.8.	DI rinse	Wet bench	Rinse with DI water and dry
2.9.	Inspect	Microscope	Inspect produced features and take pictures

Runsheet A.5 *Runsheet for test structures that enabled comparison between evaporated Pt and sputtered TaN used in direct contact with TaN features.*

Step	*Description*	Equipment	Parameters
0	*Processing starts with cleaned 3" wafers covered by thermal SiO_2*		
1.1. – 1.6.	*Same as in Runsheet A.2: 1.1. – 1.6.*		
1.7.	**Metal etch**	**JLS RIE80**	**2×10 min, 150 mTorr, 50 W, 60 sccm CF_4, 3 sccm O_2**
1.8. – 2.3.	*Same as in Runsheet A.2: 1.8. – 2.3.*		
2.4.	**Oxide etch**	**JLS RIE80**	**20+15 min, 30 mTorr, 100 W, 17.7 sccm CHF_3, 20.1 sccm Ar**
2.5. – 2.7.	*Same as in Runsheet A.2: 2.5. – 2.7.*		
3.1b.	*Same as in Runsheet A.4: 2.1.1. – 2.1.8.*		
3.2a.	**Metallization (TaN)**	**OPT Plasmalab**	**3×30 min, 3 mTorr, 500 W, 44 sccm Ar, 6 sccm N_2**
3.3a. – 3.5a.	*Same as in 1.4. – 1.6.*		
3.6a.	**Metal etch**	**JLS RIE80**	**10+15 min, 150 mTorr, 50 W, 60 sccm CF_4, 3 sccm O_2**
3.7a.	*Same as in 1.8. – 1.10.*		
3.2b.	**Metallization (TaN)**	**OPT Plasmalab**	**5 min, 3 mTorr, 500 W, 44 sccm Ar, 6 sccm N_2**
3.3b.	**Cleaning**	**Wet bench**	**Clean with air gun**
3.4b.	**Metallization (Pt)**	**ANS**	**200 nm, without Ti adhesion layer**
3.5b.	**Cleaning**	**Wet bench**	**Clean with air gun**
3.6b.	**Metal lift-off**	**Wet bench**	**1165, 15 mins, 50 °C in ultrasonic bath**
3.7b.	**IPA rinse**	**Wet bench**	**IPA in ultrasonic bath, 1 min**
3.8b.	**Inspect**	**Microscope**	**Inspect wafer and repeat 2.5/2.6 if necessary**
3.9b.	**DI rinse**	**Wet bench**	**Rinse with DI water and dry**
3.8a/3.10b.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**

Appendix B Runsheets and measurement results of devices produced by improved microfabrication process

B.1 Runsheets

Runsheet B.1.1 *'Process 1'. Runsheet of fabrication runs for sensor devices produced by improved layout design and microfabrication process.*

Step	*Description*	Equipment	Parameters
0	*Processing starts with cleaned 3" wafers covered by thermal SiO_2*		
1.1.	**Metallization (TaN)**	**OPT Plasmalab**	**3×30 min, 3 mTorr, 500 W, 44 sccm Ar, 6 sccm N_2**
1.2.	**Cleaning**	**Wet bench**	**Clean with air gun**
1.3.	**Photolithography: Metal dry etch**	**Mask 1 – L0 rev2**	
1.3.1.	Resist coat	SVG Track 1	Prime, spin-coat 1.5 μm SPR350, soft bake
1.3.2.	Resist expose	KS MA 8	Hard contact, 7.5 seconds exposure
1.3.3.	Resist develop	SVG Track 2	Develop resist and hard bake
1.4.	**Inspect**	**Microscope**	**Inspect developed features**
1.5.	**Metal etch**	**JLS RIE80**	**10+10 min, 150 mTorr, 50 W, 60 sccm CF_4, 3 sccm O_2**
1.6.	**Inspect**	**Microscope**	**Inspect resist condition**
1.7.	**Resist strip**	**Barrel Asher**	**Plasma etch for 60 minutes**
1.8.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**
2.1.	**Photolithography: Metal lift-off**	**Mask 2 – L1 rev2**	
2.1.1.	Prime	SVG Track 1	Or use HMDS box for 10 minutes
2.1.2.	Resist coat	POLOS 150	Spin-coat 1.5 μm AZ2070
2.1.3.	Soft bake	Hotplate	90 seconds, 100 °C
2.1.4.	Resist expose	KS MA 8	Hard contact, 20 seconds exposure
2.1.5.	Post-Exposure Bake	Hotplate	60 seconds, 115 °C
2.1.6.	Resist develop	Dish	AZ726MIF for 90 seconds
2.1.7.	Resist rinse	Wet bench	Rinse with DI water and dry
2.1.8.	Inspect	Microscope	Inspect resist features
2.2.	**Metallization (TaN)**	**OPT Plasmalab**	**5 min, 3 mTorr, 500 W, 44 sccm Ar, 6 sccm N_2**
2.3.	**Cleaning**	**Wet bench**	**Clean with air gun**
2.4.	**Metallization (Pt)**	**ANS**	**200 nm, without Ti adhesion layer**
2.5.	**Cleaning**	**Wet bench**	**Clean with air gun**
2.6.	**Metal lift-off**	**Wet bench**	**1165, 15 mins, 50 °C in ultrasonic bath**
2.7.	**IPA rinse**	**Wet bench**	**IPA in ultrasonic bath, 1 min**
2.8.	**Inspect**	**Microscope**	**Inspect wafer and repeat 2.6/2.7 if necessary**

2.9.	**DI rinse**	**Wet bench**	**Rinse with DI water and dry**
2.10.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**
2.11b.	**Annealing**	**Furnace 3**	**6 hours, 600 °C, vacuum – Load at 200 °C**
2.12b.	**Cleaning**	**Wet bench**	**Clean with air gun**
3.1.	**Passivation (SiO_2)**	**STS PECVD**	**8 min, 500 nm *LFSiO***
3.2.	**Photolithography: Oxide dry etch**	**Mask 3 – L2 rev1**	
3.2.1.	Resist coat	SVG Track 1	Prime, spin-coat 1.5 µm SPR350, soft bake
3.2.2.	Resist expose	KS MA 8	Hard contact, 9 seconds exposure
3.2.3.	Resist develop	SVG Track 2	Develop resist and hard bake
3.3.	**Inspect**	**Microscope**	**Inspect developed features**
3.4.	**Oxide etch**	**JLS RIE80**	**15+15 min, 30 mTorr, 100 W, 17.7 sccm CHF_3, 20.1 sccm Ar**
3.5.	**Inspect**	**Microscope**	**Inspect resist condition**
3.6.	**Resist strip**	**Barrel Asher**	**Plasma etch for 60 minutes**
3.7.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**
4.1.	**Metallization (Al)**	**OPT Plasmalab**	**2×45 min, 3 mTorr, 1000 W, 50 sccm Ar**
4.2.	**Cleaning**	**Wet bench**	**Clean with air gun**
4.3.	**Photolithography: Metal dry etch**	**Mask 4 – L3 rev2**	
4.3.1.	Resist coat	SVG Track 1	Prime, spin-coat 1.5 µm SPR350, soft bake
4.3.2.	Resist expose	KS MA 8	Hard contact, 5 seconds exposure
4.3.3.	Resist develop	SVG Track 2	Develop resist and hard bake
4.4.	**Inspect**	**Microscope**	**Inspect developed features**
4.5.	**Metal etch**	**STS Al etcher**	**15 min, 30 mTorr, 100 W, 17.7 sccm CHF_3, 15 sccm Ar**
4.6.	**Inspect**	**Microscope**	**Inspect resist condition**
4.7.	**Resist strip**	**Barrel Asher**	**Plasma etch for 60 minutes**
4.8.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**

Runsheet B.1.2 *'Process 2'. Runsheet for test structures used to produce TLM-type and other test structures.*

Step	*Description*	Equipment	Parameters
0	*Processing starts with cleaned 3" wafers covered by thermal SiO_2*		
1.1. – 2.9.	*Same as in Runsheet B.1.1: 1.1. – 2.9.*		
2.10.	**Inspect**	**Microscope**	**Inspect produced features**
2.11b.	**Annealing**	**Furnace 3**	**6 hours, 600 °C, vacuum – Load at 200 °C**
2.12b.	**Cleaning**	**Wet bench**	**Clean with air gun**
2.13.	**Inspect**	**Microscope**	**Take pictures**

Runsheet B.1.3 *'Process 3'. Runsheet used to produce step resistance test structures using LFSiO mesa layer.*

Step	*Description*	Equipment	Parameters
0	*Processing starts with cleaned 3" wafers covered by thermal SiO_2*		
1.1.	**Passivation (SiO_2)**	**STS PECVD**	**3.5 min, 200 nm LFSiO**
1.2.	**Photolithography: Oxide dry etch**	**Mask 1 – L0 rev2**	
1.2.1.	Resist coat	SVG Track 1	Prime, spin-coat 1.5 μm SPR350, soft bake
1.2.2.	Resist expose	KS MA 8	Hard contact, 5 seconds exposure
1.2.3.	Resist develop	SVG Track 2	Develop resist and hard bake
1.3.	**Inspect**	**Microscope**	**Inspect developed features**
1.4.	**Oxide etch**	**JLS RIE80**	**7.5+7.5 min, 30 mTorr, 100 W, 17.7 sccm CHF_3, 20.1 sccm Ar**
1.5.	**Inspect**	**Microscope**	**Inspect resist condition**
1.6.	**Resist strip**	**Barrel Asher**	**Plasma etch for 60 minutes**
1.7.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**
2.1. - 2.9.	*Same as in Runsheet B.1.2: 2.1. – 2.9.*		
2.10.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**

Runsheet B.1.4 *'Process 4'. Runsheet used to produce samples for second set of SEM measurements.*

Step	*Description*	Equipment	Parameters
0	*Processing starts with cleaned 3" wafers covered by thermal SiO_2*		
1.1a.	**Metallization (TaN)**	**OPT Plasmalab**	**3×30 min, 3 mTorr, 500 W, 44 sccm Ar, 6 sccm N_2**
1.1b.	**Passivation (SiO_2)**	**STS PECVD**	**3.5 min, 200 nm LFSiO**
1.2.	**Cleaning**	**Wet bench**	**Clean with air gun**
1.3.	**Photolithography: Metal dry etch**	**RW mask**	
1.3.1.	Resist coat	SVG Track 1	Prime, spin-coat 1.5 μm SPR350, soft bake
1.3.2a.	Resist expose	KS MA 8	Hard contact, 7.5 seconds exposure
1.3.2b.	Resist expose	KS MA 8	Hard contact, 5 seconds exposure
1.3.3.	Resist develop	SVG Track 2	Develop resist and hard bake
1.4.	**Inspect**	**Microscope**	**Inspect developed features**
1.5a.	**Metal etch**	**JLS RIE80**	**10+10 min, 150 mTorr, 50 W, 60 sccm CF_4, 3 sccm O_2**
1.5b.	**Oxide etch**	**JLS RIE80**	**7.5+7.5 min, 30 mTorr, 100 W, 17.7 sccm CHF_3, 20.1 sccm Ar**
1.6.	**Inspect**	**Microscope**	**Inspect resist condition**
1.7.	**Resist strip**	**Barrel Asher**	**Plasma etch for 60 minutes**
1.8.	**Inspect**	**Microscope**	**Inspect produced features and take pictures**
2.1.	**Metallization (TaN)**	**OPT Plasmalab**	**5 min, 3 mTorr, 500 W, 44 sccm Ar, 6 sccm N_2**
2.2.	**Cleaning**	**Wet bench**	**Clean with air gun**
2.3.	**Metallization (Pt)**	**ANS**	**200 nm, do not need Ti adhesion layer**
2.4.	**Inspect**	**Microscope**	**Inspect developed features and take pictures**

3.1.	**Cleaving**	**Scribe pen**	**Cleave along 1–1**
3.2.	**Cleaning**	**Wet bench**	**Clean with air gun**
3.3.	**Annealing**	**Furnace 3**	**6 hours, 600 °C, vacuum – Load at 200 °C**
3.4.	**Cleaning**	**Wet bench**	**Clean with air gun**
4.1.	**Cleaving**	**Scribe pen**	**Cleave along lines other than 1–1**
4.2.	*Cover cleaved samples with evaporated gold in Edwards E306A for 5 minutes*		
4.3.	**Sidewall inspection**	**Hitachi 4700 SEM**	**Take pictures of sidewall cross-section**

Runsheet B.1.5 *'Process 5'. Runsheet used to produce sets of sensor devices and test structures on different wafers – final run of improved microfabrication process.*

Step	*Description*	Equipment	Parameters
0	*Processing starts with cleaned 3" wafers covered by thermal SiO_2*		
1.1. – 1.6.	*Same as in Runsheet B.1.1: 1.1. – 1.6.*		
2.4.	**Metallization (Pt)**	**ANS**	**400 nm, do not need Ti adhesion layer**
2.5. – 2.10.	*Same as in Runsheet B.1.1: 2.5. – 2.10.*		
2.11b/c.	**Annealing**	**Furnace 3**	**6 hours, 600 °C, vacuum - Load at 200 °C**
2.12b/c.	**Cleaning**	**Wet bench**	**Clean with air gun**
3.1c. – 3.7c.	*Same as in Runsheet B.1.1: 3.1. – 3.7, but using L2 – rev2 mask*		
4.1c. – 4.8c.	*Same as in Runsheet B.1.1: 4.1. – 4.8.*		

B.2 Measurement results

Table B.2.1 *Measured transducer temperature response functions: wafer 3.*

Sample	*Element on wafer*	*Forward measurement*		*Reverse measurement*	
		Start of range, mV	*Sensitivity, $\mu V \cdot °C^{-1}$*	*Start of range, mV*	*Sensitivity, $\mu V \cdot °C^{-1}$*
3.0	*38*	285.51	66.13	285.51	65.51
	41	285.85	54.24	285.81	53.18
	47	306.17	29.69	306.17	29.47
	49	279.99	61.18	280.03	64.02
	56	309.97	25.78	309.97	25.66
	58	274.08	65.56	274.09	65.02
	63	310.12	29.66	310.13	29.20
	64	274.97	67.30	274.96	66.91
	69	303.91	30.73	303.92	30.38
	71	274.55	60.39	274.55	60.05
	78	307.10	27.11	307.10	26.84
	80	271.94	67.30	271.95	66.55
	83	266.17	56.42	266.18	56.07
	86	295.32	30.42	295.33	30.06
	89	297.71	31.94	297.69	32.40

3.5	*4*	349.09	58.72	349.11	58.03
	6	344.47	46.79	344.46	46.87
	9	375.53	29.35	375.52	29.59
	11	356.65	27.90	356.63	28.34
	28	341.47	69.79	341.47	69.49
	32	322.54	50.99	322.54	50.85
	33	372.43	28.71	372.45	28.39
	37	361.72	30.53	361.73	30.29
	90	325.26	76.58	325.26	76.05
	94	331.13	57.38	331.13	57.23
	95	343.65	38.38	343.65	38.01
	116	307.74	79.47	307.77	78.52
	118	325.79	63.49	325.81	62.78
	121	346.29	49.43	346.31	49.01
	123	349.03	49.03	349.05	48.41
4.0	*1*	421.59	49.71	421.61	49.17
	2	425.52	36.58	425.52	36.47
	30	418.49	68.76	418.50	68.35
	35	422.29	34.51	422.29	34.59
	42	387.18	56.66	387.16	56.92
	43	429.21	34.85	429.22	34.48
	51	370.21	67.65	370.21	67.47
	54	422.15	34.64	422.16	34.39
	73	381.42	66.73	381.43	66.43
	76	395.80	39.14	395.80	39.04
	84	378.48	64.11	378.48	63.84
	85	395.02	41.98	395.03	41.68
	92	359.50	78.89	359.50	78.47
	97	396.24	41.24	396.24	40.96
	125	379.83	81.40	379.84	81.09
	126	405.61	58.93	405.64	58.38
	1	421.59	49.71	421.61	49.17
4.5	*5*	459.72	61.59	459.74	61.13
	13	434.22	75.24	434.24	74.79
	18	475.86	38.45	475.86	38.59
	23	457.05	50.94	457.06	50.65
	24	475.16	45.17	475.14	45.57
	29	413.97	86.64	413.99	86.14
	36	473.30	37.28	473.31	37.02
	91	401.14	100.59	401.13	98.94
	98	451.25	43.26	451.26	42.91
	103	428.04	66.38	428.05	65.98
	104	439.11	56.39	439.14	55.75
	109	407.71	95.87	407.73	95.23
	114	447.19	53.79	447.21	53.39

	117	409.65	89.88	409.67	89.19
	122	443.87	63.36	443.89	62.87
	12	489.05	90.58	489.07	90.02
	19	531.27	40.26	531.27	40.33
	40	460.30	92.90	460.31	92.50
	45	525.92	44.37	525.93	43.98
	48	471.68	101.90	471.69	101.41
	52	488.45	71.96	488.46	71.67
	53	487.69	62.83	487.70	62.54
5.0	*57*	520.22	46.26	520.23	46.06
	70	461.53	106.26	461.53	105.81
	74	478.30	71.43	478.32	70.82
	75	189.82	218.78	189.82	218.44
	79	498.73	49.11	498.73	49.04
	82	456.24	105.72	456.25	105.34
	87	498.19	50.21	498.21	49.54
	108	440.54	119.53	440.55	118.86
	115	542.51	54.47	542.54	53.83
	3	588.16	47.98	588.16	48.21
	17	550.60	52.46	550.59	52.57
	21	543.13	86.57	543.16	85.88
	26	591.50	44.28	591.52	43.78
	60	540.39	75.05	540.40	74.71
	61	567.60	53.67	567.61	53.42
5.5	*66*	555.03	71.63	555.03	71.53
	67	546.28	58.50	546.31	57.67
	101	510.37	104.07	510.39	103.57
	106	511.75	68.29	511.76	68.14
	110	503.67	113.26	503.68	112.75
	113	552.88	66.21	552.90	65.60
	124	518.81	120.38	518.84	119.31
	16	641.65	52.47	641.67	52.14
	31	588.08	93.03	588.10	92.63
	34	640.54	53.50	640.52	54.12
	50	613.64	115.65	613.75	112.17
	55	632.73	51.37	632.75	50.88
	59	575.93	115.62	575.94	115.45
6.0	*16*	641.65	52.47	641.67	52.14
	65	507.17	136.18	507.20	135.51
	68	609.18	55.52	609.20	55.15
	72	550.22	115.28	550.24	114.73
	77	604.88	55.66	604.89	55.53
	93	536.04	108.56	536.05	108.28
	96	602.79	73.47	602.80	73.26
	111	565.78	100.28	565.79	100.11

6.5	8	696.76	58.27	696.79	57.94
	20	615.54	118.26	615.55	117.99
	22	656.38	83.32	656.41	82.57
	25	702.12	53.66	702.17	52.60
	27	482.43	55.21	482.49	53.83
	81	594.68	142.80	594.71	141.87
	88	648.84	67.46	648.87	66.45
	102	600.88	102.97	600.92	101.87
	105	650.69	70.04	650.70	69.90
	107	645.25	74.56	645.27	74.33
	119	620.92	108.08	620.94	107.55
	120	499.72	150.02	499.76	148.92

Table B.2.2 *Measured transducer temperature response functions: wafer 4.*

Sample	*Element on wafer*	*Forward measurement*		*Reverse measurement*	
		Start of range, mV	*Sensitivity, $\mu V \cdot °C^{-1}$*	*Start of range, mV*	*Sensitivity, $\mu V \cdot °C^{-1}$*
3.0	38	21.45	67.39	21.42	66.40
	41	154.08	35.09	153.99	36.06
	44	–19.92	86.54	–19.98	84.92
	47	–50.17	101.36	–50.23	99.79
	49	67.44	55.76	67.40	54.94
	56	155.75	11.50	155.66	11.66
	58	–9.91	84.90	–9.96	84.10
	63	40.69	48.12	40.59	48.60
	64	89.93	50.61	89.89	49.53
	69	–20.01	87.92	–20.05	86.72
	71	74.48	63.05	74.42	62.97
	78	85.22	52.51	85.13	53.27
	80	–94.17	169.89	–94.33	158.19
	83	–42.02	118.41	–41.98	115.10
	86	–22.72	88.89	–22.73	87.15
	89	–26.47	85.14	–26.51	83.96
3.5	4	87.06	42.47	86.97	42.38
	6	62.29	51.65	62.17	52.71
	9	–3.86	85.10	–3.93	84.12
	11	105.78	32.40	105.67	32.55
	28	69.20	75.04	69.14	74.29
	32	115.57	55.52	115.50	55.39
	33	–64.48	123.02	–64.47	121.52
	37	–139.4	175.20	–139.4	169.84
	90	98.96	75.10	98.90	75.30
	94	–30.48	126.33	–30.49	124.99
	95	–6.60	107.54	–6.67	107.46

	99	70.55	68.12	70.48	67.98
	116	104.68	93.62	104.64	93.29
	118	96.87	107.11	96.84	104.69
	121	45.03	92.90	45.02	91.30
4.0	*1*	–20.06	94.08	–20.14	91.97
	2	–12.80	87.81	–12.86	85.75
	30	132.87	61.77	132.81	61.63
	35	54.97	63.95	54.85	65.00
	42	–35.12	120.18	–35.18	119.70
	43	–33.12	152.26	–33.13	150.37
	51	–79.18	135.18	–79.22	133.00
	54	78.29	64.34	78.19	65.58
	73	28.26	102.59	28.20	103.22
	76	3.80	113.21	3.79	112.30
	84	119.42	82.59	119.36	82.60
	85	67.42	86.90	67.37	86.24
	92	6.78	126.74	6.76	126.05
	97	41.28	96.52	41.23	95.98
	125	105.00	135.25	104.97	134.62
	126	100.26	98.83	100.20	98.19
4.5	*5*	38.84	77.26	38.76	77.58
	10	80.52	15.91	79.09	14.83
	13	118.73	57.14	118.60	56.67
	18	29.74	85.72	29.64	85.74
	24	42.24	85.54	42.16	85.55
	29	204.80	139.68	204.74	139.46
	36	56.52	79.77	56.40	80.65
	91	68.31	116.30	68.28	115.28
	98	–3.68	119.61	–3.75	119.50
	104	126.74	103.85	126.69	103.69
	109	6.06	136.97	6.03	137.40
	114	49.06	104.58	48.99	105.35
	117	159.68	116.96	159.65	116.52
	122	–64.48	162.89	–64.49	161.85
5.0	*12*	1.83	115.76	1.77	114.77
	19	29.22	95.37	29.13	95.46
	40	16.24	135.10	16.17	135.24
	48	63.05	115.35	62.99	115.86
	52	–45.16	151.52	–45.19	149.99
	53	54.63	112.11	54.59	110.72
	57	–6.35	124.70	–6.42	123.84
	70	37.48	128.93	37.42	128.81
	74	113.87	128.39	113.82	128.12
	75	43.46	134.22	43.43	133.36
	79	49.80	104.14	49.77	102.19

	82	5.37	152.40	5.33	152.61
	87	18.86	120.41	18.77	121.19
	108	67.09	136.25	67.15	133.93
	115	71.29	107.81	71.16	111.63
5.5	*0*	75.05	68.89	74.92	69.53
	3	38.24	95.33	38.14	94.98
	14	41.34	113.88	41.23	114.34
	17	–54.52	159.37	–54.57	158.27
	26	–43.06	146.67	–43.12	144.90
	60	5.59	145.03	5.55	144.89
	61	55.43	113.54	55.37	112.42
	66	58.56	162.78	58.52	161.58
	67	62.20	113.40	62.14	113.36
	101	195.07	125.44	195.03	125.19
	106	84.25	127.29	84.10	131.88
	110	188.90	128.28	188.85	128.00
	113	30.37	147.60	30.31	149.31
	124	111.16	169.08	111.13	169.43
	127	–188.4	168.18	–188.6	173.53
6.0	*15*	72.25	105.49	72.10	107.75
	16	88.89	96.13	88.80	96.00
	31	46.48	132.27	46.41	132.12
	34	53.55	114.81	53.53	111.91
	50	58.24	127.88	58.17	128.37
	55	26.05	130.33	25.94	131.52
	59	30.50	139.24	30.48	137.60
	62	96.77	118.47	96.69	118.59
	65	72.78	129.14	72.60	133.24
	68	109.58	123.06	109.58	120.31
	72	45.39	154.07	45.20	159.17
	77	62.83	143.23	62.78	142.73
	93	61.86	166.36	61.70	171.06
	96	70.98	134.28	70.83	137.24
	111	153.83	166.41	153.78	166.35
	112	–33.54	201.10	–33.62	200.21
6.5	*7*	–2.80	151.57	–2.87	150.53
	8	50.02	118.20	49.87	119.89
	20	93.01	126.92	92.98	125.36
	25	–1.45	159.24	–1.54	159.39
	27	5.90	140.75	5.81	141.43
	39	223.88	114.59	223.81	114.53
	46	117.06	83.98	116.01	82.18
	81	149.61	160.04	149.56	159.59
	88	30.26	147.46	30.15	148.92
	100	151.52	148.94	151.47	148.93

	102	196.54	159.04	196.50	158.99
	105	35.20	188.05	35.15	188.28
	107	–16.56	188.93	–16.64	189.23
	119	160.60	195.85	160.57	195.37
	120	83.78	179.65	83.75	179.40

B.2.1 Resistive parameters of TaN thin films produced by 12% process

Summary of sheet resistance test structure measurement results related to 12% nitrogen flow ratio TaN deposition runs is shown in Table B.2.3. Deposition process run using the same recipe resulted in sheet resistance values from 13.3 to 14.0 Ω/□ when films were in as-deposited state mostly likely due to deviations in controlled nitrogen ratio and different deposition rates. Temperature coefficient of resistance values for mentioned film samples ranged from –175 to –150 ppm °C^{-1}.

Table B.2.3 *Comparison of different TaN sheet resistance and TCR values.*

Sample		*Film*	
Deposition run: process ID: wafer ID	*Film condition*	Sheet resistance value, Ω/□	TCR, ppm °C^{-1}
***1**:1:1*	*Non-annealed*	13.3	–150
***1**:2:1*	*Annealed (6 hrs)*	15.3	–160
***1**:3:1*	*Annealed (5 hrs)*	15.5	–150
***2**:1:1*	*Non-annealed*	13.45	–155
***2**:3:1*	*Annealed (5 hrs)*	13.85	–140
***3**:1:1*	*Non-annealed*	14.0	–175
***3**:2:1*	*Annealed (6 hrs)*	14.0	–190
***4**:1:1*	*Non-annealed*	13.05	–165
***4**:2:1*	*Annealed (6 hrs)*	20.65	350
***4**:2:2*	*Annealed (6 hrs)*	20.3	360
***5**:1:1 (ref. only)*	*Non-annealed*	12.95	–200

As evident from the table above, after annealing in vacuum at 600 °C for more than 5 hours sheet resistance of films was increasing to 13.85 – 15.5 Ω/□ and TCR of films was changing towards a range of –190 to –140 ppm °C^{-1}. As compared to as-deposited samples the change of sheet resistance was not higher than 16.5% for earlier process runs and the change of distribution of TCR values was within 8.5%.

The change following annealing process on samples produced by deposition run 4 was sheet resistance increase of 58% and highly positive TCR value of 350 to 360 ppm °C^{-1}. It can therefore be concluded that such a drastic change of characteristics was caused deviations in annealing process as compared to annealing steps that followed deposition runs 1 to 3.