

# High resolution electron beam lithography for exploratory silicon device fabrication

David William Travis



Thesis submitted for the degree of  
Doctor of Philosophy  
The University of Edinburgh  
July 1999



# **Abstract**

This thesis reports on a study into the fabrication of metal oxide silicon field effect transistors using electron beam lithography to pattern features with dimensions down to 100nm and below. The study is in an area of extensive research, with devices at these dimensions of interest for future generations of integrated circuit manufacture.

The design and construction of a high resolution electron beam system is reported. The system is based on a very high resolution scanning electron microscope equipped with a thermal field emission gun. Chemically amplified resist processes, for electron beam lithography, have been characterised for silicon device fabrication and sub 100nm patterns have been demonstrated.

The development of a fabrication process for silicon devices, with dimensions down to 100nm, is described. The process uses electron beam lithography for all levels of patterning and electrical measurements are reported for a range of the fabricated devices

Devices fabricated in this study are used to explore a novel width modification technique using focused ion beam milling to reduce the current drive of individual transistors. The transistors are characterised before and after modification and electrical measurements are presented which provide the basis for a new chip modification strategy.



## **Declaration**

I declare that this thesis has been completed by myself and that, except where indicated to the contrary, the research documented is entirely my own.

# Acknowledgements

I would like to thank everyone in the EMF who has helped to make this piece of work possible. Particularly my supervisor, Dr. Clive Reeves, for his excellent guidance and assistance, especially for finding time when there were more pressing matters to be dealt with. Thanks also to Alan Gundlach, Tom Stevenson and Alec Ruthven for maintaining the processing equipment and always helping with the constant requests for wafer processing.

Thanks to my parents for all the support and encouragement through the many years of education, none of my achievements would have been possible without it. Also, to my brother, whom I now expect to sit down and read this 'Ph-amphlet' from cover to cover.

To all the people down in the terrapin, past and present, I thank you for putting up with me and helping out with all the problems and questions. Thanks also to Dot for the cheerful and prompt stores service, nothing would have been built without it. I'm also grateful to everyone who has spent their time reading this thesis and providing valuable feedback, especially Professor Anthony Walton.

Finally, a special mention goes to all the members of Edinburgh University Boat Club, especially Wally, Olly, Miles and Alex, for many good times and the odd pint or two!

---

# Contents

---

GLOSSARY .....	v
LIST OF SYMBOLS .....	vii
LIST OF FIGURES .....	ix
LIST OF TABLES .....	xiii
<b>1. INTRODUCTION .....</b>	<b>1</b>
1.1 HIGH RESOLUTION LITHOGRAPHY .....	1
1.1.1 <i>Electron beam lithography</i> .....	2
1.2 MOSFET DEVICES .....	3
1.3 PROJECT AIMS .....	4
1.4 THESIS PLAN .....	5
<b>2. MOSFET DEVICE OPERATION .....</b>	<b>7</b>
2.1 THE LONG CHANNEL MOSFET .....	7
2.1.1 <i>Basic MOSFET operation</i> .....	8
2.1.2 <i>I-V characteristics of the MOSFET</i> .....	9
2.1.3 <i>Threshold Voltage</i> .....	16
2.2 THE SHORT CHANNEL MOSFET .....	17
2.2.1 <i>Short-channel device operation</i> .....	18
2.2.2 <i>Device Reliability</i> .....	25
2.3 MOSFET DEVICE SCALING .....	28
2.3.1 <i>Scaling strategies</i> .....	28
2.3.2 <i>High performance and low power scaling scenarios</i> .....	30
2.3.3 <i>Scaling projections</i> .....	31
2.4 PRESENT SILICON DEVICE RESEARCH .....	32
2.5 SUMMARY .....	33
<b>3. ELECTRON BEAM LITHOGRAPHY .....</b>	<b>34</b>
3.1 ELECTRON BEAM LITHOGRAPHY SYSTEMS .....	34
3.1.1 <i>A general system</i> .....	34



3.1.2 History of e-beam systems.....	35
3.1.3 Current e-beam technology.....	36
3.2 ALTERNATIVE EXPOSURE TECHNIQUES .....	38
3.2.1 Optical Lithography.....	38
3.2.2 X-ray lithography.....	39
3.3 E-BEAM EXPOSURE PRINCIPLES .....	42
3.3.1 Beam projection system.....	42
3.3.2 Resist technology.....	45
3.4 SUMMARY .....	48
<b>4. EDINBURGH ELECTRON BEAM LITHOGRAPHY SYSTEM .....</b>	<b>49</b>
4.1 GENERAL OPERATION.....	49
4.1.1 System Specification.....	52
4.2 PATTERN GENERATOR BOARD.....	52
4.3 CLOCK CIRCUITS .....	56
4.3.1 System Clock.....	56
4.3.2 Offset clock.....	58
4.3.3 Delay Clock.....	59
4.4 DIGITAL TO ANALOGUE CONVERTER BOARD.....	60
4.5 VIDEO BOARD.....	63
4.6 OUTPUT BOARD.....	64
4.6.1 Output Buffers .....	64
4.6.2 Beam Blanking circuit.....	65
4.6.3 Picoammeter Relay Control.....	66
4.7 SYSTEM LAYOUT .....	67
4.8 SUMMARY .....	69
<b>5. DEVICE FABRICATION LAYOUT.....</b>	<b>70</b>
5.1 DESIGN .....	70
5.2 PATTERN LAYOUT .....	71
5.2.1 Wafer layout.....	71
5.2.2 Chip Site Patterning.....	72
5.2.3 Inner e-beam area device layout.....	75
5.3 MOS DEVICE STRUCTURE.....	79
5.3.1 Transistor dimensions .....	79
5.3.2 Sidewall spacer .....	81
5.3.3 Isolation oxide.....	81
5.4 PROCESSING TECHNIQUES .....	82

<i>Contents</i>	iii
5.4.1 Layer growth/deposition .....	82
5.4.2 Dry Etching .....	85
5.4.3 End point detection .....	88
5.4.4 Ion implantation .....	89
5.5 SUMMARY .....	91
<b>6. FABRICATION PROCEDURE.....</b>	<b>92</b>
6.1 CHARACTERISATION .....	92
6.1.1 Negative photoresist.....	93
6.1.2 Positive Photoresist.....	102
6.1.3 Polysilicon processing .....	104
6.2 PROCESSING SEQUENCE .....	110
6.2.1 Active areas.....	111
6.2.2 Channel implant and gate oxide .....	111
6.2.3 Gate formation .....	112
6.2.4 Junction implants and sidewall spacer .....	112
6.2.5 Contact formation .....	113
6.2.6 Metalization .....	113
6.3 SUMMARY .....	114
<b>7. DEVICE RESULTS.....</b>	<b>115</b>
7.1 DEVICE STRUCTURE .....	115
7.2 ELECTRICAL CHARACTERISATION .....	116
7.2.1 I-V output curves.....	117
7.2.2 Subthreshold curves .....	119
7.2.3 Turn-on curves .....	121
7.2.4 Characterisation summary.....	123
7.3 FOCUSED ION BEAM WIDTH MODIFICATION OF TRANSISTORS .....	123
7.3.1 Transistor modification strategy .....	123
7.3.2 FIB removal of material (0.5 $\mu$ m devices).....	125
7.3.3 Electrical results (0.5 $\mu$ m devices).....	127
7.3.4 FIB removal of material (0.25 $\mu$ m device).....	130
7.3.5 Electrical results (0.25 $\mu$ m device).....	131
7.4 SUMMARY .....	133
<b>8. CONCLUSIONS .....</b>	<b>135</b>
8.1 NANOFABRICATION FACILITY .....	136
8.2 INTEGRATED MOS DEVICE EXPERIMENT .....	137



<i>Contents</i>	iv
8.3 FOCUSED ION BEAM MODIFICATION OF MOS DEVICES .....	138
8.4 FUTURE WORK .....	139
8.5 CONCLUSIONS .....	140
<b>A. DEVICE FABRICATION RUN SHEET .....</b>	<b>142</b>
<b>B. PUBLICATIONS .....</b>	<b>145</b>
<b>REFERENCES.....</b>	<b>150</b>



---

# Glossary

---

A/D	Analogue to Digital
CAR	Chemically Amplified Resist
CE	Constant Electric field
CVD	Chemical Vapour Deposition
CMOS	Complementary Metal Oxide Silicon
DAC	Digital to Analogue Conversion
DIBL	Drain Induced Barrier Lowering
DRAM	Dynamic Random Access Memory
E-beam	Electron beam
EBES	Electron Beam Exposure System
ECR	Electron-Cyclotron Resonance
EEBLS	Edinburgh Electron Beam Exposure System
EMF	Edinburgh Microfabrication Facility
FIB	Focused Ion Beam
GIDL	Gate Induced Drain Leakage
HMDS	Hexamethyldisilazane
I/O	Input to Output
LDD	Lightly Doped Drain
LOCOS	Local Oxidation of Silicon
LPCVD	Low Pressure Chemical Vapour Deposition
LSI	Large Scale Integration
MOS	Metal Oxide Silicon
MOSFET	Metal Oxide Silicon Field Effect Transistor
nMOSFET	n-channel Metal Oxide Silicon Field Effect Transistor
PECVD	Plasma Enhanced Chemical Vapour Deposition
PMMA	Poly Methyl Methacrylate

Resist	Photoresist
RIE	Reactive Ion Etching
SCALPEL	SCattering with Angular Limitation in Projection Electron-beam Lithography
SEM	Scanning Electron Microscope
SIA	Semiconductor Industry Association
UV	Ultraviolet
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration

---

# List Of Symbols

---

$C_{ox}$	Gate oxide capacitance
$D_n$	Electron diffusion constant
$D_I$	Dose of implanted ions
$\epsilon_0$	Permittivity in vacuum
$\epsilon_{Si}$	Semiconductor permittivity
$\epsilon_{ox}$	Oxide permittivity
$f$	frequency
$g_m$	Transconductance
$g_d$	Drain conductance
$\gamma_n$	Contrast of negative resist
$\gamma_p$	Contrast of positive resist
$I_D$	Drain current
$I_{PT}$	Punchthrough current
$k$	Boltzmann constant
$l$	Characteristic length of the channel
$L$	Channel length
$\Delta L$	Pinch off region length
$\mu_n$	Carrier velocity
$n_i$	intrinsic carrier concentration
$N_A$	Number of acceptor atoms
$N_{sub}$	Substrate doping concentration
$q$	electron charge
$Q_{tot}$	Total electronic charge
$\phi_b$	Energy required for electrons to surmount the Si/SiO <sub>2</sub> barrier
$\phi_B$	Semiconductor doping parameter



$\varphi_{\text{ms}}$	Metal-semiconductor workfunction difference
$\varphi_{\text{surf}}$	Surface potential
$\kappa_{\text{si}}$	Semiconductor interface constant
$S_t$	Subthreshold slope
$t_{\text{ox}}$	Gate oxide thickness
$T$	Temperature
$V_{\text{bi}}$	Built in potential between source-substrate and drain-substrate junctions
$V_{\text{D}}$	Drain voltage
$V_{\text{Dsat}}$	Drain voltage in saturation
$V_{\text{G}}$	Gate voltage
$V_{\text{PT}}$	Punchthrough voltage
$V_{\text{S}}$	Source voltage
$V_{\text{T}}$	Threshold voltage
$\Delta V_{\text{T}}$	Threshold voltage shift
$W$	Active area width
$x_{\text{i}}$	Implantation depth of impurities

# List of Figures

FIGURE 1.1 GRAPH SHOWING THE PERFORMANCE INCREASE, AS A FUNCTION OF TIME DELAY, IN A CMOS CIRCUIT WITH A REDUCTION IN THE MINIMUM FEATURE SIZE[TAUR 1997] .....	4
FIGURE 2.1 LAYOUT OF A LONG CHANNEL MOSFET A) CROSS SECTIONAL VIEW B) GENERAL STRUCTURE C) SCHEMATIC DIAGRAM[HODGES 1983] .....	8
FIGURE 2.2 TURN ON CHARACTERISTICS OF A N-MOSFET.....	9
FIGURE 2.3 THE VARIATION OF $I_D$ WITH INCREASING $V_D$ FOR A FIXED $V_G > V_T$ .....	10
FIGURE 2.4 VISUALISATION OF THE REGIONS OF OPERATION FOR THE MOSFET: A) $V_D \approx 0V$ , B) INVERSION LAYER NARROWING UNDER MODERATE $V_D$ BIASING, C) PINCH-OFF AND D) POST PINCH-OFF, $V_D > V_{DSAT}$ .....	11
FIGURE 2.5 SUBTHRESHOLD CHARACTERISTICS FOR A LONG CHANNEL DEVICE [TROUTMAN 1974] .....	14
FIGURE 2.6 GATE INDUCED DRAIN LEAKAGE CURRENT IN A MOSFET .....	15
FIGURE 2.7 CALCULATED THRESHOLD VOLTAGES OF A NMOSFET AS A FUNCTION $N_{SUB}$ AND $T_{OX}$ [SZE M, 1988] .....	16
FIGURE 2.8 DIAGRAMS OF INCREASING SHORT CHANNEL BEHAVIOUR IN MOSFETS. A) LONG CHANNEL BEHAVIOUR, B) WITH CHANNEL MODULATION, AND C) WITH VELOCITY SATURATION[DUVVURY 1986] .....	18
FIGURE 2.9 DIAGRAM SHOWING THE PINCHED-OFF REGION, $\Delta L$ , IN THE CHANNEL OF A SHORT CHANNEL LENGTH MOS TRANSISTOR OPERATING IN SATURATION.....	19
FIGURE 2.10 PUNCHTHROUGH CURRENT PATHS (DOTTED) IN A SURFACE-CHANNEL NMOSFET WITH $V_D=0.5$ AND $3.5V$ . SOLID LINE SHOWS THE DEPLETION REGION EDGE[ZHU 1988]. .....	21
FIGURE 2.11 SUBTHRESHOLD CURVES FOR, $\log I_D$ VERSUS $V_G$ , FOR A) LONG CHANNEL NMOSFET AND B) SHORT CHANNEL NMOSFET[WOLF 1995].....	22
FIGURE 2.12 HALO $P^+$ IMPLANTS AROUND THE JUNCTIONS OF A NMOSFET[CODELLA 1985] .....	23
FIGURE 2.13 THRESHOLD VOLTAGE AS A FUNCTION OF EFFECTIVE CHANNEL LENGTH[LIU 1993].....	24
FIGURE 2.14 REVERSE SHORT CHANNEL EFFECT ON THRESHOLD VOLTAGE[ORLOWSKI 1987].....	25
FIGURE 2.15 ILLUSTRATION OF HOT-CARRIER EFFECTS INCLUDING HOT-CARRIER GENERATION, INJECTION AND TRAPPING[CHEN 1988]. .....	26
FIGURE 2.16 A MEASURE OF THE ELECTRIC FIELD, $V_{DD}/L$ , AS A FUNCTION OF CHANNEL LENGTH FOR VARIOUS SCALING SCENARIOS[DAVARI 1995].....	31
FIGURE 3.1 SCHEMATIC DIAGRAM OF THE SCALPEL IMAGING STRATEGY[HARRIOTT 1997].....	37
FIGURE 3.2 X-RAY PROXIMITY PRINTING[LEPSELTHER 1983] .....	41



FIGURE 3.3 PROJECTION OPTICS OF AN ELECTRON COLUMN .....	43
FIGURE 3.4 RESPONSE CURVES FOR A) POSITIVE RESIST AND B) NEGATIVE RESIST IN TERMS OF THE DEVELOPED THICKNESS NORMALISED TO THE INITIAL RESIST THICKNESS AS A FUNCTION OF LOG (DOSE) [MOSS 1987].....	47
FIGURE 4.1 GENERAL LAYOUT OF THE EEBLS .....	50
FIGURE 4.2 VECTOR SCANNING OF A 5X5 PATTERN .....	53
FIGURE 4.3 SCHEMATIC DIAGRAM OF THE PATTERN GENERATOR CIRCUITRY .....	54
FIGURE 4.4 TIMING DIAGRAM FOR A 5X3 (X×Y) PATTERN FROM THE PATTERN GENERATOR CIRCUIT...	55
FIGURE 4.5 SCHEMATIC DIAGRAM OF THE SYSTEM CLOCK .....	57
FIGURE 4.6 TIMING DIAGRAM FOR 1MHZ OPERATION OF THE SYSTEM CLOCK.....	57
FIGURE 4.7 SCHEMATIC DIAGRAM OF THE OFFSET CLOCK.....	58
FIGURE 4.8 TIMING DIAGRAM OF THE OFFSET CLOCK WITH A 1MHZ SYSTEM CLOCK FREQUENCY .....	59
FIGURE 4.9 BLOCK DIAGRAM OF THE DELAY CLOCK CIRCUITRY .....	59
FIGURE 4.10 TIMING DIAGRAM OF THE DELAY CLOCK .....	60
FIGURE 4.11 LAYOUT OF THE DAC BOARD CIRCUITRY .....	62
FIGURE 4.12 VIDEO BOARD SCHEMATIC DIAGRAM.....	63
FIGURE 4.13 OUTPUT BUFFER CIRCUIT .....	64
FIGURE 4.14 SCHEMATIC DIAGRAM OF THE BEAM BLANKER CIRCUITRY .....	65
FIGURE 4.15 PICOAMMETER RELAY CONTROL CIRCUIT.....	66
FIGURE 4.16 ELECTRON BEAM LITHOGRAPHY SYSTEM LAYOUT, (A) BOARD LAYOUT VIEWED FROM THE FRONT OF THE SYSTEM AND (B) INPUT/OUTPUT CONNECTIONS VIEWED FROM THE BACK OF THE SYSTEM. ....	67
FIGURE 4.17 LAYOUT OF THE CONNECTIONS TO THE UPPER AND LOWER DATA BUSES.....	68
FIGURE 5.1 LEVELS OF LITHOGRAPHY PATTERNING FOR THE DEVICE EXPERIMENT .....	71
FIGURE 5.2 PATTERN LAYOUT ON THE 3" WAFER .....	72
FIGURE 5.3 OPTICAL MASK FOR THE FRAME LEVEL OF LITHOGRAPHY .....	73
FIGURE 5.4 OPTICAL MASK FOR THE METAL LEVEL OF LITHOGRAPHY .....	74
FIGURE 5.5 ELECTRON BEAM LITHOGRAPHY PATTERNS FOR THE INNER E-BEAM AREA.....	76
FIGURE 5.6 LAYOUT OF THE TRANSISTORS IN THE PATTERN <i>DESIGN0</i> .....	77
FIGURE 5.7 LAYOUT OF THE TRANSISTORS IN THE PATTERN <i>DESIGN1</i> .....	78
FIGURE 5.8 MOS DEVICE STRUCTURE .....	80
FIGURE 5.9 DIAGRAM OF THE SIDEWALL SPACER PROFILE AND ISOLATION OXIDE.....	81
FIGURE 5.10 DIAGRAM SHOWING THE FEATURES PRODUCED WITH A ISOTROPIC WET ETCH AND ANISOTROPIC DRY ETCH .....	86
FIGURE 5.11 REPRESENTATION OF THE PARAMETER PROBLEM IN PLASMA ETCHING SYSTEMS ( $N_e$ IS THE ELECTRON DENSITY, $f(E)$ IS THE ELECTRON ENERGY DISTRIBUTION FUNCTION, $N$ IS THE GAS DENSITY AND $\tau$ IS THE RESIDENCE TIME[WOLF 1986].....	87



FIGURE 5.12 SCHEMATIC DIAGRAM OF A LASER INTERFEROMETRY/REFLECTANCE END POINT DETECTOR	89
FIGURE 5.13 SCHEMATIC OF AN ION IMPLANTATION SYSTEM[BRODIE 1982] .....	90
FIGURE 6.1 SENSITIVITY CURVE FOR AZ PN 114 EXPOSED BY E-BEAM LITHOGRAPHY AND DEVELOPED IN SHIPLEY MF 319.....	94
FIGURE 6.2 4x6 $\mu$ m ACTIVE AREA PATTERN A) BEFORE RESIDUE REMOVAL. B) POST O <sub>2</sub> PLASMA ASH...	95
FIGURE 6.3 COLLAPSED 100NM LINE PATTERNED IN 1 $\mu$ m THICK PHOTORESIST .....	96
FIGURE 6.4 PHOTORESIST LINE PATTERNED IN RESIST DILUTED IN THE RATIO 1:5 (RESIST:THINNER) .....	97
FIGURE 6.5 TEST PATTERN OF LINES WITH INCREASING WIDTH EXPOSED WITH INCREASING DOSE BETWEEN 5 AND 50 $\mu$ C/CM-2.....	98
FIGURE 6.6 A) TEST PATTERN 'AZRESA' B)TEST PATTERN 'GATE230' .....	99
FIGURE 6.7 CROSS-SECTION OF A NEGATIVE PHOTORESIST LINE OF 1 PIXEL DEFINED WIDTH. ....	101
FIGURE 6.8 TEST PATTERN CONTACTB, USED FOR THE CALIBRATION OF THE POSITIVE RESIST AZ PF 514	103
FIGURE 6.9 IMAGE OF A 2 PIXEL WIDE TRENCH, EXPOSED IN POSITIVE AZ PF 514 PHOTORESIST. ....	104
FIGURE 6.10 PATTERNED POLYSILICON LINE AFTER STEP2 ETCH PROCESS USING AZ PN 114 RESIST AS A MASK .....	106
FIGURE 6.11 PATTERNED POLYSILICON LINE AFTER STEP2 FOLLOWED BY STEP3 ETCH PROCESS .....	107
FIGURE 6.12 IMAGE OF A SINGLE PIXEL LINE A) PRE-OXIDE ETCH AND B) POST-OXIDE ETCH.....	108
FIGURE 6.13 IMAGE OF AN OXIDE LINE AFTER A PATTERN TRANSFER STEP FROM THE RESIST AND A 2 MINUTE O <sub>2</sub> PLASMA ASH.....	109
FIGURE 6.14 CROSS-SECTION OF A POLYSILICON LINE AFTER PATTERN TRANSFER ETCH WITH AN OXIDE MASK .....	110
FIGURE 7.1 SEM IMAGE OF A FABRICATED N-MOSFET .....	115
FIGURE 7.2 FIB CROSS-SECTIONS OF A NMOSFET DEVICE: A) OVERVIEW OF DEVICE, B) MAGNIFIED VIEW .....	116
FIGURE 7.3 I-V CURVES FOR DEVICES WITH GATE LENGTHS: A) 1 $\mu$ m, B) 0.5 $\mu$ m, C) 0.25 $\mu$ m, D) 0.1 $\mu$ m	119
FIGURE 7.4 SUBTHRESHOLD CURVES FOR DEVICES WITH GATE LENGTHS: A) 1 $\mu$ m, B) 0.5 $\mu$ m, C) 0.25 $\mu$ m, D) 0.1 $\mu$ m.....	121
FIGURE 7.5 TURN ON CURVES FOR DEVICES WITH GATE LENGTHS: A) 1 $\mu$ m, B) 0.5 $\mu$ m, C) 0.25 $\mu$ m, D) 0.1 $\mu$ m .....	122
FIGURE 7.6 MODIFICATION STRATEGY OF TRANSISTORS, A) LENGTHWAYS CUT ACROSS THE GATE, B) VERTICAL CUTS UP THE WIDTH OF THE DEVICE. ....	124
FIGURE 7.7 LATERAL FIB CUTS ACROSS TRANSISTORS: A) T1 B)T2. ....	125
FIGURE 7.8 ORTHOGONAL FIB CUT IN TRANSISTOR T3 .....	126
FIGURE 7.9 SUBTHRESHOLD CURVES FOR: A) T1 B) T2.....	127
FIGURE 7.10 CURRENT-VOLTAGE CHARACTERISTICS FOR: A) T1 B) T2.....	128
FIGURE 7.11 SUBTHRESHOLD CHARACTERISTICS FOR DEVICE T3: A) FORWARD CONNECTION, B) REVERSE CONNECTION .....	129

FIGURE 7.12 CURRENT-VOLTAGE CHARACTERISTICS FOR DEVICE T3: A) FORWARD CONNECTION, B)  
REVERSE CONNECTION ..... 130

FIGURE 7.13 LATERAL FIB CUT ACROSS TRANSISTOR T4..... 131

FIGURE 7.14 SUBTHRESHOLD CURVES FOR TRANSISTOR T4 ..... 132

FIGURE 7.15 CURRENT-VOLTAGE CHARACTERISTICS FOR TRANSISTOR T4..... 133



---

# List of Tables

---

TABLE 2.1 RELATIONSHIPS BETWEEN CONSTANT-ELECTRIC FIELD AND GENERALISED SCALING[DAVARI 1995] .....	29
TABLE 2.2 MOSFET TECHNOLOGY PROJECTIONS[SIA, 1997].....	32
TABLE 4.1 EDINBURGH ELECTRON BEAM LITHOGRAPHY SYSTEM SPECIFICATION .....	52
TABLE 5-1 KEY OF TRANSISTOR GATE AND CONTACT DIMENSIONS FOR PATTERN <i>DESIGN0</i> .....	77
TABLE 5-2 KEY OF TRANSISTOR GATE AND CONTACT DIMENSIONS FOR PATTERN <i>DESIGN1</i> .....	78
TABLE 6.1 EXPOSURE CONDITIONS FOR AZ PN 114.....	101
TABLE 6.2 EXPOSURE CONDITIONS FOR AZ PF 514 .....	103
TABLE 6.3 PROCESS CONDITIONS FOR THE POLYSILICON ETCH PROCESS .....	105
TABLE 6.4 ETCH RATES OF THE POLYSILICON ETCH PROCESS .....	105
TABLE 7.1 DIMENSIONS OF THE CHARACTERISED NMOS TRANSISTORS.....	117
TABLE 7.2 DIMENSIONS OF TRANSISTORS MODIFIED USING FIB SYSTEM .....	125



# **Introduction**

---

The continued expansion of the microelectronics industry, with widespread use of semiconductor technology, has led to the demand for increased performance of silicon devices. Historically metal oxide silicon field effect transistor (MOSFET) device performance has been improved by reducing the device's physical dimensions, which increases the operating speed and packing density[Wong 1999]. This thesis demonstrates the challenges involved in the fabrication of high performance MOSFETs and reducing the dimensions of the devices.

## **1.1 High Resolution Lithography**

Lithography is an important stage in the fabrication of MOSFET devices. It involves defining patterns in a photoresist material, which is used to reproduce structures in material layers after development of the resist. Improvements in the resolution of the lithographic process have been the driving force behind performance increases in metal oxide silicon (MOS) devices, as reducing the device feature sizes increases device performance. High resolution lithography is a label given to the lithography of advanced features, beyond those achievable with current manufacturing lithography systems. Due to this definition, high resolution lithography is an imprecise term that changes as technology improvements enhance the resolution of lithography systems. Other terms that are used to describe the resolution of lithography processes are:

- Sub-micron            - lithography below  $1\mu\text{m}$
- Deep sub-micron   - lithography below  $0.35\mu\text{m}$
- nano-lithography   - lithography below  $0.1\mu\text{m}$

High resolution lithography is presently best defined by nano-lithography.



There are various forms of exposure techniques available for the lithography of MOS devices. The three most widely used methods of exposure are:

- Optical
- X-ray
- Electron beam

Optical lithography uses ultra-violet radiation as the exposing medium and is currently used in the high volume production of integrated circuits. The technology, however, is being pushed to its limits to expose features in the deep sub-micron region of pattern definition. X-ray lithography uses a smaller wavelength of exposure radiation and can hence define features of reduced dimensions from optical lithography. The use of x-rays has inherent problems, described in section 3.2.2, and because of these is not currently favoured for the production of integrated circuits. Electron beam lithography, as described in this work, is primarily used as a high resolution research tool for the lithography of advance devices.

### **1.1.1 Electron beam lithography**

For research applications, electron beam lithography is an important tool for the fabrication of advanced semiconductor devices. High resolution electron beams have enabled patterns to be produced with dimensions smaller than those achieved with the available optical lithography procedures. This is an established trend which continues to the present generation of MOSFET devices. The trend is well demonstrated by the fact that present industrial optical lithography steppers are used to manufacture devices with 0.18 $\mu\text{m}$  dimensions yet, electron lithography is used in the research environment at sub-0.1 $\mu\text{m}$  [Ochiai 1996, Kawaura 1998]

Electron beam lithography has many advantages as a patterning technique in a research environment. The systems are of relatively low cost, starting at around \$1-5M for a unit, compared to \$5-10M for an optical stepper system. The operating costs are also low with the patterns defined sequentially, in a vector scan system, by a series of co-ordinates, instead of a physical masking method as used with optical and

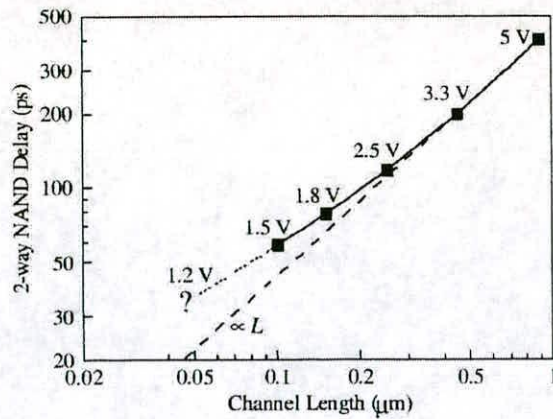
x-ray techniques. This method of pattern definition also allows for multiple sets of patterns to be defined over the area of the silicon wafer, which is also useful in a research environment as many test structures can be utilised on a single processing wafer, which reduces fabrication costs. As the patterns are defined with an electron beam, the maximum area that can be patterned without moving the stage is smaller than exposed with optical techniques, this can cause complications when imaging larger patterns. Stitching techniques with careful stage positioning can overcome these problems, but can lead to a low throughput of wafers. It is this low throughput of wafers that inhibits electron beam lithography for use in the manufacturing environment.

## 1.2 MOSFET devices

The MOS transistor is the predominant silicon device currently in use by the microelectronics industry. Since the MOSFET's first reported use in 1960 by D. Kahng and M. M. Atalla [Kahng 1976], the basic structure of the device has remained relatively unchanged. The present generation of devices still use a gate electrode that is situated between two junctions, where a voltage is applied to the gate to produce an inversion layer in the channel below that enables a flow of electrons between the junctions.

Although the MOSFET has retained its basic structure, the devices size has reduced considerably, with minimum feature sizes, in state of the art production devices down to  $0.18\mu\text{m}$ . The performance of the devices has also significantly increased with reduction in feature size, this is shown in the graph of figure 1.1 which highlights the performance increase in a CMOS circuit as the feature size of the device is reduced.





**Figure 1.1** Graph showing the performance increase, as a function of time delay, in a CMOS circuit with a reduction in the minimum feature size[Taur 1997]

### 1.3 Project aims

The motivation behind the work described in this thesis was to address the challenges of developing advanced silicon devices. As described in the previous sections, the challenges in this field are wide ranging with many different techniques available for the fabrication of silicon devices. For this reason the field of study has to be reduced to specific areas. The aims of the study can be stated as:

- Investigate high resolution electron beam lithography for application to the fabrication of silicon MOSFET devices
- Fabrication of advanced MOSFET devices using electron beam lithography
- Analysis of the operating characteristics of deep sub-micron MOSFETs

To realise these project aims it was necessary to develop the following systems and techniques.

- The design and construction of a high resolution electron beam lithography system based around a thermal field emission scanning electron microscope.

- Characterisation of this system for high resolution lithography with chemically amplified photoresists.
- The development of techniques to enable the fabrication of MOS transistors at deep submicron and nanoscale dimensions.

The development of these systems enabled the project to focus on the stated aims and investigate the challenges of advanced silicon device fabrication.

## **1.4 Thesis plan**

The operation of MOS transistors is discussed in chapter 2. Initially the characteristics of a long channel device are described and used in later sections of the discussion for more advanced short channel devices. The challenges of fabricating short channel MOSFETs are also described in this section.

Chapter 3 introduces the area of electron beam lithography. The chapter discusses the technology used with this lithography technique and includes the past and present status of electron beam systems within microelectronic processing. Alternative lithography techniques are also discussed to provide a comparison of lithographic fabrication procedures. The electron beam lithography system that was designed and constructed as part of this project is discussed in detail in chapter 4. This section provides an in depth study of the operating systems within the e-beam system and is intended to provide both an insight into such systems and provide a reference manual for any future analysis of the system.

The design and layout of the experiment to fabricate MOS transistors is described in chapter 5. The patterns that were designed for lithographic patterning with the e-beam system are discussed and the dimensions of the designed transistors are displayed. Discussion of processing techniques that were used in the fabrication procedure are included, providing reference for the later discussion on process characterisation.



The characterisation of fabrication techniques are discussed in chapter 6, including characterisation of negative and positive photoresists and polysilicon processing. The fabrication procedure of the MOSFET devices is also described.

Chapter 7 discusses the analysis of the fabricated transistors with advanced focused ion beam techniques. The electrical characteristics of the devices are described and the effect of focused ion beam sectioning of the devices is discussed. Finally, the thesis is concluded in chapter 8.



---

## MOSFET Device Operation

---

The basic operation of the MOS transistor is discussed in this chapter. The information presented provides an overview of MOSFET operation and relates to the devices that are demonstrated in subsequent chapters of this thesis. The long channel characteristics of device operation are initially presented, highlighting the parameters that affect the output characteristics of the transistors. Short channel devices are then discussed, highlighting the variations in device performance as the channel length of the MOSFET is reduced. The analysis of short channel devices is important as current and future trends of MOS device fabrication involve the reduction of geometries to increase chip packing density and performance. Finally, a discussion on the scaling strategies of MOS transistors is included, with a discussion of the current trends in MOS device research.

### 2.1 The Long Channel MOSFET

The basic layout of a long channel n-MOSFET is shown in fig 2.1. The substrate is lightly doped, p-type silicon.. The device is controlled by four terminal connections, the gate, drain, source and body. The active region of the device contains the gate, source and drain. The gate is a conducting electrode, usually polysilicon, that is insulated from the channel region of the device by a thin oxide. Either side of the gate lie the source and drain regions, these are n-type impurities implanted into the substrate. The field region bounds the active area with a field oxide and a reasonably heavily doped p-type implant, that is used to isolate the device. The basic structure of a p-MOS transistor is the same as that described for the n-MOS device, except the substrate is n-type with p-type impurities implanted in the source and drain regions. Electrons are the carriers in the n-MOSFET and the device is biased with positive

voltages. A p-MOS device has holes as the carriers and the transistor is biased with negative voltages. The analysis of the MOSFET from herein after will describe the n-MOSFET.

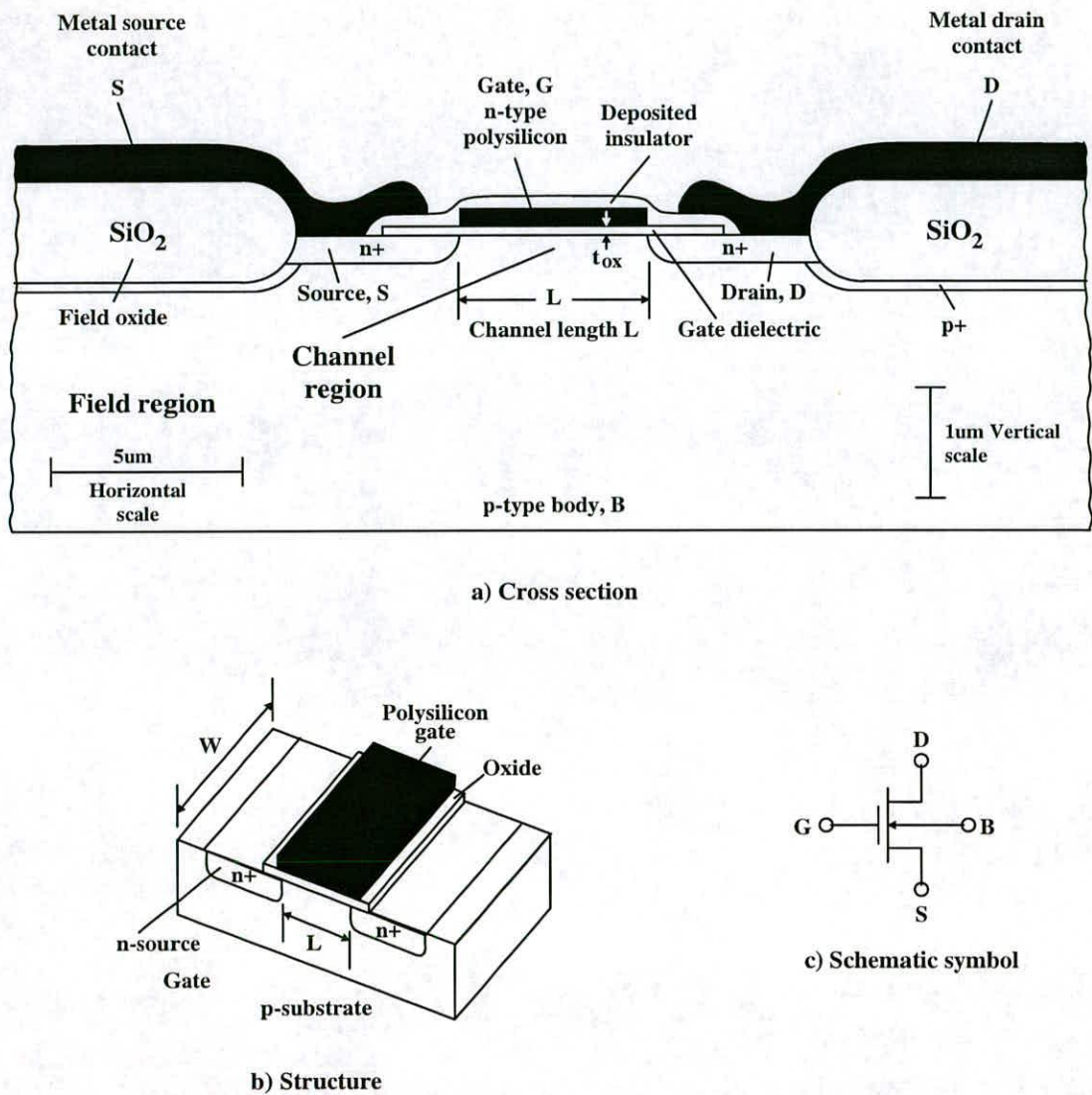


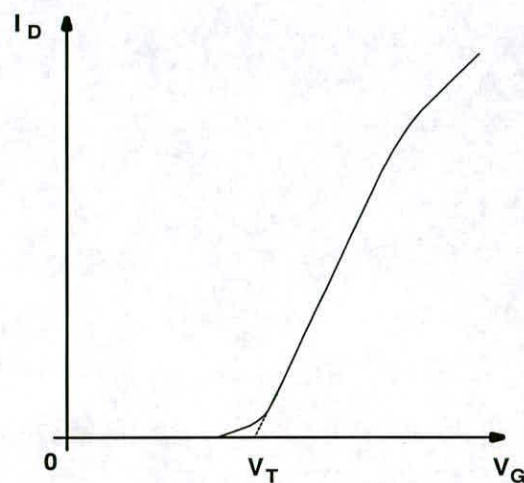
Figure 2.1 Layout of a long channel MOSFET a) Cross sectional view b) General structure c) Schematic diagram[Hodges 1983]

2.1.1 Basic MOSFET operation

For initial analysis of the MOS-transistors operation, the effect of the gate voltage on the channel will be considered. With no gate voltage applied there is a deficit of n-type carriers (electrons) in the channel region due to the doped p-type substrate, which has an excess of holes. Negligible current can flow in this condition. As  $V_G$  is



increased, the positive bias on the gate produces a transverse electric field across the channel region, this attracts electrons that form an inversion layer. The inversion layer is an induced n-type region which increases the conductance of the channel, causing a current to flow between the positively biased drain and the grounded source regions. The point at which the transistor begins to conduct is referred to as the threshold voltage,  $V_T$ . The magnitude of  $V_G$  determines the conductance of the channel and hence the output current flow,  $I_D$ . A larger gate bias accumulates more electrons and causes an increase in  $I_D$ . The graph displayed in figure 2.2 shows this relationship between the gate voltage and the output current. The relationship between  $I_D$  and  $V_G$  is not linear and the reasons behind this are discussed in the next section.



**Figure 2.2** Turn on characteristics of a n-MOSFET

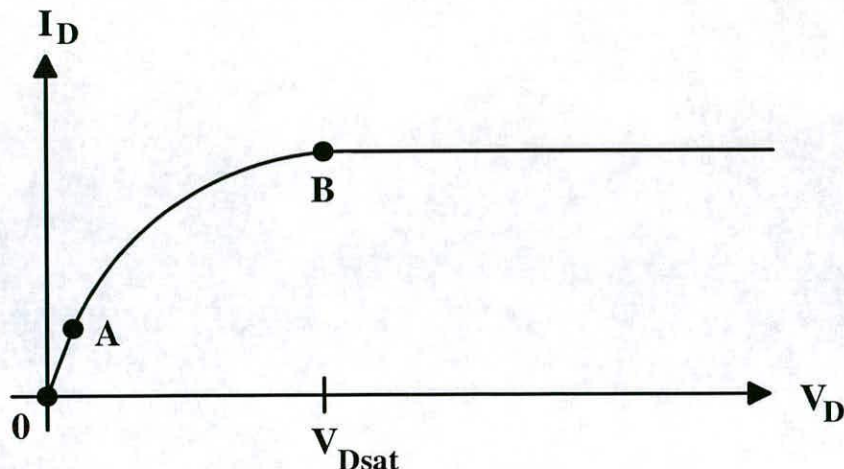
### 2.1.2 I-V characteristics of the MOSFET

There are three main regions of operation for the MOSFET:

- Subthreshold
- Linear
- Saturation

Subthreshold operation occurs when the gate voltage,  $V_G$ , is less than the threshold voltage ( $V_G < V_T$ ). Under these conditions the transistor is switched off, this is discussed in more detail later in this section. The linear and saturation regions of

operation occur under strong inversion ( $V_G > V_T$ ) and the current that flows through the channel,  $I_D$ , under these conditions is shown in figure 2.3.

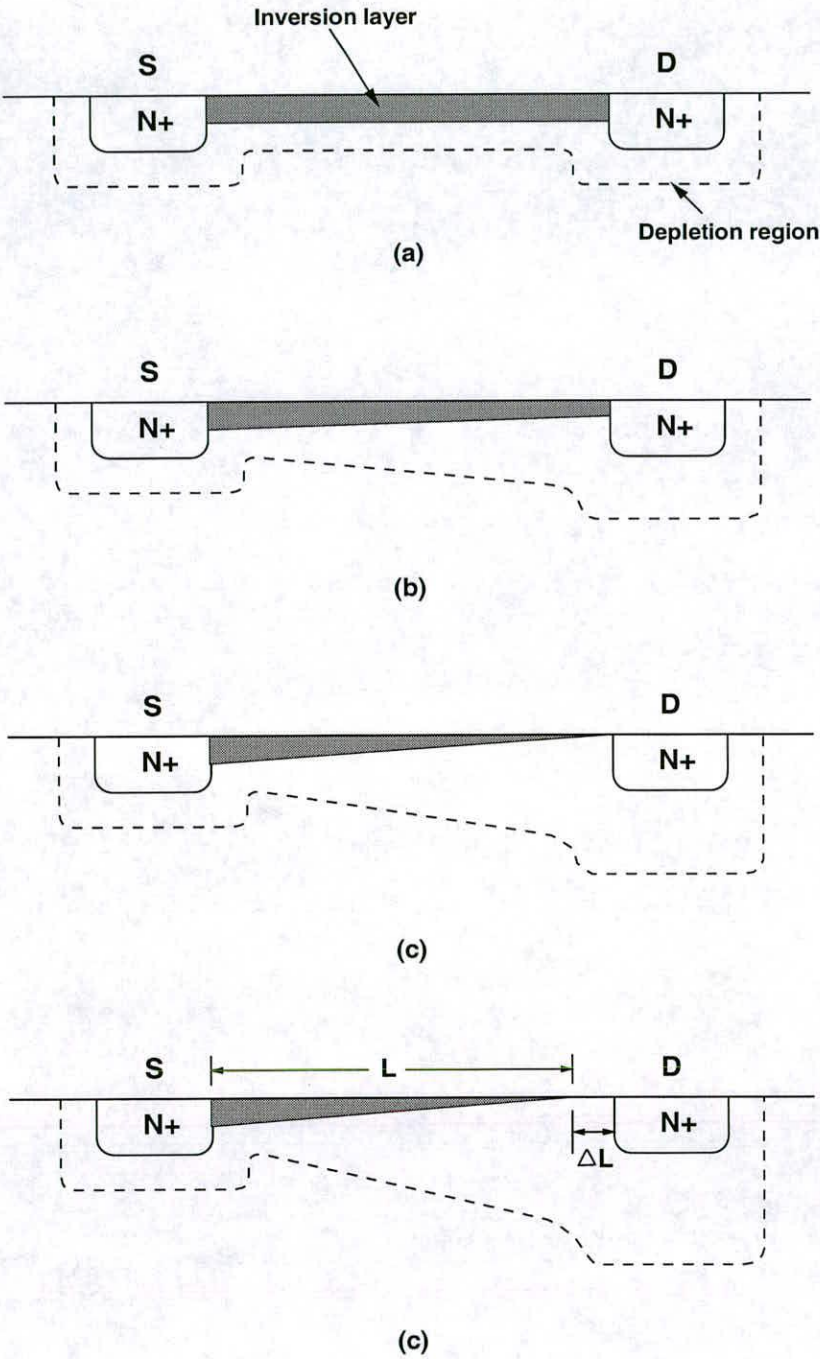


**Figure 2.3** The variation of  $I_D$  with increasing  $V_D$  for a fixed  $V_G > V_T$

With  $V_D$  at a small positive voltage the inversion region in the channel remains uniform over its length, shown in figure 2.4a. The current,  $I_D$ , increases linearly with the increase in  $V_D$  as the conductance of the channel remains constant under these conditions. This region of operation is indicated in figure 2.3 between points 0 and A and is referred to as the linear region. As  $V_D$  increases beyond a few tenths of a volt the current flowing in the channel causes a voltage gradient across the length of the channel, which in turn produces a widening of the depletion region under the gate at the drain end of the channel (see figure 2.4b). The mobile charge concentration in the inversion layer of this region decreases with the widening of the depletion region and causes a lowering of the channel conductance. The gradual increase in  $V_D$  therefore results in a smaller increase in  $I_D$ , which is displayed in the  $I_D$ - $V_D$  characteristics of figure 2.3 between points A and B. If  $V_D$  is sufficiently increased so that  $V_D = (V_G - V_T)$  the inversion layer decreases to zero at the edge of the drain. This is shown in figure 2.4c and is referred to as *pinch-off*. The pinch-off point is represented in figure 2.3 at the point B, and occurs at the saturation voltage,  $V_{Dsat}$ . Any further increase in  $V_D$  after  $V_{Dsat}$  causes a further widening of the pinch-off region,  $\Delta L$ , as shown in figure 2.4d. This widening occurs because the gate voltage is no longer sufficient to establish inversion in the pinch-off region. Most of the voltage increase above  $V_{Dsat}$  is dropped across the pinched-off region  $\Delta L$  and because of this  $I_D$  does not



significantly increase with a rise in  $V_D$  above  $V_{Dsat}$ . This remains valid as long as  $L \gg \Delta L$ . However, as  $\Delta L$  approaches the value of  $L$ , usually only occurring in short channel MOSFETs, the effect on  $I_D$  is increased and is explained in more detail in section 2.2.1.



**Figure 2.4** Visualisation of the regions of operation for the MOSFET: a)  $V_D \approx 0V$ , b) Inversion layer narrowing under moderate  $V_D$  biasing, c) pinch-off and d) post pinch-off,  $V_D > V_{Dsat}$

### Linear and Saturation regions of operation

The linear and saturation characteristics of the MOSFET can be quantified with equations to describe the devices operation. The equations are derived from models such as the Pao-Sah[Poa 1966], charge sheet[Baccarani 1978], bulk-charge[Brews 1978] and square law[Pierret 1983] models all varying in complexity and hence computational time. The simplest model, the square law model demonstrates the parameters that affect the operation of the MOSFET under strong inversion.

The square law model assumes that the electric field is constant across the length of the channel region and is perpendicular to the current flow. In the linear region the equation that models the current flow is given in equation 2.1.

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[ (V_G - V_T) V_D - \frac{V_D^2}{2} \right] \quad 2.1$$

where:

$I_D$  - Drain current

$\mu_n$  - Carrier mobility

$C_{ox}$  - Gate oxide capacitance

$W$  - Width of device active area

$L$  - Channel length

$V_G$  - Gate voltage

$V_T$  - Threshold voltage

$V_D$  - Drain voltage

In the post pinch-off regime, when the device is operating in saturation, an increase in the drain voltage is assumed to cause no increase in the drain current. The current equation is then modelled by equation 2.2.

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[ (V_G - V_T)^2 \right] \quad 2.2$$



The relationships between the output current and the gate and drain voltages, shown in equations 2.3 and 2.4, are expressed as the drain conductance  $g_d$  and the transconductance,  $g_m$ .

$$g_d = \frac{\partial I_D}{\partial V_D} \quad 2.3$$

$$g_m = \frac{\partial I_D}{\partial V_G} \quad 2.4$$

Differentiating equations 2.1 and 2.2 give expressions for  $g_d$  and  $g_m$ .

$$g_d = \mu_n C_{ox} \frac{W}{L} [V_G - V_T - V_D] \quad 2.5$$

$$g_m = \mu_n C_{ox} \frac{W}{L} [V_G - V_T] \quad 2.6$$

### Subthreshold region of operation

When the MOSFET is biased in weak inversion ( $V_G < V_T$ ) the current which flows in the channel is referred to as the subthreshold current,  $I_{Dst}$ . This current occurs because of the small number of carriers present in the channel. The equations from the square law model that were previously used to describe the behaviour of the MOSFET assume  $I_D=0$  when  $V_G > V_T$  and are, therefore, not useful in calculating  $I_{Dst}$ . The equation used to approximate the subthreshold current [Wolf 1995], shown in equation 2.7, is derived from the charge sheet model of current flow, which can account for the diffusion current in the MOSFET that is predominant when operated under weak inversion.

$$I_{Dst} = qD_n \frac{W}{L} \frac{kT}{q} \frac{\sqrt{\kappa_{si}\epsilon_0}}{\sqrt{2qN_A\phi_{surf}(source)}} \frac{n_i^2}{N_A} \exp\left(\frac{q\phi_{surf}(source)}{kT}\right) \quad 2.7$$

where:

$q$  - electron charge

$D_n$  - electron diffusion constant

$k$  - Boltzmann constant

$T$  - temperature

$N_A$  - number of acceptor atoms

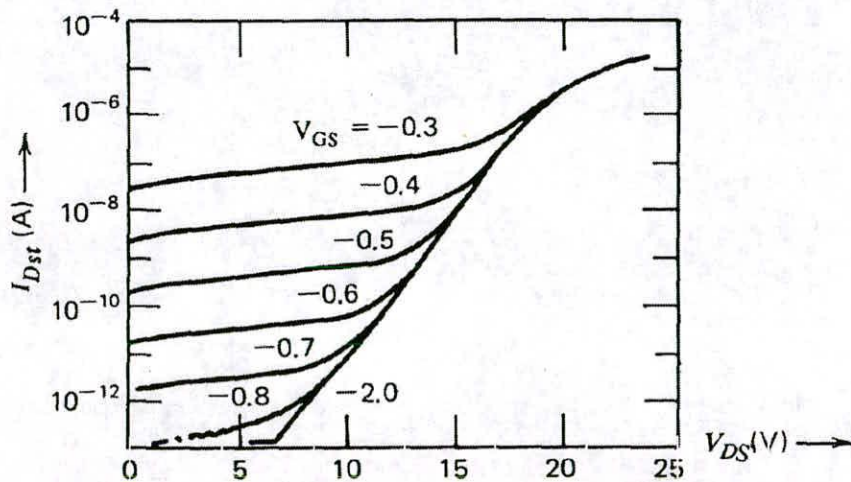
$\phi_{\text{surf}}$  - surface potential

$\kappa_{\text{si}}$  - semiconductor dielectric constant

$\epsilon_0$  - permeability of free space

$n_i$  - intrinsic carrier concentration

The component  $\phi_{\text{surf}}^{(\text{source})}$  is roughly proportional to  $V_G$  in the subthreshold region, which implies that  $I_{\text{Dst}}$  is exponentially dependant on  $V_{\text{GS}}$ . This relationship is shown in figure 2.5 which is a logarithmic plot of the current against gate voltage for a long channel MOSFET.



**Figure 2.5** Subthreshold characteristics for a long channel device [Troutman 1974]

The slope of the subthreshold curve is an important factor in the MOSFET's operation. The inverse of this slope is known as the subthreshold swing,  $S_t$ , and indicates how effectively the transistor can be switched off, i.e., the steeper the slope the more effective the switch off.  $S_t$  is calculated using equation 2.8



$$S_t = \ln 10 \left( \frac{d \ln I_D}{dV_G} \right)^{-1}$$

2.8

The value of  $S_t$  is expressed in mV/decade and a typical value for a long channel MOSFET is around 70mV/decade.

Another form of leakage current that occurs in the MOSFET when it is in the subthreshold region of operation is the gate-induced drain leakage (GIDL). This leakage current flows when the gate is grounded and the drain is at the supply voltage. A depletion region forms around the drain under the gate because of the electric field that occurs across the oxide, shown in figure 2.6. If the electric field becomes large enough an inversion layer attempts to form at the silicon surface of the drain. As the minority carriers move to form the inversion layer they are influenced by the substrate, which is at a lower potential, and drawn sideways to the substrate. This movement of minority carriers constitute the GIDL current.

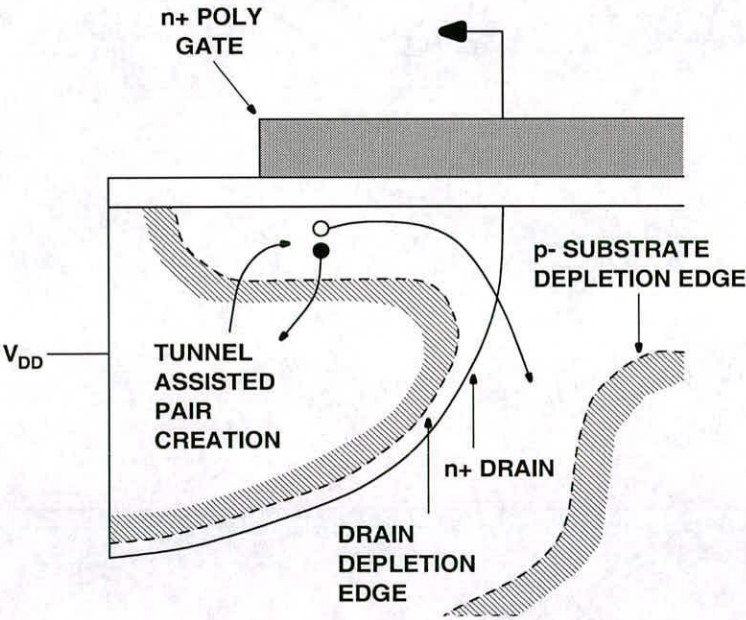


Figure 2.6      Gate induced drain leakage current in a MOSFET

2.1.3 Threshold Voltage

The threshold voltage has been previously defined as the applied voltage at which the channel of the MOSFET starts to conduct. The equation which defines  $V_T$  in a uniformly doped channel, with  $V_B = 0$ , is given by [Wolf 1995]:

$$V_T = \phi_{ms} - \frac{Q_{tot}}{C_{ox}} + \frac{2\sqrt{\kappa_{si}\epsilon_0qN_{sub}\phi_B}}{C_{ox}} + 2\phi_B$$

2.9

where:

$\phi_{ms}$  - metal-semiconductor workfunction difference

$Q_{tot}$  - total electronic charge

$N_{sub}$  - substrate doping concentration

$\phi_B$  - semiconductor doping parameter

The curves in figure 2.7 show the calculated values of  $V_T$  as a function of gate oxide thickness,  $t_{ox}$ . The graph highlights two variables of gate oxide thickness and substrate doping, which affect the value of  $V_T$ . For MOSFETs the gate oxide thickness is designed to maximise the output current,  $I_D$ , with the substrate doping of the channel region used to adjust the value of the threshold voltage.

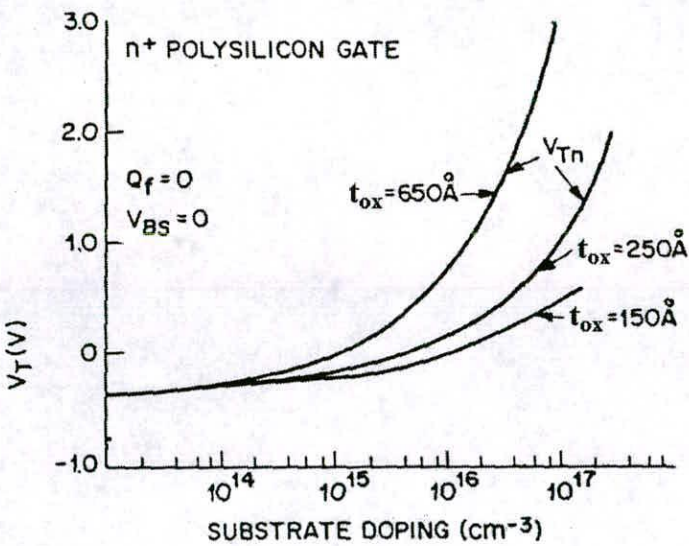


Figure 2.7      Calculated threshold voltages of a nMOSFET as a function  $N_{sub}$  and  $t_{ox}$ [Sze M, 1988]



The substrate doping is normally performed by implanting a thin layer of impurity atoms in the channel region. This causes the substrate to become non-uniformly doped. The equation for the threshold voltage has to take this non-uniformity into account and the modifications are shown in equation 2.10.

$$V_T = \varphi_{ms} - \frac{Q_{tot}}{C_{ox}} + 2\varphi_B + \frac{qD_I}{C_{ox}} + \frac{\sqrt{2\kappa_{Si}\epsilon_0 q N_A \varphi_B}}{C_{ox}} \left( \frac{2\varphi_B + qD_I x_i}{2\kappa_{Si}\epsilon_0} \right)^{\frac{1}{2}} \quad 2.10$$

where:

$D_I$  - dose of implanted ions

$x_i$  - implantation depth of impurities

## 2.2 The Short Channel MOSFET

The trend of MOSFET design is the reduction in size of the patterned features. Each progressive device generation reduces the minimum feature size to increase the density of transistors on the silicon and increase the drive current,  $I_{Dsat}$ , and hence the operating speed. The main feature that is scaled to improve device performance is the gate length, which increases the current drive of the transistor. The gate oxide thickness is also reduced and the source/drain regions are decreased in depth. All of these parameters impact the operating characteristics of the devices and the models described in the previous section, for long channel transistors, do not accurately define the characteristics of the MOSFET. This phenomena is referred to as “short-channel effects”. The short channel effects describe three main areas of the MOSFETs characteristics that are affected by the feature size reduction:

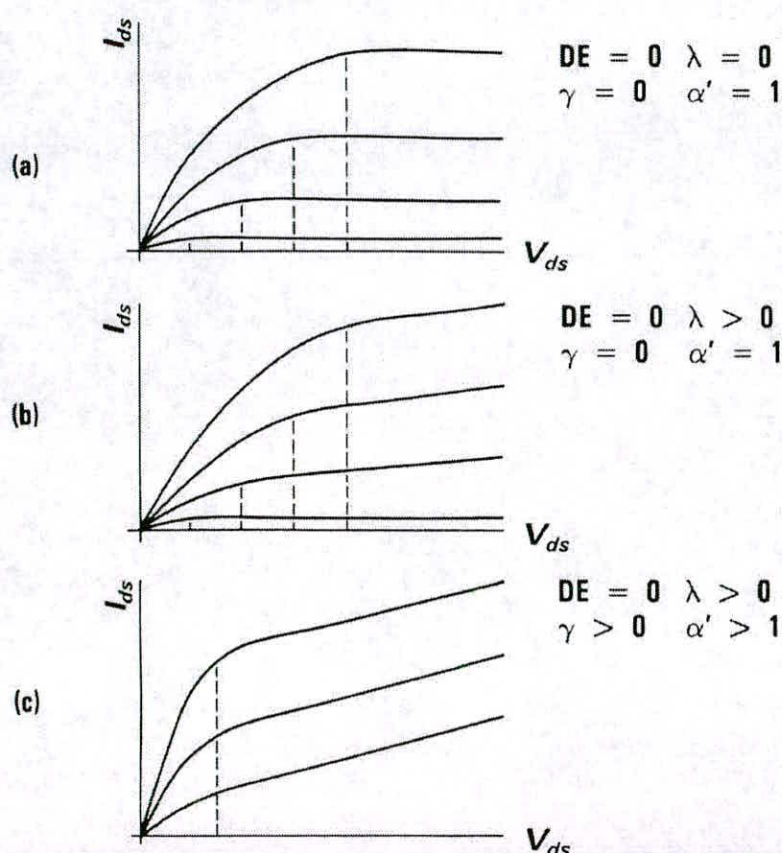
- $I_D$  is not as predicted by the long-channel models
- Subthreshold currents are increased
- Device reliability is reduced

The subsequent sections will discuss these effects and describe the steps that can be used to minimise their influence on the operation of short-channel MOSFETs.

## 2.2.1 Short-channel device operation

### Current-Voltage Characteristics

As the gate lengths of MOS transistors are reduced the prominence of short channel effects on the current-voltage characteristics increases. These occur as the electric fields from the junction regions and gate electrode have a greater effect on the relatively smaller channel region. The characteristics of the I-V curves of MOS transistors change with the onset of short-channel effects and begin to deviate from the long channel curves, that are shown in figure 2.8a.

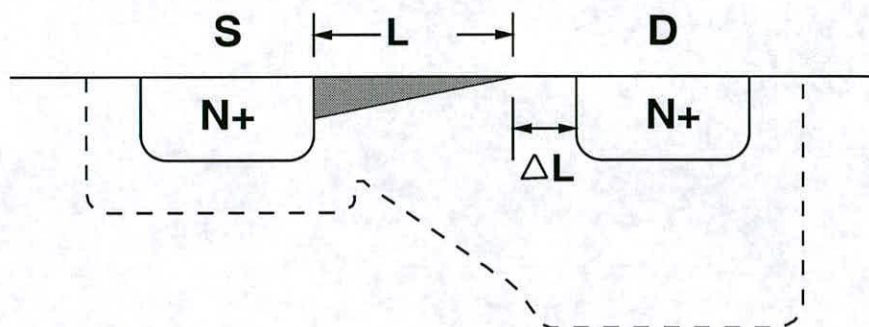


**Figure 2.8** Diagrams of increasing short channel behaviour in MOSFETs. a) Long channel behaviour, b) with channel modulation, and c) with velocity saturation[Duvvury 1986]

When operated in saturation ( $V_G > V_T$ ) the short channel transistor exhibits a constant rise in drain current with an increasing value of  $V_D$ , shown in figure 2.8b. This is due to the effect of the channel length modulation factor,  $\lambda$ . This occurs when the MOSFET is operating in saturation because the pinch-off length,  $\Delta L$ , in short channel



devices (see figure 2.9) approaches the same size as the remaining effective channel length,  $L_{\text{eff}}$ . With most of the excess voltage above  $V_{\text{Dsat}}$  dropped across  $\Delta L$ , the voltage across  $L_{\text{eff}}$  remains constant. However, with increasing  $V_{\text{D}}$ , and hence a lengthening value of  $\Delta L$ , the size of the channel progressively gets shorter. This increases the current drive of the transistor and hence causes a rise in the output current. In longer channel length transistors this effect is not as apparent because the size of  $\Delta L$  is only a small fraction of the size of  $L_{\text{eff}}$ , thus having negligible impact on the gain of the transistor.



**Figure 2.9** Diagram showing the pinched-off region,  $\Delta L$ , in the channel of a short channel length MOS transistor operating in saturation.

Velocity saturation effects also influence the I-V characteristics of short channel MOSFETs. The carriers in the channel reach a saturation velocity when the lateral electric field reaches a critical value,  $\epsilon_{\text{sat}}$ , and this occurs with the formation of the pinched-off region in the channel. The depletion region, from the drain, extends into the channel and in short-channel devices  $\epsilon_{\text{sat}}$  occurs closer to the source. This has the effect of the current saturation point,  $V_{\text{Dsat}}$ , occurring at approximately the same value of  $V_{\text{D}}$ , independent of the effect of the gate voltage. This effect is shown in figure 2.8c.

The I-V characteristics are also affected by the reduction in the mobility of the carriers in the inversion layer of short-channel devices. The mobility degradation factor,  $\theta$ , is the parameter that describes the mobility reduction of the carriers and is an empirically defined value. The mobility is reduced because of scattering of the surface charge carriers at the Si/SiO<sub>2</sub> interface that are acted upon with a transverse



electric field from the gate electrode. While this effect is present in long channel transistors it is more pronounced in short-channel devices, as the electric fields are higher because of the reduced dimensions of the channel region. The effect causes a reduction of the gain of the device, hence reduced current drive, in both the linear and saturation regions of operation.

### Subthreshold characteristics

When the MOSFET is switched off, with the gate voltage below threshold, there are three components that contribute to the leakage current; punchthrough,  $I_{PT}$ , which is a sub-surface current flowing from the drain to the source, a surface diffusion current and the gate-induced drain leakage (GIDL) current,  $I_{GIDL}$ , which was discussed in section 2.1.2.

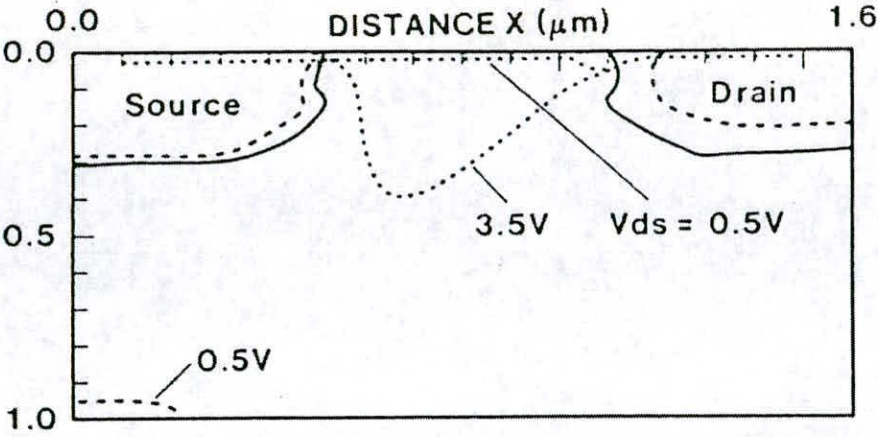
Punchthrough is an effect that occurs when the source and drain depletion regions merge together, causing a larger drain current than is predicted with the long-channel MOSFET equations. This is because the gate, that controlled  $I_D$  with the applied electric field, can no longer influences the current flow and  $I_D$  increases exponentially with applied  $V_D$ . Punchthrough can place a limit on the maximum drain voltage that can be applied to the MOSFET and hence limit the output current,  $I_D$ . The voltage at which punchthrough occurs is related to the doping profile of the channel and the effect of the gate, but a simple one-dimensional approximation of the punchthrough voltage,  $V_{PT}$ , is shown in equation 2.11[El-Kareh et al, 1986]. From this it can be determined that  $V_{PT}$  is proportional to the level of substrate doping and the square of the channel length.

$$V_{PT} = L^2 N_a \frac{q}{2\epsilon_0 \epsilon_{Si}} \quad 2.11$$

The doping in the channel region, from the  $V_T$  adjustment implant, affects the magnitude of the junction depletion regions. The increased doping near the surface of the channel reduces the depletion widths at the surface, compared to lower down in the bulk, where the regions converge to produce a sub-surface current flow[Zhu 1988]. Figure 2.10 shows the predominant path of  $I_{DST}$  change from a surface current

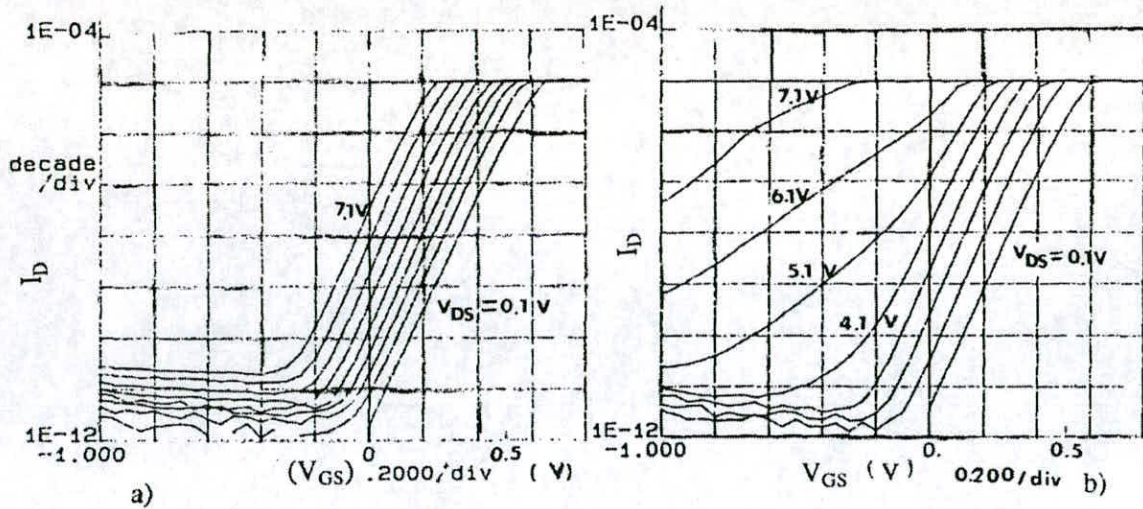


at low  $V_D$ , to a subsurface current at high  $V_D$ . From equation 2.11 it is evident that  $V_{PT}$  can be raised by increasing the doping level.



**Figure 2.10** Punchthrough current paths (dotted) in a surface-channel nMOSFET with  $V_D=0.5$  and  $3.5V$ . Solid line shows the depletion region edge[Zhu 1988].

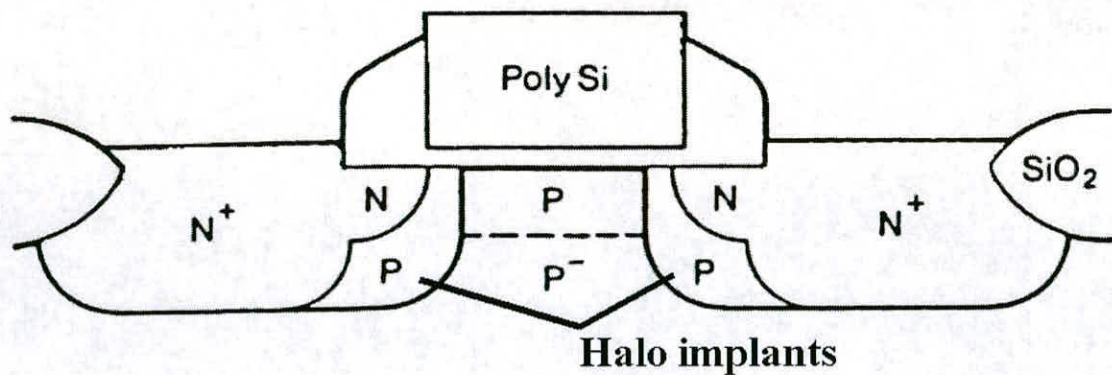
The onset of punchthrough also affects the value of the subthreshold swing.  $S_t$  increases in value with the onset of punchthrough. This is shown in figure 2.11. The curves of the long channel MOSFET in figure 2.11a do not exhibit punchthrough, as they show no change in  $S_t$  as  $V_D$  is increased. The curves of the short channel MOSFET in figure 2.11b, however, gradually begin to flatten out with increasing values of drain current, thus increasing the value of  $S_t$ . The increase in  $S_t$  occurs because there is an increase in the drain current at low gate voltages, due to the influence of the junction depletion regions merging across the shorter channel length with the increasing drain voltage.



**Figure 2.11** Subthreshold curves for,  $\log I_D$  versus  $V_{GS}$ , for a) Long channel nMOSFET and b) Short channel nMOSFET [Wolf 1995]

Punchthrough can be reduced by increasing the doping in the substrate region where the subsurface current flows. The increased doping decreases the size of the junction depletion regions, in the same way as the channel doping implant. The doping can be increased with an implantation of atoms, p-type for the nMOSFET, at an energy which locates the ion impurities in the substrate below those for the  $V_T$  adjustment implant. This implant is known as a *punchthrough stopper implant*. A development of this technique is to locally implant the impurities in the regions around the junctions, shown in figure 2.12, by tilting the sample as the implant is performed. This technique is referred to as *halo implantation* [Jung 1996]. The heavily doped inside sidewalls of the junctions suppress the extension of the depletion regions with increasing  $V_D$ , thus reducing the punchthrough effect.



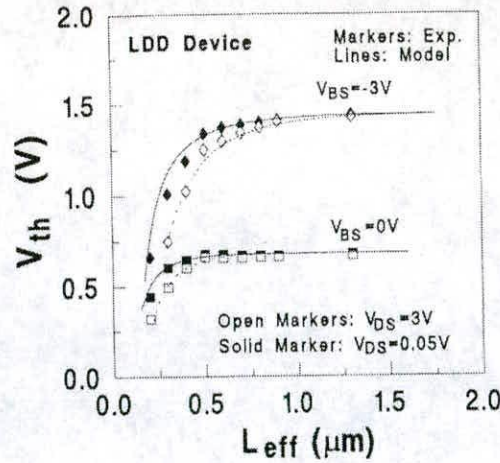


**Figure 2.12** Halo  $p^+$  implants around the junctions of a nMOSFET[Codella 1985]

At low drain biases in short channel transistors a surface current can initiate the punchthrough effect[Fu 1997]. The effect dominates the subthreshold current until the drain voltage increases enough to produce bulk punchthrough, as described in the previous paragraph. The current path of surface current is shown in figure 2.10 for the low drain voltage of 0.5V.

### Threshold voltage

The reduction in the channel length of MOSFETs affects the value of the threshold voltage,  $V_T$ . In very short channel devices the threshold voltage reduces dramatically as the device's effective gate length is reduced, as shown in figure 2.13. This occurs because of the effects of the lateral electric fields from the source/drain junction regions. As the channel length,  $L$ , approaches the dimensions of the source/drain junction depletion widths, a larger part of the channel-depletion region begins to consist of the space charge in the junction depletion regions. Under these conditions less gate charge is required to invert the channel of the MOS transistor, causing the appearance of a lowering of  $V_T$ . This effect can be suppressed with an increase in the doping of the channel region, that reduces the lateral electric fields in the channel by curbing the junction depletion regions.



**Figure 2.13** Threshold voltage as a function of effective channel length[Liu 1993]

Modelling the threshold voltage in short-channel devices therefore requires the lateral electric fields and their effect on the channel region to be considered, unlike the longer channel equation given with equation 2.10. The method of analysis to characterise the change in  $V_T$  is to calculate the shift in the threshold voltage,  $\Delta V_{Tsc}$ , from the one-dimensional value calculated using the model given in equation 2.10. Liu et-al determined a quasi-two-dimensional model to determine  $\Delta V_{Tsc}$ , which is given by [Liu 1993]

$$\Delta V_{Tsc} = 3(V_{bi} - 2\phi_B) + V_D e^{-L/l} + 2\sqrt{(V_{bi} - 2\phi_B)(V_{bi} - 2\phi_B + V_D)} e^{-L/2l} \quad 2.12$$

where:

$$l = \sqrt{\frac{\epsilon_{si} t_{ox} d_{max}}{\epsilon_{ox} \eta}} \quad 2.13$$

$V_{bi}$  - built in potential between source-substrate and drain-substrate junctions

$l$  - characteristic length

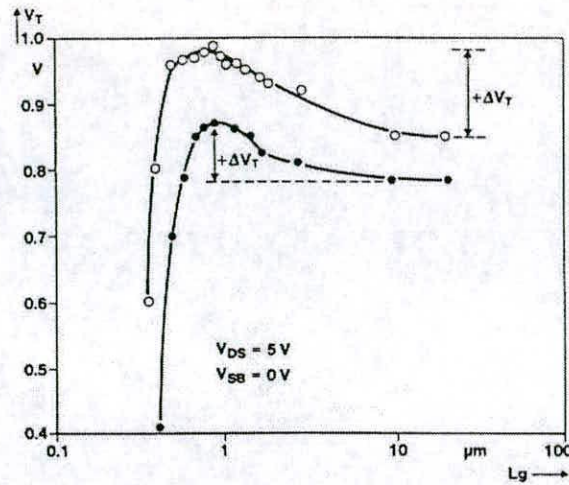
$\epsilon_{ox}$  - Oxide permittivity

$\eta$  - Fitting parameter

The overall effect of a reduction in the channel length of MOS transistors shows a decrease in the value of the threshold voltage, as described by the two-dimensional analysis of equation 2.12. Observation of fabricated short-channel devices, however,



shows an anomalous initial increase in  $V_T$  with a reduction in channel length, shown in figure 2.14 as a shift  $\Delta V_T$ . This increase in  $V_T$  is described as a reverse short channel effect (RSCE).



**Figure 2.14** Reverse short channel effect on threshold voltage[Orlowski 1987]

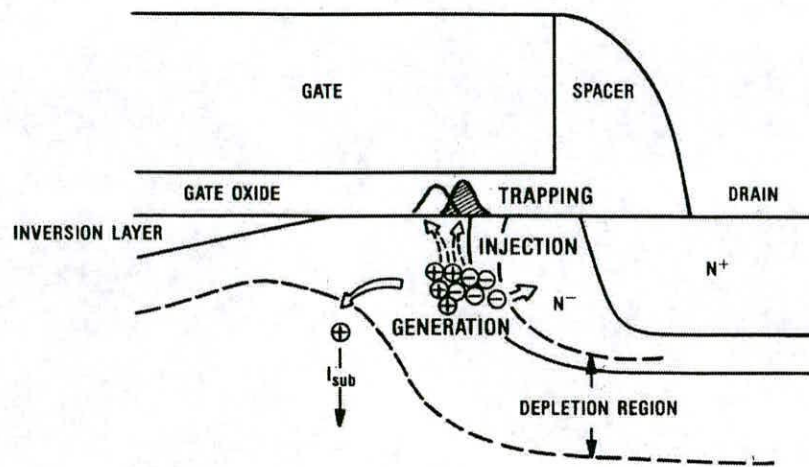
The cause of the threshold rollup due to the reverse short channel effect has been attributed to the localised pileup of channel dopants along the edge of the gate at the silicon-silicon dioxide interface. The magnitude of the effect can be reduced by adjusting the processing stages of the device fabrication[Lutze 1995]. The main processing step to affect the threshold rollup is thought to be the source/drain junction implantation that causes interstitials in the lattice that leads to transient enhanced diffusion of the channel dopant[Chaudrhry 1997]. The profile of the channel doping has also been shown to affect the magnitude of the RSCE[Lutze 1995], though adjusting the profile of the channel implant also changes many of the transistors' characteristics, such as short channel effects, which can lead to a compromise of the devices performance.

### 2.2.2 Device Reliability

Reliability is a primary concern to the integrated circuit designer, where millions of transistors can be incorporated onto a single chip design. Failure within a chip can come from two key areas[Chenming 1993]; firstly from the gate oxide and secondly the metal level for the interconnects. At the device level the gate oxide reliability is of primary concern and this type of failure is discussed in the following sections.

### Hot carrier degradation

Hot carrier degradation occurs in the gate oxide of a MOSFET when the carriers in the channel and pinch-off region, gain sufficient energy, from the lateral electric field, to surmount the energy barriers and tunnel into the oxide from the silicon. The problem is exaggerated in n-channel devices as the Si/SiO<sub>2</sub> energy gap for the carriers is smaller at  $\approx 3.1\text{eV}$  for the electrons than  $\approx 4.9\text{eV}$  for holes. Typical effects caused by hot-carriers include a shift in the threshold voltage, a change in the subthreshold swing and a reduction in the transconductance and hence current drive [Chen 1988].



**Figure 2.15** Illustration of hot-carrier effects including hot-carrier generation, injection and trapping [Chen 1988].

The main hot carrier effects of hot-carrier generation, injection and trapping are shown in figure 2.15. A high drain field generates hot carriers, which channels hot electrons and electron-hole pairs generated by impact ionisation. The generation tends to occur in the high field area of the channel called the velocity saturation region, which is produced when the device is operated in saturation, between the drain and the pinched-off inversion layer, shown in figure 2.15. The magnitude of the electric field also affects the injection of the hot-carriers into the oxide. A lower field strength corresponds to a lower electron temperature, or energy, and therefore less



probability of gaining sufficient energy to break through the Si/SiO<sub>2</sub> interface. The probability of a carrier being injected into the oxide can be expressed as[Chen 1988]:

$$p = \exp\left(\frac{\phi_b}{kT_e}\right) \exp\left(-\frac{x}{\lambda}\right) \quad 2.14$$

where:  $\phi_b$  - energy required for electrons to surmount the Si/SiO<sub>2</sub> barrier  
 $T_e(x)$  - electron temperature  
 $x$  - distance from the interface  
 $\lambda$  - energy dependant mean free path

The mechanisms of hot carrier trapping include bulk oxide trapping and interface trap generation. The predominant form of degradation is thought to occur by interface trap generation with the simultaneous injection of holes and electrons[Groeseneken 1995]. The injection of holes however are most effective by about four orders of magnitude over that of electrons. With LDD n-MOS devices the trapping of electrons in the sidewall spacer can enhance current degradation through an increase in the series resistance.

There are three main strategies for improving the hot-carrier effects in MOSFETs: Drain engineering, oxide quality and power supply reduction. Strategies for drain engineering have included the introduction of the lightly doped drain (LDD), where the doping concentration of the device's junction is reduced with a shallow implant either side of the gate, shown as the N-well extension in figure 2.12. The lower doping concentration reduces the peak of the lateral electric field near the drain and hence reduces the generation of the hot-carriers. It has also been reported[Song 1996] that an optimised halo/LDD structure at the junctions can reduce the effects of the hot-carriers by limiting their generation. Oxide quality is an important factor in increasing the life-span of MOSFETs. The reliability of the standard SiO<sub>2</sub> process has been shown to be improved upon with the introduction of nitrided oxides[Sodini 1992]. This process reduces the interface trap generation because of the presence of

nitrogen at the Si/SiO<sub>2</sub> boundary, but without optimisation of the process the influence of charge trapping increases. There is, however, a trade off with this process because of a slight degradation of the electrical characteristics over SiO<sub>2</sub>. Reduction of the drain voltage produces a corresponding reduction of the lateral electric field in the channel region, though this circuit parameter is generally outwith the control of the design engineer and is instead set for the technology generation of the devices. The supply voltage for the 0.25 $\mu$ m generation is 2.5-1.8V, which is projected to drop to 1.2-0.9V for the 0.1 $\mu$ m generation[SIA, 1997].

## 2.3 MOSFET Device Scaling

The scaling of MOSFET devices involves the downsizing of the major features of the device, including the physical dimensions and the electrical constraints, such as power supply. This section discusses the basic theory of scaling strategies and the future implementation of different scaling scenarios. A prediction of the future scaling trends is also highlighted.

### 2.3.1 Scaling strategies

#### Constant electric field scaling

The basis of scaling strategies is to reduce the dimensions of a MOS device while still maintaining the same long channel characteristics. The basic strategy is constant electric-field (CE) scaling, where the electric field potentials within a device are kept constant, while the dimensions and properties are changed using a scaling factor  $\alpha$  ( $\alpha > 1$ )[Dennard 1974]. The physical dimensions of the device are reduced by the factor  $1/\alpha$  and the electric fields within the device are kept constant by reducing the operating potentials by  $1/\alpha$  and increasing the doping concentration by  $\alpha$ . This technique increases the packing density of devices by  $\alpha^2$  and the speed by  $\alpha$ , while the power dissipation is reduced by  $\alpha^2$ . [Davari 1995].



Actual scaling strategy

The scaling of MOSFETs has taken a slightly different path than the proposed method of CE scaling. While the dimensions of the devices were decreased in accordance with the scaling theory, the power supply was maintained at the same 5V level as previous generations. This level was maintained until the 0.5μm generation of transistor, where the power supply was reduced to 3.3V. The power supply levels of the different generations of transistors was kept constant, because it allowed design compatibility between the levels, even though the electric field in the MOSFET was increasing with the progressive decrease in the gate length feature sizes. The increase of electric fields within the devices was accounted for with a more generalised scaling strategy[(I)Baccarani 1984], where the electric field patterns within a scaled device are still preserved, but the intensity of the field can be changed everywhere in the device by a multiplication factor  $\epsilon$ . The relationship between the generalised theory and constant-electric field scaling is shown in table 2.1. The supply voltage is scaled less rapidly by a factor  $\epsilon/\alpha$ , while the electric field patterns are maintained by increasing the doping concentrations by the factor  $\epsilon$ . Limits to the generalised scaling include the gradual increase in electric field which leads to long term reliability problems from gate insulator failure or hot-carrier effects.

Physical parameters	Constant-electric field scaling factor	Generalised scaling factor
Linear dimensions	$1/\alpha$	$1/\alpha$
Electric-field intensity	1	$\epsilon$
Voltage (Potential)	$1/\alpha$	$\epsilon/\alpha$
Impurity concentration	$\alpha$	$\alpha$

Table 2.1      Relationships between constant-electric field and generalised scaling[Davari 1995]

Scaling MOSFETs to 0.1μm and below

As the dimensions of MOSFETs are reduced further down to 0.1μm the scaling of devices becomes constrained by the physical limits of the scaling parameters[Iwai



1998]. Parameters such as gate insulator thickness and channel length will approach a limit where scaling can no longer occur. As these limits are approached the scaling strategy has to consider a trade off between increased device performance and reliability. Channel hot-carrier effects limit the selection of optimum power supply voltage for devices below  $0.25\mu\text{m}$ , and these effects have been discussed in section 2.2.2. Drain engineering with increased doping affects the performance of the device by increasing the source/drain resistance, although these effects can be counteracted with the use of silicides at the source, drain and gate connections to lower the sheet resistance of the silicon or polysilicon material [Murarka 1983]

### 2.3.2 High performance and low power scaling scenarios

With the scaling of MOSFETs being a trade off between device performance, reliability and subthreshold current, two different scenarios for scaling have been proposed [Davari 1995]. The high performance and low power scenarios, shown graphically in figure 2.16, provide an outlook for device scaling with the focus for each strategy focused on a different goal. The high performance scenario uses a higher supply voltage, for a given channel length, over the low power version. The electric fields within the device will be higher and so adequate long term device reliability has to be maintained. The gate oxide thickness and doping profiles are optimised with this scenario to provide low off and high drive current without the electric field producing gate oxide tunnelling and GIDL current. The low power scenario uses a reduced supply voltage, compared to the high performance case, with the aim to reduce the power dissipation per device and therefore maintain a lower power density.



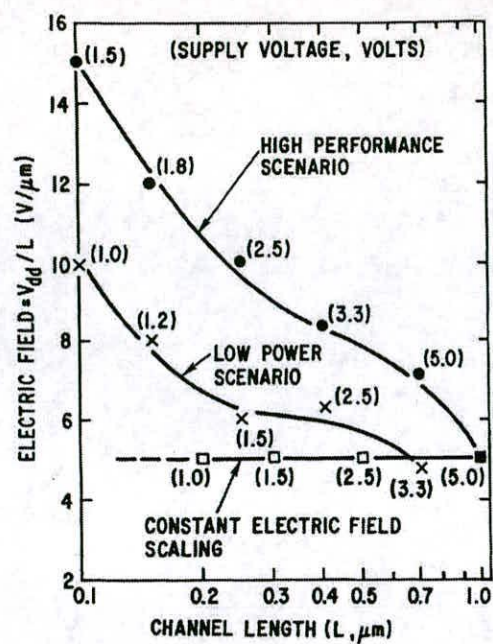


Figure 2.16 A measure of the electric field,  $V_{DD}/L$ , as a function of channel length for various scaling scenarios[Davari 1995].

2.3.3 Scaling projections

The introduction of MOS technology generations to the marketplace followed a 3-year cycle. The projections for the introduction of future technologies are documented by the Semiconductor Industry Association (SIA), and the lead time between generations with the latest predictions are a two year gap between the introduction of a new technology[SIA, 1997]. The projections for the scaling of future technologies by the SIA are shown in table 2.2.

Minimum Feature Size for Dense lines (nm)	180	150	130	100	70	50
Minimum Feature Size for Gate Lithography (nm)	140	120	100	70	50	35
Year of Introduction	1999	2001	2003	2006	2009	2012
DRAM (bits)	1G	-	4G	16G	64G	256G
Supply Voltage (V)	1.5-1.8	1.2-1.5	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6

**Table 2.2** MOSFET technology projections[SIA, 1997]

## 2.4 Present Silicon Device Research

Research into future device technologies is presently focused on devices with minimum feature sizes of 100nm and below. Devices of 100nm dimensions, and operated at low temperature, were first reported by Sai-Halasz in 1987[Sai-Halasz 1987]. Since that time a number of papers have demonstrated MOSFETs, operating at room temperature, with dimensions of 100nm[Taur 1993][Yan 1992]. More recently research has investigated devices with fabricated gates of dimensions below 100nm. Ochiai et al have reported 40nm MOSFETs using electron beam lithography to fabricate the gate electrodes[Ochiai 1996]. The current-voltage curves of the devices displayed transistor operation although punchthrough was evident from the characteristic curves. A reduction in the short channel effects of the sub-100nm transistor has been reported by Kawaura et al with the fabrication of a dual gate in a 30nm gate length MOSFET[Kawaura 1998]. The dual gate involves the fabrication of a second longer gate over the existing gate in the device. This upper gate produces an inversion layer in the channel that acts like an ultra-shallow source/drain implant, reducing the short channel effects caused by the electrostatic field in the channel region.



## 2.5 Summary

This chapter has provided an introduction to MOSFET device operation. The parameters that affect the operation of both long and short channel devices have been highlighted, and the equations used to model the respective devices performance have been introduced. Some of the short channel effects associated with the miniaturisation of MOSFETs have been presented, with reference to the current-voltage, subthreshold and threshold voltage characteristics. Reliability considerations of hot carrier effects have been discussed with methods of failure prevention highlighted. Finally a discussion of device scaling strategies was displayed with a discussion of the current state of the art research into silicon device technology.

## **Electron Beam Lithography**

---

The progressive reduction of feature sizes in the fabrication of MOS devices puts an increasing demand upon the lithography techniques used to define the nano scale features. Industrial production of devices currently uses an optical lithography process and can define feature sizes down to 180nm. Research into future device technologies, however, requires much smaller feature sizes to be defined, predicted to be down to 70nm by the year 2006[SIA, 1997]. Electron beam lithography is an ideal approach for such narrow structure patterning as the system uses a finely focused electron beam of a few nanometers diameter to define the structures.

This chapter provides an overview of electron beam lithography. The technology of electron beam systems is explained in order to provide an insight into the design strategy of the Edinburgh built system that is illustrated in chapter 4 of this thesis. Alternative techniques, of optical and x-ray lithography are also described to provide a comparison of technologies available for pattern definition.

### **3.1 Electron beam lithography systems**

Electron beam pattern writing systems can be used in two roles for LSI production[Saitou 1996]. Firstly, as a direct write lithography tool for fabricating advanced devices and structures, and secondly as a mask making device for other lithography techniques such as optical and x-ray masks.

#### **3.1.1 A general system**

Electron beam lithography uses a high energy beam of electrons to define patterns on the substrate of a silicon wafer. The imaging beam is produced by an electron gun



and is focused on a photoresist coated substrate. The beam is then scanned across defined areas of the substrate by deflecting it in a controlled way. The single beam writes one pattern at a time, so multiple patterns are imaged sequentially. After exposure, the patterns are wet developed and rinsed to produce a patterned image with the remaining resist.

### **3.1.2 History of e-beam systems**

The development of electron beam lithography has progressed steadily since the mid 1960s[Watts 1989]. Initially the main impact of this technology was the fabrication of masks for lithography tools, such as optical steppers, and more recently for x-ray lithography. Another use of the systems has been for low-volume manufacture of advanced, small scale, high performance devices.

‘EBES’ (Electron beam Exposure system) was one of the first generation production e-beam lithography tools, it was developed at the Bell Laboratories in 1975[Herriott 1975] and was designed primarily for the production of high quality, economic lithographic masks. The system exposed patterns in negative photoresist on a chromium plated glass substrate. The electron beam process had better resolution, linewidth control and a lower defect density than the emulsion masks produced by optical fabrication at that time. The beam was continuously scanned across a 140 $\mu$ m field, and the full substrate area was imaged by continuously moving the stage and modulating the beam on and off to pattern the wafer. With this system the stage position could be measured to an accuracy of 30nm. Due to a fast patterning rate of 80MHz, masks with a field of approximately 5cm square were completed in 40 minutes.

By 1986 the system had been developed into the fourth generation EBES4[Alles 1986]. A brighter electron source and higher data rate increased the wafer throughput. Pattern definition was also changed to the more efficient vector scan method, where the patterns are broken into 2 $\mu$ m blocks and scanned individually by a figure generator. The maximum field size that can be written by the beam is 280 $\mu$ m,



but larger areas could be written by the continuously moving stage. The spot size of this system allowed higher resolution patterning with a reduction in size from  $0.5\mu\text{m}$  to  $0.125\mu\text{m}$

The advanced resolution of electron beam lithography systems has enabled research into MOS devices with dimensions much smaller than the optically defined alternative at any time. A paper by Mackintosh, in 1965[Mackintosh 1965], discussed the fabrication of MOS transistors with channel lengths of  $3.5\mu\text{m}$ . Optically defined transistors of the time had features in excess of  $10\mu\text{m}$ . As techniques in optical lithography improved, knowledge in electron beam processes increased and thus feature sizes of exposed patterns reduced. A 1981 paper from the central research labs of Hitachi Ltd[Okazaki 1981] reported n-MOS transistor circuits with  $0.6\mu\text{m}$  gate lengths. Again, the optical lithographic processes of the time were producing features 3-4 times larger than this. Reports of current processing with e-beam lithography describe devices with gate features defined below  $0.1\mu\text{m}$ , while state of the art optical lithography is processing features of  $0.18\mu\text{m}$ .

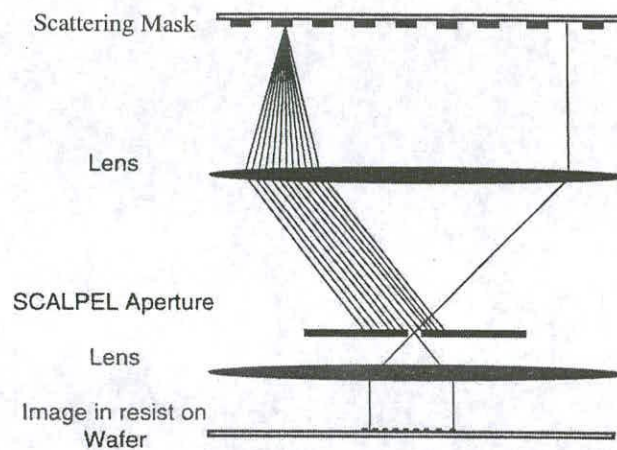
### **3.1.3 Current e-beam technology**

The direct write e-beam system still plays a major role in the fabrication of advanced devices for future technologies. However, a great deal of work is being directed at the use of e-beam as an industrial tool for the replacement of optical lithography, if in the future optical becomes impossible or uneconomical to use.

The SCALPEL system is an advanced projection lithography tool that has been developed for IC manufacture[DeJule 1999][Liddle 1995][Harriott 1996][Liddle 1998], a schematic diagram of the SCALPEL imaging strategy is shown in figure 3.1. Progress has been made with this technique using a mask to image patterns onto the wafer substrate. A thin, 100nm, membrane made of a low atomic number material constitutes the base material for the mask, while a high atomic number material is processed on top to provide the  $4\times$  mask pattern. High energy, 100keV, electrons are uniformly imaged over the mask in a  $1\times 1\text{mm}$  square electron beam. The electrons



pass through both layers of the mask, with the electrons that pass through the high atomic number mask material scattered and then blocked by an aperture before reaching the final imaging lens. Only the electrons that pass through the membrane material are imaged onto the wafer substrate.



**Figure 3.1** Schematic diagram of the SCALPEL imaging strategy[Harriott 1997]

This e-beam masking technique uses high energy electrons, which improves beam blurring and forward scattering. Previous electron beam lithography systems that employed a masking system have used stencil masks[Heritage 1975]. Stencil masks are membranes with gaps etched into the material to make transparent holes for electrons. The membranes absorb the electrons that do not pass through the holes, producing a masking effect. The limitations of this technique are that the absorption of electrons into the membrane causes significant heating of the mask, which can result in pattern distortions. The SCALPEL system does not suffer from these problems because the electrons are not absorbed by the mask, but scattered to be blocked by a mechanical aperture. Other problems that occur with stencil masks is their inability to print closed shape geometries, such as donut shapes. The SCALPEL systems mask has a continuous transparent membrane layer that enables such shapes to be patterned, with the masking material, on the surface. Limitations do however occur because of the fragile nature of the masks membrane material, with the size of the masks limited to strips of  $1\text{mm} \times 10\text{mm}$ . Larger mask designs can be

implemented by accurately stitching together different mask strips with an interferometrically measured stage positioning system.

The wafer throughput of 15 200mm wafer/hour is still inferior to the current optical stepper systems, though improvements to the SCALPEL system and the expensive challenges that face optical lithography for the 130nm generation of IC manufacturing may introduce commercial viability to SCALPEL.

Another system for e-beam manufacturing, which is still in the proof of concept phase, is the 'multi-beam' system[Electronics weekly, 1998]. Arrays of electron beams individually pattern areas of around  $800 \times 800\text{nm}$  with spot sizes of 40nm. The beam cathode arrays are to be produced on silicon chips with integral control circuitry. Unlike the SCALPEL system, the multi beam system is still in the early stages of development, working with 5x5 cathode arrays with spot imaging only down to 400nm.

## **3.2 Alternative exposure techniques**

### **3.2.1 Optical Lithography**

Optical lithography has been the major lithographic source since the beginning of the semiconductor industry in the 1960s, albeit a natural progression of sources from contact printers, to proximity printing, to scanning projection lithography, and finally to the stepper technology (steppers) used today. Steppers are so called because they expose an image from a 5x enlarged mask onto a wafer substrate, with an ultraviolet light source, then step across the wafer to an adjacent position, align and repeat the pattern exposure, thus reproducing the same pattern many times on a single wafer substrate.

The stepper has developed with the increasing demands for miniaturisation in the semiconductor industry. Each generation of stepper is referred to by the wavelength of the light source that it uses. In recent years the technology has moved from the



436nm (g-line) stepper to 365nm (i-line) to the currently used 248nm 'deep-UV' technology. Industry is looking to 193nm and 157nm technology for progression to the next generations of microchips.

Up to the i-line generation of stepper, the reduction of minimum feature size has been brought about by either a reduction of the exposing wavelength or an increase in the numerical aperture of the lens[Wauters 1998]. However, the complexity of introducing new technology while still maintaining the process latitudes necessary for control over the features critical dimensions, has caused the extension of the technology with resolution enhancement techniques such as optical proximity correction, off-axis illumination and phase shift masks. In the case of the i-line technology, production has been extended to 0.25 $\mu$ m features. Similar requirements are being made of the 248nm deep-UV generation, with industry pushing to extend the technology to produce features of 0.18 $\mu$ m and possibly 0.15 $\mu$ m.

The 1997 SIA roadmap[SIA, 1997] foresees the continued use of optical lithography up to the 0.13 $\mu$ m generation of devices, which has an estimated implementation date around 2003. Beyond this there is no recommendation as a successor for the subsequent generations of lithography, though there is optimism in the possibility of extending optical lithography down to the 0.1 $\mu$ m generation for introduction in 2006.

### **3.2.2 X-ray lithography**

X-ray lithography has been hailed as the successor to replace optical lithography for many years. The 1994 SIA roadmap[SIA, 1994] is quoted as saying 'X-ray lithography holds the most promise for near term success when industry shifts from optical to non-optical lithography'. By 1997 the SIA roadmap[SIA, 1997] was, however, still pushing optical lithography for the next generation of devices and X-ray is still required to provide solutions to fundamental problems in its processing.

The promise of X-ray lithography lies in the high resolution attainable from the use of very short wavelength radiation (4-40Å) and the elimination of many of the



problems associated with optical and e-beam lithography, such as depth of focus and reflection and scattering effects. Resists can be patterned with high aspect ratios, and any organic debris on the mask is effectively transparent to the x-ray radiation.

The fabrication of patterns with X-ray sources involves the use of a thin ( $<11\text{nm}$ ) membrane which is patterned with features of an x-ray absorbing material to produce a mask. The mask is positioned in very close proximity to the substrate being exposed because X-ray radiation can not be focused. The inability to focus the X-rays, like the UV radiation used in optical steppers, means that the mask is required to be of the same scale as the patterns being imaged, referred to as 1:1 printing. There are currently two types of sources of X-rays for lithography purposes:

- Point sources
- Synchrotron storage ring sources

Point sources are the simplest method of producing X-rays for lithography purposes. X-ray tubes involve focusing high energy electrons onto a metal (e.g. palladium) target which emits X-rays [Watts 1989]. The efficiency of this source is low, less than 1%, while the brightness of the source is 2-3 orders of magnitude lower than optical steppers. Laser plasma sources are point sources that have been demonstrated to be sufficiently bright for X-ray exposure, although contamination from the source on the X-ray window is a problem for large scale lithography.

Problems, however, arise with point sources because of the proximity printing of the mask design. Geometric effects arise, shown in figure 3.2, because the source of the X-rays is from a point that is a distance,  $D$ , from the wafer. At the edge of the wafer the X-rays cause a 'shadowing' effect which blurs the patterned image.



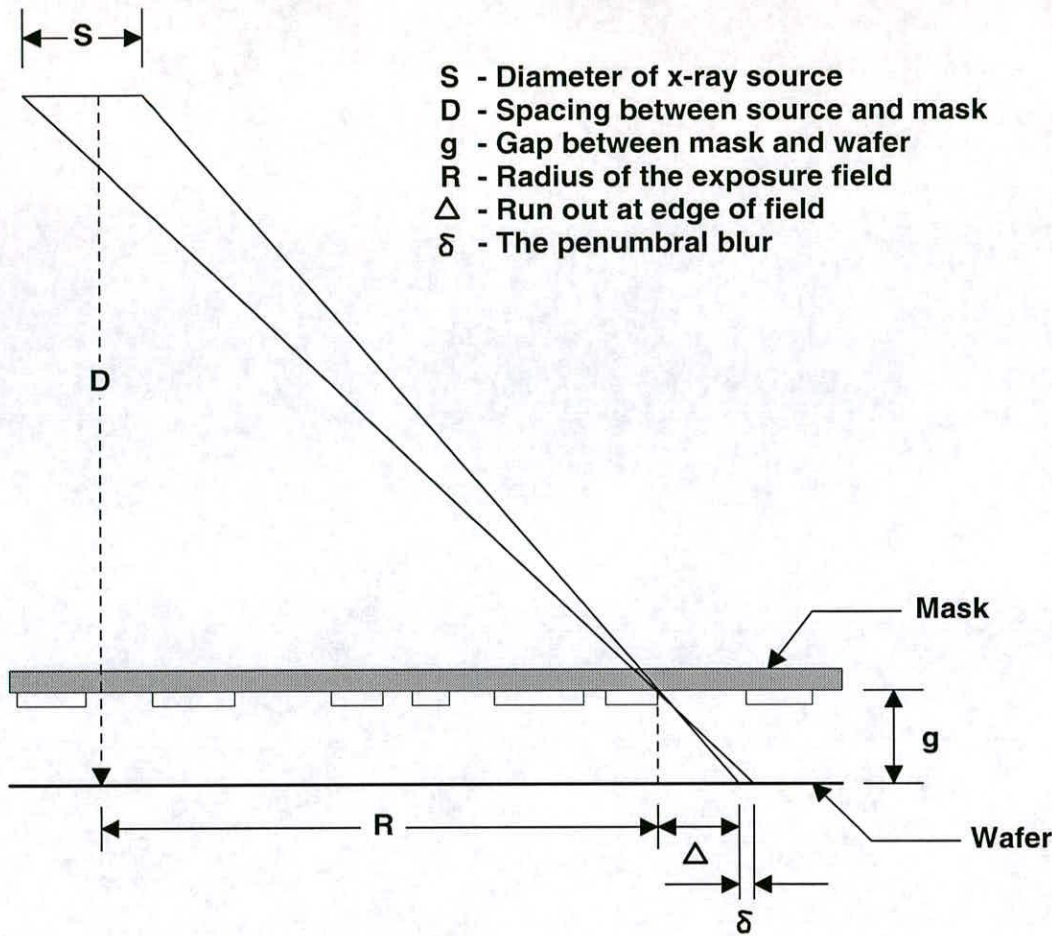


Figure 3.2 X-ray proximity printing[Lepselter 1983]

The ‘run out’ at the edge of the field ,  $\Delta$ , is defined by the equation[Watts 1989]:

$$\Delta = \frac{gR}{D} \tag{3.1}$$

Equation 3.1 shows that the run out error will increase linearly with distance from the centre of the wafer. Adjusting the image positions on the mask can compensate for this error. Problems with this effect occur with the overlay of patterns from different levels of wafer processing. If the mask is aligned at a different height,  $g$ , between levels then there will be an overlay error. This effect will also occur if there is any non-flatness on the wafer surface or in the mask itself. Another limiting geometrical effect is the penumbral blur,  $\delta$ . This results from the nonzero extent of the source, defined by equation 3.2

$$\delta = \frac{gS}{D} \tag{3.2}$$

Synchrotron storage rings almost remove the problem of run-out by collimating the X-rays as they are produced by the source, thus removing the geometric effects. The systems are the choice source for research into manufacturing work with X-rays, as they are also the brightest X-ray sources available. The cost of the systems are, however, prohibitive at up to \$25M per unit.

A large amount of research is being undertaken using synchrotron radiation lithography. The technology is being developed for future generations of devices such as the fabrication by Mitsubishi of a 1Gb DRAM site with 140nm features[Nishioka, 1995] and by IBM of CMOS test circuits with 100nm feature sizes[Wind 1995]. The advanced lithography facility at IBM has been developing the key areas of alignment, mask making and resist technology for x-ray lithography with a synchrotron[Silverman 1997][ Silverman 1998]. The patterning field size of the system is  $50 \times 50 \text{mm}^2$  and achieves a 2nm mean overlay error for the alignment of the lithography fields. The system has patterned features with dimension of 100nm and below, proving its capability of imaging the features required for future generations of devices. However, the systems throughput is relatively slow at 15 wafers per hour and below the approximate target of around 50 wafers per hour for a production system.

The majority of the resources in post optical technology are being put in the area of x-ray lithography. The capability of the techniques resolution is not in doubt. The problems lie with whether a suitable source can be found, with a process that can match the alignment criteria required for the scale of devices that will be produced.

### **3.3 E-Beam exposure principles**

#### **3.3.1 Beam projection system**

The electron optic systems used in e-beam systems are similar to those used in scanning electron microscopes. In fact SEM's are commonly modified for use as e-beam systems. Figure 3.3 illustrates a simplified model of an electron column used in



e-beam systems. An electron source emits electrons that are focused in a beam at the wafer plane by magnetic lenses. The beam shaping aperture, near the gun, limits the excess current flowing in the column by removing the electrons that are not focused into the beam. The beam shaping aperture also governs the numerical aperture of the system. The beam blanking plates operate as a very high speed on-off switch for the beam. When switched off the beam passes through the blanking plates to the wafer plane for imaging. When a charge is placed on the electrostatic blanking plates, the beam is rapidly deflected and strikes a blanking aperture, stopping the beam from imaging the wafer plane.

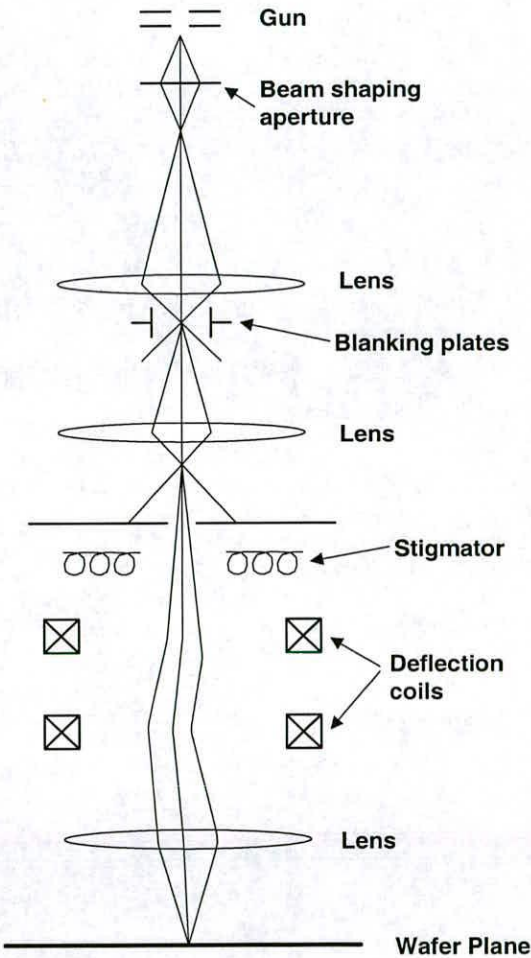


Figure 3.3 Projection optics of an electron column

Deflection coils enable defection of the beam across the wafer plane. The defection allows the beam to write patterns over a small area, usually less than 200×200μm square, which is referred to as an imaging field. Patterns with larger field sizes than

this are often required, and a moving stage with laser interferometer positioning can achieve this in two ways:

- The stage is continuously moved at a constant rate, while the pattern is scanned as the stage moves systematically around the wafer. The wafer position is known, accurately, at any time, which allows for any alignment errors to be made by the positioning of the beam.
- The pattern is imaged in a field and then the stage is moved to an adjacent location and the system prints the another pattern. This motion can be step and repeat, where the same pattern is repeated over the whole wafer, or the exact positioning of the stage by laser interferometry can 'stitch' patterns together to make a larger pattern from smaller fields.

### Electron source

There are two types of sources used in electron columns[Wolf 1986]:

- Thermionic sources
- Field-emission sources

Thermionic sources use a metal that is heated to the elevated temperatures at which electrons are emitted. Materials such as tungsten(W), thoriated tungsten and lanthanum hexaboride ( $\text{LaB}_6$ ) are used. Tungsten sources provide the most stable current, but have a low brightness, around  $1\text{-}3 \times 10^5$  ( $\text{A}/\text{cm}^2$ )/steradian.  $\text{LaB}_6$  sources require high vacuum conditions to achieve stability, but are a brighter source around  $10^6$  ( $\text{A}/\text{cm}^2$ )/steradian.

Field emission sources produce a very high electric field at the tip of a sharp emitter that extracts electrons to form a fine gaussian spot. This is the brightest form of electron source at around  $10^8$  to  $10^9$  ( $\text{A}/\text{cm}^2$ )/steradian. Though very high vacuum conditions are required for stable conditions.

### Beam characteristics

The beam current is related to the numerical aperture ( $\alpha$ ) and the diameter of the spot focused on the substrate ( $d$ ) by the relationship shown in equation 3.3[Watt 1989], where  $\beta$  is the brightness of the source.



$$I = \beta \left( \frac{\pi d^2}{4} \right) (\pi \alpha^2) \quad 3.3$$

The current density in the spot of a round beam source is not uniform, but consists of a bell shaped distribution. This distribution means that the beam diameter,  $d$ , is actually the effective spot diameter. From this equation it can be seen that the current density is directly related to the brightness of the source and the numerical aperture.

The beam current is an important factor in the calculation of exposure times for the patterning of features with e-beam systems. If the beam current is  $I$ , the area of the exposed region is  $A$ , and the charge density to be 'dosed' to the patterned area is  $Q$ , then the relationship for exposure time,  $T$ , is as follows:

$$T = \frac{QA}{I} \quad 3.4$$

From the equation it can be seen that exposure times can be reduced by either increasing the beam current or decreasing the amount of dose required by the resist, i.e. using a more sensitive resist.

### 3.3.2 Resist technology

With the very high resolution attainable from the narrow beam diameters of electron beams, it is accepted that the ultimate resolution of electron beam lithography is from the resolution of the resist and the subsequent fabrication processes[Broers 1996].

A good resist for processing requirements should have the following features[Owen 1985]:

- High sensitivity to the exposing radiation
- Capable of resolving fine features
- After development, the resist should be resistant to the subsequent etching processes that it is subjected to.

### Resist contrast and sensitivity

The resolution of a given resist for a particular set of processing conditions is determined in large part by the resist contrast ( $\gamma$ ) [Moss 1987]. The contrast of a negative resist is related to the rate of the cross-linking network formation for a constant irradiation dose. For positive resists the contrast is related to the rate of the chain scissions and change of solubility at a constant irradiation dose. The value of  $\gamma$  can be calculated from the linear portion of the response curves of a resist. The response curves of typical positive and negative resist processes are shown in figure 3.4. The contrast of a positive resist is expressed in equation 3.5 as:

$$\gamma_p = \left[ \log \left( \frac{D_c}{D_0} \right) \right]^{-1} \quad 3.5$$

where  $D_0$  is the radiation at which the developer begins to dissolve the irradiated film and  $D_c$  is the complete development dose. The contrast of a negative resist is expressed in equation 3.6 as:

$$\gamma_n = \left[ \log \left( \frac{D_g^0}{D_g^i} \right) \right]^{-1} \quad 3.6$$

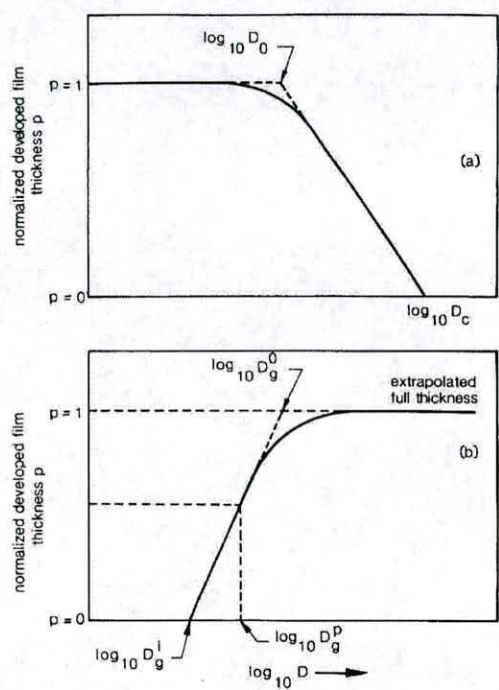
where  $D_g^0$  is the dose required to produce 100% initial film thickness and  $D_g^i$  is the interface gel dose.

Resists that exhibit a high value of contrast minimise the radiation scattering effects from the irradiating source. If a resist had an infinite contrast value the profile of the developed resist would be of vertical sidewalls. Since all exposure techniques result in some of the energy being deposited outside the pattern area, some degree of contrast is inherent.

Sensitivity of a resist is the required incident energy, or dose, that is given to the resist to produce the desired image after development. For positive resist the sensitivity is the dose required ( $D_c$  in figure 3.4a) to effect complete solubility of the exposed region, while the unexposed region remains insoluble. Sensitivity in negative resist is defined as the dose at which a lithographically useful image is formed. The point  $D_g^i$  in figure 3.4b represents the point at which cross-linking of the



resist begins to form, though no useful image will form at this point. Additional dose is required to form an image and this is accepted to be the point  $D_g^{0.5}$ , which is the dose at which 50% of the original film thickness has been retained after development.



**Figure 3.4** Response curves for a) positive resist and b) negative resist in terms of the developed thickness normalised to the initial resist thickness as a function of log (dose) [Moss 1987]

**Electron beam resists**

One of the first widely used e-beam resists is the positive working poly methyl methacrylate (PMMA). This resist is a very high resolution resist, because it does not swell under development. Small features  $<25\text{nm}$  have been demonstrated for this resist[Broers, 1996], although its other properties do not make it attractive for fabrication use. The resist has a low sensitivity ( $\sim 80\mu\text{C}/\text{cm}^2$ ) and very poor resistance to dry etching techniques.

The drive towards commercial resist technologies has developed 'chemical amplification' of the resists[Kudryashov 1996].Chemically amplified resists (CAR's) can be used with exposure by deep-UV optical steppers, x-rays and electron beam radiation. The resist contains a radiation sensitive component that is decomposed under the exposure radiation, producing an acid. When the sample is heated up in the post-exposure bake, after exposure, the acid is activated and cross-linking or scission events occur in the molecules for negative and positive working resists respectively. CAR's exhibit high sensitivity ( $<10\mu\text{C}/\text{cm}^2$ ), high contrast and resolution and good resistance to plasma etching. The advanced chemically amplified positive and negative resists from Hoechst are investigated and characterised for the processing of MOS devices in chapter 6 of the thesis.

### **3.4 Summary**

A background knowledge of electron beam lithography has been presented in this chapter. The information has provided an insight into the development of electron beam technology and how it relates to the microfabrication of silicon devices. The principles of the exposure systems to provide patterning with narrow beam dimensions have been described and the advanced chemically amplified resist technology for defining nano-scale patterns explained. This material will be used in later sections of the thesis, with the description of the electron beam system developed at Edinburgh University for advanced silicon device research.



---

## Edinburgh Electron Beam Lithography System

---

The Edinburgh Electron Beam Lithography System (EEBLS) is a high resolution lithography system, designed and developed as part of this research and is capable of imaging sub 100nm patterns in chemically amplified resists. This advanced lithography capability makes the system ideal for the research of advanced microelectronic devices and structures. The system was built to fully utilise the high resolution capabilities of a Philips XL 40 thermal field emission SEM. Also, the design specification of the systems features, such as wafer alignment, were co-ordinated so that the operation integrated with the processing capabilities of the in-house fabrication facilities. Designing and constructing the system in-house also enables the upgrade of the design to be changed if the performance of a certain area of the design is required to be increased or adjusted. The use of a thermal field emission SEM as the electron source provides a very high brightness beam that allows a small focused spot with a higher beam density than the LaB<sub>6</sub> emitters that are used in standard electron beam lithography systems, this enables a smaller spot size to be used for the exposure of a resist at a given beam current[Kamp 1999].

### 4.1 General Operation

The layout of the e-beam system is shown in figure 4.1. The system has been designed as a series of discrete boards, each providing an individual function. The boards are linked together via two 64-way data buses, this provides the ability to upgrade the system by replacing only the board relating to the specific function. The system is interfaced to the SEM with X and Y scan inputs of analogue voltages that



control the positioning of the electron beam. A beam blank input provides a signal that effectively switches off the electron beam and the picoammeter enable signal engages the system to measure the current of the electron beam with a picoammeter. A computer also interfaces to the system and is used to download the pattern data and control the alignment of different levels of lithography.

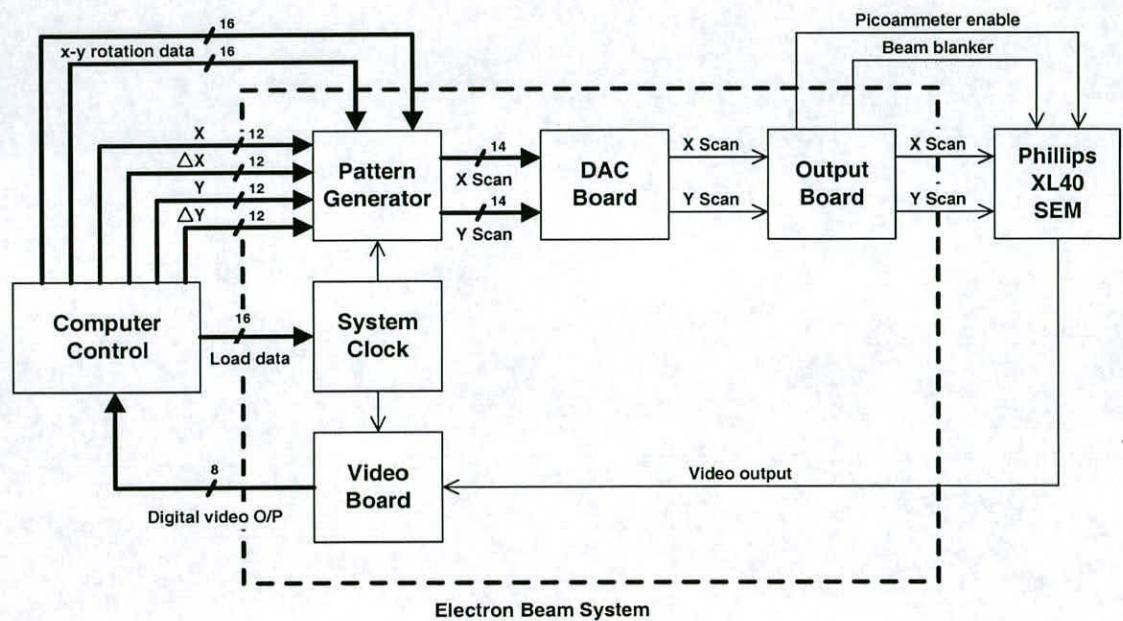


Figure 4.1 General layout of the EEELS

The pattern generator produces the beam position information from a pattern file stored on the computer. The beam is stepped sequentially within a patterning field, as a series of pixels, until the pattern is registered as finished, after which the next pattern is selected for imaging. The pattern field size is presently  $4096 \times 4096$  pixels, as defined by the 12-bit resolution of the pattern input data. The system has, however, been designed to be upgraded to a 14-bit patterning field with  $16384 \times 16384$  pixels for higher resolution. The patterns are exposed as a series of rectangles, which can be linked together to form more complex patterns. The speed at which the data is transferred to the pattern generator is governed by the energy dose given to each pixel in the pattern. A lower exposure dose increases the patterning speed and hence increases the data rate at which the system operates. The speed at which the data increments is governed by the system clock, which is ultimately limited by the



switching speeds of the pattern generator logic chips and the bus bandwidth for data transfer. The maximum designed clock speed of the EEBS is 1MHz.

The digital pattern data is transferred from the pattern generator onto two 12-bit data buses. The data is then read by the Digital to Analogue Conversion (DAC) board, where it is converted to an analogue signal that is used as the analogue beam deflection inputs of the SEM. The pattern data can also be manipulated, at this stage of the processing, to make adjustments for any registration errors in the alignment process. The data manipulation can rotate, skew and stretch the pattern so that it aligns the registration marks.

The output board interfaces the beam deflection voltages to the SEM. Protection is provided to the SEM inputs by limiting the voltage of the output buffers to below the maximum rated voltage. The output board is specifically designed for interfacing the system to the Phillips microscope, the system could be adapted for use with another microscope by adjusting the set-up of the output board. Also located on this board is the circuitry for the beam blanker and the relay to connect the picoammeter, that accurately measures the imaging beam current.

The video board converts the analogue video level signal of the scanned registration marks, from the SEM, into to a digital signal for transfer to the computer. The digital signal is analysed by the computer to detect the centre point of the alignment crosses, from which the transformation data is calculated to align the system for accurate lithography.

The following sections of this chapter provide analysis of the EEBS operating characteristics. The workings of the individual boards are explained and, where relevant, timing diagrams are used to describe their operation. The information presented is intended as a guide to the systems operation and provide a reference as to the capabilities of the designed unit.



4.1.1 System Specification

The specification of the Edinburgh electron beam lithography system is shown in table 4.1.

Edinburgh Electron Beam Lithography System	
Electron Source	Thermal field emission
Accelerating Voltage	30keV
Beam Current	15pA-2nA
Wafer Handling	up to 300mm
Patterning method	Vector Scan
Patterning field size	4096 × 4096 pixels
Field size at 230× magnification	200 × 200µm
Operating frequency	1MHz

Table 4.1      Edinburgh electron beam lithography system specification

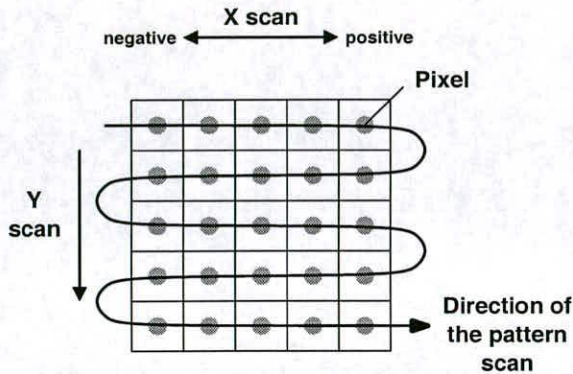
4.2 Pattern Generator Board

The pattern generator board implements the pattern scanning method and the field size. The system was designed to expose with a vector scan method, where the beam is raster scanned across rectangular areas within the patterning field. This method is ideal for the applications for which the system was designed, which are high resolution, low volume, low throughput lithography. Patterns are designed, as rectangles, using standard Cadence[Cadence] software and can be quickly downloaded to the control computer for exposures to commence.

The patterning width of the field is set by the resolution of the input data, which is a 12-bit digital word in both the X and the Y planes. This produces a field with 2<sup>12</sup> (4096) addressable locations, or pixels, in each plane. The field is of variable size depending upon the magnification used with the SEM. At a magnification of 230× the system has a field size of 200×200µm which relates to a pixel pitch of 50nm. The



vector scan method of exposure, which involves individually scanning each pixel and then moving on to the next pixel at an adjacent location, is shown with a 5×5 pixel pattern in figure 4.2. The style of patterns that can be imaged with this scanning method are squares or rectangles.



**Figure 4.2** Vector scanning of a 5x5 pattern

A schematic of the circuitry that operates the pattern generator is shown in figure 4.3. The circuit is based around five sets of counters. 12 bit data is input to four of the five counters, which have the functions described below:

- X      Increments the absolute X co-ordinate of the beam in the scan field
- +ΔX   Counts down the number of pixels in the positive direction of the X scan
- ΔX   Counts down the number of pixels remaining in the negative direction of the X scan
- Y      Increments the absolute Y co-ordinate of the beam in the scan field
- ΔY    Counts down the number of pixels remaining in the negative direction of the Y scan

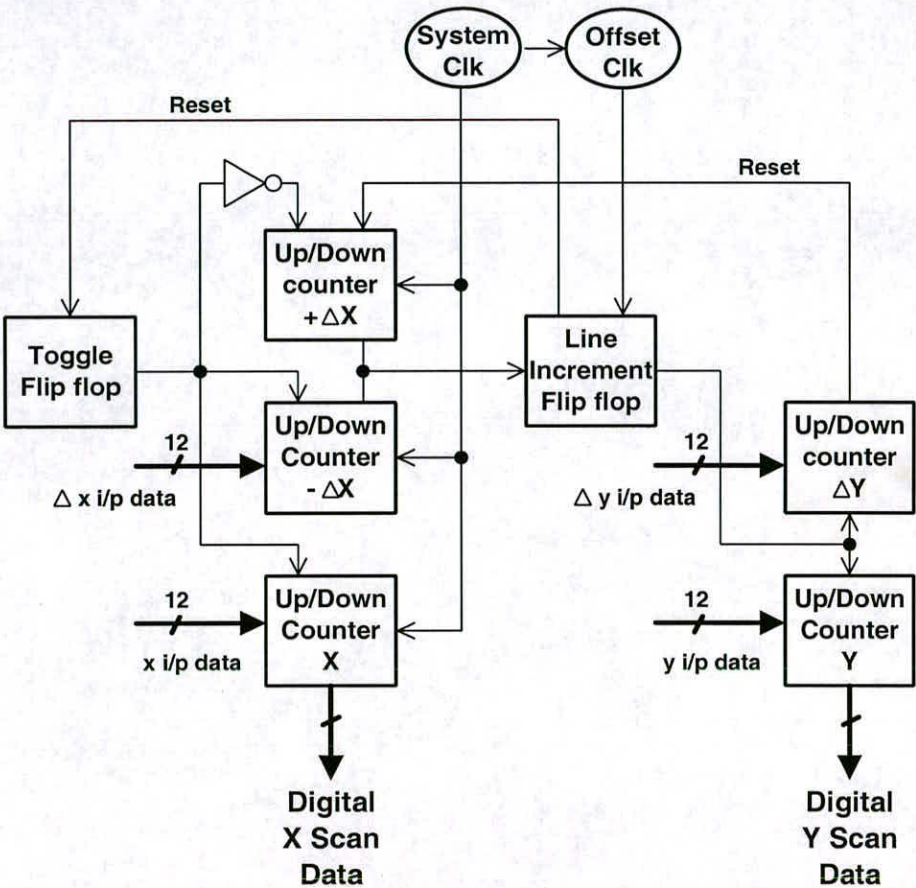
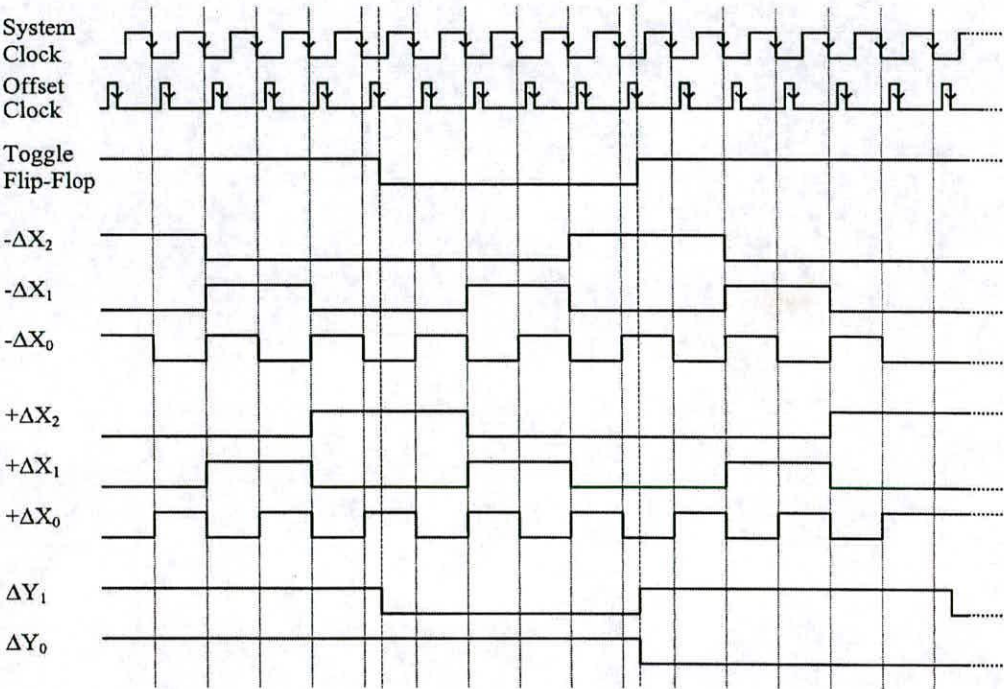


Figure 4.3      Schematic diagram of the pattern generator circuitry

The counters are pre-loaded at the beginning of the scan for each pattern. The X and Y counters are loaded with the data co-ordinates of the start pixel for the pattern in the X and Y axis of the field respectively. The +ΔX and ΔY counters are loaded with the width data that determines the width of the pattern, in terms of pixels, in each axis of the field.



The system operates as illustrated in the timing diagram of figure 4.4. The X counter counts up with each clock pulse, from its loaded value, and the  $+\Delta X$  counter counts down from its loaded number to zero. At the same time the  $-\Delta X$  counter increments up from zero. When the  $+\Delta X$  counter reaches zero the Line Increment Flip-flop is toggled. The Y counter is then incremented one unit (i.e. down one line) and the value of the  $\Delta Y$  counter is incremented down by one, i.e. one line in the pattern scan completed. After this first line is completed the beam is scanned back in the opposite direction with the X counter incrementing down, and the  $-\Delta X$  counter counting down to zero. Again at the end of the line, when the  $-\Delta X$  counter reaches zero, the Y and  $\Delta Y$  counters are incremented.



**Figure 4.4** Timing diagram for a 5x3 (XxY) pattern from the pattern generator Circuit

The toggle flip-flop changes state after each line is finished to change the operation of the three counters for the X scan. If the counter was counting upwards on the previous line its state is changed to counting downwards, and vice-versa if the counter was originally counting downwards.

When the  $\Delta Y$  counter reaches a zero value, the pattern scan is finished. A reset signal is sent to the  $-\Delta X$  counter to reset it ready for the next pattern to be loaded and a 'scan finished' signal is sent to the computer to allow for the next pattern to be downloaded for patterning.

A offset clock signal is used with the line increment flip-flop to place a 300ns delay, from the system clock signal, in the toggling of the flip-flop from the  $\Delta X$  counters output. This is so the values of the counters have had time to settle before any pulse is sent to reset them.

### 4.3 Clock circuits

The clock circuits provide timing signals to synchronise the data transfer of the pattern information around the EEBS system. The main system clock operates at a maximum clock frequency of 1MHz. The two secondary 'Offset' and 'Delay' clocks use the 'system clock' as an input to produce their output pulses.

#### 4.3.1 System Clock

The system clock produces an adjustable clock rate for the data transfer within the e-beam system. The period of the system clock frequency corresponds to the dwell time that the beam exposes each individual pixel of the patterns. Adjusting the frequency of the system clock changes the period for which the beam dwells over each pixel and hence the dose of energy given to the pixel. The dwell time period is calculated as a minimum dwell time for all the patterns in the exposure field, and any increase from that minimum dwell period can be implemented with a multiplication factor for individual patterns. The equation used to calculate the minimum dwell time of the exposure is shown in equation 4.1.

$$\text{min dwell time} = \frac{\text{area of pixel} \times \text{base dose}}{\text{beam current}} \quad 4.1$$

The schematic diagram of the system clock is shown in figure 4.5. The basic operation of the clock involves dividing down a 40MHz input and comparing the divided signal with that of a pre-set value loaded from the control computer. When



the values correspond, the toggle flip-flop is switched and the counters are simultaneously reset to start counting the second half period of the system clock pulse

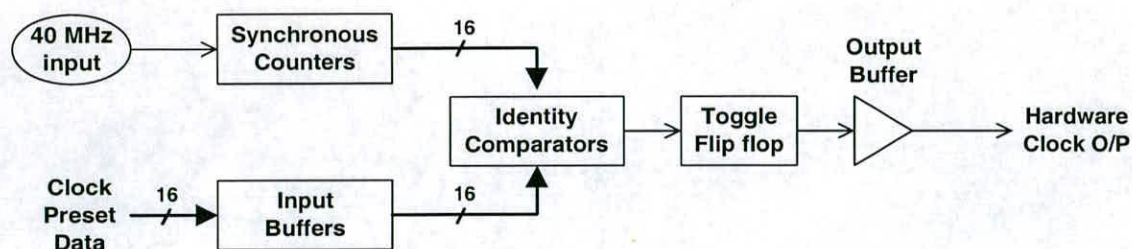


Figure 4.5 Schematic diagram of the system clock

The timing diagram for the system clock is shown in figure 4.6

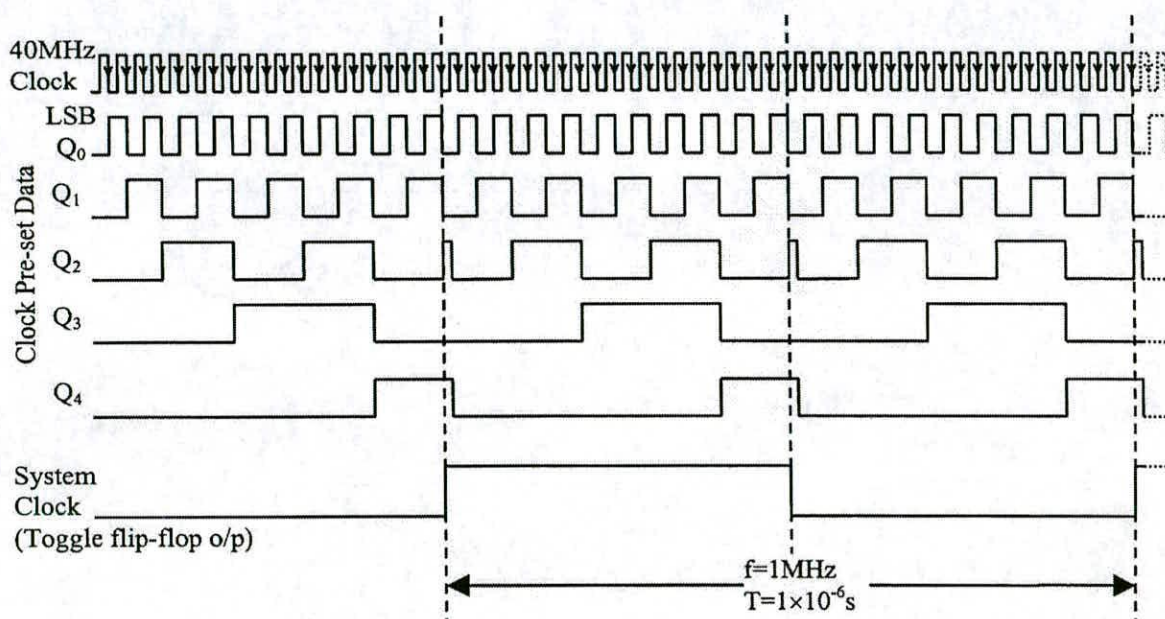


Figure 4.6 Timing diagram for 1MHz operation of the system clock.

The 40MHz clock signal is input into the 16 stage synchronous counters. The counters allow for a maximum division of  $2^{16}$  from the input signal. This corresponds to a programmable clock range down to 610Hz. The counter outputs are then used as one half of the inputs to 16-bit identity comparators. The other half of the comparator inputs are set to a 16-bit number written from the computer, through a set of isolating buffers. The pre-set 16-bit number corresponds to the number of divisions the 40MHz clock input is to undergo, set by equation 4.2 below.

$$x = \frac{40 \times 10^6}{2f} \quad 4.2$$

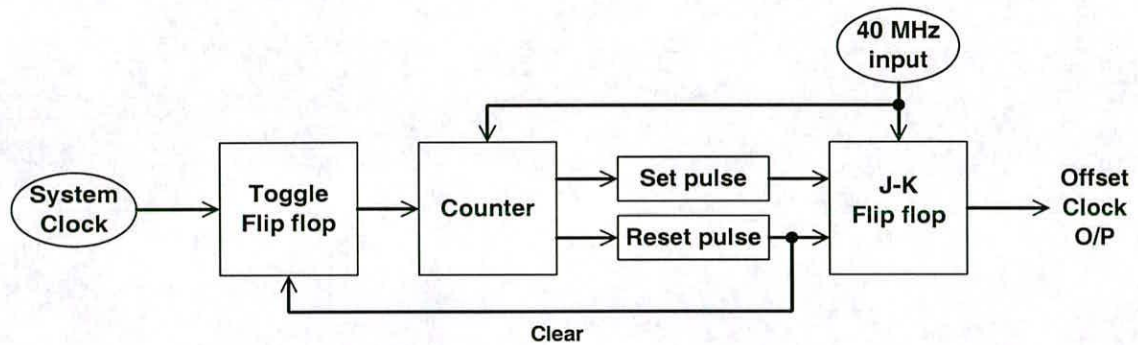
x - pre-set data (decimal)

f - required clock frequency (Hz)

When the output from the synchronous counters match the 16-bit number, a circuit simultaneously switches the state of the toggle flip-flop and resets the synchronous counters to repeat the process. With the Toggle switching state and the counter repeating the same pre-set count, a clock pulse of equal positive to negative transitions takes place, as shown in the timing diagram of figure 4.6.

### 4.3.2 Offset clock

The signal from the offset clock is used on the pattern generator board to produce a reset pulse for the line increment flip-flop. The pulse has a 300ns delay from the falling edge of the system clock, to allow the X-scan counters time to settle before their counting operation is reversed with the offset clock pulse to the toggle flip-flop, see figures 4.3 and 4.4. The circuit layout of the offset clock is shown in figure 4.7



**Figure 4.7** Schematic diagram of the offset clock

The system clock is the initial input to the offset clock, which is used to toggle a flip-flop. This flip-flop in turn, releases the clear function of a 4-bit synchronous counter that counts the pulses from a 40MHz clock input. Set Pulse and Reset Pulse circuits count 12 and 14 pulses respectively and are applied to the J and K inputs of the J-K Flip-flop. The timing diagram of the offset clock is shown in figure 4.8 for a 1MHz system clock input.



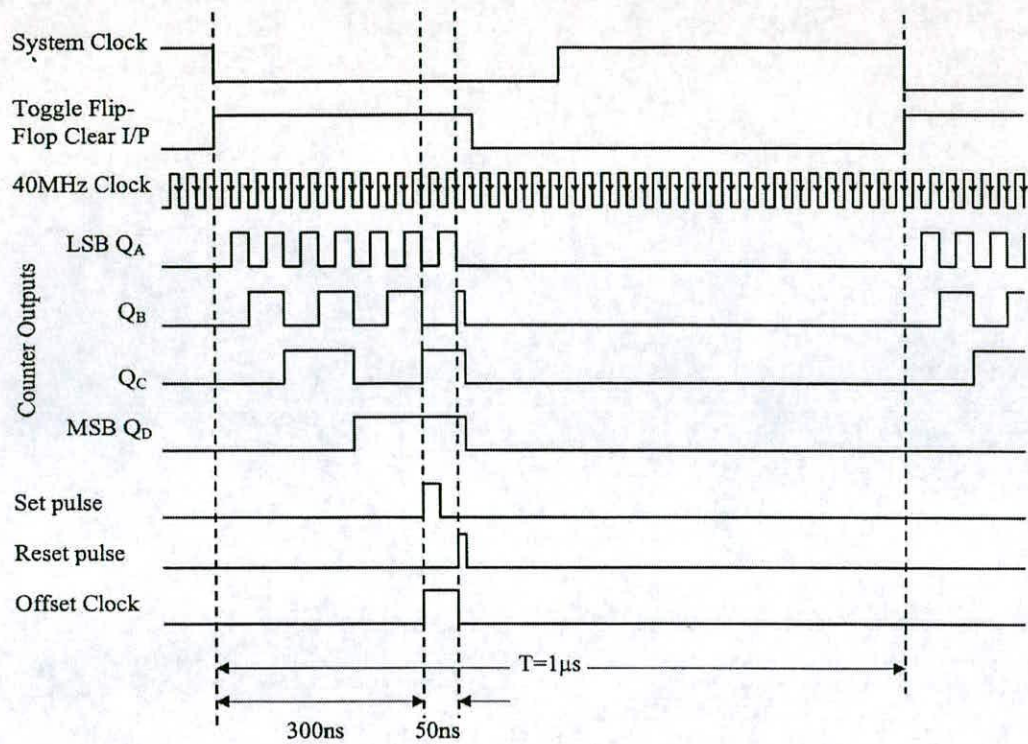


Figure 4.8 Timing diagram of the offset clock with a 1MHz system clock frequency

4.3.3 Delay Clock

The delay clock produces a zero level pulse that resets the integrator circuit on the video board, explained in section 4.5. The schematic circuit for its operation is shown in figure 4.9.

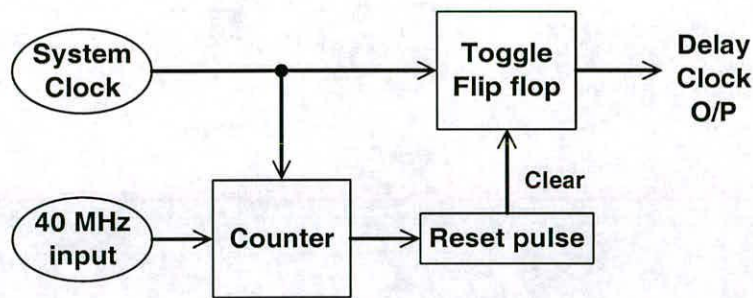
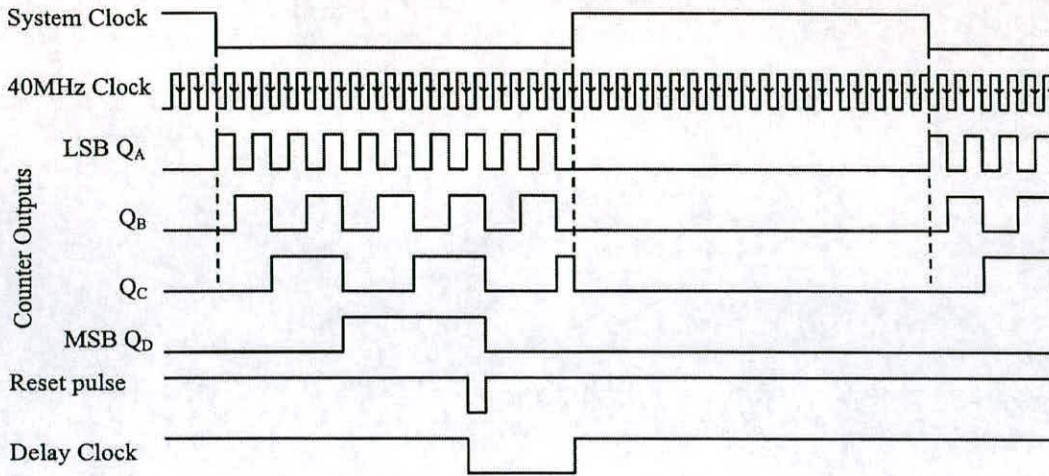


Figure 4.9 Block diagram of the delay clock circuitry

The counter starts counting with the low going transition of the system clock. Fifteen pulses from the 40MHz clock are counted before a reset pulse is input to the flip-flop which produces the output of the delay clock. The timing diagram for the delay clock is shown in figure 4.10.



**Figure 4.10** Timing diagram of the delay clock

## 4.4 Digital to Analogue Converter Board

The DAC board produces the analogue X and Y, line and field, waveforms that provide the scan inputs to the SEM. The combination of inputs to the DAC board can be combined to stretch, skew and rotate the pattern information that is input from the pattern generator board. This feature to the system produces an accurate and flexible way to manipulate the patterns for close tolerance alignment between patterning levels. The alignment of the system is designed to be within one pixel.

The DAC board uses a 14-bit digital input of the beam position data from the pattern generator and converts it to an analogue signal that can be used as a beam deflection input to the SEM. The board was constructed with 14-bit architecture to enable its use when the system is upgraded with a 14-bit resolution pattern generator board. With the current 12-bit resolution the two most significant bits of the data are set to zero on the DAC board, thus disabling the inputs, while the 12-bit data is sent to the remaining inputs.

The beam position data of the X-channel and Y-channel, that control the beam deflection coils of the SEM, is generated by the DAC board using a transformation



algorithm on the input data. The algorithm used is of the form of a transformation matrix of the input data, the basic equation of this translation is shown in equation 4.3

$$\begin{pmatrix} X \\ Y \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} x \\ y \end{pmatrix} \quad 4.3$$

x - X scan beam position  
data

y - Y scan beam position  
data

X - X channel translated  
data

Y - Y channel translated  
data

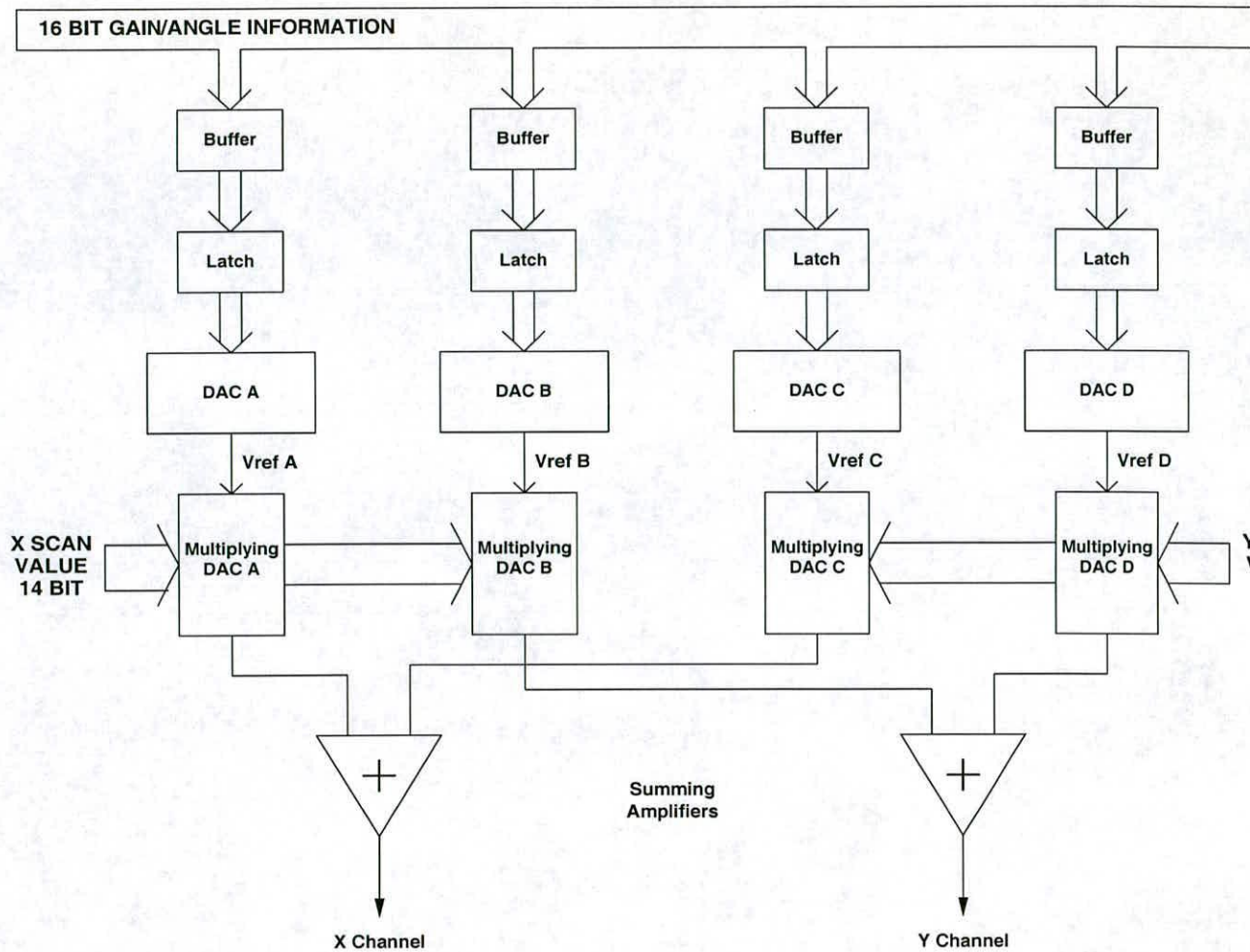
A, B, C, D - transformation  
variables

The matrix expands to produce equations for the output of each channel of the beam deflection, shown in equations 4.4 and 4.5.

$$X = Ax + By \quad 4.4$$

$$Y = Cx + Dy \quad 4.5$$

The circuit that implements the translation of the input data is shown in figure 4.11.

**DAC BOARD - SCHEMATIC DIAGRAM**

**Figure 4.11** Layout of the DAC board circuitry

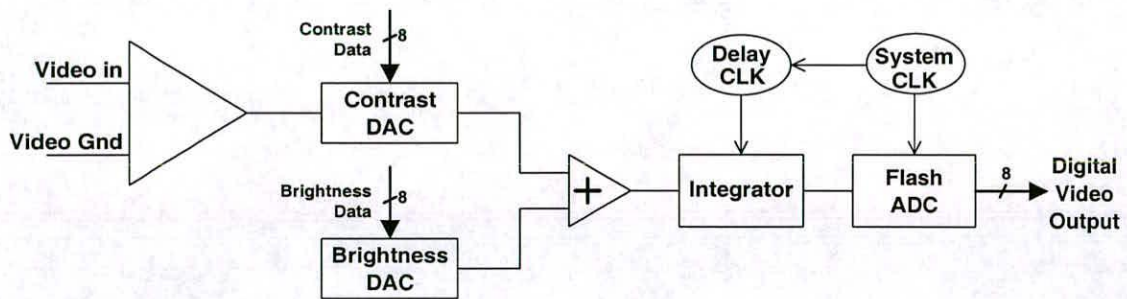
The x and y beam position data, from the pattern generator board, is input into two multiplying DACs, where the digital information is multiplied with the analogue translation data. The translation data is produced individually in four DACs, with the data values calculated by the control computer and downloaded to the DACs through sets of buffers and latches, which load and hold the data onto the DACs from the data bus. The digital data from the computer is transformed to an analogue signal in DACs A-D. The data values from the multiplying DACs are added together in two summing circuits to produce the analogue X and Y channel beam signal for relaying to the SEM inputs. The layout of the DAC board circuitry implements the operation of the equations 4.4 and 4.5.



## 4.5 Video Board

The video board changes the video signal from the analogue SEM output to a digital signal which is input to the computer. Imaging of the alignment crosses allows fully automated and manual alignment of patterns. The video scan images the alignment crosses at the edge of the patterning field, this scan is adjusted to a high contrast image that highlights the alignment crosses against the surface material. The edge of the cross is subsequently detected by image processing techniques in the control computer and the centre point of the cross is located. With the locations of three of the alignment crosses detected the transformation data to be input to the DAC board is calculated and the image is readjusted for accurate alignment.

The schematic diagram for the video board is shown in figure 4.12. The video signal is initially input to an instrumentation amplifier to keep the Ground references of the SEM and the EEELS isolated. The Brightness and Contrast DACs then manipulate the basic video signal by adjusting the voltage level or gain respectively. The signal is adjusted by a programmable 8-bit number, that produces 256 level shifts, from the computer. The contrast adjusted signal is then summed with the voltage level produced with the Brightness DAC.



**Figure 4.12** video board schematic diagram

The level adjusted signal is subsequently input to an integrator circuit. This circuit averages the input video signal over a period, this reduces any noise on the signal before being sampled by an 8-bit flash video A/D converter. The capacitor of the integrator circuit is reset after each sample from the A/D converter by a pulse from

the Delay clock, explained previously in section 4.3.3. The period integration is determined by the frequency of the system clock. Integration of the video signal starts with the rising edge of the system clock signal and the sample is taken on the falling edge of the system clock, thus the period of integration is half of the system clock period. The clock is operated at 1Mhz for video signal sampling, thus the integration period is 500ns.

## 4.6 Output Board.

The output board contains the circuitry for interfacing the EEELS outputs to the SEM. Contained on this board are the output buffer circuit, Beam Blanking circuit and the Picoammeter Relay Control circuit.

### 4.6.1 Output Buffers

The output buffers interface to the SEM and provide the line and field, X and Y, scan for the beam deflectors. Two identical sets of circuits buffer the output for each of the line and field scans, one half of the output buffer circuit is shown in figure 4.13. The reduced power supply to the two buffers provide protection to the inputs of the SEM by limiting the voltage range to within the maximum value specified for the SEM inputs. The 711 op-amp is high speed and working as a unity gain buffer. The BUF634 is a high current output, high-speed buffer. High current drive is necessary to source the low impedance input to the SEM.

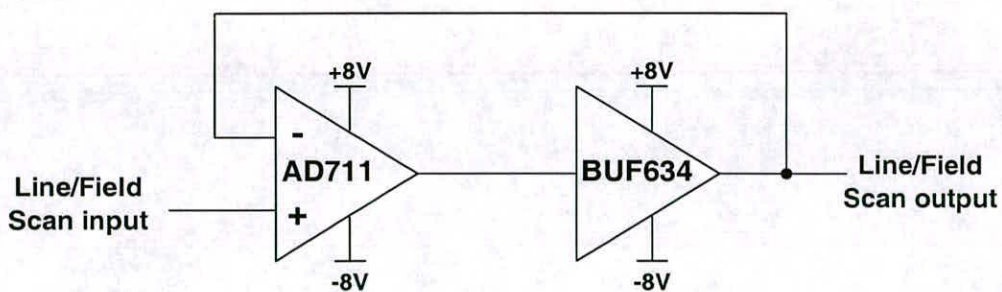


Figure 4.13 output buffer circuit



### 4.6.2 Beam Blanking circuit

The beam blaster circuit applies a voltage to the beam deflection plates of the electron column in the SEM. When the voltage is applied, the beam is electrostatically deflected away from the wafer plane at high speed. With the beam deflected away from substrate that is being exposed, the beam is repositioned to another area of the exposure field ready for imaging the next pattern. Once set-up at the next location the beam blanking voltage is removed and the beam is again controlled by the deflection coils of the SEM. The schematic layout of the beam blanking circuitry is shown in figure 4.14.

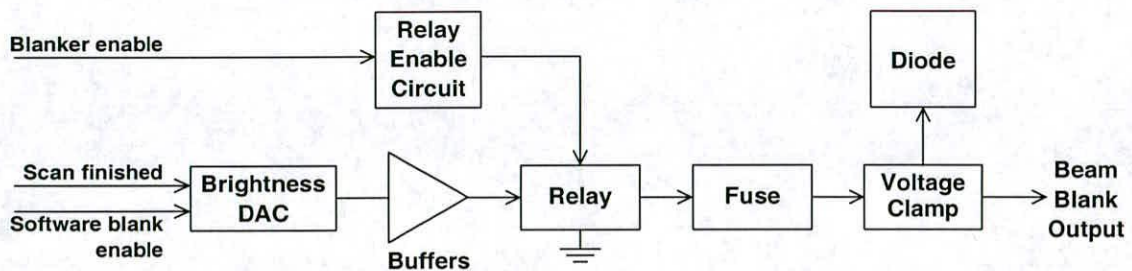


Figure 4.14 Schematic diagram of the beam blanker circuitry

The beam blanking circuitry is energised with one of three inputs:

- The 'blanker enable' input operates the relay that physically isolates the blanker circuitry from operation. When this input is high the relay is switched off, thus deactivating the relay by directly connecting the blanking plates to the ground plane, reducing any noise effects that would interfere with the exposing beam and reduce its resolution. A low input switches the relay over to blanking operation and the blanker is then controlled from the output of the buffer circuit.
- 'software blank enable' is an input that is addressable from the computer to blank the beam without switching the relay off.
- 'scan finished' is the low signal produced by the pattern generator board to register that the current pattern has finished scanning and the beam is to be blanked before scanning the next pattern.

The selector circuit is a logic circuit that produces a high output when both of the inputs are low. The circuit activates a transistor that grounds the output when switched off. The buffer circuit used is the same as for the output buffers, shown in figure 4.13. The circuits high output current drives the beam blanker input to the SEM when switched on. The fuse and voltage clamp protect the SEM by restricting the maximum current and voltage from any overload from a short circuit. The diode provides a visual indication of the beam blanker circuit's status on the front panel of the EEELS unit, the diode is illuminated when the circuit is blanking the beam.

4.6.3 Picoammeter Relay Control

The picoammeter circuit switches the state of the relay that isolates the beam current measurement output from the SEM to the picoammeter. The circuit is shown in figure 4.15. When the 'picoammeter relay enable' input is low, the input to the transistor is pulled high through the 1kΩ resistor. The transistor is switched on producing a high output and energising the relay, this opens the connection for the input to the picoammeter that enables the current to be read for the beam current measurement. The output is also used as the 'relay sense' input on the backplane of the EEELS system.

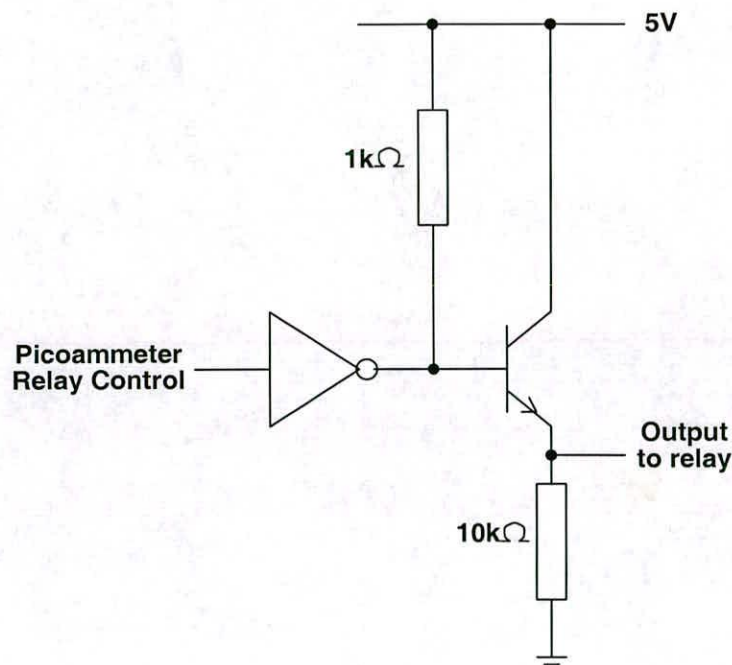
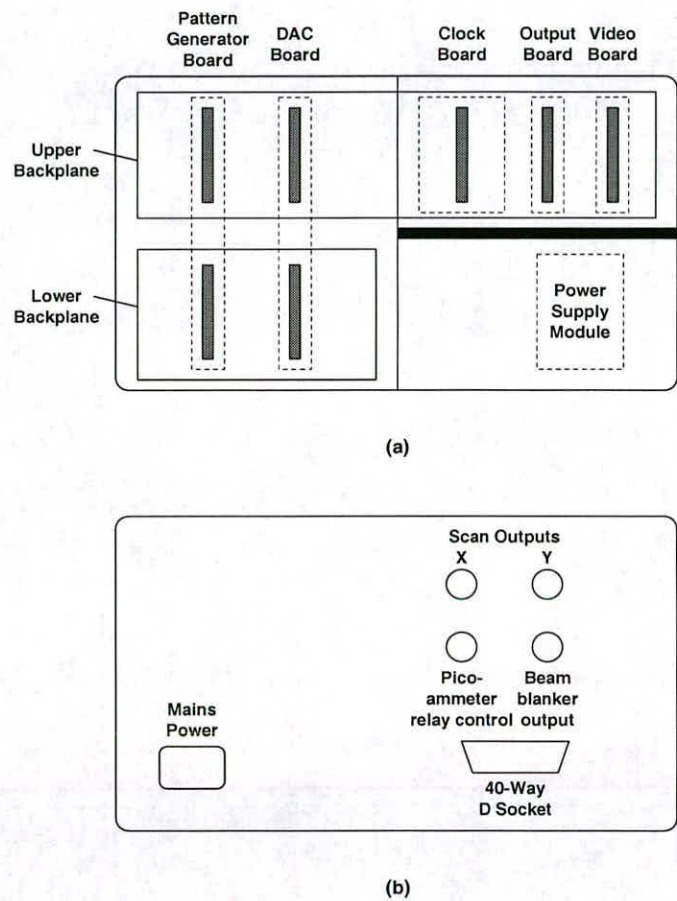


Figure 4.15 Picoammeter Relay Control circuit



4.7 System Layout

The lithography system is housed in a two level (6u) standard 19 inch sub-rack system. This construction enables the use of removable eurocard boards that connect to two 64-way backplane data-buses. The system layout in the rack is shown in figure 4.16. The backplanes are laid out in the upper and lower halves of the rack. The upper data bus is connected to the control computer and carries the data signals to and from the computer to operate the lithography system. The lower backplane carries the X and Y scan data that is produced by the pattern generator board before it is used as an input to the DAC board.



**Figure 4.16** Electron beam lithography system layout, (a) Board layout viewed from the front of the system and (b) Input/output connections viewed from the back of the system.

The connections are laid out at the rear of the system with the connections for the scan outputs, pico-ammeter relay control and beam blanker output made directly to their respective inputs on the SEM and the pico-ammeter. The 40-way D socket is

connected to the control computer and a mains socket provides the power connection to the unit.

The connections to the 64-way data buses are laid out as shown in figure 4.17. The lower backplane has power supply connections for the boards with analogue circuitry and 28 pins are allocated for the two 14-bit data buses of the X and Y scan data. The upper backplane has power supply connections for the boards with digital circuitry. The 48 connections in the middle of the backplane are allocated as connections to the I/O card of the computer, all of the programmable data to the boards is sent through these connections. The delay, offset and programmable clock are connected to the bus to provide other boards in the system access to the signals.

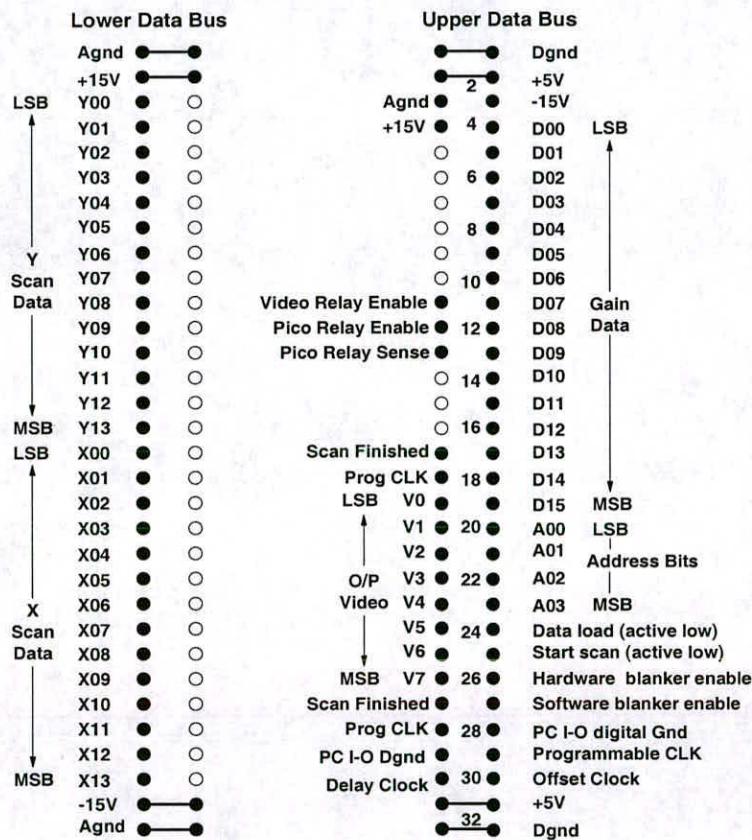


Figure 4.17      Layout of the connections to the upper and lower data buses



## **4.8 Summary**

The specification and operating parameters of the EEBS have been presented in this chapter. The system design enabling high resolution electron beam lithography has been demonstrated, with the vector scan patterning of the pattern generator board. Techniques to set up accurate automated alignment of patterning levels have been highlighted with the use of a video scan and image recognition process on alignment marks. The modular design of the system has been highlighted to allow upgrades to be made to the specification without complex re-working of the whole design. The design of the output board, that provides an interface connection to the SEM, means the EEBS can be interfaced to different SEM units with only the re-design of the output board necessary.

# Device Fabrication Layout

With the electron beam lithography system operational for lithography work, an experiment was designed for the fabrication of nano scale MOSFET devices with dimensions to 100nm and below. This chapter describes the design of the experiment, followed by a discussion of the layout of the lithography masks and pattern layouts and the structure of the MOS devices. Also included is a review of the processing techniques to be utilised in the fabrication of the devices.

## 5.1 Design

The design of the device integration experiment was centred on the fabrication of MOSFET devices with all critical lithography levels of the device processing performed with electron beam lithography. Optical lithography was only used to define the large scale features.

	E-beam lithography	Optical lithography
1		Frame and alignment marks
2	Active areas	
3	Gate electrodes	
4	Contact holes	
5	Metal (inner e-beam area)	
6		Metal (probe pads)

Patterns for the lithography levels were designed using Cadence software. The patterns were built up from a series of square and rectangular blocks, to correspond to the file formats of the electron beam lithography system and the pattern generator system, which produces masks for the optical lithography steppers. The Cadence files

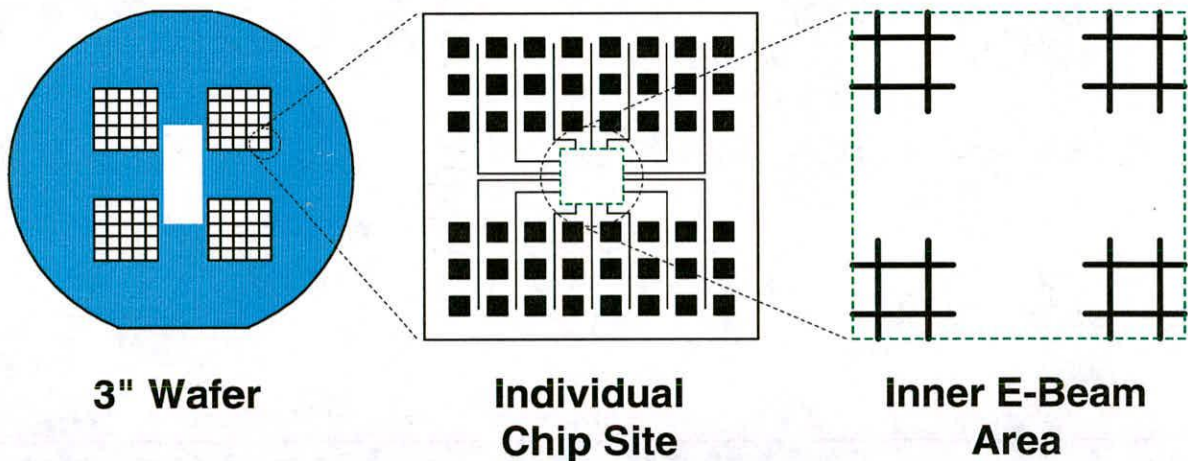


were output in the “.cif” format from which the files could be converted into the necessary format using software.

The devices were processed on n-type and p-type 75mm Si wafers. All of the processing stages were performed within the Edinburgh Microfabrication Facility (EMF).

## 5.2 Pattern Layout

The different levels of patterning for the design are shown in figure 5.1. At the highest level the wafer was patterned with four 5x5 arrays of chip sites. It was within each of these chip sites that the lithography was performed. The chip sites contained an inner e-beam area, within which the electron beam lithography was performed. The multiple pattern levels for the e-beam lithography were aligned using the crosses at the edge of the field within the inner e-beam cell.

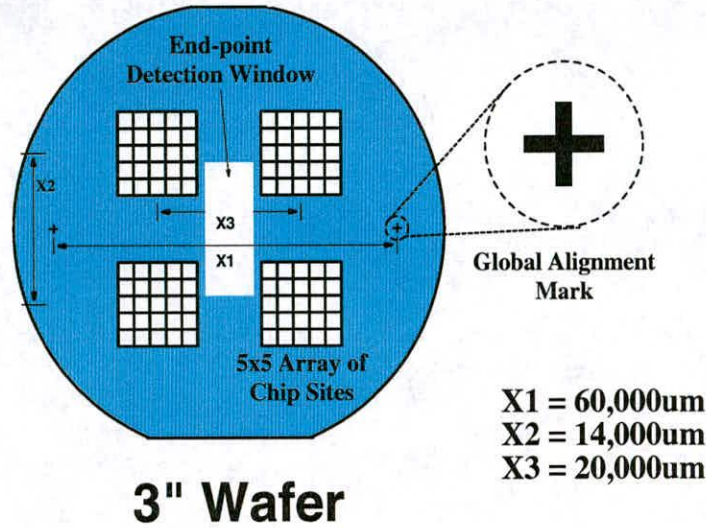


**Figure 5.1** Levels of lithography patterning for the device experiment

### 5.2.1 Wafer layout

The initial patterning on the 75mm wafers was performed with optical lithography. Global alignment marks were patterned onto the wafer to provide a calibrated reference point for an initial alignment of the e-beam system. A two point alignment from these global marks allowed the e-beam system to step to any chip site window,

as the arrays were patterned a known distance from the global marks. The layout of the patterns and the chip site patterning distances from the global marks is shown in figure 5.2. The chip sites were patterned in four individual arrays to allow space for an endpoint detection window to be located in the centre of the wafer. This is because the laser from the end point detection system is aimed at the centre of a 75mm wafer in the oxide and polysilicon dry etch systems (The end-point detection system was built specifically for this project and is described in section 5.4.3



**Figure 5.2** Pattern layout on the 3" wafer

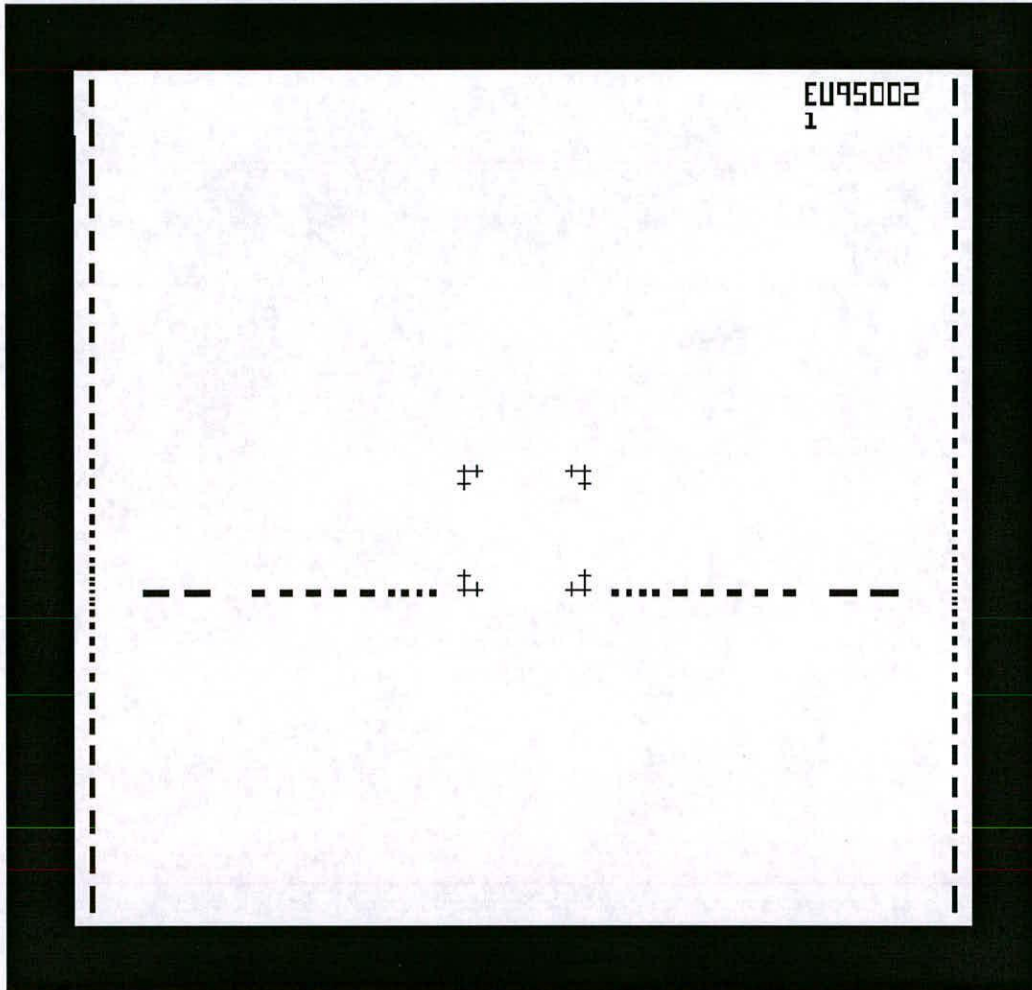
### 5.2.2 Chip Site Patterning

The patterning of chip sites with optical lithography occurs with two different levels of processing. The initial pattern is a frame level that defines the area that will contain the electron beam defined patterns. A hybrid optical/e-beam lithography step is performed near the end of the processing to define the probe pads, which are metal pads used for electrical analysis of the fabricated MOS devices.



### Frame level lithography

The pattern defined for the frame level is shown in figure 5.3. The pattern defines the e-beam alignment marks on the Si wafer. The alignment marks provide a calibrated reference point for alignment of the e-beam lithography levels. The frame around the border of the pattern gives a visible feature around each site which allows easy recognition of the individual chip sites when inspecting the wafer with optical or scanning electron microscopy.

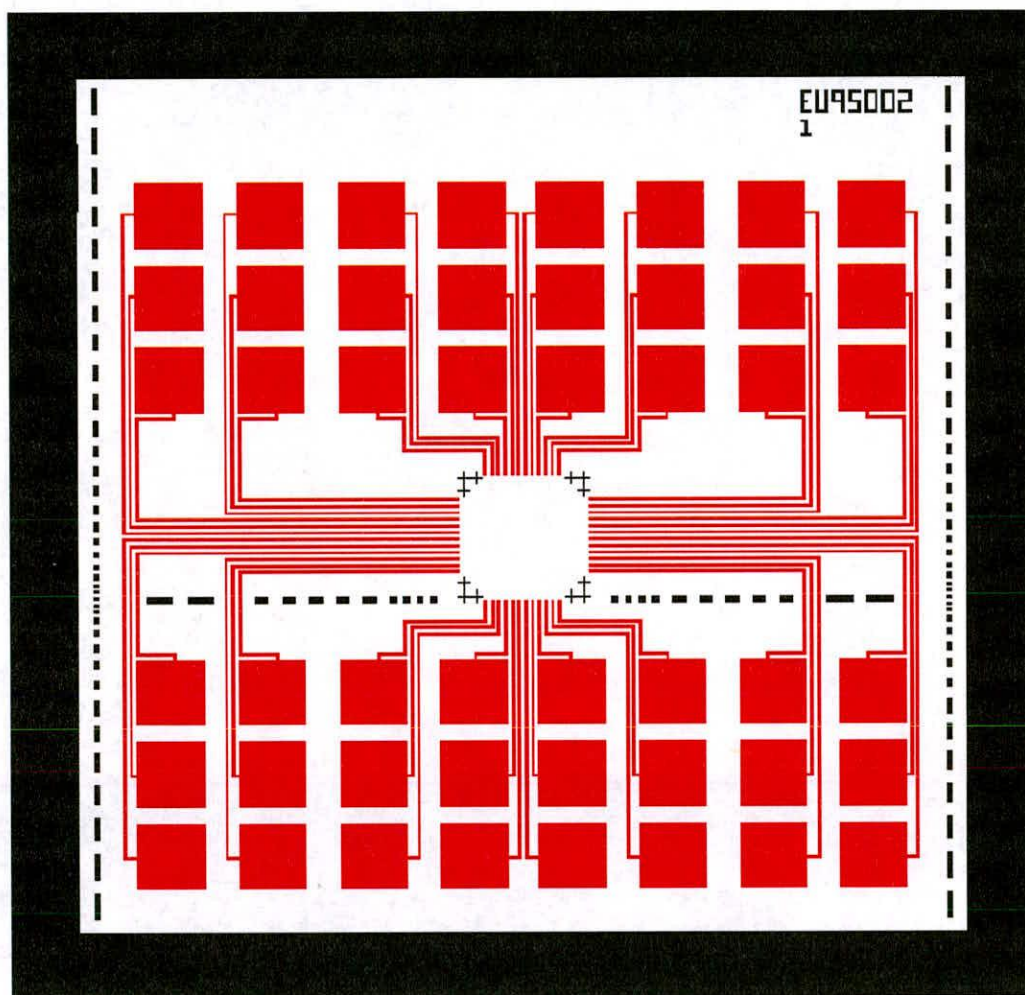


**Figure 5.3**      **Optical mask for the frame level of lithography**

The patterns from this mask are transferred from the photoresist image into the substrate of the Si wafer by etching the Si with a dry etch process.

### Metal level lithography

The optical metal level was designed to interface with the electron beam defined metal patterns within the inner e-beam cell. Optical lithography was used for this process because of the large feature sizes ( $80\mu\text{m}$  probe pads) of the defined patterns. The hybrid patterning technique allowed high resolution patterning of the metal within the inner e-beam cell area and fast patterning of the large low resolution patterns for the outer probe pad area. The metal level mask is shown in figure 5.4. The previously defined frame level is also shown in the diagram to highlight how the two masks overlay.



**Figure 5.4**      **Optical mask for the metal level of lithography**



### 5.2.3 Inner e-beam area device layout

Two designs were produced for patterning devices within the experiment. The two sets of patterns contained arrays of sixteen transistors with a matrix of different gate lengths and contact window widths, these patterns are referred to as *Design0* and *Design1*.

The complete layout of the e-beam lithography patterns within the inner e-beam area are shown in figure 5.5. The transistors are arranged in sets of four within the area with the gate electrodes running horizontally. The series of boxes located in the top right hand corner of the area display the overlay control of the lithography alignment process. Each lithography level patterns a box centrally upon the box laid down by the previous level of lithography, the degree of box misalignment indicates the overlay error of the process. All of the e-beam masks for the processing are overlaid from the array *Design1* for figure 5.5.

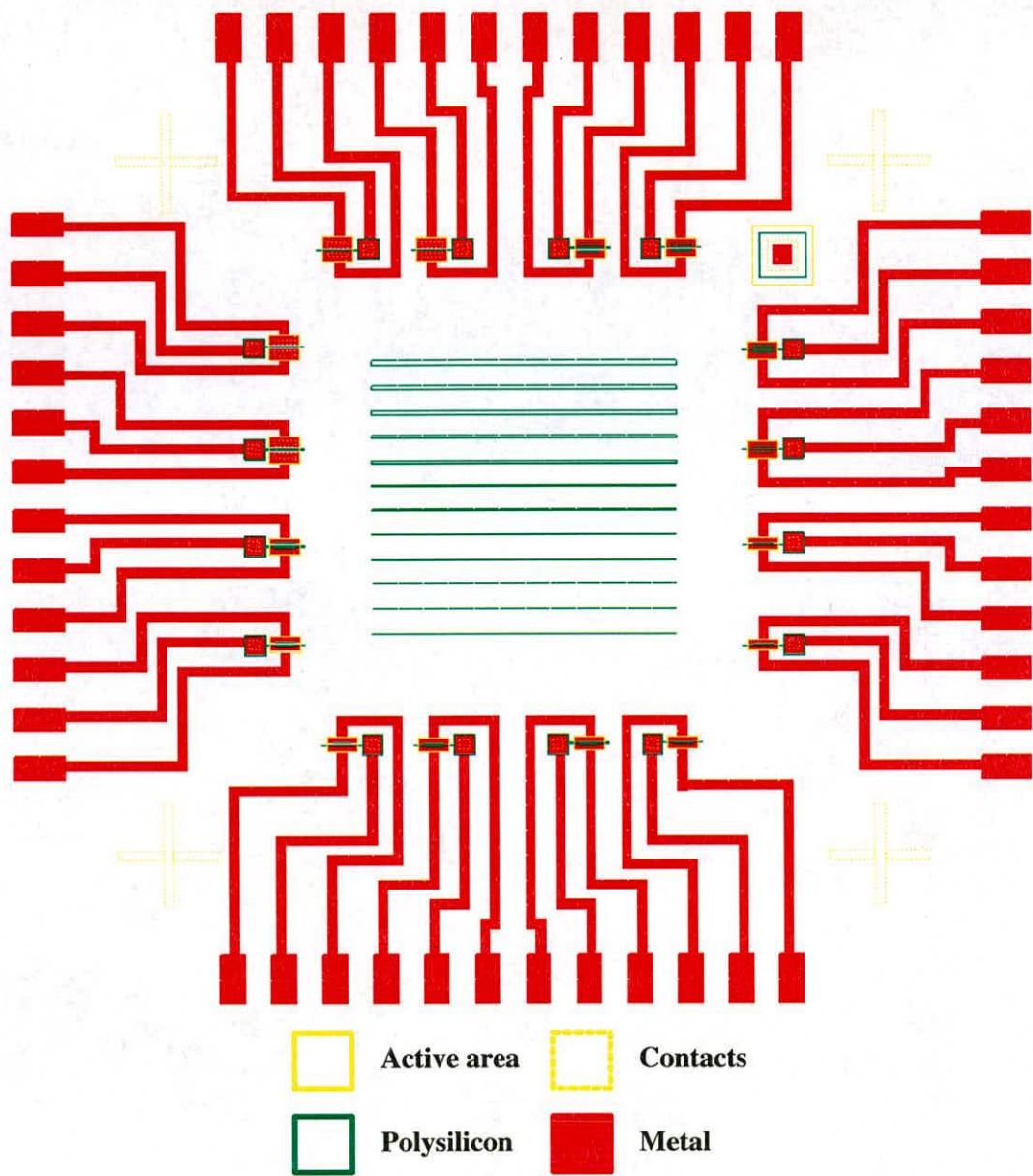


Figure 5.5      Electron beam lithography patterns for the inner e-beam area



Layout of patterns for *Design0* transistor array

The features of the pattern *Design0* range from 1μm-0.25μm for the gate lengths and 4μm-0.5μm for the contact widths. The transistors are arranged within the inner area as shown in figure 5.6 and the key to the design dimensions of the transistors are shown in table 5.1.

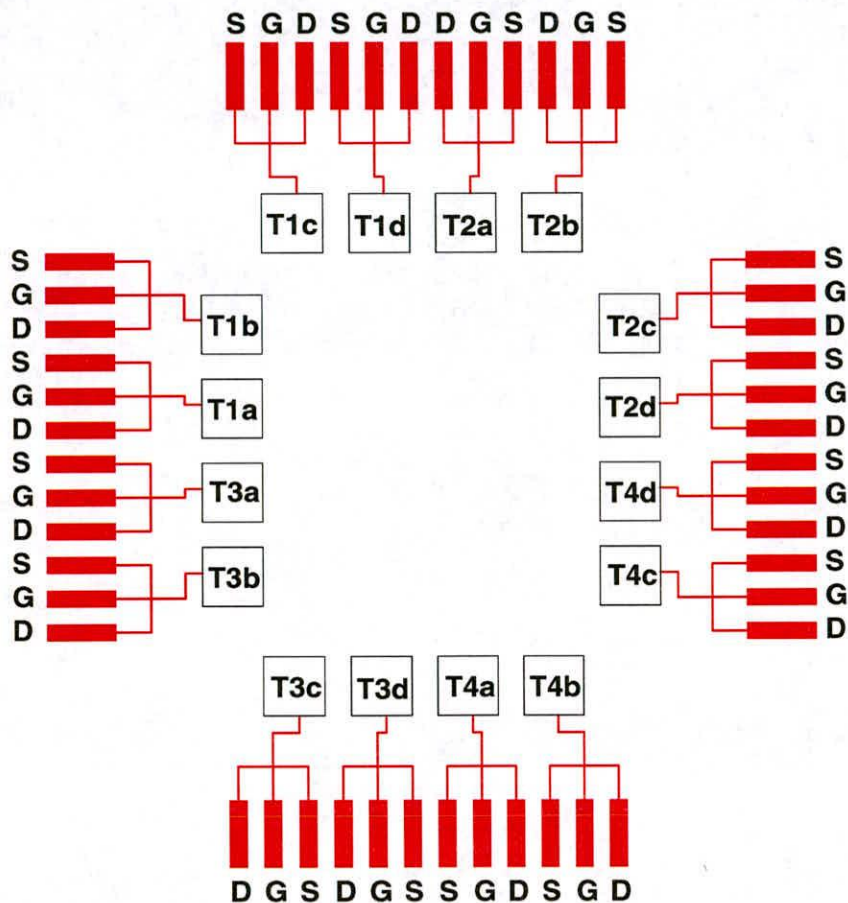


Figure 5.6      Layout of the transistors in the pattern *Design0*

Contact Length		Gate Length	
T1	4μm	a	1μm
T2	2μm	b	0.75μm
T3	1μm	c	0.5μm
T4	0.5μm	d	0.25μm

Table 5-1      Key of transistor gate and contact dimensions for pattern *Design0*

Layout of patterns for *Design1* transistor array

The features for the pattern *Design1* range from 0.5μm-0.05μm for the gate lengths and 1μm-0.1μm for the contact widths. The transistors are arranged within the inner area as shown in figure 5.7 and the key to the design dimensions of the transistors are shown in table 5.2.

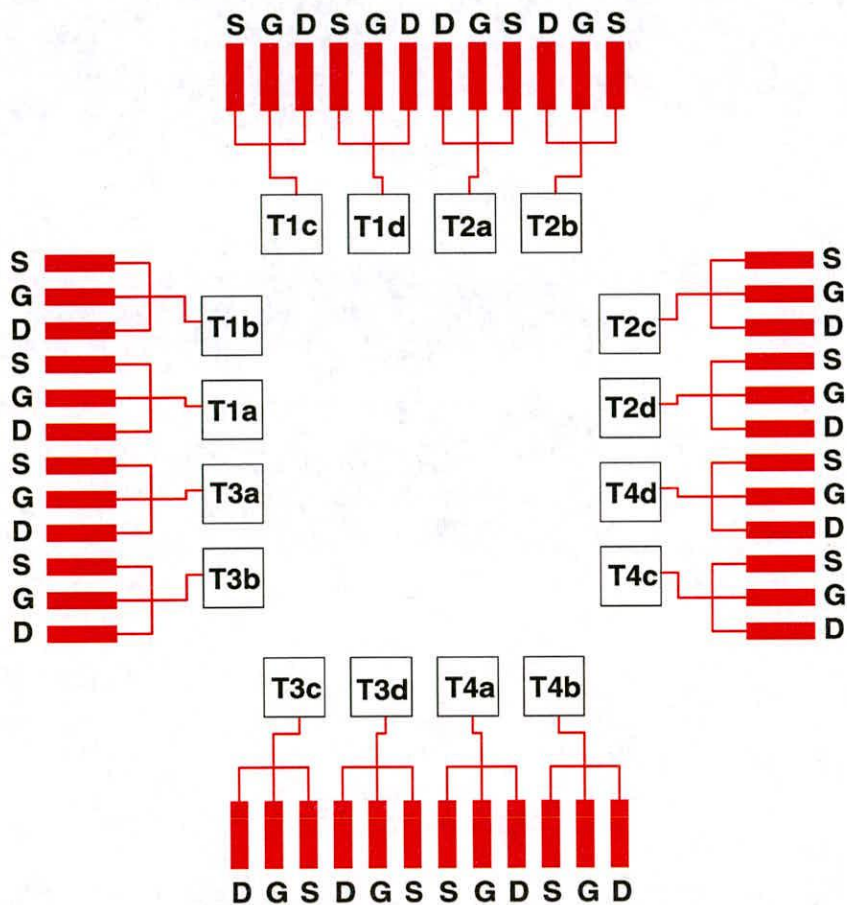


Figure 5.7      Layout of the transistors in the pattern *Design1*

Contact Length		Gate Length	
T1	1μm	a	0.5μm
T2	0.5μm	b	0.25μm
T3	0.25μm	c	0.1μm
T4	0.1μm	d	0.05μm

Table 5-2      Key of transistor gate and contact dimensions for pattern *Design1*



## 5.3 MOS Device Structure

The structure of the MOS devices was the same for both the *Design0* and *Design1* patterns, except for the variation in the defined gate, contact and spacer length parameters. The layout of a designed transistor is shown in figure 5.8. The active area is overlaid with the polysilicon gate electrode. The contact to the polysilicon is made via a pad at the end of the electrode. The source/drain contacts are situated either side of the gate electrode within the active area. A sidewall spacer is defined over the gate electrode down the width of the active area and an isolation oxide borders the active area.

### 5.3.1 Transistor dimensions

The width of the device is defined by the overlap of the gate electrode over the active area. The transistors width is  $6\mu\text{m}$  and the contact width is  $4\mu\text{m}$ . There is a defined  $1\mu\text{m}$  gap between the edge of the contact and the outside edge of the active area. The pad of the gate electrode is  $4\times 4\mu\text{m}$  and the contact hole is defined centrally on the pad with dimension  $2\times 2\mu\text{m}$ .

The length of the gate and contacts is changed for different transistors and the definitions for the two patterns are detailed in section 5.2.3. The separation of the edge of the contact and gate electrode is half the defined length of the contact ( $x/2$ ). The metal level is defined to cover the contact hole but not short circuit the two junctions by connecting them together. The pattern edge, for the metal, is defined to lie halfway between the contact hole and the gate electrode, i.e. a distance  $x/4$  from the gate.

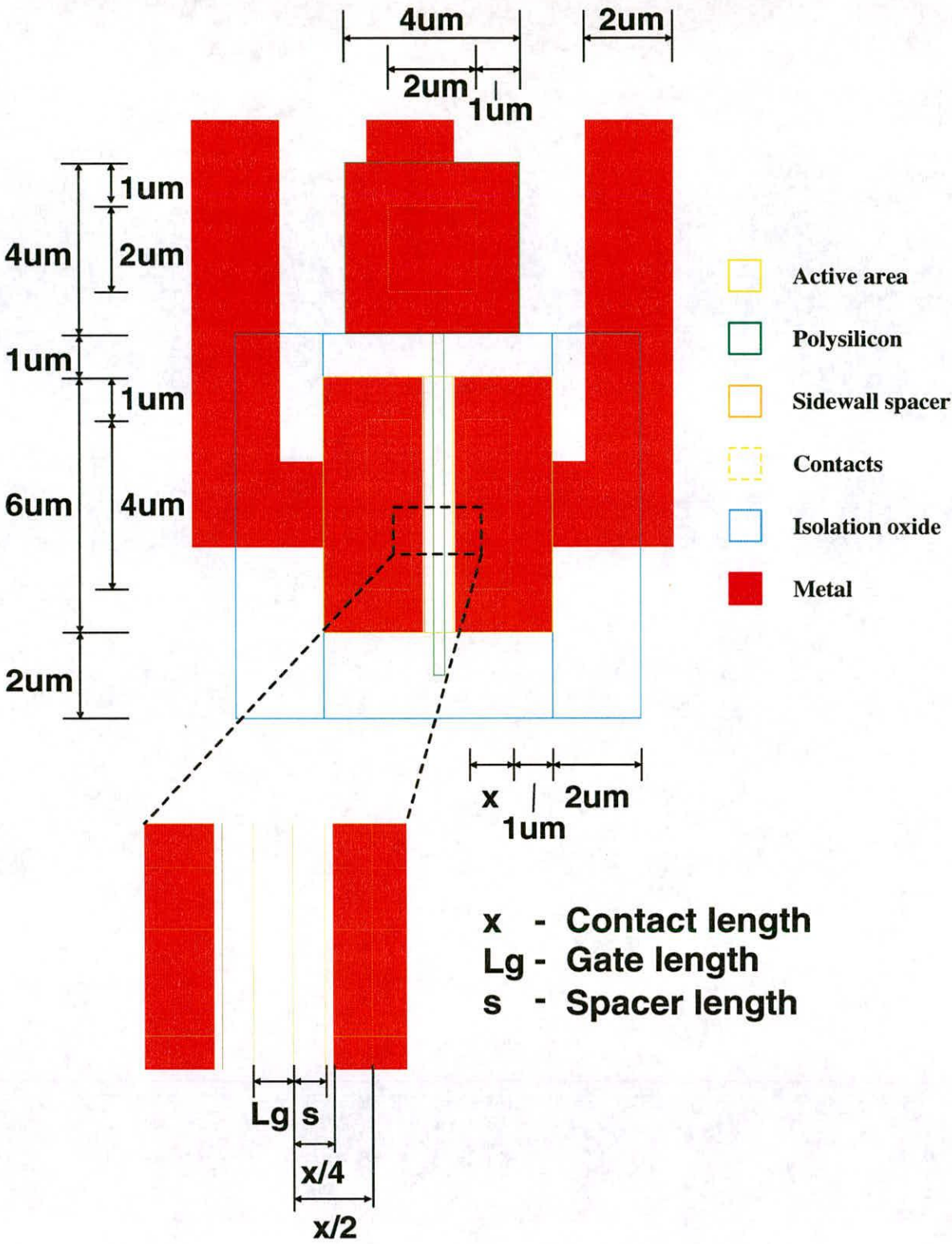


Figure 5.8 Mos device structure

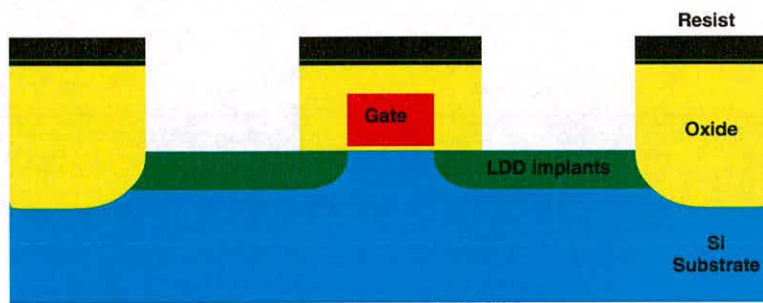


### 5.3.2 Sidewall spacer

The sidewall spacer of the devices was defined using electron beam lithography. This novel technique of defining the spacer was employed to enable the use of variable sized and asymmetric shaped profile spacers. The spacer was defined in photoresist and the pattern transferred to the oxide with a reactive ion etch process, the structure of the spacer immediately after the pattern transfer step is shown in figure 5.9. Two different types of spacer were employed in the device experiment, one with a 100nm extension from the gate electrode (defined in figure 5.8 as the distance 's') and the second with a 200nm extension.

### 5.3.3 Isolation oxide

An isolation oxide was defined around the border of the devices active area to prevent a leakage path from the ion implantation. The border was to be patterned with the same lithography process as the sidewall spacer and is displayed in figure 5.9. The border was defined to be 2 $\mu\text{m}$  wide around the active area, except between the gate electrode pad and the active area where the pattern was defined as 1 $\mu\text{m}$  wide. This pattern was implemented during the processing of the devices and was not originally designed into the experiment. The border was included in response to the removal of the field oxide bordering the devices during a processing stage. The rapid implementation of the oxide border highlights the flexibility of the e-beam system in quickly designing and implementing patterns.



**Figure 5.9**      **Diagram of the sidewall spacer profile and isolation oxide**

## 5.4 Processing Techniques

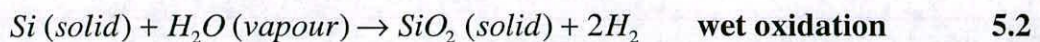
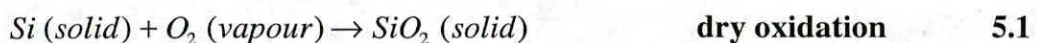
The processing of the MOS devices requires various techniques to deposit/remove layers of material or define structures on the wafer substrate. This section explains the techniques used in the device fabrication process.

### 5.4.1 Layer growth/deposition

#### Thermal oxidation

Thermal oxidation of silicon produces silicon dioxide ( $\text{SiO}_2$ ). The use of  $\text{SiO}_2$  in VLSI processing is common for many applications, including the isolation of individual devices with a local oxidation of silicon (LOCOS), gate oxide dielectric in MOS devices, a masking layer to protect against ion implantation and passivation of the silicon surface.

The growth rate of the  $\text{SiO}_2$  is related to the temperature at which the reaction takes place and the ambient that the Si material is exposed to. Temperature ranges of the order  $700^\circ\text{C}$ - $1300^\circ\text{C}$  are common for the oxidation of silicon, although a thin native oxide,  $<20\text{\AA}$ , will form at room temperature. The oxidation reaction will be increased if the ambient is changed from a dry,  $\text{O}_2$ , ambient to one that is wet,  $\text{H}_2\text{O}$ . The equations of these two reactions are highlighted in equations 5.1 and 5.2, below



The rapid growth rate of the oxide in the wet environment makes it ideal for use in the LOCOS process and as an implantation mask, although it does not possess the properties that are required for a gate oxide. The gate oxide has to be thin (15-200nm) and uniform in thickness across the wafer, also defect free to withstand the high electric fields from the gate electrode. A dry oxidation process allows control of



these parameters and the addition of impurities, such as HCl, in the process slows the reaction rate down and allows a more controlled reaction.

### Chemical vapour deposition

Chemical vapour deposition (CVD) involves the formation of solid layers on the surface of a substrate by the reaction of chemical gases. The layers that can be formed with this process include silicon nitride ( $\text{Si}_3\text{N}_4$ ) and polycrystalline silicon (poly-Si). The sequence of CVD involves the introduction of reactant and inert gases, at a controlled flow rate, into a reaction chamber. The gases then diffuse to the substrate, where the reactants are absorbed. Film-forming chemical reactions occur at the surface of the substrate which produce the required deposited layer and any by-products of the reaction are removed from the chamber.

The deposition rate of the CVD process is governed by the following two parameters[Kern 1979]:

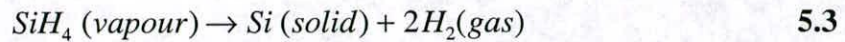
- rate of mass transfer of the reactant gases to the substrate surface.
- rate of surface reaction of the reactant at the substrate surface.

The rate of mass transfer can be increased by performing the reaction in a low pressure environment. The reduced pressure causes the boundary layer above the wafer surface, which the reactants must diffuse across, to be diminished, thus increasing the flow of reactants[Hammond 1979]. The name of this process is low pressure chemical vapour deposition (LPCVD). The surface temperature is an important parameter for the surface reaction rate, the combination of this and the mass flow rate control the rate at which the reaction takes place. At high temperatures the reaction rate exceeds the rate at which the reactants arrive at the surface and the reaction is said to be *mass-transport limited*. For lower temperatures, and hence lower reaction rates, the deposition is *reaction rate limited*.

Polycrystalline silicon (poly-Si) films, that are widely used to fabricate gate electrodes and interconnects in MOS circuits, can be deposited with an LPCVD process. The material properties of poly-Si are similar to those of bulk-Si and allow the material to be subjected to high temperature processing after deposition. The

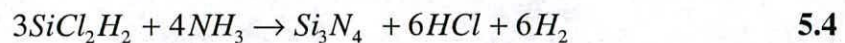


deposition process involves the thermal decomposition of silane ( $\text{SiH}_4$ ) in the temperature range 580-650°C. The overall reaction for the process is shown in equation 5.3 below.



LPCVD is used to deposit poly-Si because of its uniformity, purity and economy[Harbeke 1984]. The poly can also be heavily doped during the deposition process which reduces the sheet resistance of the material.

Silicon nitride ( $\text{Si}_3\text{N}_4$ ) can also be deposited with a LPCVD process.  $\text{Si}_3\text{N}_4$  can be used as a masking layer for selective oxidation, because it is difficult for oxygen to penetrate through the nitride to the underlying layer. The nitride is deposited on a thin pad oxide, that is used as a stress relieving layer. LPCVD of silicon nitride occurs with the reaction of dichlorosilane ( $\text{SiCl}_2\text{H}_2$ ) and ammonia ( $\text{NH}_3$ ) at temperatures between 700-800°C. The reaction is shown in equation 5.4.



### Electron-cyclotron resonance plasma CVD

Electron-cyclotron resonance (ECR) plasma CVD can be used to deposit  $\text{SiO}_2$  and silicon nitride films. Deposition occurs in a low pressure environment (1-2 mtorr) with an ECR plasma generated at microwave frequencies of 2.45ghz. Magnetic fields surround the microwave cavity and produce a field gradient that directs the ions of the plasma to the surface of the wafers. For the deposition of  $\text{SiO}_2$  a gas mixture of  $\text{SiH}_4$ ,  $\text{O}_2$  and Ar is introduced in a controlled manner into the reaction chamber[Wolf 1990].

The low temperature deposition of the ECR films (20-150°C) allows the process to be used after the deposition of metal onto the wafers. Results also indicate that the properties of the deposited  $\text{SiO}_2$  layers are identical to those of LPCVD deposited



films[Bulat 1992]. Divergence in the magnetic field can, however, produce films of non-uniform thickness across a wafer.

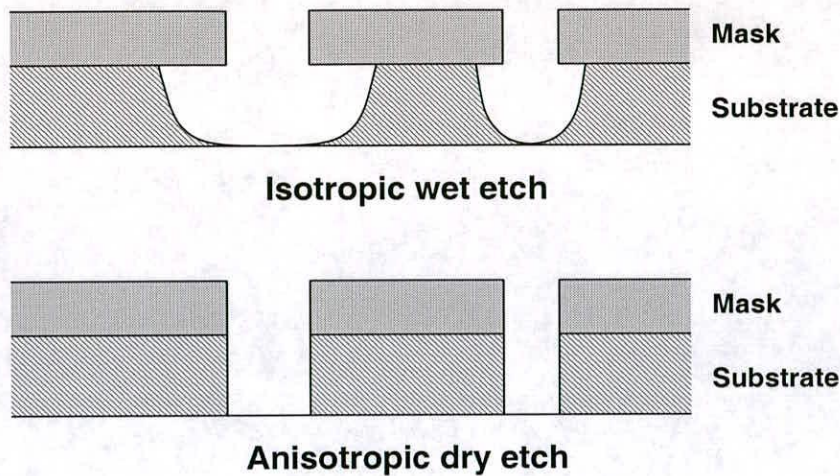
Plasma enhanced chemical vapour deposition (PECVD) operates with a similar principle to ECR plasma CVD, with a radio frequency plasma enhancing the deposition process that also occurs at low temperatures. The ECR deposition takes place in an environment that is at a pressure that is an order of magnitude lower than that for PECVD, this has the effect that ECR oxides can fill spaces with a much smaller aspect ratio than those deposited with PECVD. ECR deposition was used for the deposition of some oxides in the fabrication of the devices due to the availability of the equipment.

### **Sputter deposition of thin films**

Sputtering is a technique used in the deposition of metallic films in VLSI fabrication. Many metallic materials including aluminium, titanium, platinum and tungsten can be sputtered onto the surface of a wafer. The process involves the generation of ions in a low pressure environment, that are directed at a target of the metal that is to be deposited. The ions collide with the target and dislodge atoms from the surface of the material. The sputtered atoms are transported to the wafer surface where they condense to form a thin film[Wolf 1986]

### **5.4.2 Dry Etching**

Dry etching of layer materials in VLSI processing allows control over the etch profile of the material that is not possible with wet chemical etch techniques. Wet etching is an isotropic process, where the etched material is removed equally in both the vertical and lateral directions. A dry etch can produce an anisotropic removal of material, where the direction of the etch is restricted to a vertical profile. The results of isotropic and anisotropic etches are shown in figure 5.10.



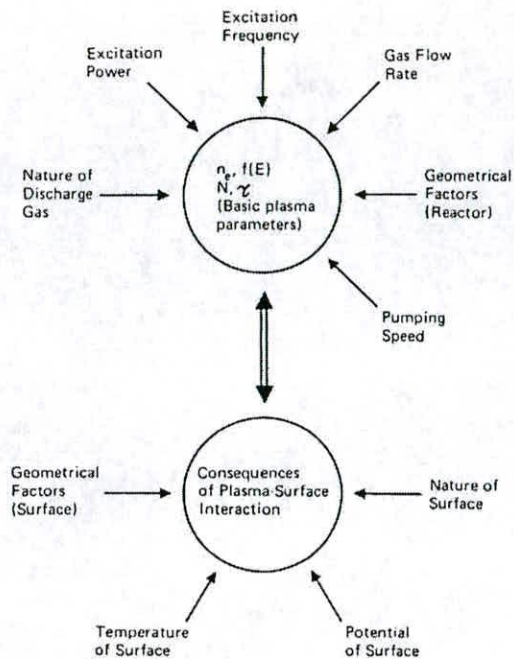
**Figure 5.10** Diagram showing the features produced with a isotropic wet etch and anisotropic dry etch

Reactive ion etching (RIE) is a dry process that combines the two techniques of sputter-etching and plasma-etching. The process occurs in a molecular-gas plasma where the dimensional control of the etch is provided by the sputtering of the layer material, and the surface reactions, induced by the plasma etching, control the selectivity of the process between different layers. The plasma is produced by applying an electric field to the reactant chemicals introduced into the low pressure (<1 Torr) chamber. The field causes the gas to break down and become ionised producing the etchant species in the plasma[Sze 1985]. The reactants are transported to the surface of the wafer by diffusion through the boundary layer above the surface. The reactant is then absorbed on the surface which is followed by a chemical reaction to form volatile compounds that etch the layer material. These compounds desorb from the surface and are then pumped out of the system. The anisotropic aspect to the etch occurs because of the assistance of the sputter ions in the vertical direction of the etch, the etch in the lateral direction is determined only by the etch rate of the plasma produced reactants, which act isotropically.

The qualities of an etch process depends upon many external aspects of the dry etch system, such as feed gas, power and pressure. Adjusting any of these parameters can affect two or more of the plasma parameters that affect the etch. Fig 5.11 shows a



representation of the parameters that affect the gas and surface interactions in a RIE system.



**Figure 5.11** Representation of the parameter problem in plasma etching systems ( $n_e$  is the electron density,  $f(E)$  is the electron energy distribution function,  $N$  is the gas density and  $\tau$  is the residence time [Wolf 1986])

### Silicon dioxide

A fluorocarbon based plasma is used to etch  $\text{SiO}_2$ . Adding Hydrogen ( $\text{H}_2$ ) to carbon tetrafluoride ( $\text{CF}_4$ ) does not significantly reduce the etch rate of  $\text{SiO}_2$ , although the selectivity of the etch over Si is improved. A mixture of trifluoromethane ( $\text{CHF}_3$ ) and Helium (He) can also be used as a selective etch for  $\text{SiO}_2$ .

The film characteristics of oxide can affect the etch rate, for a given set of processing conditions. A thermally grown oxide will etch at a slower rate than CVD  $\text{SiO}_2$  films. Doping of the oxide film will also affect the etch rate.

### Polysilicon

Poly-Si etching is used to define the gate electrode in MOS devices. The patterning of this structure is a critical feature in the processing of the devices, as a change in

the dimensions of the gate can severely affect the operating characteristics. The poly-Si etch process must exhibit excellent linewidth control and high uniformity of etching. The process must also have a high selectivity between the Si material that is to be etched and the SiO<sub>2</sub> layer of the gate oxide underneath the poly. The gate oxide can be very thin (<10nm) and overetching through this oxide would cause a rapid removal of the substrate Si material, and hence the implanted junction areas.

Process chemistry for the etching of polysilicon include the use of silicon tetrachloride (SiCl<sub>4</sub>) and argon (Ar). Chlorine plasmas exhibit good selectivity over SiO<sub>2</sub> and anisotropic characteristics, although the etch rate is slower than that of fluorine based etches.

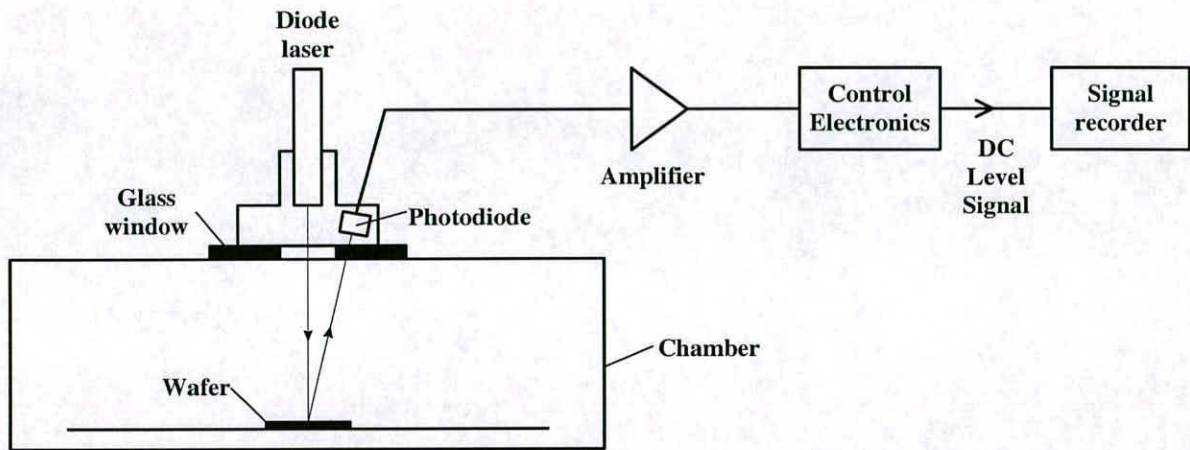
### 5.4.3 End point detection

End point detection is a non-intrusive method of determining when a dry etch has removed the layer of etch material. As highlighted in the previous section the dry etch process is sensitive to the many parameters that control the etch. Even if these parameters are tightly controlled the process is still liable to changes in the reactant chemistry from uncalibrated variables such as outgassing, virtual leaks and backstreaming from pumps. Any changes in the chemistry can lead to a change in the etch rate of the process and because of this a more reliable method of determining the end-stop of the etch process is necessary.

A reliable method of end point detection for a dry etch process allows a reduction in the amount of overetch a sample is given and increases the reproducibility of a process. Methods of end point detection include 1) Laser interferometry and relectivity; 2) Optical emission spectroscopy; 3) Direct observation of the wafer surface through a viewing port on the chamber; 4) Mass spectroscopy[Marcoux 1981]. An end point detection system was developed for monitoring the dry etch processes in the device experiment. The system was based on the laser interferometry/reflectance method. A schematic of the system layout is shown in figure 5.12 below. The laser head is situated outside the chamber and the light is emitted through a glass window onto the target wafer. The intensity of the reflected



light is amplified from the receiving photodiode and input to the control electronics. The electronic unit changes the light intensity signal into a linear d.c. signal which is then recorded by a computer after analogue to digital conversion.



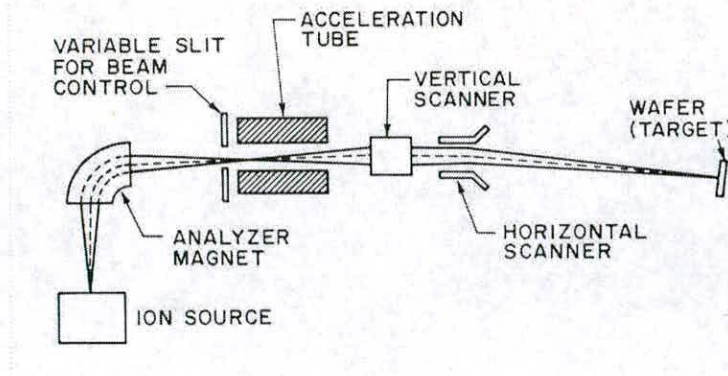
**Figure 5.12** Schematic diagram of a laser interferometry/reflectance end point detector

The method of operation of the end point detector depends upon layers that are being targeted by the laser. The system operates in interferometry mode if the film that is being monitored is a transparent film, such as  $\text{SiO}_2$ . As the film etches the amplitude of the reflected light varies, in an approximately sinusoidal manner, because of interference between the reflected light from the changing surface of the film. The end point is determined by the 'flattening' of the output signal as the film etches to zero thickness. Laser reflectance is used if the film is reflective, such as Al. If the layer being etched has a different reflectance to the layer underneath there will be a change in the reflected signal once the layer has etched to end point.

#### 5.4.4 Ion implantation

Ion implantation is a process where energetic, charged particles are introduced into a silicon substrate. The ions are implanted with typical energies in the range of 10-200keV and doses in the range  $10^{11}$  to  $10^{16}$  ions/cm<sup>2</sup>. A schematic of an ion implantation system is shown in figure 5.13. The ionised dopant atoms are contained in the ion source. The ions pass through a mass-separating analyser magnet, where any unwanted ion species are removed. The selected ions are then accelerated by an

electric field in the accelerator tube, where the beam is scanned onto the wafer surface by horizontal and vertical scanners.



**Figure 5.13** Schematic of an ion implantation system[Brodie 1982]

Ion implantation is a preferred technique over the alternative methods, such as diffusion of ions, because there is a larger degree of control over the amount of ions implanted into the substrate (typically  $\pm 3\%$ ). The implanted ions also have a vertical distribution in the substrate, where there is a greater lateral distribution with diffusion. The ions can be implanted to different depths within the substrate, allowing variable shaped implant profiles such as LDD structures.

After implantation into the target substrate the energetic ions lose their energy and come to rest. The mechanisms that stop the ions are by electrical and nucleic interaction in the substrate. Electrical stoppages occur when the energy from the ion is transferred to an adjacent electron which surrounds the atoms in the substrate lattice. This interaction cause *excitation*, where the electrons are transferred to a higher orbit, or *ionisation*, where the electrons are ejected from their atomic orbits. The energy loss that these interactions cause eventually slows the ion down until it stops. Nuclear collisions occur when the ion impacts with an atom and removes it from the lattice[Sze 1985]. The effect of dislodging atoms from the lattice causes damage to the substrate. The effect essentially makes the implanted region an amorphous layer of silicon. The region can be electrically activated by annealing the wafer to restore order in the lattice structure.



## **5.5 Summary**

The layout of the devices for fabrication have been described in this chapter. The layout of the chip sites on the silicon wafers have been displayed, with the organisation of the chip sites and their individual e-beam patterning area. The dimensions of the transistors in the patterning arrays have been highlighted and the processing techniques used in the fabrication have been described to provide an insight into the various processes.

## **Fabrication Procedure**

---

The experiment to fabricate MOSFET devices required the use of many processing techniques. Some techniques were specific to procedures used in electron beam lithography, such as the chemically amplified resists, and as such were not characterised for use within the fabrication facility of the EMF. This chapter describes the characterisation of the new processing techniques employed within the experiment, using the processing technology that was described in section 5.4. Finally the sequence with which the fabrication process was performed is described.

### **6.1 Characterisation**

Before fabrication of the experimental devices could proceed the processes used in certain fabrication steps had to be characterised. This characterisation was necessary for consistent reproduction of each stage in the fabrication process across the multiple wafers processed in the experiment. The main processing steps that required characterising were as follows:

- AZ PN 114, negative chemically amplified resist
- AZ PF 514, positive chemically amplified resist
- Gate electrode fabrication with polycrystalline silicon

Although the development of high resolution processes for these chemically amplified resists have been previously researched, the integration of the high resolution lithography processes into a device fabrication process have not previously been investigated. The characterisation for each of the processes will be described in the following sections.



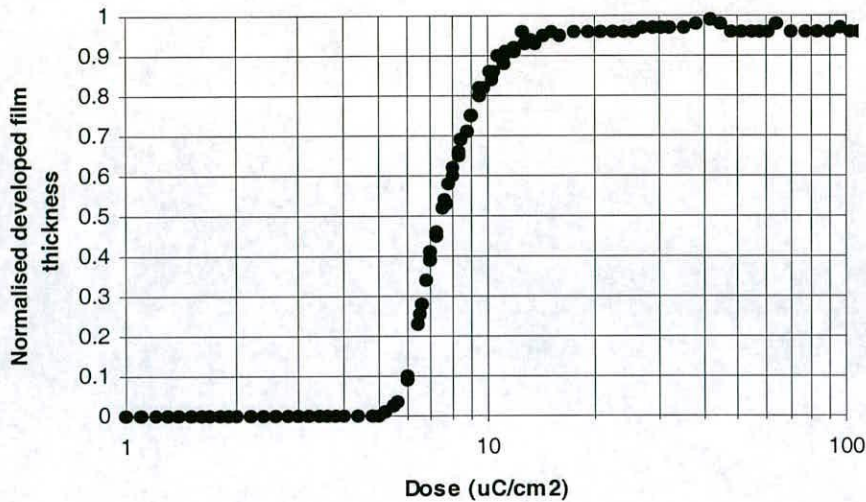
### 6.1.1 Negative photoresist

The chemically amplified negative resist used in the processing was the Hoechst AZ PN 114. This resist exhibits the properties of high sensitivity and dry etch resistance required in a manufacturing resist process [Early 1992]. The resist properties and processes for high-resolution lithography have been intensively researched [Early 1992, Macintyre 1996, Cui 1997]. The results of these studies were used in formulating the processes of the device experiment. The parameters of the resist process used were as follows:

- Vapour prime wafers with HMDS
- Spin photoresist on wafers (see section 6.1.1 on resist thinning)
- Softbake on vacuum hotplate at 120°C for 120s
- Expose wafers with electron beam lithography (refer to section 6.1.1 on dose control)
- Immersion develop in MF319 (0.237N) for 90s
- Rinse with de-ionised water
- Dry wafers in the centrifuge

#### Resist contrast and sensitivity data

The response curve of AZ PN 114, when developed using the parameters highlighted above, is shown in the graph of figure 6.1. The steep profile of the curve indicates the high contrast of the resist, which was calculated to have a value of  $\sim 4$ . The sensitivity of the resist ( $D_g^{0.5}$ ) is  $\sim 7.5 \mu\text{C}/\text{cm}^2$ .



**Figure 6.1** Sensitivity curve for AZ PN 114 exposed by e-beam lithography and developed in Shipley MF 319.

### Pattern residue removal

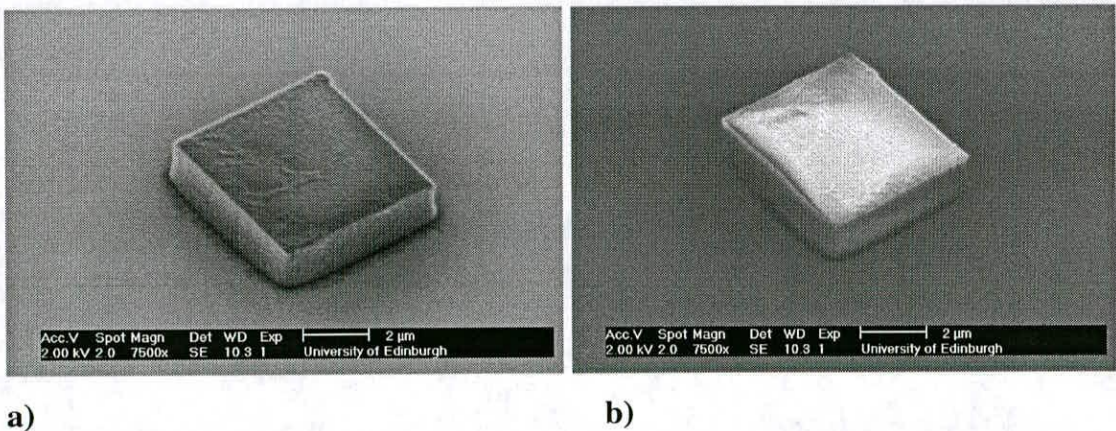
The initial development tests on the resist for the fabrication of the device active areas showed a residue around the base of the developed pattern, displayed in figure 6.2a. Secondary electron scattering, enhanced by the relatively low 30kV accelerating voltage, was probably the cause of the residue effect. This extension of resist material from the base of the pattern may have led to interference with the accurate pattern transfer of the defined resist image of the active area into the nitride layer, by causing a masking effect with the residue. For this reason the removal of the thin residue layer was investigated.

The removal of the residue was to take place after the lithography level had been performed. It was thus important for the process to maintain the dimensions of the original pattern. The properties of the oxygen plasma ash in the anisotropic RIE system were investigated for this reason. The vertical directionality of the etch would remove the small amount of the resist around the base of the pattern and also a small amount of resist from the surface of the pattern, while not affecting the profile or dimensions of the pattern sidewalls.



Test structures in the shape of active area patterns were exposed with sufficient dose for correct exposure and then imaged in the SEM to visually inspect the amount of residue around the pattern. After recording the images the patterns were split into four samples that were etched for 5, 10 and 15 seconds in a O<sub>2</sub> plasma. The samples were again imaged in the SEM for inspection of the residue material.

The residue had etched away after the first 5s etch, shown in the image of figure 6.2b. This showed that subsequent etches of 10s and 15s were superfluous, only removing more of the resist material off the pattern. Comparison of the dimensions of the pre and post-etch patterns showed no change in the dimensions of the pattern thus deeming the process suitable for the removal of the resist material from the developed patterns in the negative AZ PN 114 photoresist.



**Figure 6.2**      **4x6µm active area pattern a) before residue removal. b) post O2 plasma ash.**



Resist thinning

The resolution of photoresist increases with decreasing thickness [(I)Rangelow 1994]. The very narrow sub 100nm features required for the gate level of the experiment required the photoresist to be reduced in thickness from the undiluted solution. The layer thickness of the undiluted resist is 1 $\mu$ m when spun onto HMDS primed wafers at 8000 rpm. As well as impeding the resolution of the resist, the relatively thick 1 $\mu$ m layer has too high an aspect ratio, as the small patterned features with the thick resist were susceptible to falling sideways during the subsequent processing steps, shown in figure 6.3.

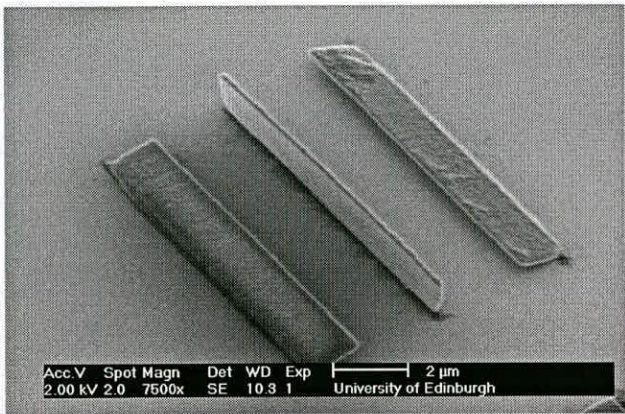
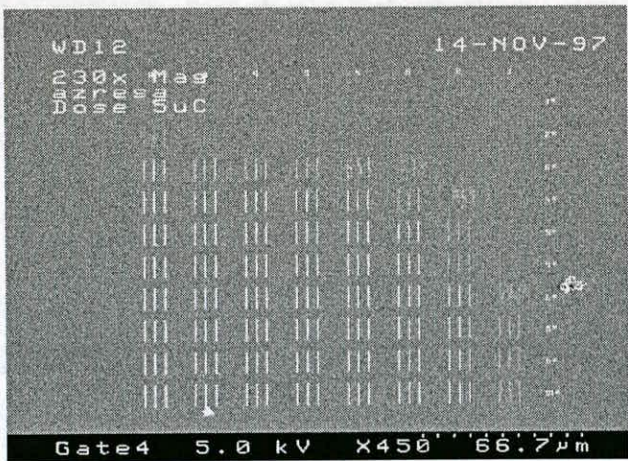


Figure 6.3 Collapsed 100nm line patterned in 1 $\mu$ m thick photoresist

High-resolution studies with the resist by Macintyre used resists of thickness ranging between 30nm and 300nm to achieve patterns with linewidths below 100nm [Macintyre 1996]. To reduce the thickness of the spun on resist it was mixed, by ratio, with AZ 1500 thinner from Hoechst. The thin resist that had been diluted in the ratio 1:5 (resist:thinner) was measured at a thickness of ~100nm and produced features that were less than 100nm across, shown in figure 6.4. The thickness of the resist used for the gate level processing was, however, thinned down in the ratio of 1:3, to a thickness of ~200nm, because of the compromise required for the subsequent processing of the wafers in the device experiment. The requirements of the resist thickness are highlighted in section 6.1.4 on the polysilicon level of processing.







**Figure 6.5** Test pattern of lines with increasing width exposed with increasing dose between 5 and 50 $\mu$ C/cm-2

The calibration of the pattern doses was characterised with test patterns of the type shown in figure 6.6. Two sets of patterns were used for this purpose, the first called ‘azresa’ and the second ‘gate230’. The two sets of patterns are shown in figures 6.6a and 6.6b.



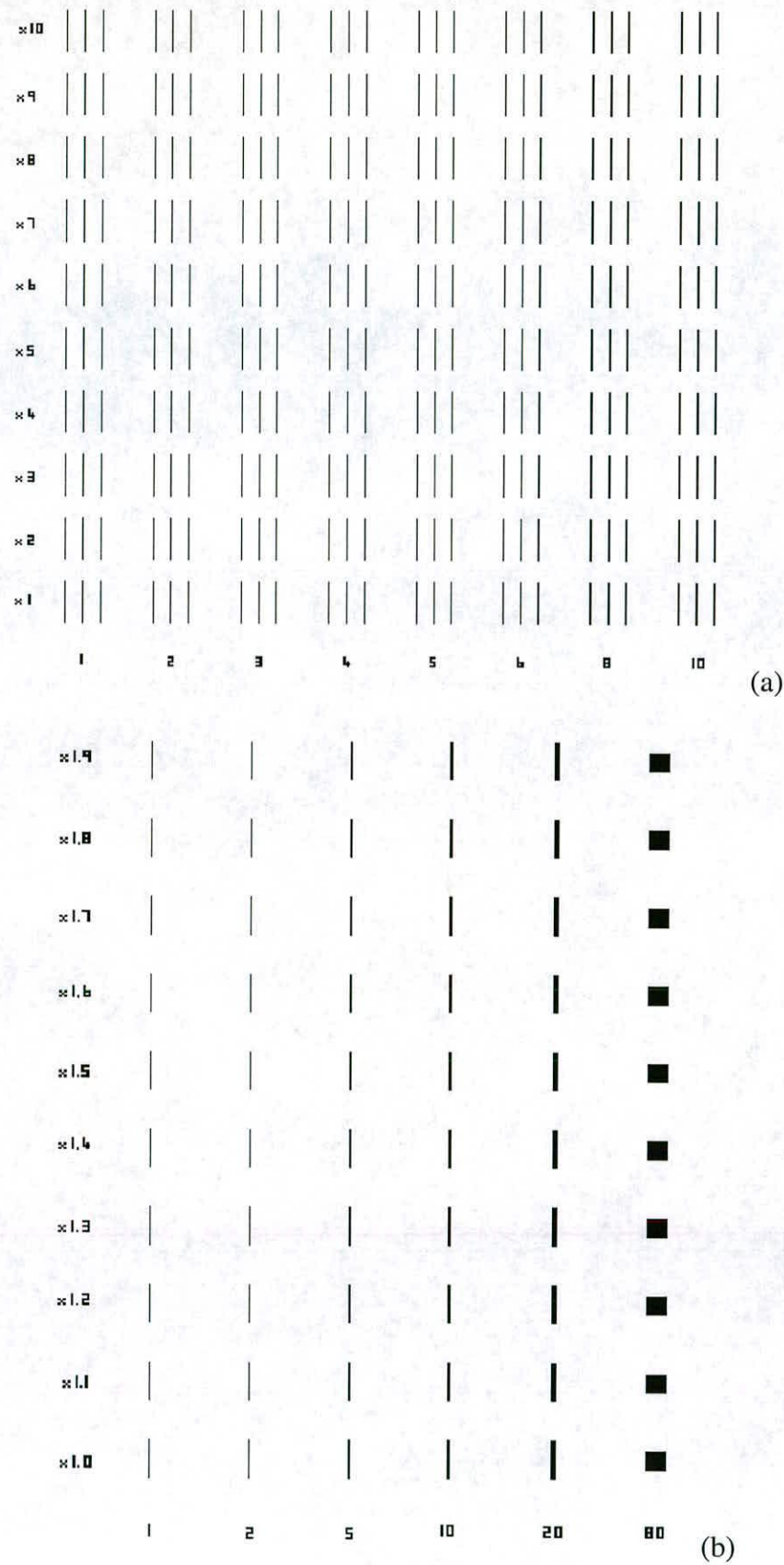


Figure 6.6 a) Test pattern 'azresa' b)Test pattern 'Gate230'

The first pattern, *azresa*, used in the early calibration tests was designed as a coarse grid to prove the reproducibility of the development process and also find the approximate doses required for exposure. The patterns were basic lines 200 pixels tall and between 1 and 10 pixels across. These dimensions defined lines of  $10\mu\text{m}$  tall and  $0.05\mu\text{m}$  to  $0.5\mu\text{m}$  across in the  $200 \times 200\mu\text{m}$  patterning field that was to be used in the device experiment. The dose given to the lines was incremented with a multiplication factor, starting at  $\times 1$ , which is the base dose as programmed into the computer for the patterning dose. This increased up to  $\times 10$  which extended the dwell time of the pattern exposure by 10 times over the dose given to the base dose pattern.

After the approximate pattern doses were determined for the different pattern sizes with the '*azresa*' pattern, the requirements for the shapes that were to be used in the critical gate lithography level of exposure could be investigated with the '*gate230*' test pattern. This pattern defined the exact shapes that were to be found in the gate level of exposure, with 1,2,5,10 and 20 pixel width lines, all 120 pixels tall and a 80 pixel square box which replicated the contact pad at the end of the gate electrode. The exposure grid used for this test pattern was a lot finer, however, with nine increments of only  $\times 0.1$  from the base dose of  $\times 1.0$  up to  $\times 1.9$ .

These test patterns were suitable for the characterisation of the pattern dosage for the critical exposure levels in the device experiment because they calibrate individual lines. The proximity effect can be ignored in this characterisation technique because of the isolated nature of the lines to be exposed in the device experiment layout.

### **Line patterning results**

The doses that were found to produce the correct exposure of the patterns, with a base dose of  $24\mu\text{C}/\text{cm}^2$ , for the gate lithography level of the experiment are shown in table 6.1:



Line Pixel Width	Defined Pattern Size (nm)	Dose Multiplier	Pattern Dose ( $\mu\text{C}/\text{cm}^2$ )
1	50	$\times 3.75$	90
2	100	$\times 2.4$	57.6
5	250	$\times 1.5$	36
$\geq 10$	$\geq 500$	$\times 1.0$	24

Table 6.1 Exposure conditions for AZ PN 114

The minimum feature size that could be reproduced in the photoresist was not, however, the defined 50nm for a 1 pixel pattern. The feature from this pattern developed with a length of 72nm. This is shown with the image of a cross-sectioned 1 pixel line in figure 6.7. The minimum feature size was consistent in its reproduction which led to the conclusion that this was the minimum feature size attainable for the defined resist process parameters. This is not the ultimate resolution that has been achieved with the resist, as Macintyre et al have demonstrated 30nm resolution with individual lines and 30nm thick resist [Macintyre 1996]. However this is the highest resolution reported for AZ PN 114 lithography that has been integrated into a fabrication process for MOSFET devices.

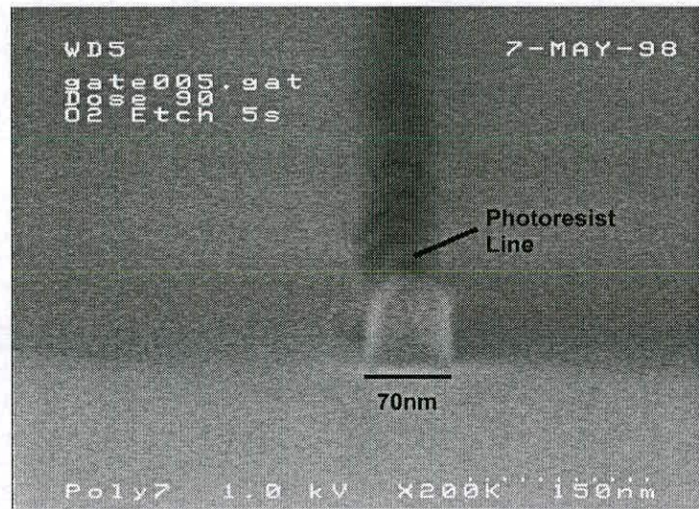


Figure 6.7 Cross-section of a negative photoresist line of 1 pixel defined width.

### 6.1.2 Positive Photoresist

The resist AZ PF 514 from Hoechst was used as the positive resist for defining the contact holes in the experiment. The process used in the deposition and development of the resist was developed from the research previously performed by I.W. Rangelow et al [Rangelow 1994] and the process used was as follows:

- Vapour prime wafers with HMDS
- Spin photoresist on wafers, 3000 rpm for 30s (see section 6.1.2 on resist thinning)
- Softbake on vacuum hotplate at 126°C for 82s
- Expose wafers (refer to section 6.1.2 on dose calibration)
- Immersion develop in diluted MF319 (0.178N) for 90s
- Rinse with de-ionised water
- Dry wafers in the centrifuge

#### Resist thinning

As with the thin layer of negative resist used for the gate level processing, the positive resist can not be reduced too much, because the layer has to provide good step coverage of the patterned devices. If the resist were too thin it would not spin over the device where the contact windows are to be etched. The dilution of 1:2 (resist:thinner) was chosen as the solution of resist for the positive resist processing as the 300nm thickness of the resist layer provided good coverage of the features on the wafer.

#### Pattern dose calibration

A similar test pattern to that of the gate230 pattern, described for the negative resist characterisation in section 6.1.1, was used for the calibration of the positive resist. The patterns were designed to mirror the dimensions of those that were to be used in the patterning of the contact level in the device experiment. Two test patterns were produced for this purpose, firstly contacta was a series of patterns with a coarse increment, in  $\times 1.0$  steps, of the multiplication factor and contactb, shown in figure 6.8 used a finer increment of  $\times 0.1$  for the multiplication factor.



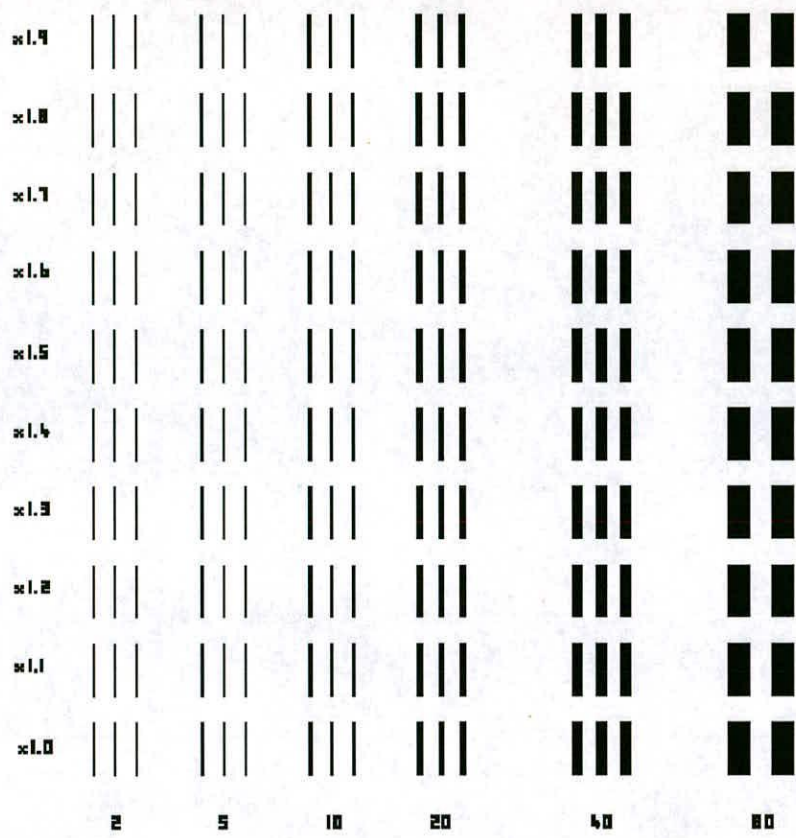


Figure 6.8      Test pattern contactb, used for the calibration of the positive resist AZ PF 514

Line patterning results

The pattern doses that produced the correct exposure dimensions of the patterns, with a base dose of  $5\mu\text{C}/\text{cm}^2$ , for the contact lithography level of exposure are shown in table 6.2:

Pixel Width	Defined Pattern Size (nm)	Dose Multiplier	Pattern Dose ( $\mu\text{C}/\text{cm}^2$ )
2	100	$\times 3.0$	15
5	250	$\times 2.0$	10
10	500	$\times 1.25$	6
20	1000	$\times 1.25$	6
$\geq 40$	$\geq 2000$	$\times 1.0$	5

Table 6.2      Exposure conditions for AZ PF 514

The smallest feature of the 2 pixel trench, exposed slightly wider than the defined 0.1μm, at 120nm. This is shown in the image of figure 6.9.



Figure 6.9 Image of a 2 pixel wide trench, exposed in positive AZ PF 514 photoresist.

6.1.3 Polysilicon processing

The polysilicon process characterisation involved the refining of the pattern transfer, using a dry reactive ion etch process, from the masking negative resist layer of the gate lithography process, through to the polysilicon layer underneath the resist.

Polysilicon etch process

The etch that is used to pattern the polysilicon must produce a line of poly that is of the same dimensions as the original masking feature. The etch must also not remove the thin gate oxide as this protects the silicon substrate from etching once the polysilicon material has been removed.

Three etch processes were used in the RIE system for polysilicon removal in the Edinburgh Microfabrication Facility. The process conditions and etch rates of the processes are displayed in the tables 6.3 and 6.4 respectively.



Process Conditions

	SiCl4 Flow	Ar Flow	Power	Pressure
	(ccm/min)	(ccm/min)	(W)	mT
Step1	15	15	100	25
Step2	15	15	50	25
Step3	15	0	50	50

Table 6.3      Process conditions for the polysilicon etch process

Etch Rates

	Si etch rate	SiO2 etch rate	Selectivity
	(nm/min)	(nm/min)	Si:SiO2
Step1	55	22	2.5:1
Step2	34	6	6:1
Step3	17	0.5	34:1

Table 6.4      Etch rates of the polysilicon etch process

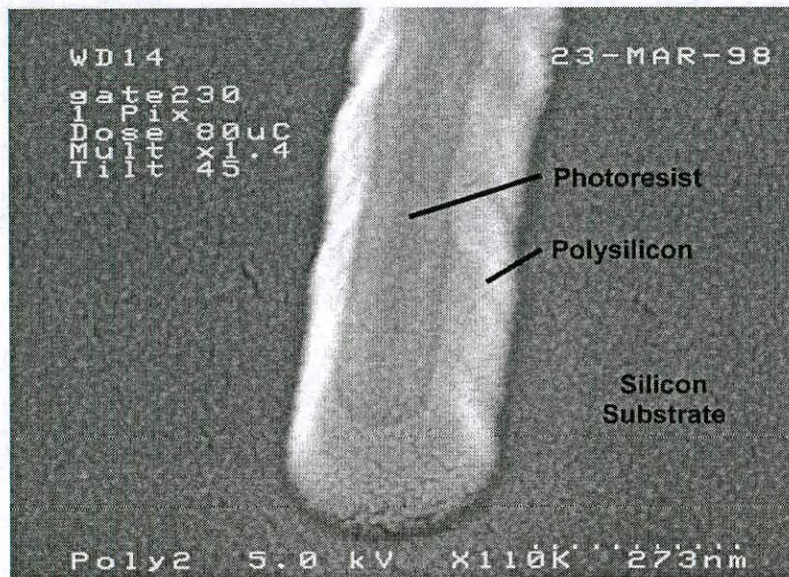
For the selectivity of the etch criteria to be met, a combination of the above processes is necessary. The unselective etches of Steps 1 and 2 can be used to remove the polysilicon material quickly without affecting the etching of the underlying gate oxide. The Step3 etch is then used as a directional etch to achieve a vertical profile of the polysilicon sidewalls, that is not achieved with the isotropic etches of Steps 1 and 2. Step3 is also highly selective to the gate oxide as the unmasked polysilicon is removed when this etch process is performed.

Resist on polysilicon etch tests

The initial tests for the pattern transfer etch involved patterning the negative resist directly onto the polysilicon layer and then etching the pattern with the RIE process after the resist had been developed.

This process was first performed using just the Step2 etch, which is mainly isotropic, and using the end point detector to determine when the poly had etched to the oxide.

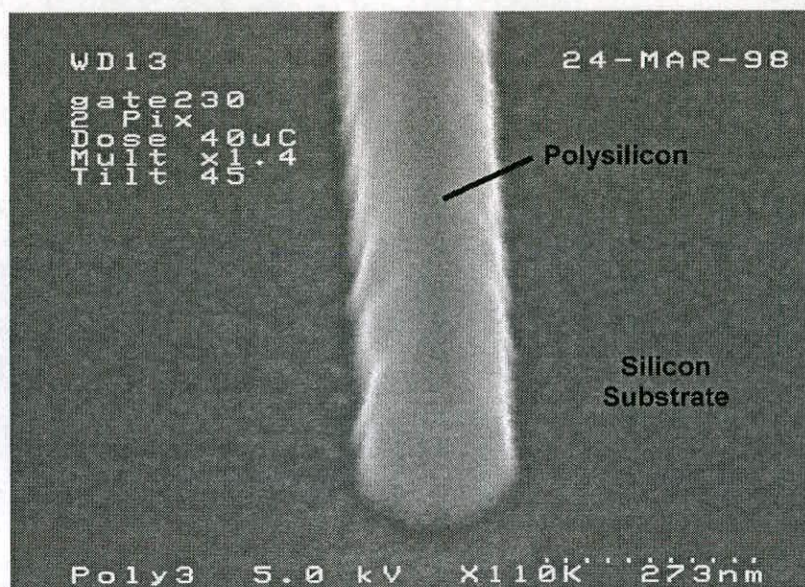
The resulting pattern is shown in figure 6.10. It can be seen from this image that the sidewalls of the poly are significantly sloped. The sidewall slope of the patterned poly is, however, required to be close to vertical to replicate the pattern from the resist. It can also be seen from this image that there is very little of the resist layer remaining. The resist for this experiment was thinned in the ratio 2:1 (resist:thinner), which resulted in a deposited layer 280nm thick. The poly layer on this experiment wafer was 145nm thick and it can be seen that although the resist layer is of undeterminable thickness, it is considerably less than twice that of the poly layer.



**Figure 6.10** Patterned polysilicon line after Step2 etch process using AZ PN 114 resist as a mask

A second test with the resist-on-poly process used the anisotropic Step3 etch after etching the poly to end-point with the Step2 process. The resulting pattern is shown in figure 6.11. The sidewalls of the patterned poly are of a more vertical profile than those highlighted in the previous paragraph. Although with this process the increased etch time, with the second etch step, has removed almost all the patterning resist.





**Figure 6.11** Patterned polysilicon line after Step2 followed by Step3 etch process

The resist on polysilicon etch process was deemed to be unreliable because of the resist removal during the process. Another process was investigated which used an intermediate pattern transfer layer that was more resistant to the harsh etch processes used in the polysilicon etch.

### Resist to oxide pattern transfer

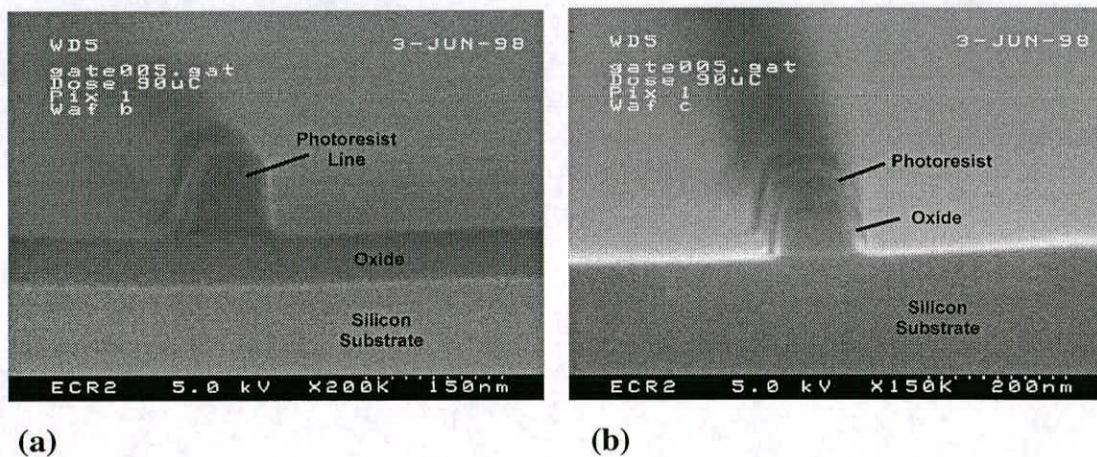
The negative resist material did not provide a reliable mask for the polysilicon etching. A more resistant material to the etch processes would need to be used if the gate level lithography was to be transferred into the polysilicon. As highlighted in the 'polysilicon etch process' parameter section, oxide has a higher selectivity over silicon with the etch steps used in the process. The properties of the resist to oxide pattern transfer were investigated to see if the resist pattern could be reliably reproduced in an oxide layer.

Because of the higher etch selectivity, the oxide layer does not need to be as thick as the polysilicon layer. With a resistant etch mask the full three step etch process could be used, and the approximate amount of oxide that would be etched with such a process can be approximated at 42nm (Step1:30s, Step2:300s, Step3:120s). The oxide that was to be used as the mask was the ECR deposited oxide. The deposition



rate of this oxide is not precise and so a 65nm layer was deposited on the polysilicon for the experiments.

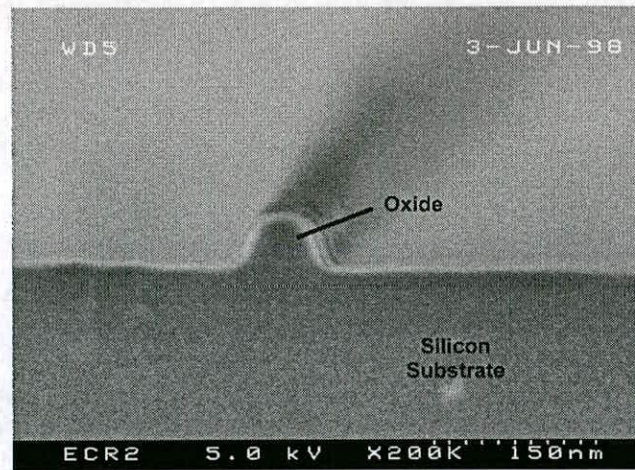
The lithography of the gate patterns was as discussed in section 6.1.1. and a dry RIE of 4 minutes duration transferred the resist pattern into the oxide. The pre and post oxide etch images of a patterned line can be seen in figure 6.12. Some resist material has been removed during the etch process, although the pattern has been successfully transferred into the oxide from the resist image, so the negative resist can provide a reliable masking material for pattern transfer into the oxide. The actual pattern transferred into the oxide is not replicated from the resist to the oxide. It can be seen from figure 6.12b that the oxide line is 124nm across the base, whereas the resist line is only 89nm. This is an unacceptable increase in linewidth for the processing.



**Figure 6.12** Image of a single pixel line a) Pre-oxide etch and b) Post-oxide etch

The increase in the patterned oxide feature during the pattern transfer was thought to have been caused by a polymer build up during the etch process. To remove this build up of material around the sidewalls of the patterned oxide a subsequent  $O_2$  plasma ash step was proposed. The results of a 2 minute ash step on a patterned oxide line is shown in figure 6.13. The image shows only the oxide line, as the resist material has been removed during the plasma ash process. The line shows that the resulting line has replicated the linewidth of the original resist line that masked the image.





**Figure 6.13** Image of an oxide line after a pattern transfer step from the resist and a 2 minute O<sub>2</sub> plasma ash

### Oxide to polysilicon pattern transfer

With the oxide as a mask for the polysilicon pattern transfer step a three stage etch process was investigated. The initial Step1 process was a highly unselective process used to cut through the native oxide at the surface of the polysilicon, this is used for a 30 second etch. The Step2 process is a mainly isotropic etch performed to the end-point of the poly etch, the sidewalls of the poly after this etch are sloped as highlighted in a previous section. The third, Step3 process is a anisotropic etch performed as a 25% overetch of the time for the Step2 process. The results of this etch are shown in figure 6.14. The polysilicon pattern transfers from the oxide pattern to within 10nm of the masking pattern. It can also be seen on this image that there is still a significant amount of oxide still masking the polysilicon after the three step etch process.





process using an Ar and  $\text{Si}_3\text{Cl}_4$  process. Removal of the masking photoresist revealed bare silicon wafers with etched alignment marks.

### 6.2.1 Active areas

A 20nm LOCOS buffer oxide was formed on the wafer with a dry oxidation process, followed by the deposition of 50nm of  $\text{Si}_3\text{N}_4$ . The active areas were then defined by a e-beam lithography process using the negative resist AZ PN 114. The nitride was then removed to expose the field region of the devices, leaving the nitride layer masking the active region of the devices. The field region was then defined with a 50kV ion implantation of Boron at dose  $4\text{e}12\text{cm}^{-2}$  for the n-FET devices and Phosphorous at dose  $2\text{e}12\text{cm}^{-2}$  for the p-FET devices. After removal of the photoresist a field oxide was grown with a wet process to a thickness of 250nm. After oxidation the nitride was removed by immersing the wafers in phosphoric acid, heated to  $165^\circ\text{C}$  for 35 minutes.

### 6.2.2 Channel implant and gate oxide

The buffer oxide covering the active region was removed by immersing the wafers in 4:1 buffered HF ( $\text{H}_2\text{O}:\text{HF}$ ) for 10s. The active area surface was then cleaned of film contaminants with a RCA clean process. A fresh mixture of  $\text{H}_2\text{O}:\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$  (5:1:1 by volume) was heated to  $70^\circ\text{C}$  and the wafer immersed for 5 minutes. After a dump rinse in DI  $\text{H}_2\text{O}$  the wafers were immersed in a  $70^\circ\text{C}$  solution of  $\text{H}_2\text{O}:\text{HCl}:\text{H}_2\text{O}_2$  (5:1:1 by volume) for 5 minutes, followed by a dump rinse in DI  $\text{H}_2\text{O}$ . Immediately after this clean process a 5nm sacrificial oxide was grown over the active region. A dual implant was performed on the n-FET devices with a shallow 20kv Boron implant at  $5\text{e}12\text{cm}^{-2}$  to change the substrate doping to adjust the threshold voltage of the devices. A deeper 60kV Boron implant at  $5\text{e}12\text{cm}^{-2}$  provides a punchthrough prevention implant. The p-FET devices were implanted at 100kV with Phosphorous at  $4\text{e}12\text{cm}^{-2}$ . After the removal of the sacrificial oxide and further RCA clean a gate oxide was grown with a dry oxidation process at  $785^\circ\text{C}$ . The measured thickness of the oxide was  $48\text{\AA}$ .



### 6.2.3 Gate formation

Approximately 150nm of polysilicon was deposited on the wafers by a LPCVD process at a temperature of 600°C. The sheet resistance of the material was reduced by doping the polysilicon using an ion implant process. The n-FET poly material was doped at 10kV with phosphorous at  $1 \times 10^{15} \text{cm}^{-2}$  and the p-FET material at 10kV with boron at  $2 \times 10^{15} \text{cm}^{-2}$ . The implants were then activated with an anneal step at 850°C for 15 minutes. The characterised pattern transfer technique described in section 6.2.4 was used to pattern the e-beam lithography defined gate patterns into the polysilicon.

### 6.2.4 Junction implants and sidewall spacer

The n-FET devices employed a lightly doped drain structure to reduce the hot carrier effects that are induced by the shortened channel lengths. After the formation of the gate a shallow source/drain extension of arsenic was implanted, at 20keV with a dose of  $2.5 \times 10^{12} \text{cm}^{-2}$ . The implant was self aligned using the gate structure as a mask. The p-FET devices were not processed at this time.

Masking for the source/drain implants is generally performed with a sidewall spacer that is engineered from a layer of CVD oxide. The oxide material remaining, after etching, provides a self aligned extension to the gate structure and masks the implantation of the junction ions. A different style of sidewall spacer was used in the device experiment. The spacer was an oxide material defined using an aligned electron beam lithography process. This type of spacer was used to investigate the suitability of the electron beam system to define novel sidewall spacer designs, such as asymmetric patterns around deep sub-micron gate structures. The types of structure defined for the experiment were, however, symmetrical spacers that extended 100nm and 200nm from the sidewalls of the gate electrode. The asymmetric sidewall spacer has recently been under investigation for sub-micron devices in the 0.35 $\mu\text{m}$  [Chen, 1998] and 0.25 $\mu\text{m}$  [Stockinger, 1999] devices. The patterning process for the sidewalls involved the deposition of 200nm of ECR planar oxide. The sidewall spacer patterns were then patterned in negative photoresist with



an alignment step to the e-beam cells alignment marks, followed by a pattern transfer of the resist patterns, by a dry etch process, into the oxide.

With the sidewalls masking the LDD source/drain extensions the source drain implants were performed with arsenic implanted for the n-FET devices at 30keV with dose  $2.5 \times 10^{15} \text{cm}^{-2}$  and  $\text{BF}_2$  implanted for the p-FET devices at 30keV with dose  $2.5 \times 10^{15} \text{cm}^{-2}$ .

### 6.2.5 Contact formation

After formation of the device junctions, the wafer was to be covered with a dielectric into which the contact holes were to be etched prior to the deposition of the metal layer. The material used for this process was a 250nm deposited layer of ECR oxide. A CVD deposited BPSG layer was not necessary for this application as only a single layer of metal was to be used on the interconnect level and the topography of the wafer, with only sixteen devices per chip site, was smooth enough to not require a dielectric smoothed with a reflow step. After deposition of the oxide the junction implants were activated with a low temperature regrowth anneal at 600°C for 30 minutes in a nitrogen ambient atmosphere, followed by a rapid thermal anneal at 950°C for 10 seconds. Contact holes were then patterned with the characterised positive photoresist process. The contact holes were etched through the dielectric layer with a RIE process.

### 6.2.6 Metalization

The patterning of the metal layer of the devices required a two step process with the metal within the e-beam cell patterned with an electron beam lithography process and the metal in the outer probe pad area defined with an optical lithography process.

Firstly a 500nm thick layer of metal was deposited on the insulator, followed by a 250nm thick layer of deposited ECR planar oxide. The e-beam cell area was patterned using the negative resist as a mask and the pattern was transferred through to the oxide. After the resist was stripped an optical lithography process using a positive resist with a light field mask was used to leave a masking layer of resist in

the outer probe pad area, the patterned oxide layer provided masking for the inner e-beam area. A defined overlap of 5 $\mu$ m ensured that the two levels connected to produce a continuous mask. The metal was etched with a RIE process and then sintered at 435°C in a H<sub>2</sub>/N<sub>2</sub> atmosphere for 10 minutes.

### **6.3 Summary**

This chapter has described the processes that have been characterised for the processing of the MOSFET devices. The negative resist AZ PN 114 has been characterised to dimensions of 72nm and the process to transfer the resist pattern into polysilicon has been demonstrated. Also, the positive resist AZ PF 514 has been characterised to pattern contacts to dimensions of 120nm.

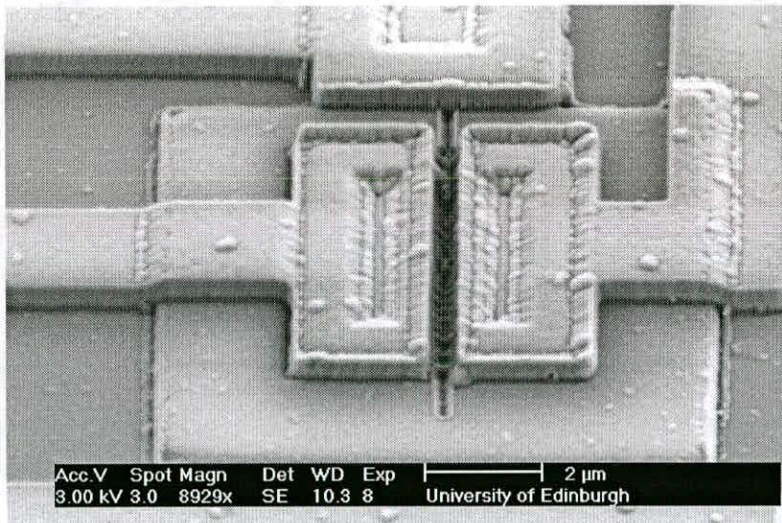


## Device Results

The results obtained from the analysis of the fabricated MOS devices are presented in this section. Analysis of the device structure is displayed and electrical results of devices with various gate lengths are presented. Also included is an investigation into the operating characteristics of n-MOSFETs after sectioning with a focused ion beam (FIB).

### 7.1 Device Structure

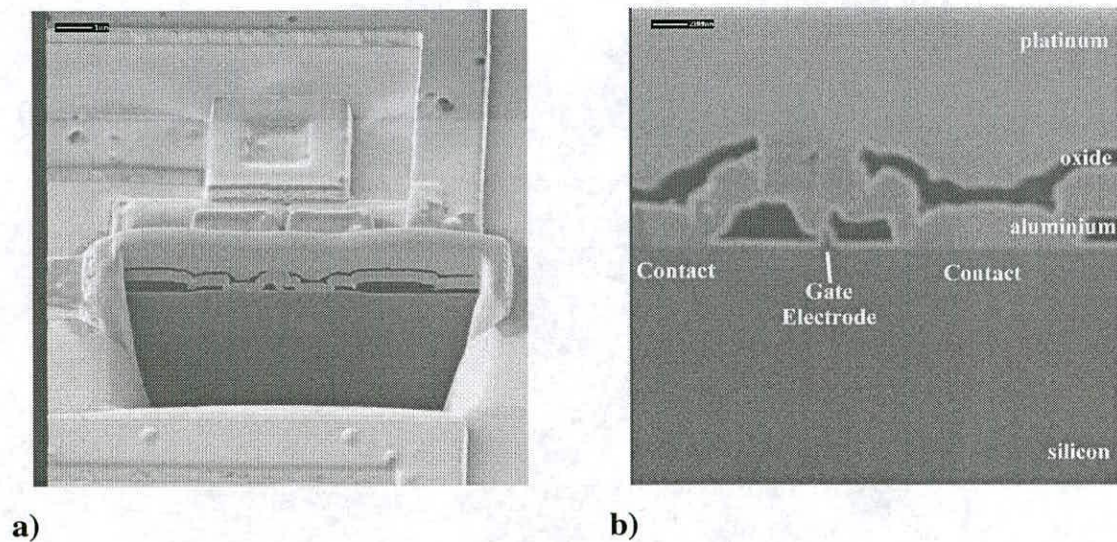
The structure of a fabricated nMOSFET is shown in the SEM image of figure 7.1. The device is designed with a gate length of 100nm and contact lengths of 500nm. The gate contact is located at the top of the picture with the gate electrode below and between the source/drain junction contacts. The isolation oxide pattern is situated around the perimeter of the device and is visible as a raised section.



**Figure 7.1** SEM image of a fabricated n-MOSFET



A cross-sectional image of a MOSFET is displayed in the FIB image of figure 7.2. The image is across the middle of the device with the 80nm gate electrode visible between the two 1 $\mu$ m contacts. The platinum was deposited on the device to produce a clear image after the removal of material by the ion beam. The magnified image of the device highlights removal of the isolation oxide above the gate electrode. This removal of material was thought to have occurred during the metal etch process as the trench is located centrally between the edges of the metal for the contacts. The gate alignment is within 100nm of the centre of the contacts, which represents an alignment accuracy to within two patterning pixels from the electron beam lithography system.



**Figure 7.2** FIB cross-sections of a nMOSFET device: a) Overview of device, b) Magnified view

## 7.2 Electrical Characterisation

Electrical measurements of the nMOS devices were made using a Hewlett Packard HP4156 semiconductor parameter analyser. Connections for each measurement were made manually using a Wentworth manual probing station.

The devices used for characterisation were the electron beam lithography defined nMOS devices fabricated in the EMF at the University of Edinburgh. The fabrication



process is described in section 6.2 and the processing sequence is shown in appendix A. Devices with four different gate length of 1 $\mu$ m, 0.5 $\mu$ m, 0.25 $\mu$ m and 0.1 $\mu$ m were characterised and their respective dimensions are displayed in table 7.1:

Nominal Gate length ( $\mu$ m)	1.0	0.5	0.25	0.1
Contact length ( $\mu$ m)	0.5	1.0	0.5	1.0
Active area width ( $\mu$ m)	6	6	6	6

Table 7.1            Dimensions of the characterised NMOS transistors

Three curves were plotted for each device:

- Current-voltage output curves
- Subthreshold curves
- Turn-on curves

7.2.1 I-V output curves

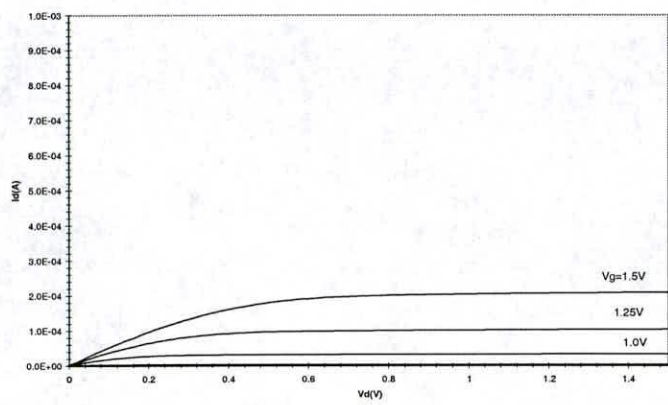
Figure 7.3 shows the I-V curves for the four devices. The trend of the curves, as the gate length of the devices is reduced, is an increase in the drain current for a constant gate voltage. The magnitude of the rise is consistent with the linear increase that is modelled by the drain current equation, 2.1. To enable comparison between the devices the transconductance ( $g_m$ ) and output conductance ( $g_d$ ) were calculated from a pre-defined measurement point. A drain voltage of 1V for  $V_G=1.5$  and 1.25V were used to calculate  $g_m$  and the range  $V_D=1.0-1.5V$  at a gate voltage of 1.5V was used to calculate  $g_d$ .

The 1 $\mu$ m and 0.5 $\mu$ m devices, in figures 7.3a and b, show good long channel operating characteristics, shown with low  $g_d$  values of 1.3mS/mm and 5mS/mm for the 1 $\mu$ m and 0.5 $\mu$ m device respectively. The transconductance for the respective devices is 69mS/mm and 94mS/mm, which indicate a voltage gain, ( $A_v$ ) of 53 for the 1 $\mu$ m device and 19for the 0.5 $\mu$ m device.

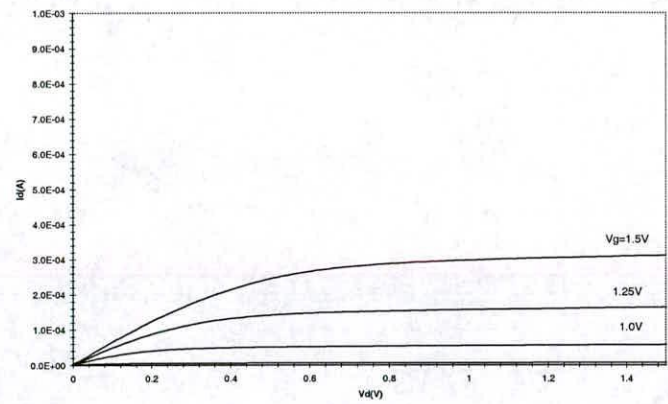
The 0.25 $\mu$ m device exhibits quasi long channel behaviour. The output current is significantly increased, with the reduction in the gate length. At  $V_D=V_G=1.5V$ , the

output current has increased from 0.31mA for the 0.5μm device to 0.84mA with the 0.25μm device. The transconductance has also significantly increased to 164mS/mm. A  $g_d$  value of 28mS/mm gives a voltage gain of 6 for the device. Severe short channel effects of punchthrough and velocity saturation are not evident in the device.

The 0.1 μm device is punched through for all values of drain voltage, with the gate voltage having little effect on the output current. The output current has a strong dependence on the drain voltage with little differentiation between the linear and saturation regions of operation for the device.

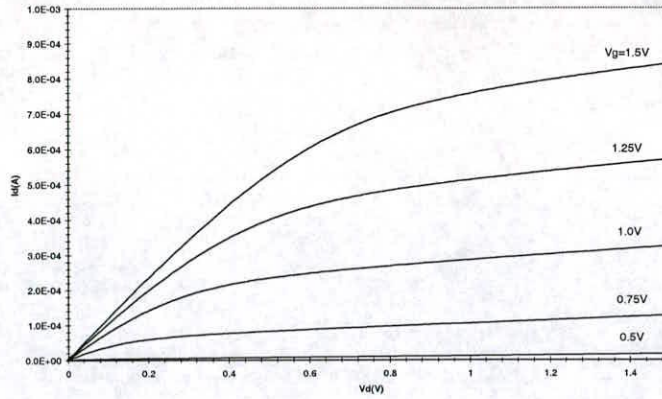


a)

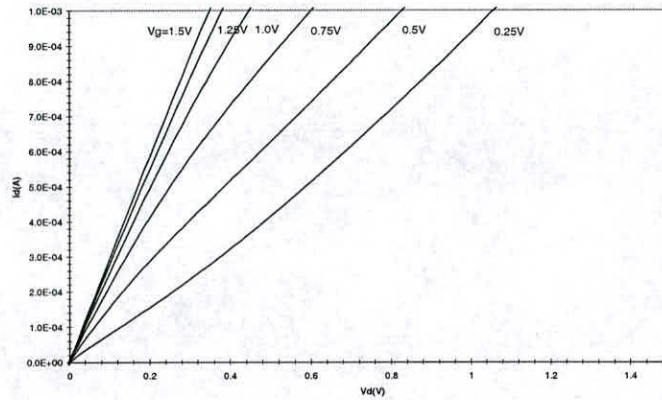


b)





c)



d)

**Figure 7.3** I-V curves for devices with gate lengths: a)  $1\mu\text{m}$ , b)  $0.5\mu\text{m}$ , c)  $0.25\mu\text{m}$ , d)  $0.1\mu\text{m}$

### 7.2.2 Subthreshold curves

The subthreshold curves for the devices were obtained for the drain voltages of 0.25, 0.5 and 0.75 volts. The resulting curves for the four devices are shown in figure 7.4. These curves indicate how effectively the transistor can be turned off as  $V_G$  falls below  $V_T$ . The rapid reduction of  $I_D$  below threshold indicates that the transistor is turning off quickly and is represented with a low value of subthreshold swing,  $S_t$ . A transistor that exhibits a gradual reduction in  $I_D$  indicates the onset of punchthrough in the device and has a larger value of  $S_t$ .

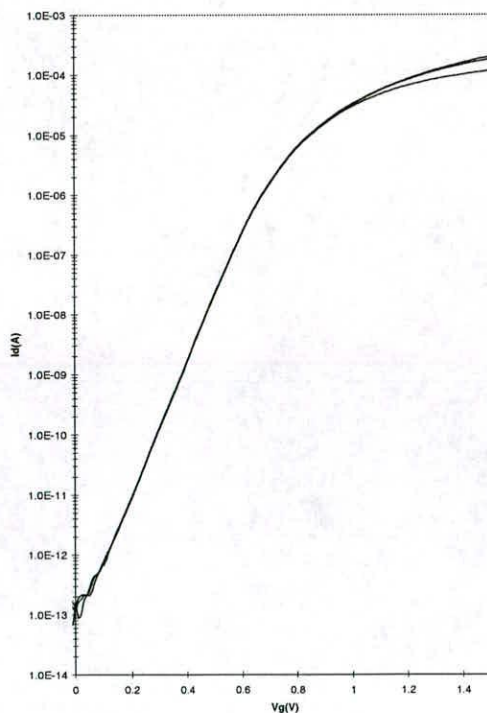
The subthreshold curve for the  $1\mu\text{m}$  device indicates long channel behaviour with a steep roll-off current when the gate voltage is less than  $V_T$ . The value of  $S_t$  at

90mV/decade, is independent of the drain voltage, which indicates the absence of a punchthrough component. The transistor also has a very low current of 100fA when the transistor is switched off with  $V_G=0V$ .

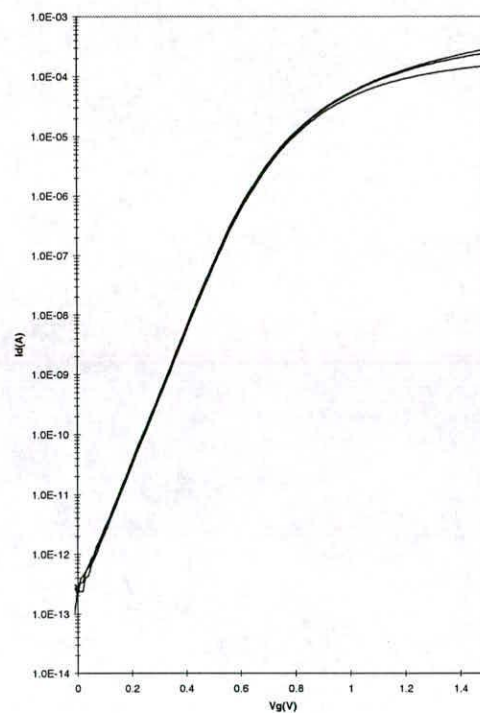
The 0.5 $\mu$ m device exhibits the same long channel behaviour as the previously described 1 $\mu$ m device. The subthreshold slope is 88mV/decade and  $I_D$  at  $V_G=0V$  is 220fA.

The 0.25 $\mu$ m device shows good turn-off characteristics with a low value of  $S_t$  at 98mV/decade. There is a slight shift in the curves with increasing  $V_D$  values, indicating a slight reduction in  $V_T$ . The current under weak inversion is 75pA at  $V_G=0V$  and  $V_D=250mV$ .

The 0.1 $\mu$ m device exhibits severe punchthrough, with the gate having little control over the drain current. With no gate voltage applied to the transistor, the value of  $I_D$  is high at 98 $\mu$ A. The significant change in  $I_D$  with increasing  $V_D$  indicates that punchthrough is dominating the output current.

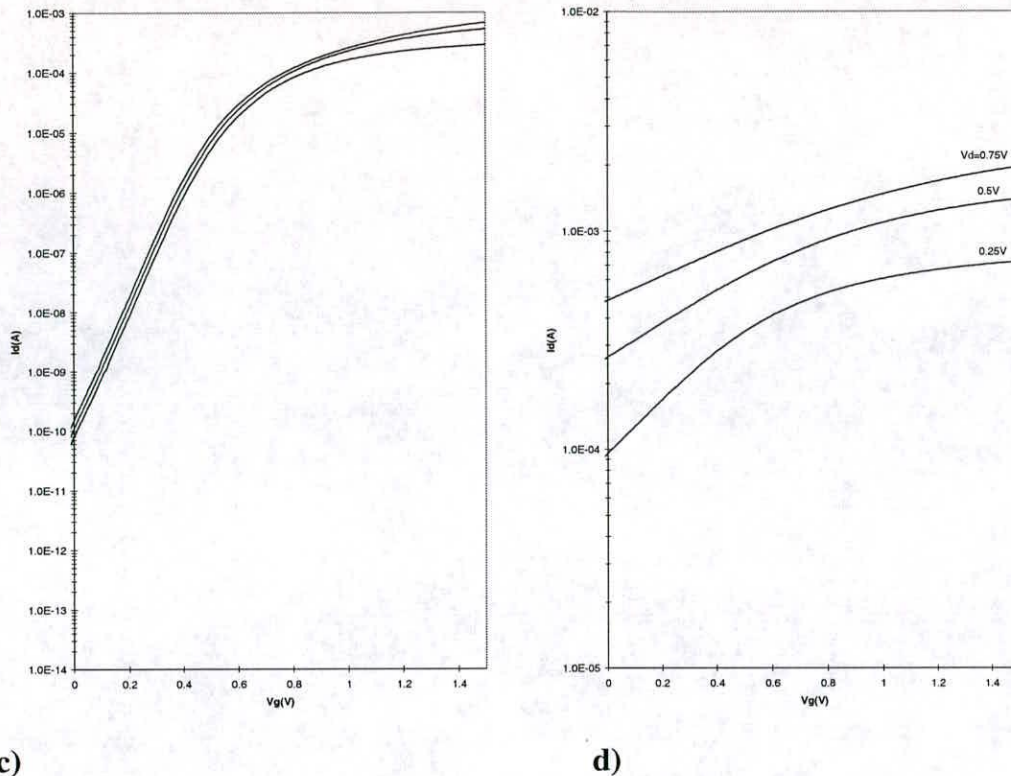


a)



b)



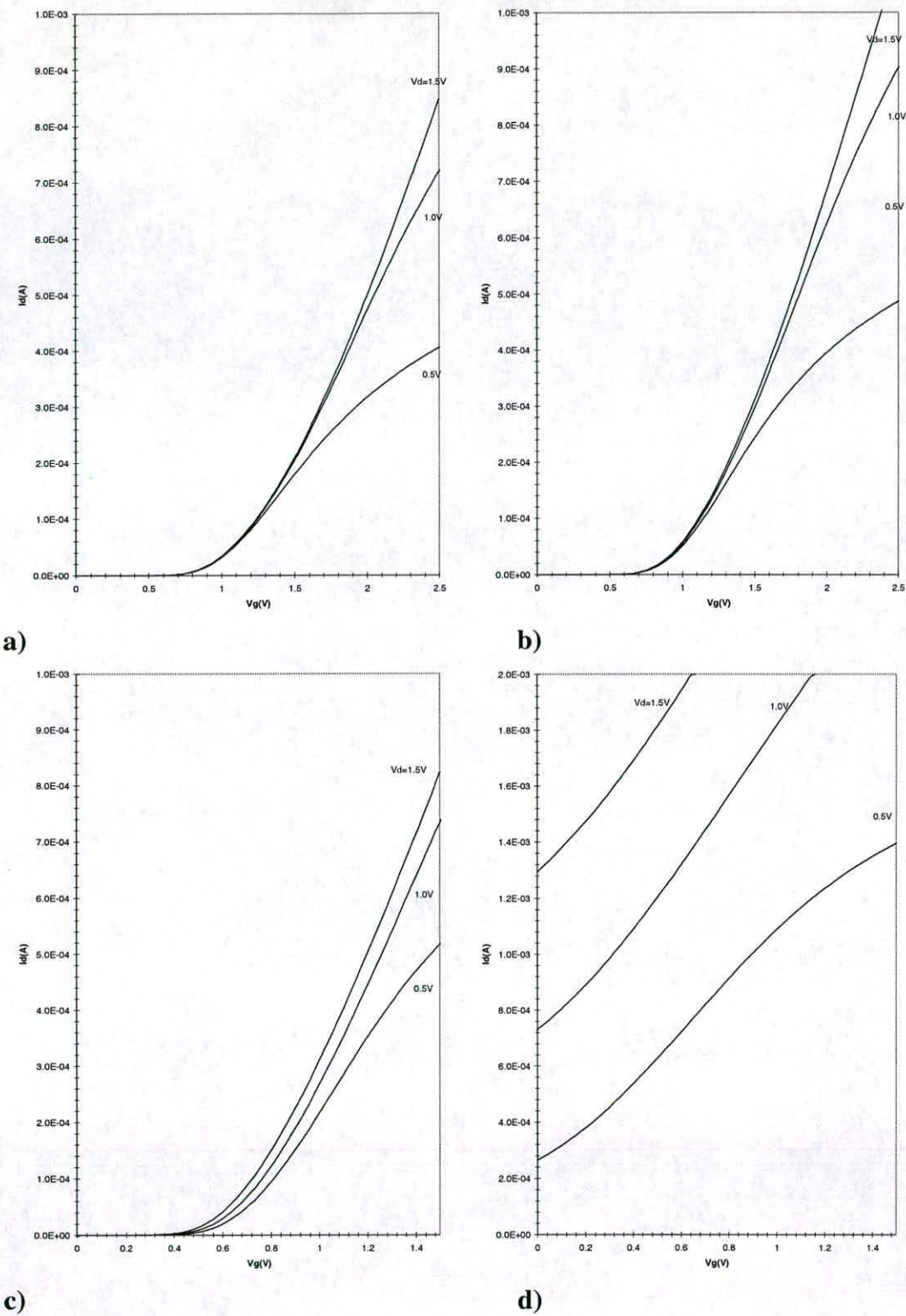


**Figure 7.4** Subthreshold curves for devices with gate lengths: a)  $1\mu\text{m}$ , b)  $0.5\mu\text{m}$ , c)  $0.25\mu\text{m}$ , d)  $0.1\mu\text{m}$

### 7.2.3 Turn-on curves

The turn on curves, shown in figure 7.5, plot  $I_D$  against  $V_G$  on a linear axis. These are used to indicate the gate voltage at which the transistor enters strong inversion, i.e. the voltage where the threshold voltage has been exceeded. The curves indicate a general trend of decreasing threshold voltage with reduction in gate lengths, to the point where the  $0.1\mu\text{m}$  transistor is effectively in strong inversion for all values of gate voltage.

As the drain voltage is reduced the value of  $V_T$  remains almost constant for the  $1\mu\text{m}$  and  $0.5\mu\text{m}$  devices, indicating good long channel behaviour. The separation of the curves for the  $0.25\mu\text{m}$  device indicates a gradual shift in  $V_T$  as the drain voltage is increased, indicating slight onset of short channel effects. The shift is further exaggerated in the  $0.1\mu\text{m}$  device, with wide separation of the curves.



**Figure 7.5** Turn on curves for devices with gate lengths: a)  $1\mu\text{m}$ , b)  $0.5\mu\text{m}$ , c)  $0.25\mu\text{m}$ , d)  $0.1\mu\text{m}$



#### **7.2.4 Characterisation summary**

The devices presented in this section are from the first batch of wafers fabricated using the EEELS. The results show good long channel transistor operation for all but the smallest devices, providing a good basis for future experiments using this design approach. With the devices measured and characterised a study was carried out, using these devices, in conjunction with a focused ion beam system.

### **7.3 Focused Ion Beam Width Modification of Transistors**

Focused ion beams have recently become widely used in the analysis and modification of ULSI circuits. The systems can be used to remove small amounts of material from a defined area of a circuit to allow cross-sectional analysis of the internal structure of the circuit. Another common use is to change the topography of circuits by modifying the metal interconnects with a cutting and re-strapping technique of the metal tracks. Novel implantation techniques have also been demonstrated, using the gallium beam to produce localised doping of the channel region with a p+ implant [Shen 1998].

Focused Ion Beam systems have not to date, however, been used to demonstrate the modification of the internal structure of silicon MOS devices and the effects of such modification on the devices electrical characteristics. Such modification of transistors would allow the characteristics of a fabricated circuit to be adjusted by designers by modifying individual transistors within the circuit without re-fabrication.

This section describes the results of a preliminary study into the effects of FIB width modification on the electrical characteristics of nMOS transistors.

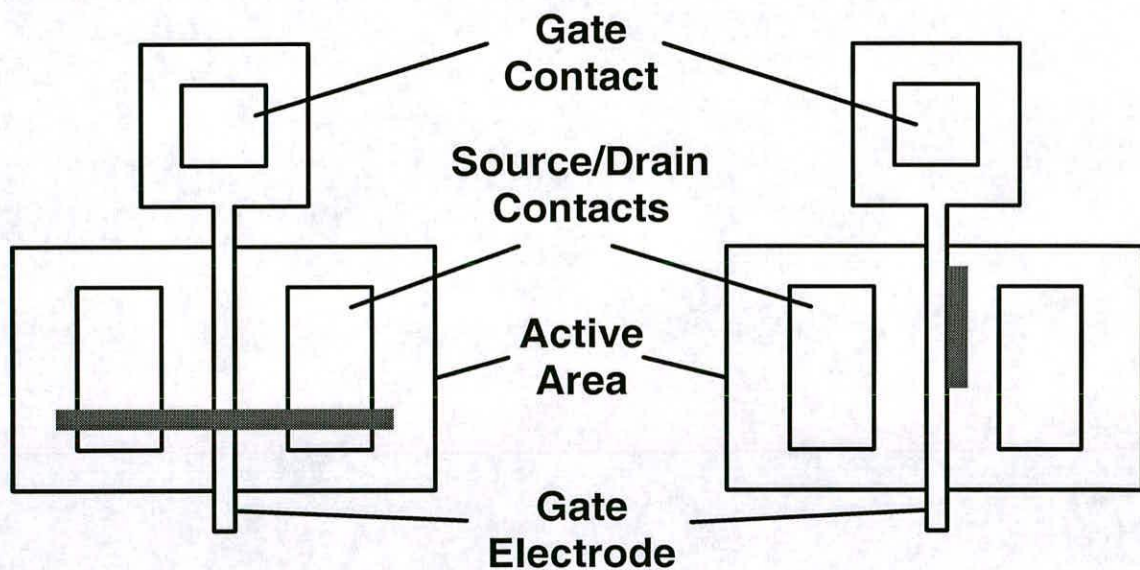
#### **7.3.1 Transistor modification strategy**

The devices used for modification with the FIB were the electron beam lithography defined nMOS devices that were from the batch of devices describes in section 7.2.

Transistors with gate lengths of  $0.25\mu\text{m}$  and  $0.5\mu\text{m}$  were modified as they represent the dimensions of industrially manufactured devices.

A FIB 200 system manufactured by FEI was used to modify the MOS devices. The system utilises a  $30\text{keV}$  gallium ion beam and material etches were performed with beam currents of  $70\text{pA}$ . An iodine etch enhancement facility was also used to minimise the re-deposition of material that had been etched.

The transistors were modified to adjust the devices effective electrical width. This was demonstrated using two different techniques, shown in figure 7.6. The first strategy, shown in figure 7.6a, was a lateral cut across the length of the gate, thus reducing the width of the transistor by effectively reducing the size of the devices active area. Figure 7.6b shows the second strategy an orthogonal cut up the width of the device, thus reducing the width in only one junction of the transistor. This technique investigates the effect of material removal in the source and drain regions of a transistor.



**Figure 7.6** Modification strategy of transistors, a) Lengthways cut across the gate, b) Vertical cuts up the width of the device.

A focused beam of ions is a useful technique to implement this strategy as small areas of material (e.g.  $1\mu\text{m}\times 0.25\mu\text{m}$ ) can be removed from a device with a positional accuracy of a few nanometers.



7.3.2 FIB removal of material (0.5μm devices)

Three transistors with gate lengths of 0.5μm were modified with lateral and orthogonal cuts using the FIB system. The dimensions of the devices are listed in table 7.2.

	T1	T2	T3
Gate length (μm)	0.5	0.5	0.5
Contact length (μm)	0.5	1.0	1.0
Active area width (μm)	6	6	6

Table 7.2          Dimensions of transistors modified using FIB system

Lateral cut

Two transistors were modified with a lateral cut, T1 and T2. The first, T1, was cut across the whole active area, shown in figure 7.7a. The effective active area after the cut was reduced to ~5μm. A cut on the second device, T2 shown in figure 7.7b, removed a smaller amount of material, cutting across the gate of the device and into approximately 0.5μm of the source/drain regions. The active area of the device was effectively reduced to ~3μm.

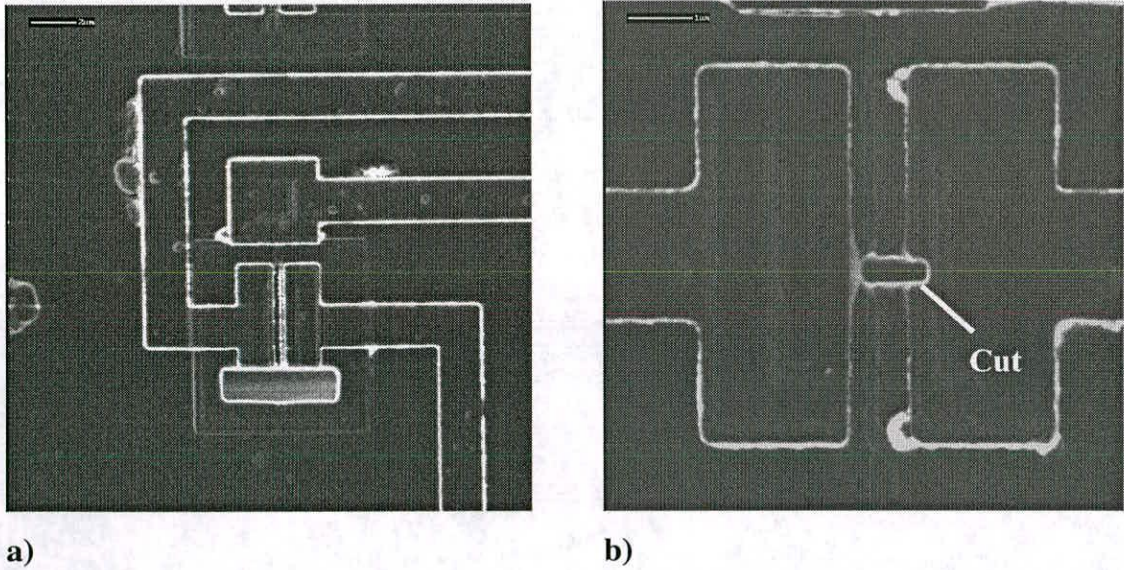
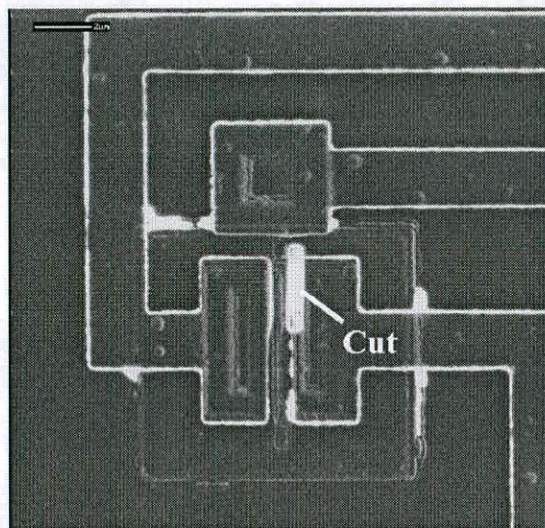


Figure 7.7          Lateral FIB cuts across transistors: a) T1 b)T2.

### Orthogonal cut

The orthogonal cut was performed on transistor T3. The cut ran up the width of the active area and was positioned to be just adjacent to the gate electrode. The cut was performed at the top of the active area, near the gate contact. The post-cut image of transistor T3 is shown in figure 7.8.



**Figure 7.8**      **Orthogonal FIB cut in transistor T3**



7.3.3 Electrical results (0.5μm devices)

Lateral cut

The subthreshold curves for transistors T1 and T2 are displayed in figure 7.9. The characteristics of the devices in the subthreshold region have been maintained after the FIB cut across the device. The subthreshold slope remains constant at 94mV/decade for T1 and 88mV/decade for T2. The cut does however increase the leakage current for gate voltages below 0.4V. It can be seen from fig 7.9 that T1 and T2 show a constant leakage of 1.4nA for gate voltages below 0.4V. The constant current that is produced at the low values of  $V_G$  is probably influenced by a leakage path, either between the drain to the substrate or across the face of the cut connecting the junction regions.

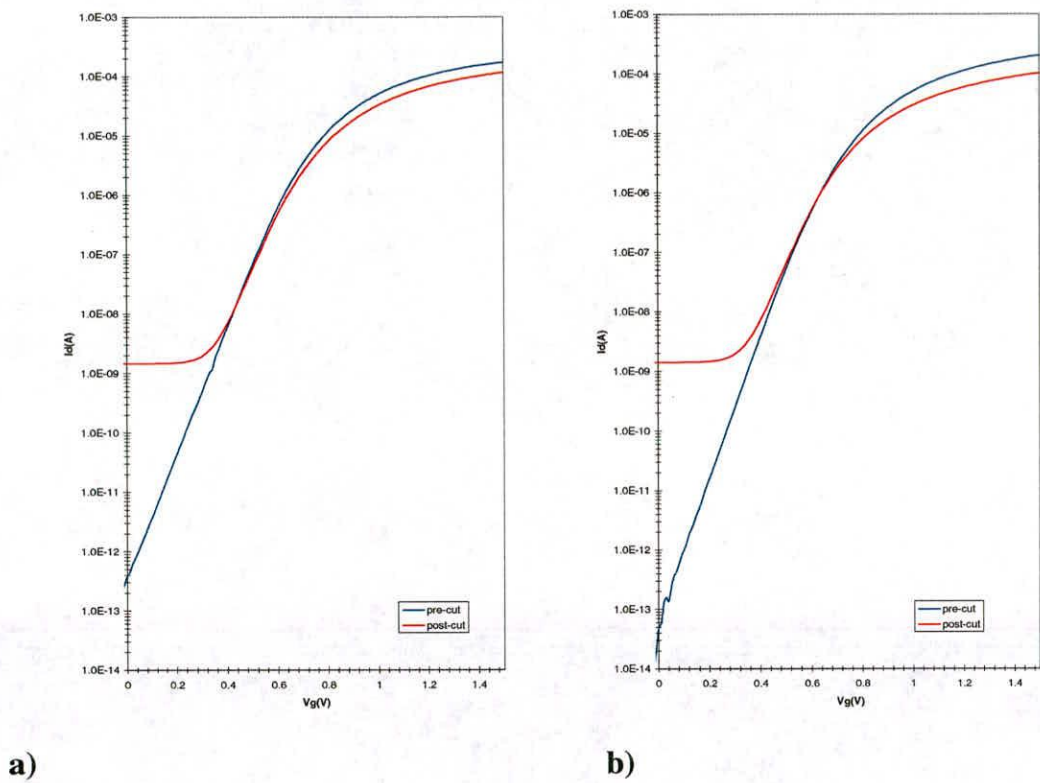
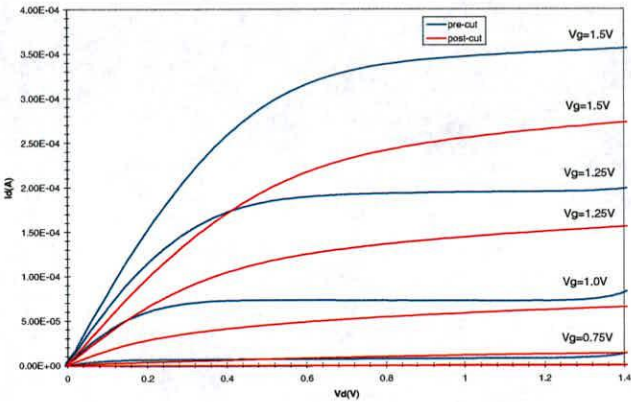


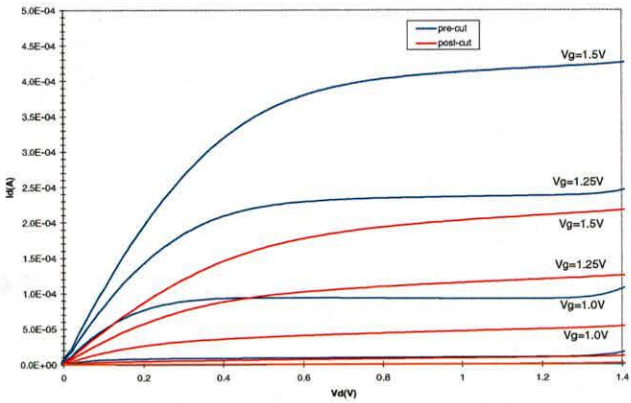
Figure 7.9 Subthreshold curves for: a) T1 b) T2

The current-voltage curves for the devices are shown in figure 7.10. The I-V characteristics exhibit a reduction in  $I_D$ , that is expected as the width of the active area is reduced. The magnitude of the reduction in drive current approximately

corresponds to the ratio of the width reduction for the two devices. The reductions of 17% and 50% in the device widths for T1 and T2 resulted in 25% and 52% drops in  $I_D$ . When operating in saturation the devices exhibit a constant rise in  $I_D$ , this is most probably due to the resistive leakage path caused by the FIB cut, also demonstrated in the subthreshold characteristics.



a)



b)

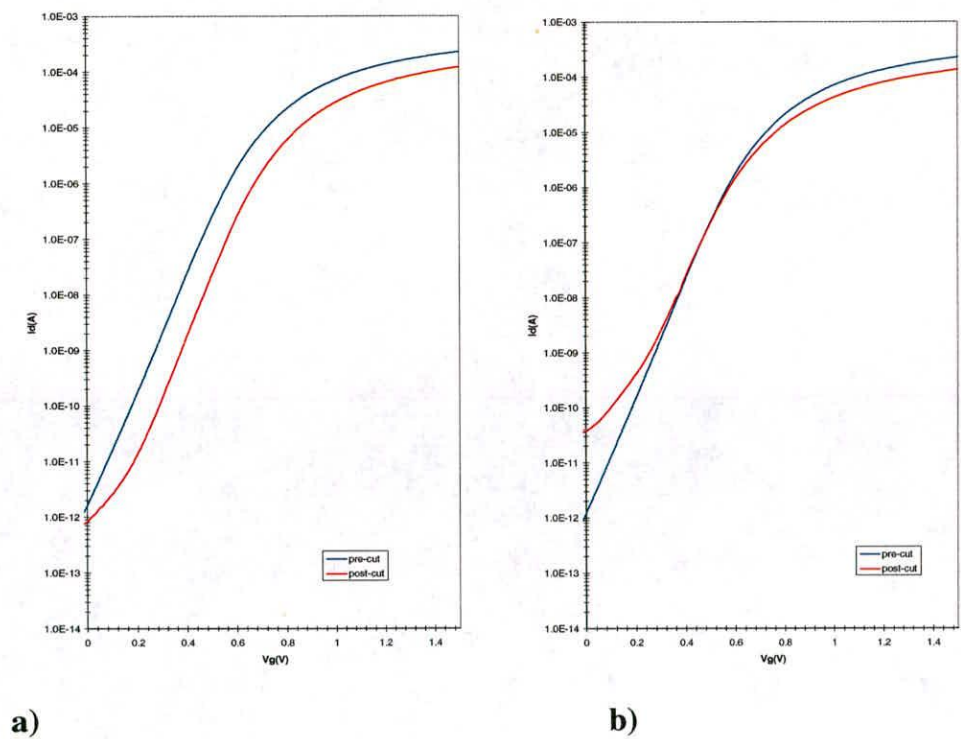
Figure 7.10 Current-voltage characteristics for: a) T1 b) T2



### Orthogonal cut

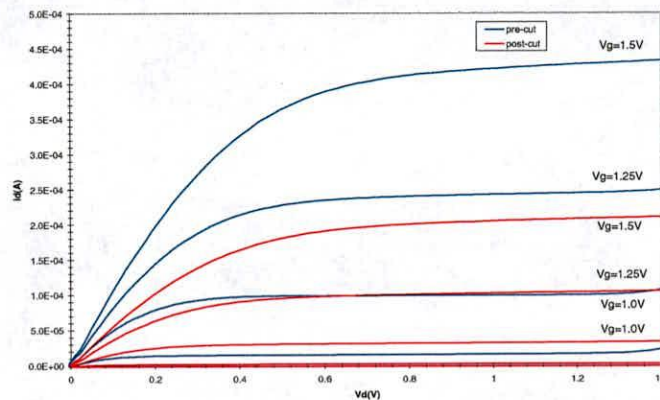
The electrical analysis on device T3 changed the connection of the source and drain contact to produce results that incorporated the orthogonal FIB cut in first the source and then the drain junction region. The results with the cut in the source region are referred to as the forward connected device, and with the cut in the drain junction region as the reverse connected device.

The subthreshold curves are shown in figure 7.11. The characteristics of the device for both forward and reverse connections are similar with a subthreshold slope in each case of 90mV/decade. With the device connected in the forward direction, there is no increase in the leakage of the subthreshold current with the curve maintaining its characteristics. The positioning of the curve is, however, shifted to the right, indicating an increase in the devices threshold voltage. When connected in the reverse direction the device exhibits increased leakage, although the level of which is not constant, as for the lateral cut. Also the leakage when  $V_G=0V$  is lower than for the lateral cut, at 39pA.

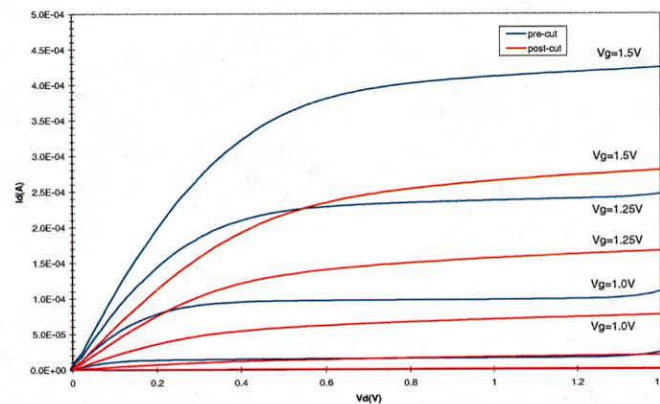


**Figure 7.11** Subthreshold characteristics for device T3: a) forward connection, b) reverse connection

The current-voltage curves shown in figure 7.12 also exhibit different characteristics in the forward and reverse connected device. The magnitude of the drive current is reduced by different margins for each of the connections, as would be expected. The reduction in  $I_D$  was 48% in the forward direction and 62% in the reverse direction and the cut covered 43% of the active area down the width of the device. The forward connected device also exhibited less increase in  $I_D$  when the device was operated in the saturation region.



a)



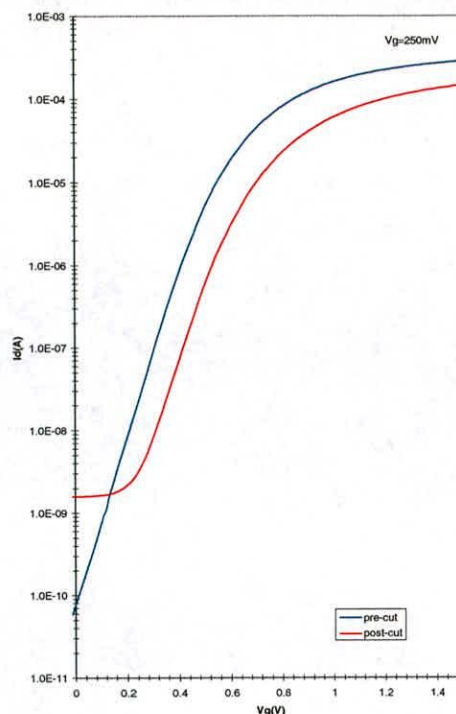
b)

**Figure 7.12** Current-voltage characteristics for device T3: a) forward connection, b) reverse connection

### 7.3.4 FIB removal of material (0.25 $\mu$ m device)

One device with a gate length of 0.25 $\mu$ m, transistor T4, was modified with a lateral FIB cut across the gate of the transistor. The structure of the device after the cut had been performed is shown in figure 7.13. The position of the cut effectively reduced

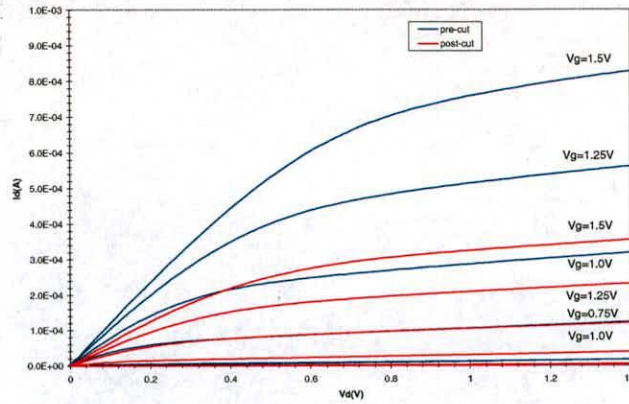




**Figure 7.14** Subthreshold curves for transistor T4

The I-V curves of the device are shown in figure 7.15. The decrease seen in the output current between the two cuts is in the same ratio as the reduction in width of the devices active area, as was seen with the 0.5 $\mu$ m devices. The active area was reduced by approximately 50% with the FIB cut and the output current decreased by 52%.

The short channel effects seen in the curves of the pre-cut measurements do not appear to be greatly exaggerated by the FIB cut in the device. The drain conductance value remains almost constant at 28mS/mm before the FIB cut to approximately 25mS/mm after the cut. The drain conductance value after the cut is only an approximation because of the measurement of the active area width after the FIB cut.



**Figure 7.15** Current-Voltage characteristics for transistor T4

## 7.4 Summary

The electrical characteristics of nMOS transistors fabricated by electron beam lithography have been demonstrated. The devices with gate lengths of  $1\mu\text{m}$  and  $0.5\mu\text{m}$  display good long channel characteristics, while the  $0.25\mu\text{m}$  devices only show the onset of short channel behaviour, with an increase in the output conductance due to channel modulation effects. The shortest channel  $0.1\mu\text{m}$  device exhibited severe punchthrough, limiting the control of the output characteristics with the gate voltage.

Devices with industrially relevant sizes have been modified with a focused ion beam to investigate techniques in post fabrication adjustment of MOSFET electrical characteristics. Reducing the width of the active area with a lateral cut across the length of the gate maintained the subthreshold characteristics of the device, but also introduced a constant leakage current under very weak inversion of approximately  $1\text{nA}$ . Reduction in the width of the devices active area, with the FIB cut, was found to result in a comparable reduction in  $I_D$ .

Investigation of the position of the cut in the source and drain junction regions indicated that there was no increase in the subthreshold current when the cut was



positioned in the source region of the device. A leakage current was shown, however, when a cut was made in the drain region of the device.

---

## Conclusions

---

This thesis has reported on the development of a nanotechnology research capability based around electron beam lithography, and its application to the fabrication of nanoscale MOS transistors. This chapter summarises the research carried out, highlighting the key achievements and concludes with a discussion of future directions for this research.

With the aim of investigating electron beam lithography for the fabrication of silicon devices, a system has been designed and constructed based around a high resolution scanning electron microscope. Patterning processes have been characterised using the system and then applied to a device fabrication experiment. The resulting MOS transistors have been electrically characterised and used to explore a new chip modification strategy using focused ion beam techniques.

This project has produced the following achievements:

- Development of a nanofabrication capability, with construction of a high resolution electron beam lithography system and characterisation of patterning processes.
- Integrated MOS device fabrication, with all device patterning levels performed by electron beam lithography.
- Demonstration of a focused ion beam chip modification strategy for adjusting the electrical characteristics of a MOS device after fabrication.

These three areas are discussed in further detail in the following sections.



## 8.1 Nanofabrication Facility

A high resolution electron beam lithography system has been designed and constructed for use with the electron optical column of a thermal field emission SEM. The unit is fully automated and can automatically align to registration marks, expose a pattern and step to the next exposure site. The system is suitable for the low volume production of small area nanoscale circuits.

Using this e-beam system chemically amplified photoresist technology was investigated. The negative AZ PN 114 and positive AZ PF 514 resists from Hoechst were investigated to determine the processing characteristics of the resists and doses required for high resolution patterning. While the use of these resists is advantageous due to their high sensitivity, their application to all levels of lithography in a device integration experiment has not previously been reported in literature.

The negative resist was found to have a contrast of 4 and a sensitivity  $7.5\mu\text{C}/\text{cm}^2$ . The exposure dose was calibrated for a range of patterns with dimensions from 70nm to 500nm and above. The dose required for the patterns was found to increase as the pattern width reduced. The doses ranged from  $24\mu\text{C}/\text{cm}^2$  for the lines above 500nm, to  $90\mu\text{C}/\text{cm}^2$  for the 70nm lines. The positive resist was characterised for patterning of the contact level of the design. The characterised exposure doses for this resist ranged from  $5\mu\text{C}/\text{cm}^2$  for the  $2\mu\text{m}$  wide patterns, to  $15\mu\text{C}/\text{cm}^2$  for the smallest contact windows which were 120nm wide.

The negative resist process was refined to remove any trace of photoresist residue in the non-exposed areas using a short oxygen dry etch step after the development process. This step had no measurable effect to the dimensions of the developed pattern.

For the critical step of gate electrode formation, an oxide on polysilicon pattern transfer process was characterised to pattern gate electrodes with 70nm lengths. The

resist pattern was initially transferred into an oxide from the resist, which was then used as a mask for a three step patterning process of the polysilicon.

## 8.2 Integrated MOS Device Experiment

MOS devices with gate lengths ranging from 70nm to 1 $\mu$ m have been fabricated. All of the critical patterning levels of active areas, gate electrodes, contact formation and metalization were performed using electron beam lithography. A novel oxide sidewall spacer, also patterned by e-beam lithography, was used as a mask for the junction implants. The novel sidewall spacer demonstrated the ability of the process to control the dimensions of the spacer to investigate new implantation processes, such as asymmetric implants, for nanoscale MOSFETs.

The fabrication process was designed for deep sub-micron devices, to demonstrate the capability of the electron beam system and the characterised lithography processes, that have been described previously. The operation of the transistors demonstrates that further investigation is warranted, to refine the process for the fabrication of optimised nanoscale MOS devices. The exposure of all lithography levels with electron beam lithography would enable investigation of extreme miniaturisation for all features of the device.

Analysis of the electrical characteristics of the fabricated MOS devices, show long channel behaviour for the transistors with dimensions down to 250nm gate lengths. The transconductance for a 250nm device is high at 164mS/mm and an associated voltage gain of 6. The subthreshold slope at these dimensions is 98mV/decade, with a drain off current of 75pA. These very good electrical characteristics confirm successful integration of the electron beam lithography system, chemically amplified resists and pattern transfer techniques. Electrically testable structures have also been fabricated down to 100nm dimensions and polysilicon gate electrodes have been patterned down to 70nm. This confirms that the lithography system is ready for application to further nanoscale devices research.



### 8.3 Focused ion beam modification of MOS devices

A transistor modification strategy has been demonstrated using focused ion beam sectioning techniques. Devices with gate lengths of  $0.5\mu\text{m}$  and  $0.25\mu\text{m}$  were used to demonstrate a process of modifying the electrical characteristics of a MOS transistor, after the fabrication process has been completed. This type of process would be of particular interest to specialised integrated circuit manufacturers, as the characteristics of a circuit could be adjusted and evaluated, without re-fabricating the whole circuit. Two strategies were implemented and involved cutting trenches in the device to remove material from the transistor. The first produced a lateral cut across the length of the device and the second involved orthogonal cuts up the width of the device.

The lateral cut reduces the width of the active area by reducing the active size of the gate electrode. The drive current, of the modified device, was reduced in the same ratio as the reduction in the width of the active area, demonstrating a method of reducing the current drive of fabricated transistors. The electrical characteristics of the modified device, exhibited the same values of subthreshold slope for the pre and post modification device, although there was a slight increase in the subthreshold current under weak inversion.

The orthogonal cut was made primarily to investigate the effect of a FIB cut in the source and drain regions of a transistor. In the source region, the cut increased the threshold voltage, while maintaining the subthreshold characteristics. However, in the drain region the cut introduced a small leakage current when operating in weak inversion, though there was no change in the operating characteristics under strong inversion. The single orthogonal cut up the width of the device also reduced the output current drive of the device, although the reduction was not proportional to the length of the cut in the active area. Also, the current drive was less when the cut was in the drain region of the device as compared to the source region.



## 8.4 Future work

The work presented has covered a wide area, with systems and processes demonstrated for a full device fabrication process. Therefore this study represents an initial investigation into the challenges of nanoscale device fabrication. The techniques developed provide an excellent basis for further investigation of nanoscale structures in silicon.

The processes have been shown to be capable of fabricating structures down to 70nm. From these dimensions it would be possible to use the system to investigate further and optimise MOS transistors to these dimensions. New features could also be included in the fabrication process to take advantage of the nanoscale feature capability in all lithography levels of the device process. Source and drain implantation techniques could be developed with the lithographically defined sidewall spacers. Contact and interconnect schemes for the nanoscale transistor could also be investigated further.

Looking beyond 70nm devices there are opportunities to research novel device features that could be applied to transistors with dimensions in the 10-70nm range. To enable this capability the lithography system could be developed further and the processes, such as photoresist exposure, could be investigated and characterised at these smaller dimensions.

The investigation into focused ion beam cross-sectioning of fabricated transistors has provided an insight of the effects of a FIB cut on the operating characteristics of a transistor. There is, however, a great deal of further investigation possible with this line of research.

With the lateral cut, across the transistor, the relationship between the active area width reduction and the associated decrease in drive current could be characterised. The study would check for a linear relationship between the two factors, as was



indicated in the initial study. The leakage current under weak inversion may be investigated to find the factors that influence the leakage path. The length, area and depth of the cut could be adjusted to determine any effect on the magnitude of the leakage current. Mechanisms to reduce the amount of this leakage current would help maintain the characteristics of the transistor after modification.

The effect of cuts in the junction regions of the device warrants further investigation. The initial study highlighted a contrast in the operating characteristics of the device with the cut performed in each of the junctions. Adjusting the length, area and depth of the cuts in these regions would determine the effect of FIB cuts and indicate optimal methods of sectioning different areas of the device.

The operating parameters of the FIB system may also introduce a variable to the operating characteristics of a sectioned device. The beam current used to etch the section from the device may introduce a variable parameter. Also the use of an enhanced etch facility could adjust the transistors characteristics.

## 8.5 Conclusions

The work carried out has demonstrated the use of electron beam lithography in the fabrication of MOS devices. An electron beam lithography system has been designed and constructed, and the system characterised for use with chemically amplified resists. Pattern transfer techniques have also been characterised for the production of nanoscale gate electrode features for the fabrication of MOSFETs. Devices with nanoscale features have been fabricated and the operation of deep sub-micron devices has been demonstrated.

A novel chip modification technique has been investigated, using a focused ion beam to section deep sub-micron MOSFETs to adjust the transistors electrical characteristics. The technique can be used to reduce the current drive of a fabricated transistor by shortening the width of the devices active area. The modification

process used is only an initial demonstration of the technique, though further studies into the process may lead to a new post fabrication chip modification strategy.



---

# Appendix A

## Device Fabrication Run-sheet

---

Edinburgh Microfabrication Facility

Batch No: 95005

### Optical/E-Beam Defined transistors with 1 $\mu$ m-50nm Gate Lengths

1. Optical Lithography Level 0	alignment marks
2. RIE silicon	Si depth 1 $\mu$ m
3. Photoresist strip	
4. Grow LOCOS buffer oxide	thickness 20nm
5. Deposit Si <sub>3</sub> N <sub>4</sub>	thickness 50nm
6. E-Beam level 1	active area
7. O <sub>2</sub> Plasma etch	time 5s
8. RIE nitride	
9. Field ion implant	
nFET Boron	4e12cm <sup>-2</sup> @ 50keV
pFET Phosphorous	2e12cm <sup>-2</sup> @ 50keV
10.Photoresist strip	
11.E-Beam level 1a	frame
12.RIE oxide and Si	Oxide depth 250nm
	Si depth 250nm
13.Photoresist strip	
14.Strip back oxi-nitride, HF dip	15s 4:1 buffered HF
15.Nitride strip	
16.Etch buffer oxide	
17.RCA clean	

18. Grow sacrificial oxide	thickness 5nm temp 785°C
19. Channel implant	
nFET Boron	$5 \times 10^{12} \text{cm}^{-2}$ @ 20keV
nFET Boron	$5 \times 10^{12} \text{cm}^{-2}$ @ 60keV
pFET Phosphorous	$4 \times 10^{12} \text{cm}^{-2}$ @ 100keV
20. Remove sacrificial oxide	
21. RCA clean	
22. Grow gate oxide	thickness 4.5-5nm
23. Polysilicon deposition	thickness 150nm
24. Polysilicon ion implantation	
nFET Phosphorous	$1 \times 10^{15} \text{cm}^{-2}$ @ 10keV
pFET Boron	$2 \times 10^{15} \text{cm}^{-2}$ @ 10keV
25. Polysilicon anneal	850°C for 15min in $\text{N}_2$
26. ECR oxide deposition	thickness 75-80nm
27. E-Beam level 2	polysilicon
28. $\text{O}_2$ Plasma etch	time 5s
29. Oxide etch	RIE
30. $\text{O}_2$ Plasma etch	time 2min
31. Ion implanted S/D extensions	depth 50nm
nFET Arsenic	$2.5 \times 10^{14} \text{cm}^{-2}$ @ 20keV
pFET No processing	
32. Field oxide RIE	
33. Photoresist strip	
34. ECR oxide deposition	thickness 200nm
35. E-beam lithography level 3	sidewall spacer
36. Oxide etch	RIE
37. Photoresist strip	
38. Ion implantation of S/D	depth 100nm
nFET Arsenic	$2.5 \times 10^{15} \text{cm}^{-2}$ @ 30keV
pFET $\text{BF}_2$	$2.5 \times 10^{15} \text{cm}^{-2}$ @ 30keV



39.ECR oxide deposition	thickness 250nm
40.Low temperature regrowth	600°C for 30min in N <sub>2</sub>
41.Rapid thermal anneal	950°C for 10s in N <sub>2</sub>
42.E-beam level 4	contacts
43.Contact RIE	
44.Photoresist strip	
45.Pre-metal clean	
46.Metal deposition	500nm of Al
47.ECR oxide deposition	250nm
48.E-beam level 5	metal
49.Oxide etch	RIE
50.Photoresist strip	
51.Optical lithography level 5b	metal fanout
52.Metal etch	
53.Photoresist strip	
54.Sinter metal	temperature 435°C

---

## Appendix B

## Publications

---

*David W. Travis, Clive M. Reeves, Alan Gundlach, Tom Stevenson, Richard Langford, Alec Ruthven “Fabrication Techniques for Nano Scale MOSFETs Using Electron Beam Lithography”, in Proceeding of PREP99, Manchester 1999.*



# Fabrication Techniques for Nano Scale MOSFETs Using Electron Beam Lithography

David W. Travis, Clive M. Reeves, Alan Gundlach, Tom Stevenson, Richard Langford, Alec Ruthven

**Abstract--** Techniques have been developed for fabrication of 70nm gate length silicon MOSFET's using thermal field emission electron beam lithography in conjunction with chemically amplified resists. The techniques will prove useful for future nano scale device research.

## I. INTRODUCTION

Improvements in lithographic techniques continue to push back the boundaries of feature size in silicon device fabrication. Advanced optical printing, with a KrF excimer laser light source at 248nm, can print down to  $0.18\mu\text{m}$ <sup>[1]</sup>. It is, however, uncertain as to how far this technology can be improved for the resolution demands of future device production. Meanwhile, electron beam lithography has been used for many years as an advanced lithography tool for nanostructure patterning. The high resolution of this lithographic technique is offset by the relatively low wafer throughput, making it unsuitable for commercial scale manufacturing.

In this paper, we report on the use of a newly commissioned electron beam lithography tool based on a Philips XL40 field emission electron column, which offers sub-5nm resolution at 30keV. The paper describes the electron beam system, basic characterization of the system for device fabrication and the processing steps for fabrication of nano-scale devices, in particular the fabrication of gate electrodes with dimensions down to 70nm with fully scaled contacts. Fig. 1. Shows a fabricated MOSFET with a 70nm gate electrode.

## II. ELECTRON BEAM LITHOGRAPHY

A high resolution Philips XL40 FEG SEM was modified for use as a 30keV direct write e-beam system. The beam diameter of the SEM is less than 5nm at 30keV. The system has been designed, built and tested as part of the nano-scale MOSFET project. A sequential vector scan technique is implemented for the patterning of rectangular shapes by the beam into photoresist. The patterns for the various

fabrication layers of the MOSFET's are defined using Cadence software and then converted into a format

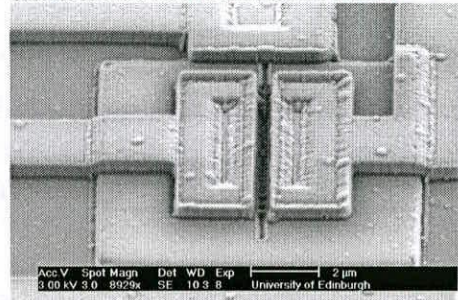


Fig.1. Scanning electron micrograph of a MOSFET with 70nm gate electrode and 1μm contacts.

to be read by the electron beam system. The resolution of the system is determined by the beam spot size in combination with the pixel pitch. A 12-bit bus architecture is used, providing a maximum of 4096 pixels in both the X and Y scan directions. At a patterning magnification of 230x, a pixel pitch of 50nm and a field size of  $200\mu\text{m} \times 200\mu\text{m}$  is achieved.

Each of the subsequent patterning levels required for device fabrication are aligned within the exposure field by using video capture of four alignment crosses, which are located at each of the four corners of the exposure field. A center point detection algorithm is performed on the image of each cross to determine the degree of mis-alignment of the field. Any mis-alignment in the system is then compensated for by adjusting the size of the patterning field with a combination of a stretch, rotate or skew transformation of the pattern data. All of the alignment and patterning procedures are performed automatically by computer control, allowing the system to automatically expose a whole series of chip patterns by step and repeat patterning.

## III. BASIC CHARACTERIZATION OF THE ELECTRON BEAM LITHOGRAPHY SYSTEM

The authors are with the University of Edinburgh at the Edinburgh Microfabrication Facility and MIAC, Edinburgh, EH9 3JL.



Before processing commenced on the fabrication of the MOS devices, basic characterization of the system was performed to optimize the resist processes for nano scale patterning. The negative AZ PN 114 and positive AZ PF 514 chemically amplified resist systems from Hoechst were used in the patterning process. Research by Macintyre and Rangelow<sup>[2],[3]</sup> has investigated the high resolution properties of the resists and from this processes were optimized for use with Hoechst AZ 1500 thinner and Shipley MF319 developer.

Pattern exposure dosage was determined by performing exposures with a multi-featured test pattern. The patterns contained several features of various linewidths and box sizes. The patterns were all repeated with an increasing exposure dose to provide a matrix of features exposed with an array of doses. From these tests, the correct dose for a specifically sized pattern could be determined for exposure in the MOSFET fabrication process.

After development of the patterns in photoresist, a small amount of residue was visible around the base of the patterns. This was especially visible in the patterns from the negative resist. It was thought that this residue may cause a widening effect in the patterns transferred from the resist in the fabrication process. In order to remove this effect the resist patterns were exposed to a short, 10s, O<sub>2</sub> plasma etch. This removed all traces of the residue without affecting the profile of the exposed patterns. Fig. 2. Shows the cross-section of a 72nm line of resist.



Fig.2. Cross section of a 72nm line of negative photoresist.

#### IV. MOSFET PROCESSING STEPS

Fig. 3. shows a schematic cross section of a MOSFET device. The processing for nFET devices firstly involved the electron beam definition of the active areas, followed by a conventional local oxidation of silicon (LOCOS) isolation. A 5nm gate oxide was thermally grown with a dry-oxidation process at 785°C for 15min. The sub 100nm

gate electrodes were then fabricated (described in section IV A). After a shallow LDD implant of As with dose  $2.5 \times 10^{14} \text{cm}^{-2}$  @ 20keV an aligned sidewall spacer was defined with electron beam lithography. The source/drain junctions were then implanted with a deeper As implant of

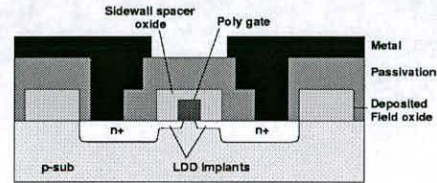


Fig. 3. Schematic cross section of an MOSFET.

dose  $2.5 \times 10^{15} \text{cm}^{-2}$  @ 30keV. Contact holes were then etched in the deposited insulating oxide (described in section IV B). The lithography for the metal interconnect level was performed with a combined e-beam/optical lithography process. The inner  $200 \times 200 \mu\text{m}$  field, to contact the devices, was defined by a e-beam process. Then a optical process defined a larger outer field that contained the probe pads, to enable electrical testing of the devices. The two field were aligned together using a common alignment mark.

##### A. Gate level processing

The high resolution lithography of the gate level was performed with the negative resist and involved an intermediate mask process. This process involved transferring the resist image into SiO<sub>2</sub> prior to the polysilicon etch process. This process was chosen due to the much higher selectivity of the SiO<sub>2</sub> than the resist during the polysilicon etch. A 200nm layer of negative resist was spun onto a deposited SiO<sub>2</sub> layer and softbaked at 120°C for 120s[2]. After a 90s development in Shipley MF319 developer a 10s O<sub>2</sub> plasma etch removed any residue around the patterns. The resist patterns were then transferred into the oxide with a dry etch step. The polysilicon was then etched with a three step process to produce a steep sidewall profile of the poly. The first etch was an isotropic etch to break through any native oxide on the poly, which was followed by a 6:1 selectivity process (Si:SiO<sub>2</sub>) which etched through the poly and then stopped immediately the etch end-point detection system registered the removal of the poly. A third highly selective 30:1 anisotropic process was then performed as a 25% over etch to produce a steep sidewall profile on the polysilicon.

##### B. Contact level

For the contact level processing A 200nm thickness of AZ PF 514 was spun onto a 250nm deposited layer of SiO<sub>2</sub>. Processing conditions for the positive resist involved the thinning of the resist with 2 parts AZ 1500 thinner to 1 part



resist. After spin coating at 3000 rpm the resist was softbaked at 126°C for 82s. Post exposure the resist was softbaked at 65°C for 70s and developed in Shipley MF319 developer, diluted 3:1 (MF319:H<sub>2</sub>O) with de-ionized water to make a 0.178N solution. The patterns, in fig. 4, show resist contact holes of length 120nm. This size of feature allows for the processing of fully scaled contact holes in the fabrication of nano scale MOS devices.



Fig. 4. Image of 120nm contact holes developed in positive resist.

V. RESULTS

Fig. 5. shows the current-voltage characteristics of two nFET devices with gate lengths of 500nm and 90nm. The width of the devices is 6µm. The 500nm device exhibits normal transistor action with suppression of the short-channel effects while the 90nm device exhibits transistor action with onset of punchthrough of the channel region. This is shown by the inability of the gate to control the drain current,  $I_D$  when the device is saturated.

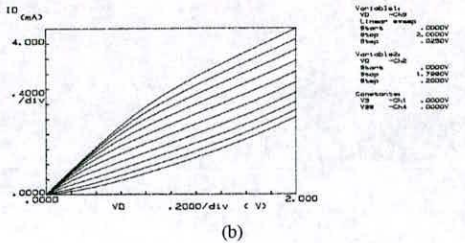
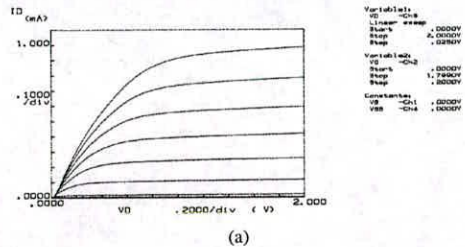


Fig.5. I-V characteristics of MOSFET devices with gate lengths of (a) 500nm, and (b) 90nm. The operation of the devices in the subthreshold region are shown in Fig. 6. The longer 500nm device displays good subthreshold operation, with a subthreshold slope of 75mV/decade. The punchthrough in the channel of the 90nm device is evident again with a subthreshold slope of just 8mV/decade.

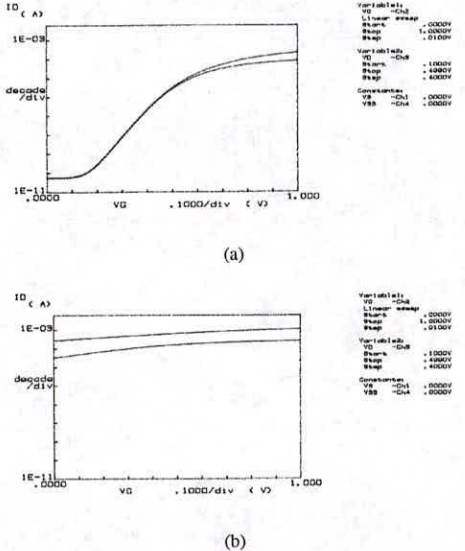


Fig. 6. Subthreshold characteristics of devices with channel lengths of (a) 500nm, and (b) 90nm.

A cross section of a 90nm MOSFET with 1µm contacts is shown in Fig. 7. The image highlights the partial etching through of the passivation layer above the gate electrode. The etching away of the material possibly occurred during the etching of the metal interconnects, but is not thought to have affected the performance of the devices.

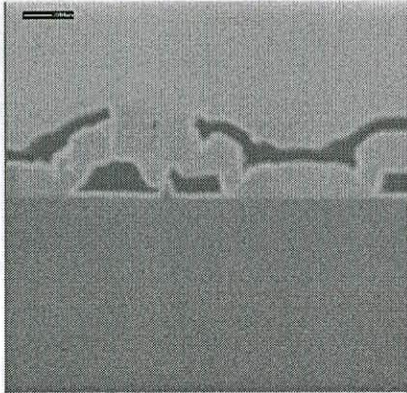


Fig. 7. Focused Ion Beam cross, section image of a 90nm MOSFET device with 1μm contacts.

#### VI. SUMMARY

Nanofabrication techniques for integration into a sub-100nm gate length silicon MOSFET fabrication have been reported. The development and characterization of an electron beam lithography system has enabled the production of MOS devices with all the lithography levels performed by electron beam lithography. Results have been presented for functional 90nm gate length devices which require further optimization to suppress the short-channel effects.

#### REFERENCES

- [1] SIA Semiconductor industry association, "The national technology roadmap for semiconductors", 1997.
- [2] D. Macintyre, S. Thoms, "High resolution studies on Hoechst AZ PN114 chemically amplified resist", *Microelectron. Eng.*, Vol 30, pp 327-330, 1996.
- [3] I.W. Rangelow, Z. Borkowicz, P. Hudek, I. Kostic, "Transfer of single-layer positive resist sub-micrometer and nanometer structures into silicon", *Microelectron. Eng.*, Vol 25, pp 49-66, 1995.



---

## References

---

D.S. Alles, C.J. Biddick, J.H. Bruning, et al. "EBES4: A new electron-beam exposure system". J. Vac. Sci. Technol. B, Vol. 5, No. 1, pp. 47-52, 1987.

G. Baccarani et al, "Analytical i.g.f.e.t. model including drift and diffusion currents". IEE Journal on Solid State and Electron Devices, Vol. 2, p62, March 1978.

(I)G. Baccarani, M.R. Wordeman, and R.H. Dennard. "Generalized scaling theory and its application to a  $\frac{1}{4}$  micrometer MOSFET design". IEEE Transactions on Electron Devices, Vol. ED-31, No. 4, pp. 452-462, 1984.

J.R. Brews. "A charge-sheet model of the MOSFET". Solid State Electronics, Vol. 21, p345, 1978.

I. Brodie and J.J. Murray. "The Physics of Microfabrication". Plenum, New York, 1982.

A.N. Broers, A.C.F. Hoole, and J.M. Ryan. "Electron beam lithography – resolution limits". Microelectronic Engineering, Vol. 32, pp. 131-142, 1996.

E.S. Bulat, G. Ditmer, C. Herrick and S. Hankin. "Characterization of biased electron cyclotron resonance deposited oxides". J. Vac. Sci. Technol. A, Vol. 10, No. 4, pp.1402-1406, 1992.

Cadence Design Systems Ltd, San Jose, California, USA.

S. Chaudhry, C.S. Rafferty, W.J. Nagy, Y.F. Chyan, M.S. Carroll, A.S. Chen, and K.H. Lee. "Suppression of reverse short channel effect by high energy implantation". Tech. Dig. IEDM, pp. 679-682, 1997

J. Chen, J. Tao, P. Fang, C. Hu. "0.35 $\mu$ m Asymmetric and symmetric LDD device comparison using a reliability/speed/power methodology". IEEE Transactions on Electron Devices, Vol. 19, No. 7, pp216-218, July 1998.

M.L. Chen, C.W. Leung, W.T. Cochran, W. Jungling, C. Dziuba and Y. Tungsheng. "Suppression of hot-carrier effects in submicrometer CMOS technology". IEEE Transactions on Electron Devices, Vol. 35, No. 12, pp2210-2220, Dec 1988.

H. Chenming. "Future CMOS scaling and reliability". Proceedings of the IEEE, Vol. 81, No. 5, May 1993.

C.F. Codella and S. Ogura. "Halo doping effects in submicron DI-LDD device design". Tech. Dig. IEDM, p230, 1985.

Z. Cui, R.A. Moody, I.M. Loader, J.G. Watson, and P.D. Prewett. "Optimized process for electron beam nanolithography using AZPN114 chemically amplified resist". Microelectronic Engineering, Vol. 35, pp. 145-148, 1997.

B. Davari, R.H. Dennard, G.G. Shahidi. "CMOS scaling for high performance and low power – the next ten years". Proceedings of the IEEE, Vol. 83, No. 4, pp. 595-606, 1995.

R. DeJouille, "Next-generation lithography tools: The choices narrow", Semiconductor international, Vol. 22, No. 3, pp48-50, 52, March 1999.

R.H. Dennard, F.H. Gaensslen, H.N. Yu, V.L. Rideout, E. Bassous, and A.R. LeBlanc. "Design of ion-implanted MOSFET's with very small physical



dimensions". IEEE Journal of Solid-State Circuits, Vol. SC-9, No. 5, pp. 256-268, 1974.

C. Duvvury. "A guide to short-channel effects in MOSFETs". IEEE Circuits and Devices Magazine, pp. 6-10, November 1986.

K. Early, D.M. Tennant, D.Y. Jeon, P.P. Mulgrew, A.A. MacDowell, and O.R. Wood II. "Characterization of AZ PN114 resist for high resolution using electron-beam and soft-x-ray projection lithographies". J. Vac. Sci. Technol. B, Vol. 10, No. 6, pp. 2600-2605, 1992.

Electronics weekly (Article from the magazine). "E-beam write from Tennessee". Reed business publications, 18<sup>th</sup> February 1998.

K.Y. Fu and Y.L. Tsang. "On the punchthrough phenomenon in submicron MOS transistors". IEEE Transactions on Electron Devices, Vol. 44, No. 5, pp. 847-855, 1997.

G. Groeseneken, R. Bellens, G. Van der bosch and H.E. Maes. "Hot-carrier degradation in submicrometre MOSFETs: from uniform injection towards the real operating conditions". Semicond. Sci. Technol., Vol. 10, pp. 1208-1220, 1995.

M.L. Hammond. "Introduction to chemical vapor deposition". Solid State Technology, pp. 61-65, Dec 1979.

G. Harbeke, L. Krausbauer, E.F. Steigmeier, A.E. Widmer, H.F. Kappert, and G. Neugebauer. "Growth and physical properties of LPCVD polycrystalline silicon films". J. Electrochem. Soc., pp.675-682, March 1984.

L.R. Harriott, S.D. Berger, C. Biddick, et al. "Preliminary results from a prototype projection electron-beam stepper-scattering with angular limitation projection

electron beam lithography proof-of-concept system". J. Vac. Sci. Technol. B, Vol. 14, No. 6, pp. 3825-3828, 1996.

M.B. Heritage. "Electron-projection microfabrication system". J. Vac. Sci. Technol., Vol. 12, No. 6, pp. 1135-1140, 1975.

D.R. Herriott, R.J. Collier, D.S. Alles, and J.W. Stafford. "EBES: A practical electron lithographic system". IEEE Transactions on Electron Devices, Vol. ED-22, No. 7, pp. 385-392, 1975.

D.A.Hodges and H.G. Jackson. "Analysis and design of digital integrated circuits". McGraw Hill, 1983.

C. Hu. "Future CMOS scaling and reliability". Proceedings of the IEEE, Vol. 81, No. 5, pp. 682-689, 1993.

H. Iwai. "Downsizing of silicon MOSFETs beyond 0.1 $\mu\text{m}$ ". Microelectronics Journal, Vol. 29, pp. 671-678, 1998.

D.J. Jung, J.K. Park, K.Y. Lee, N.S. Kang, K.N. Kim, T.E. Shim, and J.W. Park. "A 0.25  $\mu\text{m}$  complementary metal oxide semiconductor field effect transistor (CMOSFET) using halo implantation for 1 Gbit dynamic random access memory (DRAM)". Jpn. J. Appl. Phys., Vol. 35, Pt. 1, No. 2B, pp. 865-868, 1996.

D. Kahng, "A historical perspective on the development of MOS transistors and related devices". IEEE Transactions on Electron Devices, Vol. ED-23, No. 7, pp. 655-657, 1976.

M. Kamp, M. Emmerling, S. Kuhn, and A. Forchel. "Nanolithography using a 100kV electron beam lithography system with a Schottky emitter". J. Vac. Sci. Technol. B, Vol. 17, No. 1, pp. 86-89, 1999.



E.L. Kareh and R.J. Bombard "Introduction to VLSI silicon devices". Kluwer Academic Publishers, 1986.

H. Kawaura, T. Sakamoto, T. Baba, Y. Ochiai, J. Fujita, S. Matsui and J. Sone, "Transistor operation of 30-nm gate length EJ-MOSFETs". IEEE Electron Device Letters, Vol. 19, No. 3, pp. 74-76, 1998.

W. Kern and G.L. Schnable. "Low-pressure chemical vapor deposition for very large-scale integration processing – a review". IEEE Transactions on Electron Devices, Vol. ED-26, No. 4, pp. 647-657, 1979.

V.A. Kudryashov, V.V. Krasnov, S.E. Huq, P.D. Prewett, and T.J. Hall. "Electron beam lithography using chemically-amplified resist: resolution and profile control". Microelectronic Engineering, Vol. 30, pp. 305-308, 1996.

J.A. Liddle. "Lithography for 130nm and beyond". Semiconductor Fabtech, Vol. ED-8, pp. 191-198,

J.A. Liddle, S.D. Berger, C.J. Biddick, et al. "The SCattering with Angular Limitation in Projection Electron-beam Lithography (SCALPEL) system". Jpn. J. Appl. Phys., Vol. 34, Pt. 1, No. 12B, pp. 6663-6671, 1995.

Z.H. Liu, C. Hu, J.H. Huang, T.Y. Chan, M.C. Jeng, P.K. Ko, Y.C. Cheng. "Threshold voltage model for deep-submicrometer MOSFETs". IEEE Transactions on Electron Devices, Vol. 40, No. 1, pp. 86-94, 1993.

M.P. Lepselter, et al. "A system approach to 1- $\mu$ m NMOS". Proceedings of the IEEE, 71,p640, 1983.

J.Lutze and S. Venkatesan. "Techniques for reducing the reverse short channel effect in sub-0.5  $\mu\text{m}$  CMOS". IEEE Electron Device Letters, Vol. 16, No. 9, pp. 373-375, 1995.

D. Macintyre and S. Thoms. "High resolution studies on Hoechst AZ PN114 chemically amplified resist". Microelectronic Engineering, Vol. 30, pp. 327-330, 1996.

I.M. Mackintosh. "Applications of the scanning electron microscope to solid-state devices". Proceedings of the IEEE, pp370-377, April 1965.

P.J. Marcoux and P.D. Foo. "Methods of end point detection for plasma etching". Solid State Technology, pp. 115-122, April 1981.

G.E. McGuire. "Semiconductor materials and process technology handbook". Park Ridge NJ: Noyes publications, 1988.

S.J. Moss. "Chemistry of the semiconductor industry". Blackie and Son Ltd. 1987.

S.P. Murarka. "Silicides for VLSI applications", Orlando: Academic press, 1983.

Y. Nishioka, Y. Shiozawa et al "Giga-bit scale DRAM cell with new simple Ru/(Ba,Sr)TiO<sub>3</sub>/Ru stacked capacitors using x-ray lithography" Tech. Dig. IEDM, pp 903-6, 1995.

Y. Ochiai, S. Manako, S. Samukawa, K. Takeuchi and T. Yamamoto, "Accurate nano-EB lithography for 40nm gate MOSFETs". Microelectronic Engineering, Vol. 30, pp 415-418, 1996.



S. Okazaki, F. Mulai, Y. Takeda, K. Mochjii, E. Takeda, H. Kume, and S. Asai. "Electron-beam direct writing of *n*-MOS devices and analysis of overlay and linewidth accuracies". J. Vac. Sci. Technol., Vol. 19, No. 4, pp. 927-931, 1981.

M. Orlowski, C. Mazuré and F. Lau. "Submicron short channel effects due to gate reoxidation induced lateral interstitial diffusion". Tech. Dig. IEDM, pp. 632-635, 1987.

G. Owen. "Electron lithography for the fabrication of microelectronic devices", Rep. Prog. Phys, Vol 48, pp795-851, 1985

R.F. Pierret and J.A. Shields, "Simplified long channel MOSFET theory". Solid State Electronics, Vol. 26, p143, 1983.

H.C. Poa and C.T. Sah. "Effects of diffusion current on characteristics of metal-oxide(insulator)-semiconductor transistors". Solid State Electronics, Vol. 9, p927, 1966.

I.W. Rangelow, Z. Borkowicz, P. Hudek, and I. Kostić. "Transfer of single-layer positive resist sub-micrometer and nanometer structures into silicon". Microelectronic Engineering, Vol. 25, pp. 49-66, 1994.

(I)I.W. Rangelow, P. Hudek, I. Kostic, Z. Borkowicz, and G. Stangl. "Submicro- and nanometer e-beam lithography and reactive ion etching with single layer chemically amplified negative resist". Microelectronic Engineering, Vol. 23, pp. 283-286, 1994.

S.W. Ruska. "Microelectronic processing". McGraw Hill, 1987.

G. Sai-Halasz et al. "Experimental technology and characterization of self-aligned 0.1 $\mu$ m gate-length low-temperature operation NMOS devices". Tech. Dig. IEDM, p397, 1987.

N. Saitou. "Electron beam lithography – present and future". *Int. J. Japan Soc. Proc. Eng.*, Vol. 30, No. 2, pp. 107-111, 1996.

SIA94 "The National Technology Roadmap for Semiconductors" Semiconductor Industry Association, 1994

SIA97 "The National Technology Roadmap for Semiconductors" Semiconductor Industry Association, 1997

C.C. Shen, J. Murguia, N. Goldsman, M. Peckerar, J. Melngailis, and D.A. Antoniadis. "Use of focused-ion-beam and modeling to optimize submicron MOSFET characteristics". *IEEE Transactions on Electron Devices*, Vol. 45, No. 2, pp. 453-459, 1998.

J.P. Silverman. "X-ray lithography: Status, challenges, and outlook for 0.13  $\mu\text{m}$ ". *J. Vac. Sci. Technol. B*, Vol. 15, No. 6, pp. 2117-2124, 1997.

J.P. Silverman. "Challenges and progress in x-ray lithography". *J. Vac. Sci. Technol. B*, Vol. 16, No. 6, pp. 3137-3141, 1998.

C.G. Sodini and K.S. Krisch. "Silicon oxynitride gate dielectrics for scaled CMOS". *Tech. Dig. IEDM*, pp. 617-620, 1992.

D. Song, J. Lim, K. Lee, Y.J. Park, and H.S. Min. "Optimization study of halo doped MOSFETs". *Solid-State Electronics*, Vol. 39, No. 6, pp. 923-927, 1996.

M. Stockinger, A. Wild, S. Selberherr, "Drive performance of an asymmetric MOSFET structure: the peak device" *Microelectronics Journal*, Vol 30, pp229-233, 1999.



S.M. Sze. "VLSI Technology". McGraw Hill, 1988.

S.M. Sze "Semiconductor devices: Physics and technology". Wiley, 1985.

Y. Taur et al, "High transconductance 0.1 $\mu$ m pMOSFET". Tech. Dig. IEDM, pp127-30, 1993.

Y. Taur and E.J. Nowak. "CMOS devices below 0.1 $\mu$ m: How high will performance go?" Tech. Dig. IEDM, 215-218, 1997.

R.R. Troutman. "Subthreshold design considerations for IGFETs". IEEE J. Solid state circuits, SC-9 p55, 1974.

R.K. Watt. "Submicron integrated circuits", John Wiley and sons, 1989.

J. Wauters. "Extending optical lithography to 0.1 $\mu$ m?" Semiconductor Fabtech, Vol. ED-8, pp. 175-180,

S.J. Wind, Y. Taur, Y.H. Lee et al "Lithography and fabrication processes for sub-100nm scale complementary metal-oxide semiconductor". J. Vac. Sci. Technol B., Vol. 13, No. 6, pp. 2688-95, Nov-Dec 1995.

(I)S. Wolf and R.N. Tauber. "Silicon processing for the VLSI era - Volume 1, Process technology". Lattice press, 1986.

(II)S. Wolf. "Silicon processing for the VLSI era - Volume 2, Process integration". Lattice press, 1990.

(III) S. Wolf. "Silicon processing for the VLSI era - Volume 3, The submicron MOSFET". Lattice Press, 1995.

H.S.P. Wong, D.J. Frank, P.M. Solomon, C.H.J. Wann and J.J. Welser, "Nanoscale CMOS". Proceedings of the IEEE, Vol. 87, No. 4, April 1999.

R. Yan et al. "High performance 0.1 $\mu$ m room temperature Si MOSFET's". Proc. Symp. VLSI Technology, p86, 1992

J. Zhu, R.A. Martin, and J.Y. Chen. "Punchthrough current for submicrometer MOSFET's in CMOS VLSI". IEEE Transactions on Electron Devices, Vol. 35, No. 2, pp. 145-151, 1988.