Development and Characterisation of a Novel LDMOS Macro-model for Smart Power Applications

Steven Frère

A thesis submitted for the degree of Doctor of Philosophy.
The University of Edinburgh
June 30th, 2005

Abstract

In the automotive industry, there is a strong trend that has increased the electronics in cars for various functions like fuel injection, electric control of doors and windows, electric chair adjustment, air-conditioning, drive-by-wire, brake-by-wire, etc. The 12V battery used in present cars will not be sufficient for the increasing number of functions and as a consequence, a change towards 42V batteries will be necessary.

For these "automotive" systems, so-called smart power ICs must be used. These are chips in which the power functionality, e.g. the control of a motor is integrated with the logic control. There is also a trend towards operation at high voltages and integrating more intelligence using a microcontroller's RAM/ROM memory and several sensors and interfaces. The final goal is the integration of a complete system on a single chip, a so-called power System-on-Chip (SoC).

The interest in accurately modeling high-voltage transistors has increased in recent years due to the compatibility of these devices with standard CMOS technology. However, existing LDMOS models are not accurate enough for this task and SPICE models are especially weak when modeling AC performance. The limitation of these models lies in their lack of any capability to physically model some of the characteristic phenomena observed in LDMOS devices. The increased difficulty is related to complex 2D effects, specific to modern high voltage device architectures.

This thesis presents a new physically based macro-model. This model is based on the investigations performed on the key phenomena occurring in an LDMOS transistor. These phenomena were investigated by TCAD simulations and were confirmed by newly developed test-structures.

The model is accurate for wide geometry and temperature variations as well as for DC and AC operation. A novel corner extraction methodology based on neural networks has been developed making it possible to easily generate worst-case corners. As an extension of the neural network worst-case corner generation methodology, a static aging model card generation methodology is presented.

The model was verified on device level as well on circuit level yielding good results.

Declaration of originality

I hereby declare that the research recorded in this book and the manuscript itself was composed and originated entirely by myself in the department of Electronics and Electrical Engineering at the University of Edinburgh and in the Technology Research and Development group in the facilities of AMI Semiconductor Belgium BVBA. I actively contributed in the IST project Automacs and other DMOS releated R&D projects at AMIS and personally furnished original contributions on the topology of the DMOS model, especially on the AC part. I personally developed the extraction procedure and the novel corner generation methodology. I proposed a technique to create aged model cards.

Steven Frère

Acknowledgements

This thesis is dedicated to my parents. Without them all this would not have been possible.

A great many people have helped me over the past years I have been working towards my Ph.D. So I am sorry if I have left anyone out. The first person I would like to thank is Professor Anthony Walton, without whom none of this would have happened.

I would also like to thank everyone I have worked with at AMI Semiconductor's Technology Research and Development department and specifically the modelling group, most of whom have had some influence on this work in one way or another. Special thanks go to Renaud Gillon, Joseph Rhayem, Bart Desoete, Peter Moens and Davide Bolognesi for the interesting and fruitful discussions. I also would like to thank Marnix Tack, director of the Technology Research and Development department for giving me the opportunity to explore this topic at AMI Semiconductor.

The most important person I have to thank is Katrien for always being there with love and support over the last few years, even though it has meant many sacrifices. I would never have managed to finish this work without her patience and understanding.

Finally, I need to thank my friends for providing all the distractions required to make me take so long to finish the thesis. Thanks !

Contents

Abstract i

Declaration ii

Acknowledgements iii

Contents iv

List of figures viii

List of tables xiii

1. Introduction **1**

1.1. Background 2

1.2. LDMOS transistor models 4

1.3. Thesis plan 4

2. Introduction to LDMOS transistors **7**

2.1. Introduction 8

2.2. Structure of a n-type LDMOS 8

2.3. Important design parameters 9

2.4. The AMIS I2T technology family 12

2.5. LDMOS transistors in the I2T family 12

2.6. Circuit for model characterisation 16

2.7. Conclusion 19

3. Introduction to modelling **20**

3.1. Introduction 21

3.2. Definition of terms 21

3.3. Modelling example based on a diode model 22

3.4. Model types and their implementation 28

3.5. Conclusion 33

4. LDMOS macro-model characteristics and macro-model requirements **36**

4.1. Introduction 37

4.2. Electrical device characteristics 37

4.3. Model accuracy and robustness 42

4.4. Accuracy targets for the macro-model 44

4.5. Summary of accuracy targets 45

4.6. Robustness specifications 47

4.7. Conclusion 47

5. TCAD simulation of LDMOS transistors **49**

5.1. Capacitance behaviour of LDMOS transistors 50

5.2. Intrinsic Drain voltage (V_K) behaviour in relation to gate and drain voltage 56

5.3. Conclusion 60

6. Description and results of the developed test-chips for DC and AC-analyses **62**

6.1. Introduction 63

6.2. introduction to MESDRIFT test-structure 63

6.3. W-array test-structure 74

6.4. Junction diode test-structure 76

6.5. RF-measurement test-structure 78

6.6. Introduction to capacitance extraction based on s-parameter measurements 79

6.7. Capacitance calculation for an LDMOS transistor from measured s-parameters 86

6.8. Conclusion 89

7. The macro-model: definition / extraction procedure / worst-case corners **90**

7.1. Introduction 91

7.2. Macro-model topology 91

7.3. Detailed description of the macro-model components 94

7.4. Model parameter extraction procedure 102

7.5. Worst-case corner extraction 109

7.6. Conclusion 117

8. The macro-model: verification / static-aging / self-heating **118**

8.1. Introduction 119

8.2. Model verification 119

8.3. Methodology to include static-aging 140

8.4. Methodology to include self-heating 146

8.5. Conclusion 149

9. Conclusion and future work **150**

9.1. Challenges and opportunities 151

9.2. Conclusions 152

9.3. Future work 154

9.4. Final conclusion 156

Appendix A: Verilog-A model code **A-1**

Appendix B: Published papers **B-1**

List of figures

2.1	Generic structure of an n-type LDMOS	8
2.2	Current flow in an LDMOS	9
2.3	Formation of depletion regions in DMOS devices	10
2.4	Punch Through in an LDMOS	11
2.5	Identification of layout dimensions	13
2.6	Schematic view of the BULB-circuit	16
2.7	Schematic view of the motor driver-circuit	17
2.8	The four valid H-bridge switching states (excluding open circuit load state): (a) Supplies +VDC; (b) Supplies –VDC; (c) & (d) Both supply zero voltage (short-circuited load)	18
3.1	Equivalent diode circuit	22
3.2	Diode DC characteristic	23
3.3	CV measurement setup	26
4.1	Operating regions : Linear (I), Quasi-Saturation (II), Saturation (III)	37
4.2	Measured output characteristics of a device with W= 40µm, VGS = 1 – 3.5V.	43
4.3	Measured capacitances (Cgs, Cgd and Cgb) of an LDMOS device with width = 80µm at Vgs= -5 till 8V and Vds=0V.	42
5.1	Schematic and TCAD cross-section view. The black squares indicate the regions zoomed in on in the following graphs.	50
5.2	Schematic and TCAD cross-section view. The black dotted squares indicate the regions zoomed in on in the following graphs.	52
5.3	Comparison between measurements and simulations at Vds = 0V	52
5.4	Cgs, Cgb and Cgd at Vds = 0V	53
5.5	Cgs and Cgd when Vds > 0V	54
5.6	Depletion region in the drift region under the gate	55
5.7	Sensitivity of p-body/n-tub junction to VGS	56
5.8	LDMOS channel voltage variation as a function of VGS and VDS	57

5.9 VK and VBB as a function of VGS with source closed and open at VDS = 10V. 58
5.10 Space charge behaviour for different bias conditions: (a) VGS = 4.2V ; (b) VGS = 7.0V ; (c) VGS = 9.6V. For all simulations VDS was set to 10V. 59
5.11 Variation of the channel, accumulation and field oxide drift region resistance (Rchan, Racc and Rdrift) as a function of VGS (VDS=10V). 60
6.1 Cross section of MESDRIFT test structure and associated HP4156 measurement set-up. K-contact (n+ type) is designed in the drift region (close to pn junction) and its width, WK, is negligible compared to DMOS width, W. 64
6.2 Typical output characteristics, IDS vs. VDS, of X-DMOS (solid) and MESDRIFT (symbol) (both with W=40 μm): very good agreement is observed (including quasi-saturation region) demonstrating that the K-contact does not significantly change the HV MOSFET characteristics. 65
6.3 a) Intrinsic and extrinsic IDS-VGS and gm-VGS at VKS=VDS=50mV, measured with MESDRIFT mirroring X-DMOS, b) Extracted Rdrift at low VDS (=50mV). 66
6.4 Intrinsic drain (key) voltage, VK, vs. VDS with VGS as parameter, experimentally revealed by MESDRIFT. 66
6.5 Drift resistance, Rdrift vs. VDS for a range of VGS, as experimentally extracted with MESDRIFT (X-DMOS) at room temperature 67
6.6 Intrinsic drain voltage, VK, predicted by numerical simulation with calibrated 2D structure, calibrated on X-DMOS characteristics. Inset: drift depletion pinch-off limit highlighted. 68
6.7 Threshold voltage, VT, vs. temperature, T, for X- and L-DMOS. 69
6.8 Low field mobility, μn0, vs. temperature, T, for X- and L-DMOS. 69
6.9 Rdrift vs. VDS at constant VGS with the temperature, T, as a parameter. 70
6.10 Influence of temperature on Rdrift/Ron characteristics revealed by MESDRIFT. 70
6.11 Dynamic behaviour of MESDRIFT (X-DMOS) highlighted by a simple pulsed measurement set-up designed to study self-heating in HV MOSFETs: VDS and VK time constants are different. 71

6.12 Effect of pulse duration on the reconstructed output characteristics of X-DMOS. The self heating appears acceptably eliminated when impulse < 10 μs. 71

6.13 degradations of Rch, Rdrift, Ron induced by hot carrier measurements conducted on MESDRIFT with VDS=100V and VGS=12V: .Rdrift>0, Rdrift and Ron are similarly degraded. 72

6.14 degradations of Rch, Rdrift, Ron induced by hot carrier measurements conducted on MESDRIFT with VDS=98V and VGS=4.5V (at max Ibody): .Rdrift<0, Rch is significantly more degraded than in Figure 6.13. 73

6.15 W-array (a) overview of a W-array test-structure containing 17 LDMOS transistor variations. (b) Close-up 74

6.16 DC LDMOS measurement results of a W-array test-structure 76

6.17 junction diode test-structure 77

6.18 Measurement results of the junction diode teststructure for the Pbody-BLN diode 78

6.19 RF-test-structure frame 78

6.20 S-parameter comparison to reflection and through pass of a pair of spectacles 79

6.21 S-Parameters and characteristic impedance Z0 80

6.22 signal flow 81

6.23 the relationship between Sxx and the complex impedance of a twoport. 81

6.24 about the definition of S11 (S22 is just analogous). 84

6.25 how the complex resistance plane is transformed into the Smith chart 85

6.26 Smith chart overview 86

6.27 Schematic overview of the measurement setup 86

6.28 Extraction results of the RF measurement test-structure 88

7.1 Sub-circuit model of LDMOS device 91

7.2 Sub-circuit model of LDMOS device 92

7.3 JFET VT dependence as a function of VGS. 96

7.4 VK as modelled by a JFET as a function of VGS at VDS=10V. 96

7.5 VK and VBB as a function of VGS with source closed and open at VDS = 10V. 97

7.6 Capacitance behaviour for different types of MOS / DMOS transistors 99

7.7 LDMOS capacitances modelled by BSIM3V3.2 + Resistor 100

7.8 Simulated and measured CGD and CGS curves as a function of VGS at VDS = 0 and 20V for both the old and new models. (a) Comparison between measurements and simulations based on the new macro-model at VDS = 0V; (b) Comparison of CGS measurements and simulations based on the new macro-model and old model at VDS = 20V; (c) Comparison of CGD measurements and simulations based on the new macro-model and old model at VDS = 20V; (d) model topology 102

7.9 LDMOS, Ids-Vgs curve, different W, logarithmic scale 105

7.10 LDMOS, Ids-Vgs curve, different Widths, linear scale 106

7.11 LDMOS, Ids-Vds curve, different Vgs, linear scale 107

7.12 LDMOS, IDS-VDS curve, different VGS, linear scale 108

7.13 JFET VT behaviour in relation to the LDMOS VGS 109

7.14 Simulated and measured CGD and CGS curves as a function of VGS at VDS = 0 111

7.15 Section through an LDMOS. 112

7.16 Flow for translating E-Test parameter vectors into model parameter vectors. 115

7.17 Corners as the intersection of the extreme performance locus and the 99.73% confidence locus of the population. 116

7.18 Parameter excursions for worst-case models normalised to univariate standard deviations. 117

8.1 old LDMOS model topology. 119

8.2 LDMOS DC characteristics at temperature of 25C 122

8.3 LDMOS DC-characteristics at temperature of 125C 123

8.4 Comparison of measured and simulated capacitance data with the shorted MOS option at Vds = 0V 124

8.5 Comparison of measured and simulated capacitance data with the shorted MOS option at Vds = 20V 126

8.6 evolution of (RON*W) and (IDSAT/W) versus W for the extracted model 127

8.7 Robustness test at device level of the extracted model 128

8.8 Simulated E-test parameters for three corners at three temperatures for the extracted model. 129

8.9 Ids-Vgs and Gm-Vgs at Vds=100mV at three different temperatures: old and new model. 131
8.10 Ids-Vds at Vgs=5V (left) and at Vgs=12V (right) at different temperatures, old and new model. 132
8.11 Simulation results with old model / new model of the BULB circuit 135
8.12 Circuit simulations results of the motor driver with old / new model 137
8.13 Comparison of the modelled and measured RON 140
8.14 Comparison of the modelled and measured GMMAX 141
8.15 Comparison of the modelled and measured VTH 141
8.16 Comparison of the modelled and measured IDSAT 142
8.17 Logarithmic plot of the relative shifts of R1.r with time 143
8.18 Logarithmic plot of the relative shifts of U0 with time 143
8.19 Logarithmic plot of the relative shifts of VTH0 with time 144
8.20 Logarithmic plot of the relative shifts of VSAT with time 144
8.21 Comparison of measurements to the simulated values based on the Rinaldi equation 145
8.22 Comparison of corrected measurements to the simulated values based on the Rinaldi equation 146
8.23 Proposed implementation of Self-heating into the macro-model 147

List of tables

2.1. Important implants and layers thickness parameters for DMOS devices 13
2.2. Geometrical parameters definition 14
2.3. Overview of N-channel LDMOS device features 14
2.4. Overview of N-channel XDMOS features 15
2.5. Overview of P-channel XDMOS features 15
3.1. Overview/comparison of the different modelling concepts. 1 = excellent 5 = poor 32
4.1. Characteristic bias voltages for an LDMOS device. 38
4.2. Electrical parameters definitions for LDMOS devices 39
4.3. DC characteristics. The voltage values and voltage ranges in the table are specified for N-channel devices. For P-channel the inequaities and signs need to be adapted. 40
4.4. Generalised small-signal parameters of LDMOS devices 41
4.5. Pulsed characteristics for LDMOS devices 41
4.6. Summary of the accuracy targets specified as max. allowed error. 45
4.7. Summary of the accuracy targets specified as max. allowed RMS error. 46
7.1. Description of the different geometry parameters 104
7.2. Subthreshold parameters 105
7.3. Triode parameters 106
7.4. Saturation parameters 107
7.5. JFET parameters modelling quasi-saturation 108
7.6. subthreshold temperature parameter 109
7.7. linear region temperature parameters 110
7.8. Saturation temperature parameters 110
7.9. AC-parameters 111
7.10. Impact of the key model parameters on the E-test parameters. 114
7.11. Comparison between worst-case corners obtained from analysis on model parameter space versus E-test parameter space. 118

8.1. Range of DC-IV and AC-CV Characteristics. 121

8.2. Comparison of the statistically measured E-test parameters with the E-test parameters extracted from the new model based on the worst-case corner extraction method previously described. 130

8.3. Results of the BULB-circuit. 134

8.4. Results of the motor driver. 136

Introduction

1.1 Background 2
1.2 LDMOS transistor-models 4
1.3 Thesis plan 4

1.1 Background

The history of microelectronics effectively began with the creation, at the Bell Telephone Laboratories, of the point contact transistor by Bardeen and Brattain in 1947. Around the same time, Shockley developed the theory behind the bipolar junction transistor, though this was not successfully fabricated until 1951 [1]. Similarly the effect of electric fields on the conductivity of semiconductors was demonstrated by Shockley and Pearson in 1948, but it took over ten years before the first Si/SiO_2 MOSFET, which is now so widely used, was demonstrated by Kahng and Atalla [2].

Discrete transistors quickly found applications in hearing aids and transistor radios where their small size and low power consumption made them ideal replacements for thermionic valve technology [3]. However, they were not small enough for some applications and the impetus was there for the work, carried out at Texas Instruments by Kilby and at Fairchild Semiconductor by Noyce, which led to the production of the first integrated circuits at the end of the 1950's [4]. Kilby's circuits consisted of transistors fabricated using the mesa technique, where the collector contact is made to the backside of the wafer, and bonded gold wire is used for interconnect interconnect. Noyce's ICs more closely resembled present day chips because they used a planar fabrication technique, developed by Hoerni at Fairchild, where oxide masking and diffusion were used to form the transistors [5]. His chip also included interconnects, created by photolithographic definition of evaporated aluminium, in a process very similar to that used today.

The initial circuits were oscillators and simple digital flip-flops using two or three active devices along with passive elements but by 1971 the technology had advanced to the stage where the first microprocessor, the Intel 4004, was fabricated with 2300 transistors [6]. In 1965 Moore published a paper on the state of the semiconductor industry which predicted that the number of devices in an integrated circuit would double each year [7]. This prediction became known as "Moore's Law" and was revised in 1975 to state that the number of transistors per chip would double every 18 months [8]. More recently the slope has changed again to give a doubling of circuit complexity approximately every two years, which leads to the prediction that within the next ten years microprocessors will exist which contain one billion transistors [9].

The increases in integration and chip complexity have come about as a result of the scaling of the transistors, in particular the scaling of the gate length of MOSFETs, and this has driven the advances in technology. More recently however limits have been placed on the scaling of interconnect which has encouraged advanced interconnect technologies such as low-k dielectrics and copper metallisation [10]. The International Technology Roadmap for Semiconductors (ITRS) charts the requirements for future technologies and the most recent release covers the technology nodes extending to 2007 where 65nm interconnect half-pitch lengths are expected with MOS gate lengths approaching 25nm [11, 12]. The increases in complexity have placed a premium on testing for process control and verification and the most recent roadmap focuses heavily on future metrology requirements [13,14].

In the automotive industry, there is a strong trend that has increased the electronics in cars for various functions like fuel injection, electric control of doors and windows, electric chair adjustment, air-conditioning, drive-by-wire, brake-by-wire, etc. The 12V battery used in present cars will not be sufficient for the increasing number of functions and as a consequence, a change towards 42V batteries will be necessary.

For these "automotive" systems, so-called smart power ICs must be used. These are chips in which the power functionality, e.g. the control of a motor is integrated with the logic control. There is also a trend towards operation at high voltages and integrating more intelligence using a microcontroller's RAM/ROM memory and several sensors and interfaces. The final goal is the integration of a complete system on a single chip, a so-called power System-on-Chip (SoC).

For all these reasons, a more advanced technology is required. Such technologies for smart power applications are based on a standard low-voltage CMOS technology, where power devices suited for middle to high voltages (80V spikes for the 42V car-battery) are fabricated with additional process modules, for example a thicker gate oxide module.

Examples of such integrated power transistors are vertical and lateral DMOS (Double diffused MOS) and IGBT (Insulated Gate Bipolar Transistor). In many cases, a power switch is the key application.

In such devices, the on-resistance and breakdown voltage are important performance parameters. A trade-off is necessary to obtain a device with a low on-resistance and a high energy capability. Needless to say, there is also the requirement for low production costs and high reliability.

1.2 LDMOS transistor-models

The interest in accurately modelling high-voltage transistors has increased in recent years due to the compatibility of these devices with standard CMOS technology. LDMOS (Lateral Double diffused Metal Oxide Semiconductor) devices are now being more often employed in dynamic applications such as switches within power systems and fine slope control of electrical motor drivers. However, existing LDMOS models are not accurate enough for this task and SPICE models are especially weak when modelling AC performance. The limitation of these models lies in their lack of any capability to physically model some of the characteristic phenomena observed in LDMOS devices. The increased difficulty is related to complex 2D effects, specific to modern high voltage device architectures. Several workers have addressed the physics involved in the specific behaviour of these transistors [15], [16], [17], [18].

This thesis presents a new physically based macro-model. This model is based on the investigations performed on the key phenomena occurring in an LDMOS transistor. These phenomena were investigated by TCAD simulations and were confirmed by newly developed test-structures.

1.3 Thesis plan

This section briefly outlines the contents of the chapters, which follow.

Chapter 2: Introduction to LDMOS transistors A basic overview of the LDMOS transistor is presented. The LDMOS transistor is situated in the family of components that are used in automotive integrated circuits. A short description will be presented of the AMIS high voltage I2T family which is used throughout this thesis, highlighting the distinction made between the different types of LDMOS / XDMOS transistors. Finally, some circuits that are of key importance in automotive designs are presented.

Chapter 3: Introduction to modelling Some definitions in relation to modelling are outlined. An example of modelling a diode is presented which shows many different aspects of modelling.

Chapter 4: LDMOS macro-model characteristics and macro-model requirements The electrical characteristics that matter for the modelling of DMOS devices and for circuit design are identified. These characteristics will be used for benchmarking the macro-model and in particular for the specification of accuracy targets.

Chapter 5: TCAD simulation of LDMOS transistors Several physical effects are observed in a DMOS transistor and these can be simulated in TCAD (Technology Computer Aided Design). The key effects will be presented and discussed in the context of TCAD, illustrating how this can be applied to help develop models for circuit simulation programs.

Chapter 6: Description and results of the developed test-chips for DC and AC-analyses Test-structures are devices or a set of devices, used to analyse or verify a certain part of the process device behaviour. This chapter describes the different test-structures that were developed and used for the building-up and extraction of the macro-model. These test-structures and test-devices are designed so that they can be used to characterise either some of the behaviour observed from the TCAD simulations, or the complete device itself.

Chapter 7: The macro-model: definition / extraction procedure / worst-case corners Based on the findings of chapter 5 and chapter 6, a macro-model has been developed. As a first step, a topology is proposed and then the functionality of the topology is confirmed and an extraction procedure developed. As a model should be able to accurately predict the effect of process variations on the device performance, worst case models and a procedure to extract these models must be available This thesis proposes a novel method for this purpose, based on neural networks. A key element of establishing the model is to verify its performance against the targets set in chapter 4.

Chapter 8: The macro-model: verification / static-aging / self-heating This chapter presents the verification of the macro-model described in chapter 7. Proposals for future work are given at the end of the chapter, which covers methods to characterise self-heating effects and include static aging of LDMOS devices in the proposed macro-model.

Chapter 9: Conclusions and future work : In this chapter the conclusions from the work reported in the preceding chapters are reviewed. Suggestions for future work on the topics covered in this thesis are also made.

References

[1] J.I. Nishizawa, "The Transistor: A Look Back and a Look Ahead," Solid State Technology, pp. 73-75, Dec 1987.

[2] D. Kahng, "A Historical Perspective on the Development of MOS Transistors and Related Devices," IEEE Transactions on Electron Devices, vol. ED-23, pp. 655-657, Jul 1976.

[3] C. Melliar-Smith, M. Borrus, D. Haggan, T. L. A. Vincentelli, and W. Troutman, "The Transistor: An Invention Becomes a Big Business," Proceedings of the IEEE, vol. 86, pp. 86-110, Jan 1998.

[4] J. Kilby, "Invention of the Integrated Circuit," IEEE Transactions on Electron Devices, vol. ED-23, pp. 648-654, Jul 1976.

[5] G. Moore, "The Role of Fairchild in Silicon Technology in the Early days of "Silicon Valley"," Proceedings of the IEEE, vol. 86, pp. 53-62, Jan 1998.

[6] Y. Patt, "Requirements, Bottlenecks, and Good Fortune: Agents for Microprocessor Evolution," Proceedings of the IEEE, vol. 89, pp. 1553-1559, Nov 2001.

[7] G. Moore, "Cramming More Components onto Integrated Circuits," Proceedings of the IEEE, vol. 86, pp. 82-85, Jan 1998.

[8] P. Bondyopadhyay, "Moore's Law Governs the Silicon Revolution," Proceedings of the IEEE, vol. 86, pp. 78-81, Jan 1998.

[9] E. Korcynski, "Moore's Law Extended: The Return of Cleverness," Solid State Technology, vol. 40, pp. 359-364, Jul 1997.

[10] M. Bohr, "Interconnect Scaling - The Real Limiter to High Performance ULSI," Solid State Technology, pp. 105-111, Sep 1996.

[11] A. Allan, D. Edenfeld, W. Joyner, A. Kahng, M. Rodgers, and Y. Zorian, "2001 Technology Roadmap for Semiconductors," Computer, vol. 35, no. 1, pp. 42-53, 2002.

[12] P. Gargini, "The Global Route to Future Semiconductor Technology," IEEE Circuits and Devices Magazine, pp. 13-17, Mar 2002.

[13] Semiconductor Industry Association, International Technology Roadmap for Semiconductors: 2001 Edition. International SEMATECH, Austin, TX, USA, 2001. http://www.public.itrs.net/.

[14] Solid State Technology Staff, "Meeting 2001 ITRS Challenges," Solid State Technology, pp. 42-64, May 2002.

[15] Y.-S. Kim, J. Fossum, "New Physical Insights and Models for High-Voltage LDMOS IC CAD," IEEE Trans. Electron Devices, vol. 38, pp. 1641-1649.

[16] J. Jaejune, T. Amborg, Yu. Zhiping and R.W. Dutton, "Circuit model for power LDMOS including quasi-saturation," Proceedings of SISPAD '99, pp.15-18.

[17] C. Anghel, N. Hefyene, A.M. Ionescu, S. Frère, R. Gillon, M. Vermandel, B. Bakeroot and J. Doutreloigne, C. Maier and Y. Mourier, "Investigations and physical modelling of saturation effects in Lateral DMOS transistor architectures based on the concept of intrinsic drain voltage," Proceedings of ESSDERC 2001, pp. 399-402, Sep 2001.

[18] S.F. Frère, J. Rhayem, H.O. Adawe, R. Gillon, M. Tack, and A.J. Walton, "LDMOS Capacitance Analysis versus Gate and Drain Biases, Based on Comparison between TCAD Simulations and Measurements," Proceedings of ESSDERC 2001, pp. 219-223, Sep. 2001.

Introduction to LDMOS transistors

2 Introduction to LDMOS transistors 8
2.1 Introduction 8
2.2 Structure of an n-type LDMOS 8
2.3 Important design parameters 9
2.3.1 The Breakdown Voltage 9
2.3.2 The on-resistance 11
2.4 The AMIS I2T technology family 11
2.5 DMOS transistors in the I2T100 family 12
2.5.1 Implants and oxide layers 12
2.5.2 Geometrical parameters definitions 13
2.5.3 LDMOS device family 14
2.5.4 XDMOS devices 15
2.6 Circuit for model characterisation 16
2.6.1 Bulb – circuit 16
2.6.2 MOTOR-driver circuit (H-bridge) 17
2.7 Conclusion 19

2 Introduction to LDMOS transistors

2.1 Introduction

This chapter presents a basic overview of the LDMOS transistor. The LDMOS transistor is situated in the family of components that are used in automotive integrated circuits. A short description will be presented of the AMIS high voltage I2T family which is used throughout this thesis highlighting the distinction made between the different types of LDMOS / XDMOS transistors. Finally, some circuits that are of key importance in automotive designs are presented.

2.2 Structure of an n-type LDMOS

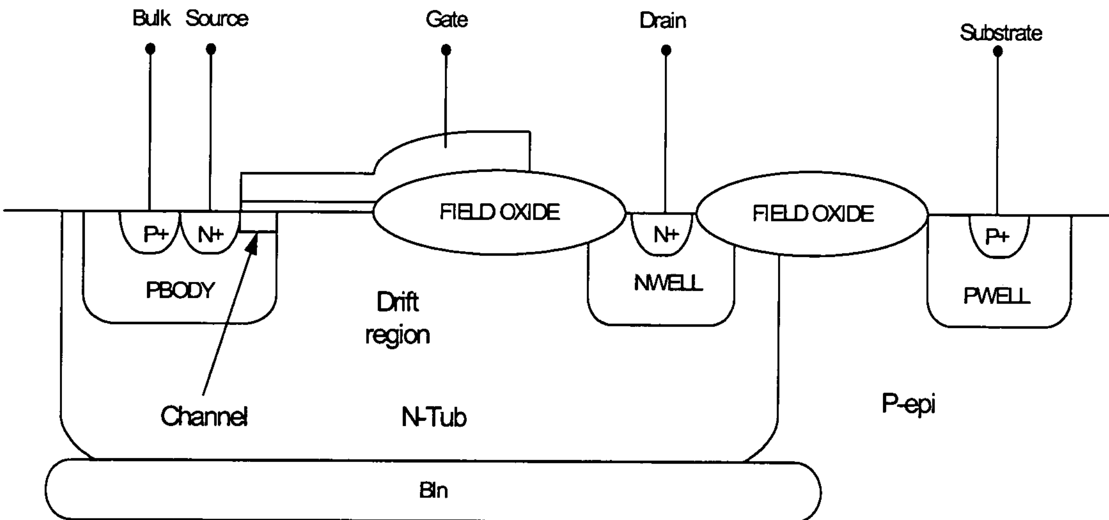


Figure 2.1 Generic structure of an n-type LDMOS

The cross-section of a generic n-type Lateral Double diffused MOS (LDMOS) is shown on Figure 2.1. The term lateral indicates the fact that the LDMOS is a horizontal device, where the current flows horizontally from the drain to the source. The second qualifier expresses the fact that the PBODY and the N+ source regions are diffused through a common window defined by the edge of the polysilicon gate.

In the on-state the LDMOS works as a normal MOS device. The positive potential applied to the gate attracts electrons (in the case of an n-type LDMOS) at the surface of the PBODY under the gate creating a channel allowing current to flow (Figure 2.2). The difference between a MOS and an LDMOS device comes from the presence of the drift

region (light grey region in Figure 2.1, which is a combination of the N-Tub and N-well areas). The drift region is lightly doped and its purpose is to provide a high voltage blocking capability during off-state. This blocking capability (characterised by the breakdown voltage) is created by the reverse biased PBODY-Ndrift junction.

The LDMOS has a parasitic Bipolar Junction Transistor (BJT). It is constituted by the source N^+, PBODY and Ndrift layers, which are respectively the emitter, the base and the collector. The triggering of this parasitic BJT reduces the performance of the LDMOS and, hence, the source and the body layers are usually shorted.

The thick field oxide is necessary to avoid the destruction of the thin gate oxide resulting from a high drain to gate voltage.

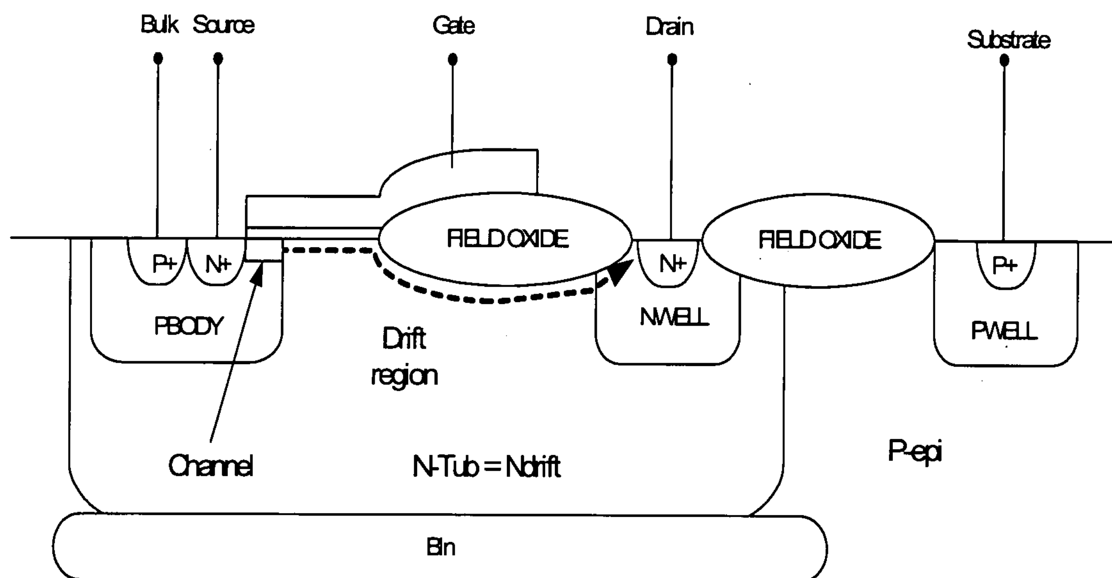


Figure 2.2 Current flow in an LDMOS

2.3 Important design parameters

2.3.1 The Breakdown Voltage.

The breakdown voltage of the device is the voltage at which the device enters into avalanche breakdown and therefore is the fundamental determinant of the maximum operating voltage. Large values of breakdown voltage are desired to provide high blocking capabilities. The breakdown voltage is largely defined by the doping profile and the length of the PBODY-Ndrift blocking junction.

To be able to provide a high forward blocking capability, an optimum has to be determined for the doping profile of the PBODY-Ndrift junction and the PBODY depth.

When a positive voltage is applied at the drain (assuming the source and the gate are set at zero volts), the PBODY-Ndrift junction becomes reverse biased. It supports the drain voltage by extending the depletion layer on both sides of the junction. (Figure 2.3) To enhance the drain blocking voltage, the doping of the Ndrift region has to be reduced.
The forward blocking capability is created by the reverse biased PBODY-Ndrift junction. The depletion layer extends effectively only into the Ndrift layer as it is lightly doped. Therefore decreasing the Ndrift doping increases the depletion width. As a result, the potential barrier becomes higher, improving the blocking capability. However this results in higher resistivity and thus a higher on-resistance.

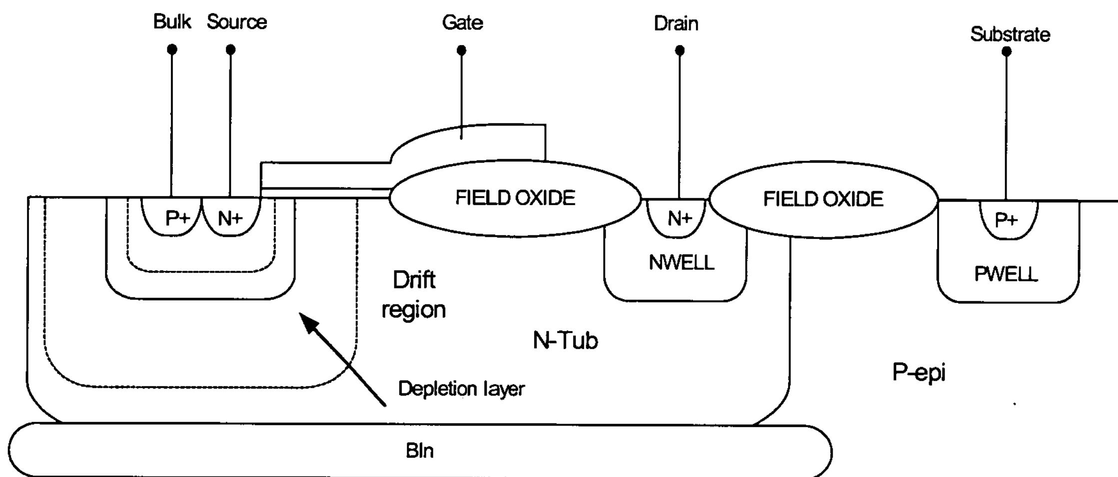


Figure 2.3 Formation of depletion regions in DMOS devices

This twofold effect implies that the doping level of the PBODY layer should be optimised between the LDMOS threshold voltage and the triggering of the parasitic bipolar. However, there is also another phenomenon which must be taken into account. It is called the punch-through effect and occurs when the depletion region in the PBODY extends so far that it comes into contact with the N+ source. At this moment, the potential barrier vanishes (Figure 2.4) and the device begins to conduct. To prevent punch-through, there are two alternatives. On the one hand, we can vary the PBODY thickness and doping level. Alternatively the N-Tub layer thickness can be increased because the depletion layer spreads approximately equally in every direction.

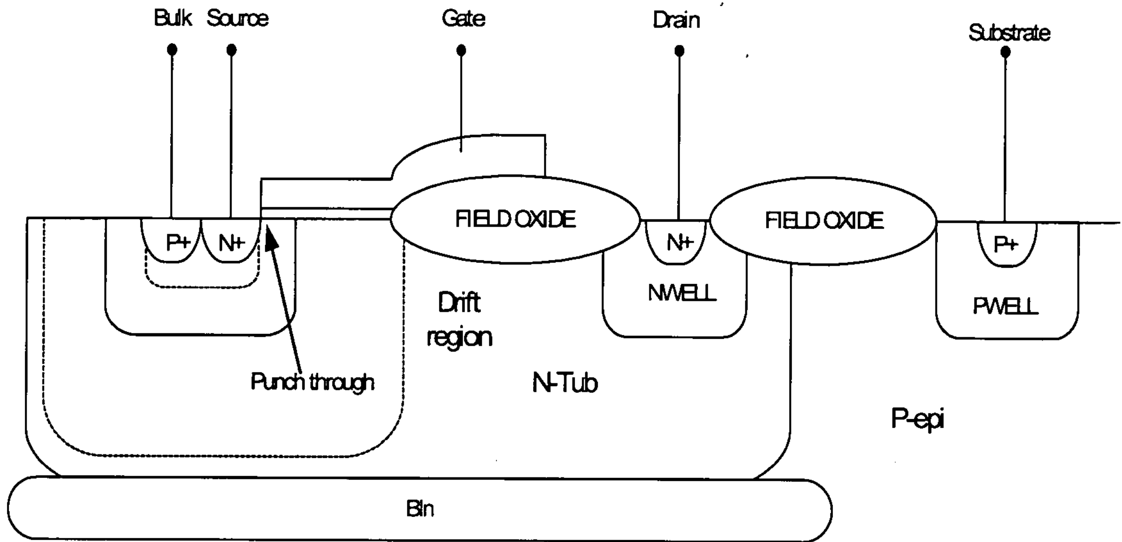


Figure 2.4 Punch Through in an LDMOS

2.3.2 The on-resistance

The on-resistance of the LDMOS is defined as the total resistance between the source and the drain contacts in the on-state. It is an important parameter as it directly determines the power dissipation during current conduction which is given by:

$$P = V_{DS}.I_D \tag{2.1}$$

$$= R_{on}.I_D^2 \tag{2.2}$$

The on-resistance is the sum of all the resistance contributions along the path travelled by the carriers during the on-state:

$$R_{on} = 2 \text{ x } R_{N+} + R_{CH} + R_A + R_{Ntub} + R_{NWELL} \tag{2.3}$$

where

R_{N+}	is the contribution from the N+ source or drain diffusion.
R_{CH}	is the channel resistance.
R_A	is the resistance of the accumulation layer formed in the Ntub under the polysilicon gate.
R_{Ntub}	is the Ntub resistance.(under the thick oxide)
R_{NWELL}	is the NWELL resistance.

2.4 The AMIS I2T technology family

The AMIS I2T100 technology family will be used for all the LDMOS devices which will be modelled in this thesis. The following gives a brief description of the major

attributes. The Intelligent Interface Technology (I2T) is the high voltage extension of the AMIS CMOS 0.7μm mixed signal technology. I2T100 has been developed to meet the increasing demand for more digital integration in mixed analogue/digital ASICs and more programmability/flexibility.

This technology is derived from a fully digital 0.7μm CMOS process and extended with the following analogue capabilities:

- Precision highly linear thin oxide poly/diffused capacitors
- Precision high ohmic polysilicon resistors
- Low Vt PMOS transistor
- Medium-High voltage NDMOS
- Floating medium-high voltage NDMOS and PDMOS
- Floating CMOS
- Low-medium-high voltage bipolar transistors
- Zener zap diode for OTP (One Time Programmable) applications
- High-Medium voltage floating capacitors
- Deep n+ doped guard rings
- EEPROM matrix blocks in the basic CMOS 0.7μm platform as well as in I2T100

Europractice distributes the design kit from AMIS, using the Cadence environment based on the Spectre simulator (Analog Artist) [1] for mixed mode front-end simulation and Silicon Ensemble place&route for CMOS 0.7μm back-end.

2.5 DMOS transistors in the I2T100 family

The purpose of this section is to describe the various devices types in more detail. In particular, it identifies the location, extent and doping level of implants as well as the range of layout dimensions. This is necessary to obtain a better understanding of the features that are required by any model that is created.

2.5.1 Implants and oxide layers

The most important layers in DMOS devices are listed in Table 2.1 together with the order of magnitude of their doping levels, diffusion depths and gate-oxide thicknesses.

	Doping level	Depth
PBody	~10^{15} cm^{-3}	~1.5 μm
PWell	~10^{17} cm^{-3}	~0.5 μm
PSub	~10^{14} cm^{-3}	~500 μm
P-Epi	~10^{16} cm^{-3}	~3.5 μm
NBody	~10^{15} cm^{-3}	~1.5 μm
NWell	~10^{17} cm^{-3}	~2 μm
NTub	~10^{15} cm^{-3}	~5 μm
Thick Gate Oxide	n.a	35 – 50 nm
Thin Gate Oxide	n.a.	15 – 20 nm

Table 2.1 Important implants and layer thickness parameters for DMOS devices

2.5.2 Geometrical parameter definitions

The naming conventions for geometrical parameters, used in this document, are defined in Figure 2.5 and Table 2.2.

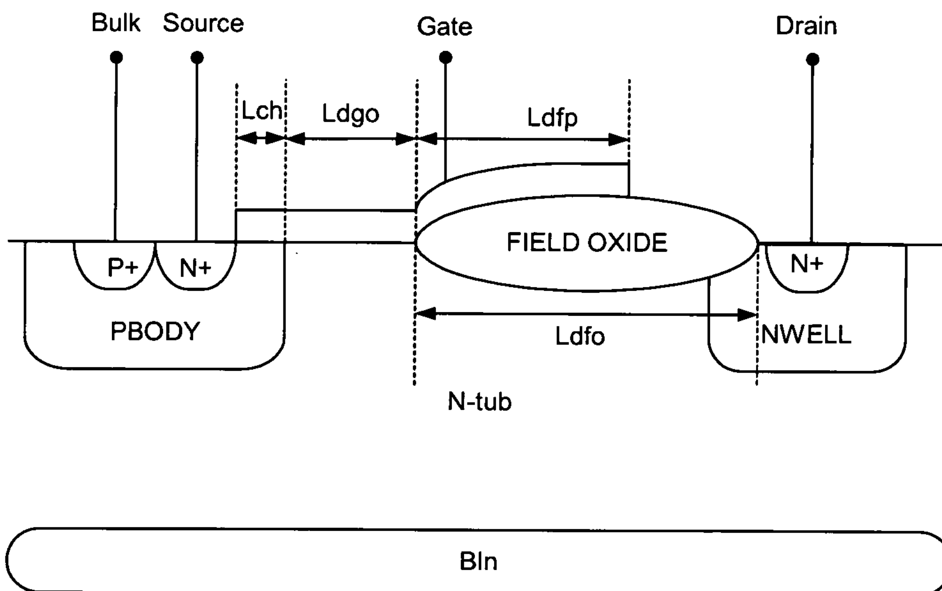


Figure 2.5 Identification of layout dimensions

Dimension	Description
W	Total width of the channel
Lch	Length of the channel region
Ldgo	Length of the drift region under the gate-oxide
Ldfp	Overlap of the gate poly on the field-oxide
Ldfo	Length of drift region under the field-oxide

Table 2.2 : Geometrical parameter definitions

2.5.3 LDMOS device family

LDMOS devices present one of the biggest modelling challenges due to the continuously varying doping concentration along the channel and the presence of an accumulation region of substantial length underneath the gate-oxide. The modelling of the drift region also requires a great deal of attention.

A description of the different parameters of the n-channel LDMOS device is presented in Table 2.3. In the I2T100-family no p-channel LDMOS device is available.

2.5.3.1 N-channel LDMOS device

Layers	Channel : Pbody Drift : Nwell Bulk : Pbody Gate Oxide : Thick	
Layout param.	Lch	0.5 μm – 1.5 μm
	Ldgo	1 μm – 2.5 μm
	Ldfp	1 μm – 6 μm
	Ldfo	2 μm – 9 μm
	W	2 μm– 10 mm
Comments	Floating, Self-aligned device	

Table 2.3 Overview of N-channel LDMOS device features

2.5.4 XDMOS devices

This new acronym was introduced to designate the family of 'eXtended Drain MOS' transistors, for which no real consensus exists in the literature. Contrary to LDMOS devices, the extent of the channel region is defined by specific masking steps, and the drain-end of the channel is not self-aligned to the source. The channel of these devices closely resembles that of common MOSFETs, and the major modelling challenges reside in the transition region at the end of the channel as well as in the drift region.

A description of the different parameters of the n and p-channel XDMOS devices is presented in Table 2.4 and Table 2.5 respectively. The cross-section of the device is similar to Figure 2.5.

<table>
<tr><td>Layers</td><td colspan="2">Channel : Pwell
Drift : Nwell or ntub
Bulk : p-epi/ psub
Gate Oxide : Thick or thin</td></tr>
<tr><td rowspan="5">Layout param.</td><td>Lch</td><td>3.5 μm – 4.5 μm</td></tr>
<tr><td>Ldgo</td><td>1.8 μm – 2.4 μm</td></tr>
<tr><td>Ldfp</td><td>2 μm – 3 μm</td></tr>
<tr><td>Ldfo</td><td>2.5 μm – 13 μm</td></tr>
<tr><td>W</td><td>2 μm – 10 mm</td></tr>
<tr><td>Comments</td><td colspan="2">Non-floating, Non self-aligned,
with or without BLN</td></tr>
</table>

Table 2.4 : Overview of N-channel XDMOS features

<table>
<tr><td>Layers levels</td><td colspan="2">Channel : Ntub or nwell
Drift : PField + Pbody or pwell
Bulk : Ntub
Gate Oxide : Thick</td></tr>
<tr><td rowspan="5">Layout param.</td><td>Lch</td><td>0.5 μm – 1.5 μm</td></tr>
<tr><td>Ldgo</td><td>1 μm – 2.5 μm</td></tr>
<tr><td>Ldfp</td><td>1 μm – 1.7 μm</td></tr>
<tr><td>Ldfo</td><td>2 μm – 3.5 μm</td></tr>
<tr><td>W</td><td>2 μm – 10 mm</td></tr>
<tr><td>Comments</td><td colspan="2">Floating device.</td></tr>
</table>

Table 2.5 : Overview of P-channel XDMOS features

2.6 Circuit for model characterisation

The following describes two standard circuits that have been used in commercial products where the main component is the DMOS transistor. These circuits will be used later in the thesis to evaluate the circuit-performance of the proposed macro-model.

2.6.1 Bulb – circuit

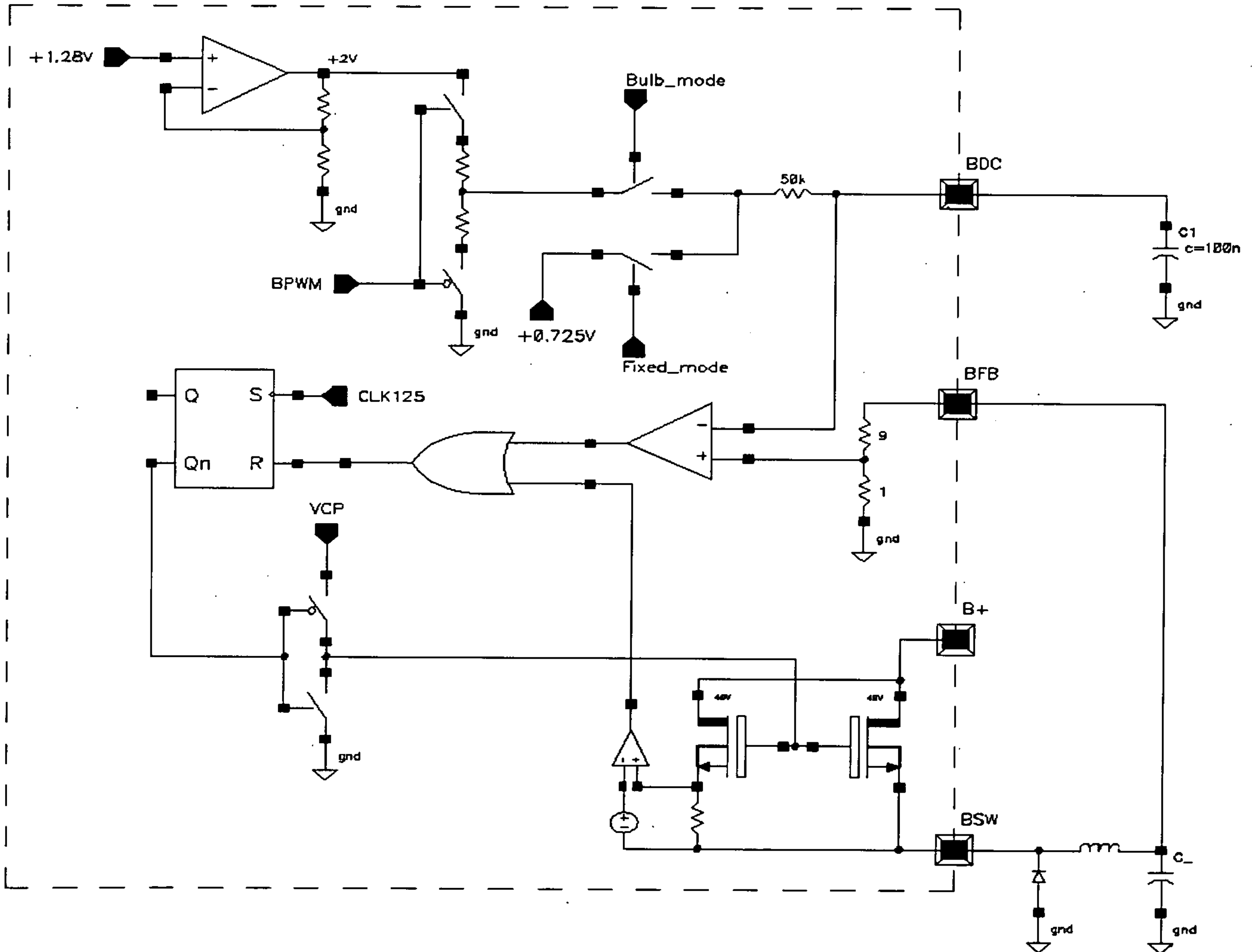


Figure 2.6 Schematic view of the BULB-circuit

The bulb driver is a variable voltage source that can be used in two different modes, either in 'bulb' or in 'fixed' mode. A circuit schematic view is shown in Figure 2.6.
In 'bulb' mode, it can generate an output voltage between 1.8V and 20V. The output voltage is defined by an external signal (Pulse Width Modulated = PWM), entering on the input pin (BPWM). In this 'bulb' mode, the load is an inverter circuit (DC/AC

converter), which supplies the bulb. In the 'fixed' mode the output voltage is fixed to a typical nominal level of 7.25V and in this mode the external PWM signal has no effect on the output voltage. In the 'fixed' mode the 7.25V output voltage is used to pre-regulate the internal 5V linear regulator and to supply the external LEDs, whose currents are controlled by internally programmable current source circuitry.

The bulb regulator/driver is implemented as a constant ripple buck regulator. This regulator can operate in discontinuous or continuous mode, depending on the load current and input voltage. The clock source is an on-board 125 kHz signal, realized by dividing down the master oscillator of 4 MHz by 32. Pulse skipping is applied for the lower current range. The N-type LDMOS power-switch is part of the ASIC, but the remaining components like the recovery diode, inductors and output capacitors, are external.

2.6.2 MOTOR-driver circuit (H-bridge)

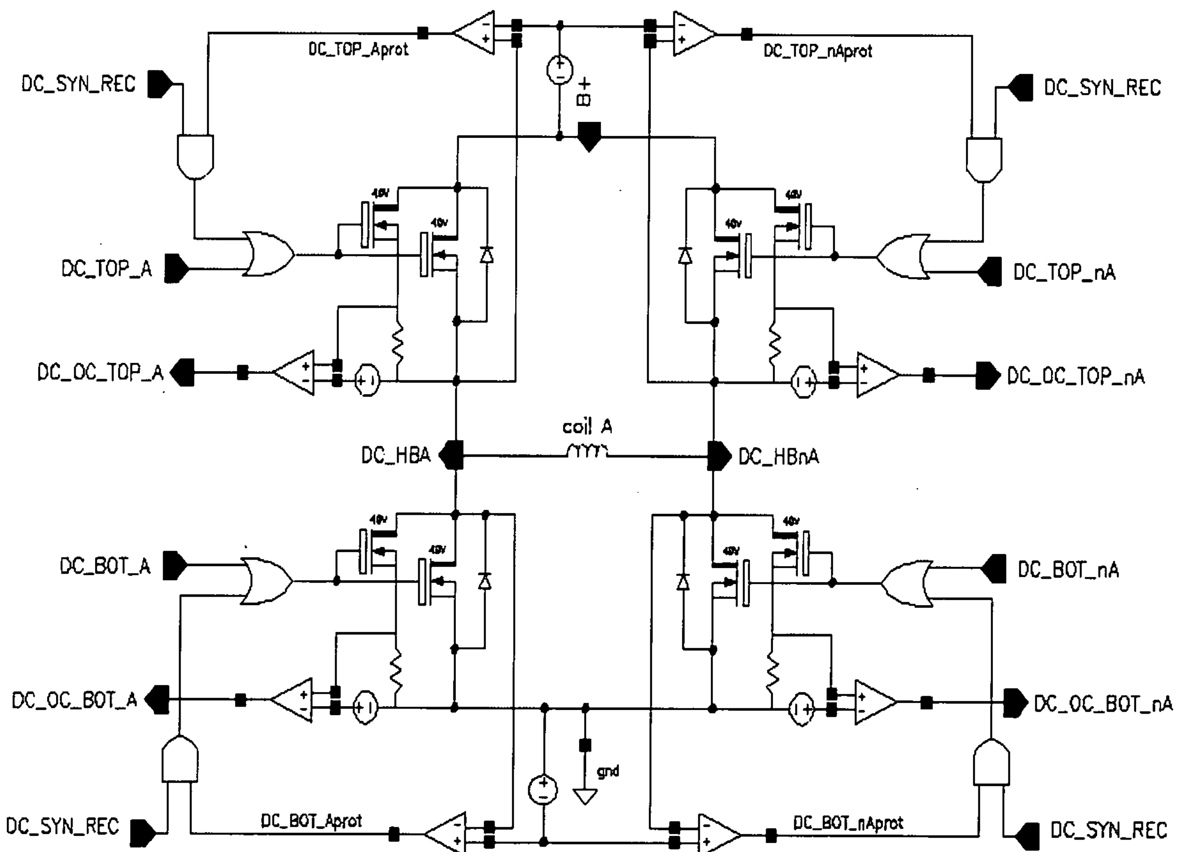


Figure 2.7 Schematic view of the motor driver-circuit

A typical circuit where DMOS transistors are used is an H-bridge driving a DC motor and a schematic view is shown in Figure 2.7. This versatile circuit is capable of applying voltages of both polarities across the load, by controlling the gating sequences of the four switches.

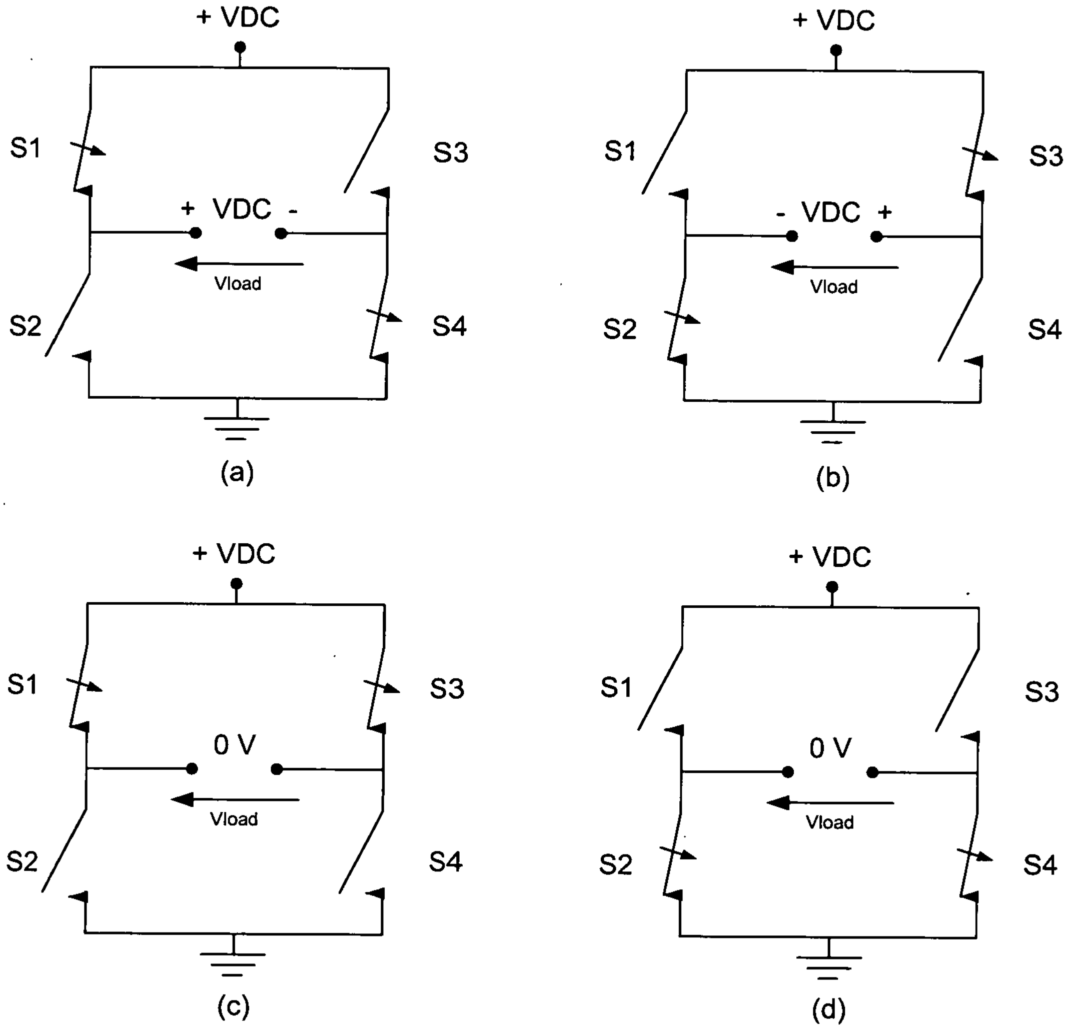


Figure 2.8 The four valid H-bridge switching states (excluding open circuit load state): (a) Supplies +VDC; (b) Supplies –VDC; (c) & (d) Both supply zero voltage (short-circuited load)

It is important to recognise that there are only four valid states for current conduction, as shown in Figure 2.8. Neglecting semiconductor voltage drops for the moment, one of these states applies +VDC across the load (Figure 2.8(a)), another applies -VDC (Figure 2.8 (b)) and the other two states (Figure 2.8(c) and (d)) effectively short circuit the load.

Current-regulated PWM control generally provides the basis for higher performance motor control than voltage regulation since torque is directly related to the motor winding current amplitude. Basic PWM voltage regulation is accomplished by means of a high-frequency duty cycle control. One straightforward PWM implementation compares the desired voltage level to a fixed-frequency ramp signal, switching the H-bridge output state when the ramp exceeds the command level. Using the H-bridge locked anti-phase control mode described above, the ramp comparison PWM strategy varies the average H-bridge output voltage over the full range from - VDC to + VDC by adjusting the relative widths of the -VDC and +VDC output pulses.

These two circuits were chosen as the key devices in these circuits are DMOS transistors. Hence the comparison of measured characteristics with simulation results will be a measure for the accuracy of the model. In addition to the issue of accurate circuit simulation results, these circuits are well suited to test the robustness of the model. This is because the device states in the circuit continuously change, introducing current spikes which the model should be able to withstand.

2.7 Conclusion

Different aspects of the DMOS transistor have been presented. An introduction to the various trade-offs that can be made when developing a DMOS transistor have been discussed. It has been shown that different classes of DMOS transistors exist, depending on how the channel is defined. It is these devices that will be used throughout this thesis to characterise the macro-model to be developed. Finally, two circuits have been selected (the bulb-circuit and the H-bridge) to validate the model and check the model accuracy and robustness.

References

[1] Affirma. Spectre Circuit Simulator Reference, Product Version 5.0.33, June 2004. website: www.cadence.com

Introduction to modelling

3 Introduction to modelling **21**

3.1 Introduction **21**

3.2 Definition of terms **21**

3.3 Modelling example based on a diode model **22**

3.3.1 Introduction 22

3.3.2 Equivalent circuit 22

3.3.3 DC Characterisation 23

3.3.4 CV Characterisation 25

3.4 Model types and their implementation **28**

3.4.1 Types of models 28

3.4.2 Implementation in circuit-simulators 30

3.4.3 Overview / comparison of different modelling concepts: 32

3.4.4 Discussion and Conclusion 32

3.5 Conclusion **33**

References **34**

3 Introduction to modelling

3.1 Introduction

The purpose of this chapter is to set some definitions in relation to modelling. An example of modelling a diode is used which shows many different aspects of modelling.

3.2 Definition of terms

The definitions for the terms analysis, simulation and modelling are derived from "Analyses and Simulation of Semiconductor Devices" by S. Selberherr. [1]

Analysis

- Separation of a whole into its component parts, possibly with comment and judgement.
- Examination of a complex, its elements, and their relations in order to learn.

Simulation

- Imitative representation of the functioning of one system or process by means of the functioning of another.
- Examination of a problem not subject to experimentation.

Modelling

- To produce a representation or simulation of a problem or process.
- To make a description or analogy used to help visualise something that cannot be directly observed.

Therefore, as difficult as it might be to decide in an individual case, analysis is at least intended to mean "exact analysis" and simulation must mean "approximate simulation" by inference. Modelling is obviously a necessity for analysis and simulation.

With a model one can analyse some phenomena, provided that the effects one wants to observe are built into the model, possibly in a very complex manner. A model for the purpose of pure simulation (like a curve fitting model) is usually much simpler than a model for analysis. Many effects can be treated in a very heuristic manner for the purpose of simulation, by representing the underlying physics in a qualitative way.

3.3 Modelling example based on a diode model

3.3.1 Introduction

A simple way to fit non-linear curves to measured non-linear data is to transform them to a linear representation. But the question is: how to do it? A look at the "target function" of the model equation gives a hint. For example in the case of an exponential function:

$$i = I_S \times e^{\frac{v_D}{N \times vt}} \tag{3.1}$$

the transformation needed is a simple logarithmic conversion. The symbols used in equation 3.1 are defined on the following pages. Once the measured data is transformed to this linear range, a linear regression analysis can be applied and the slope and y-intersect extracted. The model parameters are finally determined from these two values. This will become much more transparent in the following diode modelling example. An example of the procedure to define and extract a diode model is described in the following paragraphs.

3.3.2 Equivalent circuit

The SPICE equivalent schematic for a diode is shown in Figure 3.1. It consists of the ideal diode D representing its non-linear DC characteristic plus two voltage dependent capacitors for taking care of the space charge (C_S) and delay effects (C_D) as well as a series resistor RS for the high-current effects. Series inductors (bonding effects) as well as parasitic capacitors (housing effects) are neglected.

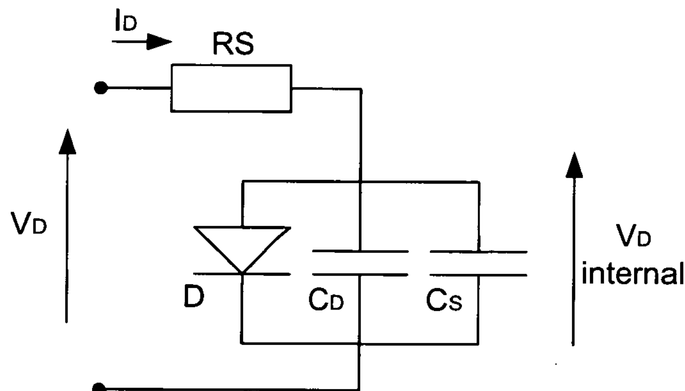


Figure 3.1 Equivalent diode circuit

3.3.3 DC Characterisation

Neglecting high current effects, assuming RS=0 or $V_D = V_{Dinternal}$, and also neglecting recombination effects for low biasing voltage, the diode current in the forward active region is modelled as follows:

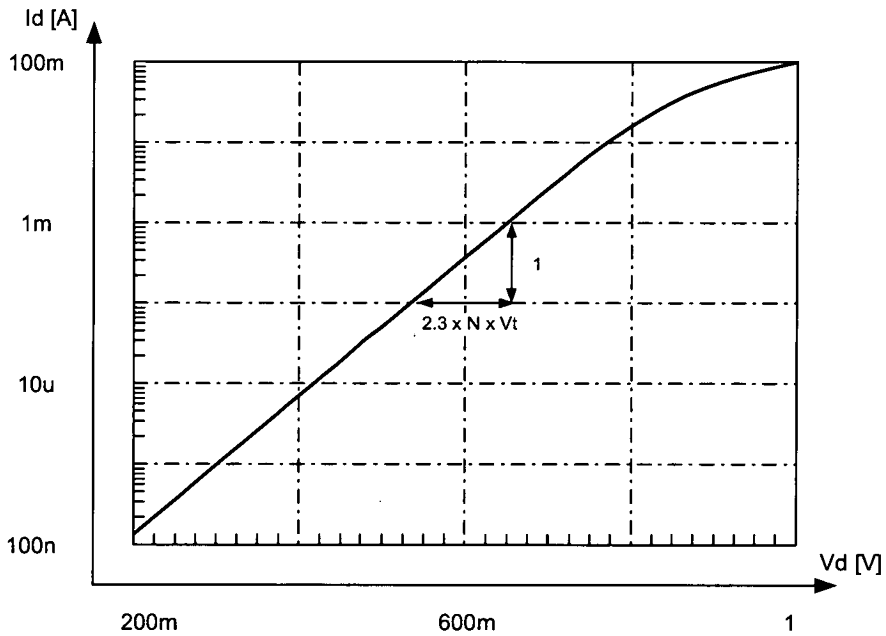
$$i_D = I_S \times \left(e^{\frac{v_D}{N \cdot Vt}} - 1 \right) \tag{3.2}$$

with :

I_s = saturation current (leakage current, typically fA)

N = emission coefficient (Ideal diode: N=1)

V_t = thermal voltage 27mV at 25°C or V_t= (k x T) / q = 8.617x10^{-5} x (T / °C + 273.15)



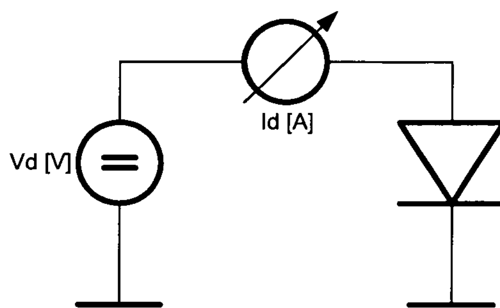


Figure 3.2 Diode DC characteristic

3.3.3.1 Determination of the parameters IS and N

Provided $V_D >> 0V$, i.e. neglecting the term (-1) in equation 3.2, and applying a logarithmic conversion gives:

$$\log(I_D) = \log(I_S) + \frac{V_D}{N \times V_T} \times \log(e) \tag{3.3}$$

$$= \log(I_S) + \left(\frac{1}{2.3 \times N \times V_T}\right) \times V_D \tag{3.4}$$

This is an equation of the form:

$$y = m \times x + b \tag{3.5}$$

In order to interpret equation 3.5 linearly, we have to substitute:

$$\begin{aligned} y &= \log(I_D) \\ b &= \log(I_S) \\ m &= \left(\frac{1}{2.3 \times N \times V_T}\right) \\ x &= V_D \end{aligned} \tag{3.6}$$

Equation 3.6 explains how to manipulate the measured data. After the logarithmic conversion of the measured values of I_D, they are introduced with the linear values of V_D into the regression equations. Thus, the y-intersect, b, and the slope, m, of the linear regression function are obtained.

Solving for I_S and for N one is able to determine these two parameters from b and m as follows:

$$I_S = 10^b \tag{3.7}$$

and

$$N = \frac{1}{2.3 \times m \times V_T} \tag{3.8}$$

The parameter extraction described above is valid only in that range of measured data, where the assumptions are true. This means: equations 3.7 and 3.8 are valid for $V_D > 0$ (data above the measurement resolution (non-noisy data), typ. > 0.2V) and where $e^{\frac{V_D}{N \times V_T}} >> 1$. The diode current should not be dominated by recombination effects (the weaker slope at low bias voltages) but not by high-current effects (non-ohmic effects, the knee in the half-logarithmic diode characteristic, typically above 0.7 V)

3.3.3.2 Determination of parameter RS

After the parameters I_S and N are extracted, the value of RS can approximately be found from the two highest bias points of index n and index (n-1) as follows:

$$RS = \frac{V_D(n) - V_D(n-1)}{I_D(n) - I_D(n-1)} \tag{3.9}$$

Another more precise method to determine the ohmic part of a diode characteristic is to consider the voltage drop between the ideal diode characteristic and its shift due to the ohmic effect. This is done by first determining the maximum current from the sweep by

$$I_{RS} = Ia.m[\max_index] \tag{3.10}$$

and then by calculating that voltage drop following

V_{RS} = measured voltage – ideal diode voltage

or

$$V_{RS} = Va.m[\max_index] - V_T \times N \times \ln\left(\frac{I_{RS}}{I_S}\right) \tag{3.11}$$

which finally gives

$$RS = \frac{V_{RS}}{I_{RS}} \tag{3.12}$$

Of course, the diode DC parameters I_S and N have to be determined first and are a pre-requisite for good RS extraction: the ohmic effect must dominate the diode characteristics in the portion used for the extraction. Referring to Figure 3.2, the reduction in slope for high bias voltage must be clearly visible in the extraction range.

3.3.4 CV Characterisation

The frequency behaviour of a diode can be modelled by a space charge capacitance (dominant at reverse bias) and a diffusion capacitance (dominant at forward bias) which models the time delay effects. The first capacitance is typically measured with a negative bias using a CV meter (capacitance versus voltage) while the latter is commonly measured using a network analyser. (Figure 3.3).

This paragraph covers the modelling of the space charge capacitor.

Extracting parameters C_{J0}, V_J and m

For $V_D < F_C \times V_J$:

$$C_S = \frac{C_{J0}}{\left(1 - \frac{V_D}{V_J}\right)^M} \tag{3.13}$$

or else :

$$C_S = \frac{C_{J0}}{\left(1 - F_C\right)^{(1+M)}} \times \left[1 - F_C \times (1 + M) + M \times \frac{V_D}{V_J}\right] \tag{3.14}$$

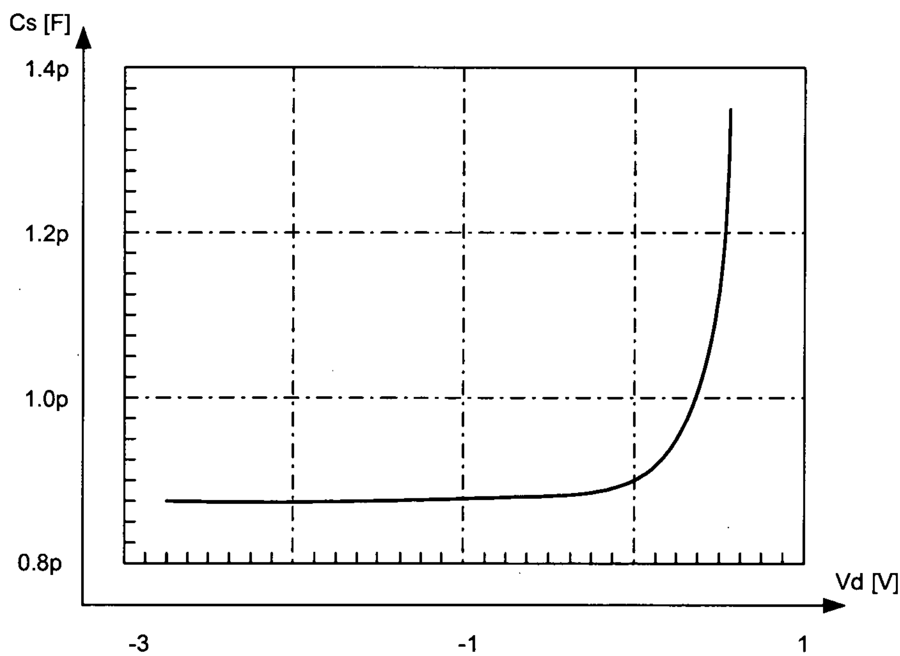
with:

C_{J0} : space charge capacitance at $V_D = 0V$

V_J : built-in potential or pole voltage

M : junction exponential factor (determines the slope of the CV plot)

F_C : forward capacitance switching coefficient (default 0.5)



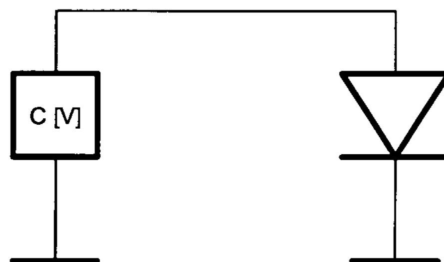


Figure 3.3 CV measurement setup

Determination of the CV parameters:

We only use the negative bias region for parameter extraction. The logarithmic conversion of equation 3.13 gives:

$$\log(C_S) = \log(C_{J0}) - M \times \log\left(1 - \frac{V_D}{V_J}\right) \tag{3.15}$$

This equation can be interpreted again as a linear function:

$$y = m \times x + b \tag{3.16}$$

with :

$$\begin{aligned} y &= \log(C_S) \\ b &= \log(C_{J0}) \\ m &= -M \\ x &= \log\left(1 - \frac{V_D}{V_J}\right) \end{aligned} \tag{3.17}$$

The procedure is to first logarithmically convert the measured values of C_S according to equation 3.17, along with the stimulating data of the voltage sweep V_D. Since the parameter V_J has a physical meaning, its value should be in the range of 0.2 to 1V. Therefore 0.2V is selected as a starting value for V_J. These two arrays are now introduced into the regression as yi- and. xi- values respectively. A linear model is fitted to this transformed "cloud" of stimulated and measured data and one gets the y-intersect b and the slope m for the value of V_J. These two values are the best choice for the given V_J. Now, this procedure is repeated with an incremented V_J, to obtain another pair of $m(V_J)$ and $b(V_J)$ values. The regression coefficient r2 will now be different from the earlier one, depending on the value of V_J, and whether the regression line fits the transformed data 'cloud' better or worse. Once the best regression coefficient is found, the iteration loop is terminated and one gets V_{J_OPT} as well as the corresponding $b(V_{J_OPT})$ and $m(V_{J_OPT})$.

The final parameter values are then:

$$M = -m(V_{J_OPT}) \tag{3.18}$$

and

$$C_{J0} = \exp\left(b(V_{J_OPT})\right) \tag{3.19}$$

The parameter extraction for the space charge capacitor is valid only for stimulus voltages below F_C x V_J, with F_{C}_default = 0.5.

In practice, there is always an overlay of this capacitance with some parasitic elements, such as packaging or bond pads. If they are not known and therefore cannot be de-embedded (eliminated from the measured data by using special test-structures or by calculations), the three modelling parameters may have values that have no physical meaning. This is especially true for V_J and M. Nevertheless, the fitting of the proposed method is generally very good

In order to keep the models simple and usable, and to have reasonable simulation times, models by definition suffer from some limitations:

DC: diodes may show recombination effects at low forward bias voltages, showing up as a lower slope on a half- logarithmic scale. In order to include this effect, the diode model is replaced by a subcircuit, consisting of a diode for the recombination effect, another one in parallel for the normal operating region and a resistance in series with both diodes.

CV: no parasitic capacitance is included in the diode model. A sub-circuit can easily be added to introduce a second parasitic capacitance

3.4 Model types and their implementation

3.4.1 Types of models

There are a number of approaches that can be taken when modelling MOS devices and the following summarises some of the options.

3.4.1.1 Functional models: [1] – [5]

The approach of a functional model treats the device as a "black box" and describes the externally observed behaviour without a detailed consideration of the physical effects occurring inside the device.

Standard low-power device models: [1]

The standard low-power device models are adapted for power semiconductor devices by optimising their parameters. Hence, the model parameters and equations can lose their physical meaning, and a pure functional description may result. These models, however, are hardly able to simulate any high-voltage phenomena.

Lookup table: [5]

In lookup tables, the data resulting directly from measurements or from calculations are stored and retrieved for simulation. This method is well suited for DC characteristics,

but it is much more difficult to use for dynamic effects of the device in the environment of different circuits. Therefore, the effort becomes very large to consider all the situations caused by the varying conditions in many different circuit topologies.

Empirical expressions: [2], [3],[4]

In many cases, the equations of functional models are selected from arbitrary mathematical expressions that describe the externally observed behaviour in a simplified way. When possible, the currents and voltages of the device terminals are approximated directly by straightforward functions. However, for a description of dynamic effects, it is often necessary to include additional variables into the equation set. These assumptions can be inspired by device physics, and, in some cases, they can be confirmed by theoretical derivations.

3.4.1.2 Approximate solutions: [6] – [13]

The model equations of this type are based on device physics, but since exact solutions are not possible or restricted to a few special cases, appropriate mathematical representations are found to approximate the solution. These approaches are purely empirical in many cases, but it is also possible to show that some functions come close to an exact solution under certain constraints of the boundary conditions.

Assumed solution : [13]

The knowledge of the characteristics is obtained from theoretical considerations or numerical calculations (device simulators) and geometrical curves are then used to model the shape.

Substitution in an equation: [6],[12]

The substitutions transform the partial differential equation into an ordinary differential equation that can easily be solved if suitable functions are chosen.

Neglecting terms: [7], [8] ,[9],[10], [11]

By assuming that certain terms become unimportant under certain conditions, one can neglect them and thus simplify the equation.

3.4.1.3 Transformation: [14] – [21]

Several mathematical techniques exist to solve differential equations analytically. For example, the differential equation can be transformed into an integral equation. Two methods have been used for the diffusion equation concerning power device models: Laplace transforms [14] – [20] and the application of Green's functions [21]. In

principle, these methods can lead to exact solutions. However, there are constraints for the boundary conditions and the solutions consist of infinite series. Since the series must be truncated to obtain results which are practicable, they do not require too much computational effort but the solutions are obviously an approximation.

3.4.1.4 Lumped Model: [22] – [25]

In the lumped-charge approach, the charge-storing region is subdivided into several sections, and the charge of each section is assigned to a charge storage node. The charge difference between two neighbouring nodes determines the current. This leads to relatively simple equations with little computation effort. The equations are valid for all stages of operation and are not limited to special cases. However, only medium accuracy is achieved with a small number of nodes.

The lumped-charge approach looks similar to the method of finite differences (described below). It can be regarded as a simplification to the greatest possible extent with a minimal number of nodes, but in a lumped model, the average charge densities of the sections instead of the densities at the nodes are inserted into the equations

3.4.1.5 Numerical Solution (TCAD approach): [26] ,[27], [32]

The most accurate solution is obtained by numerical methods, which are based on the discretisation of the considered region into a finite number of mesh points. Two methods can be distinguished.

Finite Differences: [27]

If the method of finite differences is used, the derivatives in the diffusion and transport equations are expressed by differences that have the form of an algebraic equation system.

Finite Elements: [26],[32]

Another possible numerical approach is the method of finite elements. It uses mathematical functions as approximate solutions for each of the discretised regions.

3.4.2 Implementation in circuit-simulators

The use of circuit simulators can be divided into two main methods; the subcircuit and mathematical method, which have been used in the past to implement power semiconductor device models into circuit simulation programs. The mathematical method is generally applicable to all modelling concepts and the subcircuit method, with its inherent limits in flexibility, to most of them.

3.4.2.1 The Subcircuit Implementation Method

Originally, circuit simulation programs (like SPICE and its derivatives) were not written to serve the needs of designing power electronic circuits. The widespread low-cost circuit simulation programs restrict themselves to a fixed set of functional elements (such as passive components, active components, and, in addition, controlled voltage and current sources) and do not allow user-defined functional elements except for a combination of these fixed elements into subcircuits. The subcircuit implementation method tries work within restrictions of these widespread circuit simulation programs for the implementation of new power semiconductor device models.

Unfortunately, the subcircuit implementation of accurate solutions for modelling power semiconductor devices soon becomes very complex. The reason is that the complex physical processes in the semiconductor device have to be represented by a combination of elements which bear little or no relation to the physical effect being modelled. Unavoidably, an unfavourable balance between accuracy and CPU requirements often results. Therefore, applicability and also the future development of the subcircuit implementation are expected to be rather limited. However, despite its limitations one great advantage is that the resulting models can be implemented in nearly every available circuit simulator and therefore have the best chance to become widely used, provided they can be tailored to perform the required job.

3.4.2.2 The Mathematical Implementation Method

If the circuit simulation program offers the individual definition of device models by describing them in mathematical form in a special description language or by writing a program in a general-purpose programming language, the mathematical implementation method can be used. This method is, of course, most effective with respect to modelling the unique physical phenomena present in power semiconductor devices because the mathematical relationships can be implemented directly in the form of the chosen approximation or solution. The disadvantage of the mathematical implementation method comes from the fact that the usability of the resulting power semiconductor device model is automatically restricted to just one circuit simulation program.

3.4.3 Overview / comparison of different modelling concepts: [30]

	Exactness	Calculation time	Parameter determin.	Application limits	Future potential	Main target
Functional model	5	2	1	4	4	Large circuits, system level
Approx. Solution	2	3	3	2	2	Medium circuits
Trans-formation	2	3	3	5	5	Medium circuits
Lumped model	4	1	2	3	2	Large circuits
Numerical solution	1	5	3	1	1	Small circuits

Table 3.1 Overview/comparison of the different modelling concepts. 1 = excellent 5 = poor

3.4.4 Discussion and Conclusion

The three modelling concepts, approximated solutions, lumped models and numerical solutions, have all been proven successful. These concepts are now competing for the leading position in providing the best value for practical applications. The use of the different modelling strategies depends upon the complexities of the power electronic circuits under consideration, such as the number of components (large, medium or small). Whether one of the modelling strategies can be further developed to enlarge its field of strength and can be proved superior, or whether they continue to exist successfully in parallel, is not clear at the moment.

However, there are also additional driving forces, from the area of power circuit applications. These include manufacturers of power semiconductor devices, and developments in separate research fields, predominantly the field of computational technologies. These driving forces may implement important boundary conditions for future developments in the field of power semiconductor device models for circuit simulation.

Parameter determination is one of the remaining critical issues for power semiconductor device models and will require increased attention in future. An intimate knowledge of the individual power device is needed, especially for applying the modelling concepts which allow a higher degree of accuracy.
Another set of important boundary conditions for future development will be defined by the available computational power, which fits the development budget of the user. In the past, the resources of available computational power in this sense have been steadily increasing. If this development continues, it will clearly favour the concepts of approximate and numerical solutions.

3.5 Conclusion

In this chapter some basic definitions were presented and illustrated by a simple diode model. An overview of the different types of models and how they are implemented was shown in the second part of the chapter. This enables the reader to situate the LDMOS model presented later on in this thesis. The LDMOS model, which will be discussed further on, is based on the functional model approach, more specifically it is a combination of standards low voltage components. In the simulator will be implemented by the subcircuit method.

References

[1] S. Selberherr, "Analysis and Simulation of Semiconductor Devices," Springer, 1984, ISBN: 3-211-81800-6; 294 pages.

[2] Zhou M.J., De Bruycker A., Van Calster A., Witters J., Schols G., "Modified SPICE modelling of DC characteristics for high-voltage DMOS transistors," Electronics Letters, Jan 1993, vol 29, no 1, pp. 126 – 127.

[3] Kuivalainen P., Gronlund M., Ronkainen H., "Simple analytical model for power DMOS transistors," Electronics Letters, Jan 1992, vol 28, no 2, pp. 187 – 188.

[4] Dolny G., Nostrand G., Hill K., "Characterisation and modelling of the temperature dependence of lateral DMOS transistors for high-temperature applications of power IC's," International Electron Devices Meeting, 1990, Technical Digest, pp. 789 -792.

[5] J. Pilacinski, "A method for determining the parameters of power MOSFET and IGBT transistor models applied in the PSPICE program," Proc. EPE'95, pp. 1.268 – 1.272.

[6] M. E. Clarke and S. Rahim, "A non-quasi-static empirical model of the power PIN diode for circuit simulation," International Journal on Computation Mathematical Electronics., Electron. Eng., vol. 13, no. 4, pp. 831 – 844.

[7] Lou K.H., Liu C.M., Kuo J.B., "An analytical quasi-saturation model for vertical DMOS power transistors," IEEE Transactions on Electron Devices, Volume 40, Issue 3, Mar 1993, pp. 676 – 679.

[8] Liu C.M., Shone F.C., Kuo J.B.;"A closed-form physical back-gate-bias dependent quasi-saturation model for SOI lateral DMOS device with Self-heating for circuit simulation.;" Proceedings of Technical Papers ,VLSI Technology Systems and Applications, 1995.

[9] Hong M.Y., Antoniadis D.A., "Theoretical analysis and modelling of sub-micron channel length DMOS transistors," IEEE Transactions on Electron Devices, vol 42, no 9, Sep 1995, pp. 1614 – 1622.

[10] Y. Hong, "Simulation and fabrication of sub-micron channel length DMOS transistors for analog applications," IEEE Transactions on Electron Devices, vol 40, no 12, Dec 1993, pp. 2222 – 2230.

[11] Grahn K., Andersson M., Kuivaliinen P., Eranen S., "Model for DMOST threshold voltage," Electronics Letters, Jul 1992, vol 28, no 15, pp. 1384 – 1385.

[12] P. Turkes and R. Kuhnert, "Compact models for the circuit simulation of power semiconductors," 6th Int. conf. on Power Semiconductors and Their Applications, Munich, Germany, 1992, pp. 17 – 25.

[13] C. H. Xu and D. Schroeder, "A power bipolar junction transistor model describing static and dynamic behaviour," IEEE Trans. Power Electron., vol. 7, no. 4, pp. 734 – 740, 1992.

[14] B. E. Danielsson, "Studies of turn-off effects in power semiconductor devices," Solid-State Electronics, vol. 28, no. 4, pp. 375 – 391, 1985.

[15] G. M. Strollo' "SPICE modelling of power pin diode using asymptotic waveform evaluation," PESC'96 Rec., pp. 44 – 50, 1996.

[16] G. M. Strollo and P. Spirito, "A new pin diode modelling approach for power electronic PSPICE simulations," PESC'94 Rec., pp. 52 – 58, 1994.

[17] G. M. Strollo, "A new SPICE subcircuit model of power Pin diode," IEEE Trans. Power Electron., vol. 9, no. 6, pp. 553 – 559, 1994.

[18] N. J. Conway and J. G. Lacy, "Integrated reverse-recovery model of the power bipolar diode for SPICE3," Electron. Letters, vol. 29, no. 15, pp. 1392 – 1394, Jul 1993.

[19] P. Tounsi, J. M. Dorkel, and P. Leturcq, "Thermal modelling for electrothermal simulation of power devices or circuits," 5th Europ. Conf. Power Electronics and Applications, 1993, pp. 155 – 160.

[20] S. Wu and F. A. Lindholm, "One-dimensional non-quasi-static models for arbitrary and heavily doped quasineutral layers in bipolar transistors," IEEE Trans. Electron Devices, vol. 35, no. 4, pp. 727 – 737, 1989.

[21] L. O. Chua and C. C. Chang, "High-speed non-linear circuit models for p-n junction diodes," Int. J. Circ. Theory Appl., vol. 16, no. 2, pp. 157 – 190, Apr. 1988.

[22] R. B. Darling, "A full dynamic model for pn-junction diode switching transients," IEEE Trans. Electron Devices, vol. 42, no. 5, pp. 969 – 976, 1995.

[23] Subramanian, Y., Lauritzen, P.O., Green, K.R., "Two lumped-charge based power MOSFET models," Computers in Power Electronics, 1998. 6th Workshop on, 1998, pp. 1 – 10.

[24] P.O. Lauritzen, I. Budihardjo, "The Lumped-Charge Power MOSFET model, Including Parameter Extraction," IEEE Transactions on Power Electronics, vol 10, no 3, May 1995, pp. 379 – 387.

[25] C.L. Ma, P.O. Lauritzen, Pao-Yi Lin, I. Budihardjo, "A systematic approach to modelling of power semiconductor devices based on charge control principles," Power Electronics Specialists Conference, pp. 31 – 37, 1994.

[26] P.O. Lauritzen, I. Budihardjo, Boontum Kongsang, "A power MOSFET Model based on a lumped – charge approach," IEEE PELS Workshop on Computer in Power Electronics 1992, pp. 165 – 171.

[27] Yeonbae Chung, Burk D.E, "A physically based DMOS transistor model implemented in spice for advanced power IC TCAD," Power Semiconductor Devices and ICs, ISPSD '95, Proceedings, pp. 340 - 345, 1995.

[28] Yeong-seuk Kim, J.G. Fossum, "Physical DMOST Modelling for high-voltage IC CAD," IEEE Transactions on Electron Devices, vol 37, no 3, Mar 1990, pp. 797 – 803

[29] E.C. Griffith, J.A. Power, S.C. Kelly, P. Elebert, S. Whiston, D. Bain and M. O'Neil, "Characterisation and Modelling of LDMOS transistors on a 0.6 um CMOS Technology," ICMTS 2000 Proceedings, pp. 175 – 180.

[30] Chung-Min Liu, Kuo J.B., "Quasi-saturation capacitance behaviour of a DMOS device," IEEE Transactions on Electron Devices, vol 44, no 7, Jul 1997, pp. 1117 – 1123

[31] R.Kraus, H.J. Mattausch., "Status and trends of Power Semiconductor Models for Circuit Simulation," IEEE Transactions on Power Electronics, Volume 13, Issue 3, May 1998, pp. 452 - 465

[32] Richard V.H. Booth and Colin C. McAndrew, "A 3-terminal model for diffused and ion-implanted resistors," IEEE transactions on Electron Devices, vol. 44, no. 5, May 1997, pp. 809 - 814.

LDMOS macro-model characteristics and macro-model requirements

4 LDMOS macro-model characteristics and macro-model requirements 37

4.1 Introduction 37

4.2 Electrical device characteristics 37

4.2.1 Device operating region 37

4.2.2 Temperature ranges 39

4.2.3 Electrical characteristic parameters 39

4.2.4 DC characteristic curves 40

4.2.5 Small-signal AC characteristics 41

4.2.6 Pulsed characteristics 41

4.3 Model accuracy and robustness 42

4.3.1 Accuracy 42

4.3.2 State-of-the art 42

4.4 Accuracy targets for the macro-model 44

4.4.1 DC 44

4.4.2 AC 44

4.5 Summary of accuracy targets 45

4.6 Robustness specifications 47

4.7 Conclusion 47

References 47

4 LDMOS macro-model characteristics and macro-model requirements

4.1 Introduction

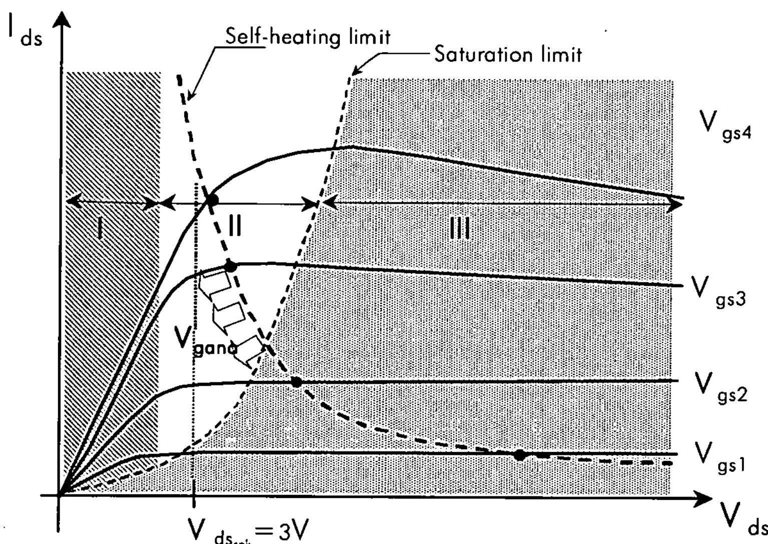
The purpose of this chapter is to identify the electrical characteristics that matter for the modelling of DMOS devices and for circuit design.[1][2][3][4][5] These characteristics will be used for benchmarking the macro-model and, in particular, for the specification of accuracy targets. These targets are similar to the ones used in the Automacs[1] project.[6].

4.2 Electrical device characteristics

4.2.1 Device operating region

Three main biasing-regions are considered for the operation of DMOS devices:

- The 'linear' or 'Ron' region, labelled '**I**' in Figure 4.1, characterised by $Vds < Vds_{snk}$
- The 'quasi-saturation' region, labelled '**II**' in Figure 4.1, where $Vds_{snk} < Vds < Vds_{sat}$
- The 'saturation' region, labelled '**III**' in Figure 4.1, where $Vds > Vds_{sat}$.



[1] Advanced unified lateral DMOS transistor model for automotive circuit simulation (AUTOMACS). The main project objective was to validate that more reliable and competitive circuits can be designed with new DMOS simulation models.

Figure 4.1 Operating regions : Linear (I), Quasi-Saturation (II), Saturation (III)

Additionally, a distinction is made between the 'analogue' operating region, where self-heating is negligible, and the region where self-heating has a marked influence on the characteristics. The analogue region is the preferred operating range for devices performing analogue functions like buffering or amplification. DMOS transistors used for switching have their quiescent states in the analogue region but during switching make a temporary incursion in the self-heating domain.

An overview of voltage terms used to describe the LDMOS device is provided in Table 4.1. This table also defines breakdown voltages and operating voltage limits which must be respected to maintain the device integrity and functionality.

Label	Description	Range (*)
Vds_{snk}	Upper limit of drain voltage for current sink (Ron) mode of operation	3V
Vds_{sat}	Limit of drain voltage at which current saturation occurs	
Vgs_{ana}	Upper limit of gate voltage for which self-heating is negligible (elevation of the average device temperature less than 10K). The region is used for analogue operation.	Vt0 + 2V
Vgs_{max}	Maximum gate operating voltage	3.3V to 20V
Vgs_{bd}	Break-down voltage for the gate oxide	Up to 30V
Vds_{max}	Maximum drain operating voltage	Up to 100V
Vds_{bd}	Break-down voltage at the drain	Up to 100V
V_{T0}	Threshold voltage at zero drain and bulk bias	0.5V to 3V
Vbs_{max}	Maximum bulk to source voltage	Up to 10V

Table 4.1 Characteristic bias voltages for an LDMOS device.

The voltages presented in this table are technology specific. These values are based on the AMIS I2T technology which is used throughout this thesis. A different technology will result in different voltages.

(*) Values are given in magnitude only. Signs have to be adapted for each type of device (N- or P-channel).

4.2.2 Temperature ranges

The temperature range over which the model should be accurate extends from –40°C to +150°C.

4.2.3 Electrical characteristic parameters

The electrical parameters defined in Table 4.2 are the LDMOS DC parameters which are measured automatically to assess process capability. It shows the typical ranges for these parameters and as they are systematically measured for process-monitoring, statistically relevant information can be obtained. Such data will turn out to be interesting for the definition of corner models.

Name	Typical ranges	Definition	Description
Vds_{lin}	/	0.1 V	Drain voltage for operation in linear regime
Vds_{sat}	/	5.0 V	Drain voltage for operation in saturation regime
V_{TO}	0.5 – 3.0 [V]	Vds_{lin}, max. slope of Ids(Vgs), V_{TO}= X intcp -Vd/2 Ids(Vgs)/sqrt(Gm(Vgs)), X intercept of HV asymptote.	Threshold voltage
BetaLin	55 – 1750 [$\mu A/V^2$]	Vds_{lin}; ß(lin) = max.slope Ids(Vgs)	Max. transconductance
SubThLin	50 – 200 [mV/dec]	Vds_{lin}, fit through Ids=2.5nA, 5nA, 7.5nA	Subthreshold slope
Ron	6.0 – 150 [Ω x mm]	Vgs = Vgsmax, Vds=0.5 V, Ron = Vds / (Ids / W)	On-resistance of unit channel width
Ids_{sat}	2.5 – 200 [μA/μm]	Vgs= 4V, $Vds=Vds_{sat}$	Specific saturation current per unit channel-width

Table 4.2 Electrical parameter definitions for LDMOS devices.

4.2.4 DC characteristic curves

For all configurations the source is the reference potential (Vs = 0).

No	Measurement	Bias Sweeps	Regions
DC1	Ids	Sweep Vgs from 0 to Vgs_{max} Several fixed Vds, $Vds_{snk} \leq Vds < Vds_{max}$	II, III
DC3	Ids, Ibs	Sweep Vg from 0 to Vgmax Several fixed Vds, $Vds_{snk} < Vds < Vds_{max}$ Several fixed Vbs, -1V < Vbs < 1V	II, III
DC4	Ids	Sweep Vds from 0 to Vds_{max} Several fixed Vgs , $V_{T0} < Vgs < Vgs_{max}$	I, II, III
DC5	Ids	Sweep Vds from 0 to Vds_{max} Several fixed Vgs, $Vgs < V_{T0}$	I, III
DC6	Ids, Ibs	Sweep Vds from 0 to Vds_{max} Several fixed Vg, $Vg < V_{T0}$ Several fixed Vbs, -1V < Vbs < 1V	I, II, III
DC8	Is, Isub	Sweep Vds from 0 to –1 Vsub=0, Vg < 0	III

Table 4.3 DC characteristics. The voltage values and voltage ranges in the table are specified for N-channel devices. For P-channel the quantities and signs need to be adapted.

The characteristics described above are necessary inputs to adequately describe an LDMOS device. These characteristics will be measured at different temperatures and on different sites on a wafer and will form the basis for the extraction of the model.

4.2.5 Small-signal AC characteristics

Table 4.4 defines the parameters used for small-signal AC characterisation of DMOS transistors. These measured characteristics should be distinguished from the generalised small-signal parameters to which they are related by an appropriate extraction procedure based on the assumption of a small-signal equivalent circuit model.

Name	Definition	Description
C_{gs}	dQg/dVs	Gate-source capacitance
C_{gd}	dQg/dVd	Gate-drain capacitance
C_{dg}	dQd/dVg	Drain-gate capacitance
C_{gb}	dQg/dVb	Gate-body capacitance
G_m	dId/dVg	Transconductance
G_{mb}	dId/dVb	Back-gate transconductance
G_{ds}	dId/dVd	Output conductance

Table 4.4 Generalised small-signal parameters of LDMOS devices

4.2.6 Pulsed characteristics

Pulsed characteristics are usefull for the characterisation of self-heating observed in devices dissipating large power. By means of pulsed measurements, the self-heating can be eliminated; making it possible to extract the basic model accurately without thermal effects. Pulses of 1 μs are applied.

No	Measured Char.	Bias Sweeps
PC1	Vg, Vd (oscilloscope)	Pulsing Ig, imposing Id << Vdmax / Ron

Table 4.5 Pulsed characteristics for LDMOS devices

4.3 Model accuracy and robustness

4.3.1 Accuracy

Accuracy is specified here in terms of the relative error (ratio of the absolute difference to the measured values) expressed as a percentage. In this document, the global model accuracy is described in terms of the maximum error found in specified bias and frequency ranges for the characteristics described above.

An alternative and less strict definition of accuracy is based on the root-mean-square (RMS) relative error. This figure gives an error globalised over the whole characteristic. Error specifications based on the RMS criterion are less strict than specifications based on the maximum error; indeed for a given RMS error bound on one characteristic, some points may have a significantly larger error, especially if the number of points in the characteristic is sufficiently large. To avoid this problem, errors are specified in this document as the maximum error found in a given range.

4.3.2 State-of-the art

Many papers report good accuracy for specific devices and on a limited set of curves and very seldom give accuracy figures over large biasing regions or provide enough data to extract them. It is also noteworthy that very few papers describe models that have been implemented into commercial simulators..

Based on published results, [7] [8] [9] [10] [11] [12] [13] [14] [15] [16] [17] [18] [19] [20] [21] [22], as well as on the experience at AMIS[2] in developing DMOS models for variable-width devices operated in a broad range of operating points, the present state-of-the-art can be summarised as follows:

For DC characteristics, within the 'Ron' and 'analogue' operating regions where self-heating is negligible, the accuracy is better than 15%. Outside these regions the accuracy degrades substantially. The negative slope of the measured output characteristics in Figure 4.2 denotes strong self-heating occurring in the device (which is not built into the model developed here). The measured data shown in Figure 4.2 looks noisy. This is due to the less accurate pulsed measurements.

[2] AMIS semiconductor Belgium bvba is a manufacturer of application specific circuits targeting the automotive, medical and industrial applications.

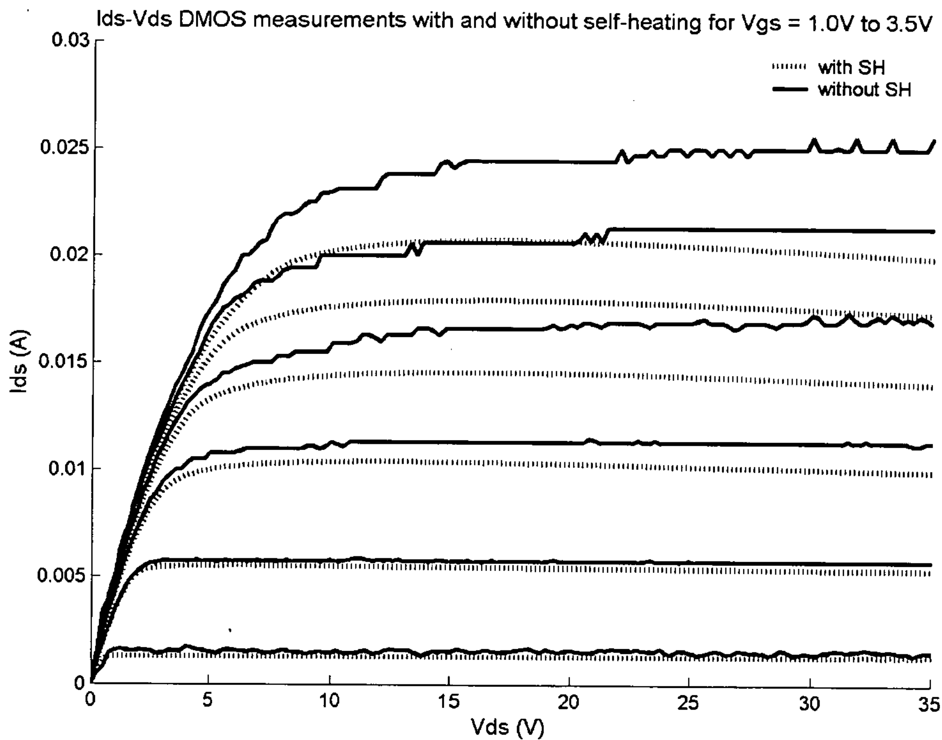


Figure 4.2 Measured output characteristics of a device with W= 40μm, VGS = 1 to 3.5V. Dotted lines: curves with self-heating; full lines: curves without self-heating

Regarding the AC characteristics the situation is more complicated. The accuracy on the (trans-) conductances is better than 25% in the 'Ron' and 'analogue' operating regions. For the susceptances, less data is available. For the Cgs, Cgd and Cgb capacitances very little data is available. Many models simply ignore these capacitances. The reason is that the channel, the transition region and the drift region all contribute to Cgs, Cgd and Cgb. For the transition and drift regions underneath the gate-oxide, models which are capable of modelling both depletion and accumulation behaviour are required. Few models have been proposed for accumulation channels and even less have become available in commercial simulators. The Cgd capacitance is often modelled as a gate bias-independent capacitor and, as shown in Figure 4.3, this can lead to dramatic errors.

Scalability (i.e. the ability to maintain the accuracy specifications for various device widths) is ensured for widths ranging from 5μm to several hundreds of μm. Limiting factors are narrow-width effects at the lower end of the range and self-heating and metal resistance for the large devices.

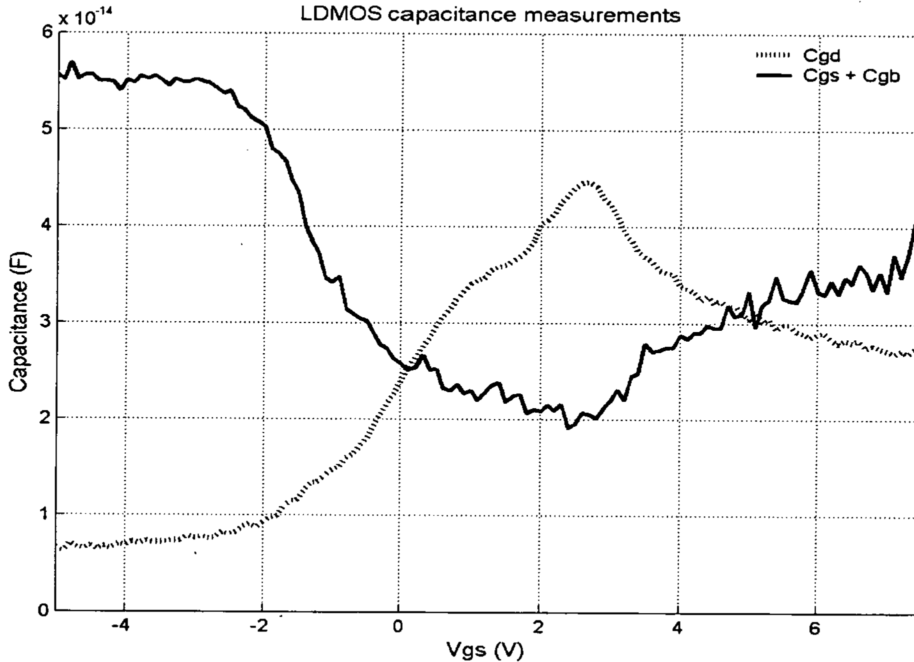


Figure 4.3 Measured capacitances (Cgs, Cgd and Cgb) of an LDMOS device with width = 80μm for a range of Vgs from -5V till 8V and Vds equal to 0V.

4.4 Accuracy targets for the macro-model

4.4.1 DC

For the improvements in region III the macro-model will need to include special features to account for self-heating. However, the characterisation and modelling of self-heating is outside the scope of this thesis.[23][24][25]

Where self-heating is not observed, the DC the macro-model focuses on improving Ron and Ids in regions II and III. For these characteristics the general target is better than 15% on the current and better than 10% on Ron.

4.4.2 AC

A challenging target for Cgd and Cgs is to raise the accuracy level to a target of better than 30%.[26]

4.5 Summary of accuracy targets

Table 4.6 and Table 4.7 show the accuracy specified in terms of the maximum / average relative percentage error tolerated in the specified range. This table will be a measure when evaluating the results obtained by an example extraction of the model later on in this work.

Parameter	Region	State-of the-art[3]	DMOS Macro-model
Ron	I	15	10
Ids	I	15	15
	II	30	15
	III	30	15
Gds	III	>100	30
Gm	I	25	20
	II	30	20
	III	30	20
C_{gs}	I	25	20
	II	25	20
	III	25	20
	Vgs < 0	NA	30
C_{ds}	I	100	30
	II	100	30
	III	100	30
C_{gd}	I	100	30
	II	100	40
	III	100	30
Ibs	I	NA	25
	II	NA	25
	III	NA	25

Table 4.6 Summary of the accuracy targets specified as max. allowed percentage error.

[3] These targets are based on previous modelling experience at AMIS. Generally in publications no exact figures are given concerning the parameters mentioned in Table 4.6 and Table 4.7

- RMS error specification for model accuracy

Parameter	Region	State-of the-art	DMOS Macro-model
Ron	I	15	5
Ids	I	15	10
	II	20	10
	III	20	10
Gds	III	>100	30
Gm	I	15	15
	II	15	15
	III	15	15
Cgs	I	25	15
	II	25	15
	III	25	15
	Vg < 0	NA	30
Cds	I	100	30
	II	100	30
	III	100	30
Cgd	I	100	30
	II	100	40
	III	100	20
Ibs	I	NA	25
	II	NA	25
	III	NA	25

Table 4.7 Summary of the accuracy targets specified as max. allowed RMS percentage error.

Notes:

- All numbers are for RMS deviation between model and measurements in the considered biasing regime. All numbers are expressed in percentage.
- Vgs < 0 for Cgs: this refers to an n-type device in common-source with Vs = 0V.

4.6 Robustness specifications

To be considered as robust, models must not cause simulator exception errors (such as floating point errors) or uncontrolled end of simulation events during DC or AC simulations in the specified temperature range, and for applied biases up to 3 times the Vgs_{max} or Vds_{max}.

4.7 Conclusion

This chapter has presented an overview of the characteristics of LDMOS transistors and its associated ranges and values. Also, a definition has been given as to what specifications a good LDMOS model should meet. These specifications will be used later to verify the performance of the LDMOS model which has been developed.

References

[1] R. Kraus and H. J. Mattausch, "Status and Trends of Power Semiconductor Device Models for Circuit Simulation", IEEE Transactions on Electron Devices, Vol. 13, no. 3, pp. 452-465, May 1998.

[2] M. Travedi, P. Khandelwal and K. Shenai, "Performance modeling of RF power MOSFET's", IEEE Transactions on Electron Devices, Vol. 46, no. 8, pp. 1794-1802, Aug 1999.

[3] P. Perugupalli, M. Trivedi, K. Shnai and S. K. Leong, "Modeling and characterization of an 80V silicon LDMOSFET for emerging RFIC applications", IEEE Transactions on Electron Devices, Vol. 45, no. 7, pp. 1468-1478, Jul 1998.

[4] P. Tuerkes and R. Kuhnert, "Compact models for the circuit simulation of power semiconductors," 6th Int. Conf. Power Semiconductors and Their Applications, 1992, pp. 17-25.

[5] Cliff L. Ma, P.O. Lauritzen, Pao-Yi Lin, I. Budihardjo, "A systematic approach to modeling of power semiconductor devices based on charge control principles," Power Electronics Specialists Conference, PESC '94 Record., vol.1, 25th Annual IEEE, 20-25 Jun 1994, pp. 31 – 37.

[6] IST automacs project, www.automacs.org.

[7] Y. Subramanian, P. O. Lauritzen and K. R. Shenei, "Two Lumped-Charge Based Power MOSFET Models", 6th workshop on Computer Power Electronics, 1998, pp. 1-10.

[8] M. Miller, T. Dinh and E. Shumate, "A new Empirical Large Signal Model for Silicon RF LDMOS FETs", Wireless Application Digest, 1997 IEEE MTT-S Symposium on Technologies for, 1997. pp. 19-22.

[9] "Motorola Electro-thermal (MET) LDMOS model", available on the Motorola web site: http://mot-sps.com/models/ldmos/ldmosmodels.html.

[10] Y. Subramanian, P. O. Lauritzen and K. R. Shenei, "A Compact Model for an IC Lateral Diffused MOSFET Using the Lumped-Charge Methodology", MSM'99, Apr 1999.

[11] Kuivalainen, P.; Gronlund, M.; Ronkainen, H., "Simple analytical model for power DMOS transistors," Electronics Letters, Jan 1992, vol 28, no 2, pp. 187 – 188.

[12] Lou, K.H, Liu C.M, Kuo, J.B., "An analytical quasi-saturation model for vertical DMOS power transistors," IEEE Transactions on Electron Devices, Vol. 40, Issue 3, March 1993, pp. 676 – 679.

[13] Liu C.M, Shone F.C., Kuo, J.B., "A closed-form physical back-gate-bias dependent quasi-saturation model for SOI lateral DMOS device with Self-heating for circuit simulation," Proceedings of Technical Papers, VLSI Technology Systems and Applications, 1995, pp. 149 - 152.

[14] Hong M.Y., Antoniadis, D.A., "Theoretical analysis and modeling of submicron channel length DMOS transistors," IEEE Transactions on Electron Devices, vol 42, no 9, sep 1995, pp. 1614 – 1622.

[15] Y. Hong, "Simulation and fabrication of submicron channel length DMOS transistors for analog applications," IEEE transactions on electron devices, vol 40, no 12, dec 1993, pp. 2222 – 2230.

[16] Grahn K., Andersson M., Kuivaliinen P., Eranen S., "Model for DMOST threshold voltage," Electronics Letters, jul 1992, vol 28, no 15, pp 1384 – 1385.

[17] P.O. Lauritzen, I. Budihardjo, "The lumped-Charge Power MOSFET model, Including Parameter Extraction," IEEE Transactions on Power Electronics, vol 10, no 3, May 1995, pp. 379 – 387

[18] P.O. Lauritzen, I. Budihardjo, Boontum Kongsang, "A power MOSFET Model based on a lumped – charge approach," IEEE PELS Workshop on Computer in Power Electronics, 1992, pp. 165 – 171.

[19] Yeonbae Chung, Burk, D.E, "A physically based DMOS transistor model implemented in spice for advanced power IC TCAD," Power Semiconductor Devices and ICs, 1995, ISPSD '95, Proceedings, pp. 340 – 345.

[20] Yeong-seuk Kim, J.G. Fossum, "Physical DMOST Modeling for high-voltage IC CAD," IEEE Transactions on Electron Devices, vol 37, no 3, March 1990, pp. 797 – 803.

[21] E.C. Griffith, J.A.Power, S.C. Kelly, P. Elebert, S. Whiston, D. Bain, and M. O'Neil, "Characterisation and Modeling of LDMOS transistors on a 0.6um CMOS Technology," ICMTS 2000 pp. 175 – 180.

[22] Richard V.H. Booth and Colin C. McAndrew, "A 3-terminal model for diffused and ion-implanted resistors," IEEE Transactions on Electron Devices, vol. 44, no. 5, May 1997, pp. 809 - 814.

[23] W. R. Curtice, J. A. Pla, D. Bridges, T. Liang and E. E. Shumate, "A New Dynamic Electro-Thermal Nonlinear Model for Silicon RF LDMOS FETs", Microwave Symposium Digest, 1999 IEEE MTT-S International, Vol. 2, pp. 419-422, 1999.

[24] Dolny G., Nostrand G., Hill K., "Characterization and modeling of the temperature dependence of lateral dmos transistors for high-temperature applications of power ICs," Electron Devices Meeting, International Technical Digest, 1990, pp. 789 -792.

[25] P. Tounsi, J. M. Dorkel, and P. Leturcq, "Thermal modeling for electrothermal simulation of power devices or circuits," 5th European Conf. Power Electronics and Applications, 1993, pp. 155-160.

[26] Chung-Min Liu, Kuo, J.B., "Quasi-saturation capacitance behavior of a dmos device," IEEE Transactions on Electron Devices, vol 44, no 7, july 1997, pp. 1117 – 1123.

TCAD simulation of LDMOS transistors

5 TCAD simulation of LDMOS transistors 50

5.1 Capacitance behaviour of LDMOS transistors 50

5.1.1 Comparison of TCAD simulations with measurements 51

5.1.2 Capacitances when $V_{DS} = 0V$ 52

5.1.3 C_{gs}, C_{gb} and C_{gd} when $V_{DS} > 0V$ 53

5.2 Intrinsic drain voltage (V_K) behaviour in relation to gate and drain voltage 56

5.3 Conclusion 61

5 TCAD simulation of LDMOS transistors

Several physical effects are observed in a DMOS transistor and these can be simulated in TCAD (Technology Computer Aided Design). The key effects will be presented and discussed in the context of TCAD, illustrating how this can be applied to help develop models for circuit simulation programs.

5.1 Capacitance behaviour of LDMOS transistors

A main figure of merit for a good LDMOS model is the accuracy of the modelled capacitances, as these devices are often used in switching applications.[1] Therefore an analysis of the capacitances for real-life bias conditions is necessary. Often the capacitances are shown at a drain voltage equal to zero. However, when the LDMOS is used in an application, the drain and gate voltage will be higher than zero. The capacitances have been analysed both by TCAD simulations and measurements (described in chapter 6). A schematic cross-section can be seen on Figure 5.1 and a TCAD simulated cross-section can be seen on Figure 5.2.

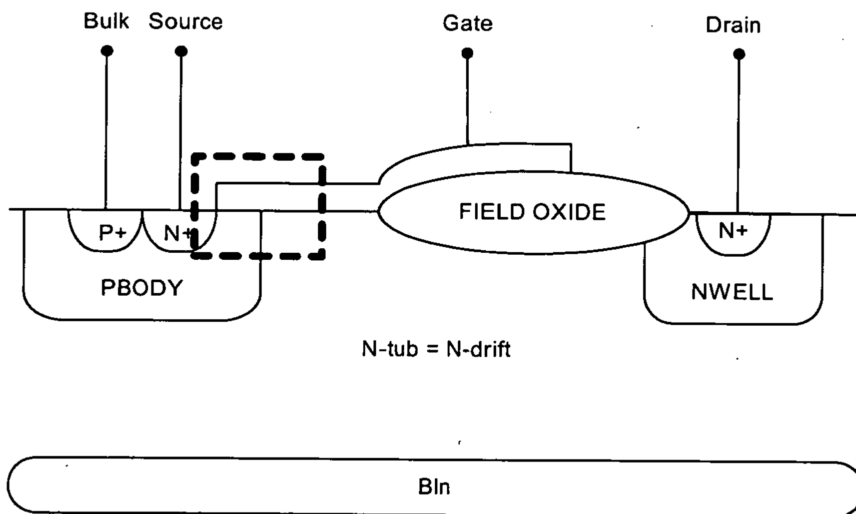


Figure 5.1 Schematic and TCAD cross-section view. The black dotted square indicates the region highlighted in the graphs on page 53.

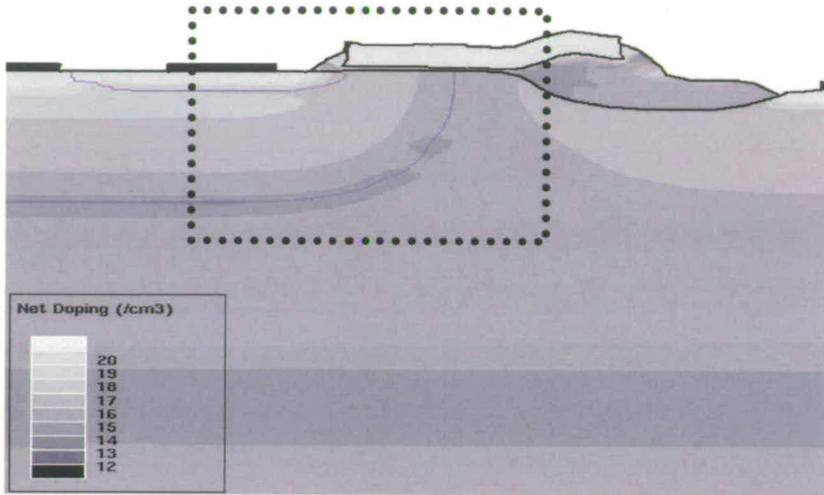


Figure 5.2 Schematic and TCAD cross-section view. The black dotted square indicates the region highlighted in the graphs on page 53.

5.1.1 Comparison of TCAD simulations with measurements

Figure 5.3 compares simulated and measured capacitance characteristics. A good agreement is observed. The good agreement between measurement and simulations allows us to accept the results obtained by TCAD simulations. The remarkable feature in Figure 5.3 is the peak in C_{gd} around the threshold voltage as has been reported in [2] . Conventional MOSFETs do not show such a peak in C_{gd}

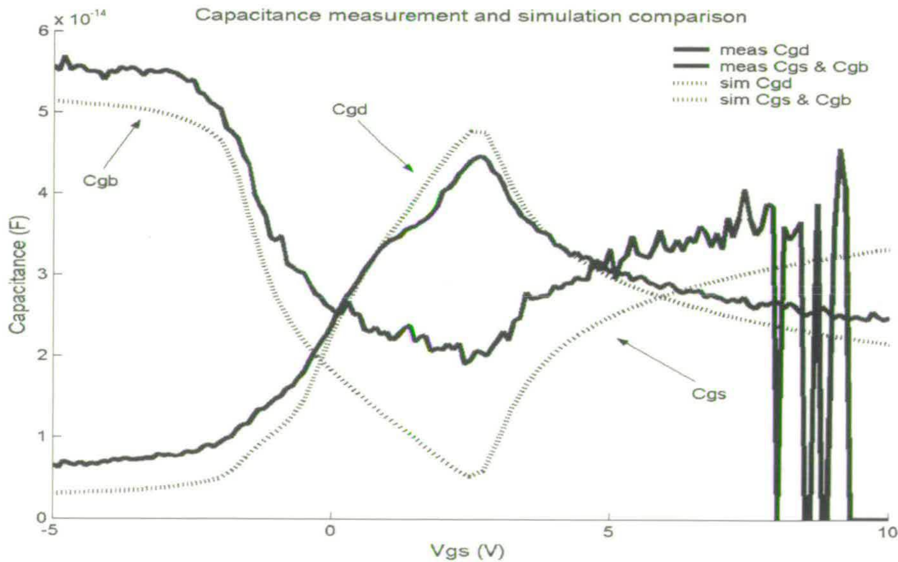


Figure 5.3 Comparison between measurements and simulations at V_{ds} = 0V. Some measurement noise in the data is observed on the C_{gs} curve at higher gate voltages

5.1.2 Capacitances when $V_{DS} = 0V$

5.1.2.1 Gate - source capacitance (C_{gs})

Following the simulated C_{gs} curve from negative to positive gate voltage up to the threshold voltage on Figure 5.4, the gate-source capacitance remains low. This corresponds to the capacitance from the gate overlap over the n^+ source region, plus the fringe capacitance from the gate sidewall. The capacitance remains at this value until the p-body is inverted. When this happens there is a conducting path underneath the whole gate, leading to an increase in capacitance. The final value at $V_{GS}>0$ is however not the oxide capacitance corresponding to the total gate-length. This is due to the fact that part of the signal is collected by the drain and does not contribute to C_{gs}. The final value of C_{gs} will then be dependent on the resistance in the signal path, over the drain and source respectively [3].

5.1.2.2 Gate - body capacitance (C_{gb})

The C_{gb} curve starts at a high value where the signal current is collected by the hole sheet that spans over the p-body to the drain. (See Figure 5.4) The signal is, however not shunted to ground by the drain because of the depletion region. When the gate-voltage increases, the C_{gb} curve falls rapidly as the drain leaves strong inversion and the signal is only collected by the accumulated hole sheet at the p-body. As the gate-voltage increases further, the p-body begins to deplete, leading to a progressive decrease in capacitance until the p-body reaches inversion. The capacitance will then become virtually zero since the signal is shunted to ground by the source and drain [3].

5.1.2.3 Gate - drain capacitance (C_{gd})

For the same reason as for C_{gs} the C_{gd} curve starts at zero since the signal is shunted to ground by the p-body as (see Figure 5.4) the capacitance will remain zero until the drain leaves inversion and the p-body can no longer supply the drain with carriers through the hole sheet. The capacitance then rises to approximately the drain oxide capacitance in series with the drain depletion capacitance and then approaches a constant value. There will however be an inversion tail close to the p-body due to the built-in potential at the pn-junction thereby reducing the capacitance. As the gate voltage increases, this tail will vanish and the level of depletion decreases, leading to an increase in the C_{gd} curve again. The curve will peak as the gate voltage approaches the threshold voltage of the p-body. As the p-body becomes strongly inverted, the signal is shunted through the

electron sheet to the source ground. The final value is then dependent on the resistance in the signal path, over the drain and source respectively [3].

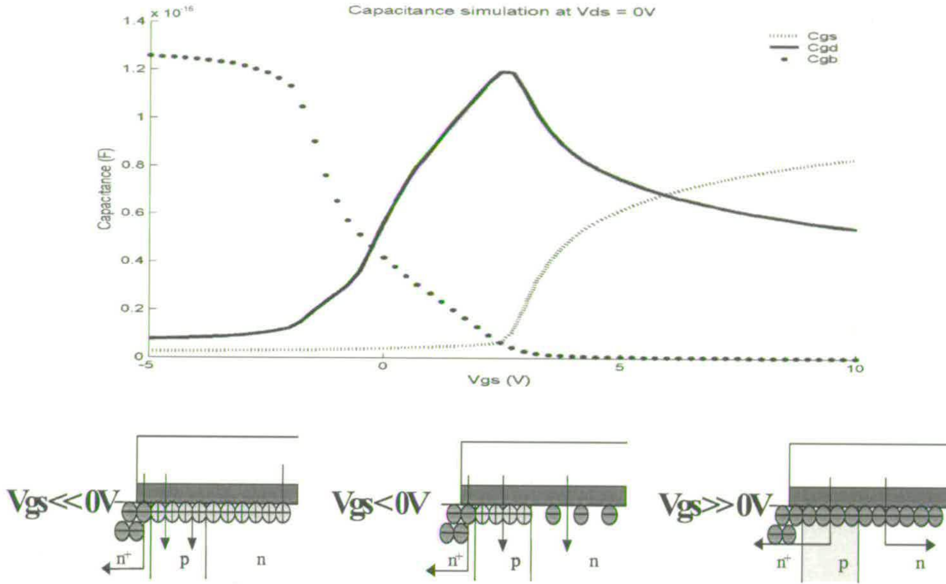
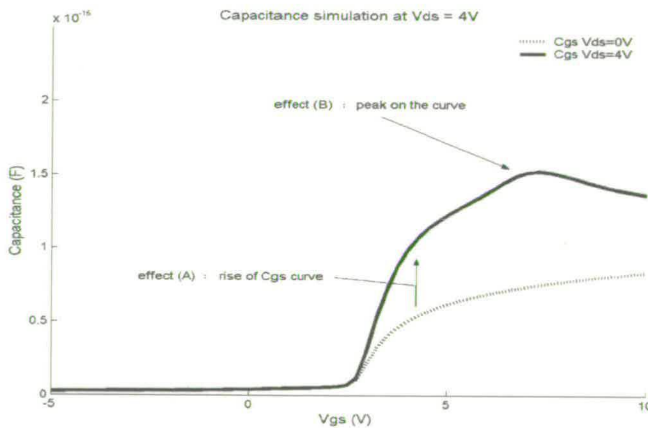


Figure 5.4 C_{gs}, C_{gb} and C_{gd} at V_{ds} = 0V

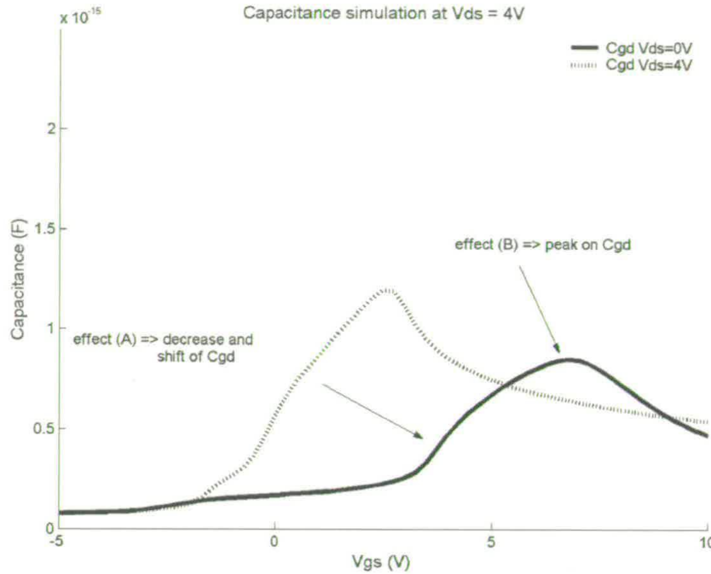
5.1.3 C_{gs}, C_{gb} and C_{gd} when V_{DS} > 0V

Using TCAD simulations, the analysis of C_{gd} and C_{gs} was extended to non-zero drain biases. [4]



Cgs at Vds = 0V and Cgs at Vds = 4V

Figure 5.5 (a) Cgs and Cgd when Vds > 0V



Cgd at Vds = 0V and Cgd at Vds = 4V

Figure 5.5 (b) Cgs and Cgd when Vds > 0V

When the drain voltage is non-zero, two effects occur ((A) and (B)) as shown in figure 5.5.

5.1.3.1 Depletion region in the drift region under the gate : effect (A)

When the drain voltage is higher than zero a depletion region is formed at the p-body / n-tub junction, extending mainly in to the lowly doped n-tub region. At V_{GS} = 0V the N_{tub} region under the gate is depleted (Figure 5.6). The charges under the gate are controlled by the p-body. When V_{GS} is increased one can see that C_{gs} is higher compared to the V_{DS} = 0V case (Figure 5.5). This is due to the fact that the p-body is already inverted (channel to the source) but there still exists a depletion region under a part of the gate in the drift region. The charges under the gate in the drift region are now controlled by the source, explaining the increase in C_{gs} (Figure 5.6). When the depletion region under the gate in the drift region disappears, charges will be distributed over the source and the drain, giving rise to C_{gd} (Figure 5.5). When V_{GS} increases further, a signal path under the oxide is created (Figure 5.6).

FN-LDMOS; V_{DS} =10V; Electron Concentration

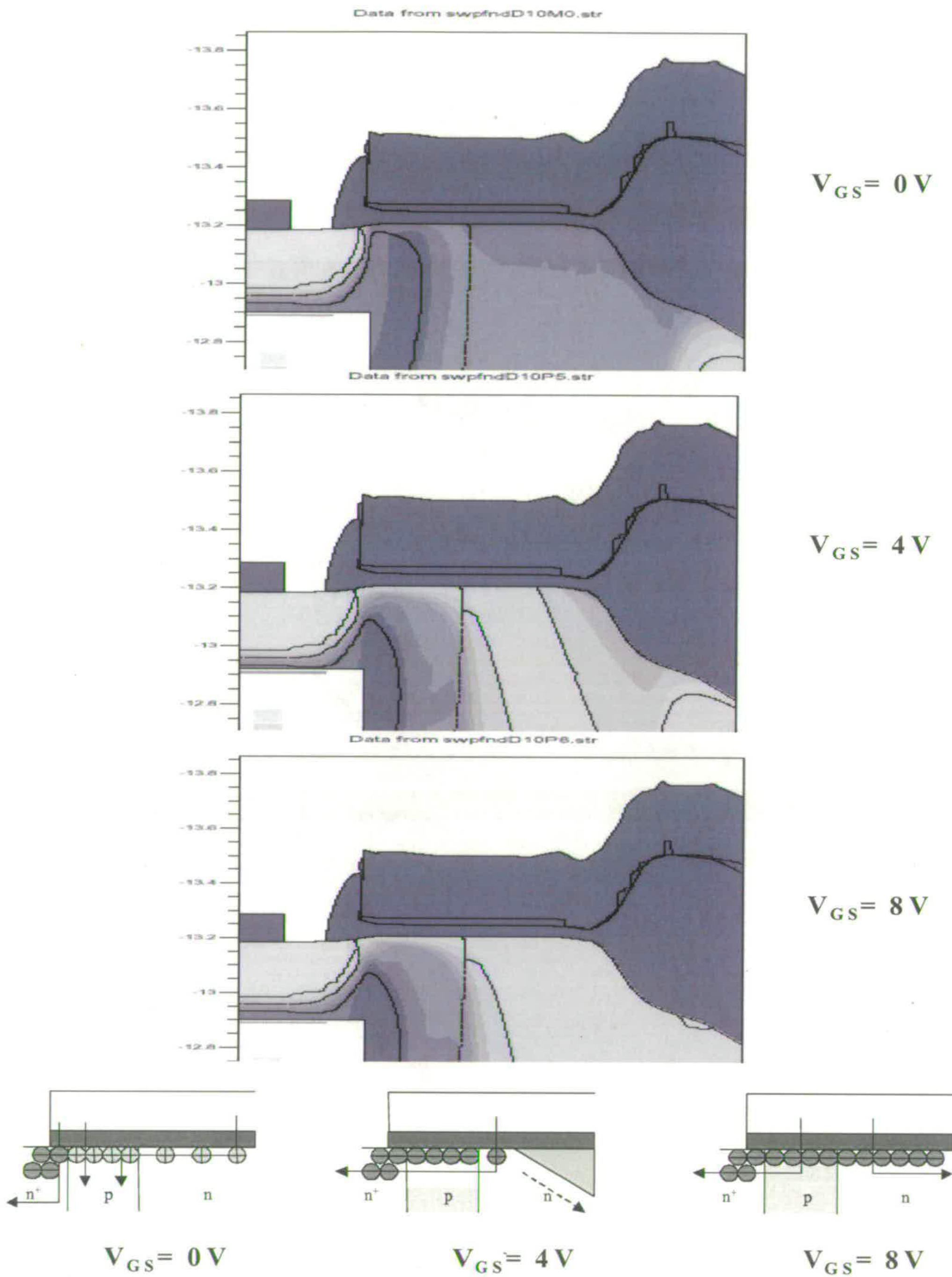


Figure 5.6 Depletion region in the drift region under the gate

5.1.3.2 Sensitivity of p-body/n-tub junction to V_{GS}: effect (B)

When V_{GS} rises, a drop in the potential at the p-body / n-tub junction (internal drain node) is observed. This drop in voltage is caused by the channel going from saturation to linear regime causes.

When a small signal is applied, the width of the depletion region will change. As the source (in linear regime) can now provide charges at the n-tub plate of the junction, a rise in C_{gs} appears. As a consequence charges at the bulk plate will be attracted, giving rise to C_{gb} (Figure 5.7 and Figure 5.5(b)).

When V_{GS} rises further a "full" signal path will be created under the oxide, which will shield the junction.

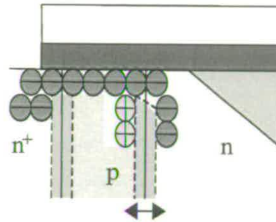


Figure 5.7 Sensitivity of p-body/n-tub junction to V_{GS}

5.2 Intrinsic drain voltage (V_K) behaviour in relation to gate and drain voltage

The intrinsic low-voltage MOS transistor is delimited by the source of the high voltage transistor and the end of intrinsic inversion channel (V_K is the potential of the boundary between the p-region and the extended drain n-region, V_{BB} is the potential at the Birds beak, see Figure 5.8).

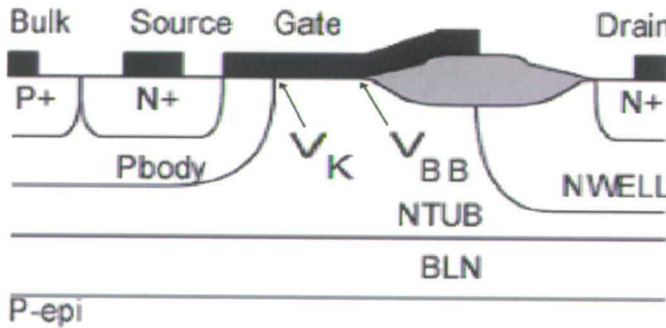


Figure 5.8: Cross section of an LDMOS indicating the location of V_K and V_{BB}.

TCAD simulation allows analysing the variation of V_K in all regions of transistor operation with respect to the gate and drain voltages. For these numerical simulations self-heating was not included; consequently its impact on device characteristics is not discussed. From Figure 5.9 one can see that V_K remains below 7V. The V_K-point can be seen as the drain of the channel region as the external drain of the device is swept up to

50V, therefore one can say that V_K remains at a low voltage, similar to that applied to normal MOS devices.

Based on this knowledge, a decision was made to use a standard low voltage model BSIM3V3.2, to model the intrinsic channel.

The analyses of V_K provides information on the operating region (linear / saturation) of the intrinsic MOS and the variation of the voltage drop over the drift region. Figure 5.9 shows the detailed behaviour of V_K as a function of V_{DS} and V_{GS}. A test-structure to measure and check these observations was developed, and is called MESDRIFT. This test-structure is discussed in detail in chapter 6.

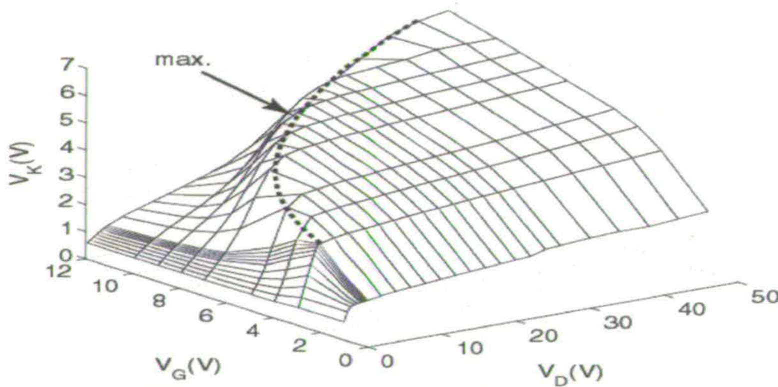


Figure 5.9 LDMOS channel voltage variation as a function of V_{GS} and V_{DS}

In previous publications [5][6], it has been shown that an analysis of the internal drain voltage (V_K) is a valid indicator to extract the drift region resistance behaviour. An explanation for the V_K behaviour was given based on an analysis of the depletion regions present in the LDMOS device. A correction of these findings was needed, as the potential distribution in the LDMOS transistor is not only determined by the voltages applied to the gate and drain, but also by the current density and associated space charge. The simulations in Figure 5.10 show the effect on V_K and V_{BB} of an open source (i.e. no current flowing in the device) compared to the normal condition (a grounded source with current flowing in the device). For $V_{GS} < V_T$, the transistor is off and the curves for open and grounded sources merge. V_K is linearly dependent on V_{GS} due to capacitive coupling of the gate. For the case when the source of the transistor is grounded, current starts to flow in the transistor from the moment V_{GS} exceeds V_T. The space charge associated with the majority carriers in the drift region will alter the potential distribution in the device, and hence also the V_K potential, provided the electron concentration is the same or exceeds the donor concentration in the drift region.

This is, in particular, true for LDMOS devices with a lightly doped drift region. It is evident from Figure 5.10 that without current flow in the device, V_K monotonically increases as a function of V_{GS}, whereas in real operating conditions (source grounded), the V_K potential starts to diverge from this as soon as $V_{GS} > V_T$. For some biasing conditions, the V_K potential even starts to decrease. Clearly, the effect of the current flow has a large effect on the V_K potential, and as such needs to be taken into account when evaluating V_K.

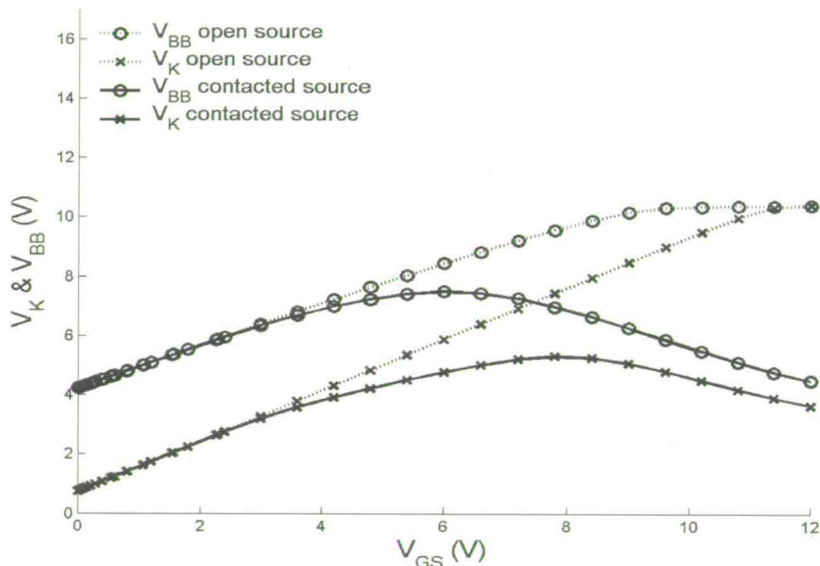


Figure 5.10. V_K and V_{BB} as a function of V_{GS} with source closed and open at V_{DS} = 10V.

An analysis of the potential, current flow and space charge has been performed using 2D device simulations. The resulting space charge simulations are presented in Figure 5.11, with the length of the accumulation layer identified as L_{acc} and the length between the channel and the field oxide being denoted by $L_{overlap}$. It can be seen that for $V_{GS} > V_T$, part of the lowly doped n-type region under the gate oxide forms an accumulation layer where the current flows. This accumulation layer becomes larger for increasing V_{GS} and at approximately V_{GS}=7V, it reaches the tip of the bird's beak (see Figure 5.11(b)). From this point on ($L_{acc} > L_{overlap}$), the lateral extension of the accumulation layer is less dependent on V_{GS} because of the thicker field oxide, which forms the bird's beak, resulting in less gate coupling.

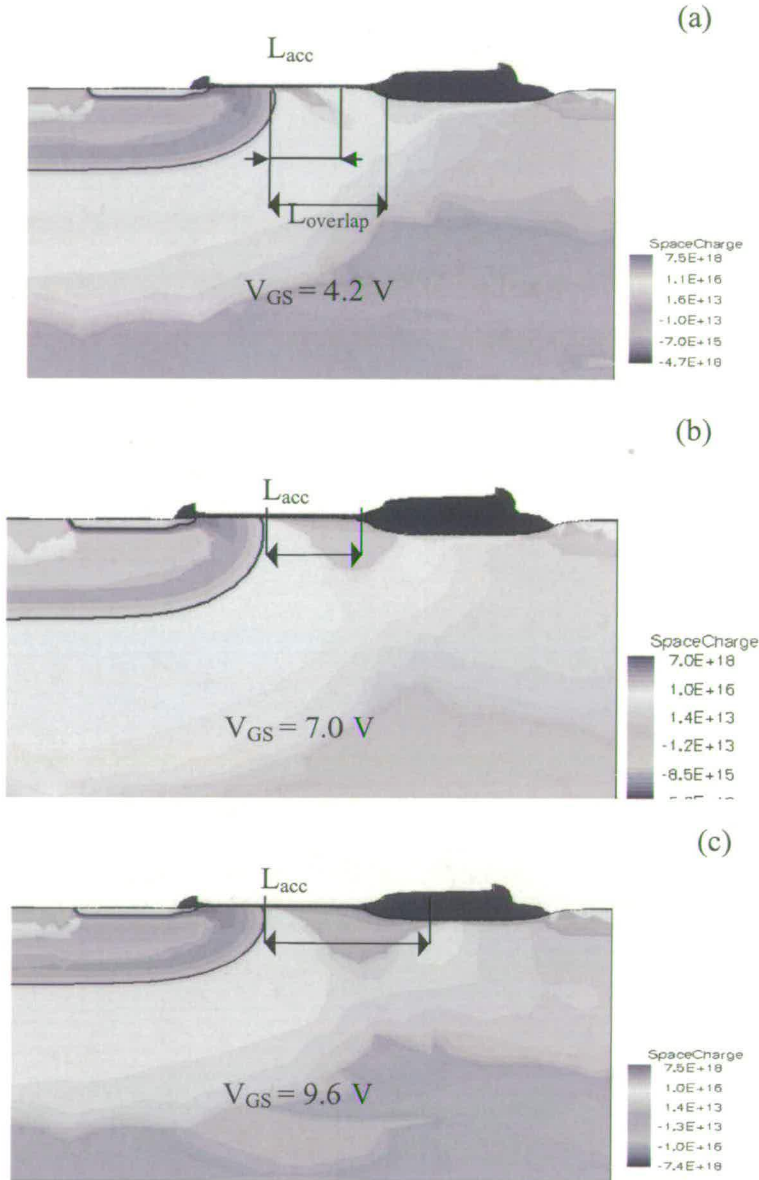


Figure 5.11. Space charge behaviour for different bias conditions: (a) V_{GS} = 4.2V ; (b) V_{GS} = 7.0V ; (c) V_{GS} = 9.6V. For all simulations V_{DS} was set to 10V.

To explain the V_K and V_{BB} behaviour, it is instructive to plot the contributions of the channel, accumulation and field oxide drift regions to the total resistance. This is presented in Figure 5.12 as a function of V_{GS}, for V_{DS}=10V. This shows the channel resistance decreases monotonically with increasing V_{GS}. The field oxide drift resistance decreases with V_{GS} until the space charge region reaches the tip of the bird's beak (at around V_{GS} = 7V). Further increases in V_{GS} show that the gate control on the field oxide drift region then becomes very small, and as such the field oxide drift resistance saturates. A similar saturation is observed for the accumulation region, but at a higher V_{GS}. This can be explained by the higher gate coupling (thin oxide) of the accumulation

region. In the end, the channel resistance also starts to saturate. These three contributions to the total transistor resistance determine the V_K and V_{BB} potential in the device, as the channel, accumulation and field oxide drift resistors are in series and hence act as a voltage divider. For example, inspection of the potential at the bird's beak (V_{BB}), shows that the field oxide drift resistance completely saturates when $V_{GS} > 7V$, whereas both the channel and the accumulation resistance decrease further for increasing values of V_{GS}. A larger potential drop occurs over the field oxide drift resistor, and hence the V_{BB} potential will start to decrease as can be observed in Figure 5.10. A similar explanation holds for the V_K potential due to saturation of the accumulation layer resistance, at a higher V_{GS} voltage (see also Figure 5.10).

The dependence of V_K and V_{BB} on V_{DS} is straightforward. When V_{DS} is increased, a wider depletion layer is formed between the P-body and N-tub regions. As a result of the larger depletion width, a higher gate voltage is needed to accumulate the lowly doped n-type region under the gate oxide. As V_{DS} increases, the maximum value of V_K shifts to a higher V_{GS}.

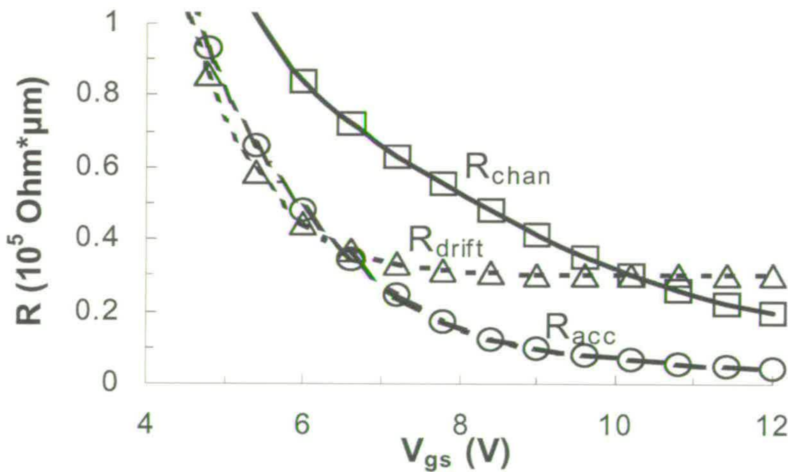


Figure 5.12. Variation of the channel, accumulation and field oxide drift region resistance (R_{chan}, R_{acc} and R_{drift}) as a function of V_{GS} (V_{DS}=10V).

5.3 Conclusion

By performing TCAD simulations, a better insight into the "internal" device behaviour has been obtained. The main achievement is a good understanding of the capacitance behaviour of an LDMOS at typical operating bias conditions (V_{DS} > 0V). This information has proven to be very helpful when developing the AC-model.

Another interesting analysis was that of the internal drain behaviour V_K. The analyses of V_K have provided information on the behaviour of the drift region. A good LDMOS macro-model should mimic this behaviour to have all its components remaining at physical bias conditions.

References:

[1] N. Mohan, T.M. Undedrland, W.P. Robbins, "Power electronic Convertors, pplications and design," John Wiley & Sons, 1995, 2nd edition.

[2] Olsson, J., Valtonen, R., Heinle, U., Vestling, L., Soderbarg, A., Norde, "A Capacitance-Voltage Measurement Method for DMOS Transistor Channel Length Extraction," IEEE Int. Conference on Microelectronic Test Structures, Mar 1999, pp. 135-140.

[3] E.C.Griffith, S.C.Kelly, J.A.Power, D.Bain, S.Whiston, P.Elebert, M.O'Neil, "Capacitance Modelling of LDMOS Transistors," IEEE Solid-State Device Research Conference, Sep 2000, pp. 624-627.

[4] S.F. Frère, J. Rhayem, H.O. Adawe, R. Gillon, M. Tack, and A.J. Walton, "LDMOS Capacitance Analysis versus Gate and Drain Biases, Based on Comparison between TCAD Simulations and Measurements," ESSDERC 2001 Proc. , Sep. 2001, pp. 219-223.

[5] N. Hefyene, C. Anghel, A.M. Ionescu, S. Frère, R. Gillon, M. Vermandel, B. Bakeroot and J. Doutreloigne, "An experimental approach for bias-dependent drain series resistances evaluation in asymmetric HV MOSFETs," ESSDERC 2001 Proc. , Sep. 2001, pp.403-406.

[6] C. Anghel, N. Hefyene, A.M. Ionescu, S. Frère, R. Gillon, M. Vermandel, B. Bakeroot and J. Doutreloigne, C. Maier, Y. Mourier, "Investigations and physical modelling of saturation effects in Lateral DMOS transistor architectures based on the concept of intrinsic drain voltage," ESSDERC 2001 Proc. , Sep. 2001, pp.399-402.

Description and results of the test-structures developed for the analyses and characterization of LDMOS devices

6 Description and results of the test-structures developed for the analyses and characterization of LDMOS devices 63

6.1 Introduction 63

6.2 Introduction to the MESDRIFT test-structure 63

6.2.1 The MESDRIFT test-structure: device, DC experiments and numerical simulations 64

6.2.2 DMOS temperature dependence with the MESDRIFT test-structure 68

6.2.3 Self heating characterization with the MESDRIFT test-structure. 71

6.2.4 Hot carrier investigations with the MESDRIFT test-structure 72

6.2.5 Conclusion of MESDRIFT structure 73

6.3 W-array test-structures: 74

6.4 Junction diode test-structure 76

6.5 RF-measurement test-structure 78

6.6 Introduction to capacitance extraction based on s-parameter measurements 79

6.6.1 The definition of S-parameters 79

6.6.2 Characteristic S-parameter values 82

6.6.3 Understanding the Smith chart 83

6.7 Capacitance calculation for a LDMOS transistor from measured s-parameters. 87

6.7.1 Measurement set-up 87

6.7.2 Conversion from Y-parameters to Cgs, Cgd and Cgb capacitances. 87

6.8 Conclusion 89

6.9 References: 89

6 Description and results of the test-structures developed for the analyses and characterization of LDMOS devices

6.1 Introduction

Test-structures are devices or a set of devices, used to analyse or verify a certain part of the device behaviour. This chapter describes the different test-structures that were developed and used for building-up and extraction of the macro-model. These test-structures and test-devices are designed so that they can be used to characterise either some of the behaviour observed from the TCAD simulations, or the complete device itself.

6.2 Introduction to the MESDRIFT test-structure

Among the most critical issues for accurate design, modelling and simulation of LDMOS transistors are the bias-dependent characteristics of the drift region and their impact on the overall transistor performance. Especially, the bias-dependent drift resistance (origin of quasi-saturation phenomena) and the C_{GS} and C_{GD} capacitances are the source of crucial interest for modelling and characterisation.

A new test-structure, MESDRIFT, has been developed. The MESDRIFT test-structure can provide useful information about temperature influence, self-heating and hot-carrier stress. This test-structure and extraction method was developed together with the Swiss Federal Institute of Technology Lausanne, Electronics Laboratory, Switzerland. (EPFL)[1]

6.2.1 The MESDRIFT test-structure: device, DC experiments and numerical simulations

The MESDRIFT test-structure and the DC measurement set-up are depicted in Figure 6.1

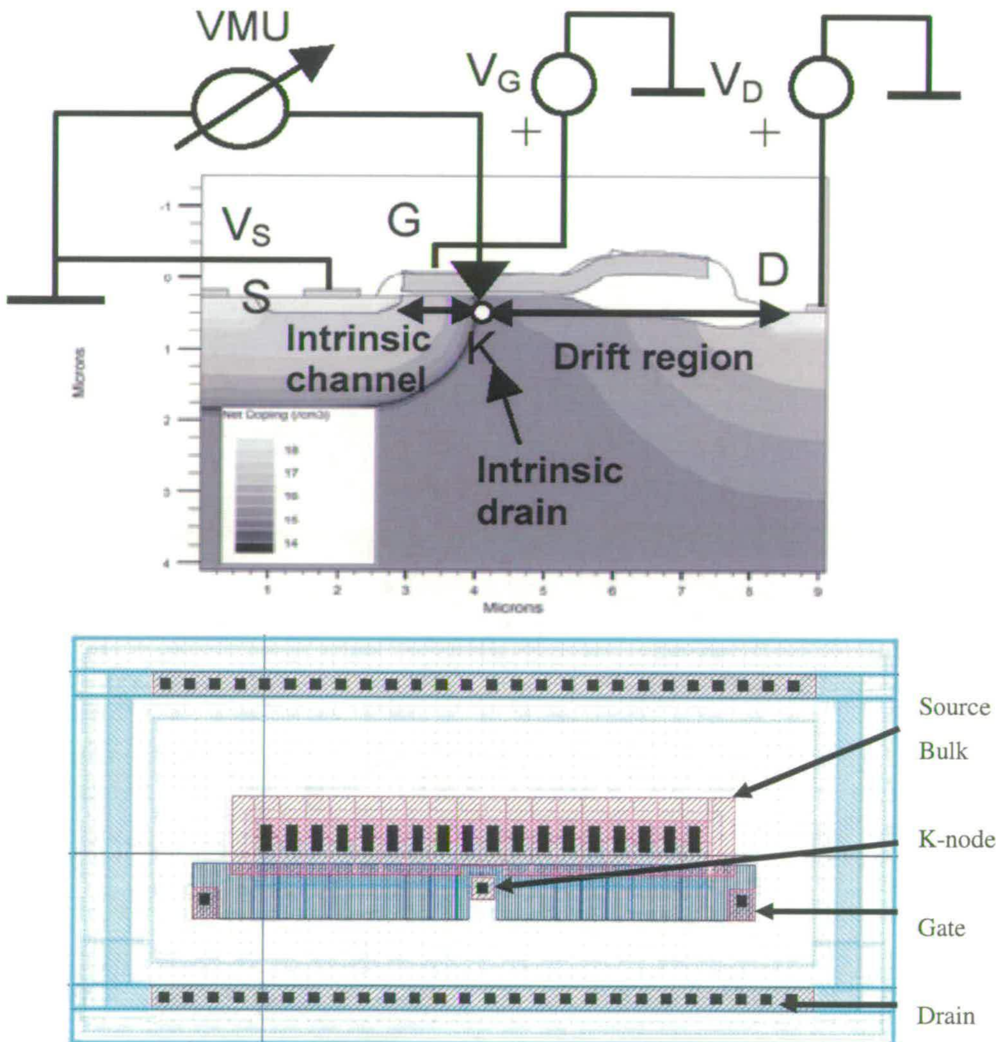


Figure 6.1 Cross section of MESDRIFT test structure and associated HP4156 measurement set-up. K-contact (n+ type) is designed in the drift region (close to pn junction) and its width, WK, is negligible compared to DMOS width, W.

The MESDRIFT test-structure reproduces the architecture of an XDMOS, with the key difference that a small contact is smartly engineered in the drift region, near the end of the MOS channel. This K-contact is designed for probing the intrinsic drain voltage, V_K

(at the end of the intrinsic channel), without significantly impacting the electrical characteristics of the overall HV MOS device. As demonstrated in Figure 6.2, this is successfully achieved when the device width, W, is much larger than the size of the K-probe contact. Due to the introduction of the K-contact a higher impact ionisation rate is observed in the lower Vgs range.

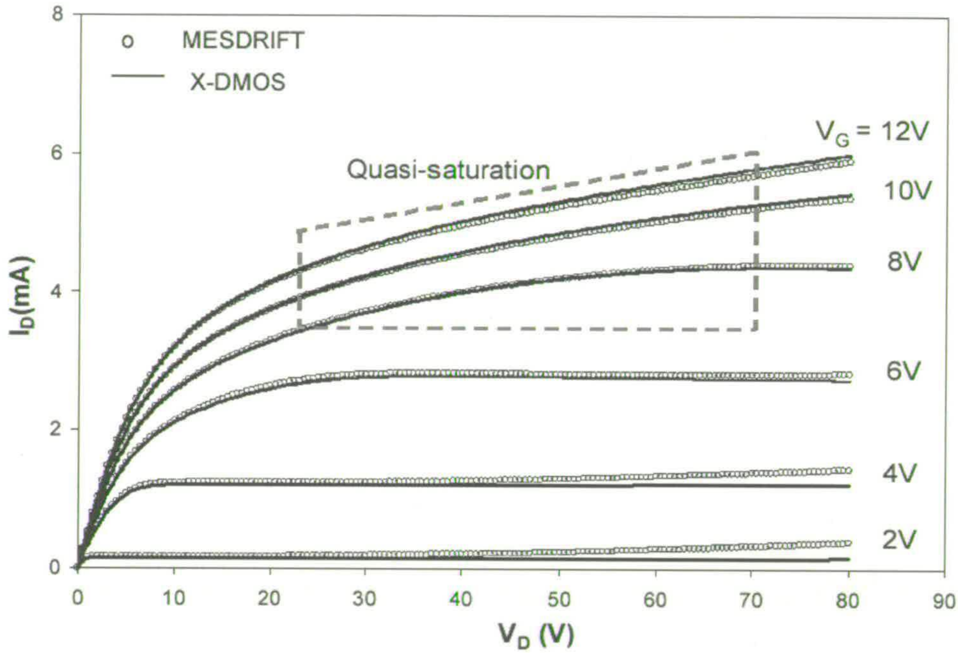


Figure 6.2 Typical output characteristics, I_{DS} vs. V_{DS}, of X-DMOS (solid) and MESDRIFT (symbol) (both with W=40 μm): very good agreement is observed (including quasi-saturation region) demonstrating that the K-contact does not significantly change the HV MOSFET characteristics.

Figure 6.3(a) depicts the I_{DS}-V_{GS} characteristics of the intrinsic and extrinsic MOS devices at the same equivalent drain voltage (V_{DS}=V_K) that captures the effect of the drift bias-dependent series resistance, R_{drift}, on the DC characteristics. At low drain voltage and uniquely based on the difference between the coefficients of mobility reduction with the transverse field in intrinsic and extrinsic channels, the R_{drift}-parameter is deduced, Figure 6.3(b).

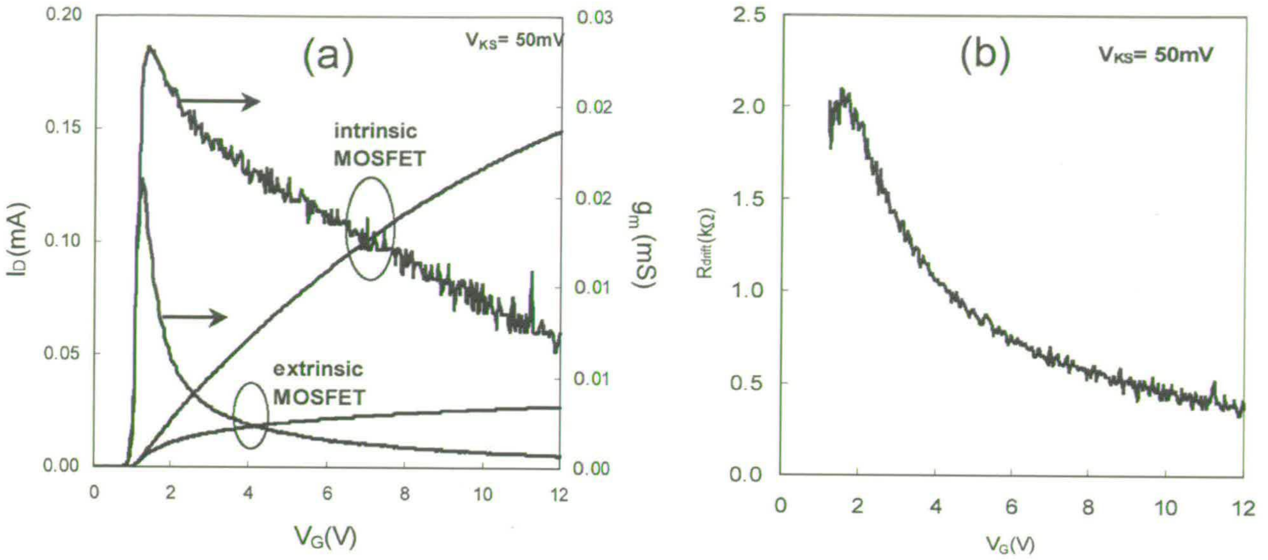


Figure 6.3 a) Intrinsic and extrinsic I_{DS}-V_{GS} and gm-V_{GS} at V_{KS}=V_{DS}=50mV, measured with MESDRIFT mirroring X-DMOS, b) Extracted Rdrift at low V_{DS} (=50mV).

For extended analysis over all the operation range (including quasi-saturation), the V_K dependence on external V_{GS} and V_{DS}, is presented in Figure 6.4.

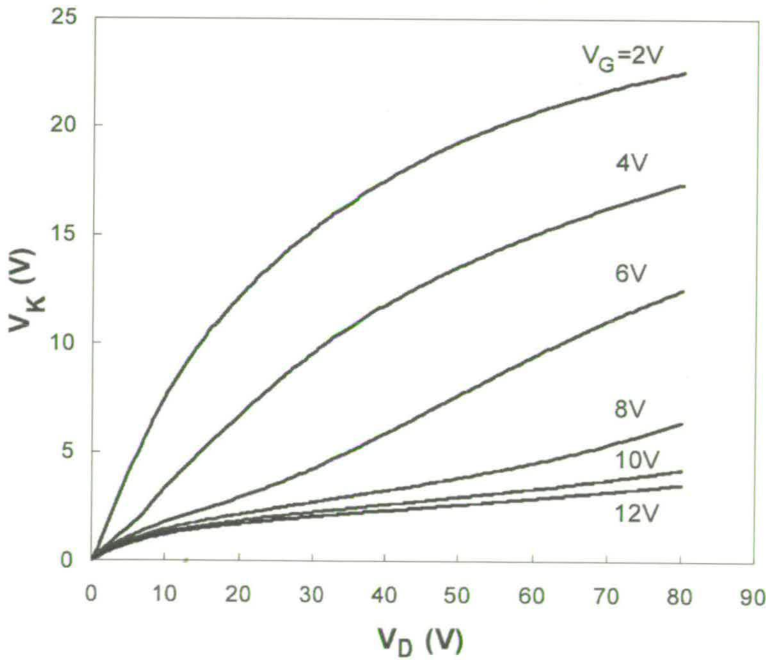


Figure 6.4 Intrinsic drain (key) voltage, V_K, vs. V_{DS} with V_{GS} as parameter, experimentally revealed by MESDRIFT.

The overall Rdrift as a function of V_G and V_D shown in Figure 6.5, is extracted based on the drift voltage drop, $V_{drift}=V_D-V_K$ at a given injected drain current, I_{DS}.

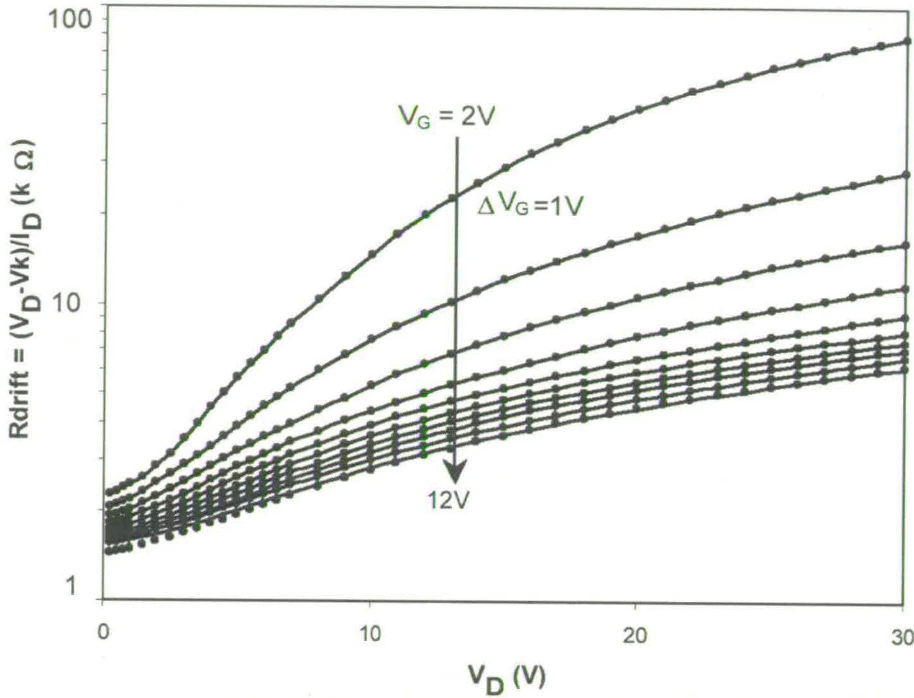


Figure 6.5 Drift resistance, R_{drift} vs. V_{DS} for a range of V_{GS}, as experimentally extracted with MESDRIFT (X-DMOS) at room temperature

Thus, for the first time, the experimental Rdrift variation with the device bias is experimentally accessible over the full operation range and the two-decade variation that has been reported is explained by the drift depletion control by V_{GS} and V_{DS}, and by the formation of an accumulation layer under the extension of the thin oxide. Numerical simulation (Figure 6.6) has been used to extensively validate the results obtained with the MESDRIFT test-structure; very good qualitative agreement is obtained and the quantitatively higher V_K extracted for fabricated MESDRIFT test-structures is related to a non-zero distance between the K-contact and the end of the intrinsic channel.

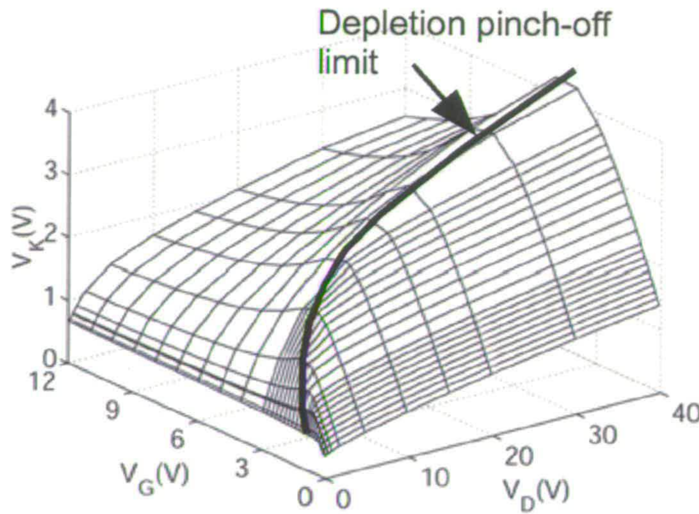


Figure 6.6 Intrinsic drain voltage, V_K, predicted by numerical simulation with calibrated 2D structure, calibrated on X-DMOS characteristics. Inset: drift depletion pinch-off limit highlighted.

In analogue operation (low V_{DS} and V_{GS}), Rch and Rdrift are comparable, while for large V_{GS} and/or V_{DS} (>5V), Ron is dominated by Rdrift. This highlights how critical the accuracy of Rdrift extraction is for precise modelling of LDMOS devices.

6.2.2 DMOS temperature dependence with the MESDRIFT test-structure

The MESDRIFT test-structure behaviour has been investigated over the range of 25°C to 150°C by monitoring the evolution of key parameters of the intrinsic MOSFET (threshold voltage, low field mobility, subthreshold swing, etc.). These are shown in Figure 6.7 and Figure 6.8.

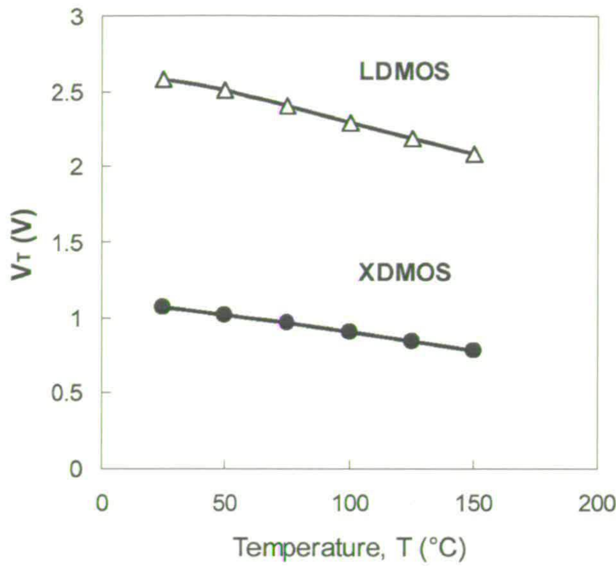


Figure 6.7 Threshold voltage, V_T, vs. temperature, T, for X- and L-DMOS.

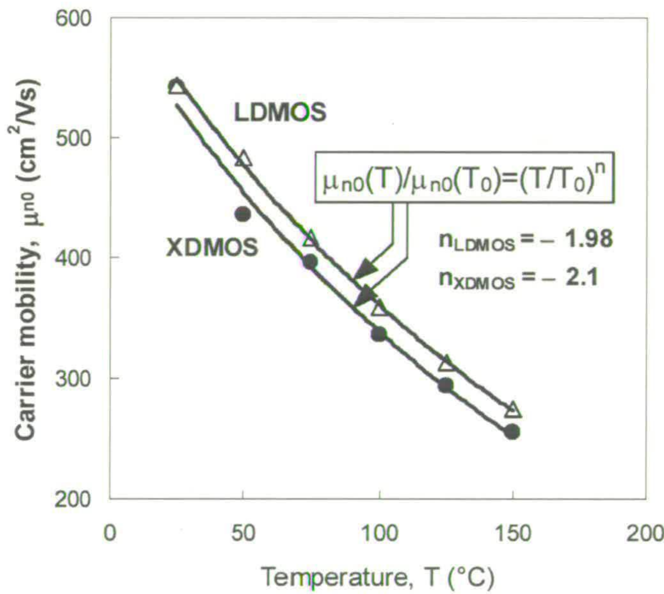


Figure 6.8 Low field mobility, μ_{n0}, vs. temperature, T, for X- and L-DMOS.

Typical signatures of measured DMOS transistors in terms of the temperature coefficients of mobility have been extracted (n = -2,) as shown in Figure 6.8. Rdrift vs. temperature at various bias conditions is shown in Figure 6.9. This analysis enables a good thermal behaviour of the drift resistance to be developed.

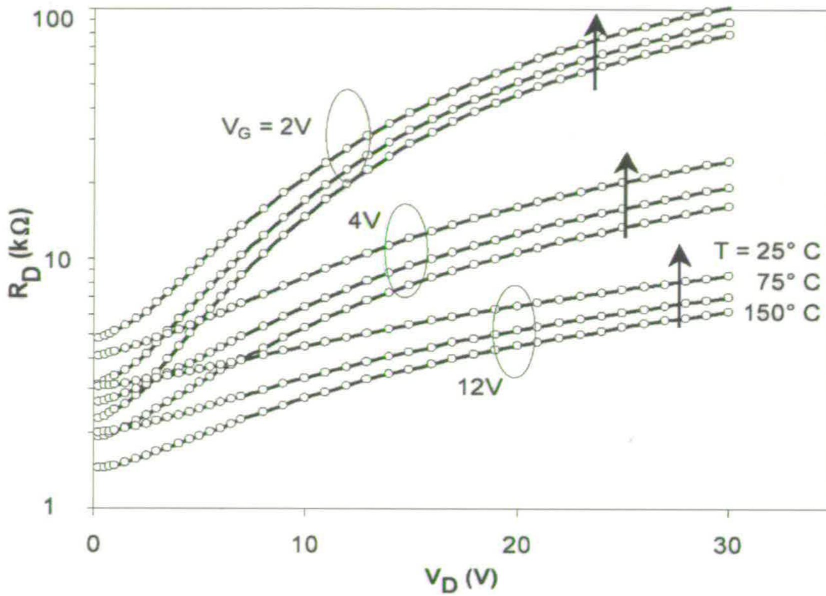


Figure 6.9 Rdrift (R_D) vs. V_{DS} at constant V_{GS} with the temperature, T, as a parameter.

From Figure 6.10 it can be observed that the influence of the temperature in terms of Rdrift/Ron is significant. The magnitude of the temperature effect is masked in Figure 6.10 due to the high V_{GS} dependency of the Rdrift.

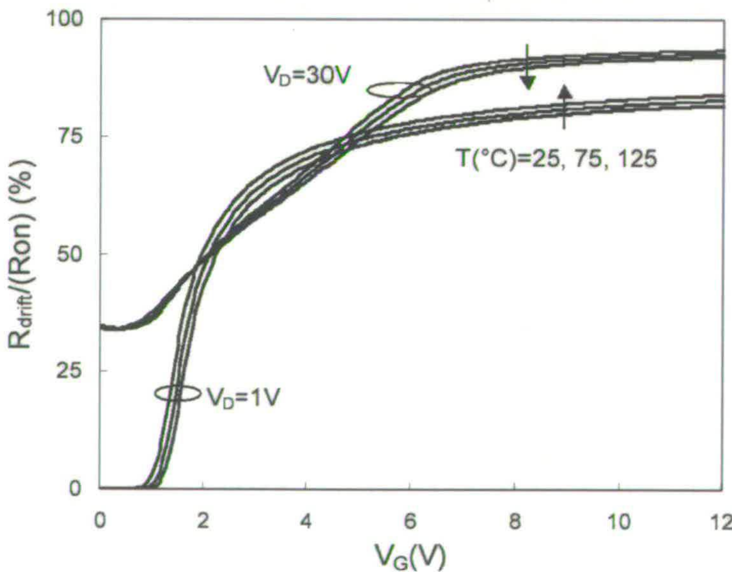


Figure 6.10 Influence of temperature on Rdrift/Ron characteristics revealed by MESDRIFT.

These results have demonstrated that by a simultaneous, yet separate, calibration of the intrinsic MOSFET excellent accuracy can be achieved.

6.2.3 Self heating characterization with the MESDRIFT test-structure.

Transients and self-heating effects of DMOS transistors with the MESDRIFT test-structure are briefly presented in Figure 6.11 and Figure 6.12.

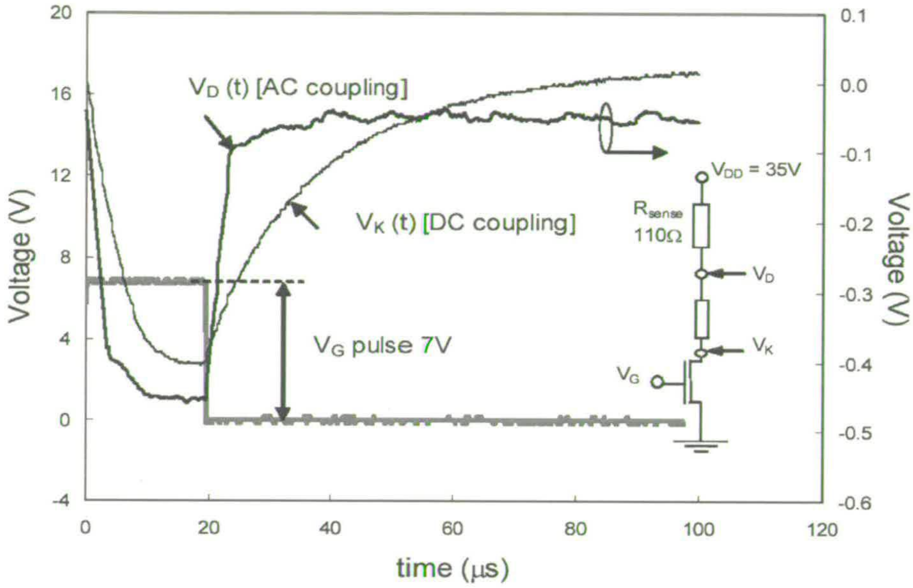


Figure 6.11 Dynamic behaviour of MESDRIFT (X-DMOS) highlighted by a simple pulsed measurement set-up designed to study self-heating in HV MOSFETs: V_{DS} and V_K time constants are different.

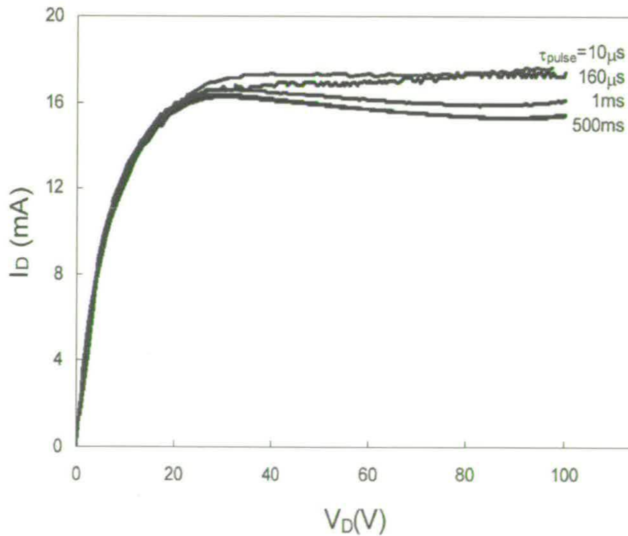


Figure 6.12 Effect of pulse duration on the reconstructed output characteristics (Vgs=12V) of X-DMOS. The self heating appears acceptably eliminated when t_{pulse} < 10 μs.

Both $V_{DS}(t)$ and $V_K(t)$ transients are recorded after abruptly switching V_{GS}, and compared in order to identify the best conditions for pulsed measurements in order to provide characteristics free of self-heating. For our DMOS devices, it is found that for a pulse duration of less than 10 μs acceptably eliminates self heating, as shown in Figure 6.12. These results will be used later on in this thesis to develop the approach to obtain self-heating free characteristics

6.2.4 Hot carrier investigations with the MESDRIFT test-structure

Another insight offered by the MESDRIFT test-structure concerns the hot carrier degradation of HV MOSFETs. Figure 6.13 and Figure 6.14 show how one can distinguish between drift region and intrinsic channel degradations using the MESDRIFT test-structure.

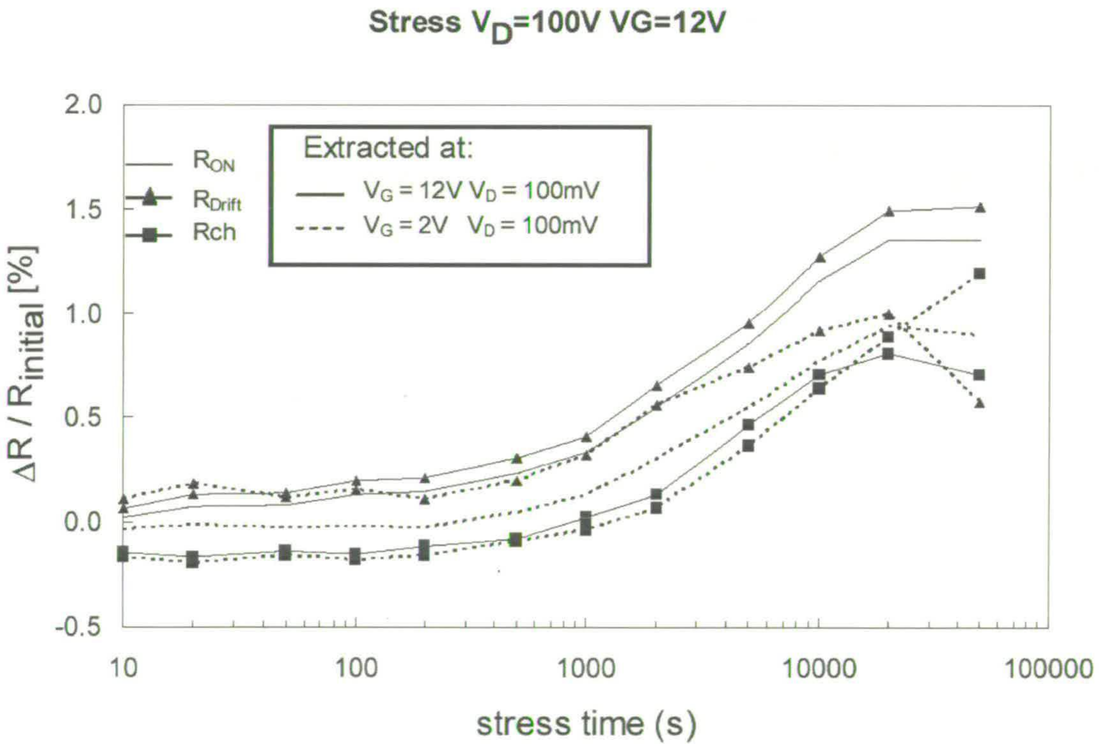


Figure 6.13 Degradations of Rch, Rdrift, Ron induced by hot carrier measurements conducted on MESDRIFT with V_{DS}=100V and V_{GS}=12V: Rdrift>0, Rdrift and Ron are similarly degraded.

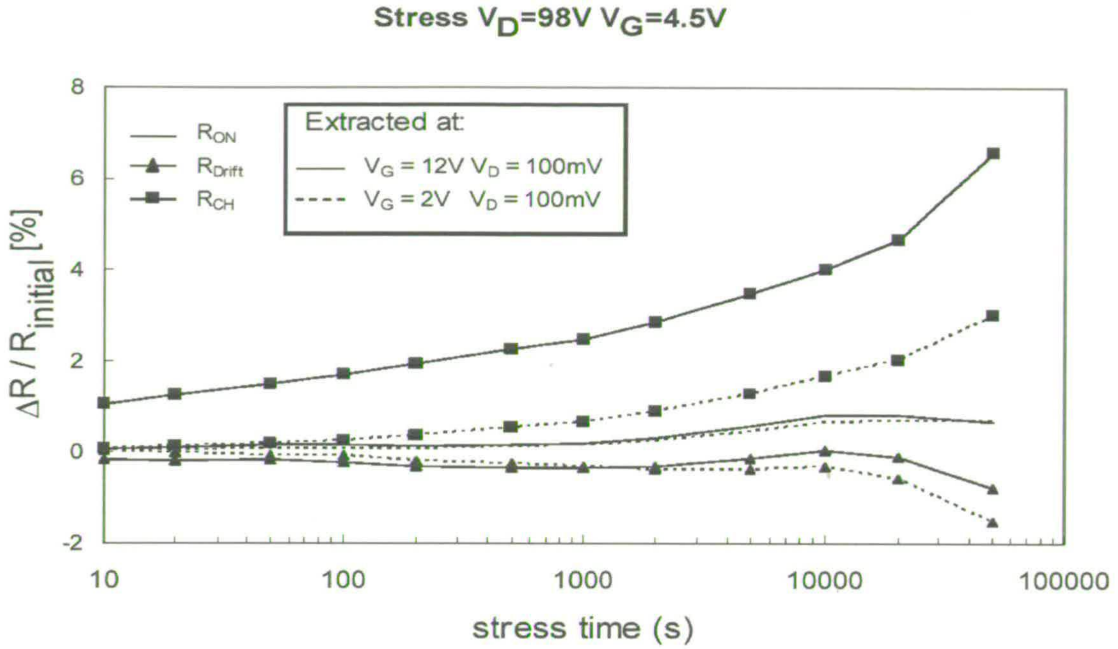


Figure 6.14 Degradations of Rch, Rdrift, Ron induced by hot carrier measurements conducted on MESDRIFT with V_{DS}=98V and V_{GS}=4.5V (at max Ibody): Rdrift<0, Rch is significantly more degraded than in Figure 6.13.

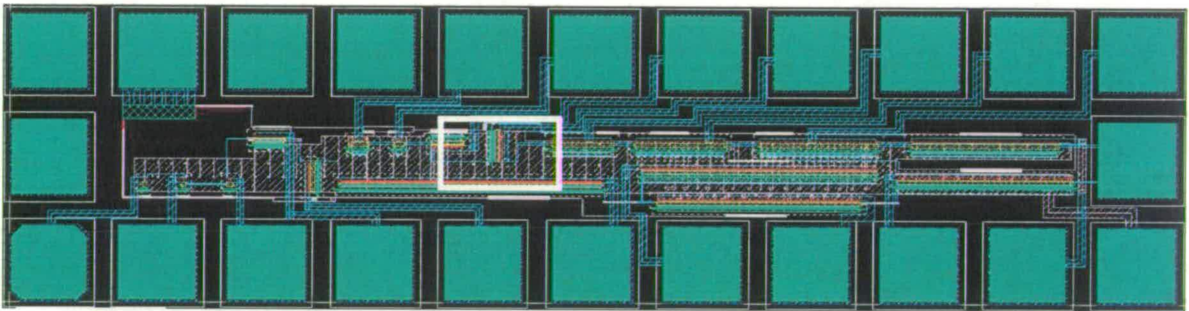
By comparing the stress impact on LDMOS devices with on the one hand (a) high V_{GS}, high V_{DS} and on the other hand (b) high V_{DS}, maximum of body current I_B, it was validated that in DMOS transistors the degradation can be assisted by both electron and/or hole injection as recently claimed in [5]. By comparing the results of Figure 6.13 and Figure 6.14, one can observe that Rdrift increases (Figure 6.13) or decreases (Figure 6.14) depending on the type of the stress (a or b) applied to the device. Furthermore, the MESDRIFT test-structure highlights that stress at I_{Bmax} results in more degradation of the intrinsic channel, compared with stress at V_{GSmax}. Finally, it should be noted that such detailed analysis of hot carrier degradation is almost impossible without the help of the MESDRIFT test-structure.

6.2.5 Conclusion of MESDRIFT structure

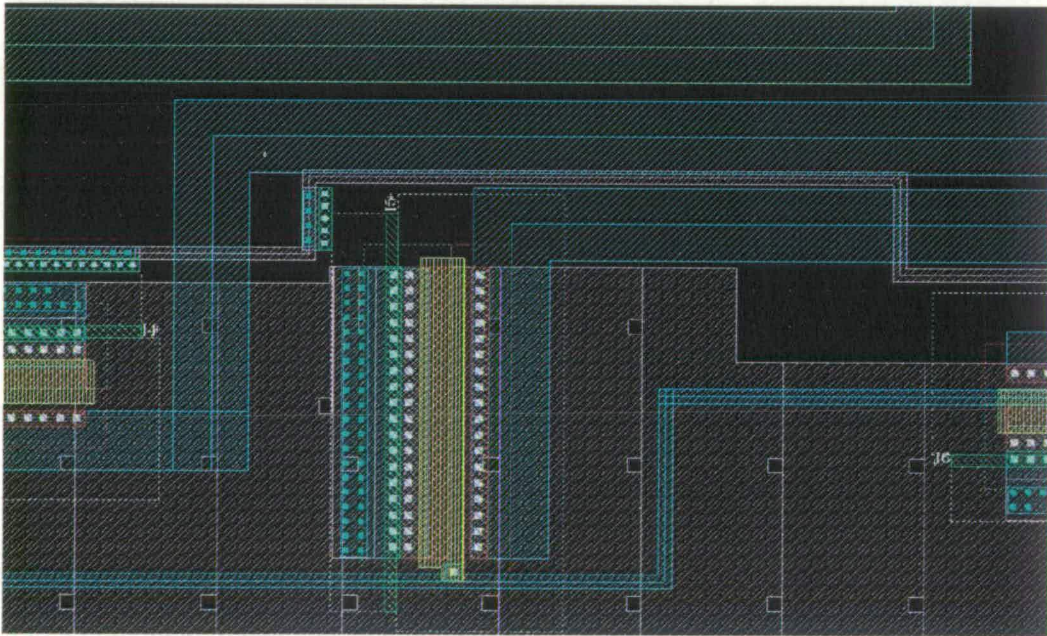
In conclusion, the MESDRIFT test-structure fully supports new DC and AC characterization methods that are simple, accurate and universal, because it is independent of the drift architecture of any asymmetrical HV MOSFET.

6.3 W-array test-structures:

The W-array test-structure consists out of an array of DMOS transistors with a range of widths. This test-structure is required for the DC model-extraction. The total width is varied from a few microns to several hundreds of microns. This width variation can either be achieved by either increasing the width of the individual device fingers or by increasing the number of fingers, i.e. by mirroring the device. An example can be seen in Figure 6.15.



(a)



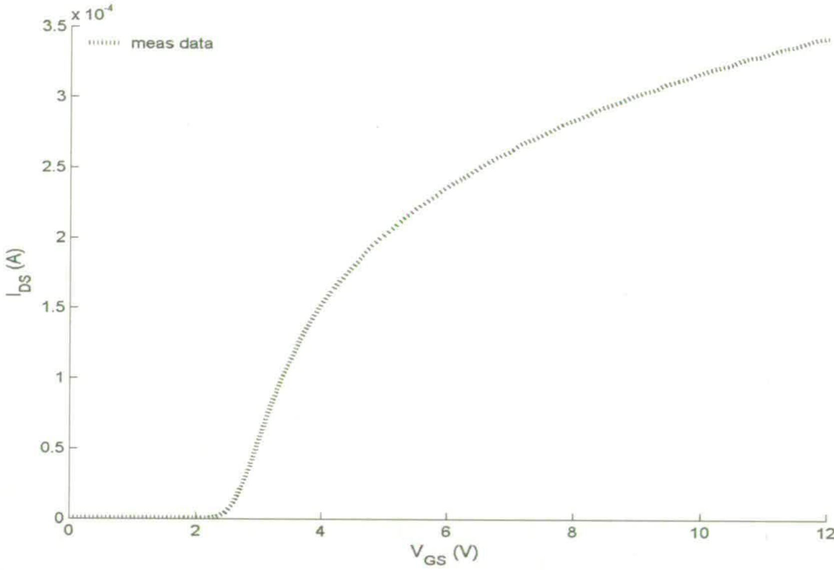
(b)

Figure 6.15 W-array (a) overview of a W-array test-structure containing 17 LDMOS transistor variations. (b) Close-up

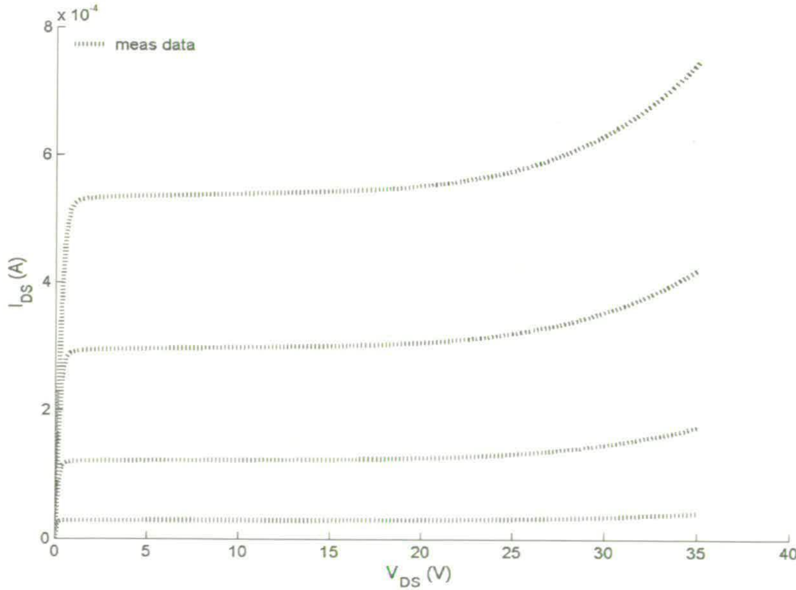
The following measurements are performed on the test-structure:

- I_{DS}-V_{DS} at different V_{GS} at different temperatures (T= -40°C, 25°C, 85°C, 125°C)
- I_{DS}-V_{GS} at different V_{DS} at different temperatures (T= -40°C, 25°C, 85°C, 125°C)

Measurement results for a n-type LDMOS transistor are presented in Figure 6.16

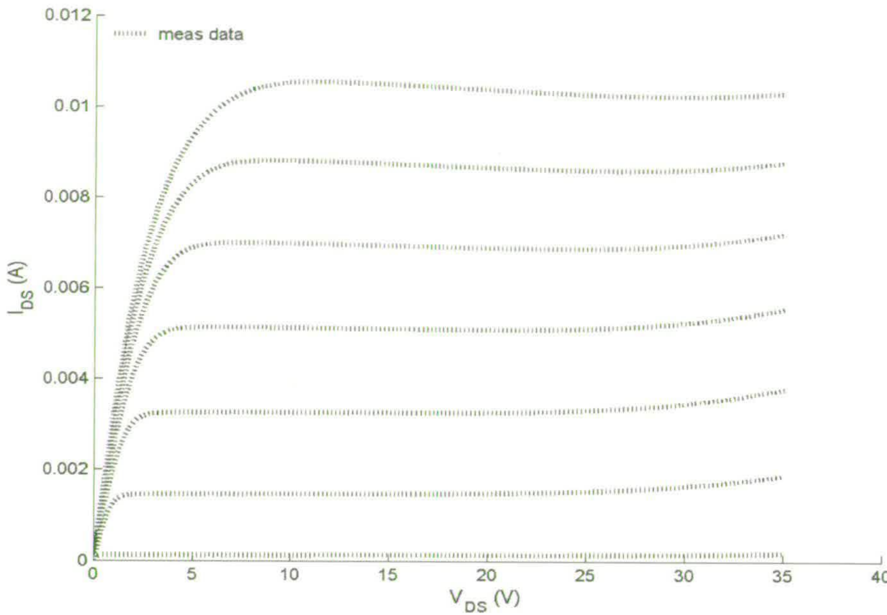


(a) I_{DS}-V_{GS} at V_{DS}=0.1V, Temp = 25°C, Width = 40um



(b) I_{DS} - V_{DS} at V_{GS} = 2.7V; 3.0V; 3.3V; 3.6V, Temp = 25°C, Width = 40um

Figure 6.16 DC LDMOS measurement results of a W-array test-structure



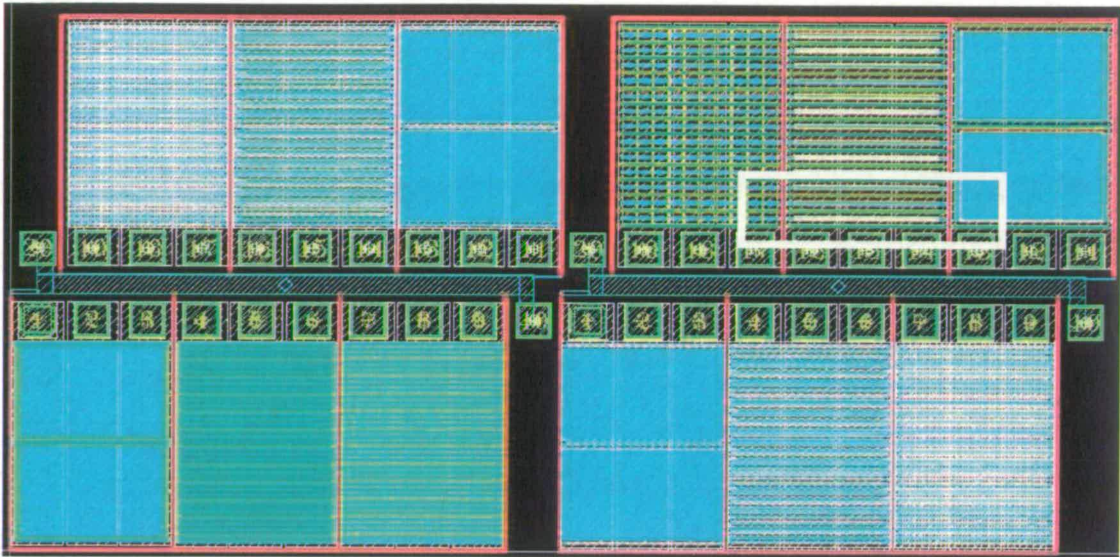
(c) I_{DS} - V_{DS} at V_{GS} = 3.0V; 4.5V; 6.0V; 7.5V; 9.0V; 10.5V; 12V, Temp = 25°C, Width = 40um

Figure 6.16 DC LDMOS measurement results of a W-array test-structure

6.4 Junction diode test-structure

The junction diode test-structure is used to characterise the junctions present in an LDMOS. The test-structure contains 3 different diodes for each type of junction based on combinations of the area and perimeter of the diodes. The purpose of these variations is to make a combination in such a way that only two parameters are changed. Based on this, one can extract the area and perimeter contribution.

An example is given in Figure 6.17

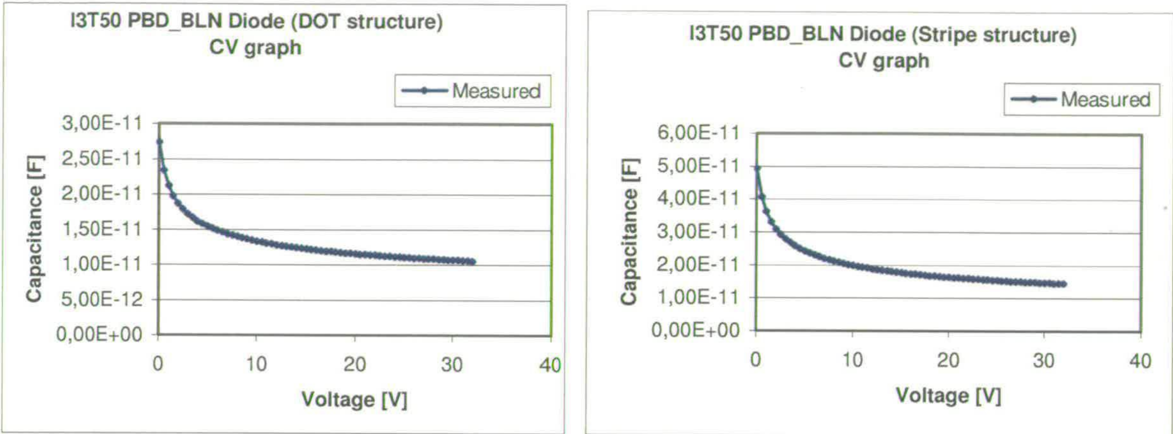


Top view of the junction diode test-structure, the white rectangle is enlarged in the next picture.

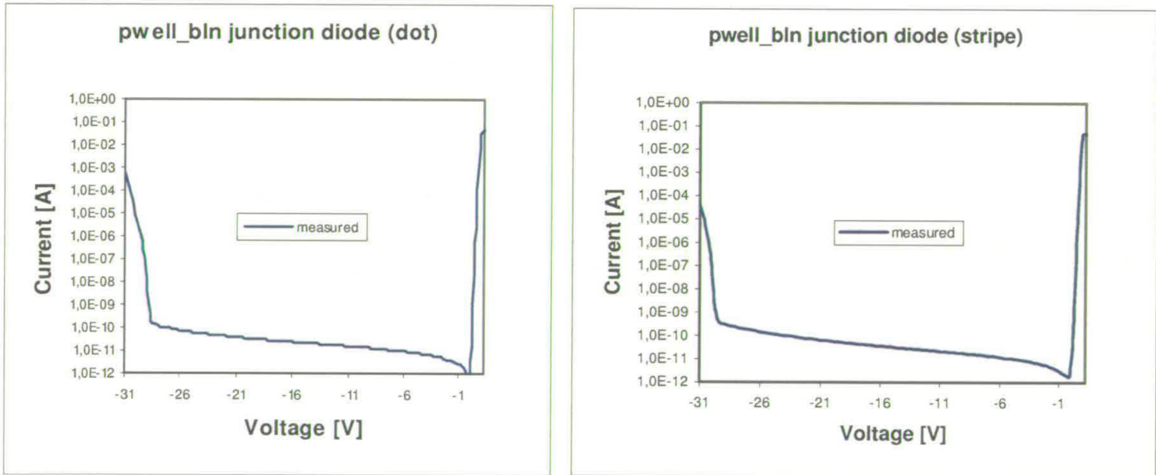
Close-up of the junction diode test-structure, on the left one can see the dotted structures, in the middle the stripe and on the left the planes.

Figure 6.17 junction diode test-structure

Sample results for the pbody – BLN junctions are illustrated in Figure 6.18



(a) capacitance curve for a DOT and a STRIPE structure of the PBODY-BLN diode



(b) current curve for a DOT and a STRIPE structure of the PBODY-BLN diode

Figure 6.18 Measurement results of the junction diode teststructure for the Pbody-BLN diode

6.5 RF-measurement test-structure

The RF measurement test-chip is required for the AC characterisation of the DMOS transistors. The AC-extraction is based on S-parameter extraction.

For each LDMOS transistor, a set of transistors is selected with a combination of width and number of fingers. S-parameters require the pad/interconnect effects to be accounted for and an example of the structures used to perform this is given in Figure 6.19

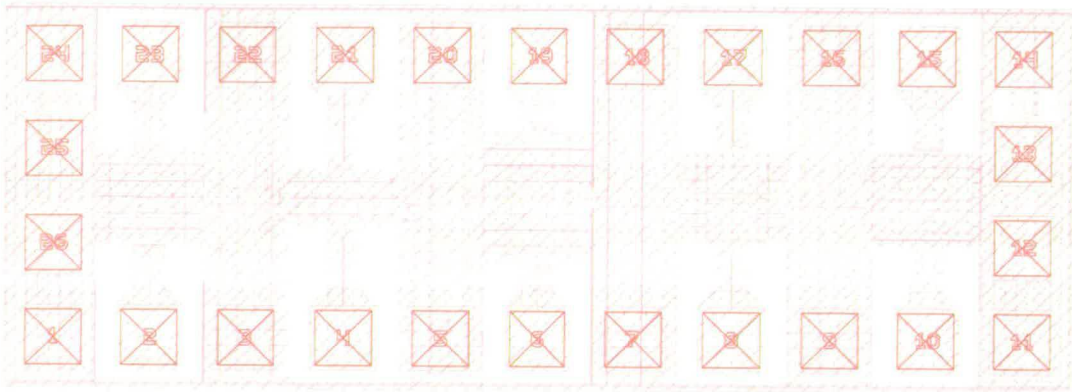


Figure 6.19 RF-test-structure frame

6.6 Introduction to capacitance extraction based on s-parameter measurements

6.6.1 The definition of S-parameters [7]

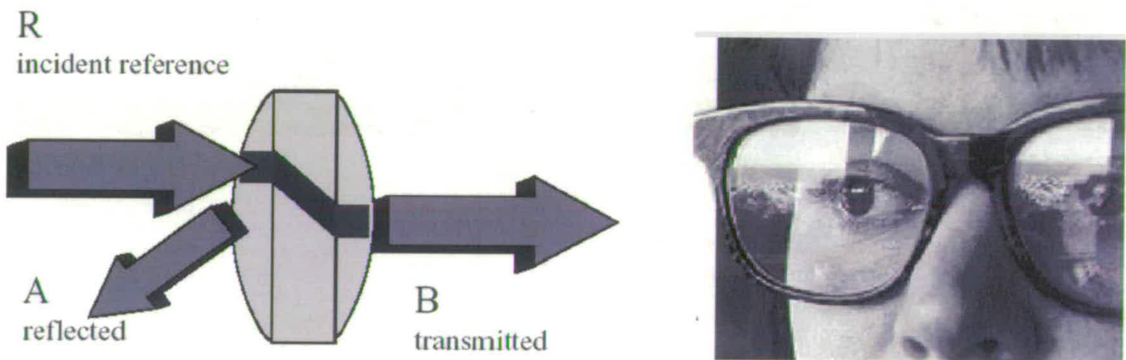


Figure 6.20 S-parameter compared with reflection and transmission through a pair of spectacles

Scattering parameters, also called S-parameters, belong to the group of parameters used in two-port theory. Like the Y or Z parameters, they describe the performance of a two-port completely. Unlike to Y and Z, however, they relate to the travelling waves that are scattered or reflected when a network is inserted into a transmission line of a certain characteristic impedance Z_0. Therefore, S-parameters can be compared to reflection and transmission of light through a lens. (Figure 6.20)

S-parameters are important in design because they are easier to measure and to work with at high frequencies than other kinds of two-port parameters. They are conceptually

simple, analytically convenient and capable of providing detailed insight into a measurement and modelling problem. However, it must be kept in mind that ,like all other two-port parameters, S-parameters are linear by default i.e. they represent the linear behaviour of the two-port.

Staying with the lens example, i.e. power-wise, the S-parameters are defined as:

$$\begin{pmatrix} |\underline{b}_1| \\ |\underline{b}_2| \end{pmatrix} = \begin{pmatrix} |\underline{S}_{11}| & |\underline{S}_{12}| \\ |\underline{S}_{21}| & |\underline{S}_{22}| \end{pmatrix} \times \begin{pmatrix} |\underline{a}_1| \\ |\underline{a}_2| \end{pmatrix} \tag{6.1}$$

with

$|\underline{a}_1|$ power wave travelling towards the two-port gate

$|\underline{b}_1|$ power wave reflected back from the two-port gate

and

$|\underline{S}_{11}|$ power reflected from port1

$|\underline{S}_{12}|$ power transmitted from port2 to port1

$|\underline{S}_{21}|$ power transmitted from port1 to port2

$|\underline{S}_{22}|$ power reflected from port2

Note: a_i, b_i and S_{ij} are effective values and not peak values of the corresponding sine functions.

This means that S-parameters relate travelling waves (power) to a two-port's reflection and transmission behaviour. Since the two-port is embedded in a characteristic impedance of Z_0, these 'waves' can be interpreted in terms of normalised voltage or current amplitudes. This is illustrated in Figure 6.21.

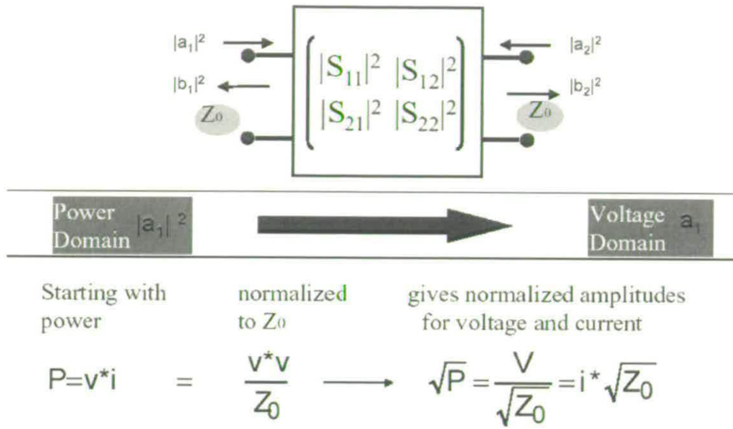


Figure 6.21 S-Parameters and characteristic impedance Z_0

In other words, we can convert the power flowing into the two-port to obtain a normalised voltage amplitude of

$$a_i = \frac{V_{towards_twoport}}{\sqrt{Z_0}} \tag{6.2}$$

and the power out of the two-port can be interpreted in terms of voltages as

$$b_i = \frac{V_{awa_from_twoport}}{\sqrt{Z_0}} \tag{6.3}$$

The following signal flow graph (Figure 6.22) gives the situation for the S-parameter interpretation in voltages:

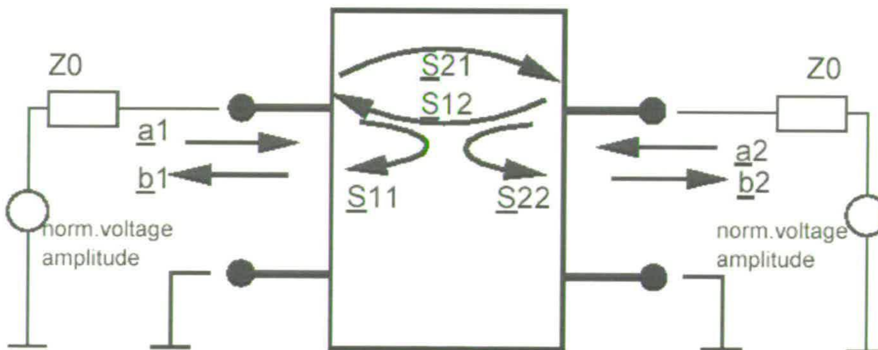


Figure 6.22 signal flow

Looking at the S-parameter coefficients individually, we have:

$$\underline{S}_{11} = \frac{\underline{b}_1}{\underline{a}_1} = \frac{V_{reflected_at_port1}}{V_{towards_port1}}\Bigg/_{\underline{a}_2 = 0} \qquad \underline{S}_{12} = \frac{\underline{b}_1}{\underline{a}_2} = \frac{V_{out_of_port1}}{V_{towards_port2}}\Bigg/_{\underline{a}_1 = 0} \tag{6.4}$$

$$\underline{S}_{21} = \frac{\underline{b}_2}{\underline{a}_1} = \frac{V_{out_of_port2}}{V_{towards_port1}}\Bigg/_{\underline{a}_2 = 0} \qquad \underline{S}_{22} = \frac{\underline{b}_2}{\underline{a}_2} = \frac{V_{reflected_at_port2}}{V_{towards_port2}}\Bigg/_{\underline{a}_1 = 0}$$

S_{11} and S_{21} are determined by measuring the magnitude and phase of the incident, reflected and transmitted signals when the output is terminated in a perfect Z_0 load. This condition guarantees that a_2 is zero. S_{11} is equivalent to the input complex reflection coefficient of the DUT, and S_{21} is the forward complex transmission coefficient.

Likewise, by placing the source at port 2 and terminating port 1 in a perfect load (making a_1 zero), S_{22} and S_{12} measurements can be made. S_{22} is equivalent to the output complex reflection coefficient of the DUT, and S_{12} is the reverse complex transmission coefficient.

The accuracy of S-parameter measurements depends greatly on how good a termination can be applied to the port not being stimulated. Anything other than a perfect load will result in a_1 or a_2 not being zero (which violates the definition for S-parameters). When the DUT is connected to the test ports of a network analyser and no account has been taken of the imperfect test port match, then the measurement will not satisfy the condition of a perfect termination.

For this reason two-port error correction, which corrects for source and load match, is very important for accurate S-parameter measurements.

6.6.2 Characteristic S-parameter values

- S_{11} and S_{22}

value	interpretation
-1	all voltage amplitudes towards the two-port are short circuited (short)
0	impedance matching, no reflections at all (50Ω)
+1	voltage amplitudes are reflected (open)

The magnitude of S_{11} and S_{22} is always less than 1. Otherwise, it would represent a negative ohmic value. On the other hand, the magnitude of S_{21} (transfer characteristics)

can exceed the value of 1 in the case of active amplification while the magnitude of S_{12} (reverse) is usually much smaller than 1. Also, S_{21} and S_{12} can be positive and negative. If they are negative, there is a phase shift.

- S_{21} and S_{12}

Magnitude	interpretation
0	no signal transmission at all
< 1	input signal is damped in the Z_0 environment
+1	unity gain signal transmission in the Z_0 environment
> +1	input signal is amplified in the Z_0 environment

The numbering convention for S-parameters is that the first number following the S is the port at which energy emerges, and the second number is the port at which energy enters. So S_{21} is a measure of power emerging from port 2 as a result of applying an RF stimulus to port 1.

6.6.3 Understanding the Smith chart

What makes S-parameters especially interesting for modelling, is that S_{11} and S_{22} can be interpreted as complex input or output impedances of the two-port (including the termination at the opposite side of the two-port with Z_0).

Hence they are usually plotted in a Smith chart and the following is intended to explain the basics of such Smith charts.

The Smith chart is a transformation of the complex impedance plane Z into the complex reflection coefficient Γ (rho) following:

$$\underline{\Gamma} = \frac{\underline{Z} - Z_0}{\underline{Z} + Z_0} \tag{6.5}$$

with the system's reference impedance $Z_0 = 50\Omega$

As a result the right half of the complex impedance plane Z is transformed into a circle in the Γ -domain. The circle radius is '1' (see Figure 6.23).

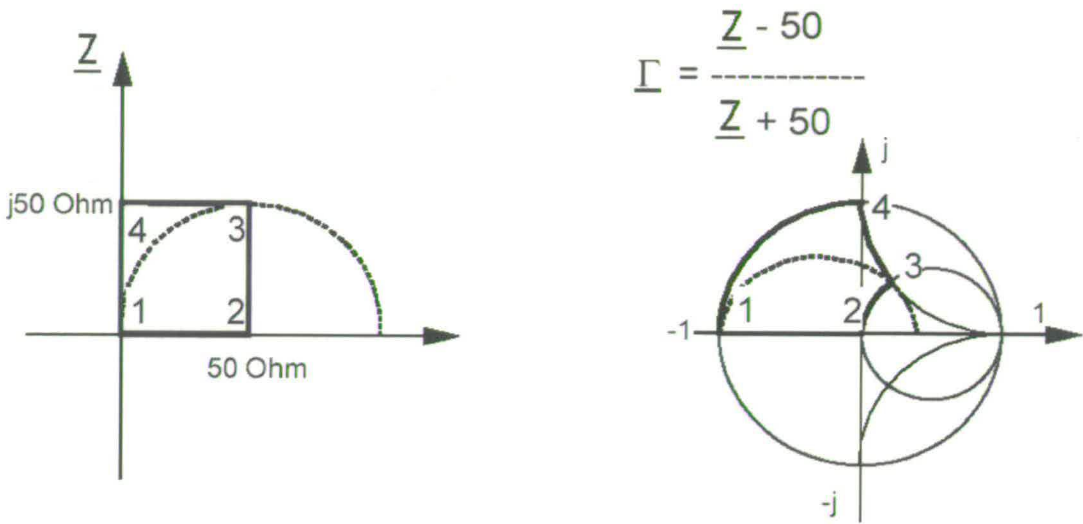


Figure 6.23: the relationship between Sxx and the complex impedance of a twoport.

On the other hand, using a network analyzer with a system impedance of Z_0, the parameter S_{11} is equal to

$$S_{11} = 2 \times \frac{v_1}{v_{01}} - 1 \qquad (6.6)$$

where v_1 is the complex voltage at port 1 and v_{01} the stimulating AC source voltage (typically normalized to '1') as shown in Figure 6.24.

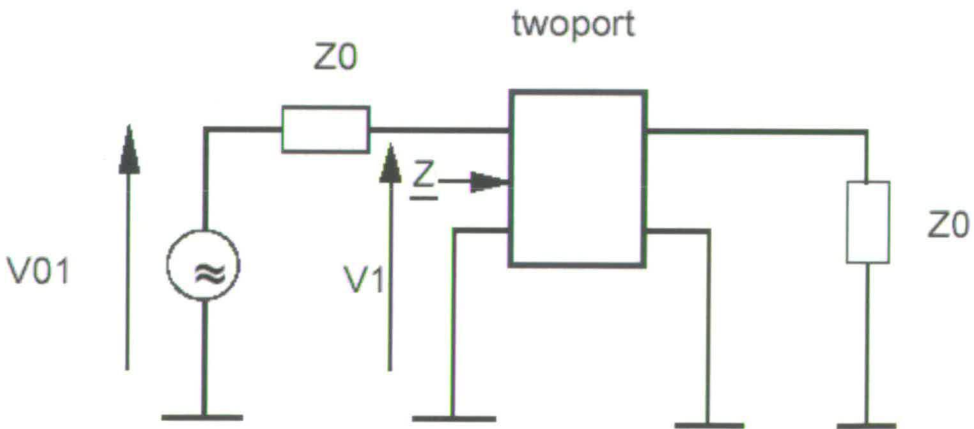


Figure 6.24: about the definition of S_{11} (S_{22} is just analogous).

Under the assumption that Z is the complex input impedance at port 1 and Z_0 is the system impedance, then by using equation 6.6 and the resistive divider formula we obtain:

$$\underline{S_{11}} = 2\times\frac{\underline{R}}{\underline{R}+Z_0} - 1 = \frac{\underline{R}-Z_0}{\underline{R}+Z_0} \tag{6.7}$$

This is the reflection coefficient Γ from port 1. So, if the reflection coefficient Γ (resp. S_{11} or S_{22}) is known, we get for the complex resistor Z:

$$\underline{Z} = Z_0 \times \frac{1+\underline{\Gamma}}{1-\underline{\Gamma}} = Z_0 \times \frac{1+\underline{S_{11}}}{1-\underline{S_{11}}} \text{, with usually } Z_0 - 50\Omega \tag{6.8}$$

This explains how to obtain the complex input/output impedance of a two-port directly from S_{11} or S_{22}, when plotting these S-parameters on a Smith chart.

Figure 6.23 shows a square with the corners (0/0), (50/0), (50/j50) and (0/j50), ιn the complex impedance plane and its equivalent in the Smith chart with Z_0=50Ω. The angle preserving property of this transform can be observed (rectangles stay rectangles close to their origins). It can also be seen how the positive and negative imaginary axis of the R plane is transformed into the Smith chart domain (Γ), and where (50/j50) is located on the Smith chart. Also it can be verified that the centre of the Smith chart represents Z_0, i.e. for Z_0=50Ω, the centre of the Smith chart is (50/j0).

Figure 6.25 shows once again the transformation of the complex ohmic plane to the Smith chart.

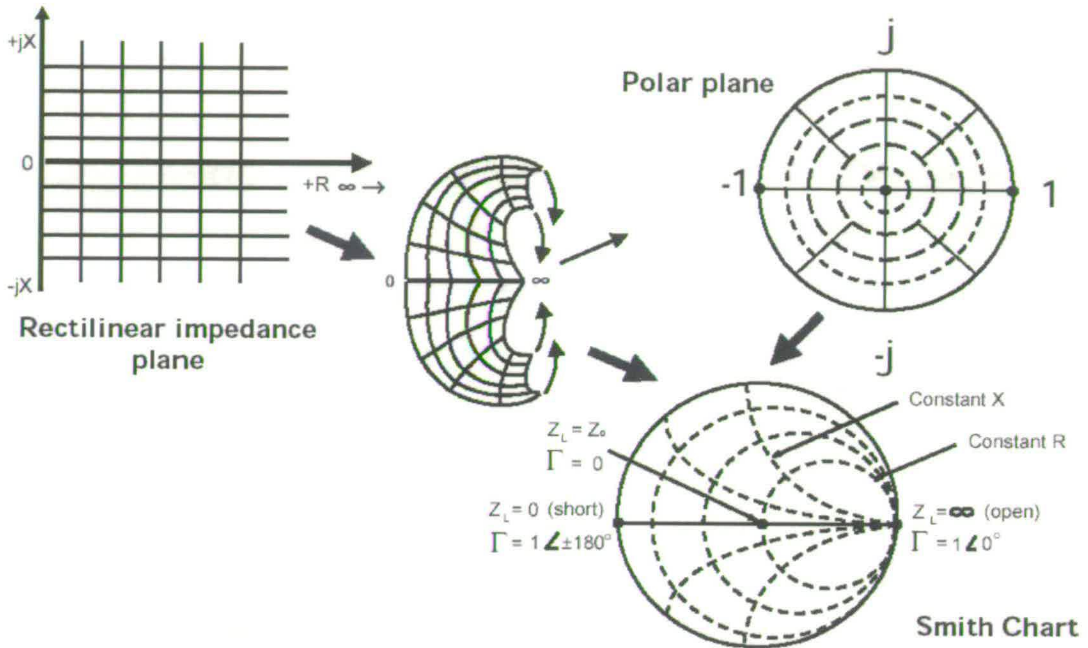


Figure 6.25: How the complex resistance plane is transformed into the Smith chart: Smith Chart rectilinear impedance plane onto a polar plane.

This allows us to make the following statements: (Figure 6.26)

- Values plotted on the Smith chart on the real axis represent ohmic resistors
- Values plotted on the Smith chart above the real axis represent inductors
- Values plotted on the Smith chart below the real axis represent capacitors

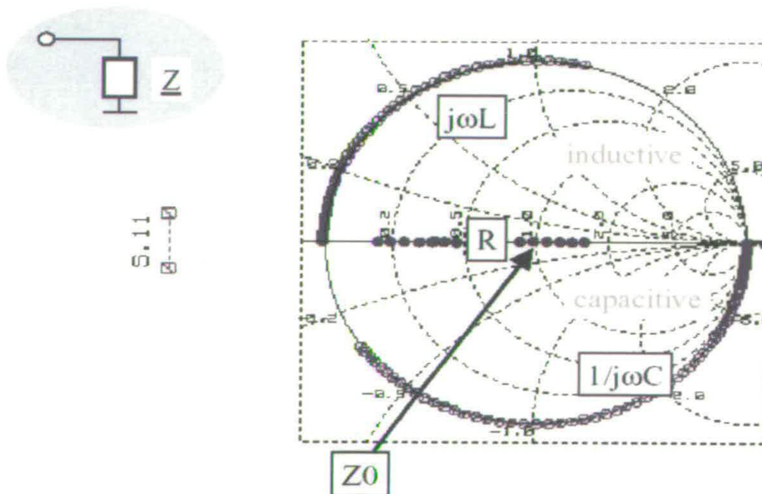


Figure 6.26 Smith chart overview

6.7 Capacitance calculation for a LDMOS transistor from measured s-parameters.

6.7.1 Measurement set-up

A schematic of the test system used in this work is shown in Figure 6.27:

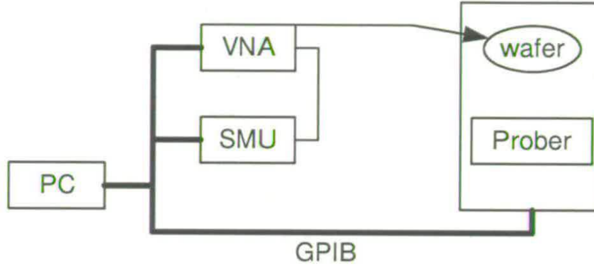


Figure 6.27 Schematic overview of the measurement setup

The main components of the test system are a Vector Network Analyser (VNA), a prober, an analyser linked to a PC through a GPIB (General Purpose Interface Bus) connection. A program was developed in Labview [8] to control the measurements.

6.7.2 Conversion from Y-parameters to C_{gs}, C_{gd} and C_{gb} capacitances.

The values for S_{11}, S_{12}, S_{21} and S_{22} are obtained from the measurements and to transform these to capacitance values, an intermediate transform to Y-parameters is used:

$$Y_{11} = \frac{\frac{1}{50.0}\times((1+S_{22})\times(1-S_{11})+S_{12}\times S_{21})}{1+S_{22}+S_{11}+S_{11}\times S_{22}-S_{12}\times S_{21}} \tag{6.9}$$

$$Y_{12} = \frac{\frac{-1}{50.0}\times((1+S_{22})\times S_{12}-S_{12}\times(1-S_{22}))}{1+S_{22}+S_{11}+S_{11}\times S_{22}-S_{12}\times S_{21}} \tag{6.10}$$

$$Y_{21} = \frac{\frac{-1}{50.0}\times((1-S_{11})\times S_{21}-S_{21}\times(1+S_{11}))}{1+S_{22}+S_{11}+S_{11}\times S_{22}-S_{12}\times S_{21}} \tag{6.11}$$

$$Y_{22} = \frac{\frac{1}{50.0}\times((1-S_{22})\times(1+S_{11})+S_{12}\times S_{21})}{1+S_{22}+S_{11}+S_{11}\times S_{22}-S_{12}\times S_{21}} \tag{6.12}$$

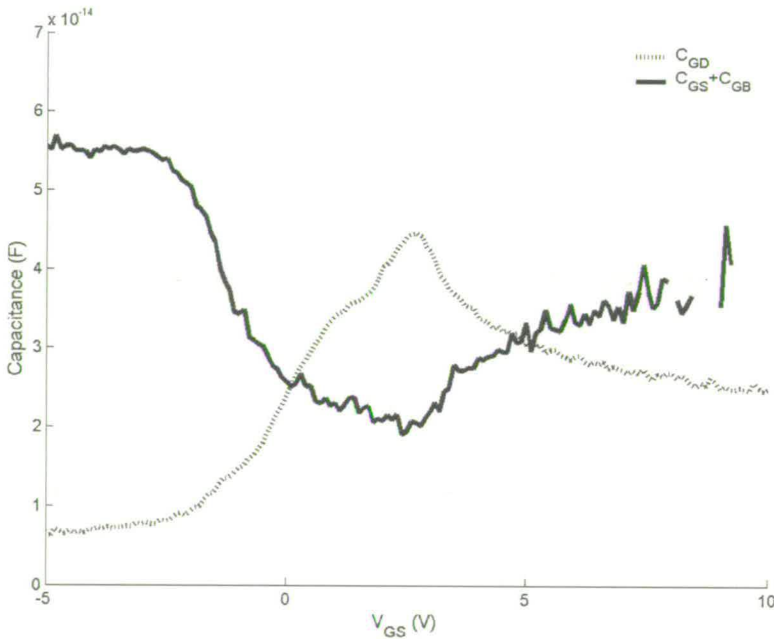
From these Y-parameters we can calculate the C_{gs}+C_{gb} and C_{gd} capacitances:

$$C_{gs} + C_{gb} = \frac{-1}{imag\left(\frac{1}{Y_{11} + Y_{12}}\right) \times freq \times 2\pi} \tag{6.13}$$

$$C_{gd} = \frac{-1}{imag\left(\frac{1}{-Y_{12}}\right) \times freq \times 2\pi} \tag{6.14}$$

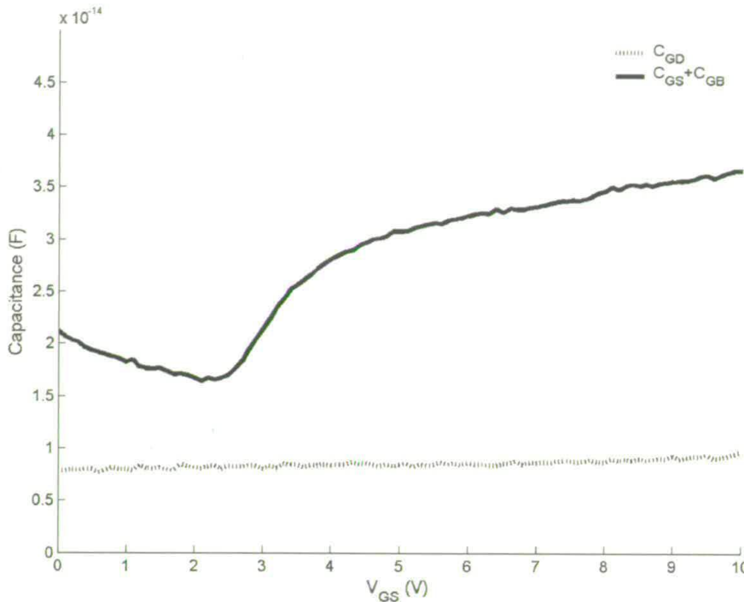
The frequency at which the capacitances are extracted is set to around 500 Mhz, based on the analyses of the measurement data.

These S-parameter measurements and conversions result in C_{gs}, C_{gd} and C_{gb} curves as shown in Figure 6.28



(a) C_{GS}+C_{GB} and C_{GD} extraction results for V_{DS} = 0V

Figure 6.28 Extraction results of the RF measurement test-structure



(b) C_{GS}+C_{GB} and C_{GD} extraction results for a V_{DS} = 20V

Figure 6.28 Extraction results of the RF measurement test-structure

6.8 Conclusion

A complete set of test-structures have been designed and measured to analyse DMOS transistors and extract their model-parameters. A novel MESDRIFT test-structure has been developed and was found useful on various domains of the DMOS characterisation (V_K behaviour, self-heating, hot-carrier)

References

[1] EPFL institute, www.epfl.ch

[2] "Performance modeling of RF power MOSFETs", M. Trivedi, P. Khandelwal, K. Shenai, IEEE Transactions on Electron. Dev., vol. 46, 1999, pp. 1794 – 1802.

[3] Circuit model for power LDMOS including quasi-saturation J. Jaejune, T. Amborg, Y. Zhiping; R.W. Dutton., SISPAD '99, 1999, pp. 15 – 18.

[4] Physically based description of quasi-saturation region of vertical DMOS power transistors C.H. Kreuzer, N. Krischke, P. Nance, IEDM Techn. Digest, 1996, pp. 489 – 492.

[5] Bias-dependent drift resistance modeling for accurate DC and AC simulation of asymmetric HV-MOSFETN. Hefyene, E. Vestiel, S. Frere, C. Anghel, A.M. Ionescu, R. Gillon, SISPAD 2002. 4-6 Sep 2002, pp. 203 - 206

[6] A novel hot-hole injection degradation model for lateral nDMOS transistors P. Moens, M. Tack, R. Degraeve, G. Groeseneken, IEDM Techn. Digest 2001, pp. 39.6.1 -39.6.4

[7] Agilent tutorial on S-parameters. www.agilent.com

[8] Labview website: www.labview.com

LDMOS macro-model: definition / extraction procedure / worst-case corner generation

LDMOS macro-model: definition / extraction procedure / worst-case corner generation 91
7.1 Introduction **91**
7.2 Macro-model topology **91**
7.2.1 MOS transistor M1 (channel) 92
7.2.2 JFET J1 (drift region) 93
7.2.3 Shorted p-type MOS transistor M2 & M3 93
7.2.4 Diodes D1 & D2 93
7.2.5 Diode D3 93
7.2.6 Resistor R1 94
7.3 Detailed description of the macro-model components **94**
7.3.1 Standard available components 94
7.3.2 Adaptation of Schichman & Hodges JFET model for modelling of DMOS drift region 95
7.3.3 Shorted MOS devices for AC modelling 97
7.3.4 Adapted capacitance Verilog-A model, replacing shorted MOST 98
7.4 Model parameter extraction procedure **102**
7.4.1 Geometry parameters 102
7.4.2 Extraction of subthreshold parameters 102
7.4.3 Triode parameters 103
7.4.4 Extraction of saturation region parameters 104
7.4.5 Extraction of temperature parameters 107
7.4.6 AC-parameter extraction 108
7.4.7 Diode DC-parameters 109
7.5 Worst-case corner extraction **109**
7.5.1 Introduction 109
7.5.2 Device and technology description 110
7.5.3 Mapping of electrical parameter space onto model parameter space 111
7.5.4 Generation of worst-case models based on a multivariate analysis 113
7.5.5 Monte-Carlo models 116
7.6 Conclusion **117**
References **117**

LDMOS macro-model: definition / extraction procedure / worst-case corner generation

7.1 Introduction

Based on the findings of chapter 5 and chapter 6, a macro-model has been developed. As a first step, a topology is proposed and then the functionality of the topology is confirmed and an extraction procedure developed. As a model should be able to accurately predict process variation on the device, worst case models and a procedure to extract these models must be available and this thesis proposes a novel methodfor this task, based on neural networks. A key element of establishing the model is to verify its performance against the targets set in chapter 4.

7.2 Macro-model topology

The non-standard behaviour of the LDMOS device, as described in chapter 4 and 5, cannot be rendered with the standard BSIM3v3.2 MOS-model. The proposed topology of a macro-model is shown in Figure 7.1. This topology will be called FRERE_V1.

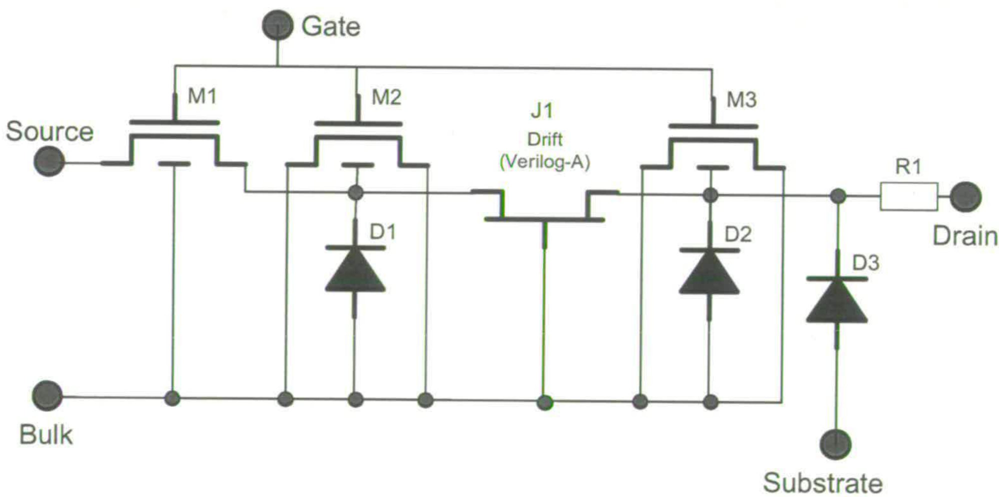


Figure 7.1 Sub-circuit model of LDMOS device (FRERE_V1)

Key features of this macro-model are: (1) the adapted JFET (J1), modelling the drift region and (2) the shorted PMOS transistors (M2 and M3), which model the drift region under the gate oxide. Special attention has been given to the modelling of the K-point behaviour.

In the second stage the topology was improved to that shown in Figure 7.2 which will be referred to as FRERE_V2:

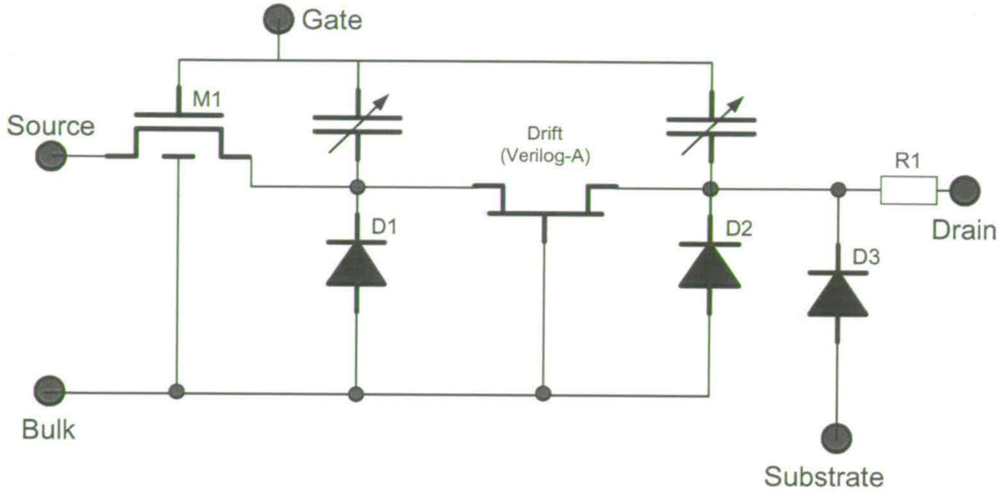


Figure 7.2 Sub-circuit model of LDMOS device (FRERE_V2)

This was introduced to further improve of the robustness of the model as will be explained later.

7.2.1 MOS transistor M1 (channel)

The channel region of the DMOS transistor is modelled, based on the standard low-voltage MOS model, BSIM3.3V2 [1]. The BSIM3.3V2 model requires a large set of parameters, which are dedicated to modelling low-voltage MOSFETs. However due to the topology of the model only a small set of them need to be extracted. This low-voltage model is well known for standard MOS devices. The BSIM3.3V2 model is implemented in almost all SPICE circuit simulators, and is thus generally available. It has also been optimised in these simulators to minimise the time needed to simulate, and converges in all operating regions. However, this model presents some limitations when modelling the channel of an LDMOS. BSIM3V3.2 has some limited non-uniform doping effects such as reverse short channel effect and vertival doping effects for V_{BS} influence on V_{TH}. Unfortunately it is not able to model non-uniformly doped regions present in an LDMOS. This poses no real problem for the DC behaviour of the LDMOS model. However, for the AC behaviour, this introduces some limitations, which will be described later.

7.2.2 JFET J1 (drift region)

The drift region is modelled using an adapted JFET model and the equations are based on the Schichman & Hodges model [2]. The behaviour of the LDMOS drift region, as described in chapter 5, requires the JFET model to be adapted. To implement this, a Verilog-A module has been used. This contains standard JFET equations with the addition an LDMOS gate-voltage dependent V_T. This component has proven to be key to the overall model behaviour, as it models the V_K behaviour. A more detailed description is given in section 7.3.2. This Verilog-A module introduces a significant increase in the time needed to simulate. Fortunately, once the model has been fully verified, this component can be compiled in native simulator code, which will drastically improve the simulation speed.

7.2.3 Shorted p-type MOS transistor M2 & M3

Two shorted p-MOS transistors (for an n-type DMOS model) were inserted, to model the region where the n-tub is overlapped by the gate and field oxide. This region changes from inversion to depletion to accumulation with increasing V_{GS} as detailed in chapter 5. The transistors are connected so that there is no contribution to the DC-behaviour of the model. These two components model the bias dependent AC behaviour as previously described in chapter 5. In a second stage these shorted p-type MOS transistors were replaced by a Verilog-A module, with the same basic functionality. However, this introduced more flexibility in modelling the AC behaviour of the LDMOS device, which led to a significant improvement of the model accuracy.

7.2.4 Diodes D1 & D2

The separation of the body-drain diode into two elements located on each side of the drift-region JFET (J1) is important in order to correctly simulate the several pronounced peaks visible in the capacitance characteristics.

7.2.5 Diode D3

This diode is inserted to model the junctions present between the different layers from drain to substrate. The exact topology of the diodes varies from device to device, depending on the technology in which the device is implemented.

7.2.6 Resistor R1

This resistor is required to model the Ron behaviour of the LDMOS transistor. This resistor models the resistance allocated under the field-oxide that is gate independent.

7.3 Detailed description of the macro-model components

7.3.1 Standard available components

In SPICE simulators a set of components represented by different models are built into the simulator code. For example, to simulate a MOS transistor one can choose between level 1, level 2, level 3, BSIM3v3.2, etc. Each of these models have their equations hard-coded inside the simulator, which increases simulation speed and enhances robustness.

The proposed macro-model has been built in such a way that a maximum number of standard devices are available in the SPICE simulator. If a component is needed with characteristics that are not implemented by the circuit simulator, a general available and accepted programming language Verilog-A [2] is available. The Verilog-HDL standard originates from the high level circuit description language which has been adapted to Verilog-A enabling the user to describe component-behaviour. As mentioned before, it is possible at a later stage, to compile these verilog-A modules into standard components available in the circuit simulator.

MOS model BSIM3V3.2

The BSIM3V3.2 model is used to model the channel region of the DMOS transistor and to model the AC-behaviour by means of two shorted MOS transistors. BSIM3V3.2 was chosen because it is a widely accepted and supported model, which has a high level of accuracy in DC as well as in AC operation. In a second stage the shorted MOS components are replaced by Verilog-A modules, to further improve the accuracy.

Junction Diode level 1 model

The following effects are included in the junction diode model: forward characteristics, reverse leakage current, breakdown, parasitic resistance, diffusion capacitance and depletion capacitance.

Standard Resistor model

A standard resistor is introduced to model accurately the R_{on} behaviour of an LDMOS.

7.3.2 Adaptation of Schichman & Hodges JFET model for modelling of DMOS drift region

When evaluating the standard available JFET component, it is observed that, depending on the JFET parameter values, one can model some regions of the LDMOS accurately for certain values of Vgs but unfortunately not all regions.

Thus, a custom made component is necessary. The Verilog-A module (available from the SPECTRE standard library), which describes the Schichman & Hodges JFET model, was used as a starting point.

The operation of the JFET is such that, when a more negative voltage is applied to the gate of the JFET, the device becomes more resistive as the depletion regions expand, thus narrowing the channel of the JFET. The gate voltage of the JFET is in fact the voltage between the bulk and the V_K point of the macro-model. Thus, an increase in V_K, making the gate voltage of the JFET more negative, will result in a higher JFET resistance, which corresponds to the behaviour detailed previously in chapter 5. The adaptation of the JFET model provides the capability for the threshold voltage of the JFET to be dependent on the gate voltage of the LDMOS (Figure 7.3), which is essential for the model to achieve a good overall accuracy. When the threshold voltage of the JFET is fixed, a large increase in V_K would pinch off the JFET channel completely, resulting in the drift region resistance being too high. By making the threshold voltage of the JFET increase with V_{GS}, the use of a wider voltage range is possible, as the JFET will never pinch off completely. Figure 7.4 shows the SPICE simulation result of V_K. The high V_K value when V_{GS} is below V_T is due to the fact that there is no current flowing. When V_{GS} is higher than V_T, the behaviour is similar to that shown in Figure 7.5 although it should be noted that the voltage level is higher. This can be explained by the fact that the voltages obtained by TCAD simulations are highly dependent on the location of the probing point.

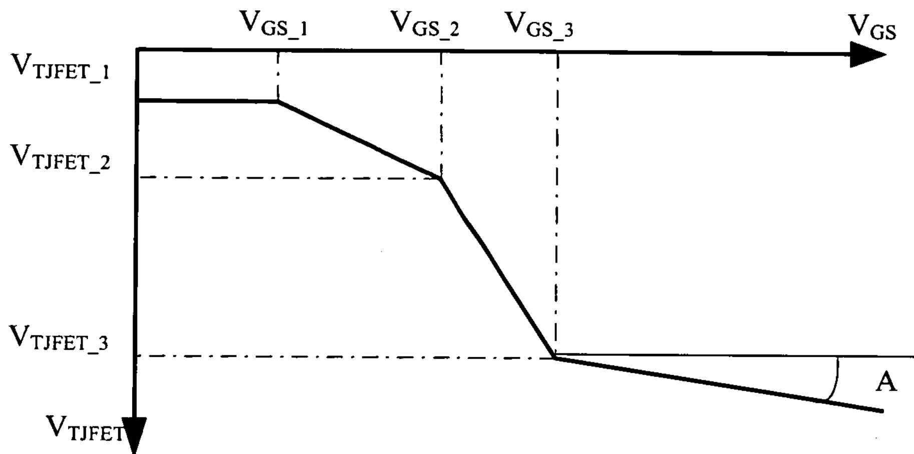


Figure 7.3. JFET V_T dependence as a function of V_{GS}.

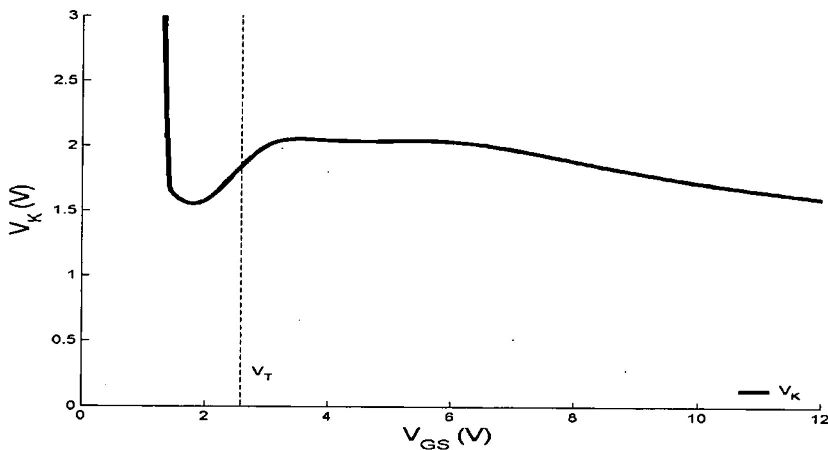


Figure 7.4. V_K as modelled by a JFET as a function of V_{GS} at V_{DS}=10V.

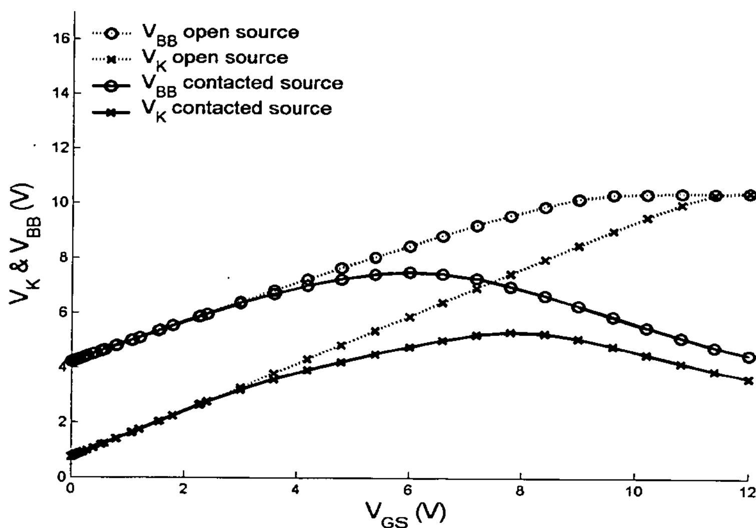
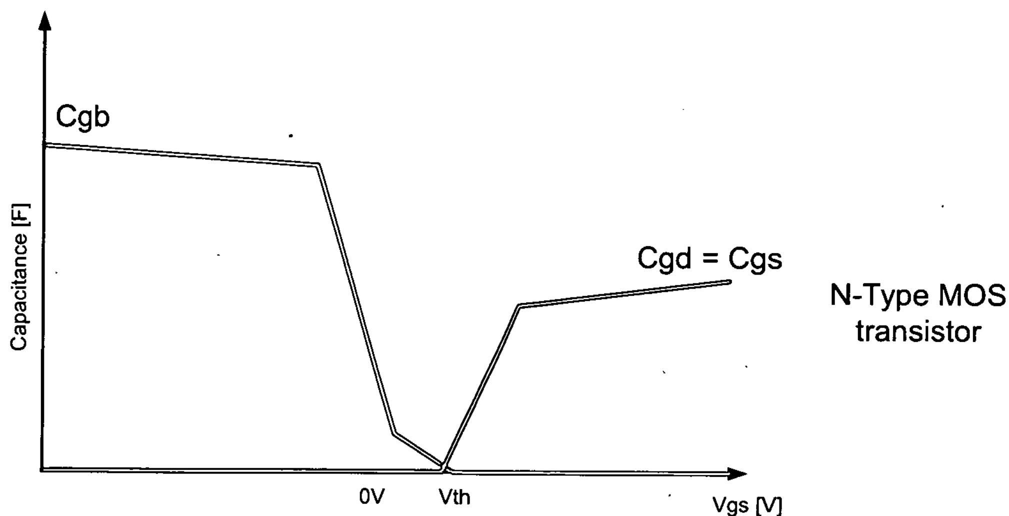


Figure 7.5. V_K and V_{BB} as a function of V_{GS} with source closed and open at V_{DS} = 10V.

To improve the robustness of the Verilog-A module, the "IF-THEN-ELSE" statements were replaced by infinitively differentiable functions. This ensures that when the function is differentiated, no discontinuities appear.
The Verilog-A code is detailed in Appendix A

7.3.3 Shorted MOS devices for AC modelling

From Figure 7.1 one can observe that the source and drain terminals of transistors M2 and M3 are connected together to guarantee that they will not influence the DC-model. The bulk terminals of the transistors are connected to the source / drain node of the JFET. This means that the Cgb capacitance of the shorted MOS transistor is used to model the Cgs and Cgd capacitance of the LDMOS.
The type of shorted MOS (n-type or p-type) depends on the type of DMOS being modelled. For an n-type DMOS, p-type shorted MOS transistors are used. (Figure 7.6(A)).
A graphical representation of the required capacitance behaviour is given in Figure 7.6(C).

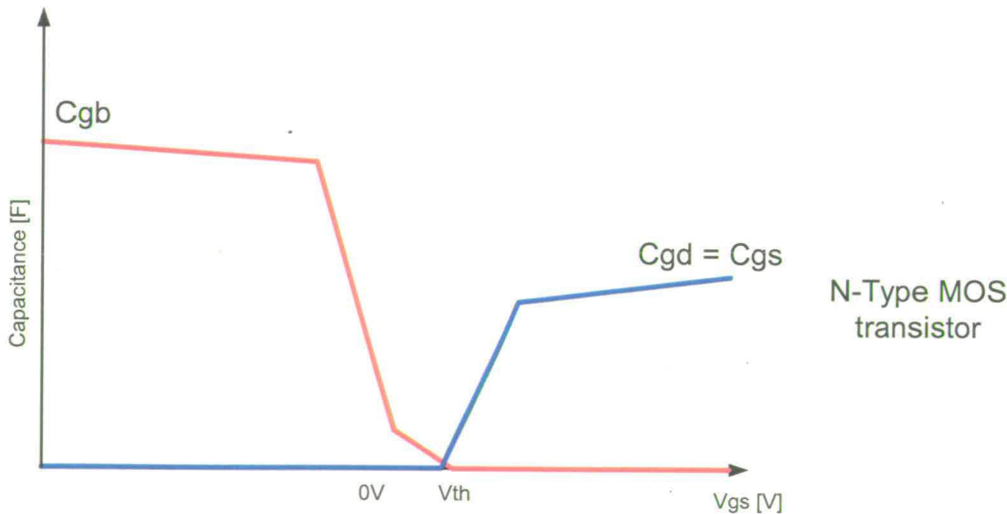


(A) Capacitance behaviour for an n-type of MOS transistor
Figure 7.6 Capacitance behaviour for different types of MOS / DMOS transistors

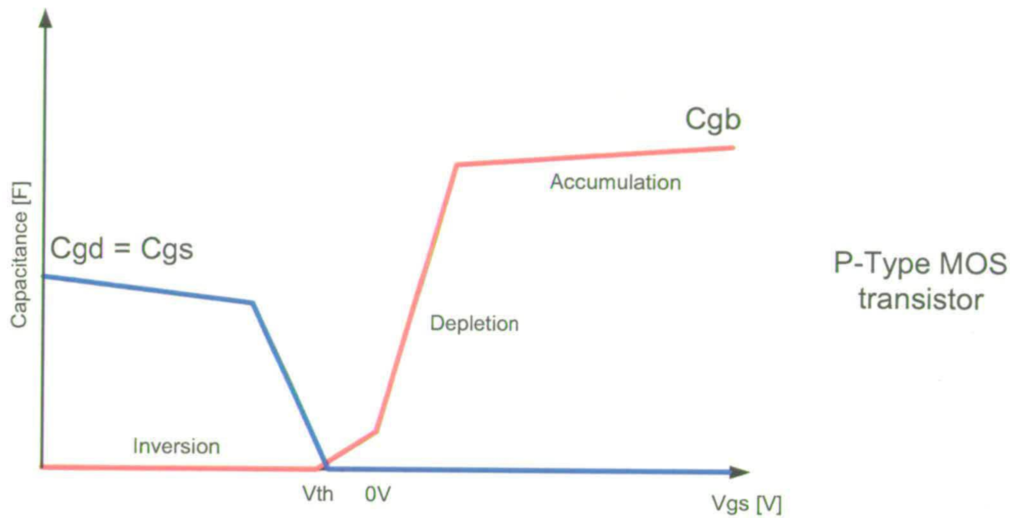
To improve the robustness of the Verilog-A module, the "IF-THEN-ELSE" statements were replaced by infinitively differentiable functions. This ensures that when the function is differentiated, no discontinuities appear.
The Verilog-A code is detailed in Appendix A

7.3.3 Shorted MOS devices for AC modelling

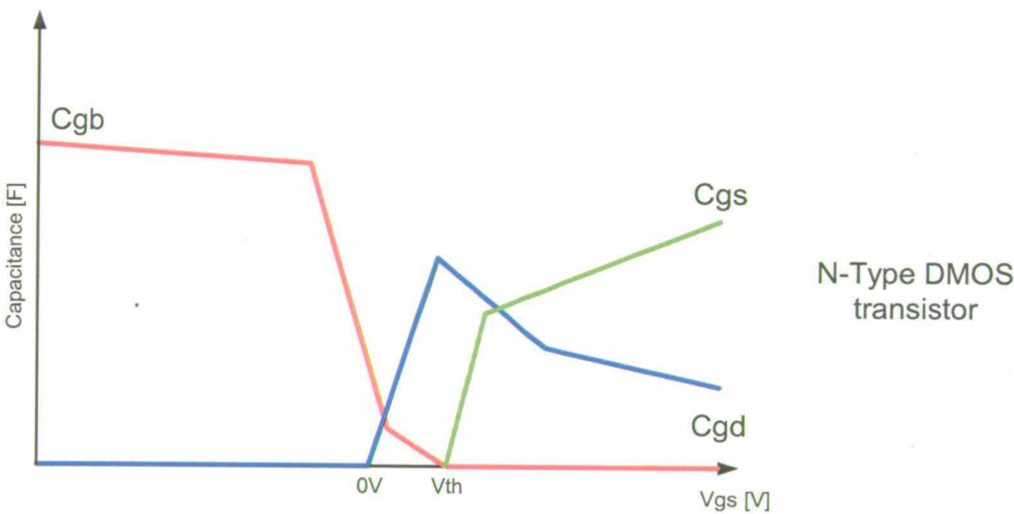
From Figure 7.1 one can observe that the source and drain terminals of transistors M2 and M3 are connected together to guarantee that they will not influence the DC-model. The bulk terminals of the transistors are connected to the source / drain node of the JFET. This means that the Cgb capacitance of the shorted MOS transistor is used to model the Cgs and Cgd capacitance of the LDMOS.
The type of shorted MOS (n-type or p-type) depends on the type of DMOS being modelled. For an n-type DMOS, p-type shorted MOS transistors are used. (Figure 7.6(A)).
A graphical representation of the required capacitance behaviour is given in Figure 7.6(C).



(A) Capacitance behaviour for an n-type of MOS transistor
Figure 7.6 Capacitance behaviour for different types of MOS / DMOS transistors



(B) Capacitance behaviour for a p-type of MOS transistor



(C) Capacitance behaviour for an n-type DMOS transistor

Figure 7.6 Capacitance behaviour for different types of MOS / DMOS transistors

As discussed in chapter 5, the area under the gate and field oxides in the drift region, changes from inversion to accumulation as a function of Vgs. When one compares this to the behaviour of a p-type MOS transistor as shown in Figure 7.6 (B), one can see this similarity as the Cgb of the device changes from inversion to depletion to accumulation.

7.3.4 Adapted capacitance Verilog-A model, replacing shorted MOST

It was confirmed that the shorted MOS transistors explained in section 7.3.3, are able to model the AC behaviour of an LDMOS to an acceptable level. However, these models

introduce a large overhead (complete BSIM3v3.2 model), slowing down the simulator. In addition to the slow-down of the simulator there is only a limited flexibility to tune the capacitance curves to the measured data. This is due to the fact that BSIM3V3.2 is developed to model low-voltage MOS devices.

In summary the LDMOS capacitance curve is the sum of the capacitance behaviour of all the different components present. These components are the BSIM3.3V2 model used for modelling the channel, the resistor R1 representing the fixed resistance contribution of the drift region and the Verilog-A capacitance module. The following sections present the contributions of the different topologies based on the set of components.

7.3.4.1 Model topology based on BSIM3V3.2 and resistor to model LDMOS capacitances

The BSIM3V3.2 model (M1) and standard resistor R1 modelling the channel and RON introduce the capacitances as illustrated in Figure 7.7.

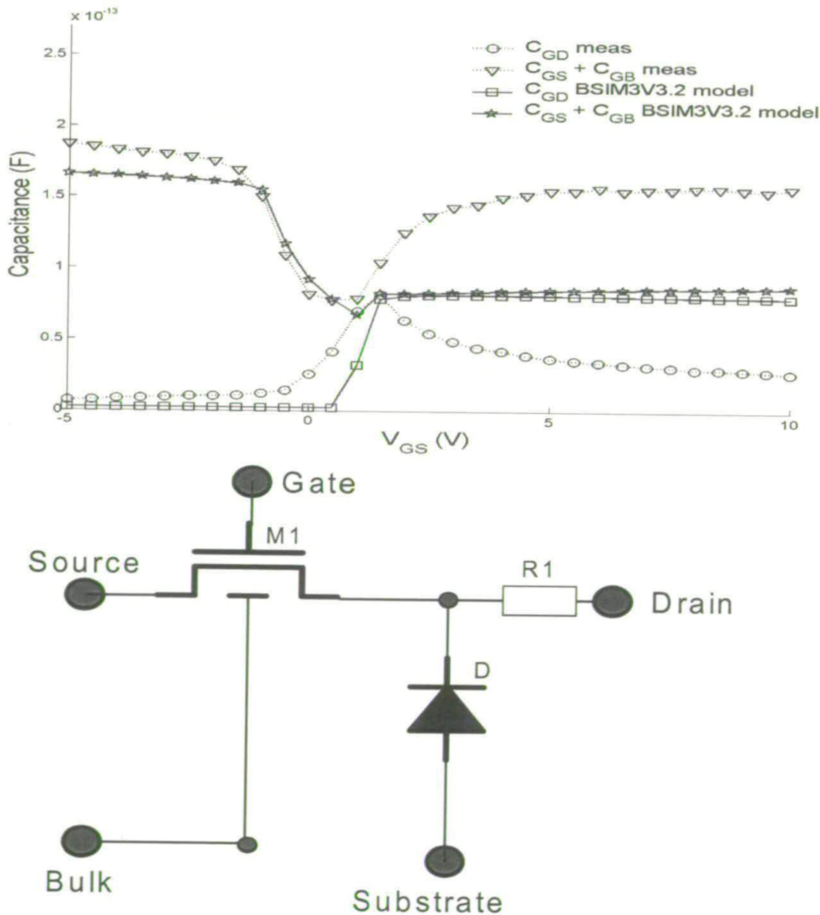


Figure 7.7 LDMOS capacitances modelled by BSIM3V3.2 and Resistor

It is the resistor R1 that introduces the difference in Cgs and Cgd for Vgs > V_T. The resistivity towards the drain is higher than the resistivity to the source, causing more charge to flow to the source than to the drain, introducing a slightly higher Cgs. However, the rise of the Cgd before the transistor's V_T is not captured in this approach as can be seen on Figure 7.7.

7.3.4.2 Model topology based on BSIM3V3.2, Shorted MOS, Verilog-A rdrift module and a resistor to model LDMOS capacitances (FRERE_V1)

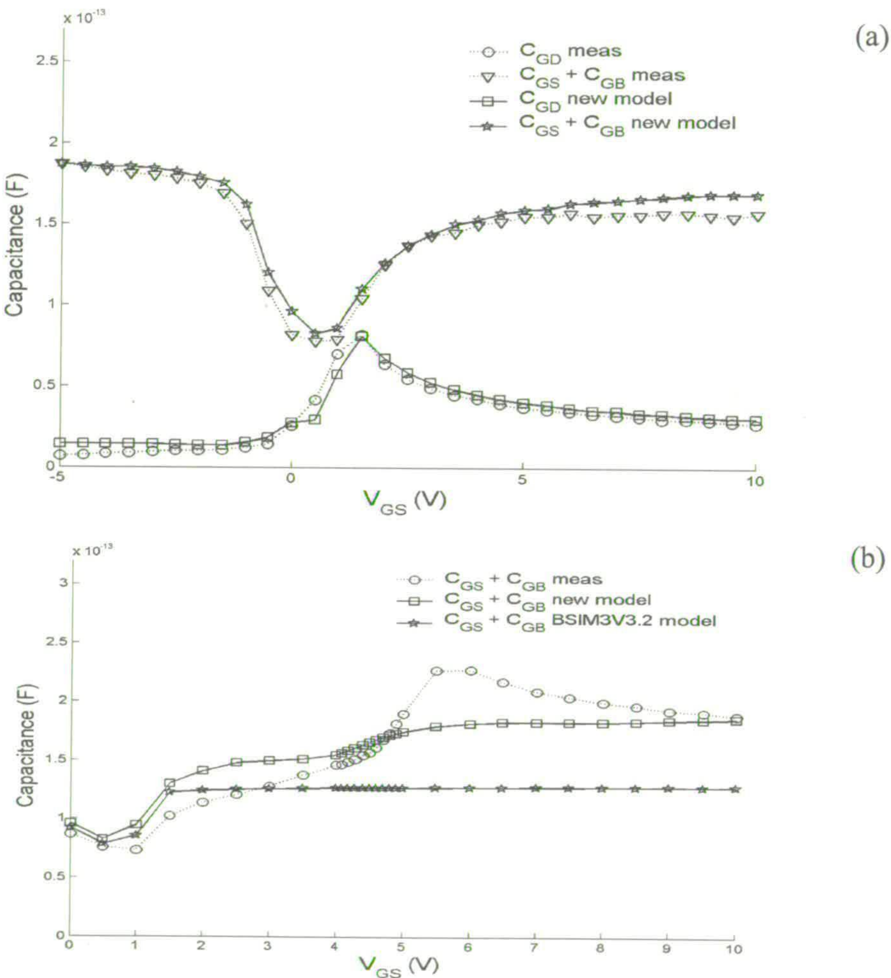


Figure 7.8 Simulated and measured C_{GD} and C_{GS} curves as a function of V_{GS} and V_{DS}

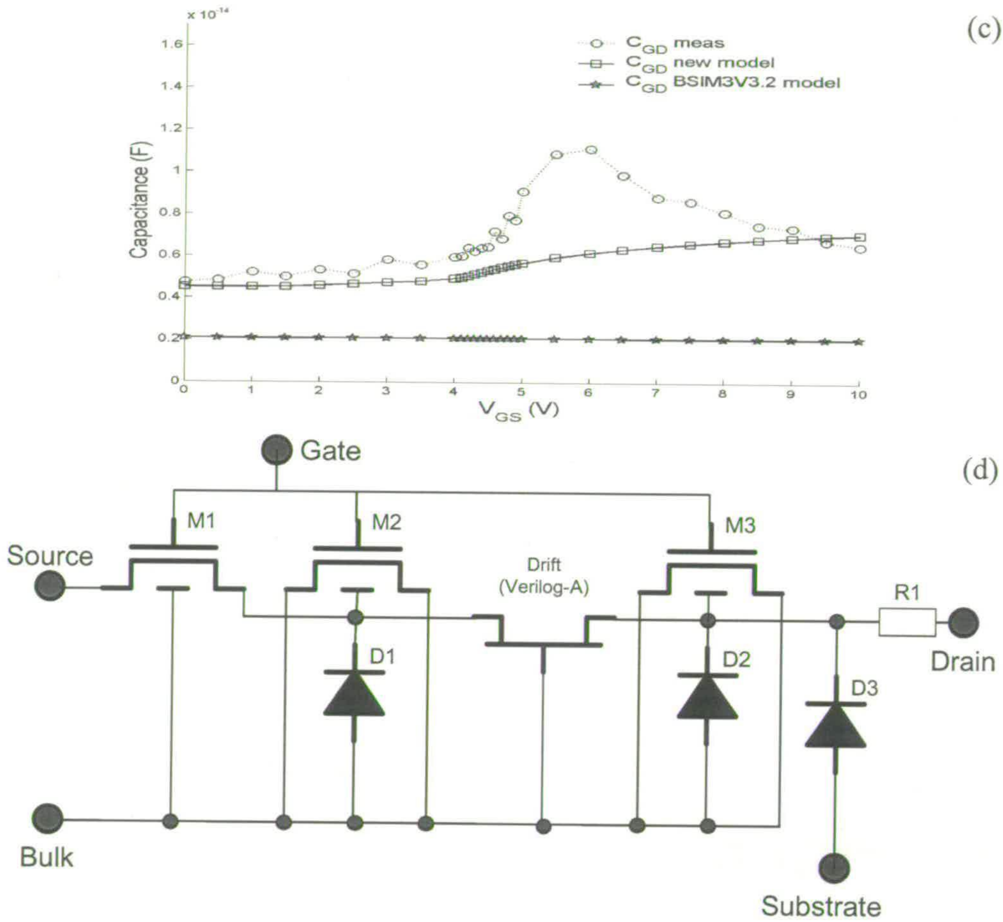


Figure 7.8 Simulated and measured C_{GD} and C_{GS} curves as a function of V_{GS} at $V_{DS} = 0$ and 20V for both the old and new models. (a) Comparison between measurements and simulations based on the new macro-model at $V_{DS} = 0V$; (b) Comparison of C_{GS} measurements and simulations based on the new and old macro-model at $V_{DS} = 20V$; (c) Comparison of C_{GD} measurements and simulations based on the new and old macro-model at $V_{DS} = 20V$; (d) model topology

Figure 7.8 shows the AC-results of the FRERE_V1 model. When $V_{DS} = 0V$ a very good fit is achieved with the FRERE_V1 model compared with the old BSIM3V3.2 one, which struggles to fit the capacitances. For V_{DS} higher than 0V the fit has a maximum error of 30%, which is considered a good fit for highly bias dependent capacitances. The peaks observed in the measured C_{GS} and C_{GD} curves (Figure 7.8(b) and (c)) are very difficult to mimic. However, the FRERE_V1 model shows an increase at the correct location, which is not present in the old model.

The distinctive characteristic of LDMOS capacitances is due to the behaviour of the drift region as explained in chapter 5. The increased understanding of the drift region has been fundamental in enabling an improved model to be developed.

7.4 Model parameter extraction procedure

7.4.1 Geometry parameters

Several device parameters relate to the layout of the devices and are technology dependent. They define the scaling of the model and have to be specified before the extraction.

Parameter	Meaning
TOX	Oxide Thickness
LCH	Channel Length
LGOX	Length Thin Gate Oxide above Drain
LFOX	Length of Field Oxide
LSDIF	Half Length of Source Diffusion
LDDIF	Half Length of Drain (Contact) Diffusion
LDI	Distance Between Drain Diffusion to Isolation ifo the length of the device
WBE	Extension of Body Region over Channel
WDI	Distance Between Drain Diffusion to Isolation ifo the width of the device

Table 7.1 Description of the different geometry parameters

For each device, the total channel width W and the number of gate stripes (NS) has to be specified. With W and NS as input, the size of the electrically efficient layers of the device is calculated from the parameters described in Table 7.1.

7.4.2 Extraction of subthreshold parameters

The parameters of the subthreshold region are simply those of the BSIM3V3.2 model and can be extracted using procedures described in the literature [1]. For the examples which are described only 3 parameters have been optimised.

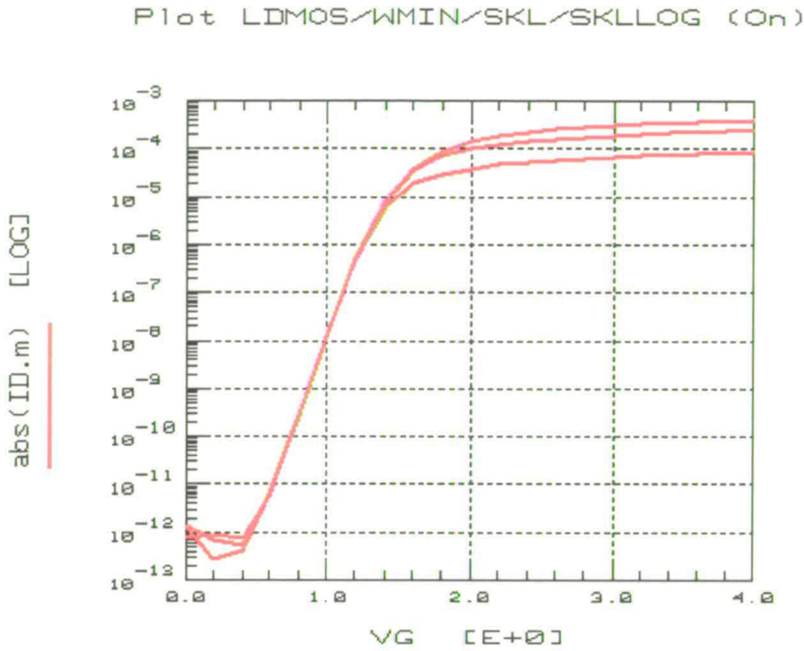


Figure 7.9 LDMOS, Ids-Vgs curve, different W, logarithmic scale

Target device:	intermediate to large widths
Target curve:	I_{DS} vs V_{GS} @ $V_{DS} < V_{DSNK}$ (Triode Region), 25°C

Parameter	Meaning	Typ. Value
VTH0	Threshold Voltage	1.0 [V]
NFACTOR	Subthreshold Slope Factor	1
VOFF	Vth offset between Subthreshold and Triode Region	-0.08 [V]

Table 7.2 Subthreshold parameters

7.4.3 Triode parameters

Triode parameters are extracted on the same curve, but now for the region above threshold as shown in figure 7.10.

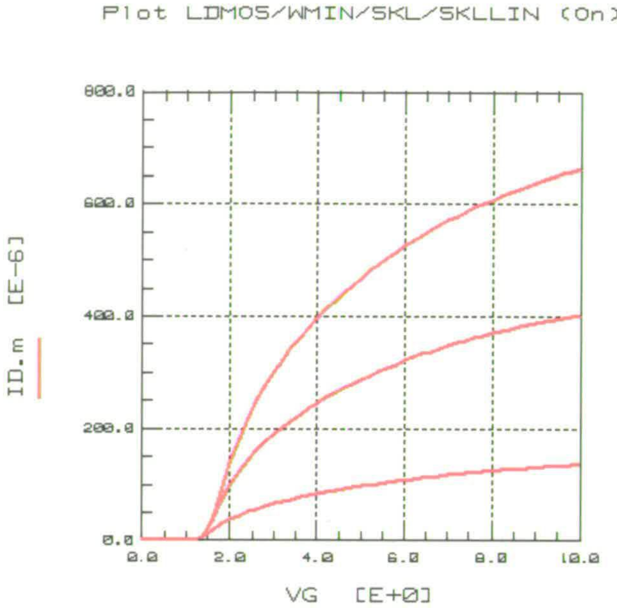


Figure 7.10 LDMOS, Ids-Vgs curve, different Widths, linear scale

Target device:	intermediate to large widths
Target curve:	I_{DS} vs V_{GS} @ $V_{DS} < V_{DSNK}$ (Triode Region), 25°C

Parameter	Meaning	Typ. Value
U0	Channel Mobility	600 [ua/V^2] (NMOS)
RDSER	Constant Drain Resistance	100 [ohm]
UA	Mobility Saturation Parameter	10 e^{-9} [m/V]
UB	Mobility Saturation Parameter, VGS dependence	-1e^{-17} [$(m/V)^2$]

Table 7.3 Triode parameters

7.4.4 Extraction of saturation region parameters

7.4.4.1 Saturation region parameters, intermediate V_{DS}

In principle, these parameters can be extracted in accordance with the BSIM3V3 description and should model the region of intermediate drain voltages (between quasi-saturation and breakdown as indicated on Figure 7.11 with an ellipse).

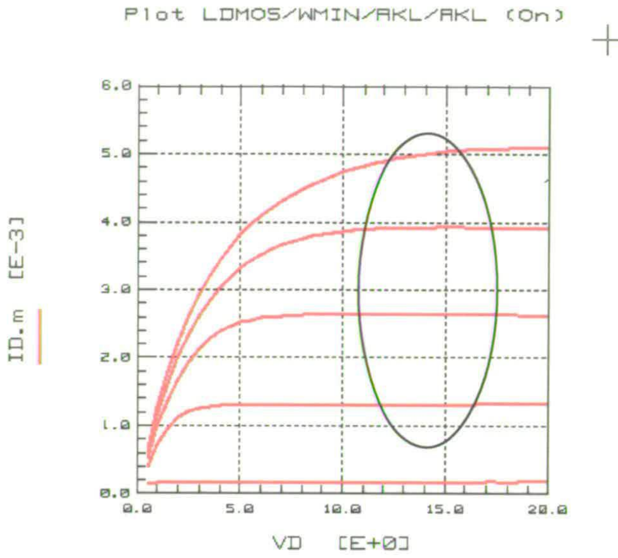


Figure 7.11 LDMOS, Ids-Vds curve, different Vgs, linear scale

Target device:	minimum width
Target curve:	I_{DS} vs V_{DS} @ several V_{GS} (Saturation Region, intermediate V_{DS}), 25°C

Parameter	Meaning	Typ. Value
A0	Bulk Charge Parameter	1
AGS	Gate Dependence of A0	0 [1/V]
PCLM	Channel Length Modulation Parameter	1.0
VSAT	Carrier Saturation Velocity	$80e^3$ [m/sec]

Table 74 Saturation parameters

7.4.4.2 Quasi-saturation region parameters, low V_{DS}

As the quasi-saturation is characteristic for DMOS devices and cannot be modelled by a standard model, the JFET parameters modelling this region (as indicated in Figure 7.12 with a ellipse) are extracted:

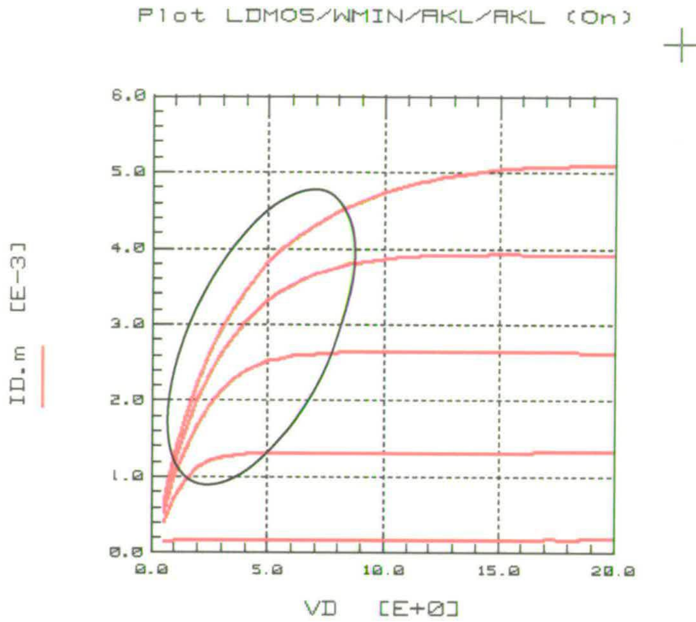


Figure 7.12 LDMOS, I_{DS}-V_{DS} curve, different V_{GS}, linear scale

Target device:	minimum to intermediate width (no self heating)
Target curve:	I_{DS} vs V_{DS} @ several V_{GS} (saturation region, low V_{DS}), 25°C

Parameter	Meaning	Typ. Value
Beta_JFET	Beta efect parameter of the JFET	1 x 10e-3 [A/V^2]
Lambda_JFET	Lambda effect parameter of the JFET	1 [1/V]
VT_jfet_X1	VT_JFET equation parameter	1.5 [V]
VT_jfet_Y1	VT_JFET equation parameter	0.5
VT_jfet_X2	VT_JFET equation parameter	2.5 [V]
VT_jfet_Y2	VT_JFET equation parameter	1.5
VT_jfet_X3	VT_JFET equation parameter	3.5 [V]
VT_jfet_Y3	VT_JFET equation parameter	2.5

Table 7.5 JFET parameters modelling quasi-saturation

See Figure 7.13 for an explanation of the parameters.

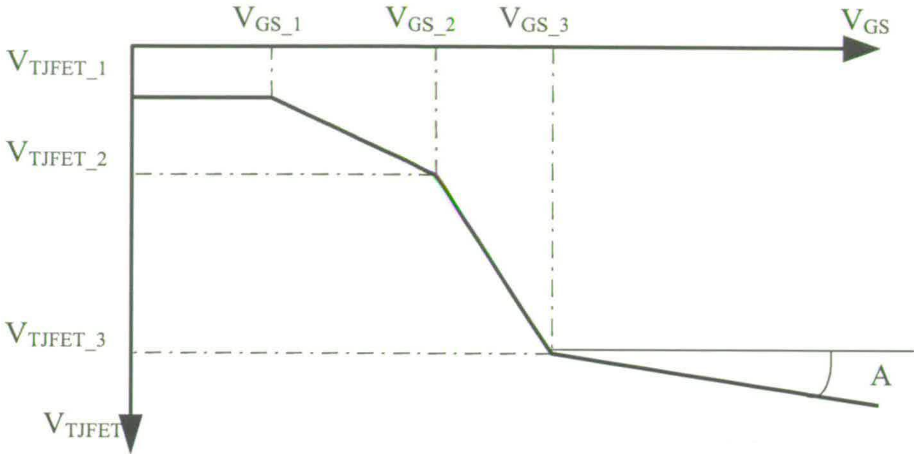


Figure 7.13 JFET V_T behaviour in relation to the LDMOS V_{GS}

7.4.5 Extraction of temperature parameters

7.4.5.1 Subthreshold temperature parameters

For our approach, the use of the BSIM3V3.2 parameters, which models the threshold voltage has proved to be very suitable:

Target device:	minimum to intermediate width
Target curve:	I_{DS} vs V_{GS} @ several V_{DS} (Subthreshold Region), several temperatures.

Parameter	Meaning	Typ. Value
KT1	Temperature Coefficient VTH	-800m [V}

Table 7.6 subthreshold temperature parameter

7.4.5.2 Linear region temperature coefficients

Here, the temperature coefficients of the BSIM3V3.2 mobility model and of the constant drain resistance are determined

Target device:	minimum to intermediate width (no self heating)
Target curve:	I_{DS} vs V_{GS} @ V_{DS} = const (Triode Region), several temperatures

Parameter	Meaning	Typ. Value
UTE	Exponential Temperature Coeff. of Mobility	-1.5

TCR1	1st order Temperature Coefficient RD	$4e^{-3}$
TCR2	2nd order Temperature Coefficient RD	$10e^{-6}$

Table 7.7 linear region temperature parameters

7.4.5.3 Saturation region temperature coefficients

The temperature coefficients for the saturation region are determined in one step

Target device:	minimum to intermediate width (no self heating)
Target curve:	I_{DS} vs V_{DS} @ several V_{GS} (Saturation Region), several temperatures

Parameter	Meaning	Typ. Value
AT	Temperature Coefficient Saturation Velocity	-1.5 [m/sec]

Table 7.8 Saturation temperature parameters

7.4.6 AC-parameter extraction

As explained previously the JFET approach uses two shorted PMOS devices and two diodes to model the AC behaviour of the LDMOS. The following set of parameters is extracted / optimised:

Parameter	Meaning	Typ. Value
CGD0I	Constant Overlap Capacitance per Width	$100e^{-12}$ [F/m]
CGS0I	Constant Overlap Capacitance per Width	$100e^{-12}$ [F/m]
CGB0I	Constant Overlap Capacitance per Width	$100e^{-12}$ [F/m]
CGD0S1	Constant Overlap Capacitance per Width	$100e^{-12}$ [F/m]
CGS0S1	Constant Overlap Capacitance per Width	$100e^{-12}$ [F/m]
CGB0S1	Constant Overlap Capacitance per Width	$100e^{-12}$ [F/m]
VTH0S1	Threshold Voltage of shorted mos	1 [V] (*)
LCHS1	Channel Length of shorted mos	1µm
CGD0S2	Constant Overlap Capacitance per Width	$100e^{-12}$ [F/m]
CGS0S2	Constant Overlap Capacitance per Width	$100e^{-12}$ [F/m]
CGB0S2	Constant Overlap Capacitance per Width	$100e^{-12}$ [F/m]
VTH0S2	Threshold Voltage of shorted mos	1 [V] (*)
LCHS2	Channel Length of shorted mos	1 µm

Table 7.9 AC-parameters

(*)The sign is dependent on the type of LDMOS: n-type or p-type. For an n-LDMOS device a negative value should be applied as the shorted MOS is a p-type MOS.

The measurements needed to extract the capacitance values are S-parameters measurements. This type of measurement has the advantage that standard geometries of devices can be used for measurements instead of larger geometries needed for CV-measurements. An example of these curves is shown in Figure 7.14

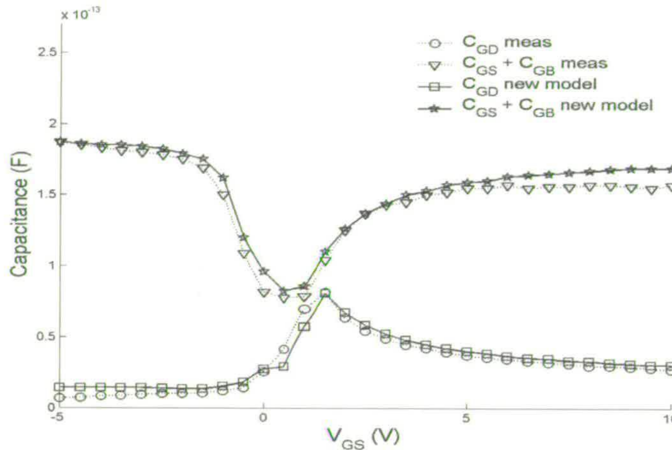


Figure 7.14 Simulated and measured C_{GD} and C_{GS} curves as a function of V_{GS} at $V_{DS} = 0$

7.4.7 Diode DC-parameters

The definition and the extraction of the DC parameters of the parasitic diodes (JS, N, RS) has been described in chapter 3.

7.5 Worst-case corner extraction

7.5.1 Introduction

A commonly used approach to create worst-case models is to use a Monte-Carlo analysis to build a large statistical database of accurate model parameter sets based on the direct extraction of parameters on a large population of devices. This involves measuring the complete I-V characteristics on all samples, extracting models using optimisation, studying the correlations between measured electrical device parameters and extracted model parameters, and the building of a regression model. Such an approach however results in the optimiser-based procedure skewing the distributions, adding variability and unexpected correlations [3]. An alternative methodology is proposed where the optimiser-based extraction step is circumvented by building a local inverse of the mapping from the model parameters to the electrical parameters around

the typical model [4]. Building this local inverse involves sampling the model parameter space and performing an analysis of the sensitivity of the simulated electrical parameters with respect to some key model parameters. The method used to build this inverse mapping around the typical parameter set involves training a neural network [5].

7.5.2 Device and technology description

A cross-section of the device under investigation is presented in Figure 7.15. The I2T-flow is based on a 0.7μm CMOS process to which some extra masks and implants have been added to provide the high-voltage features. From Figure 7.15 it can be observed that the LDMOS transistor is an asymmetric device, with the drift region on the drain-side located in a lightly doped N-tub.

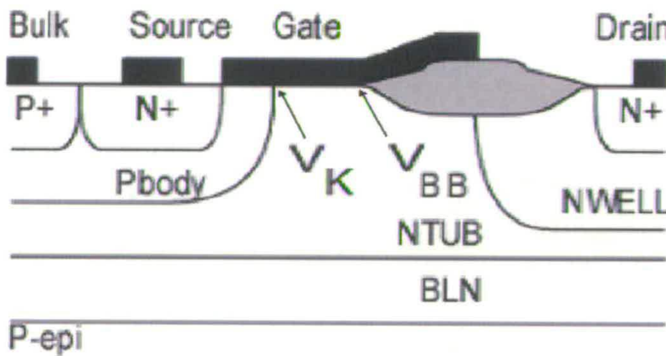


Figure 7.15: Section through an LDMOS.

The channel is self-aligned to the source and is created by the out-diffusion of the P-body under the gate. As a result the dopant distribution along the channel is non-uniform and decreases towards the drain end. Higher breakdown voltages are achieved due to the depletion region that extends from the P-body into the drain, which provides a voltage drop between the drain contact and the channel region. The gate oxide and the polysilicon extend beyond the channel of the device as illustrated in Figure 7.15.

A systematic monitoring is performed on the following key parameters (called E-test parameters) of the LDMOS transistor:

Transconductance:

$$GM_{\max} = \left(\frac{dI_D}{dV_{GS}} \right)_{\max} \quad \text{at } V_{DS} = 100\text{mV} \tag{7.1}$$

Extrapolated threshold voltage:

$$VTH = V_{GS}(GM_{max}) - \frac{I_D(GM_{max})}{GM_{max}} - \frac{V_{DS}}{2} \tag{7.2}$$

at V_{DS} = 100mV

Saturation current:

$$IDSAT = I_D \text{ at } V_{DS} = 25\text{V and } V_{GS} = 5\text{V} \tag{7.3}$$

On-resistance:

$$RON = \frac{V_{DS}}{I_D} \text{ at } V_{DS} = 500\text{mV and } V_{GS} = 12\text{V}. \tag{7.4}$$

The observation of these characteristics is a standard procedure used to monitor the stability of the production process. As a consequence a large database is generated providing statistically relevant information for every processed device.

7.5.3 Mapping of electrical parameter space onto model parameter space

7.5.3.1 Identification of key model parameters based on sensitivity analysis

In order to be able to construct a mapping from the electrical parameter space onto the model parameter space, it is important to limit the number of model parameters to a set that is able to describe the process variations. A sensitivity analysis therefore is performed to investigate the impact of the model parameters on the simulated device characteristics. The sensitivities are calculated using a measurement-based perturbation method, where a specified parameter p is perturbed from its nominal value by an amount Δp, and the change ΔF on the specified performance measure F for the device is determined. For meaningful comparisons, the result is normalised. Thus, the normalised sensitivity is determined as:

$$sensitivity = \frac{\Delta F / F}{\Delta p / p} \tag{7.5}$$

The model used to characterise the LDMOS device is a macro-model [6]. The corner extraction methodology described in this paper has been developed for DMOS devices, but could as well be applied to other devices.

For each electrical device parameter (VTH, GM_{max}, IDSAT and RON) a sensitivity analysis was performed. This analysis resulted in a set of model parameters that capture

most of the variability of the E-test parameters (see Table 7.10). The definition of these model parameters is as follows:

vth0: threshold voltage of the MOS transistor modelling the channel of the LDMOS,
u0: mobility of the MOS transistor modelling the channel of the LDMOS,
Vsat: saturation velocity of the MOS transistor modelling the channel of the LDMOS,
R: series resistance parameter modelling the on-resistance of the LDMOS, and
Tox: oxide thickness of the MOS transistor modelling the channel of the LDMOS.

	E-test parameter			
Model parameter	VTH	GM_{max}	IDSAT	RON
vth0	106%	-23.7%	-36.5%	9.2%
u0	-1.8%	82.5%	32.6%	-40.7%
Vsat	-0.3%	16.7%	81.6%	-19.3%
R	-0.1%	-15.1%	-26.2%	72.0%
Tox	-1.4%	-61.1%	-31.9%	8.8%

Table 7.10: Impact of the key model parameters on the E-test parameters.

7.5.3.2 Building the local inverse mapping

After identification of the key model parameters affecting E-test measurements, it is helpful to then build an approximate inverse mapping of the relation between the simulated E-test measurements and model parameters. This approach enables all measured E-test parameter vectors to then be directly translated into model parameter vectors. The method used in this work for building the inverse mapping is to use the typical model (matching nominal device performances) and then employ a full functional to vary the model parameters and obtain simulated E-test data. Once matching pairs of E-test and model parameter vectors are obtained, they are fed as training data to a neural network in order to achieve the desired inverse mapping. A schematic overview of this procedure is presented in Figure 7.16. The type of neural network used here is a multi-layer perceptron with 5 input neurons, 1 intermediate layer containing 7 neurons, and 5 output neurons, in combination with the quasi-Newton training algorithm.

With 3,000 data-points, a round-trip accuracy of the order of 1% or better is obtained.

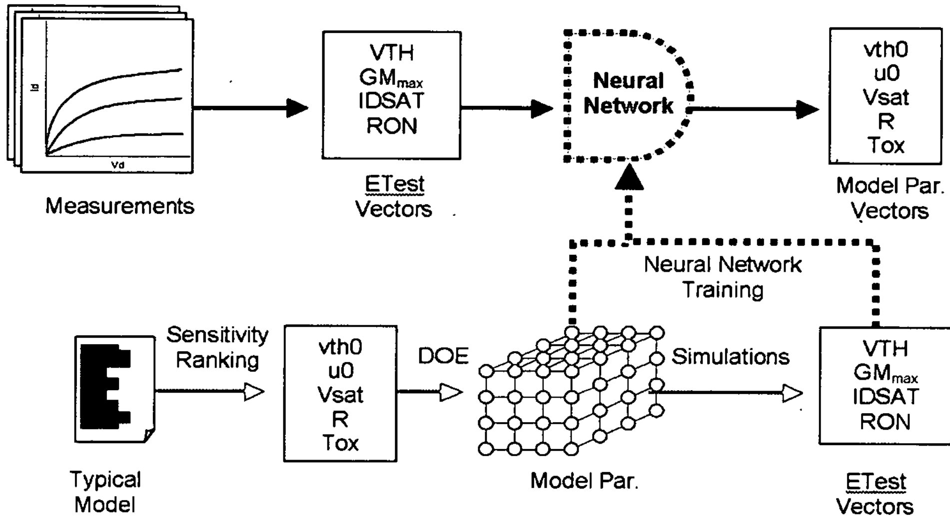


Figure 7.16: Flow for translating E-Test parameter vectors into model parameter vectors.

The total time needed to simulate the device for all different model parameter values is around 4 hours, while the time needed to train the neural network is only a couple of minutes. It is clear that this method constitutes a speed improvement over the method described in [3].

Once the neural network is trained and the accuracy of the approximation is assessed, it is possible to feed a large set of measured E-test parameter vectors to the neural network, such that a large population of model parameter vectors can be obtained.

7.5.4 Generation of worst-case models based on a multivariate analysis

7.5.4.1 Univariate approach

The philosophy used for corner simulations and worst-case models is all about the level of guarantee that these simulations can give the product. Therefore the worst-case models are defined as a function of a specific performance measure and a confidence level. The confidence level is defined as the probability of finding devices in the population with performances within the two extreme values of the worst-case models.

The traditional methodology used to generate worst-case models consists of performing a univariate statistical analysis on individual E-test parameters, selecting corner values for each individual parameter based on a desired confidence level, and fitting the model parameters to the generated worst-case parameter sets. The problem with this approach

is that it does not take into account correlations between E-test parameters and as a consequence the combinations of worst-case E-test parameters may be unrealistic in practice.

7.5.4.2 Multivariate approach

The methodology proposed here starts from a multivariate analysis on a large population of data and there are two approaches. These are either an examination of the E-test parameter vectors or the model parameter vectors, translated from E-test parameter space by the neural network. Both methods have been investigated in order to see if comparable results are obtained.

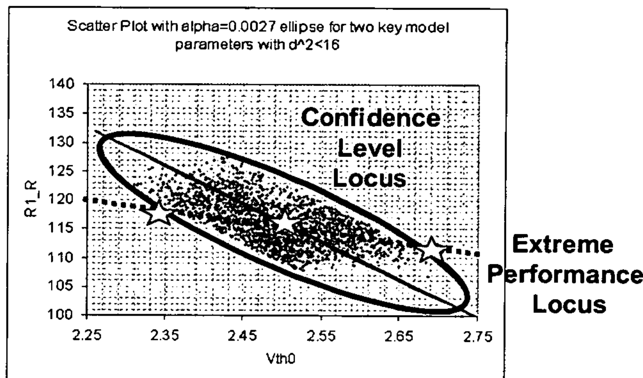


Figure 7.17: Corners as the intersection of the extreme performance locus and the 99.73% confidence locus of the population.

Setting the location of the worst-case models in the model parameter space is achieved by identifying devices with extreme performances along the specified confidence-level locus of the population. In the case of a multivariate normal distribution, the confidence locus is an ellipsoid, with all points at a fixed variance-weighted distance from the typical model. This ellipsoid can be obtained using Principal Component Analysis (PCA). Figure 7.17 shows a graphical representation of the corner selection process. In the particular case shown here, the performance measure chosen was a combination of DMOS switching speed and *RON* performance.

The resulting worst-case models are displayed in Figure 7.18 in terms of parameter excursions from the typical values, normalised by the univariate standard deviations.

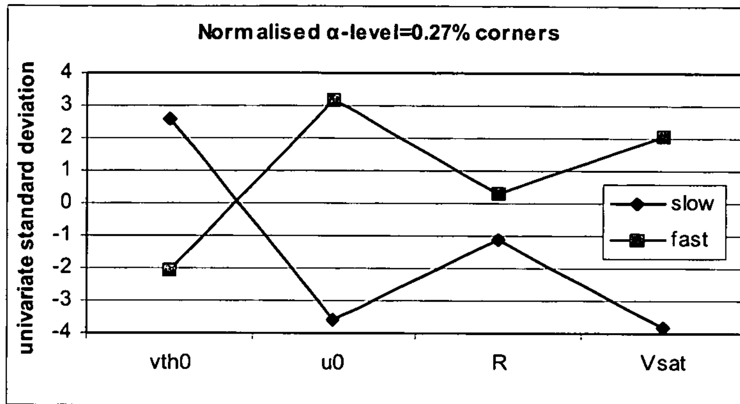


Figure 7.18: Parameter excursions for worst-case models normalised to univariate standard deviations.

A comparison between the two methods (analysis on model parameters versus analysis on E-test parameters respectively) is shown in Table 7.11. It can be observed that the relative differences between E-test worst-case values generated by both methods are less than 4%. As the neural network mapping has accuracy better than 1%, these errors can be attributed to the non-linear character of the DMOS model and the linear character of the principal component analysis. Indeed, if a confidence locus is an ellipsoid in one domain, then the transformed locus will not be an ellipsoid, and as a result it cannot be obtained using PCA in the other domain.

Slow corner			
	E-test space	Model space	Difference
VTH (V)	2.759	2.763	0.1%
GM_{max} ($\mu A/V^2$)	1216	1174	-3.5%
RON (Ω)	305.2	304.1	-0.3%
IDSAT (μA)	1646	1610	-2.2%
Fast corner			
	E-test space	Model space	Difference
VTH (V)	2.389	2.385	-0.2%
GM_{max} ($\mu A/V^2$)	1405	1390	-1.1%
RON (Ω)	279.4	276.1	-1.2%
IDSAT (μA)	2479	2461	-0.7%

Table 7.11: Comparison between worst-case corners obtained from analysis on model parameter space versus E-test parameter space.

It is clear that any analysis should strive to make principal component analyses in a domain constituted by parameters, which are either uncorrelated or related in a linear fashion to each other, e.g. dimensions and physical material parameters. In some sense model parameters are one step closer to such parameters than E-test parameters, which can be illustrated by the fact that *IDSAT* distributions are inherently non-normal.

7.5.5 Monte-Carlo models

After translation of a large set of E-test parameter vectors to model parameter space by the trained neural network, it is possible to create a Monte-Carlo model. Indeed, after performing a principal component analysis on the model parameter data set, a set of linearly independent vectors in model parameter space are available. These vectors, together with the appropriate eigenvalues (variances) can be fed to a Monte-Carlo analysis tool inside a circuit simulator.

7.6 Conclusion

This chapter has presented the macro model topology. The different components needed to build up the model were discussed together with a variation on how to model the AC-behaviour. An extraction procedure covering all aspects of the model was presented. In addition to a good basic model, it is important that process variations can be accounted for by the model and a novel technique to do this has been described. This chapter introduced a new complete macro-model and in the next chapter this will be tested and compared to the targets set at the beginning of the thesis.

References

[1] Y.Cheng; "MOSFET Modeling & BSIM3 User's guide," Kluwer Academic Publishers; 1999.

[2] "Affirma Spectre Circuit Simulator Reference," Cadence Design Systems, 1999, www.cadence.com.

[3] S. Healy, E. Horan, K. McCarthy, A. Mathewson, Z. Ning, E. Rombouts, W. Vanderbauwhede, and M. Tack, "Implementation of Statistical Characterisation and Design Techniques for an Industrial 0.5µm CMOS Technology," ICMTS 1999 Proc., vol. 12, March 1999, pp. 227-232.

[4] M. Qu and M.A. Styblinski, "Parameter Extraction for Statistical IC Modelling Based on Recursive Inverse Approximation," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 16, no. 11, Nov. 1997, pp. 1250-1259.

[5] V. Devabhaktuni, M.C.E. Yagoub, and Qi-Jm Zhang, "A robust Algorithm for Automatic Development of Neural Network Models for Microwave Applications," IEEE MTT-S Digest, Dec. 2001, pp. 2087-2089.

[6] S.F. Frère, J. Rhayem, H.O. Adawe, R. Gillon, M. Tack, and A.J. Walton, "LDMOS Capacitance Analysis versus Gate and Drain Biases, Based on Comparison between TCAD Simulations and Measurements," ESSDERC 2001 Proc. , Sep. 2001, pp. 219-223.

The macro-model: verification / static-aging / self-heating

8 The macro-model: verification / static-aging / self-heating 119

8.1 Introduction 119

8.2 Model verification 119

8.2.1 Introduction 119

8.2.2 Verification methodology 120

8.2.3 Comparison of the extracted model with measurement data. 121

8.2.4 Scalability check 127

8.2.5 Robustness check at device level 129

8.2.6 Comparison and check of E-test parameters. 130

8.2.7 Check of the I-V characteristics for all corners and temperatures 131

8.2.8 Circuit simulation tests with old and new model. 134

8.2.9 Model verification conclusions 139

8.3 Methodology to include static-aging 140

8.3.1 Measurement data and procedure for aging analyses. 140

8.3.2 Static Prediction of DMOS Aging Performance 143

8.4 Methodology to include self-heating 146

8.4.1 Self-heating free measurements 146

8.4.2 Implementation of self-heating in the model. 148

8.5 Conclusion 149

8 The macro-model: verification, static-aging and self-heating

8.1 Introduction

This chapter presents the verification of the macro-model described in chapter 7.
Initial investigations of self-heating effects and static aging of LDMOS devices are presented at the end of the chapter and proposals to include these in simulators presented.

8.2 Model verification

8.2.1 Introduction

The old topology of LDMOS models in I2T100 technology available at AMIS consists of basic standard MOS models (BSIM3V3.2 or MOS LEVEL 1 & 2) and parasitic junction diodes as shown in Figure 8.1.

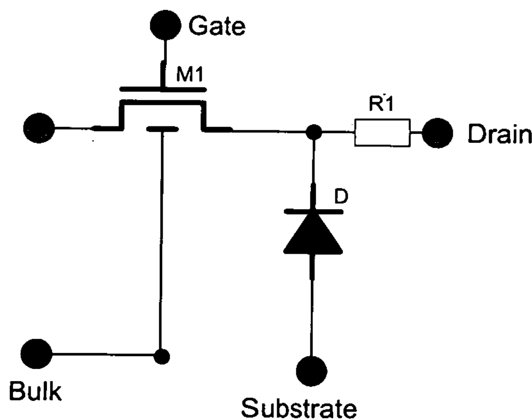


Figure 8.1: old LDMOS model topology.

This basic topology using the standard BSIM3v3 model to simulate a DMOS device showed its limitation in terms of scalability, AC and transient effects as specified in chapter 4. This chapter provides a comparison between the old model that was available at AMIS for the modelling LDMOS devices and the FRERE_V1 model presented in this thesis.

8.2.2 Verification methodology

Extensive verification at device and circuit level was performed to determine the robustness and accuracy of the model.

At device level the following tests were undertaken:

- Ids-Vgs, Ids-Vds at different Vgs, for three corners (typical, slow and fast) and at three different temperatures (-40°C, 25°C and 125°C). This is a visual check to see if the overall curve behaviour of the model remains valid for all temperatures and corners.
- Simulation of E-TEST parameters at three different temperatures. This analysis of the behaviour is to check if the generated corners are valid for all temperatures.
- Robustness test: This is a check to ensure the model does not show convergence problems when applying extreme voltage to its terminals. Typically, these are three times the allowed voltage (i.e. V_{GSmax}=12V, the test is performed at V_{GS} =36V)
- Test the scalability of the main electrical parameters as a function of the channel width.

At circuit level, two designs were provided by the design department of AMIS in order to:

- Check for simulation robustness and convergence problems.
- Check the output performance of the circuit and the impact of the FRERE_V1 model topology on the existing design.
- Check the simulation time, in order to evaluate the impact of the more complex model used in the circuit.

After the above tests were performed on one device, it was decided to install the FRERE_V1 model for all AMIS DMOS devices in the I2T and I3T technologies.
The FRERE_V2 was not yet introduced as the improvement in accuracy is not significant enough compared to the increased simulation time due to the introduction of extra Verilog-A blocks.

8.2.3 Comparison of the extracted model to the measurement data

As an example, a model will be extracted for a 40V LDMOS device form the I2T process.

The following characteristics presented in Table 8.1 were measured on the test-structures presented in chapter 6:

Output Characteristics	
V_{DS} [V]	0 → V_{DSmax} (40V)
V_{GS}[V]	2.7, 3.0, 3.3, 3.6 , 4.5, 6, 7.5, 9, 10.5 and 12V
Transfer Characteristics	
V_{GS} [V]	0 → 13V
V_{DS} [V]	0.1 and V_{DSmax}
C_{GS} and C_{GD}	
V_{GS}: –5 → 10V, V_{DS}: 0.1 and 20V, frequency: 40MHz up to 5GHz	

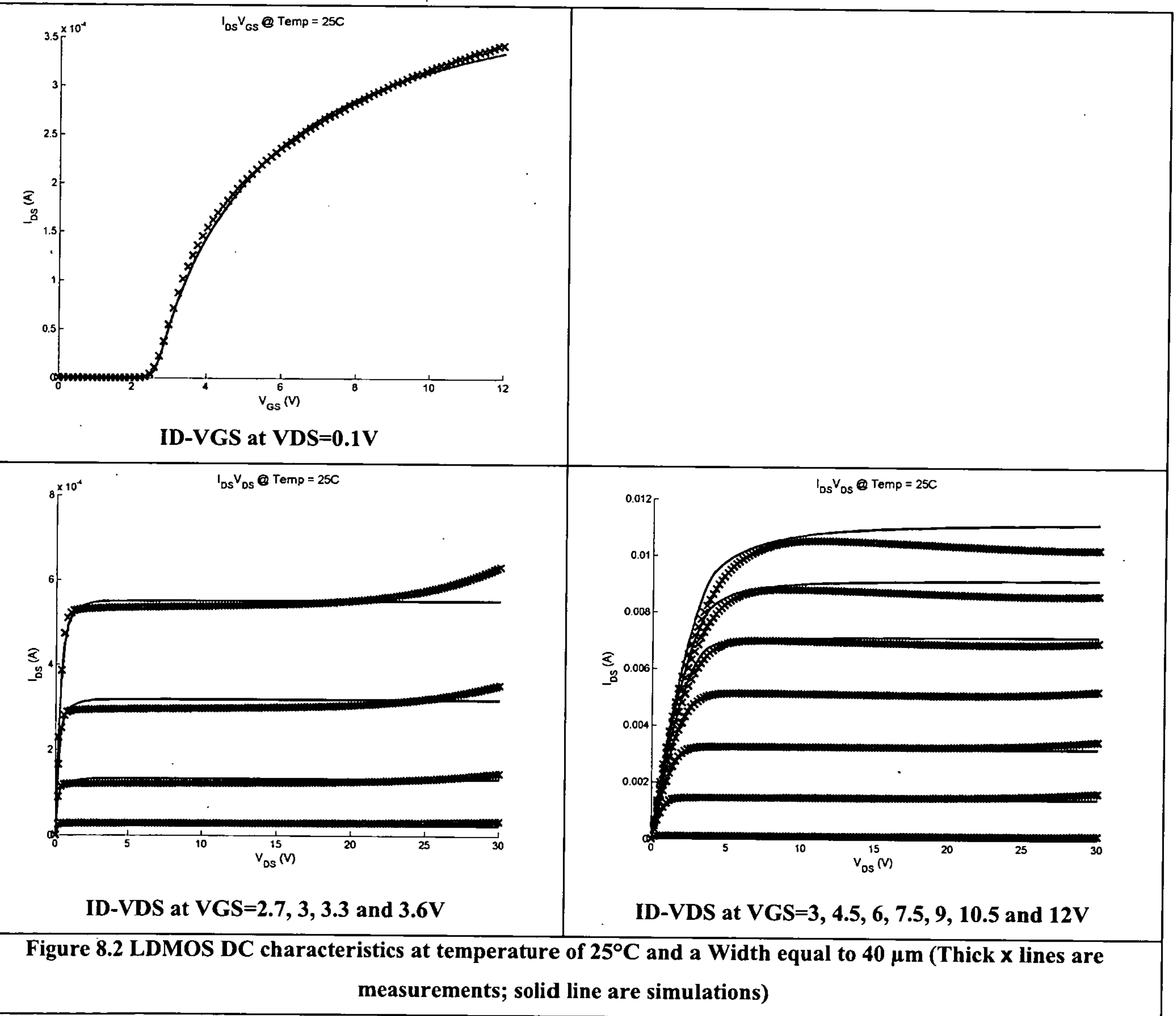
Table 8.1 Range of DC-IV and AC-CV Characteristics.

Based on these measurements a model was extracted which covers the basic DC and AC characteristics of the device. In a second stage, statistical process information (E-test or electrical test parameters) is collected and the worst-case corner extraction method is applied. This results in two corner models (fast and slow).

The next sections show the results for the basic extraction for DC at different temperatures and for AC at different drain bias conditions. For the AC part, a comparison is given between the old and the FRERE_V1 model.

8.2.3.1 DC characteristics

T=25°C



ID-VGS at VDS=0.1V

ID-VDS at VGS=2.7, 3, 3.3 and 3.6V

ID-VDS at VGS=3, 4.5, 6, 7.5, 9, 10.5 and 12V

Figure 8.2 LDMOS DC characteristics at temperature of 25°C and a Width equal to 40 μm (Thick x lines are measurements; solid line are simulations)

T=125°C

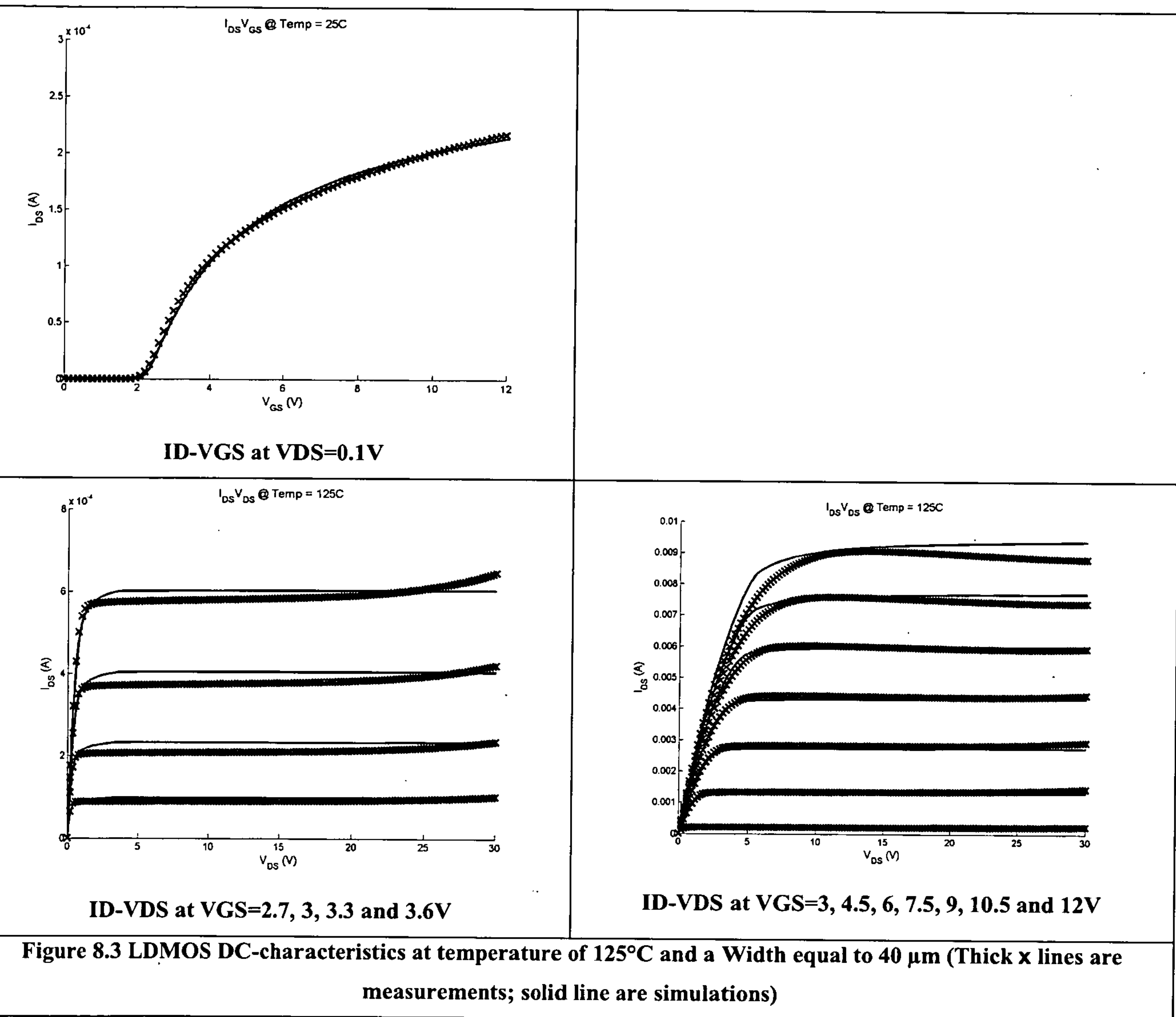
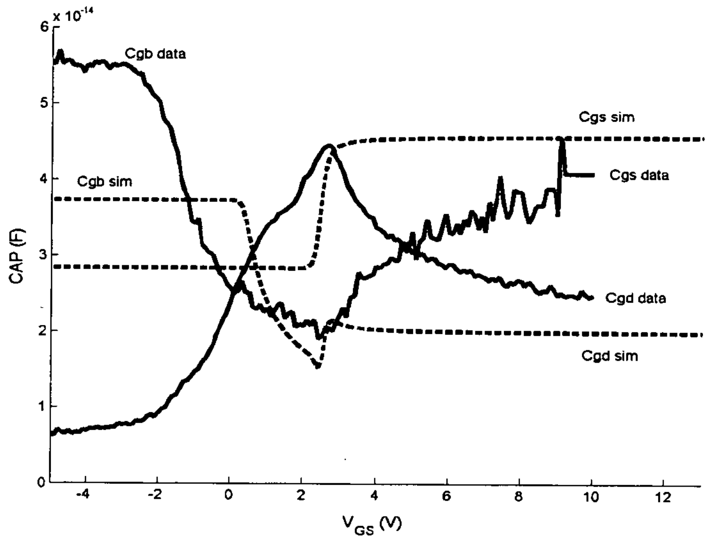


Figure 8.3 LDMOS DC-characteristics at temperature of 125°C and a Width equal to 40 μm (Thick x lines are measurements; solid line are simulations)

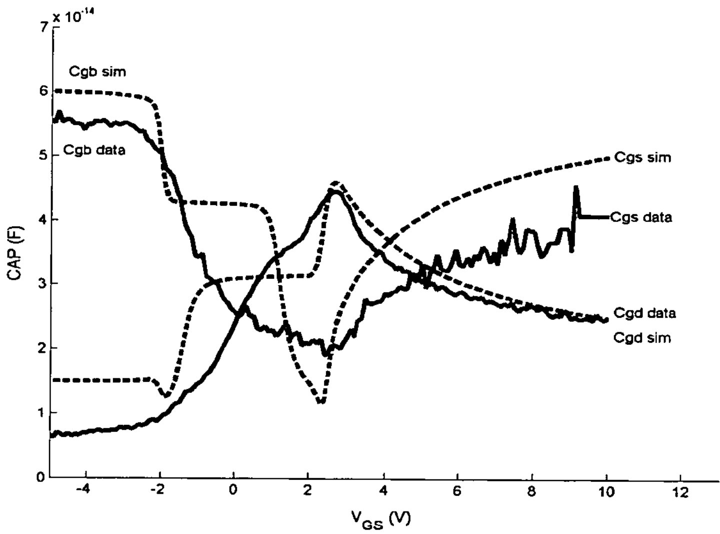
The graphs in Figure 8.2 and Figure 8.3 show a good fit with the measurements. The regions where the fit is poorer, is where self-heating (Ids-Vds at high Vgs) and impact ionisation (high Vds and low Vgs) occur. However, the maximum error in the normal operating regions is always below 10%.

8.2.3.2 AC characteristics

Figure 8.4 shows the comparison between measurements and simulations of the Cgd, Cgs and Cgb capacitances at Vds=0V.

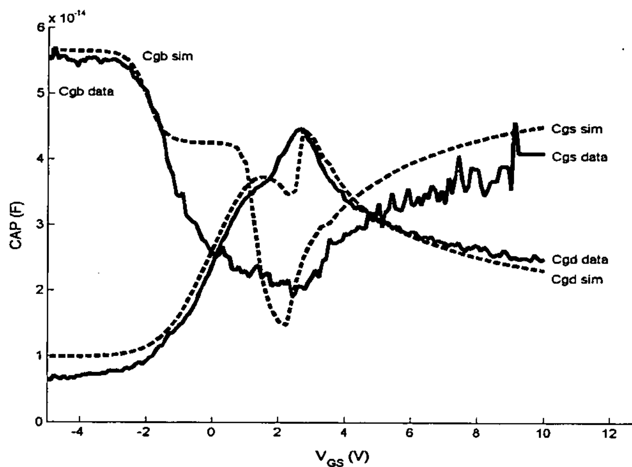


(a) Old topology model at Vds=0V



(b) FRERE_V1 Macro-model with shorted MOS at Vds=0V

Figure 8.4 Comparison of measured and simulated capacitance data with the shorted MOS option at Vds = 0V

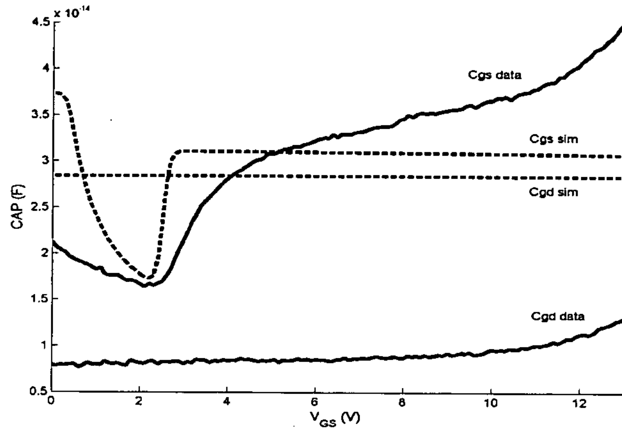


(c) FRERE_V2 Macro-model with Verilog-A block at Vds=0V

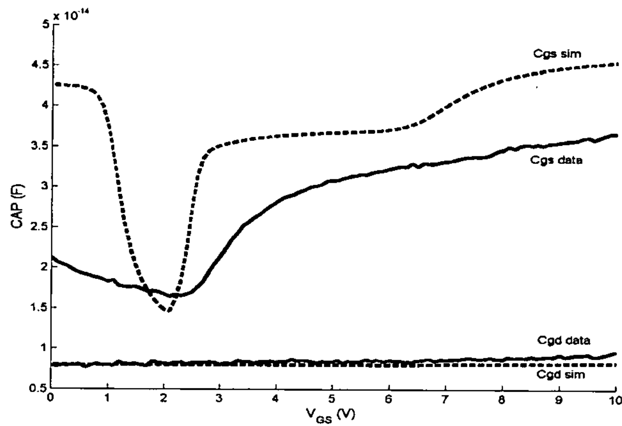
Figure 8.4 Comparison of measured and simulated capacitance data with the shorted MOS option at Vds = 0V

As can be observed in Figure 8.4(a), large differences (over 100%) between measurements and simulations are observed. Figure 8.4(b) indicates that the capacitances are dependent on Vgs. However, a mismatch is observed moving from accumulation to depletion to inversion (region from Vgs=-1V to Vgs=2.5V). This is due to the fact that normal MOS components were used for modelling the capacitance behaviour. These models show a fast transition between accumulation, depletion and inversion, which causes the steps in the graph. However, in the normal operating region (Vgs > 2.5V where the Vth of the device is 2.5V) the fit is very good. The maximum error is less than 20% compared with more than 100% for the old model. In Figure 8.4(c) one can see the results for the LDMOS in which the shorted MOS transistors are replaced by custom-made Verilog-A blocks. This yields an even better capacitance behaviour.

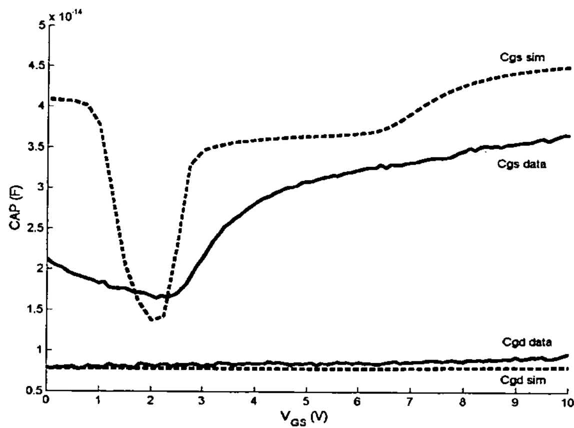
Figure 8.5 shows the comparison between measurements and simulations of the Cgd, Cgs and Cgb capacitances curves at Vds=20V.



(a) Old topology model at Vds=20V



(b) Macro-model with shorted MOS at Vds=20V



(c) Macro-model with Verilog-A block at Vds=20V

Figure 8.5 Comparison of measured and simulated capacitance data with the shorted MOS option at Vds = 20V

In Figure 8.5(a) it can be seen once again that the capacitance values, predicted by the old topology, are independent of Vgs with Cgs being underestimated and Cgd

overestimated. Figure 8.5(b) shows that the FRERE_V1 model exhibits good behaviour. However, the fit is not yet perfect with the maximum error remaining below 30%. In Figure 8.5(c) it can be observed that the fit between measured and simulated data is good. The error remains below 30% which meets the targets set in chapter 4.

8.2.4 Scalability check

In Figure 8.6, (RON x W) and (IDSAT / W) versus width simulated with both the old (dashed lines) and the FRERE_V1 model (continuous line) is presented. The channel width ranged from 4μm up to 35mm. For this type of devices it is extremely important that good scalability behaviour is obtained over a wide range, as the LDMOS can be used in this range. However, the MOS model, on which the old model is based, is not designed to be used for such a large width, hence the scalability problem.

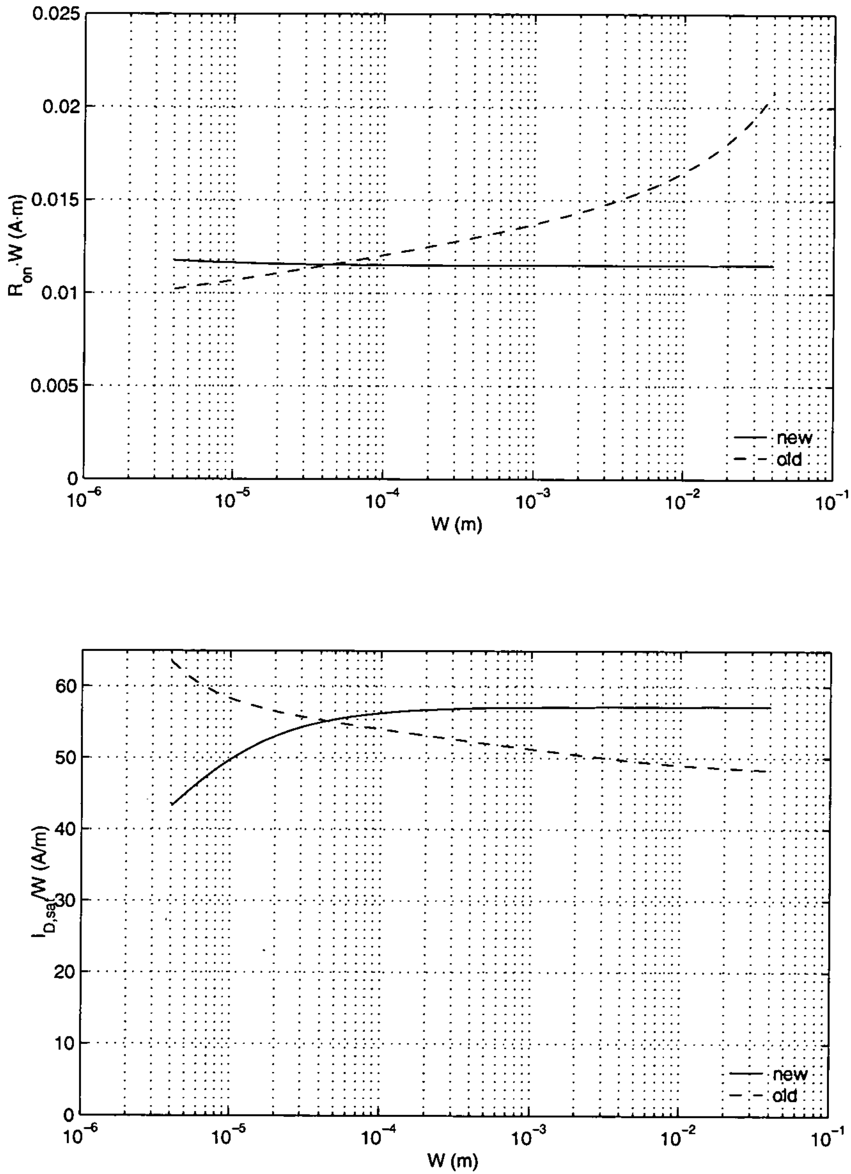


Figure 8.6 evolution of (RON*W) and (IDSAT/W) versus W for the extracted model

A good scalability of RON x W versus width results is a constant value as a function of width. As can be seen on Figure 8.6 the old model is clearly not scalable. I_{DSAT}/W as a function of width should result in the relationship like the continuous line of the FRERE_V1 model, which scales well.

8.2.5 Robustness check at device level

A robustness check requires that the normal maximum bias conditions (for the device under test, this is Vds=40V and Vgs=12V) are multiplied by three and applied to the model. Even at these voltages the model should be robust, for example to cover a voltage spike during switching. The results of the robustness check are given in Figure 8.7. They show that no spikes / discontinuities in the curves occur, confirming that the model satisfies the robustness test.

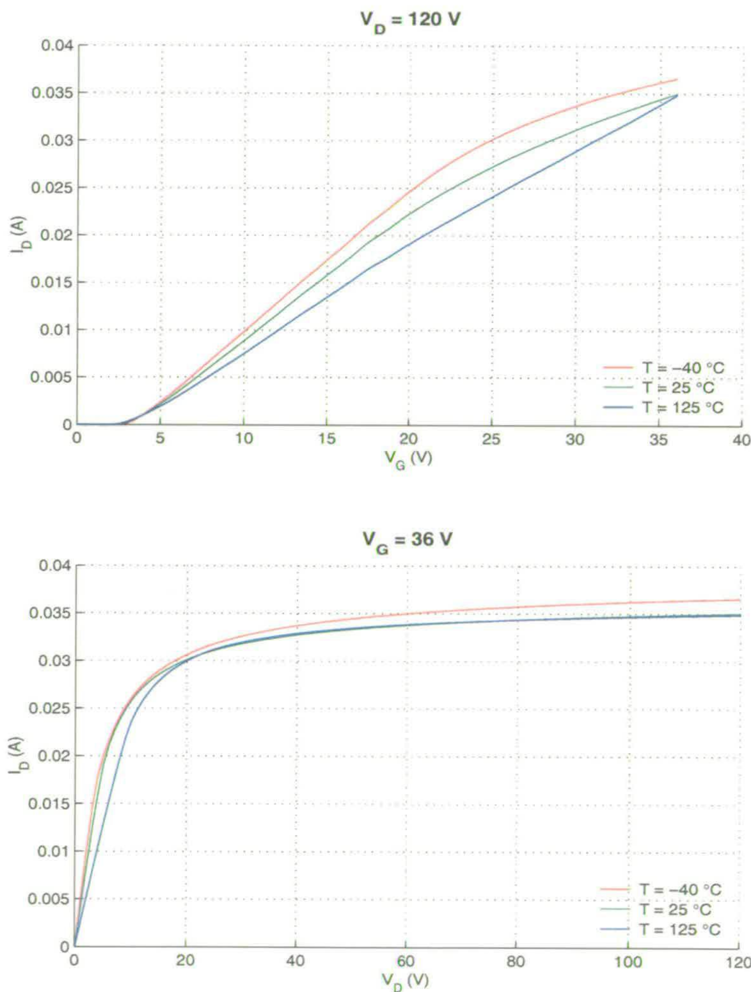


Figure 8.7 Robustness test at device level of the extracted model.

8.2.6 Comparison and check of E-test parameters.

In this section the E-TEST parameters simulated using the FRERE_V1 model topology for three different temperatures (-40°C, 27°C, 125°C) are presented. This check has been undertaken to verify the corners that were extracted using the worst-case corner extraction method described in chapter 7. The results can be seen in Figure 8.8.

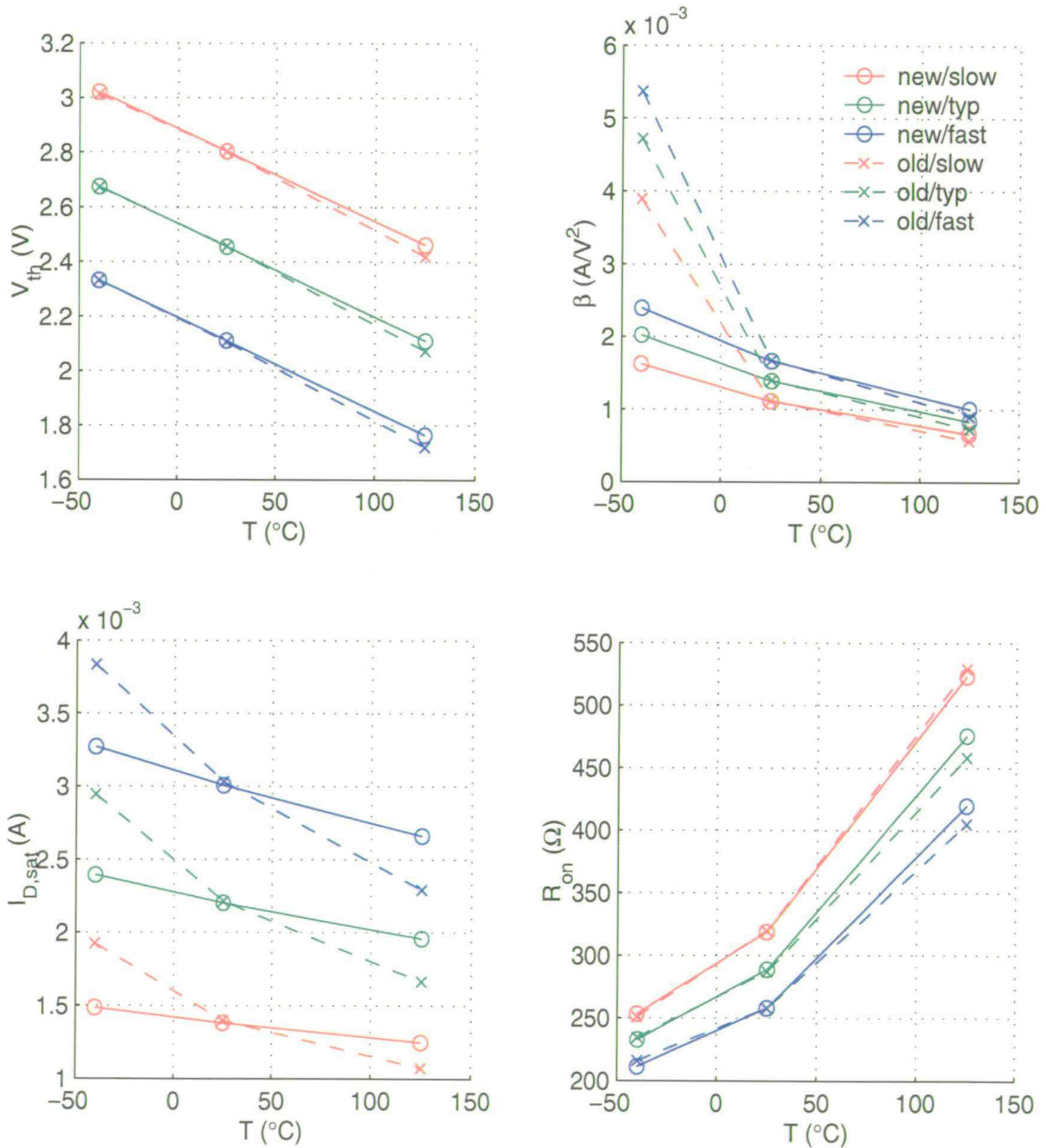


Figure 8.8 Simulated E-test parameters for three corners at three temperatures for the extracted model.

Table 8.2 compares the statistically measured E-test parameters with the E-test parameters extracted from the FRERE_V1 model.

W=40μm T=25°C	typ		slow		fast	
	Data	model	data	model	data	model
VTH(V)	2.45	2.4483	2.8	2.7979	2.1	2.1043
BETA(μA/V^2)	1375	1376	1100	1101	1650	1649
RON(Ohm)	290	289.7	320	320.6	260	258.8
IDSAT(mA)	2.2	2.197	1.4	1.38	3	3

Table 8.2 Comparison of the statistically measured E-test parameters with the E-test parameters extracted from the FRERE_V1 model based on the worst-case corner extraction method previously described.

One can conclude that for the E-test check the FRERE_V1 model has valid worst case fit for all temperatures, and that the fit of the statistically measured E-test parameters with the E-test parameters extracted from the FRERE_V1 model is very good.

8.2.7 Check of the I-V characteristics for all corners and temperatures

In the previous section only E-TEST points were checked for their behaviour over temperature and different corners. In this section, the I-V characteristics at the E-TEST specifications have been simulated with the FRERE_V1 model topology and are compared with the ones simulated using the old model topology.

This test is performed after the previous one is completed and has good results. It is not because a good fit is obtained over the E-TEST points that the full curves are ok. It can be possible that one is able to fit the E-test targets without having a good overall fit.

Figure 8.9 and Figure 8.10 show Ids-Vgs ; gm-Vgs ; Ids-Vds curves over temperature and corners.

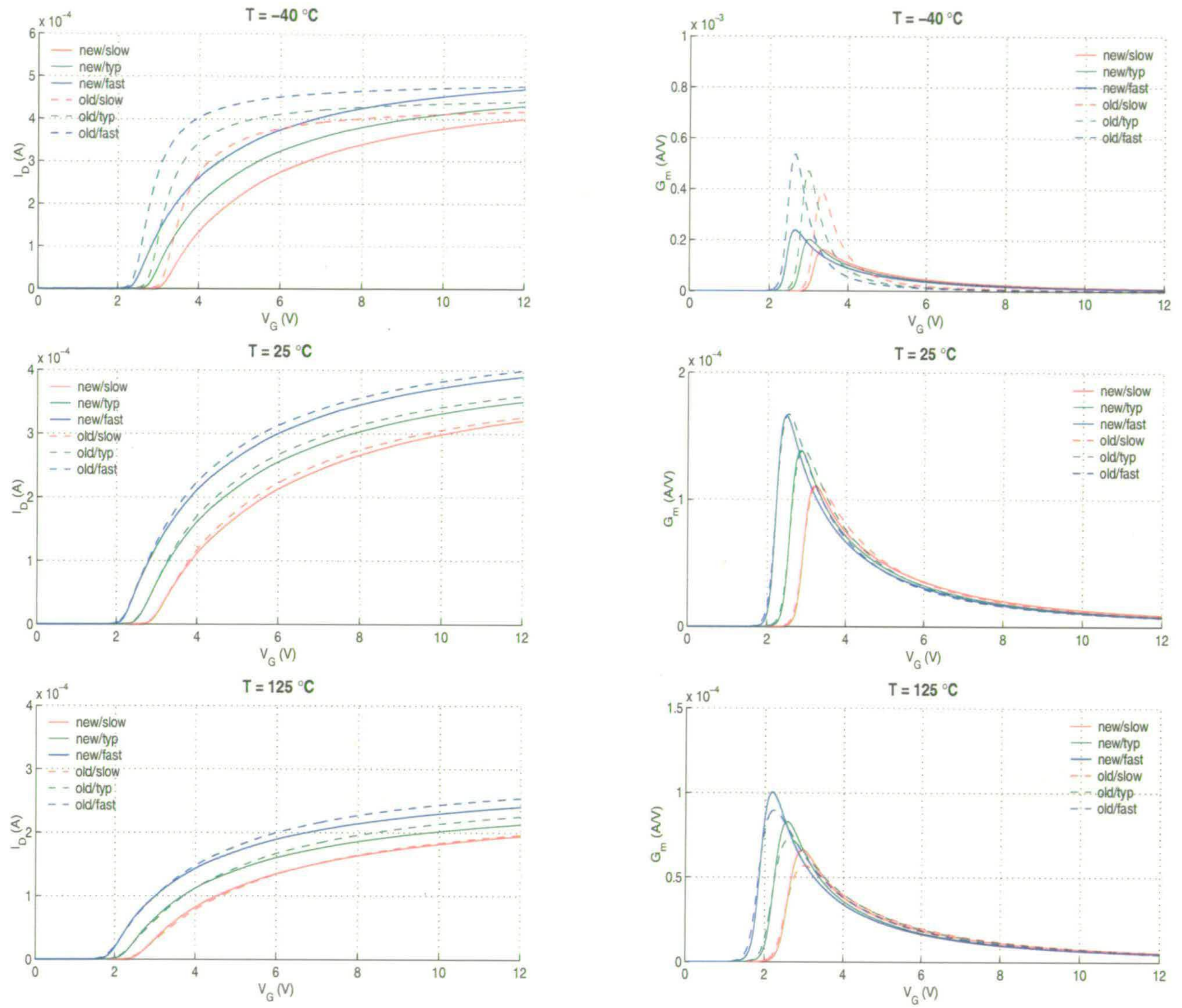


Figure 8.9 Ids-Vgs and Gm-Vgs at Vds=100mV at three different temperatures: old and FRERE_V1 model.

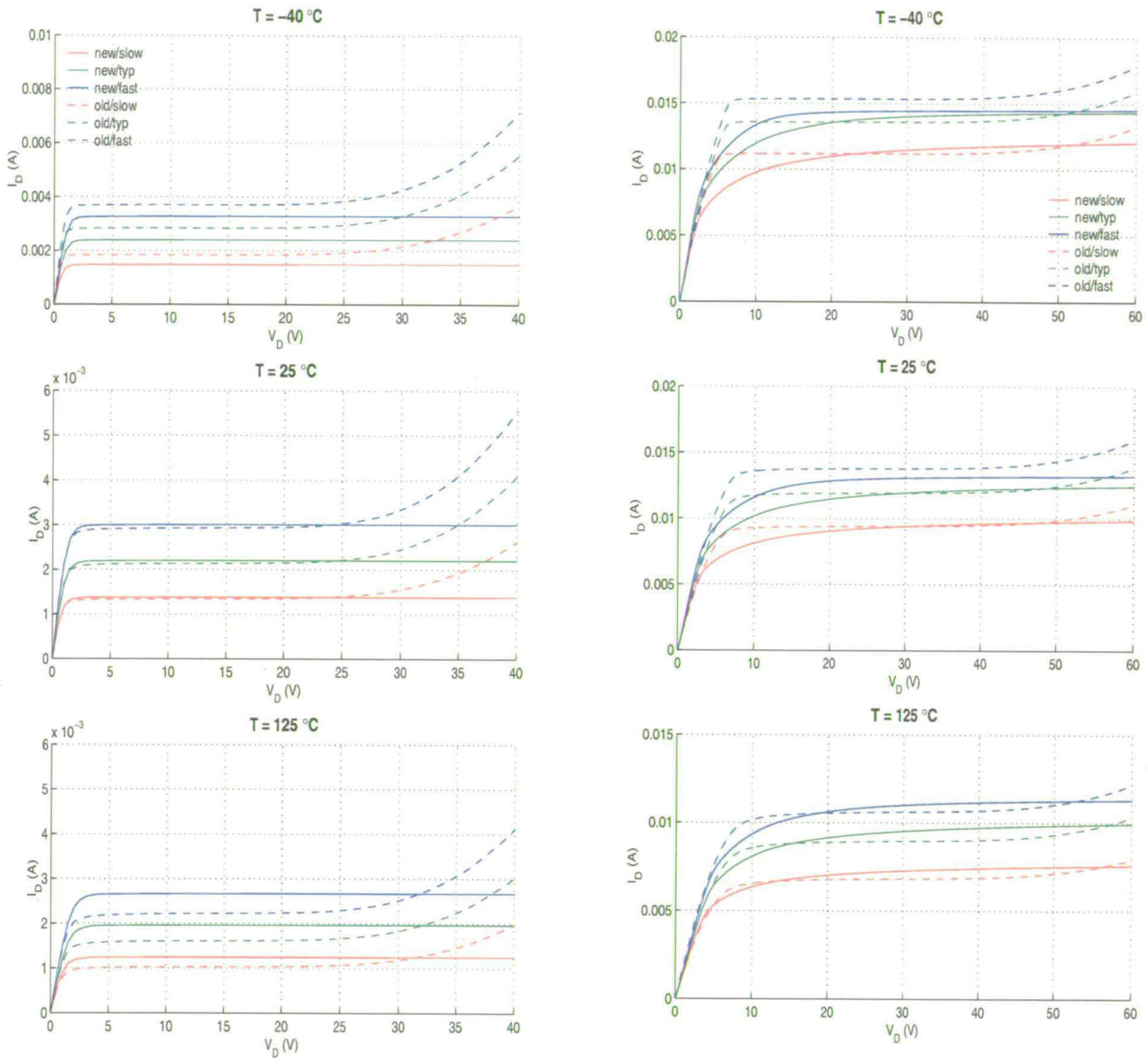


Figure 8.10 Ids-Vds at Vgs=5V (left) and at Vgs=12V (right) at different temperatures, old and FRERE_V1 model.

Figure 8.9 and Figure 8.10 show that the old model has an incorrect behaviour at low temperature which is not present for the FRERE_V1 model which performs well.

8.2.8 Circuit simulation tests with old and FRERE_V1 model

This section describes the circuit tests performed on the newly developed LDMOS model (FRERE_V1).

8.2.8.1 Description of circuit-simulations

As a first step, the circuits were simulated with the old model. These simulations will be used as a reference to compare the new model (for this test all n-type DMOS models are changed from old to FRERE_V1).
The circuits are then simulated with the FRERE_V1 models for all different MOS-corners so that all combinations of corner models and temperatures are simulated.
For each circuit a characteristic output was monitored to check for correct operation of the circuit. In addition the CPU time required for the simulation was monitored.

8.2.8.2 Results of BULB circuit simulation

This circuit is sensitive to convergence errors, as there were already convergence issues reported with the old version of the models. However, no problems were observed with the FRERE_V1 models.

An overview of the output from the simulations is presented in the Table 8.3.

Temperature	Corner	tran steps	CPU tran time [s]	CPU tran time [h / m]	time/step [s / step]
T=27°C	old model / typ	26302	4.70×10^3	1h18m	0.179
T=-45°C	ntyp_ptyp	9718	1.64×10^3	0h28m	0.169
	Nfast_pfast	9613	1.32×10^3	0h22m	0.137
	Nslow_pslow	11884	1.82×10^3	0h32m	0.153
	Nfast_pslow	9610	1.25×10^3	0h21m	0.130
	nslow_pfast	11781	1.88×10^3	0h32m	0.160
T=27°C	ntyp_ptyp	82951	5.82×10^3	1h37m	0.070
	nfast_pfast	77061	5.31×10^3	1h29m	0.069
	nslow_pslow	75242	6.04×10^3	1h42m	0.080
	nfast_pslow	77088	7.04×10^3	1h58m	0.091
	nslow_pfast	91564	6.26×10^3	1h45	0.068
T=125°C	ntyp_ptyp	135061	9.47×10^3	2h38m	0.070
	nfast_pfast	136042	9.29×10^3	2h35m	0.068
	nslow_pslow	127732	1.12×10^3	3h8m	0.088
	nfast_pslow	131069	1.18×10^3	3h17m	0.090
	nslow_pfast	135220	1.18×10^3	3h16m	0.087

Table 8.3 Results of the BULB circuit.

One should note from these results that the number of transient steps largely depends on the circuit behaviour. There is a signal (BULBFB) turning on a block as seen in Figure 8.11, that is dependent on the different corners or temperaturer. When simulating at T=-40°C, the signal did not drop down sufficiently within the time simulated to turn on the block which explains the short simulation time (it is faster to simulate a constant voltage than an oscillating signal).

A second observation is that the time required per transient step is dependent on the server load when the simulations were performed. During the tests large differences in the simulation times were observed.

A third remark is that due to the fact that the corner models of the FRERE_V1 and the old model are different, a different behaviour of the circuit is expected and thus a different number of steps and CPU calculation time can be expected.

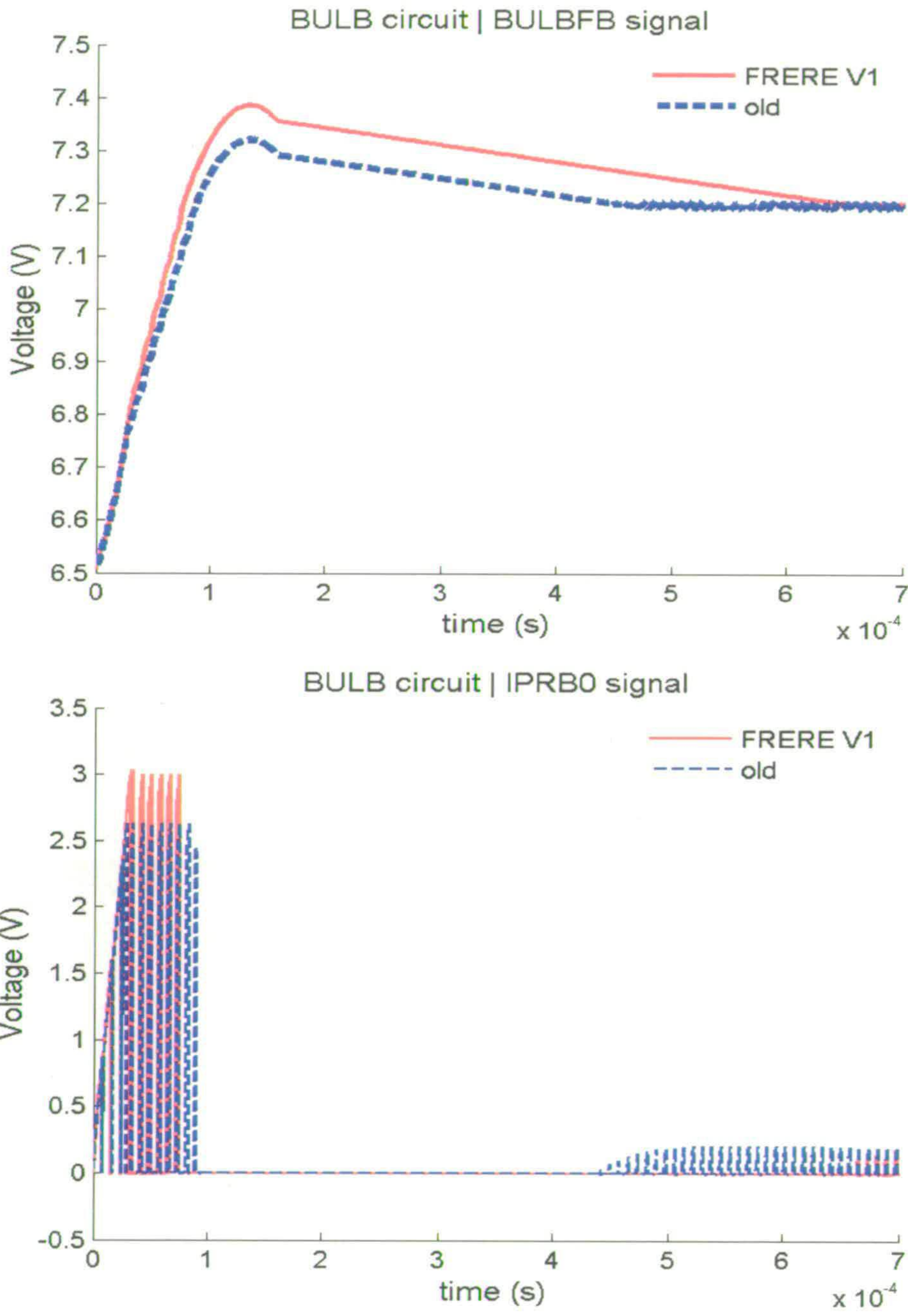


Figure 8.11 Simulation results with the old model and the FRERE_V1 model of the BULB circuit

As can be observed from Figure 8.11, the BULBFB signal simulated with the FRERE_V1 model kit rises to a slightly higher value, causing a delay of the startup of the second part of the simulation. However, the ripple on the BULBFB signal is the same, which is key to the successful operation of the circuit.

8.2.8.3 Results of the MOTOR-driver circuit

An overview of the output after simulation of the motor driver circuit is presented in Table 8.4

Temperature	Corner	tran steps	tran time [s]	tran time [h / m]	time/step [s / step]
T=27°C	old model	6112	1.33×10^3	0h22m	0.22
T=-45°C	ntyp_ptyp	2088	3.30×10^3	0h55m	1.58
	nfast_pfast	2249	3.64×10^3	1h0m	1.62
	nslow_pslow	1975	2.76×10^3	0h46m	1.40
	nfast_pslow	1940	2.66×10^3	0h44m	1.37
	nslow_pfast	2105	2.95×10^3	0h49m	1.40
T=27°C	ntyp_ptyp	1821	6.60×10^3	1h50m	3.62
	nfast_pfast	2141	9.16×10^3	2h32m	4.28
	nslow_pslow	1814	2.26×10^3	0h37m	1.25
	nfast_pslow	1822	7.20×10^3	2h0m	3.95
	nslow_pfast	1884	7.33×10^3	2h2m	3.89
T=125°C	ntyp_ptyp	1767	7.29×10^3	2h1m	4.13
	nfast_pfast	1739	4.03×10^3	1h7m	2.32
	nslow_pslow	1755	1.80×10^3	5h0m	10.27
	nfast_pslow	1648	4.21×10^3	1h10m	2.55
	nslow_pfast	1791	8.15×10^3	2h15m	4.55

resimulation

T=27°C	nslow_pslow	1835	2.45×10^3	0h40m	1.34
T=27°C	nslow_pslow	1827	3.59×10^3	0h59m	1.96
T=125°C	nslow_pslow	1713	5.21×10^3	1h26m	3.04

Table 8.4 Results of the motor driver.

A similar observation can be made related to the simulations of the BULB circuit with the time to simulate the circuit which varies from 37 minutes to 5 hours. Again, this was largely dependent on the load of the server. When re-simulating the slowest

simulation only 1hr 26min was required, which is about 3 times faster than the initial simulation.

In addition, for all corners the number of transient steps has been reduced by a factor of three. This means that the simulation needs less iterations to find a solution with the FRERE_V1 model. However, the time needed per step seems to be larger, which is probably caused by the Verilog-A module. However, if this module was converted to a standard component (i.e. converted to C-like code for hard coding into the simulator) the simulation time would be reduced.

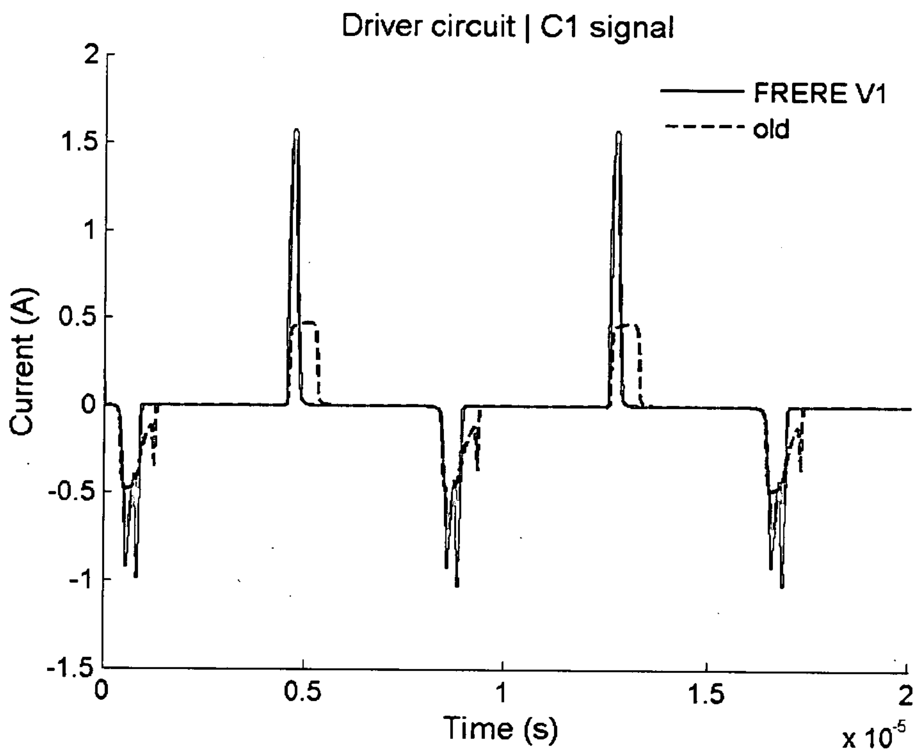


Figure 8.12 Circuit simulations results of the motor driver with the old and FRERE_V1 model

Comparing the old and FRERE_V1 models in Figure 8.12, it can be seen that the global behaviour is similar. Thus the circuit is working well with the FRERE_V1 models. However, one can observe that the shape of the peaks is different, which is caused by the different capacitance behaviour of the FRERE_V1 models.

8.2.8.4 Conclusion of the circuit simulation tests :

Both circuits were simulated and compared with the simulation results of the old models and it can be concluded that the FRERE_V1 models results in similar circuit behaviour.

The circuits were simulated for all different MOS corners in combination with 3 temperatures (-45°C, 27°C and 125°C) and no problems were observed.
The time needed to simulate was analysed, and it is clear that the total time needed to simulate a circuit is largely dependent on the load of the server on which one performs the simulation. There can be a factor of 3-4 difference depending on the load.
For the motor circuit, one can clearly see that less steps are required to simulate the circuit. For the BULB circuit, this is harder to analyse, as the circuit behaviour is altered by changing to the FRERE_V1 models and thus modifies the number of steps needed. With the FRERE_V1 model, more time is needed to simulate each step.

8.2.9 Model verification conclusions

The FRERE_V1 model has been thoroughly verified for

- Different width variations.
- A large temperature span -40°C to 125°C).
- Different operating regimes (for both individual devices and complete circuits).

For all these verifications, the model has proven to be stable and accurate.
As mentioned at the start of this chapter, the FRERE_V1 model was implemented in all AMIS technologies after the initial test proved successful. This implementation was done during 2002 - 2003. Since then a new product has been designed and simulated from the start with the FRERE_V1 model using the I3T technology. The design was first-time right and is now in production. While it cannot be concluded that this is entirely due to the FRERE_V1 model, feedback from the design department that their simulations and measurements on silicon were very close, indicated that the FRERE_V1 model has improved the design efficiency.

8.3 Methodology to include static-aging

8.3.1 Measurement data and procedure for aging analyses.

Aging tests were performed on a 40μm wide FND40B LDMOS device from the I2T100 technology. The stressing voltages were 6V on the gate and 40V on the drain. At regular intervals during the stressing experiment, electrical parameters were monitored. The experiment was conducted for 100,000 seconds at room temperature and this data set formed the basis for the procedure detailed below.

Once the measurements are available, the extraction procedure for the aged-model cards proceeds as follows: (similar to the methodology for worst-case corner extraction)

1. Check that the fresh data is not significantly different from the typical model.
2. Sample the model-parameter domain by choosing 5 points around the typical value for each of the model parameters selected for variation. In this case these were VTH0, U0, VSAT, (TOX[1]), R1.R, yielding 3125 points in total. VTH0 is the zero-bias threshold-voltage parameter from the BSIM3V3.2 model for the channel; U0 is the low-field mobility parameter for the channel; VSAT is the velocity saturation parameter of the channel; TOX the gate-oxide thickness; R1.R is a series resistance parameter for the drift region.
3. Run simulations for all 3125 points in the model-parameter domain, extracting the electrical parameters monitored during the stressing experiment. In the present case, the monitoring parameters were : IDSAT, RON, VTH, GMMAX. These simulations take roughly one day.

[1] TOX is only included in the list of model parameters to vary in order to line-up the procedures for the building of corners and aging models, so that only one neural network training exercise must be performed. In all subsequent computations the value of TOX is kept constant at its nominal value.

4. Collect the simulation results as pairs of model and electrical parameters vectors. Feed them as a training data-set to a neural-network, with the electrical-parameters vectors as inputs and the model-parameters vectors as output. The computation time for the neural network training process typically takes a couple of minutes.
5. Verify that the training process achieved the required accuracy.
6. Feed the measured electrical monitoring parameters to the neural network (including the fresh data) in order to obtain shifted model parameters.

The results of this extraction procedure are shown in the Figure 8.13 to Figure 8.16. For all electrical parameters the agreement between the measured and the simulated data is quite good. One can observe that under the applied stressing conditions, the IDSAT and the VTH are quasi-constant, whilst the RON and the GMMAX show a clear trend.

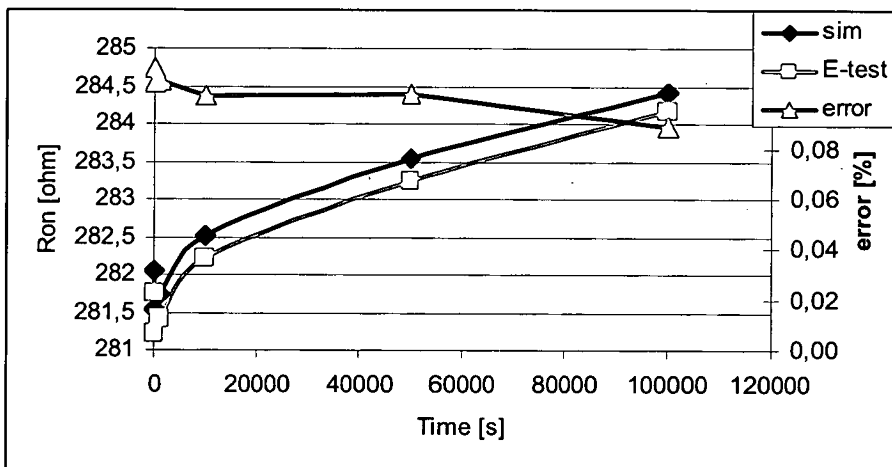


Figure 8.13 : Comparison of the modelled and measured RON

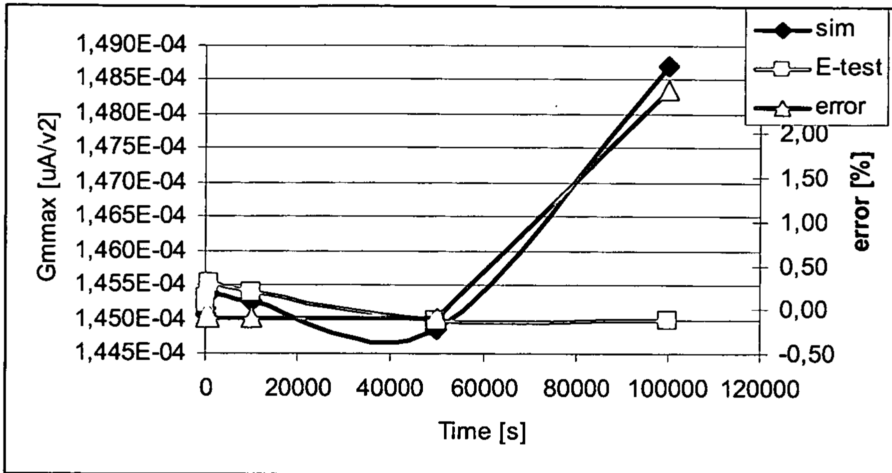


Figure 8.14 : Comparison of the modelled and measured GMMAX

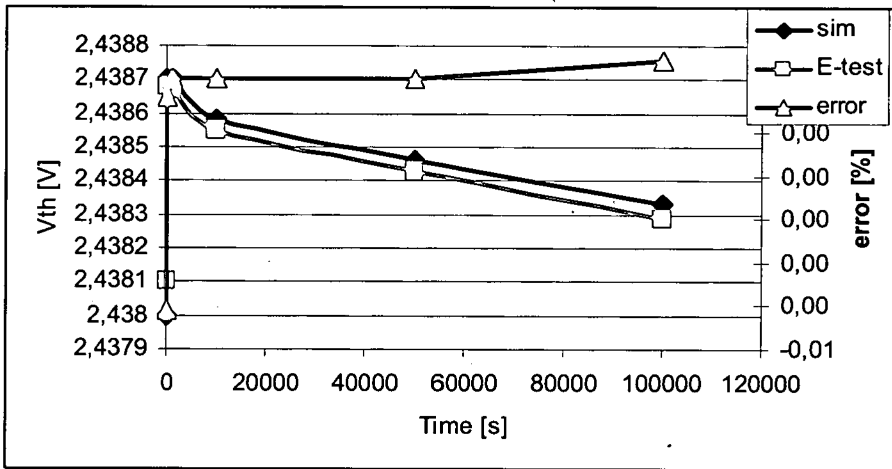


Figure 8.15 : Comparison of the modelled and measured VTH

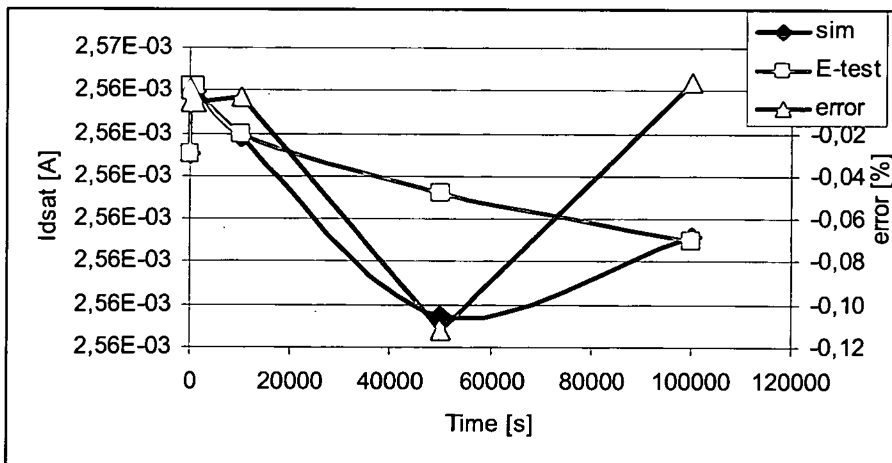


Figure 8.16 : Comparison of the modelled and measured IDSAT

8.3.2 Static Prediction of DMOS Aging Performance

Prediction of component life-times today is based on empirical formulas which allow the estimation of electrical parameter shifts measured under hot-carrier stress. The most advanced of these formulas have the following overall structure:

$$\frac{\Delta P}{P} = \frac{A.t^n}{1 + B.t^n} \tag{8.1}$$

In equation (8.1), the coefficients A and B depend on the applied stressing conditions. The parameter t is the duration of the given stress and ΔP is the relative shift in the target electrical parameter. This equation has been reported to fit the evolution of parameters such as IDSAT, RON, GMMAX and VTH as a function of stress-time. The purpose of this work is to show that this formula can also be applied to fit the evolution of aged model parameters, so that aging data can be interpolated and extrapolated to stress times other than the one used in the experiments.

Figure 8.17 to Figure 8.20 show log-log plots for all aged model parameters. These enable an easy extraction of the coefficients and powers present in equation (8.1). In Figure 8.17, a clear trend is observed for the R1.R model parameter, where no saturation effect takes place within the time-span of the stressing experiment. This data allows the extraction of values for the A and the n coefficients from (8.1). In the absence of saturation, the B coefficient is set to zero.

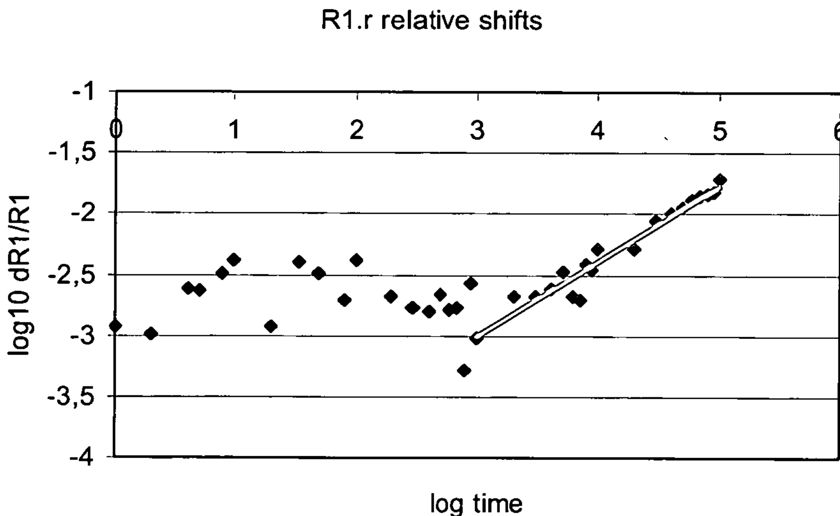


Figure 8.17 : Logarithmic plot of the relative shifts of R1.r with time

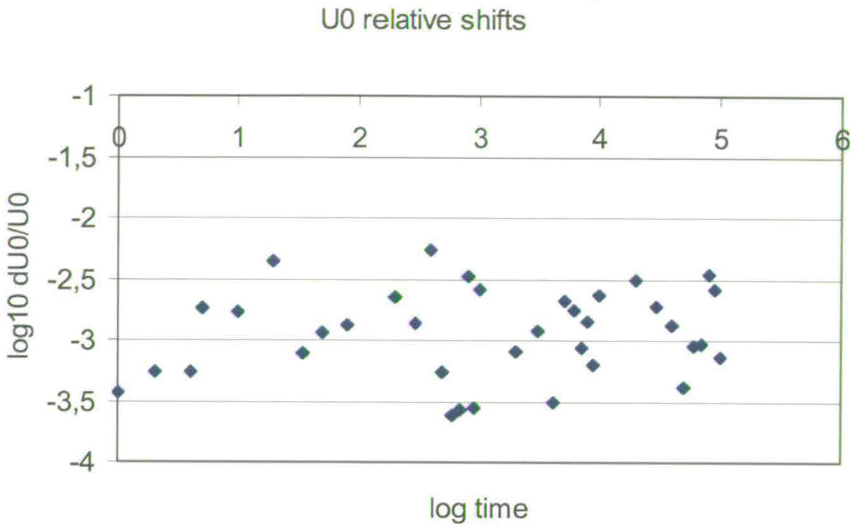


Figure 8.18 : Logarithmic plot of the relative shifts of U0 with time

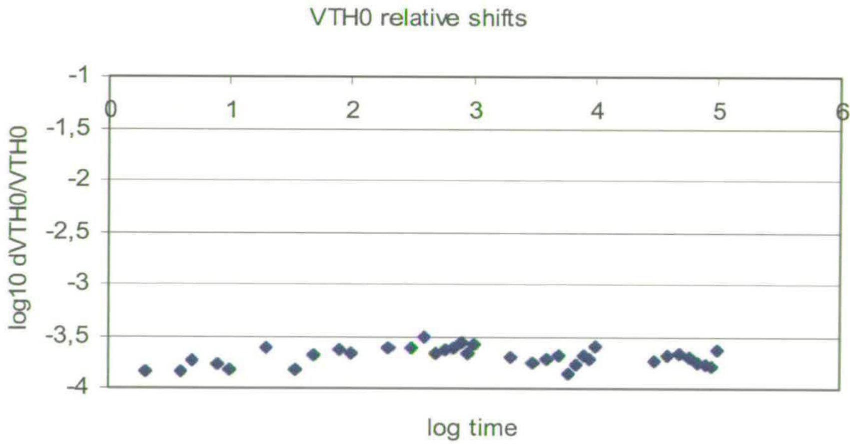


Figure 8.19 : Logarithmic plot of the relative shifts of VTH0 with time

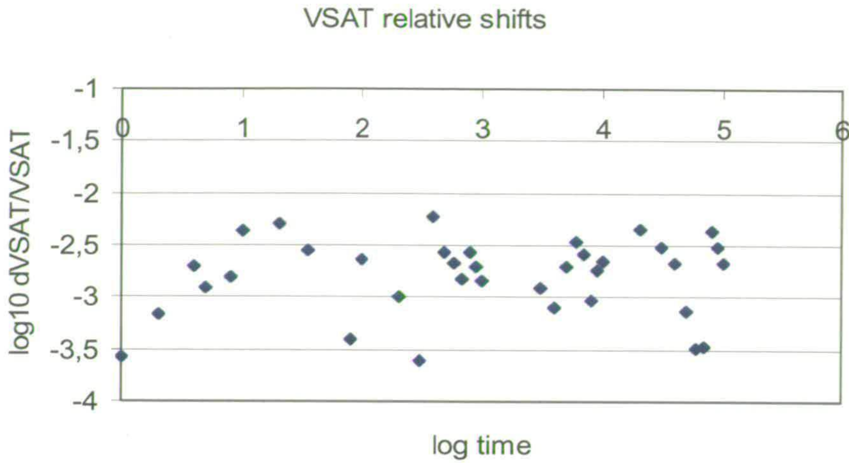


Figure 8.20 : Logarithmic plot of the relative shifts of VSAT with time

For all the other model parameters, no clear trend can be seen with the scatter of the data-points related to measurement resolution and noise. This allows the conclusion that the stressing conditions applied during the experiment do not result in any shift of the VTH0, U0 and VSAT model parameters. Extending the reasoning even further, one sees only parameters from the drift-region are affected, pointing towards the injection of hot holes at the drain-side as the underlying mechanism.

The present test-case clearly shows the power of the procedure that has been validated. Indeed, the usage of the neural network and the local inverse mapping allow the user to make an unequivocal diagnostic which is ensured by the nature of the mapping that is built.

8.4 Methodology to include self-heating

To be able to include self-heating in a DMOS macro-model, one can distinguish 2 steps:

- Correct measurement of self-heating free device characteristics.
- Implement action of a valid model to include self-heating.

8.4.1 Self-heating free measurements

As an initial step, the test-setup described in [1] was developed and measurements performed. This paper [1] describes a method to measure LDMOS output characteristics which is free of self-heating and how to extract thermal resistance and capacitance by which an equivalent RC-network can be generated.

The results of these measurement were compared to with the generic heating formulas described in [2] and the results can be seen in Figure 8.21

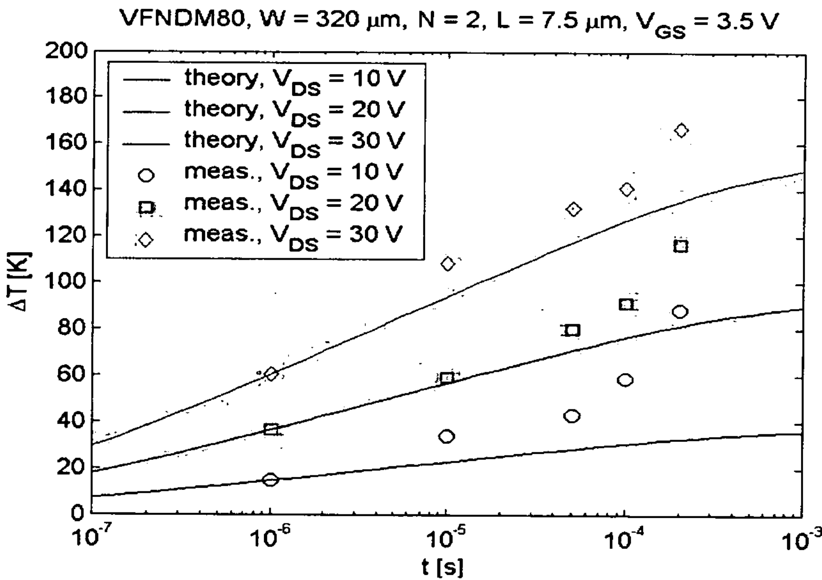


Figure 8.21: Comparison of measurements to the simulated values based on the Rinaldi equation

As can be observed, there is not a good match. Measurements and theory were matched for pulses of 1 μs. This explains the perfect fit for 1 μs.

When the initial self-heating is taken into account by using the Rinaldi formula [2], one can see that a good match is obtained between measurements and simulations as can shown in Figure 8.22.

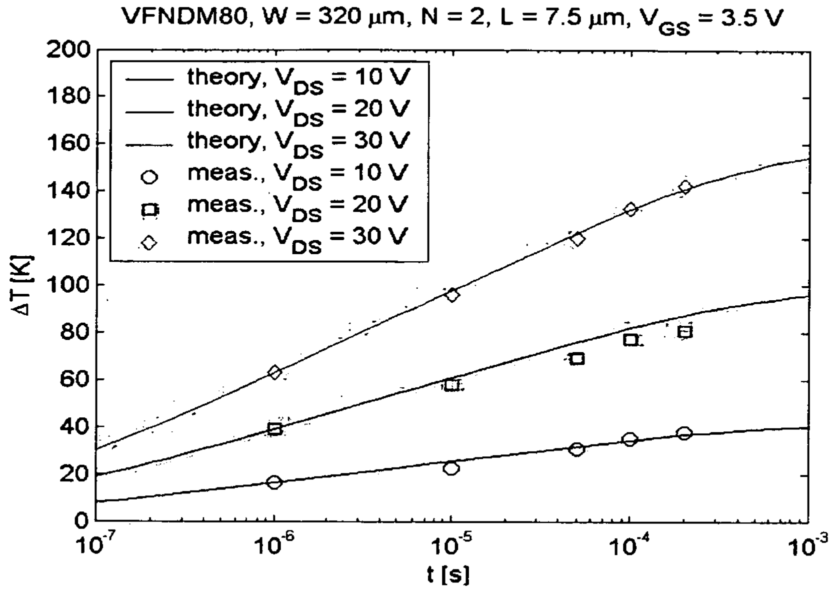


Figure 8.22: Comparison of corrected measurements to the simulated values based on the Rinaldi equation

Another method to characterise a device without self-heating is to use TLP measurements. This type of setup is able to generate accurate pulses of 100ns and at this pulsewidth almost no self-heating is present.

The drawback of this setup is that it cannot be used to measure "small" currents (less than 100mA) and it can only generate a single pulse width, thus it is not possible to extract an thermal capacitance by this method.

Proposal for implementing self-heating in the model.

The proposed schematic is shown in Figure 8.23.

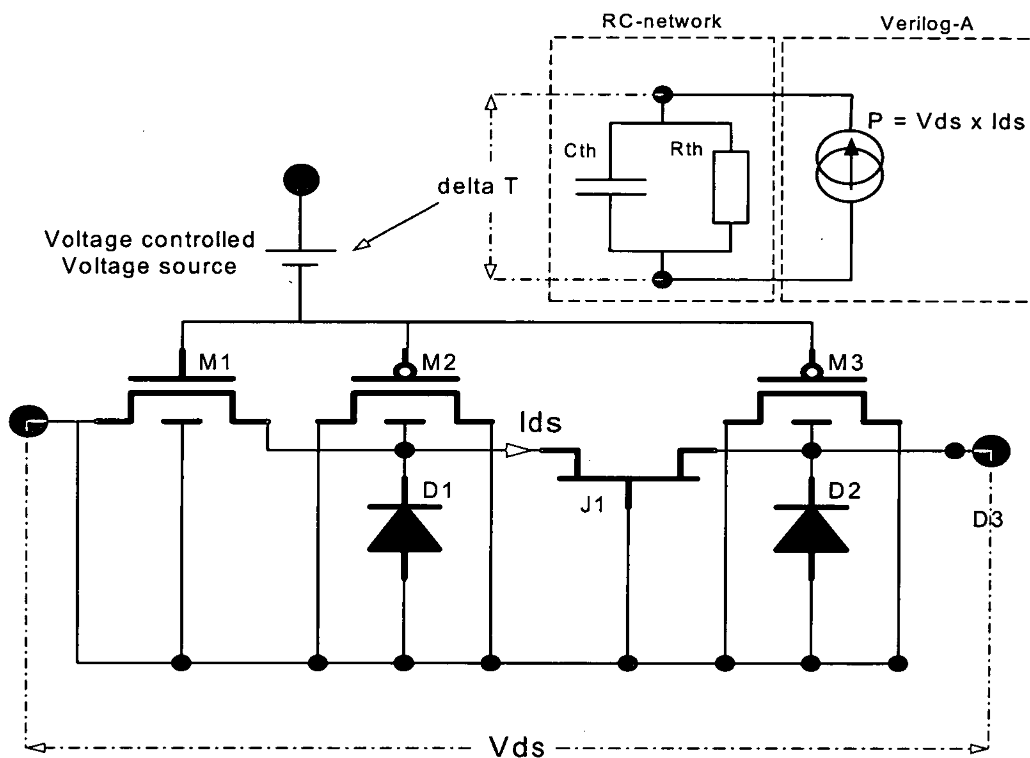


Figure 8.23: Proposed implementation of Self-heating into the macro-model

Inside the Verilog block an RC network is implemented. The Verilog-A block calculates the power produced by the device ($P = V_{DS} \times I_{DS}$). The power is fed to the RC network, and the voltage across the RC network gives the temperature rise of the device. This temperature rise has to be translated to the model.

At the moment it is thought that by implementing a delta V_{TH} and a change in the mobility of the drift region (JFET module), it should be possible to implement self-heating into the model.

8.5 Conclusion

The model developed in this work has been verified for robustness, scalability and accuracy and methodologies have been proposed to include static aging and self-heating.

The proposed model has increased the accuracy and scalability compared to existing models. The FRERE_V1 improved model has been thoroughly tested in a production environment as the model was introduced in the AMIS I3Tx-family design-kit from 2002. An increase in simulation time was observed but this issue can be improved by replacing the Verilog-A module with a hard-coded simulator element.

Further improvements that can be made to the model are:

- Include impact ionisation
- Include self-heating
- Include dynamic aging
- Replace Verilog-A blocks by hard-coded simulator elements
- Replace the shorted MOS transistor by the new capacitor models to obtain higher accuracy at AC-behaviour.

References

[1] C. Anghel, A. M. Ionescu, N. Hefyene and R. Gillon, "Self-Heating characterization and extraction method for thermal resistance and capacitance in high voltage MOSFETs," in Proceedings of the 33rd European Solid-State Device Research Conference ESSDERC, Sep. 2003, pp. 449-452.

[2] N. Rinaldi, "Generalised image method with application to the thermal modelling of power devices and circuits," IEEE Transactions on Electron Devices, vol. 49, no. 4, Apr. 2002, pp. 679-686.

Conclusion and future work

9 Conclusion and future work **151**

9.1 Challenges and opportunities **151**

9.2 Conclusions **152**

9.2.1 LDMOS transistors 152

9.2.2 Modelling basics 152

9.2.3 LDMOS macro-model characteristics and macro-model requirements 153

9.2.4 TCAD simulations of LDMOS transistors 153

9.2.5 Developed test-chips for DC and AC analyses 153

9.2.6 The macro-model: definition / extraction procedure / worst-case corner models 153

9.2.7 The macro-model: verification / static aging / self-heating 153

9.3 Future work **154**

9.3.1 Impact ionisation 154

9.3.2 Replacement of Verilog-A block to a hard coded module 154

9.3.3 Replacement of shorted MOS – transistors by custom coded capacitors 155

9.3.4 Self-heating 155

9.3.5 Dynamic aging 155

9.4 Final conclusion **156**

9 Conclusion and future work

This thesis has presented the results of developing a model that represents the complex behaviour of LDMOS transistors. This chapter begins by describing what the initial challenges were, the direction taken to solve them and then finally determines whether these solutions could have applications in other domains. The second part briefly summarises and discusses the important conclusions made in each of the preceding chapters. It then goes on to describe some areas for future investigations that have been suggested by this work.

9.1 Challenges and opportunities

At the start of this work, DMOS transistors and complex logic were more frequently being used together and integrated on a single chip. DMOS drivers generally occupy quite a large area of the die and due to the fact that the models available were not very accurate, a reasonable design margin was needed, which resulted in a larger die size. If a more accurate model could be made available, it would then be possible to reduce this size, thus lowering the cost of the product.

The accuracy improvement was mainly required for the modelling of the DMOS specific AC behaviour as this was not covered by the CMOS models used for modelling DMOS transistors. The first challenge was to fully understand the physical behaviour of a DMOS device in both DC and AC operation which was undertaken using TCAD simulations and specially developed test-structures. Once the behaviour was fully understood, the building of a new model could begin.

As the model was to be used in the design system of AMIS, a SPICE type model implemented in a commercial simulator was needed, which restricts the number of options to build up the model. Or the standard available component models of the simulator could be used or a component model using the Verilog-A language standard could be developed. The model that has been developed is a combination of both. A variety of DMOS device types are available to the designer such as n and p-type devices, devices with different breakdown voltages and on resistances. Hence, a model is needed that is flexible enough to cover all these device types. In addition to the different device types the model should also be scalable over geometry as the width of a DMOS transistor can vary from a few microns to several millimetres.

It is desirable that the model should not only fit a single device, but also give the designer information on the process variation, and so a methodology to create corner models is needed. When silicon chips are produced, a systematic monitoring of the key parameters of devices is performed to guarantee that the chip is processed within the predefined limits. This monitoring provides a large statistical database from which the process variation can be extracted. The goal for this work was to determine a direct way to couple the process variation information to the model parameters and thus generate corner models. This link is made by teaching a neural network the relationship between the process parameters and the model parameters.

The next challenge is to provide a designer with information of how the DMOS transistor will behave over time, as due to its operation the device will have aged. This means that certain parameters of the device, such as the threshold voltage, will change as a function of operation time. Aging is monitored by stressing the device and evaluating how its key parameters evolve with time. As these key parameters are the same as the parameters monitored for process variations, the link to the model is available through the neural network. This showed that the neural network technique can not only provide corner models but also aged models.

9.2 Conclusions

9.2.1 LDMOS transistors

Different aspects of the DMOS transistor have been presented. An introduction to the various trade-offs that can be made when developing a DMOS transistor have been discussed. It has been shown that different classes of DMOS transistors exist, depending on how the channel is defined. These devices have been used throughout this thesis to characterise the macro-model that was developed. Finally, two circuits have been selected (the bulb circuit and the H-bridge) to validate the model and check the model accuracy and robustness.

9.2.2 Modelling basics

Some basic definitions were presented in this chapter and illustrated by a simple diode model. An overview of the different types of models and how they are implemented was shown in the second part of the chapter to provide the background required for the LDMOS model.

9.2.3 LDMOS macro-model characteristics and macro-model requirements

This chapter presented an overview of the characteristics of LDMOS transistors and its associated ranges and values. The specifications that a good LDMOS model should meet to verify its performance, were also presented.

9.2.4 TCAD simulations of LDMOS transistors

By performing TCAD simulations, a better insight in the "internal" device behaviour has been obtained. The main achievement from these TCAD simulations is a good understanding of the capacitance behaviour of an LDMOS under typical bias conditions. This information has proved to be helpful when developing the AC-model.
Another interesting analysis was the analysis of the internal drain behaviour V_K. This has provided information on the behaviour of the drift region. A good LDMOS macro-model should mimic this behaviour to ensure that all its components operate at physical bias conditions.

9.2.5 Test-chips developed for DC and AC analyses

A complete set of test-structures have been designed and measured to analyse DMOS transistors and extract their model-parameters. A novel MESDRIFT test-structure has been developed and was found useful for various domains of the DMOS characterisation (V_K behaviour, self-heating, hot-carrier)

9.2.6 The macro-model: definition, extraction procedure and worst-case corner models

This chapter presented the macro model topology. The different components to build up the model were discussed together with a modification to model the AC-behaviour. An extraction procedure covering all aspects of the model has also been presented. In addition to a good basic model, it is important that process variations can be accounted for by the model and a novel technique has been described.

9.2.7 The macro-model: verification / static aging / self-heating

The above model has been verified for robustness, scalability and accuracy and methodologies proposed to include static aging and self-heating.

The proposed model has proven to increase the accuracy and scalability compared to existing models. The new improved model has been thoroughly tested in a production environment as the model was introduced in the AMIS I3Tx-family (I3T is the 0.35μm high voltage process at AMIS) design-kit from 2002. A small increase in simulation time was observed but this issue can be improved by replacing the Verilog-A module with a hard-coded simulator element.

9.3 Future work

Further improvements to the model would include

- Include impact ionisation
- Replace Verilog-A blocks by hard-coded simulator elements
- Include self-heating
- Include dynamic aging

These topics will be discussed in the following paragraphs:

9.3.1 Impact ionisation

Impact ionisation has not yet been included in the model. The impact ionisation model available in BSIM3V3.2 cannot be used as the MOS transistor modelling the channel has only the V_K voltage at its drain and not the full drain voltage. To include this impact ionisation, a dedicated feature should be added to the Verilog-A module. Impact ionisation occurs in a bias region that is not used or should not be used by designers. Safe Operating Area (SOA) checks are implemented to warn designers that the device operates in a non-allowed region.

9.3.2 Replacement of Verilog-A block to a hard coded module

As some adaptations were needed to a standard JFET model, the easiest and most general way of implementation was to use VERILOG-A. However, if one wants to improve the speed of the simulation, hard-coding the custom equations into the simulator will help. The drawback of hard-coding is that the model is no longer simulator independent. However, as more and more users discover the advantages of VERILOG-A, conversion algorithms form VERILOG-A to simulator specific code are expected to be included in commercially available simulators such as SPECTRE. This would significantly improve simulator speed and stability.

9.3.3 Replacement of shorted MOS transistors by custom coded capacitors

The replacement of the two shorted MOS transistors by custom coded capacitors, in a first stage in VERILOG-A, could improve the accuracy in the AC-behaviour of the model. First tests have shown this improvement but this topology should be fully tested for robustness and scalability.

9.3.4 Self-heating

As LDMOS devices are often used in power applications, prediction of the self-heating of the device is important. At the moment it is possible to measure a device without self-heating as a dedicated test-setup was developed. This should make it possible to implement self-heating prediction in the model and chapter 8 proposed how this could be implemented.

9.3.5 Dynamic aging

In chapter 8 a method for static aging prediction was presented. However, static aging is a worst case prediction as all devices are treated as if they would have operated for the same amount of time.

Dynamic aging tracks the operation of each single device and calculates the degradation. In such a way, it will be possible to accurately predict if a design will operate long enough to guarantee a certain life-time.

9.4 Final conclusion

A new physically based macro-model for LDMOS devices has been presented. Modelling the V_K for all bias conditions was a crucial step to achieve a good physical model. A test-structure to measure the V_K was developed to confirm the observations made by TCAD simulations.

The model has been verified at device and at circuit level for different criteria (accuracy, scalability, robustness, temperature range). It has been installed in the AMIS design system where it proved to be functional and has helped to deliver first-time right designs.

Appendix A: Adapted JFET VERILOG Code

```
`include "discipline.h"
`include "constants.h"

//
//
// Based on the OVI Verilog-A Language Reference Manual, version 1.0 1996
//
//

module n_jjfet(vdrain, vbulk, vsource, vprobe);
inout vdrain, vbulk, vsource;
inout vprobe;

electrical vdrain, vbulk, vsource, vprobe;

real parameter area=1 from (0:inf);
parameter real beta=0.1m from (0:inf);
parameter real lambda=0;
parameter real is=1e-16 from [0:inf);
parameter real gmin=1p from (0:inf);
parameter real mm=0.5 from (0:1);
parameter real fact1=0.0045 from (-10:inf);
parameter real fact2=-0.126 from (-10:inf);
parameter real fact3=1.2154 from (-10:inf);
parameter real fact4=1 from (-10:inf);
parameter real fact5=1 from (-10:inf);
parameter real fact6=1 from (-10:inf);
parameter real tnom=300 from (200:500);
parameter real vttc=0 from (-20:20);
parameter real betatc=0 from (-20:20);
parameter real (* integer inherited_mfactor; *) m=1;
parameter real Vref=0.1;

   real Vgs, Vgd, Vds, Vps, Vgst, Vgdt;
   real Id;
   real vtt;
   real help;
   real VK;
   real ax, ay, bx, by, cx, cy, betaa, temp;

   analog function real smooth_exp_square;
      input vv;
      real vv;
      smooth_exp_square=pow(ln(1+exp(vv)),2);
   endfunction

   analog begin

      @ ( initial_step or initial_step("static") ) begin

       temp = $temperature;
```

```
        betaa = (beta * area)*pow((1.01),(betatc*(temp-tnom)));
        ax = fact1;
        ay = fact2;
        bx = fact3;
        by = fact4;
        cx = fact5;
        cy = fact6;
        Vgs = V(vbulk, vsource);
        Vgd = V(vbulk, vdrain);
        Vds = V(vdrain, vsource);
        Vps = V(vprobe, vbulk);

      end

      temp = $temperature;
      betaa = (beta * area)*pow((1.01),(betatc*(temp-tnom)));
      ax = fact1;
      ay = fact2;
      bx = fact3;
      by = fact4;
      cx = fact5;
      cy = fact6;
      Vgs = V(vbulk, vsource);
      Vgd = V(vbulk, vdrain);
      Vds = V(vdrain, vsource);
      Vps = V(vprobe, vbulk);

help = ay + ( by - ay ) / 2 * ( tanh(( 2 * Vps - ax - bx )/( bx - ax )) + 1.0 )
+ ( cy - by ) / 2 * ( tanh(( 2 * Vps - bx - cx )/( cx - bx )) + 1.0 );

      vtt = ((help)*-1)+vttc*(temp-tnom);

      Vgst = Vgs - vtt;
      Vgdt = Vgd - vtt;

 Id = betaa * ( smooth_exp_square(Vgst/Vref) - smooth_exp_square(Vgdt/Vref) )
                * pow( Vref, 2 ) * ( 1 + lambda * abs(Vds) );


      I(vdrain, vsource) <+ Id*m + gmin*Vds;

   end
endmodule
```

Equations used in the VERILOG-A block:

$$I_{DS} = I_D.m + g\min.V_{DS}$$

Where

$$I_D = beta \times \left(\left(\ln\left(1 + e^{Vgst/Vref}\right)\right)^2 - \left(\ln\left(1 + e^{Vgdt/Vref}\right)\right)^2 \right) \times \left(V_{ref}\right)^2 \times \left(1 + lambda \times abs\left(V_{DS}\right)\right)$$

With

$$V_{gst} = V_{GS} - V_{TT}$$

$$V_{gdt} = V_{GD} - V_{TT}$$

$$V_{TT} = -\left(ay + \left(\frac{by - ay}{2}\right) \times \left(\frac{\tanh(2 \times V_{PS} - ax - bx)}{bx - ax} + 1\right) + \left(\frac{cy - by}{2}\right) \times \left(\frac{\tanh(2 \times V_{PS} - bx - cx)}{cx - bx} + 1\right)\right)$$

V_{GS} = Voltage between jfet-gate and jfet-source

V_{GD} = Voltage between jfet-gate and jfet-drain

V_{DS} = Voltage between jfet-drain and jfet-source

V_{PS} = Voltage between dmos-gate and dmos-source

I_{DS} = current flowing through jfet drain and source

Appendix B: Publications

LDMOS Capacitance Analysis versus Gate and Drain Biases, Based on Comparison between TCAD Simulations and Measurements

Essderc 2001 ....B3-B6

A neural-network-based local inverse mapping technique for building statistical DMOS models

Essderc 2003 ....B7-B10

An improved LDMOS transistor model that accurately predicts capacitance for all bias conditions

ICMTS 2005 ....B11-B15

An experimental approach for bias-dependent drain series resistances evaluation in asymmetric HV MOSFETs

Essderc 2001 ....B16-B19

Investigations and physical modeling of saturation effects in lateral DMOS transistor architectures based on the concept of intrinsic drain voltage

Essderc 2001 ....B20-B23

Physical modelling strategy for (quasi-) saturation effects in lateral DMOS transistor based on the concept of intrinsic drain voltage

CAS 2001 ....B24-B27

Universal test structure and characterisation method for bias dependent series resistance of HV MOSFETs

Essderc 2002 ....B28-B31

EKV compact model extension for HV lateral DMOS transistors
ASDM 2002 .... B32-B35

Electrical Characterisation and modeling og high-voltage MOSFETS with MESDRIFT
Iedm 2002 .... B36-B38

Bias-dependent drift resistance modeling for accurate DC and AC simulation of asymmetric HV-MOSFET
Sispad 2002 .... B39-B40

LDMOS Capacitance Analysis versus Gate and Drain Biases, Based on Comparison between TCAD Simulations and Measurements.

S.F Frère[1,2], J. Rhayem[1], H.O Adawe [1], R. Gillon[1], M. Tack[1], A.J Walton[2]

[1]Alcatel Microelectronics, Westerring 15, Oudenaarde, Belgium

[2]Dept. of Electronics and Electrical Engineering, SMC, The University of Edinburgh, Edinburgh, Scotland, UK.

Steven.frere@mie.alcatel.be; joseph.rhayem@mie.alcatel.be

Abstract

The behaviour of the capacitances of LDMOS devices is analysed as a function of gate and drain bias, using TCAD simulations and S-parameter measurements. Both simulations and measurements revealed that instead of the smooth sigmoïd shape usually seen in MOST's, the capacitances of LDMOS devices show a distinct ridge at low Vds. Examination of simulations indicates that these phenomena are linked to the non-uniform doping of the channel and the complex interaction with the depletion zones in the drift region. This insight is used to propose an improved macro-model for the DMOS device.

1. Introduction

DMOS devices are more and more applied in dynamic applications such as switching in power systems and fine slope controlling in electrical motor drivers.

Existing DMOS models are not accurate enough and spice-models are especially weak when modelling AC performance. It is known that the intrinsic gate-drain and gate-source capacitance, which to a large extent determines the turn-on and turn-off characteristics of a switch, is not well modelled.

To investigate the capacitance behaviour, TCAD simulations and S-parameter measurements were performed.

2. Device description

A cross-section of the device under investigation is presented in Figure 1. The Alcatel Microelectronics I2T-flow is based on a 0.7um CMOS process-flow to which some extra masks and implants are added to provide high voltage features.

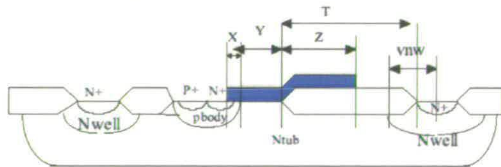


Figure 1 : LDMOS cross-section

The LDMOS is an asymmetric device, with the drift region on the drain-side located in a lightly doped N-tub. The

channel is self-aligned to the source and is created by the out-diffusion of the P-body under the gate. As a result the dopant distribution along the channel is non-uniform, decreasing towards the drain. The higher breakdown voltages are achieved by the depletion region that extends from the P-body into the drain leading to a voltage drop between the drain contact and the channel-region. The gate oxide and the polysilicon extend beyond the channel of the device.

This LDMOS device was measured and simulated for a number of bias conditions. The gate voltage was swept between –5 and 10V with the drain voltage stepped from 0 to 18V in steps of 2V.

S-parameters were measured on-wafer up to 5GHz using the 37369B Anritsu-Wiltron vector network analyser. A simple open-de-embedding procedure was used.

TCAD simulations were performed using Silvaco software with the process input deck being calibrated using SIMS and SRP profiles as well as SEM cross-sections. The device simulations were performed using the Lombardi model for the carrier mobility taking into account high-field velocity saturation effects.

3. Experimental results

Three TCAD experiments were performed: A device simulation on the complete LDMOS structure, a device simulation on the channel of the LDMOS without drift region and a device simulation on a extended drain MOS transistor which has an uniform doped channel.

3.1 Complete LDMOS structure

Figure 2 compares simulated and measured capacitance characteristics. A good agreement is observed between both, taking into account that on the measured device the body and the source are tied to ground, whilst in the TCAD, the body terminal is separated. The remarkable feature in this figure is the peak on the Cgd capacitance around the threshold as already indicated in [1].

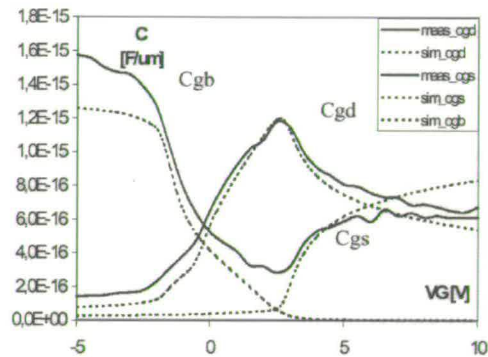


Figure 2: Measured and simulated LDMOS capacitances at Vds = 0V

Conventional MOST's do not show such a peak, as can be seen in figure 2 of reference [1]. Simulations (figure 3) and measurements of an extended drain MOS transistor, having a uniform doped channel, show capacitance characteristics similar to a conventional MOS.

This fact leads to question the validity of the statement in [1] that the peak is caused exclusively by the high resistance of the drift region.

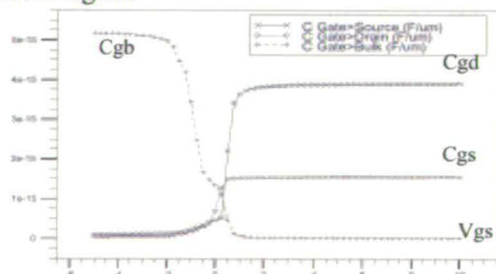


Figure 3 : Simulated extended drain MOS capacitances at Vds = 0V

3.2 LDMOS channel-only

To further demonstrate the influence of the non-uniform channel doping on the capacitance characteristics, a channel-only LDMOS device was simulated. The cross-section in figure 4(a) shows how the device was cut at the junction of the Pbody to Ntub and a new drain contact was made.

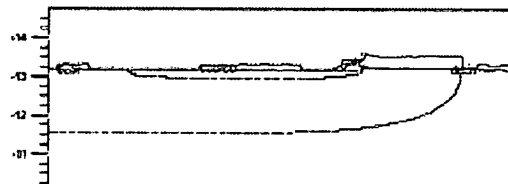


Figure 4(a) cross-section of "channel"-device

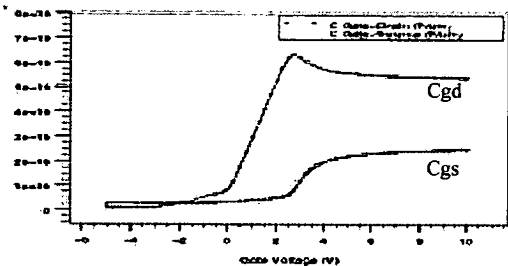


Figure 4(b) Cgs, Cgd simulations of the "channel"-device (Vds=0V)

The capacitance simulations still show the distinctive peak, although the resistance of the drain region is comparable of that of the source. This allows us to conclude that the peaking behaviour of Cgd is caused essentially by the non-uniform channel-doping and is reinforced by the interaction of the highly resistive drift region.

3.3 Cgs and Cgd at Vds = 0V

When sweeping Vgs, we see that a channel starts to form from the drain side, causing an increase of Cgd, before the onset of conduction. Then, when Vgs rises further, a channel finally forms at the source side which takes over the control of the charges at the drain causing the decrease of Cgd (fig.2) and the increase of Cgs.

3.4 Cgs and Cgd when Vds > 0V

Using TCAD simulations, the analysis of Cgd and Cgs was extended to non-zero drain biases.

At first the increase of the drain bias triggers a paradoxical increase of the Cgs capacitance.(fig.5(a)) This can be explained by a further transfer of charges controlled initially by the drain to the source charge, because of the extension of the depletion zones in the drift region.

At a given Vgs, the Cgs capacitance increases up to the point where the channel region starts to saturate. The Cgs surface shows a distinctive ridge that is tracking the saturation limit.

Beyond this point, a depletion zone appears underneath the bird's beak, repelling the current flow and the mobile charge carriers away from the oxide and squeezing them against the extension of the depletion zone from the N-tub to P-body junction. This results in a net decrease of the total gate-capacitance, that reflects in the decrease of both Cgs and Cgd. This tunnel-effect is depicted in figure 5(b) and figure 5(c).

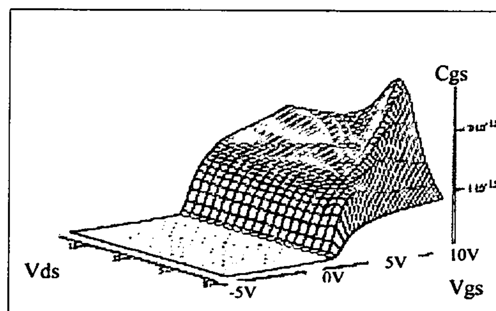


Figure 5(a) Simulations of Cgs as a function of Vgs and Vds

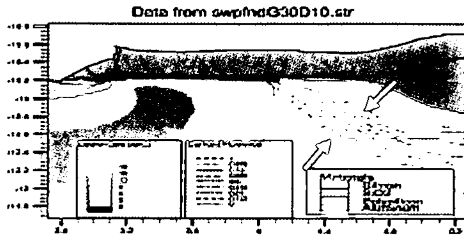


Figure 5(b) "Tunnel"-effect

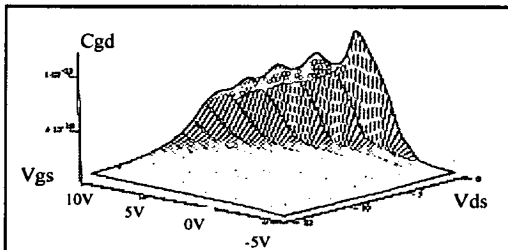


Figure 5(c) Simulations of Cgd as a function of Vgs and Vds

4. Sub-circuit model

The non-standard capacitance behaviour of the LDMOS device can not be rendered with the standard BSIM3v3 model. A dedicated subcircuit-model needs to be developed. Figure 6 shows the chosen topology.

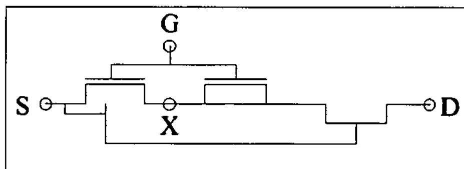


Figure 6 Sub-circuit model of LDMOS device

The subcircuit contains a standard BSIM3v3 model for the channel-region, a second MOS device with short-circuited source and drain to account for the peaking behaviour of Cgd and a JFET to model the pinch-off of the drift-region. The analysis shows that the second MOS transistor needs to have a lower threshold voltage than the channel device. This threshold voltage is fitted on the onset of the measured Cgd characteristics. On-going work is in the process of optimising both the parameter fits and the capacitance behaviour.

5. Conclusions

Good agreement has been obtained between TCAD simulations and measurements of LDMOS capacitances. As a result it has been possible to use TCAD simulations to identify the dominant regions related to the capacitance behaviour. Non-standard MOS capacitance behaviour was observed and an explanation is presented. This has resulted in the proposal of a new sub-circuit model, which is in the process of being optimised.

6. Acknowledgements

The authors would like to thank F.Valino and P.Moens for their help. This work is supported by the IST-1999-12257 Automacs project.

7. References

[1] E.C.Griffith, S.C.Kelly,J.A.Power, D.Bain, S.Whiston, P.Elebert, M.O'Neil, "Capacitance Modelling of LDMOS Transistors", IEEE Solid-State Device Research Conference, Sept 2000, pp 624-627.

[2] Olsson, J., Valtonen, R., Heinle, U., Vestling, L., Soderbarg, A., Norde, H., "A Capacitance-Voltage Measurement Method for DMOS Transistor Channel Length Extraction", *IEEE Int. Conference on Microelectronic Test Structures*, March. 1999, pp. 135-140.

A neural-network-based local inverse mapping technique for building statistical DMOS models

S.F. Frère[1,2]
B. Desoete[1]
J. Rhayem[1]

Steven_Frere@amis.com
[1]AMI Semiconductor,
Westerring 15, Oudenaarde,
Belgium

M. Anser[1]

[1]AMI Semiconductor,
2300 Buckskin Road,
Pocatello, Idaho, USA

A.J. Walton[2]

[2]School of Engineering &
Electronics, Scottish
Microelectronics Centre,
University of Edinburgh,
Scotland, UK.

Abstract

This paper presents a methodology to circumvent the time consuming standard approach for statistical model development. The methodology is a two step process. The first part defines the relationship between electrical device parameters and model device parameters by means of training a neural network. The second stage uses the neural network to create worst-case model parameter sets. In order to select an appropriate set of worst-case electrical parameters, a multivariate statistical analysis is performed, such that correlations between device parameters are taken into account. The neural network approach also enables a Monte-Carlo model to be generated. The advantages of the proposed methodology are its speed improvement and accuracy.

1 Introduction

A commonly used approach to create worst-case models is to use a Monte-Carlo analysis to build a large statistical database of accurate model parameter sets by the direct extraction of parameters on a large population of devices. This involves measuring the complete *IV* characteristics on all samples, extracting models using optimisation, studying the correlations between measured electrical device parameters and extracted model parameters, and the building of a regression model. Such an approach however results in the optimiser-based procedure skewing the distributions, adding variability and unexpected correlations [1]. In this paper we describe an alternative methodology where the optimiser-based extraction step is circumvented by building a local inverse of the mapping from the model parameters to the electrical parameters around the typical model [2]. Building this local inverse involves sampling the model parameter space and performing an analysis of the sensitivity of the simulated electrical parameters with respect to some key model parameters. The method used to build this inverse mapping around the typical parameter set involves training a neural network [3].

2 Device and technology description

A cross-section of the device under investigation is presented in Figure 1. The I2T-flow is based on a 0.7μm CMOS process to which some extra masks and implants have been added to provide the high-voltage features. From Figure 1 it can be observed that the LDMOS transistor is an asymmetric device, with the drift region on the drain-side located in a lightly doped N-tub.

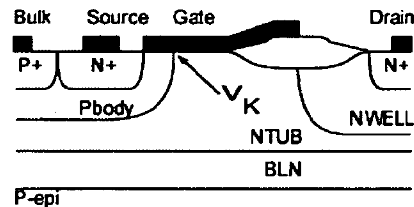


Figure 1: Section through an LDMOS.

The channel is self-aligned to the source and is created by the out-diffusion of the P-body under the gate. As a result the dopant distribution along the channel is non-uniform and decreases towards the drain end. Higher breakdown voltages are achieved due to the depletion region that extends from the P-body into the drain, which provides a voltage drop between the drain contact and the channel region. The gate oxide and the polysilicon extend beyond the channel of the device as illustrated in Figure 1.

A systematic monitoring is performed on the following key parameters (called E-test parameters) of the LDMOS transistor:

- Transconductance:

$$GM_{max} = \left(\frac{dI_D}{dV_{GS}}\right)_{max} \quad \text{at } V_{DS} = 100\text{mV}$$

- Extrapolated threshold voltage:

$$VTH = V_{GS}(GM_{max}) - \frac{I_D(GM_{max})}{GM_{max}} - \frac{V_{DS}}{2}$$

at $V_{DS} = 100$mV

- Saturation current:

$IDSAT = I_D$ at $V_{DS} = 25$V and $V_{GS} = 5$V

- On-resistance:

$RON = \frac{V_{DS}}{I_D}$ at $V_{DS} = 500$mV and $V_{GS} = 12$V.

The observation of these characteristics is a standard procedure used to monitor the stability of the production process. As a consequence a large database is generated providing statistically relevant information for every processed device.

3 Mapping of electrical parameter space onto model parameter space

3.1 Identification of key model parameters based on sensitivity analysis

In order to be able to construct a mapping from the electrical parameter space onto the model parameter space, it is important to limit the number of model parameters to a set that is able to describe the process variations. A sensitivity analysis therefore is performed to investigate the impact of the model parameters on the simulated device characteristics. The sensitivities are calculated using a measurement-based perturbation method, where a specified parameter p is perturbed from its nominal value by an amount Δp, and the change ΔF on the specified performance measure F for the device is determined. For meaningful comparisons, the result is normalised. Thus, the normalised sensitivity is determined as:

$$sensitivity = \frac{\Delta F / F}{\Delta p / p}$$

The model used to characterise the LDMOS device is a macro-model [4]. The corner extraction methodology described in this paper has been developed for DMOS devices, but could as well be applied to other devices. The motivation in choosing an LDMOS transistor is that there is no automatic direct extraction method available.

For each electrical device parameter (*VTH*, GM_{max}, *IDSAT* and *RON*) a sensitivity analysis was performed. This analysis resulted in a set of model parameters that capture most of the variability of the E-test parameters (see Table 1). The definition of these model parameters is as follows:

- *vth0*: threshold voltage of the MOS transistor modelling the channel of the LDMOS,
- *u0*: mobility of the MOS transistor modelling the channel of the LDMOS,
- *Vsat*: saturation velocity of the MOS transistor modelling the channel of the LDMOS,
- *R*: series resistance parameter modelling the on-resistance of the LDMOS, and
- *Tox*: oxide thickness of the MOS transistor modelling the channel of the LDMOS.

	E-test parameter			
Model parameter	*VTH*	GM_{max}	*IDSAT*	*RON*
vth0	106%	-23.7%	-36.5%	9.2%
u0	-1.8%	82.5%	32.6%	-40.7%
Vsat	-0.3%	16.7%	81.6%	-19.3%
R	-0.1%	-15.1%	-26.2%	72.0%
Tox	-1.4%	-61.1%	-31.9%	8.8%

Table 1: Impact of the key model parameters on the E-test parameters.

3.2 Building the local inverse mapping

After identification of the key model parameters affecting E-test measurements, it is helpful to then build an approximate inverse mapping of the relation between the simulated E-test measurements and model parameters. This approach enables all measured E-test parameter vectors to then be directly translated into model parameter vectors. The method used in this work for building the inverse mapping is to use the typical model (matching nominal device performances) and then employ experimental design (DOE) to vary the model parameters and obtain simulated E-test data. Once matching pairs of E-test and model parameter vectors are obtained, they are fed as training data to a neural network in order to achieve the desired inverse mapping. A schematic overview of this procedure is presented in Figure 2. The type of neural network used here is a multi-layer perceptron with 5 input neurons, 1 intermediate layer containing 7 neurons, and 5 output neurons, in combination with the quasi-Newton training algorithm.

A DOE comprising more than 3000 data-points yields a round-trip accuracy on the order of 1% or better.

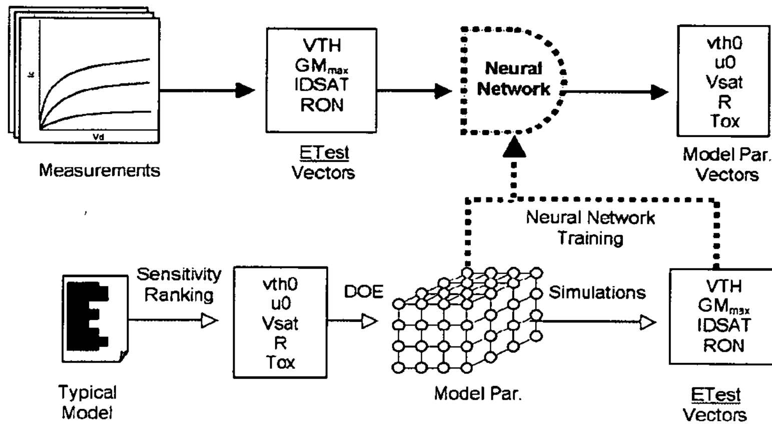


Figure 2: Flow for translating E-Test parameter vectors into model parameter vectors.

The total time needed to simulate the device for all different model parameter values is around 4 hours, while the time needed to train the neural network is only a couple of minutes. It is clear that this method constitutes a speed improvement over the method described in [1].

Once the neural network is trained and the accuracy of the approximation is assessed, it is possible to feed a large set of measured Etest parameter vectors to the neural network, such that a large population of model parameter vectors can be obtained.

4 Generation of worst-case models based on a multivariate analysis

4.1 Univariate approach

The philosophy used for corner simulations and worst-case models is all about the level of guarantee that these simulations can give at the product level. Therefore the worst-case models are defined as a function of a specific performance measure and a confidence level. The confidence level is defined as the probability of finding devices in the population with performances within the two extreme values of the worst-case models.

The traditional methodology used to generate worst-case models consists of performing a univariate statistical analysis on individual Etest parameters, selecting corner values for each individual parameter based on a desired confidence level, and fitting the model parameters to the generated worst-case parameter sets. The problem with this approach is that it does not take into account correlations between E-test parameters and as a consequence the combinations of worst-case E-test parameters may be unrealistic in practice.

4.2 Multivariate approach

The methodology proposed here starts from a multivariate analysis on a large population of data and there are two approaches. These are either an examination of the Etest parameter vectors or the model parameter vectors, translated from Etest parameter space by the neural network. Both methods have been investigated in order to see if comparable results are obtained.

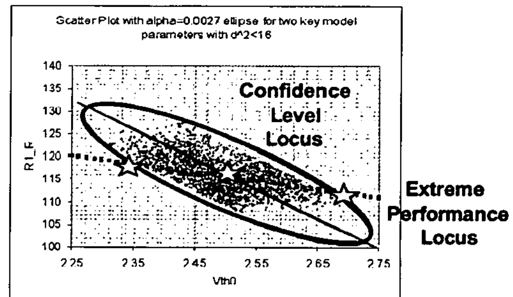


Figure 3: Corners as the intersection of the extreme performance locus and the 99.73% confidence locus of the population.

Setting the location of the worst-case models in the model parameter space is achieved by identifying devices with extreme performances along the specified confidence-level locus of the population. In the case of a multivariate normal distribution, the confidence locus is an ellipsoid, with all points at a fixed variance-weighted distance from the typical model. This ellipsoid can be obtained using Principal Component Analysis (PCA). Figure 3 shows a graphical representation of the corner selection process. In the particular case shown here, the performance

measure chosen was a combination of DMOS switching speed and *RON* performance.

The resulting worst-case models are displayed in Figure 4 in terms of parameter excursions from the typical values, normalised by the univariate standard deviations.

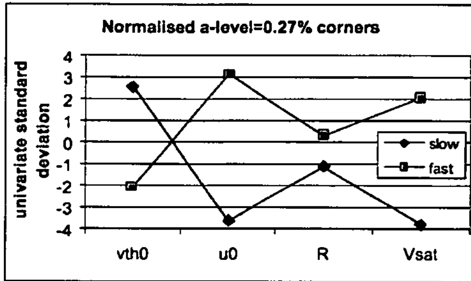


Figure 4: Parameter excursions for worst-case models normalised to univariate standard deviations.

A comparison between the two methods (analysis on model parameters versus analysis on Etest parameters respectively) is shown in Table 2. It can be observed that the relative differences between Etest worst-case values generated by both methods are less than 4%. As the neural network mapping has accuracy better than 1%, these errors can be attributed to the non-linear character of the DMOS model and the linear character of the principal component analysis. Indeed, if a confidence locus is an ellipsoid in one domain, then the transformed locus will not be an ellipsoid, and as a result it cannot be obtained using PCA in the other domain.

Slow corner			
	E-test space	Model space	Difference
VTH (V)	2.759	2.763	0.1%
GM_{max} (µA/V²)	1216	1174	-3.5%
RON (Ω)	305.2	304.1	-0.3%
IDSAT (µA)	1646	1610	-2.2%
Fast corner			
	E-test space	Model space	Difference
VTH (V)	2.389	2.385	-0.2%
GM_{max} (µA/V²)	1405	1390	-1.1%
RON (Ω)	279.4	276.1	-1.2%
IDSAT (µA)	2479	2461	-0.7%

Table 2: Comparison between worst-case corners obtained from analysis on model parameter space versus E-test parameter space.

It is clear that any analysis should strive to make principal component analyses in a domain constituted by parameters, which are either uncorrelated or related in a linear fashion to each other, e.g. dimensions and physical material parameters. In some sense model parameters are one step closer to such parameters than E-test parameters, which can be illustrated by the fact that *IDSAT* distributions are inherently non-normal.

5 Monte-Carlo models

After translation of a large set of Etest parameter vectors to model parameter space by the trained neural network, it is possible to create a Monte-Carlo model. Indeed, after performing a principal component analysis on the model parameter data set, a set of linearly independent vectors in model parameter space are available. These vectors, together with the appropriate eigenvalues (variances) can be fed to a Monte-Carlo analysis tool inside a circuit simulator.

6 Conclusion

This paper has presented an accurate new methodology that drastically reduces the time by a factor of 10 to create both worst-case and Monte-Carlo models. In addition this method also avoids skewing the distributions, adding variability and unexpected correlations, in contrast to an optimiser-based procedure.

The methodology is a simple and robust two-step process. First an extensive experimental design is set up, where by means of simulation, E-test parameters are obtained as a function of key model parameters and an inverse mapping then performed by a neural network. As a second step a large set of measured Etest parameter vectors is fed to the neural network, such that a principal component analysis can be performed in model parameter space. This information can then be used for the rapid creation of realistic worst-case and Monte-Carlo models.

Acknowledgements

This work has been supported by the IST-1999-12257 Automacs project. The authors would like to acknowledge the support of J. Callé, R. Gillon, B. Greenwood and J. Riebeek.

References

[1] S. Healy, E. Horan, K. McCarthy, A. Mathewson, Z. Ning, E. Rombouts, W. Vanderbauwhede, and M. Tack, "Implementation of Statistical Characterisation and Design Techniques for an Industrial 0.5µm CMOS Technology," ICMTS 1999 Proc., Vol. 12, pp. 227-232, March 1999.

[2] M. Qu and M.A. Styblinski, "Parameter Extraction for Statistical IC Modelling Based on Recursive Inverse Approximation," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, pp. 1250-1259, Vol. 16, No. 11, Nov. 1997.

[3] V. Devabhaktuni, M.C.E. Yagoub, and Qi-Jm Zhang, "A robust Algorithm for Automatic Development of Neural Network Models for Microwave Applications," IEEE MTT-S Digest, pp. 2087-2089.

[4] S.F. Frère, J. Rhayem, H.O. Adawe, R. Gillon, M. Tack, and A.J. Walton, "LDMOS Capacitance Analysis versus Gate and Drain Biases, Based on Comparison between TCAD Simulations and Measurements," ESSDERC 2001 Proc., pp. 219-223, Sept. 2001.

Proc. IEEE 2005 Int. Conference on Microelectronic Test Structures, Vol. 18, April 2005

4.3

An Improved LDMOS Transistor Model That Accurately Predicts Capacitance for all Bias Conditions

S.F. Frère[1,2], P. Moens[1], B. Desoete[1], D. Wojciechowski[1], A.J. Walton[2]

[1]AMI Semiconductor Belgium BVBA, Westerring 15, Oudenaarde, Belgium, steven_frere@amis.com

[2]School of Engineering and Electronics, SMC, The University of Edinburgh, Edinburgh, Scotland, UK.

Abstract: This paper proposes an improved SPICE macro-model for the LDMOS device which performs significantly better than existing models in both DC and AC regimes. It has been implemented using standard elements and Verilog-A modules and as a consequence is simulator independent.

INTRODUCTION

DMOS devices are being increasingly employed in dynamic applications such as switches in power systems and for fine slope control of electrical motor drives [1]. However, DMOS models based on a standard MOS model such as BSIM3 are not sufficiently accurate and are especially poor when modelling the AC performance of an LDMOS device as can be observed in Figure 1.

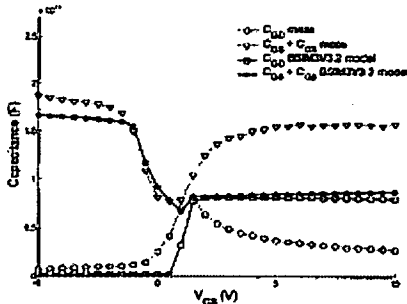


Figure 1. Comparison between measurements and simulations based on a simple BSIM3V3.2 model at V_{DS}=0V for an LDMOS device with W=40μm.

It is known that the intrinsic gate-drain and gate-source capacitances, which to a large extent determine the turn-on and off characteristics of a switch, are not well modelled [2]. To better understand the internal operation of the device TCAD simulations have been used as a platform to increase understanding and thereby develop a superior model by improving the capacitance behaviour.

DEVICE DESCRIPTION

A cross-section of the device under investigation is shown in Figure 2. The device is a floating Lateral nDMOS (LDMOS) processed using the AMI Semiconductor I2T100-flow. This is a smart power technology based on a 0.7μm CMOS process, to which some extra masks and implants have been added to provide the high voltage features [3]. From Figure 2 it can be observed that the LDMOS transistor is an asymmetric device, with the drift region on the drain-side located in a lightly doped N-tub.

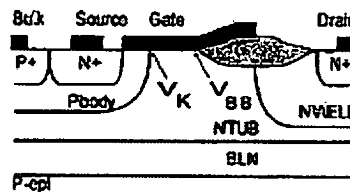


Figure 2. Cross-section of the 60V floating nLDMOS.

The channel is self-aligned to the poly and is created by the out-diffusion of the P-body under the gate. As a result the dopant distribution along the channel is non-uniform and decreases towards the drain end. Higher breakdown voltages are achieved due to the depletion region that extends from the P-body into the drain, which provides a voltage drop between the drain contact and the channel-region. The gate oxide and the polysilicon extend beyond the channel of the device as illustrated in Figure 2. For the device examined in this paper the gate oxide thickness is 42 nm, the threshold voltage (V_T) 2.4V, the off-state breakdown voltage (V_{BD}) 70V and the specific on-resistance (R_{on}) is 160 mΩxmm². Also indicated on Figure 2 are the intrinsic drain voltage V_K at the pbody/ntub junction and the bird's beak voltage V_{BB}.

INTRINSIC DRAIN VOLTAGE (VK) BEHAVIOUR IN RELATION TO GATE AND DRAIN VOLTAGE

It has been shown that an analysis of the internal drain voltage (V_K) is a valid indicator to extract the drift region resistance behaviour. In previous publications [4],[5], an explanation for the V_K behaviour was given based on an analysis of the depletion regions present in the LDMOS device. This is not correct, as the potential distribution in the LDMOS transistor is not only determined by the voltages applied to the gate and drain, but also by the current density

0-7803-8855-0/05/$20.00 ©2005 IEEE 05CH37622

and associated space charge. The simulations in Figure 3 show the effect on V_K and V_{BB} of an open source (i.e. no current flowing in the device) compared to the normal condition (a grounded source with current flowing in the device). For $V_{GS} < V_T = 2.4V$, the transistor is off and the curves for open and grounded sources merge. V_K is linearly dependent on V_{GS} due to capacitive coupling of the gate. For the case when the source of the transistor is grounded, current starts to flow in the transistor from the moment V_{GS} exceeds V_T. The space charge associated with the majority carriers in the drift region will alter the potential distribution in the device, and hence also the V_K potential, provided the electron concentration is the same or exceeds the donor concentration in the drift region. This is, in particular, true for LDMOS devices with a lightly doped drift region. It is evident from Figure 3 that without current flow in the device, V_K monotonically increases as a function of V_{GS}, whereas in real operating conditions (source grounded), the V_K potential starts to diverge from this as soon as $V_{GS} > V_T$. For some biasing conditions, the V_K potential even starts to decrease. Clearly, the effect of the current flow has a large effect on the V_K potential, and as such needs to be taken into account when evaluating V_K.

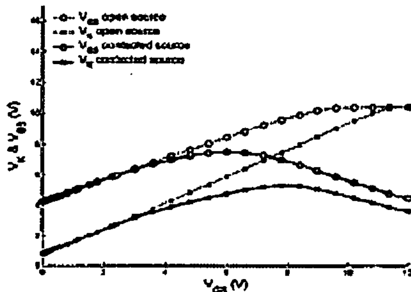


Figure 3. V_K and V_{BB} as a function of V_{GS} with source closed and open at $V_{DS} = 10V$ as from simulations.

An analysis of the potential, current flow and space charge has been performed using 2D device simulations. The resulting space charge simulations are presented in Figure 4, with the length of the accumulation layer identified as L_{acc} and the length between the channel and the field oxide being denoted by $L_{acc\text{-}tip}$. It can be seen that for $V_{GS} > V_T$, part of the lowly doped n-type region under the gate oxide forms an accumulation layer where the current flows. This accumulation layer becomes larger for increasing V_{GS} and at approximately V_{GS}=7V, it reaches the tip of the bird's beak (see Figure 4(b)). From this point on ($L_{acc} > L_{acc\text{-}tip}$), the lateral extension of the accumulation layer is less dependent on V_{GS} because of the thicker field oxide, which forms the bird's beak, resulting in less gate coupling.

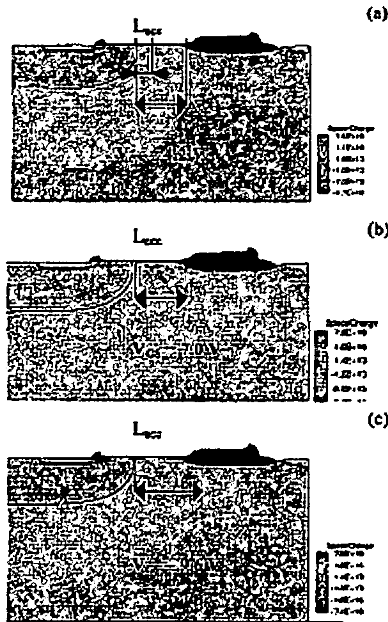


Figure 4. Space charge behaviour for different bias conditions: (a) $V_{GS} = 4.2V$; (b) $V_{GS} = 7.0V$; (c) $V_{GS} = 9.6V$. For all simulations V_{DS} was set to 10V.

To explain the V_K and V_{BB} behaviour, it is instructive to plot the contributions of the channel, accumulation and field oxide drift regions to the total resistance which is presented in Figure 5 as a function of V_{GS}, for V_{DS}=10V. These graphs show that the channel resistance decreases monotonically with increasing V_{GS}. The field oxide drift resistance decreases with V_{GS} until the space charge region reaches the tip of the bird's beak (at around $V_{GS} = 7V$). Further increases in V_{GS} show that the gate control on the field oxide drift region then becomes very small, and as such the field oxide drift resistance saturates. A similar saturation is observed for the accumulation region, but at a higher V_{GS}. This can be explained by the higher gate coupling (thin oxide) of the accumulation region. In the end, the channel resistance also starts to saturate. These three contributions to the total transistor resistance determine the V_K and V_{BB} potential in the device, as the channel, accumulation and field oxide drift resistors are in series and hence act as a voltage divider. For example, inspection of the potential at the bird's beak (V_{BB}), indicates that the field oxide drift resistance completely saturates when $V_{GS} > 7V$, whereas both the channel and the accumulation resistance decrease further for increasing values of V_{GS}. A larger potential drop occurs over the field oxide drift resistor, and hence the V_{BB} potential will start to decrease as can be observed in Figure 3. A similar explanation holds for the V_K potential due to saturation of the accumulation layer resistance, at a higher V_{GS} voltage

(see Figure 3).
The dependency of V_K and V_{DS} on V_{GS} is straightforward. When V_{DS} is increased, a wider depletion layer is formed between the P-body and N-tub regions. As a result of the larger depletion width, a higher gate voltage is needed to accumulate the lowly doped n-type region under the gate oxide. As V_{DS} increases, the maximum value of V_K shifts to a higher V_{GS}.

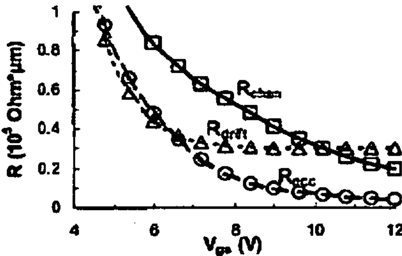


Figure 5. Variation of the channel, accumulation and field oxide drift region resistance (R_{chan}, R_{acc} and R_{drift}) as a function of V_{GS} (V_{DS}=10V).

MESDRIFT TEST-STRUCTURE

A drift resistance extraction method was developed [6]. It involves a dedicated test structure (Figure 6), which has a probing point to enable access to the voltage at the K-point for any bias condition. This structure was designed to verify the drift resistance results, which was confirmed in [6].

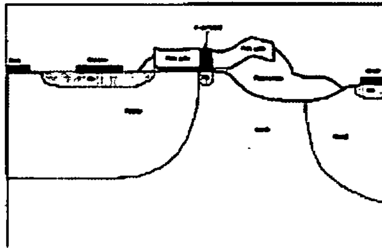


Figure 6. Cross-section of the added n+ implant within the MESDRIFT LDMOS structure.

It can be seen in Figure 7 that the probing node does not affect the DC behaviour of the device

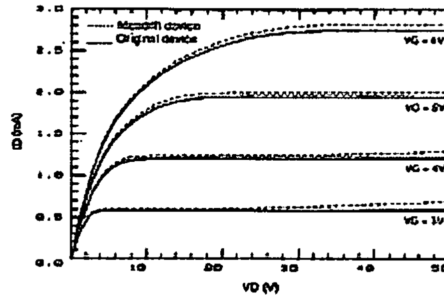


Figure 7. Ids-Vds comparison of of the original structure (without probing node) and the mesdrift structure.

PROPOSED MODEL TOPOLOGY

Figure 8 shows the proposed topology for the new improved LDMOS model, which overcomes many of the limitations of the industry standard BSIM3v3.2 model which was designed primarily for low voltage devices.

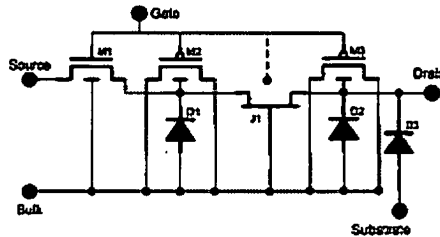


Figure 8. Sub-circuit model of LDMOS device.

Key features of this macro-model are: (1) an adapted JFET to model the drift region resistance and (2) shorted PMOS transistors, which model the capacitance behaviour of the drift region. The following section briefly describes the key components of the model.

JFET (J1) (drift region)

The drift region is modelled using a modified JFET model with the equations based on the Schichman & Hodges model [7]. These equations are implemented in a Verilog-A module. The operation of the JFET is such that, when a more negative voltage is applied to the gate of the JFET, the device becomes more resistive as the depletion regions expand narrowing the channel of the JFET. The gate voltage of the JFET is in fact the voltage between the bulk and the V_K point of the macro-model. Thus, an increase in V_K, making the gate voltage of the JFET more negative, will result in a higher JFET resistance, which corresponds to the behaviour detailed previously. The adaptation of the JFET model provides the capability for the

77

threshold voltage of the JFET to be dependent on the gate voltage of the LDMOS (Figure 9), which is essential for the model to achieve a good overall accuracy. If the threshold voltage of the JFET is fixed, a large increase in V_K pinches off the JFET channel completely, resulting in the drift region resistance being too high. By making the threshold voltage of the JFET increase with V_{GS}, the use of a wider voltage range is possible, as the JFET will never pinch off completely. This limitation is observed in [8]. Figure 10 shows the SPICE simulation result of V_K. The high V_K value when V_{GS} is below V_T is due to the fact that there is no current flowing. When V_{GS} is higher than V_T, the behaviour is similar to that shown in Figure 3 although it should be noted that the voltage level is higher. This can be explained by the fact that the voltages obtained by TCAD simulations are highly dependent on the location of the probing point.

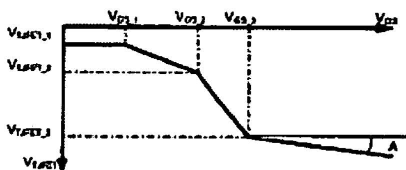


Figure 9. JFET V_T dependence as a function of V_{GS}.

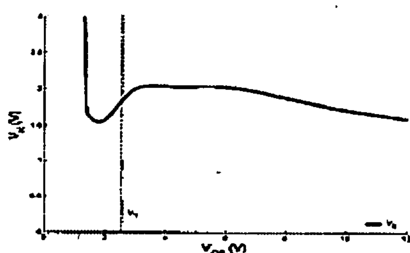


Figure 10. V_K as modelled by a JFET as a function of V_{GS} at V_{DS}=10V.

Shorted p-type MOS transistors (M2 & M3)

Two shorted p-type MOS devices (for an n-type DMOS model) have been implemented in order to model the N-tub region overlapped by the poly plate. The transistor M2 has a thin gate-oxide and models the drift region covered by the thin oxide of the DMOS. Transistor M3 has a thick gate-oxide and models the drift region covered by the field oxide of the DMOS. The drift region changes from inversion to depletion to accumulation with increasing V_{GS}, the behaviour of which is similar to the capacitance operation of a p-type MOS device under similar bias conditions. By using the capacitance behaviour of a p-type MOS device in an n-type DMOS model, together with accurate modelling of the drift resistance, a good fit of the LDMOS capacitances can be obtained.

RESULTS AND DISCUSSION

The parameters for this new model have been extracted from LDMOS devices capable of handling 60V on the drain and 12V on the gate. The extractions were performed on a device set with widths ranging from 20 to 250μm. The model has been verified for the complete bias range and good agreements between model and measurements have been obtained as illustrated by the AC-characteristics shown in Figure 11 and the DC

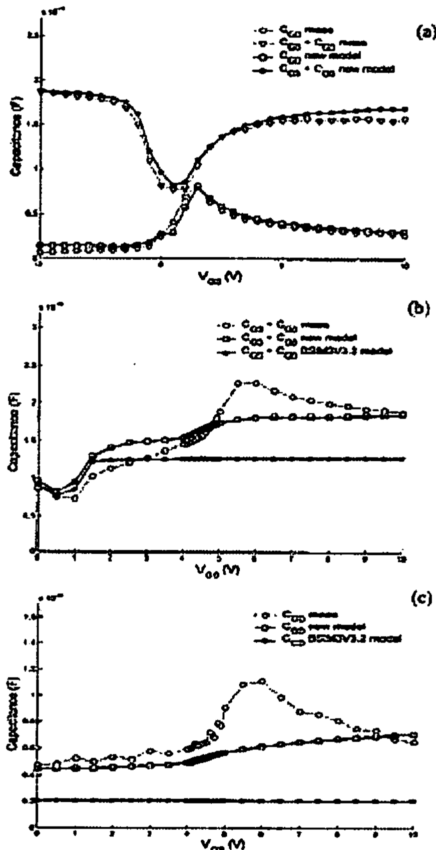


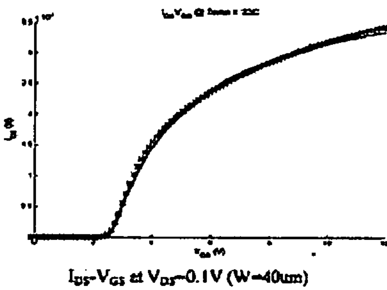
Figure 11. Simulated and measured C_{GD} and C_{GS} curves as a function of V_{GS} at V_{DS}= 0 and 20V for both the old and new models. (W=40μm) (a) Comparison between measurements and simulations based on the new macro-model at V_{DS} = 0V; (b) Comparison of C_{GS} measurements and simulations based on the new macro-model and old model at V_{DS} = 20V; (c) Comparison of C_{GD} measurements and simulations based on the new macro-model and old model at V_{DS} = 20V.

78

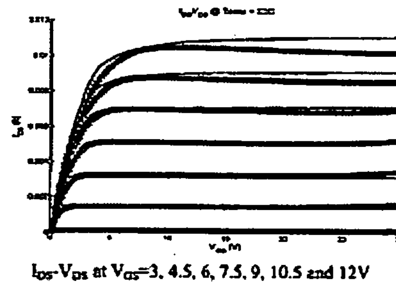
characteristics shown in Figure 12. The temperature behaviour of the model has been validated for temperatures ranging between -50 and 180°C (DC) and the overall DC-behaviour results in maximum errors of less than 10%.

The AC-measurements presented in this paper are the result of S-parameter measurements which are then converted to their corresponding capacitances. This makes it possible to measure capacitances for a V_{DS} different from 0V. A drawback is that C_{GS} and C_{GB} are measured together as the source and bulk of the device are connected together to allow S-parameter measurements.

The improvement of the new model over the BSIM3V3.2 model of the simulated capacitances can be readily observed by comparing Figure 1 and Figure 11. It is apparent that conventional MOSFET models or the Philips MM20 model do not exhibit a peak in C_{GD}, and it can clearly be seen that LDMOS devices have a distinctive capacitance behaviour. Figure 11 shows the AC results of the new model, and when V_{DS} = 0V a very good fit is achieved with the new model compared with the old BSIM3V3.2 one, which struggles to fit the capacitances at all. For V_{DS} higher than 0V the fit has a maximum error of 30%, which is considered a good fit for highly bias dependent capacitances. The peaks observed in the measured C_{GS} and C_{GD} curves (Figure 11 (b) and (c)) are very difficult to mimic. However, the new model shows an increase at the correct location, which is patently not present in the old model.
The distinctive characteristic of LDMOS capacitances is due to the behaviour of the drift region [8], [9]. The main focus of this paper is on the modelling the AC characteristics of LDMOS devices, however an overall good model should be accurate as well in AC as in DC. In Figure 12 one can see that the DC behaviour is also well modelled.



I_{DS}-V_{GS} at V_{DS}=0.1V (W=40um)



I_{DS}-V_{DS} at V_{GS}=3, 4.5, 6, 7.5, 9, 10.5 and 12V

Figure 12. LDMOS DC characteristics at temperature of 25°C (Thick x lines are measurements; solid line are simulations)

CONCLUSION

An improved DMOS macro-model has been presented which, in contrast with other macro-models, is physically based and covers all bias-regions. In particular it models the impact of the drift region on DMOS capacitance behaviour. It performs well for both DC and AC regimes and, as standard elements or Verilog-A blocks have been used, the model is simulator independent which will facilitate its use by the design community.

ACKNOWLEDGEMENTS

This work is supported by the IST-1999-12257 Automacs project.

REFERENCES

[1] N. Mohan, T.M. Underland, W.P. Robbins, *"Power Electronics - Converters, Applications and Design"*, John Wiley & Sons, 1995, 2nd edition.
[2] L. Budihardjo, P.O. Lauritzen, H.A. Mantooth, *"Performance requirements for Power MOSFETs model"*, IEEE Transactions on Power Electronics, vol.12, n°1, January 1997.
[3] H. Bellan, M. Declercq, *"High Voltage Devices and Circuits in Standard CMOS Technologies"*, Kluwer Academic Publishers, 1999.
[4] N. Hefyene, C. Anghel, A.M. Ionescu, S. Frère, R. Gillon, M. Vermandel, B. Bakeroot and J. Doutreloigne, *"An experimental approach for bias-dependent drain series resistances evaluation in asymmetric HV MOSFETs"*, ESSDERC 2001 Proc., pp.403-406, Sep. 2001.
[5] C. Anghel, N. Hefyene, A.M. Ionescu, S. Frère, R. Gillon, M. Vermandel, B. Bakeroot, J. Doutreloigne, C. Maier and Y. Mourier, *"Investigations and physical modelling of saturation effects in Lateral DMOS transistor architectures based on the concept of intrinsic drain voltage"*, ESSDERC 2001 Proc., pp.399-402, Sep. 2001.
[6] C. Anghel, N. Hefyene, A. Ionescu, S. Frère, R. Gillon, J. Rhayem, *"Universal Test Structure and Characterization Method for Bias-Dependent Drift Series Resistance of HV MOSFETs"* ESSDERC 2002 Proc., pp. 247-250, Sep. 2002.
[7] *"Affirma Spectre Circuit Simulator Reference"*, Product Version 4.4.6, June 2000.
[8] E.C.Griffith, S.C.Kelly, J.A.Power, D.Bain, S.Whiston, P.Elebert, M.O'Neill, *"Capacitance Modelling of LDMOS Transistors"*, IEEE Solid-State Device Research Conference, Sept. 2000, pp. 624-627.
[9] J. Olsson, R. Valtonen, U. Heinle, L. Vestling, A. Soderbarg, Norde, *"A Capacitance-Voltage Measurement Method for DMOS Transistor Channel Length Extraction"*, IEEE Int. Conference on Microelectronic Test Structures, March 1999, pp. 135-140.

An experimental approach for bias-dependent drain series resistances evaluation in asymmetric HV MOSFETs

N. Hefyene,
C. Anghel
A.M. Ionescu
EPFL, Lausanne, Switzerland
Naser.Hefyene@epfl.ch

S. Frere
R. Gillon
Alcatel Microelectronics Belgium

M. Vermandel
B. Bakeroot and J. Doutreloigne
ELIS-TFCG/IMEC University of Gent Belgium

Abstract

In this work, a simple experimental technique, dedicated to the evaluation of bias-dependent drain series resistance in asymmetric HV MOSFETs, independent of the extended drift region architecture, is proposed and validated. The technique consists into two experimental steps: (I) the extraction of the drift resistance at low drain voltage based on direct and reversed configurations and (II) the experimental evaluation of the series resistance derivative as a function of the drain voltage, followed by its integration. The method is used to investigate a 60V LD-MOSFET drift series resistance dependence on the gate and the drain voltages, from low- to high-voltage regimes. Numerical 2D simulations were carried out to confirm the experimental results and to conclude on the physical origins of the reported bias-dependence.

1. Introduction

The proper analytical modelling of HV MOS transistors requires adapted characterization of series resistances, with particular interest on the drain R_D (or drift, R_{Drift}) series resistance which is bias-dependent. The R_D bias-dependence is specific to the particular extended drain region, engineered in order to provide increased drain-bulk and drain-gate breakdown voltages.

In the past years, special efforts have been dedicated [1]-[3] to develop or to adapt methods for R_D or (R_D-R_S) evaluations originating in the modeling and characterization of low-voltage MOSFETs. Generally, these works agree on the fact that the accuracy and interest on a R_D series extraction method are substantially increased as far as the technique is independent on the particular $R_D(V_D,V_G)$ relationship (i.e. a minimum assumption criteria). This paper proposes and validates such a method in a two-step D.C. measurement.

2. Test devices

The experimental test devices are asymmetrical n-channel, self-aligned double-diffused DMOS (L-DMOS) transistors, selected from the I^2T technology of Alcatel Microelectronics, Fig. 1. A 0.7µm CMOS process with an adapted couple of extra-masks and implants to provide high-voltage capabilities ranging from 30V up to 100V, has been used. The technology provides both self-aligned double-diffused DMOS (LDMOS) and drain-extended MOS devices.

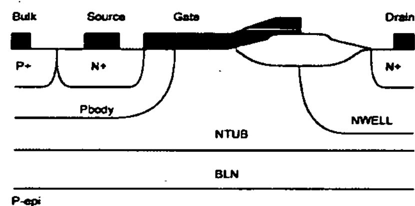


Fig. 1 Cross section of the investigated n-channel LDMOS transistor.

3. $R_D(V_G, V_D)$ extraction method

The proposed $R_D(V_G,V_D)$ extraction method consists in two main successive steps: (I) the evaluation of the drain resistance at low drain voltage, R_{D0}, with the gate bias as a parameter, and (II) the adaptation of Otten's method [2] to evaluate the drain resistance derivative with respect to the drain voltage dR_D/dV_D at constant gate voltage. Finally, the drain series resistances is evaluated as:

$$R_D(V_D, V_G) = R_{D0}(0, V_G) + \int_0^{V_D} \frac{\partial R_D}{\partial V_D} dV_D \quad (1)$$

This method is useful for the development of analytical models for voltage-controlled series series resistances in HV MOSFETs since it allows their pure experimental evaluation.

3.1 Inter-changed drain-source measurement at constant current

Asymmetric R_S and R_D series resistances are expected to differently impact the related gate and drain de-bias if the extrinsic transistor is measured successively in forward (i.e. normal) and reversed (source and drain interchanged) configurations, Fig. 2 a and b. In order to efficiently exploit this idea [1], [3], an identical constant drain current is injected in forward and reversed configuration while recording the V_{Df} and V_{Dr} drain voltages as functions of V_{Gf} and V_{Gr}, respectively. The current level is kept low in order to ensure operation in the linear regime and ensure an identical R_D value in both configurations, in contrast to [2]. As a consequence, supposing $R_S \ll R_D$, the drain series resistance is then calculated based on the difference between the gate voltages which ensure in forward and reverse modes identical extrinsic drain voltages, $V_{Df}=V_{Dr}$, with the MOS transistor in quasi-linear operation:

$$R_D \cong R_D - R_S = \frac{V_{Gf} - V_{Gr}}{I_D(1 + dV_T / dV_{SB})} \quad (2)$$

Typical measurements on a LDMOS device and the extraction procedure are illustrated in Fig. 3. Based on this measurement, the low-voltage drain, R_{D0}, series resistances is plotted as a function of $V_G=V_{Gf}$, at constant current, Fig. 4. For $V_G<4V$, the drain series resistance decreases with V_G, independently on the current levels because of the reduction of the depletion controlled regions in the LDMOS drift region. Same comments apply for current levels >250μA. An experimental R_{D0} increase for $V_G>5V$ is observed with this method for $100\mu A<I_D<250\mu A$, Fig. 4. This interesting effect can be explained by the onset of an accumulation channel in the drift region under the thin oxide. The effect of this accumulation layer is the increase of the effective MOS channel length, L_{eff}, which, at constant current, involves the increase of the extrinsic V_D (and an equivalent higher series resistance). Therefore, to correctly extract R_{D0}, the level of the injected current has to be carefully set.

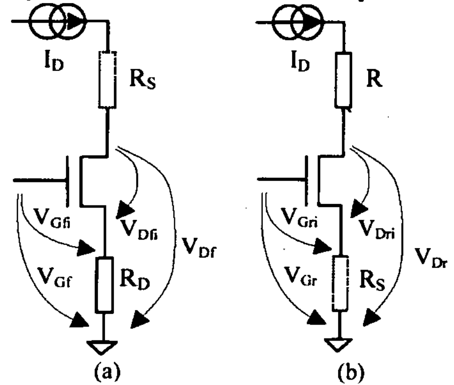


Fig. 2 Experimental setup: (a) forward and (b) reversed source and drain, measurements dedicated to R_{D0} extraction.

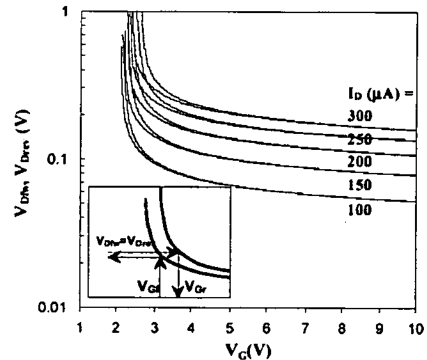


Fig. 3. Experimental dependence, V_{Df} and V_{Dr} versus V_G at constant injected I_D current in a n-channel LDMOS transistor.

Fig. 4 Drain series resistance, R_D, extracted values at low current bias vs. V_G, in n-channel LDMOS.

3.2. Experimental evaluation of drain series resistance derivative dR_D/dV_D

Generally, in case of MOS transistors with bias-dependent series resistances, it has been shown that a more complex modeling of the g_d, g_b and g_m extrinsic conductances, as functions of the intrinsic ones, and including source and drain series resistance derivatives (with respect to the gate and drain voltages) must be used for accurate modeling. For our extraction procedure, we propose to artificially re-construct the quantitative derivative dR_D/dV_D, by the use of a variable resistor in the drain of the LDMOS transistor. With the extrinsic (measured) output conductance given by [1]:

$$g_d^{-1} = \frac{1 + g_{di}(R_D + R_{Dadd}) + (g_{mi} + g_{bin})R_S}{g_{di}(1 - \partial I_D / \partial V_D)} \quad (3)$$

where superscript 'i' applies for the intrinsic transistor (see Fig. 1), it follows that the slope of dg_d^{-1}/dR_{Dadd} versus R_{Dadd} plot can be used for the dR_D/dV_D extraction according to:

$$\frac{dR_D}{dV_D} = \frac{1 - \partial g_d^{-1} / \partial R_{Dadd}}{I_D} \quad (4)$$

Note that the usefulness of this type of extraction is expected to be somewhat limited in the saturation region of the intrinsic MOS transistor, when the drain current becomes practically independent of the drain series resistance. In contrast, the method appears particularly useful for the so-called HV DMOS quasi-saturation regimes when associated with a quasi-linear operation of the intrinsic MOS transistor. Fig. 5 presents the typical effect induced on the output characteristics of the L-DMOS by adding various external series resistances. Relevant characteristics shifts are observed in the quasi-linear regions and in the saturation voltages. Based on the measured data reported in Fig. 5, we were able to plot g_d^{-1} versus R_{Dadd} and estimate with acceptable accuracy its slope up to V_D=15V, Fig. 6. The subsequently calculated drain series resistance derivative is presented in Fig. 7. Using a simple numerical integration procedure of the deduced derivative plot, combined with eq. (1) and using the corresponding value of R_{D0} at same constant V_G, permits the estimation of the overall drain-bias dependence of $R_D(V_D)$ as shown in Fig. 7.

Fig. 5 Experimental I_D-V_D and g_{ds}-V_D characteristics of a n-channel LDMOS transistor, without and with various added external drain series resistance, R_{Dadd}.

Fig. 6 Linear plot of g_{ds}^{-1} versus R_{Dadd} at various drain voltages and constant V_G (data from Fig. 4), in case of a n-channel LDMOS transistor.

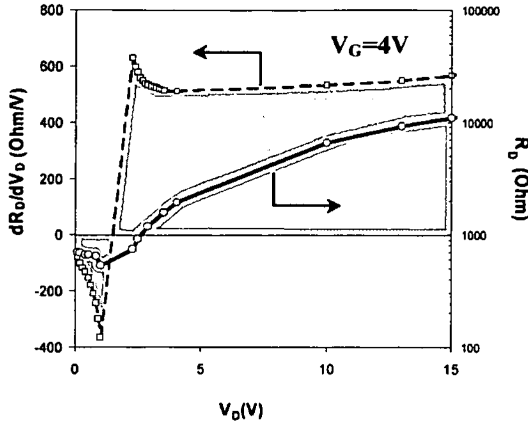


Fig. 7 Experimental dR_D/dV_D and calculated (numerical integration) R_D, as functions of V_D at constant V_G (n-channel LDMOS transistor with channel dimensions: W=40μm and L=0.9μm).

4. Simulations and discussion

In order to confirm this method, systematic 2D numerical simulations have been carried out on calibrated structures and the drain series resistance have been extracted based on the intrinsic drain-voltage concept [4] as:

$$R_D \cong R_{Drift} = (V_D - V_K)/I_D \qquad (5)$$

where V_K is the potential of the intrinsic LDMOS drain. Fig. 8 shows in a 3D plot the overall $R_D(V_G, V_D)$ dependence, as deduced from numerical simulated structures and using eq. (4). R_D decreases with V_G and increases with V_D (except V_D<0.5V) due to the corresponding control of depleted zones (J-FET like effect) and formation of accumulation/bulk channel in the drift zone. One of the most interesting simulation result is depicted in Fig. 9: when V_D is reduced toward linear region, a minimum followed by a resistance increase, more accentuated for high V_G appears, which confirms the experimental result concerning the impact of an accumulation channel. The very good agreement between the simulated and experimental $R_D(V_G,V_D)$ is demonstrated by Fig. 9, where both the drain resistance and its derivative confirm the results reported in Fig. 6 with the proposed method (even the particular dependence reported at very low V_D).

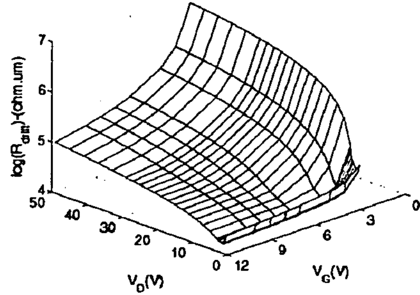


Fig. 8 R_{drift}=$R_D(V_G,V_D)$ surface plot for n-LDMOS; calculated with eq. (5) using data from numerical simulation.

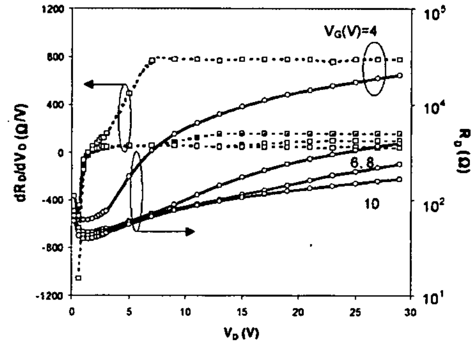


Fig. 9 Numerical simulation: drain resistance, R_D, and its derivative as functions of V_D for various V_G (W=40μm, L=0.9 μm).

6. Conclusion

A simple, yet universal methodology, dedicated to the extraction of drain series resistances in asymmetrical HV MOS transistors, has been proposed and validated. The two-step extraction technique is quasi-independent on the particular $R_D(V_G,V_D)$ dependence and consequently, extremely useful for the development of analytical models. Numerical simulations confirmed the experimental results and allowed the investigation of specific physical origins of R_D bias-dependence in n-channel LDMOS.

6. References

[1] A. Ortiz-Conde, J.J. Liou, W. Wong and F.J. Garcia Sanchez, Electronics Letters, Vol. 30, No. 12, 1994, p. 1013.

[2] Jan A. M. Otten and F. M. Klaassen, IEEE Trans. El. Dev., Vol. 43, 1996, p. 1478.

[3] A. Blaum, J. Victory and C. C. McAndrew, , ICMTS, Int. Proc. IEEE 1999, Vol. 12, 1999, pp. 141-146.

[4] C. Anghel et al., submitted to ESSDERC 2001.

Investigations and Physical Modelling of Saturation Effects in Lateral DMOS Transistor Architectures Based on the Concept of Intrinsic Drain Voltage

C. Anghel, N. Hefyene, A.M. Ionescu — EPFL, Switzerland — costin.anghel@epfl.ch

M. Vermandel, B. Bakeroot, J. Doutreloigne — IMEC, Belgium — miguel@elis.rug.ac.be

R. Gillon, S. Frere — Alcatel Microelectronics, Belgium

C. Maier — Robert Bosh GmbH, Germany

Y. Mourier — Silvaco, France

Abstract

Thorough investigations of the saturation phenomena in state-of-the-art HV Lateral DMOS architectures (L-DMOS and X-DMOS), based on 2D numerical simulation and on the new concept of intrinsic drain potential, V_K, are presented. The paper highlights the V_K evolution in all operation regimes, analyses the corresponding complex quasi-saturation mechanisms and originally demonstrates that this key potential remains at a low-voltage and shows a marked maximum value at low V_G. A simple and accurate analytical modelling strategy, which is usable for any architecture-specific bias-dependence of the drift region equivalent resistance is proposed based on the V_K-concept. Very good model performances using a BSIM3v3 low-voltage model combined with the proposed intrinsic MOSFET strategy are reported.

1. Introduction

Main interest for HV Lateral MOSFETs originates in their applications in automotive and RF. Acceptable simulation accuracy of these devices is obtained by the use of adapted macro-models based on conventional low-voltage modules. The main disadvantage of these macro-models is that they are not physical and, moreover, not able to take into account the special phenomena specific to high voltage operation, which results in a limited modelling range. Key characteristic of a HV Lateral MOS transistors are related to the architecture of the extended drain (or drift) region, which is responsible for the so-called quasi-saturation effects. Several works dealt with the physics involved in the specific behaviour, especially quasi-saturation, of these transistors [1], [2]. Unfortunately, they were focused on the analysis and modelling of some limited ranges/effects and the overall low- and high-voltage regimes are rarely discussed and modelled together The increased difficulty in physical and accurate analytical modelling are related to complex 2D effects, specific to modern HV device architectures.

2. X- and L-DMOS device architectures and TCAD

The Alcatel Microelectronics I2T flow builds up-on a 0.7um CMOS process adding a couple of extra-masks and implants to provide high-voltage capabilities ranging from 30V to 100V. The technology provides both self-aligned double-diffused DMOS (LDMOS) and drain-eXtended MOS devices (XDMOS) both with N- and P-channels. Only the N-channel architectures are analysed in this paper (fig.1)

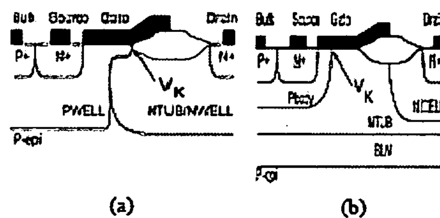


Fig. 1 Device cross-sections: (a) X-DMOS and (b) L-DMOS Inset: location of K-point (intrinsic drain).

As a preparation to the TCAD simulations, the various process layers were calibrated by verifying them with SIMS and SRP profiles. For the bird's beak, the faster compress model corrected with an additional mask biasing to justify the spacing was used. A good fit for the shape is verified using SEM cross sections.

3. Intrinsic drain voltage dependence on gate and drain potentials: $V_K(V_G, V_D)$

An original analysis of HV MOS devices based on the intrinsic drain voltage concept is proposed in the following. The intrinsic low-voltage MOS transistor is delimited by the source of the HV transistor and the end of intrinsic inversion channel (boundary between the p-region and the extended drain n-region, as shown in Figs. 1 a and b). This location is called the key-point and its potential is denoted by V_K. Numerical simulated 2D structures allow to access the variation of V_K with respect to V_G and V_D in all regions of HV transistor operation. In this analysis the self-heating was not enabled. Fig. 2a presents in a 3D plot the extracted V_K dependence on V_G and V_D voltages (V_S and V_B are grounded) for an X-DMOS structure. It is clearly demonstrated that V_K<3.5V up to V_D=20V (an extended analysis demonstrates that V_K<5V for V_D<60V). The V_K value is then used to distinguish between: the operation region of the intrinsic MOS and the voltage drop on the extended drift region. Figs. 2 b and c depict the detailed V_K-V_D and V_K-V_G variations. It is clear that, in a first approximation, the V_K potential is expected to rise up with V_D, which drives the transistor from linear to saturation (Fig. 2b) and also with V_G, which raises the surface potential (Fig. 2c). An interesting result is that V_K appears to decrease with V_G after reaching a maximum at constant V_D (see Fig. 2b). This trend is also highlighted in Fig. 2b where V_K value reduces with V_G for gate voltages higher than around 4V. The analysis of the 2D simulated structures shows that this maximum corresponds to a pinch-off of depletion regions in the drift (the current is then forced through a depletion zone), Fig. 3. A higher V_G avoids this pinch-off and can even generate a local accumulation or carrier injection in the substrate near drift region bird's beak, which explains the V_K reduction with V_G after reaching the maximum.

Similar dependences are reported in Figs. 4 a and b for the L-DMOS architecture and also for vertical devices [3]. The particularity of L-DMOS structure is more accentuated V_G- and V_D-controlled formation of a long accumulation channel in the n-region under the thin oxide, which impact the equivalent length of the intrinsic short-channel transistor.

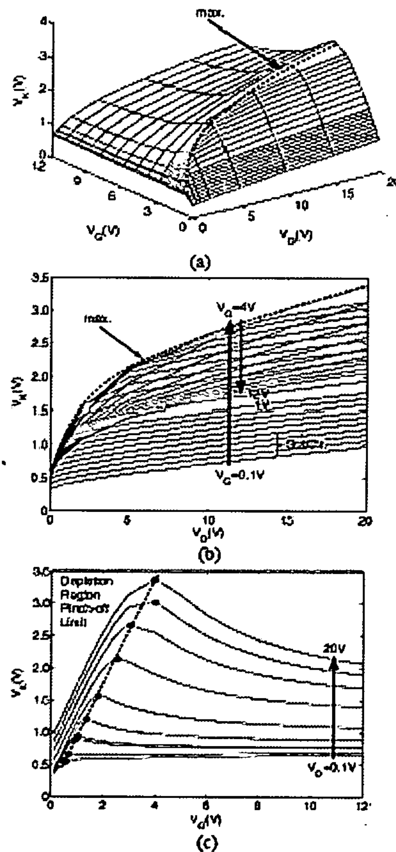


Fig. 2 X-DMOS channel voltage variation function of V_G and V_D: (a) overall 3-D representation, (b) V_K vs. V_D with V_G as a parameter and (c) V_K vs. V_G with V_D as a parameter.

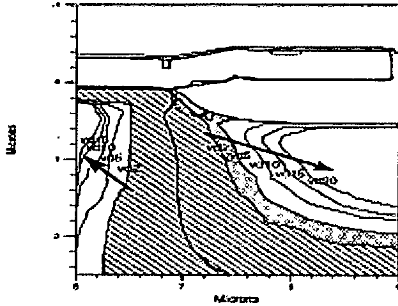


Fig. 3 XDMOS 2D structures with depletion boundary evolution vs. V_D at constant $V_G(=3V)$: depletion pinch-off in the drift for $2V<V_D<5V$.

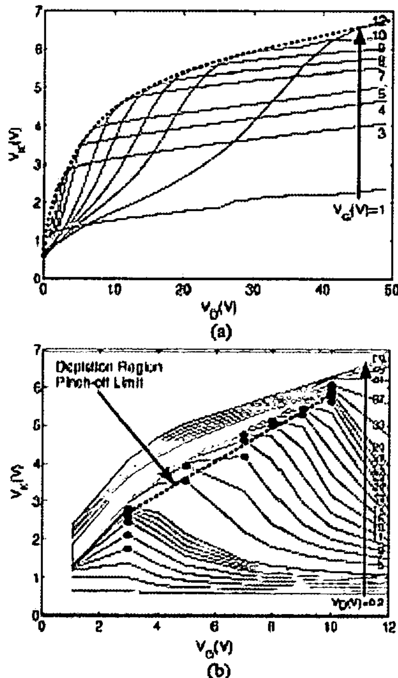


Fig. 4. LDMOS key-point characteristics: (a) V_K vs. V_G with V_D as a parameter and (b) V_K vs. V_D with V_G as a parameter. The reported characteristics demonstrate that $V_K < 7V$ in all regimes of operations, and a V_G-controlled maximum occurs.

4. Analysis of saturation mechanisms

4.1 X-DMOS architecture

The output characteristics of the intrinsic and extrinsic lateral DMOS transistors are reported in Figs. 5 a and b. The V_K quantitative investigation at high V_D allows to distinguish between the following saturation mechanisms, Fig. 5 b: (I) at low V_G values (<4V) the saturation is controlled by the intrinsic channel pinch-off, (II) for moderate gate voltages ($4V<V_G<10V$) an accumulation/bulk channel forms in the drift while the intrinsic MOS part remains in quasi-linear operation (no depleted region is present in the current path due to the injection of the electrons in the drift zone) the current is not fully saturated (quasi-saturation) and (III) for higher V_G (>10V) carrier velocity saturation occurs in the drift zone while the intrinsic MOS is in the linear region (quasi-saturation region).

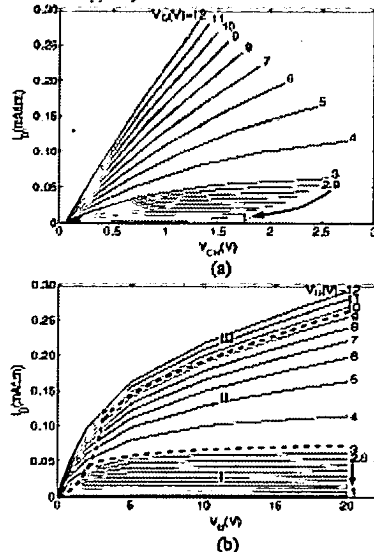


Fig. 5 XDMOS output characteristics: (a) intrinsic transistor and (b) extrinsic transistor.

4.2 L-DMOS architecture

The intrinsic and extrinsic L-DMOS transistor output characteristics are reported in Figs. 6 a and b. In regions (I) the saturation mechanism

is similar to the one described in the X-DMOS architecture (intrinsic channel or drift region pinch-off). In region (II), Fig. 6b, the current saturates due carrier velocity saturation in the intrinsic MOS (which has a short-channel). As a result, the (quasi-) saturation current becomes an almost linear function of V_G as it can be seen in Fig. 6b for V_G=7, 8, 9 and 10V. Note that for increased V_D, velocity saturation or pinch-off in the drift can also be superposed. Region III is characterized by an intrinsic transistor operating in the quasi-linear region with an accumulation channel in the drift and a J-FET like saturation control.

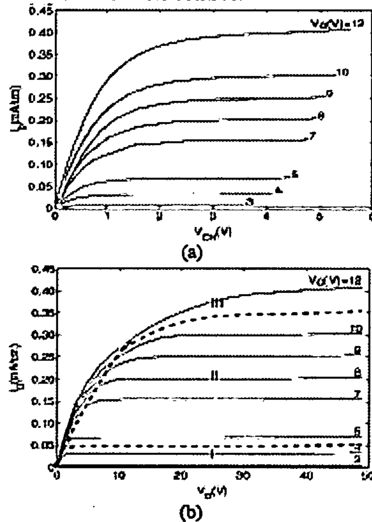


Fig.6 LDMOS output characteristics: (a) intrinsic transistor and (b) extrinsic transistor.

5. Towards a low-voltage MOS modelling strategy based on the V_K-potential

The presented investigations suggests two main results: (i) the V_K remains at a low voltage and its maximum occurs at low V_G (V_K<3.5V, V_{Gmax}<4V, for the X-DMOS) and (ii) the drift zone physical specific phenomena are mirrored in the V_K voltage and can be modelled by a controlled V_G-, V_D- voltage source. The idea to use a conventional low-voltage MOSFET (like BSIM3v3) to tune the characteristics of the intrinsic MOS (with equivalent $V_{CH}=V_K-V_S$, combined with an adapted model of a voltage controlled source appears then natural. In Fig. 7, typical fits on the numerical-simulated data are presented for the extrinsic X-DMOS transistor using a BSIM3v3 model calibrated on the intrinsic transistor, a drift resistance (with V_R voltage drop) and a voltage-controlled source V_{VAR}. The curves cover all reported saturation regions. The maximum error is reported to be <8% and the average error <5%. It is worth noting that one main advantage of this fitting strategy is that the parameter values of the intrinsic transistor are all physical.

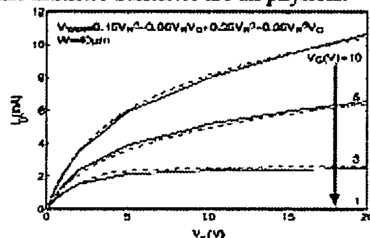


Fig.7 Extrinsic X-DMOS: simulated output characteristics: BSIM (dashed) vs. TCAD (solid). Inset: polynomial voltage-controlled source.

Conclusion

An original, 2D simulation-based analysis of saturation mechanisms in HV lateral MOS transistors, based on the intrinsic drain voltage, V_K, was proposed. It was demonstrate that saturation mechanism is a sensitive function of the device architecture. A simple V_K-based modelling strategy using a low-voltage BSIM3v3 transistor module and a polynomial voltage-controlled source was validated.

Acknowledgement: This work was supported by the IST-1999-12257 Automacs project.

References

1. Y.-S. Kim, J. Fossum, "New Physical Insights and Models for High-Voltage LDMOS IC CAD", *IEEE Trans. Electron Devices*, vol. 38, pp. 1641-1649
2. J. Jaejune, T. Arnborg, Yu. Zhiping, R.W. Dutton, "Circuit model for power LDMOS including quasi-saturation", *Proceedings of SISPAD '99*, pp.15-18
3. C.H. Kreuzer, N. Krischke, P. Nance, "Physically based description of quasi-saturation region of vertical DMOS power transistors", Proceedings of International Electron Devices Meeting, 1996, pp. 489 – 492

PHYSICAL MODELLING STRATEGY FOR (QUASI-) SATURATION EFFECTS IN LATERAL DMOS TRANSISTOR BASED ON THE CONCEPT OF INTRINSIC DRAIN VOLTAGE

C. Anghel[1], N. Hefyene[1], A.M. Ionescu[1], M. Vermandel[2], B. Bakeroot[2], J. Doutreloigne[2], R. Gillon[3], S. Frere[3], C. Maier[4], Y. Mourier[5]

[1]Ecole Polytechnique Fédérale de Lausanne, Switzerland
[2]IMEC, Belgium
[3]Alcatel Microelectronics, Belgium
[4]Robert Bosch GmbH, Germany; [5]Silvaco, France

Abstract.–This paper deals with the investigation of the LDMOSFET saturation mechanisms via 2D numerical simulations and experiments. A clear separation between the saturation of intrinsic MOS transistor and complex quasi-saturation mechanisms is made using the intrinsic drain concept. A modelling strategy for drain current based on the experimental extraction of the drift series resistance is presented. Very good model performances using a BSIM3v3 low-voltage model combined with the proposed drift resistance extracted values are reported.

I. INTRODUCTION

The interest in accurate modelling of high voltage transistors has been increased in the last years due to the compatibility of these devices with CMOS standard technology. LDMOS transistors are fast switching components able to drive high currents for large biasing voltages. As a result, nowadays LDMOS devices are largely used in automotive and RF applications. An acceptable simulation accuracy of these devices can be obtained by the use of adapted macro-models, based on conventional low-voltage modules. The limitations of these macro-models lie in the impossibility of physical modelling of some special characteristic phenomena of these devices. Several works dealt with the physics involved in the specific behaviour, especially quasi-saturation, of these transistors [1], [2]. Generally, they were focused on the analysis and modelling of some limited ranges/effects and the overall low- and high-voltage regimes are rarely discussed and modelled together. The increased difficulty in physical and accurate analytical modelling is related to complex 2D effects, specific to modern HV device architectures.

II. LDMOS ARCHITECTURE AND TCAD

The high voltage devices under investigation are asymmetrical n-channel self-aligned double-diffused DMOS (L-DMOS) transistors, selected from the I^2T technology of Alcatel Microelectronics, Fig. 1.

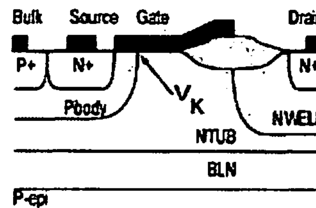


Fig. 1. Cross section of the investigated n-channel LDMOS transistor.

This technology is based on a 0.7μm CMOS process to which a couple of extra masks and implants are added to provide high-voltage capabilities ranging from 30V to 100V. The technology provides both self-aligned double-diffused DMOS (LDMOS) and drain-extended MOS devices. Only LDMOS n-channel devices are studied in this paper.

As a preparation to the TCAD simulations, the various process layers were calibrated by

0-7803-6666-2/01/$10.00 © 2001 IEEE

verifying them with SIMS and SRP profiles. A good fit for the shape is verified using SEM cross sections.

III. INTRINSIC DRAIN VOLTAGE DEPENDENCE ON GATE AND DRAIN POTENTIALS.

The intrinsic low-voltage MOS transistor is delimited by the source of the HV transistor and the end of intrinsic inversion channel (boundary between the p-region and the extended drain n-region, as shown in Fig.1). This location is called the key-point and its potential is denoted by V_K. Numerically simulated 2D structures allow to access the variation of V_K with respect to V_G and V_D in all regions of HV transistor operation. Note that in this work the self-heating was not enabled in the numerical simulations and, consequently, it's impact on the device characteristics is not discussed. Fig. 2a presents in a 3D plot the extracted V_K dependence on V_G and V_D voltages (V_S and V_B are grounded). It is clearly demonstrated that V_K<7V for the whole bias domain. The extracted V_K value is then used to distinguish between: the operation region of the intrinsic MOS and the voltage drop on the extended drift region. Figs. 2.b and c depict the detailed $V_K(V_D)$ and $V_K(V_G)$ variations. It is clear that, in a first approximation, the V_K potential is expected to rise up with V_D, which drives the transistor from linear to saturation (Fig. 2.b) and also with V_G, which raises the surface potential (Fig. 2.c). An interesting result is that V_K appears to decrease with V_G after reaching a maximum at constant V_D (see Fig. 2.c). The analysis of the 2D simulated structures shows that this maximum corresponds to a pinch-off of depletion regions in the drift (the current is then forced through a depletion zone), Fig. 3. A higher V_G avoids this pinch-off and can even generate a local accumulation or carrier injection in the substrate near drift region bird's beak, which explains the V_K reduction with V_G after reaching the maximum.

The particular characteristic of the LDMOS transistor is the formation of a long accumulation channel in the n-region under the thin oxide, which is V_G- and V_D-controlled. The accumulation channel can impact the equivalent length of the intrinsic transistor (especially for short-channels).

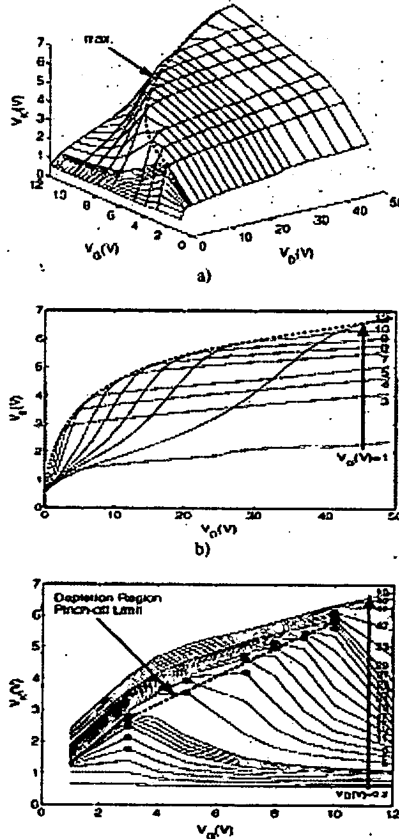


Fig. 2. L-DMOS channel voltage variation function of V_G and V_D: a) overall 3-D representation, b) V_K vs. V_D with V_G as a parameter and c) V_K vs. V_G with V_D as a parameter.

IV. ANALYSIS OF SATURATION MECHANISMS

Simulated output characteristics of the intrinsic and extrinsic lateral DMOS

418

transistors are reported in Figs. 3 a and b. The quantitative investigation of V_K at high V_D allows to distinguish between the following saturation mechanisms, Fig. 3.b. At low V_G values (<4V) the saturation is controlled by the intrinsic channel pinch-off (region I); then, when V_G is increased, the current saturates due to carrier velocity saturation in the intrinsic MOS (region II). As a result, the (quasi-) saturation current becomes an almost linear function of V_G as it can be seen in Fig. 3b for V_G=7, 8, 9 and 10V. Note that, for increased V_D, velocity saturation or pinch-off in the drift can also be superposed. Region III is characterized by an intrinsic transistor operating in the quasi-linear region with an accumulation channel in the drift and a J-FET like saturation control.

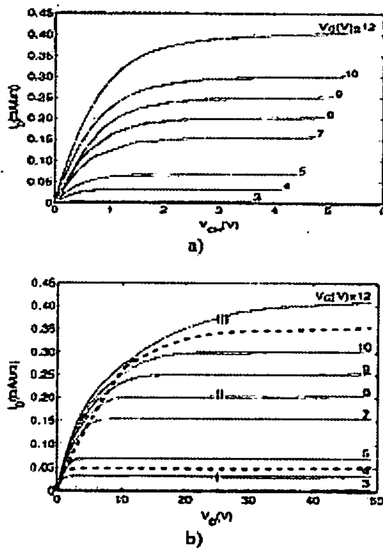


Fig.3. LDMOS (L=1□m) output characteristics: a) intrinsic transistor and b) extrinsic transistor. Region I – intrinsic MOS pinch-off, II – intrinsic MOS carrier velocity saturation, III – drift velocity saturation.

V. DRAIN RESISTANCE EXTRACTION METHOD

The previous analysis demonstrates that V_K is very useful to capture some LDMOS physical phenomena. However, in practice, this voltage is not accessible for measurements. In the following, we propose a method, which deals with the extraction of the drift series resistance, R_D. The value of this resistance is useful for both the accurate modelling of $I(V_G, V_D)$ characteristics and for evaluation of $V_K(=V_D - R_D I_D)$. The proposed $R_D(V_G,V_D)$ extraction method consists in two main successive steps. First the drain resistance at low drain voltage, R_{D0}, with the gate bias as a parameter, is evaluated. Asymmetric R_S and R_D series resistances are expected to differently impact the related gate and drain de-bias if the extrinsic transistor is measured successively in forward (i.e. normal) and reversed (source and drain interchanged) configurations, Fig. 4.a and b. An identical constant drain current is injected in forward and reversed configuration while recording the V_{Df} and V_{Dr} drain voltages as functions of V_{Gf} and V_{Gr}, respectively. As a consequence, supposing $R_S \ll R_D$, the drain series resistance is then calculated based on the difference between the gate voltages which ensure in forward and reverse modes identical extrinsic drain voltages, $V_{Df}=V_{Dr}$, with the MOS transistor in quasi-linear operation:

$$R_D \cong R_D - R_S = \frac{V_{Gr} - V_{Gf}}{I_D(1 + dV_T/dV_{SB})} \quad (1)$$

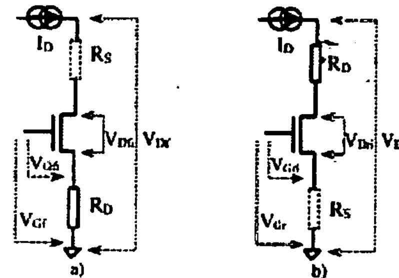


Fig. 4. Experimental setup: a) forward and b) reversed source and drain, measurements dedicated to R_{D0} extraction.

The second step is the adaptation of Otten's method [3] to evaluate the drain resistance derivative with respect to the drain voltage

dR_D/dV_D at constant gate voltage. Finally, the drain series resistances is evaluated as:

$$R_D(V_D, V_G) = R_{D0}(0, V_G) + \int_0^{V_D} \frac{\partial R_D}{\partial V_D} dV_D \quad (2)$$

For the extraction procedure, an experimental reconstruction of the quantitative derivative dR_D/dV_D was proposed, by the use of a variable resistor in the drain of the LDMOS transistor. With the extrinsic (measured) output conductance given by [4]:

$$g_d^{-1} = \frac{1 + g_d(R_D + R_{Dadd}) + (g_{mi} + g_{bin})R_S}{g_{di}(1 - \partial I_D / \partial V_D)} \quad (3)$$

where superscript 'i' applies for the intrinsic transistor (see Fig. 4), it follows that the slope of dg_d^{-1}/dR_{Dadd} versus R_{Dadd} plot can be used for the dR_D/dV_D extraction according to:

$$\frac{dR_D}{dV_D} = \frac{1 - \partial g_d^{-1} / \partial R_{Dadd}}{I_D}$$

A very good agreement between the numerical simulation, and experimental results using our method, is demonstrated in terms of both $R_D(V_G, V_D)$ and its derivative, dR_D/dV_D (even for the particular dependence reported at very low V_D) (Fig.5).

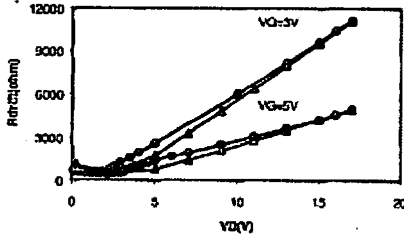


Fig. 5. Drift resistance, R_D=Rdrift, versus drain voltage, V_D (circles - measure, triangles - TCAD simulation).

An important remark is that all specific physical effects, located in the drift zone, affect the MOS intrinsic bias, if the current continuity equation is fulfilled. It follows that, the quasi-saturation phenomena for LDMOS device can be modelled using an adapted BSIM3v3 model for the intrinsic MOS device and a scalable resistance for the drift zone (Fig. 5). It is worth noting that every (VG, VD) couple has a correspondent Rdrift=R_D value. Thus, for every data point of ID(VD) characteristics a separate simulation has to be run. Despite this time consuming process, a very good fit can be obtained between the TCAD characteristics and BSIM3v3 adapted model (Fig. 6).

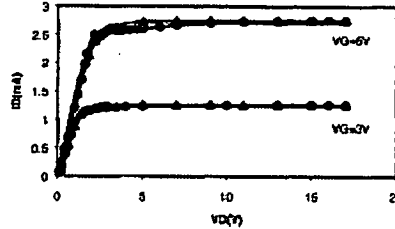


Fig. 6. LDMOS output characteristics: solid line - TCAD simulation, circles - BSIM3v3 with experimentally extracted R_D, triangles - BSIM3v3 model with R_D from numerical simulation.

VI. CONCLUSION

A new concept, the intrinsic drain voltage, was proposed for high voltage MOSFETs. An extraction method for the drift resistance was presented and the results were compared with TCAD simulations. The method is useful for the development of analytical models for voltage-controlled series resistances in HV MOSFETs since it allows their pure experimental evaluation. Its usefulness for the investigation of (quasi-) saturation mechanisms has been demonstrated.

ACKNOWLEDGEMENT

This work was supported by the IST-1999-12257 Automacs project.

REFERENCES

[1] Y.-S. Kim, J. Fossum, "New Physical Insights and Models for High-Voltage LDMOS IC CAD", *IEEE Trans. Electron Devices*, vol. 38, pp. 1641-1649.
[2] J. Jaejune, T. Arnborg, Yu. Zhiping, R.W. Dutton, "Circuit model for power LDMOS including quasi-saturation", *Proceedings of SISPAD '99*, pp.15-18.
[3] Jan A. M. Otten and F. M. Klaassen, IEEE Trans. El. Dev., Vol. 43, p. 1478, 1996.
[4] A. Ortiz-Conde, J.J. Liou, W. Wong and F.J. Garcia Sanchez, Electronics Letters, Vol. 30, No. 12, p. 1013, 1994.

420

Universal Test Structure and Characterization Method for Bias-Dependent Drift Series Resistance of HV MOSFETs

C. Anghel
N. Hefyene
A. Ionescu
costin.anghel@epfl.ch
EPFL-STI-IMM-LEG
CH-1015 Lausanne
Switzerland

S.F. Frère
R. Gillon
J. Rhayem

Alcatel Microelectronics, Westerring 15,
Oudenaarde, Belgium

Abstract

A simple, fast and accurate characterization method dedicated to the evaluation of bias-dependent drift resistance of the HV MOS transistors is presented. The procedure relies on a novel test design structure that gives direct information about the impact of the drift zone on the overall HV MOSFET characteristics. Intrinsic (MOS channel) and extrinsic (including drift region) characteristics, obtained by adapted measurements, are used for parameter extraction and physical effects identification. For the first time the variation of the drift resistance from room temperature up to 150°C is extracted. Very good performance when combining a BSIM3 V3 low voltage model with a drift resistance quasi-empirical model is reported.

1. Introduction

High-Voltage MOSFETs are key components for smart power, RF and automotive integrated circuits. The most versatile HV architecture is the Extended Drain MOSFET (XDMOS) and one of its most critical issues is the on-resistance, R_{on}. Major advances in the design and modelling of these devices are related to the accurate evaluation of their bias-dependent drift series resistance, R_{drift}, critically dependent on the design of the extended drain region, which impacts the HV performance. Especially, the quantitative comparison of R_{on} with the drift resistance, R_{drift}, is valuable insight for HV design. Moreover, R_{drift} bias-dependence on drain, V_D, and gate voltage, V_G, appears to be the origin of the so-called quasi-saturation phenomena that were subject of many reports, physical analysis and controversy last years [1-3].

2. Novel Test Structure

We report a new, universal test structure, called MESDRIFT, and the associated characterisation that are able to accurately provide the bias-dependent drift series resistance without any prior information about the detailed technological architecture of the drain extension.

The proposed MESDRIFT structure (designed by Alcatel Microelectronics) is depicted in Fig. 1: it simply reproduces the 100V n-channel extended drain X-DMOS device architecture in a dedicated test structure, with the key difference that a small contact is smartly engineered in the drift region, near the end of the MOS channel. This contact is dedicated to probe the intrinsic drain voltage, V_K, without any significant impact on the electrical characteristics.

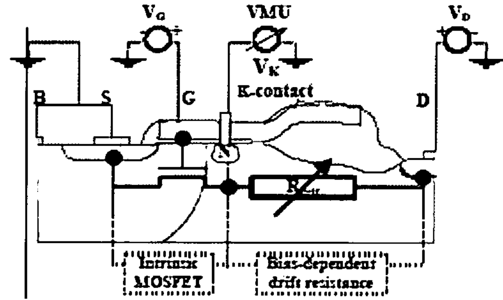


Fig. 1 MESDRIFT structure: cross section and measurement setup.

3. Experiment

3.1 Validation of the test structure

In order to validate the MESDRIFT structure, its transfer and output characteristics were measured and compared with identical measurements performed on the original device (fig.2). Although, the breakdown of the MESDRIFT structure shifts down in comparison with the original one (due to the n^+ implant in the proximity of the metallurgical pn junction) the measured characteristics present no significant change for low and medium drain voltage values. Consequently, the drift region with drain and source biased can be observed for the whole analogue voltage domain.

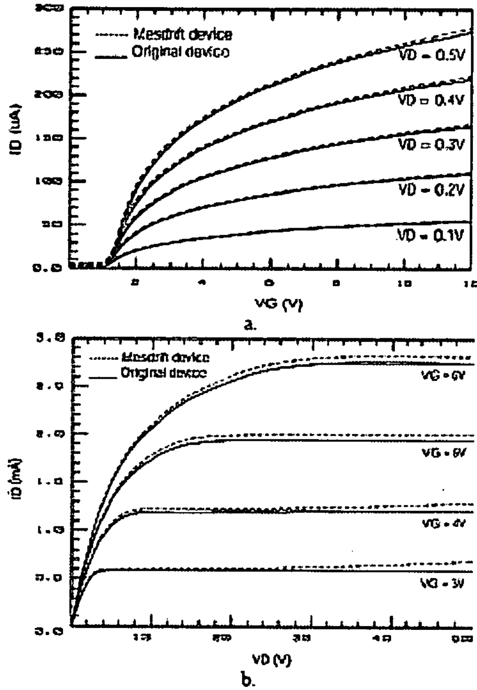


Fig. 2 Comparison between MESDRIFT (dashed) and real device (solid) a) transfer characteristics, I_D-V_{GS}; b) output characteristics, I_D-V_{DS}.

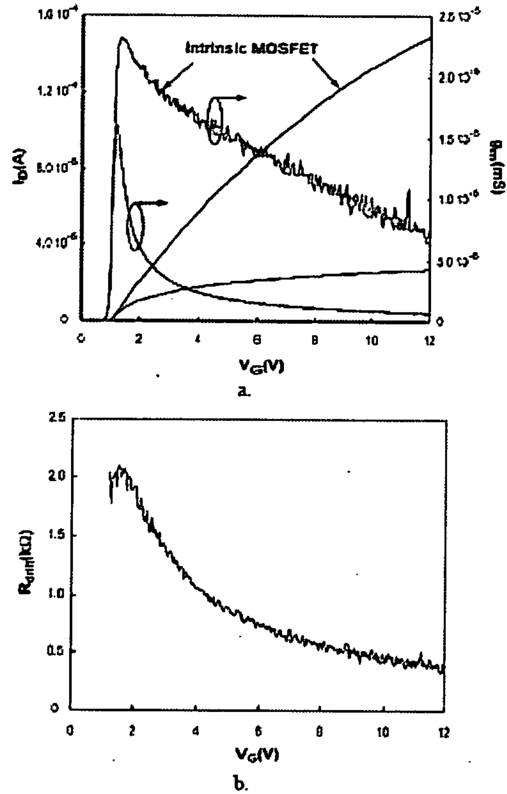


Fig. 3 a) Intrinsic and extrinsic X-DMOS I_D-V_G and g_m-V_G at identical drain-to-source voltage: V_{Dint}=50mV and V_D=50mV, respectively. b) Extracted R_{drift} vs. V_G at low V_D (=50mV).

3.2 Measurement of the intrinsic channel and drift region characteristics

The most interesting feature of this test device is the ability of measuring both intrinsic MOS characteristics and extrinsic high-voltage device characteristics. Fig. 3 (a) shows the comparison of the I_D-V_G characteristics of the intrinsic and extrinsic devices at same low drain voltage; the lower g_m of the extrinsic device is explained by the effect of the series connected R_{drift}. Based on the difference between the coefficients of mobility reduction with the transverse field in intrinsic and extrinsic channels, the series bias dependent R_{drift} given in Fig. 3b, is calculated using the expression [4]:

$$R_{drift} = \frac{\theta_{gext} - \theta_{gint}}{(W/L)C_{ox}\mu_0},$$

were θ_{gext} and θ_{gint} are the extrinsic and intrinsic mobility reduction coefficients with transverse electrical field respectively, μ_0 is the low-field mobility and C_{ox} the oxide capacitance [F/cm²].

However, this extraction is limited to low drain voltage (linear operation) and is time consuming since the intrinsic I_D-V_G needs a constant V_K.

The V_K dependence on the XDMOS gate and drain biases is shown in Fig. 4a. Bias dependent resistance $R_{drift}(V_G, V_D)$, is calculated based on the drift voltage drop, (V_D-V_K), at a given injected drain current, I_D.

For the first time, the experimental R_{drift} variation with the device bias is detailed over full operation range (see Fig. 4b, T=25°C). The reported two-decade variation of R_{drift} can be explained by the depletion region extension according to the gate and drain voltage control (Fig. 5). The formation of an accumulation layer at high V_G contributes also significantly to the reported R_{drift} variation. Based on V_K, by numerical simulation it was possible to distinguish quasi-saturation reflecting JFET-like modulation in the drift or carrier velocity saturation (at high V_G) without saturation of the intrinsic channel [5]. Experiments conducted on MESDRIFT have confirmed these quasi-saturation mechanisms. Moreover, as shown later, it can be used for development of new models.

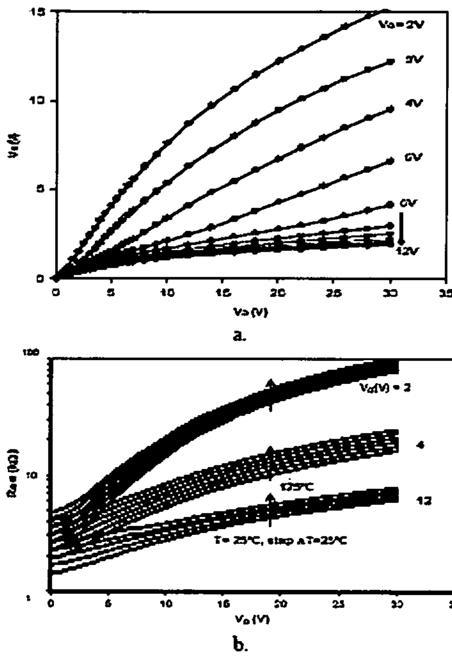


Fig. 4 Experimental data obtained with MESDRIFT: a) V_K vs. V_D with V_G as parameter. b) R_{drift} vs. V_D with V_G and T as parameters.

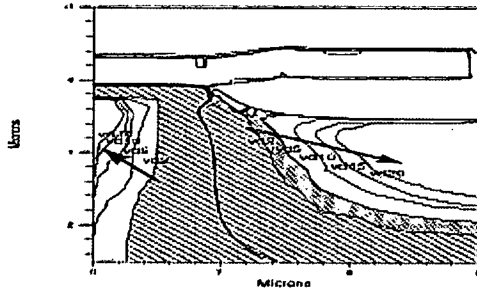


Fig. 5 2D numerical simulation of depletion region extension in the drift when V_D is increased, at constant $V_{GS}(=3V)$. Depletion pinch-off is obtained for $4V<V_D<5V$

Fig. 6 shows one useful analysis supported by MESDRIFT: the ratio between R_{drift} and R_{on} ($=R_{ch}+R_{drift}$) in XDMOS operation is depicted versus V_D at constant V_G. It appears that in analogue operation, R_{ch} dominates (or, at lest is comparable with) R_{on} and it's key for modelling to accurately describe the intrinsic channel. When V_G and/or V_D are slightly increased (>5V), R_{on} starts to be dominated by the R_{drift} and for V_G>4V and V_D>5V, the R_{ch} contribution is less than 30% of R_{on}.

In order to characterize the X-DMOS DC behaviour over extended temperature range (25°C up to 150°C), while monitoring the evolution of the main parameters of the intrinsic MOSFET (threshold voltage, mobility, subthreshold swing, etc.) we have also extracted R_{drift} vs. temperature (Fig. 4b) and found that the temperature (up to 150°C) does not impact significantly the R_{drift}/R_{on} ratio (Fig. 6b).

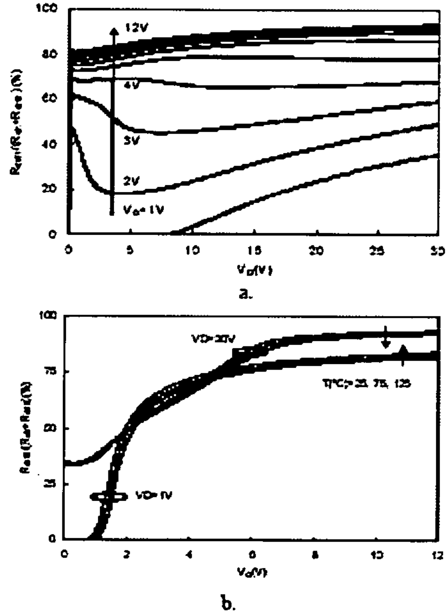


Fig. 6 a) R_{drift}/R_{on} vs. V_D with V_G as a parameter, at T=25°C. b) R_{dr}/R_{on} vs. V_G with V_G and T as parameters.

4. Model Calibration and Performances

A simple two-step procedure has been established to build a model using the information provided by MESDRIFT structure. First, the BSIM3V3 model parameters are calibrated with the intrinsic transfer and output characteristics. Drift resistance variation, experimentally revealed by MEASDRIFT, is then used to tune an empirical expression for the simulation of the drift resistance:

$$R_D = R_{D0} + A\ln[\exp(B \cdot V_D + C) + 1]$$

were R_{D0} resistance and A, B, C coefficients are function of V_G. The detailed modelling expression is elsewhere [6].

By combining these two modules the characteristics of the global device are simulated. The results are compared with the measured data for the overall voltage domain (Fig. 7 and 8). Very good agreement results are obtained from subthereshold region up to medium gate voltages (Fig. 7 a and b). The current is slightly

overestimated for high gate voltages. One important aspect concerns the ability to simulate the transconductance and, especially its peak value. Results in fig. 7c, reveal remarkable match between measurement and simulation in terms of g_m. Very good model accuracy (max err.<20%) was obtained also for quasi-saturation, which is highlighted on the output characteristics of X-DMOS (Fig. 8).

Note that the model has been tuned on experimental data that are subject to self-heating (especially for high V_D); even better results are expected when tuning the drift model on pulsed measurements. It turns out that the simultaneous yet separate calibration of the intrinsic MOSFET and the drift region appears to be a unique way to accurately model the XDMOS and its temperature dependence, with physical values of electrical parameters.

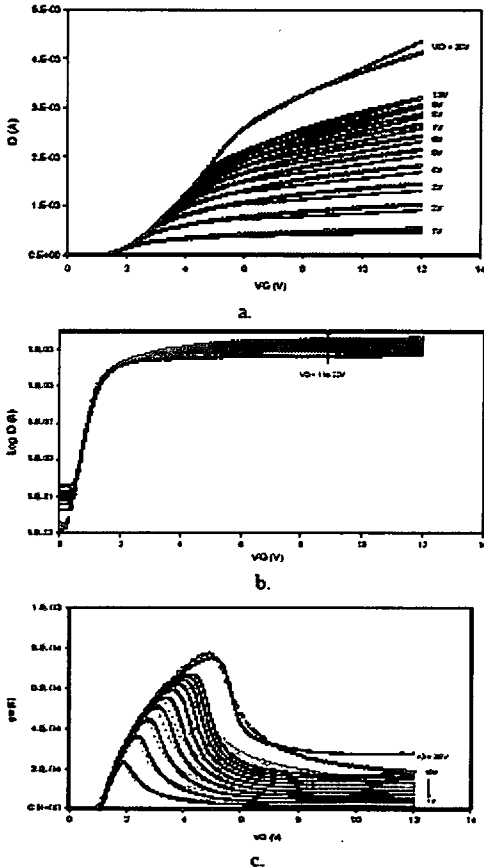


Fig. 7 Transfer characteristics: dashed line – measured data; solid line – BSIM3V3 with variable resistor a) $I_D(V_G)$; b) log $I_D(V_G)$; c) $g_m(V_G)$

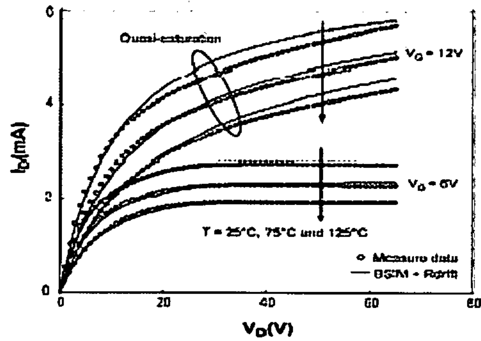


Fig. 8 XDMOS output characteristics: dashed – measured data; solid – BSIM3V3 with variable resistor

Conclusion

A new experimental test structure MESDRIFT and the related characterisation method that provide access to the drift resistance as function of gate and drain bias are proposed. The method is simple, accurate and universal as it is independent on the drift architecture of the investigated HV MOSFET. The use of MESDRIFT provides immediate results for R_{drift} in contrast with all existing extraction procedures, which are time-consuming and need extra computation. Very accurate modelling is obtained with a low voltage BSIM 3V3 for intrinsic MOS transistor and an empirical expression for the drift resistance, calibrated on MESDRIFT characteristics.

Acknowledgements

This work was supported by the IST-1999-12257 Automacs project.

References:

[1] Trivedi, M.; Khandelwal, P.; Shenai, K. Electron Devices, IEEE Transactions on , Vol. 46, 1999, pp. 1794 – 1802.

[2] Jaejune Jang; Amborg, T.; Zhiping Yu; Dutton, R.W., SISPAD '99. 1999, pp. 15 – 18.

[3] Kreuzer, C.H.; Krischke, N.; Nance, P., IEDM, 1996, pp. 489 – 492.

[4] Ghibaudo G., Electron Lett 24 (9): 543-545 APR 28, 1988

[5] Anghel C., Hefyene N., Ionescu A.M., Frere S., Gillon R., Vermandel M., Bakeroot B., Doutreloigne J., Maier C., Mourier Y., ESSDERC 2001, Nuremberg, Germany, Proc. of, pp.399-402, Sep. 2001.

[6] N. Hefyene, E. Vestiel , S. Frere, C. Anghel, A.M. Ionescu, R. Gillon submitted to SISPAD 2002

EKV Compact Model Extension for HV Lateral DMOS Transistors

N. Hefyene [(1)], J. M. Sallese [(1)], C. Anghel [(1)], A. M. Ionescu [(1)], S.F. Frère [(2)] and R. Gillon [(2)]
(1) Ecole Polytechnique Fédérale de Lausanne, EPFL, STI-IMM-LEG,
CH-1015 Lausanne, Switzerland;
(2) Alcatel Microelectronics, Westerring 15, Oudenaarde, Belgium

This paper reports for the first time on the extension of the EKV compact model for High-Voltage (HV) MOSFETs. A continuous expression is derived for the drift bias-dependent resistance of DMOS transistors and then validated in different operation regions (in linear and saturation regimes). When combined with EKV, the proposed new drift model provides very accurate DC modeling including quasi-saturation.

1. Introduction

Analytical modeling of high voltage lateral DMOS transistors has been still subject to particular interest, due to their compatibility with planar CMOS technologies as well as their versatility for automotive and RF applications. Many researches and studies were dedicated to model HV DMOS taking into account the specific physics and phenomena associated to the extended drain region architecture, such as the quasi-saturation mechanisms [1, 2].

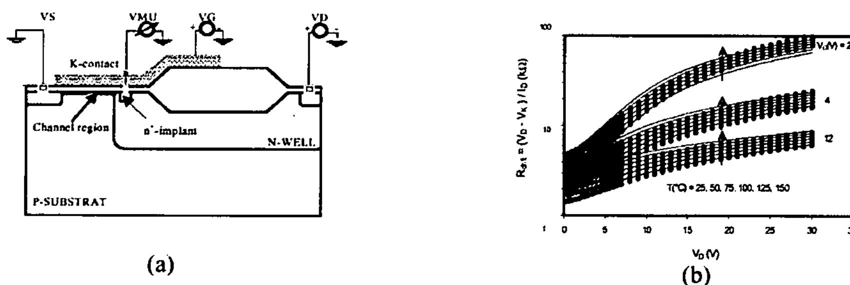
2. Test Structure for Model Validation

The investigated HV test structure is an n-channel non self-aligned drain-extended DMOS (X-DMOS) transistor; fabricated with the 0.7µm CMOS process I^2T technology of Alcatel Microelectronics (Fig. 1 a). Such architecture delivers a drain capability up to100V.

Recently, we have reported on the interest in monitoring the intrinsic drain voltage of HV DMOS transistors [3]. The proposed model needs, for full validation, access to measure this key potential (V_K). In order to experimentally measure V_K in such devices, some of the structures were designed with a small n^+-*implant* added at the end of the intrinsic drain location, of the intrinsic drain location, called *K-contact* [4]. The n^+-contact is engineered in a way that does not alter the global characteristics of the test structures compared with the original devices.

3. Extended Drift Region Modeling

The interest in modeling the bias-dependent drift resistance, $R_D(V_G,V_D)$, comes from the fact that most of the complex 2D phenomena in HV DMOS transistors, like quasi-saturation, are dictated by the drift region architecture. Using a HP4156 parameter analyzer, the K-contact potential (V_K) was monitored with the high impedance voltmeter, while varying the V_D and V_G in all regimes of transistor operations.



Figs. 1. (a) Illustration of the n-channel X-DMOS test structure and the added n^+-implant location (K-contact); (b) $R_D(V_D,V_G,T)$ characteristics of n-channel X-DMOS test structure: experiment (symbols) compared with quasi-empirical expression, (solid line, eq. 2) for various temperatures.

The bias-dependent drift resistance was extracted according to:

$$R_D \equiv R_{drift} = (V_D - V_K) / I_D \tag{1}$$

A continuous quasi-empirical mathematical expression is proposed to model the extracted drift resistance [5]:

$$R_D(V_D, V_G, T) = \left(r_{D0} + \frac{r_{D1}}{(\gamma V_G + 1)} \ln\left(e^{(\beta_1 V_G + \beta_0) V_D - (\delta_2 V_G^2 + \delta_1 V_G + \delta_0)} + 1 \right) \right) \cdot \left(\frac{T}{T_0} \right)^{\left(\frac{1}{m V_D + n} \right)} \tag{2}$$

where r_{D0}, r_{D1}, γ, β_1, β_0, δ_2, δ_1 and δ_0 are room temperature (T_0) model parameters, while m and n include the temperature dependence. Fig. 1 b, illustrates the typical accuracy that can be achieved with the new proposed expression (eq. 2), compared with experimentally extracted $R_D(V_G, V_D, T)$.

4. Transistor Modeling Approach with EKV

The inspection of the K-contact potential demonstrates that the V_K potential of the HV X-DMOS transistor remains at low voltages (<10V), independent on the applied voltage on the drain ($V_{DS} < V_{DSBR}$). This was predicted by numerical simulations, with the intrinsic drain voltage concept proposed in [3]. Thus, the intrinsic MOS channel can be modeled as a low-Voltage MOSFET. In our modeling approach with the EKV compact model, the subscripts "*K*" and "*D*" denote respectively any quantities associated to the "*intrinsic*" and "*extrinsic*" drain of the device (e.g. V_K and V_D).

According to the EKV model (long-channel approximation) [6], the normalized drain current (i) can be expressed as the difference between the *forward* (i_f) and *reverse* (i_r) current:

$$i = I_D / I_0 = i_f - i_r \tag{3}$$

where: $$i_{f(r)} = q_{S(K)}^2 - q_{S(K)} \tag{4}$$

and $I_0 = 2\, n\, C_{ox}\, \mu_0 U_t^2\, (W/L)$, is the *specific EKV current*. In terms of potentials [7], $q_{S(K)}$ is given by:

$$q_{S(K)} = -\left(\left((V_P - V_{S(K)}) / 2U_t \right) - \frac{1}{2} \ln(-q_{S(K)}) \right) \tag{5}$$

where V_P, the *pinch-off voltage*, is defined as: $V_P = [V_G - V_{T0}] / n(V_P)$.

The charge expression (5) is valid from weak to strong inversion regions and has an implicit form. Thus it can only be solved numerically. In the case when only strong inversion is considered, eq (5) can be simplified by neglecting the logarithmic term:

$$q_{S(K)} \cong -\left((V_P - V_{S(K)}) / 2U_t \right) \tag{6}$$

With this late simplified expression, eq (4) becomes:

$$i_{f(r)} \approx \left((V_P - V_{S(K)}) / 2U_t \right)^2 + \left((V_P - V_{S(K)}) / 2U_t \right) \tag{7}$$

where V_K is the intrinsic potential and as defined in EKV, $n(V_P) = 1 + \gamma / 2\sqrt{2\phi_F + V_P}$, is the *slope factor* and $\gamma = \sqrt{2\, q \epsilon_0 \epsilon_{si} N_{Sub}} / C_{ox}$ is the *body* or *substrate factor*. Combining eq (1), (2), (3), (4) and (6), with V_S = 0V, the drain current can be simply formulated as:

$$I_D \approx I_0 \left(\left(\frac{V_P}{2U_t} \right)^2 + \left(\frac{V_P}{2U_t} \right) - \left(\frac{V_P - V_D + I_D R_D(V_D, V_G)}{2U_t} \right)^2 + \left(\frac{V_P - V_D + I_D R_D(V_D, V_G)}{2U_t} \right) \right) \tag{8}$$

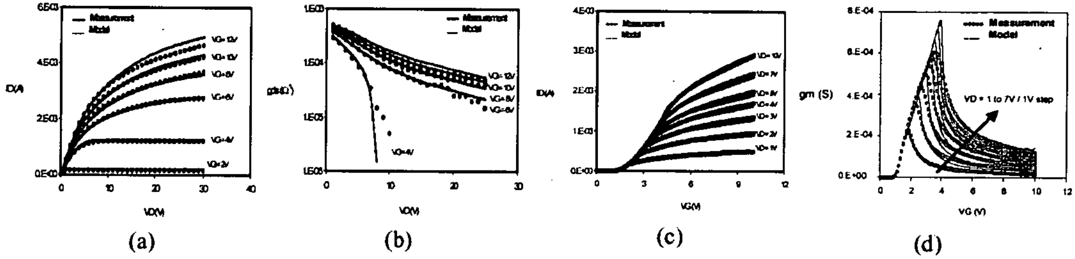
In saturation (i.e. for $V_D > V_P$), the reverse current, i_r, becomes negligible compared to the forward current, i_f, and the drain current simply reduces to the forward term [6]:

$$I_D sat \approx I_0 \left(\left(\frac{V_P}{2U_t} \right)^2 + \left(\frac{V_P}{2U_t} \right) \right) \tag{9}$$

One can observe that eq (8) has the form of a 2nd order polynomial, $f(I_D) = a \cdot I_D^2 + b \cdot I_D + c$ where *a*, *b* and *c* are constant terms for each combination of applied extrinsic voltages, and thus, can be *analytically* solved.

5. Model Validation on Silicon

Measurements have been carried out on a long-channel transistor (n-channel X-DMOS, $L_{ch} = 4$ µm), in order to fulfill the EKV long-channel approximation. Figs. 2, show measured standard DC characteristics performed at room temperature and fitted with proposed drain current expressions, eq (8) and (9). Very good fitting can be observed, especially in the analogue region, where the self-heating is not excessively pronounced (i.e. V_D and V_G up to 30V and 10V respectively).



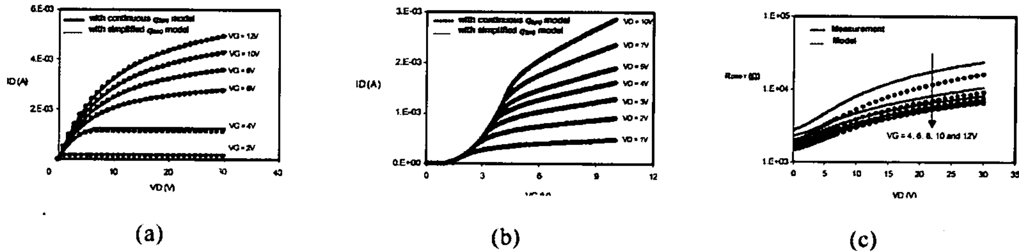
(a) (b) (c) (d)

Figs. 2. Measured and calculated extrinsic (a) I_D-V_D, (b) gds-V_D, (c) I_D-V_G and (d) gm-V_G characteristics on a standard n-channel X-DMOS test device (no K-contact) at room temperature.

6. Global Modeling Strategy

The proposed strategy relies essentially on the simplified expression of the drain current, eq (8), which has the advantage to be an explicit expression and only depends on external biasing voltages V_S, V_D and V_G. First, we show that with the simplified eq (8) one can deduce the bias-dependent drift resistance based on the drain current, I_D. Figs. 3 a and b demonstrate, as expected, that the simplified $q_{S(K)}$ expression doest not impact the model accuracy in strong inversion. Based on eq (8), the drift resistance is calculated as the solution of a 2nd order polynomial equation:

$$R_D(V_G, V_D, T) = f[V_D, V_P(V_G), I_D] \qquad (10)$$



(a) (b) (c)

Figs. 3. Modeled drain current: (a) output and (b) transfer characteristics using complete vs. simplified $q_{S(K)}$ expressions, eq (5) and (6) respectively; (c) $R_D(V_G,V_D)$ characteristics: analytically extracted, according to eq (10), vs. Measured on device at room temperature.

By considering I_D in eq (10) a measured quantity (i.e. output characteristics), eq (8) can be re-formulated in a polynomial form, $F(R_D) = AR_D^2 + BR_D + C$, where A, B and C depend on known quantities (i.e. V_G, V_D and measured I_D). Through this polynomial expression, the bias-dependent drift resistance, R_D, can be analytically solved. Good agreements, between experimentally measured and analytically extracted R_D (V_G, V_D) characteristics are illustrated in Fig. 3 c, confirming the validity of our approach.

In order to extend the drain current model to moderate and weak inversion, eq. (5) is finally used instead of eq. (6).

The modeling is sequenced as following: (i) perform standard extrinsic I-V measurements of the HV DMOS transistor; (ii) extraction of the low-field mobility, μ_0, and threshold voltage, V_{T0}, parameters with a dedicated method [8]; (iii) calculation of R_D (V_G, V_D) characteristics in strong inversion using the measured I_D according to eq (10); (iv) fit with the drift expression, eq (2), the calculated drift-resistance in (iii); (v) optimization of the set of deduced V_{T0}, μ_0 and drift parameters to fit the desired DC measured characteristics over all regions of operations.

Even if one could rise the drawback of an empirical mathematical formulation of the drift region, it should be mentioned that the proposed strategy has some essential advantages: (i) can be applied to any asymmetric MOSFET with any bias-dependent drift series resistance (an appropriate selection of the mathematical function for $R_D(V_D,V_G)$ is however needed), (ii) a special test device (i.e. with a K-contact) is no longer needed, (iii) easy extraction of low field mobility and threshold voltage and (iv) needs only few I_D-V_D measures at various V_G to extract and fit the empirical drift parameters.

7. Conclusion

An extension of the compact EKV model dedicated to HV DMOS devices is proposed based on the separated modeling of the drift resistance, specific to HV MOSFETs. It is shown that EKV modeling eliminates the need of a dedicated test structure to experimentally allow access to the intrinsic drain voltage, V_K.

A simple modeling and parameter extraction strategy dedicated to HV Lateral DMOS transistors with bias-dependent drain series resistance, is presented. This methodology requires only a few of basic measurements on standard devices. The good agreement between simulations and measurement results open the field to further developments, such as including the high electrical field-effects and temperature dependence.

Acknowledgements

This work was supported by the IST-1999-12257 'Automacs' EC project and the Swiss OFES no. 00-0009.

Many thanks are due to Sergio Pesenti, for his programming support.

References:

[1] J. Jang, T. Amborg, Y. Zhiping and R. W. Dutton, SISPAD 1999 Proc., Sep. 1999, pp. 15-18.
[2] R. Zhu and T.P. Chow, ISPSD 1998 Proc., June 1998, pp. 343-346.
[3] C. Anghel, N. Hefyene, A.M. Ionescu, S. Frere, R. Gillon, M. Vermandel, B. Bakeroot and J. Doutreloigne, C. Maier, Y. Mourier, ESSDERC 2001 Proc., Sep. 2001, pp.399-402.
[4] C. Anghel, N. Hefyene, A.M. Ionescu, S. Frere, R. Gillon and J. Rhayem, ESSDERC 2002, unpublished.
[5] N. Hefyene, E. Vestiel , S. Frere, C. Anghel, A.M. Ionescu, R. Gillon, SISPAD 2002, unpublished.
[6] Ph. D. these of M. Bucher, Lausanne, EPFL 2000.
[7] J. M. Sallese and A. -S. Porret, Solid-State Electronics, 44(2000): 887-894, appendix A.
[8] Ghibaudo G., Electron Lett 24 (9): 543-545 Apr 28, 1988.

ELECTRICAL CHARACTERIZATION AND MODELLING OF HIGH-VOLTAGE MOSFETS WITH MESDRIFT

C. Anghel[1], N. Hefyene[1], Z. El-Kihal[1], S. Frere[2], R. Gillon[2], M. Tack[2], A.M. Ionescu[1], M.J. Declercq[1]
B. Bakeroot[3], M. Vermandel[3] and J. Doutreloigne[3]
[1]Swiss Federal Institute of Technology Lausanne, Electronics Laboratory, Switzerland
[2]Alcatel Microelectronics, Oudenaarde, Belgium, [3]ELIS-TFCG/IMEC, University of Gent, Belgium

Abstract
This work reports on a new test structure, called MESDRIFT, which essentially allows the *separate* investigation of the *intrinsic channel* and *drift* regions of any type of asymmetric high-voltage (HV) DMOS transistor, without altering the overall device characteristics. Its usefulness in terms of electrical characterization and device modelling, including: (i) *static characteristics* (analysis of quasi-saturation phenomena), (ii) *temperature dependence*, (iii) *self-heating*, (iv) *bias-dependent capacitance* (AC regime) and (v) hot carriers, is demonstrated.

Introduction - With high-voltage (HV) MOSFETs as key components for smart power, RF and automotive, the most versatile HV MOSFET architecture is still the Lateral HV MOSFET (DMOS) [1-5]. Among the most critical issues for accurate design, modelling and simulation are the bias-dependent characteristics of the drift region and their impact on the overall transistor behaviour. Especially, the *bias-dependent drift resistance* (origin of *quasi-saturation* phenomena) and the C_{GS} and C_{GD} *capacitances* appear to be source of crucial interest for modelling and characterization. This paper addresses the modelling and electrical characterization of any generic DMOS device via use of a dedicated structure, called MESDRIFT. It is shown that MESDRIFT can provide extremely useful information about temperature influence, self-heating and hot-carrier stress, which are major concerns for DMOS transistors in terms of the identification of the Safe Operation Area (SOA). Both 2D numerical simulations and experiments are correlated to draw and support key conclusions.

MESDRIFT: device, DC experiments and numerical simulations - The MESDRIFT structure and the DC measurement set-up are depicted in **Fig. 1.** MESDRIFT simply reproduces the architecture of a HV n-channel extended drain transistor (called X-DMOS, fabricated in 0.7μm CMOS, with 100V capability, addressed in detail in this work), with the key difference that a small contact is smartly engineered in the drift region, near the end of the MOS channel. Similar structures have been fabricated for more conventional L-DMOS architectures. This K (key) contact is designed for probing *the intrinsic drain voltage*, V_K (at the end of the intrinsic channel), without significant impact on the electrical characteristics of the overall HV MOS device. As demonstrated in **Fig. 2**, this is successfully achieved when the device width, W, is much larger than the size of the K-probe contact: $W \gg W_K$. **Fig. 3 (a)** depicts the I_D-V_G characteristics of the intrinsic and extrinsic MOS devices at same equivalent drain voltage ($V_D=V_K$) that captures the effect of the drift bias-dependent series resistance, R_{drift}, on DC characteristics. At low drain voltage and uniquely based on the difference between the coefficients of mobility reduction with the transverse field in intrinsic and extrinsic channels, the R_{drift} is deduced, **Fig. 3 (b)**. For extended analysis over all operation range (including *quasi-saturation*), the V_K dependence on external V_G and V_D, is presented in **Fig. 4**. The overall $R_{drift}(V_G, V_D)$, given in **Fig. 5** is extracted based on the drift voltage drop, $V_{drift}=V_D-V_K$ at a given injected drain current, I_D. Thus, for the first time, the experimental R_{drift} variation with the device bias is *experimentally* accessible over full operation range and its two-decade reported variation is explained by the drift depletion control by V_G and V_D, and by the formation of an accumulation layer under the extension of the thin oxide. Numerical simulation (**Fig. 6**) has been used to extensively validate the results obtained with MESDRIFT; very good qualitative agreements are obtained and some quantitative higher V_K for fabricated MESDRIFT corresponds to a non-zero distance between the K-contact and the end of the intrinsic channel. Based on V_K investigation of X-DMOS, we have distinguished quasi-saturation (see **Fig. 7**) reflecting JFET-like modulation in the drift (region II of **Fig. 7**) or carrier velocity saturation (region III of **Fig. 7**) without saturation of the intrinsic channel, and, identified precisely the pinch-off points of depletion in the drift (**Fig. 8**). Similarly, the physics of L-DMOS quasi-saturation has been clarified. **Fig. 9** shows an original finding provided by MESDRIFT: the balance between R_{drift} and R_{on}. It appears that in *analogue* operation (low V_D and V_G), R_{ch} and R_{drift} are comparable, while when V_G and/or V_D increase (>5V), R_{on} is dominated by R_{drift}. This enlightens how critical is the accuracy needed on R_{drift} extraction and/or modelling for HV DMOS devices.

DMOS temperature dependence with MESDRIFT - The MESDRIFT behavior has been investigated from 25°C up to 150°C, by monitoring the evolution of key parameters of the intrinsic MOSFET (threshold voltage, low field mobility, subthreshold swing, etc.), **Figs. 10** and **11**. Typical signatures of DMOS transistors in terms of the temperature coefficients of mobility, $n \cong -2$, (see **Fig. 11**) have been calculated. R_{drift} vs. temperature at various bias is reported in **Fig. 12**. It is found that influence of the temperature in terms of R_{drift}/R_{on} is not very critical, **Fig. 13**. We demonstrate that by a simultaneous yet separate calibration of the intrinsic MOSFET excellent accuracy compared to any other approach can be obtained to model the temperature dependence of DMOS characteristics.

Quasi-analytical DC modelling and calibration with MESDRIFT - It is worth mentioning that MESDRIFT enables the simplest yet efficient extension of low-voltage MOS advanced models for HV device simulation. With a low voltage BSIM3v3 model, calibrated on intrinsic channel characteristics revealed by MESDRIFT, connected in series with a bias-dependent resistor the values of which are provided by MESDRIFT, high accuracy in DC modelling (<10% max error in I_D, R_{on}, and <15% in (trans)conductance, **Figs. 14** and **15**) are obtained over a wide range of temperature, with physical values of the model parameters. Quasi-analytical detailed expressions R_{drift} can be then developed [4], validated and improved with MESDRIFT, for more advanced and accurate simulation.

Bias-dependent capacitance modelling with MESDRIFT - Excellent news with MESDRIFT for AC modelling and simulations is that the V_K voltage can be exploited in order to analytically describe the particular dependence of C_{GS} and C_{GD} capacitances associated with DMOS transistors. The MESDRIFT small signal equivalent circuit is given in **Fig. 16**. Numerical simulations of capacitances and S-parameters measurements have been carried out for cross validations (**Fig. 17**) and modelling of the specific peaks observed in C_{GS} characteristics of DMOS devices.

Self heating characterization - Investigation of transients and self-heating in DMOS transistors with MESDRIFT are briefly presented in **Fig. 18** and **Fig. 19**. Both $V_D(t)$ and $V_K(t)$ transients after abruptly switching V_G, are recorded and compared in order to identify best conditions for pulsed measurements in order to provide characteristics free of self-heating and separately evaluate self-heating in intrinsic channel and drift region. For our DMOS devices, it is found that a pulse duration, τ_{pulse}, less than 10μs acceptably eliminates the self heating, **Fig. 19**.

Hot carrier investigations with MESDRIFT - One of the most valuable insights offered by MESDRIFT concern the hot carrier degradation of HV MOSFETs. In **Figs. 20** and **21** it is shown how one can distinguish between *drift region* and *intrinsic channel* degradations with MESDRIFT. By comparing stress impact with: (i) high V_G, high V_D and (ii) high V_D, maximum of body current, I_B, we have validated with MESDRIFT that in DMOS transistors the degradation can be assisted by both electron and/or hole injection, like recently claimed in [5]. By comparing results of **Fig. 20** and Fig. 21, one can observe that R_{drift} is increased (**Fig. 20**) or decreased (**Fig. 21**) depending of the type of the stress. Furthermore, MESDRIFT highlights that stress at I_{Bmax} results in more degradation of the intrinsic channel, compared with stress at V_{Gmax}. Finally, it should be noted that such detailed analysis of hot carrier degradation is almost impossible conventionally (compare *only ΔRon* in **Figs. 20** and **21**) without help of MESDRIFT.

Conclusion
In conclusion, the proposed new MESDRIFT structure fully supports new DC and AC characterization methods that are simple, accurate and universal, because independent on the drift architecture of any asymmetrical HV MOSFETs. New insights into the HV device physics are provided.

References:
[1] M. Trivedi, P. Khandelwal, K. Shenai, IEEE Transactions on Electron. Dev., Vol. 46, 1999, pp. 1794 – 1802.
[2] J. Jaejune, T. Amborg, Y. Zhiping; R.W. Dutton., SISPAD '99. 1999, pp. 15 – 18.
[3] C.H. Kreuzer, N. Krischke, P. Nance, IEDM Techn. Digest, 1996, pp. 489 – 492.
[4] N. Hefyene, E. Vestiel, S. Frere, C. Anghel, A.M. Ionescu, R. Gillon, SISPAD 2002, to appear.
[5] P. Moens, M. Tack, R. Degraeve, G. Groeseneken, IEDM Techn. Digest 2001, pp. 39.6.1 -39.6.4

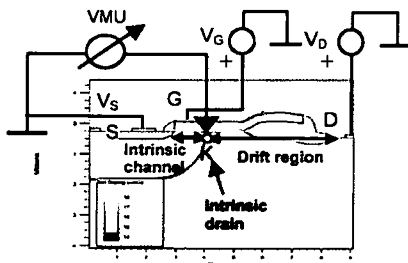


Fig. 1 Cross section of MESDRIFT test structure and associated HP4156 measurement set-up. K-contact (n+ type) is designed in the drift region (close to pn junction) and its width, W_K, is negligible compared to DMOS width, W.

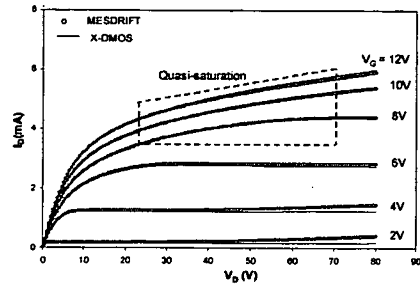
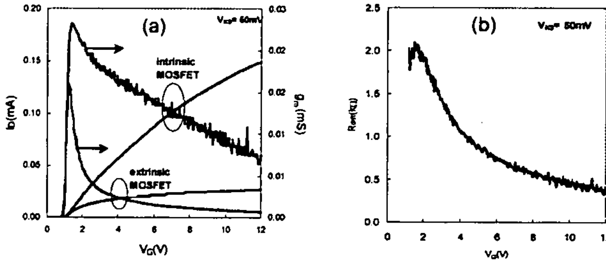


Fig. 2 Typical output characteristics, I_{DS} vs. V_{DS}, of X-DMOS (solid) and MESDRIFT (symbol) (both with W=40μm): very good agreement is observed (including quasi-saturation region) demonstrating that the K-contact does not significantly change the HV MOSFET characteristics.



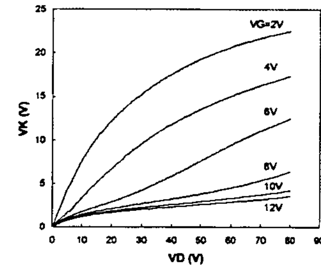


Fig. 3 a) Intrinsic and extrinsic I_D-V_G and g_m-V_G at V_{KS}=V_{DS}=50mV, measured with MESDRIFT mirroring X-DMOS, b) Extracted R_{drift} at low V_D (=50mV).

Fig. 4 Intrinsic drain (key) voltage, V_K, vs. V_D with V_G as parameter, experimentally revealed by MESDRIFT.

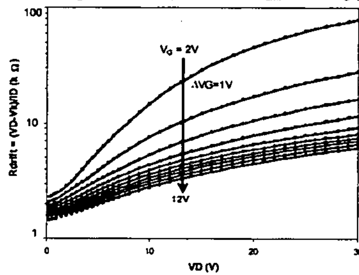


Fig. 5 Drift resistance, R_{drift} vs. V_D with V_G as parameter, as experimentally extracted with MESDRIFT (X-DMOS) at room temperature.

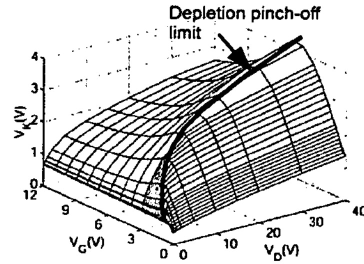


Fig. 6 Intrinsic drain voltage, V_K, predicted by numerical simulation with calibrated 2D structure, calibrated on X-DMOS characteristics. Inset: drift depletion pinch-off limit highlighted.

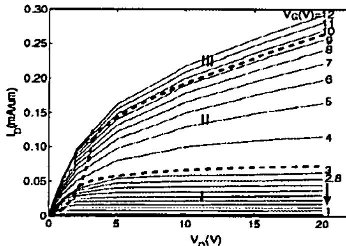


Fig. 7 Output characteristics of X-DMOS: different saturation mechanisms are identified in regions (I), (II) and (III) with the help of intrinsic drain voltage, V_K.

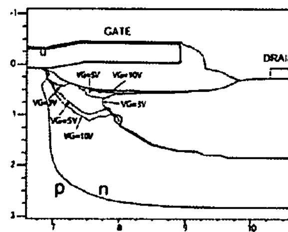


Fig. 8 Cross section of X-DMOS with depletion region limits corresponding to bias of regions (I), (II), (III) from Fig. 4 (numerical simulation).

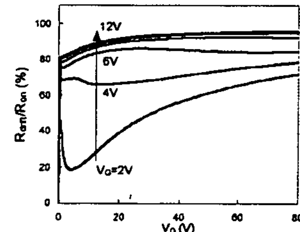


Fig. 9 R_{drift}/R_{on} as function of X-DMOS bias: R_{drift} dominates R_{on} if V_D and/or V_G bias increase (where $R_{channel}$ < R_{drift}): experimental data from MESDRIFT (X-DMOS).

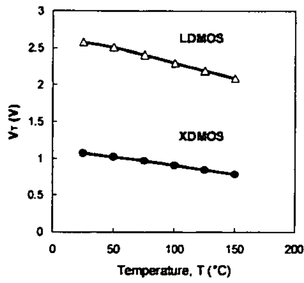


Fig. 10 Threshold voltage, V_T, vs. temperature, T, for X- and L-DMOS.

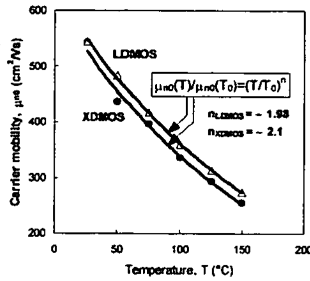


Fig. 11 Low field mobility, μ_{no}, vs. temperature, T, for X- and L-DMOS.

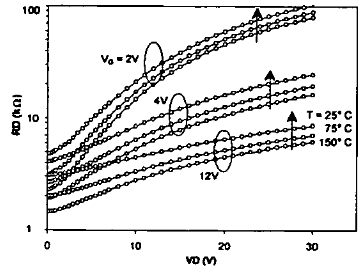


Fig. 12 R_{drift} vs. V_D at constant V_G with the temperature, T, as a parameter.

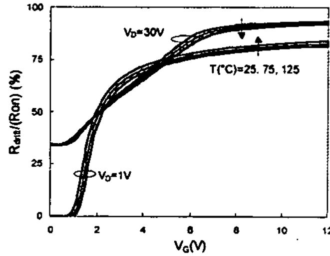


Fig. 13 Influence of temperature on R_{drift}/R_{on} characteristics revealed by MESDRIFT.

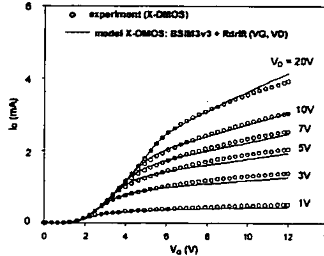


Fig. 14 Experiment vs. BSIM3v3 calibrated with MESDRIFT: I_D-V_G.

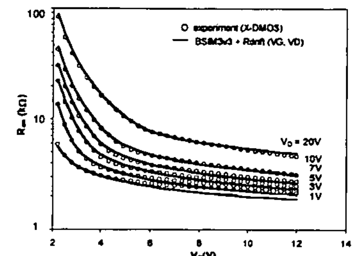


Fig. 15 Experiment vs. BSIM3v3 calibrated with MESDRIFT: R_{on}-V_G.

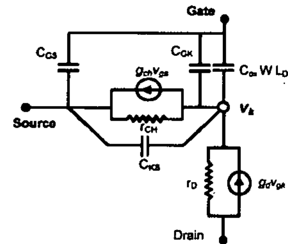


Fig. 16 Small signal equivalent schematic for AC modelling of X- and L-DMOS transistors, that exploits V_K to deduce the values of C_{GS} and C_{GD} capacitances (L_D is drift region length under the field plate)

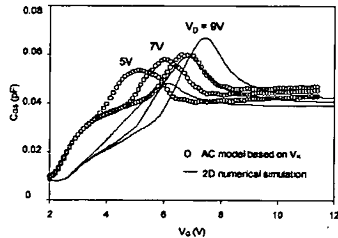


Fig. 17 C_{GS}-V_{GS} with V_D as parameter. The specific DMOS signature is the peak at given V_{DS} (increasing with V_{DS}) that can be modelled with V_K (V_G,V_D) (MESDRIFT).

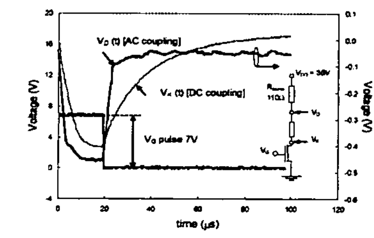


Fig. 18 Dynamic behaviour of MESDRIFT (X-DMOS) highlighted by a simple pulsed measurement set-up designed to study self-heating in HV MOSFETs: V_D and V_K time constants are different.

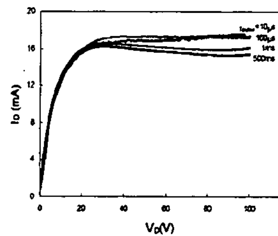


Fig. 19 Effect of τ_{pulse} (pulse duration) on the reconstructed output characteristics of X-DMOS. The self heating appears acceptably eliminated when τ_{pulse} < 10µs.

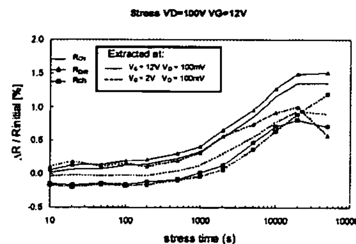


Fig. 20 Specific degradations of R_{ch}, R_{drift}, R_{on} induced by hot carrier measurements conducted on MESDRIFT with V_D=100V and V_G=12V: *ΔR_{drift}>0, R_{drift} and R_{on} are similarly degraded.*

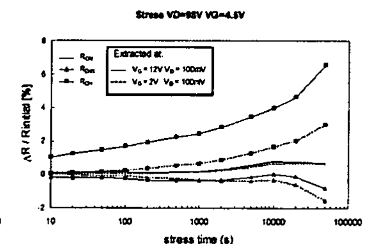


Fig. 21 Specific degradations of R_{ch}, R_{drift}, R_{on} induced by hot carrier measurements conducted on MESDRIFT with V_D=98V and V_G=4.5V (at max I_{body}): *ΔR_{drift}<0, R_{ch} is significantly more degraded* than in Fig. 20.

Bias-dependent drift resistance modeling for accurate DC and AC simulation of asymmetric HV-MOSFET

N. Hefyene[1], E. Vestiel[2], S. Frere[2], C. Anghel[1], A.M. Ionescu[1], and R. Gillon[2]
[1]Swiss Federal Institute of Technology Lausanne, Switzerland
[2]Alcatel Microelectronics, Oudenaarde, Belgium

High Voltage (HV) Lateral MOSFETs are extremely interesting for automotive and RF applications requiring more accurate analytical models for advanced IC design and simulation. A key bottleneck for the modeling of LDMOS devices is the bias-dependence of their drift resistance, $R_D(V_D,V_G)$. This dependence is specific to the architecture of extended drain region, particularly engineered to provide increased breakdown voltages. Specific phenomena dictated by the drift region like quasi-saturation [1] (the origins of which are related to JFET-like 2-D depletion region modulation, carrier velocity saturation, etc) are reflected in the bias evolution of the drift resistance and thus, very difficult to be captured in an analytical compact model.

This work reports on the modeling, 2D-numerical simulation and experimentally extracted $R_D(V_D,V_G)$, based on a new dedicated test structure that provides unique access *to measure* the intrinsic MOSFET drain-voltage [2], V_K. Two Lateral HV MOSFET architectures are investigated: the first one is self-aligned n-channel LDMOS and, the second one, a drain-extended n-channel (XDMOS), both with up to 100V breakdown voltage capability. Figs. 1 a and b show the 2-D cross-section of the investigated architectures and the corresponding intrinsic drain-voltage locations (*K-point*). In order to extract and model the R_D evolution with the external biases V_D and V_G, first, 2-D numerical simulation was carried out. DC characteristics were simulated with ATLAS and used to extract $R_D(V_G,V_D)$ in a straightforward manner, based on the intrinsic drain-voltage value that provides the calculation of the variable drift voltage drop at each V_D: $R_D \equiv R_{Ddrift} = (V_D - V_K)/I_D$.

The new test structures have been designed and fabricated by Alcatel Microelectronics to directly monitor the V_K potential and confirm the intrinsic drain-voltage concept usefulness. It consists in a HV device architecture with an extra n+ small contact (*K-contact*) added at the end of the intrinsic channel, Fig. 2 a and b. The K-contact dimensions are much smaller than the transistor width, aiming to minimize its impact on the overall transistor characteristics. With the proposed design, we report differences less than 10% in all regimes of operation between the original HV devices and the test structures with K-contact.

A measurement setup based on a HP4156 parameter analyzer has been used to measure the test structures: while varying the bias of the DMOS transistor in all operation regimes, we have monitored with a high impedance voltmeter the potential of the K-contact. Based on the experimentally monitored evolution of V_K with V_D and V_G, $R_D(V_D,V_G)$ has been extracted and the results are reported together with the numerically simulated drift resistance in Fig. 3. At low V_G, a depleted area is formed in the drift zone, below the gate oxide or the bird's beak, depending on the V_D values, which results in an increased equivalent resistance for this part of the drift zone. By increasing the V_G voltage, due to the combined effects of the accumulation and carrier injection phenomena, this depleted area could disappear. Consequently the equivalent resistance decreases. An unusual behavior is reported for low V_D values (less than 1V), when R_D decreases (Fig. 3). This trend is related to the change of the conduction mechanism from surface into volume, resulting in an equivalent mobility increase. When extracting R_D from the test devices, this phenomenon cannot be observed (see Fig. 2 a) due to the location and lateral dimensions of the n^+ implant. It is observed that experimental curves correctly follow the predictions of numerical simulations, which confirms the validity of the V_K concept.

The following continuous mathematical, quasi-empirical expression has been deduced for the drift resistance:

$$R_D(V_D, V_G, T) = \left(r_{D0} + \frac{r_{D1}}{(\gamma V_G + 1)} \ln\left(e^{(\beta_1 V_G + \beta_0)V_D - (\delta_2 V_G^2 + \delta_1 V_G + \delta_0)} + 1 \right) \right) \left(\frac{T}{T_0} \right)^{\left(\frac{1}{m V_D + n} \right)} \quad (1)$$

where, r_{D0}, r_{D1}, γ, β_1, β_0, δ_2, δ_1 and δ_0 are room temperature model parameters, while m and n are parameters for the temperature dependence of R_D. Fig. 4 shows that with this approach R_D model accuracy is better than 15% for the max error, and, better than 4% for the mean error, over all regimes of operation, *including quasi-saturation*. Fig. 5 reports the good fitting accuracy (<25% for max error, including quasi-saturation) achieved by combining a BSIM3v3 core model, calibrated on intrinsic channel characteristics, in series with the proposed bias-dependent R_D model, calibrated on data measured on the new test structure.

A final key original finding is that V_K voltage can be used in order to properly model the HV DMOS bias-dependent capacitances, C_{GS} and C_{GD}. Based on the DMOS small-signal AC circuit reported by [3], including the possibility to relate C_{GS} and C_{GD} to V_K, drift and channel resistances, r_d and r_{ch}, respectively, we have derived the following analytical expressions:

$$C_{GS} \cong \frac{\left(\frac{r_d}{r_{ch}}\right)\cdot\left(1 + \frac{r_d}{r_{ch}} + \left(\frac{\partial I_D}{\partial V_K}\cdot\frac{\partial V_K}{\partial V_{GS}}\right) r_d\right)}{\left(1 + \left(\frac{r_d}{r_{ch}}\right) + \left(\frac{\partial I_D}{\partial V_K}\cdot\frac{\partial V_K}{\partial V_{GS}}\right)\cdot\left(1 - \frac{\partial V_K}{\partial V_{GS}}\right)^{-1} r_d\right)^2} \cdot C_{ox} \cdot W \cdot L_{eff} \qquad C_{GD} \cong \frac{\left(1 + \left(\frac{\partial I_D}{\partial V_K}\cdot\frac{\partial V_K}{\partial V_{GS}}\right)\cdot\left(1 - \frac{\partial V_K}{\partial V_{GS}}\right)^{-1}\right)\cdot\left(1 + \frac{r_d}{r_{ch}} + \left(\frac{\partial I_D}{\partial V_K}\cdot\frac{\partial V_K}{\partial V_{GS}}\right) r_d\right)}{\left(1 + \left(\frac{r_d}{r_{ch}}\right) + \left(\frac{\partial I_D}{\partial V_K}\cdot\frac{\partial V_K}{\partial V_{GS}}\right)\cdot\left(1 - \frac{\partial V_K}{\partial V_{GS}}\right)^{-1} r_d\right)^2} \cdot C_{ox} \cdot W \cdot L_{eff}$$

These models need both $V_K(V_G, V_D)$ and its derivatives, in all regions of operations, which is uniquely achievable by the use of the new proposed test structure. Typical results, able to describe the untypical peaks observed in the DMOS capacitances (related to the evolution of the drift depleted regions, onset of quasi-saturation and lateral doping profiles [4]) are reported in Fig. 6. S-parameter measurements (including pad de-embedding) have been used in order to validate the model predictions.

In conclusion, we demonstrated the usefulness of the intrinsic drain-voltage concept for accurate DC (bias-dependent R_D) and AC modeling (bias-dependent C_{GS} and C_{GD}) of HV asymmetric DMOS architectures, based on measurements carried out on a new dedicated structure and fully confirmed by 2-D numerical simulations.

[1] Trivedi, M.; Khandelwal, P.; Shenai, K. Electron Devices, IEEE Transactions on , Vol. 46, 1999, pp. 1794 – 1802.
[2] C. Anghel, N. Hefyene, A.M. Ionescu, S. Frere, R. Gillon, M. Vermandel, B. Bakeroot and J. Doutreloigne, C. Maier, Y. Mourier. ESSDERC 2001, Nuremberg, Germany, Proc. of, pp.399-402, Sep. 2001.
[3] C. M. Liu and J. B. Kuo, IEEE Trans. El. Dev., Vol. 44, No. 7, July 1997.
[4] S. F. Frere, J. Rhayem, H. O. Adawe, R. Gillon, M. Tack and A. J. Walton, ESSDERC 2001, Nuremberg, Germany, Proc. of, pp.399-402, Sep. 2001.

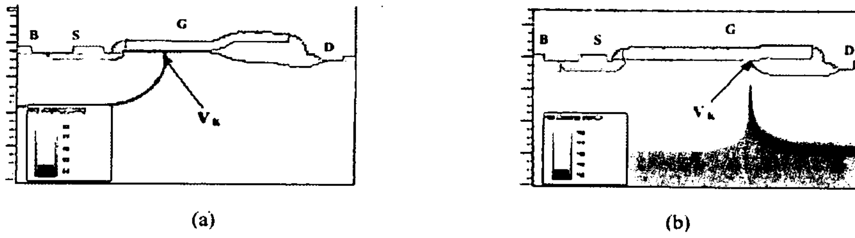


Fig. 1. Cross section of: (a) n-channel LDMOS and (b) n-channel XDMOS architectures. Inset: K-point location.

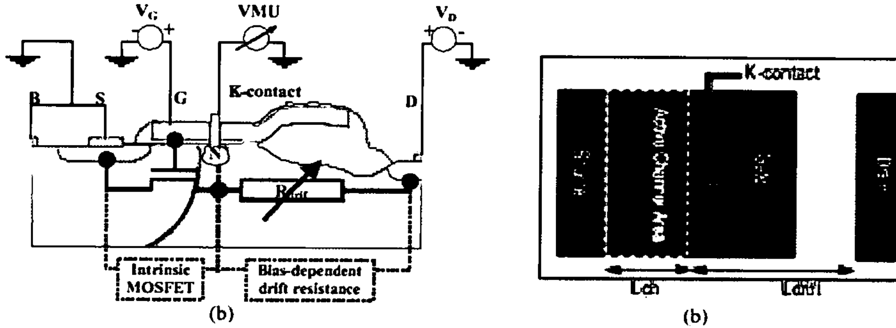


Fig. 2. (a) Cross-sectional view of the new test structure with n^+ implant located at the K-point and measurement configuration used to monitor the intrinsic drain potential, V_K. (b) Top view of the same structure.

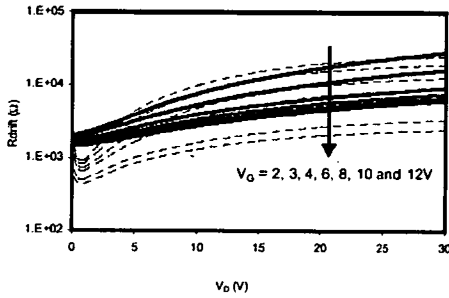


Fig. 3. $R_D(V_D, V_G)$ characteristics for L-DMOS: Numerical simulation (doted lines) compared to measurements using new test structure (solid lines).

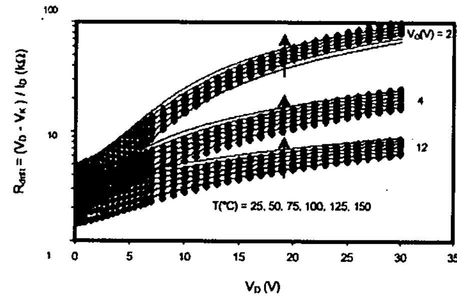


Fig. 4. $R_D(V_D, V_G)$ of n-XDMOS: experiment (symbols) compared with our model (solid line) for various temperatures (25 up to 150C).

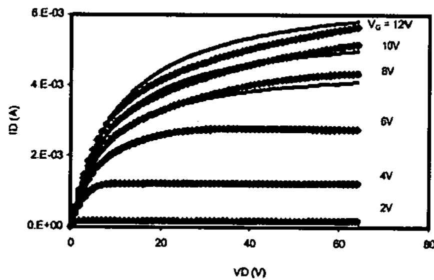


Fig.5. Comparison between measured (symbols) and modeled (solid line) output characteristics of X-DMOS. The model uses a core BSIM3v3 for intrinsic MOSFET, in series with $R_D(V_D, V_G)$ model.

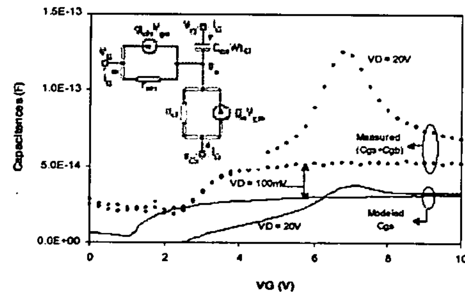


Fig.6. Measured $C_{GS}+C_{GB}$ (circles) and modeled C_{GS} (solid lines) characteristics of a n-XDMOS architecture. Inset: DMOS small-signal equivalent circuit used for the C_{GS} calculations based on V_K.